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Texas Instruments OMAP™ Family of Products

Version X

Technical Reference Manual

PRELIMINARY

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TI Embedded Processors Wiki —Texas Instruments Embedded Processors Wiki

Established to assist developers using the many Embedded Processors from Texas Instruments to get started, help each other innovate, and foster the growth of general knowledge about the hardware and software surrounding these devices.

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Register, Field, and Bit Calls

The naming convention applied for a call consists of:

- For a register call: *<Module name>.<Register name>*; for example: UART.UASR
- For a bit field call:
  - *<Module name>.<Register name>[End:Start] <Field name> field*; for example, UART.UASR[4:0] SPEED bit field
  - *<Field name> field <Module name>.<Register name>[End:Start]*; for example, SPEED bit field UART.UASR[4:0]
- For a bit call:
  - *<Module name>.<Register name>[pos] <Bit name> bit*; for example, UART.UASR[5] BIT_BY_CHAR bit
  - *<Bit name> bit <Module name>.<Register name>[pos]*; for example, BIT_BY_CHAR bit UART.UASR[5]

To help the reader navigate the document, each register call is hyperlinked to its register description in the register manual section. After each register description, a table summarizes all hyperlinked register calls.

To navigate in the PDF documents, see Acrobat Reader Tips.

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Coding Rules

The programming models or code listings follow the rules:

Type	Definition	Example
File	Starts with the module name	PRCM_test1.c MCBSP1_init.h
Variable	Global variables are prefixed by "g_" Pointers are prefixed by "p" Global pointers are prefixed by "g_p"	g_SDMA_LogicalChan pAddrCounter g_pSDMA_LogicalChan
Function	Starts with the module name	PRCM_SetupClocks() ArmIntC_MaskInterrupts()
Typedef	Ends with "_t"	PRCM_Struct_t
Definition	Starts with the module name and is followed by the register name	#define SMS_ERR_TYPE *((volatileUint32*)0x680080F4) #define MCBSP2_RCR1_REG *((volatile Uint32*)0x4807401C)
Enumeration	Starts with the module name	Typedef enum DMA_Mode_Label { INPUT_MODE OUTPUT_MODE } DMA_Mode_t;

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Flow Chart Rules

Flow charts follow the following rules:

Shape	Name	Definition
	Process	Any computational steps or processing function of a program; defined operation(s) causing change in value, form, or location of information
	Decision	A decision or switching-type operation that determines which of a number of alternate paths is followed
	Predefined process or sub-process	One or more named operations or program steps specified in a subroutine or another set of flow charts
	Data or I/O	General I/O function; information available for processing (input) or recording of processed information (output)
	Terminator	Terminal point in a flow chart: start, stop, halt, delay, or interrupt; may show exit from a closed subroutine
	Annotation	Additional descriptive clarification, comment
	On page connector (reference)	Exit to, or entry from, another part of chart in the same page
	Off page connector (reference)	The flow continues on a different page.
	Summing Junction	Logical AND
	Or	Logical OR
	Parallel mode (ISO)	Beginning or end of two or more simultaneous operations
	Flow Line	Lines indicate the sequence of steps and the direction of flow.

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Acrobat Reader Tips

Acrobat includes two methods to search for words in a PDF:

- The Find toolbar provides a basic set of options to locate a word in the current PDF.
- The Search window lista words or partial words that match your text in the current PDF.

These guidelines apply to Acrobat Reader 5.x, 6.0, and 7.0.

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2. To display the Find toolbar, right-click in the toolbar area and select Find.
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4. From the Find Options menu, select options as desired.
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1. Open the document.
2. Click the Search button on the File toolbar or right-click on your document and select Search.
3. Type the word, words, or part of a word for which you want to search.
4. Click Search.
5. The results appear in page order and, if applicable, show a few words of context. Each result displays an icon to identify the type of occurrence. All other searchable areas display the Search Result icon.
6. To display the page that contains a search result, click an item in the Results list. The occurrence is highlighted.
7. To navigate to the next result, choose Edit > Search Results > Next Result (or Ctrl+G).
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  - Right-click the toolbar area, and then choose *Navigation*.
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NOTE: This navigation tip is useful to return to your previous view after clicking on a register call hyperlink.

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History

The following table summarizes the OMAP543x ES2.0 TRM versions.

Version	Literature Number	Date	Notes
V	SWPU249	May 2013	See (1)
W	SWPU249	July 2013	See (2)
X	SWPU249	July 2013	See (3)

(1) Public version of *OMAP543x Multimedia Device Silicon Revision 2.0 Technical Reference Manual*, version V (SWPU249V) — initial release to the public domain.

(2) Public version of *OMAP543x Multimedia Device Silicon Revision 2.0 Technical Reference Manual*, version W (SWPU249W)
Chapters impacted by update to version W:
- Chapter 1: Introduction
- Chapter 3: Power Reset and Clock Management
- Chapter 19: Control Module

(3) Public version of *OMAP543x Multimedia Device Silicon Revision 2.0 Technical Reference Manual*, version X (SWPU249X)
Chapters impacted by update to version X:
- Preface
- Chapter 10: Display Subsystem

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Introduction

This chapter introduces the features, subsystems, and architecture of the OMAP543x high-performance multimedia device.

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1.2 OMAP5430 Environment 289
1.3 OMAP5430 Description 290
1.4 OMAP5430 Package-On-Package Concept 302
1.5 OMAP543x Family and Device Identification 303

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1.1 Overview

The OMAP543x high-performance multimedia application device is based on enhanced OMAP™ architecture and uses 28-nm technology.

- The architecture is designed to provide best-in-class CPU performance, video, image, and graphics processing for a broad range of multimedia-rich applications. The device supports the following functions:
  - Streaming video up to full high definition (Full-HD) (1920 × 1080p, 60 fps)
  - Stereoscopic video recording and playback up to Full-HD (1920 × 1080p, 30 fps)
  - 2-dimensional (2D)/3-dimensional (3D) gaming and video contents
  - Video conferencing
  - High-resolution still image (up to 24 MP)
  - Full-HD video capture and encode (1920 × 1080 resolution)
  - Efficient support for web browsing
- The device supports high-level operating systems (OS) such as:
  - Android™
  - Linux®

  and others.
- The device is composed of the following major subsystems:
  - Cortex™-A15 microprocessor unit (MPU) subsystem, including two ARM® Cortex-A15 cores
  - Digital signal processor (DSP) subsystem
  - Image and video accelerator high-definition (IVA-HD) subsystem
  - Cortex™-M4 image processing unit (IPU) subsystem, including two ARM Cortex-M4 microprocessors
  - Display subsystem
  - Audio back-end (ABE) subsystem
  - Imaging subsystem (ISS), consisting of image signal processor (ISP) and still image coprocessor (SIMCOP) block
  - 3D-graphics accelerator subsystem, including POWERVR™ SGX544 dual-core
  - Debug subsystem
- The device includes state-of-the-art power management techniques required for high-performance mobile products.
- Comprehensive power management is integrated into the device.
- The device also integrates:
  - On-chip memory
  - External memory interfaces
  - Memory management
  - Level 3 (L3) and level 4 (L4) interconnects
  - System and connecting peripherals

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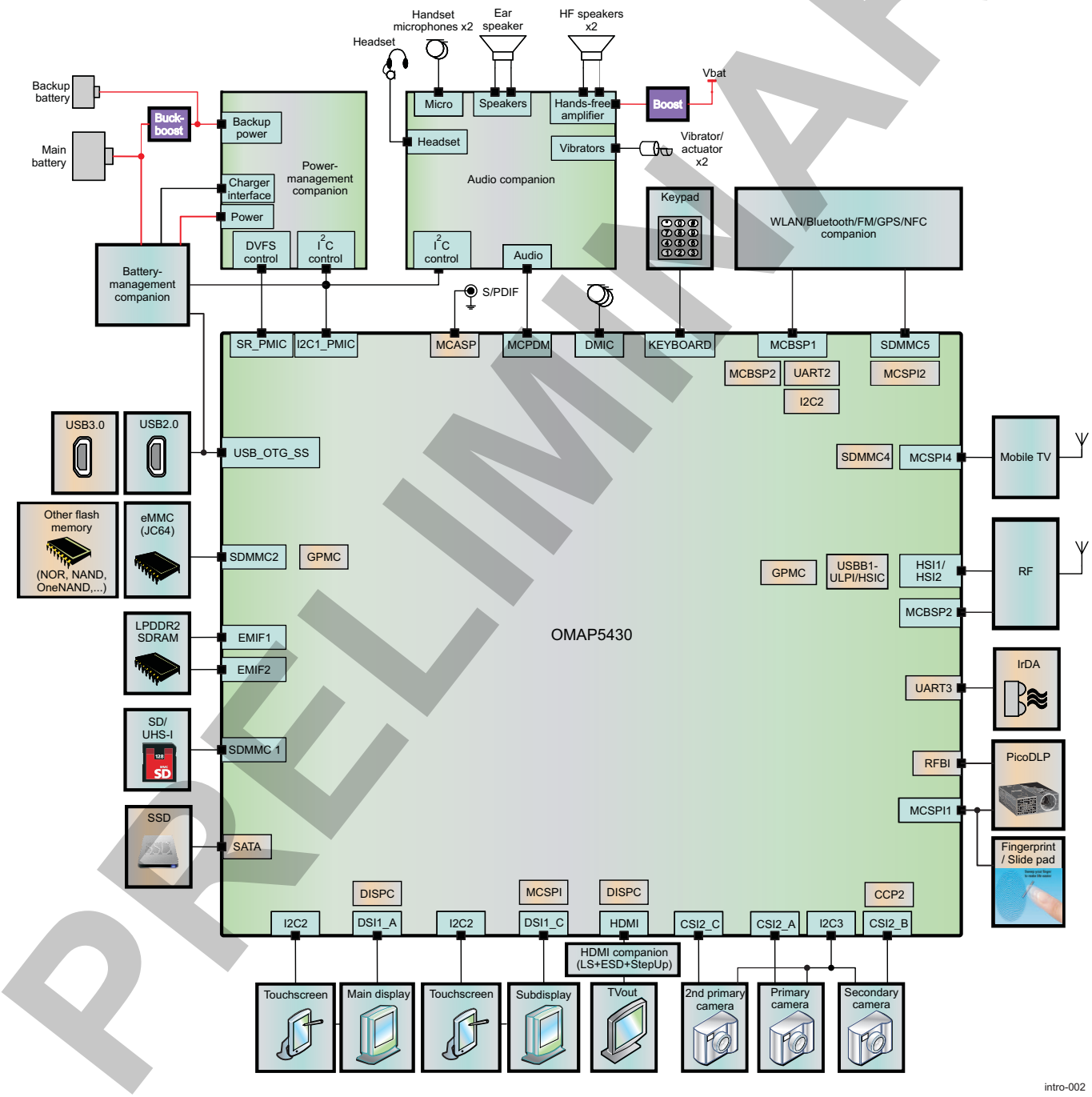
1.2 OMAP5430 Environment

This section provides an overview of the OMAP5430 high-tier environment. See more information about the OMAP5432 device in Appendix A, *OMAP5432 Multimedia Device*.

The device is associated with power-management companion and audio companion integrated circuits (ICs). TI provides a global solution with the TWL6035/TWL6037 power-management- and TWL6041 audio-companion devices.

Figure 1-1 is an overview of a nonexhaustive environment for the high-tier OMAP5430 device.

Figure 1-1. OMAP5430 High-Tier Environment



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1.3 OMAP5430 Description

The subsystems described in the current subsection apply to the OMAP5430 high-tier device. For more information about the OMAP5432 device see Appendix A, *OMAP5432 Multimedia Device.*

The OMAP5430 device is offered in a 980-ball, 14 × 14 -mm, 0.4-mm bottom ball pitch package. Some balls (240 balls, 0.5-mm pitch) are available at the top of the device to allow LPDDR2 memory stacking.

Figure 1-2 is the block diagram of the OMAP5430 device.

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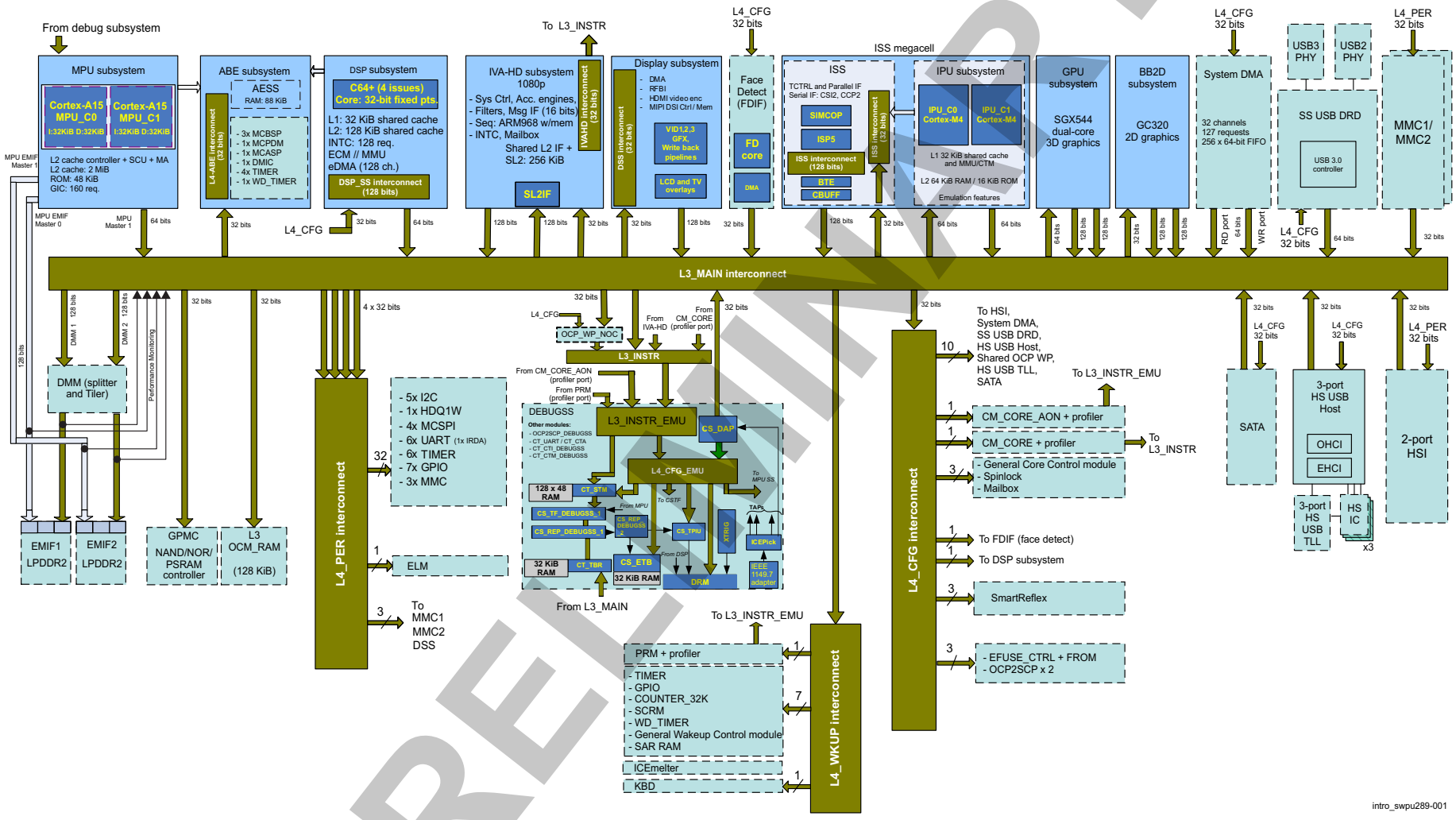
Figure 1-2. OMAP5430 Block Diagram



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1.3.1 MPU Subsystem Description

The Cortex-A15 MPU subsystem integrates the following submodules:

- ARM Cortex-A15 MPCore
  - Two central processing units (CPUs)
  - ARM Version 7 ISA: Standard ARM instruction set plus Thumb®-2, Jazelle® RCT Java™ accelerator, hardware virtualization support, and large physical address extensions (LPAE)
  - Neon™ SIMD coprocessor and VFPv4 per CPU
  - Interrupt controller with up to 160 interrupt requests
  - One general-purpose timer and one watchdog timer per CPU
  - Debug and trace features
  - 32-KiB instruction and 32-KiB data level 1 (L1) caches per CPU
- Shared 2-MiB level 2 (L2) cache
- 48-KiB bootable ROM
- Local power, reset, and clock management (PRCM) module
- Emulation features
- Digital phase-locked loop (DPLL)

1.3.2 DSP Subsystem Description

The DSP subsystem contains the following submodules:

- TMS320DM64™ 32-bit fixed DSP core for audio processing and general-purpose imaging and video processing. It is backward compatible with existing C64x™ video codecs.
  - 32-KiB L1 4-way set associative cache
  - 128-KiB L2 8-way set associative cache
- Enhanced direct memory access (DMA_DSP) engine with 128 channels for video/audio data transfer between IVA3 local memories and external SDRAM memories or peripherals
- Interrupt controller (INTC) with up to 128 interrupt requests
- Memory management unit (MMU) for address management. It translates virtual addresses handled by the DSP CPU into physical addresses.
- DPLL

The DSP subsystem allows direct access to the ABE subsystem, and has emulation capabilities.

1.3.3 IVA-HD Subsystem Description

The IVA-HD subsystem is a set of video encoder/decoder hardware accelerators that supports:

- Real-time video encoding and decoding
- MPEG4/H264 up to 1920 × 1080p @ 60 fps
- MPEG2 decoding up to 1920 × 1080p @ 60 fps
- Supporting JPEG encode/decode up to 96 MP/s

The IVA-HD subsystem is composed of:

- Improved motion estimation acceleration engine (IME3), which is used in encoding processing
- Improved loop filter acceleration engine (ILF3), which performs deblocking filtering
- Improved sequencer (ICONT1) based on the ARM968E-S™ microcontroller. It includes memory and INTC and is used as a primary sequencer.
- Intraprediction estimation engine (IPE3). It is used in encoding processing.
- Calculation engine (CALC3), which performs transform and quantization calculations
- Motion compensation engine (MC3), which creates an interprediction macroblock with given motion vectors and modes from the reference data
- Entropy coder/decoder (ECD3), which uses Huffman and arithmetic codes during the process of

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encoding and decoding the stream

- Video DMA processor (ICONT2), which is also based on the ARM968E-S microcontroller and can be used as secondary sequencer
- Video DMA engine (vDMA), which is a DMA engine for data transmission between external memories and shared L2 memory
- Synchronization box (SYNCBOX) embedded in each hardware accelerator and in both ICONTs
- Mailbox for communication between IVA-HD and external to it processors (DSP, MPU, and IPU)
- Shared L2 interface and memory
- Video local interconnect for connection between the submodules of the IVA-HD
- IVA-HD system control module (SYSCTRL), which controls the clocks in the subsystem and PRCM handshaking

The IVA-HD subsystem can process three data formats for internal data: picture or slice, macroblock header, and residual data.

The IVA-HD supports the following formats:

- MPEG-1/-2/-4 such as MPEG-2 MP, HP, and MPEG-4 as SP/ASP
- DivX 5.02 and above
- Sorenson Spark (decode)
- H.263 P0 (encode and decode) and P3 (decode)
- H.264 Annex G (scalable baseline profile up to 720p)
- H.264 BL/MP/HP
- H.264 Annex H (partial)
- Stereoscopic video
- JPEG (encode/decode)
- VC-1 SP/MP/AP
- AVS-1.0
- RealVideo® 8/9/10 (decode only)
- On2® VP6.2/VP7 (decode only)

1.3.4 Image Processing Unit (IPU) Subsystem

The Cortex-M4 IPU subsystem includes the following components:

- Two Cortex-M4 CPUs
- ARMv7E-M and Thumb-2 instruction set architecture
- Hardware division and single-cycle multiplication acceleration
- Dedicated INTC with up to 63 physical interrupt events with 16-level priority
- Two-level memory subsystem hierarchy
  - L1
    32-KiB shared cache memory
  - L2 ROM + RAM
    - 64-KiB RAM
    - 16-KiB bootable ROM
- Cortex-M4 system bus directly connected to the ISS interconnect
- MMU for address translation
- Integrated power management
- Emulation feature embedded in the Cortex-M4

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1.3.5 Display Subsystem

The display subsystem provides the control signals required to interface the OMAP system memory frame buffer (SDRAM) directly to the displays. It supports hardware cursor, independent gamma curve on all interfaces, multiple-buffer, and programmable color phase rotation. The display subsystem allows low-power display refresh and arbitration between normal and low-priority pipelines.

The display subsystem consists of the following sections:

- **Display controller:** Reads and displays the encoded pixel data stored in memory and writes the output of one of the overlays or one of the pipelines into the system memory. The display controller supports the following components:
  - Three video pipelines, one graphic pipeline, and one write-back pipeline. The graphic pipeline supports pixel formats such as: ARGB16-4444, RGB16-565, ARGB16-1555, ARGB32-8888, RGBA32-8888, RGB24-888, and BITMAP (1, 2, 4, or 8 bits per pixel). It allows selection of the color-depth expansion.
  - Write-back pipeline: Uses poly-phase filtering for independent horizontal and vertical resampling (upsampling and downsampling). It allows programmable color space conversion of RGB24 into YUV4:2:2-UYVY, YUV4:2:2-YUV2, or YUV4:2:0-NV12 or NV21, and selection of color-depth reduction from RGB24 to RGB16.
  - Three LCD outputs, each one with dedicated overlay manager, for support of active matrix color displays (up to 24-bit interface).
  - One TV output with dedicated overlay manager to support HDMI video port
  - All outputs (three LCDs and one TV), besides other interfaces, are available through the parallel CMOS interface for MIPI®-DPI 2.0 support.
  - Own direct memory access (DMA) engine
- **Remote frame buffer interface (RFBI) module:**
  - Support for MIPI-DBI protocol
  - 8-/9-/12-/16-bit parallel interface
  - Programmable pixel modes and output formats
- **Two MIPI display serial interfaces (DSI)** with the following main features:
  - Support for MIPI-DSI v01.01.00 (four data-lane complex I/Os)
  - Support for video mode and command mode
  - Data interleaving support for synchronous and asynchronous streams
  - Bidirectional data link support
- **High-definition multimedia interface (HDMI) encoder** with the following main features:
  - HDMI 1.4a, HDCP 1.4, and DVI 1.0 compliant

    Includes support for the 3D stereoscopic frame-packing formats of HDMI v1.4a standard (720p, 50 Hz; 720p, 60 Hz; 1080p, 30 Hz; and side-by-side half structure: 1080p, 60 Hz)
  - Deep-color mode support (10 bit for up to 1080p and up to 12 bit for 1080i/720p)
  - Expanded support for color spaces (xvYCC601, xvYCC709, sYCC601, AdobeYCC601, and AdobeRGB)
  - Support for uncompressed multichannel audio
  - Integrated high-bandwidth digital content protection (HDCP) encryption engine for transmitting protected audio and video content
  - Integrated transition minimized differential signaling (TMDS) and TERC4 encoders for data island support

1.3.6 ABE Subsystem

The ABE subsystem handles audio processing for the application. It manages the audio and voice streams between the MPU subsystem and/or DSP, and the physical interfaces.

The ABE subsystem allows:

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- Buffering of audio samples
- Mixing audio with voice downstream and/or microphone upstream (sidetone)
- Postprocessing of equalization, 3D effects, bass-boost

The ABE subsystem consists of:

- Audio engine (AE) subsystem, which performs real-time signal processing such as:
  - Muxing and mixing voice and data streams
  - Postprocessing operations such as sampling rate conversion, volume control, smooth muting, side tone equalization, 3D effects, bass-boost
  - Execution of whole data transfers in the ABE subsystem using audio traffic controller (ATC)

    The AE subsystem includes an AE and has the following on-chip memories available: 64-KiB data memory (DMEM); 6-KiB coefficient memory (CMEM); and 18-KiB sample memory (SMEM).

    The ATC manages the data movement in the ABE subsystem and is in charge of interrupt generation to the DSP and MPU subsystems.
- Four general-purpose timers and one watchdog timer
- Peripheral interfaces:
  - Three multichannel buffered serial ports (MCBSP) for inter-IC sound (I^2S™) external connectivity
  - One multichannel audio serial port (MCASP) supporting Sony/Philips digital interconnect format (S/PDIF) output, and four-channel I^2S in either direction
  - One digital microphone controller (DMIC) for three stereo digital microphones support
  - One multichannel pulse-density modulation (MCPDM) interface, which ensures communication with the TWL6041 audio companion chip
- Internal interfaces for connection with the DSP and MPU subsystems and other modules in the device

1.3.7 Imaging Subsystem (ISS)

The ISS processes data coming from the image sensor, memory, and IVA-HD subsystem. The ISS is responsible for multimedia applications such as: camera viewfinder; video record with up to 1080p at 60 fps or stereoscopic record up to 1080p at 30 fps with digital zoom, video stabilization, rotation and auto-convergence. The ISS supports a pixel throughput of up to 304 MP/s. It assures good performance with sensors up to 24 MP and more (higher resolution can be achieved using vertical frame division mode). ISS supports still image capture during video record. The ISS can implement third-party algorithms for further flexibility when working with image sensors.

The ISS consists of:

- The ISP, which deals with on-the-fly or memory-to-memory data processing. It allows data collection for autoexposure, autowhite balance, autofocus, resizing, and histogram generation. The ISP consists of:
  - Image pipe interface (IPIPEIF) for synchronization signals (HD, VD) for the ISIF, IPIPE, RSZ, and hardware 3A (H3A) modules, and data transfer from video port, SDRAM, ISIF. Various pixel data manipulation functions.
  - Image pipe (IPIPE) front-end and back-end modules for raw data processing and RGB and YUV data processing, respectively. They support:
    - Sensor data linearization for dynamic range extension
    - Programmable 2D lens shading compensation correction
    - Black-level compensation
    - Defect pixel correction (LUT_DPC) with look-up table
    - Defect pixel correction (OTF_DPC) with on-the-fly detection and correction
    - Green imbalance correction (GIC)
    - Gamma correction
    - RGB color correction
    - RGB to YUV4:2:2 color conversion

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- 3D look up table (LUT) for color correction
- 2D noise filtering
- 2D edge enhancement
- False chroma suppression

– H3A for autowhite balance, autoexposure, and autofocus

– Two independent resizers, which allow YUV4:2:2 to YUV4:2:0 planar chroma filtering and downsampling. The resizers support input and output flows with up to 304 MP/s, and memory-to-memory rescaling in the range ×1/4096 scale down, and ×20 scale up. RGB565, ARGB888, YUV422 co sited and YUV4:2:0 planar (NV12 or NV21) data output.

– Image sensor interface (ISIF) can process the incoming data and supports the following main functions:

- Sensor data linearization
- Supports VGA read out mode
- Color space conversion
- Digital clamp with horizontal/vertical offset drift compensation
- Vertical line defect correction
- Programmable 2D-matrix lens shading correction
- 10-to-8 bits A-Law compression table inside

– Buffer logic (BL), which processes and manages the requests to the module and memory subsystem

- Peripheral serial interfaces for connection with sensors and memories:
  – One MIPI CSI-2 compliant with four RX data lanes
  – One MIPI CSI-2 compliant with two RX data lanes
  – One MIPI CSI-2 compliant with one RX data lane / MIPI CSI-1 / CCP2
- Peripheral 16-bit parallel interface, BT656 and SYNC mode
- SIMCOP coprocessor for memory-to-memory operation; JPEG encode/decode hardware acceleration; high-ISO filtering; block-based rotation; warping and fusion; and general-purpose imaging acceleration. The SIMCOP includes the following main submodules:
  – Two imaging extension (iMX) modules – programmable image and video processing engines
  – Noise filter 2 (NSF2) – for advanced noise filtering and edge-enhancement
  – Noise filter 3 (NSF3) – next generation NSF for advanced noise filtering and edge-enhancement, supporting Bayer RGB format
  – Variable-length coder/decoder for JPEG (VLCDJ) module
  – Discrete cosine transform (DCT) module
  – Warping accelerator for lens distortion correction (LDC) and chromatic aberration correction
  – Rotation accelerator (ROT) engine
  – Hardware sequencer, which offloads sequencing tasks from the MPU
  – Shared buffers/memories
  – DMA controller
- Timing control module for CAM global reset control, CAM flash strobe, and CAM shutter
- Bayer scaler module allowing low latency still image capture and stabilization statistics collection.

1.3.8 3D Graphics Processing Unit (GPU)

The 3D graphics processing unit subsystem is based on POWERVR® SGX544 subsystem from Imagination Technologies. It supports phone/PDA and handheld gaming applications. The GPU can process different data types simultaneously, such as: pixel data, vertex data, video data, and general-purpose data processing.

The GPU subsystem has the following features:

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- Multicore GPU architecture: two SGX544 cores. Shared system level cache of 128 KiB
- Tile-based deferred rendering architecture
- Second-generation universal scalable shader engines (USSE2), multithreaded engines incorporating pixel and vertex shader functionality
- Present and texture load accelerators
  - Enables to move, rotate, twiddle and scale texture surfaces.
  - Supports RGB, ARGB, YUV422 and YUV420 surface formats
  - Supports bilinear upscale
  - Supports source colorkey
- Industry-standard API supports DirectX® 9, OpenGL®-ES 1.1 and 2.0, OpenVG™ 1.1, and OpenCL™1.1 Embedded Profile
- Fine-grained task switching, load balancing, and power management
- Programmable high-quality image antialiasing
- Bilinear, trilinear, anisotropic texture filtering
- Advanced geometry DMA driven operation for minimum CPU interaction
- Fully virtualized memory addressing for OS operation in a unified memory architecture (MMU)

1.3.9 2D Graphics Accelerator

The 2D graphics accelerator (BB2D) subsystem is based on the GC320 2D core from Vivante® Corporation and has the following features:

- API support:
  - OpenWF™, DirectFB
  - GDI/DirectDraw
  - Adobe® Flash®
- BB2D architecture:
  - BitBlt and StretchBlt
  - DirectFB hardware acceleration
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Clipping rectangle support
  - Alpha blending includes Java 2 Porter-Duff compositing rules
  - 90-, 180-, 270-degree rotation on every primitive
  - YUV-to-RGB color space conversion
  - Programmable display format conversion with 14 source and 7 destination formats
  - High-quality 9-tap, 32-phase filter for image and video scaling at 1080p
  - Monochrome expansion for text rendering
  - 32 K × 32 K coordinate system

1.3.10 Face Detect Module

The face detect module is a stand-alone module that performs face detection and tracking on a picture stored in the SDRAM memory. It communicates with the MPU, DSP, and IPU subsystems.

Face detect is typically assists:

- Video encoding
- Face-based priority auto-focusing
- Red-eye removal

The face detect module comprises:

- Face detection core with embedded DMA engine for data memory access

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- RAM and ROM memories
- L3 and L4 port interfaces

1.3.11 On-Chip Debug Support

The on-chip debug support has the following features:

- Multiprocessor debugging lets users control multiple CPU cores embedded in the device, such as:
  - Global starting and stopping of individual or multiple processors
  - Each processor can generate triggers that can be used to alter the execution flow of other processors
  - System clocking and power down
  - Interconnection of multiple devices
  - Channel triggering
- Target debugging, using IEEE1149.1 (JTAG®), or IEEE1149.7 (complementary superset of JTAG) port
- Reduction of power consumption in normal operating mode
- Real-time software trace allows the OMAP software masters to transmit trace data from OS processes or tasks on 256 different channels.

The debug subsystem includes:

- IEEE1149.7 adapter
- Generic TAP for emulation and test control (ICEPick-D™)
- Debug access port (DAP)
- Processor trace subsystem
- System trace subsystem
- EMU configuration interconnect
- Cross-triggering unit (XTRIGGER)
- Debug resource manager (DRM)

ICEMelter:

Controls the wake-up and power-down of the emulation power domain

CORE instrumentation (L3_INSTR) interconnect:

- Initiator ports:
  - L3 interconnect (for software instrumentation and performance probes)
  - OCP-WP
  - IVA-HD instrumentation (HWA profiling)
  - CM2 instrumentation
- Target port:
  - EMU instrumentation (L3_INSTR_EMU) interconnect

OCP watch-point (OCP-WP):

- Monitors L3 interconnect transaction when target transaction attributes match the user-defined attributes or trigger on external debug event
- Only one instance, shared among the following L3 targets:
  - GPMC
  - L4_PER
  - L4_CFG
  - DMM_P1 (DMM target port 1)
  - DMM_P2 (DMM target port 2)
  - OCMC_RAM

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Power management events profiler (PM instrumentation)

Clock management events profiler (CM instrumentation)

Statistics collector (performance probes)

1.3.12 Power, Reset, and Clock Management

The PRCM module allows efficient control of clocks and power according to the required performance, and reduction of power consumption.

The PRCM module is divided into:

- Power and reset management (PRM), based on the SmartReflex™ framework with the following features:
  - Dynamic clock gating
  - Dynamic voltage and frequency scaling (DVFS)
  - Dynamic power switching (DPS)
  - Static leakage management (SLM)
  - Adaptive body bias (ABB)
- Clock management part 1 (CM_CORE_AON) for clock generation, distribution, and management for the MPU, DSP, ABE, and CORE always-on power domains. The clock management allows reduction of dynamic consumption.
- Clock management part 2 (CM_CORE) for clock generation, distribution, and management for other modules.

1.3.13 On-Chip Memory

The on-chip memory is divided into L3 OCM RAM, SAR RAM, and memories in the subsystems (MPU, DSP, IPU, ABE, and IVA-HD).

- The L3 OCM RAM consists of 128 KiB of on-chip SRAM.
-
- The SAR RAM is used by device ROM code to store the software booting configuration: a logical structure that allows the redefinition of the ROM code default settings when booting after a warm reset.

1.3.14 Memory Management

The memory management is performed from:

- sDMA controller with up to 127 requests, 32 prioritizable logical channels, and 256 × 64-bit FIFO dynamically allocable between active channels
- Dynamic memory management (DMM) module, which performs global address translation, address rotation (tiling), and access interleaving between the two EMIF channels.

1.3.15 External Memory Interface Description

- The SDRAM memory controller (EMIF) allows:
  - Connection between the device and LPDDR2- or DDR3-type of memories. Supported memory depends on device and its package; see Section 1.5, *OMAP543x Family and Device Identification.*
  - Dual-port controller for efficient memory access
  - 32-bit data path, two chip-selects per memory port controller
  - Memory density up to 2 GiB supported per chip-select providing a total SDRAM space of 8 GiB addressable by the MPU extended address range.
- The general-purpose memory controller (GPMC) supports connection with:
  - Asynchronous SRAM memories
  - Asynchronous/synchronous NOR flash memories
  - NAND flash memories

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  - Pseudo-SRAM devices
- Two HS-MMC/SD initiator controllers:
  - Support JEDEC JESD64 v4.4.1 and SD3.0 physical layer with SDA3.00 standards
  - Each controller includes its DMA controller compliant to ADMA2 (SDA3.00 Part A2 DMA controller)
  - One controller with 8-bit interface for JC64 memories with dual voltage I/Os (1.2/1.8 V). One controller with a 4-bit interface for external card support with embedded dual voltage I/Os (1.8/3V)
- SATA interface for solid-state drive (SSD) or hard-disk drive (HDD) mass storage. Supports one HBA port with SATA-2 generation speed of 3 Gbps.

1.3.16 System and Connection Peripherals

The OMAP device supports a comprehensive set of peripherals to provide flexible and high-speed interfacing and on-chip programming resources.

1.3.16.1 System Peripherals

- Seven general-purpose timers (TIMER)
- One watchdog timer (WD_TIMER)
- One 32-kHz synchronization timer (COUNTER_32K)
- System control module, which contains registers for the following functions:
  - Static device configuration
  - Debug and observability
  - Status
  - Pad configuration
  - I/O configuration
  - eFuse logic
  - Analog function control
  - System boot decoding logic
- System mailbox with eight mailbox message queues
- One SPINLOCK module with 32 hardware semaphores, which can service tasks between the MPU, DSP, and IPU subsystems

1.3.16.2 Connectivity Peripherals

- Five universal asynchronous receiver/transmitter (UART) modules as serial-communication interfaces
- One UART + IrDA SIR up to FIR + TV remote control interface (CIR)
- Six HS I^2C controller modules; five of them are general-purpose modules with rates up to 3.4 Mbps, and the sixth one, in the PRCM module, performs dynamic voltage control and power sequencing with an external power IC.
- HDQ™/1-Wire® – Benchmarq HDQ and Dallas Semiconductor 1-Wire protocols interface
- Three HS MMC/SD/SDIO modules with 4-bit data bus interface
- Eight general-purpose input/output (GPIO) modules with 32 I/Os each
- One keyboard controller, which supports up to 9 × 9 matrix keypads
- Four multichannel serial peripheral interface (MCSPI) modules
- One single-port SuperSpeed universal serial bus (USB) Dual-Role-Device (DRD) module with embedded PHYs, compliant with the USB2.0 (up to 480 Mbps) and USB3.0 (5 Gbps) standard for HS and SS functions
- One high-speed (HS) multiport USB host module, which can be used for interchip connection or with an off-chip transceiver. It is compliant with the USB2.0 standard. The USB host module allows communication with USB peripherals with data rates up to 480 Mbps for high-speed, up to 12 Mbps for full-speed, and up to 1.5 Mbps for low-speed.
- One MIPI high-speed synchronous serial interface (HSI) module with two full-duplex serial

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communication interfaces. It is used for communication between the OMAP device and an external device, with data rates up to 192 Mbps for transmission, and up to 225 Mbps for reception. The MIPI HSI supports 32 logical channels on each destination (RX/TX).

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1.4 OMAP5430 Package-On-Package Concept

The OMAP5430 die uses flip-chip technology. The OMAP5430 package-on-page (POP) device supports memory stacking using a POP implementation.

The OMAP5430 die provides two LPDDR2 interfaces. Because each interface supports up to two chip-selects (CSs), up to four LPDDR2 memory dies are supported. Those interfaces are available only on device top ball out.

The two stacked memory packages are directly connected to the two LPDDR2 EMIF interfaces of the OMAP5430 die.

Figure 1-3 shows the concept of the POP solution.

Figure 1-3. POP Concept

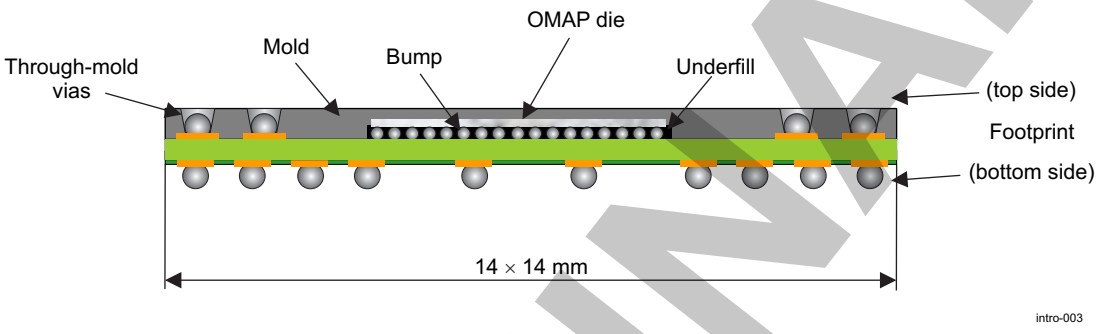
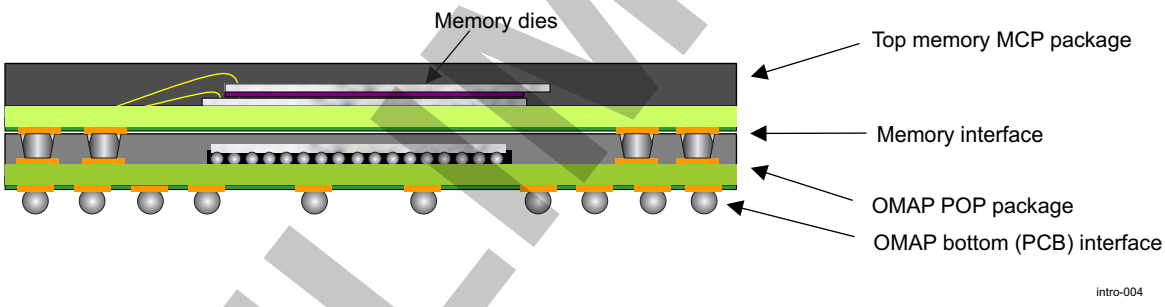


Figure 1-4 shows the stacked memory package on the POP device.

Figure 1-4. Stacked Memory Package on the POP Device



LPDDR2-SDRAM memory is supported in the POP package S4b, with a size of up to 8 GiB and 32-bit data width.

The POP device includes feedthroughs. The feedthroughs are defined from the bottom ball-grid array (BGA) to the stacked memory. The purpose of some of the feedthroughs is to provide power supply to the stacked memories.

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1.5 OMAP543x Family and Device Identification

The OMAP543x family is composed of the following devices:

- OMAP5430
- OMAP5432

The OMAP5430 device is offered in a 980-ball, 14 × 14 -mm POP package, which allows LPDDR2 memory stacking. It has all features and functions described in this TRM, except the EMIF DDR3 memory interface.

The OMAP5432 device is offered in a 754-ball, 17 × 17 -mm package, which does not support LPDDR2 memory stacking but instead can interface DDR3 on-board memories. Some of the features and functions described in this TRM are not supported by OMAP5432.

NOTE: See more information about OMAP5432 in Appendix A, OMAP5432 Multimedia Device and the OMAP5432 Data Manual.

Table 1-1 describes the identification registers.

The identification registers include the data registers listed in STD_FUSE_DIE_ID and ID_CODE. These registers are read-only accessed ports that are programmed into eFuses FARM FROM.

Table 1-1. Device Identification Register Fields

Register Field	Alias Name	Physical Address	Address Offset
CONTROL_STATUS[8:6] DEVICE_TYPE	DEVICE_TYPE	0x4A00 2134	0x134
CONTROL_STD_FUSE_DIE_ID_0[31:0] STD_FUSE_DIE_ID_0	DIE_ID[31:0]	0x4A00 2200	0x200
CONTROL_STD_FUSE_ID_CODE[31:0] STD_FUSE_IDCODE	ID_CODE	0x4A00 2204	0x204
CONTROL_STD_FUSE_DIE_ID_1[31:0] STD_FUSE_DIE_ID_1	DIE_ID[63:32]	0x4A00 2208	0x208
CONTROL_STD_FUSE_DIE_ID_2[31:0] STD_FUSE_DIE_ID_2	DIE_ID[95:64]	0x4A00 220C	0x20C
CONTROL_STD_FUSE_DIE_ID_3[31:0] STD_FUSE_DIE_ID_3	DIE_ID[127:96]	0x4A00 2210	0x210
CONTROL_STD_FUSE_PROD_ID[31:0] STD_FUSE_PROD_ID	PROD_ID	0x4A00 2214	0x214

Table 1-2. DIE_ID

Register Field	Alias Name	Value
CONTROL_STD_FUSE_DIE_ID_0[31:0] STD_FUSE_DIE_ID_0	DIE_ID[31:0]	Wafer and die unique identifier
CONTROL_STD_FUSE_DIE_ID_1[31:0] STD_FUSE_DIE_ID_1	DIE_ID[63:32]	Wafer fab and lot unique identifier
CONTROL_STD_FUSE_DIE_ID_2[31:0] STD_FUSE_DIE_ID_2	DIE_ID[95:64]	Other die data
CONTROL_STD_FUSE_DIE_ID_3[31:0] STD_FUSE_DIE_ID_3	DIE_ID[127:96]	Reserved

The product type can be read in the value of the RAMP_SYSTEM bit field of the ID_CODE register. The silicon revision can be read in the value of the VERSION bit field of the ID_CODE register.

Table 1-3. ID_CODE

Register Field	Value	Comment
CONTROL_STD_FUSE_ID_CODE[31:28] VERSION	See Table 1-4	Revision number

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Table 1-3. ID_CODE (continued)

Register Field	Value	Comment
CONTROL_STD_FUSE_ID_CODE[27:12] RAMP_SYSTEM	See Table 1-4	Ramp system number
CONTROL_STD_FUSE_ID_CODE[11:1] TI_IDM	0x17	Manufacturer identity (TI)
CONTROL_STD_FUSE_ID_CODE[0] ONE	0x1	Always set to 1

Table 1-4, *OMAP543x ID_CODE Values* lists the ramp system and revision number values.

Table 1-4. OMAP543x ID_CODE Values

Silicon Type	VERSION	RAMP_SYSTEM	ID_CODE
OMAP5430 ES1.0	0x0	0xB942	0x0B94202F
OMAP5432 ES1.0	0x0	0xB998	0x0B99802F
OMAP5430 ES2.0	0x1	0xB942	0x1B94202F
OMAP5432 ES2.0	0x1	0xB998	0x1B99802F

The device type can be read in the STD_FUSE_PROD_ID register.

Table 1-5. PROD_ID

Register Field	Value	Comment
CONTROL_STD_FUSE_PROD_ID[7:0] DEVICE_TYPE	0xF0	Reads 0xF0 when device is a general-purpose (GP) device
CONTROL_STD_FUSE_PROD_ID[31:30] SPEED_GRADE	0x00 or 0x01 0x10	Standard performance (1.5 GHz) High performance (1.7 GHz)

The device type can be read also in the CONTROL_STATUS register.

Table 1-6. DEVICE_TYPE

Register Field	Value	Comment
CONTROL_STATUS[8:6] DEVICE_TYPE	0x3	Reads 0x3 when device is a general-purpose (GP) device

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Memory Mapping

This chapter describes the memory mapping.

NOTE: This chapter gives information about all modules and features in the high-tier device. In unavailable modules and features, the memory area is reserved, read is undefined, and write can lead to unpredictable behavior.

For the availability of device modules, see , *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

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2.1 Introduction

The microprocessor unit (MPU) has a 32-bit address port, which allows it to handle a 4-GiB space divided into several regions, depending on the target type.

The memory map has the following features that are shared among the initiators, such as the MPU subsystem and the image and video accelerator (IVA) subsystem:

- Memory space: General-purpose memory controller (GPMC)
- Dynamic memory management (DMM) controller
- Register spaces: Level 3 (L3) and level 4 (L4) interconnects
- Dedicated spaces: IVA/IPU subsystem, etc.

The GPMC and DMM are dedicated to memory connection. The GPMC is used for NOR and NAND flash and static random access memories (SRAMs). The DMM is used for synchronous dynamic random access memories (SDRAMs), such as regular single-data rate (SDR)-SDRAM and mobile double-data rate (DDR)-SDRAM. For more information, see Section 15.2.1, *Dynamic Memory Manager*, and Section 15.3.1, *EMIF Controller*.

The L3 interconnect allows the sharing of resources, such as peripherals and external or on-chip memories, among all the initiators of the platform. The L4 interconnects control access to the peripherals.

Transfers across the platform between initiators and targets are physically conditioned by the chip interconnect and can be logically conditioned by firewalls. For more information about the intercommunication (L3 and L4 interconnects) and protection mechanisms implemented in the device, see Section 14.2.1, *L3 Interconnect*, and Section 14.3.1, *L4 Interconnect*.

Figure 2-1shows the interconnect of the device and the main modules and subsystems in the platform.

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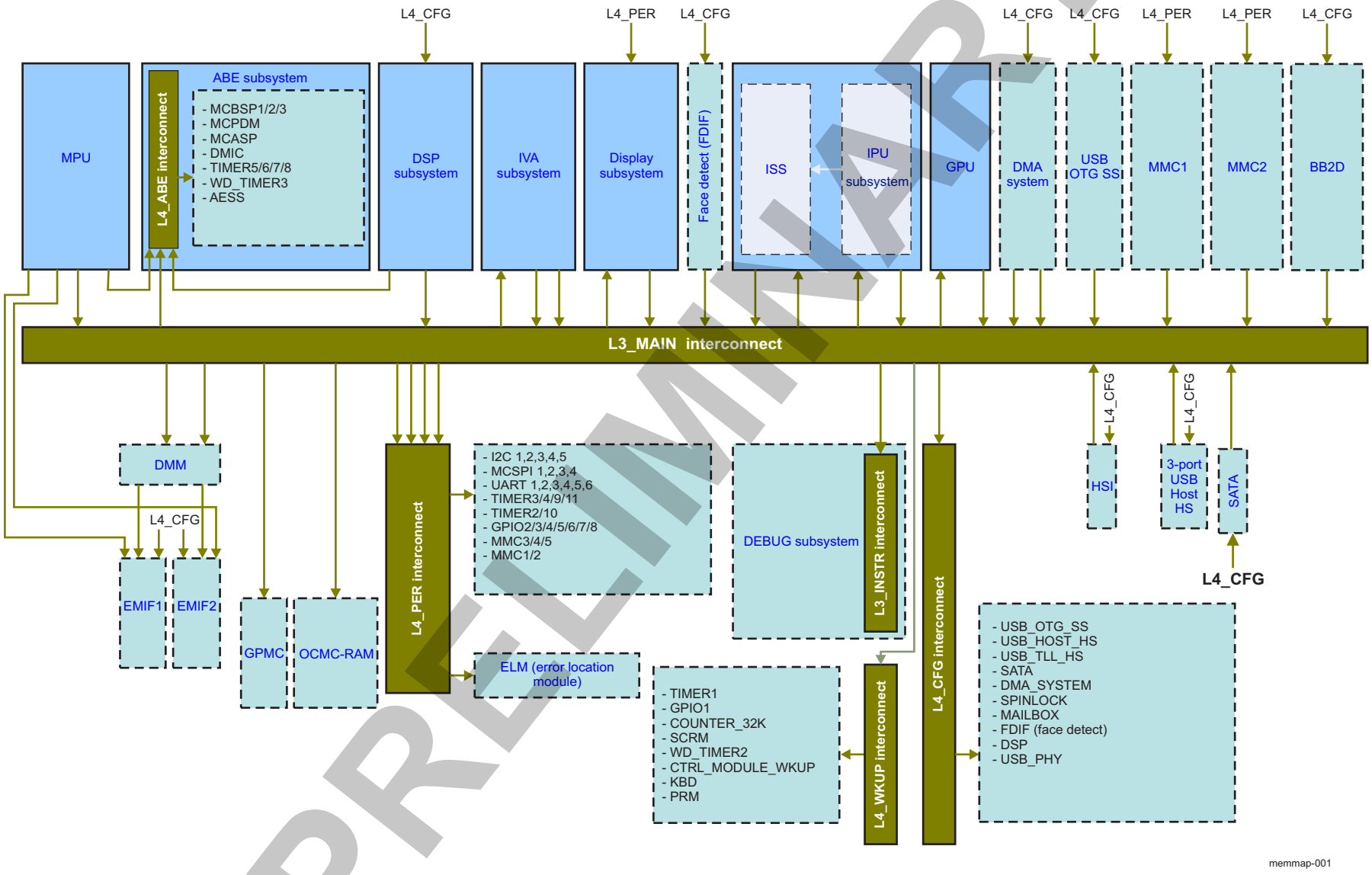
Figure 2-1. Interconnect Overview



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2.2 L3_MAIN Memory Space Mapping

The memory space system is hierarchical: level 1 (L1), level 2 (L2), L3_MAIN, and L4. L1 and L2 are memories in the MPU, IPU, and digital signal processor (DSP) subsystems. L3_MAIN handles many types of data transfers, including data exchange with system on-chip/external memories. The chip-level interconnect, which consists of one L3_MAIN and four L4s, enables communication among all modules and subsystems.

This section provides a global view of the memory mapping of the device at the L3_MAIN interconnect and describes the boot, GPMC, and SDRAM controller (SDRC) (EMIF/DMM) spaces.

The system memory mapping is flexible, with two levels of granularity for target address space allocation:

- L1: The four quarters are labeled Q0, Q1, Q2, and Q3. Each quarter corresponds to a 1-GiB address space (the total low-address space is 4 GiB, 32-bit). The CPU extended address range is labeled as high memory (Q8 – Q15) and provides a total of 8 GiB.
- L2: Each quarter is divided into eight blocks of 32 MiB, with target spaces mapped in the blocks.

This organization allows the decoding of all target spaces based on the 7 most-significant bits (MSBs) of the 32-bit address ([31:25]).

- Boot space:

  When booting from the on-chip ROM with the appropriate external sys_boot pin configuration, the lowest 1-MiB memory space [0x0000 0000–0x000F FFFF] is redirected to the on-chip boot ROM address space [0x4000 0000–0x400F FFFF].

  When booting from the GPMC, the memory space is part of the GPMC address space. At reset, the 0x0000 0000 address is available on chip-select 0 (CS0) for a memory size of 16 MiB.

  For more information about the sys_boot pins configuration, see Section 15.4.1, *General-Purpose Memory Controller*, and Section 28.1, *Initialization*.
- GPMC space:

  Eight independent GPMC chip-selects (CS0 to CS7) are available in the first quarter (Q0) of the addressing space to access NOR/NAND flash and SRAM. The chip-selects have a programmable start address and programmable size (up to 128 MiB) in a total memory space of (Q0) 1GiB, but limited now to 512 MiB.
- EMIF1/EMIF2 CS0 space:

  Q2 addressing space is interleaved on two LPDDR-memory controllers (EMIF1 and EMIF2), each activating its CS0 line. These chip-selects can be programmed to 64, 128, 256, 512, 1024, and 2048 MiB. Interleaving occurs at 128-byte granularity.

  The EMIF1-CS0 base address is always 0x8000 0000 at reset, and occupies a 1-GiB address space at reset (interleaving is disabled at reset).
- EMIF1 or EMIF2 CS1 space:

  Q3 addressing space is interleaved on two SDRAM controllers (EMIF1 and EMIF2), each activating its CS1 line. These chip-selects can be programmed to 64, 128, 256, 512, and 1024 MiB. Interleaving occurs at 128-byte granularity.

  EMIF1-CS1 and EMIF2-CS1 are disabled at reset. Their base address is programmable to achieve a continuous address space with the respective CS0, regardless of the address range programmed.

  EMIF1-CS1 is disabled if EMIF1-CS0 memory density is set to 2048 MiB (2 GiB) when interleaving is disabled, or if EMIF1-CS0 plus EMIF2-CS0 memory density is set to 1024 MiB (1 GiB) when interleaving is enabled.
- TILER space:

  Q3 addressing space is also used to access the TILER system. This space is visible only for the imaging subsystem (ISS) and the display subsystem.
- 8 GiB of SDRAM virtualization:

  This is a high address range (Q8 – Q15) that requires an address greater than 32 bits.

Table 2-1 describes the global memory space mapping.

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Table 2-1. Global Memory Space Mapping

Quarter	Module Name	Start Address (hex)	End Address (hex)	Size	Description
Q0 (1GiB)	GPMC [1]	0x0000 0000	0x2FFF FFFF	768MiB	8/16 Ex[2] /R/W
	Reserved	0x3000 0000	0x3FFF FFFF	256MiB	Reserved
Q1 (1GiB)	Reserved	0x4000 0000	0x4003 7FFF	224KiB	Reserved
	MPU	0x4003 8000	0x4004 3FFF	48KiB	MPU internal boot ROM: 32-bit Ex/R
	Reserved	0x4004 4000	0x400F FFFF	752KiB	Reserved
	ABE	0x4010 0000	0x401F FFFF	1MiB	ABE domain (direct MPU access). See Table 2-6.
	Reserved	0x4020 0000	0x402F FFFF	1MiB	Reserved
	OCMC_RAM	0x4030 0000	0x4031 FFFF	128 KiB	32-bit Ex/R/W
	Reserved	0x4032 0000	0x43FF FFFF	61MiB	Reserved
	L3_MAIN	0x4400 0000	0x457F FFFF	24MiB	L3 configuration registers (service network)
	Reserved	0x4580 0000	0x46FF FFFF	24MiB	Reserved
	MPU	0x4700 0000	0x47FF FFFF	16MiB	System trace macrocell
	L4_PER	0x4800 0000	0x481F FFFF	2MiB	Peripheral domain. See Section 2.3.3, *L4_PER Memory Space Mapping*.
	Reserved	0x4820 0000	0x4820 FFFF	64KiB	Reserved
	MPU	0x4821 0000	0x4821 7FFF	32KiB	MPU interrupt controller
	Reserved	0x4821 8000	0x4824 2FFF	172KiB	Reserved
	MPU	0x4824 3000	0x4824 3FFF	4KiB	PRM_MPU
	Reserved	0x4824 4000	0x4828 0FFF	244KiB	Reserved
	MPU	0x4828 1000	0x4828 1FFF	4 KiB	Wakeup Gen
	Reserved	0x4828 2000	0x4829 FFFF	120KiB	Reserved
	MPU	0x482A 0000	0x482A FFFF	60 KiB	AXI2OCP
	Reserved	0x482B 0000	0x483F FFFF	1344KiB	Reserved
	L4_PER	0x4840 0000	0x48FF FFFF	12MiB	Peripheral domain. See Section 2.3.3, *L4_PER Memory Space Mapping*.
	ABE	0x4900 0000	0x49FF FFFF	16MiB	L4_ABE domain (double mapped for MPU)
	L4_CFG	0x4A00 0000	0x4ADF FFFF	14MiB	Configuration Register domain. See Table 2-3.
	L4_WKUP	0x4AE0 0000	0x4AFF FFFF	2MiB	MPU configuration space
	Reserved	0x4B00 0000	0x4BFF FFFF	16MiB	Reserved
	EMIF1	0x4C00 0000	0x4CFF FFFF	16MiB	Configuration registers
	EMIF2	0x4D00 0000	0x4DFF FFFF	16MiB	Configuration registers
	DMM	0x4E00 0000	0x4FFF FFFF	32MiB	Configuration registers
	GPMC	0x5000 0000	0x51FF FFFF	32MiB	Configuration registers
	ISS	0x5200 0000	0x53FF FFFF	32MiB	ISP5 (128KiB) + SIMCOP (128KiB)
	L3_INSTR	0x5400 0000	0x547F FFFF	8MiB	Emulation domain
	DEBUGSS	0x5480 0000	0x54FF FFFF	8MiB	Emulation domain
	IPU	0x5500 0000	0x55FF FFFF	16MiB	IPU target
	GPU	0x5600 0000	0x57FF FFFF	32MiB	3D GFX (SGX 544) domain
	DSS	0x5800 0000	0x587F FFFF	8MiB	Display subsystem domain
	Reserved	0x5880 0000	0x58FF FFFF	8MiB	Reserved
	BB2D	0x5900 0000	0x59FF FFFF	16MiB	2D graphics accelerator
	IVA	0x5A00 0000	0x5AFF FFFF	16MiB	IVA CONFIG domain
	IVA	0x5B00 0000	0x5BFF FFFF	16MiB	IVA SL2IF domain

(1) Boot space location depends on the external sys_boot[5:0] pins.
(2) Ex = Executable

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Table 2-1. Global Memory Space Mapping (continued)

Quarter	Module Name	Start Address (hex)	End Address (hex)	Size	Description
	Reserved	0x5C00 0000	0x5FFF FFFF	64MiB	Reserved
	DMM	0x6000 0000	0x7FFF FFFF	512MiB	SRAM direct addressing through DMM with TILER off
Q2 (1GiB)	DRAM address space	0x8000 0000	0xBFFF FFFF	1GiB	DDR-SDRAM CS0 address space
	EMIF1	0x8000 0000	0xBFFF FFFF	1GiB	DDR Ctrl1 CS0
	EMIF2	0x8000 0000	0xBFFF FFFF	1GiB	DDR Ctrl2 CS0
Q3 (1GiB)	DRAM address space	0xC000 0000	0xFFFF FFFF	1GiB	DDR-SDRAM CS1 address space
	EMIF1	0xC000 0000	0xFFFF FFFF	1GiB	DDR Ctrl1 CS1
	EMIF2	0xC000 0000	0xFFFF FFFF	1GiB	DDR Ctrl2 CS1
	TILER view (visible only for ISS and display subsystem)				
TILER view	TILER view 0	0x1 0000 0000	0x1 1FFF FFFF	512MiB	Natural view
	TILER view 1	0x1 2000 0000	0x1 3FFF FFFF	512MiB	0-degree view with vertical mirror
	TILER view 2	0x1 4000 0000	0x1 5FFF FFFF	512MiB	0-degree view with horizontal mirror
	TILER view 3	0x1 6000 0000	0x1 7FFF FFFF	512MiB	180-degree view
	TILER view 4	0x1 8000 0000	0x1 9FFF FFFF	512MiB	90-degree view with vertical mirror
	TILER view 5	0x1 A000 0000	0x1 BFFF FFFF	512MiB	270-degree view
	TILER view 6	0x1 C000 0000	0x1 DFFF FFFF	512MiB	90-degree view
	TILER view 7	0x1 E000 0000	0x1 FFFF FFFF	512MiB	90-degree view with horizontal mirror
	8 GiB of SDRAM virtualization				
Q8	EMIF1	0x2 0000 0000	0x2 3FFF FFFF	1GiB	See[3]. EMIF1-CS0 SDRAM
Q9	EMIF1	0x2 4000 0000	0x2 7FFF FFFF	1GiB	See[3]. EMIF1-CS1 SDRAM
Q10	EMIF1	0x2 8000 0000	0x2 BFFF FFFF	1GiB	Alias of Q2. See[3]. EMIF1-CS0 SDRAM
Q11	EMIF2	0x2 C000 0000	0x2 FFFF FFFF	1GiB	Alias of Q3. See[3]. EMIF2-CS0 SDRAM
Q12	EMIF2	0x3 0000 0000	0x3 3FFF FFFF	1GiB	See[3]. EMIF2-CS1 SDRAM
Q13	EMIF2	0x3 4000 0000	0x3 7FFF FFFF	1GiB	See[3]. EMIF2-CS1 SDRAM
Q14	EMIF1	0x3 8000 0000	0x3 BFFF FFFF	1GiB	See[3]. EMIF1-CS1 SDRAM
Q15	EMIF2	0x3 C000 0000	0x3 FFFF FFFF	1GiB	See[3]. EMIF2-CS0 SDRAM
Q8	EMIF1	0x2 0000 0000	0x2 3FFF FFFF	1GiB	See[4]. EMIF1-CS0 SDRAM
Q8	EMIF2	0x2 0000 0000	0x2 3FFF FFFF	1GiB	See[4]. EMIF2-CS0 SDRAM
Q9	EMIF1	0x2 4000 0000	0x2 7FFF FFFF	1GiB	See[4]. EMIF1-CS0 SDRAM
Q9	EMIF2	0x2 4000 0000	0x2 7FFF FFFF	1GiB	See[4]. EMIF2-CS0 SDRAM
Q10	EMIF1	0x2 8000 0000	0x2 BFFF FFFF	1GiB	Alias of Q2. See[4]. EMIF1-CS0 SDRAM
Q11	EMIF2	0x2 C000 0000	0x2 FFFF FFFF	1GiB	Alias of Q3. See[4]. EMIF2-CS0 SDRAM
Q12	EMIF1	0x3 0000 0000	0x3 3FFF FFFF	1GiB	See[4]. EMIF1-CS1 SDRAM
Q12	EMIF2	0x3 0000 0000	0x3 3FFF FFFF	1GiB	See[4]. EMIF2-CS1 SDRAM
Q13	EMIF1	0x3 4000 0000	0x3 7FFF FFFF	1GiB	See[4]. EMIF1-CS1 SDRAM
Q13	EMIF2	0x3 4000 0000	0x3 7FFF FFFF	1GiB	See[4]. EMIF2-CS1 SDRAM
Q14	EMIF1	0x3 8000 0000	0x3 BFFF FFFF	1GiB	See[4]. EMIF1-CS1 SDRAM
Q14	EMIF2	0x3 8000 0000	0x3 BFFF FFFF	1GiB	See[4]. EMIF2-CS1 SDRAM
Q15	EMIF1	0x3 C000 0000	0x3 FFFF FFFF	1GiB	See[4]. EMIF1-CS1 SDRAM
Q15	EMIF2	0x3 C000 0000	0x3 FFFF FFFF	1GiB	See[4]. EMIF2-CS1 SDRAM

(3) Address range when interleaving is disabled

(4) Address range when interleaving is enabled. Interleaving is configurable with one setting in the MPU memory adapter (MA_MPU) for all 8 GiB of SDRAM high memory. For more information about interleaving, see Section 4.3.4.1, *MA_MPU Functional Description*.

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2.2.1 L3_INSTR Memory Space Mapping

The L3_INSTR interconnect is a 2-MiB space composed of the L3_INSTR interconnect configuration registers and module registers.

Table 2-2 describes the mapping of the registers for the L3_INSTR interconnect.

Table 2-2. L3_INSTR Memory Space Mapping

Region Name	Start Address (hex)	End Address (hex)	Size	Description
CT_STM_ADD_SP_0	0x5400 0000	0x540F FFFF	1MiB	MIPI_STM - System Trace Macrocell (address space 0)
CT_STM_ADD_SP_1 (address space 1)	0x5410 0000	0x5413 FFFF	256KiB	MIPI_STM - System Trace Macrocell (address space 1)
DBG_MPU_C0	0x5414 0000	0x5414 0FFF	4KiB	MPU C0 Debug Unit
PMU_MPU_C0	0x5414 1000	0x5414 1FFF	4KiB	MPU C0 Performance Monitoring Unit
DBG_MPU_C1	0x5414 2000	0x5414 2FFF	4KiB	MPU C1 Debug Unit
PMU_MPU_C1	0x5414 3000	0x5414 3FFF	4KiB	MPU C1 Performance Monitoring Unit
Reserved	0x5414 4000	0x5414 7FFF	16KiB	Reserved
CS_CTI_MPU_C0	0x5415 8000	0x5414 8FFF	4KiB	Cross-Triggering Interface (CTI0 component)
CS_CTI_MPU_C1 (CTI1 component)	0x5414 9000	0x5414 9FFF	4KiB	Cross-Triggering Interface (CTI1 component)
Reserved	0x5414 A000	0x5414 BFFF	8KiB	Reserved
CS_PTM_MPU_C0	0x5414 C000	0x5414 CFFF	4KiB	Processor Trace Macrocell Component 0
CS_PTM_MPU_C1	0x5414 D000	0x5414 DFFF	4KiB	Processor Trace Macrocell Component 1
Reserved	0x5414 E000	0x5415 7FFF	40KiB	Reserved
CS_TF_MPU (trace funnel)	0x5415 8000	0x5415 8FFF	4KiB	Trace Funnel for MPU
DAP_PC	0x5415 9000	0x5415 9FFF	4KiB	DAP_PC
CS_STM_MPU	0x5415 A000	0x5415 AFFF	4KiB	CoreSight™ System Trace Module (equivalent to MIPI_STM)
ATB_FIFO_SGU	0x5415 B000	0X5415 BFFF	4KiB	AMBA® Trace Buffer Static Gathering Unit
CS_CTI_MPU	0x5415 C000	0x5415 CFFF	4KiB	MPU Ctross Triggering Interface
Reserved	0x5415 D000	0x5415 EFFF	8KiB	Reserved
T2ASYNC_APB_MPU_DEBUG_MPU_MPU	0x5415 F000	0x5415 FFFF	4KiB	APB bridge control and time-out register
DRM	0x5416 0000	0x5416 0FFF	4KiB	Debug Register Mapping
CT_STM_CONF_PORT	0x5416 1000	0x5416 1FFF	4KiB	MIPI_STM configuration port - System Trace
Reserved	0x5416 2000	0x5416 2FFF	4KiB	Reserved
CS_TPIU	0x5416 3000	0x5416 3FFF	4KiB	Trace Port Interface UNIT
CS_TF_DEBUGSS_1	0x5416 4000	0x5416 4FFF	4KiB	Trace Funnel for DEBUGSS
Reserved	0x5416 5000	0x5416 6FFF	8KiB	Reserved
CT_TBR	0x5416 7000	0x5416 7FFF	4KiB	C-Tools Trace Buffer
CT_UART	0x5416 8000	0x5416 8FFF	4KiB	C-Tools UART
CS_CTI_DEBUGSS	0x5416 9000	0x5416 9FFF	4KiB	Cross-Triggering Interface
CS_CTM_DEBUGSS	0x5416 A000	0x5416 AFFF	4KiB	CoreSight System Trace Module (equivalent to MIPI_STM)
MASTER_TIMESTAMP	0x5416 B000	0x5416 BFFF	4KiB	Master Timestamp
Reserved	0x5416 C000	0x5417 0FFF	18KiB	Reserved

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Table 2-2. L3_INSTR Memory Space Mapping (continued)

Region Name	Start Address (hex)	End Address (hex)	Size	Description
OCP2SCP_DEBUGSS	0x5417 1000	0x5417 1FFF	4KiB	Interconnect registers
L4_CFG_EMU_CONF_REGS	0x5417 2000	0x5417 2FFF	4KiB	Interconnect registers
Reserved	0x5417 3000	0x5417 FFFF	52KiB	Reserved
L3_INSTR_EMU_CONF_REGS	0x5418 0000	0x5418 0FFF	4KiB	Interconnect registers
Reserved	0x5418 1000	0x541F FFFF	508KiB	Reserved

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2.3 L4 Memory Space Mapping

Four L4 interconnects handle transfers with peripherals. Each interconnect is in a distinct power domain:

- L4_CFG: CORE power domain
- L4_WKUP: WKUP power domain
- L4_PER: PER power domain
- L4_ABE: ABE power domain

As with the L3_MAIN interconnect, the L4 interconnect can be configured to tune the access according to the characteristics of each module.

The following sections describe the register mapping of the L4 interconnect. Software configures these registers.

2.3.1 L4_CFG Memory Space Mapping

The L4_CFG interconnect is a 16-MiB space composed of the L4_CFG interconnect configuration registers and the module registers.

Table 2-3 describes the mapping of the registers for the L4_CFG interconnect.

NOTE: All memory spaces described as modules provide direct access to module registers outside the L4_CFG interconnect. All other accesses are internal to the L4_CFG interconnect.

Table 2-3. L4_CFG Memory Space Mapping

Region Name	Related IP Name	Start Address (hex)	End Address (hex)	Size	Description
L4_CFG_AP	L4_CFG	0x4A00 0000	0x4A00 07FF	2KiB	Address protection
L4_CFG_AL	L4_CFG	0x4A00 0800	0x4A00 0FFF	2KiB	Link agent
IA_IP0	L4_CFG	0x4A00 1000	0x4A00 1FFF	4KiB	Initiator port
TP_CTRL_MODULE_CORE_TARG	CTRL_MODULE_CORE	0x4A00 2000	0x4A00 2FFF	4KiB	Module target port
TA_CTRL_MODULE_CORE_TARG	L4_CFG	0x4A00 3000	0x4A00 3FFF	4KiB	L4 target agent
TP_CM_CORE_AON_TARG	CM_CORE_AON	0x4A00 4000	0x4A00 4FFF	4 KiB	Module target port
TA_CM_CORE_TARG	L4_CFG	0x4A00 5000	0x4A00 5FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A00 6000	0x4A06 7FFF	Reserved	Reserved
TP_CM_CORE_TARG	CM_CORE	0x4A00 8000	0x4A08 9FFF	8KiB	Target port
TA_CM_CORE_TARG	L4_CFG	0x4A00 A000	0x4A00 AFFF	4KiB	L4 target agent
Reserved	Reserved	0x4A00 B000	0x4A01 FFFF	Reserved	Reserved
TP_USB_OTG_SS_TARG	USB_OTG_SS	0x4A02 0000	0x4A03 FFFF	128KiB	Module target port
TA_USB_OTG_SS_TARG	L4_CFG	0x4A04 0000	0x4A04 0FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A04 1000	0x4A05 5FFF	84KiB	Reserved
TP_DMA_SYSTEM_TARG	DMA_SYSTEM	0x4A05 6000	0x4A05 6FFF	4KiB	Module target port
TA_DMA_SYSTEM_TARG	L4_CFG	0x4A05 7000	0x4A05 7FFF	4KiB	L4 target agent
TP_HSI_TOP_ADDRSP0_TARG	HSI address space 0	0x4A05 8000	0x4A05 8FFF	4KiB	Module target port - HSI Top (Maddrspace 0)
TP_HSI_DMA_ADDRSP1_TARG	HSI address space 1	0x4A05 9000	0x4A05 9FFF	4KiB	Module target port - HSI DMA (Maddrspace 1)
TP_HSI_PORT1_ADDRSP2_TARG	HSI address space 2	0x4A05 A000	0x4A05 AFFF	4 KiB	Module target port - HSI port 1 (Maddrspace 2)

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Table 2-3. L4_CFG Memory Space Mapping (continued)

Region Name	Related IP Name	Start Address (hex)	End Address (hex)	Size	Description
TP_HSI_PORT2_ ADDRSP3_TARG	HSI addres space 3	0x4A05 B000	0x4A05 BFFF	4 KiB	Module target port - HSI port 2 (Maddrspace 3)
TA_HSI_TARG	L4_CFG	0x4A05 C000	0x4A05 CFFF	4KiB	L4 target agent
Reserved	Reserved	0x4A05 D000	0x4A06 1FFF	20KiB	Reserved
TP_USB_TLL_ HS_TARG	USB_TLL_HS	0x4A06 2000	0x4A06 2FFF	4KiB	Module target port
TA_USB_TLL_ HS_TARG	L4_CFG	0x4A06 3000	0x4A06 3FFF	4KiB	L4 target agent
TP_USB_HOST_ HS_TARG	USB_HOST_HS	0x4A06 4000	0x4A06 4FFF	4KiB	Module target port
TA_USB_HOST_ HS_TARG	L4_CFG	0x4A06 5000	0x4A06 5FFF	4KiB	L4 target agent
TP_DSP_TARG	DSP	0x4A06 6000	0x4A06 6FFF	4KiB	Target port
TA_DSP_TARG	L4_CFG	0x4A06 7000	0x4A06 7FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A06 8000	0x4A07 6FFF	96KiB	Reserved
TP_OCP2SCP1_TARG	OCP2SCP1	0x4A08 0000	0x4A08 3FFF	16KiB	Module target port
TP_OCP2SCP1_USB_ PHY_CORE_TARG	OCP2SCP1 (USB_PHY)	0x4A08 4000	0x4A08 43FF	1KiB	Module target port
TP_OCP2SCP1_USB3_ PHY_RX_TARG	OCP2SCP1 (USB3_PHY_RX)	0x4A08 4400	0x4A08 47FF	1KiB	Target port
TP_OCP2SCP1_USB3_ PHY_TX_TARG	OCP2SCP1 (USB3_PHY_TX)	0x4A08 4800	0x4A08 4BFF	1KiB	Target port
TP_OCP2SCP1_DPLLCTRL_ USB_OTG_SS_TARG	OCP2SCP1 (USB_OTG_SS)	0x4A08 4C00	0x4A0D CFFF	1KiB	Tarteg port
Reserved	Reserved	0x4A08 5000	0x4A08 7FFF	12KiB	Reserved
TA_OCP2SCP1_TARG	L4_CFG	0x4A08 8000	0x4A08 8FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A08 9000	0x4A08 FFFF	28KiB	Reserved
TP_OCP2SCP3_TARG	OCP2SCP3	0x4A09 0000	0x4A09 3FFF	16KiB	Target port
Reserved	Reserved	0x4A09 4000	0x4A09 5FFF	8KiB	Reserved
TP_OCP2SCP3_SATA_ PHY_RX_TARG	OCP2SCP3 (SATA_PHY_RX)	0x4A09 6000	0x4A09 63FF	1KiB	Target port
TP_OCP2SCP3_SATA_ PHY_TX_TARG	OCP2SCP3 (SATA_PHY_TX)	0x4A09 6400	0x4A09 67FF	1KiB	Target port
TP_OCP2SCP3_DPLLCTRL_ SATA_TARG	OCP2SCP3 (DPLLCTRL_SATA)	0x4A09 6800	0x4A09 6BFF	1KiB	Target port
Reserved	Reserved	0x4A09 6C00	0x4A09 7FFF	5KiB	Reserved
TA_OCP2SCP3_TARG	L4_CFG	0x4A09 8000	0x4A09 8FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A09 9000	0x4A0D 8FFF	200KiB	Reserved
TP_SMARTREFLEX_ MPU_TARG	SMARTREFLEX_MPU	0x4A0D 9000	0x4A0D 9FFF	4KiB	Module target port
TA_SMARTREFLEX_ MPU_TARG	L4_CFG	0x4A0D A000	0x4A0D AFFF	4KiB	L4 target agent
TP_SMARTREFLEX_ MM_TARG	SMARTREFLEX_MM	0x4A0D B000	0x4A0D BFFF	4KiB	Module target port
TA_SMARTREFLEX_ MM_TARG	L4_CFG	0x4A0D C000	0x4A0D CFFF	4KiB	L4 target agent
TP_SMARTREFLEX_ CORE_TARG	SMARTREFLEX_CORE	0x4A0D 0000	0x4A0D DFFF	4KiB	Module targe port
TA_SMARTREFLEX_ CORE_TARG	L4_CFG	0x4A0D E000	0x4A0D EFFF	4KiB	L4 target agent
Reserved	Reserved	0x4A0D F000	0x4A0F 3FFF	96KiB	Reserved
TP_MAILBOX_TARG	MAILBOX	0x4A0F 4000	0x4A0F 4FFF	4KiB	Target port

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Table 2-3. L4_CFG Memory Space Mapping (continued)

Region Name	Related IP Name	Start Address (hex)	End Address (hex)	Size	Description
TA_MAILBOX_TARG	L4_CFG	0x4A0F 5000	0x4A0F 5FFF	4KiB	L4 target agent
TP_SPINLOCK_TARG	SPINLOCK	0x4A0F 6000	0x4A0F 6FFF	4KiB	Module target port
TA_SPINLOCK_TARG	L4_CFG	0x4A0F 7000	0x4A0F 7FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A0F 8000	0x4A10 1FFF	40KiB	Reserved
TP_OCP_WP_ NOC_TARG	OCP_WP_NOC	0x4A10 2000	0x4A10 2FFF	4KiB	Module target port
TA_OCP_WP_ NOC_TARG	L4_CFG	0x4A10 3000	0x4A10 3FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A10 4000	0x4A10 9FFF	24KiB	Reserved
TP_FDIF_TARG	FDIF	0x4A10 A000	0x4A10 AFFF	4KiB	Module target port
TA_FDIF_TARG	L4_CFG	0x4A10 B000	0x4A10 BFFF	4KiB	L4 target agent
Reserved	Reserved	0x4A10 C000	0x4A13 FFFF	208KiB	Reserved
TP_SATA_TARG	SATA	0x4A14 0000	0x4A14 FFFF	64KiB	Module target port
TA_SATA_TARG	L4_CFG	0x4A15 0000	0x4A15 0FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A15 1000	0x4A20 9FFF	764KiB	Reserved
TP_MA_MPU_NTTP_ FW_CFG_TARG	GPMC	0x4A20 A000	0x4A20 AFFF	4KiB	Module target port
TA_MA_MPU_NTTP_ FW_CFG_TARG	L4_CFG	0x4A20 B000	0x4A20 BFFF	4KiB	L4 target agent
TP_EMIF_OCP_ FW_CFG_TARG	EMIF_OCP_FW	0x4A20 C000	0x4A20 CFFF	4 KiB	Module target port
TA_EMIF_OCP_ FW_CFG_TARG	L4_CFG	0x4A20 D000	0x4A20 DFFF	4KiB	L4 target agent
Reserved	Reserved	0x4A20 E000	0x4A20 FFFF	8KiB	Reserved
TP_GPMC_FW_ CFG_TARG	GPMC	0x4A21 0000	0x4A21 0FFF	4KiB	Module target port
TA_GPMC_FW_ CFG_TARG	L4_CFG	0x4A21 1000	0x4A21 1FFF	4KiB	L4 target agent
TP_OCMC_RAM_ FW_CFG_TARG	OCMC_RAM	0x4A21 2000	0x4A21 2FFF	4 KiB	Module target port
TA_OCMC_RAM_ FW_CFG_TARG	L4_CFG	0x4A21 3000	0x4A21 3FFF	4KiB	L4 target agent
TP_GPU_FW_CFG_TARG	GPU	0x4A21 4000	0x4A21 4FFF	4KiB	Module target port
TA_GPU_FW_CFG_TARG	L4_CFG	0x4A21 5000	0x4A21 5FFF	4KiB	L4 target agent
TP_ISS_FW_CFG_TARG	ISS	0x4A21 6000	0x4A21 6FFF	4KiB	Module target port
TA_ISS_FW_CFG_TARG	L4_CFG	0x4A21 7000	0x4A21 7FFF	4KiB	L4 target agent
TP_IPU_FW_CFG_TARG	IPU	0x4A21 8000	0x4A21 8FFF	4KiB	Module target port
TA_IPU_FW_CFG_TARG	L4_CFG	0x4A21 9000	0x4A21 9FFF	4KiB	L4 target agent
TP_BB2D_FW_CFG_TARG	BB2D	0x4A21 A000	0x4A21 AFFF	4KiB	Module target port
TA_BB2D_FW_CFG_TARG	L4_CFG	0x4A21 B000	0x4A21 BFFF	4KiB	L4 target agent
TP_DSS_FW_CFG_TARG	DSS	0x4A21 C000	0x4A21 CFFF	4KiB	Module target port
TP_DSS_FW_CFG_TARG	L4_CFG	0x4A21 D000	0x4A21 DFFF	4KiB	L4 target agent
TP_IVA_SL2IF_ FW_CFG_TARG	IVA_SL2IF	0x4A21 E000	0x4A21 EFFF	4 KiB	Module target port
TA_IVA_SL2IF_ FW_CFG_TARG	L4_CFG	0x4A21 F000	0x4A21 FFFF	4KiB	L4 target agent
TP_IVA_CONFIG_ FW_CFG_TARG	IVA	0x4A22 0000	0x4A22 0FFF	4KiB	Module target port
TA_IVA_CONFIG_ FW_CFG_TARG	L4_CFG	0x4A22 1000	0x4A22 1FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A22 2000	0x4A22 3FFF	8KiB	Reserved

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Table 2-3. L4_CFG Memory Space Mapping (continued)

Region Name	Related IP Name	Start Address (hex)	End Address (hex)	Size	Description
TP_DEBUGSS_CT_TBR_ FW_CFG_TARG	DEBUGSS	0x4A22 4000	0x4A22 4FFF	4KiB	Module targe prot
TA_DEBUGSS_CT_TBR_ FW_CFG_TARG	L4_CFG	0x4A22 5000	0x4A22 5FFF	4KiB	L4 target agent
TP_L3_INSTR_FW_ CFG_TARG	L3_INSTR	0x4A22 6000	0x4A22 6FFF	4KiB	Module target port
TA_L3_INSTR_FW_ CFG_TARG	L4_CFG	0x4A22 7000	0x4A22 7FFF	4KiB	L4 target agent
TP_ABE_FW_ CFG_TARG	ABE	0x4A22 8000	0x4A22 8FFF	4KiB	Module target port
TA_ABE_FW_ CFG_TARG	L4_CFG	0x4A22 9000	0x4A22 9FFF	4KiB	L4 target agent
Reserved	Reserved	0x4A22 A000	0x4ADF FFFF	12MiB	Reserved

2.3.2 L4_WKUP Memory Space Mapping

The L4_WKUP interconnect is a 256-KiB space composed of the L4_WKUP interconnect configuration registers and the module registers.

Table 2-4 describes the mapping of the registers for the L4_WKUP interconnect.

NOTE: All memory spaces described as modules provide direct access to module registers outside the L4_WKUP interconnect. All other accesses are internal to the L4_WKUP interconnect.

Table 2-4. L4_WKUP Peripheral Space Mapping

Module Name	Region name	Start Address (hex)	End Address (hex)	Size	Description
L4_WKUP configuration	L4_WKUP_AP	0x4AE0 0000	0x4AE0 07FF	2KiB	Address protection (AP)
	L4_WKUP_LA	0x4AE0 0800	0x4AE0 0FFF	2KiB	Link agent (LA)
	IA_IP0	0x4AE0 1000	0x4AE0 1FFF	4KiB	Initiator port (IP0)
Reserved	Reserved	0x4AE0 2000	0x4AE0 3FFF	8KiB	Reserved
COUNTER_32K	TP_COUNTER_32K_TARG	0x4AE0 4000	0x4AE0 4FFF	4KiB	Module
	TA_COUNTER_32K_TARG	0x4AE0 5000	0x4AE0 5FFF	4KiB	L4 interconnect
PRM (power and reset manager)	TP_PRM_TARG	0x4AE0 6000	0x4AE0 7FFF	8KiB	Module
	TA_PRM_TARG	0x4AE0 8000	0x4AE0 8FFF	4KiB	L4 interconnect
Reserved	Reserved	0x4AE0 9000	0x4AE0 9FFF	4KiB	Reserved
SCRM	TP_SCRM_TARG	0x4AE0 A000	0x4AE0 AFFF	4KiB	Module
	TA_SCRM_TARG	0x4AE0 B000	0x4AE0 BFFF	4KiB	L4 interconnect
CTRL_MODULE_WKUP	TP_CTRL_MODULE_TARG	0x4AE0 C000	0x4AE0 CFFF	4KiB	Module
	TA_CTRL_MODULE_TARG	0x4AE0 D000	0x4AE0 DFFF	4KiB	L4 interconnect
Reserved	Reserved	0x4AE0 E000	0x4AE0 FFFF	8KiB	Reserved
GPIO1	TP_GPIO1_TART	0x4AE1 0000	0x4AE1 0FFF	4KiB	Module
	TA_GPIO1_TARG	0x4AE1 1000	0x4AE1 1FFF	4KiB	L4 interconnect
Reserved	Reserved	0x4AE1 2000	0x4AE1 3FFF	8KiB	Reserved
WD_TIMER2	TP_WD_TIMER2_TARG	0x4AE1 4000	0x4AE1 4FFF	4KiB	Module
	TA_WD_TIMER_TARG	0x4AE1 5000	0x4AE1 5FFF	4KiB	L4 interconnect
Reserved	Reserved	0x4AE1 6000	0x4AE1 7FFF	8KiB	Reserved
TIMER1	TP_TIMER1_TARG	0x4AE1 8000	0x4AE1 8FFF	4KiB	Module
	TA_TIMER1_TARG	0x4AE1 9000	0x4AE1 9FFF	4KiB	L4 interconnect

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Table 2-4. L4_WKUP Peripheral Space Mapping (continued)

Module Name	Region name	Start Address (hex)	End Address (hex)	Size	Description
Reserved	Reserved	0x4AE1 A000	0x4AE1 BFFF	8KiB	Module – Address space 0
KBD	TP_KBD_TARG	0x4AE1 C000	0x4AE1 CFFF	4KiB	Module
	TA_KBD_TARG	0x4AE1 D000	0x4AE1 DFFF	4KiB	L4 interconnect
Reserved	Reserved	0x4AE1 E000	0x4AE2 5FFF	32KiB	Reserved
SAR_RAM	TP_SAR_RAM_SPACE1_TARG	0x4AE2 6000	0x4AE2 6FFF	4KiB	Module – SAR space 1
	TP_SAR_RAM_SPACE2_TARG	0x4AE2 7000	0x4AE2 73FF	1KiB	Module – SAR space 2
Reserved	Reserved	0x4AE2 7400	0x4AFF FFFF	1891KiB	Reserved

NOTE: 8- and 16-bit peripherals are aligned on 32-bit address boundaries.

2.3.3 L4_PER Memory Space Mapping

The L4_PER interconnect is a 16-MiB memory space composed of the L4_PER interconnect configuration registers and the module registers.

Table 2-5 describes the mapping of the registers for the L4_PER interconnect.

NOTE: All memory spaces described as modules provide direct access to the module registers outside the L4_PER interconnect. All other accesses are internal to the L4_PER interconnect.

Table 2-5. L4_PER Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4_PER	0x4800 0000	0x4800 07FF	2KiB	Address protection (AP)
	0x4800 0800	0x4800 0FFF	2KiB	Link agent (LA)
	0x4800 1000	0x4800 13FF	1KiB	Initiator port 0 (IP0)
	0x4800 1400	0x4800 17FF	1KiB	Initiator port 1 (IP1)
	0x4800 1800	0x4800 1BFF	1KiB	Initiator port 2 (IP2)
	0x4800 1C00	0x4800 1FFF	1KiB	Initiator port 3 (IP3)
Reserved	0x4800 2000	0x4801 FFFF	120KiB	Reserved
UART3	0x4802 0000	0x4802 0FFF	4KiB	Module
	0x4802 1000	0x4802 1FFF	4KiB	L4 interconnect
Reserved	0x4802 2000	0x4803 1FFF	64KiB	Reserved
TIMER2	0x4803 2000	0x4803 2FFF	4KiB	Module
	0x4803 3000	0x4803 3FFF	4KiB	L4 interconnect
TIMER3	0x4803 4000	0x4803 4FFF	4KiB	Module
	0x4803 5000	0x4803 5FFF	4KiB	L4 interconnect
TIMER4	0x4803 6000	0x4803 6FFF	4KiB	Module
	0x4803 7000	0x4803 7FFF	4KiB	L4 interconnect
Reserved	0x4803 8000	0x4803 DFFF	24KiB	Reserved
TIMER9	0x4803 E000	0x4803 EFFF	4KiB	Module
	0x4803 F000	0x4803 FFFF	4KiB	L4 interconnect
Reserved	0x4804 0000	0x4805 0FFF	68KiB	Reserved

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Table 2-5. L4_PER Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
GPIO7	0x4805 1000	0x4805 1FFF	4KiB	Module
	0x4805 2000	0x4805 2FFF	4KiB	L4 interconnect
GPIO8	0x4805 3000	0x4805 3FFF	4KiB	Module
	0x4805 4000	0x4805 4FFF	4KiB	L4 interconnect
GPIO2	0x4805 5000	0x4805 5FFF	4KiB	Module
	0x4805 6000	0x4805 6FFF	4KiB	L4 interconnect
GPIO3	0x4805 7000	0x4805 7FFF	4KiB	Module
	0x4805 8000	0x4805 8FFF	4KiB	L4 interconnect
GPIO4	0x4805 9000	0x4805 9FFF	4KiB	Module
	0x4805 A000	0x4805 AFFF	4KiB	L4 interconnect
GPIO5	0x4805 B000	0x4805 BFFF	4KiB	Module
	0x4805 C000	0x4805 CFFF	4KiB	L4 interconnect
GPIO6	0x4805 D000	0x4805 DFFF	4KiB	Module
	0x4805 E000	0x4805 EFFF	4KiB	L4 interconnect
Reserved	0x4805 F000	0x4805 FFFF	4KiB	Reserved
I2C3	0x4806 0000	0x4806 0FFF	4KiB	Module
	0x4806 1000	0x4806 1FFF	4KiB	L4 interconnect
Reserved	0x4806 2000	0x4806 5FFF	16KiB	Reserved
UART5	0x4806 6000	0x4806 6FFF	4 KiB	Module
	0x4806 7000	0x4806 7FFF	4KiB	L4 interconnect
UART6	0x4806 8000	0x4806 8FFF	4 KiB	Module
	0x4806 9000	0x4806 9FFF	4KiB	L4 interconnect
UART1	0x4806 A000	0x4806 AFFF	4KiB	Module
	0x4806 B000	0x4806 BFFF	4KiB	L4 interconnect
UART2	0x4806 C000	0x4806 CFFF	4KiB	Module
	0x4806 D000	0x4806 DFFF	4KiB	L4 interconnect
UART4	0x4806 E000	0x4806 EFFF	4KiB	Module
	0x4806 F000	0x4806 FFFF	4KiB	L4 interconnect
I2C1	0x4807 0000	0x4807 0FFF	4KiB	Module
	0x4807 1000	0x4807 1FFF	4KiB	L4 interconnect
I2C2	0x4807 2000	0x4807 2FFF	4KiB	Module
	0x4807 3000	0x4807 3FFF	4KiB	L4 interconnect
Reserved	0x4807 4000	0x4807 7FFF	16KiB	Reserved
ELM (error locator module)	0x4807 8000	0x4807 8FFF	4KiB	Module
	0x4807 9000	0x4807 9FFF	4KiB	L4 interconnect
I2C4	0x4807 A000	0x4807 AFFF	4KiB	Module
	0x4807 B000	0x4807 BFFF	4KiB	L4 interconnect
I2C5	0x4807 C000	0x4807 CFFF	4KiB	Module
	0x4807 D000	0x4807 DFFF	4KiB	L4 interconnect
Reserved	0x4807 E000	0x4808 5FFF	32KiB	Reserved
TIMER10	0x4808 6000	0x4808 6FFF	4KiB	Module
	0x4808 7000	0x4808 7FFF	4KiB	L4 interconnect
TIMER11	0x4808 8000	0x4808 8FFF	4KiB	Module
	0x4808 9000	0x4808 9FFF	4KiB	L4 interconnect
Reserved	0x4808 A000	0x4809 7FFF	56KiB	Reserved
McSPI1	0x4809 8000	0x4809 8FFF	4KiB	Module
	0x4809 9000	0x4809 9FFF	4KiB	L4 interconnect

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Table 2-5. L4_PER Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
McSPI2	0x4809 A000	0x4809 AFFF	4KiB	Module
	0x4809 B000	0x4809 BFFF	4KiB	L4 interconnect
MMC1	0x4809 C000	0x4809 CFFF	4KiB	Module
	0x4809 D000	0x4809 DFFF	4KiB	L4 interconnect
Reserved	0x4809 E000	0x480A CFFF	60KiB	Reserved
MMC3	0x480A D000	0x480A DFFF	4KiB	Module
	0x480A E000	0x480A EFFF	4KiB	L4 interconnect
Reserved	0x480A F000	0x480B 1FFF	12KiB	Reserved
HDQ1W	0x480B 2000	0x480B 2FFF	4KiB	Module
	0x480B 3000	0x480B 3FFF	4KiB	L4 interconnect
MMC2	0x480B 4000	0x480B 4FFF	4KiB	Module
	0x480B 5000	0x480B 5FFF	4KiB	L4 interconnect
Reserved	0x480B 6000	0x480B 7FFF	8KiB	Reserved
MCSPI3	0x480B 8000	0x480B 8FFF	4KiB	Module
	0x480B 9000	0x480B 9FFF	4KiB	L4 interconnect
MCSPI4	0x480B A000	0x480B AFFF	4KiB	Module
	0x480B B000	0x480B BFFF	4KiB	L4 interconnect
Reserved	0x480B C000	0x480D 0FFF	84KiB	Reserved
MMC4	0x480D 1000	0x480D 1FFF	4KiB	Module
	0x480D 2000	0x480D 2FFF	4KiB	L4 interconnect
Reserved	0x480D 3000	0x480D 4FFF	8KiB	Reserved
MMC5	0x480D 5000	0x480D 5FFF	4KiB	Module
	0x480D 6000	0x480D 6FFF	4KiB	L4 interconnect
Reserved	0x480D 7000	0x48FF FFFF	15MiB	Reserved

2.3.4 L4_ABE Memory Space Mapping

The L4_ABE interconnect is a memory space composed of the L4_ABE interconnect configuration registers and the module registers.

ABE modules are dual-mapped inside the MPU/DSP address space:

- Mapped in L3 as the L4 ABE space
- Mapped in MPU and DSP nonshared device map

NOTE: All memory spaces described as modules provide direct access to the module registers outside the L4_ABE interconnect. All other accesses are internal to the L4_ABE interconnect.

Table 2-6 describes the mapping of the registers for the L4_ABE interconnect in the MPU nonshared (private) device address range (L4_ABE).

Table 2-6. ABE MPU Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4_ABE	0x4010 0000	0x4010 3FFF	16KiB	ABE domain (direct MPU access)
Reserved	0x4010 4000	0x4012 1FFF	120KiB	Reserved
MCBSP1	0x4012 2000	0x4012 2FFF	4KiB	Module
	0x4012 3000	0x4012 3FFF	4KiB	L4 interconnect

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Table 2-6. ABE MPU Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
MCBSP2	0x4012 4000	0x4012 4FFF	4KiB	Module
	0x4012 5000	0x4012 5FFF	4KiB	L4 interconnect
MCBSP3	0x4012 6000	0x4012 6FFF	4KiB	Module
	0x4012 7000	0x4012 7FFF	4KiB	L4 interconnect
MCASP	0x4012 8000	0x4012 8FFF	4KiB	McASP CFG port
	0x4012 9000	0x4012 9FFF	4KiB	L4 interconnect
	0x4012 A000	0x4012 AFFF	4KiB	McASP data port
	0x4012 B000	0x4012 BFFF	4KiB	L4 interconnect
Reserved	0x4012 C000	0x4012 DFFF	8KiB	Reserved
DMIC	0x4012 E000	0x4012 EFFF	4KiB	Module
	0x4012 F000	0x4012 FFFF	4KiB	L4 interconnect
WD_TIMER3	0x4013 0000	0x4013 0FFF	4KiB	Module
	0x4013 1000	0x4013 1FFF	4KiB	L4 interconnect
MCPDM	0x4013 2000	0x4013 2FFF	4KiB	Module
	0x4013 3000	0x4013 3FFF	4KiB	L4 interconnect
Reserved	0x4013 4000	0x4013 7FFF	16KiB	Reserved
TIMER5	0x4013 8000	0x4013 8FFF	4KiB	Module
	0x4013 9000	0x4013 9FFF	4KiB	L4 interconnect
TIMER6	0x4013 A000	0x4013 AFFF	4KiB	Module
	0x4013 B000	0x4013 BFFF	4KiB	L4 interconnect
TIMER7	0x4013 C000	0x4013 CFFF	4KiB	Module
	0x4013 D000	0x4013 DFFF	4KiB	L4 interconnect
TIMER8	0x4013 E000	0x4013 EFFF	4KiB	Module
	0x4013 F000	0x4013 FFFF	4KiB	L4 interconnect
Reserved	0x4014 0000	0x4017 FFFF	256KiB	Reserved
DMEM (64KiB)	0x4018 0000	0x4018 FFFF	64KiB	Data memory
	0x4019 0000	0x4019 0FFF	4KiB	L4 interconnect
Reserved	0x4019 1000	0x4019 FFFF	60KiB	Reserved
CMEM (4KiB)	0x401A 0000	0x401A FFFF	64KiB	Coefficient memory
	0x401B 0000	0x401B 0FFF	4KiB	L4 interconnect
Reserved	0x401B 1000	0x401B FFFF	60KiB	Reserved
SMEM (32KiB)	0x401C 0000	0x401C FFFF	64KiB	Module
	0x401D 0000	0x401D 0FFF	4KiB	L4 interconnect
Reserved	0x401D 1000	0x401D FFFF	60KiB	Reserved
AESS configuration	0X401F 1000	0x401F 1FFF	4KiB	Module
	0X401F 2000	0x401F 2FFF	4KiB	L4 interconnect
Reserved	0x401F 3000	0x401F FFFF	52KiB	Reserved

Table 2-7 describes the mapping of the registers for the L3 interconnect.

Table 2-7. ABE L3 Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4_ABE	0x4900 0000	0x4900 3FFF	16KiB	ABE domain (double-mapped for MPU)
Reserved	0x4900 4000	0x4902 1FFF	120KiB	Reserved
MCBSP1	0x4902 2000	0x4902 2FFF	4KiB	Module
	0x4902 3000	0x4902 3FFF	4KiB	L4 interconnect

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Table 2-7. ABE L3 Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
MCBSP2	0x4902 4000	0x4902 4FFF	4KiB	Module
	0x4902 5000	0x4902 5FFF	4KiB	L4 interconnect
MCBSP3	0x4902 6000	0x4902 6FFF	4KiB	Module
	0x4902 7000	0x4902 7FFF	4KiB	L4 interconnect
MCASP	0x4902 8000	0x4902 8FFF	4KiB	MCASP CFG port
	0x4902 9000	0x4902 9FFF	4KiB	L4 interconnect
	0x4902 A000	0x4902 AFFF	4KiB	MCASP data port
	0x4902 B000	0x4902 BFFF	4KiB	L4 interconnect
Reserved	0x4902 C000	0x4902 DFFF	8KiB	Reserved
DMIC	0x4902 E000	0x4902 EFFF	4KiB	Module
	0x4902 F000	0x4902 FFFF	4KiB	L4 interconnect
WD_TIMER3	0x4903 0000	0x4903 0FFF	4KiB	Module
	0x4903 1000	0x4903 1FFF	4KiB	L4 interconnect
MCPDM	0x4903 2000	0x4903 2FFF	4KiB	Module
	0x4903 3000	0x4903 3FFF	4KiB	L4 interconnect
Reserved	0x4903 4000	0x4903 7FFF	16KiB	Reserved
TIMER5	0x4903 8000	0x4903 8FFF	4KiB	Module
	0x4903 9000	0x4903 9FFF	4KiB	L4 interconnect
TIMER6	0x4903 A000	0x4903 AFFF	4KiB	Module
	0x4903 B000	0x4903 BFFF	4KiB	L4 interconnect
TIMER7	0x4903 C000	0x4903 CFFF	4KiB	Module
	0x4903 D000	0x4903 DFFF	4KiB	L4 interconnect
TIMER8	0x4903 E000	0x4903 EFFF	4KiB	Module
	0x4903 F000	0x4903 FFFF	4KiB	L4 interconnect
Reserved	0x4904 0000	0x4907 FFFF	256KiB	Reserved
DMEM (64KiB)	0x4908 0000	0x4908 FFFF	64KiB	Data memory
	0x4909 0000	0x4909 0FFF	4KiB	L4 interconnect
Reserved	0x4909 1000	0x4909 FFFF	60KiB	Reserved
CMEM (4KiB)	0x490A 0000	0x490A FFFF	64KiB	Coefficient memory
	0x490B 0000	0x490B 0FFF	4KiB	L4 interconnect
Reserved	0x490B 1000	0x490B FFFF	60KiB	Reserved
SMEM (32KiB)	0x490C 0000	0x490C FFFF	64KiB	Module
	0x490D 0000	0x490D 0FFF	4KiB	L4 interconnect
Reserved	0x490D 1000	0x490D FFFF	60KiB	Reserved
AESS configuration	0x490F 1000	0x490F 1FFF	4KiB	Module
	0x490F 2000	0x490F 2FFF	4KiB	L4 interconnect
Reserved	0x490F 3000	0x490F FFFF	52KiB	Reserved

Table 2-8 describes the mapping of the registers for the DSP subsystem.

Table 2-8. ABE DSP Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4 ABE	0x0000 0000	0x0000 3FFF	16KiB	Boot space
Reserved	0x0000 4000	0x0002 1FFF	120KiB	Reserved
MCBSP1	0x0002 2000	0x0002 2FFF	4KiB	Module
	0x0002 3000	0x0002 3FFF	4KiB	L4 interconnect

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Table 2-8. ABE DSP Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
MCBSP2	0x0002 4000	0x0002 4FFF	4KiB	Module
	0x0002 5000	0x0002 5FFF	4KiB	L4 interconnect
MCBSP3	0x0002 6000	0x0002 6FFF	4KiB	Module
	0x0002 7000	0x0002 7FFF	4KiB	L4 interconnect
MCASP	0x0002 8000	0x0002 8FFF	4KiB	MCASP CFG port
	0x0002 9000	0x0002 9FFF	4KiB	L4 interconnect
	0x0002 A000	0x0002 AFFF	4KiB	MCASP data port
	0x0002 B000	0x0002 BFFF	4KiB	L4 interconnect
Reserved	0x0002 C000	0x0002 DFFF	8KiB	Reserved
DMIC	0x0002 E000	0x0002 EFFF	4KiB	Module
	0x0002 F000	0x0002 FFFF	4KiB	L4 interconnect
WD_TIMER3	0x0003 0000	0x0003 0FFF	4KiB	Module
	0x0003 1000	0x0003 1FFF	4KiB	L4 interconnect
MCPDM	0x0003 2000	0x0003 2FFF	4KiB	Module
	0x0003 3000	0x0003 3FFF	4KiB	L4 interconnect
Reserved	0x0003 4000	0x0003 7FFF	16KiB	Reserved
TIMER5	0x0003 8000	0x0003 8FFF	4KiB	Module
	0x0003 9000	0x0003 9FFF	4KiB	L4 interconnect
TIMER6	0x0003 A000	0x0003 AFFF	4KiB	Module
	0x0003 B000	0x0003 BFFF	4KiB	L4 interconnect
TIMER7	0x0003 C000	0x0003 CFFF	4KiB	Module
	0x0003 D000	0x0003 DFFF	4KiB	L4 interconnect
TIMER8	0x0003 E000	0x0003 EFFF	4KiB	Module
	0x0003 F000	0x0003 FFFF	4KiB	L4 interconnect
Reserved	0x0004 0000	0x0007 FFFF	256KiB	Reserved
DMEM (64KiB)	0x0008 0000	0x0008 FFFF	64KiB	Data memory
	0x0009 0000	0x0009 0FFF	4KiB	L4 interconnect
Reserved	0x0009 1000	0x0009 FFFF	60KiB	Reserved
CMEM (4KiB)	0x000A 0000	0x000A FFFF	64KiB	Coefficient memory
	0x000B 0000	0x000B 0FFF	4KiB	L4 interconnect
Reserved	0x490B 1000	0x490B FFFF	60KiB	Reserved
SMEM (32KiB)	0x000C 0000	0x000C FFFF	64KiB	Module
	0x000D 0000	0x000D 0FFF	4KiB	L4 interconnect
Reserved	0x000D 1000	0x000D FFFF	60KiB	Reserved
AESS configuration	0x000F 1000	0x000F 1FFF	4KiB	Module
	0x000F 2000	0x000F 2FFF	4KiB	L4 interconnect
Reserved	0x000F 3000	0x000F FFFF	52KiB	Reserved

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2.4 IPU Memory Space Mapping

Table 2-9 describes the mapping of the registers for the IPU subsystem.

Table 2-9. IPU Subsystem Memory Space Mapping

Region Name	Related IP Name	Start Address (hex)	End Address (hex)	Size	Note	Description
IPU_BOOT_SPACE	IPU	0x0000 0000	0x0000 3FFF	16KiB	See (1).	Boot space
L3_MAIN	L3_MAIN	0x0000 0000	0x54FF FFFF	1360MiB		L3_MAIN space: Access to L3 and L4 peripherals
ROM_IPU	IPU	0x5500 0000	0x5500 3FFF	16KiB	See (2).	IPU ROM
Reserved	Reserved	0x5500 0000	0x5501 FFFF	112 KiB		Reserved
RRAM_IPU	IPU	0x5502 0000	0x5502 FFFF	64KiB	See (2).	IPU RAM
Reserved		0x5503 0000	0x5503 FFFF	64KiB		Reserved
ISS	IPU	0x5504 0000	0x5507 FFFF	256KiB	See (2).	ISS: ISP5 and SIMCOP, accessed by IPU master port to ISS
SCACHE_MMU_IPU_CONF_REGS	IPU	0x5508 0000	0x5508 0FFF	4KiB	See (2).	Shared cache and MMU config registers
WUGEN_IPU	IPU	0x5508 1000	0x5508 2FFF	4KiB	See (2).	Local PRCM registers and WKUPGEN masks
SCACHE_MMU_IPU_CONF_REGS	IPU	0x5508 2000	0x5508 2FFF	4KiB	See (2).	L3 shared cache MMU configuration space
Reserved	Reserved	0x5508 3000	0x55FF FFFF	15860KiB		Reserved
L3_MAIN	L3_MAIN	0x5600 0000	0x5FFF FFFF	160MiB		L3_MAIN space
TILER	DMM	0x6000 0000	0x7FFF FFFF	512MiB		Tiled view
EMIFS	EMIFS	0x8000 0000	0xDFFF FFFF	1536MiB		EMIFs
Reserved	Reserved	0xE000 0000	0xE000 0FFF	4KiB		Reserved
DWT_IPU	IPU	0xE000 1000	0xE000 1FFF	4KiB	See (3).	Data watchpoint and trace unit
FPB_IPU	IPU	0xE000 2000	0xE000 2FFF	4KiB	See (3).	Flash patch and breakpoint unit
Reserved	Reserved	0xE000 3000	0xE000 DFFF	44KiB		Reserved
INTC_IPU	IPU	0xE000 E000	0xE000 EFFF	4KiB	See (3).	Interrupt controller
Reserved	Reserved	0xE000 F000	0xE004 1FFF	204KiB		Reserved
ICECRUSHER_IPU	IPU	0xE004 2000	0xE004 2FFF	4KiB	See (3).	ICECrusher™
Reserved	Reserved	0xE004 3000	0xE00F DFFF	748KiB		Reserved
IPU_RW_TABLE	IPU	0xE00F E000	0xE00F EFFF	4KiB	See (3).	RW table
IPU_ROM_TABLE	IPU	0xE00F F000	0xE00F FFFF	4KiB	See (3).	ROM table
EMIFS	EMIFS	0xE010 0000	0xFFFF FFFF	512MiB		Access to LPDDR2 SDRAM

(1) At reset, the MMU is loaded with page 0, which forces the L2 RAM to be at address 0x0. Page 1 is loaded with the physical address of the shared cache MMU register and WUGEN_IPU registers to the virtual address 0x4000 0000.
(2) Can also be accessed by OCP slave port
(3) Different view from each IPU

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2.5 DSP Subsystem Memory Space Mapping

The DSP subsystem can access ABE.

ABE has three address spaces:

- ABE NC: This region is for accesses to registers in ABE. For more information about ABE peripheral memory mapping, see Table 2-6.
- ABE: This region is for accesses to memory in ABE. Memory in the ABE subsystem can be cached in DSP L1 and L2. When eDMA tries to access this space, L1/L2 is snooped and if data is present in DSP subsystem caches, data is provided to eDMA from DSP caches. However, if data is not present in DSP caches, the shared cache sends the access to ABE and data returned is not allocated into DSP cache; instead, it is sent to eDMA.
- ABE locked region: This region is similar to the ABE region, except that data from ABE is allocated into Tesla caches and returned to eDMA.

Table 2-10 describes the mapping of the registers of the DSP subsystem.

Table 2-10. DSP Subsystem Memory Space Mapping

Region Name	Start Address (hex)	End Address (hex)	Size	Description
INTC_DSP	0x0180 0000	0x0180 FFFF	64KiB	Interrupt controller
PDC_CMD	0x0181 0000	0x0181 0FFF	4KiB	PDC command registers
DSP_REV_ID	0x0181 2000	0x0181 2FFF	4KiB	DSP revision ID
EDM	0x01BC 0000	0x01BC 0FFF	4KiB	EDM registers
TPCC_CONFIG_REGS	0x01C0 0000	0x01C0 FFFF	64KiB	TPCC configuration registers
TPTC0_CONFIG_REGS	0x01C1 0000	0x01C1 03FF	1KiB	TPTC0 configuration registers
TPTC1_CONFIG_REGS	0x01C1 0400	0x01C1 07FF	1KiB	TPTC1 configuration registers
SYSC_CONFIG_REGS	0x01C2 0000	0x01C2 0FFF	4KiB	SYSC_CONFIG
WUGEN_DSP	0x01C2 1000	0x01C2 1FFF	4KiB	Wkup generator
SCACHE_DSP_L1	0x01C3 0000	0x01C3 00FF	256B	Shared cache L1 configuration registers
SCACHE_DSP_L2	0x01C3 0200	0x01C3 02FF	256B	Shared cache L2 configuration registers
SCACHE_DSP_DEBUG	0x01C3 0400	0x01C3 05FF	512B	Shared cache debug
SCACHE_DSP_ATTR_MMU	0x01C3 0800	0x01C3 0FFF	2KiB	Shared cache Attr MMU
ABE_NC	0x01D0 0000	0x01DF FFFF	1MiB	ABE NC region
L2_MAIN_DSP	0x01F0 0000	0x01FF FFFF	1MiB	OCP interconnect registers
ABE	0x10D0 0000	0x10DF FFFF	1MiB	ABE region
ABE_LOCKED	0x10E0 0000	0x10EF FFFF	1MiB	ABE locked region
L3_MAIN	0x2000 0000	0xFFFF FFFF	3584MiB	External – SOC Mems and peripherals

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2.6 Display Subsystem Memory Space Mapping

The display subsystem integrates a display controller (DISPC), a remote frame buffer interface (RFBI), two MIPI® display serial interfaces (DSI1_A and DSI1_C), and a high-definition multimedia interface (HDMI, digital part) link with its PHY.

The DISPC is connected through an interconnect master port to the L3 interconnect and has its own DMAs to fetch the data from the system memory.

2.6.1 L3 Interconnect View of the Display Memory Space

Table 2-11 lists the memory space mapping in the display subsystem from the perspective of the MPU subsystem through the L3 interconnect.

Table 2-11. L3 Access – Display Subsystem Space Mapping

Region Name	Start Address (hex)	End Address (hex)	Size	Description
TP_DSS_TARG	0x5800 0000	0x5800 0FFF	4KiB	Display subsystem and DSI registers
TP_DISPC_TARG	0x5800 1000	0x5800 1FFF	4KiB	Display controller
TP_RFBI_TARG	0x5800 2000	0x5800 2FFF	4KiB	Remote frame buffer interface
Reserved	0x5800 3000	0x5800 3FFF	4KiB	Reserved
TP_DSI1_A_TARG	0x5800 4000	0x5800 4FFF	4KiB	Display serial interface A
Reserved	0x5800 5000	0x5800 8FFF	16KiB	Reserved
TP_DSI1_C_TARG	0x5800 9000	0x5800 9FFF	4KiB	Display serial interface C
Reserved	0x5800 A000	0x5805 FFFF	344KiB	Reserved
Reserved	0x5800 A000	0x587F FFFF	8152KiB	Reserved

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Power, Reset, and Clock Management

This chapter describes the power, reset, and clock management in the device.

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3.1 Device Power Management Introduction

Power management (efficient use of the limited battery resources on a mobile device) is one of the most important design aspects of any mobile system. It imposes strong control over limited available power resources to ensure they function for the longest possible length of time.

The device power-management architecture ensures maximum performance and operation time for user satisfaction (audio/video support) while offering versatile power-management techniques for maximum design flexibility, depending on application requirements.

This introduction contains the following information:

- Power-management architecture building blocks for the device
- State-of-the-art power-management techniques supported by the power-management architecture of the device

3.1.1 Device Power-Management Architecture Building Blocks

To provide a versatile architecture that supports multiple power-management techniques, the power-management framework is built with three levels of resource management: clock, power, and voltage.

These management levels are enforced by defining the managed entities or building blocks of the power-management architecture, called the clock, power, and voltage domains.

A domain is a group of modules or subsections of the device that share a common entity (for example, common clock source, common voltage source, or common power switch). The group forming the domain is managed by a policy manager. For example, a clock for a clock domain is managed by a dedicated clock manager within the power, reset, and clock management (PRCM) module. The clock manager considers the joint clocking constraints of all the modules belonging to that clock domain (and, hence, receiving that clock).

NOTE: In the following sections, the term <*module*> is used to represent the device IPs (that is, modules or subsystems), other than the PRCM module, that receive clock, reset, or power signals from the PRCM module.

3.1.1.1 Clock Management

The PRCM module manages the gating (that is, switching off) and enabling of the clocks to the device modules. The clocks are managed based on the requirement constraints of the associated modules. The following sections identify the module clock characteristics, management policy, clock domains, and clock domain management.

3.1.1.1.1 Module Interface and Functional Clocks

Each module within the device has specific clock input characteristics requirements. Based on the characteristics of the clocks delivered to the modules, the clocks are divided into two categories: interface clocks and functional clocks (see Figure 3-1).

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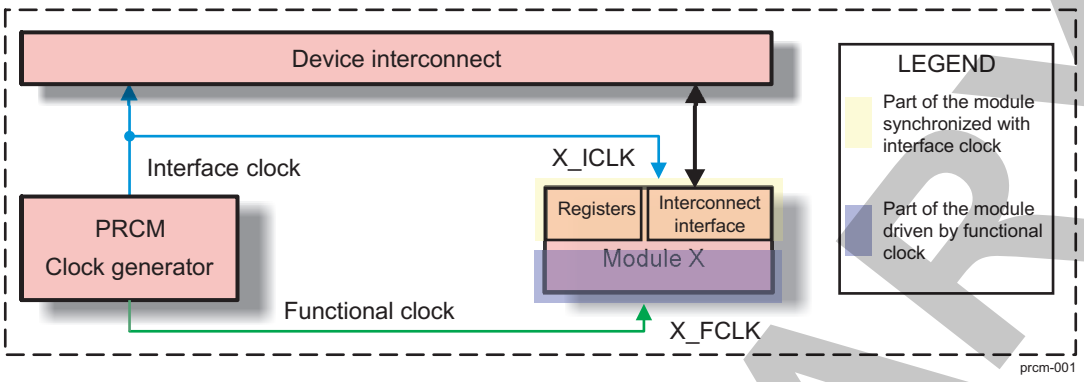
Figure 3-1. Functional and Interface Clocks



The interface clocks have the following characteristics:

- They ensure proper communication between any module/subsystem and the interconnect.
- In most cases, they supply the system interconnect interface and registers of the module.
- A typical module has one interface clock, but modules with multiple interface clocks may also exist (that is, when connected to multiple interconnect buses).
- Interface clock management is done at the device level.
- From the standpoint of the PRCM module, an interface clock is identified with an _ICLK suffix.

Functional clocks have the following characteristics:

- They supply the functional part of a module or subsystem.
- A module can have one or more functional clocks. Some functional clocks are mandatory, while others are optional. A module needs its mandatory clock(s) to be operational. The optional clocks are used for specific features and can be shut down without stopping the module activity (for example, the clock for the camera).
- From the standpoint of the PRCM module, a functional clock is distributed directly to the related modules through a dedicated clock tree. It is identified with an _FCLK suffix.

Some clocks are qualified as permanent clocks. They are functional clocks, that can stay active while the corresponding entity manages them.

NOTE: At the module level, the interface clocks are always fed by the interface clock outputs of the PRCM module. The functional clocks are fed by a PRCM module functional clock output or a PRCM module interface clock output. In the latter case, the functional and interface module clocks inherit the clock-management features (autoidle features) of the PRCM module interface clock.

3.1.1.1.2 Module-Level Clock Management

Each module in the device may also have specific clock requirements. Certain module clocks must be active when operating in specific modes, or they may be gated. Globally, the activation and gating of the module clocks are managed by the PRCM module. Hence, the PRCM module must be aware of when to activate and when to gate the module clocks.

The PRCM module differentiates the clock-management behavior for device modules based on whether the module can initiate transactions on the device interconnect (called master module) or it cannot initiate transactions and only responds to the transactions initiated by the master (called slave module). Thus, two hardware-based power-management protocols are used:

- Master standby protocol: Clock-management protocol between the PRCM and master modules
- Slave idle protocol: Clock-management protocol between the PRCM and slave modules

Master standby protocol

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This protocol is used to indicate that a master module must initiate a transaction on the device interconnect and requests specific (functional and interface) clocks for that purpose. The PRCM module ensures that the required clocks are active when the master module requests the PRCM module to enable them. This is called a module wake-up transition and the module is said to be functional after this transition completes.

Similarly, when the master module no longer requires the clocks, it informs the PRCM module, which can then gate the clocks to the module. The master module is then said to be in standby mode.

Although the protocol is completely hardware-controlled, software must configure the clock-management behavior for the module. This is done by setting the <*Module*>_SYSCONFIG. MIDLEMODE or <*Module*>_SYSCONFIG. STANDBYMODE bit fields, as described in Table 3-1. The behavior, identified in the STANDBYMODE Bit Value column, must be configured.

Table 3-1. Master Module Standby Mode Settings

STANDBYMODE Bit Value	Selected Mode	Description
0x0	Force-standby	The module unconditionally asserts the standby request to the PRCM module, regardless of its internal operations. The PRCM module may gate the functional and interface clocks to the module. This mode must be used carefully because it does not prevent loss of data at the time the clocks are gated.
0x1	No-standby	The module never asserts the standby request to the PRCM module. This mode is safe from a module point of view because it ensures that the clocks remain active; however, it is not efficient from a power-saving perspective because it never allows the PRCM module output clocks to be gated.
0x2	Smart-standby	The module asserts the standby request based on its internal activity status. The standby signal is asserted only when all ongoing transactions are complete and the module is idled. The PRCM module can then gate the clocks to the module.
0x3	Smart-standby wake-up-capable mode	The module asserts the standby request based on its internal activity status. The standby signal is asserted only when all ongoing transactions are complete and the module is idle. The PRCM module can then gate the clocks to the module. The module may generate (master-related) wake-up events when in standby state. The mode is relevant only if the appropriate module mwakeup output is implemented.

NOTE:

- Smart-standby mode is the preferred mode of operation, while force-standby and no-standby modes are intended for debugging purposes.
- A master module may support all or some of the standby modes listed in Table 3-1. See the power-management section in the module chapter to identify the supported standby mode.

The standby status of a master module is indicated by the CM_<*Power domain*>_<*Module*>_CLKCTRL[x]. STBYST bit in the PRCM module. Table 3-2 describes the master module standby status.

Table 3-2. Master Module Standby Status

STBYST Bit Value	Description
0x0	The module is functional.
0x1	The module is in standby mode.

Table 3-3 lists the enabling conditions for the master module clocks managed by the standby protocol.

Table 3-3. Master Module Clock Enabling Conditions

Relation		Condition
AND		Clock domain is ready.
	OR	Master module standby request is deasserted.

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Table 3-3. Master Module Clock Enabling Conditions (continued)

Relation		Condition
		Master module wake-up request is asserted.

Slave idle protocol

This hardware protocol allows the PRCM module to control the state of a slave module. The PRCM module informs the slave module, through assertion of an IDLE request, when its clocks (interface and functional) can be gated. The slave can then acknowledge the request from the PRCM module, and the PRCM module is then allowed to gate the clocks to the module. A slave module is said to be in IDLE state when its clocks are gated by the PRCM module.

Similarly, an idled slave module may need to be woken up because of a service request from a master module or because the slave module receives a wake-up event (for example, an interrupt or a direct memory access [DMA] request). In this situation the PRCM module enables the clocks for the module, and then signals the module to wake up by deasserting the IDLE request.

Although the protocol is completely hardware-controlled, software must configure the clock-management behavior for the slave module. This is done by setting the <*Module*>_SYSCONFIG. SIDLEMODE or <*Module*>_SYSCONFIG. IDLEMODE bit field, as described in Table 3-4. The behavior, identified in the IDLEMODE Bit Value column, must be configured by software.

Table 3-4. Module Idle Mode Settings

IDLEMODE Bit Value	Selected Mode	Description
0x0	Force-idle	The module unconditionally acknowledges the IDLE request from the PRCM module, regardless of its internal operations. This mode must be used carefully because it does not prevent loss of data at the time the clock is switched off.
0x1	No-idle	The module never acknowledges any IDLE request from the PRCM module. This mode is safe from a module point of view because it ensures the clocks remain active; however, it is not efficient from a power-saving perspective because it does not allow the PRCM module output clock to be shut off, and thus the power domain to be set to a lower power state.
0x2	Smart-idle	The module acknowledges the IDLE request, basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions, interrupts, or DMA requests are processed. This is the best approach to efficient system power management.
0x3	Smart-idle wake-up-capable mode	The module acknowledges the IDLE request, basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions, interrupts, or DMA requests are processed. This is the best approach to efficient system power management. The module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state. The mode is relevant only if the appropriate module swakeup output(s) is implemented.

NOTE:

- Smart-idle mode is the preferred mode of operation, while force-idle and no-idle modes are intended for debugging purposes.
- A slave module may support all or some of the idle modes listed in Table 3-4. See the power-management section in the module chapter to identify the supported idle modes.

The idle status of a slave module is indicated by the CM_<*Power domain*>_<*Module*>_CLKCTRL[x] IDLEST bit field in the PRCM module. Table 3-5 lists the possible idle statuses for a slave module.

Table 3-5. Slave Module Idle Status

IDLEST Bit Value	Idle Status	Description
0x0	Functional	The module is fully functional. The interface and functional clocks are active.
0x1	In transition	The module is performing a wake-up or a sleep transition.

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Table 3-5. Slave Module Idle Status (continued)

IDLEST Bit Value	Idle Status	Description
0x2	Interface idle	The module interface clock is idled. The module may remain functional if using a separate functional clock.
0x3	Full idle	The module is fully idle. The interface and functional clocks are gated.

When configured in smart-idle mode, the slave module may acknowledge the IDLE request of the PRCM module based on the activity of its interface and/or functional clocks. To define which module clocks (that is, interface and/or functional) should be considered when responding to the PRCM module request, software must configure the <*Module*>_SYSCONFIG[x] CLOCKACTIVITY bit field.

The CLOCKACTIVITY setting is used internally by the module to determine the part of the module on which the conditions to acknowledge the PRCM module IDLE request are tested. As an example, if the functional clock must remain active when the module is in idle mode, the module must acknowledge a PRCM module IDLE request by considering only the interface clock gating conditions (that is, there is no pending activity on the interconnect).

NOTE: See the power-management section in the module chapter to identify whether this feature is configurable.

Using the CLOCKACTIVITY setting along with smart-idle mode ensures that the clock remains active for the module features that must remain available during the module idle mode. Table 3-6 describes the possible CLOCKACTIVITY settings for a module.

Table 3-6. Slave Module Clock Activity Settings

CLOCKACTIVITY Bit Value	Module Interface Clock	Module Functional Clock	Description
0x0	Gated	Gated	The interface and functional clocks are considered when generating the acknowledgment. This setting also means both clocks may be gated upon a PRCM module IDLE request.
0x1	Active	Gated	The interface clock is not shut down and is not considered when generating the acknowledgment to the PRCM module IDLE request. Only the functional clock is considered.
0x2	Gated	Active	The functional clock is not shut down and is not considered when generating the acknowledgment to the PRCM module IDLE request. Only the interface clock is considered.
0x3	Active	Active	The interface and functional clocks are not shut down. The module can acknowledge the IDLE request without checking the internal functions linked to its clocks.

NOTE:

- The software configuration of the CLOCKACTIVITY settings may not be available for a given module. For some modules, the CLOCKACTIVITY settings can be hardwired.
- A slave module may support all or some of the CLOCKACTIVITY settings listed in Table 3-6.

See the power-management section in the specific module chapter to identify the supported idle feature and settings.

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The PRCM module does not have any hardware means to read the CLOCKACTIVITY settings of the module. Software must ensure consistent programming between the CLOCKACTIVITY settings of the module and the clock-gating control bits in the PRCM module. The PRCM module must be configured (where software control is available) not to gate the module clock, which should remain active according to the CLOCKACTIVITY settings of the module.

For idle protocol management on the PRCM module side, the behavior of the PRCM module is configured in the CM_<Power domain>_<module>_CLKCTRL[x] MODULEMODE bit field. Based on the configured behavior, the PRCM module asserts the IDLE request to the module unconditionally (that is, immediately when software requests) or through hardware control when the module idle conditions are satisfied. Table 3-7 describes the configurable behavior of MODULEMODE.

Table 3-7. Slave Module Mode Settings in PRCM

MODULEMODE Bit Value	Selected Mode	Description
0x0	Disabled	The PRCM module unconditionally asserts the module IDLE request. This request applies to the gating of the functional and interface clocks to the module. If acknowledged by the module, the PRCM module can gate all clocks to the module (that is, the module is completely disabled). It can react only to an asynchronous wake-up event (that is, a wake-up event that does not require the module functional clock to be active).
0x1	Auto	This mode applies to a module when the PRCM module manages only its interface clock and not its functional clock. The PRCM module automatically asserts/deasserts the module IDLE request based on the clock domain transitions. If acknowledged by the module, the PRCM module can gate the interface clock to the module.
0x2	Enabled	This mode applies to a module when the PRCM module manages its interface and functional clocks. The functional clock to the module remains active unconditionally, while the PRCM module automatically asserts/deasserts the module IDLE request based on the clock domain transitions. If acknowledged by the module, the PRCM module can gate only the interface clock to the module.
0x3	Reserved	Not available

NOTE: The PRCM module may support all or some of the MODULEMODE module settings listed in Table 3-7. See the CM_<Power domain>_<module>_CLKCTRL[x] MODULEMODE bit field description for the module to identify the supported settings.

NOTE: Modules, which can be configured with DISABLED or AUTO values of ModuleMode, cannot go from IDLE to DISABLED state if ModuleMode is changed from AUTO to DISABLED while module is in IDLE state. To Perform this transition domain has to be put in force wakeup (CM_<Clock domain>_CLKSTCTRL[1:0] CLKTRCTRL = SW_WKUP).

Table 3-8 and Table 3-9 list the enabling conditions for the slave module clocks managed by the idle protocol.

Table 3-8. Slave Module Interface Clock Enabling Conditions

Relation		Condition
AND		Clock domain is ready.
	OR	Slave module idle status is 0x0 (fully functional).
		Slave module idle status is 0x1 (in transition).
		Slave module wake-up request is asserted.

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Table 3-9. Slave Module Functional Clock Enabling Conditions

Relation		Condition
AND		Clock domain is ready.
	OR	Slave module idle status is 0x0 (fully functional).
		Slave module idle status is 0x1 (in transition).
		Slave module idle status is 0x2 (interface clock is idled).
		Slave module wake-up request is asserted.

The module clock domain must be ready for the optional clocks to the module, and any associated clock-enable control is asserted.

NOTE: A given clock can be used by more that one module. Clock-enabling conditions are then ORed together (that is, the clock is provided as soon as one of the enabling conditions is true). As a consequence, the clock is disabled only when all related enabling conditions are false.

Module wake-up request

In IDLE state, a slave module may have to wake up to generate an interrupt or a DMA request. This can be the result of an external request (for example, to the input/output [I/O] port of a general-purpose input/output [GPIO] module) or an internally generated event (for example, WD_TIMER time up). The slave module, with wake-up capability, sends a wake-up request to the PRCM module. The PRCM module then activates the module clocks and acknowledges the module wake-up request.

In IDLE state, some slave modules may require functional clock(s) to generate a wake-up event. Such requests are called synchronous wake-up events on the PRCM module side, while the events generated when the functional or interface module clocks are gated are called asynchronous wake-up events.

NOTE: See the power-management section in the module chapter to identify whether its wake-up event is synchronous or asynchronous.

The standby and idle clock-management protocols allow the configuration of the module-level clock-management interaction between the PRCM module and individual modules of the device. However, the PRCM module may not necessarily gate the clock to the module immediately after the module switches to standby or idle mode at the end of this interaction. This is because the same clock can be shared by other modules that are active and need this shared clock to complete their activity. As a result, the PRCM module provides a second level of clock management called the clock-domain level, as explained in Section 3.1.1.1.3, *Clock Domain*.

3.1.1.1.3 Clock Domain

A clock domain is a group of modules fed by clock signals controlled by the same clock manager in the PRCM module (see Figure 3-2). By gating the clocks in a clock domain, the clocks to all the modules belonging to that clock domain can be cut to lower their active power consumption (that is, the device is on and the clocks to the modules are dynamically switched to ACTIVE or INACTIVE [gated] state). Thus, a clock domain allows control of the dynamic power consumption of the device.

The device is partitioned into multiple clock domains and each clock domain is controlled by an associated clock manager within the PRCM module. This allows the PRCM module to activate and gate individually each device clock domain.

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Figure 3-2. Generic Clock Domain

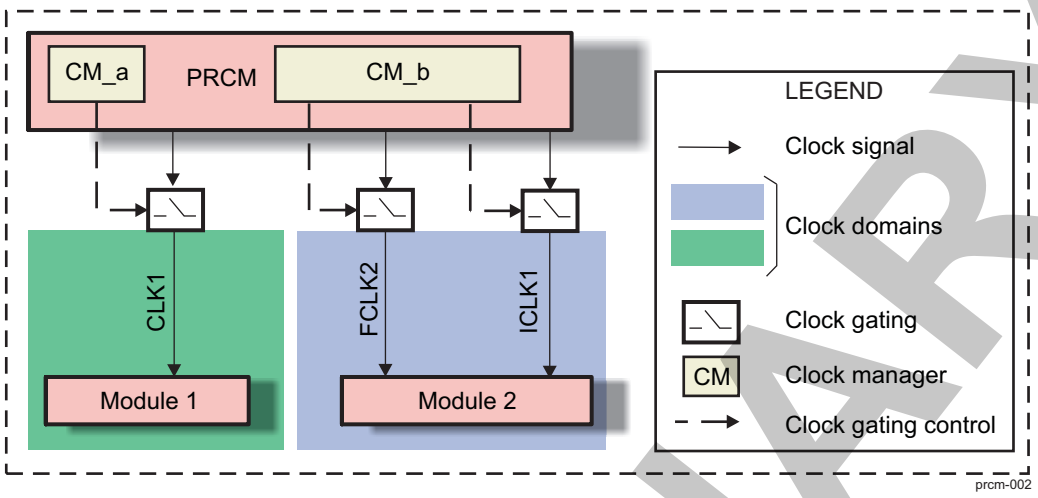

Figure 3-2 is an example of two clock managers: CM_a and CM_b. Each clock manager manages a clock domain. The clock domain of CM_b is composed of two clocks, a functional clock (FCLK2) and an interface clock (ICLK1), while that of CM_a consists of a clock (CLK1) that is used by the module as functional and interface clock. The clocks to Module 2 can be gated independently of the clock to Module 1, thus ensuring power savings when Module 2 is not in use.

The PRCM module lets software check the status of the clock domain functional clocks. The CM_<Clock domain>_CLKSTCTRL[x] CLKACTIVITY_FCLK/<Clock name>_FCLK bit in the PRCM module identifies the state of the functional clock(s) within the clock domain. Table 3-10 lists the two possible states of the functional clock.

Table 3-10. Clock Domain Functional Clock States

CLKACTIVITY Bit Value	Status	Description
0x0	Gated	The functional clock of the clock domain is inactive.
0x1	Active	The functional clock of the clock domain is running.

3.1.1.1.4 Clock Domain-Level Clock Management

The domain clock manager can automatically (that is, based on hardware conditions) and jointly manage the interface clocks within the clock domain. The functional clocks within the clock domain are managed through software settings.

A clock domain can switch between three possible states: ACTIVE, IDLE_TRANSITION (IDLEREQ), and INACTIVE (IDLE). Figure 3-3 shows the sleep and wake-up transitions of the clock domain between ACTIVE and INACTIVE states.

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Figure 3-3. Clock Domain State Transitions

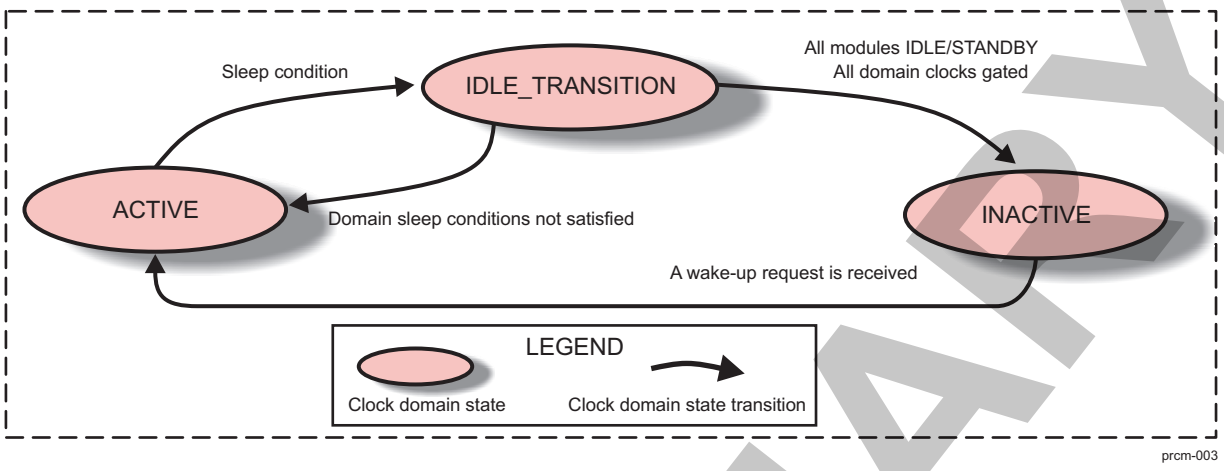

Table 3-11 defines the clock domain states.

Table 3-11. Clock Domain Clock States

State	Description
ACTIVE	• Every nondisabled slave module (that is, those whose MODULEMODE value is not set to disabled) is put out of IDLE state. • All functional clocks to the active slave modules (that is, not idled) of the clock domain are provided. • All interface clocks to the nondisabled slave modules in the clock domain are provided. • All functional and interface clocks to the active master modules (that is, not in STANDBY state) in the clock domain are provided. • Every enabled optional clock to the modules in the clock domain is provided.
IDLE_TRANSITION	This is a transitory state. • Every master module in the clock domain is in STANDBY state. • Every IDLE request to all the slave modules in the clock domain is asserted. • The functional clocks to the slave module in enabled state (that is, those whose MODULEMODE values are set to enabled) remain active. • Every enabled optional clock to the modules in the clock domain is provided.
INACTIVE	All clocks within the clock domain are gated. • Every slave module in the clock domain (that is, those whose MODULEMODE value is set to disabled or auto) is in IDLE state and set to disabled or auto mode. • Every master module in the clock domain is in STANDBY state. • Every optional functional clock in the clock domain is gated.

Each clock domain transition behavior is managed by an associated register bit field in the CM_<Clock domain>_CLKSTCTRL[x] CLKTRCTRL PRCM module.

Table 3-12 describes the clock transition mode settings of the clock domain.

Table 3-12. Clock Domain Clock Transition Mode Settings

CLKTRCTRL Bit Value	Selected Mode	Description
0x0	NO_SLEEP	A clock domain sleep transition is never initiated, regardless of the hardware conditions.
0x1	SW_SLEEP	A software-forced sleep transition. The transition is initiated when the associated hardware conditions are satisfied (see Table 3-14).
0x2	SW_WKUP	A software-forced clock domain wake-up transition is initiated, regardless of the hardware conditions identified in Table 3-13.

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Table 3-12. Clock Domain Clock Transition Mode Settings (continued)

CLKTRCTRL Bit Value	Selected Mode	Description
0x3	HW_AUTO	Hardware-controlled automatic sleep and wake-up transition is initiated by the PRCM module when the associated hardware conditions are satisfied (see Table 3-13 and Table 3-14).

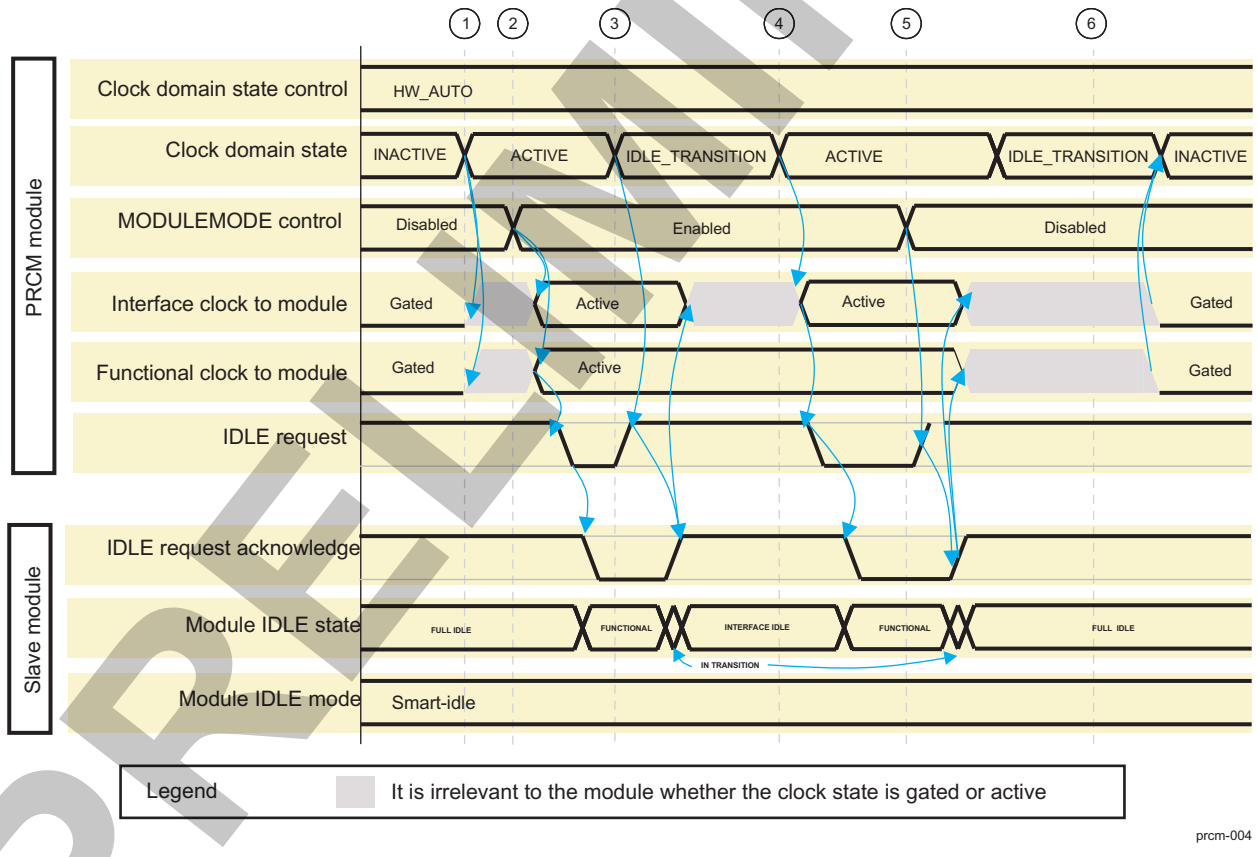
NOTE: Depending on its characteristics, a clock domain may or may not support all the clock transition mode settings described in Table 3-12. See the clock domain clock management section of the specific clock domain to identify the supported clock transition mode settings.

3.1.1.1.5 Clock Domain HW_AUTO Mode Sequences

The sequence diagrams in Figure 3-4 through Figure 3-6 identify the PRCM module hardware-controlled enabling and gating of the functional and interface clocks to the module. They show the changes in the state of the module based on the changes to the clock domain state and module mode settings.

Figure 3-4 shows the behavior of a slave module receiving the interface and functional clocks and having two configurable module modes: disabled and enabled.

Figure 3-4. Clock Domain/Slave Module Clock-Management Interaction Sequence 1



Initially, the clock domain, which includes the slave module, is inactive. The module is in FULL IDLE state and its functional and interface clocks are gated.

1. The clock domain wakes up and changes its state to ACTIVE. Because the MODULEMODE control is still disabled, this event has no effect on the state of the module. The functional and interface clocks can still be restarted automatically, based on the requirements of other modules sharing these clocks.

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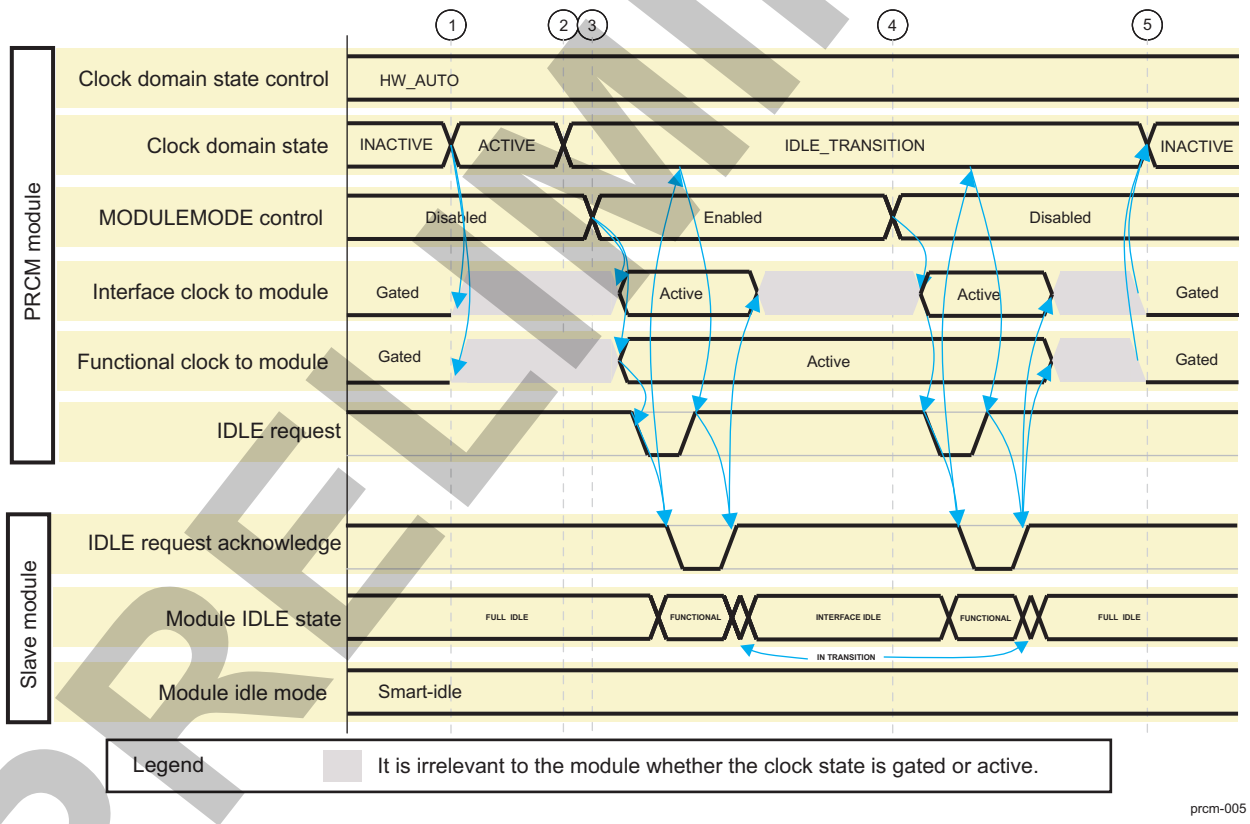
2. Software changes the module mode to enabled. The clocks to the module are automatically restarted. The PRCM module then deasserts a hardware IDLE request signal to the module. The module sends an IDLE request acknowledge to the PRCM module. The module is now effectively awake. The module IDLE state is functional. If the module is enabled before the clock domain wakes up, Steps 1 and 2 are simultaneous.
3. The clock domain switches to IDLE_TRANSITION state. In turn, the PRCM module requests the module to go into IDLE state by asserting the IDLE request signal. When acknowledged, the clock to the module can be gated, depending on other modules sharing the same clock. The functional clock of the module remains enabled because the module is in enabled mode.
4. The clock domain does not have all conditions to complete the sleep transition and wakes up again. In turn, the interface clock to the module is automatically restarted, if applicable, and then the module is put out of IDLE state.
5. Software disables the module. The PRCM module requests the module to go to IDLE state by asserting the IDLE request signal. When acknowledged, the clock to the module can be gated, depending on other modules sharing the same clock.
6. The clock domain switches to IDLE_TRANSITION state. When the sleep transition conditions of the clock domain are satisfied, the clocks (functional and interface) are gated. The clock domain then switches to INACTIVE state. This has no effect on the module, which is already in FULL IDLE state.

Figure 3-5 shows the behavior of the same slave module, receiving the interface and functional clocks, when the module mode is changed while the clock domain state is IDLE_TRANSITION.

Figure 3-5. Clock Domain/Slave Module Clock-Management Interaction Sequence 2



Initially, the clock domain, which includes the slave module, is inactive. The module is in FULL IDLE state and its functional and interface clocks are gated.

1. The clock domain wakes up and changes its state to ACTIVE. Because the MODULEMODE control is disabled, this event has no effect on the state of the module. The functional and interface clocks can still be restarted automatically, based on the requirements of other modules sharing these clocks.
2. The clock domain goes into the IDLE_TRANSITION state. Because the module mode control is disabled, this event has no effect on the module state.

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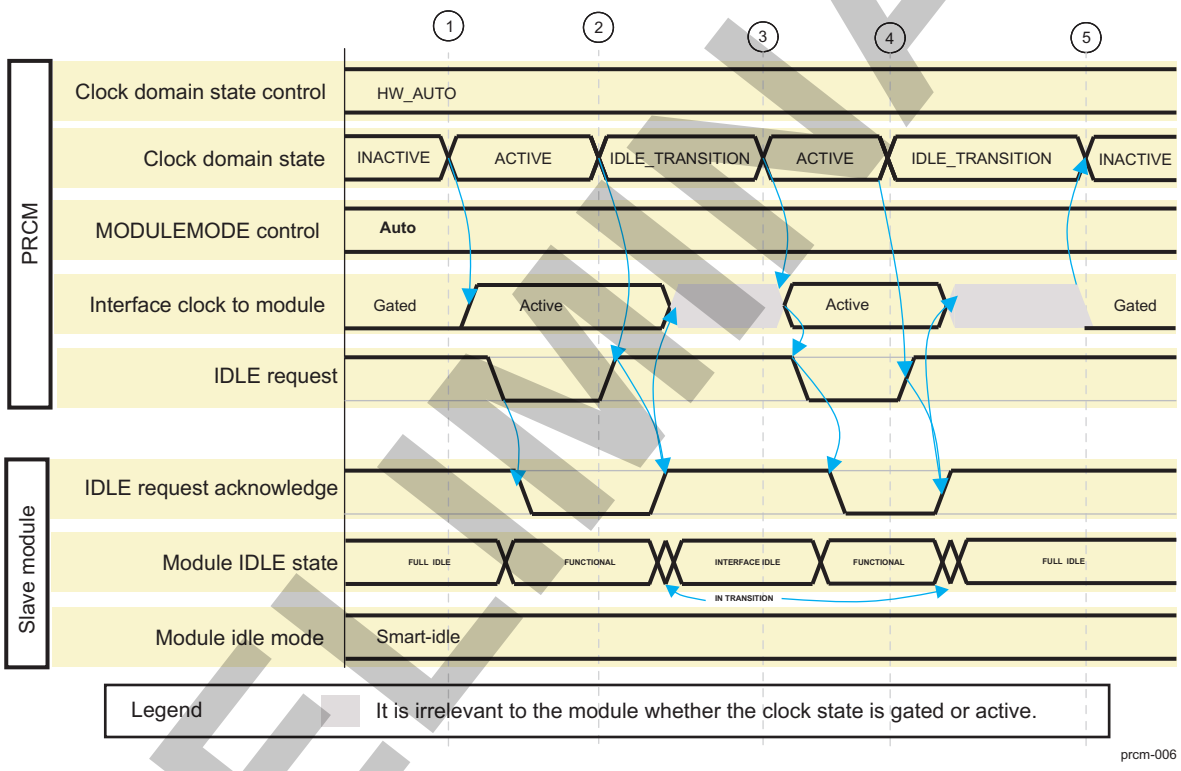
3. Software changes the module mode to enabled. The clocks to the module are restarted automatically and then the module is put out of IDLE state. As soon as acknowledged, the module is requested to go back to IDLE state with gating of the interface clock only (that is, the INTERFACE IDLE state). The interface clock to the module can be gated, depending on other modules sharing the same clocks.
4. Software disables the module. The interface clock to the module is restarted automatically. The PRCM module requests the module to go to IDLE state by asserting the IDLE request signal. When acknowledged, the interface and the functional clocks to the module can be gated, depending on other modules sharing the same clock.
5. When the clock domain sleep transition conditions are satisfied and the functional and interface clocks are gated, the clock domain switches to INACTIVE state. This has no effect on the module, which is already in FULL IDLE state.

Figure 3-6 shows the behavior of a slave module receiving only interface clock and supporting the configurable auto module mode.

Figure 3-6. Clock Domain/Slave Module Clock-Management Interaction Sequence 3



Initially, the clock domain, which includes the slave module, is inactive. The module is in FULL IDLE state and its interface clock is gated.

1. The clock domain wakes up and changes its state to ACTIVE. In turn, the interface clock to the module is automatically restarted. The PRCM module then deasserts a hardware IDLE request signal to the module. The module sends an IDLE request acknowledge to the PRCM module. The module is now effectively awake; that is, the module IDLE state is functional.
2. The clock domain switches to IDLE_TRANSITION state. The PRCM module requests the module to go to IDLE state by asserting the IDLE request signal. When acknowledged, the interface clock to the module can be gated, depending on other modules sharing the same clock.
3. The clock domain does not have all conditions to complete the sleep transition and wakes up again. In turn, the interface clock to the module is automatically restarted, if applicable, and then the module goes out of IDLE state.
4. This step is the same as Step 2.
5. The clock domain has all conditions to complete the sleep transition. The module is in IDLE state and its clock is gated.

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3.1.1.1.6 Clock Domain Sleep/Wake-up

The clock domain manager initiates a domain wake-up transition when the conditions listed in Table 3-13 are satisfied.

Table 3-13. Clock Domain Wake-Up Conditions

Relation	Condition
OR	The SW_WKUP clock transition mode for the clock domain is set (CLKTRCTRL = 0x2).
	At least one wake-up request is asserted by one of the modules of the clock domain.
	At least one dynamic dependency(1) from another clock domain is active.
	At least one static dependency(1) from another clock domain is active.
	At least one wake-up dependency(1) from a module in another clock domain is active.

(1) The dynamic, static, and wake-up dependencies are explained in Section 3.1.1.1.7, *Clock Domain Dependency*.

The clock domain manager initiates a domain sleep transition when the conditions listed in Table 3-14 are satisfied.

Table 3-14. Clock Domain Sleep Conditions

Relation		Condition
AND		All master modules in the clock domain are in STANDBY state.
		No wake-up request is asserted by any module of the clock domain.
		No dynamic domain dependency(1) from any other domain is active.
		No wake-up dependency(1) from any module in another domain is active.
		No static domain dependency(1) from any other domain is active.
	OR	The SW_SLEEP clock transition mode is set for the clock domain (CLKTRCTRL = 0x1).
		The HW_AUTO clock transition mode is set for the clock domain (CLKTRCTRL = 0x3).

(1) The dynamic, static, and wake-up dependencies are explained in Section 3.1.1.1.7, *Clock Domain Dependency*.

3.1.1.1.7 Clock Domain Dependency

A domain dependency is a binary relationship between two clock domains. A clock domain A is said to depend on a clock domain B when a module in clock domain B provides services to a module in clock domain A. As a result, clock domain B must be active when clock domain A is active so that the module in clock domain B is accessible by the module in clock domain A.

Dependency between two clock domains can also exist if one clock domain serves to ensure communication between two modules (for example, the clock domain of the device interconnect).

Thus, a clock domain can support the types of clock domain dependencies described in the following sections.

Table 3-15 and Table 3-16 detail all the domain dependencies:

- **NA/NA**: if no dependency can exist because no corresponding interconnect path exists in the device
- When cell is different than NA/NA, the cell contains two attributes:
  - First attribute for the presence and control method of a static dependency:
    - **SW**: Static dependency is controlled by a software bit. This is the most generic way of control. Depending on the use case and on latency requirement for accessing target domain, software can enable or not the static dependency. When not enabled, access to those domains is performed using dynamic dependencies.
    - **1**: Static dependency is always enabled (hard-wired). This is relevant for a domain that has an "exact standby" system initiator with the target domain being the domain containing the interconnect module to which the initiator is connected.
    - **0**: Static dependency is never enabled (hard-wired). This is relevant for domains that do not have strong access latency requirements, or for which a static dependency is not desired for

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specific reasons (for example, dependencies with emulation domain). Access to those domains is performed using dynamic dependencies.

- **NA**: Nonapplicable (means domain has no system initiator able to access the other domain)

– Second attribute for the presence and control method of a dynamic dependency:

- **1..n**: Dynamic dependency is always enabled (hard-wired). The number of corresponding interconnect interfaces is also specified. This is relevant for most of the domain-to-domain direct interconnect connection.
- **0**: Dynamic dependency is never enabled (hard-wired). This is relevant only when a static dependency is always enabled between same domains, or when the target domain cannot support the wakeup on access feature.
- **NA**: Nonapplicable (means that both domains are not directly linked by an OCP interface)

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Table 3-15. Device Domain Dependencies (Table 1)

Static/dynamic dependencies from below domains to right-side domains	ABE	L4_CFG	DMA_SYSTEM	EMIF	IPU	L3_INSTR	L3_MAIN1	L3_MAIN2	COREAON	CUSTEFUSE
CAM	0/NA	0/NA	0/NA	SW/NA	0/NA	0/NA	SW/NA	1/0	0/NA	0/NA
L4_CFG	NA/NA	NA/NA	0/1	0/1	NA/NA	0/0	0/1	0/13	0/3	0/1
DMA_SYSTEM	SW/NA	SW/NA	NA/NA	SW/NA	SW/NA	0/NA	SW/NA	1/0	0/NA	0/NA
IPU	SW/NA	SW/NA	0/NA	SW/NA	NA/NA	0/NA	SW/NA	SW/1	0/NA	0/NA
L3_INSTR	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA
L3_MAIN1	0/1	0/1	0/NA	0/2	0/NA	0/0	NA/NA	0/1	0/NA	0/NA
L3_MAIN2	0/NA	0/NA	0/NA	0/NA	0/1	0/0	0/1	NA/NA	0/NA	0/NA
DSP	SW/1	SW/NA	0/NA	SW/NA	0/NA	0/NA	SW/1	SW/NA	0/NA	0/NA
DSS	0/NA	0/NA	0/NA	SW/NA	0/NA	0/NA	1/0	1/0	0/NA	0/NA
EMU	0/NA	0/NA	0/NA	0/NA	0/NA	0/NA	0/NA	0/1	0/NA	0/NA
GPU	0/NA	0/NA	0/NA	SW/NA	0/NA	0/NA	SW/NA	1/ 0	0/NA	0/NA
IVA	0/NA	0/NA	0/NA	SW/NA	0/NA	0/0	SW/NA	1/0	0/NA	0/NA
L3_INIT	SW/NA	SW/NA	0/NA	SW/NA	0/NA	0/NA	1/0	1/0	0/NA	0/NA
L4_PER	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA	NA/NA
L4_SEC	0/NA	0/NA	0/NA	SW/NA	0/NA	0/NA	SW/NA	1/0	0/NA	0/NA
MPU	SW/1	SW/NA	0/NA	SW/2	SW/NA	0/NA	SW/1	SW/NA	0/NA	0/NA

Table 3-16. Device Domain Dependencies (Table 2)

Static/dynamic dependencies from below domains to right-side domains	CAM	DSP	DSS	EMU	GPU	IVA	L3_INIT	L4_PER	L4_SEC	MPU	WKUPAON
CAM	NA/NA	0/NA	0/NA	0/NA	0/NA	SW/NA	0/NA	0/NA	0/NA	0/NA	0/NA
L4_CFG	0/0	0/1	0/1	NA/NA	NA/NA	NA/NA	0/9	NA/NA	NA/NA	0/1	NA/NA
DMA_SYSTEM	0/NA	0/NA	SW/NA	0/NA	0/NA	SW/NA	SW/NA	SW/NA	SW/NA	0/NA	SW/NA
IPU	0/NA	SW/NA	SW/NA	0/NA	SW/NA	SW/NA	SW/NA	SW/NA	SW/NA	0/NA	SW/NA
L3_INSTR	NA/NA	NA/NA	NA/NA	0/0	NA/NA	NA/NA	NA/NA	NA/NA	SW/NA	NA/NA	NA/NA
L3_MAIN1	0/NA	0/NA	0/NA	0/NA	0/NA	0/NA	0/NA	0/NA	0/NA	0/NA	0/1
L3_MAIN2	0/0	0/NA	0/2	0/NA	0/1	0/2	0/NA	0/1	0/3	0/NA	0/NA
DSP	0/NA	NA/NA	0/NA	0/NA	0/NA	SW/2	SW/NA	SW/NA	0/NA	0/NA	SW/NA
DSS	0/NA	0/NA	NA/NA	0/NA	0/NA	SW/NA	0/NA	0/NA	0/NA	0/NA	0/NA
EMU	0/NA	0/NA	0/NA	NA/NA	0/NA	0/NA	0/NA	0/NA	0/NA	0/0	0/NA
GPU	0/NA	0/NA	0/NA	0/NA	NA/NA	SW/NA	0/NA	0/NA	0/NA	0/NA	0/NA
IVA	0/NA	0/NA	0/NA	0/NA	0/NA	NA/NA	0/NA	0/NA	0/NA	0/NA	0/NA
L3_INIT	0/NA	0/NA	0/NA	0/NA	0/NA	SW/NA	NA/NA	SW/NA	SW/NA	0/NA	SW/NA

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Table 3-16. Device Domain Dependencies (Table 2) (continued)

Static/dynamic dependencies from below domains to right-side domains	CAM	DSP	DSS	EMU	GPU	IVA	L3_INIT	L4_PER	L4_SEC	MPU	WKUPAON
L4_PER	NA/NA	NA/NA	0/1	NA/NA	NA/NA	NA/NA	0/2	NA/NA	0/4	NA/NA	NA/NA
L4_SEC	0/NA	0/NA	0/NA	0/NA	0/NA	0/NA	0/NA	SW/NA	NA/NA	0/NA	0/NA
MPU	0/NA	SW/NA	SW/NA	0/NA	SW/NA	SW/NA	SW/NA	SW/NA	SW/NA	NA/NA	SW/NA

When a static dependency is hardware-coded between two domains directly linked by one or several interconnect interfaces, then the corresponding dynamic dependency is useless.

Emulation domain (DAP initiator) has no static dependency with any other domain. It has, however, a dynamic dependency with the L3_MAIN2 interconnect. A domain that can access an emulation domain does not have static or dynamic dependency with it.

Domain dependencies are chosen such that any access (even from EMU/DAP) towards a nondisabled target is always completed normally. Using static dependencies allows having minimal access latencies by keeping necessary domains on whenever the initiator is not standby. This may be at the expense of additional power consumption because some domains may stay on while not in use for a long time. By disabling static dependencies, applicative access is still completed normally by waking up, if applicable, the necessary domain on the path from the initiator to the target. Power consumption can be optimized at the expense of additional access latencies.

NOTE: It is required to put destination domain into forced wakeup (CLKTRCTRL = SW_WKUP) before changing a configurable static dependency.

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3.1.1.1.7.1 Static Dependency

If clock domain A has a master module that can access a slave module in clock domain B, then clock domain A can have a static dependency with clock domain B. Similarly, a static dependency can also exist between domain A and B if domain B conveys the transactions from a domain A module toward a module in any other domain. For example, CD_DSP can have a static dependency with CD_L3_MAIN1 because this domain has a level 3 (L3) interconnect to carry the transactions from the digital signal processor (DSP) module.

This static dependency consists of forcing clock domain B to stay active as long as there is at least one master module of clock domain A that is not in STANDBY state. If clock domains A and B are initially in GATED state, then clock domain B becomes active as soon as clock domain A becomes active when a wake-up request from the master module is received by the PRCM module.

Similarly, as a result of the static dependency, clock domain B can be gated only if all the master modules of clock domain A that can access the slave modules in clock domain B are in STANDBY state.

The static dependency between a source clock domain and a destination clock domain is configured in the PRCM module by setting the CM_<Source Clock domain>_STATICDEP[x] <Destination Clock domain>_STATDEP bit. As a result, the source clock domain forces the destination clock domain to become active and stay active as long as the source clock domain is active.

The destination domain must be put into forced wake-up (CM_<X>_CLKSTCTRL[1:0] CLKTRCTRL = SW_WKUP) before changing a configurable static dependency.

3.1.1.1.7.2 Dynamic Dependency

When clock domains A and B contain modules directly linked to a common device interconnect, these clock domains can have a dynamic dependency.

A dynamic dependency consists of forcing clock domain B to stay active as long as a module from clock domain A is communicating with the module in clock domain B through the interconnect. Clock domain B becomes active as soon as the communication is initiated. This is automatically managed by the PRCM module by monitoring the communication on the interconnect between the modules of the two clock domains.

Similarly, the inverse condition of this dependency can be stated: Clock domain B can be inactive only if all modules between clock domains A and B are quiet for a given sampling delay, identified as a sliding window duration on the interconnect activity status.

The size of the sliding window is based on the number of cycles of a prescaled level 4 (L4) clock whose frequency is configured by setting the CM_DYN_DEP_PRESCAL[5:0] PRESCAL bit field. The prescaled clock frequency is given as:

Prescaled clock frequency = L4 interface clock frequency / (PRESCAL + 1)

The size of the sliding window is fixed by setting the CM_<Clock domain>_DYNAMICDEP[27:24] WINDOWSIZE bit field. It is given as:

Sliding window duration = WINDOWSIZE × Period of Prescaled clock cycle

Figure 3-7 is an example of the sliding window duration equal to eight clock cycles of an L4 clock when PRESCAL is set to 3 and WINDOWSIZE is set to 2.

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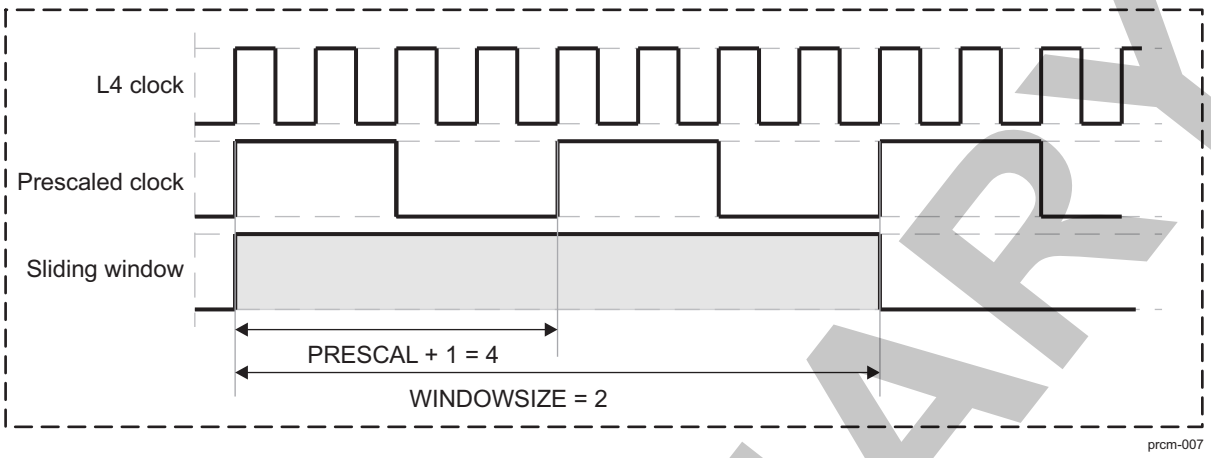
Figure 3-7. Sliding Window for Dynamic Dependency



This dynamic dependency is also referred to as the autosleep/autowakeup feature.

NOTE:

- The static dependency between two clock domains can be configured by software (PRCM module registers) or hardwired in the PRCM module.
- The dynamic dependency between two clock domains is hardwired in the PRCM module.

A dynamic dependency is said to be active when both of the following conditions are met:

- At least one master module or a slave interconnect module from clock domain A to domain B is active (that is, the master module is not in STANDBY state and/or the interconnect slave module is not in IDLE state)
- There has been one or more transaction on the interconnect within the sliding window duration.

Otherwise, a dynamic dependency is said to be inactive.

The dynamic dependency between a source clock domain and a destination clock domain can be read in the PRCM module from the corresponding read-only CM_<Source Clock domain>_DYNAMICDEP[x] <Destination Clock domain>_DYNDEP bit.

NOTE: It is recommended to use dynamic dependencies. They give better power results. Static dependencies should be rarely used (in some cases they can be used as they give shorter latency for a system initiator to access slave).

3.1.1.1.7.3 Wake-Up Dependency

A wake-up dependency is a dependency between the clock domain of a module that owns one or several wake-up signals toward the clock domain of another module needed to service the associated wake-up event. As a result of this dependency, the wake-up event to a module activates not only its clock domain but also the clock domain of the servicing module.

NOTE: To ensure that the clock domain of the servicing module remains active, the wake-up signal that triggers a wake-up dependency stays active as long as the source of the event is not serviced.

Wake-up dependencies allow acceleration of the wake-up transition of multiple domains needed to service the wake-up event by initiating their transition in parallel. The static and dynamic dependencies can allow the wake-up of related domains, but the complete wake-up transition of all the associated domains is slower because of the sequential cascading of their wake-up transitions.

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In the device, the source event of the wake-up signal to a slave module can be either of following types:

- Interrupt request to the microprocessor unit (MPU), DSP, or image processor unit (IPU) interrupt controller (INTC)
- DMA request to a DMA controller

Upon wake-up by these types of wake-up events, and for as long as they remain asserted, the PRCM module takes the following actions:

- The power domain of the servicing module (for example, MPU, DSP, IPU, or DMA) is forced to POWER ON state and the clock domain becomes active.
- The power domain of the device interconnect between the servicing module and the module originator of the wake-up event is forced to POWER ON state and the clock domain becomes active.
- The power domain of the slave module originator of the wake-up event is forced to POWER ON state and the clock domain becomes active.
- The slave module originator of the wake-up event is switched from IDLE to ACTIVE state.

On assertion of a wake-up event of a stand-alone master module, and as long as it remains asserted, the PRCM module takes the following action:

- The power domain of the master module originator of the wake-up event is forced to POWER ON state and the clock domain becomes active.

NOTE: For slave modules, the static and dynamic dependencies of a clock domain are not affected by its wake-up dependency settings. For master modules, the static dependencies are not affected.

Hence, in addition to the activation of the clock domains previously described, all clock domains associated by static dependencies are also activated.

However, the clock domains associated with the wake-up clock domain through dynamic dependencies are activated only if a transaction is initiated to these clock domains.

For each wake-up signal coming from a slave module, the type of the corresponding event can be configured in the PM_<Power domain>_<Originator Module> _WKDEP[x] WKUPDEP_<Originator Module>_<Servicing Module> bit of the PRCM module, where <Power domain> is the name of the power domain of the originator module of the wake-up event identified as <Originator Module>. Servicing Module refers to the module servicing the wake-up event.

NOTE: When only one event type is associated with the wake-up signal of a slave module, the wake-up dependency (WKUPDEP) for the module clock domain is not configurable and may be hardwired in the PRCM module.

For the master modules, there is no configurable wake-up dependency. Their power domain is switched on and their clock domain is activated by the PRCM module when they assert their wake-up signal.

3.1.1.2 Power Management

The PRCM module manages the switching on and off of the power supply to the device modules. To minimize device power consumption, the power to the modules can be switched off when they are not in use. Independent power control of sections of the device lets the PRCM module turn on and off specific sections of the device without affecting other sections.

3.1.1.2.1 Power Domain

A power domain is a section (that is, a group of modules) of the device with an independent and dedicated power manager (see Figure 3-8). A power domain can be turned on and off without affecting other parts of the device.

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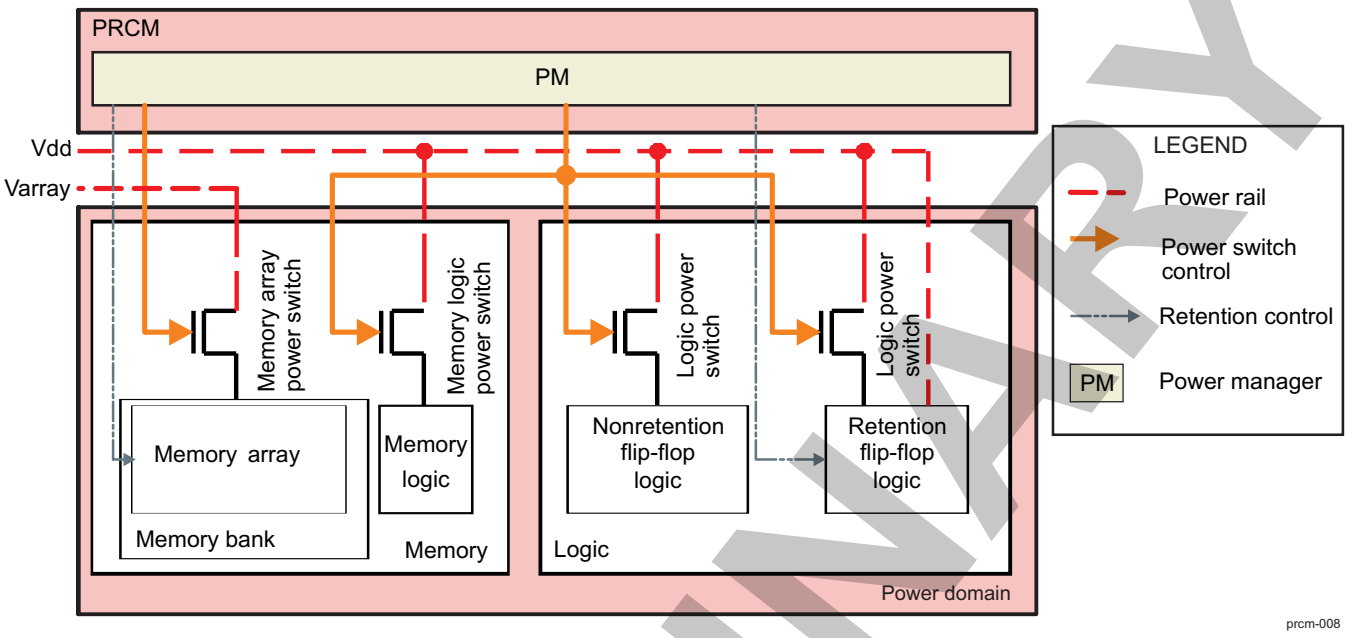
Figure 3-8. Generic Power Domain



To minimize device power consumption, the modules are grouped into power domains. A power domain can be split into logic and memory areas.

The memory area contains two entities:

- Memory bank: Composed of memory arrays. It is powered by a dedicated voltage rail and an associated power switch (for example, Varray and memory array power switches).
- Memory logic: Powered by the same voltage source as the logic area of the power domain, but has its dedicated power switch (for example, Vdd and memory logic power switches)

The logic area in the power domain can also be split between retention flip-flops (RFFs) and nonretention flip-flops (DFFs).

Table 3-17 lists the possible states and substates of the logic area in a power domain.

Table 3-17. States of a Logic Area in a Power Domain

State	Substate	Description
ON	ON-ACTIVE	Logic is fully powered and at least one enclosed clock domain is active.
	ON-INACTIVE	Logic is fully powered and all enclosed clock domains are idled.
RETENTION	CSWR (close switch retention)	Logic is fully powered and all enclosed clock domains are idled.

The RETENTION state is useful for quickly switching to low-power idle mode (in which the domain clocks are gated and the domain voltage is less than the on-voltage level) without losing the context, and then quickly switching back to ON-ACTIVE state when necessary. In RETENTION state, power consumption is less than in ON power state.

Similarly, in RETENTION state the CSWR state has faster turn-on times and higher leakage currents.

The behavior of the memory array power switch and memory logic power switch can be selected through software settings in the PRCM module or can be hardwired. Once the behavior is selected, the PRCM module hardware automatically handles these elements to ensure correct power transition sequencing between the power domain states.

Software can also initiate power state changes of the memory array when the associated power domain is in ON power state. This allows the memory array to be turned off and on as needed.

The memory area can be configured to any of the power states listed in Table 3-18.

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Table 3-18. States of a Memory Area in a Power Domain

State	Description
ON	The memory array is powered and fully functional.
RETENTION	The memory array is fully powered, but memory is not accessible. The array can be put into retention through an applicable direct retention control signal. Data in memory are always retained.

3.1.1.2.2 Module Logic and Memory Context

In case of a power state transition in the logic or memory areas, the context of the module may no longer be valid. This can also be the case when the domain resets are asserted by the device. A specific RM_<Clock Domain Name>_<Module Name>_CONTEXT register provides the status of the device logic and memory context.

- The module logic context consists of simple flip-flops (DFFs) if the module has no logic RFFs.
- If the module has logic retention (full or partial), it is assumed that the context consists only of RFFs.

NOTE: The display subsystem is an exception where the status of DFF and RFF context is given, because only HMDI keys are retained, while most of the display subsystem is not retained.

These context status bits must be cleared by software.

3.1.1.2.3 Power Domain Management

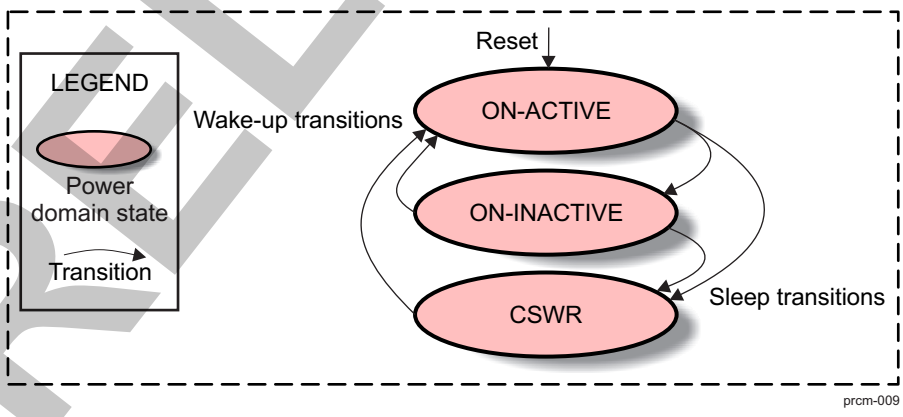
The power manager associated with each power domain is assigned the task of managing the domain power transitions. It ensures that all hardware conditions are satisfied before it can initiate a power domain transition from a source to a target power state (for example, from ON-ACTIVE state to CSWR RETENTION state).

The hardware condition for power domain transition from ON-ACTIVE to any other transition state is:

- All clock domain managers in the power domain are in ON-INACTIVE state: All modules in the domain are in IDLE or STANDBY state, and there is no constraining dependency (static, dynamic, or wake-up dependency) between the clock domains blocking the clock domain sleep transition.

Figure 3-9 shows all possible power domain state transitions.

Figure 3-9. Power Domain Transitions



Successive power-down transitions can be performed by lowering the power state from ON-ACTIVE to ON-INACTIVE, and then to RETENTION, as long as the hardware condition is satisfied.

However, the power domain wake-up transition from any low-power state (ON-INACTIVE or CSWR) to ON-ACTIVE state is always direct. For example, user software cannot request a power domain transition from the ON-INACTIVE state to the CSWR state, but only to the ON-ACTIVE state.

The power domain manager initiates a power domain wake-up transition when the conditions listed in Table 3-19 are satisfied.

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Table 3-19. Power Domain Wake-Up Conditions

Relation		Condition
AND		Voltage domain is on.
	OR	There is at least a wake-up condition for one enclosed functional clock domain.
		There is a request for clock generation or distribution enclosed in the power domain.
		There is a PRCM module service request (applicable only to power domains, including PRCM module logic).

The power domain manager initiates a domain sleep transition when the conditions listed in Table 3-20 are satisfied.

Table 3-20. Power Domain Sleep Conditions

Relation	Condition
AND	All functional clock domains enclosed in the power domain are idled.
	All clock generation or distribution enclosed in the power domain is quiet, and corresponding input clocks are gated. For example, DPLL, if present, must be in stop mode.
	There is no PRCM module service request (applicable only to power domains, including PRCM module logic).

Table 3-21 lists the control and status features of the PRCM module power domain.

Table 3-21. Power Domain Control and Status Registers

Register/Bit Field	Type	Description
PM_<Power domain>_PWRSTCTRL[1:0] POWERSTATE	Control	Selects the target power state of the power domain among ON-ACTIVE, ON-INACTIVE, and RETENTION
PM_<Power domain>_PWRSTCTRL[x] LOWPOWERSTATECHANGE	Control	Power state change request when domain has already performed a sleep transition. Allows going into deeper low-power state without waking up the power domain.
PM_<Power domain>_PWRSTCTRL[2] LOGICRETSTATE	Control	Selects whether the power domain logic is in CSWR RETENTION state when the domain transitions to RETENTION state
PM_<Power domain>_PWRSTCTRL[x] <memory bank>_RETSTATE	Control	Selects whether the memory bank in the power domain is in ON or RETENTION state when the power domain is in RETENTION state. The memory bank cannot be in ON state when the power domain is in RETENTION state.
PM_<Power domain>_PWRSTCTRL[x] <memory bank>_ONSTATE	Control	Selects whether the memory bank is in the ON or the RETENTION state when the power domain is in the ON state
PM_<Power domain>_PWRSTST[1:0] POWERSTATEST	Status	Identifies the current state of the power domain. It can be RETENTION, ON-INACTIVE, or ON-ACTIVE.
PM_<Power domain>_PWRSTST[2] LOGICSTATEST	Status	Identifies the current state of the logic area in the power domain.
PM_<Power domain>_PWRSTST[20] INTRANSITION	Status	Identifies whether a power state transition in the power domain is in progress or there is no ongoing transition
PM_<Power domain>_PWRSTST[x] <memory bank>_STATEST	Status	Identifies the current power state of the memory bank in the power domain. It can be RETENTION or ON.
PM_<Power domain>_PWRSTST[25:24] LASTPOWERSTATEENTERED	Status	Identifies the last (previous) power state of the power domain. It can be RETENTION, ON-INACTIVE, or ON-ACTIVE.

3.1.1.3 Voltage Management

The PRCM module controls the voltage scaling (that is, switching the voltage in discrete steps or in a continuum within a range of possible values) of the power sources of the device. This allows control of the power consumption of the device according to the defined performance criteria. Higher performance is ensured with higher voltage and clock frequencies (and hence higher power consumption), while lower performance can be supported with lowered power consumption by reducing or completely gating the power supply to specific areas of the device and gating the associated clocks.

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3.1.1.3.1 Voltage Domain

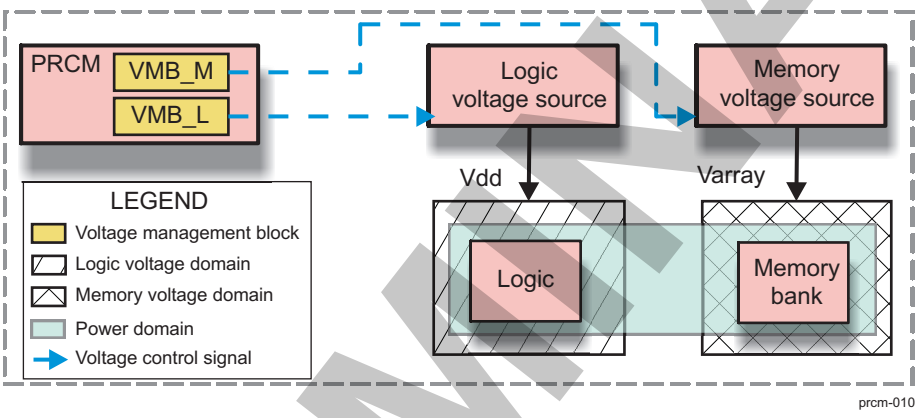
A voltage domain is a section of the device supplied by a dedicated voltage source (that is, an internal LDO or external switch mode power supply [SMPS]). A voltage domain may or may not be controlled by the PRCM module. When a voltage domain is controlled by the PRCM module, a dedicated voltage manager is associated. The voltage manager allows regulation of the voltage level of the source for the voltage domain independently of other voltage domains of the device.

The voltage managers in the PRCM module can be of two types:

- Dynamically configurable by software to scale the domain voltage level to specific values within the operational voltage range of the device. This is called adaptive voltage scaling (AVS).
- Hardware-controlled to automatically switch the domain voltage levels according to the associated hardware conditions.

Figure 3-10 shows a voltage domain.

Figure 3-10. Generic Voltage Domain



By partitioning the device into independent voltage domains, different operating voltages can be assigned to the different sections of the device (that is, a group of modules or memory banks). The independent voltage control allows voltage scaling of device subsections to ensure that each module or memory bank operates at the optimized operating voltage level based on the application performance requirements. When all modules within a voltage domain are idle (that is, have no ongoing transaction), the domain voltage can be lowered to reduce power consumption and then switched back to normal operating voltage level when a wake-up event is received by one of the modules of the voltage domain. Similarly, when a memory bank is not in use, it can be switched to retentionvoltage levels to ensure power savings.

Table 3-22 describes the different states of the logic voltage domain.

Table 3-22. States of Logic Voltage Domain

State	Description
ON	The voltage regulator source for the voltage domain is active and operating in its normal voltage range for the current operating performance point (OPP) and can deliver up to the maximum load current defined for the current OPP.
SLEEP	The voltage regulator source is operating in its normal voltage range, but it can deliver only a limited load current (no logic activity on this voltage domain). In sleep mode, regulator power consumption is reduced.
RETENTION	The voltage regulator source is operating at retention voltage level. It delivers the minimal load current required to maintain the voltage domain logic context.

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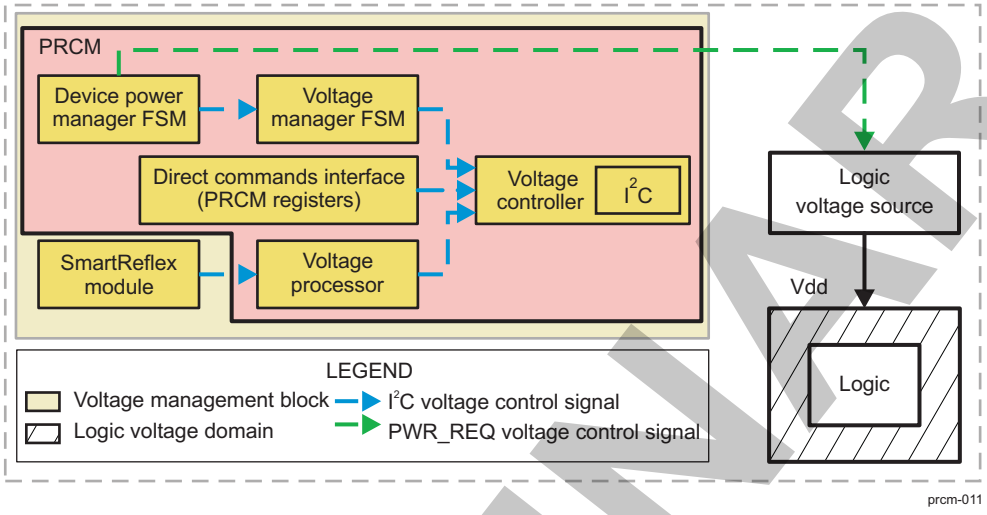
3.1.1.3.2 Voltage Domain Management

Figure 3-11 shows the different voltage control paths available within a generic logic voltage management block to control the voltage supply to the logic voltage domains of the device.

Figure 3-11. Generic Logic Voltage Management



3.1.1.3.2.1 Logic Voltage PWR_REQ Voltage Control

A PWR_REQ signal is deasserted when the device needs to change its current power state to other. The external power integrated circuit (IC) can be used to properly manage turn-off or turn-on of the logic voltage source.

3.1.1.3.2.2 Logic Voltage I^2C Voltage Control

The PRCM module allows three voltage control paths to a dedicated inter-integrated circuit (I^2C™) interface for the logic voltage domains it manages:

1. The hardware-managed voltage of the PRCM module changes from device power manager voltage finite state-machine (FSM) through a voltage manager FSM based on hardware conditions. It sends the voltage commands when the device enters the RETENTION state and upon device wakeup.
2. Direct control by user software through the PRCM module registers for voltage scaling
3. AVS (see Section 3.1.1.3.3, *AVS Overview*) with SmartReflex™ voltage control commands through the voltage processor

NOTE: An I^2C host module (not controlled by the PRCM module) can be used to program the external power IC. Because this procedure completely bypasses the PRCM module, see Section 23.1, *I^2C*.

Figure 3-12 shows the voltage control path available within a generic memory voltage management block to control the voltage supply to the memory voltage domains of the device.

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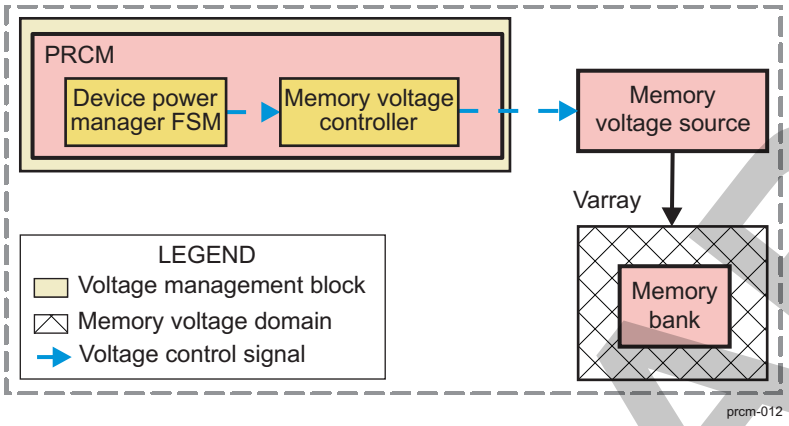
Figure 3-12. Generic Memory Voltage Management



The PRCM hardware supports automatic scaling down of the memory array supply whenever the memory domains transition to the RETENTION power state. The device power manager FSM manages the voltage scaling of memory voltage domains through the memory voltage controller (or LDO).

3.1.1.3.3 AVS Overview

SmartReflex is a power-management technique used to control the operating voltage of a device to reduce its active power consumption.

With SmartReflex, the power supply voltage is adapted to the silicon performance in two ways:

- Statically adapted to the manufacturing process of a given device
- Dynamically adapted to the temperature-induced current performance of the device

SmartReflex achieves optimal performance/power trade-off for all devices across the technology process spectrum and across temperature variations.

The static correction of the device voltage level (see Figure 3-13) is based on the desired performance level and silicon performance characteristics of the device. As a result of process dispersion, each die has its specific silicon performance. The range of the process distribution defines the weak devices (low-performance silicon) and the strong devices (high-performance silicon).

A weak device is a device with the lowest performance tolerated for a process distribution; that is, at the typical voltage, the inherent maximum frequency is the lowest frequency of the chip distribution. Considered as the worst case, weak devices are used to constrain the target frequency of all the chips (OPP definition).

A strong device is a device with the highest performance tolerated for a process distribution. The inherent maximum frequency at the typical voltage is greater than the targeted frequency.

Figure 3-13 shows that with the SmartReflex voltage-control architecture, it is possible to compensate for the device silicon characteristics and obtain optimal performance characteristics. Based on the device characteristics, the device voltage level can be adjusted for specific performance level.

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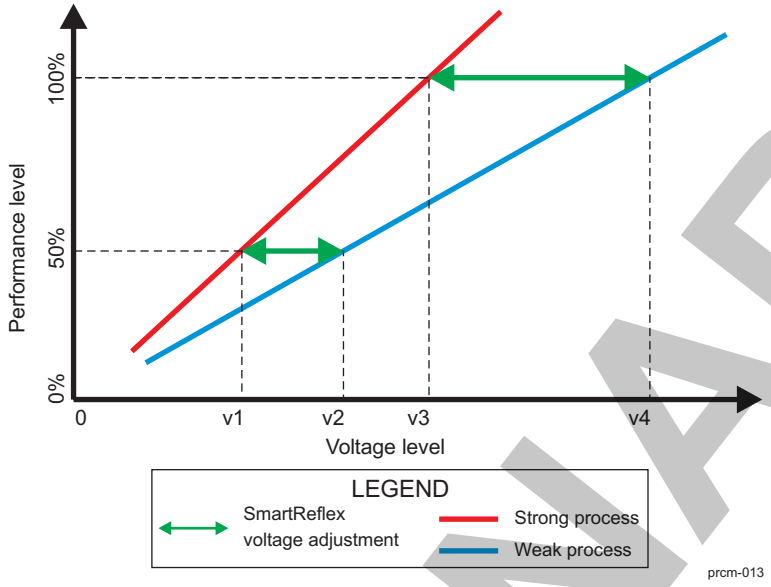
Figure 3-13. SmartReflex Static Voltage Adjustment

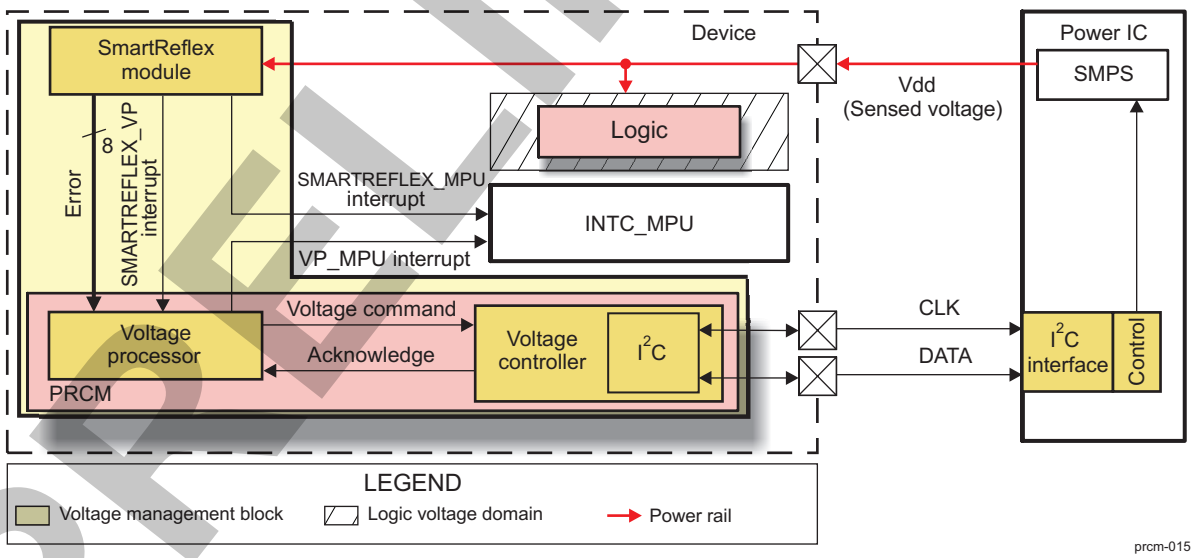


The dynamic correction of the device voltage is based on the real-time comparison of predefined performance points to the on-chip measured performance level. The device voltage level is raised or lowered to compensate for temperature-induced performance variations.

Without SmartReflex, the voltage variation is near the nominal voltage level and is not controlled through any active dynamic compensation. This leads to power waste.

Figure 3-14 is a functional overview of the SmartReflex voltage-control architecture of the device connected to an external power IC.

Figure 3-14. SmartReflex Voltage Control Functional Overview



SmartReflex voltage control consists of the following modules:

- SmartReflex
- INTC_MPU
- Voltage processor
- Voltage controller
- I^2C interface

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- SMPS

The SmartReflex module senses input voltage (Vdd) and generates an error value that identifies the difference between the desired optimal voltage and the actual value of the SMPS. This error value is set in an internal register (for software read, if necessary) and is also passed to the voltage processor.

The voltage processor converts the error value to a voltage command that defines the change in the output voltage of the SMPS required to bring it to the desired voltage level.

The voltage command is sent to the voltage controller, which passes it to the power IC through the dedicated I^2C interface. The power IC then adjusts the output voltage of the SMPS according to the command.

In this way, the SmartReflex module dynamically adjusts the SMPS voltage to compensate for voltage variations.

The device supports Class 1.5 for SmartReflex voltage control or software-controlled hardware calibration mechanism.

3.1.1.3.3.1 Class 1.5 SmartReflex Voltage Control

SmartReflex Class 1.5 is a software controlled hardware calibration mechanism designed to improve DVFS latencies and system performance. When SmartReflex modules are used in class 1.5, the Voltage Processors should be disabled. Here the calibration is only at boot time.

In SmartReflex Class 1.5, the calibration procedure is triggered by the user software (for example once per day or week) to account for device aging. Additional temperature margins are fused, thus no user software is involved.

3.1.2 Power-Management Techniques

The following sections describe the power-management techniques supported by the device.

NOTE: The values in Figure 3-15 through Figure 3-17, which show the power-management techniques, are hypothetical. They do not represent valid test results on the device.

3.1.2.1 Standby Leakage Management

Standby leakage management (SLM) is a power-management technique that reduces standby power consumption by reducing power leakage.

With SLM, the device switches into low-power system modes automatically or in response to user requests during system standby (that is, in situations when no application is started and system activity is negligible or limited).

When applying SLM, the system remains in the lowest static power mode compatible with the system response time requirement.

This technique trades static power consumption for wake-up latency.

3.1.2.2 Dynamic Voltage and Frequency Scaling

Dynamic voltage and frequency scaling (DVFS) consists of minimizing the idle time of the system. The DVFS technique uses dynamic selection of the optimal operating frequency and voltage to allow a task to be performed in the required length of time. This reduces the active power consumption (power consumed while executing a task) of the device while still meeting task requirements.

NOTE: The values in Figure 3-15 are hypothetical. They are meant only to clarify the concept and do not represent valid test results on the device.

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Figure 3-15. Comparison of Energy Consumed With/Without DVFS

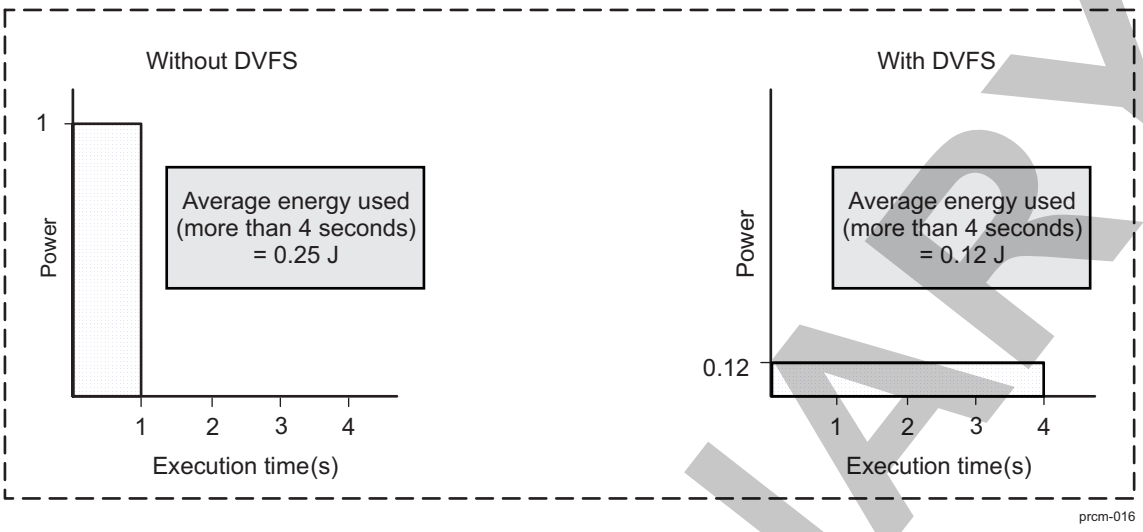

Figure 3-15 shows the DVFS technique by comparing a process executed at maximum frequency and operating voltage without applying DVFS to the same process executed at optimal frequency and voltage using DVFS, based on the task requirements. If a task that must terminate in 4 seconds is performed at maximum operating frequency (see the left side of the figure), it terminates in 1 second, and the remaining 3 seconds are spent in idle mode.

With DVFS (see the right side of the figure), the operating frequency is reduced to optimal level; the task takes the full 4 seconds to complete, but power consumption is reduced. In addition, the voltage can be reduced further to save power so the dynamic and leakage power consumption are reduced.

DVFS requires control over the clock frequency and the operating voltage of the device elements. By intelligently switching the individual elements of the device to their OPPs, the power consumption of the device for a given task can be minimized.

For practical reasons related to the development of the device (flow, tools), DVFS can be used only for a few discrete steps, not over a continuum of voltage and frequency values. Each step, or OPP, is composed of a voltage (V) and frequency (F) pair. For an OPP, the frequency corresponds to the maximum frequency allowed at a voltage, or reciprocally; the voltage corresponds to the minimum voltage allowed for a frequency.

When applying DVFS, a processor or system always runs at the lowest OPP that meets the performance requirement at a given time. The user determines the optimal OPP for a given task and then switches to that OPP to save power.

3.1.2.3 Dynamic Power Switching

Like DVFS, dynamic power switching (DPS) is a power-management technique intended to reduce the active power consumption of a device. However, whereas DVFS reduces dynamic and leakage power consumption, DPS reduces only leakage power consumption, at the expense of a slight overhead in dynamic power consumption.

With DPS, the system switches dynamically between high- and low-consumption system power modes during system active time. When DPS is applied, a processor or system runs at the highest OPP (maximum frequency and voltage) to complete its tasks quickly, followed by an automatic switch to a low-power mode for minimum power consumption. DPS is useful when a real-time application is waiting for an event. The system can switch into a low-power system mode if the wake-up latency conditions allow it.

This technique consists of maximizing the idle period of the system to reduce its power consumption.

NOTE: The values in Figure 3-16 are hypothetical. They are meant only to clarify the concept and do not represent valid test results on the device.

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Figure 3-16. Comparison of Energy Consumed With/Without DPS

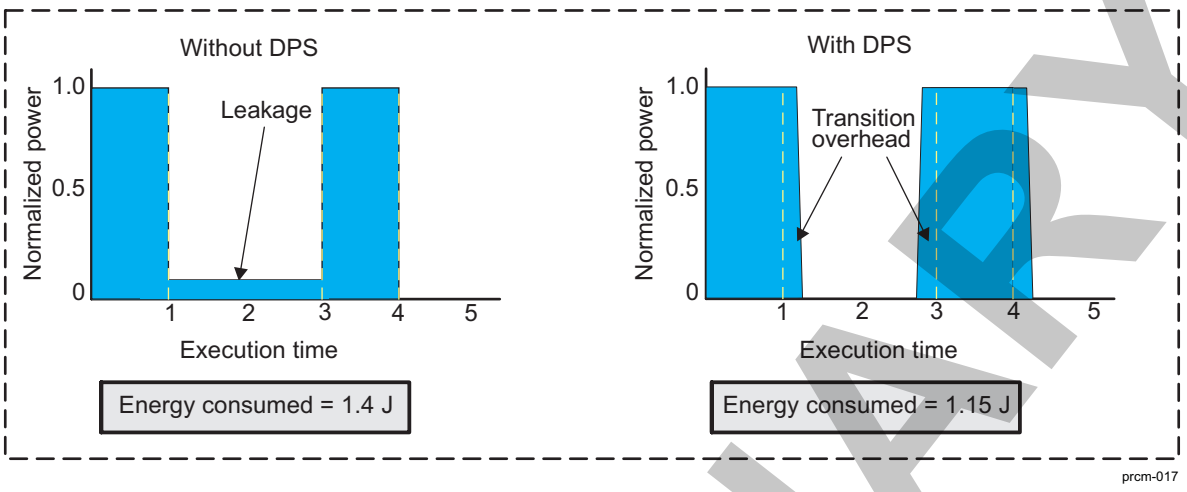

Figure 3-16 compares the behavior of power consumption for the same operation of the device without DPS (see the left side of the figure) and with DPS (see the right side of the figure). When operating without DPS, the device has a constant leakage current in idle mode. By using DPS, the system reduces the leakage current to 0. However, the transitions between system power modes may require storing the information before entering a low-power inactive state and restoring the information after a wake-up event (see Figure 3-16). This results in additional dynamic power consumption, referred to as transition overhead (see Figure 3-16). Transition overhead must be considered for a DPS operation.

For efficient deployment of DPS techniques, it is necessary to predict dynamically the performance requirement of the applications running on the processor. The DPS controller must account for the overhead of wake-up latencies related to domain switching and ensure that they do not significantly affect the performance of the device. Even with transition overhead, the user can identify an optimal idle-time limit, after which the DPS is useful for dynamic power saving.

3.1.2.4 Adaptive Voltage Scaling

SmartReflex-based AVS is a power-management technique for automatic control of the operating voltages of the device to reduce active power consumption.

With SmartReflex, power-supply voltage is adapted to silicon performance, either statically (based on performance points predefined in the manufacturing process of a given device) or dynamically (based on the temperature-induced real-time performance of the device). A comparison of these predefined performance points to the real-time on-chip measured performance determines whether to raise or lower the power supply voltage.

AVS achieves the optimal performance/power trade-off for all devices across the technology process spectrum and across temperature variation. The device voltage is automatically adapted to maintain performance of the device. This ensures optimal power consumption for a given OPP.

With AVS, the frequency steps are identified and the voltage is adapted according to the silicon performance of the device. In this case, instead of a voltage step for each frequency step, there is a corresponding range of voltages. The range depends on the fabrication process of the device and its real-time operating state (temperature) at a given frequency.

3.1.2.5 Adaptive Body Bias

The device implements transistor body bias techniques for forward body bias (FBB) to boost the operating clock frequency for operation at higher OPPs.

Adaptive body bias (ABB) is based on the process corner and the current OPP. This is configured in the EFUSE_CTRL_CUST bit field at the device characterization and is not continuously updated. A dedicated LDO (VBBLDO) is used to produce the voltage bias.

ABB is supported only for MPU and MM domains.

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3.1.2.6 SR3-APG (Automatic Power Gating)

In addition to power-management techniques supported in the device, the MPU subsystem also employs SR3-APG power-management technology to reduce leakage. This technology allows for full logic and memory retention on MPU_C0 and MPU_C1 when required conditions are satisfied. It is controlled by the PRCM_MPU. For more information, see Chapter 4, *Dual Cortex-A15 MPU Subsystem*.

3.1.2.7 Combining Power-Management Techniques

The power-management techniques previously described have specific features and are most effective when used under the specific operating conditions of the device. Hence, the best active power savings are obtained by combining the DVFS, DPS, SLM, and AVS techniques. For a given operating state, one or more of the power-saving techniques can be applied to ensure optimal operation with maximum power saving.

AVS can be used at boot time to adapt the voltage to the process characteristics (strong/weak) of the device and then be used continuously to compensate temperature variations. AVS can also ensure the maximum available application performance of the device at a given OPP.

When medium application performance is required, or when application performance requirements vary, DVFS can be applied. The voltage and frequency can be scaled to match the closest OPP that meets the performance requirement.

When application performance requirements fall between two OPPs, or when a low application performance is required that is below the lowest performance OPP, DPS can be applied to switch to low-power mode.

When combining DVFS and DPS, the operating frequency must not be scaled to match the performance requirement without scaling the voltage. Lower operating frequency increases task completion time and reduces idle time. This prevents DPS or reduces its efficiency (DPS becomes more effective as idle time increases). Unless DPS cannot be applied for other reasons, for a given operating point of DVFS the operating frequency must always be set to the maximum allowed at a given voltage. This ensures optimal process completion time and application of DPS.

If DPS cannot be applied in a given context, scaling the frequency while keeping the voltage constant does not save energy; it does, however, reduce peak power consumption. This can have a positive effect on temperature dissipation and battery life.

SLM must be used when no applications are running and performance requirement drops to 0.

NOTE: The OPPs shown in Figure 3-17 are only for indication and clarity of text. They do not correspond to validated OPPs of the device.

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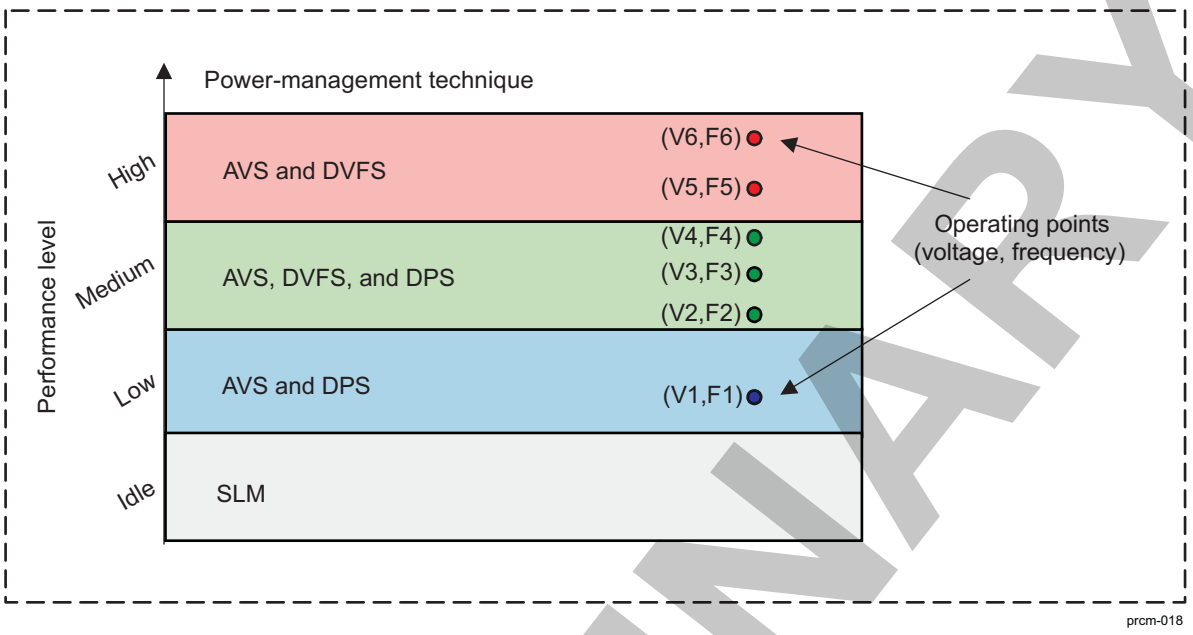
Figure 3-17. Performance Level and Applied Power-Management Techniques



3.1.2.7.1 DPS Versus SLM

DPS and SLM are similar concepts: they consist of switching the system between high- and low-power consumption modes. However, their operating timescales differ, principally in the latency allowed for mode transitions.

DPS is generally used in an applicative context (tasks are started). Therefore, mode transitions are related to system performance requirements or the processor load. DPS transition latencies must be small (typically between 10 µs and 100 µs) compared to the time constraints or deadlines of the application so that they do not degrade application performance. DPS requires performance prediction to ensure that transition latencies do not deteriorate device performance to the point that real-time application deadlines are missed or the user experience degrades too much for an interactive application.

SLM is not used in an applicative context (no task started). Mode transitions are related more to system responsiveness, and the transition latencies must be small compared to user sensitivity so that they do not degrade the user experience. For SLM, transition latencies are typically 1–10 ms or more.

DPS and SLM also differ in the type of wake-up event used to exit low-power idle mode. For DPS, wake-up events are application-related (timer, DMA request, peripheral interrupt, etc.); for SLM, wake-up events are user-related (touch screen, key pressed, peripheral connections, etc.).

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3.2 PRCM Subsystem Overview

3.2.1 Introduction

The power-management framework of the device significantly reduces dynamic power consumption and static leakage current to extend the life of the battery in the end product. This framework incorporates support for state-of-the-art power-management techniques. It ensures optimal device operation with significantly reduced power consumption. The power-management framework (PMFW) of the device is split over the following modules:

- SCRM: Handles system-level (with one or more devices) clock and reset distribution and management
- PRCM: A logical module composed of the following three physical submodules:
  - PRM: Handles device-level power and reset management. It also handles some clocks in the device. This module always remains on, unless no power is supplied to the device pads.
  - CM_CORE_AON: Handles device-level clock management of the MPU, DSP, and ABE power domains. This module always remains on, unless no power is supplied to the device pads.
  - CM_CORE: Handles device-level clock management of the IVA, CORE, COREAON, display subsystem (DSS), CAM, GPU, L3INIT, and L4_PER domains. This module does not always remain on. It is switched to full retention mode when its power domain (PD_CORE) is in RETENTION state. It is off when no power is supplied to the device pads.
- SMARTREFLEX_MPU, SMARTREFLEX_MM, and SMARTREFLEX_CORE (SmartReflex): Handle AVS features

Together, these modules provide enhanced power-management features with centralized control for the clock, reset, and power-management signals in the device.

The device supports the power-management techniques with the following features:

- Partitioning of the device into voltage, power, clock, and reset domains
- Domain isolation that allows any combination of domain ON/OFF states
- Clock tree with selective clock-gating conditions
- Hardware-controlled reset sequencing management
- Power, reset, and clock control hardware mechanism to manage sleep and wake-up dependencies of the power domains
- Support for hardware-controlled autogating of module clocks
- Memory retention capability for preserving memory contents in low-power sleep mode
- DVFS support for the processor and peripherals
- AVS support for the processor and peripherals, for real-time performance adjustments
- Support for I/O pad configuration in low-power device mode for minimum power consumption when in a low-power power state

The PMFW interfaces with all the components of the device for power, clock, and reset management through associated control signals. It integrates enhanced features to let the device adapt energy consumption dynamically according to changing application and performance requirements. The innovative hardware architecture allows a substantial reduction in leakage current.

The power-management modules are fully configurable through their L4 interface ports.

Figure 3-18 is an overview of the power-management modules and their internal connections with a generic power domain.

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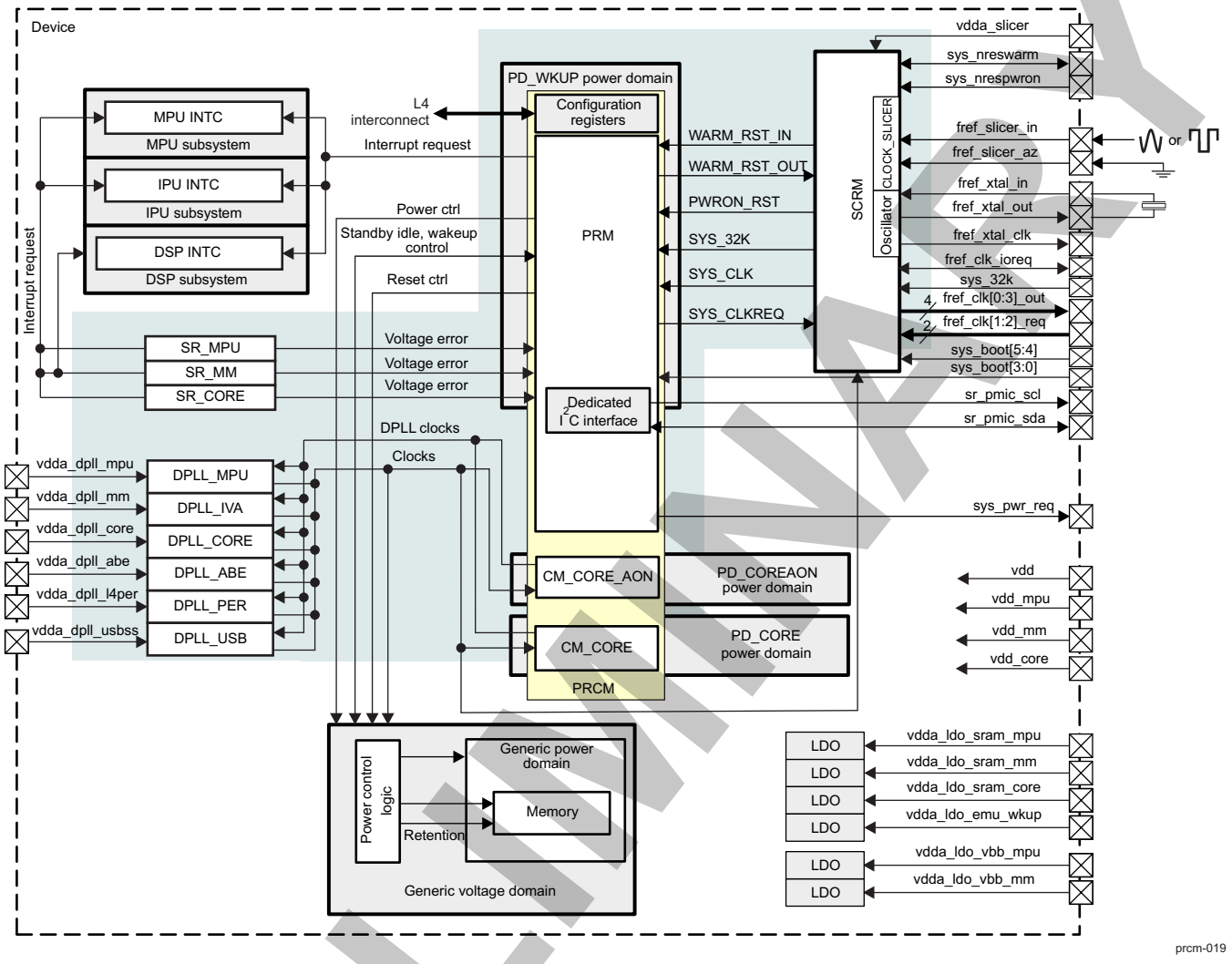
Figure 3-18. PMFW Overview



NOTE: The device I/O logic maps the module signals to the different pads of the device. For more information, see the *Common Pad Configuration Controls* and *I/O Cell Specific Pad Group Controls* sections in Section 18.4.8, *Control Module*.

3.2.2 Power-Management Framework Features

The power-management modules:

- Manage independent power domains
- Control scalable logic voltage domains and selectable voltage modes for memory voltage domains
- Handle standby, idle, and wake-up procedures for the modules of the device
- Allow software and partial hardware control
- Monitor and handle wake-up events
- Control system clock and reset input sources
- Manage and distribute clocks and resets with high control granularity
- Handle power-up sequences
- Have debug and emulation features
- Allow adaptive and dynamic voltage scaling with dedicated high-speed (HS) master I^2C interface

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- Control RFFs of device modules to support DPS

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3.3 PRCM Subsystem Environment

The modules of the PMFW receive the external reset, clock, and power signals. See Figure 3-18.

NOTE: In the remainder of this chapter, power IC refers to a peripheral power source IC that is interfaced with the device. It receives power control commands (voltage scaling and power switching) from the device and provides the necessary voltages and reset signals.

The following sections describe the interfaces for external clock, reset, and power sources.

3.3.1 External Clock Signals

The SCRM module receives a low-frequency clock input, sys_32k, at 32,768-Hz frequency, which will be referenced as a 32-kHz clock. The SCRM module can receive a high-frequency system clock through two possible inputs: fref_slicer_in or fref_xtal_in. The fref_slicer_in input supplies the input clock to an on-chip CLOCK_SLICER, while the fref_xtal_in input can be used as an external crystal connection for internal high-frequency clock generation through an on-chip oscillator.

The SCRM can output four auxiliary clocks, fref_clk[0:3]_out. Output clocks 1 and 2 can be gated or enabled through associated clock request signals, fref_clk[1:2]_req.

Table 3-23 lists the external clock pins, signal names, their direction, associated module, and description of the signals. If the signal is input to the device, the module is the destination module for the signal; if the signal is an output from the device, the module is the source module of the signal.

Table 3-23. External Clock Signals

Pin	Signal	I/O[1]	PMFW Module	Description	Module Reset Value
sys_32k	SYS_32K	I	SCRM	32-kHz clock input (sleep clock)	Z
fref_clk_ioreq	SYSCLK_REQ	I/O	SCRM	System clock request. Input when pins sysboot4 = 0 and sysboot5 = 0 (oscillator mode). Output when pins sysboot4 = 0 and sysboot5 = 1 (CLOCK_SLICER mode).	Z
fref_slicer_in	SLICER_IN	I	SCRM	System clock input to the CLOCK_SLICER. It can be sinusoidal or square input signal.	Z
fref_slicer_az	SLICER_AZ	I	SCRM	Connected to ground at package level	Z
fref_xtal_in	XTAL_IN	I	SCRM	Oscillator drive input from crystal	Z
fref_xtal_out	XTAL_OUT	O	SCRM	Oscillator drive output to crystal	NA
fref_xtal_clk	XTAL_CLK	O	SCRM	Oscillator buffered output	0
fref_clk[1:2]_req	CLK[1:2]_REQ	I	SCRM	Auxiliary clocks request	Z
fref_clk[0:3]_out	CLK[0:3]_OUT	O	SCRM	Auxiliary clocks outputs 0 to 3	For fref_clk0_out value is 0, for all rest value is Z

(1) I = Input; O = Output; I/O = Bidirectional

The signal on the oscillator buffered output (fref_xtal_clk) pin is a direct image of the signal on the fref_xtal_in input pin. The fref_xtal_clk pin provides the oscillator-generated clock to external devices. It is available when the oscillator is active or bypassed.

The XTAL_CLK clock signal is controlled by the CONTROL_CKOBUFFER register in the CTRL_MODULE_WKUP module. The CONTROL_CKOBUFFER register controls the following features of the oscillator output buffer:

- Output buffer enable signal - CONTROL.CONTROL_CKOBUFFER[31] CKOBUFFER_OUT_EN
- Selection of an alternate clock source for the input square signal - CONTROL.CONTROL_CKOBUFFER[30] CKOBUFFER_ALTSEL
- Polarity control for output clock signal - CONTROL.CONTROL_CKOBUFFER[29] CKOBUFFER_POLARITY
- Output clock enable control signal - CONTROL.CONTROL_CKOBUFFER[28] CKOBUFFER_CLK_EN

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NOTE: To enable the XTAL_CLK clock signal on the fref_xtal_clk pin, the CONTROL.CONTROL_CKOBUFFER[28] CKOBUFFER_CLK_EN bit must be set.

For information about the CONTROL_CKOBUFFER register, see Section 18.6, *Control Module Register Manual*, in Chapter 18, *Control Module*.

The auxiliary clocks are controlled by the configuration of the SCRM.AUXCLK <clock ID> (where the <clock ID> can be 0 to 4); for example, fref_clk1_out is controlled by the SCRM.AUXCLK1 register. It controls the following features:

- Select the clock-off output polarity
- Source clock input:
  - System clock
  - Clock from DPLL_CORE
  - Clock from DPLL_PER
- Initiate software-generated request
- Software-controlled clock gating
- Divide factor configuration between 1 and 16

NOTE: The SCRM provides a software control to enable and disable each output clock path. To allow the system clock (SYS_CLK) gating, all of the SCRM.AUXCLK<clock ID>[8] ENABLE bits must be cleared.

By default, the SCRM.AUXCLK<clock ID>[8] ENABLE bits are 0x0 after reset.

Software must clear the default reset value in the SCRM.AUXCLK4[8] ENABLE bit.

The bidirectional fref_clk_ioreq pad can be used to manage the external system clock request and auxiliary clock request 0. With this implementation, it is not expected to drive the system clock request externally when the SOC is the clock requester. This implementation requires programming the SCRM accordingly, in case the SOC needs the external system clock request. The programming consists in setting the AUXCLK0[9] DISABLECLK bit to 1 and the AUXCLKREQ0[4:2] MAPPING bit field to 0. Without these settings the SCRM wrongly interprets an external clock request as auxiliary clock request 0.

The SCRM must enable the output buffer of this bidirectional pad as long as it needs to request the external clock source, and the output buffer must be put in high-Z when it no longer needs the system clock source.

If device low-power mode is entered with fref_clk[1:2]_req active, then fref_clk[0:3]_out will be kept running from the system clock (SYS_CLK). LDO_WKUP stays in Active mode.
If fref_clk[1:2]_req is de-asserted while in low-power mode, then fref_clk[0:3]_out will be gated and LDO_WKUP will enter Sleep mode. SYS_CLK can be stopped.
If fref_clk[1:2]_req is re-asserted while in low-power mode, then fref_clk[0:3]_out will stay gated waiting for wake-up event that will trigger transition of LDO_WKUP to Active mode.

3.3.2 External Boot Signals

The PRM receives SYSBOOT[3:0] information from external pins sys_boot[3:0]. They are used to select interfaces or devices for the booting list. For more information, see Chapter 28, *Initialization*, Section 28.2.4.2, *Booting Device Order Selection*.

The SCRM receives SYSBOOT[5:4] information from external pins sys_boot[5:4]. They define the source clock configuration of the device. For more information, see Chapter 28, *Initialization*, Section 28.2.4.1, *Clock Source Selection*.

Table 3-24 lists the external boot pins, signal names, their direction, the associated modules, description, and reset values of the signals. If the signal is input to the device, the module is the destination module for the signal; if the signal is an output from the device, the module is the source module of the signal.

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Table 3-24. External Boot Signals

Pin	Signal	I/O [1]	PMWF Module	Description	Module Reset Value
sys_boot0	SYSBOOT0	I	PRM	System boot configuration pin 0: Latched at power-on reset (POR)	Z
sys_boot1	SYSBOOT1	I	PRM	System boot configuration pin 1: Latched at POR	Z
sys_boot2	SYSBOOT2	I	PRM	System boot configuration pin 2: Latched at POR	Z
sys_boot3	SYSBOOT3	I	PRM	System boot configuration pin 3: Latched at POR	Z
sys_boot4	SYSBOOT4	I	SCRM	System boot configuration pin 4: Latched at POR	Z
sys_boot5	SYSBOOT5	I	SCRM	System boot configuration pin 5: Latched at POR	Z

(1) I = Input; O = Output; I/O = bidirectional

3.3.3 External Reset Signals

The SCRM manages two reset signals:

- POR input on the sys_nrespwron pin
- Warm reset on the sys_nreswarm pin

sys_nrespwron is asserted at device power up to reset the full logic in the device.

sys_nreswarm is a bidirectional pin. It can be activated at any time by an external device or an external reset push button action to cause a global warm reset event. The SCRM then holds sys_nreswarm to be driven out and maintained for a limited length of time at the boundary of the device. In this way, the device and its related peripherals are reset together.

The sys_reswarm and sys_nrespwron signals are active low.

Table 3-25 lists the external reset pins, signal names, their direction, associated module, and description of the signals. If the signal is input to the device, the module is the destination module for the signal; if the signal is an output from the device, the module is the source module of the signal.

Table 3-25. External Reset Signals

Pin	Signal	I/O[1]	PMFW Module	Description	Module Reset Value
sys_nreswarm	SYS_WARM_RST	I/O	SCRM	Warm reset input and output	Z
sys_nrespwron	SYS_PWRON_RST_IN	I	SCRM	POR input	Z

(1) I = Input; O = Output; I/O = bidirectional

3.3.4 External Power Control Signals

The power control signals let the PMFW modules control the voltage levels of the device.

The voltage level of the scalable voltage sources in the external power IC can be scaled by sending commands to the power IC through a dedicated I^2C interface in the PRCM module. The clock and data pins for this I^2C interface are sr_pmic_scl and sr_pmic_sda, respectively.

The PRCM module can also command the external power IC to switch the device voltages to off level when the device is switched off, and reactivate them when it wakes up. This is managed through the signal on the sys_pwr_req pin.

Table 3-26 lists the pins, signal names, their direction, associated module, and description for the signals to the external power IC.

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Table 3-26. Power Control Interface

Pin	Signal	I/O[1]	PMFW Module	Description	Module Reset Value
sr_pmic_scl	SR_PMIC_SCL	I/O	PRM	The SmartReflex dedicated I^2C interface clock line	1
sr_pmic_sda	SR_PMIC_SDA	I/O	PRM	The SmartReflex dedicated I^2C interface data line	1
sys_pwr_req	PWR_REQ	O	PRM	Power request to the external power IC to switch on or change the device power state	1

(1) I = Input; O = Output; I/O = bidirectional

3.3.5 External Voltage Inputs

Table 3-27 lists the external voltage sources related to the PRCM module.

NOTE: Table 3-27 lists only the voltage sources that are directly managed by the PRCM module or received by parts of the PRCM module (for example, DPLLs, LDOs, etc.). It does not give the device voltage sources not directly associated with the PRCM module.

Table 3-27. Voltage Sources

Pin	Signal	Managed by the PRCM	Description
vdd	VDD_CORE_L	Yes (AVS and DVFS)	Supplies VDD_CORE_L logic voltage domain
vdd_mpu	VDD_MPU_L	Yes (AVS and DVFS)	Supplies VDD_MPU_L logic voltage domain
vdd_mm	VDD_MM_L	Yes (AVS and DVFS)	Supplies VDD_MM_L logic voltage domain (that is, DSP and IVA)
vdda_dpll_core	VDDA_DPLL_CORE	No (fixed)	DPLL_CORE analog power supply
vdda_dpll_mpu	VDDA_DPLL_MPU	No (fixed)	DPLL_MPU analog power supply
vdda_dpll_mm	VDDA_DPLL_IVA	No (fixed)	DPLL_IVA analog power supply
vdda_dpll_l4per	VDDA_DPLL_PER	No (fixed)	DPLL_PER analog power supply
vdda_dpll_abe	VDDA_DPLL_ABE	No (fixed)	DPLL_ABE analog power supply
vdda_dpll_usbss	VDDA_DPLL_USB	No (fixed)	DPLL_USB analog power supply
vdda_slicer	VDDA_SLICER	No (fixed)	CLOCK_SLICER power supply
vdd_osc	VDD_OSC	No (fixed)	Clock oscillator core power supply
vdda_ldo_sram_mpu	VDDA_LDO_SRAM_MPU	No	Supplies SLDO_MPU
vdda_ldo_sram_mm	VDDA_LDO_SRAM_MM	No	Supplies SLDO_MM for MM SRAM
vdda_ldo_sram_core	VDDA_LDO_SRAM_CORE	No	Supplies SLDO_CORE for CORE SRAM
vdda_ldo_emu_wkup	VDDA_LDO_EMU_WKUP	No	Supplies LDO_WKUP for WAKEUP/EMU logic
vdda_bdgp	VDDA_BDGP	No (fixed)	BANDGAPs supply input
vdda_ldo_vbb_mpu	VDDA_VBBLDO_MPU	No	MPU VBB LDO supply input
vdda_ldo_vbb_mm	VDDA_VBBLDO_MM	No	MM VBB LDO supply input

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3.4 PRCM Subsystem Integration

The internal configuration registers of the power-management modules can be accessed for configuration and control through their respective L4_WKUP interconnect. In addition to the L4 interconnect, the internal module interface contains the following interfaces and signals:

- A set of signals for idle/wake-up control for each module
- Clocks and reset signals for the modules
- Power control signals (switches and memories) to the power domains
- Interrupts to the MPU, IPU, and DSP INTCs
- Voltage error commands from the SmartReflex modules to the external power IC
- Phase-locked loop (PLL) control commands for recalibration and bypass of the digital phase-locked loops (DPLLs)

Figure 3-18 shows details of the control interface to a generic power domain.

3.4.1 Device Power-Management Layout

The PMFW sees the device split into voltage domains, power domains, and clock domains. Table 3-28 provides the device-level view with module association to the clock, power, and voltage domains.

Table 3-28. PMFW Device-Level Layout

Voltage Domain	Power Domain	Clock Domain	Module
VD_WKUP	PD_EMU	CD_EMU	DEBUGSS
	PD_WKUPAON	CD_WKUPAON	CTRL_MODULE_WKUP
			L4_WKUP interconnect
			GPIO1
			TIMER1
			WD_TIMER2
			SAR_RAM
			PRCM_MPU
			COUNTER_32K
			KBD
			IO_SRCOMP_WKUP
		N/A (the PRCM module)	PRM
		N/A (the PRCM module)	SCRM
VD_CORE	PD_COREAON	CD_COREAON	SMARTREFLEX_CORE
			SMARTREFLEX_MM
			SMARTREFLEX_MPU
			IO_SRCOMP_CORE
			USB2PHY
		N/A (the PRCM module)	CM_CORE_AON
		N/A (clock generator)	DPLL_ABE
		N/A (clock generator)	DPLL_CORE
		N/A (clock generator)	DPLL_PER
		N/A (not clocked by the PRCM module)	WUGEN_IPU
		N/A (not clocked by the PRCM module)	WUGEN_DMA_SYSTEM
		N/A (PRCM itself)	CM_CORE_AON
	PD_CAM	CD_CAM	FDIF
			ISS and CSI_PHY_ISS_ADDON and CSI_PHY_ISS_CORE

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Table 3-28. PMFW Device-Level Layout (continued)

Voltage Domain	Power Domain	Clock Domain	Module
	PD_CORE	CD_L4_CFG	CTRL_MODULE_CORE
			SPINLOCK
			L4_CFG interconnect
			MAILBOX
			SAR_ROM
		CD_EMIF	CMDPHY_EMIF and DATAPHY_EMIF
			DLL_M_EMIF and DLL_S_EMIF
			DMM
			EMIF1
			EMIF2
			EMIF_OCP_FW
		CD_IPU	IPU
		CD_L3_MAIN2	GPMC
			L3_MAIN_2 interconnect
			OCMC_RAM
		CD_L3_INSTR	L3_MAIN_3 interconnect
			L3_INSTR interconnect
			OCP_WP_NOC
			CTRL_MODULE_BANDGAP
		CD_L3_MAIN1	L3_MAIN_1 interconnect
		CD_DMA	DMA_SYSTEM
		N/A (the PRCM module)	CM_CORE
		CD_L4_SEC	DMA_CRYPTO
			AES1
			AES2
			SHA2MD5
			RNG
			DES3DES
			FPKA
		CD_L4_PER	TIMER10
			TIMER11
			TIMER2
			TIMER3
			TIMER4
			TIMER9
			ELM
			GPIO2
			GPIO3
			GPIO4
			GPIO5
			GPIO6
			GPIO7
			GPIO8
			HDQ1W
			I2C1
			I2C2

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Table 3-28. PMFW Device-Level Layout (continued)

Voltage Domain	Power Domain	Clock Domain	Module
			I2C3
			I2C4
			I2C5
			L4_PER interconnect
			MCSPI1
			MCSPI2
			MCSPI3
			MCSPI4
			MMC3
			MMC4
			MMC5
			UART1
			UART2
			UART3
			UART4
			UART5
			UART6
	PD_DSS	CD_DSS	DSS, DSI_PHY_DSS_ADDON, DSI_PHY_DSS_CORE and associated DPLLs
			BB2D
	PD_CUSTEFUSE	CD_CUSTEFUSE	EFUSE_CTRL_CUST
	PD_L3INIT	CD_L3INIT	HSI
			IEEE1500_2_OCP
			MMC1
			MMC2
			OCP2SCP1
			USB_HOST_HS
			USB_OTG_SS
			USB_TLL_HS
			SATA
			OCP2SCP3
		N/A (clock generator)	DPLL_USB
	PD_ABE	CD_ABE	AESS
			DMIC
			L4_ABE interconnect
			MCASP
			MCBSP1
			MCBSP2
			MCBSP3
			MCPDM
			TIMER5
			TIMER6
			TIMER7
			TIMER8
			WD_TIMER3
VD_MM	PD_DSP	CD_DSP	DSP
	PD_GPU	CD_GPU	GPU

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Table 3-28. PMFW Device-Level Layout (continued)

Voltage Domain	Power Domain	Clock Domain	Module
	PD_MMAON	N/A (not clocked by the PRCM module)	WUGEN_DSP
		N/A (clock generator)	DPLL_IVA
	PD_IVA	CD_IVA	IVA
			SL2
VD_MPU	PD_MPUAON	N/A (clock generator)	DPLL_MPU
		N/A (not clocked by the PRCM module)	INTC_MPU, TIMER_MPU_C0 and TIMER_MPU_C1
	PD_MPU	CD_MPU	MPU

3.4.2 Power-Management Scheme, Reset, and Interrupt Requests

3.4.2.1 Power Domain

Table 3-29 lists the PMFW modules and their associated power domains.

Table 3-29. PMFW Module Power Domains

PMFW Module	Power Domain
SCRM	PD_WKUPAON
PRM	PD_WKUPAON
CM_CORE_AON	PD_COREAON
CM_CORE	PD_CORE
SMARTREFLEX_MPU	PD_COREAON
SMARTREFLEX_MM	PD_COREAON
SMARTREFLEX_CORE	PD_COREAON

The PRM part of the PRCM module is in the PD_WKUPAON power domain, which is continuously active. It is composed of the logic that must be permanently supplied to manage domain power-state transitions and detect wake-up events.

The CM_CORE_AON part of the PRCM module is in the PD_COREAON power domain, which is an always-on power domain, while the CM_CORE part of the PRCM module is in the PD_CORE power domain, which can be activated and deactivated according to the requirements of the executing applications.

3.4.2.2 Resets

The PMFW modules are reset by independent reset signals (see Table 3-30).

Table 3-30. PMFW Module Reset Signals

PMFW Module	Reset Signal
SCRM	SYS_PWRON_RST_IN
PRM	SYS_PWRON_RST_IN
CM_CORE_AON	CM_CORE_AON_PWRON_RST
	CM_CORE_AON_RST
CM_CORE	CM_CORE_PWRON_RET_RST
	CM_CORE_RET_RST
SMARTREFLEX_MPU	COREAON_RST
SMARTREFLEX_MM	COREAON_RST
SMARTREFLEX_CORE	COREAON_RST

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NOTE: For more information about the reset trigger sources and assertion conditions, see Section 3.5.3, *Reset Sources*.

3.4.2.3 Interrupt Requests

The PMFW modules can generate the interrupts listed in Table 3-31.

Table 3-31. PMFW Module Interrupts

Source PMFW Module	Source Signal Name	Destination INTC	Destination Signal Name
PRCM	PRM_MPU_IRQ	INTC_MPU	MPU_IRQ_11
PRCM	PRM_IRQ_IPU	INTC_IPU	IPU_IRQ_47
PRCM	PRM_IRQ_DSP	INTC_DSP	DSP_IRQ_57
SMARTREFLEX_MM	SMARTREFLEX_MM_IRQ	INTC_MPU	MPU_IRQ_102
SMARTREFLEX_MPU	SMARTREFLEX_MPU_IRQ	INTC_MPU	MPU_IRQ_18
SMARTREFLEX_CORE	SMARTREFLEX_CORE_IRQ	INTC_MPU or INTC_IPU	MPU_IRQ_19 or IPU_IRQ_48

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3.5 Reset Management Functional Description

3.5.1 Overview

In the device, the reset scheme is managed by the following modules:

- SCRM: System-level reset management. It provides correct reset routing and sequencing when one or more devices are stacked together in the same package.
- PRM: Device-level reset management

3.5.1.1 SCRM Reset Management Functional Description

The SCRM handles the device power-on and warm reset pads, sys_nrespwron and sys_nreswarm resets. The SCRM:

- Extends the reset duration beyond the pad reset release
- Routes the device pad resets to the reset manager in the PRM module

The SCRM is functionally sensitive to the device POR. However, some of the register bits of the SCRM registers are reset when a device warm reset occurs.

3.5.1.1.1 Power-On Reset

The SCRM receives the device POR on the sys_nrespwron reset pad of the device. It extends the duration of the POR to the device PRM module until at least a stable 32-kHz clock can be provided to it. The 32-kHz clock version of the device is active once the SCRM releases the internal POR. The SCRM automatically deasserts the reset.

The SCRM automatically requests the system clock under a POR condition. This mechanism is functionally active on the 32-kHz clock.

The POR can also be asserted through software control. Software must enable the software reset assertion feature by setting the SCRM.EXTPWRONRSTCTRL[0] ENABLE bit and then by setting the SCRM.EXTPWRONRSTCTRL[1] PWRONRST bit to assert the reset.

3.5.1.1.2 Warm Reset

The device warm reset can be received from an external source through the sys_nreswarm warm reset pad or from the device PRM module as a result of an internal event.

The SCRM extends the duration of the device pad warm reset to the device PRM module.

The SCRM routes a warm reset source (that is, sys_nreswarm pad/PRM module) to a warm reset destination (that is, the PRM module).

The status of a warm reset source for each destination is logged in the corresponding SCRM.EXTWARMRSTST_REG[0] EXTWARMRSTST bit, when the destination reset is released. This is done at the 32-kHz clock.

Software must clear the reset status bit.

When one source of any global warm reset is detected, PRCM logic insures that all voltage domains have transitioned to ON state before starting warm reset sequence.

3.5.1.2 PRM Reset Management Functional Description

The PRM module manages the resets to all power domains inside the device.

NOTE: The PRM module has no knowledge or control over resets generated locally within a module (for example, through the <Module name>_SYSCONFIG[x] SOFTRESET configuration register bit). A software reset has the same effect on the module logic as a hardware reset.

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All PRM reset outputs are asynchronously asserted, while the deassertion is synchronous to the SYS_CLK clock. The reset managers in PRM use this clock for internal stall (delay) counter to delay deassertion of reset when the input reset source is deasserted.

In each power domain one or more reset domains are defined. A reset domain is defined by a unique reset signal that originates from the reset manager and is connected to one or more modules of the device. All the connected modules of the reset domain are reset simultaneously when the reset signal is asserted. Independent control of these reset domains allows sequencing of the release of resets and ensures a safe reset of the entire power domain.

NOTE: All internal reset signals are active low, including the DPLL reset signals.

3.5.2 General Characteristics of Reset Signals

Reset signals can be categorized based on four criteria:

- Scope: Global or local reset
- Occurrence: Cold or warm reset
- Source type: Software-controlled or hardware-triggered reset
- Retention type: Retention reset or nonretention reset

3.5.2.1 Scope

A reset signal can be categorized according to its scope (the area of the device affected by the reset):

- Global reset: Affects the entire logic of the device; all modules are reset. Generally, occurs when the device powers up or an abnormal operation is detected.
- Local reset: Affects one power domain, reset domain, or module. Generally, when a power domain transitions from a switched-off state to an active state, or when a software-reset control bit for a domain is set, only the group of modules within that domain is affected.

3.5.2.2 Occurrence

A reset signal can be categorized depending on when the reset occurs:

- Cold reset: Occurs only on device power up or in certain emulation modes. The cold reset is a global reset that affects every module in the device. It usually corresponds to the initial POR.
- Warm reset: Occurs when the device is in normal operating state. A module can use a warm reset to reset a subset of its logic. This is often done to speed up reset recovery time; that is, the time to transition to a safe operating state, compared to the time required upon receipt of a cold reset. Warm reset events include software-triggered reset per power domain, watchdog time-out, externally triggered and emulation initiated.

Modules that behave differently in cold reset and warm reset have two reset signals: RST and PWRON_RST. These reset signals reconstruct warm reset and cold reset in modules that require them.

The following modules are reset upon global cold reset events and not upon global warm reset events:

- All DPLLs associated with the PRCM module
- EMIF
- Control module: All the module instances in the PD_WKUPAON power domain

NOTE: For information about the PRCM module registers affected by the global warm reset, see the register description in Section 3.11, *PRCM Register Manual*.

3.5.2.3 Source Type

A reset can be categorized depending on whether it is software-controlled or hardware-triggered:

- Software reset: Triggered by setting a bit in a configuration register of the PRCM module

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- Hardware reset: Triggered by a signal from a hardware module inside or outside the PRCM module

3.5.2.4 Retention Type

The power domain manager in PRM controls the assertion of two types of local cold reset sources, retention and nonretention reset. They are identified by the naming convention <PowerDomain>_DOM_RET_RST and <PowerDomain>_DOM_RST, respectively.

Upon transitioning a power domain to the ON-ACTIVE power state from the OFF power state:

- Retention type reset source is always asserted.
- Nonretention type reset source is always asserted.

Upon transitioning a power domain to the ON-ACTIVE power state from a switched-off state:

- Retention type reset source is never asserted.
- Nonretention type reset source is optionally asserted. The software-selectable option enables the PRM to support the CSWRET retention mechanism. Nonretention type reset source is not asserted if the power domain state transitions from the CSWR-RETENTION state.

3.5.3 Reset Sources

The reset sources triggering the reset managers in the PRM are described in this section.

3.5.3.1 Global Reset Sources

Table 3-32 lists the global reset sources of the device. The global reset source signals received by the reset manager trigger the reset of all the device modules. For all hardware reset signals, the source of the reset is identified; for the software reset signals, the bit triggering the reset is identified.

Table 3-32. Global Reset Sources

Type[(1)]	Name	Source/Control	Description
H/C	SYS_PWRON_RST	Received from the SCRM through input pin or through software control	The entire device is reset on power up.
H/W	SYS_WARMIN_RST	Received from the SCRM through input pin or through software control	External hardware warm reset
S/C	GLOBAL_COLD_SW_RST	PRCM module.PRM_RSTCTRL[1] RST_GLOBAL_COLD_SW	Global software cold reset
S/W	GLOBAL_WARM_SW_RST	PRCM module.PRM_RSTCTRL[0] RST_GLOBAL_WARM_SW	Global software warm reset
H/W	VDD_CORE_VOLT_MGR_RST	PRCM module	Asserted by the voltage manager FSMs when no response from the power IC is received during wake-up transition from retention or off mode
H/W	VDD_MM_VOLT_MGR_RST	PRCM module	
H/W	VDD_MPU_VOLT_MGR_RST	PRCM module	
H/W	TSHUT_MPU_RST	MPU voltage domain thermal sensor	Asserted when measured temperature is greater than shutdown temperature threshold
H/W	TSHUT_MM_RST	MM voltage domain thermal sensor	
H/W	TSHUT_CORE_RST	Device thermal sensor, placed close to the ISS, DSP, and IVA	
H/W	ICEPICK_RST	ICEPick™ module	It is used only in emulation mode.
H/W	ICEPICKPOR_RST	ICEPick module	It is used only in emulation mode.
H/W	MPU_WDT_RST	WD_TIMER2 or MPU subsystem	It is triggered by a time-out event.

(1) H = Hardware reset, S = Software reset, C = Cold reset, W = Warm reset

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3.5.3.2 Local Reset Sources

In addition to the global reset sources the device can have a number of local reset sources for each power domain. The local reset sources can be cold or warm reset sources. They can be software-controlled or hardware-triggered. Table 3-33 identifies the possible types of hardware-triggered local cold reset sources. Some power domains can support one or both of these local cold reset sources. The table does not list the software-triggered local warm reset sources that are listed in the reset management section of the respective power domains. A local reset source signal received by the reset manager resets only a specific part of the device (for example, some modules/subsystems within the power domain).

Table 3-33. Local Reset Sources

Type[(1)]	Name	Source/Control	Description
H/C	<Power domain>_RET_RST	PRCM	Asserted only for a power domain state transition to the ON-ACTIVE state
H/C	<Power domain>_RST	PRCM	Asserted for any power domain state transition to the ON-ACTIVE state

(1) H = Hardware reset, C = Cold reset

3.5.4 Reset Domains

A power domain can receive power-on reset (PWRON_RST) and/or normal reset (RST) signals. These signals reset nonretention logic and behave as follows:

- On any global or local cold reset, RST and PWRON_RST are asserted.
- On any global or local warm reset, only RST is asserted.

A power domain can receive two additional retention logic reset signals: power-on retention reset (PWRON_RET_RST) and/or retention reset (RET_RST). These signals behave as follows:

- On any global cold reset or wakeup from an off (no power supply) state to the ON-ACTIVE state, RET_RST and PWRON_RET_RST are asserted.
- On any global warm reset, only RET_RST is asserted.
- On wakeup from RETENTION state, these signals are not asserted.

This section discusses the trigger sources and attributes for all reset domains of the device. For an explanation of each reset trigger source of the device, see Section 3.5.3, *Reset Sources.*

Table 3-34 identifies the associated power and rest domains for each module.

Table 3-34. Modules, Power Domains, and Reset Domains Association

Module	Power Domain	Reset Domains
CM_CORE_AON	PD_COREAON	CM_CORE_AON_PWRON_RST, CM_CORE_AON_RST
DPLL_ABE	PD_COREAON	COREAON_PWRON_RST
DPLL_CORE	PD_COREAON	COREAON_PWRON_RST
DPLL_PER	PD_COREAON	COREAON_PWRON_RST
WUGEN_IPU	PD_COREAON	None
WUGEN_DMA_SYSTEM	PD_COREAON	None
SMARTREFLEX_CORE	PD_COREAON	COREAON_RST
SMARTREFLEX_MM	PD_COREAON	COREAON_RST
SMARTREFLEX_MPU	PD_COREAON	COREAON_RST
USB_PHY_AON	PD_COREAON	COREAON_RST
SPINNER	PD_COREAON	None
IO_SRCOMP_CORE	PD_COREAON	COREAON_PWRON_RST
DPLL_IVA	PD_MMAON	DPLL_IVA_PWRON_RST
WUGEN_DSP	PD_MMAON	MMAON_RST
DPLL_MPU	PD_MPUAON	DPLL_MPU_PWRON_RST

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Table 3-34. Modules, Power Domains, and Reset Domains Association (continued)

Module	Power Domain	Reset Domains
INTC_MPU	PD_MPUAON	MPUAON_RST
AESS	PD_ABE	ABE_RST
CKGEN_ABE	PD_ABE	ABE_PWRON_RST
DMIC	PD_ABE	ABE_RST
L4_ABE interconnect	PD_ABE	ABE_RST
MCASP	PD_ABE	ABE_RST
MCBSP1	PD_ABE	ABE_RST
MCBSP2	PD_ABE	ABE_RST
MCBSP3	PD_ABE	ABE_RST
MCPDM	PD_ABE	ABE_RST
TIMER5	PD_ABE	ABE_RST
TIMER6	PD_ABE	ABE_RST
TIMER7	PD_ABE	ABE_RST
TIMER8	PD_ABE	ABE_RST
WD_TIMER3	PD_ABE	ABE_RST
FDIF	PD_CAM	CAM_RST
ISS	PD_CAM	CAM_RST
EFUSE_CTRL_CUST	PD_CUSTEFUSE	CUSTEFUSE_RST
CM_CORE	PD_CORE	CM_CORE_PWRON_RET_RST, CM_CORE_RET_RST
CTRL_MODULE_CORE	PD_CORE	CORE_PWRON_RET_RST
CTRL_MODULE_BANDGAP	PD_CORE	CORE_PWRON_RET_RST
EMIFPHY	PD_CORE	EMIF_DDR_PHY_PWRON_RST
DLL	PD_CORE	DLL_RST
DLL_AGING	PD_CORE	CORE_RST
DMM	PD_CORE	CORE_RST
IPU	PD_CORE	IPU_PWRON_RST, IPU_RET_RST, IPU_CPU0_RST, IPU_CPU1_RST, IPU_MMU_CACHE_RST
EMIF1	PD_CORE	CORE_PWRON_RET_RST, CORE_PWRON_RST
EMIF2	PD_CORE	CORE_PWRON_RET_RST, CORE_PWRON_RST
EMIF_OCP_FW	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
GPMC	PD_CORE	CORE_RET_RST
SPINLOCK	PD_CORE	CORE_RET_RST
L3_MAIN_2 interconnect	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
L3_MAIN_3 interconnect	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
L3_MAIN_1 interconnect	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
L3_INSTR interconnect	PD_CORE	CORE_RST
OCP_WP_NOC	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
L4_CFG interconnect	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
MAILBOX	PD_CORE	CORE_RET_RST
OCMC_RAM	PD_CORE	CORE_RST
SAR_ROM	PD_CORE	CORE_RST
DMA_SYSTEM	PD_CORE	SDMA_RET_RST
DSS	PD_DSS	DSS_RET_RST, DSS_RST
BB2D	PD_DSS	DSS_RST
CM_EMU	PD_EMU	EMU_PWRON_RST

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Table 3-34. Modules, Power Domains, and Reset Domains Association (continued)

Module	Power Domain	Reset Domains
DEBUGSS	PD_EMU	EMU_EARLY_PWRON_RST, EMU_PWRON_RST, EMU_RST
GPU	PD_GPU	GPU_RST
IVA	PD_IVA	IVA_PWRON_RST, IVA_RST, IVA_SEQ1_RST, IVA_SEQ2_RST
SL2	PD_IVA	IVA_RST
CKGEN_USB	PD_L3INIT	L3INIT_PWRON_RST
DPLL_USB	PD_L3INIT	DPLL_L3INIT_PWRON_RET_RST
HSI	PD_L3INIT	L3INIT_RET_RST
IEEE1500_2_OCP	PD_L3INIT	L3INIT_RST
MMC1	PD_L3INIT	L3INIT_RET_RST
MMC2	PD_L3INIT	L3INIT_RET_RST
USB_OTG_SS	PD_L3INIT	L3INIT_RET_RST
USB_HOST_HS	PD_L3INIT	L3INIT_RET_RST
USB_TLL_HS	PD_L3INIT	L3INIT_RET_RST
OCP2SCP1	PD_L3INIT	L3INIT_RST
OCP2SCP3	PD_L3INIT	L3INIT_RST
SATA	PD_L3INIT	L3INIT_RST
TIMER10	PD_CORE	CORE_RST
TIMER11	PD_CORE	CORE_RST
TIMER2	PD_CORE	CORE_RST
TIMER3	PD_CORE	CORE_RST
TIMER4	PD_CORE	CORE_RST
TIMER9	PD_CORE	CORE_RST
ELM	PD_CORE	CORE_RST
GPIO2	PD_CORE	CORE_RET_RST
GPIO3	PD_CORE	CORE_RET_RST
GPIO4	PD_CORE	CORE_RET_RST
GPIO5	PD_CORE	CORE_RET_RST
GPIO6	PD_CORE	CORE_RET_RST
GPIO7	PD_CORE	CORE_RET_RST
GPIO8	PD_CORE	CORE_RET_RST
HDQ1W	PD_CORE	CORE_RST
I2C1	PD_CORE	CORE_RET_RST
I2C2	PD_CORE	CORE_RST
I2C3	PD_CORE	CORE_RST
I2C4	PD_CORE	CORE_RST
I2C5	PD_CORE	CORE_RST
L4_PER interconnect	PD_CORE	CORE_PWRON_RET_RST, CORE_RST
MCSPI1	PD_CORE	CORE_RST
MCSPI2	PD_CORE	CORE_RST
MCSPI3	PD_CORE	CORE_RST
MCSPI4	PD_CORE	CORE_RST
MMC3	PD_CORE	CORE_RST
MMC4	PD_CORE	CORE_RST
MMC5	PD_CORE	CORE_RST
UART1	PD_CORE	CORE_RET_RST
UART2	PD_CORE	CORE_RET_RST

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Table 3-34. Modules, Power Domains, and Reset Domains Association (continued)

Module	Power Domain	Reset Domains
UART3	PD_CORE	CORE_RET_RST
UART4	PD_CORE	CORE_RET_RST
UART5	PD_CORE	CORE_RET_RST
UART6	PD_CORE	CORE_RET_RST
DMA_CRYPTO	PD_CORE	CORE_RET_RST
AES1	PD_CORE	CORE_RET_RST
AES2	PD_CORE	CORE_RET_RST
SHA2MD5	PD_CORE	CORE_RET_RST
RNG	PD_CORE	CORE_RET_RST
DES3DES	PD_CORE	CORE_RET_RST
FPKA	PD_CORE	CORE_RST
MPU	PD_MPU	MPU_PWRON_RST, MPU_RST, MPU_MA_PWRON_RET_RST, MPU_MA_RET_RST, MPU_MA_RST
DSP	PD_DSP	DSP_RST, DSP_PWRON_RST, DSP_RET_RST, DSP_SYS_RST
CTRL_MODULE_WKUP	PD_WKUPAON	WKUPAON_PWRON_RST
PRM	PD_WKUPAON	PRM_PWRON_RST, PRM_RST
PRCM_MPU	PD_WKUPAON	LPRM_PWRON_RST, LPRM_RST
GPIO1	PD_WKUPAON	WKUPAON_RST
KBD	PD_WKUPAON	WKUPAON_RST
SAR_RAM	PD_WKUPAON	WKUPAON_RST
COUNTER_32K	PD_WKUPAON	WKUPAON_RST, WKUPAON_SYS_PWRON_RST
TIMER1	PD_WKUPAON	WKUPAON_RST
WD_TIMER2	PD_WKUPAON	WKUPAON_RST
L4_WKUP interconnect	PD_WKUPAON	WKUPAON_RST
IO_SRCOMP_WKUP	PD_WKUPAON	WKUPAON_PWRON_RST

Table 3-35 lists the reset sources that trigger the reset domains of the device.

Table 3-35. Reset Sources for the Reset Domains

Reset Domain	Reset Source	Reset Source Type
ABE_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
ABE_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
CM_CORE_AON_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
CM_CORE_AON_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
COREAON_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
	IO_SRCOMP_CORE	Global cold
COREAON_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
MMAON_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
MPUAON_RST	GLOBAL_COLD_SW_RST	Global cold

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
MPU_L2RSTDISABLE	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
CAM_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
CM_CORE_PWRON_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
CM_CORE_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
CORE_PWRON_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	SYS_PWRON_RST	Global cold
	ICEPICKPOR_RST	Global cold
CORE_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	SYS_PWRON_RST	Global cold
	ICEPICKPOR_RST	Global cold
CORE_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
CORE_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
CUSTEFUSE_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
DLL_RST	DLL_FREQCHANGE_RST	Local warm
	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
DPLL_IVA_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
DPLL_L3INIT_PWRON_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
DPLL_MPU_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
DSS_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
DSS_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
IPU_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
IPU_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	RM_IPU_RSTCTRL[2] RST_IPU_MMU_CACHE	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
IPU_CPU0_RST	IPU_ICECRUSHER0_RST	Local warm
	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	RM_IPU_RSTCTRL[0] RST_CPU0	Local Warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
IPU_CPU1_RST	IPU_ICECRUSHER1_RST	Local Warm
	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	RM_IPU_RSTCTRL[1] RST_CPU1	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
IPU_MMU_CACHE_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	RM_IPU_RSTCTRL[2] RST_IPU_MMU_CACHE	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
EMIF_DDR_PHY_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
EMU_EARLY_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	SYS_PWRON_RST	Global cold
EMU_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
EMU_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
GPU_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
IVA_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
IVA_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	RM_IVA_RSTCTRL[2] RST_LOGIC	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
IVA_SEQ1_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	IVA_ICECRUSHER1_RST	Local warm
	MPU_WDT_RST	Global warm
	RM_IVA_RSTCTRL[0] RST_SEQ1	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
IVA_SEQ2_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	IVA_ICECRUSHER2_RST	Local warm
	MPU_WDT_RST	Global warm
	RM_IVA_RSTCTRL[1] RST_SEQ2	Local warm
	SYS_PWRON_RST	Global cold

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
L3INIT_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
L3INIT_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
L3INIT_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
MPU_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
MPU_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
MPU_MA_PWRON_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
MPU_MA_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
MPU_MA_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
SDMA_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	ICEPICK_RST	Global warm
DSP_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	RM_DSP_RSTCTRL[0] RST_DSP	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	DSP_EMU_RESET_REQ_TR	Local warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
DSP_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
DSP_RET_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	RM_DSP_RSTCTRL[1] RST_DSP_MMU_CACHE	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
DSP_SYS_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	RM_DSP_RSTCTRL[1] RST_DSP_MMU_CACHE	Local warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	ICEPICK_RST	Global warm
WKUPAON_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
	IO_SRCOMP_WKUP	Global cold
WKUPAON_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
WKUPAON_SYS_PWRON_RST	SYS_PWRON_RST	Global cold
PRM_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm
	ICEPICK_RST	Global warm
PRM_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold
LPRM_RST	GLOBAL_COLD_SW_RST	Global cold
	GLOBAL_WARM_SW_RST	Global warm
	ICEPICKPOR_RST	Global cold
	MPU_WDT_RST	Global warm
	SYS_PWRON_RST	Global cold
	SYS_WARMIN_RST	Global warm
	VDD_CORE_VOLT_MGR_RST	Global warm
	VDD_MM_VOLT_MGR_RST	Global warm
	VDD_MPU_VOLT_MGR_RST	Global warm
	TSHUT_CORE_RST	Global warm
	TSHUT_MM_RST	Global warm
	TSHUT_MPU_RST	Global warm

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Table 3-35. Reset Sources for the Reset Domains (continued)

Reset Domain	Reset Source	Reset Source Type
	ICEPICK_RST	Global warm
LPRM_PWRON_RST	GLOBAL_COLD_SW_RST	Global cold
	ICEPICKPOR_RST	Global cold
	SYS_PWRON_RST	Global cold

Table 3-36 lists the attributes of the reset manager associated with the reset domains. The clock to the reset manager, the delay count before release of reset, and the reset release stall conditions for the reset domains are listed.

Table 3-36. Reset Domains Attributes

Reset Domain	RM Clock	RM Clock Count	Release Stall Conditions
ABE_PWRON_RST	WKUPAON_GCLK	0x0	None
ABE_RST	WKUPAON_GCLK	0x0	None
CM_CORE_AON_PWRON_RST	WKUPAON_GCLK	0x2	None
CM_CORE_AON_RST	WKUPAON_GCLK	0x2	L4_ROOT_CLK clock is not active.
COREAON_PWRON_RST	WKUPAON_GCLK	0x0	None
COREAON_RST	WKUPAON_GCLK	0x0	None
MMAON_RST	WKUPAON_GCLK	ResetTime2 (1)	DSP_GCLK is not active.
MPUAON_RST	WKUPAON_GCLK	ResetTime2 (1)	MPU_GCLK is not active.
CUSTEFUSE_RST	WKUPAON_GCLK	ResetTime2 (1)	CUSTEFUSE_SYS_GFCLK is not active.
CAM_RST	WKUPAON_GCLK	0x0	None
CM_CORE_PWRON_RET_RST	WKUPAON_GCLK	0x2	None
CM_CORE_RET_RST	WKUPAON_GCLK	0x2	L4_ICLK clock is not active.
CORE_PWRON_RET_RST	WKUPAON_GCLK	0x0	None
CORE_RET_RST	WKUPAON_GCLK	0x0	None
CORE_RST	WKUPAON_GCLK	0x0	None
DLL_RST	WKUPAON_GCLK	0x3	None
DPLL_IVA_PWRON_RST	WKUPAON_GCLK	0x0	None
DPLL_L3INIT_PWRON_RET_RST	WKUPAON_GCLK	0x0	None
DPLL_MPU_PWRON_RST	WKUPAON_GCLK	0x0	None
DSS_RET_RST	WKUPAON_GCLK	0x0	None
DSS_RST	WKUPAON_GCLK	0x0	None

(1) ResetTime2 is set in the PRM_RSTTIME[14:10] RSTTIME2 bit field.

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Table 3-36. Reset Domains Attributes (continued)

Reset Domain	RM Clock	RM Clock Count	Release Stall Conditions
IPU_PWRON_RST	WKUPAON_GCLK	ResetTime2 (2)	IPU_GCLK clock is not active, RM_IPU_RSTCTRL[2] RST_IPU_MM U_CACHE bit is set, and automatic restore is complete.
IPU_RET_RST	WKUPAON_GCLK	ResetTime2 (2)	IPU_GCLK clock is not active and the subsystem is reset.
IPU_CPU0_RST	WKUPAON_GCLK	ResetTime2 (2)	IPU_GCLK clock is not active and the subsystem is reset.
IPU_CPU1_RST	WKUPAON_GCLK	ResetTime2 (2)	IPU_GCLK clock is not active.
IPU_MMU_CACHE_RST	WKUPAON_GCLK	ResetTime2 (2)	IPU_GCLK clock is not active and the subsystem is reset.
EMIF_DDR_PHY_PWRON_RST	WKUPAON_GCLK	0x0	None
EMU_EARLY_PWRON_RST	WKUPAON_ICLK	0x20	None
EMU_PWRON_RST	WKUPAON_ICLK	ResetTime2 (2)	EMU_SYS_GCLK clock is not active.
EMU_RST	WKUPAON_ICLK	ResetTime2 (2)	EMU_SYS_GCLK clock is not active.
GPU_RST	WKUPAON_GCLK	0x0	None
IVA_PWRON_RST	WKUPAON_GCLK	ResetTime2 (2)	IVA_GCLK clock is not active and RM_IVA_RSTCTRL[2] RST_LOGIC bit is set.
IVA_RST	WKUPAON_GCLK	ResetTime2 (2)	IVA_GCLK clock is not active.
IVA_SEQ1_RST	WKUPAON_GCLK	ResetTime2 (2)	IVA_GCLK clock is not active and IVA and SL2 are idle.
IVA_SEQ2_RST	WKUPAON_GCLK	ResetTime2 (2)	IVA_GCLK clock is not active and IVA and SL2 are idle.
L3INIT_PWRON_RST	WKUPAON_GCLK	0x0	None
L3INIT_RET_RST	WKUPAON_GCLK	0x0	None
L3INIT_RST	WKUPAON_GCLK	0x0	None
MPU_L2RSTDISABLE	WKUPAON_GCLK	ResetTime2 + 32 (2)	MPU_RST is asserted high or PD_MPU is OFF.
MPU_MA_PWRON_RET_RST	WKUPAON_GCLK	ResetTime2 (2)	MPU_DPLL_CLK clock is not active.
MPU_MA_RET_RST	WKUPAON_GCLK	ResetTime2 (2)	MPU_DPLL_CLK clock is not active.
MPU_MA_RST	WKUPAON_GCLK	ResetTime2 (2)	MPU_DPLL_CLK clock is not active.
MPU_PWRON_RST	WKUPAON_GCLK	ResetTime2 (2)	MPU_DPLL_CLK clock is not active.
MPU_RST	WKUPAON_GCLK	ResetTime2 (2)	MPU_DPLL_CLK clock is not active, the subsystem is reset, and automatic restore is complete.
DMA_RET_RST	WKUPAON_GCLK	0x0	None
DSP_RST	WKUPAON_GCLK	ResetTime2 (2)	DSP_GCLK clock is not active and the subsystem is reset.
DSP_PWRON_RST	WKUPAON_GCLK	ResetTime2 (2)	DSP_GCLK clock is not active, RM_DSP_RSTCTRL[1] RST_DSP_MMU_CACHE bit is cleared, and automatic restore is complete.

(2) ResetTime2 is set in the PRM_RSTTIME[14:10] RSTTIME2 bit field.

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Table 3-36. Reset Domains Attributes (continued)

Reset Domain	RM Clock	RM Clock Count	Release Stall Conditions
DSP_RET_RST	WKUPAON_GCLK	ResetTime2[3]	DSP_GCLK clock is not active and the subsystem is reset.
DSP_SYS_RST	WKUPAON_GCLK	ResetTime2[3]	DSP_GCLK clock is not active and the subsystem is reset.
WKUPAON_PWRON_RST	WKUPAON_GCLK	0x0	None
WKUPAON_RST	WKUPAON_GCLK	0x0	None
WKUPAON_SYS_PWRON_RST	WKUPAON_GCLK	0x0	None
PRM_PWRON_RST	WKUPAON_GCLK	0x0	WKUPAON_ICLK clock is not active.
PRM_RST	WKUPAON_GCLK	0x0	WKUPAON_ICLK clock is not active.
LPRM_PWRON_RST	WKUPAON_GCLK	0x0	WKUPAON_ICLK clock is not active.
LPRM_RST	WKUPAON_GCLK	0x0	WKUPAON_ICLK clock is not active.

(3) ResetTime2 is set in the PRM_RSTTIME[14:10] RSTTIME2 bit field.

NOTE: WKUPAON_SYS_PWRON_RST is connected directly to the SYS_PWRON_RST source reset.

3.5.5 Reset Logging

A reset of the device is logged in two ways:

1. Dedicated registers in the PRCM module (the RM_<Power domain>_RSTST) log the reset sources to the power domain.
2. The control module logs the device reset activity in dedicated registers.

3.5.5.1 PRCM Module Reset Logging Mechanism

The reset status registers RM_<power domain>_RSTST and PRM_RSTST are reset asynchronously on assertion of a global cold reset. However, a reset status bit is always logged when the reset is released to the domain.

For this reason, after the assertion of a global cold reset, the reset status register is cleared to 0. When the domain reset is released, the register bit to log the global cold reset (the PRM_RSTST[0] GLOBAL_COLD_RST bit) is updated to 1. For the same reason, the reset status register of domains released from reset by software is updated only when software releases the domain reset.

The assertion of a global cold reset prevents logging any other source of reset until after the release of the domain reset. This is valid in the following situations:

- A source of reset other than global cold reset is asserted before, during, or after the active period of a global cold source of reset and before the release of the domain reset signal.
- A source of reset other than global cold reset is asserted and then released, but a global cold reset source is asserted before the release of the domain reset signal.

3.5.6 Reset Sequences

3.5.6.1 SCRM Power-On Reset Sequence

Figure 3-19 shows the power-on reset sequence as the reset is received by the SCRM, and the resulting interaction between the SCRM and PRCM modules. Figure 3-20 shows the power-on reset sequence within the PRCM module.

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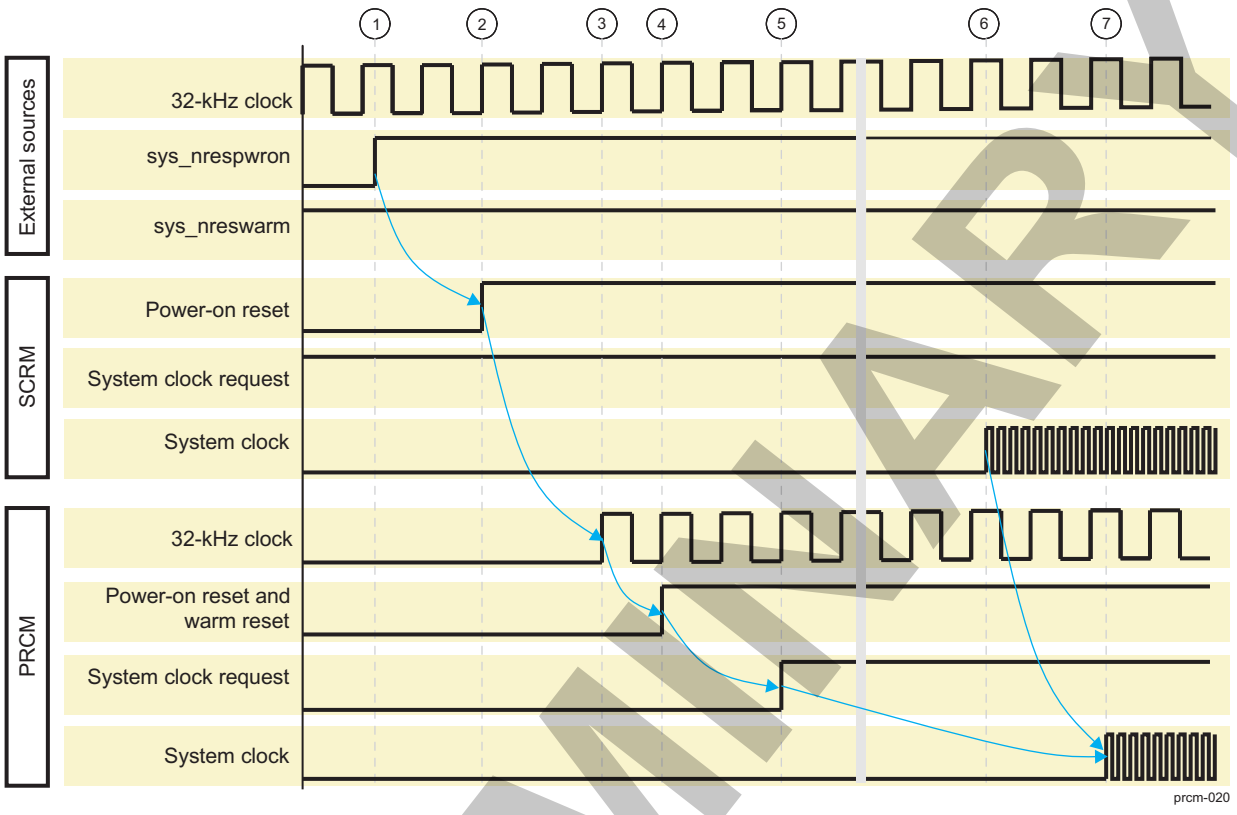
Figure 3-19. SCRM Power-On Reset Sequence



The power-on reset sequence is:

1. The power-on reset pad is released from reset when the 32-kHz clock is already active.
2. SCRM releases its internal power-on reset clocked at the 32-kHz clock.
3. SCRM delays the release of the PRCM module resets to account for the stabilization time of the system clock source. It routes the 32-kHz clock to the PRCM module.
4. SCRM releases the PRCM module from reset (both power-on and warm reset).
5. The PRCM module asserts a system clock request to the SCRM.
6. Once the system clock setup-time counter overflows, the internal system clock version of SCRM is stable.
7. SCRM ungates the system clock to the PRCM module.

3.5.6.2 PRCM Module Power-On Reset Sequence

Figure 3-20 shows the power-on reset sequence.

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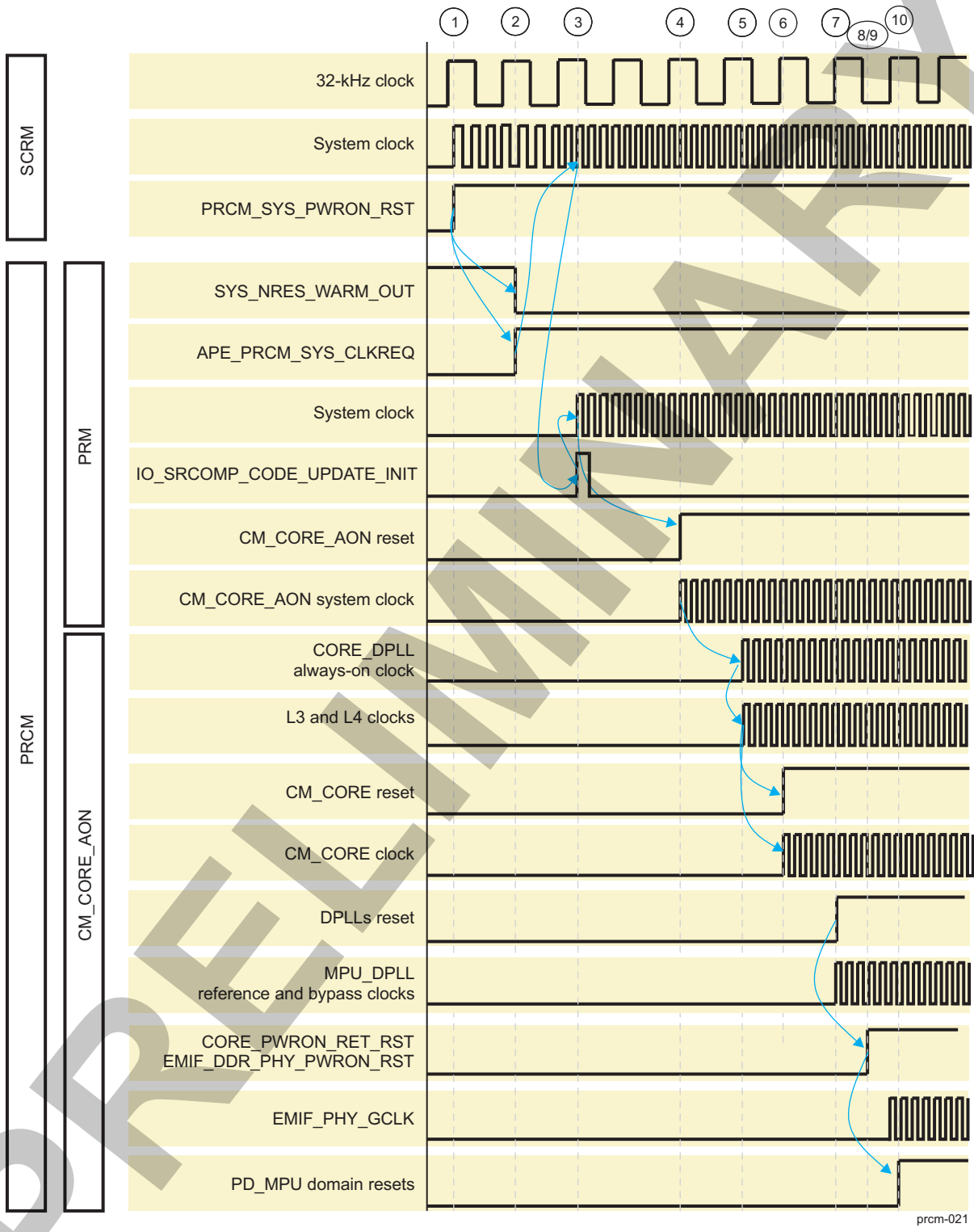
Figure 3-20. PRCM Module Power-On Reset Sequence



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The assumptions are:

- All the logic and memory voltage sources are at their nominal voltage levels.
- The SCRM module is supplying the 32-kHz clock to the PRCM module and the clock is stable.
- The power-on reset (SYS_PWRON_RST_IN) has been released by the external power IC.

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The power-on reset sequence is:

1. The SCRM releases a global power-on reset to the PRCM module (that is, PRCM_SYS_PWRON_RST). As a result, the PRCM module starts the Power-On Reset sequence.
2. The PRCM module releases SYS_NRES_WARM_OUT to the SCRM (only after all voltage domains are ramped up) after some 32-kHz clock cycles, and it also asserts APE_PRCM_SYS_CLKREQ to the SCRM module to request the system clock.
3. The SCRM provides the system clock to the PRCM module when the system clock source is stable. After LDOs stabilization, PRM generates IO_SRCOMP_CODE_UPDATE_INIT signal (one cycle pulse) used by the slew rate compensation cells to load default compensation code defined in CTRL_MODULE_CORE.
4. The PRM logic is then released from reset. The PRM provides CM_CORE_AON with a version of the system clock and releases CM_CORE_AON from reset.
5. CM_CORE_AON starts the reference clock (and also the bypass clock) of the CORE DPLL. In turn, the CORE DPLL, which is configured in bypass mode, generates the L3 clock (running at the system clock frequency at this stage). Now the CM_CORE_AON logic is fully operational: CM_CORE_AON logic is released from reset and the L3 clock is running.
6. CM_CORE_AON starts the L4 clock version for CM_CORE_AON, and the PRM deasserts the reset of CM_CORE.
7. The DPLLs are released from reset. The DPLLs can be released from reset before the L3 clock is running. The DPLL being under reset does not prevent the output clock from running. CM_CORE_AON starts the reference and bypass clocks to DPLL_MPU.
8. The CORE is released from reset, provided the L3 clock is running. The EMIF comes out of reset as soon as the CORE power domain power on retention reset (CORE_PWRON_RET_RST) (see Table 3-36) is released by the PRCM module. The PRCM module also releases EMIF_DDR_PHY_PWRON_RST. The EMIF_PHY_GCLK clock is not running at this point; hence, all the PHYs are asynchronously reset at the same time. The EMIF_PHY_GCLK clock is started later.
9. The PRCM module releases the IDLE request signal to the EMIF module once the EMIF functional clock is enabled. The EMIF then acknowledges the deassertion of IDLE request and becomes active.
10. The MPU subsystem is released from reset provided its clock is active and the L3 interconnect is operational.

NOTE:

- The PD_DSP and PD_IVA power domains are held under reset after power up by the assertion of software source of reset.
- After the power-up sequence completes, software must reprogram the value of the PRM_RSTTIME[9:0] RSTTIME1 bit field to ensure that in case of a new warm reset assertion, generated global warm reset is extended for a sufficient time (defined by the external power IC requirements).

3.5.6.3 MPU Subsystem Power-On Reset Sequence

Figure 3-21 shows the POR sequence of the MPU subsystem.

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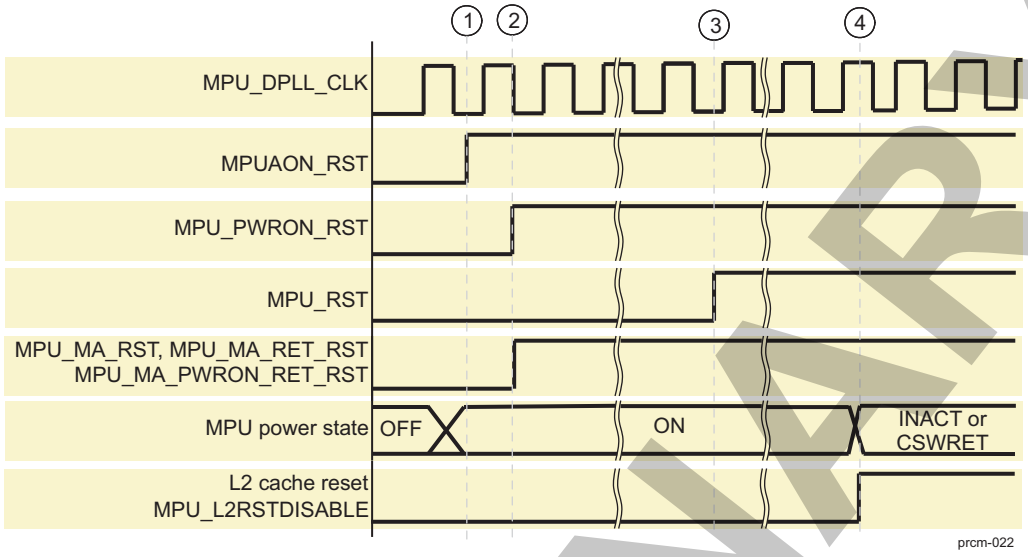
Figure 3-21. MPU Power-On Reset Sequence



The assumptions after power-on reset assertion are:

- The PRCM module provides the DPLL_MPU reference clock and the bypass clock.
- The PRCM module has released DPLL_MPU reset and DPLL_MPU is in bypass mode providing the clock (that is, bypass clock) to all the modules in the MPU subsystem.

The POR sequence is:

1. The PRCM module releases asynchronously in PD_MPUAON the MPUAON_RST reset to the INTC_MPU module in the MPU subsystem.
2. The PRCM module releases in PD_MPU the MPU_PWRON_RST (only after MPU_DPLL_CLK is active) to the MPU subsystem and waits until the subsystem completes its internal reset sequence. MA_MPU (Memory-adapter) dedicated reset signals (MPU_MA_RST, MPU_MA_RET_RST, and MPU_MA_PWRON_RET_RST) are released when MPU_DPLL_CLK is running (at the same time as MPU_PWRON_RST).
3. When the MPU subsystem internal reset sequence completes, the PRCM module releases in PD_MPU the MPU_RST signal and the MPU starts booting.
4. The PRCM module drives the MPU_L2RSTDISABLE signal low a minimum of 32 SYS_CLK cycles after MPU_RST is deasserted. The PRCM module keeps the MPU_L2RSTDISABLE signal low until the next power domain transition.

NOTE:

- The reset to the L2 cache memory (MPU_L2RSTDISABLE) in the MPU subsystem is asserted during initial POR (that is, when the PD_MPU wakes up from OFF state). It is also asserted during local or global warm reset. However, it is not asserted when the PD_MPU wakes up from RETENTION state (that is, when the logic is OFF and L2 memory is in RETENTION state). This ensures that the L2 cache is retained on wakeup.
- The L1 cache memory in the MPU subsystem is not retained on PD_MPU wakeup.

For more information about power management in the MPU subsystem, see Section 4.3.7, *MPU Subsystem Power Management*, in Chapter 4, *Dual Cortex-A15 MPU Subsystem*,

3.5.6.4 MPU Subsystem Warm Reset Sequence

Figure 3-22 shows the warm reset sequence of the MPU subsystem.

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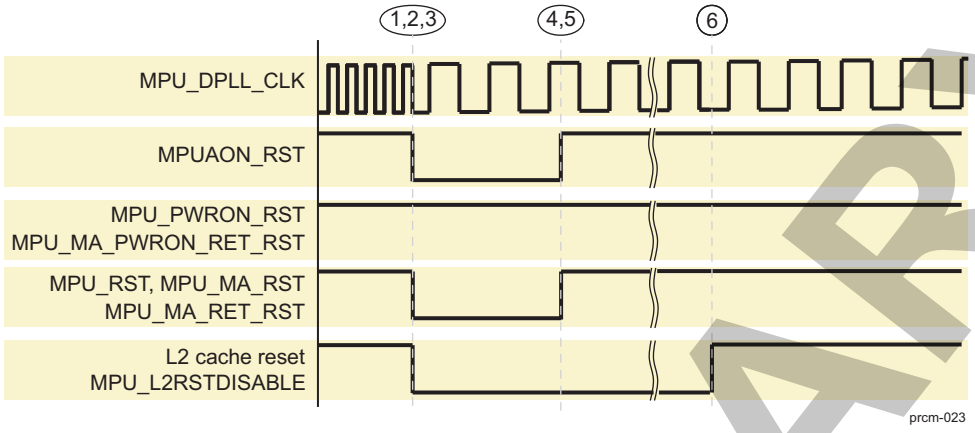
Figure 3-22. MPU Warm Reset Sequence



The assumptions are:

- The DPLL_MPU is locked and is providing the clock to the MPU subsystem.
- A global or local warm reset to the MPU subsystem is asserted.

The warm reset sequence is:

1. The PRCM module asserts in PD_MPUAON the MPUAON_RST reset to the INTC_MPU module in the MPU subsystem. The MPU DPLL is locked.
2. The PRCM module asserts in PD_MPU the MPU_RST reset to the MPU subsystem and also asserts MPU_MA_RST and MPU_MA_RET_RST resets to the MA_MPU module.
3. The PRCM module resets the L2 cache memory in the MPU subsystem by asserting its reset.
4. The PRCM module releases the MPUAON_RST reset to the INTC_MPU module. The MPU DPLL is in bypass mode.
5. The PRCM module releases MPU_RST, MPU_MA_RST, and MPU_MA_RET_RST only after DPLL_MPU is in bypass mode and MPU_DPLL_CLK is stable and active.
6. The PRCM module drives the MPU_L2RSTDISABLE signal low a minimum of 32 SYS_CLK cycles after MPU_RST is deasserted. The PRCM keeps the MPU_L2RSTDISABLE signal low until the next power domain transition.

3.5.6.5 MPU Subsystem Reset Sequence on Sleep and Wake-Up Transitions From RETENTION and OFF States

Figure 3-23 shows the sleep and wake-up transitions reset sequence from the RETENTION and off (no power supply) states of the MPU subsystem.

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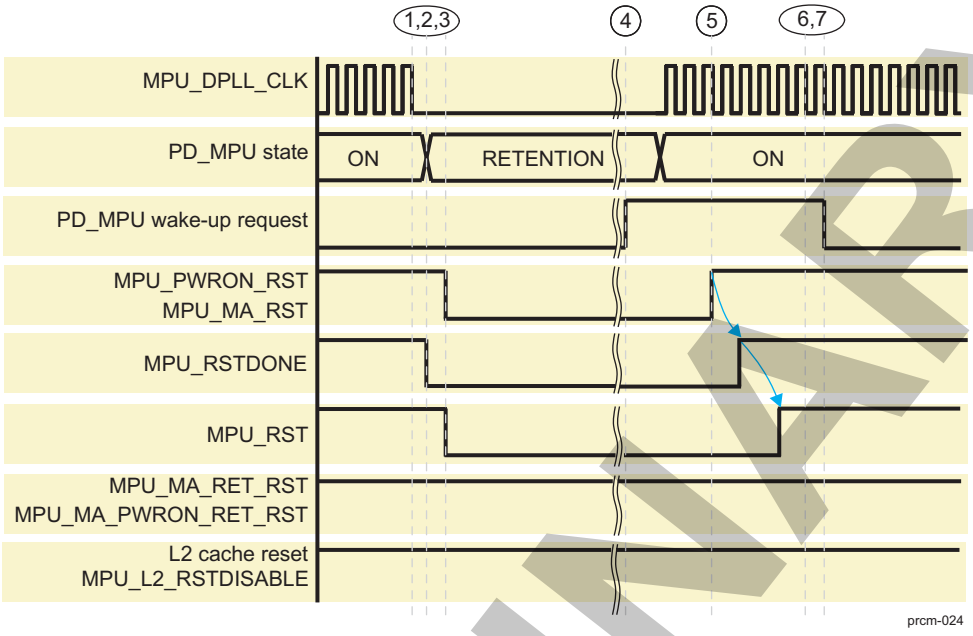
Figure 3-23. MPU Reset Sequence on Sleep and Wake-Up Transition



The assumption is:

- The DPLL_MPU is locked and is providing the clock to the MPU subsystem.

The sleep and wake-up transitions reset sequence is:

1. The PRCM module gates MPU_DPLL_CLK to the MPU subsystem.
2. The PRCM module switches PD_MPU to RETENTION state.
3. The PRCM module asserts MPU_PWRON_RST and MPU_RST resets to the MPU subsystem, and asserts MPU_MA_RST to the MA_MPU module. The entire logic in the PD_MPU is held in reset. The reset to the L2 cache memory in the MPU subsystem is not asserted if the logic in PD_MPU is held in reset.
4. The PRCM module resets the L2 cache memory in the MPU subsystem by asserting its reset.
5. The PRCM module releases MPU_RST only after the DPLL_MPU is in bypass mode and the MPU_DPLL_CLK is stable and active. The PRCM deasserts the MPU_PWRON_RST, MPU_MA_RST. When PRCM receives active MPU_RSTDONE signal from MPU, it de-asserts MPU_RST.
6. During the wakeup from RET state, the MPU_L2RSTDISABLE signal must be maintained at active high so the L2 cache will not be reset when the MPU is reset.

3.5.6.6 IVA Subsystem Power-On Reset Sequence

Figure 3-24 shows the power-on reset sequence of the IVA subsystem.

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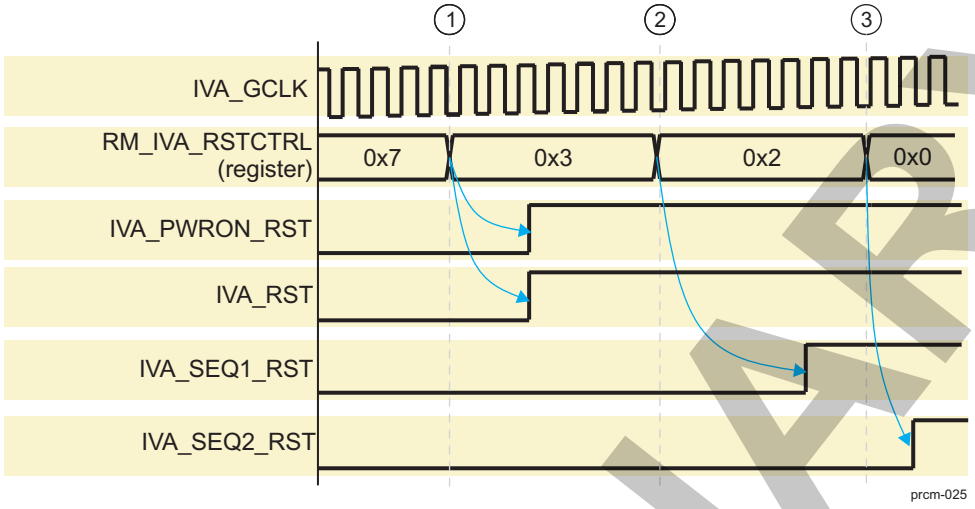
Figure 3-24. IVA Power-On Reset Sequence



The power-on reset to IVA is applied when PD_IVA is powered. The assumptions after power-on reset assertion are:

- The PRCM module provides the IVA_GCLK functional clock to the IVA subsystem, and it has been enabled by MPU software control.

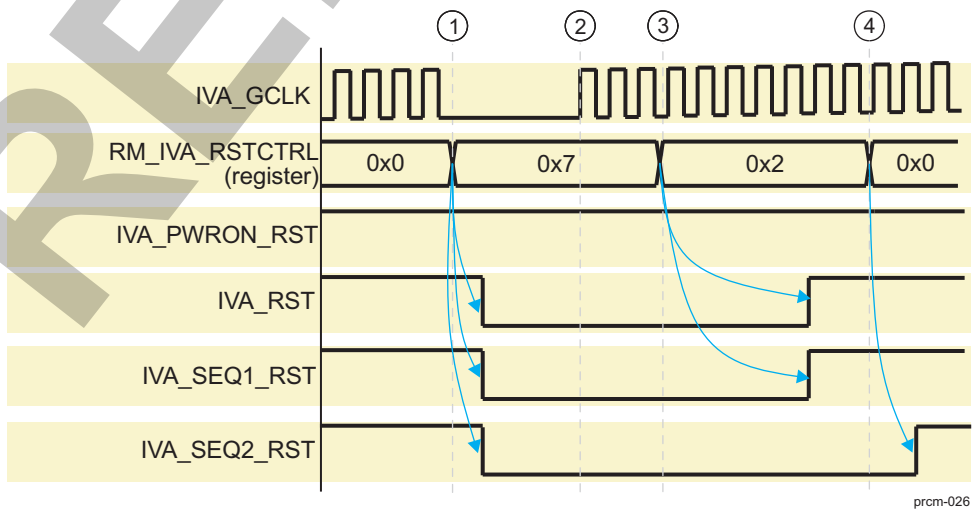
The power-on reset sequence is:

1. Software clears the RM_IVA_RSTCTRL[2] RST_LOGIC bit. This causes the PRCM module to release the IVA_PWRON_RST reset used inside IVA mainly to reset the emulation logic and the IVA_RST reset used to reset all logic inside IVA. Then software can download data into TCM memory while keeping the sequencer CPUs under reset.
2. When the TCM memory is initialized, software clears the RM_IVA_RSTCTRL[0] RST_SEQ1 bit. This releases IVA_SEQ1_RST reset to the Sequencer1 CPU.
3. Similarly, software can clear the RM_IVA_RSTCTRL[1] RST_SEQ2 bit. This releases IVA_SEQ2_RST reset to the Sequencer2 CPU.

3.5.6.7 IVA Subsystem Software Warm Reset Sequence

Figure 3-25 shows the software warm reset sequence of the IVA subsystem.

Figure 3-25. IVA Software Warm Reset Sequence



Before asserting the software reset to the IVA subsystem the MPU software must ensure that:

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- IVA sequencer CPUs are in IDLE state (CM_IVA_IVA_CLKCTRL[17:16] IDLEST).
- The IVA subsystem is in STANDBY state (CM_IVA_IVA_CLKCTRL[18] STBYST).
- The functional clock to the IVA subsystem has been gated by the PRCM module (CM_IVA_CLKSTCTRL[8] CLKACTIVITY_IVA_GCLK).

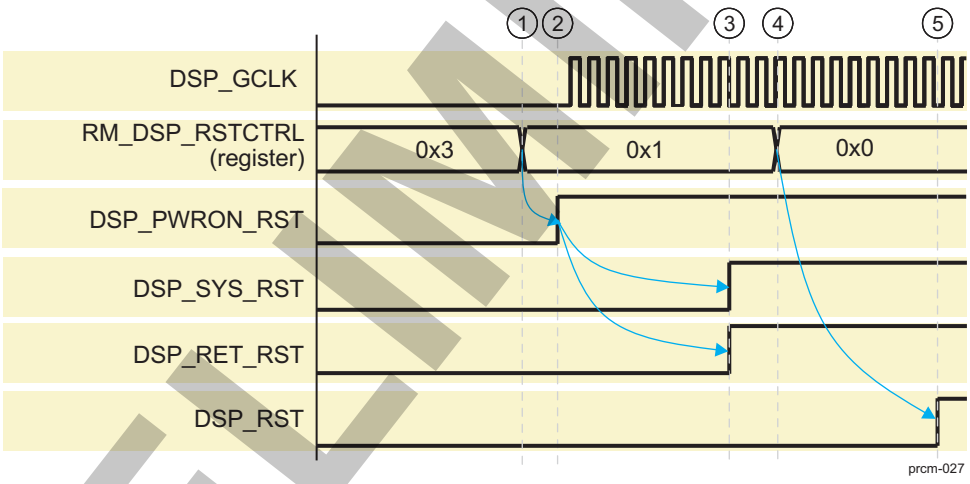
The software reset sequence is:

1. The MPU software sets the RM_IVA_RSTCTRL[2] RST_LOGIC, RM_IVA_RSTCTRL[1] RST_SEQ2, and RM_IVA_RSTCTRL[0] RST_SEQ1 bits. This causes the PRCM module to assert the IVA_RST, IVA_SEQ1_RST, and IVA_SEQ2_RST resets to the IVA subsystem. The IVA_PWRON_RST remains deasserted.
2. The MPU software enables the functional clock to the IVA subsystem.
3. The MPU software clears the RM_IVA_RSTCTRL[2] RST_LOGIC and RM_IVA_RSTCTRL[0] RST_SEQ1 bits. This causes the PRCM module to release the IVA_RST and IVA_SEQ1_RST resets to the IVA subsystem.
4. The MPU software clears the RM_IVA_RSTCTRL[1] RST_SEQ2 bit. This releases the IVA_SEQ2_RST reset to the Sequencer2 CPU.

3.5.6.8 DSP Subsystem Power-On Reset Sequence

Figure 3-26 shows the power-on reset sequence of the DSP subsystem.

Figure 3-26. DSP Subsystem Power-On Reset Sequence



The assumptions on power-on reset assertion are:

- PD_DSP is on.
- The MPU software sets the CM_DSP_DSP_CLKCTRL[1:0] MODULEMODE bit field to Auto (0x1).
- The MPU software sets the CM_DSP_CLKSTCTRL[1:0] CLKTRCTRL bit field to SW_WKUP or HW_AUTO.
- DPLL_IVA is active and is providing the DSP_GCLK. It can be locked before this sequence.

The Power-On Reset sequence is:

1. MPU software clears the RM_DSP_RSTCTRL[1] RST_DSP_MMU_CACHE bit in the PRCM module register to release the DSP, MMU_DSP, and CACHE_DSP interface from reset.
2. The PRCM module releases DSP_PWRON_RST when the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) reaches its limit. Upon deassertion of the POR signal, the DSP subsystem starts the initialization sequence. During this initialization sequence all the internal registers inside the DSP are properly reset and DSP, MMU_DSP, and CACHE_DSP interface are reset.
3. When the reset sequence of Step 2 completes and the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) expires, the PRCM module releases the DSP_SYS_RST and DSP_RET_RST signals.
4. MPU software must configure the MMU_DSP once the MMU_DSP is out of reset. After MMU_DSP

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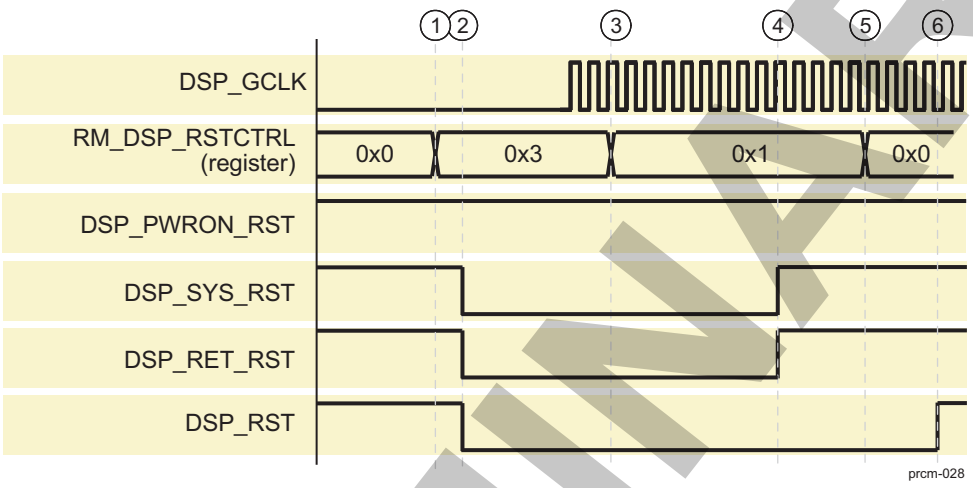
configuration is done, MPU software clears the RM_DSP_RSTCTRL[0] RST_DSP bit in the PRCM module register.

5. The PRCM module releases DSP_RST, which causes the DSP to start booting.

3.5.6.9 DSP Subsystem Software Warm Reset Sequence

Figure 3-27 shows the software warm reset sequence of the DSP subsystem.

Figure 3-27. DSP Subsystem Software Warm Reset Sequence



The assumptions on software warm reset assertion are:

- The DSP is in IDLE state.
- The DSP_GCLK (functional clock) is gated.

The software warm reset sequence is:

1. MPU software sets the RM_DSP_RSTCTRL[1] RST_DSP_MMU_CACHE and RM_DSP_RSTCTRL[0] RST_DSP bits.
2. The PRCM module asserts the DSP_SYS_RST, DSP_RET_RST, and DSP_RST reset signals. DSP_PWRON_RST remains deasserted in this case.
3. MPU software reenables DSP_GCLK and clears the RM_DSP_RSTCTRL[1] RST_DSP_MMU_CACHE bit in the PRCM module register to reset DSP, MMU_DSP, and CACHE_DSP interface. The DSP subsystem starts the partial initialization sequence for the warm reset.
4. When the reset sequence of Step 3 completes and the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) expires, the PRCM module releases the DSP_SYS_RST and DSP_RET_RST signals.
5. MPU software clears the RM_DSP_RSTCTRL[0] RST_DSP bit in the PRCM module register.
6. The PRCM module releases DSP_RST, which causes the DSP to start booting.

3.5.6.10 IPU Subsystem Power-On Reset Sequence

Figure 3-28 shows the power-on reset sequence of the IPU subsystem.

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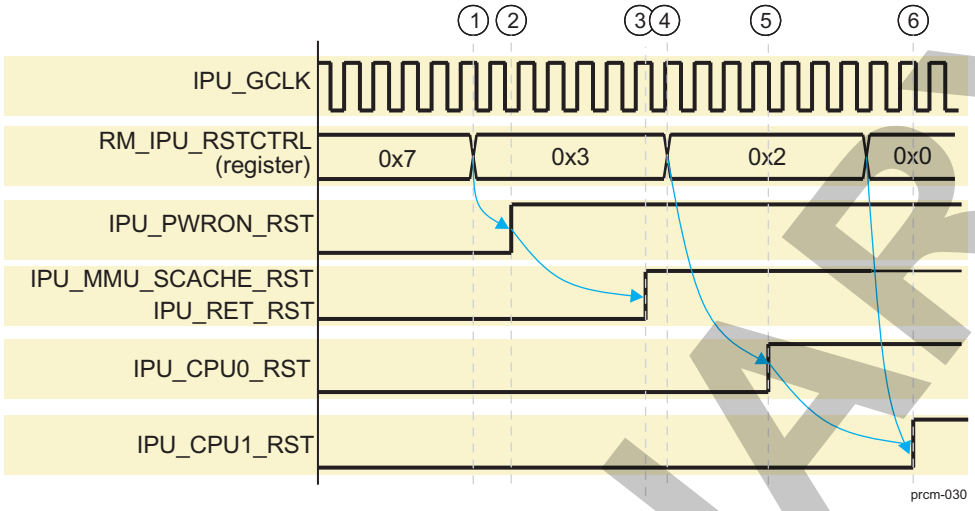
Figure 3-28. IPU Power-On Reset Sequence



The assumptions on power-on reset assertion are:

- The IPU subsystem is held in reset by the PRCM module and the following are asserted:
  - IPU_PWRON_RST
  - IPU_RET_RST
  - IPU_CPU0_RST
  - IPU_CPU1_RST
  - IPU_MMU_CACHE_RST

The power-on reset sequence is:

1. Software clears the RM_IPU_RSTCTRL[2] RST_IPU_MMU_CACHE bit in the PRCM module register to release the IPU shared cache and CACHE_MMU_IPU from reset.
2. The PRCM module releases IPU_PWRON_RST once the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) reaches its limit and the IPU_GCLK is running. Upon deassertion of the POR signal, the IPU subsystem starts the CPU and CACHE_MMU_IPU initialization sequence.
3. When the reset sequence of Step 2 completes and the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) expires, the PRCM module releases the IPU_MMU_CACHE_RST and IPU_RET_RST signals.
4. MPU software must configure CACHE_MMU_IPU once CACHE_MMU_IPU is out of reset. After CACHE_MMU_IPU configuration and cache initialization is done, MPU software clears the RM_IPU_RSTCTRL[0] RST_CPU0 bit in the PRCM module register.
5. The PRCM module releases IPU_CPU0_RST, which causes IPU_C0 to start booting.
6. MPU software can clear the RM_IPU_RSTCTRL[1] RST_CPU1 bit in the PRCM module register so that the PRCM module releases the IPU_CPU1_RST to IPU_C1.

3.5.6.11 IPU Subsystem Software Warm Reset Sequence

Figure 3-29 shows the software warm reset sequence of the IPU subsystem.

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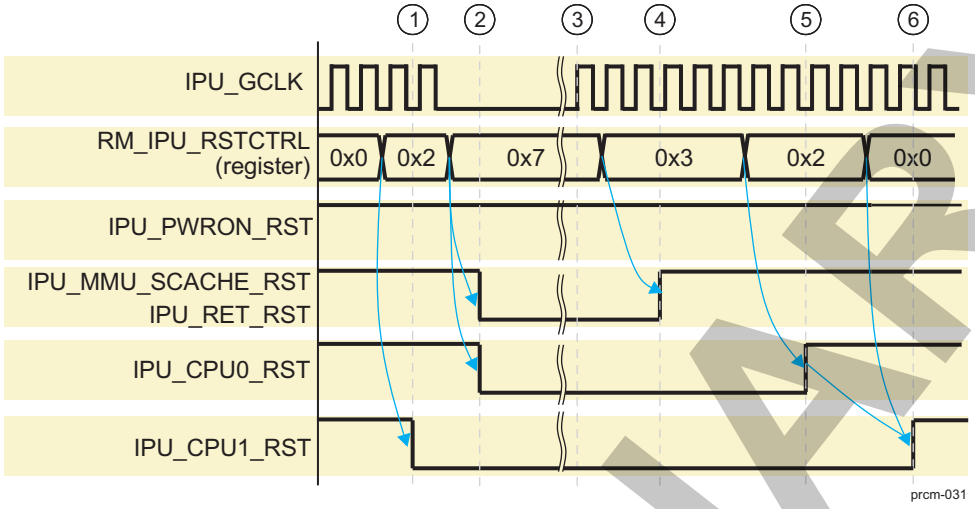
Figure 3-29. IPU Subsystem Software Warm Reset Sequence



For doing the software reset of IPU, the MPU software must ensure that IPU CPUs (IPU_C0 and IPU_C1) are in IDLE state and clock is gated

The software warm reset sequence is:

1. When IPU_C1 is in IDLE state, IPU_C0 software or MPU software sets the RM_IPU_RSTCTRL[1] RST_CPU1 bit. The PRCM module asserts the IPU_CPU1_RST reset signal to IPU_C1.
2. When IPU_C0 is in IDLE state, the MPU software sets the RM_IPU_RSTCTRL[2] RST_IPU_MMU_CACHE and RM_IPU_RSTCTRL[0] RST_CPU0 bits.
3. The PRCM module asserts the IPU_MMU_CACHE_RST, IPU_RET_RST, and IPU_CPU0_RST reset signals. The IPU_PWRON_RST remains deasserted in this case.
4. The MPU software reenables the IPU_GCLK and the initialization sequence starts inside the IPU subsystem. Software clears the RM_IPU_RSTCTRL[2] RST_IPU_MMU_CACHE bit and RM_IPU_RSTCTRL[0] RST_CPU0 bit in the PRCM module register.
5. When the reset sequence of Step 4 completes and the reset manager counter (PRM_RSTTIME[14:10] RSTTIME2) expires, the PRCM module releases the IPU_MMU_CACHE_RST, IPU_RET_RST, and IPU_CPU0_RST reset signals. IPU_C0 starts rebooting.
6. Software can then clear the RM_IPU_RSTCTRL[1] RST_CPU1 bit in the PRCM module register. The PRCM module releases the IPU_CPU1_RST reset signal to IPU_C1 to start booting.

3.5.6.12 Global Warm Reset Sequence

This section describes the global warm reset sequence.

Figure 3-30 shows the global warm reset sequence.

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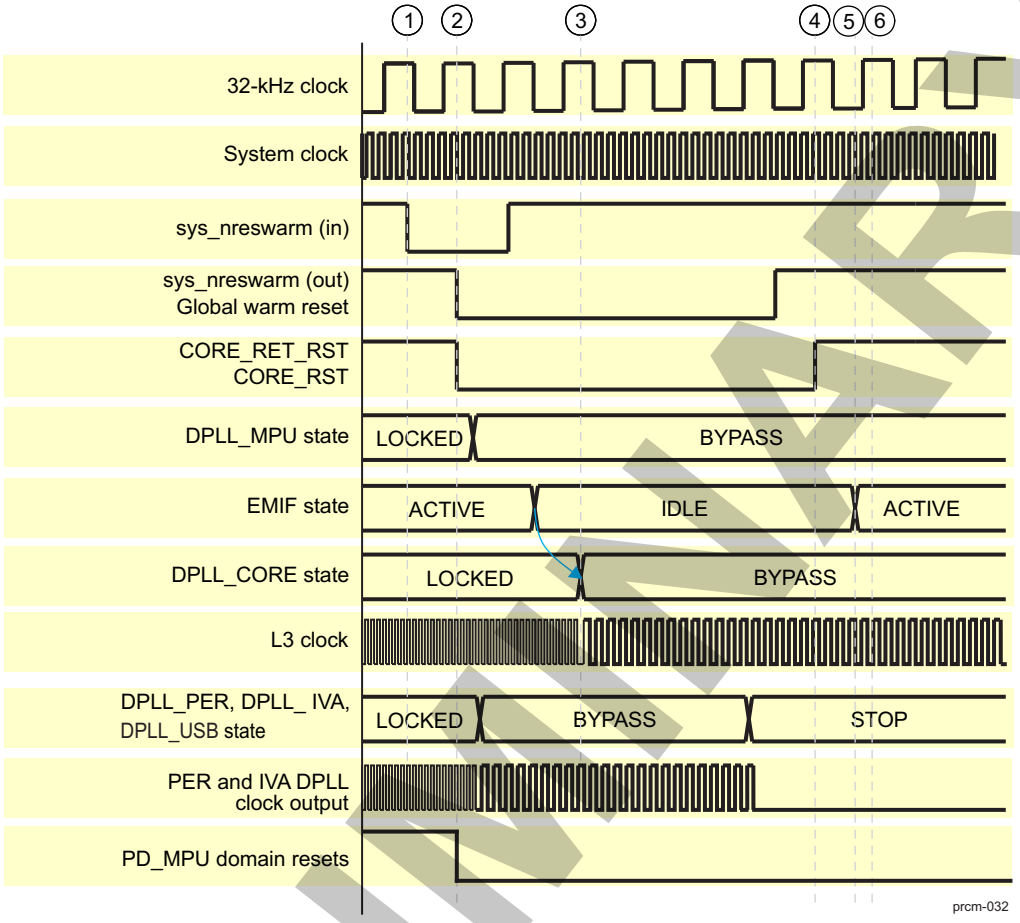
Figure 3-30. Global Warm Reset Sequence



The assumptions are:

- All the logic and memory voltage sources are at their nominal voltage levels.
- The device is active:
  - All resets are released.
  - MPU, CORE, and IVA DPLLs are locked.

The steps of a global warm reset sequence are:

1. On assertion of any global warm reset source the PRM signals the EMIF that a global warm reset event has occurred. The EMIF initiates the transition to IDLE state. The PRCM module delays global warm reset to the device for a minimum of 16 L3 clock cycles so that the EMIF switches to IDLE state and switches the external SDRAM to self-refresh mode.
2. The reset managers in the PRM assert the following resets:
   - The external warm reset SYS_WARM_RST (output) to the SCRM
   - All power domain warm resets are asserted.
   - DPLL hardware resets are not asserted.
     - DPLL_MPU transitions to bypass mode.
     - DPLL_CORE transitions to bypass mode once the EMIF switches to IDLE state.
     - DPLL_IVA, DPLL_PER and DPLL_USB transition to idle bypass low-power mode. Then as clock signals are no more requested, they are gated and these DPLLs goes to stop mode.
     - DPLL_ABE configuration is not changed.
   - The system clock remains active.
   - The PRM and CM registers, sensitive to warm reset, are asynchronously reset.

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- CM gates the clocks that are not needed, as per their default reset setting in the associated registers.

3. After the warm reset source is released, the global warm reset (internal and external) is extended until the following conditions are met:
   - The device reset manager counter overflows. It is set up by the PRM_RSTTIME[9:0] RSTTIME1 bit field. During this time, the DPLL_ABE control registers are reset and DPLL_ABE transitions to bypass mode when the system clock restarts and the DPLL_ABE outputs are no longer used.
   - All logic voltage sources (VD_MM, VD_MPU and VD_CORE) are stable.

NOTE: Voltage stabilization is an additional condition if voltage scaling was performed before the assertion of the warm reset.

4. The CORE power domain is released from reset (that is, warm reset-sensitive modules in the CORE power domain).
5. The PRCM module switches the EMIF from IDLE state back to ACTIVE state.
6. PD_MPU is released from reset when the clocks to the MPU subsystem are active. The MPU reboots.

NOTE:

- The PD_DSP and PD_IVA power domains are held under reset after global warm reset by assertion of the software source of the reset.
- The following are held under reset after global warm reset until the PRCM module enables their interface clock:
  - PD_L3INIT
  - PD_DSS
  - PD_GPU
  - PD_CAM

External power IC is sensitive to warm reset. When it detects a warm reset, it initiates its warm reset sequence to ramp all regulators.

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3.6 Clock Management Functional Description

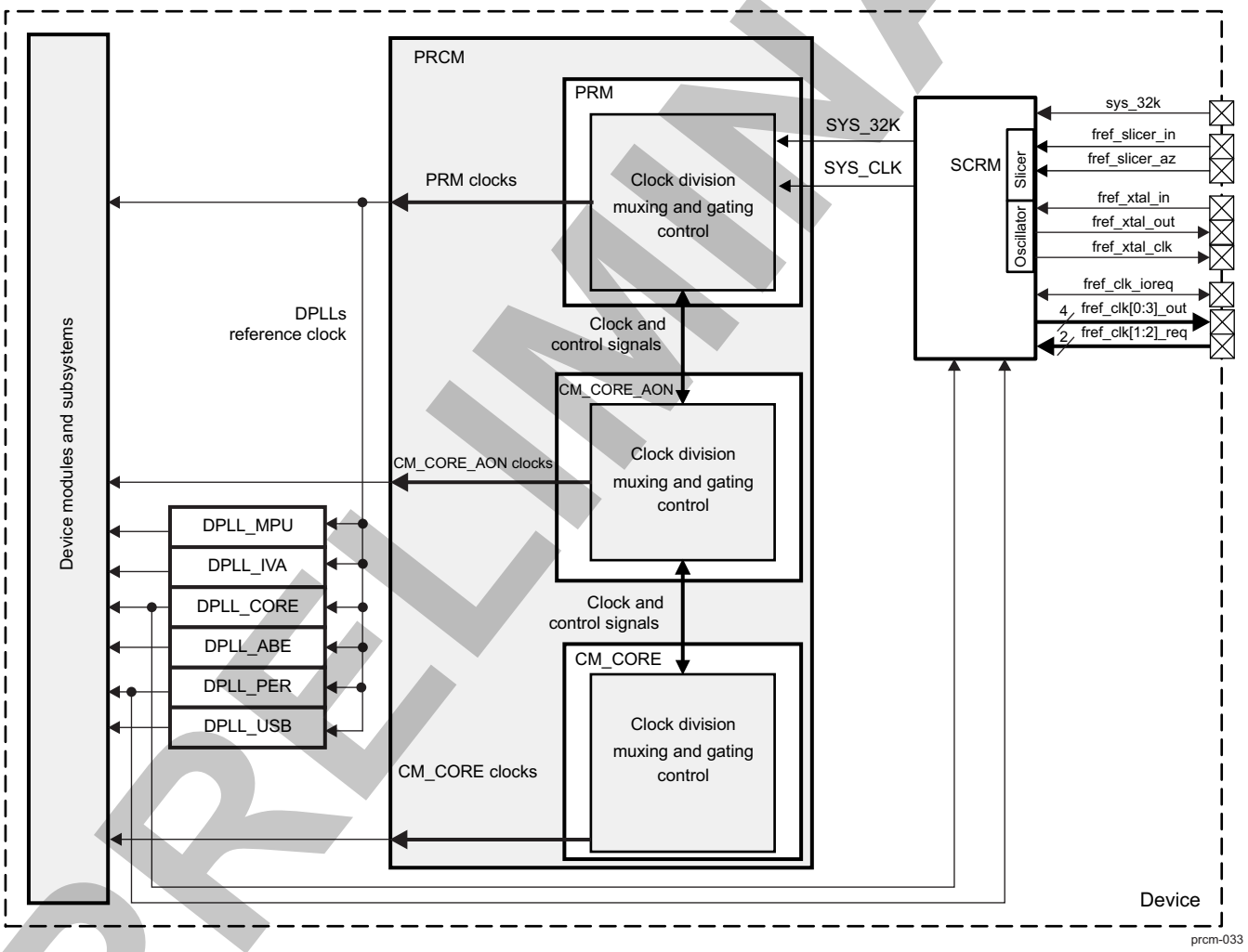
3.6.1 Overview

The PRCM module provides the control for clock generation, division, distribution, synchronization, and gating. It distributes the clock sources to all modules in the device. For information about the clock-management functional architecture of the device, see Section 3.1.1.1, *Clock Management*.

The high-frequency system clock is received by the device from an external source or generated within the device (internal oscillator) by the SCRM. The SCRM also receives the 32-kHz low-frequency clock from the external source.

The stable versions of the system and 32-kHz clock are provided by the SCRM to the PRCM module. The PRCM module provides clocks to the internal DPLLs for internal high-frequency clock generation. Clock division and gating are handled by the PRM, CM_CORE_AON, and CM_CORE sections of the PRCM module. Figure 3-31 shows the high-level clock-management scheme in the device.

Figure 3-31. PRCM Module Clock Manager Overview



3.6.2 External Clock Inputs

3.6.2.1 sys_32k Clock Input

The 32-kHz frequency is used for low-frequency operation (timer, debouncing, etc.). It supplies the always-on wake-up domain for operation in lowest power mode and as the clock source to the DPLL_ABE module (for audio back-end [ABE]).

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3.6.2.2 High-Frequency System Clock Input

The system clock, SYS_CLK, is the main source clock of the device. SYS_CLK is received directly from the SCRM by the PRM subsection of the PRCM module. It is supplied as the reference clock to the DPLLs and as functional clock to several modules.

3.6.3 Internal Clock Sources/Generators

The PRCM module clock sources/generators are split into the following parts:

- PRM clock source that receives the 32-kHz and system clocks from SCRM
- CM_CORE_AON and CM_CORE clock sources that distribute high-frequency clocks
- DPLL clock generators that synthesize high-frequency clocks for the device

Table 3-37. Internal Clock Sources

Clock Name	Source	Frequency	Note
FUNC_32K_CLK	SYS_32K	32KHz	See Section 3.6.3.1, *PRM Clock Source*
SYS_CLKIN	SYS_CLKIN	12, 16.8, 19.2, 26, 38.4MHz	See Section 3.6.3.1, *PRM Clock Source*
FUNC_96M_AON_CLK	DPLL_PER	96MHz	See Section 3.6.3.4, *DPLL_PER Description*
FUNC_192M_CLK	DPLL_PER	192MHz	See Section 3.6.3.4, *DPLL_PER Description*
FUNC_256M_CLK	DPLL_PER	256MHz	See Section 3.6.3.4, *DPLL_PER Description*
CORE_CLK	DPLL_CORE	532MHz	See Section 3.6.3.5, *DPLL_CORE Description*

3.6.3.1 PRM Clock Source

The PRM clock source receives the SYS_32K and SYS_CLK clocks from the SCRM. Along with these clocks, it receives a clock (ABE_LP_CLK) from ABE, generated by DPLL_ABE. The PRM manages the low-frequency clocks associated with these three input clocks. The PRM sources various versions (through gating controls) of these externally sourced clocks to supply:

- PRCM-managed DPLLs with a reference clock, which is permanently supplied with always-on buffers
- The SMARTREFLEX modules with a reference clock, which is permanently supplied with always-on buffers
- The DSS with a reference clock, which is permanently supplied with always-on buffers
- The various timers and watchdog timers with clocks supplied by always-on buffers
- The clocks for the CM clock generator and the CORE power domain
- A version of SYS_CLK to ABE supplied by always-on buffers
- Timer functional clocks
- The bandgap and control module for thermal sensor feature
- Reference clock for various modules:
  - USB_OTG_SS
  - SATA

Figure 3-32 is a logical representation of the PRM clock source.

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Figure 3-32. PRM Clock Manager Overview

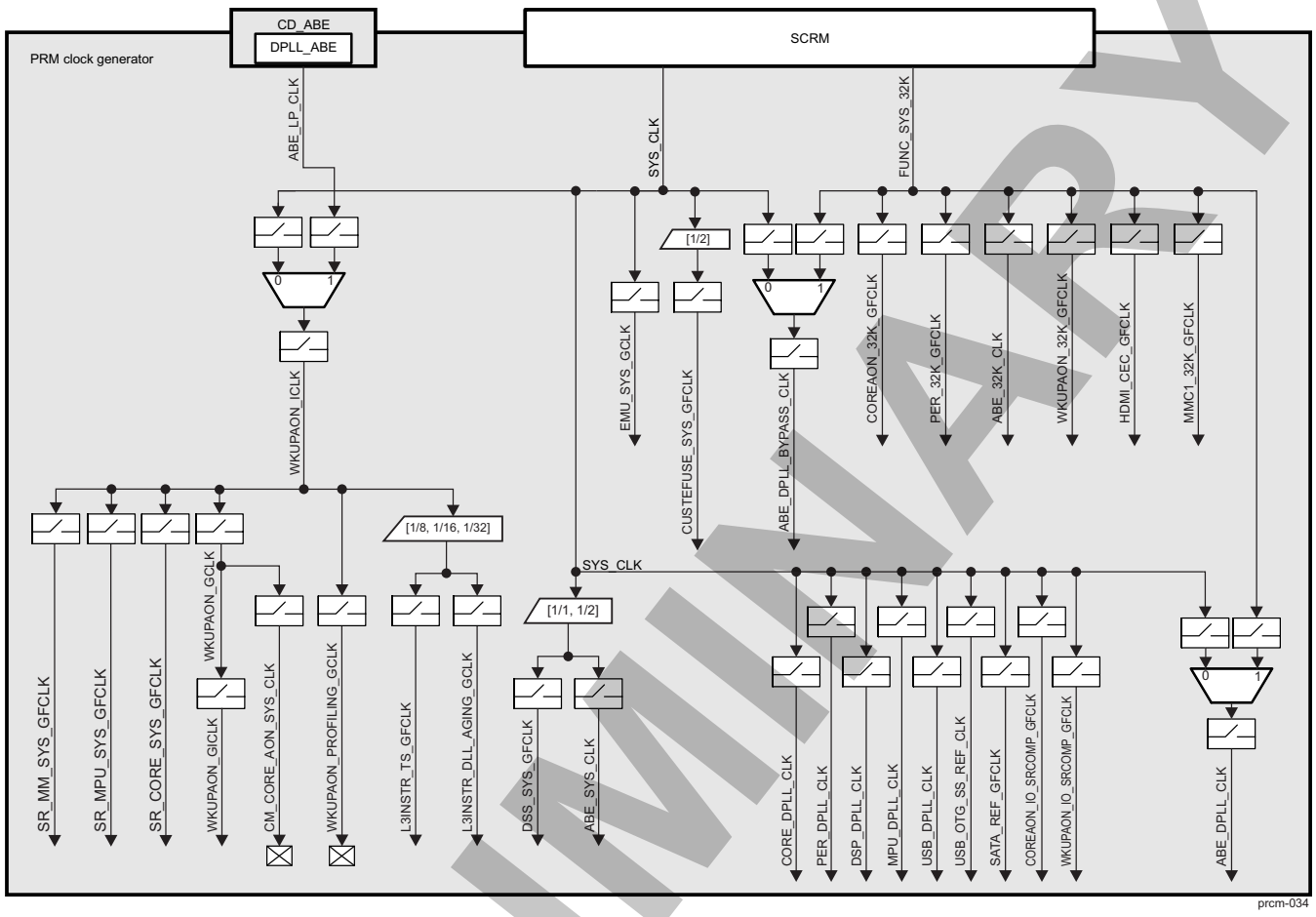

Table 3-38 identifies controls for clock dividers or muxes in the PRM.

Table 3-38. PRM Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Mux ABE_DPLL_CLK	CM_CLKSEL_ABE_PLL_REF[0] CLKSEL
Mux WKUPAON_ICLK	CM_CLKSEL_WKUPAON[0] CLKSEL
Mux ABE_DPLL_BYPASS_CLK	CM_CLKSEL_WKUPAON[0] CLKSEL
Divider ABE_SYS_CLK and DSS_SYS_GFCLK	CM_CLKSEL_ABE_DSS_SYS[0] CLKSEL
Divider MPU_DPLL_CLK – ABE	CM_MPU_MPU_CLKCTRL[26] CLKSEL_ABE_DIV_MODE
Divider MPU_DPLL_CLK – EMIF	CM_MPU_MPU_CLKCTRL[25:24] CLKSEL_EMIF_DIV_MODE
Divider L3INSTR_TS_GFCLK	CM_L3INSTR_CTRL_MODULE_BANDGAP_CLKCTRL[25:24] CLKSEL

NOTE: For clock signals control (gating/ungating management), see Section 3.1.1.1, *Clock Management*.

The PRM provides a 32-kHz gated and ungated clock for use by portions of the PD_WKUPAON power domain and some peripherals outside the PD_WKUPAON power domain.

It also provides the system clock to the DSS, a gated and buffered version to the WKUPAON_GICLK interconnect clock, and the DPLLs controlled by the PRCM module. The gated version of SYS_CLK is also provided to the SmartReflex modules of the device.

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PRM creates MMC1_32K_GFCLK, a gated version of SYS_32K provided to MMC1. This clock may be used by MMC1 for debouncing. It is controlled by the software through writing bit CM_L3INIT_MMC1_CLKCTRL[8] OPTFCLKEN_32KHZ_CLK.

3.6.3.1.1 CD_PRM_TIMER Overview

Figure 3-33 is an overview of the PRM clock manager related to the device timers.

Figure 3-33. CD_PRM_TIMER

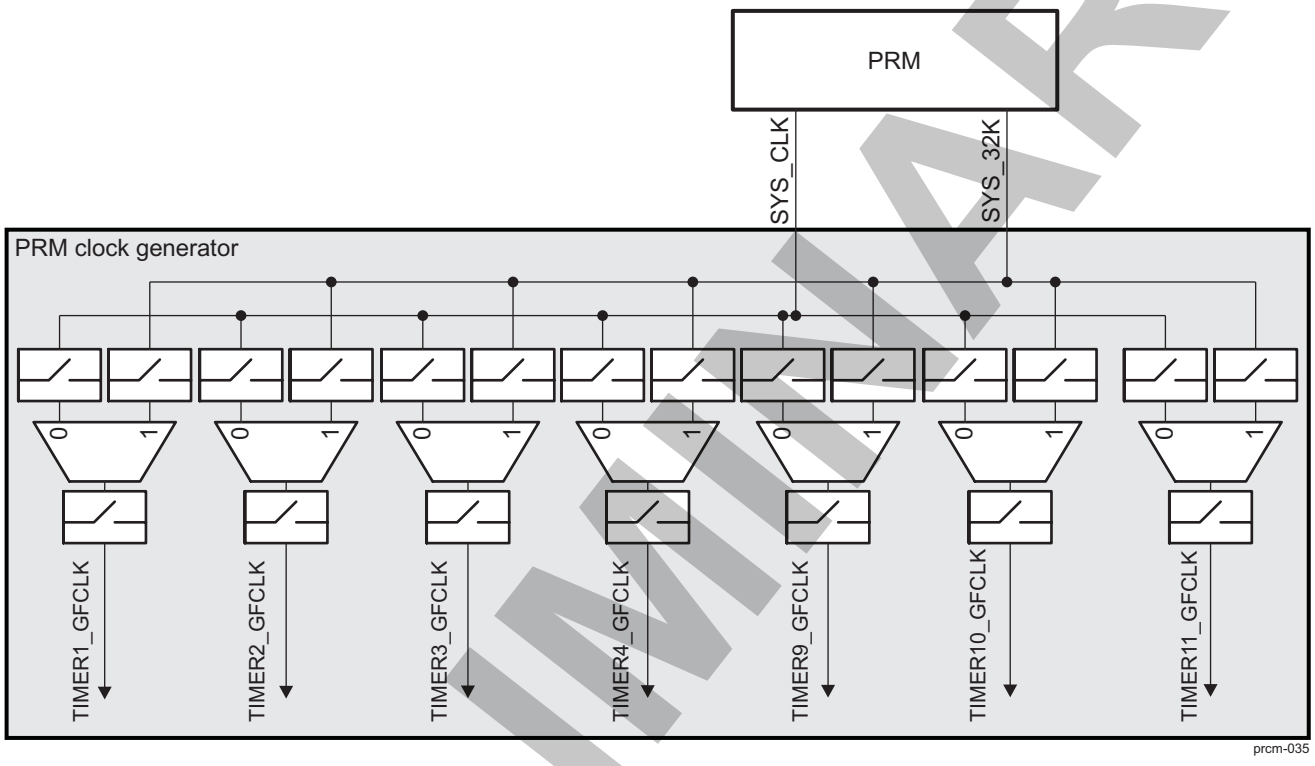

Table 3-39 identifies controls for clock muxes in the CD_PRM_TIMER.

Table 3-39. CD_PRM_TIMER Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Mux TIMER1_GFCLK	CM_WKUPAON_TIMER1_CLKCTRL[24]CLKSEL
Mux TIMER2_GFCLK	CM_L4PER_TIMER2_CLKCTRL[24]CLKSEL
Mux TIMER3_GFCLK	CM_L4PER_TIMER3_CLKCTRL[24]CLKSEL
Mux TIMER4_GFCLK	CM_L4PER_TIMER4_CLKCTRL[24]CLKSEL
Mux TIMER9_GFCLK	CM_L4PER_TIMER9_CLKCTRL[24]CLKSEL
Mux TIMER10_GFCLK	CM_L4PER_TIMER10_CLKCTRL[24]CLKSEL
Mux TIMER11_GFCLK	CM_L4PER_TIMER11_CLKCTRL[24]CLKSEL

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NOTE: For clock signals control (gating/ungating management), see Section 3.1.1.1, *Clock Management*.

3.6.3.2 CM Clock Source

The clock manager (CM) is primarily responsible for generating interface and functional clocks from the internal clocks provided by DPLL_CORE and DPLL_PER. The CM is physically divided into two independent entities: CM_CORE_AON, which is placed in the PD_COREAON always-on power domain, and CM_CORE, which is placed in the PD_CORE switchable power domain. The split is done to provide control over various entities, such as modules, DPLLs, and clocks, during low-power use case scenarios when the PD_CORE power domain can be switched to RETENTION state.

3.6.3.2.1 CM_CORE_AON Clock Generator

CM_CORE_AON receives a system clock from the PRM, which serves as its functional clock. CM_CORE_AON provides a gated clock to PD_ABE, PD_DSP, PD_MPU, and some DPLLs (DPLL_MPU, DPLL_IVA and its associated HSDivider,DPLL_ABE, DPLL_CORE and its associated HSDivider). It also provides the clock to the L3 and L4 interconnects in the device.

Figure 3-34 shows the various functional and interface clocks generated by CM_CORE_AON.

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Figure 3-34. CM_CORE_AON Overview

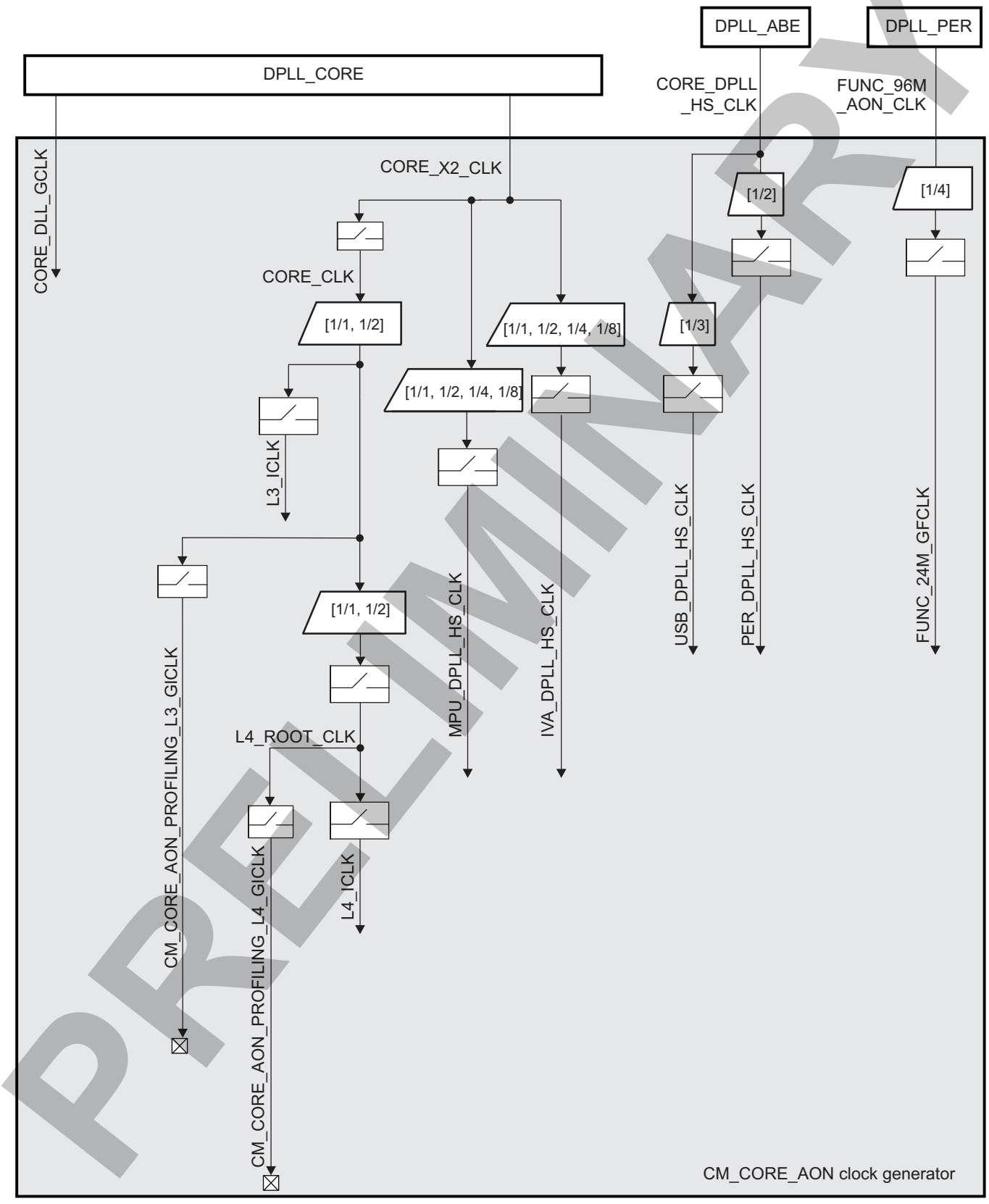

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Table 3-40 identifies controls for clock dividers or muxes in the CM_CORE_AON clock source.

Table 3-40. CM_CORE_AON Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Divider L3_ICLK	CM_CLKSEL_CORE[4] CLKSEL_L3
Divider L4_ROOT_CLK	CM_CLKSEL_CORE[8] CLKSEL_L4
Divider MPU_DPLL_HS_CLK	CM_BYPCLK_DPLL_MPU[1:0] CLKSEL
Divider IVA_DPLL_HS_CLK	CM_BYPCLK_DPLL_IVA[1:0] CLKSEL

NOTE: For clock signals control (gating/ungating management), see Section 3.1.1.1, *Clock Management*.

3.6.3.2.2 CKGEN_USB Clock Generator

CKGEN_USB receives a system clock from DPLL_USB. It provides a gated clock to CD_L3INIT.

Figure 3-35 shows the various functional and interface clocks generated by CKGEN_USB.

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Figure 3-35. CKGEN_USB Clock Manager Overview

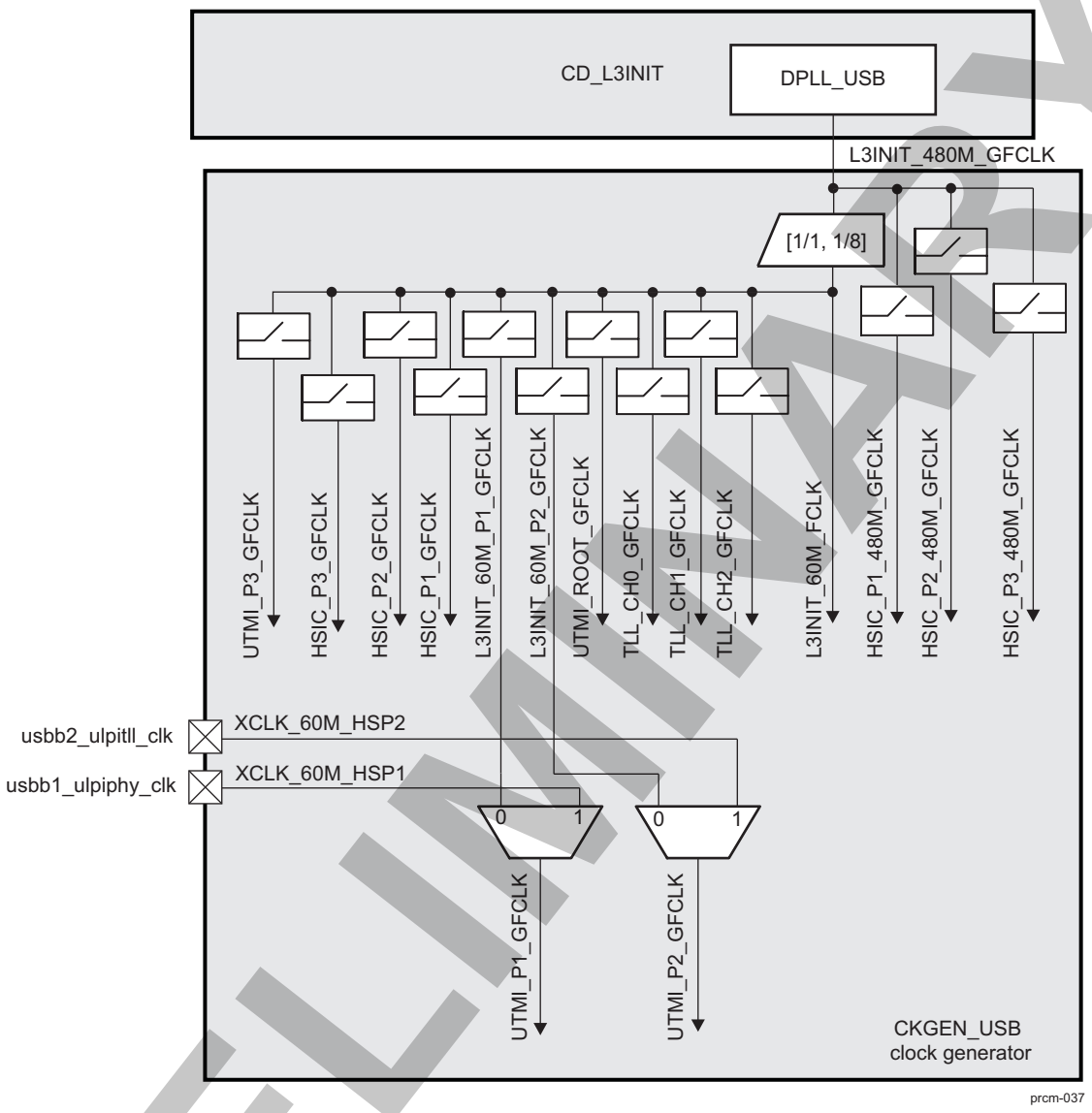

Table 3-41 identifies controls for clock dividers or muxes in the CKGEN_USB clock source.

Table 3-41. CKGEN_USB Clock Division and Muxing Control

Divider/Mux/Switch	Control Bit Field
Divider L3INIT_60M_FCLK	CM_CLKSEL_USB_60MHZ[0] CLKSEL
Mux UTMI_P1_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[24] CLKSEL_UTMI_P1
Mux UTMI_P2_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[25] CLKSEL_UTMI_P2
Switch HSIC_P1_480M_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[13] OPTFCLKEN_HSIC480M_P1_CLK
Switch HSIC_P2_480M_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[14] OPTFCLKEN_HSIC480M_P2_CLK
Switch HSIC_P3_480M_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[7] OPTFCLKEN_HSIC480M_P3_CLK
Switch HSIC_P1_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[11] OPTFCLKEN_HSIC60M_P1_CLK
Switch HSIC_P2_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[12] OPTFCLKEN_HSIC60M_P2_CLK

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Table 3-41. CKGEN_USB Clock Division and Muxing Control (continued)

Divider/Mux/Switch	Control Bit Field
Switch HSIC_P3_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[6] OPTFCLKEN_HSIC60M_P3_CLK
Switch UTMI_P1_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[8] OPTFCLKEN_UTMI_P1_CLK
Switch UTMI_P2_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[9] OPTFCLKEN_UTMI_P2_CLK
Switch UTMI_P3_GFCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[10] OPTFCLKEN_UTMI_P3_CLK

NOTE: For the clock status bits, see Table 3-130.

NOTE: For clock signals control (gating/ungating management), see Section 3.1.1.1, *Clock Management*.

NOTE: For information about the CKGEN_USB clock signals control and status, see Section 3.6.10, *CD_L3INIT Clock Domain*.

3.6.3.2.3 CKGEN_ABE Clock Generator

CKGEN_ABE receives a system clock from the PRM.

Figure 3-36 shows the various functional and interface clocks generated by the CKGEN_ABE clock source.

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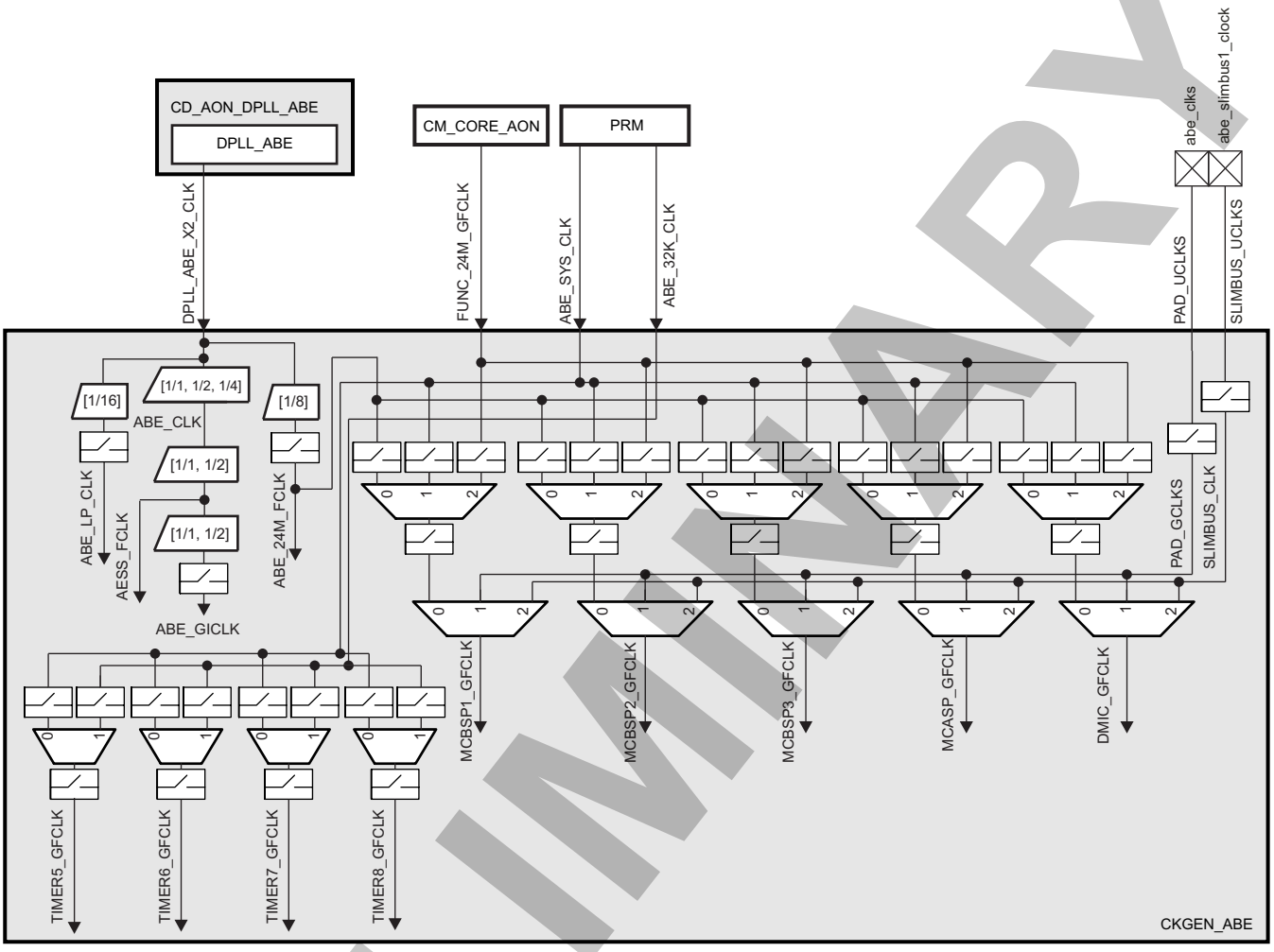
Figure 3-36. CKGEN_ABE Clock Manager Overview



prcm-038

Table 3-42 identifies the controls for clock dividers or muxes in CKGEN_ABE.

Table 3-42. CKGEN_ABE Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Clock switch PAD_GCLKS	CM_CLKSEL_ABE[8] PAD_CLKS_GATE
Clock switch SLIMBUS_CLK	CM_CLKSEL_ABE[10] SLIMBUS1_CLK_GATE
Divider ABE_CLK	CM_CLKSEL_ABE[1:0] CLKSEL_OPP
Divider AESS_FCLK and ABE_GICLK (1)	CM_ABE_AESS_CLKCTRL[24] CLKSEL_AESS_FCLK
Mux TIMER5_GFCLK	CM_ABE_TIMER5_CLKCTRL[24] CLKSEL
Mux TIMER6_GFCLK	CM_ABE_TIMER6_CLKCTRL[24] CLKSEL
Mux TIMER7_GFCLK	CM_ABE_TIMER7_CLKCTRL[24] CLKSEL
Mux TIMER8_GFCLK	CM_ABE_TIMER8_CLKCTRL[24] CLKSEL
Mux DMIC_GFCLK	CM_ABE_DMIC_CLKCTRL[25:24] CLKSEL_SOURCE
Mux DMIC internal functional clock	CM_ABE_DMIC_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE
Mux MCASP internal functional clock	CM_ABE_MCASP_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE
Mux MCASP_GFCLK	CM_ABE_MCASP_CLKCTRL[25:24] CLKSEL_SOURCE

(1) ABE_GICLK depends on the divider settings of AESS_GFCLK and is always divided by 2 of the ABE_CLK. Therefore, when the AESS_GFCLK divider is set to 1, the ABE_GICLK divider is set to 2, and vice versa.

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Table 3-42. CKGEN_ABE Clock Division and Muxing Control (continued)

Divider/Mux	Control Bit Field
Mux MCBSP1_GFCLK	CM_ABE_MCBSP1_CLKCTRL[25:24] CLKSEL_SOURCE
Mux MCBSP1 internal functional clock	CM_ABE_MCBSP1_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE
Mux MCBSP2_GFCLK	CM_ABE_MCBSP2_CLKCTRL[25:24] CLKSEL_SOURCE
Mux MCBSP2 internal functional clock	CM_ABE_MCBSP2_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE
Mux MCBSP3_GFCLK	CM_ABE_MCBSP3_CLKCTRL[25:24] CLKSEL_SOURCE
Mux MCBSP3 internal functional clock	CM_ABE_MCBSP3_CLKCTRL[27:26] CLKSEL_INTERNAL_SOURCE

NOTE: For the ABE subsystem, functional clock DPLL_ABE_X2_CLK must be set to 196.608 MHz in DPLL_ABE. ABE_CLK, which is sourced by the DPLL_ABE_X2_CLK, can be configured in the CM_CLKSEL_ABE[1:0] CLKSEL_OPP bit field according to the OPP. AESS_FCLK can be the same as ABE_CLK or ABE_CLK divided by 2, depending on the CM_ABE_AESS_CLKCTRL[24] CLKSEL_AESS_FCLK bit. For more information about setting DPLL parameters, see Section 3.6.3.3.1, *DPLLs Output Clocks Parameters*.

NOTE: For clock signals control (gating/ungating management), see Section 3.1.1.1, *Clock Management*.

NOTE: For information about the CKGEN_ABE clock signals control and status, see Section 3.6.23, *CD_ABE Clock Domain*.

3.6.3.2.4 CKGEN_ISS Clock Generator

CKGEN_ISS receives clock signals from DPLL_CORE. It provides gated clock signals to CD_CAM and CD_IPU clock domains.

Figure 3-37 shows the various functional and interface clocks generated by CKGEN_ISS.

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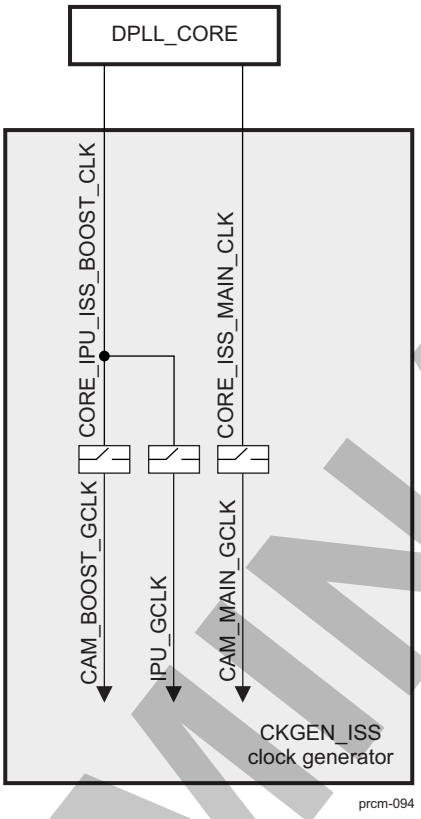
Figure 3-37. CKGEN_ISS Clock Manager Overview



NOTE: For clock signals control (gating/ungating management), see Section 3.1.1.1, *Clock Management*.

NOTE: For information about the CKGEN_ISS clock signals control and status, see Section 3.6.20, *CD_IPU Clock Domain*, and Section 3.6.22, *CD_CAM Clock Domain*.

3.6.3.2.5 CM_CORE Clock Generator

The CM_CORE module is in the CORE power domain. Its clock generation part generates the clock sources for all peripherals and modules besides those generated by CM_CORE_AON. It generates several functional clocks (12, 24, 48, 96, 128, 192 and 256 MHz) that feed all its peripherals and modules besides containing clock control, muxes, gating, etc. for other power domains. These clocks are constant through OPP. CM_CORE also provides a gated clock to DPLL_PER and its associated HSDivider, DPLL_USB.

GPU_SYS_CLK can be a divide by 1 or a devide by 2 version of L3 clock. This divide ration is controlled with CM_GPU_GPU_CLKCTRL[26] CLKSEL_GPU_SYS_CLK bit.

Figure 3-38 and Figure 3-39 show the various functional and interface clocks generated by CM_CORE.

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Figure 3-38. CM_CORE Overview (a)

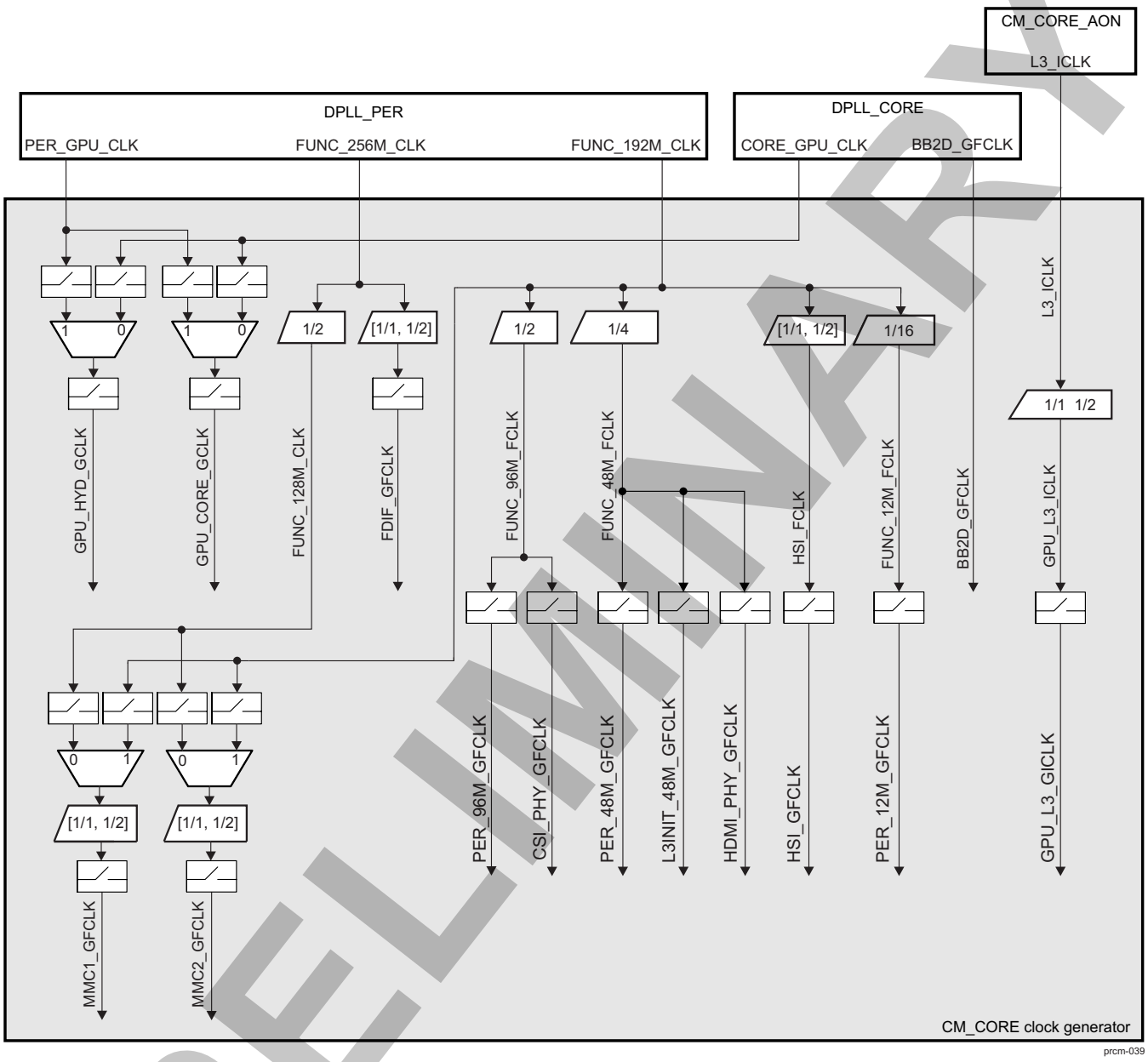

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Figure 3-39. CM_CORE Overview (b)

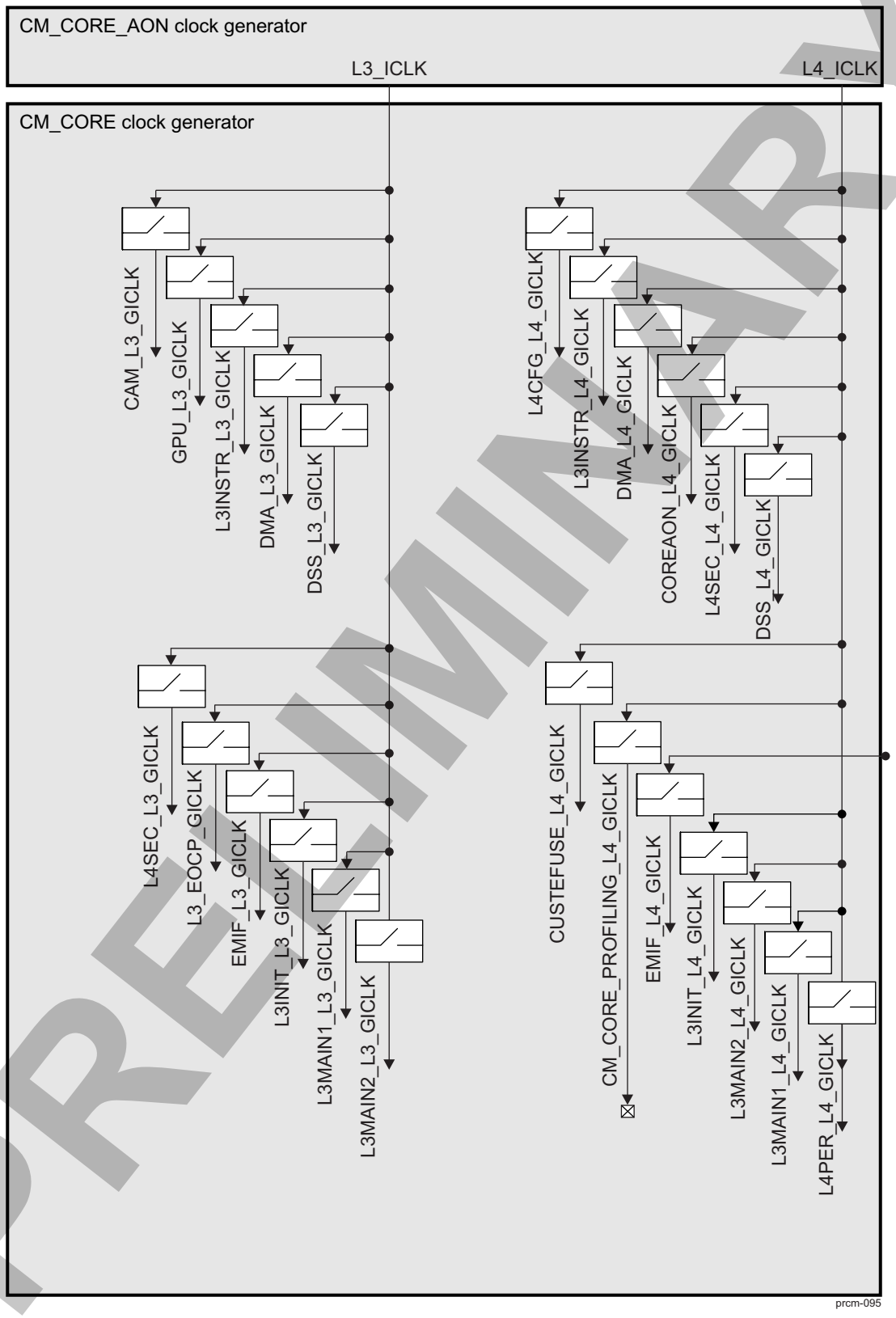

Table 3-43 identifies controls for clock dividers or muxes in the CM_CORE clock source.

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Table 3-43. CM_CORE Clock Division and Muxing Control

Divider/Mux/Switch	Control Bit Field
Divider FDIF_GFCLK	CM_CAM_FDIF_CLKCTRL[24] CLKSEL_FCLK
Divider HSI_GFCLK	CM_L3INIT_HSI_CLKCTRL[24] CLKSEL
Mux MMC1_GFCLK	CM_L3INIT_MMC1_CLKCTRL[24] CLKSEL_SOURCE
Divider MMC1_GFCLK	CM_L3INIT_MMC1_CLKCTRL[25] CLKSEL_DIV
Mux MMC2_GFCLK	CM_L3INIT_MMC2_CLKCTRL[24] CLKSEL_SOURCE
Divider MMC2_GFCLK	CM_L3INIT_MMC2_CLKCTRL[25] CLKSEL_DIV
Mux GPU_HYD_GCLK	CM_GPU_GPU_CLKCTRL[25] CLKSEL_GPU_HYD_GCLK
Mux GPU_CORE_GCLK	CM_GPU_GPU_CLKCTRL[24] CLKSEL_GPU_CORE_GCLK
Divider GPU_L3_GICLK	CM_GPU_GPU_CLKCTRL[26] CLKSEL_GPU_SYS_CLK
Switch FUNC_48M_FCLK	CM_L3INIT_USB_HOST_HS_CLKCTRL[15] OPTFCLKEN_FUNC48M_CLK

NOTE: For clock signals control (gating/ungating management), see Section 3.1.1.1, *Clock Management*.

3.6.3.3 Generic DPLL Overview

To generate high-frequency clocks, the device supports multiple on-chip DPLLs controlled directly by the PRCM module. They are of two types: type A and type B DPLLs.

The following DPLLs belong to type A:

- DPLL_MPU
- DPLL_IVA
- DPLL_CORE
- DPLL_PER
- DPLL_ABE

The following DPLLs belong to type B:

- DPLL_USB

All DPLLs (type A and type B) support the features described in the following sections, unless otherwise identified.

NOTE: This chapter discusses only the DPLLs that are directly controlled by the PRCM module. The other DPLLs embedded in and managed by other subsystems are described in their respective subsystems. For example, Section 10.3.4.5, *DSI PLL Controllers,* in Chapter 10, *Display Subsystem*, discusses the DPLLs in the display subsystem.

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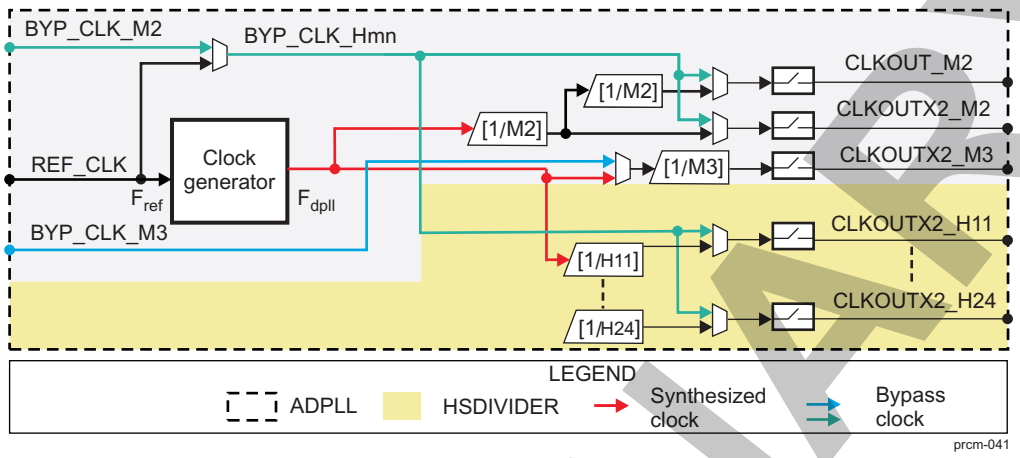
3.6.3.3.1 DPLLs Output Clocks Parameters

Figure 3-40 shows the functional architecture of a generic DPLL.

Figure 3-40. Generic DPLL Functional Diagram



The DPLL has three input clocks:

- REF_CLK: Used to generate the synthesized clock but can also be used as the bypass clock for some outputs of the DPLL whenever the DPLL enters bypass mode. It is mandatory for the DPLL clock synthesis.
- BYP_CLK_M2: Selectable bypass clock for the output of an M2 post-divider (optional)
- BYP_CLK_M3: Selectable bypass clock for the output of an M3 post-divider (optional)

The DPLL provides the bypass clock used by HSDIVIDER: BYP_CLK_Hmn, which is output by the multiplexer between the BYP_CLK_M2 and REF_CLK clock signals.

NOTE: The [1/2] divider located after the M2 post-divider is not valid when the CM_CLKSEL_DPLL_MPU[22] DCC_EN bit is set (applies only to DPLL_MPU when a frequency higher than 1.4 GHz is needed).

The DPLL can be programmed to be locked at any frequency given by one of the following equations:

- $F_{dpll} = F_{ref} \times 2 \times M / (N + 1)$
- $F_{dpll} = F_{ref} \times 2 \times (4 \times M / (N + 1))$ in case the CM_CLKMODE_DPLL_ABE[11] DPLL_REGM4XEN bit is set (applies only to DPLL_ABE)
- $F_{dpll} = F_{ref} \times (M / (N + 1))$ in case the CM_CLKSEL_DPLL_MPU[22] DCC_EN bit is set (applies only to DPLL_MPU when frequency higher than 1.4GHz is needed).

Where:

- F_{dpll} is the DPLL lock frequency.
- F_{ref} is the REF_CLK frequency. F_{ref} is also known as CLKINP.
- M is the software-configured multiplication ratio binary value.
- N is the software-configured division ratio binary value.

NOTE: It is preferred to minimize the value for N parameter (it minimizes lock time and jitter). Then M should be chosen to provide correct frequency (with lowest delta as possible).

It internally generates three main clocks: CLKOUT_M2, CLKOUTX2_M2, and CLKOUTX2_M3 as shown in Table 3-44.

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Table 3-44. CLKOUT_M2, CLKOUTX2_M2, and CLKOUTX2_M3 Frequencies With DPLL State

Output	Equation	DPLL Mode
CLKOUT_M2	F_{dpll} / (2 x M2)	Locked (typical case)
	F_{ref} or BYP_CLK_M2	Before lock or during relock
	F_{dpll} / M2	DC corrector logic is used (DCC_EN bit is set).
CLKOUTX2_M2	F_{dpll} / M2	Locked (typical case)
	F_{ref} or BYP_CLK_M2	Before lock or during relock
	F_{dpll} / M2	DC corrector logic is used (DCC_EN bit is set).
CLKOUTX2_M3	F_{dpll} / M3 or BYP_CLK_M3/M3	Locked (typical case)
	0	Before lock or during relock
	F_{dpll} / M3 or BYP_CLK_M3/M3	DC corrector logic is used (DCC_EN bit is set).

Where:

- M2 is the software-configured division ratio binary value.
- M3 is the software-configured division ratio binary value.
- CLKOUT_M2 and CLKOUTX2_M2 bypass clock input can be switched when the DPLL is not in locked state by using the M2 bypass clock select control bit.
- CLKOUTX2_M3 output clock can be switched when the DPLL is in locked state by using the M3 clock select control bit.

NOTE:

- A value of 0 for M2 and M3 division ratios is not allowed. They are set to 1 after reset.
- CLKOUT_M2 is generated based on a fixed divide-by-2 ratio, except in bypass mode.

The DPLL can contain one or two HSDIVIDER modules to produce more clocks with divided ratio based on the DPLL synthesized clock frequency. HSDIVIDER1 provides four extra post-dividers from H11 to H14 (the output clocks are CLKOUTX2_H11 through CLKOUTX2_H14). HSDIVIDER2 provides four extra post-dividers from H21 through H24 (the output clocks are CLKOUTX2_H21 through CLKOUTX2_H24). The HSDIVIDER output clock frequency is given by the equations in Table 3-45.

Table 3-45. CLKOUTX2_Hmn Frequencies With DPLL State

Equation	DPLL Mode
CLKOUTX2_Hmn = F_{dpll} /(Hmn + 1)	Locked
CLKOUTX2_Hmn = BYP_CLK_Hmn	Before lock or during relock

Where:

- F_{dpll} is the DPLL lock frequency.
- (Hmn + 1) is the software-configured division ratio binary value.
- n is in the range from 1 to 4.
- m is equal to 1 or 2.

NOTE: Hmn + 1 division ratio is set to 1 after reset. 63 (0x3f) is an illegal value.

All clock outputs of the DPLL can be gated. The PRCM module provides the DPLL with a clock-gating control signal to enable or disable the clock. DPLL provides the PRCM module with a clock activity status signal to let the PRCM module hardware know when the clock is effectively running or effectively gated. The PRCM module provides a CM_IDLEST_DPLL_dpll_name[0] ST_DPLL_CLK status bit, which indicates the lock state or nonlock state of the DPLL.

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The type B DPLL (DPLL_USB) has two outputs: CLKOUT and CLKDCOLDO. The DPLL can be programmed to be locked with the output clock frequencies given by the following equation:

- $F_{clkout} = F_{ref} \times (M / (N + 1)) \times (1 / M2)$
- $F_{clkdcoldo} = F_{ref} \times (M / (N + 1))$

Where:

- F_{clkout} is the frequency of the clock at output CLKOUT.
- $F_{clkdcoldo}$ is the frequency of the clock at output CLKDCOLDO.
- F_{ref} is the REF_CLK frequency.
- M is the software-configured multiplication ratio binary value.
- N is the software-configured division ratio binary value.
- M2 is the software-configured division ratio binary value.

CLKOUT supports the same bypass modes as previously identified. CLKDCOLDO does not support bypass mode.

The type B DPLL output clock is synthesized by an internal oscillator that is phase-locked to the REF_CLK. Two oscillators are built within a type B DPLL. The oscillators are user-selectable based on the synthesized output clock frequency requirement. If the required frequency is greater than or equal to 1500 MHz, the user must program a value of 1 in the CM_CLKSEL_DPLL_dpll_name[21] DPLL_SELFREQDCO bit. This drives a value of 100 on the SELFREQDCO input of the corresponding type B DPLL. If the required frequency is less than 1500 MHz, the user must program a value of 0 in the CM_CLKSEL_DPLL_dpll_name[21] DPLL_SELFREQDCO bit. This drives a value of 010 on the SELFREQDCO input of the corresponding type B DPLL.

3.6.3.3.2 Enable Control, Status, and Low-Power Operation Mode

The DPLL has a manual mode control bit field, which allows the setting of the different operating modes of the DPLL. When the DPLL is switched to lock mode, the current values of the multiplication ratio (M) and the division ratio (N) are latched in the DPLL. The DPLL then starts the lock or relock sequence to synthesize the corresponding output frequency clock.

The status of the synthesized clock output of the DPLL is represented by the CLKOUT status bit. It can be gated or active.

The type A DPLLs can be switched to low-power operation mode (also called LPMODE) to optimize DPLL power consumption when the input and output clock frequencies are low. This mode can be software-enabled using the low-power mode control bit of the DPLL.

It must be enabled only if both of the following operating conditions are satisfied:

- $F_{ref} / (N + 1)$ is less than or equal to 1 MHz.
- $F_{ref} \times M / (N + 1)$ is less than or equal to 100 MHz.

Where:

- F_{ref} is the REF_CLK frequency.
- M is the software-configured multiplication ratio binary value.
- N is the software-configured division ratio binary value.

3.6.3.3.3 DPLL Power Modes

DPLL supports several power modes for type A and only one power mode for type B. Each mode results in a tradeoff between power savings and relock time. The PRCM module allows only a few modes for each DPLL, depending on the use of the DPLL.

Table 3-46 lists the DPLL power modes.

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Table 3-46. DPLL Power Modes

Power Mode	CLKOUT State	Logic Current (mA)	Analog Current (mA)	Freq Lock Time	Phase Lock Time
Low-power stop	Clock stopped	0.065 (leakage)	0.009 (leakage)	2.5 µs + (70 × (N+1) / F_{ref})	2.5 µs + (120 × (N+1) / F_{ref})
Fast-relock stop	Clock stopped	0.065 (leakage)	0.009 (leakage)	2.5 µs + (70 × (N+1) / F_{ref})	2.5 µs + (120 × (N+1) / F_{ref})
Low-power bypass	Bypass clock/clock stopped	0.065 (leakage)	0.009 (leakage)	2.5 µs + (70 × (N+1) / F_{ref})	2.5 µs + (120 × (N+1) / F_{ref})
Fast-relock bypass	Bypass clock/clock stopped	0.065 (leakage)	0.5 (leakage)	0.05 µs + (70 × (N+1) / F_{ref})	0.05 µs + (120 × (N+1) / F_{ref})
Lock	Synthesized clock	0.95 (active)	3 (active)	N/A	N/A

Where:

- F_{ref} is the REF_CLK frequency.

A DPLL power mode can be achieved on a software request (manual) and/or automatically (automatic), depending on the specific hardware conditions.

A DPLL can switch from one mode to another as a result of the following:

- Software-programmed transition (manual): Software configures the dedicated DPLL manual mode control feature for the next desired DPLL mode. It must ensure that the transition can be performed based on the clock activity on the device.
- Combined software-programmed and hardware-conditions-based transition (auto): This mode allows the DPLL to automatically transition to a low-power state (that is, any state other than the LOCK state) when the output clocks are gated or the destination clock domain is inactive, and to switch back to the LOCK state when the output clock is needed (that is, the clock is ungated or the clock domain becomes active). The desired low-power state for the automatic transition is configured in the dedicated Auto Mode Control parameter of the DPLL.

NOTE: With T_{ref} = 1 / F_{ref} = (N + 1) / CLKINP; (Fref = CLKINP / (N + 1)):

$T_{ref}$is the REF_CLK period.

This formula indicates that a smaller N divider value provides a smaller time for switching the clock after an M2 post-divider change.

A compromise is necessary between the clock switching latency and power consumption. Having a smaller N value:

- Requires a higher M2 post-divider value to obtain the same target frequency.
- Results in a higher DPLL lock frequency, and then higher power consumption.

NOTE:

- A manual transition can be performed from any power mode to any other power mode.
- An automatic transition can be performed from lock mode to any low-power mode.

NOTE: When the DPLL is in Low-power bypass mode, Auto-idle mode is disabled and no clock is requested, the DPLL makes a transition to Low-power stop mode. Thus the device can switch off even if the DPLL is set to Low-power bypass mode.

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3.6.3.3.4 DPLL Recalibration

The DPLL recalibration applies only to type-A DPLLs. Each time the DPLL is reset or performs a lock sequence (following a change in the value of multiplier M or divider N), it performs a recalibration of the output frequency, based on voltage and temperature conditions. In lock mode, the DPLL maintains a steady lock frequency output by compensating for voltage and temperature changes within a certain range. However, if the voltage or temperature drifts outside the range or shows a significant or fast change, the DPLL may not be able to track and compensate it. It would need a recalibration, which is signaled by assertion of a recalibration flag.

NOTE:

- The recalibration mechanism is active only while the DPLL is in lock mode. When the DPLL is in off or bypass mode (low-power or fast-relock), it does not assert the recalibration flag.
- If the DPLL drifts out of the operating range limits while not locked, and then when it tries to relock, it fails to lock within the normal delay and recalibrates automatically before eventually locking. The only difference between this case and a standard relock is the recalibration delay.

During recalibration, the DPLL loses lock and output clock switches to the bypass clock.

The DPLL can automatically start recalibration when the recalibration flag is asserted, or recalibration can be triggered by software control. The trigger setting of the recalibration can be configured by the corresponding registers of the DPLL in the PRCM module. The software-controlled recalibration mode is selected by default.

Software-controlled recalibration: The DPLL continues its tracking mechanism as long as the recalibration is not triggered by software (that is, by enabling the recalibration-enable control parameter). If the DPLL reaches upper or lower bounds of the DCO control code and software has still not triggered recalibration, the DPLL stops its tracking mechanism. The output clock remains active, but frequency and jitter are not ensured to meet the requirement.

Automatic recalibration: The DPLL immediately starts the recalibration as soon as the recalibration flag is asserted.

NOTE: Automatic recalibration of the DPLL can start at any time. While relocking, the DPLL switches to bypass mode, which introduces a frequency change. For modules that are sensitive to frequency change while operating, this can introduce operational instability. For example, the external memory EMIF controller is sensitive to a frequency change on the DPLL because its embedded DLL relocks on a frequency change. Any EMIF access during this DLL relock period can be corrupted. It is, therefore, important to stall EMIF access during DPLL recalibration.

To allow software to recalibrate the DPLL at the correct time depending on the device activity, the PRCM module can generate a wake-up event on the processor power domain, followed by an interrupt on the processor subsystem when the DPLL recalibration flag is asserted.

Table 3-47 lists the DPLL recalibration and control parameters.

Table 3-47. DPLL Recalibration Control Parameters

Parameter	Register	Description
Recalibration-enable control	CM_CLKMODE_DPLL_<module>[8] DPLL_DRIFTGUARD_EN	Enable/disable the DPLL automatic recalibration feature.
Recalibration-interrupt mask control	PRM_IRQENABLE_MPU PRM_IRQENABLE_IPU PRM_IRQENABLE_DSP	Mask/unmask the DPLL recalibration interrupt to processor.
Recalibration-interrupt status	PRM_IRQSTATUS_MPU PRM_IRQSTATUS_IPU PRM_IRQSTATUS_DSP	Status of the DPLL recalibration interrupt to processor

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3.6.3.3.5 DPLL Spread Spectrum Clocking

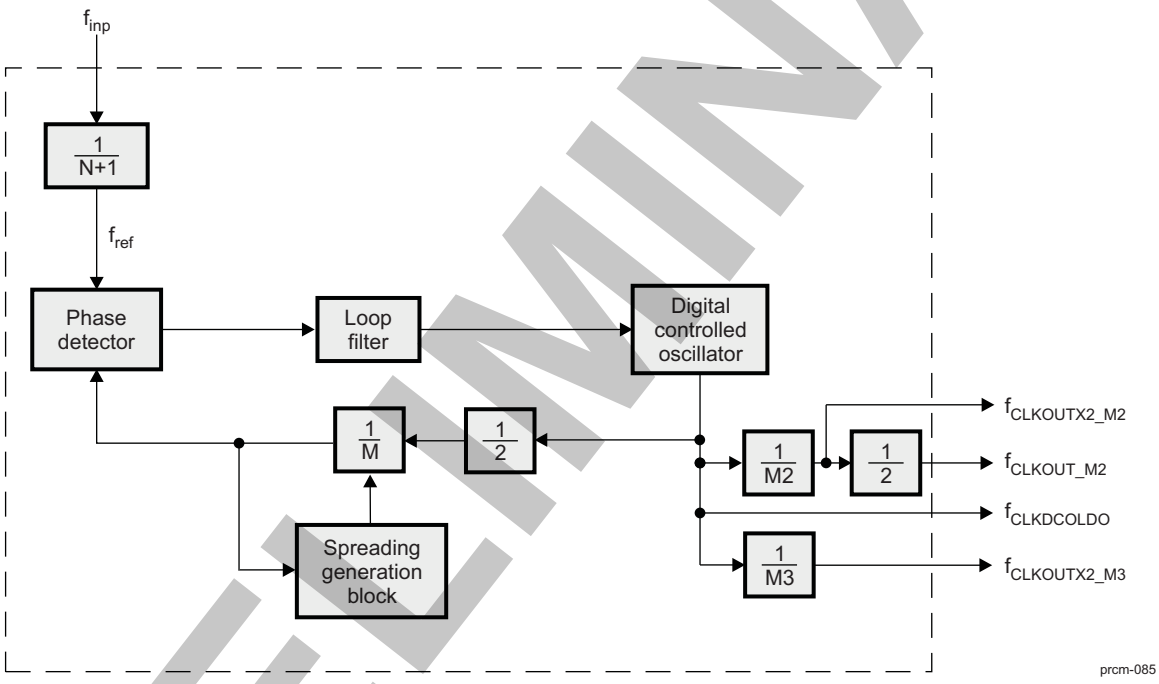
The synthesized clock output of the DPLL has a stable frequency. This periodicity generates a significant power peak at the selected frequency, which in turn causes an electromagnetic interference (EMI) disturbance to the environment. In communication devices, this clock signal generates unwanted spurious signals that interfere with the decoding of information received. It results in performance degradation; for example, in the form of high bit-error rates in case of a wireless communication interface.

To reduce the power peaks (and the electromagnetic noise generated at a specific frequency), an internal frequency modulation of the DPLL is used to distribute the energy to many different frequencies, thereby reducing the power peaks. This is called spread spectrum clocking (SSC). DPLL supports triangular SSC.

SSC in the DPLL is performed by changing the feedback divider (M) in a triangular pattern. This varies the frequency of the output clock in a triangular pattern. The frequency of this pattern is the modulation frequency (fm). It is programmed as a ratio of the REF_CLK/4. This frequency modulation feature is directly integrated into some DPLLs of the device.

shows a diagram of a type A DPLL that supports the SSC feature with DC correction logic disable.

Figure 3-41. Type A DPLL With SSC Reduction Feature and DC correction logic disable



shows a diagram of the DPLL_MPU that supports the SSC feature with DC correction logic enable.

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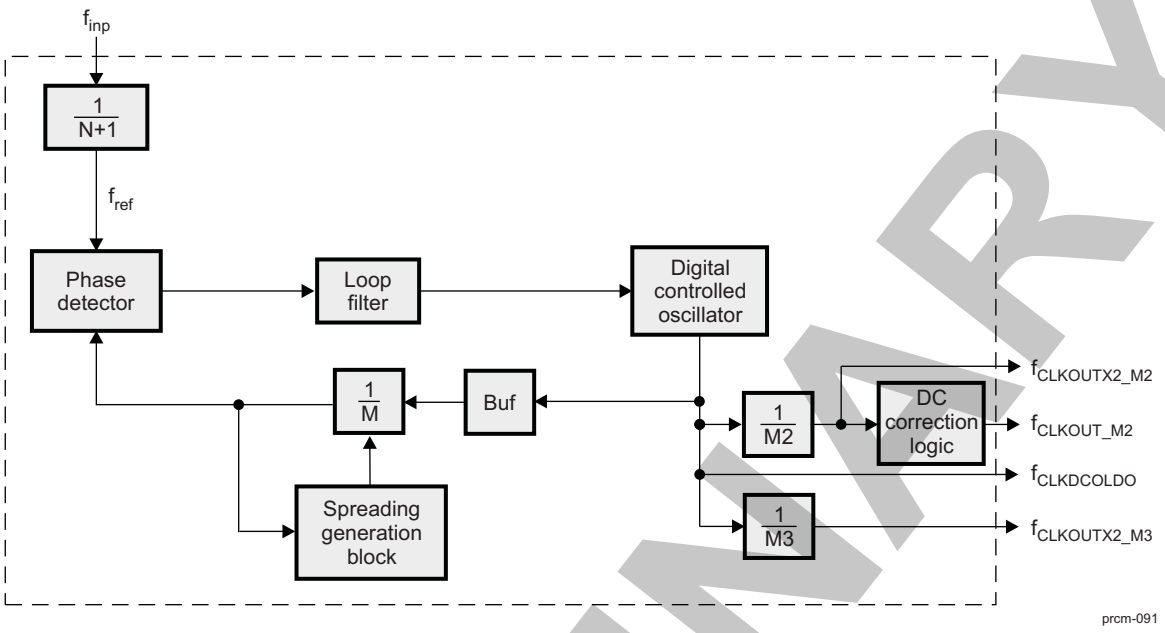
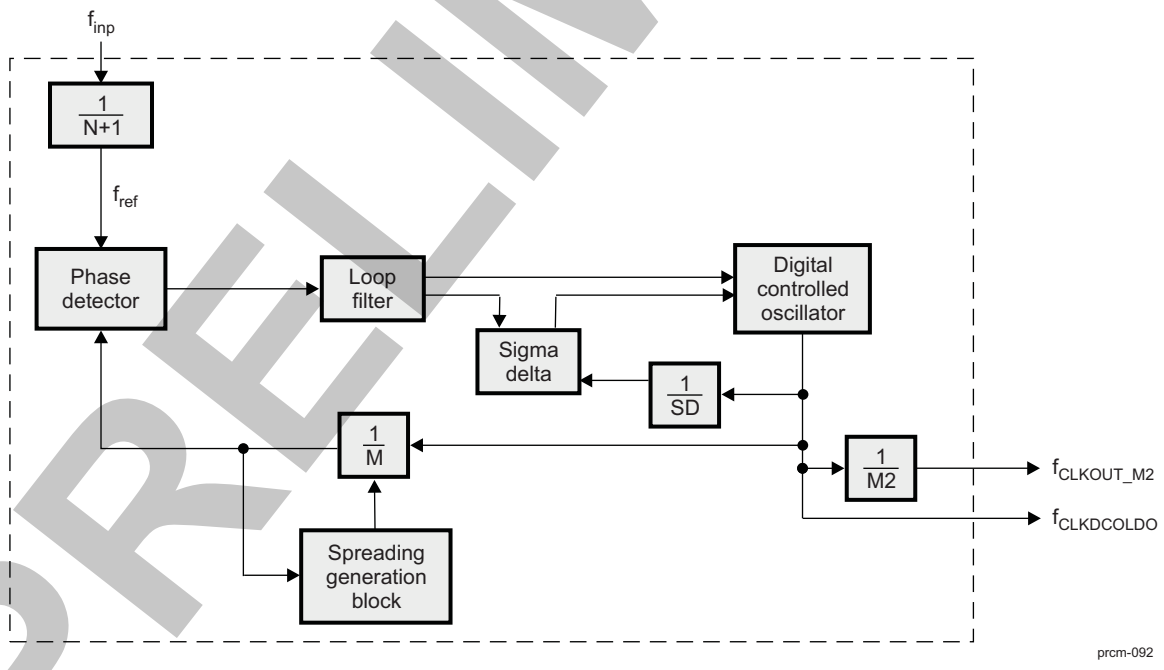
Figure 3-42. DPLL_MPU With SSC Reduction Feature and DC correction logic enable



NOTE: The M2 post divider value should be set to 0x1 before enabling DC correction logic.

shows a diagram of a type B DPLL that supports the SSC feature.

Figure 3-43. Type B DPLL With SSC Reduction Feature



shows a diagram of the spreading generation block.

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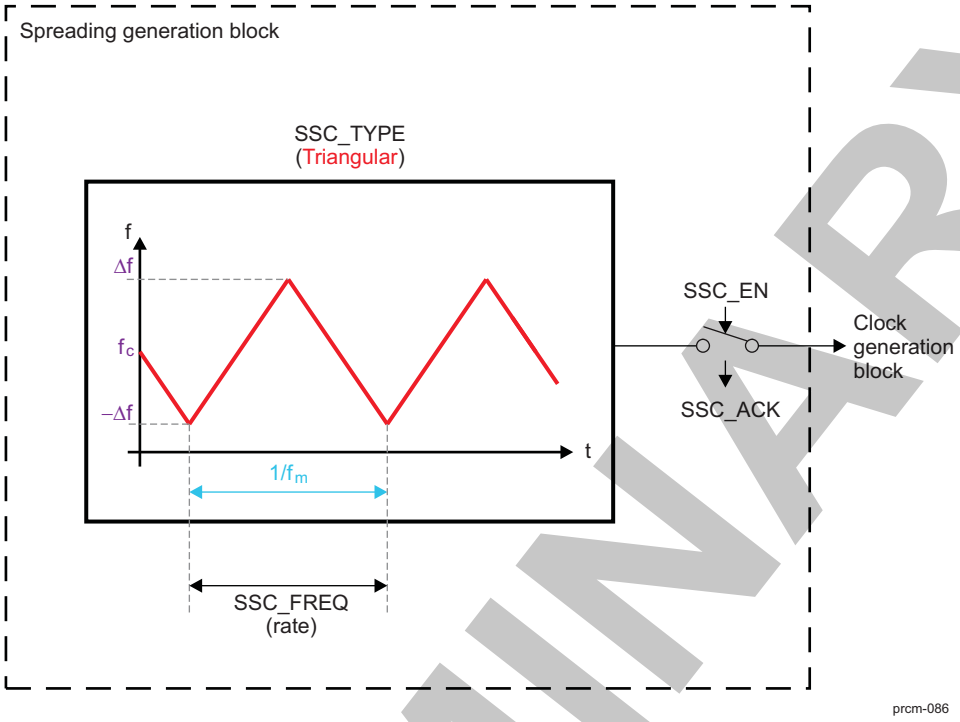
Figure 3-44. Spreading Generation Block Diagram



NOTE: Δf is the deviation from the center frequency. The total spreading deviation is equal to twice Δf. The peak (ΔM) or the amplitude of the triangular/square pattern as a percent of M would be equal to the percent of the frequency spread (Δf), $\Delta M/M = \Delta f/f_c$.

f_c is the original output clock frequency.

f_m is the spreading frequency.

This additional block generates the required waveform used to reduce EMI. This waveform is then modulated with the initial signal to add some controlled deviation to the clock signal frequency, which spreads the energy of the clock and its harmonics into a band of frequencies, and then reduces EMI. SSC_DOWNSPREAD can control the position of the generated signal. It is controlled by the CM_CLKMODE_DPLL_<module>[14] DPLL_SSC_DOWNSPREAD bit of the corresponding registers (where <module> is the name of the concerned DPLLs). If the DOWNSPREAD bit is set to 1, the frequency spread on the lower side is twice the programmed value. The frequency spread on the higher side is 0.

The value of SSC_FREQ controls the rate of the generated signal. It can be programmed as a ratio of the reference clock: $f_{ref}/4$. The value that must be programmed is calculated as follows:
$ModFreqDivider = f_{ref}/(4 \times f_m)$, where $f_m < f_{ref}/70$, $f_{ref} = f_{inp}/(1+N)$, and f_{inp} is the input clock for the DPLL.
The ModFreqDivider is split into mantissa and exponent: $ModFreqDivider = Mantissa \times 2^{Exponent}$
The same value of ModFreqDivider can be obtained by different combinations of mantissa and exponent values. However, it is recommended to set the target ModFreqDivider by programming a maximum mantissa and a minimum exponent. This is controlled by the CM_SSC_MODFREQDIV_DPLL_<module>[10:8] MODFREQDIV_EXPONENT and CM_SSC_MODFREQDIV_DPLL_<module>[6:0] MODFREQDIV_MANTISSA bit fields of the corresponding registers (where <module> is the name of the concerned DPLL).
To define the modulation-frequency divider step size (ΔM) for triangular SSC, a DeltaMStep parameter must be programmed. DeltaMStep is split into integer and fractional parts. The step size can be calculated as follows:
$\Delta M = ModFreqDivider \times DeltaMStep$, if Exponent ≤3
$\Delta M = 8 \times Mantissa \times DeltaMStep$, if Exponent > 3

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It is controlled by the CM_SSC_DELTAMSTEP_DPLL_<module>[19:0] DELTAMSTEP bit field of the corresponding register (where <module> is the name of the concerned DPLL). The CM_SSC_DELTAMSTEP_DPLL_<module>[19:18] bit field defines the integer part, while the CM_SSC_DELTAMSTEP_DPLL_<module>[17:0] bit field defines the fractional part.
The SSC_EN signal enables and disables the frequency modulation feature of the DPLL. It is controlled by the CM_CLKMODE_DPLL_<module>[12] DPLL_SSC_EN bit of the corresponding registers (where <module> is the name of the concerned DPLL).
The SSC_ACK signal notifies of the exact start and SSC end of the DPLL. It can be read by the CM_CLKMODE_DPLL_<module>[13] DPLL_SSC_ACK bit of the corresponding registers (where <module> is the name of the concerned DPLL).
The following restriction applies to the range of M values: M – ΔM should be ≥ 20. Also, M+ΔM should be ≤ 2045. If DOWNSPREAD is enabled, M – 2 × ΔM should be ≥ 20, and M ≤ 2045. In any case, the frequency modulation is programmed and it is not generally something that must be changed in real time.

describes the DPLL SSC control parameters.

Table 3-48. DPLL SSC Control Parameters

Parameter	Register	Description
SSC enable control	CM_CLKMODE_DPLL_<module>[12] DPLL_SSC_EN	Enable/disable the DPLL SSC feature. When set to disable, SSC is disabled only after completion of one full cycle of the modulation pattern to maintain the average frequency.
SSC acknowledge	CM_CLKMODE_DPLL_<module>[13] DPLL_SSC_ACK	Notifies the exact start and end of SSC
Modulation frequency divider setting (Mantissa and Exponent)	CM_SSC_MODFREQDIV_DPLL_<module>[6:0] MODFREQDIV_MANTISSA CM_SSC_MODFREEQDIV_DPLL_<module>[10:8] MODFREQDIV_EXPONENT	Set the ratio of the modulation frequency with respect to the REF_CLK/4 frequency.
M step size setting (DeltaMStepInteger and DeltaMStepFraction)	CM_SSC_DELTAMSTEP_DPLL_<module>[19:0] DELTAMSTEP	Set the feedback divider variation step-size.

3.6.3.3.5.1 Definition

The aim of the SSC is to add a variation to the frequency of an original clock, which spreads the generated interference over a larger band of frequencies.
In theory, SSC means that the clock signal is varied around the desired frequency. For example, for a 1 GHz clock, the frequency might be 999.5 MHz at one time and 1.0005 GHz at another. Doing this constantly causes the power of the tone to be spread out more over a broader band of tight frequencies (centered at the desired tone). To realize this constant variation on the original signal, a modulation with an additional signal (called spreading waveform) is realized.
Creating an SSC by spreading the initial clock frequency is done by defining the following parameters:

- The spreading frequency (deviation), which is the ratio of the range of spreading frequency over the original clock frequency
- The modulation rate (f_m), which is used to determine the clock-frequency spreading-cycling rate, and is the time during which the generated clock frequency varies through f and returns to the original frequency
- The modulation waveform, which describes the variation curve over time The spectral power reduction in the DPLL clocks is dependent on the modulation index (K), which is a ratio of spreading frequency, calculated from the frequency deviation (f) and the modulation rate (f_m).

3.6.3.3.5.2 Modulation Waveforms

The shape (profile) of the generated clock signal depends on the modulation waveform that is used during the frequency modulation. Several profiles can be used, according to the desired shaping for the energy spreading.

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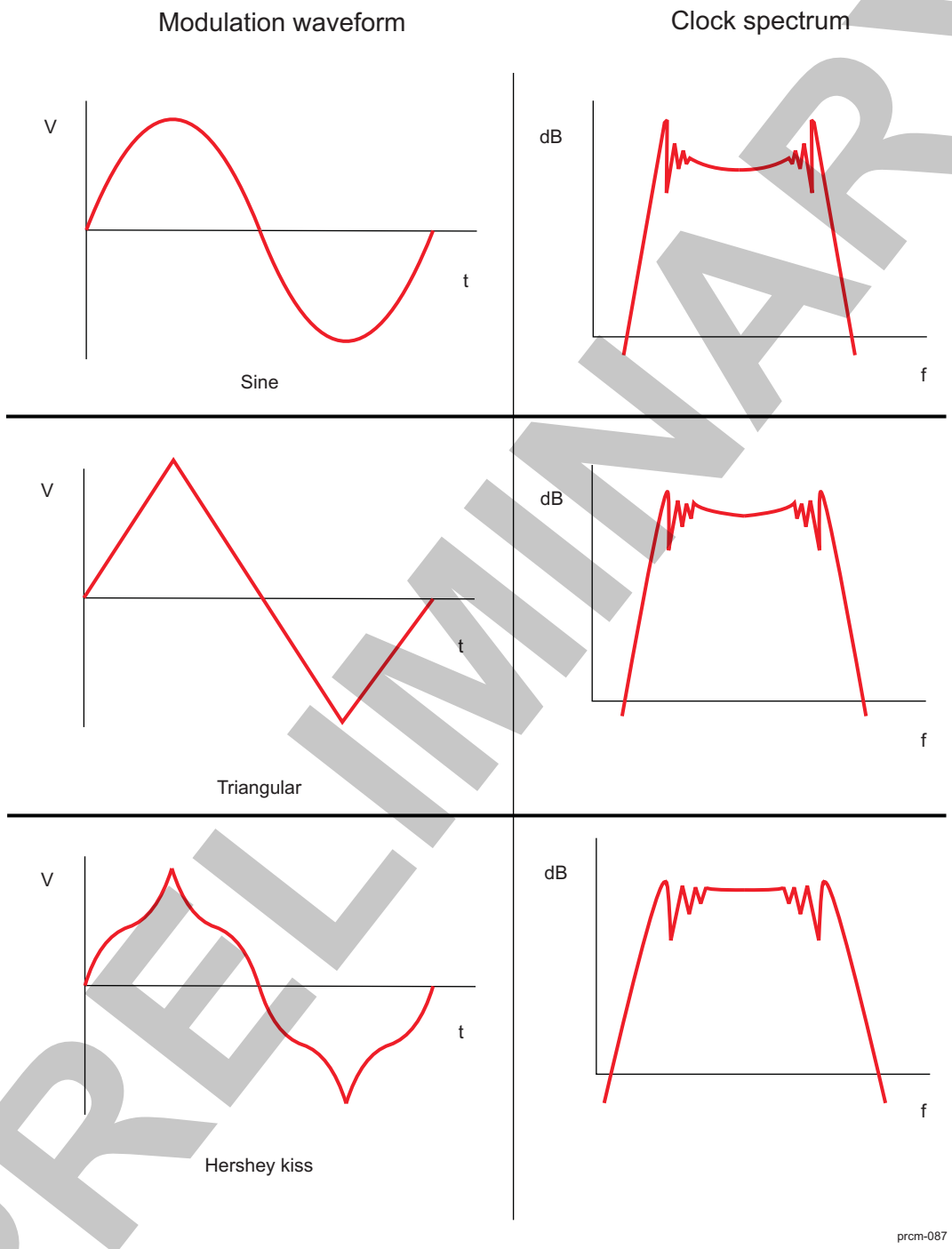
shows three examples of modulation waveforms and the spectrum of the corresponding modulated clock signal.

Figure 3-45. Modulation Profiles



The triangular wave gives a relatively flat spectrum and is also easy to generate.

3.6.3.3.5.3 Effects on the Clock Signal

shows an example of the effect of triangular spreading on a clock signal.

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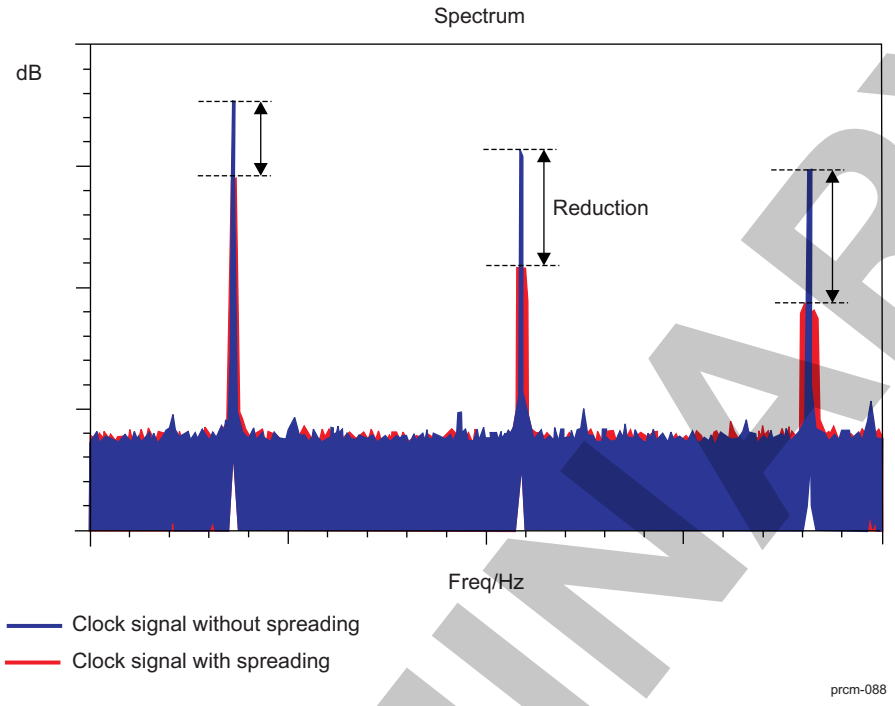
Figure 3-46. Effect of the SSC in Frequency

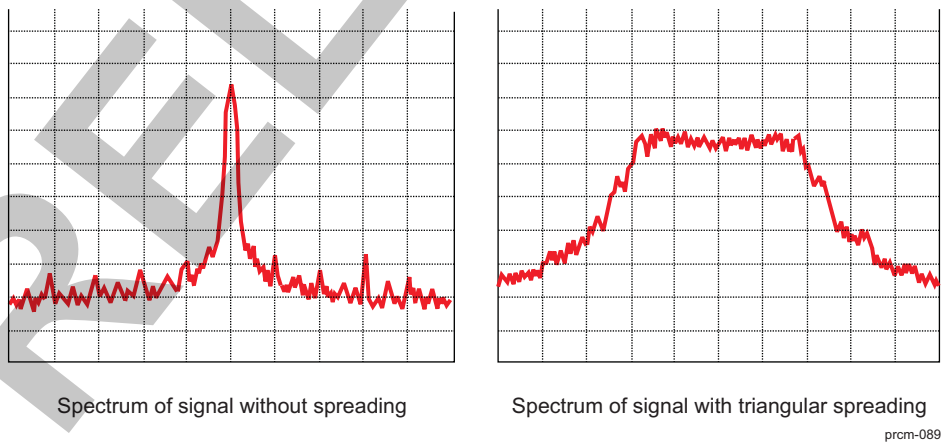


highlights the power reduction of the main peak, but also the flatter aspect of the modulated signal. Notice that the minimum level of the second signal is higher than the first one. This effect is normal and is due to the noise added for the modulation.

NOTE: The spreading technique scatters the energy of the peaks on the other frequencies, which reduces the power of the peaks but increases the global noise of the signal.

shows the effect of triangular spreading on a clock signal in the time domain.

Figure 3-47. Effect of the SSC in the Time Domain



3.6.3.3.5.4 Estimation of the EMI Reduction Level

shows the effect of spreading on a clock and its harmonics.

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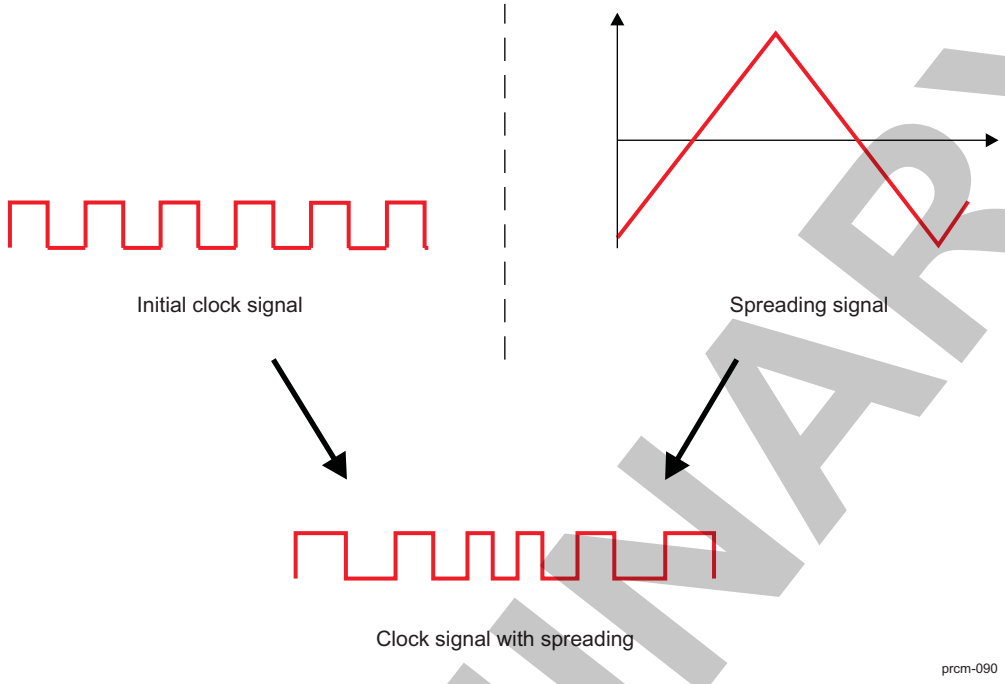
Figure 3-48. Peaks Reduction Due to Spreading



Electromagnetic interference (EMI) reduction can be estimated using the following equation:
(1) Peak_power_reduction = 10 × log ((Deviation × f_c)/f_m) – 10
Where:

- Peak_power_reduction in dB
- Deviation in percentage of the initial clock frequency (f_c), is equal to $\Delta f/f_c$
- f_c is the original clock frequency, in MHz
- f_m is the spreading frequency, in MHz

  According to equation (1), the deviation can also be calculated, and then f for a required reduction in peak-power:
  (2) Deviation = $(f_m/f_c) \times 10^{((Peak\_power\_reduction + 10)/10)}$
  Example:
  For f_c = 160 MHz, Deviation = 1% peak from f_c (Δf = 1.6 MHz) and f_m = 16 kHz, the estimated peak power reduction is 10 dB.

3.6.3.3.5.5 Bandwidth Calculation (Carson's Bandwidth Rule)

Carson's bandwidth rule defines the approximate bandwidth requirements of communications system components for a carrier signal that is frequency modulated by a continuous or broad spectrum of frequencies, rather than by a single frequency.

Carson's bandwidth rule is expressed by the relation CBR = 2 × (f + f_m), where CBR is the bandwidth requirement, f is the peak frequency deviation, and f_m is the highest frequency in the modulating signal. For example, an FM signal with a 5-kHz peak deviation, and a maximum audio frequency of 3 kHz, would require an approximate bandwidth 2 × (5 + 3) = 16 kHz.

Theoretically, any FM signal has an infinite number of sidebands and, hence, an infinite bandwidth. In practice, all significant sideband energy (98 percent or more) is concentrated within the bandwidth defined by Carson's bandwidth rule.

3.6.3.3.5.6 SSC Configuration

The configuration of the spreading feature is not mandatory when programming the DPLL. This feature is usually enabled when the DPLL clocks generate harmonics, which can potentially interfere with the GSM carrier frequencies.

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Once the clock generation control registers are configured, the spreading on the clock signal can be configured as follows:

1. Calculate ModFreqDivider and DeltaMStep based on the desired peak-power reduction.
2. Configure the MODFREQDIV_EXPONENT, MODFREQDIV_MANTISSA, and DELTAMSTEP bit fields according to the calculated values.
3. Enable the spreading using the DPLL_SSC_EN bit.

NOTE: Spreading on a clock must be carefully configured to avoid adding noise on frequencies that are used by another module. For example, adding spreading on a clock to reduce noise on GSM frequencies can move the generated noise to the frequency of the memory controller and thus degrade its performance.

Example:
For f_c = 160 MHz, Deviation = 1% peak from f_c (Δf = 1.6 MHz) and f_m = 16 kHz, the estimated peak power reduction is 10 dB.
The output clock can be calculated using the following equation: $f_c = (f_{inp} \times M)/((N + 1) \times M2)$ (where M is a software-controlled multiplier, N is software-controlled divider, M2 is software-controlled output divider, f_c stands for f_{CLKOUT_M2}, for other output clock frequencies calculation and more information see section Section 3.6.3.3.1 *DPLLs Output Clocks Parameters* and the Clock Tree Tool).

The input clock is f_{inp} = 38.4 MHz. The following settings of the DPLL are required to have f_c = 160 MHz: M = 25, N = 2, M2 = 2. The value of M satisfies the restrictions: M – ΔM > = 20. Also, M + ΔM < = 2045.
f_{ref} can be calculated using the following equation: $f_{ref} = f_{inp}/(1 + N)$ = 12.8 MHz
ModFreqDivider can be calculated using the following equation: ModFreqDivider = $f_{ref}/(4 \times f_m)$ = 200
The exponent and mantissa of ModFreqDivider can now be calculated (where ModFreqDivider = Mantissa $\times 2^{Exponent}$ and it must be used as the minimal value for the exponent): Mantissa = 100, Exponent = 1
Knowing the deviation and M, ΔM can now be calculated: $\Delta M/M = 1\% \geq \Delta M = 0.01 \times 25 = 0.25$
DeltaMStep can be calculated as follows: DeltaMStep = ΔM/ModFreqDivider = 0.00125
The integer and fractional part of DeltaMStep can now be determined: Integer part = 0, Fractional part = $0.00125 \times 2^{18} = 327$ (for an 18-bit fractional part)
The DPLL can be configured as follows:

- MODFREQDIV_EXPONENT = 1
- MODFREQDIV_MANTISSA = 100
- DELTAMSTEP = 327

  The state of the modulation feature can be monitored with the DPLL_SSC_ACK bit of the corresponding register.

NOTE: Because this is in-band modulation for the DPLL, the modulation frequency must be within the DPLL loop bandwidth ($f_m < f_{ref}/70$). A higher modulation frequency would result in less spreading in the output clock.

When deactivating the spreading (DPLL_SSC_EN = 0), the end-of-spreading is synchronous to the internal spreading cycle. Thus, there is no residual average frequency error.

3.6.3.3.6 DPLL Output Power Down

The DCO clock LDO (DCOCLKLDO) of the DPLL can be powered down if all output dividers of the DPLL are powered down. The PRCM module automatically reenables the power to the LDO when an output divider is powered up or the DPLL switches to bypass mode.

Table 3-49. DPLL Power-Down Control Parameters

Parameter	Description
DCO clock LDO power down control	Enable/disable automatic power-down feature if all output dividers are powered down.

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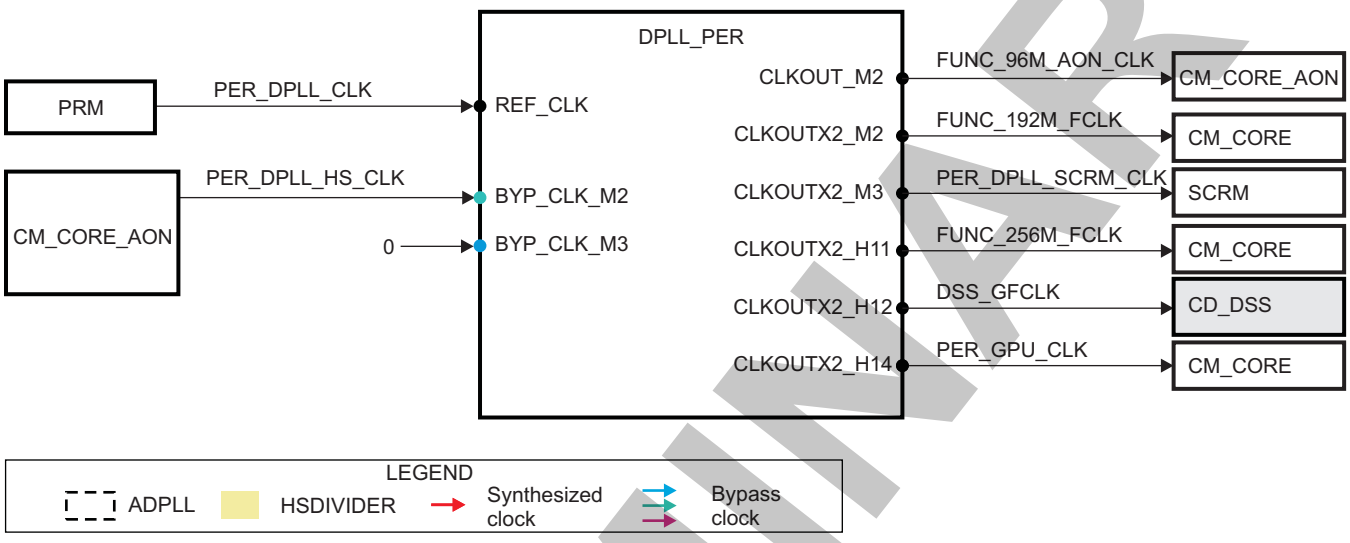
3.6.3.4 DPLL_PER Description

3.6.3.4.1 Overview

Figure 3-49 is an overview of the DPLL. For a functional overview of a generic DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

Figure 3-49. DPLL_PER Overview



3.6.3.4.2 Synthesized Clock Parameters

This section describes the clock synthesis and clock out divider parameters of the DPLL. For an explanation of the clock synthesis and output divider parameters of the DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*

Table 3-50 lists the clock synthesis parameters of the DPLL.

Table 3-50. DPLL_PER Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_PER[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_PER[6:0] DPLL_DIV

Table 3-51 lists the clock output divider parameters of the DPLL.

Table 3-51. DPLL_PER Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Status	CM_DIV_M2_DPLL_PER[9] CLKST
CLKOUT_M2	Divider control	CM_DIV_M2_DPLL_PER[4:0] DIVHS
CLKOUTX2_M2	Status	CM_DIV_M2_DPLL_PER[11] CLKX2ST
CLKOUTX2_M3	Status	CM_DIV_M3_DPLL_PER[9] CLKST
CLKOUTX2_M3	Divider control	CM_DIV_M3_DPLL_PER[4:0] DIVHS
CLKOUTX2_H11	Status	CM_DIV_H11_DPLL_PER[9] CLKST
CLKOUTX2_H11	Divider control	CM_DIV_H11_DPLL_PER[5:0] DIVHS
CLKOUTX2_H12	Status	CM_DIV_H12_DPLL_PER[9] CLKST
CLKOUTX2_H12	Divider control	CM_DIV_H12_DPLL_PER[5:0] DIVHS
CLKOUTX2_H14	Status	CM_DIV_H14_DPLL_PER[9] CLKST
CLKOUTX2_H14	Divider control	CM_DIV_H14_DPLL_PER[5:0] DIVHS

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3.6.3.4.3 Power Modes

This section identifies the operating modes supported by the DPLL and the control bit fields to set its operating modes. For an explanation of the DPLL operating modes and the associated control and status features, see Section 3.6.3.3.2, *Enable Control, Status, and Low-Power Operation Mode*, and Section 3.6.3.3.3, *DPLL Power Modes*.

Table 3-52 lists the operating modes supported by the DPLL.

Table 3-52. DPLL_PER Modes

Low-Power Stop	Fast-Relock Stop	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available	Available	Available

Table 3-53 lists the control bit fields for the operating mode control of the DPLL.

Table 3-53. DPLL_PER Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_PER[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_PER[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_PER[2:0] AUTO_DPLL_MODE

3.6.3.4.4 Recalibration

Table 3-54 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. For an explanation of the DPLL recalibration feature, see Section 3.6.3.3.4, *DPLL Recalibration*.

Table 3-54. DPLL_PER Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration – Enable Control	CM_CLKMODE_DPLL_PER[8] DPLL_DRIFTGUARD_EN
Recalibration – Interrupt Status	PRM_IRQSTATUS_MPU[3] DPLL_PER_RECAL_ST
Recalibration – Interrupt Mask Control	PRM_IRQENABLE_MPU[3] DPLL_PER_RECAL_EN
Recalibration – Interrupt Status	PRM_IRQSTATUS_IPU[3] DPLL_PER_RECAL_ST
Recalibration – Interrupt Mask Control	PRM_IRQENABLE_IPU[3] DPLL_PER_RECAL_EN

3.6.3.4.5 Spread Spectrum Clocking

Table 3-55 lists the control bit fields associated with the SSC features of the DPLL. For an explanation of the DPLL SSC feature, see Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*.

Table 3-55. DPLL_PER Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_PER[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_PER[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_PER[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_PER[19:0] DELTAMSTEP
Modulation Frequency Divider – Exponent	CM_SSC_MODFREQDIV_DPLL_PER[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider – Mantissa	CM_SSC_MODFREQDIV_DPLL_PER[6:0] MODFREQDIV_MANTISSA

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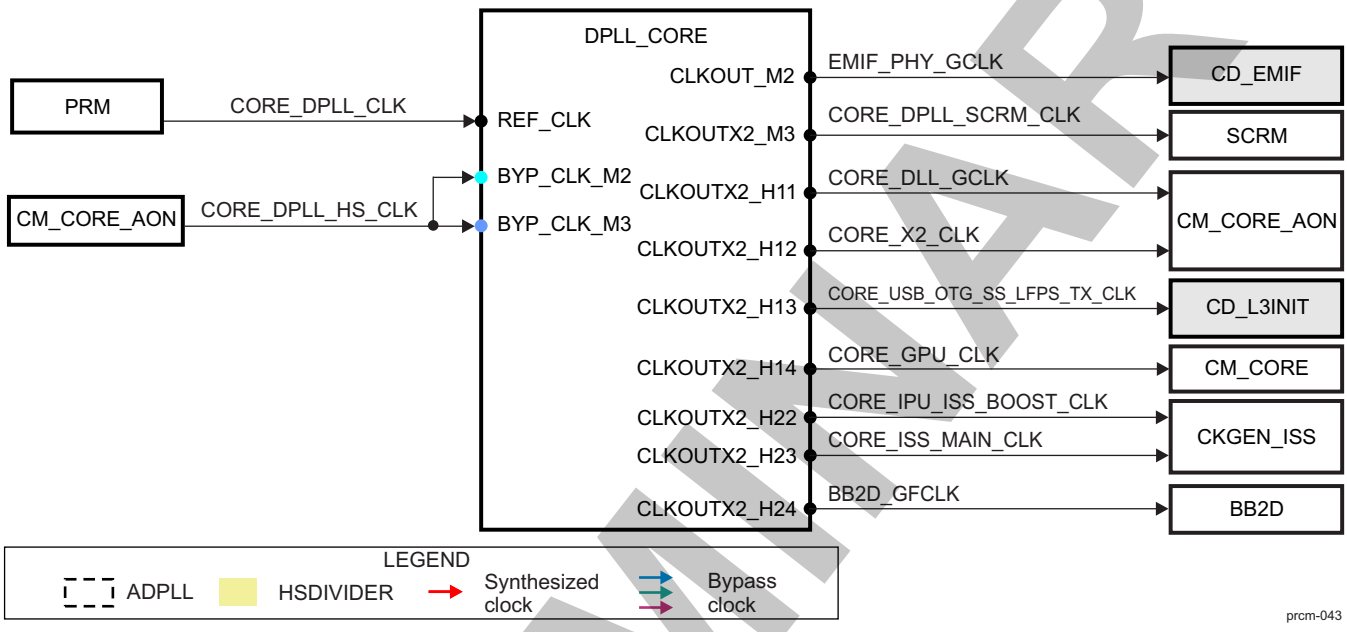
3.6.3.5 DPLL_CORE Description

3.6.3.5.1 Overview

Figure 3-50 is an overview of the DPLL. For a functional overview of a generic DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

Figure 3-50. DPLL_CORE Overview



3.6.3.5.2 Synthesized Clock Parameters

This section describes the clock synthesis and clock-out divider parameters of the DPLL. For an explanation of the clock synthesis and output divider parameters of the DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

Table 3-56 lists the clock synthesis parameters of the DPLL.

Table 3-56. DPLL_CORE Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_CORE[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_CORE[6:0] DPLL_DIV

Table 3-57 lists the clock output divider parameters of the DPLL.

Table 3-57. DPLL_CORE Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Status	CM_DIV_M2_DPLL_CORE[9] CLKST
CLKOUT_M2	Divider control	CM_DIV_M2_DPLL_CORE[4:0] DIVHS
CLKOUTX2_M3	Status	CM_DIV_M3_DPLL_CORE[9] CLKST
CLKOUTX2_M3	Divider control	CM_DIV_M3_DPLL_CORE[4:0] DIVHS
CLKOUTX2_H11	Status	CM_DIV_H11_DPLL_CORE[9] CLKST
CLKOUTX2_H11	Divider control	CM_DIV_H11_DPLL_CORE[5:0] DIVHS
CLKOUTX2_H12	Status	CM_DIV_H12_DPLL_CORE[9] CLKST
CLKOUTX2_H12	Divider control	CM_DIV_H12_DPLL_CORE[5:0] DIVHS
CLKOUTX2_H13	Status	CM_DIV_H13_DPLL_CORE[9] CLKST

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Table 3-57. DPLL_CORE Clock Output Parameters (continued)

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUTX2_H13	Divider control	CM_DIV_H13_DPLL_CORE[5:0] DIVHS
CLKOUTX2_H14	Status	CM_DIV_H14_DPLL_CORE[9] CLKST
CLKOUTX2_H14	Divider control	CM_DIV_H14_DPLL_CORE[5:0] DIVHS
CLKOUTX2_H22	Status	CM_DIV_H22_DPLL_CORE[9] CLKST
CLKOUTX2_H22	Divider control	CM_DIV_H22_DPLL_CORE[5:0] DIVHS
CLKOUTX2_H23	Status	CM_DIV_H23_DPLL_CORE[9] CLKST
CLKOUTX2_H23	Divider control	CM_DIV_H23_DPLL_CORE[5:0] DIVHS
CLKOUTX2_H24	Status	CM_DIV_H24_DPLL_CORE[9]CLKST
CLKOUTX2_H24	Divider control	CM_DIV_H24_DPLL_CORE[5:0]DIVHS

3.6.3.5.3 Power Modes

This section identifies the operating modes supported by the DPLL and the control bit fields to set its operating modes. For an explanation of the DPLL operating modes and associated control and status features, see Section 3.6.3.3.2, *Enable Control, Status, and Low-Power Operation Mode,* and Section 3.6.3.3.3, *DPLL Power Modes*.

Table 3-58 lists the operating modes supported by the DPLL.

Table 3-58. DPLL_CORE Modes

Low-Power Stop	Fast-Relock Stop	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available	Available	Available

Table 3-59 lists the control bit fields for the operating mode control of the DPLL.

Table 3-59. DPLL_CORE Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_CORE[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_CORE[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_CORE[2:0] AUTO_DPLL_MODE

3.6.3.5.4 Recalibration

Table 3-60 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. For an explanation of the DPLL recalibration feature, see Section 3.6.3.3.4, *DPLL Recalibration*.

Table 3-60. DPLL_CORE Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration – Enable Control	CM_CLKMODE_DPLL_CORE[8] DPLL_DRIFTGUARD_EN
Recalibration – Interrupt Status	PRM_IRQSTATUS_MPU[0] DPLL_CORE_RECAL_ST
Recalibration – Interrupt Mask Control	PRM_IRQENABLE_MPU[0] DPLL_CORE_RECAL_EN
Recalibration – Interrupt Status	PRM_IRQSTATUS_IPU[0] DPLL_CORE_RECAL_ST
Recalibration – Interrupt Mask Control	PRM_IRQENABLE_IPU[0] DPLL_CORE_RECAL_EN

3.6.3.5.5 Spread Spectrum Clocking

Table 3-61 lists the control bit fields associated with the SSC features of the DPLL. For an explanation of the DPLL SSC feature, see Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*.

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Table 3-61. DPLL_CORE Spread-Spectrum Clocking Feature Parameters

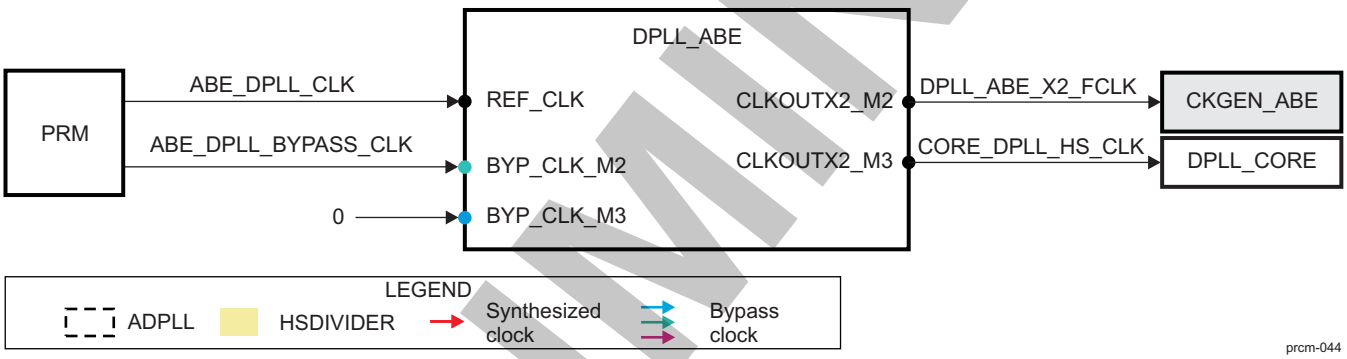
Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_CORE[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_CORE[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_CORE[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_CORE[19:0] DELTAMSTEP
Modulation Frequency Divider – Exponent	CM_SSC_MODFREQDIV_DPLL_CORE[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider – Mantissa	CM_SSC_MODFREQDIV_DPLL_CORE[6:0] MODFREQDIV_MANTISSA

3.6.3.6 DPLL_ABE Description

3.6.3.6.1 Overview

Figure 3-51 is an overview of the DPLL. For a functional overview of a generic DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

Figure 3-51. DPLL_ABE Overview



3.6.3.6.2 Synthesized Clock Parameters

This section describes the clock synthesis and clock-out divider parameters of the DPLL. For an explanation of the clock synthesis and output divider parameters of the DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

Table 3-62 lists the clock synthesis parameters of the DPLL.

Table 3-62. DPLL_ABE Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_ABE[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_ABE[6:0] DPLL_DIV
REGM4XEN	CM_CLKMODE_DPLL_ABE[11] DPLL_REGM4XEN

Table 3-63 lists the clock output divider parameters of the DPLL.

Table 3-63. DPLL_ABE Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUTX2_M2	Status	CM_DIV_M2_DPLL_ABE[11] CLKX2ST
CLKOUTX2_M2	Divider Control	CM_DIV_M2_DPLL_ABE[4:0] DIVHS
CLKOUTX2_M3	Status	CM_DIV_M3_DPLL_ABE[9] CLKST
CLKOUTX2_M3	Divider Control	CM_DIV_M3_DPLL_ABE [4:0] DIVHS

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3.6.3.6.3 Power Modes

This section identifies the operating modes supported by the DPLL and the control bit fields to set its operating modes. For an explanation of the DPLL operating modes and associated control and status features, see Section 3.6.3.3.2, *Enable Control, Status, and Low-Power Operation Mode*, and Section 3.6.3.3.3, *DPLL Power Mode*.

Table 3-64 lists the operating modes supported by the DPLL.

Table 3-64. DPLL_ABE Modes

Low-Power Stop	Fast-Relock Stop	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available	Available	Available

Table 3-65 lists the control bit fields for the operating mode control of the DPLL.

Table 3-65. DPLL_ABE Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_ABE[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_ABE[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_ABE[2:0] AUTO_DPLL_MODE

3.6.3.6.4 Recalibration

Table 3-66 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. For an explanation of the DPLL recalibration feature, see Section 3.6.3.3.4, *DPLL Recalibration*.

Table 3-66. DPLL_ABE Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration – Enable Control	CM_CLKMODE_DPLL_ABE[8] DPLL_DRIFTGUARD_EN
Recalibration – Interrupt Status	PRM_IRQSTATUS_MPU[4] DPLL_ABE_RECAL_ST
Recalibration – Interrupt Mask Control	PRM_IRQENABLE_MPU[4] DPLL_ABE_RECAL_EN

3.6.3.6.5 Spread Spectrum Clocking

Table 3-67 lists the control bit fields associated with the SSC features of the DPLL. For an explanation of the DPLL SSC feature, see Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*.

Table 3-67. DPLL_ABE Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_ABE[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_ABE[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_ABE[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_ABE[19:0] DELTAMSTEP
Modulation Frequency Divider – Exponent	CM_SSC_MODFREQDIV_DPLL_ABE[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider – Mantissa	CM_SSC_MODFREQDIV_DPLL_ABE[6:0] MODFREQDIV_MANTISSA

3.6.3.7 DPLL_MPU Description

3.6.3.7.1 Overview

Figure 3-52 is an overview of the DPLL. For a functional overview of a generic DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

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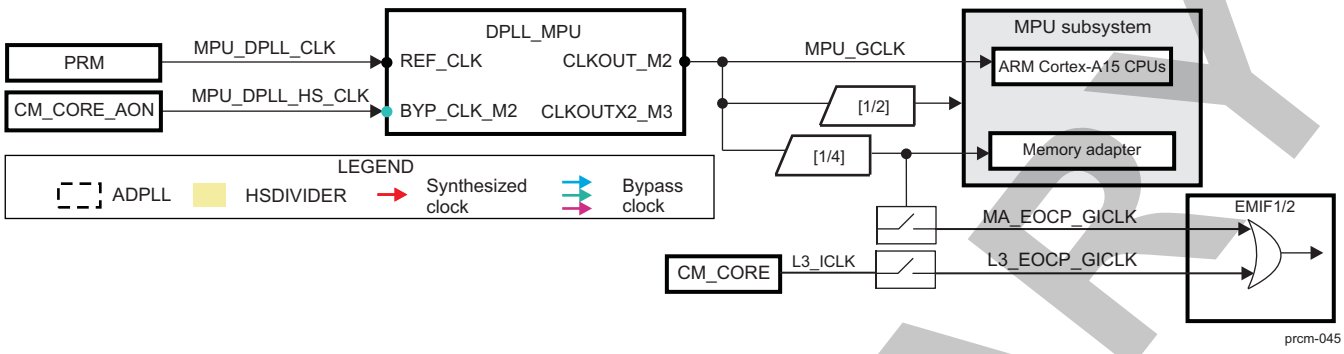
Figure 3-52. DPLL_MPU Overview



3.6.3.7.2 Tactical Clocking Adjustment

Figure 3-52 includes the clocking adjustment scheme for DPLL_MPU. Another clock is requested by the EMIF1/2 modules and this clock must be dynamically switched between L3_EOCP_GICLK clock and MA_EOCP_GICLK clock coming from the MPU subsystem (namely from Memory Adapter part of it), depending on the respective activity of MPU and EMIF clock domain.

3.6.3.7.3 Synthesized Clock Parameters

This section describes the clock synthesis and clock out divider parameters of the DPLL. See Section 3.6.3.3, *Generic DPLL Overview*, for an explanation of the clock synthesis and output divider parameters of the DPLL module.

Table 3-68 lists the clock synthesis parameters of the DPLL.

Table 3-68. DPLL_MPU Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_MPU[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_MPU[6:0] DPLL_DIV

Table 3-69 lists the clock output divider parameters of the DPLL.

Table 3-69. DPLL_MPU Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Status	CM_DIV_M2_DPLL_MPU[9] CLKST
CLKOUT_M2	Divider control	CM_DIV_M2_DPLL_MPU[4:0] DIVHS
CLKOUT_M2 - DCC	DCC feature control	CM_CLKSEL_DPLL_MPU[22] DCC_EN

3.6.3.7.4 Power Modes

This section identifies the operating modes supported by the DPLL and the control bit fields to set its operating modes. For an explanation of the DPLL operating modes, and associated control and status features, see Section 3.6.3.3.2, *Enable Control, Status, and Low-Power Operation Mode*, and Section 3.6.3.3.3, *DPLL Power Modes*.

Table 3-70 lists the operating modes supported by the DPLL.

Table 3-70. DPLL_MPU Modes

Low-Power Stop	Fast-Relock Stop	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available	Available	Available

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Table 3-71 lists the control bit fields for the operating mode control of the DPLL.

Table 3-71. DPLL_MPU Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_MPU[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_MPU[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_MPU[2:0] AUTO_DPLL_MODE

NOTE: The user software must ensure that the MPU voltage domain is on before programming DPLL_MPU. This can be ensured by performing a forced wakeup (CLKCTRL= SW_WKUP) on MPU domain. When software detects that the domain is "ON", DPLL_MPU can be programmed.

3.6.3.7.5 Recalibration

Table 3-72 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. For an explanation of the DPLL recalibration feature, see Section 3.6.3.3.4, *DPLL Recalibration*.

Table 3-72. DPLL_MPU Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration – Enable Control	CM_CLKMODE_DPLL_MPU[8] DPLL_DRIFTGUARD_EN
Recalibration – Interrupt Status	PRM_IRQSTATUS_MPU[1] DPLL_MPU_RECAL_ST
Recalibration – Interrupt Mask Control	PRM_IRQENABLE_MPU[1] DPLL_MPU_RECAL_EN

3.6.3.7.6 Spread Spectrum Clocking

Table 3-73 lists the control bit fields associated with the SSC features of the DPLL. For an explanation of the DPLL SSC feature, see Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*.

Table 3-73. DPLL_MPU Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_MPU[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_MPU[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_MPU[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_MPU[19:0] DELTAMSTEP
Modulation Frequency Divider – Exponent	CM_SSC_MODFREQDIV_DPLL_MPU[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider – Mantissa	CM_SSC_MODFREQDIV_DPLL_MPU[6:0] MODFREQDIV_MANTISSA

3.6.3.8 DPLL_IVA Description

3.6.3.8.1 Overview

Figure 3-53 is an overview of the DPLL. For a functional overview of a generic DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

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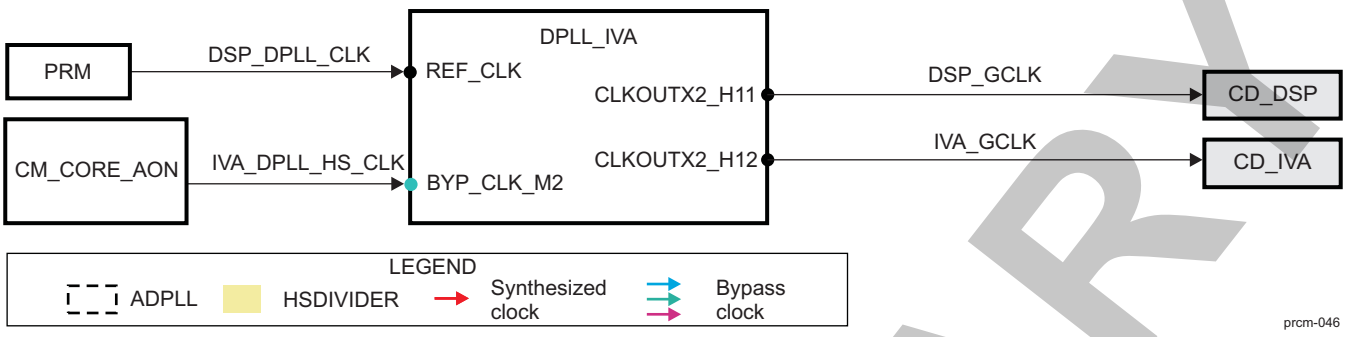
Figure 3-53. DPLL_IVA Overview



3.6.3.8.2 Synthesized Clock Parameters

This section describes the clock synthesis and clock-out divider parameters of the DPLL. For an explanation of the clock synthesis and output divider parameters of the DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

Table 3-74 lists the clock synthesis parameters of the DPLL.

Table 3-74. DPLL_IVA Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_IVA[18:8] DPLL_MULT
N	CM_CLKSEL_DPLL_IVA[6:0] DPLL_DIV

Table 3-75 lists the clock output divider parameters of the DPLL.

Table 3-75. DPLL_IVA Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUTX2_H11	Status	CM_DIV_H11_DPLL_IVA[9] CLKST
CLKOUTX2_H11	Divider control	CM_DIV_H11_DPLL_IVA[5:0] DIVHS
CLKOUTX2_H12	Status	CM_DIV_H12_DPLL_IVA[9] CLKST
CLKOUTX2_H12	Divider control	CM_DIV_H12_DPLL_IVA[5:0] DIVHS

NOTE: Softaware must be ensure that MM Voltage domain is ON before programming DPLL_IVA. This can be guarantied by performing force wakeup (CLKCTRL = SW_WKUP) on one of the domain of the MM voltage domain. When software detects domain is "ON", DPLL_IVA can be programmed.

3.6.3.8.3 Power Modes

This section identifies the operating modes supported by the DPLL and the control bit fields to set its operating modes. For an explanation of the DPLL operating modes and associated control and status features, see Section 3.6.3.3.2, *Enable Control, Status, and Low-Power Operation Mode*, and Section 3.6.3.3.3, *DPLL Power Modes*.

Table 3-76 lists the operating modes supported by the DPLL.

Table 3-76. DPLL_IVA Modes

Low-Power Stop	Fast-Relock Stop	Low-Power Bypass	Fast-Relock Bypass	Lock
Not available	Not available	Available	Available	Available

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Table 3-77 lists the control bit fields for the operating mode control of the DPLL.

Table 3-77. DPLL_IVA Mode Control Parameters

Parameter Name	Control Bit Field
Low-Power Mode Control	CM_CLKMODE_DPLL_IVA[10] DPLL_LPMODE_EN
Manual Mode Control	CM_CLKMODE_DPLL_IVA[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_IVA[2:0] AUTO_DPLL_MODE

NOTE: The user software must ensure that the MM voltage domain is on before programming DPLL_IVA. This can be ensured by performing a forced wakeup (CLKCTRL= SW_WKUP) on one of the domains of the MM voltage domain. When software detects that the domain is on, DPLL_IVA can be programmed.

3.6.3.8.4 Recalibration

Table 3-78 lists the control bit fields for the recalibration feature enable and interrupts of the DPLL. For an explanation of the DPLL recalibration feature, see Section 3.6.3.3.4, *DPLL Recalibration*.

Table 3-78. DPLL_IVA Recalibration Feature Parameters

Parameter Name	Control/Status Bit Field
Recalibration – Enable Control	CM_CLKMODE_DPLL_IVA[8] DPLL_DRIFTGUARD_EN
Recalibration – Interrupt Status	PRM_IRQSTATUS_MPU[2] DPLL_IVA_RECAL_ST
Recalibration – Interrupt Mask Control	PRM_IRQENABLE_MPU[2] DPLL_IVA_RECAL_EN
Recalibration – Interrupt Status	PRM_IRQSTATUS_IPU[2] DPLL_IVA_RECAL_ST
Recalibration – Interrupt Mask Control	PRM_IRQENABLE_IPU[2] DPLL_IVA_RECAL_EN

3.6.3.8.5 Spread Spectrum Clocking

Table 3-79 lists the control bit fields associated with the SSC features of the DPLL. For an explanation of the DPLL SSC feature, see Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*.

Table 3-79. DPLL_IVA Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_IVA[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_IVA[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_IVA[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_IVA[19:0] DELTAMSTEP
Modulation Frequency Divider – Exponent	CM_SSC_MODFREQDIV_DPLL_IVA[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider – Mantissa	CM_SSC_MODFREQDIV_DPLL_IVA[6:0] MODFREQDIV_MANTISSA

3.6.3.9 DPLL_USB Description

3.6.3.9.1 Overview

Figure 3-54 is an overview of the DPLL. For a functional overview of a generic DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

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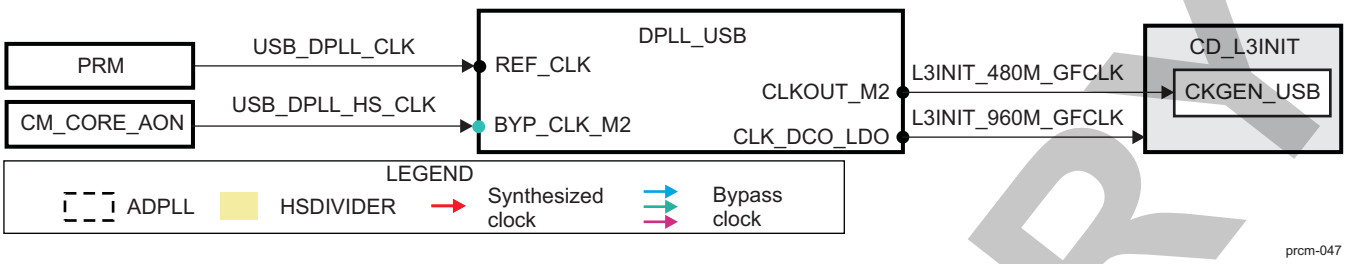
Figure 3-54. DPLL_USB Overview



3.6.3.9.2 Synthesized Clock Parameters

This section describes the clock synthesis and clock out divider parameters of the DPLL. For an explanation of the clock synthesis and output divider parameters of the DPLL module, see Section 3.6.3.3, *Generic DPLL Overview*.

Table 3-80 lists the clock synthesis parameters of the DPLL.

Table 3-80. DPLL_USB Clock Synthesis Parameters

Parameter Name	Control Bit Field
M	CM_CLKSEL_DPLL_USB[19:8] DPLL_MULT
N	CM_CLKSEL_DPLL_USB[7:0] DPLL_DIV

Table 3-81 lists the clock output divider parameters of the DPLL.

Table 3-81. DPLL_USB Clock Output Parameters

Clock Output/Divider	Parameter Name	Control/Status Bit Field
CLKOUT_M2	Status	CM_DIV_M2_DPLL_USB[9] CLKST
CLKOUT_M2	Divider control	CM_DIV_M2_DPLL_USB[6:0] DIVHS
CLK_DCO_LDO	DCO output control	CM_CLKSEL_DPLL_USB[21] DPLL_SELFREQDCO

3.6.3.9.3 Power Modes

This section identifies the operating modes supported by the DPLL and the control bit fields to set its operating modes. For an explanation of the DPLL operating modes and associated control and status features, see Section 3.6.3.3.2, *Enable Control, Status, and Low-Power Operation Mode,* and Section 3.6.3.3.3, *DPLL Power Modes*.

Table 3-82 lists the operating modes supported by the DPLL.

Table 3-82. DPLL_USB Modes

Low-Power Stop	Low-Power Bypass	Lock
Available	Available	Available

NOTE: It is prohibited to program DPLL_USB automatic idle mode with a PD_L3_INIT low power state equal to OFF. Moreover, DPLL_USB programming can be done only when PD_L3_INIT power domain is ON

Table 3-83 lists the control bit fields for the operating mode control of the DPLL.

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Table 3-83. DPLL_USB Mode Control Parameters

Parameter Name	Control Bit Field
Manual Mode Control	CM_CLKMODE_DPLL_USB[2:0] DPLL_EN
Auto Mode Control	CM_AUTOIDLE_DPLL_USB[2:0] AUTO_DPLL_MODE

3.6.3.9.4 Spread Spectrum Clocking

Table 3-84 lists the control bit fields associated with the SSC features of the DPLL. For an explanation of the DPLL SSC feature, see Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*.

Table 3-84. DPLL_USB Spread-Spectrum Clocking Feature Parameters

Parameter Name	Control Bit Field
SSC Downspread	CM_CLKMODE_DPLL_USB[14] DPLL_SSC_DOWNSPREAD
SSC Acknowledge	CM_CLKMODE_DPLL_USB[13] DPLL_SSC_ACK
SSC Enable Control	CM_CLKMODE_DPLL_USB[12] DPLL_SSC_EN
Modulation Step Size Setting	CM_SSC_DELTAMSTEP_DPLL_USB[20:0] DELTAMSTEP
Modulation Frequency Divider – Exponent	CM_SSC_MODFREQDIV_DPLL_USB[10:8] MODFREQDIV_EXPONENT
Modulation Frequency Divider – Mantissa	CM_SSC_MODFREQDIV_DPLL_USB[6:0] MODFREQDIV_MANTISSA

3.6.3.10 DPLLs Cascading

To reduce the device power consumption in certain low-power use cases of the device, the DPLLs in the device can be cascaded so that the functional clock to a power domain is provided by a DPLL upstream without locking the DPLL associated with the domain. In such a case, the unlocked DPLLs can be kept in low-power bypass mode.

Figure 3-55 shows a generic scheme for cascading DPLLs.

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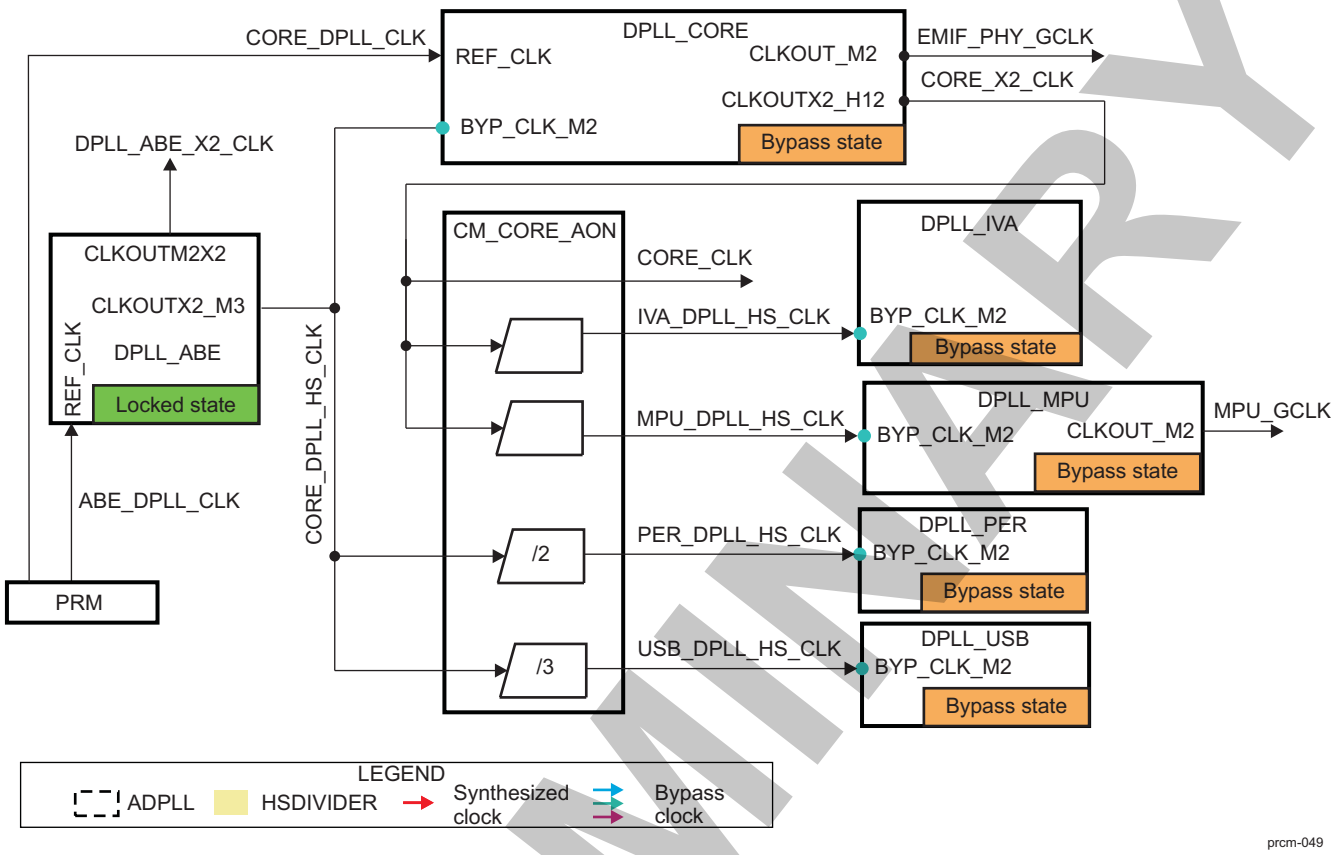
Figure 3-55. DPLLs Cascading Overview



The sequence to enable DPLL cascading is:

1. DPLL_ABE is locked by software request. Other DPLLs downstream must not be moved to bypass mode before DPLL_ABE is locked. This ensures that the output clocks of these DPLLs are not stopped when they switch to the DPLL_ABE output clock. The ABE clock domain must be configured into SW_WKUP during DPLL cascading mode.
2. Internal EMIF shadow registers are set to take the PHY clock and DLL reference clock derived from DPLL_ABE.
3. Bypass path for DPLL_IVA is set up by configuring the programmable dividers in CM_CORE_AON that provide the bypass clock. The setting is based on the OPP requirements.
4. DPLL_IVA and DPLL_MPU are put into bypass mode by software (any of the bypass mode is allowed), and the output of the DPLLs, if already enabled, switches from locked clock to bypass clock from DPLL_CORE.
5. DPLL_PER and DPLL_USB are also put into bypass mode by software, if required. The outputs of the DPLLs, if enabled, switch to the divided clock of DPLL_ABE CLKOUTX2_M3.
6. Ensure that the CORE_CLK divider in CM_CORE_AON is programmed correctly to handle the OPP needs of the CORE power domain before this step.

   DPLL_CORE is set in bypass mode by configuring the input mux of the bypass clocks and the CM_SHADOW_FREQ_CONFIG1[10:8] DPLL_CORE_DPLL_EN bit field to bypass mode in the DVFS shadow register in CM_CORE_AON, and setting the CM_SHADOW_FREQ_CONFIG1[0] FREQ_UPDATE bit to 1 by software. This step triggers the handshake with EMIF to safely unlock the DPLL and move the output clock of DPLL_CORE to CORE_DPLL_HS_CLK.
7. Software can then switch the L4_WKUP interface clock from SYS_CLK to ABE_LP_CLK to allow for deasserting the SYS_CLK request line to SCRM, if SYS_CLK is not requested by any other dependency.

The sequence to disable the DPLL cascading is:

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1. Software switches the L4_WKUP interface clock from ABE_LP_CLK to SYS_CLK requesting the restart of SYS_CLK by the SCRM, if not already present.
2. Software programs the EMIF internal shadow registers to prepare the switchback of EMIF from using the DPLL_ABE clock to the DPLL_CORE clock.
3. DPLL_IVA/DPLL_MPU bypass path is correctly set for the targeted DPLL_CORE frequency by programming the bypass dividers for the DPLL in CM_CORE_AON.
4. DPLL_CORE is relocked using the DVFS shadow register in CM_CORE_AON. The PRCM module ensures that this step is executed with proper handshake with EMIF to allow for a frequency update on the EMIF.
5. Other DPLLs are also locked, if required, to exit completely from DPLL cascading mode.
6. DPLL_ABE may be forced into STOPMODE or bypass mode by software or may enter one of the auto modes if so programmed.

NOTE: The DPLLs cascading is useful in MP3 playback use case, while using the SYS_32K clock only, and SYS_CLK is gated.

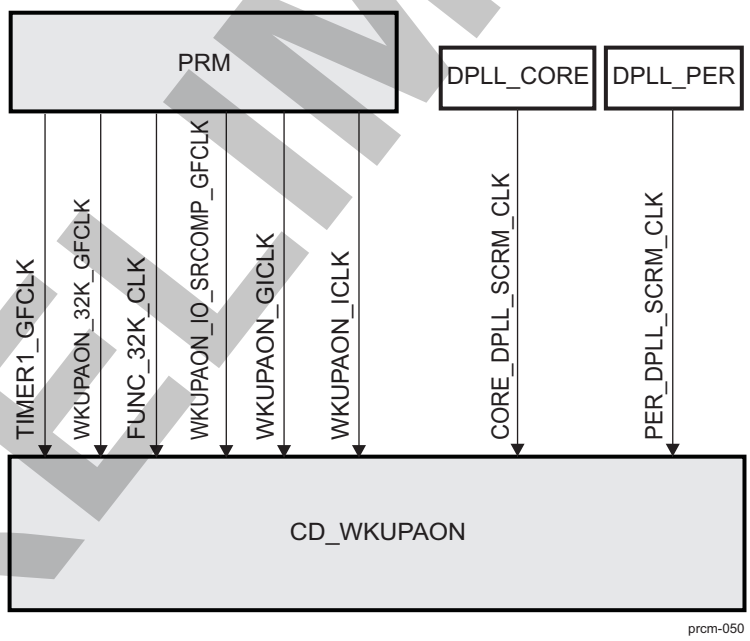
3.6.4 CD_WKUPAON Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.4.1 Overview

Figure 3-56 is an overview of the clock domain.

Figure 3-56. CD_WKUPAON Overview



3.6.4.2 Specific properties and signals.

PRCM provides WKUPAON_IO_SRCOMP_PWRDN signal to the smart IO compensation cell part of WKUP voltage domain. This signal is fully controlled by HW. After power on reset, SW has to enable IO slew rate compensation cell clock by setting CM_WKUPAON_IO_SRCOMP_CLKCTRL[8] CLKEN_SRCOMP_FCLK. PRCM enables WKUPAON_IO_SRCOMP_GFCLK clock and de-assert WKUPAON_IO_SRCOMP_PWRDN signal.

Before device transition to low power state, PRCM:

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1. Asserts WKUPAON_IO_SRCOMP_PWRDN signal first.
2. Wait for 8 SYS_CLK cycles.
3. Gates WKUPAON_IO_SRCOMP_GFCLK clock.

When device wakes-up from low power state, PRCM enables automatically WKUPAON_IO_SRCOMP_GFCLK clock and de-asserts WKUPAON_IO_SRCOMP_PWRDN signal.

NOTE:

1. By clearing CM_WKUPAON_IO_SRCOMP_CLKCTRL[8] CLKEN_SRCOMP_FCLK bitfield can disable WKUPAON_IO_SRCOMP_GFCLK clock and set WKUPAON_IO_SRCOMP_PWRDN signal.
2. For low power cases, to allow gating of SYS_CLK, it has to disable WKUPAON_IO_SRCOMP_GFCLK clock.

3.6.4.3 Clock Domain Modes

Table 3-85 lists the clock domain modes supported by the clock domain.

Table 3-85. CD_WKUPAON Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Not available	Available

Table 3-86 lists the clock domain state transition control and status bits for the clock in this clock domain

Table 3-86. CD_WKUPAON Control and Status Parameters

Parameter Name	Control/Status Bit Field
ABE_LP_CLK Clock Status	CM_WKUPAON_CLKSTCTRL[9] CLKACTIVITY_ABE_LP_CLK
WKUPAON_GICLK Clock Status	CM_WKUPAON_CLKSTCTRL[12] CLKACTIVITY_WKUPAON_GICLK
SYS_CLK Clock Status; includes profiling EMU_SYS_CLK and all functional SYS_CLK	CM_WKUPAON_CLKSTCTRL[8] CLKACTIVITY_SYS_CLK
SYS_CLK Status when running at SCRM level	CM_WKUPAON_CLKSTCTRL[15] CLKACTIVITY_SYS_CLK_ALL
SYS_CLK Clock Status of functional branches, exclude activity of the EMU_SYS_GCLK clock	CM_WKUPAON_CLKSTCTRL[14] CLKACTIVITY_SYS_CLK_FUNC
WKUPAON_32K_GFCLK Clock Status	CM_WKUPAON_CLKSTCTRL[11] CLKACTIVITY_WKUPAON_32K_GFCLK
WKUPAON_32K_GFCLK Clock Control for GPIO1	CM_WKUPAON_GPIO1_CLKCTRL[8] OPTFCLKEN_DBCLK
WKUPAON_IO_SRCOMP_GFCLK Clock Status	CM_WKUPAON_CLKSTCTRL[13] CLKACTIVITY_WKUPAON_IO_SRCOMP_GFCLK
PER_DPLL_SCRM_CLK Clock Control	CM_WKUPAON_SCRM_CLKCTRL[9] OPTFCLKEN_SCRM_PER
CORE_DPLL_SCRM_CLK Clock Control	CM_WKUPAON_SCRM_CLKCTRL[8] OPTFCLKEN_SCRM_CORE
WKUPAON_IO_SRCOMP_GFCLK Clock Control	CM_WKUPAON_IO_SRCOMP_CLKCTRL[8] CLKEN_SRCOMP_FCLK
Clock Domain State Transition Control	CM_WKUPAON_CLKSTCTRL[1:0] CLKTRCTRL

3.6.4.4 Clock Domain Dependency

CD_WKUPAON has no static dependency or dynamic dependency with any other clock domain of the device.

3.6.4.4.1 Wake-Up Dependency

Table 3-87 lists the wake-up dependency settings for the modules of this clock domain.

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Table 3-87. CD_WKUPAON Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
GPIO1	CD_WKUPAON	CD_DSP	Enabled	PM_WKUPAON_GPIO1_WKDEP[6] WKUPDEP_GPIO1_IRQ2_DSP	Read/write
GPIO1	CD_WKUPAON	CD_IPU	Disabled	PM_WKUPAON_GPIO1_WKDEP[1] WKUPDEP_GPIO1_IRQ1_IPU	Read/write
GPIO1	CD_WKUPAON	CD_MPU	Disabled	PM_WKUPAON_GPIO1_WKDEP[0] WKUPDEP_GPIO1_IRQ1_MPU	Read/write
KBD	CD_WKUPAON	CD_MPU	Enabled	PM_WKUPAON_KBD_WKDEP[0] WKUPDEP_KBD_MPU	Read/write
TIMER1	CD_WKUPAON	CD_MPU	Enabled	PM_WKUPAON_TIMER1_WKDEP[0] WKUPDEP_TIMER1_MPU	Read/write
WD_TIMER2	CD_WKUPAON	CD_MPU	Disabled	PM_WKUPAON_WD_TIMER2_WKDEP[0] WKUPDEP_WD_TIMER2_MPU	Read/write

3.6.4.5 Clock Domain Module Attributes

Table 3-88 lists for each module of the clock domain the clocks it receives and their role (that is, functional or interface clock).

Table 3-88. CD_WKUPAON Modules Clocks Association

Module	Clock	Clock Type
PRCM_MPU	SYS_32K	Functional
	WKUPAON_ICLK	Interface
GPIO1	WKUPAON_GICLK	Interface
	WKUPAON_32K_GFCLK	Functional
KBD	WKUPAON_GICLK	Interface
	WKUPAON_32K_GFCLK	Functional
SAR_RAM	WKUPAON_GICLK	Interface
COUNTER_32K	SYS_32K	Functional
	WKUPAON_GICLK	Interface
TIMER1	TIMER1_FCLK	Functional
	WKUPAON_GICLK	Interface
WD_TIMER2	WKUPAON_GICLK	Interface
	WKUPAON_32K_GFCLK	Functional
CTRL_MODULE_WKUP	WKUPAON_GICLK	Interface
SCRM	WKUPAON_GICLK	Interface
	PER_DPLL_SCRM_CLK	Functional
	CORE_DPLL_SCRM_CLK	Functional
L4_WKUP interconnect	WKUPAON_GICLK	Interface
IO_SRCOMP_WKUP	WKUPAON_IO_SRCOMP_GFCLK	Functional

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Table 3-89 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-89. CD_WKUPAON Modules Wake-Up Request

Module	Wake-Up Feature
PRCM_MPU	None
CTRL_MODULE_WKUP	None
IO_SRCOMP_WKUP	None
SCRM	None
GPIO1	Slave wake-up request (MPU-IRQ, IPU-IRQ, DSP-IRQ)
KBD	Slave wake-up request (MPU-IRQ)
SAR_RAM	None
COUNTER_32K	None
TIMER1	Slave wake-up request (MPU-IRQ)
WD_TIMER2	Slave wake-up request (MPU-IRQ)
L4_WKUP interconnect	None

Table 3-90 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-90. CD_WKUPAON Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
GPIO1	Slave	CM_WKUPAON_GPIO1_CLKCTRL[17:16] IDLEST	Idle status
KBD	Slave	CM_WKUPAON_KBD_CLKCTRL[17:16] IDLEST	Idle status
SAR_RAM	Slave	CM_WKUPAON_SAR_RAM_CLKCTRL[17:16] IDLEST	Idle status
COUNTER_32K	Slave	CM_WKUPAON_COUNTER_32K_CLKCTRL[17:16] IDLEST	Idle status
TIMER1	Slave	CM_WKUPAON_TIMER1_CLKCTRL[17:16] IDLEST	Idle status
WD_TIMER2	Slave	CM_WKUPAON_WD_TIMER2_CLKCTRL[17:16] IDLEST	Idle status
L4_WKUP interconnect	Slave	CM_WKUPAON_L4_WKUP_CLKCTRL[17:16] IDLEST	Idle status

Table 3-91 lists the supported clock management modes and associated software control bit fields for each module of the power domain.

Table 3-91. CD_WKUPAON Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
GPIO1	Available	Available	N/A	CM_WKUPAON_GPIO1_CLKCTRL[1:0] MODULEMODE	Read/write
KBD	Available	N/A	Available	CM_WKUPAON_KBD_CLKCTRL[1:0] MODULEMODE	Read/write
SAR_RAM	N/A	Available	N/A	CM_WKUPAON_SAR_RAM_CLKCTRL[1:0] MODULEMODE	Read only
COUNTER_32K	N/A	Available	N/A	CM_WKUPAON_COUNTER_32K_CLKCTRL[1:0] MODULEMODE	Read only
TIMER1	Available	N/A	Available	CM_WKUPAON_TIMER1_CLKCTRL[1:0] MODULEMODE	Read/write

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Table 3-91. CD_WKUPAON Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
WD_TIMER2	Available	N/A	Available	CM_WKUPAON_WD_TIMER2_CLKCTRL[1:0] MODULEMODE	Read/write
L4_WKUP interconnect	N/A	Available	N/A	CM_WKUPAON_L4_WKUP_CLKCTRL[1:0] MODULEMODE	Read only

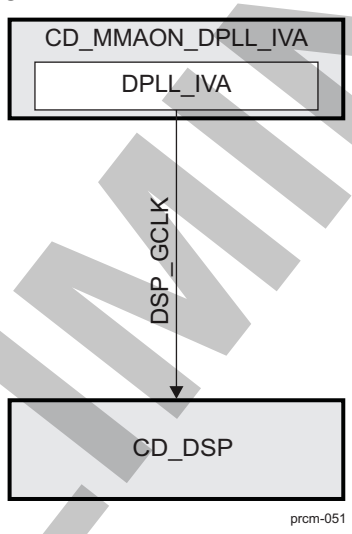
3.6.5 CD_DSP Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.5.1 Overview

Figure 3-57 is an overview of the clock domain.

Figure 3-57. CD_DSP Overview



3.6.5.2 Clock Domain Modes

Table 3-92 lists the modes supported by the clock domain.

Table 3-92. CD_DSP Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-93 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-93. CD_DSP Control and Status Parameters

Parameter Name	Control/Status Bit Field
DSP_GCLK Clock Status	CM_DSP_CLKSTCTRL[8] CLKACTIVITY_DSP_GCLK
Clock Domain State Transition Control	CM_DSP_CLKSTCTRL[1:0] CLKTRCTRL

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3.6.5.3 Clock Domain Dependency

CD_DSP has no module wake-up dependency with any other clock domain of the device.

3.6.5.3.1 Static Dependency

Table 3-94 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-94. CD_DSP Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_DSP_STATICDEP[3] ABE_STATDEP	Read/write
CD_CAM	Always disabled	CM_DSP_STATICDEP[9] CAM_STATDEP	Read only
CD_IVA	Disabled	CM_DSP_STATICDEP[2] IVA_STATDEP	Read/write
CD_L3_MAIN1	Disabled	CM_DSP_STATICDEP[5] L3MAIN1_STATDEP	Read/write
CD_L3_MAIN2	Disabled	CM_DSP_STATICDEP[6] L3MAIN2_STATDEP	Read/write
CD_L3INIT	Disabled	CM_DSP_STATICDEP[7] L3INIT_STATDEP	Read/write
CD_L4_CFG	Disabled	CM_DSP_STATICDEP[12] L4CFG_STATDEP	Read/write
CD_L4_PER	Disabled	CM_DSP_STATICDEP[13] L4PER_STATDEP	Read/write
CD_EMIF	Disabled	CM_DSP_STATICDEP[4] EMIF_STATDEP	Read/write
CD_WKUPAON	Disabled	CM_DSP_STATICDEP[15] WKUPAON_STATDEP	Read/write
CD_COREAON	Always disabled	CM_DSP_STATICDEP[16] COREAON_STATDEP	Read only
CD_CUSTEFUSE	Always disabled	CM_DSP_STATICDEP[17] CUSTEFUSE_STATDEP	Read only

3.6.5.3.2 Dynamic Dependency

Table 3-95 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-95. CD_DSP Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Always enabled	CM_DSP_DYNAMICDEP[3] ABE_DYNDEP	Read only
CD_IVA	Always enabled	CM_DSP_DYNAMICDEP[2] IVA_DYNDEP	Read only
CD_L3_MAIN1	Always enabled	CM_DSP_DYNAMICDEP[5] L3MAIN1_DYNDEP	Read only

3.6.5.4 Clock Domain Module Attributes

Table 3-96 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

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Table 3-96. CD_DSP Modules Clocks Association

Module	Clock	Clock Type
DSP	DSP_GCLK	Interface and functional

Table 3-97 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-97. CD_DSP Modules Wake-Up Request

Module	Wake-Up Feature
DSP	Master wake-up request

Table 3-98 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-98. CD_DSP Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
DSP	Master/slave	CM_DSP_DSP_CLKCTRL[18] STBYST	Standby status
		CM_DSP_DSP_CLKCTRL[17:16] IDLEST	Idle status

Table 3-99 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-99. CD_DSP Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
DSP	Available	Available	N/A	CM_DSP_DSP_CLKCTRL[1:0] MODULEMODE	Read/write

3.6.6 CD_CUSTEFUSE Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.6.1 Overview

Figure 3-57 is an overview of the clock domain.

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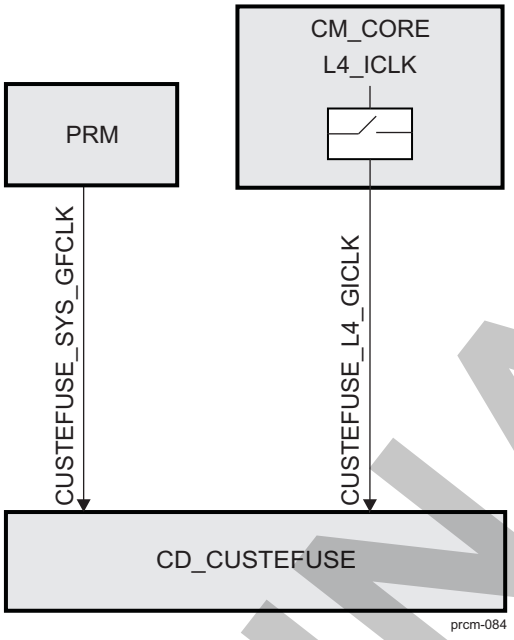
Figure 3-58. CD_CUSTEFUSE Overview



3.6.6.2 Clock Domain Modes

Table 3-92 lists the modes supported by the clock domain.

Table 3-100. CD_CUSTEFUSE Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	N/A	Available	Available

Table 3-93 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-101. CD_CUSTEFUSE Control and Status Parameters

Parameter Name	Control/Status Bit Field
CUSTEFUSE_SYS_GFCLK Clock Status	CM_CUSTEFUSE_CLKSTCTRL[9] CLKACTIVITY_CUSTEFUSE_SYS_GFCLK
CUSTEFUSE_L4_GICLK Clock Status	CM_CUSTEFUSE_CLKSTCTRL[8] CLKACTIVITY_CUSTEFUSE_L4_GICLK
Clock Domain State Transition Control	CM_CUSTEFUSE_CLKSTCTRL[1:0] CLKTRCTRL

3.6.6.3 Clock Domain Dependency

CD_CUSTEFUSE has no static or dynamic dependency with any other clock domain of the device.

3.6.6.4 Clock Domain Module Attributes

Table 3-96 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-102. CD_CUSTEFUSE Modules Clocks Association

Module	Clock	Clock Type
EFUSE_CTRL_CUST	CUSTEFUSE_SYS_GFCLK	Functional
	CUSTEFUSE_L4_GICLK	Interface

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Table 3-97 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-103. CD_CUSTEFUSE Modules Wake-Up Request

Module	Wake-Up Feature
EFUSE_CTRL_CUST	None

Table 3-98 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-104. CD_CUSTEFUSE Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
EFUSE_CTRL_CUST	Idle	CM_CUSTEFUSE_EFUSE_CTRL_CUST_CLKCTRL[17:16] IDLEST	Idle status

Table 3-99 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-105. CD_CUSTEFUSE Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
EFUSE_CTRL_CUST	Available	N/A	Available	CM_CUSTEFUSE_EFUSE_CTRL_CUST_CLKCTRL[1:0] MODULEMODE	Read/write

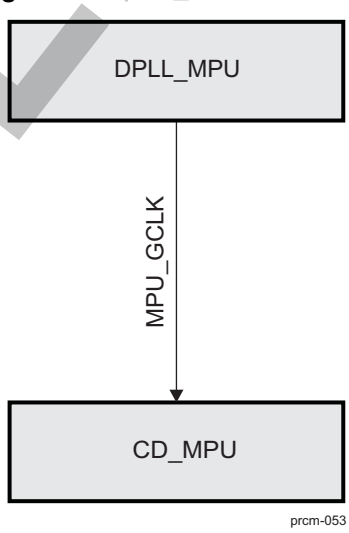
3.6.7 CD_MPU Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.7.1 Overview

Figure 3-59 is an overview of the clock domain.

Figure 3-59. CD_MPU Overview



3.6.7.2 Clock Domain Modes

Table 3-106 lists the clock domain modes supported by the clock domain.

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Table 3-106. CD_MPU Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Available	Available

Table 3-107 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-107. CD_MPU Control and Status Parameters

Parameter Name	Control/Status Bit Field
MPU_GCLK Clock Status	CM_MPU_CLKSTCTRL[8] CLKACTIVITY_MPU_GCLK
Clock Domain State Transition Control	CM_MPU_CLKSTCTRL[1:0] CLKTRCTRL

3.6.7.3 Clock Domain Dependency

CD_MPU has no module wake-up dependency with any other clock domain of the device.

3.6.7.3.1 Static Dependency

Table 3-108 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-108. CD_MPU Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_MPU_STATICDEP[3] ABE_STATDEP	Read/write
CD_CUSTEFUSE	Always disabled	CM_MPU_STATICDEP[17] CUSTEFUSE_STATDEP	Read only
CD_DSS	Disabled	CM_MPU_STATICDEP[8] DSS_STATDEP	Read/write
CD_IPU	Disabled	CM_MPU_STATICDEP[0] IPU_STATDEP	Read/write
CD_GPU	Disabled	CM_MPU_STATICDEP[10] GPU_STATDEP	Read/write
CD_CAM	Always disabled	CM_MPU_STATICDEP[9] CAM_STATDEP	Read only
CD_IVA	Disabled	CM_MPU_STATICDEP[2] IVA_STATDEP	Read/write
CD_L3_MAIN1	Enabled	CM_MPU_STATICDEP[5] L3MAIN1_STATDEP	Read/write
CD_L3_MAIN2	Enabled	CM_MPU_STATICDEP[6] L3MAIN2_STATDEP	Read/write
CD_L3INIT	Enabled	CM_MPU_STATICDEP[7] L3INIT_STATDEP	Read/write
CD_L4_CFG	Enabled	CM_MPU_STATICDEP[12] L4CFG_STATDEP	Read/write
CD_L4_PER	Enabled	CM_MPU_STATICDEP[13] L4PER_STATDEP	Read/write
CD_L4_SEC	Disabled	CM_MPU_STATICDEP[14] L4SEC_STATDEP	Read/write
CD_EMIF	Enabled	CM_MPU_STATICDEP[4] EMIF_STATDEP	Read/write
CD_DMA	Always disabled	CM_MPU_STATICDEP[11] SDMA_STATDEP	Read only
CD_DSP	Disabled	CM_MPU_STATICDEP[1] DSP_STATDEP	Read/write
CD_WKUPAON	Enabled	CM_MPU_STATICDEP[15] WKUPAON_STATDEP	Read/write

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Table 3-108. CD_MPU Static Dependency Association Parameters (continued)

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_COREAON	Always disabled	CM_MPU_STATICDEP[16] COREAON_STATDEP	Read only

3.6.7.3.2 Dynamic Dependency

Table 3-109 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-109. CD_MPU Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Always enabled	CM_MPU_DYNAMICDEP[3] ABE_DYNDEP	Read only
CD_L3_MAIN1	Always enabled	CM_MPU_DYNAMICDEP[5] L3_1_DYNDEP	Read only
CD_EMIF	Always enabled	CM_MPU_DYNAMICDEP[4] EMIF_DYNDEP	Read only

3.6.7.4 Clock Domain Module Attributes

Table 3-110 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-110. CD_MPU Modules Clocks Association

Module	Clock	Clock Type
MPU	MPU_GCLK	Interface and functional

Table 3-111 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-111. CD_MPU Modules Wake-Up Request

Module	Wake-Up Feature
MPU	Master wake-up request

Table 3-112 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-112. CD_MPU Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
MPU	Master/slave	CM_MPU_MPU_CLKCTRL[18] STBYST	Standby status
		CM_MPU_MPU_CLKCTRL[17:16] IDLEST	Idle status

Table 3-113 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-113. CD_MPU Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
MPU	N/A	Available	N/A	CM_MPU_MPU_CLKCTRL[1:0] MODULEMODE	Read only

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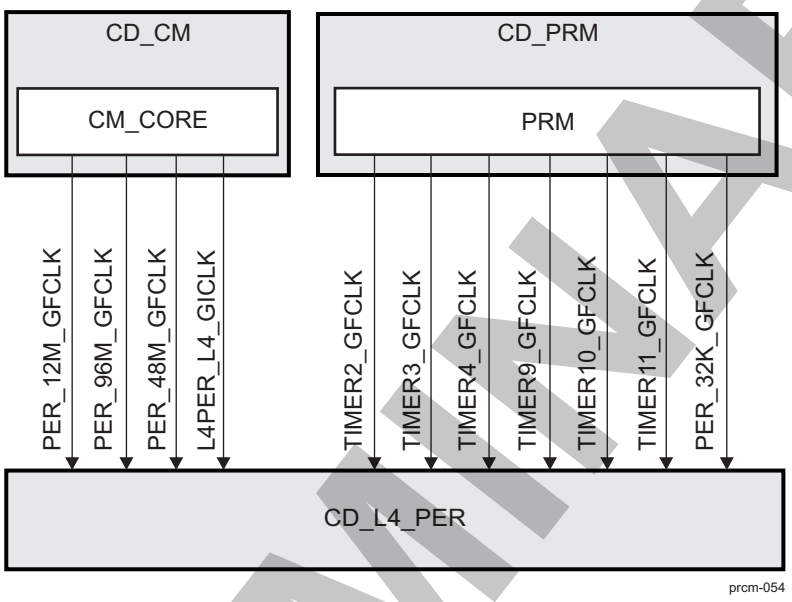
3.6.8 CD_L4_PER Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.8.1 Overview

Figure 3-60 is an overview of the clock domain.

Figure 3-60. CD_L4_PER Overview



3.6.8.2 Clock Domain Modes

Table 3-114 lists the clock domain modes supported by the clock domain.

Table 3-114. CD_L4_PER Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-115 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-115. CD_L4_PER Control and Status Parameters

Parameter Name	Control/Status Bit Field
TIMER10_GFCLK clock status	CM_L4PER_CLKSTCTRL[9] CLKACTIVITY_TIMER10_GFCLK
TIMER11_GFCLK clock status	CM_L4PER_CLKSTCTRL[10] CLKACTIVITY_TIMER11_GFCLK
TIMER2_GFCLK clock status	CM_L4PER_CLKSTCTRL[11] CLKACTIVITY_TIMER2_GFCLK
TIMER3_GFCLK clock status	CM_L4PER_CLKSTCTRL[12] CLKACTIVITY_TIMER3_GFCLK
TIMER4_GFCLK clock status	CM_L4PER_CLKSTCTRL[13] CLKACTIVITY_TIMER4_GFCLK
TIMER9_GFCLK clock status	CM_L4PER_CLKSTCTRL[14] CLKACTIVITY_TIMER9_GFCLK
L4PER_L4_GICLK clock status	CM_L4PER_CLKSTCTRL[8] CLKACTIVITY_L4PER_L4_GICLK
PER_12M_GFCLK clock status	CM_L4PER_CLKSTCTRL[15] CLKACTIVITY_PER_12M_GFCLK
PER_32K_GFCLK clock status	CM_L4PER_CLKSTCTRL[17] CLKACTIVITY_PER_32K_GFCLK
PER_48M_GFCLK clock status	CM_L4PER_CLKSTCTRL[18] CLKACTIVITY_PER_48M_GFCLK

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Table 3-115. CD_L4_PER Control and Status Parameters (continued)

Parameter Name	Control/Status Bit Field
PER_96M_GFCLK clock status	CM_L4PER_CLKSTCTRL[19] CLKACTIVITY_PER_96M_GFCLK
Clock Domain State Transition Control	CM_L4PER_CLKSTCTRL[1:0] CLKTRCTRL

3.6.8.3 Clock Domain Dependency

CD_L4_PER has no static dependency with any other clock domain of the device.

3.6.8.3.1 Dynamic Dependency

Table 3-116 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-116. CD_L4_PER Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L4_SEC	Always enabled	CM_L4PER_DYNAMICDEP[14] L4SEC_DYNDEP	Read only
CD_DSS	Always enabled	CM_L4PER_DYNAMICDEP[8] DSS_DYNDEP	Read only
CD_L3INIT	Always enabled	CM_L4PER_DYNAMICDEP[7] L3INIT_DYNDEP	Read only

3.6.8.3.2 Wake-Up Dependency

Table 3-117 lists the wake-up dependency settings for the modules of this clock domain.

Table 3-117. CD_L4_PER Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
TIMER10	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_TIMER10_WKDEP[0] WKUPDEP_TIMER10_MPU	Read/write
TIMER11	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_TIMER11_WKDEP[1] WKUPDEP_TIMER11_IPU	Read/write
TIMER11	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_TIMER11_WKDEP[0] WKUPDEP_TIMER11_MPU	Read/write
TIMER2	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_TIMER2_WKDEP[0] WKUPDEP_TIMER2_MPU	Read/write
TIMER3	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_TIMER3_WKDEP[1] WKUPDEP_TIMER3_IPU	Read/write
TIMER3	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_TIMER3_WKDEP[0] WKUPDEP_TIMER3_MPU	Read/write
TIMER4	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_TIMER4_WKDEP[1] WKUPDEP_TIMER4_IPU	Read/write

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Table 3-117. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
TIMER4	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_TIMER4_WKDEP[0] WKUPDEP_TIMER4_MPU	Read/write
TIMER9	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_TIMER9_WKDEP[1] WKUPDEP_TIMER9_IPU	Read/write
TIMER9	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_TIMER9_WKDEP[0] WKUPDEP_TIMER9_MPU	Read/write
GPIO2	CD_L4_PER	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_GPIO2_WKDEP[6] WKUPDEP_GPIO2_IRQ2_DSP	Read/write
GPIO2	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_GPIO2_WKDEP[1] WKUPDEP_GPIO2_IRQ1_IPU	Read/write
GPIO2	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_GPIO2_WKDEP[0] WKUPDEP_GPIO2_IRQ1_MPU	Read/write
GPIO3	CD_L4_PER	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_GPIO3_WKDEP[6] WKUPDEP_GPIO3_IRQ2_DSP	Read/write
GPIO3	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_GPIO3_WKDEP[0] WKUPDEP_GPIO3_IRQ1_MPU	Read/write
GPIO4	CD_L4_PER	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_GPIO4_WKDEP[6] WKUPDEP_GPIO4_IRQ2_DSP	Read/write
GPIO4	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_GPIO4_WKDEP[0] WKUPDEP_GPIO4_IRQ1_MPU	Read/write
GPIO5	CD_L4_PER	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_GPIO5_WKDEP[6] WKUPDEP_GPIO5_IRQ2_DSP	Read/write
GPIO5	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_GPIO5_WKDEP[0] WKUPDEP_GPIO5_IRQ1_MPU	Read/write
GPIO6	CD_L4_PER	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_GPIO6_WKDEP[6] WKUPDEP_GPIO6_IRQ2_DSP	Read/write
GPIO6	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_GPIO6_WKDEP[0] WKUPDEP_GPIO6_IRQ1_MPU	Read/write
GPIO7	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_GPIO7_WKDEP[0] WKUPDEP_GPIO7_IRQ1_MPU	Read/write

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Table 3-117. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
GPIO8	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Enabled	PM_L4PER_GPIO8_WKDEP[0] WKUPDEP_GPIO8_IRQ1_MPU	Read/write
I2C1	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Enabled	PM_L4PER_I2C1_WKDEP[7] WKUPDEP_I2C1_DMA_SDMA	Read/write
I2C1	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_I2C1_WKDEP[1] WKUPDEP_I2C1_IRQ_IPU	Read/write
I2C1	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_I2C1_WKDEP[0] WKUPDEP_I2C1_IRQ_MPU	Read/write
I2C2	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Enabled	PM_L4PER_I2C2_WKDEP[7] WKUPDEP_I2C2_DMA_SDMA	Read/write
I2C2	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_I2C2_WKDEP[1] WKUPDEP_I2C2_IRQ_IPU	Read/write
I2C2	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_I2C2_WKDEP[0] WKUPDEP_I2C2_IRQ_MPU	Read/write
I2C3	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Enabled	PM_L4PER_I2C3_WKDEP[7] WKUPDEP_I2C3_DMA_SDMA	Read/write
I2C3	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_I2C3_WKDEP[1] WKUPDEP_I2C3_IRQ_IPU	Read/write
I2C3	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_I2C3_WKDEP[0] WKUPDEP_I2C3_IRQ_MPU	Read/write
I2C4	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Enabled	PM_L4PER_I2C4_WKDEP[7] WKUPDEP_I2C4_DMA_SDMA	Read/write
I2C4	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_I2C4_WKDEP[1] WKUPDEP_I2C4_IRQ_IPU	Read/write
I2C4	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_I2C4_WKDEP[0] WKUPDEP_I2C4_IRQ_MPU	Read/write
I2C5	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_I2C5_WKDEP[0] WKUPDEP_I2C5_IRQ_MPU	Read/write
MCSPI1	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI1_WKDEP[3] WKUPDEP_MCSPI1_SDMA	Read/write

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Table 3-117. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
MCSPI1	CD_L4_PER	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI1_WKDEP[2] WKUPDEP_MCSPI1_DSP	Read/write
MCSPI1	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI1_WKDEP[1] WKUPDEP_MCSPI1_IPU	Read/write
MCSPI1	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI1_WKDEP[0] WKUPDEP_MCSPI1_MPU	Read/write
MCSPI2	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI2_WKDEP[3] WKUPDEP_MCSPI2_SDMA	Read/write
MCSPI2	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI2_WKDEP[1] WKUPDEP_MCSPI2_IPU	Read/write
MCSPI2	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI2_WKDEP[0] WKUPDEP_MCSPI2_MPU	Read/write
MCSPI3	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI3_WKDEP[3] WKUPDEP_MCSPI3_SDMA	Read/write
MCSPI3	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI3_WKDEP[0] WKUPDEP_MCSPI3_MPU	Read/write
MCSPI4	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI4_WKDEP[3] WKUPDEP_MCSPI4_SDMA	Read/write
MCSPI4	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_MCSPI4_WKDEP[0] WKUPDEP_MCSPI4_MPU	Read/write
MMC3	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_MMC3_WKDEP[3] WKUPDEP_MMC3_SDMA	Read/write
MMC3	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_MMC3_WKDEP[1] WKUPDEP_MMC3_IPU	Read/write
MMC3	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_MMC3_WKDEP[0] WKUPDEP_MMC3_MPU	Read/write
MMC4	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_MMC4_WKDEP[3] WKUPDEP_MMC4_SDMA	Read/write
MMC4	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_MMC4_WKDEP[0] WKUPDEP_MMC4_MPU	Read/write

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Table 3-117. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
MMC5	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_MMC5_WKDEP[3] WKUPDEP_MMC5_SDMA	Read/write
MMC5	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_MMC5_WKDEP[0] WKUPDEP_MMC5_MPU	Read/write
UART1	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_UART1_WKDEP[3] WKUPDEP_UART1_SDMA	Read/write
UART1	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_UART1_WKDEP[0] WKUPDEP_UART1_MPU	Read/write
UART2	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_UART2_WKDEP[3] WKUPDEP_UART2_SDMA	Read/write
UART2	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_UART2_WKDEP[0] WKUPDEP_UART2_MPU	Read/write
UART3	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_UART3_WKDEP[3] WKUPDEP_UART3_SDMA	Read/write
UART3	CD_L4_PER	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_UART3_WKDEP[2] WKUPDEP_UART3_DSP	Read/write
UART3	CD_L4_PER	CD_IPU, CD_L3_MAIN2	Disabled	PM_L4PER_UART3_WKDEP[1] WKUPDEP_UART3_IPU	Read/write
UART3	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_UART3_WKDEP[0] WKUPDEP_UART3_MPU	Read/write
UART4	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_UART4_WKDEP[3] WKUPDEP_UART4_SDMA	Read/write
UART4	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_UART4_WKDEP[0] WKUPDEP_UART4_MPU	Read/write
UART5	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_UART5_WKDEP[3] WKUPDEP_UART5_SDMA	Read/write
UART5	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_UART5_WKDEP[0] WKUPDEP_UART5_MPU	Read/write
UART6	CD_L4_PER	CD_DMA, CD_L3_MAIN2	Disabled	PM_L4PER_UART6_WKDEP[3] WKUPDEP_UART6_SDMA	Read/write

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Table 3-117. CD_L4_PER Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
UART6	CD_L4_PER	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_L4PER_UART6_WKDEP[0] WKUPDEP_UART6_MPU	Read/write

3.6.8.4 Clock Domain Module Attributes

Table 3-118 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-118. CD_L4_PER Modules Clocks Association

Module	Clock	Clock Type
TIMER10	TIMER10_GFCLK	Functional
	L4PER_L4_GICLK	Interface
TIMER11	TIMER11_GFCLK	Functional
	L4PER_L4_GICLK	Interface
TIMER2	TIMER2_GFCLK	Functional
	L4PER_L4_GICLK	Interface
TIMER3	TIMER3_GFCLK	Functional
	L4PER_L4_GICLK	Interface
TIMER4	TIMER4_GFCLK	Functional
	L4PER_L4_GICLK	Interface
TIMER9	TIMER9_GFCLK	Functional
	L4PER_L4_GICLK	Interface
ELM	L4PER_L4_GICLK	Interface
GPIO2	L4PER_L4_GICLK	Interface
	PER_32K_GFCLK	Functional
GPIO3	L4PER_L4_GICLK	Interface
	PER_32K_GFCLK	Functional
GPIO4	L4PER_L4_GICLK	Interface
	PER_32K_GFCLK	Functional
GPIO5	L4PER_L4_GICLK	Interface
	PER_32K_GFCLK	Functional
GPIO6	L4PER_L4_GICLK	Interface
	PER_32K_GFCLK	Functional
GPIO7	L4PER_L4_GICLK	Interface
	PER_32K_GFCLK	Functional
GPIO8	L4PER_L4_GICLK	Interface
	PER_32K_GFCLK	Functional
HDQ1W	L4PER_L4_GICLK	Interface
	PER_12M_GFCLK	Functional
I2C1	L4PER_L4_GICLK	Interface
	PER_96M_GFCLK	Functional
I2C2	L4PER_L4_GICLK	Interface
	PER_96M_GFCLK	Functional
I2C3	L4PER_L4_GICLK	Interface
	PER_96M_GFCLK	Functional
I2C4	L4PER_L4_GICLK	Interface

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Table 3-118. CD_L4_PER Modules Clocks Association (continued)

Module	Clock	Clock Type
	PER_96M_GFCLK	Functional
I2C5	L4PER_L4_GICLK	Interface
	PER_96M_GFCLK	Functional
L4_PER interconnect	L4PER_L4_GICLK	Interface
MCSPI1	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
MCSPI2	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
MCSPI3	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
MCSPI4	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
MMC3	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
MMC4	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
MMC5	L4PER_L4_GICLK	Interface
	PER_96M_GFCLK	Functional
UART1	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
UART2	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
UART3	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
UART4	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
UART5	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional
UART6	L4PER_L4_GICLK	Interface
	PER_48M_GFCLK	Functional

Table 3-119 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-119. CD_L4_PER Modules Wake-Up Request

Module	Wake-Up Feature
TIMER10	Slave wake-up request (MPU-IRQ)
TIMER11	Slave wake-up request (MPU-IRQ, IPU-IRQ)
TIMER2	Slave wake-up request (MPU-IRQ)
TIMER3	Slave wake-up request (MPU-IRQ, IPU-IRQ)
TIMER4	Slave wake-up request (MPU-IRQ, IPU-IRQ)
TIMER9	Slave wake-up request (MPU-IRQ, IPU-IRQ)
ELM	None
GPIO2	Slave wake-up request (MPU-IRQ, IPU-IRQ, DSP-IRQ)
GPIO3	Slave wake-up request (MPU-IRQ, DSP-IRQ)
GPIO4	Slave wake-up request (MPU-IRQ, DSP-IRQ)
GPIO5	Slave wake-up request (MPU-IRQ, DSP-IRQ)
GPIO6	Slave wake-up request (MPU-IRQ, DSP-IRQ)

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Table 3-119. CD_L4_PER Modules Wake-Up Request (continued)

Module	Wake-Up Feature
GPIO7	Slave wake-up request (MPU-IRQ)
GPIO8	Slave wake-up request (MPU-IRQ)
HDQ1W	None
I2C1	Slave wake-up request (MPU-IRQ, IPU-IRQ, DMA_SYSTEM-DMA)
I2C2	Slave wake-up request (MPU-IRQ, IPU-IRQ, DMA_SYSTEM-DMA)
I2C3	Slave wake-up request (MPU-IRQ, IPU-IRQ, DMA_SYSTEM-DMA)
I2C4	Slave wake-up request (MPU-IRQ, IPU-IRQ, DMA_SYSTEM-DMA)
I2C5	Slave wake-up request (MPU-IRQ)
L4_PER interconnect	None
MCSPI1	Slave wake-up request (MPU-IRQ, IPU-IRQ, DSP-IRQ, DMA_SYSTEM-DMA)
MCSPI2	Slave wake-up request (MPU-IRQ, IPU-IRQ, DMA_SYSTEM-DMA)
MCSPI3	Slave wake-up request (MPU-IRQ, DMA_SYSTEM-DMA)
MCSPI4	Slave wake-up request (MPU-IRQ, DMA_SYSTEM -DMA)
MMC3	Slave wake-up request (MPU-IRQ, IPU-IRQ, DMA_SYSTEM-DMA)
MMC4	Slave wake-up request (MPU-IRQ, DMA_SYSTEM -DMA)
MMC5	Slave wake-up request (MPU-IRQ, DMA_SYSTEM-DMA)
UART1	Slave wake-up request (MPU-IRQ, DMA_SYSTEM-DMA)
UART2	Slave wake-up request (MPU-IRQ, DMA_SYSTEM-DMA)
UART3	Slave wake-up request (MPU-IRQ, IPU -IRQ, DSP-IRQ and DMA, DMA_SYSTEM-DMA)
UART4	Slave wake-up request (MPU-IRQ, DMA_SYSTEM-DMA)
UART5	Slave wake-up request (MPU-IRQ, DMA_SYSTEM-DMA)
UART6	Slave wake-up request (MPU-IRQ, DMA_SYSTEM-DMA)

Table 3-120 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-120. CD_L4_PER Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
TIMER10	Slave	CM_L4PER_TIMER10_CLKCTRL[17:16] IDLEST	Idle status
TIMER11	Slave	CM_L4PER_TIMER11_CLKCTRL[17:16] IDLEST	Idle status
TIMER2	Slave	CM_L4PER_TIMER2_CLKCTRL[17:16] IDLEST	Idle status
TIMER3	Slave	CM_L4PER_TIMER3_CLKCTRL[17:16] IDLEST	Idle status
TIMER4	Slave	CM_L4PER_TIMER4_CLKCTRL[17:16] IDLEST	Idle status
TIMER9	Slave	CM_L4PER_TIMER9_CLKCTRL[17:16] IDLEST	Idle status
ELM	Slave	CM_L4PER_ELM_CLKCTRL[17:16] IDLEST	Idle status
GPIO2	Slave	CM_L4PER_GPIO2_CLKCTRL[17:16] IDLEST	Idle status
GPIO3	Slave	CM_L4PER_GPIO3_CLKCTRL[17:16] IDLEST	Idle status
GPIO4	Slave	CM_L4PER_GPIO4_CLKCTRL[17:16] IDLEST	Idle status
GPIO5	Slave	CM_L4PER_GPIO5_CLKCTRL[17:16] IDLEST	Idle status
GPIO6	Slave	CM_L4PER_GPIO6_CLKCTRL[17:16] IDLEST	Idle status
GPIO7	Slave	CM_L4PER_GPIO7_CLKCTRL[17:16] IDLEST	Idle status

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Table 3-120. CD_L4_PER Modules Clock-Management Modes and Control (continued)

Module	Clock-Management Protocol	Status Bit Field	Role
GPIO8	Slave	CM_L4PER_GPIO8_CLKCTRL[17:16] IDLEST	Idle status
HDQ1W	Slave	CM_L4PER_HDQ1W_CLKCTRL[17:16] IDLEST	Idle status
I2C1	Slave	CM_L4PER_I2C1_CLKCTRL[17:16] IDLEST	Idle status
I2C2	Slave	CM_L4PER_I2C1_CLKCTRL[17:16] IDLEST	Idle status
I2C3	Slave	CM_L4PER_I2C3_CLKCTRL[17:16] IDLEST	Idle status
I2C4	Slave	CM_L4PER_I2C4_CLKCTRL[17:16] IDLEST	Idle status
I2C5	Slave	CM_L4PER_I2C5_CLKCTRL[17:16] IDLEST	Idle status
L4_PER interconnect	Slave	CM_L4PER_L4_PER_CLKCTRL[17:16] IDLEST	Idle status
MCSPI1	Slave	CM_L4PER_MCSPI1_CLKCTRL[17:16] IDLEST	Idle status
MCSPI2	Slave	CM_L4PER_MCSPI2_CLKCTRL[17:16] IDLEST	Idle status
MCSPI3	Slave	CM_L4PER_MCSPI3_CLKCTRL[17:16] IDLEST	Idle status
MCSPI4	Slave	CM_L4PER_MCSPI4_CLKCTRL[17:16] IDLEST	Idle status
MMC3	Slave	CM_L4PER_MMC3_CLKCTRL[17:16] IDLEST	Idle status
MMC4	Slave	CM_L4PER_MMC4_CLKCTRL[17:16] IDLEST	Idle status
MMC5	Slave	CM_L4PER_MMC5_CLKCTRL[17:16] IDLEST	Idle status
UART1	Slave	CM_L4PER_UART1_CLKCTRL[17:16] IDLEST	Idle status
UART2	Slave	CM_L4PER_UART2_CLKCTRL[17:16] IDLEST	Idle status
UART3	Slave	CM_L4PER_UART3_CLKCTRL[17:16] IDLEST	Idle status
UART4	Slave	CM_L4PER_UART4_CLKCTRL[17:16] IDLEST	Idle status
UART5	Slave	CM_L4PER_UART5_CLKCTRL[17:16] IDLEST	Idle status
UART6	Slave	CM_L4PER_UART6_CLKCTRL[17:16] IDLEST	Idle status

Table 3-121 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-121. CD_L4_PER Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
TIMER10	Available	N/A	Available	CM_L4PER_TIMER10_CLKCTRL[1:0] MODULEMODE	Read/write
TIMER11	Available	N/A	Available	CM_L4PER_TIMER11_CLKCTRL[1:0] MODULEMODE	Read/write
TIMER2	Available	N/A	Available	CM_L4PER_TIMER2_CLKCTRL[1:0] MODULEMODE	Read/write
TIMER3	Available	N/A	Available	CM_L4PER_TIMER3_CLKCTRL[1:0] MODULEMODE	Read/write
TIMER4	Available	N/A	Available	CM_L4PER_TIMER4_CLKCTRL[1:0] MODULEMODE	Read/write
TIMER9	Available	N/A	Available	CM_L4PER_TIMER9_CLKCTRL[1:0] MODULEMODE	Read/write
ELM	N/A	Available	N/A	CM_L4PER_ELM_CLKCTRL[1:0] MODULEMODE	Read only
GPIO2	Available	Available	N/A	CM_L4PER_GPIO2_CLKCTRL[1:0] MODULEMODE	Read/write

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Table 3-121. CD_L4_PER Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
GPIO3	Available	Available	N/A	CM_L4PER_GPIO3_CLKCTRL[1:0] MODULEMODE	Read/write
GPIO4	Available	Available	N/A	CM_L4PER_GPIO4_CLKCTRL[1:0] MODULEMODE	Read/write
GPIO5	Available	Available	N/A	CM_L4PER_GPIO5_CLKCTRL[1:0] MODULEMODE	Read/write
GPIO6	Available	Available	N/A	CM_L4PER_GPIO6_CLKCTRL[1:0] MODULEMODE	Read/write
GPIO7	Available	Available	N/A	CM_L4PER_GPIO7_CLKCTRL[1:0] MODULEMODE	Read/write
GPIO8	Available	Available	N/A	CM_L4PER_GPIO8_CLKCTRL[1:0] MODULEMODE	Read/write
HDQ1W	Available	N/A	Available	CM_L4PER_HDQ1W_CLKCTRL[1:0] MODULEMODE	Read/write
I2C1	Available	N/A	Available	CM_L4PER_I2C1_CLKCTRL[1:0] MODULEMODE	Read/write
I2C2	Available	N/A	Available	CM_L4PER_I2C2_CLKCTRL[1:0] MODULEMODE	Read/write
I2C3	Available	N/A	Available	CM_L4PER_I2C3_CLKCTRL[1:0] MODULEMODE	Read/write
I2C4	Available	N/A	Available	CM_L4PER_I2C4_CLKCTRL[1:0] MODULEMODE	Read/write
I2C5	Available	N/A	Available	CM_L4PER_I2C5_CLKCTRL[1:0] MODULEMODE	Read/write
L4_PER interconnect	N/A	Available	N/A	CM_L4PER_L4_PER_CLKCTRL[1:0] MODULEMODE	Read only
MCSPI1	Available	N/A	Available	CM_L4PER_MCSPI1_CLKCTRL[1:0] MODULEMODE	Read/write
MCSPI2	Available	N/A	Available	CM_L4PER_MCSPI2_CLKCTRL[1:0] MODULEMODE	Read/write
MCSPI3	Available	N/A	Available	CM_L4PER_MCSPI3_CLKCTRL[1:0] MODULEMODE	Read/write
MCSPI4	Available	N/A	Available	CM_L4PER_MCSPI4_CLKCTRL[1:0] MODULEMODE	Read/write
MMC3	Available	N/A	Available	CM_L4PER_MMC3_CLKCTRL[1:0] MODULEMODE	Read/write
MMC4	Available	N/A	Available	CM_L4PER_MMC4_CLKCTRL[1:0] MODULEMODE	Read/write
MMC5	Available	N/A	Available	CM_L4PER_MMC5_CLKCTRL[1:0] MODULEMODE	Read/write

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Table 3-121. CD_L4_PER Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
UART1	Available	N/A	Available	CM_L4PER_UART1_CLKCTRL[1:0] MODULEMODE	Read/write
UART2	Available	N/A	Available	CM_L4PER_UART2_CLKCTRL[1:0] MODULEMODE	Read/write
UART3	Available	N/A	Available	CM_L4PER_UART3_CLKCTRL[1:0] MODULEMODE	Read/write
UART4	Available	N/A	Available	CM_L4PER_UART4_CLKCTRL[1:0] MODULEMODE	Read/write
UART5	Available	N/A	Available	CM_L4PER_UART5_CLKCTRL[1:0] MODULEMODE	Read/write

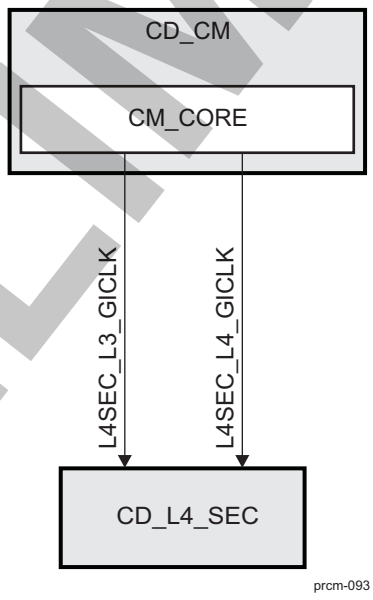
3.6.9 CD_L4_SEC Clock Domain

This section identifies the modes supported by the clock domain, the associated control, and status bits. It also identifies the dependencies of the domain with the other clock domains of the device.

3.6.9.1 Overview

Figure 3-61 shows an overview of the clock domain.

Figure 3-61. CD_L4_SEC Overview



3.6.9.2 Clock Domain Modes

Table 3-122 lists the clock domain modes supported by the clock domain.

Table 3-122. CD_L4_SEC Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

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Table 3-123 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-123. CD_L4_SEC Control and Status Parameters

Parameter Name	Control/Status Bit Field
L4SEC_L3_GICLK clock status	CM_L4SEC_CLKSTCTRL[8] CLKACTIVITY_L4SEC_L3_GICLK
L4SEC_L4_GICLK clock status	CM_L4SEC_CLKSTCTRL[9] CLKACTIVITY_L4SEC_L4_GICLK
Clock Domain State Transition Control	CM_L4SEC_CLKSTCTRL[1:0] CLKTRCTRL

3.6.9.3 Clock Domain Dependency

CD_L4_SEC has no module wake-up dependency with any other clock domain of the device.

3.6.9.3.1 Static Dependency

Table 3-124 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-124. CD_L4_SEC Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L4_PER	Disabled	CM_L4SEC_STATICDEP[13] L4PER_STATDEP	Read/Write
CD_L3_MAIN2	Always enabled	CM_L4SEC_STATICDEP[6] L3MAIN2_STATDEP	Read only
CD_L3_MAIN1	Disabled	CM_L4SEC_STATICDEP[5] L3MAIN1_STATDEP	Read/Write
CD_EMIF	Disabled	CM_L4SEC_STATICDEP[4] EMIF_STATDEP	Read/Write

3.6.9.3.2 Dynamic Dependency

Table 3-125 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-125. CD_L4_SEC Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN2	Always disabled	CM_L4SEC_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only

3.6.9.4 Clock Domain Module Attributes

Table 3-126 lists the clocks received by each module of the clock domain and the role (that is, functional clock or interface clock).

Table 3-126. CD_L4_SEC Modules Clocks Association

Module	Clock	Clock Type
AES1	L4SEC_L3_GICLK	Interface
AES2	L4SEC_L3_GICLK	Interface
SHA2MD5	L4SEC_L3_GICLK	Interface
CryptoDMA	L4SEC_L3_GICLK	Interface and Functional
	L4SEC_L4_GICLK	Interface
DES3DES	L4SEC_L4_GICLK	Interface
RNG	L4SEC_L4_GICLK	Interface
FPKA	L4SEC_L4_GICLK	Interface and Functional

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Table 3-127 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-127. CD_L4_SEC Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
AES1	Slave	CM_L4SEC_AES1_CLKCTRL[17:16] IDLEST	Idle status
AES2	Slave	CM_L4SEC_AES2_CLKCTRL[17:16] IDLEST	Idle status
SHA2MD5	Slave	CM_L4SEC_SHA2MD5_CLKCTRL[17:16] IDLEST	Idle status
CryptoDMA	Master/Slave	CM_L4SEC_DMA_CRYPTO_CLKCTRL[18] STBYST	Standby status
		CM_L4SEC_DMA_CRYPTO_CLKCTRL [17:16] IDLEST	Idle status
DES3DES	Slave	CM_L4SEC_DES3DES_CLKCTRL[17:16] IDLEST	Idle status
RNG	Slave	CM_L4SEC_RNG_CLKCTRL[17:16] IDLEST	Idle status
FPKA	Slave	CM_L4SEC_FPKA_CLKCTRL[17:16] IDLEST	Idle status

NOTE: PRCM insures that DMA_CRYPTO idle sequence start only when AES1, AES2, SHA2MD5 and DES3DES modules are already in Idle state.

Table 3-128 lists the supported slave clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-128. CD_L4_SEC Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
AES1	Available	Available	N/A	CM_L4SEC_AES1_CLKCTRL[1:0] MODULEMODE	Read/Write
AES2	Available	Available	N/A	CM_L4SEC_AES2_CLKCTRL[1:0] MODULEMODE	Read/Write
SHA2MD5	Available	Available	N/A	CM_L4SEC_SHA2MD5_CLKCTRL[1:0] MODULEMODE	Read/Write
DMA_CRYPTO	N/A	Available	N/A	CM_L4SEC_DMA_CRYPTO_CLKCTRL[1:0] MODULEMODE	Read only
DES3DES	Available	Available	N/A	CM_L4SEC_DES3DES_CLKCTRL[1:0] MODULEMODE	Read/Write
RNG	Available	Available	N/A	CM_L4SEC_RNG_CLKCTRL[1:0] MODULEMODE	Read/Write
FPKA	Available	N/A	Available	CM_L4SEC_FPKA_CLKCTRL[1:0] MODULEMODE	Read/Write

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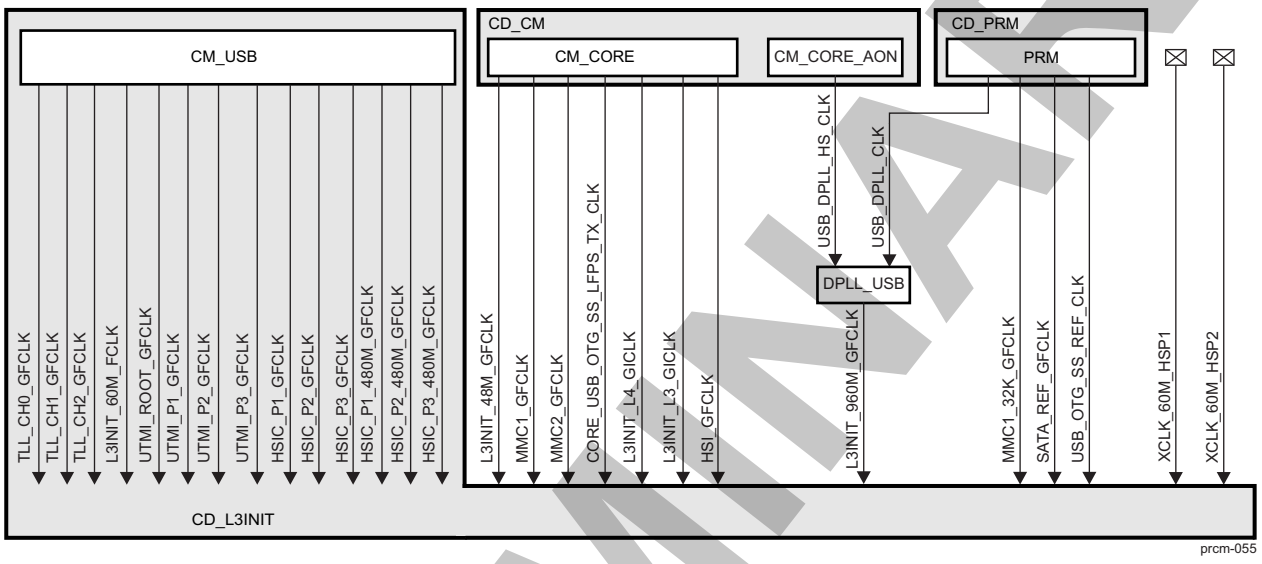
3.6.10 CD_L3INIT Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.10.1 Overview

Figure 3-62 is an overview of the clock domain.

Figure 3-62. CD_L3INIT Overview



3.6.10.2 Clock Domain Modes

Table 3-129 lists the clock domain modes supported by the clock domain.

Table 3-129. CD_L3INIT Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-130 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-130. CD_L3INIT Control and Status Parameters

Parameter Name	Control/Status Bit Field
HSIC_P1_480M_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[20] CLKACTIVITY_HSIC_P1_480M_GFCLK
HSIC_P1_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[26] CLKACTIVITY_HSIC_P1_GFCLK
HSIC_P2_480M_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[21] CLKACTIVITY_HSIC_P2_480M_GFCLK
HSIC_P2_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[27] CLKACTIVITY_HSIC_P2_GFCLK
HSIC_P3_480M_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[6] CLKACTIVITY_HSIC_P3_480M_GFCLK
HSIC_P3_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[7] CLKACTIVITY_HSIC_P3_GFCLK
USB_OTG_SS_REF_CLK Clock Status	CM_L3INIT_CLKSTCTRL[31] CLKACTIVITY_USB_OTG_SS_REF_CLK
USB_OTG_SS_REF_CLK Clock Control	CM_L3INIT_USB_OTG_SS_CLKCTRL[8] OPTFCLKEN_REFCLK960M
USB_DPLL_HS_CLK Clock Status	CM_L3INIT_CLKSTCTRL[15] CLKACTIVITY_USB_DPLL_HS_CLK

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Table 3-130. CD_L3INIT Control and Status Parameters (continued)

Parameter Name	Control/Status Bit Field
USB_DPLL_CLK Clock Status	CM_L3INIT_CLKSTCTRL[14] CLKACTIVITY_USB_DPLL_CLK
L3INIT_48M_GFCLK Clock Statuss	CM_L3INIT_CLKSTCTRL[12] CLKACTIVITY_L3INIT_48M_GFCLK
L3INIT_60M_P1_FCLK Clock Status	CM_L3INIT_CLKSTCTRL[28] CLKACTIVITY_L3INIT_60M_P1_FCLK
L3INIT_60M_P2_FCLK Clock Status	CM_L3INIT_CLKSTCTRL[29] CLKACTIVITY_L3INIT_60M_P2_FCLK
HSI_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[16] CLKACTIVITY_HSI_GFCLK
MMC1_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[17] CLKACTIVITY_MMC1_GFCLK
MMC1_32K_GFCLK Optional functional clock control	CM_L3INIT_MMC1_CLKCTRL[8] OPTFCLKEN_32KHZ_CLK
MMC1_32K_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[2] CLKACTIVITY_MMC1_32K_GFCLK
MMC2_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[18] CLKACTIVITY_MMC2_GFCLK
SATA_REF_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[19] CLKACTIVITY_SATA_REF_GFCLK
L3INIT_L3_GICLK Clock Status	CM_L3INIT_CLKSTCTRL[8] CLKACTIVITY_L3INIT_L3_GICLK
L3INIT_L4_GICLK Clock Status	CM_L3INIT_CLKSTCTRL[9] CLKACTIVITY_L3INIT_L4_GICLK
TLL_CH0_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[22] CLKACTIVITY_TLL_CH0_GFCLK
TLL_CH1_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[23] CLKACTIVITY_TLL_CH1_GFCLK
TLL_CH2_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[24] CLKACTIVITY_TLL_CH2_GFCLK
UTMI_ROOT_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[25] CLKACTIVITY_UTMI_ROOT_GFCLK
UTMI_P3_GFCLK Clock Status	CM_L3INIT_CLKSTCTRL[30] CLKACTIVITY_UTMI_P3_GFCLK
XCLK60MHSP2 Clock Status	CM_L3INIT_CLKSTCTRL[4] CLKACTIVITY_PAD_XCLK60MHSP2
L3INIT_USB_OTG_SS_LFPS_TX_FCLK Clock Status	CM_L3INIT_CLKSTCTRL[11] CLKACTIVITY_L3INIT_USB_OTG_SS_LFPS_TX_FCLK
Clock Domain State Transition Control	CM_L3INIT_CLKSTCTRL[1:0] CLKTRCTRL

3.6.10.3 Clock Domain Dependency

3.6.10.3.1 Static Dependency

Table 3-131 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-131. CD_L3INIT Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_L3INIT_STATICDEP[3] ABE_STATDEP	Read/write
CD_IVA	Disabled	CM_L3INIT_STATICDEP[2] IVA_STATDEP	Read/write
CD_L3_MAIN1	Always enabled	CM_L3INIT_STATICDEP[5] L3MAIN1_STATDEP	Read only
CD_L3_MAIN2	Always enabled	CM_L3INIT_STATICDEP[6] L3_MAIN2_STATDEP	Read only
CD_L4_CFG	Disabled	CM_L3INIT_STATICDEP[12] L4CFG_STATDEP	Read/write
CD_L4_PER	Disabled	CM_L3INIT_STATICDEP[13] L4PER_STATDEP	Read/write
CD_L4_SEC	Disabled	CM_L3INIT_STATICDEP[14] L4SEC_STATDEP	Read/write

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Table 3-131. CD_L3INIT Static Dependency Association Parameters (continued)

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_EMIF	Disabled	CM_L3INIT_STATICDEP[4] EMIF_STATDEP	Read/write
CD_WKUPAON	Disabled	CM_L3INIT_STATICDEP[15] WKUPAON_STATDEP	Read/write

3.6.10.3.2 Dynamic Dependency

Table 3-132 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-132. CD_L3INIT Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN1	Always disabled	CM_L3INIT_DYNAMICDEP[5] L3MAIN1_DYNDEP	Read only
CD_L3_MAIN2	Always disabled	CM_L3INIT_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only

3.6.10.3.3 Wake-Up Dependency

Table 3-133 lists the wake-up dependency settings for the modules of this clock in the clock domain.

Table 3-133. CD_L3INIT Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
HSI	CD_L3INIT	CD_DSP, CD_L3_MAIN1, CD_L4_CFG	Enabled	PM_L3INIT_HSI_WKDEP[6] WKUPDEP_HSI_DSP_DSP	Read/write
HSI	CD_L3INIT	CD_IPU, CD_L3_MAIN2, CD_L3_MAIN1, CD_L4_CFG	Disabled	PM_L3INIT_HSI_WKDEP[1] WKUPDEP_HSI_MCU_IPU	Read/write
HSI	CD_L3INIT	CD_MPU, CD_L3_MAIN1, CD_L4_CFG	Disabled	PM_L3INIT_HSI_WKDEP[0] WKUPDEP_HSI_MCU_MPU	Read/write
MMC1	CD_L3INIT	CD_DMA, CD_L3_MAIN2, CD_L4_PER	Disabled	PM_L3INIT_MMC1_WKDEP[3] WKUPDEP_MMC1_SDMA	Read/write
MMC1	CD_L3INIT	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2, CD_L4_PER	Disabled	PM_L3INIT_MMC1_WKDEP[2] WKUPDEP_MMC1_DSP	Read/write
MMC1	CD_L3INIT	CD_IPU, CD_L3_MAIN2, CD_L4_PER	Disabled	PM_L3INIT_MMC1_WKDEP[1] WKUPDEP_MMC1_IPU	Read/write
MMC1	CD_L3INIT	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2, CD_L4_PER	Disabled	PM_L3INIT_MMC1_WKDEP[0] WKUPDEP_MMC1_MPU	Read/write
MMC2	CD_L3INIT	CD_DMA, CD_L3_MAIN2, CD_L4_PER	Disabled	PM_L3INIT_MMC2_WKDEP[3] WKUPDEP_MMC2_SDMA	Read/write

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Table 3-133. CD_L3INIT Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
MMC2	CD_L3INIT	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2, CD_L4_PER	Disabled	PM_L3INIT_MMC2_WKDEP[2] WKUPDEP_MMC2_DSP	Read/write
MMC2	CD_L3INIT	CD_IPU, CD_L3_MAIN2, CD_L4_PER	Disabled	PM_L3INIT_MMC2_WKDEP[1] WKUPDEP_MMC2_IPU	Read/write
MMC2	CD_L3INIT	CD_MPU, CD_L3_MAIN1, CD_L4_PER	Disabled	PM_L3INIT_MMC2_WKDEP[0] WKUPDEP_MMC2_MPU	Read/write
USB_OTG_SS	CD_L3INIT	CD_IPU, CD_L3_MAIN1, CD_L3_MAIN2, CD_L4_CFG	Disabled	PM_L3INIT_USB_OTG_SS_WKDEP[1] WKUPDEP_USB_OTG_SS_IPU	Read/write
USB_OTG_SS	CD_L3INIT	CD_MPU, CD_L3_MIAN1, CD_L4_CFG	Disabled	PM_L3INIT_USB_OTG_SS_WKDEP[0] WKUPDEP_USB_OTG_SS_MPU	Read/write
USB_HOST_HS	CD_L3INIT	CD_IPU, CD_L3_MAIN1, CD_L3_MAIN2, CD_L4_CFG	Disabled	PM_L3INIT_USB_HOST_HS_WKDEP[1] WKUPDEP_USB_HOST_HS_IPU	Read/write
USB_HOST_HS	CD_L3INIT	CD_MPU, CD_L3_MAIN1, CD_L4_CFG	Disabled	PM_L3INIT_USB_HOST_HS_WKDEP[0] WKUPDEP_USB_HOST_HS_MPU	Read/write
USB_TLL_HS	CD_L3INIT	CD_IPU, CD_L3_MAIN1, CD_L3_MAIN2, CD_L4_CFG	Disabled	PM_L3INIT_USB_TLL_HS_WKDEP[1] WKUPDEP_USB_TLL_HS_IPU	Read/write
USB_TLL_HS	CD_L3INIT	CD_MPU, CD_L3_MAIN1, CD_L4_CFG	Disabled	PM_L3INIT_USB_TLL_HS_WKDEP[0] WKUPDEP_USB_TLL_HS_MPU	Read/write
SATA	CD_L3INIT	CD_MPU, CD_L3_MAIN1, CD_L4_CFG	Disabled	PM_L3INIT_SATA_WKDEP[0] WKUPDEP_SATA_MPU	Read/write

3.6.10.4 Clock Domain Module Attributes

Table 3-134 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-134. CD_L3INIT Modules Clocks Association

Module	Clock	Clock Type
HSI	HSI_GFCLK	Interface and functional
	L3INIT_L3_GICLK	Interface
	L3INIT_L4_GICLK	Interface
IEEE1500_2_OCP	L3INIT_L3_GICLK	Interface and functional
	L3INIT_L4_GICLK	Interface
MMC1	MMC1_GFCLK	Functional
	MMC1_32K_GFCLK	Functional
	L3INIT_L3_GICLK	Interface

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Table 3-134. CD_L3INIT Modules Clocks Association (continued)

Module	Clock	Clock Type
	L3INIT_L4_GICLK	Interface
MMC2	MMC2_GFCLK	Functional
	L3INIT_L3_GICLK	Interface
	L3INIT_L4_GICLK	Interface
USB_OTG_SS	L3INIT_960M_GFCLK	Functional
	L3INIT_L3_GICLK	Interface
	L3INIT_L4_GICLK	Interface
	USB_OTG_SS_REF_CLK	Reference clock for the DPLL_USB_OTG_SS (not managed by the PRCM module)
	CORE_USB_OTG_SS_LFPS_TX_CLK	Interface
USB_HOST_HS	HSIC_P1_480M_GFCLK	Functional
	HSIC_P1_GFCLK	Functional
	HSIC_P2_480M_GFCLK	Functional
	HSIC_P2_GFCLK	Functional
	HSIC_P3_480M_GFCLK	Functional
	HSIC_P3_GFCLK	Functional
	L3INIT_48M_GFCLK	Functional (mandatory)
	L3INIT_48M_GFCLK	Functional (optional)
	L3INIT_L3_GICLK	Interface
	L3INIT_L4_GICLK	Interface
	UTMI_P1_GFCLK	Functional
	UTMI_P2_GFCLK	Functional
	UTMI_P3_GFCLK	Functional
	UTMI_ROOT_GFCLK	Functional
USB_TLL_HS	L3INIT_L4_GICLK	Interface
	TLL_CH0_GFCLK	Functional
	TLL_CH1_GFCLK	Functional
	TLL_CH2_GFCLK	Functional
OCP2SCP1	L3INIT_L4_GICLK	Interface
OCP2SCP3	L3INIT_L4_GICLK	Interface
SATA	L3INIT_L3_GICLK	Interface
	L3INIT_48M_GFCLK	Functional
	SATA_REF_GFCLK	Functional

Table 3-135 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-135. CD_L3INIT Modules Wake-Up Request

Module	Wake-Up Feature
HSI	Slave wake-up request (MPU-IRQ, IPU-IRQ, DSP-IRQ)/Master wake-up request
MMC1	Slave wake-up request (MPU-IRQ, IPU-IRQ, DSP-IRQ, DMA_SYSTEM-DMA)
MMC2	Slave wake-up request (MPU-IRQ, IPU-IRQ, DSP-IRQ, DMA_SYSTEM-DMA)
DPLL_USB, OCP2SCP1, OCP2SCP3	None
IEEE1500_2_OCP	Master wake-up request
USB_OTG_SS	Slave wake-up request (MPU-IRQ, IPU-IRQ)

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Table 3-135. CD_L3INIT Modules Wake-Up Request (continued)

Module	Wake-Up Feature
USB_HOST_HS	Slave wake-up request (MPU-IRQ, IPU-IRQ)
USB_TLL_HS	Slave wake-up request (MPU-IRQ, IPU-IRQ)
SATA	Slave wake-up request (MPU-IRQ)/Master wake-up request

Table 3-136 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-136. CD_L3INIT Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
HSI	Slave/master	CM_L3INIT_HSI_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_HSI_CLKCTRL[17:16] IDLEST	Idle status
IEEE1500_2_OCP	Slave/master	CM_L3INIT_IEEE1500_2_OCP_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_IEEE1500_2_OCP_CLKCTRL[17:16] IDLEST	Idle status
MMC1	Master/slave	CM_L3INIT_MMC1_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_MMC1_CLKCTRL[17:16] IDLEST	Idle status
MMC2	Master/slave	CM_L3INIT_MMC2_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_MMC2_CLKCTRL[17:16] IDLEST	Idle status
USB_OTG_SS	Slave/master	CM_L3INIT_USB_OTG_SS_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_USB_OTG_SS_CLKCTRL[17:16] IDLEST	Idle status
USB_HOST_HS	Slave/master	CM_L3INIT_USB_HOST_HS_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_USB_HOST_HS_CLKCTRL[17:16] IDLEST	Idle status
USB_TLL_HS	Slave	CM_L3INIT_USB_TLL_HS_CLKCTRL[17:16] IDLEST	Idle status
SATA	Slave/master	CM_L3INIT_SATA_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_SATA_CLKCTRL[17:16] IDLEST	Idle status
OCP2SCP1	Slave	CM_L3INIT_OCP2SCP1_CLKCTRL[17:16] IDLEST	Standby status
OCP2SCP3	Slave	CM_L3INIT_OCP2SCP3_CLKCTRL[17:16] IDLEST	Standby status

Table 3-137 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-137. CD_L3INIT Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
HSI	Available	Available	N/A	CM_L3INIT_HSI_CLKCTRL[1:0] MODULEMODE	Read/write

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Table 3-137. CD_L3INIT Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
IEEE1500_2_OCP	N/A	Available	N/A	CM_L3INIT_IEEE1500_2_OCP_CLKCTRL[1:0] MODULEMODE	Read
MMC1	Available	N/A	Available	CM_L3INIT_MMC1_CLKCTRL[1:0] MODULEMODE	Read/write
MMC2	Available	N/A	Available	CM_L3INIT_MMC2_CLKCTRL[1:0] MODULEMODE	Read/write
USB_OTG_SS	Available	Available	N/A	CM_L3INIT_USB_OTG_SS_CLKCTRL[1:0] MODULEMODE	Read/write
USB_HOST_HS	Available	N/A	Available	CM_L3INIT_USB_HOST_HS_CLKCTRL[1:0] MODULEMODE	Read/write
USB_TLL_HS	Available	Available	N/A	CM_L3INIT_USB_TLL_HS_CLKCTRL[1:0] MODULEMODE	Read/write
SATA	Available	N/A	Available	CM_L3INIT_SATA_CLKCTRL[1:0] MODULEMODE	Read/write
OCP2SCP1	N/A	Available	N/A	CM_L3INIT_OCP2SCP1_CLKCTRL[1:0] MODULEMODE	Read/write
OCP2SCP3	Available	Available	N/A	CM_L3INIT_OCP2SCP3_CLKCTRL[1:0] MODULEMODE	Read/write

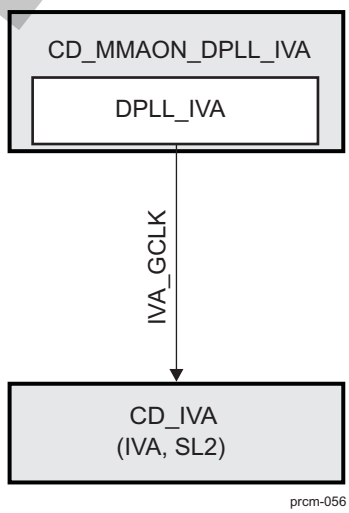
3.6.11 CD_IVA Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.11.1 Overview

Figure 3-63 is an overview of the clock domain.

Figure 3-63. CD_IVA Overview



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3.6.11.2 Clock Domain Modes

Table 3-138 lists the clock domain modes supported by the clock domain.

Table 3-138. CD_IVA Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-139 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-139. CD_IVA Control and Status Parameters

Parameter Name	Control/Status Bit Field
IVA_GCLK Clock Status	CM_IVA_CLKSTCTRL[8] CLKACTIVITY_IVA_GCLK
Clock Domain State Transition Control	CM_IVA_CLKSTCTRL[1:0] CLKTRCTRL

3.6.11.3 Clock Domain Dependency

CD_IVA has no module wake-up dependency with any other clock domain of the device.

3.6.11.3.1 Static Dependency

Table 3-140 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-140. CD_IVA Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN1	Disabled	CM_IVA_STATICDEP[5] L3MAIN1_STATDEP	Read/write
CD_L3_MAIN2	Always enabled	CM_IVA_STATICDEP[6] L3MAIN2_STATDEP	Read only
CD_EMIF	Disabled	CM_IVA_STATICDEP[4] EMIF_STATDEP	Read/write

3.6.11.3.2 Dynamic Dependency

Table 3-141 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-141. CD_IVA Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN2	Alway disabled	CM_IVA_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only

3.6.11.4 Clock Domain Module Attributes

Table 3-142 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-142. CD_IVA Modules Clocks Association

Module	Clock	Clock Type
IVA	IVA_GCLK	Interface and functional
SL2	IVA_GCLK	Interface

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Table 3-143 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-143. CD_IVA Modules Wake-Up Request

Module	Wake-Up Feature
IVA	None
SL2	None

Table 3-144 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-144. CD_IVA Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
IVA	Master/Slave	CM_IVA_IVA_CLKCTRL[18] STBYST	Standby status
		CM_IVA_IVA_CLKCTRL[17:16] IDLEST	Idle status
SL2	Slave	CM_IVA_SL2_CLKCTRL[17:16] IDLEST	Idle status

Table 3-145 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-145. CD_IVA Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
IVA	Available	Available	N/A	CM_IVA_IVA_CLKCTRL[1:0] MODULEMODE	Read/write
SL2	Available	Available	N/A	CM_IVA_SL2_CLKCTRL[1:0] MODULEMODE	Read/write

3.6.12 CD_GPU Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.12.1 Overview

Figure 3-64 is an overview of the clock domain.

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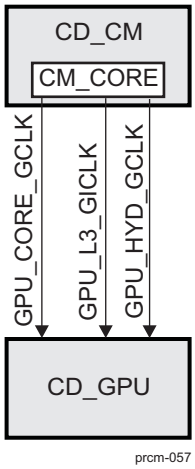
Figure 3-64. CD_GPU Overview



3.6.12.2 Clock Domain Modes

Table 3-146 lists the clock domain modes supported by the clock domain.

Table 3-146. CD_GPU Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-147 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-147. CD_GPU Control and Status Parameters

Parameter Name	Control/Status Bit Field
GPU_L3_GICLK clock status	CM_GPU_CLKSTCTRL[8] CLKACTIVITY_GPU_L3_GICLK
Select the ratio of GPU_L3_GICLK (SYS_CLK) to L3_ICLK	CM_GPU_GPU_CLKCTRL[26] CLKSEL_GPU_SYS_CLK
GPU_CORE_GCLK clock status	CM_GPU_CLKSTCTRL[9] CLKACTIVITY_GPU_CORE_GCLK
Select the source of GPU_CORE_GCLK	CM_GPU_GPU_CLKCTRL[24] CLKSEL_GPU_CORE_GCLK
GPU_HYD_GCLK clock status	CM_GPU_CLKSTCTRL[10] CLKACTIVITY_GPU_HYD_GCLK
Select the source of GPU_HYD_GCLK	CM_GPU_GPU_CLKCTRL[25] CLKSEL_GPU_HYD_GCLK
Clock Domain State Transition Control	CM_GPU_CLKSTCTRL[1:0] CLKTRCTRL

3.6.12.3 Clock Domain Dependency

CD_GPU has no module wake-up dependency with any other clock domain of the device.

3.6.12.3.1 Static Dependency

Table 3-148 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-148. CD_GPU Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_IVA	Disabled	CM_GPU_STATICDEP[2] IVA_STATDEP	Read/write
CD_L3_MAIN1	Disabled	CM_GPU_STATICDEP[5] L3MAIN1_STATDEP	Read/write

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Table 3-148. CD_GPU Static Dependency Association Parameters (continued)

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN2	Always enabled	CM_GPU_STATICDEP[6] L3MAIN2_STATDEP	Read only
CD_EMIF	Disabled	CM_GPU_STATICDEP[4] EMIF_STATDEP	Read/write

3.6.12.3.2 Dynamic Dependency

Table 3-149 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-149. CD_GPU Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN2	Alway disabled	CM_GPU_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only

3.6.12.4 Clock Domain Module Attributes

Table 3-150 identifies for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-150. CD_GPU Modules Clocks Association

Module	Clock	Clock Type
GPU	GPU_L3_GICLK	Interface
	GPU_CORE_GCLK	Functional
	GPU_HYD_GCLK	Functional

Table 3-151 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-151. CD_GPU Modules Wake-Up Request

Module	Wake-Up Feature
GPU	None

Table 3-152 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-152. CD_GPU Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
GPU	Master/slave	CM_GPU_GPU_CLKCTRL[18] STBYST	Standby status
		CM_GPU_GPU_CLKCTRL[17:16] IDLEST	Idle status

Table 3-153 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-153. CD_GPU Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
GPU	Available	N/A	Available	CM_GPU_GPU_CLKCTRL[1:0] MODULEMODE	Read/write

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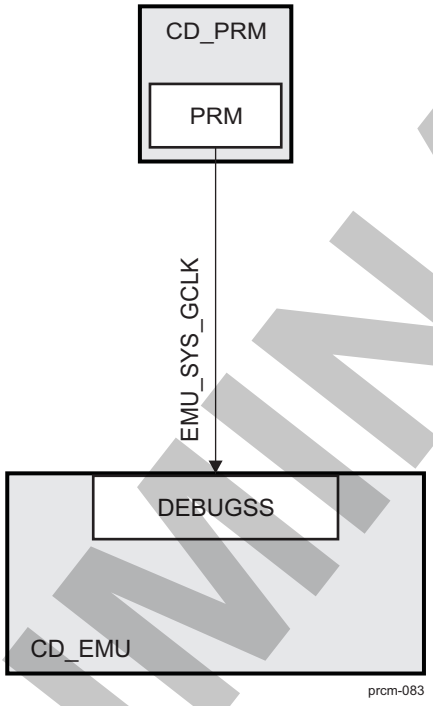
3.6.13 CD_EMU Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.13.1 Overview

Figure 3-65 is an overview of the clock domain.

Figure 3-65. CD_EMU Overview



3.6.13.2 Clock Domain Modes

Table 3-154 lists the clock domain modes supported by the clock domain.

Table 3-154. CD_EMU Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Not available	Not available	Available	Available

Table 3-155 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-155. CD_EMU Control and Status Parameters

Parameter Name	Control/Status Bit Field
EMU_SYS_GCLK Clock Status	CM_EMU_CLKSTCTRL[8] CLKACTIVITY_EMU_SYS_GCLK
Clock Domain State Transition Control	CM_EMU_CLKSTCTRL[1:0] CLKTRCTRL

3.6.13.3 Clock Domain Dependency

CD_EMU has no static or module wake-up dependency with any other clock domain of the device.

3.6.13.3.1 Dynamic Dependency

Table 3-156 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

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Table 3-156. CD_EMU Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN2	Always enabled	CM_EMU_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only

3.6.13.4 Clock Domain Module Attributes

Table 3-157 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-157. CD_EMU Modules Clocks Association

Module	Clock	Clock Type
DEBUGSS	EMU_SYS_GCLK	Interface and functional

Table 3-158 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-158. CD_EMU Modules Wake-Up Request

Module	Wake-Up Feature
DEBUGSS	Master wake-up request

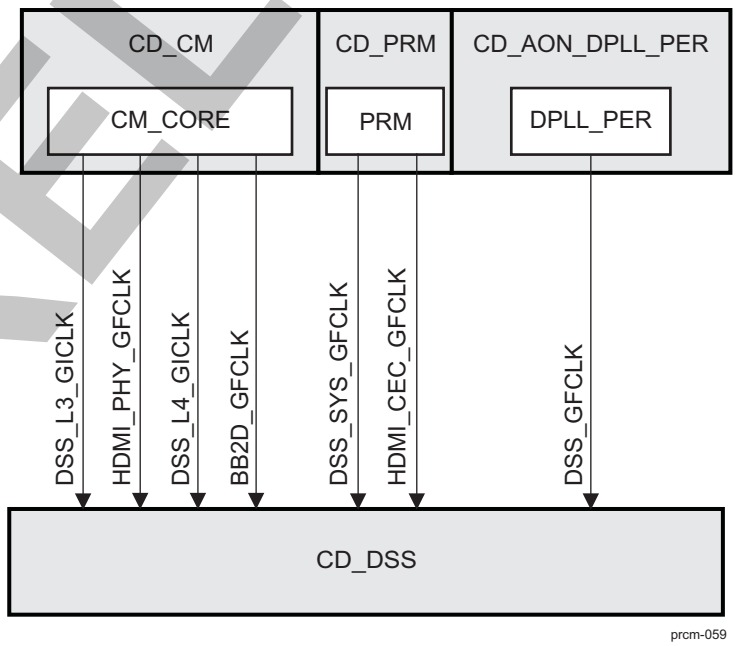
3.6.14 CD_DSS Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device. BB2D is a part of CD_DSS clock domain. BB2D_GFCLK is the functional clock for BB2D module. It is derived from H24 post divider of DPLL_CORE.

3.6.14.1 Overview

Figure 3-66 is an overview of the clock domain.

Figure 3-66. CD_DSS Overview



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3.6.14.2 Clock Domain Modes

Table 3-159 lists the clock domain modes supported by the clock domain.

Table 3-159. CD_DSS Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-160 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-160. CD_DSS Control and Status Parameters

Parameter Name	Control/Status Bit Field
DSS_SYS_GFCLK Clock Status	CM_DSS_CLKSTCTRL[10] CLKACTIVITY_DSS_SYS_GFCLK
DSS_SYS_GFCLK Clock Control	CM_DSS_DSS_CLKCTRL[10] OPTFCLKEN_SYS_CLK
DSS_GFCLK Clock Status	CM_DSS_CLKSTCTRL[9] CLKACTIVITY_DSS_GFCLK
DSS_GFCLK Clock Control	CM_DSS_DSS_CLKCTRL[8] OPTFCLKEN_DSSCLK
HDMI_PHY_GFCLK Clock Status	CM_DSS_CLKSTCTRL[11] CLKACTIVITY_HDMI_PHY_GFCLK
HDMI_PHY_GFCLK Clock Control	CM_DSS_DSS_CLKCTRL[9] OPTFCLKEN_48MHZ_CLK
HDMI_CEC_GFCLK Clock Status	CM_DSS_CLKSTCTRL[12] CLKACTIVITY_HDMI_CEC_GFCLK
HDMI_CEC_GFCLK Clock Control	CM_DSS_DSS_CLKCTRL[11] OPTFCLKEN_32KHZ_CLK
BB2D_GFCLK Clock Control	CM_DSS_CLKSTCTRL[13] CLKACTIVITY_BB2D_GFCLK
DSS_L3_GICLK and DSS_L4_GICLK Clock Status	CM_DSS_CLKSTCTRL[8] CLKACTIVITY_DSS_L3_GICLK
Clock Domain State Transition Control	CM_DSS_CLKSTCTRL[1:0] CLKTRCTRL

3.6.14.3 Clock Domain Dependency

3.6.14.3.1 Static Dependency

Table 3-161 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-161. CD_DSS Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_IVA	Disabled	CM_DSS_STATICDEP[2] IVA_STATDEP	Read/write
CD_L3_MAIN1	Always enabled	CM_DSS_STATICDEP[5] L3MAIN1_STATDEP	Read only
CD_L3_MAIN2	Enabled	CM_DSS_STATICDEP[6] L3MAIN2_STATDEP	Read/write
CD_EMIF	Disabled	CM_DSS_STATICDEP[4] EMIF_STATDEP	Read/write

3.6.14.3.2 Dynamic Dependency

Table 3-162 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-162. CD_DSS Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN1	Alway disabled	CM_DSS_DYNAMICDEP[5] L3MAIN1_DYNDEP	Read only
CD_L3_MAIN2	Alway disabled	CM_DSS_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only

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3.6.14.3.3 Wake-Up Dependency

Table 3-163 lists the wake-up dependency settings for the modules of this clock in the clock domain

Table 3-163. CD_DSS Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
DSS-DSI1_A	CD_DSS	CD_DMA, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[7] WKUPDEP_DSI1_A_SDMA	Read/write
DSS-DSI1_A	CD_DSS	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[6] WKUPDEP_DSI1_A_DSP	Read/write
DSS-DSI1_A	CD_DSS	CD_IPU, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[5] WKUPDEP_DSI1_A_IPU	Read/write
DSS-DSI1_A	CD_DSS	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[4] WKUPDEP_DSI1_A_MPU	Read/write
DSS-DSI1_C	CD_DSS	CD_IPU, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[16] WKUPDEP_DSI1_C_IPU	Read/write
DSS-DSI1_C	CD_DSS	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[15] WKUPDEP_DSI1_C_MPU	Read/write
DSS-DSI1_C	CD_DSS	CD_DMA, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[18] WKUPDEP_DSI1_C_SDMA	Read/write
DSS-DSI1_C	CD_DSS	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[17] WKUPDEP_DSI1_C_DSP	Read/write
DSS-HDMI	CD_DSS	CD_DMA, CD_L3_MAIN2	Enabled	PM_DSS_DSS_WKDEP[19] WKUPDEP_HDMIDMA_SDMA	Read/write
DSS-HDMI	CD_DSS	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[14] WKUPDEP_HDMIIRQ_DSP	Read/write
DSS-HDMI	CD_DSS	CD_IPU, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[13] WKUPDEP_HDMIIRQ_IPU	Read/write
DSS-HDMI	CD_DSS	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[12] WKUPDEP_HDMIIRQ_MPU	Read/write
DSS-DISPC	CD_DSS	CD_IPU, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[1] WKUPDEP_DISPC_IPU	Read/write
DSS-DISPC	CD_DSS	CD_MPU, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[0] WKUPDEP_DISPC_MPU	Read/write

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Table 3-163. CD_DSS Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
DSS-DISPC	CD_DSS	CD_DSP, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[2] WKUPDEP_DISPC_DSP	Read/write
DSS-DISPC	CD_DSS	CD_DMA, CD_L3_MAIN2	Disabled	PM_DSS_DSS_WKDEP[3] WKUPDEP_DISPC_SDMA	Read/write

3.6.14.4 Clock Domain Module Attributes

Table 3-164 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-164. CD_DSS Modules Clocks Association

Module	Clock	Clock Type
DSS	DSS_SYS_GFCLK	Functional
	DSS_GFCLK	Functional
	HDMI_PHY_GFCLK	Functional
	HDMI_CEC_GFCLK	Functional
	DSS_L3_GICLK	Interface
	DSS_L4_GICLK	Interface
BB2D	BB2D_GFCLK	Functional
	DSS_L3_GICLK	Interface

Table 3-165 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-165. CD_DSS Modules Wake-Up Request

Module	Wake-Up Feature
DSS	Slave wake-up request (MPU-IRQ, IPU-IRQ, DSP-IRQ, DMA_SYSTEM-DMA)
BB2D	None

Table 3-166 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-166. CD_DSS Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
DSS	Master/slave	CM_DSS_DSS_CLKCTRL[18] STBYST	Standby status
		CM_DSS_DSS_CLKCTRL[17:16] IDLEST	Idle status
BB2D	Master/slave	CM_DSS_BB2D_CLKCTRL[18] STBYST	Standby status
		CM_DSS_BB2D_CLKCTRL[17:16] IDLEST	Idle status

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Table 3-167 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-167. CD_DSS Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
DSS	Available	N/A	Available	CM_DSS_DSS_CLKCTRL[1:0] MODULEMODE	Read/write
BB2D	Available	N/A	Available	CM_DSS_BB2D_CLKCTRL[1:0] MODULEMODE	Read/write

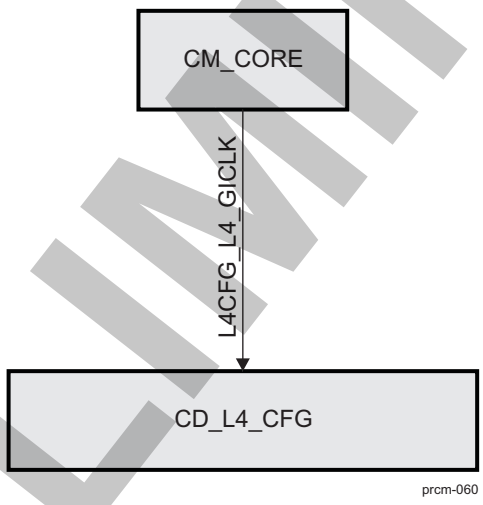
3.6.15 CD_L4_CFG Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.15.1 Overview

Figure 3-67 is an overview of the clock domain.

Figure 3-67. CD_L4_CFG Overview



3.6.15.2 Clock Domain Modes

Table 3-168 lists the clock domain modes supported by the clock domain.

Table 3-168. CD_L4_CFG Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Not available	Available

Table 3-169 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-169. CD_L4_CFG Control and Status Parameters

Parameter Name	Control/Status Bit Field
L4CFG_L4_GICLK Clock Status	CM_L4CFG_CLKSTCTRL[8] CLKACTIVITY_L4CFG_L4_GICLK
Clock Domain State Transition Control	CM_L4CFG_CLKSTCTRL[1:0] CLKTRCTRL

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3.6.15.3 Clock Domain Dependency

CD_L4_CFG has no static or module wake-up dependency with any other clock domain of the device.

3.6.15.3.1 Dynamic Dependency

Table 3-170 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-170. CD_L4_CFG Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_CUSTEFUSE	Always enabled	CM_L4CFG_DYNAMICDEP[17] CUSTEFUSE_DYNDEP	Read only
CD_CAM	Alway disabled	CM_L4CFG_DYNAMICDEP[9] CAM_DYNDEP	Read only
CD_L3_MAIN1	Always enabled	CM_L4CFG_DYNAMICDEP[5] L3MAIN1_DYNDEP	Read only
CD_L3_MAIN2	Always enabled	CM_L4CFG_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only
CD_L3INIT	Always enabled	CM_L4CFG_DYNAMICDEP[7] L3INIT_DYNDEP	Read only
CD_EMIF	Always enabled	CM_L4CFG_DYNAMICDEP[4] EMIF_DYNDEP	Read only
CD_DMA	Always enabled	CM_L4CFG_DYNAMICDEP[11] SDMA_DYNDEP	Read only
CD_DSP	Always enabled	CM_L4CFG_DYNAMICDEP[1] DSP_DYNDEP	Read only
CD_MPU	Always enabled	CM_L4CFG_DYNAMICDEP[19] MPU_DYNDEP	Read only
CD_COREAON	Always enabled	CM_L4CFG_DYNAMICDEP[16] COREAON_DYNDEP	Read only

3.6.15.4 Clock Domain Module Attributes

Table 3-171 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-171. CD_L4_CFG Modules Clocks Association

Module	Clock	Clock Type
CTRL_MODULE_CORE	L4CFG_L4_GICLK	Functional
SPINLOCK	L4CFG_L4_GICLK	Interface
L4_CFG interconnect	L4CFG_L4_GICLK	Interface
MAILBOX	L4CFG_L4_GICLK	Interface
SAR_ROM	L4CFG_L4_GICLK	Interface

Table 3-172 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-172. CD_L4_CFG Modules Wake-Up Request

Module	Wake-Up Feature
CONTROL_MODULE_CORE	None
SPINLOCK	None
L4_CFG interconnect	None
MAILBOX	None
SAR_ROM	None

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Table 3-173 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-173. CD_L4_CFG Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
SPINLOCK	Slave	CM_L4CFG_SPINLOCK_CLKCTRL[17:16] IDLEST	Idle status
L4_CFG interconnect	Slave	CM_L4CFG_L4_CFG_CLKCTRL[17:16] IDLEST	Idle status
MAILBOX	Slave	CM_L4CFG_MAILBOX_CLKCTRL[17:16] IDLEST	Idle status
SAR_ROM	Slave	CM_L4CFG_SAR_ROM_CLKCTRL[17:16] IDLEST	Idle status

Table 3-174 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-174. CD_L4_CFG Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
SPINLOCK	N/A	Available	N/A	CM_L4CFG_SPINLOCK_CLKCTRL[1:0] MODULEMODE	Read only
L4_CFG interconnect	N/A	Available	N/A	CM_L4CFG_L4_CFG_CLKCTRL[1:0] MODULEMODE	Read only
MAILBOX	N/A	Available	N/A	CM_L4CFG_MAILBOX_CLKCTRL[1:0] MODULEMODE	Read only
SAR_ROM	N/A	Available	N/A	CM_L4CFG_SAR_ROM_CLKCTRL[1:0] MODULEMODE	Read only

3.6.16 CD_L3_INSTR Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.16.1 Overview

Figure 3-68 is an overview of the clock domain.

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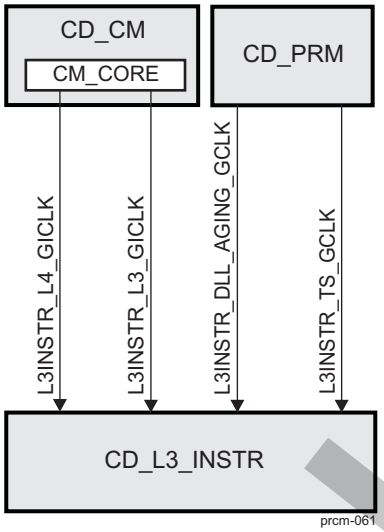
Figure 3-68. CD_L3_INSTR Overview



3.6.16.2 Clock Domain Modes

Table 3-175 lists the clock domain modes supported by the clock domain.

Table 3-175. CD_L3_INSTR Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Not available	Not available	Not available	Available

Table 3-176 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-176. CD_L3_INSTR Control and Status Parameters

Parameter Name	Control/Status Bit Field
L3INSTR_L3_GICLK Clock Status	CM_L3INSTR_CLKSTCTRL[8] CLKACTIVITY_L3INSTR_L3_GICLK
L3INSTR_DLL_AGING_GCLK Clock Status	CM_L3INSTR_CLKSTCTRL[9] CLKACTIVITY_L3INSTR_DLL_AGING_GCLK
L3INSTR_TS_GCLK Clock Status	CM_L3INSTR_CLKSTCTRL[10] CLKACTIVITY_L3INSTR_TS_GCLK
Clock Domain State Transition Control	CM_L3INSTR_CLKSTCTRL[1:0] CLKTRCTRL

3.6.16.3 Clock Domain Dependency

CD_L3_INSTR has no static, dynamic, or module wake-up dependency with any other clock domain of the device.

For aging, DLL requires a low-frequency clock that must run as long as the CORE power domain is on. To match this requirement, the DLL_AGING module has been created and instantiated in this clock domain, which is the last to transition in low-power state.

3.6.16.4 Clock Domain Module Attributes

Table 3-177 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

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Table 3-177. CD_L3_INSTR Modules Clocks Association

Module	Clock	Clock Type
L3_MAIN_3 interconnect	L3INSTR_L3_GICLK	Interface
	L3INSTR_L4_GICLK	Interface
L3_INSTR interconnect	L3INSTR_L3_GICLK	Interface
OCP_WP_NOC	L3INSTR_L3_GICLK	Interface
	L3INSTR_L4_GICLK	Interface
DLL_AGING	L3INSTR_DLL_AGING_GCLK	Interface
CTRL_MODULE_BANDGAP	L3INSTR_TS_GCLK	Interface

Table 3-178 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-178. CD_L3_INSTR Modules Wake-Up Request

Module	Wake-Up Feature
L3_MAIN_3 interconnect	None
L3_INSTR interconnect	None
OCP_WP_NOC	None
DLL_AGING	None
CTRL_MODULE_BANDGAP	None

Table 3-179 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-179. CD_L3_INSTR Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
L3_MAIN_3 interconnect	Slave	CM_L3INSTR_L3_MAIN_3_CLKCTRL[17:16] IDLEST	Idle status
L3_INSTR interconnect	Slave	CM_L3INSTR_L3_INSTR_CLKCTRL[17:16] IDLEST	Idle status
OCP_WP_NOC	Slave	CM_L3INSTR_OCP_WP_NOC_CLKCTRL[17:16] IDLEST	Idle status
DLL_AGING	Slave	CM_L3INSTR_DLL_AGING_CLKCTRL[17:16] IDLEST	Idle status
CTRL_MODULE_BANDGAP	Slave	CM_L3INSTR_CTRL_MODULE_BANDGAP_CLKCTRL[17:16] IDLEST	Idle status

Table 3-180 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-180. CD_L3_INSTR Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
L3_MAIN_3 interconnect	Available	Available	N/A	CM_L3INSTR_L3_MAIN_3_CLKCTRL[1:0] MODULEMODE	Read/write
L3_INSTR interconnect	Available	Available	N/A	CM_L3INSTR_L3_INSTR_CLKCTRL[1:0] MODULEMODE	Read/write
OCP_WP_NOC	Available	Available	N/A	CM_L3INSTR_OCP_WP_NOC_CLKCTRL[1:0] MODULEMODE	Read/write
DLL_AGING	N/A	Available	N/A	CM_L3INSTR_DLL_AGING_CLKCTRL[1:0] MODULEMODE	Read only

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Table 3-180. CD_L3_INSTR Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
CTRL_MODULE_BANDGAP	N/A	Available	N/A	CM_L3INSTR_CTRL_MODULE_BANDGAP_CLKCTRL[1:0] MODULEMODE	Read only

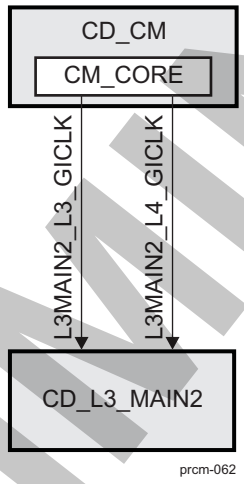
3.6.17 CD_L3_MAIN2 Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.17.1 Overview

Figure 3-69 is an overview of the clock domain.

Figure 3-69. CD_L3_MAIN2 Overview



3.6.17.2 Clock Domain Modes

Table 3-181 lists the clock domain modes supported by the clock domain.

Table 3-181. CD_L3_MAIN2 Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Not available	Available

Table 3-182 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-182. CD_L3_MAIN2 Control and Status Parameters

Parameter Name	Control/Status Bit Field
L3MAIN2_L3_GICLK Clock Status	CM_L3MAIN2_CLKSTCTRL[8] CLKACTIVITY_L3MAIN2_L3_GICLK
Clock Domain State Transition Control	CM_L3MAIN2_CLKSTCTRL[1:0] CLKTRCTRL

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3.6.17.3 Clock Domain Dependency

CD_L3_MAIN2 has no static or module wake-up dependency with any other clock domain of the device.

3.6.17.3.1 Dynamic Dependency

Table 3-183 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-183. CD_L3_MAIN2 Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_DSS	Always enabled	CM_L3MAIN2_DYNAMICDEP[8] DSS_DYNDEP	Read only
CD_IPU	Always enabled	CM_L3MAIN2_DYNAMICDEP[0] IPU_DYNDEP	Read only
CD_GPU	Always enabled	CM_L3MAIN2_DYNAMICDEP[10] GPU_DYNDEP	Read only
CD_CAM	Alway disabled	CM_L3MAIN2_DYNAMICDEP[9] CAM_DYNDEP	Read only
CD_IVA	Always enabled	CM_L3MAIN2_DYNAMICDEP[2] IVAHD_DYNDEP	Read only
CD_L3_MAIN1	Always enabled	CM_L3MAIN2_DYNAMICDEP[5] L3_MAIN1_DYNDEP	Read only
CD_L4_PER	Always enabled	CM_L3MAIN2_DYNAMICDEP[13] L4PER_DYNDEP	Read only
CD_L4_SEC	Always enabled	CM_L3MAIN2_DYNAMICDEP[14] L4SEC_DYNDEP	Read only

3.6.17.4 Clock Domain Module Attributes

Table 3-184 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-184. CD_L3_MAIN2 Modules Clocks Association

Module	Clock	Clock Type
GPMC	L3MAIN2_L3_GICLK	Interface
L3_MAIN2 interconnect	L3MAIN2_L3_GICLK	Interface
	L3MAIN2_L4_GICLK	Interface
OCMC_RAM	L3MAIN2_L3_GICLK	Interface

Table 3-185 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-185. CD_L3_MAIN2 Modules Wake-Up Request

Module	Wake-Up Feature
GPMC	None
L3_MAIN2 interconnect	None
OCMC_RAM	None

Table 3-186 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

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Table 3-186. CD_L3_MAIN2 Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
GPMC	Slave	CM_L3MAIN2_GPMC_CLKCTRL[17:16] IDLEST	Idle status
L3_MAIN2 interconnect	Slave	CM_L3MAIN2_L3_MAIN_2_CLKCTRL[17:16] IDLEST	Idle status
OCMC_RAM	Slave	CM_L3MAIN2_OCMC_RAM_CLKCTRL[17:16] IDLEST	Idle status

Table 3-187 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-187. CD_L3_MAIN2 Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
GPMC	Available	Available	N/A	CM_L3MAIN2_GPMC_CLKCTRL[1:0] MODULEMODE	Read/write
L3_MAIN2 interconnect	N/A	Available	N/A	CM_L3MAIN2_L3_MAIN_2_CLKCTRL[1:0] MODULEMODE	Read only
OCMC_RAM	N/A	Available	N/A	CM_L3MAIN2_OCMC_RAM_CLKCTRL[1:0] MODULEMODE	Read only

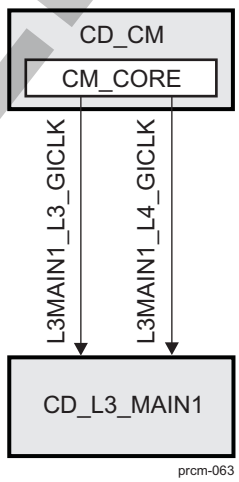
3.6.18 CD_L3_MAIN1 Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.18.1 Overview

Figure 3-70 is an overview of the clock domain.

Figure 3-70. CD_L3_MAIN1 Overview



3.6.18.2 Clock Domain Modes

Table 3-188 lists the clock domain modes supported by the clock domain.

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Table 3-188. CD_L3_MAIN1 Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Not available	Available

Table 3-189 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-189. CD_L3_MAIN1 Control and Status Parameters

Parameter Name	Control/Status Bit Field
L3MAIN1_L3_GICLK Clock Status	CM_L3MAIN1_CLKSTCTRL[8] CLKACTIVITY_L3MAIN1_L3_GICLK
Clock Domain State Transition Control	CM_L3MAIN1_CLKSTCTRL[1:0] CLKTRCTRL

3.6.18.3 Clock Domain Dependency

CD_L3_MAIN1 has no static or module wake-up dependency with any other clock domain of the device.

3.6.18.3.1 Dynamic Dependency

Table 3-190 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-190. CD_L3_MAIN1 Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Always enabled	CM_L3MAIN1_DYNAMICDEP[3] ABE_DYNDEP	Read only
CD_L3_MAIN2	Always enabled	CM_L3MAIN1_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only
CD_L4_CFG	Always enabled	CM_L3MAIN1_DYNAMICDEP[12] L4CFG_DYNDEP	Read only
CD_EMIF	Always enabled	CM_L3MAIN1_DYNAMICDEP[4] EMIF_DYNDEP	Read only
CD_WKUPAON	Always enabled	CM_L3MAIN1_DYNAMICDEP[15] WKUPAON_DYNDEP	Read only

3.6.18.4 Clock Domain Module Attributes

Table 3-191 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-191. CD_L3_MAIN1 Modules Clocks Association

Module	Clock	Clock Type
L3_MAIN1 interconnect	L3MAIN1_L3_GICLK	Interface
	L3MAIN1_L4_GICLK	Interface

Table 3-192 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-192. CD_L3_MAIN1 Modules Wake-Up Request

Module	Wake-Up Feature
L3_MAIN1 interconnect	None

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Table 3-193 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-193. CD_L3_MAIN1 Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
L3_MAIN1 interconnect	Slave	CM_L3MAIN1_L3_MAIN_1_CLKCTRL[17:16] IDLEST	Idle status

Table 3-194 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-194. CD_L3_MAIN1 Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
L3_MAIN1 interconnect	N/A	Available	N/A	CM_L3MAIN1_L3_MAIN_1_CLKCTRL[1:0] MODULEMODE	Read only

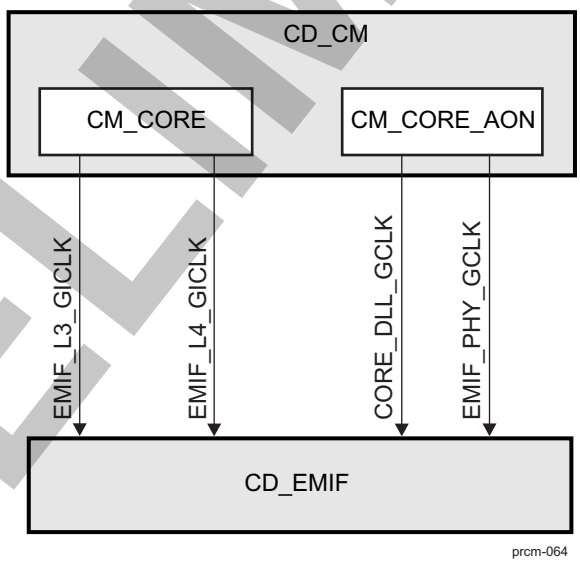
3.6.19 CD_EMIF Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.19.1 Overview

Figure 3-71 is an overview of the clock domain.

Figure 3-71. CD_EMIF Overview



3.6.19.2 Clock Domain Modes

Table 3-195 lists the clock domain modes supported by the clock domain.

Table 3-195. CD_EMIF Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Available	Available

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Table 3-196 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-196. CD_EMIF Control and Status Parameters

Parameter Name	Control/Status Bit Field
CORE_DLL_GCLK Clock Status	CM_EMIF_CLKSTCTRL[9] CLKACTIVITY_DLL_GCLK
CORE_DLL_GCLK Clock Control	CM_EMIF_EMIF_DLL_CLKCTRL[8] OPTFCLKEN_DLL_CLK
EMIF_L3_GICLK Clock Status	CM_EMIF_CLKSTCTRL[8] CLKACTIVITY_EMIF_L3_GICLK
EMIF_PHY_GCLK Clock Status	CM_EMIF_CLKSTCTRL[10] CLKACTIVITY_EMIF_PHY_GCLK
Clock Domain State Transition Control	CM_EMIF_CLKSTCTRL[1:0] CLKTRCTRL

3.6.19.3 Clock Domain Dependency

CD_EMIF has no static, dynamic, or module wake-up dependency with any other clock domain of the device.

3.6.19.4 Clock Domain Module Attributes

Table 3-197 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-197. CD_EMIF Modules Clocks Association

Module	Clock	Clock Type
DLL	CORE_DLL_GCLK	Functional
DMM	EMIF_L3_GICLK	Interface
DDRPHY	EMIF_PHY_GCLK	Interface
EMIF1	CORE_DLL_GCLK	Interface
	EMIF_L3_GICLK	Interface
	MA_EOCP_GICLK(1)	Interface
	L3_EOCP_GICLK(1)	Interface
	EMIF_PHY_GCLK	Interface
EMIF2	CORE_DLL_GCLK	Interface
	EMIF_L3_GICLK	Interface
	MA_EOCP_GICLK(1)	Interface
	L3_EOCP_GICLK(1)	Interface
	EMIF_PHY_GCLK	Interface
EMIF_OCP_FW	EMIF_L3_GICLK	Interface
	EMIF_L4_GICLK	Interface

(1) EMIF modules are clocked by MA_EOCP_GICLK when MPU is active; otherwise, the L3_EOCP_GICLK clock is used.

Table 3-198 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-198. CD_EMIF Modules Wake-Up Request

Module	Wake-Up Feature
DDRPHY	None
DLL	None
DMM	None
EMIF1	None
EMIF2	None
EMIF_OCP_FW	None

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Table 3-199 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-199. CD_EMIF Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
DMM	Slave	CM_EMIF_DMM_CLKCTRL[17:16] IDLEST	Idle status
EMIF1	Slave	CM_EMIF_EMIF1_CLKCTRL[17:16] IDLEST	Idle status
EMIF2	Slave	CM_EMIF_EMIF2_CLKCTRL[17:16] IDLEST	Idle status
EMIF_OCP_FW	Slave	CM_EMIF_EMIF_OCP_FW_CLKCTRL[17:16] IDLEST	Idle status

Table 3-200 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-200. CD_EMIF Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
DMM	N/A	Available	N/A	CM_EMIF_DMM_CLKCTRL[1:0] MODULEMODE	Read only
EMIF1	Available	Available	N/A	CM_EMIF_EMIF1_CLKCTRL[1:0] MODULEMODE	Read/write
EMIF2	Available	Available	N/A	CM_EMIF_EMIF2_CLKCTRL[1:0] MODULEMODE	Read/write
EMIF_OCP_FW	N/A	Available	N/A	CM_EMIF_EMIF_OCP_FW_CLKCTRL[1:0] MODULEMODE	Read only

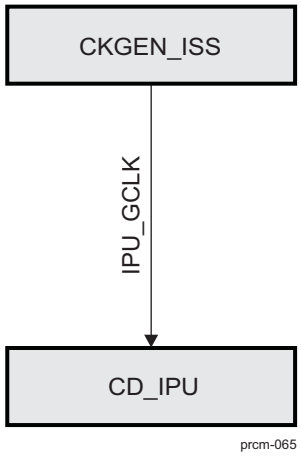
3.6.20 CD_IPU Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.20.1 Overview

Figure 3-72 is an overview of the clock domain.

Figure 3-72. CD_IPU Overview



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3.6.20.2 Clock Domain Modes

Table 3-201 lists the clock domain modes supported by the clock domain.

Table 3-201. CD_IPU Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-202 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-202. CD_IPU Control and Status Parameters

Parameter Name	Control/Status Bit Field
IPU_GCLK Clock Status	CM_IPU_CLKSTCTRL[8] CLKACTIVITY_IPU_GCLK
Clock Domain State Transition Control	CM_IPU_CLKSTCTRL[1:0] CLKTRCTRL

3.6.20.3 Clock Domain Dependency

CD_IPU has no module wake-up dependency with any other clock domain of the device.

3.6.20.3.1 Static Dependency

Table 3-203 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-203. CD_IPU Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_IPU_STATICDEP[3] ABE_STATDEP	Read/write
CD_DSS	Disabled	CM_IPU_STATICDEP[8] DSS_STATDEP	Read/write
CD_GPU	Disabled	CM_IPU_STATICDEP[10] GPU_STATDEP	Read/write
CD_CAM	Always disabled	CM_IPU_STATICDEP[9] CAM_STATDEP	Read only
CD_IVA	Disabled	CM_IPU_STATICDEP[2] IVA_STATDEP	Read/write
CD_L3_MAIN1	Enabled	CM_IPU_STATICDEP[5] L3MAIN1_STATDEP	Read/write
CD_L3_MAIN2	Enabled	CM_IPU_STATICDEP[6] L3MAIN2_STATDEP	Read/write
CD_L3INIT	Disabled	CM_IPU_STATICDEP[7] L3INIT_STATDEP	Read/write
CD_L4_CFG	Enabled	CM_IPU_STATICDEP[12] L4CFG_STATDEP	Read/write
CD_L4_PER	Disabled	CM_IPU_STATICDEP[13] L4PER_STATDEP	Read/write
CD_L4_SEC	Disabled	CM_IPU_STATICDEP[14] L4SEC_STATDEP	Read/write
CD_EMIF	Enabled	CM_IPU_STATICDEP[4] EMIF_STATDEP	Read/write
CD_DMA	Always disabled	CM_IPU_STATICDEP[11] SDMA_STATDEP	Read only
CD_DSP	Disabled	CM_IPU_STATICDEP[1] DSP_STATDEP	Read/write
CD_WKUPAON	Enabled	CM_IPU_STATICDEP[15] WKUPAON_STATDEP	Read/write

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Table 3-203. CD_IPU Static Dependency Association Parameters (continued)

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_COREAON	Always disabled	CM_IPU_STATICDEP[16] COREAON_STATDEP	Read only
CD_CUSTEFUSE	Always disabled	CM_IPU_STATICDEP[17] CUSTEFUSE_STATDEP	Read only

3.6.20.3.2 Dynamic Dependency

Table 3-204 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-204. CD_IPU Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_CAM	Alway disabled	CM_IPU_DYNAMICDEP[9] CAM_DYNDEP	Read only
CD_L3_MAIN2	Always enabled	CM_IPU_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only

3.6.20.4 Clock Domain Module Attributes

Table 3-205 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-205. CD_IPU Modules Clocks Association

Module	Clock	Clock Type
IPU	IPU_GCLK	Interface and functional

Table 3-206 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-206. CD_IPU Modules Wake-Up Request

Module	Wake-Up Feature
IPU	Master wake-up request

Table 3-207 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-207. CD_IPU Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
IPU	Master/slave	CM_IPU_IPU_CLKCTRL[18] STBYST	Standby status
		CM_IPU_IPU_CLKCTRL[17:16] IDLEST	Idle status

Table 3-208 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-208. CD_IPU Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
IPU	Available	Available	N/A	CM_IPU_IPU_CLKCTRL[1:0] MODULEMODE	Read/write

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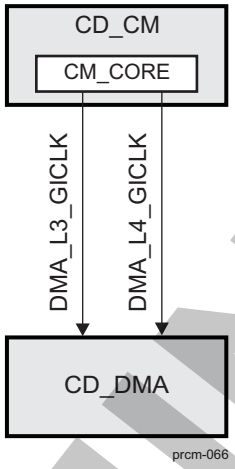
3.6.21 CD_DMA Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.21.1 Overview

Figure 3-73 is an overview of the clock domain.

Figure 3-73. CD_DMA Overview



3.6.21.2 Clock Domain Modes

Table 3-209 lists the clock domain modes supported by the clock domain.

Table 3-209. CD_DMA Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Not available	Available	Available

Table 3-210 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-210. CD_DMA Control and Status Parameters

Parameter Name	Control/Status Bit Field
DMA_L3_GICLK Clock Status	CM_DMA_CLKSTCTRL[8] CLKACTIVITY_DMA_L3_GICLK
Clock Domain State Transition Control	CM_DMA_CLKSTCTRL[1:0] CLKTRCTRL

3.6.21.3 Clock Domain Dependency

CD_DMA has no module wake-up dependency with any other clock domain of the device.

3.6.21.3.1 Static Dependency

Table 3-211 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-211. CD_DMA Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_ABE	Disabled	CM_DMA_STATICDEP[3] ABE_STATDEP	Read/write
CD_DSS	Disabled	CM_DMA_STATICDEP[8] DSS_STATDEP	Read/write

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Table 3-211. CD_DMA Static Dependency Association Parameters (continued)

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_CAM	Alway disabled	CM_DMA_STATICDEP[9] CAM_STATDEP	Read only
CD_IVA	Disabled	CM_DMA_STATICDEP[2] IVA_STATDEP	Read/write
CD_L3_MAIN1	Enabled	CM_DMA_STATICDEP[5] L3MAIN1_STATDEP	Read/write
CD_L3_MAIN2	Enabled	CM_DMA_STATICDEP[6] L3MAIN2_STATDEP	Read only
CD_L3INIT	Enabled	CM_DMA_STATICDEP[7] L3INIT_STATDEP	Read/write
CD_L4_CFG	Enabled	CM_DMA_STATICDEP[12] L4CFG_STATDEP	Read/write
CD_L4_PER	Enabled	CM_DMA_STATICDEP[13] L4PER_STATDEP	Read/write
CD_EMIF	Enabled	CM_IPU_STATICDEP[4] EMIF_STATDEP	Read/write
CD_WKUPAON	Enabled	CM_DMA_STATICDEP[15] WKUPAON_STATDEP	Read/write
CD_IPU	Disabled	CM_DMA_STATICDEP[0] IPU_STATDEP	Read/write

3.6.21.3.2 Dynamic Dependency

Table 3-212 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-212. CD_DMA Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN2	Always disabled	CM_DMA_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only

3.6.21.4 Clock Domain Module Attributes

Table 3-213 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-213. CD_DMA Modules Clocks Association

Module	Clock	Clock Type
DMA_SYSTEM	DMA_L3_GICLK	Interface and functional
	DMA_L4_GICLK	Interface

Table 3-214 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-214. CD_DMA Modules Wake-Up Request

Module	Wake-Up Feature
DMA_SYSTEM	Master wake-up request

Table 3-215 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

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Table 3-215. CD_DMA Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
DMA_SYSTEM	Master/slave	CM_DMA_DMA_SYSTEM_CLKCTRL[18] STBYST	Standby status
		CM_DMA_DMA_SYSTEM_CLKCTRL[17:16] IDLEST	Idle status

Table 3-216 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-216. CD_DMA Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
DMA_SYSTEM	N/A	Available	N/A	CM_DMA_DMA_SYSTEM_CLKCTRL[1:0] MODULEMODE	Read only

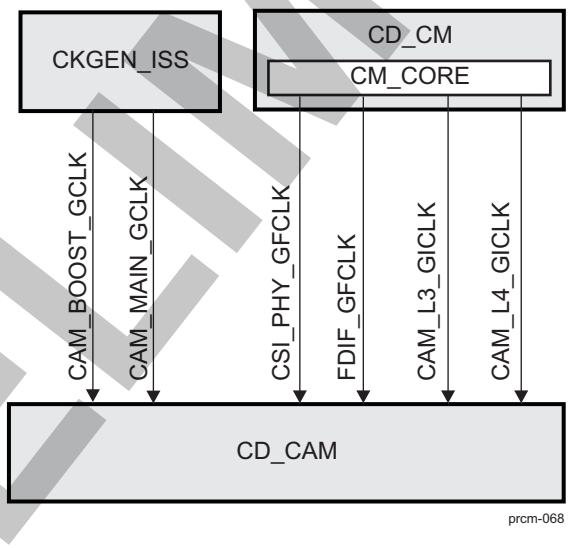
3.6.22 CD_CAM Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.22.1 Overview

Figure 3-74 is an overview of the clock domain.

Figure 3-74. CD_CAM Overview



The CKGEN_ISS (clock generator) is not part of the PRCM module. It is in the ISS.

3.6.22.2 Clock Domain Modes

Table 3-217 lists the clock domain modes supported by the clock domain.

Table 3-217. CD_CAM Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

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Table 3-218 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-218. CD_CAM Control and Status Parameters

Parameter Name	Control/Status Bit Field
CSI_PHY_GFCLK Clock Status	CM_CAM_CLKSTCTRL[9] CLKACTIVITY_CSI_PHY_GFCLK
CSI_PHY_GFCLK Clock Control	CM_CAM_ISS_CLKCTRL[8] OPTFCLKEN_CTRLCLK
FDIF_GFCLK Clock Status	CM_CAM_CLKSTCTRL[10] CLKACTIVITY_FDIF_GCLK
FDIF_GFCLK Clock Control	CM_CAM_FDIF_CLKCTRL[24] CLKSEL_FCLK
CAM_MAIN_GCLK Clock Status	CM_CAM_CLKSTCTRL[8] CLKACTIVITY_CAM_GCLK
CAM_L3_GICLK Clock Status	CM_CAM_CLKSTCTRL[12] CLKACTIVITY_CAM_L3_GICLK
CAM_BOOST_GCLK Clock Status	CM_CAM_CLKSTCTRL[11] CLKACTIVITY_CAM_BOOST_GCLK
Clock Domain State Transition Control	CM_CAM_CLKSTCTRL[1:0] CLKTRCTRL

3.6.22.3 Clock Domain Dependency

CD_CAM has no module wake-up dependency with any other clock domain of the device.

3.6.22.3.1 Static Dependency

Table 3-219 lists the static dependency of the clock domain with respect to other clock domains of the device.

Table 3-219. CD_CAM Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_IVA	Disabled	CM_CAM_STATICDEP[2] IVA_STATDEP	Read/write
CD_L3_MAIN1	Disabled	CM_CAM_STATICDEP[5] L3MAIN1_STATDEP	Read/write
CD_L3_MAIN2	Always enabled	CM_CAM_STATICDEP[6] L3MAIN2_STATDEP	Read only
CD_EMIF	Disabled	CM_CAM_STATICDEP[4] EMIF_STATDEP	Read/write

3.6.22.3.2 Dynamic Dependency

Table 3-220 lists the dynamic dependency of the clock domain with respect to other clock domains of the device.

Table 3-220. CD_CAM Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_MAIN2	Alway disabled	CM_CAM_DYNAMICDEP[6] L3MAIN2_DYNDEP	Read only

3.6.22.4 Clock Domain Module Attributes

Table 3-221 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-221. CD_CAM Modules Clocks Association

Module	Clock	Clock Type
FDIF	FDIF_GCLK	Interface and functional
ISS	CAM_BOOST_GCLK	Functional

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Table 3-221. CD_CAM Modules Clocks Association (continued)

Module	Clock	Clock Type
	CSI_PHY_GFCLK	Functional
	CAM_MAIN_GCLK	Interface

Table 3-222 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-222. CD_CAM Modules Wake-Up Request

Module	Wake-Up Feature
FDIF	None
ISS	None

Table 3-223 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-223. CD_CAM Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
FDIF	Master/slave	CM_CAM_FDIF_CLKCTRL[18] STBYST	Standby status
		CM_CAM_FDIF_CLKCTRL[17:16] IDLEST	Idle status
ISS	Master/slave	CM_CAM_ISS_CLKCTRL[18] STBYST	Standby status
		CM_CAM_ISS_CLKCTRL[17:16] IDLEST	Idle status

Table 3-224 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-224. CD_CAM Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
FDIF	Available	N/A	Available	CM_CAM_FDIF_CLKCTRL[1:0] MODULEMODE	Read/write
ISS	Available	N/A	Available	CM_CAM_ISS_CLKCTRL[1:0] MODULEMODE	Read/write

NOTE: In order to enable and access ISS module, first the IPU module must be enabled and the reset for CACHE_IPU and CACHE_MMU_IPU must be cleared.

3.6.23 CD_ABE Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.23.1 Overview

Figure 3-75 is an overview of the clock domain.

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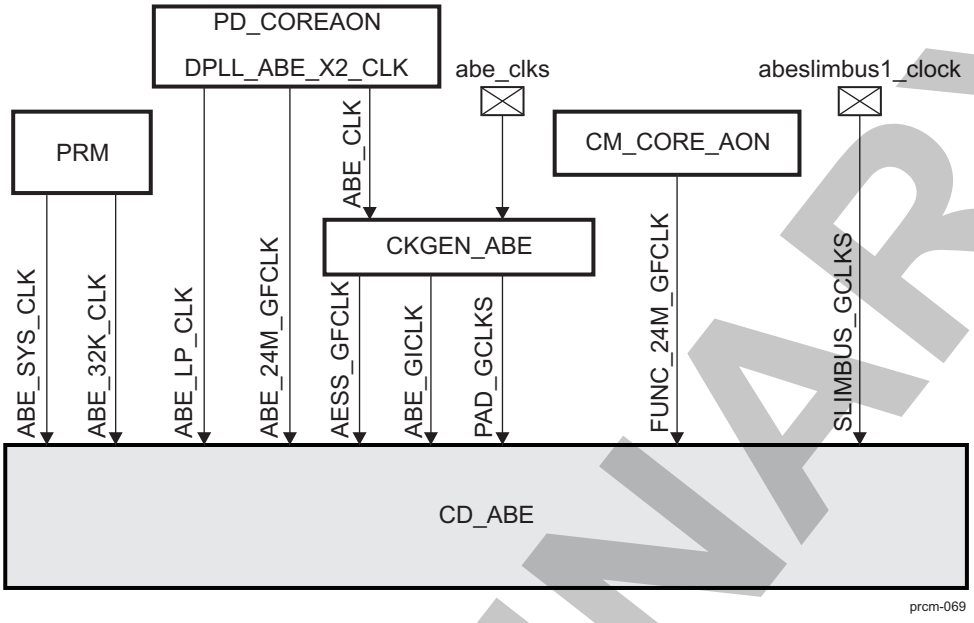
Figure 3-75. CD_ABE Overview



3.6.23.2 Clock Domain Modes

Table 3-225 lists the clock domain modes supported by the clock domain.

Table 3-225. CD_ABE Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	Available	Available	Available

Table 3-226 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-226. CD_ABE Control and Status Parameters

Parameter Name	Control/Status Bit Field
ABE_24M_GFCLK Clock Status	CM_ABE_CLKSTCTRL[13] CLKACTIVITY_ABE_24M_GFCLK
ABE_32K_CLK Clock Status	CM_ABE_CLKSTCTRL[12] CLKACTIVITY_ABE_32K_CLK
ABE_SYS_CLK Clock Status	CM_ABE_CLKSTCTRL[11] CLKACTIVITY_ABE_SYS_CLK
DPLL_ABE_X2_CLK Clock Status	CM_ABE_CLKSTCTRL[8] CLKACTIVITY_ABE_X2_CLK
FUNC_24M_GFCLK Clock Status	CM_ABE_CLKSTCTRL[10] CLKACTIVITY_FUNC_24M_GFCLK
ABE_GICLK Clock Status	CM_ABE_CLKSTCTRL[9] CLKACTIVITY_ABE_GICLK
AESS_GFCLK Clock Control	CM_ABE_AESS_CLKCTRL[24] CLKSEL_AESS_GFCLK
Clock Domain State Transition Control	CM_ABE_CLKSTCTRL[1:0] CLKTRCTRL

3.6.23.3 Clock Domain Dependency

CD_ABE has no static or dynamic dependency with any other clock domain of the device.

3.6.23.3.1 Wake-Up Dependency

Table 3-227 lists the wake-up dependency settings for the modules of this clock in the clock domain

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Table 3-227. CD_ABE Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
DMIC	CD_ABE	CD_DMA, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_ABE_DMIC_WKDEP[7] WKUPDEP_DMIC_DMA_SDMA	Read/write
DMIC	CD_ABE	CD_DSP	Disabled	PM_ABE_DMIC_WKDEP[6] WKUPDEP_DMIC_DMA_DSP	Read/write
DMIC	CD_ABE	CD_DSP	Disabled	PM_ABE_DMIC_WKDEP[2] WKUPDEP_DMIC_IRQ_DSP	Read/write
DMIC	CD_ABE	CD_MPU	Disabled	PM_ABE_DMIC_WKDEP[0] WKUPDEP_DMIC_IRQ_MPU	Read/write
MCASP	CD_ABE	CD_DMA, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_ABE_MCASP_WKDEP[7] WKUPDEP_MCASP_DMA_SDMA	Read/write
MCASP	CD_ABE	CD_DSP	Disabled	PM_ABE_MCASP_WKDEP[6] WKUPDEP_MCASP_DMA_DSP	Read/write
MCASP	CD_ABE	CD_DSP	Disabled	PM_ABE_MCASP_WKDEP[2] WKUPDEP_MCASP_IRQ_DSP	Read/write
MCASP	CD_ABE	CD_MPU	Disabled	PM_ABE_MCASP_WKDEP[0] WKUPDEP_MCASP_IRQ_MPU	Read/write
MCBSP1	CD_ABE	CD_DMA, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_ABE_MCBSP1_WKDEP[3] WKUPDEP_MCBSP1_SDMA	Read/write
MCBSP1	CD_ABE	CD_DSP	Disabled	PM_ABE_MCBSP1_WKDEP[2] WKUPDEP_MCBSP1_DSP	Read/write
MCBSP1	CD_ABE	CD_MPU	Disabled	PM_ABE_MCBSP1_WKDEP[0] WKUPDEP_MCBSP1_MPU	Read/write
MCBSP2	CD_ABE	CD_DMA, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_ABE_MCBSP2_WKDEP[3] WKUPDEP_MCBSP2_SDMA	Read/write
MCBSP2	CD_ABE	CD_DSP	Disabled	PM_ABE_MCBSP2_WKDEP[2] WKUPDEP_MCBSP2_DSP	Read/write
MCBSP2	CD_ABE	CD_MPU	Disabled	PM_ABE_MCBSP2_WKDEP[0] WKUPDEP_MCBSP2_MPU	Read/write
MCBSP3	CD_ABE	CD_DMA, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_ABE_MCBSP3_WKDEP[3] WKUPDEP_MCBSP3_SDMA	Read/write

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Table 3-227. CD_ABE Wake-Up Dependency Association Parameters (continued)

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
MCBSP3	CD_ABE	CD_DSP	Disabled	PM_ABE_MCBSP3_WKDEP[2] WKUPDEP_MCBSP3_DSP	Read/write
MCBSP3	CD_ABE	CD_MPU	Disabled	PM_ABE_MCBSP3_WKDEP[0] WKUPDEP_MCBSP3_MPU	Read/write
MCPDM	CD_ABE	CD_DMA, CD_L3_MAIN1, CD_L3_MAIN2	Disabled	PM_ABE_MCPDM_WKDEP[7] WKUPDEP_MCPDM_DMA_SDMA	Read/write
MCPDM	CD_ABE	CD_DSP	Disabled	PM_ABE_MCPDM_WKDEP[6] WKUPDEP_MCPDM_DMA_DSP	Read/write
MCPDM	CD_ABE	CD_DSP	Disabled	PM_ABE_MCPDM_WKDEP[2] WKUPDEP_MCPDM_IRQ_DSP	Read/write
MCPDM	CD_ABE	CD_MPU	Disabled	PM_ABE_MCPDM_WKDEP[0] WKUPDEP_PDM_IRQ_MPU	Read/write
TIMER5	CD_ABE	CD_DSP	Disabled	PM_ABE_TIMER5_WKDEP[2] WKUPDEP_TIMER5_DSP	Read/write
TIMER5	CD_ABE	CD_MPU	Disabled	PM_ABE_TIMER5_WKDEP[0] WKUPDEP_TIMER5_MPU	Read/write
TIMER6	CD_ABE	CD_DSP	Disabled	PM_ABE_TIMER6_WKDEP[2] WKUPDEP_TIMER6_DSP	Read/write
TIMER6	CD_ABE	CD_MPU	Disabled	PM_ABE_TIMER6_WKDEP[0] WKUPDEP_TIMER6_MPU	Read/write
TIMER7	CD_ABE	CD_DSP	Disabled	PM_ABE_TIMER7_WKDEP[2] WKUPDEP_TIMER7_DSP	Read/write
TIMER7	CD_ABE	CD_MPU	Disabled	PM_ABE_TIMER7_WKDEP[0] WKUPDEP_TIMER7_MPU	Read/write
TIMER8	CD_ABE	CD_DSP	Disabled	PM_ABE_TIMER8_WKDEP[2] WKUPDEP_TIMER8_DSP	Read/write
TIMER8	CD_ABE	CD_MPU	Disabled	PM_ABE_TIMER8_WKDEP[0] WKUPDEP_TIMER8_MPU	Read/write
WD_TIMER3	CD_ABE	CD_MPU	Enabled	PM_ABE_WD_TIMER3_WKDEP[0] WKUPDEP_WD_TIMER3_MPU	Read/write

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3.6.23.4 Clock Domain Module Attributes

Table 3-228 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-228. CD_ABE Modules Clocks Association

Module	Clock	Clock Type
AESS	AESS_GFCLK	Functional
	ABE_GICLK	Interface
DMIC	DMIC_GFCLK	Functional
	ABE_GICLK	Interface
L4_ABE interconnect	ABE_GICLK	Interface
MCASP	MCASP_GFCLK	Functional
	ABE_GICLK	Interface and functional
MCBSP1	MCBSP1_GFCLK	Functional
	ABE_GICLK	Interface
MCBSP2	MCBSP2_GFCLK	Functional
	ABE_GICLK	Interface
MCBSP3	MCBSP3_GFCLK	Functional
	ABE_GICLK	Interface
MCPDM	ABE_GICLK	Interface
	PAD_GCLKS	Functional
TIMER5	TIMER5_GFCLK	Functional
	ABE_GICLK	Interface
TIMER6	TIMER6_GFCLK	Functional
	ABE_GICLK	Interface
TIMER7	TIMER7_GFCLK	Functional
	ABE_GICLK	Interface
TIMER8	TIMER8_GFCLK	Functional
	ABE_GICLK	Interface
WD_TIMER3	ABE_32K_CLK	Functional
	ABE_GICLK	Interface

Table 3-229 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-229. CD_ABE Modules Wake-Up Request

Module	Wake-Up Feature
AESS	None
DMIC	Slave wake-up request (MPU-IRQ, DSP-IRQ and DMA, DMA_SYSTEM-DMA)
L4_ABE interconnect	None
MCASP	Slave wake-up request (MPU-IRQ, DSP-IRQ and DMA, DMA_SYSTEM-DMA)
MCBSP1	Slave wake-up request (MPU-IRQ, DSP-IRQ and DMA, DMA_SYSTEM-DMA)
MCBSP2	Slave wake-up request (MPU-IRQ, DSP-IRQ and DMA, DMA_SYSTEM-DMA)
MCBSP3	Slave wake-up request (MPU-IRQ, DSP-IRQ and DMA, DMA_SYSTEM-DMA)
MCPDM	Slave wake-up request (MPU-IRQ, DSP-IRQ and DMA, DMA_SYSTEM-DMA)
TIMER5	Slave wake-up request (MPU-IRQ, DSP-IRQ)

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Table 3-229. CD_ABE Modules Wake-Up Request (continued)

Module	Wake-Up Feature
TIMER6	Slave wake-up request (MPU-IRQ, DSP-IRQ)
TIMER7	Slave wake-up request (MPU-IRQ, DSP-IRQ)
TIMER8	Slave wake-up request (MPU-IRQ, DSP-IRQ)
WD_TIMER3	Slave wake-up request (MPU-IRQ)

Table 3-230 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-230. CD_ABE Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
AESS	Slave/master	CM_ABE_AESS_CLKCTRL[18] STBYST	Standby status
		CM_ABE_AESS_CLKCTRL[17:16] IDLEST	Idle status
DMIC	Slave	CM_ABE_DMIC_CLKCTRL[17:16] IDLEST	Idle status
L4_ABE interconnect	Slave	CM_ABE_L4_ABE_CLKCTRL[17:16] IDLEST	Idle status
MCASP	Slave	CM_ABE_MCASP_CLKCTRL[17:16] IDLEST	Idle status
MCBSP1	Slave	CM_ABE_MCBSP1_CLKCTRL[17:16] IDLEST	Idle status
MCBSP2	Slave	CM_ABE_MCBSP2_CLKCTRL[17:16] IDLEST	Idle status
MCBSP3	Slave	CM_ABE_MCBSP3_CLKCTRL[17:16] IDLEST	Idle status
MCPDM	Slave	CM_ABE_MCPDM_CLKCTRL[17:16] IDLEST	Idle status
TIMER5	Slave	CM_ABE_TIMER5_CLKCTRL[17:16] IDLEST	Idle status
TIMER6	Slave	CM_ABE_TIMER6_CLKCTRL[17:16] IDLEST	Idle status
TIMER7	Slave	CM_ABE_TIMER7_CLKCTRL[17:16] IDLEST	Idle status
TIMER8	Slave	CM_ABE_TIMER8_CLKCTRL[17:16] IDLEST	Idle status
WD_TIMER3	Slave	CM_ABE_WD_TIMER3_CLKCTRL[17:16] IDLEST	Idle status

Table 3-231 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-231. CD_ABE Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
AESS	Available	N/A	Available	CM_ABE_AESS_CLKCTRL[1:0] MODULEMODE	Read/write
DMIC	Available	N/A	Available	CM_ABE_DMIC_CLKCTRL[1:0] MODULEMODE	Read/write
L4_ABE interconnect	N/A	Available	N/A	CM_ABE_L4_ABE_CLKCTRL[1:0] MODULEMODE	Read only

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Table 3-231. CD_ABE Modules Slave Clock-Management Modes and Control (continued)

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
MCASP	Available	N/A	Available	CM_ABE_MCASP_CLKCTRL[1:0] MODULEMODE	Read/write
MCBSP1	Available	N/A	Available	CM_ABE_MCBSP1_CLKCTRL[1:0] MODULEMODE	Read/write
MCBSP2	Available	N/A	Available	CM_ABE_MCBSP2_CLKCTRL[1:0] MODULEMODE	Read/write
MCBSP3	Available	N/A	Available	CM_ABE_MCBSP3_CLKCTRL[1:0] MODULEMODE	Read/write
MCPDM	Available	N/A	Available	CM_ABE_MCPDM_CLKCTRL[1:0] MODULEMODE	Read/write
TIMER5	Available	N/A	Available	CM_ABE_TIMER5_CLKCTRL[1:0] MODULEMODE	Read/write
TIMER6	Available	N/A	Available	CM_ABE_TIMER6_CLKCTRL[1:0] MODULEMODE	Read/write
TIMER7	Available	N/A	Available	CM_ABE_TIMER7_CLKCTRL[1:0] MODULEMODE	Read/write
TIMER8	Available	N/A	Available	CM_ABE_TIMER8_CLKCTRL[1:0] MODULEMODE	Read/write
WD_TIMER3	Available	N/A	Available	CM_ABE_WD_TIMER3_CLKCTRL[1:0] MODULEMODE	Read/write

3.6.24 CD_COREAON_L4 Clock Domain

This section identifies the modes supported by the clock domain and the associated control and status bits. It also identifies its dependencies with other clock domains of the device.

3.6.24.1 CD_COREAON_L4 Overview

Figure 3-76 is an overview of the clock domain.

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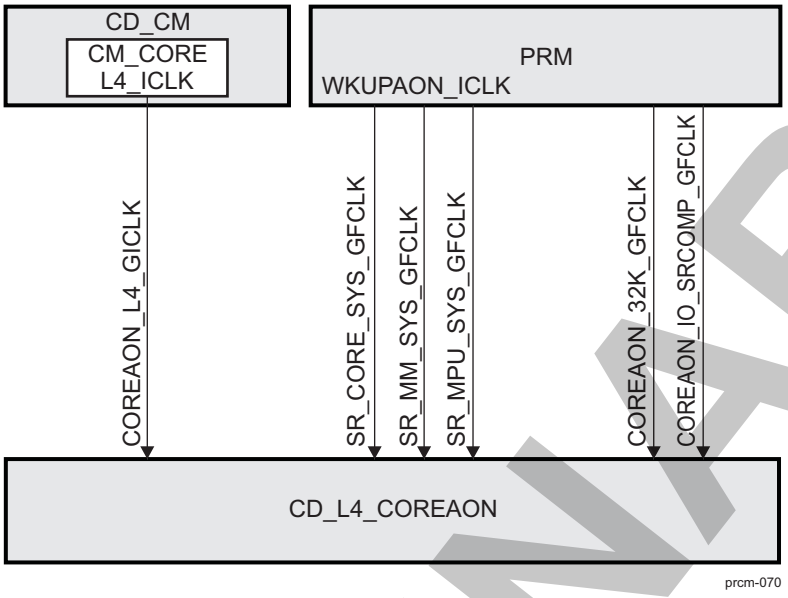
Figure 3-76. CD_COREAON_L4 Overview



3.6.24.2 Clock Domain Modes

Table 3-232 lists the clock domain modes supported by the clock domain.

Table 3-232. CD_COREAON_L4 Clock Domain Modes

NO_SLEEP	SW_SLEEP	SW_WKUP	HW_AUTO
Available	N/A	Available	Available

Table 3-233 lists the clock domain state transition control and status bits for the clock in this clock domain.

Table 3-233. CD_COREAON_L4 Control and Status Parameters

Parameter Name	Control/Status Bit Field
COREAON_32K_GFCLK Clock Status	CM_COREAON_CLKSTCTRL[12] CLKACTIVITY_COREAON_32K_GFCLK
COREAON_32K_GFCLK Clock Control	CM_COREAON_USB_PHY_CORE_CLKCTRL[8] OPTFCLKEN_CLK32K
SR_CORE_SYS_GFCLK Clock Status	CM_COREAON_CLKSTCTRL[11] CLKACTIVITY_SR_CORE_SYS_GFCLK
SR_MM_SYS_GFCLK Clock Status	CM_COREAON_CLKSTCTRL[10] CLKACTIVITY_SR_MM_SYS_GFCLK
SR_MPU_SYS_GFCLK Clock Status	CM_COREAON_CLKSTCTRL[9] CLKACTIVITY_SR_MPU_SYS_GFCLK
COREAON_L4_GICLK Clock Status	CM_COREAON_CLKSTCTRL[8] CLKACTIVITY_COREAON_L4_GICLK
COREAON_IO_SRCOMP_GFCLK Clock Status	CM_COREAON_CLKSTCTRL[14] CLKACTIVITY_COREAON_IO_SRCOMP_GFCLK
COREAON_IO_SRCOMP_GFCLK Clock Control	CM_COREAON_IO_SRCOMP_CLKCTRL[8] CLKEN_SRCOMP_FCLK
Clock Domain State Transition Control	CM_COREAON_CLKSTCTRL[1:0] CLKTRCTRL

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3.6.24.3 Clock Domain Dependency

CD_COREAON_L4 has no static or dynamic dependency with any other clock domain of the device.

3.6.24.3.1 Wake-Up Dependency

Table 3-234 lists the wake-up dependency settings for the modules of this clock domain.

Table 3-234. CD_COREAON_L4 Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
SMARTREFLEX_CORE	CD_COREAON_L4	CD_IPU, CD_L3_MAIN2, CD_L3_MAIN1, CD_L4_CFG	Disabled	PM_COREAON_SMARTREFLEX_CORE_WKDEP[1] WKUPDEP_SMARTREFLEX_CORE_IPU	Read/write
	CD_COREAON_L4	CD_MPU, CD_L3_MAIN1, CD_L4_CFG	Disabled	PM_COREAON_SMARTREFLEX_CORE_WKDEP[0] WKUPDEP_SMARTREFLEX_CORE_MPU	Read/write
SMARTREFLEX_MM	CD_COREAON_L4	CD_MPU, CD_L3_MAIN1, CD_L4_CFG	Disabled	PM_COREAON_SMARTREFLEX_MM_WKDEP[0] WKUPDEP_SMARTREFLEX_MM_MPU	Read/write
SMARTREFLEX_MPU	CD_COREAON_L4	CD_MPU, CD_L3_MAIN1, CD_L4_CFG	Enabled	PM_COREAON_SMARTREFLEX_MPU_WKDEP[0] WKUPDEP_SMARTREFLEX_MPU_MPU	Read/write

3.6.24.4 Clock Domain Module Attributes

Table 3-235 lists for each module of the clock domain the clocks the module receives and their role (that is, functional or interface clock).

Table 3-235. CD_COREAON_L4 Modules Clocks Association

Module	Clock	Clock Type
SMARTREFLEX_CORE	COREAON_L4_GICLK	Interface
	SR_CORE_SYS_GFCLK	Functional
SMARTREFLEX_MM	COREAON_L4_GICLK	Interface
	SR_MM_SYS_GFCLK	Functional
SMARTREFLEX_MPU	COREAON_L4_GICLK	Interface
	SR_MPU_SYS_GFCLK	Functional
USB_PHY_CORE	COREAON_32K_GFCLK	Functional
IO_SRCOMP_CORE	COREAON_IO_SRCOMP_GFCLK	Functional

Table 3-236 lists the supported wake-up request generation capability for each module of the clock domain.

Table 3-236. CD_COREAON_L4 Modules Wake-Up Request

Module	Wake-Up Feature
SMARTREFLEX_CORE	Slave wake-up request (MPU-IRQ, IPU-IRQ)
SMARTREFLEX_MM	Slave wake-up request (MPU-IRQ)

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Table 3-236. CD_COREAON_L4 Modules Wake-Up Request (continued)

Module	Wake-Up Feature
SMARTREFLEX_MPU	Slave wake-up request (MPU-IRQ)
USB_PHY_CORE	None
IO_SRCOMP_CORE	None

Table 3-237 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-237. CD_COREAON_L4 Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
SMARTREFLEX_CORE	Slave	CM_COREAON_SMARTREFLEX_CORE_CLKCTRL[17:16] IDLEST	Idle status
SMARTREFLEX_MM	Slave	CM_COREAON_SMARTREFLEX_MM_CLKCTRL[17:16] IDLEST	Idle status
SMARTREFLEX_MPU	Slave	CM_COREAON_SMARTREFLEX_MPU_CLKCTRL[17:16] IDLEST	Idle status

Table 3-238 lists the supported clock-management modes and associated software control bit fields for each module of the power domain.

Table 3-238. CD_COREAON_L4 Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
SMARTREFLEX_CORE	Available	N/A	Available	CM_COREAON_SMARTREFLEX_CORE_CLKCTRL[1:0] MODULEMODE	Read/write
SMARTREFLEX_MM	Available	N/A	Available	CM_COREAON_SMARTREFLEX_MM_CLKCTRL[1:0] MODULEMODE	Read/write
SMARTREFLEX_MPU	Available	N/A	Available	CM_COREAON_SMARTREFLEX_MPU_CLKCTRL[1:0] MODULEMODE	Read/write

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3.7 Power Management Functional Description

This section describes the functional concepts of power management at the power domain level in the device.

The following power domains support dynamic power switching (DPS) with switching times of less than 5 µs.

- PD_CORE
- PD_DSP
- PD_MPU

For these three power domains, the "SWITCH_LOOPBACK" parameter of corresponding PSCON must be chosen correctly in order to allow loop-back of PONOUT to PGOODIN.

For other power domains, the "SWITCH_LOOPBACK" parameter will be chosen in the other way. A 10µs delay will be included by PSCON between PONIN and PGOODIN.

3.7.1 PD_WKUPAON Description

PD_WKUPAON contains the following reset domains:

- WKUPAON_PWRON_RST
- WKUPAON_RST
- WKUPAON_SYS_PWRON_RST
- PRM_PWRON_RST
- PRM_RST
- LPRM_PWRON_RST
- LPRM_RST

PD_WKUPAON contains the CD_WKUPAON clock domain.

Table 3-239 lists the logic retention capability for each module of the power domain.

Table 3-239. PD_WKUPAON Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
CTRL_MODULE_WKUP	No	None	None
GPIO1	No	RM_WKUPAON_GPIO1_CONTEXT[0] LOSTCONTEXT_DFF	None
KBD	No	RM_WKUPAON_KBD_CONTEXT[0] LOSTCONTEXT_DFF	None
PRCM_MPU	No	None	None
SAR_RAM	No	RM_WKUPAON_SAR_RAM_CONTEXT[0] LOSTCONTEXT_DFF	None
SCRM	No	None	None
COUNTER_32K	No	RM_WKUPAON_COUNTER_32K_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER1	No	RM_WKUPAON_TIMER1_CONTEXT[0] LOSTCONTEXT_DFF	None
WD_TIMER2	No	RM_WKUPAON_WD_TIMER2_CONTEXT[0] LOSTCONTEXT_DFF	None
L4_WKUP interconnect	No	RM_WKUPAON_L4_WKUP_CONTEXT[0] LOSTCONTEXT_DFF	None
PRM	No	None	None
IO_SRCOMP_WKUP	No	None	None

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3.7.1.1 Power Domain Modes

The PD_WKUPAON power domain is an always-on power domain and does not switch to RETENTION state. There is no logic power state control or status bit field for this power domain.

The PD_WKUPAON power domain has one memory bank, sar_bank, which is related to SAR_RAM.

3.7.1.1.1 Logic and Memory Area Power Modes

Table 3-240 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention columns in the table identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

Table 3-240. PD_WKUPAON Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention	Logic Off
WKUP_BANK		ON		

3.7.2 PD_DSP Description

PD_DSP contains the following reset domains:

- DSP_RST
- DSP_PWRON_RST
- DSP_RET_RST
- DSP_SYS_RST

PD_DSP contains the CD_DSP clock domain.

Table 3-241 lists the logic retention capability for each module of the power domain.

Table 3-241. PD_DSP Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DSP	Partial	RM_DSP_DSP_CONTEXT[0] LOSTCONTEXT_DFF	RM_DSP_DSP_CONTEXT[1] LOSTCONTEXT_RFF

3.7.2.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.2.1.1 Logic and Memory Area Power Modes

Table 3-242 lists the power modes supported by the logic area of the power domain.

Table 3-242. PD_DSP Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
Available	Available	Available

Table 3-243 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On and Logic Retention columns in the table identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

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Table 3-243. PD_DSP Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
DSP_DMA		ON	RETENTION
	DSP – DSP_DMA	always_on	always_retention
DSP_L1		ON	RETENTION
	DSP – DSP_L1	always_on	software_control
DSP_L2		ON	RETENTION
	DSP – DSP_L2	always_on	software_control

3.7.2.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-244 lists the power mode controls for the power domain.

Table 3-244. PD_DSP Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area – State Control (logic in RETENTION state)	DSP_L2	PM_DSP_PWRSTCTRL[9] DSP_L2_RETSTATE	Read/write
Memory Area – State Control (logic in RETENTION state)	DSP_L1	PM_DSP_PWRSTCTRL[8] DSP_L1_RETSTATE	Read/write
Power Domain – Low-Power State Change Control		PM_DSP_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/write
Memory Area – State Control (logic in ON state)	DSP_DMA	PM_DSP_PWRSTCTRL[21:20] DSP_EDMA_ONSTATE	Read only
Logic Area – Retention State Control		PM_DSP_PWRSTCTRL[2] LOGICRETSTATE	Read/write
Memory Area – State Control (logic in ON state)	DSP_L2	PM_DSP_PWRSTCTRL[19:18] DSP_L2_ONSTATE	Read only
Memory Area – State Control (logic in ON state)	DSP_L1	PM_DSP_PWRSTCTRL[17:16] DSP_L1_ONSTATE	Read only
Memory Area – State Control (logic in RETENTION state)	DSP_EDMA	PM_DSP_PWRSTCTRL[10] DSP_EDMA_RETSTATE	Read only
Power Domain – State Transition Control		PM_DSP_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 3-245 lists the power mode status for the power domain.

Table 3-245. PD_DSP Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain – Last Power State Entered Status		PM_DSP_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area – State Status	DSP_EDMA	PM_DSP_PWRSTST[9:8] DSP_EDMA_STATEST
Memory Area – State Status	DSP_L2	PM_DSP_PWRSTST[7:6] DSP_L2_STATEST
Memory Area – State Status	DSP_L1	PM_DSP_PWRSTST[5:4] DSP_L1_STATEST
Power Domain – State Transition Status		PM_DSP_PWRSTST[20] INTRANSITION
Logic Area – State Status		PM_DSP_PWRSTST[2] LOGICSTATEST
Power Domain – State Status		PM_DSP_PWRSTST[1:0] POWERSTATEST

3.7.3 PD_CUSTEFUSE Description

PD_CUSTEFUSE contains the following reset domains:

- CUSTEFUSE_RST

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PD_CUSTEFUSE contains the CD_CUSTEFUSE clock domain.

Table 3-241 lists the logic retention capability for each module of the power domain.

Table 3-246. PD_CUSTEFUSE Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
EFUSE_CTRL_CUST	No	RM_CUSTEFUSE_EFUSE_CTRL_CUST_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.3.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.3.1.1 Logic and Memory Area Power Modes

Table 3-242 lists the power modes supported by the logic area of the power domain.

Table 3-247. PD_CUSTEFUSE Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
N/A	Available	Available

Table 3-243 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On and Logic Retention columns in the table identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

There is no memory bank implemented for the PD_CUSTEFUSE.

3.7.3.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-244 lists the power mode controls for the power domain.

Table 3-248. PD_CUSTEFUSE Power Modes Control Parameters

Parameter Name	Control Bit Field	Access Type
Power Domain – Low-Power State Change Control	PM_CUSTEFUSE_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/write
Power Domain – State Transition Control	PM_CUSTEFUSE_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 3-245 lists the power mode status for the power domain.

Table 3-249. PD_CUSTEFUSE Power Modes Status Parameters

Parameter Name	Status Bit Field
Power Domain – Last Power State Entered Status	PM_CUSTEFUSE_PWRSTST[25:24] LASTPOWERSTATEENTERED
Power Domain – State Transition Status	PM_CUSTEFUSE_PWRSTST[20] INTRANSITION
Logic Area – State Status	PM_CUSTEFUSE_PWRSTST[2] LOGICSTATEST
Power Domain – State Status	PM_CUSTEFUSE_PWRSTST[1:0] POWERSTATEST

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3.7.4 PD_MPU Description

PD_MPU contains the following reset domains:

- MPU_PWRON_RST
- MPU_RST
- MPU_MA_RST
- MPU_MA_RET_RST
- MPU_MA_PWRON_RET_RST

PD_MPU contains the CD_MPU clock domain.

Table 3-250 lists the logic retention capability for each module of the power domain.

Table 3-250. PD_MPU Module Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
MPU	Partial	RM_MPU_MPU_CONTEXT[0] LOSTCONTEXT_DFF	RM_MPU_MPU_CONTEXT[1] LOSTCONTEXT_RFF

3.7.4.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.4.1.1 Logic and Memory Area Power Modes

Table 3-251 lists the power modes supported by the logic area of the power domain.

Table 3-251. PD_MPU Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
Available	Available	Available

Table 3-252 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On and Logic Retention columns in the table identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

Table 3-252. PD_MPU Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
MPU_L2		ON	RETENTION
	MPU – MPU_L2	always_on	software_control
MPU_RAM		ON	RETENTION
	MPU - MPU_RAM	always_on	software_control

3.7.4.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-253 lists the power mode controls for the power domain.

Table 3-253. PD_MPU Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area – State Control (logic in RETENTION state)	MPU_L2	PM_MPU_PWRSTCTRL[9] MPU_L2_RETSTATE	Read/write
Memory Area – State Control (logic in RETENTION state)	MPU_RAM	PM_MPU_PWRSTCTRL[10] MPU_RAM_RETSTATE	Read only

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Table 3-253. PD_MPU Power Modes Control Parameters (continued)

Parameter Name	Memory Bank	Control Bit Field	Access Type
Power Domain – Low-Power State Change Control		PM_MPU_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read only
Logic Area – Retention State Control		PM_MPU_PWRSTCTRL[2] LOGICRETSTATE	Read/write
Memory Area – State Control (logic in ON state)	MPU_L2	PM_MPU_PWRSTCTRL[19:18] MPU_L2_ONSTATE	Read only
Memory Area – State Control (logic in ON state)	MPU_RAM	PM_MPU_PWRSTCTRL[21:20] MPU_RAM_ONSTATE	Read only
Power Domain – State Transition Control		PM_MPU_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 3-254 lists the status of the power modes for the power domain.

Table 3-254. PD_MPU Power Mode Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain – Last Power State Entered Status		PM_MPU_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area – State Status	MPU_L2	PM_MPU_PWRSTST[7:6] MPU_L2_STATEST
Memory Area – State Status	MPU_RAM	PM_MPU_PWRSTST[9:8] MPU_RAM_STATEST
Power Domain – State Transition Status		PM_MPU_PWRSTST[20] INTRANSITION
Logic Area – State Status		PM_MPU_PWRSTST[2] LOGICSTATEST
Power Domain – State Status		PM_MPU_PWRSTST[1:0] POWERSTATEST

3.7.4.1.3 Power State Override

The PRCM module controls the power state of the MPU subsystem, whereas the PRCM_MPU controls the power state of each CPU (CPU0 and CPU1). The MPU subsystem requires that the MPU power domain can transition only to a low-power mode when CPU0 and CPU1 are in a lower power mode than is specified in the PM_MPU_PWRSTCTRL register. The power mode of the CPUs is communicated to the PRCM module by the PRCM_MPU through two dedicated internal signals. These two signals specify the lowest power state that the MPU can enter and, if necessary, override the low-power state programmed in the PM_MPU_PWRSTCTRL register.

Table 3-255 lists the low-power modes allowed by the MPU.

Table 3-255. MPU Allowed Low-Power Mode

MPU Allowed Low-Power Mode	Comment
CSWRET	CPUs are in SR3-APG mode and L1$ is in RETENTION state.
INACTIVE	CPUs are in SR3-APG mode and L1$ is in ON state, or CPUs are in INACTIVE state.
ON	CPUs are in ON state.

If PM_MPU_PWRSTCTRL is programmed to a lower power state than allowed (specified by the two signals), then it is overwritten by the hardware. The valued of the PM_MPU_PWRSTCTRL register is not changed (that is, not overwritten).

MPU subsystem guaranties that MPU_LP_ALLOWED[1:0] signals are steady before MPU subsystem STANDBY is asserted.

3.7.5 PD_L3INIT Description

PD_L3INIT contains the following reset domains:

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- DPLL_L3INIT_PWRON_RET_RST
- L3INIT_PWRON_RST
- L3INIT_RET_RST
- L3INIT_RST

PD_L3INIT contains the CD_L3INIT clock domain.

Table 3-256 lists the logic retention capability for each module of the power domain.

Table 3-256. PD_L3INIT Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DPLL_USB	Full	None	None
HSI	Full	None	RM_L3INIT_HSI_CONTEXT[1] LOSTCONTEXT_RFF
IEEE1500_2_OCP	No	RM_L3INIT_IEEE1500_2_OCP_CONTEXT[0] LOSTCONTEXT_DFF	None
MMC1	Full	None	RM_L3INIT_MMC1_CONTEXT [1] LOSTCONTEXT_RFF
MMC2	Full	None	RM_L3INIT_MMC2_CONTEXT [1] LOSTCONTEXT_RFF
USB_HOST_HS	Full	None	RM_L3INIT_USB_HOST_HS_CONTEXT[1] LOSTCONTEXT_RFF
USB_OTG_SS	Full	None	RM_L3INIT_USB_OTG_SS_CONTEXT[1] LOSTCONTEXT_RFF
USB_TLL_HS	Full	None	RM_L3INIT_USB_TLL_HS_CONTEXT[1] LOSTCONTEXT_RFF
SATA	No	RM_L3INIT_SATA_CONTEXT[0] LOSTCONTEXT_DFF	None
OCP2SCP1	No	RM_L3INIT_OCP2SCP1_CONTEXT [0] LOSTCONTEXT_DFF	None
OCP2SCP3	No	RM_L3INIT_OCP2SCP3_CONTEXT [0] LOSTCONTEXT_DFF	None

3.7.5.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.5.1.1 Logic and Memory Area Power Modes

Table 3-257 lists the power modes supported by the logic area of the power domain.

Table 3-257. PD_L3INIT Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
Available	Available	Available

Table 3-258 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On and Logic Retention columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

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Table 3-258. PD_L3INIT Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
L3INIT_BANK1		ON	
	HSI – HSI_DMAFIFO	always_on	always_off
	MMC1 – MMC_RAM	always_on	always_off
	MMC2 – MMC_RAM	always_on	always_off
	SATA – sata_bank	always_on	always_off
L3INIT_BANK2		ON	RETENTION
	USB_OTG_SS – USB_MEM	always_on	always_retention

3.7.5.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-259 lists the power modes controls for the power domain.

Table 3-259. PD_L3INIT Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area – State Control (logic in RETENTION state)	L3INIT_BANK1	PM_L3INIT_PWRSTCTRL[8] L3INIT_BANK1_RETSTATE	Read only
Memory Area – State Control (logic in RETENTION state)	L3INIT_BANK2	PM_L3INIT_PWRSTCTRL[9] L3INIT_BANK2_RETSTATE	Read only
Power Domain – Low-Power State Change Control		PM_L3INIT_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/write
Logic Area – RETENTION State Control		PM_L3INIT_PWRSTCTRL[2] LOGICRETSTATE	Read/write
Memory Area – State Control (logic in ON state)	L3INIT_BANK1	PM_L3INIT_PWRSTCTRL[17:16] L3INIT_BANK1_ONSTATE	Read only
Memory Area – State Control (logic in ON state)	L3INIT_BANK2	PM_L3INIT_PWRSTCTRL[19:18] L3INIT_BANK2_ONSTATE	Read only
Power Domain – State Transition Control		PM_L3INIT_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 3-260 lists the status of the power modes for the power domain.

Table 3-260. PD_L3INIT Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain – Last Power State Entered Status		PM_L3INIT_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area – State Status	L3INIT_BANK1	PM_L3INIT_PWRSTST[5:4] L3INIT_BANK1_STATEST
Memory Area – State Status	L3INIT_BANK2	PM_L3INIT_PWRSTST[7:6] L3INIT_BANK2_STATEST
Power Domain – State Transition Status		PM_L3INIT_PWRSTST[20] INTRANSITION
Logic Area – State Status		PM_L3INIT_PWRSTST[2] LOGICSTATEST
Power Domain – State Status		PM_L3INIT_PWRSTST[1:0] POWERSTATEST

3.7.6 PD_IVA Description

PD_IVA contains the following reset domains:

- IVA_PWRON_RST
- IVA_RST
- IVA_SEQ1_RST

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- IVA_SEQ2_RST

PD_IVA contains the CD_IVA clock domain.

Table 3-261 lists the logic retention capability for each module of the power domain.

Table 3-261. PD_IVA Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
IVA	No	RM_IVA_IVA_CONTEXT[0] LOSTCONTEXT_DFF	None
SL2	No	RM_IVA_SL2_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.6.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.6.1.1 Logic and Memory Area Power Modes

Table 3-262 lists the power modes supported by the logic area of the power domain.

Table 3-262. PD_IVA Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
Not available	Available	Available

Table 3-263 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On and Logic Retention columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

Table 3-263. PD_IVA Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
HWA_MEM		ON	
	IVA – HWA_MEM	always_on	always_off
SL2_MEM		ON	RETENTION
	SL2 – SL2MEM	always_on	software_control
TCM_1_MEM		ON	RETENTION
	IVA – TCM_1	always_on	software_control
TCM_2_MEM		ON	RETENTION
	IVA – TCM_2	always_on	software_control

3.7.6.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-264 lists the power mode controls for the power domain.

Table 3-264. PD_IVA Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area – State Control (logic in RETENTION state)	SL2_MEM	PM_IVA_PWRSTCTRL[9] SL2_MEM_RETSTATE	Read/write
Memory Area – State Control (logic in RETENTION state)	HWA_MEM	PM_IVA_PWRSTCTRL[8] HWA_MEM_RETSTATE	Read only

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Table 3-264. PD_IVA Power Modes Control Parameters (continued)

Parameter Name	Memory Bank	Control Bit Field	Access Type
Power Domain – Low-Power State Change Control		PM_IVA_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/write
Memory Area – State Control (logic in ON state)	TCM_2_MEM	PM_IVA_PWRSTCTRL[23:22] TCM2_MEM_ONSTATE	Read only
Memory Area – State Control (logic in ON state)	TCM_1_MEM	PM_IVA_PWRSTCTRL[21:20] TCM1_MEM_ONSTATE	Read only
Logic Area – Retention State Control		PM_IVA_PWRSTCTRL[2] LOGICRETSTATE	Read only
Memory Area – State Control (logic in ON state)	SL2_MEM	PM_IVA_PWRSTCTRL[19:18] SL2_MEM_ONSTATE	Read only
Memory Area – State Control (logic in ON state)	HWA_MEM	PM_IVA_PWRSTCTRL[17:16] HWA_MEM_ONSTATE	Read only
Memory Area – State Control (logic in RETENTION state)	TCM_2_MEM	PM_IVA_PWRSTCTRL[11] TCM2_MEM_RETSTATE	Read/write
Memory Area – State Control (logic in RETENTION state)	TCM_1_MEM	PM_IVA_PWRSTCTRL[10] TCM1_MEM_RETSTATE	Read/write
Power Domain – State Transition Control		PM_IVA_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 3-265 lists the status of the power modes for the power domain.

Table 3-265. PD_IVA Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain – Last Power State Entered Status		PM_IVA_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area – State Status	TCM_1_MEM	PM_IVA_PWRSTST[9:8] TCM1_MEM_STATEST
Memory Area – State Status	SL2_MEM	PM_IVA_PWRSTST[7:6] SL2_MEM_STATEST
Memory Area – State Status	HWA_MEM	PM_IVA_PWRSTST[5:4] HWA_MEM_STATEST
Power Domain – State Transition Status		PM_IVA_PWRSTST[20] INTRANSITION
Logic Area – State Status		PM_IVA_PWRSTST[2] LOGICSTATEST
Memory Area – State Status	TCM_2_MEM	PM_IVA_PWRSTST[11:10] TCM2_MEM_STATEST
Power Domain – State Status		PM_IVA_PWRSTST[1:0] POWERSTATEST

3.7.7 PD_GPU Description

The GPU_RST reset domain and the CD_GPU clock domain belong to PD_GPU.

Table 3-266 lists the logic retention capability for each module of the power domain.

Table 3-266. PD_GPU Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
GPU	No	RM_GPU_GPU_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.7.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

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3.7.7.1.1 Logic and Memory Area Power Modes

Table 3-267 lists the power modes supported by the logic area of the power domain.

Table 3-267. PD_GPU Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
Not available	Available	Available

Table 3-268 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On and Logic Retention columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

Table 3-268. PD_GPU Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
GPU_MEM		ON	
	GPU – GPU_MEM	always_on	always_off

3.7.7.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-269 lists the power mode controls for the power domain.

Table 3-269. PD_GPU Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Power Domain – Low-Power State Change Control		PM_GPU_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/write
Memory Area – State Control (logic in ON state)	GPU_MEM	PM_GPU_PWRSTCTRL[17:16] GPU_MEM_ONSTATE	Read only
Power Domain – State Transition Control		PM_GPU_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 3-270 lists the status of the power modes for the power domain.

Table 3-270. PD_GPU Power Mode Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Memory Area – State Status	GPU_MEM	PM_GPU_PWRSTST[5:4] GPU_MEM_STATEST
Power Domain – Last Power State Entered Status		PM_GPU_PWRSTST[25:24] LASTPOWERSTATEENTERED
Power Domain – State Transition Status		PM_GPU_PWRSTST[20] INTRANSITION
Logic Area – State Status		PM_GPU_PWRSTST[2] LOGICSTATEST
Power Domain – State Status		PM_GPU_PWRSTST[1:0] POWERSTATEST

3.7.8 PD_EMU Description

PD_EMU contains the following reset domains:

- EMU_EARLY_PWRON_RST
- EMU_PWRON_RST
- EMU_RST

PD_EMU contains the CD_EMU clock domain.

Table 3-271 lists the logic retention capability for each module of the power domain.

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Table 3-271. PD_EMU Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DEBUGSS logic	No	RM_EMU_DEBUGSS_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.8.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.8.1.1 Logic and Memory Area Power Modes

Table 3-272 lists the power modes supported by the logic area of the power domain.

Table 3-272. PD_EMU Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
Not available	Not available	Available

Table 3-273 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

Table 3-273. PD_EMU Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
EMU_BANK		ON	
	DEBUGSS – DebugSS_MEM	always_on	always_off

3.7.8.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-274 lists the power modes controls for the power domain.

Table 3-274. PD_EMU Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area - State Control (logic in ON state)	EMU_BANK	PM_EMU_PWRSTCTRL[17:16] EMU_BANK_ONSTATE	Read only
Power Domain - State Transition Control		PM_EMU_PWRSTCTRL[1:0] POWERSTATE	Read only

NOTE: To minimize leakage of DEBUGSS internal PLL when PD_EMU is switched off, AIPOFF_WKUP is driven high by PRCM. When PD_EMU is switched on, PRCM drives AIPOFF_WKUP to low before PD_EMU reaches ON state.

Table 3-275 lists the status of the power modes for the power domain.

Table 3-275. PD_EMU Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Memory Area – State Status	EMU_BANK	PM_EMU_PWRSTST[5:4] EMU_BANK_STATEST
Power Domain – Last Power State Entered Status		PM_EMU_PWRSTST[25:24] LASTPOWERSTATEENTERED

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Table 3-275. PD_EMU Power Modes Status Parameters (continued)

Parameter Name	Memory Bank	Status Bit Field
Power Domain – State Transition Status		PM_EMU_PWRSTST[20] INTRANSITION
Logic Area – State Status		PM_EMU_PWRSTST[2] LOGICSTATEST
Power Domain – State Status		PM_EMU_PWRSTST[1:0] POWERSTATEST

3.7.9 PD_DSS Description

PD_DSS contains the following reset domains:

- DSS_RET_RST
- DSS_RST

PD_DSS contains the CD_DSS clock domain.

Table 3-276 lists the logic retention capability for each module of the power domain.

Table 3-276. PD_DSS Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DSS	Partial	RM_DSS_DSS_CONTEXT[0] LOSTCONTEXT_DFF	RM_DSS_DSS_CONTEXT[1] LOSTCONTEXT_RFF
BB2D	None	RM_DSS_BB2D_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.9.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.9.1.1 Logic and Memory Area Power Modes

Table 3-277 lists the power modes supported by the logic area of the power domain.

Table 3-277. PD_DSS Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
N/A	Available	Available

Table 3-278 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On and Logic Retention columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

Table 3-278. PD_DSS Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
DSS_MEM		ON	
	DSS – DSSMEM	always_on	always_off
	BB2D - BB2D_MEM	always_on	always_off

3.7.9.1.2 Logic and Memory Area Power Mode Control and Status

Table 3-279 lists the power modes controls for the power domain.

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Table 3-279. PD_DSS Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area – State Control (logic in RETENTION state)	DSS_MEM	PM_DSS_PWRSTCTRL[8] DSS_MEM_RETSTATE	Read only
Power Domain – Low-Power State Change Control		PM_DSS_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/write
Logic Area – RETENTION State Control		PM_DSS_PWRSTCTRL[2] LOGICRETSTATE	Read only
Memory Area – State Control (logic in ON state)	DSS_MEM	PM_DSS_PWRSTCTRL[17:16] DSS_MEM_ONSTATE	Read only
Power Domain – State Transition Control		PM_DSS_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 3-280 lists the status of the power modes for the power domain.

Table 3-280. PD_DSS Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Memory Area – State Status	DSS_MEM	PM_DSS_PWRSTST[5:4] DSS_MEM_STATEST
Power Domain – Last Low Power State Entered Status		PM_DSS_PWRSTST[25:24] LASTPOWERSTATEENTERED
Power Domain – State Transition Status		PM_DSS_PWRSTST[20] INTRANSITION
Logic Area – State Status		PM_DSS_PWRSTST[2] LOGICSTATEST
Power Domain – Current Power State Status		PM_DSS_PWRSTST[1:0] POWERSTATEST

3.7.10 PD_CORE Description

PD_CORE contains the following reset domains:

- CM_CORE_PWRON_RET_RST
- CM_CORE_RET_RST
- CORE_PWRON_RET_RST
- CORE_PWRON_RST
- CORE_RET_RST
- CORE_RST
- DLL_RST
- IPU_PWRON_RST
- IPU_RET_RST
- IPU_CPU0_RST
- IPU_CPU1_RST
- IPU_RST
- EMIF_DDR_PHY_PWRON_RST
- DMA_RET_RST

PD_CORE contains the following clock domains:

- CD_DMA
- CD_IPU
- CD_EMIF
- CD_L3_MAIN1
- CD_L3_MAIN2
- CD_L3_INSTR

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- CD_L4_CFG
- CD_L4_PER
- CD_L4_SEC

Table 3-281 lists the logic retention capability for each module of the power domain.

Table 3-281. PD_CORE Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
CONTROL_MODULE_CORE	Full	None	None
CONTROL_MODULE_BANDGAP	No	None	None
CM_CORE	Full	None	None
DDRPHY	No	None	None
DLL	No	RM_EMIF_EMIF_DLL_CONTEXT[0] LOSTCONTEXT_DFF	None
DLL_AGING	No	None	None
DMM	Partial	RM_EMIF_DMM_CONTEXT[0] LOSTCONTEXT_DFF	RM_EMIF_DMM_CONTEXT[1] LOSTCONTEXT_RFF
IPU	Partial	RM_IPU_IPU_CONTEXT[0] LOSTCONTEXT_DFF	RM_IPU_IPU_CONTEXT[1] LOSTCONTEXT_RFF
EMIF1	Partial	RM_EMIF_EMIF1_CONTEXT[0] LOSTCONTEXT_DFF	RM_EMIF_EMIF1_CONTEXT[1] LOSTCONTEXT_RFF
EMIF2	Partial	RM_EMIF_EMIF2_CONTEXT[0] LOSTCONTEXT_DFF	RM_EMIF_EMIF2_CONTEXT[1] LOSTCONTEXT_RFF
EMIF_OCP_FW	Partial	RM_EMIF_EMIF_OCP_FW_CONTEXT[0] LOSTCONTEXT_DFF	RM_EMIF_EMIF_OCP_FW_CONTEXT[1] LOSTCONTEXT_RFF
GPMC	Full	None	RM_L3MAIN2_GPMC_CONTEXT[1] LOSTCONTEXT_RFF
SPINLOCK	Full	None	RM_L4CFG_SPINLOCK_CONTEXT[1] LOSTCONTEXT_RFF
L3_MAIN_2 interconnect	Partial	RM_L3MAIN2_L3_MAIN_2_CONTEXT[0] LOSTCONTEXT_DFF	RM_L3MAIN2_L3_MAIN_2_CONTEXT[1] LOSTCONTEXT_RFF
L3_MAIN_3 interconnect	Partial	RM_L3INSTR_L3_MAIN_3_CONTEXT[0] LOSTCONTEXT_DFF	RM_L3INSTR_L3_MAIN_3_CONTEXT[1] LOSTCONTEXT_RFF
L3_MAIN_1 interconnect	Partial	RM_L3MAIN1_L3_MAIN_1_CONTEXT[0] LOSTCONTEXT_DFF	RM_L3MAIN1_L3_MAIN_1_CONTEXT[1] LOSTCONTEXT_RFF
L3_INSTR interconnect	No	RM_L3INSTR_L3_INSTR_CONTEXT[0] LOSTCONTEXT_DFF	None
L4_CFG interconnect	Partial	RM_L4CFG_L4_CFG_CONTEXT[0] LOSTCONTEXT_DFF	RM_L4CFG_L4_CFG_CONTEXT[1] LOSTCONTEXT_RFF
MAILBOX	Full	None	RM_L4CFG_MAILBOX_CONTEXT[1] LOSTCONTEXT_RFF
OCMC_RAM	No	RM_L3MAIN2_OCMC_RAM_CONTEXT[0] LOSTCONTEXT_DFF	None
SAR_ROM	No	RM_L4CFG_SAR_ROM_CONTEXT[0] LOSTCONTEXT_DFF	None
DMA_SYSTEM	Full	None	RM_DMA_DMA_SYSTEM_CONTEXT[1] LOSTCONTEXT_RFF
OCP_WP_NOC	Partial	RM_L3INSTR_OCP_WP_NOC_CONTEXT[0] LOSTCONTEXT_DFF	RM_L3INSTR_OCP_WP_NOC_CONTEXT[1] LOSTCONTEXT_RFF
AES1	Full	None	RM_L4SEC_AES1_CONTEXT[1] LOSTCONTEXT_RFF
AES2	Full	None	RM_L4SEC_AES2_CONTEXT[1] LOSTCONTEXT_RFF
DES3DES	Full	None	RM_L4SEC_DES3DES_CONTEXT[1] LOSTCONTEXT_RFF

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Table 3-281. PD_CORE Modules Power Attributes (continued)

Module	Logic Retention	DFF Context Status	RFF Context Status
DMA_CRYPTO	Full	None	RM_DMA_CRYPTO_CONTEXT [1] LOSTCONTEXT_RFF
ELM	No	RM_L4PER_ELM_CONTEXT[0] LOSTCONTEXT_DFF	None
FPKA	No	RM_L4SEC_FPKA_CONTEXT[0] LOSTCONTEXT_DFF	None
RNG	Full	None	RM_L4SEC_RNG_CONTEXT[1] LOSTCONTEXT_RFF
SHA2MD5	Full	None	RM_L4SEC_SHA2MD5_CONTEXT[1] LOSTCONTEXT_RFF
GPIO2	Full	None	RM_L4PER_GPIO2_CONTEXT[1] LOSTCONTEXT_RFF
GPIO3	Full	None	RM_L4PER_GPIO3_CONTEXT[1] LOSTCONTEXT_RFF
GPIO4	Full	None	RM_L4PER_GPIO4_CONTEXT[1] LOSTCONTEXT_RFF
GPIO5	Full	None	RM_L4PER_GPIO5_CONTEXT[1] LOSTCONTEXT_RFF
GPIO6	Full	None	RM_L4PER_GPIO6_CONTEXT[1] LOSTCONTEXT_RFF
GPIO7	Full	None	RM_L4PER_GPIO7_CONTEXT[1] LOSTCONTEXT_RFF
GPIO8	Full	None	RM_L4PER_GPIO8_CONTEXT[1] LOSTCONTEXT_RFF
HDQW1	No	RM_L4PER_HDQ1W_CONTEXT[0] LOSTCONTEXT_DFF	None
I2C1	Full	None	RM_L4PER_I2C1_CONTEXT[1] LOSTCONTEXT_RFF
I2C2	No	RM_L4PER_I2C2_CONTEXT[0] LOSTCONTEXT_DFF	None
I2C3	No	RM_L4PER_I2C3_CONTEXT[0] LOSTCONTEXT_DFF	None
I2C4	No	RM_L4PER_I2C4_CONTEXT[0] LOSTCONTEXT_DFF	None
I2C5	No	RM_L4PER_I2C5_CONTEXT[0] LOSTCONTEXT_DFF	None
L4_PER interconnect	Partial	RM_L4PER_L4_PER_CONTEXT[0] LOSTCONTEXT_DFF	RM_L4PER_L4_PER_CONTEXT[1] LOSTCONTEXT_RFF
MCSPI1	No	RM_L4PER_MCSPI1_CONTEXT[0] LOSTCONTEXT_DFF	None
MCSPI2	No	RM_L4PER_MCSPI2_CONTEXT[0] LOSTCONTEXT_DFF	None
MCSPI3	No	RM_L4PER_MCSPI3_CONTEXT[0] LOSTCONTEXT_DFF	None
MCSPI4	No	RM_L4PER_MCSPI4_CONTEXT[0] LOSTCONTEXT_DFF	None
MMC3	No	RM_L4PER_MMC3_CONTEXT[0] LOSTCONTEXT_DFF	None
MMC4	No	RM_L4PER_MMC4_CONTEXT[0] LOSTCONTEXT_DFF	None
MMC5	No	RM_L4PER_MMC5_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER10	No	RM_L4PER_TIMER10_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER11	No	RM_L4PER_TIMER11_CONTEXT[0] LOSTCONTEXT_DFF	None

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Table 3-281. PD_CORE Modules Power Attributes (continued)

Module	Logic Retention	DFF Context Status	RFF Context Status
TIMER2	No	RM_L4PER_TIMER2_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER3	No	RM_L4PER_TIMER3_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER4	No	RM_L4PER_TIMER4_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER9	No	RM_L4PER_TIMER9_CONTEXT[0] LOSTCONTEXT_DFF	None
UART1	Full	None	RM_L4PER_UART1_CONTEXT [1] LOSTCONTEXT_RFF
UART2	Full	None	RM_L4PER_UART2_CONTEXT [1] LOSTCONTEXT_RFF
UART3	Full	None	RM_L4PER_UART3_CONTEXT [1] LOSTCONTEXT_RFF
UART4	Full	None	RM_L4PER_UART4_CONTEXT [1] LOSTCONTEXT_RFF
UART5	Full	None	RM_L4PER_UART5_CONTEXT [1] LOSTCONTEXT_RFF
UART6	Full	None	RM_L4PER_UART6_CONTEXT [1] LOSTCONTEXT_RFF

3.7.10.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.10.1.1 Logic and Memory Area Power Modes

Table 3-282 lists the power modes supported by the logic area of the power domain.

Table 3-282. PD_CORE Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
Available	Available	Available

Table 3-283 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On and Logic Retention columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

Table 3-283. PD_CORE Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
CORE_NRET_BANK		ON	
	DMM – DMM_MEMBANK2	always_on	always_off
	OCP_WP_NOC – OCPWP_BANK	always_on	always_off
	MMC3 - MMC_RAM	always_on	always_off
	MMC4 - MMC_RAM	always_on	always_off
	MMC5 - MMC_RAM	always_on	always_off
	FPKA - pka_mem	always_on	always_off
CORE_OCMRAM		ON	RETENTION

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Table 3-283. PD_CORE Memory Area Power Modes (continued)

Memory Bank	Module – Memory	Logic On	Logic Retention
	OCMC_RAM – OCMC_RAM_Bank1	always_on	always_retention
CORE_OTHER_BANK		ON	RETENTION
	DMA_SYSTEM – DMA_MEM	always_on	always_retention
	DMM – DMM_MEMBANK1	always_on	always_retention
	DMA_CRYPTO - DMA_CRYPTO_MEM	always_on	always_retention
	UART1 - UART_MEM	always_on	always_retention
	UART2 - UART_MEM	always_on	always_retention
	UART3 - UART_MEM	always_on	always_retention
	UART4 - UART_MEM	always_on	always_retention
	UART5 - UART_MEM	always_on	always_retention
	UART6 - UART_MEM	always_on	always_retention
IPU_L2RAM		ON	RETENTION
	IPU – IPU_L2RAM_MEM	always_on	software_control
IPU_UNICACHE		ON	RETENTION
	IPU – IPU_UNICACHE_mem	always_on	software_control

3.7.10.1.2 Logic and Memory Area Power Mode Control and Status

Table 3-284 lists the power mode controls for the power domain.

Table 3-284. PD_CORE Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area – State Control (Logic in RETENTION state)	CORE_OCMRAM	PM_CORE_PWRSTCTRL[9] CORE_OCMRAM_RETSTATE	Read only
Memory Area – State Control (Logic in RETENTION state)	CORE_OTHER_BANK	PM_CORE_PWRSTCTRL[8] CORE_OTHER_BANK_RETSTATE	Read only
Memory Area – State Control (Logic in ON state)	CORE_NRET_BANK	PM_CORE_PWRSTCTRL[25:24] OCP_NRET_BANK_ONSTATE	Read only
Memory Area – State Control (Logic in ON state)	IPU_UNICACHE	PM_CORE_PWRSTCTRL[23:22] IPU_UNICACHE_ONSTATE	Read only
Memory Area – State Control (Logic in ON state)	IPU_L2RAM	PM_CORE_PWRSTCTRL[21:20] IPU_L2RAM_ONSTATE	Read only
Memory Area – State Control (Logic in ON state)	CORE_OCMRAM	PM_CORE_PWRSTCTRL[19:18] CORE_OCMRAM_ONSTATE	Read only
Memory Area – State Control (Logic in ON state)	CORE_OTHER_BANK	PM_CORE_PWRSTCTRL[17:16] CORE_OTHER_BANK_ONSTATE	Read only
Memory Area – State Control (Logic in RETENTION state)	CORE_NRET_BANK	PM_CORE_PWRSTCTRL[12] OCP_NRET_BANK_RETSTATE	Read only
Memory Area – State Control (Logic in RETENTION state)	IPU_UNICACHE	PM_CORE_PWRSTCTRL[11] IPU_UNICACHE_RETSTATE	Read/write
Memory Area – State Control (Logic in RETENTION state)	IPU_L2RAM	PM_CORE_PWRSTCTRL[10] IPU_L2RAM_RETSTATE	Read/write
Logic Area – RETENTION State Control	N/A	PM_CORE_PWRSTCTRL[2] LOGICRETSTATE	Read/write
Power Domain – Low-Power State Change Control	N/A	PM_CORE_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/write
Power Domain – State Transition Control	N/A	PM_CORE_PWRSTCTRL[1:0] POWERSTATE	Read/write

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Table 3-285 lists the status of the power modes for the power domain.

Table 3-285. PD_CORE Power Mode Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain – Last Power State Entered Status		PM_CORE_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area – State Status	IPU_L2RAM	PM_CORE_PWRSTST[9:8] IPU_L2RAM_STATEST
Memory Area – State Status	CORE_OCMRAM	PM_CORE_PWRSTST[7:6] CORE_OCMRAM_STATEST
Memory Area – State Status	CORE_OTHER_BANK	PM_CORE_PWRSTST[5:4] CORE_OTHER_BANK_STATEST
Memory Area – State Status	CORE_NRET_BANK	PM_CORE_PWRSTST[13:12] OCP_NRET_BANK_STATEST
Memory Area – State Status	IPU_UNICACHE	PM_CORE_PWRSTST[11:10] IPU_UNICACHE_STATEST
Logic Area – State Status		PM_CORE_PWRSTST[2] LOGICSTATEST
Power Domain – State Transition Status		PM_CORE_PWRSTST[20] INTRANSITION
Power Domain – State Status		PM_CORE_PWRSTST[1:0] POWERSTATEST

3.7.11 PD_CAM Description

PD_CAM contains the CAM_RST reset domain.

PD_CAM contains the CD_CAM clock domain.

Table 3-286 lists the logic retention capability for each module of the power domain.

Table 3-286. PD_CAM Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
FDIF	No	RM_CAM_FDIF_CONTEXT[0] LOSTCONTEXT_DFF	None
ISS	No	RM_CAM_ISS_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.11.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.11.1.1 Logic and Memory Area Power Modes

Table 3-287 lists the power modes supported by the logic area of the power domain.

Table 3-287. PD_CAM Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
Not available	Available	Available

Table 3-288 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On and Logic Retention columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

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Table 3-288. PD_CAM Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
CAM_MEM		ON	
	FDIF – FDIFMEM	always_on	always_off
	ISS – ISSMEM	always_on	always_off

3.7.11.1.2 Logic and Memory Area Power Mode Control and Status

Table 3-289 lists the power mode controls for the power domain.

Table 3-289. PD_CAM Power Mode Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Power Domain – Low-Power State Change Control		PM_CAM_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/write
Memory Area – State Control (Logic in ON state)	CAM_MEM	PM_CAM_PWRSTCTRL[17:16] CAM_MEM_ONSTATE	Read only
Power Domain – State Transition Control		PM_CAM_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 3-290 lists the status of the power modes for the power domain.

Table 3-290. PD_CAM Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Memory Area – State Status	CAM_MEM	PM_CAM_PWRSTST[5:4] CAM_MEM_STATEST
Power Domain – Last Power State Entered Status		PM_CAM_PWRSTST[25:24] LASTPOWERSTATEENTERED
Power Domain – State Transition Status		PM_CAM_PWRSTST[20] INTRANSITION
Logic Area – State Status		PM_CAM_PWRSTST[2] LOGICSTATEST
Power Domain – State Status		PM_CAM_PWRSTST[1:0] POWERSTATEST

3.7.12 PD_ABE Description

PD_ABE contains the following reset domains:

- ABE_PWRON_RST
- ABE_RST

PD_ABE contains the CD_ABE clock domain.

Table 3-291 lists the logic retention capability for each module of the power domain.

Table 3-291. PD_ABE Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
AESS	No	RM_ABE_AESS_CONTEXT[0] LOSTCONTEXT_DFF	None
CKGEN_ABE	No	None	None
DMIC	No	RM_ABE_DMIC_CONTEXT[0] LOSTCONTEXT_DFF	None
L4_ABE interconnect	No	None	None
MCASP	No	RM_ABE_MCASP_CONTEXT[0] LOSTCONTEXT_DFF	None
MCBSP1	No	RM_ABE_MCBSP1_CONTEXT[0] LOSTCONTEXT_DFF	None

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Table 3-291. PD_ABE Modules Power Attributes (continued)

Module	Logic Retention	DFF Context Status	RFF Context Status
MCBSP2	No	RM_ABE_MCBSP2_CONTEXT[0] LOSTCONTEXT_DFF	None
MCBSP3	No	RM_ABE_MCBSP3_CONTEXT[0] LOSTCONTEXT_DFF	None
MCPDM	No	RM_ABE_MCPDM_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER5	No	RM_ABE_TIMER5_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER6	No	RM_ABE_TIMER6_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER7	No	RM_ABE_TIMER7_CONTEXT[0] LOSTCONTEXT_DFF	None
TIMER8	No	RM_ABE_TIMER8_CONTEXT[0] LOSTCONTEXT_DFF	None
WD_TIMER3	No	RM_ABE_WD_TIMER3_CONTEXT[0] LOSTCONTEXT_DFF	None

3.7.12.1 Power Domain Modes

This section describes the various power modes supported by the logic and memory areas of the power domain. It also identifies the associated software control and status bit fields. For a functional description of the power-management architecture of a generic power domain, see Section 3.1.1.2.1, *Power Domain*.

3.7.12.1.1 Logic and Memory Area Power Modes

Table 3-292 lists the power modes supported by the logic area of the power domain.

Table 3-292. PD_ABE Logic Area Power Modes

Retention-CSWR	On-Inactive	On-Active
Not available	Available	Available

Table 3-293 lists the power modes supported by the memory area of the power domain. A memory area power mode is identified with respect to a power state of the power domain. The Logic On, Logic Retention columns identify the power states of the power domain. The values in these columns identify the supported power state of the memory area (identified in the Memory Bank column) or the module memory inside the memory area (identified in the Module – Memory column).

Table 3-293. PD_ABE Memory Area Power Modes

Memory Bank	Module – Memory	Logic On	Logic Retention
AESSMEM		ON	RETENTION
	AESS – AESS_MemBank1	always_on	always_retention
PERIPHMEM		ON	
	DMIC – DMIC_BANK	always_on	always_off
	MCBSP1 – MCBSP_BANK	always_on	always_off
	MCBSP2 – MCBSP_BANK	always_on	always_off
	MCBSP3 – MCBSP_BANK	always_on	always_off
	MCPDM – MCPDM_BANK	always_on	always_off

3.7.12.1.2 Logic and Memory Area Power Modes Control and Status

Table 3-294 lists the power modes controls for the power domain.

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Table 3-294. PD_ABE Power Modes Control Parameters

Parameter Name	Memory Bank	Control Bit Field	Access Type
Memory Area – State Control (logic in RETENTION state)	AESSMEM	PM_ABE_PWRSTCTRL[8] AESSMEM_RETSTATE	Read only
Memory Area – State Control (logic in ON state)	PERIPHMEM	PM_ABE_PWRSTCTRL[21:20] PERIPHMEM_ONSTATE	Read only
Memory Area – State Control (logic in ON state)	AESSMEM	PM_ABE_PWRSTCTRL[17:16] AESSMEM_ONSTATE	Read only
Memory Area – State Control (logic in RETENTION state)	PERIPHMEM	PM_ABE_PWRSTCTRL[10] PERIPHMEM_RETSTATE	Read only
Logic Area – RETENTION State Control		PM_ABE_PWRSTCTRL[2] LOGICRETSTATE	Read only
Power Domain – Low-Power State Change Control		PM_ABE_PWRSTCTRL[4] LOWPOWERSTATECHANGE	Read/write
Power Domain – State Transition Control		PM_ABE_PWRSTCTRL[1:0] POWERSTATE	Read/write

Table 3-295 lists the status of the power modes for the power domain.

Table 3-295. PD_ABE Power Modes Status Parameters

Parameter Name	Memory Bank	Status Bit Field
Power Domain – Last Power State Entered Status		PM_ABE_PWRSTST[25:24] LASTPOWERSTATEENTERED
Memory Area – State Status	PERIPHMEM	PM_ABE_PWRSTST[9:8] PERIPHMEM_STATEST
Memory Area – State Status	AESSMEM	PM_ABE_PWRSTST[5:4] AESSMEM_STATEST
Power Domain – State Transition Status		PM_ABE_PWRSTST[20] INTRANSITION
Logic Area – State Status		PM_ABE_PWRSTST[2] LOGICSTATEST
Power Domain – State Status		PM_ABE_PWRSTST[1:0] POWERSTATEST

3.7.13 PD_MPUAON Description

PD_MPUAON contains the following reset domains:

- MPUAON_RST
- DPLL_MPU_PWRON_RST

PD_MPUAON has no associated clock domains.

Table 3-296 lists the logic retention capability for each module of the power domain.

Table 3-296. PD_MPUAON Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DPLL_MPU	No	None	None
INTC_MPU	No	None	None

3.7.13.1 Power Domain Modes

The PD_MPUAON power domain is an always-on power domain and does not switch to RETENTION state. There is no logic power-state control or status bit field for this power domain.

The PD_MPUAON power domain has no memory banks.

3.7.14 PD_MMAON Description

PD_MMAON contains the following reset domains:

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- MMAON_RST
- DPLL_IVA_PWRON_RST

PD_MMAON has no associated clock domains.

Table 3-297 lists the logic retention capability for each module of the power domain.

Table 3-297. PD_MMAON Module Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DPLL_IVA	No	None	None
WUGEN_DSP	No	None	None

3.7.14.1 Power Domain Modes

The PD_MMAON power domain is an always-on power domain and does not switch to RETENTION state. There is no logic power-state control or status bit field for this power domain.

The PD_MMAON power domain has no memory banks.

3.7.15 PD_COREAON Description

PD_COREAON contains the following reset domains:

- CM_CORE_AON_PWRON_RST
- CM_CORE_AON_RST
- COREAON_PWRON_RST
- COREAON_RST

PD_COREAON contains the CD_COREAON_L4 clock domain.

Table 3-298 lists the logic retention capability for each module of the power domain.

Table 3-298. PD_COREAON Module Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
CM_CORE_AON	No	None	None
DPLL_ABE	No	None	None
DPLL_CORE	No	None	None
DPLL_PER	No	None	None
IO_SRCOMP_CORE	No	None	None
WUGEN_IPU	No	None	None
WUGEN_DMA_SYSTEM	No	None	None
SMARTREFLEX_CORE	No	RM_COREAON_SMARTREFLEX_CORE_CONTEXT[0] LOSTCONTEXT_DFF	None
SMARTREFLEX_MM	No	RM_COREAON_SMARTREFLEX_MM_CONTEXT[0] LOSTCONTEXT_DFF	None
SMARTREFLEX_MPU	No	RM_COREAON_SMARTREFLEX_MPU_CONTEXT[0] LOSTCONTEXT_DFF	None
SPINNER	No	None	None
USB_PHY_CORE	No	None	None

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3.7.15.1 Power Domain Modes

The PD_COREAON power domain is an always-on power domain and does not switch to RETENTION state. There is no logic power-state control or status bit field for this power domain.

The PD_COREAON power domain has no memory banks.

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3.8 Voltage-Management Functional Description

This section describes the voltage domains and voltage control architecture. It also explains the interactions between the device and the external power IC.

3.8.1 Overview

The voltage-management architecture of the device is based on voltage sources managed by the PRCM module. They define the voltage domains within the device (see Section 3.1.1.3, *Voltage Management*). This partition of the voltage domains ensures independent voltage control of each voltage domain through dedicated SMPS or LDO. The following voltage domains are managed by the PRCM module:

- VDD_CORE_L
- VDD_MPU_L
- VDD_MM_L
- VDD_WKUP_L
- VDD_CORE_M
- VDD_MM_M
- VDD_MPU_M
- VDD_MM_ABB
- VDD_MPU_ABB

NOTE: For the association of the device power supply pin to the power domain, see Table 3-27.

The PRCM module supports the AVS technique on the VDD_MPU_L, VDD_CORE_L, and VDD_MM_L voltage domains through automatic monitoring and adjustments of voltages by their dedicated SmartReflex modules. The VDD_MPU_L voltage domain supports four DVFS OPPs. The VDD_MM_L and VDD_WKUP_L voltage domains support three DVFS OPPs. The VDD_CORE_L voltage domain supports two DVFS OPPs.

The PRCM module also supports the ABB technique on the MPU and MM voltage domains through the VDD_MPU_ABB and VDD_MM_ABB biasing voltages.

The PRCM module automatically scales down VDD_MPU_M, VDD_CORE_M, and VDD_MM_M to retention voltage level whenever all memory banks on these domains transition to the RETENTION power state.

Table 3-299 lists the supported DVFS OPPs for each voltage domain. The exact values depend on the silicon; for more information, see the Data Manual Operating Condition addendum.

Table 3-299. Supported DVFS OPPs Summary

Voltage Domain	Operating Point	Control
VDD_MPU_L (VD_MPU)	RETENTION OPP_LOW OPP_NOM OPP_HIGH OPP_SPEEDBIN	Hardware and software
VDD_MM_L (VD_MM)	RETENTION OPP_LOW OPP_NOM OPP_OD	Hardware and software
VDD_CORE_L (VD_CORE)	RETENTION OPP_NOM	Hardware and software
VDD_WKUP_L (VD_WKUP)	RETENTION OPP_WKUP_ACTIVE OPP_WKUP_EMULATION	Hardware and software

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Table 3-299. Supported DVFS OPPs Summary (continued)

Voltage Domain	Operating Point	Control
	OPP_WKUP_SLEEP	

At boot time, the device is set with all two voltage domains (VDD_MPU_L, VDD_MM_L) at OPP_LOW.

VDD_MPU_L (MPU voltage domain) voltage state status can be checked by reading bitfield PRM_VOLTST_MPU[1:0] VOLTSTATEST.

VDD_MM_L (MM voltage domain) voltage state status can be checked by reading bitfield PRM_VOLTST_MM[1:0] VOLTSTATEST.

DVFS OPPs dependencies:

For detailed information about DVFS OPPs dependencies, see the *Data Manual Operating Condition Addendum*.

Other OPPs limitations:

- When exiting from off (no power source) mode, voltage values for MPU, MM domains must be at OPP_LOW.

3.8.2 Voltage-Control Architecture

The PRM is split over several blocks that manage the different voltage sources.

- Voltage processors for converting SmartReflex data to voltage values before sending to the voltage controller
- Voltage FSMs for managing VDD_MPU_L, VDD_MM_L voltages (hardware control of voltages). They send commands to the voltage controller (I^2C mode).
- A voltage controller for gathering commands from the PRCM module register (direct access), voltage processors, and voltage FSMs. It then handles communication with the external power IC through the dedicated I^2C interface.
- A device FSM for managing the voltage FSMs and I/O wake-up control and system clock control sequencing during device sleep and wake-up transitions
- LDO regulator controllers for ABB management, memory array voltage management, and wake-up logic.
- BANDGAPs reference voltage sleep control

NOTE: The SmartReflex module allows dynamic voltage adjustments around an OPP voltage level to ensure target performance. It also allows switching from one OPP to another. However, it does not control voltage switching of the voltage domain to RETENTION level when all power domains within the power domain are in RETENTION power state. This is handled by the voltage FSMs.

Figure 3-77 shows the architecture for PRM voltage control.

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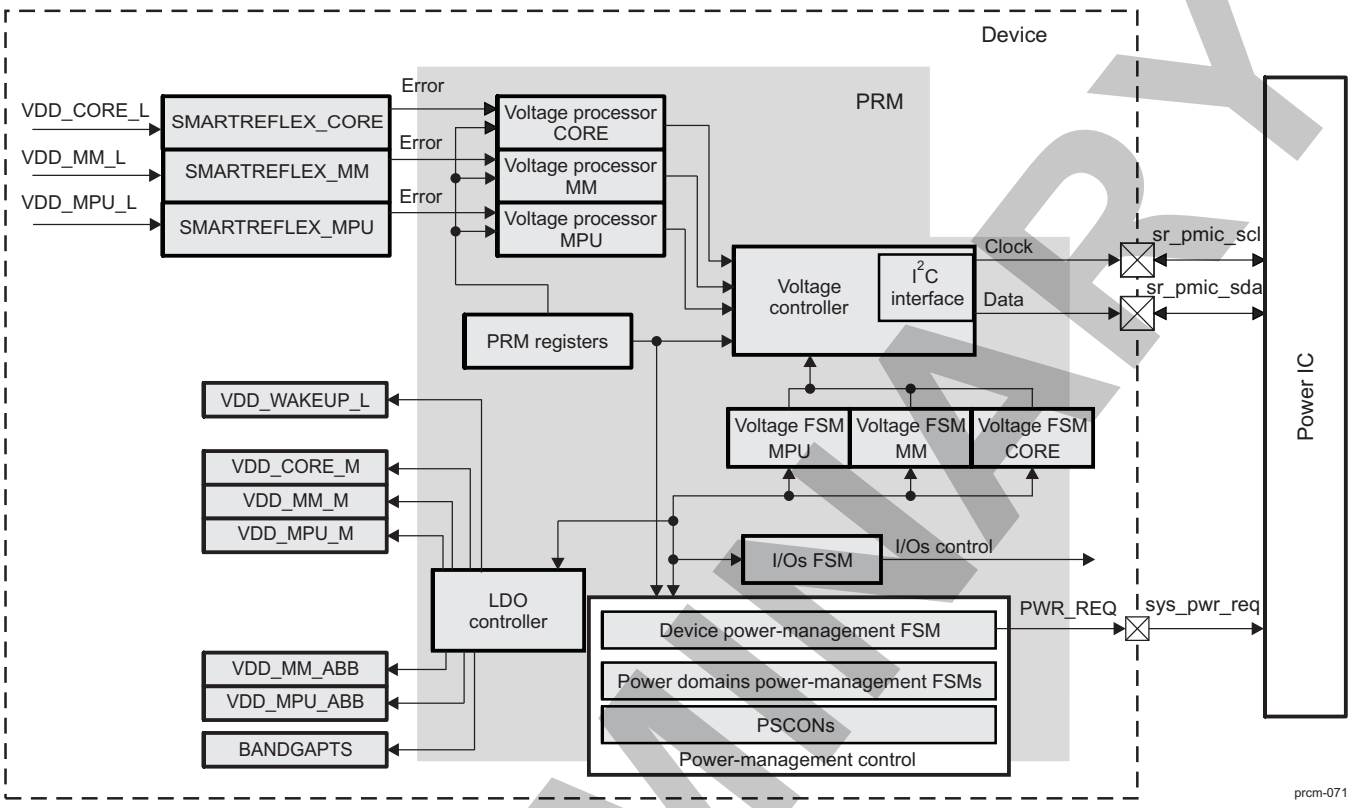
Figure 3-77. PRM Voltage Control Architecture



3.8.3 VDD_MPU_L, VDD_CORE_L, and VDD_MM_L Control

These power supply sources can be controlled using PRM dedicated I²C control.

3.8.3.1 PRM Dedicated I²C Control

The PRM I²C interface is dedicated to SmartReflex voltage control. It enables the voltage controller to send voltage commands to the external power IC. To reduce latency of voltage changes, the voltage controller is configurable to run in HS I²C mode. The PRM I²C interface supports multimaster mode.

The voltage controller receives voltage control commands from the following input ports:

- Voltage processors ports: Each voltage processor sends voltage change commands to the voltage controller depending on the information received from the associated SmartReflex module.
- Voltage PRCM ports: Each voltage PRCM sends commands to the voltage controller when the device enters RETENTION or off (no power supply) power state, and also when the device wakes up.
- PRM register port: The PRM registers give direct software control over the voltage levels of the external voltage sources.

An arbitration scheme in the voltage controller manages concurrent requests on different ports.

Each internal port has a handshake to indicate when the I²C frame that results from the request on that port is acknowledged by the external power IC.

The PRM can also send external voltage source sleep commands that can be used to activate power IC sleep mode, where the voltage regulator maintains output voltage but only a small load is supported. This also lets the external power IC reduce its power consumption.

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NOTE: An I^2C interface not controlled by the PRM can be used to program the voltage levels of the external power IC. Because the I^2C interface is not a hardware-controlled interface, its use is restricted to moving the voltage level from one OPP to another.

In this case, the control software must operate the voltage transition when device activity allows one.

3.8.3.2 Adaptive Voltage Scaling

As explained in Section 3.1.2.4, *Adaptive Voltage Scaling*, the SmartReflex technology uses adaptive power supply to reduce active power consumption. With SmartReflex, the power supply voltage can be adapted to the silicon performance statically (for example, adapted to the manufacturing process of a given device) or dynamically (for example, adapted to the temperature-induced current performance of the device).

SmartReflex voltage control in the device is based on the dedicated SmartReflex modules and the voltage processors, in addition to the voltage controller with a dedicated I^2C interface, which are shared with the voltage PRCM modules and voltage control registers.

The SmartReflex modules allow a continuous real-time monitoring of the voltage supply and device performance to:

- Minimize the supply voltage to reduce the device power consumption
- Maintain the desired device performance (by dynamically adjusting the device voltage) as the temperature of the device varies

Because the SmartReflex modules and the voltage processors are dedicated to SmartReflex voltage control, they are described together in this section.

3.8.3.2.1 SmartReflex in the Device

Figure 3-78 shows the SmartReflex integration.

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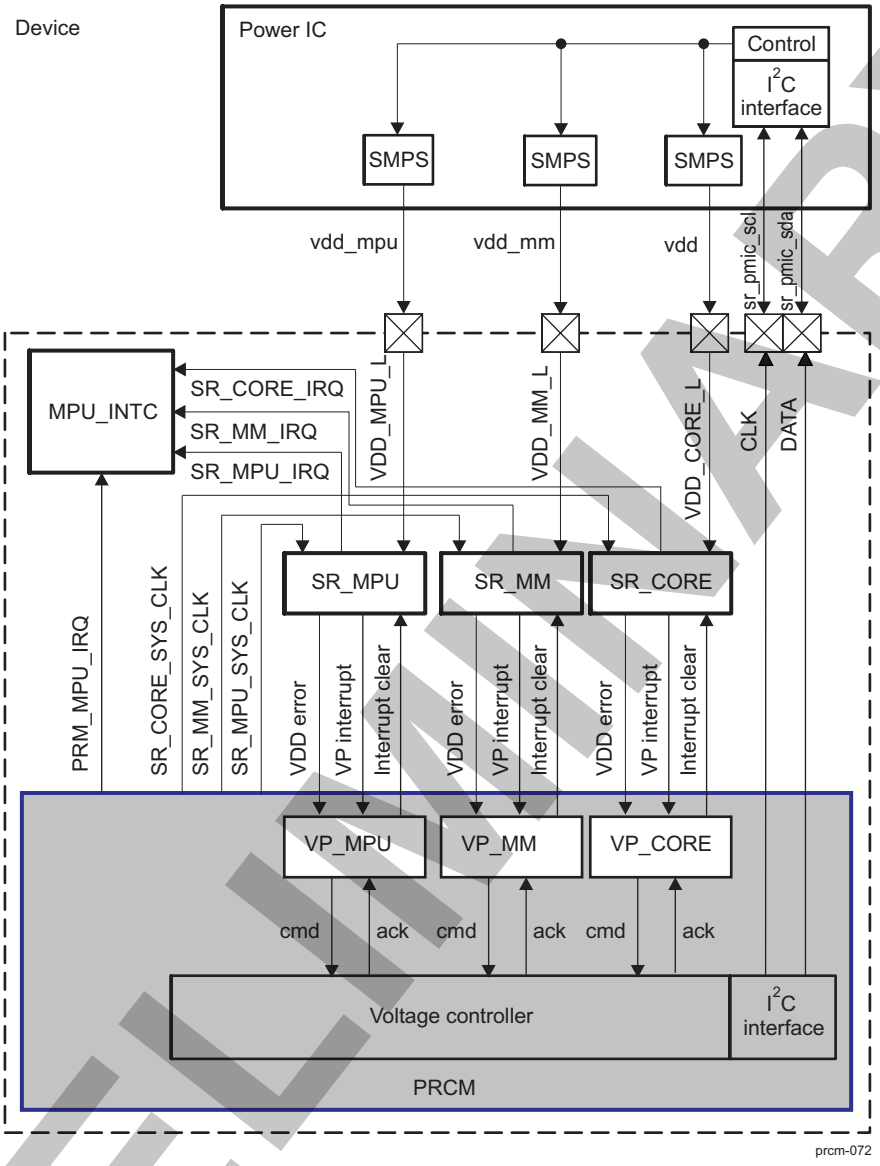
Figure 3-78. SmartReflex Integration



SmartReflex voltage control in the device is implemented for simultaneous control of three independent voltage sources. One SmartReflex module controls the VDD_CORE_L voltage, the second one is dedicated to VDD_MM_L control, and the third controls the VDD_MPU_L voltage. Each SmartReflex module is connected to a voltage processor. Voltage commands from all voltage processors are passed to a voltage control, which sends them through a dedicated I^2C master interface to the power IC.

SmartReflex modules are in the PD_COREAON power domain and supplied by the VDD_CORE_L voltage domain. Each module senses its own voltage domain (VDD_CORE_L, VDD_MM_L, or VDD_MPU_L).

3.8.3.2.2 SmartReflex Module

Figure 3-79 is a functional overview of the SmartReflex module.

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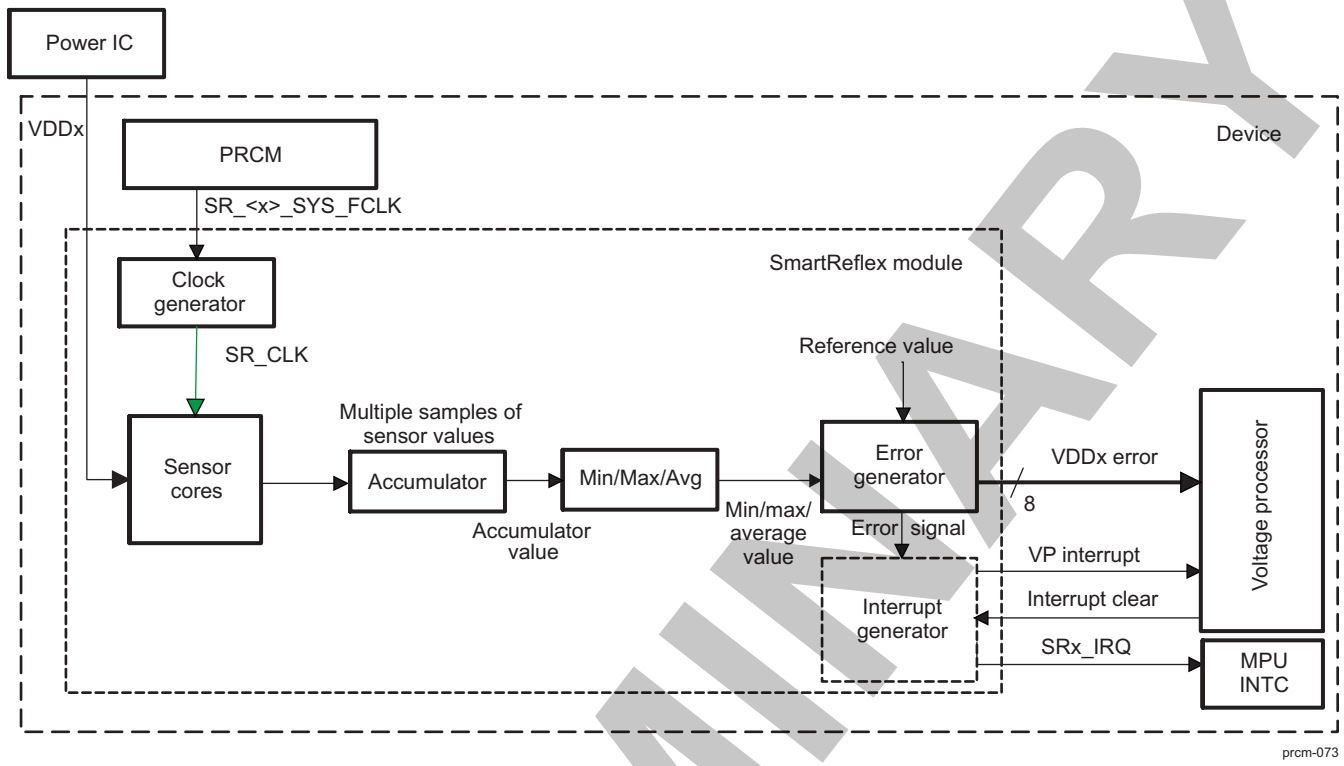
Figure 3-79. SmartReflex Module Functional Overview



3.8.3.2.3 SmartReflex Submodules

NOTE: In this and the following section, SMARTREFLEXn refers to the SMARTREFLEX_MM, SMARTREFLEX_MPU, and SMARTREFLEX_CORE SmartReflex modules.

The SmartReflex module is enabled by setting the SMARTREFLEXn.SRCONFIG[11] SRENABLE bit. The SmartReflex module is composed of six blocks:

- Clock generator
- Sensor core
- Accumulator
- Minimum/maximum/average
- Error generator
- Interrupt generator

Clock Generator

The clock generator provides the internal SMARTREFLEX_CLK sampling clock to the sensor core of the module. The SMARTREFLEXn.SRCONFIG[21:12] SRCLKLENGTH bit field allows the setting of the frequency divider ratio between SMARTREFLEXn_SYS_CLK and the SMARTREFLEX_CLK. It is calculated using Equation 1:

$$\text{SMARTREFLEXn.SRCONFIG[21:12] SRCLKLENGTH} = f_{\text{SMARTREFLEXn\_SYS\_CLK}} / (2 * f_{\text{SMARTREFLEX\_CLK}}) \quad (1)$$

Where $f_{\text{SMARTREFLEXn\_SYS\_CLK}}$ is the frequency of the SMARTREFLEXn_SYS_CLK, and $f_{\text{SMARTREFLEX\_CLK}}$ is the desired SMARTREFLEX_CLK frequency.

To make accurate use of the target values programmed for the SmartReflex modules in the device, the SRCLKLENGTH parameter must be set correctly. The target values for the SmartReflex modules are calculated with the SMARTREFLEX_CLK frequency set at 100 kHz. It is thus mandatory that the value of the SRCLKLENGTH parameter is calculated from Equation 1 with $f_{\text{SMARTREFLEX\_CLK}}$ set at 100 kHz.

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For example, if the system clock has a frequency of 38.4 MHz, and the target SMARTREFLEX_CLK frequency is 100 kHz, the SMARTREFLEXn.SRCONFIG[21:12] SRCLKLENGTH bit field is 192 (0x0C0).

Sensor Core

The sensor cores (SVT and LVT) receive the SMARTREFLEX_CLK sampling clock and the voltage to be sensed. They generate sensor value samples proportional to the voltage sensed. For accuracy, a sensor core is composed of two sensors (N and P) and generates two values per sample (one from each sensor).

Two sample values generated by the SVT sensor core output can be read from the SMARTREFLEXn.SENVAL[15:0] SENNVAL and SMARTREFLEXn.SENVAL[31:16] SENPVAL bit fields. The other two sample values generated by the LVT sensor core output can be read from the SMARTREFLEXn.LVTSENVAL[15:0] LVTSENNVAL and SMARTREFLEXn.LVTSENVAL[31:16] LVTSENPVAL bit fields.

The SVT sensor core is enabled by the SMARTREFLEXn.SRCONFIG[10] SENENABLE bit. The LVT sensor core is enabled by the SMARTREFLEXn.SRCONFIG[4] LVTSENENABLE bit.

Accumulator

The accumulator consists of two stacks that store multiple samples of the four sensor values received from the sensor cores.

The SMARTREFLEXn.SRCONFIG[31:22] ACCUMDATA bit field defines the size of the accumulator in the number of samples to be stored. The allowable range is from 2 to 1023. The value of the SMARTREFLEXn.SRCONFIG[31:22] ACCUMDATA bit field is related to the desired sampling time window ($T_{TimeWindow}$) and the SMARTREFLEX_CLK frequency ($f_{SMARTREFLEX\_CLK}$). It can be calculated using Equation 2:

$$\text{SMARTREFLEXn.SRCONFIG[31:22] ACCUMDATA} = T_{TimeWindow} * f_{SMARTREFLEX\_CLK} \quad (2)$$

For example, for an accumulator time window of 10 ms and SMARTREFLEX_CLK frequency of 32 kHz, the value of SMARTREFLEXn.SRCONFIG[31:22] ACCUMDATA is 320 (0x140). The accumulation window must be large enough so that the minimum, maximum, and average counter values are accurate.

Minimum/Maximum/Average

The minimum/maximum/average block reads the samples stored in the accumulator and returns the minimum, maximum, and average values of the samples. Because the accumulator contains four separate groups of samples (one from each sensor of the sensor cores), the minimum/maximum/average block also generates four sets of minimum, maximum, and average values.

The minimum, maximum, and average values of the samples of the first SVT sensor can be read from the SMARTREFLEXn.SENMIN[15:0] SENNMIN, SMARTREFLEXn.SENMAX[15:0] SENNMAX, and SMARTREFLEXn.SENAVG[15:0] SENNAVG bit fields. The minimum, maximum, and average values of the samples of the first LVT sensor can be read from the following bit fields:

- SMARTREFLEXn.LVTSENMIN[15:0] LVTSENNMIN
- SMARTREFLEXn.LVTSENMAX[15:0] SENNMAX
- SMARTREFLEXn.LVTSENAVG[15:0] LVTSENNAVG

For the sample values of the second SVT sensor, the minimum, maximum, and average values can be read from the SMARTREFLEXn.SENMIN[31:16] SENPMIN, SMARTREFLEXn.SENMAX[31:16] SENPMAX, and SMARTREFLEXn.SENAVG[31:16] SENPAVG bit fields. For the sample values of the second LVT sensor, the minimum, maximum, and average values can be read from the following bit fields:

- SMARTREFLEXn.LVTSENMIN[31:16] LVTSENPMIN
- SMARTREFLEXn.LVTSENMAX[31:16] LVTSENPMAX
- SMARTREFLEXn.LVTSENAVG[31:16] LVTSENPAVG

The minimum/maximum/average block is enabled by the SMARTREFLEXn.SRCONFIG[8] MINMAXAVGENABLE bit.

The accumulated values and status registers are reset when one of the following occurs:

- SMARTREFLEXn.SRCONFIG[11] SRENABLE is cleared to 0x0.
- SMARTREFLEXn.IRQSTATUS[3] MCUACCUMINTSTATENA is cleared by writing 0x1 to it.

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Error Generator

The error generator block reads the sample value generated by the sensor cores and compares it with a reference value to calculate the error. This error is then passed to the voltage processor and the internal interrupt generator block.

The reference value for a given OPP of the device is configured by setting the following bit fields by reading the corresponding values from the control module (see Section 3.8.3.2.6, *SmartReflex Parameters Set After Silicon Characterization*):

- SMARTREFLEXn.NVALUERECIPROCAL[23:20] SENPGAIN
- SMARTREFLEXn.NVALUERECIPROCAL[19:16] SENNGAIN
- SMARTREFLEXn.NVALUERECIPROCAL[15:8] RNSENP
- SMARTREFLEXn.LVTNVALUERECIPROCAL[23:20] SENPGAIN
- SMARTREFLEXn.NVALUERECIPROCAL[7:0] RNSENN
- SMARTREFLEXn.LVTNVALUERECIPROCAL[19:16] SENNGAIN
- SMARTREFLEXn.LVTNVALUERECIPROCAL[15:8] RNSENP
- SMARTREFLEXn.LVTNVALUERECIPROCAL[7:0] RNSENN

The error generator sets the SMARTREFLEXn.SRSTATUS[1] ERRORGENERATORVALID status bit when a valid error value is set in the SMARTREFLEXn.SENERROR_REG register.

The SMARTREFLEXn.SENERROR_REG register contains the average error (SMARTREFLEXn.SENERROR_REG[15:8] AVGERROR) and the percentage of error (SMARTREFLEXn.SENERROR_REG[7:0] SENERROR).

The error generator block is enabled by the SMARTREFLEXn.SRCONFIG[9] ERRORGENERATORENABLE bit.

In the error generator module, the sensor with the highest frequency error (SVT or LVT) is selected for processing the voltage change request.

Interrupt Generator

The interrupt generator block generates interrupts to INTC_MPU and the voltage processor module (if the corresponding interrupts are enabled) to indicate errors.

Table 3-300 and Table 3-301 list the interrupt events in the SmartReflex module and their enable and status bits.

Table 3-300. SmartReflex Interrupt Events

Interrupt Type	Description
Accumulator	The minimum/maximum/average module has completed computation of the accumulator data.
Valid	The average error is less than 2 percent of the true average error.
Disable acknowledge	The SmartReflex module is disabled and has cleared all INTC_MPU and VP interrupts (internal registers are reset). This interrupt indicates to the software that the SmartReflex module is available for programming.
Bounds	The frequency error has crossed the maximum limit (ERRMAXLIMIT) or the minimum limit (ERRMINLIMIT). It is also mapped to the voltage processor.

The SMARTREFLEXn_IPU_IRQs from SMARTREFLEX_MM and SMARTREFLEX_CORE are mapped to the IPU_IRQ_48 interrupt line of the INTC_IPU.

Table 3-301. SmartReflex Interrupt Events Enable and Status Bits

Interrupt Type	Enable Bit	Status Bit
Accumulator	SMARTREFLEXn.IRQENABLE_SET[3] MCUACCUMINTENSET	SMARTREFLEXn.IRQSTATUS[3] MCUACCUMINTSTATENA
	SMARTREFLEXn.IRQENABLE_CLR[3] MCUACCUMINTENCLR	

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Table 3-301. SmartReflex Interrupt Events Enable and Status Bits (continued)

Interrupt Type	Enable Bit	Status Bit
Valid	SMARTREFLEXn.IRQENABLE_SET[2] MCUVALIDINTENSET	SMARTREFLEXn.IRQSTATUS[2] MCUVALIDINTSTATENA
	SMARTREFLEXn.IRQENABLE_CLR[2] MCUVALIDINTENCLR	
Disable acknowledge	SMARTREFLEXn.IRQENABLE_SET[0] MCUDISABLEACKINTENSET	SMARTREFLEXn.IRQSTATUS[0] MCUDISABLEACKINTSTATENA
	SMARTREFLEXn.IRQENABLE_CLR[0] MCUDISABLEACKINTENCLR	
Bounds	SMARTREFLEXn.IRQENABLE_SET[1] MCUBOUNDSINTENSET	SMARTREFLEXn.IRQSTATUS[1] MCUBOUNDSINTSTATENA
	SMARTREFLEXn.IRQENABLE_CLR[1] MCUBOUNDSINTENCLR	
	SMARTREFLEXn.ERRCONFIG[22] VPBOUNDSINTENABLE	SMARTREFLEXn.ERRCONFIG[23] VPBOUNDSINTSTATENA

The minimum and maximum error limits for the bounds interrupt are configured in the SMARTREFLEXn.ERRCONFIG[15:8] ERRMAXLIMIT and SMARTREFLEXn.ERRCONFIG[7:0] ERRMINLIMIT bit fields.

Writing 1 to a bit in the SMARTREFLEXn.IRQSTATUS register clears the interrupt pending status of each interrupt source whose corresponding bit is 1 in the value written. Other interrupt pending status bits are not affected (writing 0 to that bit does not affect the status).

3.8.3.2.4 SmartReflex Convergence Verification

SmartReflex convergence verification is mandatory for the MPU, IVA, and CORE power domains. The goal of this verification is that the VSR (Voltage SmartReflex) is calibrated with SmartReflex within the expected error range. If VSR is calibrated within the expected error range, the calibration is converged without issue. If VSR is not calibrated within the expected error range, the following issues may occur:

- If the calibration of VSR is high, there is a convergence issue that could lead to an increase in power consumption.
- Low VSR (near the VMIN) could lead to platform instability.

Convergence verification requires the following steps, with at least one sample on the customer product with customer software:

1. Set the device to the desired OPP (for more information, see Section 3.10.4.3, *Changing OPP*.
2. Enable the SmartReflex in the SRCONFIG[11] SRENABLE register.
3. Wait for the SmartReflex to converge.
4. Retrieve the required SmartReflex registers to verify that the error percentage (%error) per calculation is in the expected range.

NOTE: Convergence verification must be done in the listed sequence for each power rail and each OPP.

The following registers exist for each power rail; the appropriate register must be used:

1. The following registers must be retrieved after SmartReflex has converged to verify that the convergence is within the expected range:
   - SR.SENVAL
   - SR.NVALUERECIPROCAL
   - SR.ERRCONFIG
2. The following calculations are used to verify that the obtained voltage is converged:

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(a) Extract the following values from the listed registers:
NCOUNT:

- COUNT of SENP = SR.SENVAL[31:16] SENPVAL
- COUNT of SENN = SR.SENVAL[15:0] SENNVAL

TARGET:

$$\text{TARGET OF SENP} = \frac{2^{[\text{hex2dec(SR.NVALUERECIPROCAL[23:20] SENPGAIN + 8)}]}}{\text{hex2dec(SR.NVALUERECIPROCAL[15:8] SENPRN)}}$$

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$$\text{TARGET OF SENN} = \frac{2^{[\text{hex2dec(SR.NVALUERECIPROCAL[19:16] SENNGAIN + 8)}]}}{\text{hex2dec(SR.NVALUERECIPROCAL[7:0] SENNRN)}}$$

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ERRMINLIMIT:

- ERRMINLIMIT = SR.ERRCONFIG[7:0] ERRMINLIMIT

ERRMAXLIMIT:

- ERRMAXLIMIT = SR.ERRCONFIG[15:8] ERRMAXLIMIT

(b) Calculate %error:

$$\text{SENP\%error} = \frac{\text{TARGET of SENP} - \text{COUNT of SENP}}{\text{TARGET of SENP}}$$

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$$\text{SENN\%error} = \frac{\text{TARGET of SENN} - \text{COUNT of SENN}}{\text{TARGET of SENN}}$$

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- %error = max(SENP%error, SENN%error)

NOTE: To be successfully converged, %error must be within the follwing range:
ERRMINLIMIN < %error < ERRMAXLIMIT

NOTE: If the %error is not within the expected range, check the SmartReflex parameters that are used in customer software.

3.8.3.2.5 Status Register

The status register (SRSTATUS) indicates the validity of the minimum/maximum/average and error generator output values.

SRSTATUS has the following bits and bit fields:

- SMARTREFLEXn.SRSTATUS[3] AVGERRVALID: Indicates the validity of the value in the SMARTREFLEXn.SENERROR_REG[15:8] AVGERROR bit field. When the value is 0, the average error is not valid. When the value is 1, the average error is within 2 percent of the valid average error.
- SMARTREFLEXn.SRSTATUS[2] MINMAXAVGVALID: Indicates the validity of the following registers:
  - SMARTREFLEXn.SENVAL
  - SMARTREFLEXn.SENMIN
  - SMARTREFLEXn.SENMAX
  - SMARTREFLEXn.SENAVG
  - SMARTREFLEXn.LVTSENVAL
  - SMARTREFLEXn.LVTSENMIN

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  - SMARTREFLEXn.LVTSENMAX
  - SMARTREFLEXn.LVTSENAVG

  When the value is 0, the registers are not valid. When the value is 1, the registers contain valid values, although the values are not necessarily fully accumulated.
- SMARTREFLEXn.SRSTATUS[1] ERRGEN_VALID: Indicates the validity of the value in the SMARTREFLEXn.SENERROR_REG[7:0] SENERROR bit field. When the value is 0, the error value is invalid. When the value is 1, the error value is valid.
- SMARTREFLEXn.SRSTATUS[0] MINMAXAVGACCUMVALID: Indicates that the following registers contain their final values accumulated over the defined sample time period:
  - SMARTREFLEXn.SENVAL
  - SMARTREFLEXn.SENMIN
  - SMARTREFLEXn.SENMAX
  - SMARTREFLEXn.SENAVG
  - SMARTREFLEXn.LVTSENVAL
  - SMARTREFLEXn.LVTSENMIN
  - SMARTREFLEXn.LVTSENMAX
  - SMARTREFLEXn.LVTSENAVG

3.8.3.2.6 SmartReflex Parameters Set After Silicon Characterization

Certain parameters of the SmartReflex module are characterized and calibrated after silicon testing. These values are then provided separately. Users must configure these parameters according to their given values to ensure correct functioning of the module.

The values for the following parameters (explained in Section 3.8.3.2.3, *SmartReflex Submodules*) are set in the control module after device silicon characterization:

- SMARTREFLEXn.NVALUERECIPROCAL[23:20] SENPGAIN
- SMARTREFLEXn.NVALUERECIPROCAL[19:16] SENNGAIN
- SMARTREFLEXn.NVALUERECIPROCAL[15:8] SENPRN
- SMARTREFLEXn.NVALUERECIPROCAL[7:0] SENNRN
- SMARTREFLEXn.LVTNVALUERECIPROCAL[23:20] SENPGAIN
- SMARTREFLEXn.LVTNVALUERECIPROCAL[19:16] SENNGAIN
- SMARTREFLEXn.LVTNVALUERECIPROCAL[15:8] SENPRN
- SMARTREFLEXn.LVTNVALUERECIPROCAL[7:0] SENNRN

The value of these parameters must be read from the corresponding registers of the control module.

Information about the following parameters of the SmartReflex module is provided after silicon characterization:

- SMARTREFLEXn.AVGWEIGHT_REG[3:2] SENPAVGWEIGHT
- SMARTREFLEXn.AVGWEIGHT_REG[1:0] SENNAVGWEIGHT
- SMARTREFLEXn.ERRCONFIG[18:16] ERRWEIGHT
- SMARTREFLEXn.ERRCONFIG[15:8] ERRMAXLIMIT
- SMARTREFLEXn.ERRCONFIG[7:0] ERRMINLIMIT

The recommended values for the ERRCONFIG register bit fields are:

- ERRCONFIG[18:16] ERRWEIGHT: Recommended value is 0x4 (1280 µs)
- ERRCONFIG[15:8] ERRMAXLIMIT: Recommended value is 0x2 (1.60%)
- ERRCONFIG[7:0] ERRMINLIMIT: Recommended values are OPP and technology-dependent. Initial development values are:
  - 0xF4 (–9.6%) for OPP_LOW
  - 0xF9 (–5.6%) for OPP_NOM

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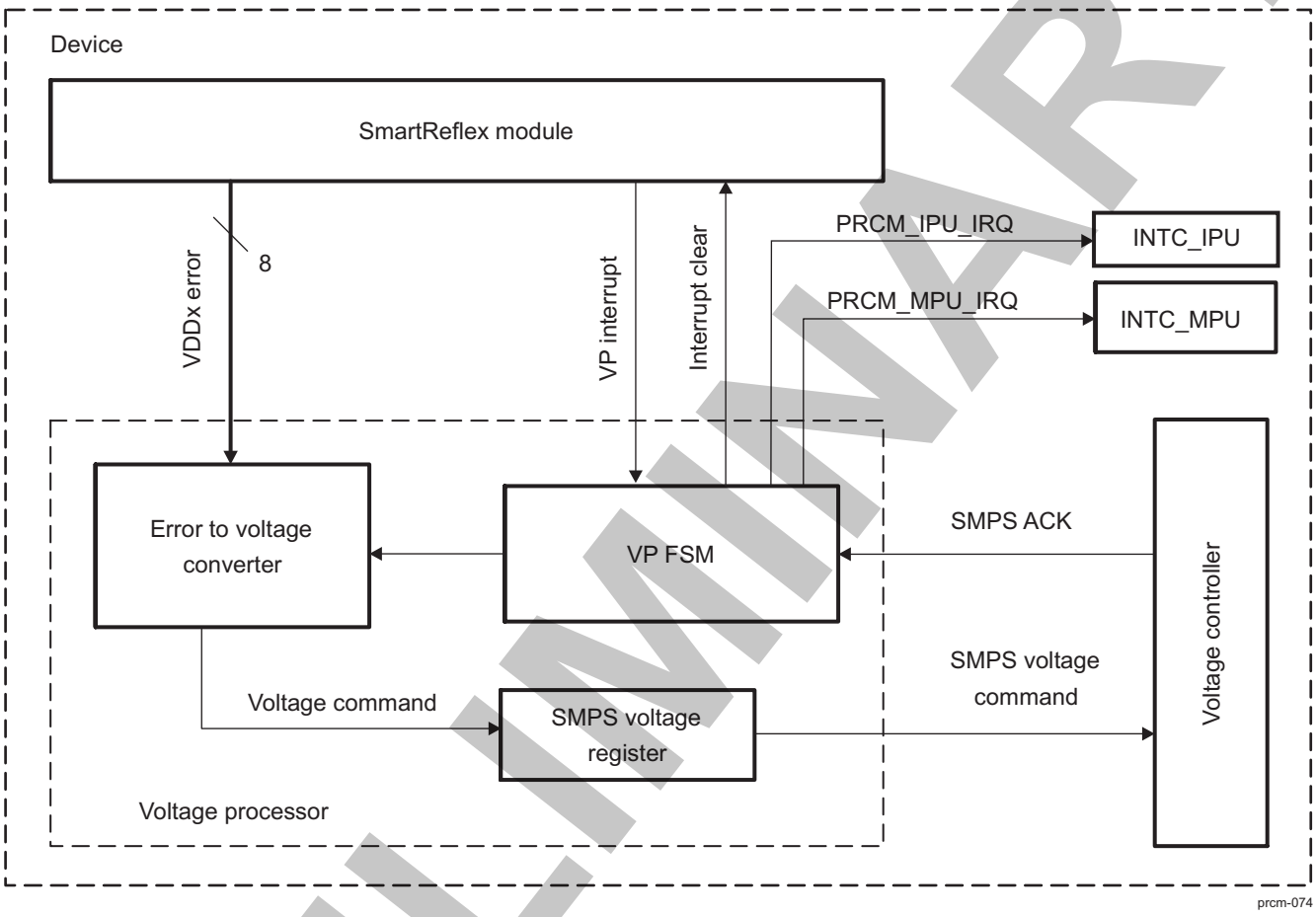
– 0xFA (–4.0%) for OPP_HIGH

3.8.3.2.7 Voltage Processor Module

Figure 3-80 is a functional overview of the voltage processor.

Figure 3-80. Voltage Processor Functional Overview



The voltage processor receives an error value and a VP interrupt signal from the SmartReflex module. Each time a new error value is sent, the SmartReflex module triggers an interrupt to inform the voltage processor. The voltage processor consists of an error-to-voltage command converter and a state controller. It processes an error and sends a voltage command to the voltage controller. It receives an acknowledge signal from the voltage controller when the SMPS receives the command. The voltage processor then acknowledges the SmartReflex module by clearing its interrupt.

The voltage processor is enabled by the PRM_VP_n_CONFIG[0] VPENABLE bit.

Voltage Processor Interrupts

The voltage processor uses the PRM_IPU_IRQ (IPU_IRQ_47 of INTC_IPU) interrupt line of the IPU and PRM_MPU_IRQ (MPU_IRQ_11 of INTC_MPU) interrupt line of the MPU. They can be enabled through PRM_IRQENABLE_IPU and PRM_IRQENABLE_MPU registers. Table 3-302 and Table 3-303 list the interrupt events in the voltage processor module and their enable and status bits.

Table 3-302. Voltage Processor Interrupt Events

Interrupt Type	Description
Transaction done	Voltage processor transaction is complete.
Equal value	Voltage requested in the new voltage command is the same as the current SMPS voltage.

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Table 3-302. Voltage Processor Interrupt Events (continued)

Interrupt Type	Description
No SMPS acknowledge	SMPS has not responded in a defined time interval to the transmitted voltage command.
Maximum VDD	New voltage requested in the voltage command is equal to or greater than maximum VDD.
Minimum VDD	New voltage requested in the voltage command is equal to or less than minimum VDD.
OPP change done	The average error is within the desired limit.

NOTE: Transaction done and OPP change done interrupt events are generated under the same conditions (after voltage change).

Table 3-303. Voltage Processor Interrupt Event Enable and Status Bits

Interrupt Type	Enable Bit	Status Bit
Transaction done	PRM_IRQENABLE_IPU[21] VP_CORE_TRANXDONE_EN	PRM_IRQSTATUS_IPU[21] VP_CORE_TRANXDONE_ST
	PRM_IRQENABLE_IPU[29] VP_MM_TRANXDONE_EN	PRM_IRQSTATUS_IPU[29] VP_MM_TRANXDONE_ST
Equal value	PRM_IRQENABLE_IPU[20] VP_CORE_EQVALUE_EN	PRM_IRQSTATUS_IPU[20] VP_CORE_EQVALUE_ST
	PRM_IRQENABLE_IPU[28] VP_MM_EQVALUE_EN	PRM_IRQSTATUS_IPU[28] VP_MM_EQVALUE_ST
No SMPS acknowledge	PRM_IRQENABLE_IPU[19] VP_CORE_NOSMPSACK_EN	PRM_IRQSTATUS_IPU[19] VP_CORE_NOSMPSACK_ST
	PRM_IRQENABLE_IPU[27] VP_MM_NOSMPSACK_EN	PRM_IRQSTATUS_IPU[27] VP_MM_NOSMPSACK_ST
Maximum VDD	PRM_IRQENABLE_IPU[18] VP_CORE_MAXVDD_EN	PRM_IRQSTATUS_IPU[18] VP_CORE_MAXVDD_ST
	PRM_IRQENABLE_IPU[26] VP_MM_MAXVDD_EN	PRM_IRQSTATUS_IPU[26] VP_MM_MAXVDD_ST
Minimum VDD	PRM_IRQENABLE_IPU[17] VP_CORE_MINVDD_EN	PRM_IRQSTATUS_IPU[17] VP_CORE_MINVDD_ST
	PRM_IRQENABLE_IPU[25] VP_MM_MINVDD_EN	PRM_IRQSTATUS_IPU[25] VP_MM_MINVDD_ST
OPP change done	PRM_IRQENABLE_IPU[16] VP_CORE_OPPCHANGEDONE_EN	PRM_IRQSTATUS_IPU[16] VP_CORE_OPPCHANGEDONE_ST
	PRM_IRQENABLE_IPU[24] VP_MM_OPPCHANGEDONE_EN	PRM_IRQSTATUS_IPU[24] VP_MM_OPPCHANGEDONE_ST
VP command acknowledged	PRM_IRQENABLE_IPU[22] VC_CORE_VPACK_EN	PRM_IRQSTATUS_IPU[22] VC_CORE_VPACK_ST
	PRM_IRQENABLE_IPU[30] VC_MM_VPACK_EN	PRM_IRQSTATUS_IPU[30] VC_MM_VPACK_ST

Voltage Processor Status

The status of the voltage processor is represented by the following:

Bits	Parameter	Description
PRCM module.PRM_VPn_VOLTAGE[7:0] VPVOLTAGE	Current voltage for SMPS	Value of the current voltage level requested by the voltage processor
PRCM module.PRM_VPn_STATUS[0] VPINIDLE	Voltage processor in INACTIVE state	The voltage processor is in idle mode.

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Voltage Processor Parameters

The following parameters of the voltage processor must be configured:

Bits	Parameter	Description
PRCM.PRM_VPn_CONFIG[31:24] ERROROFFSET	Error offset	Error in voltage offset value
PRCM.PRM_VPn_CONFIG[23:16] ERRORGAIN	Error gain	Error in voltage gain value
PRCM.PRM_VPn_CONFIG[3] TIMEOUTEN	Time-out enable	Enables/disables the time-out set by the time-out delay parameter. 0: Time-out is disabled, VP FSM waits indefinitely. 1: Time-out is enabled. Time out will occurs when the programmed time-out value have elapsed.
PRCM.PRM_VPn_VSTEPMIN[7:0] VSTEPMIN	Minimum step size	Minimum voltage step size
PRCM.PRM_VPn_VSTEPMAX[7:0] VSTEPMAX	Maximum step size	Maximum voltage step size
PRCM.PRM_VPn_VLIMITTO[31:24] VDDMAX	Maximum VDD limit	Maximum voltage limit of the VDD. The VDDMAX registers are the maximum allowable voltage levels of the SMPS. This value is determined by the SMPS specification as well as the application specification. The upper bound on the SMPS voltage is VddMax.
PRCM.PRM_VPn_VLIMITTO[23:16] VDDMIN	Minimum VDD limit	Minimum voltage limit of the VDD. The VDDMIN registers are the minimum allowable voltage levels of the SMPS. This value is determined by the SMPS specification as well as the application specification. The lower bound on the SMPS voltage is VddMin.
PRCM.PRM_VPn_VLIMITTO[15:0] TIMEOUT	Time-out delay	Maximum delay between a voltage change command and its acknowledge. The TIMEOUT register determines the number of SYS_CLK cycles that the voltage controller state-machine will wait for the rising edge of SMPS VP_acknowledge, when PRCM.PRM_VPn_CONFIG[3] TIMEOUTEN = 1. If PRCM.PRM_VPn_CONFIG[3] TIMEOUTEN = 0, the loop will wait indefinitely.
PRCM.PRM_VPn_CONFIG[15:8] INITVDD	Initial VDD voltage	Initial voltage set in the voltage processor
PRCM.PRM_VPn_CONFIG[2] INITVDD	Initialize VDD	Set initial voltage given in initial VDD voltage parameter in the voltage processor
PRCM.PRM_VPn_VSTEPMIN[23:8] SMPSWAITTIMEMIN	Minimum SMPS wait time	Slew rate for negative voltage steps
PRCM.PRM_VPn_VSTEPMAX[28:8] SMPSWAITTIMEMAX	Maximum SMPS wait time	Slew rate for positive voltage steps
PRCM.PRM_VPn_CONFIG[1] FORCEUPDATE	Force update	Sends the value of the VP current voltage parameter as the new voltage command to SMPS

3.8.3.2.8 SMPS-Dependent Parameter Configuration

The values of the following parameters of the voltage processor module depend on the characteristics of the SMPS used:

- PRCM.PRM_VPn_CONFIG[31:24] ERROROFFSET
- PRCM.PRM_VPn_CONFIG[23:16] ERRORGAIN
- PRCM.PRM_VPn_VSTEPMIN[7:0] VSTEPMIN
- PRCM.PRM_VPn_VSTEPMAX[7:0] VSTEPMAX
- PRCM.PRM_VPn_VLIMITTO[31:24] VDDMAX
- PRCM.PRM_VPn_VLIMITTO[23:16] VDDMIN
- PRCM.PRM_VPn_VLIMITTO[15:0] TIMEOUT
- PRCM.PRM_VPn_VSTEPMIN[23:8] SMPSWAITTIMEMIN
- PRCM.PRM_VPn_VSTEPMAX[28:8] SMPSWAITTIMEMAX

For information about the values of these parameters, see the specification document of the SMPS used.

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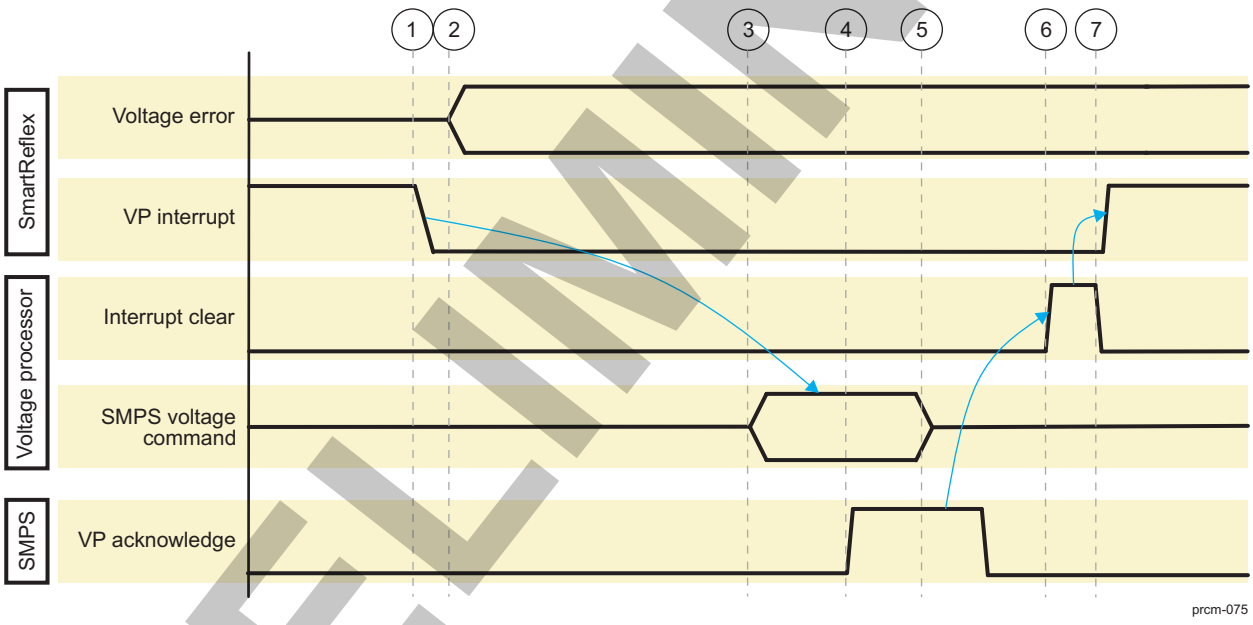
3.8.3.2.9 Communication Between SmartReflex, Voltage Processor, Voltage Controller, and SMPS

The SmartReflex module, voltage processor, voltage controller, and SMPS implement a simple handshake protocol based on a request/acknowledge mechanism (see Figure 3-81):

1. The SmartReflex module generates a VP interrupt (clears to 0) when the average error crosses the minimum or maximum error bounds.
2. The average VDDx error is passed to the voltage processor when automatic voltage control is enabled.
3. The voltage processor reads the error and generates the voltage command for the SMPS. It then informs the voltage controller that a new voltage command is ready for the SMPS. The voltage controller sends the voltage command to the SMPS (external power IC) through the dedicated I^2C interface.
4. The SMPS responds to the reception of the voltage command with an acknowledgment to the voltage controller.
5. The voltage controller sends the acknowledgment to the voltage processor.
6. The voltage processor sends the interrupt-clear signal to the SmartReflex module.
7. The SmartReflex module clears the VP interrupt. It is now again ready to send a new frequency-error interrupt to the voltage processor.

Figure 3-81. SmartReflex – SMPS Communication for Automatic Voltage Adjustments



3.8.4 Internal LDOs Control

3.8.4.1 Memory LDOs

Embedded SRAM LDOs are used to supply power to the split-rail memory arrays. The PRM generates the controls used to select LDO operating mode: on-active, on-retention, or off.

Split-rail type SRAMs are used in the device to implement the larger memories. These SRAMs feature memory array and periphery logic, which are on separate supplies to allow independent power management. Proper memory operation, however, requires the SRAM array voltage never to be operated at a level lower than the SRAM periphery logic.

Memory LDO can switch to on, retention, and off modes:

- On (active) mode: 1.15 V is the normal voltage reference used through all functional OPPs whenever memories must be functional. When logic voltage level VDD_x_L (where x can be MPU, CORE, or MM) becomes higher than the associated memory voltage level VDD_x_M, the LDO operates in tracking mode and follows its respective VDD_x_M or VDD_x_ABB voltage level.

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- Retention mode: 0.6 V is set when software allows and when all memory banks belonging to the LDO memory voltage are in RETENTION state. In this mode, the output voltage is generated from the corresponding VDD_WKUP_L logic voltage source.

Section 3.8.6.1, *Memory LDOs Transitions*, describes the state transition conditions and sequences for the memory LDOs.

NOTE: The voltage levels associated with the different modes may depend on the device characteristics.

3.8.4.2 WAKEUP LDOs

When the device enters its lower standby mode (named off mode), some logic blocks and memories remain supplied to allow restarting the device without needing to perform its full reinitialization: this is the wake-up voltage domain. This domain also includes most of the logic needed to perform the emulation and debug features. The lowest power consumption in standby mode is achieved by supplying the wake-up voltage domain only in off mode. To minimize power consumption at the platform level when the device is in this mode, all logic voltage supply regulators can be turned off, because the wake-up voltage domain is supplied by an embedded LDO using the 1.2-V I/O voltage supply on its input.

The WAKEUP LDO supports three voltage states, depending on the PD_WKUPAON and PD_EMU activity:

- EMULATION overdrive: The voltage level is 1.16 V, and the LDO is set in bypass mode. OPP_WKUP_EMULATION is reached as soon as emulation/debug is active, regardless of the device mode (standby, off, or on)
- ON: The voltage reference (default state) is 1.0 V. Other voltage domains are active or idle, emulation/debug is inactive.
- SLEEP: The voltage reference is 0.9 V. It is set when the device enters sleep mode. All other voltage domains are inactive or off, and emulation/debug is inactive.

Section 3.8.6.3, *VDD_WKUP_L Transitions,* describes the state transition conditions and sequences for the WAKEUP LDO.

NOTE: The voltage levels associated with the different modes may depend on the device characteristics.

At boot time, the WAKEUP LDO is started in emulation mode. It is a software command (that is, from OS or ROM code) to set it to a different mode.

3.8.4.3 ABB LDOs Control

The ABBLDO supports three voltage modes:

- Bypass mode: In this mode, the ABBLDO_x is bypassed and outputs the VDD_x_L voltages (x refers to the MPU and MM). This mode is activated when FBB is not required, or when the voltage domain enters low-power mode.
- FBB mode is enabled when the device is a weak process device at the highest OPP.

The PRCM module provides the PRM_ABBLDO_MPU_SETUP and PRM_ABBLDO_MM_SETUP registers for configuration with the following controls:

- SR2EN: To enable or bypass the ABB power management
- ACTIVE_FBB_SEL: To enable or bypass FBB mode
- SR2_WTCNT_VALUE: LDO settling delay on OPP change. The delay is in the number of system clock cycles.

The PRCM module provides the PRM_ABBLDO_MPU_CTRL and PRM_ABBLDO_MM_CTRL registers for control:

- OPP_SEL: Current operational OPP

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- OPP_CHANGE: Initiate an OPP-based ABBLDO setting change
- SR2_STATUS: Current mode of operation of ABBLDO
- SR2_IN_TRANSITION: ABBLDO in transition

For the ABBLDO state-change programming sequence, see Section 3.10.4.3, *Changing OPP*.

3.8.4.4 BANDGAPsControl

BANDGAPs provides voltage reference for internal LDOs. The PRCM module automatically controls the switching between ON and OFF states of the BANDGAPs, based on the power state of the device. It is completely transparent to user software.

BANDGAPs startup time is 100 µs. The PRM_BANDGAP_SETUP[7:0] STARTUP_COUNT bit field must be set accordingly.

3.8.5 EMIF-Specific Interface

The PRCM module provides to the EMIF a special signal to increase the rate of incremental leveling during the voltage update. This signal is active when OPP changes during the voltage ramp of VD_CORE.

This signal is driven by hardware during the OPP change of VD_CORE, if it passes through the voltage processor (force update). It is controlled by software in case the OPP voltage change is done through VOLCON without passing through the voltage processor (bypass).

An override bit, PRM_VC_VAL_BYPASS[25] OPP_CHANGE_EMIF_LVL, is available. When this bit is set to 1, the special signal is forced to 1. When this bit is cleared to 0, the special signal is forced to 0 (if not driven to 1 by hardware).

3.8.6 Voltage Domain State Transitions

Section 3.1.1.3.1, *Voltage Domain*, describes the supported states of a voltage domain. This section describes the trigger conditions to enable and perform sleep and wake-up transitions on PRCM module-controlled voltage domains:

- VDD_MPU_L
- VDD_MM_L
- VDD_CORE_L
- VDD_MPU_M
- VDD_MM_M
- VDD_CORE_M

It also identifies state transition sequences for these voltage domains.

When the voltage domain state-transition control is set to automatic, the PRCM module initiates the voltage domain state transition when the required hardware conditions are satisfied. These hardware conditions can be based on the power domain state conditions and/or system clock state conditions. The PRCM module prevents any transition when the associated conditions are not satisfied.

The VDD_MPU_M, VDD_MM_M, or VDD_CORE_M memory voltage domain is automatically transitioned to the retention level whenever all memory arrays in the domain reach the RETENTION power state. Similarly, a transition back to ON power state is triggered upon one or more domain memory arrays requiring a transition back to ON power state.

If a voltage command acknowledgment is not received within an allowed response time window (communications error over the I^2C interface), an error status is logged, a global warm reset is generated, and the transition is skipped.

3.8.6.1 VDD_x_L Transitions

The transition trigger conditions for sleep transition from ON to SLEEP or RETENTION state are:

- Software setting: PRM_VOLTCTRL[a:b] AUTO_CTRL_VDD_<x>_L = SLEEP (0x1) or RETENTION (0x2)

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- Power state conditions:
  - For voltage domain SLEEP state transition: All power domains in the voltage domain must be in the ON-INACTIVE or the RETENTION state.
  - For voltage domain RETENTION state transition: All power domains in the voltage domain must be in the RETENTION state.
  - VDD_MPU_L (MPU voltage domain) transition status can be check by reading bit PRM_VOLTST_MPU[20] INTRANSITION. VDD_MM_L (MM voltage domain) transition status can be checked by reading bit PRM_VOLTST_MM[20] INTRANSITION.
- Clock state conditions: No clock activity on voltage domain

NOTE:

- In case of VDD_CORE_L sleep transition from ON to SLEEP state, the PD_CORE can be only in ON-INACTIVE or RETENTION state.
- In case of VDD_MPU_L and VDD_MM_L sleep transition from ON to SLEEP state, the reference and bypass clocks to their respective DPLLs must also be gated.
- In both cases, upon completion of CORE voltage domain sleep transition, PRCM asserts COREAON_IO_SRCOMP_PWRDN signal. It waits for 8 SYS_CLK cycles then disables COREAON_IO_SRCOMP_GFCLK clock.

The transition trigger condition for a wake-up transition from SLEEP or RETENTION to ON state is:

- Any wake-up event occurs on the voltage domain.

The state transition sequence is:

1. All transition trigger conditions are met.
2. The voltage controller sends an ON, SLEEP, or RETENTION command sequence over the I^2C interface.
3. The PRCM module waits for an I^2C command sequence acknowledge.
4. The PRCM module starts the voltage transition counter.
5. When the counter expires, a voltage transition is complete.

NOTE: Upon completion of CORE voltage domain transition to ON from SLEEP or RET, PRCM enables COREAON_IO_SRCOMP_GFCLK clock. It waits for 8 SYS_CLK cycles then de-asserts COREAON_IO_SRCOMP_PWRDN signal.

3.8.6.2 Memory LDO Transitions

The transition trigger condition for on-to-retention mode is:

- At least one memory bank associated with the LDO is in RETENTION state and the rest of the memory banks are in RETENTION state.

The transition sequence is:

1. Transition trigger conditions are true (that is, satisfied).
2. Switch LDO reference to RETENTION mode value if on-to-retention mode transition.
3. Start counter for LDO stabilization.
4. When counter expires, voltage transition is complete.

3.8.6.3 VDD_WKUP_L Transitions

The ON-to-SLEEP transition trigger conditions are:

- Power domain states: Device is in low-power state (STANDBY state) and PD_EMU power domain is off.
- Clock states: Only the 32K clock is active in CD_WKUPAON (and the system clock is gated at the SCRM level).

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The SLEEP-to-ON transition trigger conditions are:

- Any device wake-up event other than emulation wake-up event

The EMULATION-to-ON transition trigger conditions are:

- Power domain states: PD_EMU is off and device is in active mode.
- Clock states: PD_EMU is off and any clock other than 32K clock is active in PD_WKUPAON.

The EMULATION-to-SLEEP transition trigger conditions are:

- Power domain states: Device is in low-power state (STANDBY state) and PD_EMU power domain is off.
- Clock states: Only the 32K clock is active in CD_WKUPAON (and the system clock is gated at the SCRM level)

The SLEEP or ON-to-EMULATION transition trigger condition is:

- Any wake-up event on PD_EMU

The transition sequence is:

1. Transition trigger conditions are met.
2. VDD_WKUP_L initiates the transition.
3. Starts a counter for VDD_WKUP_L transition.
4. VDD_WKUP_L transition completes.

3.8.7 DVFS

Dynamic voltage and frequency scaling is a technique that can be used on the logic voltage domains (VDD_MPU_L, VDD_MM_L, and VDD_CORE_L), independently of one another. Upon a current or predictive performance request, determined by software according to ad hoc algorithms or heuristics, software can configure the PRCM module to change the OPP of a voltage domain. For an increase in performance, the voltage is first raised, and then the frequency is increased. For a decrease in performance, the frequency is first decreased, and then the voltage is dropped.

3.8.7.1 EMIF Clock Frequency Scaling Constraints

CD_EMIF is inside PD_CORE. The EMIF subsystem receives the following clocks:

- L3 interface clock
- DLL clock (CORE_DLL_GCLK): for the DLL only
- EMIF_PHY_GCLK clock: Clock used to access the external memory DDR_PHY and to provide the EMIF functional clock. The EMIF functional clock is EMIF_PHY_GCLK divided by 2 inside the EMIF.

The L3 interface clock frequency can be changed on the fly without affecting EMIF operations if the CORE_DLL_GCLK and EMIF_PHY_GCLK clocks are not affected. The EMIF has an internal asynchronous bridge to handle different interface and functional clocks.

When the EMIF_PHY_GCLK clock frequency is to be changed, the EMIF must be put into IDLE state. This ensures that external memory is in self-refresh mode.

Similarly, a change in the DLL frequency implies that the DLL must relock. This can be done only when the EMIF is in IDLE state. Relock time is 250 DLL clock cycles.

The EMIF clocking scheme allows for a change of the OPP without a DLL relock (that is, the DLL is clocked by a relatively low frequency supported in all OPPs); then a change of the OPP consists only in changing the frequency of the EMIF_PHY_GCLK clock (and eventually the frequency of the L3 interface clock).

The EMIF clock control requirements in the PRCM module are:

- The EMIF clock frequency setting must be done through shadow registers for the CORE_DLL_GCLK and EMIF_PHY_GCLK clocks.
- The EMIF clock frequency update bit field must be used to copy the value of the shadow register as the current value.

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- The PRCM module hardware manages the following automatic EMIF clock-frequency update sequence:
  1. Put the EMIF into IDLE state.
  2. Upload shadow register values in the corresponding current register and wait for new EMIF clocks to be stable.
  3. Return the EMIF module to ACTIVE state.

NOTE: The PRCM module must not gate the CORE_DLL_GCLK and EMIF_PHY_GCLK clocks during automatic EMIF frequency change.

Programming model to perform automatic EMIF frequency change as part or not of an OPP change (DVFS). The automatic EMIF frequency change must always be performed while CD_EMIF is under software-forced wakeup (SW_WKUP).

VDD_CORE_L voltage fixed and only clock frequency switching

Changing the frequency of the EMIF clock without changing the voltage (example, change in the value of the SYS_CLK divider while DPLL_CORE is in bypass, change of DPLL_CORE mode between bypass and lock):

1. Software writes new EMIF timing parameters in the shadow registers of the EMIF.
2. Software configures the clock selection and frequency setting shadow registers in the PRCM module.
3. The PRCM module sends an IDLE request to the EMIF (overriding software settings of the MODULEMODE bit field for the EMIF).
4. The EMIF stalls transactions on internal interconnect, completes all committed transactions to external memory, and then puts the external memory in self-refresh mode.
5. The EMIF module then acknowledges the IDLE request of the PRCM module.
6. The PRCM module uploads the values configured in the shadow register bit fields to the corresponding current register bit fields.
7. The PRCM module waits for stabilization of the EMIF_PHY_GCLK and CORE_DLL_GCLK clocks through hardware monitoring, according to new settings.
8. The PRCM module requests the EMIF to exit idle (stops the overriding of software settings of the MODULEMODE bit field for the EMIF).
9. The PRCM module clears the frequency update field.
10. The EMIF copies the timing parameter configured in the shadow register as the current values.
11. The EMIF acknowledges that the PRCM module is functional, and starts accepting the transactions on the internal interconnect.
12. If the DLL clock was changed, the EMIF waits for the DLL to be relocked and for transactions on internal interconnect, if required. The PRCM module is not aware of the DLL operations.
13. Accesses to SDRAM are serviced again.

    Software execution can be stalled during the frequency change without harm as the critical hardware sequence is performed without software intervention. After setting the frequency update field, software must poll only for its clearing.

    Accesses to external SDRAM are stalled for the following duration:

- 2-µs maximum because EMIF is entering and exiting idle
- + 250 DLL clock cycles in case the DLL clock frequency has changed
- + DPLL lock time in case DPLL is locked

VDD_CORE_L voltage change for OPP switching

It is assumed that the frequency of the DLL clock is not changed and that the DPLL_CORE mode is not changed, and remains locked. Only the frequency of the EMIF_PHY_GCLK clock is changed using the post divider. The L3 clock is likely also to be changed, but it does not affect the EMIF.

Accesses to external SDRAM must be stalled for a maximum of 2 µs because of this sequence.

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Voltage scaling up consists of:

1. Software indicates to the EMIF that a voltage change operation has started to allow the EMIF to ensure regular code updates from DLL masters.
2. Software disables SmartReflex for core voltage.
3. Software performs direct VD_CORE setting to new noncorrected value (for weak silicon) and waits for voltage stabilization.
4. Software configures SmartReflex for the corresponding OPP.
5. Software re-enables SmartReflex for core voltage.
6. Software indicates to the EMIF that the voltage change operation is complete and it does not need to control the code update from DLL masters directly.

3.8.7.2 GPMC Clock Frequency Scaling Constraints

CD_L3_MAIN2 is inside the PD_CORE. It supplies the L3MAIN2_L3_GICLK clock to the general-purpose memory controller (GPMC) module, which is used as an interface and functional clock. GPMC timing parameters are programmed at boot for the nominal OPP. These timing parameters can be used for lower L3 frequency, at the expense of slower access to external memory.

External memory connected to the GPMC may not support on-the-fly L3 frequency changes. The following is the sequence to perform L3 frequency change as part or not of an OPP change (DVFS):

- Hardware-controlled sequence:
  1. Software writes new L3 clock settings in the shadow register and sets the frequency update field.
  2. The PRCM module requests idle to the GPMC.
  3. The GPMC requests disconnection of its interconnect port and completes all outstanding transactions.
  4. The GPMC acknowledges idle. Any access to the GPMC is then stalled.
  5. The PRCM module uploads the values of the shadow register bit field in the corresponding current bit field.
  6. The PRCM module waits for stabilization of the L3 clocks by monitoring the DPLL_CORE clock and/or divider acknowledge signals according to new settings.
  7. The PRCM module clears the frequency update field.
  8. The PRCM module requests the GPMC to exit idle.
  9. The GPMC reallows interconnect connection and acknowledges it is functional.
  10. Accesses to external memory are serviced again.

  NOTE:
  - The frequency update field is the same as the one for the EMIF clock change. The same hardware in the PRCM module handles the frequency change of the L3, DDR_PHY, and DLL clocks.
  - If the GPMC supports on-the-fly L3 frequency change, then the CM_SHADOW_FREQ_CONFIG2[0] GPMC_FREQ_UPDATE bit can allow bypassing of the sequence.

- Software-controlled sequence:
  1. Software configures the PRCM module to disable the GPMC.
  2. The PRCM module requests idle to the GPMC.
  3. The GPMC requests disconnection of its interconnect port and completes all outstanding transactions.
  4. The GPMC acknowledges idle. Any access to GPMC is then stalled.
  5. Software programs the PRCM module to change L3 frequency and wait for L3 stabilization.
  6. Software configures the PRCM module to reenable the GPMC.
  7. The GPMC reallows interconnect connection and acknowledges it is functional.

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8. Accesses to external memory are serviced again.

3.8.7.3 CORE DVFS Versus Subsystem Functionality

3.8.7.3.1 Display Subsystem

The display subsystem is part of the CORE voltage domain. It has internal FIFOs that are sized to sustain a change of OPP on the CORE voltage domain with no DPLL relock and no DLL frequency change. Accesses to external SDRAM are stalled for a maximum of 2 µs in these conditions. The display subsystem functional clock is not affected by the change of OPP on the CORE voltage domain. Therefore, the display subsystem supports on-the-fly DVFS of the CORE voltage domain, assuming the selected OPP remains compatible with the current display subsystem processing.

3.8.7.3.2 IVA

IVA is part of the MM voltage domain. It can sustain a temporary stall of external SDRAM accesses because it is not real-time processing. The IVA functional clock is not affected by the change of OPP on the CORE voltage domain; therefore, IVA supports on-the-fly DVFS of the CORE voltage domain.

3.8.7.3.3 Imaging Subsystem

The imaging subsystem (ISS) is part of the CORE voltage domain. It is real-time processing (or data flow). It cannot support a 2-µs stall of external SDRAM access, because of the heavy data throughput (FIFO size increase is prohibitive). As a consequence, the ISS does not support on-the-fly change of OPP on the CORE voltage domain. However, the CORE DVFS can be synchronized to the interframe idle window of the ISS. During this window, the ISS does not initiate a transaction to external SDRAM. The CORE OPP can be changed safely assuming the selected OPP remains compatible with the current ISS processing. The ISS functional clock frequency can remain unchanged or be scaled according to the OPP change, assuming it remains compatible with the current ISS processing. This is the responsibility of software.

Software performs the OPP change: OPP_LOW → OPP_NOM: The ISS/IPU primary functional clock is now running at 400 MHz, software sets the ISS clock divider to 4, and the ISS functional clock is back at 100 MHz.

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3.9 Device Low-Power States

The device low-power states are the result of any valid combination of power domain states in which all the power domains are no longer in ACTIVE state. In such a situation the PRCM module hardware can trigger events to further lower the consumption of the device and the system.

Typically, the PRCM module can lower or even turn off the SMPS, shut down the system clock supplier, and allow the external power IC to turn off its internal resources.

These device low-power states are characterized by the system power consumption, wake-up latency, and required functionality.

The low-power states are:

- RETENTION: All logic voltage domains (VDD_MPU_L, VDD_MM_L, and VDD_CORE_L) are in RETENTION state.
- LOW POWER: Any combination of logic voltage domain states (SLEEP or RETENTION) other than those previously identified.

Once the PRCM module hardware detects any valid combination of power domain states, and if a proper programming model of the PRCM module is set, the PRCM module automatically triggers the transition into the device low-power mode.

3.9.1 Device Wake-Up Source Summary

Each power domain in the device may contain modules that can generate wake-up events. Modules in the other power domains require that their voltage domain be in RETENTION, SLEEP, or ON state to generate a wake-up event. Some modules may have a further constraint that their power domain must be in ON-INACTIVE or CSWR RETENTION state to generate a wake-up event.

The wake-up events can be asynchronous or synchronous. Synchronous wake-up events require the 32-kHz clock or the system clock to be active, while asynchronous wake-up events do not require an active clock.

The *Modules Attributes* subsection of each clock domain in Section 3.6, *Clock Management Functional Description*, describes the wake-up capability support for each module of the corresponding power domain.

While the device is in STANDBY mode, additional asynchronous wakeup events from other domains are able to wake up the device.

Table 3-304 identifies which modules in which power domains can be configured to generate a wake-up while the device is in a low-power mode.

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Table 3-304. Wake-Up Sources During Device Low Power Mode

Device Power Mode	VDD_CORE state	VDD_MPU state	VDD_MM state	Domain able to generate wakeup	Wakeup source
STANDBY	Any combination of RET or SLEEP state			PD_ABE[1]	DMIC, McASP, WD_TIMER3
					McBSP1, McBSP2, McBSP3
					McPDM
				PD_CORE	IPU[2][3]
					DMA_SYSTEM[2][3]
					[1][4]
					GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8
					I2C1, I2C2, I2C3, I2C4, I2C5
					MCSPI1, MCSPI2, MCSPI3, MCSPI4
					MMC3, MMC4, MMC5
					UART1, UART2, UART3, UART4, UART5, UART6
				PD_L3_INIT[1]	MMC1, MMC2
					HSI[4], IEEE1500_2_OCP[3]
					SATA[4]
					USB_OTG_SS
					USB_HOST_HS, USB_TLL_HS
				PD_MPU	MPU[2][3]
				PD_DSP	DSP[2][3]
				PD_WKUPAON	GPIO1
					TIMER1, TIMER12
					PRM interrupt request towards MPU, IPU, or DSP
				PD_EMU	Any FORCEACTIVE directive
					Dynamic depedency towards L3_MAIN_2

(1) Only modules able to generate asynchronous wake-up have to be taken into account, and only when domain is in INACT or CSWRET state.
(2) True in every domain power state
(3) These modules have master wake-up (mwakeup) capability.
(4) These modules have both master wake-up and slave wake-up capability.

3.9.2 Device RETENTION State Management

In RETENTION state, the voltages to the device are lowered to their minimum value to retain only the logic build with RFFs, while all DFF logic is lost. The memory area may be retained, depending on the software configuration.

The device integrates enhanced device wake-up management while in RETENTION state. This allows:

- Triggering wakeup with limited capabilities from almost all programmed input pads around the device

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- Triggering wakeup with full capabilities by using few GPIO inputs in the PD_WKUPAON power domain

The logic voltages VDD_CORE_L, VDD_MPU_L, and VDD_MM_L can transition to their retention value independently. Once the voltage domain state transition conditions are met in compliance with the software configuration, the PRCM module hardware initiates the transition into RETENTION state by sending an I^2C command for the corresponding SMPS.

When all the logic voltages are transitioned to their RETENTION state, the PRCM module hardware can, depending on a software configuration, toggle its system clock request and/or its power request to allow the SCRM to shut down the system clock source and to request the external power IC to shut down internal resources.

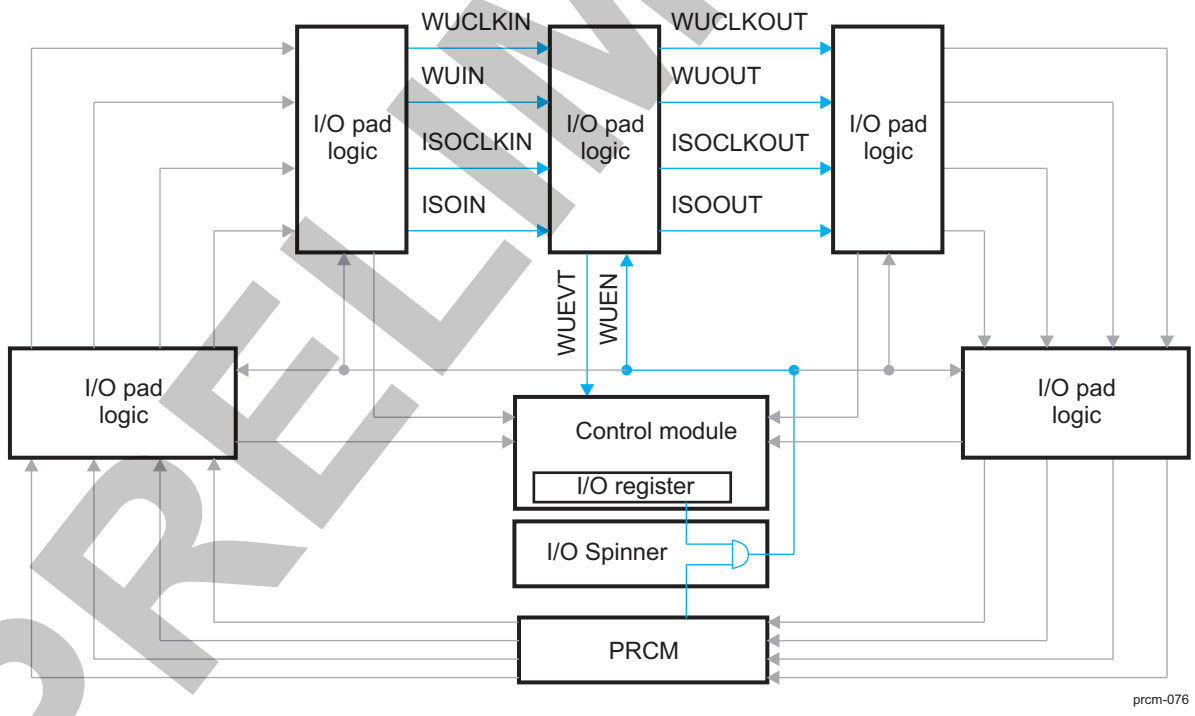
The PRCM module, SCRM, and the external power IC can also be programmed so that the voltage VDD_CORE_L is managed by the power request signal. This means:

- The power IC manages the ramp-down and ramp-up time of the VDD_CORE_L SMPS when the power request is toggled.
- The SCRM accounts for the overall setup of the PMIC resources (internal PMIC resources and VDD_CORE_L SMPS).
- The PRCM module sends RETENTION and ON commands through the I^2C interface. The value of the RETENTION voltage must be equal to the value of the current voltage, and the value of the ON voltage must be set to the expected voltage value following the wakeup. Also, the setup time periods corresponding to the SMPS ramp up and ramp down must be set to 0.

3.9.3 I/O Management

Figure 3-82 is an overview of the power-management modules and their internal connections with a generic power domain.

Figure 3-82. I/O Pads Daisy-Chain Configuration



The I/O pad logic at the two ends of the chain is connected to the PRM.

The I/O pad wake-up scheme must be enabled (WUEN signal) globally by setting the PRM_IO_PMCTRL[16] GLOBAL_WUEN bit and by also setting the I/O pad wake-up enabled/disabled individually (WUEN signal) by writing to the following bits in the control module:

- CONTROL.CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y[14] X_WAKEUPENABLE

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- CONTROL.CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y[30] Y_WAKEUPENABLE

Once configured, the wake-up scheme within each I/O pad is enabled and disabled by triggering a control (WUCLKIN signal) of the I/O daisy chain. This is done through the PRM_IO_PMCTRL[8] WUCLK_CTRL bit. Software must enable the I/O wakeup before entering low-power mode and must disable it following a wake-up event.

Setting the PRM_IO_PMCTRL[8] WUCLK_CTRL bit to 1 asserts the WUCLKIN signal high to reset spurious wake-up event and to latch the current pad input value. The PRM_IO_PMCTRL[9] WUCLK_STATUS bit logs the WUCLKOUT signal of the last pad of the I/O ring. When this status is set to 1, software can clear the PRM_IO_PMCTRL[8] WUCLK_CTRL bit to effectively enable or disable the wake-up feature within each pad.

Additionally, it is required that WUCLKIN is forced to 1 during global POR. The I/O wake-up feature is enabled or disabled depending on a control (WUEN) for each I/O pad. This control is generated by the SPINNER logic resulting from the combination of a local enable/disable bit per pad in the control module and a global enable/disable bit in the PRCM module (that is, the PRM_IO_PMCTRL[16] GLOBAL_WUEN bit).

When a wake-up event is detected by a wakeup-enabled I/O pad in the daisy chain, it is logged within the I/O and is conveyed to the system control module (WUEVT signal). All the I/O wake-up event statuses are mapped on memory-mapped registers in the system control module.

When the device wakes up, the MPU can determine all sources of the current wake-up event logged into the following corresponding bits in the control module:

- CONTROL.CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y[15] X_WAKEUPEVENT
- CONTROL.CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y[31] Y_WAKEUPEVENT

For information about the control module, see Chapter 18, *Control Module*.

3.9.3.1 Hardware-Controlled I/O Isolation Sequences

I/Os have two buffers: 1.2 V and 1.8 V.

The software configuration determines whether the 1.2-V buffer or the 1.8-V buffer is used.

3.9.3.2 Software-Controlled I/O Isolation

In addition to the hardware-controlled I/O transitions, the PRM_IO_PMCTRL[0] ISOCLK_OVERRIDE bit can be used by software to force the ISOCLKIN signal to the I/O pad. It is then propagated from one pad to the other in the wake-up enabled daisy chain of I/Os. The PRM_IO_PMCTRL[1] ISOCLK_STATUS bit logs the ISOCLKOUT signal of the last pad of the I/O daisy chain.

NOTE: Override must be used at boot time only when software must change the mode of an I/O from 1.8-V default mode to 1.2-V mode. When not overridden, this signal is controlled only by hardware.

The PRM_IO_PMCTRL[4] ISOOVR_EXTEND bit allows extending the non-EMIF I/O isolation. This feature can be used by software to restore modules driving output, such as GPIO, while non-EMIF I/Os are still isolated. Once software completes the relevant module restore, it clears the bit and hardware performs full-isolation-to-EMIF on the hardware-controlled I/O transition.

The PRM_IO_PMCTRL[5] IO_ON_STATUS bit is available for software to check completion of the EMIF on transition.

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3.10 PRCM Module Programming Guide

3.10.1 DPLLs Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

3.10.1.1 Global Initialization

3.10.1.1.1 Surrounding Module Global Initialization

This section identifies the requirements for initializing the surrounding modules when the module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DPLLs.

Table 3-305 describes the global initialization of the surrounding modules.

Table 3-305. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Ensure that the DPLL reference clock (gated version of system clock) is active.

3.10.1.1.2 DPLL Global Initialization

3.10.1.1.2.1 Main Sequence – DPLL Global Initialization

This procedure initializes the DPLL after a POR or software reset and then locks it to the desired synthesized clock frequency.

Table 3-306. DPLL Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure SSC parameters.	See Section 3.10.1.1.2.2.	
Configure recalibration parameters.	See Section 3.10.1.1.2.3.	
Set DPLL automatic idle mode.	CM_AUTOIDLE_<DPLL name>[2:0] AUTO_DPLL_MODE	xx(1)
Configure synthesized clock parameters.	See Section 3.10.1.1.2.4.	
Configure output clocks parameters.	See Section 3.10.1.1.2.5.	
Lock DPLL.	CM_CLKMODE_<DPLL name>[2:0] DPLL_EN	0x7

(1) It depends on the desired auto idle mode. See Section 3.6.3.3.3, *DPLL Power Modes*.

3.10.1.1.2.2 Subsequence – SSC Parameter Configuration

This procedure configures the SSC parameters for the DPLL and enables the SSC feature.

Table 3-307. DPLL SSC Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Configure M Step Size.	CM_SSC_DELTAMSTEP_<DPLL name>[19:0] DELTAMSTEP	xx(1)
Configure modulation frequency divider exponent part.	CM_SSC_MODFREQDIV_<DPLL name>[10:8] MODFREQDIV_EXPONENT	xx(1)
Configure modulation frequency divider mantissa part.	CM_SSC_MODFREQDIV_<DPLL name>[6:0] MODFREQDIV_MANTISSA	xx(1)
Enable/disable frequency downspread.	CM_CLKMODE_<DPLL name>[14] DPLL_SSC_DOWNSPREAD	xx(2)

(1) See the SSC description in Section 3.6.3.3.5, *DPLL Spread Spectrum Clocking*.
(2) The selected value depends on the desired SSC feature settings.

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Table 3-307. DPLL SSC Parameter Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Enable SSC feature.	CM_CLKMODE_<DPLL name>[12] DPLL_SSC_EN	0x1
Wait until SSC start acknowledge.	CM_CLKMODE_<DPLL name>[13] DPLL_SSC_ACK	0x1

3.10.1.1.2.3 Subsequence – Recalibration Parameter Configuration

This procedure enables the recalibration feature and the associated processor interrupt flag.

Table 3-308. DPLL Recalibration Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Clear recalibration interrupt status.	PRM_IRQSTATUS _<Processor name>[x] <DPLL name>_RECAL_ST	0x0
Unmask recalibration interrupt flag.	PRM_IRQENABLE _<Processor name>[x] <DPLL name>_RECAL_EN	0x1
Enable recalibration feature.	CM_CLKMODE_<DPLL name>[8] DPLL_DRIFTGUARD_EN	0x1

3.10.1.1.2.4 Subsequence – Synthesized Clock Parameter Configuration

This procedure configures the settings for the synthesized clock of the DPLL.

Table 3-309. DPLL Synthesized Clock Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Set DPLL clock synthesis multiplier.	CM_CLKSEL_<DPLL name>[18:8] DPLL_MULT	xx(1)
Set DPLL clock synthesis divider.	CM_CLKSEL_<DPLL name>[6:0] DPLL_DIV	xx(1)
IF : Low-power mode operation conditions satisfied?	Software test condition. See Section 3.6.3.3.2.	
Enable DPLL low-power operation mode.	CM_CLKMODE_<DPLL name>[10] DPLL_LPMODE_EN	0x1
ENDIF		

(1) It depends on the desired synthesized clock frequency. See Section 3.6.3.3, *Generic DPLL Overview*.

3.10.1.1.2.5 Subsequence – Output Clock Parameter Configuration

This procedure configures the settings for the output clocks of the DPLL.

Table 3-310. DPLL Output Clock Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Set output clock dividers (that is, M2, M3, and Hmn), where m is 1 or 2, and n is from 1 to 4. It depends on the available clock output of the DPLL.	CM_DIV_M2_<DPLL name>[4:0] DIVHS CM_DIV_M3_<DPLL name>[4:0] DIVHS CM_DIV_Hmn_<DPLL name>[5:0] DIVHS	xx(1)

(1) It depends on the desired output clock frequency. See Section 3.6.3.3, *Generic DPLL Overview*.

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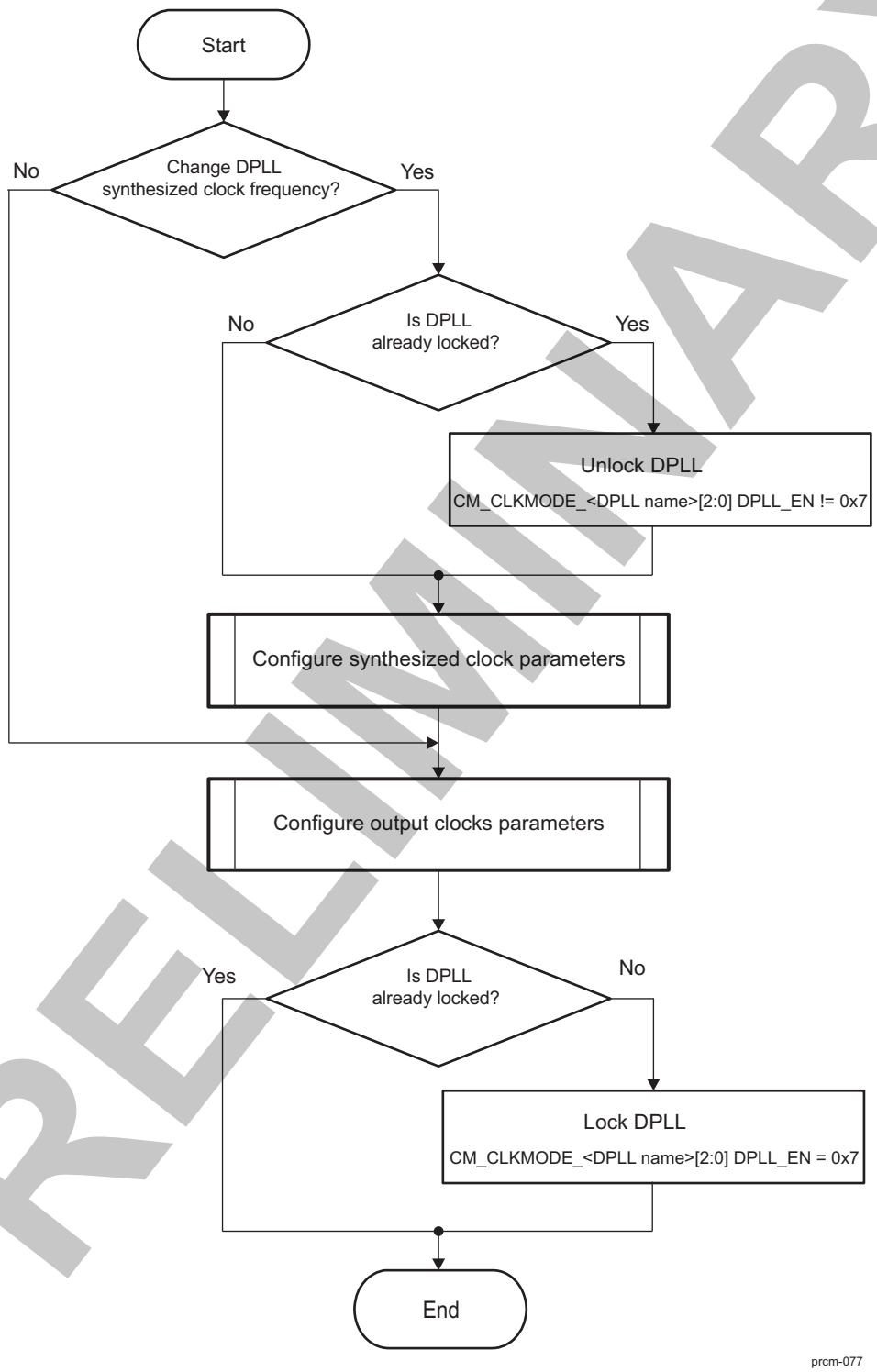
3.10.1.2 DPLL Output Frequency Change

Figure 3-83 shows the DPLL output-frequency change.

Figure 3-83. DPLL Output-Frequency Change



To unlock a DPLL, a mode different from the Lock Mode (0x7) should be programmed in the CM_CLKMODE_<DPLL NAME>[2:0] DPLL_EN bit field. The modes that can be programmed in the DPLL_EN bit field and can unlock the DPLL are:

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- For type A DPLLs: Idle Low Power bypass mode (0x5) and Idle Fast Relock bypass mode (0x6)
- For type B DPLLs: Low Power Stop mode (0x1) and Idle Low Power bypass mode (0x5)

Table 3-311 and Table 3-312 summarize register and subprocess call sequences for DPLL output frequency changes.

Table 3-311. Register Call Summary for Sequence – DPLL Output Frequency Change

Register Name
CM_CLKMODE_DPLL name

Table 3-312. Subprocess Call Summary for Sequence – DPLL Output Frequency Change

Subprocess Name	Cross-Reference
Configure synthesized clock parameters.	See Section 3.10.1.1.2.4.
Configure output clocks parameters.	See Section 3.10.1.1.2.5.

3.10.2 Clock Management Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the clocks in the device.

3.10.2.1 Global Initialization

3.10.2.1.1 Surrounding Module Global Initialization

This section identifies the requirements for initializing the surrounding modules when the module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DPLLs.

Table 3-313 describes the global initialization of the surrounding modules.

Table 3-313. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM DPLLs	Ensure that the DPLLS managed by the PRCM module are initialized.

3.10.2.1.2 Clock Management Global Initialization

3.10.2.1.2.1 Main Sequence – Clock Domain Global Initialization

This procedure initializes the clock domain of the device after a POR or software reset.

Table 3-314. Clock Domain Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure module clock-management feature of master modules in the clock domain.	<Module name>_SYSCONFIG[x] MIDLEMODE <Module name>_SYSCONFIG[x] STANDBYMODE	xx(1)
Configure module clock-management feature of slave modules in the clock domain.	See Section 3.10.3.3.	
Enable/disable static sleep dependency with other clock domains (that is, destination clock domains). Not all dependencies are configurable.	CM_<Clock Domain name>_STATICDEP[x] <Destination Clock Domain name>_STATDEP	0x0: Disable 0x1: Enable
Set dynamic dependency window size.	CM_<Clock Domain name>_DYNAMICDEP[27:24] WINDOWSIZE	xx(2)

(1) See the module register for valid modes.
(2) It depends on the desired size of the window. See Section 3.1.1.1.7.2, *Clock Domain Dependency*.

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Table 3-314. Clock Domain Global Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Enable/disable module wake-up dependency for the modules of the clock domain. It is available when the module can generate an interrupt or a DMA request to a service provider module (for example, a processor or DMA).	PM_<Clock Domain name>_<Module name>_WKDEP[x] WKUPDEP_<Module name>_<DMA/IRQ reques>t_<DMA/Processor name>	0x0: Disable 0x1: Enable
Set clock domain state transition feature.	CM_<Clock Domain name>_CLKSTCTRL[1:0] CLKTRCTRL	xx(3)

(3) It depends on the desired state of the clock domain. See Table 3-11.

3.10.2.1.2.2 Subsequence – Slave Module Clock-Management Parameters Configuration

This procedure configures the SSC parameters for the DPLL and enables the SSC feature.

Table 3-315. Slave Module Clock-Management Parameter Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module idle mode feature.	<Module name>_SYSCONFIG[x] SIDLEMODE <Module name>_SYSCONFIG[x] IDLEMODE	xx(1)
IF : Smart-idle mode is selected	<Module name>_SYSCONFIG[x] SIDLEMODE <Module name>_SYSCONFIG[x] IDLEMODE	0x10
Configure module clock requirement feature.	<Module name>_SYSCONFIG[x] CLOCKACTIVITY	x(1)
ENDIF		
Configure module management behavior on the PRCM module side.	CM_<Clock Domain name>_<Module name>_CLKCTRL[1:0] MODULEMODE	xx(2)

(1) See the module register for valid settings.
(2) The selected value depends on the desired clock-management behavior.

3.10.2.2 Clock Domain Sleep Transition and Troubleshooting

This procedure initiates a sleep transition on a clock domain and allows debugging if the transition does not occur.

Table 3-316. Clock Domain Sleep Transition and Troubleshooting

Step	Register/Bit Field/Programming Model	Value
Set clock domain sleep transition state.	CM_<Clock Domain name>_CLKSTCTRL[1:0] CLKTRCTRL	0x1: SW_SLEEP 0x3: HW_AUTO
IF : Clock domain sleep transition not initiated?		
Check that all clock domain master modules are in standby mode.	CM_<Clock Domain name>_<Module name>_CLKCTRL[18] STBYST	0x1: Module in standby
Check that all clock domain slave modules are in idle mode.	CM_<Clock Domain name>_<Module name>_CLKCTRL[17:16] IDLEST	0x1: In transition 0x2: Interface clock idled 0x3: Module idled
ENDIF		

3.10.2.3 Enable/Disable Software-Programmable Static Dependency

To change the setting of a software-programmable static dependency, use the procedure described in Table 3-317.

Table 3-317. Enable/Disable Software-Programmable Static Dependency

Step	Register/Bit Field/Programming Model	Value
Force destination domain to be awake (SW_WKUP).	CM_<Dest_CDname>_CLKSTCTRL[1:0] CLKTRCTRL	0x2

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Table 3-317. Enable/Disable Software-Programmable Static Dependency (continued)

Step	Register/Bit Field/Programming Model	Value
Wait until power domain that encloses the destination domain is ON.	PM_<Dest_PDname>_PWRSTST	=0x3
Change the static dependency.	CM_<Src_CDname>_STATICDEP[x] Dest_CDname_STATDEP	0x1
Put destination domain back to automatic transition (HW_AUTO).	CM_<Dest_CDname> _CLKSTCTRL[1:0] CLKTRCTRL	0x3

3.10.3 Power Management Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and control of the power domain in the device.

3.10.3.1 Global Initialization

3.10.3.1.1 Surrounding Module Global Initialization

Initialization of any surrounding modules within the device is not required. The external power IC and the device clocks should be active.

3.10.3.1.2 Power Management Global Initialization

3.10.3.1.2.1 Main Sequence – Power Domain Global Initialization and Setting

This procedure initializes the power domain of the device after a POR or software reset.

Table 3-318. Power Domain Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure memory area power state when the power domain is on. Not all memory area states are programmable.	PM_<Power Domain name>_PWRSTCTRL[x] <Memory Bank name>_ONSTATE	0x1: RETAINED 0x3: ON
Configure memory area power state when the power domain transitions to RETENTION state. Not all memory area states are programmable.	PM_<Power Domain name>_PWRSTCTRL[x] <Memory Bank name>_RETSTATE	0x1: RETAINED
Configure logic area RETENTION power state when the power domain transitions to RETENTION state.	PM_<Power Domain name>_PWRSTCTRL[2] LOGICRETSTATE	0x1: CSWR
Select target power state of the power domain. Not all states are programmable.	PM_<Power Domain name>_PWRSTCTRL[1:0] POWERSTATE	0x1: RETENTION 0x2: ON-INACTIVE 0x3: ON-ACTIVE
Wait until power state change is complete.	PM_<Power Domain name>_PWRSTST[1:0] POWERSTATEST	0x1: RETENTION 0x2: ON-INACTIVE 0x3: ON-ACTIVE

3.10.3.2 Forced Memory Area State Change With Power Domain ON

This procedure initiates a forced memory area state change while the power domain is ON.

Table 3-319. Forced Memory Area State Change With Power Domain ON

Step	Register/Bit Field/Programming Model	Value
Configure memory area target power state. Not all memory area states are programmable.	PM_<Power Domain name>_PWRSTCTRL[x] <Memory Bank name>_ONSTATE	0x1: RETAINED 0x3: ON
Get memory area current state.	PM_<Power Domain name>_PWRSTST[x] <Memory Bank name>_STATEST	0x1: RETAINED 0x3: ON

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3.10.3.3 Forced Power Domain Low-Power State Transition

This procedure initiates a power state transition on a power domain from current low-power state (ON-INACTIVE or RETENTION) to a lower power state (RETENTION).

Table 3-320. Forced Power Domain Low-Power State Transition

Step	Register/Bit Field/Programming Model	Value
Select target low-power state of the power domain. Not all states are programmable.	PM_<Power Domain name>_PWRSTCTRL[1:0] POWERSTATE	0x1: RETENTION
Force power domain low-power state transition.	PM_<Power Domain name>_PWRSTCTRL[4] LOWPOWERSTATECHANGE	0x1: Force change
Wait until state change is complete.	PM_<Power Domain name>_PWRSTCTRL[4] LOWPOWERSTATECHANGE	0x0: Change complete
Get current power state.	PM_<Power Domain name>_PWRSTST[1:0] POWERSTATEST	0x1: RETENTION

3.10.4 Voltage Management Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and management of the voltage domains of the device.

3.10.4.1 Global Initialization

3.10.4.1.1 Surrounding Module Global Initialization

Initialization of any surrounding modules within the device is not required. The external power IC and the device clocks should be active.

3.10.4.1.2 Voltage Management Global Initialization

3.10.4.1.2.1 Main Sequence – Voltage Management Global Initialization and Setting

This procedure initializes the voltage management framework in the device.

Table 3-321. Power Domain Global Initialization

Step	Register/Bit Field/Programming Model	Value
Initialize SmartReflex modules.	See Section 3.10.4.1.3.	
Initialize voltage processor modules.	See Section 3.10.4.1.4.	
Initialize voltage controller module.	See Section 3.10.4.1.5.	

3.10.4.1.3 SmartReflex Module Initialization

This procedure initializes the SmartReflex module.

Table 3-322. SmartReflex Module Configuration

Step	Register/Bit Field/Programming Model	Value
Configure clock.	See Section 3.10.4.1.3.1.	
Configure sensor.	See Section 3.10.4.1.3.2.	
Configure accumulator and minimum/maximum/average.	See Section 3.10.4.1.3.3.	
Configure error generator.	See Section 3.10.4.1.3.4.	
Configure interrupt generator.	See Section 3.10.4.1.3.5.	
Enable module.	SMARTREFLEXn.SRCONFIG[11] SRENABLE	0x1

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3.10.4.1.3.1 Subsequence – Clock Configuration

This procedure configures the clock for the SmartReflex module.

Table 3-323. SmartReflex Module Clock Configuration

Step	Register/Bit Field/Programming Model	Value
Configure desired clock frequency.	SMARTREFLEXn.SRCONFIG[21:12] SRCLKLENGTH	xx(1)
Configure desired idle mode.	SMARTREFLEXn.ERRCONFIG[25:24] IDLEMODE	0x0: Forced-idle 0x1: No-idle 0x2: Smart-idle 0x3: Smart-idle wakeup
Enable/disable wake-up feature.	SMARTREFLEXn.ERRCONFIG[26] WAKEUPENABLE	0x0: Disable 0x1: Enable
Enable clock.	CM_COREAON_ SMARTREFLEX_<SR name>_CLKCTRL[1:0] MODULEMODE	0x2: Enable

(1) See Equation 1 for clock frequency calculation.

3.10.4.1.3.2 Subsequence – Sensors Configuration

This procedure configures the sensors in the SmartReflex module.

Table 3-324. SmartReflex Module Sensors Configuration

Step	Register/Bit Field/Programming Model	Value
Enable SVT sensor core N.	SMARTREFLEXn.SRCONFIG[1] SENNENABLE	0x1
Enable SVT sensor core P.	SMARTREFLEXn.SRCONFIG[0] SENPENABLE	0x1
Enable SVT sensor core.	SMARTREFLEXn.SRCONFIG[10] SENENABLE	0x1
Enable LVT sensor core N.	SMARTREFLEXn.SRCONFIG[3] LVTSENNENABLE	0x1
Enable LVT sensor core P.	SMARTREFLEXn.SRCONFIG[2] LVTSENPENABLE	0x1
Enable LVT sensor core.	SMARTREFLEXn.SRCONFIG[4] LVTSENENABLE	0x1

3.10.4.1.3.3 Subsequence – Accumulator and Min/Max/Avg Configuration

This procedure configures the accumulator and minimum/maximum/average part of the SmartReflex module.

Table 3-325. Accumulator and Minimum/Maximum/Average Configuration

Step	Register/Bit Field/Programming Model	Value
Set size of the accumulator.	SMARTREFLEXn.SRCONFIG[31:22] ACCUMDATA	xxx(1)
Set average weight parameter for sensor A.	SMARTREFLEXn.AVGWEIGHT_REG[1:0] SENNAVGWEIGHT	x(1)
Set average weight parameter for sensor B.	SMARTREFLEXn.AVGWEIGHT_REG[3:2] SENPAVGWEIGHT	x(1)
Enable minimum/maximum/average.	SMARTREFLEXn.SRCONFIG[8] MINMAXAVGENABLE	0x1

(1) These parameters are calculated as given in Section 3.8.3.2.3, *SmartReflex Submodules*.

3.10.4.1.3.4 Subsequence – Error Generator Configuration

This procedure configures the error generator part of the SmartReflex module.

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Table 3-326. Error Generator Configuration

Step	Register/Bit Field/Programming Model	Value
Configure four reference value parameters for SVT sensor core.	SMARTREFLEXn.NVALUERECIPROCAL[23:20] SENPGAIN	x[1]
	SMARTREFLEXn.NVALUERECIPROCAL[19:16] SENNGAIN	x[1]
	SMARTREFLEXn.NVALUERECIPROCAL[15:8] SENPRN	xx[1]
	SMARTREFLEXn.NVALUERECIPROCAL[7:0] SENNRN	xx[1]
Configure four reference value parameters for LVT sensor core.	SMARTREFLEXn.LVTNVALUERECIPROCAL[23:20] SENPGAIN	x[1]
	SMARTREFLEXn.LVTNVALUERECIPROCAL[19:16] SENNGAIN	x[1]
	SMARTREFLEXn.LVTNVALUERECIPROCAL[15:8] SENPRN	xx[1]
	SMARTREFLEXn.LVTNVALUERECIPROCAL[7:0] SENNRN	xx[1]
Enable the error generator.	SMARTREFLEXn.SRCONFIG[9] ERRORGENERATORENABLE	0x1

(1) Configured according to the values read for the current operating voltage level from the control module register in Section 3.8.3.2.3, *SmartReflex Submodules*.

3.10.4.1.3.5 Subsequence – Interrupt Generator Configuration

This procedure configures the interrupt generator part of the SmartReflex module.

Table 3-327. Interrupt Generator Configuration

Step	Register/Bit Field/Programming Model	Value
Set the four reference value parameters.	SMARTREFLEXn.ERRCONFIG[18:16] ERRWEIGHT	x
	SMARTREFLEXn.ERRCONFIG[15:8] ERRMAXLIMIT	xx
	SMARTREFLEXn.ERRCONFIG[7:0] ERRMINLIMIT	xx
IF : Automatic voltage control using voltage processor	Software test condition	
Clear voltage processor bounds interrupt status.	SMARTREFLEXn.ERRCONFIG[23] VPBOUNDSINTSTATENA	0x1
Unmask voltage processor bounds interrupt.	SMARTREFLEXn.ERRCONFIG[22] VPBOUNDSINTENABLE	0x1
ELSE-IF : Software-controlled voltage management	Software test condition	
Unmask <processor> interrupt events.	SMARTREFLEXn.IRQENABLE_SET[3] MCUACCUMINTENASET	0x1
	SMARTREFLEXn.IRQENABLE_SET[2] MCUVALIDINTENASET	0x1
	SMARTREFLEXn.IRQENABLE_SET[1] MCUBOUNDSINTENASET	0x1
ENDIF		

3.10.4.1.4 Voltage Processor Initialization

This procedure initializes the voltage processor.

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Table 3-328. Voltage Processor Module Initialization

Step	Register/Bit Field/Programming Model	Value
Configure error-to-voltage converter.	See Section 3.10.4.1.4.1.	
Configure PRCM module.	See Section 3.10.4.1.4.2.	
Mask/unmask interrupt events.	PRCM.PRM_IRQENABLE_<Processor name>	
Enable module.	PRCM.PRM_<Voltage Processor name>_CONFIG[0] VPENABLE	0x1

3.10.4.1.4.1 Subsequence – Error-to-Voltage Converter Configuration

This procedure configures the error-to-voltage converter of the voltage processor.

Table 3-329. Error-to-Voltage Converter Configuration

Step	Register/Bit Field/Programming Model	Value
Set error offset. Offset value in the Error to Voltage converter (8-bit signed two's complement number)(1). The default value for ERROROFFSET is zero.	PRCM.PRM_<Voltage Processor name>_CONFIG[31:24] ERROROFFSET	xx(2)
Set error gain. Gain value in the Error to Voltage converter (8-bit signed two's complement number). ERRORGAIN = ((Error2voltageGAIN(3))*100/SMPSstepsize)	PRCM.PRM_<Voltage Processor name>_CONFIG[23:16] ERRORGAIN	xx(2)
Set SMPS negative voltage step slew rate (in number of cycles per SMPS step).	PRCM.PRM_<Voltage Processor name>_VSTEPMIN[23:8] SMPSWAITTIMEMIN	xx(2)
Set SMPS minimum voltage (VDD) step size. 0 ≤ ΔVdd(4) ≤ VStepMin	PRCM.PRM_<Voltage Processor name>_VSTEPMIN[7:0] VSTEPMIN	xx(2)
Set SMPS positive voltage step slew rate (in number of cycles per SMPS step).	PRCM.PRM_<Voltage Processor name>_VSTEPMAX[23:8] SMPSWAITTIMEMAX	xx(2)
Set SMPS maximum voltage (VDD) step size. ΔVDD(4) > VStepMax	PRCM.PRM_<Voltage Processor name>_VSTEPMAX[7:0] VSTEPMAX	xx(2)
Set SMPS minimum voltage level.	PRCM.PRM_<Voltage Processor name>_VLIMITTO[23:16] VDDMIN	xx(2)
Set SMPS maximum voltage level.	PRCM.PRM_<Voltage Processor name>_VLIMITTO[31:24] VDDMAX	xx(2)

(1) ErrorOffset is an 8-bit two's complement signed frequency error and adding 1-bit is equivalent to adding 0.79% to the frequency error.
(2) Depends on the characteristics of the SMPS
(3) Recommended value for Error2voltage gain is approximately 0.004V/% error.
(4) ΔVdd = (FreqError + ErrorOffset) * Error2VoltageGain. FreqError is a two complement value fixed-point fraction, MSB is a signed bit.

3.10.4.1.4.2 Subsequence – FSM Configuration

This procedure configures the FSM of the voltage processor.

Table 3-330. FSM Configuration

Step	Register/Bit Field/Programming Model	Value
Set maximum length of time to wait for the command acknowledge from the SMPS.	PRCM.PRM_<Voltage Processor name>_VLIMITTO[15:0] TIMEOUT	xxxx(1)
Set target initial voltage level of the SMPS.	PRCM.PRM_<Voltage Processor name>_CONFIG[15:8] INITVOLTAGE	xx
Assert the initial voltage into the voltage processor FSM.	PRCM.PRM_<Voltage Processor name>_CONFIG[2] INITVDD	0x1

(1) Depends on the characteristics of the SMPS

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3.10.4.1.5 Voltage Controller Initialization

This procedure initializes the voltage controller.

Table 3-331. Voltage Controller Module Initialization

Step	Register/Bit Field/Programming Model	Value
Configure external power IC device I^2C slave addresses. 7 bits for each SMPS IC: [20:14] SMPS2, [13:7] SMPS1, [6:0] SMPS0.	PRCM.PRM_VC_SMPS_<Memory Volatge Domain>_CONFIG[6:0] SA_<Voltage Domain name>	xx(1)
Configure voltage configuration register addresses for the VDD channels. Voltage values – 8 bits for each SMPS IC: [23:16] SMPS2, [15:8] SMPS1, [7:0] SMPS0..	PRCM.PRM_VC_SMPS_<Memory Volatge Domain>_CONFIG[15:8] VOLRA_<Voltage Domain name>	xx(1)
Configure command configuration register addresses. Command (ON/ON-Low-Power/Retention). Command values – 8 bits for each SMPS IC: [23:16] SMPS2, [15:8] SMPS1, [7:0] SMPS0.	PRCM.PRM_VC_SMPS_<Memory Volatge Domain>_CONFIG[23:16] CMDRA_<Voltage Domain name>	xx(1) (2)
Configure voltage domain command values. ON/ON-Low-Power/Retention, command values are 8 bits for each channel.	PRCM.PRM_VC_VAL_CMD_<Voltage Domain name>[x] <Command name>	xx(1)
Configure pointers for the VDD channels.	See Section 3.10.4.1.5.1.	
Configure I^2C interface.	See Section 3.10.4.1.5.2.	

(1) Depends on the connectivity characteristics of the external SMPS device. For more information, see the corresponding SMPS reference documents.

(2) Second register address values are useful when the SMPS ICs have different configuration registers to switch ON or OFF, then VDD voltage configuration register.

3.10.4.1.5.1 Subsequence – VDD Channel Pointer Configuration

This procedure configures the FSM of the voltage processor.

Table 3-332. VDD Channel Pointer Configuration

Step	Register/Bit Field/Programming Model	Value
Set slave address pointer for each VDD channel (1 bit per VDD channel) – (0) VDD0, (1) VDD1, (2) VDD2.	PRCM.PRM_VC_SMPS_<Memory Voltage Domain>_CONFIG[24] SEL_SA_<Voltage Domain name>	
Set voltage configuration register address pointer for each VDD channel (1 bit per VDD channel) – (0) VDD0, (1) VDD1, (2)VDD2.	PRCM.PRM_VC_SMPS_<Memory Voltage Domain>_CONFIG[25] RAV_<Voltage Domain name>	
Set command (ON/Retention) configuration register address pointer for each VDD channel (1 bit per VDD channel) – (0) VDD0, (1) VDD1, (2) VDD2.	PRCM.PRM_VC_SMPS_<Memory Voltage Domain>_CONFIG[26] RAC_<Voltage Domain name>	
Select voltage or command configuration register for FSM commands. Enables bits for PIREGSCHRAC usage (1 bit per VDD channel) – (0) VDD0, (1) VDD1, (2) VDD2.	PRCM.PRM_VC_SMPS_<Memory Voltage Domain>_CONFIG[27] RACEN_<Voltage Domain name>	
Set command voltage level selection pointer. ON/ONLP/RET voltage values set selection for each VDD channel (1 bit per VDD channel) (2) VDD2, (1) VDD1, (0) VDD0.	PRCM.PRM_VC_SMPS_<Memory Voltage Domain>_CONFIG[28] CMD_<Voltage Domain name>	

3.10.4.1.5.2 Subsequence – I^2C Configuration

This procedure configures the I^2C in the voltage controller.

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Table 3-333. I²C Configuration

Step	Register/Bit Field/Programming Model	Value
Enable/disable I²C bus double digital filter.	PRCM.PRM_VC_CFG_I2C_MODE[6] DFILTEREN	
Set master code value for I²C HS preamble.	PRCM.PRM_VC_CFG_I2C_MODE[2:0] HSMCODE	
Enable/disable I²C HS mode.	PRCM.PRM_VC_CFG_I2C_MODE[3] HSMODEEN	0x0: Disable 0x1: Enable
Enable/disable repeated start operation.	PRCM.PRM_VC_CFG_I2C_MODE[4] SRMODEEN	0x0: Disable 0x1: Enable

3.10.4.2 Disable Sequence for AVS (SmartReflex) and VP

3.10.4.2.1 Disable the Error Generator Module

This procedure disables the Error Genarator Module.

Table 3-334. Disable the Error Generator

Step	Register/Bit Field/Programming Model	Value
Disable the VP BOUND IRQ (1)	SMARTREFLEXn.ERRCONFIG[22] VPBOUNDSINTENABLE	0x0
Disable sensors	SMARTREFLEXn.SRCONFIG[10] SENENABLE	
Disable the Error Generator module	SMARTREFLEXn.SRCONFIG[9] ERRORGENERATORENABLE	

(1) At this stage, it is important to not write 0x1 on bit SMARTREFLEXn.ERRCONFIG[23] VPBOUNDSINTSTATENA

3.10.4.2.2 Disable the Voltage Processor

This procedure disables the Voltage Processor.

Table 3-335. Disable the Voltage Processor

Step	Register/Bit Field/Programming Model	Value
Disable the VP module	PRCM.PRM_<Voltage_Processor_name>_CONFIG[0] VPENABLE	0x0
Wait for VP being idled by pooling bit VPINIDLE to 0x1	PRCM.PRM_<Voltage_Processor_name>_STATUS[0] VPINIDLE	==0x1

3.10.4.2.3 Disable AVS (SmartReflex)

This procedure disables the Adaptive Voltage Scaling (AVS).

Table 3-336. Disable the SmartReflex Module

Step	Register/Bit Field/Programming Model	Value
Enable the MPU Disable Acknowledge IRQ	SMARTREFLEXn. IRQENABLE_SET[0] MCUDISABLEACTINTENASET	0x1
Disable the SmartReflex module	SMARTREFLEXn. SRCONFIG[11] SRENABLE	0x0
Clear the VP BOUND IRQ status bit only if it is set	SMARTREFLEXn. ERRCONFIG[23] VPBOUNDSINTSTATENA	0x1
Disable the following MPU IRQs or at least check these IRQs are not enabled: ACCUM IRQ, VALID IRQ and BOUND IRQ	SMARTREFLEXn. IRQENABLE_CLR[3] MCUACCUMINTENACLR SMARTREFLEXn. IRQENABLE_CLR[2] MCUVALIDINTENACLR SMARTREFLEXn. IRQENABLE_CLR[1] MCUBOUNDSINTENACLR	0x1
Clear the following MPU IRQ statuses: ACCUM IRQ, VALID IRQ and BOUND IRQ	SMARTREFLEXn. IRQSTATUS[3] MCUACCUMINTSTATENA SMARTREFLEXn. IRQSTATUS[2] MCUVALIDINTSTATENA SMARTREFLEXn. IRQSTATUS[1] MCUBOUNDSINTSTATENA	0x1

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Table 3-336. Disable the SmartReflex Module (continued)

Step	Register/Bit Field/Programming Model	Value
Wait for the MPU Disable Acknowledge IRQ	SMARTREFLEXn. IRQSTATUS[0] MCUDISABLEACKINTSTATENA	==0x1
Clear the MPU Disable Acknowledge IRQ status	SMARTREFLEXn. IRQSTATUS[0] MCUDISABLEACKINTSTATENA	0x1
Disable the MPU Disable Acknowledge IRQ status	SMARTREFLEXn. IRQENABLE_CLR[0] MCUDISABLEACKINTENACLR	0x1

3.10.4.3 Changing OPP

This procedure allows changing of the voltage of the external SMPS from one OPP to the other. It also covers the programming sequence for ABBLDO if the OPP change requires a change in state of the ABBLDO.

NOTE: When switching from the current OPP to a target OPP, if the clock frequency of the target OPP is less than that of the current OPP, the clock frequency is first switched to the lower frequency of the target OPP, and only then is voltage scaling initiated. However, if the clock frequency of the target OPP is greater than that of the current OPP, voltage scaling is initiated before frequency scaling.

In Table 3-337 and Table 3-338, "xxx" denotes MPU or MM.

Table 3-337. Transition From Nominal/Slow OPP to Fast OPP

Step ID	Step Description	Register/Register Bit Field/Programming Model	Value
1	Disable the SmartReflex module.	SMARTREFLEXn.SRCONFIG[11] SRENABLE and/or [10] SENENABLE	0x0
2	Mask SmartReflex interrupts		
3	Disable the voltage processor module	PRCM.PRM_<Voltage_Processor_Name>_CONFIG[0] VPENABLE	0x0
4	Set the new OPP – Fast OPP	PRCM.PRM_ABBLDO_xxx_CTRL[1:0] OPP_SEL	0x1
5	Set the voltage processor with new voltage level	PRCM.PRM_VP_xxx_CONFIG [15:8] INITVOLTAGE	
6	Triggers a write of the value in the INITVOLTAGE into the voltage processor	PRCM.PRM_<Voltage_Processor_Name>_CONFIG[2] INITVDD	0x1
7	Force update of the SMPS. This command is sent from the Voltage Processor to the Voltage controller. The Voltage controller sends the new voltage to the power IC via the I^2C Interface. In response the Power IC returns the "SMPS ACK" acknowledge signal to the Voltage controller via the I^2C interface.	PRCM.PRM_VP_xxx_CONFIG [1] FORCEUPDATE	0x1
8	The "SMPS ACK" response is then transmitted to the Voltage processor which will start the counter ForceUpdateWait.	PRCM.PRM_VP_xxx_VOLTAGE[31:8] FORCEUPDATEWAIT	
9	When ForceUpdateWait counter expires, VP_xxx_TRANXDONE_ST interrupt status is set.	PRM_IRQSTATUS_MPU and PRM_IRQSTATUS_MPU_2	0x1

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Table 3-337. Transition From Nominal/Slow OPP to Fast OPP (continued)

10	Initiate the state change for the ABB LDO	PRCM.PRM_ABBLDO_xxx_CTRL[2] OPP_CHANGE	0x1
11	ABB LDO performs its transition from bypass mode to FBB mode. The transition is complete when SR2_WTCNT_VALUE counter expires. When this counter expires, OPP_CHANGE bit is set to 0 and ABB_xxx_DONE_ST interrupt status is set.	PRCM.PRM_ABBLDO_xxx_SETUP PRCM.PRM_ABBLDO_xxx_CTRL PRM_IRQSTATUS_MPU PRM_IRQSTATUS_MPU_2	
12	Re-enable the SmartReflex module and interrupts	SMARTREFLEXn.SRCONFIG[11] SR_EN	0x1
13	Re-enable the voltage processor (via I^2C commands sent through the voltage controller)		

Table 3-338. Transition From Fast OPP to Nominal OPP

Step ID	Step Description	Register/Register Bit Field/Programming Model	Value
1	Disable the SmartReflex module.	SMARTREFLEXn.SRCONFIG[11] SRENABLE and/or [10] SENENABLE	0x0
2	Mask SmartReflex interrupts		
3	Disable the voltage processor module	PRCM.PRM_<Voltage_Processor_Name>_CONFIG[0] VPENABLE	0x0
4	Set the new OPP – Nominal OPP	PRM_ABBLDO_xxx_CTRL[1:0] OPP_SEL	0x2
5	Initiate the state change for the ABB LDO	PRM_ABBLDO_xxx_CTRL[2] OPP_CHANGE	0x1
6	ABB LDO performs its transition from FBB mode to bypass mode. The transition is complete when PRM_ABBLDO_xxx_SETUP. sr2_wtcnt_value counter expires. When this counter expires, OPP_CHANGE bit is set to 0 and ABB_xxx_DONE_ST interrupt status is set.	PRM_ABBLDO_xxx_SETUP PRM_ABBLDO_xxx_CTRL PRM_IRQSTATUS_MPU PRM_IRQSTATUS_MPU_2	
7	Set the voltage processor with new voltage level.	PRCM.PRM_<Voltage_Processor_Name>_CONFIG[15:8] INITVOLTAGE	
8	Triggers a write of the value in the INITVOLTAGE into the voltage processor	PRCM.PRM_<Voltage_Processor_Name>_CONFIG[2] INITVDD	0x1
9	Force update of the SMPS. This command is sent from the Voltage Processor to the Voltage controller. The Voltage controller sends the new voltage to the power IC via the I^2C Interface. In response the Power IC returns the "SMPS ACK" acknowledge signal to the Voltage controller via the I^2C interface.	PRM_VP_xxx_CONFIG[1] FORCEUPDATE	0x1
10	The "SMPS ACK" response is then transmitted to the Voltage processor which will start the counter ForceUpdateWait.	PRM_VP_xxx_VOLTAGE[31:8] FORCEUPDATEWAIT	
11	When ForceUpdateWait counter expires, VP_xxx_TRANXDONE_ST interrupt status is set.	PRM_IRQSTATUS_MPU and PRM_IRQSTATUS_MPU_2	0x1

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Table 3-338. Transition From Fast OPP to Nominal OPP (continued)

12	Re-enable the SmartReflex module and interrupts	SRn.SRCONFIG[11] SR_EN	0x1
13	Re-enable the voltage processor (via I^2C commands sent through the voltage controller)		

When the SMPS ACK is received from the I^2C interface, this ACK signal sets the PRM_IRQSTATUS_MPU/PRM_IRQSTATUS_IPU[14] VC_BYPASS_ST interrupt status. When this interrupt is received, the software starts a counter. At the end of the counter, the VDD_xxx.L supply has reached its final state. Software must set the PRM_ABBLDO_xx_CTRL[2] OPP_CHANGE bit to initiate the state change for the ABB LDO. ABB LDO performs its transition from FBB mode to bypass mode. The transition is complete when the PRM_ABBLDO_xxx_SETUP[15:8] SR2_WTCNT_VALUE counter expires. When this counter expires, the PRM_ABBLDO_xxx_CTRL[2] OPP_CHANGE bit is set to 0, and the status of the ABB_xxx_DONE_ST interrupt is set.

3.11 PRCM Register Manual

3.11.1 PRM Instance Summary

Table 3-339. PRM Instance Summary

Module Name	Base Address	Size
OCP_SOCKET_PRM	0x4AE0 6000	256 bytes
CKGEN_PRM	0x4AE0 6100	256 bytes
MPU_PRM	0x4AE0 6300	256 bytes
DSP_PRM	0x4AE0 6400	256 bytes
ABE_PRM	0x4AE0 6500	256 bytes
COREAON_PRM	0x4AE0 6600	256 bytes
CORE_PRM	0x4AE0 6700	2816 bytes
IVA_PRM	0x4AE0 7200	256 bytes
CAM_PRM	0x4AE0 7300	256 bytes
DSS_PRM	0x4AE0 7400	256 bytes
GPU_PRM	0x4AE0 7500	256 bytes
L3INIT_PRM	0x4AE0 7600	256 bytes
CUSTEFUSE_PRM	0x4AE0 7700	256 bytes
WKUPAON_PRM	0x4AE0 7800	256 bytes
WKUPAON_CM	0x4AE0 7900	256 bytes
EMU_PRM	0x4AE0 7A00	256 bytes
EMU_CM	0x4AE0 7B00	256 bytes
DEVICE_PRM	0x4AE0 7C00	512 bytes
INSTR_PRM	0x4AE0 7F00	256 bytes

NOTE: The RW WSpecial type of access is used for bit fields that can be written by software and changed by hardware (for example, an automatically-cleared bit).

3.11.2 OCP_SOCKET_PRM Registers

3.11.2.1 OCP_SOCKET_PRM Register Summary

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Table 3-340. OCP_SOCKET_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	OCP_SOCKET_PRM Base Address
REVISION_PRM	R	32	0x0000 0000	0x4AE0 6000
PRM_IRQSTATUS_MPU	RW	32	0x0000 0010	0x4AE0 6010
PRM_IRQSTATUS_MPU_2	RW	32	0x0000 0014	0x4AE0 6014
PRM_IRQENABLE_MPU	RW	32	0x0000 0018	0x4AE0 6018
PRM_IRQENABLE_MPU_2	RW	32	0x0000 001C	0x4AE0 601C
PRM_IRQSTATUS_IPU	RW	32	0x0000 0020	0x4AE0 6020
PRM_IRQENABLE_IPU	RW	32	0x0000 0028	0x4AE0 6028
PRM_IRQSTATUS_DSP	RW	32	0x0000 0030	0x4AE0 6030
PRM_IRQENABLE_DSP	RW	32	0x0000 0038	0x4AE0 6038
CM_PRM_PROFILING_CLKCTRL	RW	32	0x0000 0040	0x4AE0 6040
PRM_DEBUG_CFG	RW	32	0x0000 0080	0x4AE0 6080

3.11.2.2 OCP_SOCKET_PRM Register Description

Table 3-341. REVISION_PRM

Address Offset	0x0000 0000		
Physical Address	0x4AE0 6000	**Instance**	OCP_SOCKET_PRM
Description	This register contains the IP revision code for the PRM part of the PRCM		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	Revision Number	R	0x- - TI Internal data

Table 3-342. Register Call Summary for Register REVISION_PRM

PRCM Register Manual
- OCP_SOCKET_PRM Register Summary: [0]

Table 3-343. PRM_IRQSTATUS_MPU

Address Offset	0x0000 0010		
Physical Address	0x4AE0 6010	**Instance**	OCP_SOCKET_PRM
Description	This register provides status on MPU interrupt events. Any event is logged independently of the corresponding IRQENABLE value. SW is required to clear a set bit by writing a '1' into the bit-position to be cleared.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABB_MM_DONE_ST	VC_MM_VPACK_ST	VP_MM_TRANXDONE_ST	VP_MM_EQVALUE_ST	VP_MM_NOSMPSACK_ST	VP_MM_MAXVDD_ST	VP_MM_MINVDD_ST	VP_MM_OPPCHANGEDONE_ST	RESERVED	VC_CORE_VPACK_ST	VP_CORE_TRANXDONE_ST	VP_CORE_EQVALUE_ST	VP_CORE_NOSMPSACK_ST	VP_CORE_MAXVDD_ST	VP_CORE_MINVDD_ST	VP_CORE_OPPCHANGEDONE_ST	RESERVED	VC_BYPASSACK_ST	VC_TOERR_ST	VC_RAERR_ST	VC_SAERR_ST	RESERVED	IO_ST	TRANSITION_ST	RESERVED			DPLL_ABE_RECAL_ST	DPLL_PER_RECAL_ST	DPLL_IVA_RECAL_ST	DPLL_MPU_RECAL_ST	DPLL_CORE_RECAL_ST

Bits	Field Name	Description	Type	Reset
31	ABB_MM_DONE_ST	MM ABB mode change done. This status is set when OPP_CHANGE bit is cleared by hardware in PRM_ABBLDO_MM_CRTL register. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
30	VC_MM_VPACK_ST	Voltage Controller MM voltage processor command acknowledge status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
29	VP_MM_TRANXDONE_ST	Voltage Processor MM transaction completion status. This status is set when a transaction is completed in the voltage processor. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
28	VP_MM_EQVALUE_ST	Voltage Processor MM voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
27	VP_MM_NOSMPSACK_ST	Voltage Processor MM timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
26	VP_MM_MAXVDD_ST	Voltage Processor MM voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
25	VP_MM_MINVDD_ST	Voltage Processor MM voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
24	VP_MM_OPPCHANGEDONE_ST	Voltage Processor MM OPP change done status, including ABB mode change done if applicable (OPP_CHANGE bit cleared in PRM_ABBLDO_MM_CRTL). It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
23	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
22	VC_CORE_VPACK_ST	Voltage Controller CORE voltage processor command acknowledge status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
21	VP_CORE_TRANXDONE_ST	Voltage Processor CORE transaction completion status. This status is set when a transaction is completed in the voltage processor. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
20	VP_CORE_EQVALUE_ST	Voltage Processor CORE voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
19	VP_CORE_NOSMPSACK_ST	Voltage Processor CORE timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
18	VP_CORE_MAXVDD_ST	Voltage Processor CORE voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
17	VP_CORE_MINVDD_ST	Voltage Processor CORE voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
16	VP_CORE_OPPCHANGEDONE_ST	Voltage Processor CORE OPP change done status. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
15	Reserved		R	0
14	VC_BYPASSACK_ST	Voltage Controller bypass command acknowledge status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
13	VC_TOERR_ST	Voltage Controller timeout error event status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
12	VC_RAERR_ST	Voltage Controller register address acknowledge error event status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
11	VC_SAERR_ST	Voltage Controller slave address acknowledge error event status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0x0
10	RESERVED		R	0
9	IO_ST	IO pad event interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
8	TRANSITION_ST	Software supervised transition completed event interrupt status (any domain). Asserted upon completion of any clock domain force wakeup transition or upon completion of any power domain sleep transition with at least one enclosed clock domain configured in forced-sleep. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
7:5	RESERVED		R	0x0
4	DPLL_ABE_RECAL_ST	ABE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
3	DPLL_PER_RECAL_ST	PER DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
2	DPLL_IVA_RECAL_ST	IVA DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
1	DPLL_MPU_RECAL_ST	MPU DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
0	DPLL_CORE_RECAL_ST	CORE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

Table 3-344. Register Call Summary for Register PRM_IRQSTATUS_MPU

Clock Management Functional Description
- DPLL Recalibration: [0]
- Recalibration: [1]
- Recalibration: [2]
- Recalibration: [3]
- Recalibration: [4]
- Recalibration: [5]

PRCM Module Programming Guide
- Changing OPP: [6] [7] [8] [9] [10]

PRCM Register Manual
- OCP_SOCKET_PRM Register Summary: [11]

Table 3-345. PRM_IRQSTATUS_MPU_2

Address Offset	0x0000 0014		
Physical Address	0x4AE0 6014	**Instance**	OCP_SOCKET_PRM
Description	This register provides status on MPU interrupt events. Any event is logged independently of the corresponding IRQENABLE value. SW is required to clear a set bit by writing a '1' into the bit-position to be cleared.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ABB_MPU_DONE_ST	VC_MPU_VPACK_ST	VP_MPU_TRANXDONE_ST	VP_MPU_EQVALUE_ST	VP_MPU_NOSMPSACK_ST	VP_MPU_MAXVDD_ST	VP_MPU_MINVDD_ST	VP_MPU_OPPCHANGEDONE_ST

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	ABB_MPU_DONE_ST	MPU ABB mode change done. This status is set when OPP_CHANGE bit is cleared by hardware in PRM_ABBLDO_MPU_CRTL register. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
6	VC_MPU_VPACK_ST	Voltage Controller MPU voltage processor command acknowledge status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
5	VP_MPU_TRANXDONE_ST	Voltage Processor MPU transaction completion status. This status is set when a transaction is completed in the voltage processor. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
4	VP_MPU_EQVALUE_ST	Voltage Processor MPU voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
3	VP_MPU_NOSMPSACK_ST	Voltage Processor MPU timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
2	VP_MPU_MAXVDD_ST	Voltage Processor MPU voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
1	VP_MPU_MINVDD_ST	Voltage Processor MPU voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
0	VP_MPU_OPPCHANGEDONE_ST	Voltage Processor MPU OPP change done status, including ABB mode change done if applicable (OPP_CHANGE bit cleared in PRM_ABBLDO_MPU_CRTL). It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Table 3-346. Register Call Summary for Register PRM_IRQSTATUS_MPU_2

PRCM Module Programming Guide
- Changing OPP: [0] [1] [2] [3]

PRCM Register Manual
- OCP_SOCKET_PRM Register Summary: [4]

Table 3-347. PRM_IRQENABLE_MPU

Address Offset	0x0000 0018
Physical Address	0x4AE0 6018 **Instance** OCP_SOCKET_PRM
Description	This register is used to enable or disable MPU interrupt activation upon presence of corresponding IRQSTATUS bit.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABB_MM_DONE_EN	VC_MM_VPACK_EN	VP_MM_TRANXDONE_EN	VP_MM_EQVALUE_EN	VP_MM_NOSMPSACK_EN	VP_MM_MAXVDD_EN	VP_MM_MINVDD_EN	VP_MM_OPPCHANGEDONE_EN	RESERVED	VC_CORE_VPACK_EN	VP_CORE_TRANXDONE_EN	VP_CORE_EQVALUE_EN	VP_CORE_NOSMPSACK_EN	VP_CORE_MAXVDD_EN	VP_CORE_MINVDD_EN	VP_CORE_OPPCHANGEDONE_EN	RESERVED	VC_BYPASSACK_EN	VC_TOERR_EN	VC_RAERR_EN	VC_SAERR_EN	RESERVED	IO_EN	TRANSITION_EN	RESERVED			DPLL_ABE_RECAL_EN	DPLL_PER_RECAL_EN	DPLL_IVA_RECAL_EN	DPLL_MPU_RECAL_EN	DPLL_CORE_RECAL_EN

Bits	Field Name	Description	Type	Reset
31	ABB_MM_DONE_EN	MM ABB mode change done enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
30	VC_MM_VPACK_EN	Voltage Controller MM voltage processor command acknowledge enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
29	VP_MM_TRANXDONE_EN	Voltage Processor MM transaction completion enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
28	VP_MM_EQVALUE_EN	Voltage Processor MM voltage value change event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
27	VP_MM_NOSMPSACK_EN	Voltage Processor MM timeout event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
26	VP_MM_MAXVDD_EN	Voltage Processor MM voltage higher limit event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
25	VP_MM_MINVDD_EN	Voltage Processor MM voltage lower limit event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
24	VP_MM_OPPCHANGEDONE_EN	Voltage Processor MM OPP change done enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
23	RESERVED		R	0
22	VC_CORE_VPACK_EN	Voltage Controller CORE voltage processor command acknowledge enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
21	VP_CORE_TRANXDONE_EN	Voltage Processor CORE transaction completion enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
20	VP_CORE_EQVALUE_EN	Voltage Processor CORE voltage value change event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
19	VP_CORE_NOSMPSACK_EN	Voltage Processor CORE timeout event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
18	VP_CORE_MAXVDD_EN	Voltage Processor CORE voltage higher limit event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
17	VP_CORE_MINVDD_EN	Voltage Processor CORE voltage lower limit event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
16	VP_CORE_OPPCHANGEDONE_EN	Voltage Processor CORE OPP change done enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
15	RESERVED		R	0
14	VC_BYPASSACK_EN	Voltage Controller bypass command acknowledge enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
13	VC_TOERR_EN	Voltage Controller timeout error event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
12	VC_RAERR_EN	Voltage Controller register address acknowledge error event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
11	VC_SAERR_EN	Voltage Controller slave address acknowledge error event enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0x0
10	RESERVED		R	0
9	IO_EN	IO pad event interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
8	TRANSITION_EN	Software supervised transition completed event interrupt enable (any domain). 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
7:5	RESERVED		R	0x0
4	DPLL_ABE_RECAL_EN	ABE DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
3	DPLL_PER_RECAL_EN	PER DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
2	DPLL_IVA_RECAL_EN	IVA DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1	DPLL_MPU_RECAL_EN	MPU DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
0	DPLL_CORE_RECAL_EN	CORE DPLL recalibration interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

Table 3-348. Register Call Summary for Register PRM_IRQENABLE_MPU

Clock Management Functional Description • DPLL Recalibration: [0] • Recalibration: [1] • Recalibration: [2] • Recalibration: [3] • Recalibration: [4] • Recalibration: [5]
Voltage-Management Functional Description • Voltage Processor Module: [6]
PRCM Register Manual • OCP_SOCKET_PRM Register Summary: [7]

Table 3-349. PRM_IRQENABLE_MPU_2

Address Offset	0x0000 001C		
Physical Address	0x4AE0 601C	**Instance**	OCP_SOCKET_PRM
Description	This register is used to enable or disable MPU interrupt activation upon presence of corresponding IRQSTATUS bit.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ABB_MPU_DONE_EN	VC_MPU_VPACK_EB	VP_MPU_TRANXDONE_EN	VP_MPU_EQVALUE_EN	VP_MPU_NOSMPSACK_EN	VP_MPU_MAXVDD_EN	VP_MPU_MINVDD_EN	VP_MPU_OPPCHANGEDONE_EN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x0000000
7	ABB_MPU_DONE_EN	MPU ABB mode change done enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
6	VC_MPU_VPACK_EB	Voltage Controller MPU voltage processor command acknowledge enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
5	VP_MPU_TRANXDONE_EN	Voltage Processor MPU transaction completion enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
4	VP_MPU_EQVALUE_EN	Voltage Processor MPU voltage value change event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
3	VP_MPU_NOSMPSACK_EN	Voltage Processor MPU timeout event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
2	VP_MPU_MAXVDD_EN	Voltage Processor MPU voltage higher limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1	VP_MPU_MINVDD_EN	Voltage Processor MPU voltage lower limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
0	VP_MPU_OPPCHANGEDONE_EN	Voltage Processor MPU OPP change done enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

Table 3-350. Register Call Summary for Register PRM_IRQENABLE_MPU_2

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- OCP_SOCKET_PRM Register Summary: [0]

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Table 3-351. PRM_IRQSTATUS_IPU

Address Offset	0x0000 0020		
Physical Address	0x4AE0 6020	**Instance**	OCP_SOCKET_PRM
Description	This register provides status on IPU interrupt events. Any event is logged independently of the corresponding IRQENABLE value. SW is required to clear a set bit by writing a '1' into the bit-position to be cleared.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABB_MM_DONE_ST	VC_MM_VPACK_ST	VP_MM_TRANXDONE_ST	VP_MM_EQVALUE_ST	VP_MM_NOSMPSACK_ST	VP_MM_MAXVDD_ST	VP_MM_MINVDD_ST	VP_MM_OPPCHANGEDONE_ST	RESERVED	VC_CORE_VPACK_ST	VP_CORE_TRANXDONE_ST	VP_CORE_EQVALUE_ST	VP_CORE_NOSMPSACK_ST	VP_CORE_MAXVDD_ST	VP_CORE_MINVDD_ST	VP_CORE_OPPCHANGEDONE_ST	RESERVED	VC_BYPASSACK_ST	VC_TOERR_ST	VC_RAERR_ST	VC_SAERR_ST	FORCEWKUP_ST	IO_ST	TRANSITION_ST	RESERVED			DPLL_ABE_RECAL_ST	DPLL_PER_RECAL_ST	DPLL_IVA_RECAL_ST	RESERVED	DPLL_CORE_RECAL_ST

Bits	Field Name	Description	Type	Reset
31	ABB_MM_DONE_ST	MM ABB mode change done. This status is set when OPP_CHANGE bit is cleared by hardware in PRM_ABBLDO_MM_CRTL register. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
30	VC_MM_VPACK_ST	Voltage Controller MM voltage processor command acknowledge status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
29	VP_MM_TRANXDONE_ST	Voltage Processor MM transaction completion status. This status is set when a transaction is completed in the voltage processor. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
28	VP_MM_EQVALUE_ST	Voltage Processor MM voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
27	VP_MM_NOSMPSACK_ST	Voltage Processor MM timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
26	VP_MM_MAXVDD_ST	Voltage Processor MM voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
25	VP_MM_MINVDD_ST	Voltage Processor MM voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
24	VP_MM_OPPCHANGEDONE_ST	Voltage Processor MM OPP change done status, including ABB mode change done if applicable (OPP_CHANGE bit cleared in PRM_ABBLDO_MM_CRTL). It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
23	RESERVED		R	0
22	VC_CORE_VPACK_ST	Voltage Controller CORE voltage processor command acknowledge status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
21	VP_CORE_TRANXDONE_ST	Voltage Processor CORE transaction completion status. This status is set when a transaction is completed in the voltage processor. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
20	VP_CORE_EQVALUE_ST	Voltage Processor CORE voltage value change event. This status is set when an update has been requested but the new voltage value is the same as the current SMPS voltage value. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
19	VP_CORE_NOSMPSACK_ST	Voltage Processor CORE timeout event status. This status is set when the timeout occured before the SMPS acknowledge. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
18	VP_CORE_MAXVDD_ST	Voltage Processor CORE voltage higher limit event status. This status is set when the voltage higher limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
17	VP_CORE_MINVDD_ST	Voltage Processor CORE voltage lower limit event status. This status is set when the voltage lower limit is reached. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
16	VP_CORE_OPPCHANGEDONE_ST	Voltage Processor CORE OPP change done status. It is cleared by SW. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
15	RESERVED		R	0
14	VC_BYPASSACK_ST	Voltage Controller bypass command acknowledge status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
13	VC_TOERR_ST	Voltage Controller timeout error event status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
12	VC_RAERR_ST	Voltage Controller register address acknowledge error event status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
11	VC_SAERR_ST	Voltage Controller slave address acknowledge error event status 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
10	FORCEWKUP_ST	IPU domain software supervised wakeup transition completed event interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
9	IO_ST	IO pad event interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
8	TRANSITION_ST	Software supervised transition completed event interrupt status (any domain). Asserted upon completion of any clock domain force wakeup transition or upon completion of any power domain sleep transition with at least one enclosed clock domain configured in forced-sleep. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
7:5	RESERVED		R	0x0
4	DPLL_ABE_RECAL_ST	ABE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
3	DPLL_PER_RECAL_ST	PER DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
2	DPLL_IVA_RECAL_ST	IVA DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
1	RESERVED		R	0
0	DPLL_CORE_RECAL_ST	CORE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0

Table 3-352. Register Call Summary for Register PRM_IRQSTATUS_IPU

Clock Management Functional Description • DPLL Recalibration: [0] • Recalibration: [1] • Recalibration: [2] • Recalibration: [3]
Voltage-Management Functional Description • Voltage Processor Module: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17]
PRCM Module Programming Guide • Changing OPP: [18]
PRCM Register Manual • OCP_SOCKET_PRM Register Summary: [19]

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Table 3-353. PRM_IRQENABLE_IPU

Address Offset	0x0000 0028		
Physical Address	0x4AE0 6028	**Instance**	OCP_SOCKET_PRM
Description	This register is used to enable or disable IPU interrupt activation upon presence of corresponding IRQSTATUS bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABB_MM_DONE_EN	VC_MM_VPACK_EN	VP_MM_TRANXDONE_EN	VP_MM_EQVALUE_EN	VP_MM_NOSMPSACK_EN	VP_MM_MAXVDD_EN	VP_MM_MINVDD_EN	VP_MM_OPPCHANGEDONE_EN	RESERVED	VC_CORE_VPACK_EN	VP_CORE_TRANXDONE_EN	VP_CORE_EQVALUE_EN	VP_CORE_NOSMPSACK_EN	VP_CORE_MAXVDD_EN	VP_CORE_MINVDD_EN	VP_CORE_OPPCHANGEDONE_EN	RESERVED	VC_BYPASSACK_EN	VC_TOERR_EN	VC_RAERR_EN	VC_SAERR_EN	FORCEWKUP_EN	IO_EN	TRANSITION_EN	RESERVED			DPLL_ABE_RECAL_EN	DPLL_PER_RECAL_EN	DPLL_IVA_RECAL_EN	RESERVED	DPLL_CORE_RECAL_EN

Bits	Field Name	Description	Type	Reset
31	ABB_MM_DONE_EN	MM ABB mode change done enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
30	VC_MM_VPACK_EN	Voltage Controller MM voltage processor command acknowledge enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
29	VP_MM_TRANXDONE_EN	Voltage Processor MM transaction completion enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
28	VP_MM_EQVALUE_EN	Voltage Processor MM voltage value change event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
27	VP_MM_NOSMPSACK_EN	Voltage Processor MM timeout event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
26	VP_MM_MAXVDD_EN	Voltage Processor MM voltage higher limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
25	VP_MM_MINVDD_EN	Voltage Processor MM voltage lower limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
24	VP_MM_OPPCHANGEDONE_EN	Voltage Processor MM OPP change done enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
23	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
22	VC_CORE_VPACK_EN	Voltage Controller CORE voltage processor command acknowledge enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
21	VP_CORE_TRANXDONE_EN	Voltage Processor CORE transaction completion enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
20	VP_CORE_EQVALUE_EN	Voltage Processor CORE voltage value change event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
19	VP_CORE_NOSMPSACK_EN	Voltage Processor CORE timeout event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
18	VP_CORE_MAXVDD_EN	Voltage Processor CORE voltage higher limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
17	VP_CORE_MINVDD_EN	Voltage Processor CORE voltage lower limit event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
16	VP_CORE_OPPCHANGEDONE_EN	Voltage Processor CORE OPP change done enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
15	RESERVED		R	0
14	VC_BYPASSACK_EN	Voltage Controller bypass command acknowledge enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
13	VC_TOERR_EN	Voltage Controller timeout error event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
12	VC_RAERR_EN	Voltage Controller register address acknowledge error event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
11	VC_SAERR_EN	Voltage Controller slave address acknowledge error event enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
10	FORCEWKUP_EN	IPU domain software supervised wakeup transition completed event interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
9	IO_EN	IO pad event interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
8	TRANSITION_EN	Software supervised transition completed event interrupt enable (any domain) 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	DPLL_ABE_RECAL_EN	ABEDPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
3	DPLL_PER_RECAL_EN	PER DPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
2	DPLL_IVA_RECAL_EN	IVA DPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1	RESERVED		R	0
0	DPLL_CORE_RECAL_EN	CORE DPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

Table 3-354. Register Call Summary for Register PRM_IRQENABLE_IPU

Clock Management Functional Description
- DPLL Recalibration: [0]
- Recalibration: [1]
- Recalibration: [2]
- Recalibration: [3]

Voltage-Management Functional Description
- Voltage Processor Module: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]

PRCM Register Manual
- OCP_SOCKET_PRM Register Summary: [19]

Table 3-355. PRM_IRQSTATUS_DSP

Address Offset	0x0000 0030		
Physical Address	0x4AE0 6030	**Instance**	OCP_SOCKET_PRM
Description	This register provides status on DSP interrupt events. Any event is logged independently of the corresponding IRQENABLE value. SW is required to clear a set bit by writing a '1' into the bit-position to be cleared.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					FORCEWKUP_ST	RESERVED					DPLL_ABE_RECAL_ST	RESERVED	DPLL_IVA_RECAL_ST	RESERVED	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	FORCEWKUP_ST	DSP domain software supervised wakeup transition completed event interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
9:5	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
4	DPLL_ABE_RECAL_ST	ABE DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
3	RESERVED		R	0
2	DPLL_IVA_RECAL_ST	IVA DPLL recalibration interrupt status. 0x0: No interrupt 0x1: Interrupt is pending	RW W1toClr	0
1:0	RESERVED		R	0x0

Table 3-356. Register Call Summary for Register PRM_IRQSTATUS_DSP

Clock Management Functional Description
- DPLL Recalibration: [0]

PRCM Register Manual
- OCP_SOCKET_PRM Register Summary: [1]

Table 3-357. PRM_IRQENABLE_DSP

Address Offset	0x0000 0038		
Physical Address	0x4AE0 6038	**Instance**	OCP_SOCKET_PRM
Description	This register is used to enable or disable DSP interrupt activation upon presence of corresponding IRQSTATUS bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					FORCEWKUP_EN	RESERVED						DPLL_ABE_RECAL_EN	RESERVED	DPLL_IVA_RECAL_EN	RESERVED		

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	FORCEWKUP_EN	DSP domain software supervised wakeup transition completed event interrupt enable. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
9:5	RESERVED		R	0x00
4	DPLL_ABE_RECAL_EN	ABEDPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
3	RESERVED		R	0
2	DPLL_IVA_RECAL_EN	IVA DPLL recalibration interrupt enable 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1:0	RESERVED		R	0x0

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Table 3-358. Register Call Summary for Register PRM_IRQENABLE_DSP

Clock Management Functional Description
- DPLL Recalibration: [0]

PRCM Register Manual
- OCP_SOCKET_PRM Register Summary: [1]

Table 3-359. CM_PRM_PROFILING_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4AE0 6040	**Instance**	OCP_SOCKET_PRM
Description	This register manages the WKUPAON_PROFILING_GCLK clock. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status Read 0x0: Module is fully functional Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle Read 0x3: Module is disabled	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. INTRCONN configuration port is not accessible. 0x1: Module is managed automatically by HW along with EMU domain. INTRCONN configuration port is accessible only when EMU domain is on. 0x2: Reserved 0x3: Reserved	RW	0x0

Table 3-360. Register Call Summary for Register CM_PRM_PROFILING_CLKCTRL

PRCM Register Manual
- OCP_SOCKET_PRM Register Summary: [0]

Table 3-361. PRM_DEBUG_CFG

Address Offset	0x0000 0080		
Physical Address	0x4AE0 6080	**Instance**	OCP_SOCKET_PRM
Description	This register is used to configure the PRM's 32-bit debug output. There is one 7-bit source select field for selecting from a shared set of 8-bit internal signal blocks per byte. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3								SEL2								SEL1								SEL0							

Bits	Field Name	Description	Type	Reset
31:24	SEL3	Internal signal block select for debug word byte-3	RW	0x03
23:16	SEL2	Internal signal block select for debug word byte-2	RW	0x02
15:8	SEL1	Internal signal block select for debug word byte-1	RW	0x01
7:0	SEL0	Internal signal block select for debug word byte-0	RW	0x00

Table 3-362. Register Call Summary for Register PRM_DEBUG_CFG

PRCM Register Manual
- OCP_SOCKET_PRM Register Summary: [0]

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3.11.3 CKGEN_PRM Registers

3.11.3.1 CKGEN_PRM Register Summary

Table 3-363. CKGEN_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_PRM Base Address
CM_CLKSEL_ABE_DSS_SYS	RW	32	0x0000 0000	0x4AE0 6100
CM_CLKSEL_WKUPAON	RW	32	0x0000 0008	0x4AE0 6108
CM_CLKSEL_ABE_PLL_REF	RW	32	0x0000 000C	0x4AE0 610C
CM_CLKSEL_SYS	RW	32	0x0000 0010	0x4AE0 6110

3.11.3.2 CKGEN_PRM Register Description

Table 3-364. CM_CLKSEL_ABE_DSS_SYS

Address Offset	0x0000 0000		
Physical Address	0x4AE0 6100	**Instance**	CKGEN_PRM
Description	Select the SYS_CLK for ABE and DSS subsystems. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKSEL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CLKSEL	Selects the divider value 0x0: Select SYS_CLK divided by 1 0x1: Select SYS_CLK divided by 2. Must be used for SYS_CLK > 26MHz	RW	0

Table 3-365. Register Call Summary for Register CM_CLKSEL_ABE_DSS_SYS

Clock Management Functional Description
- PRM Clock Source: [0]

PRCM Register Manual
- CKGEN_PRM Register Summary: [1]

Table 3-366. CM_CLKSEL_WKUPAON

Address Offset	0x0000 0008		
Physical Address	0x4AE0 6108	**Instance**	CKGEN_PRM
Description	Control the functional clock source of the WKUPAON, PRM and Smart Reflex functional clock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKSEL

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CLKSEL	Select the clock source for WKUPAON_ICLK and for ABE_DPLL_BYPASS_CLK clocks. 0x0: Selects SYS_CLK for WKUPAON_ICLK Selects SYS_CLK for ABE_DPLL_BYPASS_CLK 0x1: Selects ABE_LP_CLK for WKUPAON_ICLK Selects FUNC_32K_CLK for ABE_DPLL_BYPASS_CLK	RW	0

Table 3-367. Register Call Summary for Register CM_CLKSEL_WKUPAON

Clock Management Functional Description • PRM Clock Source: [0] [1]
PRCM Register Manual • CKGEN_PRM Register Summary: [2]

Table 3-368. CM_CLKSEL_ABE_PLL_REF

Address Offset	0x0000 000C		
Physical Address	0x4AE0 610C	**Instance**	CKGEN_PRM
Description	Control the source of the reference clock for DPLL_ABE		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKSEL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CLKSEL	Select the source for the DPLL_ABE reference clock. 0x0: Selects SYS_CLK 0x1: Selects SYS_32K	RW	1

Table 3-369. Register Call Summary for Register CM_CLKSEL_ABE_PLL_REF

Clock Management Functional Description • PRM Clock Source: [0]
PRCM Register Manual • CKGEN_PRM Register Summary: [1]

Table 3-370. CM_CLKSEL_SYS

Address Offset	0x0000 0010		
Physical Address	0x4AE0 6110	**Instance**	CKGEN_PRM
Description	Software sets the SYS_CLK configuration corresponding to the frequency of SYS_CLK. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SYS_CLKSEL	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	SYS_CLKSEL	System clock input selection. 0x0: Uninitialized 0x1: Input clock is 12 MHz 0x2: reserved 0x3: Input clock is 16.8 MHz 0x4: Input clock is 19.2 MHz 0x5: Input clock is 26 MHz 0x6: reserved 0x7: Input clock is 38.4 MHz	RW	0x0

Table 3-371. Register Call Summary for Register CM_CLKSEL_SYS

PRCM Register Manual
- CKGEN_PRM Register Summary: [0]

3.11.4 MPU_PRM Registers

3.11.4.1 MPU_PRM Register Summary

Table 3-372. MPU_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MPU_PRM Base Address
PM_MPU_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 6300
PM_MPU_PWRSTST	RW	32	0x0000 0004	0x4AE0 6304
RM_MPU_MPU_CONTEXT	RW	32	0x0000 0024	0x4AE0 6324

3.11.4.2 MPU_PRM Register Description

Table 3-373. PM_MPU_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 6300	**Instance**	MPU_PRM
Description	This register controls the MPU domain power state to reach upon a domain sleep transition. If the value programmed in this register correspond to a lower power state than the one programmed in MPU SS for CPU0 and/or CPU1, then value of this register is overwritten in PRCM logic to limit the power state to enter. Even if value of this register is overwitten in PRCM logic, value of this register remains unchanged.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MPU_L2_ONSTATE				RESERVED						MPU_L2_RETSTATE	RESERVED				LOWPOWERSTATECHANGE	RESERVED	LOGICRETSTATE	POWERSTATE	

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x003
19:18	MPU_L2_ONSTATE	MPU_L2 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
17:10	RESERVED		R	0x01
9	MPU_L2_RETSTATE	MPU_L2 memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
8:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change.	R	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1
1:0	POWERSTATE	Power state control. 0x0: reserved 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

Table 3-374. Register Call Summary for Register PM_MPU_PWRSTCTRL

Power Management Functional Description
- Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5] [6]
- Power State Override: [7] [8] [9] [10]

PRCM Register Manual
- MPU_PRM Register Summary: [11]

Table 3-375. PM_MPU_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 6304	**Instance**	MPU_PRM
Description	This register provides a status on the MPU domain current power state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LASTPOWERSTATEENTERED			RESERVED				INTRANSITION	RESERVED								MPU_L2_STATEST		RESERVED			LOGICSTATEST	POWERSTATEST	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Reserved	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:8	RESERVED		R	0x003
7:6	MPU_L2_STATEST	MPU_L2 memory state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
5:3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-376. Register Call Summary for Register PM_MPU_PWRSTST

Power Management Functional Description • Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5]
PRCM Register Manual • MPU_PRM Register Summary: [6]

Table 3-377. RM_MPU_MPU_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 6324	**Instance**	MPU_PRM
Description	This register contains dedicated MPU context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						LOSTMEM_MPU_L2	RESERVED							LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000001
9	LOSTMEM_MPU_L2	Specify if memory-based context in MPU_L2 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of MPU_MA_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of MPU_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-378. Register Call Summary for Register RM_MPU_MPU_CONTEXT

Power Management Functional Description • PD_MPU Description: [0] [1]
PRCM Register Manual • MPU_PRM Register Summary: [2]

3.11.5 DSP_PRM Registers

3.11.5.1 DSP_PRM Register Summary

Table 3-379. DSP_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSP_PRM Base Address
PM_DSP_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 6400
PM_DSP_PWRSTST	RW	32	0x0000 0004	0x4AE0 6404
RM_DSP_RSTCTRL	RW	32	0x0000 0010	0x4AE0 6410
RM_DSP_RSTST	RW	32	0x0000 0014	0x4AE0 6414
RM_DSP_DSP_CONTEXT	RW	32	0x0000 0024	0x4AE0 6424

3.11.5.2 DSP_PRM Register Description

Table 3-380. PM_DSP_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 6400	**Instance**	DSP_PRM
Description	This register controls the DSP power state to reach upon a domain sleep transition		
Type	RW		

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31 30 29 28 27 26 25 24	23 22	21 20	19 18	17 16	15 14 13 12 11	10	9	8	7 6 5	4	3	2	1 0
RESERVED		DSP_EDMA_ONSTATE	DSP_L2_ONSTATE	DSP_L1_ONSTATE	RESERVED	DSP_EDMA_RETSTATE	DSP_L2_RETSTATE	DSP_L1_RETSTATE	RESERVED	LOWPOWERSTATECHANGE	RESERVED	LOGICRETSTATE	POWERSTATE

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:20	DSP_EDMA_ONSTATE	DSP_EDMA state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
19:18	DSP_L2_ONSTATE	DSP_L2 state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
17:16	DSP_L1_ONSTATE	DSP_L1 state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:11	RESERVED		R	0x00
10	DSP_EDMA_RETSTATE	DSP_EDMA state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R	1
9	DSP_L2_RETSTATE	DSP_L2 state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
8	DSP_L1_RETSTATE	DSP_L2 state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1
1:0	POWERSTATE	Power state control 0x0: Reserved 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

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Table 3-381. Register Call Summary for Register PM_DSP_PWRSTCTRL

Power Management Functional Description

- Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5] [6] [7] [8]

PRCM Register Manual

- DSP_PRM Register Summary: [9]

Table 3-382. PM_DSP_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 6404	**Instance**	DSP_PRM
Description	This register provides a status on the DSP domain current power state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LASTPOWERSTATEENTERED		RESERVED		INTRANSITION		RESERVED								DSP_EDMA_STATEST		DSP_L2_STATEST		DSP_L1_STATEST		RESERVED		LOGICSTATEST		POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Reserved	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:10	RESERVED		R	0x000
9:8	DSP_EDMA_STATEST	DSP_EDMA memory state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	DSP_L2_STATEST	DSP_L2 memory state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3

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Bits	Field Name	Description	Type	Reset
5:4	DSP_L1_STATEST	DSP_L1 memory state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-383. Register Call Summary for Register PM_DSP_PWRSTST

Power Management Functional Description
- Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5] [6]

PRCM Register Manual
- DSP_PRM Register Summary: [7]

Table 3-384. RM_DSP_RSTCTRL

Address Offset	0x0000 0010		
Physical Address	0x4AE0 6410	**Instance**	DSP_PRM
Description	This register controls the release of the DSP sub-system resets.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														RST_DSP_MMU_CACHE	RST_DSP

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	RST_DSP_MMU_CACHE	DSP MMU, cache and slave interface reset control 0x0: Reset is cleared for the MMU, cache and slave interface 0x1: Reset is asserted for the MMU, cache and slave interface	RW	1
0	RST_DSP	DSP reset control 0x0: Reset is cleared for the DSP 0x1: Reset is asserted for the DSP	RW	1

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Table 3-385. Register Call Summary for Register RM_DSP_RSTCTRL

Reset Management Functional Description

- Reset Domains: [0] [1] [2] [3]
- DSP Subsystem Power-On Reset Sequence: [4] [5]
- DSP Subsystem Software Warm Reset Sequence: [6] [7] [8] [9]

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- DSP_PRM Register Summary: [10]

Table 3-386. RM_DSP_RSTST

Address Offset	0x0000 0014		
Physical Address	0x4AE0 6414	**Instance**	DSP_PRM
Description	This register logs the different reset sources of the DSP domain. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												RST_DSP_EMU_REQ	RST_DSP_EMU	RST_DSP_MMU_CACHE	RST_DSP

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	RST_DSP_EMU_REQ	DSP processor has been reset due to DSP emulation reset request driven from DSP SS 0x0: No emulation reset 0x1: DSP has been reset upon emulation reset request	RW W1toClr	0
2	RST_DSP_EMU	DSP domain has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: DSP has been reset upon emulation reset	RW W1toClr	0
1	RST_DSP_MMU_CACHE	DSP MMU, cache and slave interface SW reset status 0x0: No SW reset occured 0x1: MMU, cache and slave interface has been reset upon SW reset	RW W1toClr	0
0	RST_DSP	DSP SW reset 0x0: No SW reset occured 0x1: DSP has been reset upon SW reset	RW W1toClr	0

Table 3-387. Register Call Summary for Register RM_DSP_RSTST

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- DSP_PRM Register Summary: [0]

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Table 3-388. RM_DSP_DSP_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 6424	**Instance**	DSP_PRM
Description	This register contains dedicated DSP context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					LOSTMEM_DSP_EDMA	LOSTMEM_DSP_L2	LOSTMEM_DSP_L1	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	LOSTMEM_DSP_EDMA	Specify if memory-based context in DSP_EDMA memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
9	LOSTMEM_DSP_L2	Specify if memory-based context in DSP_L2 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8	LOSTMEM_DSP_L1	Specify if memory-based context in DSP_L1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSP_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSP_SYS_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-389. Register Call Summary for Register RM_DSP_DSP_CONTEXT

Power Management Functional Description
- PD_DSP Description: [0] [1]

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- DSP_PRM Register Summary: [2]

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3.11.6 ABE_PRM Registers

3.11.6.1 ABE_PRM Register Summary

Table 3-390. ABE_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ABE_PRM Base Address
PM_ABE_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 6500
PM_ABE_PWRSTST	RW	32	0x0000 0004	0x4AE0 6504
RM_ABE_AESS_CONTEXT	RW	32	0x0000 002C	0x4AE0 652C
PM_ABE_MCPDM_WKDEP	RW	32	0x0000 0030	0x4AE0 6530
RM_ABE_MCPDM_CONTEXT	RW	32	0x0000 0034	0x4AE0 6534
PM_ABE_DMIC_WKDEP	RW	32	0x0000 0038	0x4AE0 6538
RM_ABE_DMIC_CONTEXT	RW	32	0x0000 003C	0x4AE0 653C
PM_ABE_MCASP_WKDEP	RW	32	0x0000 0040	0x4AE0 6540
RM_ABE_MCASP_CONTEXT	RW	32	0x0000 0044	0x4AE0 6544
PM_ABE_MCBSP1_WKDEP	RW	32	0x0000 0048	0x4AE0 6548
RM_ABE_MCBSP1_CONTEXT	RW	32	0x0000 004C	0x4AE0 654C
PM_ABE_MCBSP2_WKDEP	RW	32	0x0000 0050	0x4AE0 6550
RM_ABE_MCBSP2_CONTEXT	RW	32	0x0000 0054	0x4AE0 6554
PM_ABE_MCBSP3_WKDEP	RW	32	0x0000 0058	0x4AE0 6558
RM_ABE_MCBSP3_CONTEXT	RW	32	0x0000 005C	0x4AE0 655C
RESERVED	R	32	0x0000 0060	0x4AE0 6560
RESERVED	R	32	0x0000 0064	0x4AE0 6564
PM_ABE_TIMER5_WKDEP	RW	32	0x0000 0068	0x4AE0 6568
RM_ABE_TIMER5_CONTEXT	RW	32	0x0000 006C	0x4AE0 656C
PM_ABE_TIMER6_WKDEP	RW	32	0x0000 0070	0x4AE0 6570
RM_ABE_TIMER6_CONTEXT	RW	32	0x0000 0074	0x4AE0 6574
PM_ABE_TIMER7_WKDEP	RW	32	0x0000 0078	0x4AE0 6578
RM_ABE_TIMER7_CONTEXT	RW	32	0x0000 007C	0x4AE0 657C
PM_ABE_TIMER8_WKDEP	RW	32	0x0000 0080	0x4AE0 6580
RM_ABE_TIMER8_CONTEXT	RW	32	0x0000 0084	0x4AE0 6584
PM_ABE_WD_TIMER3_WKDEP	R	32	0x0000 0088	0x4AE0 6588
RM_ABE_WD_TIMER3_CONTEXT	RW	32	0x0000 008C	0x4AE0 658C

3.11.6.2 ABE_PRM Register Description

Table 3-391. PM_ABE_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 6500	**Instance**	ABE_PRM
Description	This register controls the ABE domain power state to reach upon a domain sleep transition		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PERIPHMEM_ONSTATE		RESERVED		AESSMEM_ONSTATE		RESERVED					PERIPHMEM_RETSTATE	RESERVED	AESSMEM_RETSTATE	RESERVED			LOWPOWERSTATECHANGE	RESERVED	LOGICRETSTATE	POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:20	PERIPHMEM_ONSTATE	PERIPHMEM memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
19:18	RESERVED		R	0x0
17:16	AESSMEM_ONSTATE	AESSMEM memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:11	RESERVED		R	0x00
10	PERIPHMEM_RETSTATE	PERIPHMEM memory state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
9	RESERVED		R	0
8	AESSMEM_RETSTATE	AESSMEM memory state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R	1
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION Read 0x0: Whole logic is off when the domain is in RETENTION state.	R	0
1:0	POWERSTATE	Power state control 0x0: Reserved 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-392. Register Call Summary for Register PM_ABE_PWRSTCTRL

Power Management Functional Description
- Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5] [6]

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- ABE_PRM Register Summary: [7]

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Table 3-393. PM_ABE_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 6504	**Instance**	ABE_PRM
Description	This register provides a status on the ABE domain current power domain state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED										PERIPHMEM_STATEST		RESERVED		AESSMEM_STATEST		RESERVED		LOGICSTATEST		POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Reserved	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:10	RESERVED		R	0x000
9:8	PERIPHMEM_STATEST	PERIPHMEM memory state status Read 0x0: Reserved Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	RESERVED		R	0x0
5:4	AESSMEM_STATEST	AESSMEM memory state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1

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Bits	Field Name	Description	Type	Reset
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-394. Register Call Summary for Register PM_ABE_PWRSTST

Power Management Functional Description • Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5]
PRCM Register Manual • ABE_PRM Register Summary: [6]

Table 3-395. RM_ABE_AESS_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4AE0 652C	**Instance**	ABE_PRM
Description	This register contains dedicated AESS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_AESSMEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_AESSMEM	Specify if memory-based context in AESSMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-396. Register Call Summary for Register RM_ABE_AESS_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

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Table 3-397. PM_ABE_MCPDM_WKDEP

Address Offset	0x0000 0030		
Physical Address	0x4AE0 6530	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on McPDM service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_MCPDM_DMA_SDMA	WKUPDEP_MCPDM_DMA_DSP	RESERVED			WKUPDEP_MCPDM_IRQ_DSP	RESERVED	WKUPDEP_MCPDM_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_MCPDM_DMA_SDMA	Wakeup dependency from McPDM module (SWakeup_dma signal) towards DMA_SYSTEM + L3_MAIN2 + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_MCPDM_DMA_DSP	Wakeup dependency from McPDM module (SWakeup_dma signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5:3	RESERVED		R	0x0
2	WKUPDEP_MCPDM_IRQ_DSP	Wakeup dependency from McPDM module (SWakeup_irq signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_MCPDM_IRQ_MPU	Wakeup dependency from McPDM module (SWakeup_irq signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-398. Register Call Summary for Register PM_ABE_MCPDM_WKDEP

Clock Management Functional Description
- Wake-Up Dependency: [0] [1] [2] [3]

PRCM Register Manual
- ABE_PRM Register Summary: [4]

Table 3-399. RM_ABE_MCPDM_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4AE0 6534	**Instance**	ABE_PRM
Description	This register contains dedicated McPDM context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LOSTMEM_PERIHPMEM	RESERVED						LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-400. Register Call Summary for Register RM_ABE_MCPDM_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-401. PM_ABE_DMIC_WKDEP

Address Offset	0x0000 0038		
Physical Address	0x4AE0 6538	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on DMIC service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_DMIC_DMA_SDMA	WKUPDEP_DMIC_DMA_DSP	RESERVED			WKUPDEP_DMIC_IRQ_DSP	RESERVED	WKUPDEP_DMIC_IRQ_MPU

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_DMIC_DMA_SDMA	Wakeup dependency from DMIC module (SWakeup_dma signal) towards DMA_SYSTEM + L3_MAIN2 + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_DMIC_DMA_DSP	Wakeup dependency from DMIC module (SWakeup_dma signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5:3	RESERVED		R	0x0
2	WKUPDEP_DMIC_IRQ_DSP	Wakeup dependency from DMIC module (SWakeup_irq signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_DMIC_IRQ_MPU	Wakeup dependency from DMIC module (SWakeup_irq signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-402. Register Call Summary for Register PM_ABE_DMIC_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2] [3]
PRCM Register Manual • ABE_PRM Register Summary: [4]

Table 3-403. RM_ABE_DMIC_CONTEXT

Address Offset	0x0000 003C		
Physical Address	0x4AE0 653C	**Instance**	ABE_PRM
Description	This register contains dedicated DMIC context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_PERIHPMEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-404. Register Call Summary for Register RM_ABE_DMIC_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-405. PM_ABE_MCASP_WKDEP

Address Offset	0x0000 0040		
Physical Address	0x4AE0 6540	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on MCASP service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_MCASP1_DMA_SDMA	WKUPDEP_MCASP1_DMA_DSP	RESERVED			WKUPDEP_MCASP1_IRQ_DSP	RESERVED	WKUPDEP_MCASP1_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	WKUPDEP_MCASP_DMA_SDMA	Wakeup dependency from MCASP module (SWakeup_dma signal) towards DMA_SYSTEM + L3_MAIN2 + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_MCASP_DMA_DSP	Wakeup dependency from MCASP module (SWakeup_dma signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5:3	RESERVED		R	0x0
2	WKUPDEP_MCASP_IRQ_DSP	Wakeup dependency from MCASP module (SWakeup_irq signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
0	WKUPDEP_MCASP_IRQ_MPU	Wakeup dependency from MCASP module (SWakeup_irq signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-406. Register Call Summary for Register PM_ABE_MCASP_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2] [3]
PRCM Register Manual • ABE_PRM Register Summary: [4]

Table 3-407. RM_ABE_MCASP_CONTEXT

Address Offset	0x0000 0044		
Physical Address	0x4AE0 6544	**Instance**	ABE_PRM
Description	This register contains dedicated MCASP context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-408. Register Call Summary for Register RM_ABE_MCASP_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-409. PM_ABE_MCBSP1_WKDEP

Address Offset	0x0000 0048		
Physical Address	0x4AE0 6548	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on MCBSP1 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCBSP1_SDMA	WKUPDEP_MCBSP1_DSP	RESERVED	WKUPDEP_MCBSP1_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCBSP1_SDMA	Wakeup dependency from MCBSP1 module (SWakeup signal) towards DMA_SYSTEM + L3_MAIN2 + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MCBSP1_DSP	Wakeup dependency from MCBSP1 module (SWakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_MCBSP1_MPU	Wakeup dependency from MCBSP1 module (SWakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-410. Register Call Summary for Register PM_ABE_MCBSP1_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • ABE_PRM Register Summary: [3]

Table 3-411. RM_ABE_MCBSP1_CONTEXT

Address Offset	0x0000 004C		
Physical Address	0x4AE0 654C	**Instance**	ABE_PRM
Description	This register contains dedicated MCBSP1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LOSTMEM_PERIHPMEM	RESERVED						LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-412. Register Call Summary for Register RM_ABE_MCBSP1_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-413. PM_ABE_MCBSP2_WKDEP

Address Offset	0x0000 0050		
Physical Address	0x4AE0 6550	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on MCBSP2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCBSP2_SDMA	WKUPDEP_MCBSP2_DSP	RESERVED	WKUPDEP_MCBSP2_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCBSP2_SDMA	Wakeup dependency from MCBSP2 module (SWakeup signal) towards DMA_SYSTEM + L3_MAIN2 + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MCBSP2_DSP	Wakeup dependency from MCBSP2 module (SWakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
0	WKUPDEP_MCBSP2_MPU	Wakeup dependency from MCBSP2 module (SWakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-414. Register Call Summary for Register PM_ABE_MCBSP2_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • ABE_PRM Register Summary: [3]

Table 3-415. RM_ABE_MCBSP2_CONTEXT

Address Offset	0x0000 0054		
Physical Address	0x4AE0 6554	**Instance**	ABE_PRM
Description	This register contains dedicated MCBSP2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_PERIHPMEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-416. Register Call Summary for Register RM_ABE_MCBSP2_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

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Table 3-417. PM_ABE_MCBSP3_WKDEP

Address Offset	0x0000 0058		
Physical Address	0x4AE0 6558	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on MCBSP3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCBSP3_SDMA	WKUPDEP_MCBSP3_DSP	RESERVED	WKUPDEP_MCBSP3_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MCBSP3_SDMA	Wakeup dependency from MCBSP3 module (SWakeup signal) towards DMA_SYSTEM + L3_MAIN2 + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MCBSP3_DSP	Wakeup dependency from MCBSP3 module (SWakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_MCBSP3_MPU	Wakeup dependency from MCBSP3 module (SWakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-418. Register Call Summary for Register PM_ABE_MCBSP3_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • ABE_PRM Register Summary: [3]

Table 3-419. RM_ABE_MCBSP3_CONTEXT

Address Offset	0x0000 005C		
Physical Address	0x4AE0 655C	**Instance**	ABE_PRM
Description	This register contains dedicated MCBSP3 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_PERIHPMEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_PERIHPMEM	Specify if memory-based context in PERIHPMEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-420. Register Call Summary for Register RM_ABE_MCBSP3_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-421. PM_ABE_TIMER5_WKDEP

Address Offset	0x0000 0068		
Physical Address	0x4AE0 6568	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on TIMER5 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													WKUPDEP_TIMER5_DSP	RESERVED	WKUPDEP_TIMER5_MPU

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	WKUPDEP_TIMER5_DSP	Wakeup dependency from TIMER5 module (SWakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_TIMER5_MPU	Wakeup dependency from TIMER5 module (SWakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-422. Register Call Summary for Register PM_ABE_TIMER5_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • ABE_PRM Register Summary: [2]

Table 3-423. RM_ABE_TIMER5_CONTEXT

Address Offset	0x0000 006C		
Physical Address	0x4AE0 656C	**Instance**	ABE_PRM
Description	This register contains dedicated TIMER5 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-424. Register Call Summary for Register RM_ABE_TIMER5_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

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Table 3-425. PM_ABE_TIMER6_WKDEP

Address Offset	0x0000 0070		
Physical Address	0x4AE0 6570	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on TIMER6 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													WKUPDEP_TIMER6_DSP	RESERVED	WKUPDEP_TIMER6_MPU

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	WKUPDEP_TIMER6_DSP	Wakeup dependency from TIMER6 module (SWakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_TIMER6_MPU	Wakeup dependency from TIMER6 module (SWakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-426. Register Call Summary for Register PM_ABE_TIMER6_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • ABE_PRM Register Summary: [2]

Table 3-427. RM_ABE_TIMER6_CONTEXT

Address Offset	0x0000 0074		
Physical Address	0x4AE0 6574	**Instance**	ABE_PRM
Description	This register contains dedicated TIMER6 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-428. Register Call Summary for Register RM_ABE_TIMER6_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-429. PM_ABE_TIMER7_WKDEP

Address Offset	0x0000 0078		
Physical Address	0x4AE0 6578	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on TIMER7 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													WKUPDEP_TIMER7_DSP	RESERVED	WKUPDEP_TIMER7_MPU

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	WKUPDEP_TIMER7_DSP	Wakeup dependency from TIMER7 module (SWakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	WKUPDEP_TIMER7_MPU	Wakeup dependency from TIMER7 module (SWakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-430. Register Call Summary for Register PM_ABE_TIMER7_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • ABE_PRM Register Summary: [2]

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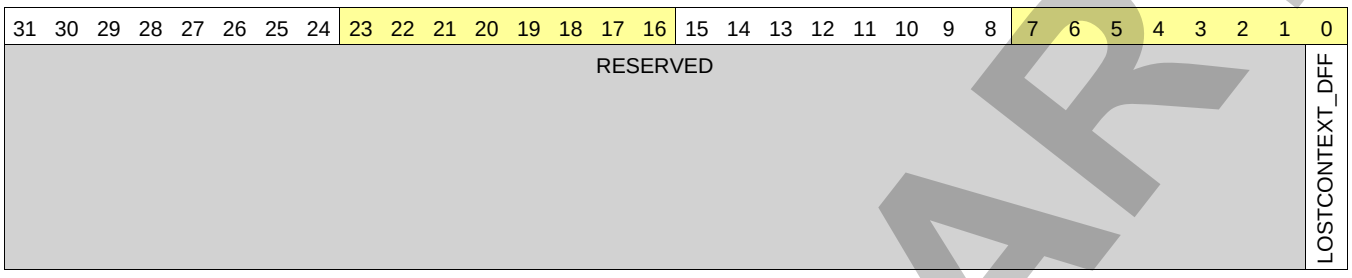
Table 3-431. RM_ABE_TIMER7_CONTEXT

Address Offset	0x0000 007C		
Physical Address	0x4AE0 657C	**Instance**	ABE_PRM
Description	This register contains dedicated TIMER7 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

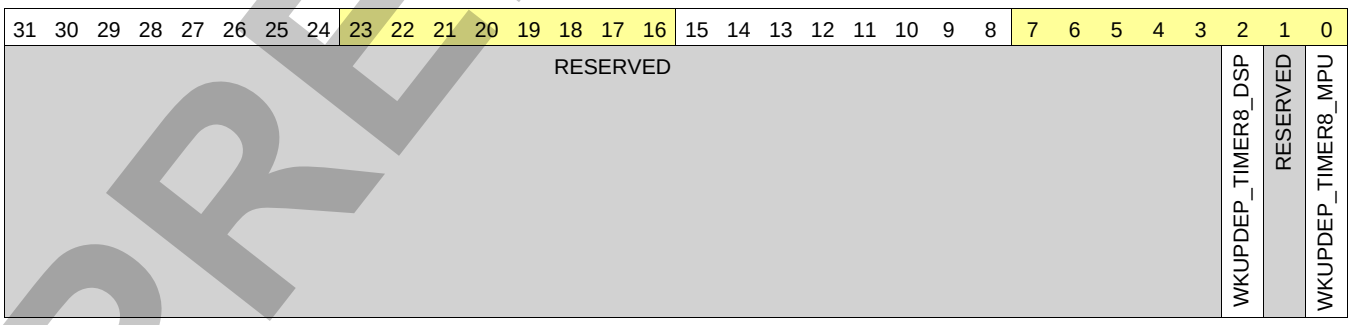
Table 3-432. Register Call Summary for Register RM_ABE_TIMER7_CONTEXT

Power Management Functional Description
- PD_ABE Description: [0]

PRCM Register Manual
- ABE_PRM Register Summary: [1]

Table 3-433. PM_ABE_TIMER8_WKDEP

Address Offset	0x0000 0080		
Physical Address	0x4AE0 6580	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on TIMER8 service requests.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	WKUPDEP_TIMER8_DSP	Wakeup dependency from TIMER8 module (SWakeup signal) towards DSP domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
1	RESERVED		R	0
0	WKUPDEP_TIMER8_MPU	Wakeup dependency from TIMER8 module (SWakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-434. Register Call Summary for Register PM_ABE_TIMER8_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • ABE_PRM Register Summary: [2]

Table 3-435. RM_ABE_TIMER8_CONTEXT

Address Offset	0x0000 0084		
Physical Address	0x4AE0 6584	**Instance**	ABE_PRM
Description	This register contains dedicated TIMER8 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-436. Register Call Summary for Register RM_ABE_TIMER8_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-437. PM_ABE_WD_TIMER3_WKDEP

Address Offset	0x0000 0088		
Physical Address	0x4AE0 6588	**Instance**	ABE_PRM
Description	This register controls wakeup dependency based on WD_TIMER3 service requests.		
Type	RW		

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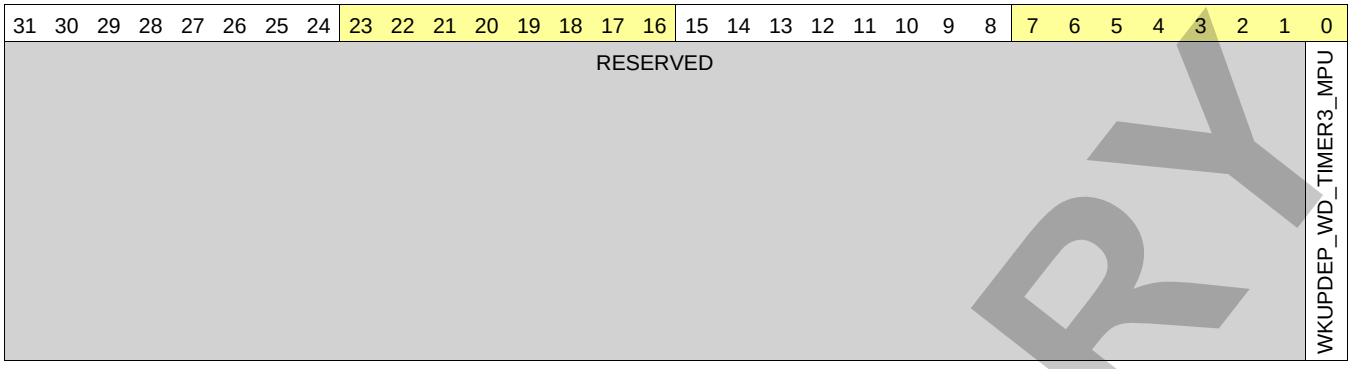


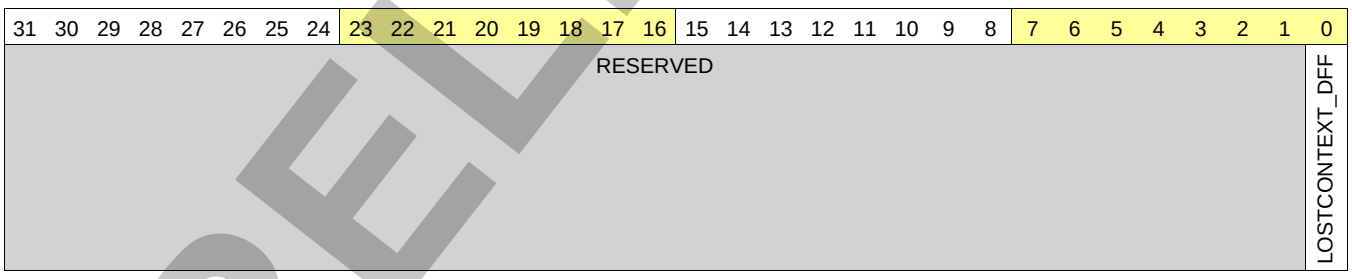
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_WD_TIMER3_MPU	Wakeup dependency from WD_TIMER3 module (SWakeup signal) towards MPU domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

Table 3-438. Register Call Summary for Register PM_ABE_WD_TIMER3_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

Table 3-439. RM_ABE_WD_TIMER3_CONTEXT

Address Offset	0x0000 008C		
Physical Address	0x4AE0 658C	**Instance**	ABE_PRM
Description	This register contains dedicated WD_TIMER3 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of ABE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-440. Register Call Summary for Register RM_ABE_WD_TIMER3_CONTEXT

Power Management Functional Description • PD_ABE Description: [0]
PRCM Register Manual • ABE_PRM Register Summary: [1]

3.11.7 COREAON_PRM Registers

3.11.7.1 COREON_PRM Register Summary

Table 3-441. COREAON_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	COREAON_PRM Base Address
PM_COREAON_SMARTREFLEX_MPU_WKDEP	RW	32	0x0000 0028	0x4AE0 6628
RM_COREAON_SMARTREFLEX_MPU_CONTEXT	RW	32	0x0000 002C	0x4AE0 662C
PM_COREAON_SMARTREFLEX_MM_WKDEP	RW	32	0x0000 0030	0x4AE0 6630
RM_COREAON_SMARTREFLEX_MM_CONTEXT	RW	32	0x0000 0034	0x4AE0 6634
PM_COREAON_SMARTREFLEX_CORE_WKDEP	RW	32	0x0000 0038	0x4AE0 6638
RM_COREAON_SMARTREFLEX_CORE_CONTEXT	RW	32	0x0000 003C	0x4AE0 663C

3.11.7.2 COREON_PRM Register Description

Table 3-442. PM_COREAON_SMARTREFLEX_MPU_WKDEP

Address Offset	0x0000 0028		
Physical Address	0x4AE0 6628	**Instance**	COREAON_PRM
Description	This register controls wakeup dependency based on SMARTREFLEX_MPU service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_SMARTREFLEX_MPU_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_SMARTREFLEX_MPU_MPU	Wakeup dependency from SR_MPU module (SWakeup signal) towards MPU + L3MAIN1 + L4CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

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Table 3-443. Register Call Summary for Register PM_COREAON_SMARTREFLEX_MPU_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • COREON_PRM Register Summary: [1]

Table 3-444. RM_COREAON_SMARTREFLEX_MPU_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4AE0 662C	**Instance**	COREAON_PRM
Description	This register contains dedicated SMARTREFLEX_MPU context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of COREAON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-445. Register Call Summary for Register RM_COREAON_SMARTREFLEX_MPU_CONTEXT

Power Management Functional Description • PD_COREAON Description: [0]
PRCM Register Manual • COREON_PRM Register Summary: [1]

Table 3-446. PM_COREAON_SMARTREFLEX_MM_WKDEP

Address Offset	0x0000 0030		
Physical Address	0x4AE0 6630	**Instance**	COREAON_PRM
Description	This register controls wakeup dependency based on SMARTREFLEX_MM service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_SMARTREFLEX_MM_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_SMARTREFLEX_MM_MPU	Wakeup dependency from SMARTREFLEX_MM module (SWakeup signal) towards MPU + L3_MAIN1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-447. Register Call Summary for Register PM_COREAON_SMARTREFLEX_MM_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • COREON_PRM Register Summary: [1]

Table 3-448. RM_COREAON_SMARTREFLEX_MM_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4AE0 6634	**Instance**	COREAON_PRM
Description	This register contains dedicated SMARTREFLEX_MM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of Always_on_CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-449. Register Call Summary for Register RM_COREAON_SMARTREFLEX_MM_CONTEXT

Power Management Functional Description • PD_COREAON Description: [0]
PRCM Register Manual • COREON_PRM Register Summary: [1]

Table 3-450. PM_COREAON_SMARTREFLEX_CORE_WKDEP

Address Offset	0x0000 0038		
Physical Address	0x4AE0 6638	**Instance**	COREAON_PRM
Description	This register controls wakeup dependency based on SMARTREFLEX_CORE service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_SMARTREFLEX_CORE_IPU	WKUPDEP_SMARTREFLEX_CORE_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_SMARTREFLEX_CORE_IPU	Wakeup dependency from SMARTREFLEX_CORE module (SWakeup signal) towards IPU + L3_MAIN2 + L3_MAIN1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_SMARTREFLEX_CORE_MPU	Wakeup dependency from SMARTREFLEX_CORE module (SWakeup signal) towards MPU + L3_MAIN1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-451. Register Call Summary for Register PM_COREAON_SMARTREFLEX_CORE_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • COREON_PRM Register Summary: [2]

Table 3-452. RM_COREAON_SMARTREFLEX_CORE_CONTEXT

Address Offset	0x0000 003C		
Physical Address	0x4AE0 663C	**Instance**	COREAON_PRM
Description	This register contains dedicated SMARTREFLEX_CORE context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of COREAON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-453. Register Call Summary for Register RM_COREAON_SMARTREFLEX_CORE_CONTEXT

Power Management Functional Description • PD_COREAON Description: [0]
PRCM Register Manual • COREON_PRM Register Summary: [1]

3.11.8 CORE_PRM Registers

3.11.8.1 CORE_PRM Register Summary

Table 3-454. CORE_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORE_PRM L4 Base Address
PM_CORE_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 6700
PM_CORE_PWRSTST	RW	32	0x0000 0004	0x4AE0 6704
RM_L3MAIN1_L3_MAIN_1_CONTEXT	RW	32	0x0000 0024	0x4AE0 6724
RM_L3MAIN2_L3_MAIN_2_CONTEXT	RW	32	0x0000 0124	0x4AE0 6824
RM_L3MAIN2_GPMC_CONTEXT	RW	32	0x0000 012C	0x4AE0 682C
RM_L3MAIN2_OCMC_RAM_CONTEXT	RW	32	0x0000 0134	0x4AE0 6834
RM_IPU_RSTCTRL	RW	32	0x0000 0210	0x4AE0 6910
RM_IPU_RSTST	RW	32	0x0000 0214	0x4AE0 6914
RM_IPU_IPU_CONTEXT	RW	32	0x0000 0224	0x4AE0 6924
RM_DMA_DMA_SYSTEM_CONTEXT	RW	32	0x0000 0324	0x4AE0 6A24
RM_EMIF_DMM_CONTEXT	RW	32	0x0000 0424	0x4AE0 6B24
RM_EMIF_EMIF_FW_CONTEXT	RW	32	0x0000 042C	0x4AE0 6B2C
RM_EMIF_EMIF1_CONTEXT	RW	32	0x0000 0434	0x4AE0 6B34
RM_EMIF_EMIF2_CONTEXT	RW	32	0x0000 043C	0x4AE0 6B3C
RM_EMIF_EMIF_DLL_CONTEXT	RW	32	0x0000 0444	0x4AE0 6B44
RESERVED	R	32	0x0000 0524	0x4AE0 6C24
RESERVED	R	32	0x0000 052C	0x4AE0 6C2C
RESERVED	R	32	0x0000 0534	0x4AE0 6C34
RM_L4CFG_L4_CFG_CONTEXT	RW	32	0x0000 0624	0x4AE0 6D24
RM_L4CFG_SPINLOCK_CONTEXT	RW	32	0x0000 062C	0x4AE0 6D2C

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Table 3-454. CORE_PRM Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CORE_PRM L4 Base Address
RM_L4CFG_MAILBOX_CONTEXT	RW	32	0x0000 0634	0x4AE0 6D34
RM_L4CFG_SAR_ROM_CONTEXT	RW	32	0x0000 063C	0x4AE0 6D3C
RESERVED	R	32	0x0000 0644	0x4AE0 6D44
RM_L3INSTR_L3_MAIN_3_CONTEXT	RW	32	0x0000 0724	0x4AE0 6E24
RM_L3INSTR_L3_INSTR_CONTEXT	RW	32	0x0000 072C	0x4AE0 6E2C
RM_L3INSTR_OCP_WP_NOC_CONTEXT	RW	32	0x0000 0744	0x4AE0 6E44
RESERVED	R	32	0x0000 0824	0x4AE0 6F24
RESERVED	R	32	0x0000 082C	0x4AE0 6F2C
RESERVED	R	32	0x0000 0834	0x4AE0 6F34
PM_L4PER_TIMER10_WKDEP	RW	32	0x0000 0928	0x4AE0 7028
RM_L4PER_TIMER10_CONTEXT	RW	32	0x0000 092C	0x4AE0 702C
PM_L4PER_TIMER11_WKDEP	RW	32	0x0000 0930	0x4AE0 7030
RM_L4PER_TIMER11_CONTEXT	RW	32	0x0000 0934	0x4AE0 7034
PM_L4PER_TIMER2_WKDEP	RW	32	0x0000 0938	0x4AE0 7038
RM_L4PER_TIMER2_CONTEXT	RW	32	0x0000 093C	0x4AE0 703C
PM_L4PER_TIMER3_WKDEP	RW	32	0x0000 0940	0x4AE0 7040
RM_L4PER_TIMER3_CONTEXT	RW	32	0x0000 0944	0x4AE0 7044
PM_L4PER_TIMER4_WKDEP	RW	32	0x0000 0948	0x4AE0 7048
RM_L4PER_TIMER4_CONTEXT	RW	32	0x0000 094C	0x4AE0 704C
PM_L4PER_TIMER9_WKDEP	RW	32	0x0000 0950	0x4AE0 7050
RM_L4PER_TIMER9_CONTEXT	RW	32	0x0000 0954	0x4AE0 7054
RM_L4PER_ELM_CONTEXT	RW	32	0x0000 095C	0x4AE0 705C
PM_L4PER_GPIO2_WKDEP	RW	32	0x0000 0960	0x4AE0 7060
RM_L4PER_GPIO2_CONTEXT	RW	32	0x0000 0964	0x4AE0 7064
PM_L4PER_GPIO3_WKDEP	RW	32	0x0000 0968	0x4AE0 7068
RM_L4PER_GPIO3_CONTEXT	RW	32	0x0000 096C	0x4AE0 706C
PM_L4PER_GPIO4_WKDEP	RW	32	0x0000 0970	0x4AE0 7070
RM_L4PER_GPIO4_CONTEXT	RW	32	0x0000 0974	0x4AE0 7074
PM_L4PER_GPIO5_WKDEP	RW	32	0x0000 0978	0x4AE0 7078
RM_L4PER_GPIO5_CONTEXT	RW	32	0x0000 097C	0x4AE0 707C
PM_L4PER_GPIO6_WKDEP	RW	32	0x0000 0980	0x4AE0 7080
RM_L4PER_GPIO6_CONTEXT	RW	32	0x0000 0984	0x4AE0 7084
RM_L4PER_HDQ1W_CONTEXT	RW	32	0x0000 098C	0x4AE0 708C
PM_L4PER_I2C1_WKDEP	RW	32	0x0000 09A0	0x4AE0 70A0
RM_L4PER_I2C1_CONTEXT	RW	32	0x0000 09A4	0x4AE0 70A4
PM_L4PER_I2C2_WKDEP	RW	32	0x0000 09A8	0x4AE0 70A8
RM_L4PER_I2C2_CONTEXT	RW	32	0x0000 09AC	0x4AE0 70AC
PM_L4PER_I2C3_WKDEP	RW	32	0x0000 09B0	0x4AE0 70B0
RM_L4PER_I2C3_CONTEXT	RW	32	0x0000 09B4	0x4AE0 70B4
PM_L4PER_I2C4_WKDEP	RW	32	0x0000 09B8	0x4AE0 70B8
RM_L4PER_I2C4_CONTEXT	RW	32	0x0000 09BC	0x4AE0 70BC
RM_L4PER_L4_PER_CONTEXT	RW	32	0x0000 09C0	0x4AE0 70C0
PM_L4PER_MCSPI1_WKDEP	RW	32	0x0000 09F0	0x4AE0 70F0
RM_L4PER_MCSPI1_CONTEXT	RW	32	0x0000 09F4	0x4AE0 70F4
PM_L4PER_MCSPI2_WKDEP	RW	32	0x0000 09F8	0x4AE0 70F8
RM_L4PER_MCSPI2_CONTEXT	RW	32	0x0000 09FC	0x4AE0 70FC

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Table 3-454. CORE_PRM Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CORE_PRM L4 Base Address
PM_L4PER_MCSPI3_WKDEP	RW	32	0x0000 0A00	0x4AE0 7100
RM_L4PER_MCSPI3_CONTEXT	RW	32	0x0000 0A04	0x4AE0 7104
PM_L4PER_MCSPI4_WKDEP	RW	32	0x0000 0A08	0x4AE0 7108
RM_L4PER_MCSPI4_CONTEXT	RW	32	0x0000 0A0C	0x4AE0 710C
PM_L4PER_GPIO7_WKDEP	RW	32	0x0000 0A10	0x4AE0 7110
RM_L4PER_GPIO7_CONTEXT	RW	32	0x0000 0A14	0x4AE0 7114
PM_L4PER_GPIO8_WKDEP	RW	32	0x0000 0A18	0x4AE0 7118
RM_L4PER_GPIO8_CONTEXT	RW	32	0x0000 0A1C	0x4AE0 711C
PM_L4PER_MMC3_WKDEP	RW	32	0x0000 0A20	0x4AE0 7120
RM_L4PER_MMC3_CONTEXT	RW	32	0x0000 0A24	0x4AE0 7124
PM_L4PER_MMC4_WKDEP	RW	32	0x0000 0A28	0x4AE0 7128
RM_L4PER_MMC4_CONTEXT	RW	32	0x0000 0A2C	0x4AE0 712C
PM_L4PER_UART1_WKDEP	RW	32	0x0000 0A40	0x4AE0 7140
RM_L4PER_UART1_CONTEXT	RW	32	0x0000 0A44	0x4AE0 7144
PM_L4PER_UART2_WKDEP	RW	32	0x0000 0A48	0x4AE0 7148
RM_L4PER_UART2_CONTEXT	RW	32	0x0000 0A4C	0x4AE0 714C
PM_L4PER_UART3_WKDEP	RW	32	0x0000 0A50	0x4AE0 7150
RM_L4PER_UART3_CONTEXT	RW	32	0x0000 0A54	0x4AE0 7154
RM_L4PER_UART4_CONTEXT	RW	32	0x0000 0A58	0x4AE0 7158
PM_L4PER_UART4_WKDEP	RW	32	0x0000 0A5C	0x4AE0 715C
PM_L4PER_MMC5_WKDEP	RW	32	0x0000 0A60	0x4AE0 7160
RM_L4PER_MMC5_CONTEXT	RW	32	0x0000 0A64	0x4AE0 7164
PM_L4PER_I2C5_WKDEP	RW	32	0x0000 0A68	0x4AE0 7168
RM_L4PER_I2C5_CONTEXT	RW	32	0x0000 0A6C	0x4AE0 716C
PM_L4PER_UART5_WKDEP	RW	32	0x0000 0A70	0x4AE0 7170
RM_L4PER_UART5_CONTEXT	RW	32	0x0000 0A74	0x4AE0 7174
PM_L4PER_UART6_WKDEP	RW	32	0x0000 0A78	0x4AE0 7178
RM_L4PER_UART6_CONTEXT	RW	32	0x0000 0A7C	0x4AE0 717C
RM_L4SEC_AES1_CONTEXT	RW	32	0x0000 0AA4	0x4AE0 71A4
RM_L4SEC_AES2_CONTEXT	RW	32	0x0000 0AAC	0x4AE0 71AC
RM_L4SEC_DES3DES_CONTEXT	RW	32	0x0000 0AB4	0x4AE0 71B4
RM_L4SEC_FPKA_CONTEXT	RW	32	0x0000 0ABC	0x4AE0 71BC
RM_L4SEC_RNG_CONTEXT	RW	32	0x0000 0AC4	0x4AE0 71C4
RM_L4SEC_SHA2MD5_CONTEXT	RW	32	0x0000 0ACC	0x4AE0 71CC
RM_L4SEC_DMA_CRYPTO_CONTEXT	RW	32	0x0000 0ADC	0x4AE0 71DC

3.11.8.2 CORE_PRM Register Description

Table 3-455. PM_CORE_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 6700	**Instance**	CORE_PRM
Description	This register controls the CORE power state to reach upon a domain sleep transition		
Type	RW		

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31 30 29 28 27 26	25 24	23 22	21 20	19 18	17 16	15 14 13	12	11	10	9	8	7 6 5	4	3	2	1 0
RESERVED	OCP_NRET_BANK_ONSTATE	IPU_SCACHE_ONSTATE	IPU_L2RAM_ONSTATE	CORE_OCMRAM_ONSTATE	CORE_OTHER_BANK_ONSTATE	RESERVED	OCP_NRET_BANK_RETSTATE	IPU_SCACHE_RETSTATE	MPU_M3_L2RAM_RETSTATE	CORE_OCMRAM_RETSTATE	CORE_OTHER_BANK_RETSTATE	RESERVED	LOWPOWERSTATECHANGE	RESERVED	LOGICRETSTATE	POWERSTATE

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	OCP_NRET_BANK_ONSTATE	OCP_NRET_BANK state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
23:22	IPU_SCACHE_ONSTATE	IPU SCACHE bank state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
21:20	IPU_L2RAM_ONSTATE	IPU L2 bank state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
19:18	CORE_OCMRAM_ONSTATE	OCMRAM bank state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
17:16	CORE_OTHER_BANK_ONSTATE	CORE_OTHER_BANK state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:13	RESERVED		R	0x0
12	OCP_NRET_BANK_RETSTATE	OCP_NRET_BANK state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
11	IPU_SCACHE_RETSTATE	IPU SCACHE bank state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
10	IPU_L2RAM_RETSTATE	IPU L2 bank state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
9	CORE_OCMRAM_RETSTATE	OCMRAM bank state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R	1
8	CORE_OTHER_BANK_RETSTATE	CORE_OTHER_BANK state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R	1
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0

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Bits	Field Name	Description	Type	Reset
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1
1:0	POWERSTATE	Power state control Read 0x0: Reserved 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

Table 3-456. Register Call Summary for Register PM_CORE_PWRSTCTRL

Power Management Functional Description • Logic and Memory Area Power Mode Control and Status: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
PRCM Register Manual • CORE_PRM Register Summary: [13]

Table 3-457. PM_CORE_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 6704	**Instance**	CORE_PRM
Description	This register provides a status on the current CORE power domain state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
						LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED						OCP_NRET_BANK_STATEST		IPU_SCACHE_STATEST		IPU_L2RAM_STATEST		CORE_OCMRAM_STATEST		CORE_OTHER_BANK_STATEST		RESERVED		LOGICSTATEST		POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Reserved	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:14	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
13:12	OCP_NRET_BANK_STATEST	OCP_NRET_BANK bank state status Read 0x0: Reserved Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
11:10	IPU_SCACHE_STATEST	IPU SCACHE bank state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
9:8	IPU_L2RAM_STATEST	IPU L2 bank state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	CORE_OCMRAM_STATEST	OCMRAM bank state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
5:4	CORE_OTHER_BANK_STATEST	CORE_OTHER_BANK state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-458. Register Call Summary for Register PM_CORE_PWRSTST

Power Management Functional Description • Logic and Memory Area Power Mode Control and Status: [0] [1] [2] [3] [4] [5] [6] [7] [8]
PRCM Register Manual • CORE_PRM Register Summary: [9]

Table 3-459. RM_L3MAIN1_L3_MAIN_1_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 6724	**Instance**	CORE_PRM
Description	This register contains dedicated L3_MAIN1 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-460. Register Call Summary for Register RM_L3MAIN1_L3_MAIN_1_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-461. RM_L3MAIN2_L3_MAIN_2_CONTEXT

Address Offset	0x0000 0124		
Physical Address	0x4AE0 6824	**Instance**	CORE_PRM
Description	This register contains dedicated L3_MAIN2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-462. Register Call Summary for Register RM_L3MAIN2_L3_MAIN_2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-463. RM_L3MAIN2_GPMC_CONTEXT

Address Offset	0x0000 012C		
Physical Address	0x4AE0 682C	**Instance**	CORE_PRM
Description	This register contains dedicated GPMC context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-464. Register Call Summary for Register RM_L3MAIN2_GPMC_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-465. RM_L3MAIN2_OCMC_RAM_CONTEXT

Address Offset	0x0000 0134		
Physical Address	0x4AE0 6834	**Instance**	CORE_PRM
Description	This register contains dedicated OCMC_RAM context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_CORE_OCMRAM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CORE_OCMRAM	Specify if memory-based context in CORE_OCMRAM memory bank has been lost due to a previous power transition or other reset source (not affected by a global warm reset). 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-466. Register Call Summary for Register RM_L3MAIN2_OCMC_RAM_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-467. RM_IPU_RSTCTRL

Address Offset	0x0000 0210		
Physical Address	0x4AE0 6910	**Instance**	CORE_PRM
Description	This register controls the release of the IPU sub-system resets.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													RST_IPU_MMU_CACHE	RST_CPU1	RST_CPU0

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	RST_IPU_MMU_CACHE	IPU MMU and CACHE interface reset control. 0x0: Reset is cleared for IPU CACHE and MMU 0x1: Reset is asserted for the IPU CACHE and MMU	RW	1
1	RST_CPU1	IPU CPU1 reset control. 0x0: Reset is cleared for the IPU CPU1 0x1: Reset is asserted for the IPU CPU1	RW	1
0	RST_CPU0	IPU CPU0 reset control. 0x0: Reset is cleared for the IPU CPU0 0x1: Reset is asserted for the IPU CPU0	RW	1

Table 3-468. Register Call Summary for Register RM_IPU_RSTCTRL

Reset Management Functional Description
- Reset Domains: [0] [1] [2] [3] [4]
- IPU Subsystem Power-On Reset Sequence: [5] [6] [7]
- IPU Subsystem Software Warm Reset Sequence: [8] [9] [10] [11] [12] [13]

PRCM Register Manual
- CORE_PRM Register Summary: [14]

Table 3-469. RM_IPU_RSTST

Address Offset	0x0000 0214		
Physical Address	0x4AE0 6914	**Instance**	CORE_PRM
Description	This register logs the different reset sources of the IPU SS. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RST_ICECRUSHER_CPU1	RST_ICECRUSHER_CPU0	RST_EMULATION_CPU1	RST_EMULATION_CPU0	RST_IPU_MMU_CACHE	RST_CPU1	RST_CPU0	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	RST_ICECRUSHER_CPU1	IPU CPU1 has been reset due to IPU ICECRUSHER1 reset source 0x0: No icecrusher reset 0x1: IPU CPU1 has been reset upon icecrusher reset	RW W1toClr	0
5	RST_ICECRUSHER_CPU0	IPU CPU0 has been reset due to IPU ICECRUSHER0 reset source 0x0: No icecrusher reset 0x1: CPU0 has been reset upon icecrusher reset	RW W1toClr	0
4	RST_EMULATION_CPU1	IPU CPU1 has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: IPU CPU1 has been reset upon emulation reset	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
3	RST_EMULATION_CPU0	IPU CPU0 has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: IPU CPU0 has been reset upon emulation reset	RW W1toClr	0
2	RST_IPU_MMU_CACHE	IPU MMU and CACHE interface SW reset status 0x0: No SW reset occured 0x1: IPU MMU and CACHE interface has been reset upon SW reset	RW W1toClr	0
1	RST_CPU1	IPU CPU1 SW reset status 0x0: No SW reset occured 0x1: IPU CPU1 has been reset upon SW reset	RW W1toClr	0
0	RST_CPU0	IPU CPU0 SW reset status 0x0: No SW reset occured 0x1: IPU CPU0 has been reset upon SW reset	RW W1toClr	0

Table 3-470. Register Call Summary for Register RM_IPU_RSTST

PRCM Register Manual
- CORE_PRM Register Summary: [0]

Table 3-471. RM_IPU_IPU_CONTEXT

Address Offset	0x0000 0224		
Physical Address	0x4AE0 6924	**Instance**	CORE_PRM
Description	This register contains dedicated IPU context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						LOSTMEM_IPU_L2RAM	LOSTMEM_IPU_SCACHE	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	LOSTMEM_IPU_L2RAM	Specify if memory-based context in IPU_L2RAM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8	LOSTMEM_IPU_SCACHE	Specify if memory-based context in IPU_SCACHE memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of IPU_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of IPU_RST3 signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-472. Register Call Summary for Register RM_IPU_IPU_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-473. RM_DMA_DMA_SYSTEM_CONTEXT

Address Offset	0x0000 0324		
Physical Address	0x4AE0 6A24	**Instance**	CORE_PRM
Description	This register contains dedicated DMA_SYSTEM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_CORE_OTHER_BANK	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CORE_OTHER_BANK	Specify if memory-based context in CORE_OTHER_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of SDMA_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

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Table 3-474. Register Call Summary for Register RM_DMA_DMA_SYSTEM_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-475. RM_EMIF_DMM_CONTEXT

Address Offset	0x0000 0424		
Physical Address	0x4AE0 6B24	**Instance**	CORE_PRM
Description	This register contains dedicated DMM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						LOSTMEM_CORE_NRET_BANK	LOSTMEM_CORE_OTHER_BANK	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	LOSTMEM_CORE_NRET_BANK	Specify if memory-based context in CORE_NRET_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8	LOSTMEM_CORE_OTHER_BANK	Specify if memory-based context in CORE_OTHER_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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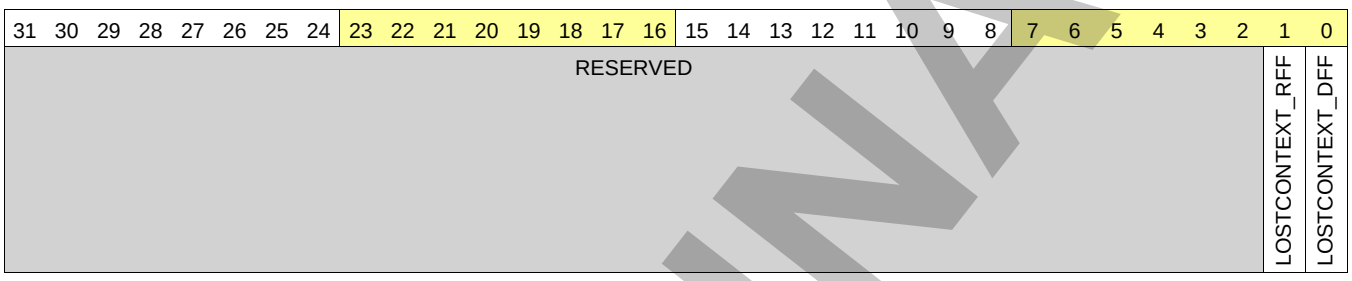
Table 3-476. Register Call Summary for Register RM_EMIF_DMM_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-477. RM_EMIF_EMIF_FW_CONTEXT

Address Offset	0x0000 042C		
Physical Address	0x4AE0 6B2C	**Instance**	CORE_PRM
Description	This register contains dedicated EMIF_FW context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-478. Register Call Summary for Register RM_EMIF_EMIF_FW_CONTEXT

PRCM Register Manual • CORE_PRM Register Summary: [0]

Table 3-479. RM_EMIF_EMIF1_CONTEXT

Address Offset	0x0000 0434		
Physical Address	0x4AE0 6B34	**Instance**	CORE_PRM
Description	This register contains dedicated EMIF1 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-480. Register Call Summary for Register RM_EMIF_EMIF1_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-481. RM_EMIF_EMIF2_CONTEXT

Address Offset	0x0000 043C		
Physical Address	0x4AE0 6B3C	**Instance**	CORE_PRM
Description	This register contains dedicated EMIF2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-482. Register Call Summary for Register RM_EMIF_EMIF2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-483. RM_EMIF_EMIF_DLL_CONTEXT

Address Offset	0x0000 0444		
Physical Address	0x4AE0 6B44	**Instance**	CORE_PRM
Description	This register contains dedicated DLL context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DLL_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-484. Register Call Summary for Register RM_EMIF_EMIF_DLL_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-485. RM_L4CFG_L4_CFG_CONTEXT

Address Offset	0x0000 0624		
Physical Address	0x4AE0 6D24	**Instance**	CORE_PRM
Description	This register contains dedicated L4_CFG context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-486. Register Call Summary for Register RM_L4CFG_L4_CFG_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-487. RM_L4CFG_SPINLOCK_CONTEXT

Address Offset	0x0000 062C		
Physical Address	0x4AE0 6D2C	**Instance**	CORE_PRM
Description	This register contains dedicated HW_SEM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

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Table 3-488. Register Call Summary for Register RM_L4CFG_SPINLOCK_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-489. RM_L4CFG_MAILBOX_CONTEXT

Address Offset	0x0000 0634		
Physical Address	0x4AE0 6D34	**Instance**	CORE_PRM
Description	This register contains dedicated MAILBOX context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-490. Register Call Summary for Register RM_L4CFG_MAILBOX_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-491. RM_L4CFG_SAR_ROM_CONTEXT

Address Offset	0x0000 063C		
Physical Address	0x4AE0 6D3C	**Instance**	CORE_PRM
Description	This register contains dedicated SAR_ROM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-492. Register Call Summary for Register RM_L4CFG_SAR_ROM_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-493. RM_L3INSTR_L3_MAIN_3_CONTEXT

Address Offset	0x0000 0724		
Physical Address	0x4AE0 6E24	**Instance**	CORE_PRM
Description	This register contains dedicated L3_MAIN3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-494. Register Call Summary for Register RM_L3INSTR_L3_MAIN_3_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

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Table 3-495. RM_L3INSTR_L3_INSTR_CONTEXT

Address Offset	0x0000 072C		
Physical Address	0x4AE0 6E2C	**Instance**	CORE_PRM
Description	This register contains dedicated L3_INSTR context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-496. Register Call Summary for Register RM_L3INSTR_L3_INSTR_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-497. RM_L3INSTR_OCP_WP_NOC_CONTEXT

Address Offset	0x0000 0744		
Physical Address	0x4AE0 6E44	**Instance**	CORE_PRM
Description	This register contains dedicated OCP_WP_NOC context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_CORE_NRET_BANK	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CORE_NRET_BANK	Specify if memory-based context in CORE_NRET_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-498. Register Call Summary for Register RM_L3INSTR_OCP_WP_NOC_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-499. PM_L4PER_TIMER10_WKDEP

Address Offset	0x0000 0928		
Physical Address	0x4AE0 7028	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on TIMER10 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_TIMER10_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_TIMER10_MPU	Wakeup dependency from TIMER10 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

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Table 3-500. Register Call Summary for Register PM_L4PER_TIMER10_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-501. RM_L4PER_TIMER10_CONTEXT

Address Offset	0x0000 092C		
Physical Address	0x4AE0 702C	**Instance**	CORE_PRM
Description	This register contains dedicated TIMER10 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-502. Register Call Summary for Register RM_L4PER_TIMER10_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-503. PM_L4PER_TIMER11_WKDEP

Address Offset	0x0000 0930		
Physical Address	0x4AE0 7030	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on TIMER11 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_TIMER11_IPU	WKUPDEP_TIMER11_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_TIMER11_IPU	Wakeup dependency from TIMER11 module (SWakeup signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_TIMER11_MPU	Wakeup dependency from TIMER11 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-504. Register Call Summary for Register PM_L4PER_TIMER11_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-505. RM_L4PER_TIMER11_CONTEXT

Address Offset	0x0000 0934		
Physical Address	0x4AE0 7034	**Instance**	CORE_PRM
Description	This register contains dedicated TIMER11 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-506. Register Call Summary for Register RM_L4PER_TIMER11_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-507. PM_L4PER_TIMER2_WKDEP

Address Offset	0x0000 0938		
Physical Address	0x4AE0 7038	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on TIMER2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_TIMER2_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_TIMER2_MPU	Wakeup dependency from TIMER2 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

Table 3-508. Register Call Summary for Register PM_L4PER_TIMER2_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-509. RM_L4PER_TIMER2_CONTEXT

Address Offset	0x0000 093C		
Physical Address	0x4AE0 703C	**Instance**	CORE_PRM
Description	This register contains dedicated TIMER2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-510. Register Call Summary for Register RM_L4PER_TIMER2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-511. PM_L4PER_TIMER3_WKDEP

Address Offset	0x0000 0940		
Physical Address	0x4AE0 7040	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on TIMER3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_TIMER3_IPU	WKUPDEP_TIMER3_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_TIMER3_IPU	Wakeup dependency from TIMER3 module (SWakeup signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_TIMER3_MPU	Wakeup dependency from TIMER3 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-512. Register Call Summary for Register PM_L4PER_TIMER3_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

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Table 3-513. RM_L4PER_TIMER3_CONTEXT

Address Offset	0x0000 0944		
Physical Address	0x4AE0 7044	**Instance**	CORE_PRM
Description	This register contains dedicated TIMER3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-514. Register Call Summary for Register RM_L4PER_TIMER3_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-515. PM_L4PER_TIMER4_WKDEP

Address Offset	0x0000 0948		
Physical Address	0x4AE0 7048	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on TIMER4 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_TIMER4_IPU	WKUPDEP_TIMER4_MPU

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_TIMER4_IPU	Wakeup dependency from TIMER4 module (SWakeup signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_TIMER4_MPU	Wakeup dependency from TIMER4 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-516. Register Call Summary for Register PM_L4PER_TIMER4_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-517. RM_L4PER_TIMER4_CONTEXT

Address Offset	0x0000 094C		
Physical Address	0x4AE0 704C	**Instance**	CORE_PRM
Description	This register contains dedicated TIMER4 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-518. Register Call Summary for Register RM_L4PER_TIMER4_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

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Table 3-519. PM_L4PER_TIMER9_WKDEP

Address Offset	0x0000 0950		
Physical Address	0x4AE0 7050	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on TIMER9 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_TIMER9_IPU	WKUPDEP_TIMER9_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_TIMER9_IPU	Wakeup dependency from TIMER9 module (SWakeup signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_TIMER9_MPU	Wakeup dependency from TIMER9 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-520. Register Call Summary for Register PM_L4PER_TIMER9_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-521. RM_L4PER_TIMER9_CONTEXT

Address Offset	0x0000 0954		
Physical Address	0x4AE0 7054	**Instance**	CORE_PRM
Description	This register contains dedicated TIMER9 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-522. Register Call Summary for Register RM_L4PER_TIMER9_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-523. RM_L4PER_ELM_CONTEXT

Address Offset	0x0000 095C		
Physical Address	0x4AE0 705C	**Instance**	CORE_PRM
Description	This register contains dedicated ELM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-524. Register Call Summary for Register RM_L4PER_ELM_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-525. PM_L4PER_GPIO2_WKDEP

Address Offset	0x0000 0960		
Physical Address	0x4AE0 7060	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on GPIO2 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_GPIO2_IRQ2_DSP	RESERVED					WKUPDEP_GPIO2_IRQ1_IPU	WKUPDEP_GPIO2_IRQ1_MPU

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000
6	WKUPDEP_GPIO2_IRQ2_DSP	Wakeup dependency from GPIO2 module (POINTRSWAKEUP2 signal) towards DSP + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5:2	RESERVED		R	0x0
1	WKUPDEP_GPIO2_IRQ1_IPU	Wakeup dependency from GPIO2 module (POINTRSWAKEUP1 signal) module towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_GPIO2_IRQ1_MPU	Wakeup dependency from GPIO2 module (POINTRSWAKEUP1 signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-526. Register Call Summary for Register PM_L4PER_GPIO2_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • CORE_PRM Register Summary: [3]

Table 3-527. RM_L4PER_GPIO2_CONTEXT

Address Offset	0x0000 0964		
Physical Address	0x4AE0 7064	**Instance**	CORE_PRM
Description	This register contains dedicated GPIO2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-528. Register Call Summary for Register RM_L4PER_GPIO2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-529. PM_L4PER_GPIO3_WKDEP

Address Offset	0x0000 0968		
Physical Address	0x4AE0 7068	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on GPIO3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_GPIO3_IRQ2_DSP	RESERVED						WKUPDEP_GPIO3_IRQ1_MPU

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000
6	WKUPDEP_GPIO3_IRQ2_DSP	Wakeup dependency from GPIO3 module (POINTRSWAKEUP2 signal) towards DSP + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5:1	RESERVED		R	0x00
0	WKUPDEP_GPIO3_IRQ1_MPU	Wakeup dependency from GPIO3 module (POINTRSWAKEUP1 signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-530. Register Call Summary for Register PM_L4PER_GPIO3_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

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Table 3-531. RM_L4PER_GPIO3_CONTEXT

Address Offset	0x0000 096C		
Physical Address	0x4AE0 706C	**Instance**	CORE_PRM
Description	This register contains dedicated GPIO3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-532. Register Call Summary for Register RM_L4PER_GPIO3_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-533. PM_L4PER_GPIO4_WKDEP

Address Offset	0x0000 0970		
Physical Address	0x4AE0 7070	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on GPIO4 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_GPIO4_IRQ2_DSP	RESERVED					WKUPDEP_GPIO4_IRQ1_MPU

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000
6	WKUPDEP_GPIO4_IRQ2_DSP	Wakeup dependency from GPIO4 module (POINTRSWAKEUP2 signal) towards DSP + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5:1	RESERVED		R	0x00
0	WKUPDEP_GPIO4_IRQ1_MPU	Wakeup dependency from GPIO4 module (POINTRSWAKEUP1 signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-534. Register Call Summary for Register PM_L4PER_GPIO4_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-535. RM_L4PER_GPIO4_CONTEXT

Address Offset	0x0000 0974		
Physical Address	0x4AE0 7074	**Instance**	CORE_PRM
Description	This register contains dedicated GPIO4 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-536. Register Call Summary for Register RM_L4PER_GPIO4_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

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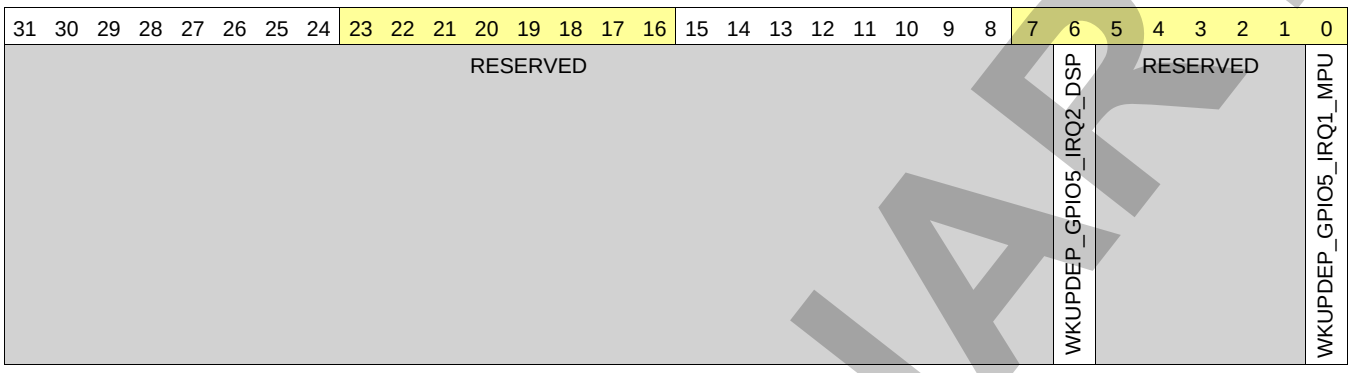
Table 3-537. PM_L4PER_GPIO5_WKDEP

Address Offset	0x0000 0978		
Physical Address	0x4AE0 7078	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on GPIO5 service requests.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000
6	WKUPDEP_GPIO5_IRQ2_DSP	Wakeup dependency from GPIO5 module (POINTRSWAKEUP2 signal) towards DSP + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5:1	RESERVED		R	0x00
0	WKUPDEP_GPIO5_IRQ1_MPU	Wakeup dependency from GPIO5 module (POINTRSWAKEUP1 signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

Table 3-538. Register Call Summary for Register PM_L4PER_GPIO5_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-539. RM_L4PER_GPIO5_CONTEXT

Address Offset	0x0000 097C		
Physical Address	0x4AE0 707C	**Instance**	CORE_PRM
Description	This register contains dedicated GPIO5 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-540. Register Call Summary for Register RM_L4PER_GPIO5_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-541. PM_L4PER_GPIO6_WKDEP

Address Offset	0x0000 0980		
Physical Address	0x4AE0 7080	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on GPIO6 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_GPIO6_IRQ2_DSP	RESERVED					WKUPDEP_GPIO6_IRQ1_MPU

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000
6	WKUPDEP_GPIO6_IRQ2_DSP	Wakeup dependency from GPIO6 module (POINTRSWAKEUP2 signal) towards DSP + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5:1	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
0	WKUPDEP_GPIO6_IRQ1_MPU	Wakeup dependency from GPIO6 module (POINTRSWAKEUP1 signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

Table 3-542. Register Call Summary for Register PM_L4PER_GPIO6_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-543. RM_L4PER_GPIO6_CONTEXT

Address Offset	0x0000 0984		
Physical Address	0x4AE0 7084	**Instance**	CORE_PRM
Description	This register contains dedicated GPIO6 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-544. Register Call Summary for Register RM_L4PER_GPIO6_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-545. RM_L4PER_HDQ1W_CONTEXT

Address Offset	0x0000 098C		
Physical Address	0x4AE0 708C	**Instance**	CORE_PRM
Description	This register contains dedicated HDQ1W context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-546. Register Call Summary for Register RM_L4PER_HDQ1W_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-547. PM_L4PER_I2C1_WKDEP

Address Offset	0x0000 09A0		
Physical Address	0x4AE0 70A0	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on I2C1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_I2C1_DMA_SDMA	RESERVED					WKUPDEP_I2C1_IRQ_IPU	WKUPDEP_I2C1_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7	WKUPDEP_I2C1_DMA_SDMA	Wakeup dependency from I2C1 module (SWakeup_dma signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
6:2	RESERVED		R	0x00
1	WKUPDEP_I2C1_IRQ_IPU	Wakeup dependency from I2C1 module (SWakeup_irq signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	WKUPDEP_I2C1_IRQ_MPU	Wakeup dependency from I2C1 module (SWakeup_irq signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-548. Register Call Summary for Register PM_L4PER_I2C1_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • CORE_PRM Register Summary: [3]

Table 3-549. RM_L4PER_I2C1_CONTEXT

Address Offset	0x0000 09A4		
Physical Address	0x4AE0 70A4	**Instance**	CORE_PRM
Description	This register contains dedicated I2C1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-550. Register Call Summary for Register RM_L4PER_I2C1_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-551. PM_L4PER_I2C2_WKDEP

Address Offset	0x0000 09A8		
Physical Address	0x4AE0 70A8	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on I2C2 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_I2C2_DMA_SDMA	RESERVED					WKUPDEP_I2C2_IRQ_IPU	WKUPDEP_I2C2_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7	WKUPDEP_I2C2_DMA_SDMA	Wakeup dependency from I2C2 module (SWakeup_dma signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
6:2	RESERVED		R	0x00
1	WKUPDEP_I2C2_IRQ_IPU	Wakeup dependency from I2C2 module (SWakeup_irq signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_I2C2_IRQ_MPU	Wakeup dependency from I2C2 module (SWakeup_irq signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-552. Register Call Summary for Register PM_L4PER_I2C2_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • CORE_PRM Register Summary: [3]

Table 3-553. RM_L4PER_I2C2_CONTEXT

Address Offset	0x0000 09AC		
Physical Address	0x4AE0 70AC	**Instance**	CORE_PRM
Description	This register contains dedicated I2C2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-554. Register Call Summary for Register RM_L4PER_I2C2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-555. PM_L4PER_I2C3_WKDEP

Address Offset	0x0000 09B0		
Physical Address	0x4AE0 70B0	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on I2C3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_I2C3_DMA_SDMA	RESERVED					WKUPDEP_I2C3_IRQ_IPU	WKUPDEP_I2C3_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7	WKUPDEP_I2C3_DMA_SDMA	Wakeup dependency from I2C3 module (SWakeup_dma signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
6:2	RESERVED		R	0x00
1	WKUPDEP_I2C3_IRQ_IPU	Wakeup dependency from I2C3 module (SWakeup_irq signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_I2C3_IRQ_MPU	Wakeup dependency from I2C3 module (SWakeup_irq signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Table 3-556. Register Call Summary for Register PM_L4PER_I2C3_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • CORE_PRM Register Summary: [3]

Table 3-557. RM_L4PER_I2C3_CONTEXT

Address Offset	0x0000 09B4		
Physical Address	0x4AE0 70B4	**Instance**	CORE_PRM
Description	This register contains dedicated I2C3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-558. Register Call Summary for Register RM_L4PER_I2C3_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-559. PM_L4PER_I2C4_WKDEP

Address Offset	0x0000 09B8		
Physical Address	0x4AE0 70B8	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on I2C4 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WKUPDEP_I2C4_DMA_SDMA	RESERVED					WKUPDEP_I2C4_IRQ_IPU	WKUPDEP_I2C4_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7	WKUPDEP_I2C4_DMA_SDMA	Wakeup dependency from I2C4 module (SWakeup_dma signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
6:2	RESERVED		R	0x00
1	WKUPDEP_I2C4_IRQ_IPU	Wakeup dependency from I2C4 module (SWakeup_irq signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_I2C4_IRQ_MPU	Wakeup dependency from I2C4 module (SWakeup_irq signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-560. Register Call Summary for Register PM_L4PER_I2C4_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • CORE_PRM Register Summary: [3]

Table 3-561. RM_L4PER_I2C4_CONTEXT

Address Offset	0x0000 09BC		
Physical Address	0x4AE0 70BC	**Instance**	CORE_PRM
Description	This register contains dedicated I2C4 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-562. Register Call Summary for Register RM_L4PER_I2C4_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-563. RM_L4PER_L4_PER_CONTEXT

Address Offset	0x0000 09C0		
Physical Address	0x4AE0 70C0	**Instance**	CORE_PRM
Description	This register contains dedicated L4_PER context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-564. Register Call Summary for Register RM_L4PER_L4_PER_CONTEXT

Power Management Functional Description • PD_CORE Description: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

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Table 3-565. PM_L4PER_MCSPI1_WKDEP

Address Offset	0x0000 09F0		
Physical Address	0x4AE0 70F0	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on MCSPI1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCSPI1_SDMA	WKUPDEP_MCSPI1_DSP	WKUPDEP_MCSPI1_IPU	WKUPDEP_MCSPI1_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_MCSPI1_SDMA	Wakeup dependency from MCSPI1 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MCSPI1_DSP	Wakeup dependency from MCSPI1 module (SWakeup signal) towards DSP + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_MCSPI1_IPU	Wakeup dependency from MCSPI1 module (SWakeup signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MCSPI1_MPU	Wakeup dependency from MCSPI1 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-566. Register Call Summary for Register PM_L4PER_MCSPI1_WKDEP

Clock Management Functional Description
- Wake-Up Dependency: [0] [1] [2] [3]

PRCM Register Manual
- CORE_PRM Register Summary: [4]

Table 3-567. RM_L4PER_MCSPI1_CONTEXT

Address Offset	0x0000 09F4		
Physical Address	0x4AE0 70F4	**Instance**	CORE_PRM
Description	This register contains dedicated MCSPI1 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-568. Register Call Summary for Register RM_L4PER_MCSPI1_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-569. PM_L4PER_MCSPI2_WKDEP

Address Offset	0x0000 09F8		
Physical Address	0x4AE0 70F8	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on MCSPI2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCSPI2_SDMA	RESERVED	WKUPDEP_MCSPI2_IPU	WKUPDEP_MCSPI2_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_MCSPI2_SDMA	Wakeup dependency from MCSPI2 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	RESERVED		R	0
1	WKUPDEP_MCSPI2_IPU	Wakeup dependency from MCSPI2 module (SWakeup signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	WKUPDEP_MCSPI2_MPU	Wakeup dependency from MCSPI2 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-570. Register Call Summary for Register PM_L4PER_MCSPI2_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • CORE_PRM Register Summary: [3]

Table 3-571. RM_L4PER_MCSPI2_CONTEXT

Address Offset	0x0000 09FC		
Physical Address	0x4AE0 70FC	**Instance**	CORE_PRM
Description	This register contains dedicated MCSPI2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-572. Register Call Summary for Register RM_L4PER_MCSPI2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-573. PM_L4PER_MCSPI3_WKDEP

Address Offset	0x0000 0A00		
Physical Address	0x4AE0 7100	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on MCSPI3 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCSPI3_SDMA	RESERVED		WKUPDEP_MCSPI3_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_MCSPI3_SDMA	Wakeup dependency from MCSPI3 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_MCSPI3_MPU	Wakeup dependency from MCSPI3 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-574. Register Call Summary for Register PM_L4PER_MCSPI3_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-575. RM_L4PER_MCSPI3_CONTEXT

Address Offset	0x0000 0A04		
Physical Address	0x4AE0 7104	**Instance**	CORE_PRM
Description	This register contains dedicated MCSPI3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-576. Register Call Summary for Register RM_L4PER_MCSPI3_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-577. PM_L4PER_MCSPI4_WKDEP

Address Offset	0x0000 0A08		
Physical Address	0x4AE0 7108	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on MCSPI4 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MCSPI4_SDMA	RESERVED		WKUPDEP_MCSPI4_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_MCSPI4_SDMA	Wakeup dependency from MCSPI4 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_MCSPI4_MPU	Wakeup dependency from MCSPI4 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-578. Register Call Summary for Register PM_L4PER_MCSPI4_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-579. RM_L4PER_MCSPI4_CONTEXT

Address Offset	0x0000 0A0C		
Physical Address	0x4AE0 710C	**Instance**	CORE_PRM
Description	This register contains dedicated MCSPI4 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-580. Register Call Summary for Register RM_L4PER_MCSPI4_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-581. PM_L4PER_GPIO7_WKDEP

Address Offset	0x0000 0A10		
Physical Address	0x4AE0 7110	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on GPIO7 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_GPIO7_IRQ1_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	WKUPDEP_GPIO7_IRQ1_MPU	Wakeup dependency from GPIO7 module (POINTRSWAKEUP1 signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

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Table 3-582. Register Call Summary for Register PM_L4PER_GPIO7_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-583. RM_L4PER_GPIO7_CONTEXT

Address Offset	0x0000 0A14		
Physical Address	0x4AE0 7114	**Instance**	CORE_PRM
Description	This register contains dedicated GPIO7 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-584. Register Call Summary for Register RM_L4PER_GPIO7_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-585. PM_L4PER_GPIO8_WKDEP

Address Offset	0x0000 0A18		
Physical Address	0x4AE0 7118	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on GPIO8 service requests.		
Type	RW		

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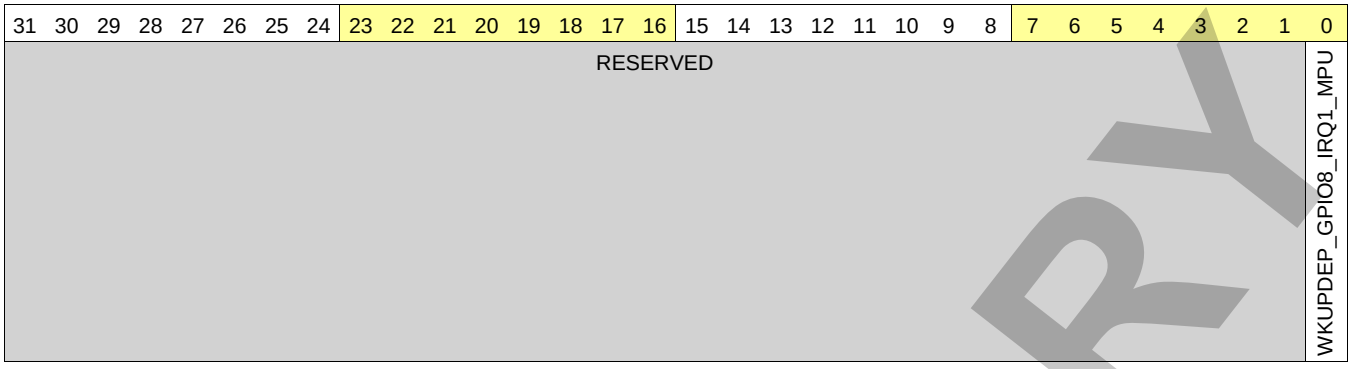


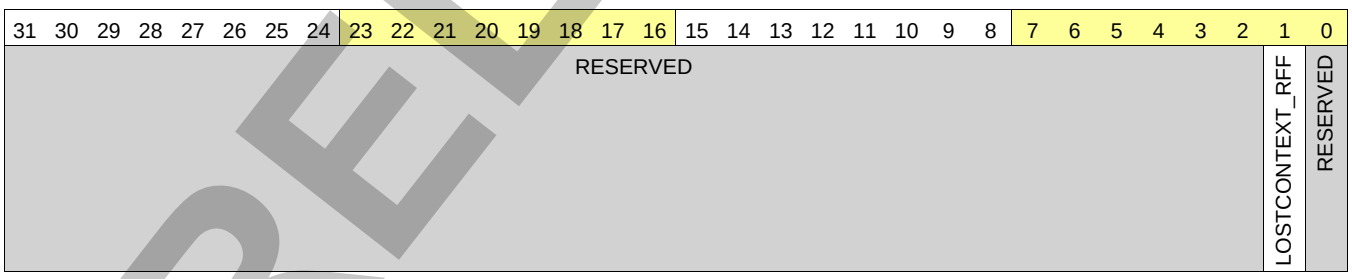
Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	WKUPDEP_GPIO8_IRQ1_MPU	Wakeup dependency from GPIO8 module (POINTRSWAKEUP1 signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

Table 3-586. Register Call Summary for Register PM_L4PER_GPIO8_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-587. RM_L4PER_GPIO8_CONTEXT

Address Offset	0x0000 0A1C		
Physical Address	0x4AE0 711C	**Instance**	CORE_PRM
Description	This register contains dedicated GPIO8 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

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Table 3-588. Register Call Summary for Register RM_L4PER_GPIO8_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-589. PM_L4PER_MMC3_WKDEP

Address Offset	0x0000 0A20		
Physical Address	0x4AE0 7120	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on MMC3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMC3_SDMA	RESERVED	WKUPDEP_MMC3_IPU	WKUPDEP_MMC3_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_MMC3_SDMA	Wakeup dependency from MMCSD3 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	RESERVED		R	0
1	WKUPDEP_MMC3_IPU	Wakeup dependency from MMCSD3 module (SWakeup signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MMC3_MPU	Wakeup dependency from MMCSD3 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-590. Register Call Summary for Register PM_L4PER_MMC3_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • CORE_PRM Register Summary: [3]

Table 3-591. RM_L4PER_MMC3_CONTEXT

Address Offset	0x0000 0A24		
Physical Address	0x4AE0 7124	**Instance**	CORE_PRM
Description	This register contains dedicated MMC3 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_NONRETAINED_BANK	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_NONRETAINED_BANK	Specify if memory-based context in NONRETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-592. Register Call Summary for Register RM_L4PER_MMC3_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-593. PM_L4PER_MMC4_WKDEP

Address Offset	0x0000 0A28		
Physical Address	0x4AE0 7128	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on MMC4 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMC4_SDMA	RESERVED	WKUPDEP_MMC4_MPU

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x000 0000
3	WKUPDEP_MMC4_SDMA	Wakeup dependency from MMCSD4 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED	Reserved	R	0x0
0	WKUPDEP_MMC4_MPU	Wakeup dependency from MMCSD4 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-594. Register Call Summary for Register PM_L4PER_MMC4_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-595. RM_L4PER_MMC4_CONTEXT

Address Offset	0x0000 0A2C		
Physical Address	0x4AE0 712C	**Instance**	CORE_PRM
Description	This register contains dedicated MMC4 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_NONRETAINED_BANK	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_NONRETAINED_BANK	Specify if memory-based context in NONRETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-596. Register Call Summary for Register RM_L4PER_MMC4_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-597. PM_L4PER_UART1_WKDEP

Address Offset	0x0000 0A40		
Physical Address	0x4AE0 7140	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on UART1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_UART1_SDMA	RESERVED		WKUPDEP_UART1_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_UART1_SDMA	Wakeup dependency from UART1 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_UART1_MPU	Wakeup dependency from UART1 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-598. Register Call Summary for Register PM_L4PER_UART1_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-599. RM_L4PER_UART1_CONTEXT

Address Offset	0x0000 0A44		
Physical Address	0x4AE0 7144	**Instance**	CORE_PRM
Description	This register contains dedicated UART1 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_RETAINED_BANK	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-600. Register Call Summary for Register RM_L4PER_UART1_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-601. PM_L4PER_UART2_WKDEP

Address Offset	0x0000 0A48		
Physical Address	0x4AE0 7148	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on UART2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_UART2_SDMA	RESERVED		WKUPDEP_UART2_MPU

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_UART2_SDMA	Wakeup dependency from UART2 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_UART2_MPU	Wakeup dependency from UART2 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-602. Register Call Summary for Register PM_L4PER_UART2_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-603. RM_L4PER_UART2_CONTEXT

Address Offset	0x0000 0A4C		
Physical Address	0x4AE0 714C	**Instance**	CORE_PRM
Description	This register contains dedicated UART2 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_RETAINED_BANK	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

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Table 3-604. Register Call Summary for Register RM_L4PER_UART2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-605. PM_L4PER_UART3_WKDEP

Address Offset	0x0000 0A50		
Physical Address	0x4AE0 7150	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on UART3 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_UART3_SDMA	WKUPDEP_UART3_DSP	WKUPDEP_UART3_IPU	WKUPDEP_UART3_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_UART3_SDMA	Wakeup dependency from UART3 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_UART3_DSP	Wakeup dependency from UART3 module (SWakeup signal) towards DSP + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_UART3_IPU	Wakeup dependency from UART3 module (SWakeup signal) towards IPU + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_UART3_MPU	Wakeup dependency from UART3 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-606. Register Call Summary for Register PM_L4PER_UART3_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2] [3]
PRCM Register Manual • CORE_PRM Register Summary: [4]

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Table 3-607. RM_L4PER_UART3_CONTEXT

Address Offset	0x0000 0A54		
Physical Address	0x4AE0 7154	**Instance**	CORE_PRM
Description	This register contains dedicated UART3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_RETAINED_BANK	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-608. Register Call Summary for Register RM_L4PER_UART3_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-609. RM_L4PER_UART4_CONTEXT

Address Offset	0x0000 0A58		
Physical Address	0x4AE0 7158	**Instance**	CORE_PRM
Description	This register contains dedicated UART4 context statuses. [warm reset insensitive]		
Type	RW		

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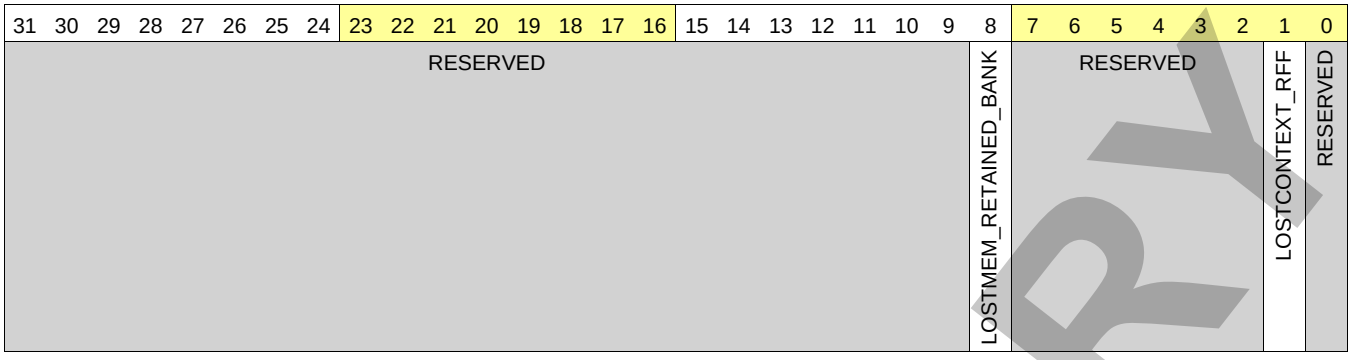


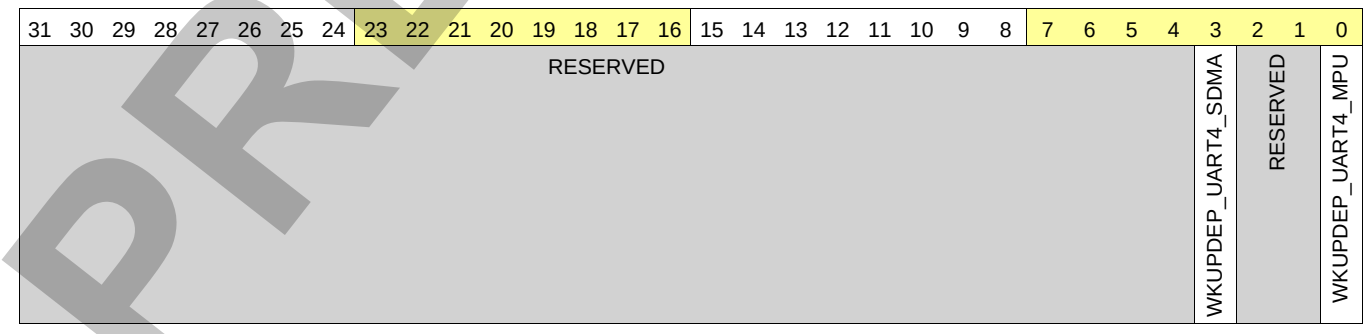
Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-610. Register Call Summary for Register RM_L4PER_UART4_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-611. PM_L4PER_UART4_WKDEP

Address Offset	0x0000 0A5C		
Physical Address	0x4AE0 715C	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on UART4 service requests.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_UART4_SDMA	Wakeup dependency from UART4 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_UART4_MPU	Wakeup dependency from UART4 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-612. Register Call Summary for Register PM_L4PER_UART4_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-613. PM_L4PER_MMC5_WKDEP

Address Offset	0x0000 0A60		
Physical Address	0x4AE0 7160	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on MMC5 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMC5_SDMA	RESERVED		WKUPDEP_MMC5_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x000 0000
3	WKUPDEP_MMC5_SDMA	Wakeup dependency from MMCSD5 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED	Reserved	R	0x0
0	WKUPDEP_MMC5_MPU	Wakeup dependency from MMCSD5 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-614. Register Call Summary for Register PM_L4PER_MMC5_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

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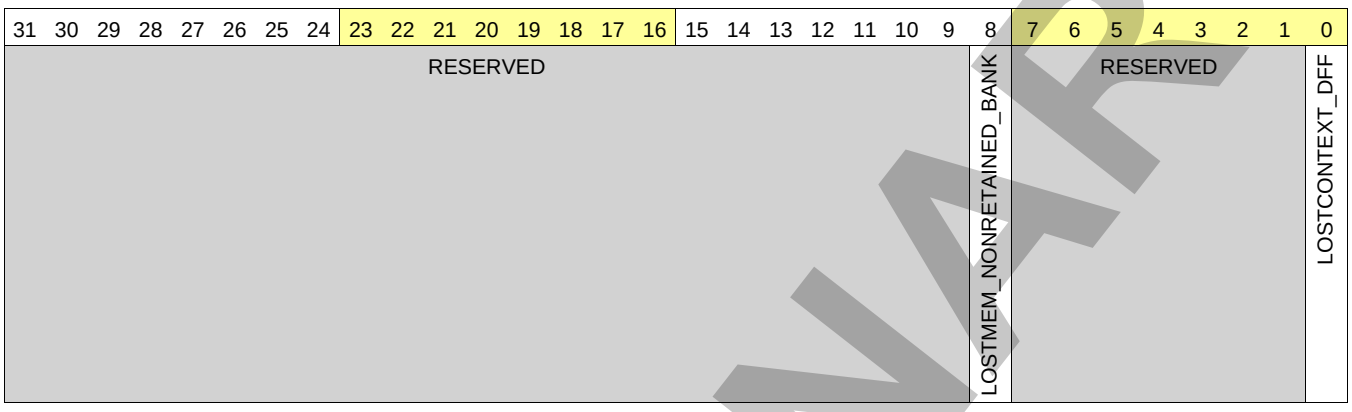
Table 3-615. RM_L4PER_MMC5_CONTEXT

Address Offset	0x0000 0A64		
Physical Address	0x4AE0 7164	**Instance**	CORE_PRM
Description	This register contains dedicated MMC5 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_NONRETAINED_BANK	Specify if memory-based context in NONRETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-616. Register Call Summary for Register RM_L4PER_MMC5_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-617. PM_L4PER_I2C5_WKDEP

Address Offset	0x0000 0A68		
Physical Address	0x4AE0 7168	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on I2C5 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_I2C5_IRQ_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_I2C5_IRQ_MPU	Wakeup dependency from I2C5 module (SWakeup_irq signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-618. Register Call Summary for Register PM_L4PER_I2C5_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-619. RM_L4PER_I2C5_CONTEXT

Address Offset	0x0000 0A6C		
Physical Address	0x4AE0 716C	**Instance**	CORE_PRM
Description	This register contains dedicated I2C5 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-620. Register Call Summary for Register RM_L4PER_I2C5_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-621. PM_L4PER_UART5_WKDEP

Address Offset	0x0000 0A70		
Physical Address	0x4AE0 7170	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on UART5 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_UART5_SDMA	RESERVED		WKUPDEP_UART5_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_UART5_SDMA	Wakeup dependency from UART5 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_UART5_MPU	Wakeup dependency from UART5 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-622. Register Call Summary for Register PM_L4PER_UART5_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-623. RM_L4PER_UART5_CONTEXT

Address Offset	0x0000 0A74		
Physical Address	0x4AE0 7174	**Instance**	CORE_PRM
Description	This register contains dedicated UART5 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_RETAINED_BANK	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-624. Register Call Summary for Register RM_L4PER_UART5_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-625. PM_L4PER_UART6_WKDEP

Address Offset	0x0000 0A78		
Physical Address	0x4AE0 7178	**Instance**	CORE_PRM
Description	This register controls wakeup dependency based on UART6 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_UART6_SDMA	RESERVED		WKUPDEP_UART6_MPU

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	WKUPDEP_UART6_SDMA	Wakeup dependency from UART6 module (SWakeup signal) towards SDMA + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2:1	RESERVED		R	0x0
0	WKUPDEP_UART6_MPU	Wakeup dependency from UART6 module (SWakeup signal) towards MPU + L3MAIN1 + L3MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-626. Register Call Summary for Register PM_L4PER_UART6_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • CORE_PRM Register Summary: [2]

Table 3-627. RM_L4PER_UART6_CONTEXT

Address Offset	0x0000 0A7C		
Physical Address	0x4AE0 717C	**Instance**	CORE_PRM
Description	This register contains dedicated UART6 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_RETAINED_BANK	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

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Table 3-628. Register Call Summary for Register RM_L4PER_UART6_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-629. RM_L4SEC_AES1_CONTEXT

Address Offset	0x0000 0AA4		
Physical Address	0x4AE0 71A4	**Instance**	CORE_PRM
Description	This register contains dedicated AES1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-630. Register Call Summary for Register RM_L4SEC_AES1_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-631. RM_L4SEC_AES2_CONTEXT

Address Offset	0x0000 0AAC		
Physical Address	0x4AE0 71AC	**Instance**	CORE_PRM
Description	This register contains dedicated AES2 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-632. Register Call Summary for Register RM_L4SEC_AES2_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-633. RM_L4SEC_DES3DES_CONTEXT

Address Offset	0x0000 0AB4		
Physical Address	0x4AE0 71B4	**Instance**	CORE_PRM
Description	This register contains dedicated DES3DES context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

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Table 3-634. Register Call Summary for Register RM_L4SEC_DES3DES_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-635. RM_L4SEC_FPKA_CONTEXT

Address Offset	0x0000 0ABC		
Physical Address	0x4AE0 71BC	**Instance**	CORE_PRM
Description	This register contains dedicated FPKA context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_NONRETAINED_BANK	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_NONRETAINED_BANK	Specify if memory-based context in NONRETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-636. Register Call Summary for Register RM_L4SEC_FPKA_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

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Table 3-637. RM_L4SEC_RNG_CONTEXT

Address Offset	0x0000 0AC4		
Physical Address	0x4AE0 71C4	**Instance**	CORE_PRM
Description	This register contains dedicated RNG context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-638. Register Call Summary for Register RM_L4SEC_RNG_CONTEXT

Power Management Functional Description
- PD_CORE Description: [0]

PRCM Register Manual
- CORE_PRM Register Summary: [1]

Table 3-639. RM_L4SEC_SHA2MD5_CONTEXT

Address Offset	0x0000 0ACC		
Physical Address	0x4AE0 71CC	**Instance**	CORE_PRM
Description	This register contains dedicated SHA2MD5 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-640. Register Call Summary for Register RM_L4SEC_SHA2MD5_CONTEXT

Power Management Functional Description • PD_CORE Description: [0]
PRCM Register Manual • CORE_PRM Register Summary: [1]

Table 3-641. RM_L4SEC_DMA_CRYPTO_CONTEXT

Address Offset	0x0000 0ADC		
Physical Address	0x4AE0 71DC	**Instance**	CORE_PRM
Description	This register contains dedicated DMA_CRYPTO context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_RETAINED_BANK	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_RETAINED_BANK	Specify if memory-based context in RETAINED_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CORE_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-642. Register Call Summary for Register RM_L4SEC_DMA_CRYPTO_CONTEXT

PRCM Register Manual • CORE_PRM Register Summary: [0]

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3.11.9 IVA_PRM Registers

3.11.9.1 IVA_PRM Register Summary

Table 3-643. IVA_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	IVA_PRM Base Address
PM_IVA_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 7200
PM_IVA_PWRSTST	RW	32	0x0000 0004	0x4AE0 7204
RM_IVA_RSTCTRL	RW	32	0x0000 0010	0x4AE0 7210
RM_IVA_RSTST	RW	32	0x0000 0014	0x4AE0 7214
RM_IVA_IVA_CONTEXT	RW	32	0x0000 0024	0x4AE0 7224
RM_IVA_SL2_CONTEXT	RW	32	0x0000 002C	0x4AE0 722C

3.11.9.2 IVA_PRM Register Description

Table 3-644. PM_IVA_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7200	**Instance**	IVA_PRM
Description	This register controls the IVA power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TCM2_MEM_ONSTATE		TCM1_MEM_ONSTATE		SL2_MEM_ONSTATE		HWA_MEM_ONSTATE		RESERVED				TCM2_MEM_RETSTATE		TCM1_MEM_RETSTATE		SL2_MEM_RETSTATE		HWA_MEM_RETSTATE		RESERVED		LOWPOWERSTATECHANGE		RESERVED		LOGICRETSTATE		POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:22	TCM2_MEM_ONSTATE	TCM2 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
21:20	TCM1_MEM_ONSTATE	TCM1 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
19:18	SL2_MEM_ONSTATE	SL2 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
17:16	HWA_MEM_ONSTATE	HWA memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:12	RESERVED		R	0x0
11	TCM2_MEM_RETSTATE	TCM2 memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1

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Bits	Field Name	Description	Type	Reset
10	TCM1_MEM_RETSTATE	TCM1 memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
9	SL2_MEM_RETSTATE	SL2 memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
8	HWA_MEM_RETSTATE	HWA memory state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION Read 0x0: Whole logic is off when the domain is in RETENTION state.	R	0
1:0	POWERSTATE	Power state control 0x0: Reserved 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

Table 3-645. Register Call Summary for Register PM_IVA_PWRSTCTRL

Power Management Functional Description • Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
PRCM Register Manual • IVA_PRM Register Summary: [11]

Table 3-646. PM_IVA_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 7204	**Instance**	IVA_PRM
Description	This register provides a status on the current IVA power domain state. [warm reset insensitive]		
Type	RW		

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31 30 29 28 27 26	25 24	23 22 21	20	19 18 17 16	15 14 13 12	11 10	9 8	7 6	5 4	3	2	1 0
RESERVED	LASTPOWERSTATEENTERED	RESERVED	INTRANSITION	RESERVED		TCM2_MEM_STATEST	TCM1_MEM_STATEST	SL2_MEM_STATEST	HWA_MEM_STATEST	RESERVED	LOGICSTATEST	POWERSTATEST

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Reserved	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:12	RESERVED		R	0x00
11:10	TCM2_MEM_STATEST	TCM2 memory state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
9:8	TCM1_MEM_STATEST	TCM1 memory state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	SL2_MEM_STATEST	SL2 memory state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
5:4	HWA_MEM_STATEST	HWA memory state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1

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Bits	Field Name	Description	Type	Reset
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-647. Register Call Summary for Register PM_IVA_PWRSTST

Power Management Functional Description • Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5] [6] [7]
PRCM Register Manual • IVA_PRM Register Summary: [8]

Table 3-648. RM_IVA_RSTCTRL

Address Offset	0x0000 0010		
Physical Address	0x4AE0 7210	**Instance**	IVA_PRM
Description	This register controls the release of the IVA sub-system resets.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													RST_LOGIC	RST_SEQ2	RST_SEQ1

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	RST_LOGIC	IVA logic and SL2 reset control 0x0: Reset is cleared for the IVA logic and SL2 0x1: Reset is asserted for IVA logic and SL2	RW	1
1	RST_SEQ2	IVA Sequencer2 reset control 0x0: Reset is cleared for IVA Sequencer CPU2 0x1: Reset is asserted for IVA Sequencer CPU2	RW	1
0	RST_SEQ1	IVA sequencer1 reset control 0x0: Reset is cleared for the IVA Sequencer CPU1 0x1: Reset is asserted for the IVA sequencer CPU1	RW	1

Table 3-649. Register Call Summary for Register RM_IVA_RSTCTRL

Reset Management Functional Description • Reset Domains: [0] [1] [2] [3] • IVA Subsystem Power-On Reset Sequence: [4] [5] [6] • IVA Subsystem Software Warm Reset Sequence: [7] [8] [9] [10] [11] [12]
PRCM Register Manual • IVA_PRM Register Summary: [13]

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Table 3-650. RM_IVA_RSTST

Address Offset	0x0000 0014		
Physical Address	0x4AE0 7214	**Instance**	IVA_PRM
Description	This register logs the different reset sources of the IVA domain. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ICECRUSHER_SEQ2_RST2ST	ICECRUSHER_SEQ1_RST1ST	EMULATION_SEQ2_RST2ST	EMULATION_SEQ1_RST1ST	RST3ST	RST2ST	RST1ST	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	RST_ICECRUSHER_SEQ2	Sequencer2 CPU has been reset due to IVA ICECRUSHER2 reset event 0x0: No icecrusher reset 0x1: Sequencer2 has been reset upon icecrusher reset	RW W1toClr	0
5	RST_ICECRUSHER_SEQ1	Sequencer1 CPU has been reset due to IVA ICECRUSHER1 reset event 0x0: No icecrusher reset 0x1: Sequencer1 has been reset upon icecrusher reset	RW W1toClr	0
4	RST_EMULATION_SEQ2	Sequencer2 CPU has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: Sequencer2 has been reset upon emulation reset	RW W1toClr	0
3	RST_EMULATION_SEQ1	Sequencer1 CPU has been reset due to emulation reset source e.g. assert reset command initiated by the icepick module 0x0: No emulation reset 0x1: Sequencer1 has been reset upon emulation reset	RW W1toClr	0
2	RST_LOGIC	IVA logic and SL2 SW reset 0x0: No SW reset occured 0x1: IVA logic and SL2 has been reset upon SW reset	RW W1toClr	0
1	RST_SEQ2	IVA Sequencer2 CPU SW reset 0x0: No SW reset occured 0x1: Sequencer2 has been reset upon SW reset	RW W1toClr	0
0	RST_SEQ1	IVA Sequencer1 CPU SW reset 0x0: No SW reset occured 0x1: Sequencer1 has been reset upon SW reset	RW W1toClr	0

Table 3-651. Register Call Summary for Register RM_IVA_RSTST

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- IVA_PRM Register Summary: [0]

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Table 3-652. RM_IVA_IVA_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 7224	**Instance**	IVA_PRM
Description	This register contains dedicated IVA context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					LOSTMEM_HWA_MEM	LOSTMEM_TCM2_MEM	LOSTMEM_TCM1_MEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	LOSTMEM_HWA_MEM	Specify if memory-based context in HWA_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
9	LOSTMEM_TCM2_MEM	Specify if memory-based context in TCM2_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
8	LOSTMEM_TCM1_MEM	Specify if memory-based context in TCM1_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of IVA_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-653. Register Call Summary for Register RM_IVA_IVA_CONTEXT

Power Management Functional Description
- PD_IVA Description: [0]

PRCM Register Manual
- IVA_PRM Register Summary: [1]

Table 3-654. RM_IVA_SL2_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4AE0 722C	**Instance**	IVA_PRM
Description	This register contains dedicated SL2 context statuses. [warm reset insensitive]		
Type	RW		

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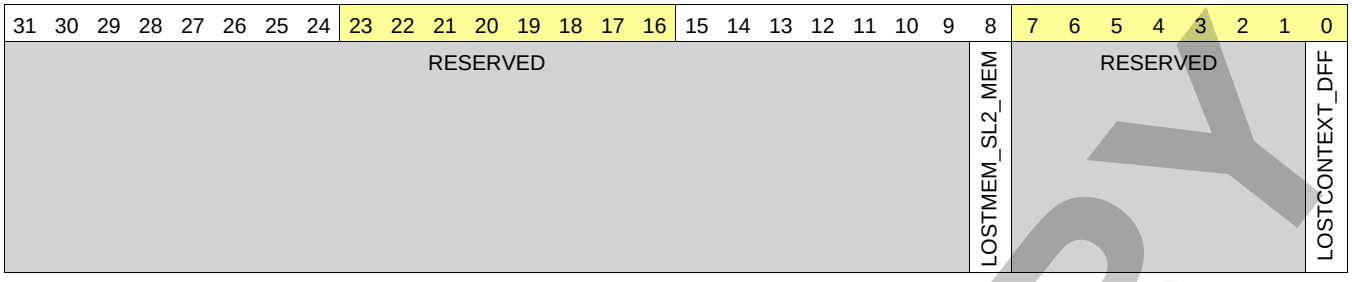

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_SL2_MEM	Specify if memory-based context in SL2_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of IVA_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-655. Register Call Summary for Register RM_IVA_SL2_CONTEXT

Power Management Functional Description • PD_IVA Description: [0]
PRCM Register Manual • IVA_PRM Register Summary: [1]

3.11.10 CAM_PRM Registers

3.11.10.1 CAM_PRM Register Summary

Table 3-656. CAM_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CAM_PRM Base Address
PM_CAM_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 7300
PM_CAM_PWRSTST	RW	32	0x0000 0004	0x4AE0 7304
RM_CAM_ISS_CONTEXT	RW	32	0x0000 0024	0x4AE0 7324
RM_CAM_FDIF_CONTEXT	RW	32	0x0000 002C	0x4AE0 732C
RESERVED	R	32	0x0000 0034	0x4AE0 7334

3.11.10.2 CAM_PRM Register Description

Table 3-657. PM_CAM_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7300	**Instance**	CAM_PRM
Description	This register controls the CAM power state to reach upon a domain sleep transition		
Type	RW		

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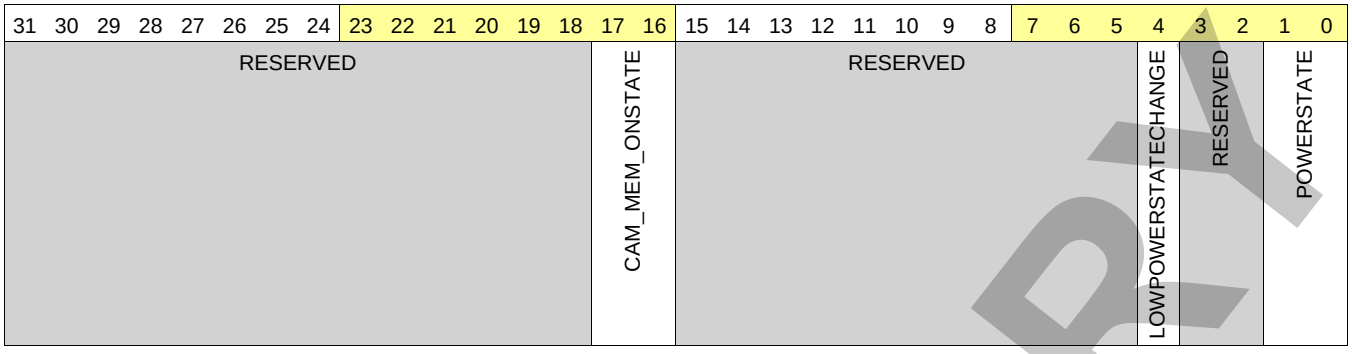

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	CAM_MEM_ONSTATE	CAM_MEM memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:5	RESERVED		R	0x000
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3:2	RESERVED		R	0x0
1:0	POWERSTATE	Power state control 0x0: Reserved Read 0x1: Reserved 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-658. Register Call Summary for Register PM_CAM_PWRSTCTRL

Power Management Functional Description • Logic and Memory Area Power Mode Control and Status: [0] [1] [2]
PRCM Register Manual • CAM_PRM Register Summary: [3]

Table 3-659. PM_CAM_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 7304	**Instance**	CAM_PRM
Description	This register provides a status on the current CAM power domain state. [warm reset insensitive]		
Type	RW		

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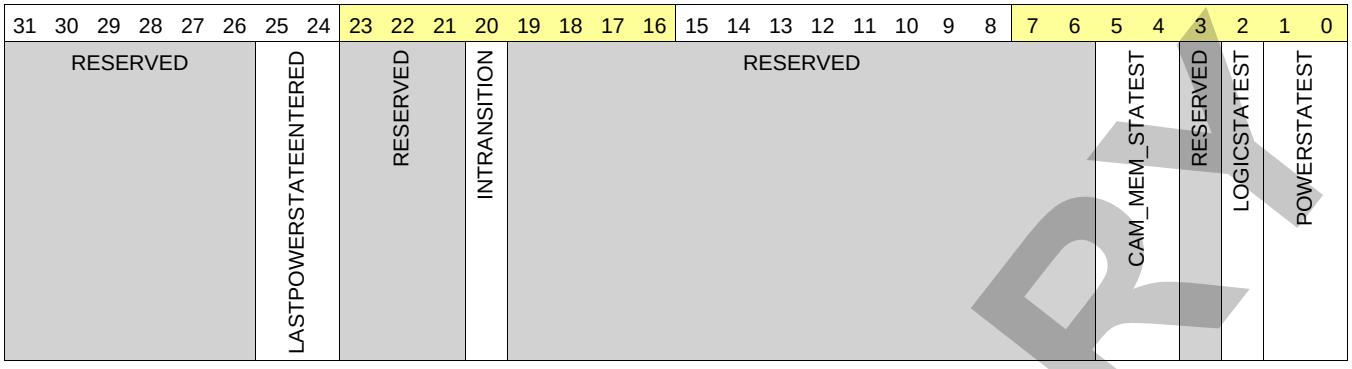

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x000
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x0: Reserved Read 0x1: Power domain was previously in RETENTION Read 0x2: Power domain was previously ON-INACTIVE Read 0x3: Power domain was previously ON-ACTIVE	RW W1toSet	0x0
23:21	RESERVED		R	0x000
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000
5:4	CAM_MEM_STATEST	CAM_MEM memory state status Read 0x0: Reserved Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-660. Register Call Summary for Register PM_CAM_PWRSTST

Power Management Functional Description
- Logic and Memory Area Power Mode Control and Status: [0] [1] [2] [3] [4]

PRCM Register Manual
- CAM_PRM Register Summary: [5]

Table 3-661. RM_CAM_ISS_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 7324	**Instance**	CAM_PRM
Description	This register contains dedicated ISS context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_CAM_MEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CAM_MEM	Specify if memory-based context in CAM_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CAM_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-662. Register Call Summary for Register RM_CAM_ISS_CONTEXT

Power Management Functional Description • PD_CAM Description: [0]
PRCM Register Manual • CAM_PRM Register Summary: [1]

Table 3-663. RM_CAM_FDIF_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4AE0 732C	**Instance**	CAM_PRM
Description	This register contains dedicated FDIF context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_CAM_MEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_CAM_MEM	Specify if memory-based context in CAM_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Bits	Field Name	Description	Type	Reset
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CAM_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-664. Register Call Summary for Register RM_CAM_FDIF_CONTEXT

Power Management Functional Description • PD_CAM Description: [0]
PRCM Register Manual • CAM_PRM Register Summary: [1]

3.11.11 DSS_PRM Registers

3.11.11.1 DSS_PRM Register Summary

Table 3-665. DSS_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS_PRM Base Address
PM_DSS_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 7400
PM_DSS_PWRSTST	RW	32	0x0000 0004	0x4AE0 7404
PM_DSS_DSS_WKDEP	RW	32	0x0000 0020	0x4AE0 7420
RM_DSS_DSS_CONTEXT	RW	32	0x0000 0024	0x4AE0 7424
RM_DSS_BB2D_CONTEXT	RW	32	0x0000 0034	0x4AE0 7434

3.11.11.2 DSS_PRM Register Description

Table 3-666. PM_DSS_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7400	**Instance**	DSS_PRM
Description	This register controls the DSS power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DSS_MEM_ONSTATE		RESERVED							DSS_MEM_RETSTATE	RESERVED			LOWPOWERSTATECHANGE	RESERVED	LOGICRETSTATE	POWERSTATE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	DSS_MEM_ONSTATE	DSS_MEM state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:9	RESERVED		R	0x00
8	DSS_MEM_RETSTATE	DSS_MEM state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION Read 0x0: Whole logic is off when the domain is in RETENTION state.	R	0
1:0	POWERSTATE	Power state control 0x0: Reserved 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-667. Register Call Summary for Register PM_DSS_PWRSTCTRL

Power Management Functional Description • Logic and Memory Area Power Mode Control and Status: [0] [1] [2] [3] [4]
PRCM Register Manual • DSS_PRM Register Summary: [5]

Table 3-668. PM_DSS_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 7404	**Instance**	DSS_PRM
Description	This register provides a status on the current DSS power domain state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED												DSS_MEM_STATEST		RESERVED		LOGICSTATEST		POWERSTATEST	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x0: Reserved Read 0x1: Power domain was previously in RETENTION Read 0x2: Power domain was previously ON-INACTIVE Read 0x3: Power domain was previously ON-ACTIVE	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000
5:4	DSS_MEM_STATEST	DSS_MEM state status Read 0x0: Reserved Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-669. Register Call Summary for Register PM_DSS_PWRSTST

Power Management Functional Description • Logic and Memory Area Power Mode Control and Status: [0] [1] [2] [3] [4]
PRCM Register Manual • DSS_PRM Register Summary: [5]

Table 3-670. PM_DSS_DSS_WKDEP

Address Offset	0x0000 0020		
Physical Address	0x4AE0 7420	**Instance**	DSS_PRM
Description	This register controls wakeup dependency based on DSS service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												WKUPDEP_HDMIDMA_SDMA	WKUPDEP_DSI1_C_SDMA	WKUPDEP_DSI1_C_DSP	WKUPDEP_DSI1_C_IPU	WKUPDEP_DSI1_C_MPU	WKUPDEP_HDMIIRQ_DSP	WKUPDEP_HDMIIRQ_IPU	WKUPDEP_HDMIIRQ_MPU	RESERVED				WKUPDEP_DSI1_A_SDMA	WKUPDEP_DSI1_A_DSP	WKUPDEP_DSI1_A_IPU	WKUPDEP_DSI1_A_MPU	WKUPDEP_DISPC_SDMA	WKUPDEP_DISPC_DSP	WKUPDEP_DISPC_IPU	WKUPDEP_DISPC_MPU

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	WKUPDEP_HDMIDMA_SDMA	Wakeup dependency from HDMI module (SWakeup_HDMI_dma signal) towards DMA_SYSTEM + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
18	WKUPDEP_DSI1_C_SDMA	Wakeup dependency from DSI1_C module (SWakeup_DSI1_C signal) towards DMA_SYSTEM + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0x0
17	WKUPDEP_DSI1_C_DSP	Wakeup dependency from DSI1_C module (SWakeup_DSI1_C signal) towards DSP + L3_MAIN1 + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0x0
16	WKUPDEP_DSI1_C_IPU	Wakeup dependency from DSI1_C module (SWakeup_DSI1_C signal) towards IPU + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0x0
15	WKUPDEP_DSI1_C_MPU	Wakeup dependency from DSI1_C module (SWakeup_DSI1_C signal) towards MPU + L3_MAIN1 + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0x0
14	WKUPDEP_HDMIIRQ_DSP	Wakeup dependency from HDMI module (SWakeup_HDMI_irq signal) towards DSP + L3_MAIN1 + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
13	WKUPDEP_HDMIIRQ_IPU	Wakeup dependency from HDMI module (SWakeup_HDMI_irq signal) towards IPU + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	WKUPDEP_HDMIIRQ_MPU	Wakeup dependency from HDMI module (SWakeup_HDMI_irq signal) towards MPU + L3_MAIN1 + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
11:8	RESERVED	Reserved	R	0
7	WKUPDEP_DSI1_A_SDMA	Wakeup dependency from DSI1_A module (SWakeup_DSI1_A signal) towards DMA_SYSTEM + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_DSI1_A_DSP	Wakeup dependency from DSI1_A module (SWakeup_DSI1_A signal) towards DSP + L3_MAIN1 + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5	WKUPDEP_DSI1_A_IPU	Wakeup dependency from DSI1_A module (SWakeup_DSI1_A signal) towards IPU + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
4	WKUPDEP_DSI1_A_MPU	Wakeup dependency from DSI1_A module (SWakeup_DSI1_A signal) towards MPU + L3_MAIN1 + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	WKUPDEP_DISPC_SDMA	Wakeup dependency from DISPC module (SWakeup_DISPC signal) towards DMA_SYSTEM + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_DISPC_DSP	Wakeup dependency from DISPC module (SWakeup_DISPC signal) towards DSP + L3_MAIN1 + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_DISPC_IPU	Wakeup dependency from DISPC module (SWakeup_DISPC signal) towards IPU + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_DISPC_MPU	Wakeup dependency from DISPC module (SWakeup_DISPC signal) towards MPU + L3_MAIN1 + L3_MAIN2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-671. Register Call Summary for Register PM_DSS_DSS_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
PRCM Register Manual • DSS_PRM Register Summary: [16]

Table 3-672. RM_DSS_DSS_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 7424	**Instance**	DSS_PRM
Description	This register contains dedicated DSS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_DSS_MEM	RESERVED						LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_DSS_MEM	Specify if memory-based context in DSS_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSS_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSS_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-673. Register Call Summary for Register RM_DSS_DSS_CONTEXT

Power Management Functional Description
- PD_DSS Description: [0] [1]

PRCM Register Manual
- DSS_PRM Register Summary: [2]

Table 3-674. RM_DSS_BB2D_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4AE0 7434	**Instance**	DSS_PRM
Description	This register contains dedicated BB2B context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_DSS_MEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_DSS_MEM	Specify if memory-based context in DSS_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSS_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-675. Register Call Summary for Register RM_DSS_BB2D_CONTEXT

Power Management Functional Description • PD_DSS Description: [0]
PRCM Register Manual • DSS_PRM Register Summary: [1]

3.11.12 GPU_PRM Registers

3.11.12.1 GPU_PRM Register Summary

Table 3-676. GPU_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPU_PRM Base Address
PM_GPU_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 7500
PM_GPU_PWRSTST	RW	32	0x0000 0004	0x4AE0 7504
RM_GPU_GPU_CONTEXT	RW	32	0x0000 0024	0x4AE0 7524

3.11.12.2 GPU_PRM Register Description

Table 3-677. PM_GPU_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7500	**Instance**	GPU_PRM
Description	This register controls the GPU power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														GPU_MEM_ONSTATE		RESERVED											LOWPOWERSTATECHANGE	RESERVED		POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	GPU_MEM_ONSTATE	GPU_MEM memory bank state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:5	RESERVED		R	0x000

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Bits	Field Name	Description	Type	Reset
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3:2	RESERVED		R	0x0
1:0	POWERSTATE	Power state control 0x0: Reserved 0x1: Reserved 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-678. Register Call Summary for Register PM_GPU_PWRSTCTRL

Power Management Functional Description • Logic and Memory Area Power Modes Control and Status: [0] [1] [2]
PRCM Register Manual • GPU_PRM Register Summary: [3]

Table 3-679. PM_GPU_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 7504	**Instance**	GPU_PRM
Description	This register provides a status on the current GPU power domain state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED												GPU_MEM_STATEST		RESERVED		LOGICSTATEST		POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x000
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x0: Reserved Read 0x1: Power domain was previously in RETENTION Read 0x2: Power domain was previously ON-INACTIVE Read 0x3: Power domain was previously ON-ACTIVE	RW W1toSet	0x0
23:21	RESERVED		R	0x000
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
5:4	GPU_MEM_STATEST	GPU_MEM memory bank state status Read 0x0: Reserved Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3-680. Register Call Summary for Register PM_GPU_PWRSTST

Power Management Functional Description • Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4]
PRCM Register Manual • GPU_PRM Register Summary: [5]

Table 3-681. RM_GPU_GPU_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 7524	**Instance**	GPU_PRM
Description	This register contains dedicated GPU context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_GPU_MEM	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_GPU_MEM	Specify if memory-based context in GPU_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of GPU_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Table 3-682. Register Call Summary for Register RM_GPU_GPU_CONTEXT

Power Management Functional Description • PD_GPU Description: [0]
PRCM Register Manual • GPU_PRM Register Summary: [1]

3.11.13 L3INIT_PRM Registers

3.11.13.1 L3INIT_PRM Register Summary

Table 3-683. L3INIT_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_PRM Base Address
PM_L3INIT_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 7600
PM_L3INIT_PWRSTST	RW	32	0x0000 0004	0x4AE0 7604
PM_L3INIT_MMC1_WKDEP	RW	32	0x0000 0028	0x4AE0 7628
RM_L3INIT_MMC1_CONTEXT	RW	32	0x0000 002C	0x4AE0 762C
PM_L3INIT_MMC2_WKDEP	RW	32	0x0000 0030	0x4AE0 7630
RM_L3INIT_MMC2_CONTEXT	RW	32	0x0000 0034	0x4AE0 7634
PM_L3INIT_HSI_WKDEP	RW	32	0x0000 0038	0x4AE0 7638
RM_L3INIT_HSI_CONTEXT	RW	32	0x0000 003C	0x4AE0 763C
RESERVED	R	32	0x0000 0040	0x4AE0 7640
RESERVED	R	32	0x0000 0044	0x4AE0 7644
PM_L3INIT_USB_HOST_HS_WKDEP	RW	32	0x0000 0058	0x4AE0 7658
RM_L3INIT_USB_HOST_HS_CONTEXT	RW	32	0x0000 005C	0x4AE0 765C
PM_L3INIT_USB_TLL_HS_WKDEP	RW	32	0x0000 0068	0x4AE0 7668
RM_L3INIT_USB_TLL_HS_CONTEXT	RW	32	0x0000 006C	0x4AE0 766C
RM_L3INIT_IEEE1500_2_OCP_CONTEXT	RW	32	0x0000 007C	0x4AE0 767C
PM_L3INIT_SATA_WKDEP	R	32	0x0000 0088	0x4AE0 7688
RM_L3INIT_SATA_CONTEXT	RW	32	0x0000 008C	0x4AE0 768C
RM_L3INIT_OCP2SCP1_CONTEXT	RW	32	0x0000 00E4	0x4AE0 76E4
RM_L3INIT_OCP2SCP3_CONTEXT	RW	32	0x0000 00EC	0x4AE0 76EC
PM_L3INIT_USB_OTG_SS_WKDEP	RW	32	0x0000 00F0	0x4AE0 76F0
RM_L3INIT_USB_OTG_SS_CONTEXT	RW	32	0x0000 00F4	0x4AE0 76F4

3.11.13.2 L3INIT_PRM Register Description

Table 3-684. PM_L3INIT_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7600	**Instance**	L3INIT_PRM
Description	This register controls the L3INIT power state to reach upon a domain sleep transition		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												L3INIT_BANK2_ONSTATE		L3INIT_BANK1_ONSTATE		RESERVED							L3INIT_BANK2_RETSTATE	L3INIT_BANK1_RETSTATE	RESERVED			LOWPOWERSTATECHANGE	RESERVED	LOGICRETSTATE		POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x0000
19:18	L3INIT_BANK2_ONSTATE	L3INIT BANK2 state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
17:16	L3INIT_BANK1_ONSTATE	L3INIT BANK1 state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:10	RESERVED		R	0x00
9	L3INIT_BANK2_RETSTATE	L3INIT BANK2 state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R	0x1
8	L3INIT_BANK1_RETSTATE	L3INIT BANK1 state when domain is RETENTION. Read 0x0: Memory bank is off when the domain is in the RETENTION state.	R	0
7:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW WSpecial	0
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1
1:0	POWERSTATE	Power state control 0x0: Reserved 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-685. Register Call Summary for Register PM_L3INIT_PWRSTCTRL

Power Management Functional Description
• Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5] [6]
PRCM Register Manual
• L3INIT_PRM Register Summary: [7]

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Table 3-686. PM_L3INIT_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 7604	**Instance**	L3INIT_PRM
Description	This register provides a status on the current L3INIT power domain state. [warm reset insensitive]		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4	3	2	1 0
RESERVED	LASTPOWERSTATEENTERED	RESERVED	INTRANSITION	RESERVED	L3INIT_BANK2_STATEST	L3INIT_BANK1_STATEST	RESERVED	LOGICSTATEST	POWERSTATEST

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Reserved	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:8	RESERVED		R	0x0000
7:6	L3INIT_BANK2_STATEST	L3INIT BANK2 state status Read 0x0: Reserved Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
5:4	L3INIT_BANK1_STATEST	L3INIT BANK1 state status Read 0x0: Reserved Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

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Table 3-687. Register Call Summary for Register PM_L3INIT_PWRSTST

Power Management Functional Description • Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4] [5]
PRCM Register Manual • L3INIT_PRM Register Summary: [6]

Table 3-688. PM_L3INIT_MMC1_WKDEP

Address Offset	0x0000 0028		
Physical Address	0x4AE0 7628	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on MMC1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMC1_SDMA	WKUPDEP_MMC1_DSP	WKUPDEP_MMC1_IPU	WKUPDEP_MMC1_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MMC1_SDMA	Wakeup dependency from MMC1 module (SWakeup signal) towards DMA_SYSTEM + L3_MAIN2 + L4_PER clock domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MMC1_DSP	Wakeup dependency from MMC1 module (SWakeup signal) towards DSP + L3_MAIN1 + L3_MAIN2 + L4_PER clock domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_MMC1_IPU	Wakeup dependency from MMC1 module (SWakeup signal) towards IPU + L3_MAIN2 + L4_PER clock domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MMC1_MPU	Wakeup dependency from MMC1 module (SWakeup signal) towards MPU + L3_MAIN1 + L3_MAIN2 + L4_PER clock domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-689. Register Call Summary for Register PM_L3INIT_MMC1_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2] [3]
PRCM Register Manual • L3INIT_PRM Register Summary: [4]

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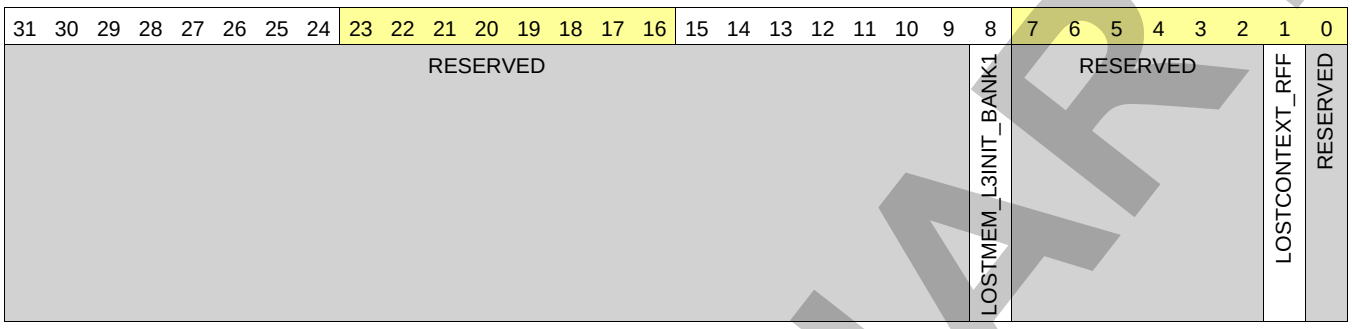
Table 3-690. RM_L3INIT_MMC1_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4AE0 762C	**Instance**	L3INIT_PRM
Description	This register contains dedicated MMC1 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_L3INIT_BANK1	Specify if memory-based context in L3INIT_BANK1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-691. Register Call Summary for Register RM_L3INIT_MMC1_CONTEXT

Power Management Functional Description
- PD_L3INIT Description: [0]

PRCM Register Manual
- L3INIT_PRM Register Summary: [1]

Table 3-692. PM_L3INIT_MMC2_WKDEP

Address Offset	0x0000 0030		
Physical Address	0x4AE0 7630	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on MMC2 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WKUPDEP_MMC2_SDMA	WKUPDEP_MMC2_DSP	WKUPDEP_MMC2_IPU	WKUPDEP_MMC2_MPU

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	WKUPDEP_MMC2_SDMA	Wakeup dependency from MMC2 module (SWakeup signal) towards DMA_SYSTEM + L3_MAIN2 + L4_PER clock domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_MMC2_DSP	Wakeup dependency from MMC2 module (SWakeup signal) towards DSP + L3_MAIN1 + L3_MAIN2 + L4_PER clock domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_MMC2_IPU	Wakeup dependency from MMC2 module (SWakeup signal) towards IPU + L3_MAIN2 + L4_PER clock domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_MMC2_MPU	Wakeup dependency from MMC2 module (SWakeup signal) towards MPU + L3_MAIN1 + L3_MAIN2 + L4_PER clock domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-693. Register Call Summary for Register PM_L3INIT_MMC2_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2] [3]
PRCM Register Manual • L3INIT_PRM Register Summary: [4]

Table 3-694. RM_L3INIT_MMC2_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4AE0 7634	**Instance**	L3INIT_PRM
Description	This register contains dedicated MMC2 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_L3INIT_BANK1	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_L3INIT_BANK1	Specify if memory-based context in L3INIT_BANK1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-695. Register Call Summary for Register RM_L3INIT_MMC2_CONTEXT

Power Management Functional Description • PD_L3INIT Description: [0]
PRCM Register Manual • L3INIT_PRM Register Summary: [1]

Table 3-696. PM_L3INIT_HSI_WKDEP

Address Offset	0x0000 0038		
Physical Address	0x4AE0 7638	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on HSI service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_HSI_DSP_DSP	RESERVED					WKUPDEP_HSI_MCU_IPU	WKUPDEP_HSI_MCU_MPU

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000
6	WKUPDEP_HSI_DSP_DSP	Wakeup dependency from HSI module (SWakeup_DSP signal) towards DSP + L3MAIN1 + L4CFG domains 0x0: Dependency is disabled Read 0x1: Dependency is enabled	RW	1
5:2	RESERVED		R	0x0
1	WKUPDEP_HSI_MCU_IPU	Wakeup dependency from HSI module (SWakeup_MPU signal) towards IPU + L3MAIN2 + L3MAIN1 + L4CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_HSI_MCU_MPU	Wakeup dependency from HSI module (SWakeup_MPU signal) towards MPU + L3MAIN1 + L4CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-697. Register Call Summary for Register PM_L3INIT_HSI_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • L3INIT_PRM Register Summary: [3]

Table 3-698. RM_L3INIT_HSI_CONTEXT

Address Offset	0x0000 003C		
Physical Address	0x4AE0 763C	**Instance**	L3INIT_PRM
Description	This register contains dedicated HSI context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_L3INIT_BANK1	RESERVED						LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_L3INIT_BANK1	Specify if memory-based context in L3INIT_BANK1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

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Bits	Field Name	Description	Type	Reset
0	RESERVED		R	0

Table 3-699. Register Call Summary for Register RM_L3INIT_HSI_CONTEXT

Power Management Functional Description • PD_L3INIT Description: [0]
PRCM Register Manual • L3INIT_PRM Register Summary: [1]

Table 3-700. PM_L3INIT_USB_HOST_HS_WKDEP

Address Offset	0x0000 0058		
Physical Address	0x4AE0 7658	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on USB_HOST_HS service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_USB_HOST_HS_IPU	WKUPDEP_USB_HOST_HS_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_USB_HOST_HS_IPU	Wakeup dependency from USB_HOST_HS module (SWakeup signal) towards IPU + L3_MAIN2 + L3_MAIN1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_USB_HOST_HS_MPU	Wakeup dependency from USB_HOST_HS module (SWakeup signal) towards MPU + L3_MAIN1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-701. Register Call Summary for Register PM_L3INIT_USB_HOST_HS_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • L3INIT_PRM Register Summary: [2]

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Table 3-702. RM_L3INIT_USB_HOST_HS_CONTEXT

Address Offset	0x0000 005C		
Physical Address	0x4AE0 765C	**Instance**	L3INIT_PRM
Description	This register contains dedicated USB_HOST_HS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-703. Register Call Summary for Register RM_L3INIT_USB_HOST_HS_CONTEXT

Power Management Functional Description
- PD_L3INIT Description: [0]

PRCM Register Manual
- L3INIT_PRM Register Summary: [1]

Table 3-704. PM_L3INIT_USB_TLL_HS_WKDEP

Address Offset	0x0000 0068		
Physical Address	0x4AE0 7668	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on USB_TLL_HS service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_USB_TLL_HS_IPU	WKUPDEP_USB_TLL_HS_MPU

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_USB_TLL_HS_IPU	Wakeup dependency from USB_TLL_HS module (SWakeup signal) towards IPU + L3_MAIN2 + L3_MAIN1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_USB_TLL_HS_MPU	Wakeup dependency from USB_TLL_HS module (SWakeup signal) towards MPU + L3_MAIN1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-705. Register Call Summary for Register PM_L3INIT_USB_TLL_HS_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • L3INIT_PRM Register Summary: [2]

Table 3-706. RM_L3INIT_USB_TLL_HS_CONTEXT

Address Offset	0x0000 006C		
Physical Address	0x4AE0 766C	**Instance**	L3INIT_PRM
Description	This register contains dedicated USB_TLL_HS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LOSTCONTEXT_RFF	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-707. Register Call Summary for Register RM_L3INIT_USB_TLL_HS_CONTEXT

Power Management Functional Description • PD_L3INIT Description: [0]
PRCM Register Manual • L3INIT_PRM Register Summary: [1]

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Table 3-708. RM_L3INIT_IEEE1500_2_OCP_CONTEXT

Address Offset	0x0000 007C		
Physical Address	0x4AE0 767C	**Instance**	L3INIT_PRM
Description	This register contains dedicated IEEE1500_2_OCP context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-709. Register Call Summary for Register RM_L3INIT_IEEE1500_2_OCP_CONTEXT

Power Management Functional Description
- PD_L3INIT Description: [0]

PRCM Register Manual
- L3INIT_PRM Register Summary: [1]

Table 3-710. PM_L3INIT_SATA_WKDEP

Address Offset	0x0000 0088		
Physical Address	0x4AE0 7688	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on SATA service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_SATA_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	WKUPDEP_SATA_MPU	Wakeup dependency from SATA module (SWakeup signal) towards MPU + L3MAIN1 + L4CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Table 3-711. Register Call Summary for Register PM_L3INIT_SATA_WKDEP

Clock Management Functional Description
- Wake-Up Dependency: [0]

PRCM Register Manual
- L3INIT_PRM Register Summary: [1]

Table 3-712. RM_L3INIT_SATA_CONTEXT

Address Offset	0x0000 008C		
Physical Address	0x4AE0 768C	**Instance**	L3INIT_PRM
Description	This register contains dedicated SATA context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_L3INIT_BANK1	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_L3INIT_BANK1	Specify if memory-based context in L3INIT_BANK1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-713. Register Call Summary for Register RM_L3INIT_SATA_CONTEXT

Power Management Functional Description
- PD_L3INIT Description: [0]

PRCM Register Manual
- L3INIT_PRM Register Summary: [1]

Table 3-714. RM_L3INIT_OCP2SCP1_CONTEXT

Address Offset	0x0000 00E4		
Physical Address	0x4AE0 76E4	**Instance**	L3INIT_PRM
Description	This register contains dedicated OCP2SCP1 context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-715. Register Call Summary for Register RM_L3INIT_OCP2SCP1_CONTEXT

Power Management Functional Description • PD_L3INIT Description: [0]
PRCM Register Manual • L3INIT_PRM Register Summary: [1]

Table 3-716. RM_L3INIT_OCP2SCP3_CONTEXT

Address Offset	0x0000 00EC		
Physical Address	0x4AE0 76EC	**Instance**	L3INIT_PRM
Description	This register contains dedicated OCP2SCP3 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-717. Register Call Summary for Register RM_L3INIT_OCP2SCP3_CONTEXT

Power Management Functional Description • PD_L3INIT Description: [0]
PRCM Register Manual • L3INIT_PRM Register Summary: [1]

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Table 3-718. PM_L3INIT_USB_OTG_SS_WKDEP

Address Offset	0x0000 00F0		
Physical Address	0x4AE0 76F0	**Instance**	L3INIT_PRM
Description	This register controls wakeup dependency based on USB_OTG_SS service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WKUPDEP_USB_OTG_SS_IPU	WKUPDEP_USB_OTG_SS_MPU

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WKUPDEP_USB_OTG_SS_IPU	Wakeup dependency from USB_OTG_SS module (SWakeup signal) towards IPU + L3_MAIN2 + L3_MAIN1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_USB_OTG_SS_MPU	Wakeup dependency from USB_OTG_SS module (SWakeup signal) towards MPU + L3_MAIN1 + L4_CFG domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-719. Register Call Summary for Register PM_L3INIT_USB_OTG_SS_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1]
PRCM Register Manual • L3INIT_PRM Register Summary: [2]

Table 3-720. RM_L3INIT_USB_OTG_SS_CONTEXT

Address Offset	0x0000 00F4		
Physical Address	0x4AE0 76F4	**Instance**	L3INIT_PRM
Description	This register contains dedicated USB_OTG_SS context statuses. [warm reset insensitive]		
Type	RW		

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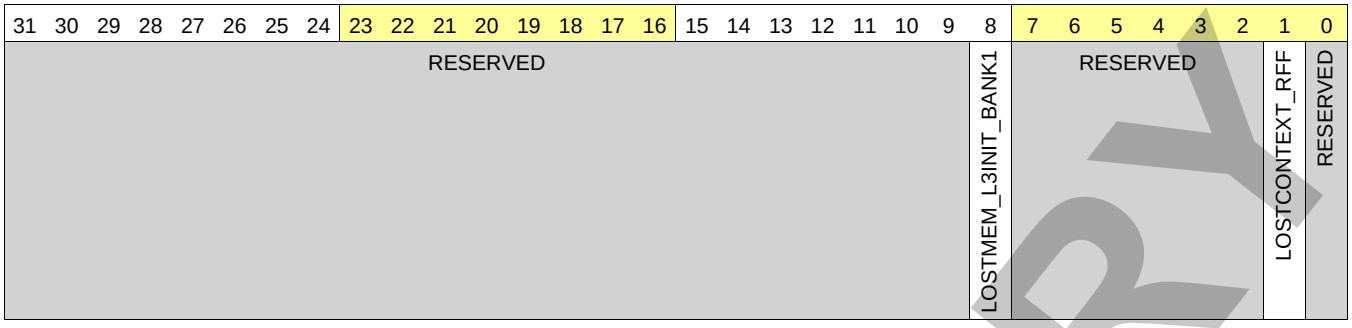

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_L3INIT_BANK1	Specify if memory-based context in L3INIT_BANK1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of L3INIT_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
0	RESERVED		R	0

Table 3-721. Register Call Summary for Register RM_L3INIT_USB_OTG_SS_CONTEXT

Power Management Functional Description • PD_L3INIT Description: [0]
PRCM Register Manual • L3INIT_PRM Register Summary: [1]

3.11.14 CUSTEFUSE_PRM Registers

3.11.14.1 CUSTEFUSE_PRM Register Summary

Table 3-722. CUSTEFUSE_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CUSTEFUSE_PRM Base Address
PM_CUSTEFUSE_PWRSTCTRL	RW	32	0x0000 0000	0x4AE0 7700
PM_CUSTEFUSE_PWRSTST	RW	32	0x0000 0004	0x4AE0 7704
RM_CUSTEFUSE_EFUSE_CTRL_CUST_CONTEXT	RW	32	0x0000 0024	0x4AE0 7724

3.11.14.2 CUSTEFUSE_PRM Register Description

Table 3-723. PM_CUSTEFUSE_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7700	**Instance**	CUSTEFUSE_PRM
Description	This register controls the EFUSE_CTRL_CUST power state to reach upon a domain sleep transition		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											LOWPOWERSTATECHANGE	RESERVED		POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain. 0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.	RW	0
3:2	RESERVED		R	0x0
1:0	POWERSTATE	Power state control 0x0: Reserved 0x1: Reserved 0x2: INACTIVE state 0x3: ON State	RW	0x0

Table 3-724. Register Call Summary for Register PM_CUSTEFUSE_PWRSTCTRL

Power Management Functional Description • Logic and Memory Area Power Modes Control and Status: [0] [1]
PRCM Register Manual • CUSTEFUSE_PRM Register Summary: [2]

Table 3-725. PM_CUSTEFUSE_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 7704	**Instance**	CUSTEFUSE_PRM
Description	This register provides a status on the current EFUSE_CTRL_CUST power domain state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED																		LOGICSTATEST	POWERSTATEST	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION Read 0x0: Reserved	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x1: Power domain transition is in progress. Read 0x0: No on-going transition on power domain	R	0
19:3	RESERVED		R	0x0 0000
2	LOGICSTATEST	Logic state status Read 0x1: Logic in domain is ON Read 0x0: Logic in domain is OFF	R	1
1:0	POWERSTATEST	Current power state status Read 0x3: Power domain is ON-ACTIVE Read 0x2: Power domain is ON-INACTIVE Read 0x1: Power domain is in RETENTION Read 0x0: Reserved	R	0x3

Table 3-726. Register Call Summary for Register PM_CUSTEFUSE_PWRSTST

Power Management Functional Description • Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3]
PRCM Register Manual • CUSTEFUSE_PRM Register Summary: [4]

Table 3-727. RM_CUSTEFUSE_EFUSE_CTRL_CUST_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 7724	**Instance**	CUSTEFUSE_PRM
Description	This register contains dedicated EFUSE_CTRL_CUST module context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of CUSTEFUSE_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-728. Register Call Summary for Register RM_CUSTEFUSE_EFUSE_CTRL_CUST_CONTEXT

Power Management Functional Description • PD_CUSTEFUSE Description: [0]
PRCM Register Manual • CUSTEFUSE_PRM Register Summary: [1]

3.11.15 WKUPAON_PRM Registers

3.11.15.1 WKUPAON_PRM Register Summary

Table 3-729. WKUPAON_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	WKUPAON_PRM Base Address
RM_WKUPAON_L4_WKUP_CONTEXT	RW	32	0x0000 0024	0x4AE0 7824
RESERVED	RW	32	0x0000 002C	0x4AE0 782C
PM_WKUPAON_WD_TIMER2_WKDEP	RW	32	0x0000 0030	0x4AE0 7830
RM_WKUPAON_WD_TIMER2_CONTEXT	RW	32	0x0000 0034	0x4AE0 7834
PM_WKUPAON_GPIO1_WKDEP	RW	32	0x0000 0038	0x4AE0 7838
RM_WKUPAON_GPIO1_CONTEXT	RW	32	0x0000 003C	0x4AE0 783C
PM_WKUPAON_TIMER1_WKDEP	R	32	0x0000 0040	0x4AE0 7840
RM_WKUPAON_TIMER1_CONTEXT	RW	32	0x0000 0044	0x4AE0 7844
RESERVED	RW	32	0x0000 0048	0x4AE0 7848
RESERVED	RW	32	0x0000 004C	0x4AE0 784C
RM_WKUPAON_COUNTER_32K_CONTEXT	RW	32	0x0000 0054	0x4AE0 7854
RM_WKUPAON_SAR_RAM_CONTEXT	RW	32	0x0000 0064	0x4AE0 7864
PM_WKUPAON_KBD_WKDEP	RW	32	0x0000 0078	0x4AE0 7878
RM_WKUPAON_KBD_CONTEXT	RW	32	0x0000 007C	0x4AE0 787C

3.11.15.2 WKUPAON_PRM Register Description

Table 3-730. RM_WKUPAON_L4_WKUP_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 7824	**Instance**	WKUPAON_PRM
Description	This register contains dedicated L4_WKUP context statuses. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUPAON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-731. Register Call Summary for Register RM_WKUPAON_L4_WKUP_CONTEXT

Power Management Functional Description • PD_WKUPAON Description: [0]
PRCM Register Manual • WKUPAON_PRM Register Summary: [1]

Table 3-732. PM_WKUPAON_WD_TIMER2_WKDEP

Address Offset	0x0000 0030		
Physical Address	0x4AE0 7830	**Instance**	WKUPAON_PRM
Description	This register controls wakeup dependency based on WD_TIMER2 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_WD_TIMER2_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_WD_TIMER2_MPU	Wakeup dependency from WD_TIMER2 module (SWakeup signal) towards MPU + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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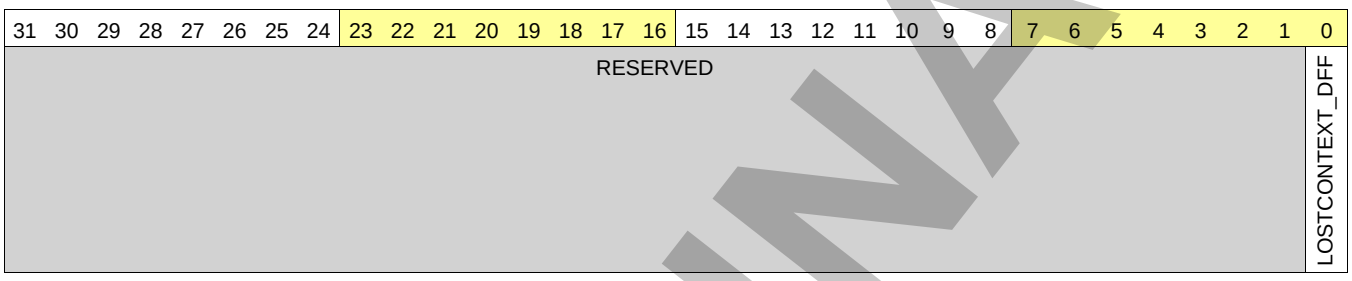
Table 3-733. Register Call Summary for Register PM_WKUPAON_WD_TIMER2_WKDEP

Clock Management Functional Description
- Wake-Up Dependency: [0]

PRCM Register Manual
- WKUPAON_PRM Register Summary: [1]

Table 3-734. RM_WKUPAON_WD_TIMER2_CONTEXT

Address Offset	0x0000 0034		
Physical Address	0x4AE0 7834	**Instance**	WKUPAON_PRM
Description	This register contains dedicated WD_TIMER2 context statuses. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUPAON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-735. Register Call Summary for Register RM_WKUPAON_WD_TIMER2_CONTEXT

Power Management Functional Description
- PD_WKUPAON Description: [0]

PRCM Register Manual
- WKUPAON_PRM Register Summary: [1]

Table 3-736. PM_WKUPAON_GPIO1_WKDEP

Address Offset	0x0000 0038		
Physical Address	0x4AE0 7838	**Instance**	WKUPAON_PRM
Description	This register controls wakeup dependency based on GPIO1 service requests.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									WKUPDEP_GPIO1_IRQ2_DSP	RESERVED					WKUPDEP_GPIO1_IRQ1_IPU	WKUPDEP_GPIO1_IRQ1_MPU

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	WKUPDEP_GPIO1_IRQ2_DSP	Wakeup dependency from GPIO1 module (POINTRSWAKEUP2 signal) towards DSP + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5:2	RESERVED		R	0x0
1	WKUPDEP_GPIO1_IRQ1_IPU	Wakeup dependency from GPIO1 module (POINTRSWAKEUP1 signal) module towards IPU + L3_MAIN2 + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_GPIO1_IRQ1_MPU	Wakeup dependency from GPIO1 module (POINTRSWAKEUP1 signal) towards MPU + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-737. Register Call Summary for Register PM_WKUPAON_GPIO1_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0] [1] [2]
PRCM Register Manual • WKUPAON_PRM Register Summary: [3]

Table 3-738. RM_WKUPAON_GPIO1_CONTEXT

Address Offset	0x0000 003C		
Physical Address	0x4AE0 783C	**Instance**	WKUPAON_PRM
Description	This register contains dedicated GPIO1 context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUPAON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-739. Register Call Summary for Register RM_WKUPAON_GPIO1_CONTEXT

Power Management Functional Description • PD_WKUPAON Description: [0]
PRCM Register Manual • WKUPAON_PRM Register Summary: [1]

Table 3-740. PM_WKUPAON_TIMER1_WKDEP

Address Offset	0x0000 0040		
Physical Address	0x4AE0 7840	**Instance**	WKUPAON_PRM
Description	This register controls wakeup dependency based on TIMER1 service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_TIMER1_MPU

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_TIMER1_MPU	Wakeup dependency from TIMER1 module (SWakeup signal) towards MPU + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

Table 3-741. Register Call Summary for Register PM_WKUPAON_TIMER1_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • WKUPAON_PRM Register Summary: [1]

Table 3-742. RM_WKUPAON_TIMER1_CONTEXT

Address Offset	0x0000 0044		
Physical Address	0x4AE0 7844	**Instance**	WKUPAON_PRM
Description	This register contains dedicated TIMER1 context statuses. [warm reset insensitive]		
Type	RW		

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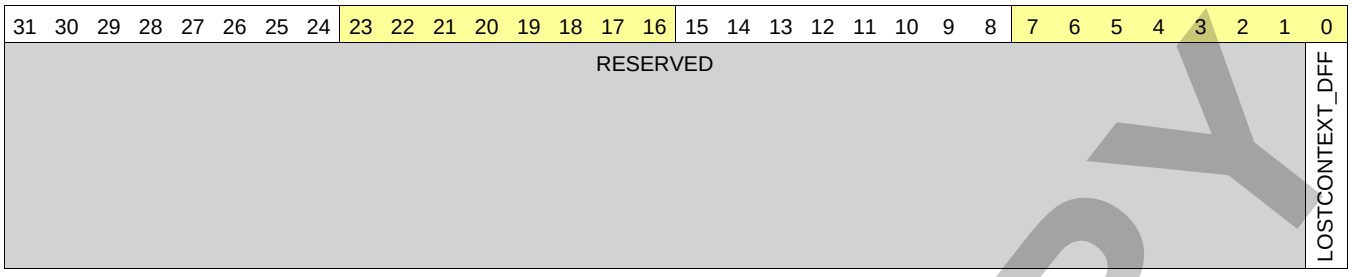


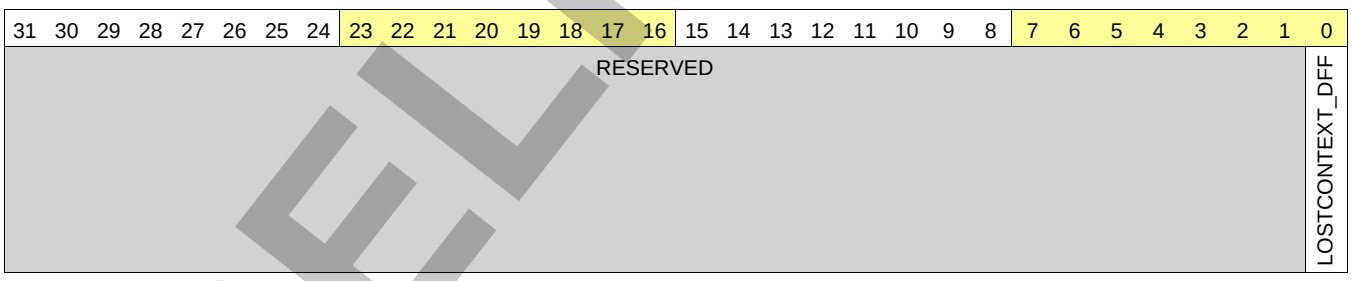
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUPAON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-743. Register Call Summary for Register RM_WKUPAON_TIMER1_CONTEXT

Power Management Functional Description • PD_WKUPAON Description: [0]
PRCM Register Manual • WKUPAON_PRM Register Summary: [1]

Table 3-744. RM_WKUPAON_COUNTER_32K_CONTEXT

Address Offset	0x0000 0054		
Physical Address	0x4AE0 7854	**Instance**	WKUPAON_PRM
Description	This register contains dedicated COUNTER_32K context statuses.This bit-field is only sensitive to the external power-on reset (SYS_PWRON_RST reset line)		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUPAON_SYS_PWRON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-745. Register Call Summary for Register RM_WKUPAON_COUNTER_32K_CONTEXT

Power Management Functional Description • PD_WKUPAON Description: [0]
PRCM Register Manual • WKUPAON_PRM Register Summary: [1]

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Table 3-746. RM_WKUPAON_SAR_RAM_CONTEXT

Address Offset	0x0000 0064		
Physical Address	0x4AE0 7864	**Instance**	WKUPAON_PRM
Description	This register contains dedicated SAR_RAM context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_WKUP_BANK	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_WKUP_BANK	Specify if memory-based context in WKUP_BANK memory bank has been lost due to a previous global cold reset. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUPAON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-747. Register Call Summary for Register RM_WKUPAON_SAR_RAM_CONTEXT

Power Management Functional Description
- PD_WKUPAON Description: [0]

PRCM Register Manual
- WKUPAON_PRM Register Summary: [1]

Table 3-748. PM_WKUPAON_KBD_WKDEP

Address Offset	0x0000 0078		
Physical Address	0x4AE0 7878	**Instance**	WKUPAON_PRM
Description	This register controls wakeup dependency based on KBD service requests.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKUPDEP_KBD_MPU

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WKUPDEP_KBD_MPU	Wakeup dependency from KBD module (SWakeup signal) towards MPU + L3_MAIN1 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

Table 3-749. Register Call Summary for Register PM_WKUPAON_KBD_WKDEP

Clock Management Functional Description • Wake-Up Dependency: [0]
PRCM Register Manual • WKUPAON_PRM Register Summary: [1]

Table 3-750. RM_WKUPAON_KBD_CONTEXT

Address Offset	0x0000 007C		
Physical Address	0x4AE0 787C	**Instance**	WKUPAON_PRM
Description	This register contains dedicated KBD context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of WKUPAON_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-751. Register Call Summary for Register RM_WKUPAON_KBD_CONTEXT

Power Management Functional Description • PD_WKUPAON Description: [0]
PRCM Register Manual • WKUPAON_PRM Register Summary: [1]

3.11.16 WKUPAON_CM Registers

3.11.16.1 WKUPAON_CM Register Summary

Table 3-752. WKUPAON_CM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	WKUPAON_CM Base Address
CM_WKUPAON_CLKSTCTRL	RW	32	0x0000 0000	0x4AE0 7900

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Table 3-752. WKUPAON_CM Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	WKUPAON_CM Base Address
CM_WKUPAON_L4_WKUP_CLKCTRL	R	32	0x0000 0020	0x4AE0 7920
RESERVED	R	32	0x0000 0028	0x4AE0 7928
CM_WKUPAON_WD_TIMER2_CLKCTRL	RW	32	0x0000 0030	0x4AE0 7930
CM_WKUPAON_GPIO1_CLKCTRL	RW	32	0x0000 0038	0x4AE0 7938
CM_WKUPAON_TIMER1_CLKCTRL	RW	32	0x0000 0040	0x4AE0 7940
RESERVED	R	32	0x0000 0048	0x4AE0 7948
CM_WKUPAON_COUNTER_32K_CLKCTRL	R	32	0x0000 0050	0x4AE0 7950
CM_WKUPAON_SAR_RAM_CLKCTRL	R	32	0x0000 0060	0x4AE0 7960
CM_WKUPAON_KBD_CLKCTRL	RW	32	0x0000 0078	0x4AE0 7978
CM_WKUPAON_SCRM_CLKCTRL	RW	32	0x0000 0090	0x4AE0 7990
CM_WKUPAON_IO_SRCOMP_CLKCTRL	RW	32	0x0000 0098	0x4AE0 7998

3.11.16.2 WKUPAON_CM Register Description

Table 3-753. CM_WKUPAON_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7900	**Instance**	WKUPAON_CM
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLKACTIVITY_SYS_CLK_ALL	CLKACTIVITY_SYS_CLK_FUNC	CLKACTIVITY_WKUPAON_IO_SRCOMP_GFCLK	CLKACTIVITY_WKUPAON_GICLK	CLKACTIVITY_WKUPAON_32K_GFCLK	RESERVED	CLKACTIVITY_ABE_LP_CLK	CLKACTIVITY_SYS_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	CLKACTIVITY_SYS_CLK_ALL	This field indicates the state of the SYS_CLK runing at SCRM level because of any SCRM clock request. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0

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Bits	Field Name	Description	Type	Reset
14	CLKACTIVITY_SYS_CLK_FUNC	This field indicates the state of the functional SYS_CLK clocks in the domain (this exclude activity of EMU_SYS_GCLK clock). [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
13	CLKACTIVITY_WKUPAON_IO_SRCOMP_GFCLK	This field indicates the state of the WKUPAON_IO_SRCOMP_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
12	CLKACTIVITY_L4_WKUPAON_GICLK	This field indicates the state of the WKUPAON_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
11	CLKACTIVITY_WKUPAON_32K_GFCLK	This field indicates the state of the WKUPAON_32K_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
10	RESERVED		R	0
9	CLKACTIVITY_ABE_LP_CLK	This field indicates the state of the ABE_LP_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
8	CLKACTIVITY_SYS_CLK	This field indicates the state of the SYS_CLK clock in the domain (it includes profiling, EMU_SYS_GCLK and all functional SYS_CLK). [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the WKUPAON clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-754. Register Call Summary for Register CM_WKUPAON_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7]

PRCM Register Manual
- WKUPAON_CM Register Summary: [8]
- WKUPAON_CM Register Description: [9] [10]

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Table 3-755. CM_WKUPAON_L4_WKUP_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4AE0 7920	**Instance**	WKUPAON_CM
Description	This register manages the WKUPAON clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_WKUPAON_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-756. Register Call Summary for Register CM_WKUPAON_L4_WKUP_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- WKUPAON_CM Register Summary: [2]
- WKUPAON_CM Register Description: [3] [4]

Table 3-757. CM_WKUPAON_WD_TIMER2_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4AE0 7930	**Instance**	WKUPAON_CM
Description	This register manages the WD_TIMER2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-758. Register Call Summary for Register CM_WKUPAON_WD_TIMER2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • WKUPAON_CM Register Summary: [2]

Table 3-759. CM_WKUPAON_GPIO1_CLKCTRL

Address Offset	0x0000 0038		
Physical Address	0x4AE0 7938	**Instance**	WKUPAON_CM
Description	This register manages the GPIO1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3

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Bits	Field Name	Description	Type	Reset
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_WKUPAON_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-760. Register Call Summary for Register CM_WKUPAON_GPIO1_CLKCTRL

Clock Management Functional Description • Clock Domain Modes: [0] • Clock Domain Module Attributes: [1] [2]
PRCM Register Manual • WKUPAON_CM Register Summary: [3]

Table 3-761. CM_WKUPAON_TIMER1_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4AE0 7940	**Instance**	WKUPAON_CM
Description	This register manages the TIMER1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-762. Register Call Summary for Register CM_WKUPAON_TIMER1_CLKCTRL

Clock Management Functional Description
- CD_PRM_TIMER Overview: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- WKUPAON_CM Register Summary: [3]

Table 3-763. CM_WKUPAON_COUNTER_32K_CLKCTRL

Address Offset	0x0000 0050		
Physical Address	0x4AE0 7950	**Instance**	WKUPAON_CM
Description	This register manages the COUNTER_32K clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_WKUPAON_L4_WKUP_CLKCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-764. Register Call Summary for Register CM_WKUPAON_COUNTER_32K_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • WKUPAON_CM Register Summary: [2]

Table 3-765. CM_WKUPAON_SAR_RAM_CLKCTRL

Address Offset	0x0000 0060		
Physical Address	0x4AE0 7960	**Instance**	WKUPAON_CM
Description	This register manages the SAR_RAM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_WKUPAON_L4_WKUP_CLKCTRL[1:0]CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

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Table 3-766. Register Call Summary for Register CM_WKUPAON_SAR_RAM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • WKUPAON_CM Register Summary: [2]

Table 3-767. CM_WKUPAON_KBD_CLKCTRL

Address Offset	0x0000 0078		
Physical Address	0x4AE0 7978	**Instance**	WKUPAON_CM
Description	This register manages the KBD clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-768. Register Call Summary for Register CM_WKUPAON_KBD_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • WKUPAON_CM Register Summary: [2]

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Table 3-769. CM_WKUPAON_SCRM_CLKCTRL

Address Offset	0x0000 0090		
Physical Address	0x4AE0 7990	**Instance**	WKUPAON_CM
Description	This register manages the SCRM clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						OPTFCLKEN_SCRM_PER	OPTFCLKEN_SCRM_CORE	RESERVED							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	OPTFCLKEN_SCRM_PER	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_SCRM_CORE	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:0	RESERVED		R	0x00

Table 3-770. Register Call Summary for Register CM_WKUPAON_SCRM_CLKCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1]

PRCM Register Manual
- WKUPAON_CM Register Summary: [2]

Table 3-771. CM_WKUPAON_IO_SRCOMP_CLKCTRL

Address Offset	0x0000 0098		
Physical Address	0x4AE0 7998	**Instance**	WKUPAON_CM
Description	This register manages the clock delivered to the IO Slew rate compensation cells. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKEN_SRCOMP_FCLK	RESERVED							

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	CLKEN_SRCOMP_FCLK	Functional clock control. 0x0: Functional clock is disabled 0x1: Functional clock is enabled.	RW	0
7:0	RESERVED		R	0x00

Table 3-772. Register Call Summary for Register CM_WKUPAON_IO_SRCOMP_CLKCTRL

Clock Management Functional Description • Specific properties and signals.: [0] [1] • Clock Domain Modes: [2]
PRCM Register Manual • WKUPAON_CM Register Summary: [3]

3.11.17 EMU_PRM Registers

3.11.17.1 EMU_PRM Register Summary

Table 3-773. EMU_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMU_PRM Base Address
PM_EMU_PWRSTCTRL	R	32	0x0000 0000	0x4AE0 7A00
PM_EMU_PWRSTST	RW	32	0x0000 0004	0x4AE0 7A04
RM_EMU_DEBUGSS_CONTEXT	RW	32	0x0000 0024	0x4AE0 7A24

3.11.17.2 EMU_PRM Register Description

Table 3-774. PM_EMU_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7A00	**Instance**	EMU_PRM
Description	This register controls the EMU power state to reach upon a domain sleep transition		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	EMU_BANK_ONSTATE	RESERVED	POWERSTATE

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	EMU_BANK_ONSTATE	EMU memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R	0x3
15:2	RESERVED		R	0x0000
1:0	POWERSTATE	Power state control Read 0x0: Reserved	R	0x0

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Table 3-775. Register Call Summary for Register PM_EMU_PWRSTCTRL

Power Management Functional Description
- Logic and Memory Area Power Modes Control and Status: [0] [1]

PRCM Register Manual
- EMU_PRM Register Summary: [2]

Table 3-776. PM_EMU_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 7A04	**Instance**	EMU_PRM
Description	This register provides a status on the EMU domain current power state. [warm reset insensitive]		
Type	RW		

31 30 29 28 27 26	25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4	3	2	1 0
RESERVED	LASTPOWERSTATEENTERED	RESERVED	INTRANSITION	RESERVED		EMU_BANK_STATEST	RESERVED	LOGICSTATEST	POWERSTATEST

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x000
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x0: Reserved Read 0x1: Power domain was previously in RETENTION Read 0x2: Power domain was previously ON-INACTIVE Read 0x3: Power domain was previously ON-ACTIVE	RW W1toSet	0x000
23:21	RESERVED		R	0x000
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000
5:4	EMU_BANK_STATEST	EMU memory bank state status Read 0x0: Reserved Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON It is supplied by WKUP LDO	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Reserved Read 0x3: Power domain is ON-ACTIVE	R	0x3

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Table 3-777. Register Call Summary for Register PM_EMU_PWRSTST

Power Management Functional Description
• Logic and Memory Area Power Modes Control and Status: [0] [1] [2] [3] [4]
PRCM Register Manual
• EMU_PRM Register Summary: [5]

Table 3-778. RM_EMU_DEBUGSS_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4AE0 7A24	**Instance**	EMU_PRM
Description	This register contains dedicated DEBUGSS context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_EMU_BANK	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	LOSTMEM_EMU_BANK	Specify if memory-based context in EMU_BANK memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of EMU_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 3-779. Register Call Summary for Register RM_EMU_DEBUGSS_CONTEXT

Power Management Functional Description
• PD_EMU Description: [0]
PRCM Register Manual
• EMU_PRM Register Summary: [1]

3.11.18 EMU_CM Registers

3.11.18.1 EMU_CM Register Summary

Table 3-780. EMU_CM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMU_CM Base Address
CM_EMU_CLKSTCTRL	RW	32	0x0000 0000	0x4AE0 7B00
CM_EMU_DYNAMICDEP	RW	32	0x0000 0008	0x4AE0 7B08

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Table 3-780. EMU_CM Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	EMU_CM Base Address
CM_EMU_DEBUGSS_CLKCTRL	R	32	0x0000 0020	0x4AE0 7B20
CM_EMU_MPU_EMU_DBG_CLKCTRL	R	32	0x0000 0028	0x4AE0 7B28

3.11.18.2 EMU_CM Register Description

Table 3-781. CM_EMU_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7B00	**Instance**	EMU_CM
Description	This register enables the EMU domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_EMU_SYS_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x0000000
8	CLKACTIVITY_EMU_SYS_CLK	This field indicates the state of the EMU_SYS_CLK clock in the domain. Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the EMU clock domain. Read 0x0: Reserved Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x2

Table 3-782. Register Call Summary for Register CM_EMU_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1]

PRCM Register Manual
- EMU_CM Register Summary: [2]
- EMU_CM Register Description: [3]

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Table 3-783. CM_EMU_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4AE0 7B08	**Instance**	EMU_CM
Description	This register controls the dynamic domain depedencies from EMU domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED																	L3MAIN2_DYNDEP	RESERVED						

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:7	RESERVED		R	0x00000
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3_MAIN2 clock domain Read 0x1: Dependency is enabled	R	1
5:0	RESERVED		R	0x00

Table 3-784. Register Call Summary for Register CM_EMU_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [0]
PRCM Register Manual • EMU_CM Register Summary: [1]

Table 3-785. CM_EMU_DEBUGSS_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4AE0 7B20	**Instance**	EMU_CM
Description	This register manages the DEBUGSS clocks. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x000
18	STBYST	Module standby status Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_EMU_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-786. Register Call Summary for Register CM_EMU_DEBUGSS_CLKCTRL

PRCM Register Manual
- EMU_CM Register Summary: [0]

Table 3-787. CM_EMU_MPU_EMU_DBG_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4AE0 7B28	**Instance**	EMU_CM
Description	This register manages the MPU_EMU_DBG clocks. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only INTERCONN part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including INTERCONN	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTERCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-788. Register Call Summary for Register CM_EMU_MPU_EMU_DBG_CLKCTRL

PRCM Register Manual
- EMU_CM Register Summary: [0]

3.11.19 DEVICE_PRM Registers

3.11.19.1 DEVICE_PRM Register Summary

Table 3-789. DEVICE_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DEVICE_PRM Base Address
PRM_RSTCTRL	RW	32	0x0000 0000	0x4AE0 7C00
PRM_RSTST	RW	32	0x0000 0004	0x4AE0 7C04
PRM_RSTTIME	RW	32	0x0000 0008	0x4AE0 7C08
PRM_CLKREQCTRL	RW	32	0x0000 000C	0x4AE0 7C0C
PRM_VOLTCTRL	RW	32	0x0000 0010	0x4AE0 7C10
PRM_PWRREQCTRL	RW	32	0x0000 0014	0x4AE0 7C14
PRM_PSCON_COUNT	RW	32	0x0000 0018	0x4AE0 7C18
PRM_IO_COUNT	RW	32	0x0000 001C	0x4AE0 7C1C
PRM_IO_PMCTRL	RW	32	0x0000 0020	0x4AE0 7C20
PRM_VOLTSETUP_WARMRESET	RW	32	0x0000 0024	0x4AE0 7C24
PRM_VOLTSETUP_CORE_OFF	RW	32	0x0000 0028	0x4AE0 7C28
PRM_VOLTSETUP_MPU_OFF	RW	32	0x0000 002C	0x4AE0 7C2C
PRM_VOLTSETUP_MM_OFF	RW	32	0x0000 0030	0x4AE0 7C30
PRM_VOLTSETUP_CORE_RET_SLEEP	RW	32	0x0000 0034	0x4AE0 7C34
PRM_VOLTSETUP_MPU_RET_SLEEP	RW	32	0x0000 0038	0x4AE0 7C38
PRM_VOLTSETUP_MM_RET_SLEEP	RW	32	0x0000 003C	0x4AE0 7C3C
PRM_VP_CORE_CONFIG	RW	32	0x0000 0040	0x4AE0 7C40
PRM_VP_CORE_STATUS	R	32	0x0000 0044	0x4AE0 7C44
PRM_VP_CORE_VLIMITTO	RW	32	0x0000 0048	0x4AE0 7C48
PRM_VP_CORE_VOLTAGE	RW	32	0x0000 004C	0x4AE0 7C4C
PRM_VP_CORE_VSTEPMAX	RW	32	0x0000 0050	0x4AE0 7C50
PRM_VP_CORE_VSTEPMIN	RW	32	0x0000 0054	0x4AE0 7C54
PRM_VP_MPU_CONFIG	RW	32	0x0000 0058	0x4AE0 7C58
PRM_VP_MPU_STATUS	R	32	0x0000 005C	0x4AE0 7C5C
PRM_VP_MPU_VLIMITTO	RW	32	0x0000 0060	0x4AE0 7C60
PRM_VP_MPU_VOLTAGE	RW	32	0x0000 0064	0x4AE0 7C64
PRM_VP_MPU_VSTEPMAX	RW	32	0x0000 0068	0x4AE0 7C68
PRM_VP_MPU_VSTEPMIN	RW	32	0x0000 006C	0x4AE0 7C6C
PRM_VP_MM_CONFIG	RW	32	0x0000 0070	0x4AE0 7C70
PRM_VP_MM_STATUS	R	32	0x0000 0074	0x4AE0 7C74

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Table 3-789. DEVICE_PRM Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DEVICE_PRM Base Address
PRM_VP_MM_VLIMITTO	RW	32	0x0000 0078	0x4AE0 7C78
PRM_VP_MM_VOLTAGE	RW	32	0x0000 007C	0x4AE0 7C7C
PRM_VP_MM_VSTEPMAX	RW	32	0x0000 0080	0x4AE0 7C80
PRM_VP_MM_VSTEPMIN	RW	32	0x0000 0084	0x4AE0 7C84
PRM_VC_SMPS_CORE_CONFIG	RW	32	0x0000 0088	0x4AE0 7C88
PRM_VC_SMPS_MM_CONFIG	RW	32	0x0000 008C	0x4AE0 7C8C
PRM_VC_SMPS_MPU_CONFIG	RW	32	0x0000 0090	0x4AE0 7C90
PRM_VC_VAL_CMD_VDD_CORE_L	RW	32	0x0000 0094	0x4AE0 7C94
PRM_VC_VAL_CMD_VDD_MM_L	RW	32	0x0000 0098	0x4AE0 7C98
PRM_VC_VAL_CMD_VDD_MPU_L	RW	32	0x0000 009C	0x4AE0 7C9C
PRM_VC_VAL_BYPASS	RW	32	0x0000 00A0	0x4AE0 7CA0
PRM_VC_CORE_ERRST	RW	32	0x0000 00A4	0x4AE0 7CA4
PRM_VC_MM_ERRST	RW	32	0x0000 00A8	0x4AE0 7CA8
PRM_VC_MPU_ERRST	RW	32	0x0000 00AC	0x4AE0 7CAC
PRM_VC_BYPASS_ERRST	RW	32	0x0000 00B0	0x4AE0 7CB0
PRM_VC_CFG_I2C_MODE	RW	32	0x0000 00B4	0x4AE0 7CB4
PRM_VC_CFG_I2C_CLK	RW	32	0x0000 00B8	0x4AE0 7CB8
PRM_SRAM_COUNT	RW	32	0x0000 00BC	0x4AE0 7CBC
RESERVED	R	32	0x0000 00C0	0x4AE0 7CC0
PRM_SLDO_CORE_SETUP	RW	32	0x0000 00C4	0x4AE0 7CC4
PRM_SLDO_CORE_CTRL	RW	32	0x0000 00C8	0x4AE0 7CC8
PRM_SLDO_MPU_SETUP	RW	32	0x0000 00CC	0x4AE0 7CCC
PRM_SLDO_MPU_CTRL	RW	32	0x0000 00D0	0x4AE0 7CD0
PRM_SLDO_MM_SETUP	RW	32	0x0000 00D4	0x4AE0 7CD4
PRM_SLDO_MM_CTRL	RW	32	0x0000 00D8	0x4AE0 7CD8
PRM_ABBLDO_MPU_SETUP	RW	32	0x0000 00DC	0x4AE0 7CDC
PRM_ABBLDO_MPU_CTRL	RW	32	0x0000 00E0	0x4AE0 7CE0
PRM_ABBLDO_MM_SETUP	RW	32	0x0000 00E4	0x4AE0 7CE4
PRM_ABBLDO_MM_CTRL	RW	32	0x0000 00E8	0x4AE0 7CE8
PRM_BANDGAP_SETUP	RW	32	0x0000 00EC	0x4AE0 7CEC
Reserved	R	32	0x0000 00F0	0x4AE0 7CF0
Reserved	R	32	0x0000 00F4	0x4AE0 7CF4
Reserved	R	32	0x0000 00F8	0x4AE0 7CF8
Reserved	R	32	0x0000 00FC	0x4AE0 7CFC
RESERVED	3	32	0x0000 0100	0x4AE0 7D00
PRM_VOLTST_MPU	R	32	0x0000 0110	0x4AE0 7D10
PRM_VOLTST_MM	R	32	0x0000 0114	0x4AE0 7D14

3.11.19.2 DEVICE_PRM Register Description

Table 3-790. PRM_RSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7C00	**Instance**	DEVICE_PRM
Description	Global software cold and warm reset control. This register is auto-cleared. Only write 1 is possible. A read returns 0 only.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														RST_GLOBAL_COLD_SW	RST_GLOBAL_WARM_SW

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	RST_GLOBAL_COLD_SW	Global COLD software reset control. This bit is reset only upon a global cold source of reset. 0x0: Global COLD software reset is cleared. 0x1: Triggers a global COLD software reset.	RW	0
0	RST_GLOBAL_WARM_SW	Global WARM software reset control. This bit is reset upon any global source of reset (warm and cold). 0x0: Global warm software reset is cleared. 0x1: Triggers a global warm software reset.	RW	0

Table 3-791. Register Call Summary for Register PRM_RSTCTRL

Reset Management Functional Description • Global Reset Sources: [0] [1]
PRCM Register Manual • DEVICE_PRM Register Summary: [2]

Table 3-792. PRM_RSTST

Address Offset	0x0000 0004		
Physical Address	0x4AE0 7C04	**Instance**	DEVICE_PRM
Description	This register logs the global reset sources. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TSHUT_CORE_RST	TSHUT_MM_RST	TSHUT_MPU_RST	RESERVED	ICEPICK_RST	VDD_CORE_VOLT_MGR_RST	VDD_MM_VOLT_MGR_RST	VDD_MPU_VOLT_MGR_RST	EXTERNAL_WARM_RST	RESERVED	MPU_WDT_RST	RESERVED	GLOBAL_WARM_SW_RST	GLOBAL_COLD_RST

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x000000
13	TSHUT_CORE_RST	TSHUT_CORE warm reset event. This is a source of global WARM reset. 0x0: No TSHUT_CORE reset 0x1: TSHUT_CORE reset has occurred.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
12	TSHUT_MM_RST	TSHUT_MM warm reset event. This is a source of global WARM reset. 0x0: No TSHUT_MM reset 0x1: TSHUT_MM reset has occurred.	RW W1toClr	0
11	TSHUT_MPU_RST	TSHUT_MPU warm reset event. This is a source of global WARM reset. 0x0: No TSHUT_MPU reset 0x1: TSHUT_MPU reset has occurred.	RW W1toClr	0
10	RESERVED		R	0
9	ICEPICK_RST	IcePick reset event. This is a source of global warm reset initiated by the emulation. 0x0: No ICEPICK reset. 0x1: IcePick reset has occurred.	RW W1toClr	0
8	VDD_CORE_VOLT_MGR_RST	VDD_CORE voltage manager reset event This is a source of global WARM reset. 0x0: No VDD_CORE voltage manager reset. 0x1: VDD_CORE voltage manager reset has occurred.	RW W1toClr	0
7	VDD_MM_VOLT_MGR_RST	VDD_MM voltage manager reset event This is a source of global WARM reset. 0x0: No VDD_MM voltage manager reset. 0x1: VDD_MM voltage manager reset has occurred.	RW W1toClr	0
6	VDD_MPU_VOLT_MGR_RST	VDD_MPU voltage manager reset event This is a source of global WARM reset. 0x0: No VDD_MPU voltage manager reset. 0x1: VDD_MPU voltage manager reset has occurred.	RW W1toClr	0
5	EXTERNAL_WARM_RST	External warm reset event 0x0: No global warm reset. 0x1: Global external warm reset has occurred.	RW W1toClr	0
4	RESERVED		RW W1toClr	0
3	MPU_WDT_RST	MPU Watchdog timer reset event. This is a source of global WARM reset. 0x0: No MPU watchdog reset. 0x1: MPU wachtdog reset has occurred.	RW W1toClr	0
2	RESERVED		RW W1toClr	0
1	GLOBAL_WARM_SW_RST	Global warm software reset event 0x0: No global warm SW reset 0x1: Global warm SW reset has occurred.	RW W1toClr	0
0	GLOBAL_COLD_RST	Power-on (cold) reset event 0x0: No power-on reset. 0x1: Power-on reset has occurred.	RW W1toClr	1

Table 3-793. Register Call Summary for Register PRM_RSTST

Reset Management Functional Description
- PRCM Module Reset Logging Mechanism: [0] [1]

PRCM Register Manual
- DEVICE_PRM Register Summary: [2]

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Table 3-794. PRM_RSTTIME

Address Offset	0x0000 0008		
Physical Address	0x4AE0 7C08	**Instance**	DEVICE_PRM
Description	Reset duration control. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RSTTIME2								RSTTIME1							

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:10	RSTTIME2	Power domain reset duration 2 in number of RM.SYS_CLK clock cycles. 0x0: Reserved	RW	0x10
9:0	RSTTIME1	Global reset duration 1 in number of FUNC_32K_CLK clock cycles. This bit-field is only sensitive to the external power-on reset (WKUP_SYS_PWRON_RST reset line). 0x0: Reserved	RW	0x06

Table 3-795. Register Call Summary for Register PRM_RSTTIME

Reset Management Functional Description

- PRCM Module Power-On Reset Sequence: [0]
- DSP Subsystem Power-On Reset Sequence: [1] [2]
- DSP Subsystem Software Warm Reset Sequence: [3]
- IPU Subsystem Power-On Reset Sequence: [4] [5]
- IPU Subsystem Software Warm Reset Sequence: [6]
- Global Warm Reset Sequence: [7]

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- DEVICE_PRM Register Summary: [8]

Table 3-796. PRM_CLKREQCTRL

Address Offset	0x0000 000C		
Physical Address	0x4AE0 7C0C	**Instance**	DEVICE_PRM
Description	This register allows controlling the CLKREQ signal towards SCRM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKREQ_COND

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	CLKREQ_COND	Control upon which condition CLKREQ signal is de-asserted. 0x0: CLKREQ is never de-asserted 0x1: Reserved 0x2: CLKREQ is de-asserted when system clock is not required by any function in the device and if all voltage domains are in RET state. 0x3: CLKREQ is de-asserted when system clock is not required by any function in the device and if all voltage domains are in SLEEP or RET state. 0x4: CLKREQ is de-asserted when system clock is not required by any function in the device. This is designed for low-power use-cases using the DPLL cascading scheme (ex: MP3) Read 0x5: Reserved Read 0x6: Reserved Read 0x7: Reserved	RW	0x0

Table 3-797. Register Call Summary for Register PRM_CLKREQCTRL

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-798. PRM_VOLTCTRL

Address Offset	0x0000 0010		
Physical Address	0x4AE0 7C10	**Instance**	DEVICE_PRM
Description	This register provides voltage domain management controls.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VDD_MM_I2C_DISABLE	VDD_MPU_I2C_DISABLE	VDD_CORE_I2C_DISABLE	RESERVED			VDD_MM_PRESENCE	VDD_MPU_PRESENCE	RESERVED		AUTO_CTRL_VDD_IVA_L		AUTO_CTRL_VDD_MPU_L		AUTO_CTRL_VDD_CORE_L	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x000000
14	VDD_MM_I2C_DISABLE	This bit allows disabling I2C interface with powerIC for MM voltage (for debug purpose only). [warm reset insensitive] 0x0: Normal mode: I2C is enabled. 0x1: Debug mode: I2C is disabled.	RW	0
13	VDD_MPU_I2C_DISABLE	This bit allows disabling I2C interface with powerIC for MPU voltage (for debug purpose only). [warm reset insensitive] 0x0: Normal mode: I2C is enabled. 0x1: Debug mode: I2C is disabled.	RW	0

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Bits	Field Name	Description	Type	Reset
12	VDD_CORE_I2C_DISABLE	This bit allows disabling I2C interface with powerIC for CORE voltage (for debug purpose only). [warm reset insensitive] 0x0: Normal mode: I2C is enabled. 0x1: Debug mode: I2C is disabled.	RW	0
11:10	RESERVED		R	0x0
9	VDD_MM_PRESENCE	This bit control the presence of MM voltage in device. [warm reset insensitive] 0x0: MM voltage is not present as an individual voltage: MM voltage is merged with MPU voltage if VDD_MPU_PRESENCE=1. MM voltage is merged with CORE voltage if VDD_MPU_PRESENCE=0. 0x1: MM voltage is present on the device.	RW	1
8	VDD_MPU_PRESENCE	This bit control the presence of MPU voltage in device. [warm reset insensitive] 0x0: MPU voltage is not present as an individual voltage: MPU voltage is merged with MM voltage if VDD_MM_PRESENCE=1. MPU voltage is merged with CORE voltage if VDD_MM_PRESENCE=0. 0x1: MPU voltage is present on the device.	RW	1
7:6	RESERVED		R	0x0
5:4	AUTO_CTRL_VDD_MM_L	This bit field specifies the state to which the hardware can automatically transition the VDD_MM_L voltage domain. 0x0: Voltage domain transitions are disabled. 0x1: Voltage domain transitions to SLEEP are enabled. 0x2: Voltage domain transitions to RET are enabled. Read 0x3: reserved	RW	0x0
3:2	AUTO_CTRL_VDD_MPU_L	This bit field specifies the state to which the hardware can automatically transition the VDD_MPU_L voltage domain. 0x0: Voltage domain transitions are disabled. 0x1: Voltage domain transitions to SLEEP are enabled. 0x2: Voltage domain transitions to RET are enabled. Read 0x3: reserved	RW	0x0
1:0	AUTO_CTRL_VDD_CORE_L	This bit field specifies the state to which the hardware can automatically transition the VDD_CORE_L voltage domain. 0x0: Voltage domain transitions are disabled. 0x1: Voltage domain transitions to SLEEP are enabled. 0x2: Voltage domain transitions to RET are enabled. Read 0x3: reserved	RW	0x0

Table 3-799. Register Call Summary for Register PRM_VOLTCTRL

Voltage-Management Functional Description
- VDD_x_L Transitions: [0]

PRCM Register Manual
- DEVICE_PRM Register Summary: [1]

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Table 3-800. PRM_PWRREQCTRL

Address Offset	0x0000 0014		
Physical Address	0x4AE0 7C14	**Instance**	DEVICE_PRM
Description	This register allows controlling the PWRREQ signal towards power IC.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														PWRREQ_COND	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	PWRREQ_COND	Control upon which condition from MPU, MM and CORE voltage domains PWRREQ is de-asserted. 0x0: PWRREQ is never de-asserted 0x1: PWRREQ is de-asserted if all voltage domain are in SLEEP or RET state. Conversely, PWRREQ is asserted upon any voltage domain entering or staying in ON state. 0x2: PWRREQ is de-asserted if all voltage domain are in RET state. Conversely, PWRREQ is asserted upon any voltage domain entering or staying in ON or SLEEP state. 0x3: Reserved	RW	0x0

Table 3-801. Register Call Summary for Register PRM_PWRREQCTRL

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-802. PRM_PSCON_COUNT

Address Offset	0x0000 0018		
Physical Address	0x4AE0 7C18	**Instance**	DEVICE_PRM
Description	This register allows controlling 2 parameters for power state controller. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PONOUT_2_PGOODIN_TIME								PCHARGE_TIME							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	PONOUT_2_PGOODIN_TIME	The value NbCycles set in this field determines the duration of the PONOUT to PGOODIN transition for power domain without DPS. The duration is computed as 8 x NbCycles of system clock cycles.	RW	0x30
7:0	PCHARGE_TIME	Number of system clock cycles for the SRAM pre-charge duration.	RW	0x17

Table 3-803. Register Call Summary for Register PRM_PSCON_COUNT

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

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Table 3-804. PRM_IO_COUNT

Address Offset	0x0000 001C		
Physical Address	0x4AE0 7C1C	**Instance**	DEVICE_PRM
Description	This register allows controlling LPDDR2 IO isolation removal setup. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ISO_2_ON_TIME							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	ISO_2_ON_TIME	Determines the setup time of the LPDDR2 IOs going out of isolation. Counting on the system clock.	RW	0x3A

Table 3-805. Register Call Summary for Register PRM_IO_COUNT

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-806. PRM_IO_PMCTRL

Address Offset	0x0000 0020		
Physical Address	0x4AE0 7C20	**Instance**	DEVICE_PRM
Description	This register allows controlling power management features of the IOs.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															GLOBAL_WUEN	RESERVED						WUCLK_STATUS	WUCLK_CTRL	RESERVED		IO_ON_STATUS	ISOOVR_EXTEND	RESERVED		ISOCLK_STATUS	ISOCLK_OVERRIDE

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	GLOBAL_WUEN	Global IO wakeup enable. This is a gating condition to all individual IO WUEN coming from control module. Gating is done in the Spinner logic. 0x0: All individual IO WUEN are gated in the Spinner logic (overriden to 0). 0x1: All individual IO WUEN from control module are going to IOs.	RW	0
15:10	RESERVED		R	0x00
9	WUCLK_STATUS	Gives value of WUCLKOUT signal coming back from IO pad ring.	R	0
8	WUCLK_CTRL	Direct control on WUCLKIN signal to IO pad ring. 0x0: WUCLKIN signal is driven to 0. IO wakeup daisy chain is functional as well as IO whose wakeup feature is enabled. 0x1: WUCLKIN signal is driven to 1. IO wakeup daisy chain is reset and is latching current pad states and WUEN inputs.	RW	0
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	IO_ON_STATUS	Gives the functional status of the IO ring. Read 0x0: Part or all of the IOs are not in the ON state, that is are in isolation state Read 0x1: All IOs are in the ON state	R	1
4	ISOOVR_EXTEND	Control non-EMIF IO isolation extension upon a device wakeup from low-power mode. 0x0: Non-EMIF IO isolation is not extended. EMIF_ON IO transition happens as soon as automatic restore is completed 0x1: Non-EMIF IO isolation is extended. EMIF_ON IO transition is stalled	RW	0
3:2	RESERVED		R	0x0
1	ISOCLK_STATUS	Gives value of ISOCLKOUT signal coming back from IO pad ring.	R	0
0	ISOCLK_OVERRIDE	Override control on ISOCLKIN signal to IO pad ring. Override should be used at boot time only when it is needed to change the mode of an IO from 1.8V default mode to 1.2V mode. When not overriden, this signal is controlled by hardware only. 0x0: ISOCLKIN signal is not overriden. 0x1: ISOCLKIN signal is overriden to active value ('1').	RW	0

Table 3-807. Register Call Summary for Register PRM_IO_PMCTRL

Device Low-Power States
- I/O Management: [0] [1] [2] [3] [4] [5]
- Software-Controlled I/O Isolation: [6] [7] [8] [9]

PRCM Register Manual
- DEVICE_PRM Register Summary: [10]

Table 3-808. PRM_VOLTSETUP_WARMRESET

Address Offset	0x0000 0024		
Physical Address	0x4AE0 7C24	**Instance**	DEVICE_PRM
Description	This register provides bit-fields for specifying voltage stabilization duration upon a global warm reset. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						STABLE_PRESCAL		RESERVED						STABLE_COUNT	

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:8	STABLE_PRESCAL	Determines prescaler for stabilization duration counting. 0x0: Ramp-up counter is incremented every 32 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 2048 system clock cycles 0x3: Ramp-up counter is incremented every 16384 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	STABLE_COUNT	Determines the stabilization duration of all VDD_xxx_L regulators upon a global warm reset assertion. The duration is computed according to Stable_Prescal.	RW	0x00

Table 3-809. Register Call Summary for Register PRM_VOLTSETUP_WARMRESET

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-810. PRM_VOLTSETUP_CORE_OFF

Address Offset	0x0000 0028		
Physical Address	0x4AE0 7C28	**Instance**	DEVICE_PRM
Description	This register provides bit-fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						RAMP_DOWN_PRESCAL		RESERVED		RAMP_DOWN_COUNT						RESERVED						RAMP_UP_PRESCAL		RESERVED		RAMP_UP_COUNT					

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Up_Prescal. At cold reset, PRCM assumes that VDD_CORE_L will be at a valid ON voltage before SYS_NRESPWRON is de-asserted.	RW	0x00

Table 3-811. Register Call Summary for Register PRM_VOLTSETUP_CORE_OFF

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-812. PRM_VOLTSETUP_MPU_OFF

Address Offset	0x0000 002C		
Physical Address	0x4AE0 7C2C	**Instance**	DEVICE_PRM
Description	This register provides bit-fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. [warm reset insensitive]		
Type	RW		

31 30 29 28 27 26	25 24	23 22	21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6	5 4 3 2 1 0
RESERVED	RAMP_DOWN_PRESCAL	RESERVED	RAMP_DOWN_COUNT	RESERVED	RAMP_UP_PRESCAL	RESERVED	RAMP_UP_COUNT

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_MPU_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_MPU_L regulators. The duration is computed according to Ramp_Up_Prescal. At cold reset, PRCM assumes that VDD_MPU_L will be at a valid ON voltage before SYS_NRESPWRON is de-asserted.	RW	0x00

Table 3-813. Register Call Summary for Register PRM_VOLTSETUP_MPU_OFF

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-814. PRM_VOLTSETUP_MM_OFF

Address Offset	0x0000 0030
Physical Address	0x4AE0 7C30 **Instance** DEVICE_PRM
Description	This register provides bit-fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. [warm reset insensitive]
Type	RW

31 30 29 28 27 26	25 24	23 22	21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6	5 4 3 2 1 0
RESERVED	RAMP_DOWN_PRESCAL	RESERVED	RAMP_DOWN_COUNT	RESERVED	RAMP_UP_PRESCAL	RESERVED	RAMP_UP_COUNT

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_MM_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_MM_L regulators. The duration is computed according to Ramp_Up_Prescal. At cold reset, PRCM assumes that VDD_MM_L will be at a valid ON voltage before SYS_NRESPWRON is de-asserted.	RW	0x00

Table 3-815. Register Call Summary for Register PRM_VOLTSETUP_MM_OFF

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-816. PRM_VOLTSETUP_CORE_RET_SLEEP

Address Offset	0x0000 0034		
Physical Address	0x4AE0 7C34	**Instance**	DEVICE_PRM
Description	This register provides bit-fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_CORE_L domain transitions between ON and RET or SLEEP state. [warm reset insensitive]		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	RAMP_DOWN_PRESCAL | RESERVED | RAMP_DOWN_COUNT	RESERVED | RAMP_UP_PRESCAL	RESERVED | RAMP_UP_COUNT

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_CORE_L regulators. The duration is computed according to Ramp_Up_Prescal.	RW	0x00

Table 3-817. Register Call Summary for Register PRM_VOLTSETUP_CORE_RET_SLEEP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-818. PRM_VOLTSETUP_MPU_RET_SLEEP

Address Offset	0x0000 0038
Physical Address	0x4AE0 7C38 **Instance** DEVICE_PRM
Description	This register provides bit-fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_MPU_L domain transitions between ON and RET or SLEEP state. [warm reset insensitive]
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							RAMP_DOWN_PRESCAL	RESERVED		RAMP_DOWN_COUNT						RESERVED						RAMP_UP_PRESCAL		RESERVED		RAMP_UP_COUNT					

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_MPU_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_MPU_L regulators. The duration is computed according to Ramp_Up_Prescal.	RW	0x00

Table 3-819. Register Call Summary for Register PRM_VOLTSETUP_MPU_RET_SLEEP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-820. PRM_VOLTSETUP_MM_RET_SLEEP

Address Offset	0x0000 003C
Physical Address	0x4AE0 7C3C **Instance** DEVICE_PRM
Description	This register provides bit-fields for specifying voltage ramp-up and ramp-down times for PRM managed external regulators. These values are used for VDD_MM_L domain transitions between ON and RET or SLEEP state. [warm reset insensitive]
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RAMP_DOWN_PRESCAL		RESERVED						RAMP_DOWN_COUNT								RESERVED							
																						RAMP_UP_PRESCAL		RESERVED		RAMP_UP_COUNT					

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	RAMP_DOWN_PRESCAL	Determines prescaler for ramp-down duration counting. 0x0: Ramp-down counter is incremented every 64 system clock cycles 0x1: Ramp-down counter is incremented every 256 system clock cycles 0x2: Ramp-down counter is incremented every 512 system clock cycles 0x3: Ramp-down counter is incremented every 2048 system clock cycles	RW	0x0
23:22	RESERVED		R	0x0
21:16	RAMP_DOWN_COUNT	Determines the ramp-down duration of VDD_MM_L regulators. The duration is computed according to Ramp_Down_Prescal.	RW	0x00
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9:8	RAMP_UP_PRESCAL	Determines prescaler for ramp-up duration counting. 0x0: Ramp-up counter is incremented every 64 system clock cycles 0x1: Ramp-up counter is incremented every 256 system clock cycles 0x2: Ramp-up counter is incremented every 512 system clock cycles 0x3: Ramp-up counter is incremented every 2048 system clock cycles	RW	0x0
7:6	RESERVED		R	0x0
5:0	RAMP_UP_COUNT	Determines the ramp-up duration of VDD_MM_L regulators. The duration is computed according to Ramp_Up_Prescal.	RW	0x00

Table 3-821. Register Call Summary for Register PRM_VOLTSETUP_MM_RET_SLEEP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-822. PRM_VP_CORE_CONFIG

Address Offset	0x0000 0040		
Physical Address	0x4AE0 7C40	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the Voltage Processor dedicated to CORE Voltage Domain (VDD_CORE_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROROFFSET								ERRORGAIN								INITVOLTAGE								RESERVED				TIMEOUTEN	INITVDD	FORCEUPDATE	VPENABLE

Bits	Field Name	Description	Type	Reset
31:24	ERROROFFSET	Offset value in the Error to Voltage converter (two's complement number).	RW	0x00
23:16	ERRORGAIN	Gain value in the Error to Voltage converter (two's complement number).	RW	0x00
15:8	INITVOLTAGE	Set the initial voltage level of the SMPS. It must be reconfigured before enable the SmartReflex around a new OPP.	RW	0x00
7:4	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0
3	TIMEOUTEN	Enable or disable the timeout capability of the Voltage Controller State Machine. 0x0: Timeout is disabled. Loop will wait indefinitely. 0x1: Timeout will occur when TIMEOUT cycles have elapsed.	RW	0
2	INITVDD	Initializes the voltage in the Voltage Processor. 0x0: Reset the initialization bit. 0x1: The positive edge of InitVdd triggers a write of the value in the InitVoltage into the Voltage Processor.	RW	0

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Bits	Field Name	Description	Type	Reset
1	FORCEUPDATE	Forces an update of the SMPS. 0x0: Reset the force bit. 0x1: The positive edge of ForceUpdate triggers an update of the voltage to the SMPS.	RW	0
0	VPENABLE	Enables or disables the Voltage Processor updates on SMARTREFLEX_SInterruptz. 0x0: Disables the Voltage Processor. 0x1: Enables the Voltage Processor.	RW	0

Table 3-823. Register Call Summary for Register PRM_VP_CORE_CONFIG

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-824. PRM_VP_CORE_STATUS

Address Offset	0x0000 0044		
Physical Address	0x4AE0 7C44	**Instance**	DEVICE_PRM
Description	This register reflects the idle state of the Voltage Processor dedicated to the CORE Voltage Domain (VDD_CORE_L. This register is read only and automatically updated.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															VPINIDLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0000 0000
0	VPINIDLE	CORE Voltage Processor idle status. Read 0x0: The Voltage Processor for CORE is processing. Warm reset sensitive Read 0x1: The Voltage Processor for CORE is in idle state.	R	1

Table 3-825. Register Call Summary for Register PRM_VP_CORE_STATUS

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-826. PRM_VP_CORE_VLIMITTO

Address Offset	0x0000 0048		
Physical Address	0x4AE0 7C48	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the voltage limits and timeout values of the Voltage Processor dedicated to the CORE Voltage Domain (VDD_CORE_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDMAX								VDDMIN								TIMEOUT															

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Bits	Field Name	Description	Type	Reset
31:24	VDDMAX	Defines the maximum voltage supply level.	RW	0x00
23:16	VDDMIN	Defines the minimum voltage supply level.	RW	0x00
15:0	TIMEOUT	Defines Voltage Controller maximum wait time for responses, measured in sysclk cycles.	RW	0x0000

Table 3-827. Register Call Summary for Register PRM_VP_CORE_VLIMITTO

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- DEVICE_PRM Register Summary: [0]

Table 3-828. PRM_VP_CORE_VOLTAGE

Address Offset	0x0000 004C		
Physical Address	0x4AE0 7C4C	**Instance**	DEVICE_PRM
Description	This register indicates the current value of the SMPS voltage for the Voltage Processor dedicated to the CORE Voltage Domain (VDD_CORE_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FORCEUPDATEWAIT																								VPVOLTAGE							

Bits	Field Name	Description	Type	Reset
31:8	FORCEUPDATEWAIT	The time voltage processor needs to wait for SMPS to be settled after receiving SMPS acknowledge. This wait only be used during force_update operation.	RW	0x000111
7:0	VPVOLTAGE	Indicates the current SMPS programmed voltage.	R	0x00

Table 3-829. Register Call Summary for Register PRM_VP_CORE_VOLTAGE

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- DEVICE_PRM Register Summary: [0]

Table 3-830. PRM_VP_CORE_VSTEPMAX

Address Offset	0x0000 0050		
Physical Address	0x4AE0 7C50	**Instance**	DEVICE_PRM
Description	This register allows the programming of the maximum voltage step and waiting time of the Voltage Processor dedicated to CORE Voltage Domain (VDD_CORE_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPSWAITTIMEMAX																VSTEPMAX							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPSWAITTIMEMAX	Slew rate for positive voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMAX	Maximum voltage step	RW	0x00

Table 3-831. Register Call Summary for Register PRM_VP_CORE_VSTEPMAX

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- DEVICE_PRM Register Summary: [0]

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Table 3-832. PRM_VP_CORE_VSTEPMIN

Address Offset	0x0000 0054		
Physical Address	0x4AE0 7C54	**Instance**	DEVICE_PRM
Description	This register allows the programming of the minimum voltage step and waiting time of the Voltage Processor dedicated to the CORE Voltage Domain (VDD_CORE_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPSWAITTIMEMIN																VSTEPMIN							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPSWAITTIMEMIN	Slew rate for negative voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMIN	Minimum voltage step	RW	0x00

Table 3-833. Register Call Summary for Register PRM_VP_CORE_VSTEPMIN

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-834. PRM_VP_MPU_CONFIG

Address Offset	0x0000 0058		
Physical Address	0x4AE0 7C58	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the Voltage Processor dedicated to MPU Voltage Domain (VDD_MPU_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROROFFSET								ERRORGAIN								INITVOLTAGE								RESERVED				TIMEOUTEN	INITVDD	FORCEUPDATE	VPENABLE

Bits	Field Name	Description	Type	Reset
31:24	ERROROFFSET	Offset value in the Error to Voltage converter (two's complement number).	RW	0x00
23:16	ERRORGAIN	Gain value in the Error to Voltage converter (two's complement number).	RW	0x00
15:8	INITVOLTAGE	Set the initial voltage level of the SMPS. It must be reconfigured before enable the SmartReflex around a new OPP.	RW	0x00
7:4	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0
3	TIMEOUTEN	Enable or disable the timeout capability of the Voltage Controller State Machine. 0x0: Timeout is disabled. Loop will wait indefinitely. 0x1: Timeout will occur when TIMEOUT cycles have elapsed.	RW	0
2	INITVDD	Initializes the voltage in the Voltage Processor. 0x0: Reset the initialization bit. 0x1: The positive edge of InitVdd triggers a write of the value in the InitVoltage into the Voltage Processor.	RW	0

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Bits	Field Name	Description	Type	Reset
1	FORCEUPDATE	Forces an update of the SMPS. 0x0: Reset the force bit. 0x1: The positive edge of ForceUpdate triggers an update of the voltage to the SMPS.	RW	0
0	VPENABLE	Enables or disables the Voltage Processor updates on SMARTREFLEX_SInterruptz. 0x0: Disables the Voltage Processor. 0x1: Enables the Voltage Processor.	RW	0

Table 3-835. Register Call Summary for Register PRM_VP_MPU_CONFIG

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-836. PRM_VP_MPU_STATUS

Address Offset	0x0000 005C		
Physical Address	0x4AE0 7C5C	**Instance**	DEVICE_PRM
Description	This register reflects the idle state of the Voltage Processor dedicated to the MPU Voltage Domain (VDD_MPU_L. This register is read only and automatically updated.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															VPINIDLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0000 0000
0	VPINIDLE	Voltage Processor 1 idle status. Read 0x0: The Voltage Processor 1 is processing. Read 0x1: The Voltage Processor 1 is in idle state.	R	1

Table 3-837. Register Call Summary for Register PRM_VP_MPU_STATUS

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-838. PRM_VP_MPU_VLIMITTO

Address Offset	0x0000 0060		
Physical Address	0x4AE0 7C60	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the voltage limits and timeout values of the Voltage Processor dedicated to the MPU Voltage Domain (VDD_MPU_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDMAX								VDDMIN								TIMEOUT															

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Bits	Field Name	Description	Type	Reset
31:24	VDDMAX	Defines the maximum voltage supply level.	RW	0x00
23:16	VDDMIN	Defines the minimum voltage supply level.	RW	0x00
15:0	TIMEOUT	Defines Voltage Controller maximum wait time for responses, measured in sysclk cycles.	RW	0x0000

Table 3-839. Register Call Summary for Register PRM_VP_MPU_VLIMITTO

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-840. PRM_VP_MPU_VOLTAGE

Address Offset	0x0000 0064		
Physical Address	0x4AE0 7C64	**Instance**	DEVICE_PRM
Description	This register indicates the current value of the SMPS voltage for the Voltage Processor dedicated to the MPU Voltage Domain (VDD_MPU_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FORCEUPDATEWAIT																								VPVOLTAGE							

Bits	Field Name	Description	Type	Reset
31:8	FORCEUPDATEWAIT	The time voltage processor needs to wait for SMPS to be settled after receiving SMPS acknowledge. This wait only be used during force_update operation.	RW	0x000111
7:0	VPVOLTAGE	Indicates the current SMPS programmed voltage.	R	0x00

Table 3-841. Register Call Summary for Register PRM_VP_MPU_VOLTAGE

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-842. PRM_VP_MPU_VSTEPMAX

Address Offset	0x0000 0068		
Physical Address	0x4AE0 7C68	**Instance**	DEVICE_PRM
Description	This register allows the programming of the maximum voltage step and waiting time of the Voltage Processor dedicated to MPU Voltage Domain (VDD_MPU_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPSWAITTIMEMAX																VSTEPMAX							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPSWAITTIMEMAX	Slew rate for positive voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMAX	Maximum voltage step	RW	0x00

Table 3-843. Register Call Summary for Register PRM_VP_MPU_VSTEPMAX

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

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Table 3-844. PRM_VP_MPU_VSTEPMIN

Address Offset	0x0000 006C		
Physical Address	0x4AE0 7C6C	**Instance**	DEVICE_PRM
Description	This register allows the programming of the minimum voltage step and waiting time of the Voltage Processor dedicated to the MPU Voltage Domain (VDD_MPU_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPSWAITTIMEMIN																VSTEPMIN							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPSWAITTIMEMIN	Slew rate for negative voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMIN	Minimum voltage step	RW	0x00

Table 3-845. Register Call Summary for Register PRM_VP_MPU_VSTEPMIN

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-846. PRM_VP_MM_CONFIG

Address Offset	0x0000 0070		
Physical Address	0x4AE0 7C70	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the Voltage Processor dedicated to MM Voltage Domain (VDD_MM_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROROFFSET								ERRORGAIN								INITVOLTAGE								RESERVED				TIMEOUTEN	INITVDD	FORCEUPDATE	VPENABLE

Bits	Field Name	Description	Type	Reset
31:24	ERROROFFSET	Offset value in the Error to Voltage converter (two's complement number).	RW	0x00
23:16	ERRORGAIN	Gain value in the Error to Voltage converter (two's complement number).	RW	0x00
15:8	INITVOLTAGE	Set the initial voltage level of the SMPS. It must be reconfigured before enable the SmartReflex around a new OPP.	RW	0x00
7:4	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0
3	TIMEOUTEN	Enable or disable the timeout capability of the Voltage Controller State Machine. 0x0: Timeout is disabled. Loop will wait indefinitely. 0x1: Timeout will occur when TIMEOUT cycles have elapsed.	RW	0
2	INITVDD	Initializes the voltage in the Voltage Processor. 0x0: Reset the initialization bit. 0x1: The positive edge of InitVdd triggers a write of the value in the InitVoltage into the Voltage Processor.	RW	0

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Bits	Field Name	Description	Type	Reset
1	FORCEUPDATE	Forces an update of the SMPS. 0x0: Reset the force bit. 0x1: The positive edge of ForceUpdate triggers an update of the voltage to the SMPS.	RW	0
0	VPENABLE	Enables or disables the Voltage Processor updates on SMARTREFLEX_SInterrupt. 0x0: Disables the Voltage Processor. 0x1: Enables the Voltage Processor.	RW	0

Table 3-847. Register Call Summary for Register PRM_VP_MM_CONFIG

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-848. PRM_VP_MM_STATUS

Address Offset	0x0000 0074		
Physical Address	0x4AE0 7C74	**Instance**	DEVICE_PRM
Description	This register reflects the idle state of the Voltage Processor dedicated to the MM Voltage Domain (VDD_MM_L). This register is read only and automatically updated.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															VPINIDLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x0000 0000
0	VPINIDLE	Voltage Processor 1 idle status. Read 0x0: The Voltage Processor 1 is processing. Read 0x1: The Voltage Processor 1 is in idle state.	R	1

Table 3-849. Register Call Summary for Register PRM_VP_MM_STATUS

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-850. PRM_VP_MM_VLIMITTO

Address Offset	0x0000 0078		
Physical Address	0x4AE0 7C78	**Instance**	DEVICE_PRM
Description	This register allows the configuration of the voltage limits and timeout values of the Voltage Processor dedicated to the MM Voltage Domain (VDD_MM_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDMAX								VDDMIN								TIMEOUT															

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Bits	Field Name	Description	Type	Reset
31:24	VDDMAX	Defines the maximum voltage supply level.	RW	0x00
23:16	VDDMIN	Defines the minimum voltage supply level.	RW	0x00
15:0	TIMEOUT	Defines Voltage Controller maximum wait time for responses, measured in sysclk cycles.	RW	0x0000

Table 3-851. Register Call Summary for Register PRM_VP_MM_VLIMITTO

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- DEVICE_PRM Register Summary: [0]

Table 3-852. PRM_VP_MM_VOLTAGE

Address Offset	0x0000 007C		
Physical Address	0x4AE0 7C7C	**Instance**	DEVICE_PRM
Description	This register indicates the current value of the SMPS voltage for the Voltage Processor dedicated to the MM Voltage Domain (VDD_MM_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FORCEUPDATEWAIT																								VPVOLTAGE							

Bits	Field Name	Description	Type	Reset
31:8	FORCEUPDATEWAIT	The time voltage processor needs to wait for SMPS to be settled after receiving SMPS acknowledge. This wait only be used during force_update operation.	RW	0x000111
7:0	VPVOLTAGE	Indicates the current SMPS programmed voltage.	R	0x00

Table 3-853. Register Call Summary for Register PRM_VP_MM_VOLTAGE

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-854. PRM_VP_MM_VSTEPMAX

Address Offset	0x0000 0080		
Physical Address	0x4AE0 7C80	**Instance**	DEVICE_PRM
Description	This register allows the programming of the maximum voltage step and waiting time of the Voltage Processor dedicated to MM Voltage Domain (VDD_MM_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPSWAITTIMEMAX																VSTEPMAX							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPSWAITTIMEMAX	Slew rate for positive voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMAX	Maximum voltage step	RW	0x00

Table 3-855. Register Call Summary for Register PRM_VP_MM_VSTEPMAX

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- DEVICE_PRM Register Summary: [0]

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Table 3-856. PRM_VP_MM_VSTEPMIN

Address Offset	0x0000 0084		
Physical Address	0x4AE0 7C84	**Instance**	DEVICE_PRM
Description	This register allows the programming of the minimum voltage step and waiting time of the Voltage Processor dedicated to the MM Voltage Domain (VDD_MM_L).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPSWAITTIMEMIN																VSTEPMIN							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0x00
23:8	SMPSWAITTIMEMIN	Slew rate for negative voltage step (in number of cycles per step).	RW	0x0000
7:0	VSTEPMIN	Minimum voltage step	RW	0x00

Table 3-857. Register Call Summary for Register PRM_VP_MM_VSTEPMIN

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- DEVICE_PRM Register Summary: [0]

Table 3-858. PRM_VC_SMPS_CORE_CONFIG

Address Offset	0x0000 0088		
Physical Address	0x4AE0 7C88	**Instance**	DEVICE_PRM
Description	This register allows the setting of the I2C slave address of the Power IC device, the setting of the voltage configuration register address for the VD_CORE and the Command (ON/ON-Low-Power/Retention) configuration register address values for VD_CORE (if used SMPS chips have different command configuration register than voltage configuration register). [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CMD_VDD_CORE_L	RACEN_VDD_CORE_L	RAC_VDD_CORE_L	RAV_VDD_CORE_L	SEL_SA_VDD_CORE_L	CMDRA_VDD_CORE_L								VOLRA_VDD_CORE_L								RESERVED	SA_VDD_CORE_L						

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28	CMD_VDD_CORE_L	Command values (ON/ON-Low-Power/Retention voltage values) set selection for VDD_CORE_L channel 0x0: VDD_CORE_L channel use VC_VAL_CMD_VDD_MPU_L set for command values 0x1: VDD_CORE_L channel use VC_VAL_CMD_VDD_CORE_L set for command values	RW	0x1
27	RACEN_VDD_CORE_L	Enable bit for usage of RAC_VDD_CORE_L 0x0: VDD_CORE_L channel use VOLRA values for register address of VFSM-s commands. VFSM-s commands goes also to voltage configuration register 0x1: VDD_CORE_L channel use CMDRA values for register address of VFSM-s commands. VFSM-s commands goes to different command configuration register	RW	0x0

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Bits	Field Name	Description	Type	Reset
26	RAC_VDD_CORE_L	Command (ON/ON-Low-Power/Retention) configuration register address pointer for VDD_CORE_L channel 0x0: Select CMDRA_VDD_MPU_L for VDD_CORE_L channel 0x1: Select CMDRA_VDD_CORE_L for VDD_CORE_L channel	RW	0x1
25	RAV_VDD_CORE_L	Voltage configuration register address pointer for VDD_CORE_L channel 0x0: Select VOLRA_VDD_MPU_L for VDD_CORE_L channel 0x1: Select VOLRA_VDD_CORE_L for VDD_CORE_L channel	RW	0x1
24	SEL_SA_VDD_CORE_L	Slave address pointer for VDD_CORE_L channel 0x0: Select SA_VDD_MPU_L for VDD_CORE_L channel 0x1: Select SA_VDD_CORE_L for VDD_CORE_L channel	RW	0x0
23:16	CMDRA_VDD_CORE_L	Command (ON/ON-Low-Power /Retention) configuration register address value for VDD_CORE_L channel.(if VDD_CORE_L source has different command configuration register than voltage VDD_MPU_L)	RW	0x00
15:8	VOLRA_VDD_CORE_L	Set the voltage configuration register address value for the VDD_CORE_L channel (if VDD_CORE_L source is placed in same chip as VDD_MPU_L source and have different voltage configuration register)	RW	0x00
7	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0
6:0	SA_VDD_CORE_L	Set the I2C slave address value for the first Power IC device.	RW	0x00

Table 3-859. Register Call Summary for Register PRM_VC_SMPS_CORE_CONFIG

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- DEVICE_PRM Register Summary: [0]

Table 3-860. PRM_VC_SMPS_MM_CONFIG

Address Offset	0x0000 008C		
Physical Address	0x4AE0 7C8C	**Instance**	DEVICE_PRM
Description	This register allows the setting of the I2C slave address of the Power IC device, the setting of the voltage configuration register address for the MM VDD and the Command (ON/ON-Low-Power/Retention) configuration register address values for MM VDD (if used SMPS chips have different command configuration register than voltage configuration register) [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CMD_VDD_MM_L	RACEN_VDD_MM_L	RAC_VDD_MM_L	RAV_VDD_MM_L	SEL_SA_VDD_MM_L	CMDRA_VDD_MM_L								VOLRA_VDD_MM_L								RESERVED	SA_VDD_MM_L						

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28	CMD_VDD_MM_L	Command values (ON/ON-Low-Power/Retention voltage values) set selection for VDD_MM_L channel 0x0: VDD_MM_L channel use VC_VAL_CMD_VDD_MPU_L set for command values 0x1: VDD_MM_L channel use VC_VAL_CMD_VDD_MM_L set for command values	RW	0x1

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Bits	Field Name	Description	Type	Reset
27	RACEN_VDD_MM_L	Enable bit for usage of RAC_VDD_MM_L 0x0: VDD_MM_L channel uses VOLRA values for register address of VFSM-s commands. VFSM-s commands goes also to voltage configuration register 0x1: VDD_MM_L channel uses CMDRA values for register address of VFSM-s commands. VFSM-s commands goes to different command configuration register	RW	0x0
26	RAC_VDD_MM_L	Command (ON/ON-Low-Power/Retention) configuration register address pointer for VDD_MM_L channel 0x0: Select CMDRA_VDD_MPU_L for VDD_MM_L channel 0x1: Select CMDRA_VDD_MM_L for VDD_MM_L channel	RW	0x1
25	RAV_VDD_MM_L	Voltage configuration register address pointer for VDD_MM_L channel. 0x0: Select VOLRA_VDD_MPU_L for VDD_MM_L channel 0x1: Select VOLRA_VDD_MM_L for VDD_MM_L channel	RW	0x1
24	SEL_SA_VDD_MM_L	Slave address pointer for VDD_MM_L channel 0x0: Select SA_VDD_MPU_L for VDD_MM_L channel 0x1: Select SA_VDD_MM_L for VDD_MM_L channel	RW	0x0
23:16	CMDRA_VDD_MM_L	Command (ON/ON-Low-Power /Retention) configuration register address value for VDD_MM_L channel (if VDD_MM_L source has different command configuration register than voltage VDD_MPU_L)	RW	0x00
15:8	VOLRA_VDD_MM_L	Voltage configuration register address value for VDD_MM_L channel (if VDD_MM_L source is placed in same chip as VDD_MPU_L source and have different voltage configuration register)	RW	0x00
7	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0
6:0	SA_VDD_MM_L	Set the I2C slave address value for the second (if any) Power IC device.	RW	0x00

Table 3-861. Register Call Summary for Register PRM_VC_SMPS_MM_CONFIG

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- DEVICE_PRM Register Summary: [0]

Table 3-862. PRM_VC_SMPS_MPU_CONFIG

Address Offset	0x0000 0090		
Physical Address	0x4AE0 7C90	**Instance**	DEVICE_PRM
Description	This register allows the setting of the I2C slave address of the Power IC device, the setting of the voltage configuration register address for the MPU VDD and the Command (ON/ON-Low-Power/Retention) configuration register address values for MPU VDD (if used SMPS chips have different command configuration register than voltage configuration register). [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CMD_VDD_MPU_L	RACEN_VDD_MPU_L	RAC_VDD_MPU_L	RAV_VDD_MPU_L	SEL_SA_VDD_MPU_L	CMDRA_VDD_MPU_L								VOLRA_VDD_MPU_L								RESERVED	SA_VDD_MPU_L						

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28	CMD_VDD_MPU_L	Command values (ON/ON-Low-Power/Retention voltage values) set selection for VDD_MPU_L channel (This bit has no influence on VDD_MPU_L channel)	RW	0x0
27	RACEN_VDD_MPU_L	Enable bit for usage of RAC_VDD_MPU_L 0x0: VDD_MPU_L channel uses VOLRA values for register address of VFSM-s commands. VFSM-s commands goes also to voltage configuration register 0x1: VDD_MPU_L channel uses CMDRA values for register address of VFSM-s commands. VFSM-s commands goes to different command configuration register	RW	0x0
26	RAC_VDD_MPU_L	Command (ON/ON-Low-Power/Retention) configuration register address pointer for VDD_MPU_L channel. (This bit has no influence on first VDD_MPU_L channel)	RW	0x0
25	RAV_VDD_MPU_L	Voltage configuration register address pointer for VDD_MPU_L channel. (This bit has no influence on first VDD_MPU_L channel)	RW	0x0
24	SEL_SA_VDD_MPU_L	Slave address pointer for VDD_MPU_L channel. (This bit has no influence on first VDD_MPU_L channel)	RW	0x0
23:16	CMDRA_VDD_MPU_L	Command (ON/ON-Low-Power /Retention) configuration register address value for VDD_MPU_L channel.	RW	0x00
15:8	VOLRA_VDD_MPU_L	Voltage configuration register address value for VDD_MPU_L channel.	RW	0x00
7	RESERVED	Write 0's for future compatibility. Read is undefined.	R	0
6:0	SA_VDD_MPU_L	Set the I2C slave address value for the third (if any) Power IC device.	RW	0x00

Table 3-863. Register Call Summary for Register PRM_VC_SMPS_MPU_CONFIG

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-864. PRM_VC_VAL_CMD_VDD_CORE_L

Address Offset	0x0000 0094		
Physical Address	0x4AE0 7C94	**Instance**	DEVICE_PRM
Description	This register allows the setting of the ON/ON-Low-Power/Retention command values for VDD_CORE_L channel. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ON								ONLP								RET								RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	ON	Set the ON command value.	RW	0x00
23:16	ONLP	Set the ON-Low-Power command value.	RW	0x00
15:8	RET	Set the RET command value.	RW	0x00
7:0	RESERVED	Reserved	R	0x00

Table 3-865. Register Call Summary for Register PRM_VC_VAL_CMD_VDD_CORE_L

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- DEVICE_PRM Register Summary: [0]

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Table 3-866. PRM_VC_VAL_CMD_VDD_MM_L

Address Offset	0x0000 0098		
Physical Address	0x4AE0 7C98	**Instance**	DEVICE_PRM
Description	This register allows the setting of the ON/ON-Low-Power/Retention command values for VDD_MM_L channel. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ON								ONLP								RET								RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	ON	Set the ON command value.	RW	0x00
23:16	ONLP	Set the ON-Low-Power command value.	RW	0x00
15:8	RET	Set the RET command value.	RW	0x00
7:0	RESERVED	Reserved	R	0x00

Table 3-867. Register Call Summary for Register PRM_VC_VAL_CMD_VDD_MM_L

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- DEVICE_PRM Register Summary: [0]

Table 3-868. PRM_VC_VAL_CMD_VDD_MPU_L

Address Offset	0x0000 009C		
Physical Address	0x4AE0 7C9C	**Instance**	DEVICE_PRM
Description	This register allows the setting of the ON/ON-Low-Power/Retention command values for VDD_MPU_L channel. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ON								ONLP								RET								RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	ON	Set the ON command value.	RW	0x00
23:16	ONLP	Set the ON-Low-Power command value.	RW	0x00
15:8	RET	Set the RET command value.	RW	0x00
7:0	RESERVED	Reserved	R	0x00

Table 3-869. Register Call Summary for Register PRM_VC_VAL_CMD_VDD_MPU_L

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- DEVICE_PRM Register Summary: [0]

Table 3-870. PRM_VC_VAL_BYPASS

Address Offset	0x0000 00A0		
Physical Address	0x4AE0 7CA0	**Instance**	DEVICE_PRM
Description	Bypass data values register used for bypass command channel to send other configuration information (other then voltage configuration parameters) for SMPS chips which have no other configuration interface then this I2C interface and flag to indicate OPP change to EMIF to allow read/write leveling. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						OPP_CHANGE_EMIF_LVL	VALID	DATA								REGADDR								RESERVED	SLAVEADDR						

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	OPP_CHANGE_EMIF_LVL	This bit controls read-write leveling of EMIF memories (DDR3). It must be set in case OPP voltage change is done through Voltage Controller whithout passing through Voltage processor. 0x0: Enable leveling 0x1: Disable leveling	RW	0
24	VALID	This bit validates the bypass command. It is automatically cleared by HW either after getting the acknowledge back from the SMPS or if an error occured. Read 0x0: The last command send has been acknowledged 0x1: Pending command is being process	RW WSpecial	0
23:16	DATA	Data to send to the Power IC device.	RW	0x00
15:8	REGADDR	Set the address of Power IC device register to configure.	RW	0x00
7	RESERVED		R	0
6:0	SLAVEADDR	Set the I2C slave address value.	RW	0x00

Table 3-871. Register Call Summary for Register PRM_VC_VAL_BYPASS

Voltage-Management Functional Description • EMIF-Specific Interface: [0]
PRCM Register Manual • DEVICE_PRM Register Summary: [1]

Table 3-872. PRM_VC_CORE_ERRST

Address Offset	0x0000 00A4		
Physical Address	0x4AE0 7CA4	**Instance**	DEVICE_PRM
Description	This debug register logs CORE related error status coming from Voltage Controller. Must be cleared by software.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										VFSM_TIMEOUT_ERR_CORE	VFSM_RA_ERR_CORE	VFSM_SA_ERR_CORE	SMPS_TIMEOUT_ERR_CORE	SMPS_RA_ERR_CORE	SMPS_SA_ERR_CORE

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x000
5	VFSM_TIMEOUT_ERR_CORE	CORE voltage FSM command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0x0
4	VFSM_RA_ERR_CORE	Wrong register address error for CORE voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
3	VFSM_SA_ERR_CORE	Wrong slave address error for CORE voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
2	SMPS_TIMEOUT_ERR_CORE	CORE voltage processor command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
1	SMPS_RA_ERR_CORE	Wrong register address error for CORE voltage processor. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
0	SMPS_SA_ERR_CORE	Wrong slave address error for CORE voltage processor 0x0: No error 0x1: An error has been logged	RW W1toClr	0

Table 3-873. Register Call Summary for Register PRM_VC_CORE_ERRST

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- DEVICE_PRM Register Summary: [0]

Table 3-874. PRM_VC_MM_ERRST

Address Offset	0x0000 00A8		
Physical Address	0x4AE0 7CA8	**Instance**	DEVICE_PRM
Description	This debug register logs MM related error status coming from Voltage Controller. Must be cleared by software.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										VFSM_TIMEOUT_ERR_MM	VFSM_RA_ERR_MM	VFSM_SA_ERR_MM	SMPS_TIMEOUT_ERR_MM	SMPS_RA_ERR_MM	SMPS_SA_ERR_MM

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x000
5	VFSM_TIMEOUT_ERR_MM	MM voltage FSM command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0x0

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Bits	Field Name	Description	Type	Reset
4	VFSM_RA_ERR_MM	Wrong register address error for MM voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
3	VFSM_SA_ERR_MM	Wrong slave address error for MM voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
2	SMPS_TIMEOUT_ERR_MM	MM voltage processor command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
1	SMPS_RA_ERR_MM	Wrong register address error for MM voltage processor. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
0	SMPS_SA_ERR_MM	Wrong slave address error for MM voltage processor 0x0: No error 0x1: An error has been logged	RW W1toClr	0

Table 3-875. Register Call Summary for Register PRM_VC_MM_ERRST

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-876. PRM_VC_MPU_ERRST

Address Offset	0x0000 00AC		
Physical Address	0x4AE0 7CAC	**Instance**	DEVICE_PRM
Description	This debug register logs MPU related error status coming from Voltage Controller. Must be cleared by software.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VFSM_TIMEOUT_ERR_MPU	VFSM_RA_ERR_MPU	VFSM_SA_ERR_MPU	SMPS_TIMEOUT_ERR_MPU	SMPS_RA_ERR_MPU	SMPS_SA_ERR_MPU		

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x000
5	VFSM_TIMEOUT_ERR_MPU	MPU voltage FSM command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0x0
4	VFSM_RA_ERR_MPU	Wrong register address error for MPU voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0
3	VFSM_SA_ERR_MPU	Wrong slave address error for MPU voltage FSM 0x0: No error 0x1: An error has been logged	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	SMPS_TIMEOUT_ERR_MPU	MPU voltage processor command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
1	SMPS_RA_ERR_MPU	Wrong register address error for MPU voltage processor. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
0	SMPS_SA_ERR_MPU	Wrong slave address error for MPU voltage processor 0x0: No error 0x1: An error has been logged	RW W1toClr	0

Table 3-877. Register Call Summary for Register PRM_VC_MPU_ERRST

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- DEVICE_PRM Register Summary: [0]

Table 3-878. PRM_VC_BYPASS_ERRST

Address Offset	0x0000 00B0		
Physical Address	0x4AE0 7CB0	**Instance**	DEVICE_PRM
Description	This debug register logs BYPASS related error status coming from Voltage Controller. Must be cleared by software.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													BYPS_TIMEOUT_ERR	BYPS_RA_ERR	BYPS_SA_ERR

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x000
2	BYPS_TIMEOUT_ERR	BYPASS command frame is finished but is not acknowledged by the slave, or (I2C multimaster) arbitration lost. 0x0: No error 0x1: An error has been logged	RW W1toClr	0
1	BYPS_RA_ERR	Wrong register address error for BYPASS command 0x0: No error 0x1: An error has been logged	RW W1toClr	0
0	BYPS_SA_ERR	Wrong slave address error for BYPASS command 0x0: No error 0x1: An error has been logged	RW W1toClr	0

Table 3-879. Register Call Summary for Register PRM_VC_BYPASS_ERRST

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- DEVICE_PRM Register Summary: [0]

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Table 3-880. PRM_VC_CFG_I2C_MODE

Address Offset	0x0000 00B4		
Physical Address	0x4AE0 7CB4	**Instance**	DEVICE_PRM
Description	I2C configuration register. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DFILTEREN	RESERVED	SRMODEEN	HSMODEEN	HSMCODE			

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000 0000
6	DFILTEREN	This field enables double filter procedure for I2C input lines 0x0: I2C bus digital filter rejects all glitches smaller than 1 system clock cycle 0x1: I2C bus digital filter rejects all glitches smaller than 2 system clock cycle	RW	0x0
5	RESERVED		R	0x0
4	SRMODEEN	Enables the I2C repeated start operation mode (effect of holding the SCL and SDA lines low, in effect blocking the I2C bus from losing arbitration between repeated start points). Use of this feature results from a trade-off between speed and power consumption of I2C interface 0x0: Disables the repeated start operation mode 0x1: Enables the repeated start operation mode	RW	0x1
3	HSMODEEN	Enables I2C bus High Speed mode 0x0: Disables the I2C high speed mode 0x1: Enables the I2C high speed mode	RW	0x1
2:0	HSMCODE	Master code value for I2C High Speed preamble transmission.	RW	0

Table 3-881. Register Call Summary for Register PRM_VC_CFG_I2C_MODE

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- Voltage Controller Initialization: [0] [1] [2] [3]

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- DEVICE_PRM Register Summary: [4]

Table 3-882. PRM_VC_CFG_I2C_CLK

Address Offset	0x0000 00B8		
Physical Address	0x4AE0 7CB8	**Instance**	DEVICE_PRM
Description	I2C Interface clock configuration parameters. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSSCLL								HSSCLH								SCLL								SCLH							

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Bits	Field Name	Description	Type	Reset
31:24	HSSCLL	Number of the system clock cycles, necessary to count the low period of the I2C clock signal, when the I2C interface runs in High-Speed mode of operation.	RW	0x00
23:16	HSSCLH	Number of the system clock cycles, necessary to count the high period of the I2C clock signal, when the I2C interface runs in High-Speed mode of operation.	RW	0x00
15:8	SCLL	Number of the system clock cycles, necessary to count the low period of the I2C clock signal, when the I2C interface runs in Fast mode of operation.	RW	0x00
7:0	SCLH	Number of the system clock cycles, necessary to count the high period of the I2C clock signal, when the I2C interface runs in Fast mode of operation.	RW	0x00

Table 3-883. Register Call Summary for Register PRM_VC_CFG_I2C_CLK

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- DEVICE_PRM Register Summary: [0]

Table 3-884. PRM_SRAM_COUNT

Address Offset	0x0000 00BC		
Physical Address	0x4AE0 7CBC	**Instance**	DEVICE_PRM
Description	Common setup for SRAM LDO transition counters. Applies to all voltage domains.[warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STARTUP_COUNT								SLPCNT_VALUE								VSETUPCNT_VALUE								RESERVED							

Bits	Field Name	Description	Type	Reset
31:24	STARTUP_COUNT	Determines the start-up duration of SRAM and ABBLDO. The duration is computed as 16 x NbCycles of system clock cycles.	RW	0x78
23:16	SLPCNT_VALUE	Delay between retention assertion of last SRAM bank and SRAMALLRET signal to LDO is driven high. Counting on system clock.	RW	0x00
15:8	VSETUPCNT_VALUE	SRAM LDO rampup time from retention to active mode. The duration is computed as 8 x NbCycles of system clock cycles.	RW	0x00
7:0	RESERVED		R	0x00

Table 3-885. Register Call Summary for Register PRM_SRAM_COUNT

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- DEVICE_PRM Register Summary: [0]

Table 3-886. PRM_SLDO_CORE_SETUP

Address Offset	0x0000 00C4		
Physical Address	0x4AE0 7CC4	**Instance**	DEVICE_PRM
Description	Setup of the SRAM LDO for CORE voltage domain. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							AIPOFF	ENFUNC5	ENFUNC4	ENFUNC3	ENFUNC2	ENFUNC1	ABBOFF_SLEEP	ABBOFF_ACT	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	AIPOFF	Override on AIPOFF input of SRAM LDO. 0x0: AIPOFF signal is not overriden 0x1: AIPOFF signal is overriden to '1'. Corresponding SRAM LDO is disabled and in HZ mode.	RW	0
7	ENFUNC5	ENFUNC5 input of SRAM LDO. 0x0: Active to retention is a one step transfer 0x1: Active to retention is a two steps transfer	RW	0
6	ENFUNC4	ENFUNC4 input of SRAM LDO. 0x0: One external clock is supplied 0x1: No external clock is supplied	RW	0
5	ENFUNC3	ENFUNC3 input of SRAM LDO. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: Sub regulation is disabled 0x1: Sub regulation is enabled	RW	0
4	ENFUNC2	ENFUNC2 input of SRAM LDO. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: External cap is used 0x1: External cap is not used	RW WSpecial	0
3	ENFUNC1	ENFUNC1 input of SRAM LDO. After PowerOn reset , this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: Short circuit protection is disabled 0x1: Short circuit protection is enabled	RW	0
2	ABBOFF_SLEEP	Determines whether SRAMNWA is supplied by VDDS or VDDAR during deep-sleep. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	1
1	ABBOFF_ACT	Determines whether SRAMNWA is supplied by VDDS or VDDAR during active mode. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	1
0	RESERVED	Reserved	R	0

Table 3-887. Register Call Summary for Register PRM_SLDO_CORE_SETUP

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- DEVICE_PRM Register Summary: [0]

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Table 3-888. PRM_SLDO_CORE_CTRL

Address Offset	0x0000 00C8		
Physical Address	0x4AE0 7CC8	**Instance**	DEVICE_PRM
Description	Control and status of the SRAM LDO for CORE voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						SRAM_IN_TRANSITION	SRAMLDO_STATUS	RESERVED							RETMODE_ENABLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	SRAM_IN_TRANSITION	Status indicating SRAM LDO state machine state. Read 0x0: SRAM LDO state machine is stable Read 0x1: SRAM LDO state machine is in transition state	R	0
8	SRAMLDO_STATUS	SRAMLDO status Read 0x0: SRAMLDO is in ACTIVE mode. Read 0x1: SRAMLDO is on RETENTION mode.	R	0
7:1	RESERVED	Reserved	R	0x00
0	RETMODE_ENABLE	Control if the SRAM LDO retention mode is used or not. 0x0: SRAM LDO is not allowed to go to RET mode 0x1: SRAM LDO go to RET mode when all memory of voltage domain are RET	RW	0

Table 3-889. Register Call Summary for Register PRM_SLDO_CORE_CTRL

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- DEVICE_PRM Register Summary: [0]

Table 3-890. PRM_SLDO_MPU_SETUP

Address Offset	0x0000 00CC		
Physical Address	0x4AE0 7CCC	**Instance**	DEVICE_PRM
Description	Setup of the SRAM LDO for MPU voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							AIPOFF	ENFUNC5	ENFUNC4	ENFUNC3	ENFUNC2	ENFUNC1	ABBOFF_SLEEP	ABBOFF_ACT	RESERVED

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	AIPOFF	Override on AIPOFF input of SRAM LDO. 0x0: AIPOFF signal is not overriden 0x1: AIPOFF signal is overriden to '1'. Corresponding SRAM LDO is disabled and in HZ mode.	RW	0
7	ENFUNC5	ENFUNC5 input of SRAM LDO. 0x0: Active to retention is a one step transfer 0x1: Active to retention is a two steps transfer	RW	0
6	ENFUNC4	ENFUNC4 input of SRAM LDO. 0x0: One external clock is supplied 0x1: No external clock is supplied	RW	0
5	ENFUNC3	ENFUNC3 input of SRAM LDO. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: Sub regulation is disabled 0x1: Sub regulation is enabled	RW	0
4	ENFUNC2	ENFUNC2 input of SRAM LDO. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: External cap is used 0x1: External cap is not used	RW WSpecial	0
3	ENFUNC1	ENFUNC1 input of SRAM LDO. After PowerOn reset , this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: Short circuit protection is disabled 0x1: Short circuit protection is enabled	RW	0
2	ABBOFF_SLEEP	Determines whether SRAMNWA is supplied by VDDS or VDDAR during deep-sleep. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	1
1	ABBOFF_ACT	Determines whether SRAMNWA is supplied by VDDS or VDDAR during active mode. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	1
0	RESERVED	Reserved	R	0

Table 3-891. Register Call Summary for Register PRM_SLDO_MPU_SETUP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-892. PRM_SLDO_MPU_CTRL

Address Offset	0x0000 00D0		
Physical Address	0x4AE0 7CD0	**Instance**	DEVICE_PRM
Description	Control and status of the SRAM LDO for MPU voltage domain. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						SRAM_IN_TRANSITION	SRAMLDO_STATUS	RESERVED							RETMODE_ENABLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	SRAM_IN_TRANSITION	Status indicating SRAM LDO state machine state. Read 0x0: SRAM LDO state machine is stable Read 0x1: SRAM LDO state machine is in transition state	R	0
8	SRAMLDO_STATUS	SRAMLDO status Read 0x0: SRAMLDO is in ACTIVE mode. Read 0x1: SRAMLDO is on RETENTION mode.	R	0
7:1	RESERVED		R	0x00
0	RETMODE_ENABLE	Control if the SRAM LDO retention mode is used or not. 0x0: SRAM LDO is not allowed to go to RET mode 0x1: SRAM LDO go to RET mode when all memory of voltage domain are RET	RW	0

Table 3-893. Register Call Summary for Register PRM_SLDO_MPU_CTRL

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-894. PRM_SLDO_MM_SETUP

Address Offset	0x0000 00D4		
Physical Address	0x4AE0 7CD4	**Instance**	DEVICE_PRM
Description	Setup of the SRAM LDO for MM voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							AIPOFF	ENFUNC5	ENFUNC4	ENFUNC3	ENFUNC2	ENFUNC1	ABBOFF_SLEEP	ABBOFF_ACT	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	AIPOFF	Override on AIPOFF input of SRAM LDO. 0x0: AIPOFF signal is not overriden 0x1: AIPOFF signal is overriden to '1'. Corresponding SRAM LDO is disabled and in HZ mode.	RW	0
7	ENFUNC5	ENFUNC5 input of SRAM LDO. 0x0: Active to retention is a one step transfer 0x1: Active to retention is a two steps transfer	RW	0

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Bits	Field Name	Description	Type	Reset
6	ENFUNC4	ENFUNC4 input of SRAM LDO. 0x0: One external clock is supplied 0x1: No external clock is supplied	RW	0
5	ENFUNC3	ENFUNC3 input of SRAM LDO. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: Sub regulation is disabled 0x1: Sub regulation is enabled	RW	0
4	ENFUNC2	ENFUNC2 input of SRAM LDO. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: External cap is used 0x1: External cap is not used	RW WSpecial	0
3	ENFUNC1	ENFUNC1 input of SRAM LDO. After PowerOn reset , this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: Short circuit protection is disabled 0x1: Short circuit protection is enabled	RW	0
2	ABBOFF_SLEEP	Determines whether SRAMNWA is supplied by VDDS or VDDAR during deep-sleep. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	1
1	ABBOFF_ACT	Determines whether SRAMNWA is supplied by VDDS or VDDAR during active mode. After PowerOn reset, this bitfield is automatically loaded with a value from control module. Bitfield remains writable after this. 0x0: SRAMNWA supplied with VDDS 0x1: SRAMNWA supplied with VDDAR	RW WSpecial	1
0	RESERVED	Reserved	R	0

Table 3-895. Register Call Summary for Register PRM_SLDO_MM_SETUP

PRCM Register Manual
- DEVICE_PRM Register Summary: [0]

Table 3-896. PRM_SLDO_MM_CTRL

Address Offset	0x0000 00D8		
Physical Address	0x4AE0 7CD8	**Instance**	DEVICE_PRM
Description	Control and status of the SRAM LDO for MM voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						SRAM_IN_TRANSITION	SRAMLDO_STATUS	RESERVED							RETMODE_ENABLE

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	SRAM_IN_TRANSITION	Status indicating SRAM LDO state machine state. Read 0x0: SRAM LDO state machine is stable Read 0x1: SRAM LDO state machine is in transition state	R	0
8	SRAMLDO_STATUS	SRAMLDO status Read 0x0: SRAMLDO is in ACTIVE mode. Read 0x1: SRAMLDO is on RETENTION mode.	R	0
7:1	RESERVED		R	0x00
0	RETMODE_ENABLE	Control if the SRAM LDO retention mode is used or not. 0x0: SRAM LDO is not allowed to go to RET mode 0x1: SRAM LDO go to RET mode when all memory of voltage domain are RET	RW	0

Table 3-897. Register Call Summary for Register PRM_SLDO_MM_CTRL

PRCM Register Manual

- DEVICE_PRM Register Summary: [0]

Table 3-898. PRM_ABBLDO_MPU_SETUP

Address Offset	0x0000 00DC		
Physical Address	0x4AE0 7CDC	**Instance**	DEVICE_PRM
Description	Selects the ABBLDO_MPU mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SR2_WTCNT_VALUE								RESERVED				RESERVED	ACTIVE_FBB_SEL	ACTIVE_RBB_SEL	SR2EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	SR2_WTCNT_VALUE	LDO settling time for active-mode OPP change. Counting at a 16 system clock cycles rate. [warm reset insensitive]	RW	0x00
7:4	RESERVED		R	0x0
3	RESERVED		R	0
2	ACTIVE_FBB_SEL	Defines ABBLDO mode when voltage is in slow fast OPP. [warm reset insensitive] 0x0: ABBLDO is in bypass mode 0x1: ABBLDO is in FBB mode	RW	0
1	RESERVED		R	0
0	SR2EN	Enable ABB power management 0x0: ABBLDO is put in bypass mode 0x1: ABBLDO will operate accordingly to settings	RW	0

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Table 3-899. Register Call Summary for Register PRM_ABBLDO_MPU_SETUP

Voltage-Management Functional Description • ABB LDOs Control: [0]
PRCM Register Manual • DEVICE_PRM Register Summary: [1]

Table 3-900. PRM_ABBLDO_MPU_CTRL

Address Offset	0x0000 00E0		
Physical Address	0x4AE0 7CE0	**Instance**	DEVICE_PRM
Description	Control and Status of ABB on MPU voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SR2_IN_TRANSITION	RESERVED	SR2_STATUS			OPP_CHANGE	OPP_SEL	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	SR2_IN_TRANSITION	Indicates VBBLDO_CON is or is not in transition state. This output should be used by programming interface to clear OPP_CHANGE bit as an indication of OPP change completion. Read 0x0: Read 0x1: Indicates that VBBLDO_CON is in transition and SR2_STATUS bits are not stable to read.	R	0
5	RESERVED		R	0
4:3	SR2_STATUS	Indicate ABBLDO current operation status Read 0x0: ABBLDO is placed in bypass mode. Read 0x1: Reserved Read 0x2: ABBLDO is placed in FBB active mode. Read 0x3: Reserved	R	0x0
2	OPP_CHANGE	When OPP_CHANGE is set to 1, VBBLDO_CON samples OPP_SEL and ACTIVE_FBB_SEL upon detecting rising edge. VBBLDO_CON asserts signal SR2_IN_TRANSITION in response to OPP_CHANGE. OPP_CHANGE should be cleared to 0 when SR2_IN_TRANSITION from VBBLDO_CON is de-asserted.	RW WSpecial	0
1:0	OPP_SEL	Selects the OPP at which the MPU voltage domain is operating 0x0: default : Nominal 0x1: Fast OPP 0x2: Nominal 0x3: Slow OPP	RW	0x0

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Table 3-901. Register Call Summary for Register PRM_ABBLDO_MPU_CTRL

Voltage-Management Functional Description • ABB LDOs Control: [0]
PRCM Register Manual • DEVICE_PRM Register Summary: [1]

Table 3-902. PRM_ABBLDO_MM_SETUP

Address Offset	0x0000 00E4		
Physical Address	0x4AE0 7CE4	**Instance**	DEVICE_PRM
Description	Selects the ABBLDO_MM mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SR2_WTCNT_VALUE								RESERVED				RESERVED	ACTIVE_FBB_SEL	ACTIVE_RBB_SEL	SR2EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	SR2_WTCNT_VALUE	LDO settling time for active-mode OPP change. Counting at a 16 system clock cycles rate. [warm reset insensitive]	RW	0x00
7:4	RESERVED		R	0x0
3	RESERVED		R	0
2	ACTIVE_FBB_SEL	Defines ABBLDO mode when voltage is in slow fast OPP. [warm reset insensitive] 0x0: ABBLDO is in bypass mode 0x1: ABBLDO is in FBB mode	RW	0
1	RESERVED		R	0
0	SR2EN	Enable ABB power management 0x0: ABBLDO is put in bypass mode 0x1: ABBLDO will operate accordingly to settings	RW	0

Table 3-903. Register Call Summary for Register PRM_ABBLDO_MM_SETUP

Voltage-Management Functional Description • ABB LDOs Control: [0]
PRCM Register Manual • DEVICE_PRM Register Summary: [1]

Table 3-904. PRM_ABBLDO_MM_CTRL

Address Offset	0x0000 00E8		
Physical Address	0x4AE0 7CE8	**Instance**	DEVICE_PRM
Description	Control and Status of ABB on MM voltage domain. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SR2_IN_TRANSITION	RESERVED	SR2_STATUS		OPP_CHANGE		OPP_SEL	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	SR2_IN_TRANSITION	Indicates VBBLDO_CON is or is not in transition state. This output should be used by programming interface to clear OPP_CHANGE bit as an indication of OPP change completion. Read 0x0: Read 0x1: Indicates that VBBLDO_CON is in transition and SR2_STATUS bits are not stable to read.	R	0
5	RESERVED		R	0
4:3	SR2_STATUS	Indicate ABBLDO current operation status Read 0x0: ABBLDO is placed in bypass mode. Read 0x1: Reserved Read 0x2: ABBLDO is placed in FBB active mode. Read 0x3: Reserved	R	0x0
2	OPP_CHANGE	When OPP_CHANGE is set to 1, VBBLDO_CON samples OPP_SEL and ACTIVE_FBB_SEL upon detecting rising edge. VBBLDO_CON asserts signal SR2_IN_TRANSITION in response to OPP_CHANGE. OPP_CHANGE should be cleared to 0 when SR2_IN_TRANSITION from VBBLDO_CON is de-asserted.	RW WSpecial	0
1:0	OPP_SEL	Selects the OPP at which the MM voltage domain is operating (Fast OPP, Nominal OPP or Slow OPP) 0x0: default : Nominal 0x1: Fast OPP 0x2: Nominal 0x3: Slow OPP	RW	0x0

Table 3-905. Register Call Summary for Register PRM_ABBLDO_MM_CTRL

Voltage-Management Functional Description • ABB LDOs Control: [0]
PRCM Register Manual • DEVICE_PRM Register Summary: [1]

Table 3-906. PRM_BANDGAP_SETUP

Address Offset	0x0000 00EC		
Physical Address	0x4AE0 7CEC	**Instance**	DEVICE_PRM
Description	Setup of the BANDGAPTS. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STARTUP_COUNT							

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STARTUP_COUNT	Determines the start-up duration of BANDGAPTS. The duration is computed as 32 x NbCycles of system clock cycles.	RW	0x78

Table 3-907. Register Call Summary for Register PRM_BANDGAP_SETUP

Voltage-Management Functional Description • BANDGAPsControl: [0]
PRCM Register Manual • DEVICE_PRM Register Summary: [1]

Table 3-908. PRM_VOLTST_MPU

Address Offset	0x0000 0110		
Physical Address	0x4AE0 7D10	**Instance**	DEVICE_PRM
Description	This register provides a status on the current MPU voltage domain state. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											INTRANSITION	RESERVED																		VOLTSTATEST	

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	INTRANSITION	Domain transition status Read 0x1: Voltage domain transition is in progress. Read 0x0: No on-going transition on voltage domain	R	0
19:2	RESERVED		R	0x0 0000
1:0	VOLTSTATEST	Current voltage state status Read 0x3: Voltage domain is ON Read 0x2: Voltage domain is SLEEP Read 0x1: Voltage domain is in RETENTION Read 0x0: Reserved	R	0x3

Table 3-909. Register Call Summary for Register PRM_VOLTST_MPU

Voltage-Management Functional Description • Overview: [0] • VDD_x_L Transitions: [1]
PRCM Register Manual • DEVICE_PRM Register Summary: [2]

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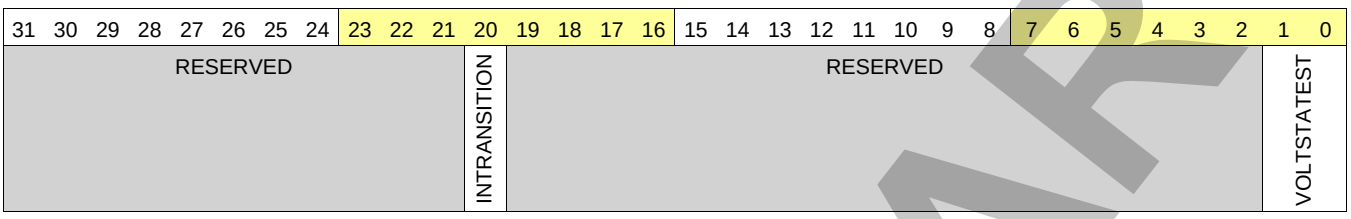
Table 3-910. PRM_VOLTST_MM

Address Offset	0x0000 0114		
Physical Address	0x4AE0 7D14	**Instance**	DEVICE_PRM
Description	This register provides a status on the current MM voltage domain state. [warm reset insensitive]		
Type	R		



Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	INTRANSITION	Domain transition status Read 0x1: Voltage domain transition is in progress. Read 0x0: No on-going transition on voltage domain	R	0
19:2	RESERVED		R	0x0 0000
1:0	VOLTSTATEST	Current voltage state status Read 0x3: Voltage domain is ON Read 0x2: Voltage domain is SLEEP Read 0x1: Voltage domain is in RETENTION Read 0x0: Reserved	R	0x3

Table 3-911. Register Call Summary for Register PRM_VOLTST_MM

Voltage-Management Functional Description
- Overview: [0]
- VDD_x_L Transitions: [1]

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- DEVICE_PRM Register Summary: [2]

3.11.20 INSTR_PRM Registers

3.11.20.1 INSTR_PRM Register Summary

Table 3-912. INSTR_PRM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INSTR_PRM Base Address
PMI_IDENTICATION	R	32	0x0000 0000	0x4AE0 7F00
PMI_SYS_CONFIG	RW	32	0x0000 0010	0x4AE0 7F10
PMI_STATUS	R	32	0x0000 0014	0x4AE0 7F14
PMI_CONFIGURATION	RW	32	0x0000 0024	0x4AE0 7F24
PMI_CLASS_FILTERING	RW	32	0x0000 0028	0x4AE0 7F28
PMI_TRIGGERING	RW	32	0x0000 002C	0x4AE0 7F2C
PMI_SAMPLING	RW	32	0x0000 0030	0x4AE0 7F30

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3.11.20.2 INSTR_PRM Register Description

Table 3-913. PMI_IDENTICATION

Address Offset	0x0000 0000		
Physical Address	0x4AE0 7F00	**Instance**	INSTR_PRM
Description	PM profiling identification register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	0x-- TI Internal data.

Table 3-914. Register Call Summary for Register PMI_IDENTICATION

PRCM Register Manual

- INSTR_PRM Register Summary: [0]

Table 3-915. PMI_SYS_CONFIG

Address Offset	0x0000 0010		
Physical Address	0x4AE0 7F10	**Instance**	INSTR_PRM
Description	PM profiling system configuartion register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED		IDLEMODE		RESERVED		SOFTRESET	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	RESERVED	Reserved	R	0x0
3:2	IDLEMODE	Configuration of the local tartget state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters idle state. Backup mode, for debug only. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the module's internal requirements. Module shall not generate (IRQ- or DMA-request-related) wakeup events. 0x3: Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the module's internal requirements. Module may generate (IRQ- or DMA-request-related) wakeup events when in idle state. Mode is only relevant if the appropriate module swakeup output(s) is (are) implemented.	RW	0x2

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Bits	Field Name	Description	Type	Reset
1	RESERVED	Reserved	R	0
0	SOFTRESET	Software reset read 0x0: Reset done, no pending action write 0x0: No action write 0x1: Initiate software reset read 0x1: Reset (software or other) ongoing	RW	0

Table 3-916. Register Call Summary for Register PMI_SYS_CONFIG

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

Table 3-917. PMI_STATUS

Address Offset	0x0000 0014		
Physical Address	0x4AE0 7F14	**Instance**	INSTR_PRM
Description	PM profiling status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FIFOEMPTY	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FIFOEMPTY	PM Profiling buffer empty status 0x0: PM profiling buffer not empty – PM events not yet exported 0x1: PM profiling buffer empty	R	1
7:0	RESERVED	Reserved	R	0x00

Table 3-918. Register Call Summary for Register PMI_STATUS

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

Table 3-919. PMI_CONFIGURATION

Address Offset	0x0000 0024		
Physical Address	0x4AE0 7F24	**Instance**	INSTR_PRM
Description	PM profiling configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAIM_3		CLAIM_2	CLAIM_1	RESERVED				RESERVED								RESERVED								EVT_CAPT_EN	RESERVED						

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Bits	Field Name	Description	Type	Reset
31:30	CLAIM_3	Ownership	RW	0x0
29	CLAIM_2	Debugger override qualifier	RW	1
28	CLAIM_1	Current owner	R	0
27:24	RESERVED	Reserved	R	0x0
23	RESERVED	Reserved	R	0
22:16	RESERVED	Reserved	R	0x00
15	RESERVED	Reserved	R	0
14:8	RESERVED	Reserved	R	0x00
7	EVT_CAPT_EN	When HIGH the PM events capture is enabled	RW	0
6:0	RESERVED	Reserved	R	0x00

Table 3-920. Register Call Summary for Register PMI_CONFIGURATION

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

Table 3-921. PMI_CLASS_FILTERING

Address Offset	0x0000 0028		
Physical Address	0x4AE0 7F28	**Instance**	INSTR_PRM
Description	PM profiling class filtering register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SNAP_CAPT_EN_03	SNAP_CAPT_EN_02	SNAP_CAPT_EN_01	SNAP_CAPT_EN_00

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	SNAP_CAPT_EN_03	Snapshot capture enable - Class-ID = 0x03	RW	0
2	SNAP_CAPT_EN_02	Snapshot capture enable - Class-ID = 0x02	RW	0
1	SNAP_CAPT_EN_01	Snapshot capture enable - Class-ID = 0x01	RW	0
0	SNAP_CAPT_EN_00	Snapshot capture enable - Class-ID = 0x00	RW	0

Table 3-922. Register Call Summary for Register PMI_CLASS_FILTERING

PRCM Register Manual
- INSTR_PRM Register Summary: [0]

Table 3-923. PMI_TRIGGERING

Address Offset	0x0000 002C		
Physical Address	0x4AE0 7F2C	**Instance**	INSTR_PRM
Description	PM profiling triggering control register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TRIG_STOP_EN	TRIG_START_EN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	TRIG_STOP_EN	Enable stop capturing PM events from external trigger detection	RW	0
0	TRIG_START_EN	Enable start capturing PM events from external trigger detection	RW	0

Table 3-924. Register Call Summary for Register PMI_TRIGGERING

PRCM Register Manual • INSTR_PRM Register Summary: [0]

Table 3-925. PMI_SAMPLING

Address Offset	0x0000 0030		
Physical Address	0x4AE0 7F30	**Instance**	INSTR_PRM
Description	PM profiling sampling window register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FCLK_DIV_FACOR				RESERVED								SAMP_WIND_SIZE							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:16	FCLK_DIV_FACOR	FunClk divide factor ranging from 1 to 16	RW	0x0
15:8	RESERVED	Reserved	R	0x00
7:0	SAMP_WIND_SIZE	PM events sampling window size	RW	0x00

Table 3-926. Register Call Summary for Register PMI_SAMPLING

PRCM Register Manual • INSTR_PRM Register Summary: [0]

3.11.21 CM_CORE_AON Instance Summary

Table 3-927. CM_CORE_AON Instance Summary

Module Name	Base Address	Size
INTRCONN_SOCKET_CM_CORE_AON	0x4A00 4000	256 bytes
CKGEN_CM_CORE_AON	0x4A00 4100	512 bytes
MPU_CM_CORE_AON	0x4A00 4300	256 bytes

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Table 3-927. CM_CORE_AON Instance Summary (continued)

Module Name	Base Address	Size
DSP_CM_CORE_AON	0x4A00 4400	256 bytes
ABE_CM_CORE_AON	0x4A00 4500	256 bytes
RESERVED	0x4A00 4E00	256 bytes
INSTR_CM_CORE_AON	0x4A00 4F00	256 bytes

3.11.22 INTRCONN_SOCKET_CM_CORE_AON Registers

3.11.22.1 INTRCONN_SOCKET_CM_CORE_AON Register Summary

Table 3-928. INTRCONN_SOCKET_CM_CORE_AON Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INTRCONN_SOCKET_CM_CORE_AON Base Address
REVISION_CM_CORE_AON	R	32	0x0000 0000	0x4A00 4000
CM_CM_CORE_AON_PROFILING_CLKCTRL	RW	32	0x0000 0040	0x4A00 4040
CM_CORE_AON_DEBUG_CFG	RW	32	0x0000 0080	0x4A00 4080

3.11.22.2 INTRCONN_SOCKET_CM_CORE_AON Register Description

Table 3-929. REVISION_CM_CORE_AON

Address Offset	0x0000 0000		
Physical Address	0x4A00 4000	**Instance**	INTRCONN_SOCKET_CM_CORE_AON
Description	This register contains the IP revision code for the CM_CORE_AON part of the PRCM		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	Revision Number	R	0x- - TI Internal data.

Table 3-930. Register Call Summary for Register REVISION_CM_CORE_AON

PRCM Register Manual
- INTRCONN_SOCKET_CM_CORE_AON Register Summary: [0]

Table 3-931. CM_CM_CORE_AON_PROFILING_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A00 4040	**Instance**	INTRCONN_SOCKET_CM_CORE_AON
Description	This register manages the CM_CORE_AON_PROFILING clocks.[warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:16	IDLEST	Module idle status Read 0x0: Module is fully functional Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle Read 0x3: Module is disabled	R	0x3
15:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. INTRCONN configuration port is not accessible. 0x1: Module is managed automatically by HW along with CM_CORE_AON and EMU domain. INTRCONN configuration port is accessible only when EMU domain is on. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-932. Register Call Summary for Register CM_CM_CORE_AON_PROFILING_CLKCTRL

PRCM Register Manual

- INTRCONN_SOCKET_CM_CORE_AON Register Summary: [0]

Table 3-933. CM_CORE_AON_DEBUG_CFG

Address Offset	0x0000 0080		
Physical Address	0x4A00 4080	**Instance**	INTRCONN_SOCKET_CM_CORE_AON
Description	This register is used to configure the CM_CORE_AON's 32-bit debug output. There is one 7-bit source select field for selecting from a shared set of 8-bit internal signal blocks per byte. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	SEL3							RESERVED	SEL2							RESERVED	SEL1							RESERVED	SEL0						

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30:24	SEL3	Internal signal block select for debug word byte-3	RW	0x03
23	RESERVED		R	0
22:16	SEL2	Internal signal block select for debug word byte-2	RW	0x02
15	RESERVED		R	0
14:8	SEL1	Internal signal block select for debug word byte-1	RW	0x01

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Bits	Field Name	Description	Type	Reset
7	RESERVED		R	0
6:0	SEL0	Internal signal block select for debug word byte-0	RW	0x00

Table 3-934. Register Call Summary for Register CM_CORE_AON_DEBUG_CFG

PRCM Register Manual
- INTRCONN_SOCKET_CM_CORE_AON Register Summary: [0]

3.11.23 CKGEN_CM_CORE_AON Registers

3.11.23.1 CKGEN_CM_CORE_AON Register Summary

Table 3-935. CKGEN_CM_CORE_AON Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM_CORE_AON Base Address
CM_CLKSEL_CORE	RW	32	0x0000 0000	0x4A00 4100
CM_CLKSEL_ABE	RW	32	0x0000 0008	0x4A00 4108
CM_DLL_CTRL	RW	32	0x0000 0010	0x4A00 4110
CM_CLKMODE_DPLL_CORE	RW	32	0x0000 0020	0x4A00 4120
CM_IDLEST_DPLL_CORE	R	32	0x0000 0024	0x4A00 4124
CM_AUTOIDLE_DPLL_CORE	RW	32	0x0000 0028	0x4A00 4128
CM_CLKSEL_DPLL_CORE	RW	32	0x0000 002C	0x4A00 412C
CM_DIV_M2_DPLL_CORE	RW	32	0x0000 0030	0x4A00 4130
CM_DIV_M3_DPLL_CORE	RW	32	0x0000 0034	0x4A00 4134
CM_DIV_H11_DPLL_CORE	RW	32	0x0000 0038	0x4A00 4138
CM_DIV_H12_DPLL_CORE	RW	32	0x0000 003C	0x4A00 413C
CM_DIV_H13_DPLL_CORE	RW	32	0x0000 0040	0x4A00 4140
CM_DIV_H14_DPLL_CORE	RW	32	0x0000 0044	0x4A00 4144
CM_SSC_DELTAMSTEP_DPLL_CORE	RW	32	0x0000 0048	0x4A00 4148
CM_SSC_MODFREQDIV_DPLL_CORE	RW	32	0x0000 004C	0x4A00 414C
CM_DIV_H22_DPLL_CORE	RW	32	0x0000 0054	0x4A00 4154
CM_DIV_H23_DPLL_CORE	RW	32	0x0000 0058	0x4A00 4158
CM_DIV_H24_DPLL_CORE	RW	32	0x0000 005C	0x4A00 415C
CM_CLKMODE_DPLL_MPU	RW	32	0x0000 0060	0x4A00 4160
CM_IDLEST_DPLL_MPU	R	32	0x0000 0064	0x4A00 4164
CM_AUTOIDLE_DPLL_MPU	RW	32	0x0000 0068	0x4A00 4168
CM_CLKSEL_DPLL_MPU	RW	32	0x0000 006C	0x4A00 416C
CM_DIV_M2_DPLL_MPU	RW	32	0x0000 0070	0x4A00 4170
CM_SSC_DELTAMSTEP_DPLL_MPU	RW	32	0x0000 0088	0x4A00 4188
CM_SSC_MODFREQDIV_DPLL_MPU	RW	32	0x0000 008C	0x4A00 418C
CM_BYPCLK_DPLL_MPU	RW	32	0x0000 009C	0x4A00 419C
CM_CLKMODE_DPLL_IVA	RW	32	0x0000 00A0	0x4A00 41A0
CM_IDLEST_DPLL_IVA	R	32	0x0000 00A4	0x4A00 41A4
CM_AUTOIDLE_DPLL_IVA	RW	32	0x0000 00A8	0x4A00 41A8
CM_CLKSEL_DPLL_IVA	RW	32	0x0000 00AC	0x4A00 41AC
CM_DIV_H11_DPLL_IVA	RW	32	0x0000 00B8	0x4A00 41B8
CM_DIV_H12_DPLL_IVA	RW	32	0x0000 00BC	0x4A00 41BC
CM_SSC_DELTAMSTEP_DPLL_IVA	RW	32	0x0000 00C8	0x4A00 41C8
CM_SSC_MODFREQDIV_DPLL_IVA	RW	32	0x0000 00CC	0x4A00 41CC

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Table 3-935. CKGEN_CM_CORE_AON Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM_CORE_AON Base Address
CM_BYPCLK_DPLL_IVA	RW	32	0x0000 00DC	0x4A00 41DC
CM_CLKMODE_DPLL_ABE	RW	32	0x0000 00E0	0x4A00 41E0
CM_IDLEST_DPLL_ABE	R	32	0x0000 00E4	0x4A00 41E4
CM_AUTOIDLE_DPLL_ABE	RW	32	0x0000 00E8	0x4A00 41E8
CM_CLKSEL_DPLL_ABE	RW	32	0x0000 00EC	0x4A00 41EC
CM_DIV_M2_DPLL_ABE	RW	32	0x0000 00F0	0x4A00 41F0
CM_DIV_M3_DPLL_ABE	RW	32	0x0000 00F4	0x4A00 41F4
CM_SSC_DELTAMSTEP_DPLL_ABE	RW	32	0x0000 0108	0x4A00 4208
CM_SSC_MODFREQDIV_DPLL_ABE	RW	32	0x0000 010C	0x4A00 420C
CM_SHADOW_FREQ_CONFIG1	RW	32	0x0000 0160	0x4A00 4260
CM_SHADOW_FREQ_CONFIG2	RW	32	0x0000 0164	0x4A00 4264
CM_DYN_DEP_PRESCAL	RW	32	0x0000 0170	0x4A00 4270
Reserved	R	32	0x0000 0180	0x4A00 4280

3.11.23.2 CKGEN_CM_CORE_AON Register Description

Table 3-936. CM_CLKSEL_CORE

Address Offset	0x0000 0000		
Physical Address	0x4A00 4100	**Instance**	CKGEN_CM_CORE_AON
Description	CORE module clock selection.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKSEL_L4	RESERVED			CLKSEL_L3	RESERVED			

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKSEL_L4	Selects L4 interconnect clock (L4_CLK) 0x0: L4_CLK is L3_CLK divided by 1 0x1: L4_CLK is L3_CLK divided by 2, to be used for both OPP_NOM and OPP_LOW	RW	0
7:5	RESERVED		R	0x0
4	CLKSEL_L3	Selects L3 interconnect clock (L3_CLK) 0x0: L3_CLK is CORE_CLK divided by 1 0x1: L3_CLK is CORE_CLK divided by 2, to be used for both OPP_NOM and OPP_LOW	RW	0
3:0	RESERVED		R	0x0

Table 3-937. Register Call Summary for Register CM_CLKSEL_CORE

Clock Management Functional Description • CM_CORE_AON Clock Generator: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2] • CKGEN_CM_CORE_AON Register Description: [3]

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Table 3-938. CM_CLKSEL_ABE

Address Offset	0x0000 0008		
Physical Address	0x4A00 4108	**Instance**	CKGEN_CM_CORE_AON
Description	ABE module clock selection.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					SLIMBUS1_CLK_GATE	RESERVED	PAD_CLKS_GATE	RESERVED							CLKSEL_OPP

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	SLIMBUS1_CLK_GATE	Gating control for SLIMBUS_CLK clock tree in ABE. 0x0: The clock is gated 0x1: The clock is enabled	RW	0
9	RESERVED		R	0
8	PAD_CLKS_GATE	Gating control for PAD_CLKS clock tree in ABE 0x0: The clock is gated 0x1: The clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	CLKSEL_OPP	Selects the OPP divider ABE domain 0x0: ABE_CLK is divide by 1 of DPLL_ABE_X2_CLK, to be used for OPP_NOM 0x1: ABE_CLK is divide by 2 of DPLL_ABE_X2_CLK, to be used for OPP_LOW 0x2: ABE_CLK is divide by 4 of DPLL_ABE_X2_CLK 0x3: Reserved	RW	0x0

Table 3-939. Register Call Summary for Register CM_CLKSEL_ABE

Clock Management Functional Description
- CKGEN_ABE Clock Generator: [0] [1] [2] [3]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [4]

Table 3-940. CM_DLL_CTRL

Address Offset	0x0000 0010		
Physical Address	0x4A00 4110	**Instance**	CKGEN_CM_CORE_AON
Description	Special register for DLL control		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DLL_OVERRIDE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DLL_OVERRIDE	Control if DLL lock and code outputs are overriden or not 0x0: Lock and code outputs are not overriden 0x1: Lock output is overriden to '1' and code output is overriden with a value coming from control module.	RW	1

Table 3-941. Register Call Summary for Register CM_DLL_CTRL

PRCM Register Manual

- CKGEN_CM_CORE_AON Register Summary: [0]
- CKGEN_CM_CORE_AON Register Description: [1]

Table 3-942. CM_CLKMODE_DPLL_CORE

Address Offset	0x0000 0020		
Physical Address	0x4A00 4120	**Instance**	CKGEN_CM_CORE_AON
Description	This register allows controlling the DPLL modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED							DPLL_EN

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0

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Bits	Field Name	Description	Type	Reset
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Read 0x0: REGM4XEN mode of the DPLL is disabled	R	0
10	DPLL_LPMODE_EN	Set the DPLL in Low Power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low power mode of the DPLL is disabled 0x1: Low power mode of the DPLL is enabled	RW	0
9	RESERVED		R	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00
2:0	DPLL_EN	DPLL control 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: Put the DPLL in Idle Bypass Low Power mode. 0x6: Put the DPLL in Idle Bypass Fast Relock mode. 0x7: Enables the DPLL in Lock mode	RW	0x5

Table 3-943. Register Call Summary for Register CM_CLKMODE_DPLL_CORE

Clock Management Functional Description
- Power Modes: [0] [1]
- Recalibration: [2]
- Spread Spectrum Clocking: [5] [6] [7]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [8]
- CKGEN_CM_CORE_AON Register Description: [9]

Table 3-944. CM_IDLEST_DPLL_CORE

Address Offset	0x0000 0024		
Physical Address	0x4A00 4124	**Instance**	CKGEN_CM_CORE_AON
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											ST_DPLL_INIT	ST_DPLL_MODE			ST_DPLL_CLK

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000000
4	ST_DPLL_INIT	DPLL init status (for debug purpose) Read 0x1: DPLL has been init Read 0x0: DPLL is not init	R	0
3:1	ST_DPLL_MODE	DPLL mode status (for debug purpose) Read 0x0: Transient state. From reset to any LP (low power) idle state or from any power state to any power state (Power states are Low Power Stop mode, Fast Relock Stop mode, Idle Bypass Low Power mode and Idle Bypass Fast Relock mode). Read 0x1: The DPLL is in Low Power Stop mode Read 0x2: The DPLL is in Fast Relock Stop mode Read 0x3: reserved Read 0x4: reserved Read 0x5: The DPLL is in Idle Bypass Low Power mode Read 0x6: The DPLL is in Idle Bypass Fast Relock mode Read 0x7: reserved	R	0
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-945. Register Call Summary for Register CM_IDLEST_DPLL_CORE

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [0]

Table 3-946. CM_AUTOIDLE_DPLL_CORE

Address Offset	0x0000 0028		
Physical Address	0x4A00 4128	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides automatic control over the DPLL activity.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														AUTO_DPLL_MODE	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000000
2:0	AUTO_DPLL_MODE	DPLL automatic control. 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in Low Power Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in Fast Relock Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in Idle Bypass Low Power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in Idle Bypass Fast Relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

Table 3-947. Register Call Summary for Register CM_AUTOIDLE_DPLL_CORE

Clock Management Functional Description • Power Modes: [0]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [1]

Table 3-948. CM_CLKSEL_DPLL_CORE

Address Offset	0x0000 002C		
Physical Address	0x4A00 412C	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	DCC_EN	RESERVED	DPLL_CLKOUTHIF_CLKSEL	RESERVED	DPLL_MULT											RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. In DPLL Locked mode: 0 - No impact; 1 - No impact In DPLL Bypass mode: 0x0 - CLKINP is selected as the BYPASS clock for CLKOUT/CLKOUTX2 0x1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT/CLKOUTX2	RW	0
22	DCC_EN	Duty-cycle corrector for high frequency clock read 0x0: Duty-cycle corrector is disabled	R	0x0
21	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
20	DPLL_CLKOUTHIF_CLKSEL	Selects the source of the DPLL CLKOUTHIF clock. 0x0: CLKOUTHIF is generated from the DPLL oscillator (DCO) 0x1: CLKOUTHIF is generated from CLKINPHIF	RW	0
19	RESERVED		R	0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). Equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M. [warm reset insensitive] 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1). [warm reset insensitive]	RW	0x00

Table 3-949. Register Call Summary for Register CM_CLKSEL_DPLL_CORE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-950. CM_DIV_M2_DPLL_CORE

Address Offset	0x0000 0030		
Physical Address	0x4A00 4130	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED					DIVHS			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	CLKST	DPLL CLKOUT status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:5	RESERVED		R	0x0
4:0	DIVHS	DPLL post-divider factor, M2, for internal clock generation (1 to 31); Divide value from 1 to 31. 0x0: Reserved 0x2: 2, to be used for OPP_NOM 0x4: 4, to be used for OPP_LOW	RW	0x01

Table 3-951. Register Call Summary for Register CM_DIV_M2_DPLL_CORE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2] • CKGEN_CM_CORE_AON Register Description: [3]

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Table 3-952. CM_DIV_M3_DPLL_CORE

Address Offset	0x0000 0034		
Physical Address	0x4A00 4134	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the M3 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED				DIVHS				

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	CLKST	DPLL CLKOUTHIF status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:5	RESERVED		R	0x0
4:0	DIVHS	DPLL M3 post-divider factor (1 to 31). 0x0: Reserved 0x5: 5, to be used for OPP_NOM 0x8: 8, to be used for OPP_LOW	RW	0x01

Table 3-953. Register Call Summary for Register CM_DIV_M3_DPLL_CORE

Clock Management Functional Description
- Synthesized Clock Parameters: [0] [1]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-954. CM_DIV_H11_DPLL_CORE

Address Offset	0x0000 0038		
Physical Address	0x4A00 4138	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the CLKOUT1 o/p of the HSDIVIDER1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED				DIVHS				

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	CLKST	HSDIVIDER1 CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED		R	0x0
5:0	DIVHS	DPLL (H11+1) post-divider factor (1 to 63). 0x0: Reserved 0x8: 8, to be used for both OPP_NOM and OPP_LOW	RW	0x1

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Table 3-955. Register Call Summary for Register CM_DIV_H11_DPLL_CORE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-956. CM_DIV_H12_DPLL_CORE

Address Offset	0x0000 003C		
Physical Address	0x4A00 413C	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED					DIVHS			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	CLKST	HSDIVIDER1 CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED		R	0x0
5:0	DIVHS	DPLL (H12+1) post-divider factor (1 to 63). 0x0: Reserved 0x4: 4, to be used for OPP_NOM 0x8: 8, to be used for OPP_LOW	RW	0x1

Table 3-957. Register Call Summary for Register CM_DIV_H12_DPLL_CORE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2] • CKGEN_CM_CORE_AON Register Description: [3]

Table 3-958. CM_DIV_H13_DPLL_CORE

Address Offset	0x0000 0040		
Physical Address	0x4A00 4140	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the CLKOUT3 o/p of the HSDIVIDER1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED					DIVHS			

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	CLKST	HSDIVIDER1 CLKOUT3 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED		R	0x0
5:0	DIVHS	DPLL (H13+1) post-divider factor (1 to 63). 0x0: Reserved 0x3E: 62, to be used for both OPP_NOM and OPP_LOW	RW	0x1

Table 3-959. Register Call Summary for Register CM_DIV_H13_DPLL_CORE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-960. CM_DIV_H14_DPLL_CORE

Address Offset	0x0000 0044		
Physical Address	0x4A00 4144	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the CLKOUT4 o/p of the HSDIVIDER1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED							DIVHS	

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	CLKST	HSDIVIDER1 CLKOUT4 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED		R	0x0
5:0	DIVHS	DPLL (H14+1) post-divider factor (1 to 63). When a value of 63 is programmed in this register, HSdivider will perform division by 2.5 that is divided by 2 at top level 0x0: Reserved	RW	0x1

Table 3-961. Register Call Summary for Register CM_DIV_H14_DPLL_CORE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

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Table 3-962. CM_SSC_DELTAMSTEP_DPLL_CORE

Address Offset	0x0000 0048		
Physical Address	0x4A00 4148	**Instance**	CKGEN_CM_CORE_AON
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELTAMSTEP																							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-963. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_CORE

Clock Management Functional Description
- Spread Spectrum Clocking: [0]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [1]

Table 3-964. CM_SSC_MODFREQDIV_DPLL_CORE

Address Offset	0x0000 004C		
Physical Address	0x4A00 414C	**Instance**	CKGEN_CM_CORE_AON
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						MODFREQDIV_EXPONENT		RESERVED	MODFREQDIV_MANTISSA						

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-965. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_CORE

Clock Management Functional Description
- Spread Spectrum Clocking: [0] [1]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [2]

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Table 3-966. CM_DIV_H22_DPLL_CORE

Address Offset	0x0000 0054		
Physical Address	0x4A00 4154	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED			DIVHS					

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	CLKST	HSDIVIDER2 CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED		R	0x0
5:0	DIVHS	DPLL (H22+1) post-divider factor (1 to 63). 0x0: Reserved 0x5: 5, to be used for OPP_NOM 0xA: 10, to be used for OPP_LOW	RW	0x1

Table 3-967. Register Call Summary for Register CM_DIV_H22_DPLL_CORE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-968. CM_DIV_H23_DPLL_CORE

Address Offset	0x0000 0058		
Physical Address	0x4A00 4158	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the CLKOUT3 o/p of the HSDIVIDER2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED			DIVHS					

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	CLKST	HSDIVIDER2 CLKOUT3 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5:0	DIVHS	DPLL (H23+1) post-divider factor (1 to 63). 0x0: Reserved 0x7: 7, to be used for OPP_NOM 0xE: 14, to be used for OPP_LOW	RW	0x1

Table 3-969. Register Call Summary for Register CM_DIV_H23_DPLL_CORE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-970. CM_DIV_H24_DPLL_CORE

Address Offset	0x0000 005C		
Physical Address	0x4A00 415C	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the CLKOUT4 o/p of the 2nd HSDIVIDER.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED					DIVHS			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00 0000
9	CLKST	HSDIVIDER2 CLKOUT4 status Read 0x1: The clock output is enabled Read 0x0: The clock output is gated	R	0
8:6	RESERVED		R	0x0
5:0	DIVHS	DPLL (H24+1) post-divider factor (1 to 63). 0x0: Reserved	RW	0x01

Table 3-971. Register Call Summary for Register CM_DIV_H24_DPLL_CORE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-972. CM_CLKMODE_DPLL_MPU

Address Offset	0x0000 0060		
Physical Address	0x4A00 4160	**Instance**	CKGEN_CM_CORE_AON
Description	This register allows controlling the DPLL modes.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED					DPLL_EN		

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Read 0x0: REGM4XEN mode of the DPLL is disabled	R	0
10	DPLL_LPMODE_EN	Set the DPLL in Low Power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low power mode of the DPLL is disabled 0x1: Low power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00
2:0	DPLL_EN	DPLL control 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: Put the DPLL in Idle Bypass Low Power mode. 0x6: Put the DPLL in Idle Bypass Fast Relock mode. 0x7: Enables the DPLL in Lock mode	RW	0x5

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Table 3-973. Register Call Summary for Register CM_CLKMODE_DPLL_MPU

Clock Management Functional Description
- Power Modes: [0] [1]
- Recalibration: [2]
- Spread Spectrum Clocking: [5] [6] [7]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [8]

Table 3-974. CM_IDLEST_DPLL_MPU

Address Offset	0x0000 0064		
Physical Address	0x4A00 4164	**Instance**	CKGEN_CM_CORE_AON
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											ST_DPLL_INIT	ST_DPLL_MODE			ST_DPLL_CLK

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000000
4	ST_DPLL_INIT	DPLL init status (for debug purpose) Read 0x1: DPLL has been init Read 0x0: DPLL is not init	R	0
3:1	ST_DPLL_MODE	DPLL mode status (for debug purpose) Read 0x0: Transient state. From reset to any LP (low power) idle state or from any power state to any power state (Power states are Low Power Stop mode, Fast Relock Stop mode, Idle Bypass Low Power mode and Idle Bypass Fast Relock mode). Read 0x1: The DPLL is in Low Power Stop mode. Read 0x2: The DPLL is in Fast Relock Stop mode. Read 0x3: reserved Read 0x4: reserved Read 0x5: The DPLL is in Idle Bypass Low Power mode. Read 0x6: The DPLL is in Idle Bypass Fast Relock mode Read 0x7: reserved	R	0
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-975. Register Call Summary for Register CM_IDLEST_DPLL_MPU

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [0]

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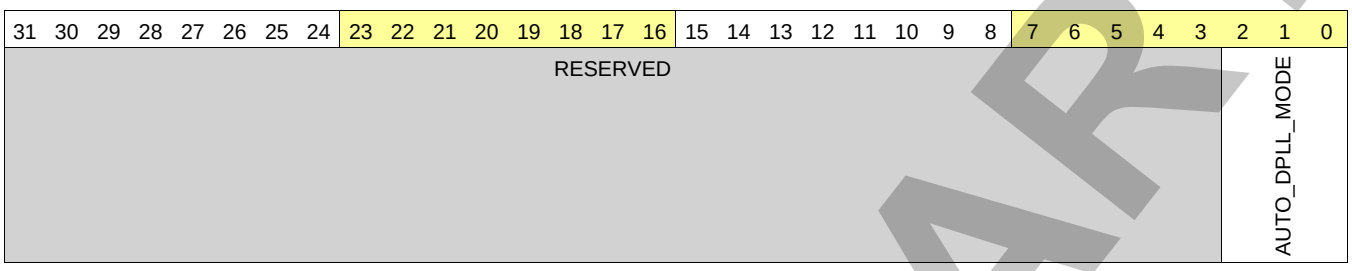
Table 3-976. CM_AUTOIDLE_DPLL_MPU

Address Offset	0x0000 0068		
Physical Address	0x4A00 4168	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides automatic control over the DPLL activity.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in Low Power Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in Fast Relock Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in Idle Bypass Low Power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in Idle Bypass Fast Relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

Table 3-977. Register Call Summary for Register CM_AUTOIDLE_DPLL_MPU

Clock Management Functional Description • Power Modes: [0]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [1]

Table 3-978. CM_CLKSEL_DPLL_MPU

Address Offset	0x0000 006C		
Physical Address	0x4A00 416C	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the DPLL.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	DCC_EN	RESERVED						DPLL_MULT								RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Only CLKINPULOW bypass clock supported for this PLL	R	1
22	DCC_EN	Duty-cycle corrector for high frequency clock 0x0: Duty-cycle corrector is disabled 0x1: Duty-cycle corrector is enabled	RW	0x0
21:19	RESERVED		R	0x0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047) Equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M. [warm reset insensitive] 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1). [warm reset insensitive]	RW	0x00

Table 3-979. Register Call Summary for Register CM_CLKSEL_DPLL_MPU

Clock Management Functional Description
- DPLLs Output Clocks Parameters: [0] [1]
- Synthesized Clock Parameters: [2] [3] [4]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [5]

Table 3-980. CM_DIV_M2_DPLL_MPU

Address Offset	0x0000 0070		
Physical Address	0x4A00 4170	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED				DIVHS				

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	CLKST	DPLL CLKOUT status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4:0	DIVHS	DPLL M2 post-divider factor (1 to 31). 0x0: Reserved 0x1: 1, to be used for OPP_NOM, OPP_HIGH and OPP_SPEEDBIN 0x2: 2, to be used for OPP_LOW	RW	0x01

Table 3-981. Register Call Summary for Register CM_DIV_M2_DPLL_MPU

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-982. CM_SSC_DELTAMSTEP_DPLL_MPU

Address Offset	0x0000 0088		
Physical Address	0x4A00 4188	**Instance**	CKGEN_CM_CORE_AON
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DELTAMSTEP															

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-983. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_MPU

Clock Management Functional Description • Spread Spectrum Clocking: [0]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [1]

Table 3-984. CM_SSC_MODFREQDIV_DPLL_MPU

Address Offset	0x0000 008C		
Physical Address	0x4A00 418C	**Instance**	CKGEN_CM_CORE_AON
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					MODFREQDIV_EXPONENT			RESERVED	MODFREQDIV_MANTISSA						

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-985. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_MPU

Clock Management Functional Description • Spread Spectrum Clocking: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-986. CM_BYPCLK_DPLL_MPU

Address Offset	0x0000 009C		
Physical Address	0x4A00 419C	**Instance**	CKGEN_CM_CORE_AON
Description	Control MPU PLL BYPASS clock. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CLKSEL	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	CLKSEL	Select the DPLL MPU bypass clock 0x0: DPLL_MPU bypass clock is CORE_X2_CLK divided by 1, to be used for both OPP_NOM and OPP_LOW 0x1: DPLL_MPU bypass clock is CORE_X2_CLK divided by 2 0x2: DPLL_MPU bypass clock is CORE_X2_CLK divided by 4 0x3: DPLL_MPU bypass clock is CORE_X2_CLK divided by 8	RW	0x0

Table 3-987. Register Call Summary for Register CM_BYPCLK_DPLL_MPU

Clock Management Functional Description • CM_CORE_AON Clock Generator: [0]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [1]

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Table 3-988. CM_CLKMODE_DPLL_IVA

Address Offset	0x0000 00A0		
Physical Address	0x4A00 41A0	**Instance**	CKGEN_CM_CORE_AON
Description	This register allows controlling the DPLL modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED							DPLL_EN

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Read 0x0: REGM4XEN mode of the DPLL is disabled	R	0
10	DPLL_LPMODE_EN	Set the DPLL in Low Power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low power mode of the DPLL is disabled 0x1: Low power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00

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Bits	Field Name	Description	Type	Reset
2:0	DPLL_EN	DPLL control 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: Put the DPLL in Idle Bypass Low Power mode. 0x6: Put the DPLL in Idle Bypass Fast Relock mode 0x7: Enables the DPLL in Lock mode	RW	0x5

Table 3-989. Register Call Summary for Register CM_CLKMODE_DPLL_IVA

Clock Management Functional Description
- Power Modes: [0] [1]
- Recalibration: [2]
- Spread Spectrum Clocking: [5] [6] [7]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [8]

Table 3-990. CM_IDLEST_DPLL_IVA

Address Offset	0x0000 00A4		
Physical Address	0x4A00 41A4	**Instance**	CKGEN_CM_CORE_AON
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											ST_DPLL_INIT	ST_DPLL_MODE			ST_DPLL_CLK

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000000
4	ST_DPLL_INIT	DPLL init status (for debug purpose) Read 0x1: DPLL has been init Read 0x0: DPLL is not init	R	0
3:1	ST_DPLL_MODE	DPLL mode status (for debug purpose) Read 0x0: Transient state. From reset to any LP (low power) idle state or from any power state to any power state (Power states are Low Power Stop mode, Fast Relock Stop mode, Idle Bypass Low Power mode and Idle Bypass Fast Relock mode). Read 0x1: The DPLL is in Low Power Stop mode. Read 0x2: The DPLL is in Fast Relock Stop mode. Read 0x3: reserved Read 0x4: reserved Read 0x5: The DPLL is in Idle Bypass Low Power mode. Read 0x6: The DPLL is in Idle Bypass Low Power mode. Read 0x7: reserved	R	0

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Bits	Field Name	Description	Type	Reset
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-991. Register Call Summary for Register CM_IDLEST_DPLL_IVA

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [0]

Table 3-992. CM_AUTOIDLE_DPLL_IVA

Address Offset	0x0000 00A8		
Physical Address	0x4A00 41A8	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides automatic control over the DPLL activity.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														AUTO_DPLL_MODE	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in Low Power Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in Fast Relock Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in Idle Bypass Low Power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in Idle Bypass Fast Relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

Table 3-993. Register Call Summary for Register CM_AUTOIDLE_DPLL_IVA

Clock Management Functional Description
- Power Modes: [0]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [1]

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Table 3-994. CM_CLKSEL_DPLL_IVA

Address Offset	0x0000 00AC		
Physical Address	0x4A00 41AC	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	DCC_EN	RESERVED						DPLL_MULT								RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. In DPLL Locked mode, 0 - No impact 1 - No impact In DPLL Bypass mode, 0 - CLKINP is selected as the BYPASS clock for CLKOUT/CLKOUTX2 1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT/CLKOUTX2	RW	0
22	DCC_EN	Duty-cycle corrector for high frequency clock Read 0: Duty-cycle corrector is disabled	R	0x0
21:19	RESERVED		R	0x0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). Equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M). [warm reset insensitive] 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1). [warm reset insensitive]	RW	0x00

Table 3-995. Register Call Summary for Register CM_CLKSEL_DPLL_IVA

Clock Management Functional Description
- Synthesized Clock Parameters: [0] [1]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-996. CM_DIV_H11_DPLL_IVA

Address Offset	0x0000 00B8		
Physical Address	0x4A00 41B8	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the CLKOUT1 o/p of the HSDIVIDER1.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED					DIVHS			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	CLKST	HSDIVIDER1 CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED		R	0x0
5:0	DIVHS	DPLL (H11+1) post-divider factor (1 to 63). 0x00: Reserved 0x2: 2, to be used for OPP_OD 0x5: 5, to be used for OPP_NOM 0xA: 10, to be used for OPP_LOW	RW	0x1

Table 3-997. Register Call Summary for Register CM_DIV_H11_DPLL_IVA

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-998. CM_DIV_H12_DPLL_IVA

Address Offset	0x0000 00BC		
Physical Address	0x4A00 41BC	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED					DIVHS			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	CLKST	HSDIVIDER1 CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED		R	0x0
5:0	DIVHS	DPLL (H12+1) post-divider factor (1 to 31). 0x00: Reserved 0x2: 2, to be used for OPP_OD 0x6: 6, to be used for OPP_NOM 0xC: 12, to be used for OPP_LOW	RW	0x1

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Table 3-999. Register Call Summary for Register CM_DIV_H12_DPLL_IVA

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-1000. CM_SSC_DELTAMSTEP_DPLL_IVA

Address Offset	0x0000 00C8		
Physical Address	0x4A00 41C8	**Instance**	CKGEN_CM_CORE_AON
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELTAMSTEP																							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-1001. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_IVA

Clock Management Functional Description • Spread Spectrum Clocking: [0]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [1]

Table 3-1002. CM_SSC_MODFREQDIV_DPLL_IVA

Address Offset	0x0000 00CC		
Physical Address	0x4A00 41CC	**Instance**	CKGEN_CM_CORE_AON
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						MODFREQDIV_EXPONENT		RESERVED	MODFREQDIV_MANTISSA						

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-1003. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_IVA

Clock Management Functional Description
- Spread Spectrum Clocking: [0] [1]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-1004. CM_BYPCLK_DPLL_IVA

Address Offset	0x0000 00DC		
Physical Address	0x4A00 41DC	**Instance**	CKGEN_CM_CORE_AON
Description	Control IVA PLL BYPASS clock. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CLKSEL	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	CLKSEL	Select the DPLL IVA bypass clock 0x0: DPLL_IVA bypass clock is CORE_X2_CLK divided by 1, to be used for both OPP_NOM and OPP_LOW 0x1: DPLL_IVA bypass clock is CORE_X2_CLK divided by 2 0x2: DPLL_IVA bypass clock is CORE_X2_CLK divided by 4 0x3: DPLL_IVA bypass clock is CORE_X2_CLK divided by 8	RW	0x0

Table 3-1005. Register Call Summary for Register CM_BYPCLK_DPLL_IVA

Clock Management Functional Description
- CM_CORE_AON Clock Generator: [0]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [1]

Table 3-1006. CM_CLKMODE_DPLL_ABE

Address Offset	0x0000 00E0		
Physical Address	0x4A00 41E0	**Instance**	CKGEN_CM_CORE_AON
Description	This register allows controlling the DPLL modes.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED					DPLL_EN		

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. 0x0: REGM4XEN mode of the DPLL is disabled 0x1: REGM4XEN mode of the DPLL is enabled	RW	0
10	DPLL_LPMODE_EN	Set the DPLL in Low Power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low power mode of the DPLL is disabled 0x1: Low power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00
2:0	DPLL_EN	DPLL control 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: Put the DPLL in Idle Bypass Low Power mode. 0x6: Put the DPLL in Idle Bypass Fast Relock mode. 0x7: Enables the DPLL in Lock mode	RW	0x5

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Table 3-1007. Register Call Summary for Register CM_CLKMODE_DPLL_ABE

Clock Management Functional Description
- DPLLs Output Clocks Parameters: [0]
- Synthesized Clock Parameters: [1]
- Power Modes: [2] [3]
- Recalibration: [4]
- Spread Spectrum Clocking: [7] [8] [9]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [10]

Table 3-1008. CM_IDLEST_DPLL_ABE

Address Offset	0x0000 00E4		
Physical Address	0x4A00 41E4	**Instance**	CKGEN_CM_CORE_AON
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											ST_DPLL_INIT	ST_DPLL_MODE			ST_DPLL_CLK

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000000
4	ST_DPLL_INIT	DPLL init status (for debug purpose) Read 0x0: DPLL is not init Read 0x1: DPLL has been init	R	0
3:1	ST_DPLL_MODE	DPLL mode status (for debug purpose) Read 0x0: Transient state. From reset to any LP (low power) idle state or from any power state to any power state (Power states are Low Power Stop mode, Fast Relock Stop mode, Idle Bypass Low Power mode and Idle Bypass Fast Relock mode). Read 0x1: The DPLL is in Low Power Stop mode Read 0x2: The DPLL is in Fast Relock Stop mode Read 0x3: reserved Read 0x4: reserved Read 0x5: The DPLL is in Idle Bypass Low Power mode Read 0x6: The DPLL is in Idle Bypass Fast Relock mode Read 0x7: reserved	R	0
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-1009. Register Call Summary for Register CM_IDLEST_DPLL_ABE

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [0]

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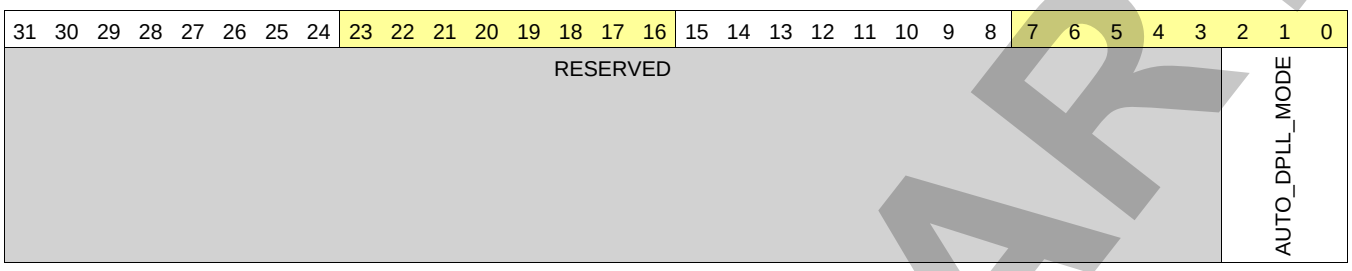
Table 3-1010. CM_AUTOIDLE_DPLL_ABE

Address Offset	0x0000 00E8		
Physical Address	0x4A00 41E8	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides automatic control over the DPLL activity.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in Low Power Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in Fast Relock Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in Idle Bypass Low Power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in Idle Bypass Fast Relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

Table 3-1011. Register Call Summary for Register CM_AUTOIDLE_DPLL_ABE

Clock Management Functional Description • Power Modes: [0]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [1]

Table 3-1012. CM_CLKSEL_DPLL_ABE

Address Offset	0x0000 00EC		
Physical Address	0x4A00 41EC	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the DPLL.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	DCC_EN	RESERVED						DPLL_MULT								RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Only CLKINPULOW bypass clock supported for this PLL	R	1
22	DCC_EN	Duty-cycle corrector for high frequency clock Read 0: Duty-cycle corrector is disabled	R	0
21:19	RESERVED		R	0x0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). Equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M [warm reset insensitive] 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) Equal to input N of DPLL, actual division factor is N+1. [warm reset insensitive]	RW	0x00

Table 3-1013. Register Call Summary for Register CM_CLKSEL_DPLL_ABE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-1014. CM_DIV_M2_DPLL_ABE

Address Offset	0x0000 00F0		
Physical Address	0x4A00 41F0	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				CLKX2ST	RESERVED	CLKST	RESERVED					DIVHS			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	CLKX2ST	DPLL CLKOUTX2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
10	RESERVED		R	0
9	CLKST	DPLL CLKOUT status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0

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Bits	Field Name	Description	Type	Reset
8:5	RESERVED		R	0x0
4:0	DIVHS	DPLL M2 post-divider factor (1 to 31). 0x0: Reserved 0x1: 1, to be used for both OPP_NOM and OPP_LOW	RW	0x01

Table 3-1015. Register Call Summary for Register CM_DIV_M2_DPLL_ABE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-1016. CM_DIV_M3_DPLL_ABE

Address Offset	0x0000 00F4		
Physical Address	0x4A00 41F4	**Instance**	CKGEN_CM_CORE_AON
Description	This register provides controls over the M3 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED						DIVHS		

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	CLKST	DPLL CLKOUTHIF status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:5	RESERVED		R	0x0
4:0	DIVHS	DPLL M3 post-divider factor (1 to 31). 0x0: Reserved 0x1: 1, to be used for both OPP_NOM and OPP_LOW	RW	0x01

Table 3-1017. Register Call Summary for Register CM_DIV_M3_DPLL_ABE

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-1018. CM_SSC_DELTAMSTEP_DPLL_ABE

Address Offset	0x0000 0108		
Physical Address	0x4A00 4208	**Instance**	CKGEN_CM_CORE_AON
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DELTAMSTEP															

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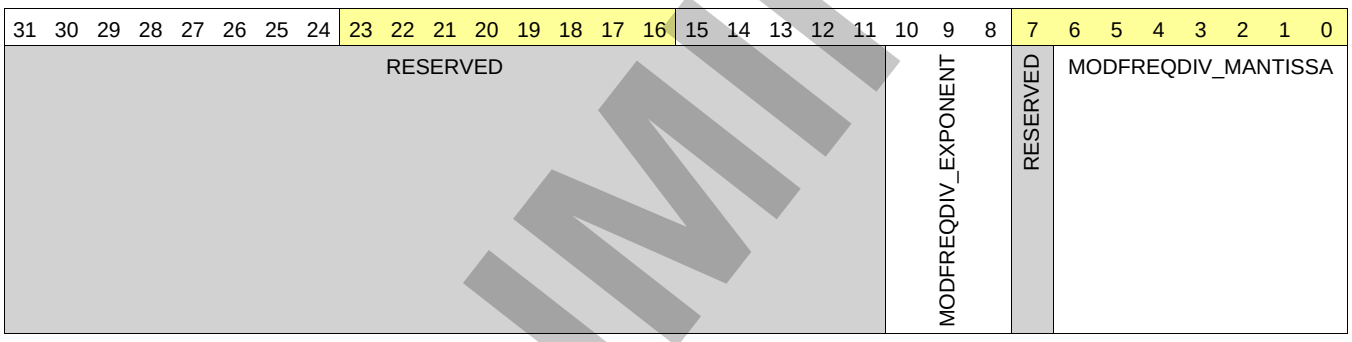
Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-1019. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_ABE

Clock Management Functional Description • Spread Spectrum Clocking: [0]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [1]

Table 3-1020. CM_SSC_MODFREQDIV_DPLL_ABE

Address Offset	0x0000 010C		
Physical Address	0x4A00 420C	**Instance**	CKGEN_CM_CORE_AON
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-1021. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_ABE

Clock Management Functional Description • Spread Spectrum Clocking: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE_AON Register Summary: [2]

Table 3-1022. CM_SHADOW_FREQ_CONFIG1

Address Offset	0x0000 0160		
Physical Address	0x4A00 4260	**Instance**	CKGEN_CM_CORE_AON
Description	Shadow register to program new DPLL configuration affecting EMIF and GPMC (L3 clock) functional frequency during DVFS. The PRCM HW automatically applies the new configuration after EMIF/GPMC have been put in idle state.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_CORE_M2_DIV					DPLL_CORE_DPLL_EN			RESERVED				DLL_RESET	DLL_OVERRIDE	RESERVED	FREQ_UPDATE

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x000
15:11	DPLL_CORE_M2_DIV	Shadow register for CM_DIV_M2_DPLL_CORE[4:0] DIVHS. The main register is automatically loaded with the shadow register value after EMIF IDLE if the FREQ_UPDATE field is set to '1'. Divide value from 1 to 31. 0x0: Reserved	RW	0x01
10:8	DPLL_CORE_DPLL_EN	Shadow register for CM_CLKMODE_DPLL_CORE[2:0] DPLL_EN. The main register is automatically loaded with the shadow register value after EMIF IDLE if the FREQ_UPDATE field is set to '1'. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: Put the DPLL in Idle Bypass Low Power mode. 0x6: Put the DPLL in Idle Bypass Fast Relock mode. 0x7: Enables the DPLL in Lock mode	RW	0x5
7:4	RESERVED		R	0x0
3	DLL_RESET	Specify if DLL should be reset or not during the frequency change hardware sequence. 0x0: DLL is not reset during the frequency change hardware sequence 0x1: DLL is reset automatically during the frequency change hardware sequence	RW	1
2	DLL_OVERRIDE	Shadow register for CM_DLL_CTRL[0] DLL_OVERRIDE. The main register is automatically loaded with the shadow register value after EMIF IDLE if the FREQ_UPDATE field is set to '1'. 0x0: Lock and code outputs are not overriden 0x1: Lock output is overriden to '1' and code output is overriden with a value coming from control module.	RW	1
1	RESERVED		RW	0
0	FREQ_UPDATE	Writing '1' indicates that a new configuration is available. It is automatically cleared by HW after the configuration has been applied.	RW WSpecial	0

Table 3-1023. Register Call Summary for Register CM_SHADOW_FREQ_CONFIG1

Clock Management Functional Description
- DPLLs Cascading: [0] [1]

PRCM Register Manual
- CKGEN_CM_CORE_AON Register Summary: [2]
- CKGEN_CM_CORE_AON Register Description: [3] [4]

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Table 3-1024. CM_SHADOW_FREQ_CONFIG2

Address Offset	0x0000 0164		
Physical Address	0x4A00 4264	**Instance**	CKGEN_CM_CORE_AON
Description	Shadow register to program new DPLL configuration affecting GPMC (L3 clock) functional frequency during DVFS. The PRCM HW automatically applies the new configuration after EMIF/GPMC have been put in idle state.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DPLL_CORE_H12_DIV						CLKSEL_L3	GPMC_FREQ_UPDATE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:2	DPLL_CORE_H12_DIV	Shadow register for CM_DIV_H12_DPLL_CORE[5:0] DIVHS. The main register is automatically loaded with the shadow register value after GPMC IDLE if the CM_SHADOW_FREQ_CONFIG1[0] FREQ_UPDATE field is set to '1' and GPMC_FREQ_UPDATE is set to '1'. Divide value from 1 to 31. 0x0: Reserved	RW	0x1
1	CLKSEL_L3	Shadow register for CM_CLKSEL_CORE[4] CLKSEL_L3. The main register is automatically loaded with the shadow register value after GPMC IDLE if the CM_SHADOW_FREQ_CONFIG1[0] FREQ_UPDATE field is set to '1' and GPMC_FREQ_UPDATE is set to '1'. 0x0: L3_CLK is CORE_CLK divided by 1 0x1: L3_CLK is CORE_CLK divided by 2	RW	0
0	GPMC_FREQ_UPDATE	Controls whether or not GPMC has to be put automatically into idle during the frequency change operation. 0x0: GPMC is not put automatically into idle during frequency change operation. 0x1: GPMC is put automatically into idle during frequency change operation.	RW	0

Table 3-1025. Register Call Summary for Register CM_SHADOW_FREQ_CONFIG2

Voltage-Management Functional Description

- GPMC Clock Frequency Scaling Constraints: [0]

PRCM Register Manual

- CKGEN_CM_CORE_AON Register Summary: [1]

Table 3-1026. CM_DYN_DEP_PRESCAL

Address Offset	0x0000 0170		
Physical Address	0x4A00 4270	**Instance**	CKGEN_CM_CORE_AON
Description	Control the time unit of the sliding window for dynamic dependencies (auto-sleep feature).		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRESCAL							

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:0	PRESCAL	Time unit is equal to (PRESCAL + 1) L4 clock cycles.	RW	0x20

Table 3-1027. Register Call Summary for Register CM_DYN_DEP_PRESCAL

Device Power Management Introduction
- Clock Domain Dependency: [0]

PRCM Register Manual
- EMU_CM Register Description: [1]
- CKGEN_CM_CORE_AON Register Summary: [2]
- MPU_CM_CORE_AON Register Description: [3]
- DSP_CM_CORE_AON Register Description: [4]
- CORE_CM_CORE Register Description: [5] [6] [7] [9] [10]

3.11.24 MPU_CM_CORE_AON Registers

3.11.24.1 MPU_CM_CORE_AON Register Summary

Table 3-1028. MPU_CM_CORE_AON Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MPU_CM_CORE_AON Base Address
CM_MPU_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 4300
CM_MPU_STATICDEP	RW	32	0x0000 0004	0x4A00 4304
CM_MPU_DYNAMICDEP	RW	32	0x0000 0008	0x4A00 4308
CM_MPU_MPU_CLKCTRL	RW	32	0x0000 0020	0x4A00 4320
CM_MPU_MPU_MPU_DBG_CLKCTRL	R	32	0x0000 0028	0x4A00 4328

3.11.24.2 MPU_CM_CORE_AON Register Description

Table 3-1029. CM_MPU_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 4300	**Instance**	MPU_CM_CORE_AON
Description	This register enables the MPU domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_MPU_GCLK	RESERVED						CLKTRCTRL	

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_MPU_GCLK	This field indicates the state of the MPU_GCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the MPU clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1030. Register Call Summary for Register CM_MPU_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1]
PRCM Register Manual • MPU_CM_CORE_AON Register Summary: [2]

Table 3-1031. CM_MPU_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 4304	**Instance**	MPU_CM_CORE_AON
Description	This register controls the static domain dependencies from MPU domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														CUSTEFUSE_STATDEP	COREAON_STATDEP	WKUPAON_STATDEP	L4SEC_STATDEP	L4PER_STATDEP	L4CFG_STATDEP	SDMA_STATDEP	GPU_STATDEP	CAM_STATDEP	DSS_STATDEP	L3INIT_STATDEP	L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	ABE_STATDEP	IVA_STATDEP	DSP_STATDEP	IPU_STATDEP

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	CUSTEFUSE_STATDEP	Static dependency towards CUSTEFUSE clock domain Read 0x0: Dependency is disabled	R	0
16	COREAON_STATDEP	Static dependency towards COREAON clock domain Read 0x0: Dependency is disabled	R	0
15	WKUPAON_STATDEP	Static dependency towards WKUPAON clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
14	L4SEC_STATDEP	Static dependency towards L4SEC clock domain 0: Dependency is disabled 1: Dependency is enabled	RW	0
13	L4PER_STATDEP	Static dependency towards L4_PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
12	L4CFG_STATDEP	Static dependency towards L4_CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
11	SDMA_STATDEP	Static dependency towards DMA_SYSTEM clock domain Read 0x0: Dependency is disabled	R	0
10	GPU_STATDEP	Static dependency towards GPU clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
9	CAM_STATDEP	Static dependency towards CAM clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_STATDEP	Static dependency towards DSS clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
6	L3MAIN2_STATDEP	Static dependency towards L3_MAIN2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5	L3MAIN1_STATDEP	Static dependency towards L3_MAIN1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVA_STATDEP	Static dependency towards IVA clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	DSP_STATDEP	Static dependency towards DSP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	IPU_STATDEP	Static dependency towards IPU clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-1032. Register Call Summary for Register CM_MPU_STATICDEP

Clock Management Functional Description • Static Dependency: [0] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
PRCM Register Manual • MPU_CM_CORE_AON Register Summary: [19]

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Table 3-1033. CM_MPU_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 4308	**Instance**	MPU_CM_CORE_AON
Description	This register controls the dynamic domain depedencies from MPU domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED																		L3MAIN1_DYNDEP		EMIF_DYNDEP		ABE_DYNDEP		RESERVED	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:6	RESERVED		R	0x00000
5	L3MAIN1_DYNDEP	Dynamic dependency towards L3_MAIN1 clock domain Read 0x1: Dependency is enabled	R	1
4	EMIF_DYNDEP	Dynamic dependency towards EMIF clock domain Read 0x1: Dependency is enabled	R	1
3	ABE_DYNDEP	Dynamic dependency towards ABE clock domain Read 0x1: Dependency is enabled	R	1
2:0	RESERVED		R	0x0

Table 3-1034. Register Call Summary for Register CM_MPU_DYNAMICDEP

Clock Management Functional Description
- Dynamic Dependency: [0] [1] [2]

PRCM Register Manual
- MPU_CM_CORE_AON Register Summary: [3]

Table 3-1035. CM_MPU_MPU_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 4320	**Instance**	MPU_CM_CORE_AON
Description	This register manages the MPU clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					CLKSEL_ABE_DIV_MODE	CLKSEL_EMIF_DIV_MODE		RESERVED					STBYST	IDLEST		RESERVED																MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x0000
26	CLKSEL_ABE_DIV_MODE	Selects the ratio for MPU - ABE Subsystem bridge versus MPU DPLL clock 0x0: MPU DPLL clock divided by 8 0x1: MPU DPLL clock divided by 16	RW	0x0
25:24	CLKSEL_EMIF_DIV_MODE	Selects the ratio for MPU - L3_MAIN interconnect bridge versus MPU DPLL clock. 0x0: MPU DPLL clock divided by 4 0x1: MPU DPLL clock divided by 4 0x2: MPU DPLL clock divided by 8 0x3: MPU DPLL clock divided by 8	RW	0x0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1036. Register Call Summary for Register CM_MPU_MPU_CLKCTRL

Clock Management Functional Description • PRM Clock Source: [0] [1] • Clock Domain Module Attributes: [2] [3] [4]
PRCM Register Manual • MPU_CM_CORE_AON Register Summary: [5]

Table 3-1037. CM_MPU_MPU_MPU_DBG_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 4328	**Instance**	MPU_CM_CORE_AON
Description	This register manages the MPU_MPU_DBG clocks. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1038. Register Call Summary for Register CM_MPU_MPU_MPU_DBG_CLKCTRL

PRCM Register Manual
- MPU_CM_CORE_AON Register Summary: [0]

3.11.25 DSP_CM_CORE_AON Registers

3.11.25.1 DSP_CM_CORE_AON Register Summary

Table 3-1039. DSP_CM_CORE_AON Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSP_CM_CORE_AON Base Address
CM_DSP_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 4400
CM_DSP_STATICDEP	RW	32	0x0000 0004	0x4A00 4404
CM_DSP_DYNAMICDEP	RW	32	0x0000 0008	0x4A00 4408
CM_DSP_DSP_CLKCTRL	RW	32	0x0000 0020	0x4A00 4420

3.11.25.2 DSP_CM_CORE_AON Register Description

Table 3-1040. CM_DSP_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 4400	**Instance**	DSP_CM_CORE_AON
Description	This register enables the DSP domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

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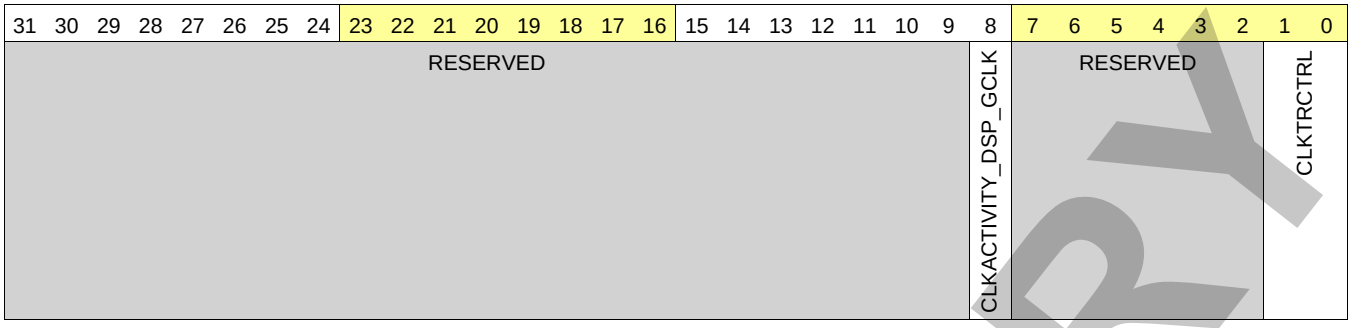

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_DSP_GCLK	This field indicates the state of the DSP_GCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the DSP clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1041. Register Call Summary for Register CM_DSP_CLKSTCTRL

Reset Management Functional Description • DSP Subsystem Power-On Reset Sequence: [0]
Clock Management Functional Description • Clock Domain Modes: [1] [2]
PRCM Register Manual • DSP_CM_CORE_AON Register Summary: [3] • DSP_CM_CORE_AON Register Description: [4]

Table 3-1042. CM_DSP_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 4404	**Instance**	DSP_CM_CORE_AON
Description	This register controls the static domain depedencies from DSP domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														CUSTEFUSE_STATDEP	COREAON_STATDEP	WKUPAON_STATDEP	RESERVED	L4PER_STATDEP	L4CFG_STATDEP	RESERVED		CAM_STATDEP	RESERVED	L3INIT_STATDEP	L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	ABE_STATDEP	IVA_STATDEP	RESERVED	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17	CUSTEFUSE_STATDEP	Static dependency towards CUSTEFUSE clock domain Read 0x0: Dependency is disabled	R	0
16	COREAON_STATDEP	Static dependency towards COREAON clock domain Read 0x0: Dependency is disabled	R	0
15	WKUPAON_STATDEP	Static dependency towards WKUPAON clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
14	RESERVED	Reserved	R	0
13	L4PER_STATDEP	Static dependency towards L4_PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	L4CFG_STATDEP	Static dependency towards L4_CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
11:10	RESERVED	Reserved	R	0x0
9	CAM_STATDEP	Static dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	RESERVED	Reserved	R	0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	L3MAIN2_STATDEP	Static dependency towards L3_MAIN2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5	L3MAIN1_STATDEP	Static dependency towards L3_MAIN1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVA_STATDEP	Static dependency towards IVA clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED	Reserved	R	0x0

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Table 3-1043. Register Call Summary for Register CM_DSP_STATICDEP

Clock Management Functional Description
- Static Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]

PRCM Register Manual
- DSP_CM_CORE_AON Register Summary: [12]

Table 3-1044. CM_DSP_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 4408	**Instance**	DSP_CM_CORE_AON
Description	This register controls the dynamic domain depedencies from DSP domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED																		L3MAIN1_DYNDEP	RESERVED	ABE_DYNDEP	IVA_DYNDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:6	RESERVED	Reserved	R	0x00000
5	L3MAIN1_DYNDEP	Dynamic dependency towards L3_MAIN1 clock domain Read 0x1: Dependency is enabled	R	1
4	RESERVED	Reserved	R	0
3	ABE_DYNDEP	Dynamic dependency towards ABE clock domain Read 0x1: Dependency is enabled	R	1
2	IVA_DYNDEP	Dynamic dependency towards IVA clock domain Read 0x1: Dependency is enabled	R	1
1:0	RESERVED	Reserved	R	0x0

Table 3-1045. Register Call Summary for Register CM_DSP_DYNAMICDEP

Clock Management Functional Description
- Dynamic Dependency: [0] [1] [2]

PRCM Register Manual
- DSP_CM_CORE_AON Register Summary: [3]

Table 3-1046. CM_DSP_DSP_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 4420	**Instance**	DSP_CM_CORE_AON
Description	This register manages the DSP clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Reserved	R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_DSP_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1047. Register Call Summary for Register CM_DSP_DSP_CLKCTRL

Reset Management Functional Description • DSP Subsystem Power-On Reset Sequence: [0]
Clock Management Functional Description • Clock Domain Module Attributes: [1] [2] [3]
PRCM Register Manual • DSP_CM_CORE_AON Register Summary: [4]

3.11.26 ABE_CM_CORE_AON Registers

3.11.26.1 ABE_CM_CORE_AON Register Summary

Table 3-1048. ABE_CM_CORE_AON Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ABE_CM_CORE_AON Base Address
CM_ABE_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 4500
CM_ABE_L4_ABE_CLKCTRL	R	32	0x0000 0020	0x4A00 4520

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Table 3-1048. ABE_CM_CORE_AON Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ABE_CM_CORE_AON Base Address
CM_ABE_AESS_CLKCTRL	RW	32	0x0000 0028	0x4A00 4528
CM_ABE_MCPDM_CLKCTRL	RW	32	0x0000 0030	0x4A00 4530
CM_ABE_DMIC_CLKCTRL	RW	32	0x0000 0038	0x4A00 4538
CM_ABE_MCASP_CLKCTRL	RW	32	0x0000 0040	0x4A00 4540
CM_ABE_MCBSP1_CLKCTRL	RW	32	0x0000 0048	0x4A00 4548
CM_ABE_MCBSP2_CLKCTRL	RW	32	0x0000 0050	0x4A00 4550
CM_ABE_MCBSP3_CLKCTRL	RW	32	0x0000 0058	0x4A00 4558
RESERVED	R	32	0x0000 0060	0x4A00 4560
CM_ABE_TIMER5_CLKCTRL	RW	32	0x0000 0068	0x4A00 4568
CM_ABE_TIMER6_CLKCTRL	RW	32	0x0000 0070	0x4A00 4570
CM_ABE_TIMER7_CLKCTRL	RW	32	0x0000 0078	0x4A00 4578
CM_ABE_TIMER8_CLKCTRL	RW	32	0x0000 0080	0x4A00 4580
CM_ABE_WD_TIMER3_CLKCTRL	RW	32	0x0000 0088	0x4A00 4588

3.11.26.2 ABE_CM_CORE_AON Register Description

Table 3-1049. CM_ABE_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 4500	**Instance**	ABE_CM_CORE_AON
Description	This register enables the ABE domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLKACTIVITY_PAD_SLIMBUS1_CLK	CLKACTIVITY_PAD_CLKS	CLKACTIVITY_ABE_24M_GFCLK	CLKACTIVITY_ABE_32K_CLK	CLKACTIVITY_ABE_SYS_CLK	CLKACTIVITY_FUNC_24M_GFCLK	CLKACTIVITY_ABE_GICLK	CLKACTIVITY_ABE_X2_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x00000
15	CLKACTIVITY_PAD_SLIMBUS1_CLK	This field indicates the state of the SLIMBUS_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0

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Bits	Field Name	Description	Type	Reset
14	CLKACTIVITY_PAD_CLKS	This field indicates the state of the PAD_CLKS clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
13	CLKACTIVITY_ABE_24M_GFCLK	This field indicates the state of the ABE_24M_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
12	CLKACTIVITY_ABE_32K_CLK	This field indicates the state of the ABE_32K_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
11	CLKACTIVITY_ABE_SYS_CLK	This field indicates the state of the ABE_SYS_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
10	CLKACTIVITY_FUNC_24M_GFCLK	This field indicates the state of the FUNC_24M_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
9	CLKACTIVITY_ABE_GICLK	This field indicates the state of the ABE_GICLK interface clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
8	CLKACTIVITY_DPLL_ABE_X2_CLK	This field indicates the state of the DPLL_ABE_X2_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED	Reserved	R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the ABE clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1050. Register Call Summary for Register CM_ABE_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] [4] [5] [6]
PRCM Register Manual • ABE_CM_CORE_AON Register Summary: [7] • ABE_CM_CORE_AON Register Description: [8]

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Table 3-1051. CM_ABE_L4_ABE_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 4520	**Instance**	ABE_CM_CORE_AON
Description	This register manages the L4ABE clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_ABE_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1052. Register Call Summary for Register CM_ABE_L4_ABE_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- ABE_CM_CORE_AON Register Summary: [2]

Table 3-1053. CM_ABE_AESS_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 4528	**Instance**	ABE_CM_CORE_AON
Description	This register manages the AESS clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL_AESS_FCLK	RESERVED					STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL_AESS_FCLK	Selects the ratio of AESS_FCLK to ABE_CLK 0x0: AESS_FCLK is divide by 1 of ABE_CLK 0x1: AESS_FCLK is divide by 2 of ABE_CLK	RW	0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1054. Register Call Summary for Register CM_ABE_AESS_CLKCTRL

Clock Management Functional Description
- CKGEN_ABE Clock Generator: [0] [1]
- Clock Domain Modes: [2]
- Clock Domain Module Attributes: [3] [4] [5]

PRCM Register Manual
- ABE_CM_CORE_AON Register Summary: [6]

Table 3-1055. CM_ABE_MCPDM_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4A00 4530	**Instance**	ABE_CM_CORE_AON
Description	This register manages the McPDM clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1056. Register Call Summary for Register CM_ABE_MCPDM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • ABE_CM_CORE_AON Register Summary: [2]

Table 3-1057. CM_ABE_DMIC_CLKCTRL

Address Offset	0x0000 0038		
Physical Address	0x4A00 4538	**Instance**	ABE_CM_CORE_AON
Description	This register manages the DMIC clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKSEL_INTERNAL_SOURCE		CLKSEL_SOURCE		RESERVED						IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYS_CLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SLIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1058. Register Call Summary for Register CM_ABE_DMIC_CLKCTRL

Clock Management Functional Description
- CKGEN_ABE Clock Generator: [0] [1]
- Clock Domain Module Attributes: [2] [3]

PRCM Register Manual
- ABE_CM_CORE_AON Register Summary: [4]

Table 3-1059. CM_ABE_MCASP_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A00 4540	**Instance**	ABE_CM_CORE_AON
Description	This register manages the MCASP clocks.		
Type	RW		

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31 30 29 28	27 26	25 24	23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2	1 0
RESERVED	CLKSEL_INTERNAL_SOURCE	CLKSEL_SOURCE	RESERVED	IDLEST	RESERVED		MODULEMODE

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYS_CLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1060. Register Call Summary for Register CM_ABE_MCASP_CLKCTRL

Clock Management Functional Description
- CKGEN_ABE Clock Generator: [0] [1]
- Clock Domain Module Attributes: [2] [3]

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Table 3-1060. Register Call Summary for Register CM_ABE_MCASP_CLKCTRL (continued)

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- ABE_CM_CORE_AON Register Summary: [4]

Table 3-1061. CM_ABE_MCBSP1_CLKCTRL

Address Offset	0x0000 0048		
Physical Address	0x4A00 4548	**Instance**	ABE_CM_CORE_AON
Description	This register manages the MCBSP1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKSEL_INTERNAL_SOURCE		CLKSEL_SOURCE		RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYS_CLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1062. Register Call Summary for Register CM_ABE_MCBSP1_CLKCTRL

Clock Management Functional Description • CKGEN_ABE Clock Generator: [0] [1] • Clock Domain Module Attributes: [2] [3]
PRCM Register Manual • ABE_CM_CORE_AON Register Summary: [4]

Table 3-1063. CM_ABE_MCBSP2_CLKCTRL

Address Offset	0x0000 0050		
Physical Address	0x4A00 4550	**Instance**	ABE_CM_CORE_AON
Description	This register manages the MCBSP2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CLKSEL_INTERNAL_SOURCE		CLKSEL_SOURCE		RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYS_CLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1064. Register Call Summary for Register CM_ABE_MCBSP2_CLKCTRL

Clock Management Functional Description
- CKGEN_ABE Clock Generator: [0] [1]
- Clock Domain Module Attributes: [2] [3]

PRCM Register Manual
- ABE_CM_CORE_AON Register Summary: [4]

Table 3-1065. CM_ABE_MCBSP3_CLKCTRL

Address Offset	0x0000 0058		
Physical Address	0x4A00 4558	**Instance**	ABE_CM_CORE_AON
Description	This register manages the MCBSP3 clocks.		
Type	RW		

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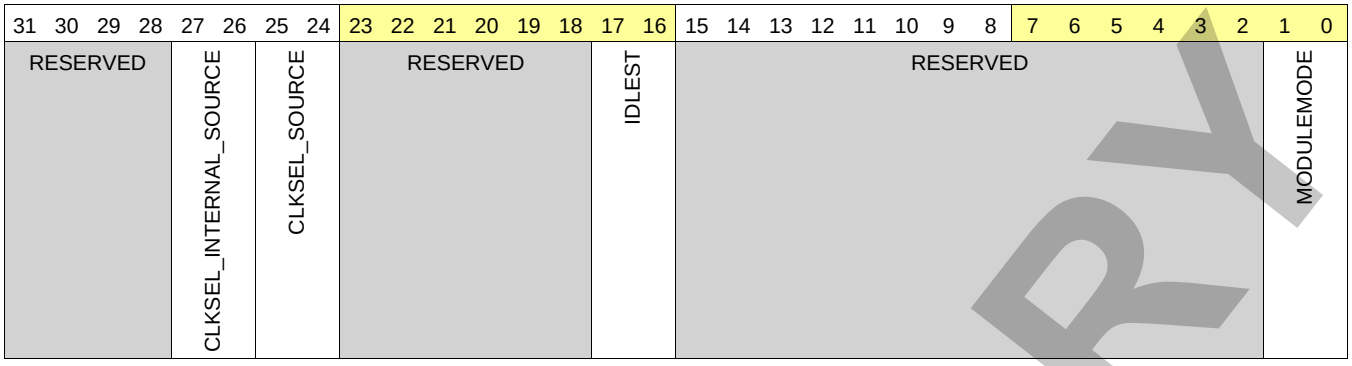

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	CLKSEL_INTERNAL_SOURCE	Selects the internal clock to be used as the functional clock in case CLKSEL_SOURCE selects the internal clock source as the functional clock source. 0x0: 24MHz clock derived from DPLL_ABE is selected 0x1: ABE_SYS_CLK is selected 0x2: 24MHz clock derived from DPLL_PER is selected 0x3: Reserved	RW	0x0
25:24	CLKSEL_SOURCE	Selects the source of the functional clock between, internal source, CLKS pad and Audio SLIMBUS_CLK pad. The switching between the clocks is not guaranteed to be glitchless. 0x0: Functional clock is sourced from an internal clock 0x1: Functional clock is sourced from CLKS pad 0x2: Functional clock is sourced from Audio SLIMBUS pad 0x3: Reserved	RW	0x0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1066. Register Call Summary for Register CM_ABE_MCBSP3_CLKCTRL

Clock Management Functional Description
- CKGEN_ABE Clock Generator: [0] [1]
- Clock Domain Module Attributes: [2] [3]

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Table 3-1066. Register Call Summary for Register CM_ABE_MCBSP3_CLKCTRL (continued)

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- ABE_CM_CORE_AON Register Summary: [4]

Table 3-1067. CM_ABE_TIMER5_CLKCTRL

Address Offset	0x0000 0068		
Physical Address	0x4A00 4568	**Instance**	ABE_CM_CORE_AON
Description	This register manages the TIMER5 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED															MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects between ABE_SYS_CLK and ABE_32K_CLK as the timer functional clock 0x0: Selects ABE_SYS_CLK as the functional clock 0x1: Selects ABE_32K_CLK as the functional clock	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1068. Register Call Summary for Register CM_ABE_TIMER5_CLKCTRL

Clock Management Functional Description

- CKGEN_ABE Clock Generator: [0]
- Clock Domain Module Attributes: [1] [2]

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- ABE_CM_CORE_AON Register Summary: [3]

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Table 3-1069. CM_ABE_TIMER6_CLKCTRL

Address Offset	0x0000 0070		
Physical Address	0x4A00 4570	**Instance**	ABE_CM_CORE_AON
Description	This register manages the TIMER6 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects between ABE_SYS_CLK and ABE_32K_CLK as the timer functional clock 0x0: Selects ABE_SYS_CLK as the functional clock 0x1: Selects ABE_32K_CLK as the functional clock	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1070. Register Call Summary for Register CM_ABE_TIMER6_CLKCTRL

Clock Management Functional Description
- CKGEN_ABE Clock Generator: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- ABE_CM_CORE_AON Register Summary: [3]

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Table 3-1071. CM_ABE_TIMER7_CLKCTRL

Address Offset	0x0000 0078		
Physical Address	0x4A00 4578	**Instance**	ABE_CM_CORE_AON
Description	This register manages the TIMER7 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects between ABE_SYS_CLK and ABE_32K_CLK as the timer functional clock 0x0: Selects ABE_SYS_CLK as the functional clock 0x1: Selects ABE_32K_CLK as the functional clock	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1072. Register Call Summary for Register CM_ABE_TIMER7_CLKCTRL

Clock Management Functional Description
- CKGEN_ABE Clock Generator: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- ABE_CM_CORE_AON Register Summary: [3]

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Table 3-1073. CM_ABE_TIMER8_CLKCTRL

Address Offset	0x0000 0080		
Physical Address	0x4A00 4580	**Instance**	ABE_CM_CORE_AON
Description	This register manages the TIMER8 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects between ABE_SYS_CLK and ABE_32K_CLK as the timer functional clock 0x0: Selects ABE_SYS_CLK as the functional clock 0x1: Selects ABE_32K_CLK as the functional clock	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1074. Register Call Summary for Register CM_ABE_TIMER8_CLKCTRL

Clock Management Functional Description
- CKGEN_ABE Clock Generator: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- ABE_CM_CORE_AON Register Summary: [3]

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Table 3-1075. CM_ABE_WD_TIMER3_CLKCTRL

Address Offset	0x0000 0088		
Physical Address	0x4A00 4588	**Instance**	ABE_CM_CORE_AON
Description	This register manages the WD_TIMER3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1076. Register Call Summary for Register CM_ABE_WD_TIMER3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • ABE_CM_CORE_AON Register Summary: [2]

3.11.27 INSTR_CM_CORE_AON Registers

3.11.27.1 INSTR_CM_CORE_AON Register Summary

Table 3-1077. INSTR_CM_CORE_AON Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INSTR_CM_CORE_AON Base Address
CMI_IDENTICATION_AON	R	32	0x0000 0000	0x4A00 4F00
CMI_SYS_CONFIG_AON	RW	32	0x0000 0010	0x4A00 4F10

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Table 3-1077. INSTR_CM_CORE_AON Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	INSTR_CM_CORE_AON Base Address
CMI_STATUS_AON	R	32	0x0000 0014	0x4A00 4F14
CMI_CONFIGURATION_AON	RW	32	0x0000 0024	0x4A00 4F24
CMI_CLASS_FILTERING_AON	RW	32	0x0000 0028	0x4A00 4F28
CMI_TRIGGERING_AON	RW	32	0x0000 002C	0x4A00 4F2C
CMI_SAMPLING_AON	RW	32	0x0000 0030	0x4A00 4F30

3.11.27.2 INSTR_CM_CORE_AON Register Description

Table 3-1078. CMI_IDENTICATION_AON

Address Offset	0x0000 0000		
Physical Address	0x4A00 4F00	**Instance**	INSTR_CM_CORE_AON
Description	CM profiling identification register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	0x-- TI Internal data.

Table 3-1079. Register Call Summary for Register CMI_IDENTICATION_AON

PRCM Register Manual
- INSTR_CM_CORE_AON Register Summary: [0]

Table 3-1080. CMI_SYS_CONFIG_AON

Address Offset	0x0000 0010		
Physical Address	0x4A00 4F10	**Instance**	INSTR_CM_CORE_AON
Description	CM profiling system configuartion register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED				IDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	RESERVED	Reserved	R	0x0
3:2	IDLEMODE	Configuration of the local tartget state management mode	RW	0x2
1	RESERVED	Reserved	R	0
0	SOFTRESET	Software reset	RW	0

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Table 3-1081. Register Call Summary for Register CMI_SYS_CONFIG_AON

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- INSTR_CM_CORE_AON Register Summary: [0]

Table 3-1082. CMI_STATUS_AON

Address Offset	0x0000 0014		
Physical Address	0x4A00 4F14	**Instance**	INSTR_CM_CORE_AON
Description	CM profiling status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FIFOEMPTY	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FIFOEMPTY	CM Profiling buffer empty status 0x0: CM profiling buffer not empty – CM events not yet exported 0x1: CM profiling buffer empty	R	0x1
7:0	RESERVED	Reserved	R	0x00

Table 3-1083. Register Call Summary for Register CMI_STATUS_AON

PRCM Register Manual

- INSTR_CM_CORE_AON Register Summary: [0]

Table 3-1084. CMI_CONFIGURATION_AON

Address Offset	0x0000 0024		
Physical Address	0x4A00 4F24	**Instance**	INSTR_CM_CORE_AON
Description	CM profiling configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAIM_3		CLAIM_2	CLAIM_1	RESERVED				RESERVED	RESERVED							MOD_ACT_EN	RESERVED							EVT_CAPT_EN	RESERVED						

Bits	Field Name	Description	Type	Reset
31:30	CLAIM_3	Ownership	RW	0x0
29	CLAIM_2	Debugger override qualifier	RW	1
28	CLAIM_1	Current owner	R	0
27:24	RESERVED	Reserved	R	0x0
23	RESERVED	Reserved	R	0
22:16	RESERVED	Reserved	R	0x00
15	MOD_ACT_EN	When HIGH the CM Module Activity collection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
14:8	RESERVED	Reserved	R	0x00
7	EVT_CAPT_EN	When HIGH the CM events capture is enabled	RW	0
6:0	RESERVED	Reserved	R	0x00

Table 3-1085. Register Call Summary for Register CMI_CONFIGURATION_AON

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- INSTR_CM_CORE_AON Register Summary: [0]

Table 3-1086. CMI_CLASS_FILTERING_AON

Address Offset	0x0000 0028		
Physical Address	0x4A00 4F28	**Instance**	INSTR_CM_CORE_AON
Description	CM profiling class filtering register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SNAP_CAPT_EN_1F	SNAP_CAPT_EN_1E	SNAP_CAPT_EN_1D	SNAP_CAPT_EN_1C	SNAP_CAPT_EN_1B	SNAP_CAPT_EN_1A	SNAP_CAPT_EN_19	SNAP_CAPT_EN_18	SNAP_CAPT_EN_17	SNAP_CAPT_EN_16	SNAP_CAPT_EN_15	SNAP_CAPT_EN_14	SNAP_CAPT_EN_13	SNAP_CAPT_EN_12	SNAP_CAPT_EN_11	SNAP_CAPT_EN_10	RESERVED												SNAP_CAPT_EN_03	SNAP_CAPT_EN_02	SNAP_CAPT_EN_01	SNAP_CAPT_EN_00

Bits	Field Name	Description	Type	Reset
31	SNAP_CAPT_EN_1F	Snapshot capture enable - Class-ID = 0x1F	RW	0
30	SNAP_CAPT_EN_1E	Snapshot capture enable - Class-ID = 0x1E	RW	0
29	SNAP_CAPT_EN_1D	Snapshot capture enable - Class-ID = 0x1D	RW	0
28	SNAP_CAPT_EN_1C	Snapshot capture enable - Class-ID = 0x1C	RW	0
27	SNAP_CAPT_EN_1B	Snapshot capture enable - Class-ID = 0x1B	RW	0
26	SNAP_CAPT_EN_1A	Snapshot capture enable - Class-ID = 0x1A	RW	0
25	SNAP_CAPT_EN_19	Snapshot capture enable - Class-ID = 0x19	RW	0
24	SNAP_CAPT_EN_18	Snapshot capture enable - Class-ID = 0x18	RW	0
23	SNAP_CAPT_EN_17	Snapshot capture enable - Class-ID = 0x17	RW	0
22	SNAP_CAPT_EN_16	Snapshot capture enable - Class-ID = 0x16	RW	0
21	SNAP_CAPT_EN_15	Snapshot capture enable - Class-ID = 0x15	RW	0
20	SNAP_CAPT_EN_14	Snapshot capture enable - Class-ID = 0x14	RW	0
19	SNAP_CAPT_EN_13	Snapshot capture enable - Class-ID = 0x13	RW	0
18	SNAP_CAPT_EN_12	Snapshot capture enable - Class-ID = 0x12	RW	0
17	SNAP_CAPT_EN_11	Snapshot capture enable - Class-ID = 0x11	RW	0
16	SNAP_CAPT_EN_10	Snapshot capture enable - Class-ID = 0x10	RW	0
15:4	RESERVED		R	0x000
3	SNAP_CAPT_EN_03	Snapshot capture enable - Class-ID = 0x03 [0x23]	RW	0
2	SNAP_CAPT_EN_02	Snapshot capture enable - Class-ID = 0x02 [0x22]	RW	0
1	SNAP_CAPT_EN_01	Snapshot capture enable - Class-ID = 0x01 [0x21]	RW	0
0	SNAP_CAPT_EN_00	Snapshot capture enable - Class-ID = 0x00 [0x20]	RW	0

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Table 3-1087. Register Call Summary for Register CMI_CLASS_FILTERING_AON

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- INSTR_CM_CORE_AON Register Summary: [0]

Table 3-1088. CMI_TRIGGERING_AON

Address Offset	0x0000 002C		
Physical Address	0x4A00 4F2C	**Instance**	INSTR_CM_CORE_AON
Description	CM profiling triggering control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TRIG_STOP_EN	TRIG_START_EN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	TRIG_STOP_EN	Enable stop capturing CM events from external trigger detection	RW	0
0	TRIG_START_EN	Enable start capturing CM events from external trigger detection	RW	0

Table 3-1089. Register Call Summary for Register CMI_TRIGGERING_AON

PRCM Register Manual

- INSTR_CM_CORE_AON Register Summary: [0]

Table 3-1090. CMI_SAMPLING_AON

Address Offset	0x0000 0030		
Physical Address	0x4A00 4F30	**Instance**	INSTR_CM_CORE_AON
Description	CM profiling sampling window register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FCLK_DIV_FACOR				RESERVED								SAMP_WIND_SIZE							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:16	FCLK_DIV_FACOR	FunClk divide factor ranging from 1 to 16	RW	0x0
15:8	RESERVED	Reserved	R	0x00
7:0	SAMP_WIND_SIZE	CM events sampling window size	RW	0x00

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Table 3-1091. Register Call Summary for Register CMI_SAMPLING_AON

PRCM Register Manual

- INSTR_CM_CORE_AON Register Summary: [0]

3.11.28 CM_CORE Instance Summary

Table 3-1092. CM_CORE Instance Summary

Module Name	Base Address	Size
INTRCONN_SOCKET_CM_CORE	0x4A00 8000	256 bytes
CKGEN_CM_CORE	0x4A00 8100	512 bytes
COREAON_CM_CORE	0x4A00 8600	256 bytes
CORE_CM_CORE	0x4A00 8700	2KB
IVA_CM_CORE	0x4A00 9200	256 bytes
CAM_CM_CORE	0x4A00 9300	256 bytes
DSS_CM_CORE	0x4A00 9400	256 bytes
GPU_CM_CORE	0x4A00 9500	256 bytes
L3INIT_CM_CORE	0x4A00 9600	256 bytes
CUSTEFUSE_CM_CORE	0x4A00 9700	256 bytes
RESERVED	0x4A00 9E00	256 bytes
INSTR_CM_CORE	0x4A00 9F00	256 bytes

3.11.29 INTRCONN_SOCKET_CM_CORE Registers

3.11.29.1 INTRCONN_SOCKET_CM_CORE Register Summary

Table 3-1093. INTRCONN_SOCKET_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INTRCONN_SOCKET_CM_CORE Base Address
REVISION_CM_CORE	R	32	0x0000 0000	0x4A00 8000
CM_CM_CORE_PROFILING_CLKCTRL	RW	32	0x0000 0040	0x4A00 8040
CM_CORE_DEBUG_CFG	RW	32	0x0000 0080	0x4A00 8080

3.11.29.2 INTRCONN_SOCKET_CM_CORE Register Description

Table 3-1094. REVISION_CM_CORE

Address Offset	0x0000 0000		
Physical Address	0x4A00 8000	**Instance**	INTRCONN_SOCKET_CM_CORE
Description	This register contains the IP revision code for the CM_CORE part of the PRCM		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

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Bits	Field Name	Description	Type	Reset
31:0	REVISION	Revision Number	R	0x- - TI Internal data.

Table 3-1095. Register Call Summary for Register REVISION_CM_CORE

PRCM Register Manual
- INTRCONN_SOCKET_CM_CORE Register Summary: [0]

Table 3-1096. CM_CM_CORE_PROFILING_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A00 8040	**Instance**	INTRCONN_SOCKET_CM_CORE
Description	This register manages the CM_CORE_PROFILING clock. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:16	IDLEST	Module idle status Read 0x0: Module is fully functional Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle Read 0x3: Module is disabled	R	0x3
15:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. INTRCONN configuration port is not accessible. 0x1: Module is managed automatically by HW along with L3_INSTR domain. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1097. Register Call Summary for Register CM_CM_CORE_PROFILING_CLKCTRL

PRCM Register Manual
- INTRCONN_SOCKET_CM_CORE Register Summary: [0]

Table 3-1098. CM_CORE_DEBUG_CFG

Address Offset	0x0000 0080		
Physical Address	0x4A00 8080	**Instance**	INTRCONN_SOCKET_CM_CORE
Description	This register is used to configure the CM_CORE's 32-bit debug output. There is one 8-bit source select field for selecting from a shared set of 8-bit internal signal blocks per byte. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3								SEL2								SEL1								SEL0							

Bits	Field Name	Description	Type	Reset
31:24	SEL3	Internal signal block select for debug word byte-3	RW	0x03
23:16	SEL2	Internal signal block select for debug word byte-2	RW	0x02
15:8	SEL1	Internal signal block select for debug word byte-1	RW	0x01
7:0	SEL0	Internal signal block select for debug word byte-0	RW	0x00

Table 3-1099. Register Call Summary for Register CM_CORE_DEBUG_CFG

PRCM Register Manual
- INTRCONN_SOCKET_CM_CORE Register Summary: [0]

3.11.30 CKGEN_CM_CORE Registers

3.11.30.1 CKGEN_CM_CORE Register Summary

Table 3-1100. CKGEN_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM_CORE Base Address
CM_CLKSEL_USB_60MHZ	RW	32	0x0000 0004	0x4A00 8104
CM_CLKMODE_DPLL_PER	RW	32	0x0000 0040	0x4A00 8140
CM_IDLEST_DPLL_PER	R	32	0x0000 0044	0x4A00 8144
CM_AUTOIDLE_DPLL_PER	RW	32	0x0000 0048	0x4A00 8148
CM_CLKSEL_DPLL_PER	RW	32	0x0000 004C	0x4A00 814C
CM_DIV_M2_DPLL_PER	RW	32	0x0000 0050	0x4A00 8150
CM_DIV_M3_DPLL_PER	RW	32	0x0000 0054	0x4A00 8154
CM_DIV_H11_DPLL_PER	RW	32	0x0000 0058	0x4A00 8158
CM_DIV_H12_DPLL_PER	RW	32	0x0000 005C	0x4A00 815C
RESERVED	R	32	0x0000 0060	0x4A00 8160
CM_DIV_H14_DPLL_PER	RW	32	0x0000 0064	0x4A00 8164
CM_SSC_DELTAMSTEP_DPLL_PER	RW	32	0x0000 0068	0x4A00 8168
CM_SSC_MODFREQDIV_DPLL_PER	RW	32	0x0000 006C	0x4A00 816C
CM_CLKMODE_DPLL_USB	RW	32	0x0000 0080	0x4A00 8180
CM_IDLEST_DPLL_USB	R	32	0x0000 0084	0x4A00 8184
CM_AUTOIDLE_DPLL_USB	RW	32	0x0000 0088	0x4A00 8188
CM_CLKSEL_DPLL_USB	RW	32	0x0000 008C	0x4A00 818C
CM_DIV_M2_DPLL_USB	RW	32	0x0000 0090	0x4A00 8190
CM_SSC_DELTAMSTEP_DPLL_USB	RW	32	0x0000 00A8	0x4A00 81A8
CM_SSC_MODFREQDIV_DPLL_USB	RW	32	0x0000 00AC	0x4A00 81AC
CM_CLKDCOLDO_DPLL_USB	RW	32	0x0000 00B4	0x4A00 81B4
RESERVED	R	32	0x0000 00C0	0x4A00 81C0
RESERVED	R	32	0x0000 00C4	0x4A00 81C4
RESERVED	R	32	0x0000 00C8	0x4A00 81C8
RESERVED	R	32	0x0000 00CC	0x4A00 81CC
RESERVED	R	32	0x0000 00D0	0x4A00 81D0
RESERVED	R	32	0x0000 00E8	0x4A00 81E8
RESERVED	R	32	0x0000 00EC	0x4A00 81EC
RESERVED	R	32	0x0000 00F4	0x4A00 81F4

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Table 3-1100. CKGEN_CM_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM_CORE Base Address
RESERVED	R	32	0x0000 0100	0x4A00 8200
RESERVED	R	32	0x0000 0104	0x4A00 8204
RESERVED	R	32	0x0000 0108	0x4A00 8208
RESERVED	R	32	0x0000 010C	0x4A00 820C
RESERVED	R	32	0x0000 0110	0x4A00 8210
RESERVED	R	32	0x0000 0128	0x4A00 8228
RESERVED	R	32	0x0000 012C	0x4A00 822C
RESERVED	R	32	0x0000 0134	0x4A00 8234

3.11.30.2 CKGEN_CM_CORE Register Description

Table 3-1101. CM_CLKSEL_USB_60MHZ

Address Offset	0x0000 0004		
Physical Address	0x4A00 8104	**Instance**	CKGEN_CM_CORE
Description	Selects the configuration of the divider generating 60MHz clock for USB from the DPLL_USB o/p.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKSEL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CLKSEL	Select the configuration of the divider 0x0: Set the divider in bypass mode to support bypass clock from DPLL_USB to pass through without division. 0x1: Set the divider to divide the DPLL o/p (480MHz typical) by 8 to generate 60MHz clock, to be used for both OPP_NOM and OPP_LOW.	RW	1

Table 3-1102. Register Call Summary for Register CM_CLKSEL_USB_60MHZ

Clock Management Functional Description
- CKGEN_USB Clock Generator: [0]

PRCM Register Manual
- CKGEN_CM_CORE Register Summary: [1]

Table 3-1103. CM_CLKMODE_DPLL_PER

Address Offset	0x0000 0040		
Physical Address	0x4A00 8140	**Instance**	CKGEN_CM_CORE
Description	This register allows controlling the DPLL modes.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	RESERVED	DPLL_DRIFTGUARD_EN	RESERVED					DPLL_EN		

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Read 0x0: REGM4XEN mode of the DPLL is disabled	R	0
10	DPLL_LPMODE_EN	Set the DPLL in Low Power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low power mode of the DPLL is disabled 0x1: Low power mode of the DPLL is enabled	RW	0
9	RESERVED		RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:3	RESERVED		RW	0x00
2:0	DPLL_EN	DPLL control 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: Put the DPLL in Idle Bypass Low Power mode. 0x6: Put the DPLL in Idle Bypass Fast Relock mode. 0x7: Enables the DPLL in Lock mode	RW	0x5

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Table 3-1104. Register Call Summary for Register CM_CLKMODE_DPLL_PER

Clock Management Functional Description

- Power Modes: [0] [1]
- Recalibration: [2]
- Spread Spectrum Clocking: [5] [6] [7]

PRCM Register Manual

- CKGEN_CM_CORE Register Summary: [8]

Table 3-1105. CM_IDLEST_DPLL_PER

Address Offset	0x0000 0044		
Physical Address	0x4A00 8144	**Instance**	CKGEN_CM_CORE
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											ST_DPLL_INIT	ST_DPLL_MODE			ST_DPLL_CLK

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000000
4	ST_DPLL_INIT	DPLL init status (for debug purpose). Read 0x1: DPLL has been init Read 0x0: DPLL is not init	R	0
3:1	ST_DPLL_MODE	DPLL mode status (for debug purpose) Read 0x0: Transient state. From reset to any LP (low power) idle state or from any power state to any power state (Power states are Low Power Stop mode, Fast Relock Stop mode, Idle Bypass Low Power mode and Idle Bypass Fast Relock mode). Read 0x1: The DPLL is in Low Power Stop mode Read 0x2: The DPLL is in Fast Relock Stop mode Read 0x3: reserved Read 0x4: reserved Read 0x5: The DPLL is in Idle Bypass Low Power mode Read 0x6: The DPLL is in Idle Bypass Fast Relock mode Read 0x7: reserved	R	0
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-1106. Register Call Summary for Register CM_IDLEST_DPLL_PER

PRCM Register Manual

- CKGEN_CM_CORE Register Summary: [0]

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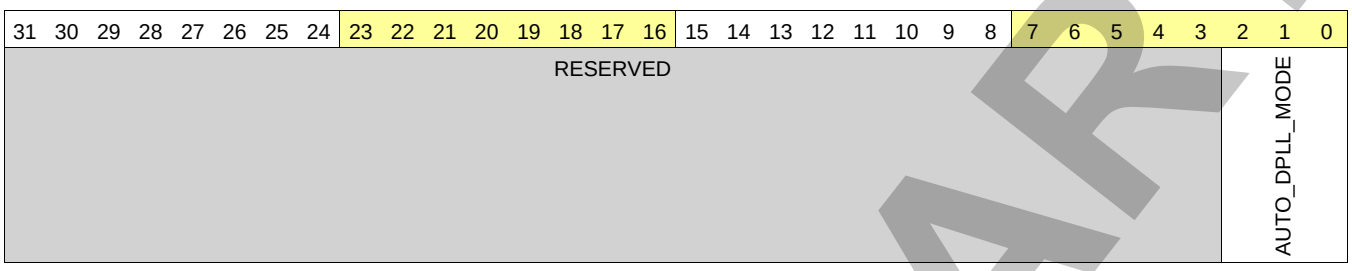
Table 3-1107. CM_AUTOIDLE_DPLL_PER

Address Offset	0x0000 0048		
Physical Address	0x4A00 8148	**Instance**	CKGEN_CM_CORE
Description	This register provides automatic control over the DPLL activity.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in Low Power Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: The DPLL is automatically put in Fast Relock Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in Idle Bypass Low Power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: The DPLL is automatically put in Idle Bypass Fast Relock mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x7: Reserved	RW	0x0

Table 3-1108. Register Call Summary for Register CM_AUTOIDLE_DPLL_PER

Clock Management Functional Description • Power Modes: [0]
PRCM Register Manual • CKGEN_CM_CORE Register Summary: [1]

Table 3-1109. CM_CLKSEL_DPLL_PER

Address Offset	0x0000 004C		
Physical Address	0x4A00 814C	**Instance**	CKGEN_CM_CORE
Description	This register provides controls over the DPLL.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DPLL_BYP_CLKSEL	DCC_EN	RESERVED						DPLL_MULT								RESERVED	DPLL_DIV						

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. Same as ULOWCLKEN on DPLL. In DPLL Locked mode, 0 - No impact 1 - No impact In DPLL Bypass mode, 0 - CLKINP is selected as the BYPASS clock for CLKOUT/CLKOUTX2, 1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT/CLKOUTX2	RW	0
22	DCC_EN	Duty-cycle corrector for high frequency clock Read 0: Duty-cycle corrector is disabled	R	0x0
21:19	RESERVED		R	0x0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). Equal to input M of DPLL; M=2 to 2047 = DPLL multiplies by M. [warm reset insensitive] 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) Equal to input N of DPLL; actual division factor is N+1. [warm reset insensitive]	RW	0x00

Table 3-1110. Register Call Summary for Register CM_CLKSEL_DPLL_PER

Clock Management Functional Description
- Synthesized Clock Parameters: [0] [1]

PRCM Register Manual
- CKGEN_CM_CORE Register Summary: [2]

Table 3-1111. CM_DIV_M2_DPLL_PER

Address Offset	0x0000 0050		
Physical Address	0x4A00 8150	**Instance**	CKGEN_CM_CORE
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				CLKX2ST	RESERVED	CLKST	RESERVED					DIVHS			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	CLKX2ST	DPLL CLKOUTX2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0

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Bits	Field Name	Description	Type	Reset
10	RESERVED		RW	0
9	CLKST	DPLL CLKOUT status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:5	RESERVED		R	0x0
4:0	DIVHS	DPLL M2 post-divider factor (1 to 31). 0x0: Reserved 0x4: 4, to be used for both OPP_NOM and OPP_LOW	RW	0x01

Table 3-1112. Register Call Summary for Register CM_DIV_M2_DPLL_PER

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1] [2]
PRCM Register Manual • CKGEN_CM_CORE Register Summary: [3]

Table 3-1113. CM_DIV_M3_DPLL_PER

Address Offset	0x0000 0054		
Physical Address	0x4A00 8154	**Instance**	CKGEN_CM_CORE
Description	This register provides controls over the M3 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED							DIVHS	

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9	CLKST	DPLL CLKOUTHIF status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:5	RESERVED	Reserved	R	0x0
4:0	DIVHS	DPLL M3 post-divider factor (1 to 31). The values listed for 0x3 and 0x4 are used for maximum supported frequency at each OPP. Higher dividers (max 31), thus lower frequencies, are also supported. 0x0: Reserved 0x3: 3, to be used for OPP_NOM (when DPLL_PER is locked at 768MHz) 0x4: 4, to be used for OPP_LOW (when DPLL_PER is locked at 768MHz)	RW	0x01

Table 3-1114. Register Call Summary for Register CM_DIV_M3_DPLL_PER

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE Register Summary: [2]

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Table 3-1115. CM_DIV_H11_DPLL_PER

Address Offset	0x0000 0058		
Physical Address	0x4A00 8158	**Instance**	CKGEN_CM_CORE
Description	This register provides controls over the CLKOUT1 o/p of the HSDIVIDER1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED			DIVHS					

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x00000
9	CLKST	HSDIVIDER1 CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED	Reserved	R	0x0
5:0	DIVHS	DPLL (H11+1) post-divider factor (1 to 63). 0x0: Reserved 0x6: 6, to be used for both OPP_NOM and OPP_LOW (when DPLL_PER is locked at 768MHz)	RW	0x1

Table 3-1116. Register Call Summary for Register CM_DIV_H11_DPLL_PER

Clock Management Functional Description
- Synthesized Clock Parameters: [0] [1]

PRCM Register Manual
- CKGEN_CM_CORE Register Summary: [2]

Table 3-1117. CM_DIV_H12_DPLL_PER

Address Offset	0x0000 005C		
Physical Address	0x4A00 815C	**Instance**	CKGEN_CM_CORE
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED			DIVHS					

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x00000
9	CLKST	HSDIVIDER1 CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED	Reserved	R	0x0
5:0	DIVHS	DPLL (H12+1) post-divider factor (1 to 63). 0x0: Reserved 0x4: 4, to be used for both OPP_NOM and OPP_LOW	RW	0x1

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Table 3-1118. Register Call Summary for Register CM_DIV_H12_DPLL_PER

Clock Management Functional Description
• Synthesized Clock Parameters: [0] [1]
PRCM Register Manual
• CKGEN_CM_CORE Register Summary: [2]

Table 3-1119. CM_DIV_H14_DPLL_PER

Address Offset	0x0000 0064		
Physical Address	0x4A00 8164	**Instance**	CKGEN_CM_CORE
Description	This register provides controls over the CLKOUT4 o/p of the HSDIVIDER1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED					DIVHS			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x00000
9	CLKST	HSDIVIDER1 CLKOUT4 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:6	RESERVED	Reserved	R	0x0
5:0	DIVHS	DPLL (H14+1) post-divider factor (1 to 63). 0x0: Reserved 0x2: 2, to be used for OPP_NOM 0x4: 4, to be used for OPP_LOW	RW	0x1

Table 3-1120. Register Call Summary for Register CM_DIV_H14_DPLL_PER

Clock Management Functional Description
• Synthesized Clock Parameters: [0] [1]
PRCM Register Manual
• CKGEN_CM_CORE Register Summary: [2]

Table 3-1121. CM_SSC_DELTAMSTEP_DPLL_PER

Address Offset	0x0000 0068		
Physical Address	0x4A00 8168	**Instance**	CKGEN_CM_CORE
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DELTAMSTEP															

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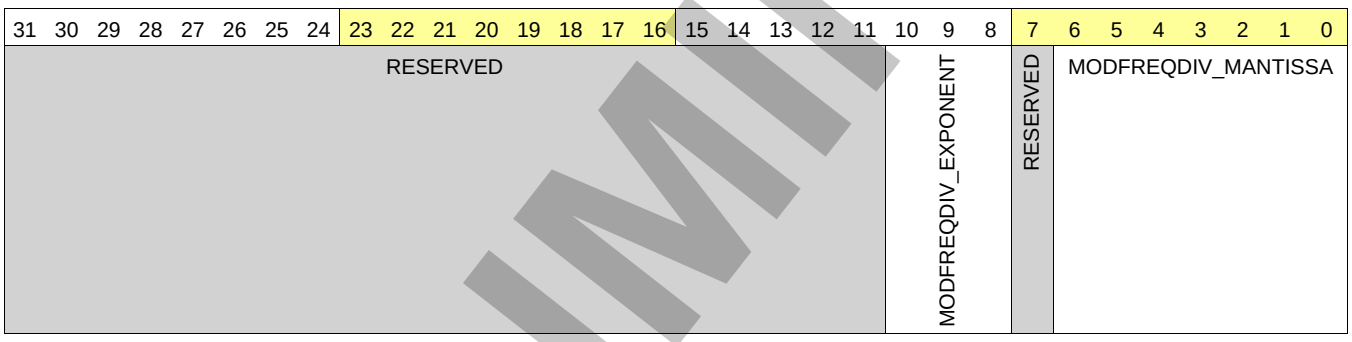
Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [19:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-1122. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_PER

Clock Management Functional Description • Spread Spectrum Clocking: [0]
PRCM Register Manual • CKGEN_CM_CORE Register Summary: [1]

Table 3-1123. CM_SSC_MODFREQDIV_DPLL_PER

Address Offset	0x0000 006C		
Physical Address	0x4A00 816C	**Instance**	CKGEN_CM_CORE
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-1124. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_PER

Clock Management Functional Description • Spread Spectrum Clocking: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE Register Summary: [2]

Table 3-1125. CM_CLKMODE_DPLL_USB

Address Offset	0x0000 0080		
Physical Address	0x4A00 8180	**Instance**	CKGEN_CM_CORE
Description	This register allows controlling the DPLL_USB modes.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	RESERVED									DPLL_EN		

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spread on both sides of the programmed frequency 0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency	RW	0
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11:3	RESERVED		R	0x000
2:0	DPLL_EN	DPLL control. Upon Warm Reset, the PRCM DPLL control state machine updates this register to reflect DPLL Low Power Stop mode. 0x0: Reserved 0x1: Put the DPLL in Low Power Stop mode 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: Put the DPLL in Idle Bypass Low Power mode. 0x6: Reserved 0x7: Enables the DPLL in Lock mode	RW	0x5

Table 3-1126. Register Call Summary for Register CM_CLKMODE_DPLL_USB

Clock Management Functional Description
- Power Modes: [0]
- Spread Spectrum Clocking: [1] [2] [3]

PRCM Register Manual
- CKGEN_CM_CORE Register Summary: [4]

Table 3-1127. CM_IDLEST_DPLL_USB

Address Offset	0x0000 0084		
Physical Address	0x4A00 8184	**Instance**	CKGEN_CM_CORE
Description	This register allows monitoring DPLL activity. This register is read only and automatically updated. [warm reset insensitive]		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											ST_DPLL_INIT	ST_DPLL_MODE			ST_DPLL_CLK

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000000
4	ST_DPLL_INIT	DPLL init status (for debug purpose). Read 0x1: DPLL has been init Read 0x0: DPLL is not init	R	0
3:1	ST_DPLL_MODE	DPLL mode status (for debug purpose). Read 0x0: Transient state. From reset to any LP (low power) idle state or from any power state to any power state (Power states are Low Power Stop mode, Fast Relock Stop mode, Idle Bypass Low Power mode and Idle Bypass Fast Relock mode). Read 0x1: The DPLL is in Low Power Stop mode Read 0x2: reserved Read 0x3: reserved Read 0x4: reserved Read 0x5: The DPLL is in Idle Bypass Low Power mode Read 0x6: reserved Read 0x7: reserved	R	0
0	ST_DPLL_CLK	DPLL lock status Read 0x1: DPLL is LOCKED Read 0x0: DPLL is either in bypass mode or in stop mode.	R	0

Table 3-1128. Register Call Summary for Register CM_IDLEST_DPLL_USB

PRCM Register Manual
- CKGEN_CM_CORE Register Summary: [0]

Table 3-1129. CM_AUTOIDLE_DPLL_USB

Address Offset	0x0000 0088		
Physical Address	0x4A00 8188	**Instance**	CKGEN_CM_CORE
Description	This register provides automatic control over the DPLL activity.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														AUTO_DPLL_MODE	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	AUTO_DPLL_MODE	DPLL automatic control; 0x0: DPLL auto control disabled 0x1: The DPLL is automatically put in Low Power Stop mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x2: Reserved 0x3: Reserved 0x4: Reserved 0x5: The DPLL is automatically put in Idle Bypass Low Power mode when its DPLL generated clocks are not required anymore. It is also restarted automatically. 0x6: Reserved 0x7: Reserved	RW	0x0

Table 3-1130. Register Call Summary for Register CM_AUTOIDLE_DPLL_USB

Clock Management Functional Description • Power Modes: [0]
PRCM Register Manual • CKGEN_CM_CORE Register Summary: [1]

Table 3-1131. CM_CLKSEL_DPLL_USB

Address Offset	0x0000 008C		
Physical Address	0x4A00 818C	**Instance**	CKGEN_CM_CORE
Description	This register provides controls over the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPLL_SD_DIV								DPLL_BYP_CLKSEL	DCC_EN	DPLL_SELFREQDCO	RESERVED	DPLL_MULT												DPLL_DIV							

Bits	Field Name	Description	Type	Reset
31:24	DPLL_SD_DIV	Sigma-Delta divider select (2-255). This factor must be set by software to ensure optimum jitter performance. DPLL_SD_DIV = CEILING ([DPLL_MULT/(DPLL_DIV+1)] * CLKINP / 250), where CLKINP is the input clock of the DPLL in MHz). DPLL_MULT must be set with M multiplier factor and DPLL_DIV with N divider factor, and must not be changed once DPLL is locked. For more information, see Section 3.6.3.9, *DPLL_USB Description*. 0x0: Reserved 0x1: Reserved	RW	0x04
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. Same as ULOWCLKEN on DPLL. In DPLL Locked mode, 0 - No impact 1 - No impact In DPLL Bypass mode, 0 - CLKINP is selected as the BYPASS clock for CLKOUT 1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT	RW	0

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Bits	Field Name	Description	Type	Reset
22	DCC_EN	Duty-cycle corrector for high frequency clock Read 0: Duty-cycle corrector is disabled	R	0x0
21	DPLL_SELFREQDCO	Select DCO output according to required frequency. 0x0: DCO clock is 1500MHz SELFREQDCO input of DPLL is set to '010' 0x1: DCO clock is 1250MHz SELFREQDCO input of DPLL is set to '100''	RW	0x0
20	RESERVED		R	0x0
19:8	DPLL_MULT	DPLL multiplier factor (2 to 4095). Equal to input M (multiplier) factor of DPLL; M=2 to 4095 = DPLL multiplies by M. [warm reset insensitive] 0x0: Reserved 0x1: Reserved	RW	0x000
7:0	DPLL_DIV	DPLL divider factor (0 to 255) Equal to input N (divider) factor of DPLL; actual division factor is N+1 [warm reset insensitive]	RW	0x00

Table 3-1132. Register Call Summary for Register CM_CLKSEL_DPLL_USB

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1] [2]
PRCM Register Manual • CKGEN_CM_CORE Register Summary: [3]

Table 3-1133. CM_DIV_M2_DPLL_USB

Address Offset	0x0000 0090		
Physical Address	0x4A00 8190	**Instance**	CKGEN_CM_CORE
Description	This register provides controls over the M2 divider of the DPLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLKST	RESERVED							DIVHS	

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00000
9	CLKST	DPLL CLKOUT status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:7	RESERVED		R	0x0
6:0	DIVHS	DPLL M2 post-divider factor (1 to 127). 0x0: Reserved 0x2: 2, to be used for both OPP_NOM and OPP_LOW	RW	0x01

Table 3-1134. Register Call Summary for Register CM_DIV_M2_DPLL_USB

Clock Management Functional Description • Synthesized Clock Parameters: [0] [1]
PRCM Register Manual • CKGEN_CM_CORE Register Summary: [2]

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Table 3-1135. CM_SSC_DELTAMSTEP_DPLL_USB

Address Offset	0x0000 00A8		
Physical Address	0x4A00 81A8	**Instance**	CKGEN_CM_CORE
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELTAMSTEP																							

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [20:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3-1136. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_USB

Clock Management Functional Description
- Spread Spectrum Clocking: [0]

PRCM Register Manual
- CKGEN_CM_CORE Register Summary: [1]

Table 3-1137. CM_SSC_MODFREQDIV_DPLL_USB

Address Offset	0x0000 00AC		
Physical Address	0x4A00 81AC	**Instance**	CKGEN_CM_CORE
Description	Control the Modulation Frequency (Fm) for Spread Spectrum. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						MODFREQDIV_EXPONENT			RESERVED	MODFREQDIV_MANTISSA					

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:8	MODFREQDIV_EXPONENT	Set the Exponent component of MODFREQDIV factor	RW	0x0
7	RESERVED		R	0
6:0	MODFREQDIV_MANTISSA	Set the Mantissa component of MODFREQDIV factor	RW	0x00

Table 3-1138. Register Call Summary for Register CM_SSC_MODFREQDIV_DPLL_USB

Clock Management Functional Description
- Spread Spectrum Clocking: [0] [1]

PRCM Register Manual
- CKGEN_CM_CORE Register Summary: [2]

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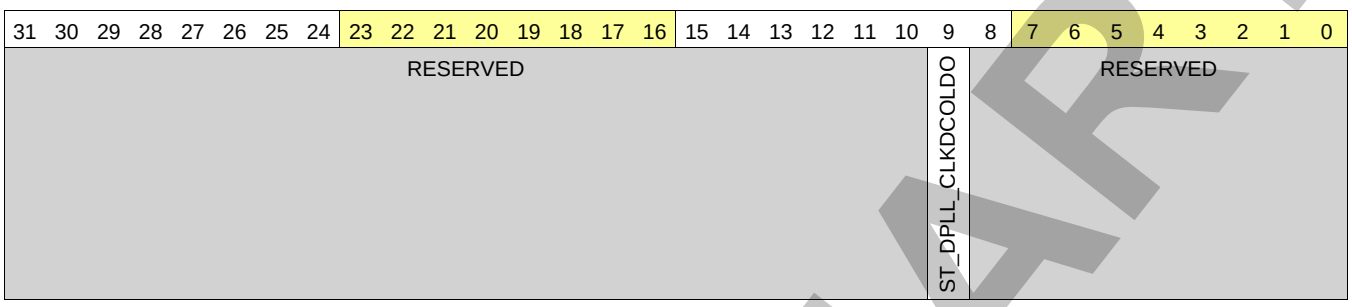
Table 3-1139. CM_CLKDCOLDO_DPLL_USB

Address Offset	0x0000 00B4		
Physical Address	0x4A00 81B4	**Instance**	CKGEN_CM_CORE
Description	This register provides status over CLKDCOLDO output of the DPLL.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	ST_DPLL_CLKDCOLDO	DPLL CLKDCOLDO status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8:0	RESERVED		R	0x00

Table 3-1140. Register Call Summary for Register CM_CLKDCOLDO_DPLL_USB

PRCM Register Manual
- CKGEN_CM_CORE Register Summary: [0]

3.11.31 COREAON_CM_CORE Registers

3.11.31.1 COREAON_CM_CORE Register Summary

Table 3-1141. COREAON_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	COREAON_CM_CORE Base Address
CM_COREAON_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 8600
CM_COREAON_SMARTREFLEX_MPU_CLKCTRL	RW	32	0x0000 0028	0x4A00 8628
CM_COREAON_SMARTREFLEX_MM_CLKCTRL	RW	32	0x0000 0030	0x4A00 8630
CM_COREAON_SMARTREFLEX_CORE_CLKCTRL	RW	32	0x0000 0038	0x4A00 8638
CM_COREAON_USB_PHY_CORE_CLKCTRL	RW	32	0x0000 0040	0x4A00 8640
RESERVED	R	32	0x0000 0048	0x4A00 8648
CM_COREAON_IO_SRCOMP_CLKCTRL	RW	32	0x0000 0050	0x4A00 8650

3.11.31.2 COREAON_CM_CORE Register Description

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Table 3-1142. CM_COREAON_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 8600	**Instance**	COREAON_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLKACTIVITY_COREAON_IO_SRCOMP_GFCLK	RESERVED	CLKACTIVITY_COREAON_32K_GFCLK	CLKACTIVITY_SR_CORE_SYS_GFCLK	CLKACTIVITY_SR_MM_SYS_GFCLK	CLKACTIVITY_SR_MPU_SYS_GFCLK	CLKACTIVITY_COREAON_L4_GICLK	RESERVED						CLKTRCTRL		

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	CLKACTIVITY_COREAON_IO_SRCOMP_GFCLK	This field indicates the state of the COREAON_IO_SRCOMP_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0x0
13	RESERVED		R	0x0
12	CLKACTIVITY_COREAON_32K_GFCLK	This field indicates the state of the COREAON_32K_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0x0
11	CLKACTIVITY_SR_CORE_SYS_GFCLK	This field indicates the state of the SR_CORE_SYS_GFCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
10	CLKACTIVITY_SR_MM_SYS_GFCLK	This field indicates the state of the SR_MM_SYS_GFCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
9	CLKACTIVITY_SR_MPU_SYS_GFCLK	This field indicates the state of the SR_MPU_SYS_GFCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0

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Bits	Field Name	Description	Type	Reset
8	CLKACTIVITY_COREAON_L4_GICLK	This field indicates the state of the COREAON_L4_GICLK clock of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the COREAON clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1143. Register Call Summary for Register CM_COREAON_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] [4] [5] [6]
PRCM Register Manual • COREAON_CM_CORE Register Summary: [7]

Table 3-1144. CM_COREAON_SMARTREFLEX_MPU_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 8628	**Instance**	COREAON_CM_CORE
Description	This register manages the SMARTREFLEX_MPU clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1145. Register Call Summary for Register CM_COREAON_SMARTREFLEX_MPU_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • COREAON_CM_CORE Register Summary: [2]

Table 3-1146. CM_COREAON_SMARTREFLEX_MM_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4A00 8630	**Instance**	COREAON_CM_CORE
Description	This register manages the SMARTREFLEX_MM clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

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Table 3-1147. Register Call Summary for Register CM_COREAON_SMARTREFLEX_MM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • COREAON_CM_CORE Register Summary: [2]

Table 3-1148. CM_COREAON_SMARTREFLEX_CORE_CLKCTRL

Address Offset	0x0000 0038		
Physical Address	0x4A00 8638	**Instance**	COREAON_CM_CORE
Description	This register manages the SMARTREFLEX_CORE clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1149. Register Call Summary for Register CM_COREAON_SMARTREFLEX_CORE_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • COREAON_CM_CORE Register Summary: [2]

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Table 3-1150. CM_COREAON_USB_PHY_CORE_CLKCTRL

Address Offset	0x0000 0040		
Physical Address	0x4A00 8640	**Instance**	COREAON_CM_CORE
Description	This register manages the USB_PHY_CORE 32KHz clock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							OPTFCLKEN_CLK32K	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	OPTFCLKEN_CLK32K	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:0	RESERVED		R	0x00

Table 3-1151. Register Call Summary for Register CM_COREAON_USB_PHY_CORE_CLKCTRL

Clock Management Functional Description
- Clock Domain Modes: [0]

PRCM Register Manual
- COREAON_CM_CORE Register Summary: [1]

Table 3-1152. CM_COREAON_IO_SRCOMP_CLKCTRL

Address Offset	0x0000 0050		
Physical Address	0x4A00 8650	**Instance**	COREAON_CM_CORE
Description	This register manages the clock delivered to the IO Slew rate compensation cells. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKEN_SRCOMP_FCLK	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	CLKEN_SRCOMP_FCLK	Functional clock control. 0x0: Functional clock is disabled 0x1: Functional clock is enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
7:0	RESERVED		R	0x00

Table 3-1153. Register Call Summary for Register CM_COREAON_IO_SRCOMP_CLKCTRL

Clock Management Functional Description • Clock Domain Modes: [0]
PRCM Register Manual • COREAON_CM_CORE Register Summary: [1]

3.11.32 CORE_CM_CORE Registers

3.11.32.1 CORE_CM_CORE Register Summary

Table 3-1154. CORE_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORE_CM_CORE Base Address
CM_L3MAIN1_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 8700
CM_L3MAIN1_DYNAMICDEP	RW	32	0x0000 0008	0x4A00 8708
CM_L3MAIN1_L3_MAIN_1_CLKCTRL	R	32	0x0000 0020	0x4A00 8720
CM_L3MAIN2_CLKSTCTRL	RW	32	0x0000 0100	0x4A00 8800
CM_L3MAIN2_DYNAMICDEP	RW	32	0x0000 0108	0x4A00 8808
CM_L3MAIN2_L3_MAIN_2_CLKCTRL	R	32	0x0000 0120	0x4A00 8820
CM_L3MAIN2_GPMC_CLKCTRL	RW	32	0x0000 0128	0x4A00 8828
CM_L3MAIN2_OCMC_RAM_CLKCTRL	R	32	0x0000 0130	0x4A00 8830
CM_IPU_CLKSTCTRL	RW	32	0x0000 0200	0x4A00 8900
CM_IPU_STATICDEP	RW	32	0x0000 0204	0x4A00 8904
CM_IPU_DYNAMICDEP	RW	32	0x0000 0208	0x4A00 8908
CM_IPU_IPU_CLKCTRL	RW	32	0x0000 0220	0x4A00 8920
CM_DMA_CLKSTCTRL	RW	32	0x0000 0300	0x4A00 8A00
CM_DMA_STATICDEP	RW	32	0x0000 0304	0x4A00 8A04
CM_DMA_DYNAMICDEP	R	32	0x0000 0308	0x4A00 8A08
CM_DMA_DMA_SYSTEM_CLKCTRL	R	32	0x0000 0320	0x4A00 8A20
CM_EMIF_CLKSTCTRL	RW	32	0x0000 0400	0x4A00 8B00
CM_EMIF_DMM_CLKCTRL	R	32	0x0000 0420	0x4A00 8B20
CM_EMIF_EMIF_OCP_FW_CLKCTRL	R	32	0x0000 0428	0x4A00 8B28
CM_EMIF_EMIF1_CLKCTRL	RW	32	0x0000 0430	0x4A00 8B30
CM_EMIF_EMIF2_CLKCTRL	RW	32	0x0000 0438	0x4A00 8B38
CM_EMIF_EMIF_DLL_CLKCTRL	RW	32	0x0000 0440	0x4A00 8B40
RESERVED	R	32	0x0000 0500	0x4A00 8C00
RESERVED	R	32	0x0000 0504	0x4A00 8C04
RESERVED	R	32	0x0000 0508	0x4A00 8C08
RESERVED	R	32	0x0000 0520	0x4A00 8C20
RESERVED	R	32	0x0000 0528	0x4A00 8C28
RESERVED	R	32	0x0000 0530	0x4A00 8C30
CM_L4CFG_CLKSTCTRL	RW	32	0x0000 0600	0x4A00 8D00
CM_L4CFG_DYNAMICDEP	RW	32	0x0000 0608	0x4A00 8D08
CM_L4CFG_L4_CFG_CLKCTRL	R	32	0x0000 0620	0x4A00 8D20
CM_L4CFG_SPINLOCK_CLKCTRL	R	32	0x0000 0628	0x4A00 8D28
CM_L4CFG_MAILBOX_CLKCTRL	R	32	0x0000 0630	0x4A00 8D30
CM_L4CFG_SAR_ROM_CLKCTRL	R	32	0x0000 0638	0x4A00 8D38

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Table 3-1154. CORE_CM_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CORE_CM_CORE Base Address
RESERVED	R	32	0x0000 0640	0x4A00 8D40
CM_L3INSTR_CLKSTCTRL	R	32	0x0000 0700	0x4A00 8E00
CM_L3INSTR_L3_MAIN_3_CLKCTRL	R	32	0x0000 0720	0x4A00 8E20
CM_L3INSTR_L3_INSTR_CLKCTRL	RW	32	0x0000 0728	0x4A00 8E28
CM_L3INSTR_OCP_WP_NOC_CLKCTRL	RW	32	0x0000 0740	0x4A00 8E40
CM_L3INSTR_DLL_AGING_CLKCTRL	R	32	0x0000 0748	0x4A00 8E48
CM_L3INSTR_CTRL_MODULE_BANDGAP_CLKCTRL	RW	32	0x0000 0750	0x4A00 8E50
RESERVED	R	32	0x0000 0800	0x4A00 8F00
RESERVED	R	32	0x0000 0804	0x4A00 8F04
RESERVED	R	32	0x0000 0808	0x4A00 8F08
RESERVED	R	32	0x0000 0820	0x4A00 8F20
RESERVED	R	32	0x0000 0828	0x4A00 8F28
RESERVED	R	32	0x0000 0830	0x4A00 8F30
CM_L4PER_CLKSTCTRL	RW	32	0x0000 0900	0x4A00 9000
CM_L4PER_DYNAMICDEP	RW	32	0x0000 0908	0x4A00 9008
CM_L4PER_TIMER10_CLKCTRL	RW	32	0x0000 0928	0x4A00 9028
CM_L4PER_TIMER11_CLKCTRL	RW	32	0x0000 0930	0x4A00 9030
CM_L4PER_TIMER2_CLKCTRL	RW	32	0x0000 0938	0x4A00 9038
CM_L4PER_TIMER3_CLKCTRL	RW	32	0x0000 0940	0x4A00 9040
CM_L4PER_TIMER4_CLKCTRL	RW	32	0x0000 0948	0x4A00 9048
CM_L4PER_TIMER9_CLKCTRL	RW	32	0x0000 0950	0x4A00 9050
CM_L4PER_ELM_CLKCTRL	R	32	0x0000 0958	0x4A00 9058
CM_L4PER_GPIO2_CLKCTRL	RW	32	0x0000 0960	0x4A00 9060
CM_L4PER_GPIO3_CLKCTRL	RW	32	0x0000 0968	0x4A00 9068
CM_L4PER_GPIO4_CLKCTRL	RW	32	0x0000 0970	0x4A00 9070
CM_L4PER_GPIO5_CLKCTRL	RW	32	0x0000 0978	0x4A00 9078
CM_L4PER_GPIO6_CLKCTRL	RW	32	0x0000 0980	0x4A00 9080
CM_L4PER_HDQ1W_CLKCTRL	RW	32	0x0000 0988	0x4A00 9088
CM_L4PER_I2C1_CLKCTRL	RW	32	0x0000 09A0	0x4A00 90A0
CM_L4PER_I2C2_CLKCTRL	RW	32	0x0000 09A8	0x4A00 90A8
CM_L4PER_I2C3_CLKCTRL	RW	32	0x0000 09B0	0x4A00 90B0
CM_L4PER_I2C4_CLKCTRL	RW	32	0x0000 09B8	0x4A00 90B8
CM_L4PER_L4_PER_CLKCTRL	R	32	0x0000 09C0	0x4A00 90C0
CM_L4PER_MCSPI1_CLKCTRL	RW	32	0x0000 09F0	0x4A00 90F0
CM_L4PER_MCSPI2_CLKCTRL	RW	32	0x0000 09F8	0x4A00 90F8
CM_L4PER_MCSPI3_CLKCTRL	RW	32	0x0000 0A00	0x4A00 9100
CM_L4PER_MCSPI4_CLKCTRL	RW	32	0x0000 0A08	0x4A00 9108
CM_L4PER_GPIO7_CLKCTRL	RW	32	0x0000 0A10	0x4A00 9110
CM_L4PER_GPIO8_CLKCTRL	RW	32	0x0000 0A18	0x4A00 9118
CM_L4PER_MMC3_CLKCTRL	RW	32	0x0000 0A20	0x4A00 9120
CM_L4PER_MMC4_CLKCTRL	RW	32	0x0000 0A28	0x4A00 9128
CM_L4PER_UART1_CLKCTRL	RW	32	0x0000 0A40	0x4A00 9140
CM_L4PER_UART2_CLKCTRL	RW	32	0x0000 0A48	0x4A00 9148
CM_L4PER_UART3_CLKCTRL	RW	32	0x0000 0A50	0x4A00 9150
CM_L4PER_UART4_CLKCTRL	RW	32	0x0000 0A58	0x4A00 9158
CM_L4PER_MMC5_CLKCTRL	RW	32	0x0000 0A60	0x4A00 9160

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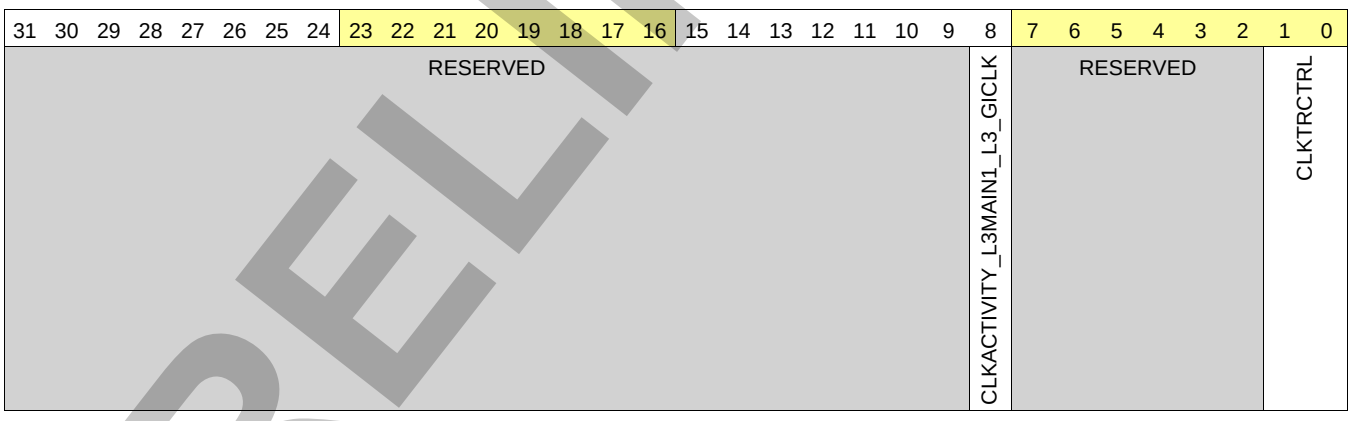
Table 3-1154. CORE_CM_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CORE_CM_CORE Base Address
CM_L4PER_I2C5_CLKCTRL	RW	32	0x0000 0A68	0x4A00 9168
CM_L4PER_UART5_CLKCTRL	RW	32	0x0000 0A70	0x4A00 9170
CM_L4PER_UART6_CLKCTRL	RW	32	0x0000 0A78	0x4A00 9178
CM_L4SEC_CLKSTCTRL	RW	32	0x0000 0A80	0x4A00 9180
CM_L4SEC_STATICDEP	RW	32	0x0000 0A84	0x4A00 9184
CM_L4SEC_DYNAMICDEP	R	32	0x0000 0A88	0x4A00 9188
CM_L4SEC_AES1_CLKCTRL	RW	32	0x0000 0AA0	0x4A00 91A0
CM_L4SEC_AES2_CLKCTRL	RW	32	0x0000 0AA8	0x4A00 91A8
CM_L4SEC_DES3DES_CLKCTRL	RW	32	0x0000 0AB0	0x4A00 91B0
CM_L4SEC_FPKA_CLKCTRL	RW	32	0x0000 0AB8	0x4A00 91B8
CM_L4SEC_RNG_CLKCTRL	RW	32	0x0000 0AC0	0x4A00 91C0
CM_L4SEC_SHA2MD5_CLKCTRL	RW	32	0x0000 0AC8	0x4A00 91C8
CM_L4SEC_DMA_CRYPTO_CLKCTRL	R	32	0x0000 0AD8	0x4A00 91D8

3.11.32.2 CORE_CM_CORE Register Description

Table 3-1155. CM_L3MAIN1_CLKSTCTRL

Address Offset	0x0000 0000
Physical Address	0x4A00 8700 **Instance** CORE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.
Type	RW



Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	CLKACTIVITY_L3MAIN1_L3_GICLK	This field indicates the state of the L3MAIN1_L3_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED	Reserved	R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	CLKTRCTRL	Controls the clock state transition of the L3_MAIN1 clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1156. Register Call Summary for Register CM_L3MAIN1_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2] • CORE_CM_CORE Register Description: [3]

Table 3-1157. CM_L3MAIN1_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 8708	**Instance**	CORE_CM_CORE
Description	This register controls the dynamic domain depedencies from L3_MAIN1 domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED								WKUPAON_DYNDEP	RESERVED		L4CFG_DYNDEP	RESERVED				L3MAIN2_DYNDEP	RESERVED		EMIF_DYNDEP	ABE_DYNDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:16	RESERVED	Reserved	R	0x000
15	WKUPAON_DYNDEP	Dynamic dependency towards WKUPAON clock domain Read 1: Dependency is enabled	R	0x1
14:13	RESERVED	Reserved	R	0x000
12	L4CFG_DYNDEP	Dynamic dependency towards L4_CFG clock domain Read 0x1: Dependency is enabled	R	1
11:7	RESERVED	Reserved	R	0x00
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3_MAIN2 clock domain Read 0x1: Dependency is enabled	R	1
5	RESERVED	Reserved	R	0
4	EMIF_DYNDEP	Dynamic dependency towards EMIF clock domain Read 0x1: Dependency is enabled	R	1
3	ABE_DYNDEP	Dynamic dependency towards ABE clock domain Read 0x1: Dependency is enabled	R	1

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Bits	Field Name	Description	Type	Reset
2:0	RESERVED	Reserved	R	0x0

Table 3-1158. Register Call Summary for Register CM_L3MAIN1_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [0] [1] [2] [3] [4]
PRCM Register Manual • CORE_CM_CORE Register Summary: [5]

Table 3-1159. CM_L3MAIN1_L3_MAIN_1_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 8720	**Instance**	CORE_CM_CORE
Description	This register manages the L3_MAIN1 clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3MAIN1_CLKSTCTRL[1:0] CLKTRCTRL = 0x3, any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1160. Register Call Summary for Register CM_L3MAIN1_L3_MAIN_1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

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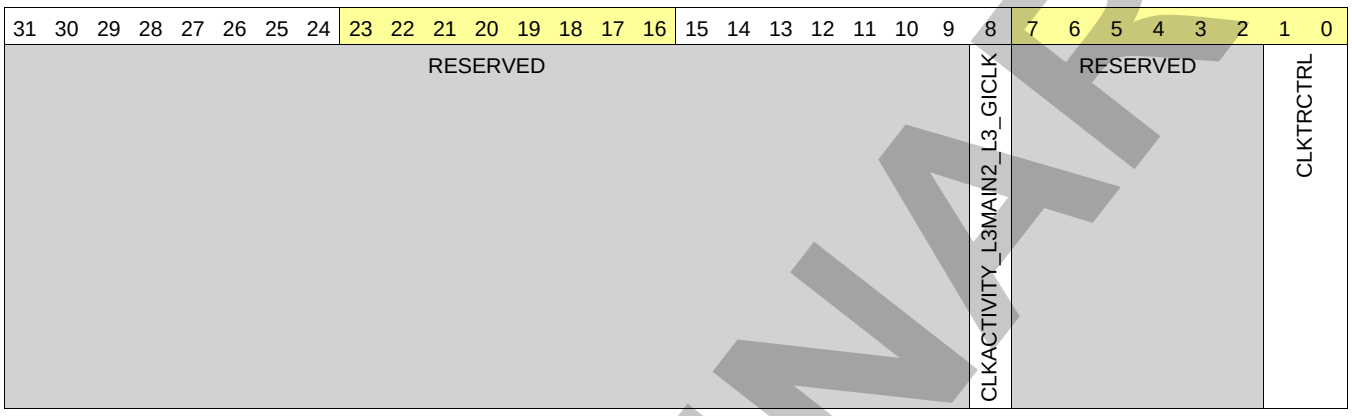
Table 3-1161. CM_L3MAIN2_CLKSTCTRL

Address Offset	0x0000 0100		
Physical Address	0x4A00 8800	**Instance**	CORE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	CLKACTIVITY_L3MAIN2_L3_GICLK	This field indicates the state of the L3MAIN2_L3_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED	Reserved	R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L3_MAIN2 clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1162. Register Call Summary for Register CM_L3MAIN2_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [2]
- CORE_CM_CORE Register Description: [3] [4] [5]

Table 3-1163. CM_L3MAIN2_DYNAMICDEP

Address Offset	0x0000 0108		
Physical Address	0x4A00 8808	**Instance**	CORE_CM_CORE
Description	This register controls the dynamic domain dependencies from L3_MAIN2 domain towards 'target' domains. It is relevant only for domain having INTERCONN master port(s).		
Type	RW		

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31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12 11	10	9	8	7 6	5	4 3	2	1	0
RESERVED	WINDOWSIZE	RESERVED		L4SEC_DYNDEP	L4PER_DYNDEP	RESERVED	GPU_DYNDEP	CAM_DYNDEP	DSS_DYNDEP	RESERVED	L3MAIN1_DYNDEP	RESERVED	IVA_DYNDEP	RESERVED	IPU_DYNDEP

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:15	RESERVED	Reserved	R	0x000
14	L4SEC_DYNDEP	Dynamic dependency towards L4SEC clock domain Read 1: Dependency is enabled	R	1
13	L4PER_DYNDEP	Dynamic dependency towards L4_PER clock domain Read 0x1: Dependency is enabled	R	1
12:11	RESERVED	Reserved	R	0x0
10	GPU_DYNDEP	Dynamic dependency towards GPU clock domain Read 0x1: Dependency is enabled	R	1
9	CAM_DYNDEP	Dynamic dependency towards CAM clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R	1
7:6	RESERVED	Reserved	R	0
5	L3MAIN1_DYNDEP	Dynamic dependency towards L3_MAIN1 clock domain Read 0x1: Dependency is enabled	R	1
4:3	RESERVED	Reserved	R	0x0
2	IVA_DYNDEP	Dynamic dependency towards IVA clock domain Read 0x1: Dependency is enabled	R	1
1	RESERVED	Reserved	R	0
0	IPU_DYNDEP	Dynamic dependency towards IPU clock domain Read 0x1: Dependency is enabled	R	1

Table 3-1164. Register Call Summary for Register CM_L3MAIN2_DYNAMICDEP

Clock Management Functional Description
- Dynamic Dependency: [1] [2] [3] [4] [5] [6] [7] [8]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [9]

Table 3-1165. CM_L3MAIN2_L3_MAIN_2_CLKCTRL

Address Offset	0x0000 0120		
Physical Address	0x4A00 8820	**Instance**	CORE_CM_CORE
Description	This register manages the L3_MAIN2 clocks.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3MAIN2_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1166. Register Call Summary for Register CM_L3MAIN2_L3_MAIN_2_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [2]

Table 3-1167. CM_L3MAIN2_GPMC_CLKCTRL

Address Offset	0x0000 0128		
Physical Address	0x4A00 8828	**Instance**	CORE_CM_CORE
Description	This register manages the GPMC clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is temporarily disabled by SW. Interconnect access to module are stalled. Can be used to change timing parameter of GPMC module. 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3MAIN2_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1168. Register Call Summary for Register CM_L3MAIN2_GPMC_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1169. CM_L3MAIN2_OCMC_RAM_CLKCTRL

Address Offset	0x0000 0130		
Physical Address	0x4A00 8830	**Instance**	CORE_CM_CORE
Description	This register manages the OCMC_RAM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3MAIN2_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1170. Register Call Summary for Register CM_L3MAIN2_OCMC_RAM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1171. CM_IPU_CLKSTCTRL

Address Offset	0x0000 0200		
Physical Address	0x4A00 8900	**Instance**	CORE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_IPU_CLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_IPU_CLK	This field indicates the state of the IPU_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	CLKTRCTRL	Controls the clock state transition of the IPU clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1172. Register Call Summary for Register CM_IPU_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2] • CORE_CM_CORE Register Description: [3]

Table 3-1173. CM_IPU_STATICDEP

Address Offset	0x0000 0204		
Physical Address	0x4A00 8904	**Instance**	CORE_CM_CORE
Description	This register controls the static domain dependencies from IPU domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															COREAON_STATDEP	WKUPAON_STATDEP	L4SEC_STATDEP	L4PER_STATDEP	L4CFG_STATDEP	SDMA_STATDEP	GPU_STATDEP	CAM_STATDEP	DSS_STATDEP	L3INIT_STATDEP	L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	ABE_STATDEP	IVA_STATDEP	DSP_STATDEP	RESERVED

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	COREAON_STATDEP	Static dependency towards COREAON clock domain Read 0x0: Dependency is disabled	R	0
15	WKUPAON_STATDEP	Static dependency towards WKUPAON clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
14	L4SEC_STATDEP	Static dependency towards L4SEC clock domain 0: Dependency is disabled 1: Dependency is enabled	RW	0
13	L4PER_STATDEP	Static dependency towards L4_PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	L4CFG_STATDEP	Static dependency towards L4_CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
11	SDMA_STATDEP	Static dependency towards DMA_SYSTEM clock domain Read 0x0: Dependency is disabled	R	0
10	GPU_STATDEP	Static dependency towards GPU clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
9	CAM_STATDEP	Static dependency towards CAM clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_STATDEP	Static dependency towards DSS clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	L3MAIN2_STATDEP	Static dependency towards L3_MAIN2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5	L3MAIN1_STATDEP	Static dependency towards L3_MAIN1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVA_STATDEP	Static dependency towards IVA clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	DSP_STATDEP	Static dependency towards DSP clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	RESERVED		R	0

Table 3-1174. Register Call Summary for Register CM_IPU_STATICDEP

Clock Management Functional Description • Static Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] • Static Dependency: [17]
PRCM Register Manual • CORE_CM_CORE Register Summary: [18]

Table 3-1175. CM_IPU_DYNAMICDEP

Address Offset	0x0000 0208		
Physical Address	0x4A00 8908	**Instance**	CORE_CM_CORE
Description	This register controls the dynamic domain depedencies from IPU domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED														CAM_DYNDEP	RESERVED	L3_2_DYNDEP	RESERVED						

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:10	RESERVED		R	0x0000
9	CAM_DYNDEP	Dynamic dependency towards CAM clock domain Read 0x0: Dependency is disabled	R	0
8:7	RESERVED		R	0x0
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3_MAIN2 clock domain Read 0x1: Dependency is enabled	R	1
5:0	RESERVED		R	0x00

Table 3-1176. Register Call Summary for Register CM_IPU_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1177. CM_IPU_IPU_CLKCTRL

Address Offset	0x0000 0220		
Physical Address	0x4A00 8920	**Instance**	CORE_CM_CORE
Description	This register manages the IPU clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_IPU_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1178. Register Call Summary for Register CM_IPU_IPU_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2]
PRCM Register Manual • CORE_CM_CORE Register Summary: [3]

Table 3-1179. CM_DMA_CLKSTCTRL

Address Offset	0x0000 0300		
Physical Address	0x4A00 8A00	**Instance**	CORE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_DMA_L3_GICLK	RESERVED						CLKTRCTRL	

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_DMA_L3_GICLK	This field indicates the state of the L3_DMA_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the DMA_SYSTEM clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1180. Register Call Summary for Register CM_DMA_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [2]
- CORE_CM_CORE Register Description: [3]

Table 3-1181. CM_DMA_STATICDEP

Address Offset	0x0000 0304		
Physical Address	0x4A00 8A04	**Instance**	CORE_CM_CORE
Description	This register controls the static domain dependencies from DMA_SYSTEM domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																WKUPAON_STATDEP	L4SEC_STATDEP	L4PER_STATDEP	L4CFG_STATDEP	RESERVED		CAM_STATDEP	DSS_STATDEP	L3INIT_STATDEP	L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	ABE_STATDEP	IVA_STATDEP	RESERVED	IPU_STATDEP

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	WKUPAON_STATDEP	Static dependency towards WKUPAON clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
14	L4SEC_STATDEP	Static dependency towards L4SEC clock domain 0: Dependency is disabled 1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	L4PER_STATDEP	Static dependency towards L4_PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
12	L4CFG_STATDEP	Static dependency towards L4_CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
11:10	RESERVED		R	0x0
9	CAM_STATDEP	Static dependency towards CAM clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_STATDEP	Static dependency towards DSS clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	L3INIT_STATDEP	Static dependency towards L3INIT clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
6	L3MAIN2_STATDEP	Static dependency towards L3_MAIN2 clock domain Read 0x1: Dependency is enabled	R	1
5	L3MAIN1_STATDEP	Static dependency towards L3_MAIN1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVA_STATDEP	Static dependency towards IVA clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	RESERVED		R	0
0	IPU_STATDEP	Static dependency towards IPU clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3-1182. Register Call Summary for Register CM_DMA_STATICDEP

Clock Management Functional Description • Static Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
PRCM Register Manual • CORE_CM_CORE Register Summary: [11]

Table 3-1183. CM_DMA_DYNAMICDEP

Address Offset	0x0000 0308		
Physical Address	0x4A00 8A08	**Instance**	CORE_CM_CORE
Description	This register controls the dynamic domain depedencies from DMA_SYSTEM domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									L3_2_DYNDEP	RESERVED						

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3_MAIN2 clock domain Read 0x0: Dependency is disabled	R	0
5:0	RESERVED		R	0x00

Table 3-1184. Register Call Summary for Register CM_DMA_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [0]
PRCM Register Manual • CORE_CM_CORE Register Summary: [1]

Table 3-1185. CM_DMA_DMA_SYSTEM_CLKCTRL

Address Offset	0x0000 0320		
Physical Address	0x4A00 8A20	**Instance**	CORE_CM_CORE
Description	This register manages the DMA_SYSTEM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE		

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_DMA_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1186. Register Call Summary for Register CM_DMA_DMA_SYSTEM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2]
PRCM Register Manual • CORE_CM_CORE Register Summary: [3]

Table 3-1187. CM_EMIF_CLKSTCTRL

Address Offset	0x0000 0400		
Physical Address	0x4A00 8B00	**Instance**	CORE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also hold one status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					CLKACTIVITY_EMIF_PHY_GCLK	CLKACTIVITY_DLL_GCLK	CLKACTIVITY_EMIF_L3_GICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x0 0000
10	CLKACTIVITY_EMIF_PHY_GCLK	This field indicates the state of the EMIF_PHY_GCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
9	CLKACTIVITY_DLL_GCLK	This field indicates the state of the DLL_GCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0

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Bits	Field Name	Description	Type	Reset
8	CLKACTIVITY_EMIF_L3_GICLK	This field indicates the state of the EMIF_L3_GICLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the EMIF clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions. Read 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain.	RW	0x0

Table 3-1188. Register Call Summary for Register CM_EMIF_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [2] [3] [4]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [5]
- CORE_CM_CORE Register Description: [6] [7] [8]

Table 3-1189. CM_EMIF_DMM_CLKCTRL

Address Offset	0x0000 0420		
Physical Address	0x4A00 8B20	**Instance**	CORE_CM_CORE
Description	This register manages the DMM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_EMIF_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1190. Register Call Summary for Register CM_EMIF_DMM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1191. CM_EMIF_EMIF_OCP_FW_CLKCTRL

Address Offset	0x0000 0428		
Physical Address	0x4A00 8B28	**Instance**	CORE_CM_CORE
Description	This register manages the EMIF_OCP_FW clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_EMIF_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

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Table 3-1192. Register Call Summary for Register CM_EMIF_EMIF_OCP_FW_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [2]

Table 3-1193. CM_EMIF_EMIF1_CLKCTRL

Address Offset	0x0000 0430		
Physical Address	0x4A00 8B30	**Instance**	CORE_CM_CORE
Description	This register manages the EMIF1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including OCP Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is temporarily disabled by SW. OCP access to module are stalled. Can be used to change timing parameter of EMIF_1 module. 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1194. Register Call Summary for Register CM_EMIF_EMIF1_CLKCTRL

Clock Management Functional Description
- CM_CORE Clock Generator:
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [3]

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Table 3-1195. CM_EMIF_EMIF2_CLKCTRL

Address Offset	0x0000 0438		
Physical Address	0x4A00 8B38	**Instance**	CORE_CM_CORE
Description	This register manages the EMIF2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is temporarily disabled by SW. Interconnect access to module are stalled. Can be used to change timing parameter of EMIF2 module. 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_EMIF_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1196. Register Call Summary for Register CM_EMIF_EMIF2_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [2]

Table 3-1197. CM_EMIF_EMIF_DLL_CLKCTRL

Address Offset	0x0000 0440		
Physical Address	0x4A00 8B40	**Instance**	CORE_CM_CORE
Description	This register manages the DLL clock.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							OPTFCLKEN_DLL_CLK	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	OPTFCLKEN_DLL_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled. DLL_CLK can be gated when EMIF domain performs sleep transition 0x1: Optional functional clock is enabled. DLL_CLK is garantied to not be gated if already running.	RW	0
7:0	RESERVED		R	0x00

Table 3-1198. Register Call Summary for Register CM_EMIF_EMIF_DLL_CLKCTRL

Clock Management Functional Description • Clock Domain Modes: [0]
PRCM Register Manual • CORE_CM_CORE Register Summary: [1]

Table 3-1199. CM_L4CFG_CLKSTCTRL

Address Offset	0x0000 0600		
Physical Address	0x4A00 8D00	**Instance**	CORE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLKACTIVITY_L4CFG_L4_GICLK	RESERVED						CLKTRCTRL

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	CLKACTIVITY_L4CFG_L4_GICLK	This field indicates the state of the L4CFG_L4_GICLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L4CFG clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x2: Reserved Read 0x1: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1200. Register Call Summary for Register CM_L4CFG_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [2]
- CORE_CM_CORE Register Description: [3] [4] [5] [6]

Table 3-1201. CM_L4CFG_DYNAMICDEP

Address Offset	0x0000 0608		
Physical Address	0x4A00 8D08	**Instance**	CORE_CM_CORE
Description	This register controls the dynamic domain depedencies from L4CFG domain towards 'target' domains. It is relevant only for domain having OCP master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED				MPU_DYNDEP	RESERVED	CUSTEFUSE_DYNDEP	COREAON_DYNDEP	RESERVED				SDMA_DYNDEP	RESERVED	CAM_DYNDEP	RESERVED	L3INIT_DYNDEP	L3MAIN2_DYNDEP	L3MAIN1_DYNDEP	EMIF_DYNDEP	RESERVED		DSP_DYNDEP	RESERVED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor OCP interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:20	RESERVED		R	0x0
19	MPU_DYNDEP	Dynamic dependency towards MPU clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
18	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
17	CUSTEFUSE_DYNDEP	Dynamic dependency towards CUSTEFUSE clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
16	COREAON_DYNDEP	Dynamic dependency towards COREAON clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
15:12	RESERVED		R	0x0
11	SDMA_DYNDEP	Dynamic dependency towards DMA clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
10	RESERVED		R	0
9	CAM_DYNDEP	Dynamic dependency towards CAM clock domain Read 0x0: Dependency is disabled	R	0
8	RESERVED		R	0
7	L3INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3MAIN2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3MAIN1_DYNDEP	Dynamic dependency towards L3MAIN1 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
4	EMIF_DYNDEP	Dynamic dependency towards EMIF clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
3:2	RESERVED		R	0x0
1	DSP_DYNDEP	Dynamic dependency towards DSP clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
0	RESERVED		R	0

Table 3-1202. Register Call Summary for Register CM_L4CFG_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
PRCM Register Manual • CORE_CM_CORE Register Summary: [11]

Table 3-1203. CM_L4CFG_L4_CFG_CLKCTRL

Address Offset	0x0000 0620		
Physical Address	0x4A00 8D20	**Instance**	CORE_CM_CORE
Description	This register manages the L4_CFG clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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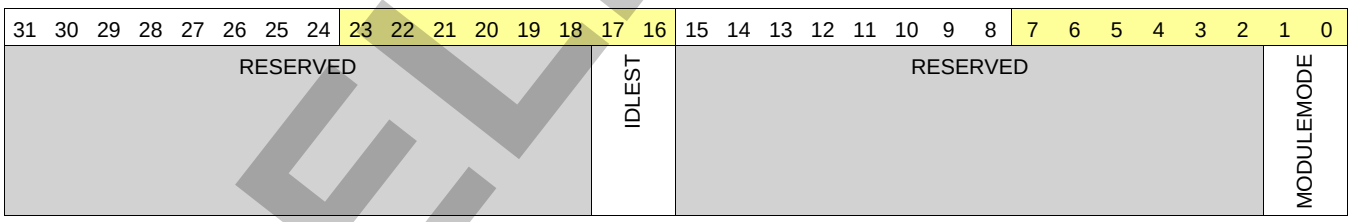
Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L4CFG_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1204. Register Call Summary for Register CM_L4CFG_L4_CFG_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1205. CM_L4CFG_SPINLOCK_CLKCTRL

Address Offset	0x0000 0628		
Physical Address	0x4A00 8D28	**Instance**	CORE_CM_CORE
Description	This register manages the SPINLOCK clocks.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L4CFG_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1206. Register Call Summary for Register CM_L4CFG_SPINLOCK_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1207. CM_L4CFG_MAILBOX_CLKCTRL

Address Offset	0x0000 0630		
Physical Address	0x4A00 8D30	**Instance**	CORE_CM_CORE
Description	This register manages the MAILBOX clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L4CFG_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

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Table 3-1208. Register Call Summary for Register CM_L4CFG_MAILBOX_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1209. CM_L4CFG_SAR_ROM_CLKCTRL

Address Offset	0x0000 0638		
Physical Address	0x4A00 8D38	**Instance**	CORE_CM_CORE
Description	This register manages the SAR_ROM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L4CFG_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state.	R	0x1

Table 3-1210. Register Call Summary for Register CM_L4CFG_SAR_ROM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

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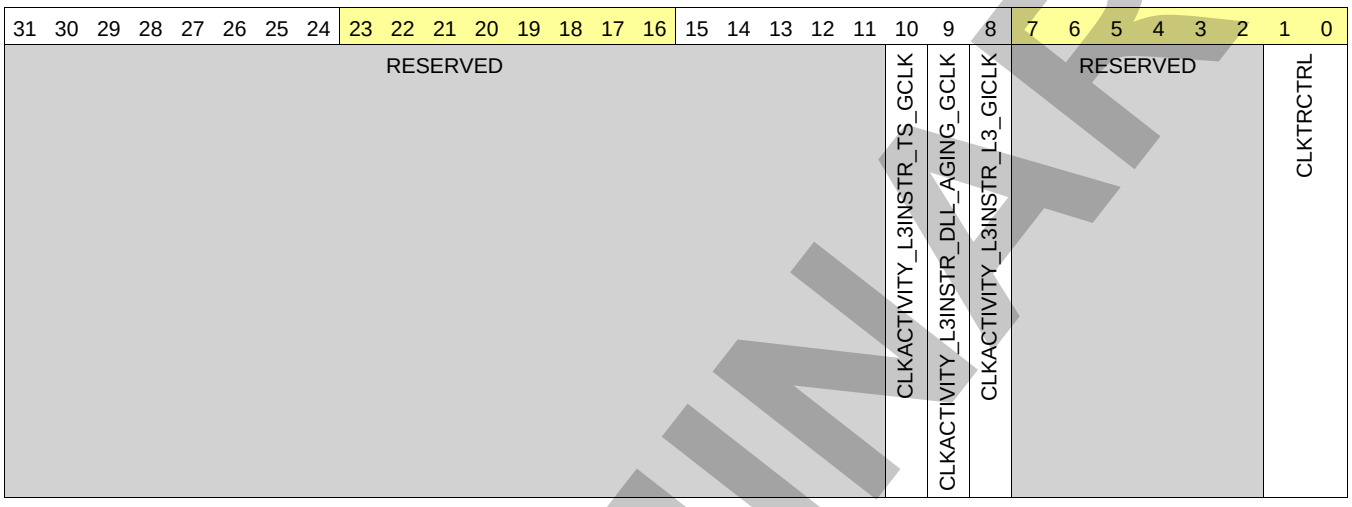
Table 3-1211. CM_L3INSTR_CLKSTCTRL

Address Offset	0x0000 0700		
Physical Address	0x4A00 8E00	**Instance**	CORE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also hold one status bit per clock input of the domain.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x00 0000
10	CLKACTIVITY_L3INSTR_TS_GCLK	This field indicates the state of the L3INSTR_TS_GCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
9	CLKACTIVITY_L3INSTR_DLL_AGING_GCLK	This field indicates the state of the L3INSTR_DLL_AGING_GCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
8	CLKACTIVITY_L3INSTR_L3_GICLK	This field indicates the state of the L3INSTR_L3_GICLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L3INSTR clock domain. Read 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	R Rreturns 1s	0x3

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Table 3-1212. Register Call Summary for Register CM_L3INSTR_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3]
PRCM Register Manual • CORE_CM_CORE Register Summary: [4] • CORE_CM_CORE Register Description: [5] [6] [7] [8]

Table 3-1213. CM_L3INSTR_L3_MAIN_3_CLKCTRL

Address Offset	0x0000 0720		
Physical Address	0x4A00 8E20	**Instance**	CORE_CM_CORE
Description	This register manages the L3_MAIN3 clocks. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3INSTR_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1214. Register Call Summary for Register CM_L3INSTR_L3_MAIN_3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

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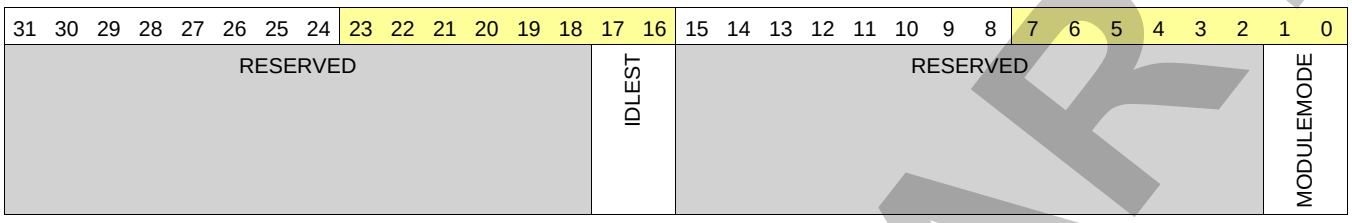
Table 3-1215. CM_L3INSTR_L3_INSTR_CLKCTRL

Address Offset	0x0000 0728		
Physical Address	0x4A00 8E28	**Instance**	CORE_CM_CORE
Description	This register manages the L3 INSTRUMENTATION clocks. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3INSTR_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1216. Register Call Summary for Register CM_L3INSTR_L3_INSTR_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [2]

Table 3-1217. CM_L3INSTR_OCP_WP_NOC_CLKCTRL

Address Offset	0x0000 0740		
Physical Address	0x4A00 8E40	**Instance**	CORE_CM_CORE
Description	This register manages the OCP_WP_NOC clocks. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including Interconnect	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3INSTR_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any Interconnect access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x1

Table 3-1218. Register Call Summary for Register CM_L3INSTR_OCP_WP_NOC_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1219. CM_L3INSTR_DLL_AGING_CLKCTRL

Address Offset	0x0000 0748		
Physical Address	0x4A00 8E48	**Instance**	CORE_CM_CORE
Description	This register manages the DLL_AGING clocks		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including Interconnect	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x0: Reserved Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3INSTR_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any Interconnect access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	R	0x1

Table 3-1220. Register Call Summary for Register CM_L3INSTR_DLL_AGING_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1221. CM_L3INSTR_CTRL_MODULE_BANDGAP_CLKCTRL

Address Offset	0x0000 0750		
Physical Address	0x4A00 8E50	**Instance**	CORE_CM_CORE
Description	This register manages the CTRL_MODULE_BANDGAP clock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLKSEL	RESERVED							IDLEST	RESERVED													MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	CLKSEL	Selects the divider value for generating the Thermal Sensor clock from WKUPAON_ICLK source. The divider has to be selected so as to guarantee a frequency between 1MHz and 2MHz. 0x0: Divide by 8 0x1: Divide by 16 0x3: Reserved 0x2: Divide by 32	RW	0x2
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1222. Register Call Summary for Register CM_L3INSTR_CTRL_MODULE_BANDGAP_CLKCTRL

Clock Management Functional Description
- PRM Clock Source: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [3]

Table 3-1223. CM_L4PER_CLKSTCTRL

Address Offset	0x0000 0900		
Physical Address	0x4A00 9000	**Instance**	CORE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also hold one status bit per clock input of the domain.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CLKACTIVITY_PER_96M_GFCLK	CLKACTIVITY_PER_48M_GFCLK	CLKACTIVITY_PER_32K_GFCLK	RESERVED	CLKACTIVITY_PER_12M_GFCLK	CLKACTIVITY_TIMER9_GFCLK	CLKACTIVITY_TIMER4_GFCLK	CLKACTIVITY_TIMER3_GFCLK	CLKACTIVITY_TIMER2_GFCLK	CLKACTIVITY_TIMER11_GFCLK	CLKACTIVITY_TIMER10_GFCLK	CLKACTIVITY_L4PER_L4_GICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	CLKACTIVITY_PER_96M_GFCLK	This field indicates the state of the PER_96M_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
18	CLKACTIVITY_PER_48M_GFCLK	This field indicates the state of the PER_48M_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
17	CLKACTIVITY_PER_32K_GFCLK	This field indicates the state of the PER_32K_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
16	RESERVED		R	0
15	CLKACTIVITY_PER_12M_GFCLK	This field indicates the state of the PER_12M_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
14	CLKACTIVITY_TIMER9_GFCLK	This field indicates the state of the TIMER9_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
13	CLKACTIVITY_TIMER4_GFCLK	This field indicates the state of the TIMER4_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
12	CLKACTIVITY_TIMER3_GFCLK	This field indicates the state of the TIMER3_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0

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Bits	Field Name	Description	Type	Reset
11	CLKACTIVITY_TIMER2_GFCLK	This field indicates the state of the TIMER2_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
10	CLKACTIVITY_TIMER11_GFCLK	This field indicates the state of the TIMER11_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
9	CLKACTIVITY_TIMER10_GFCLK	This field indicates the state of the TIMER10_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
8	CLKACTIVITY_L4PER_L4_GICLK	This field indicates the state of the L4PER_L4_GICLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L4PER clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain.	RW	0x0

Table 3-1224. Register Call Summary for Register CM_L4PER_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]
PRCM Register Manual • CORE_CM_CORE Register Summary: [12]

Table 3-1225. CM_L4PER_DYNAMICDEP

Address Offset	0x0000 0908		
Physical Address	0x4A00 9008	**Instance**	CORE_CM_CORE
Description	This register controls the dynamic domain depedencies from L4PER domain towards 'target' domains. It is relevant only for domain having OCP master port(s).		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED								L4SEC_DYNDEP	RESERVED						DSS_DYNDEP	L3INIT_DYNDEP	RESERVED						

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTERCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:15	RESERVED		R	0x000
14	L4SEC_DYNDEP	Dynamic dependency towards L4SEC clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
13:9	RESERVED		R	0x00
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
7	L3INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
6:0	RESERVED		R	0x00

Table 3-1226. Register Call Summary for Register CM_L4PER_DYNAMICDEP

Clock Management Functional Description
- Dynamic Dependency: [0] [1] [2]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [3]

Table 3-1227. CM_L4PER_TIMER10_CLKCTRL

Address Offset	0x0000 0928		
Physical Address	0x4A00 9028	**Instance**	CORE_CM_CORE
Description	This register manages the TIMER10 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED															MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only INTERCONN part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including INTERCONN	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any INTERCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1228. Register Call Summary for Register CM_L4PER_TIMER10_CLKCTRL

Clock Management Functional Description • CD_PRM_TIMER Overview: [0] • Clock Domain Module Attributes: [1] [2]
PRCM Register Manual • CORE_CM_CORE Register Summary: [3]

Table 3-1229. CM_L4PER_TIMER11_CLKCTRL

Address Offset	0x0000 0930		
Physical Address	0x4A00 9030	**Instance**	CORE_CM_CORE
Description	This register manages the TIMER11 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1230. Register Call Summary for Register CM_L4PER_TIMER11_CLKCTRL

Clock Management Functional Description
- CD_PRM_TIMER Overview: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [3]

Table 3-1231. CM_L4PER_TIMER2_CLKCTRL

Address Offset	0x0000 0938		
Physical Address	0x4A00 9038	**Instance**	CORE_CM_CORE
Description	This register manages the TIMER2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1232. Register Call Summary for Register CM_L4PER_TIMER2_CLKCTRL

Clock Management Functional Description • CD_PRM_TIMER Overview: [0] • Clock Domain Module Attributes: [1] [2]
PRCM Register Manual • CORE_CM_CORE Register Summary: [3]

Table 3-1233. CM_L4PER_TIMER3_CLKCTRL

Address Offset	0x0000 0940		
Physical Address	0x4A00 9040	**Instance**	CORE_CM_CORE
Description	This register manages the TIMER3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1234. Register Call Summary for Register CM_L4PER_TIMER3_CLKCTRL

Clock Management Functional Description
- CD_PRM_TIMER Overview: [0]
- Clock Domain Module Attributes: [1] [2]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [3]

Table 3-1235. CM_L4PER_TIMER4_CLKCTRL

Address Offset	0x0000 0948		
Physical Address	0x4A00 9048	**Instance**	CORE_CM_CORE
Description	This register manages the TIMER4 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1236. Register Call Summary for Register CM_L4PER_TIMER4_CLKCTRL

Clock Management Functional Description • CD_PRM_TIMER Overview: [0] • Clock Domain Module Attributes: [1] [2]
PRCM Register Manual • CORE_CM_CORE Register Summary: [3]

Table 3-1237. CM_L4PER_TIMER9_CLKCTRL

Address Offset	0x0000 0950		
Physical Address	0x4A00 9050	**Instance**	CORE_CM_CORE
Description	This register manages the TIMER9 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED						IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Select the source of the functional clock 0x0: Selects the SYS_CLK as the source 0x1: Selects the 32KHz as the source	RW	0
23:18	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1238. Register Call Summary for Register CM_L4PER_TIMER9_CLKCTRL

Clock Management Functional Description • CD_PRM_TIMER Overview: [0] • Clock Domain Module Attributes: [1] [2]
PRCM Register Manual • CORE_CM_CORE Register Summary: [3]

Table 3-1239. CM_L4PER_ELM_CLKCTRL

Address Offset	0x0000 0958		
Physical Address	0x4A00 9058	**Instance**	CORE_CM_CORE
Description	This register manages the ELM clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1240. Register Call Summary for Register CM_L4PER_ELM_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1241. CM_L4PER_GPIO2_CLKCTRL

Address Offset	0x0000 0960		
Physical Address	0x4A00 9060	**Instance**	CORE_CM_CORE
Description	This register manages the GPIO2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1242. Register Call Summary for Register CM_L4PER_GPIO2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1243. CM_L4PER_GPIO3_CLKCTRL

Address Offset	0x0000 0968		
Physical Address	0x4A00 9068	**Instance**	CORE_CM_CORE
Description	This register manages the GPIO3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1244. Register Call Summary for Register CM_L4PER_GPIO3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1245. CM_L4PER_GPIO4_CLKCTRL

Address Offset	0x0000 0970		
Physical Address	0x4A00 9070	**Instance**	CORE_CM_CORE
Description	This register manages the GPIO4 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1246. Register Call Summary for Register CM_L4PER_GPIO4_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1247. CM_L4PER_GPIO5_CLKCTRL

Address Offset	0x0000 0978		
Physical Address	0x4A00 9078	**Instance**	CORE_CM_CORE
Description	This register manages the GPIO5 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1248. Register Call Summary for Register CM_L4PER_GPIO5_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1249. CM_L4PER_GPIO6_CLKCTRL

Address Offset	0x0000 0980		
Physical Address	0x4A00 9080	**Instance**	CORE_CM_CORE
Description	This register manages the GPIO6 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1250. Register Call Summary for Register CM_L4PER_GPIO6_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1251. CM_L4PER_HDQ1W_CLKCTRL

Address Offset	0x0000 0988		
Physical Address	0x4A00 9088	**Instance**	CORE_CM_CORE
Description	This register manages the HDQ1W clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

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Table 3-1252. Register Call Summary for Register CM_L4PER_HDQ1W_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1253. CM_L4PER_I2C1_CLKCTRL

Address Offset	0x0000 09A0		
Physical Address	0x4A00 90A0	**Instance**	CORE_CM_CORE
Description	This register manages the I2C1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1254. Register Call Summary for Register CM_L4PER_I2C1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2]
PRCM Register Manual • CORE_CM_CORE Register Summary: [3]

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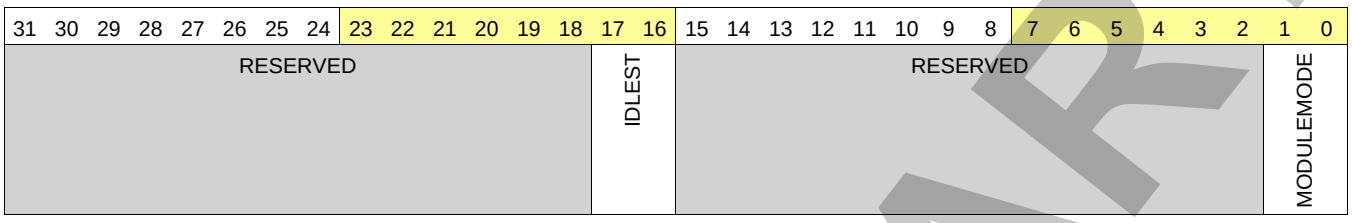
Table 3-1255. CM_L4PER_I2C2_CLKCTRL

Address Offset	0x0000 09A8		
Physical Address	0x4A00 90A8	**Instance**	CORE_CM_CORE
Description	This register manages the I2C2 clocks.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1256. Register Call Summary for Register CM_L4PER_I2C2_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [1]

Table 3-1257. CM_L4PER_I2C3_CLKCTRL

Address Offset	0x0000 09B0		
Physical Address	0x4A00 90B0	**Instance**	CORE_CM_CORE
Description	This register manages the I2C3 clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1258. Register Call Summary for Register CM_L4PER_I2C3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1259. CM_L4PER_I2C4_CLKCTRL

Address Offset	0x0000 09B8		
Physical Address	0x4A00 90B8	**Instance**	CORE_CM_CORE
Description	This register manages the I2C4 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1260. Register Call Summary for Register CM_L4PER_I2C4_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1261. CM_L4PER_L4_PER_CLKCTRL

Address Offset	0x0000 09C0		
Physical Address	0x4A00 90C0	**Instance**	CORE_CM_CORE
Description	This register manages the L4_PER clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1262. Register Call Summary for Register CM_L4PER_L4_PER_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1263. CM_L4PER_MCSPI1_CLKCTRL

Address Offset	0x0000 09F0		
Physical Address	0x4A00 90F0	**Instance**	CORE_CM_CORE
Description	This register manages the MCSPI1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

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Table 3-1264. Register Call Summary for Register CM_L4PER_MCSPI1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1265. CM_L4PER_MCSPI2_CLKCTRL

Address Offset	0x0000 09F8		
Physical Address	0x4A00 90F8	**Instance**	CORE_CM_CORE
Description	This register manages the MCSPI2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1266. Register Call Summary for Register CM_L4PER_MCSPI2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

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Table 3-1267. CM_L4PER_MCSPI3_CLKCTRL

Address Offset	0x0000 0A00		
Physical Address	0x4A00 9100	**Instance**	CORE_CM_CORE
Description	This register manages the MCSPI3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1268. Register Call Summary for Register CM_L4PER_MCSPI3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1269. CM_L4PER_MCSPI4_CLKCTRL

Address Offset	0x0000 0A08		
Physical Address	0x4A00 9108	**Instance**	CORE_CM_CORE
Description	This register manages the MCSPI4 clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1270. Register Call Summary for Register CM_L4PER_MCSPI4_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1271. CM_L4PER_GPIO7_CLKCTRL

Address Offset	0x0000 0A10		
Physical Address	0x4A00 9110	**Instance**	CORE_CM_CORE
Description	This register manages the GPIO7 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1272. Register Call Summary for Register CM_L4PER_GPIO7_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1273. CM_L4PER_GPIO8_CLKCTRL

Address Offset	0x0000 0A18		
Physical Address	0x4A00 9118	**Instance**	CORE_CM_CORE
Description	This register manages the GPIO8 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED							OPTFCLKEN_DBCLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_DBCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1274. Register Call Summary for Register CM_L4PER_GPIO8_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1275. CM_L4PER_MMC3_CLKCTRL

Address Offset	0x0000 0A20		
Physical Address	0x4A00 9120	**Instance**	CORE_CM_CORE
Description	This register manages the MMC3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1276. Register Call Summary for Register CM_L4PER_MMC3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1277. CM_L4PER_MMC4_CLKCTRL

Address Offset	0x0000 0A28		
Physical Address	0x4A00 9128	**Instance**	CORE_CM_CORE
Description	This register manages the MMC4 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1278. Register Call Summary for Register CM_L4PER_MMC4_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1279. CM_L4PER_UART1_CLKCTRL

Address Offset	0x0000 0A40		
Physical Address	0x4A00 9140	**Instance**	CORE_CM_CORE
Description	This register manages the UART1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

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Table 3-1280. Register Call Summary for Register CM_L4PER_UART1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1281. CM_L4PER_UART2_CLKCTRL

Address Offset	0x0000 0A48		
Physical Address	0x4A00 9148	**Instance**	CORE_CM_CORE
Description	This register manages the UART2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1282. Register Call Summary for Register CM_L4PER_UART2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

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Table 3-1283. CM_L4PER_UART3_CLKCTRL

Address Offset	0x0000 0A50		
Physical Address	0x4A00 9150	**Instance**	CORE_CM_CORE
Description	This register manages the UART3 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1284. Register Call Summary for Register CM_L4PER_UART3_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [2]

Table 3-1285. CM_L4PER_UART4_CLKCTRL

Address Offset	0x0000 0A58		
Physical Address	0x4A00 9158	**Instance**	CORE_CM_CORE
Description	This register manages the UART4 clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1286. Register Call Summary for Register CM_L4PER_UART4_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1287. CM_L4PER_MMC5_CLKCTRL

Address Offset	0x0000 0A60		
Physical Address	0x4A00 9160	**Instance**	CORE_CM_CORE
Description	This register manages the MMC5 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1288. Register Call Summary for Register CM_L4PER_MMC5_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1289. CM_L4PER_I2C5_CLKCTRL

Address Offset	0x0000 0A68		
Physical Address	0x4A00 9168	**Instance**	CORE_CM_CORE
Description	This register manages the I2C5 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1290. Register Call Summary for Register CM_L4PER_I2C5_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1291. CM_L4PER_UART5_CLKCTRL

Address Offset	0x0000 0A70		
Physical Address	0x4A00 9170	**Instance**	CORE_CM_CORE
Description	This register manages the UART5 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

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Table 3-1292. Register Call Summary for Register CM_L4PER_UART5_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1293. CM_L4PER_UART6_CLKCTRL

Address Offset	0x0000 0A78		
Physical Address	0x4A00 9178	**Instance**	CORE_CM_CORE
Description	This register manages the UART6 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1294. Register Call Summary for Register CM_L4PER_UART6_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0]
PRCM Register Manual • CORE_CM_CORE Register Summary: [1]

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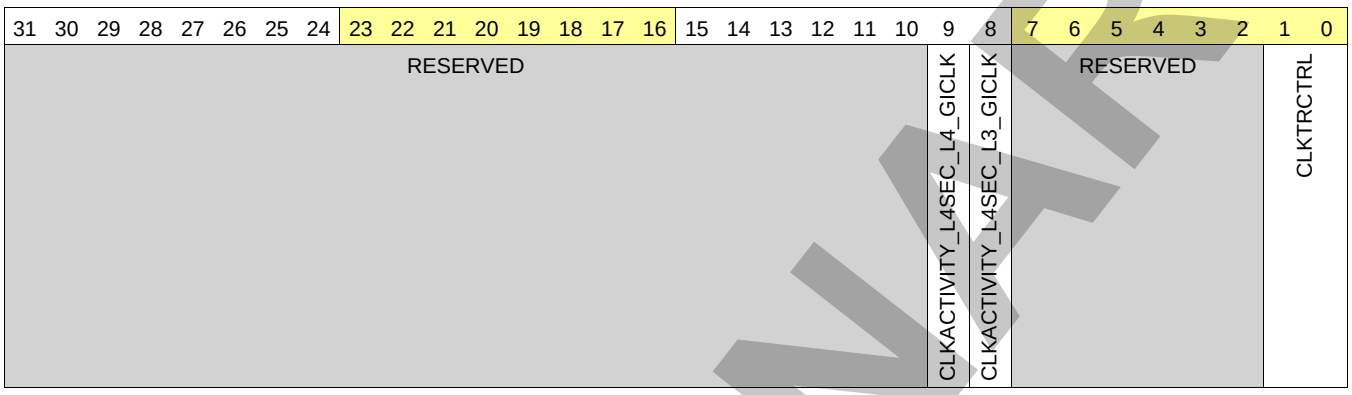
Table 3-1295. CM_L4SEC_CLKSTCTRL

Address Offset	0x0000 0A80		
Physical Address	0x4A00 9180	**Instance**	CORE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also hold one status bit per clock input of the domain.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00 0000
9	CLKACTIVITY_L4SEC_L4_GICLK	This field indicates the state of the L4_SECURE_GICLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
8	CLKACTIVITY_L4SEC_L3_GICLK	This field indicates the state of the L3_SECURE_GICLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L4SEC clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain.	RW	0x3

Table 3-1296. Register Call Summary for Register CM_L4SEC_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1] [2]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [3]

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Table 3-1297. CM_L4SEC_STATICDEP

Address Offset	0x0000 0A84		
Physical Address	0x4A00 9184	**Instance**	CORE_CM_CORE
Description	This register controls the static domain depedencies from L4SEC domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		L4PER_STATDEP	RESERVED						L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	RESERVED				

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x0 0000
13	L4PER_STATDEP	Static dependency towards L4PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12:7	RESERVED		R	0x00
6	L3MAIN2_STATDEP	Static dependency towards L3MAIN2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3MAIN1_STATDEP	Static dependency towards L3MAIN1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3:0	RESERVED		R	0x0

Table 3-1298. Register Call Summary for Register CM_L4SEC_STATICDEP

Clock Management Functional Description
- Static Dependency: [0] [1] [2] [3]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [4]

Table 3-1299. CM_L4SEC_DYNAMICDEP

Address Offset	0x0000 0A88		
Physical Address	0x4A00 9188	**Instance**	CORE_CM_CORE
Description	This register controls the dynamic domain depedencies from L4SEC domain towards 'target' domains. It is relevant only for domain having OCP master port(s).		
Type	R		

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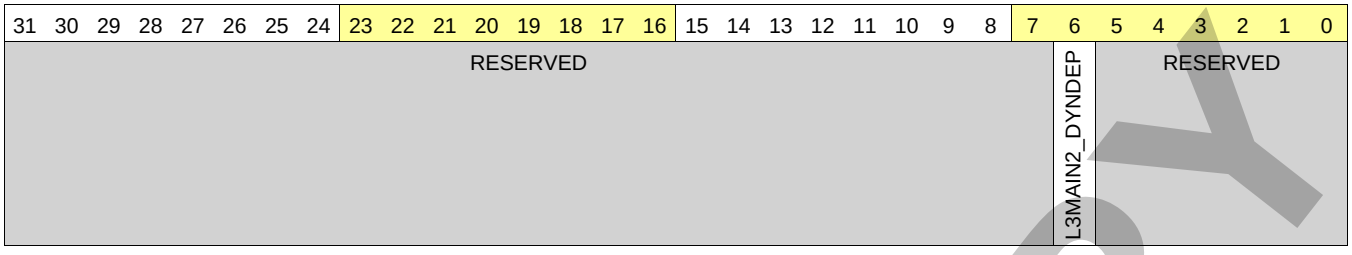


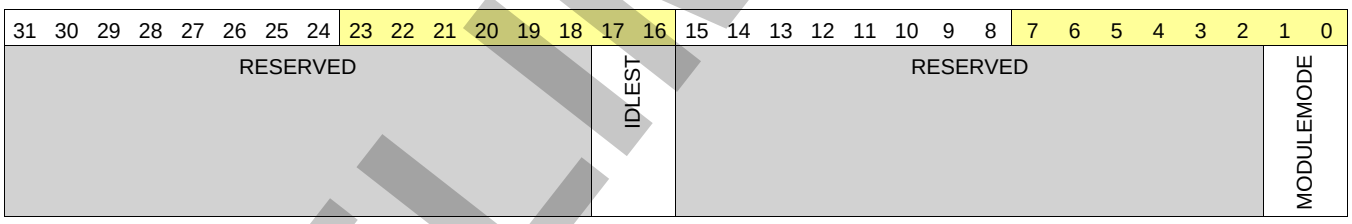
Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3MAIN2 clock domain Read 0x0: Dependency is disabled	R	0
5:0	RESERVED		R	0x00

Table 3-1300. Register Call Summary for Register CM_L4SEC_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [0]
PRCM Register Manual • CORE_CM_CORE Register Summary: [1]

Table 3-1301. CM_L4SEC_AES1_CLKCTRL

Address Offset	0x0000 0AA0		
Physical Address	0x4A00 91A0	**Instance**	CORE_CM_CORE
Description	This register manages the AES1 clocks.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any INTERCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1302. Register Call Summary for Register CM_L4SEC_AES1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1303. CM_L4SEC_AES2_CLKCTRL

Address Offset	0x0000 0AA8		
Physical Address	0x4A00 91A8	**Instance**	CORE_CM_CORE
Description	This register manages the AES2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including INTERCONN	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any INTERCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any INTERCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1304. Register Call Summary for Register CM_L4SEC_AES2_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1305. CM_L4SEC_DES3DES_CLKCTRL

Address Offset	0x0000 0AB0		
Physical Address	0x4A00 91B0	**Instance**	CORE_CM_CORE
Description	This register manages the DES3DES clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1306. Register Call Summary for Register CM_L4SEC_DES3DES_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1307. CM_L4SEC_FPKA_CLKCTRL

Address Offset	0x0000 0AB8		
Physical Address	0x4A00 91B8	**Instance**	CORE_CM_CORE
Description	This register manages the FPKA clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

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Table 3-1308. Register Call Summary for Register CM_L4SEC_FPKA_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

Table 3-1309. CM_L4SEC_RNG_CLKCTRL

Address Offset	0x0000 0AC0		
Physical Address	0x4A00 91C0	**Instance**	CORE_CM_CORE
Description	This register manages the RNG clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1310. Register Call Summary for Register CM_L4SEC_RNG_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CORE_CM_CORE Register Summary: [2]

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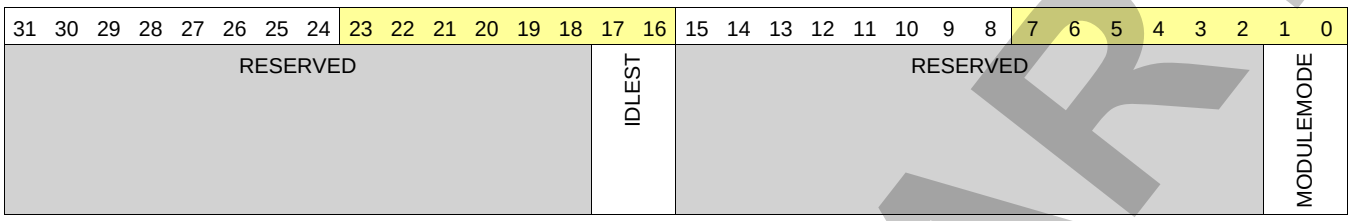
Table 3-1311. CM_L4SEC_SHA2MD5_CLKCTRL

Address Offset	0x0000 0AC8		
Physical Address	0x4A00 91C8	**Instance**	CORE_CM_CORE
Description	This register manages the SHA2MD5 clocks.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1312. Register Call Summary for Register CM_L4SEC_SHA2MD5_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- CORE_CM_CORE Register Summary: [2]

Table 3-1313. CM_L4SEC_DMA_CRYPTO_CLKCTRL

Address Offset	0x0000 0AD8		
Physical Address	0x4A00 91D8	**Instance**	CORE_CM_CORE
Description	This register manages the DMA_CRYPTO clocks.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x1: Module is in standby Read 0x0: Module is functional (not in standby)	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CLKTRCTRL=3, any OCP access to module is always granted. Module clocks may be gated according to the clock domain state.	R Rreturns	0x1

Table 3-1314. Register Call Summary for Register CM_L4SEC_DMA_CRYPTO_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2]
PRCM Register Manual • CORE_CM_CORE Register Summary: [3]

3.11.33 IVA_CM_CORE Registers

3.11.33.1 IVA_CM_CORE Register Summary

Table 3-1315. IVA_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	IVA_CM_CORE Base Address
CM_IVA_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9200
CM_IVA_STATICDEP	RW	32	0x0000 0004	0x4A00 9204
CM_IVA_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9208
CM_IVA_IVA_CLKCTRL	RW	32	0x0000 0020	0x4A00 9220
CM_IVA_SL2_CLKCTRL	RW	32	0x0000 0028	0x4A00 9228

3.11.33.2 IVA_CM_CORE Register Description

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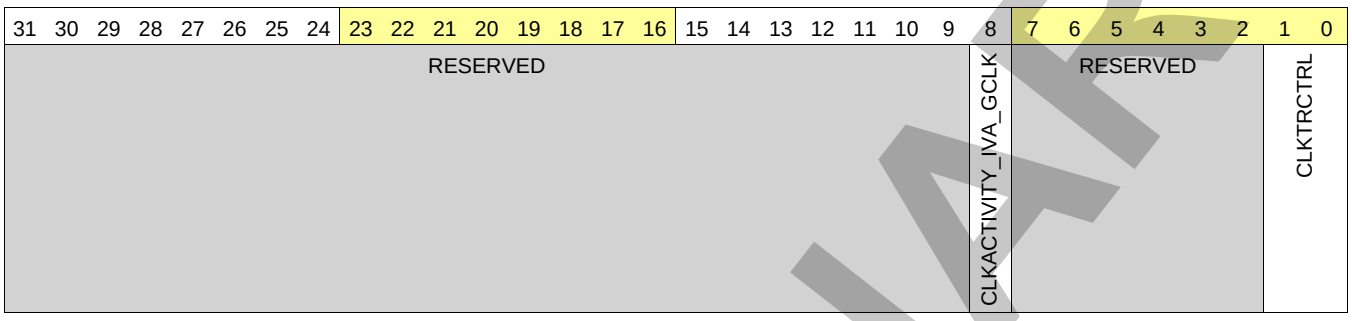
Table 3-1316. CM_IVA_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9200	**Instance**	IVA_CM_CORE
Description	This register enables the IVA domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	CLKACTIVITY_IVA_GCLK	This field indicates the state of the IVA_GCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the IVA clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1317. Register Call Summary for Register CM_IVA_CLKSTCTRL

Reset Management Functional Description
- IVA Subsystem Software Warm Reset Sequence: [0]

Clock Management Functional Description
- Clock Domain Modes: [1] [2]

PRCM Register Manual
- IVA_CM_CORE Register Summary: [3]
- IVA_CM_CORE Register Description: [4] [5]

Table 3-1318. CM_IVA_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9204	**Instance**	IVA_CM_CORE
Description	This register controls the static domain depedencies from IVA domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	RESERVED				

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_STATDEP	Static dependency towards L3_MAIN2 clock domain Read 0x1: Dependency is enabled	R	1
5	L3MAIN1_STATDEP	Static dependency towards L3_MAIN1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3:0	RESERVED		R	0x0

Table 3-1319. Register Call Summary for Register CM_IVA_STATICDEP

Clock Management Functional Description • Static Dependency: [0] [1] [2]
PRCM Register Manual • IVA_CM_CORE Register Summary: [3]

Table 3-1320. CM_IVA_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9208	**Instance**	IVA_CM_CORE
Description	This register controls the dynamic domain depedencies from IVA domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									L3_MAIN2_DYNDEP	RESERVED					

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3_MAIN2 clock domain Read 0x0: Dependency is disabled	R	0
5:0	RESERVED		R	0x00

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Table 3-1321. Register Call Summary for Register CM_IVA_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [0]
PRCM Register Manual • IVA_CM_CORE Register Summary: [1]

Table 3-1322. CM_IVA_IVA_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9220	**Instance**	IVA_CM_CORE
Description	This register manages the IVA clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_IVA_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1323. Register Call Summary for Register CM_IVA_IVA_CLKCTRL

Reset Management Functional Description • IVA Subsystem Software Warm Reset Sequence: [0] [1]
Clock Management Functional Description • Clock Domain Module Attributes: [2] [3] [4]

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Table 3-1323. Register Call Summary for Register CM_IVA_IVA_CLKCTRL (continued)

PRCM Register Manual
- IVA_CM_CORE Register Summary: [5]

Table 3-1324. CM_IVA_SL2_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 9228	**Instance**	IVA_CM_CORE
Description	This register manages the SL2 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_IVA_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any INTRCONN access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1325. Register Call Summary for Register CM_IVA_SL2_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1]

PRCM Register Manual
- IVA_CM_CORE Register Summary: [2]

3.11.34 CAM_CM_CORE Registers

3.11.34.1 CAM_CM_CORE Register Summary

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Table 3-1326. CAM_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CAM_CM_CORE Base Address
CM_CAM_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9300
CM_CAM_STATICDEP	RW	32	0x0000 0004	0x4A00 9304
CM_CAM_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9308
CM_CAM_ISS_CLKCTRL	RW	32	0x0000 0020	0x4A00 9320
CM_CAM_FDIF_CLKCTRL	RW	32	0x0000 0028	0x4A00 9328
RESERVED	R	32	0x0000 0030	0x4A00 9330

3.11.34.2 CAM_CM_CORE Register Description

Table 3-1327. CM_CAM_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9300	**Instance**	CAM_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			CLKACTIVITY_CAM_L3_GICLK	CLKACTIVITY_CAM_BOOST_GCLK	CLKACTIVITY_FDIF_GCLK	CLKACTIVITY_CSI_PHY_GFCLK	CLKACTIVITY_CAM_GCLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x000000
12	CLKACTIVITY_CAM_L3_GICLK	This field indicates the state of the CAM_L3_GICLK clock input of the domain. [warm reset insensitive] read 0x0: Corresponding clock is definitely gated read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0x000000
11	CLKACTIVITY_CAM_BOOST_GCLK	This field indicates the state of the CAM_BOOST_GCLK clock input of the domain. [warm reset insensitive] read 0x0: Corresponding clock is definitely gated read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0x000000
10	CLKACTIVITY_FDIF_GCLK	This field indicates the state of the FDIF_GCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0

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Bits	Field Name	Description	Type	Reset
9	CLKACTIVITY_CSI_PHY_GFCLK	This field indicates the state of the CSI_PHY_GFCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
8	CLKACTIVITY_CAM_GCLK	This field indicates the state of the CAM_GCLK clock input of the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the CAM clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1328. Register Call Summary for Register CM_CAM_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] [4] [5]
PRCM Register Manual • CAM_CM_CORE Register Summary: [6]

Table 3-1329. CM_CAM_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9304	**Instance**	CAM_CM_CORE
Description	This register controls the static domain depedencies from CAM domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	RESERVED	IVA_STATDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_STATDEP	Static dependency towards L3_MAIN2 clock domain Read 0x1: Dependency is enabled	R	1
5	L3MAIN1_STATDEP	Static dependency towards L3_MAIN1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	RESERVED		R	0
2	IVA_STATDEP	Static dependency towards IVA clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1330. Register Call Summary for Register CM_CAM_STATICDEP

Clock Management Functional Description • Static Dependency: [0] [1] [2] [3]
PRCM Register Manual • CAM_CM_CORE Register Summary: [4]

Table 3-1331. CM_CAM_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9308	**Instance**	CAM_CM_CORE
Description	This register controls the dynamic domain depedencies from CAM domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									L3MAIN2_DYNDEP	RESERVED					

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3_MAIN2 clock domain Read 0x0: Dependency is disabled	R	0
5:0	RESERVED		R	0x00

Table 3-1332. Register Call Summary for Register CM_CAM_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [0]
PRCM Register Manual • CAM_CM_CORE Register Summary: [1]

Table 3-1333. CM_CAM_ISS_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9320	**Instance**	CAM_CM_CORE
Description	This register manages the ISS clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED							OPTFCLKEN_CTRLCLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_CTRLCLK	Optional functional clock control for CSI_PHY_GFCLK 96Mhz clock. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1334. Register Call Summary for Register CM_CAM_ISS_CLKCTRL

Clock Management Functional Description
- Clock Domain Modes: [0]
- Clock Domain Module Attributes: [1] [2] [3]

PRCM Register Manual
- CAM_CM_CORE Register Summary: [4]

Table 3-1335. CM_CAM_FDIF_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 9328	**Instance**	CAM_CM_CORE
Description	This register manages the FDIF clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL_FCLK	RESERVED					STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL_FCLK	Select the ration of FDIF_FCLK to FUNC_256M_CLK 0x0: FDIF_CLK is divide by 1 of FUNC_256M_CLK, to be used for OPP_NOM 0x1: FDIF_CLK is divide by 2 of FUNC_256M_CLK, to be used for OPP_LOW	RW	0x0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guaranteed to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1336. Register Call Summary for Register CM_CAM_FDIF_CLKCTRL

Clock Management Functional Description
- CM_CORE Clock Generator: [0]
- Clock Domain Modes: [1]
- Clock Domain Module Attributes: [2] [3] [4]

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- CAM_CM_CORE Register Summary: [5]

3.11.35 DSS_CM_CORE Registers

3.11.35.1 DSS_CM_CORE Register Summary

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Table 3-1337. DSS_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS_CM_CORE Base Address
CM_DSS_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9400
CM_DSS_STATICDEP	RW	32	0x0000 0004	0x4A00 9404
CM_DSS_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9408
CM_DSS_DSS_CLKCTRL	RW	32	0x0000 0020	0x4A00 9420
CM_DSS_BB2D_CLKCTRL	RW	32	0x0000 0030	0x4A00 9430

3.11.35.2 DSS_CM_CORE Register Description

Table 3-1338. CM_DSS_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9400	**Instance**	DSS_CM_CORE
Description	This register enables the DSS domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		CLKACTIVITY_BB2D_GFCLK	CLKACTIVITY_HDMI_CEC_GFCLK	CLKACTIVITY_HDMI_PHY_GFCLK	CLKACTIVITY_DSS_SYS_GFCLK	CLKACTIVITY_DSS_GFCLK	CLKACTIVITY_DSS_L3_GICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x0
13	CLKACTIVITY_BB2D_GFCLK	This field indicates the state of the BB2D_GFCLK clock in the domain. [warm reset insesitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
12	CLKACTIVITY_HDMI_CEC_GFCLK	This field indicates the state of the HDMI_CEC_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
11	CLKACTIVITY_HDMI_PHY_GFCLK	This field indicates the state of the HDMI_PHY_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
10	CLKACTIVITY_DSS_SYS_GFCLK	This field indicates the state of the DSS_SYS_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0

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Bits	Field Name	Description	Type	Reset
9	CLKACTIVITY_DSS_GFCLK	This field indicates the state of the DSS_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
8	CLKACTIVITY_DSS_L3_GICLK	This field indicates the state of the DSS_L3_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the DSS clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1339. Register Call Summary for Register CM_DSS_CLKSTCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] [4] [5] [6]
PRCM Register Manual • DSS_CM_CORE Register Summary: [7]

Table 3-1340. CM_DSS_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9404	**Instance**	DSS_CM_CORE
Description	This register controls the static domain depedencies from DSS domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	RESERVED	IVA_STATDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_STATDEP	Static dependency towards L3_MAIN2 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	1
5	L3MAIN1_STATDEP	Static dependency towards L3_MAIN1 clock domain Read 0x1: Dependency is enabled	R Returns 1s	1

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Bits	Field Name	Description	Type	Reset
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	RESERVED		R	0
2	IVA_STATDEP	Static dependency towards IVA clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1341. Register Call Summary for Register CM_DSS_STATICDEP

Clock Management Functional Description • Static Dependency: [0] [1] [2] [3]
PRCM Register Manual • DSS_CM_CORE Register Summary: [4]

Table 3-1342. CM_DSS_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9408	**Instance**	DSS_CM_CORE
Description	This register controls the dynamic domain depedencies from DSS domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L3MAIN2_DYNDEP	L3MAIN1_DYNDEP	RESERVED					

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3_MAIN2 domain Read 0x0: Dependency is disabled	R	0
5	L3MAIN1_DYNDEP	Dynamic dependency towards L3_MAIN1 domain Read 0x0: Dependency is disabled	R	0
4:0	RESERVED		R	0x00

Table 3-1343. Register Call Summary for Register CM_DSS_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [0] [1]
PRCM Register Manual • DSS_CM_CORE Register Summary: [2]

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Table 3-1344. CM_DSS_DSS_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9420	**Instance**	DSS_CM_CORE
Description	This register manages the DSS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED				OPTFCLKEN_32KHZ_CLK	OPTFCLKEN_SYS_CLK	OPTFCLKEN_48MHZ_CLK	OPTFCLKEN_DSSCLK	RESERVED							MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Reserved	R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:12	RESERVED	Reserved	R	0x0
11	OPTFCLKEN_32KHZ_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
10	OPTFCLKEN_SYS_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
9	OPTFCLKEN_48MHZ_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_DSSCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED	Reserved	R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1345. Register Call Summary for Register CM_DSS_DSS_CLKCTRL

Clock Management Functional Description • Clock Domain Modes: [0] [1] [2] [3] • Clock Domain Module Attributes: [4] [5] [6]
PRCM Register Manual • DSS_CM_CORE Register Summary: [7]

Table 3-1346. CM_DSS_BB2D_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4A00 9430	**Instance**	DSS_CM_CORE
Description	This register manages the DSS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Reserved	R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1347. Register Call Summary for Register CM_DSS_BB2D_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2]
PRCM Register Manual • DSS_CM_CORE Register Summary: [3]

3.11.36 GPU_CM_CORE Registers

3.11.36.1 GPU_CM_CORE Register Summary

Table 3-1348. GPU_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPU_CM_CORE Base Address
CM_GPU_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9500
CM_GPU_STATICDEP	RW	32	0x0000 0004	0x4A00 9504
CM_GPU_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9508
CM_GPU_GPU_CLKCTRL	RW	32	0x0000 0020	0x4A00 9520

3.11.36.2 GPU_CM_CORE Register Description

Table 3-1349. CM_GPU_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9500	**Instance**	GPU_CM_CORE
Description	This register enables the GPU domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					CLKACTIVITY_GPU_HYD_GCLK	CLKACTIVITY_GPU_CORE_GCLK	CLKACTIVITY_GPU_L3_GICLK	RESERVED						CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	CLKACTIVITY_GPU_HYD_GCLK	This field indicates the state of the GPU_HYD_GCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
9	CLKACTIVITY_GPU_CORE_GCLK	This field indicates the state of the GPU_CORE_GCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
8	CLKACTIVITY_GPU_L3_GICLK	This field indicates the state of the GPU_L3_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the GPU clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x3

Table 3-1350. Register Call Summary for Register CM_GPU_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1] [2] [3]

PRCM Register Manual
- GPU_CM_CORE Register Summary: [4]

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Table 3-1351. CM_GPU_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9504	**Instance**	GPU_CM_CORE
Description	This register controls the static domain depedencies from GPU domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	RESERVED	IVA_STATDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_STATDEP	Static dependency towards L3_MAIN2 clock domain Read 0x1: Dependency is enabled	R Rreturns 1s	1
5	L3MAIN1_STATDEP	Static dependency towards L3_MAIN1 clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	RESERVED		R	0
2	IVA_STATDEP	Static dependency towards IVA clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1352. Register Call Summary for Register CM_GPU_STATICDEP

Clock Management Functional Description
- Static Dependency: [0] [1] [2] [3]

PRCM Register Manual
- GPU_CM_CORE Register Summary: [4]

Table 3-1353. CM_GPU_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9508	**Instance**	GPU_CM_CORE
Description	This register controls the dynamic domain depedencies from GPU domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

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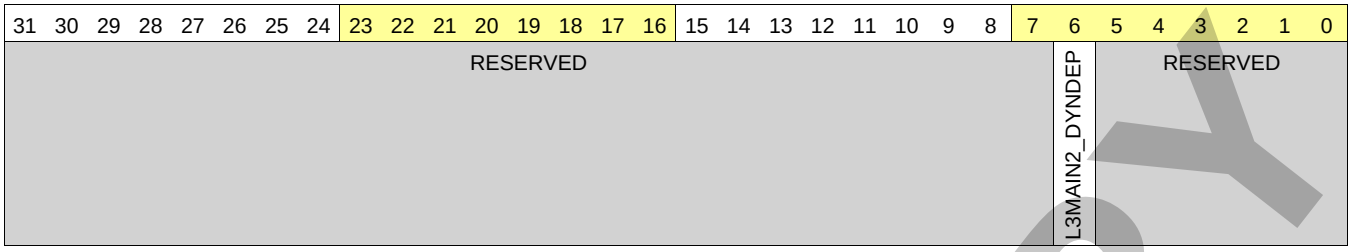


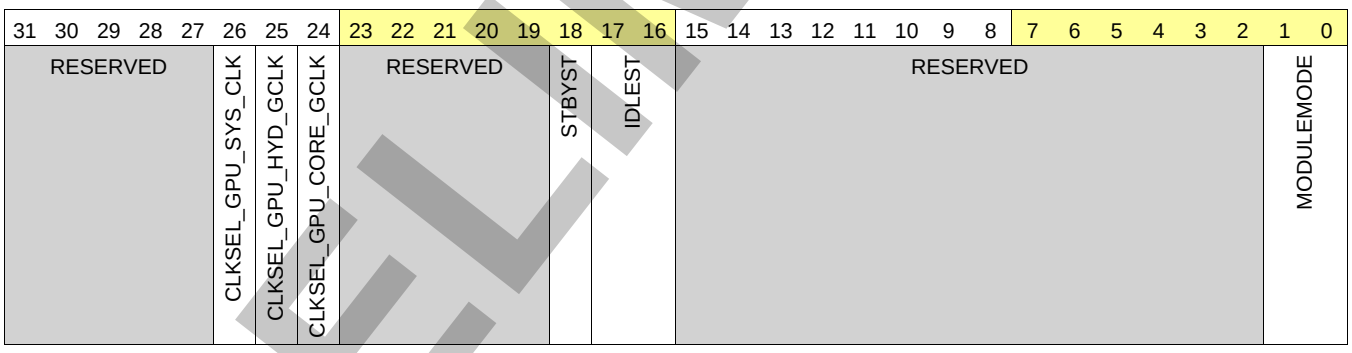
Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3_MAIN2 clock domain Read 0x0: Dependency is disabled	R	0
5:0	RESERVED		R	0x00

Table 3-1354. Register Call Summary for Register CM_GPU_DYNAMICDEP

Clock Management Functional Description • Dynamic Dependency: [0]
PRCM Register Manual • GPU_CM_CORE Register Summary: [1]

Table 3-1355. CM_GPU_GPU_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9520	**Instance**	GPU_CM_CORE
Description	This register manages the GPU clocks.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	CLKSEL_GPU_SYS_CLK	Select the ratio of GPU_L3_GICLK (SYS_CLK) to L3_ICLK 0x0: GPU_L3_ICLK (SYS_CLK) is divide by 1 of L3_ICLK 0x1: GPU_L3_ICLK (SYS_CLK) is divide by 2 of L3_ICLK	RW	0
25	CLKSEL_GPU_HYD_GCLK	Select the source of GPU_HYD_GCLK 0x0: Functional clock is sourced from DPLL_CORE HSDIVIDER 0x1: Functional clock is sourced from DPLL_PER HSDIVIDER	RW	0

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Bits	Field Name	Description	Type	Reset
24	CLKSEL_GPU_CORE_GCLK	Select the source of GPU_CORE_GCLK 0x0: Functional clock is sourced from DPLL_CORE HSDIVIDER 0x1: Functional clock is sourced from DPLL_PER HSDIVIDER	RW	0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guaranteed to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1356. Register Call Summary for Register CM_GPU_GPU_CLKCTRL

Clock Management Functional Description
- CM_CORE Clock Generator: [0] [1] [2] [3]
- Clock Domain Modes: [4] [5] [6]
- Clock Domain Module Attributes: [7] [8] [9]

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- GPU_CM_CORE Register Summary: [10]

3.11.37 L3INIT_CM_CORE Registers

3.11.37.1 L3INIT_CM_CORE Register Summary

Table 3-1357. L3INIT_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_CM_CORE Base Address
CM_L3INIT_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9600
CM_L3INIT_STATICDEP	RW	32	0x0000 0004	0x4A00 9604
CM_L3INIT_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9608
CM_L3INIT_MMC1_CLKCTRL	RW	32	0x0000 0028	0x4A00 9628
CM_L3INIT_MMC2_CLKCTRL	RW	32	0x0000 0030	0x4A00 9630
CM_L3INIT_HSI_CLKCTRL	RW	32	0x0000 0038	0x4A00 9638
RESERVED	R	32	0x0000 0040	0x4A00 9640

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Table 3-1357. L3INIT_CM_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_CM_CORE Base Address
RESERVED	R	32	0x0000 0048	0x4A00 9648
CM_L3INIT_USB_HOST_HS_CLKCTRL	RW	32	0x0000 0058	0x4A00 9658
CM_L3INIT_USB_TLL_HS_CLKCTRL	RW	32	0x0000 0068	0x4A00 9668
CM_L3INIT_IEEE1500_2_OCP_CLKCTRL	R	32	0x0000 0078	0x4A00 9678
CM_L3INIT_SATA_CLKCTRL	RW	32	0x0000 0088	0x4A00 9688
CM_L3INIT_OCP2SCP1_CLKCTRL	RW	32	0x0000 00E0	0x4A00 96E0
CM_L3INIT_OCP2SCP3_CLKCTRL	RW	32	0x0000 00E8	0x4A00 96E8
CM_L3INIT_USB_OTG_SS_CLKCTRL	RW	32	0x0000 00F0	0x4A00 96F0

3.11.37.2 L3INIT_CM_CORE Register Description

Table 3-1358. CM_L3INIT_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9600	**Instance**	L3INIT_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds one status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKACTIVITY_USB_OTG_SS_REF_CLK	CLKACTIVITY_UTMI_P3_GFCLK	CLKACTIVITY_L3INIT_60M_P2_GFCLK	CLKACTIVITY_L3INIT_60M_P1_GFCLK	CLKACTIVITY_HSIC_P2_GFCLK	CLKACTIVITY_HSIC_P1_GFCLK	CLKACTIVITY_UTMI_ROOT_GFCLK	CLKACTIVITY_TLL_CH2_GFCLK	CLKACTIVITY_TLL_CH1_GFCLK	CLKACTIVITY_TLL_CH0_GFCLK	CLKACTIVITY_HSIC_P2_480M_GFCLK	CLKACTIVITY_HSIC_P1_480M_GFCLK	CLKACTIVITY_SATA_REF_GFCLK	CLKACTIVITY_MMC2_GFCLK	CLKACTIVITY_MMC1_GFCLK	CLKACTIVITY_HSI_GFCLK	CLKACTIVITY_USB_DPLL_HS_CLK	CLKACTIVITY_USB_DPLL_CLK	RESERVED	CLKACTIVITY_L3INIT_48M_GFCLK	CLKACTIVITY_L3INIT_USB_OTG_SS_LFPS_TX_GFCLK	RESERVED	CLKACTIVITY_L3INIT_L4_GICLK	CLKACTIVITY_L3INIT_L3_GICLK	CLKACTIVITY_HSIC_P3_GFCLK	CLKACTIVITY_HSIC_P3_480M_GFCLK	RESERVED	CLKACTIVITY_PAD_XCLK60MHSP2	RESERVED	CLKACTIVITY_MMC1_32K_GFCLK	CLKTRCTRL

Bits	Field Name	Description	Type	Reset
31	CLKACTIVITY_USB_OTG_SS_REF_CLK	This field indicates the state of the USB_OTG_SS_REF_CLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0

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Bits	Field Name	Description	Type	Reset
30	CLKACTIVITY_UTMI_P3_GFCLK	This field indicates the state of the UTMI_P3_GFCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
29	CLKACTIVITY_L3INIT_60M_P2_GFCLK	This field indicates the state of the INIT_60M_P2_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
28	CLKACTIVITY_L3INIT_60M_P1_GFCLK	This field indicates the state of the INIT_60M_P1_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
27	CLKACTIVITY_HSIC_P2_GFCLK	This field indicates the state of the HSIC_P2_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
26	CLKACTIVITY_HSIC_P1_GFCLK	This field indicates the state of the HSIC_P1_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
25	CLKACTIVITY_UTMI_ROOT_GFCLK	This field indicates the state of the UTMI_ROOT_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
24	CLKACTIVITY_TLL_CH2_GFCLK	This field indicates the state of the TLL_CH2_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
23	CLKACTIVITY_TLL_CH1_GFCLK	This field indicates the state of the TLL_CH1_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
22	CLKACTIVITY_TLL_CH0_GFCLK	This field indicates the state of the TLL_CH0_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
21	CLKACTIVITY_HSIC_P2_480M_GFCLK	This field indicates the state of the HSIC_P2_480M_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0

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Bits	Field Name	Description	Type	Reset
20	CLKACTIVITY_HSIC_P1_480M_GFCLK	This field indicates the state of the HSIC_P1_480M_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
19	CLKACTIVITY_SATA_REF_GFCLK	This field indicates the state of the SATA_REF_GFCLK clock in the domain. [warm reset insensitive] read 0x0: Corresponding clock is definitely gated read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
18	CLKACTIVITY_MMC2_GFCLK	This field indicates the state of the MMC2_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
17	CLKACTIVITY_MMC1_GFCLK	This field indicates the state of the MMC1_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
16	CLKACTIVITY_HSI_GFCLK	This field indicates the state of the HSI_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
15	CLKACTIVITY_USB_DPLL_HS_CLK	This field indicates the state of the USB_DPLL_HS_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
14	CLKACTIVITY_USB_DPLL_CLK	This field indicates the state of the USB_DPLL_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
13	RESERVED	Reserved	R	0
12	CLKACTIVITY_L3INIT_48M_GFCLK	This field indicates the state of the L3INIT_48M_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
11	CLKACTIVITY_L3INIT_USB_OTG_SS_LFPS_TX_GFCLK	This field indicates the state of the L3INIT_USB_OTG_SS_LFPS_TX_GFCLK clock in the domain.[warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
10	RESERVED	Reserved	R	0
9	CLKACTIVITY_L3INIT_L4_GICLK	This field indicates the state of the L3INIT_L4_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0

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Bits	Field Name	Description	Type	Reset
8	CLKACTIVITY_L3INIT_L3_GICLK	This field indicates the state of the L3INIT_L3_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7	CLKACTIVITY_HSIC_P3_GFCLK	This field indicates the state of the HSIC_P3_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
6	CLKACTIVITY_HSIC_P3_480M_GFCLK	This field indicates the state of the HSIC_P3_480M_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
5	RESERVED	Reserved	R	0
4	CLKACTIVITY_PAD_XCLK60MHSP2	This field indicates the state of the XCLK60MHSP2 clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
3	RESERVED	Reserved	R	0
2	CLKACTIVITY_MMC1_32K_GFCLK	This field indicates the state of the MMC1_32K_GFCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
1:0	CLKTRCTRL	Controls the clock state transition of the L3INIT clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep transition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3-1359. Register Call Summary for Register CM_L3INIT_CLKSTCTRL

Clock Management Functional Description

- Clock Domain Modes: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26]

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- L3INIT_CM_CORE Register Summary: [27]
- L3INIT_CM_CORE Register Description: [28] [29] [30] [31]

Table 3-1360. CM_L3INIT_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9604	**Instance**	L3INIT_CM_CORE
Description	This register controls the static domain dependencies from L3INIT domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																WKUPAON_STATDEP	L4SEC_STATDEP	L4PER_STATDEP	L4CFG_STATDEP	RESERVED				L3MAIN2_STATDEP	L3MAIN1_STATDEP	EMIF_STATDEP	ABE_STATDEP	IVA_STATDEP	RESERVED		

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	WKUPAON_STATDEP	Static dependency towards WKUPAON clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
14	L4SEC_STATDEP	Static dependency towards L4SEC clock domain 0: Dependency is disabled 1: Dependency is enabled	RW	0
13	L4PER_STATDEP	Static dependency towards L4_PER clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	L4CFG_STATDEP	Static dependency towards L4_CFG clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
11:7	RESERVED		R	0x00
6	L3MAIN2_STATDEP	Static dependency towards L3_MAIN2 clock domain Read 0x1: Dependency is enabled	R	1
5	L3MAIN1_STATDEP	Static dependency towards L3_MAIN1 clock domain Read 0x1: Dependency is enabled	R	1
4	EMIF_STATDEP	Static dependency towards EMIF clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	ABE_STATDEP	Static dependency towards ABE clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	IVA_STATDEP	Static dependency towards IVA clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3-1361. Register Call Summary for Register CM_L3INIT_STATICDEP

Clock Management Functional Description
- Static Dependency: [0] [1] [2] [3] [4] [5] [6] [7] [8]

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- L3INIT_CM_CORE Register Summary: [9]

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Table 3-1362. CM_L3INIT_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9608	**Instance**	L3INIT_CM_CORE
Description	This register controls the dynamic domain depedencies from L3INIT domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									L3MAIN2_DYNDEP	L3MAIN1_DYNDEP	RESERVED				

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6	L3MAIN2_DYNDEP	Dynamic dependency towards L3_MAIN2 clock domain Read 0x0: Dependency is disabled	R	0
5	L3MAIN1_DYNDEP	Dynamic dependency towards L3_MAIN1 clock domain Read 0x0: Dependency is disabled	R	0
4:0	RESERVED		R	0x00

Table 3-1363. Register Call Summary for Register CM_L3INIT_DYNAMICDEP

Clock Management Functional Description
- Dynamic Dependency: [0] [1]

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- L3INIT_CM_CORE Register Summary: [2]

Table 3-1364. CM_L3INIT_MMC1_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 9628	**Instance**	L3INIT_CM_CORE
Description	This register manages the MMC1 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKSEL_DIV	CLKSEL_SOURCE	RESERVED					STBYST	IDLEST		RESERVED							OPTFCLKEN_32KHZ_CLK	RESERVED						MODULEMODE	

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Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	CLKSEL_DIV	MMC1 clock divide ratio 0x0: MMC1 clock is divided by 1, to be used for OPP_NOM. 0x1: MMC1 clock is divided by 2	RW	0x0
24	CLKSEL_SOURCE	Selects the source of the functional clock. 0x0: 128MHz clock derived from DPLL_PER is selected 0x1: 192MHz clock derived from DPLL_PER is selected	RW	1
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00
8	OPTFCLKEN_32KHZ_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1365. Register Call Summary for Register CM_L3INIT_MMC1_CLKCTRL

Clock Management Functional Description

- PRM Clock Source: [0]
- CM_CORE Clock Generator: [1] [2]
- Clock Domain Modes: [3]
- Clock Domain Module Attributes: [4] [5] [6]

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- L3INIT_CM_CORE Register Summary: [7]

Table 3-1366. CM_L3INIT_MMC2_CLKCTRL

Address Offset	0x0000 0030		
Physical Address	0x4A00 9630	**Instance**	L3INIT_CM_CORE
Description	This register manages the MMC2 clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKSEL_DIV	CLKSEL_SOURCE	RESERVED					STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	CLKSEL_DIV	MMC2 clock divide ratio 0x0: MMC2 clock is divided by 1, to be used for OPP_NOM. 0x1: MMC2 clock is divided by 2	RW	0x0
24	CLKSEL_SOURCE	Selects the source of the functional clock. 0x0: 128MHz clock derived from DPLL_PER is selected 0x1: 192MHz clock derived from DPLL_PER is selected	RW	1
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guaranteed to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1367. Register Call Summary for Register CM_L3INIT_MMC2_CLKCTRL

Clock Management Functional Description
- CM_CORE Clock Generator: [0] [1]
- Clock Domain Module Attributes: [2] [3] [4]

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- L3INIT_CM_CORE Register Summary: [5]

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Table 3-1368. CM_L3INIT_HSI_CLKCTRL

Address Offset	0x0000 0038		
Physical Address	0x4A00 9638	**Instance**	L3INIT_CM_CORE
Description	This register manages the HSI clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLKSEL	RESERVED					STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects the functional clock source. 0x0: HSI_FCLK is divide by 1 of 192MHz clock, to be used for OPP_NOM 0x1: HSI_FCLK is divide by 2 of 192MHz clock	RW	0x0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED	Reserved	R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain Read 0x: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1369. Register Call Summary for Register CM_L3INIT_HSI_CLKCTRL

Clock Management Functional Description
- CM_CORE Clock Generator: [0]
- Clock Domain Module Attributes: [1] [2] [3]

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- L3INIT_CM_CORE Register Summary: [4]

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Table 3-1370. CM_L3INIT_USB_HOST_HS_CLKCTRL

Address Offset	0x0000 0058		
Physical Address	0x4A00 9658	**Instance**	L3INIT_CM_CORE
Description	This register manages the USB_HOST_HS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKSEL_UTMI_P2	CLKSEL_UTMI_P1	RESERVED					STBYST	IDLEST		OPTFCLKEN_FUNC48M_CLK	OPTFCLKEN_HSIC480M_P2_CLK	OPTFCLKEN_HSIC480M_P1_CLK	OPTFCLKEN_HSIC60M_P2_CLK	OPTFCLKEN_HSIC60M_P1_CLK	OPTFCLKEN_UTMI_P3_CLK	OPTFCLKEN_UTMI_P2_CLK	OPTFCLKEN_UTMI_P1_CLK	OPTFCLKEN_HSIC480M_P3_CLK	OPTFCLKEN_HSIC60M_P3_CLK	RESERVED	SAR_MODE	RESERVED		MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25	CLKSEL_UTMI_P2	Selects the source of the functional clock for UTMI Port2 on USB_HOST_HS 0x0: The functional clock is provided by the internal clock source 0x1: The functional clock is provided by an external PHY through an IO pad.	RW	0
24	CLKSEL_UTMI_P1	Selects the source of the functional clock for UTMI Port1 on USB_HOST_HS 0x0: The functional clock is provided by the internal clock source 0x1: The functional clock is provided by an external PHY through an IO pad.	RW	0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including Interconnect Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15	OPTFCLKEN_FUNC48M_CLK	USB_HOST_HS optional clock control: FUNC_48M_CLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
14	OPTFCLKEN_HSIC480M_P2_CLK	USB_HOST_HS optional clock control: HSIC_P2_480M_GFCLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	OPTFCLKEN_HSIC480M_P1_CLK	USB_HOST_HS optional clock control: HSIC_P1_480M_GFCLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
12	OPTFCLKEN_HSIC60M_P2_CLK	USB_HOST_HS optional clock control: HSIC_P2_GFCLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
11	OPTFCLKEN_HSIC60M_P1_CLK	USB_HOST_HS optional clock control: HSIC_P1_GFCLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
10	OPTFCLKEN_UTMI_P3_CLK	USB_HOST_HS optional clock control: UTMI_P3_GCLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
9	OPTFCLKEN_UTMI_P2_CLK	USB_HOST_HS optional clock control: UTMI_P2_GCLK when CLKSEL_UTMI_P2 is 0 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_UTMI_P1_CLK	USB_HOST_HS optional clock control: UTMI_P1_GCLK when CLKSEL_UTMI_P1 is 0 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7	OPTFCLKEN_HSIC480M_P3_CLK	USB_HOST_HS optional clock control: HSIC_P3_480_GFCLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0x0
6	OPTFCLKEN_HSIC60M_P3_CLK	USB_HOST_HS optional clock control: HSIC_P3_GFCLK 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0x0
5	RESERVED		R	0x0
4	SAR_MODE	SAR mode control for the module. Shall not be modify except if module is disabled. 0x0: SAR mode is disabled 0x1: SAR mode is enabled	RW	0
3:2	RESERVED		R	0x0
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1371. Register Call Summary for Register CM_L3INIT_USB_HOST_HS_CLKCTRL

Clock Management Functional Description
- CKGEN_USB Clock Generator: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- CM_CORE Clock Generator: [11]
- Clock Domain Module Attributes: [12] [13] [14]

PRCM Register Manual
- L3INIT_CM_CORE Register Summary: [15]

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Table 3-1372. CM_L3INIT_USB_TLL_HS_CLKCTRL

Address Offset	0x0000 0068		
Physical Address	0x4A00 9668	**Instance**	L3INIT_CM_CORE
Description	This register manages the USB_TLL_HS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED					OPTFCLKEN_USB_CH2_CLK	OPTFCLKEN_USB_CH1_CLK	OPTFCLKEN_USB_CH0_CLK	RESERVED			SAR_MODE	RESERVED		MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:11	RESERVED		R	0x00
10	OPTFCLKEN_USB_CH2_CLK	USB_TLL_HS optional clock control: USB_CH2_CLK (TLL_CH2_GFCLK) 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
9	OPTFCLKEN_USB_CH1_CLK	USB_TLL_HS optional clock control: USB_CH1_CLK (TLL_CH1_GFCLK) 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
8	OPTFCLKEN_USB_CH0_CLK	USB_TLL_HS optional clock control: USB_CH0_CLK (TLL_CH0_GFCLK) 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:5	RESERVED		R	0x0
4	SAR_MODE	SAR mode control for the module. Shall not be modify except if module is disabled. 0x0: SAR mode is disabled 0x1: SAR mode is enabled	RW	0
3:2	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3INIT_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any Interconnect access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1373. Register Call Summary for Register CM_L3INIT_USB_TLL_HS_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L3INIT_CM_CORE Register Summary: [2]

Table 3-1374. CM_L3INIT_IEEE1500_2_OCP_CLKCTRL

Address Offset	0x0000 0078		
Physical Address	0x4A00 9678	**Instance**	L3INIT_CM_CORE
Description	This register manages the IEEE1500_2_OCP clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including Interconnect Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x1

Table 3-1375. Register Call Summary for Register CM_L3INIT_IEEE1500_2_OCP_CLKCTRL

Clock Management Functional Description
- Clock Domain Module Attributes: [0] [1] [2]

PRCM Register Manual
- L3INIT_CM_CORE Register Summary: [3]

Table 3-1376. CM_L3INIT_SATA_CLKCTRL

Address Offset	0x0000 0088		
Physical Address	0x4A00 9688	**Instance**	L3INIT_CM_CORE
Description	This register manages the SATA clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED							OPTFCLKEN_REF_CLK	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including Interconnect Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x0000
8	OPTFCLKEN_REF_CLK	SATA optional clock control: REF_CLK (from SYS_CLK clock) 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0x0000
7:2	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0x0

Table 3-1377. Register Call Summary for Register CM_L3INIT_SATA_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1] [2]
PRCM Register Manual • L3INIT_CM_CORE Register Summary: [3]

Table 3-1378. CM_L3INIT_OCP2SCP1_CLKCTRL

Address Offset	0x0000 00E0		
Physical Address	0x4A00 96E0	**Instance**	L3INIT_CM_CORE
Description	This register manages the OCP2SCP1 clocks and the optional clock of USB_PHY_CORE.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED								MODULEMODE							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including Interconnect Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3INIT_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any Interconnect access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1379. Register Call Summary for Register CM_L3INIT_OCP2SCP1_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L3INIT_CM_CORE Register Summary: [2]

Table 3-1380. CM_L3INIT_OCP2SCP3_CLKCTRL

Address Offset	0x0000 00E8		
Physical Address	0x4A00 96E8	**Instance**	L3INIT_CM_CORE
Description	This register manages the OCP2SCP3 clocks and the optional clock of USB_PHY_CORE.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including Interconnect Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3INIT_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any Interconnect access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1381. Register Call Summary for Register CM_L3INIT_OCP2SCP3_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • L3INIT_CM_CORE Register Summary: [2]

Table 3-1382. CM_L3INIT_USB_OTG_SS_CLKCTRL

Address Offset	0x0000 00F0		
Physical Address	0x4A00 96F0	**Instance**	L3INIT_CM_CORE
Description	This register manages the USB_OTG_SS clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STBYST	IDLEST		RESERVED							OPTFCLKEN_REFCLK960M	RESERVED						MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including Interconnect Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be accessed	R	0x3
15:9	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
8	OPTFCLKEN_REFCLK960M	USB_OTG_SS optional clock control: L3INIT_960M_GFCLK (960MHz clock) 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. If CM_L3INIT_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 (HW_AUTO), any Interconnect access to module is always granted. Module clocks may be gated according to the clock domain state. Read 0x2: Reserved Read 0x3: Reserved	RW	0x0

Table 3-1383. Register Call Summary for Register CM_L3INIT_USB_OTG_SS_CLKCTRL

Clock Management Functional Description • Clock Domain Modes: [0] • Clock Domain Module Attributes: [1] [2] [3]
PRCM Register Manual • L3INIT_CM_CORE Register Summary: [4]

3.11.38 CUSTEFUSE_CM_CORE Registers

3.11.38.1 CUSTEFUSE_CM_CORE Register Summary

Table 3-1384. CUSTEFUSE_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CUSTEFUSE_CM_CORE Base Address
CM_CUSTEFUSE_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9700
CM_CUSTEFUSE_EFUSE_CTRL_CUST_CLKCTRL	RW	32	0x0000 0020	0x4A00 9720

3.11.38.2 CUSTEFUSE_CM_CORE Register Description

Table 3-1385. CM_CUSTEFUSE_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9700	**Instance**	CUSTEFUSE_CM_CORE
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also hold one status bit per clock input of the domain.		
Type	RW		

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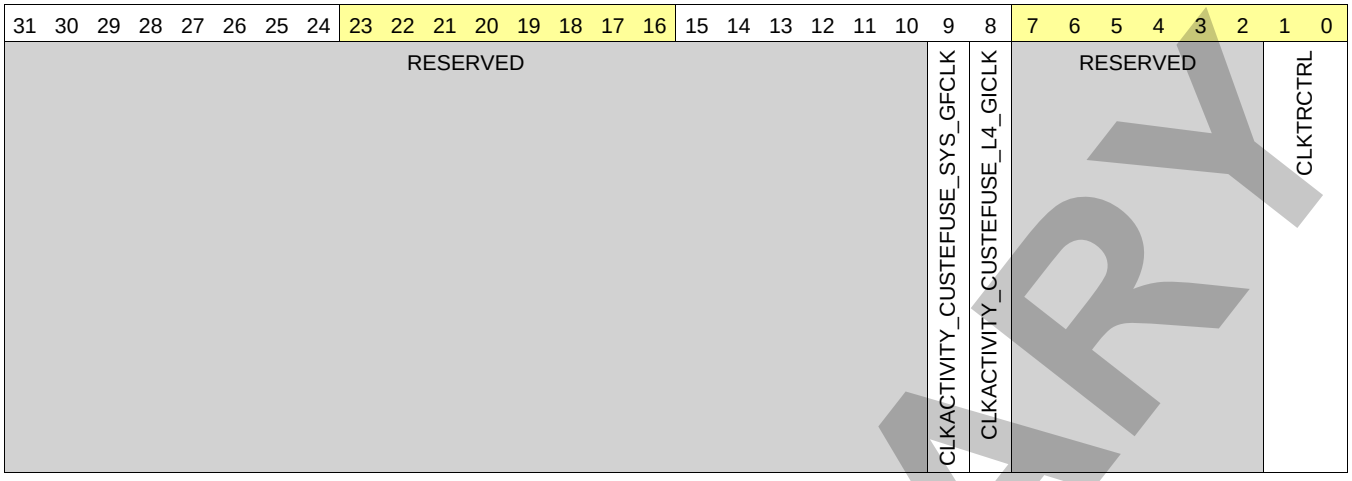

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00 0000
9	CLKACTIVITY_CUSTEFUSE_SYS_GFCLK	This field indicates the state of the CUSTEFUSE_SYS_GFCLK clock input of the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
8	CLKACTIVITY_CUSTEFUSE_L4_GICLK	This field indicates the state of the CUSTEFUSE_L4_GICLK clock input of the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the EFUSE_CTRL_CUST clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions. 0x1: Reserved 0x2: SW_WKUP: Start a software forced wake-up transition on the domain.	RW	0x3

Table 3-1386. Register Call Summary for Register CM_CUSTEFUSE_CLKSTCTRL

Clock Management Functional Description
- Clock Domain Modes: [0] [1] [2]

PRCM Register Manual
- CUSTEFUSE_CM_CORE Register Summary: [3]

Table 3-1387. CM_CUSTEFUSE_EFUSE_CTRL_CUST_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9720	**Instance**	CUSTEFUSE_CM_CORE
Description	This register manages the EFUSE_CTRL_CUST clocks.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														IDLEST		RESERVED														MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be accessed Read 0x2: Module is in Idle mode (only Interconnect part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including Interconnect	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disabled by SW. Any Interconnect access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). 0x3: Reserved 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3-1388. Register Call Summary for Register CM_CUSTEFUSE_EFUSE_CTRL_CUST_CLKCTRL

Clock Management Functional Description • Clock Domain Module Attributes: [0] [1]
PRCM Register Manual • CUSTEFUSE_CM_CORE Register Summary: [2]

3.11.39 INSTR_CM_CORE Registers

3.11.39.1 INSTR_CM_CORE Register Summary

Table 3-1389. INSTR_CM_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INSTR_CM_CORE Base Address
CMI_IDENTICATION	R	32	0x0000 0000	0x4A00 9F00
CMI_SYS_CONFIG	RW	32	0x0000 0010	0x4A00 9F10
CMI_STATUS	R	32	0x0000 0014	0x4A00 9F14
CMI_CONFIGURATION	RW	32	0x0000 0024	0x4A00 9F24
CMI_CLASS_FILTERING	RW	32	0x0000 0028	0x4A00 9F28
CMI_TRIGGERING	RW	32	0x0000 002C	0x4A00 9F2C
CMI_SAMPLING	RW	32	0x0000 0030	0x4A00 9F30

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3.11.39.2 INSTR_CM_CORE Register Description

Table 3-1390. CMI_IDENTICATION

Address Offset	0x0000 0000		
Physical Address	0x4A00 9F00	**Instance**	INSTR_CM_CORE
Description	CM profiling identification register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	0x-- TI Internal data.

Table 3-1391. Register Call Summary for Register CMI_IDENTICATION

PRCM Register Manual
- INSTR_CM_CORE Register Summary: [0]

Table 3-1392. CMI_SYS_CONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A00 9F10	**Instance**	INSTR_CM_CORE
Description	CM profiling system configuartion register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED				IDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	RESERVED	Reserved	R	0x0
3:2	IDLEMODE	Configuration of the local tartget state management mode	RW	0x2
1	RESERVED	Reserved	R	0
0	SOFTRESET	Software reset	RW	0

Table 3-1393. Register Call Summary for Register CMI_SYS_CONFIG

PRCM Register Manual
- INSTR_CM_CORE Register Summary: [0]

Table 3-1394. CMI_STATUS

Address Offset	0x0000 0014		
Physical Address	0x4A00 9F14	**Instance**	INSTR_CM_CORE
Description	CM profiling status register		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FIFOEMPTY	RESERVED							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FIFOEMPTY	CM Profiling buffer empty status 0x0: CM profiling buffer not empty – CM events not yet exported 0x1: CM profiling buffer empty	R	0x1
7:0	RESERVED	Reserved	R	0x00

Table 3-1395. Register Call Summary for Register CMI_STATUS

PRCM Register Manual
- INSTR_CM_CORE Register Summary: [0]

Table 3-1396. CMI_CONFIGURATION

Address Offset	0x0000 0024		
Physical Address	0x4A00 9F24	**Instance**	INSTR_CM_CORE
Description	CM profiling configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAIM_3		CLAIM_2	CLAIM_1	RESERVED				RESERVED								MOD_ACT_EN	RESERVED							EVT_CAPT_EN	RESERVED						

Bits	Field Name	Description	Type	Reset
31:30	CLAIM_3	Ownership	RW	0x0
29	CLAIM_2	Debugger override qualifier	RW	1
28	CLAIM_1	Current owner	R	0
27:24	RESERVED	Reserved	R	0x0
23	RESERVED	Reserved	R	0
22:16	RESERVED	Reserved	R	0x00
15	MOD_ACT_EN	When HIGH the CM Module Activity collection is enabled	RW	0
14:8	RESERVED	Reserved	R	0x00
7	EVT_CAPT_EN	When HIGH the CM events capture is enabled	RW	0
6:0	RESERVED	Reserved	R	0x00

Table 3-1397. Register Call Summary for Register CMI_CONFIGURATION

PRCM Register Manual
- INSTR_CM_CORE Register Summary: [0]

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Table 3-1398. CMI_CLASS_FILTERING

Address Offset	0x0000 0028		
Physical Address	0x4A00 9F28	**Instance**	INSTR_CM_CORE
Description	CM profiling class filtering register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SNAP_CAPT_EN_1F	SNAP_CAPT_EN_1E	SNAP_CAPT_EN_1D	SNAP_CAPT_EN_1C	SNAP_CAPT_EN_1B	SNAP_CAPT_EN_1A	SNAP_CAPT_EN_19	SNAP_CAPT_EN_18	SNAP_CAPT_EN_17	SNAP_CAPT_EN_16	SNAP_CAPT_EN_15	SNAP_CAPT_EN_14	SNAP_CAPT_EN_13	SNAP_CAPT_EN_12	SNAP_CAPT_EN_11	SNAP_CAPT_EN_10	RESERVED												SNAP_CAPT_EN_03	SNAP_CAPT_EN_02	SNAP_CAPT_EN_01	SNAP_CAPT_EN_00

Bits	Field Name	Description	Type	Reset
31	SNAP_CAPT_EN_1F	Snapshot capture enable - Class-ID = 0x1F	RW	0
30	SNAP_CAPT_EN_1E	Snapshot capture enable - Class-ID = 0x1E	RW	0
29	SNAP_CAPT_EN_1D	Snapshot capture enable - Class-ID = 0x1D	RW	0
28	SNAP_CAPT_EN_1C	Snapshot capture enable - Class-ID = 0x1C	RW	0
27	SNAP_CAPT_EN_1B	Snapshot capture enable - Class-ID = 0x1B	RW	0
26	SNAP_CAPT_EN_1A	Snapshot capture enable - Class-ID = 0x1A	RW	0
25	SNAP_CAPT_EN_19	Snapshot capture enable - Class-ID = 0x19	RW	0
24	SNAP_CAPT_EN_18	Snapshot capture enable - Class-ID = 0x18	RW	0
23	SNAP_CAPT_EN_17	Snapshot capture enable - Class-ID = 0x17	RW	0
22	SNAP_CAPT_EN_16	Snapshot capture enable - Class-ID = 0x16	RW	0
21	SNAP_CAPT_EN_15	Snapshot capture enable - Class-ID = 0x15	RW	0
20	SNAP_CAPT_EN_14	Snapshot capture enable - Class-ID = 0x14	RW	0
19	SNAP_CAPT_EN_13	Snapshot capture enable - Class-ID = 0x13	RW	0
18	SNAP_CAPT_EN_12	Snapshot capture enable - Class-ID = 0x12	RW	0
17	SNAP_CAPT_EN_11	Snapshot capture enable - Class-ID = 0x11	RW	0
16	SNAP_CAPT_EN_10	Snapshot capture enable - Class-ID = 0x10	RW	0
15:4	RESERVED		R	0x000
3	SNAP_CAPT_EN_03	Snapshot capture enable - Class-ID = 0x03 [0x23]	RW	0
2	SNAP_CAPT_EN_02	Snapshot capture enable - Class-ID = 0x02 [0x22]	RW	0
1	SNAP_CAPT_EN_01	Snapshot capture enable - Class-ID = 0x01 [0x21]	RW	0
0	SNAP_CAPT_EN_00	Snapshot capture enable - Class-ID = 0x00 [0x20]	RW	0

Table 3-1399. Register Call Summary for Register CMI_CLASS_FILTERING

PRCM Register Manual

- INSTR_CM_CORE Register Summary: [0]

Table 3-1400. CMI_TRIGGERING

Address Offset	0x0000 002C		
Physical Address	0x4A00 9F2C	**Instance**	INSTR_CM_CORE
Description	CM profiling triggering control register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TRIG_STOP_EN	TRIG_START_EN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	TRIG_STOP_EN	Enable stop capturing CM events from external trigger detection	RW	0
0	TRIG_START_EN	Enable start capturing CM events from external trigger detection	RW	0

Table 3-1401. Register Call Summary for Register CMI_TRIGGERING

PRCM Register Manual
- INSTR_CM_CORE Register Summary: [0]

Table 3-1402. CMI_SAMPLING

Address Offset	0x0000 0030		
Physical Address	0x4A00 9F30	**Instance**	INSTR_CM_CORE
Description	CM profiling sampling window register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FCLK_DIV_FACOR				RESERVED								SAMP_WIND_SIZE							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:16	FCLK_DIV_FACOR	FunClk divide factor ranging from 1 to 16	RW	0x0
15:8	RESERVED	Reserved	R	0x00
7:0	SAMP_WIND_SIZE	CM events sampling window size	RW	0x00

Table 3-1403. Register Call Summary for Register CMI_SAMPLING

PRCM Register Manual
- INSTR_CM_CORE Register Summary: [0]

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3.12 SCRM Register Manual

3.12.1 SCRM Instance Summary

Table 3-1404. SCRM Instance Summary

Module Name	Base Address	Size
SCRM	0x4AE0 A000	4KB

3.12.2 SCRM Registers

3.12.2.1 SCRM Register Summary

Table 3-1405. SCRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SCRM Base Address
REVISION_SCRM	R	32	0x0000 0000	0x4AE0 A000
CLKSETUPTIME	RW	32	0x0000 0100	0x4AE0 A100
PMICSETUPTIME	RW	32	0x0000 0104	0x4AE0 A104
RESERVED	R	32	0x0000 0110	0x4AE0 A110
RESERVED	R	32	0x0000 0118	0x4AE0 A118
RESERVED	R	32	0x0000 011C	0x4AE0 A11C
EXTCLKREQ	RW	32	0x0000 0200	0x4AE0 A200
ACCCLKREQ	RW	32	0x0000 0204	0x4AE0 A204
PWRREQ	RW	32	0x0000 0208	0x4AE0 A208
AUXCLKREQ0	RW	32	0x0000 0210	0x4AE0 A210
AUXCLKREQ1	RW	32	0x0000 0214	0x4AE0 A214
AUXCLKREQ2	RW	32	0x0000 0218	0x4AE0 A218
AUXCLKREQ3	RW	32	0x0000 021C	0x4AE0 A21C
AUXCLKREQ4	RW	32	0x0000 0220	0x4AE0 A220
RESERVED	R	32	0x0000 0224	0x4AE0 A224
RESERVED	R	32	0x0000 0234	0x4AE0 A224
AUXCLK0	RW	32	0x0000 0310	0x4AE0 A310
AUXCLK1	RW	32	0x0000 0314	0x4AE0 A314
AUXCLK2	RW	32	0x0000 0318	0x4AE0 A318
AUXCLK3	RW	32	0x0000 031C	0x4AE0 A31C
AUXCLK4	RW	32	0x0000 0320	0x4AE0 A320
RESERVED	R	32	0x0000 0324	0x4AE0 A324
RSTTIME_REG	RW	32	0x0000 0400	0x4AE0 A400
RESERVED	R	32	0x0000 0418	0x4AE0 A418
RESERVED	R	32	0x0000 041C	0x4AE0 A41C
EXTPWRONRSTCTRL	RW	32	0x0000 0420	0x4AE0 A420
EXTWARMRSTST_REG	RW	32	0x0000 0510	0x4AE0 A510
APEWARMRSTST_REG	RW	32	0x0000 0514	0x4AE0 A514
RESERVED	R	32	0x0000 0518	0x4AE0 A518
RESERVED	R	32	0x0000 051C	0x4AE0 A51C

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3.12.2.2 SCRM Register Description

Table 3-1406. REVISION_SCRM

Address Offset	0x0000 0000		
Physical Address	0x4AE0 A000	**Instance**	SCRM
Description	This register contains the IP revision code for the SCRM.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REV							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reads returns 0.	R	0x000000
7:0	REV	Revision Number	R	0x- - TI Internal data.

Table 3-1407. Register Call Summary for Register REVISION_SCRM

SCRM Register Manual

- SCRM Register Summary: [0]

Table 3-1408. CLKSETUPTIME

Address Offset	0x0000 0100		
Physical Address	0x4AE0 A100	**Instance**	SCRM
Description	This register holds the clock setup time counters of the system clock source supplier.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DOWNTIME								RESERVED				SETUPTIME											

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reads returns 0.	R	0x000
21:16	DOWNTIME	Holds the number of 32 kHz clock cycles it takes to gate the clock source supplier.	RW	0x00
15:12	RESERVED	Reads returns 0.	R	0x0
11:0	SETUPTIME	Holds the number of 32 kHz clock cycles it takes to stabilize the clock source supplier.	RW	0x000

Table 3-1409. Register Call Summary for Register CLKSETUPTIME

SCRM Register Manual

- SCRM Register Summary: [0]

Table 3-1410. PMICSETUPTIME

Address Offset	0x0000 0104		
Physical Address	0x4AE0 A104	**Instance**	SCRM
Description	This register holds the setup time counters for the sleep mode of the clock-source generator power supply (the power supply in external connected PMIC or LDO).		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WAKEUPTIME								RESERVED								SLEEPTIME							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reads returns 0.	R	0x000
21:16	WAKEUPTIME	Holds the number of 32 kHz clock cycles it takes to exit the clock-source generator power supply from sleep mode. SCRM starts Wakeup-time counter by activation of power request.	RW	0x00
15:6	RESERVED	Reads returns 0.	R	0x000
5:0	SLEEPTIME	Holds the number of 32 kHz clock cycles it takes to enter the clock source generator power supply in sleep mode. SCRM activates Sleep-time counter by deactivation of power request.	RW	0x00

Table 3-1411. Register Call Summary for Register PMICSETUPTIME

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1412. EXTCLKREQ

Address Offset	0x0000 0200		
Physical Address	0x4AE0 A200	**Instance**	SCRM
Description	This register holds qualifiers for the external clock request.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															POLARITY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	POLARITY	This bit defines the active level of the external clock request. 0x0: The external clock request is active low. 0x1: The external clock request is active high.	RW	1

Table 3-1413. Register Call Summary for Register EXTCLKREQ

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1414. ACCCLKREQ

Address Offset	0x0000 0204		
Physical Address	0x4AE0 A204	**Instance**	SCRM
Description	This register holds qualifiers for the accurate clock request.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															POLARITY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	POLARITY	This bit defines the active level of the accurate clock request. 0x0: The accurate clock request is active low. 0x1: The accurate clock request is active high.	RW	1

Table 3-1415. Register Call Summary for Register ACCCLKREQ

SCRM Register Manual • SCRM Register Summary: [0]

Table 3-1416. PWRREQ

Address Offset	0x0000 0208		
Physical Address	0x4AE0 A208	**Instance**	SCRM
Description	This register holds qualifiers for the external power request.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															POLARITY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	POLARITY	This bit defines the active level of the external power request. 0x0: The external power request is active low. 0x1: The external power request is active high.	RW	1

Table 3-1417. Register Call Summary for Register PWRREQ

PRCM Register Manual • DEVICE_PRM Register Description: [0] [1] [2] [3] [4] [5] [6]
SCRM Register Manual • SCRM Register Summary: [7]

Table 3-1418. AUXCLKREQ0

Address Offset	0x0000 0210		
Physical Address	0x4AE0 A210	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #0 on another auxiliary clock output than auxiliary clock #0. 0x0: The auxiliary clock request #0 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #0 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #0 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #0 is mapped on the auxiliary clock #3. 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved	RW	0x0
1	ACCURACY	This bit qualifies the auxiliary clock request #0 as an accurate clock request. 0x0: An active auxiliary clock request #0 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #0 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #0. 0x0: The auxiliary clock request #0 is active low. 0x1: The auxiliary clock request #0 is active high.	RW	1

Table 3-1419. Register Call Summary for Register AUXCLKREQ0

PRCM Subsystem Environment • External Clock Signals: [0]
SCRM Register Manual • SCRM Register Summary: [1]

Table 3-1420. AUXCLKREQ1

Address Offset	0x0000 0214		
Physical Address	0x4AE0 A214	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads returns 0.	R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #1 on another auxiliary clock output than auxiliary clock #1. 0x0: The auxiliary clock request #1 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #1 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #1 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #1 is mapped on the auxiliary clock #3. 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved	RW	0x1
1	ACCURACY	This bit qualifies the auxiliary clock request #1 as an accurate clock request. 0x0: An active auxiliary clock request #1 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #1 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #1. 0x0: The auxiliary clock request #1 is active low. 0x1: The auxiliary clock request #1 is active high.	RW	1

Table 3-1421. Register Call Summary for Register AUXCLKREQ1

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1422. AUXCLKREQ2

Address Offset	0x0000 0218		
Physical Address	0x4AE0 A218	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #2.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads returns 0.	R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #2 on another auxiliary clock output than auxiliary clock #2. 0x0: The auxiliary clock request #2 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #2 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #2 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #2 is mapped on the auxiliary clock #3. 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved	RW	0x2
1	ACCURACY	This bit qualifies the auxiliary clock request #2 as an accurate clock request. 0x0: An active auxiliary clock request #2 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #2 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #2. 0x0: The auxiliary clock request #2 is active low. 0x1: The auxiliary clock request #2 is active high.	RW	1

Table 3-1423. Register Call Summary for Register AUXCLKREQ2

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1424. AUXCLKREQ3

Address Offset	0x0000 021C		
Physical Address	0x4AE0 A21C	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #3.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads returns 0.	R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #3 on another auxiliary clock output than auxiliary clock #3. 0x0: The auxiliary clock request #3 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #3 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #3 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #3 is mapped on the auxiliary clock #3. 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved	RW	0x3
1	ACCURACY	This bit qualifies the auxiliary clock request #3 as an accurate clock request. 0x0: An active auxiliary clock request #3 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #3 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #3. 0x0: The auxiliary clock request #3 is active low. 0x1: The auxiliary clock request #3 is active high.	RW	1

Table 3-1425. Register Call Summary for Register AUXCLKREQ3

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1426. AUXCLKREQ4

Address Offset	0x0000 0220		
Physical Address	0x4AE0 A220	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock request #4.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MAPPING			ACCURACY	POLARITY

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads returns 0.	R	0x0000000
4:2	MAPPING	This field allows re-mapping the auxiliary clock request #4 on another auxiliary clock output than auxiliary clock #4. 0x0: The auxiliary clock request #4 is mapped on the auxiliary clock #0. 0x1: The auxiliary clock request #4 is mapped on the auxiliary clock #1. 0x2: The auxiliary clock request #4 is mapped on the auxiliary clock #2. 0x3: The auxiliary clock request #4 is mapped on the auxiliary clock #3. 0x4: The auxiliary clock request #4 is mapped on the auxiliary clock #4. 0x5: The auxiliary clock request #4 is mapped on the auxiliary clock #5. 0x6: Reserved 0x7: Reserved	RW	0x4
1	ACCURACY	This bit qualifies the auxiliary clock request #4 as an accurate clock request. 0x0: An active auxiliary clock request #4 doesn't generate an accurate clock request. 0x1: An active auxiliary clock request #4 generates an accurate clock request.	RW	0
0	POLARITY	This bit defines the active level of the auxiliary clock request #4. 0x0: The auxiliary clock request #4 is active low. 0x1: The auxiliary clock request #4 is active high.	RW	1

Table 3-1427. Register Call Summary for Register AUXCLKREQ4

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1428. AUXCLK0

Address Offset	0x0000 0310		
Physical Address	0x4AE0 A310	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLKDIV								RESERVED						DISABLECLK	ENABLE	RESERVED					SRCSELECT		POLARITY

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #0. 0x0: The auxiliary clock #0 is divided by 1. 0x1: The auxiliary clock #0 is divided by 2. 0x2: The auxiliary clock #0 is divided by 3. 0x3: The auxiliary clock #0 is divided by 4. 0x4: The auxiliary clock #0 is divided by 5. 0x5: The auxiliary clock #0 is divided by 6. 0x6: The auxiliary clock #0 is divided by 7. 0x7: The auxiliary clock #0 is divided by 8. 0x8: The auxiliary clock #0 is divided by 9. 0x9: The auxiliary clock #0 is divided by 10. 0xA: The auxiliary clock #0 is divided by 11. 0xB: The auxiliary clock #0 is divided by 12. 0xC: The auxiliary clock #0 is divided by 13. 0xD: The auxiliary clock #0 is divided by 14. 0xE: The auxiliary clock #0 is divided by 15. 0xF: The auxiliary clock #0 is divided by 16.	RW	0x0
15:10	RESERVED	Reads returns 0.	R	0x00
9	DISABLECLK	This bit allows to gate the auxiliary clock #0 without condition. This is bit is intended to be used only when the SOC is not clock provider. 0x0: The auxiliary clock #0 is gated upon normal condition: auxiliary clock requests mapped on this path or ENABLE bit set. 0x1: The auxiliary clock #0 is gated wihout conditon.	RW	0
8	ENABLE	This bit allows to request the auxiliary clock #0 by software. 0x0: The auxiliary clock #0 is not requested by software. 0x1: The auxiliary clock #0 is requested by software.	RW	0
7:3	RESERVED	Reads returns 0.	R	0x00
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #0. 0x0: The clock source is the system clock (SYS_CLK). 0x1: The clock source is the version from the DPLL_CORE. 0x2: The clock source is the version from the DPLL_PER. 0x3: Reserved	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #0 is gated. 0x0: The auxiliary clock #0 is gated low. 0x1: The auxiliary clock #0 is gated high.	RW	0

Table 3-1429. Register Call Summary for Register AUXCLK0

PRCM Subsystem Environment • External Clock Signals: [0]
SCRM Register Manual • SCRM Register Summary: [1]

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Table 3-1430. AUXCLK1

Address Offset	0x0000 0314		
Physical Address	0x4AE0 A314	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CLKDIV				RESERVED							ENABLE	RESERVED					SRCSELECT		POLARITY

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #1. 0x0: The auxiliary clock #1 is divided by 1. 0x1: The auxiliary clock #1 is divided by 2. 0x2: The auxiliary clock #1 is divided by 3. 0x3: The auxiliary clock #1 is divided by 4. 0x4: The auxiliary clock #1 is divided by 5. 0x5: The auxiliary clock #1 is divided by 6. 0x6: The auxiliary clock #1 is divided by 7. 0x7: The auxiliary clock #1 is divided by 8. 0x8: The auxiliary clock #1 is divided by 9. 0x9: The auxiliary clock #1 is divided by 10. 0xA: The auxiliary clock #1 is divided by 11. 0xB: The auxiliary clock #1 is divided by 12. 0xC: The auxiliary clock #1 is divided by 13. 0xD: The auxiliary clock #1 is divided by 14. 0xE: The auxiliary clock #1 is divided by 15. 0xF: The auxiliary clock #1 is divided by 16.	RW	0x0
15:9	RESERVED	Reads returns 0.	R	0x00
8	ENABLE	This bit allows to request the auxiliary clock #1 by software. 0x0: The auxiliary clock #1 is not requested by software. 0x1: The auxiliary clock #1 is requested by software.	RW	0
7:3	RESERVED	Reads returns 0.	R	0x00
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #1. 0x0: The clock source is the system clock (SYS_CLK) 0x1: The clock source is the version from the DPLL_CORE. 0x2: The clock source is the version from the DPLL_PER. 0x3: Reserved	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #1 is gated. 0x0: The auxiliary clock #1 is gated low. 0x1: The auxiliary clock #1 is gated high.	RW	0

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Table 3-1431. Register Call Summary for Register AUXCLK1

PRCM Subsystem Environment • External Clock Signals: [0]
SCRM Register Manual • SCRM Register Summary: [1]

Table 3-1432. AUXCLK2

Address Offset	0x0000 0318		
Physical Address	0x4AE0 A318	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #2.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLKDIV								RESERVED							ENABLE	RESERVED					SRCSELECT		POLARITY

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #2. 0x0: The auxiliary clock #2 is divided by 1. 0x1: The auxiliary clock #2 is divided by 2. 0x2: The auxiliary clock #2 is divided by 3. 0x3: The auxiliary clock #2 is divided by 4. 0x4: The auxiliary clock #2 is divided by 5. 0x5: The auxiliary clock #2 is divided by 6. 0x6: The auxiliary clock #2 is divided by 7. 0x7: The auxiliary clock #2 is divided by 8. 0x8: The auxiliary clock #2 is divided by 9. 0x9: The auxiliary clock #2 is divided by 10. 0xA: The auxiliary clock #2 is divided by 11. 0xB: The auxiliary clock #2 is divided by 12. 0xC: The auxiliary clock #2 is divided by 13. 0xD: The auxiliary clock #2 is divided by 14. 0xE: The auxiliary clock #2 is divided by 15. 0xF: The auxiliary clock #2 is divided by 16.	RW	0x0
15:9	RESERVED	Reads returns 0.	R	0x00
8	ENABLE	This bit allows to request the auxiliary clock #2 by software. 0x0: The auxiliary clock #2 is not requested by software. 0x1: The auxiliary clock #2 is requested by software.	RW	0
7:3	RESERVED	Reads returns 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #2. 0x0: The clock source is the system clock (SYS_CLK) 0x1: The clock source is the version from the DPLL_CORE. 0x2: The clock source is the version from the DPLL_PER. 0x3: Reserved	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #2 is gated. 0x0: The auxiliary clock #2 is gated low. 0x1: The auxiliary clock #2 is gated high.	RW	0

Table 3-1433. Register Call Summary for Register AUXCLK2

SCRM Register Manual

- SCRM Register Summary: [0]

Table 3-1434. AUXCLK3

Address Offset	0x0000 031C		
Physical Address	0x4AE0 A31C	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #3.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CLKDIV				RESERVED							ENABLE	RESERVED					SRCSELECT		POLARITY

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #3. 0x0: The auxiliary clock #3 is divided by 1. 0x1: The auxiliary clock #3 is divided by 2. 0x2: The auxiliary clock #3 is divided by 3. 0x3: The auxiliary clock #3 is divided by 4. 0x4: The auxiliary clock #3 is divided by 5. 0x5: The auxiliary clock #3 is divided by 6. 0x6: The auxiliary clock #3 is divided by 7. 0x7: The auxiliary clock #3 is divided by 8. 0x8: The auxiliary clock #3 is divided by 9. 0x9: The auxiliary clock #3 is divided by 10. 0xA: The auxiliary clock #3 is divided by 11. 0xB: The auxiliary clock #3 is divided by 12. 0xC: The auxiliary clock #3 is divided by 13. 0xD: The auxiliary clock #3 is divided by 14. 0xE: The auxiliary clock #3 is divided by 15. 0xF: The auxiliary clock #3 is divided by 16.	RW	0x0
15:9	RESERVED	Reads returns 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
8	ENABLE	This bit allows to request the auxiliary clock #3 by software. 0x0: The auxiliary clock #3 is disabled by software. 0x1: The auxiliary clock #3 is requested by software.	RW	0
7:3	RESERVED	Reads returns 0.	R	0x00
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #3. 0x0: The clock source is the system clock. 0x1: The clock source is the version from the DPLL_CORE. 0x2: The clock source is the version from the DPLL_PER. 0x3: Reserved	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #3 is gated. 0x0: The auxiliary clock #3 is gated low. 0x1: The auxiliary clock #3 is gated high.	RW	0

Table 3-1435. Register Call Summary for Register AUXCLK3

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1436. AUXCLK4

Address Offset	0x0000 0320		
Physical Address	0x4AE0 A320	**Instance**	SCRM
Description	This register holds qualifiers for the auxiliary clock #4.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLKDIV								RESERVED							ENABLE	RESERVED					SRCSELECT		POLARITY

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads returns 0.	R	0x000
19:16	CLKDIV	This field holds the divider value for the auxiliary clock #4. 0x0: The auxiliary clock #4 is divided by 1. 0x1: The auxiliary clock #4 is divided by 2. 0x2: The auxiliary clock #4 is divided by 3. 0x3: The auxiliary clock #4 is divided by 4. 0x4: The auxiliary clock #4 is divided by 5. 0x5: The auxiliary clock #4 is divided by 6. 0x6: The auxiliary clock #4 is divided by 7. 0x7: The auxiliary clock #4 is divided by 8. 0x8: The auxiliary clock #4 is divided by 9. 0x9: The auxiliary clock #4 is divided by 10. 0xA: The auxiliary clock #4 is divided by 11. 0xB: The auxiliary clock #4 is divided by 12. 0xC: The auxiliary clock #4 is divided by 13. 0xD: The auxiliary clock #4 is divided by 14. 0xE: The auxiliary clock #4 is divided by 15. 0xF: The auxiliary clock #4 is divided by 16.	RW	0x1
15:9	RESERVED	Reads returns 0.	R	0x00
8	ENABLE	This bit allows to request the auxiliary clock #4 by software. 0x0: The auxiliary clock #4 is disabled by software. 0x1: The auxiliary clock #4 is requested by software.	RW	1
7:3	RESERVED	Reads returns 0.	R	0x00
2:1	SRCSELECT	This field allows selecting the clock source of the auxiliary clock #4. 0x0: The clock source is the system clock. 0x1: The clock source is the version from the DPLL_CORE. 0x2: The clock source is the version from the DPLL_PER. 0x3: The clock source is the alternate clock	RW	0x0
0	POLARITY	This bit defines the output level when the auxiliary clock #4 is gated. 0x0: The auxiliary clock #4 is gated low. 0x1: The auxiliary clock #4 is gated high.	RW	0

Table 3-1437. Register Call Summary for Register AUXCLK4

PRCM Subsystem Environment • External Clock Signals: [0]
SCRM Register Manual • SCRM Register Summary: [1]

Table 3-1438. RSTTIME_REG

Address Offset	0x0000 0400		
Physical Address	0x4AE0 A400	**Instance**	SCRM
Description	This register holds the reset time counter which is used to extend the reset lines beyond the release of the pad reset.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												RSTTIME			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads returns 0.	R	0x0000000
3:0	RSTTIME	Holds the number of 32 kHz clock cycles for which the reset duration is extended. Values 0,1 and 2 are not allowed. 0x0: Reserved. 0x1: Reserved. 0x2: Reserved.	RW	0x4

Table 3-1439. Register Call Summary for Register RSTTIME_REG

SCRM Register Manual
- SCRM Register Summary: [0]

Table 3-1440. EXTPWRONRSTCTRL

Address Offset	0x0000 0420		
Physical Address	0x4AE0 A420	**Instance**	SCRM
Description	This register allows the software to perform an external power-on reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														PWRONRST	ENABLE

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0.	R	0x0000 0000
1	PWRONRST	This bit controls the assertion and the de-assertion of the external power-on reset. 0x0: De-asserts the external power-on reset. 0x1: Asserts the external power-on reset.	RW WSpecial	0
0	ENABLE	This bit must be set to 1 to allow the software to assert the external power-on reset. 0x0: Prevents the software to assert the external power-on reset. 0x1: Allows the software to assert the external power-on reset.	RW WSpecial	0

Table 3-1441. Register Call Summary for Register EXTPWRONRSTCTRL

Reset Management Functional Description
- Power-On Reset: [0] [1]

SCRM Register Manual
- SCRM Register Summary: [2]

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Table 3-1442. EXTWARMRSTST_REG

Address Offset	0x0000 0510		
Physical Address	0x4AE0 A510	**Instance**	SCRM
Description	This register logs the source of warm reset output. Each bit is set upon release of the warm reset output and must be cleared by software.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EXTWARMRSTST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	EXTWARMRSTST	This bit logs the external warm reset source. 0x0: No external warm reset occurred. 0x1: An external warm reset occurred.	RW W1toClr	0

Table 3-1443. Register Call Summary for Register EXTWARMRSTST_REG

Reset Management Functional Description • Warm Reset: [0]
SCRM Register Manual • SCRM Register Summary: [1]

Table 3-1444. APEWARMRSTST_REG

Address Offset	0x0000 0514		
Physical Address	0x4AE0 A514	**Instance**	SCRM
Description	This register logs the source of warm reset on the APE. Each bit is set upon release of the APE warm reset and must be cleared by software.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														APEWARMRSTST	RESERVED

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0.	R	0x0000 0000
1	APEWARMRSTST	This bit logs the APE warm reset source. 0x0: No APE warm reset occurred. 0x1: An APE warm reset occurred.	RW W1toClr	0
0	RESERVED	Reads returns 0.	R	0

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Table 3-1445. Register Call Summary for Register APEWARMRSTST_REG

SCRM Register Manual

- SCRM Register Summary: [0]

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3.13 SmartReflex Register Manual

3.13.1 SmartReflex Instance Summary

Table 3-1446. SmartReflex Instance Summary

Module Name	Base Address	Size
SMARTREFLEX_MPU	0x4A0D 9000	256 bytes
SMARTREFLEX_MM	0x4A0D B000	256 bytes
SMARTREFLEX_CORE	0x4A0D D000	256 bytes

3.13.2 SmartReflex Registers

3.13.2.1 SmartReflex Register Summary

Table 3-1447. SmartReflex Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SMARTREFLEX_MPU Base Address	SMARTREFLEX_MM Base Address	SMARTREFLEX_CORE Base Address
SRCONFIG	RW	32	0x0000 0000	0x4A0D 9000	0x4A0D B000	0x4A0D D000
SRSTATUS	R	32	0x0000 0004	0x4A0D 9004	0x4A0D B004	0x4A0D D004
SENVAL	R	32	0x0000 0008	0x4A0D 9008	0x4A0D B008	0x4A0D D008
SENMIN	R	32	0x0000 000C	0x4A0D 900C	0x4A0D B00C	0x4A0D D00C
SENMAX	R	32	0x0000 0010	0x4A0D 9010	0x4A0D B010	0x4A0D D010
SENAVG	R	32	0x0000 0014	0x4A0D 9014	0x4A0D B014	0x4A0D D014
AVGWEIGHT_REG	RW	32	0x0000 0018	0x4A0D 9018	0x4A0D B018	0x4A0D D018
NVALUERECIPROCAL	RW	32	0x0000 001C	0x4A0D 901C	0x4A0D B01C	0x4A0D D01C
RESERVED	W	32	0x0000 0020	0x4A0D 9020	0x4A0D B020	0x4A0D D020
IRQSTATUS_RAW	RW	32	0x0000 0024	0x4A0D 9024	0x4A0D B024	0x4A0D D024
IRQSTATUS	RW	32	0x0000 0028	0x4A0D 9028	0x4A0D B028	0x4A0D D028
IRQENABLE_SET	RW	32	0x0000 002C	0x4A0D 902C	0x4A0D B02C	0x4A0D D02C
IRQENABLE_CLR	RW	32	0x0000 0030	0x4A0D 9030	0x4A0D B030	0x4A0D D030
SENERROR_REG	R	32	0x0000 0034	0x4A0D 9034	0x4A0D B034	0x4A0D D034
ERRCONFIG	RW	32	0x0000 0038	0x4A0D 9038	0x4A0D B038	0x4A0D D038
LVTSENVAL	R	32	0x0000 003C	0x4A0D 903C	0x4A0D B03C	0x4A0D D03C
LVTSENMIN	R	32	0x0000 0040	0x4A0D 9040	0x4A0D B040	0x4A0D D040
LVTSENMAX	R	32	0x0000 0044	0x4A0D 9044	0x4A0D B044	0x4A0D D044

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Table 3-1447. SmartReflex Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SMARTREFLEX_MPU Base Address	SMARTREFLEX_MM Base Address	SMARTREFLEX_CORE Base Address
LVTSENAVG	R	32	0x0000 0048	0x4A0D 9048	0x4A0D B048	0x4A0D D048
LVTNVALUERECIPROCAL	RW	32	0x0000 004C	0x4A0D 904C	0x4A0D B04C	0x4A0D D04C

3.13.2.2 SmartReflex Register Description

Table 3-1448. SRCONFIG

Address Offset	0x0000 0000		
Physical Address	0x4A0D 9000 0x4A0D B000 0x4A0D D000	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	Configuration bits for the Sensor Core and the Digital Processing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCUMDATA																SRCLKLENGTH															
																				SRENABLE	SENENABLE	ERRORGENERATORENABLE	MINMAXAVGENABLE	RESERVED			LVTSENENABLE	LVTSENNENABLE	LVTSENPENABLE	SENNENABLE	SENPENABLE

Bits	Field Name	Description	Type	Reset
31:22	ACCUMDATA	Number of Values to Accumulate	RW	0x080
21:12	SRCLKLENGTH	Determines frequency of SMARTREFLEX_CLK	RW	0x200
11	SRENABLE	0: Synchronously resets MINMAXAVGACCUMVALID, MINMAXAVGVALID, ERRORGENERATORVALID, ACCUMDATA sensor, SMARTREFLEX_CLK counter, and MINMAXAVG bits. Also gates the clock for power savings and disables all the digital logic. 1: Enables the module	RW	0
10	SENENABLE	0: All SVT sensors disabled 1: SVT sensors enabled per SenNEnable and SenPEnable	RW	1
9	ERRORGENERATORENABLE	0: Error Generator Module disabled 1: Error Generator Module enabled	RW	0
8	MINMAXAVGENABLE	0: Min/Max/Avg Detector Module disabled 1: Min/Max/Avg Detector Module enabled	RW	0
7:5	RESERVED	Reserved	RW	0x00
4	LVTSENENABLE	LVT sensor enable control 0x0: All LVT sensors disabled 0x1: LVT Sensors enabled per LVTSENxENABLE (x=N/P)	RW	0x1
3	LVTSENNENABLE	LVT SensorN enable control 0x0: Disables LVTSenN sensor 0x1: Enables LVTSenN sensor	RW	0x1

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Bits	Field Name	Description	Type	Reset
2	LVTSENPENABLE	LVT SensorP enable control 0x0: Disables LVTSenP sensor 0x1: Enables LVTSenP sensor	RW	0x0
1	SENNENABLE	0: Disable SenN sensor 1: Enable SenN sensor	RW	1
0	SENPENABLE	0: Disable SenP sensor 1: Enable SenP sensor	RW	0

Table 3-1449. Register Call Summary for Register SRCONFIG

Voltage-Management Functional Description
- SmartReflex Submodules: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- SmartReflex Convergence Verification: [11]

PRCM Module Programming Guide
- SmartReflex Module Initialization: [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22]
- Disable the Error Generator Module: [23] [24]
- Disable AVS (SmartReflex): [25]
- Changing OPP: [26] [27] [28] [29]

SmartReflex Register Manual
- SmartReflex Register Summary: [30]

Table 3-1450. SRSTATUS

Address Offset	0x0000 0004		
Physical Address	0x4A0D 9004 0x4A0D B004 0x4A0D D004	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	Status bits that indicate that the values in the register are valid or events have occurred.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												AVGERRVALID	MINMAXAVGVALID	ERRORGENERATORVALID	MINMAXAVGACCUMVALID

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	AVGERRVALID	0: AVGERROR bits are not valid 1: AVGERROR bits are valid.	R	0
2	MINMAXAVGVALID	0: SENVAL, SENMIN, SENMAX, SENAVG registers are not valid 1: SeENVAL, SENMIN, SENMAX, SENAVG registers are valid, but not necessarily fully accumulated	R	0
1	ERRORGENERATORVALID	0: SENERROR_REG register do not have valid data 1: SENERROR_REG registers have valid data.	R	0
0	MINMAXAVGACCUMVALID	0: SENVAL, SENMIN, SENMAX, SENAVG registers are not valid 1: SENVAL, SENMIN, SENMAX, SENAVG registers have valid, final data	R	0

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Table 3-1451. Register Call Summary for Register SRSTATUS

Voltage-Management Functional Description • SmartReflex Submodules: [0] • Status Register: [1] [2] [3] [4] [5] [6]
SmartReflex Register Manual • SmartReflex Register Summary: [7]

Table 3-1452. SENVAL

Address Offset	0x0000 0008		
Physical Address	0x4A0D 9008 0x4A0D B008 0x4A0D D008	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The current sensor values from the Sensor Core (SVT)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENPVAL																SENNVAL															

Bits	Field Name	Description	Type	Reset
31:16	SENPVAL	The latest value of the SenPVal from the SVT sensor core.	R	0x0000
15:0	SENNVAL	The latest value of the SenNVal from the SVT sensor core.	R	0x0000

Table 3-1453. Register Call Summary for Register SENVAL

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] • SmartReflex Convergence Verification: [2] [3] [4] • Status Register: [5] [6]
SmartReflex Register Manual • SmartReflex Register Summary: [7] • SmartReflex Register Description: [8] [9] [10]

Table 3-1454. SENMIN

Address Offset	0x0000 000C		
Physical Address	0x4A0D 900C 0x4A0D B00C 0x4A0D D00C	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The minimum sensor values (SVT)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENPMIN																SENNMIN															

Bits	Field Name	Description	Type	Reset
31:16	SENPMIN	The minimum value of the SenPVal from the SVT sensor core since the last restat operation.	R	0xFFFF
15:0	SENNMIN	The minimum value of the SenNVal from the SVT sensor core since the last restat operation.	R	0xFFFF

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Table 3-1455. Register Call Summary for Register SENMIN

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] • Status Register: [2] [3]
SmartReflex Register Manual • SmartReflex Register Summary: [4] • SmartReflex Register Description: [5] [6] [7] [8]

Table 3-1456. SENMAX

Address Offset	0x0000 0010		
Physical Address	0x4A0D 9010 0x4A0D B010 0x4A0D D010	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The maximum sensor values (SVT)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENPMAX																SENNMAX															

Bits	Field Name	Description	Type	Reset
31:16	SENPMAX	The maximum value of the SenPVal from the SVT sensor core since the last restat operation.	R	0x0000
15:0	SENNMAX	The maximum value of the SenNVal from the SVT sensor core since the last restat operation.	R	0x0000

Table 3-1457. Register Call Summary for Register SENMAX

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] • Status Register: [2] [3]
SmartReflex Register Manual • SmartReflex Register Summary: [4] • SmartReflex Register Description: [5] [6] [7] [8]

Table 3-1458. SENAVG

Address Offset	0x0000 0014		
Physical Address	0x4A0D 9014 0x4A0D B014 0x4A0D D014	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The average sensor values (SVT)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENPAVG																SENNAVG															

Bits	Field Name	Description	Type	Reset
31:16	SENPAVG	The running average of the SenPVal from the SVT sensor core since the last restat operation.	R	0x0000
15:0	SENNAVG	The running average of the SenNVal from the SVT sensor core since the last restat operation.	R	0x0000

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Table 3-1459. Register Call Summary for Register SENAVG

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] • Status Register: [2] [3]
SmartReflex Register Manual • SmartReflex Register Summary: [4] • SmartReflex Register Description: [5] [6] [7] [8]

Table 3-1460. AVGWEIGHT_REG

Address Offset	0x0000 0018		
Physical Address	0x4A0D 9018 0x4A0D B018 0x4A0D D018	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The weighting factor in the average computation.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SENPAVGWEIGHT		SENNAVGWEIGHT	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits.	R	0x0000000
3:2	SENPAVGWEIGHT	The weighting factor for the SenP averager.	RW	0x0
1:0	SENNAVGWEIGHT	The weighting factor for the SenN averager.	RW	0x0

Table 3-1461. Register Call Summary for Register AVGWEIGHT_REG

Voltage-Management Functional Description • SmartReflex Parameters Set After Silicon Characterization: [0] [1]
PRCM Module Programming Guide • SmartReflex Module Initialization: [2] [3]
SmartReflex Register Manual • SmartReflex Register Summary: [4]

Table 3-1462. NVALUERECIPROCAL

Address Offset	0x0000 001C		
Physical Address	0x4A0D 901C 0x4A0D B01C 0x4A0D D01C	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The reciprocal of the SenN and SenP values used in error generation (SVT)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SENPGAIN				SENNGAIN				SENPRN								SENNRN							

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved bits.	R	0x00
23:20	SENPGAIN	The gain value for the SVT SenP reciprocal.	RW	0x0
19:16	SENNGAIN	The gain value for the SVT SenN reciprocal.	RW	0x0
15:8	SENPRN	The scale value for the SVT SenP reciprocal.	RW	0x00
7:0	SENNRN	The scale value for the SVT SenN reciprocal.	RW	0x00

Table 3-1463. Register Call Summary for Register NVALUERECIPROCAL

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] [2] [3] • SmartReflex Convergence Verification: [4] • SmartReflex Parameters Set After Silicon Characterization: [5] [6] [7] [8]
PRCM Module Programming Guide • SmartReflex Module Initialization: [9] [10] [11] [12]
SmartReflex Register Manual • SmartReflex Register Summary: [13]

Table 3-1464. IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x4A0D 9024 0x4A0D B024 0x4A0D D024	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	MPU raw interrup status and set.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MCUACCUMINTSTATRAW	MCUVALIDINTSTATRAW	MCUBOUNDSINTSTATRAW	MCUDISABLEACKINTSTATRAW

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits.	R	0x0000000
3	MCUACCUMINTSTATRAW	0: Accum interrupt status is unchanged 1: Accum interrupt status is set	RW	0
2	MCUVALIDINTSTATRAW	0: Valid interrupt status is unchanged 1: Valid interrupt status is set	RW	0
1	MCUBOUNDSINTSTATRAW	0: Bounds interrupt status is unchanged 1: Bounds interrupt status is set	RW	0
0	MCUDISABLEACKINTSTATRAW	0: MPU Disable acknowledge status is unchanged 1: MPU Disable acknowledge status is set	RW	0

Table 3-1465. Register Call Summary for Register IRQSTATUS_RAW

SmartReflex Register Manual • SmartReflex Register Summary: [0]

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Table 3-1466. IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4A0D 9028 0x4A0D B028 0x4A0D D028	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	MPU masked interrupt status and clear.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MCUACCUMINTSTATENA	MCUVALIDINTSTATENA	MCUBOUNDSINTSTATENA	MCUDISABLEACKINTSTATENA

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits.	R	0x0000000
3	MCUACCUMINTSTATENA	Read 0: Accum interrupt status is unchanged Read 1: Accum interrupt status is set Write 0: Accum interrupt status is unchanged Write 1: Accum interrupt status is cleared	RW	0
2	MCUVALIDINTSTATENA	Read 0: Valid interrupt status is unchanged Read 1: Valid interrupt status is set Write 0: Valid interrupt status is unchanged Write 1: Valid interrupt status is cleared	RW	0
1	MCUBOUNDSINTSTATENA	Read 0: Bounds interrupt status is unchanged Read 1: Bounds interrupt status is set Write 0: Bounds interrupt status is unchanged Write 1: Bounds interrupt status is cleared	RW	0
0	MCUDISABLEACKINTSTATENA	Read 0: MPUDisable acknowledge status is unchanged Read 1: MPUDisable acknowledge status is set Write 0: MPUDisable acknowledge status is unchanged Write 1: MPUDisable acknowledge status is cleared	RW	0

Table 3-1467. Register Call Summary for Register IRQSTATUS

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] [2] [3] [4] [5]
PRCM Module Programming Guide • Disable AVS (SmartReflex): [6] [7] [8] [9] [10]
PRCM Register Manual • OCP_SOCKET_PRM Register Description: [11] [12] [13] [14]
SmartReflex Register Manual • SmartReflex Register Summary: [15]

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Table 3-1468. IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x4A0D 902C 0x4A0D B02C 0x4A0D D02C	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	MPU interrupt enable flag and set.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MCUACCUMINTENASET	MCUVALIDINTENASET	MCUBOUNDSINTENASET	MCUDISABLEACTINTENASET

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits.	R	0x0000000
3	MCUACCUMINTENASET	Read mode: 0: Accum interrupt generation is disabled/masked, 1: Accum interrupt generation is enabled; Write mode: 0: No change to Accum interrupt enable, 1: Enable Accum interrupt generation.	RW	0
2	MCUVALIDINTENASET	Read mode: 0: Valid interrupt generation is disabled/masked, 1: Valid interrupt generation is enabled; Write mode: 0: No change to Valid interrupt enable, 1: Enable Valid interrupt generation.	RW	0
1	MCUBOUNDSINTENASET	Read mode: 0: Bounds interrupt generation is disabled/masked, 1: Bounds interrupt generation is enabled; Write mode: 0: No change to Bounds interrupt enable, 1: Enable Bounds interrupt generation.	RW	0
0	MCUDISABLEACTINTENASET	Read mode: 0: MPUDisableAck interrupt generation is disabled/masked, 1: MPUDisableAck interrupt generation is enabled; Write mode: 0: No change to MPUDisAck interrupt enable, 1: Enable MPUDisableAck interrupt generation.	RW	0

Table 3-1469. Register Call Summary for Register IRQENABLE_SET

Voltage-Management Functional Description
- SmartReflex Submodules: [0] [1] [2] [3]

PRCM Module Programming Guide
- SmartReflex Module Initialization: [4] [5] [6]
- Disable AVS (SmartReflex): [7]

SmartReflex Register Manual
- SmartReflex Register Summary: [8]

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Table 3-1470. IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x4A0D 9030 0x4A0D B030 0x4A0D D030	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	MPU interrup enable flag and clear.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MCUACCUMINTENACLR	MCUVALIDINTENACLR	MCUBOUNDSINTENACLR	MCUDISABLEACKINTENACLR

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved bits.	R	0x0000000
3	MCUACCUMINTENACLR	Read mode: 0: Accum interrupt generation is disabled/masked, 1: Accum interrupt generation is enabled; Write mode: 0: No change to Accum interrupt enable, 1: Disable Accum interrupt generation.	RW	0
2	MCUVALIDINTENACLR	Read mode: 0: Valid interrupt generation is disabled/masked, 1: Valid interrupt generation is enabled; Write mode: 0: No change to Valid interrupt enable, 1: Disable Valid interrupt generation.	RW	0
1	MCUBOUNDSINTENACLR	Read mode: 0: Bounds interrupt generation is disabled/masked, 1: Bounds interrupt generation is enabled; Write mode: 0: No change to Bounds interrupt enable, 1: Disable Bounds interrupt generation.	RW	0
0	MCUDISABLEACKINTENACLR	Read mode: 0: MPUDisableAck interrupt generation is disabled/masked, 1: MPUDisableAck interrupt generation is enabled; Write mode: 0: No change to MPUDisAck interrupt enable, 1: Disable MPUDisableAck interrupt generation.	RW	0

Table 3-1471. Register Call Summary for Register IRQENABLE_CLR

Voltage-Management Functional Description
- SmartReflex Submodules: [0] [1] [2] [3]

PRCM Module Programming Guide
- Disable AVS (SmartReflex): [4] [5] [6] [7]

SmartReflex Register Manual
- SmartReflex Register Summary: [8]

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Table 3-1472. SENERROR_REG

Address Offset	0x0000 0034		
Physical Address	0x4A0D 9034 0x4A0D B034 0x4A0D D034	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The sensor error from the error generator.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																AVGERROR								SENERROR							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved bits.	R	0x0000
15:8	AVGERROR	The average sensor error.	R	0x00
7:0	SENERROR	The percentage of sensor error.	R	0x00

Table 3-1473. Register Call Summary for Register SENERROR_REG

Voltage-Management Functional Description
- SmartReflex Submodules: [0] [1] [2] [3]
- Status Register: [4] [5]

SmartReflex Register Manual
- SmartReflex Register Summary: [6]
- SmartReflex Register Description: [7] [8]

Table 3-1474. ERRCONFIG

Address Offset	0x0000 0038		
Physical Address	0x4A0D 9038 0x4A0D B038 0x4A0D D038	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The sensor error configuration.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					WAKEUPENABLE	IDLEMODE		VPBOUNDSINTSTATENA	VPBOUNDSINTENABLE	RESERVED			ERRWEIGHT			ERRMAXLIMIT								ERRMINLIMIT							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved bits.	R	0x00
26	WAKEUPENABLE	Wakeup from MPU Interrupts enable.	RW	0
25:24	IDLEMODE	0b00: Force-Idle Mode, 0b01: No Idle Mode, 0b10: SmartIdle Mode #2, 0b11: Smart-Idle-Wkup mode	RW	0x2
23	VPBOUNDSINTSTATENA	0: Bounds interrupt status is unchanged, 1: Bounds interrupt status is cleared.	RW	0
22	VPBOUNDSINTENABLE	0: Bounds interrupt disabled, 1: Bounds interrupt enabled.	RW	0
21:19	RESERVED	Reserved bits.	R	0x0

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Bits	Field Name	Description	Type	Reset
18:16	ERRWEIGHT	The AvgSenError weight.	RW	0x0
15:8	ERRMAXLIMIT	The upper limit of SenError for interrupt generation.	RW	0x7F
7:0	ERRMINLIMIT	The lower limit of SenError for interrupt generation.	RW	0x80

Table 3-1475. Register Call Summary for Register ERRCONFIG

Voltage-Management Functional Description
- SmartReflex Submodules: [0] [1] [2] [3]
- SmartReflex Convergence Verification: [4] [5] [6]
- SmartReflex Parameters Set After Silicon Characterization: [7] [8] [9] [10] [11] [12] [13]

PRCM Module Programming Guide
- SmartReflex Module Initialization: [14] [15] [16] [17] [18] [19] [20]
- Disable the Error Generator Module: [21]
- Disable AVS (SmartReflex): [22]

SmartReflex Register Manual
- SmartReflex Register Summary: [23]

Table 3-1476. LVTSENVAL

Address Offset	0x0000 003C		
Physical Address	0x4A0D 903C 0x4A0D B03C 0x4A0D D03C	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The current sensor values from the Sensor Core (LVT)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVTSENPVAL																LVTSENNVAL															

Bits	Field Name	Description	Type	Reset
31:16	LVTSENPVAL	The latest value of the SenPVal from the LVT sensor core.	R	0x0000
15:0	LVTSENNVAL	The latest value of the SenNVal from the LVT sensor core.	R	0x0000

Table 3-1477. Register Call Summary for Register LVTSENVAL

Voltage-Management Functional Description
- SmartReflex Submodules: [0] [1]
- Status Register: [2] [3]

SmartReflex Register Manual
- SmartReflex Register Summary: [4]

Table 3-1478. LVTSENMIN

Address Offset	0x0000 0040		
Physical Address	0x4A0D 9040 0x4A0D B040 0x4A0D D040	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The minimum sensor values (LVT)		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVTSENPMIN																LVTSENNMIN															

Bits	Field Name	Description	Type	Reset
31:16	LVTSENPMIN	The minimum value of the SenPVal from the LVT sensor core since the last restat operation.	R	0xFFFF
15:0	LVTSENNMIN	The minimum value of the SenNVal from the LVT sensor core since the last restat operation.	R	0xFFFF

Table 3-1479. Register Call Summary for Register LVTSENMIN

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] • Status Register: [2] [3]
SmartReflex Register Manual • SmartReflex Register Summary: [4]

Table 3-1480. LVTSENMAX

Address Offset	0x0000 0044		
Physical Address	0x4A0D 9044 0x4A0D B044 0x4A0D D044	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The maximum sensor values (LVT)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVTSENPMAX																LVTSENNMAX															

Bits	Field Name	Description	Type	Reset
31:16	LVTSENPMAX	The maximum value of the SenPVal from the LVT sensor core since the last restat operation.	R	0x0000
15:0	LVTSENNMAX	The maximum value of the SenNVal from the LVT sensor core since the last restat operation.	R	0x0000

Table 3-1481. Register Call Summary for Register LVTSENMAX

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] • Status Register: [2] [3]
SmartReflex Register Manual • SmartReflex Register Summary: [4]

Table 3-1482. LVTSENAVG

Address Offset	0x0000 0048		
Physical Address	0x4A0D 9048 0x4A0D B048 0x4A0D D048	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The average sensor values (LVT)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVTSENPAVG																LVTSENNAVG															

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Bits	Field Name	Description	Type	Reset
31:16	LVTSENPAVG	The running average of the SenPVal from the LVT sensor core since the last restat operation.	R	0x0000
15:0	LVTSENNAVG	The running average of the SenNVal from the LVT sensor core since the last restat operation.	R	0x0000

Table 3-1483. Register Call Summary for Register LVTSENAVG

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] • Status Register: [2] [3]
SmartReflex Register Manual • SmartReflex Register Summary: [4]

Table 3-1484. LVTNVALUERECIPROCAL

Address Offset	0x0000 004C		
Physical Address	0x4A0D 904C 0x4A0D B04C 0x4A0D D04C	**Instance**	SMARTREFLEX_MPU SMARTREFLEX_MM SMARTREFLEX_CORE
Description	The reciprocal of the SenN and SenP values used in error generation (LVT)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SENPGAIN				SENNGAIN				SENPRN								SENNRN							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved bits.	R	0x00
23:20	SENPGAIN	The gain value for the LVT SenP reciprocal.	RW	0x0
19:16	SENNGAIN	The gain value for the LVT SenN reciprocal.	RW	0x0
15:8	SENPRN	The scale value for the LVT SenP reciprocal.	RW	0x00
7:0	SENNRN	The scale value for the LVT SenN reciprocal.	RW	0x00

Table 3-1485. Register Call Summary for Register LVTNVALUERECIPROCAL

Voltage-Management Functional Description • SmartReflex Submodules: [0] [1] [2] [3] • SmartReflex Parameters Set After Silicon Characterization: [4] [5] [6] [7]
PRCM Module Programming Guide • SmartReflex Module Initialization: [8] [9] [10] [11]
SmartReflex Register Manual • SmartReflex Register Summary: [12]

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Dual Cortex-A15 MPU Subsystem

This chapter describes the dual Cortex™-A15 MPU subsystem.

Topic **Page**

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4.3	Dual Cortex-A15 MPU Subsystem Functional Description	1066
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4.1 Dual Cortex-A15 MPU Subsystem Overview

4.1.1 Introduction

The dual Cortex™-A15 microprocessor unit (MPU) subsystem serves the applications processing role by running the high-level operating system (HLOS) and application code. The MPU subsystem is based on the symmetric multiprocessor (SMP) architecture, and thus it delivers high performance and optimal power management, debug, and emulation capabilities.

The MPU subsystem incorporates two Cortex-A15 MPU cores (MPU_C0 and MPU_C1), individual level 1 (L1) caches, level 2 (L2) cache (L2CACHE_MPU) shared between them, and various other shared peripherals. To aid software development, the processor cores are kept cache-coherent with each other and with the L2 cache.

The MPU subsystem provides a high-performance computing platform with high peak-computing performance and low memory latency, while also supporting a configuration to shut off one core and run the other at low voltage and low frequency to achieve low-power operation.

Figure 4-1 is a high-level block diagram of the MPU subsystem.

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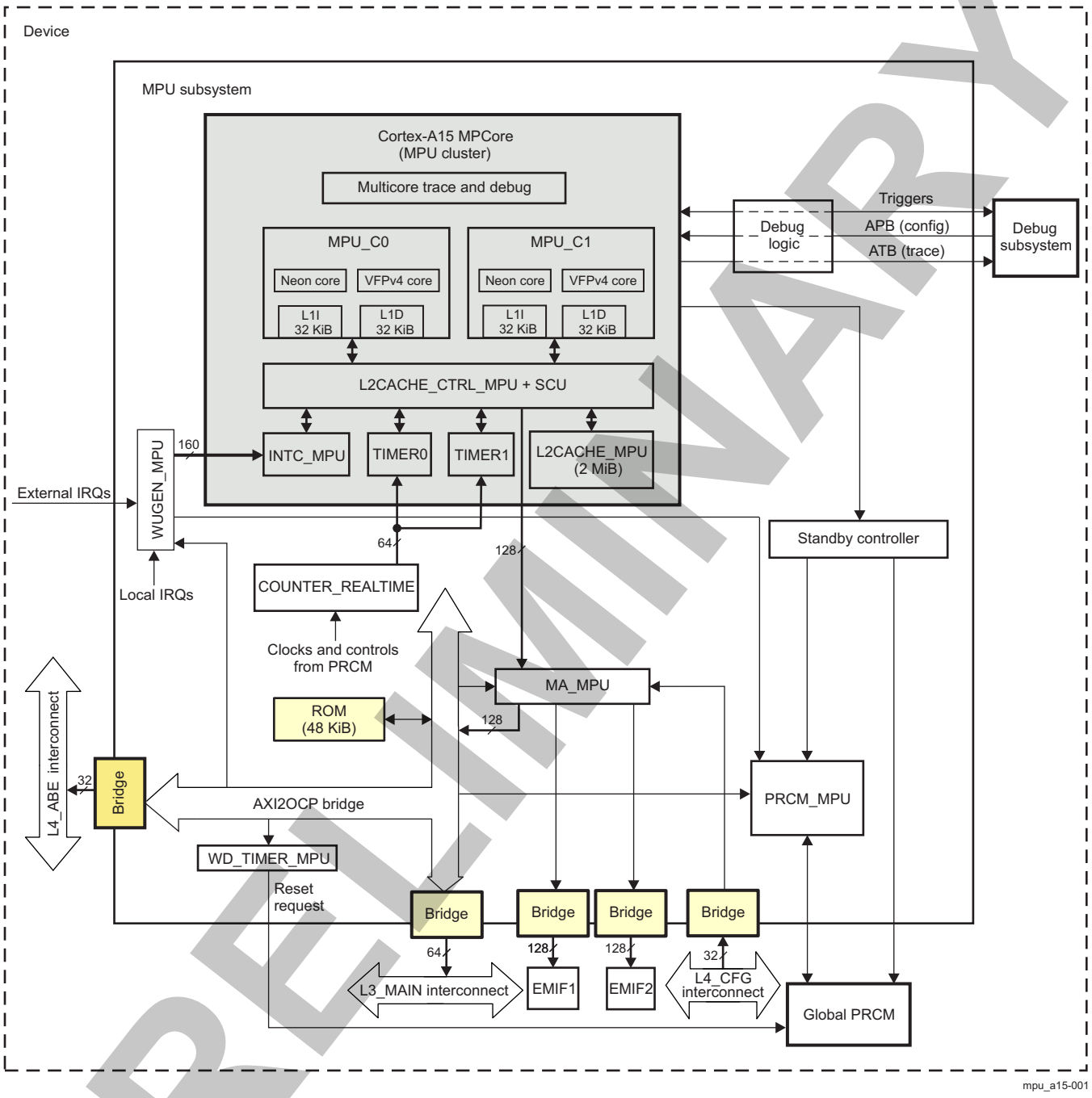
Figure 4-1. MPU Subsystem Overview



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4.1.2 Features

The MPU subsystem integrates the following:

- ARM®Cortex-A15 MPCore™ (MPU cluster)
  - Two Cortex-A15 MPU cores (revision r2p2, SMP architecture), each of them having the following features:
    - Superscalar, dynamic multi-issue technology
      - Out-of-order (OoO) instruction dispatch and completion
      - Dynamic branch prediction with branch target buffer (BTB), global history buffer (GHB), and 48-entry return stack
      - Continuous fetch and decoding of three instructions per clock cycle
      - Dispatch of up to four instructions and completion of eight instructions per clock cycle
      - Provides optimal performance from binaries compiled for previous ARM processors
      - Five execution units handle simple instructions, branch instructions, Neon™ and floating point instructions, multiply instructions, and load and store instructions.
      - Simple instructions take two cycles from dispatch, while complex instructions take up to 11 cycles.
      - Can issue two simple instructions in a cycle
      - Can issue a load and a store instruction in the same cycle
    - Integrated Neon processing engine to include the ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
    - Includes VFPv4-compatible hardware to support single- and double-precision add, subtract, divide, multiply and accumulate, and square root operations
    - Extensive support to accelerate virtualization using a hypervisor
    - 32-KiB L1 instruction (L1I) and 32-KiB L1 data (L1D) cache:
      - 64-byte line size
      - 2-way set associative
    - Memory management unit (MMU):
      - Two-level translation lookaside buffer (TLB) organization
        - First level is an 32-entry, fully associative micro-TLB implemented for each of instruction fetch, load, and store.
        - Second level is a unified, 4-way associative, 512-entry main TLB
      - Supports hardware TLB table-walk for backward-compatible and new 64-bit entry page table formats
      - New page table format can produce 40-bit physical addresses
      - Two-stage translation where first stage is HLOS-controlled and the second level may be controlled by a hypervisor. Second stage always uses the new page table format
  - Integrated L2 cache (L2CACHE_MPU) and snoop control unit (SCU):
    - 2-MiB of unified (instructions and data) cache organized as 16 ways of 2048 sets of 64-byte lines
    - Redundant L1 data (cache) tags to perform snoop filtering (L1 instruction cache tags are not duplicated)
    - Operates at Cortex-A15 MPU core clock rate
    - Integrated L2 cache controller (L2CACHE_CTRL_MPU):
      - Sixteen 64-byte line buffers that handle evictions, line fills and snoop transfers
      - One 128-bit AMBA4 Coherent Bus (AXI4-ACE) port
      - Auto-prefetch buffer for up to 16 streams per core and detecting forward and backward strides
      - L1 cache coherency between the MPU cores is maintained by the L2 cache controller, which

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also serves as a snoop controller.
    - SCU ensures memory coherency between the two MPU cores
  - Generalized interrupt controller (GIC, also referred to as INTC_MPU): An interrupt controller (INTC) supplied by ARM. The single GIC in the MPU cluster routes interrupts to each of the MPU cores. The GIC supports:
    - Number of shared peripheral interrupts (SPI): 160
    - Number of software generated interrupts (SGI): 16
    - Number of CPU interfaces: 2
    - Virtual CPU interface for virtualization support. This allows the majority of guest operating system (OS) interactions with the GIC to be handled in hardware, but with physical interrupts still requiring hypervisor intervention to assign them to the appropriate virtual machine.
  - Integrated timer counter and one timer block per MPU core
  - ARM CoreSight™ debug and trace modules. For more information, see Chapter 29, *On-Chip Debug Support*.
- AXI2OCP bridge (local interconnect):
  - Connected to Memory Adapter (MA_MPU), which routes the non-EMIF address space transactions to AXI2OCP
  - Single request multiple data (SRMD) protocol on L3_MAIN port
  - Multiple targets:
    - 64-bit port to the L3_MAIN interconnect. Interface frequency is 1/4 or 1/8 of core frequency
    - 32-bit port to audio back-end (ABE): This enables direct connection between ARM microprocessor and the ABE module to reduce power consumption during long audio playback. ABE interface frequency is 1/8 or 1/16 of core frequency
    - ROM
    - Internal MPU subsystem peripheral targets, including Memory Adapter LISA Section Manager (MA_LSM), wake-up generator (WUGEN_MPU), and local PRCM module (PRCM_MPU) configuration
    - Internal AXI target, CoreSight System Trace Module (CS_STM)
- Memory adapter (MA_MPU): Helps decrease the latency of accesses between the L2CACHE_MPU and the two EMIFs (EMIF0 and EMIF1) by providing a direct path between the MPU subsystem and the EMIFs:
  - Connected to 128-bit AMBA4 interface of MPU cluster
  - Direct 128-bit interface to each of EMIF0 and EMIF1
  - Interface speed between MPU cluster and MA_MPU is at half-speed of MPU cluster internal core frequency
  - Programmable one-fourth (default value) or one-sixth speed interface (versus reference clock) to the EMIFs
  - Performs interleaving functions to load-balance the activities across the two EMIFs
  - Uses firewall logic to check access rights of incoming addresses
- Local PRCM (PRCM_MPU):
  - Handles MPU_C0 and MPU_C1 power domains
  - Supports SR3-APG (SmartReflex3 Automatic Power Gating) power management technology inside the MPU cluster
  - MPU subsystem has six power domains
- Wake-up generator (WUGEN_MPU)
  - Responsible for waking up the MPU cores
  - Used by the ROM code and OS during SMP boot
- Standby controller: Handles the power transitions inside the MPU subsystem
- Realtime (master) counter (COUNTER_REALTIME): Produces the count used by the private timer

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peripherals in the MPU cluster

- Watchdog timer (WD_TIMER_MPU): Used to generate a watchdog reset request to global PRCM
- On-chip ROM: MPU_C0 (the master MPU core) can boot from this memory. The ROM size is 48-KiB, and the address range is from 0x4003 8000 to 0x4004 3FFF. For more information, see Chapter 28, *Initialization*.
- Interfaces:
  - 128-bit interface to each of EMIF0 and EMIF1
  - 64-bit master port to the L3_MAIN interconnect
  - 32-bit master port to ABE for enabling direct connection between the Cortex-A15 MPCore and the ABE module to reduce power consumption during long audio playback
  - 32-bit slave port from the L4_CFG_EMU interconnect (debug subsystem) for configuration of the MPU subsystem debug modules
  - 32-bit slave port from the L4_CFG interconnect for memory adapter firewall (MA_MPU_NTTP_FW) configuration
  - 32-bit ATB output for transmitting debug and trace data
  - 160 peripheral interrupt inputs

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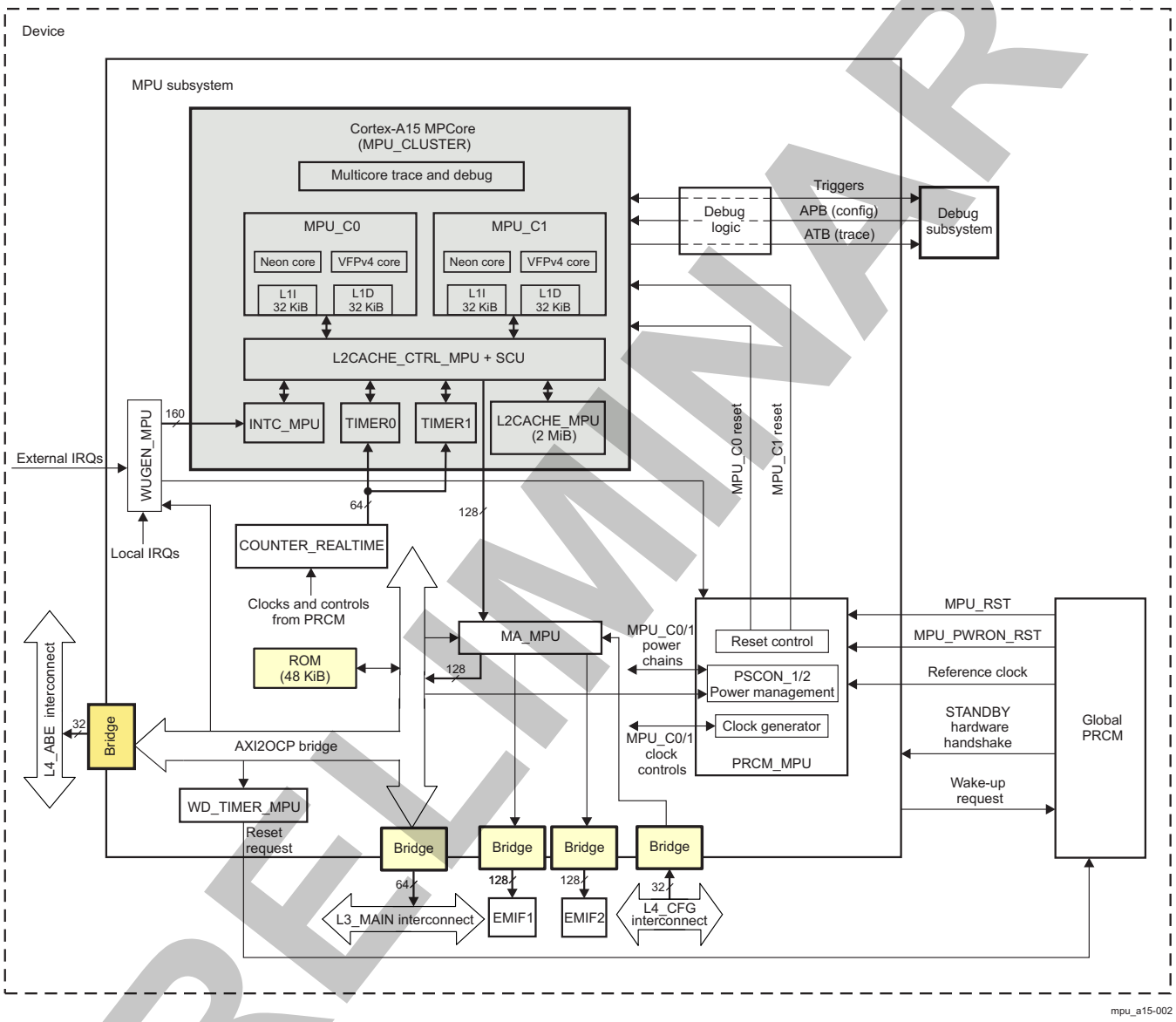
4.2 Dual Cortex-A15 MPU Subsystem Integration

This section describes the integration of the module in the device, including information about clocks, resets, and hardware requests.

Figure 4-2 shows the MPU subsystem integration.

Figure 4-2. MPU Subsystem Integration



NOTE: Some debug, trace, and emulation features are implemented in the MPU subsystem. For more information about debug and emulation features, see Chapter 29, *On-Chip Debug Support*.

NOTE: For more information about the STANDBY hardware handshake and the wake-up request, see Module-Level Clock Management, in Chapter 3, *Power, Reset, and Clock Management*.

Table 4-1 and Table 4-2 summarize the integration of the module in the device.

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Table 4-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
MPU	PD_MPU	L3_MAIN

Table 4-2. Clocks and Resets

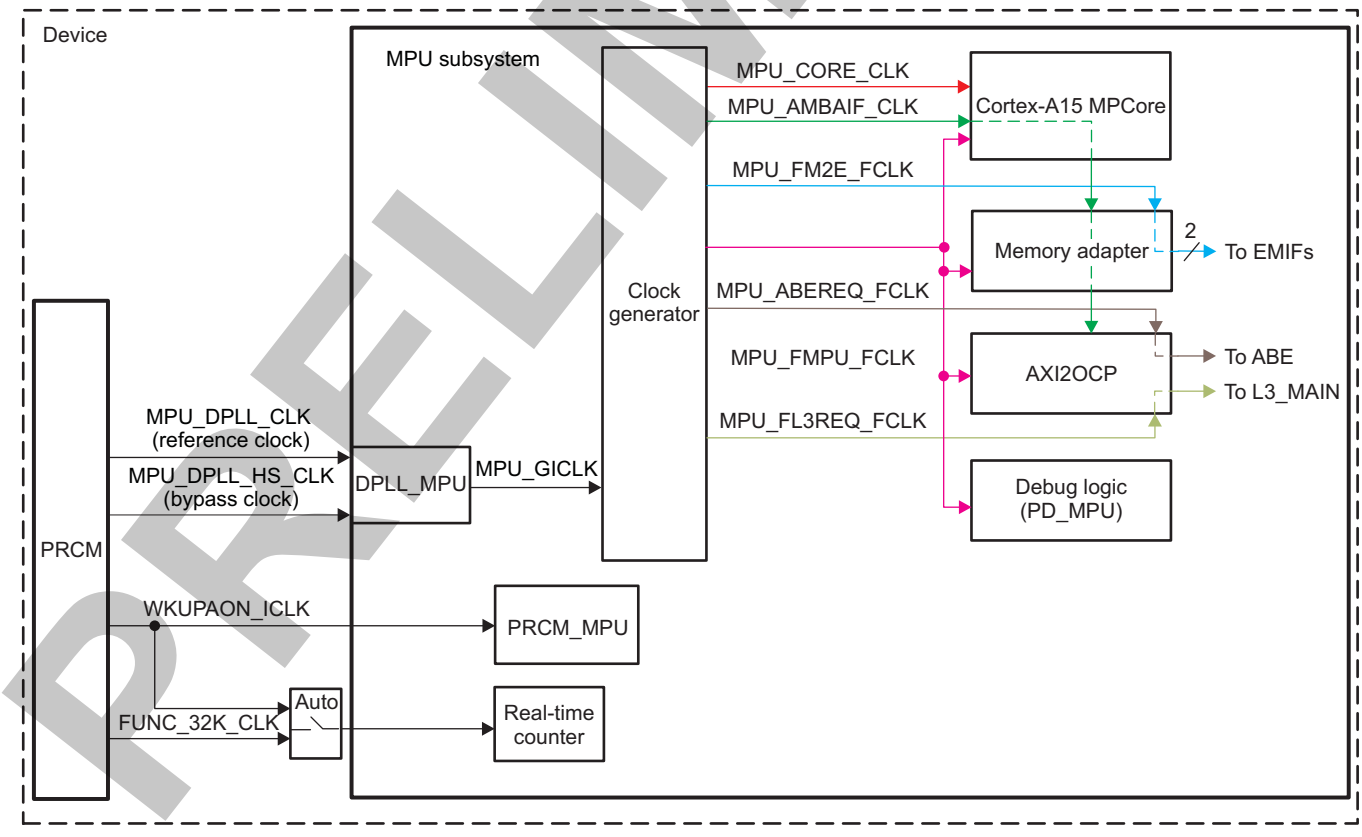
			Clocks	
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MPU	MPU_DPLL_CLK	MPU_DPLL_CLK	PRCM	Reference clock for the MPU clock generator
			Resets	
MPU	MPU_PWRON_RST	MPU_PWRON_RST	PRCM	Power-on reset (POR) for all the modules inside the MPU system power domain; nonretention
	MPU_RST	MPU_RST	PRCM	Warm reset for all the modules inside the MPU system power domain; nonretention

4.2.1 Clock Distribution

The Cortex-A15 MPU clock generator is fed by the MPU digital phase-locked loop (DPLL), which can be gated off by the global power, reset, and clock management (PRCM) module when system power domain is in a low-power state. There is a global clock gating for each CPU. Because of the DPLL_MPU, the MPU subsystem is asynchronous from the rest of the device.

Figure 4-3 shows the MPU subsystem clocking scheme.

Figure 4-3. MPU Subsystem Clocking Scheme



The clock generator generates the following clocks from the DPLL_MPU output clock (MPU_GICLK):

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- MPU_CORE_CLK
- MPU_AMBAIF_CLK
- MPU_FMPU_FCLK
- MPU_FL3REQ_FCLK
- MPU_ABEREQ_FCLK
- MPU_FM2E_FCLK

MPU_CORE_CLK is directly derived (no hardware dividing) from the DPLL_MPU output clock (that is, MPU_CORE_CLK = MPU_GICLK). The other clocks are derived via dividers.

Table 4-3 shows the supported frequency values for MPU subsystem clocks at different OPPs.

Table 4-3. MPU Subsystem Clocks Frequency Value Versus OPP

Clocks (Derived From DPLL_MPU)	OPP_LOW	OPP_NOM	OPP_HIGH	OPP_SPEEDBIN
MPU_CORE_CLK (f)	See (1)	See (1)	See (1)	See (1)
MPU_AMBAIF_CLK	f/2	f/2	f/2	f/2
MPU_FMPU_FCLK	f/4	f/4	f/4	f/4
MPU_FL3REQ_FCLK	f/4	f/4	f/8	f/8
MPU_ABEREQ_FCLK	f/8	f/8	f/16	f/16
MPU_FM2E_FCLK	f/4	f/4	f/6	f/6

(1) See device *Data Manual* for information about frequency value

NOTE: For more information about the DPLL_MPU, see DPLL_MPU Description, in Chapter 3, *Power, Reset, and Clock Management*.

The two MPU cores cannot be clocked at different frequencies.

The realtime counter (COUNTER_REALTIME) is clocked by either WKUPAON_ICLK or FUNC_32K_CLK clocks, provided by the global PRCM module. By default, WKUPAON_ICLK is used as a COUNTER_REALTIME clock. When the MPU subsystem goes to standby mode, the counter automatically switches to a low-power mode using the 32-kHz clock (FUNC_32K_CLK).

4.2.2 Reset Distribution

Resets to the MPU subsystem are provided by the global PRCM module and controlled by the local PRCM_MPU module.

For more information about the power domains in the MPU subsystem, see Section 4.3.7.1, *Power Domains*. Figure 4-4 shows the reset scheme of the MPU subsystem.

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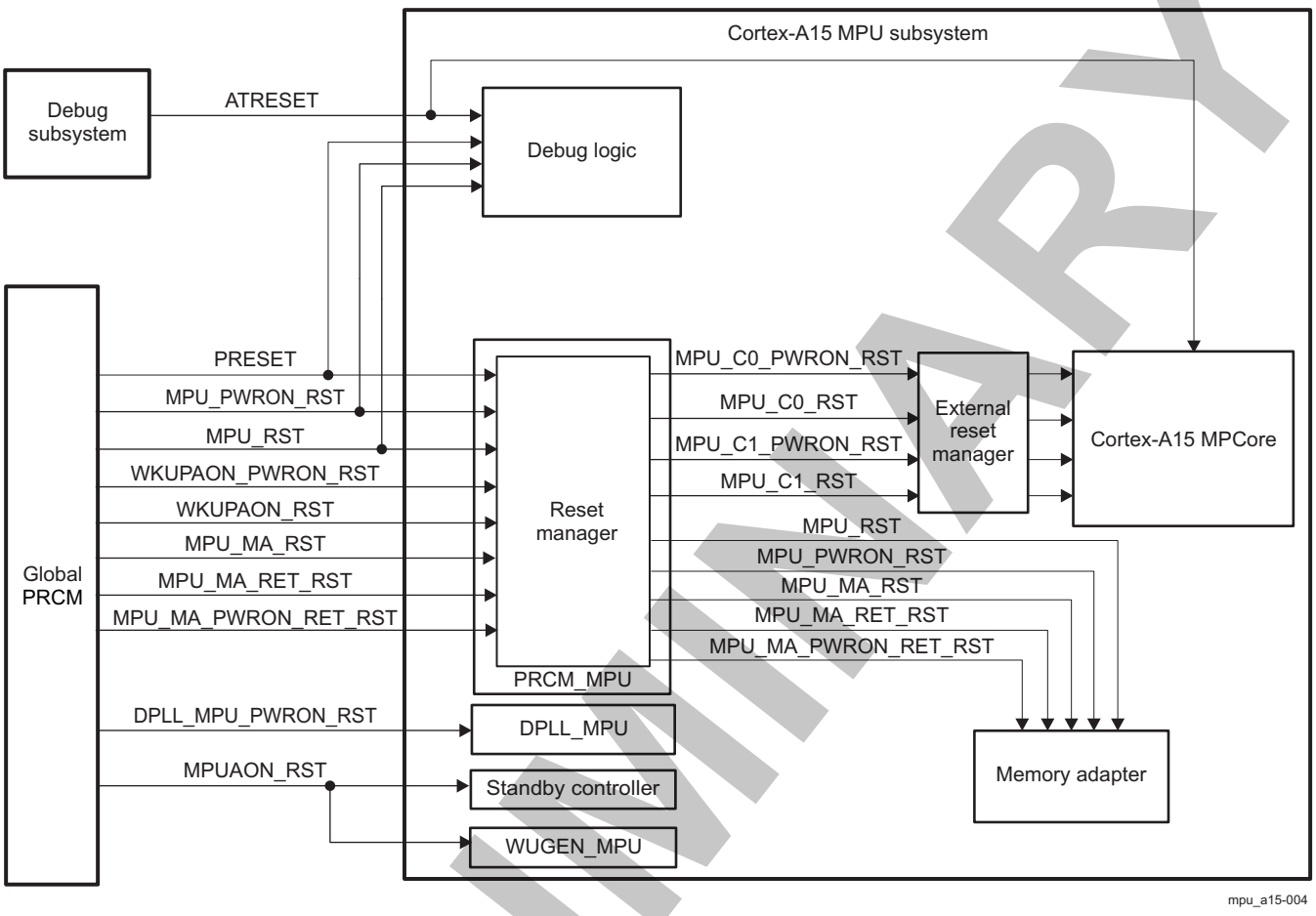
Figure 4-4. MPU Subsystem Reset Scheme



All eight external resets that are input to the local PRCM signals are active low. All 11 external reset input signals are driven by the global PRCM, except the ATRESET reset signal, which is driven by the device debug subsystem. Four internal reset signals are generated by the local PRCM module.

ATRESET is asserted at initial device power up and resets the debug and trace modules. ATRESET affects the debug logic of the MPU cluster and its cores.

The PRESET reset signal resets the debug logic in the Cortex-A15 MPU and ARM MPU cores.

The WKUPAON_PWRON_RST reset signal is a global cold reset for the wake-up logic and resets the wake-up domain logic (the PSCON modules) in the local PRCM module. A cold reset is typically asserted when power is initially applied to the system. The user can check whether this reset event has occurred by reading the PRM_RSTST[0] GLOBAL_COLD_RST bit.

The WKUPAON_RST reset signal is a global warm reset that resets the wake-up domain logic (the PSCON modules) in the local PRCM module. Warm reset is typically used to reset a system that has been operating for some time. The user can check whether this reset event has occurred by reading the PRM_RSTST[1] GLOBAL_WARM_RST bit.

The DPLL_MPU_PWRON_RST reset signal resets the DPLL_MPU.

The MPUAON_RST reset signal resets the MPU always-on domain: the standby controller and the WUGEN_MPU. The user can check whether the reset has occurred by reading the WKG_CONTROL_0[15] DOMAIN_RST bit for MPU_C0 and the WKG_CONTROL_1[15] DOMAIN_RST bit for MPU_C1.

The MA_MPU has five incoming reset signals:

- MPU_RST

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- MPU_PWRON_RST
- MPU_MA_RST
- MPU_MA_RET_RST
- MPU_MA_PWRON_RET_RST

These five reset signals are driven by the Cortex-A15 MPU local reset manager and are active low.

The local PRCM module provides two reset signals for each CPU:

- The MPU_C0_RST and MPU_C1_RST reset signals are warm reset events. These reset signals initialize most of the ARM MPU cores, except the debug logic (breakpoints and watchpoints are retained during this reset). The user can check whether these reset events have occurred by reading the RM_CPUx_RSTCTRL[0] RST bit.
- The MPU_C0_PWRON_RST and MPU_C1_PWRON_RST reset signals are cold and debug reset events.

For more information about clocks, resets, and power domains, and the MPU_PWRON_RST and MPU_RST reset signals, see Chapter 3, *Power, Reset, and Clock Management*.

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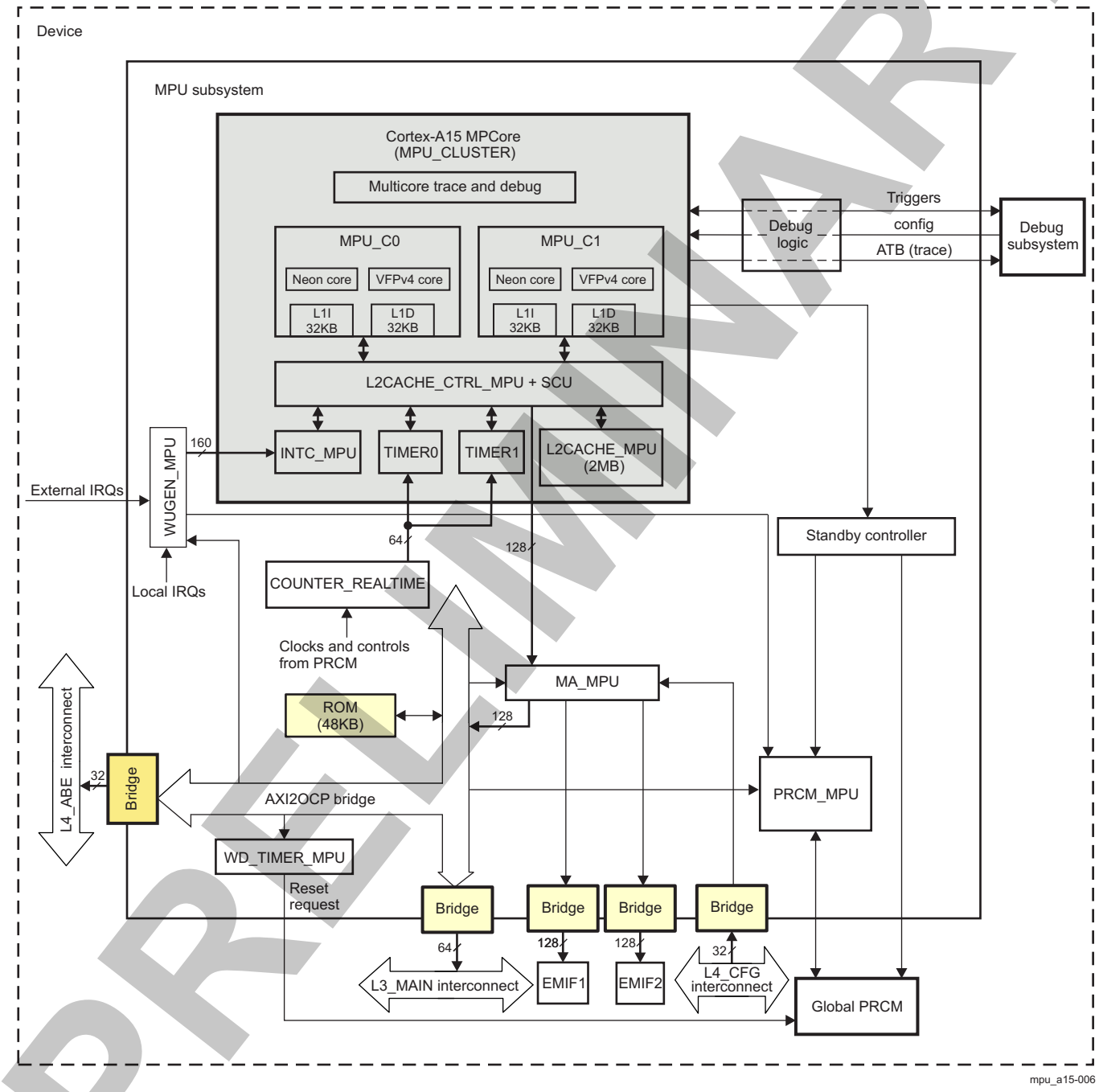
4.3 Dual Cortex-A15 MPU Subsystem Functional Description

4.3.1 MPU Subsystem Block Diagram

Figure 4-5 is the block diagram of the MPU subsystem.

Figure 4-5. MPU Subsystem Block Diagram



4.3.2 Cortex-A15 MPCore (MPU Cluster)

The MPU cluster consists of:

- Two CPUs (dual-core configuration), including:
  - ARM version 7 ISA™: Standard ARM instruction set plus Thumb®-2 , Jazelle® RCT, and Jazelle

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DBX Java™ accelerator
  - Neon SIMD coprocessor and VFPv4
  - 12-stage in-order MPU core pipeline
  - 128-bit-wide instruction fetch allows fetching up to four instructions/cycle
  - 32 KiB/32 KiB instruction and data cache for each MPU core
  - Complex Execution Unit (FPU) per MPU core
  - 32-entry fully-associative micro-TLB each for instruction and data per MPU core
  - 512-entry 4-way set-associative unified TLB per MPU core
- Unified L2 cache control including tags
- Interrupt controller (INTC_MPU)
  - Supports 160 hardware interrupts. For more information about interrupt mapping, see Interrupt Controllers.
- One timer and watchdog timer per MPU core
- Internal APB bridge that connects to the APB port of each MPU core

The major interfaces of the MPU cluster are:

- Single AXI master supporting 128-bit interface
- System coherency supported through the AXI4 ACE interface
- An ATB port (for processor trace)
- An APB port
- Interrupt request lines

NOTE: The device supports only the following ACE configurations:
- **AXI3** mode (default). In this configuration, barrier transactions are not issued on the AMBA4 interface.
- **ACE non-coherent, no L3** mode. In this configuration, barrier transactions are issued on the AMBA4 interface.

For more information, see Section 4.3.8, *MPU Subsystem AMBA Interface Configuration*.

NOTE: The MPU subsystem does not implement the ACP port to support hardware coherency with external master.

The MPU subsystem implementation of Cortex-A15 MPCore does not include ECC/parity support for the L1 or L2 caches.

4.3.2.1 MPU L2 Cache Memory System

The MPU subsystem implements an L2 memory system. This memory system consists of an L2 cache and associated L2 cache controller. The MPU L2 cache controller runs at full-CPU speed and is configured to have one 128-bit master port. The L2 cache controller is configurable via CP15 registers and is tightly coupled to the L1 memory system. The MPU L2 memory system supports ARM Instruction Set Architecture (v7).

MPU L2 supports hardware cache coherency, but is used in a limited way in the device. Because the rest of the system does not support coherency with the MPU L2 cache, software coherence is required.

The L2 cache size on the MPU subsystem is 2 MiB. The cache is configured as 16-way set associative, with 64-B line size. The L2 cache controller performs critical word-first-refilling with a random or pseudo-random cache replacement policy.

The L2 includes logic to support cache event monitoring. The events being monitored are routed to the hardware debug (MPUHWDBGOUT[31:0]) port. The mapping of these events to the MPUHWDBGOUT[31:0] port is described in Section 18.4.11.5.1, *MPU Subsystem Observable Signals*, Chapter 18, *Control Module*.

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The L2 can be configured to generate interrupts on error conditions or event counter overflow/increment. The L2 interrupt (MPU_CLUSTER_IRQ_AXI) is routed to interrupt line MPU_IRQ_3. When an interrupt occurs, software may look at corresponding interrupt register to determine the source of the interrupt.

4.3.2.1.1 MPU L2 Cache Architecture

The main features of the L2CACHE_MPU are:

- 2048-KiB 16-way set-associative unified instruction/data cache
- 9-stage L2 pipeline
- L2 hit latency of 12 cycles
- Fixed line length of 64-bytes (16 words)
- L1 inclusive
- Physically indexed and tagged
- 16-way set-associative (maximum)
- Bank partitions to support streaming Neon loads and simultaneous (two) L2 requests
- Exclusive-D L2 cache fill policy
- Global-random replacement strategy
- Four dirty bits per cache line to minimize traffic to L3
- Low-leakage sleep mode (retention until accessed)
- Cache redundancy and repair

4.3.2.1.2 MPU L2 Cache Controller

The main features of the L2CACHE_CTRL_MPU are:

- Single 128-bit AXI4 master port interface
- Tightly coupled L2/SCU for better L2 hit latency
- Nonblocking: Supports hit-under-miss and miss-under-miss for Neon requests
- Performs critical data first refilling
- Supports the following cache modes:
  - Write-through, read allocate
  - Write-back, read allocate, and write allocate
- Supports write-combining to two independently tagged quad-words
- 12 × 128-bit write buffers to buffer subblock writes (per MPU core)
- 12 × 128-bit ACP write buffer (shared across MPU cores)
- 16-entry × 512-bit victim buffers (shared across MPU cores)
- Separate 128-bit interfaces to the I-side and the D-side:
  - Four beat (128-bit) transfers to refill L1 from L2 (or 128-bit AXI)
  - Eight beat (64-bit) transfers to refill L1 from AXI
- 128-bit subblock write and copy-back interface on the D-side
- Outstanding transactions on the AXI4 master port:
  - 16 read
  - 16 write
- Performs hardware table walk using the L2 unified TLB

For more information about Cortex-A15 MPCore, see the ARM *Cortex-A15 MPCore Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

For more information about debug and emulation features in the MPU subsystem, see Chapter 29, *On-Chip Debug Support*.

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4.3.3 AXI2OCP

AXI2OCP provides a protocol bridge between buses and also serves as a small local interconnect to handle traffic to the L3_MAIN interconnect and ABE OCP buses and local configuration registers in the MPU subsystem.

Main features:

- Connects to the L3_MAIN interconnect through a 64-bit port. The interface frequency is configurable between one fourth (default value) and one eighth of the MPU_DPLL_CLK clock signal frequency. This is programmable in the CM_MPU_MPU_CLKCTRL[25:24] CLKSEL_EMIF_DIV_MODE bit.
- Connects to the ABE through a 32-bit port. The interface frequency is configurable between one eighth (default value) and one sixteenth of the MPU_DPLL_CLK clock signal frequency. This is programmable in the CM_MPU_MPU_CLKCTRL[26] CLKSEL_ABE_DIV_MODE bit.
- Connects to the CS_STM module through a 32-bit AXI interface (for software instrumentation)
- Connection to the following modules for register configuration:
  - MA_MPU
  - PRCM_MPU
  - WUGEN_MPU
- Contains internal configuration register related to the MA_MPU function (MA_PRIORITY)
- Supports memory barrier instruction
- Supports single-request-multiple-data (data handshaking) burst mode to pipeline requests
- Supports multiple outstanding requests
- Supports posted and nonposted write transactions, based on the attributes of the transactions coming from the Cortex-A15 processor. Software can override all writes from the local interconnect to the L3 interconnect to be nonposted, regardless of the attributes of the transactions coming from the ARM Cortex-A15 processor, by setting the FORCEWRNP[0] MPUFORCEWRNP bit to 0x1. For the register description, see Chapter 18, *Control Module*.

NOTE: For the description of the CM_MPU_MPU_CLKCTRL register, see Chapter 3, *Power, Reset, and Clock Management*.

4.3.4 Memory Adapter

To decrease the latency of accesses between the MPU L2 cache, and the two EMIF modules, a direct path between the MPU subsystem and the EMIFs is created. To support the direct path between the MPU subsystem and the EMIFs, a memory adapter (MA_MPU) module is instantiated. The MA_MPU splits the incoming (from L2 cache) AXI4 traffic into AXI2OCP and the EMIF accesses. The AXI2OCP accesses are sent to the MA_MPU A2O ports. The EMIF accesses are optionally interleaved between the two EMIF ports. Mandatory firewall checks are performed on all accesses to the EMIFs.

The main features of the MA_MPU are:

- Splits accesses between the AXI2OCP and the EMIF
- Input from L2 cache and output to AXI2OCP is AMBA4-compatible and runs at Cortex-A15 CPU/2 frequency.
- Supported read response interleaving on A2O port
- Parallel processing of reads and writes
- Support for narrow bursts
- Supports 4 × 128-bit line fills and eviction with critical word first
- Supports barrier instructions on normal read and write channels
- Direct 128-bit interface each to EMIF1 and EMIF2:
  - Single request multiple data
  - No write response on posted writes
- Programmable one-fourth (default value) or one-sixth speed interface to the EMIFs (EMIF1 and

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EMIF2). This is selected by the CM_MPU_MPU_CLKCTRL[25:24] CLKSEL_EMIF_DIV_MODE bit.

- Performs interleaving functions to load-balance the activities across the two EMIFs
- Uses firewall logic to check access rights of incoming addresses. The firewall on both EMIFs supports:
  - Configurable number of regions with fixed priority
  - Access support for up to eight execution domains
  - Busy indicator during reconfiguration
- Blocked read and write access to the EMIF for all accesses failing authorization checks
- Burst wrap for single cache line fills
- Supports boot from EMIF space
- Supports 8 GiB of memory
- MA_LSM supports interleaving for 2 GiB of shared memory:
  - Programmable multizone DRAM mapping and interleaving configuration
  - Supports four prioritized sections for defining configuration regions within the external memory
  - Supports interleaving at 128-, 256-, and 512-byte boundaries
- Fixed interleaving for extended 6 GiB of MPU-only memory
- Supports standard disconnect and idle protocols for independent powering down of the MA_MPU and both EMIFs (the EMIF must be powered down or up as a pair)
- Probe interface for performance monitoring of the EMIF ports
- Eleven outstanding reads and 16 outstanding writes
- Supports exclusive accesses used for MPU internal synchronization
- Provides watchpoint capability on AXI bus. For more information, see Chapter 29, *On-Chip Debug Support*.

Figure 4-6 shows the integration of the MA_MPU in the device.

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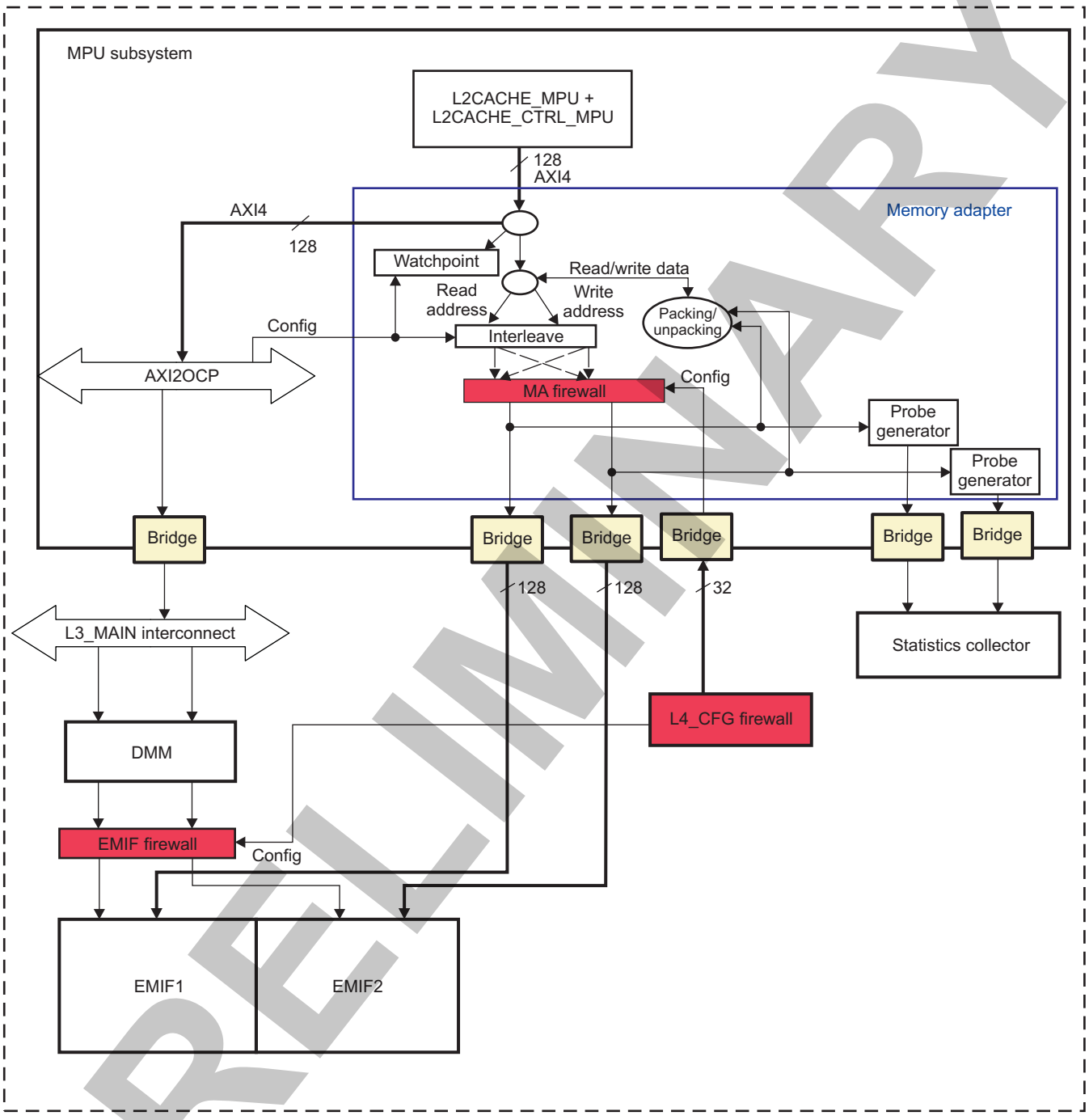
Figure 4-6. MA_MPU Block Diagram



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4.3.4.1 MA_MPU Functional Description

4.3.4.1.1 AXI Input Interface

The AXI input is driven from the single external port of the L2 cache. The incoming accesses are directed to the AXI2OCP module through the A2O port or begin their processing for a potential EMIF access. The routing of accesses is based on the AXI address and the EMIF boot input (pi_emifboot).

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Table 4-4 lists the AXI access memory mapping. If the accesses are targeted for the AXI2OCP, then they are registered and sent to the A2O port without any alterations in its attributes (size, ID, etc.). The reserved space in the lower order memory area is a result of providing 8 GiB of continuous space for all the nonaliased regions.

The EMIF memory space is broken into eight 1-GiB sections, which are denoted *emif(a)* through *emif(h)*. This partitioning helps to specify the aliasing of several memory ranges. It also aids in the discussion of how the MPU memory space is mapped into the physical EMIF space.

It is expected that the OS uses either the lower 2-GiB space and the lower aliased address of emif(a) and (b), or the continuous 8-GiB space and the upper aliasing of the emif(a) and (b) for all EMIF accesses.

Table 4-4. AXI Access Memory Mapping

Region Name	Start Address	End Address	Interleaving	MA_MPU Action
Boot space	0x00 0000 0000	0x00 000F FFFF	Default	Sent to Firewall/EMIF, if pi_emifboot = 1
			N/A	Sent to A2O port, if pi_emifboot = 0
Non-emif	0x00 0010 0000	0x00 7FFF FFFF	N/A	Sent to A2O port
Emif(a)	0x00 8000 0000	0x00 BFFF FFFF	Programmable	Aliased to address range 0x02 8000 0000–0x02 FFFF FFFF
Emif(b)	0x00 C000 0000	0x00 FFFF FFFF	Programmable	
Reserved	0x01 0000 0000	0x01 FFFF FFFF	N/A	DECERR returned
Emif(c)	0x02 0000 0000	0x02 3FFF FFFF	Fixed	Sent to Firewall/EMIF
Emif(d)	0x02 4000 0000	0x02 7FFF FFFF	Fixed	Sent to Firewall/EMIF
Emif(a)	0x02 8000 0000	0x02 BFFF FFFF	Programmable	Sent to Firewall/EMIF
Emif(b)	0x02 C000 0000	0x02 FFFF FFFF	Programmable	Sent to Firewall/EMIF
Emif(g)	0x03 0000 0000	0x03 3FFF FFFF	Fixed	Sent to Firewall/EMIF
Emif(h)	0x03 4000 0000	0x03 7FFF FFFF	Fixed	Sent to Firewall/EMIF
Emif(e)	0x03 8000 0000	0x03 BFFF FFFF	Fixed	Sent to Firewall/EMIF
Emif(f)	0x03 C000 0000	0x03 FFFF FFFF	Fixed	Sent to Firewall/EMIF
Reserved	0x04 0000 0000	0xFF FFFF FFFF	N/A	DECERR returned

4.3.4.1.2 Interleaving

To load-balance the activities across the two EMIFs, interleaving is used. For the lower 2-GiB address space, which is used by the system and the MPU, a wide range of interleaving options are provided. Because the EMIF memories are accessible by the MPU subsystem through MA_MPU and by the L3_MAIN interconnect through the DMM, the same interleaving scheme must be used in both paths. To ensure compatibility, the interleaving function is implemented by a scaled down version of the LISA Section Manager (LSM), which implements the interleaving function in the DMM.

The high-order memory space, which is accessible only from the MPU subsystem, uses a simple fixed-interleaving scheme, which can be disabled. Heavy use in high memory space under noninterleaved configuration affects the balancing of the system access in lower-order memory.

4.3.4.1.2.1 High-Order Fixed Interleaving Model

The memory address ranges *emif(c)* through *emif(h)* can be interleaved between the two EMIFs by setting the MA_PRIORITY[8] HIMEM_INTERLEAVE_UN bit to 0x1. If enabled, the interleaving occurs on a 256-byte boundary.

Figure 4-7 and Figure 4-8 show how the predefined emif sections are mapped into the EMIF. The LISA configuration can be programmed to allow emif(a) and emif(b) address ranges to be remapped anywhere in EMIF1 or EMIF2. Restricting them to the locations 0x0000 0000–0x7FFF FFFF allows the fully programmable regions to co-exist with the fixed interleaving regions without overlap. Although it is not recommended, the user can program the interleaver to map the emif(a) and emif(b) address ranges to the EMIF 0x8000 0000–0xFFFF FFFF location. If this is done, then additional address aliasing exists between emif sections (a/b) and sections (c) through (h).

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NOTE: In fixed interleaving, memory address space 0 is always used.

Figure 4-7. EMIF Partitioning Without High-Order Interleaving

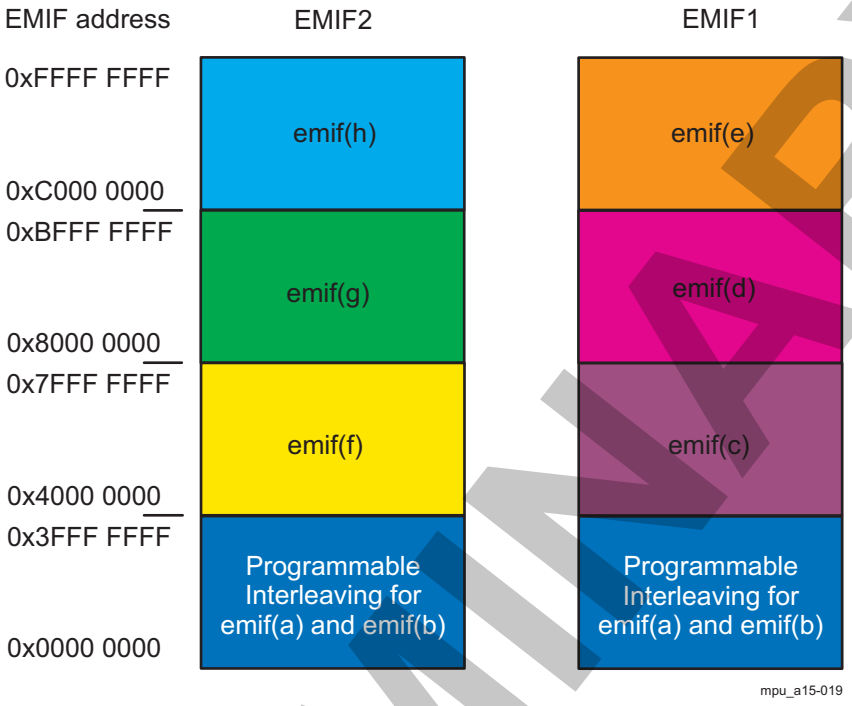
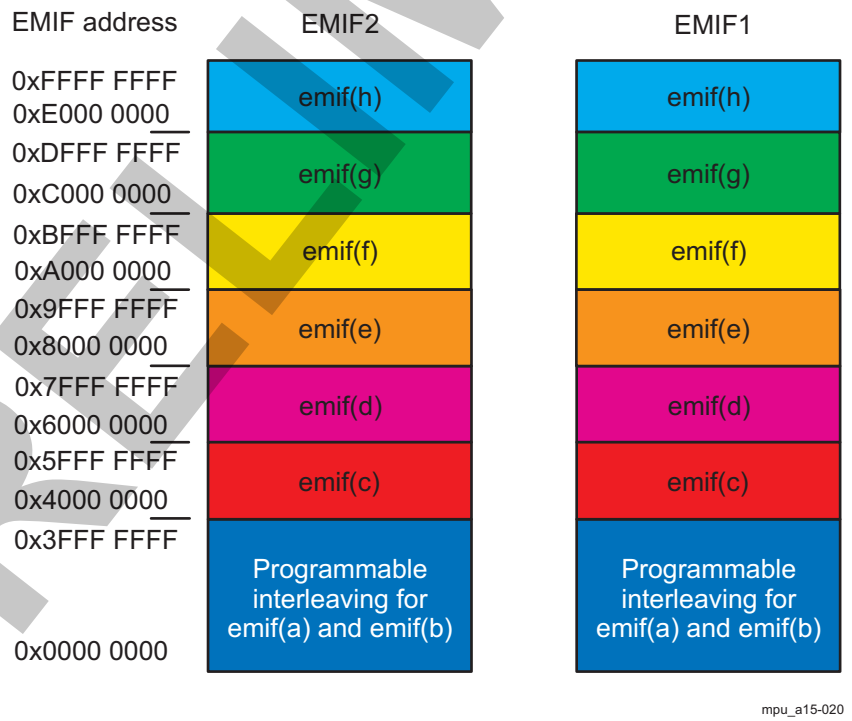


Figure 4-8. EMIF Partitioning With High-Order Interleaving



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4.3.4.1.2.2 Lower 2-GiB Programmable Interleaving Model

For more information about the lower 2-GiB programmable interleaving model of the MA_LSM, see Dynamic Mapping, and Address Mapping in *Dynamic Memory Manager* chapter. When reading, replace DMM with MA_LSM.

4.3.4.1.2.3 Local Interconnect and Synchronization Agent (LISA) Section Manager

The LSM module in the MA_MPU contains one set of registers and two ports. Each port can handle one address translation, provide the interface size, and determine the EMIF mapping. The two ports process read and write addresses simultaneously. The MA_LSM supports four sections.

4.3.4.1.2.4 MA_LSM Registers

Table 4-5 lists the DMM registers that are duplicated locally in the MA_MPU. These registers have the same names except that DMM is replaced by MA_MPU. Software must keep the content of these registers equal to the content of their counterparts in the DMM.

Table 4-5. MA_MPU Registers Duplicated From the DMM Register Map

Register	Type	Width (Bits)	Base Address
MA_LISA_LOCK	RW	32	0x482A F01C
MA_LISA_MAP_i (where i = 0 to 3)	RW	32	0x482A F040–0x482A F04C

For descriptions of the registers, see *Section 15.2.6, DMM Register Manual*, in Chapter 15, *Memory Subsystem*. The only differences are the following reset values of the MA_LISA_MAP_0 register:

- MA_LISA_MAP_0[22:20] SYS_SIZE = 0x1 (32-MiB section)
- MA_LISA_MAP_0[17:16] SDRC_ADDRSPC = 0x1
- MA_LISA_MAP_0[9:8] SDRC_MAP = 0x1

The configuration of the MA_MPU must be programmed by the Cortex-A15 MPU to match the configuration of the DMM during boot. The registers must be locked after initial programming to avoid corruption by application software. When the SM configuration registers are being programmed, there are no interlocks or safeguards to prevent accesses from being processed at the same time. The MA_LISA_LOCK and MA_LISA_MAP_i registers are retained during power down of retention mode.

If an access is made to a region marked as having unused address space or an unmapped SDRC map, no access is made to the EMIF and an error is returned. If an access is made to a region marked as accesses-SDRC-internal-registers, no access occurs to the EMIF and an error is returned. This is because the internal registers are not accessible from this port.

If an access is made to a region that is not mapped to any LISA section, or selects a section with one of the following programmations, then no access is made to the EMIF and an error is returned on the AXI port:

- SDRC_MAP field equal to UNMAPPED
- SDRC_ADDRSPC field equal to INTERNAL REGISTER
- SDRC_ADDRSPC field equal to UNUSED

4.3.4.1.2.5 Posted and Nonposted Writes

On posted writes, a response is returned after all write data is accepted by the MA_MPU and one of the following occurs:

- The request is canceled, because of an interleaving error.
- The request is pushed into the firewall FIFO.

On nonposted writes, a response is not returned until after all write data is accepted by the MA_MPU and one of the following occurs:

- The request is canceled, because of an interleaving error.

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- The request has a firewall violation.
- The associated response is received from the EMIF (access is completed in the EMIF).

When the FORCEWRNP[0] MPUFORCEWRNP bit is set to 0x1, all writes are forced to be converted to nonposted writes (prevents posted writes).

4.3.4.1.2.6 Errors

If the region is marked as unmapped, o targets EMIF internal registers or reserved space, access is blocked and an error response is returned. Such an error occurs on the first half of a potential split access and aborts the entire access at that time. DECERR errors ultimately generate ARM aborts. See the ARM Fault Status Register for more information.

To avoid undefined results, the following program rules must be followed:

- A section cannot be mapped as interleaving (MA_LISA_MAP_i[9:8] SDRC_MAP = 0x3), and the MA_LISA_MAP_i[19:18] SDRC_INTL bit field must be equal to 0x0.
- If the section maps to a single EMIF (MA_LISA_MAP_i[9:8] SDRC_MAP = 0x1 or 0x2), the MA_LISA_MAP_i[7:0] SDRC_ADDR bit field must be aligned to the MA_LISA_MAP_i[22:20] SYS_SIZE bit field (that is, the lower SDRC_ADDR bits must be 0).
- If the section maps to both EMIFs (MA_LISA_MAP_i[9:8] SDRC_MAP = 0x3), the MA_LISA_MAP_i[7:0] SDRC_ADDR bit field must be aligned to MA_LISA_MAP_i[22:20] SYS_SIZE – 1, because the addressable space for each EMIF is half.
- If the section maps to both EMIFs (MA_LISA_MAP_i[9:8] SDRC_MAP = 0x3), the MA_LISA_MAP_i[22:20] SYS_SIZE bit field cannot be 0.

4.3.4.1.3 Statistics Collector Probe Ports

To enable performance monitoring by the debug subsystem, a subset of interconnect signals must be monitored and sent to a statistics collector in the CORE domain. For more information about the statistics collector, see Chapter 29, *On-Chip Debug Support*.

4.3.4.1.4 MA_MPU Firewall

A firewall exists between the interleaving logic and each EMIF port. The firewall checks the address and access qualifiers against the permission attributes for the highest priority region to which the address belongs. If the access fails to get permission, a violation occurs and the fw_func_error or fw_debug_error output is asserted. The failing access is blocked and a slave error response is returned on the MA_MPU port for read and nonposted accesses. For more information about the MA_MPU firewall, see Chapter 14, *Interconnect*.

4.3.4.1.5 MA_MPU Power and Reset Management

The MA_MPU supports a power-down state where the MA_LSM and firewall configurations are retained.

The MA_LSM supports only smart-idle mode.

4.3.5 Realtime Counter (Master Counter)

The realtime counter (COUNTER_REALTIME), also called master counter, is a free-running counter, which is related to real time. It produces the count used by the private timer peripherals in the MPU cluster. The timer counts at a rate of 6.144 million counts per second. Because the device operates on different clocks in different power modes, the master counter shifts operation between clocks, adjusting the increment per clock accordingly to maintain a constant count rate.

COUNTER_REALTIME runs on the PRCM_MPU clock coming from the global PRCM (WKUPAON_ICLK). The two sources for this clock are:

- SYS_CLK: System clock from external source. The supported frequencies are 12, 13, 19.2, 26, 27, and 38.4 MHz.
- ABE_LP_CLK: Clock derived from DPLL_ABE, used in some low-power use cases, runs at 12.288 MHz (DPLL cascading)

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When the MPU subsystem goes to standby mode, the counter automatically switches to a low-power mode using the 32-kHz clock (FUNC_32K_CLK).

Table 4-6 shows the counter increment value for different counter clock frequencies and corresponding register programming.

Table 4-6. COUNTER_REALTIME Increment Values

COUNTER_ REALTIME Clock Mode	COUNTER_ REALTIME Clock Name	COUNTER_ REALTIME Clock Frequencies	COUNTER_ REALTIME Increment Value	PRCM_MPU Register Programming
System (SYS)	SYS_CLK, MHz	12	64 / 125	PRM_FRAC_INCREMENTER_NUMERATOR [11:0] SYS_MODE_NUMERATOR divided by PRM_FRAC_INCREMENTER_DENUMERATOR_ RELOAD [11:0] DENOMINATOR
		13	768 / 1625	
		19.2	8 / 25	
		26	384 / 1625	
		27	256 / 1125	
		38.4	4 / 25	
ABE Low-Power (ABE_LP)	ABE_LP_CLK, MHz	12.288	1 / 2	PRM_FRAC_INCREMENTER_NUMERATOR [27:16] ABE_LP_MODE_NUMERATOR divided by PRM_FRAC_INCREMENTER_DENUMERATOR_ RELOAD [11:0] DENOMINATOR
Low-Power (LP)	FUNC_32K_CLK, Hz	32 768	375 / 2	PRM_FRAC_INCREMENTER_DENUMERATOR_ RELOAD [16] RELOAD

4.3.5.1 Frequency Change Procedure

The change between the system clock (SYS_CLK) and the ABE low-power clock (ABE_LP_CLK) is performed within global PRCM. A software-controllable bit (CM_CLKSEL_WKUPAON[0] CLKSEL) controls this change. A glitch-free clock multiplexer produces the resulting clock (WKUPAON_ICLK), which is used as the functional clock of the master counter. The CM_CLKSEL_WKUPAON[0] CLKSEL bit is exported from global PRCM to the master counter to control simultaneously the mode (SYS or ABE_LP).

The transition from SYS to ABE_LP mode (DPLL cascading entry) is done under software control as follows:

- DPLL_ABE must be locked before (under software control, global PRCM register CM_CLKMODE_DPLL_ABE[2:0] DPLL_EN = 0x7).
- Software writes 1 in the global PRCM register CM_CLKSEL_WKUPAON[0] CLKSEL bit to choose DPLL_ABE clock.

The transition from ABE_LP to SYS mode (DPLL cascading exit) is done under software control as follows:

- Software writes 0 in the global PRCM register CM_CLKSEL_WKUPAON[0] CLKSEL bit to choose SYS CLK.
- DPLL_ABE may be unlocked after.

Transition from FUNC (ABE_LP or SYS) to LP mode is done by hardware upon MPU subsystem standby entry sequence.

Transition from LP to FUNC (ABE_LP or SYS) mode is done by hardware upon MPU subsystem standby exit sequence.

The frequency change involves some uncertainty on the counter due to a glitch-free clock MUX in global PRCM. In order not to accumulate them, a free-running coarse counter on the FUNC_32K_CLK clock holds the reference count, used for realignment when necessary. To load and reload the reference count value (375/2) from the coarse counter, the user must write 1 in the PRM_FRAC_INCREMENTER_DENUMERATOR_RELOAD[16] RELOAD bit (but it must be 0 before doing that).

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Once configured (at first boot time), the counter is running in all modes without any action required by software.

4.3.6 MPU Watchdog Timer

The MPU watchdog timer (WD_TIMER_MPU) implements two channels, one per MPU core (WD_TIMER_MPU_C0 and WD_TIMER_MPU_C1, respectively; an unified name WD_TIMER_MPU_Cx is used hereafter in the chapter). The WD_TIMER_MPU operates on MPU subsystem clock (MPU_DPLL_CLK).

Each WD_TIMER_MPU_Cx channel implements:

- A 32-bit decrementing counter which has a period set by the value loaded into the counter (via the WDT_LOAD_REGISTER_i[31:0] NEWCOUNT bit field) and the prescaler ratio (set via the WDT_PRESCALER_REGISTER[9:0] PRESCALER bit field). The period is calculated as follows: $T_{WD\_TIMER\_MPU\_Cx}$ = (PRESCALER + 1) x (NEWCOUNT + 1) / f(MPU_DPLL_CLK).
- Two interrupt output signals (WARN, INTR)
- One reset request output (MPUSSRST)

The counter starts decrementing when the WDT_CONTROL_REGISTER_i[0] ENABLE bit is set to 0x1. The current count value can be monitored by reading the WDT_COUNT_REGISTER_i[31:0] CURRENTCOUNT bit field. When the counter reaches zero, a timeout condition occurs. In the timeout condition, the counter stops counting and:

- WD_TIMER_MPU_Cx_IRQ interrupt is generated to the INTC_MPU, if enabled by setting the WDT_CONTROL_REGISTER_i[1] INTREN bit to 0x1.
- Reset request is generated to the global PRCM, if enabled by setting the WDT_CONTROL_REGISTER_i[3] MPUSSRSTEN bit to 0x1.

NOTE: If the MPU core corresponding to the WD_TIMER_MPU_Cx channel is in debug state, the counter does not decrement until the MPU core returns to non-debug state. Debug state is inferred by monitoring the DBGACK signal corresponding to this core.

Additionally, the user can also setup a warning condition which can be used to signal an interrupt that gives software a notice when the WD_TIMER_MPU_Cx is getting close to a timeout. The threshold value is set in the WDT_WARNING_REGISTER_i[31:0] WARNING_WATERMARK bit field. The current count value is then compared to the threshold (warning watermark) level value and when CURRENTCOUNT = WARNING_WATERMARK, a warning interrupt (WD_TIMER_MPU_Cx_IRQ_WARN) is generated to the INTC_MPU (if enabled by setting the WDT_CONTROL_REGISTER_i[1] WARNEN bit to 0x1).

The mapping of the four WD_TIMER_MPU interrupts is as follows:

- WD_TIMER_MPU_C0_IRQ_WARN mapped to MPU_IRQ_4
- WD_TIMER_MPU_C1_IRQ_WARN mapped to MPU_IRQ_5
- WD_TIMER_MPU_C0_IRQ mapped to MPU_IRQ_139
- WD_TIMER_MPU_C1_IRQ mapped to MPU_IRQ_140

The user can also poll the following status bits:

- WDT_RESET_STATUS_REGISTER_i[0] TO, to know when the timeout condition has occured. This bit might also be used to figure out which WD_TIMER_MPU_Cx signalled a reset request.
- WDT_RESET_STATUS_REGISTER_i[1] WARN, to know when the warning condition has occured.

The following programming guidelines should be taken into account:

- The WDT_PRESCALER_REGISTER_i register should be written (if needed) before the WDT_LOAD_REGISTER_i register is written. This is because when the WDT_LOAD_REGISTER_i register is written, the WDT_COUNT_REGISTER_i register is immediately updated with this value and at the same time, the PRESCALER value is sampled to be used by the decrement logic which controls the WDT_COUNT_REGISTER_i register.
- The WDT_WARNING_REGISTER_i and WDT_LOAD_REGISTER_i registers should be written before the WD_TIMER_MPU_Cx is enabled (WDT_CONTROL_REGISTER_i[0] ENABLE = 0x1). Otherwise, interrupts and reset request may be asserted immediately depending on the state of these registers.

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For example, after reset these registers have '0' and if the WDT_CONTROL_REGISTER register is configured to enable the corresponding interrupts and reset request, and then WD_TIMER_MPU_Cx is enabled, interrupts and reset request are immediately asserted.

The suggested programming order is as follows:

1. Set the warning watermark level (WDT_WARNING_REGISTER_i), if needed
2. Set the prescaler ratio (WDT_PRESCALER_REGISTER_i[9:0] PRESCALER)
3. Set the new count value (WDT_LOAD_REGISTER_i)
4. Enable corresponding interrupts and reset request in WDT_CONTROL_REGISTER_i, if needed
5. Enable WD_TIMER_MPU_Cx (WDT_CONTROL_REGISTER_i[0] ENABLE = 0x1)

NOTE: When the MPU cores are going to low power state, the WD_TIMER_MPU may need to be disabled. If it is not disabled, then the WD_TIMER_MPU may timeout (since the MPU core is not refreshing the timeout counters) and will generate MPUSS reset request which will reset the MPU domain, including both MPU cores.

4.3.7 MPU Subsystem Power Management

The MPU subsystem implements a local PRCM (PRCM_MPU) module to handle the local Cortex-A15 CPU power domains, along with the corresponding L1 cache. The PRCM_MPU module includes two power-management control (PSCON) modules to control the power chains for MPU_C0 and MPU_C1. The PRM_PSCON_COUNT register is used for that control purpose.

In addition to the standard power-management technique supported in the device, the MPU subsystem also employs an SR3-APG (automatic power gating) power-management technology to reduce leakage. This technology allows for full logic and memories retention on MPU_C0 and MPU_C1 and is controlled by the PRCM_MPU. The SR3-APG power-management can be enabled by setting the PRM_PSCON_COUNT[24] HG_EN bit. For more information about how to enable SR3-APG fast-wakeup, see Section 4.3.7.6, *SR3-APG Technology Fail-Safe Mode*.

4.3.7.1 Power Domains

The MPU subsystem is divided into six power domains controlled by the local or global PRCM module, as shown in Figure 4-9.

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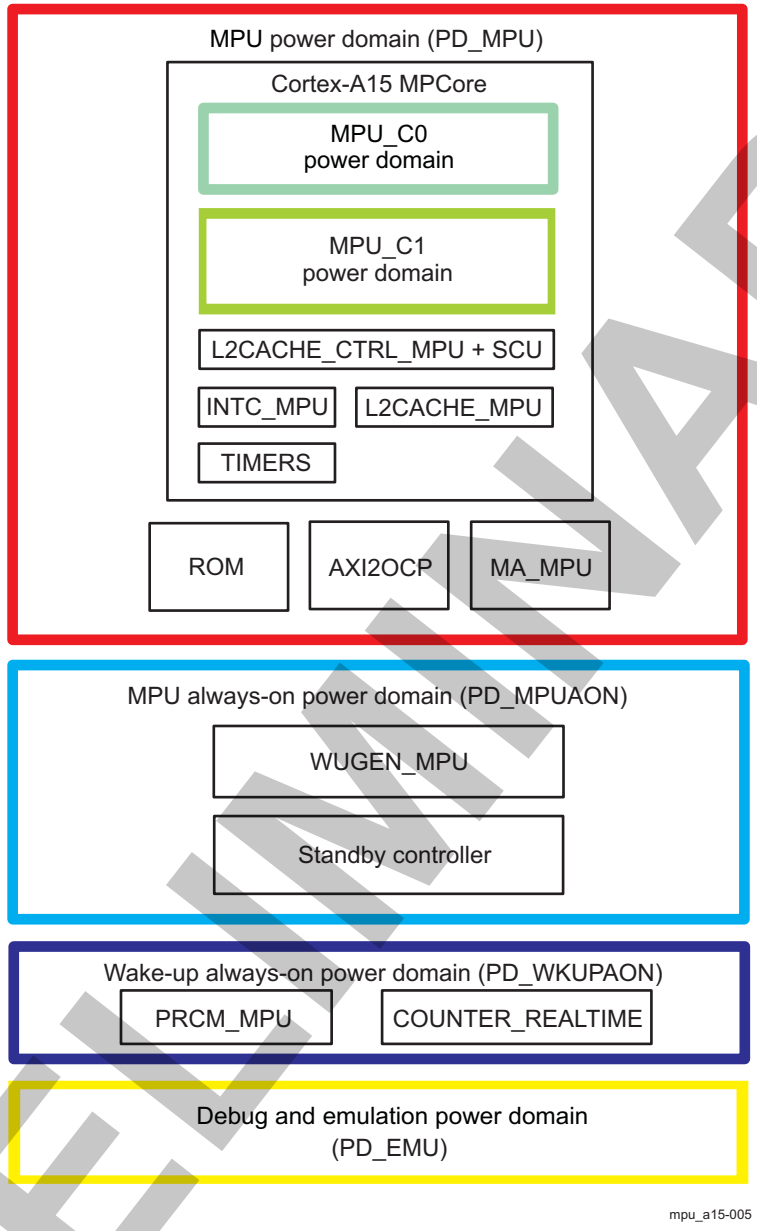
Figure 4-9. MPU Subsystem Power Domains Overview



NOTE: The MPU debug and trace modules are implemented in various power domains. For more information, see Chapter 29, *On-Chip Debug Support*.

The device-level power domains are directly aligned with voltage domains and thus can be represented as a cross-reference to the different voltage domains.

For information about the physical power domains (PD_MPU, PD_MPUAON, PD_WKUPAON, and PD_EMU) and the related voltage domains, see Chapter 3, *Power, Reset, and Clock Management*.

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4.3.7.2 Power States of MPU_Cx

MPU_Cx (where x = 0 or 1) changes power states only when the StandbyWFI signal is asserted. There is no signal coming from the MPU cores, or the MPU cluster to define in which power state MPU_Cx can go. Software must program such information by writing to the PM_CPUx_PWRSTCTRL[1:0] POWERSTATE bit field before executing the WFI instruction. Table 4-7 provides the software requirements before executing the WFI instruction, and the condition to return to run mode.

Table 4-7. MPU_Cx State Transitions

Low-Power State	Software Sequence Before Executing WFI	Wakeup (Transition Back to Run Mode)
WFI/ON Logic ON L1$ ON	Execute a Data Synchronization Barrier (DSB) instruction.	Managed locally to MPU_Cx upon one of the following sources: • An interrupt, masked or unmasked (important: masked does not mean disabled) • An imprecise data abort, regardless of the value of the CPSRA bit • A debug request generated by writing 1 to the HALTING DEBUG MODE bit of the Cortex-A15 DBGSCR register, or the assertion of the Cortex-A15 EDBGRQ pin • Global device cold or warm reset source
WFI/INACT Logic ON L1$ ON	Execute a DSB instruction.	Managed locally by PRCM_MPU upon following source: • An interrupt, enabled at WUGEN_MPU level • A forced wakeup (sw_wkup) • A full debug wake-up request sequence: ForceActive from the DAP_PC, a debug request (as explained previously), assert block reset, wait for processor to halt and clear the block reset • Global device cold or warm reset source
WFI/RETENTION Logic RET L1$ ON L1$ peripheral OFF	1. Set the PM_CPUx_PWRSTCTRL[1:0] POWERSTATE bit field to 0x1 (RETENTION state). 2. Execute a DSB instruction.	Managed locally by PRCM_MPU upon following source: • An interrupt, enabled at WUGEN_MPU level • A forced wakeup (sw_wkup) • A full debug wake-up request sequence: ForceActive from the DAP_PC, a debug request (as explained previously), assert block reset, wait for processor to halt and clear the block reset • Global device cold or warm reset source PRCM_MPU does not need to reset MPU_Cx.

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Table 4-7. MPU_Cx State Transitions (continued)

Low-Power State	Software Sequence Before Executing WFI	Wakeup (Transition Back to Run Mode)
WFI/OFF Logic OFF L1$ OFF	1. Save INTC_MPU configuration for MPU_Cx interrupts. 2. Disable SGI and PPI toward MPU_Cx in INTC_MPU. 3. Save all ARM registers, including CPSR and SPSR. 4. Save all CP15 registers. 5. Save all debug-related states. 6. Set the PM_CPUx_PWRSTCTRL[1:0] POWERSTATE bit field to 0x0 (OFF state). 7. Clear the C-bit in the SCTLR to prevent further data cache allocation. 8. Clean/invalidate L1$ content on an as-needed basis. 9. Execute an Instruction Synchronization Barrier (ISB) instruction to ensure that all of the above CP15 register changes have been committed. 10. Execute a DSB instruction.	Managed locally by PRCM_MPU upon following source: • An interrupt, enabled at WUGEN_MPU level • A forced wakeup (sw_wkup) • A full debug wake-up request sequence (as previously mentioned) • Global device cold or warm reset source PRCM_MPU must reset MPU_Cx to make it reboot and restore its context, including INTC_MPU.
WFI/FORCED_OFF[(1)] Logic OFF L1$ OFF	1. Save INTC_MPU configuration for MPU_C1 interrupts. 2. Disable SGI and PPI toward MPU_C1 in INTC_MPU. 3. Save all ARM registers, including CPSR and SPSR. 4. Save all CP15 registers. 5. Save all debug-related states. 6. Set the PM_CPU1_PWRSTCTRL[1:0] POWERSTATE bit field to 0x0 (OFF state). 7. Set the PM_CPU1_PWRSTCTRL[7] FORCED_OFF bit to 0x1. 8. Clear the C-bit in the SCTLR to prevent further data cache allocation. 9. Clean/invalidate L1$ content on an as-needed basis. 10. Clear SMP bit to take CPU out of coherency. 11. Execute an ISB instruction to ensure that all of the above CP15 register changes have been committed. 12. Execute a DSB instruction.	Managed locally by PRCM_MPU upon following source: • A forced wakeup (sw_wkup) • A full debug wake-up request sequence (as previously mentioned). Block reset is not supported. • Global device cold or warm reset source PRCM_MPU must reset MPU_Cx to make it reboot and restore its context, including INTC_MPU.

(1) Applies to MPU_C1 only.

NOTE: For the description of the Cortex-A15 CPU registers and the DSB/ISB instructions, see the ARM *Cortex-A15 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

The RETENTION low-power state is not natively supported by the MPU cluster. This mode is implemented with SR3-APG power-management technology. The MPU subsystem power-management hardware is designed to ensure that the system does not have an L1 cache coherency problem when putting both MPU cores in retention mode. In this mode, the MPU_Cx logic is in full retention with all memory content preserved by keeping the array of memories fully powered and the logic of the memory peripheries shut down. In slow wake-up mode, memories are put into retention to prevent more leakage.

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In OFF and RETENTION low-power states, the standby controller gates the clock to the MPU cluster by deasserting the CLKEN signal before signaling the PRCM_MPU to perform a power transition. In these low-power states, the MPU core can be wakened only by the PRCM_MPU. A number of important actions must be performed by software before entering such a state.

FORCED_OFF mode applies only to MPU_C1. In this mode, it is critically important for software to clear the SMP bit of the targeted MPU core to take that MPU core out of coherency and to prevent TLB, BTB, or instruction cache maintenance operations from other MPU core in the cluster being issued to this MPU core. The SMP bit is part of the Auxiliary Control Register (ACTLR); there is one ACTLR per MPU core. The ACTLR is a CP15 register. For more information about this register, see the ARM *Cortex-A15 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

A wakeup from OFF low-power state must always happen through a MPU core reset so that the MPU core restores its state to the same level as before the power transition before handling the wake-up event itself (the interrupt). A wakeup from RETENTION low-power state does not need to happen through a MPU core reset because MPU core logics are fully retained.

NOTE: The private peripheral interrupts (PPIs) cannot wake up an MPU core in INACT, RETENTION, or OFF low-power state. Software-generated interrupts (SGI) cannot wake up an MPU core in the same low-power state. However, it is possible to work around the issue by applying the following method:

- When MPU_Cx wants to send an SGI to MPU_Cy (that is, the other MPU core), it must first systematically set the CM_CPUy_CLKSTCTRL[1:0] CLKTRCTRL bit field to 0x2 (software-forced wake-up transition),
- The MPU_Cy corresponding ISR must write back the CM_CPUy_CLKSTCTRL[1:0] CLKTRCTRL bit field to 0x3 (HW_AUTO, automatic transition).

Table 4-8 gives details of the power state of the supported MPU_Cx and the corresponding values of the PRCM_MPU register.

Table 4-8. MPU_Cx Supported Power States

Hardware Conditions		MPU_Cx Programming Model		Resulting MPU_Cx State			
StandbyWFI StandbyWFE	**State of L2/Other MPU core**	**PRCM_MPU Power State PM_CPUx_PWRSTCTRL[1:0] POWERSTATE**	**PRCM_MPU Clock Transition Control CM_CPUx_CLKSTCTRL[1:0] CLKTRCTRL**	**Logic**	**L1 Cache**	**ARM Cortex-A15 Internal Clock Gating**	**Power State at PRCM_MPU**
MPU_Cx running	Any	Any	Any	ON	ON	ON	ON
MPU_Cx in WFE	Any	Any	Any	ON	ON	OFF	ON
MPU_Cx in WFI	Any	Any	NO_SLEEP/SW_WKUP	ON	ON	OFF	ON
MPU_Cx in WFI	Any	ON	HW_AUTO	ON	ON	OFF	ON
MPU_C1 in WFI	Any	FORCED_OFF(1)	HW_AUTO	OFF	OFF	OFF	OFF
MPU_Cx in WFI	!= (IDLE/WFI/WFI)	Any	HW_AUTO	ON	ON	OFF	ON
MPU_Cx in WFI	IDLE/WFI/WFI	INACT	HW_AUTO	ON	ON	OFF	INACT
MPU_Cx in WFI	IDLE/WFI/WFI	RETENTION	HW_AUTO	SR3-APG/ON(2)	ON/RETENTION(3)	OFF	CSWRET

(1) FORCED_OFF mode applies only to MPU_C1. See Table 4-7 for the guidelines about how to enter FORCED_OFF mode.
(2) If PRM_PSCON_COUNT[24] HG_EN = 1, MPU core logic is put in SR3-APG state. If not, MPU core logic is kept ON.
(3) L1$ state depends on the values of the PRM_PSCON_COUNT[25] HG_RAMPUP and PRM_PSCON_COUNT[24] HG_EN bits. When CPU PD is in the CSWRET state, if HG_ENABLE = 0x1 and HG_RAMPUP = 0x1, then L1$ memory is in ON state, else L1$ memory is in the RETENTION state. For more information, see Section 4.3.7.6, *SR3-APG Technology Fail-Safe Mode*.

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Table 4-8. MPU_Cx Supported Power States (continued)

Hardware Conditions		MPU_Cx Programming Model		Resulting MPU_Cx State			
StandbyWFI StandbyWFE	State of L2/Other MPU core	PRCM_MPU Power State PM_CPUx_PWRSTCTRL[1:0] POWERSTATE	PRCM_MPU Clock Transition Control CM_CPUx_CLKSTCTRL[1:0] CLKTRCTRL	Logic	L1 Cache	ARM Cortex-A15 Internal Clock Gating	Power State at PRCM_MPU
MPU_Cx in WFI	IDLE/WFI/ WFI	OFF[4]	HW_AUTO	OFF	OFF	OFF	OFF
MPU_Cx in WFI	Any	OFF[5]	HW_AUTO	OFF	OFF	OFF	OFF

[4] ES1 OFF mode. See the note below for details.
[5] ES2 OFF mode. See the note below for details.

NOTE: The behavior of the OFF mode is different between ES1 and ES2:

- ES1 mode (AMBA_IF_MODE[5] ES2_PM_MODE = 0x0): MPU cores would enter and exit OFF mode together. This is the default mode.
- ES2 mode (AMBA_IF_MODE[5] ES2_PM_MODE = 0x1): MPU cores are allowed to enter/exit OFF mode independently.

The AMBA_IF_MODE[5] ES2_PM_MODE bit is a static bit that should not be changed dynamically.

The ROM code provides specific API for configuring the AMBA_IF_MODE register. For more information, see Section 28.4.3, *Wakeup Generator*, in Chapter 28, *Initialization*.

The PM_CPUx_PWRSTCTRL register is static over any power transition. That is, software programs it before executing the WFI instruction and does not change it until MPU_Cx is again in running mode. In other words, when MPU_Cx reaches a low-power state, it cannot move to another low-power state. It must be woken up to reach another low-power state. To wake up MPU_Cx, the user must:

1. Execute a forced wake-up transition to the MPU_Cx: CM_CPUx_CLKSTCTRL[1:0] CLKTRCTRL = 0x2.
2. The MPU_Cx interrupt handler must write back the automatic hardware transition: CM_CPUx_CLKSTCTRL[1:0] CLKTRCTRL = 0x3.

Table 4-9 shows the available MPU_Cx power states in single and coherency mode. For coherency, software must ensure that both MPU cores are in the same power state.

Table 4-9. Available MPU_Cx Power States in Single and Coherency Mode

MPU_C0 Power State	MPU_C1 Power State	Mode
Running/ON or WFI/ON	Running/ON or WFI/ON	SMP mode (coherent mode)
WFI/INACT	WFI/INACT	
WFI/CSWRET	WFI/CSWRET	
WFI/OFF[1]	WFI/OFF[1]	
WFI/OFF[2]	Any state[2]	
Any state[2]	WFI/OFF[2]	
Running/ON or WFI/ON	OFF (Forced-off)	Single mode (MPU_C1 is out of coherency)
WFI/INACT	OFF (Forced-off)	
WFI/CSWRET	OFF (Forced-off)	
WFI/OFF	OFF (Forced-off)	

[1] Valid for ES1 PM mode (AMBA_IF_MODE[5] ES2_PM_MODE = 0x0).
[2] Valid for ES2 PM mode (AMBA_IF_MODE[5] ES2_PM_MODE = 0x1).

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4.3.7.3 Power States of MPU Subsystem

The MPU subsystem power domain (PD_MPU) must be at a higher or equal power state (a state that consumes more power) than the higher of the two MPU cores. For example, it is illegal for the MPU subsystem power state to be OFF, while the power state of one or both of the MPU cores is RETENTION. Software must ensure that only legal power states are programmed. When an illegal state is entered, the behavior of the hardware is unpredictable.

Table 4-10 lists the MPU subsystem legal power states.

Table 4-10. MPU Subsystem Legal Power States

Hardware Conditions		MPU/System Programming Model				Resulting MPU/System State			
MPU_Cx States	State of L2	PRCM Power State PM_MPU_PWRSTCTRL[1:0] POWERSTATE	PRCM Logic Retention State PM_MPU_PWRSTCTRL[2] LOGICRETSTATE	PRCM L2 Memory Retention State PM_MPU_PWRSTCTRL[9] MPU_L2_RETSTATE	PRCM Clock Transition Control CM_MPU_CLKSTCTRL[1:0] CLKTRCTRL	Logic	L2 Cache	DPLL Clock	Power State (at PRCM)
At least one is ON	Any	Any	Any	Any	Any	ON	ON	ON	ON
Any	!= (IDLE / WFI)	Any	Any	Any	Any	ON	ON	ON	ON
Power state of both MPU cores is less than or equal to INACT	IDLE / WFI	Any	Any	Any	NO_SLEEP/SW_WKUP	ON	ON	ON	ON
	IDLE / WFI	ON	Any	Any	HW_AUTO	ON	ON	ON	ON
	IDLE / WFI	INACT	Any	Any	HW_AUTO	ON	ON	OFF	INACT
Power state of both MPU cores is less than or equal to CSWRET	IDLE / WFI	RETENTION	CSWRET	RETENTION	HW_AUTO	ON	RETENTION	OFF	CSWRET

NOTE: All the transitions presented in Table 4-10, except for the first line, are handled by the PRCM_MPU and the global PRCM.

Once the MPU subsystem reaches a low-power state (INACT, CSWRET, OFF), it cannot move to another low-power state. It must be woken up to reach another low-power state.

4.3.7.4 WUGEN_MPU

The WUGEN_MPU belongs to the MPU always-on power domain (PD_MPUAON) and is responsible for generating wake-up events from the incoming interrupts (external and local to the MPU subsystem) according to the WUGEN_MPU 160-bit enable field (from WKG_ENB_A_x to WKG_ENB_E_x for MPU_Cx, where x = 0 or 1), which defines the interrupt that wakes up the MPU cores. Note that each MPU core cannot be independently wakened by interrupts. Instead, an enabled interrupt wakes up both MPU cores (except if MPU_C1 is in FORCED_OFF state). Therefore, the WUGEN_MPU is designed to handle interrupts for both MPU cores and generates a single wake-up request signal to the standby controller.

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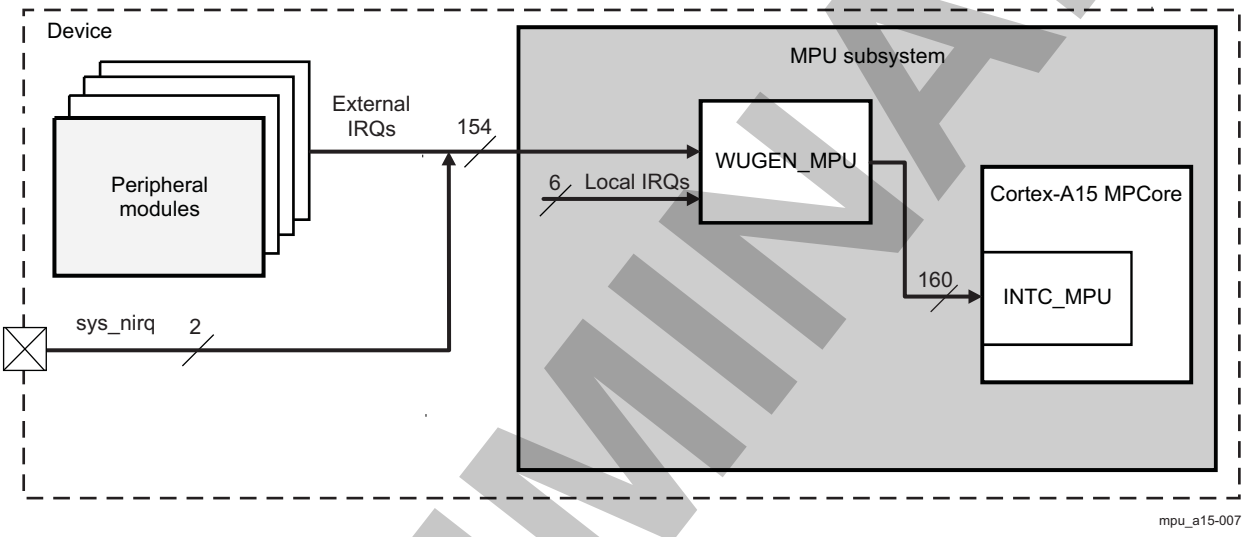
All interrupts are enabled after reset, except MPU_IRQ_8 (which is not supported by the GP device). The Cortex-A15 MPU can access the WUGEN_MPU internal configuration registers through the AXI2OCP.

Software must program interrupt enabling and disabling coherently in the INTC_MPU and in the WUGEN_MPU enable registers. That is, a given interrupt for a given MPU core is either enabled at both INTC_MPU and WUGEN_MPU, or disabled at both; no combination is allowed.

WUGEN_MPU includes two registers (AUX_CORE_BOOT0 and AUX_CORE_BOOT1) which can be used by the ROM code and OS during SMP boot. The AUX_CORE_BOOT0 register is intended to indicate boot status to either cores; the AUX_CORE_BOOT1 register can be used to store execution start address of the second core (also known as aux core). For more information, see Chapter 28, *Initialization*.

Figure 4-10 is a functional overview of the WUGEN_MPU in the MPU subsystem.

Figure 4-10. WUGEN_MPU Overview



4.3.7.5 Power Transition Sequence

At power-on-reset (POR), or global warm reset, both MPU cores are powered on. Software can determine the appropriate power mode for both MPU cores and program the PRCM_MPU accordingly.

There are three types of power transitions:

- Power transitions that do not involve the local or global PRCM module
  - MPU_Cx transition to WFE/ON - corresponds to line 2 of Table 4-8
  - MPU_Cx transition to WFI/ON - corresponds to lines 3, 4, and 6 of Table 4-8
- Power transitions handled by the local PRCM module
  - MPU_C1 transition to WFI/FORCED_OFF - corresponds to line 5 of Table 4-8. Requires software to program PRCM_MPU with FORCED_OFF mode.
  - MPU_Cx transition to WFI/INACT, WFI/RET or WFI/OFF - corresponds to line 7, 8 and 9 of Table 4-8. Requires software to program the PRCM_MPU with INACT/RET/OFF mode.
- Power transitions handled by the local and global PRCM modules

4.3.7.6 SR3-APG Technology Fail-Safe Mode

The SR3-APG power-management technology implements a fast power ramp-up technology. To take advantage of the fast ramp-up feature in SR3-APG, software must first enable it by setting the PRM_PSCON_COUNT[25] HG_RAMPUP bit to 1.

A fail-safe mechanism is put in place to revert back to the standard power ramp-up time by setting the PRM_PSCON_COUNT[25] HG_RAMPUP bit to 0.

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The slow ramp-up time can be set through the PRM_PSCON_COUNT[23:16] HG_PONOUT_2_PGDOODIN_TIME bit field when the HG weak chain is used (in other words, the PRM_PSCON_COUNT[25] HG_RAMPUP bit is set to 0x0).

This applies only when SR3-APG is enabled (PRM_PSCON_COUNT[24] HG_EN = 1).

The L1 cache memory state depends on the values of the PRM_PSCON_COUNT[25] HG_RAMPUP and PRM_PSCON_COUNT[24] HG_EN bits. When CPU PD is in CSWRET state and HG_ENABLE and HG_RAMPUP are set to 0x1, L1 cache is in the ON state.

If SR3-APG is disabled (PRM_PSCON_COUNT[24] HG_EN = 0), the L1 cache array can be put in RETENTION during CSWRET regardless of the PRM_PSCON_COUNT[25] HG_RAMPUP bit.

4.3.8 MPU Subsystem AMBA Interface Configuration

There are some inputs at the MPU core (MPU_Cx) boundary which can be tied off to disable certain kind of transactions appearing on the AMBA4 interface:

- SYSBARDISABLE (SBD): This controls whether:
  - Barriers are handled internal to MPU core (SBD = 1), or
  - Barriers are issued on the AMBA4 interface (SBD = 0).
- BROADCASTINNER (BI), BROADCASTOUTER (BO), BROADDCASTMAINTENANCE (BCM): These control whether external snoops are issued on AMBA4 interface or not:
  - BI=BO=BCM=0: No external snoops issued.
  - BI=BO=BCM=1: External snoops can be issued. Not supported in the device.

For detailed description on these inputs, see the ARM *Cortex-A15 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

To give flexibility and mitigate risk, a programmable register (AMBA_IF_MODE) is added to control the tie-off value of these MPU_Cx inputs.

These are the only legal combinations of [BI, BO, BCM, SBD] allowed:

- BI, BO, BCM, SBD = 0001 – Corresponds to **AXI3** mode. Barriers not issued on AMBA4 interface. External snoops not issued. This is the default mode.
- BI, BO, BCM, SBD = 0000 – Corresponds to **ACE non-coherent, no L3** mode. Barriers issued on AMBA4 interface. External snoops not issued.

The ROM code provides specific API for configuring the AMBA_IF_MODE register. For more information, see Section 28.4.3, *Wakeup Generator*, in Chapter 28, *Initialization*.

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4.4 Dual Cortex-A15 MPU Subsystem Register Manual

4.4.1 Dual Cortex-A15 MPU Subsystem Instance Summary

Table 4-11. Dual Cortex-A15 MPU Subsystem Instance Summary

Module Name	Base Address	Size
CS_STM_MPU	0x4700 0000	16 MiB
INTC_MPU	0x4821 0000	32 KiB
PRCM_MPU_OCP_SOCKET	0x4824 3000	512 bytes
PRCM_MPU_DEVICE	0x4824 3200	512 bytes
PRCM_MPU_PRM_C0	0x4824 3400	512 bytes
PRCM_MPU_CM_C0	0x4824 3600	512 bytes
PRCM_MPU_PRM_C1	0x4824 3800	512 bytes
PRCM_MPU_CM_C1	0x4824 3A00	512 bytes
WUGEN_MPU	0x4828 1000	4 KiB
Reserved	0x4829 0000	12 KiB
WD_TIMER_MPU	0x482A 0000	4 KiB
AXI2OCP_MISC	0x482A 2000	4 KiB
MA_MPU_LSM	0x482A F000	256 bytes
MA_MPU_WP	0x482A F200	256 bytes

4.4.2 CS_STM_MPU Registers

For information about the CS_STM_MPU registers and their description, see the ARM *CoreSight STM Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

4.4.3 INTC_MPU Registers

For information about the INTC_MPU registers and their description, see the ARM *Cortex-A15 MPCore Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

4.4.4 PRCM_MPU_OCP_SOCKET Registers

4.4.4.1 PRCM_MPU_OCP_SOCKET Register Summary

Table 4-12. Local PRCM Revision Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PRCM_MPU_OCP_SOCKET Base Address
REVISION_PRCM_MPU	R	32	0x0	0x4824 3000

4.4.4.2 PRCM_MPU_OCP_SOCKET Register Description

Table 4-13. REVISION_PRCM_MPU

Address Offset	0x0000 0000		
Physical Address	0x4824 3000	**Instance**	PRCM_MPU_OCP_SOCKET
Description	IP Revision register		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 4-14. Register Call Summary for Register REVISION_PRCM_MPU

Dual Cortex-A15 MPU Subsystem Register Manual

- PRCM_MPU_OCP_SOCKET Register Summary: [0]

4.4.5 PRCM_MPU_DEVICE Registers

4.4.5.1 PRCM_MPU_DEVICE Register Summary

Table 4-15. PRCM_MPU_DEVICE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PRCM_MPU_DEVICE Base Address
PRM_RSTST	RW	32	0x0000 0000	0x4824 3200
PRM_PSCON_COUNT	RW	32	0x0000 0004	0x4824 3204
PRM_FRAC_INCREMENTER_NUMERATOR	RW	32	0x0000 0010	0x4824 3210
PRM_FRAC_INCREMENTER_DENUMERATOR_RELOAD	RW	32	0x0000 0014	0x4824 3214

4.4.5.2 PRCM_MPU_DEVICE Register Description

Table 4-16. PRM_RSTST

Address Offset	0x0000 0000		
Physical Address	0x4824 3200	**Instance**	PRCM_MPU_DEVICE
Description	This register logs the global reset sources, thus contains information regarding the cold/warm reset events generated by global PRCM. Each bit is set upon release of the domain reset signal. Must be cleared by software.		
Type	RW (W1toClr - write 0x1 to clear the bit)		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														GLOBAL_WARM_RST	GLOBAL_COLD_RST

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	GLOBAL_WARM_RST	Global warm reset event generated by global PRCM 0x0: No global warm reset. 0x1: Global external warm reset has occurred.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	GLOBAL_COLD_RST	Power-on (cold) reset event generated by global PRCM 0x0: No power-on reset. 0x1: Power-on reset has occurred.	RW W1toClr	1

Table 4-17. Register Call Summary for Register PRM_RSTST

Dual Cortex-A15 MPU Subsystem Integration • Reset Distribution: [0] [1]
Dual Cortex-A15 MPU Subsystem Register Manual • PRCM_MPU_DEVICE Register Summary: [2]

Table 4-18. PRM_PSCON_COUNT

Address Offset	0x0000 0004		
Physical Address	0x4824 3204	**Instance**	PRCM_MPU_DEVICE
Description	Programmable precharge count for L1cache		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						HG_RAMPUP	HG_EN	HG_PONOUT_2_PGDOODIN_TIME								RESERVED								PCHARGE_TIME							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved	R	0x00
25	HG_RAMPUP	Ramp-up mode selection of HG power chain switch 0x0: Slow ramp-up mode – HG weak chain is used. The delay between PONOUTHG and PGOODINHG is defined by the HG_PONOUT_2_PGDOODIN_TIME bit field. 0x1: Fast ramp-up mode – HG weak chain is not used	RW	0
24	HG_EN	HG power chain switch enable 0x0: HG power chain switch is disabled 0x1: HG power chain switch is enabled	RW	0
23:16	HG_PONOUT_2_PGDOODIN_TIME	The value set in this field determines the slow ramp-up time and the duration (number of cycles) of the PONOUTHG to PGOODINHG (transition for power domain without DPS). The duration is computed as 8 x HG_PONOUT_2_PGDOODIN_TIME of system clock cycles. Target is 10us.	RW	0x30
15:8	RESERVED	Reserved	R	0x00
7:0	PCHARGE_TIME	Programmable Precharge count during retention	RW	0x17

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Table 4-19. Register Call Summary for Register PRM_PSCON_COUNT

Dual Cortex-A15 MPU Subsystem Functional Description

- MPU Subsystem Power Management: [0] [1]
- SR3-APG Technology Fail-Safe Mode: [2] [3] [4] [5] [6] [7] [8] [9] [10]

Dual Cortex-A15 MPU Subsystem Register Manual

- PRCM_MPU_DEVICE Register Summary: [11]

Table 4-20. PRM_FRAC_INCREMENTER_NUMERATOR

Address Offset	0x0000 0010		
Physical Address	0x4824 3210	**Instance**	PRCM_MPU_DEVICE
Description	Fractional incrementor		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ABE_LP_MODE_NUMERATOR								RESERVED				SYS_MODE_NUMERATOR											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Resevred	R	0x0
27:16	ABE_LP_MODE_NUMERATOR	Numerator to be used in fractional incrementor when ABE_LP_CLK clock is used as PRCM clock. Reset value corresponds to ABE_LP_CLK clock = 12.288 MHz.	RW	0x659
15:12	RESERVED	Reserved	R	0x0
11:0	SYS_MODE_NUMERATOR	Numerator to be used in fractional incrementor when SYS_CLK is used as PRCM clock. Reset value corresponds to SYS_CLK = 38.4 MHz.	RW	0x208

Table 4-21. Register Call Summary for Register PRM_FRAC_INCREMENTER_NUMERATOR

Dual Cortex-A15 MPU Subsystem Functional Description

- Realtime Counter (Master Counter): [0] [1]

Dual Cortex-A15 MPU Subsystem Register Manual

- PRCM_MPU_DEVICE Register Summary: [2]

Table 4-22. PRM_FRAC_INCREMENTER_DENUMERATOR_RELOAD

Address Offset	0x0000 0014		
Physical Address	0x4824 3214	**Instance**	PRCM_MPU_DEVICE
Description	Reload command and denominator to be used in fractional incrementor		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															RELOAD	RESERVED				DENOMINATOR											

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	RELOAD	Reload counter value from coarse counter. 0->1 transition in this field is used to load the coarse counter into counter.	RW	0
15:12	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
11:0	DENOMINATOR	Denominator to be used in fractional incrementor when when SYS_CLK is used as PRCM clock. Reset value corresponds to SYS_CLK = 38.4 MHz.	RW	0xCB2

Table 4-23. Register Call Summary for Register PRM_FRAC_INCREMENTER_DENUMERATOR_RELOAD

Dual Cortex-A15 MPU Subsystem Functional Description • Realtime Counter (Master Counter): [0] [1] [2] • Frequency Change Procedure: [3]
Dual Cortex-A15 MPU Subsystem Register Manual • PRCM_MPU_DEVICE Register Summary: [4]

4.4.6 PRCM_MPU_PRM_C0 Registers

4.4.6.1 PRCM_MPU_PRM_C0 Register Summary

Table 4-24. PRCM_MPU_PRM_C0 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PRCM_MPU_PRM_C0 Base Address
PM_CPU0_PWRSTCTRL	RW	32	0x0000 0000	0x4824 3400
PM_CPU0_PWRSTST	RW	32	0x0000 0004	0x4824 3404
RM_CPU0_CPU0_RSTCTRL	RW	32	0x0000 0010	0x4824 3410
RM_CPU0_CPU0_RSTST	RW	32	0x0000 0014	0x4824 3414
RM_CPU0_CPU0_CONTEXT	RW	32	0x0000 0024	0x4824 3424

4.4.6.2 PRCM_MPU_PRM_C0 Register Description

Table 4-25. PM_CPU0_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4824 3400	**Instance**	PRCM_MPU_PRM_C0
Description	This register controls the CPU domain power state to reach upon a domain sleep transition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														L1_BANK_ONSTATE		RESERVED							L1_BANK_RETSTATE	RESERVED					LOGICRETSTATE	POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:16	L1_BANK_ONSTATE	CPU_L1 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3

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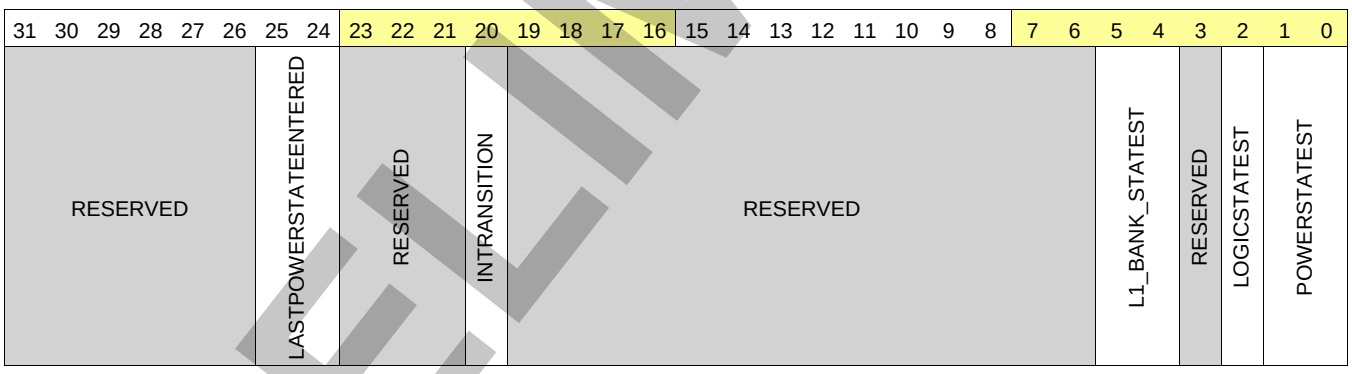
Bits	Field Name	Description	Type	Reset
15:9	RESERVED	Reserved	R	0x00
8	L1_BANK_RETSTATE	CPU_L1 memory state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R Rreturns 1s	1
7:3	RESERVED	Reserved	R	0x00
2	LOGICRETSTATE	Logic state when power domain is RETENTION Read 0x1: Whole logic is retained when domain is in RETENTION state.	R Rreturns 1s	1
1:0	POWERSTATE	Power state control 0x0: OFF state 0x1: RETENTION state 0x3: ON state 0x2: INACTIVE state	RW	0x3

Table 4-26. Register Call Summary for Register PM_CPU0_PWRSTCTRL

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_PRM_C0 Register Summary: [0]

Table 4-27. PM_CPU0_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4824 3404	**Instance**	PRCM_MPU_PRM_C0
Description	This register provides a status on the CPU domain current power state. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved	R	0x00
25:24	LASTPOWERSTATEENTERED	Last low power state entered 0x0: Power domain was previously in OFF 0x1: Power domain was previously RETENTION 0x3: Power domain was previously ON 0x2: Power domain was previously INACTIVE	RW W1toSet	0x0
23:21	RESERVED	Reserved	R	0x0
20	INTRANSITION	Domain transition status Read 0x1: Power domain transition is in progress. Read 0x0: No ongoing transition on power domain	R	0
19:6	RESERVED	Reserved	R	0x0000

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Bits	Field Name	Description	Type	Reset
5:4	L1_BANK_STATEST	CPU_L1 memory state status Read 0x3: Memory is ON Read 0x2: Reserved Read 0x1: Memory is RET Read 0x0: Memory is OFF	R	0x3
3	RESERVED	Reserved	R	0
2	LOGICSTATEST	Logic state status Read 0x1: Logic in domain is ON Read 0x0: Logic in domain is OFF	R	1
1:0	POWERSTATEST	Current power state status Read 0x3: Power domain is ON-ACTIVE Read 0x2: Power domain is ON-INACTIVE Read 0x1: Power domain is in RETENTION Read 0x0: Power domain is OFF	R	0x3

Table 4-28. Register Call Summary for Register PM_CPU0_PWRSTST

Dual Cortex-A15 MPU Subsystem Register Manual • PRCM_MPU_PRM_C0 Register Summary: [0]

Table 4-29. RM_CPU0_CPU0_RSTCTRL

Address Offset	0x0000 0010		
Physical Address	0x4824 3410	**Instance**	PRCM_MPU_PRM_C0
Description	This register controls the assertion/release of the CPU CORE reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RST	CPU warm local reset control 0x0: Reset is cleared 0x1: Reset is asserted	RW	0

Table 4-30. Register Call Summary for Register RM_CPU0_CPU0_RSTCTRL

Dual Cortex-A15 MPU Subsystem Register Manual • PRCM_MPU_PRM_C0 Register Summary: [0]

Table 4-31. RM_CPU0_CPU0_RSTST

Address Offset	0x0000 0014		
Physical Address	0x4824 3414	**Instance**	PRCM_MPU_PRM_C0
Description	This register logs the different reset sources of the MPU domain. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DBGRST_REQ_RSTST	RSTST

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	DBGRST_REQ_RSTST	MPU_C0 processor has been reset due to MPU_C0 emulation reset request driven from MPUSS. Read 0x1: MPU_C0 has been reset upon emulation request. Read 0x0: No emulation reset	RW W1toClr	0
0	RSTST	MPU_C0 software reset Read 0x1: MPU_C0 has been reset upon software reset. Read 0x0: No software reset occurred.	RW W1toClr	0

Table 4-32. Register Call Summary for Register RM_CPU0_CPU0_RSTST

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_PRM_C0 Register Summary: [0]

Table 4-33. RM_CPU0_CPU0_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4824 3424	**Instance**	PRCM_MPU_PRM_C0
Description	This register contains dedicated CPU context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LOSTMEM_CPU_L1	RESERVED						LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_CPU_L1	Specify if memory-based context in CPU_L1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1
7:1	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W1toClr	1

Table 4-34. Register Call Summary for Register RM_CPU0_CPU0_CONTEXT

Dual Cortex-A15 MPU Subsystem Register Manual
• PRCM_MPU_PRM_C0 Register Summary: [0]

4.4.7 PRCM_MPU_CM_C0 Registers

4.4.7.1 PRCM_MPU_CM_C0 Register Summary

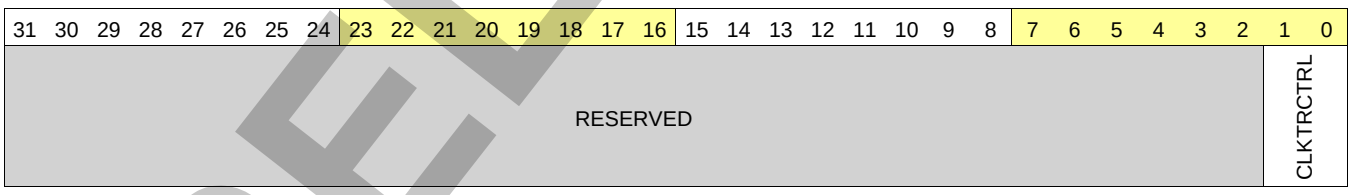
Table 4-35. PRCM_MPU_CM_C0 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PRCM_MPU_CM_C0 Base Address
CM_CPU0_CLKSTCTRL	RW	32	0x0000 0000	0x4824 3600
CM_CPU0_CPU0_CLKCTRL	R	32	0x0000 0020	0x4824 3620

4.4.7.2 PRCM_MPU_CM_C0 Register Description

Table 4-36. CM_CPU0_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4824 3600	**Instance**	PRCM_MPU_CM_C0
Description	This register enables the CPU domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	CLKTRCTRL	Controls the full domain transition of the CPU domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may, however, occur. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions. Read 0x1: Reserved 0x2: Start a software forced wakeup transition on the domain.	RW	0x0

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Table 4-37. Register Call Summary for Register CM_CPU0_CLKSTCTRL

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_CM_C0 Register Summary: [0]

Table 4-38. CM_CPU0_CPU0_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4824 3620	**Instance**	PRCM_MPU_CM_C0
Description	This register manages the CPU clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STBYST
R-0																															R-1

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STBYST	Module standby status. [warm reset insensitive] Read 0x1: Module is in standby. Read 0x0: Module is functional (not in standby).	R	1

Table 4-39. Register Call Summary for Register CM_CPU0_CPU0_CLKCTRL

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_CM_C0 Register Summary: [0]

4.4.8 PRCM_MPU_PRM_C1 Registers

4.4.8.1 PRCM_MPU_PRM_C1 Register Summary

Table 4-40. PRCM_MPU_PRM_C1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PRCM_MPU_PRM_C1 Base Address
PM_CPU1_PWRSTCTRL	RW	32	0x0000 0000	0x4824 3800
PM_CPU1_PWRSTST	RW	32	0x0000 0004	0x4824 3804
RM_CPU1_CPU1_RSTCTRL	RW	32	0x0000 0010	0x4824 3810
RM_CPU1_CPU1_RSTST	RW	32	0x0000 0014	0x4824 3814
RM_CPU1_CPU1_CONTEXT	RW	32	0x0000 0024	0x4824 3824

4.4.8.2 PRCM_MPU_PRM_C1 Register Description

Table 4-41. PM_CPU1_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4824 3800	**Instance**	PRCM_MPU_PRM_C1
Description	This register controls the CPU domain power state to reach upon a domain sleep transition		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														L1_BANK_ONSTATE		RESERVED							L1_BANK_RETSTATE	FORCED_OFF	RESERVED				LOGICRETSTATE	POWERSTATE	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:16	L1_BANK_ONSTATE	CPU_L1 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Rreturns 1s	0x3
15:9	RESERVED		R	0x00
8	L1_BANK_RETSTATE	CPU L1 memory state when domain is RETENTION. Read 0x1: Memory bank is retained when domain is in RETENTION state.	R Rreturns 1s	1
7	FORCED_OFF	Selects if logic must be forced in OFF state. 0x0: Whole logic is not forced in OFF state. 0x1: Whole logic is forced in OFF state.	RW	0
6:3	RESERVED		R	0x0
2	LOGICRETSTATE	Logic state when power domain is RETENTION Read 0x1: Whole logic is retained when domain is in RETENTION state.	R Rreturns 1s	1
1:0	POWERSTATE	Power state control 0x0: OFF state 0x1: RETENTION state 0x3: ON state 0x2: INACTIVE state	RW	0x3

Table 4-42. Register Call Summary for Register PM_CPU1_PWRSTCTRL

Dual Cortex-A15 MPU Subsystem Functional Description • Power States of MPU_Cx: [0] [1]
Dual Cortex-A15 MPU Subsystem Register Manual • PRCM_MPU_PRM_C1 Register Summary: [2]

Table 4-43. PM_CPU1_PWRSTST

Address Offset	0x0000 0004		
Physical Address	0x4824 3804	**Instance**	PRCM_MPU_PRM_C1
Description	This register provides a status on the CPU domain current power state. [warm reset insensitive]		
Type	RW		

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	LASTPOWERSTATEENTERED	RESERVED	INTRANSITION	RESERVED	L1_BANK_STATEST	RESERVED	LOGICSTATEST	POWERSTATEST

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERSTATEENTERED	Last low-power state entered 0x0: Power domain was previously OFF. 0x1: Power domain was previously in RETENTION. 0x3: Power domain was previously ON. 0x2: Power domain previously was INACTIVE.	RW W1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x1: Power domain transition is in progress. Read 0x0: No ongoing transition on power domain	R	0
19:6	RESERVED		R	0x0000
5:4	L1_BANK_STATEST	CPU_L1 memory state status Read 0x3: Memory is ON. Read 0x2: Reserved Read 0x1: Memory is RET. Read 0x0: Memory is OFF.	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x1: Logic in domain is ON. Read 0x0: Logic in domain is OFF.	R	1
1:0	POWERSTATEST	Current power state status Read 0x3: Power domain is ON-ACTIVE. Read 0x2: Power domain is ON-INACTIVE. Read 0x1: Power domain is in RETENTION. Read 0x0: Power domain is OFF.	R	0x3

Table 4-44. Register Call Summary for Register PM_CPU1_PWRSTST

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_PRM_C1 Register Summary: [0]

Table 4-45. RM_CPU1_CPU1_RSTCTRL

Address Offset	0x0000 0010		
Physical Address	0x4824 3810	**Instance**	PRCM_MPU_PRM_C1
Description	This register controls the assertion/release of the CPU CORE reset.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RST	CPU warm local reset control 0x0: Reset is cleared. 0x1: Reset is asserted.	RW	0

Table 4-46. Register Call Summary for Register RM_CPU1_CPU1_RSTCTRL

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_PRM_C1 Register Summary: [0]

Table 4-47. RM_CPU1_CPU1_RSTST

Address Offset	0x0000 0014		
Physical Address	0x4824 3814	**Instance**	PRCM_MPU_PRM_C1
Description	This register logs the different reset sources of the MPU domain. Each bit is set upon release of the domain reset signal. Must be cleared by software. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DBGRST_REQ_RSTST	RSTST

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	DBGRST_REQ_RSTST	MPU_C1 processor has been reset due to MPU_C0 emulation reset request driven from MPUSS Read 0x1: MPU_C1 has been reset upon emulation request. Read 0x0: No emulation reset	RW W1toClr	0
0	RSTST	MPU_C1 software reset Read 0x1: MPU_C1 has been reset upon software reset. Read 0x0: No software reset occurred.	RW W1toClr	0

Table 4-48. Register Call Summary for Register RM_CPU1_CPU1_RSTST

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_PRM_C1 Register Summary: [0]

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Table 4-49. RM_CPU1_CPU1_CONTEXT

Address Offset	0x0000 0024		
Physical Address	0x4824 3824	**Instance**	PRCM_MPU_PRM_C1
Description	This register contains dedicated CPU context statuses. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							LOSTMEM_CPU_L1	RESERVED							LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	LOSTMEM_CPU_L1	Specify if memory-based context in CPU_L1 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained. 0x1: Context has been lost.	RW W1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained. 0x1: Context has been lost.	RW W1toClr	1

Table 4-50. Register Call Summary for Register RM_CPU1_CPU1_CONTEXT

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_PRM_C1 Register Summary: [0]

4.4.9 PRCM_MPU_CM_C1 Registers

4.4.9.1 PRCM_MPU_CM_C1 Register Summary

Table 4-51. PRCM_MPU_CM_C1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PRCM_MPU_CM_C1 Base Address
CM_CPU1_CLKSTCTRL	RW	32	0x0000 0000	0x4824 3A00
CM_CPU1_CPU1_CLKCTRL	R	32	0x0000 0020	0x4824 3A20

4.4.9.2 PRCM_MPU_CM_C1 Register Description

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Table 4-52. CM_CPU1_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4824 3A00	**Instance**	PRCM_MPU_CM_C1
Description	This register enables the MPU domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CLKTRCTRL	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	CLKTRCTRL	Controls the full domain transition of the CPU domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may, however, occur. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wake-up transition are based upon hardware conditions. Read 0x1: Reserved 0x2: Start a software forced wake-up transition on the domain.	RW	0x0

Table 4-53. Register Call Summary for Register CM_CPU1_CLKSTCTRL

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_CM_C1 Register Summary: [0]

Table 4-54. CM_CPU1_CPU1_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4824 3A20	**Instance**	PRCM_MPU_CM_C1
Description	This register manages the MPU clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STBYST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STBYST	Module standby status. [warm reset insensitive] Read 0x1: Module is in standby. Read 0x0: Module is functional (not in standby).	R	1

Table 4-55. Register Call Summary for Register CM_CPU1_CPU1_CLKCTRL

Dual Cortex-A15 MPU Subsystem Register Manual
- PRCM_MPU_CM_C1 Register Summary: [0]

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4.4.10 WUGEN_MPU Registers

4.4.10.1 WUGEN_MPU Register Summary

Table 4-56. WUGEN_MPU Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	WUGEN_MPU Base Address
WKG_CONTROL_0	RW	32	0x0000 0000	0x4828 1000
WKG_ENB_A_0	RW	32	0x0000 0010	0x4828 1010
WKG_ENB_B_0	RW	32	0x0000 0014	0x4828 1014
WKG_ENB_C_0	RW	32	0x0000 0018	0x4828 1018
WKG_ENB_D_0	RW	32	0x0000 001C	0x4828 101C
WKG_ENB_E_0	RW	32	0x0000 0020	0x4828 1020
RESERVED	R	32	0x0000 0024	0x4828 1024
RESERVED	R	32	0x0000 0028	0x4828 1028
RESERVED	R	32	0x0000 002C	0x4828 102C
RESERVED	R	32	0x0000 0030	0x4828 1030
RESERVED	R	32	0x0000 0034	0x4828 1034
WKG_CONTROL_1	RW	32	0x0000 0400	0x4828 1400
WKG_ENB_A_1	RW	32	0x0000 0410	0x4828 1410
WKG_ENB_B_1	RW	32	0x0000 0414	0x4828 1414
WKG_ENB_C_1	RW	32	0x0000 0418	0x4828 1418
WKG_ENB_D_1	RW	32	0x0000 041C	0x4828 141C
WKG_ENB_E_1	RW	32	0x0000 0420	0x4828 1420
RESERVED	R	32	0x0000 0424	0x4828 1424
RESERVED	R	32	0x0000 0428	0x4828 1428
RESERVED	R	32	0x0000 042C	0x4828 142C
RESERVED	R	32	0x0000 0430	0x4828 1430
RESERVED	R	32	0x0000 0434	0x4828 1434
AUX_CORE_BOOT_0	RW	32	0x0000 0800	0x4828 1800
AUX_CORE_BOOT_1	RW	32	0x0000 0804	0x4828 1804
STM_HWEVENTS_INV	RW	32	0x0000 0808	0x4828 1808
AMBA_IF_MODE	RW	32	0x0000 080C	0x4828 180C
RESERVED	R	32	0x0000 0C00	0x4828 1C00
RESERVED	R	32	0x0000 0C04	0x4828 1C04
TIMESTAMPCYCLELO	R	32	0x0000 0C08	0x4828 1C08
TIMESTAMPCYCLEHI	R	32	0x0000 0C0C	0x4828 1C0C

4.4.10.2 WUGEN_MPU Register Description

Table 4-57. WKG_CONTROL_0

Address Offset	0x0000 0000		
Physical Address	0x4828 1000	**Instance**	WUGEN_MPU
Description	Wake-up generator status register for MPU_C0		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DOMAINRESET	MPU_WARM_RESET	MPU_COLD_RESET	RESERVED		EVENTO	STANDBYWFE	STANDBYWFI	RESERVED								

Bits	Field Name	Description	Type[1]	Reset
31:16	RESERVED	Reserved	R	0x0000
15	DOMAINRESET	MPU always-on power domain (PD_MPUAON) reset status bit. It shows if the reset occurred previously. 0x0: no reset occur 0x1: reset occur	R	0
14	MPU_WARM_RESET	This bit is set when the MPU_WARM_RESET signal is asserted. 0x0: MPU_WARM_RESET reset signal has not been asserted 0x1: MPU_WARM_RESET reset request has been asserted	RW (WCtoClr)	0
13	MPU_COLD_RESET	This bit is set when the MPU_COLD_RESET signal is asserted. 0x0: MPU_COLD_RESET reset signal has not been asserted 0x1: MPU_COLD_RESET reset request has been asserted	RW (WCtoClr)	0
12:11	RESERVED	Reserved	R	0x0
10	EVENTO	EVENTO status bit. The event output signal is active, when one SEV instruction is executed. This bit is set when a rising edge of EVENTO from CPU is detected. 0x0: Rising edge of EVENTO is not detected 0x1: Rising edge of EVENTO is detected	RW (WCtoClr)	0
9	STANDBYWFE	This bit gives software the visibility to track whether WFE mode have been entered. 0x0: WFE mode has not been entered 0x1: WFE mode has been entered	RW (WCtoClr)	0
8	STANDBYWFI	This bit gives software the visibility to track whether WFI mode have been entered. 0x0: WFI mode has not been entered 0x1: WFI mode has been entered	RW (WCtoClr)	0
7:0	RESERVED	Reserved	R	0x00

(1) RW (WCtoClr) means that a register bit can be read and is cleared by a write of any value.

Table 4-58. Register Call Summary for Register WKG_CONTROL_0

Dual Cortex-A15 MPU Subsystem Integration • Reset Distribution: [0]
Dual Cortex-A15 MPU Subsystem Register Manual • WUGEN_MPU Register Summary: [1]

Table 4-59. WKG_ENB_A_0

Address Offset	0x0000 0010		
Physical Address	0x4828 1010	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C0) from MPU_IRQ_0 to MPU_IRQ_31. Write 0x0:Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKG_ENB_FOR_INTR31	WKG_ENB_FOR_INTR30	WKG_ENB_FOR_INTR29	WKG_ENB_FOR_INTR28	WKG_ENB_FOR_INTR27	WKG_ENB_FOR_INTR26	WKG_ENB_FOR_INTR25	WKG_ENB_FOR_INTR24	WKG_ENB_FOR_INTR23	WKG_ENB_FOR_INTR22	WKG_ENB_FOR_INTR21	WKG_ENB_FOR_INTR20	WKG_ENB_FOR_INTR19	WKG_ENB_FOR_INTR18	WKG_ENB_FOR_INTR17	WKG_ENB_FOR_INTR16	WKG_ENB_FOR_INTR15	WKG_ENB_FOR_INTR14	WKG_ENB_FOR_INTR13	WKG_ENB_FOR_INTR12	WKG_ENB_FOR_INTR11	WKG_ENB_FOR_INTR10	WKG_ENB_FOR_INTR9	RESERVED	WKG_ENB_FOR_INTR7	WKG_ENB_FOR_INTR6	RESERVED	WKG_ENB_FOR_INTR4	RESERVED	WKG_ENB_FOR_INTR2	WKG_ENB_FOR_INTR1	WKG_ENB_FOR_INTR0

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR31		RW	1
30	WKG_ENB_FOR_INTR30		RW	1
29	WKG_ENB_FOR_INTR29		RW	1
28	WKG_ENB_FOR_INTR28		RW	1
27	WKG_ENB_FOR_INTR27		RW	1
26	WKG_ENB_FOR_INTR26		RW	1
25	WKG_ENB_FOR_INTR25		RW	1
24	WKG_ENB_FOR_INTR24		RW	1
23	WKG_ENB_FOR_INTR23		RW	1
22	WKG_ENB_FOR_INTR22		RW	1
21	WKG_ENB_FOR_INTR21		RW	1
20	WKG_ENB_FOR_INTR20		RW	1
19	WKG_ENB_FOR_INTR19		RW	1
18	WKG_ENB_FOR_INTR18		RW	1
17	WKG_ENB_FOR_INTR17		RW	1
16	WKG_ENB_FOR_INTR16		RW	1
15	WKG_ENB_FOR_INTR15		RW	1
14	WKG_ENB_FOR_INTR14		RW	1
13	WKG_ENB_FOR_INTR13		RW	1
12	WKG_ENB_FOR_INTR12		RW	1
11	WKG_ENB_FOR_INTR11		RW	1
10	WKG_ENB_FOR_INTR10		RW	1
9	WKG_ENB_FOR_INTR9		RW	1
8	WKG_ENB_FOR_INTR8[1]		RW	0
7	WKG_ENB_FOR_INTR7		RW	1
6	WKG_ENB_FOR_INTR6		RW	1
5	WKG_ENB_FOR_INTR5		RW	1
4	WKG_ENB_FOR_INTR4		RW	1
3	WKG_ENB_FOR_INTR3		RW	1
2	WKG_ENB_FOR_INTR2		RW	1
1	WKG_ENB_FOR_INTR1		RW	1
0	WKG_ENB_FOR_INTR0		RW	1

(1) The reset value is 0x0 by safety reasons.

Table 4-60. Register Call Summary for Register WKG_ENB_A_0

Dual Cortex-A15 MPU Subsystem Register Manual
- WUGEN_MPU Register Summary: [0]

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Table 4-61. WKG_ENB_B_0

Address Offset	0x0000 0014		
Physical Address	0x4828 1014	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C0) from MPU_IRQ_32 to MPU_IRQ_63. Write 0x0: Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	WKG_ENB_FOR_INTR62	WKG_ENB_FOR_INTR61	RESERVED	WKG_ENB_FOR_INTR59	WKG_ENB_FOR_INTR58	WKG_ENB_FOR_INTR57	WKG_ENB_FOR_INTR56	RESERVED	RESERVED	WKG_ENB_FOR_INTR53	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR48	WKG_ENB_FOR_INTR47	WKG_ENB_FOR_INTR46	WKG_ENB_FOR_INTR45	WKG_ENB_FOR_INTR44	WKG_ENB_FOR_INTR43	WKG_ENB_FOR_INTR42	WKG_ENB_FOR_INTR41	WKG_ENB_FOR_INTR40	WKG_ENB_FOR_INTR39	WKG_ENB_FOR_INTR38	WKG_ENB_FOR_INTR37	WKG_ENB_FOR_INTR36	RESERVED	WKG_ENB_FOR_INTR34	WKG_ENB_FOR_INTR33	WKG_ENB_FOR_INTR32

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR63		RW	1
30	WKG_ENB_FOR_INTR62		RW	1
29	WKG_ENB_FOR_INTR61		RW	1
28	WKG_ENB_FOR_INTR60		RW	1
27	WKG_ENB_FOR_INTR59		RW	1
26	WKG_ENB_FOR_INTR58		RW	1
25	WKG_ENB_FOR_INTR57		RW	1
24	WKG_ENB_FOR_INTR56		RW	1
23	WKG_ENB_FOR_INTR55		RW	1
22	WKG_ENB_FOR_INTR54		RW	1
21	WKG_ENB_FOR_INTR53		RW	1
20	WKG_ENB_FOR_INTR52		RW	1
19	WKG_ENB_FOR_INTR51		RW	1
18	WKG_ENB_FOR_INTR50		RW	1
17	WKG_ENB_FOR_INTR49		RW	1
16	WKG_ENB_FOR_INTR48		RW	1
15	WKG_ENB_FOR_INTR47		RW	1
14	WKG_ENB_FOR_INTR46		RW	1
13	WKG_ENB_FOR_INTR45		RW	1
12	WKG_ENB_FOR_INTR44		RW	1
11	WKG_ENB_FOR_INTR43		RW	1
10	WKG_ENB_FOR_INTR42		RW	1
9	WKG_ENB_FOR_INTR41		RW	1
8	WKG_ENB_FOR_INTR40		RW	1
7	WKG_ENB_FOR_INTR39		RW	1
6	WKG_ENB_FOR_INTR38		RW	1
5	WKG_ENB_FOR_INTR37		RW	1
4	WKG_ENB_FOR_INTR36		RW	1
3	WKG_ENB_FOR_INTR35		RW	1
2	WKG_ENB_FOR_INTR34		RW	1
1	WKG_ENB_FOR_INTR33		RW	1
0	WKG_ENB_FOR_INTR32		RW	1

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Table 4-62. Register Call Summary for Register WKG_ENB_B_0

Dual Cortex-A15 MPU Subsystem Register Manual

- WUGEN_MPU Register Summary: [0]

Table 4-63. WKG_ENB_C_0

Address Offset	0x0000 0018		
Physical Address	0x4828 1018	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C0) from MPU_IRQ_64 to MPU_IRQ_95. Write 0x0: Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	WKG_ENB_FOR_INTR94	WKG_ENB_FOR_INTR93	WKG_ENB_FOR_INTR92	WKG_ENB_FOR_INTR91	WKG_ENB_FOR_INTR90	WKG_ENB_FOR_INTR89	WKG_ENB_FOR_INTR88	WKG_ENB_FOR_INTR87	WKG_ENB_FOR_INTR86	RESERVED	WKG_ENB_FOR_INTR84	WKG_ENB_FOR_INTR83	RESERVED	RESERVED	WKG_ENB_FOR_INTR80	RESERVED	WKG_ENB_FOR_INTR78	WKG_ENB_FOR_INTR77	WKG_ENB_FOR_INTR76	WKG_ENB_FOR_INTR75	WKG_ENB_FOR_INTR74	WKG_ENB_FOR_INTR73	WKG_ENB_FOR_INTR72	WKG_ENB_FOR_INTR71	WKG_ENB_FOR_INTR70	WKG_ENB_FOR_INTR69	WKG_ENB_FOR_INTR68	WKG_ENB_FOR_INTR67	WKG_ENB_FOR_INTR66	WKG_ENB_FOR_INTR65	RESERVED

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR95		RW	1
30	WKG_ENB_FOR_INTR94		RW	1
29	WKG_ENB_FOR_INTR93		RW	1
28	WKG_ENB_FOR_INTR92		RW	1
27	WKG_ENB_FOR_INTR91		RW	1
26	WKG_ENB_FOR_INTR90		RW	1
25	WKG_ENB_FOR_INTR89		RW	1
24	WKG_ENB_FOR_INTR88		RW	1
23	WKG_ENB_FOR_INTR87		RW	1
22	WKG_ENB_FOR_INTR86		RW	1
21	WKG_ENB_FOR_INTR85		RW	1
20	WKG_ENB_FOR_INTR84		RW	1
19	WKG_ENB_FOR_INTR83		RW	1
18	WKG_ENB_FOR_INTR82		RW	1
17	WKG_ENB_FOR_INTR81		RW	1
16	WKG_ENB_FOR_INTR80		RW	1
15	WKG_ENB_FOR_INTR79		RW	1
14	WKG_ENB_FOR_INTR78		RW	1
13	WKG_ENB_FOR_INTR77		RW	1
12	WKG_ENB_FOR_INTR76		RW	1
11	WKG_ENB_FOR_INTR75		RW	1
10	WKG_ENB_FOR_INTR74		RW	1
9	WKG_ENB_FOR_INTR73		RW	1
8	WKG_ENB_FOR_INTR72		RW	1
7	WKG_ENB_FOR_INTR71		RW	1
6	WKG_ENB_FOR_INTR70		RW	1
5	WKG_ENB_FOR_INTR69		RW	1

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Bits	Field Name	Description	Type	Reset
4	WKG_ENB_FOR_INTR68		RW	1
3	WKG_ENB_FOR_INTR67		RW	1
2	WKG_ENB_FOR_INTR66		RW	1
1	WKG_ENB_FOR_INTR65		RW	1
0	WKG_ENB_FOR_INTR64		RW	1

Table 4-64. Register Call Summary for Register WKG_ENB_C_0

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- WUGEN_MPU Register Summary: [0]

Table 4-65. WKG_ENB_D_0

Address Offset	0x0000 001C		
Physical Address	0x4828 101C	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C0) from MPU_IRQ_96 to MPU_IRQ_127. Write 0x0: Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR120	WKG_ENB_FOR_INTR119	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR114	WKG_ENB_FOR_INTR113	WKG_ENB_FOR_INTR112	WKG_ENB_FOR_INTR111	WKG_ENB_FOR_INTR110	WKG_ENB_FOR_INTR109	RESERVED	WKG_ENB_FOR_INTR107	RESERVED	RESERVED	WKG_ENB_FOR_INTR104	WKG_ENB_FOR_INTR103	WKG_ENB_FOR_INTR102	WKG_ENB_FOR_INTR101	WKG_ENB_FOR_INTR100	WKG_ENB_FOR_INTR99	WKG_ENB_FOR_INTR98	WKG_ENB_FOR_INTR97	WKG_ENB_FOR_INTR96

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR127		RW	1
30	WKG_ENB_FOR_INTR126		RW	1
29	WKG_ENB_FOR_INTR125		RW	1
28	WKG_ENB_FOR_INTR124		RW	1
27	WKG_ENB_FOR_INTR123		RW	1
26	WKG_ENB_FOR_INTR122		RW	1
25	WKG_ENB_FOR_INTR121		RW	1
24	WKG_ENB_FOR_INTR120		RW	1
23	WKG_ENB_FOR_INTR119		RW	1
22	WKG_ENB_FOR_INTR118		RW	1
21	WKG_ENB_FOR_INTR117		RW	1
20	WKG_ENB_FOR_INTR116		RW	1
19	WKG_ENB_FOR_INTR115		RW	1
18	WKG_ENB_FOR_INTR114		RW	1
17	WKG_ENB_FOR_INTR113		RW	1
16	WKG_ENB_FOR_INTR112		RW	1
15	WKG_ENB_FOR_INTR111		RW	1
14	WKG_ENB_FOR_INTR110		RW	1
13	WKG_ENB_FOR_INTR109		RW	1
12	WKG_ENB_FOR_INTR108		RW	1

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Bits	Field Name	Description	Type	Reset
11	WKG_ENB_FOR_INTR107		RW	1
10	WKG_ENB_FOR_INTR106		RW	1
9	WKG_ENB_FOR_INTR105		RW	1
8	WKG_ENB_FOR_INTR104		RW	1
7	WKG_ENB_FOR_INTR103		RW	1
6	WKG_ENB_FOR_INTR102		RW	1
5	WKG_ENB_FOR_INTR101		RW	1
4	WKG_ENB_FOR_INTR100		RW	1
3	WKG_ENB_FOR_INTR99		RW	1
2	WKG_ENB_FOR_INTR98		RW	1
1	WKG_ENB_FOR_INTR97		RW	1
0	WKG_ENB_FOR_INTR96		RW	1

Table 4-66. Register Call Summary for Register WKG_ENB_D_0

Dual Cortex-A15 MPU Subsystem Register Manual
- WUGEN_MPU Register Summary: [0]

Table 4-67. WKG_ENB_E_0

Address Offset	0x0000 001C		
Physical Address	0x4828 1020	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C0) from MPU_IRQ_128 to MPU_IRQ_159. Write 0x0: Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKG_ENB_FOR_INTR159	WKG_ENB_FOR_INTR158	WKG_ENB_FOR_INTR157	WKG_ENB_FOR_INTR156	WKG_ENB_FOR_INTR155	WKG_ENB_FOR_INTR154	WKG_ENB_FOR_INTR153	WKG_ENB_FOR_INTR152	WKG_ENB_FOR_INTR151	WKG_ENB_FOR_INTR150	WKG_ENB_FOR_INTR149	WKG_ENB_FOR_INTR148	WKG_ENB_FOR_INTR147	WKG_ENB_FOR_INTR146	WKG_ENB_FOR_INTR145	WKG_ENB_FOR_INTR144	WKG_ENB_FOR_INTR143	WKG_ENB_FOR_INTR142	WKG_ENB_FOR_INTR141	WKG_ENB_FOR_INTR140	WKG_ENB_FOR_INTR139	WKG_ENB_FOR_INTR138	WKG_ENB_FOR_INTR137	WKG_ENB_FOR_INTR136	WKG_ENB_FOR_INTR135	WKG_ENB_FOR_INTR134	WKG_ENB_FOR_INTR133	WKG_ENB_FOR_INTR132	WKG_ENB_FOR_INTR131	WKG_ENB_FOR_INTR130	WKG_ENB_FOR_INTR129	WKG_ENB_FOR_INTR128

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR159		RW	1
30	WKG_ENB_FOR_INTR158		RW	1
29	WKG_ENB_FOR_INTR157		RW	1
28	WKG_ENB_FOR_INTR156		RW	1
27	WKG_ENB_FOR_INTR155		RW	1
26	WKG_ENB_FOR_INTR154		RW	1
25	WKG_ENB_FOR_INTR153		RW	1
24	WKG_ENB_FOR_INTR152		RW	1
23	WKG_ENB_FOR_INTR151		RW	1
22	WKG_ENB_FOR_INTR150		RW	1
21	WKG_ENB_FOR_INTR149		RW	1
20	WKG_ENB_FOR_INTR148		RW	1
19	WKG_ENB_FOR_INTR147		RW	1

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Bits	Field Name	Description	Type	Reset
18	WKG_ENB_FOR_INTR146		RW	1
17	WKG_ENB_FOR_INTR145		RW	1
16	WKG_ENB_FOR_INTR144		RW	1
15	WKG_ENB_FOR_INTR143		RW	1
14	WKG_ENB_FOR_INTR142		RW	1
13	WKG_ENB_FOR_INTR141		RW	1
12	WKG_ENB_FOR_INTR140		RW	1
11	WKG_ENB_FOR_INTR139		RW	1
10	WKG_ENB_FOR_INTR138		RW	1
9	WKG_ENB_FOR_INTR137		RW	1
8	WKG_ENB_FOR_INTR136		RW	1
7	WKG_ENB_FOR_INTR135		RW	1
6	WKG_ENB_FOR_INTR134		RW	1
5	WKG_ENB_FOR_INTR133		RW	1
4	WKG_ENB_FOR_INTR132		RW	1
3	WKG_ENB_FOR_INTR131		RW	1
2	WKG_ENB_FOR_INTR130		RW	1
1	WKG_ENB_FOR_INTR129		RW	1
0	WKG_ENB_FOR_INTR128		RW	1

Table 4-68. Register Call Summary for Register WKG_ENB_E_0

Dual Cortex-A15 MPU Subsystem Register Manual

- WUGEN_MPU Register Summary: [0]

Table 4-69. WKG_CONTROL_1

Address Offset	0x0000 0400		
Physical Address	0x4828 1400	**Instance**	WUGEN_MPU
Description	Wake-up generator status register for MPU_C1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DOMAINRESET	MPU_WARM_RESET	MPU_COLD_RESET	RESERVED		EVENTO	STANDBYWFE	STANDBYWFI	RESERVED							

Bits	Field Name	Description	Type[1]	Reset
31:16	RESERVED	Reserved	R	0x0000
15	DOMAINRESET	MPU always-on power domain (PD_MPUAON) reset status bit. It shows if the reset occurred previously. 0x0: No reset occurred. 0x1: Reset occurred.	RW (WCtoClr)	0

(1) RW (WCtoClr) means that a register bit can be read and is cleared by a write of any value.

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Bits	Field Name	Description	Type[1]	Reset
14	MPU_WARM_RESET	This bit is set when the MPU_WARM_RESET signal is asserted. 0x0: MPU_WARM_RESET reset signal has not been asserted. 0x1: MPU_WARM_RESET reset request has been asserted.	RW (WCtoClr)	0
13	MPU_COLD_RESET	This bit is set when the MPU_COLD_RESET signal is asserted. 0x0: MPU_COLD_RESET reset signal has not been asserted. 0x1: MPU_COLD_RESET reset request has been asserted.	RW (WCtoClr)	0
12:11	RESERVED	Reserved	R	0x0
10	EVENTO	EVENTO status bit. The event output signal is active, when one SEV instruction is executed. This bit is set when a rising edge of EVENTO from CPU is detected. 0x0: Rising edge of EVENTO is not detected. 0x1: Rising edge of EVENTO is detected.	RW (WCtoClr)	0
9	STANDBYWFE	This bit gives software the visibility to track whether WFE mode have been entered. 0x0: WFE mode has not been entered. 0x1: WFE mode has been entered.	RW (WCtoClr)	0
8	STANDBYWFI	This bit gives software the visibility to track whether WFI mode have been entered. 0x0: WFI mode has not been entered. 0x1: WFI mode has been entered.	RW (WCtoClr)	0
7:0	RESERVED	Reserved	R	0x00

Table 4-70. Register Call Summary for Register WKG_CONTROL_1

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- Reset Distribution: [0]

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- WUGEN_MPU Register Summary: [1]

Table 4-71. WKG_ENB_A_1

Address Offset	0x0000 0410		
Physical Address	0x4828 1410	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C1) from MPU_IRQ_0 to MPU_IRQ_31. Write 0x0: Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKG_ENB_FOR_INTR31	WKG_ENB_FOR_INTR30	WKG_ENB_FOR_INTR29	WKG_ENB_FOR_INTR28	WKG_ENB_FOR_INTR27	WKG_ENB_FOR_INTR26	WKG_ENB_FOR_INTR25	WKG_ENB_FOR_INTR24	WKG_ENB_FOR_INTR23	WKG_ENB_FOR_INTR22	WKG_ENB_FOR_INTR21	WKG_ENB_FOR_INTR20	WKG_ENB_FOR_INTR19	WKG_ENB_FOR_INTR18	WKG_ENB_FOR_INTR17	WKG_ENB_FOR_INTR16	WKG_ENB_FOR_INTR15	WKG_ENB_FOR_INTR14	WKG_ENB_FOR_INTR13	WKG_ENB_FOR_INTR12	WKG_ENB_FOR_INTR11	WKG_ENB_FOR_INTR10	WKG_ENB_FOR_INTR9	RESERVED	WKG_ENB_FOR_INTR7	WKG_ENB_FOR_INTR6	RESERVED	WKG_ENB_FOR_INTR4	RESERVED	WKG_ENB_FOR_INTR2	WKG_ENB_FOR_INTR1	WKG_ENB_FOR_INTR0

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR31		RW	1
30	WKG_ENB_FOR_INTR30		RW	1
29	WKG_ENB_FOR_INTR29		RW	1

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Bits	Field Name	Description	Type	Reset
28	WKG_ENB_FOR_INTR28		RW	1
27	WKG_ENB_FOR_INTR27		RW	1
26	WKG_ENB_FOR_INTR26		RW	1
25	WKG_ENB_FOR_INTR25		RW	1
24	WKG_ENB_FOR_INTR24		RW	1
23	WKG_ENB_FOR_INTR23		RW	1
22	WKG_ENB_FOR_INTR22		RW	1
21	WKG_ENB_FOR_INTR21		RW	1
20	WKG_ENB_FOR_INTR20		RW	1
19	WKG_ENB_FOR_INTR19		RW	1
18	WKG_ENB_FOR_INTR18		RW	1
17	WKG_ENB_FOR_INTR17		RW	1
16	WKG_ENB_FOR_INTR16		RW	1
15	WKG_ENB_FOR_INTR15		RW	1
14	WKG_ENB_FOR_INTR14		RW	1
13	WKG_ENB_FOR_INTR13		RW	1
12	WKG_ENB_FOR_INTR12		RW	1
11	WKG_ENB_FOR_INTR11		RW	1
10	WKG_ENB_FOR_INTR10		RW	1
9	WKG_ENB_FOR_INTR9		RW	1
8	WKG_ENB_FOR_INTR8		RW	0[(1)]
7	WKG_ENB_FOR_INTR7		RW	1
6	WKG_ENB_FOR_INTR6		RW	1
5	WKG_ENB_FOR_INTR5		RW	1
4	WKG_ENB_FOR_INTR4		RW	1
3	WKG_ENB_FOR_INTR3		RW	1
2	WKG_ENB_FOR_INTR2		RW	1
1	WKG_ENB_FOR_INTR1		RW	1
0	WKG_ENB_FOR_INTR0		RW	1

(1) The reset value is 0x0 by safety reasons.

Table 4-72. Register Call Summary for Register WKG_ENB_A_1

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- WUGEN_MPU Register Summary: [0]

Table 4-73. WKG_ENB_B_1

Address Offset	0x0000 0414		
Physical Address	0x4828 1414	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C1) from MPU_IRQ_32 to MPU_IRQ_63. Write 0x0: Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	WKG_ENB_FOR_INTR62	WKG_ENB_FOR_INTR61	RESERVED	WKG_ENB_FOR_INTR59	WKG_ENB_FOR_INTR58	WKG_ENB_FOR_INTR57	WKG_ENB_FOR_INTR56	RESERVED	RESERVED	WKG_ENB_FOR_INTR53	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR48	WKG_ENB_FOR_INTR47	WKG_ENB_FOR_INTR46	WKG_ENB_FOR_INTR45	WKG_ENB_FOR_INTR44	WKG_ENB_FOR_INTR43	WKG_ENB_FOR_INTR42	WKG_ENB_FOR_INTR41	WKG_ENB_FOR_INTR40	WKG_ENB_FOR_INTR39	WKG_ENB_FOR_INTR38	WKG_ENB_FOR_INTR37	WKG_ENB_FOR_INTR36	RESERVED	WKG_ENB_FOR_INTR34	WKG_ENB_FOR_INTR33	WKG_ENB_FOR_INTR32

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR63		RW	1
30	WKG_ENB_FOR_INTR62		RW	1
29	WKG_ENB_FOR_INTR61		RW	1
28	WKG_ENB_FOR_INTR60		RW	1
27	WKG_ENB_FOR_INTR59		RW	1
26	WKG_ENB_FOR_INTR58		RW	1
25	WKG_ENB_FOR_INTR57		RW	1
24	WKG_ENB_FOR_INTR56		RW	1
23	WKG_ENB_FOR_INTR55		RW	1
22	WKG_ENB_FOR_INTR54		RW	1
21	WKG_ENB_FOR_INTR53		RW	1
20	WKG_ENB_FOR_INTR52		RW	1
19	WKG_ENB_FOR_INTR51		RW	1
18	WKG_ENB_FOR_INTR50		RW	1
17	WKG_ENB_FOR_INTR49		RW	1
16	WKG_ENB_FOR_INTR48		RW	1
15	WKG_ENB_FOR_INTR47		RW	1
14	WKG_ENB_FOR_INTR46		RW	1
13	WKG_ENB_FOR_INTR45		RW	1
12	WKG_ENB_FOR_INTR44		RW	1
11	WKG_ENB_FOR_INTR43		RW	1
10	WKG_ENB_FOR_INTR42		RW	1
9	WKG_ENB_FOR_INTR41		RW	1
8	WKG_ENB_FOR_INTR40		RW	1
7	WKG_ENB_FOR_INTR39		RW	1
6	WKG_ENB_FOR_INTR38		RW	1
5	WKG_ENB_FOR_INTR37		RW	1
4	WKG_ENB_FOR_INTR36		RW	1
3	WKG_ENB_FOR_INTR35		RW	1
2	WKG_ENB_FOR_INTR34		RW	1
1	WKG_ENB_FOR_INTR33		RW	1
0	WKG_ENB_FOR_INTR32		RW	1

Table 4-74. Register Call Summary for Register WKG_ENB_B_1

Dual Cortex-A15 MPU Subsystem Register Manual

- WUGEN_MPU Register Summary: [0]

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Table 4-75. WKG_ENB_C_1

Address Offset	0x0000 0418		
Physical Address	0x4828 1418	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C1) from MPU_IRQ_64 to MPU_IRQ_95. Write 0x0: Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	WKG_ENB_FOR_INTR94	WKG_ENB_FOR_INTR93	WKG_ENB_FOR_INTR92	WKG_ENB_FOR_INTR91	WKG_ENB_FOR_INTR90	WKG_ENB_FOR_INTR89	WKG_ENB_FOR_INTR88	WKG_ENB_FOR_INTR87	WKG_ENB_FOR_INTR86	RESERVED	WKG_ENB_FOR_INTR84	WKG_ENB_FOR_INTR83	RESERVED	RESERVED	WKG_ENB_FOR_INTR80	RESERVED	WKG_ENB_FOR_INTR78	WKG_ENB_FOR_INTR77	WKG_ENB_FOR_INTR76	WKG_ENB_FOR_INTR75	WKG_ENB_FOR_INTR74	WKG_ENB_FOR_INTR73	WKG_ENB_FOR_INTR72	WKG_ENB_FOR_INTR71	WKG_ENB_FOR_INTR70	WKG_ENB_FOR_INTR69	WKG_ENB_FOR_INTR68	WKG_ENB_FOR_INTR67	WKG_ENB_FOR_INTR66	WKG_ENB_FOR_INTR65	RESERVED

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR95		RW	1
30	WKG_ENB_FOR_INTR94		RW	1
29	WKG_ENB_FOR_INTR93		RW	1
28	WKG_ENB_FOR_INTR92		RW	1
27	WKG_ENB_FOR_INTR91		RW	1
26	WKG_ENB_FOR_INTR90		RW	1
25	WKG_ENB_FOR_INTR89		RW	1
24	WKG_ENB_FOR_INTR88		RW	1
23	WKG_ENB_FOR_INTR87		RW	1
22	WKG_ENB_FOR_INTR86		RW	1
21	WKG_ENB_FOR_INTR85		RW	1
20	WKG_ENB_FOR_INTR84		RW	1
19	WKG_ENB_FOR_INTR83		RW	1
18	WKG_ENB_FOR_INTR82		RW	1
17	WKG_ENB_FOR_INTR81		RW	1
16	WKG_ENB_FOR_INTR80		RW	1
15	WKG_ENB_FOR_INTR79		RW	1
14	WKG_ENB_FOR_INTR78		RW	1
13	WKG_ENB_FOR_INTR77		RW	1
12	WKG_ENB_FOR_INTR76		RW	1
11	WKG_ENB_FOR_INTR75		RW	1
10	WKG_ENB_FOR_INTR74		RW	1
9	WKG_ENB_FOR_INTR73		RW	1
8	WKG_ENB_FOR_INTR72		RW	1
7	WKG_ENB_FOR_INTR71		RW	1
6	WKG_ENB_FOR_INTR70		RW	1
5	WKG_ENB_FOR_INTR69		RW	1
4	WKG_ENB_FOR_INTR68		RW	1
3	WKG_ENB_FOR_INTR67		RW	1
2	WKG_ENB_FOR_INTR66		RW	1
1	WKG_ENB_FOR_INTR65		RW	1
0	WKG_ENB_FOR_INTR64		RW	1

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Table 4-76. Register Call Summary for Register WKG_ENB_C_1

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- WUGEN_MPU Register Summary: [0]

Table 4-77. WKG_ENB_D_1

Address Offset	0x0000 041C		
Physical Address	0x4828 141C	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C1) from MPU_IRQ_96 to MPU_IRQ_127. Write 0x0: Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR120	WKG_ENB_FOR_INTR119	RESERVED	RESERVED	RESERVED	RESERVED	WKG_ENB_FOR_INTR114	WKG_ENB_FOR_INTR113	WKG_ENB_FOR_INTR112	WKG_ENB_FOR_INTR111	WKG_ENB_FOR_INTR110	WKG_ENB_FOR_INTR109	RESERVED	WKG_ENB_FOR_INTR107	RESERVED	RESERVED	WKG_ENB_FOR_INTR104	WKG_ENB_FOR_INTR103	WKG_ENB_FOR_INTR102	WKG_ENB_FOR_INTR101	WKG_ENB_FOR_INTR100	WKG_ENB_FOR_INTR99	WKG_ENB_FOR_INTR98	WKG_ENB_FOR_INTR97	WKG_ENB_FOR_INTR96

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR127		RW	1
30	WKG_ENB_FOR_INTR126		RW	1
29	WKG_ENB_FOR_INTR125		RW	1
28	WKG_ENB_FOR_INTR124		RW	1
27	WKG_ENB_FOR_INTR123		RW	1
26	WKG_ENB_FOR_INTR122		RW	1
25	WKG_ENB_FOR_INTR121		RW	1
24	WKG_ENB_FOR_INTR120		RW	1
23	WKG_ENB_FOR_INTR119		RW	1
22	WKG_ENB_FOR_INTR118		RW	1
21	WKG_ENB_FOR_INTR117		RW	1
20	WKG_ENB_FOR_INTR116		RW	1
19	WKG_ENB_FOR_INTR115		RW	1
18	WKG_ENB_FOR_INTR114		RW	1
17	WKG_ENB_FOR_INTR113		RW	1
16	WKG_ENB_FOR_INTR112		RW	1
15	WKG_ENB_FOR_INTR111		RW	1
14	WKG_ENB_FOR_INTR110		RW	1
13	WKG_ENB_FOR_INTR109		RW	1
12	WKG_ENB_FOR_INTR108		RW	1
11	WKG_ENB_FOR_INTR107		RW	1
10	WKG_ENB_FOR_INTR106		RW	1
9	WKG_ENB_FOR_INTR105		RW	1
8	WKG_ENB_FOR_INTR104		RW	1
7	WKG_ENB_FOR_INTR103		RW	1
6	WKG_ENB_FOR_INTR102		RW	1
5	WKG_ENB_FOR_INTR101		RW	1

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Bits	Field Name	Description	Type	Reset
4	WKG_ENB_FOR_INTR100		RW	1
3	WKG_ENB_FOR_INTR99		RW	1
2	WKG_ENB_FOR_INTR98		RW	1
1	WKG_ENB_FOR_INTR97		RW	1
0	WKG_ENB_FOR_INTR96		RW	1

Table 4-78. Register Call Summary for Register WKG_ENB_D_1

Dual Cortex-A15 MPU Subsystem Register Manual

- WUGEN_MPU Register Summary: [0]

Table 4-79. WKG_ENB_E_1

Address Offset	0x0000 041C		
Physical Address	0x4828 1420	**Instance**	WUGEN_MPU
Description	This register enables the interrupts (for MPU_C1) from MPU_IRQ_128 to MPU_IRQ_159. Write 0x0: Disable interrupt. Write 0x1: Enable interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKG_ENB_FOR_INTR159	WKG_ENB_FOR_INTR158	WKG_ENB_FOR_INTR157	WKG_ENB_FOR_INTR156	WKG_ENB_FOR_INTR155	WKG_ENB_FOR_INTR154	WKG_ENB_FOR_INTR153	WKG_ENB_FOR_INTR152	WKG_ENB_FOR_INTR151	WKG_ENB_FOR_INTR150	WKG_ENB_FOR_INTR149	WKG_ENB_FOR_INTR148	WKG_ENB_FOR_INTR147	WKG_ENB_FOR_INTR146	WKG_ENB_FOR_INTR145	WKG_ENB_FOR_INTR144	WKG_ENB_FOR_INTR143	WKG_ENB_FOR_INTR142	WKG_ENB_FOR_INTR141	WKG_ENB_FOR_INTR140	WKG_ENB_FOR_INTR139	WKG_ENB_FOR_INTR138	WKG_ENB_FOR_INTR137	WKG_ENB_FOR_INTR136	WKG_ENB_FOR_INTR135	WKG_ENB_FOR_INTR134	WKG_ENB_FOR_INTR133	WKG_ENB_FOR_INTR132	WKG_ENB_FOR_INTR131	WKG_ENB_FOR_INTR130	WKG_ENB_FOR_INTR129	WKG_ENB_FOR_INTR128

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR159		RW	1
30	WKG_ENB_FOR_INTR158		RW	1
29	WKG_ENB_FOR_INTR157		RW	1
28	WKG_ENB_FOR_INTR156		RW	1
27	WKG_ENB_FOR_INTR155		RW	1
26	WKG_ENB_FOR_INTR154		RW	1
25	WKG_ENB_FOR_INTR153		RW	1
24	WKG_ENB_FOR_INTR152		RW	1
23	WKG_ENB_FOR_INTR151		RW	1
22	WKG_ENB_FOR_INTR150		RW	1
21	WKG_ENB_FOR_INTR149		RW	1
20	WKG_ENB_FOR_INTR148		RW	1
19	WKG_ENB_FOR_INTR147		RW	1
18	WKG_ENB_FOR_INTR146		RW	1
17	WKG_ENB_FOR_INTR145		RW	1
16	WKG_ENB_FOR_INTR144		RW	1
15	WKG_ENB_FOR_INTR143		RW	1
14	WKG_ENB_FOR_INTR142		RW	1
13	WKG_ENB_FOR_INTR141		RW	1
12	WKG_ENB_FOR_INTR140		RW	1

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Bits	Field Name	Description	Type	Reset
11	WKG_ENB_FOR_INTR139		RW	1
10	WKG_ENB_FOR_INTR138		RW	1
9	WKG_ENB_FOR_INTR137		RW	1
8	WKG_ENB_FOR_INTR136		RW	1
7	WKG_ENB_FOR_INTR135		RW	1
6	WKG_ENB_FOR_INTR134		RW	1
5	WKG_ENB_FOR_INTR133		RW	1
4	WKG_ENB_FOR_INTR132		RW	1
3	WKG_ENB_FOR_INTR131		RW	1
2	WKG_ENB_FOR_INTR130		RW	1
1	WKG_ENB_FOR_INTR129		RW	1
0	WKG_ENB_FOR_INTR128		RW	1

Table 4-80. Register Call Summary for Register WKG_ENB_E_1

Dual Cortex-A15 MPU Subsystem Register Manual
- WUGEN_MPU Register Summary: [0]

Table 4-81. AUX_CORE_BOOT_0

Address Offset	0x800		
Physical Address	0x4828 1800	**Instance**	WUGEN_MPU
Description	This register is used by the ROM code and OS during SMP boot. It is intended to store the execution start address of MPU_C1. When needed, the SMP OS (executing on the MPU_C0) wakes up MPU_C1 by executing a SEV command. MPU_C0 needs to communicate some start-up information (for example, the starting address) to MPU_C1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX_CORE_BOOT_0																															

Bits	Field Name	Description	Type	Reset
31:0	AUX_CORE_BOOT_0	SMP boot register	RW	0x00000000

Table 4-82. Register Call Summary for Register AUX_CORE_BOOT_0

Dual Cortex-A15 MPU Subsystem Register Manual
- WUGEN_MPU Register Summary: [0]
- WUGEN_MPU Register Description: [1]

Table 4-83. AUX_CORE_BOOT_1

Address Offset	0x804		
Physical Address	0x4828 1804	**Instance**	WUGEN_MPU
Description	This register is used by the ROM code and OS during SMP boot. It is used to indicate boot status to either MPU core. When MPU_C1 receives an event (caused by the SEV command), it continues execution in the ROM, which set up the code to branch to the address signaled by MPU_C0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX_CORE_BOOT_1																															

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Bits	Field Name	Description	Type	Reset
31:0	AUX_CORE_BOOT_1	SMP boot register	RW	0x00000000

Table 4-84. Register Call Summary for Register AUX_CORE_BOOT_1

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- WUGEN_MPU Register Summary: [0]
- WUGEN_MPU Register Description: [1]

Table 4-85. STM_HWEVENTS_INV

Address Offset	0x0000 0808		
Physical Address	0x4828 1808	**Instance**	WUGEN_MPU
Description	Gives programmable control of inverting or not inverting MPUHWDBGOUT[31:0] going to HWEVENTS[31:0] input of CS_STM		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STM_HWEVENT_INV_31	STM_HWEVENT_INV_30	STM_HWEVENT_INV_29	STM_HWEVENT_INV_28	STM_HWEVENT_INV_27	STM_HWEVENT_INV_26	STM_HWEVENT_INV_25	STM_HWEVENT_INV_24	STM_HWEVENT_INV_23	STM_HWEVENT_INV_22	STM_HWEVENT_INV_21	STM_HWEVENT_INV_20	STM_HWEVENT_INV_19	STM_HWEVENT_INV_18	STM_HWEVENT_INV_17	STM_HWEVENT_INV_16	STM_HWEVENT_INV_15	STM_HWEVENT_INV_14	STM_HWEVENT_INV_13	STM_HWEVENT_INV_12	STM_HWEVENT_INV_11	STM_HWEVENT_INV_10	STM_HWEVENT_INV_9	STM_HWEVENT_INV_8	STM_HWEVENT_INV_7	STM_HWEVENT_INV_6	STM_HWEVENT_INV_5	STM_HWEVENT_INV_4	STM_HWEVENT_INV_3	STM_HWEVENT_INV_2	STM_HWEVENT_INV_1	STM_HWEVENT_INV_0

Bits	Field Name	Description	Type	Reset
31	STM_HWEVENT_INV_31	Polarity inversion control for MPUHWDBGOUT31 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
30	STM_HWEVENT_INV_30	Polarity inversion control for MPUHWDBGOUT30 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
29	STM_HWEVENT_INV_29	Polarity inversion control for MPUHWDBGOUT29 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
28	STM_HWEVENT_INV_28	Polarity inversion control for MPUHWDBGOUT28 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
27	STM_HWEVENT_INV_27	Polarity inversion control for MPUHWDBGOUT27 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
26	STM_HWEVENT_INV_26	Polarity inversion control for MPUHWDBGOUT26 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
25	STM_HWEVENT_INV_25	Polarity inversion control for MPUHWDBGOUT25 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0

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Bits	Field Name	Description	Type	Reset
24	STM_HWEVENT_INV_24	Polarity inversion control for MPUHWDBGOUT24 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
23	STM_HWEVENT_INV_23	Polarity inversion control for MPUHWDBGOUT23 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
22	STM_HWEVENT_INV_22	Polarity inversion control for MPUHWDBGOUT22 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
21	STM_HWEVENT_INV_21	Polarity inversion control for MPUHWDBGOUT21 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
20	STM_HWEVENT_INV_20	Polarity inversion control for MPUHWDBGOUT20 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
19	STM_HWEVENT_INV_19	Polarity inversion control for MPUHWDBGOUT19 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
18	STM_HWEVENT_INV_18	Polarity inversion control for MPUHWDBGOUT18 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
17	STM_HWEVENT_INV_17	Polarity inversion control for MPUHWDBGOUT17 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
16	STM_HWEVENT_INV_16	Polarity inversion control for MPUHWDBGOUT16 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
15	STM_HWEVENT_INV_15	Polarity inversion control for MPUHWDBGOUT15 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
14	STM_HWEVENT_INV_14	Polarity inversion control for MPUHWDBGOUT14 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
13	STM_HWEVENT_INV_13	Polarity inversion control for MPUHWDBGOUT13 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
12	STM_HWEVENT_INV_12	Polarity inversion control for MPUHWDBGOUT12 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
11	STM_HWEVENT_INV_11	Polarity inversion control for MPUHWDBGOUT11 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
10	STM_HWEVENT_INV_10	Polarity inversion control for MPUHWDBGOUT10 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
9	STM_HWEVENT_INV_9	Polarity inversion control for MPUHWDBGOUT9 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0

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Bits	Field Name	Description	Type	Reset
8	STM_HWEVENT_INV_8	Polarity inversion control for MPUHWDBGOUT8 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
7	STM_HWEVENT_INV_7	Polarity inversion control for MPUHWDBGOUT7 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
6	STM_HWEVENT_INV_6	Polarity inversion control for MPUHWDBGOUT6 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
5	STM_HWEVENT_INV_5	Polarity inversion control for MPUHWDBGOUT5 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
4	STM_HWEVENT_INV_4	Polarity inversion control for MPUHWDBGOUT4 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
3	STM_HWEVENT_INV_3	Polarity inversion control for MPUHWDBGOUT3 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
2	STM_HWEVENT_INV_2	Polarity inversion control for MPUHWDBGOUT2 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
1	STM_HWEVENT_INV_1	Polarity inversion control for MPUHWDBGOUT1 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0
0	STM_HWEVENT_INV_0	Polarity inversion control for MPUHWDBGOUT0 signal. 0x0: Polarity unchanged 0x1 Polarity inverted	RW	0

Table 4-86. Register Call Summary for Register STM_HWEVENTS_INV

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- WUGEN_MPU Register Summary: [0]

Table 4-87. AMBA_IF_MODE

Address Offset	0x0000 080C
Physical Address	0x4828 180C **Instance** WUGEN_MPU
Description	This register controls the MPU core interface tie-off values for BI, BO, BCM and SBD. This register is located in MPU always-on domain and is reset by MPUAON_RST.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										ES2_PM_MODE	APB_FENCE_EN	BI	BO	BCM	SBD

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved. Ignored on write and zero on read.	R	0x000 0000
5	ES2_PM_MODE	Enables ES2 PM Mode. 0x0: ES1 behavior, MPU cores would enter and exit OFF mode together. 0x1: ES2 behavior, MPU cores are allowed to enter/exit OFF mode independently.	RW	0
4	APB_FENCE_EN	Enables APB fencing logic.	RW	1
3	BI	BROADCASTINNER input of MPU core.	RW	0
2	BO	BROADCASTOUTER input of MPU core.	RW	0
1	BCM	BROADCASTMAINTENANCE input of MPU core.	RW	0
0	SBD	SYSBARDISABLE input of MPU core.	RW	1

Table 4-88. Register Call Summary for Register AMBA_IF_MODE

Dual Cortex-A15 MPU Subsystem Functional Description
- Power States of MPU_Cx: [0] [1] [2] [3]
- MPU Subsystem AMBA Interface Configuration: [4] [5]

Dual Cortex-A15 MPU Subsystem Register Manual
- WUGEN_MPU Register Summary: [6]

Table 4-89. TIMESTAMPCYCLELO

Address Offset	0x0000 0C08		
Physical Address	0x4828 1C08	**Instance**	WUGEN_MPU
Description	Lower 32 bits of the 48-bit timestamp counter value		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER_31_0																															

Bits	Field Name	Description	Type	Reset
31:0	COUNTER_31_0	Lower 32 bits of the 48-bit timestamp counter value.	R	0x000 0000

Table 4-90. Register Call Summary for Register TIMESTAMPCYCLELO

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- WUGEN_MPU Register Summary: [0]

Table 4-91. TIMESTAMPCYCLEHI

Address Offset	0x0000 0C0C		
Physical Address	0x4828 1C0C	**Instance**	WUGEN_MPU
Description	Higher 16 bits of the 48-bit timestamp counter value		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																COUNTER_47_32															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved. Ignored on write and zero on read.	R	0x0000
15:0	COUNTER_47_32	Higher 16 bits of the timestamp counter value.	R	0x0000

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Table 4-92. Register Call Summary for Register TIMESTAMPCYCLEHI

Dual Cortex-A15 MPU Subsystem Register Manual
• WUGEN_MPU Register Summary: [0]

4.4.11 WD_TIMER_MPU Registers

4.4.11.1 WD_TIMER_MPU Register Summary

Table 4-93. WD_TIMER_MPU Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	WD_TIMER_MPU Physical Address
WDT_LOAD_REGISTER_i [(1)]	RW	32	0x0000 0000 + (0x20 * i)	0x482A 0000 + (0x20 * i)
WDT_COUNT_REGISTER_i [(1)]	R	32	0x0000 0004 + (0x20 * i)	0x482A 0004 + (0x20 * i)
WDT_WARNING_REGISTER_i [(1)]	RW	32	0x0000 0008 + (0x20 * i)	0x482A 0008 + (0x20 * i)
WDT_PRESCALER_REGISTER_i [(1)]	RW	32	0x0000 000C + (0x20 * i)	0x482A 000C + (0x20 * i)
WDT_CONTROL_REGISTER_i [(1)]	RW	32	0x0000 0010 + (0x20 * i)	0x482A 0010 + (0x20 * i)
WDT_RESET_STATUS_REGISTER_i [(1)]	RW	32	0x0000 0014 + (0x20 * i)	0x482A 0014 + (0x20 * i)

(1) i = 0 to 1

4.4.11.2 WD_TIMER_MPU Register Description

Table 4-94. WDT_LOAD_REGISTER_i

Address Offset	0x0000 0000 + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x482A 0000 + (0x20 * i)	**Instance**	WD_TIMER_MPU
Description	When this register is stored, the WDT_COUNT_REGISTER_i is immediately loaded with this value and the prescaler state is cleared. This register is reset by warm reset of the corresponding MPU core.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEWCOUNT																															

Bits	Field Name	Description	Type	Reset
31:0	NEWCOUNT	New value to load into WDT_COUNT_REGISTER_i.	RW	0x0000 0000

Table 4-95. Register Call Summary for Register WDT_LOAD_REGISTER_i

Dual Cortex-A15 MPU Subsystem Functional Description
• MPU Watchdog Timer: [0] [1] [2] [3] [4]
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• WD_TIMER_MPU Register Summary: [5]
• WD_TIMER_MPU Register Description: [6]

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Table 4-96. WDT_COUNT_REGISTER_i

Address Offset	0x0000 0004 + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x482A 0004 + (0x20 * i)	**Instance**	WD_TIMER_MPU
Description	This register is a 32-bit decrementing counter. The decrement rate is programmed in the WDT_PRESCALER_REGISTER_i. The WDT_COUNT_REGISTER_i can be read to get the current count. It decrements if the WD_TIMER_MPU_Cx is enabled (WDT_CONTROL_REGISTER_i[0] ENABLE = 0x1). If the processor corresponding to the watchdog channel is in debug state, the counter does not decrement until the processor returns to non-debug state. The WDT_COUNT_REGISTER_i decrements down to zero and stops. The only way to update the WDT_COUNT_REGISTER_i is to write to the WDT_LOAD_REGISTER_i. If a software failure prevents the WDT_COUNT_REGISTER_i from being refreshed, the WDT_COUNT_REGISTER_i reaches zero, the watchdog timeout status flag is set and all interrupt requests or reset requests enabled in the WDT_CONTROL_REGISTER_i are signalled. If a reset request is enabled, the global PRCM is then responsible for resetting the MPUSS. Debug state is inferred by monitoring the DBGACK signal corresponding to this core. This register is reset by warm reset of the corresponding MPU core.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENTCOUNT																															

Bits	Field Name	Description	Type	Reset
31:0	CURRENTCOUNT	Current count of the WD_TIMER_MPU.	R	0x0000 0000

Table 4-97. Register Call Summary for Register WDT_COUNT_REGISTER_i

Dual Cortex-A15 MPU Subsystem Functional Description

- MPU Watchdog Timer: [0] [1] [2]

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- WD_TIMER_MPU Register Summary: [3]
- WD_TIMER_MPU Register Description: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Table 4-98. WDT_WARNING_REGISTER_i

Address Offset	0x0000 0008 + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x482A 0008 + (0x20 * i)	**Instance**	WD_TIMER_MPU
Description	The WDT_COUNT_REGISTER_i is compared to the WDT_WARNING_REGISTER_i. If WDT_COUNT_REGISTER_i is less than or equal to the WDT_WARNING_REGISTER_i and WDT_CONTROL_REGISTER_i[8] WARNEN = 0b1, a warning interrupt is signalled to the INTC_MPU. The warning condition can be used to signal an interrupt that gives software a notice that the WD_TIMER_MPU_Cx is getting close to a timeout, when a more serious action should be taken.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WARNING_WATERMARK																															

Bits	Field Name	Description	Type	Reset
31:0	WARNING_WATERMARK	A warning condition occurs when the WDT_COUNT_REGISTER_i value is less than or equal to the WDT_WARNING_REGISTER_i.	RW	0x0000 0000

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Table 4-99. Register Call Summary for Register WDT_WARNING_REGISTER_i

Dual Cortex-A15 MPU Subsystem Functional Description
- MPU Watchdog Timer: [0] [1] [2]

Dual Cortex-A15 MPU Subsystem Register Manual
- WD_TIMER_MPU Register Summary: [3]
- WD_TIMER_MPU Register Description: [4] [5] [6]

Table 4-100. WDT_PRESCALER_REGISTER_i

Address Offset	0x0000 000C + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x482A 000C + (0x20 * i)	**Instance**	WD_TIMER_MPU
Description	This register is used to set the count rate of the WD_TIMER_MPU_Cx counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRESCALER							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved. Ignored on writes. Reads return 0s.	R	0x00 0000
9:0	PRESCALER	Sets the prescaler ratio. WDT_COUNT_REGISTER_i decrements every (PRESCALER + 1) MPU_DPLL_CLK clocks. Note: If the prescaler is set to (MPU_DPLL_CLK [in MHz] - 1), the WD_TIMER_MPU_Cx counter counts at a 1 microsecond rate.	RW	0x000

Table 4-101. Register Call Summary for Register WDT_PRESCALER_REGISTER_i

Dual Cortex-A15 MPU Subsystem Functional Description
- MPU Watchdog Timer: [0] [1]

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- WD_TIMER_MPU Register Summary: [2]
- WD_TIMER_MPU Register Description: [3]

Table 4-102. WDT_CONTROL_REGISTER_i

Address Offset	0x0000 0010 + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x482A 0010 + (0x20 * i)	**Instance**	WD_TIMER_MPU
Description	This register controls the behavior of the WD_TIMER_MPU_Cx. This register is reset by warm reset of the corresponding MPU core.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WARNEN	RESERVED		MULTITO	SOCRSTEN	MPUSSRSTEN	CPURSTEN	INTREN	ENABLE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved. Ignored on writes. Reads return 0s.	R	0x00 0000
8	WARNEN	Warning Interrupt Enable. If this bit is set and the warning watermark test is true, a warning interrupt is generated to the INTC_MPU.	RW	0
7:4	RESERVED	Reserved. Ignored on writes. Reads return 0s.	R	0x0

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Bits	Field Name	Description	Type	Reset
3	MPUSSRSTEN	MPUSS Reset Enable. If this field is 0b1 when the timer reaches zero, a request is sent to the PRCM to reset the MPUSS including both MPU cores.	RW	0
2	RESERVED	Reserved. Ignored on writes. Reads return 0s.	R	0
1	INTREN	Interrupt Enable. If this field is 0b1 when the timer reaches zero, an interrupt request is sent to the INTC_MPU.	RW	0
0	ENABLE	Enable for WD_TIMER_MPU_Cx. 0: WD_TIMER_MPU_Cx is disabled. It will not count down and it will not generate a reset request. All WD_TIMER_MPU_Cx registers may be accessed. 1: WD_TIMER_MPU_Cx is enabled. It will count down and generate a reset request if it reaches 0. This bit is reset by warm or power-on reset.	RW	0

Table 4-103. Register Call Summary for Register WDT_CONTROL_REGISTER_i

Dual Cortex-A15 MPU Subsystem Functional Description
- MPU Watchdog Timer: [0] [1] [2] [3] [4] [5] [6]

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- WD_TIMER_MPU Register Summary: [7]
- WD_TIMER_MPU Register Description: [8] [9] [10] [11] [12]

Table 4-104. WDT_RESET_STATUS_REGISTER_i

Address Offset	0x0000 0014 + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x482A 0014 + (0x20 * i)	**Instance**	WD_TIMER_MPU
Description	The TO bit indicated that this WD_TIMER_MPU_Cx has timed out. This might be used to figure out which WD_TIMER_MPU_Cx signalled a reset. This register is not reset by warm reset, but only by cold reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WARN	TO

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved. Ignored on writes. Reads return 0s.	R	0x0000 0000
1	WARN	Warning. Indicates that the count has passed the warning watermark level while the WDT_CONTROL_REGISTER_i[8] WARNEN bit was set. Write a '1' to this bit to reset it.	RW W1toClr	0
0	TO	Timeout. Indicates the WDT_COUNT_REGISTER_i has reached zero (timed out) and the signalling enabled in the WDT_CONTROL_REGISTER_i has occurred. Can be used to determine which WD_TIMER_MPU_Cx instance caused a reset. Write a '1' to this bit to reset it.	RW W1toClr	0

Table 4-105. Register Call Summary for Register WDT_RESET_STATUS_REGISTER_i

Dual Cortex-A15 MPU Subsystem Functional Description
- MPU Watchdog Timer: [0] [1]

Dual Cortex-A15 MPU Subsystem Register Manual
- WD_TIMER_MPU Register Summary: [2]

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4.4.12 AXI2OCP_MISC Registers

4.4.12.1 AXI2OCP_MISC Register Summary

Table 4-106. AXI2OCP_MISC Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	AXI2OCP_MISC Base Address
MA_PRIORITY	RW	32	0x0	0x482A 2000

4.4.12.2 AXI2OCP_MISC Register Description

Table 4-107. MA_PRIORITY

Address Offset	0x0000 0000		
Physical Address	0x482A 2000	**Instance**	AXI2OCP_MISC
Description	Memory adapter priority register. This register indicates the priority of memory access from MA_MPU to EMIF. This priority is used by EMIF in scheduling MA_MPU access to EMIF. 0x0 is lowest priority and 0x7 is highest priority.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							HIMEM_INTERLEAVE_UN	RESERVED						PRIORITY	

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x00 0000
8	HIMEM_INTERLEAVE_UN	HIMEM_INTERLEAVE_UN	RW	0
7:3	RESERVED	Reserved	R	0x00
2:0	PRIORITY	MA_MPU priority value	RW	0x4

Table 4-108. Register Call Summary for Register MA_PRIORITY

Dual Cortex-A15 MPU Subsystem Functional Description
- AXI2OCP: [0]
- Interleaving: [1]

Dual Cortex-A15 MPU Subsystem Register Manual
- AXI2OCP_MISC Register Summary: [2]

4.4.13 MA_MPU_LSM Registers

4.4.13.1 MA_MPU_LSM Register Summary

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Table 4-109. MA_MPU_LSM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MA_MPU_LSM Base Address
RESERVED	R	32	0x0000 0010	0x482A F010
MA_LISA_LOCK	RW	32	0x0000 001C	0x482A F01C
MA_LISA_MAP_i [(1)]	RW	32	0x0000 0040 + (0x4 * i)	0x482A F040 + (0x4 * i)

(1) i = 0 to 3

4.4.13.2 MA_MPU_LSM Register Description

For the description of the MA_MPU_LSM registers, see Section 15.2.6, *DMM Register Manual*, in Chapter 15, *Memory Subsystem*, where MA_LISA_LOCK corresponds to the DMM_LISA_LOCK register description, and MA_LISA_MAP_i corresponds to the DMM_LISA_MAP_i register description.

4.4.14 MA_MPU_WP Registers

For information about the MA_MPU_WP registers and their description, see Chapter 29, *On-Chip Debug Support*.

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DSP Subsystem

This chapter describes the digital signal processor (DSP) subsystem of the device.

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5.2 DSP Subsystem Integration 1131
5.3 DSP Subsystem Functional Description 1134
5.4 DSP Subsystem Programming Guide 1173
5.5 DSP Subsystem Register Manual 1194

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5.1 DSP Subsystem Overview

The device includes the digital signal processor (DSP) subsystem, based on a derivative of the TMS320DMC64x+™ very long instruction word (VLIW) DSP core.

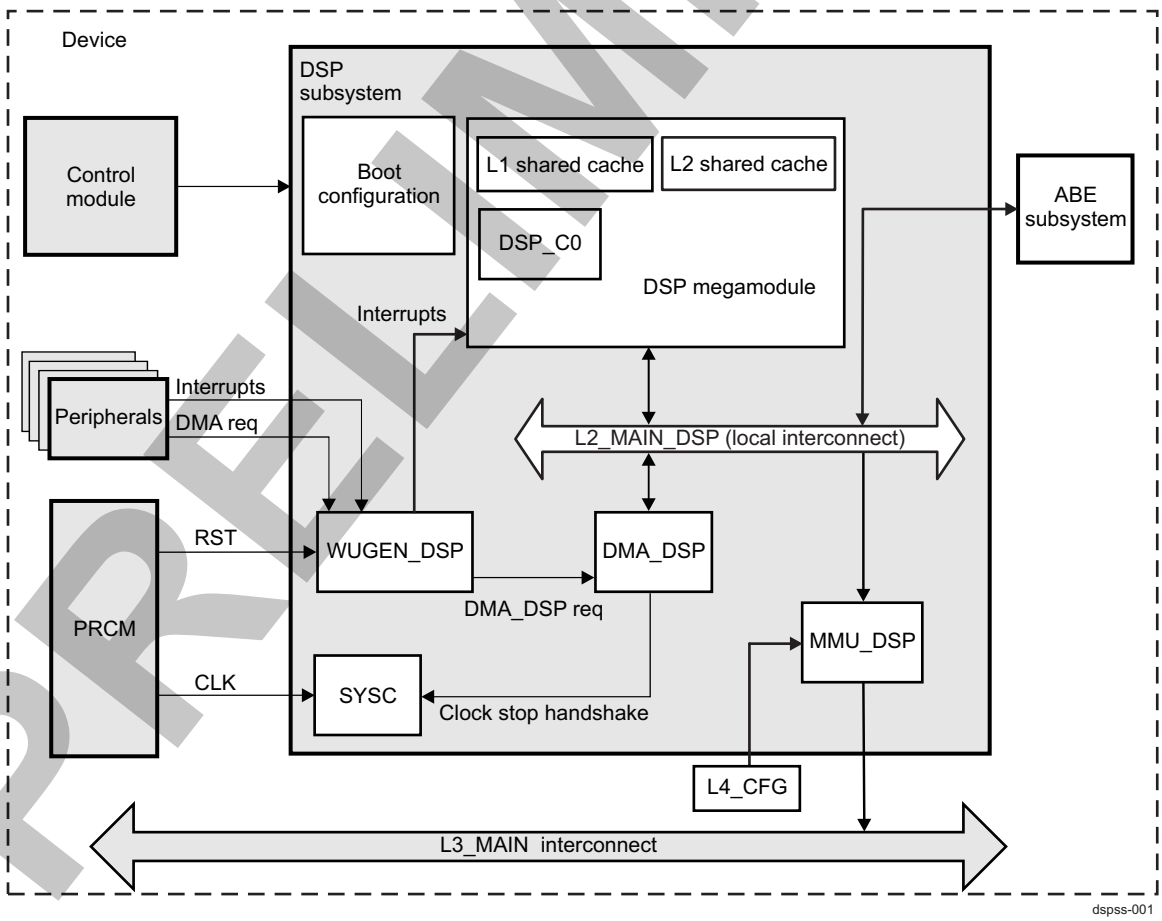
The internal architecture is an assembly of the following components:

- High-performance TI DSP (TMS320DMC64x™) derivative (DSP_C0) integrated in a megamodule, including local level 1 (L1) and level 2 (L2) cache and memory controllers for audio processing and general-purpose imaging and video processing
- L1 and L2 shared cache - (part of the DSP megamodule located - SCACHE_MMU_DSP block)
- Subsystem counter timer module (SCTM)
- Dedicated enhanced data memory access engine - DMA_DSP, to download/upload data from/to memories and peripherals external to the subchip
- Dedicated memory management unit (MMU_DSP) for accessing level 3 (L3_MAIN) interconnect address space
- Local interconnect network
- Dedicated SYSC and wake-up generator (WUGEN_DSP) modules responsible for power management, clock generation, and connection to the power, reset, and clock management (PRCM) module

For information about C64x™ to C64x+™ core migration, see the documents listed in Section 5.3.2.7, *Other DSP Reference Documents*.

Figure 5-1 is the DSP subsystem top-level architecture.

Figure 5-1. DSP Subsystem Highlight



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5.1.1 DSP Subsystem Key Features

The main features of the DSP subsystem are:

- 32-bit fixed-point media processor
- VLIW architecture based on programmable enhanced version of the C64x DSP core
- Coprocessor connection through the coprocessor hardware Interface
- Four instructions per cycle, four execution units:
  - Optimized instruction set for video and image processing
  - Four 8 x 8 or 16 x 16 multiply accumulate (MAC) per cycle
  - Four slave synchronous die (SAD) per cycle
  - Eight interpolations (a + b + 1) >> 1 per cycle
  - Two (32-bit x 32-bit -> 64-bit) multiply operations per cycle
- Low-power processor and megamodule:
  - Dynamically mixed 32-bit and 16-bit instruction sets
  - Separate power domain
  - Supported multiple power-down states
- 2-level memory subsystem hierarchy:
  - L1 (program and data):
    - 32-KiB 4-way set associative cache-32-byte cache line
  - L2 (program and data):
    - 128-KiB 8-way set associative cache-32-byte cache line
- Private direct memory access controller - DMA_DSP:
  - 128 logical channels
  - 1-dimensional/2-dimensional (1D/2D) addressing
  - Chaining capability
  - Fully pipelined, two 64-bit read ports, two 64-bit write ports
  - Single-access 32- or 64-byte incrementing bursts
- L1 interrupt controller (INTC_DSP)
- Local DSP digital phase-locked loop (DPLL_IVA) supplying DSP subsystem clocking
- 32-entry MMU (MMU_DSP) for seamless integration in high-level operating system (OS) environment
- DSP subsystem interfaces:
  - 64-bit L3_MAIN port shared for external memory accesses:
    - Multithreaded link shared by the DSP core - DSP_C0 and DMA_DSPs
    - Interface with the L3_MAIN interconnect that can be synchronous or asynchronous for clock decoupling between DSP and L3_MAIN
    - Incrementing burst support
    - Critical line first, to reduce line-fetch latency to the processor
  - Host port interface (HPI) for MMU programming and access to DSP internal memories. Can be synchronous or asynchronous.
  - System interfaces: Clocking, power management
- C-friendly environment (state-of-the-art C-compiler for VLIW architecture)
- TI low-overhead DSP-BIOS™ OS
- Backward compatibility (not binary compatible) with existing C64x video coders.decoders (codecs) and high level of programmability and flexibility

Known restrictions on the C64x+ DSP core:

- 4-issue VLIW central processing unit (CPU) instead of 8-issue
- SPLOOP not supported

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- L1 and L2 flat static random access memory (SRAM) not supported
- No EFI port

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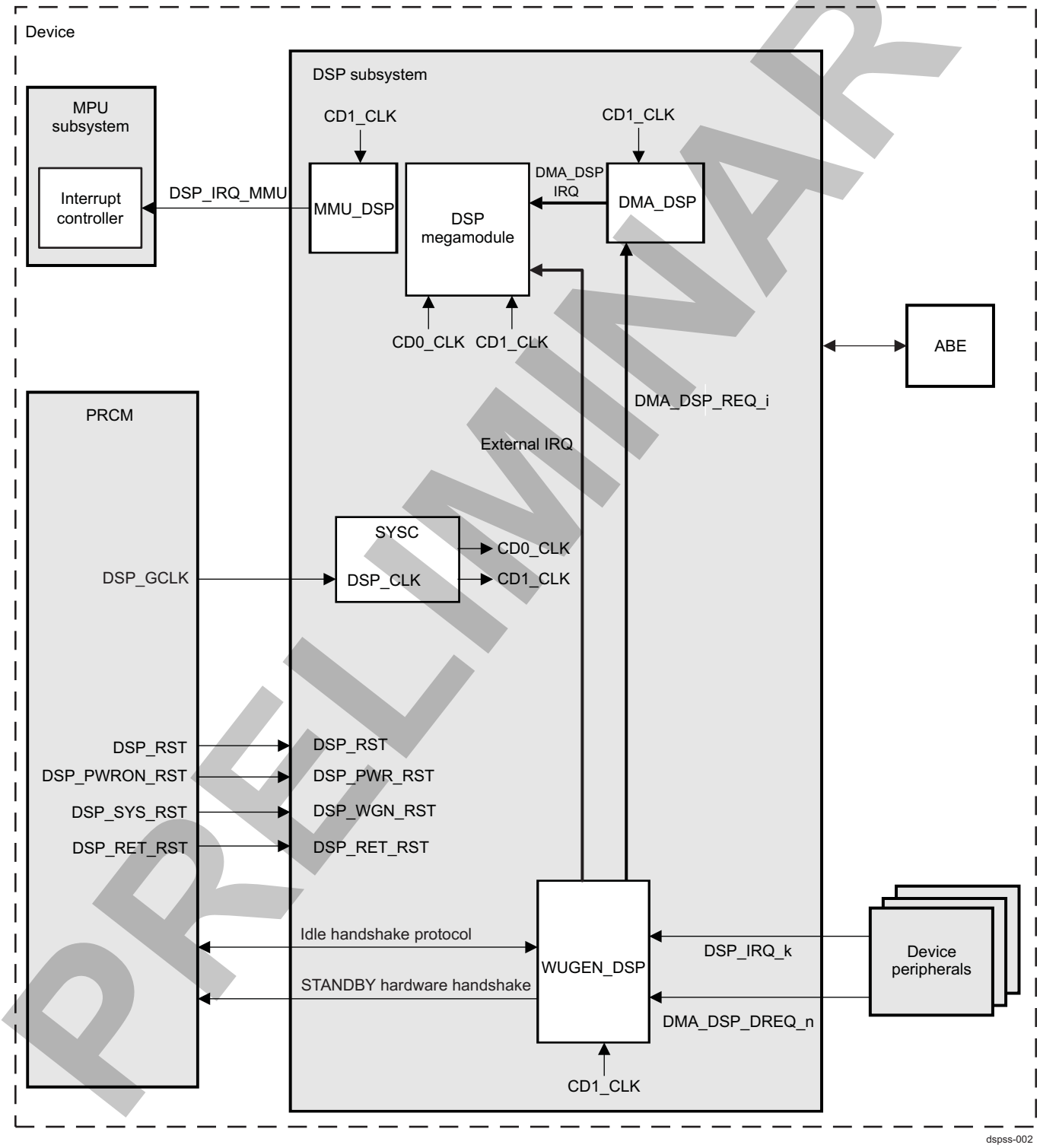
5.2 DSP Subsystem Integration

This section describes the integration of the module in the device, including information about clocks, resets, and hardware requests.

Figure 5-2 shows the integration of the DSP subsystem.

Figure 5-2. DSP Subsystem Integration



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NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 5-1 through Table 5-3 summarize the integration of the module in the device.

Table 5-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
DSP	PD_DSP	L3_MAIN

Table 5-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DSP	DSP_CLK	DSP_GCLK	PRCM module	For information about PRCM clock gating and management, see Section 3.7.2, *PD_DSP Description* in Chapter 3, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DSP	DSP_PWR_RST	DSP_PWRON_RST	PRCM module	For information about PRCM reset sources and distribution, see Section 3.7.2, *PD_DSP Description* in Chapter 3, *Power, Reset, and Clock Management*.
	DSP_RET_RST	DSP_RET_RST	PRCM module	
	DSP_WGN_RST	DSP_SYS_RST	PRCM module	
	DSP_RST	DSP_RST	PRCM module	

Hardware requests include interrupt requests and DMA requests. The INTC_DSP receives interrupts from the DSP subsystem (internal) and from other modules (D_IRQ_k interrupt signals). For more information about interrupt requests, see Table 5-6.

Table 5-3 lists the DMA requests.

Table 5-3. Hardware Requests – DMA Requests

Module Instance	Source Signal Name	Destination Signal Name	Destination	Description
DSP	Reserved	DMA_DSP_DREQ_0-1	DMA_DSP	Reserved
	MCBSP1_DREQ_TX	DMA_DSP_DREQ_2	DMA_DSP	MCBSP1 transmit request [0]
	MCBSP1_DREQ_RX	DMA_DSP_DREQ_3	DMA_DSP	MCBSP1 receive request [0]
	MCBSP2_DREQ_TX	DMA_DSP_DREQ_4	DMA_DSP	MCBSP2 transmit request [0]
	MCBSP2_DREQ_RX	DMA_DSP_DREQ_5	DMA_DSP	MCBSP2 receive request [0]
	MCBSP3_DREQ_TX	DMA_DSP_DREQ_6	DMA_DSP	MCBSP3 transmit request [0]
	MCBSP3_DREQ_RX	DMA_DSP_DREQ_7	DMA_DSP	MCBSP3 receive request [0]
	Reserved	DMA_DSP_DREQ_8-9	DMA_DSP	Reserved
	UART3_DREQ_TX	DMA_DSP_DREQ_10	DMA_DSP	UART3 transmit request [0]
	UART3_DREQ_RX	DMA_DSP_DREQ_11	DMA_DSP	UART3 receive request [0]
	Reserved	DMA_DSP_DREQ_12-27	DMA_DSP	Reserved
	ABE_DREQ_FIFO0	DMA_DSP_DREQ_28	DMA_DSP	Audio back-end (ABE) - request FIFO 0
	ABE_DREQ_FIFO1	DMA_DSP_DREQ_29	DMA_DSP	ABE - request FIFO 1

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Table 5-3. Hardware Requests – DMA Requests (continued)

Module Instance	Source Signal Name	Destination Signal Name	Destination	Description
	ABE_DREQ_FIFO2	DMA_DSP_DREQ_30	DMA_DSP	ABE - request FIFO 2
	ABE_DREQ_FIFO3	DMA_DSP_DREQ_31	DMA_DSP	ABE - request FIFO 3
	ABE_DREQ_FIFO4	DMA_DSP_DREQ_32	DMA_DSP	ABE - request FIFO 4
	ABE_DREQ_FIFO5	DMA_DSP_DREQ_33	DMA_DSP	ABE - request FIFO 5
	ABE_DREQ_FIFO6	DMA_DSP_DREQ_34	DMA_DSP	ABE - request FIFO 6
	ABE_DREQ_FIFO7	DMA_DSP_DREQ_35	DMA_DSP	ABE - request FIFO 7
	MCASP_DREQ_AXEVT	DMA_DSP_DREQ_36	DMA_DSP	MCASP transmit request
	Reserved	DMA_DSP_DREQ_37-41	DMA_DSP	Reserved
	MCPDM_DREQ_UP_LINK	DMA_DSP_DREQ_42	DMA_DSP	MCPDM Uplink DMA request
	MCPDM_DREQ_DN_LINK	DMA_DSP_DREQ_43	DMA_DSP	MCPDM Downlink DMA request
	DMIC_DREQ	DMA_DSP_DREQ_44	DMA_DSP	DMIC DMA Request
	Reserved	DMA_DSP_DREQ_45-63	DMA_DSP	Reserved

NOTE:

- For a description of the interrupt source, see Section 5.3.7, *Interrupt Requests*.
- For a description of the DMA source, see Section 5.3.8, *DMA Requests*.

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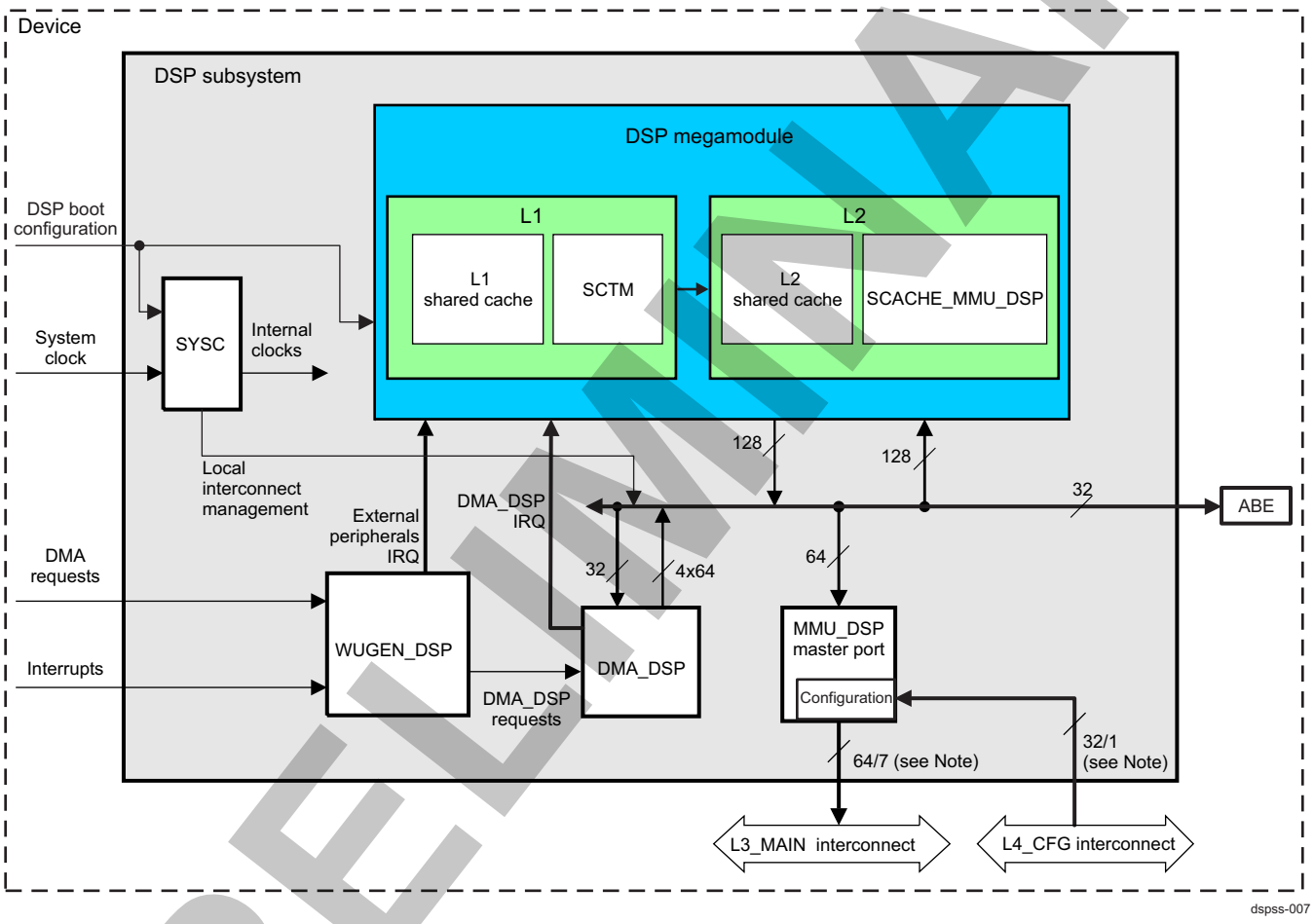
5.3 DSP Subsystem Functional Description

5.3.1 Block Diagram

The DSP subsystem is composed of a DSP megamodule coupled with several submodules that enable its integration in the device architecture. The DSP subsystem provides one slave port connected to the L4_CFG interconnect (used to configure MMU_DSP from the device MPU) and one master port which is connected to the L3_MAIN interconnect. There is also a single master port for direct access to a port of the ABE subsystem.

Figure 5-3 is a block diagram of the DSP subsystem.

Figure 5-3. DSP Subsystem Block Diagram



NOTE: The first number indicates bus width in bits, and the next indicates the number of L3_MAIN connected targets/ initiators for DSPSS master / slave ports. For more information, see subchapter Section 14.2, *L3 Interconnect* in Chapter 14, *Interconnect*.

5.3.2 DSP Megamodule

The C64x+ DSP megamodule is a class of derivative sections of the generalized embedded megamodule. The DSP megamodule is hardware-configurable and comprises a version of the C64x+, an L1 program memory controller (PMC), an L1 data memory controller (DMC), and L1/L2 shared caches.

Figure 5-4 is a block diagram of the DSP megamodule.

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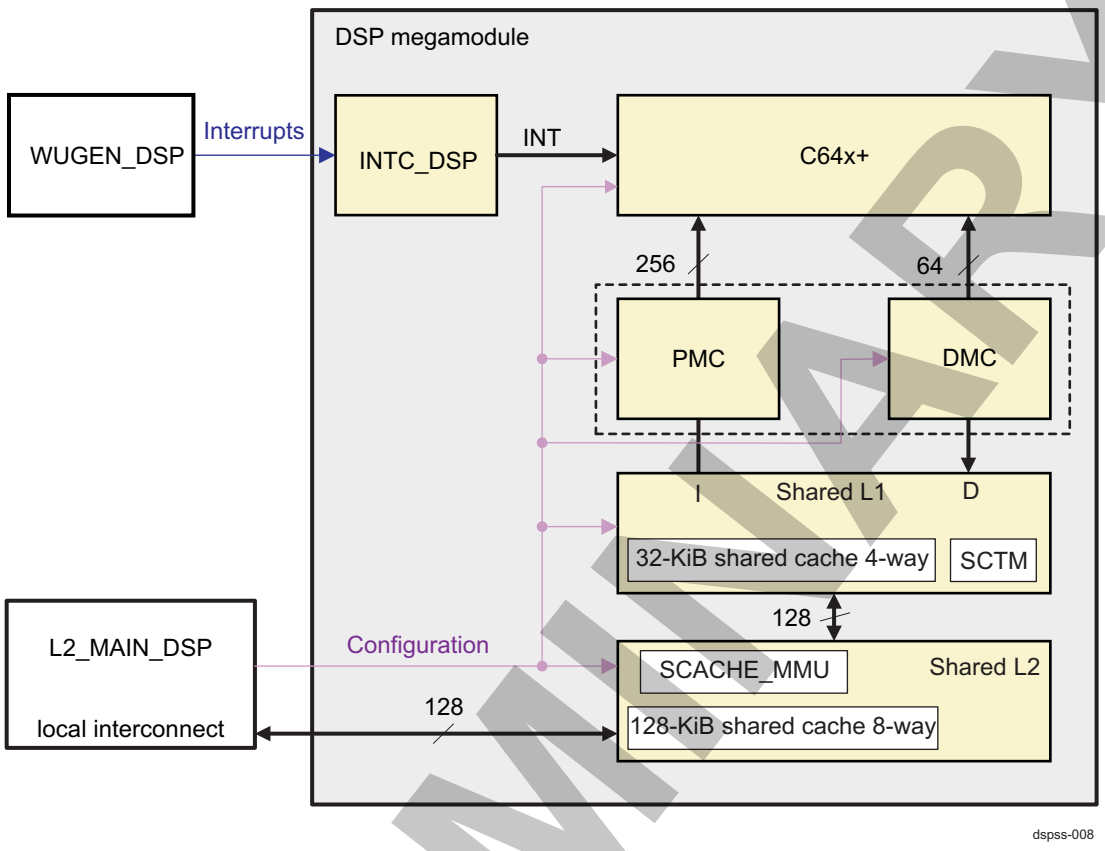
Figure 5-4. DSP Megamodule Block Diagram



5.3.2.1 DSP Overview

The C64x+ is an extension of the first C64x DSP section.

The DSP core features:

- 32-bit fixed-point media processor
- VLIW architecture
- Four instructions per cycle, four execution units
  - Optimized instruction set for video and image processing
  - Four 8 x 8 or 16 x 16 MACs per cycle
  - Four SADs per cycle
  - Eight interpolations (a + b + 1) >> 1 per cycle
  - Two (32-bit x 32-bit > 64-bit) multiply operations per cycle

In addition to the existing C64x features, the C64x+ includes the following:

- Compact instructions
- Extended function support
- Exception handling
- Privilege mode support
- HLOS time-stamp counter register

Known restrictions on the C64x+ DSP core are:

- 4-issue VLIW CPU instead of 8-issue
- SPLOOP not supported

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- L1 and L2 flat SRAM not supported
- No EFI port

For information about the C64x+ DSP, see the C64x+ reference manual listed in Section 5.3.2.7, *Other DSP Reference Documents*.

5.3.2.2 PMC Overview

The PMC is the DSP megamodule component that delivers program fetch packets when they are requested by the DSP_C0.

The PMC supports the following features:

- One 256-bit fetch packet per cycle (sustainable)
- DMA transfer from/to L1/L2 caches
- Fair priority-based arbitration between DSP, DMA_DSP, and cache controller for access to the SRAM
- Block and global program-initiated cache coherence support (invalidate)
- Freeze mode

For more information, see Section 5.4.5, *Memory Management*.

5.3.2.3 DMC Overview

The DMC is the DSP megamodule component that reads or writes data from/to local memories, as requested by the DSP.

The DMC supports the following features:

- One 64-bit memory access per cycle (sustainable)
- A memory access pair can be any combination of read and write, with no incurred penalty.
- DMA transfer from/to L1/L2 caches
- Fair priority-based arbitration between the DSP, DMA_DSP, and cache controller for access to the SRAM
- Hardware coherence maintenance with L2 (snooping)
- Block and global program-initiated cache coherence support (write-back, invalidate, and write-back-invalidate)
- Freeze and bypass mode

5.3.2.4 Shared L1/L2 Cache Overview

The following features are supported by the shared cache design:

- 32-KiB L1 shared cache implemented with high-performance bit cell to run at full speed
- 128-KiB L2 shared cache implemented with high-density bit cell to optimize area at half speed
- L1 cache is 32B line size, 4-way set-associative and organized as 16-bank.
- L2 cache is 32B line size and 8-way set associative.
- L1 cache supports snooping.
- L2 cache slave port to support snooping from DMA_DSP accesses
- Fully pipelined/supports critical-word-first
- Write-combining
- Fill and eviction buffers, and hit in fill buffer
- Dynamic sizing, I/D allocation
- Prefetch 4 lines/preload N lines
- Background preload/clean

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5.3.2.5 Attribute MMU Overview

The attribute MMU for the shared cache - SCACHE_MMU_DSP, provides the multi-access cache with a region-based address translation, read/write control, access type control, endiannism, and multilevel cache maintenance.

The SCACHE_MMU_DSP is directly connected to the shared cache, and there is a dedicated interface for pipeline write policy management. L1 policies are queried at the allocation control of the cache, and L2 policies are propagated to the master interface.

For flexibility, the SCACHE_MMU_DSP can be dedicated to an L1 or an L2 cache configuration, with or without address translation, or as an L1/L2 cache combination.

The SCACHE_MMU_DSP supports different page sizes: large, medium, and small. The number of large pages, number of medium pages, etc., is defined at design time. The maximum number of large pages is eight. This address space includes addresses for all eight regions. However, if the DSP subsystem defines only five large pages, only the first five addresses are valid.

The page sizes for the 17 entries are:

- Large pages (eight): The page size supported is 512 MiB.
- Medium pages (seven): The page sizes supported are 128 KiB and 1 MiB.
- Small pages (two): The page sizes supported are 4 KiB and 32 KiB.

The size of the page is configured by setting:

- SCACHE_MMU_LARGE_POLICY_i[1] SIZE
- SCACHE_MMU_MED_POLICY_j[1] SIZE
- SCACHE_MMU_SMALL_POLICY_k[1] SIZE

The logical source address is configured in:

- SCACHE_MMU_LARGE_ADDR_i[31:25] ADDRESS
- SCACHE_MMU_MED_ADDR_j[31:17] ADDRESS
- SCACHE_MMU_SMALL_ADDR_k[31:12] ADDRESS

The logical source translated address is configured in:

- SCACHE_MMU_LARGE_XLTE_i[31:25] ADDRESS
- SCACHE_MMU_MED_XLTE_j[31:17] ADDRESS
- SCACHE_MMU_SMALL_XLTE_k[31:12] ADDRESS

When the SIZE bit is set to 0, all the bits in the ADDRESS bit field of the corresponding logical source address and logical source translated address can be used.

When the SIZE bit is set to 1, the ADDRESS bit field of the corresponding logical source address and logical source translated address must be programmed only with addresses that can address the size of a second possible page.

5.3.2.6 DSP INTC

The DSP megamodule interrupt controller - INTC_DSP detects, potentially combines, and routes up to 128 system events (internal and external) to the DSP_C0 CPU interrupt lines. Table 5-6 lists the global interrupt mappings of the DSP subsystem (internal and external interrupts).

The DSP_C0 CPU has 12 maskable interrupts and one exception input. The INTC_DSP includes an interrupt selector, exception combiner, and event combiner. The interrupt selector allows the routing of any of the 128 system events (or a combination of them) to the 12 maskable interrupts of the DSP_C0 CPU, and software determines the priorities of those system events. To handle potential conflicts, the 12 CPU interrupts have fixed priorities. The exception combiner allows the combination of any of the 128 system events to the single exception input of the DSP_C0 CPU (see Figure 5-5).

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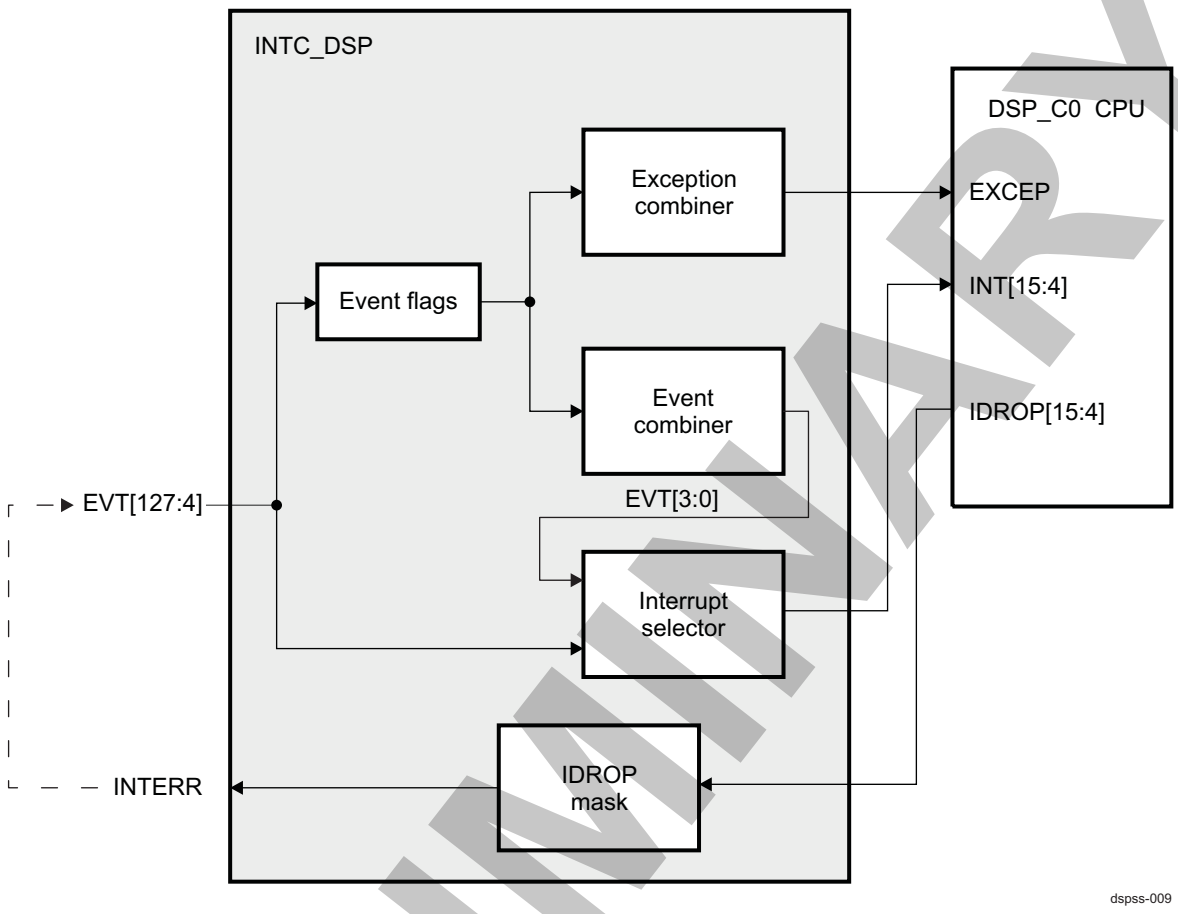
Figure 5-5. DSP Megamodule INTC Block Diagram



NOTE: Not all 128 event inputs of the INTC_DSP are connected to an internal or external event line. Table 5-6 lists the global interrupt mapping of the INTC_DSP. Some interrupts at the DSP boundary are reserved for future use or are not used by the DSP subsystem. For information about the DSP core interrupt controller - INTC_DSP, see the C64x+ DSP documents listed in Section 5.3.2.7, *Other DSP Reference Documents*.

5.3.2.6.1 Event Type

The INTC_DSP provides three types of interrupt sources to the DSP_C0 CPU:

- Single event
  - A single system event can be directly routed to a CPU interrupt input.
  - A dropped system event is supported through the CPU dropped interrupt reporting mechanism (if the CPU misses the interrupt input, the system event is missed).
- Combined event
  - Up to four event combiners
  - Each combiner allows up to 32 system events to be logically ORed into a single event that can be routed to the DSP_C0 CPU.
- Exception event: This event is considered a single event, but it is directly connected to the exception input of the DSP_C0 CPU.

5.3.2.6.2 Event Behavior

- Single event source: The interrupt selector routes 1 of 124 events to a DSP_C0 CPU interrupt, as

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programmed in the interrupt selector registers (SYS_INTC_INTMUXj, where j = 1 to 3). Logic in the CPU and INTC_DSP combine to detect instances in which an interrupt request is asserted before an earlier interrupt request is serviced. The INTC_DSP records the interrupt number of the first interrupt and keeps this information until directed to release the interrupt, either through reset or by application software. This record can be used as an additional system event to notify the application of an interrupt failure. Interrupts that qualify for dropped detection are defined through an IDROP mask that sets the SYS_INTC_INTDMASK register. The masked IDROP event output (EVT96; see Table 5-6) is available as a system event that can be selected as a DSP_C0 CPU interrupt or an exception event.

- Combined source: The event combiners create a combined event from the logical OR of 32 system-event flags qualified by a mask provided through programmable registers (SYS_INTC_EVTMASKi, where i = 0 to 3). The combination of the event flags creates an event that is asserted when any of the event flags included in its generation is active. Software must clear the event flags (SYS_INTC_EVTCLRi, where i = 0 to 3) to deassert a combined event.

  NOTE: The use of event flags makes it impossible for the CPU to detect the dropping of independent system events; therefore, dropped interrupt capability is not directly supported for combined events.

  The interrupt event combiners create four shared interrupt sources:

  – EVT0: Logical OR of SYS_INTC_EVTFLAGi[31:4] (where i = 0) masked by SYS_INTC_EVTMASKi[31:4] (i = 0)
  – EVT1: Logical OR of SYS_INTC_EVTFLAGi[63:32] (where i = 1) masked by SYS_INTC_EVTMASKi[63:32] (i = 1)
  – EVT2: Logical OR of SYS_INTC_EVTFLAGi[95:64] (where i = 2) masked by SYS_INTC_EVTMASKi[95:64] (i = 2)
  – EVT3: Logical OR of SYS_INTC_EVTFLAGi[127:96] (where i = 3) masked by SYS_INTC_EVTMASKi[127:96] (where i = 3)

  SYS_INTC_EVTFLAGi are the event flag registers and SYS_INTC_EVTMASKi are the event mask registers. These combined events are presented to the interrupt selection logic.

- Exception event source: As with the event combiner, the exception combiner allows multiple system events to be grouped as a single event input to the CPU, and the combiner provides mask registers to remove undesirable events. Because only one exception is input to the CPU, all mask registers work together to combine up to 128 events as a single EXCEP output. This lets the CPU service all available system exceptions.

  The shared exception source is created as follows:

  EXCEP: Logical OR of EF[127:4] masked by XM[127:4]

  Where EF[i × 32 + j] = EVTFLAGi[j] and XM[i × 32 + j] = EXPMASKi[j] (i = 0, 1, 2, 3 and j = 0 to 31).

  The logic is similar to that of the event combiners, except that only one combined event is routed to EXCEP.

5.3.2.6.3 Event Detection

The INTC_DSP contains a set of status and control registers to manage the status of system events received by the controller. These include set, flag, and clear registers that cover all 128 system events. Enabling of the events is managed in the CPU for direct mapped interrupts, in the event combiner for combined events, and in the exception combiner for system exceptions. Events to the INTC_DSP can be enabled or disabled only at the event source.

The event flag registers (SYS_INTC_EVTFLAGi, where i = 0 to 3) capture every system event received, regardless of its destination: event combiner, exception combiner, or interrupt selector. Events that are not masked by the event combiner or the exception combiner are captured in the SYS_INTC_EVTFLAGi register (where i = 0 to 3) corresponding to the event and are used to determine when the combined event is generated. Events that are masked by the event combiner or the exception combiner are captured in the SYS_INTC_EVTFLAGi register but do not affect when the DSP_C0 CPU interrupt is generated.

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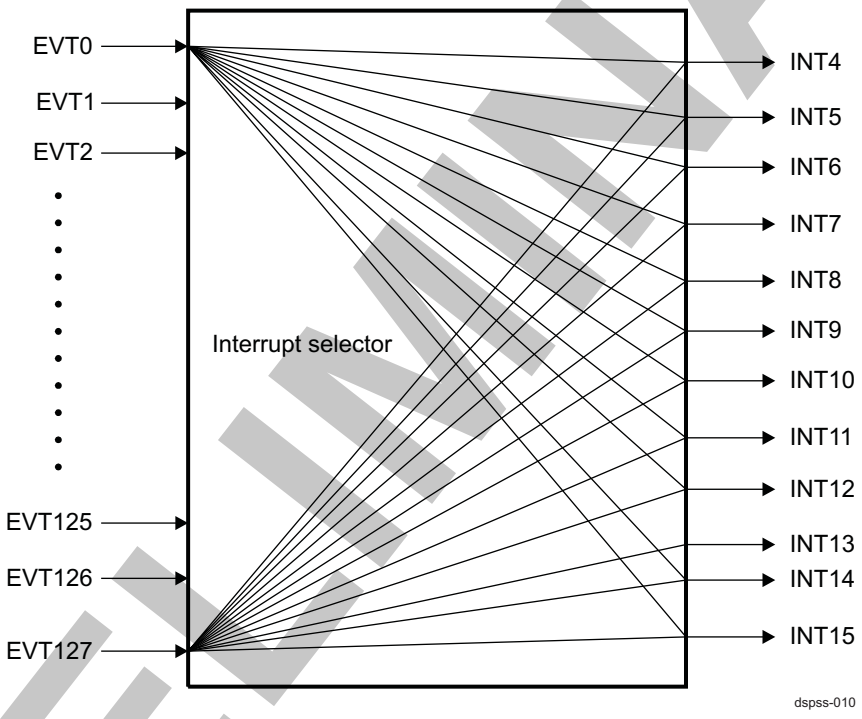
The event flags in the SYS_INTC_EVTFLAGi registers retain the value of 1 for any event received. These registers are read-only and must be cleared through the write-only SYS_INTC_EVTCLRi registers. The SYS_INTC_EVTSETi registers can be used to manually set bits in the SYS_INTC_EVTFLAGi registers, including those that are masked.

NOTE: Because external events are maintained by the peripheral until they are explicitly cleared by software, drop event detection does not work for external events (interrupts from peripherals external to the DSP subsystem).

5.3.2.6.4 Event Selection

The DSP_C0 CPU has 12 available maskable interrupts. The interrupt selector allows any of the 128 system events, either from the event inputs or from the event combiners, to be routed to any of the 12 CPU interrupt inputs (see Figure 5-6).

Figure 5-6. Interrupt Selector Block Diagram



Users can choose which of the 128 input events is mapped to each of the 12 CPU interrupts by writing the event number in the bit field corresponding to the CPU interrupt in the SYS_INTC_INTMUXj register. CPU priority is fixed. This event -> interrupt mapping allows software to define the priority of the event. For more information, see Section 5.4, *DSP Subsystem Basic Programming Guide*.

5.3.2.6.5 Event Combination

The event combiner allows multiple system events to be combined into a single event for routing to the interrupt selector. This allows the CPU to service all available system events, even though only 12 are available.

A set of event mask registers (SYS_INTC_EVTMASKi, where i = 0 to 3) is used to program the event combiner. These registers allow up to 32 events to be combined into a single event output that is used as one DSP_C0 CPU interrupt. The event mask bits in the SYS_INTC_EVTMASKi registers act as enablers for the received system events combined on the event outputs. There are four event outputs to the interrupt selector (EVT[3:0]).

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By default, every system event is unmasked and combined with its associated EVTx. To mask out an event source (for example, to disable an event from being combined), the corresponding mask bit (the SYS_INTC_EVTMASKi[y] EMy bit for EVTy) must be set to 1.

NOTE: Because the event masks for events 0 through 3 are combined events, and thus cannot contribute to the generation of a combined event, they are reserved.

For more information, see Section 5.4.4, *Interrupt Management*.

5.3.2.6.6 Interrupt Event Error

The INTC_DSP can generate a system event internally routed to system event input EVT96. This event is generated when a DSP_C0 CPU interrupt is received while the interrupt flag (IFR, internal DSP register) is already set in the CPU. This signals possible problems in the code, such as whether interrupts were disabled for an extended time or pipelined (noninterruptible) code sections were too long.

NOTE: The same strategy of register settings (events, event set, event clear, event mask) is used in the WUGEN_DSP (which is not an interrupt controller), which enables defining wake-up events so they can wake up the DSP subsystem. For more information, see Section 5.3.9, *Wake-Up Generator*.

For more information on interrupt management, see Section 5.4.4, *Interrupt Management*. For information on associated programming, see Section 5.4, *DSP Subsystem Programming Guide*.

5.3.2.7 Other DSP Reference Documents

For more information about the DSP megamodule architecture, instruction set, and DSP core INTC, and for a complete description of the DSP memory-mapped registers, see the following documents (www.ti.com):

- *TMS320C6000 DSP Peripherals Overview Reference Guide* (TI Literature number SPRU190) describes the peripherals available on the TMS320C6000 DSPs.
- *TMS320C64x™ Technical Overview* (TI Literature number SPRU395) introduces the TMS320C64x DSP and discusses the application areas enhanced by the TMS320C64x VelociT.
- *TMS320C64x+ DSP Megamodule Reference Guide* (TI Literature number SPRU871) describes the C64x+ megamodule peripherals.
- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (TI Literature number SPRU732)
- *TMS320C6000 Programmer's Guide* (TI Literature number SPRU198) describes ways to optimize C and assembly code for the TMS320C6000 DSPs, and includes application program examples.

5.3.3 DSP DMA

The DSP subsystem has an integrated DMA module - DMA_DSP to transfer instructions and data from/to external memory connected to the L3_MAIN interconnect to/from L1 and L2 local memories in the DSP megamodule. The DMA_DSP can also perform transfers between external memories and between DSP megamodule internal memories, with some performance loss caused by resource sharing between the read and write ports. For transfers between DSP megamodule internal memories, use the DMA_DSP with the locked feature.

The DMA_DSP is based on two primary components:

- DMA third-party channel controller (TPCC)
- DMA third-party transfer controller (TPTC)

There are two instances of the TPTC in the DSP subsystem.

Figure 5-7 shows how the DMA_DSP is integrated in the DSP subsystem:

- Code running on the DSP can configure the DMA_DSP; through the configuration port of the DSP megamodule and the local level2 interconnect - L2_MAIN_DSP, the code can program DMA transfers and trigger them by software by writing to the TPCC configuration registers.

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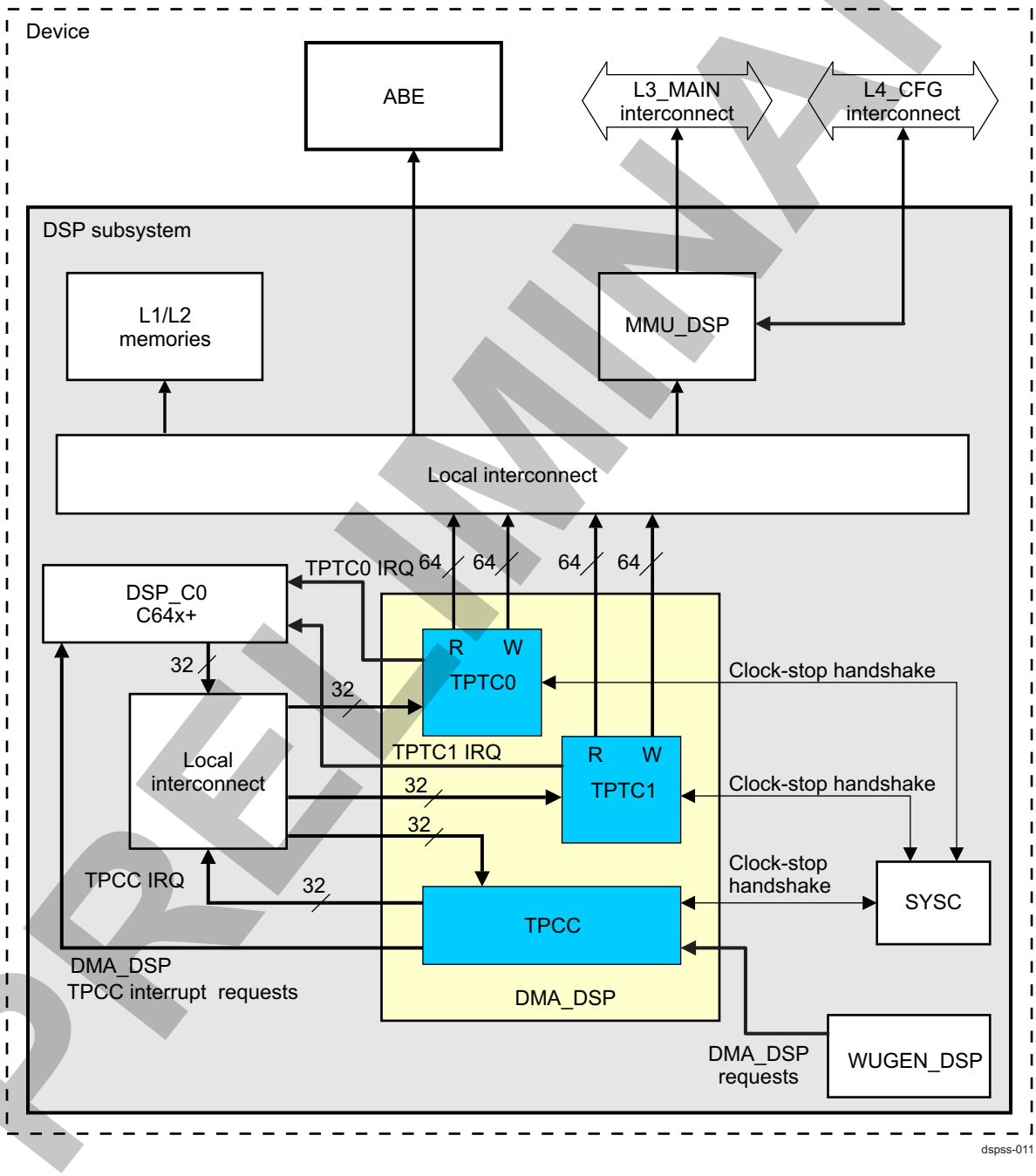
- Preprogrammed DMA transfers can be triggered by external events, referred to in this chapter as DMA requests.
- The TPCC schedules DMA transfers to the TPTC DMA engines (TPTC0 and TPTC1) through dedicated local interconnect 32-bit configuration ports.
- Each TPTC issues concurrent traffic on the local interconnect through dedicated read and write 64-bit ports.
- Interrupts generated by the DMA_DSP are routed to the INTC_DSP.
- Power-management handshakes are exchanged between DMA_DSP components and the SYSC.

Figure 5-7. DSP DMA Overview



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5.3.3.1 Third-Party Channel Controller

The TPCC is the DMA_DSP transfer scheduler responsible for scheduling, arbitrating, and issuing user-programmed transfers to the two TPTCs.

5.3.3.1.1 TPCC Features

The TPCC features are:

- Parameter RAM (PaRAM) entries, which hold up to 128 transfer contexts, with the following capabilities:
  - Ping-pong and circular buffering
  - Channel chaining
  - Auto-reloading

Each PaRAM entry can be used as a DMA entry (up to 64), QDMA entry (up to 8), or link entry (remaining):

- Up to 64 DMA logical channels:
  - 64 channels can be triggered explicitly by the DSP_C0 CPU (DMA entry).
  - 64 channels can be triggered by external events (see Table 5-3).
  - All channels can be triggered by completion of a previous transfer in a user-programmed chain of transfers (linked entry).
- 12 interrupt lines connected to the DSP_C0 CPU
- Boundaries for synchronization with the CPU are programmable.
- Two queues holding events waiting for submission to the TPTC
- Each transfer can be programmed to a priority level (three possible levels).

Figure 5-8 is a block diagram of the TPCC.

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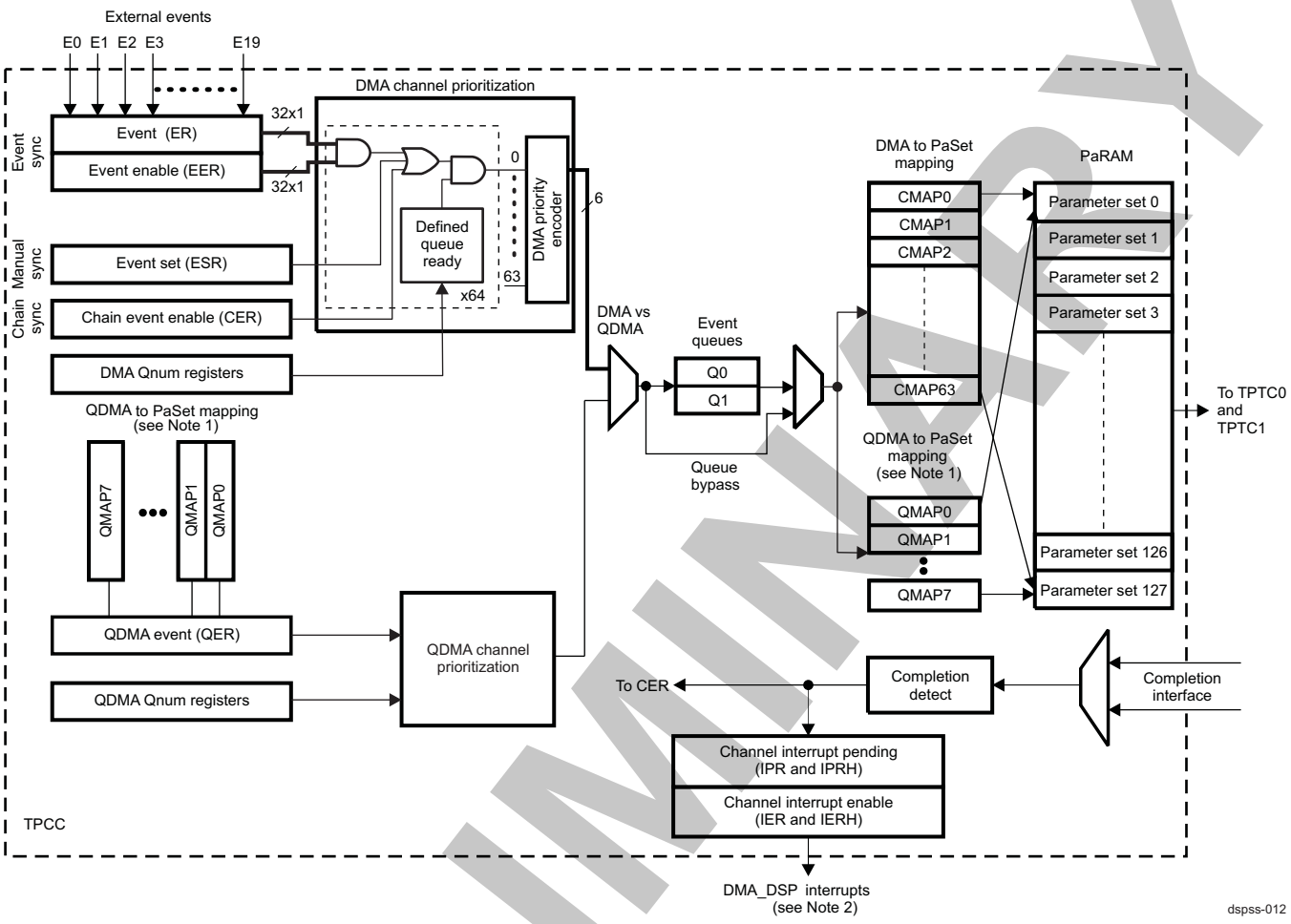
Figure 5-8. TPCC Block Diagram



(1) Although it is depicted twice in Figure 5-8, there is only one physical register set for the QDMA to PaRAM set mapping block.

(2) For more information, see Table 5-6.

A channel is a specific event that can cause a transfer to be submitted to the TPTCs as a transfer request. The TPCC supports up to 64 DMA channels and up to 8 QDMA channels. These channels are identical, except for how they are triggered:

- DMA channels can be triggered by external events (such as MCBSP TX Evt and MCBSP RX Evt) by the software writing 1 to a given bit location or channel, by the event set register, or through chaining.
- QDMA channels are triggered automatically (auto-triggered) by the CPU. QDMAs allow a minimum number of linear writes to be issued to the TPCC to force a series of transfers to occur.

The TPCC arbitrates among pending DMA and QDMA events with a fixed 64:1 and 4:1 priority encoder for these events, respectively (a low channel number corresponds to a high priority). DMA events are always higher priority than QDMA events. The higher-priority event is placed in the event queue to await submission to the transfer controller, which occurs at the earliest opportunity. Each event queue is serviced in FIFO order, with a maximum of 16 queued events per event queue. If more than one TPTC is ready to be programmed with a transmission request (TR), the event queues are serviced with fixed priority: Q0 is higher than Q1. When an event is ready to be queued and the event queue and the TC channel are empty, the event bypasses the event queue and goes directly to the PaRAM processing logic for submission to the appropriate TC. If the TR bus/PaRAM processing is busy, the bypass path is not used. The bypass is not used to dequeue for a higher-priority event.

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Events are extracted from the event queue when the TPTC is available for a new TR to be programmed into the TPTC (signaled with the empty signal, indicating an empty program register set). As an event is extracted from the event queue, the associated PaRAM entry is processed and submitted to the TPTC as a TR. The TPCC updates the appropriate counts and addresses in the PaRAM entry in anticipation of the next trigger event for that PaRAM entry. The PaRAM entry consists of eight words of DMA context, including source address, destination address, count, indexes, etc.

5.3.3.1.2 DMA Versus QDMA

The only difference between a QDMA and a DMA transfer is the means of generating and recognizing TR synchronization. From the user point of view, DMA and QDMA transfer types can be combined to perform various types of transfers.

DMA channel TR synchronization can be generated from one of three sources:

- Event-triggered: The event register (TPCC_ER) channel *n* bit is set as the result of an external event. An external event is latched in the event register. If the corresponding event is enabled through the event enable register (TPCC_EER), this is recognized as a TR synchronization.
- Manually triggered: The event set register channel *n* bit is set manually to the event set registers (TPCC_ESR and TPCC_ESRH) for channel *n* (the TPCC_ESR[n] En bit or TPCC_ESRH[n] En bit). Manually set events do not have to be enabled to be recognized as a TR synchronization.
- Chain-triggered: The chain event register channel *n* (the TPCC_CER and TPCC_CERH registers) bit is set when a chaining completion code is detected on the completion interface for channel *n*. Chain events do not have to be enabled. If a chain trigger is detected, this is always recognized as a TR synchronization.

QDMA TR synchronization occurs in one of two ways:

- Auto-triggered: The QDMA event register channel *n* (the TPCC_QER and TPCC_QER_RN_k[n] En) bit is set when a CPU write address matches the address defined by the QDMA mapping register for channel *n* (TPCC_QCHMAPN_j) and the QDMA channel is enabled (the TPCC_QEER[n] En bit field).
- Link-triggered: The TPCC_QER[n] En bit is set when a link update is performed on a PaRAM address that matches the TPCC_QCHMAPN_j setting, and the TPCC_QEER[n] En bit is set.

There is a subtle difference between each trigger type and the associated enablers. Event assertion always results in the TPCC_ER[n] En bit being set, regardless of the state of the enable (TPCC_EER.En). It is recognized as a TR synchronization only if enabled. Chain triggering always sets the TPCC_CER[n] En bit and is always treated as a TR synchronization. Manual triggering always sets the TPCC_ESR[*n*] En bit and is always treated as a TR synchronization. Auto-triggering (QDMA) sets only the event register TPCC_QER[n] En bit only if the corresponding event is enabled (TPCC_QEER[n] En); when the TPCC_QER[n] En bit is set, it is always treated as a TR synchronization.

For more information, see Section 5.4, *DSP Subsystem Programming Guide*.

5.3.3.1.3 DMA/QDMA Channel Mapping and PaRAM Entry

The DMA and QDMA channel mapping registers (TPCC_DCHMAPN_i and TPCC_QCHMAPN_j) allow each DMA and QDMA channel to be mapped to arbitrary locations in the PaRAM memory map. The entry is designated with a 9-bit PAENTRY (the TPCC_DCHMAPN_i[13:5] PAENTRY and TPCC_QCHMAPN_j[13:5] PAENTRY bit fields) PaRAM entry number that defines the entry number in a 128-entry maximum PaRAM (see Figure 5-9). The TPCC_QCHMAPN_j[4:2] TRWORD bit field points to the trigger word of the PaRAM entry defined by PAENTRY. A write to the trigger word results in a QDMA event being recognized.

Figure 5-9 shows DMA/QDMA channel mapping and PaRAM entry.

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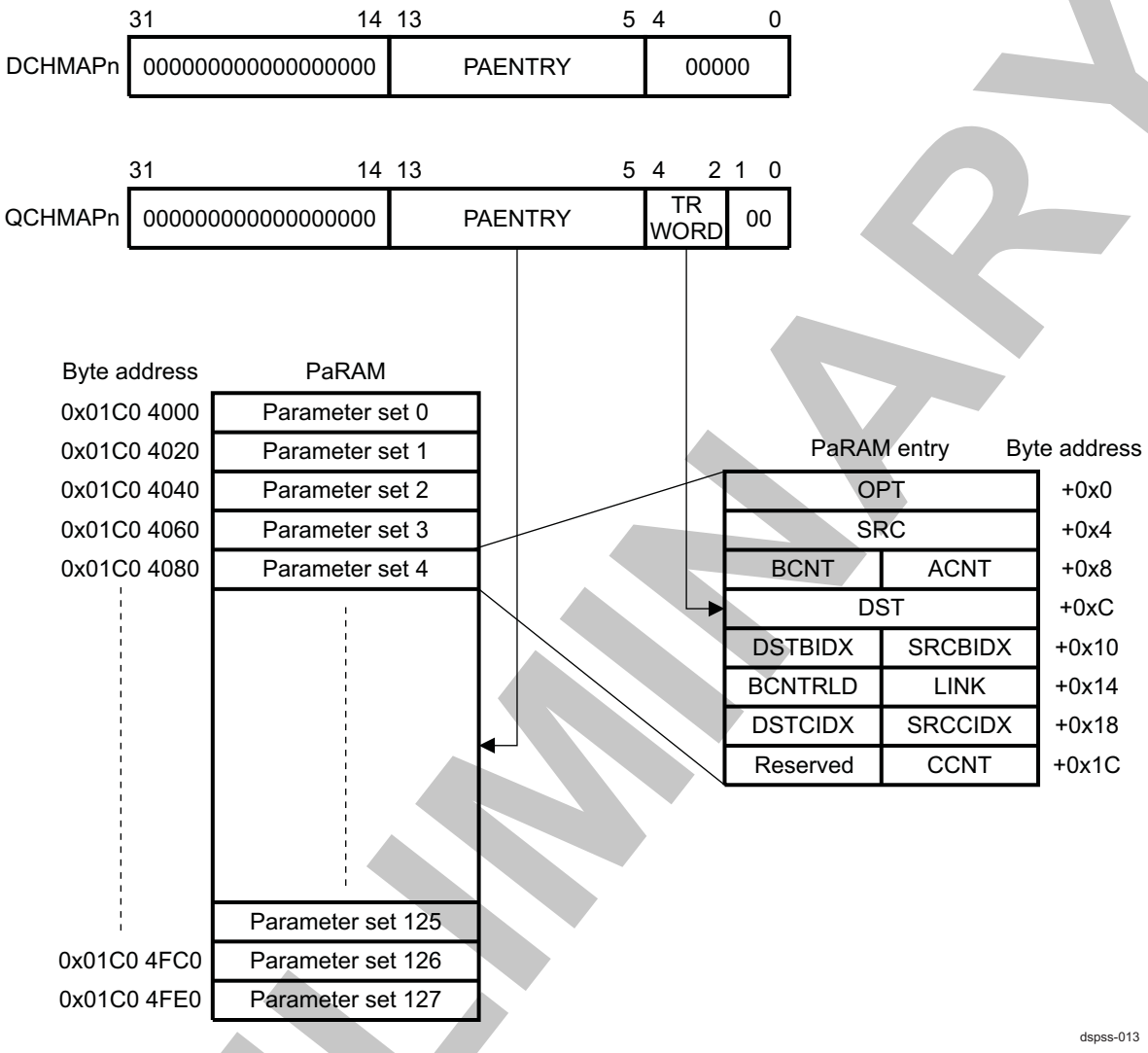
Figure 5-9. DMA/QDMA Channel Mapping and PaRAM Entry



NOTE: Each parameter entry of PaRAM is organized as eight 32-bit words or 32 bytes, as shown in Figure 5-9.

The location of fields in each entry, and the bit positions in the options field, must match the TR packet format as closely as possible to the requirements of the TPTC0 and TPTC1 programming. Each PaRAM entry consists of 16- and 32-bit parameters that correspond to the transfer geometry. For more information about the parameters, see Section 5.3.3.1.2, *DMA Versus QDMA.*

5.3.3.1.4 Types of TPCC Transfers

The TPCC streamlines transfers into an orthogonal transfer structure that is always defined by three dimensions. Of the three dimensions, only two synchronization types are supported: 1D synchronized transfers and 2D synchronized transfers; three-dimensional (3D) synchronized transfers can be logically achieved by chaining.

The following terms are used:

- 1D transfer or array: ACNT contiguous byte transfer. For information about the 1D transfer programming model, see Section 5.3.3.1.5, *Transfer Synchronization*.
- 2D transfer or frame: BCNT arrays of ACNT byte transfer. Each array transfer in 2D transfer is

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separated from other transfers by an index programmed through the TPCC_BIDX_m register.

- 3D or block: CCNT frames of BCNT arrays of ACNT bytes. Each transfer in 3D is separated from the previous transfer by an index programmed by the TPCC_CIDX register. The reference point for the index depends on the synchronization type.

5.3.3.1.5 Transfer Synchronization

In a 1D synchronized transfer, each TPCC TR synchronization triggers the transfer of the first dimension of ACNT bytes, or one array of ACNT bytes. In other words, each TR packet consists of transfer information for only one array. Arrays can be separated by SBIDX and DBIDX (see Figure 5-9) where the start address of array N equals the start address of array 1 plus SRC or DST BIDX. Frames can be separated by SCIDX and DCIDX. For 1D synchronized transfers, after the frame is exhausted, the address is updated by adding (S|D)CIDX to the beginning address of the last array in the frame.

Contrast this to the (S|D)CIDX update in 2D synchronized transfers, which are referenced from the beginning address of the first array in the previous frame. For information about parameter updates, see Section 5.3.14, *Error Reporting*.

In a 2D synchronized transfer, each TR synchronization triggers the transfer of two dimensions or one frame. In other words, each TR packet conveys information for one entire frame of BCNT arrays of ACNT bytes. Arrays can be separated by SBIDX and DBIDX (see Figure 5-11). Frames can be separated by SCIDX and DCIDX. For 2D synchronized transfers, after a TR for the frame is submitted, the address is updated by adding (S|D)CIDX to the beginning address of the beginning array in the frame. Contrast this to the (S|D)BIDX update in 1D synchronized transfers. For information about parameter updates, see Section 5.3.14, *Error Reporting*.

5.3.3.1.6 DMA Channel Prioritization

If multiple trigger sources (event trigger/chain trigger/manual trigger) for a single channel are active at the same time, the TPCC services events in the following order:

1. Event trigger (through the event register [ER])
2. Chain trigger (through the chain event register [CER])
3. Manual trigger (through the event set register [ESR])

5.3.3.1.7 Transfer Completion

Transfer completion can be used for two different mechanisms in the TPCC:

- Generating chained events
- Generating interrupts to an external processor

The underlying mechanism for both features is the same. The user programs the PaRAM options field with a specific transfer completion code (the TPCC_OPT_m[17:12] TCC bit field) and indicates whether that completion code is to be used to generate a chained event and/or an interrupt when a transfer completes. The user can selectively program whether completion signaling is enabled for the final TR of a PaRAM set, for all except the final TR of a PaRAM set, or for all TRs of a PaRAM set. The specific TCC value (6-bit binary value) programmed by the user dictates which bit of the 64-bit CER and/or interrupt pending register (IPR) is used.

There is no direct correlation between the TCC value used for a specific PaRAM entry and the channel number for that entry. Software controls the allocation of TCC values. There is always a 1:1 relationship between the value of the TCC and the IPR bit and/or the CER bit set when that transfer completes. For example, completion of the PaRAM entry for channel 0 can chain-trigger the PaRAM entry for channel 1.

5.3.3.2 Third-Party Transfer Controller

The TPTC is the DMA_DSP transfer engine that generates transfers as programmed in dedicated working registers, using two dedicated master ports: a read-only port and a write-only port.

NOTE: The port data bus width of the instances of the TPTC is fixed at 64 bits.

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5.3.3.2.1 TPTC Features

The TPTC features:

- Pipelined transfers (multiple in-flight transfers)
- Background programming
- 2D or 1D transfer
- Increment addressing modes
- Clock-stop handshaking with the SYSC
- Programmable tracking of transfer completion
- 2D qualifications of transfers to allow 2D bandwidth optimization

Two instances of the TPTC generate concurrent traffic on the DSP local interconnect. Each TC controller consists of the following components:

- DMA_DSP program register set: Stores the context for the DMA transfer that is loaded into the active register set when the current active register set completes. The CPU or TPCC programs the program register set, not the active register set. For a typical stand-alone operation, the CPU programs the program register while the TC services the active register set. The program register set includes ownership control that synchronizes the CPU software and the DMA_DSP.
- Source DMA_DSP active register set: Stores the context (src/dst/cnt/, etc.) for the DMA transfer request in progress in the read controller. The active register set is split into independent source and distant register, because the source local interconnect controller and the distant local interconnect controller operate independently of one another.
- Distant DMA_DSP register set: Stores the context (src/dst/cnt/, etc.) for the DMA transfer request in progress or pending in the write controller. The pending register sets must allow the source controller to begin processing a new TR while the distant register set processes the previous TR.
- Channel FIFO: Temporary holding buffer for in-flight data. The read return data of the source peripheral is stored in the data FIFO, and then is written to the destination peripheral by the write command/data bus.
- Read controller/local interconnect read interface: The local interconnect read interface issues optimally sized read commands to the source peripheral, based on a burst size of 64 bytes and available landing space in the channel FIFO.
- Write controller/local interconnect write interface: The local interconnect write interface issues optimally sized write commands to the destination peripheral, based on a burst size of 64 bytes and available data in the channel FIFO.
- Completion interface: Sends completion information to the TPCC for posting interrupts in the TPCC.
- Configuration port: Slave interface that provides read/write access to program registers and read access to all memory-mapped TC registers. For information about TPTC registers, see Section 5.3.1, *DSP Subsystem Register Manual*.

Table 5-4 lists the hardware settings.

Figure 5-10 shows the internal structure of the TPTC and its connection to the TPCC.

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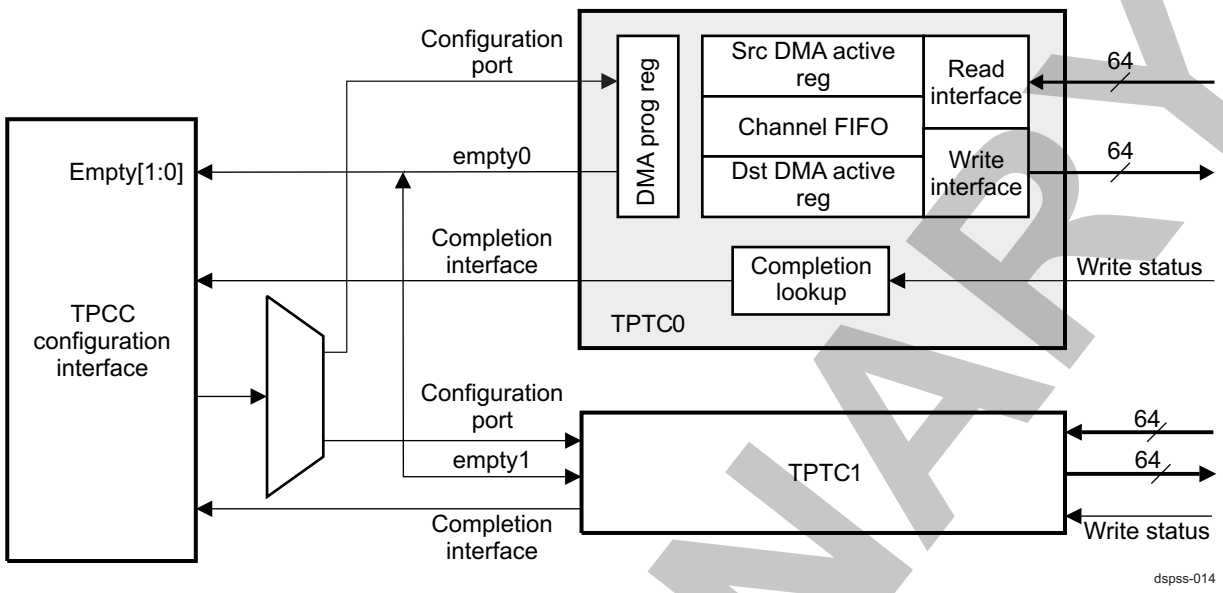
Figure 5-10. TPTC Block Diagram



The primary responsibility of the TPTC is to perform read and write transfers through the local interconnect to the slave peripherals, as programmed in the active and program register sets:

- In the TC stand-alone use model, the user directly programs the program and active register sets for a given channel (TPTC0 or TPTC1). Because of the TPCC, this mode is not the use case targeted for device applications; therefore, it is not emphasized in this chapter. For information about its programming model, see Section 5.4.3.5.5, *Direct Configuration to Transfer Channel (Not Recommended)*.
- In the TC external-control use model, the user does not directly program the active and program register sets. Instead, the TPCC is the user interface to the DMA_DSP system, and the TPTCs (TPTC0 and TPTC1) are slaves to the TPCC. This is the use case of the DMA_DSP in device applications.

5.3.3.2.2 Transfer Geometry

The TPTC supports a transfer geometry fully defined by the registers summarized here (see Figure 5-11):

- OPTx: Options, where x = 0 or 1
  - SAM: Source address mode; controls whether the source array is from incrementing addresses or from one FIFO address
  - DAM: Distant address mode; controls whether the destination array is to an incrementing address or to one FIFO address
  - FWID: Controls the width of the FIFO
- SRC: Source address
- DST: Distant address
- CNT: BCNT, ACNT
  - ACNT: Number of bytes in each array
  - BCNT: Number of arrays in each TR
- BIDX: DBIDX, SBIDX
  - SBIDX: Source B-dimension index; defines the address offset between starting addresses of each source array
  - DBIDX: Distant B-dimension index; defines the address offset between starting addresses of each destination array

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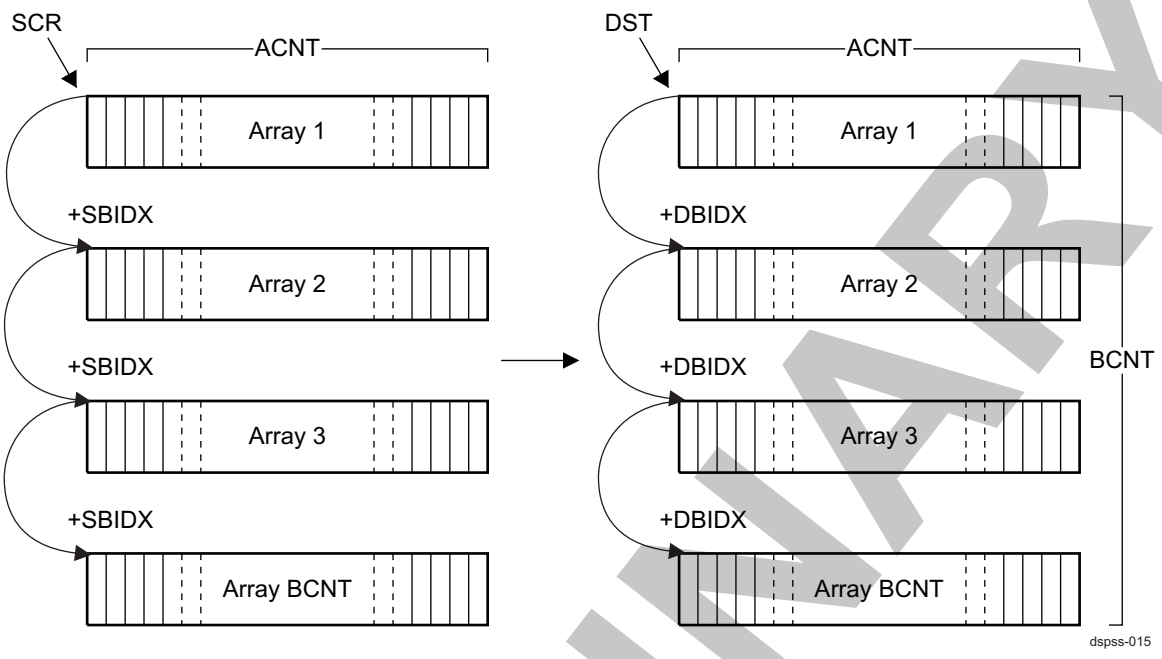
Figure 5-11. Transfer Geometry



NOTE: Many TI DMA controllers employ a concept of element size and element indexing. To maintain orthogonality, the concept of element size has been dropped. An element-indexed transfer is logically achieved by programming ACNT to the size of the element, and programming BCNT to the number of elements that must be transferred.

5.3.3.2.3 Tracking Transfers

Each TPTC channel consists of three register sets: a program register set and a source-active register set. The status of each of these register sets is indicated by the PROGBUSY, SRCACTV, DSTACTV, and WSACTV status bits, which are user-readable in the TPTC_TCSTAT register.

The program register set (TPTC_POPT, TPTC_PSRC, TPTC_PCNT, TPTC_PDST, TPTC_PBIDX, and TPTC_PMPPRXY) is never modified by the TPTC, because it is simply holding registers processed by the active register set. The source active register set (TPTC_SAOPT, TPTC_SASRC, TPTC_SACNT, TPTC_SADST, TPTC_SABIDX, TPTC_SAMPPRXY, TPTC_SACNTRLD, TPTC_SASRCBREF, and TPTC_SADSTBREF) tracks commands for the source side of the transfer.

As the source controller processes a TR, the SRC, DST, and CNT fields must be continuously updated as commands are issued. A reference value for these registers is also maintained. The active register set uses the reference address (SRCBREF and/or DSTBREF) to calculate the addresses of subsequent arrays in a transfer. This is required because subsequent arrays are defined as an offset from the starting address of the current array. Similarly, when a new array begins, the CNT must be restored (from CNTRLD) to the originally programmed value and decremented as the new array is processed.

The following summarizes the use of the active register sets:

- Static fields:
  - OPT
  - BIDX: DBIDX/SBIDX
- Dynamic fields:
  - SRC: Source address of the next read command to be issued
    - Tracked by the source active register set
  - DST: Distant address of the next write command to be issued
    - Tracked by the distant FIFO register set

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  - CNT: BCNT/ACNT
    - BCNT: Number of arrays remaining to be transferred. This includes the current array; that is, BCNT is decremented after all commands for an array are issued (or at least after all read or write commands are scheduled).
    - ACNT: Number of bytes remaining to be transferred
    - Tracked independently in the source and distant FIFO register sets
- Reference fields:
  - CNTRLD: ACNTRLD only
    - CNTRLD.ACNTRLD is set with the initial value of CNT.ACNT. The reload value is copied into CNT.ACNT when CNT.ACNT decrements to 0.
    - Tracked independently in the source and distant FIFO register sets

    Because a command is complete when BCNT decrements to 0, there is no reload value for BCNT.
  - SRCBREF: Source address reference points to the starting address of the array being read. The starting address of the next array is calculated as SRCBREF + SBIDX.
    - Tracked by the source active register set
  - DSTBREF: Distant address reference points to the starting address of the array being written. The starting address of the next array is calculated as DSTBREF + DBIDX.
    - Tracked by the distant FIFO register set

5.3.3.2.4 Completion Interface to TPCC

If TCINTEN or TCCHEN is set to 1, the TPTC must return completion information when the entire TR completes. The TPCC uses the completion information for chaining (enabled by TCCHEN) or posting interrupts (enabled by TCINTEN).

The TPTC generates status conditions based on the completion of a transfer (the TPTC_INTSTAT[1] TRDONE bit) and on the program register set transitioning to the downstream registers (the TPTC_INTSTAT[0] PROGEMPTY bit).

These two conditions can be enabled by the corresponding bits in the TPTC_INTEN register to generate an interrupt to the DSP_C0 CPU through the TCERRINTx interrupt line (TCERRINT0 for TPTC0, and TCERRINT1 for TPTC1). For the event mapping of these interrupt lines, see Table 5-3.

NOTE: The TRDONE and PROGEMPTY status bits are always available and are stored in the TPTC_INTSTAT register, regardless of the use model and regardless of whether the corresponding bits are enabled. Typically, these bits are used not in the TPCC use model, but in a stand-alone use model in which the user directly programs the TC.

For more information about DMA_DSP completion and its programming model, see Section 5.4.3.1, *Transfers From/to Device Memories/Peripherals (DMA_DSP)*.

5.3.3.3 DSP DMA Hardware Parameters

Table 5-4 lists the hardware parameter settings for the DSP subsystem.

Table 5-4. DMA_DSP Hardware Parameters

Module		Parameter	DSP Subsystem
DMA_DSP	TC	FIFO size for TC0	256 bytes
		FIFO size for TC1	128 bytes
		Data bus width	64 bits
		TR pipelining depth TC0	4
		TR pipelining depth TC1	2
		Endianness	Little
		Burst size	64

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Table 5-4. DMA_DSP Hardware Parameters (continued)

Module		Parameter	DSP Subsystem
	CC	Number of DMA channels	64
		Number of QDMA channels	8
		Number of PaRAM entries	128
		Number of Event Qs	2
		Number of TPTCs	2

NOTE: The TR pipelining depth controls the number of read TRs for a given transfer channel that can be serviced by the source transfer controller without being serviced by the distant transfer controller. This dictates the amount of storage required in the distant queue channel registers for in-flight TRs.

The user cannot directly program burst size, as with the system DMA (DMA_SYSTEM), but must rely on the ACNT/BCNT and issue 1D synchronization transfers to do so.

5.3.4 DSP MMU on L3_MAIN Interconnect

The MMU_DSP (the DSP subsystem level MMU with port on L3_MAIN interconnect) communicates accesses from the DSP core - DSP_C0 of the DSP subsystem to the L3_MAIN interconnect, mapping the 4 GiB of the DSP virtual addresses to any place in the 4-GiB address space of the device.

At reset, the MMU_DSP is disabled, and the DSP core CPU, i.e. DSP_C0, can access global memory mapping in the device from the 0x1100 0000 address. Addresses in the range of 0x0000 0000 to 0x10FF FFFF can be reached only by the DSP_C0, because it performs its own internal memory mapping. For more information, see Section 2.2, *L3_MAIN Memory Space Mapping* in Chapter 2, *Memory Mapping*.

The MMU_DSP features:

- 32 entries/fully associative translation lookaside buffer (TLB)
- One interrupt line to the MPU
- 32-bit virtual addresses, 32-bit physical addresses
- 4-KiB, 64-KiB, 1-MiB, and 16-MiB pages
- Predefined (static), software-driven (interrupt-based), or table-driven (hardware table-walker) software translation strategies
- 2-level descriptor hierarchy
- One intermediate page table
- Fault status and fault address register

NOTE: The endianness conversion capability of the MMU_DSP is not used in the DSP subsystem (the DSP is configured as a little-endian processor in the device). With this configuration, the setting of the MMU_RAM[9] ENDIANNESS bit is ignored, even if the user changes the value. For more information, see Chapter 20, *Memory Management Units*.

Figure 5-12 shows the integration and functionality of the MMU_DSP.

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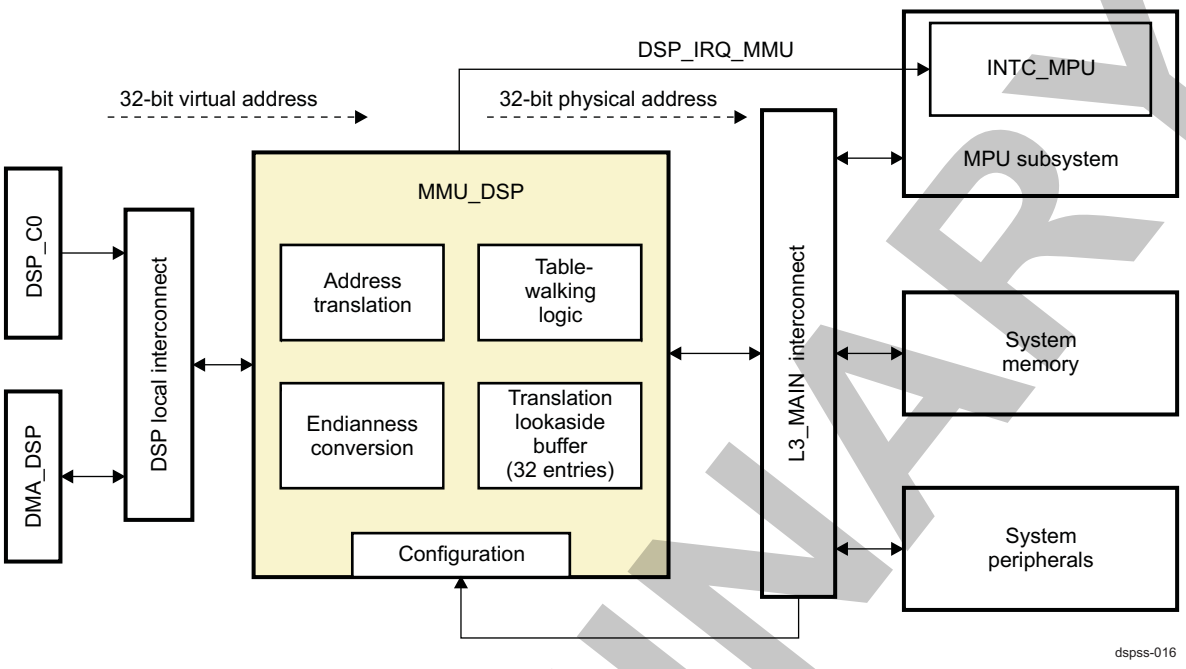
Figure 5-12. DSP MMU Block Diagram



5.3.4.1 DSP MMU VA-to-PA Translation

The MMU_DSP translates the 32-bit DSP external addresses to physical addresses in the 32-bit MPU address space. Address translation is performed by a translation table base (TTB) structure that maps the most-significant bits (MSBs) of the DSP byte address to another set of MSBs of a 32-bit MPU byte address. The least-significant bits (LSBs) of the DSP-generated byte address are used as page/section indices in the address translations and are not altered when forming the new 32-bit physical address. The TTB translations are expedited by a TLB that serves as a cache of recently used page translations. The address mapping can be programmed at the TTB level or by writing the TLB entries directly. The MMU_DSP contains 32 TLB entries that can be configured to remap 4-KiB, 64-KiB, 1-MiB, or 16-MiB segments of memory.

The TLB can be managed statically or dynamically (through the use of interrupts) by the MPU OS, but the MMU_DSP also includes hardware table-walking logic that lets it autonomously traverse the page table on a TLB miss. On a TLB miss, the translation table-walking logic automatically retrieves the information from the translation table stored in physical memory and updates the TLB cache.

Figure 5-13 shows the TTB structure in detail.

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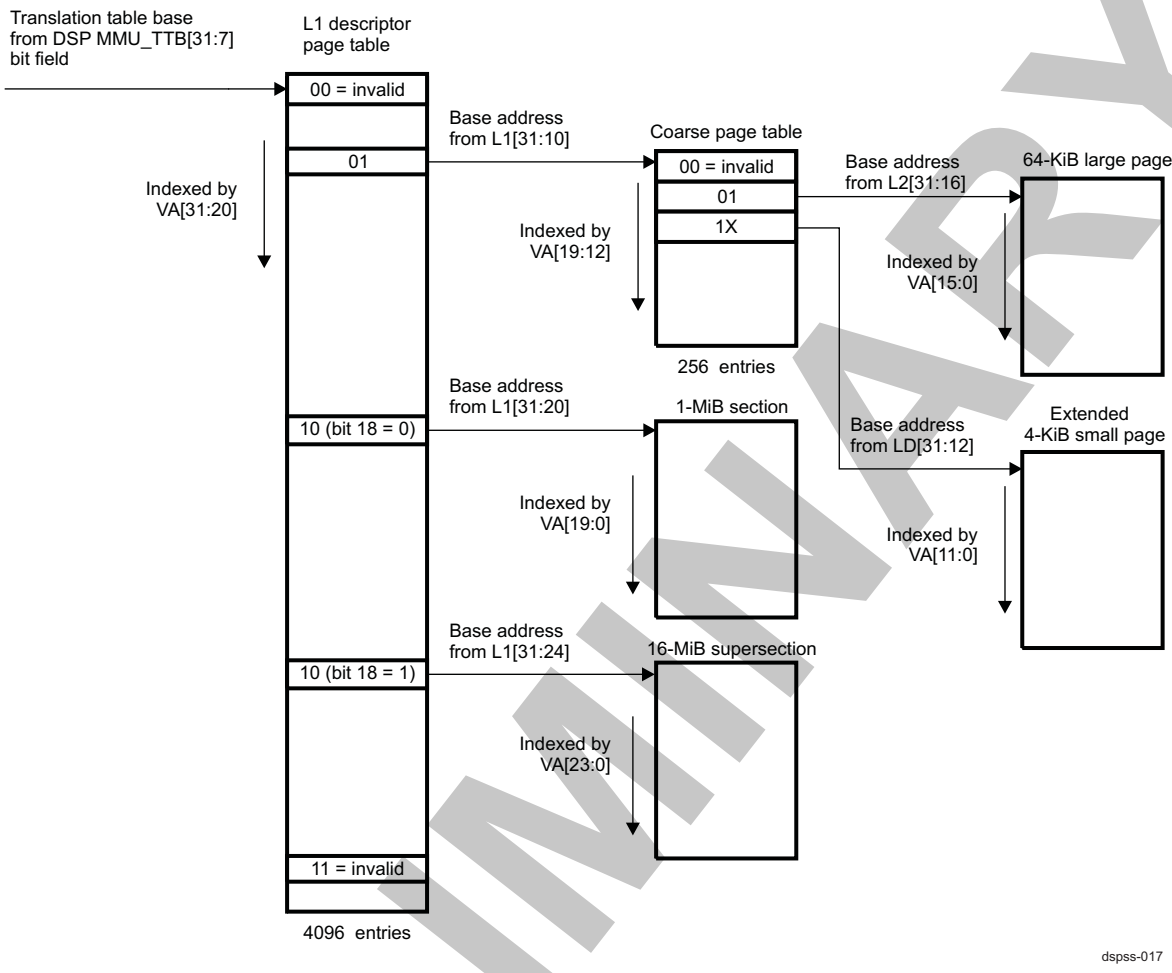
Figure 5-13. DSP MMU Translation Table Hierarchy



NOTE: The MMU_DSP passes the lower bits of the virtual address unchanged.

5.3.4.2 DSP MMU Configuration

If the MMU_DSP requires software intervention, the MPU services the event; MMU_DSP service requests are signaled to the MPU with a dedicated interrupt (see Table 5-3).

Generally, the MMU_DSP is initialized at boot time, but it can also be dynamically reprogrammed. Typically, the MMU_DSP is programmed by the device MPU through the DSP slave L4_CFG port on the L3_MAIN interconnect when a new task is created on the DSP subsystem. However, the DSP also has access to the MMU_DSP configuration registers for the save-and-restore process. At reset, the MMU_DSP is disabled and DSP virtual addresses are passed directly through as physical addresses (not translated).

For more information about the functions of the MMU_DSP in the DSP subsystem, including interrupts, register descriptions, and programming model, see Chapter 20, *Memory Management Units*.

5.3.5 Clock Configuration

The DSP subsystem receives one clock signal from the PRCM module (see Table 5-2).

Generation of these clocks is handled internally to the DSP subsystem by the SYSC module under direct control of the PRCM module.

Table 5-5 lists the clock domains in the DSP subsystem and the roles of the clocks.

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Table 5-5. DSP Internal Clock

Clock Domain	Clock	Description
CD0	CD0_CLK	DSP_C0 + PMC + DMC + L1/L2 caches + SCTM
CD1	CD1_CLK	Power-down logic (WUGEN_DSP) + INTC_DSP + external interfaces + DSP megamodule external interfaces + local interconnect + DMA_DSP + MMU_DSP + SYSC

NOTE: The internal clocks can be shut down by the PRCM module after the handshake protocol is complete. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management* in Chapter 3, *Power, Reset, and Clock Management*.

5.3.6 Hardware and Software Resets

5.3.6.1 Hardware Resets

See Table 5-2 for more information on the following reset signals:

- DSP_RST: Connected to the DSP megamodule and the DMA_DSP module
- DSP_WGN_RST: Connected to the DSP subsystem WUGEN module - WUGEN_DSP
- DSP_RET_RST: Connected to most of the blocks of the DSP subsystem. It resets the DSP subsystem logic, including the cache valid bits, cache enable bits, INTC_DSP, and some registers in the MMU_DSP.
- DSP_PWRON_RST: Performs a power-on initialization of the DSP subsystem logic

After chip power on, the DSP subsystem is kept under reset and only the DSP_RET_RST signal is released from reset. Then, only the WUGEN_DSP is released from reset as part of the CORE power domain. The DSP subsystem remains under reset until the MPU clears the DSP reset bit (see Section 3.5.4 , *Reset Domains* in Chapter 3, *Power, Reset, and Clock Management*). On this action, the PRCM module switches on the DSP power domain, sets the clocks back, and releases the power-on reset (POR). When the DSP power-on sequence completes (hardware handshake), the PRCM module releases the reset signal. At this stage, the DSP megamodule is kept under reset; the MPU can upload some code and data in the C64x+ memory. When the MPU has uploaded the code in the C64x+ memory, it releases the DSP megamodule from reset. At this point, the sequencer is kept under reset; the DSP can upload some code and data in the sequencer memory. When the DSP has uploaded the code in the sequencer memory, the DSP releases the sequencer from reset.

5.3.6.2 Software Resets

DSP subsystem reset signals are sourced from the PRCM module. Some modules of the DSP subsystem can also be reset by software control.

The MPU can apply a software reset to the DSP. For a software reset to be safe, the DSP subsystem must be in clock-off mode (DSP is in idle mode with clocks shut down by the PRCM module; for information about the clock-off state transition, see Section 5.4.6.3, *Power-Down and Wake-Up Management*). For instance, the MPU can use a mailbox interrupt to ask the DSP subsystem to go into IDLE state.

For some detected severe issues or if the user applies an external system reset, the DSP can receive a warm reset. All reset signals except POR are applied.

For more information on the DSP reset bits, see Section 3.7.2, *PD_DSP Description*, in Chapter 3, *Power, Reset, and Clock Management*.

NOTE: Software reset can be applied only while the DSP subsystem is in clock-off mode.

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The WUGEN_DSP reset signal (DSP_WGN_RST) is reset with the CORE power domain, which is reset when global cold or global warm reset events occur. For more information about global reset sources, see Section 3.5.4, *Reset Domains* in Chapter 3, *Power, Reset, and Clock Management*.

For more information about software resets, see Section 5.4.6.2, *Reset Management*.

5.3.7 Interrupt Requests

The DSP subsystem manages three types of interrupts (see Figure 5-14):

- Internal interrupts: Requests generated by modules in the DSP subsystem or in the DSP megamodule
- External interrupts: Requests generated by peripherals external to the DSP subsystem, such as serial port interface (SPI), display subsystem, or camera subsystem. Peripherals that generate interrupts at the DSP level use the D_IRQ_k input lines of the DSP subsystem.
- MMU_DSP interrupt: The DSP MMU on L3_MAIN interconnect can generate an interrupt to an external host outside the DSP subsystem. As shown in Figure 5-2, the interrupt line of the MMU_DSP (DSP_IRQ_MMU) is connected to the MPU interrupt controller - INTC_MPU.

For more information about the functions of the MMU_DSP, see Section 5.3, *DSP Subsystem Functional Description*.

To manage and expand the interrupt capabilities of the DSP megamodule (internal and external interrupt requests), the DSP subsystem includes two levels of interrupt control (see Figure 5-14):

- One INTC_DSP, integrated in the DSP megamodule. This module controls all interrupt requests (internal and external), except the MMU_DSP interrupt.

  For more information about the INTC_DSP, see Section 5.3.2.6, *DSP INTC*.
- One wake-up generator - WUGEN_DSP: Responsible at the DSP subsystem level for detecting wake-up events (interrupts, DMA requests, and slave port access) when the DSP subsystem is powered down (note that this may be a DSP low-power state under which DSP logic is still powered ON). The WUGEN_DSP also handles formatting interrupts from device peripherals to the DSP megamodule interrupt controller - INTC_DSP.

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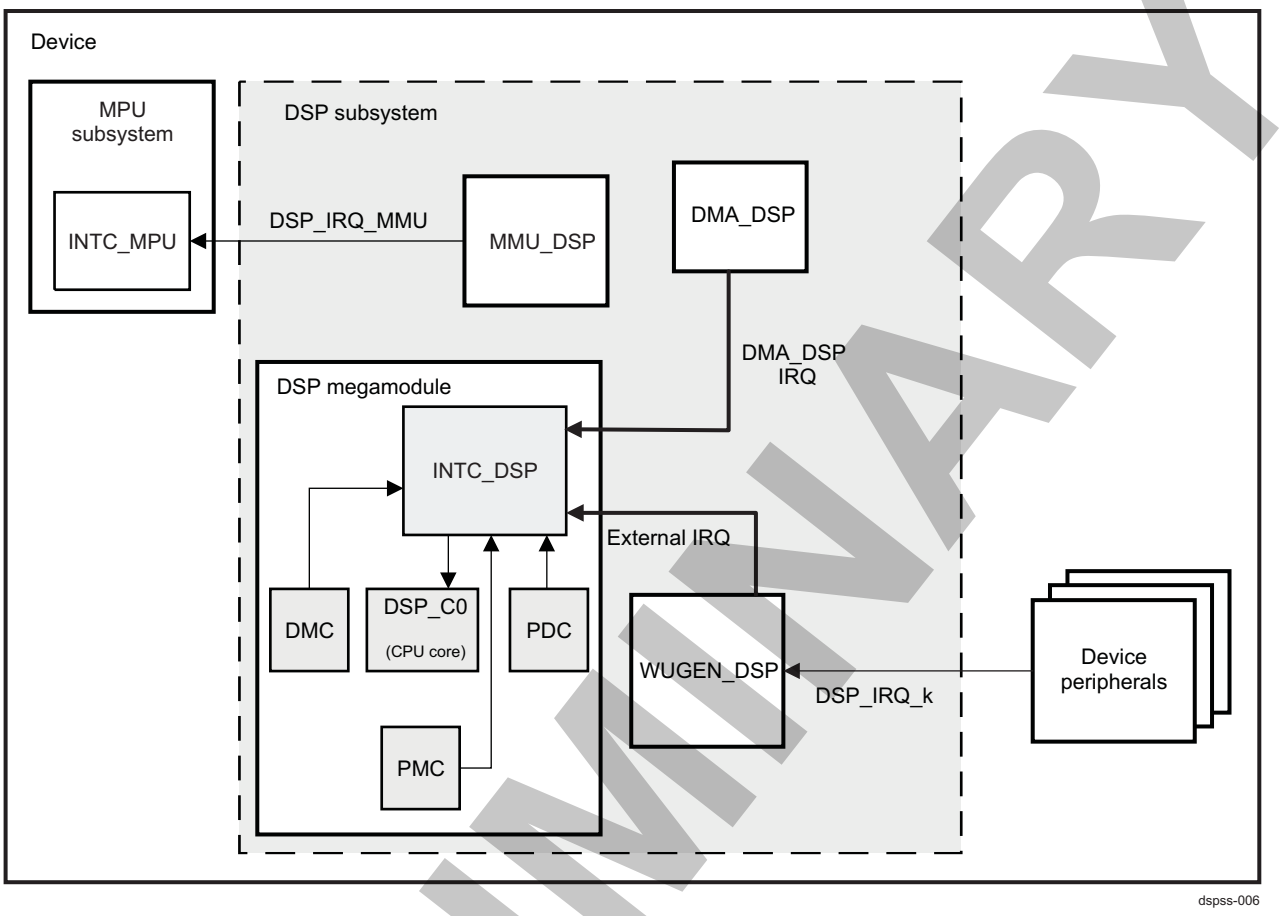
Figure 5-14. DSP Subsystem Interrupt Management



In addition to interrupt sources internal to the DSP subsystem, several interrupt sources coming from device peripherals are connected to the DSP megamodule interrupt controller - INTC_DSP, but not directly.

These external interrupt sources are resynchronized in the WUGEN_DSP, synchronously with the CD1_CLK clock, and then they are connected to the INTC_DSP.

Table 5-6 lists the global interrupt mappings of the DSP subsystem.

Table 5-6. DSP Interrupt Mappings

EVT	Interrupts/Events	DSP Subsystem Pin Name	Interrupt Source	Description
DSP_IRQ_0	EVT0	N/A (internal)	INTC_DSP	Output of event combiner 0, for events 4-31
DSP_IRQ_1	EVT1	N/A (internal)	INTC_DSP	Output of event combiner 1, for events 32-63
DSP_IRQ_2	EVT2	N/A (internal)	INTC_DSP	Output of event combiner 2, for events 64-95
DSP_IRQ_3	EVT3	N/A (internal)	INTC_DSP	Output of event combiner 3, for events 96-127
DSP_IRQ_4-8	Reserved	N/A (internal)	INTC_DSP	Reserved
DSP_IRQ_9	EMU_DTDMA	N/A (internal)	INTC_DSP	ECM interrupt (host scan access, DTDMA)
DSP_IRQ_10-14	Reserved	N/A (internal)	INTC_DSP	Reserved
DSP_IRQ_15	ABE_IRQ_DSP	D_WUGEN_0	INTC_DSP	ABE interrupt
DSP_IRQ_16	MMC1_IRQ	D_WUGEN_1	INTC_DSP	MMC/SD module 1 (L3_MAIN initiator)

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Table 5-6. DSP Interrupt Mappings (continued)

EVT	Interrupts/Events	DSP Subsystem Pin Name	Interrupt Source	Description
DSP_IRQ_17	MMC2_IRQ	D_WUGEN_2	INTC_DSP	MMC/SD module 2 (L3_MAIN initiator)
DSP_IRQ_18	Reserved	D_WUGEN_3	INTC_DSP	Reserved
DSP_IRQ_19	Reserved	D_WUGEN_4	INTC_DSP	Reserved
DSP_IRQ_20	Reserved	D_WUGEN_5	INTC_DSP	Reserved
DSP_IRQ_21	Reserved	D_WUGEN_6	INTC_DSP	Reserved
DSP_IRQ_22	Reserved	D_WUGEN_7	INTC_DSP	Reserved
DSP_IRQ_23	Reserved	D_WUGEN_8	INTC_DSP	Reserved
DSP_IRQ_24	Reserved	D_WUGEN_9	INTC_DSP	Reserved
DSP_IRQ_25	Reserved	D_WUGEN_10	INTC_DSP	Reserved
DSP_IRQ_26	ELM_IRQ	D_WUGEN_11	INTC_DSP	Error location process completion
DSP_IRQ_27	CCAET	N/A (internal)	INTC_DSP	TPCC AET event
DSP_IRQ_28	Reserved	N/A (internal)	INTC_DSP	Reserved
DSP_IRQ_29	CCINTG	N/A (internal)	INTC_DSP	TPCC global interrupt
DSP_IRQ_30	CCINT3	N/A (internal)	INTC_DSP	TPCC region 3 interrupt
DSP_IRQ_31	CCINT4	N/A (internal)	INTC_DSP	TPCC region 4 interrupt
DSP_IRQ_32	CCINT5	N/A (internal)	INTC_DSP	TPCC region 5 interrupt
DSP_IRQ_33	CCINT6	N/A (internal)	INTC_DSP	TPCC region 6 interrupt
DSP_IRQ_34	CCINT7	N/A (internal)	INTC_DSP	TPCC region 7 interrupt
DSP_IRQ_35	CCINT8	N/A (internal)	INTC_DSP	TPCC region 8 interrupt
DSP_IRQ_36	CCINT1	N/A (internal)	INTC_DSP	TPCC region 1 interrupt
DSP_IRQ_37	CCINT2	N/A (internal)	INTC_DSP	TPCC region 2 interrupt
DSP_IRQ_38	CCERRINT	N/A (internal)	INTC_DSP	TPCC error interrupt
DSP_IRQ_39	TCERRINT0	N/A (internal)	INTC_DSP	TPTC0 error interrupt
DSP_IRQ_40	TCERRINT1	N/A (internal)	INTC_DSP	TPTC1 error interrupt
DSP_IRQ_41-44	Reserved	N/A (internal)	INTC_DSP	Reserved
DSP_IRQ_45	IVA_IRQ_MAILBOX_1	D_WUGEN_12	INTC_DSP	IVA Mailbox interrupt 1
DSP_IRQ_46	HSI_IRQ_DSP_DMA	D_WUGEN_13	INTC_DSP	HSI DSP DMA interrupt request
DSP_IRQ_47	HSI_IRQ_DSP_P1	D_WUGEN_14	INTC_DSP	HSI DSP interrupt request - Port 1
DSP_IRQ_48	HSI_IRQ_DSP_P2	D_WUGEN_15	INTC_DSP	HSI DSP interrupt request - Port 2
DSP_IRQ_49	Reserved	D_WUGEN_16	INTC_DSP	Reserved
DSP_IRQ_50	Reserved	D_WUGEN_17	INTC_DSP	Reserved
DSP_IRQ_51	TIMER5_IRQ	D_WUGEN_18	INTC_DSP	General purpose timer module 5 (in ABE)
DSP_IRQ_52	TIMER6_IRQ	D_WUGEN_19	INTC_DSP	General purpose timer module 6 (in ABE)
DSP_IRQ_53	TIMER7_IRQ	D_WUGEN_20	INTC_DSP	General purpose timer module 7 (in ABE)
DSP_IRQ_54	TIMER8_IRQ	D_WUGEN_21	INTC_DSP	General purpose timer module 8 (in ABE)
DSP_IRQ_55	MAILBOX_IRQ_USER1	D_WUGEN_22	INTC_DSP	Mailbox user 1 interrupt request
DSP_IRQ_56	ISS_IRQ_4	D_WUGEN_23	INTC_DSP	Imaging Subsystem interrupt request
DSP_IRQ_57	PRM_IRQ_DSP	D_WUGEN_24	INTC_DSP	PRM Module (Part of PRCM)
DSP_IRQ_58	DISPC_IRQ	D_WUGEN_25	INTC_DSP	Display controller interrupt request
DSP_IRQ_59	GPMC_IRQ	D_WUGEN_26	INTC_DSP	GPMC interrupt
DSP_IRQ_60	UART3_IRQ	D_WUGEN_27	INTC_DSP	UART3 module interrupt (also infrared - IRDA)
DSP_IRQ_61	Reserved	D_WUGEN_28	INTC_DSP	Reserved
DSP_IRQ_62	Reserved	D_WUGEN_29	INTC_DSP	Reserved
DSP_IRQ_63	MCPDM_IRQ	D_WUGEN_30	INTC_DSP	MCPDM interrupt (in Audio BE)
DSP_IRQ_64	Reserved	D_WUGEN_31	INTC_DSP	Reserved

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Table 5-6. DSP Interrupt Mappings (continued)

EVT	Interrupts/Events	DSP Subsystem Pin Name	Interrupt Source	Description
DSP_IRQ_65	Reserved	D_WUGEN_32	INTC_DSP	Reserved
DSP_IRQ_66	Reserved	D_WUGEN_33	INTC_DSP	Reserved
DSP_IRQ_67	Reserved	D_WUGEN_34	INTC_DSP	Reserved
DSP_IRQ_68	Reserved	D_WUGEN_35	INTC_DSP	Reserved
DSP_IRQ_69	Reserved	D_WUGEN_36	INTC_DSP	Reserved
DSP_IRQ_70	Reserved	D_WUGEN_37	INTC_DSP	Reserved
DSP_IRQ_71	Reserved	D_WUGEN_38	INTC_DSP	Reserved
DSP_IRQ_72	Reserved	D_WUGEN_39	INTC_DSP	Reserved
DSP_IRQ_73	GPIO1_IRQ_2	D_WUGEN_40	INTC_DSP	GPIO1 module - interrupt 2
DSP_IRQ_74	GPIO2_IRQ_2	D_WUGEN_41	INTC_DSP	GPIO2 module - interrupt 2
DSP_IRQ_75	GPIO3_IRQ_2	D_WUGEN_42	INTC_DSP	GPIO3 module - interrupt 2
DSP_IRQ_76	GPIO4_IRQ_2	D_WUGEN_43	INTC_DSP	GPIO4 module - interrupt 2
DSP_IRQ_77	GPIO5_IRQ_2	D_WUGEN_44	INTC_DSP	GPIO5 module - interrupt 2
DSP_IRQ_78	MCBSP1_IRQ	D_WUGEN_45	INTC_DSP	MCBSP1 / PORCOMMONIRQ : Common Synchronous Interrupt Request line
DSP_IRQ_79	MCBSP2_IRQ	D_WUGEN_46	INTC_DSP	MCBSP2 / PORCOMMONIRQ : Common Synchronous Interrupt Request line
DSP_IRQ_80	MCBSP3_IRQ	D_WUGEN_47	INTC_DSP	MCBSP3 / PORCOMMONIRQ : Common Synchronous Interrupt Request line
DSP_IRQ_81	Reserved	D_WUGEN_48	INTC_DSP	Reserved
DSP_IRQ_82	Reserved	D_WUGEN_49	INTC_DSP	Reserved
DSP_IRQ_83	DMIC_IRQ	D_WUGEN_50	INTC_DSP	DMIC interrupt (in Audio BE)
DSP_IRQ_84	L3_MAIN_IRQ_APP_ERR	D_WUGEN_51	INTC_DSP	Reports application or non-attributable errors on L3_MAIN interconnect
DSP_IRQ_85	Reserved	D_WUGEN_52	INTC_DSP	Reserved
DSP_IRQ_86	Reserved	D_WUGEN_53	INTC_DSP	Reserved
DSP_IRQ_87	MCSPI1_IRQ	D_WUGEN_54	INTC_DSP	MCSPI1 module - interrupt
DSP_IRQ_88	GPIO6_IRQ_2	D_WUGEN_55	INTC_DSP	GPIO6 module - interrupt 2
DSP_IRQ_89	DMA_SYSTEM_IRQ_0	D_WUGEN_59	INTC_DSP	DMA_SYSTEM interrupt 0
DSP_IRQ_90	DMA_SYSTEM_IRQ_1	D_WUGEN_57	INTC_DSP	DMA_SYSTEM interrupt 1
DSP_IRQ_91	Reserved	D_WUGEN_58	INTC_DSP	Reserved
DSP_IRQ_92	MCASP_IRQ_AXEVT	D_WUGEN_59	INTC_DSP	MCASP transmit interrupt (in Audio BE)
DSP_IRQ_93	Reserved	D_WUGEN_60	INTC_DSP	Reserved
DSP_IRQ_94	Reserved	D_WUGEN_61	INTC_DSP	Reserved
DSP_IRQ_95	DSI1_A_IRQ	D_WUGEN_62	INTC_DSP	Display DSI1_A interrupt request
DSP_IRQ_96	Reserved	D_WUGEN_63	INTC_DSP	Reserved
DSP_IRQ_97	DSI1_C_IRQ	D_WUGEN_64	INTC_DSP	Display DSI1_C interrupt request
DSP_IRQ_98	HDMI_IRQ	D_WUGEN_65	INTC_DSP	Display HDMI interrupt request
DSP_IRQ_99	IVA_IRQ_SYNC_0	D_WUGEN_66	INTC_DSP	Sync interrupt from iCONT1
DSP_IRQ_100	IVA_IRQ_SYNC_1	D_WUGEN_67	INTC_DSP	Sync interrupt from iCONT2 (DMA_IVA)
DSP_IRQ_101	FDIF_IRQ_2	D_WUGEN_68	INTC_DSP	Face detect interrupt 2
DSP_IRQ_102	Reserved	D_WUGEN_69	INTC_DSP	Reserved
DSP_IRQ_103	Reserved	D_WUGEN_70	INTC_DSP	Reserved
DSP_IRQ_104	Reserved	D_WUGEN_71	INTC_DSP	Reserved
DSP_IRQ_105	Reserved	D_WUGEN_72	INTC_DSP	Reserved
DSP_IRQ_106	Reserved	D_WUGEN_73	INTC_DSP	Reserved
DSP_IRQ_107	Reserved	D_WUGEN_74	INTC_DSP	Reserved
DSP_IRQ_108	Reserved	D_WUGEN_75	INTC_DSP	Reserved

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Table 5-6. DSP Interrupt Mappings (continued)

EVT	Interrupts/Events	DSP Subsystem Pin Name	Interrupt Source	Description
DSP_IRQ_109	Reserved	D_WUGEN_76	INTC_DSP	Reserved
DSP_IRQ_110	Reserved	D_WUGEN_77	INTC_DSP	Reserved
DSP_IRQ_111	Reserved	D_WUGEN_78	INTC_DSP	Reserved
DSP_IRQ_112 -119	Reserved	N/A (internal)	INTC_DSP	Reserved
DSP_IRQ_120	INTERR	N/A (internal)	INTC_DSP	Dropped CPU interrupt event
DSP_IRQ_121	MMU_CPU_INTR	N/A (internal)	INTC_DSP	MMU CPU maintenance completion interrupt
DSP_IRQ_122	MMU_HOST_INTR	N/A (internal)	INTC_DSP	MMU host maintenance completion interrupt
DSP_IRQ_123	L1_CPU_INTR	N/A (internal)	INTC_DSP	L1 maintenance completion interrupt
DSP_IRQ_124	L2_CPU_INTR	N/A (internal)	INTC_DSP	L2 maintenance completion interrupt
DSP_IRQ_125	SCTM_TIMEVT1_INTR	N/A (internal)	INTC_DSP	Timer interrupt 1
DSP_IRQ_126	SCTM_TIMEEVT2_INTR	N/A (internal)	INTC_DSP	Timer interrupt 2
DSP_IRQ_127	BUSERR	N/A (internal)	INTC_DSP	BUSERR interrupt

The interrupts generated by the WUGEN_DSP (interrupts from device peripherals) are programmable using a set of registers accessible by the user.

Events related to these external interrupts can be masked by writing to registers WUGEN_MEVTSET0 through WUGEN_MEVTSET4. The interrupts can also be individually unmasked by using registers WUGEN_MEVTCLR0 through WUGEN_MEVTCLR4. By default (after power on), these external interrupts are masked in the WUGEN_DSP.

All other interrupts are directly managed by the INTC_DSP, and the DSP registers are set. For information about the INTC_DSP, see the documents listed in Section 5.3.2.7, *Other DSP Reference Documents*.

5.3.8 DMA Requests

The DSP subsystem receives DMA requests from specific peripherals, such as the multichannel buffered serial port (MCBSP) module and the universal asynchronous receiver/transmitter (UART) module (see Figure 5-15).

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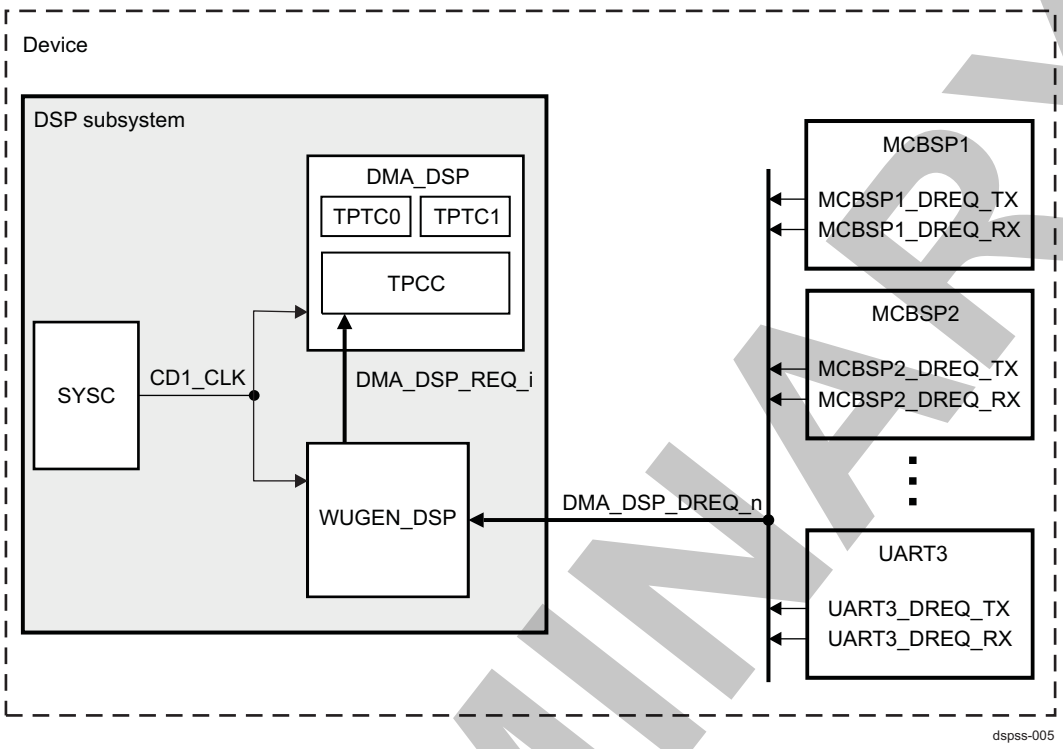
Figure 5-15. DSP DMA Requests



For a description of the DMA_DSP controller, see Section 5.3.3, *DSP DMA*.

For the DMA request mappings to the DSP subsystem DMA_DSP controller, see Table 5-3.

NOTE: All DMA_DSP requests are shared DMA requests, and they are mapped on the DMA_SYSTEM. For more information, see Section 16.5, *DMA_SYSTEM Basic Programming Model* in Chapter 16, *DMA_SYSTEM*.

For more information about DMA request management, see Section 5.4.3.2, *Programming an DMA_DSP Transfer*.

5.3.9 Wake-Up Generator

The WUGEN_DSP controls the following:

- Implementing the DSP idle handshake protocol with the PRCM module
- Resynchronizing interrupts and DMA requests from device peripherals external to the DSP subsystem
- Blocking the interrupts and DMA requests to the DSP on clean boundaries, when the WUGEN_DSP is asked to go into IDLE state
- Detecting the enabled wake-up interrupts and DMA requests and generating a wake-up event to the PRCM module
- Formatting interrupts to the DSP megamodule interrupt format

Figure 5-16 shows the WUGEN_DSP in the DSP subsystem and its interactions with other submodules.

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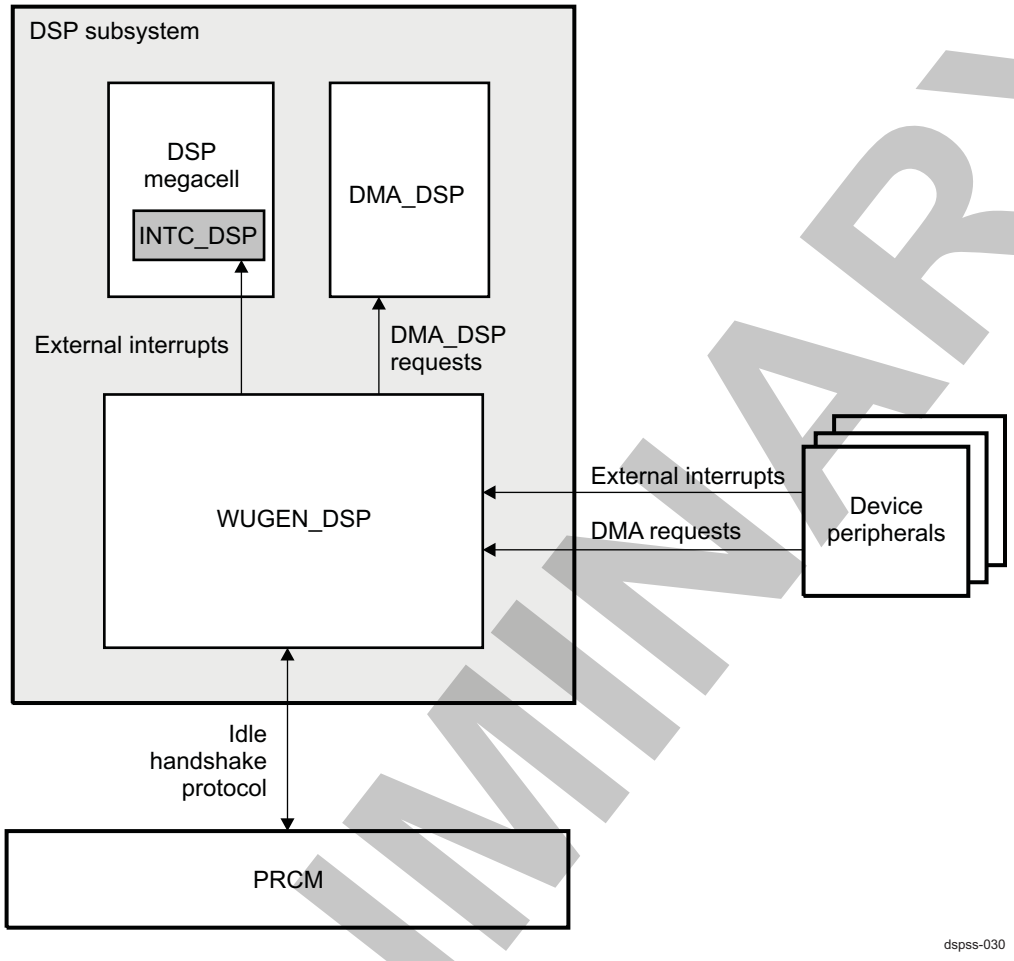
Figure 5-16. DSP WUGEN Description



5.3.9.1 Interrupts, DMA Requests, and Event Management

Interrupts and DMA requests are generated in the same way in the WUGEN_DSP. In this section, both are called events.

To manage interrupts, DMA requests, and slave port accesses from external modules, the WUGEN_DSP uses several sets of user-programmable registers:

- The WUGEN_MEVT0 through WUGEN_MEVT4 registers define individual mask bits for external asynchronous events (interrupts, DMA requests, and slave port access). This register is read-only, accessible only by the DSP. To modify the value of the individual mask, write 1 to the associated bits of the WUGEN_MEVTCLR0 through WUGEN_MEVTCLR4 registers (to clear) and to the WUGEN_MEVTSET0 through WUGEN_MEVTSET4 registers (to set).
- WUGEN_PENDEVT0 through WUGEN_PENDEVT4 are read-only registers that track which external events are pending in the WUGEN_DSP and are not yet generated to the DSP megamodule INTC or DMA_DSP. If an event is masked, this information is stable until the corresponding mask bit is cleared. If an event is unmasked, this information may not be stable, and therefore corresponds to a transitive period of processing the event in the WUGEN_DSP.

5.3.9.1.1 Event Generation

Figure 5-17 shows event-generation steps in the WUGEN_DSP.

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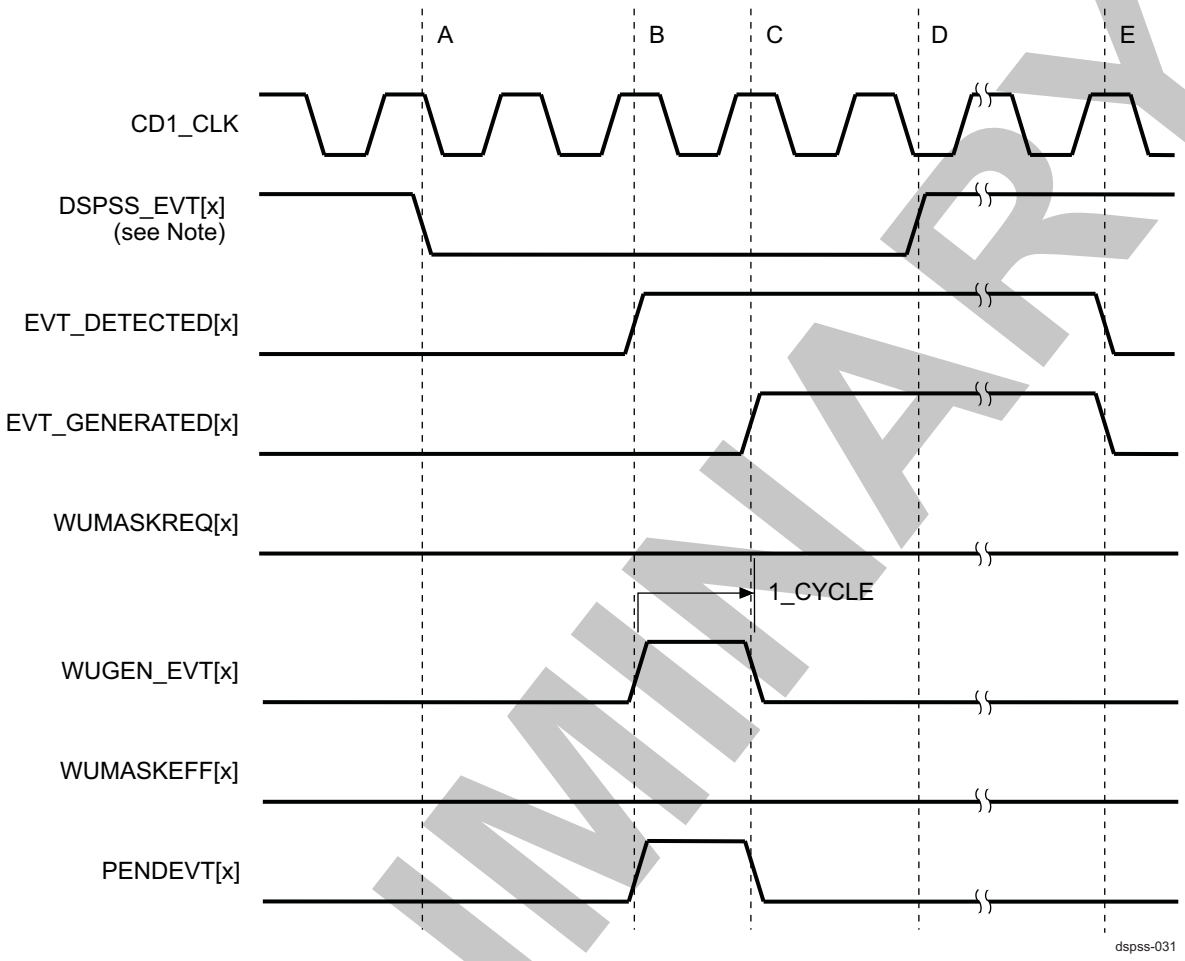
Figure 5-17. DSP WUGEN Event Generation



A An asynchronous event is asserted.

B The event is resynchronized and detected. Because the event is not masked, it is propagated to the DSP megamodule or DMA_DSP.

C The event-pending flag is cleared because the event was generated. The event to the DSP megamodule or DMA_DSP is deasserted after one WUGEN_DSP clock cycle.

D After a period of time, the source of the event is released (probably because it cleared in the corresponding interrupt status register).

E The release of the event is detected and clears the internal EVT_GENERATED flag for that interrupt.

NOTE: DSPSS_EVT[x] refers to DSPSSnIRQ[x] or DSPSS_nDMAREQ[x].

5.3.9.1.2 Individual Event Masking

To mask individual events, write 1 in the WUGEN_MEVTSET0 through WUGEN_MEVTSET4 registers of the WUGEN_DSP. These registers are used to mask interrupts and DMA requests.

Figure 5-18 shows event masking in the WUGEN_DSP.

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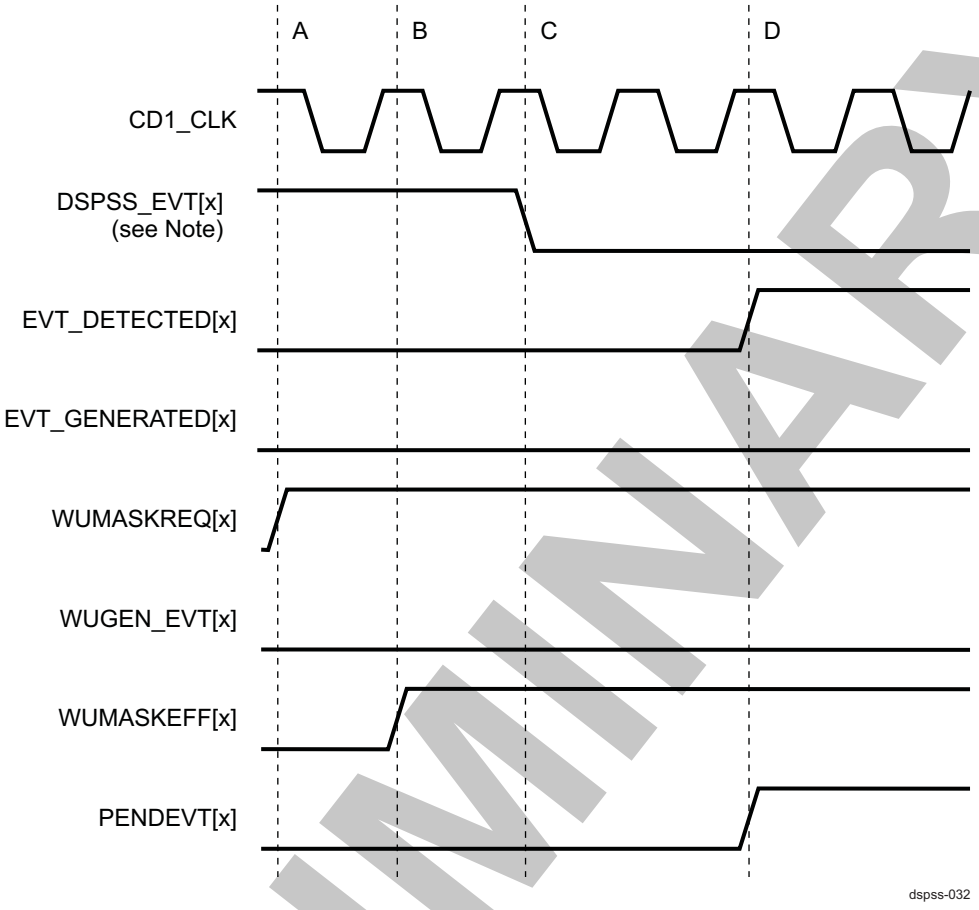
Figure 5-18. DSP WUGEN Event Masking



A The user sets the corresponding bit in the mask. Event generation is disabled.

B Completion of the event mask is shown in reads of the WUGEN_MEVT0 through WUGEN_MEVT4 registers.

C An asynchronous event is asserted.

D The event is resynchronized and detected. Because the event is masked, it is not propagated to the DSP megamodule or DMA_DSP. The event-pending flag is kept active (sticky) until the mask is removed.

NOTE: DSPSS_EVT[x] refers to DSPSS_nIRQ[x] or DSPSS_nDMAREQ[x].

5.3.9.1.3 Individual Event Mask Clear

To unmask individual events, write 1 in the WUGEN_MEVTCLR0 through WUGEN_MEVTCLR4 registers of the WUGEN_DSP.

Figure 5-19 shows event-mask-clearing in the WUGEN_DSP.

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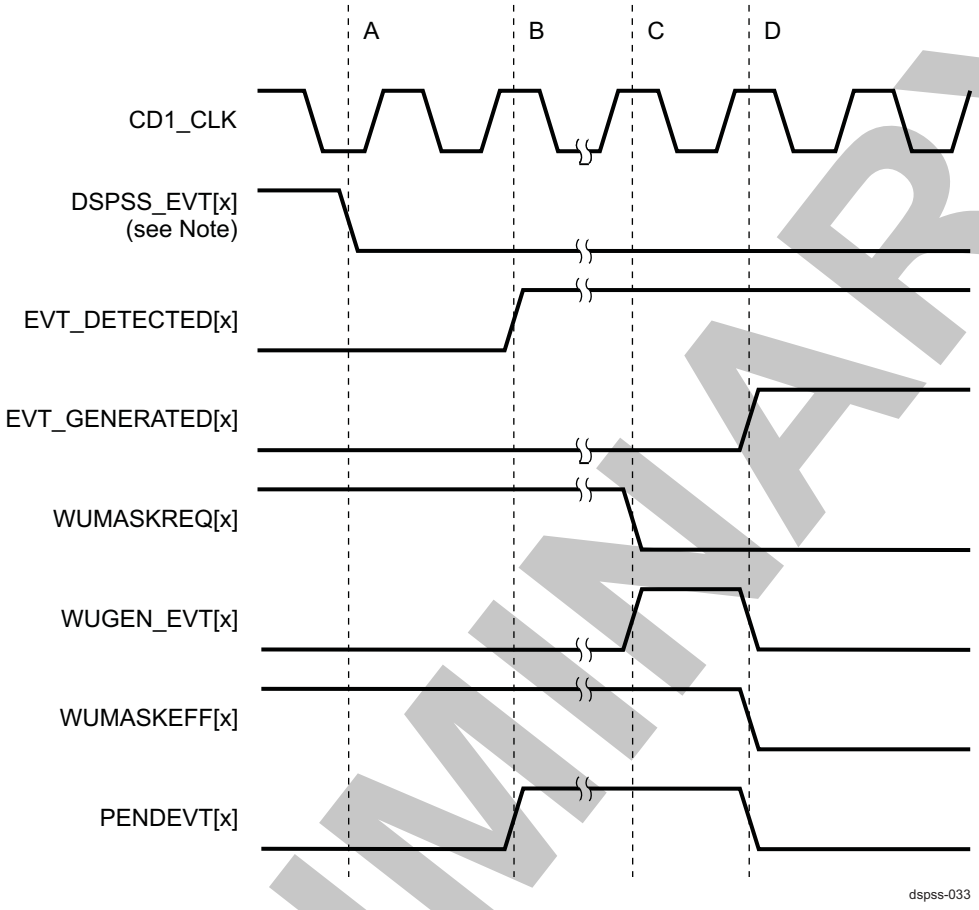
Figure 5-19. DSP WUGEN Event Mask Clear



A An asynchronous event is asserted.

B The event is resynchronized and detected. Because the event is masked, it is not propagated to the DSP megamodule or DMA_DSP. The event-pending flag is kept active (sticky) until the mask is removed.

C After a period of time, clear the corresponding bit in the WUGEN_DSP mask. The event is automatically generated to the DSP megamodule if the event is still seen as active. If the event is not seen as active, nothing happens.

D In both of the previous cases, the event-pending flag is cleared.

NOTE: DSPSS_EVT[x] refers to DSPSS_nIRQ[x] or DSPSS_nDMAREQ[x].

For more information about interrupts and the DMA_DSP programming model, see Section 5.4.4, *Interrupt Management*, and Section 5.4.3.1, *Transfers From/to Device Memories/Peripherals (DMA_DSP)*.

5.3.9.2 Idle Handshake

After reset, the WUGEN_DSP waits for a request. If the user executes the DSP IDLE instruction to put the DSP in STANDBY state, the SYSC initiates a clock-off handshake with the WUGEN_DSP.

5.3.10 SYSC Module

The SYSC module of the DSP subsystem controls the following functions:

- Generation of the divided clocks to all components of the DSP subsystem
- Synchronization of the DSP divided clocks and the DSP megamodule internal-divided clocks
- PRCM module power handshaking
- Sequencing of clock-to-off transition for the DSP modules

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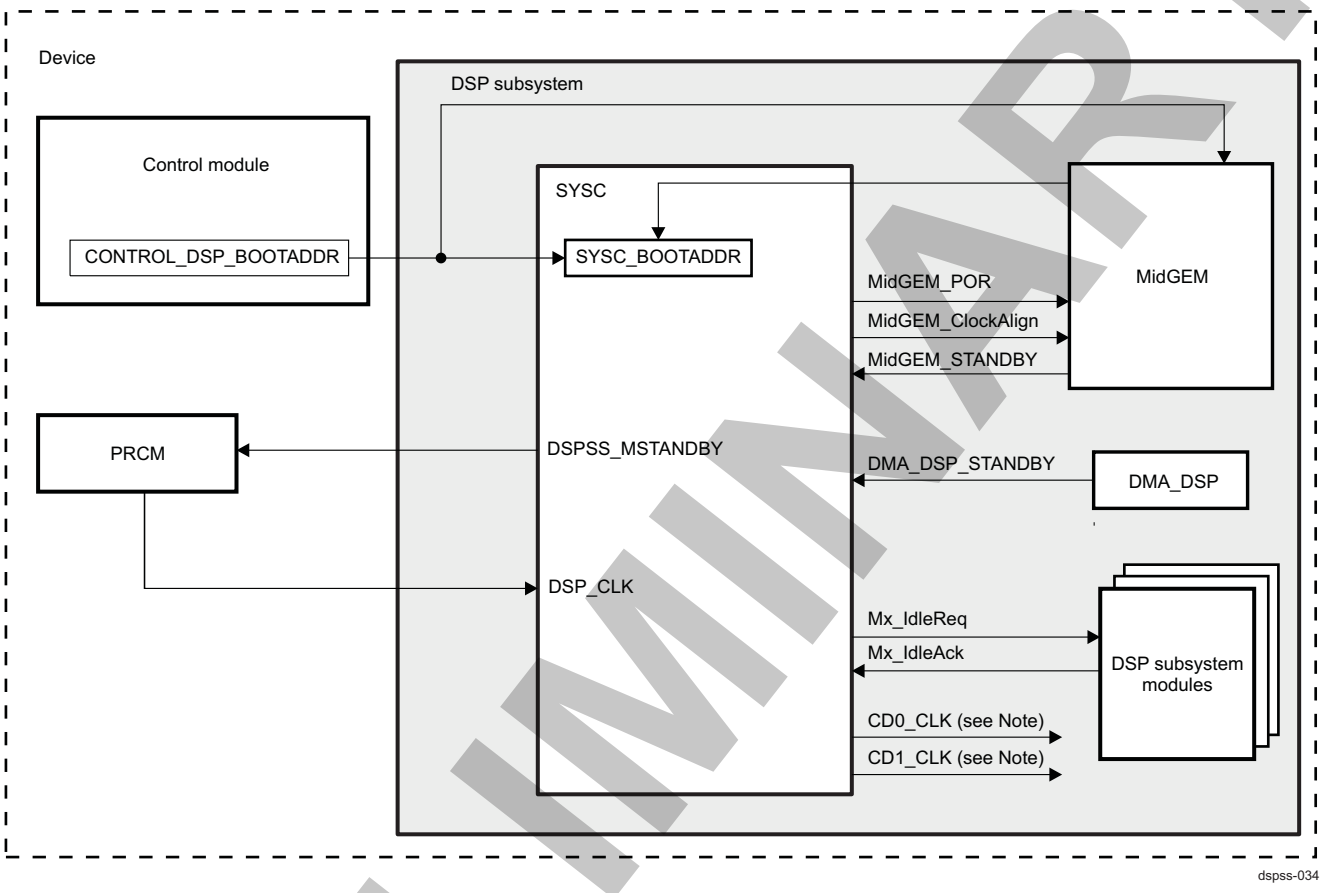
- Reset input resynchronization of the active-to-inactive transition to the CD1_CLK clock
- DSP subsystem boot configuration and its access from the DSP

Figure 5-20 is the block diagram of the SYSC in the DSP subsystem.

Figure 5-20. SYSC Block Diagram



NOTE: For more information, see Section 5.3.5, *Clock Configuration*.

5.3.10.1 Divided Clock Generation

The SYSC module generates the divided clocks used by the modules in the DSP subsystem. The SYSC generates the following clocks:

- CD0_CLK
- CD1_CLK

Based on the DSP_FCLK clock, these clocks are configured from the PRCM module. For details, see Section 5.3.5, *Clock Configuration*.

5.3.10.2 Clock Management, Power Down, and Wakeup

The SYSC ensures correct generation of the clocks described in Figure 5-20. The SYSC also allows management of the clock gating of the DMA_DSP and DSP megamodule if the user wants to lead some dynamic power aspects.

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The SYSC controls the transition to the DSP subsystem STANDBY state and standby signal generation (the DSPSS_MSTANDBY signal in Figure 5-20) to the PRCM module. Using the signals DSP_MEGACELL_STANDBY, DMA_DSP_STANDBY, Mx_IdleReq, and Mx_IdleAck, the SYSC manages and controls the correct power-down transition of the DSP subsystem and its submodules to ensure that the DSP subsystem internal clocks can be cut. For information about the DSP power-down transition and its programming model, see Section 5.4.6.3, *Power Down and Wakeup Management*.

External events can also occur at the DSP subsystem boundary (access to the DSP subsystem using the slave access port or external nonmasked events), requiring the restart of the DSP subsystem clocks (in case of DSP subsystem STANDBY state). The WUGEN_DSP controls the asynchronous generation of a wake-up signal to the PRCM module; this signal restarts DSP phase-locked loop (PLL) clock generation, allowing the SYSC to regenerate the DSP subsystem internal clocks.

5.3.10.3 Boot Configuration

SYSC_BOOTADDR is the boot-time configuration register. This read-only register is accessible only by the DSP, and its value is determined when the DSP subsystem is released from reset by the PRCM module.

The value of this register is driven externally by the control module register (CTRL_MODULE_CORE.CONTROL_DSP_BOOTADDR), which is read-write accessible by the MPU subsystem for MPU-driven DSP subsystem boot sequence and/or by the DSP for autonomous boot. For more information, see Section 5.4.1, *DSP Boot*.

NOTE: If the values of the CTRL_MODULE_CORE.CONTROL_DSP_BOOTADDR register change, the values of the new SYSC_BOOTADDR register are not updated until the next reset.

For more information, see Section 5.4.1, *DSP Boot*.

5.3.10.4 Interconnect Optimization

SYSC_VBUSM2OCP is a local interconnect configuration register. It is read-write accessible only by the DSP. Setting this register enables or disables interconnect optimization.

5.3.11 Local Memories

The DSP subsystem integrates the following memory controllers under the control of the DSP megamodule:

- Data memory controller (DMC)
- Program memory controller (PMC)

Depending on the software configuration of these memory controllers, local memories in the DSP subsystem can be used as cache or memory-mapped memories.

NOTE: When locking, the cache memory acts as if it is a memory-mapped memory. For more information about cache maintenance, see Section 5.4.2.2.3.1, *Maintenance of Caches*.

Figure 5-21 shows the memory hierarchy of the DSP subsystem.

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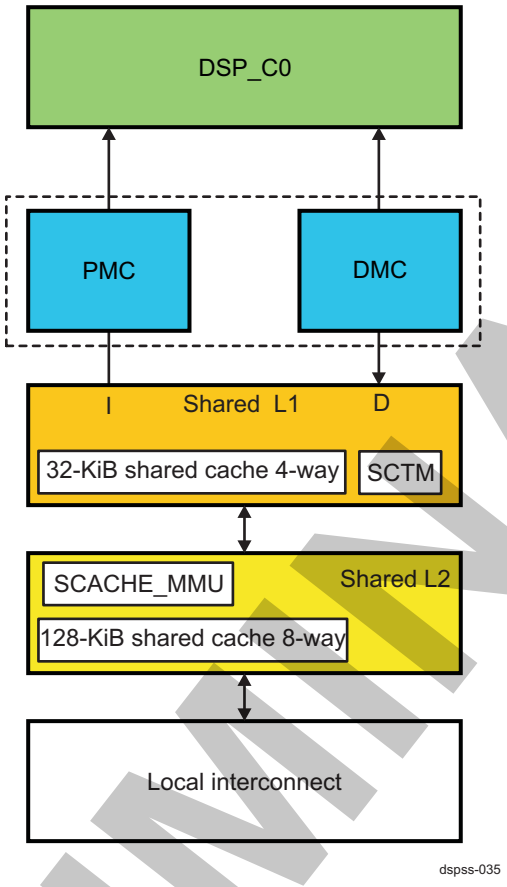
Figure 5-21. DSP Local Memories Hierarchy



5.3.11.1 L1/L2 shared cache Overview

The following features are supported by the shared cache controllers:

- 32-KiB L1 shared cache implemented with high-performance bit cell to run at full-speed
- 128-KiB L2 shared cache implemented with high-density bit cell to optimize area at half-speed
- L1 cache is 32B line size, 4-way set-associative, and organized as 16-bank.
- L2 cache is 32B line size and 8-way set associative.
- L1 cache supports snooping.
- L2 cache slave port to support snooping from DMA_DSP accesses
- Fully pipelined, supports critical-word-first
- Supports write-combining
- Fill and eviction buffers. Supports hit in fill buffer.
- Dynamic sizing, I/D allocation
- Prefetch 4 lines, preload N lines
- Background preload and clean

For information about the software programming model for cache management of the local RAM memories of the DSP subsystem, see Section 5.4.2, *Cache Management*.

5.3.12 SCTM

The SCTM is a generic profile counter and timer module that provides the following functions:

- Counter functions:

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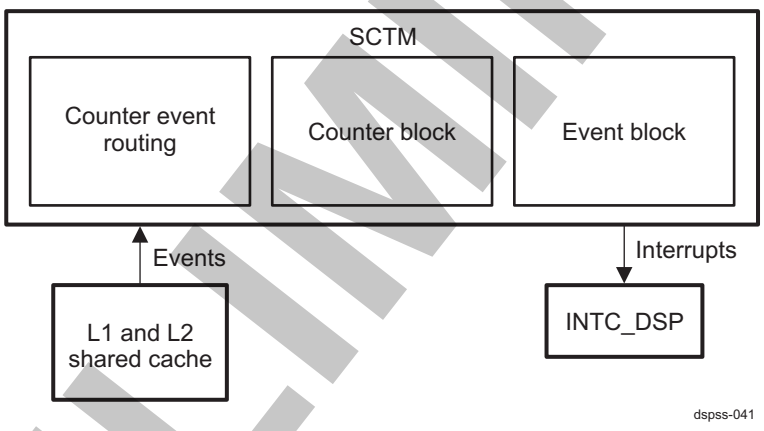
  - Input events counting
  - Two counter modes:
    - Event counting
    - Duration counting
  - Counter chaining
- Timer functions:
  - Periodic intervals generation
  - Two timer modes:
    - Run once mode
    - Restart mode
  - Events and/or interrupt generation

The SCTM has eight counters (two of which have timer functions). There are input events going into the SCTM and interrupt events going to the INTC_DSP. For more information about the counter configuration and the SCTM input events, see Section 29.6.3, *DSP Subsystem Performance Monitoring*, in Chapter 29, *On-Chip Debug Support*. For more information about the interrupt event signals, see Section 5.3.7, *Interrupt Requests*.

Figure 5-22 shows the SCTM block diagram.

Figure 5-22. SCACHE SCTM Block Diagram



5.3.12.1 Counter Functions

5.3.12.1.1 Input Events

Signals from within the subsystem are routed to the SCTM and used to control the counters and timers in the module. The routing of the input events from the module boundary to an individual counter is accomplished through an input event multiplexer and is controlled by the SCACHE_SCTM_CTCR_WT_i[20:16] INPSEL and SCACHE_SCTM_CTCR_WOT_j[20:16] INPSEL bit fields.

NOTE: For more information about input events to the module boundary, see Section 29.6.2.2, *Cache Events*, in Chapter 29, *On-Chip Debug Support*.

5.3.12.1.2 Counters

There are individual 32-bit counters in the SCTM. The counters count when the input event signals are asserted.

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5.3.12.1.2.1 Counting Modes

The counters in the SCTM support two mutually exclusive counting modes:

- Event mode: The counter increments each time a rising edge is detected on the designated input event signal.
- Duration mode: The counter continually increments when the event input is asserted.

5.3.12.1.2.2 Counter Overflow

When the counter reaches the terminal value (0xFFFFFFF) it wraps and continues to increment. This is considered a timer overflow condition. The SCACHE_SCTM_CTCR_WT_i[6] OVRFLW and SCACHE_SCTM_CTCR_WOT_j[6] OVRFLW bits indicate that overflow has occurred. The overflow bit can be cleared by reading it. When chained, only the high-order counter overflows.

5.3.12.1.2.3 Counters and Processor State

The counters can be configured to alter their behavior based on the state of the CPU. The SCACHE_SCTM_CTCR_WT_i[4] FREE and SCACHE_SCTM_CTCR_WOT_j[4] FREE bits determine whether the counter will continue to operate when the processor enters debug halt state. When the FREE bit is set to 0, the counter stops incrementing while the debug halt input from the CPU is asserted. Normal operation resumes when the processor exits the debug halt state and the debug halt input is deasserted. When the FREE bit is set to 1, the state of the debug halt input is not used to control counter operation.

The SCACHE_SCTM_CTCR_WT_i[5] IDLE and SCACHE_SCTM_CTCR_WOT_j[5] IDLE bits determine whether the counter will continue to operate when the processor enters idle state (the processor is no longer executing instructions and is waiting for a wake-up event). When the IDLE bit is set to 0, the counter stops incrementing while the idle input from the CPU is asserted. Normal operation resumes when the processor exits the idle state and the idle input is deasserted. When the IDLE bit is set to 1, the state of the idle input is not used to control counter operation.

5.3.12.1.2.4 Chaining Counters

The individual 32-bit counters in the SCTM can be chained with an adjacent counter to form a 64-bit counter. Counters chained to a counter across an even-odd index boundary with the even counter contain the least-significant 32 bits of the 64-bit pairing. For example, counters 1 and 0 can be paired and counter 1 will contain bits 63:32 and counter 0 will contain bits 31:0. The high-order counter increments by 1 each time the low-order counter wraps.

Counters are chained by setting the SCACHE_SCTM_CTCR_WT_i[2] CHAIN or SCACHE_SCTM_CTCR_WOT_j[2] CHAIN bit for both counters. When chained, the counter control for both counters is taken from the SCACHE_SCTM_CTCR_WT_i or SCACHE_SCTM_CTCR_WOT_j register of the low-order counter. Other than the CHAIN bit, all other bits in the high-order SCACHE_SCTM_CTCR_WT_i or SCACHE_SCTM_CTCR_WOT_j register are ignored.

Chained counters can function only in counter mode. Timer mode is not supported.

The SCACHE_SCTM_CTCR_WT_i[7] CHNSDW and SCACHE_SCTM_CTCR_WOT_j[7] CHNSDW bits are used to indicate that a counter can provide atomics accessed when chained. These bits are valid only for counters with even indexes (the lower half of a 64-bit counter pair). When these bits are set, the counter can shadow the value of the lower half of the chained counter value at the same time the upper half of the counter is read. The shadowed value (not the current value) is returned when the value of the low-order counter is read. Therefore, when a chained counter has atomic read capability, an atomic counter value can be obtained simply by reading the high-order counter first, followed by the low-order counter. This order must always be observed to prevent reading stale counter values from the low-order counter. When counters are functioning independently, the shadow feature is deactivated and a read of the counter always returns the current value.

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5.3.12.1.2.5 Enabling and Disabling Counters

After the counter is correctly configured, it can be started by setting the SCACHE_SCTM_CTCR_WT_i[0] ENBL or SCACHE_SCTM_CTCR_WOT_j[0] ENBL bit. At this point, the counter begins incrementing under the control of the configured event input. The counter can be disabled (counting stops) at any time by clearing the ENBL bit. Counters can be enabled and disabled dynamically during application flow.

Counters can also be enabled and disabled as groups through the SCACHE_SCTM_CTGNBL register. This register provides control of the individual counter-enable in groups. This allows an application to enable or disable groups of counters in lockstep by setting corresponding bits to 1 (bit number corresponds to counter number).

5.3.12.1.2.6 Resetting Counters

The counters can be reset to their initial value (0x00000000) by writing 1 to the SCACHE_SCTM_CTCR_WT_i[1] RESET or SCACHE_SCTM_CTCR_WOT_j[1] RESET bit. If the counter is chained, the high-order and low-order counters are reset when the RESET bit is written for the low-order counter.

Counters can also be reset as groups through the SCACHE_SCTM_CTGRST registers. These registers provide control of the individual counter reset in groups. This allows an application to reset groups of counters in lockstep.

5.3.12.2 Timer Functions

Counters 0 and 1 in the SCTM can function as timers. When operating as timers, interrupts and/or debug input events are generated when the value of the counter reaches a designated interval.

5.3.12.2.1 Periodic Intervals

The interval for a timer is contained in the SCACHE_SCTM_TINTVLR_i register. There is a SCACHE_SCTM_TINTVLR_i register for every timer-capable counter in the SCTM. Timers are initialized to 0. When the corresponding SCACHE_SCTM_CTCNTR_k increments and matches the values designated in SCACHE_SCTM_TINTVLR_i, the timer is considered to be triggered and events configured in SCACHE_SCTM_CTCR_WT_i are generated.

Timers can function in one of two mutually exclusive modes:

- Run-once mode: The timer stops after the first interval match and is not re-enabled until the timer is reset to the initial value (0) by setting the SCACHE_SCTM_CTCR_WT_i[1] RESET bit to 1.
- Restart mode: The timer automatically resets to the initial value (0) each time the designated interval is reached.

The SCACHE_SCTM_CTCR_WT_i[10] RESTART bit is used to configure the timer mode.

5.3.12.2.2 Event Generation

Timers can generate interrupts and debug events. Interrupts are routed from the module boundary to the INTC_DSP in the subsystem. Debug events are routed as triggers to debug logic within the subsystem.

The generation of the interrupts is controlled by the SCACHE_SCTM_CTCR_WT_i[8] INT bit. The generation of debug events is controlled by the SCACHE_SCTM_CTCR_WT_i[9] DBG bit. The INT and DBG bits can be set simultaneously and both signals are generated on interval match.

If neither INT nor DBG is set, the timer function is disabled and the counter functions as a regular counter.

5.3.13 Local Interconnect Network

The local interconnect network - (L2_MAIN_DSP) is the DSP subsystem internal logic that allows internal communication between the modules of the subsystem (for example, the DSP megamodule can communicate with the DMA_DSP or the WUGEN_DSP). Communication with the rest of the system is through the MMU_DSP as master port (accesses from the DSP subsystem to the L3_MAIN interconnect).

The MMU_DSP itself is configured from device MPU via a 32-bit DSPSS slave port on the L4_CFG interconnect.

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For information about global memory mapping of the DSP subsystem (DSP_C0 CPU view or MPU view through the L3_MAIN interconnect), see Section 2.2, *L3_MAIN Memory Space Mapping* in Chapter 2, *Memory Mapping*.

5.3.13.1 Endianness

The DSP subsystem local interconnect network does not support the big-endian convention or any type of endianness conversion. Only little endian is supported by the local interconnect network.

5.3.14 Error Reporting

Several mechanisms are available in the DSP subsystem to report errors at different levels.

The interrupt controller of the DSP megamodule allows reporting of dropped interrupts, through the INTERR signal.

L3_MAIN out-of-band errors are reported through the external L3_MAIN interrupt signal. For details about interrupt mapping, see Table 5-6. For information about L3_MAIN interconnect error reporting, see Section 14.2, *L3 Interconnect* in Chapter 14, *Interconnect*.

The DMA_DSP has its own error-reporting mechanism. Error-status registers and error interrupts inform the user of problems during internal operation (data error, bus activity error, etc.) of the DSP subsystem.

For information about error management and the register set that allows error tracing, see Section 5.4.7, *Error Identification Process*.

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5.4 DSP Subsystem Programming Guide

5.4.1 DSP Boot

The boot-time configuration register is SYSC_BOOTADDR. This read-only register is accessible only by the DSP_C0 CPU, and its value is determined when the DSP is released from reset, using the CTRL_MODULE_CORE.CONTROL_DSP_BOOTADDR register of the control module (for more information, see Section 18.4.12.1, *DSP Boot Register*, in Chapter 18, *Control Module*). A change to this register is not seen (not sampled) by the DSP subsystem until the next reset.

The DSP normally boots under MPU control, described in Section 5.4.1.2.1, *Boot Under MPU Control*.

A boot under MPU control occurs after the cold reset of the device as a first-time configuration of the DSP subsystem.

5.4.1.1 DSP Boot Configuration

When the DSP subsystem is released from reset, the first fetch address of the C64x equals the address defined in the CTRL_MODULE_CORE.CONTROL_DSP_BOOTADDR[31:10] DSP_BOOT_LOAD_ADDR bit field.

This address can be aligned on any 1-KiB boundary, in ROM, DSP local RAM, or on-chip memory (OCM-RAM), or directly in external memory (for example, SDRAM through the EMIF).

5.4.1.2 Example of DSP Boot

5.4.1.2.1 Boot Under MPU Control

Before waking up the DSP subsystem, the MPU performs the following sequence:

Step 1. The MPU prepares a translation table hierarchy (TTH) in SDRAM at address <TTH Physical Address>. This TTH must contain at least an address translation for the MMU_DSP physical address range.

NOTE: The DSP_C0 CPU does not require an address translation for the TTH, because the TTH is under MPU control only. The DSP_C0 CPU is responsible only for saving and restoring an MMU_DSP context that has been programmed by the MPU.

Step 2. The MPU writes a bootstrap sequence in SDRAM at address <BootLoader Physical Address>. This sequence is executable by the DSP_C0 CPU and contains only relative address references so that it is relocatable without code modification. This sequence must do at least the following:

(a) Set the size of the bootstrap code.

(b) Program the MMU_DSP.

NOTE: At minimum, the bootloader prepares the MMU_DSP for address translation of external accesses. Only from this point can the DSP subsystem work with virtual addresses.

For more information on the MMU_DSP, see Chapter 20, *Memory Management Units*.

Step 3. Program the MMU_DSP.

Step 4. The MPU can lock some other TLB entries, define some power-management MMU_DSP settings, and/or enable some interrupts.

Step 5. The MPU correctly programs the associated L3_MAIN firewall, ensuring that the DSP_C0 CPU has read access to the memory area containing the DSP bootstrap sequence.

Step 6. The MPU programs the associated L3_MAIN firewall, ensuring that the DSP_C0 CPU has read and write access to the configuration registers of the MMU_DSP.

Step 7. The MPU writes <bootloader physical address> to the CTRL_MODULE_CORE.CONTROL_DSP_BOOTADDR[31:10] DSP_BOOT_LOAD_ADDR

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bit field.

NOTE: For a detailed description of the system boot register, see Section 18.4.12.1, *DSP Boot Register*, in Chapter 18, *Control Module.*

Step 8. The MPU configures the DSP subsystem clock rate and DSP subsystem-related power-management settings in the PRCM module.

NOTE: Following Step 1 through Step 8, the DSP boot sequence is identical to the autonomous boot sequence. For information about the DSP boot sequence, see Section 5.4.1, *DSP Boot*.

After initialization completes, the MPU allows the DSP to boot:

1. The MPU brings the DSP to the ON state by programming the PRCM module.
2. The MPU sets the clocks back to the DSP subsystem.
3. The MPU releases the DSP from reset.

5.4.2 Cache Management

The DSP subsystem has a 2-level cache-based architecture:

- L1 cache (L1 shared cache) consists of a 32-KiB memory space.
- L2 memory/cache consists of a 128-KiB memory space shared by program and data space. L2 memory can be configured as mapped memory, cache, or a combination of the two.

The virtual address space is split into contiguous chunks to configure which parts of the memory are cacheable and which are not cacheable.

5.4.2.1 Cacheability Settings

This section describes the configuration of cacheability.

The address space of the DSP subsystem is split into contiguous regions of 16 MiB each. Each region has a cacheable attribute that defines whether a reference to a location belonging to the associated memory region must be sent directly to the memory (with exact size and occurrence as requested by the CPU) or must induce a cache line refill and potentially an eviction of another cache line.

The shared cache contains registers that control whether certain ranges of memory are cacheable and whether one or more requestors is allowed access to these ranges.

5.4.2.2 Coherence Maintenance

5.4.2.2.1 Memory-Mapped L1 or L2 Coherence

Coherence is maintained by hardware between L1 cache content and the L2 memory-mapped memory region.

An L2 reference from the DSP_C0 CPU updating an L1 cache location is automatically made visible to the DMA_DSP and any master processor on the device with access to the memory-mapped L2 of the DSP megamodule through the DSP subsystem slave port.

An L2 reference from the DMA_DSP and any other master processor on the device with access to the memory-mapped L2 of the DSP megamodule through the DSP subsystem slave port is automatically made visible to the DSP_C0 CPU through the L1 cache, if it is holding the associated cache line.

5.4.2.2.2 Device Memory Coherence

Coherence is not maintained by hardware between the L2 cache (and L1 cache) and device memories (on-chip memories external to the DSP subsystem and off-chip memories connected to the SDRAM controller and/or general-purpose memory controller [GPMC]). Coherence in this case must be handled by software. The DSP megamodule offers two sets of registers for user-initiated coherence maintenance between DSP local memories and device memories.

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Software coherence maintenance must be synchronized in the system (for example, through message passing; for information, see Chapter 19, *Mailbox*). In the producer/consumer model, the producer sends a completion message to the consumer only after the write is complete in end memory. If the producer has a cache-based architecture, the producer must initiate a write-back and track for the completion of the write-back sequence in end memory. When the consumer receives the message, if the consumer has a cache-based architecture, updates by the producer must be seen (not a local nonupdated copy). For a description of how the invalidate sequence occurs in the DSP subsystem, see Section 5.4.2.2.3, *Global Cache Management*.

Two types of cache coherence management are possible:

- Global cache coherence allows the DSP_C0 CPU to ensure coherence of the entire cache at once. See Section 5.4.2.2.3, *Global Cache Management*.
- Block cache coherence allows the DSP_C0 CPU to ensure coherence of a contiguous region of the virtual address map, restricted in size to only what is needed.

Each management type provides three sets of actions:

- Invalidate ensures that all required lines are made invalid in the cache. After that operation, any update (before invalidate operation) in end memory by an alternate processor/DMA_DSP is seen by the DSP_C0 CPU, thus forcing a cache line refill.
- Write-back ensures that all required cache lines modified by the DSP_C0 CPU (also called dirty lines) are written back to end memory so that any local update by the DSP_C0 CPU is made visible by an alternate processor / DMA_DSP. This applies to L1 and L2 caches.
- Write-back and invalidate ensure that all required cache lines modified by the DSP_C0 CPU are written back to end memory so that any local update by the DSP_C0 CPU is made visible by an alternate processor / DMA_DSP; they also ensure that all required lines are made invalid in the cache. After that operation, any update in end memory by an alternate processor / DMA_DSP is seen by the DSP_C0 CPU, thus forcing a cache line refill. This applies to L1 and L2 caches.

5.4.2.2.3 Global Cache Management

This section describes how to invalidate and write-back cache memory.

Maintenance is provided using the SCACHE_MMU_DSP. In addition, the L1 and L2 caches have independent start and end regions that are not limited by the size of the SCACHE_MMU_DSP entries.

Either SCACHE_MMU_DSP maintenance or cache maintenance can be used. However, only one maintenance operation at a time occurs. Direct cache maintenance also provides interrupts when complete.

Unlike SCACHE_MMU_DSP maintenance, direct cache (i.e. L1_SCACHE / L2_SCACHE controllers supported) maintenance locks only the lines already allocated in the cache, and not as needed during allocation.

5.4.2.2.3.1 Direct Maintenance of Caches

Shared cache allows basic maintenance operations, which are performed through a dedicated interface:

1. Preload
2. Lock
3. Clean
4. Invalidate

Maintenance of the cache is performed between the start and end addresses. This allows for direct control of the memory regions. All maintenance operations occur in the background and can generate an interrupt when they complete.

Cache maintenance is controlled by the following registers:

- SCACHE_MTSTART
- SCACHE_MTEND
- SCACHE_INT

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- SCACHE_MAINT

Example of global maintenance operation:

1. Configure the start address for cache maintenance by writing the SCACHE_MTSTART register.
2. Configure the end address for cache maintenance by writing the SCACHE_MTEND register.
3. (optional) Activate interrupt generation by writing 0x1 to the SCACHE_MAINT[5] INTERRUPT bit.
4. Select the maintenance type by writing to the SCACHE_MAINT[4:0] bit field (according to the selected maintenance).
5. Wait for the SCACHE_INT[2] MAINT bit to be set to 0 (maintenance is done).

NOTE: Hardware ensures that the maintenance operations are done first in L1, and then in L2.

5.4.2.2.3.2 Attribute MMU Maintenance

The attribute MMU - SCACHE_MMU_DSP provides maintenance control for the DSP_C0 cpu and MPORT. This can be done by setting the SCACHE_MMU_DSP small pages, or alternatively by setting the region for maintenance.

This is done to ensure that the caches can be maintained automatically across cache boundaries. For all maintenance operations, the L1 caches are updated before the L2 caches. This ensures that evictions from L1 are complete before any L2 maintenance.

If there are cache misses during maintenance clean/invalidate, they are considered noncacheable misses until the operation completes. However, hits function normally.

Individual caches can also be maintained separately using start and end addresses instead of pages. However, using SCACHE_MMU_DSP page maintenance has the benefit that the serialization is automatic. Also, the preload/lock feature is automatic during cache misses if the SCACHE_MMU_DSP maintenance is performed.

The basic control functions for maintenance are:

1. Preload
2. Lock
3. Clean (write out dirty lines, but do not invalidate directly)
4. Invalidate

These functions can be used in combination as described in Table 5-7. Either an interrupt or polling of the small page maintenance register indicates whether the maintenance operation is complete.

Only one maintenance operation at a time can be performed, including whether the processor directly accesses the cache maintenance registers. If the user writes a new maintenance operation before the first one completes, the configuration interface stalls.

Table 5-7 shows the combinations and results of setting multiple maintenance functions.

Table 5-7. Maintenance Combinations

Action Combinations	Preload	Lock	Unlock	Clean	Invalidate
Preload	1	0	0	0	0
Lock	0	1	0	0	0
Unlock	0	0	1	0	0
Clean dirty lines	0	0	0	1	0
Invalidate lines only	0	0	0	0	1
Clean -> Invalidate	0	0	0	1	1
Preload -> Lock	1	1	0	0	0
Clean -> Lock	0	1	0	1	0
Bus error	1	x	x	1	x
Bus error	1	x	x	x	1

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NOTE:

1. Illegal maintenance combinations (anything not listed in Table 5-7) generate a bus error (response error) on the configuration interface.
2. When a region is set for locking, the pages currently in the cache and any further misses to that region are locked.
3. Locked pages can still be cleaned or invalidated.
4. If all ways of the cache are locked and an allocation cannot occur, no bus error is generated. If a cache is missed when all ways are locked, the data is returned to the CPU, but the line is not allocated in the cache.
5. Queries from MPORT clean and invalidate lines even if they are locked.
6. Once page maintenance begins, the user cannot update the page again until the maintenance is complete.

5.4.2.2.3.2.1 Global Flush

Global flush is controlled by the SCACHE_MMU_MAINT and SCACHE_MMU_MAINTST registers.

Example of global flush:

1. Write 1 to the SCACHE_MMU_MAINT[10] G_FLUSH bit.
2. Wait for the SCACHE_MMU_MAINTST [0] STATUS bit to be set to 0 (maintenance is done).

NOTE: Hardware ensures that the maintenance operations are done first in L1, and then in L2.

5.4.2.2.3.2.2 Maintenance of Caches Through Attribute MMU

Global maintenance is controlled by the SCACHE_MMU_MAINT and SCACHE_MMU_MAINTST registers.

Example of global maintenance:

1. Start cache maintenance by writing 1 to the following registers:
   (a) SCACHE_MMU_MAINT[7] L1_CACHE1 bit to invalidate L1 cache 1
   (b) SCACHE_MMU_MAINT[8] L1_CACHE2 bit to invalidate L1 cache 2
   (c) SCACHE_MMU_MAINT[9] L2_CACHE bit to invalidate L2 cache
2. Wait for the SCACHE_INT[2] MAINT bit to be set to 0 (maintenance is done).

NOTE: Hardware ensures that the maintenance operations are done first in L1, and then in L2.

5.4.2.2.3.2.3 Maintenance of Attribute MMU Pages

SCACHE_MMU_DSP page maintenance is controlled by the following registers:

- SCACHE_MMU_MAINT
- SCACHE_MMU_MTSTART
- SCACHE_MMU_MTEND
- SCACHE_MMU_MAINTST

Example of invalidate:

1. Configure the start address for the cache maintenance by writing the SCACHE_MMU_MTSTART register.
2. Configure the end address for the cache maintenance by writing the SCACHE_MMU_MTEND register.
3. (optional) Activate interrupt by setting the SCACHE_MMU_MAINT[6:5] bit field to 1.
4. Select the maintenance type by setting the SCACHE_MMU_MAINT[4:0] bit field.
5. Wait for the SCACHE_MMU_MAINTST[0] STATUS bit to be set to 0 (maintenance is done).

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5.4.3 DSP DMA Management

5.4.3.1 Transfers From/To Device Memories/Peripherals (DMA_DSP)

The DMA_DSP optimizes transfers from/to the DSP megamodule (memory-mapped) memories to/from device on-chip and off-chip memories.

The DMA_DSP can perform transfers from DSP internal memories to DSP internal memories. In this case, use the DMA_DSP with the locked feature.

The DMA_DSP can perform transfers between device memories/peripherals, but it is not designed for that purpose. The DMA_SYSTEM is recommended in that case. For more information, see Section 16.5 , *DMA_SYSTEM Basic Programming Model* in Chapter 16, *Direct Memory Access Controllers*.

5.4.3.2 Programming an DMA_DSP Transfer

Programming a complete DMA_DSP transfer requires the following steps:

Step 1. Define the logical channel(s).

Step 2. Prioritize the defined transfer (with respect to other defined transfers).

Step 3. Start the transfer.

Step 4. Review the progression and completion of the transfer.

5.4.3.3 Defining a Logical Channel

5.4.3.3.1 Single Logical Channel Definition

A complete DMA_DSP transfer can be defined by one or several chained and/or linked logical channels.

Up to 128 independent contexts, each fully defining a logical channel, can be defined. These 128 contexts correspond to the 128 PaRAM entries available in the DSP subsystem. For more information about these PaRAM entries, see Section 5.3.3.1.3, *DMA/QDMA Channel Mapping and PaRAM Entry*, and the corresponding Figure 5-9.

Logical channel definition relies on the following:

- Base addresses:
  - PARAM[LCH#].SRCi: 32-bit source address
  - PARAM[LCH#].DSTi: 32-bit destination address
- Transfer sizes:

  Transfer size is common to source and destination. A transfer can be constituted on a 3D array; C is an array of CCNT arrays, each composed of BCNT arrays, each composed of ACNT bytes:
  - PARAM[LCH#].ACNT: Number of bytes in the A array (from 0 to 65,535)
  - PARAM[LCH#].BCNT: Number of A arrays in the B array (from 0 to 65,535)
  - PARAM[LCH#].CCNT: Number of B arrays in the C array (from 0 to 65,535)

  NOTE: Setting one of the ACNT, BCNT, or CCNT arrays to 0x0 prevents a transfer from being submitted to one of the physical channels (assuming that the compatibility mode is not set; see Kelvin DMA compatibility mode).
  - PARAM[LCH#].BCNTRLD: BCNT reload value when BCNT reaches 0 (from 0 to 65,535)

  NOTE: When programming CCNT>1, it is recommended to program PARAM[LCH#].BCNTRLD to be equal to PARAM[LCH#].BCNT.
- Indexes between dimensions:
  - PARAM[LCH#].SRCBIDX: Index between A arrays at source (from -32,768 to 32,767)
  - PARAM[LCH#].SCRCIDX: Index between B arrays at source (from -32,768 to 32,767)

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– PARAM[LCH#].DSTBIDX: Index between A arrays at destination (from -32,768 to 32,767)
– PARAM[LCH#].DSTCIDX: Index between B arrays at destination (from -32,768 to 32,767)

NOTE: Programming the logical channel does not automatically start it. See Section 5.4.3.5.1, *Assigning a Logical Channel to a Trigger Event.*

- Addressing modes:
  – PARAM[LCH#].OPT[0] SAM: Source addressing mode (0: post-incremented; 1: constant)
  – PARAM[LCH#].OPT[1] DAM: Destination addressing mode (0: post-incremented; 1: constant)

NOTE: Constant addressing mode is supported only from/to the DSP megamodule memories, not from/to device memories and peripherals. This can be replaced by using a post-increment addressing mode and an index equal to 0.

Example:

```
/* ------------------------------------------------- */
/* fills dstArray with cstValue values (w/o constant AM) */
/* ------------------------------------------------- */
PARAM[LCH#].SRC = &cstValue;
PARAM[LCH#].DST = &dstArray[0];
PARAM[LCH#].ACNT = sizeof(int);
PARAM[LCH#].BCNT = sizeof(dstArray) / sizeof(int);
PARAM[LCH#].CCNT = 1;
PARAM[LCH#].SRCBIDX = 0;
PARAM[LCH#].DSTBIDX = sizeof(int);
PARAM[LCH#].OPT.SAM = 0;
PARAM[LCH#].OPT.DAM = 0;
```

5.4.3.3.2 Controlling Submission Granularity

The logical channel (when triggered) can split a transfer into several requests submitted to one of the physical channels. The physical channel supports submitted requests of up to two dimensions, meaning that a 3D transfer is always split into (at least) 2D transfers. The user can also program the logical channel so that submitted requests are 1D transfers; for example:

- PARAM[LCH#].SYNCDIM = 0; // submitted transfers are maximum 1D.
- PARAM[LCH#].SYNCDIM = 1; // submitted transfers are maximum 2D.

5.4.3.3.3 Linking to Another Logical Channel

A logical channel can be programmed so that on its completion another context is copied from another logical channel. This is useful because the logical channel is used as a working set during the DMA transfer, meaning that the initial context configuration is lost after the associated transfer completes.

- PARAM[LCH#].LINK = linkLCH# << 5

The LINK value is the base address of the linked logical channel context.

When the LINK value is set to 0xFFFF, no context is loaded for that logical channel:

- PARAM[LCH#].LINK = –1

NOTE: Only the context is copied, and the logical channel is not automatically restarted on link. Restarting a logical channel that just received its new context occurs only when a trigger event associated with that logical channel is detected. See Section 5.4.3.5.1, *Assigning a Logical Channel to a Trigger Event*.

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5.4.3.3.4 Chaining Logical Channel

A logical channel can be programmed so that on its total or partial completion, another logical channel is started. This is useful for defining a series of transfers with different contexts as a complete DMA transfer. The main advantage is that the overhead to program all the chained transfers is shared among all channels.

- Partial completion chaining

  After the submitted section (see Section 5.4.3.3.2, *Controlling Submission Granularity*) of a logical channel is complete, a programmable completion code is returned. If partial completion chaining is enabled in the context of the logical channel, this completion code defines which trigger event is set. The logical channel associated with that trigger event is automatically submitted. See Section 5.4.3.5.1, *Assigning a Logical Channel to a Trigger Event*.

  For example, to chain a logical channel LCHi to LCHj so that LCHj is automatically started after each LCHi submission to a physical channel completes:

  – PARAM[LCHi].OPT.TCC = trigEvtx; // trigEvtx: Trigger event number
  – PARAM[LCHi].OPT.ITCCHEN = 1
  – DCHMAP[trigEvtx] = LCHj

- Total completion chaining

  After all submitted parts of a logical channel are complete, the programmable completion code is returned. If total completion chaining is enabled in the context of the logical channel, this completion code defines which trigger event is set. The logical channel associated with that trigger event is automatically submitted. See Section 5.4.3.5.1, *Assigning a Logical Channel to a Trigger Event*.

  For example, to chain a logical channel LCHi to LCHj so that LCHj is automatically started after LCHi completes:

  – PARAM[LCHi].OPT.TCC = trigEvtx; // trigEvtx: Trigger event number
  – PARAM[LCHi].OPT.TCCHEN = 1
  – DCHMAP[trigEvtx] = LCHj

5.4.3.4 Prioritizing Defined Transfers

5.4.3.4.1 Mapping Between DMA/QDMA Events and Event Queues

The assignment of 64 DMA and 8 QDMA channels to two event queues of the channel controller is achieved by configuring the DMA queue number register (TPCC_DMAQNUM_n, where n = 0 to 7) and the QDMA queue number register (TPCC_QDMAQNUM). When an event is selected for submission, it is queued in the user-defined event queue. This typically defines a 2-level priority preemption scheme, because queues are usually mapped to different transfer controllers.

5.4.3.4.2 Mapping a Queue to a Transfer Controller

Events at the head of an event queue define which logical channel (PaRam entry) is selected for submission to the associated physical channel (transfer controller). The association between an event queue and a physical channel can be defined in the TPCC_QUETCMAP register. By default, TPTC0 is associated with event queue 0, and TPTC1 is associated with event queue 1. This mapping is a static decision; it does not change during DMA operation.

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NOTE: TPTC0 and TPTC1 are not symmetrical; their numbers are simply inverted, compared to the Davinci device. To improve compatibility with Davinci devices, invert the mapping of the event queue to the transfer controller, as shown in the following:

QUETCMAP = (QUETCMAP &~0xFF) | 0x10;

Typically, this is used to allow submission-time preemption so that by example:

- Event queue 0 is used for background, potentially long, not latency-sensitive, noncritical DMA transfers.
- Event queue 1 is used for short, latency-sensitive, or critical (for example, hardware-synchronized) DMA transfers.

5.4.3.4.3 Handling Priority

In DSP subsystem local interconnect arbitration, the priority of individual bus requests for a DMA transfer over other DMA- or CPU-initiated bus requests is defined by the event queue to which the event associated with the transfer is submitted. This can be configured per event queue in the TPCC_QUEPRI[2:0] PRIQ0 and TPCC_QUEPRI[6:4] PRIQ1 bit fields. By default, event queues 0 and 1 have the same priority (the highest possible priority is 0x0).

Typically, this is used to allow transfer-time preemption so that, for example, bus requests associated with event queue 1 are served before event queue 1 or CPU requests.

Example:

- // DMA#0->0x7 (lowest), DMA#1->0x0 (highest), CPU->0x4 (mid)
- QUEPRI = (QUEPRI &~0xFF) | 0x07;
- MDMAARBE = (QUEPRI &~(0xF16)) | 0x4 16;

5.4.3.4.4 Aged Priority

To prevent DMA requests from being stalled for a long time, the DSP subsystem implements an aged priority scheme (also referred to as an inversion priority scheme) on the DMA_DSP ports to change the priority defined in the TPCC_QUEPRI register. This is done by regularly decreasing the priority level (increasing the priority in arbitration) of a stalled request. The interval between two consecutive updates of the priority level is defined in the SYSC_EDMA register. By default, the aged priority scheme is disabled (SYSC_EDMA = 0x0), and the arbitration priority is dictated by values programmed in TPCC_QUEPRI.

5.4.3.5 Starting the Transfer

Before starting the transfer, a trigger event must be associated with the logical channel. Three modes trigger a DMA transfer:

- Manual (software-synchronized transfers)
- Hardware (hardware-synchronized transfers)
- Automatic (automatic on-submission transfer start)

5.4.3.5.1 Assigning a Logical Channel to a Trigger Event

The 64 DMA channels and the 8 QDMA channels can be flexibly mapped to any of the 128 available PaRAM entries (see Figure 5-9).

Any of the 64 DMA channels can be mapped to any of the 128 PaRAM entries through the DMA channel-mapping registers TPCC_DCHMAPN_i (where i = 0 to 63).

Any of the 8 QDMA channels can be mapped to any of the 128 PaRAM entries through the QDMA channel-mapping registers TPCC_QCHMAPN_j (where j = 0 to 7).

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5.4.3.5.2 Manual Trigger (Software-Synchronized Transfers)

When a logical channel is defined and prioritized, the user can assign the logical channel (or the first in the chained list) to a trigger event (from 0 to 63) by writing the number of the logical channel (PaRAMEntry #) to one of the DMA channel-mapping registers (TPCC_DCHMAPN_i, where i = 0 to 63). Then, the user can manually start the transfer (one logical channel or a chained list of logical channels) by writing 1 to the bit in the TPCC_ESR or TPCC_ESRH register associated with the trigger event of the logical channel (or the first logical channel in the chained list).

NOTE: The event does not have to be enabled in the TPCC_EER register to be manually triggered.

Example:

```
/* ------------------------------------------- */
/* To manually start defined logical channel #0x3, uses event #20 */
/* ------------------------------------------- */
DCHMAP[20] = (DCHMAP[20] & ~(0x1FF<<5)) | 0x3<<5;ESR = 1 << 20;
```

5.4.3.5.3 Hardware Trigger (Hardware-Synchronized Transfers)

When a logical channel is defined and prioritized, the user can assign the logical channel (or the first in the chained list) to a trigger event (from 0 to 19) by writing the number of the logical channel (PaRAMEntry #) to one of the DMA channel-mapping registers (TPCC_DCHMAPN_i, where i = 0 to 19). The user can allow this logical channel to be triggered by an associated hardware DMA request by writing 1 in the associated bit of the EER register. The mapping of a hardware DMA request to DMA events is fixed. The mapping of DMA requests to device peripheral sources is listed in Table 5-3.

Example:

```
/* ---------------------------------------------------- */
/* Associate defined logical channel #0x5 to UART3_DMA_TX */
/* UART3_DMA_TX is DMA request #10 and associated to evt #10 */
/* ---------------------------------------------------- */
DCHMAP[10] = (DCHMAP[10] & ~(0x1FF<<5)) | 0x5<<5;
```

5.4.3.5.4 Automatic Trigger (QDMA)

The user can specify a trigger word from any of the eight 32-bit words of the logical channel context (PaRAM entry) for QDMA. Writing to the trigger word triggers the channel controller of QDMA to issue a transfer request. The trigger word field of the QDMA channel mapping register TPCC_QCHMAPN_j (where j = 0 to 7) defines the trigger word for a particular QDMA channel, as shown in Figure 5-9.

This flexibility enables the CPU to selectively modify only the PaRAM entry that requires modification and thereby trigger the transfer. For example, after a transfer, if only the count must change, QCHMAP can be configured so that count is the trigger word, and a write to it automatically triggers the transfer.

Example:

```
/* ------------------------------------------------ */
/* Associate defined logical channel #0x5 to QDMA #1 */
/* ------------------------------------------------ */
QCHMAP[1] = (QCHMAP[1] & ~(0x1FF<<5)) | 0x5<<5;
/* ------------------------------------------------ */
/* Define DST parameter (0x3) to be trigger word of LCH */
/* ------------------------------------------------ */
QCHMAP[1] = (QCHMAP[1] & ~( 0x7<<2)) | 0x3<<2;
```

5.4.3.5.5 Direct Configuration to Transfer Channel (Not Recommended)

The registers of the physical channels are memory-mapped primarily to enable, clear, and read status for error interrupts generated by the physical channel. For more information, see Section 5.4.7, *Error Identification Process*.

It is possible to write directly to other control registers of the physical channels and to issue a transfer; however, this is not recommended and therefore is not described here.

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This can work safely only if the DMA_DSP controller is not used.

5.4.3.5.6 DSP DMA Completion Mode

The DSP DMA defines when a DMA transfer is complete:

- Early completion: All associated transfers were submitted to the physical channel. Early completion does not ensure that the transfer is complete in end memory.
  - PARAM[LCHi].OPT.TCCMODE = 1
- True completion: All associated transfers were submitted to the physical channel and all are complete from the physical channel standpoint. True completion ensures that the transfer is complete in end memory.
  - SYSC_VBUSM2OCP.DMATRUECOMPEN = 1; // is statically set.
  - PARAM[LCHi].OPT.TCCMODE = 0

NOTE: TCCMODE = 0 does not ensure that the transfer is complete in end memory if DMATRUECOMPEN = 0.

By default, DMATRUECOMPEN = 0. This is recommended to statically set DMATRUECOMPEN.

True completion is typically used when the DMA_DSP is the producer of a buffer shared with another master processor or a DMA (consumer). A completion message is sent to the consumer only after the DMA transfer is complete.

Completion mode affects the timing for the following actions:

- IPR/IPRH bit update (for polling scheme)
- Interrupt generation (for interrupt scheme)
- CER/CERH bit update (for chaining)

5.4.3.5.7 Partial Versus Total Completion

DMA_DSP can be programmed so that the IPR bit update and interrupt generation occur:

- After each submission to the physical channel is complete
- After the last submission to the physical channel is complete

Partial completion interrupt

After the submitted section (see Section 5.4.3.3.2, *Controlling Submission Granularity*) of a logical channel is complete, a programmable completion code is returned. If a partial completion interrupt is enabled in the context of the logical channel, this completion code defines which IPR bit is set.

For example, to allow IPR to be updated (and possibly an interrupt to be generated) after each LCHi submission to a physical channel is complete:

- PARAM[LCHi].OPT.TCC = intEvtx; // intEvtx: IPR bit to be updated
- PARAM[LCHi].OPT.ITCINTEN = 1

Total completion interrupt

After all submitted parts of a logical channel are complete, a programmable completion code is returned. If a total completion interrupt is enabled in the context of the logical channel, this completion code defines which IPR bit is set.

For example, to allow IPR to be updated (and possibly an interrupt to be generated) after all LCHi submissions to a physical channel are complete:

- PARAM[LCHi].OPT.TCC = intEvtx; // intEvtx: IPR bit to be updated
- PARAM[LCHi].OPT.TCINTEN = 1

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– By polling
– By interrupt

5.4.3.5.8 Tracking DMA Completion

There are two ways to track DMA completion:

- Polling the completion register when the estimated completion time has elapsed
- Enabling completion interrupts

Polling example (total completion)

- PARAM[myLCH].OPT.TCINTEN = 1; // total interrupt completion bit update
- PARAM[myLCH].OPT.ITCINTEN = 0; // no partial interrupt completion bit update
- PARAM[myLCH].OPT.TCC = myTCC
- // myTCC does not contribute to interrupt generation (polling mode)
- IER = (IER &~(1<<myTCC)) | 0<<myTCC
- // start transfer
- DCHMAP[myEvt] = (DCHMAP[myEvt] &~(0x1FF<<5)) | myLCH<<5
- ESR = 1 << myEvt
- // do something useful (that does not depend on DMA completion)
- // poll IPR bit
- while(!(IPR & (1<<myTCC))); // polls for completion

Interrupt example (total completion)

- disable_interrupts()
- PARAM[myLCH].OPT.TCINTEN = 1; // total interrupt completion bit update
- PARAM[myLCH].OPT.ITCINTEN = 0; // no partial interrupt completion bit update
- PARAM[myLCH].OPT.TCC = myTCC
- // myTCC does contribute to interrupt generation (polling mode)
- IER = (IER &~(1<<myTCC)) | 1<<myTCC
- INTMUX[0] = (INTMUX[0] &~(0x7F)) | 0x1D; // map CPU it #4
- CPU.IER = (CPU.IER & (1<<4)) | 1<<4; // unmask CPU it #4
- enable_interrupts()
- // start transfer
- DCHMAP[myEvt] = (DCHMAP[myEvt] &~(0x1FF<<5)) | myLCH<<5
- ESR = 1 << myEvt
- // do something useful (that does not depend on DMA completion)
- // this code is interrupted when DMA completes

5.4.3.5.9 DMA Interrupt Service Routine

The channel controller does not generate a new interrupt signal for new pending interrupts if the user did not clear previous pending interrupts. There are two options for constructing an interrupt service routine (ISR) for DMA. The first option is to poll all the bits during execution of the ISR and clear all enabled bits in an interrupt-pending register by writing to the interrupt-pending clear (ICR/ICRH) register before exiting any ISR. The pseudo-code for this option is:

Step 1. Enter ISR.
Step 2. Read TPCC_IPR.
Step 3. For the condition set in TPCC_IPR:
(a) Perform operation as needed.
(b) Clear bit for serviced INT.

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Step 4. Read IPR:

(a) If TPCC_IPR = 0, exit ISR.

(b) If TPCC_IPR = 1, return to Step 3.

The second option is to service the ISR, and then before exiting the ISR, write to the EVAL bit of the IEVAL register. This forces the DMA_DSP channel controller to generate a new interrupt signal, if there are interrupts in the interrupt-pending register (IPR/IPRH). The pseudo-code for this ISR option is:

Step 1. Enter ISR.

Step 2. Read TPCC_IPR.

Step 3. For the condition set in TPCC_IPR:

(a) Perform operation as needed.

(b) Clear bit for serviced INT.

Step 4. Read IPR:

(a) If TPCC_IPR= 0, exit ISR.

(b) If TPCC_IPR= 1, set the TPCC_IEVAL.EVAL bit to force triggering a new interrupt.

5.4.3.5.10 Benchmarking

The DMA channel controller monitors the number of event entries in an event queue to determine whether they exceed the user-programmed threshold. The queue threshold for each event queue can be programmed in the TPCC_QWMTHRA and TPCC_QWMTHRB registers. When the number of event entries in an event queue exceeds the user-programmed threshold, a queue threshold error occurs. This error is captured in the THRXCD bit field of event-queue status register TPCC_QSTATN_i (where i = 0 or 1) and in the TPCC_CCERR QTHRXCDn bit field.

5.4.3.5.11 Kelvin DMA Compatibility Mode

Any channel can be configured to keep compatibility with Kelvin DMA settings. To do this, the user must set the TPCC_OPT_m[19] WIMODE bit. It is recommended to always clear this bit, except when reusing existing Kelvin code.

- PARAM[LCH#].OPT.WIMODE = 0

NOTE: If reusing existing Kelvin code, see the *eDMA Migration Guide for DM420*.

5.4.4 Interrupt Management

5.4.4.1 Interrupt Flow in DSP Subsystem

The DSP megamodule INTC_DSP detects, combines, and routes up to 128 system events (internal and external) to the 12 DSP_C0 CPU interrupt lines. For more information about interrupt mapping of the DSP subsystem (internal and external interrupts), see Table 5-6.

The WUGEN_DSP generator of the DSP megamodule internally routes the interrupt request to the IC module.

Figure 5-23 shows the interrupt flow of the DSP subsystem with the main wake-up generator and IC registers used for event generation.

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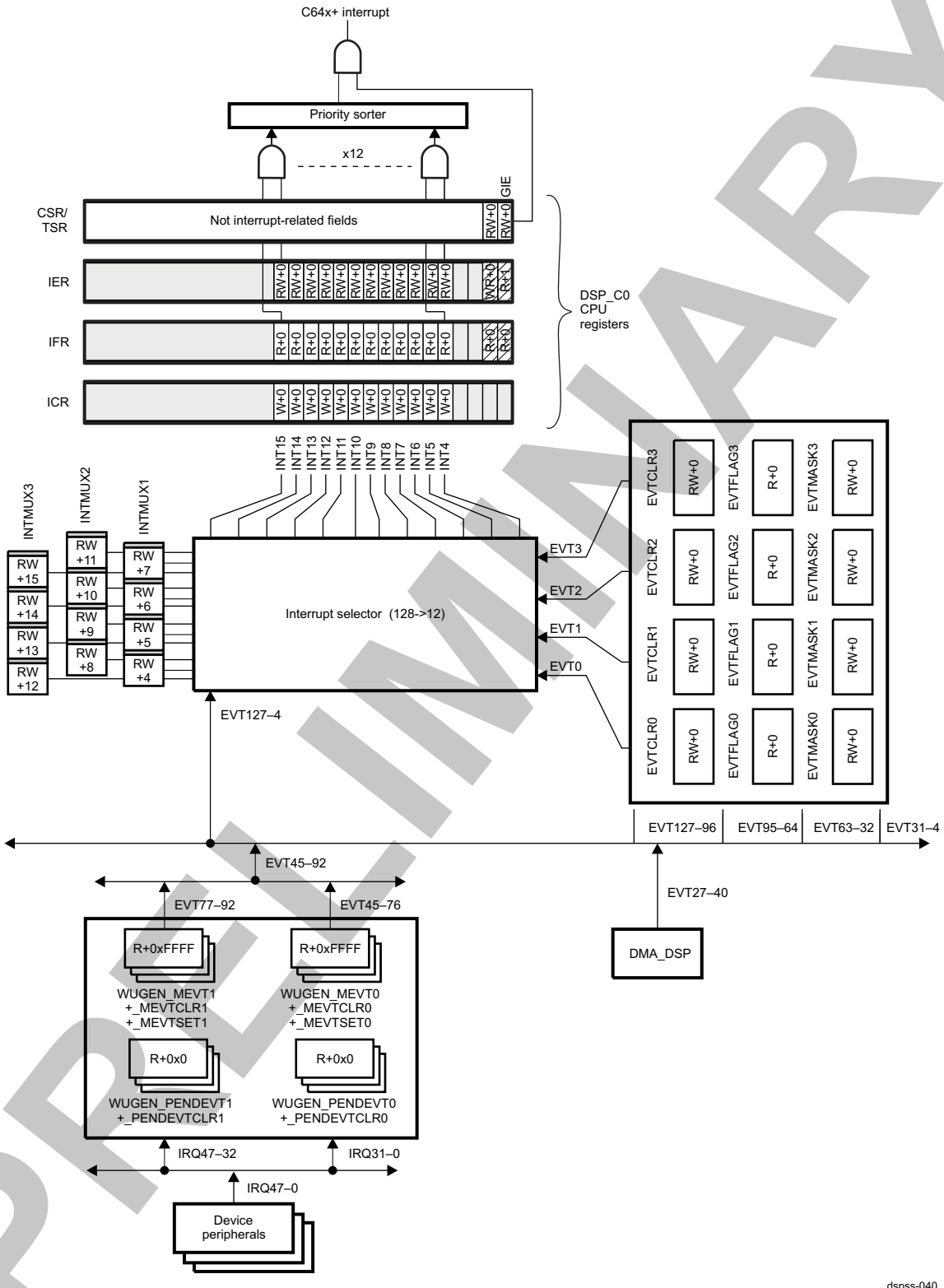
Figure 5-23. DSP Subsystem Interrupt Flow



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NOTE: The CSR/TCR, IER, IFR, and ICR registers belong to the DSP_C0 CPU block (C64x+). For more information, see the C64x+ documents listed in Section 5.3.2.7, *Other DSP Reference Documents*.

5.4.4.2 Event Combined Programming Sequence

In addition to generating a combined interrupt based on programmable event combinations, the event combiner provides a masked view of the event flag registers. By reading the masked event flag registers (SYS_INTC_MEVTFLAGi, where i = 0 to 3), the DSP_C0 CPU sees only the event flags pertaining to the corresponding combined event (EVTx, where x = 0 to 3).

When servicing a combined interrupt, perform the following steps:

Step 1. Read the SYS_INTC_MEVTFLAGi register corresponding to the combined event EVTx.

Step 2. Check the pending events.

Step 3. Write the value of the SYS_INTC_MEVTFLAGi register into the SYS_INTC_EVTCLRi register (where i = 0 to 3).

Step 4. Service the received interrupts.

Step 5. Repeat Step 1 through Step 4 until SYS_INTC_MEVTFLAGi = 0x0.

This clears only those events combined on EVTx. Events masked in the SYS_INTC_EVTMASKi register (where i = 0 to 3) do not need to be cleared if they are set in the SYS_INTC_EVTFLAGi register (where i = 0 to 3) (they can generate an exception or are used as event outputs).

Before returning, the DSP_C0 CPU must repeat Step 1 through Step 4 until no pending events are found. This ensures that events received during the ISR are captured. If an event EVTx is received at the same time that its flag is being cleared in the SYS_INTC_EVTCLRi register, it does not clear. Repeating Step 1 through Step 4 ensures that no events are missed.

5.4.4.3 Event <-> Interrupt Mapping Programming Sequence

The INTC_DSP allows programming independently which of the 128 input events is mapped to each DSP_C0 CPU interrupt; this is done by writing the event number in the bit field that corresponds to the CPU interrupt in the SYS_INTC_INTMUXj register (where j = 1 to 3).

Example:

```
/* ------------------------------------------------- */
/* evtTable has the 12 evt <-> CPU interrupt mapping */
/* ------------------------------------------------- */
evtTable[0] = 55;
// Mailbox event highest priorityevtTable[1] = 61;
// MCBSP1TX event[...]evtTable[11] = 29;
// DMA_DSP 3 gbl completion event lowest priorityfor(I=0; i<12; I++)
// for each CPU maskeable interrupt{
INTMUX(I >> 2 + 1) |= (evtTable[i] & 0x7F) << ((I & 0x3) << 3);}
```

5.4.4.4 Interrupt Exception Programming Sequence

The INTC_DSP can generate a system event (INTERR) that is internally routed to system event input EVT96. This event is generated when a DSP_C0 CPU interrupt is dropped (a DSP_C0 CPU interrupt is received while the interrupt flag is already set in the DSP_C0 CPU).

This can inform the user of possible problems in the software code, such as whether interrupts were disabled for an extended period of time, or whether pipelined (noninterruptible) code sections were too long.

NOTE: Because the interrupt drop detection logic is in the CPU, only interrupts sourced from a single system event can be detected. The dropping of individual combined events is not possible, although dropping the output of an event combiner is possible. Only the first dropped interrupt detected is reported by the INTERR event.

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The SYS_INTC_INTXSTAT register holds the ID of the CPU interrupt and the system event number of the dropped event. By setting the SYS_INTC_INTXCLR[0] CLEAR bit to 1, the software user resets the SYS_INTC_INTXSTAT register to 0.

When servicing the interrupt exception, the CPU performs three steps:

1. Reads the SYS_INTC_INTXSTAT register
2. Checks the error condition
3. Clears the error through the SYS_INTC_INTXCLR register

The dropped events that generate the INTERR event (EVT96) can be qualified by a mask register. CPU interrupts that are to be ignored by the drop detection hardware can be masked in the SYS_INTC_INTDMASK register.

5.4.4.5 INTC Basic Programming Model for Low-Power State of DSP Subsystem

To run the procedure for a correct transition to power-down state not involving logic-off, the user must perform the following procedure:

1. Ensure that all wake-up events are correctly mapped to enabled DSP_C0 CPU interrupts and are unmasked in combined event registers (if combined events are used).
2. Clear the associated bits in the WUGEN_MEVT0 and WUGEN_MEVT1 registers to unmask wake-up interrupts.

NOTE: Software must not unmask an event in the WUGEN_DSP that is not correctly mapped to an enabled DSP_C0 CPU interrupt. If that event is triggered, the DSP subsystem exits the power-down state but does not wake up.

5.4.4.6 INTC Basic Programming Model for Power On of DSP Subsystem

Programming model at boot time:

There is no specific software setting required to use combined/noncombined events during normal operation. However, at boot time, the event can be captured in the event-combiner event flag and not be propagated to the DSP. To do this, the following procedure must be performed:

1. The DSP subsystem logic ensures that interrupts are presented to the DSP megamodule only after:
   (a) The DSP megamodule module has its clock.
   (b) The DSP megamodule module is reset correctly.
2. From the time the pre-idle sequence is started to the time when the DSP subsystem context is fully restored and operational after wakeup, it is assumed that only external (from device peripherals) interrupts can occur. Internal interrupts in the DSP megamodule can result only from an application software side effect; the application is stopped when entering the pre-idle sequence and is restarted only after the DSP subsystem context is fully restored and operational. DMA interrupts are inactive at this stage, because the DMA_DSP module is completely reset after power up, and a software action is required to reactivate the DMA_DSP interrupts.
3. All device peripheral interrupts are level and are kept asserted until software acknowledges the interrupt by writing 1 to the interrupt status register (DSP_C0 CPU ISR) bit corresponding to the enabled asserted event(s). The device peripheral must keep an event flag to track missed interrupts. For a complete description of the DSP_C0 CPU ISR, see the C64x+ documents listed in Section 5.3.2.7, *Other DSP Reference Documents*.
4. There is no specific requirement to configure or restore interrupt mapping, except having the interrupts globally disabled during the sequence:
   (a) Set the DSP_C0 CPU TSR[0] or CSR[0] GIE bit to 0 to disable all interrupts except the reset interrupt and nonmaskable interrupt (NMI). The GIE bit is the same physical bit in the TSR and CSR. For a complete description of these registers, see the C64x + documents listed in Section 5.3.2.7, *Other DSP Reference Documents*.
   (b) Remap interrupts by configuring the SYS_INTC_INTMUXj registers (where j = 1 to 3).
   (c) Set the DSP_C0 CPU TSR[0] or CSR[0] GIE bit to 1 to enable all DSP_C0 CPU interrupts.

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The DSP_C0 CPU software recognizes which degree of power state the C64x reaches when executing the IDLE instruction, because the PRCM module is under C64x software control. Therefore, the DSP_C0 CPU software can correctly skip some unnecessary parts of the pre-idle routine.

State after reset for DSP_C0 CPU and INTC_DSP registers:

- The value of DSP_C0 CPU IER is 0x0.
- The value of DSP_C0 CPU IFR is 0x0 because the interrupt selector default mapping is routing only emulation and unmapped events.
- The SYS_INTC_INTMUXj registers (where j = 1 to 3): The default mapping is to route EVTx (where x = 0 to 3) on INTy (where y = 4 .. 15) (emulation and nonmapped events).
- The value of the SYS_INTC_EVTMASKi registers (where i = 0 to 3) is 0x0 (all events are unmasked). The values of these registers are don't care because of the default interrupt selector mapping (the SYS_INTC_INTMUXj registers (where j = 1 to 3).
- The SYS_INTC_EVTFLAGi registers (where i = 0 to 3): These registers log the possible wake-up interrupt(s) (if more than one). At this stage, a new wake-up interrupt from device peripherals cannot be missed, because interrupts are level in the device, waiting for a software acknowledge (the user must clear the interrupt in the module to deassert the interrupt line).

For a complete description of the DSP_C0 CPU IER and IFR, see the C64x+ documents listed in Section 5.3.2.7, *Other DSP Reference Documents*.

State after reset for the WUGEN_DSP registers (two cases depending on the reset type):

- In case of cold POR (the CORE power domain has been powered off), the value of the WUGEN_MEVT0 register is 0xFFFF FFFF, and the value of the WUGEN_MEVT1 register is 0xFFFF, meaning that all interrupts are masked.
- In case of warm POR (the CORE power domain was in ACTIVE state), the value of the WUGEN_MEVT0 and WUGEN_MEVT1 registers is the previous programmed one, enabling only wake-up interrupts.

Programming model for a correct warm-reset:

The user must replay the noncombined events required for wakeup (if any):

1. Globally mask interrupts by setting the DSP_C0 CPU TSR[0] or CSR[0] GIE bit to 0 (already done at boot time).
2. Restore the interrupt selector configuration:
   (a) SYS_INTC_INTMUXj register (where j = 1 to 3)
   (b) SYS_INTC_EVTMASKi register (optional, where i = 0 to 3)
   (c) SYS_INTC_INTDMASK register (optional)
3. Replay the noncombined event captured in SYS_INTC_EVTFLAGi (where i = 0 to 3):
   For each DSP_C0 CPU interrupt, i = 4 to 15:
   (a) Grab mapped event by setting the SYS_INTC_INTMUXj[6:0] INTSELi bit field (where j = 1 to 3).
   (b) Check whether the event is combined (EVT0...3) or not combined (EVT4...127).
   (c) If combined, exit the loop and go to the next loop iteration.
   (d) If noncombined:
      (i) Check whether the event is pending in the SYS_INTC_EVTFLAGi EFy bit (where i = 0 to 3, and y = 0 to 127).
      (ii) If not pending, exit the loop and go to the next loop iteration.
      (iii) If pending, set the associated IFi bit in the DSP_C0 CPU IFR.

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NOTE: Software must ensure that an event is enabled only once in the interrupt selector/combiner of the DSP megamodule. If a noncombined event is mapped to an enabled DSP_C0 CPU interrupt, the associated combined event is masked in the associated SYS_INTC_EVTMASKi register (where i = 0 to 3) (and/or the combined event is not mapped to the DSP_C0 CPU interrupt). Reciprocally, if a combined event is mapped to a DSP_C0 CPU interrupt, all unmasked events in the associated SYS_INTC_EVTMASKi register (where i = 0 to 3) are not mapped as noncombined events to an enabled DSP_C0 CPU interrupt (through the DSP_C0 CPU IER).

Software program example for Step 3:

```
/* ---------------------------------------------------- */
/* Replays IFR bits associated to noncombined events */
/* Assumes interrupts globally disabled (GIE bit set to 0)*/
/* Assumes SYS_INTC.INTMUXj() and SYS_INTC.EVTFLAGi() are */
/* access macros to DSP megamodule IC registers */
/* ---------------------------------------------------- */
myIPR = IPR; // save IPRfor(I=0; i<12; I++)
// for each CPU maskable interrupt{
myEvt = ( INTMUX( I >> 2 + 1) >> ( (I & 0x3) << 3 ) ) & 0x7F;
if(myEvt >= 4)
// noncombined event
{
if( (EVTFLAG(myEvt >> 5 ) >> (myEvt & 0x1F ) ) & 0x1 )
{
myIPR |= (1<<(I+4));
}
}}
IPR=myIPR;
// update IPR register
/* ---------------------------------------------------- */
/* Interrupts can be globally re-enabled from that point */
/* ---------------------------------------------------- */
```

4. Restore the CPU interrupt configuration by setting the DSP_C0 CPU IER accordingly.
5. Restore the DSP subsystem context (except saved return-PC).
6. Globally enable the interrupts by setting the DSP_C0 CPU TSR[0] or CSR[0] GIE bit to 1.
7. Branch to saved return-PC.

For a complete description of the DSP_C0 CPU TSR, CSR, IER, or IFR, see the C64x+ documents listed in Section 5.3.2.7, *Other DSP Reference Documents*.

Procedure for a cold reset:

1. Globally mask interrupts by setting the DSP_C0 CPU TSR[0] or CSR[0] GIE bit to 0 (already done at boot time).
2. Restore the interrupt selector configuration:
   (a) SYS_INTC_INTMUXj register (where j = 1 to 3)
   (b) SYS_INTC_EVTMASKi register (optional, where i = 0 to 3)
   (c) SYS_INTC_INTDMASK register (optional)
3. It is unnecessary to replay events, because they are masked in the WUGEN_MEVT0 and WUGEN_MEVT1 registers (default WUGEN_DSP configuration). This can be done to simplify the boot sequence without discriminating between cold reset and warm reset.
4. Restore the CPU interrupt configuration by setting the DSP_C0 CPU IER accordingly.
5. Restore the WUGEN_DSP context. This can be forced even in warm reset to simplify the boot sequence without discriminating between cold reset and warm reset.

NOTE: If Step 3 and Step 5 are performed systematically, the boot code can be shared between warm reset and cold reset boot without programming two distinct software boot codes.

6. Restore the rest of the DSP subsystem context (except saved return-PC).

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7. Globally enable the interrupts by setting the DSP_C0 CPU TSR[0] or CSR[0] GIE bit to 1.
8. Branch to saved return-PC.

5.4.5 Memory Management

5.4.5.1 External Memory

5.4.5.1.1 Cacheability

The SCACHE_CONFIG and SCACHE_OCP registers are used to configure the caches.

5.4.5.1.2 Virtual Addressing

The device embeds an instance of MMU dedicated to the DSP (MMU_DSP). For more information about MMU_DSP software settings at DSP boot, see Section 5.4.1.2, *Example of DSP Boot*.

For a programming guide of the MMU_DSP, see Chapter 20, *Memory Management Units*.

5.4.6 DSP Power Management

5.4.6.1 Clock Management

5.4.6.1.1 Clock Configuration

The DSP subsystem receives one single-clock signal (DSP_CLK) from the PRCM module.

From the DSP_GCLK functional clock, internal clocks (CD0_CLK and CD1_CLK) are generated by the DPLL_IVA and SYSC.

For a complete description of the PRCM module registers used to configure these clocks, see Section 3.6, *Clock Management Functional Description* in Chapter 3, *Power, Reset, and Clock Management*.

5.4.6.1.2 Clock Gating

- DSP subsystem:

  The DSP internal clocks can be hardware-disabled by the PRCM module when the MSTANDBY/WAIT handshake protocol occurs. To configure the PRCM module so that DSP internal clocks are hardware-supervised, set the corresponding PRCM.CM_AUTOIDLE_xxx bit field to 0x1.

  When the DSP subsystem does not require its internal clocks, they can be disabled at the PRCM module level by setting the corresponding PRCM.CM_FCLKEN_xxx bit field to 0.

  For a complete description of the PRCM module registers, see Chapter 3, *Power, Reset, and Clock Management*.
- SYSC module:

  The DSP SYSC module implements automatic clock gating on internal hardware detection of the absence of activity. The transition from clock-gated to clock-nongated state operates with no penalty for cycle latency.

  Automatic clock-gating is enabled by setting the SYSC_SYSCONFIG[0] AUTOIDLE bit to 1 (default value). This feature can be disabled by setting the SYSC_SYSCONFIG[0] AUTOIDLE bit to 0, which makes the clock free-running.
- WUGEN_DSP module:

  The DSP WUGEN module implements automatic clock gating on internal hardware detection of the absence of activity. The transition from clock-gated to clock-nongated state operates with no penalty for cycle latency.

  Automatic clock gating is enabled by setting the WUGEN_SYSCONFIG[0] AUTOIDLE bit to 1 (default value). The clock can be made free-running by setting the WUGEN_SYSCONFIG[0] AUTOIDLE bit to 0.
- TPCC from the DMA_DSP module:

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The DMA_DSP (or TPCC) module implements automatic clock gating on internal hardware detection of the absence of activity. The transition from clock-nongated to clock-gated state operates with no penalty for cycle latency.

Automatic clock gating is enabled by default. It can be disabled by setting the TPCC_CLKGDIS[0] CLKGDIS bit to 1. In this case, all TPCC internal clocks are free-running.

NOTE: To save power, it is recommended to not disable TPCC clock gating and to leave the TPCC_CLKGDIS register at its reset value.

5.4.6.2 Reset Management

In addition to hardware reset signals generated by the PRCM module, the DSP subsystem can be reset by software control.

For a complete description of the PRCM module registers, see Section 3.5.4, *Reset Domains*, in Chapter 3, *Power, Reset, and Clock Management*.

NOTE: Software reset can be applied only while the DSP subsystem is in clock-off mode.

5.4.6.3 Power Down and Wakeup Management

- DSP megamodule power-down controller (PDC):

  The DSP megamodule embeds a PDC block that allows power-down management by software. Individual DSP megamodule blocks such as DSP_C0 CPU, PMC, DMC, EMC, and shared cache can be powered off by the PDC.
- This software control is ensured by the SYS_PD_PDCCMD register:
  - By setting the SYS_PD_PDCCMD[16] GEMPD bit to 1, the user enables power-down management during idle mode.
  - By setting the SYS_PD_PDCCMD[1:0] xMCLOG and SYS_PD_PDCCMD[1:0] xMCMEM bit fields (where x = {P, D, U}), the user controls the XMC clock-gating and standby memory modes. For example, DMC is controlled with the SYS_PD_PDCCMD[5:4] DMCLOG and SYS_PD_PDCCMD[7:6] xMCMEM bit fields.
- The programming sequence for transition to clock-off state is:

  Before executing the IDLE instruction, the following sequence must be performed:

  1. Write 1 to the SYS_PD_PDCCMD[16] GEMPD bit (STANDBY state); by default, the values of the SYS_PD_PDCCMD[1:0] xMCLOG and SYS_PD_PDCCMD[1:0] xMCMEM bit fields (where x = {P, D, U}) are 0x1 so that module clock gating is enabled and the standby mode of memories is statically activated after the IDLE instruction executes.
  2. Mask all interrupts not intended to wake up the DSP subsystem.
  3. Program the PRCM module so that the DSP clocks are cut on DSP standby. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management* in Chapter 3, *Power, Reset, and Clock Management*
  4. Read back all the written registers to ensure write completion.
  5. Confirm that no user-initiated cache coherence operations are in progress.
  6. Ensure that the IDLE code sequence is in L1 or L2.

  The user must also ensure that no other instruction is executed parallel to the IDLE instruction.

5.4.7 Error Identification Process

Several mechanisms are available in the DSP subsystem to report errors at different levels.

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5.4.7.1 Error Reporting for DSP DMA

The TPTC and TPCC blocks of the DMA_DSP module also contain registers to inform the user of a problem during DSP external DMA communication.

TPCC block

The TPCC provides one error interrupt output, CCERRINT (EVT38; see Table 5-6), which consolidates the following error conditions:

- QDMA missed events (stored in the TPCC_QEMR)
- DMA missed events (stored in the TPCC_EMR)
- Transfer completion code error (stored in the TPCC_CCERR[16] TCCERR bit)
- Queue threshold error events (stored in the TPCC_CCERR[n] QTHRXCDn bit, where n = 0, 1)

When an error is detected, the CCERRINT event is asserted, because error events do not have enables.

NOTE: The CCERRINT event follows the same convention as other TPCC interrupt outputs. When the error interrupt condition transitions from a no-errors-are-set state to at least one error set, the error output (CCERRINT) pulses high for one TPCC clock cycle. If additional errors are latched before the original error is cleared by the user, the TPCC does not generate additional interrupt pulses. Software must poll all bits during execution of the ISR and clear all error conditions so that subsequent error pulses can be generated by the TPCC block.

Error interrupts can be set and/or reevaluated by writes to the TPCC_EEVAL register.

TPTC block

Each TPTC can also detect several error conditions:

- Read status or write status errors in the TPTC_ERRSTAT[0] BUSERR bit
- TR error in the TPTC_ERRSTAT[2] TRERR bit
- MMR address error in the TPTC_ERRSTAT[3] MMRAERR bit

Errors are recorded in the TPTC_ERRSTAT register, regardless of whether they are enabled. They can be cleared from the TPTC_ERRSTAT register only by writing 1 to the corresponding bit of the TPTC_ERRCLR register.

The error details register (TPTC_ERRDET) contains additional information about the first read status error or write status error detected. Future errors are bit-recorded until the TPTC_ERRDET register is cleared.

If read status and write status are returned to the TPTC in the same cycle, the value of the read or write status that has an error (nonzero) is latched in the TPTC_ERRDET register, and the TPTC_ERRSTAT[0] BUSERR bit is set. If both the read and write status are nonzero, the write status is given priority for setting the TPTC_ERRDET register. The TPTC_ERRDET register is cleared by setting the TPTC_ERRCLR[0] BUSERR bit to 1.

If an error is enabled (by the TPTC_ERREN register), the first occurrence of an enabled error generates a pulsed interrupt to the CPU by the TCERRINT event output (TCERRINT0 with EVT39 for TPTG0, and TCERRINT1 with EVT40 for TPTG1, respectively; see Table 5-6). Subsequent errors do not generate a new pulse until all accumulated errors are cleared by the CPU. The CPU clears bits in the TPTC_INTSTAT register by writing 1 to the corresponding bit(s) of the TPTC_INTCLR register.

5.4.7.2 Error Reporting for the L3_MAIN Interconnect

L3_MAIN interconnect out-of-band errors are also reported by the external L3_MAIN interrupt signal. This signal corresponds to the EVT84 event and is directly connected to the DSP_nIRQ[39] DSP_C0 CPU interrupt line. For more information about L3_MAIN interconnect error reporting, see Section 14.2, *L3 Interconnect* in Chapter 14, *Interconnect*.

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5.5 DSP Subsystem Register Manual

5.5.1 DSP Subsystem Instance Summary

Table 5-8. DSP Subsystem Instance Summary

Module Name	Physical Address	Size
INTC_DSP	0x0180 0000	64KiB
PDC	0x0181 0000	4KiB
EDM	0x01BC 0000	4KiB
TPCC	0x01C0 0000	64KiB
TPTC0	0x01C1 0000	1KiB
TPTC1	0x01C1 0400	1KiB
SYSC	0x01C2 0000	4KiB
WUGEN_DSP	0x01C2 1000	4KiB
L1_SCACHE	0x01C3 0000	256 bytes
L2_SCACHE	0x01C3 0200	256 bytes
SCACHE_SCTM	0x01C3 0400	512 bytes
SCACHE_MMU_DSP	0x01C3 0800	2KiB

CAUTION

The SCACHE_MMU_DSP registers are limited to 32-bit data access; 16- and 8-bit access are not allowed and can corrupt register content.

5.5.2 DSP Subsystem Logical Register Mapping

Table 5-9. SYS_INTC_EVTFLAGi Logical Register Mapping

Hardware Register
SYS_INTC_EVTFLAG0
SYS_INTC_EVTFLAG1
SYS_INTC_EVTFLAG2
SYS_INTC_EVTFLAG3

Table 5-10. SYS_INTC_EVTMASKi Logical Register Mapping

Hardware Register
SYS_INTC_EVTMASK0
SYS_INTC_EVTMASK1
SYS_INTC_EVTMASK2
SYS_INTC_EVTMASK3

Table 5-11. SYS_INTC_EVTCLRi Logical Register Mapping

Hardware Register
SYS_INTC_EVTCLR0
SYS_INTC_EVTCLR1
SYS_INTC_EVTCLR2
SYS_INTC_EVTCLR3

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Table 5-12. SYS_INTC_EVTSETi Logical Register Mapping

Hardware Register
SYS_INTC_EVTSET0
SYS_INTC_EVTSET1
SYS_INTC_EVTSET2
SYS_INTC_EVTSET3

Table 5-13. SYS_INTC_INTMUXj Logical Register Mapping

Hardware Register
SYS_INTC_INTMUX1
SYS_INTC_INTMUX2
SYS_INTC_INTMUX3

5.5.3 INTC_DSP Registers

5.5.3.1 INTC_DSP Register Summary

Table 5-14. INTC_DSP Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	INTC_DSP Physical Address
SYS_INTC_EVTFLAG0	R	32	0x0000 0000	0x0180 0000
SYS_INTC_EVTFLAG1	R	32	0x0000 0004	0x0180 0004
SYS_INTC_EVTFLAG2	R	32	0x0000 0008	0x0180 0008
SYS_INTC_EVTFLAG3	R	32	0x0000 000C	0x0180 000C
SYS_INTC_EVTSET0	W	32	0x0000 0020	0x0180 0020
SYS_INTC_EVTSET1	W	32	0x0000 0024	0x0180 0024
SYS_INTC_EVTSET2	W	32	0x0000 0028	0x0180 0028
SYS_INTC_EVTSET3	W	32	0x0000 002C	0x0180 002C
SYS_INTC_EVTCLR0	W	32	0x0000 0040	0x0180 0040
SYS_INTC_EVTCLR1	W	32	0x0000 0044	0x0180 0044
SYS_INTC_EVTCLR2	W	32	0x0000 0048	0x0180 0048
SYS_INTC_EVTCLR3	W	32	0x0000 004C	0x0180 004C
SYS_INTC_EVTMASK0	RW	32	0x0000 0080	0x0180 0080
SYS_INTC_EVTMASK1	RW	32	0x0000 0084	0x0180 0084
SYS_INTC_EVTMASK2	RW	32	0x0000 0088	0x0180 0088
SYS_INTC_EVTMASK3	RW	32	0x0000 008C	0x0180 008C
SYS_INTC_MEVTFLAG0	R	32	0x0000 00A0	0x0180 00A0
SYS_INTC_MEVTFLAG1	R	32	0x0000 00A4	0x0180 00A4
SYS_INTC_MEVTFLAG2	R	32	0x0000 00A8	0x0180 00A8
SYS_INTC_MEVTFLAG3	R	32	0x0000 00AC	0x0180 00AC
SYS_INTC_EXPMASK0	RW	32	0x0000 00C0	0x0180 00C0
SYS_INTC_EXPMASK1	RW	32	0x0000 00C4	0x0180 00C4
SYS_INTC_EXPMASK2	RW	32	0x0000 00C8	0x0180 00C8
SYS_INTC_EXPMASK3	RW	32	0x0000 00CC	0x0180 00CC
SYS_INTC_MEXPFLAG0	R	32	0x0000 00E0	0x0180 00E0
SYS_INTC_MEXPFLAG1	R	32	0x0000 00E4	0x0180 00E4
SYS_INTC_MEXPFLAG2	R	32	0x0000 00E8	0x0180 00E8
SYS_INTC_MEXPFLAG3	R	32	0x0000 00EC	0x0180 00EC
SYS_INTC_INTMUX1	RW	32	0x0000 0104	0x0180 0104

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Table 5-14. INTC_DSP Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	INTC_DSP Physical Address
SYS_INTC_INTMUX2	RW	32	0x0000 0108	0x0180 0108
SYS_INTC_INTMUX3	RW	32	0x0000 010C	0x0180 010C
SYS_INTC_AEGMUX0	RW	32	0x0000 0140	0x0180 0140
SYS_INTC_AEGMUX1	RW	32	0x0000 0144	0x0180 0144
SYS_INTC_INTXSTAT	R	32	0x0000 0180	0x0180 0180
SYS_INTC_INTXCLR	W	32	0x0000 0184	0x0180 0184
SYS_INTC_INTDMASK	RW	32	0x0000 0188	0x0180 0188
SYS_INTC_EVTASRT	W	32	0x0000 01C0	0x0180 01C0

5.5.3.2 INTC_DSP Register Description

Table 5-15. SYS_INTC_EVTFLAG0

Address Offset	0x0000 0000		
Physical Address	0x0180 0000	**Instance**	INTC_DSP
Description	Event Flag Register 0		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EF31	EF30	EF29	EF28	EF27	EF26	EF25	EF24	EF23	EF22	EF21	EF20	EF19	EF18	EF17	EF16	EF15	EF14	EF13	EF12	EF11	EF10	EF9	EF8	EF7	EF6	EF5	EF4	EF3	EF2	EF1	EF0

Bits	Field Name	Description	Type	Reset
31	EF31	Event Flag number 31 0: no event occurred 1: an event occurred	R	0
30	EF30	Event Flag number 30 0: no event occurred 1: an event occurred	R	0
29	EF29	Event Flag number 29 0: no event occurred 1: an event occurred	R	0
28	EF28	Event Flag number 28 0: no event occurred 1: an event occurred	R	0
27	EF27	Event Flag number 27 0: no event occurred 1: an event occurred	R	0
26	EF26	Event Flag number 26 0: no event occurred 1: an event occurred	R	0
25	EF25	Event Flag number 25 0: no event occurred 1: an event occurred	R	0
24	EF24	Event Flag number 24 0: no event occurred 1: an event occurred	R	0
23	EF23	Event Flag number 23 0: no event occurred 1: an event occurred	R	0
22	EF22	Event Flag number 22 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
21	EF21	Event Flag number 21 0: no event occurred 1: an event occurred	R	0
20	EF20	Event Flag number 20 0: no event occurred 1: an event occurred	R	0
19	EF19	Event Flag number 19 0: no event occurred 1: an event occurred	R	0
18	EF18	Event Flag number 18 0: no event occurred 1: an event occurred	R	0
17	EF17	Event Flag number 17 0: no event occurred 1: an event occurred	R	0
16	EF16	Event Flag number 16 0: no event occurred 1: an event occurred	R	0
15	EF15	Event Flag number 15 0: no event occurred 1: an event occurred	R	0
14	EF14	Event Flag number 14 0: no event occurred 1: an event occurred	R	0
13	EF13	Event Flag number 13 0: no event occurred 1: an event occurred	R	0
12	EF12	Event Flag number 12 0: no event occurred 1: an event occurred	R	0
11	EF11	Event Flag number 11 0: no event occurred 1: an event occurred	R	0
10	EF10	Event Flag number 10 0: no event occurred 1: an event occurred	R	0
9	EF9	Event Flag number 9 0: no event occurred 1: an event occurred	R	0
8	EF8	Event Flag number 8 0: no event occurred 1: an event occurred	R	0
7	EF7	Event Flag number 7 0: no event occurred 1: an event occurred	R	0
6	EF6	Event Flag number 6 0: no event occurred 1: an event occurred	R	0
5	EF5	Event Flag number 5 0: no event occurred 1: an event occurred	R	0
4	EF4	Event Flag number 4 0: no event occurred 1: an event occurred	R	0
3	EF3	Event Flag number 3 0: no event occurred 1: an event occurred	R	0
2	EF2	Event Flag number 2 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
1	EF1	Event Flag number 1 0: no event occurred 1: an event occurred	R	0
0	EF0	Event Flag number 0 0: no event occurred 1: an event occurred	R	0

Table 5-16. Register Call Summary for Register SYS_INTC_EVTFLAG0

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- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-17. SYS_INTC_EVTFLAG1

Address Offset	0x0000 0004		
Physical Address	0x0180 0004	**Instance**	INTC_DSP
Description	Event Flag Register 1		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EF63	EF62	EF61	EF60	EF59	EF58	EF57	EF56	EF55	EF54	EF53	EF52	EF51	EF50	EF49	EF48	EF47	EF46	EF45	EF44	EF43	EF42	EF41	EF40	EF39	EF38	EF37	EF36	EF35	EF34	EF33	EF32

Bits	Field Name	Description	Type	Reset
31	EF63	Event Flag number 63 0: no event occurred 1: an event occurred	R	0
30	EF62	Event Flag number 62 0: no event occurred 1: an event occurred	R	0
29	EF61	Event Flag number 61 0: no event occurred 1: an event occurred	R	0
28	EF60	Event Flag number 60 0: no event occurred 1: an event occurred	R	0
27	EF59	Event Flag number 59 0: no event occurred 1: an event occurred	R	0
26	EF58	Event Flag number 58 0: no event occurred 1: an event occurred	R	0
25	EF57	Event Flag number 57 0: no event occurred 1: an event occurred	R	0
24	EF56	Event Flag number 56 0: no event occurred 1: an event occurred	R	0
23	EF55	Event Flag number 55 0: no event occurred 1: an event occurred	R	0
22	EF54	Event Flag number 54 0: no event occurred 1: an event occurred	R	0
21	EF53	Event Flag number 53 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
20	EF52	Event Flag number 52 0: no event occurred 1: an event occurred	R	0
19	EF51	Event Flag number 51 0: no event occurred 1: an event occurred	R	0
18	EF50	Event Flag number 50 0: no event occurred 1: an event occurred	R	0
17	EF49	Event Flag number 49 0: no event occurred 1: an event occurred	R	0
16	EF48	Event Flag number 48 0: no event occurred 1: an event occurred	R	0
15	EF47	Event Flag number 47 0: no event occurred 1: an event occurred	R	0
14	EF46	Event Flag number 46 0: no event occurred 1: an event occurred	R	0
13	EF45	Event Flag number 45 0: no event occurred 1: an event occurred	R	0
12	EF44	Event Flag number 44 0: no event occurred 1: an event occurred	R	0
11	EF43	Event Flag number 43 0: no event occurred 1: an event occurred	R	0
10	EF42	Event Flag number 42 0: no event occurred 1: an event occurred	R	0
9	EF41	Event Flag number 41 0: no event occurred 1: an event occurred	R	0
8	EF40	Event Flag number 40 0: no event occurred 1: an event occurred	R	0
7	EF39	Event Flag number 39 0: no event occurred 1: an event occurred	R	0
6	EF38	Event Flag number 38 0: no event occurred 1: an event occurred	R	0
5	EF37	Event Flag number 37 0: no event occurred 1: an event occurred	R	0
4	EF36	Event Flag number 36 0: no event occurred 1: an event occurred	R	0
3	EF35	Event Flag number 35 0: no event occurred 1: an event occurred	R	0
2	EF34	Event Flag number 34 0: no event occurred 1: an event occurred	R	0
1	EF33	Event Flag number 33 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
0	EF32	Event Flag number 32 0: no event occurred 1: an event occurred	R	0

Table 5-18. Register Call Summary for Register SYS_INTC_EVTFLAG1

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-19. SYS_INTC_EVTFLAG2

Address Offset	0x0000 0008		
Physical Address	0x0180 0008	**Instance**	INTC_DSP
Description	Event Flag Register 2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EF95	EF94	EF93	EF92	EF91	EF90	EF89	EF88	EF87	EF86	EF85	EF84	EF83	EF82	EF81	EF80	EF79	EF78	EF77	EF76	EF75	EF74	EF73	EF72	EF71	EF70	EF69	EF68	EF67	EF66	EF65	EF64

Bits	Field Name	Description	Type	Reset
31	EF95	Event Flag number 95 0: no event occurred 1: an event occurred	R	0
30	EF94	Event Flag number 94 0: no event occurred 1: an event occurred	R	0
29	EF93	Event Flag number 93 0: no event occurred 1: an event occurred	R	0
28	EF92	Event Flag number 92 0: no event occurred 1: an event occurred	R	0
27	EF91	Event Flag number 91 0: no event occurred 1: an event occurred	R	0
26	EF90	Event Flag number 90 0: no event occurred 1: an event occurred	R	0
25	EF89	Event Flag number 89 0: no event occurred 1: an event occurred	R	0
24	EF88	Event Flag number 88 0: no event occurred 1: an event occurred	R	0
23	EF87	Event Flag number 87 0: no event occurred 1: an event occurred	R	0
22	EF86	Event Flag number 86 0: no event occurred 1: an event occurred	R	0
21	EF85	Event Flag number 85 0: no event occurred 1: an event occurred	R	0
20	EF84	Event Flag number 84 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
19	EF83	Event Flag number 83 0: no event occurred 1: an event occurred	R	0
18	EF82	Event Flag number 82 0: no event occurred 1: an event occurred	R	0
17	EF81	Event Flag number 81 0: no event occurred 1: an event occurred	R	0
16	EF80	Event Flag number 80 0: no event occurred 1: an event occurred	R	0
15	EF79	Event Flag number 79 0: no event occurred 1: an event occurred	R	0
14	EF78	Event Flag number 78 0: no event occurred 1: an event occurred	R	0
13	EF77	Event Flag number 77 0: no event occurred 1: an event occurred	R	0
12	EF76	Event Flag number 76 0: no event occurred 1: an event occurred	R	0
11	EF75	Event Flag number 75 0: no event occurred 1: an event occurred	R	0
10	EF74	Event Flag number 74 0: no event occurred 1: an event occurred	R	0
9	EF73	Event Flag number 73 0: no event occurred 1: an event occurred	R	0
8	EF72	Event Flag number 72 0: no event occurred 1: an event occurred	R	0
7	EF71	Event Flag number 71 0: no event occurred 1: an event occurred	R	0
6	EF70	Event Flag number 70 0: no event occurred 1: an event occurred	R	0
5	EF69	Event Flag number 69 0: no event occurred 1: an event occurred	R	0
4	EF68	Event Flag number 68 0: no event occurred 1: an event occurred	R	0
3	EF67	Event Flag number 67 0: no event occurred 1: an event occurred	R	0
2	EF66	Event Flag number 66 0: no event occurred 1: an event occurred	R	0
1	EF65	Event Flag number 65 0: no event occurred 1: an event occurred	R	0
0	EF64	Event Flag number 64 0: no event occurred 1: an event occurred	R	0

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Table 5-20. Register Call Summary for Register SYS_INTC_EVTFLAG2

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- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-21. SYS_INTC_EVTFLAG3

Address Offset	0x0000 000C		
Physical Address	0x0180 000C	**Instance**	INTC_DSP
Description	Event Flag Register 3		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EF127	EF126	EF125	EF124	EF123	EF122	EF121	EF120	EF119	EF118	EF117	EF116	EF115	EF114	EF113	EF112	EF111	EF110	EF109	EF108	EF107	EF106	EF105	EF104	EF103	EF102	EF101	EF100	EF99	EF98	EF97	EF96

Bits	Field Name	Description	Type	Reset
31	EF127	Event Flag number 127 0: no event occurred 1: an event occurred	R	0
30	EF126	Event Flag number 126 0: no event occurred 1: an event occurred	R	0
29	EF125	Event Flag number 125 0: no event occurred 1: an event occurred	R	0
28	EF124	Event Flag number 124 0: no event occurred 1: an event occurred	R	0
27	EF123	Event Flag number 123 0: no event occurred 1: an event occurred	R	0
26	EF122	Event Flag number 122 0: no event occurred 1: an event occurred	R	0
25	EF121	Event Flag number 121 0: no event occurred 1: an event occurred	R	0
24	EF120	Event Flag number 120 0: no event occurred 1: an event occurred	R	0
23	EF119	Event Flag number 119 0: no event occurred 1: an event occurred	R	0
22	EF118	Event Flag number 118 0: no event occurred 1: an event occurred	R	0
21	EF117	Event Flag number 117 0: no event occurred 1: an event occurred	R	0
20	EF116	Event Flag number 116 0: no event occurred 1: an event occurred	R	0
19	EF115	Event Flag number 115 0: no event occurred 1: an event occurred	R	0
18	EF114	Event Flag number 114 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
17	EF113	Event Flag number 113 0: no event occurred 1: an event occurred	R	0
16	EF112	Event Flag number 112 0: no event occurred 1: an event occurred	R	0
15	EF111	Event Flag number 111 0: no event occurred 1: an event occurred	R	0
14	EF110	Event Flag number 110 0: no event occurred 1: an event occurred	R	0
13	EF109	Event Flag number 109 0: no event occurred 1: an event occurred	R	0
12	EF108	Event Flag number 108 0: no event occurred 1: an event occurred	R	0
11	EF107	Event Flag number 107 0: no event occurred 1: an event occurred	R	0
10	EF106	Event Flag number 106 0: no event occurred 1: an event occurred	R	0
9	EF105	Event Flag number 105 0: no event occurred 1: an event occurred	R	0
8	EF104	Event Flag number 104 0: no event occurred 1: an event occurred	R	0
7	EF103	Event Flag number 103 0: no event occurred 1: an event occurred	R	0
6	EF102	Event Flag number 102 0: no event occurred 1: an event occurred	R	0
5	EF101	Event Flag number 101 0: no event occurred 1: an event occurred	R	0
4	EF100	Event Flag number 100 0: no event occurred 1: an event occurred	R	0
3	EF99	Event Flag number 99 0: no event occurred 1: an event occurred	R	0
2	EF98	Event Flag number 98 0: no event occurred 1: an event occurred	R	0
1	EF97	Event Flag number 97 0: no event occurred 1: an event occurred	R	0
0	EF96	Event Flag number 96 0: no event occurred 1: an event occurred	R	0

Table 5-22. Register Call Summary for Register SYS_INTC_EVTFLAG3

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

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Table 5-23. SYS_INTC_EVTSET0

Address Offset	0x0000 0020		
Physical Address	0x0180 0020	**Instance**	INTC_DSP
Description	Event Set Register 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ES31	ES30	ES29	ES28	ES27	ES26	ES25	ES24	ES23	ES22	ES21	ES20	ES19	ES18	ES17	ES16	ES15	ES14	ES13	ES12	ES11	ES10	ES9	ES8	ES7	ES6	ES5	ES4	ES3	ES2	ES1	ES0

Bits	Field Name	Description	Type	Reset
31	ES31	Event Set number 31 write 0: no action write 1: set corresponding event flag	W	0
30	ES30	Event Set number 30 write 0: no action write 1: set corresponding event flag	W	0
29	ES29	Event Set number 29 write 0: no action write 1: set corresponding event flag	W	0
28	ES28	Event Set number 28 write 0: no action write 1: set corresponding event flag	W	0
27	ES27	Event Set number 27 write 0: no action write 1: set corresponding event flag	W	0
26	ES26	Event Set number 26 write 0: no action write 1: set corresponding event flag	W	0
25	ES25	Event Set number 25 write 0: no action write 1: set corresponding event flag	W	0
24	ES24	Event Set number 24 write 0: no action write 1: set corresponding event flag	W	0
23	ES23	Event Set number 23 write 0: no action write 1: set corresponding event flag	W	0
22	ES22	Event Set number 22 write 0: no action write 1: set corresponding event flag	W	0
21	ES21	Event Set number 21 write 0: no action write 1: set corresponding event flag	W	0
20	ES20	Event Set number 20 write 0: no action write 1: set corresponding event flag	W	0
19	ES19	Event Set number 19 write 0: no action write 1: set corresponding event flag	W	0
18	ES18	Event Set number 18 write 0: no action write 1: set corresponding event flag	W	0
17	ES17	Event Set number 17 write 0: no action write 1: set corresponding event flag	W	0
16	ES16	Event Set number 16 write 0: no action write 1: set corresponding event flag	W	0

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Bits	Field Name	Description	Type	Reset
15	ES15	Event Set number 15 write 0: no action write 1: set corresponding event flag	W	0
14	ES14	Event Set number 14 write 0: no action write 1: set corresponding event flag	W	0
13	ES13	Event Set number 13 write 0: no action write 1: set corresponding event flag	W	0
12	ES12	Event Set number 12 write 0: no action write 1: set corresponding event flag	W	0
11	ES11	Event Set number 11 write 0: no action write 1: set corresponding event flag	W	0
10	ES10	Event Set number 10 write 0: no action write 1: set corresponding event flag	W	0
9	ES9	Event Set number 9 write 0: no action write 1: set corresponding event flag	W	0
8	ES8	Event Set number 8 write 0: no action write 1: set corresponding event flag	W	0
7	ES7	Event Set number 7 write 0: no action write 1: set corresponding event flag	W	0
6	ES6	Event Set number 6 write 0: no action write 1: set corresponding event flag	W	0
5	ES5	Event Set number 5 write 0: no action write 1: set corresponding event flag	W	0
4	ES4	Event Set number 4 write 0: no action write 1: set corresponding event flag	W	0
3	ES3	Event Set number 3 write 0: no action write 1: set corresponding event flag	W	0
2	ES2	Event Set number 2 write 0: no action write 1: set corresponding event flag	W	0
1	ES1	Event Set number 1 write 0: no action write 1: set corresponding event flag	W	0
0	ES0	Event Set number 0 write 0: no action write 1: set corresponding event flag	W	0

Table 5-24. Register Call Summary for Register SYS_INTC_EVTSET0

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-25. SYS_INTC_EVTSET1

Address Offset	0x0000 0024		
Physical Address	0x0180 0024	**Instance**	INTC_DSP
Description	Event Set Register 1		
Type	W		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ES63	ES62	ES61	ES60	ES59	ES58	ES57	ES56	ES55	ES54	ES53	ES52	ES51	ES50	ES49	ES48	ES47	ES46	ES45	ES44	ES43	ES42	ES41	ES40	ES39	ES38	ES37	ES36	ES35	ES34	ES33	ES32

Bits	Field Name	Description	Type	Reset
31	ES63	Event Set number 63 write 0: no action write 1: set corresponding event flag	W	0
30	ES62	Event Set number 62 write 0: no action write 1: set corresponding event flag	W	0
29	ES61	Event Set number 61 write 0: no action write 1: set corresponding event flag	W	0
28	ES60	Event Set number 60 write 0: no action write 1: set corresponding event flag	W	0
27	ES59	Event Set number 59 write 0: no action write 1: set corresponding event flag	W	0
26	ES58	Event Set number 58 write 0: no action write 1: set corresponding event flag	W	0
25	ES57	Event Set number 57 write 0: no action write 1: set corresponding event flag	W	0
24	ES56	Event Set number 56 write 0: no action write 1: set corresponding event flag	W	0
23	ES55	Event Set number 55 write 0: no action write 1: set corresponding event flag	W	0
22	ES54	Event Set number 54 write 0: no action write 1: set corresponding event flag	W	0
21	ES53	Event Set number 53 write 0: no action write 1: set corresponding event flag	W	0
20	ES52	Event Set number 52 write 0: no action write 1: set corresponding event flag	W	0
19	ES51	Event Set number 51 write 0: no action write 1: set corresponding event flag	W	0
18	ES50	Event Set number 50 write 0: no action write 1: set corresponding event flag	W	0
17	ES49	Event Set number 49 write 0: no action write 1: set corresponding event flag	W	0
16	ES48	Event Set number 48 write 0: no action write 1: set corresponding event flag	W	0
15	ES47	Event Set number 47 write 0: no action write 1: set corresponding event flag	W	0
14	ES46	Event Set number 46 write 0: no action write 1: set corresponding event flag	W	0
13	ES45	Event Set number 45 write 0: no action write 1: set corresponding event flag	W	0

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Bits	Field Name	Description	Type	Reset
12	ES44	Event Set number 44 write 0: no action write 1: set corresponding event flag	W	0
11	ES43	Event Set number 43 write 0: no action write 1: set corresponding event flag	W	0
10	ES42	Event Set number 42 write 0: no action write 1: set corresponding event flag	W	0
9	ES41	Event Set number 41 write 0: no action write 1: set corresponding event flag	W	0
8	ES40	Event Set number 40 write 0: no action write 1: set corresponding event flag	W	0
7	ES39	Event Set number 39 write 0: no action write 1: set corresponding event flag	W	0
6	ES38	Event Set number 38 write 0: no action write 1: set corresponding event flag	W	0
5	ES37	Event Set number 37 write 0: no action write 1: set corresponding event flag	W	0
4	ES36	Event Set number 36 write 0: no action write 1: set corresponding event flag	W	0
3	ES35	Event Set number 35 write 0: no action write 1: set corresponding event flag	W	0
2	ES34	Event Set number 34 write 0: no action write 1: set corresponding event flag	W	0
1	ES33	Event Set number 33 write 0: no action write 1: set corresponding event flag	W	0
0	ES32	Event Set number 32 write 0: no action write 1: set corresponding event flag	W	0

Table 5-26. Register Call Summary for Register SYS_INTC_EVTSET1

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-27. SYS_INTC_EVTSET2

Address Offset	0x0000 0028		
Physical Address	0x0180 0028	**Instance**	INTC_DSP
Description	Event Set Register 2		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ES95	ES94	ES93	ES92	ES91	ES90	ES89	ES88	ES87	ES86	ES85	ES84	ES83	ES82	ES81	ES80	ES79	ES78	ES77	ES76	ES75	ES74	ES73	ES72	ES71	ES70	ES69	ES68	ES67	ES66	ES65	ES64

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Bits	Field Name	Description	Type	Reset
31	ES95	Event Set number 95 write 0: no action write 1: set corresponding event flag	W	0
30	ES94	Event Set number 94 write 0: no action write 1: set corresponding event flag	W	0
29	ES93	Event Set number 93 write 0: no action write 1: set corresponding event flag	W	0
28	ES92	Event Set number 92 write 0: no action write 1: set corresponding event flag	W	0
27	ES91	Event Set number 91 write 0: no action write 1: set corresponding event flag	W	0
26	ES90	Event Set number 90 write 0: no action write 1: set corresponding event flag	W	0
25	ES89	Event Set number 89 write 0: no action write 1: set corresponding event flag	W	0
24	ES88	Event Set number 88 write 0: no action write 1: set corresponding event flag	W	0
23	ES87	Event Set number 87 write 0: no action write 1: set corresponding event flag	W	0
22	ES86	Event Set number 86 write 0: no action write 1: set corresponding event flag	W	0
21	ES85	Event Set number 85 write 0: no action write 1: set corresponding event flag	W	0
20	ES84	Event Set number 84 write 0: no action write 1: set corresponding event flag	W	0
19	ES83	Event Set number 83 write 0: no action write 1: set corresponding event flag	W	0
18	ES82	Event Set number 82 write 0: no action write 1: set corresponding event flag	W	0
17	ES81	Event Set number 81 write 0: no action write 1: set corresponding event flag	W	0
16	ES80	Event Set number 80 write 0: no action write 1: set corresponding event flag	W	0
15	ES79	Event Set number 79 write 0: no action write 1: set corresponding event flag	W	0
14	ES78	Event Set number 78 write 0: no action write 1: set corresponding event flag	W	0
13	ES77	Event Set number 77 write 0: no action write 1: set corresponding event flag	W	0
12	ES76	Event Set number 76 write 0: no action write 1: set corresponding event flag	W	0

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Bits	Field Name	Description	Type	Reset
11	ES75	Event Set number 75 write 0: no action write 1: set corresponding event flag	W	0
10	ES74	Event Set number 74 write 0: no action write 1: set corresponding event flag	W	0
9	ES73	Event Set number 73 write 0: no action write 1: set corresponding event flag	W	0
8	ES72	Event Set number 72 write 0: no action write 1: set corresponding event flag	W	0
7	ES71	Event Set number 71 write 0: no action write 1: set corresponding event flag	W	0
6	ES70	Event Set number 70 write 0: no action write 1: set corresponding event flag	W	0
5	ES69	Event Set number 69 write 0: no action write 1: set corresponding event flag	W	0
4	ES68	Event Set number 68 write 0: no action write 1: set corresponding event flag	W	0
3	ES67	Event Set number 67 write 0: no action write 1: set corresponding event flag	W	0
2	ES66	Event Set number 66 write 0: no action write 1: set corresponding event flag	W	0
1	ES65	Event Set number 65 write 0: no action write 1: set corresponding event flag	W	0
0	ES64	Event Set number 64 write 0: no action write 1: set corresponding event flag	W	0

Table 5-28. Register Call Summary for Register SYS_INTC_EVTSET2

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-29. SYS_INTC_EVTSET3

Address Offset	0x0000 002C		
Physical Address	0x0180 002C	**Instance**	INTC_DSP
Description	Event Set Register 3		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ES127	ES126	ES125	ES124	ES123	ES122	ES121	ES120	ES119	ES118	ES117	ES116	ES115	ES114	ES113	ES112	ES111	ES110	ES109	ES108	ES107	ES106	ES105	ES104	ES103	ES102	ES101	ES100	ES99	ES98	ES97	ES96

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Bits	Field Name	Description	Type	Reset
31	ES127	Event Set number 127 write 0: no action write 1: set corresponding event flag	W	0
30	ES126	Event Set number 126 write 0: no action write 1: set corresponding event flag	W	0
29	ES125	Event Set number 125 write 0: no action write 1: set corresponding event flag	W	0
28	ES124	Event Set number 124 write 0: no action write 1: set corresponding event flag	W	0
27	ES123	Event Set number 123 write 0: no action write 1: set corresponding event flag	W	0
26	ES122	Event Set number 122 write 0: no action write 1: set corresponding event flag	W	0
25	ES121	Event Set number 121 write 0: no action write 1: set corresponding event flag	W	0
24	ES120	Event Set number 120 write 0: no action write 1: set corresponding event flag	W	0
23	ES119	Event Set number 119 write 0: no action write 1: set corresponding event flag	W	0
22	ES118	Event Set number 118 write 0: no action write 1: set corresponding event flag	W	0
21	ES117	Event Set number 117 write 0: no action write 1: set corresponding event flag	W	0
20	ES116	Event Set number 116 write 0: no action write 1: set corresponding event flag	W	0
19	ES115	Event Set number 115 write 0: no action write 1: set corresponding event flag	W	0
18	ES114	Event Set number 114 write 0: no action write 1: set corresponding event flag	W	0
17	ES113	Event Set number 113 write 0: no action write 1: set corresponding event flag	W	0
16	ES112	Event Set number 112 write 0: no action write 1: set corresponding event flag	W	0
15	ES111	Event Set number 111 write 0: no action write 1: set corresponding event flag	W	0
14	ES110	Event Set number 110 write 0: no action write 1: set corresponding event flag	W	0
13	ES109	Event Set number 109 write 0: no action write 1: set corresponding event flag	W	0
12	ES108	Event Set number 108 write 0: no action write 1: set corresponding event flag	W	0

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Bits	Field Name	Description	Type	Reset
11	ES107	Event Set number 107 write 0: no action write 1: set corresponding event flag	W	0
10	ES106	Event Set number 106 write 0: no action write 1: set corresponding event flag	W	0
9	ES105	Event Set number 105 write 0: no action write 1: set corresponding event flag	W	0
8	ES104	Event Set number 104 write 0: no action write 1: set corresponding event flag	W	0
7	ES103	Event Set number 103 write 0: no action write 1: set corresponding event flag	W	0
6	ES102	Event Set number 102 write 0: no action write 1: set corresponding event flag	W	0
5	ES101	Event Set number 101 write 0: no action write 1: set corresponding event flag	W	0
4	ES100	Event Set number 100 write 0: no action write 1: set corresponding event flag	W	0
3	ES99	Event Set number 99 write 0: no action write 1: set corresponding event flag	W	0
2	ES98	Event Set number 98 write 0: no action write 1: set corresponding event flag	W	0
1	ES97	Event Set number 97 write 0: no action write 1: set corresponding event flag	W	0
0	ES96	Event Set number 96 write 0: no action write 1: set corresponding event flag	W	0

Table 5-30. Register Call Summary for Register SYS_INTC_EVTSET3

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-31. SYS_INTC_EVTCLR0

Address Offset	0x0000 0040		
Physical Address	0x0180 0040	**Instance**	INTC_DSP
Description	Event Clear Register 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EC31	EC30	EC29	EC28	EC27	EC26	EC25	EC24	EC23	EC22	EC21	EC20	EC19	EC18	EC17	EC16	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

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Bits	Field Name	Description	Type	Reset
31	EC31	Event Clear number 31 write 0: no action write 1: clear corresponding event	W	0
30	EC30	Event Clear number 30 write 0: no action write 1: clear corresponding event	W	0
29	EC29	Event Clear number 29 write 0: no action write 1: clear corresponding event	W	0
28	EC28	Event Clear number 28 write 0: no action write 1: clear corresponding event	W	0
27	EC27	Event Clear number 27 write 0: no action write 1: clear corresponding event	W	0
26	EC26	Event Clear number 26 write 0: no action write 1: clear corresponding event	W	0
25	EC25	Event Clear number 25 write 0: no action write 1: clear corresponding event	W	0
24	EC24	Event Clear number 24 write 0: no action write 1: clear corresponding event	W	0
23	EC23	Event Clear number 23 write 0: no action write 1: clear corresponding event	W	0
22	EC22	Event Clear number 22 write 0: no action write 1: clear corresponding event	W	0
21	EC21	Event Clear number 21 write 0: no action write 1: clear corresponding event	W	0
20	EC20	Event Clear number 20 write 0: no action write 1: clear corresponding event	W	0
19	EC19	Event Clear number 19 write 0: no action write 1: clear corresponding event	W	0
18	EC18	Event Clear number 18 write 0: no action write 1: clear corresponding event	W	0
17	EC17	Event Clear number 17 write 0: no action write 1: clear corresponding event	W	0
16	EC16	Event Clear number 16 write 0: no action write 1: clear corresponding event	W	0
15	EC15	Event Clear number 15 write 0: no action write 1: clear corresponding event	W	0
14	EC14	Event Clear number 14 write 0: no action write 1: clear corresponding event	W	0
13	EC13	Event Clear number 13 write 0: no action write 1: clear corresponding event	W	0
12	EC12	Event Clear number 12 write 0: no action write 1: clear corresponding event	W	0

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Bits	Field Name	Description	Type	Reset
11	EC11	Event Clear number 11 write 0: no action write 1: clear corresponding event	W	0
10	EC10	Event Clear number 10 write 0: no action write 1: clear corresponding event	W	0
9	EC9	Event Clear number 9 write 0: no action write 1: clear corresponding event	W	0
8	EC8	Event Clear number 8 write 0: no action write 1: clear corresponding event	W	0
7	EC7	Event Clear number 7 write 0: no action write 1: clear corresponding event	W	0
6	EC6	Event Clear number 6 write 0: no action write 1: clear corresponding event	W	0
5	EC5	Event Clear number 5 write 0: no action write 1: clear corresponding event	W	0
4	EC4	Event Clear number 4 write 0: no action write 1: clear corresponding event	W	0
3	EC3	Event Clear number 3 write 0: no action write 1: clear corresponding event	W	0
2	EC2	Event Clear number 2 write 0: no action write 1: clear corresponding event	W	0
1	EC1	Event Clear number 1 write 0: no action write 1: clear corresponding event	W	0
0	EC0	Event Clear number 0 write 0: no action write 1: clear corresponding event	W	0

Table 5-32. Register Call Summary for Register SYS_INTC_EVTCLR0

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-33. SYS_INTC_EVTCLR1

Address Offset	0x0000 0044		
Physical Address	0x0180 0044	**Instance**	INTC_DSP
Description	Event Clear Register 1		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EC63	EC62	EC61	EC60	EC59	EC58	EC57	EC56	EC55	EC54	EC53	EC52	EC51	EC50	EC49	EC48	EC47	EC46	EC45	EC44	EC43	EC42	EC41	EC40	EC39	EC38	EC37	EC36	EC35	EC34	EC33	EC32

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Bits	Field Name	Description	Type	Reset
31	EC63	Event Clear number 63 write 0: no action write 1: clear corresponding event	W	0
30	EC62	Event Clear number 62 write 0: no action write 1: clear corresponding event	W	0
29	EC61	Event Clear number 61 write 0: no action write 1: clear corresponding event	W	0
28	EC60	Event Clear number 60 write 0: no action write 1: clear corresponding event	W	0
27	EC59	Event Clear number 59 write 0: no action write 1: clear corresponding event	W	0
26	EC58	Event Clear number 58 write 0: no action write 1: clear corresponding event	W	0
25	EC57	Event Clear number 57 write 0: no action write 1: clear corresponding event	W	0
24	EC56	Event Clear number 56 write 0: no action write 1: clear corresponding event	W	0
23	EC55	Event Clear number 55 write 0: no action write 1: clear corresponding event	W	0
22	EC54	Event Clear number 54 write 0: no action write 1: clear corresponding event	W	0
21	EC53	Event Clear number 53 write 0: no action write 1: clear corresponding event	W	0
20	EC52	Event Clear number 52 write 0: no action write 1: clear corresponding event	W	0
19	EC51	Event Clear number 51 write 0: no action write 1: clear corresponding event	W	0
18	EC50	Event Clear number 50 write 0: no action write 1: clear corresponding event	W	0
17	EC49	Event Clear number 49 write 0: no action write 1: clear corresponding event	W	0
16	EC48	Event Clear number 48 write 0: no action write 1: clear corresponding event	W	0
15	EC47	Event Clear number 47 write 0: no action write 1: clear corresponding event	W	0
14	EC46	Event Clear number 46 write 0: no action write 1: clear corresponding event	W	0
13	EC45	Event Clear number 45 write 0: no action write 1: clear corresponding event	W	0
12	EC44	Event Clear number 44 write 0: no action write 1: clear corresponding event	W	0

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Bits	Field Name	Description	Type	Reset
11	EC43	Event Clear number 43 write 0: no action write 1: clear corresponding event	W	0
10	EC42	Event Clear number 42 write 0: no action write 1: clear corresponding event	W	0
9	EC41	Event Clear number 41 write 0: no action write 1: clear corresponding event	W	0
8	EC40	Event Clear number 40 write 0: no action write 1: clear corresponding event	W	0
7	EC39	Event Clear number 39 write 0: no action write 1: clear corresponding event	W	0
6	EC38	Event Clear number 38 write 0: no action write 1: clear corresponding event	W	0
5	EC37	Event Clear number 37 write 0: no action write 1: clear corresponding event	W	0
4	EC36	Event Clear number 36 write 0: no action write 1: clear corresponding event	W	0
3	EC35	Event Clear number 35 write 0: no action write 1: clear corresponding event	W	0
2	EC34	Event Clear number 34 write 0: no action write 1: clear corresponding event	W	0
1	EC33	Event Clear number 33 write 0: no action write 1: clear corresponding event	W	0
0	EC32	Event Clear number 32 write 0: no action write 1: clear corresponding event	W	0

Table 5-34. Register Call Summary for Register SYS_INTC_EVTCLR1

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-35. SYS_INTC_EVTCLR2

Address Offset	0x0000 0048		
Physical Address	0x0180 0048	**Instance**	INTC_DSP
Description	Event Clear Register 2		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EC95	EC94	EC93	EC92	EC91	EC90	EC89	EC88	EC87	EC86	EC85	EC84	EC83	EC82	EC81	EC80	EC79	EC78	EC77	EC76	EC75	EC74	EC73	EC72	EC71	EC70	EC69	EC68	EC67	EC66	EC65	EC64

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Bits	Field Name	Description	Type	Reset
31	EC95	Event Clear number 95 write 0: no action write 1: clear corresponding event	W	0
30	EC94	Event Clear number 94 write 0: no action write 1: clear corresponding event	W	0
29	EC93	Event Clear number 93 write 0: no action write 1: clear corresponding event	W	0
28	EC92	Event Clear number 92 write 0: no action write 1: clear corresponding event	W	0
27	EC91	Event Clear number 91 write 0: no action write 1: clear corresponding event	W	0
26	EC90	Event Clear number 90 write 0: no action write 1: clear corresponding event	W	0
25	EC89	Event Clear number 89 write 0: no action write 1: clear corresponding event	W	0
24	EC88	Event Clear number 88 write 0: no action write 1: clear corresponding event	W	0
23	EC87	Event Clear number 87 write 0: no action write 1: clear corresponding event	W	0
22	EC86	Event Clear number 86 write 0: no action write 1: clear corresponding event	W	0
21	EC85	Event Clear number 85 write 0: no action write 1: clear corresponding event	W	0
20	EC84	Event Clear number 84 write 0: no action write 1: clear corresponding event	W	0
19	EC83	Event Clear number 83 write 0: no action write 1: clear corresponding event	W	0
18	EC82	Event Clear number 82 write 0: no action write 1: clear corresponding event	W	0
17	EC81	Event Clear number 81 write 0: no action write 1: clear corresponding event	W	0
16	EC80	Event Clear number 80 write 0: no action write 1: clear corresponding event	W	0
15	EC79	Event Clear number 79 write 0: no action write 1: clear corresponding event	W	0
14	EC78	Event Clear number 78 write 0: no action write 1: clear corresponding event	W	0
13	EC77	Event Clear number 77 write 0: no action write 1: clear corresponding event	W	0
12	EC76	Event Clear number 76 write 0: no action write 1: clear corresponding event	W	0

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Bits	Field Name	Description	Type	Reset
11	EC75	Event Clear number 75 write 0: no action write 1: clear corresponding event	W	0
10	EC74	Event Clear number 74 write 0: no action write 1: clear corresponding event	W	0
9	EC73	Event Clear number 73 write 0: no action write 1: clear corresponding event	W	0
8	EC72	Event Clear number 72 write 0: no action write 1: clear corresponding event	W	0
7	EC71	Event Clear number 71 write 0: no action write 1: clear corresponding event	W	0
6	EC70	Event Clear number 70 write 0: no action write 1: clear corresponding event	W	0
5	EC69	Event Clear number 69 write 0: no action write 1: clear corresponding event	W	0
4	EC68	Event Clear number 68 write 0: no action write 1: clear corresponding event	W	0
3	EC67	Event Clear number 67 write 0: no action write 1: clear corresponding event	W	0
2	EC66	Event Clear number 66 write 0: no action write 1: clear corresponding event	W	0
1	EC65	Event Clear number 65 write 0: no action write 1: clear corresponding event	W	0
0	EC64	Event Clear number 64 write 0: no action write 1: clear corresponding event	W	0

Table 5-36. Register Call Summary for Register SYS_INTC_EVTCLR2

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-37. SYS_INTC_EVTCLR3

Address Offset	0x0000 004C		
Physical Address	0x0180 004C	**Instance**	INTC_DSP
Description	Event Clear Register 3		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EC127	EC126	EC125	EC124	EC123	EC122	EC121	EC120	EC119	EC118	EC117	EC116	EC115	EC114	EC113	EC112	EC111	EC110	EC109	EC108	EC107	EC106	EC105	EC104	EC103	EC102	EC101	EC100	EC99	EC98	EC97	EC96

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Bits	Field Name	Description	Type	Reset
31	EC127	Event Clear number 127 write 0: no action write 1: clear corresponding event	W	0
30	EC126	Event Clear number 126 write 0: no action write 1: clear corresponding event	W	0
29	EC125	Event Clear number 125 write 0: no action write 1: clear corresponding event	W	0
28	EC124	Event Clear number 124 write 0: no action write 1: clear corresponding event	W	0
27	EC123	Event Clear number 123 write 0: no action write 1: clear corresponding event	W	0
26	EC122	Event Clear number 122 write 0: no action write 1: clear corresponding event	W	0
25	EC121	Event Clear number 121 write 0: no action write 1: clear corresponding event	W	0
24	EC120	Event Clear number 120 write 0: no action write 1: clear corresponding event	W	0
23	EC119	Event Clear number 119 write 0: no action write 1: clear corresponding event	W	0
22	EC118	Event Clear number 118 write 0: no action write 1: clear corresponding event	W	0
21	EC117	Event Clear number 117 write 0: no action write 1: clear corresponding event	W	0
20	EC116	Event Clear number 116 write 0: no action write 1: clear corresponding event	W	0
19	EC115	Event Clear number 115 write 0: no action write 1: clear corresponding event	W	0
18	EC114	Event Clear number 114 write 0: no action write 1: clear corresponding event	W	0
17	EC113	Event Clear number 113 write 0: no action write 1: clear corresponding event	W	0
16	EC112	Event Clear number 112 write 0: no action write 1: clear corresponding event	W	0
15	EC111	Event Clear number 111 write 0: no action write 1: clear corresponding event	W	0
14	EC110	Event Clear number 110 write 0: no action write 1: clear corresponding event	W	0
13	EC109	Event Clear number 109 write 0: no action write 1: clear corresponding event	W	0
12	EC108	Event Clear number 108 write 0: no action write 1: clear corresponding event	W	0

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Bits	Field Name	Description	Type	Reset
11	EC107	Event Clear number 107 write 0: no action write 1: clear corresponding event	W	0
10	EC106	Event Clear number 106 write 0: no action write 1: clear corresponding event	W	0
9	EC105	Event Clear number 105 write 0: no action write 1: clear corresponding event	W	0
8	EC104	Event Clear number 104 write 0: no action write 1: clear corresponding event	W	0
7	EC103	Event Clear number 103 write 0: no action write 1: clear corresponding event	W	0
6	EC102	Event Clear number 102 write 0: no action write 1: clear corresponding event	W	0
5	EC101	Event Clear number 101 write 0: no action write 1: clear corresponding event	W	0
4	EC100	Event Clear number 100 write 0: no action write 1: clear corresponding event	W	0
3	EC99	Event Clear number 99 write 0: no action write 1: clear corresponding event	W	0
2	EC98	Event Clear number 98 write 0: no action write 1: clear corresponding event	W	0
1	EC97	Event Clear number 97 write 0: no action write 1: clear corresponding event	W	0
0	EC96	Event Clear number 96 write 0: no action write 1: clear corresponding event	W	0

Table 5-38. Register Call Summary for Register SYS_INTC_EVTCLR3

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-39. SYS_INTC_EVTMASK0

Address Offset	0x0000 0080		
Physical Address	0x0180 0080	**Instance**	INTC_DSP
Description	Event Mask Register 0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EM31	EM30	EM29	EM28	EM27	EM26	EM25	EM24	EM23	EM22	EM21	EM20	EM19	EM18	EM17	EM16	EM15	EM14	EM13	EM12	EM11	EM10	EM9	EM8	EM7	EM6	EM5	EM4	EM3	EM2	EM1	EM0

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Bits	Field Name	Description	Type	Reset
31	EM31	Event Mask number 31 write 0: no action write 1: mask corresponding event	RW	0
30	EM30	Event Mask number 30 write 0: no action write 1: mask corresponding event	RW	0
29	EM29	Event Mask number 29 write 0: no action write 1: mask corresponding event	RW	0
28	EM28	Event Mask number 28 write 0: no action write 1: mask corresponding event	RW	0
27	EM27	Event Mask number 27 write 0: no action write 1: mask corresponding event	RW	0
26	EM26	Event Mask number 26 write 0: no action write 1: mask corresponding event	RW	0
25	EM25	Event Mask number 25 write 0: no action write 1: mask corresponding event	RW	0
24	EM24	Event Mask number 24 write 0: no action write 1: mask corresponding event	RW	0
23	EM23	Event Mask number 23 write 0: no action write 1: mask corresponding event	RW	0
22	EM22	Event Mask number 22 write 0: no action write 1: mask corresponding event	RW	0
21	EM21	Event Mask number 21 write 0: no action write 1: mask corresponding event	RW	0
20	EM20	Event Mask number 20 write 0: no action write 1: mask corresponding event	RW	0
19	EM19	Event Mask number 19 write 0: no action write 1: mask corresponding event	RW	0
18	EM18	Event Mask number 18 write 0: no action write 1: mask corresponding event	RW	0
17	EM17	Event Mask number 17 write 0: no action write 1: mask corresponding event	RW	0
16	EM16	Event Mask number 16 write 0: no action write 1: mask corresponding event	RW	0
15	EM15	Event Mask number 15 write 0: no action write 1: mask corresponding event	RW	0
14	EM14	Event Mask number 14 write 0: no action write 1: mask corresponding event	RW	0
13	EM13	Event Mask number 13 write 0: no action write 1: mask corresponding event	RW	0
12	EM12	Event Mask number 12 write 0: no action write 1: mask corresponding event	RW	0

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Bits	Field Name	Description	Type	Reset
11	EM11	Event Mask number 11 write 0: no action write 1: mask corresponding event	RW	0
10	EM10	Event Mask number 10 write 0: no action write 1: mask corresponding event	RW	0
9	EM9	Event Mask number 9 write 0: no action write 1: mask corresponding event	RW	0
8	EM8	Event Mask number 8 write 0: no action write 1: mask corresponding event	RW	0
7	EM7	Event Mask number 7 write 0: no action write 1: mask corresponding event	RW	0
6	EM6	Event Mask number 6 write 0: no action write 1: mask corresponding event	RW	0
5	EM5	Event Mask number 5 write 0: no action write 1: mask corresponding event	RW	0
4	EM4	Event Mask number 4 write 0: no action write 1: mask corresponding event	RW	0
3	EM3	Event Mask number 3 write 0: no action write 1: mask corresponding event	R	1
2	EM2	Event Mask number 2 write 0: no action write 1: mask corresponding event	R	1
1	EM1	Event Mask number 1 write 0: no action write 1: mask corresponding event	R	1
0	EM0	Event Mask number 0 write 0: no action write 1: mask corresponding event	R	1

Table 5-40. Register Call Summary for Register SYS_INTC_EVTMASK0

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-41. SYS_INTC_EVTMASK1

Address Offset	0x0000 0084		
Physical Address	0x0180 0084	**Instance**	INTC_DSP
Description	Event Mask Register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EM63	EM62	EM61	EM60	EM59	EM58	EM57	EM56	EM55	EM54	EM53	EM52	EM51	EM50	EM49	EM48	EM47	EM46	EM45	EM44	EM43	EM42	EM41	EM40	EM39	EM38	EM37	EM36	EM35	EM34	EM33	EM32

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Bits	Field Name	Description	Type	Reset
31	EM63	Event Mask number 63 write 0: no action write 1: mask corresponding event	RW	0
30	EM62	Event Mask number 62 write 0: no action write 1: mask corresponding event	RW	0
29	EM61	Event Mask number 61 write 0: no action write 1: mask corresponding event	RW	0
28	EM60	Event Mask number 60 write 0: no action write 1: mask corresponding event	RW	0
27	EM59	Event Mask number 59 write 0: no action write 1: mask corresponding event	RW	0
26	EM58	Event Mask number 58 write 0: no action write 1: mask corresponding event	RW	0
25	EM57	Event Mask number 57 write 0: no action write 1: mask corresponding event	RW	0
24	EM56	Event Mask number 56 write 0: no action write 1: mask corresponding event	RW	0
23	EM55	Event Mask number 55 write 0: no action write 1: mask corresponding event	RW	0
22	EM54	Event Mask number 54 write 0: no action write 1: mask corresponding event	RW	0
21	EM53	Event Mask number 53 write 0: no action write 1: mask corresponding event	RW	0
20	EM52	Event Mask number 52 write 0: no action write 1: mask corresponding event	RW	0
19	EM51	Event Mask number 51 write 0: no action write 1: mask corresponding event	RW	0
18	EM50	Event Mask number 50 write 0: no action write 1: mask corresponding event	RW	0
17	EM49	Event Mask number 49 write 0: no action write 1: mask corresponding event	RW	0
16	EM48	Event Mask number 48 write 0: no action write 1: mask corresponding event	RW	0
15	EM47	Event Mask number 47 write 0: no action write 1: mask corresponding event	RW	0
14	EM46	Event Mask number 46 write 0: no action write 1: mask corresponding event	RW	0
13	EM45	Event Mask number 45 write 0: no action write 1: mask corresponding event	RW	0
12	EM44	Event Mask number 44 write 0: no action write 1: mask corresponding event	RW	0

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Bits	Field Name	Description	Type	Reset
11	EM43	Event Mask number 43 write 0: no action write 1: mask corresponding event	RW	0
10	EM42	Event Mask number 42 write 0: no action write 1: mask corresponding event	RW	0
9	EM41	Event Mask number 41 write 0: no action write 1: mask corresponding event	RW	0
8	EM40	Event Mask number 40 write 0: no action write 1: mask corresponding event	RW	0
7	EM39	Event Mask number 39 write 0: no action write 1: mask corresponding event	RW	0
6	EM38	Event Mask number 38 write 0: no action write 1: mask corresponding event	RW	0
5	EM37	Event Mask number 37 write 0: no action write 1: mask corresponding event	RW	0
4	EM36	Event Mask number 36 write 0: no action write 1: mask corresponding event	RW	0
3	EM35	Event Mask number 35 write 0: no action write 1: mask corresponding event	RW	0
2	EM34	Event Mask number 34 write 0: no action write 1: mask corresponding event	RW	0
1	EM33	Event Mask number 33 write 0: no action write 1: mask corresponding event	RW	0
0	EM32	Event Mask number 32 write 0: no action write 1: mask corresponding event	RW	0

Table 5-42. Register Call Summary for Register SYS_INTC_EVTMASK1

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-43. SYS_INTC_EVTMASK2

Address Offset	0x0000 0088		
Physical Address	0x0180 0088	**Instance**	INTC_DSP
Description	Event Mask Register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EM95	EM94	EM93	EM92	EM91	EM90	EM89	EM88	EM87	EM86	EM85	EM84	EM83	EM82	EM81	EM80	EM79	EM78	EM77	EM76	EM75	EM74	EM73	EM72	EM71	EM70	EM69	EM68	EM67	EM66	EM65	EM64

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Bits	Field Name	Description	Type	Reset
31	EM95	Event Mask number 95 write 0: no action write 1: mask corresponding event	RW	0
30	EM94	Event Mask number 94 write 0: no action write 1: mask corresponding event	RW	0
29	EM93	Event Mask number 93 write 0: no action write 1: mask corresponding event	RW	0
28	EM92	Event Mask number 92 write 0: no action write 1: mask corresponding event	RW	0
27	EM91	Event Mask number 91 write 0: no action write 1: mask corresponding event	RW	0
26	EM90	Event Mask number 90 write 0: no action write 1: mask corresponding event	RW	0
25	EM89	Event Mask number 89 write 0: no action write 1: mask corresponding event	RW	0
24	EM88	Event Mask number 88 write 0: no action write 1: mask corresponding event	RW	0
23	EM87	Event Mask number 87 write 0: no action write 1: mask corresponding event	RW	0
22	EM86	Event Mask number 86 write 0: no action write 1: mask corresponding event	RW	0
21	EM85	Event Mask number 85 write 0: no action write 1: mask corresponding event	RW	0
20	EM84	Event Mask number 84 write 0: no action write 1: mask corresponding event	RW	0
19	EM83	Event Mask number 83 write 0: no action write 1: mask corresponding event	RW	0
18	EM82	Event Mask number 82 write 0: no action write 1: mask corresponding event	RW	0
17	EM81	Event Mask number 81 write 0: no action write 1: mask corresponding event	RW	0
16	EM80	Event Mask number 80 write 0: no action write 1: mask corresponding event	RW	0
15	EM79	Event Mask number 79 write 0: no action write 1: mask corresponding event	RW	0
14	EM78	Event Mask number 78 write 0: no action write 1: mask corresponding event	RW	0
13	EM77	Event Mask number 77 write 0: no action write 1: mask corresponding event	RW	0
12	EM76	Event Mask number 76 write 0: no action write 1: mask corresponding event	RW	0

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Bits	Field Name	Description	Type	Reset
11	EM75	Event Mask number 75 write 0: no action write 1: mask corresponding event	RW	0
10	EM74	Event Mask number 74 write 0: no action write 1: mask corresponding event	RW	0
9	EM73	Event Mask number 73 write 0: no action write 1: mask corresponding event	RW	0
8	EM72	Event Mask number 72 write 0: no action write 1: mask corresponding event	RW	0
7	EM71	Event Mask number 71 write 0: no action write 1: mask corresponding event	RW	0
6	EM70	Event Mask number 70 write 0: no action write 1: mask corresponding event	RW	0
5	EM69	Event Mask number 69 write 0: no action write 1: mask corresponding event	RW	0
4	EM68	Event Mask number 68 write 0: no action write 1: mask corresponding event	RW	0
3	EM67	Event Mask number 67 write 0: no action write 1: mask corresponding event	RW	0
2	EM66	Event Mask number 66 write 0: no action write 1: mask corresponding event	RW	0
1	EM65	Event Mask number 65 write 0: no action write 1: mask corresponding event	RW	0
0	EM64	Event Mask number 64 write 0: no action write 1: mask corresponding event	RW	0

Table 5-44. Register Call Summary for Register SYS_INTC_EVTMASK2

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-45. SYS_INTC_EVTMASK3

Address Offset	0x0000 008C		
Physical Address	0x0180 008C	**Instance**	INTC_DSP
Description	Event Mask Register 3		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EM127	EM126	EM125	EM124	EM123	EM122	EM121	EM120	EM119	EM118	EM117	EM116	EM115	EM114	EM113	EM112	EM111	EM110	EM109	EM108	EM107	EM106	EM105	EM104	EM103	EM102	EM101	EM100	EM99	EM98	EM97	EM96

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Bits	Field Name	Description	Type	Reset
31	EM127	Event Mask number 127 write 0: no action write 1: mask corresponding event	RW	0
30	EM126	Event Mask number 126 write 0: no action write 1: mask corresponding event	RW	0
29	EM125	Event Mask number 125 write 0: no action write 1: mask corresponding event	RW	0
28	EM124	Event Mask number 124 write 0: no action write 1: mask corresponding event	RW	0
27	EM123	Event Mask number 123 write 0: no action write 1: mask corresponding event	RW	0
26	EM122	Event Mask number 122 write 0: no action write 1: mask corresponding event	RW	0
25	EM121	Event Mask number 121 write 0: no action write 1: mask corresponding event	RW	0
24	EM120	Event Mask number 120 write 0: no action write 1: mask corresponding event	RW	0
23	EM119	Event Mask number 119 write 0: no action write 1: mask corresponding event	RW	0
22	EM118	Event Mask number 118 write 0: no action write 1: mask corresponding event	RW	0
21	EM117	Event Mask number 117 write 0: no action write 1: mask corresponding event	RW	0
20	EM116	Event Mask number 116 write 0: no action write 1: mask corresponding event	RW	0
19	EM115	Event Mask number 115 write 0: no action write 1: mask corresponding event	RW	0
18	EM114	Event Mask number 114 write 0: no action write 1: mask corresponding event	RW	0
17	EM113	Event Mask number 113 write 0: no action write 1: mask corresponding event	RW	0
16	EM112	Event Mask number 112 write 0: no action write 1: mask corresponding event	RW	0
15	EM111	Event Mask number 111 write 0: no action write 1: mask corresponding event	RW	0
14	EM110	Event Mask number 110 write 0: no action write 1: mask corresponding event	RW	0
13	EM109	Event Mask number 109 write 0: no action write 1: mask corresponding event	RW	0
12	EM108	Event Mask number 108 write 0: no action write 1: mask corresponding event	RW	0

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Bits	Field Name	Description	Type	Reset
11	EM107	Event Mask number 107 write 0: no action write 1: mask corresponding event	RW	0
10	EM106	Event Mask number 106 write 0: no action write 1: mask corresponding event	RW	0
9	EM105	Event Mask number 105 write 0: no action write 1: mask corresponding event	RW	0
8	EM104	Event Mask number 104 write 0: no action write 1: mask corresponding event	RW	0
7	EM103	Event Mask number 103 write 0: no action write 1: mask corresponding event	RW	0
6	EM102	Event Mask number 102 write 0: no action write 1: mask corresponding event	RW	0
5	EM101	Event Mask number 101 write 0: no action write 1: mask corresponding event	RW	0
4	EM100	Event Mask number 100 write 0: no action write 1: mask corresponding event	RW	0
3	EM99	Event Mask number 99 write 0: no action write 1: mask corresponding event	RW	0
2	EM98	Event Mask number 98 write 0: no action write 1: mask corresponding event	RW	0
1	EM97	Event Mask number 97 write 0: no action write 1: mask corresponding event	RW	0
0	EM96	Event Mask number 96 write 0: no action write 1: mask corresponding event	RW	0

Table 5-46. Register Call Summary for Register SYS_INTC_EVTMASK3

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-47. SYS_INTC_MEVTFLAG0

Address Offset	0x0000 00A0		
Physical Address	0x0180 00A0	**Instance**	INTC_DSP
Description	Masked Event Flag Register 0		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEF31	MEF30	MEF29	MEF28	MEF27	MEF26	MEF25	MEF24	MEF23	MEF22	MEF21	MEF20	MEF19	MEF18	MEF17	MEF16	MEF15	MEF14	MEF13	MEF12	MEF11	MEF10	MEF9	MEF8	MEF7	MEF6	MEF5	MEF4	MEF3	MEF2	MEF1	MEF0

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Bits	Field Name	Description	Type	Reset
31	MEF31	Masked Event Flag number 31 0: no event occurred 1: an event occurred	R	0
30	MEF30	Masked Event Flag number 30 0: no event occurred 1: an event occurred	R	0
29	MEF29	Masked Event Flag number 29 0: no event occurred 1: an event occurred	R	0
28	MEF28	Masked Event Flag number 28 0: no event occurred 1: an event occurred	R	0
27	MEF27	Masked Event Flag number 27 0: no event occurred 1: an event occurred	R	0
26	MEF26	Masked Event Flag number 26 0: no event occurred 1: an event occurred	R	0
25	MEF25	Masked Event Flag number 25 0: no event occurred 1: an event occurred	R	0
24	MEF24	Masked Event Flag number 24 0: no event occurred 1: an event occurred	R	0
23	MEF23	Masked Event Flag number 23 0: no event occurred 1: an event occurred	R	0
22	MEF22	Masked Event Flag number 22 0: no event occurred 1: an event occurred	R	0
21	MEF21	Masked Event Flag number 21 0: no event occurred 1: an event occurred	R	0
20	MEF20	Masked Event Flag number 20 0: no event occurred 1: an event occurred	R	0
19	MEF19	Masked Event Flag number 19 0: no event occurred 1: an event occurred	R	0
18	MEF18	Masked Event Flag number 18 0: no event occurred 1: an event occurred	R	0
17	MEF17	Masked Event Flag number 17 0: no event occurred 1: an event occurred	R	0
16	MEF16	Masked Event Flag number 16 0: no event occurred 1: an event occurred	R	0
15	MEF15	Masked Event Flag number 15 0: no event occurred 1: an event occurred	R	0
14	MEF14	Masked Event Flag number 14 0: no event occurred 1: an event occurred	R	0
13	MEF13	Masked Event Flag number 13 0: no event occurred 1: an event occurred	R	0
12	MEF12	Masked Event Flag number 12 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
11	MEF11	Masked Event Flag number 11 0: no event occurred 1: an event occurred	R	0
10	MEF10	Masked Event Flag number 10 0: no event occurred 1: an event occurred	R	0
9	MEF9	Masked Event Flag number 9 0: no event occurred 1: an event occurred	R	0
8	MEF8	Masked Event Flag number 8 0: no event occurred 1: an event occurred	R	0
7	MEF7	Masked Event Flag number 7 0: no event occurred 1: an event occurred	R	0
6	MEF6	Masked Event Flag number 6 0: no event occurred 1: an event occurred	R	0
5	MEF5	Masked Event Flag number 5 0: no event occurred 1: an event occurred	R	0
4	MEF4	Masked Event Flag number 4 0: no event occurred 1: an event occurred	R	0
3	MEF3	Masked Event Flag number 3 0: no event occurred 1: an event occurred	R	0
2	MEF2	Masked Event Flag number 2 0: no event occurred 1: an event occurred	R	0
1	MEF1	Masked Event Flag number 1 0: no event occurred 1: an event occurred	R	0
0	MEF0	Masked Event Flag number 0 0: no event occurred 1: an event occurred	R	0

Table 5-48. Register Call Summary for Register SYS_INTC_MEVTFLAG0

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-49. SYS_INTC_MEVTFLAG1

Address Offset	0x0000 00A4		
Physical Address	0x0180 00A4	**Instance**	INTC_DSP
Description	Masked Event Flag Register 1		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEF63	MEF62	MEF61	MEF60	MEF59	MEF58	MEF57	MEF56	MEF55	MEF54	MEF53	MEF52	MEF51	MEF50	MEF49	MEF48	MEF47	MEF46	MEF45	MEF44	MEF43	MEF42	MEF41	MEF40	MEF39	MEF38	MEF37	MEF36	MEF35	MEF34	MEF33	MEF32

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Bits	Field Name	Description	Type	Reset
31	MEF63	Masked Event Flag number 63 0: no event occurred 1: an event occurred	R	0
30	MEF62	Masked Event Flag number 62 0: no event occurred 1: an event occurred	R	0
29	MEF61	Masked Event Flag number 61 0: no event occurred 1: an event occurred	R	0
28	MEF60	Masked Event Flag number 60 0: no event occurred 1: an event occurred	R	0
27	MEF59	Masked Event Flag number 59 0: no event occurred 1: an event occurred	R	0
26	MEF58	Masked Event Flag number 58 0: no event occurred 1: an event occurred	R	0
25	MEF57	Masked Event Flag number 57 0: no event occurred 1: an event occurred	R	0
24	MEF56	Masked Event Flag number 56 0: no event occurred 1: an event occurred	R	0
23	MEF55	Masked Event Flag number 55 0: no event occurred 1: an event occurred	R	0
22	MEF54	Masked Event Flag number 54 0: no event occurred 1: an event occurred	R	0
21	MEF53	Masked Event Flag number 53 0: no event occurred 1: an event occurred	R	0
20	MEF52	Masked Event Flag number 52 0: no event occurred 1: an event occurred	R	0
19	MEF51	Masked Event Flag number 51 0: no event occurred 1: an event occurred	R	0
18	MEF50	Masked Event Flag number 50 0: no event occurred 1: an event occurred	R	0
17	MEF49	Masked Event Flag number 49 0: no event occurred 1: an event occurred	R	0
16	MEF48	Masked Event Flag number 48 0: no event occurred 1: an event occurred	R	0
15	MEF47	Masked Event Flag number 47 0: no event occurred 1: an event occurred	R	0
14	MEF46	Masked Event Flag number 46 0: no event occurred 1: an event occurred	R	0
13	MEF45	Masked Event Flag number 45 0: no event occurred 1: an event occurred	R	0
12	MEF44	Masked Event Flag number 44 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
11	MEF43	Masked Event Flag number 43 0: no event occurred 1: an event occurred	R	0
10	MEF42	Masked Event Flag number 42 0: no event occurred 1: an event occurred	R	0
9	MEF41	Masked Event Flag number 41 0: no event occurred 1: an event occurred	R	0
8	MEF40	Masked Event Flag number 40 0: no event occurred 1: an event occurred	R	0
7	MEF39	Masked Event Flag number 39 0: no event occurred 1: an event occurred	R	0
6	MEF38	Masked Event Flag number 38 0: no event occurred 1: an event occurred	R	0
5	MEF37	Masked Event Flag number 37 0: no event occurred 1: an event occurred	R	0
4	MEF36	Masked Event Flag number 36 0: no event occurred 1: an event occurred	R	0
3	MEF35	Masked Event Flag number 35 0: no event occurred 1: an event occurred	R	0
2	MEF34	Masked Event Flag number 34 0: no event occurred 1: an event occurred	R	0
1	MEF33	Masked Event Flag number 33 0: no event occurred 1: an event occurred	R	0
0	MEF32	Masked Event Flag number 32 0: no event occurred 1: an event occurred	R	0

Table 5-50. Register Call Summary for Register SYS_INTC_MEVTFLAG1

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-51. SYS_INTC_MEVTFLAG2

Address Offset	0x0000 00A8		
Physical Address	0x0180 00A8	**Instance**	INTC_DSP
Description	Masked Event Flag Register 2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEF95	MEF94	MEF93	MEF92	MEF91	MEF90	MEF89	MEF88	MEF87	MEF86	MEF85	MEF84	MEF83	MEF82	MEF81	MEF80	MEF79	MEF78	MEF77	MEF76	MEF75	MEF74	MEF73	MEF72	MEF71	MEF70	MEF69	MEF68	MEF67	MEF66	MEF65	MEF64

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Bits	Field Name	Description	Type	Reset
31	MEF95	Masked Event Flag number 95 0: no event occurred 1: an event occurred	R	0
30	MEF94	Masked Event Flag number 94 0: no event occurred 1: an event occurred	R	0
29	MEF93	Masked Event Flag number 93 0: no event occurred 1: an event occurred	R	0
28	MEF92	Masked Event Flag number 92 0: no event occurred 1: an event occurred	R	0
27	MEF91	Masked Event Flag number 91 0: no event occurred 1: an event occurred	R	0
26	MEF90	Masked Event Flag number 90 0: no event occurred 1: an event occurred	R	0
25	MEF89	Masked Event Flag number 89 0: no event occurred 1: an event occurred	R	0
24	MEF88	Masked Event Flag number 88 0: no event occurred 1: an event occurred	R	0
23	MEF87	Masked Event Flag number 87 0: no event occurred 1: an event occurred	R	0
22	MEF86	Masked Event Flag number 86 0: no event occurred 1: an event occurred	R	0
21	MEF85	Masked Event Flag number 85 0: no event occurred 1: an event occurred	R	0
20	MEF84	Masked Event Flag number 84 0: no event occurred 1: an event occurred	R	0
19	MEF83	Masked Event Flag number 83 0: no event occurred 1: an event occurred	R	0
18	MEF82	Masked Event Flag number 82 0: no event occurred 1: an event occurred	R	0
17	MEF81	Masked Event Flag number 81 0: no event occurred 1: an event occurred	R	0
16	MEF80	Masked Event Flag number 80 0: no event occurred 1: an event occurred	R	0
15	MEF79	Masked Event Flag number 79 0: no event occurred 1: an event occurred	R	0
14	MEF78	Masked Event Flag number 78 0: no event occurred 1: an event occurred	R	0
13	MEF77	Masked Event Flag number 77 0: no event occurred 1: an event occurred	R	0
12	MEF76	Masked Event Flag number 76 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
11	MEF75	Masked Event Flag number 75 0: no event occurred 1: an event occurred	R	0
10	MEF74	Masked Event Flag number 74 0: no event occurred 1: an event occurred	R	0
9	MEF73	Masked Event Flag number 73 0: no event occurred 1: an event occurred	R	0
8	MEF72	Masked Event Flag number 72 0: no event occurred 1: an event occurred	R	0
7	MEF71	Masked Event Flag number 71 0: no event occurred 1: an event occurred	R	0
6	MEF70	Masked Event Flag number 70 0: no event occurred 1: an event occurred	R	0
5	MEF69	Masked Event Flag number 69 0: no event occurred 1: an event occurred	R	0
4	MEF68	Masked Event Flag number 68 0: no event occurred 1: an event occurred	R	0
3	MEF67	Masked Event Flag number 67 0: no event occurred 1: an event occurred	R	0
2	MEF66	Masked Event Flag number 66 0: no event occurred 1: an event occurred	R	0
1	MEF65	Masked Event Flag number 65 0: no event occurred 1: an event occurred	R	0
0	MEF64	Masked Event Flag number 64 0: no event occurred 1: an event occurred	R	0

Table 5-52. Register Call Summary for Register SYS_INTC_MEVTFLAG2

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-53. SYS_INTC_MEVTFLAG3

Address Offset	0x0000 00AC		
Physical Address	0x0180 00AC	**Instance**	INTC_DSP
Description	Masked Event Flag Register 3		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEF127	MEF126	MEF125	MEF124	MEF123	MEF122	MEF121	MEF120	MEF119	MEF118	MEF117	MEF116	MEF115	MEF114	MEF113	MEF112	MEF111	MEF110	MEF109	MEF108	MEF107	MEF106	MEF105	MEF104	MEF103	MEF102	MEF101	MEF100	MEF99	MEF98	MEF97	MEF96

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Bits	Field Name	Description	Type	Reset
31	MEF127	Masked Event Flag number 127 0: no event occurred 1: an event occurred	R	0
30	MEF126	Masked Event Flag number 126 0: no event occurred 1: an event occurred	R	0
29	MEF125	Masked Event Flag number 125 0: no event occurred 1: an event occurred	R	0
28	MEF124	Masked Event Flag number 124 0: no event occurred 1: an event occurred	R	0
27	MEF123	Masked Event Flag number 123 0: no event occurred 1: an event occurred	R	0
26	MEF122	Masked Event Flag number 122 0: no event occurred 1: an event occurred	R	0
25	MEF121	Masked Event Flag number 121 0: no event occurred 1: an event occurred	R	0
24	MEF120	Masked Event Flag number 120 0: no event occurred 1: an event occurred	R	0
23	MEF119	Masked Event Flag number 119 0: no event occurred 1: an event occurred	R	0
22	MEF118	Masked Event Flag number 118 0: no event occurred 1: an event occurred	R	0
21	MEF117	Masked Event Flag number 117 0: no event occurred 1: an event occurred	R	0
20	MEF116	Masked Event Flag number 116 0: no event occurred 1: an event occurred	R	0
19	MEF115	Masked Event Flag number 115 0: no event occurred 1: an event occurred	R	0
18	MEF114	Masked Event Flag number 114 0: no event occurred 1: an event occurred	R	0
17	MEF113	Masked Event Flag number 113 0: no event occurred 1: an event occurred	R	0
16	MEF112	Masked Event Flag number 112 0: no event occurred 1: an event occurred	R	0
15	MEF111	Masked Event Flag number 111 0: no event occurred 1: an event occurred	R	0
14	MEF110	Masked Event Flag number 110 0: no event occurred 1: an event occurred	R	0
13	MEF109	Masked Event Flag number 109 0: no event occurred 1: an event occurred	R	0
12	MEF108	Masked Event Flag number 108 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
11	MEF107	Masked Event Flag number 107 0: no event occurred 1: an event occurred	R	0
10	MEF106	Masked Event Flag number 106 0: no event occurred 1: an event occurred	R	0
9	MEF105	Masked Event Flag number 105 0: no event occurred 1: an event occurred	R	0
8	MEF104	Masked Event Flag number 104 0: no event occurred 1: an event occurred	R	0
7	MEF103	Masked Event Flag number 103 0: no event occurred 1: an event occurred	R	0
6	MEF102	Masked Event Flag number 102 0: no event occurred 1: an event occurred	R	0
5	MEF101	Masked Event Flag number 101 0: no event occurred 1: an event occurred	R	0
4	MEF100	Masked Event Flag number 100 0: no event occurred 1: an event occurred	R	0
3	MEF99	Masked Event Flag number 99 0: no event occurred 1: an event occurred	R	0
2	MEF98	Masked Event Flag number 98 0: no event occurred 1: an event occurred	R	0
1	MEF97	Masked Event Flag number 97 0: no event occurred 1: an event occurred	R	0
0	MEF96	Masked Event Flag number 96 0: no event occurred 1: an event occurred	R	0

Table 5-54. Register Call Summary for Register SYS_INTC_MEVTFLAG3

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-55. SYS_INTC_EXPMASK0

Address Offset	0x0000 00C0		
Physical Address	0x0180 00C0	**Instance**	INTC_DSP
Description	Exception Mask Register 0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XM31	XM30	XM29	XM28	XM27	XM26	XM25	XM24	XM23	XM22	XM21	XM20	XM19	XM18	XM17	RESERVED	XM15	XM14	XM13	XM12	XM11	XM10	XM9	XM8	XM7	XM6	XM5	XM4	XM3	XM2	XM1	XM0

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Bits	Field Name	Description	Type	Reset
31	XM31	Exception Mask number 31 write 0: no action write 1: mask corresponding event	RW	1
30	XM30	Exception Mask number 30 write 0: no action write 1: mask corresponding event	RW	1
29	XM29	Exception Mask number 29 write 0: no action write 1: mask corresponding event	RW	1
28	XM28	Exception Mask number 28 write 0: no action write 1: mask corresponding event	RW	1
27	XM27	Exception Mask number 27 write 0: no action write 1: mask corresponding event	RW	1
26	XM26	Exception Mask number 26 write 0: no action write 1: mask corresponding event	RW	1
25	XM25	Exception Mask number 25 write 0: no action write 1: mask corresponding event	RW	1
24	XM24	Exception Mask number 24 write 0: no action write 1: mask corresponding event	RW	1
23	XM23	Exception Mask number 23 write 0: no action write 1: mask corresponding event	RW	1
22	XM22	Exception Mask number 22 write 0: no action write 1: mask corresponding event	RW	1
21	XM21	Exception Mask number 21 write 0: no action write 1: mask corresponding event	RW	1
20	XM20	Exception Mask number 20 write 0: no action write 1: mask corresponding event	RW	1
19	XM19	Exception Mask number 19 write 0: no action write 1: mask corresponding event	RW	1
18	XM18	Exception Mask number 18 write 0: no action write 1: mask corresponding event	RW	1
17	XM17	Exception Mask number 17 write 0: no action write 1: mask corresponding event	RW	1
16	RESERVED	Reserved.	R	1
15	XM15	Exception Mask number 15 write 0: no action write 1: mask corresponding event	RW	1
14	XM14	Exception Mask number 14 write 0: no action write 1: mask corresponding event	RW	1
13	XM13	Exception Mask number 13 write 0: no action write 1: mask corresponding event	RW	1
12	XM12	Exception Mask number 12 write 0: no action write 1: mask corresponding event	RW	1
11	XM11	Exception Mask number 11 write 0: no action write 1: mask corresponding event	RW	1

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Bits	Field Name	Description	Type	Reset
10	XM10	Exception Mask number 10 write 0: no action write 1: mask corresponding event	RW	1
9	XM9	Exception Mask number 9 write 0: no action write 1: mask corresponding event	RW	1
8	XM8	Exception Mask number 8 write 0: no action write 1: mask corresponding event	RW	1
7	XM7	Exception Mask number 7 write 0: no action write 1: mask corresponding event	RW	1
6	XM6	Exception Mask number 6 write 0: no action write 1: mask corresponding event	RW	1
5	XM5	Exception Mask number 5 write 0: no action write 1: mask corresponding event	RW	1
4	XM4	Exception Mask number 4 write 0: no action write 1: mask corresponding event	RW	1
3	XM3	Exception Mask number 3 write 0: no action write 1: mask corresponding event	R	1
2	XM2	Exception Mask number 2 write 0: no action write 1: mask corresponding event	R	1
1	XM1	Exception Mask number 1 write 0: no action write 1: mask corresponding event	R	1
0	XM0	Exception Mask number 0 write 0: no action write 1: mask corresponding event	R	1

Table 5-56. Register Call Summary for Register SYS_INTC_EXPMASK0

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-57. SYS_INTC_EXPMASK1

Address Offset	0x0000 00C4		
Physical Address	0x0180 00C4	**Instance**	INTC_DSP
Description	Exception Mask Register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XM63	XM62	XM61	XM60	XM59	XM58	XM57	XM56	XM55	XM54	XM53	XM52	XM51	XM50	XM49	XM48	XM47	XM46	XM45	XM44	XM43	XM42	XM41	XM40	XM39	XM38	XM37	XM36	XM35	XM34	XM33	XM32

Bits	Field Name	Description	Type	Reset
31	XM63	Exception Mask number 63 write 0: no action write 1: mask corresponding event	RW	1
30	XM62	Exception Mask number 62 write 0: no action write 1: mask corresponding event	RW	1

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Bits	Field Name	Description	Type	Reset
29	XM61	Exception Mask number 61 write 0: no action write 1: mask corresponding event	RW	1
28	XM60	Exception Mask number 60 write 0: no action write 1: mask corresponding event	RW	1
27	XM59	Exception Mask number 59 write 0: no action write 1: mask corresponding event	RW	1
26	XM58	Exception Mask number 58 write 0: no action write 1: mask corresponding event	RW	1
25	XM57	Exception Mask number 57 write 0: no action write 1: mask corresponding event	RW	1
24	XM56	Exception Mask number 56 write 0: no action write 1: mask corresponding event	RW	1
23	XM55	Exception Mask number 55 write 0: no action write 1: mask corresponding event	RW	1
22	XM54	Exception Mask number 54 write 0: no action write 1: mask corresponding event	RW	1
21	XM53	Exception Mask number 53 write 0: no action write 1: mask corresponding event	RW	1
20	XM52	Exception Mask number 52 write 0: no action write 1: mask corresponding event	RW	1
19	XM51	Exception Mask number 51 write 0: no action write 1: mask corresponding event	RW	1
18	XM50	Exception Mask number 50 write 0: no action write 1: mask corresponding event	RW	1
17	XM49	Exception Mask number 49 write 0: no action write 1: mask corresponding event	RW	1
16	XM48	Exception Mask number 48 write 0: no action write 1: mask corresponding event	RW	1
15	XM47	Exception Mask number 47 write 0: no action write 1: mask corresponding event	RW	1
14	XM46	Exception Mask number 46 write 0: no action write 1: mask corresponding event	RW	1
13	XM45	Exception Mask number 45 write 0: no action write 1: mask corresponding event	RW	1
12	XM44	Exception Mask number 44 write 0: no action write 1: mask corresponding event	RW	1
11	XM43	Exception Mask number 43 write 0: no action write 1: mask corresponding event	RW	1
10	XM42	Exception Mask number 42 write 0: no action write 1: mask corresponding event	RW	1

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Bits	Field Name	Description	Type	Reset
9	XM41	Exception Mask number 41 write 0: no action write 1: mask corresponding event	RW	1
8	XM40	Exception Mask number 40 write 0: no action write 1: mask corresponding event	RW	1
7	XM39	Exception Mask number 39 write 0: no action write 1: mask corresponding event	RW	1
6	XM38	Exception Mask number 38 write 0: no action write 1: mask corresponding event	RW	1
5	XM37	Exception Mask number 37 write 0: no action write 1: mask corresponding event	RW	1
4	XM36	Exception Mask number 36 write 0: no action write 1: mask corresponding event	RW	1
3	XM35	Exception Mask number 35 write 0: no action write 1: mask corresponding event	RW	1
2	XM34	Exception Mask number 34 write 0: no action write 1: mask corresponding event	RW	1
1	XM33	Exception Mask number 33 write 0: no action write 1: mask corresponding event	RW	1
0	XM32	Exception Mask number 32 write 0: no action write 1: mask corresponding event	RW	1

Table 5-58. Register Call Summary for Register SYS_INTC_EXPMASK1

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-59. SYS_INTC_EXPMASK2

Address Offset	0x0000 00C8		
Physical Address	0x0180 00C8	**Instance**	INTC_DSP
Description	Exception Mask Register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XM95	XM94	XM93	XM92	XM91	XM90	XM89	XM88	XM87	XM86	XM85	XM84	XM83	XM82	XM81	XM80	XM79	XM78	XM77	XM76	XM75	XM74	XM73	XM72	XM71	XM70	XM69	XM68	XM67	XM66	XM65	XM64

Bits	Field Name	Description	Type	Reset
31	XM95	Exception Mask number 95 write 0: no action write 1: mask corresponding event	RW	1
30	XM94	Exception Mask number 94 write 0: no action write 1: mask corresponding event	RW	1
29	XM93	Exception Mask number 93 write 0: no action write 1: mask corresponding event	RW	1

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Bits	Field Name	Description	Type	Reset
28	XM92	Exception Mask number 92 write 0: no action write 1: mask corresponding event	RW	1
27	XM91	Exception Mask number 91 write 0: no action write 1: mask corresponding event	RW	1
26	XM90	Exception Mask number 90 write 0: no action write 1: mask corresponding event	RW	1
25	XM89	Exception Mask number 89 write 0: no action write 1: mask corresponding event	RW	1
24	XM88	Exception Mask number 88 write 0: no action write 1: mask corresponding event	RW	1
23	XM87	Exception Mask number 87 write 0: no action write 1: mask corresponding event	RW	1
22	XM86	Exception Mask number 86 write 0: no action write 1: mask corresponding event	RW	1
21	XM85	Exception Mask number 85 write 0: no action write 1: mask corresponding event	RW	1
20	XM84	Exception Mask number 84 write 0: no action write 1: mask corresponding event	RW	1
19	XM83	Exception Mask number 83 write 0: no action write 1: mask corresponding event	RW	1
18	XM82	Exception Mask number 82 write 0: no action write 1: mask corresponding event	RW	1
17	XM81	Exception Mask number 81 write 0: no action write 1: mask corresponding event	RW	1
16	XM80	Exception Mask number 80 write 0: no action write 1: mask corresponding event	RW	1
15	XM79	Exception Mask number 79 write 0: no action write 1: mask corresponding event	RW	1
14	XM78	Exception Mask number 78 write 0: no action write 1: mask corresponding event	RW	1
13	XM77	Exception Mask number 77 write 0: no action write 1: mask corresponding event	RW	1
12	XM76	Exception Mask number 76 write 0: no action write 1: mask corresponding event	RW	1
11	XM75	Exception Mask number 75 write 0: no action write 1: mask corresponding event	RW	1
10	XM74	Exception Mask number 74 write 0: no action write 1: mask corresponding event	RW	1
9	XM73	Exception Mask number 73 write 0: no action write 1: mask corresponding event	RW	1

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Bits	Field Name	Description	Type	Reset
8	XM72	Exception Mask number 72 write 0: no action write 1: mask corresponding event	RW	1
7	XM71	Exception Mask number 71 write 0: no action write 1: mask corresponding event	RW	1
6	XM70	Exception Mask number 70 write 0: no action write 1: mask corresponding event	RW	1
5	XM69	Exception Mask number 69 write 0: no action write 1: mask corresponding event	RW	1
4	XM68	Exception Mask number 68 write 0: no action write 1: mask corresponding event	RW	1
3	XM67	Exception Mask number 67 write 0: no action write 1: mask corresponding event	RW	1
2	XM66	Exception Mask number 66 write 0: no action write 1: mask corresponding event	RW	1
1	XM65	Exception Mask number 65 write 0: no action write 1: mask corresponding event	RW	1
0	XM64	Exception Mask number 64 write 0: no action write 1: mask corresponding event	RW	1

Table 5-60. Register Call Summary for Register SYS_INTC_EXPMASK2

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-61. SYS_INTC_EXPMASK3

Address Offset	0x0000 00CC		
Physical Address	0x0180 00CC	**Instance**	INTC_DSP
Description	Exception Mask Register 3		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XM127	XM126	XM125	XM124	XM123	XM122	XM121	XM120	XM119	XM118	XM117	XM116	XM115	XM114	XM113	XM112	XM111	XM110	XM109	XM108	XM107	XM106	XM105	XM104	XM103	XM102	XM101	XM100	XM99	XM98	XM97	XM96

Bits	Field Name	Description	Type	Reset
31	XM127	Exception Mask number 127 write 0: no action write 1: mask corresponding event	RW	1
30	XM126	Exception Mask number 126 write 0: no action write 1: mask corresponding event	RW	1
29	XM125	Exception Mask number 125 write 0: no action write 1: mask corresponding event	RW	1
28	XM124	Exception Mask number 124 write 0: no action write 1: mask corresponding event	RW	1

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Bits	Field Name	Description	Type	Reset
27	XM123	Exception Mask number 123 write 0: no action write 1: mask corresponding event	RW	1
26	XM122	Exception Mask number 122 write 0: no action write 1: mask corresponding event	RW	1
25	XM121	Exception Mask number 121 write 0: no action write 1: mask corresponding event	RW	1
24	XM120	Exception Mask number 120 write 0: no action write 1: mask corresponding event	RW	1
23	XM119	Exception Mask number 119 write 0: no action write 1: mask corresponding event	RW	1
22	XM118	Exception Mask number 118 write 0: no action write 1: mask corresponding event	RW	1
21	XM117	Exception Mask number 117 write 0: no action write 1: mask corresponding event	RW	1
20	XM116	Exception Mask number 116 write 0: no action write 1: mask corresponding event	RW	1
19	XM115	Exception Mask number 115 write 0: no action write 1: mask corresponding event	RW	1
18	XM114	Exception Mask number 114 write 0: no action write 1: mask corresponding event	RW	1
17	XM113	Exception Mask number 113 write 0: no action write 1: mask corresponding event	RW	1
16	XM112	Exception Mask number 112 write 0: no action write 1: mask corresponding event	RW	1
15	XM111	Exception Mask number 111 write 0: no action write 1: mask corresponding event	RW	1
14	XM110	Exception Mask number 110 write 0: no action write 1: mask corresponding event	RW	1
13	XM109	Exception Mask number 109 write 0: no action write 1: mask corresponding event	RW	1
12	XM108	Exception Mask number 108 write 0: no action write 1: mask corresponding event	RW	1
11	XM107	Exception Mask number 107 write 0: no action write 1: mask corresponding event	RW	1
10	XM106	Exception Mask number 106 write 0: no action write 1: mask corresponding event	RW	1
9	XM105	Exception Mask number 105 write 0: no action write 1: mask corresponding event	RW	1
8	XM104	Exception Mask number 104 write 0: no action write 1: mask corresponding event	RW	1

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Bits	Field Name	Description	Type	Reset
7	XM103	Exception Mask number 103 write 0: no action write 1: mask corresponding event	RW	1
6	XM102	Exception Mask number 102 write 0: no action write 1: mask corresponding event	RW	1
5	XM101	Exception Mask number 101 write 0: no action write 1: mask corresponding event	RW	1
4	XM100	Exception Mask number 100 write 0: no action write 1: mask corresponding event	RW	1
3	XM99	Exception Mask number 99 write 0: no action write 1: mask corresponding event	RW	1
2	XM98	Exception Mask number 98 write 0: no action write 1: mask corresponding event	RW	1
1	XM97	Exception Mask number 97 write 0: no action write 1: mask corresponding event	RW	1
0	XM96	Exception Mask number 96 write 0: no action write 1: mask corresponding event	RW	1

Table 5-62. Register Call Summary for Register SYS_INTC_EXPMASK3

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-63. SYS_INTC_MEXPFLAG0

Address Offset	0x0000 00E0		
Physical Address	0x0180 00E0	**Instance**	INTC_DSP
Description	Masked Exception Flag Register 0		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MXF31	MXF30	RESERVED	MXF28	MXF27	MXF26	MXF25	MXF24	MXF23	MXF22	MXF21	MXF20	MXF19	RESERVED	MXF17	MXF16	MXF15	MXF14	MXF13	MXF12	MXF11	MXF10	MXF9	MXF8	MXF7	MXF6	MXF5	MXF4	MXF3	MXF2	MXF1	RESERVED

Bits	Field Name	Description	Type	Reset
31	MXF31	Masked Exception Flag number 31 0: no event occurred 1: an event occurred	R	0
30	MXF30	Masked Exception Flag number 30 0: no event occurred 1: an event occurred	R	0
29	RESERVED	Reserved.	R	0
28	MXF28	Masked Exception Flag number 28 0: no event occurred 1: an event occurred	R	0
27	MXF27	Masked Exception Flag number 27 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
26	MXF26	Masked Exception Flag number 26 0: no event occurred 1: an event occurred	R	0
25	MXF25	Masked Exception Flag number 25 0: no event occurred 1: an event occurred	R	0
24	MXF24	Masked Exception Flag number 24 0: no event occurred 1: an event occurred	R	0
23	MXF23	Masked Exception Flag number 23 0: no event occurred 1: an event occurred	R	0
22	MXF22	Masked Exception Flag number 22 0: no event occurred 1: an event occurred	R	0
21	MXF21	Masked Exception Flag number 21 0: no event occurred 1: an event occurred	R	0
20	MXF20	Masked Exception Flag number 20 0: no event occurred 1: an event occurred	R	0
19	MXF19	Masked Exception Flag number 19 0: no event occurred 1: an event occurred	R	0
18	RESERVED	Reserved.	R	0
17	MXF17	Masked Exception Flag number 17 0: no event occurred 1: an event occurred	R	0
16	MXF16	Masked Exception Flag number 16 0: no event occurred 1: an event occurred	R	0
15	MXF15	Masked Exception Flag number 15 0: no event occurred 1: an event occurred	R	0
14	MXF14	Masked Exception Flag number 14 0: no event occurred 1: an event occurred	R	0
13	MXF13	Masked Exception Flag number 13 0: no event occurred 1: an event occurred	R	0
12	MXF12	Masked Exception Flag number 12 0: no event occurred 1: an event occurred	R	0
11	MXF11	Masked Exception Flag number 11 0: no event occurred 1: an event occurred	R	0
10	MXF10	Masked Exception Flag number 10 0: no event occurred 1: an event occurred	R	0
9	MXF9	Masked Exception Flag number 9 0: no event occurred 1: an event occurred	R	0
8	MXF8	Masked Exception Flag number 8 0: no event occurred 1: an event occurred	R	0
7	MXF7	Masked Exception Flag number 7 0: no event occurred 1: an event occurred	R	0
6	MXF6	Masked Exception Flag number 6 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
5	MXF5	Masked Exception Flag number 5 0: no event occurred 1: an event occurred	R	0
4	MXF4	Masked Exception Flag number 4 0: no event occurred 1: an event occurred	R	0
3	MXF3	Masked Exception Flag number 3 0: no event occurred 1: an event occurred	R	0
2	MXF2	Masked Exception Flag number 2 0: no event occurred 1: an event occurred	R	0
1	MXF1	Masked Exception Flag number 1 0: no event occurred 1: an event occurred	R	0
0	RESERVED	Reserved.	R	0

Table 5-64. Register Call Summary for Register SYS_INTC_MEXPFLAG0

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-65. SYS_INTC_MEXPFLAG1

Address Offset	0x0000 00E4		
Physical Address	0x0180 00E4	**Instance**	INTC_DSP
Description	Masked Exception Flag Register 1		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MXF63	MXF62	MXF61	MXF60	MXF59	MXF58	MXF57	MXF56	MXF55	MXF54	MXF53	MXF52	MXF51	MXF50	MXF49	MXF48	MXF47	MXF46	MXF45	MXF44	MXF43	MXF42	MXF41	MXF40	MXF39	MXF38	MXF37	MXF36	MXF35	MXF34	MXF33	MXF32

Bits	Field Name	Description	Type	Reset
31	MXF63	Masked Exception Flag number 63 0: no event occurred 1: an event occurred	R	0
30	MXF62	Masked Exception Flag number 62 0: no event occurred 1: an event occurred	R	0
29	MXF61	Masked Exception Flag number 61 0: no event occurred 1: an event occurred	R	0
28	MXF60	Masked Exception Flag number 60 0: no event occurred 1: an event occurred	R	0
27	MXF59	Masked Exception Flag number 59 0: no event occurred 1: an event occurred	R	0
26	MXF58	Masked Exception Flag number 58 0: no event occurred 1: an event occurred	R	0
25	MXF57	Masked Exception Flag number 57 0: no event occurred 1: an event occurred	R	0
24	MXF56	Masked Exception Flag number 56 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
23	MXF55	Masked Exception Flag number 55 0: no event occurred 1: an event occurred	R	0
22	MXF54	Masked Exception Flag number 54 0: no event occurred 1: an event occurred	R	0
21	MXF53	Masked Exception Flag number 53 0: no event occurred 1: an event occurred	R	0
20	MXF52	Masked Exception Flag number 52 0: no event occurred 1: an event occurred	R	0
19	MXF51	Masked Exception Flag number 51 0: no event occurred 1: an event occurred	R	0
18	MXF50	Masked Exception Flag number 50 0: no event occurred 1: an event occurred	R	0
17	MXF49	Masked Exception Flag number 49 0: no event occurred 1: an event occurred	R	0
16	MXF48	Masked Exception Flag number 48 0: no event occurred 1: an event occurred	R	0
15	MXF47	Masked Exception Flag number 47 0: no event occurred 1: an event occurred	R	0
14	MXF46	Masked Exception Flag number 46 0: no event occurred 1: an event occurred	R	0
13	MXF45	Masked Exception Flag number 45 0: no event occurred 1: an event occurred	R	0
12	MXF44	Masked Exception Flag number 44 0: no event occurred 1: an event occurred	R	0
11	MXF43	Masked Exception Flag number 43 0: no event occurred 1: an event occurred	R	0
10	MXF42	Masked Exception Flag number 42 0: no event occurred 1: an event occurred	R	0
9	MXF41	Masked Exception Flag number 41 0: no event occurred 1: an event occurred	R	0
8	MXF40	Masked Exception Flag number 40 0: no event occurred 1: an event occurred	R	0
7	MXF39	Masked Exception Flag number 39 0: no event occurred 1: an event occurred	R	0
6	MXF38	Masked Exception Flag number 38 0: no event occurred 1: an event occurred	R	0
5	MXF37	Masked Exception Flag number 37 0: no event occurred 1: an event occurred	R	0
4	MXF36	Masked Exception Flag number 36 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
3	MXF35	Masked Exception Flag number 35 0: no event occurred 1: an event occurred	R	0
2	MXF34	Masked Exception Flag number 34 0: no event occurred 1: an event occurred	R	0
1	MXF33	Masked Exception Flag number 33 0: no event occurred 1: an event occurred	R	0
0	MXF32	Masked Exception Flag number 32 0: no event occurred 1: an event occurred	R	0

Table 5-66. Register Call Summary for Register SYS_INTC_MEXPFLAG1

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- INTC_DSP Register Summary: [0]

Table 5-67. SYS_INTC_MEXPFLAG2

Address Offset	0x0000 00E8		
Physical Address	0x0180 00E8	**Instance**	INTC_DSP
Description	Masked Exception Flag Register 2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MXF95	RESERVED	MXF93	MXF92	MXF91	RESERVED	MXF89	MXF88	MXF87	MXF86	MXF85	MXF84	MXF83	MXF82	MXF81	MXF80	MXF79	MXF78	MXF77	MXF76	MXF75	MXF74	MXF73	MXF72	MXF71	MXF70	MXF69	MXF68	MXF67	MXF66	MXF65	MXF64

Bits	Field Name	Description	Type	Reset
31	MXF95	Masked Exception Flag number 95 0: no event occurred 1: an event occurred	R	0
30	RESERVED	Reserved.	R	0
29	MXF93	Masked Exception Flag number 93 0: no event occurred 1: an event occurred	R	0
28	MXF92	Masked Exception Flag number 92 0: no event occurred 1: an event occurred	R	0
27	MXF91	Masked Exception Flag number 91 0: no event occurred 1: an event occurred	R	0
26	RESERVED	Reserved.	R	0
25	MXF89	Masked Exception Flag number 89 0: no event occurred 1: an event occurred	R	0
24	MXF88	Masked Exception Flag number 88 0: no event occurred 1: an event occurred	R	0
23	MXF87	Masked Exception Flag number 87 0: no event occurred 1: an event occurred	R	0
22	MXF86	Masked Exception Flag number 86 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
21	MXF85	Masked Exception Flag number 85 0: no event occurred 1: an event occurred	R	0
20	MXF84	Masked Exception Flag number 84 0: no event occurred 1: an event occurred	R	0
19	MXF83	Masked Exception Flag number 83 0: no event occurred 1: an event occurred	R	0
18	MXF82	Masked Exception Flag number 82 0: no event occurred 1: an event occurred	R	0
17	MXF81	Masked Exception Flag number 81 0: no event occurred 1: an event occurred	R	0
16	MXF80	Masked Exception Flag number 80 0: no event occurred 1: an event occurred	R	0
15	MXF79	Masked Exception Flag number 79 0: no event occurred 1: an event occurred	R	0
14	MXF78	Masked Exception Flag number 78 0: no event occurred 1: an event occurred	R	0
13	MXF77	Masked Exception Flag number 77 0: no event occurred 1: an event occurred	R	0
12	MXF76	Masked Exception Flag number 76 0: no event occurred 1: an event occurred	R	0
11	MXF75	Masked Exception Flag number 75 0: no event occurred 1: an event occurred	R	0
10	MXF74	Masked Exception Flag number 74 0: no event occurred 1: an event occurred	R	0
9	MXF73	Masked Exception Flag number 73 0: no event occurred 1: an event occurred	R	0
8	MXF72	Masked Exception Flag number 72 0: no event occurred 1: an event occurred	R	0
7	MXF71	Masked Exception Flag number 71 0: no event occurred 1: an event occurred	R	0
6	MXF70	Masked Exception Flag number 70 0: no event occurred 1: an event occurred	R	0
5	MXF69	Masked Exception Flag number 69 0: no event occurred 1: an event occurred	R	0
4	MXF68	Masked Exception Flag number 68 0: no event occurred 1: an event occurred	R	0
3	MXF67	Masked Exception Flag number 67 0: no event occurred 1: an event occurred	R	0
2	MXF66	Masked Exception Flag number 66 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
1	MXF65	Masked Exception Flag number 65 0: no event occurred 1: an event occurred	R	0
0	MXF64	Masked Exception Flag number 64 0: no event occurred 1: an event occurred	R	0

Table 5-68. Register Call Summary for Register SYS_INTC_MEXPFLAG2

DSP Subsystem Register Manual

- INTC_DSP Register Summary: [0]

Table 5-69. SYS_INTC_MEXPFLAG3

Address Offset	0x0000 00EC		
Physical Address	0x0180 00EC	**Instance**	INTC_DSP
Description	Masked Exception Flag Register 3		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MXF127	MXF126	MXF125	MXF124	MXF123	MXF122	MXF121	MXF120	MXF119	MXF118	MXF117	MXF116	MXF115	MXF114	MXF113	MXF112	MXF111	MXF110	MXF109	MXF108	MXF107	MXF106	MXF105	MXF104	MXF103	MXF102	MXF101	MXF100	MXF99	MXF98	MXF97	MXF96

Bits	Field Name	Description	Type	Reset
31	MXF127	Masked Exception Flag number 127 0: no event occurred 1: an event occurred	R	0
30	MXF126	Masked Exception Flag number 126 0: no event occurred 1: an event occurred	R	0
29	MXF125	Masked Exception Flag number 125 0: no event occurred 1: an event occurred	R	0
28	MXF124	Masked Exception Flag number 124 0: no event occurred 1: an event occurred	R	0
27	MXF123	Masked Exception Flag number 123 0: no event occurred 1: an event occurred	R	0
26	MXF122	Masked Exception Flag number 122 0: no event occurred 1: an event occurred	R	0
25	MXF121	Masked Exception Flag number 121 0: no event occurred 1: an event occurred	R	0
24	MXF120	Masked Exception Flag number 120 0: no event occurred 1: an event occurred	R	0
23	MXF119	Masked Exception Flag number 119 0: no event occurred 1: an event occurred	R	0
22	MXF118	Masked Exception Flag number 118 0: no event occurred 1: an event occurred	R	0
21	MXF117	Masked Exception Flag number 117 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
20	MXF116	Masked Exception Flag number 116 0: no event occurred 1: an event occurred	R	0
19	MXF115	Masked Exception Flag number 115 0: no event occurred 1: an event occurred	R	0
18	MXF114	Masked Exception Flag number 114 0: no event occurred 1: an event occurred	R	0
17	MXF113	Masked Exception Flag number 113 0: no event occurred 1: an event occurred	R	0
16	MXF112	Masked Exception Flag number 112 0: no event occurred 1: an event occurred	R	0
15	MXF111	Masked Exception Flag number 111 0: no event occurred 1: an event occurred	R	0
14	MXF110	Masked Exception Flag number 110 0: no event occurred 1: an event occurred	R	0
13	MXF109	Masked Exception Flag number 109 0: no event occurred 1: an event occurred	R	0
12	MXF108	Masked Exception Flag number 108 0: no event occurred 1: an event occurred	R	0
11	MXF107	Masked Exception Flag number 107 0: no event occurred 1: an event occurred	R	0
10	MXF106	Masked Exception Flag number 106 0: no event occurred 1: an event occurred	R	0
9	MXF105	Masked Exception Flag number 105 0: no event occurred 1: an event occurred	R	0
8	MXF104	Masked Exception Flag number 104 0: no event occurred 1: an event occurred	R	0
7	MXF103	Masked Exception Flag number 103 0: no event occurred 1: an event occurred	R	0
6	MXF102	Masked Exception Flag number 102 0: no event occurred 1: an event occurred	R	0
5	MXF101	Masked Exception Flag number 101 0: no event occurred 1: an event occurred	R	0
4	MXF100	Masked Exception Flag number 100 0: no event occurred 1: an event occurred	R	0
3	MXF99	Masked Exception Flag number 99 0: no event occurred 1: an event occurred	R	0
2	MXF98	Masked Exception Flag number 98 0: no event occurred 1: an event occurred	R	0
1	MXF97	Masked Exception Flag number 97 0: no event occurred 1: an event occurred	R	0

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Bits	Field Name	Description	Type	Reset
0	MXF96	Masked Exception Flag number 96 0: no event occurred 1: an event occurred	R	0

Table 5-70. Register Call Summary for Register SYS_INTC_MEXPFLAG3

DSP Subsystem Register Manual
- INTC_DSP Register Summary: [0]

Table 5-71. SYS_INTC_INTMUX1

Address Offset	0x0000 0104		
Physical Address	0x0180 0104	**Instance**	INTC_DSP
Description	Interrupt Mux Register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	INTSEL7							RESERVED	INTSEL6							RESERVED	INTSEL5							RESERVED	INTSEL4						

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved.	R	0
30:24	INTSEL7	Source event number of the CPU interrupt #7	RW	0x07
23	RESERVED	write 0 for further compatibility reads return 0's	RW	0
22:16	INTSEL6	Source event number of the CPU interrupt #6	RW	0x06
15	RESERVED	write 0 for further compatibility reads return 0's	RW	0
14:8	INTSEL5	Source event number of the CPU interrupt #5	RW	0x05
7	RESERVED	write 0 for further compatibility reads return 0's	RW	0
6:0	INTSEL4	Source event number of the CPU interrupt #4	RW	0x04

Table 5-72. Register Call Summary for Register SYS_INTC_INTMUX1

DSP Subsystem Register Manual
- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-73. SYS_INTC_INTMUX2

Address Offset	0x0000 0108		
Physical Address	0x0180 0108	**Instance**	INTC_DSP
Description	Interrupt Mux Register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	INTSEL11							RESERVED	INTSEL10							RESERVED	INTSEL9							RESERVED	INTSEL8						

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved.	R	0
30:24	INTSEL11	Source event number of the CPU interrupt #11	RW	0x0B
23	RESERVED	write 0 for further compatibility reads return 0's	RW	0
22:16	INTSEL10	Source event number of the CPU interrupt #10	RW	0x0A
15	RESERVED	write 0 for further compatibility reads return 0's	RW	0
14:8	INTSEL9	Source event number of the CPU interrupt #9	RW	0x09
7	RESERVED	write 0 for further compatibility reads return 0's	RW	0
6:0	INTSEL8	Source event number of the CPU interrupt #8	RW	0x08

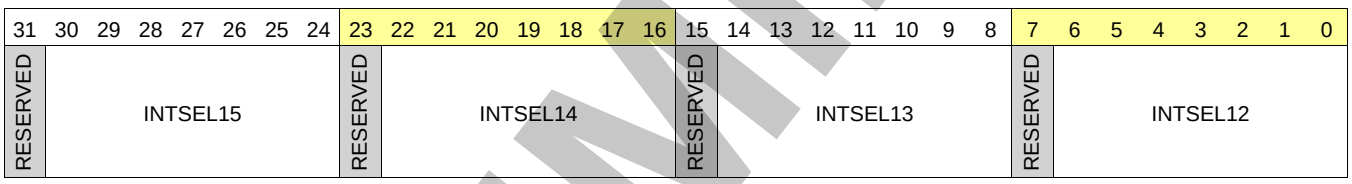
Table 5-74. Register Call Summary for Register SYS_INTC_INTMUX2

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-75. SYS_INTC_INTMUX3

Address Offset	0x0000 010C		
Physical Address	0x0180 010C	**Instance**	INTC_DSP
Description	Interrupt Mux Register 3		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved.	R	0
30:24	INTSEL15	Source event number of the CPU interrupt #15	RW	0x0F
23	RESERVED	write 0 for further compatibility reads return 0's	RW	0
22:16	INTSEL14	Source event number of the CPU interrupt #14	RW	0x0E
15	RESERVED	write 0 for further compatibility reads return 0's	RW	0
14:8	INTSEL13	Source event number of the CPU interrupt #13	RW	0x0D
7	RESERVED	write 0 for further compatibility reads return 0's	RW	0
6:0	INTSEL12	Source event number of the CPU interrupt #12	RW	0x0C

Table 5-76. Register Call Summary for Register SYS_INTC_INTMUX3

DSP Subsystem Register Manual

- DSP Subsystem Logical Register Mapping: [0]
- INTC_DSP Register Summary: [1]

Table 5-77. SYS_INTC_AEGMUX0

Address Offset	0x0000 0140		
Physical Address	0x0180 0140	**Instance**	INTC_DSP
Description	AEG Mux Register 0		
Type	RW		

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
AEGSEL3	AEGSEL2	AEGSEL1	AEGSEL0

Bits	Field Name	Description	Type	Reset
31:24	AEGSEL3	Source for Advanced Emulation Event #3	RW	0x03
23:16	AEGSEL2	Source for Advanced Emulation Event #2	RW	0x02
15:8	AEGSEL1	Source for Advanced Emulation Event #1	RW	0x01
7:0	AEGSEL0	Source for Advanced Emulation Event #0	RW	0x00

Table 5-78. Register Call Summary for Register SYS_INTC_AEGMUX0

DSP Subsystem Register Manual
- INTC_DSP Register Summary: [0]

Table 5-79. SYS_INTC_AEGMUX1

Address Offset	0x0000 0144		
Physical Address	0x0180 0144	**Instance**	INTC_DSP
Description	AEG Mux Register 1		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
AEGSEL7	AEGSEL6	AEGSEL5	AEGSEL4

Bits	Field Name	Description	Type	Reset
31:24	AEGSEL7	Source for Advanced Emulation Event #7	RW	0x07
23:16	AEGSEL6	Source for Advanced Emulation Event #6	RW	0x06
15:8	AEGSEL5	Source for Advanced Emulation Event #5	RW	0x05
7:0	AEGSEL4	Source for Advanced Emulation Event #4	RW	0x04

Table 5-80. Register Call Summary for Register SYS_INTC_AEGMUX1

DSP Subsystem Register Manual
- INTC_DSP Register Summary: [0]

Table 5-81. SYS_INTC_INTXSTAT

Address Offset	0x0000 0180		
Physical Address	0x0180 0180	**Instance**	INTC_DSP
Description	Interrupt Exception Status Register		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
SYSINT	CPUINT	RESERVED	DROP

Bits	Field Name	Description	Type	Reset
31:24	SYSINT	System Event number 0x0: EVT0 .... 0x7F: EVT128 others: reserved	R	0x00

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Bits	Field Name	Description	Type	Reset
23:16	CPUINT	CPU interrupt number 0x0: CPUINT0 ... 0xF: CPUINT15 others: reserved	R	0x00
15:1	RESERVED	reserved reads return 0's	R	0x0000
0	DROP	Dropped event flag 0: No events dropped 1: Event was dropped by the CPU	R	0

Table 5-82. Register Call Summary for Register SYS_INTC_INTXSTAT

DSP Subsystem Programming Guide • Interrupt Exception Programming Sequence: [0] [1] [2]
DSP Subsystem Register Manual • INTC_DSP Register Summary: [3]

Table 5-83. SYS_INTC_INTXCLR

Address Offset	0x0000 0184		
Physical Address	0x0180 0184	**Instance**	INTC_DSP
Description	Interrupt Exception Clear Register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLEAR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	write 0 for further compatibility	W	0x0000 0000
0	CLEAR	Interrupt exception status clear register: write 0: no effect write 1: clears the Interrupt Exception Status register	W	0

Table 5-84. Register Call Summary for Register SYS_INTC_INTXCLR

DSP Subsystem Programming Guide • Interrupt Exception Programming Sequence: [0] [1]
DSP Subsystem Register Manual • INTC_DSP Register Summary: [2]

Table 5-85. SYS_INTC_INTDMASK

Address Offset	0x0000 0188		
Physical Address	0x0180 0188	**Instance**	INTC_DSP
Description	Dropped Interrupt Mask Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																IDM15	IDM14	IDM13	IDM12	IDM11	IDM10	IDM9	IDM8	IDM7	IDM6	IDM5	IDM4	RESERVED			

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved.	R	0x0000
15	IDM15	Dropped event mask for CPU interrupt #15	RW	0
14	IDM14	Dropped event mask for CPU interrupt #14	RW	0
13	IDM13	Dropped event mask for CPU interrupt #13	RW	0
12	IDM12	Dropped event mask for CPU interrupt #12	RW	0
11	IDM11	Dropped event mask for CPU interrupt #11	RW	0
10	IDM10	Dropped event mask for CPU interrupt #10	RW	0
9	IDM9	Dropped event mask for CPU interrupt #9	RW	0
8	IDM8	Dropped event mask for CPU interrupt #8	RW	0
7	IDM7	Dropped event mask for CPU interrupt #7	RW	0
6	IDM6	Dropped event mask for CPU interrupt #6	RW	0
5	IDM5	Dropped event mask for CPU interrupt #5	RW	0
4	IDM4	Dropped event mask for CPU interrupt #4	RW	0
3:0	RESERVED	Reserved.	R	0x0

Table 5-86. Register Call Summary for Register SYS_INTC_INTDMASK

DSP Subsystem Functional Description • Event Behavior: [0]
DSP Subsystem Programming Guide • Interrupt Exception Programming Sequence: [1] • INTC Basic Programming Model for Power On of DSP Subsystem: [2] [3]
DSP Subsystem Register Manual • INTC_DSP Register Summary: [4]

Table 5-87. SYS_INTC_EVTASRT

Address Offset	0x0000 01C0		
Physical Address	0x0180 01C0	**Instance**	INTC_DSP
Description	Event Assert Register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MXF7	MXF6	MXF5	MXF4	MXF3	MXF2	MXF1	MXF0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved.	R	0x000000
7	MXF7	Event Assert output #7 EA7 = 0: No effect EA7 = 1: EVTOUT7 pulsed high for 4 clk1 cycles, then low.	W	0
6	MXF6	Event Assert output #6 EA6 = 0: No effect EA6 = 1: EVTOUT6 pulsed high for 4 clk1 cycles, then low.	W	0
5	MXF5	Event Assert output #5 EA5 = 0: No effect EA5 = 1: EVTOUT5 pulsed high for 4 clk1 cycles, then low.	W	0
4	MXF4	Event Assert output #4 EA4 = 0: No effec EA4 = 1: EVTOUT4 pulsed high for 4 clk1 cycles, then low.	W	0

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Bits	Field Name	Description	Type	Reset
3	MXF3	Event Assert output #3 EA3 = 0: No effect EA3 = 1: EVTOUT3 pulsed high for 4 clk1 cycles, then low.	W	0
2	MXF2	Event Assert output #2 EA2 = 0: No effect EA2 = 1: EVTOUT2 pulsed high for 4 clk1 cycles, then low.	W	0
1	MXF1	Event Assert output #1 EA1 = 0: No effect EA1 = 1: EVTOUT1 pulsed high for 4 clk1 cycles, then low.	W	0
0	MXF0	Event Assert output #0 EA0 = 0: No effect EA0 = 1: EVTOUT0 pulsed high for 4 clk1 cycles, then low.	W	0

Table 5-88. Register Call Summary for Register SYS_INTC_EVTASRT

DSP Subsystem Register Manual
- INTC_DSP Register Summary: [0]

5.5.4 PDC Registers

5.5.4.1 PDC Register Summary

Table 5-89. PDC Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PDC Physical Address
SYS_PD_PDCCMD	RW	32	0x0000 0000	0x0181 0000
RESERVED (1)	R	32	0x0000 1000 + (0x4 * i)	0x0181 1000 + (0x4 * i)
SYS_PD_REVID	R	32	0x0000 2000	0x0181 2000

(1) i = 0 to 7

5.5.4.2 PDC Register Description

Table 5-90. SYS_PD_PDCCMD

Address Offset	0x0000 0000		
Physical Address	0x0181 0000	**Instance**	PDC
Description	Power-Down Command Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															GEMPD	EMCMEM		EMCLOG		UMCMEM		UMCLOG		DMCMEM		DMCLOG		PMCMEM		PMCLOG	

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Reserved.	R	0x0000
16	GEMPD	Power-down during IDLE: GEMPD = 0: Normal operation. Do not power-down CPU or GEM when CPU is IDLE. GEMPD = 1: Sleep mode. Power-down CPU and GEM when CPU enters IDLE state	RW	0

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Bits	Field Name	Description	Type	Reset
15:14	EMCMEM	SRAM Sleep Modes Determines the RAM sleep modes used by the EMC for powering-down internal memories. 0x0: No sleep mode supported 0x1: Sleep mode 1 Write 0x2: Sleep mode 2 - equivalent to sleep mode 1 Write 0x3: Sleep mode 3 - equivalent to sleep mode 1	RW	0x1
13:12	EMCLOG	Logic Clock Gating Modes. Determines to what degree the EMC gates its clock internally. 0x0: No clock gating supported beyond leaf clock gating. 0x1: Static clock gating of unused modules regions when GEM is active (pmc_pd_pdstat[1:0] = 00) and Static clock gating when GEM is in standby (pmc_pd_pdstat[1:0] = 11)	RW	0x1
11:10	UMCMEM	SRAM Sleep Modes Determines the RAM sleep modes used by the UMC for powering-down L2 pages. 0x0: No sleep mode supported 0x1: Sleep mode 1 Write 0x2: Sleep mode 2 - equivalent to sleep mode 1 Write 0x3: Sleep mode 3 - equivalent to sleep mode 1	RW	0x1
9:8	UMCLOG	Logic Clock Gating Modes. Determines to what degree the UMC gates its clock internally. 0x0: No clock gating supported beyond leaf clock gating. 0x1: Static clock gating of unused modules regions when GEM is active (pmc_pd_pdstat[1:0] = 00) and Static clock gating when GEM is in standby (pmc_pd_pdstat[1:0] = 11)	RW	0x1
7:6	DMCMEM	SRAM Sleep Modes Determines the RAM sleep modes used by the DMC for powering-down L1D pages. 0x0: No sleep mode supported 0x1: Sleep mode 1 Write 0x2: Sleep mode 2 - equivalent to sleep mode 1 Write 0x3: Sleep mode 3 - equivalent to sleep mode 1	RW	0x1
5:4	DMCLOG	Logic Clock Gating Modes. Determines to what degree the DMC gates its clock internally. 0x0: No clock gating supported beyond leaf clock gating. 0x1: Static clock gating of unused modules regions when GEM is active (pmc_pd_pdstat[1:0] = 00) and Static clock gating when GEM is in standby (pmc_pd_pdstat[1:0] = 11)	RW	0x1
3:2	PMCMEM	SRAM Sleep Modes Determines the RAM sleep modes used by the PMC for powering-down L1P pages. 0x0: No sleep mode supported 0x1: Sleep mode 1 Write 0x2: Sleep mode 2 - equivalent to sleep mode 1 Write 0x3: Sleep mode 3 - equivalent to sleep mode 1	RW	0x1
1:0	PMCLOG	Logic Clock Gating Modes. Determines to what degree the PMC gates its clock internally. 0x0: No clock gating supported beyond leaf clock gating. 0x1: Static clock gating of unused modules regions when GEM is active (pmc_pd_pdstat[1:0] = 00) and Static clock gating when GEM is in standby (pmc_pd_pdstat[1:0] = 11)	RW	0x1

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Table 5-91. Register Call Summary for Register SYS_PD_PDCCMD

DSP Subsystem Programming Guide • Power Down and Wakeup Management: [0] [1] [2] [3] [4] [5] [6] [7] [8]
DSP Subsystem Register Manual • PDC Register Summary: [9]

Table 5-92. SYS_PD_REVID

Address Offset	0x0000 2000		
Physical Address	0x0181 2000	**Instance**	PDC
Description	GEM Revision ID Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	0x- TI internal data

Table 5-93. Register Call Summary for Register SYS_PD_REVID

DSP Subsystem Register Manual • PDC Register Summary: [0]

5.5.5 EDM Registers

5.5.5.1 EDM Register Summary

Table 5-94. EDM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EDM Physical Address
EDM_IAR_ADD	RW	32	0x0000 0020	0x01BC 0020
EDM_IAR_DAT	RW	32	0x0000 0024	0x01BC 0024
EDM_DP_EVT	RW	32	0x0000 0028	0x01BC 0028
EDM_DP_PID	RW	32	0x0000 002C	0x01BC 002C
EDM_DP_PC	R	32	0x0000 0030	0x01BC 0030

5.5.5.2 EDM Register Description

Table 5-95. EDM_IAR_ADD

Address Offset	0x0000 0020		
Physical Address	0x01BC 0020	**Instance**	EDM
Description	Indirect Register Acces		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBEND	RESERVED									RREND	RESERVED													ADRS							

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Bits	Field Name	Description	Type	Reset
31	RBEND	A one results the Breakpoint End(BEND) status. A zero causes no action.	RW	0
30:22	RESERVED	Reserved.	R	0x000
21	RREND	A one resets the RTOSS Int (AINT) End (RREND) status. A zero causes no action	RW	0
20:10	RESERVED	Reserved.	R	0x000
9:0	ADRS	This 10-bit value creates the indirect register address.	RW	0x000

Table 5-96. Register Call Summary for Register EDM_IAR_ADD

DSP Subsystem Register Manual
- EDM Register Summary: [0]

Table 5-97. EDM_IAR_DAT

Address Offset	0x0000 0024		
Physical Address	0x01BC 0024	**Instance**	EDM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	Read: Indirectly Addressable Register Read Data. Write: Indirectly Addressable Register Write Data.	RW	0x0000 0000

Table 5-98. Register Call Summary for Register EDM_IAR_DAT

DSP Subsystem Register Manual
- EDM Register Summary: [0]

Table 5-99. EDM_DP_EVT

Address Offset	0x0000 0028		
Physical Address	0x01BC 0028	**Instance**	EDM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CEE				CSE				CCE				CAE				CBE															

Bits	Field Name	Description	Type	Reset
31:28	CEE	Reserved for Extra Events	RW	0x0
27:24	CSE	State Events	RW	0x0
23:20	CCE	Counter Events	RW	0x0
19:16	CAE	Auxiliary Events	RW	0x0
15:0	CBE	Bus Events	RW	0x0000

Table 5-100. Register Call Summary for Register EDM_DP_EVT

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- EDM Register Summary: [0]

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Table 5-101. EDM_DP_PID

Address Offset	0x0000 002C		
Physical Address	0x01BC 002C	**Instance**	EDM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DP_AOWN	RESERVED															REVISION														DP_STATE	

Bits	Field Name	Description	Type	Reset
31	DP_AOWN	Ownership 0x0: Debug owned 0x1: Application owned	RW	0
30:16	RESERVED	Reserved.	R	0x0000
15:2	REVISION	Revision ID	R	0x- TI internal data
1:0	DP_STATE	State 0x0: AVAIL state 0x1: APP CLAIMor DBG CLAIM 0x2: APP ENA or DBG ENA	RW	0x0

Table 5-102. Register Call Summary for Register EDM_DP_PID

DSP Subsystem Register Manual
- EDM Register Summary: [0]

Table 5-103. EDM_DP_PC

Address Offset	0x0000 0030		
Physical Address	0x01BC 0030	**Instance**	EDM
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPC																															

Bits	Field Name	Description	Type	Reset
31:0	CPC	Current CPU PC	R	0x0000 0000

Table 5-104. Register Call Summary for Register EDM_DP_PC

DSP Subsystem Register Manual
- EDM Register Summary: [0]

5.5.6 TPCC Registers

5.5.6.1 TPCC Register Summary

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Table 5-105. TPCC Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TPCC Physical Address
TPCC_PID	R	32	0x0000 0000	0x01C0 0000
TPCC_CCCFG	R	32	0x0000 0004	0x01C0 0004
TPCC_CLKGDIS	RW	32	0x0000 00FC	0x01C0 00FC
TPCC_DCHMAPN_i (1)	RW	32	0x0000 0100 + (0x4 * i)	0x01C0 0100 + (0x4 * i)
TPCC_QCHMAPN_j (3)	RW	32	0x0000 0200 + (0x4 * j)	0x01C0 0200 + (0x4 * j)
TPCC_DMAQNUM_n (6)	RW	32	0x0000 0240 + (0x4 * n)	0x01C0 0240 + (0x4 * n)
TPCC_QDMAQNUM	RW	32	0x0000 0260	0x01C0 0260
TPCC_QUETCMAP	RW	32	0x0000 0280	0x01C0 0280
TPCC_QUEPRI	RW	32	0x0000 0284	0x01C0 0284
TPCC_EMR	R	32	0x0000 0300	0x01C0 0300
TPCC_EMRH	R	32	0x0000 0304	0x01C0 0304
TPCC_EMCR	W	32	0x0000 0308	0x01C0 0308
TPCC_EMCRH	W	32	0x0000 030C	0x01C0 030C
TPCC_QEMR	R	32	0x0000 0310	0x01C0 0310
TPCC_QEMCR	W	32	0x0000 0314	0x01C0 0314
TPCC_CCERR	R	32	0x0000 0318	0x01C0 0318
TPCC_CCERRCLR	W	32	0x0000 031C	0x01C0 031C
TPCC_EEVAL	W	32	0x0000 0320	0x01C0 0320
TPCC_DRAEM_k (2)	RW	32	0x0000 0340 + (0x8 * k)	0x01C0 0340 + (0x8 * k)
TPCC_DRAEHM_k (2)	RW	32	0x0000 0344 + (0x8 * k)	0x01C0 0344 + (0x8 * k)
TPCC_QRAEM_k (2)	RW	32	0x0000 0380 + (0x4 * k)	0x01C0 0380 + (0x4 * k)
TPCC_Q0E_o (7)	R	32	0x0000 0400 + (0x4 * o)	0x01C0 0400 + (0x4 * o)
TPCC_Q1E_o (7)	R	32	0x0000 0440 + (0x4 * o)	0x01C0 0440 + (0x4 * o)
TPCC_QSTATN_l (5)	R	32	0x0000 0600 + (0x4 * l)	0x01C0 0600 + (0x4 * l)
TPCC_QWMTHRA	RW	32	0x0000 0620	0x01C0 0620
TPCC_QWMTHRB	RW	32	0x0000 0624	0x01C0 0624
TPCC_CCSTAT	R	32	0x0000 0640	0x01C0 0640
TPCC_AETCTL	RW	32	0x0000 0700	0x01C0 0700
TPCC_AETSTAT	R	32	0x0000 0704	0x01C0 0704
TPCC_AETCMD	W	32	0x0000 0708	0x01C0 0708
RESERVED	R	32	0x0000 0800	0x01C0 0800
RESERVED	R	32	0x0000 0804	0x01C0 0804
RESERVED	W	32	0x0000 0808	0x01C0 0808
RESERVED	RW	32	0x0000 080C	0x01C0 080C
RESERVED	RW	32	0x0000 0810	0x01C0 0810
TPCC_ER	R	32	0x0000 1000	0x01C0 1000
TPCC_ERH	R	32	0x0000 1004	0x01C0 1004
TPCC_ECR	W	32	0x0000 1008	0x01C0 1008
TPCC_ECRH	W	32	0x0000 100C	0x01C0 100C
TPCC_ESR	W	32	0x0000 1010	0x01C0 1010
TPCC_ESRH	W	32	0x0000 1014	0x01C0 1014
TPCC_CER	R	32	0x0000 1018	0x01C0 1018
TPCC_CERH	R	32	0x0000 101C	0x01C0 101C
TPCC_EER	R	32	0x0000 1020	0x01C0 1020
TPCC_EERH	R	32	0x0000 1024	0x01C0 1024
TPCC_EECR	W	32	0x0000 1028	0x01C0 1028

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Table 5-105. TPCC Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	TPCC Physical Address
TPCC_EECRH	W	32	0x0000 102C	0x01C0 102C
TPCC_EESR	W	32	0x0000 1030	0x01C0 1030
TPCC_EESRH	W	32	0x0000 1034	0x01C0 1034
TPCC_SER	R	32	0x0000 1038	0x01C0 1038
TPCC_SERH	R	32	0x0000 103C	0x01C0 103C
TPCC_SECR	W	32	0x0000 1040	0x01C0 1040
TPCC_SECRH	W	32	0x0000 1044	0x01C0 1044
TPCC_IER	R	32	0x0000 1050	0x01C0 1050
TPCC_IERH	R	32	0x0000 1054	0x01C0 1054
TPCC_IECR	W	32	0x0000 1058	0x01C0 1058
TPCC_IECRH	W	32	0x0000 105C	0x01C0 105C
TPCC_IESR	W	32	0x0000 1060	0x01C0 1060
TPCC_IESRH	W	32	0x0000 1064	0x01C0 1064
TPCC_IPR	R	32	0x0000 1068	0x01C0 1068
TPCC_IPRH	R	32	0x0000 106C	0x01C0 106C
TPCC_ICR	W	32	0x0000 1070	0x01C0 1070
TPCC_ICRH	W	32	0x0000 1074	0x01C0 1074
TPCC_IEVAL	W	32	0x0000 1078	0x01C0 1078
TPCC_QER	R	32	0x0000 1080	0x01C0 1080
TPCC_QEER	R	32	0x0000 1084	0x01C0 1084
TPCC_QEECR	W	32	0x0000 1088	0x01C0 1088
TPCC_QEESR	W	32	0x0000 108C	0x01C0 108C
TPCC_QSER	R	32	0x0000 1090	0x01C0 1090
TPCC_QSECR	W	32	0x0000 1094	0x01C0 1094
TPCC_ER_RN_k (2)	R	32	0x0000 2000 + (0x200 * k)	0x01C0 2000 + (0x200 * k)
TPCC_ERH_RN_k (2)	R	32	0x0000 2004 + (0x200 * k)	0x01C0 2004 + (0x200 * k)
TPCC_ECR_RN_k (2)	W	32	0x0000 2008 + (0x200 * k)	0x01C0 2008 + (0x200 * k)
TPCC_ECRH_RN_k (2)	W	32	0x0000 200C + (0x200 * k)	0x01C0 200C + (0x200 * k)
TPCC_ESR_RN_k (2)	W	32	0x0000 2010 + (0x200 * k)	0x01C0 2010 + (0x200 * k)
TPCC_ESRH_RN_k (2)	W	32	0x0000 2014 + (0x200 * k)	0x01C0 2014 + (0x200 * k)
TPCC_CER_RN_k (2)	R	32	0x0000 2018 + (0x200 * k)	0x01C0 2018 + (0x200 * k)
TPCC_CERH_RN_k (2)	R	32	0x0000 201C + (0x200 * k)	0x01C0 201C + (0x200 * k)
TPCC_EER_RN_k (2)	R	32	0x0000 2020 + (0x200 * k)	0x01C0 2020 + (0x200 * k)
TPCC_EERH_RN_k (2)	R	32	0x0000 2024 + (0x200 * k)	0x01C0 2024 + (0x200 * k)
TPCC_EECR_RN_k (2)	W	32	0x0000 2028 + (0x200 * k)	0x01C0 2028 + (0x200 * k)
TPCC_EECRH_RN_k (2)	W	32	0x0000 202C + (0x200 * k)	0x01C0 202C + (0x200 * k)
TPCC_EESR_RN_k (2)	W	32	0x0000 2030 + (0x200 * k)	0x01C0 2030 + (0x200 * k)
TPCC_EESRH_RN_k (2)	W	32	0x0000 2034 + (0x200 * k)	0x01C0 2034 + (0x200 * k)
TPCC_SER_RN_k (2)	R	32	0x0000 2038 + (0x200 * k)	0x01C0 2038 + (0x200 * k)
TPCC_SERH_RN_k (2)	R	32	0x0000 203C + (0x200 * k)	0x01C0 203C + (0x200 * k)
TPCC_SECR_RN_k (2)	W	32	0x0000 2040 + (0x200 * k)	0x01C0 2040 + (0x200 * k)
TPCC_SECRH_RN_k (2)	W	32	0x0000 2044 + (0x200 * k)	0x01C0 2044 + (0x200 * k)
TPCC_IER_RN_k (2)	R	32	0x0000 2050 + (0x200 * k)	0x01C0 2050 + (0x200 * k)
TPCC_IERH_RN_k (2)	R	32	0x0000 2054 + (0x200 * k)	0x01C0 2054 + (0x200 * k)

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Table 5-105. TPCC Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	TPCC Physical Address
TPCC_IECR_RN_k (2)	W	32	0x0000 2058 + (0x200 * k)	0x01C0 2058 + (0x200 * k)
TPCC_IECRH_RN_k (2)	W	32	0x0000 205C + (0x200 * k)	0x01C0 205C + (0x200 * k)
TPCC_IESR_RN_k (2)	W	32	0x0000 2060 + (0x200 * k)	0x01C0 2060 + (0x200 * k)
TPCC_IESRH_RN_k (2)	W	32	0x0000 2064 + (0x200 * k)	0x01C0 2064 + (0x200 * k)
TPCC_IPR_RN_k (2)	R	32	0x0000 2068 + (0x200 * k)	0x01C0 2068 + (0x200 * k)
TPCC_IPRH_RN_k (2)	R	32	0x0000 206C + (0x200 * k)	0x01C0 206C + (0x200 * k)
TPCC_ICR_RN_k (2)	W	32	0x0000 2070 + (0x200 * k)	0x01C0 2070 + (0x200 * k)
TPCC_ICRH_RN_k (2)	W	32	0x0000 2074 + (0x200 * k)	0x01C0 2074 + (0x200 * k)
TPCC_IEVAL_RN_k (2)	W	32	0x0000 2078 + (0x200 * k)	0x01C0 2078 + (0x200 * k)
TPCC_QER_RN_k (2)	R	32	0x0000 2080 + (0x200 * k)	0x01C0 2080 + (0x200 * k)
TPCC_QEER_RN_k (2)	R	32	0x0000 2084 + (0x200 * k)	0x01C0 2084 + (0x200 * k)
TPCC_QEECR_RN_k (2)	W	32	0x0000 2088 + (0x200 * k)	0x01C0 2088 + (0x200 * k)
TPCC_QEESR_RN_k (2)	W	32	0x0000 208C + (0x200 * k)	0x01C0 208C + (0x200 * k)
TPCC_QSER_RN_k (2)	R	32	0x0000 2090 + (0x200 * k)	0x01C0 2090 + (0x200 * k)
TPCC_QSECR_RN_k (2)	W	32	0x0000 2094 + (0x200 * k)	0x01C0 2094 + (0x200 * k)
TPCC_OPT_m (4)	RW	32	0x0000 4000 + (0x20 * m)	0x01C0 4000 + (0x20 * m)
TPCC_SRC_m (4)	RW	32	0x0000 4004 + (0x20 * m)	0x01C0 4004 + (0x20 * m)
TPCC_ABCNT_m (4)	RW	32	0x0000 4008 + (0x20 * m)	0x01C0 4008 + (0x20 * m)
TPCC_DST_m (4)	RW	32	0x0000 400C + (0x20 * m)	0x01C0 400C + (0x20 * m)
TPCC_BIDX_m (4)	RW	32	0x0000 4010 + (0x20 * m)	0x01C0 4010 + (0x20 * m)
TPCC_LNK_m (4)	RW	32	0x0000 4014 + (0x20 * m)	0x01C0 4014 + (0x20 * m)
TPCC_CIDX_m (4)	RW	32	0x0000 4018 + (0x20 * m)	0x01C0 4018 + (0x20 * m)
TPCC_CCNT_m (4)	RW	32	0x0000 401C + (0x20 * m)	0x01C0 401C + (0x20 * m)

(1) i = 0 to 63
(2) k = 0 to 7
(3) j = 0 to 3
(4) m = 0 to 127
(5) l = 0 to 1
(6) n = 0 to 7
(7) o = 0 to 15

5.5.6.2 TPCC Register Description

Table 5-106. TPCC_PID

Address Offset	0x0000 0000		
Physical Address	0x01C0 0000	**Instance**	TPCC
Description	Peripheral ID Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
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Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	0x- TI internal data

Table 5-107. Register Call Summary for Register TPCC_PID

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-108. TPCC_CCCFG

Address Offset	0x0000 0004		
Physical Address	0x01C0 0004	**Instance**	TPCC
Description	CC Configuration Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						MPEXIST	CHMAPEXIST	RESERVED		NUMREGN		RESERVED	NUMTC			RESERVED	NUMPAENTRY			RESERVED	NUMINTCH			RESERVED	NUMQDMACH			RESERVED	NUMDMACH		

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	reads return 0's	R	0x00
25	MPEXIST	Memory Protection Existence 0 : No memory protection. 1 : Memory Protection logic included.	R	0
24	CHMAPEXIST	Channel Mapping Existence 0 : No Channel mapping. 1 : Channel mapping logic included.	R	1
23:22	RESERVED	reads return 0's	R	0x0
21:20	NUMREGN	Number of MP and Shadow regions Read 0x0: 0 Regions Read 0x1: 2 Regions Read 0x2: 4 Regions Read 0x3: 8 Regions	R	0x3
19	RESERVED	reads return 0's	R	0
18:16	NUMTC	Number of Queues/Number of TCs Read 0x0: 1 TC/Event Queue Read 0x1: 2 TC/Event Queue Read 0x2: 3 TC/Event Queue Read 0x3: 4 TC/Event Queue Read 0x4: 5 TC/Event Queue Read 0x5: 6 TC/Event Queue Read 0x6: 7 TC/Event Queue Read 0x7: 8 TC/Event Queue	R	0x1
15	RESERVED	reads return 0's	R	0

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Bits	Field Name	Description	Type	Reset
14:12	NUMPAENTRY	Number of PaRAM entries Read 0x0: 16 entries Read 0x1: 32 entries (unsupported setting) Read 0x2: 64 entries Read 0x3: 128 entries Read 0x4: 256 entries Read 0x5: 512 entries	R	0x3
11	RESERVED	reads return 0's	R	0
10:8	NUMINTCH	Number of Interrupt Channels Read 0x1: 8 Interrupt channels Read 0x2: 16 Interrupt channels Read 0x3: 32 Interrupt channels Read 0x4: 64 Interrupt channels	R	0x4
7	RESERVED	reads return 0's	R	0
6:4	NUMQDMACH	Number of QDMA Channels Read 0x0: No QDMA Channels Read 0x1: 2 QDMA Channels Read 0x2: 4 QDMA Channels Read 0x3: 6 QDMA Channels Read 0x4: 8 QDMA Channels	R	0x4
3	RESERVED	reads return 0's	R	0
2:0	NUMDMACH	Number of DMA Channels Read 0x0: No DMA Channels Read 0x1: 4 DMA Channels Read 0x2: 8 DMA Channels Read 0x3: 16 DMA Channels Read 0x4: 32 DMA Channels Read 0x5: 64 DMA Channels	R	0x5

Table 5-109. Register Call Summary for Register TPCC_CCCFG

DSP Subsystem Register Manual

- TPCC Register Summary: [0]

Table 5-110. TPCC_CLKGDIS

Address Offset	0x0000 00FC		
Physical Address	0x01C0 00FC	**Instance**	TPCC
Description	Auto Clock Gate Disable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLKGDIS

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0000 0000
0	CLKGDIS	Auto Clock Gate Disable	RW	0

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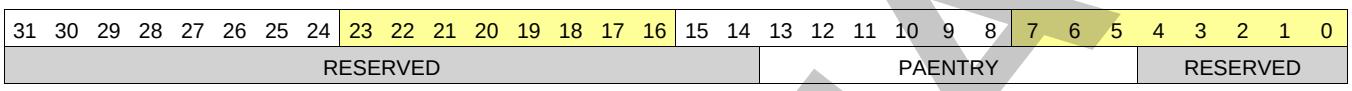
Table 5-111. Register Call Summary for Register TPCC_CLKGDIS

DSP Subsystem Programming Guide
- Clock Gating: [0] [1]

DSP Subsystem Register Manual
- TPCC Register Summary: [2]

Table 5-112. TPCC_DCHMAPN_i

Address Offset	0x0000 0100 + (0x4 * i)		
Physical Address	0x01C0 0100 + (0x4 * i)	**Instance**	TPCC
Description	DMA Channel N Mapping Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:14	RESERVED	write 0's for future compatibility reads return 0's	RW	0x00000
13:5	PAENTRY	PaRAM Entry number for DMA Channel N.	RW	0x000
4:0	RESERVED	write 0's for future compatibility reads return 0's	RW	0x00

Table 5-113. Register Call Summary for Register TPCC_DCHMAPN_i

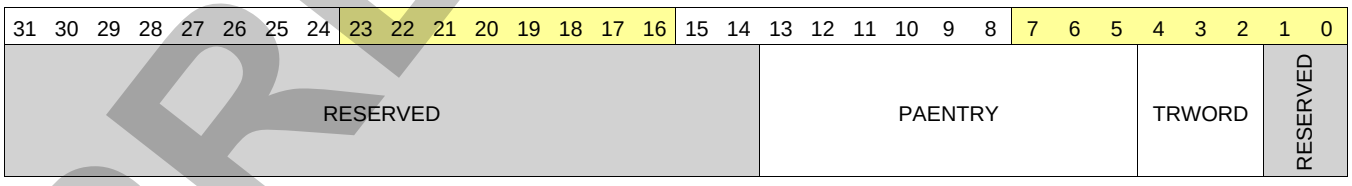
DSP Subsystem Functional Description
- DMA/QDMA Channel Mapping and PaRAM Entry: [0] [1]

DSP Subsystem Programming Guide
- Assigning a Logical Channel to a Trigger Event: [2]
- Manual Trigger (Software-Synchronized Transfers): [3]
- Hardware Trigger (Hardware-Synchronized Transfers): [4]

DSP Subsystem Register Manual
- TPCC Register Summary: [5]

Table 5-114. TPCC_QCHMAPN_j

Address Offset	0x0000 0200 + (0x4 * j)		
Physical Address	0x01C0 0200 + (0x4 * j)	**Instance**	TPCC
Description	QDMA Channel N Mapping Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:14	RESERVED	write 0's for future compatibility reads return 0's	RW	0x00000
13:5	PAENTRY	PaRAM Entry number for QDMA Channel N.	RW	0x000
4:2	TRWORD	TRWORD points to the specific trigger word of the PaRAM Entry defined by PAENTRY. A write to the trigger word results in a QDMA Event being recognized.	RW	0x0
1:0	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0

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Table 5-115. Register Call Summary for Register TPCC_QCHMAPN_j

DSP Subsystem Functional Description
- DMA Versus QDMA: [0] [1]
- DMA/QDMA Channel Mapping and PaRAM Entry: [2] [3] [4]

DSP Subsystem Programming Guide
- Assigning a Logical Channel to a Trigger Event: [5]
- Automatic Trigger (QDMA): [6]

DSP Subsystem Register Manual
- TPCC Register Summary: [7]
- TPCC Register Description: [8] [9]

Table 5-116. TPCC_DMAQNUM_n

Address Offset	0x0000 0240 + (0x4 * n)		
Physical Address	0x01C0 0240 + (0x4 * n)	**Instance**	TPCC
Description	DMA Queue Number Register n contains the Event queue number to be used for the corresponding DMA Channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			E7	RESERVED			E6	RESERVED			E5	RESERVED			E4	RESERVED			E3	RESERVED			E2	RESERVED			E1	RESERVED			E0

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
28	E7	DMA Queue Number for event #(8 * n + 7) 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
27:25	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
24	E6	DMA Queue Number for event #(8 * n + 6) 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
20	E5	DMA Queue Number for event #(8 * n + 5) 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
19:17	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
16	E4	DMA Queue Number for event #(8 * n + 4) 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
15:13	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
12	E3	DMA Queue Number for event #(8 * n + 3) 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
11:9	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
8	E2	DMA Queue Number for event #(8 * n + 2) 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	E1	DMA Queue Number for event #(8 * n + 1) 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
3:1	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
0	E0	DMA Queue Number for event #(8 * n + 0) 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0

Table 5-117. Register Call Summary for Register TPCC_DMAQNUM_n

DSP Subsystem Programming Guide
- Mapping Between DMA/QDMA Events and Event Queues: [0]

DSP Subsystem Register Manual
- TPCC Register Summary: [1]

Table 5-118. TPCC_QDMAQNUM

Address Offset	0x0000 0260		
Physical Address	0x01C0 0260	**Instance**	TPCC
Description	QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			E7	RESERVED			E6	RESERVED			E5	RESERVED			E4	RESERVED			E3	RESERVED			E2	RESERVED			E1	RESERVED			E0

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	R	0x0
28	E7	QDMA Queue Number for event #7 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
27:25	RESERVED	Reserved	R	0x0
24	E6	QDMA Queue Number for event #6 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
23:21	RESERVED	Reserved	R	0x0
20	E5	QDMA Queue Number for event #5 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
19:17	RESERVED	Reserved	R	0x0
16	E4	QDMA Queue Number for event #4 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
15:13	RESERVED	Reserved	R	0x0
12	E3	QDMA Queue Number for event #3 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
11:9	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
8	E2	QDMA Queue Number for event #2 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
7:5	RESERVED	Reserved	R	0x0
4	E1	QDMA Queue Number for event #1 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0
3:1	RESERVED	Reserved	R	0x0
0	E0	QDMA Queue Number for event #0 0x0: Event En is queued on Q0 0x1: Event En is queued on Q1	RW	0

Table 5-119. Register Call Summary for Register TPCC_QDMAQNUM

DSP Subsystem Programming Guide • Mapping Between DMA/QDMA Events and Event Queues: [0]
DSP Subsystem Register Manual • TPCC Register Summary: [1]

Table 5-120. TPCC_QUETCMAP

Address Offset	0x0000 0280		
Physical Address	0x01C0 0280	**Instance**	TPCC
Description	Queue to TC Mapping		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED			TCNUMQ1	RESERVED			TCNUMQ0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
4	TCNUMQ1	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to. 0x0: TRs from this queue are routed to TC0 0x1: TRs from this queue are routed to TC1	RW	1
3:1	RESERVED	Write 0s for future compatibility. Reads return 0s.	RW	0x0
0	TCNUMQ0	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to. 0x0: TRs from this queue are routed to TC0 0x1: TRs from this queue are routed to TC1	RW	0

Table 5-121. Register Call Summary for Register TPCC_QUETCMAP

DSP Subsystem Programming Guide • Mapping a Queue to a Transfer Controller: [0]
DSP Subsystem Register Manual • TPCC Register Summary: [1]

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Table 5-122. TPCC_QUEPRI

Address Offset	0x0000 0284		
Physical Address	0x01C0 0284	**Instance**	TPCC
Description	Queue Priority		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED	PRIQ1			RESERVED	PRIQ0		

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	write 0's for future compatibility reads return 0's	RW	0
7	RESERVED	write 0's for future compatibility reads return 0's	RW	0
6:4	PRIQ1	Priority Level for Queue 1 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands. 0x0: Priority 0 - Highest priority 0x1: Priority 1 0x2: Priority 2 0x3: Priority 3 0x4: Priority 4 0x5: Priority 5 0x6: Priority 6 0x7: Priority 7 - Lowest Priority	RW	0x0
3	RESERVED	write 0's for future compatibility reads return 0's	RW	0
2:0	PRIQ0	Priority Level for Queue 0 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands. 0x0: Priority 0 - Highest priority 0x1: Priority 1 0x2: Priority 2 0x3: Priority 3 0x4: Priority 4 0x5: Priority 5 0x6: Priority 6 0x7: Priority 7 - Lowest Priority	RW	0x0

Table 5-123. Register Call Summary for Register TPCC_QUEPRI

DSP Subsystem Programming Guide
- Handling Priority: [0] [1]
- Aged Priority: [2] [3]

DSP Subsystem Register Manual
- TPCC Register Summary: [4]

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Table 5-124. TPCC_EMR

Address Offset	0x0000 0300		
Physical Address	0x01C0 0300	**Instance**	TPCC
Description	Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER), Set Events (ESR), and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear), then an error will be signaled with TPCC error interrupt.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event Missed #31	R	0
30	E30	Event Missed #30	R	0
29	E29	Event Missed #29	R	0
28	E28	Event Missed #28	R	0
27	E27	Event Missed #27	R	0
26	E26	Event Missed #26	R	0
25	E25	Event Missed #25	R	0
24	E24	Event Missed #24	R	0
23	E23	Event Missed #23	R	0
22	E22	Event Missed #22	R	0
21	E21	Event Missed #21	R	0
20	E20	Event Missed #20	R	0
19	E19	Event Missed #19	R	0
18	E18	Event Missed #18	R	0
17	E17	Event Missed #17	R	0
16	E16	Event Missed #16	R	0
15	E15	Event Missed #15	R	0
14	E14	Event Missed #14	R	0
13	E13	Event Missed #13	R	0
12	E12	Event Missed #12	R	0
11	E11	Event Missed #11	R	0
10	E10	Event Missed #10	R	0
9	E9	Event Missed #9	R	0
8	E8	Event Missed #8	R	0
7	E7	Event Missed #7	R	0
6	E6	Event Missed #6	R	0
5	E5	Event Missed #5	R	0
4	E4	Event Missed #4	R	0
3	E3	Event Missed #3	R	0
2	E2	Event Missed #2	R	0
1	E1	Event Missed #1	R	0
0	E0	Event Missed #0	R	0

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Table 5-125. Register Call Summary for Register TPCC_EMR

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- Error Reporting for DSP DMA: [0]

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- TPCC Register Summary: [1]
- TPCC Register Description: [2] [3] [4] [5] [6]

Table 5-126. TPCC_EMRH

Address Offset	0x0000 0304		
Physical Address	0x01C0 0304	**Instance**	TPCC
Description	Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER), Set Events (ESR), and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear), then an error will be signaled with TPCC error interrupt.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event Missed #63	R	0
30	E62	Event Missed #62	R	0
29	E61	Event Missed #61	R	0
28	E60	Event Missed #60	R	0
27	E59	Event Missed #59	R	0
26	E58	Event Missed #58	R	0
25	E57	Event Missed #57	R	0
24	E56	Event Missed #56	R	0
23	E55	Event Missed #55	R	0
22	E54	Event Missed #54	R	0
21	E53	Event Missed #53	R	0
20	E52	Event Missed #52	R	0
19	E51	Event Missed #51	R	0
18	E50	Event Missed #50	R	0
17	E49	Event Missed #49	R	0
16	E48	Event Missed #48	R	0
15	E47	Event Missed #47	R	0
14	E46	Event Missed #46	R	0
13	E45	Event Missed #45	R	0
12	E44	Event Missed #44	R	0
11	E43	Event Missed #43	R	0
10	E42	Event Missed #42	R	0
9	E41	Event Missed #41	R	0
8	E40	Event Missed #40	R	0
7	E39	Event Missed #39	R	0
6	E38	Event Missed #38	R	0
5	E37	Event Missed #37	R	0
4	E36	Event Missed #36	R	0

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Bits	Field Name	Description	Type	Reset
3	E35	Event Missed #35	R	0
2	E34	Event Missed #34	R	0
1	E33	Event Missed #33	R	0
0	E32	Event Missed #32	R	0

Table 5-127. Register Call Summary for Register TPCC_EMRH

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2]

Table 5-128. TPCC_EMCR

Address Offset	0x0000 0308
Physical Address	0x01C0 0308 **Instance** TPCC
Description	Event Missed Clear Register: CPU write of 1 to the TPCC_EMCR[n] En bit causes the TPCC_EMR[n] En bit to be cleared. CPU write of 0 has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event Missed Clear #31	W	0
30	E30	Event Missed Clear #30	W	0
29	E29	Event Missed Clear #29	W	0
28	E28	Event Missed Clear #28	W	0
27	E27	Event Missed Clear #27	W	0
26	E26	Event Missed Clear #26	W	0
25	E25	Event Missed Clear #25	W	0
24	E24	Event Missed Clear #24	W	0
23	E23	Event Missed Clear #23	W	0
22	E22	Event Missed Clear #22	W	0
21	E21	Event Missed Clear #21	W	0
20	E20	Event Missed Clear #20	W	0
19	E19	Event Missed Clear #19	W	0
18	E18	Event Missed Clear #18	W	0
17	E17	Event Missed Clear #17	W	0
16	E16	Event Missed Clear #16	W	0
15	E15	Event Missed Clear #15	W	0
14	E14	Event Missed Clear #14	W	0
13	E13	Event Missed Clear #13	W	0
12	E12	Event Missed Clear #12	W	0
11	E11	Event Missed Clear #11	W	0
10	E10	Event Missed Clear #10	W	0
9	E9	Event Missed Clear #9	W	0
8	E8	Event Missed Clear #8	W	0
7	E7	Event Missed Clear #7	W	0
6	E6	Event Missed Clear #6	W	0

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Bits	Field Name	Description	Type	Reset
5	E5	Event Missed Clear #5	W	0
4	E4	Event Missed Clear #4	W	0
3	E3	Event Missed Clear #3	W	0
2	E2	Event Missed Clear #2	W	0
1	E1	Event Missed Clear #1	W	0
0	E0	Event Missed Clear #0	W	0

Table 5-129. Register Call Summary for Register TPCC_EMCR

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2]

Table 5-130. TPCC_EMCRH

Address Offset	0x0000 030C		
Physical Address	0x01C0 030C	**Instance**	TPCC
Description	Event Missed Clear Register (High Part): CPU write of 1 to the TPCC_EMCR[n] En bit causes the TPCC_EMR[n] En bit to be cleared. CPU write of 0 has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event Missed Clear #63	W	0
30	E62	Event Missed Clear #62	W	0
29	E61	Event Missed Clear #61	W	0
28	E60	Event Missed Clear #60	W	0
27	E59	Event Missed Clear #59	W	0
26	E58	Event Missed Clear #58	W	0
25	E57	Event Missed Clear #57	W	0
24	E56	Event Missed Clear #56	W	0
23	E55	Event Missed Clear #55	W	0
22	E54	Event Missed Clear #54	W	0
21	E53	Event Missed Clear #53	W	0
20	E52	Event Missed Clear #52	W	0
19	E51	Event Missed Clear #51	W	0
18	E50	Event Missed Clear #50	W	0
17	E49	Event Missed Clear #49	W	0
16	E48	Event Missed Clear #48	W	0
15	E47	Event Missed Clear #47	W	0
14	E46	Event Missed Clear #46	W	0
13	E45	Event Missed Clear #45	W	0
12	E44	Event Missed Clear #44	W	0
11	E43	Event Missed Clear #43	W	0
10	E42	Event Missed Clear #42	W	0
9	E41	Event Missed Clear #41	W	0
8	E40	Event Missed Clear #40	W	0

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Bits	Field Name	Description	Type	Reset
7	E39	Event Missed Clear #39	W	0
6	E38	Event Missed Clear #38	W	0
5	E37	Event Missed Clear #37	W	0
4	E36	Event Missed Clear #36	W	0
3	E35	Event Missed Clear #35	W	0
2	E34	Event Missed Clear #34	W	0
1	E33	Event Missed Clear #33	W	0
0	E32	Event Missed Clear #32	W	0

Table 5-131. Register Call Summary for Register TPCC_EMCRH

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-132. TPCC_QEMR

Address Offset	0x0000 0310		
Physical Address	0x01C0 0310	**Instance**	TPCC
Description	QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced. If any bit in the TPCC_QEMR register is set (and all errors (including TPCC_EMR/TPCC_CCERR) were previously clear), then an error will be signaled with TPCC error interrupt.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	reads return 0's	R	0x000000
7	E7	Event Missed #7	R	0
6	E6	Event Missed #6	R	0
5	E5	Event Missed #5	R	0
4	E4	Event Missed #4	R	0
3	E3	Event Missed #3	R	0
2	E2	Event Missed #2	R	0
1	E1	Event Missed #1	R	0
0	E0	Event Missed #0	R	0

Table 5-133. Register Call Summary for Register TPCC_QEMR

DSP Subsystem Programming Guide
- Error Reporting for DSP DMA: [0]

DSP Subsystem Register Manual
- TPCC Register Summary: [1]
- TPCC Register Description: [2] [3] [4] [5]

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Table 5-134. TPCC_QEMCR

Address Offset	0x0000 0314		
Physical Address	0x01C0 0314	**Instance**	TPCC
Description	QDMA Event Missed Clear Register: CPU write of 1 to the TPCC_QEMCR[n] En bit causes the TPCC_QEMR[n] En bit to be cleared. CPU write of 0 has no effect. All error bits must be cleared before additional error interrupts will be asserted by CC.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	write 0's for future compatibility	W	0x000000
7	E7	Event Missed Clear #7	W	0
6	E6	Event Missed Clear #6	W	0
5	E5	Event Missed Clear #5	W	0
4	E4	Event Missed Clear #4	W	0
3	E3	Event Missed Clear #3	W	0
2	E2	Event Missed Clear #2	W	0
1	E1	Event Missed Clear #1	W	0
0	E0	Event Missed Clear #0	W	0

Table 5-135. Register Call Summary for Register TPCC_QEMCR

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- TPCC Register Summary: [0]
- TPCC Register Description: [1]

Table 5-136. TPCC_CCERR

Address Offset	0x0000 0318		
Physical Address	0x01C0 0318	**Instance**	TPCC
Description	CC Error Register Each bit can be cleared by writing a 1 to corresponding bit in TPCC_CCERRCLR register. If any bit in the TPCC_CCERR register is set (and all errors were previously clear), then an error will be signaled with TPCC error interrupt.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TCERR	RESERVED								QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	reads return 0's	R	0x0000
16	TCERR	Transfer Completion Code Error: 0 : Total number of allowed TCCs outstanding has not been reached. 1 : Total number of allowed TCCs has been reached.	R	0
15:8	RESERVED	reads return 0's	R	0x00

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Bits	Field Name	Description	Type	Reset
7	QTHRXCD7	Queue Threshold Error for Q7: 0 : Watermark/threshold has not been exceeded. 1 : Watermark/threshold has been exceeded.	R	0
6	QTHRXCD6	Queue Threshold Error for Q6: 0 : Watermark/threshold has not been exceeded. 1 : Watermark/threshold has been exceeded.	R	0
5	QTHRXCD5	Queue Threshold Error for Q5: 0 : Watermark/threshold has not been exceeded. 1 : Watermark/threshold has been exceeded.	R	0
4	QTHRXCD4	Queue Threshold Error for Q4: 0 : Watermark/threshold has not been exceeded. 1 : Watermark/threshold has been exceeded.	R	0
3	QTHRXCD3	Queue Threshold Error for Q3: 0 : Watermark/threshold has not been exceeded. 1 : Watermark/threshold has been exceeded.	R	0
2	QTHRXCD2	Queue Threshold Error for Q2: 0 : Watermark/threshold has not been exceeded. 1 : Watermark/threshold has been exceeded.	R	0
1	QTHRXCD1	Queue Threshold Error for Q1: 0 : Watermark/threshold has not been exceeded. 1 : Watermark/threshold has been exceeded.	R	0
0	QTHRXCD0	Queue Threshold Error for Q0: 0 : Watermark/threshold has not been exceeded. 1 : Watermark/threshold has been exceeded.	R	0

Table 5-137. Register Call Summary for Register TPCC_CCERR

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- Benchmarking: [0]
- Error Reporting for DSP DMA: [1] [2]

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- TPCC Register Summary: [3]
- TPCC Register Description: [4] [5] [6] [7]

Table 5-138. TPCC_CCERRCLR

Address Offset	0x0000 031C		
Physical Address	0x01C0 031C	**Instance**	TPCC
Description	CC Error Clear Register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TCERR	RESERVED								QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	write 0's for future compatibility	W	0x0000
16	TCERR	Clear Error for TCERR: Write of 1 clears the value of TPCC_CCERR bit N. Writes of 0 have no affect.	W	0
15:8	RESERVED	write 0's for future compatibility	W	0x00
7	QTHRXCD7	Clear error for QTHRXCD7: Write of 1 clears the values of QSTATN_7[20:16] WM, QSTATN_7[24] THRXCD, QTHRXCD7 Writes of 0 have no affect.	W	0

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Bits	Field Name	Description	Type	Reset
6	QTHRXCD6	Clear error for QTHRXCD6: Write of 1 clears the values of QSTATN_6[20:16] WM, QSTATN_6[24] THRXCD, QTHRXCD6 Writes of 0 have no affect.	W	0
5	QTHRXCD5	Clear error for QTHRXCD5: Write of 1 clears the values of QSTATN_5[20:16] WM, QSTATN_5[24] THRXCD, QTHRXCD5 Writes of 0 have no affect.	W	0
4	QTHRXCD4	Clear error for QTHRXCD4: Write of 1 clears the values of QSTATN_4[20:16] WM, QSTATN_4[24] THRXCD, QTHRXCD4 Writes of 0 have no affect.	W	0
3	QTHRXCD3	Clear error for QTHRXCD3: Write of 1 clears the values of QSTATN_3[20:16] WM, QSTATN_3[24] THRXCD, QTHRXCD3 Writes of 0 have no affect.	W	0
2	QTHRXCD2	Clear error for QTHRXCD2: Write of 1 clears the values of QSTATN_2[20:16] WM, QSTATN_2[24] THRXCD, QTHRXCD2 Writes of 0 have no affect.	W	0
1	QTHRXCD1	Clear error for QTHRXCD1: Write of 1 clears the values of QSTATN_1[20:16] WM, QSTATN_1[24] THRXCD, QTHRXCD1 Writes of 0 have no affect.	W	0
0	QTHRXCD0	Clear error for QTHRXCD0: Write of 1 clears the values of QSTATN_0[20:16] WM, QSTATN_0[24] THRXCD, QTHRXCD0 Writes of 0 have no affect.	W	0

Table 5-139. Register Call Summary for Register TPCC_CCERRCLR

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- TPCC Register Summary: [0]
- TPCC Register Description: [1]

Table 5-140. TPCC_EEVAL

Address Offset	0x0000 0320		
Physical Address	0x01C0 0320	**Instance**	TPCC
Description	Error Eval Register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SET	EVAL

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	write 0's for future compatibility	W	0x0000 0000
1	SET	Error Interrupt Set: CPU write of 1 to the SET bit causes the TPCC error interrupt to be pulsed regardless of state of TPCC_EMR/TPCC_EMRH, TPCC_QEMR, or CPU write of 0 has no effect.	W	0
0	EVAL	Error Interrupt Evaluate: CPU write of 1 to the EVAL bit causes the TPCC error interrupt to be pulsed if any errors have not been cleared in the TPCC_EMR/TPCC_EMRH, TPCC_QEMR, or TPCC_CCERR registers. CPU write of 0 has no effect.	W	0

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Table 5-141. Register Call Summary for Register TPCC_EEVAL

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- Error Reporting for DSP DMA: [0]

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- TPCC Register Summary: [1]

Table 5-142. TPCC_DRAEM_k

Address Offset	0x0000 0340 + (0x8 * k)
Physical Address	0x01C0 0340 + (0x8 * k) **Instance** TPCC
Description	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	DMA Region Access enable for Region M, bit #31	RW	0
30	E30	DMA Region Access enable for Region M, bit #30	RW	0
29	E29	DMA Region Access enable for Region M, bit #29	RW	0
28	E28	DMA Region Access enable for Region M, bit #28	RW	0
27	E27	DMA Region Access enable for Region M, bit #27	RW	0
26	E26	DMA Region Access enable for Region M, bit #26	RW	0
25	E25	DMA Region Access enable for Region M, bit #25	RW	0
24	E24	DMA Region Access enable for Region M, bit #24	RW	0
23	E23	DMA Region Access enable for Region M, bit #23	RW	0
22	E22	DMA Region Access enable for Region M, bit #22	RW	0
21	E21	DMA Region Access enable for Region M, bit #21	RW	0
20	E20	DMA Region Access enable for Region M, bit #20	RW	0
19	E19	DMA Region Access enable for Region M, bit #19	RW	0
18	E18	DMA Region Access enable for Region M, bit #18	RW	0
17	E17	DMA Region Access enable for Region M, bit #17	RW	0
16	E16	DMA Region Access enable for Region M, bit #16	RW	0
15	E15	DMA Region Access enable for Region M, bit #15	RW	0
14	E14	DMA Region Access enable for Region M, bit #14	RW	0
13	E13	DMA Region Access enable for Region M, bit #13	RW	0
12	E12	DMA Region Access enable for Region M, bit #12	RW	0
11	E11	DMA Region Access enable for Region M, bit #11	RW	0
10	E10	DMA Region Access enable for Region M, bit #10	RW	0
9	E9	DMA Region Access enable for Region M, bit #9	RW	0
8	E8	DMA Region Access enable for Region M, bit #8	RW	0
7	E7	DMA Region Access enable for Region M, bit #7	RW	0
6	E6	DMA Region Access enable for Region M, bit #6	RW	0
5	E5	DMA Region Access enable for Region M, bit #5	RW	0
4	E4	DMA Region Access enable for Region M, bit #4	RW	0
3	E3	DMA Region Access enable for Region M, bit #3	RW	0

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Bits	Field Name	Description	Type	Reset
2	E2	DMA Region Access enable for Region M, bit #2	RW	0
1	E1	DMA Region Access enable for Region M, bit #1	RW	0
0	E0	DMA Region Access enable for Region M, bit #0	RW	0

Table 5-143. Register Call Summary for Register TPCC_DRAEM_k

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-144. TPCC_DRAEHM_k

Address Offset	0x0000 0344 + (0x8 * k)		
Physical Address	0x01C0 0344 + (0x8 * k)	**Instance**	TPCC
Description	DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	DMA Region Access enable for Region M, bit #63	RW	0
30	E62	DMA Region Access enable for Region M, bit #62	RW	0
29	E61	DMA Region Access enable for Region M, bit #61	RW	0
28	E60	DMA Region Access enable for Region M, bit #60	RW	0
27	E59	DMA Region Access enable for Region M, bit #59	RW	0
26	E58	DMA Region Access enable for Region M, bit #58	RW	0
25	E57	DMA Region Access enable for Region M, bit #57	RW	0
24	E56	DMA Region Access enable for Region M, bit #56	RW	0
23	E55	DMA Region Access enable for Region M, bit #55	RW	0
22	E54	DMA Region Access enable for Region M, bit #54	RW	0
21	E53	DMA Region Access enable for Region M, bit #53	RW	0
20	E52	DMA Region Access enable for Region M, bit #52	RW	0
19	E51	DMA Region Access enable for Region M, bit #51	RW	0
18	E50	DMA Region Access enable for Region M, bit #50	RW	0
17	E49	DMA Region Access enable for Region M, bit #49	RW	0
16	E48	DMA Region Access enable for Region M, bit #48	RW	0
15	E47	DMA Region Access enable for Region M, bit #47	RW	0
14	E46	DMA Region Access enable for Region M, bit #46	RW	0
13	E45	DMA Region Access enable for Region M, bit #45	RW	0
12	E44	DMA Region Access enable for Region M, bit #44	RW	0
11	E43	DMA Region Access enable for Region M, bit #43	RW	0
10	E42	DMA Region Access enable for Region M, bit #42	RW	0

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Bits	Field Name	Description	Type	Reset
9	E41	DMA Region Access enable for Region M, bit #41	RW	0
8	E40	DMA Region Access enable for Region M, bit #40	RW	0
7	E39	DMA Region Access enable for Region M, bit #39	RW	0
6	E38	DMA Region Access enable for Region M, bit #38	RW	0
5	E37	DMA Region Access enable for Region M, bit #37	RW	0
4	E36	DMA Region Access enable for Region M, bit #36	RW	0
3	E35	DMA Region Access enable for Region M, bit #35	RW	0
2	E34	DMA Region Access enable for Region M, bit #34	RW	0
1	E33	DMA Region Access enable for Region M, bit #33	RW	0
0	E32	DMA Region Access enable for Region M, bit #32	RW	0

Table 5-145. Register Call Summary for Register TPCC_DRAEHM_k

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- TPCC Register Summary: [0]

Table 5-146. TPCC_QRAEM_k

Address Offset	0x0000 0380 + (0x4 * k)		
Physical Address	0x01C0 0380 + (0x4 * k)	**Instance**	TPCC
Description	QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	write 0's for future compatibility reads return 0's	RW	0x000000
7	E7	QDMA Region Access enable for Region M, bit #7	RW	0
6	E6	QDMA Region Access enable for Region M, bit #6	RW	0
5	E5	QDMA Region Access enable for Region M, bit #5	RW	0
4	E4	QDMA Region Access enable for Region M, bit #4	RW	0
3	E3	QDMA Region Access enable for Region M, bit #3	RW	0
2	E2	QDMA Region Access enable for Region M, bit #2	RW	0
1	E1	QDMA Region Access enable for Region M, bit #1	RW	0
0	E0	QDMA Region Access enable for Region M, bit #0	RW	0

Table 5-147. Register Call Summary for Register TPCC_QRAEM_k

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

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Table 5-148. TPCC_Q0E_o

Address Offset	0x0000 0400 + (0x4 * o)		
Physical Address	0x01C0 0400 + (0x4 * o)	**Instance**	TPCC
Description	Event Queue Entry Diagram for Queue 0 - Entry o		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ETYPE		ENUM					

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	reads return 0's	R	0x------
7:6	ETYPE	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Read 0x0: Event Triggered via ER Read 0x1: Manual Triggered via ESR Read 0x2: Chain Triggered via CER Read 0x3: Auto-Triggered via QER	R	0bxx
5:0	ENUM	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER), ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER), ENUM will range between 0 and NUM_QDMACH (up to 7).	R	0bxxxxxx

Table 5-149. Register Call Summary for Register TPCC_Q0E_o

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- TPCC Register Summary: [0]

Table 5-150. TPCC_Q1E_o

Address Offset	0x0000 0440 + (0x4 * o)		
Physical Address	0x01C0 0440 + (0x4 * o)	**Instance**	TPCC
Description	Event Queue Entry Diagram for Queue 1 - Entry o		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ETYPE		ENUM					

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	reads return 0's	R	0x------
7:6	ETYPE	Event Type: Specifies the specific Event Type for the given entry in the Event Queue. Read 0x0: Event Triggered via ER Read 0x1: Manual Triggered via ESR Read 0x2: Chain Triggered via CER Read 0x3: Auto-Triggered via QER	R	0bxx

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Bits	Field Name	Description	Type	Reset
5:0	ENUM	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER), ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER), ENUM will range between 0 and NUM_QDMACH (up to 7).	R	0bxxxxxx

Table 5-151. Register Call Summary for Register TPCC_Q1E_o

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-152. TPCC_QSTATN_l

Address Offset	0x0000 0600 + (0x4 * l)		
Physical Address	0x01C0 0600 + (0x4 * l)	**Instance**	TPCC
Description	QSTATn Register Set		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRXCD	RESERVED							WM								RESERVED								NUMVAL								RESERVED				STRTPTR			

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	reads return 0's	R	0x00
24	THRXCD	Threshold Exceeded: 0 : Threshold specified by QWMTHR(A|B).Qn has not been exceeded. 1 : Threshold specified by QWMTHR(A|B).Qn has been exceeded. THRXCD is cleared via WMCLRn bit.	R	0
23:21	RESERVED	reads return 0's	R	0x0
20:16	WM	Watermark for Maximum Queue Usage: Watermark tracks the most entries that have been in QueueN since reset or since the last time that the watermark (WM) was cleared. WM is cleared via WMCLRn bit. Legal values = 0x0 (empty) to 0x10 (full)	R	0x00
15:13	RESERVED	reads return 0's	R	0x0
12:8	NUMVAL	Number of Valid Entries in QueueN: Represents the total number of entries residing in the Queue Manager FIFO at a given instant. Always enabled. Legal values = 0x0 (empty) to 0x10 (full)	R	0x00
7:4	RESERVED	reads return 0's	R	0x0
3:0	STRTPTR	Start Pointer: Represents the offset to the head entry of QueueN, in units of *entries*. Always enabled. Legal values = 0x0 (0th entry) to 0xF (15th entry)	R	0x0

Table 5-153. Register Call Summary for Register TPCC_QSTATN_l

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- TPCC Register Summary: [0]

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Table 5-154. TPCC_QWMTHRA

Address Offset	0x0000 0620		
Physical Address	0x01C0 0620	**Instance**	TPCC
Description	Queue Threshold A for Q[3:0]: QTHRXCDn and THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			Q3					RESERVED			Q2					RESERVED			Q1					RESERVED			Q0				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
28:24	Q3	Queue Threshold for Q3 value	RW	0x10
23:21	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
20:16	Q2	Queue Threshold for Q2 value	RW	0x10
15:13	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
12:8	Q1	Queue Threshold for Q1 value	RW	0x10
7:5	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
4:0	Q0	Queue Threshold for Q0 value	RW	0x10

Table 5-155. Register Call Summary for Register TPCC_QWMTHRA

DSP Subsystem Programming Guide
- Benchmarking: [0]

DSP Subsystem Register Manual
- TPCC Register Summary: [1]

Table 5-156. TPCC_QWMTHRB

Address Offset	0x0000 0624		
Physical Address	0x01C0 0624	**Instance**	TPCC
Description	Queue Threshold B for Q[7:4]: QTHRXCDn and THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via NUMVAL) equals or exceeds the value specified by QWMTHRB.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			Q7					RESERVED			Q6					RESERVED			Q5					RESERVED			Q4				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
28:24	Q7	Queue Threshold for Q7 value	RW	0x10
23:21	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
20:16	Q6	Queue Threshold for Q6 value	RW	0x10

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Bits	Field Name	Description	Type	Reset
15:13	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
12:8	Q5	Queue Threshold for Q5 value	RW	0x10
7:5	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
4:0	Q4	Queue Threshold for Q4 value	RW	0x10

Table 5-157. Register Call Summary for Register TPCC_QWMTHRB

DSP Subsystem Programming Guide • Benchmarking: [0]
DSP Subsystem Register Manual • TPCC Register Summary: [1]

Table 5-158. TPCC_CCSTAT

Address Offset	0x0000 0640		
Physical Address	0x01C0 0640	**Instance**	TPCC
Description	CC Status Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QUEACTV7	QUEACTV6	QUEACTV5	QUEACTV4	QUEACTV3	QUEACTV2	QUEACTV1	QUEACTV0	RESERVED		COMPACTV						RESERVED			ACTV	RESERVED	TRACTV	QEVTACTV	EVTACTV

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	reads return 0's	R	0x00
23	QUEACTV7	Queue 7 Active 0 : No Evts are queued in Q7. 1 : At least one TR is queued in Q7.	R	0
22	QUEACTV6	Queue 6 Active 0 : No Evts are queued in Q6. 1 : At least one TR is queued in Q6.	R	0
21	QUEACTV5	Queue 5 Active 0 : No Evts are queued in Q5. 1 : At least one TR is queued in Q5.	R	0
20	QUEACTV4	Queue 4 Active 0 : No Evts are queued in Q4. 1 : At least one TR is queued in Q4.	R	0
19	QUEACTV3	Queue 3 Active 0 : No Evts are queued in Q3. 1 : At least one TR is queued in Q3.	R	0
18	QUEACTV2	Queue 2 Active 0 : No Evts are queued in Q2. 1 : At least one TR is queued in Q2.	R	0
17	QUEACTV1	Queue 1 Active 0 : No Evts are queued in Q1. 1 : At least one TR is queued in Q1.	R	0
16	QUEACTV0	Queue 0 Active 0 : No Evts are queued in Q0. 1 : At least one TR is queued in Q0.	R	0
15:14	RESERVED	reads return 0's	R	0x0

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Bits	Field Name	Description	Type	Reset
13:8	COMPACTV	Completion Request Active: Counter that tracks the total number of completion requests submitted to the TC. The counter increments when a TR is submitted with TCINTEN or TCCHEN set to 1. The counter decrements for every valid completion code received from any of the external TCs. The CC will not service new TRs if COMPACTV count is already at the limit. 0 : No completion requests outstanding. 1: Total of 1 completion request outstanding. ... 63 : Total of 63 completion requests are outstanding. No additional TRs will be submitted until count is less than 63.	R	0x00
7:5	RESERVED	reads return 0's	R	0x0
4	ACTV	Channel Controller Active: Channel Controller Active is a logical-OR of each of the *ACTV signals. The ACTV bit must remain high through the life of a TR. 0 : Channel is idle. 1 : Channel is busy.	R	0
3	RESERVED	reads return 0's	R	0
2	TRACTV	Transfer Request Active: 0 : Transfer Request processing/submission logic is inactive. 1 : Transfer Request processing/submission logic is active.	R	0
1	QEVTACTV	QDMA Event Active: 0 : No enabled QDMA Events are active within the CC. 1 : At least one enabled DMA Event (ER & EER, ESR, CER) is active within the CC.	R	0
0	EVTACTV	DMA Event Active: 0 : No enabled DMA Events are active within the CC. 1 : At least one enabled DMA Event (ER & EER, ESR, CER) is active within the CC.	R	0

Table 5-159. Register Call Summary for Register TPCC_CCSTAT

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-160. TPCC_AETCTL

Address Offset	0x0000 0700		
Physical Address	0x01C0 0700	**Instance**	TPCC
Description	Advanced Event Trigger Control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	RESERVED															ENDINT								RESERVED	TYPE	STRTEVT					

Bits	Field Name	Description	Type	Reset
31	EN	AET Enable: 0 : AET event generation is disabled. 1 : AET event generation is enabled.	RW	0
30:14	RESERVED	write 0's for future compatibility reads return 0's	RW	0x00000

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Bits	Field Name	Description	Type	Reset
13:8	ENDINT	AET End Interrupt: Dictates the completion interrupt number that will force the tpcc_aet signal to be deasserted (low)	RW	0x00
7	RESERVED	write 0's for future compatibility reads return 0's	RW	0
6	TYPE	AET Event Type: 0 : Event specified by STARTEVT applies to DMA Events (set by ER, ESR, or CER) 1 : Event specified by STARTEVT applies to QDMA Events	RW	0
5:0	STRTEVT	AET Start Event: Dictates the Event Number that will force the tpcc_aet signal to be asserted (high)	RW	0x00

Table 5-161. Register Call Summary for Register TPCC_AETCTL

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-162. TPCC_AETSTAT

Address Offset	0x0000 0704		
Physical Address	0x01C0 0704	**Instance**	TPCC
Description	Advanced Event Trigger Stat		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STAT

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	reads return 0's	R	0x0000 0000
0	STAT	AET Status: 0 : tpcc_aet is currently low. 1 : tpcc_aet is currently high.	R	0

Table 5-163. Register Call Summary for Register TPCC_AETSTAT

DSP Subsystem Register Manual
- TPCC Register Summary: [0]
- TPCC Register Description: [1]

Table 5-164. TPCC_AETCMD

Address Offset	0x0000 0708		
Physical Address	0x01C0 0708	**Instance**	TPCC
Description	AET Command		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLR

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	write 0's for future compatibility	W	0x0000 0000
0	CLR	AET Clear command: CPU write of 1 to the CLR bit causes the tpcc_aet output signal and TPCC_AETSTAT register to be cleared. CPU write of 0 has no effect..	W	0

Table 5-165. Register Call Summary for Register TPCC_AETCMD

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-166. TPCC_ER

Address Offset	0x0000 1000		
Physical Address	0x01C0 1000	**Instance**	TPCC
Description	Event Register: If TPCC_ER[n] En bit is set and the TPCC_EER[n] En bit is also set, then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. TPCC_ER[n] En bit is set when the input event #n transitions from inactive (low) to active (high), regardless of the state of TPCC_EER[n] En bit. TPCC_ER[n] En bit is cleared when the corresponding event is prioritized and serviced. If the TPCC_ER[n] En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the TPCC_EER register is set, then the corresponding bit in the Event Missed Register is set. Event N can be cleared via software by writing a 1 to the TPCC_ECR pseudo-register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	R	0
30	E30	Event #30	R	0
29	E29	Event #29	R	0
28	E28	Event #28	R	0
27	E27	Event #27	R	0
26	E26	Event #26	R	0
25	E25	Event #25	R	0
24	E24	Event #24	R	0
23	E23	Event #23	R	0
22	E22	Event #22	R	0
21	E21	Event #21	R	0
20	E20	Event #20	R	0
19	E19	Event #19	R	0
18	E18	Event #18	R	0
17	E17	Event #17	R	0
16	E16	Event #16	R	0
15	E15	Event #15	R	0
14	E14	Event #14	R	0
13	E13	Event #13	R	0
12	E12	Event #12	R	0
11	E11	Event #11	R	0
10	E10	Event #10	R	0

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Bits	Field Name	Description	Type	Reset
9	E9	Event #9	R	0
8	E8	Event #8	R	0
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-167. Register Call Summary for Register TPCC_ER

DSP Subsystem Functional Description

- DMA Versus QDMA: [0] [1]

DSP Subsystem Register Manual

- TPCC Register Summary: [2]
- TPCC Register Description: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35]

Table 5-168. TPCC_ERH

Address Offset	0x0000 1004		
Physical Address	0x01C0 1004	**Instance**	TPCC
Description	Event Register (High Part): If TPCC_ERH[n] En bit is set and the TPCC_EERH[n] En bit is also set, then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TPCC_ERH[n] En bit is set when the input event #n transitions from inactive (low) to active (high), regardless of the state of TPCC_EERH[n] En bit. TPCC_ER[n] En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactiveTC. to active transition is detected on the input event #n input AND the corresponding bit in the TPCC_EERH register is set, then the corresponding bit in the Event Missed Register is set. Event N can be cleared via software by writing a 1 to the TPCC_ECRH pseudo-register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	R	0
30	E62	Event #62	R	0
29	E61	Event #61	R	0
28	E60	Event #60	R	0
27	E59	Event #59	R	0
26	E58	Event #58	R	0
25	E57	Event #57	R	0
24	E56	Event #56	R	0
23	E55	Event #55	R	0
22	E54	Event #54	R	0
21	E53	Event #53	R	0
20	E52	Event #52	R	0
19	E51	Event #51	R	0
18	E50	Event #50	R	0

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Bits	Field Name	Description	Type	Reset
17	E49	Event #49	R	0
16	E48	Event #48	R	0
15	E47	Event #47	R	0
14	E46	Event #46	R	0
13	E45	Event #45	R	0
12	E44	Event #44	R	0
11	E43	Event #43	R	0
10	E42	Event #42	R	0
9	E41	Event #41	R	0
8	E40	Event #40	R	0
7	E39	Event #39	R	0
6	E38	Event #38	R	0
5	E37	Event #37	R	0
4	E36	Event #36	R	0
3	E35	Event #35	R	0
2	E34	Event #34	R	0
1	E33	Event #33	R	0
0	E32	Event #32	R	0

Table 5-169. Register Call Summary for Register TPCC_ERH

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]

Table 5-170. TPCC_ECR

Address Offset	0x0000 1008		
Physical Address	0x01C0 1008	**Instance**	TPCC
Description	Event Clear Register: CPU write of 1 to the TPCC_ECR[n] En bit causes the ER.En bit to be cleared. CPU write of 0 has no effect.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0
24	E24	Event #24	W	0
23	E23	Event #23	W	0
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0

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Bits	Field Name	Description	Type	Reset
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-171. Register Call Summary for Register TPCC_ECR

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-172. TPCC_ECRH

Address Offset	0x0000 100C		
Physical Address	0x01C0 100C	**Instance**	TPCC
Description	Event Clear Register (High Part): CPU write of 1 to the TPCC_ECRH[n] En bit causes the ERH.En bit to be cleared. CPU write of 0 has no effect.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0
25	E57	Event #57	W	0
24	E56	Event #56	W	0
23	E55	Event #55	W	0
22	E54	Event #54	W	0

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Bits	Field Name	Description	Type	Reset
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

Table 5-173. Register Call Summary for Register TPCC_ECRH

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-174. TPCC_ESR

Address Offset	0x0000 1010		
Physical Address	0x01C0 1010	**Instance**	TPCC
Description	Event Set Register: CPU write of 1 to the TPCC_ESR[n] En bit causes the TPCC_ER[n] En bit to be set. CPU write of 0 has no effect.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0
24	E24	Event #24	W	0

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Bits	Field Name	Description	Type	Reset
23	E23	Event #23	W	0
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-175. Register Call Summary for Register TPCC_ESR

DSP Subsystem Functional Description • DMA Versus QDMA: [0] [1] [2]
DSP Subsystem Programming Guide • Manual Trigger (Software-Synchronized Transfers): [3]
DSP Subsystem Register Manual • TPCC Register Summary: [4] • TPCC Register Description: [5] [6] [7] [8]

Table 5-176. TPCC_ESRH

Address Offset	0x0000 1014		
Physical Address	0x01C0 1014	**Instance**	TPCC
Description	Event Set Register (High Part) CPU write of 1 to the TPCC_ESRH[n] En bit causes the TPCC_ERH[n] En bit to be set. CPU write of 0 has no effect.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0

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Bits	Field Name	Description	Type	Reset
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0
25	E57	Event #57	W	0
24	E56	Event #56	W	0
23	E55	Event #55	W	0
22	E54	Event #54	W	0
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

Table 5-177. Register Call Summary for Register TPCC_ESRH

DSP Subsystem Functional Description • DMA Versus QDMA: [0] [1]
DSP Subsystem Programming Guide • Manual Trigger (Software-Synchronized Transfers): [2]
DSP Subsystem Register Manual • TPCC Register Summary: [3] • TPCC Register Description: [4] [5] [6] [7]

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Table 5-178. TPCC_CER

Address Offset	0x0000 1018		
Physical Address	0x01C0 1018	**Instance**	TPCC
Description	Chained Event Register: If TPCC_CER[n] En bit is set (regardless of state of TPCC_EER[5] En), then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TPCC_CER[n] En bit is set when a chaining completion code is returned from one of the TPTCs via the completion interface, or is generated internally via Early Completion path. TPCC_CER[n] En bit is cleared when the corresponding event is prioritized and serviced. If the TPCC_CER[n] En bit is already set and the corresponding chaining completion code is returned from the TPCC_TC, then the corresponding bit in the Event Missed Register is set. TPCC_CER[n] En cannot be set or cleared via software.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	R	0
30	E30	Event #30	R	0
29	E29	Event #29	R	0
28	E28	Event #28	R	0
27	E27	Event #27	R	0
26	E26	Event #26	R	0
25	E25	Event #25	R	0
24	E24	Event #24	R	0
23	E23	Event #23	R	0
22	E22	Event #22	R	0
21	E21	Event #21	R	0
20	E20	Event #20	R	0
19	E19	Event #19	R	0
18	E18	Event #18	R	0
17	E17	Event #17	R	0
16	E16	Event #16	R	0
15	E15	Event #15	R	0
14	E14	Event #14	R	0
13	E13	Event #13	R	0
12	E12	Event #12	R	0
11	E11	Event #11	R	0
10	E10	Event #10	R	0
9	E9	Event #9	R	0
8	E8	Event #8	R	0
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

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Table 5-179. Register Call Summary for Register TPCC_CER

DSP Subsystem Functional Description

- DMA Versus QDMA: [0] [1]

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- TPCC Register Summary: [2]
- TPCC Register Description: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

Table 5-180. TPCC_CERH

Address Offset	0x0000 101C		
Physical Address	0x01C0 101C	**Instance**	TPCC
Description	Chained Event Register (High Part): If TPCC_CERH[n] En bit is set (regardless of state of TPCC_EERH[n] En), then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TPCC_CERH[n] En bit is set when a chaining completion code is returned from one of the TPTCs via the completion interface, or is generated internally via Early Completion path. TPCC_CERH[n] En bit is cleared when the corresponding event is prioritized and serviced. If the TPCC_CERH[n] En bit is already set and the corresponding chaining completion code is returned from the TC, then the corresponding bit in the Event Missed Register is set. TPCC_CERH[n] En cannot be set or cleared via software.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	R	0
30	E62	Event #62	R	0
29	E61	Event #61	R	0
28	E60	Event #60	R	0
27	E59	Event #59	R	0
26	E58	Event #58	R	0
25	E57	Event #57	R	0
24	E56	Event #56	R	0
23	E55	Event #55	R	0
22	E54	Event #54	R	0
21	E53	Event #53	R	0
20	E52	Event #52	R	0
19	E51	Event #51	R	0
18	E50	Event #50	R	0
17	E49	Event #49	R	0
16	E48	Event #48	R	0
15	E47	Event #47	R	0
14	E46	Event #46	R	0
13	E45	Event #45	R	0
12	E44	Event #44	R	0
11	E43	Event #43	R	0
10	E42	Event #42	R	0
9	E41	Event #41	R	0
8	E40	Event #40	R	0
7	E39	Event #39	R	0
6	E38	Event #38	R	0

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Bits	Field Name	Description	Type	Reset
5	E37	Event #37	R	0
4	E36	Event #36	R	0
3	E35	Event #35	R	0
2	E34	Event #34	R	0
1	E33	Event #33	R	0
0	E32	Event #32	R	0

Table 5-181. Register Call Summary for Register TPCC_CERH

DSP Subsystem Functional Description
- DMA Versus QDMA: [0]

DSP Subsystem Register Manual
- TPCC Register Summary: [1]
- TPCC Register Description: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]

Table 5-182. TPCC_EER

Address Offset	0x0000 1020		
Physical Address	0x01C0 1020	**Instance**	TPCC
Description	Event Enable Register: Enables DMA transfers for TPCC_ER[n] En pending events. TPCC_ER[n] En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (TPCC_CER) or Event Set Register (TPCC_ESR). Note that if a bit is set in TPCC_ER[n] En while TPCC_EER[n] En is disabled, no action is taken. If TPCC_EER[n] En is enabled at a later point (and TPCC_ER[n] En has not been cleared via software) then the event will be recognized as a valid 'TR Sync' TPCC_EER[n] En is not directly writeable. Events can be enabled via writes to TPCC_EESR and can be disabled via writes to TPCC_EECR register. TPCC_EER[n] En = 0: TPCC_ER[n] En is not enabled to trigger DMA transfers. TPCC_EER[n] En = 1: TPCC_ER[n] En is enabled to trigger DMA transfers.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	R	0
30	E30	Event #30	R	0
29	E29	Event #29	R	0
28	E28	Event #28	R	0
27	E27	Event #27	R	0
26	E26	Event #26	R	0
25	E25	Event #25	R	0
24	E24	Event #24	R	0
23	E23	Event #23	R	0
22	E22	Event #22	R	0
21	E21	Event #21	R	0
20	E20	Event #20	R	0
19	E19	Event #19	R	0
18	E18	Event #18	R	0
17	E17	Event #17	R	0
16	E16	Event #16	R	0
15	E15	Event #15	R	0

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Bits	Field Name	Description	Type	Reset
14	E14	Event #14	R	0
13	E13	Event #13	R	0
12	E12	Event #12	R	0
11	E11	Event #11	R	0
10	E10	Event #10	R	0
9	E9	Event #9	R	0
8	E8	Event #8	R	0
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-183. Register Call Summary for Register TPCC_EER

DSP Subsystem Functional Description • DMA Versus QDMA: [0] [1]
DSP Subsystem Programming Guide • Manual Trigger (Software-Synchronized Transfers): [2]
DSP Subsystem Register Manual • TPCC Register Summary: [3] • TPCC Register Description: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]

Table 5-184. TPCC_EERH

Address Offset	0x0000 1024		
Physical Address	0x01C0 1024	**Instance**	TPCC
Description	Event Enable Register (High Part): Enables DMA transfers for TPCC_ERH[n] En pending events. TPCC_ERH[n] En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (TPCC_CERH) or Event Set Register (TPCC_ESRH). Note that if a bit is set in TPCC_ERH[n] En while TPCC_EERH[n] En is disabled, no action is taken. If TPCC_EERH[n] En is enabled at a later point (and TPCC_ERH[n] En has not been cleared via software) then the event will be recognized as a valid 'TR Sync' TPCC_EERH[n] En is not directly writeable. Events can be enabled via writes to TPCC_EESRH and can be disabled via writes to TPCC_EECRH register. EERH[n] En = 0: TPCC_ER[n] En is not enabled to trigger DMA transfers. TPCC_EERH[n] En = 1: TPCC_ER[n] En is enabled to trigger DMA transfers.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	R	0
30	E62	Event #62	R	0
29	E61	Event #61	R	0
28	E60	Event #60	R	0
27	E59	Event #59	R	0

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Bits	Field Name	Description	Type	Reset
26	E58	Event #58	R	0
25	E57	Event #57	R	0
24	E56	Event #56	R	0
23	E55	Event #55	R	0
22	E54	Event #54	R	0
21	E53	Event #53	R	0
20	E52	Event #52	R	0
19	E51	Event #51	R	0
18	E50	Event #50	R	0
17	E49	Event #49	R	0
16	E48	Event #48	R	0
15	E47	Event #47	R	0
14	E46	Event #46	R	0
13	E45	Event #45	R	0
12	E44	Event #44	R	0
11	E43	Event #43	R	0
10	E42	Event #42	R	0
9	E41	Event #41	R	0
8	E40	Event #40	R	0
7	E39	Event #39	R	0
6	E38	Event #38	R	0
5	E37	Event #37	R	0
4	E36	Event #36	R	0
3	E35	Event #35	R	0
2	E34	Event #34	R	0
1	E33	Event #33	R	0
0	E32	Event #32	R	0

Table 5-185. Register Call Summary for Register TPCC_EERH

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]

Table 5-186. TPCC_EECR

Address Offset 0x0000 1028

Physical Address 0x01C0 1028 **Instance** TPCC

Description Event Enable Clear Register:
CPU write of 1 to the TPCC_EECR[n] En bit causes the TPCC_EER[n] En bit to be cleared.
CPU write of 0 has no effect..

Type W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0

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Bits	Field Name	Description	Type	Reset
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0
24	E24	Event #24	W	0
23	E23	Event #23	W	0
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-187. Register Call Summary for Register TPCC_EECR

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-188. TPCC_EECRH

Address Offset	0x0000 102C		
Physical Address	0x01C0 102C	**Instance**	TPCC
Description	Event Enable Clear Register (High Part): CPU write of 1 to the TPCC_EECRH[n] En bit causes the TPCC_EERH[n] En bit to be cleared. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

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Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0
25	E57	Event #57	W	0
24	E56	Event #56	W	0
23	E55	Event #55	W	0
22	E54	Event #54	W	0
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

Table 5-189. Register Call Summary for Register TPCC_EECRH

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-190. TPCC_EESR

Address Offset	0x0000 1030		
Physical Address	0x01C0 1030	**Instance**	TPCC
Description	Event Enable Set Register: CPU write of 1 to the TPCC_EESR[n] En bit causes the TPCC_EER[n] En bit to be set. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

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Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0
24	E24	Event #24	W	0
23	E23	Event #23	W	0
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-191. Register Call Summary for Register TPCC_EESR

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-192. TPCC_EESRH

Address Offset	0x0000 1034
Physical Address	0x01C0 1034 **Instance** TPCC
Description	Event Enable Set Register (High Part): CPU write of 1 to the TPCC_EESRH[n] En bit causes the TPCC_EERH[n] En bit to be set. CPU write of 0 has no effect..
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

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Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0
25	E57	Event #57	W	0
24	E56	Event #56	W	0
23	E55	Event #55	W	0
22	E54	Event #54	W	0
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

Table 5-193. Register Call Summary for Register TPCC_EESRH

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-194. TPCC_SER

Address Offset	0x0000 1038		
Physical Address	0x01C0 1038	**Instance**	TPCC
Description	Secondary Event Register: The secondary event register is used along with the Event Register (TPCC_ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	R	0
30	E30	Event #30	R	0
29	E29	Event #29	R	0
28	E28	Event #28	R	0
27	E27	Event #27	R	0
26	E26	Event #26	R	0
25	E25	Event #25	R	0
24	E24	Event #24	R	0
23	E23	Event #23	R	0
22	E22	Event #22	R	0
21	E21	Event #21	R	0
20	E20	Event #20	R	0
19	E19	Event #19	R	0
18	E18	Event #18	R	0
17	E17	Event #17	R	0
16	E16	Event #16	R	0
15	E15	Event #15	R	0
14	E14	Event #14	R	0
13	E13	Event #13	R	0
12	E12	Event #12	R	0
11	E11	Event #11	R	0
10	E10	Event #10	R	0
9	E9	Event #9	R	0
8	E8	Event #8	R	0
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-195. Register Call Summary for Register TPCC_SER

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4] [5]

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Table 5-196. TPCC_SERH

Address Offset	0x0000 103C		
Physical Address	0x01C0 103C	**Instance**	TPCC
Description	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (TPCC_ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	R	0
30	E62	Event #62	R	0
29	E61	Event #61	R	0
28	E60	Event #60	R	0
27	E59	Event #59	R	0
26	E58	Event #58	R	0
25	E57	Event #57	R	0
24	E56	Event #56	R	0
23	E55	Event #55	R	0
22	E54	Event #54	R	0
21	E53	Event #53	R	0
20	E52	Event #52	R	0
19	E51	Event #51	R	0
18	E50	Event #50	R	0
17	E49	Event #49	R	0
16	E48	Event #48	R	0
15	E47	Event #47	R	0
14	E46	Event #46	R	0
13	E45	Event #45	R	0
12	E44	Event #44	R	0
11	E43	Event #43	R	0
10	E42	Event #42	R	0
9	E41	Event #41	R	0
8	E40	Event #40	R	0
7	E39	Event #39	R	0
6	E38	Event #38	R	0
5	E37	Event #37	R	0
4	E36	Event #36	R	0
3	E35	Event #35	R	0
2	E34	Event #34	R	0
1	E33	Event #33	R	0
0	E32	Event #32	R	0

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Table 5-197. Register Call Summary for Register TPCC_SERH

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-198. TPCC_SECR

Address Offset	0x0000 1040		
Physical Address	0x01C0 1040	**Instance**	TPCC
Description	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of 1 to the TPCC_SECR[n] En bit clears the TPCC_SER register. CPU write of 0 has no effect.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0
24	E24	Event #24	W	0
23	E23	Event #23	W	0
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

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Table 5-199. Register Call Summary for Register TPCC_SECR

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2]

Table 5-200. TPCC_SECRH

Address Offset	0x0000 1044		
Physical Address	0x01C0 1044	**Instance**	TPCC
Description	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the TPCC_SERH registers. CPU write of 1 to the TPCC_SECRH[n] En bit clears the TPCC_SERH register. CPU write of 0 has no effect.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0
25	E57	Event #57	W	0
24	E56	Event #56	W	0
23	E55	Event #55	W	0
22	E54	Event #54	W	0
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

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Table 5-201. Register Call Summary for Register TPCC_SECRH

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2]

Table 5-202. TPCC_IER

Address Offset	0x0000 1050		
Physical Address	0x01C0 1050	**Instance**	TPCC
Description	Int Enable Register: TPCC_IER[n] In is not directly writeable. Interrupts can be enabled via writes to TPCC_IESR and can be disabled via writes to TPCC_IECR register. TPCC_IER[n] In = 0: TPCC_IPR[n] In is NOT enabled for interrupts. TPCC_IER[n] In = 1: TPCC_IPR[n] In IS enabled for interrupts.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	R	0
30	I30	Interrupt associated with TCC #30	R	0
29	I29	Interrupt associated with TCC #29	R	0
28	I28	Interrupt associated with TCC #28	R	0
27	I27	Interrupt associated with TCC #27	R	0
26	I26	Interrupt associated with TCC #26	R	0
25	I25	Interrupt associated with TCC #25	R	0
24	I24	Interrupt associated with TCC #24	R	0
23	I23	Interrupt associated with TCC #23	R	0
22	I22	Interrupt associated with TCC #22	R	0
21	I21	Interrupt associated with TCC #21	R	0
20	I20	Interrupt associated with TCC #20	R	0
19	I19	Interrupt associated with TCC #19	R	0
18	I18	Interrupt associated with TCC #18	R	0
17	I17	Interrupt associated with TCC #17	R	0
16	I16	Interrupt associated with TCC #16	R	0
15	I15	Interrupt associated with TCC #15	R	0
14	I14	Interrupt associated with TCC #14	R	0
13	I13	Interrupt associated with TCC #13	R	0
12	I12	Interrupt associated with TCC #12	R	0
11	I11	Interrupt associated with TCC #11	R	0
10	I10	Interrupt associated with TCC #10	R	0
9	I9	Interrupt associated with TCC #9	R	0
8	I8	Interrupt associated with TCC #8	R	0
7	I7	Interrupt associated with TCC #7	R	0
6	I6	Interrupt associated with TCC #6	R	0
5	I5	Interrupt associated with TCC #5	R	0
4	I4	Interrupt associated with TCC #4	R	0
3	I3	Interrupt associated with TCC #3	R	0
2	I2	Interrupt associated with TCC #2	R	0
1	I1	Interrupt associated with TCC #1	R	0

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Bits	Field Name	Description	Type	Reset
0	I0	Interrupt associated with TCC #0	R	0

Table 5-203. Register Call Summary for Register TPCC_IER

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]

Table 5-204. TPCC_IERH

Address Offset	0x0000 1054		
Physical Address	0x01C0 1054	**Instance**	TPCC
Description	Int Enable Register (High Part): TPCC_IERH[n] In is not directly writeable. Interrupts can be enabled via writes to TPCC_IESRH and can be disabled via writes to TPCC_IECRH register. TPCC_IERH[n] In = 0: TPCC_IPRH[n] In is NOT enabled for interrupts. TPCC_IERH[n] In = 1: TPCC_IPRH[n] In IS enabled for interrupts.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	R	0
30	I62	Interrupt associated with TCC #62	R	0
29	I61	Interrupt associated with TCC #61	R	0
28	I60	Interrupt associated with TCC #60	R	0
27	I59	Interrupt associated with TCC #59	R	0
26	I58	Interrupt associated with TCC #58	R	0
25	I57	Interrupt associated with TCC #57	R	0
24	I56	Interrupt associated with TCC #56	R	0
23	I55	Interrupt associated with TCC #55	R	0
22	I54	Interrupt associated with TCC #54	R	0
21	I53	Interrupt associated with TCC #53	R	0
20	I52	Interrupt associated with TCC #52	R	0
19	I51	Interrupt associated with TCC #51	R	0
18	I50	Interrupt associated with TCC #50	R	0
17	I49	Interrupt associated with TCC #49	R	0
16	I48	Interrupt associated with TCC #48	R	0
15	I47	Interrupt associated with TCC #47	R	0
14	I46	Interrupt associated with TCC #46	R	0
13	I45	Interrupt associated with TCC #45	R	0
12	I44	Interrupt associated with TCC #44	R	0
11	I43	Interrupt associated with TCC #43	R	0
10	I42	Interrupt associated with TCC #42	R	0
9	I41	Interrupt associated with TCC #41	R	0
8	I40	Interrupt associated with TCC #40	R	0
7	I39	Interrupt associated with TCC #39	R	0
6	I38	Interrupt associated with TCC #38	R	0
5	I37	Interrupt associated with TCC #37	R	0
4	I36	Interrupt associated with TCC #36	R	0

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Bits	Field Name	Description	Type	Reset
3	I35	Interrupt associated with TCC #35	R	0
2	I34	Interrupt associated with TCC #34	R	0
1	I33	Interrupt associated with TCC #33	R	0
0	I32	Interrupt associated with TCC #32	R	0

Table 5-205. Register Call Summary for Register TPCC_IERH

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4] [5] [6] [7] [8]

Table 5-206. TPCC_IECR

Address Offset	0x0000 1058		
Physical Address	0x01C0 1058	**Instance**	TPCC
Description	Int Enable Clear Register: CPU write of 1 to the TPCC_IECR[n] In bit causes the TPCC_IER[n] In bit to be cleared. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	W	0
30	I30	Interrupt associated with TCC #30	W	0
29	I29	Interrupt associated with TCC #29	W	0
28	I28	Interrupt associated with TCC #28	W	0
27	I27	Interrupt associated with TCC #27	W	0
26	I26	Interrupt associated with TCC #26	W	0
25	I25	Interrupt associated with TCC #25	W	0
24	I24	Interrupt associated with TCC #24	W	0
23	I23	Interrupt associated with TCC #23	W	0
22	I22	Interrupt associated with TCC #22	W	0
21	I21	Interrupt associated with TCC #21	W	0
20	I20	Interrupt associated with TCC #20	W	0
19	I19	Interrupt associated with TCC #19	W	0
18	I18	Interrupt associated with TCC #18	W	0
17	I17	Interrupt associated with TCC #17	W	0
16	I16	Interrupt associated with TCC #16	W	0
15	I15	Interrupt associated with TCC #15	W	0
14	I14	Interrupt associated with TCC #14	W	0
13	I13	Interrupt associated with TCC #13	W	0
12	I12	Interrupt associated with TCC #12	W	0
11	I11	Interrupt associated with TCC #11	W	0
10	I10	Interrupt associated with TCC #10	W	0
9	I9	Interrupt associated with TCC #9	W	0
8	I8	Interrupt associated with TCC #8	W	0
7	I7	Interrupt associated with TCC #7	W	0
6	I6	Interrupt associated with TCC #6	W	0
5	I5	Interrupt associated with TCC #5	W	0

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Bits	Field Name	Description	Type	Reset
4	I4	Interrupt associated with TCC #4	W	0
3	I3	Interrupt associated with TCC #3	W	0
2	I2	Interrupt associated with TCC #2	W	0
1	I1	Interrupt associated with TCC #1	W	0
0	I0	Interrupt associated with TCC #0	W	0

Table 5-207. Register Call Summary for Register TPCC_IECR

DSP Subsystem Register Manual
- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-208. TPCC_IECRH

Address Offset	0x0000 105C		
Physical Address	0x01C0 105C	**Instance**	TPCC
Description	Int Enable Clear Register (High Part): CPU write of 1 to the TPCC_IECRH[n] In bit causes the TPCC_IERH[n] In bit to be cleared. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	W	0
30	I62	Interrupt associated with TCC #62	W	0
29	I61	Interrupt associated with TCC #61	W	0
28	I60	Interrupt associated with TCC #60	W	0
27	I59	Interrupt associated with TCC #59	W	0
26	I58	Interrupt associated with TCC #58	W	0
25	I57	Interrupt associated with TCC #57	W	0
24	I56	Interrupt associated with TCC #56	W	0
23	I55	Interrupt associated with TCC #55	W	0
22	I54	Interrupt associated with TCC #54	W	0
21	I53	Interrupt associated with TCC #53	W	0
20	I52	Interrupt associated with TCC #52	W	0
19	I51	Interrupt associated with TCC #51	W	0
18	I50	Interrupt associated with TCC #50	W	0
17	I49	Interrupt associated with TCC #49	W	0
16	I48	Interrupt associated with TCC #48	W	0
15	I47	Interrupt associated with TCC #47	W	0
14	I46	Interrupt associated with TCC #46	W	0
13	I45	Interrupt associated with TCC #45	W	0
12	I44	Interrupt associated with TCC #44	W	0
11	I43	Interrupt associated with TCC #43	W	0
10	I42	Interrupt associated with TCC #42	W	0
9	I41	Interrupt associated with TCC #41	W	0
8	I40	Interrupt associated with TCC #40	W	0
7	I39	Interrupt associated with TCC #39	W	0
6	I38	Interrupt associated with TCC #38	W	0

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Bits	Field Name	Description	Type	Reset
5	I37	Interrupt associated with TCC #37	W	0
4	I36	Interrupt associated with TCC #36	W	0
3	I35	Interrupt associated with TCC #35	W	0
2	I34	Interrupt associated with TCC #34	W	0
1	I33	Interrupt associated with TCC #33	W	0
0	I32	Interrupt associated with TCC #32	W	0

Table 5-209. Register Call Summary for Register TPCC_IECRH

DSP Subsystem Register Manual

- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-210. TPCC_IESR

Address Offset	0x0000 1060		
Physical Address	0x01C0 1060	**Instance**	TPCC
Description	Int Enable Set Register: CPU write of 1 to the TPCC_IESR[n] In bit causes the TPCC_IESR[n] In bit to be set. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	W	0
30	I30	Interrupt associated with TCC #30	W	0
29	I29	Interrupt associated with TCC #29	W	0
28	I28	Interrupt associated with TCC #28	W	0
27	I27	Interrupt associated with TCC #27	W	0
26	I26	Interrupt associated with TCC #26	W	0
25	I25	Interrupt associated with TCC #25	W	0
24	I24	Interrupt associated with TCC #24	W	0
23	I23	Interrupt associated with TCC #23	W	0
22	I22	Interrupt associated with TCC #22	W	0
21	I21	Interrupt associated with TCC #21	W	0
20	I20	Interrupt associated with TCC #20	W	0
19	I19	Interrupt associated with TCC #19	W	0
18	I18	Interrupt associated with TCC #18	W	0
17	I17	Interrupt associated with TCC #17	W	0
16	I16	Interrupt associated with TCC #16	W	0
15	I15	Interrupt associated with TCC #15	W	0
14	I14	Interrupt associated with TCC #14	W	0
13	I13	Interrupt associated with TCC #13	W	0
12	I12	Interrupt associated with TCC #12	W	0
11	I11	Interrupt associated with TCC #11	W	0
10	I10	Interrupt associated with TCC #10	W	0
9	I9	Interrupt associated with TCC #9	W	0
8	I8	Interrupt associated with TCC #8	W	0
7	I7	Interrupt associated with TCC #7	W	0

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Bits	Field Name	Description	Type	Reset
6	I6	Interrupt associated with TCC #6	W	0
5	I5	Interrupt associated with TCC #5	W	0
4	I4	Interrupt associated with TCC #4	W	0
3	I3	Interrupt associated with TCC #3	W	0
2	I2	Interrupt associated with TCC #2	W	0
1	I1	Interrupt associated with TCC #1	W	0
0	I0	Interrupt associated with TCC #0	W	0

Table 5-211. Register Call Summary for Register TPCC_IESR

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4] [5] [6]

Table 5-212. TPCC_IESRH

Address Offset	0x0000 1064		
Physical Address	0x01C0 1064	**Instance**	TPCC
Description	Int Enable Set Register (High Part): CPU write of 1 to the TPCC_IESRH[n] In bit causes the TPCC_IESRH[n] In bit to be set. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	W	0
30	I62	Interrupt associated with TCC #62	W	0
29	I61	Interrupt associated with TCC #61	W	0
28	I60	Interrupt associated with TCC #60	W	0
27	I59	Interrupt associated with TCC #59	W	0
26	I58	Interrupt associated with TCC #58	W	0
25	I57	Interrupt associated with TCC #57	W	0
24	I56	Interrupt associated with TCC #56	W	0
23	I55	Interrupt associated with TCC #55	W	0
22	I54	Interrupt associated with TCC #54	W	0
21	I53	Interrupt associated with TCC #53	W	0
20	I52	Interrupt associated with TCC #52	W	0
19	I51	Interrupt associated with TCC #51	W	0
18	I50	Interrupt associated with TCC #50	W	0
17	I49	Interrupt associated with TCC #49	W	0
16	I48	Interrupt associated with TCC #48	W	0
15	I47	Interrupt associated with TCC #47	W	0
14	I46	Interrupt associated with TCC #46	W	0
13	I45	Interrupt associated with TCC #45	W	0
12	I44	Interrupt associated with TCC #44	W	0
11	I43	Interrupt associated with TCC #43	W	0
10	I42	Interrupt associated with TCC #42	W	0
9	I41	Interrupt associated with TCC #41	W	0
8	I40	Interrupt associated with TCC #40	W	0

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Bits	Field Name	Description	Type	Reset
7	I39	Interrupt associated with TCC #39	W	0
6	I38	Interrupt associated with TCC #38	W	0
5	I37	Interrupt associated with TCC #37	W	0
4	I36	Interrupt associated with TCC #36	W	0
3	I35	Interrupt associated with TCC #35	W	0
2	I34	Interrupt associated with TCC #34	W	0
1	I33	Interrupt associated with TCC #33	W	0
0	I32	Interrupt associated with TCC #32	W	0

Table 5-213. Register Call Summary for Register TPCC_IESRH

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4] [5] [6]

Table 5-214. TPCC_IPR

Address Offset	0x0000 1068		
Physical Address	0x01C0 1068	**Instance**	TPCC
Description	Interrupt Pending Register: TPCC_IPR[n] In bit is set when a interrupt completion code with TCC of N is detected. TPCC_IPR[n] In bit is cleared via software by writing a 1 to TPCC_ICR[n] In bit.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	R	0
30	I30	Interrupt associated with TCC #30	R	0
29	I29	Interrupt associated with TCC #29	R	0
28	I28	Interrupt associated with TCC #28	R	0
27	I27	Interrupt associated with TCC #27	R	0
26	I26	Interrupt associated with TCC #26	R	0
25	I25	Interrupt associated with TCC #25	R	0
24	I24	Interrupt associated with TCC #24	R	0
23	I23	Interrupt associated with TCC #23	R	0
22	I22	Interrupt associated with TCC #22	R	0
21	I21	Interrupt associated with TCC #21	R	0
20	I20	Interrupt associated with TCC #20	R	0
19	I19	Interrupt associated with TCC #19	R	0
18	I18	Interrupt associated with TCC #18	R	0
17	I17	Interrupt associated with TCC #17	R	0
16	I16	Interrupt associated with TCC #16	R	0
15	I15	Interrupt associated with TCC #15	R	0
14	I14	Interrupt associated with TCC #14	R	0
13	I13	Interrupt associated with TCC #13	R	0
12	I12	Interrupt associated with TCC #12	R	0
11	I11	Interrupt associated with TCC #11	R	0
10	I10	Interrupt associated with TCC #10	R	0
9	I9	Interrupt associated with TCC #9	R	0

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Bits	Field Name	Description	Type	Reset
8	I8	Interrupt associated with TCC #8	R	0
7	I7	Interrupt associated with TCC #7	R	0
6	I6	Interrupt associated with TCC #6	R	0
5	I5	Interrupt associated with TCC #5	R	0
4	I4	Interrupt associated with TCC #4	R	0
3	I3	Interrupt associated with TCC #3	R	0
2	I2	Interrupt associated with TCC #2	R	0
1	I1	Interrupt associated with TCC #1	R	0
0	I0	Interrupt associated with TCC #0	R	0

Table 5-215. Register Call Summary for Register TPCC_IPR

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- DMA Interrupt Service Routine: [0] [1] [2] [3] [4] [5] [6] [7]

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- TPCC Register Summary: [8]
- TPCC Register Description: [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]

Table 5-216. TPCC_IPRH

Address Offset	0x0000 106C		
Physical Address	0x01C0 106C	**Instance**	TPCC
Description	Interrupt Pending Register (High Part): TPCC_IPRH[n] In bit is set when a interrupt completion code with TCC of N is detected. TPCC_IPRH[n] In bit is cleared via software by writing a 1 to TPCC_ICRH[n] In bit.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	R	0
30	I62	Interrupt associated with TCC #62	R	0
29	I61	Interrupt associated with TCC #61	R	0
28	I60	Interrupt associated with TCC #60	R	0
27	I59	Interrupt associated with TCC #59	R	0
26	I58	Interrupt associated with TCC #58	R	0
25	I57	Interrupt associated with TCC #57	R	0
24	I56	Interrupt associated with TCC #56	R	0
23	I55	Interrupt associated with TCC #55	R	0
22	I54	Interrupt associated with TCC #54	R	0
21	I53	Interrupt associated with TCC #53	R	0
20	I52	Interrupt associated with TCC #52	R	0
19	I51	Interrupt associated with TCC #51	R	0
18	I50	Interrupt associated with TCC #50	R	0
17	I49	Interrupt associated with TCC #49	R	0
16	I48	Interrupt associated with TCC #48	R	0
15	I47	Interrupt associated with TCC #47	R	0
14	I46	Interrupt associated with TCC #46	R	0
13	I45	Interrupt associated with TCC #45	R	0
12	I44	Interrupt associated with TCC #44	R	0

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Bits	Field Name	Description	Type	Reset
11	I43	Interrupt associated with TCC #43	R	0
10	I42	Interrupt associated with TCC #42	R	0
9	I41	Interrupt associated with TCC #41	R	0
8	I40	Interrupt associated with TCC #40	R	0
7	I39	Interrupt associated with TCC #39	R	0
6	I38	Interrupt associated with TCC #38	R	0
5	I37	Interrupt associated with TCC #37	R	0
4	I36	Interrupt associated with TCC #36	R	0
3	I35	Interrupt associated with TCC #35	R	0
2	I34	Interrupt associated with TCC #34	R	0
1	I33	Interrupt associated with TCC #33	R	0
0	I32	Interrupt associated with TCC #32	R	0

Table 5-217. Register Call Summary for Register TPCC_IPRH

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

Table 5-218. TPCC_ICR

Address Offset	0x0000 1070		
Physical Address	0x01C0 1070	**Instance**	TPCC
Description	Interrupt Clear Register: CPU write of 1 to the TPCC_ICR[n] In bit causes the TPCC_IPR[n] In bit to be cleared. CPU write of 0 has no effect. All TPCC_IPR[n] In bits must be cleared before additional interrupts will be asserted by CC.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	W	0
30	I30	Interrupt associated with TCC #30	W	0
29	I29	Interrupt associated with TCC #29	W	0
28	I28	Interrupt associated with TCC #28	W	0
27	I27	Interrupt associated with TCC #27	W	0
26	I26	Interrupt associated with TCC #26	W	0
25	I25	Interrupt associated with TCC #25	W	0
24	I24	Interrupt associated with TCC #24	W	0
23	I23	Interrupt associated with TCC #23	W	0
22	I22	Interrupt associated with TCC #22	W	0
21	I21	Interrupt associated with TCC #21	W	0
20	I20	Interrupt associated with TCC #20	W	0
19	I19	Interrupt associated with TCC #19	W	0
18	I18	Interrupt associated with TCC #18	W	0
17	I17	Interrupt associated with TCC #17	W	0
16	I16	Interrupt associated with TCC #16	W	0
15	I15	Interrupt associated with TCC #15	W	0
14	I14	Interrupt associated with TCC #14	W	0

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Bits	Field Name	Description	Type	Reset
13	I13	Interrupt associated with TCC #13	W	0
12	I12	Interrupt associated with TCC #12	W	0
11	I11	Interrupt associated with TCC #11	W	0
10	I10	Interrupt associated with TCC #10	W	0
9	I9	Interrupt associated with TCC #9	W	0
8	I8	Interrupt associated with TCC #8	W	0
7	I7	Interrupt associated with TCC #7	W	0
6	I6	Interrupt associated with TCC #6	W	0
5	I5	Interrupt associated with TCC #5	W	0
4	I4	Interrupt associated with TCC #4	W	0
3	I3	Interrupt associated with TCC #3	W	0
2	I2	Interrupt associated with TCC #2	W	0
1	I1	Interrupt associated with TCC #1	W	0
0	I0	Interrupt associated with TCC #0	W	0

Table 5-219. Register Call Summary for Register TPCC_ICR

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-220. TPCC_ICRH

Address Offset	0x0000 1074		
Physical Address	0x01C0 1074	**Instance**	TPCC
Description	Interrupt Clear Register (High Part): CPU write of 1 to the TPCC_ICRH[n] In bit causes the TPCC_IPRH[n] In bit to be cleared. CPU write of 0 has no effect. All TPCC_IPRH[n] In bits must be cleared before additional interrupts will be asserted by CC.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	W	0
30	I62	Interrupt associated with TCC #62	W	0
29	I61	Interrupt associated with TCC #61	W	0
28	I60	Interrupt associated with TCC #60	W	0
27	I59	Interrupt associated with TCC #59	W	0
26	I58	Interrupt associated with TCC #58	W	0
25	I57	Interrupt associated with TCC #57	W	0
24	I56	Interrupt associated with TCC #56	W	0
23	I55	Interrupt associated with TCC #55	W	0
22	I54	Interrupt associated with TCC #54	W	0
21	I53	Interrupt associated with TCC #53	W	0
20	I52	Interrupt associated with TCC #52	W	0
19	I51	Interrupt associated with TCC #51	W	0
18	I50	Interrupt associated with TCC #50	W	0
17	I49	Interrupt associated with TCC #49	W	0
16	I48	Interrupt associated with TCC #48	W	0

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Bits	Field Name	Description	Type	Reset
15	I47	Interrupt associated with TCC #47	W	0
14	I46	Interrupt associated with TCC #46	W	0
13	I45	Interrupt associated with TCC #45	W	0
12	I44	Interrupt associated with TCC #44	W	0
11	I43	Interrupt associated with TCC #43	W	0
10	I42	Interrupt associated with TCC #42	W	0
9	I41	Interrupt associated with TCC #41	W	0
8	I40	Interrupt associated with TCC #40	W	0
7	I39	Interrupt associated with TCC #39	W	0
6	I38	Interrupt associated with TCC #38	W	0
5	I37	Interrupt associated with TCC #37	W	0
4	I36	Interrupt associated with TCC #36	W	0
3	I35	Interrupt associated with TCC #35	W	0
2	I34	Interrupt associated with TCC #34	W	0
1	I33	Interrupt associated with TCC #33	W	0
0	I32	Interrupt associated with TCC #32	W	0

Table 5-221. Register Call Summary for Register TPCC_ICRH

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-222. TPCC_IEVAL

Address Offset	0x0000 1078		
Physical Address	0x01C0 1078	**Instance**	TPCC
Description	Interrupt Eval Register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SET	EVAL

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	write 0's for future compatibility	W	0x0000 0000
1	SET	Interrupt Set: CPU write of 1 to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable (IERn) and status (IPRn). CPU write of 0 has no effect.	W	0
0	EVAL	Interrupt Evaluate: CPU write of 1 to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts (IERn) are still pending (IPRn). CPU write of 0 has no effect..	W	0

Table 5-223. Register Call Summary for Register TPCC_IEVAL

DSP Subsystem Programming Guide
- DMA Interrupt Service Routine: [0]

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- TPCC Register Summary: [1]

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Table 5-224. TPCC_QER

Address Offset	0x0000 1080		
Physical Address	0x01C0 1080	**Instance**	TPCC
Description	QDMA Event Register: If TPCC_QER[n] En bit is set, then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TPCC_QER[n] En bit is set when a vbus write byte matches the address defined in the TPCC_QCHMAPN_j register. TPCC_QER[n] En bit is cleared when the corresponding event is prioritized and serviced. TPCC_QER[n] En is also cleared when user writes a 1 to the TPCC_QSECR[n] En bit. If the TPCC_QER[n] En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and TPCC_QEER register is set, then the corresponding bit in the QDMA Event Missed Register is set.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	reads return 0's	R	0x000000
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-225. Register Call Summary for Register TPCC_QER

DSP Subsystem Functional Description

- DMA Versus QDMA: [0] [1] [2] [3]

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- TPCC Register Summary: [4]
- TPCC Register Description: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]

Table 5-226. TPCC_QEER

Address Offset	0x0000 1084		
Physical Address	0x01C0 1084	**Instance**	TPCC
Description	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. TPCC_QEER[n] En is not directly writeable. QDMA channels can be enabled via writes to TPCC_QEESR and can be disabled via writes to TPCC_QEECR register. TPCC_QEER[n] En = 1, The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in TPCC_QER[n] En. TPCC_QEER[n] En = 0, The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in TPCC_QER[n] En.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	reads return 0's	R	0x000000
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-227. Register Call Summary for Register TPCC_QEER

DSP Subsystem Functional Description
- DMA Versus QDMA: [0] [1] [2]

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- TPCC Register Summary: [3]
- TPCC Register Description: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]

Table 5-228. TPCC_QEECR

Address Offset	0x0000 1088		
Physical Address	0x01C0 1088	**Instance**	TPCC
Description	QDMA Event Enable Clear Register: CPU write of 1 to the TPCC_QEECR[n] En bit causes the TPCC_QEER[n] En bit to be cleared. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	write 0's for future compatibility	W	0x000000
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-229. Register Call Summary for Register TPCC_QEECR

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

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Table 5-230. TPCC_QEESR

Address Offset	0x0000 108C
Physical Address	0x01C0 108C **Instance** TPCC
Description	QDMA Event Enable Set Register: CPU write of 1 to the TPCC_QEESR[n] En bit causes the TPCC_QEESR[n] En bit to be set. CPU write of 0 has no effect..
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	write 0's for future compatibility	W	0x000000
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-231. Register Call Summary for Register TPCC_QEESR

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4] [5] [6]

Table 5-232. TPCC_QSER

Address Offset	0x0000 1090
Physical Address	0x01C0 1090 **Instance** TPCC
Description	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (TPCC_QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	reads return 0's	R	0x000000
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

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Table 5-233. Register Call Summary for Register TPCC_QSER

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-234. TPCC_QSECR

Address Offset	0x0000 1094		
Physical Address	0x01C0 1094	**Instance**	TPCC
Description	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the TPCC_QSER and TPCC_QER register (note that this is slightly different than the TPCC_SER operation, which does not clear the TPCC_ER[n] En register). CPU write of 1 to the TPCC_QSECR[n] En bit clears the TPCC_QSER[n] En and TPCC_QER[n] En register fields. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	write 0's for future compatibility	W	0x000000
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-235. Register Call Summary for Register TPCC_QSECR

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- TPCC Register Summary: [0]
- TPCC Register Description: [1] [2] [3] [4]

Table 5-236. TPCC_ER_RN_k

Address Offset	0x0000 2000 + (0x200 * k)		
Physical Address	0x01C0 2000 + (0x200 * k)	**Instance**	TPCC
Description	Event Register: If TPCC_ER[n] En bit is set and the TPCC_EER[n] En bit is also set, then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TPCC_ER[n] En bit is set when the input event #n transitions from inactive (low) to active (high), regardless of the state of TPCC_EER[n] En bit. TPCC_ER[n] En bit is cleared when the corresponding event is prioritized and serviced. If the TPCC_ER[n] En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the TPCC_EER register is set, then the corresponding bit in the Event Missed Register is set. Event N can be cleared via software by writing a 1 to the TPCC_ECR pseudo-register.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	R	0
30	E30	Event #30	R	0
29	E29	Event #29	R	0
28	E28	Event #28	R	0
27	E27	Event #27	R	0
26	E26	Event #26	R	0
25	E25	Event #25	R	0
24	E24	Event #24	R	0
23	E23	Event #23	R	0
22	E22	Event #22	R	0
21	E21	Event #21	R	0
20	E20	Event #20	R	0
19	E19	Event #19	R	0
18	E18	Event #18	R	0
17	E17	Event #17	R	0
16	E16	Event #16	R	0
15	E15	Event #15	R	0
14	E14	Event #14	R	0
13	E13	Event #13	R	0
12	E12	Event #12	R	0
11	E11	Event #11	R	0
10	E10	Event #10	R	0
9	E9	Event #9	R	0
8	E8	Event #8	R	0
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-237. Register Call Summary for Register TPCC_ER_RN_k

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- TPCC Register Summary: [0]

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Table 5-238. TPCC_ERH_RN_k

Address Offset	0x0000 2004 + (0x200 * k)		
Physical Address	0x01C0 2004 + (0x200 * k)	**Instance**	TPCC
Description	Event Register (High Part): If TPCC_ERH[n] En bit is set and the TPCC_EERH[n] En bit is also set, then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. TPCC_ERH[n] En bit is set when the input event #n transitions from inactive (low) to active (high), regardless of the state of TPCC_EERH[n] En bit. TPCC_ER[n] En bit is cleared when the corresponding event is prioritized and serviced. If the TPCC_ERH[n] En bit is already set and a new inactive to active transition is detected onTPCC_ERH_RN_k the input event #n input AND the corresponding bit in the TPCC_EERH register is set, then the corresponding bit in the Event Missed Register is set. Event N can be cleared via software by writing a 1 to the TPCC_ECRH pseudo-register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	R	0
30	E62	Event #62	R	0
29	E61	Event #61	R	0
28	E60	Event #60	R	0
27	E59	Event #59	R	0
26	E58	Event #58	R	0
25	E57	Event #57	R	0
24	E56	Event #56	R	0
23	E55	Event #55	R	0
22	E54	Event #54	R	0
21	E53	Event #53	R	0
20	E52	Event #52	R	0
19	E51	Event #51	R	0
18	E50	Event #50	R	0
17	E49	Event #49	R	0
16	E48	Event #48	R	0
15	E47	Event #47	R	0
14	E46	Event #46	R	0
13	E45	Event #45	R	0
12	E44	Event #44	R	0
11	E43	Event #43	R	0
10	E42	Event #42	R	0
9	E41	Event #41	R	0
8	E40	Event #40	R	0
7	E39	Event #39	R	0
6	E38	Event #38	R	0
5	E37	Event #37	R	0
4	E36	Event #36	R	0
3	E35	Event #35	R	0
2	E34	Event #34	R	0
1	E33	Event #33	R	0
0	E32	Event #32	R	0

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Table 5-239. Register Call Summary for Register TPCC_ERH_RN_k

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- TPCC Register Summary: [0]
- TPCC Register Description: [1]

Table 5-240. TPCC_ECR_RN_k

Address Offset	0x0000 2008 + (0x200 * k)		
Physical Address	0x01C0 2008 + (0x200 * k)	**Instance**	TPCC
Description	Event Clear Register: CPU write of 1 to the TPCC_ECR[n] En bit causes the TPCC_ER[n] En bit to be cleared. CPU write of 0 has no effect.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0
24	E24	Event #24	W	0
23	E23	Event #23	W	0
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

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Table 5-241. Register Call Summary for Register TPCC_ECR_RN_k

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- TPCC Register Summary: [0]

Table 5-242. TPCC_ECRH_RN_k

Address Offset	0x0000 200C + (0x200 * k)
Physical Address	0x01C0 200C + (0x200 * k) **Instance** TPCC
Description	Event Clear Register (High Part): CPU write of 1 to the TPCC_ECRH[n] En bit causes the TPCC_ERH[n] En bit to be cleared. CPU write of 0 has no effect.
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0
25	E57	Event #57	W	0
24	E56	Event #56	W	0
23	E55	Event #55	W	0
22	E54	Event #54	W	0
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

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Table 5-243. Register Call Summary for Register TPCC_ECRH_RN_k

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- TPCC Register Summary: [0]

Table 5-244. TPCC_ESR_RN_k

Address Offset	0x0000 2010 + (0x200 * k)
Physical Address	0x01C0 2010 + (0x200 * k) **Instance** TPCC
Description	Event Set Register: CPU write of 1 to the TPCC_ESR[n] En bit causes the TPCC_ER[n] En bit to be set. CPU write of 0 has no effect.
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0
24	E24	Event #24	W	0
23	E23	Event #23	W	0
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

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Table 5-245. Register Call Summary for Register TPCC_ESR_RN_k

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- TPCC Register Summary: [0]

Table 5-246. TPCC_ESRH_RN_k

Address Offset	0x0000 2014 + (0x200 * k)		
Physical Address	0x01C0 2014 + (0x200 * k)	**Instance**	TPCC
Description	Event Set Register (High Part) CPU write of 1 to the TPCC_ESRH[n] En bit causes the TPCC_ERH[n] En bit to be set. CPU write of 0 has no effect.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0
25	E57	Event #57	W	0
24	E56	Event #56	W	0
23	E55	Event #55	W	0
22	E54	Event #54	W	0
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

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Table 5-247. Register Call Summary for Register TPCC_ESRH_RN_k

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- TPCC Register Summary: [0]

Table 5-248. TPCC_CER_RN_k

Address Offset	0x0000 2018 + (0x200 * k)		
Physical Address	0x01C0 2018 + (0x200 * k)	**Instance**	TPCC
Description	Chained Event Register: If TPCC_CER[n] En bit is set (regardless of state of TPCC_EER[n] En), then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TPCC_CER[n] En bit is set when a chaining completion code is returned from one of the TPTCs via the completion interface, or is generated internally via Early Completion path. TPCC_CER[n] En bit is cleared when the corresponding event is prioritized and serviced. If the TPCC_CER[n] En bit is already set and the corresponding chaining completion code is returned from the TC, then the corresponding bit in the Event Missed Register is set. TPCC_CER[n] En cannot be set or cleared via software.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	R	0
30	E30	Event #30	R	0
29	E29	Event #29	R	0
28	E28	Event #28	R	0
27	E27	Event #27	R	0
26	E26	Event #26	R	0
25	E25	Event #25	R	0
24	E24	Event #24	R	0
23	E23	Event #23	R	0
22	E22	Event #22	R	0
21	E21	Event #21	R	0
20	E20	Event #20	R	0
19	E19	Event #19	R	0
18	E18	Event #18	R	0
17	E17	Event #17	R	0
16	E16	Event #16	R	0
15	E15	Event #15	R	0
14	E14	Event #14	R	0
13	E13	Event #13	R	0
12	E12	Event #12	R	0
11	E11	Event #11	R	0
10	E10	Event #10	R	0
9	E9	Event #9	R	0
8	E8	Event #8	R	0
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0

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Bits	Field Name	Description	Type	Reset
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-249. Register Call Summary for Register TPCC_CER_RN_k

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-250. TPCC_CERH_RN_k

Address Offset	0x0000 201C + (0x200 * k)		
Physical Address	0x01C0 201C + (0x200 * k)	**Instance**	TPCC
Description	Chained Event Register (High Part): If TPCC_CERH[n] En bit is set (regardless of state of TPCC_EERH[n] En), then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TPCC_CERH[n] En bit is set when a chaining completion code is returned from one of the TPTCs via the completion interface, or is generated internally via Early Completion path. TPCC_CERH[n] bit is cleared when the corresponding event is prioritized and serviced. If the TPCC_CERH[n] bit is already set and the corresponding chaining completion code is returned from the TC, then the corresponding bit in the Event Missed Register is set. TPCC_CERH[n] cannot be set or cleared via software.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	R	0
30	E62	Event #62	R	0
29	E61	Event #61	R	0
28	E60	Event #60	R	0
27	E59	Event #59	R	0
26	E58	Event #58	R	0
25	E57	Event #57	R	0
24	E56	Event #56	R	0
23	E55	Event #55	R	0
22	E54	Event #54	R	0
21	E53	Event #53	R	0
20	E52	Event #52	R	0
19	E51	Event #51	R	0
18	E50	Event #50	R	0
17	E49	Event #49	R	0
16	E48	Event #48	R	0
15	E47	Event #47	R	0
14	E46	Event #46	R	0
13	E45	Event #45	R	0
12	E44	Event #44	R	0
11	E43	Event #43	R	0
10	E42	Event #42	R	0
9	E41	Event #41	R	0
8	E40	Event #40	R	0

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Bits	Field Name	Description	Type	Reset
7	E39	Event #39	R	0
6	E38	Event #38	R	0
5	E37	Event #37	R	0
4	E36	Event #36	R	0
3	E35	Event #35	R	0
2	E34	Event #34	R	0
1	E33	Event #33	R	0
0	E32	Event #32	R	0

Table 5-251. Register Call Summary for Register TPCC_CERH_RN_k

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-252. TPCC_EER_RN_k

Address Offset	0x0000 2020 + (0x200 * k)		
Physical Address	0x01C0 2020 + (0x200 * k)	**Instance**	TPCC
Description	Event Enable Register: Enables DMA transfers for TPCC_ER[n] En pending events. TPCC_ER[n] En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (TPCC_CER) or Event Set Register (TPCC_ESR). Note that if a bit is set in TPCC_ER[n] En while TPCC_EER[n] En is disabled, no action is taken. If TPCC_EER[n] En is enabled at a later point (and TPCC_ER[n] En has not been cleared via software) then the event will be recognized as a valid 'TR Sync' TPCC_EER[n] En is not directly writeable. Events can be enabled via writes to TPCC_EESR and can be disabled via writes to TPCC_EECR register. TPCC_EER[n] En = 0: TPCC_ER[n] En is not enabled to trigger DMA transfers. TPCC_EER[n] En = 1: TPCC_ER[n] En is enabled to trigger DMA transfers.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	R	0
30	E30	Event #30	R	0
29	E29	Event #29	R	0
28	E28	Event #28	R	0
27	E27	Event #27	R	0
26	E26	Event #26	R	0
25	E25	Event #25	R	0
24	E24	Event #24	R	0
23	E23	Event #23	R	0
22	E22	Event #22	R	0
21	E21	Event #21	R	0
20	E20	Event #20	R	0
19	E19	Event #19	R	0
18	E18	Event #18	R	0
17	E17	Event #17	R	0
16	E16	Event #16	R	0
15	E15	Event #15	R	0
14	E14	Event #14	R	0

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Bits	Field Name	Description	Type	Reset
13	E13	Event #13	R	0
12	E12	Event #12	R	0
11	E11	Event #11	R	0
10	E10	Event #10	R	0
9	E9	Event #9	R	0
8	E8	Event #8	R	0
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-253. Register Call Summary for Register TPCC_EER_RN_k

DSP Subsystem Register Manual

- TPCC Register Summary: [0]

Table 5-254. TPCC_EERH_RN_k

Address Offset	0x0000 2024 + (0x200 * k)		
Physical Address	0x01C0 2024 + (0x200 * k)	**Instance**	TPCC
Description	Event Enable Register (High Part): Enables DMA transfers for TPCC_ERH[n] En pending events. TPCC_ERH[n] En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (TPCC_CERH) or Event Set Register (TPCC_ESRH). Note that if a bit is set in TPCC_ERH[n] En while TPCC_EERH[n] En is disabled, no action is taken. If TPCC_EERH[n] En is enabled at a later point (and TPCC_ERH[n] En has not been cleared via software) then the event will be recognized as a valid 'TR Sync' TPCC_EERH[n] En is not directly writeable. Events can be enabled via writes to TPCC_EESRH and can be disabled via writes to TPCC_EECRH register. TPCC_EERH[n] En = 0: TPCC_ER[n] En is not enabled to trigger DMA transfers. TPCC_EERH[n] En = 1: TPCC_ER[n] En is enabled to trigger DMA transfers.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	R	0
30	E62	Event #62	R	0
29	E61	Event #61	R	0
28	E60	Event #60	R	0
27	E59	Event #59	R	0
26	E58	Event #58	R	0
25	E57	Event #57	R	0
24	E56	Event #56	R	0
23	E55	Event #55	R	0
22	E54	Event #54	R	0

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Bits	Field Name	Description	Type	Reset
21	E53	Event #53	R	0
20	E52	Event #52	R	0
19	E51	Event #51	R	0
18	E50	Event #50	R	0
17	E49	Event #49	R	0
16	E48	Event #48	R	0
15	E47	Event #47	R	0
14	E46	Event #46	R	0
13	E45	Event #45	R	0
12	E44	Event #44	R	0
11	E43	Event #43	R	0
10	E42	Event #42	R	0
9	E41	Event #41	R	0
8	E40	Event #40	R	0
7	E39	Event #39	R	0
6	E38	Event #38	R	0
5	E37	Event #37	R	0
4	E36	Event #36	R	0
3	E35	Event #35	R	0
2	E34	Event #34	R	0
1	E33	Event #33	R	0
0	E32	Event #32	R	0

Table 5-255. Register Call Summary for Register TPCC_EERH_RN_k

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-256. TPCC_EECR_RN_k

Address Offset	0x0000 2028 + (0x200 * k)		
Physical Address	0x01C0 2028 + (0x200 * k)	**Instance**	TPCC
Description	Event Enable Clear Register: CPU write of 1 to the TPCC_EECR[n] En bit causes the TPCC_EER[n] En bit to be cleared. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0
24	E24	Event #24	W	0
23	E23	Event #23	W	0

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Bits	Field Name	Description	Type	Reset
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-257. Register Call Summary for Register TPCC_EECR_RN_k

DSP Subsystem Register Manual

- TPCC Register Summary: [0]

Table 5-258. TPCC_EECRH_RN_k

Address Offset	0x0000 202C + (0x200 * k)		
Physical Address	0x01C0 202C + (0x200 * k)	**Instance**	TPCC
Description	Event Enable Clear Register (High Part): CPU write of 1 to the TPCC_EECRH[n] En bit causes the TPCC_EERH[n] En bit to be cleared. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0
25	E57	Event #57	W	0
24	E56	Event #56	W	0

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Bits	Field Name	Description	Type	Reset
23	E55	Event #55	W	0
22	E54	Event #54	W	0
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

Table 5-259. Register Call Summary for Register TPCC_EECRH_RN_k

DSP Subsystem Register Manual

- TPCC Register Summary: [0]

Table 5-260. TPCC_EESR_RN_k

Address Offset	0x0000 2030 + (0x200 * k)		
Physical Address	0x01C0 2030 + (0x200 * k)	**Instance**	TPCC
Description	Event Enable Set Register: CPU write of 1 to the TPCC_EESR[n] En bit causes the TPCC_EER[n] En bit to be set. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0

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Bits	Field Name	Description	Type	Reset
24	E24	Event #24	W	0
23	E23	Event #23	W	0
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-261. Register Call Summary for Register TPCC_EESR_RN_k

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- TPCC Register Summary: [0]

Table 5-262. TPCC_EESRH_RN_k

Address Offset	0x0000 2034 + (0x200 * k)		
Physical Address	0x01C0 2034 + (0x200 * k)	**Instance**	TPCC
Description	Event Enable Set Register (High Part): CPU write of 1 to the TPCC_EESRH[n] En bit causes the TPCC_EERH[n] En bit to be set. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0

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Bits	Field Name	Description	Type	Reset
25	E57	Event #57	W	0
24	E56	Event #56	W	0
23	E55	Event #55	W	0
22	E54	Event #54	W	0
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

Table 5-263. Register Call Summary for Register TPCC_EESRH_RN_k

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- TPCC Register Summary: [0]

Table 5-264. TPCC_SER_RN_k

Address Offset	0x0000 2038 + (0x200 * k)		
Physical Address	0x01C0 2038 + (0x200 * k)	**Instance**	TPCC
Description	Secondary Event Register: The secondary event register is used along with the Event Register (TPCC_ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31	E31	Event #31	R	0
30	E30	Event #30	R	0
29	E29	Event #29	R	0

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Bits	Field Name	Description	Type	Reset
28	E28	Event #28	R	0
27	E27	Event #27	R	0
26	E26	Event #26	R	0
25	E25	Event #25	R	0
24	E24	Event #24	R	0
23	E23	Event #23	R	0
22	E22	Event #22	R	0
21	E21	Event #21	R	0
20	E20	Event #20	R	0
19	E19	Event #19	R	0
18	E18	Event #18	R	0
17	E17	Event #17	R	0
16	E16	Event #16	R	0
15	E15	Event #15	R	0
14	E14	Event #14	R	0
13	E13	Event #13	R	0
12	E12	Event #12	R	0
11	E11	Event #11	R	0
10	E10	Event #10	R	0
9	E9	Event #9	R	0
8	E8	Event #8	R	0
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-265. Register Call Summary for Register TPCC_SER_RN_k

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- TPCC Register Summary: [0]

Table 5-266. TPCC_SERH_RN_k

Address Offset	0x0000 203C + (0x200 * k)		
Physical Address	0x01C0 203C + (0x200 * k)	**Instance**	TPCC
Description	Secondary Event Register (High Part): The secondary event register is used along with the Event Register (TPCC_ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

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Bits	Field Name	Description	Type	Reset
31	E63	Event #63	R	0
30	E62	Event #62	R	0
29	E61	Event #61	R	0
28	E60	Event #60	R	0
27	E59	Event #59	R	0
26	E58	Event #58	R	0
25	E57	Event #57	R	0
24	E56	Event #56	R	0
23	E55	Event #55	R	0
22	E54	Event #54	R	0
21	E53	Event #53	R	0
20	E52	Event #52	R	0
19	E51	Event #51	R	0
18	E50	Event #50	R	0
17	E49	Event #49	R	0
16	E48	Event #48	R	0
15	E47	Event #47	R	0
14	E46	Event #46	R	0
13	E45	Event #45	R	0
12	E44	Event #44	R	0
11	E43	Event #43	R	0
10	E42	Event #42	R	0
9	E41	Event #41	R	0
8	E40	Event #40	R	0
7	E39	Event #39	R	0
6	E38	Event #38	R	0
5	E37	Event #37	R	0
4	E36	Event #36	R	0
3	E35	Event #35	R	0
2	E34	Event #34	R	0
1	E33	Event #33	R	0
0	E32	Event #32	R	0

Table 5-267. Register Call Summary for Register TPCC_SERH_RN_k

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- TPCC Register Summary: [0]

Table 5-268. TPCC_SECR_RN_k

Address Offset	0x0000 2040 + (0x200 * k)
Physical Address	0x01C0 2040 + (0x200 * k) **Instance** TPCC
Description	Secondary Event Clear Register: The secondary event clear register is used to clear the status of the TPCC_SER registers. CPU write of 1 to the TPCC_SECR[n] En bit clears the TPCC_SER register. CPU write of 0 has no effect.
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

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Bits	Field Name	Description	Type	Reset
31	E31	Event #31	W	0
30	E30	Event #30	W	0
29	E29	Event #29	W	0
28	E28	Event #28	W	0
27	E27	Event #27	W	0
26	E26	Event #26	W	0
25	E25	Event #25	W	0
24	E24	Event #24	W	0
23	E23	Event #23	W	0
22	E22	Event #22	W	0
21	E21	Event #21	W	0
20	E20	Event #20	W	0
19	E19	Event #19	W	0
18	E18	Event #18	W	0
17	E17	Event #17	W	0
16	E16	Event #16	W	0
15	E15	Event #15	W	0
14	E14	Event #14	W	0
13	E13	Event #13	W	0
12	E12	Event #12	W	0
11	E11	Event #11	W	0
10	E10	Event #10	W	0
9	E9	Event #9	W	0
8	E8	Event #8	W	0
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-269. Register Call Summary for Register TPCC_SECR_RN_k

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- TPCC Register Summary: [0]

Table 5-270. TPCC_SECRH_RN_k

Address Offset	0x0000 2044 + (0x200 * k)		
Physical Address	0x01C0 2044 + (0x200 * k)	**Instance**	TPCC
Description	Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the TPCC_SERH registers. CPU write of 1 to the TPCC_SECRH[n] En bit clears the TPCC_SERH register. CPU write of 0 has no effect.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E63	E62	E61	E60	E59	E58	E57	E56	E55	E54	E53	E52	E51	E50	E49	E48	E47	E46	E45	E44	E43	E42	E41	E40	E39	E38	E37	E36	E35	E34	E33	E32

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Bits	Field Name	Description	Type	Reset
31	E63	Event #63	W	0
30	E62	Event #62	W	0
29	E61	Event #61	W	0
28	E60	Event #60	W	0
27	E59	Event #59	W	0
26	E58	Event #58	W	0
25	E57	Event #57	W	0
24	E56	Event #56	W	0
23	E55	Event #55	W	0
22	E54	Event #54	W	0
21	E53	Event #53	W	0
20	E52	Event #52	W	0
19	E51	Event #51	W	0
18	E50	Event #50	W	0
17	E49	Event #49	W	0
16	E48	Event #48	W	0
15	E47	Event #47	W	0
14	E46	Event #46	W	0
13	E45	Event #45	W	0
12	E44	Event #44	W	0
11	E43	Event #43	W	0
10	E42	Event #42	W	0
9	E41	Event #41	W	0
8	E40	Event #40	W	0
7	E39	Event #39	W	0
6	E38	Event #38	W	0
5	E37	Event #37	W	0
4	E36	Event #36	W	0
3	E35	Event #35	W	0
2	E34	Event #34	W	0
1	E33	Event #33	W	0
0	E32	Event #32	W	0

Table 5-271. Register Call Summary for Register TPCC_SECRH_RN_k

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- TPCC Register Summary: [0]

Table 5-272. TPCC_IER_RN_k

Address Offset	0x0000 2050 + (0x200 * k)		
Physical Address	0x01C0 2050 + (0x200 * k)	**Instance**	TPCC
Description	Int Enable Register: TPCC_IER[n] In is not directly writeable. Interrupts can be enabled via writes to TPCC_IESR and can be disabled via writes to TPCC_IECR register. TPCC_IER[n] In = 0: TPCC_IPR[n] In is NOT enabled for interrupts. TPCC_IER[n] In = 1: TPCC_IPR[n] In IS enabled for interrupts.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	R	0
30	I30	Interrupt associated with TCC #30	R	0
29	I29	Interrupt associated with TCC #29	R	0
28	I28	Interrupt associated with TCC #28	R	0
27	I27	Interrupt associated with TCC #27	R	0
26	I26	Interrupt associated with TCC #26	R	0
25	I25	Interrupt associated with TCC #25	R	0
24	I24	Interrupt associated with TCC #24	R	0
23	I23	Interrupt associated with TCC #23	R	0
22	I22	Interrupt associated with TCC #22	R	0
21	I21	Interrupt associated with TCC #21	R	0
20	I20	Interrupt associated with TCC #20	R	0
19	I19	Interrupt associated with TCC #19	R	0
18	I18	Interrupt associated with TCC #18	R	0
17	I17	Interrupt associated with TCC #17	R	0
16	I16	Interrupt associated with TCC #16	R	0
15	I15	Interrupt associated with TCC #15	R	0
14	I14	Interrupt associated with TCC #14	R	0
13	I13	Interrupt associated with TCC #13	R	0
12	I12	Interrupt associated with TCC #12	R	0
11	I11	Interrupt associated with TCC #11	R	0
10	I10	Interrupt associated with TCC #10	R	0
9	I9	Interrupt associated with TCC #9	R	0
8	I8	Interrupt associated with TCC #8	R	0
7	I7	Interrupt associated with TCC #7	R	0
6	I6	Interrupt associated with TCC #6	R	0
5	I5	Interrupt associated with TCC #5	R	0
4	I4	Interrupt associated with TCC #4	R	0
3	I3	Interrupt associated with TCC #3	R	0
2	I2	Interrupt associated with TCC #2	R	0
1	I1	Interrupt associated with TCC #1	R	0
0	I0	Interrupt associated with TCC #0	R	0

Table 5-273. Register Call Summary for Register TPCC_IER_RN_k

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- TPCC Register Summary: [0]

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Table 5-274. TPCC_IERH_RN_k

Address Offset	0x0000 2054 + (0x200 * k)
Physical Address	0x01C0 2054 + (0x200 * k) **Instance** TPCC
Description	Int Enable Register (High Part): TPCC_IERH[n] In is not directly writeable. Interrupts can be enabled via writes to TPCC_IESRH and can be disabled via writes to TPCC_IECRH register. TPCC_IERH[n] In = 0: TPCC_IPRH[n] In is NOT enabled for interrupts. TPCC_IERH[n] In = 1: TPCC_IPRH[n] In IS enabled for interrupts.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	R	0
30	I62	Interrupt associated with TCC #62	R	0
29	I61	Interrupt associated with TCC #61	R	0
28	I60	Interrupt associated with TCC #60	R	0
27	I59	Interrupt associated with TCC #59	R	0
26	I58	Interrupt associated with TCC #58	R	0
25	I57	Interrupt associated with TCC #57	R	0
24	I56	Interrupt associated with TCC #56	R	0
23	I55	Interrupt associated with TCC #55	R	0
22	I54	Interrupt associated with TCC #54	R	0
21	I53	Interrupt associated with TCC #53	R	0
20	I52	Interrupt associated with TCC #52	R	0
19	I51	Interrupt associated with TCC #51	R	0
18	I50	Interrupt associated with TCC #50	R	0
17	I49	Interrupt associated with TCC #49	R	0
16	I48	Interrupt associated with TCC #48	R	0
15	I47	Interrupt associated with TCC #47	R	0
14	I46	Interrupt associated with TCC #46	R	0
13	I45	Interrupt associated with TCC #45	R	0
12	I44	Interrupt associated with TCC #44	R	0
11	I43	Interrupt associated with TCC #43	R	0
10	I42	Interrupt associated with TCC #42	R	0
9	I41	Interrupt associated with TCC #41	R	0
8	I40	Interrupt associated with TCC #40	R	0
7	I39	Interrupt associated with TCC #39	R	0
6	I38	Interrupt associated with TCC #38	R	0
5	I37	Interrupt associated with TCC #37	R	0
4	I36	Interrupt associated with TCC #36	R	0
3	I35	Interrupt associated with TCC #35	R	0
2	I34	Interrupt associated with TCC #34	R	0
1	I33	Interrupt associated with TCC #33	R	0
0	I32	Interrupt associated with TCC #32	R	0

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Table 5-275. Register Call Summary for Register TPCC_IERH_RN_k

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- TPCC Register Summary: [0]

Table 5-276. TPCC_IECR_RN_k

Address Offset	0x0000 2058 + (0x200 * k)
Physical Address	0x01C0 2058 + (0x200 * k) **Instance** TPCC
Description	Int Enable Clear Register: CPU write of 1 to the TPCC_IECR[n] In bit causes the TPCC_IER[n] In bit to be cleared. CPU write of 0 has no effect..
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	W	0
30	I30	Interrupt associated with TCC #30	W	0
29	I29	Interrupt associated with TCC #29	W	0
28	I28	Interrupt associated with TCC #28	W	0
27	I27	Interrupt associated with TCC #27	W	0
26	I26	Interrupt associated with TCC #26	W	0
25	I25	Interrupt associated with TCC #25	W	0
24	I24	Interrupt associated with TCC #24	W	0
23	I23	Interrupt associated with TCC #23	W	0
22	I22	Interrupt associated with TCC #22	W	0
21	I21	Interrupt associated with TCC #21	W	0
20	I20	Interrupt associated with TCC #20	W	0
19	I19	Interrupt associated with TCC #19	W	0
18	I18	Interrupt associated with TCC #18	W	0
17	I17	Interrupt associated with TCC #17	W	0
16	I16	Interrupt associated with TCC #16	W	0
15	I15	Interrupt associated with TCC #15	W	0
14	I14	Interrupt associated with TCC #14	W	0
13	I13	Interrupt associated with TCC #13	W	0
12	I12	Interrupt associated with TCC #12	W	0
11	I11	Interrupt associated with TCC #11	W	0
10	I10	Interrupt associated with TCC #10	W	0
9	I9	Interrupt associated with TCC #9	W	0
8	I8	Interrupt associated with TCC #8	W	0
7	I7	Interrupt associated with TCC #7	W	0
6	I6	Interrupt associated with TCC #6	W	0
5	I5	Interrupt associated with TCC #5	W	0
4	I4	Interrupt associated with TCC #4	W	0
3	I3	Interrupt associated with TCC #3	W	0
2	I2	Interrupt associated with TCC #2	W	0
1	I1	Interrupt associated with TCC #1	W	0
0	I0	Interrupt associated with TCC #0	W	0

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Table 5-277. Register Call Summary for Register TPCC_IECR_RN_k

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- TPCC Register Summary: [0]

Table 5-278. TPCC_IECRH_RN_k

Address Offset	0x0000 205C + (0x200 * k)
Physical Address	0x01C0 205C + (0x200 * k) **Instance** TPCC
Description	Int Enable Clear Register (High Part): CPU write of 1 to the TPCC_IECRH[n] In bit causes the TPCC_IERH[n] In bit to be cleared. CPU write of 0 has no effect..
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	W	0
30	I62	Interrupt associated with TCC #62	W	0
29	I61	Interrupt associated with TCC #61	W	0
28	I60	Interrupt associated with TCC #60	W	0
27	I59	Interrupt associated with TCC #59	W	0
26	I58	Interrupt associated with TCC #58	W	0
25	I57	Interrupt associated with TCC #57	W	0
24	I56	Interrupt associated with TCC #56	W	0
23	I55	Interrupt associated with TCC #55	W	0
22	I54	Interrupt associated with TCC #54	W	0
21	I53	Interrupt associated with TCC #53	W	0
20	I52	Interrupt associated with TCC #52	W	0
19	I51	Interrupt associated with TCC #51	W	0
18	I50	Interrupt associated with TCC #50	W	0
17	I49	Interrupt associated with TCC #49	W	0
16	I48	Interrupt associated with TCC #48	W	0
15	I47	Interrupt associated with TCC #47	W	0
14	I46	Interrupt associated with TCC #46	W	0
13	I45	Interrupt associated with TCC #45	W	0
12	I44	Interrupt associated with TCC #44	W	0
11	I43	Interrupt associated with TCC #43	W	0
10	I42	Interrupt associated with TCC #42	W	0
9	I41	Interrupt associated with TCC #41	W	0
8	I40	Interrupt associated with TCC #40	W	0
7	I39	Interrupt associated with TCC #39	W	0
6	I38	Interrupt associated with TCC #38	W	0
5	I37	Interrupt associated with TCC #37	W	0
4	I36	Interrupt associated with TCC #36	W	0
3	I35	Interrupt associated with TCC #35	W	0
2	I34	Interrupt associated with TCC #34	W	0
1	I33	Interrupt associated with TCC #33	W	0
0	I32	Interrupt associated with TCC #32	W	0

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Table 5-279. Register Call Summary for Register TPCC_IECRH_RN_k

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- TPCC Register Summary: [0]

Table 5-280. TPCC_IESR_RN_k

Address Offset	0x0000 2060 + (0x200 * k)		
Physical Address	0x01C0 2060 + (0x200 * k)	**Instance**	TPCC
Description	Int Enable Set Register: CPU write of 1 to the TPCC_IESR[n] In bit causes the TPCC_IESR[n] In bit to be set. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	W	0
30	I30	Interrupt associated with TCC #30	W	0
29	I29	Interrupt associated with TCC #29	W	0
28	I28	Interrupt associated with TCC #28	W	0
27	I27	Interrupt associated with TCC #27	W	0
26	I26	Interrupt associated with TCC #26	W	0
25	I25	Interrupt associated with TCC #25	W	0
24	I24	Interrupt associated with TCC #24	W	0
23	I23	Interrupt associated with TCC #23	W	0
22	I22	Interrupt associated with TCC #22	W	0
21	I21	Interrupt associated with TCC #21	W	0
20	I20	Interrupt associated with TCC #20	W	0
19	I19	Interrupt associated with TCC #19	W	0
18	I18	Interrupt associated with TCC #18	W	0
17	I17	Interrupt associated with TCC #17	W	0
16	I16	Interrupt associated with TCC #16	W	0
15	I15	Interrupt associated with TCC #15	W	0
14	I14	Interrupt associated with TCC #14	W	0
13	I13	Interrupt associated with TCC #13	W	0
12	I12	Interrupt associated with TCC #12	W	0
11	I11	Interrupt associated with TCC #11	W	0
10	I10	Interrupt associated with TCC #10	W	0
9	I9	Interrupt associated with TCC #9	W	0
8	I8	Interrupt associated with TCC #8	W	0
7	I7	Interrupt associated with TCC #7	W	0
6	I6	Interrupt associated with TCC #6	W	0
5	I5	Interrupt associated with TCC #5	W	0
4	I4	Interrupt associated with TCC #4	W	0
3	I3	Interrupt associated with TCC #3	W	0
2	I2	Interrupt associated with TCC #2	W	0
1	I1	Interrupt associated with TCC #1	W	0
0	I0	Interrupt associated with TCC #0	W	0

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Table 5-281. Register Call Summary for Register TPCC_IESR_RN_k

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- TPCC Register Summary: [0]

Table 5-282. TPCC_IESRH_RN_k

Address Offset	0x0000 2064 + (0x200 * k)
Physical Address	0x01C0 2064 + (0x200 * k) **Instance** TPCC
Description	Int Enable Set Register (High Part): CPU write of 1 to the TPCC_IESRH[n] In bit causes the TPCC_IESRH[n] In bit to be set. CPU write of 0 has no effect..
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	W	0
30	I62	Interrupt associated with TCC #62	W	0
29	I61	Interrupt associated with TCC #61	W	0
28	I60	Interrupt associated with TCC #60	W	0
27	I59	Interrupt associated with TCC #59	W	0
26	I58	Interrupt associated with TCC #58	W	0
25	I57	Interrupt associated with TCC #57	W	0
24	I56	Interrupt associated with TCC #56	W	0
23	I55	Interrupt associated with TCC #55	W	0
22	I54	Interrupt associated with TCC #54	W	0
21	I53	Interrupt associated with TCC #53	W	0
20	I52	Interrupt associated with TCC #52	W	0
19	I51	Interrupt associated with TCC #51	W	0
18	I50	Interrupt associated with TCC #50	W	0
17	I49	Interrupt associated with TCC #49	W	0
16	I48	Interrupt associated with TCC #48	W	0
15	I47	Interrupt associated with TCC #47	W	0
14	I46	Interrupt associated with TCC #46	W	0
13	I45	Interrupt associated with TCC #45	W	0
12	I44	Interrupt associated with TCC #44	W	0
11	I43	Interrupt associated with TCC #43	W	0
10	I42	Interrupt associated with TCC #42	W	0
9	I41	Interrupt associated with TCC #41	W	0
8	I40	Interrupt associated with TCC #40	W	0
7	I39	Interrupt associated with TCC #39	W	0
6	I38	Interrupt associated with TCC #38	W	0
5	I37	Interrupt associated with TCC #37	W	0
4	I36	Interrupt associated with TCC #36	W	0
3	I35	Interrupt associated with TCC #35	W	0
2	I34	Interrupt associated with TCC #34	W	0
1	I33	Interrupt associated with TCC #33	W	0
0	I32	Interrupt associated with TCC #32	W	0

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Table 5-283. Register Call Summary for Register TPCC_IESRH_RN_k

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- TPCC Register Summary: [0]

Table 5-284. TPCC_IPR_RN_k

Address Offset	0x0000 2068 + (0x200 * k)		
Physical Address	0x01C0 2068 + (0x200 * k)	**Instance**	TPCC
Description	Interrupt Pending Register: TPCC_IPR[n] In bit is set when a interrupt completion code with TCC of N is detected. TPCC_IPR[n] In bit is cleared via software by writing a 1 to TPCC_ICR[n] In bit.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	R	0
30	I30	Interrupt associated with TCC #30	R	0
29	I29	Interrupt associated with TCC #29	R	0
28	I28	Interrupt associated with TCC #28	R	0
27	I27	Interrupt associated with TCC #27	R	0
26	I26	Interrupt associated with TCC #26	R	0
25	I25	Interrupt associated with TCC #25	R	0
24	I24	Interrupt associated with TCC #24	R	0
23	I23	Interrupt associated with TCC #23	R	0
22	I22	Interrupt associated with TCC #22	R	0
21	I21	Interrupt associated with TCC #21	R	0
20	I20	Interrupt associated with TCC #20	R	0
19	I19	Interrupt associated with TCC #19	R	0
18	I18	Interrupt associated with TCC #18	R	0
17	I17	Interrupt associated with TCC #17	R	0
16	I16	Interrupt associated with TCC #16	R	0
15	I15	Interrupt associated with TCC #15	R	0
14	I14	Interrupt associated with TCC #14	R	0
13	I13	Interrupt associated with TCC #13	R	0
12	I12	Interrupt associated with TCC #12	R	0
11	I11	Interrupt associated with TCC #11	R	0
10	I10	Interrupt associated with TCC #10	R	0
9	I9	Interrupt associated with TCC #9	R	0
8	I8	Interrupt associated with TCC #8	R	0
7	I7	Interrupt associated with TCC #7	R	0
6	I6	Interrupt associated with TCC #6	R	0
5	I5	Interrupt associated with TCC #5	R	0
4	I4	Interrupt associated with TCC #4	R	0
3	I3	Interrupt associated with TCC #3	R	0
2	I2	Interrupt associated with TCC #2	R	0
1	I1	Interrupt associated with TCC #1	R	0
0	I0	Interrupt associated with TCC #0	R	0

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Table 5-285. Register Call Summary for Register TPCC_IPR_RN_k

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- TPCC Register Summary: [0]

Table 5-286. TPCC_IPRH_RN_k

Address Offset	0x0000 206C + (0x200 * k)
Physical Address	0x01C0 206C + (0x200 * k) **Instance** TPCC
Description	Interrupt Pending Register (High Part): TPCC_IPRH[n] In bit is set when a interrupt completion code with TCC of N is detected. TPCC_IPRH[n] In bit is cleared via software by writing a 1 to TPCC_ICRH[n] In bit.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	R	0
30	I62	Interrupt associated with TCC #62	R	0
29	I61	Interrupt associated with TCC #61	R	0
28	I60	Interrupt associated with TCC #60	R	0
27	I59	Interrupt associated with TCC #59	R	0
26	I58	Interrupt associated with TCC #58	R	0
25	I57	Interrupt associated with TCC #57	R	0
24	I56	Interrupt associated with TCC #56	R	0
23	I55	Interrupt associated with TCC #55	R	0
22	I54	Interrupt associated with TCC #54	R	0
21	I53	Interrupt associated with TCC #53	R	0
20	I52	Interrupt associated with TCC #52	R	0
19	I51	Interrupt associated with TCC #51	R	0
18	I50	Interrupt associated with TCC #50	R	0
17	I49	Interrupt associated with TCC #49	R	0
16	I48	Interrupt associated with TCC #48	R	0
15	I47	Interrupt associated with TCC #47	R	0
14	I46	Interrupt associated with TCC #46	R	0
13	I45	Interrupt associated with TCC #45	R	0
12	I44	Interrupt associated with TCC #44	R	0
11	I43	Interrupt associated with TCC #43	R	0
10	I42	Interrupt associated with TCC #42	R	0
9	I41	Interrupt associated with TCC #41	R	0
8	I40	Interrupt associated with TCC #40	R	0
7	I39	Interrupt associated with TCC #39	R	0
6	I38	Interrupt associated with TCC #38	R	0
5	I37	Interrupt associated with TCC #37	R	0
4	I36	Interrupt associated with TCC #36	R	0
3	I35	Interrupt associated with TCC #35	R	0
2	I34	Interrupt associated with TCC #34	R	0
1	I33	Interrupt associated with TCC #33	R	0
0	I32	Interrupt associated with TCC #32	R	0

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Table 5-287. Register Call Summary for Register TPCC_IPRH_RN_k

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- TPCC Register Summary: [0]

Table 5-288. TPCC_ICR_RN_k

Address Offset	0x0000 2070 + (0x200 * k)		
Physical Address	0x01C0 2070 + (0x200 * k)	**Instance**	TPCC
Description	Interrupt Clear Register: CPU write of 1 to the TPCC_ICR[n] In bit causes the TPCC_IPR[n] In bit to be cleared. CPU write of 0 has no effect. All TPCC_IPR[n] In bits must be cleared before additional interrupts will be asserted by CC.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0

Bits	Field Name	Description	Type	Reset
31	I31	Interrupt associated with TCC #31	W	0
30	I30	Interrupt associated with TCC #30	W	0
29	I29	Interrupt associated with TCC #29	W	0
28	I28	Interrupt associated with TCC #28	W	0
27	I27	Interrupt associated with TCC #27	W	0
26	I26	Interrupt associated with TCC #26	W	0
25	I25	Interrupt associated with TCC #25	W	0
24	I24	Interrupt associated with TCC #24	W	0
23	I23	Interrupt associated with TCC #23	W	0
22	I22	Interrupt associated with TCC #22	W	0
21	I21	Interrupt associated with TCC #21	W	0
20	I20	Interrupt associated with TCC #20	W	0
19	I19	Interrupt associated with TCC #19	W	0
18	I18	Interrupt associated with TCC #18	W	0
17	I17	Interrupt associated with TCC #17	W	0
16	I16	Interrupt associated with TCC #16	W	0
15	I15	Interrupt associated with TCC #15	W	0
14	I14	Interrupt associated with TCC #14	W	0
13	I13	Interrupt associated with TCC #13	W	0
12	I12	Interrupt associated with TCC #12	W	0
11	I11	Interrupt associated with TCC #11	W	0
10	I10	Interrupt associated with TCC #10	W	0
9	I9	Interrupt associated with TCC #9	W	0
8	I8	Interrupt associated with TCC #8	W	0
7	I7	Interrupt associated with TCC #7	W	0
6	I6	Interrupt associated with TCC #6	W	0
5	I5	Interrupt associated with TCC #5	W	0
4	I4	Interrupt associated with TCC #4	W	0
3	I3	Interrupt associated with TCC #3	W	0
2	I2	Interrupt associated with TCC #2	W	0
1	I1	Interrupt associated with TCC #1	W	0
0	I0	Interrupt associated with TCC #0	W	0

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Table 5-289. Register Call Summary for Register TPCC_ICR_RN_k

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- TPCC Register Summary: [0]

Table 5-290. TPCC_ICRH_RN_k

Address Offset	0x0000 2074 + (0x200 * k)
Physical Address	0x01C0 2074 + (0x200 * k) **Instance** TPCC
Description	Interrupt Clear Register (High Part): CPU write of 1 to the TPCC_ICRH[n] In bit causes the TPCC_IPRH[n] In bit to be cleared. CPU write of 0 has no effect. All TPCC_IPRH[n] In bits must be cleared before additional interrupts will be asserted by CC.
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I63	I62	I61	I60	I59	I58	I57	I56	I55	I54	I53	I52	I51	I50	I49	I48	I47	I46	I45	I44	I43	I42	I41	I40	I39	I38	I37	I36	I35	I34	I33	I32

Bits	Field Name	Description	Type	Reset
31	I63	Interrupt associated with TCC #63	W	0
30	I62	Interrupt associated with TCC #62	W	0
29	I61	Interrupt associated with TCC #61	W	0
28	I60	Interrupt associated with TCC #60	W	0
27	I59	Interrupt associated with TCC #59	W	0
26	I58	Interrupt associated with TCC #58	W	0
25	I57	Interrupt associated with TCC #57	W	0
24	I56	Interrupt associated with TCC #56	W	0
23	I55	Interrupt associated with TCC #55	W	0
22	I54	Interrupt associated with TCC #54	W	0
21	I53	Interrupt associated with TCC #53	W	0
20	I52	Interrupt associated with TCC #52	W	0
19	I51	Interrupt associated with TCC #51	W	0
18	I50	Interrupt associated with TCC #50	W	0
17	I49	Interrupt associated with TCC #49	W	0
16	I48	Interrupt associated with TCC #48	W	0
15	I47	Interrupt associated with TCC #47	W	0
14	I46	Interrupt associated with TCC #46	W	0
13	I45	Interrupt associated with TCC #45	W	0
12	I44	Interrupt associated with TCC #44	W	0
11	I43	Interrupt associated with TCC #43	W	0
10	I42	Interrupt associated with TCC #42	W	0
9	I41	Interrupt associated with TCC #41	W	0
8	I40	Interrupt associated with TCC #40	W	0
7	I39	Interrupt associated with TCC #39	W	0
6	I38	Interrupt associated with TCC #38	W	0
5	I37	Interrupt associated with TCC #37	W	0
4	I36	Interrupt associated with TCC #36	W	0
3	I35	Interrupt associated with TCC #35	W	0
2	I34	Interrupt associated with TCC #34	W	0
1	I33	Interrupt associated with TCC #33	W	0
0	I32	Interrupt associated with TCC #32	W	0

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Table 5-291. Register Call Summary for Register TPCC_ICRH_RN_k

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- TPCC Register Summary: [0]

Table 5-292. TPCC_IEVAL_RN_k

Address Offset	0x0000 2078 + (0x200 * k)		
Physical Address	0x01C0 2078 + (0x200 * k)	**Instance**	TPCC
Description	Interrupt Eval Register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SET	EVAL

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	write 0's for future compatibility	W	0x0000 0000
1	SET	Interrupt Set: CPU write of 1 to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable (IERn) and status (IPRn). CPU write of 0 has no effect.	W	0
0	EVAL	Interrupt Evaluate: CPU write of 1 to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts (IERn) are still pending (IPRn). CPU write of 0 has no effect..	W	0

Table 5-293. Register Call Summary for Register TPCC_IEVAL_RN_k

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- TPCC Register Summary: [0]

Table 5-294. TPCC_QER_RN_k

Address Offset	0x0000 2080 + (0x200 * k)		
Physical Address	0x01C0 2080 + (0x200 * k)	**Instance**	TPCC
Description	QDMA Event Register: If TPCC_QER[n] En bit is set, then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TPCC_QER[n] En bit is set when a vbus write byte matches the address defined in the TPCC_QCHMAPN_j register. TPCC_QER[n] En bit is cleared when the corresponding event is prioritized and serviced. TPCC_QER[n] En is also cleared when user writes a 1 to the TPCC_QSECR[n] En bit. If the TPCC_QER[n] En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and TPCC_QEER register is set, then the corresponding bit in the QDMA Event Missed Register is set.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	reads return 0's	R	0x000000
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0

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Bits	Field Name	Description	Type	Reset
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-295. Register Call Summary for Register TPCC_QER_RN_k

DSP Subsystem Functional Description • DMA Versus QDMA: [0]
DSP Subsystem Register Manual • TPCC Register Summary: [1]

Table 5-296. TPCC_QEER_RN_k

Address Offset	0x0000 2084 + (0x200 * k)		
Physical Address	0x01C0 2084 + (0x200 * k)	**Instance**	TPCC
Description	QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. TPCC_QEER[n] En is not directly writeable. QDMA channels can be enabled via writes to TPCC_QEESR and can be disabled via writes to TPCC_QEECR register. TPCC_QEER[n] En = 1, The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in TPCC_QER[n] En. TPCC_QEER[n] En = 0, The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in TPCC_QER[n] En.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	reads return 0's	R	0x000000
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-297. Register Call Summary for Register TPCC_QEER_RN_k

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Table 5-298. TPCC_QEECR_RN_k

Address Offset	0x0000 2088 + (0x200 * k)
Physical Address	0x01C0 2088 + (0x200 * k) **Instance** TPCC
Description	QDMA Event Enable Clear Register: CPU write of 1 to the TPCC_QEECR[n] En bit causes the TPCC_QEER[n] En bit to be cleared. CPU write of 0 has no effect..
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	write 0's for future compatibility	W	0x000000
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-299. Register Call Summary for Register TPCC_QEECR_RN_k

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- TPCC Register Summary: [0]

Table 5-300. TPCC_QEESR_RN_k

Address Offset	0x0000 208C + (0x200 * k)
Physical Address	0x01C0 208C + (0x200 * k) **Instance** TPCC
Description	QDMA Event Enable Set Register: CPU write of 1 to the TPCC_QEESR[n] En bit causes the TPCC_QEESR[n] En bit to be set. CPU write of 0 has no effect..
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	write 0's for future compatibility	W	0x000000
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

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Table 5-301. Register Call Summary for Register TPCC_QEESR_RN_k

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- TPCC Register Summary: [0]

Table 5-302. TPCC_QSER_RN_k

Address Offset	0x0000 2090 + (0x200 * k)		
Physical Address	0x01C0 2090 + (0x200 * k)	**Instance**	TPCC
Description	QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (TPCC_QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	reads return 0's	R	0x000000
7	E7	Event #7	R	0
6	E6	Event #6	R	0
5	E5	Event #5	R	0
4	E4	Event #4	R	0
3	E3	Event #3	R	0
2	E2	Event #2	R	0
1	E1	Event #1	R	0
0	E0	Event #0	R	0

Table 5-303. Register Call Summary for Register TPCC_QSER_RN_k

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- TPCC Register Summary: [0]

Table 5-304. TPCC_QSECR_RN_k

Address Offset	0x0000 2094 + (0x200 * k)		
Physical Address	0x01C0 2094 + (0x200 * k)	**Instance**	TPCC
Description	QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the TPCC_QSER and TPCC_QER register (note that this is slightly different than the TPCC_SER operation, which does not clear the TPCC_ER[n] En register). CPU write of 1 to the TPCC_QSECR[n] En bit clears the TPCC_QSER[n] En and TPCC_QER[n] En register fields. CPU write of 0 has no effect..		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								E7	E6	E5	E4	E3	E2	E1	E0

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	write 0's for future compatibility	W	0x000000
7	E7	Event #7	W	0
6	E6	Event #6	W	0
5	E5	Event #5	W	0
4	E4	Event #4	W	0
3	E3	Event #3	W	0
2	E2	Event #2	W	0
1	E1	Event #1	W	0
0	E0	Event #0	W	0

Table 5-305. Register Call Summary for Register TPCC_QSECR_RN_k

DSP Subsystem Register Manual

- TPCC Register Summary: [0]

Table 5-306. TPCC_OPT_m

Address Offset	0x0000 4000 + (0x20 * m)		
Physical Address	0x01C0 4000 + (0x20 * m)	**Instance**	TPCC
Description	Options Parameter		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIV	RESERVED	RESERVED		PRIVID				ITCCHEN	TCCHEN	ITCINTEN	TCINTEN	WIMODE	RESERVED	TCC						TCCMODE	FWID			RESERVED				STATIC	SYNCDIM	DAM	SAM

Bits	Field Name	Description	Type	Reset
31	PRIV	Privilege level: privilege level (supervisor vs. user) for the host/cpu/dma that programmed this PaRAM Entry. Value is set with the vbus priv value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus. 0 : User level privilege 1 : Supervisor level privilege	R	-
30	RESERVED	Reserved	R	0
29:28	RESERVED	write 0's for future compatibility reads return 0's	RW	0bxx
27:24	PRIVID	Privilege ID: Privilege ID for the external host/cpu/dma that programmed this PaRAM Entry. This value is set with the vbus privid value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus.	R	0x-
23	ITCCHEN	Intermediate transfer completion chaining enable: 0: disabled 1: enabled.	RW	-
22	TCCHEN	Transfer complete chaining enable: 0: disabled 1: enabled.	RW	-
21	ITCINTEN	Intermediate transfer completion interrupt enable: 0: disabled. 1: enabled (corresponding TPCC_IER bit must be set to 1 to generate interrupt)	RW	-

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Bits	Field Name	Description	Type	Reset
20	TCINTEN	Transfer complete interrupt enable: 0: disabled. 1: enabled (corresponding TPCC_IER bit must be set to 1 to generate interrupt)	RW	-
19	WIMODE	Backward compatibility mode: 0: Normal operation 1 : WI Backwards Compatibility mode, forces BCNT to be adjusted by 1 upon TR submission (0 means 1, 1 means 2, ...) and forces ACNT to be treated as a word-count (left shifted by 2 by hardware to create byte cnt for TR submission)	RW	-
18	RESERVED	write 0's for future compatibility reads return 0's	RW	-
17:12	TCC	Transfer Complete Code: The 6-bit code is used to set the relevant bit in TPCC_CER for chaining or in TPCC_IER for interrupts.	RW	0bxxxxxx
11	TCCMODE	Transfer complete code mode: Indicates the point at which a transfer is considered completed. Applies to both chaining and interrupt. 0: Normal Completion, A transfer is considered completed after the transfer parameters are returned to the CC from the TC (which was returned from the peripheral). 1: Early Completion, A transfer is considered completed after the CC submits a TR to the TC. CC generates completion code internally .	RW	-
10:8	FWID	FIFO width: Applies if either SAM or DAM is set to FIFO mode. Pass-thru to TC. 0x0: FIFO width is 8-bit 0x1: FIFO width is 16-bit 0x2: FIFO width is 32-bit 0x3: FIFO width is 64-bit 0x4: FIFO width is 128-bit 0x5: FIFO width is 256-bit	RW	0bxxx
7:4	RESERVED	write 0's for future compatibility reads return 0's	RW	0x-
3	STATIC	Static Entry: 0: Entry is updated as normal 1: Entry is static, Count and Address updates are not updated after TRP is submitted. Linking is not performed.	RW	-
2	SYNCDIM	Transfer Synchronization Dimension: 0: A-Sync, Each event triggers the transfer of ACNT elements. 1: AB-Sync, Each event triggers the transfer of BCNT arrays of ACNT elements	RW	-
1	DAM	Destination Address Mode: Destination Address Mode within an array. Pass-thru to TC. 0: INCR, Dst addressing within an array increments. Dst is not a FIFO. 1: FIFO, Dst addressing within an array wraps around upon reaching FIFO width.	RW	-
0	SAM	Source Address Mode: Source Address Mode within an array. Pass-thru to TC. 0: INCR, Src addressing within an array increments. Source is not a FIFO. 1: FIFO, Src addressing within an array wraps around upon reaching FIFO width.	RW	-

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Table 5-307. Register Call Summary for Register TPCC_OPT_m

DSP Subsystem Functional Description • Transfer Completion: [0]
DSP Subsystem Programming Guide • Kelvin DMA Compatibility Mode: [1]
DSP Subsystem Register Manual • TPCC Register Summary: [2]

Table 5-308. TPCC_SRC_m

Address Offset	0x0000 4004 + (0x20 * m)		
Physical Address	0x01C0 4004 + (0x20 * m)	**Instance**	TPCC
Description	Source Address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC																															

Bits	Field Name	Description	Type	Reset
31:0	SRC	Source Address: The 32-bit source address parameters specify the starting byte address of the source . If SAM is set to FIFO mode then the user should program the Source address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.	RW	0x--------

Table 5-309. Register Call Summary for Register TPCC_SRC_m

DSP Subsystem Register Manual • TPCC Register Summary: [0]

Table 5-310. TPCC_ABCNT_m

Address Offset	0x0000 4008 + (0x20 * m)		
Physical Address	0x01C0 4008 + (0x20 * m)	**Instance**	TPCC
Description	A and B byte count		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCNT																ACNT															

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Bits	Field Name	Description	Type	Reset
31:16	BCNT	Count for 2nd Dimension: BCNT is a 16-bit unsigned value that specifies the number of arrays of length ACNT. For normal operation, valid values for BCNT can be anywhere between 1 and 65535. Therefore, the maximum number of arrays in a frame is 65535 (64K-1 arrays). BCNT=1 means 1 array in the frame, and BCNT=0 means 0 arrays in the frame. In normal mode, a BCNT of 0 is considered as either a Null or Dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set, then the programmed BCNT value will be incremented by 1 before submission to TC. that is, 0 means 1, 1 means 2, 2 means 3, ..., 0xFFFE means 0xFFFF. A value of 0xFFFF is an illegal value that will be treated as a Null TR.	RW	0x----
15:0	ACNT	number of bytes in 1st dimension: ACNT represents the number of bytes within the first dimension of a transfer. ACNT is a 16-bit unsigned value with valid values between 0 and 65535. Therefore, the maximum number of bytes in an array is 65535 bytes (64K-1 bytes). ACNT must be greater than or equal to 1 for a TR to be submitted to TC. An ACNT of 0 is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the ACNT field represents a word count. The CC must internally multiply by 4 to translate the word count to a byte count prior to submission to the TC. The 2 MSBs of the 16-bit ACNT are reserved and should always be written as 'b00 by the user. If user writes a value other than 0, it will still be treated as 0 since the multiply-by-4 operation (to translate between a word count and a byte count) will drop the 2 msbits. For dummy and null transfer definition, the ACNT definition will disregard the 2 msbits. that is, a programmed ACNT value of 0x8000 in WI-mode will be treated as 0 byte transfer, resulting in null or dummy operation dependent on the state of BCNT and CCNT.	RW	0x----

Table 5-311. Register Call Summary for Register TPCC_ABCNT_m

DSP Subsystem Register Manual

- TPCC Register Summary: [0]

Table 5-312. TPCC_DST_m

Address Offset	0x0000 400C + (0x20 * m)		
Physical Address	0x01C0 400C + (0x20 * m)	**Instance**	TPCC
Description	Destination Address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST																															

Bits	Field Name	Description	Type	Reset
31:0	DST	Destination Address: The 32-bit destination address parameters specify the starting byte address of the destination. If DAM is set to FIFO mode then the user should program the Destination address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.	RW	0x--------

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Table 5-313. Register Call Summary for Register TPCC_DST_m

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-314. TPCC_BIDX_m

Address Offset	0x0000 4010 + (0x20 * m)		
Physical Address	0x01C0 4010 + (0x20 * m)	**Instance**	TPCC
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBIDX																SBIDX															

Bits	Field Name	Description	Type	Reset
31:16	DBIDX	Destination 2nd Dimension Index: DBIDX is a 16-bit signed value (2's complement) used for destination address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the destination array to the beginning of the next destination array within the current frame. It applies to both A-Sync and AB-Sync transfers.	RW	0x----
15:0	SBIDX	Source 2nd Dimension Index: SBIDX is a 16-bit signed value (2's complement) used for source address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the source array to the beginning of the next source array. It applies to both A-sync and AB-sync transfers.	RW	0x----

Table 5-315. Register Call Summary for Register TPCC_BIDX_m

DSP Subsystem Functional Description
- Types of TPCC Transfers: [0]

DSP Subsystem Register Manual
- TPCC Register Summary: [1]

Table 5-316. TPCC_LNK_m

Address Offset	0x0000 4014 + (0x20 * m)		
Physical Address	0x01C0 4014 + (0x20 * m)	**Instance**	TPCC
Description	Link and Reload parameters		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCNTRLD																LINK															

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Bits	Field Name	Description	Type	Reset
31:16	BCNTRLD	BCNT Reload: BCNTRLD is a 16-bit unsigned value used to reload the BCNT field once the last array in the 2nd dimension is transferred. This field is only used for A-Sync'ed transfers. In this case, the CC decrements the BCNT value by one on each TR submission. When BCNT (conceptually) reaches zero, then the CC decrements CCNT and uses the BCNTRLD value to reinitialize the BCNT value. For AB-synchronized transfers, the CC submits the BCNT in the TR and therefore the TC is responsible to keep track of BCNT, not thus BCNTRLD is a don't care field.	RW	0x----
15:0	LINK	Link Address: The CC provides a mechanism to reload the current PaRAM Entry upon its natural termination (that is, after count fields are decremented to 0) with a new PaRAM Entry. This is called 'linking'. The 16-bit parameter LINK specifies the byte address offset in the PaRAM from which the CC loads/reloads the next PaRAM entry in the link. The CC should disregard the value in the upper 2 bits of the LINK field as well as the lower 5-bits of the LINK field. The upper two bits are ignored such that the user can program either the 'literal' byte address of the LINK parameter or the 'PaRAM base-relative' address of the link field. Therefore, if the user uses the literal address with a range from 0x4000 to 0x7FFF, it will be treated as a PaRAM-base-relative value of 0x0000 to 0x3FFF. The lower-5 bits are ignored and treated as 'b00000, thereby guaranteeing that all Link pointers point to a 32-byte aligned PaRAM entry. In the latter case (5-lsbs), behavior is undefined for the user (that is, don't have to test it). In the former case (2 msbs), user should be able to take advantage of this feature (that is, do have to test it). If a Link Update is requested to a PaRAM address that is beyond the actual range of implemented PaRAM, then the Link will be treated as a Null Linkand all 0s plus 0xFFFF will be written to the current entry location. A LINK value of 0xFFFF is referred to as a NULL link which should cause the CC to write 0x0 to all entries of the current PaRAM Entry except for the LINK field which is set to 0xFFFF. The Priv/Privid state is overwritten to 0x0 when linking. MSBs and LSBS should not be masked when comparing against the 0xFFFF value. that is, a value of 0x3FFE is a non-NULL PaRAM link field.	RW	0x----

Table 5-317. Register Call Summary for Register TPCC_LNK_m

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-318. TPCC_CIDX_m

Address Offset	0x0000 4018 + (0x20 * m)		
Physical Address	0x01C0 4018 + (0x20 * m)	**Instance**	TPCC
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCIDX																SCIDX															

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Bits	Field Name	Description	Type	Reset
31:16	DCIDX	Destination Frame Index: DCIDX is a 16-bit signed value (2's complement) used for destination address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array (pointed to by DST address) to the beginning of the first destination array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when DCIDX is applied, the current array in an A-sync transfer is the last array in the frame, while the current array in a ABsync transfer is the first array in the frame.	RW	0x----
15:0	SCIDX	Source Frame Index: SCIDX is a 16-bit signed value (2's complement) used for source address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array (pointed to by SRC address) to the beginning of the first source array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when SCIDX is applied, the current array in an A-sync transfer is the last array in the frame, while the current array in a AB-sync transfer is the first array in the frame.	RW	0x----

Table 5-319. Register Call Summary for Register TPCC_CIDX_m

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

Table 5-320. TPCC_CCNT_m

Address Offset	0x0000 401C + (0x20 * m)		
Physical Address	0x01C0 401C + (0x20 * m)	**Instance**	TPCC
Description	C byte count		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CCNT															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	write 0's for future compatibility reads return 0's	RW	0x----
15:0	CCNT	Count for 3rd Dimension: CCNT is a 16-bit unsigned value that specifies the number of frames in a block. Valid values for CCNT can be anywhere between 1 and 65535. Therefore, the maximum number of frames in a block is 65535 (64K-1 frames). CCNT of 1 means 1 frame in the block, and CCNT of 0 means 0 frames in the block. A CCNT value of 0 is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. WIMODE has no affect on CCNT operation.	RW	0x----

Table 5-321. Register Call Summary for Register TPCC_CCNT_m

DSP Subsystem Register Manual
- TPCC Register Summary: [0]

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5.5.7 TPTC Registers

5.5.7.1 TPTC Register Summary

Table 5-322. TPTC Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TPTC0 Physical Address	TPTC1 Physical Address
TPTC_TCSTAT	R	32	0x0000 0100	0x01C1 0100	0x01C1 0500
TPTC_INTSTAT	R	32	0x0000 0104	0x01C1 0104	0x01C1 0504
TPTC_INTEN	RW	32	0x0000 0108	0x01C1 0108	0x01C1 0508
TPTC_INTCLR	W	32	0x0000 010C	0x01C1 010C	0x01C1 050C
TPTC_INTCMD	W	32	0x0000 0110	0x01C1 0110	0x01C1 0510
TPTC_ERRSTAT	R	32	0x0000 0120	0x01C1 0120	0x01C1 0520
TPTC_ERREN	RW	32	0x0000 0124	0x01C1 0124	0x01C1 0524
TPTC_ERRCLR	W	32	0x0000 0128	0x01C1 0128	0x01C1 0528
TPTC_ERRDET	R	32	0x0000 012C	0x01C1 012C	0x01C1 052C
TPTC_ERRCMD	W	32	0x0000 0130	0x01C1 0130	0x01C1 0530
TPTC_RDRATE	RW	32	0x0000 0140	0x01C1 0140	0x01C1 0540
TPTC_POPT	RW	32	0x0000 0200	0x01C1 0200	0x01C1 0600
TPTC_PSRC	RW	32	0x0000 0204	0x01C1 0204	0x01C1 0604
TPTC_PCNT	RW	32	0x0000 0208	0x01C1 0208	0x01C1 0608
TPTC_PDST	RW	32	0x0000 020C	0x01C1 020C	0x01C1 060C
TPTC_PBIDX	RW	32	0x0000 0210	0x01C1 0210	0x01C1 0610
TPTC_PMPPRXY	R	32	0x0000 0214	0x01C1 0214	0x01C1 0614
TPTC_SAOPT	R	32	0x0000 0240	0x01C1 0240	0x01C1 0640
TPTC_SASRC	R	32	0x0000 0244	0x01C1 0244	0x01C1 0644
TPTC_SACNT	R	32	0x0000 0248	0x01C1 0248	0x01C1 0648
TPTC_SADST	R	32	0x0000 024C	0x01C1 024C	0x01C1 064C
TPTC_SABIDX	R	32	0x0000 0250	0x01C1 0250	0x01C1 0650
TPTC_SAMPPRXY	R	32	0x0000 0254	0x01C1 0254	0x01C1 0654
TPTC_SACNTRLD	R	32	0x0000 0258	0x01C1 0258	0x01C1 0658
TPTC_SASRCBREF	R	32	0x0000 025C	0x01C1 025C	0x01C1 065C
TPTC_SADSTBREF	R	32	0x0000 0260	0x01C1 0260	0x01C1 0660
TPTC_DFCNTRLD	R	32	0x0000 0280	0x01C1 0280	0x01C1 0680
TPTC_DFSRCBREF	R	32	0x0000 0284	0x01C1 0284	0x01C1 0684
TPTC_DFDSTBREF	R	32	0x0000 0288	0x01C1 0288	0x01C1 0688

5.5.7.2 TPTC Register Description

Table 5-323. TPTC_TCSTAT

Address Offset	0x0000 0100		
Physical Address	0x01C1 0100 0x01C1 0500	**Instance**	TPTC0 TPTC1
Description	TC Status Register		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		DFSTRTPTR		RESERVED			ACTV	RESERVED	DSTACTV			RESERVED	WSACTV	SRCACTV	PROGBUSY

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	reads return 0's	R	0x00000
13:12	DFSTRTPTR	Dst FIFO Start Pointer Represents the offset to the head entry of Dst Register FIFO, in units of *entries*. Legal values = 0x0 to 0x3	R	0x0
11:9	RESERVED	reads return 0's	R	0x0
8	ACTV	Channel Active Channel Active is a logical-OR of each of the *BUSY/ACTV signals. The ACTV bit must remain high through the life of a TR. 0 : Channel is idle. 1 : Channel is busy.	R	1
7	RESERVED	reads return 0's	R	0
6:4	DSTACTV	Destination Active State Specifies the number of TRs that are resident in the Dst Register FIFO at a given instant. Legal values are constrained by the DSTREGDEPTH parameter. Read 0x0: FIFO set is empty. Read 0x1: Dst FIFO contains 1 TR Read 0x2: Dst FIFO contains 2 TR Read 0x3: Dst FIFO contains 3 TR Read 0x4: Dst FIFO contains 4 TR	R	0x0
3	RESERVED	reads return 0's	R	0
2	WSACTV	Write Status Active 0 : Write status is not pending. Write status has been received for all previously issued write commands. 1 : Write Status is pending. Write status has not been received for all previously issued write commands.	R	0
1	SRCACTV	Source Active State 0 : Source Active set is idle. Any TR written to Prog Set will immediately transition to Source Active set as long as the Dst FIFO Set is not full (DSTFULL == 1). 1 : Source Active set is busy either performing read transfers or waiting to perform read transfers for current Transfer Request.	R	0
0	PROGBUSY	Program Register Set Busy 0 : Prog set idle and is available for programming. 1 : Prog set busy. User should poll for PROGBUSY equal to 0 prior to re-programming the Program Register set.	R	0

Table 5-324. Register Call Summary for Register TPTC_TCSTAT

DSP Subsystem Functional Description
- Tracking Transfers: [0]

DSP Subsystem Register Manual
- TPTC Register Summary: [1]

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Table 5-325. TPTC_INTSTAT

Address Offset	0x0000 0104		
Physical Address	0x01C1 0104 0x01C1 0504	**Instance**	TPTC0 TPTC1
Description	Interrupt Status Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TRDONE	PROGEMPTY
R-0																														R-0	R-0

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	reads return 0's	R	0x0000 0000
1	TRDONE	TR Done Event Status: 0 : Condition not detected. 1 : Set when TC has completed a Transfer Request. TRDONE should be set when the write status is returned for the final write of a TR. Cleared when write 1	R	0
0	PROGEMPTY	Program Set Empty Event Status: PROGEMPTY = 0 : Condition not detected. PROGEMPTY = 1 : Set when Program Register set transitions to empty state. Cleared when write 1	R	0

Table 5-326. Register Call Summary for Register TPTC_INTSTAT

DSP Subsystem Functional Description
- Completion Interface to TPCC: [0] [1] [2]

DSP Subsystem Programming Guide
- Error Reporting for DSP DMA: [3]

DSP Subsystem Register Manual
- TPTC Register Summary: [4]
- TPTC Register Description: [5]

Table 5-327. TPTC_INTEN

Address Offset	0x0000 0108		
Physical Address	0x01C1 0108 0x01C1 0508	**Instance**	TPTC0 TPTC1
Description	Interrupt Enable Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TRDONE	PROGEMPTY
R-0																														R-0	R-0

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0000 0000
1	TRDONE	TR Done Event Enable: 0 : disabled. 1 : enabled, and contributes to interrupt generation	RW	0
0	PROGEMPTY	Program Set Empty Event Enable: 0 : PROGEMPTY Event is disabled. 1 : PROGEMPTY Event is enabled, and contributes to interrupt generation	RW	0

Table 5-328. Register Call Summary for Register TPTC_INTEN

DSP Subsystem Functional Description
- Completion Interface to TPCC: [0]

DSP Subsystem Register Manual
- TPTC Register Summary: [1]

Table 5-329. TPTC_INTCLR

Address Offset	0x0000 010C		
Physical Address	0x01C1 010C 0x01C1 050C	**Instance**	TPTC0 TPTC1
Description	Interrupt Clear Register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TRDONE	PROGEMPTY

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	write 0's for future compatibility	W	0x0000 0000
1	TRDONE	TR Done Event Clear: 0 : no effect. 1 : clears TRDONE bit	W	0
0	PROGEMPTY	Program Set Empty Event Clear: 0 : no effect. 1 : clears PROGEMPTY bit	W	0

Table 5-330. Register Call Summary for Register TPTC_INTCLR

DSP Subsystem Programming Guide
- Error Reporting for DSP DMA: [0]

DSP Subsystem Register Manual
- TPTC Register Summary: [1]

Table 5-331. TPTC_INTCMD

Address Offset	0x0000 0110		
Physical Address	0x01C1 0110 0x01C1 0510	**Instance**	TPTC0 TPTC1
Description	Interrupt Command Register		
Type	W		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SET	EVAL

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	write 0's for future compatibility	W	0x0000 0000
1	SET	Set TPTC interrupt: Write 1: causes TPTC interrupt to be pulsed unconditionally. Write 0: no affect.	W	0
0	EVAL	Evaluate state of TPTC interrupt Write 1 causes TPTC interrupt to be pulsed if any of the TPTC_INTSTAT bits are set to 1. Write 0: no affect.	W	0

Table 5-332. Register Call Summary for Register TPTC_INTCMD

DSP Subsystem Register Manual
- TPTC Register Summary: [0]

Table 5-333. TPTC_ERRSTAT

Address Offset	0x0000 0120		
Physical Address	0x01C1 0120 0x01C1 0520	**Instance**	TPTC0 TPTC1
Description	Error Status Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MMRAERR	TRERR	RESERVED	BUSERR

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	reads return 0's	R	0x0000000
3	MMRAERR	MMR Address Error: 0 : Condition not detected. 1 : User attempted to read or write to invalid address configuration memory map. No additional error information is recorded.	R	0
2	TRERR	TR Error: TR detected that violates FIFO Mode transfer (SAM or DAM is 1) alignment rules or has ACNT or BCNT == 0. No additional error information is recorded.	R	0
1	RESERVED	reads return 0's	R	0
0	BUSERR	Bus Error Event: 0: Condition not detected. 1: TC has detected an error code on the write response bus or read response bus. Error information is stored in Error Details Register (TPTC_ERRDET).	R	0

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Table 5-334. Register Call Summary for Register TPTC_ERRSTAT

DSP Subsystem Programming Guide
- Error Reporting for DSP DMA: [0] [1] [2] [3] [4] [5]

DSP Subsystem Register Manual
- TPTC Register Summary: [6]
- TPTC Register Description: [7]

Table 5-335. TPTC_ERREN

Address Offset	0x0000 0124		
Physical Address	0x01C1 0124 0x01C1 0524	**Instance**	TPTC0 TPTC1
Description	Error Enable Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MMRAERR	TRERR	RESERVED	BUSERR

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	write 0's for future compatibility reads return 0's	R	0x0000000
3	MMRAERR	Interrupt enable MMRAERR: 0: disabled. 1: enabled, and contributes to the TPTC error interrupt generation.	RW	0
2	TRERR	Interrupt enable for TRERR: 0: disabled. 1: enabled, and contributes to the TPTC error interrupt generation.	RW	0
1	RESERVED	write 0's for future compatibility reads return 0's	RW	0
0	BUSERR	Interrupt enable for BUSERR: 0: disabled. 1: enabled, and contributes to the TPTC error interrupt generation.	RW	0

Table 5-336. Register Call Summary for Register TPTC_ERREN

DSP Subsystem Programming Guide
- Error Reporting for DSP DMA: [0]

DSP Subsystem Register Manual
- TPTC Register Summary: [1]

Table 5-337. TPTC_ERRCLR

Address Offset	0x0000 0128		
Physical Address	0x01C1 0128 0x01C1 0528	**Instance**	TPTC0 TPTC1
Description	Error Clear Register		
Type	W		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MMRAERR	TRERR	RESERVED	BUSERR

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	write 0's for future compatibility	W	0x0000000
3	MMRAERR	Interrupt clear for MMRAERR: Write 0 : no effect. Write 1: clears MMRAERR bit. This does not clear the TPTC_ERRDET register.	W	0
2	TRERR	Interrupt clear for TRERR: Writes 0: no effect. Write of 1: clears TRERR bit. This does not clear the ERRDET register.	W	0
1	RESERVED	write 0's for future compatibility	W	0
0	BUSERR	Interrupt clear for BUSERR: Writes 0: no effect. Write 1: clears BUSERR bit. This does not clear the ERRDET register.	W	0

Table 5-338. Register Call Summary for Register TPTC_ERRCLR

DSP Subsystem Programming Guide
- Error Reporting for DSP DMA: [0] [1]

DSP Subsystem Register Manual
- TPTC Register Summary: [2]

Table 5-339. TPTC_ERRDET

Address Offset	0x0000 012C		
Physical Address	0x01C1 012C 0x01C1 052C	**Instance**	TPTC0 TPTC1
Description	Error Details Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TCCHEN	TCINTEN	RESERVED				TCC				RESERVED				STAT			

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	reads return 0's	R	0x0000
17	TCCHEN	Contains the OPT.TCCHEN value programmed by the user for the Read or Write transaction that resulted in an error.	R	0
16	TCINTEN	Contains the OPT.TCINTEN value programmed by the user for the Read or Write transaction that resulted in an error.	R	0
15:14	RESERVED	reads return 0's	R	0x0
13:8	TCC	Transfer Complete Code: Contains the OPT.TCC value programmed by the user for the Read or Write transaction that resulted in an error.	R	0x00
7:4	RESERVED	reads return 0's	R	0x0

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Bits	Field Name	Description	Type	Reset
3:0	STAT	Transaction Status: Stores the non-zero status/error code that was detected on the read status or write status bus. MS-bit effectively serves as the read vs. write error code. If read status and write status are returned on the same cycle, then the TC chooses non-zero version. If both are non-zero then write status is treated as higher priority. Read 0x0: No Error (should not cause error to be latched) Read 0x1: Read Addressing error Read 0x2: Read Privilege error Read 0x3: Read Timeout error Read 0x4: Read Data error Read 0x7: Read Exclusive-operation failure Read 0x8: No Error (should not cause error to be latched) Read 0x9: Write Addressing error Read 0xA: Write Privilege error Read 0xB: Write Timeout error Read 0xC: Write Data error Read 0xF: Write Exclusive-operation failure	R	0x0

Table 5-340. Register Call Summary for Register TPTC_ERRDET

DSP Subsystem Programming Guide
- Error Reporting for DSP DMA: [0] [1] [2] [3] [4]

DSP Subsystem Register Manual
- TPTC Register Summary: [5]
- TPTC Register Description: [6] [7]

Table 5-341. TPTC_ERRCMD

Address Offset	0x0000 0130		
Physical Address	0x01C1 0130 0x01C1 0530	**Instance**	TPTC0 TPTC1
Description	Error Command Register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SET	EVAL

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	write 0's for future compatibility	W	0x0000 0000
1	SET	Set TPTC error interrupt: Write 1: cause TPTC error interrupt to be pulsed unconditionally. Write 0: no affect.	W	0
0	EVAL	Evaluate state of TPTC error interrupt Write 1: cause TPTC error interrupt to be pulsed if any of the TPTC_ERRSTAT bits are set to 1. Write 0: no affect.	W	0

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Table 5-342. Register Call Summary for Register TPTC_ERRCMD

DSP Subsystem Register Manual

- TPTC Register Summary: [0]

Table 5-343. TPTC_RDRATE

Address Offset	0x0000 0140		
Physical Address	0x01C1 0140 0x01C1 0540	**Instance**	TPTC0 TPTC1
Description	Read Rate Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														RDRATE	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0000 0000
2:0	RDRATE	Read Rate Control: Controls the number of cycles between read commands. This is a global setting that applies to all TRs for this TC. 0x0: Reads issued as fast as possible. 0x1: 4 cycles between reads 0x2: 8 cycles between reads 0x3: 16 cycles between reads 0x4: 32 cycles between reads	RW	0x0

Table 5-344. Register Call Summary for Register TPTC_RDRATE

DSP Subsystem Register Manual

- TPTC Register Summary: [0]

Table 5-345. TPTC_POPT

Address Offset	0x0000 0200		
Physical Address	0x01C1 0200 0x01C1 0600	**Instance**	TPTC0 TPTC1
Description	Prog Set Options		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TCCHEN	RESERVED	TCINTEN	RESERVED					TCC				RESERVED	FWID			RESERVED	PRI			RESERVED		DAM	SAM

Bits	Field Name	Description	Type	Reset
31:23	RESERVED	write 0's for future compatibility reads return 0's	RW	0x000
22	TCCHEN	Transfer complete chaining enable: 0: disabled. 1: enabled.	RW	0
21	RESERVED	write 0's for future compatibility reads return 0's	RW	0
20	TCINTEN	Transfer complete interrupt enable: 0: disabled. 1: enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
19:18	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
17:12	TCC	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.	RW	0x00
11	RESERVED	write 0's for future compatibility reads return 0's	RW	0
10:8	FWID	FIFO width control: Applies if either SAM or DAM is set to FIFO mode. 0x0: FIFO width is 8-bit 0x1: FIFO width is 16-bit 0x2: FIFO width is 32-bit 0x3: FIFO width is 64-bit 0x4: FIFO width is 128-bit 0x5: FIFO width is 256-bit	RW	0x0
7	RESERVED	write 0's for future compatibility reads return 0's	RW	0
6:4	PRI	Transfer Priority: 0x0: Priority 0 - Highest priority 0x1: Priority 1 0x2: Priority 2 0x3: Priority 3 0x4: Priority 4 0x5: Priority 5 0x6: Priority 6 0x7: Priority 7 - Lowest Priority	RW	0x0
3:2	RESERVED	write 0's for future compatibility reads return 0's	RW	0x0
1	DAM	Destination Address Mode within an array: 0: INCR, Dst addressing within an array increments. 1: FIFO, Dst addressing within an array wraps around upon reaching FIFO width.	RW	0
0	SAM	Source Address Mode within an array: 0: INCR, Src addressing within an array increments. 1: FIFO, Src addressing within an array wraps around upon reaching FIFO width.	RW	0

Table 5-346. Register Call Summary for Register TPTC_POPT

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-347. TPTC_PSRC

Address Offset	0x0000 0204		
Physical Address	0x01C1 0204 0x01C1 0604	**Instance**	TPTC0 TPTC1
Description	Prog Set Src Address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR																															

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Bits	Field Name	Description	Type	Reset
31:0	SADDR	Source address for Program Register Set	RW	0x0000 0000

Table 5-348. Register Call Summary for Register TPTC_PSRC

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-349. TPTC_PCNT

Address Offset	0x0000 0208		
Physical Address	0x01C1 0208 0x01C1 0608	**Instance**	TPTC0 TPTC1
Description	Prog Set Count		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCNT																ACNT															

Bits	Field Name	Description	Type	Reset
31:16	BCNT	B-Dimension count. Number of arrays to be transferred, where each array is ACNT in length.	RW	0x0000
15:0	ACNT	A-Dimension count. Number of bytes to be transferred in first dimension.	RW	0x0000

Table 5-350. Register Call Summary for Register TPTC_PCNT

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-351. TPTC_PDST

Address Offset	0x0000 020C		
Physical Address	0x01C1 020C 0x01C1 060C	**Instance**	TPTC0 TPTC1
Description	Prog Set Dst Address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR																															

Bits	Field Name	Description	Type	Reset
31:0	DADDR	Destination address for Program Register Set	RW	0x0000 0000

Table 5-352. Register Call Summary for Register TPTC_PDST

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

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Table 5-353. TPTC_PBIDX

Address Offset	0x0000 0210		
Physical Address	0x01C1 0210 0x01C1 0610	**Instance**	TPTC0 TPTC1
Description	Prog Set B-Dim Idx		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBIDX																SBIDX															

Bits	Field Name	Description	Type	Reset
31:16	DBIDX	B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array (recall that there are BCNT arrays of ACNT elements). DBIDX is always used, regardless of whether DAM is Increment or FIFO mode.	RW	0x0000
15:0	SBIDX	B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array (recall that there are BCNT arrays of ACNT elements). SBIDX is always used, regardless of whether SAM is Increment or FIFO mode.	RW	0x0000

Table 5-354. Register Call Summary for Register TPTC_PBIDX

DSP Subsystem Functional Description

- Tracking Transfers: [0]

DSP Subsystem Register Manual

- TPTC Register Summary: [1]

Table 5-355. TPTC_PMPPRXY

Address Offset	0x0000 0214		
Physical Address	0x01C1 0214 0x01C1 0614	**Instance**	TPTC0 TPTC1
Description	Prog Set Mem Protect Proxy		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						RESERVED	PRIV	RESERVED				PRIVID			

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED	reads return 0's	R	0x000000
9	RESERVED	Reserved	R	0
8	PRIV	Privilege Level: 0 : User level privilege 1 : Supervisor level privilege PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register (trigger register). The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.	R	0
7:4	RESERVED	reads return 0's	R	0x0
3:0	PRIVID	Privilege ID: PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register (trigger register). The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.	R	0x0

Table 5-356. Register Call Summary for Register TPTC_PMPPRXY

DSP Subsystem Functional Description
- Tracking Transfers: [0]

DSP Subsystem Register Manual
- TPTC Register Summary: [1]

Table 5-357. TPTC_SAOPT

Address Offset	0x0000 0240		
Physical Address	0x01C1 0240 0x01C1 0640	**Instance**	TPTC0 TPTC1
Description	Src Actv Set Options		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TCCHEN	RESERVED	TCINTEN	RESERVED				TCC				RESERVED		FWID		RESERVED		PRI			RESERVED		DAM	SAM

Bits	Field Name	Description	Type	Reset
31:23	RESERVED	reads return 0's	R	0x000
22	TCCHEN	Transfer complete chaining enable: 0: disabled. 1: enabled.	R	0
21	RESERVED	reads return 0's	R	0
20	TCINTEN	Transfer complete interrupt enable: 0: disabled. 1: enabled.	R	0
19:18	RESERVED	reads return 0's	R	0x0

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Bits	Field Name	Description	Type	Reset
17:12	TCC	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.	R	0x00
11	RESERVED	reads return 0's	R	0
10:8	FWID	FIFO width control: Applies if either SAM or DAM is set to FIFO mode. Read 0x0: FIFO width is 8-bit Read 0x1: FIFO width is 16-bit Read 0x2: FIFO width is 32-bit Read 0x3: FIFO width is 64-bit Read 0x4: FIFO width is 128-bit Read 0x5: FIFO width is 256-bit	R	0x0
7	RESERVED	reads return 0's	R	0
6:4	PRI	Transfer Priority: Read 0x0: Priority 0 - Highest priority Read 0x1: Priority 1 Read 0x2: Priority 2 Read 0x3: Priority 3 Read 0x4: Priority 4 Read 0x5: Priority 5 Read 0x6: Priority 6 Read 0x7: Priority 7 - Lowest Priority	R	0x0
3:2	RESERVED	reads return 0's	R	0x0
1	DAM	Destination Address Mode within an array: 0: INCR, Dst addressing within an array increments. 1: FIFO, Dst addressing within an array wraps around upon reaching FIFO width.	R	0
0	SAM	Source Address Mode within an array: 0: INCR, Src addressing within an array increments. 1: FIFO, Src addressing within an array wraps around upon reaching FIFO width.	R	0

Table 5-358. Register Call Summary for Register TPTC_SAOPT

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-359. TPTC_SASRC

Address Offset	0x0000 0244		
Physical Address	0x01C1 0244 0x01C1 0644	**Instance**	TPTC0 TPTC1
Description	Src Actv Set Src Address		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR																															

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Bits	Field Name	Description	Type	Reset
31:0	SADDR	Source address for Source Active Register Set: Initial value is copied from PSRC.SADDR. TC updates value according to source addressing mode (OPT.SAM) and/or source index value (BIDX.SBIDX) after each read command is issued. When a TR is complete, the final value should be the address of the last read command issued.	R	0x0000 0000

Table 5-360. Register Call Summary for Register TPTC_SASRC

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-361. TPTC_SACNT

Address Offset	0x0000 0248		
Physical Address	0x01C1 0248 0x01C1 0648	**Instance**	TPTC0 TPTC1
Description	Src Actv Set Count		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCNT																ACNT															

Bits	Field Name	Description	Type	Reset
31:16	BCNT	B-Dimension count: Number of arrays to be transferred, where each array is ACNT in length. Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete.	R	0x0000
15:0	ACNT	A-Dimension count: Number of bytes to be transferred in first dimension. Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete.	R	0x0000

Table 5-362. Register Call Summary for Register TPTC_SACNT

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-363. TPTC_SADST

Address Offset	0x0000 024C		
Physical Address	0x01C1 024C 0x01C1 064C	**Instance**	TPTC0 TPTC1
Description	return 0x0 w/o AERROR		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR																															

Bits	Field Name	Description	Type	Reset
31:0	DADDR	Destination address is not applicable for Src Active Register Set. Reads return 0x0	R	0x0000 0000

Table 5-364. Register Call Summary for Register TPTC_SADST

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-365. TPTC_SABIDX

Address Offset	0x0000 0250		
Physical Address	0x01C1 0250 0x01C1 0650	**Instance**	TPTC0 TPTC1
Description	Src Actv Set B-Dim Idx		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBIDX																SBIDX															

Bits	Field Name	Description	Type	Reset
31:16	DBIDX	Dest B-Idx for Source Active Register Set Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array (recall that there are BCNT arrays of ACNT elements). DBIDX is always used, regardless of whether DAM is Increment or FIFO mode.	R	0x0000
15:0	SBIDX	Source B-Idx for Source Active Register Set Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array (recall that there are BCNT arrays of ACNT elements). SBIDX is always used, regardless of whether SAM is Increment or FIFO mode.	R	0x0000

Table 5-366. Register Call Summary for Register TPTC_SABIDX

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-367. TPTC_SAMPPRXY

Address Offset	0x0000 0254		
Physical Address	0x01C1 0254 0x01C1 0654	**Instance**	TPTC0 TPTC1
Description	Src Actv Set Mem Protect Proxy		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						RESERVED	PRIV	RESERVED				PRIVID			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	reads return 0's	R	0x000000
9	RESERVED	Reserved	R	0
8	PRIV	Privilege Level: 0 : User level privilege 1 : Supervisor level privilege PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register (trigger register). The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.	R	0
7:4	RESERVED	reads return 0's	R	0x0
3:0	PRIVID	Privilege ID: PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register (trigger register). The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.	R	0x0

Table 5-368. Register Call Summary for Register TPTC_SAMPPRXY

DSP Subsystem Functional Description

- Tracking Transfers: [0]

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- TPTC Register Summary: [1]

Table 5-369. TPTC_SACNTRLD

Address Offset	0x0000 0258		
Physical Address	0x01C1 0258 0x01C1 0658	**Instance**	TPTC0 TPTC1
Description	Src Actv Set Cnt Reload		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ACNTRLD															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	reads return 0's	R	0x0000
15:0	ACNTRLD	A-Cnt Reload value for Source Active Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT. The Reload value is used to reinitialize ACNT after each array is serviced (that is, ACNT decrements to 0). by the Src offset in bytes between the starting address of each source array (recall that there are BCNT arrays of ACNT bytes)	R	0x0000

Table 5-370. Register Call Summary for Register TPTC_SACNTRLD

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-371. TPTC_SASRCBREF

Address Offset	0x0000 025C		
Physical Address	0x01C1 025C 0x01C1 065C	**Instance**	TPTC0 TPTC1
Description	Src Actv Set Src Addr A-Reference		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF																															

Bits	Field Name	Description	Type	Reset
31:0	SADDRBREF	Source address reference for Source Active Register Set: Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.	R	0x0000 0000

Table 5-372. Register Call Summary for Register TPTC_SASRCBREF

DSP Subsystem Functional Description • Tracking Transfers: [0]
DSP Subsystem Register Manual • TPTC Register Summary: [1]

Table 5-373. TPTC_SADSTBREF

Address Offset	0x0000 0260		
Physical Address	0x01C1 0260 0x01C1 0660	**Instance**	TPTC0 TPTC1
Description	return 0x0 w/o AERROR		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDRBREF																															

Bits	Field Name	Description	Type	Reset
31:0	DADDRBREF	Dst address reference is not applicable for Src Active Register Set. Reads return 0x0.	R	0x0000 0000

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Table 5-374. Register Call Summary for Register TPTC_SADSTBREF

DSP Subsystem Functional Description
- Tracking Transfers: [0]

DSP Subsystem Register Manual
- TPTC Register Summary: [1]

Table 5-375. TPTC_DFCNTRLD

Address Offset	0x0000 0280		
Physical Address	0x01C1 0280 0x01C1 0680	**Instance**	TPTC0 TPTC1
Description	Dst FIFO Set Cnt Reload		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ACNTRLD															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	reads return 0's	R	0x0000
15:0	ACNTRLD	A-Cnt Reload value for Destination FIFO Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT. The Reload value is used to reinitialize ACNT after each array is serviced (that is, ACNT decrements to 0). by the Src offset in bytes between the starting address of each source array (recall that there are BCNT arrays of ACNT bytes)	R	0x0000

Table 5-376. Register Call Summary for Register TPTC_DFCNTRLD

DSP Subsystem Register Manual
- TPTC Register Summary: [0]

Table 5-377. TPTC_DFSRCBREF

Address Offset	0x0000 0284		
Physical Address	0x01C1 0284 0x01C1 0684	**Instance**	TPTC0 TPTC1
Description	return 0x0 w/o AERROR		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDRBREF																															

Bits	Field Name	Description	Type	Reset
31:0	SADDRBREF	Source address reference is not applicable for Dst FIFO Register Set. Reads return 0x0.	R	0x0000 0000

Table 5-378. Register Call Summary for Register TPTC_DFSRCBREF

DSP Subsystem Register Manual
- TPTC Register Summary: [0]

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Table 5-379. TPTC_DFDSTBREF

Address Offset	0x0000 0288		
Physical Address	0x01C1 0288 0x01C1 0688	**Instance**	TPTC0 TPTC1
Description	Dst FIFO Set Dst Addr A-Reference		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDRBREF																															

Bits	Field Name	Description	Type	Reset
31:0	DADDRBREF	Destination address reference for Dst FIFO Register Set: Represents the starting address for the array currently being written. The next array's starting address is calculated as the 'reference address' plus the 'dest bidx' value.	R	0x0000 0000

Table 5-380. Register Call Summary for Register TPTC_DFDSTBREF

DSP Subsystem Register Manual

- TPTC Register Summary: [0]

5.5.8 SYSC Registers

5.5.8.1 SYSC Register Summary

Table 5-381. SYSC Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSC Physical Address
SYSC_REVISION	R	32	0x0000 0000	0x01C2 0000
SYSC_SYSCONFIG	RW	32	0x0000 0008	0x01C2 0008
SYSC_BUSERR	RW	32	0x0000 0010	0x01C2 0010
SYSC_VBUSM2OCP	RW	32	0x0000 0040	0x01C2 0040
SYSC_EDMA	RW	32	0x0000 0048	0x01C2 0048
SYSC_CORE	RW	32	0x0000 004C	0x01C2 004C
SYSC_DSP_ICTRL	RW	32	0x0000 0050	0x01C2 0050
SYSC_BOOTADDR	R	32	0x0000 0100	0x01C2 0100
SYSC_IDLEDLY	RW	32	0x0000 0F08	0x01C2 0F08

5.5.8.2 SYSC Register Description

Table 5-382. SYSC_REVISION

Address Offset	0x0000 0000		
Physical Address	0x01C2 0000	**Instance**	SYSC
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

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Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	0x- TI internal data

Table 5-383. Register Call Summary for Register SYSC_REVISION

DSP Subsystem Register Manual
- SYSC Register Summary: [0]

Table 5-384. SYSC_SYSCONFIG

Address Offset	0x0000 0008		
Physical Address	0x01C2 0008	**Instance**	SYSC
Description	This register allows controlling various parameters of the SYSC module		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved. write 0's for future compatibility reads return 0's	RW	0x0000 0000
0	AUTOIDLE	Internal auto-clock gating strategy 0: Clock is free running 1: Automatic clock gating strategy is applied	RW	1

Table 5-385. Register Call Summary for Register SYSC_SYSCONFIG

DSP Subsystem Programming Guide
- Clock Gating: [0] [1]

DSP Subsystem Register Manual
- SYSC Register Summary: [2]

Table 5-386. SYSC_BUSERR

Address Offset	0x0000 0010		
Physical Address	0x01C2 0010	**Instance**	SYSC
Description	store bus error information		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DISCERRL3	DISCERRABE	RESERVED	DISCERRCFG

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved.	R	0x0000000
3	DISCERRL3	OCP Disconnect Bus Error status of L3	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	DISCERRABE	OCP Disconnect Bus Error status of ABE	RW W1toClr	0
1	RESERVED		R	0
0	DISCERRCFG	OCP Disconnect Bus Error status of CFG	RW W1toClr	0

Table 5-387. Register Call Summary for Register SYSC_BUSERR

DSP Subsystem Register Manual
- SYSC Register Summary: [0]

Table 5-388. SYSC_VBUSM2OCP

Address Offset	0x0000 0040		
Physical Address	0x01C2 0040	**Instance**	SYSC
Description	This register controls the VBUSM2OCP bridge.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							MAXBURSTSIZE	RESERVED							RESERVED	RESERVED						RESERVED	DMA_WNPEN	WFCTIMEOUT				RESERVED		PAGEXINGEN	RESERVED

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved	R	0x00
24	MAXBURSTSIZE	V2O burst maximum size 1: Burst maximum size is unknown. 0: Burst maximum size is 8.	RW	0
23:17	RESERVED	Reserved	R	0x00
16:15	RESERVED	Reserved	RW	0
14:10	RESERVED	Reserved	R	0x00
9	RESERVED	Reserved	RW	0
8	DMA_WNPEN	DMA write nonposted enable 0: DMA write access is write posted only. 1: Enable convert write access to write nonposted.	RW	0
7:4	WFCTIMEOUT	VBUSM2OCP burst closing timeout: The value drives the number of cycles the bridge waits without any new requests coming in before it automatically closes a burst.	RW	0xF
3:2	RESERVED	Reserved.	R	0x0
1	PAGEXINGEN	MMU page crossing enable: 0: Bursts are not allowed to cross 4kB page boundaries 1: Bursts are allowed to cross 4kB page boundaries	RW	0
0	RESERVED	Reserved.	R	0

Table 5-389. Register Call Summary for Register SYSC_VBUSM2OCP

DSP Subsystem Functional Description
- Interconnect Optimization: [0]

DSP Subsystem Programming Guide
- DSP DMA Completion Mode: [1]

DSP Subsystem Register Manual
- SYSC Register Summary: [2]

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Table 5-390. SYSC_EDMA

Address Offset	0x0000 0048		
Physical Address	0x01C2 0048	**Instance**	SYSC
Description	This register allows controlling various parameters of the SCRM and SCRP local interconnects		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											EDMA_CLK_AUTOGATING			EDMA_CLKEN_CTRL	EDMA_CLKEN	RESERVED												APINTERVAL				

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved.	R	0x000
20:18	EDMA_CLK_AUTOGATING	DMA_DSP clock autogating 0x0: DMA_DSP root clock is not autogated by hardware. 0x1: DMA_DSP root clock is autogated by hardware. [18] is for TPCC (no actual clock gating, same as IVA2.2). 19] is for TPTC0. [20] is for TPTC1.	RW	0x0
17	EDMA_CLKEN_CTRL	DMA_DSP clock control enable 0x0: DMA_DSP clock is controlled by hardware. 0x1: DMA_DSP clock is controlled by SYSC_EDMA [16] EDMA_CLKEN.	RW	0
16	EDMA_CLKEN	DMA_DSP clock enable When SYSC_EDMA_CTRL[17] EDMA_CLKEN_CTRL = 1, then: 0x0: DMA_DSP clock is disabled. 0x1: DMA_DSP clock is enabled. EDMA_CLKEN is for TPCC, TPTC0, and TPTC1.	RW	0
15:5	RESERVED	Reserved.	R	0x000
4:0	APINTERVAL	Control of the Aged Priority (priority inversion) for DMA accesses: When set to 0x0, the aged priority is disabled when set to another value. This controls how often the priority is adjusted: every APInterval cycle, the priority of the port is decreased until the associated request is accepted or the priority of the port equals 0. The priority of the port is reinitialized to the transaction priority each time a new VBUS command is generated, that is, the last one has been accepted. 0x0: Aged Priority Disabled: There is no aged priority in SCR. DMA transaction keeps the fixed priority defined internally, and has to wait for the bus to be freed by higher priority initiatorsAged Priority Disabled:	RW	0x00

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Table 5-391. Register Call Summary for Register SYSC_EDMA

DSP Subsystem Programming Guide • Aged Priority: [0] [1]
DSP Subsystem Register Manual • SYSC Register Summary: [2] • SYSC Register Description: [3]

Table 5-392. SYSC_CORE

Address Offset	0x0000 004C		
Physical Address	0x01C2 004C	**Instance**	SYSC
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												INT_CLKENCTRL	INT_CLKEN	RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved.	R	0x0000000
3	INT_CLKENCTRL	DSP core local clock-gating control 0x0: DSP core root clock is controlled by hardware. 0x1: DSP core root clock is controlled by SYSC_CORE[2] INT_CLKEN.	RW	0
2	INT_CLKEN	DSP core local clock gate enabled When SYSC_CORE[3] INT_CLKENCTRL = 1, then: 0x0: DSP core clock is disabled. 0x1: DSP core clock is enabled.	RW	0
1:0	RESERVED	Reserved.	R	0x0

Table 5-393. Register Call Summary for Register SYSC_CORE

DSP Subsystem Register Manual • SYSC Register Summary: [0] • SYSC Register Description: [1] [2]

Table 5-394. SYSC_DSP_ICTRL

Address Offset	0x0000 0050		
Physical Address	0x01C2 0050	**Instance**	SYSC
Description	This register allows controlling local to DSP subsystem clock gating		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DMACGDIS	GEMCGDIS	RESERVED			LOCALCG

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved.	R	0x0000000
5	DMACGDIS	DMA local clock gating disable bit (only applicable when LOCALCG=1): 0: DMA clock can be stopped locally 1: DMA clock can not be stopped locally	RW	0
4	GEMCGDIS	GEM local clock gating disable bit (only applicable when LOCALCG=1): 0: GEM clock can be stopped locally 1: GEM clock can not be stopped locally	RW	0
3:1	RESERVED	Reserved.	R	0x0
0	LOCALCG	Internal auto-clock gating strategy 0: Global DSP power management (DMA and GEM clocks are not stopped independently but very low power state can be reached) 1: Local DSP power management (DMA and GEM clocks can be stopped independently but very low power state cannot be reached)	RW	0

Table 5-395. Register Call Summary for Register SYSC_DSP_ICTRL

DSP Subsystem Register Manual
- SYSC Register Summary: [0]

Table 5-396. SYSC_BOOTADDR

Address Offset	0x0000 0100		
Physical Address	0x01C2 0100	**Instance**	SYSC
Description	This register defines the physical address of the DSP boot loader. This is a copy of the CONTROL_DSP_BOOTADDR when the DSP is released from reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTLOADADDR																						RESERVED									

Bits	Field Name	Description	Type	Reset
31:10	BOOTLOADADDR	Physical address of the DSP boot loader: This is the read-only copy of the CONTROL_DSP_BOOTADDR when the DSP is released from reset.	R	0x20000
9:0	RESERVED	Reads return 0s.	R	0x000

Table 5-397. Register Call Summary for Register SYSC_BOOTADDR

DSP Subsystem Functional Description
- Boot Configuration: [0] [1]

DSP Subsystem Programming Guide
- DSP Boot: [2]

DSP Subsystem Register Manual
- SYSC Register Summary: [3]

Table 5-398. SYSC_IDLEDLY

Address Offset	0x0000 0F08		
Physical Address	0x01C2 0F08	**Instance**	SYSC
Description	configurable idle delay counter		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								IDLEDELAYCNT							RESERVED

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved.	R	0x0000000
6:1	IDLEDELAYCNT	Idle Delay Counter	RW	0x10
0	RESERVED	Reserved.	R	0

Table 5-399. Register Call Summary for Register SYSC_IDLEDLY

DSP Subsystem Register Manual
- SYSC Register Summary: [0]

5.5.9 WUGEN_DSP Registers

5.5.9.1 WUGEN_DSP Register Summary

Table 5-400. WUGEN_DSP Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	WUGEN_DSP Physical Address
WUGEN_REVISION	R	32	0x0000 0000	0x01C2 1000
WUGEN_SYSCONFIG	RW	32	0x0000 0008	0x01C2 1008
WUGEN_MEVT0	R	32	0x0000 0060	0x01C2 1060
WUGEN_MEVT1	R	32	0x0000 0064	0x01C2 1064
WUGEN_MEVT2	R	32	0x0000 0068	0x01C2 1068
WUGEN_MEVT3	R	32	0x0000 006C	0x01C2 106C
WUGEN_MEVT4	R	32	0x0000 0070	0x01C2 1070
WUGEN_MEVTCLR0	W	32	0x0000 0074	0x01C2 1074
WUGEN_MEVTCLR1	W	32	0x0000 0078	0x01C2 1078
WUGEN_MEVTCLR2	W	32	0x0000 007C	0x01C2 107C
WUGEN_MEVTCLR3	W	32	0x0000 0080	0x01C2 1080
WUGEN_MEVTCLR4	W	32	0x0000 0084	0x01C2 1084
WUGEN_MEVTSET0	W	32	0x0000 0088	0x01C2 1088
WUGEN_MEVTSET1	W	32	0x0000 008C	0x01C2 108C
WUGEN_MEVTSET2	W	32	0x0000 0090	0x01C2 1090
WUGEN_MEVTSET3	W	32	0x0000 0094	0x01C2 1094
WUGEN_MEVTSET4	W	32	0x0000 0098	0x01C2 1098
WUGEN_PENDEVT0	R	32	0x0000 009C	0x01C2 109C
WUGEN_PENDEVT1	R	32	0x0000 00A0	0x01C2 10A0
WUGEN_PENDEVT2	R	32	0x0000 00A4	0x01C2 10A4
WUGEN_PENDEVT3	R	32	0x0000 00A8	0x01C2 10A8
WUGEN_PENDEVT4	R	32	0x0000 00AC	0x01C2 10AC
WUGEN_PENDEVTCLR0	W	32	0x0000 00B0	0x01C2 10B0
WUGEN_PENDEVTCLR1	W	32	0x0000 00B4	0x01C2 10B4
WUGEN_PENDEVTCLR2	W	32	0x0000 00B8	0x01C2 10B8
WUGEN_PENDEVTCLR3	W	32	0x0000 00BC	0x01C2 10BC
WUGEN_PENDEVTCLR4	W	32	0x0000 00C0	0x01C2 10C0

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5.5.9.2 WUGEN_DSP Register Description

Table 5-401. WUGEN_REVISION

Address Offset	0x0000 0000		
Physical Address	0x01C2 1000	**Instance**	WUGEN_DSP
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	0x- TI internal data

Table 5-402. Register Call Summary for Register WUGEN_REVISION

DSP Subsystem Register Manual
- WUGEN_DSP Register Summary: [0]

Table 5-403. WUGEN_SYSCONFIG

Address Offset	0x0000 0008		
Physical Address	0x01C2 1008	**Instance**	WUGEN_DSP
Description	This register allows controlling various parameters of the WUGEN_DSP module		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	reserved write 0's for future compatibility reads return 0's	RW	0x0000 0000
0	AUTOIDLE	Internal auto-clock gating strategy 0: Clock is free running 1: Automatic clock gating strategy is applied	RW	1

Table 5-404. Register Call Summary for Register WUGEN_SYSCONFIG

DSP Subsystem Programming Guide
- Clock Gating: [0] [1]

DSP Subsystem Register Manual
- WUGEN_DSP Register Summary: [2]

Table 5-405. WUGEN_MEVT0

Address Offset	0x0000 0060		
Physical Address	0x01C2 1060	**Instance**	WUGEN_DSP
Description	This register contains the interrupt mask (LSB)		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQ31	MIRQ30	MIRQ29	MIRQ28	MIRQ27	MIRQ26	MIRQ25	MIRQ24	MIRQ23	MIRQ22	MIRQ21	MIRQ20	MIRQ19	MIRQ18	MIRQ17	MIRQ16	MIRQ15	MIRQ14	MIRQ13	MIRQ12	MIRQ11	MIRQ10	MIRQ9	MIRQ8	MIRQ7	MIRQ6	MIRQ5	MIRQ4	MIRQ3	MIRQ2	MIRQ1	MIRQ0

Bits	Field Name	Description	Type	Reset
31	MIRQ31	Interrupt Mask bit #31	R	1
30	MIRQ30	Interrupt Mask bit #30	R	1
29	MIRQ29	Interrupt Mask bit #29	R	1
28	MIRQ28	Interrupt Mask bit #28	R	1
27	MIRQ27	Interrupt Mask bit #27	R	1
26	MIRQ26	Interrupt Mask bit #26	R	1
25	MIRQ25	Interrupt Mask bit #25	R	1
24	MIRQ24	Interrupt Mask bit #24	R	1
23	MIRQ23	Interrupt Mask bit #23	R	1
22	MIRQ22	Interrupt Mask bit #22	R	1
21	MIRQ21	Interrupt Mask bit #21	R	1
20	MIRQ20	Interrupt Mask bit #20	R	1
19	MIRQ19	Interrupt Mask bit #19	R	1
18	MIRQ18	Interrupt Mask bit #18	R	1
17	MIRQ17	Interrupt Mask bit #17	R	1
16	MIRQ16	Interrupt Mask bit #16	R	1
15	MIRQ15	Interrupt Mask bit #15	R	1
14	MIRQ14	Interrupt Mask bit #14	R	1
13	MIRQ13	Interrupt Mask bit #13	R	1
12	MIRQ12	Interrupt Mask bit #12	R	1
11	MIRQ11	Interrupt Mask bit #11	R	1
10	MIRQ10	Interrupt Mask bit #10	R	1
9	MIRQ9	Interrupt Mask bit #9	R	1
8	MIRQ8	Interrupt Mask bit #8	R	1
7	MIRQ7	Interrupt Mask bit #7	R	1
6	MIRQ6	Interrupt Mask bit #6	R	1
5	MIRQ5	Interrupt Mask bit #5	R	1
4	MIRQ4	Interrupt Mask bit #4	R	1
3	MIRQ3	Interrupt Mask bit #3	R	1
2	MIRQ2	Interrupt Mask bit #2	R	1
1	MIRQ1	Interrupt Mask bit #1	R	1
0	MIRQ0	Interrupt Mask bit #0	R	1

Table 5-406. Register Call Summary for Register WUGEN_MEVT0

DSP Subsystem Functional Description
- Interrupts, DMA Requests, and Event Management: [0]
- Individual Event Masking: [1]

DSP Subsystem Programming Guide
- INTC Basic Programming Model for Low-Power State of DSP Subsystem: [2]
- INTC Basic Programming Model for Power On of DSP Subsystem: [3] [4] [5]

DSP Subsystem Register Manual
- WUGEN_DSP Register Summary: [6]
- WUGEN_DSP Register Description: [7] [8]

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Table 5-407. WUGEN_MEVT1

Address Offset	0x0000 0064		
Physical Address	0x01C2 1064	**Instance**	WUGEN_DSP
Description	This register contains the interrupt mask (MSB)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQ63	MIRQ62	MIRQ61	MIRQ60	MIRQ59	MIRQ58	MIRQ57	MIRQ56	MIRQ55	MIRQ54	MIRQ53	MIRQ52	MIRQ51	MIRQ50	MIRQ49	MIRQ48	MIRQ47	MIRQ46	MIRQ45	MIRQ44	MIRQ43	MIRQ42	MIRQ41	MIRQ40	MIRQ39	MIRQ38	MIRQ37	MIRQ36	MIRQ35	MIRQ34	MIRQ33	MIRQ32

Bits	Field Name	Description	Type	Reset
31	MIRQ63	Interrupt Mask bit #63	R	1
30	MIRQ62	Interrupt Mask bit #62	R	1
29	MIRQ61	Interrupt Mask bit #61	R	1
28	MIRQ60	Interrupt Mask bit #60	R	1
27	MIRQ59	Interrupt Mask bit #59	R	1
26	MIRQ58	Interrupt Mask bit #58	R	1
25	MIRQ57	Interrupt Mask bit #57	R	1
24	MIRQ56	Interrupt Mask bit #56	R	1
23	MIRQ55	Interrupt Mask bit #55	R	1
22	MIRQ54	Interrupt Mask bit #54	R	1
21	MIRQ53	Interrupt Mask bit #53	R	1
20	MIRQ52	Interrupt Mask bit #52	R	1
19	MIRQ51	Interrupt Mask bit #51	R	1
18	MIRQ50	Interrupt Mask bit #50	R	1
17	MIRQ49	Interrupt Mask bit #49	R	1
16	MIRQ48	Interrupt Mask bit #48	R	1
15	MIRQ47	Interrupt Mask bit #47	R	1
14	MIRQ46	Interrupt Mask bit #46	R	1
13	MIRQ45	Interrupt Mask bit #45	R	1
12	MIRQ44	Interrupt Mask bit #44	R	1
11	MIRQ43	Interrupt Mask bit #43	R	1
10	MIRQ42	Interrupt Mask bit #42	R	1
9	MIRQ41	Interrupt Mask bit #41	R	1
8	MIRQ40	Interrupt Mask bit #40	R	1
7	MIRQ39	Interrupt Mask bit #39	R	1
6	MIRQ38	Interrupt Mask bit #38	R	1
5	MIRQ37	Interrupt Mask bit #37	R	1
4	MIRQ36	Interrupt Mask bit #36	R	1
3	MIRQ35	Interrupt Mask bit #35	R	1
2	MIRQ34	Interrupt Mask bit #34	R	1
1	MIRQ33	Interrupt Mask bit #33	R	1
0	MIRQ32	Interrupt Mask bit #32	R	1

Table 5-408. Register Call Summary for Register WUGEN_MEVT1

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- INTC Basic Programming Model for Low-Power State of DSP Subsystem: [0]
- INTC Basic Programming Model for Power On of DSP Subsystem: [1] [2] [3]

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Table 5-408. Register Call Summary for Register WUGEN_MEVT1 (continued)

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- WUGEN_DSP Register Summary: [4]
- WUGEN_DSP Register Description: [5] [6] [7] [8]

Table 5-409. WUGEN_MEVT2

Address Offset	0x0000 0068		
Physical Address	0x01C2 1068	**Instance**	WUGEN_DSP
Description	This register contains the interrupt mask (MSB)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MIRQ78	MIRQ77	MIRQ76	MIRQ75	MIRQ74	MIRQ73	MIRQ72	MIRQ71	MIRQ70	MIRQ69	MIRQ68	MIRQ67	MIRQ66	MIRQ65	MIRQ64	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved.	R	0x00000
14	MIRQ78	Interrupt Mask bit #78	R	1
13	MIRQ77	Interrupt Mask bit #77	R	1
12	MIRQ76	Interrupt Mask bit #76	R	1
11	MIRQ75	Interrupt Mask bit #75	R	1
10	MIRQ74	Interrupt Mask bit #74	R	1
9	MIRQ73	Interrupt Mask bit #73	R	1
8	MIRQ72	Interrupt Mask bit #72	R	1
7	MIRQ71	Interrupt Mask bit #71	R	1
6	MIRQ70	Interrupt Mask bit #70	R	1
5	MIRQ69	Interrupt Mask bit #69	R	1
4	MIRQ68	Interrupt Mask bit #68	R	1
3	MIRQ67	Interrupt Mask bit #67	R	1
2	MIRQ66	Interrupt Mask bit #66	R	1
1	MIRQ65	Interrupt Mask bit #65	R	1
0	MIRQ64	Interrupt Mask bit #64	R	1

Table 5-410. Register Call Summary for Register WUGEN_MEVT2

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- WUGEN_DSP Register Summary: [0]
- WUGEN_DSP Register Description: [1] [2] [3] [4]

Table 5-411. WUGEN_MEVT3

Address Offset	0x0000 006C		
Physical Address	0x01C2 106C	**Instance**	WUGEN_DSP
Description	This register contains the dma request mask		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDMARQ31	MDMARQ30	MDMARQ29	MDMARQ28	MDMARQ27	MDMARQ26	MDMARQ25	MDMARQ24	MDMARQ23	MDMARQ22	MDMARQ21	MDMARQ20	MDMARQ19	MDMARQ18	MDMARQ17	MDMARQ16	MDMARQ15	MDMARQ14	MDMARQ13	MDMARQ12	MDMARQ11	MDMARQ10	MDMARQ9	MDMARQ8	MDMARQ7	MDMARQ6	MDMARQ5	MDMARQ4	MDMARQ3	MDMARQ2	MDMARQ1	MDMARQ0

Bits	Field Name	Description	Type	Reset
31	MDMARQ31	DMA request Mask bit #31	R	1
30	MDMARQ30	DMA request Mask bit #30	R	1
29	MDMARQ29	DMA request Mask bit #29	R	1
28	MDMARQ28	DMA request Mask bit #28	R	1
27	MDMARQ27	DMA request Mask bit #27	R	1
26	MDMARQ26	DMA request Mask bit #26	R	1
25	MDMARQ25	DMA request Mask bit #25	R	1
24	MDMARQ24	DMA request Mask bit #24	R	1
23	MDMARQ23	DMA request Mask bit #23	R	1
22	MDMARQ22	DMA request Mask bit #22	R	1
21	MDMARQ21	DMA request Mask bit #21	R	1
20	MDMARQ20	DMA request Mask bit #20	R	1
19	MDMARQ19	DMA request Mask bit #19	R	1
18	MDMARQ18	DMA request Mask bit #18	R	1
17	MDMARQ17	DMA request Mask bit #17	R	1
16	MDMARQ16	DMA request Mask bit #16	R	1
15	MDMARQ15	DMA request Mask bit #15	R	1
14	MDMARQ14	DMA request Mask bit #14	R	1
13	MDMARQ13	DMA request Mask bit #13	R	1
12	MDMARQ12	DMA request Mask bit #12	R	1
11	MDMARQ11	DMA request Mask bit #11	R	1
10	MDMARQ10	DMA request Mask bit #10	R	1
9	MDMARQ9	DMA request Mask bit #9	R	1
8	MDMARQ8	DMA request Mask bit #8	R	1
7	MDMARQ7	DMA request Mask bit #7	R	1
6	MDMARQ6	DMA request Mask bit #6	R	1
5	MDMARQ5	DMA request Mask bit #5	R	1
4	MDMARQ4	DMA request Mask bit #4	R	1
3	MDMARQ3	DMA request Mask bit #3	R	1
2	MDMARQ2	DMA request Mask bit #2	R	1
1	MDMARQ1	DMA request Mask bit #1	R	1
0	MDMARQ0	DMA request Mask bit #0	R	1

Table 5-412. Register Call Summary for Register WUGEN_MEVT3

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- WUGEN_DSP Register Summary: [0]

Table 5-413. WUGEN_MEVT4

Address Offset	0x0000 0070		
Physical Address	0x01C2 1070	**Instance**	WUGEN_DSP
Description	This register contains the dma request mask		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MDMARQ58	MDMARQ57	MDMARQ56	MDMARQ55	MDMARQ54	MDMARQ53	MDMARQ52	MDMARQ51	MDMARQ50	MDMARQ49	MDMARQ48	MDMARQ47	MDMARQ46	MDMARQ45	MDMARQ44	MDMARQ43	MDMARQ42	MDMARQ41	MDMARQ40	MDMARQ39	MDMARQ38	MDMARQ37	MDMARQ36	MDMARQ35	MDMARQ34	MDMARQ33	MDMARQ32	

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved.	R	0x00
26	MDMARQ58	DMA request Mask bit #58	R	1
25	MDMARQ57	DMA request Mask bit #57	R	1
24	MDMARQ56	DMA request Mask bit #56	R	1
23	MDMARQ55	DMA request Mask bit #55	R	1
22	MDMARQ54	DMA request Mask bit #54	R	1
21	MDMARQ53	DMA request Mask bit #53	R	1
20	MDMARQ52	DMA request Mask bit #52	R	1
19	MDMARQ51	DMA request Mask bit #51	R	1
18	MDMARQ50	DMA request Mask bit #50	R	1
17	MDMARQ49	DMA request Mask bit #49	R	1
16	MDMARQ48	DMA request Mask bit #48	R	1
15	MDMARQ47	DMA request Mask bit #47	R	1
14	MDMARQ46	DMA request Mask bit #46	R	1
13	MDMARQ45	DMA request Mask bit #45	R	1
12	MDMARQ44	DMA request Mask bit #44	R	1
11	MDMARQ43	DMA request Mask bit #43	R	1
10	MDMARQ42	DMA request Mask bit #42	R	1
9	MDMARQ41	DMA request Mask bit #41	R	1
8	MDMARQ40	DMA request Mask bit #40	R	1
7	MDMARQ39	DMA request Mask bit #39	R	1
6	MDMARQ38	DMA request Mask bit #38	R	1
5	MDMARQ37	DMA request Mask bit #37	R	1
4	MDMARQ36	DMA request Mask bit #36	R	1
3	MDMARQ35	DMA request Mask bit #35	R	1
2	MDMARQ34	DMA request Mask bit #34	R	1
1	MDMARQ33	DMA request Mask bit #33	R	1
0	MDMARQ32	DMA request Mask bit #32	R	1

Table 5-414. Register Call Summary for Register WUGEN_MEVT4

DSP Subsystem Functional Description
- Interrupts, DMA Requests, and Event Management: [0]
- Individual Event Masking: [1]

DSP Subsystem Register Manual
- WUGEN_DSP Register Summary: [2]

Table 5-415. WUGEN_MEVTCLR0

Address Offset	0x0000 0074		
Physical Address	0x01C2 1074	**Instance**	WUGEN_DSP
Description	This register is used to clear the interrupt mask bits (LSB) write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_MEVT0 register reads always return 0		
Type	W		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQCLR31	MIRQCLR30	MIRQCLR29	MIRQCLR28	MIRQCLR27	MIRQCLR26	MIRQCLR25	MIRQCLR24	MIRQCLR23	MIRQCLR22	MIRQCLR21	MIRQCLR20	MIRQCLR19	MIRQCLR18	MIRQCLR17	MIRQCLR16	MIRQCLR15	MIRQCLR14	MIRQCLR13	MIRQCLR12	MIRQCLR11	MIRQCLR10	MIRQCLR9	MIRQCLR8	MIRQCLR7	MIRQCLR6	MIRQCLR5	MIRQCLR4	MIRQCLR3	MIRQCLR2	MIRQCLR1	MIRQCLR0

Bits	Field Name	Description	Type	Reset
31	MIRQCLR31	MIRQ clear #31	W W1toSet	0
30	MIRQCLR30	MIRQ clear #30	W W1toSet	0
29	MIRQCLR29	MIRQ clear #29	W W1toSet	0
28	MIRQCLR28	MIRQ clear #28	W W1toSet	0
27	MIRQCLR27	MIRQ clear #27	W W1toSet	0
26	MIRQCLR26	MIRQ clear #26	W W1toSet	0
25	MIRQCLR25	MIRQ clear #25	W W1toSet	0
24	MIRQCLR24	MIRQ clear #24	W W1toSet	0
23	MIRQCLR23	MIRQ clear #23	W W1toSet	0
22	MIRQCLR22	MIRQ clear #22	W W1toSet	0
21	MIRQCLR21	MIRQ clear #21	W W1toSet	0
20	MIRQCLR20	MIRQ clear #20	W W1toSet	0
19	MIRQCLR19	MIRQ clear #19	W W1toSet	0
18	MIRQCLR18	MIRQ clear #18	W W1toSet	0
17	MIRQCLR17	MIRQ clear #17	W W1toSet	0
16	MIRQCLR16	MIRQ clear #16	W W1toSet	0
15	MIRQCLR15	MIRQ clear #15	W W1toSet	0
14	MIRQCLR14	MIRQ clear #14	W W1toSet	0
13	MIRQCLR13	MIRQ clear #13	W W1toSet	0
12	MIRQCLR12	MIRQ clear #12	W W1toSet	0
11	MIRQCLR11	MIRQ clear #11	W W1toSet	0
10	MIRQCLR10	MIRQ clear #10	W W1toSet	0
9	MIRQCLR9	MIRQ clear #9	W W1toSet	0
8	MIRQCLR8	MIRQ clear #8	W W1toSet	0
7	MIRQCLR7	MIRQ clear #7	W W1toSet	0

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Bits	Field Name	Description	Type	Reset
6	MIRQCLR6	MIRQ clear #6	W W1toSet	0
5	MIRQCLR5	MIRQ clear #5	W W1toSet	0
4	MIRQCLR4	MIRQ clear #4	W W1toSet	0
3	MIRQCLR3	MIRQ clear #3	W W1toSet	0
2	MIRQCLR2	MIRQ clear #2	W W1toSet	0
1	MIRQCLR1	MIRQ clear #1	W W1toSet	0
0	MIRQCLR0	MIRQ clear #0	W W1toSet	0

Table 5-416. Register Call Summary for Register WUGEN_MEVTCLR0

DSP Subsystem Functional Description
- Interrupt Requests: [0]
- Interrupts, DMA Requests, and Event Management: [1]
- Individual Event Mask Clear: [2]

DSP Subsystem Register Manual
- WUGEN_DSP Register Summary: [3]

Table 5-417. WUGEN_MEVTCLR1

Address Offset	0x0000 0078		
Physical Address	0x01C2 1078	**Instance**	WUGEN_DSP
Description	This register is used to clear the interrupt mask bits (MSB) write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_MEVT1 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQCLR63	MIRQCLR62	MIRQCLR61	MIRQCLR60	MIRQCLR59	MIRQCLR58	MIRQCLR57	MIRQCLR56	MIRQCLR55	MIRQCLR54	MIRQCLR53	MIRQCLR52	MIRQCLR51	MIRQCLR50	MIRQCLR49	MIRQCLR48	MIRQCLR47	MIRQCLR46	MIRQCLR45	MIRQCLR44	MIRQCLR43	MIRQCLR42	MIRQCLR41	MIRQCLR40	MIRQCLR39	MIRQCLR38	MIRQCLR37	MIRQCLR36	MIRQCLR35	MIRQCLR34	MIRQCLR33	MIRQCLR32

Bits	Field Name	Description	Type	Reset
31	MIRQCLR63	MIRQ clear #63	W W1toSet	0
30	MIRQCLR62	MIRQ clear #62	W W1toSet	0
29	MIRQCLR61	MIRQ clear #61	W W1toSet	0
28	MIRQCLR60	MIRQ clear #60	W W1toSet	0
27	MIRQCLR59	MIRQ clear #59	W W1toSet	0
26	MIRQCLR58	MIRQ clear #58	W W1toSet	0
25	MIRQCLR57	MIRQ clear #57	W W1toSet	0
24	MIRQCLR56	MIRQ clear #56	W W1toSet	0

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Bits	Field Name	Description	Type	Reset
23	MIRQCLR55	MIRQ clear #55	W W1toSet	0
22	MIRQCLR54	MIRQ clear #54	W W1toSet	0
21	MIRQCLR53	MIRQ clear #53	W W1toSet	0
20	MIRQCLR52	MIRQ clear #52	W W1toSet	0
19	MIRQCLR51	MIRQ clear #51	W W1toSet	0
18	MIRQCLR50	MIRQ clear #50	W W1toSet	0
17	MIRQCLR49	MIRQ clear #49	W W1toSet	0
16	MIRQCLR48	MIRQ clear #48	W W1toSet	0
15	MIRQCLR47	MIRQ clear #47	W W1toSet	0
14	MIRQCLR46	MIRQ clear #46	W W1toSet	0
13	MIRQCLR45	MIRQ clear #45	W W1toSet	0
12	MIRQCLR44	MIRQ clear #44	W W1toSet	0
11	MIRQCLR43	MIRQ clear #43	W W1toSet	0
10	MIRQCLR42	MIRQ clear #42	W W1toSet	0
9	MIRQCLR41	MIRQ clear #41	W W1toSet	0
8	MIRQCLR40	MIRQ clear #40	W W1toSet	0
7	MIRQCLR39	MIRQ clear #39	W W1toSet	0
6	MIRQCLR38	MIRQ clear #38	W W1toSet	0
5	MIRQCLR37	MIRQ clear #37	W W1toSet	0
4	MIRQCLR36	MIRQ clear #36	W W1toSet	0
3	MIRQCLR35	MIRQ clear #35	W W1toSet	0
2	MIRQCLR34	MIRQ clear #34	W W1toSet	0
1	MIRQCLR33	MIRQ clear #33	W W1toSet	0
0	MIRQCLR32	MIRQ clear #32	W W1toSet	0

Table 5-418. Register Call Summary for Register WUGEN_MEVTCLR1

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- WUGEN_DSP Register Summary: [0]

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Table 5-419. WUGEN_MEVTCLR2

Address Offset	0x0000 007C		
Physical Address	0x01C2 107C	**Instance**	WUGEN_DSP
Description	This register is used to clear the interrupt mask bits (MSB) write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_MEVT1 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MIRQCLR78	MIRQCLR77	MIRQCLR76	MIRQCLR75	MIRQCLR74	MIRQCLR73	MIRQCLR72	MIRQCLR71	MIRQCLR70	MIRQCLR69	MIRQCLR68	MIRQCLR67	MIRQCLR66	MIRQCLR65	MIRQCLR64		

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved.	R	0x00000
14	MIRQCLR78	MIRQ clear #78	W W1toSet	0
13	MIRQCLR77	MIRQ clear #77	W W1toSet	0
12	MIRQCLR76	MIRQ clear #76	W W1toSet	0
11	MIRQCLR75	MIRQ clear #75	W W1toSet	0
10	MIRQCLR74	MIRQ clear #74	W W1toSet	0
9	MIRQCLR73	MIRQ clear #73	W W1toSet	0
8	MIRQCLR72	MIRQ clear #72	W W1toSet	0
7	MIRQCLR71	MIRQ clear #71	W W1toSet	0
6	MIRQCLR70	MIRQ clear #70	W W1toSet	0
5	MIRQCLR69	MIRQ clear #69	W W1toSet	0
4	MIRQCLR68	MIRQ clear #68	W W1toSet	0
3	MIRQCLR67	MIRQ clear #67	W W1toSet	0
2	MIRQCLR66	MIRQ clear #66	W W1toSet	0
1	MIRQCLR65	MIRQ clear #65	W W1toSet	0
0	MIRQCLR64	MIRQ clear #64	W W1toSet	0

Table 5-420. Register Call Summary for Register WUGEN_MEVTCLR2

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- WUGEN_DSP Register Summary: [0]

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Table 5-421. WUGEN_MEVTCLR3

Address Offset	0x0000 0080		
Physical Address	0x01C2 1080	**Instance**	WUGEN_DSP
Description	This register is used to clear the dma request mask bits write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_MEVT2 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDMARQCLR31	MDMARQCLR30	MDMARQCLR29	MDMARQCLR28	MDMARQCLR27	MDMARQCLR26	MDMARQCLR25	MDMARQCLR24	MDMARQCLR23	MDMARQCLR22	MDMARQCLR21	MDMARQCLR20	MDMARQCLR19	MDMARQCLR18	MDMARQCLR17	MDMARQCLR16	MDMARQCLR15	MDMARQCLR14	MDMARQCLR13	MDMARQCLR12	MDMARQCLR11	MDMARQCLR10	MDMARQCLR9	MDMARQCLR8	MDMARQCLR7	MDMARQCLR6	MDMARQCLR5	MDMARQCLR4	MDMARQCLR3	MDMARQCLR2	MDMARQCLR1	MDMARQCLR0

Bits	Field Name	Description	Type	Reset
31	MDMARQCLR31	MDMARQ clear #31	W W1toSet	0
30	MDMARQCLR30	MDMARQ clear #30	W W1toSet	0
29	MDMARQCLR29	MDMARQ clear #29	W W1toSet	0
28	MDMARQCLR28	MDMARQ clear #28	W W1toSet	0
27	MDMARQCLR27	MDMARQ clear #27	W W1toSet	0
26	MDMARQCLR26	MDMARQ clear #26	W W1toSet	0
25	MDMARQCLR25	MDMARQ clear #25	W W1toSet	0
24	MDMARQCLR24	MDMARQ clear #24	W W1toSet	0
23	MDMARQCLR23	MDMARQ clear #23	W W1toSet	0
22	MDMARQCLR22	MDMARQ clear #22	W W1toSet	0
21	MDMARQCLR21	MDMARQ clear #21	W W1toSet	0
20	MDMARQCLR20	MDMARQ clear #20	W W1toSet	0
19	MDMARQCLR19	MDMARQ clear #19	W W1toSet	0
18	MDMARQCLR18	MDMARQ clear #18	W W1toSet	0
17	MDMARQCLR17	MDMARQ clear #17	W W1toSet	0
16	MDMARQCLR16	MDMARQ clear #16	W W1toSet	0
15	MDMARQCLR15	MDMARQ clear #15	W W1toSet	0
14	MDMARQCLR14	MDMARQ clear #14	W W1toSet	0
13	MDMARQCLR13	MDMARQ clear #13	W W1toSet	0
12	MDMARQCLR12	MDMARQ clear #12	W W1toSet	0

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Bits	Field Name	Description	Type	Reset
11	MDMARQCLR11	MDMARQ clear #11	W W1toSet	0
10	MDMARQCLR10	MDMARQ clear #10	W W1toSet	0
9	MDMARQCLR9	MDMARQ clear #9	W W1toSet	0
8	MDMARQCLR8	MDMARQ clear #8	W W1toSet	0
7	MDMARQCLR7	MDMARQ clear #7	W W1toSet	0
6	MDMARQCLR6	MDMARQ clear #6	W W1toSet	0
5	MDMARQCLR5	MDMARQ clear #5	W W1toSet	0
4	MDMARQCLR4	MDMARQ clear #4	W W1toSet	0
3	MDMARQCLR3	MDMARQ clear #3	W W1toSet	0
2	MDMARQCLR2	MDMARQ clear #2	W W1toSet	0
1	MDMARQCLR1	MDMARQ clear #1	W W1toSet	0
0	MDMARQCLR0	MDMARQ clear #0	W W1toSet	0

Table 5-422. Register Call Summary for Register WUGEN_MEVTCLR3

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]

Table 5-423. WUGEN_MEVTCLR4

Address Offset	0x0000 0084		
Physical Address	0x01C2 1084	**Instance**	WUGEN_DSP
Description	This register is used to clear the dma request mask bits write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_MEVT2 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MDMARQCLR58	MDMARQCLR57	MDMARQCLR56	MDMARQCLR55	MDMARQCLR54	MDMARQCLR53	MDMARQCLR52	MDMARQCLR51	MDMARQCLR50	MDMARQCLR49	MDMARQCLR48	MDMARQCLR47	MDMARQCLR46	MDMARQCLR45	MDMARQCLR44	MDMARQCLR43	MDMARQCLR42	MDMARQCLR41	MDMARQCLR40	MDMARQCLR39	MDMARQCLR38	MDMARQCLR37	MDMARQCLR36	MDMARQCLR35	MDMARQCLR34	MDMARQCLR33	MDMARQCLR32

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved.	R	0x00
26	MDMARQCLR58	MDMARQ clear #58	W W1toSet	0
25	MDMARQCLR57	MDMARQ clear #57	W W1toSet	0
24	MDMARQCLR56	MDMARQ clear #56	W W1toSet	0
23	MDMARQCLR55	MDMARQ clear #55	W W1toSet	0

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Bits	Field Name	Description	Type	Reset
22	MDMARQCLR54	MDMARQ clear #54	W W1toSet	0
21	MDMARQCLR53	MDMARQ clear #53	W W1toSet	0
20	MDMARQCLR52	MDMARQ clear #52	W W1toSet	0
19	MDMARQCLR51	MDMARQ clear #51	W W1toSet	0
18	MDMARQCLR50	MDMARQ clear #50	W W1toSet	0
17	MDMARQCLR49	MDMARQ clear #49	W W1toSet	0
16	MDMARQCLR48	MDMARQ clear #48	W W1toSet	0
15	MDMARQCLR47	MDMARQ clear #47	W W1toSet	0
14	MDMARQCLR46	MDMARQ clear #46	W W1toSet	0
13	MDMARQCLR45	MDMARQ clear #45	W W1toSet	0
12	MDMARQCLR44	MDMARQ clear #44	W W1toSet	0
11	MDMARQCLR43	MDMARQ clear #43	W W1toSet	0
10	MDMARQCLR42	MDMARQ clear #42	W W1toSet	0
9	MDMARQCLR41	MDMARQ clear #41	W W1toSet	0
8	MDMARQCLR40	MDMARQ clear #40	W W1toSet	0
7	MDMARQCLR39	MDMARQ clear #39	W W1toSet	0
6	MDMARQCLR38	MDMARQ clear #38	W W1toSet	0
5	MDMARQCLR37	MDMARQ clear #37	W W1toSet	0
4	MDMARQCLR36	MDMARQ clear #36	W W1toSet	0
3	MDMARQCLR35	MDMARQ clear #35	W W1toSet	0
2	MDMARQCLR34	MDMARQ clear #34	W W1toSet	0
1	MDMARQCLR33	MDMARQ clear #33	W W1toSet	0
0	MDMARQCLR32	MDMARQ clear #32	W W1toSet	0

Table 5-424. Register Call Summary for Register WUGEN_MEVTCLR4

DSP Subsystem Functional Description
- Interrupt Requests: [0]
- Interrupts, DMA Requests, and Event Management: [1]
- Individual Event Mask Clear: [2]

DSP Subsystem Register Manual
- WUGEN_DSP Register Summary: [3]

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Table 5-425. WUGEN_MEVTSET0

Address Offset	0x0000 0088
Physical Address	0x01C2 1088 **Instance** WUGEN_DSP
Description	This register is used to set the interrupt mask bits (LSB) write 0: no effect write 1: sets the corresponding mask bit in the WUGEN_MEVT0 register reads always return 0
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQSET31	MIRQSET30	MIRQSET29	MIRQSET28	MIRQSET27	MIRQSET26	MIRQSET25	MIRQSET24	MIRQSET23	MIRQSET22	MIRQSET21	MIRQSET20	MIRQSET19	MIRQSET18	MIRQSET17	MIRQSET16	MIRQSET15	MIRQSET14	MIRQSET13	MIRQSET12	MIRQSET11	MIRQSET10	MIRQSET9	MIRQSET8	MIRQSET7	MIRQSET6	MIRQSET5	MIRQSET4	MIRQSET3	MIRQSET2	MIRQSET1	MIRQSET0

Bits	Field Name	Description	Type	Reset
31	MIRQSET31	MIRQ set #31	W W1toSet	0
30	MIRQSET30	MIRQ set #30	W W1toSet	0
29	MIRQSET29	MIRQ set #29	W W1toSet	0
28	MIRQSET28	MIRQ set #28	W W1toSet	0
27	MIRQSET27	MIRQ set #27	W W1toSet	0
26	MIRQSET26	MIRQ set #26	W W1toSet	0
25	MIRQSET25	MIRQ set #25	W W1toSet	0
24	MIRQSET24	MIRQ set #24	W W1toSet	0
23	MIRQSET23	MIRQ set #23	W W1toSet	0
22	MIRQSET22	MIRQ set #22	W W1toSet	0
21	MIRQSET21	MIRQ set #21	W W1toSet	0
20	MIRQSET20	MIRQ set #20	W W1toSet	0
19	MIRQSET19	MIRQ set #19	W W1toSet	0
18	MIRQSET18	MIRQ set #18	W W1toSet	0
17	MIRQSET17	MIRQ set #17	W W1toSet	0
16	MIRQSET16	MIRQ set #16	W W1toSet	0
15	MIRQSET15	MIRQ set #15	W W1toSet	0
14	MIRQSET14	MIRQ set #14	W W1toSet	0
13	MIRQSET13	MIRQ set #13	W W1toSet	0
12	MIRQSET12	MIRQ set #12	W W1toSet	0
11	MIRQSET11	MIRQ set #11	W W1toSet	0

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Bits	Field Name	Description	Type	Reset
10	MIRQSET10	MIRQ set #10	W W1toSet	0
9	MIRQSET9	MIRQ set #9	W W1toSet	0
8	MIRQSET8	MIRQ set #8	W W1toSet	0
7	MIRQSET7	MIRQ set #7	W W1toSet	0
6	MIRQSET6	MIRQ set #6	W W1toSet	0
5	MIRQSET5	MIRQ set #5	W W1toSet	0
4	MIRQSET4	MIRQ set #4	W W1toSet	0
3	MIRQSET3	MIRQ set #3	W W1toSet	0
2	MIRQSET2	MIRQ set #2	W W1toSet	0
1	MIRQSET1	MIRQ set #1	W W1toSet	0
0	MIRQSET0	MIRQ set #0	W W1toSet	0

Table 5-426. Register Call Summary for Register WUGEN_MEVTSET0

DSP Subsystem Functional Description

- Interrupt Requests: [0]
- Interrupts, DMA Requests, and Event Management: [1]
- Individual Event Masking: [2]

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [3]

Table 5-427. WUGEN_MEVTSET1

Address Offset	0x0000 008C		
Physical Address	0x01C2 108C	**Instance**	WUGEN_DSP
Description	This register is used to set the interrupt mask bits (MSB) write 0: no effect write 1: sets the corresponding mask bit in the WUGEN_MEVT1 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQSET63	MIRQSET62	MIRQSET61	MIRQSET60	MIRQSET59	MIRQSET58	MIRQSET57	MIRQSET56	MIRQSET55	MIRQSET54	MIRQSET53	MIRQSET52	MIRQSET51	MIRQSET50	MIRQSET49	MIRQSET48	MIRQSET47	MIRQSET46	MIRQSET45	MIRQSET44	MIRQSET43	MIRQSET42	MIRQSET41	MIRQSET40	MIRQSET39	MIRQSET38	MIRQSET37	MIRQSET36	MIRQSET35	MIRQSET34	MIRQSET33	MIRQSET32

Bits	Field Name	Description	Type	Reset
31	MIRQSET63	MIRQ set #63	W W1toSet	0
30	MIRQSET62	MIRQ set #62	W W1toSet	0
29	MIRQSET61	MIRQ set #61	W W1toSet	0
28	MIRQSET60	MIRQ set #60	W W1toSet	0

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Bits	Field Name	Description	Type	Reset
27	MIRQSET59	MIRQ set #59	W W1toSet	0
26	MIRQSET58	MIRQ set #58	W W1toSet	0
25	MIRQSET57	MIRQ set #57	W W1toSet	0
24	MIRQSET56	MIRQ set #56	W W1toSet	0
23	MIRQSET55	MIRQ set #55	W W1toSet	0
22	MIRQSET54	MIRQ set #22	W W1toSet	0
21	MIRQSET53	MIRQ set #53	W W1toSet	0
20	MIRQSET52	MIRQ set #52	W W1toSet	0
19	MIRQSET51	MIRQ set #51	W W1toSet	0
18	MIRQSET50	MIRQ set #50	W W1toSet	0
17	MIRQSET49	MIRQ set #49	W W1toSet	0
16	MIRQSET48	MIRQ set #48	W W1toSet	0
15	MIRQSET47	MIRQ set #47	W W1toSet	0
14	MIRQSET46	MIRQ set #46	W W1toSet	0
13	MIRQSET45	MIRQ set #45	W W1toSet	0
12	MIRQSET44	MIRQ set #44	W W1toSet	0
11	MIRQSET43	MIRQ set #43	W W1toSet	0
10	MIRQSET42	MIRQ set #42	W W1toSet	0
9	MIRQSET41	MIRQ set #41	W W1toSet	0
8	MIRQSET40	MIRQ set #40	W W1toSet	0
7	MIRQSET39	MIRQ set #39	W W1toSet	0
6	MIRQSET38	MIRQ set #38	W W1toSet	0
5	MIRQSET37	MIRQ set #37	W W1toSet	0
4	MIRQSET36	MIRQ set #36	W W1toSet	0
3	MIRQSET35	MIRQ set #35	W W1toSet	0
2	MIRQSET34	MIRQ set #34	W W1toSet	0
1	MIRQSET33	MIRQ set #33	W W1toSet	0
0	MIRQSET32	MIRQ set #32	W W1toSet	0

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Table 5-428. Register Call Summary for Register WUGEN_MEVTSET1

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]

Table 5-429. WUGEN_MEVTSET2

Address Offset	0x0000 0090		
Physical Address	0x01C2 1090	**Instance**	WUGEN_DSP
Description	This register is used to set the interrupt mask bits (MSB) write 0: no effect write 1: sets the corresponding mask bit in the WUGEN_MEVT1 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MIRQSET78	MIRQSET77	MIRQSET76	MIRQSET75	MIRQSET74	MIRQSET73	MIRQSET72	MIRQSET71	MIRQSET70	MIRQSET69	MIRQSET68	MIRQSET67	MIRQSET66	MIRQSET65	MIRQSET64	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved.	R	0x00000
14	MIRQSET78	MIRQ set #78	W W1toSet	0
13	MIRQSET77	MIRQ set #77	W W1toSet	0
12	MIRQSET76	MIRQ set #76	W W1toSet	0
11	MIRQSET75	MIRQ set #75	W W1toSet	0
10	MIRQSET74	MIRQ set #74	W W1toSet	0
9	MIRQSET73	MIRQ set #73	W W1toSet	0
8	MIRQSET72	MIRQ set #72	W W1toSet	0
7	MIRQSET71	MIRQ set #71	W W1toSet	0
6	MIRQSET70	MIRQ set #70s	W W1toSet	0
5	MIRQSET69	MIRQ set #69	W W1toSet	0
4	MIRQSET68	MIRQ set #68	W W1toSet	0
3	MIRQSET67	MIRQ set #67	W W1toSet	0
2	MIRQSET66	MIRQ set #66	W W1toSet	0
1	MIRQSET65	MIRQ set #65	W W1toSet	0
0	MIRQSET64	MIRQ set #64	W W1toSet	0

Table 5-430. Register Call Summary for Register WUGEN_MEVTSET2

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]

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Table 5-431. WUGEN_MEVTSET3

Address Offset	0x0000 0094		
Physical Address	0x01C2 1094	**Instance**	WUGEN_DSP
Description	This register is used to set the dma requests mask bits write 0: no effect write 1: sets the corresponding mask bit in the WUGEN_MEVT2 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDMARQSET31	MDMARQSET30	MDMARQSET29	MDMARQSET28	MDMARQSET27	MDMARQSET26	MDMARQSET25	MDMARQSET24	MDMARQSET23	MDMARQSET22	MDMARQSET21	MDMARQSET20	MDMARQSET19	MDMARQSET18	MDMARQSET17	MDMARQSET16	MDMARQSET15	MDMARQSET14	MDMARQSET13	MDMARQSET12	MDMARQSET11	MDMARQSET10	MDMARQSET9	MDMARQSET8	MDMARQSET7	MDMARQSET6	MDMARQSET5	MDMARQSET4	MDMARQSET3	MDMARQSET2	MDMARQSET1	MDMARQSET0

Bits	Field Name	Description	Type	Reset
31	MDMARQSET31	MDMARQ set #31	W W1toSet	0
30	MDMARQSET30	MDMARQ set #30	W W1toSet	0
29	MDMARQSET29	MDMARQ set #29	W W1toSet	0
28	MDMARQSET28	MDMARQ set #28	W W1toSet	0
27	MDMARQSET27	MDMARQ set #27	W W1toSet	0
26	MDMARQSET26	MDMARQ set #26	W W1toSet	0
25	MDMARQSET25	MDMARQ set #25	W W1toSet	0
24	MDMARQSET24	MDMARQ set #24	W W1toSet	0
23	MDMARQSET23	MDMARQ set #23	W W1toSet	0
22	MDMARQSET22	MDMARQ set #22	W W1toSet	0
21	MDMARQSET21	MDMARQ set #21	W W1toSet	0
20	MDMARQSET20	MDMARQ set #20	W W1toSet	0
19	MDMARQSET19	MDMARQ set #19	W W1toSet	0
18	MDMARQSET18	MDMARQ set #18	W W1toSet	0
17	MDMARQSET17	MDMARQ set #17	W W1toSet	0
16	MDMARQSET16	MDMARQ set #16	W W1toSet	0
15	MDMARQSET15	MDMARQ set #15	W W1toSet	0
14	MDMARQSET14	MDMARQ set #14	W W1toSet	0
13	MDMARQSET13	MDMARQ set #13	W W1toSet	0
12	MDMARQSET12	MDMARQ set #12	W W1toSet	0

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Bits	Field Name	Description	Type	Reset
11	MDMARQSET11	MDMARQ set #11	W W1toSet	0
10	MDMARQSET10	MDMARQ set #10	W W1toSet	0
9	MDMARQSET9	MDMARQ set #9	W W1toSet	0
8	MDMARQSET8	MDMARQ set #8	W W1toSet	0
7	MDMARQSET7	MDMARQ set #7	W W1toSet	0
6	MDMARQSET6	MDMARQ set #6	W W1toSet	0
5	MDMARQSET5	MDMARQ set #5	W W1toSet	0
4	MDMARQSET4	MDMARQ set #4	W W1toSet	0
3	MDMARQSET3	MDMARQ set #3	W W1toSet	0
2	MDMARQSET2	MDMARQ set #2	W W1toSet	0
1	MDMARQSET1	MDMARQ set #1	W W1toSet	0
0	MDMARQSET0	MDMARQ set #0	W W1toSet	0

Table 5-432. Register Call Summary for Register WUGEN_MEVTSET3

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]

Table 5-433. WUGEN_MEVTSET4

Address Offset	0x0000 0098		
Physical Address	0x01C2 1098	**Instance**	WUGEN_DSP
Description	This register is used to set the dma requests mask bits write 0: no effect write 1: sets the corresponding mask bit in the WUGEN_MEVT2 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MDMARQSET58	MDMARQSET57	MDMARQSET56	MDMARQSET55	MDMARQSET54	MDMARQSET53	MDMARQSET52	MDMARQSET51	MDMARQSET50	MDMARQSET49	MDMARQSET48	MDMARQSET47	MDMARQSET46	MDMARQSET45	MDMARQSET44	MDMARQSET43	MDMARQSET42	MDMARQSET41	MDMARQSET40	MDMARQSET39	MDMARQSET38	MDMARQSET37	MDMARQSET36	MDMARQSET35	MDMARQSET34	MDMARQSET33	MDMARQSET32

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved.	R	0x00
26	MDMARQSET58	MDMARQ set #58	W W1toSet	0
25	MDMARQSET57	MDMARQ set #57	W W1toSet	0
24	MDMARQSET56	MDMARQ set #56	W W1toSet	0
23	MDMARQSET55	MDMARQ set #55	W W1toSet	0

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Bits	Field Name	Description	Type	Reset
22	MDMARQSET54	MDMARQ set #54	W W1toSet	0
21	MDMARQSET53	MDMARQ set #53	W W1toSet	0
20	MDMARQSET52	MDMARQ set #52	W W1toSet	0
19	MDMARQSET51	MDMARQ set #51	W W1toSet	0
18	MDMARQSET50	MDMARQ set #50	W W1toSet	0
17	MDMARQSET49	MDMARQ set #49	W W1toSet	0
16	MDMARQSET48	MDMARQ set #48	W W1toSet	0
15	MDMARQSET47	MDMARQ set #47	W W1toSet	0
14	MDMARQSET46	MDMARQ set #46	W W1toSet	0
13	MDMARQSET45	MDMARQ set #45	W W1toSet	0
12	MDMARQSET44	MDMARQ set #44	W W1toSet	0
11	MDMARQSET43	MDMARQ set #43	W W1toSet	0
10	MDMARQSET42	MDMARQ set #42	W W1toSet	0
9	MDMARQSET41	MDMARQ set #41	W W1toSet	0
8	MDMARQSET40	MDMARQ set #40	W W1toSet	0
7	MDMARQSET39	MDMARQ set #39	W W1toSet	0
6	MDMARQSET38	MDMARQ set #38	W W1toSet	0
5	MDMARQSET37	MDMARQ set #37	W W1toSet	0
4	MDMARQSET36	MDMARQ set #36	W W1toSet	0
3	MDMARQSET35	MDMARQ set #35	W W1toSet	0
2	MDMARQSET34	MDMARQ set #34	W W1toSet	0
1	MDMARQSET33	MDMARQ set #33	W W1toSet	0
0	MDMARQSET32	MDMARQ set #32	W W1toSet	0

Table 5-434. Register Call Summary for Register WUGEN_MEVTSET4

DSP Subsystem Functional Description

- Interrupt Requests: [0]
- Interrupts, DMA Requests, and Event Management: [1]
- Individual Event Masking: [2]

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [3]

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Table 5-435. WUGEN_PENDEVT0

Address Offset	0x0000 009C		
Physical Address	0x01C2 109C	**Instance**	WUGEN_DSP
Description	This register holds the masked pending interrupts (LSB)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PENDIRQ31	PENDIRQ30	PENDIRQ29	PENDIRQ28	PENDIRQ27	PENDIRQ26	PENDIRQ25	PENDIRQ24	PENDIRQ23	PENDIRQ22	PENDIRQ21	PENDIRQ20	PENDIRQ19	PENDIRQ18	PENDIRQ17	PENDIRQ16	PENDIRQ15	PENDIRQ14	PENDIRQ13	PENDIRQ12	PENDIRQ11	PENDIRQ10	PENDIRQ9	PENDIRQ8	PENDIRQ7	PENDIRQ6	PENDIRQ5	PENDIRQ4	PENDIRQ3	PENDIRQ2	PENDIRQ1	PENDIRQ0

Bits	Field Name	Description	Type	Reset
31	PENDIRQ31	Masked pending interrupt number 31	R	0
30	PENDIRQ30	Masked pending interrupt number 30	R	0
29	PENDIRQ29	Masked pending interrupt number 29	R	0
28	PENDIRQ28	Masked pending interrupt number 28	R	0
27	PENDIRQ27	Masked pending interrupt number 27	R	0
26	PENDIRQ26	Masked pending interrupt number 26	R	0
25	PENDIRQ25	Masked pending interrupt number 25	R	0
24	PENDIRQ24	Masked pending interrupt number 24	R	0
23	PENDIRQ23	Masked pending interrupt number 23	R	0
22	PENDIRQ22	Masked pending interrupt number 22	R	0
21	PENDIRQ21	Masked pending interrupt number 21	R	0
20	PENDIRQ20	Masked pending interrupt number 20	R	0
19	PENDIRQ19	Masked pending interrupt number 19	R	0
18	PENDIRQ18	Masked pending interrupt number 18	R	0
17	PENDIRQ17	Masked pending interrupt number 17	R	0
16	PENDIRQ16	Masked pending interrupt number 16	R	0
15	PENDIRQ15	Masked pending interrupt number 15	R	0
14	PENDIRQ14	Masked pending interrupt number 14	R	0
13	PENDIRQ13	Masked pending interrupt number 13	R	0
12	PENDIRQ12	Masked pending interrupt number 12	R	0
11	PENDIRQ11	Masked pending interrupt number 11	R	0
10	PENDIRQ10	Masked pending interrupt number 10	R	0
9	PENDIRQ9	Masked pending interrupt number 9	R	0
8	PENDIRQ8	Masked pending interrupt number 8	R	0
7	PENDIRQ7	Masked pending interrupt number 7	R	0
6	PENDIRQ6	Masked pending interrupt number 6	R	0
5	PENDIRQ5	Masked pending interrupt number 5	R	0
4	PENDIRQ4	Masked pending interrupt number 4	R	0
3	PENDIRQ3	Masked pending interrupt number 3	R	0
2	PENDIRQ2	Masked pending interrupt number 2	R	0
1	PENDIRQ1	Masked pending interrupt number 1	R	0
0	PENDIRQ0	Masked pending interrupt number 0	R	0

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Table 5-436. Register Call Summary for Register WUGEN_PENDEVT0

DSP Subsystem Functional Description

- Interrupts, DMA Requests, and Event Management: [0]

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- WUGEN_DSP Register Summary: [1]
- WUGEN_DSP Register Description: [2]

Table 5-437. WUGEN_PENDEVT1

Address Offset	0x0000 00A0		
Physical Address	0x01C2 10A0	**Instance**	WUGEN_DSP
Description	This register holds the masked pending interrupts (MSB)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PENDIRQ63	PENDIRQ62	PENDIRQ61	PENDIRQ60	PENDIRQ59	PENDIRQ58	PENDIRQ57	PENDIRQ56	PENDIRQ55	PENDIRQ54	PENDIRQ53	PENDIRQ52	PENDIRQ51	PENDIRQ50	PENDIRQ49	PENDIRQ48	PENDIRQ47	PENDIRQ46	PENDIRQ45	PENDIRQ44	PENDIRQ43	PENDIRQ42	PENDIRQ41	PENDIRQ40	PENDIRQ39	PENDIRQ38	PENDIRQ37	PENDIRQ36	PENDIRQ35	PENDIRQ34	PENDIRQ33	PENDIRQ32

Bits	Field Name	Description	Type	Reset
31	PENDIRQ63	Masked pending interrupt number 63	R	0
30	PENDIRQ62	Masked pending interrupt number 62	R	0
29	PENDIRQ61	Masked pending interrupt number 61	R	0
28	PENDIRQ60	Masked pending interrupt number 60	R	0
27	PENDIRQ59	Masked pending interrupt number 59	R	0
26	PENDIRQ58	Masked pending interrupt number 58	R	0
25	PENDIRQ57	Masked pending interrupt number 57	R	0
24	PENDIRQ56	Masked pending interrupt number 56	R	0
23	PENDIRQ55	Masked pending interrupt number 55	R	0
22	PENDIRQ54	Masked pending interrupt number 54	R	0
21	PENDIRQ53	Masked pending interrupt number 53	R	0
20	PENDIRQ52	Masked pending interrupt number 52	R	0
19	PENDIRQ51	Masked pending interrupt number 51	R	0
18	PENDIRQ50	Masked pending interrupt number 50	R	0
17	PENDIRQ49	Masked pending interrupt number 49	R	0
16	PENDIRQ48	Masked pending interrupt number 48	R	0
15	PENDIRQ47	Masked pending interrupt number 47	R	0
14	PENDIRQ46	Masked pending interrupt number 46	R	0
13	PENDIRQ45	Masked pending interrupt number 45	R	0
12	PENDIRQ44	Masked pending interrupt number 44	R	0
11	PENDIRQ43	Masked pending interrupt number 43	R	0
10	PENDIRQ42	Masked pending interrupt number 42	R	0
9	PENDIRQ41	Masked pending interrupt number 41	R	0
8	PENDIRQ40	Masked pending interrupt number 40	R	0
7	PENDIRQ39	Masked pending interrupt number 39	R	0
6	PENDIRQ38	Masked pending interrupt number 38	R	0
5	PENDIRQ37	Masked pending interrupt number 37	R	0
4	PENDIRQ36	Masked pending interrupt number 36	R	0
3	PENDIRQ35	Masked pending interrupt number 35	R	0

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Bits	Field Name	Description	Type	Reset
2	PENDIRQ34	Masked pending interrupt number 34	R	0
1	PENDIRQ33	Masked pending interrupt number 33	R	0
0	PENDIRQ32	Masked pending interrupt number 32	R	0

Table 5-438. Register Call Summary for Register WUGEN_PENDEVT1

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]
- WUGEN_DSP Register Description: [1]

Table 5-439. WUGEN_PENDEVT2

Address Offset	0x0000 00A4		
Physical Address	0x01C2 10A4	**Instance**	WUGEN_DSP
Description	This register holds the masked pending interrupts (MSB)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PENDIRQ78	PENDIRQ77	PENDIRQ76	PENDIRQ75	PENDIRQ74	PENDIRQ73	PENDIRQ72	PENDIRQ71	PENDIRQ70	PENDIRQ69	PENDIRQ68	PENDIRQ67	PENDIRQ66	PENDIRQ65	PENDIRQ64	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved.	R	0x00000
14	PENDIRQ78	Masked pending interrupt number 78	R	0
13	PENDIRQ77	Masked pending interrupt number 77	R	0
12	PENDIRQ76	Masked pending interrupt number 76	R	0
11	PENDIRQ75	Masked pending interrupt number 75	R	0
10	PENDIRQ74	Masked pending interrupt number 74	R	0
9	PENDIRQ73	Masked pending interrupt number 73	R	0
8	PENDIRQ72	Masked pending interrupt number 72	R	0
7	PENDIRQ71	Masked pending interrupt number 71	R	0
6	PENDIRQ70	Masked pending interrupt number 70	R	0
5	PENDIRQ69	Masked pending interrupt number 69	R	0
4	PENDIRQ68	Masked pending interrupt number 68	R	0
3	PENDIRQ67	Masked pending interrupt number 67	R	0
2	PENDIRQ66	Masked pending interrupt number 66	R	0
1	PENDIRQ65	Masked pending interrupt number 65	R	0
0	PENDIRQ64	Masked pending interrupt number 64	R	0

Table 5-440. Register Call Summary for Register WUGEN_PENDEVT2

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]
- WUGEN_DSP Register Description: [1]

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Table 5-441. WUGEN_PENDEVT3

Address Offset	0x0000 00A8		
Physical Address	0x01C2 10A8	**Instance**	WUGEN_DSP
Description	This register holds the masked pending dma requests		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PENDDMARQ31	PENDDMARQ30	PENDDMARQ29	PENDDMARQ28	PENDDMARQ27	PENDDMARQ26	PENDDMARQ25	PENDDMARQ24	PENDDMARQ23	PENDDMARQ22	PENDDMARQ21	PENDDMARQ20	PENDDMARQ19	PENDDMARQ18	PENDDMARQ17	PENDDMARQ16	PENDDMARQ15	PENDDMARQ14	PENDDMARQ13	PENDDMARQ12	PENDDMARQ11	PENDDMARQ10	PENDDMARQ9	PENDDMARQ8	PENDDMARQ7	PENDDMARQ6	PENDDMARQ5	PENDDMARQ4	PENDDMARQ3	PENDDMARQ2	PENDDMARQ1	PENDDMARQ0

Bits	Field Name	Description	Type	Reset
31	PENDDMARQ31	Masked pending dma request number 31	R	0
30	PENDDMARQ30	Masked pending dma request number 30	R	0
29	PENDDMARQ29	Masked pending dma request number 29	R	0
28	PENDDMARQ28	Masked pending dma request number 28	R	0
27	PENDDMARQ27	Masked pending dma request number 27	R	0
26	PENDDMARQ26	Masked pending dma request number 26	R	0
25	PENDDMARQ25	Masked pending dma request number 25	R	0
24	PENDDMARQ24	Masked pending dma request number 24	R	0
23	PENDDMARQ23	Masked pending dma request number 23	R	0
22	PENDDMARQ22	Masked pending dma request number 22	R	0
21	PENDDMARQ21	Masked pending dma request number 21	R	0
20	PENDDMARQ20	Masked pending dma request number 20	R	0
19	PENDDMARQ19	Masked pending dma request number 19	R	0
18	PENDDMARQ18	Masked pending dma request number 18	R	0
17	PENDDMARQ17	Masked pending dma request number 17	R	0
16	PENDDMARQ16	Masked pending dma request number 16	R	0
15	PENDDMARQ15	Masked pending dma request number 15	R	0
14	PENDDMARQ14	Masked pending dma request number 14	R	0
13	PENDDMARQ13	Masked pending dma request number 13	R	0
12	PENDDMARQ12	Masked pending dma request number 12	R	0
11	PENDDMARQ11	Masked pending dma request number 11	R	0
10	PENDDMARQ10	Masked pending dma request number 10	R	0
9	PENDDMARQ9	Masked pending dma request number 9	R	0
8	PENDDMARQ8	Masked pending dma request number 8	R	0
7	PENDDMARQ7	Masked pending dma request number 7	R	0
6	PENDDMARQ6	Masked pending dma request number 6	R	0
5	PENDDMARQ5	Masked pending dma request number 5	R	0
4	PENDDMARQ4	Masked pending dma request number 4	R	0
3	PENDDMARQ3	Masked pending dma request number 3	R	0
2	PENDDMARQ2	Masked pending dma request number 2	R	0
1	PENDDMARQ1	Masked pending dma request number 1	R	0
0	PENDDMARQ0	Masked pending dma request number 0	R	0

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Table 5-442. Register Call Summary for Register WUGEN_PENDEVT3

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]
- WUGEN_DSP Register Description: [1]

Table 5-443. WUGEN_PENDEVT4

Address Offset	0x0000 00AC		
Physical Address	0x01C2 10AC	**Instance**	WUGEN_DSP
Description	This register holds the masked pending dma requests		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PENDDMARQ58	PENDDMARQ57	PENDDMARQ56	PENDDMARQ55	PENDDMARQ54	PENDDMARQ53	PENDDMARQ52	PENDDMARQ51	PENDDMARQ50	PENDDMARQ49	PENDDMARQ48	PENDDMARQ47	PENDDMARQ46	PENDDMARQ45	PENDDMARQ44	PENDDMARQ43	PENDDMARQ42	PENDDMARQ41	PENDDMARQ40	PENDDMARQ39	PENDDMARQ38	PENDDMARQ37	PENDDMARQ36	PENDDMARQ35	PENDDMARQ34	PENDDMARQ33	PENDDMARQ32

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved.	R	0x00
26	PENDDMARQ58	Masked pending dma request number 58	R	0
25	PENDDMARQ57	Masked pending dma request number 57	R	0
24	PENDDMARQ56	Masked pending dma request number 56	R	0
23	PENDDMARQ55	Masked pending dma request number 55	R	0
22	PENDDMARQ54	Masked pending dma request number 54	R	0
21	PENDDMARQ53	Masked pending dma request number 53	R	0
20	PENDDMARQ52	Masked pending dma request number 52	R	0
19	PENDDMARQ51	Masked pending dma request number 51	R	0
18	PENDDMARQ50	Masked pending dma request number 50	R	0
17	PENDDMARQ49	Masked pending dma request number 49	R	0
16	PENDDMARQ48	Masked pending dma request number 48	R	0
15	PENDDMARQ47	Masked pending dma request number 47	R	0
14	PENDDMARQ46	Masked pending dma request number 46	R	0
13	PENDDMARQ45	Masked pending dma request number 45	R	0
12	PENDDMARQ44	Masked pending dma request number 44	R	0
11	PENDDMARQ43	Masked pending dma request number 43	R	0
10	PENDDMARQ42	Masked pending dma request number 42	R	0
9	PENDDMARQ41	Masked pending dma request number 41	R	0
8	PENDDMARQ40	Masked pending dma request number 40	R	0
7	PENDDMARQ39	Masked pending dma request number 39	R	0
6	PENDDMARQ38	Masked pending dma request number 38	R	0
5	PENDDMARQ37	Masked pending dma request number 37	R	0
4	PENDDMARQ36	Masked pending dma request number 36	R	0
3	PENDDMARQ35	Masked pending dma request number 35	R	0
2	PENDDMARQ34	Masked pending dma request number 34	R	0
1	PENDDMARQ33	Masked pending dma request number 33	R	0
0	PENDDMARQ32	Masked pending dma request number 32	R	0

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Table 5-444. Register Call Summary for Register WUGEN_PENDEVT4

DSP Subsystem Functional Description

- Interrupts, DMA Requests, and Event Management: [0]

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [1]
- WUGEN_DSP Register Description: [2]

Table 5-445. WUGEN_PENDEVTCLR0

Address Offset	0x0000 00B0		
Physical Address	0x01C2 10B0	**Instance**	WUGEN_DSP
Description	This register clears the masked pending interrupts (LSB) : write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_PENDEVT0 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PENDIRQ31	PENDIRQ30	PENDIRQ29	PENDIRQ28	PENDIRQ27	PENDIRQ26	PENDIRQ25	PENDIRQ24	PENDIRQ23	PENDIRQ22	PENDIRQ21	PENDIRQ20	PENDIRQ19	PENDIRQ18	PENDIRQ17	PENDIRQ16	PENDIRQ15	PENDIRQ14	PENDIRQ13	PENDIRQ12	PENDIRQ11	PENDIRQ10	PENDIRQ9	PENDIRQ8	PENDIRQ7	PENDIRQ6	PENDIRQ5	PENDIRQ4	PENDIRQ3	PENDIRQ2	PENDIRQ1	PENDIRQ0

Bits	Field Name	Description	Type	Reset
31	PENDIRQ31	Masked pending interrupt number 31	W	0
30	PENDIRQ30	Masked pending interrupt number 30	W	0
29	PENDIRQ29	Masked pending interrupt number 29	W	0
28	PENDIRQ28	Masked pending interrupt number 28	W	0
27	PENDIRQ27	Masked pending interrupt number 27	W	0
26	PENDIRQ26	Masked pending interrupt number 26	W	0
25	PENDIRQ25	Masked pending interrupt number 25	W	0
24	PENDIRQ24	Masked pending interrupt number 24	W	0
23	PENDIRQ23	Masked pending interrupt number 23	W	0
22	PENDIRQ22	Masked pending interrupt number 22	W	0
21	PENDIRQ21	Masked pending interrupt number 21	W	0
20	PENDIRQ20	Masked pending interrupt number 20	W	0
19	PENDIRQ19	Masked pending interrupt number 19	W	0
18	PENDIRQ18	Masked pending interrupt number 18	W	0
17	PENDIRQ17	Masked pending interrupt number 17	W	0
16	PENDIRQ16	Masked pending interrupt number 16	W	0
15	PENDIRQ15	Masked pending interrupt number 15	W	0
14	PENDIRQ14	Masked pending interrupt number 14	W	0
13	PENDIRQ13	Masked pending interrupt number 13	W	0
12	PENDIRQ12	Masked pending interrupt number 12	W	0
11	PENDIRQ11	Masked pending interrupt number 11	W	0
10	PENDIRQ10	Masked pending interrupt number 10	W	0
9	PENDIRQ9	Masked pending interrupt number 9	W	0
8	PENDIRQ8	Masked pending interrupt number 8	W	0
7	PENDIRQ7	Masked pending interrupt number 7	W	0
6	PENDIRQ6	Masked pending interrupt number 6	W	0
5	PENDIRQ5	Masked pending interrupt number 5	W	0
4	PENDIRQ4	Masked pending interrupt number 4	W	0

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Bits	Field Name	Description	Type	Reset
3	PENDIRQ3	Masked pending interrupt number 3	W	0
2	PENDIRQ2	Masked pending interrupt number 2	W	0
1	PENDIRQ1	Masked pending interrupt number 1	W	0
0	PENDIRQ0	Masked pending interrupt number 0	W	0

Table 5-446. Register Call Summary for Register WUGEN_PENDEVTCLR0

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]

Table 5-447. WUGEN_PENDEVTCLR1

Address Offset	0x0000 00B4		
Physical Address	0x01C2 10B4	**Instance**	WUGEN_DSP
Description	This register clears the masked pending interrupts (MSB) : write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_PENDEVT1 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PENDIRQ63	PENDIRQ62	PENDIRQ61	PENDIRQ60	PENDIRQ59	PENDIRQ58	PENDIRQ57	PENDIRQ56	PENDIRQ55	PENDIRQ54	PENDIRQ53	PENDIRQ52	PENDIRQ51	PENDIRQ50	PENDIRQ49	PENDIRQ48	PENDIRQ47	PENDIRQ46	PENDIRQ45	PENDIRQ44	PENDIRQ43	PENDIRQ42	PENDIRQ41	PENDIRQ40	PENDIRQ39	PENDIRQ38	PENDIRQ37	PENDIRQ36	PENDIRQ35	PENDIRQ34	PENDIRQ33	PENDIRQ32

Bits	Field Name	Description	Type	Reset
31	PENDIRQ63	Masked pending interrupt number 63	W	0
30	PENDIRQ62	Masked pending interrupt number 62	W	0
29	PENDIRQ61	Masked pending interrupt number 61	W	0
28	PENDIRQ60	Masked pending interrupt number 60	W	0
27	PENDIRQ59	Masked pending interrupt number 59	W	0
26	PENDIRQ58	Masked pending interrupt number 58	W	0
25	PENDIRQ57	Masked pending interrupt number 57	W	0
24	PENDIRQ56	Masked pending interrupt number 56	W	0
23	PENDIRQ55	Masked pending interrupt number 55	W	0
22	PENDIRQ54	Masked pending interrupt number 54	W	0
21	PENDIRQ53	Masked pending interrupt number 53	W	0
20	PENDIRQ52	Masked pending interrupt number 52	W	0
19	PENDIRQ51	Masked pending interrupt number 51	W	0
18	PENDIRQ50	Masked pending interrupt number 50	W	0
17	PENDIRQ49	Masked pending interrupt number 49	W	0
16	PENDIRQ48	Masked pending interrupt number 48	W	0
15	PENDIRQ47	Masked pending interrupt number 47	W	0
14	PENDIRQ46	Masked pending interrupt number 46	W	0
13	PENDIRQ45	Masked pending interrupt number 45	W	0
12	PENDIRQ44	Masked pending interrupt number 44	W	0
11	PENDIRQ43	Masked pending interrupt number 43	W	0
10	PENDIRQ42	Masked pending interrupt number 42	W	0
9	PENDIRQ41	Masked pending interrupt number 41	W	0
8	PENDIRQ40	Masked pending interrupt number 40	W	0
7	PENDIRQ39	Masked pending interrupt number 39	W	0

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Bits	Field Name	Description	Type	Reset
6	PENDIRQ38	Masked pending interrupt number 38	W	0
5	PENDIRQ37	Masked pending interrupt number 37	W	0
4	PENDIRQ36	Masked pending interrupt number 36	W	0
3	PENDIRQ35	Masked pending interrupt number 35	W	0
2	PENDIRQ34	Masked pending interrupt number 34	W	0
1	PENDIRQ33	Masked pending interrupt number 33	W	0
0	PENDIRQ32	Masked pending interrupt number 32	W	0

Table 5-448. Register Call Summary for Register WUGEN_PENDEVTCLR1

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]

Table 5-449. WUGEN_PENDEVTCLR2

Address Offset	0x0000 00B8		
Physical Address	0x01C2 10B8	**Instance**	WUGEN_DSP
Description	This register clears the masked pending interrupts (LSB) : write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_PENDEVT2 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PENDIRQ78	PENDIRQ77	PENDIRQ76	PENDIRQ75	PENDIRQ74	PENDIRQ73	PENDIRQ72	PENDIRQ71	PENDIRQ70	PENDIRQ69	PENDIRQ68	PENDIRQ67	PENDIRQ66	PENDIRQ65	PENDIRQ64	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved.	R	0x00000
14	PENDIRQ78	Masked pending interrupt number 78	W	0
13	PENDIRQ77	Masked pending interrupt number 77	W	0
12	PENDIRQ76	Masked pending interrupt number 76	W	0
11	PENDIRQ75	Masked pending interrupt number 75	W	0
10	PENDIRQ74	Masked pending interrupt number 74	W	0
9	PENDIRQ73	Masked pending interrupt number 73	W	0
8	PENDIRQ72	Masked pending interrupt number 72	W	0
7	PENDIRQ71	Masked pending interrupt number 71	W	0
6	PENDIRQ70	Masked pending interrupt number 70	W	0
5	PENDIRQ69	Masked pending interrupt number 69	W	0
4	PENDIRQ68	Masked pending interrupt number 68	W	0
3	PENDIRQ67	Masked pending interrupt number 67	W	0
2	PENDIRQ66	Masked pending interrupt number 66	W	0
1	PENDIRQ65	Masked pending interrupt number 65	W	0
0	PENDIRQ64	Masked pending interrupt number 64	W	0

Table 5-450. Register Call Summary for Register WUGEN_PENDEVTCLR2

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]

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Table 5-451. WUGEN_PENDEVTCLR3

Address Offset	0x0000 00BC		
Physical Address	0x01C2 10BC	**Instance**	WUGEN_DSP
Description	This register clears the masked pending dma_requests: write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_PENDEVT3 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PENDDMARQ31	PENDDMARQ30	PENDDMARQ29	PENDDMARQ28	PENDDMARQ27	PENDDMARQ26	PENDDMARQ25	PENDDMARQ24	PENDDMARQ23	PENDDMARQ22	PENDDMARQ21	PENDDMARQ20	PENDDMARQ19	PENDDMARQ18	PENDDMARQ17	PENDDMARQ16	PENDDMARQ15	PENDDMARQ14	PENDDMARQ13	PENDDMARQ12	PENDDMARQ11	PENDDMARQ10	PENDDMARQ9	PENDDMARQ8	PENDDMARQ7	PENDDMARQ6	PENDDMARQ5	PENDDMARQ4	PENDDMARQ3	PENDDMARQ2	PENDDMARQ1	PENDDMARQ0

Bits	Field Name	Description	Type	Reset
31	PENDDMARQ31	Masked pending dma request number 31	W	0
30	PENDDMARQ30	Masked pending dma request number 30	W	0
29	PENDDMARQ29	Masked pending dma request number 29	W	0
28	PENDDMARQ28	Masked pending dma request number 28	W	0
27	PENDDMARQ27	Masked pending dma request number 27	W	0
26	PENDDMARQ26	Masked pending dma request number 26	W	0
25	PENDDMARQ25	Masked pending dma request number 25	W	0
24	PENDDMARQ24	Masked pending dma request number 24	W	0
23	PENDDMARQ23	Masked pending dma request number 23	W	0
22	PENDDMARQ22	Masked pending dma request number 22	W	0
21	PENDDMARQ21	Masked pending dma request number 21	W	0
20	PENDDMARQ20	Masked pending dma request number 20	W	0
19	PENDDMARQ19	Masked pending dma request number 19	W	0
18	PENDDMARQ18	Masked pending dma request number 18	W	0
17	PENDDMARQ17	Masked pending dma request number 17	W	0
16	PENDDMARQ16	Masked pending dma request number 16	W	0
15	PENDDMARQ15	Masked pending dma request number 15	W	0
14	PENDDMARQ14	Masked pending dma request number 14	W	0
13	PENDDMARQ13	Masked pending dma request number 13	W	0
12	PENDDMARQ12	Masked pending dma request number 12	W	0
11	PENDDMARQ11	Masked pending dma request number 11	W	0
10	PENDDMARQ10	Masked pending dma request number 10	W	0
9	PENDDMARQ9	Masked pending dma request number 9	W	0
8	PENDDMARQ8	Masked pending dma request number 8	W	0
7	PENDDMARQ7	Masked pending dma request number 7	W	0
6	PENDDMARQ6	Masked pending dma request number 6	W	0
5	PENDDMARQ5	Masked pending dma request number 5	W	0
4	PENDDMARQ4	Masked pending dma request number 4	W	0
3	PENDDMARQ3	Masked pending dma request number 3	W	0
2	PENDDMARQ2	Masked pending dma request number 2	W	0
1	PENDDMARQ1	Masked pending dma request number 1	W	0
0	PENDDMARQ0	Masked pending dma request number 0	W	0

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Table 5-452. Register Call Summary for Register WUGEN_PENDEVTCLR3

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]

Table 5-453. WUGEN_PENDEVTCLR4

Address Offset	0x0000 00C0		
Physical Address	0x01C2 10C0	**Instance**	WUGEN_DSP
Description	This register clears the masked pending dma_requests: write 0: no effect write 1: clears the corresponding mask bit in the WUGEN_PENDEVT4 register reads always return 0		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PENDDMARQ58	PENDDMARQ57	PENDDMARQ56	PENDDMARQ55	PENDDMARQ54	PENDDMARQ53	PENDDMARQ52	PENDDMARQ51	PENDDMARQ50	PENDDMARQ49	PENDDMARQ48	PENDDMARQ47	PENDDMARQ46	PENDDMARQ45	PENDDMARQ44	PENDDMARQ43	PENDDMARQ42	PENDDMARQ41	PENDDMARQ40	PENDDMARQ39	PENDDMARQ38	PENDDMARQ37	PENDDMARQ36	PENDDMARQ35	PENDDMARQ34	PENDDMARQ33	PENDDMARQ32

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved.	R	0x00
26	PENDDMARQ58	Masked pending dma request number 58	W	0
25	PENDDMARQ57	Masked pending dma request number 57	W	0
24	PENDDMARQ56	Masked pending dma request number 56	W	0
23	PENDDMARQ55	Masked pending dma request number 55	W	0
22	PENDDMARQ54	Masked pending dma request number 54	W	0
21	PENDDMARQ53	Masked pending dma request number 53	W	0
20	PENDDMARQ52	Masked pending dma request number 52	W	0
19	PENDDMARQ51	Masked pending dma request number 51	W	0
18	PENDDMARQ50	Masked pending dma request number 50	W	0
17	PENDDMARQ49	Masked pending dma request number 49	W	0
16	PENDDMARQ48	Masked pending dma request number 48	W	0
15	PENDDMARQ47	Masked pending dma request number 47	W	0
14	PENDDMARQ46	Masked pending dma request number 46	W	0
13	PENDDMARQ45	Masked pending dma request number 45	W	0
12	PENDDMARQ44	Masked pending dma request number 44	W	0
11	PENDDMARQ43	Mask pending dma request number 43	W	0
10	PENDDMARQ42	Masked pending dma request number 42	W	0
9	PENDDMARQ41	Masked pending dma request number 41	W	0
8	PENDDMARQ40	Masked pending dma request number 40	W	0
7	PENDDMARQ39	Masked pending dma request number 39	W	0
6	PENDDMARQ38	Masked pending dma request number 38	W	0
5	PENDDMARQ37	Masked pending dma request number 37	W	0
4	PENDDMARQ36	Masked pending dma request number 36	W	0
3	PENDDMARQ35	Masked pending dma request number 35	W	0
2	PENDDMARQ34	Masked pending dma request number 34	W	0
1	PENDDMARQ33	Masked pending dma request number 33	W	0
0	PENDDMARQ32	Masked pending dma request number 32	W	0

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Table 5-454. Register Call Summary for Register WUGEN_PENDEVTCLR4

DSP Subsystem Register Manual

- WUGEN_DSP Register Summary: [0]

5.5.10 SCACHE_CFG Registers

5.5.10.1 SCACHE_CFG Register Summary

Table 5-455. SCACHE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L1_SCACHE Physical Address	L2_SCACHE Physical Address
SCACHE_CONFIG	RW	32	0x0000 0004	0x01C3 0004	0x01C3 0204
SCACHE_INT	RW	32	0x0000 0008	0x01C3 0008	0x01C3 0208
SCACHE_OCP	RW	32	0x0000 000C	0x01C3 000C	0x01C3 020C
SCACHE_MAINT	RW	32	0x0000 0010	0x01C3 0010	0x01C3 0210
SCACHE_MTSTART	RW	32	0x0000 0014	0x01C3 0014	0x01C3 0214
SCACHE_MTEND	RW	32	0x0000 0018	0x01C3 0018	0x01C3 0218
SCACHE_CTADDR	RW	32	0x0000 001C	0x01C3 001C	0x01C3 021C
SCACHE_CTDATA	RW	32	0x0000 0020	0x01C3 0020	0x01C3 0220

5.5.10.2 SCACHE_CFG Register Description

Table 5-456. SCACHE_CONFIG

Address Offset	0x0000 0004		
Physical Address	0x01C3 0004 0x01C3 0204	**Instance**	L1_SCACHE L2_SCACHE
Description	Configuration Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											LOCK_MAIN	LOCK_PORT	LOCK_INT	BYPASS	SCACHE_LOCK

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0
4	LOCK_MAIN	Lock access to maintenance registers 0x0: Locked 0x1: Not locked	RW	1
3	LOCK_PORT	Lock access to interface registers 0x0: Locked 0x1: Not locked	RW	1
2	LOCK_INT	Lock access to interrupt registers 0x0: Locked 0x1: Not locked	RW	1

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Bits	Field Name	Description	Type	Reset
1	BYPASS	Bypass cache 0x0: Everything is non-cacheable. 0x1: Everything is cacheable.	RW	0
0	SCACHE_LOCK	SCACHE lock. Once this bit is set only debugger or hardware reset can clear. 0x0: No effect 0x1: Only debug accesses allowed	RW	0

Table 5-457. Register Call Summary for Register SCACHE_CONFIG

DSP Subsystem Programming Guide • Cacheability: [0]
DSP Subsystem Register Manual • SCACHE_CFG Register Summary: [1]

Table 5-458. SCACHE_INT

Address Offset	0x0000 0008		
Physical Address	0x01C3 0008 0x01C3 0208	**Instance**	L1_SCACHE L2_SCACHE
Description	Interrupt Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PORT			READ	WRITE	MAINT	PAGEFAULT	CONFIG

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved.	R	0x000000
8:5	PORT	slave interface number that has recorded an error	RW W1toClr	0x0
4	READ	interface read response error	RW W1toClr	0
3	WRITE	interface write response error	RW W1toClr	0
2	MAINT	maintenance is completed	RW W1toClr	0
1	PAGEFAULT	AMMU page fault	RW W1toClr	0
0	CONFIG	configuration error	RW W1toClr	0

Table 5-459. Register Call Summary for Register SCACHE_INT

DSP Subsystem Programming Guide • Global Cache Management: [0] [1] [2]
DSP Subsystem Register Manual • SCACHE_CFG Register Summary: [3]

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Table 5-460. SCACHE_OCP

Address Offset	0x0000 000C		
Physical Address	0x01C3 000C 0x01C3 020C	**Instance**	L1_SCACHE L2_SCACHE
Description	Interface Configuration Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										CLEANBUF	PREFETCH	CACHED	WRALLOCATE	WRBUFFER	WRAP

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved.	R	0x0000000
5	CLEANBUF	clean write and prefetch buffers in cache 0x0: do not clean 0x1: clean	RW	0
4	PREFETCH	always prefetch data 0x0: follow MMU policies 0x1: always prefetch	RW	0
3	CACHED	follow cacheable sideband signals 0x0: reads always not allocated, writes write through if cached 0x1: slave sideband signals determine policy	RW	1
2	WRALLOCATE	follow write allocate sideband signals 0x0: no writes are allocated independent to sideband 0x1: follow sideband	RW	0
1	WRBUFFER	write throughs and write back no allocate are buffered 0x0: write throughs and write back no allocated are not buffered 0x1: write throughs and write back no allocated are buffered	RW	0
0	WRAP	OCP wrap mode (critical word first) 0x0: disabled 0x1: enabled	RW	0

Table 5-461. Register Call Summary for Register SCACHE_OCP

DSP Subsystem Programming Guide
- Cacheability: [0]

DSP Subsystem Register Manual
- SCACHE_CFG Register Summary: [1]

Table 5-462. SCACHE_MAINT

Address Offset	0x0000 0010		
Physical Address	0x01C3 0010 0x01C3 0210	**Instance**	L1_SCACHE L2_SCACHE
Description	Maintenance Configuration Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										INTERRUPT	INVALIDATE	CLEAN	UNLOCK	LOCK	PRELOAD

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved.	R	0x0000000
5	INTERRUPT	generate interrupt when maintenance operation is complete 0x0: do not generate interrupt 0x1: generate interrupt	RW	0
4	INVALIDATE	invalidate lines in region defined by maintenance start/end addresses 0x0: do nothing 0x1: invalidate	RW	0
3	CLEAN	evict dirty lines in region defined by maintenance start/end addresses 0x0: do nothing 0x1: clean	RW	0
2	UNLOCK	unlock region defined by maintenance start/end addresses 0x0: do nothing 0x1: unlock	RW	0
1	LOCK	lock region defined by maintenance start/end addresses 0x0: do nothing 0x1: lock	RW	0
0	PRELOAD	preload region defined by maintenance start/end addresses 0x0: do nothing 0x1: preload	RW	0

Table 5-463. Register Call Summary for Register SCACHE_MAINT

DSP Subsystem Programming Guide
- Global Cache Management: [0] [1] [2]

DSP Subsystem Register Manual
- SCACHE_CFG Register Summary: [3]

Table 5-464. SCACHE_MTSTART

Address Offset 0x0000 0014

Physical Address 0x01C3 0014 (L1_SCACHE), 0x01C3 0214 (L2_SCACHE) **Instance** L1_SCACHE, L2_SCACHE

Description Maintenance Start Configuration Register

Type RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDR																															

Bits	Field Name	Description	Type	Reset
31:0	START_ADDR	start address of maintenance operations, reset to 0x0000 when finished	RW	0x0000 0000

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Table 5-465. Register Call Summary for Register SCACHE_MTSTART

DSP Subsystem Programming Guide • Global Cache Management: [0] [1]
DSP Subsystem Register Manual • SCACHE_CFG Register Summary: [2]

Table 5-466. SCACHE_MTEND

Address Offset	0x0000 0018		
Physical Address	0x01C3 0018 0x01C3 0218	**Instance**	L1_SCACHE L2_SCACHE
Description	Maintenance End Configuration Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDR																															

Bits	Field Name	Description	Type	Reset
31:0	END_ADDR	end address of maintenance operations, resets to 0x0000 when finished	RW	0x0000 0000

Table 5-467. Register Call Summary for Register SCACHE_MTEND

DSP Subsystem Programming Guide • Global Cache Management: [0] [1]
DSP Subsystem Register Manual • SCACHE_CFG Register Summary: [2]

Table 5-468. SCACHE_CTADDR

Address Offset	0x0000 001C		
Physical Address	0x01C3 001C 0x01C3 021C	**Instance**	L1_SCACHE L2_SCACHE
Description	Cache Test Address Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	ADDRESS	address of cache visibility when read CTDATA register, autoincrements	RW	0x0000 0000

Table 5-469. Register Call Summary for Register SCACHE_CTADDR

DSP Subsystem Register Manual • SCACHE_CFG Register Summary: [0]

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Table 5-470. SCACHE_CTDATA

Address Offset	0x0000 0020		
Physical Address	0x01C3 0020 0x01C3 0220	**Instance**	L1_SCACHE L2_SCACHE
Description	Cache Test Data Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	cache data at address of CTADDR register, CTADDR autoincrements each time CTDATA is read	RW	0x0000 0000

Table 5-471. Register Call Summary for Register SCACHE_CTDATA

DSP Subsystem Register Manual

- SCACHE_CFG Register Summary: [0]

5.5.11 SCACHE_SCTM Registers

5.5.11.1 SCACHE_SCTM Register Summary

Table 5-472. SCACHE_SCTM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SCACHE_SCTM Physical Address
SCACHE_SCTM_CTCNTL	RW	32	0x0000 0000	0x01C3 0400
RESERVED	R	32	0x0000 0020	0x01C3 0420
RESERVED	R	32	0x0000 0024	0x01C3 0424
RESERVED	R	32	0x0000 0028	0x01C3 0428
RESERVED	R	32	0x0000 002C	0x01C3 042C
SCACHE_SCTM_TINTVLR_i (1)	RW	32	0x0000 0040 + (0x4 * i)	0x01C3 0440 + (0x4 * i)
SCACHE_SCTM_CTDBGNUM	R	32	0x0000 007C	0x01C3 047C
SCACHE_SCTM_CTGNBL	RW	32	0x0000 00F0	0x01C3 04F0
SCACHE_SCTM_CTGRST	RW	32	0x0000 00F8	0x01C3 04F8
SCACHE_SCTM_CTCR_WT_i (1)	RW	32	0x0000 0100 + (0x4 * i)	0x01C3 0500 + (0x4 * i)
SCACHE_SCTM_CTCR_WOT_j (3)	RW	32	0x0000 0108 + (0x4 * j)	0x01C3 0508 + (0x4 * j)
SCACHE_SCTM_CTCNTR_k (2)	R	32	0x0000 0180 + (0x4 * k)	0x01C3 0580 + (0x4 * k)

(1) i = 0 to 1

(2) k = 0 to 7

(3) j = 0 to 5

5.5.11.2 SCACHE_SCTM Register Description

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Table 5-473. SCACHE_SCTM_CTCNTL

Address Offset	0x0000 0000		
Physical Address	0x01C3 0400	**Instance**	SCACHE_SCTM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUMSTM								NUMINPT								NUMTIMR								NUMCNTR							
REVISION																													IDLEMODE		ENBL

Bits	Field Name	Description	Type	Reset
31:26	NUMSTM	Number of timers that can export via STM	R	0x00
25:18	NUMINPT	Number of event input signals	R	0x1F
17:13	NUMTIMR	Number of timers in the module	R	0x02
12:7	NUMCNTR	Number of counters in the module	R	0x08
6:3	REVISION	Revision ID of SCTM	R	0x- TI internal data
2:1	IDLEMODE	Idle mode control 0x0: Force Idle mode 0x1: Ths SCTM will ackneledge the idle request, but never transition to the idle state 0x2: Ths SCTM uses the smart idle protocol. This is the default mode 0x3: Since the SCTM does not support internal wakeup, this mode is identical to smart_idle	RW	0x2
0	ENBL	SCTM global enable 0x0: Ths mode is disable. Only the configuration interface is functional. All other logic is reset 0x1: The module is enabled and individual counter/timers can be configured	RW	0

Table 5-474. Register Call Summary for Register SCACHE_SCTM_CTCNTL

DSP Subsystem Register Manual

- SCACHE_SCTM Register Summary: [0]

Table 5-475. SCACHE_SCTM_TINTVLR_i

Address Offset	0x0000 0040 + (0x4 * i)		
Physical Address	0x01C3 0440 + (0x4 * i)	**Instance**	SCACHE_SCTM
Description	These registers contain the interval match value for the corresponding timers in the SCTM		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERVAL																															

Bits	Field Name	Description	Type	Reset
31:0	INTERVAL	Interval match value for the timers in the SCTM	RW	0x0000 0000

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Table 5-476. Register Call Summary for Register SCACHE_SCTM_TINTVLR_i

DSP Subsystem Functional Description
- Periodic Intervals: [0] [1] [2]

DSP Subsystem Register Manual
- SCACHE_SCTM Register Summary: [3]

Table 5-477. SCACHE_SCTM_CTDBGNUM

Address Offset	0x0000 007C		
Physical Address	0x01C3 047C	**Instance**	SCACHE_SCTM
Description	Counter Timer Number Debug Event Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														NUMEVT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved.	R	0x0000 0000
2:0	NUMEVT	Number of input selectors for debug events	R	0x0

Table 5-478. Register Call Summary for Register SCACHE_SCTM_CTDBGNUM

DSP Subsystem Register Manual
- SCACHE_SCTM Register Summary: [0]

Table 5-479. SCACHE_SCTM_CTGNBL

Address Offset	0x0000 00F0		
Physical Address	0x01C3 04F0	**Instance**	SCACHE_SCTM
Description	These registers provide for simultaneous enable/disable of 32 counters		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ENABLE							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved.	R	0x000000
7:0	ENABLE	The counter enable bit field	RW	0x00

Table 5-480. Register Call Summary for Register SCACHE_SCTM_CTGNBL

DSP Subsystem Functional Description
- Counters: [0]

DSP Subsystem Register Manual
- SCACHE_SCTM Register Summary: [1]

Table 5-481. SCACHE_SCTM_CTGRST

Address Offset	0x0000 00F8		
Physical Address	0x01C3 04F8	**Instance**	SCACHE_SCTM
Description	These registers provide for simultaneous reset of 32 counters		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESET							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved.	R	0x000000
7:0	RESET	The counter reset bit field	RW	0x00

Table 5-482. Register Call Summary for Register SCACHE_SCTM_CTGRST

DSP Subsystem Functional Description
- Counters: [0]

DSP Subsystem Register Manual
- SCACHE_SCTM Register Summary: [1]

Table 5-483. SCACHE_SCTM_CTCR_WT_i

Address Offset	0x0000 0100 + (0x4 * i)		
Physical Address	0x01C3 0500 + (0x4 * i)	**Instance**	SCACHE_SCTM
Description	These registers contain the control and status settings for a single counter in the module. There will be a CTCR for every counter in the module (WT: with timer)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								INPSEL								RESERVED					RESTART	DBG	INT	CHNSDW	OVRFLW	IDLE	FREE	DURMODE	CHAIN	RESET	ENBL

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved.	R	0x000
20:16	INPSEL	Counter Timer input selection 0: Constantly asserted input that results in a free-running counter/timer 1-31: Index of event input signal selected	RW	0x00
15:11	RESERVED	Reserved.	R	0x00
10	RESTART	Restart the timer after an interval match 0: The timer stops after the first interval match. It must be manually reset by software before it starts counting again (run-once timer mode). 1: The timer immediately resets to 0 and begins incrementing again based on the current input configuration (restart timer mode).	RW	0
9	DBG	Signal debug logic on interval match 0: No debug event is generated. 1: Upon interval match, generates a debug event on the corresponding debug output event signal	RW	0
8	INT	Generate interrupt on interval match 0: No interrupt is generated. 1: Upon interval match, generates an interrupt on the corresponding interrupt output event signal	RW	0
7	CHNSDW	Counter has a shadow register for chain reads. 0: The read of the corresponding counter register returns the current value.	R	0

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Bits	Field Name	Description	Type	Reset
		1: Read of the high-order counter register, simultaneously loads the current value of the 32 LSBs into a shadow register. The read of the counter register that corresponds to this counter returns the value of the shadow register. This is applicable only when the counter is chained.		
6	OVRFLW	Counter has wrapped since it was last read 0: The counter has not wrapped since the last read. 1: The counter has wrapped since the last read.	R	0
5	IDLE	Counter ignores processor IDLE state 0: The counter does not increment during IDLE state. 1: The counter continues to function during IDLE state; applicable if IDLEMODE = 1.	RW	0
4	FREE	Counter ignores processor debug halt state 0: The counter does not increment (decrement) during the debug halt state. 1: The counter continues to function during debug halt state.	RW	0
3	DURMODE	Counter is in duration or occurrence mode 0: The counter operates in event mode. The counter increments by 1 each time a rising edge is seen on the designated input event signal. 1: The counter operates in duration mode. The counter increments every time a clock cycle is seen and the corresponding input event signal is asserted.	RW	0
2	CHAIN	Counter is chained to an adjacent counter 0: The counter is not chained. 1: Reserved	RW	0
1	RESET	Counter reset control 0: No effect 1: The corresponding counter is reset to the initial value and the OVERFLW bit is cleared. It continues to function if it is still enabled.	RW	0
0	ENBL	Counter enable control 0: The counter does not increment. 1: The counter increments as configured.	RW	0

Table 5-484. Register Call Summary for Register SCACHE_SCTM_CTCR_WT_i

DSP Subsystem Functional Description
- Input Events: [0]
- Counters: [1] [2] [3] [4] [5] [6] [7] [8] [9]
- Periodic Intervals: [10] [11] [12]
- Event Generation: [13] [14]

DSP Subsystem Register Manual
- SCACHE_SCTM Register Summary: [15]

Table 5-485. SCACHE_SCTM_CTCR_WOT_j

Address Offset	0x0000 0108 + (0x4 * j)		
Physical Address	0x01C3 0508 + (0x4 * j)	**Instance**	SCACHE_SCTM
Description	These registers contain the control and status settings for a single counter in the module. There will be a CTCR for every counter in the module (WOT: without timer)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											INPSEL					RESERVED								CHNSDW	OVRFLW	IDLE	FREE	DURMODE	CHAIN	RESET	ENBL

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved.	R	0x000
20:16	INPSEL	Counter input selection 0: Constant low signal on the output interface 1–31: Index of event input signal selected	RW	0x000
15:8	RESERVED	Reserved.	R	0x00
7	CHNSDW	Counter has a shadow register for chain reads. 0: The read of the corresponding counter register returns the current value. 1: Read of the high-order counter register, simultaneously loads the current value of the 32 LSBs into a shadow register. The read of the counter register that corresponds to this counter returns the value of the shadow register. This is applicable only when the counter is chained.	R	0
6	OVRFLW	Counter has wrapped since it was last read 0: The counter has not wrapped since the last read. 1: The counter has wrapped since the last read.	R	0
5	IDLE	Counter ignores processor IDLE state 0: The counter does not increment during IDLE state. 1: The counter continues to function during IDLE state; applicable if IDLEMODE = 1.	RW	0
4	FREE	Counter ignores processor debug halt state 0: The counter does not increment (decrement) during the debug halt state. 1: The counter continues to function during debug halt state.	RW	0
3	DURMODE	Counter is in duration or occurrence mode 0: The counter operates in event mode. The counter increments by 1 each time a rising edge is seen on the designated input event signal. 1: The counter operates in duration mode. The counter increments every time a clock cycle is seen and the corresponding input event signal is asserted.	RW	0
2	CHAIN	Counter is chained to an adjacent counter 0: The counter is not chained. 1: Reserved	RW	0
1	RESET	Counter reset control 0: No effect 1: The corresponding counter is reset to the initial value and the OVERFLW bit is cleared. It continues to function if it is still enabled.	RW	0
0	ENBL	Counter enable control 0: The counter does not increment. 1: The counter increments as configured.	RW	0

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Table 5-486. Register Call Summary for Register SCACHE_SCTM_CTCR_WOT_j

DSP Subsystem Functional Description • Input Events: [0] • Counters: [1] [2] [3] [4] [5] [6] [7] [8] [9]
DSP Subsystem Register Manual • SCACHE_SCTM Register Summary: [10]

Table 5-487. SCACHE_SCTM_CTCNTR_k

Address Offset	0x0000 0180 + (0x4 * k)		
Physical Address	0x01C3 0580 + (0x4 * k)	**Instance**	SCACHE_SCTM
Description	These registers contain the value of an individual counter in the moduel. There will be a CTCNTR for every counter in the module		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Counter value	R	0x0000 0000

Table 5-488. Register Call Summary for Register SCACHE_SCTM_CTCNTR_k

DSP Subsystem Functional Description • Periodic Intervals: [0]
DSP Subsystem Register Manual • SCACHE_SCTM Register Summary: [1]

5.5.12 SCACHE_MMU_DSP Registers

5.5.12.1 SCACHE_MMU_DSP Register Summary

Table 5-489. SCACHE_MMU_DSP Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SCACHE_MMU_DSP Physical Address
SCACHE_MMU_LARGE_ADDR_i [1]	RW	32	0x0000 0000 + (0x4 * i)	0x01C3 0800 + (0x4 * i)
SCACHE_MMU_LARGE_XLTE_i [1]	RW	32	0x0000 0020 + (0x4 * i)	0x01C3 0800 + (0x4 * i)
SCACHE_MMU_LARGE_POLICY_i [1]	RW	32	0x0000 0040 + (0x4 * i)	0x01C3 0840 + (0x4 * i)
SCACHE_MMU_MED_ADDR_j [2]	RW	32	0x0000 0060 + (0x4 * j)	0x01C3 0860 + (0x4 * j)
SCACHE_MMU_MED_XLTE_j [2]	RW	32	0x0000 00A0 + (0x4 * j)	0x01C3 08A0 + (0x4 * j)
SCACHE_MMU_MED_POLICY_j [2]	RW	32	0x0000 00E0 + (0x4 *j)	0x01C3 08E0 + (0x4 * j)
SCACHE_MMU_SMALL_ADDR_k [3]	RW	32	0x0000 0120 + (0x4 * k)	0x01C3 0920 + (0x4 * k)
SCACHE_MMU_SMALL_XLTE_k [3]	RW	32	0x0000 01A0 + (0x4 * k)	0x01C3 09A0 + (0x4 * k)

(1) i = 0 to 7
(2) j = 0 to 6
(3) k = 0 to 1

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Table 5-489. SCACHE_MMU_DSP Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	SCACHE_MMU_DSP Physical Address
SCACHE_MMU_SMALL_POLICY_k (3)	RW	32	0x0000 0220 + (0x4 * k)	0x01C3 0A20 + (0x4 * k)
SCACHE_MMU_SMALL_MAINT_k (3)	RW	32	0x0000 02A0 + (0x4 * k)	0x01C3 0AA0 + (0x4 * k)
SCACHE_MMU_MAINT	RW	32	0x0000 04A8	0x01C3 0CA8
SCACHE_MMU_MTSTART	RW	32	0x0000 04AC	0x01C3 0CAC
SCACHE_MMU_MTEND	RW	32	0x0000 04B0	0x01C3 0CB0
SCACHE_MMU_MAINTST	R	32	0x0000 04B4	0x01C3 0CB4
SCACHE_MMU_MMUCONFIG	RW	32	0x0000 04B8	0x01C3 0CB8

NOTE: The registers:

- SCACHE_MMU_LARGE_XLTE_i, where (i=0 to 7)
- SCACHE_MMU_MED_XLTE_j, where (j=0 to 6)
- SCACHE_MMU_SMALL_XLTE_k, where (k=0 to 1)

are NOT available in the DSP subsystem SCACHE_MMU_DSP register map. They are available only in the shared cache MMU in the IPU subsystem.

5.5.12.2 SCACHE_MMU_DSP Register Description

Table 5-490. SCACHE_MMU_LARGE_ADDR_i

Address Offset	0x0000 0000 + (0x4 * i)		
Physical Address	0x01C3 0800 + (0x4 * i)	**Instance**	SCACHE_MMU_DSP
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS								RESERVED																							

Bits	Field Name	Description	Type	Reset
31:25	ADDRESS	logical source address	RW	0x00
24:0	RESERVED	Reserved.	R	0x0000000

Table 5-491. Register Call Summary for Register SCACHE_MMU_LARGE_ADDR_i

DSP Subsystem Functional Description

- Attribute MMU Overview: [0]

DSP Subsystem Register Manual

- SCACHE_MMU_DSP Register Summary: [1]

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Table 5-492. SCACHE_MMU_LARGE_XLTE_i

Address Offset	0x0000 0020 + (0x4 * i)		
Physical Address	0x01C3 0800 + (0x4 * i)	**Instance**	SCACHE_MMU_DSP
Description	Large page translated address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS								RESERVED																							IGNORE

Bits	Field Name	Description	Type	Reset
31:25	ADDRESS	Logical source translated address	RW	0x00
24:1	RESERVED	Reserved	R	0x000000
0	IGNORE	Do not use translated address.	RW	0

Table 5-493. Register Call Summary for Register SCACHE_MMU_LARGE_XLTE_i

DSP Subsystem Functional Description

- Attribute MMU Overview: [0]

DSP Subsystem Register Manual

- SCACHE_MMU_DSP Register Summary: [1] [2]

Table 5-494. SCACHE_MMU_LARGE_POLICY_i

Address Offset	0x0000 0040 + (0x4 * i)		
Physical Address	0x01C3 0840 + (0x4 * i)	**Instance**	SCACHE_MMU_DSP
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								L2_WR_POLICY	L2_ALLOCATE	L2_POSTED	L2_CACHEABLE	L1_WR_POLICY	L1_ALLOCATE	L1_POSTED	L1_CACHEABLE	RESERVED								EXCLUSION	PRELOAD	READ	EXECUTE	VOLATILE	RESERVED	SIZE	ENABLE

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved.	R	0x00
23	L2_WR_POLICY	L2 write policy 0x0: write through 0x1: write back	RW	0
22	L2_ALLOCATE	L2 allocate policy 0x0: no writes are allocated 0x1: follow sideband	RW	0
21	L2_POSTED	L2 posted policy 0x0: not posted 0x1: posted	RW	0
20	L2_CACHEABLE	L2 cache policy 0x0: non-cacheable 0x1: cacheable	RW	0

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Bits	Field Name	Description	Type	Reset
19	L1_WR_POLICY	L1 write policy 0x0: write through 0x1: write back	RW	0
18	L1_ALLOCATE	L1 allocate policy 0x0: no writes are allocated 0x1: follow sideband	RW	0
17	L1_POSTED	L1 posted policy 0x0: not posted 0x1: posted	RW	0
16	L1_CACHEABLE	L1 cache policy 0x0: non-cacheable 0x1: cacheable	RW	0
15:8	RESERVED	Reserved.	R	0x00
7	EXCLUSION	cache exclusion 0x0: do not send exclusion sideband 0x1: send exclusion sideband	RW	0
6	PRELOAD	preload region 0x0: do not preload 0x1: preload	RW	0
5	READ	read only	RW	0
4	EXECUTE	execute only	RW	0
3	VOLATILE	volatile qualifier, see policy matrix 0x0: do not follow volatile qualifier 0x1: follow volatile qualifier	RW	0
2	RESERVED	Read returns 0. Write has no effect.	RW	0
1	SIZE	size of page	RW	0
0	ENABLE	enable page 0x0: page not enabled 0x1: page enabled	RW	0

Table 5-495. Register Call Summary for Register SCACHE_MMU_LARGE_POLICY_i

DSP Subsystem Functional Description
- Attribute MMU Overview: [0]

DSP Subsystem Register Manual
- SCACHE_MMU_DSP Register Summary: [1]

Table 5-496. SCACHE_MMU_MED_ADDR_j

Address Offset	0x0000 0060 + (0x4 * j)		
Physical Address	0x01C3 0860 + (0x4 * j)	**Instance**	SCACHE_MMU_DSP
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																RESERVED															

Bits	Field Name	Description	Type	Reset
31:17	ADDRESS	logical source address	RW	0x0000
16:0	RESERVED	Reserved	R	0x00000

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Table 5-497. Register Call Summary for Register SCACHE_MMU_MED_ADDR_j

DSP Subsystem Functional Description • Attribute MMU Overview: [0]
DSP Subsystem Register Manual • SCACHE_MMU_DSP Register Summary: [1]

Table 5-498. SCACHE_MMU_MED_XLTE_j

Address Offset	0x0000 00A0 + (0x4 * j)		
Physical Address	0x01C3 08A0 + (0x4 * j)	**Instance**	SCACHE_MMU_DSP
Description	Medium page translated address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																RESERVED															IGNORE

Bits	Field Name	Description	Type	Reset
31:17	ADDRESS	Logical source translated address	RW	0x0000
16:1	RESERVED	Reserved.	R	0x0000
0	IGNORE	Do not use translated address.	RW	0

Table 5-499. Register Call Summary for Register SCACHE_MMU_MED_XLTE_j

DSP Subsystem Functional Description • Attribute MMU Overview: [0]
DSP Subsystem Register Manual • SCACHE_MMU_DSP Register Summary: [1] [2]

Table 5-500. SCACHE_MMU_MED_POLICY_j

Address Offset	0x0000 00E0 + (0x4 * j)		
Physical Address	0x01C3 08E0 + (0x4 * j)	**Instance**	SCACHE_MMU_DSP
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								L2_WR_POLICY	L2_ALLOCATE	L2_POSTED	L2_CACHEABLE	L1_WR_POLICY	L1_ALLOCATE	L1_POSTED	L1_CACHEABLE	RESERVED								EXCLUSION	PRELOAD	READ	EXECUTE	VOLATILE	RESERVED	SIZE	ENABLE

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23	L2_WR_POLICY	L2 write policy 0x0: write through 0x1: write back	RW	0

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Bits	Field Name	Description	Type	Reset
22	L2_ALLOCATE	L2 allocate policy 0x0: no writes are allocated 0x1: follow sideband	RW	0
21	L2_POSTED	L2 posted policy 0x0: non posted 0x1: posted	RW	0
20	L2_CACHEABLE	L2 cache policy 0x0: non-cacheable 0x1: cacheable	RW	0
19	L1_WR_POLICY	L1 write policy 0x0: write through 0x1: write back	RW	0
18	L1_ALLOCATE	L1 allocate policy 0x0: no writes are allocated 0x1: follow sideband	RW	0
17	L1_POSTED	L1 posted policy 0x0: non posted 0x1: posted	RW	0
16	L1_CACHEABLE	L1 cache policy 0x0: non-cacheable 0x1: cacheable	RW	0
15:8	RESERVED	Reserved.	R	0x00
7	EXCLUSION	cache exclusion 0x0: do not send exclusion sideband 0x1: send exclusion sideband	RW	0
6	PRELOAD	preload region 0x0: do not preload 0x1: preload	RW	0
5	READ	read only	RW	0
4	EXECUTE	execute only	RW	0
3	VOLATILE	volatile qualifier, see policy matrix 0x0: do not follow volatile qualifier 0x1: follow volatile qualifier	RW	0
2	RESERVED	Read returns 0. Write has no effect.	RW	0
1	SIZE	size of page	RW	0
0	ENABLE	enable page 0x0: page not enabled 0x1: page enabled	RW	0

Table 5-501. Register Call Summary for Register SCACHE_MMU_MED_POLICY_j

DSP Subsystem Functional Description
- Attribute MMU Overview: [0]

DSP Subsystem Register Manual
- SCACHE_MMU_DSP Register Summary: [1]

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Table 5-502. SCACHE_MMU_SMALL_ADDR_k

Address Offset	0x0000 0120 + (0x4 * k)		
Physical Address	0x01C3 0920 + (0x4 * k)	**Instance**	SCACHE_MMU_DSP
Description	Small Page0 Address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																				RESERVED											

Bits	Field Name	Description	Type	Reset
31:12	ADDRESS	logical source address	RW	See Table 5-504.
11:0	RESERVED	Reserved.	R	0x000

Table 5-503. Register Call Summary for Register SCACHE_MMU_SMALL_ADDR_k

DSP Subsystem Functional Description
- Attribute MMU Overview: [0]

DSP Subsystem Register Manual
- SCACHE_MMU_DSP Register Summary: [1]

Table 5-504. Reset Value for ADDRESS

Instance	RETMODE
SCACHE_MMU_SMALL_ADDR_0	0x10800
SCACHE_MMU_SMALL_ADDR_1	0x1c300

Table 5-505. SCACHE_MMU_SMALL_XLTE_k

Address Offset	0x0000 01A0 + (0x4 * k)		
Physical Address	0x01C3 09A0 + (0x4 * k)	**Instance**	SCACHE_MMU_DSP
Description	Small page translated address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																				RESERVED											IGNORE

Bits	Field Name	Description	Type	Reset
31:12	ADDRESS	Logical source translated address	RW	0x00000
11:1	RESERVED	Reserved	R	0x000
0	IGNORE	Do not use translated address.	RW	0

Table 5-506. Register Call Summary for Register SCACHE_MMU_SMALL_XLTE_k

DSP Subsystem Functional Description
- Attribute MMU Overview: [0]

DSP Subsystem Register Manual
- SCACHE_MMU_DSP Register Summary: [1] [2]

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Table 5-507. SCACHE_MMU_SMALL_POLICY_k

Address Offset	0x0000 0220 + (0x4 * k)		
Physical Address	0x01C3 0A20 + (0x4 * k)	**Instance**	SCACHE_MMU_DSP
Description	Small page0 policy		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								L2_WR_POLICY	L2_ALLOCATE	L2_POSTED	L2_CACHEABLE	L1_WR_POLICY	L1_ALLOCATE	L1_POSTED	L1_CACHEABLE	RESERVED								COHERENCY	EXCLUSION	PRELOAD	READ	EXECUTE	VOLATILE	RESERVED	SIZE	ENABLE

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved.	R	0x00
23	L2_WR_POLICY	L2 write policy 0x0: write through 0x1: write back	RW	0
22	L2_ALLOCATE	L2 allocate policy 0x0: no writes are allocated 0x1: follow sideband	RW	0
21	L2_POSTED	L2 posted policy 0x0: non posted 0x1: posted	RW	0
20	L2_CACHEABLE	L2 cache policy 0x0: non-cacheable 0x1: cacheable	RW	0
19	L1_WR_POLICY	L1 write policy 0x0: write through 0x1: write back	RW	0
18	L1_ALLOCATE	L1 allocate policy 0x0: no writes are allocated 0x1: follow sideband	RW	0
17	L1_POSTED	L1 posted policy 0x0: non posted 0x1: posted	RW	0
16	L1_CACHEABLE	L1 cache policy 0x0: non-cacheable 0x1: cacheable	RW	0
15:9	RESERVED	Reserved.	R	0x00
8	COHERENCY	coherency	R	0
7	EXCLUSION	cache exclusion 0x0: do not send exclusion sideband 0x1: send exclusion sideband	RW	0
6	PRELOAD	preload region 0x0: do not preload 0x1: preload	RW	0
5	READ	read only	RW	1
4	EXECUTE	execute only	RW	1

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Bits	Field Name	Description	Type	Reset
3	VOLATILE	volatile qualifier, see policy matrix 0x0: do not follow volatile qualifier 0x1: follow volatile qualifier	RW	1
2	RESERVED	Read returns 1. Write has no effect.	RW	1
1	SIZE	size of page	RW	0
0	ENABLE	enable page 0x0: page not enabled 0x1: page enabled	RW	1

Table 5-508. Register Call Summary for Register SCACHE_MMU_SMALL_POLICY_k

DSP Subsystem Functional Description
- Attribute MMU Overview: [0]

DSP Subsystem Register Manual
- SCACHE_MMU_DSP Register Summary: [1]

Table 5-509. SCACHE_MMU_SMALL_MAINT_k

Address Offset	0x0000 02A0 + (0x4 * k)		
Physical Address	0x01C3 0AA0 + (0x4 * k)	**Instance**	SCACHE_MMU_DSP
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											INTERRUPT	INVALIDATE	CLEAN	LOCK	PRELOAD

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved.	R	0x0000000
4	INTERRUPT	generate interrupt when maintenance operation is complete	RW	0
3	INVALIDATE	invalidate page	RW	0
2	CLEAN	evict page	RW	0
1	LOCK	lock page	RW	0
0	PRELOAD	preload page	RW	0

Table 5-510. Register Call Summary for Register SCACHE_MMU_SMALL_MAINT_k

DSP Subsystem Register Manual
- SCACHE_MMU_DSP Register Summary: [0]

Table 5-511. SCACHE_MMU_MAINT

Address Offset	0x0000 04A8		
Physical Address	0x01C3 0CA8	**Instance**	SCACHE_MMU_DSP
Description	Maintenance Configuration Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					G_FLUSH	L2_CACHE	L1_CACHE2	L1_CACHE1	CPU_INTERRUPT	HOST_INTERRUPT	INVALIDATE	CLEAN	UNLOCK	LOCK	PRELOAD

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved.	R	0x000000
10	G_FLUSH	Global flush bit 0x0: do nothing, global flush done 0x1: invalidate L1+L2	RW	0
9	L2_CACHE	do maintenance operation in L2 Cache. Note: Hardware ensures that the maintenance operations are done in L1 first and then in L2 0x0: do nothing 0x1: perform maintenance operation selected by the maintenance bits	RW	0
8	L1_CACHE2	do maintenance operation in L1 Cache 2 0x0: do nothing 0x1: perform maintenance operation selected by the maintenance bits	RW	0
7	L1_CACHE1	do maintenance operation in L1 Cache1 0x0: do not perform maintenance operation 0x1: perform maintenance operation selected by the maintenance bits	RW	0
6	CPU_INTERRUPT	generate interrupt to cpu when maintenance operation initiated by CPU is complete 0x0: do not generate interrupt 0x1: generate interrupt	RW	0
5	HOST_INTERRUPT	generate interrupt when maintenance operation is complete 0x0: do not generate interrupt 0x1: generate interrupt	RW	0
4	INVALIDATE	invalidate lines in region defined by maintenance start/end addresses 0x0: do nothing 0x1: invalidate	RW	0
3	CLEAN	evict dirty lines in region defined by maintenance start/end addresses 0x0: do nothing 0x1: clean	RW	0
2	UNLOCK	unlock region defined by maintenance start/end addresses 0x0: do nothing 0x1: unlock	RW	0
1	LOCK	lock region defined by maintenance start/end addresses 0x0: do nothing 0x1: lock	RW	0

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Bits	Field Name	Description	Type	Reset
0	PRELOAD	preload region defined by maintenance start/end addresses 0x0: do nothing 0x1: preload	RW	0

Table 5-512. Register Call Summary for Register SCACHE_MMU_MAINT

DSP Subsystem Programming Guide • Global Cache Management: [0] [1] [2] [3] [4] [5] [6] [7] [8]
DSP Subsystem Register Manual • SCACHE_MMU_DSP Register Summary: [9]

Table 5-513. SCACHE_MMU_MTSTART

Address Offset	0x0000 04AC		
Physical Address	0x01C3 0CAC	**Instance**	SCACHE_MMU_DSP
Description	Maintenance Start Configuratoin Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BEGIN_ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	BEGIN_ADDRESS	Start address of maintenance operations, resets to 0x0000 when finished	RW	0x0000 0000

Table 5-514. Register Call Summary for Register SCACHE_MMU_MTSTART

DSP Subsystem Programming Guide • Global Cache Management: [0] [1]
DSP Subsystem Register Manual • SCACHE_MMU_DSP Register Summary: [2]

Table 5-515. SCACHE_MMU_MTEND

Address Offset	0x0000 04B0		
Physical Address	0x01C3 0CB0	**Instance**	SCACHE_MMU_DSP
Description	Maintenance End Configuration Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	END_ADDRESS	End address of maintenance operations, resets to 0x0000 when finished	RW	0x0000 0000

Table 5-516. Register Call Summary for Register SCACHE_MMU_MTEND

DSP Subsystem Programming Guide • Global Cache Management: [0] [1]
DSP Subsystem Register Manual • SCACHE_MMU_DSP Register Summary: [2]

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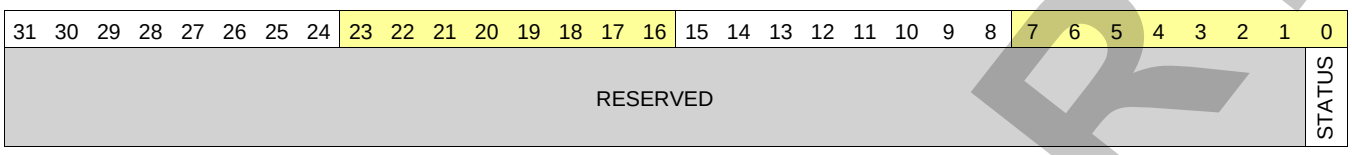
Table 5-517. SCACHE_MMU_MAINTST

Address Offset	0x0000 04B4		
Physical Address	0x01C3 0CB4	**Instance**	SCACHE_MMU_DSP
Description	Maintenance Status Register		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved.	R	0x0000 0000
0	STATUS	status bit Read 0x0: do nothing, maintenance completed Read 0x1: maintenance ongoing	R	0

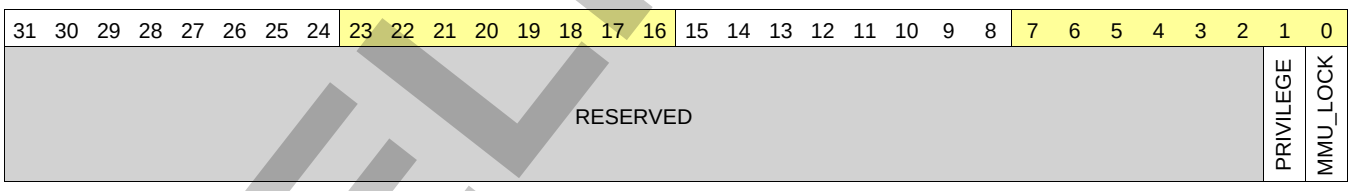
Table 5-518. Register Call Summary for Register SCACHE_MMU_MAINTST

DSP Subsystem Programming Guide
- Global Cache Management: [0] [1] [2] [3] [4]

DSP Subsystem Register Manual
- SCACHE_MMU_DSP Register Summary: [5]

Table 5-519. SCACHE_MMU_MMUCONFIG

Address Offset	0x0000 04B8		
Physical Address	0x01C3 0CB8	**Instance**	SCACHE_MMU_DSP
Description	MMU Configuration Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved.	R	0x0000 0000
1	PRIVILEGE	Privilege bit. Once this bit is set, only global flush, debugger, or hardware reset can clear. 0x0: CPU can access everything. 0x1: CPU can only access maintenance, and DMA cannot access MMU at all.	RW	0
0	MMU_LOCK	MMU lock. Once this bit is set only a global flush, debugger, or hardware reset can clear. 0x0: CPU can access everything. 0x1: CPU can only access maintenance, and DMA cannot access the MMU.	RW	0

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Table 5-520. Register Call Summary for Register SCACHE_MMU_MMUCONFIG

DSP Subsystem Register Manual

- SCACHE_MMU_DSP Register Summary: [0]

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IVA Subsystem

This chapter describes the IVA subsystem in the multimedia device.

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6.1 IVA Overview **1444**

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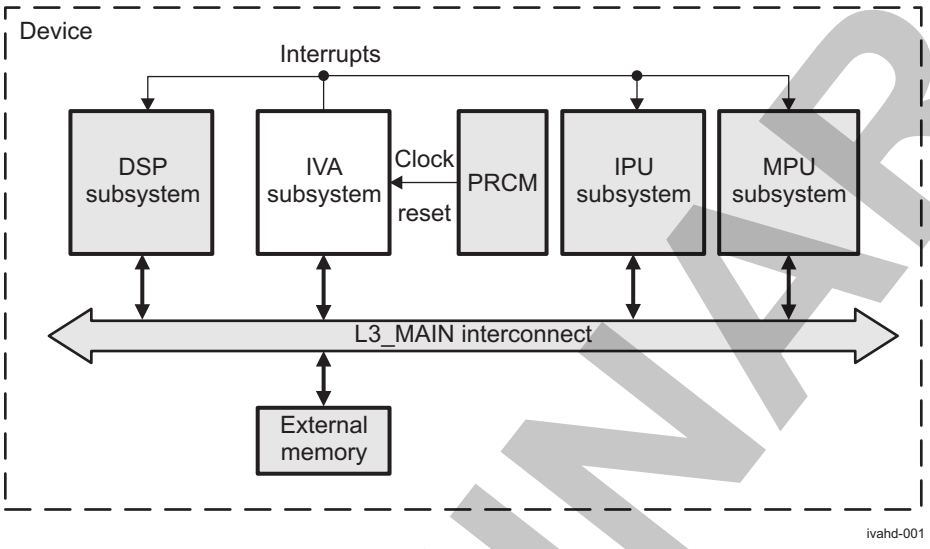
6.1 IVA Overview

The IVA is the image and video imaging hardware accelerator subsystem. Figure 6-1 shows the IVA subsystem in the device.

Figure 6-1. IVA in the Device



The IVA supports resolutions up to 1080 p/i with full performance of 60 fps (or 120 fields), achievable for encode or decode only (not for simultaneous encode and decode). The IVA subsystem supports the following coder/decoder (codec) standards natively; that is, all functions of standards are accelerated (without intervention of the digital signal processor [DSP]):

- H.264: BP/MP/HP encode and decode
- H.264: Fast profile/RCDO encode and decode
- MPEG-4: SP/ASP encode/decode (no support for GMC)
- DivX 5.x and higher encode/decode (no lower version; for example, 3.11 and 4.x)
- H.263: Profile 0 and 3 for decode, profile 0 for encode
- Sorenson Spark: V0 and V1 decode (no encode support)
- MPEG-2 SP/MP encode/decode
- MPEG-1 encode/decode
- VC-1/WMV9/RTV: SP/MP/AP encode and decode
- On2™ VP6/VP7 decode
- RealVideo® 8/9/10 decode
- AVS 1.0 encode and decode
- JPEG (also MJPEG) baseline encode/decode
- H.264 annex G (SVC) scalable baseline profile to 480p–720p30
- H.264 annex H (MVC) up to 720p30

The IVA subsystem is composed of:

- A primary sequencer, including its memories and an imaging controller: ICONT1
- A video direct memory access (VDMA) processor, which can be used as a secondary sequencer: ICONT2
- A VDMA engine: DMA_IVA
- An entropy codec: ECD3
- A motion compensation engine: MC3
- A transform and quantization calculation engine: CALC3

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- A loop filter acceleration engine: ILF3
- A motion estimation acceleration engine: IME3
- An intraprediction estimation engine: IPE3
- Shared level 2 (L2) interface and memory
- Local interconnect (L4_IVA)
- A message interface for communication between SYNCBOXes
- Mailbox
- A debug module for trace event and software instrumentation: SMSET

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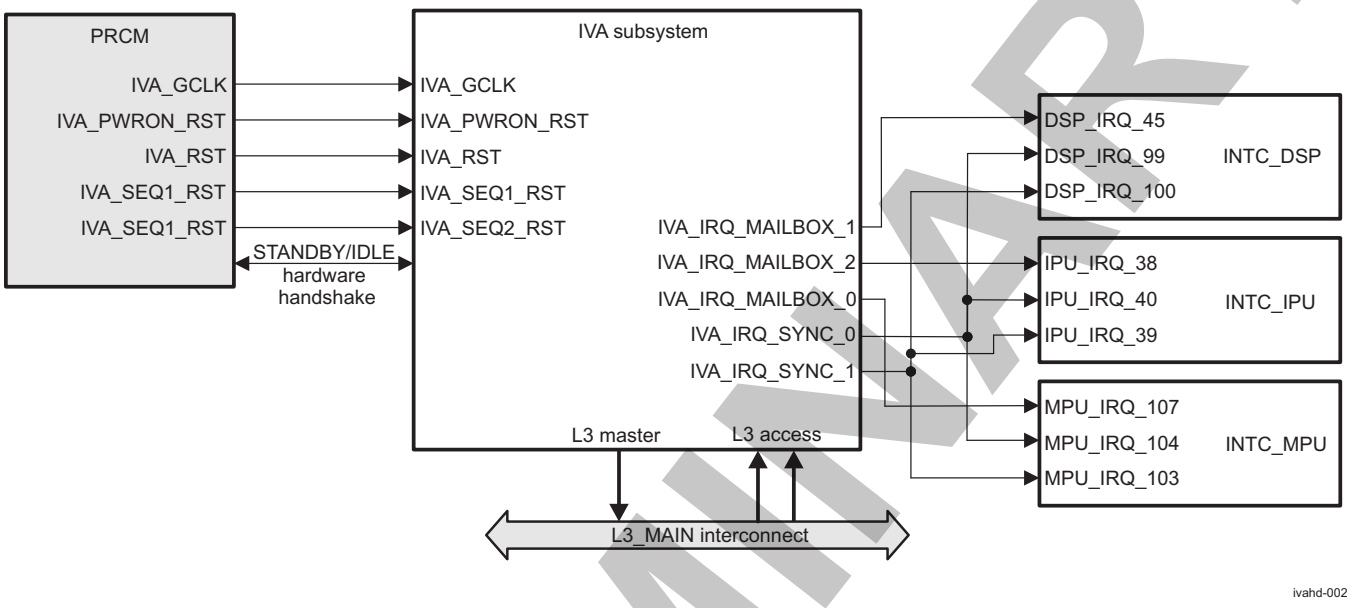
6.1.1 IVA Integration

This section describes the IVA in the device, including information about clocks, resets, and hardware requests.

Figure 6-2 shows the IVA integration.

Figure 6-2. IVA Integration



NOTE: For more information about the STANDBY/IDLE hardware handshake and the wake-up request, see Section 3.1.1.1.2, *Module-Level Clock Management*, in *Chapter 3, Power, Reset, and Clock Management*.

Table 6-1 through Table 6-3 summarize the integration of the module in the device.

Table 6-1. IVA Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
IVA	PD_IVA	L3_MAIN

Table 6-2. IVA Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
IVA	IVA_GCLK	IVA_GCLK	PRCM	IVA clock (functional and interface)
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
IVA	IVA_PWRON_RST	IVA_PWRON_RST	PRCM	IVA power-on reset (POR)
IVA	IVA_RST	IVA_RST	PRCM	IVA global reset (all logic is reset)
IVA	IVA_SEQ1_RST	IVA_SEQ1_RST	PRCM	ICONT1 reset
IVA	IVA_SEQ2_RST	IVA_SEQ2_RST	PRCM	ICONT2 reset

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Table 6-3. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
IVA	IVA_IRQ_MAILBOX_0	MPU_IRQ_107	INTC_MPU	IVA mailbox user 0 interrupt
IVA	IVA_IRQ_SYNC_0	MPU_IRQ_104	INTC_MPU	Sync interrupt from ICONT1
IVA	IVA_IRQ_SYNC_1	MPU_IRQ_103	INTC_MPU	Sync interrupt from ICONT2
IVA	IVA_IRQ_MAILBOX_1	DSP_IRQ_45	INTC_DSP	IVA mailbox user 1 interrupt
IVA	IVA_IRQ_SYNC_0	DSP_IRQ_99	INTC_DSP	Sync interrupt from ICONT1
IVA	IVA_IRQ_SYNC_1	DSP_IRQ_100	INTC_DSP	Sync interrupt from ICONT2
IVA	IVA_IRQ_MAILBOX_2	IPU_IRQ_38	INTC_IPU	IVA mailbox user 2 interrupt
IVA	IVA_IRQ_SYNC_0	IPU_IRQ_40	INTC_IPU	Sync interrupt from ICONT1
IVA	IVA_IRQ_SYNC_1	IPU_IRQ_39	INTC_IPU	Sync interrupt from ICONT2

NOTE:

- For more information about the mailbox interrupt, see Section 19.1.

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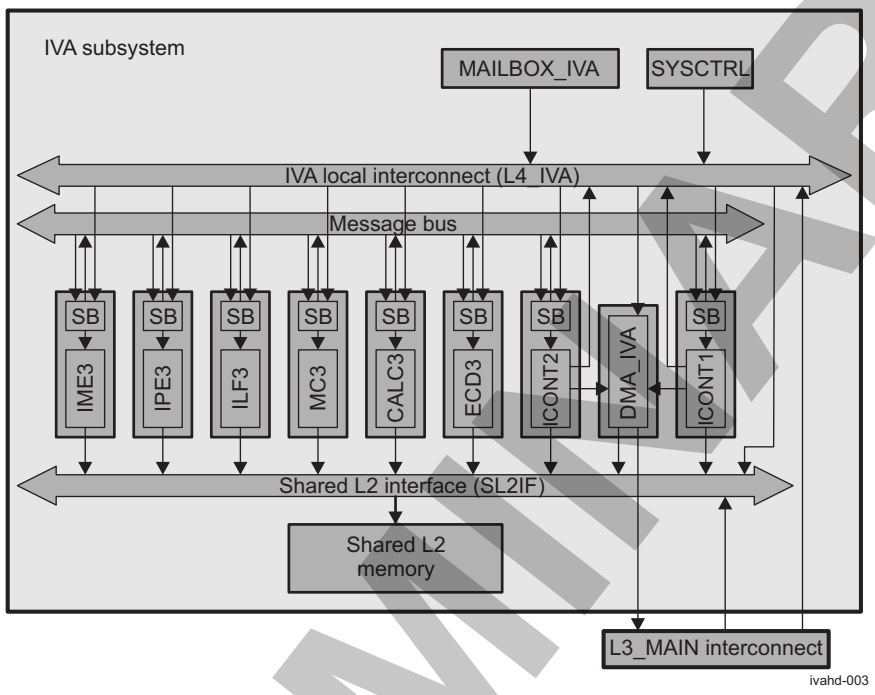
6.1.2 IVA Functional Description

6.1.2.1 IVA Block Diagram

Figure 6-3 is a block diagram of the IVA subsystem.

Figure 6-3. IVA Block Diagram



NOTE: SB stands for SYNCBOX.

NOTE: IPE3, MC3, CALC3, and ECD3 include a load and store engine (LSE), which is the same in each of these modules.

6.1.2.1.1 SYNCBOX

The SYNCBOX is a configurable module that schedules all embedded hardware modules within the IVA subsystem. The SYNCBOX handles all aspects of synchronization, data sharing, and parameters passing between accelerators. Also, the SYNCBOX permits the use of asynchronous messages.

6.1.2.1.2 ICONTs

The ICONT module is an ARM968E-S™-based microcontroller with 32 KiB of instruction tightly coupled memory and 16 KiB of data tightly coupled memory. It includes an interrupt controller (INTC), a local data mover, its own SYNCBOX module for synchronizing tasks with other modules, and its associated SYNCBOX handler.

Two identical instances of ICONT (ICONT1 and ICONT2) are present in the IVA subsystem. They can typically be used to perform high-level processing (at frame and slice levels), control bounding box computation at the macroblock level, and process other DMA_IVA tasks.

Software can map process equally on either ICONT module.

6.1.2.1.3 DMA_IVA

The DMA_IVA is a DMA engine that performs data transfers between external memories and shared L2 memory, and also memory-copies inside the SL2 and external memory.

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6.1.2.1.4 IME3

The IME3 accelerator performs motion estimation in encode processing. The IME3 embeds its own SYNCBOX module for synchronizing tasks with other modules.

The IME3 compares a current macroblock to a reference area and provides area in a reference region (in terms of offsets) that differs least from the current macroblock. IME3 can also interpolate a block with half- or quarter-pixel precision, thus producing 4 (half pixel) or 16 (quarter pixel) interpolated blocks from the original block. Additionally, the IME3 supports searching for the best matching block within the interpolated planes.

6.1.2.1.5 IPE3

The IPE3 accelerator performs intraprediction estimation in encode. The IPE3 embeds its own SYNCBOX module for synchronizing tasks with other modules and an LSE to transfer data from internal memories to shared L2 memory.

The IPE3 supports two modes, depending on the video standard:

- Spatial intraprediction estimation for H.264 and AVS. It creates intraprediction macroblocks with given intramodes from the original macroblock and provides cost estimation between the original macroblock and each pseudo intraprediction macroblock, and then chooses a mode with the smallest cost to recommend as an optimal intraprediction mode.
- Spatial activity for MPEG-1/-/2/-4 and VC-1. It calculates the spatial activity of the original luminance samples with the specified block size. This mode provides information on the original Luma pixels. The values can be used to decide the coding parameters of the macroblock, such as the coding mode and quantization parameter.

6.1.2.1.6 MC3

The MC3 accelerator performs motion compensation. The MC3 embeds its own SYNCBOX module for synchronizing tasks with other HWAs and an LSE to transfer data from internal memories to shared L2 memory.

The MC3 creates an interprediction macroblock with given motion vectors and modes from the reference data.

6.1.2.1.7 CALC3

The CALC3 accelerator performs forward and inverse transform and quantization calculation. The CALC3 embeds its own SYNCBOX module for synchronizing tasks with other HWAs and an LSE to transfer data from internal memories to shared L2 memory.

The CALC3 can perform transform and inverse transform, Q/iQ, and DC/AC prediction.

6.1.2.1.8 ILF3

The ILF3 accelerator performs deblocking filtering and boundary strength computation. The ILF3 embeds its own SYNCBOX module for synchronizing tasks with other HWAs.

6.1.2.1.9 ECD3

The ECD3 accelerator encodes and decodes the stream. The ECD3 embeds its own SYNCBOX module for synchronizing tasks with other HWAs and an LSE to transfer data from internal memories to shared L2 memory.

The ECD3 supports Huffman codes and arithmetic codes.

For encode, the ECD3 encodes the macroblock information and residual data into the bitstream. For decode, the ECD3 decodes the bitstream and recovers the macroblock information and residual data.

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6.1.2.1.10 SL2 Interface

The shared L2 interface (SL2IF) is an arbitrator that lets 18 initiators access an interleaved set of eight memory banks.

The SL2IF has two sets of interfaces:

- Eighteen 128-bit interfaces for accesses from modules to shared L2 memories
- Eight 128-bit memory interfaces for direct accesses to the memory bank

6.1.2.1.11 Message Bus

The message bus is an arbitrator that allows eight initiators to access eight targets. It is used to dispatch messages generated by the SYNCBOX of the different IPs.

6.1.2.1.12 IVA Local Interconnect (L4_IVA)

The IVA local interconnect provides connectivity between:

- One external host interconnect (L3_MAIN)
- Two local sequencers (ICONT1 and ICONT2)
- Video hardware accelerators (IME3, ILF3, ECD3, CALC3, MC3, IPE3)
- Video DMA engine (DMA_IVA)
- Local modules (mailbox and sysctrl)

6.1.2.1.13 MailBox

The mailbox supports 2-way communication between two hosts through an interrupt. It allows software to establish a communication channel between processors through a set of registers and associated interrupt signals by sending and receiving messages.

The mailbox embedded inside the IVA subsystem implements a 2-way communication between three external users and one internal user. This communication is ensured through three pairs of mailboxes and a 4-message deep FIFO for each message queue.

NOTE: The internal user is one of the two ICONTs. ICONT1 and ICONT2 are connected on a shared interrupt line. The choice between ICONT1 and ICONT2 is done by masking a mailbox interrupt on ICONT1 or ICONT2. ICONT1 and ICONT2 can access the mailbox through the IVA local interconnect.

6.1.2.1.14 IVA System Control

The SYSCTRL module of the IVA:

- Controls clocks to modules, upon software control and power handshaking state
- Controls power handshaking in the power, reset, and clock management (PRCM) module
- Provides the status of the previously mentioned operation
- Supports synchronization through external event

6.1.2.2 IVA Power Management

Table 6-4 lists the power-management features available for the IVA module.

NOTE: For descriptions of the IdleMode and StandbyMode features, see Module-Level Clock Management, in *Power, Reset, and Clock Management* chapter.

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Table 6-4. Local Power-Management Features

Feature	Registers	Description
Slave- idle modes	IVAHD_SYSCONFIG[3:2] IDLEMODE	No-idle and smart-idle modes are available.
Master standby modes	IVAHD_SYSCONFIG[5:4] STANDBYMODE	No-standby and smart-standby modes are available.

6.1.2.3 IVA Memory Mapping

ARM968E-S (of each ICONT) can address a 4-GiB memory space. The lower address range (8 MiB) is allocated to its level 1 (L1) memories (ITCM and DTCM). The higher address range is allocated to L2 memories. Access to L2 memories can be buffered or nonbuffered, depending on the selected address range. For more information, see the *ARM968E-STM Technical Reference Manual*.

In Table 6-5, the address spaces of buffered regions are shown as EXT_BUF, and the address spaces of nonbuffered regions are listed as EXT_NBUF.

Table 6-5. ICONT Memory Mapping Regions

Region Name	Address		Size	Description
	Start	Stop	(KiB)	
ITCM	0x0000 0000	0x0000 FFFF	64	ITCM memory aliased 64 times
	...	...	...	
ITCM (alias 63)	0x003F 0000	0x003F FFFF	64	
DTCM	0x0040 0000	0x0040 7FFF	32	DTCM memory aliased 128 times
	...	...	...	
DTCM (alias 127)	0x007F 8000	0x007F FFFF	32	
EXT_BUF	0x0080 0000	0x008F FFFF	1024	External buffered region
	...	...	...	
EXT_BUF (alias 247)	0x0FF0 0000	0x0FFF FFFF	1024	External buffered region
EXT_NBUF (alias)	0x1000 0000	0x100F 0000	1024	External nonbuffered region
	...	...	...	
EXT_NBUF (alias)	0x1FF0 00000	0x1FFF FFFF	1024	External nonbuffered region
	...	...	...	
EXT_BUF (alias)	0xM000 0000	0xM0FF FFFF	1024	External buffered region
	...	...	...	
EXT_NBUF (alias)	0xFFF0 0000	0xFFFF FFFF	1024	External nonbuffered region

Each of these regions (EXT_BUF and EXT_NBUF) has the same memory map, aliased throughout the address range of the region. Table 6-6 lists ICONT1 memory mapping, and Table 6-7 lists ICONT2 memory mapping. Offsets shown are from the start of the region.

Table 6-6. ICONT1 Memory Mapping

Module	Offset in Region		Size
	Begin	End	KiB
SL2 – Mem	0x0000 0000	0x0003 FFFF	256
Reserved	0x0004 0000	0x0007 FFFF	256
ICONT1 – DMem	0x0008 0000	0x0008 3FFF	16
Reserved	0x0008 4000	0x0008 7FFF	16
ICONT1 – IMem	0x0008 8000	0x0008 FFFF	32
ICONT2 – DMem	0x0009 0000	0x0009 3FFF	16
Reserved	0x0009 4000	0x0009 7FFF	16
ICONT2 – IMem	0x0009 8000	0x0009 FFFF	32

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Table 6-6. ICONT1 Memory Mapping (continued)

Module	Offset in Region		Size
	Begin	End	KiB
ECD3 – Mem	0x000A 0000	0x000A 7FFF	32
CALC3 – Mem	0x000A 8000	0x000A BFFF	16
Reserved	0x000A C000	0x000A FFFF	16
MC3 – Mem	0x000B 0000	0x000B 7FFF	32
IPE3 – Mem	0x000B 8000	0x000B 8FFF	4
Reserved	0x000B 9000	0x000C 0FFF	32
SMSET – Reg	0x000C 1000	0x000C 1FFF	4
SMSET – SWI	0x000C 2000	0x000C 27FF	2
Reserved	0x000C 2800	0x000C FFFF	54
DMA_IVA – Reg	0x000D 0000	0x000D 1FFF	8
ILF3 – Reg	0x000D 2000	0x000D 2FFF	4
Reserved	0x000D 3000	0x000D 3FFF	4
IME3 – Reg	0x000D 4000	0x000D 7FFF	16
CALC3 – Reg	0x000D 8000	0x000D 87FF	2
IPE3 – Reg	0x000D 8800	0x000D 8FFF	2
MC3 – Reg	0x000D 9000	0x000D 97FF	2
ECD3 – Reg	0x000D 9800	0x000D 9FFF	2
Reserved	0x000D A000	0x000D A3FF	1
SysControl	0x000D A400	0x000D A7FF	1
Mailbox	0x000D A800	0x000D ABFF	1
Reserved	0x000D AC00	0x000D FFFF	21
ICONT1 – SYNCBOX	0x000E 0000	0x000E 07FF	2
ICONT2 – SYNCBOX	0x000E 0800	0x000E 0FFF	2
ILF3 – SYNCBOX	0x000E 1000	0x000E 17FF	2
IME3 – SYNCBOX	0x000E 1800	0x000E 1FFF	2
CALC3 – SYNCBOX	0x000E 2000	0x000E 27FF	2
IPE3 – SYNCBOX	0x000E 2800	0x000E 2FFF	2
MC3 – SYNCBOX	0x000E 3000	0x000E 37FF	2
ECD3 – SYNCBOX	0x000E 3800	0x000E 3FFF	2
Reserved	0x000E 4000	0x000E FFFF	48
ICONT1 – Reg[(1)]	0x000F 0000	0x000F 0FFF	4
ICONT2 – Reg	0x000F 1000	0x000F 1FFF	4
ICONT1 – Reg [(2)]	0x000F 2000	0x000F 2FFF	4
Reserved	0x000F 3000	0x000F FFFF	52

(1) ICONT1 private access to its own registers
(2) ICONT1 self-access to its own registers

Table 6-7. ICONT2 Memory Mapping

Module	Offset in Region		Size
	Begin	End	KiB
SL2 – Mem	0x0000 0000	0x0003 FFFF	256
Reserved	0x0004 0000	0x0007 FFFF	256
ICONT1 – DMem	0x0008 0000	0x0008 3FFF	16
Reserved	0x0008 4000	0x0008 7FFF	16
ICONT1 – IMem	0x0008 8000	0x0008 FFFF	32
ICONT2 – DMem	0x0009 0000	0x0009 3FFF	16

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Table 6-7. ICONT2 Memory Mapping (continued)

Module	Offset in Region		Size
Reserved	0x0009 4000	0x0009 7FFF	16
ICONT2 – IMem	0x0009 8000	0x0009 FFFF	32
ECD3 – Mem	0x000A 0000	0x000A 7FFF	32
CALC3 – Mem	0x000A 8000	0x000A BFFF	16
Reserved	0x000A C000	0x000A FFFF	16
MC3 – Mem	0x000B 0000	0x000B 7FFF	32
IPE3 – Mem	0x000B 8000	0x000B 8FFF	4
Reserved	0x000B 9000	0x000C 0FFF	32
SMSET – Reg	0x000C 1000	0x000C 1FFF	4
SMSET – SWI	0x000C 2000	0x000C 27FF	2
Reserved	0x000C 2800	0x000C FFFF	54
DMA_IVA – Reg	0x000D 0000	0x000D 1FFF	8
ILF3 – Reg	0x000D 2000	0x000D 2FFF	4
Reserved	0x000D 3000	0x000D 3FFF	4
IME3 – Reg	0x000D 4000	0x000D 7FFF	16
CALC3 – Reg	0x000D 8000	0x000D 87FF	2
IPE3 – Reg	0x000D 8800	0x000D 8FFF	2
MC3 – Reg	0x000D 9000	0x000D 97FF	2
ECD3 – Reg	0x000D 9800	0x000D 9FFF	2
Reserved	0x000D A000	0x000D A3FF	1
SysControl	0x000D A400	0x000D A7FF	1
Mailbox	0x000D A800	0x000D ABFF	1
Reserved	0x000D AC00	0x000D FFFF	21
ICONT1 – SYNCBOX	0x000E 0000	0x000E 07FF	2
ICONT2 – SYNCBOX	0x000E 0800	0x000E 0FFF	2
ILF3 – SYNCBOX	0x000E 1000	0x000E 17FF	2
IME3 – SYNCBOX	0x000E 1800	0x000E 1FFF	2
CALC3 – SYNCBOX	0x000E 2000	0x000E 27FF	2
IPE3 – SYNCBOX	0x000E 2800	0x000E 2FFF	2
MC3 – SYNCBOX	0x000E 3000	0x000E 37FF	2
ECD3 – SYNCBOX	0x000E 3800	0x000E 3FFF	2
Reserved	0x000E 4000	0x000E FFFF	48
ICONT1 – Reg	0x000F 0000	0x000F 0FFF	4
ICONT2 – Reg (1)	0x000F 1000	0x000F 1FFF	4
Reserved	0x000F 2000	0x000F 2FFF	4
ICONT2 – Reg (2)	0x000F 3000	0x000F 3FFF	4
Reserved	0x000F 4000	0x000F FFFF	48

(1) ICONT2 private access to its own registers
(2) ICONT2 self-access to its own registers

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NOTE: Definitions of ICONT self-access and private access:

- Self-access: Direct access of ICONT to its own memory-mapped registers (MMRs) (reduced latency); that is, without using the IVA local interconnect. Internal ICONT configuration (CFG) registers are not visible. Only IRQ, DM, and SBH registers can be accessed.
- Private access: Access through IVA local interconnect. By default, all ICONT accesses described in Table 6-6 and Table 6-7 are private, except for corresponding self-access. In case of ICONT private access to its own registers, internal ICONT CFG registers are visible (on top of IRQ, DM, and SBH).

NOTE: Examples of start address:

- Buffered region: 0x0080 0000, 0x0090 0000, 0x00A0 0000, 0x0FF0 0000, 0x2000 0000, and so forth.
- Nonbuffered region: 0x1000 0000, 0x1010 0000, 0x1020 0000, 0x1FF0 0000, 0x3000 0000, and so forth.

Table 6-8 lists the IVA modules and memory addresses for the L3_MAIN access.

Table 6-8. L3_MAIN Interconnect Memory Mapping

Module	Begin Offset	L3_MAIN Interconnect Address		Size
		Begin	End	(KiB)
ICONT1 – DMem	0x0000 0000	0x5A00 0000	0x5A00 3FFF	16
Reserved	0x0000 4000	0x5A00 4000	0x5A00 7FFF	16
ICONT1 – IMem	0x0000 8000	0x5A00 8000	0x5A00 FFFF	32
ICONT2 – DMem	0x0001 0000	0x5A01 0000	0x5A01 3FFF	16
Reserved	0x0001 4000	0x5A01 4000	0x5A01 7FFF	16
ICONT2 – IMem	0x0001 8000	0x5A01 8000	0x5A01 FFFF	32
ECD3 – Mem	0x0002 0000	0x5A02 0000	0x5A02 7FFF	32
CALC3 – Mem	0x0002 8000	0x5A02 8000	0x5A02 BFFF	16
Reserved	0x0002 C000	0x5A02 C000	0x5A02 FFFF	16
MC3 – Mem	0x0003 0000	0x5A03 0000	0x5A03 7FFF	32
IPE3 – Mem	0x0003 8000	0x5A03 8000	0x5A03 8FFF	4
Reserved	0x0003 9000	0x5A03 9000	0x5A04 FFFF	92
DMA_IVA – Reg	0x0005 0000	0x5A05 0000	0x5A05 1FFF	8
ILF3 – Reg	0x0005 2000	0x5A05 2000	0x5A05 2FFF	4
Reserved	0x0005 3000	0x5A05 3000	0x5A05 3FFF	4
IME3 – Reg	0x0005 4000	0x5A05 4000	0x5A05 7FFF	16
CALC3 – Reg	0x0005 8000	0x5A05 8000	0x5A05 87FF	2
IPE3 – Reg	0x0005 8800	0x5A05 8800	0x5A05 8FFF	2
MC3 – Reg	0x0005 9000	0x5A05 9000	0x5A05 97FF	2
ECD3 – Reg	0x0005 9800	0x5A05 9800	0x5A05 9FFF	2
Reserved	0x0005 A000	0x5A05 A000	0x5A05 A3FF	1
SysControl	0x0005 A400	0x5A05 A400	0x5A05 A7FF	1
Mailbox	0x0005 A800	0x5A05 A800	0x5A05 ABFF	1
Reserved	0x0005 AC00	0x5A05 AC00	0x5A05 FFFF	21
ICONT1 – SYNCBOX	0x0006 0000	0x5A06 0000	0x5A06 07FF	2
ICONT2 – SYNCBOX	0x0006 0800	0x5A06 0800	0x5A06 0FFF	2
ILF3 – SYNCBOX	0x0006 1000	0x5A06 1000	0x5A06 17FF	2
IME3 – SYNCBOX	0x0006 1800	0x5A06 1800	0x5A06 1FFF	2
CALC3 – SYNCBOX	0x0006 2000	0x5A06 2000	0x5A06 27FF	2

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Table 6-8. L3_MAIN Interconnect Memory Mapping (continued)

Module	Begin Offset	L3_MAIN Interconnect Address		Size
		Begin	End	(KiB)
IPE3 – SYNCBOX	0x0006 2800	0x5A06 2800	0x5A06 2FFF	2
MC3 – SYNCBOX	0x0006 3000	0x5A06 3000	0x5A06 37FF	2
ECD3 – SYNCBOX	0x0006 3800	0x5A06 3800	0x5A06 3FFF	2
Reserved	0x0006 4000	0x5A06 4000	0x5A06 FFFF	48
ICONT1 – Reg	0x0007 0000	0x5A07 0000	0x5A07 0FFF	4
ICONT2 – Reg	0x0007 1000	0x5A07 1000	0x5A07 1FFF	4
Reserved	0x0007 2000	0x5A07 2000	0x5A07 FFFF	56

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6.1.3 IVA Register Manual

CAUTION

This section provides information about ICONT memory mapping (private access). This information represents only the address offsets from the start of relevant buffered (EXT_BUF) or nonbuffered (EXT_NBUF) regions. For more information, see Section 6.1.2.3, *IVA Memory Mapping*.

6.1.3.1 IVA Instance Summary

Table 6-9 shows the IVA instance summary.

Table 6-9. IVA Instance Summary

Module Name	Base Address (L3_MAIN Interconnect)	Base Address (ICONT Private Access)	Size
SYSCTRL	0x5A05 A400	0x000D A400	1 KiB

NOTE: Private access is an access through the IVA local interconnect without using the L3_MAIN interconnect.

6.1.3.2 SYSCTRL Registers

6.1.3.2.1 SYSCTRL Register Summary

Table 6-10 lists the mapping summary for the SYSCTRL registers.

CAUTION

SYSCTRL registers are limited to 32-bit access; 16- and 8-bit accesses are not allowed and can corrupt register content.

Table 6-10. SYSCTRL Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address (L3_MAIN Interconnect)	Physical Address (ICONT Private Access)
IVAHD_REVISION	R	32	0x0000 0000	0x5A05 A400	0x000D A400
IVAHD_HWINFO	R	32	0x0000 0004	0x5A05 A404	0x000D A404
IVAHD_SYSCONFIG	RW	32	0x0000 0010	0x5A05 A410	0x000D A410
RESERVED	RW	32	0x0000 0020	0x5A05 A420	0x000D A420
IVAHD_IRQSTATUS_RAW	RW	32	0x0000 0024	0x5A05 A424	0x000D A424
IVAHD_IRQSTATUS	RW	32	0x0000 0028	0x5A05 A428	0x000D A428
IVAHD_IRQENABLE_SET	RW	32	0x0000 002C	0x5A05 A42C	0x000D A42C
IVAHD_IRQENABLE_CLR	RW	32	0x0000 0030	0x5A05 A430	0x000D A430
IVAHD_SYNC_IRQSTATUS_RAW	RW	32	0x0000 0034	0x5A05 A434	0x000D A434
IVAHD_SYNC_IRQSTATUS	RW	32	0x0000 0038	0x5A05 A438	0x000D A438
IVAHD_SYNC_IRQENABLE_SET	RW	32	0x0000 003C	0x5A05 A43C	0x000D A43C
IVAHD_SYNC_IRQENABLE_CLR	RW	32	0x0000 0040	0x5A05 A440	0x000D A440
IVAHD_CLKCTRL	RW	32	0x0000 0050	0x5A05 A450	0x000D A450
IVAHD_CLKST	R	32	0x0000 0054	0x5A05 A454	0x000D A454

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Table 6-10. SYSCTRL Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address (L3_MAIN Interconnect)	Physical Address (ICONT Private Access)
IVAHD_STDBYST	R	32	0x0000 0058	0x5A05 A458	0x000D A458

6.1.3.2.2 SYSCTRL Register Description

Table 6-11. IVAHD_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5A05 A400 0x000D A400	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	IP revision identifier (X.Y.R). Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI Internal Data

Table 6-12. Register Call Summary for Register IVAHD_REVISION

IVA Overview
- SYSCTRL Register Summary: [0]

Table 6-13. IVAHD_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5A05 A404 0x000D A404	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Information about the IP module's hardware configuration.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECD3	MC3	IPE3	CALC3	IME3	ILF3	DMA_IVA	ICONT2	ICONT1	SL2BANK	SL2SIZE					

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	ECD3	ECD3 available 0: ECD3 not present 1: ECD3 present	R	1
13	MC3	MC3 available 0: MC3 not present 1: MC3 present	R	1
12	IPE3	IPE3 available 0: IPE3 not present 1: IPE3 present	R	1
11	CALC3	CALC3 available 0: CALC3 not present 1: CALC3 present	R	1

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Bits	Field Name	Description	Type	Reset
10	IME3	IME3 available 0: IME3 not present 1: IME3 present	R	1
9	ILF3	ILF3 available 0: ILF3 not present 1: ILF3 present	R	1
8	DMA_IVA	DMA_IVA available 0: DMA_IVA not present 1: DMA_IVA present	R	1
7	ICONT2	ICONT2 available 0: ICONT2 not present 1: ICONT2 present	R	1
6	ICONT1	ICONT1 available 0: ICONT1 not present 1: ICONT1 present	R	1
5:4	SL2BANK	Read 0x0: 1 memory bank Read 0x1: 2 memory bank Read 0x2: 4 memory bank Read 0x3: 8 memory bank	R	0x3
3:0	SL2SIZE	Size of SL2 memory Read 0x1: 16 KiB Read 0x2: 32 KiB Read 0x3: 48 KiB Read 0x4: 64 KiB Read 0x5: 96 KiB Read 0x6: 128 KiB Read 0x7: 160 KiB Read 0x8: 192 KiB Read 0x9: 224 KiB Read 0xA: 256 KiB Read 0xB: 320 KiB Read 0xC: 384 KiB Read 0xD: 448 KiB Read 0xE: 512 KiB	R	0xA

Table 6-14. Register Call Summary for Register IVAHD_HWINFO

IVA Overview

- SYSCTRL Register Summary: [0]

Table 6-15. IVAHD_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5A05 A410 0x000D A410	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Clock management configuration		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		IDLEMODE		RESERVED	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0 and 0x3: Reserved 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. IP module shall not generate (initiator-related) wakeup events.	RW	0x2
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0 and 0x3: Reserved 0x1: No-idle mode: local target never enters idle state. Backup mode, for debug only. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wakeup events.	RW	0x2
1:0	RESERVED	Reserved	R	0x0

Table 6-16. Register Call Summary for Register IVAHD_SYSCONFIG

IVA Overview
- IVA Power Management: [0] [1]
- SYSCTRL Register Summary: [2]

Table 6-17. IVAHD_IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x5A05 A424 0x000D A424	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SYSCTRL_CLKERR

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SYSCTRL_CLKERR	Settable raw status for Clock Programming Error event Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW	0

Table 6-18. Register Call Summary for Register IVAHD_IRQSTATUS_RAW

IVA Overview
- SYSCTRL Register Summary: [1]

Table 6-19. IVAHD_IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x5A05 A428 0x000D A428	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Per-event "enabled" interrupt status vector, line 0. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SYSCTRL_CLKERR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SYSCTRL_CLKERR	Clearable, enabled status for Clock Programming Error event Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW	0

Table 6-20. Register Call Summary for Register IVAHD_IRQSTATUS

IVA Overview
- SYSCTRL Register Summary: [3]

Table 6-21. IVAHD_IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x5A05 A42C 0x000D A42C	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

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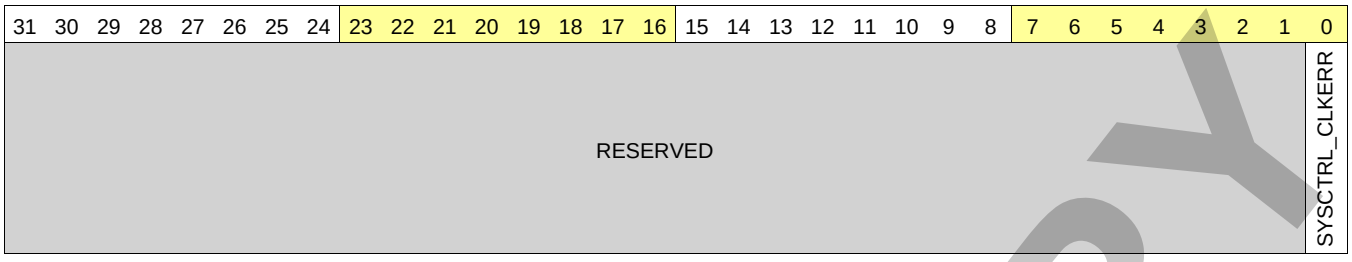


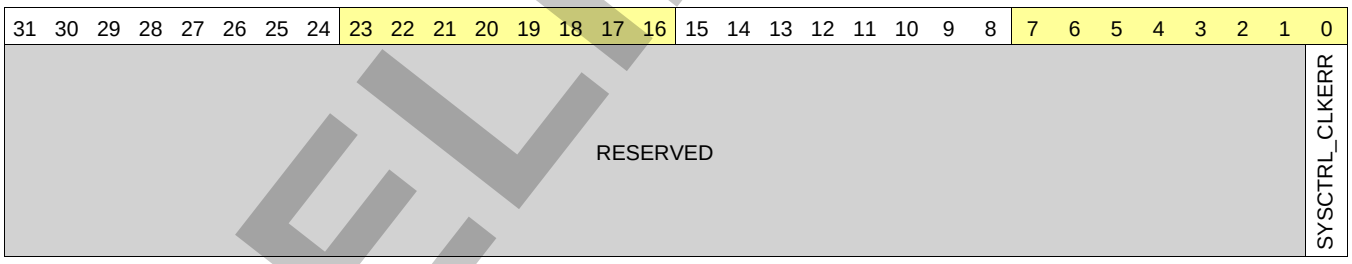
Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SYSCTRL_CLKERR	Clock Programing Error Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

Table 6-22. Register Call Summary for Register IVAHD_IRQENABLE_SET

IVA Overview
- SYSCTRL Register Summary: [3]

Table 6-23. IVAHD_IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x5A05 A430 0x000D A430	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SYSCTRL_CLKERR	Clock Programing Error Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0

Table 6-24. Register Call Summary for Register IVAHD_IRQENABLE_CLR

IVA Overview
- SYSCTRL Register Summary: [1]

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Table 6-25. IVAHD_SYNC_IRQSTATUS_RAW

Address Offset	0x0000 0034		
Physical Address	0x5A05 A434 0x000D A434	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SYNC_INPUT7_0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SYNC_INPUT7_0	Settable raw status for SYNC INPUT event. For each bit of the bit field: Read 0: No event pending Read 1: Event pending Write 0: No action Write 1: Set event (debug)	RW	0x00

Table 6-26. Register Call Summary for Register IVAHD_SYNC_IRQSTATUS_RAW

IVA Overview

- SYSCTRL Register Summary: [1]

Table 6-27. IVAHD_SYNC_IRQSTATUS

Address Offset	0x0000 0038		
Physical Address	0x5A05 A438 0x000D A438	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Per-event "enabled" interrupt status vector, line 0. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SYNC_INPUT7_0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SYNC_INPUT7_0	Clearable, enabled status for SYNC INPUT event. For each bit of the bit field: Read 0: No (enabled) event pending Read 1: Event pending Write 0: No action Write 1: Clear (raw) event	RW	0x00

Table 6-28. Register Call Summary for Register IVAHD_SYNC_IRQSTATUS

IVA Overview

- SYSCTRL Register Summary: [1]

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Table 6-29. IVAHD_SYNC_IRQENABLE_SET

Address Offset	0x0000 003C		
Physical Address	0x5A05 A43C 0x000D A43C	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SYNC_INPUT7_0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SYNC_INPUT7_0	Enable for interrupt event. For each bit of the bit field: Read 0: Interrupt disabled (masked) Read 1: Interrupt enabled Write 0: No action Write 1: Enable interrupt	RW	0x00

Table 6-30. Register Call Summary for Register IVAHD_SYNC_IRQENABLE_SET

IVA Overview

- SYSCTRL Register Summary: [1]

Table 6-31. IVAHD_SYNC_IRQENABLE_CLR

Address Offset	0x0000 0040		
Physical Address	0x5A05 A440 0x000D A440	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SYNC_INPUT7_0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SYNC_INPUT7_0	Enable for interrupt event. For each bit of the bitfiled: Read 0: Interrupt disabled (masked) Read 1: Interrupt enabled Write 0: No action Write 1: Disable interrupt	RW	0x00

Table 6-32. Register Call Summary for Register IVAHD_SYNC_IRQENABLE_CLR

IVA Overview

- SYSCTRL Register Summary: [1]

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Table 6-33. IVAHD_CLKCTRL

Address Offset	0x0000 0050		
Physical Address	0x5A05 A450 0x000D A450	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	IVA clock control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					SMSET	MSGIF	ECD3	MC3	IPE3	CALC3	ILF3	IME3	DMA_IVA	ICONT2	ICONT1

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10	SMSET	Clock control of SMSET 0: Exit idle state and start SMSET clock 1: Request SMSET to go to idle state and stop SMSET clock Note: Shutting down SMSET clock may hang system if software performs software instrumentation and/or access to its configuration port.	RW	0
9	MSGIF	Clock control of MSGIF 0: Exit idle state and start MSGIF clock 1: Request MSGIF to go to idle state and stop MSGIF clock	RW	0
8	ECD3	Clock control of ECD3 0: Exit idle state and start ECD3 clock 1: Request ECD3 to go to idle state and stop ECD3 clock	RW	0
7	MC3	Clock control of MC3 0: Exit idle state and start MC3 clock 1: Request MC3 to go to idle state and stop MC3 clock	RW	0
6	IPE3	Clock control of IPE3 0: Exit idle state and start IPE3 clock 1: Request IME3 to go to idle state and stop IPE3 clock	RW	0
5	CALC3	Clock control of CALC3 0: Exit idle state and start CALC3 clock 1: Request CALC3 to go to idle state and stop CALC3 clock	RW	0
4	ILF3	Clock control of ILF3 0: Exit idle state and start ILF3 clock 1: Request ILF3 to go to idle state and stop ILF3 clock	RW	0
3	IME3	Clock control of IME3 0: Exit idle state and start IME3 clock 1: Request IME3 to go to idle state and stop IME3 clock	RW	0
2	DMA_IVA	Clock control of DMA_IVA 0: Exit idle state and start DMA_IVA clock 1: Request DMA_IVA to go to idle state and stop DMA_IVA clock	RW	0
1	ICONT2	Clock control of ICONT2 0: Exit idle state and start ICONT2 clock 1: Request ICONT2 to go to idle state and stop ICONT2 clock	RW	0
0	ICONT1	Clock control of ICONT1 0: Exit idle state and start ICONT1 clock 1: Request ICONT1 to go to idle state and stop ICONT1 clock	RW	0

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Table 6-34. Register Call Summary for Register IVAHD_CLKCTRL

IVA Overview

- SYSCTRL Register Summary: [4]

Table 6-35. IVAHD_CLKST

Address Offset	0x0000 0054		
Physical Address	0x5A05 A454 0x000D A454	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	IVA clock status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					SMSET	MSGIF	ECD3	MC3	IPE3	CALC3	ILF3	IME3	DMA_IVA	ICONT2	ICONT1

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10	SMSET	Clock status of SMSET 1: SMSET clock is active 0: SMSET clock is idled	R	0
9	MSGIF	Clock status of MSGIF 1: MSGIF clock is active 0: MSGIF clock is idled	R	0
8	ECD3	Clock status of ECD3 1: ECD3 clock is active 0: ECD3 clock is idled	R	0
7	MC3	Clock status of MC3 1: MC3 clock is active 0: MC3 clock is idled	R	0
6	IPE3	Clock status of IPE3 1: IPE3 clock is active 0: IPE3 clock is idled	R	0
5	CALC3	Clock status of CALC3 1: CALC3 clock is active 0: CALC3 clock is idled	R	0
4	ILF3	Clock status of ILF3 1: ILF3 clock is active 0: ILF3 clock is idled	R	0
3	IME3	Clock status of IME3 1: IME3 clock is active 0: IME3 clock is idled	R	0
2	DMA_IVA	Clock status of DMA_IVA 1: DMA_IVA clock is active 0: DMA_IVA clock is idled	R	0
1	ICONT2	Clock status of ICONT2 1: ICONT2 clock is active 0: ICONT2 clock is idled	R	0
0	ICONT1	Clock status of ICONT1 1: ICONT1 clock is active 0: ICONT1 clock is idled	R	0

Table 6-36. Register Call Summary for Register IVAHD_CLKST

IVA Overview

- SYSCTRL Register Summary: [1]

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Table 6-37. IVAHD_STDBYST

Address Offset	0x0000 0058		
Physical Address	0x5A05 A458 0x000D A458	**Instance**	SYSCTRL_MAIN_L3 SYSCTRL_ICONT
Description	IVA STANDBY status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													DMA_IVA	ICONT2	ICONT1

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	DMA_IVA	DMA_IVA Standby status 0: module is not in Standby 1: module is in Standby	R	1
1	ICONT2	ICONT2 Standby status 0: module is not in Standby 1: module is in Standby	R	1
0	ICONT1	ICONT1 Standby status 0: module is not in Standby 1: module is in Standby	R	1

Table 6-38. Register Call Summary for Register IVAHD_STDBYST

IVA Overview

- SYSCTRL Register Summary: [2]

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Dual Cortex-M4 IPU Subsystem

This chapter describes the dual Cortex-M4 image processor unit (IPU) subsystem.

Topic **Page**

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7.2	**Dual Cortex-M4 IPU Subsystem Integration**	**1470**
7.3	**Dual Cortex-M4 IPU Subsystem Functional Description**	**1474**
7.4	**Dual Cortex-M4 IPU Subsystem Register Manual**	**1484**

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7.1 Dual Cortex-M4 IPU Subsystem Overview

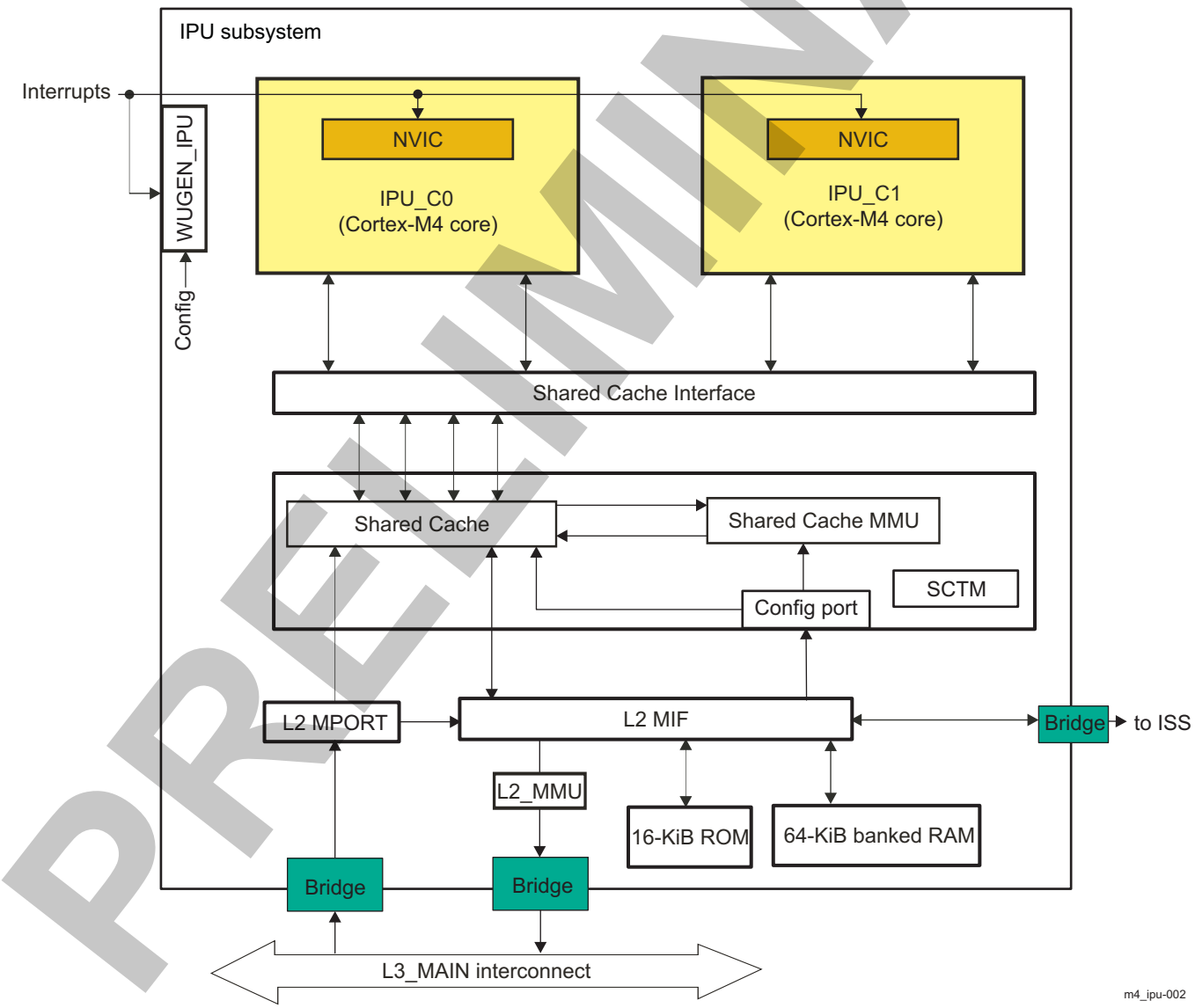
7.1.1 Introduction

The dual Cortex™-M4 image processor unit (IPU) subsystem is used primarily to configure and control the imaging subsystem (ISS), but it can also manage other tasks. It contains two ARM® Cortex-M4 processors (IPUC0 and IPU_C1) that share a common level 1 (L1) cache (called shared cache [SCACHE_IPU]). The integrated interrupt handling of the IPU subsystem allows it to function as an efficient control unit.

NOTE: The two Cortex-M4 cores are completely homogeneous to one another. Any task possible using one Cortex-M4 core is also possible using the other Cortex-M4 core. Both Cortex-M4 cores can be used to run RTOS and control ISP, SIMCOP, DSS, IVA, etc., as well as other tasks. It is software responsibility to distribute these tasks between each Cortex-M4 core for optimal performance.

Figure 7-1 is a high-level block diagram of the IPU subsystem.

Figure 7-1. IPU Subsystem Overview



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7.1.2 Features

The IPU subsystem integrates the following:

- Two ARM Cortex-M4 microprocessors (IPU_C0 and IPU_C1):
  - ARMv7-M and Thumb®-2 instruction set architecture (ISA)
  - ARMv6 SIMD and digital signal processor (DSP) extensions
  - Single-cycle MAC
  - Integrated nested vector interrupt controller (NVIC) (also called INTC_IPU)
  - Integrated bus matrix
  - Registers:
    - Thirteen general-purpose 32-bit registers
    - Link register (LR)
    - Program counter (PC)
    - Program status register, xPSR
    - Two banked SP registers
  - Integrated power management
  - Extensive debug capabilities
- Shared cache interface:
  - Instruction and data interface
  - Supports paralleled accesses
- Level 2 (L2) master interface (MIF) splitter for access to memory or configuration port
- Configuration port: Used for shared cache maintenance and shared cache memory management unit (SCACHE_MMU_IPU) configuration
- Shared cache:
  - 32 KiB divided into 16 banks
  - 4-way
  - Cache configuration lock/freeze/preload
  - Internal MMU:
    - 16-entry region-based address translation
    - Read/write control and access type control
    - Execute Never (XN) MMU protection policy
    - Little-endian format
- Subsystem counter timer module (SCTM)
- On-chip ROM (ROM_IPU) and banked RAM (RAM_IPU) memory
- Emulation/debug: Emulation feature embedded in Cortex-M4
- L2_MMU: 32 entries with table walking logic
- Wake-up generator (WUGEN_IPU): Generates wake-up request from external interrupts
- Power management:
  - Local power-management control: Configurable through the WUGEN_IPU registers.
  - Three sleep modes supported, controlled by the local power-management module.
  - IPU is clock-gated in all sleep modes.
  - INTC_IPU interrupt interface stays awake.

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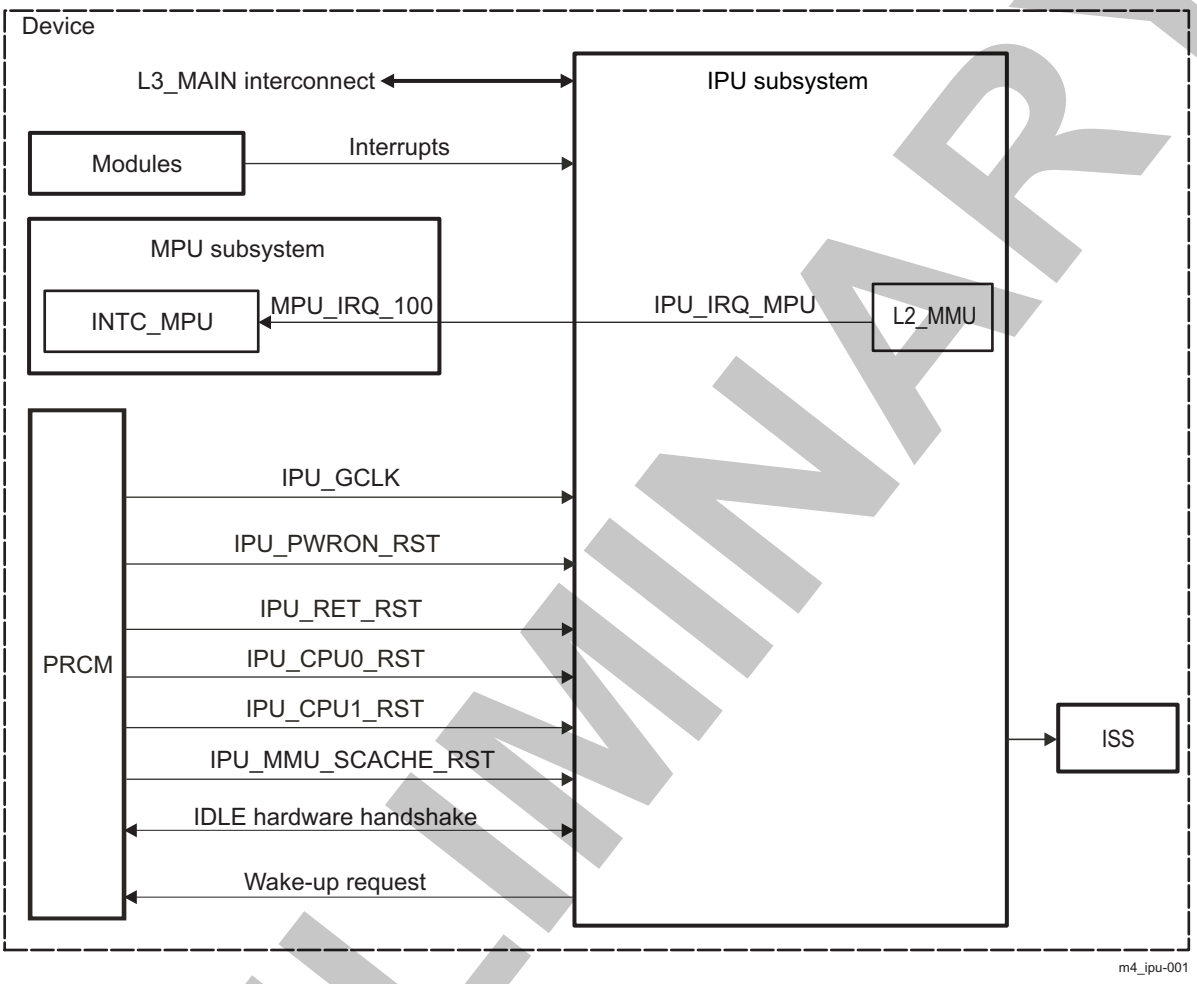
7.2 Dual Cortex-M4 IPU Subsystem Integration

Figure 7-2 shows the signals that interface with other modules.

Figure 7-2. IPU Subsystem Integration Overview



NOTE: Some debug, trace, and emulation features are implemented in the IPU subsystem. This chapter includes only the clock/reset inputs and power-management aspects for these features.

Table 7-1 through Table 7-3 summarize the integration of the module in the device.

Table 7-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
IPU	PD_CORE	L3_MAIN

Table 7-2. Hardware Requests

	Interrupt Requests			
Module Instance	Source Signal Name	Destination Signal Name	Destination	Description
L2_MMU	IPU_IRQ_MPU	MPU_IRQ_100	INTC_MPU	L2_MMU fault interrupt

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Table 7-3. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
IPU	IPU_GCLK	IPU_GCLK	PRCM module	Interface and functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
IPU	IPU_PWRON_RST	IPU_PWRON_RST	PRCM module	Power-on reset, used to reset the whole IPU subsystem
	IPU_RET_RST	IPU_RET_RST	PRCM module	Retention reset to few retention logic inside the SCACHE_IPU
	IPU_CPU0_RST	IPU_CPU0_RST	PRCM module	Reset signal to IPU_C0
	IPU_CPU1_RST	IPU_CPU1_RST	PRCM module	Reset signal to IPU_C1
	IPU_MMU_SCACHE_RST	IPU_MMU_SCACHE_RST	PRCM module	Reset signal to the SCACHE_IPU and the L2_MMU

For more information about clocks, resets, and power domains, see Chapter 3, *Power, Reset, and Clock Management*.

7.2.1 Dual Cortex-M4 IPU Subsystem Clock and Reset Distribution

7.2.1.1 Clock Distribution

The IPU subsystem receives only one clock, IPU_GCLK, which is divided by 2 (CORE_IPU_CLK) for each ARM Cortex-M4 processor, the ROM_IPU and RAM_IPU memory, and the L2_MMU. The SCACHE_IPU and the L2 MIF are directly clocked by the IPU_GCLK, without any division. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

Figure 7-3 shows the clocking scheme of the IPU subsystem.

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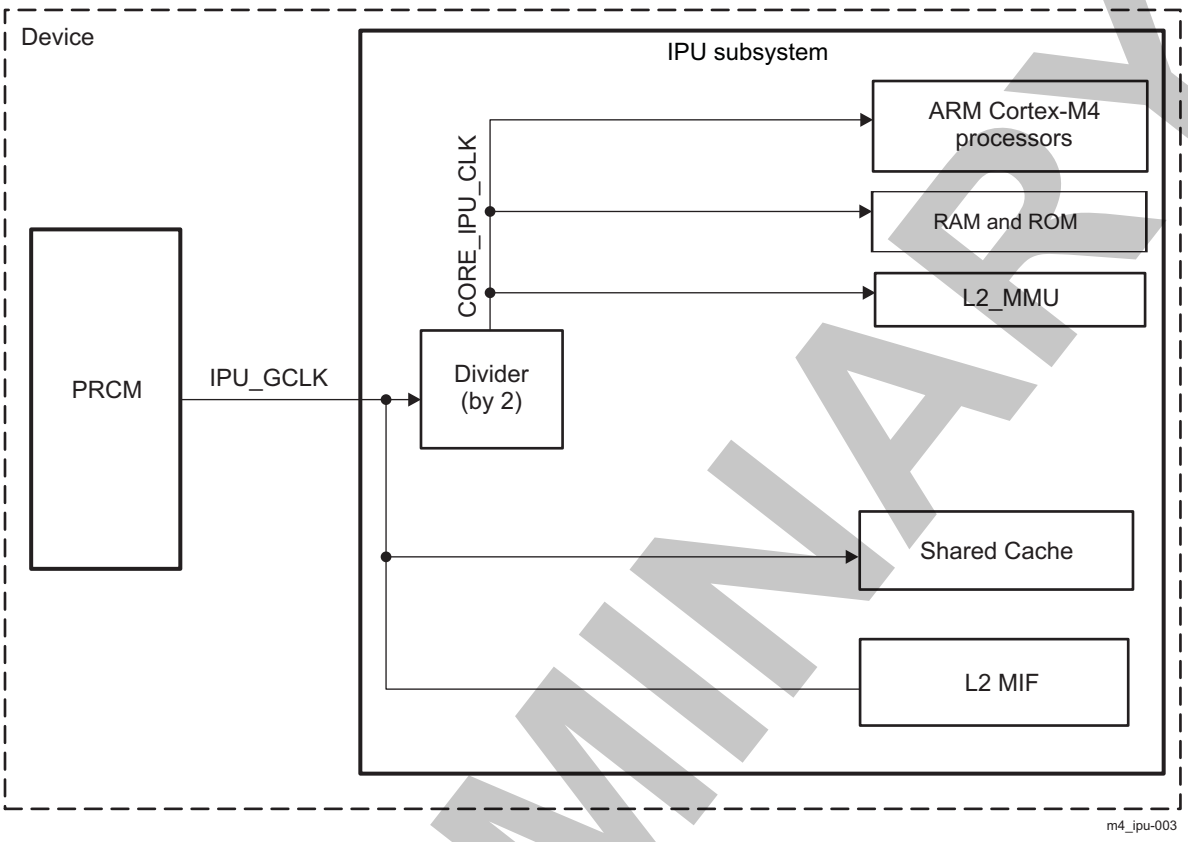
Figure 7-3. IPU Subsystem Clocking Scheme



7.2.1.2 Reset Distribution

Three reset signals controlled by the power, reset, and clock management (PRCM) module let the two ARM Cortex-M4 processors and the rest of the IPU subsystem be reset independently. These three reset signals are: IPU_CPU0_RST, IPU_CPU1_RST, and IPU_MMU_SCACHE_RST. The ARM Cortex-M4 processors must come out of reset one at a time:

- At IPU_CPU0_RST, IPU_C0 comes out of reset, but IPU_C1 is held in reset.
- IPU_C0 controls the reset for IPU_C1 (through the PRCM RM_IPU_RSTCTRL[1] RST2 bit).

Because IPU_C0 controls the reset for IPU_C1 (through the PRCM registers), the code running on IPU_C0 decides the mode of operation, whether it is:

- Mode 1: One ARM Cortex-M4 processor is running, and the other processor is held on reset.
- Mode 2: The two ARM Cortex-M4 processors are running.

This decision of which mode to use is driven by the use case. If the software partitioning and performance requirement for a use case requires two Cortex-M4 processors to run simultaneously, the user must go to mode 2. If IPU_C1 is not required for a particular use case, the user can remain in mode 1.

Figure 7-4 shows the reset scheme of the IPU subsystem.

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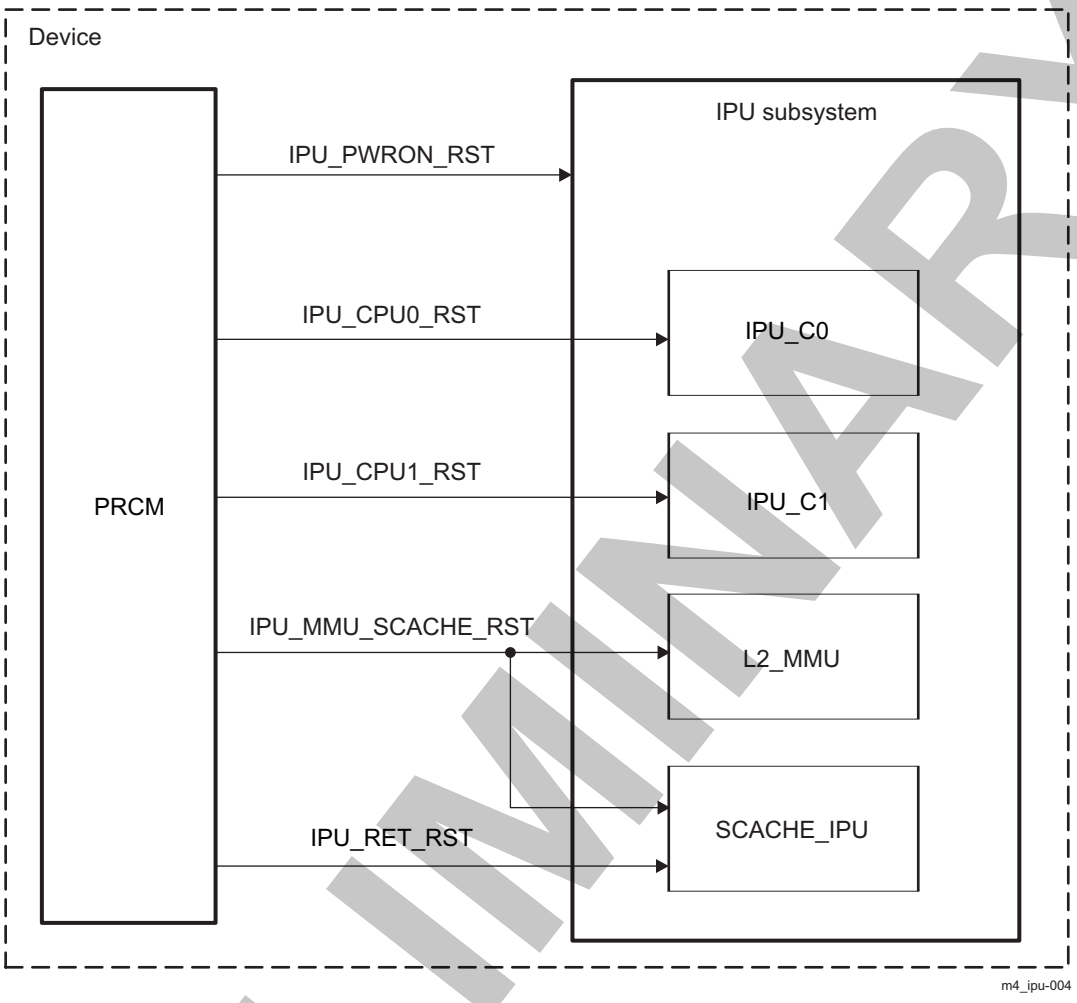
Figure 7-4. IPU Subsystem Reset Scheme



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7.3 Dual Cortex-M4 IPU Subsystem Functional Description

7.3.1 IPU Subsystem Block Diagram

The IPU subsystem integrates the following group of submodules:

- Two ARM Cortex-M4 processors: Two cores (r0p1 revision), IPU_C0 and IPU_C1. For a description of the ARM Cortex-M4 processor, see the *ARMCortex-M4 Technical Reference Manual*, available at infocenter.arm.com/help/index.jsp.
- Interrupt controller (INTC_IPU): To facilitate parallel processing, the interrupt mapping is the same for the two cores. Each Cortex-M4 processor receives the same interrupts, except for a few internal interrupts. Every IRQ line is shared between the two ARM processors. By properly configuring the INTC_IPU registers inside each ARM processor, it can be ensured that the shared IRQ is taken by only one of the ARM processors (for more information, see Chapter 17, *Interrupt Controllers*).
- SCACHE_IPU interface: The cache interface converts the data between the different protocols in the subsystem. Four ports are required to support the four buses from the ARM Cortex-M4 processors (two for each processor).The instruction and data connections from each ARM Cortex-M4 are multiplexed, but the ARM Cortex-M4 prevents conflicts on this connection. Default cache policies are provided through the sideband signals and are not used to access the cache. Cacheability is provided through the MMU inside the cache.
- SCACHE_IPU: Allows basic maintenance operations, which are performed through a dedicated interface: preload, lock, clean (write out dirty lines, but do not invalidate directly), and invalidate.
- SCACHE_MMU_IPU: Provides the multiple access cache with region-based address translation, read/write control, access type control, and multilevel cache maintenance. Access to the SCACHE_MMU_IPU is done only under privilege mode. The SCACHE_MMU_IPU can be programmed by the dual Cortex-A15 microprocessor unit (MPU) subsystem through the IPU subsystem slave port.
- SCTM: Embedded in the SCACHE_IPU
- Interconnect configuration port: Cache maintenance and MMU configuration are done through an interconnect slave port. Accesses must be performed to a noncacheable area that must be defined within the SCACHE_MMU_IPU. Interconnect accesses are generated from the L2 MIF.
- L2_MMU: Provides address translation for all the accesses done from the IPU subsystem to the level 3 (L3_MAIN) interconnect. The L2_MMU can be programmed by the MPU subsystem through the IPU subsystem slave port.
- L3_MAIN interconnect port: Allows access to the system memories and peripherals. For the address mapping of the modules in the IPU subsystem, see Chapter 2, *Memory Mapping*.
- On-chip ROM_IPU and banked RAM_IPU memory. The ROM_IPU memory is used for boot/initialization purposes. For more information about the initialization of the device, see Chapter 28, *Initialization*. The address range of the ROM_IPU memory is from 0x5500_0000 to 0x5500_3FFF. The address range of the on-chip banked RAM_IPU memory is from 0x5502_0000 to 0x5502_FFFF.

Figure 7-5 is a block diagram of the IPU subsystem.

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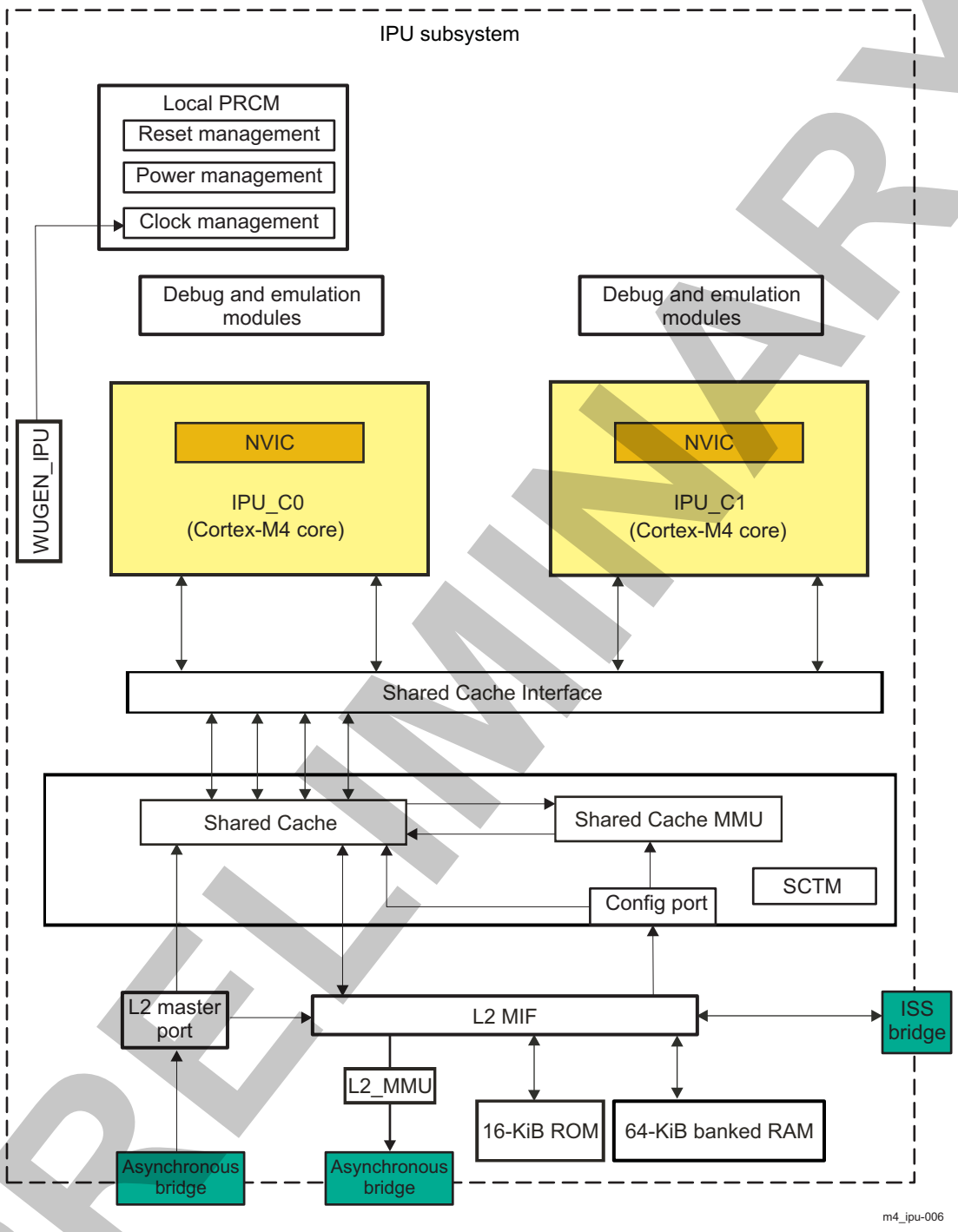
Figure 7-5. IPU Subsystem Block Diagram



7.3.2 Power Management

NOTE: For information about source clock gating and for a description of the sleep/wake-up transitions, see Module-Level Clock Management in Chapter 3, *Power, Reset, and Clock Management*.

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7.3.2.1 Local Power Management

The user can configure the local power management through the STANDBY_CORE_SYSCONFIG, IDLE_CORE_SYSCONFIG, and WUGEN_IRQ_EN registers. The user can:

- Configure the different standby modes (the default is smart wake-up standby mode) through the STANDBY_CORE_SYSCONFIG[1:0] STANDBYMODE bit field
- Configure the different idle modes (the default is smart wake-up idle mode) through the IDLE_CORE_SYSCONFIG[1:0] IDLEMODE bit field
- Control which interrupts will cause a wakeup by appropriately configuring the WUGEN_MEVT0 and WUGEN_MEVT1 registers (the default is ALL_MASKED)

The IPU subsystem provides three sleep modes:

- On mode: Sleep on exit (wait for the interrupt service routine [ISR] to complete)
- Sleep mode: Wait for interrupt to wake up the processor
- Deep-sleep mode: Long duration sleep; phase-locked loop (PLL) can be stopped

During sleep mode, the system clock can be stopped, but the free-running clock input must still be running to allow the processor to be wakened by an interrupt or an event. The sleep modes are invoked by wait for interrupt (WFI) or wait for event (WFE) instructions. The processor clock is automatically stopped, waiting for an interrupt or an event. Deep-sleep mode also stops the processor clock, but this can also be supported by the PRCM module. A combined signal is generated from the two Cortex-M4 processors in deep-sleep mode to initiate another power state and let the PRCM module handle the next power states. At this time, software must ensure that all SCACHE_IPU background operations (for example, maintenance) are complete.

Table 7-4 describes local clock gating.

Table 7-4. Local Clock Gating

Cortex-M4 CPU Mode	IPU_C1 On	IPU_C1 Sleep	IPU_C1 Deep Sleep
IPU_C0 On	On	Functional clock 2 stopped locally	Functional clock 2 stopped locally
IPU_C0 Sleep	Functional clock 1 stopped locally	Functional clock 1 and clock 2 stopped locally	Functional clock 1 and clock 2 stopped locally
IPU_C0 Deep Sleep	Functional clock 1 stopped locally	Functional clock 1 and clock 2 stopped locally	Standby request to power-management module

7.3.2.2 Power Domains

The IPU subsystem is divided into two power domains (PD_CORE and PD_WKUP), which are controlled by the PRCM module (see Section 7.3.2.3, *Voltage Domain*).

The PD_CORE power domain is the main power domain and includes all the IPU subsystem components (two ARM Cortex-M4 processors, SCACHE_IPU, ROM_IPU and RAM_IPU memories, and emulation\debug modules) except the WUGEN_IPU.

The PD_COREAON power domain is an always-on power domain. The PD_COREAON power domain contains the WUGEN_IPU, which generates a wake-up request from external interrupts. By this separate PD_COREAON power domain, the wake-up request can be generated even when the PD_CORE power domain is in OFF or RET state.

For information about the PD_CORE and PD_COREAON power domains, see Chapter 3, *Power, Reset, and Clock Management*.

7.3.2.3 Voltage Domain

The IPU subsystem is composed of two voltage domains. Each voltage domain can control individual voltage levels:

- VDD1: Cortex-M4 cores, SCACHE_IPU/MMU, WUGEN_IPU
- VDD_array: All memories array

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The PD_COREAON and PD_CORE power domains are in the same voltage domain, the CORE voltage domain (CORE_VD).

For information about the physical power domains, see Chapter 3, *Power, Reset, and Clock Management*.

7.3.2.4 Power States and Modes

Table 7-5 lists the different power modes and the expected states for each power domain.

Table 7-5. IPU Subsystem Power Modes

		Activity			Power Status	
	Functional Domain	Core		IPU subsystem	PD_DSP Power Domain	PD_WKUPAON Power Domain
	Modules included	IPU_C0	IPU_C1	WUGEN_IPU		
Power modes	Active	Active	Active	Active	ON	ON
	IPU_C0 idle	Idle	Active	Active	ON	ON
	IPU_C1 idle	Active	Idle	Active	ON	ON
	Core standby	Idle	Idle	Active	ON	ON
	Full idle	Idle	Idle	Idle	ON	ON
	CSWR	Idle	Idle	Idle	ON/LOWV	ON/LOWV
	OSWR	Idle	Idle	Idle	RET	ON
	Power off	Idle	Idle	Idle	OFF	OFF

Table 7-6 lists the power mode transitions in the IPU subsystem.

Table 7-6. Power Mode Transitions

	Active	IPU_C0 Idle	IPU_C1 Idle	Standby	Full-Idle	Retention	Power Off
Active		WFE/WFI instruction	WFE/WFI instruction				
IPU_C0 idle	Events/ interrupts			Deep sleep			
IPU_C1 idle	Events/ interrupts			Deep sleep			
Standby	Wake-up IRQ				L1/L2/ WUGEN_IPU functional domain idle		
Full idle	Wake-up IRQ			Wake-up (through interconnect)		PRCM module	PRCM module
CSWR/OSWR					PRCM module or wakeup		PRCM module
Power off					PRCM module or wakeup	PRCM module	

The different power modes and their features are:

- Active mode: All function domains are operable.
- IPU_C0 and IPU_C1 idle mode:
  - Only the CPU core is idled (when running WFE/WFI instructions).
  - Only one Cortex-M4 core can be in this mode. Interrupts or events can waken the core.
  - Can go into sleep or deep-sleep mode. Potentially, both cores can be in sleep mode.
  - When both cores are in deep-sleep mode, a standby request is sent to the PRCM module.
  - Software must ensure that all SCACHE_IPU background operations (for example, maintenance) are complete before the PRCM module asserts an IdleReq. For more information, see Chapter 5, *DSP*, Section 5.4.2.2.3.1, *Direct Maintenance of Caches*.

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- Core standby mode
  - Both cores in the CORE functional domain are in idle mode (an interrupt cannot wake up either of the cores).
  - The PRCM module must have acknowledged its acceptance by an MWait signal.
  - After this handshake, all power management is under the control of the PRCM module.
- Full-idle mode:
  - The IPU subsystem functional domain is also idled.
  - After coming to this mode, power states can be moved deeper.
- Retention mode:
  - The voltage of the logic supply is lowered to reduce static power consumption by leakage current. The logic power switch in the PD_CORE power domain is still closed (ON); thus, all logic states are retained.
  - L1 and/or L2 memories can go independently into retention depending on the settings done at the PRCM level.
- Power off mode:
  - The voltage source is shut down. The logic states, including the retention logic, are lost.
  - The WUGEN_IPU is not operating and only the PRCM module can trigger the IPU subsystem wakeup.
  - Reset must be applied to the IPU subsystem to restart the two ARM Cortex-M4 processors and the memory subsystem.

7.3.2.5 Wake-Up Generator (WUGEN_IPU)

The WUGEN_IPU in the IPU subsystem enables efficient power management. The WUGEN_IPU generates a wake-up signal to the PRCM module to enable the IPU subsystem to recover its functional clocks, which are gated by the PRCM module when at least one request is active. The WUGEN_IPU can be configured in standby mode or idle mode through the STANDBY_CORE_SYSCONFIG[1:0] STANDBYMODE and IDLE_CORE_SYSCONFIG[1:0] IDLEMODE bit fields.

7.3.2.5.1 WUGEN_IPU Main Features

The WUGEN_IPU allows:

- Gating of the IPU subsystem clock dynamically, thus reducing power consumption
- Simplifying of dependencies in the PRCM module

Figure 7-6 is an overview of the WUGEN_IPU.

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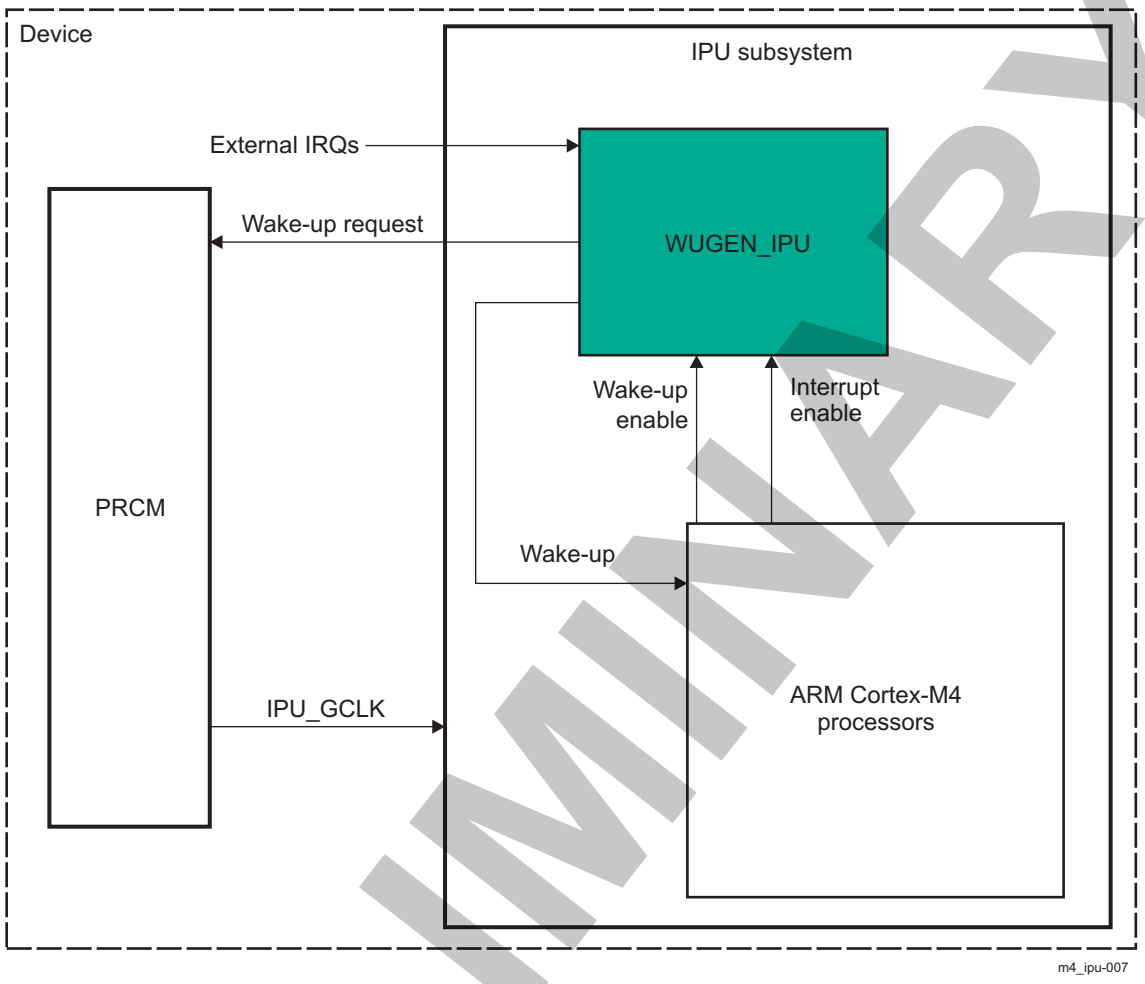
Figure 7-6. WUGEN_IPU Overview



The wake-up signal to the PRCM module requests the IPU subsystem functional clock (IPU_GCLK). The wake-up signal to the ARM Cortex-M4 processors indicates to them that at least one enabled request is active.

Two retention registers WUGEN_MEVT0 (for IPU_C0) and WUGEN_MEVT1 (for IPU_C1), enable the WUGEN_IPU requests to the INTC_IPUs.

7.3.3 SCACHE_IPU

Table 7-7 describes the SCACHE_IPU configuration in the IPU subsystem platform.

Table 7-7. SCACHE_IPU Configuration

Parameter	Value
Way	4
Size	32 KiB
Bank elements	32 bits
Bank number	16
Slave interface data size	32 bits
Master interface data size	64 bits
Line size	256 bits
MMU lookup	Included
Number of slaves	4

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Table 7-7. SCACHE_IPU Configuration (continued)

Parameter	Value
Number of masters	1
Number of fill/prefetch buffers	Four prefetch buffers
Slave types	SCACHE_IPU interface

SCACHE_IPU allows basic maintenance operations, which are performed through a dedicated interface:

1. Preload
2. Lock
3. Clean
4. Invalidate

Maintenance of the cache is performed between the start and end addresses. This allows for direct control of memory regions. All maintenance operations occur in the background and can generate an interrupt when they complete. Such operations are protected by software semaphore, because only one operation at a time can be performed. The maintenance operations can also be performed using MMU small entries.

The SCACHE_IPU is the same as the one in the DSP subsystem. For more information about the SCACHE_IPU, see DSP Subsystem chapter.

7.3.4 SCACHE_MMU_IPU

The MMU for the SCACHE_IPU provides the multi-access cache with region-based address translation, read/write control, access type control, and multilevel cache maintenance. Table 7-8 describes the MMU configuration in the IPU subsystem.

Table 7-8. SCACHE_MMU_IPU Configuration

Parameter	Values
Number of large pages	Four entries
Size of large pages	512 MiB or 32 MiB (configurable)
Number of medium pages	Two entries
Size of medium pages	256 KiB or 128 MiB (configurable)
Number of small pages	10 entries
Size of small pages	16 KiB or 4 KiB (configurable)
Number of patch pages	Not included
Size of line pages	256-bit
Number of comparison interfaces	4
Number of comparator sets	1
Write pipeline data comparison	Disabled
Number of SCACHE_IPU maintenance interfaces	3
Size of entry address	32-bit

The size of the pages is configurable in the SCACHE_MMU_IPU registers. The different MMU page sizes can be used to create smaller policies within a larger region. The SCACHE_MMU_IPU is the same as the one in the DSP subsystem. For more information, see Chapter 5, *DSP Subsystem*.

7.3.5 L2_MMU

An additional MMU provides address translation for the accesses done from the IPU subsystem to the L3_MAIN interconnect. The main characteristics of this MMU are:

- 32 entries
- Compatible with ARMv6 architecture MMU translation tables (protection bits not used)
- Page-based or access-based endianness conversion

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- Two-level descriptor hierarchy
- One intermediate page table
- Four page sizes (16 MiB, 1 MiB, 64 KiB, 4 KiB)
- Page table alignment on 128-byte boundary for ARM11® compatibility

The configuration of the MMU can be done from one of the Cortex-M4 cores or from the L3_MAIN interconnect slave port. The accesses done to configure the MMU cannot be part of a burst access.

For more information about the L2_MMU, see Memory Management Units chapter.

7.3.5.1 L2_MMU Behavior on Page-Fault in IPU Subsystem

Table 7-9. L2_MMU Behavior on Page-Fault

Application		Debug	
Table-Walker Enabled	**Table-Walker Disabled**	**Table-Walker Enabled**	**Table-Walker Disabled**
Use Table-Walker to find translation. Update TLB cache if successful, set TRANSLATIONFAULT bit and interrupt if not. The following bits are used for the purpose: MMU_IRQENABLE[1] TRANSLATIONFAULT and MMU_IRQSTATUS[1] TRANSLATIONFAULT.	Set TLBMISS bit and interrupt and stall. The following registers are used for the purpose: MMU_IRQENABLE[0] TLBMISS and MMU_IRQSTATUS[0] TLBMISS.	Use Table-Walker to find translation. Update TLB cache if successful (only if the MMU_CNTL[3] EMUTLBUPDATE bit is set), generate in-band bus error if not.	Set EMUMISS bit and interrupt and stall. The following bits are used for the purpose: MMU_IRQENABLE[2] EMUMISS and MMU_IRQSTATUS[2] EMUMISS.

The MMU fault interrupt line is connected to both Cortex-M4 cores and is also propagated outside of the IPU subsystem and connected to the Cortex-A15 MPU (MA_IRQ_100). The Cortex-A15 MPU receives the MMU fault and must clean up the fault to resume the execution of the code (or reset IPU subsystem). It is not possible for one of the Cortex-M4 CPUs to clean up the fault caused by the other Cortex-M4 CPU. This is because both the slave port of the L2_MMU (which is stalled) and the configuration port of L2_MMU are connected (through a splitter) to the same SCACHE_IPU master port.

The default behavior of the L2_MMU previously described can be overridden by setting the MMU_GP_REG[0] BUS_ERR_BACK_EN bit to 1. Once this bit is set, all MMU faults (including TLB miss) return a bus error to the IPU subsystem (interrupt event XLATE_MMU_FAULT). This allows the end user to quickly establish the cause of the MMU fault by having appropriate code in the ISR.

7.3.6 Interprocessor Communication (IPC)

7.3.6.1 Use of WFE and SEV

The IPU subsystem provides a multiprocessor communication interface for synchronizing tasks. The ARM processors have one output signal, TXEV (transmit event), for sending events and one input signal, RXEV (receive event), for receiving events. Figure 7-7 shows how TXEV and RXEV are connected in the IPU subsystem.

When a WFE instruction is executed, the processor enters into sleep mode waiting for an event and continues instruction execution when an external event is received. With an SEV (send event) instruction, one processor can wake up the other processor, which is in sleep mode.

The WFE and SEV instructions can help reduce the number of iterations around a lock acquire loop (a spinlock), and thereby reduce power consumption. The basic mechanism involves an observer that is in a spinlock executing a WFE instruction, which suspends execution on that observer until an asynchronous exception or an explicit event (sent by an observer using the SEV instruction) is seen by that observer. The observer that holds the lock uses the SEV instruction to send an event after a lock is released.

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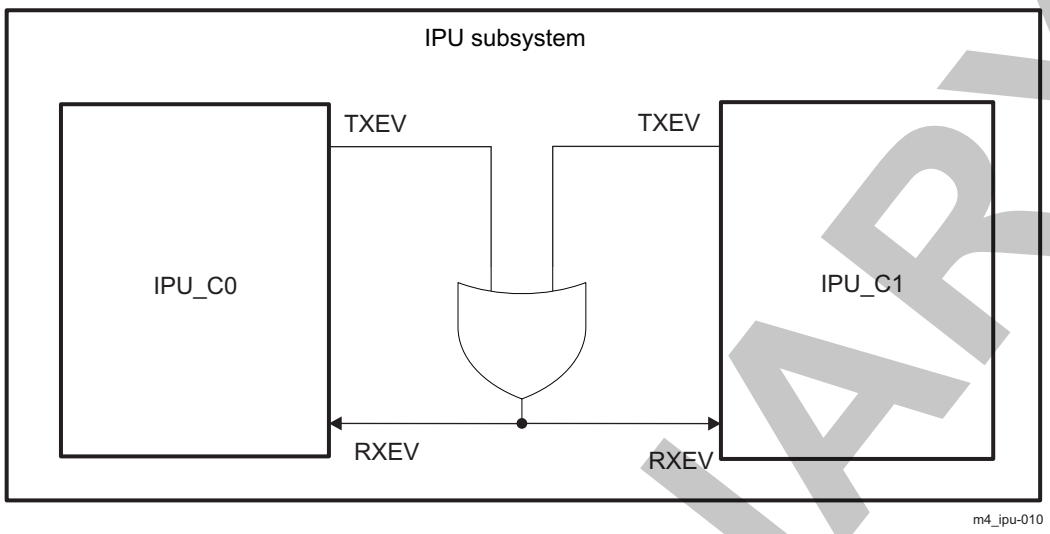
Figure 7-7. Event Communication Connection in IPU Subsystem



7.3.6.2 Use of Interrupt for IPC

Each Cortex-M4 core can interrupt the other Cortex-M4 core by setting up an interrupt register (CORTEXM4_CTRL_REG). Because the priority level for that interrupt can be defined, it is possible to choose the task level at which the interrupt will run. For example, if IPU_C0 was active and IPU_C1 was idle (WFI state), when IPU_C0 completes its task it sets the bit for IPU_C1 in the control register (CORTEXM4_CTRL_REG[16] INT_CORTEX_2) and goes into sleep mode. IPU_C1 wakes up seeing this interrupt, and starts running its task. After the completion of its task, IPU_C1 sets the interrupt for IPU_C0 (CORTEXM4_CTRL_REG[0] INT_CORTEX_1), and then goes into WFI state. This kind of handshake ensures that if IPU_C0 and IPU_C1 are accessing the same resources (memory, registers etc.), only one of the CPUs at a time is active.

7.3.6.3 Use of the Bit-Band Feature for Semaphore Operations

The two Cortex-M4 cores share the same memory system, and it is possible to use the bit-band feature to carry semaphore operations. Because the bit-band alias writes are locked read-modify-write transfers, provided that all tasks changed only the lock bit representing themselves, the lock bits of other tasks are not lost, even if two tasks try to write to the same memory location at the same time.

Each Cortex-M4 core supports two bit-band regions.

Bit-band 1 applies to the virtual address space 0x2000 0000–0x200F FFFF (1 MiB). This virtual address space can be mapped to any physical address and bit-banding will apply to that region. It is recommended that the user map the L2 RAM_IPU (64 KiB) to this virtual space and use it only for bit-banding operations. If required, the user can define other available small and medium pages over and above the L2 RAM_IPU virtual space and further extend the use of the bit-band feature.

Bit-band 2 applies to the virtual address space 0x4000 0000–0x400F FFFF (1 MiB). The first 16 KiB of this space (0x4000 0000–0x4000 3FFF) are already reserved for small (one page) pages and cannot be remapped by software. The bit-band alias that corresponds to this 16-KiB region (0x4200 0000–0x4207 FFFF) must also be treated as reserved and no access should be made. The rest of bit-band 2 can be used by appropriately defining the available small and medium pages. In this device, because it is likely that during normal AMMU programming all of L3_MAIN is mapped to this region, it is highly recommended that the user use only bit-band 1 for all purposes and bit-band 2 only if it is necessary.

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7.3.6.4 Private Memory Space

Each ARM Cortex-M4 processor has its own memory space, inaccessible by the other processor. In the private memory space are the INTC_IPUs and RW table registers: CORTEXM4_RW_PID1 and CORTEXM4_RW_PID2. CORTEXM4_RW_PID1 and CORTEXM4_RW_PID2 are accessible only by the respective Cortex-M4 cores (CORTEXM4_RW_PID1 is accessible only by IPU_C0, while CORTEXM4_RW_PID2 is accessible only by IPU_C1) . These registers are not accessible from the Cortex-A15 MPU. Because they are not shared, they do not require the bit-band feature (semaphore) to read and write to them.

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7.4 Dual Cortex-M4 IPU Subsystem Register Manual

7.4.1 IPU Subsystem Instance Summary

Table 7-10 summarizes the IPU subsystem instances.

Table 7-10. IPU subsystem Instance Summary

Module Name	Base Address	Size
SCACHE_CFG_IPU	0x5508 0000	4 KiB
SCACHE_SCTM_IPU	0x5508 0400	4 KiB
SCACHE_MMU_IPU	0x5508 0800	4 KiB
WUGEN_IPU	0x5508 1000	4 KiB
IPU_L2_MMU	0x5508 2000	4 KiB
INTC_IPU_C0(1)	0xE000 E000	4 KiB
INTC_IPU_C1(2)	0xE000 E000	4 KiB
IPU_RW_TABLE(3)	0xE00F E000	4 KiB

(1) Private memory space for IPU_C0
(2) Private memory space for IPU_C1
(3) Private memory space for each CPU

7.4.2 SCACHE_CFG_IPU Registers

For information about the SCACHE_CFG_IPU registers and their description, see DSP Subsystem chapter.

7.4.3 SCACHE_SCTM_IPU Registers

For information about the SCACHE_SCTM_IPU registers and their description, see DSP Subsystem chapter.

The SCTM registers in the IPU subsystem differ from the registers listed in Chapter 5, *DSP Subsystem*, in the following ways:

- Counters with indexes from i = 2 to 5 can be chained and shadowing is enabled.
- The reset value of the SCACHE_SCTM_CTCR_WOT_j[7] CHNSDW bit is 1.
- The option to write 1 in the SCACHE_SCTM_CTCR_WOT_j[4] CHAIN bit is not reserved and when the bit is write 1, the counter is chained.

7.4.4 SCACHE_MMU_IPU Registers

For information about the SCACHE_MMU_IPU registers and their description, see DSP Subsystem chapter.

The SCACHE_MMU_IPU in the IPU subsystem has four large pages, two medium pages, and ten small pages. Because of the different page sizes, there are differences with the registers described in - Chapter 5, *DSP Subsystem*, in the enumerated indexes below the register mapping, which are the following: (i = 0 to 3), (j = 0 to 1), (k = 0 to 9). There are also differences in the reset value of the following registers:

- SCACHE_MMU_SMALL_ADDR_0 with reset value 0x00000000
- SCACHE_MMU_SMALL_ADDR_1 with reset value 0x40000000
- SCACHE_MMU_SMALL_POLICY_k with reset value 0x0000000 (k = 0 to 9)
- SCACHE_MMU_SMALL_XLTE_0 with reset value 0x55020000
- SCACHE_MMU_SMALL_XLTE_1 with reset value 0x55080000
- SCACHE_MMU_SMALL_XLTE_k with reset value 0x00000000 (k = 2 to 9)

The page sizes for the 16 entries are:

- Large pages (four): The page sizes supported are 32 MiB and 512 MiB.

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- Medium pages (two): The page sizes supported are 128 KiB and 256 KiB.
- Small pages (ten): The page sizes supported are 4 KiB and 16 KiB.

7.4.5 IPU_L2_MMU Registers

For information about the IPU_L2_MMU registers and their description, see Memory Management Units chapter.

7.4.6 INTC_IPU_C0/1 Registers

For information about the INTC_IPU_C0/1 (NVICs) registers and their description, see the *ARM Cortex-M4 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

7.4.7 WUGEN_IPU Registers

7.4.7.1 WUGEN_IPU Register Summary

Table 7-11 summarizes the WUGEN_IPU register mapping.

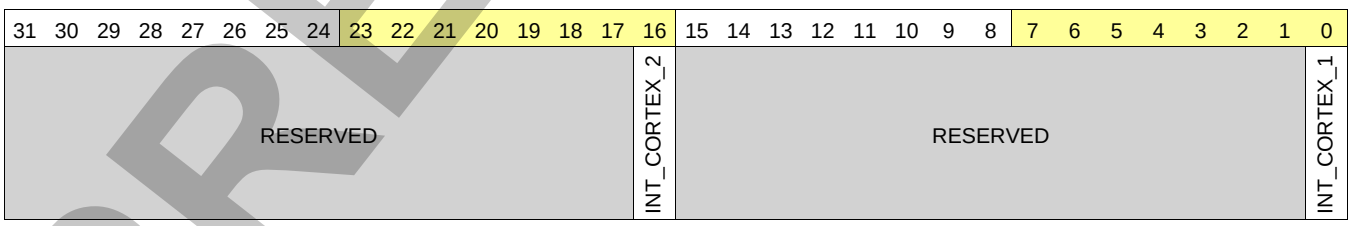
Table 7-11. WUGEN_IPU Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	IPU Base Address
CORTEXM4_CTRL_REG	RW	32	0x0000 0000	0x5508 1000
STANDBY_CORE_SYSCONFIG	RW	32	0x0000 0004	0x5508 1004
IDLE_CORE_SYSCONFIG	RW	32	0x0000 0008	0x5508 1008
WUGEN_MEVT0	RW	32	0x0000 000C	0x5508 100C
WUGEN_MEVT1	RW	32	0x0000 0010	0x5508 1010
RESERVED	R	32	0x0000 0014	0x5508 1014

7.4.7.2 WUGEN_IPU Register Description

Table 7-12. CORTEXM4_CTRL_REG

Address Offset	0x0000 0000		
Physical Address	0x5508 1000	**Instance**	WUGEN_IPU
Description	The register is used by one CPU to interrupt the other, thus used as a handshake between the two CPUs 0x0: Interrupt is cleared; 0x1: Interrupt is set.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:17	RESERVED		RW	0x0000 0000
16	INT_CORTEX_2	Interrupt to IPU_C1	RW	0
15:1	RESERVED		RW	0x0000 0000
0	INT_CORTEX_1	Interrupt to IPU_C0	RW	0

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Table 7-13. Register Call Summary for Register CORTEXM4_CTRL_REG

Dual Cortex-M4 IPU Subsystem Functional Description • Use of Interrupt for IPC: [0] [1] [2]
Dual Cortex-M4 IPU Subsystem Register Manual • WUGEN_IPU Register Summary: [3]

Table 7-14. STANDBY_CORE_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x5508 1004	**Instance**	WUGEN_IPU
Description	Standby protocol		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STANDBYMODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		RW	0x0000 0000
1:0	STANDBYMODE	0x0: Force-standby mode 0x1: No-standby mode 0x2: Smart-standby mode 0x3: Smart-standby wake-up mode – normal mode to be used	RW	0x3

Table 7-15. Register Call Summary for Register STANDBY_CORE_SYSCONFIG

Dual Cortex-M4 IPU Subsystem Functional Description • Local Power Management: [0] [1] • Wake-Up Generator (WUGEN_IPU): [2]
Dual Cortex-M4 IPU Subsystem Register Manual • WUGEN_IPU Register Summary: [3]

Table 7-16. IDLE_CORE_SYSCONFIG

Address Offset	0x0000 0008		
Physical Address	0x5508 1008	**Instance**	WUGEN_IPU
Description	Idle protocol		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														IDLEMODE	

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		RW	0x0000 0000
1:0	IDLEMODE	0x0: Force-idle mode 0x1: No-idle mode 0x2: Smart-idle mode 0x3: Smart-idle wake-up mode – normal mode to be used	RW	0x3

Table 7-17. Register Call Summary for Register IDLE_CORE_SYSCONFIG

Dual Cortex-M4 IPU Subsystem Functional Description • Local Power Management: [0] [1] • Wake-Up Generator (WUGEN_IPU): [2]
Dual Cortex-M4 IPU Subsystem Register Manual • WUGEN_IPU Register Summary: [3]

Table 7-18. WUGEN_MEVT0

Address Offset	0x0000 000C		
Physical Address	0x5508 100C	**Instance**	WUGEN_IPU
Description	This register contains the interrupt mask (LSB) wake-up enable bit per interrupt request: 0x0: Interrupt is disabled; 0x1: Interrupt is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQ31	RESERVED	MIRQ29	MIRQ28	MIRQ27	MIRQ26	MIRQ25	MIRQ24	MIRQ23	MIRQ22	MIRQ21	MIRQ20	MIRQ19	MIRQ18	MIRQ17	MIRQ16	MIRQ15	MIRQ14	MIRQ13	MIRQ12	MIRQ11	MIRQ10	MIRQ9	MIRQ8	MIRQ7	RESERVED							

Bits	Field Name	Description	Type	Reset
31	MIRQ31	Interrupt Mask bit 31	RW	0
30	RESERVED	Reserved	R	0
29	MIRQ29	Interrupt Mask bit 29	RW	0
28	MIRQ28	Interrupt Mask bit 28	RW	0
27	MIRQ27	Interrupt Mask bit 27	RW	0
26	MIRQ26	Interrupt Mask bit 26	RW	0
25	MIRQ25	Interrupt Mask bit 25	RW	0
24	MIRQ24	Interrupt Mask bit 24	RW	0
23	MIRQ23	Interrupt Mask bit 23	RW	0
22	MIRQ22	Interrupt Mask bit 22	RW	0
21	MIRQ21	Interrupt Mask bit 21	RW	0
20	MIRQ20	Interrupt Mask bit 20	RW	0
19	MIRQ19	Interrupt Mask bit 19	RW	0
18	MIRQ18	Interrupt Mask bit 18	RW	0
17	MIRQ17	Interrupt Mask bit 17	RW	0
16	MIRQ16	Interrupt Mask bit 16	RW	0
15	MIRQ15	Interrupt Mask bit 15	RW	0
14	MIRQ14	Interrupt Mask bit 14	RW	0
13	MIRQ13	Interrupt Mask bit 13	RW	0
12	MIRQ12	Interrupt Mask bit 12	RW	0
11	MIRQ11	Interrupt Mask bit 11	RW	0
10	MIRQ10	Interrupt Mask bit 10	RW	0

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Bits	Field Name	Description	Type	Reset
9	MIRQ9	Interrupt Mask bit 9	RW	0
8	MIRQ8	Interrupt Mask bit 8	RW	0
7	MIRQ7	Interrupt Mask bit 7	RW	0
6:0	RESERVED	Reserved	R	0

Table 7-19. Register Call Summary for Register WUGEN_MEVT0

Dual Cortex-M4 IPU Subsystem Functional Description

- Local Power Management: [0]
- Wake-Up Generator (WUGEN_IPU): [1]

Dual Cortex-M4 IPU Subsystem Register Manual

- WUGEN_IPU Register Summary: [2]

Table 7-20. WUGEN_MEVT1

Address Offset	0x0000 0010		
Physical Address	0x5508 1010	**Instance**	WUGEN_IPU
Description	This register contains the interrupt mask (MSB) wake-up enable bit per interrupt request: 0x0: Interrupt is disabled; 0x1: Interrupt is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIRQ63	MIRQ62	MIRQ61	MIRQ60	MIRQ59	MIRQ58	MIRQ57	MIRQ56	RESERVED	MIRQ54	MIRQ53	MIRQ52	MIRQ51	MIRQ50	RESERVED	MIRQ48	MIRQ47	MIRQ46	RESERVED			MIRQ42	MIRQ41	MIRQ40	MIRQ39	MIRQ38	MIRQ37	MIRQ36	MIRQ35	MIRQ34	MIRQ33	RESERVED

Bits	Field Name	Description	Type	Reset
31	MIRQ63	Interrupt Mask bit 63	RW	0
30	MIRQ62	Interrupt Mask bit 62	RW	0
29	MIRQ61	Interrupt Mask bit 61	RW	0
28	MIRQ60	Interrupt Mask bit 60	RW	0
27	MIRQ59	Interrupt Mask bit 59	RW	0
26	MIRQ58	Interrupt Mask bit 58	RW	0
25	MIRQ57	Interrupt Mask bit 57	RW	0
24	MIRQ56	Interrupt Mask bit 56	RW	0
23	RESERVED	Reserved	R	0
22	MIRQ54	Interrupt Mask bit 54	RW	0
21	MIRQ53	Interrupt Mask bit 53	RW	0
20	MIRQ52	Interrupt Mask bit 52	RW	0
19	MIRQ51	Interrupt Mask bit 51	RW	0
18	MIRQ50	Interrupt Mask bit 50	RW	0
17	RESERVED	Reserved	R	0
16	MIRQ48	Interrupt Mask bit 48	RW	0
15	MIRQ47	Interrupt Mask bit 47	RW	0
14	MIRQ46	Interrupt Mask bit 46	RW	0
13:11	RESERVED	Reserved	R	0
10	MIRQ42	Interrupt Mask bit 42	RW	0
9	MIRQ41	Interrupt Mask bit 41	RW	0
8	MIRQ40	Interrupt Mask bit 40	RW	0
7	MIRQ39	Interrupt Mask bit 39	RW	0

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Bits	Field Name	Description	Type	Reset
6	MIRQ38	Interrupt Mask bit 38	RW	0
5	MIRQ37	Interrupt Mask bit 37	RW	0
4	MIRQ36	Interrupt Mask bit 36	RW	0
3	MIRQ35	Interrupt Mask bit 35	RW	0
2	MIRQ34	Interrupt Mask bit 34	RW	0
1	MIRQ33	Interrupt Mask bit 33	RW	0
0	RESERVED	Reserved	R	0

Table 7-21. Register Call Summary for Register WUGEN_MEVT1

Dual Cortex-M4 IPU Subsystem Functional Description • Local Power Management: [0] • Wake-Up Generator (WUGEN_IPU): [1]
Dual Cortex-M4 IPU Subsystem Register Manual • WUGEN_IPU Register Summary: [2]

7.4.8 IPU_RW_TABLE Registers

7.4.8.1 IPU_RW_TABLE Register Summary

Table 7-22. IPU_RW_TABLE Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	IPU Base Address
CORTEXM4_RW_PID1	RW	32	0x0000 0000	0xE00F E000
CORTEXM4_RW_PID2	RW	32	0x0000 0004	0xE00F E004
RESERVED	R	32	0x0000 0008	0xE00F E008

7.4.8.2 IPU_RW_TABLE Register Description

Table 7-23. CORTEXM4_RW_PID1

Address Offset	0x0000 0000		
Physical Address	0xE00F E000	**Instance**	IPU_RW_TABLE
Description	Peripheral Identification register– allows the user software to differentiate between the two ARM Cortex-M4 processors (two CPUs). The same piece of code running on the two CPUs can result in different execution (for example, branch to different location) depending on the address stored in the register. The address is stored by the BIOS code. The register cannot be accessed when the BIOS code is running (used).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASEADD1																															

Bits	Field Name	Description	Type	Reset
31:0	BASEADD1	ROM_IPU memory address	RW	0x0000 0000

Table 7-24. Register Call Summary for Register CORTEXM4_RW_PID1

Dual Cortex-M4 IPU Subsystem Functional Description • Private Memory Space: [0] [1] [2]
Dual Cortex-M4 IPU Subsystem Register Manual • IPU_RW_TABLE Register Summary: [3]

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Table 7-25. CORTEXM4_RW_PID2

Address Offset	0x0000 0004		
Physical Address	0xE00F E004	**Instance**	IPU_RW_TABLE
Description	Peripheral Identification register – allows the user software to differentiate between the two ARM Cortex-M4 processors (two CPUs). The same piece of code running on the two CPUs can result in different execution (for example, branch to different location) depending on the address stored in the register. The address is stored by the BIOS code. The register cannot be accessed when the BIOS code is running (used).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASEADD2																															

Bits	Field Name	Description	Type	Reset
31:0	BASEADD2	ROM_IPU memory address	RW	0x0000 0000

Table 7-26. Register Call Summary for Register CORTEXM4_RW_PID2

Dual Cortex-M4 IPU Subsystem Functional Description

- Private Memory Space: [0] [1] [2]

Dual Cortex-M4 IPU Subsystem Register Manual

- IPU_RW_TABLE Register Summary: [3]

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Imaging Subsystem

This chapter gives a top-level overview of the imaging subsystem (ISS) in the device.

NOTE: This chapter gives information about all modules and features in the high-tier device. For power-management saving consideration, ensure that power domains of unavailable features and modules are switched off and clocks are cut off.

For the availability of device modules, see , *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

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8.2 ISS Interfaces 1534
8.3 ISS ISP 1866
8.4 ISS Still Image Coprocessor 2314

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8.1 ISS Overview

The imaging subsystem (ISS) deals with the processing of the pixel data coming from an external image sensor, data from memory (image format encoding and decoding can be done to and from memory), or data from SL2 in IVA-HD for hardware encoding. With its subparts, such as interfaces and interconnects, image signal processor (ISP), and still image coprocessor (SIMCOP), the ISS is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture. Figure 8-1 shows an overview of the ISS.

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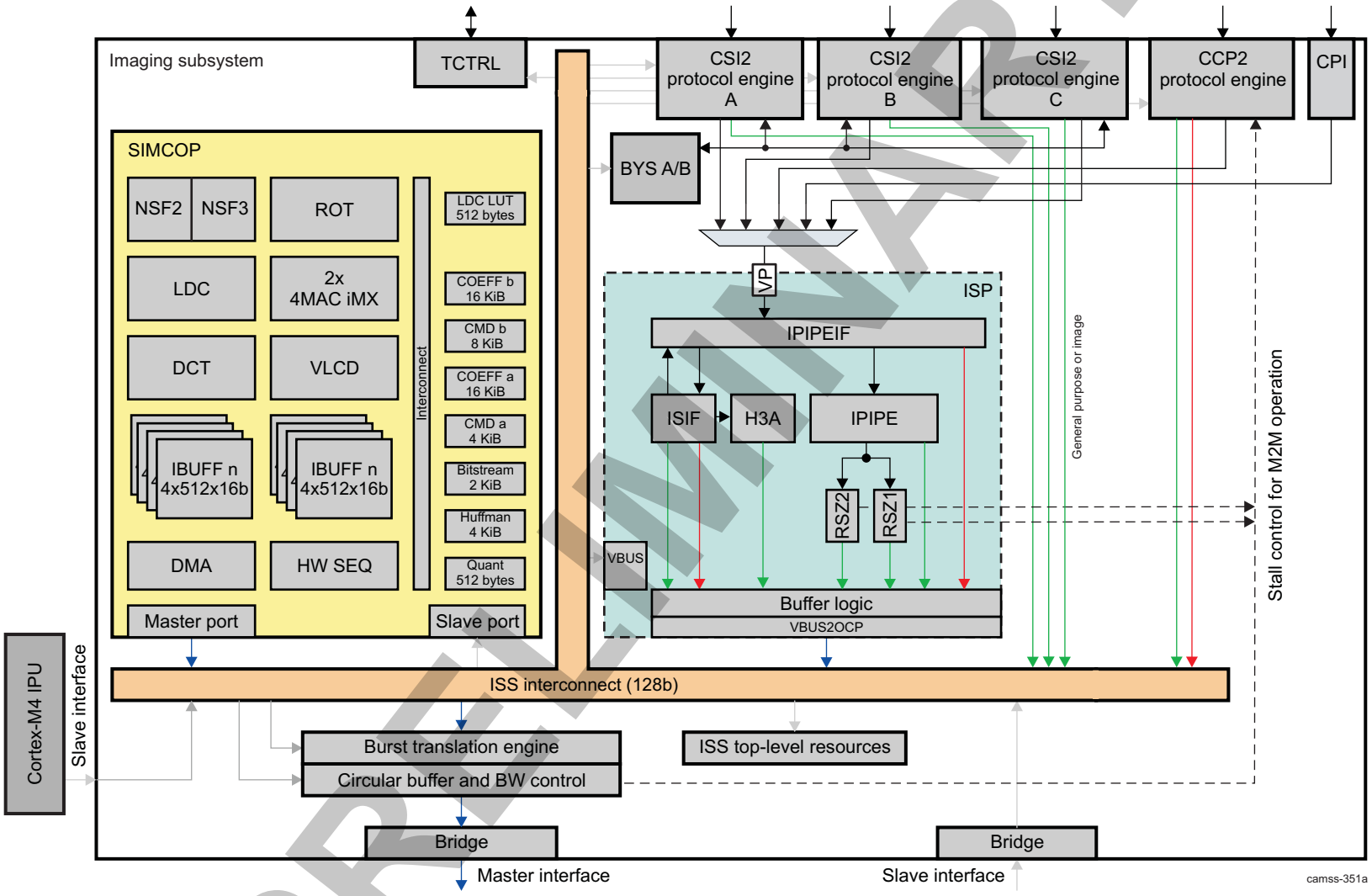
Figure 8-1. ISS Overview



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The direction of the arrows shows the command flow direction from the master (initiator) to the slave (target). The following color conventions are used for the connections:

- Blue: Bidirectional, 128-bit-wide interface data connection
- Green: Write (ISS → system memory) data connection. Either 64-bit interface, 128-bit interface, or 32-bit MTC (inside ISP).
- Red: Read (system memory to ISS) data connection. 128-bit interface port or 32-bit MTC (inside ISP).
- Gray: 32-bit interface configuration connection
- Solid black: Video port and camera interface related signals
- Dotted black: Data flow stall control signal. Used to slow down ISP for memory-to-memory operation.

The ISS is mainly composed of CCP2, CSI2_A, CSI2_B, CSI2_C camera interfaces, a parallel interface (CPI), two bayer scalers (BYS_A and BYS_B), an ISP, and a block-based imaging accelerator (SIMCOP).

The ISS is designed to reach high throughput and low latency with large image sensors. In high-performance mode, the ISP supports a pixel throughput of 304 MPix/s.

Two programmable image processors (iMX4) are included in the SIMCOP subsystem to add further flexibility to implement new algorithms or where new issues are encountered with the image sensors. The iMX4 processors are also open to third-party algorithms.

The ISS is tightly coupled with a low-interrupt latency microprocessor subsystem (Cortex™-M4 IPU) that runs a real-time operating system (OS) to reach optimal performance. Mainly, the Cortex-M4 IPU can quickly change the ISS configuration during frame blanking periods and run some sequencing tasks. It can also be configured using the main MPU subsystem (Cortex™-A15 MPU) or the system DMA controller (DMA_SYSTEM). Typically, Cortex-A15 MPU can run some less latency-sensitive tasks, and the DMA_SYSTEM can be used to transfer large configuration tables used by the ISS (for example, Gamma tables and iMX software).

The ISS targets the following major use cases:

- Viewfinder with digital zoom, video stabilization, and rotations
- Up to 1080p video record at 60 fps with digital zoom, video stabilization, and rotation
- Up to 1080p stereo video record at 30 fps with digital zoom, video stabilization, rotation and auto-convergence
- Up to 24 MPix still image capture with digital zoom and rotation
  - High performance mode: Up to 304 MPix/s throughput
  - High quality and low light modes: Up to 75 MPix/s throughput
- Still image capture during video record

NOTE: The ISS is not limited to 24 Mpix. Higher resolution can be achieved through multiple passes.

NOTE: For a detailed list of features of a certain submodule, see the related subsection.

The ISS offers the following features:

- SIMCOP:
  - Memory-to-memory operation
  - JPEG encode and decode hardware acceleration
  - High-ISO noise filtering
    - NSF 2.0 providing the following throughput:
      - Up to 127 MPix/s for YUV420 format
      - Up to 85 MPix/s for YUV422 format
    - NSF 3.0 with up to 190 MPix/s throughput at 426Mhz clock speed
  - Rotation accelerator

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  - Warping accelerator
  - Lens distortion correction (YUV space) with up to 213 MPix/s throughput
  - General-purpose (GP) imaging accelerator (2x iMX4) with up to 426MHz clock speed
  - Direct memory access (DMA) controller
  - Hardware sequencer
- ISP:
  - On-the-fly or memory-to-memory processing
  - Up to 304MHz pixel throughput
  - Statistic data collection
  - Image pipe interface front-end raw data processing
  - RGB and YUV data processing through ISIF and IPIPE
  - Hardware 3A (H3A) statistics block for real-time auto focus (AF), auto exposure (AE), and auto white balance (AWB)
  - Two image continuous real-time resizers
  - Video port (VP) for interfacing with the receivers and directing data to the ISP
- ISS interfaces:
  - 128-bit-wide data interface to the level 3 (L3_MAIN) interconnect
  - Burst translation engine (BTE) tightly coupled with the TILER to support efficient rotation
  - Circular buffer for linear space, physically located in memory
  - The ISS relies on the centralized memory management unit (MMU). See Chapter 20, *Memory Management Unit*.
  - Three CSI2 camera interfaces: CSI2_A (primary), CSI2_B (secondary)and CSI2_C
  - CCP2 camera interface (secondary)
  - Parallel interface (CPI) (16 bit wide, with up to 148.5 MPix/s throughput, and supporting BT656, SYNC modes)
  - System memory data read-back port (supported by the CCP2 protocol engine module)
- BYS:
  - Two instances, BYS_A and BYS_B (connection to CSI2/3 interfaces)
  - Up to 5 MPix output image size
  - Down scaler and stabilization statistics collection

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8.1.1 ISS Integration

This section describes the integration of the module in the device, including information about clocks, resets, and hardware requests.

Figure 8-2 shows the ISS integration.

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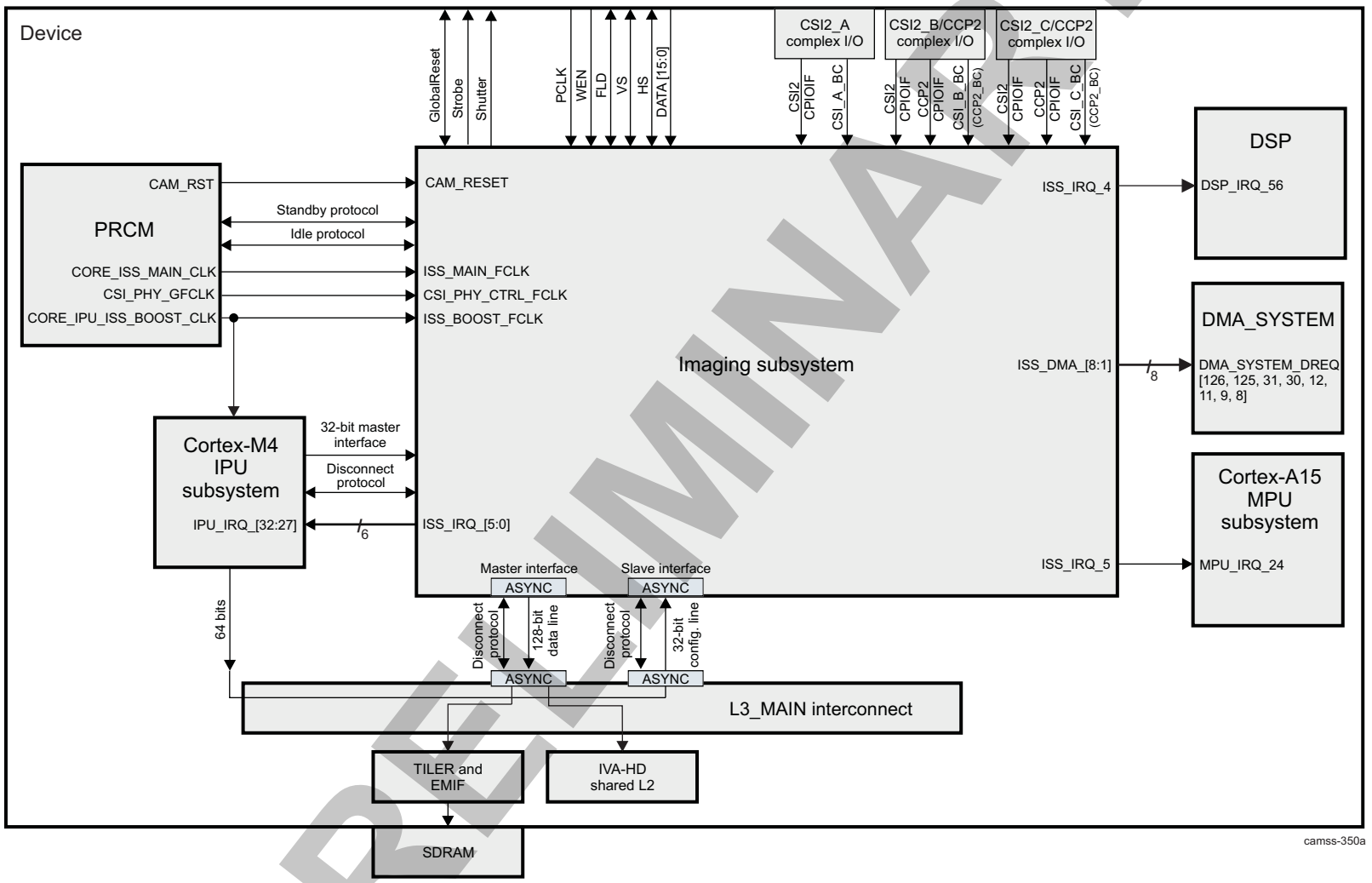
Figure 8-2. ISS Integration



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NOTE: For more information about the IDLE hardware handshake and wake-up request, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

This section gives an overview of typical uses of the module. For more information about the relationship of the power, reset, and clock management (PRCM) module to the ISS clocks and the reset settings, see the detailed functional description in Chapter 3, *Power, Reset, and Clock Management*.

The ISS is part of ISS-IPU hardware and power management, which comprises the Cortex-M4 IPU, ISS, and a clock generator. These are all independent power domains. The ISS is part of the CAM power domain.

The PRCM module provides two clocks to the ISS-IPU power management (CORE_IPU_ISS_BOOST_CLK and CORE_ISS_MAIN_CLK). The ISS-IPU clock generator generates from CORE_IPU_ISS_BOOST_CLK the clocks for the Cortex-M4 IPU and ISS. The CORE_ISS_MAIN_CLK is used by ISS only.

When enabled, CORE_IPU_ISS_BOOST_CLK is gated to provide CAM_BOOST_GCLK, which, after entering the ISS boundary, is named ISS_BOOST_FCLK. The CORE_IPU_ISS_BOOST_CLK is provided as long as the Cortex-M4 IPU or ISS sub-modules require it. The gating control is handled by the PRCM module.

When enabled, CORE_ISS_MAIN_CLK is gated to provide CAM_MAIN_GCLK, which, after entering the ISS boundary, is named ISS_MAIN_FCLK. The gating control is handled by the PRCM module.

CSI_PHY_GFCLK is gated from FUNC_96M_FCLK, which comes from the PRCM module. When enabled and inside the ISS boundary, it is called CSI_PHY_CTRL_FCLK.

NOTE: For more information about the device clocks and how they are handled by the PRCM module before going into the ISS, see Section 3.6.3.5, *DPLL_CORE Description*, and Section 3.6.22, *CD_CAM Clock Domain*, in Chapter 3, *Power, Reset, and Clock Management.*

The ISS also supports software reset. A software reset has the same function as a hardware reset, except that it does not reset the power-management protocols.

Table 8-1 through Table 8-3 summarize the integration of the module in the device.

Table 8-1. ISS Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
ISS	PD_CAM	No	L3_MAIN

Table 8-2. ISS Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
ISS	ISS_MAIN_FLCK	CORE_ISS_MAIN_CLK	PRCM	ISS main functional clock from the PRCM module. Up to 304 MHz for OPP_NOM.
	ISS_BOOST_FCLK	CORE_IPU_ISS_BOOST_CLK	PRCM	Functional clock for LDC, iMX, NSF2 and NSF3 modules in SIMCOP, as well as for attached memories. Up to 425,6 MHz for OPP_NOM.
	CSI_PHY_CTRL_FCLK	CSI_PHY_GFCLK	PRCM	Physical layer functional clock from the PRCM module. Up to 96 MHz for OPP_NOM.
Resets				

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Table 8-2. ISS Clocks and Resets (continued)

Module Instance - Destination Signal Name	Source Signal Name	Source	Description
ISS CAM_RESET	CAM_RST	PRCM	ISS global reset

Table 8-3. ISS Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
ISS	ISS_IRQ_4	DSP_IRQ_56	DSP INTC	Interrupt generated by ISS to DSP
	ISS_IRQ_5	MPU_IRQ_24	Cortex-A15 INTC	Interrupt generated by ISS to Cortex-A15
	ISS_IRQ_0	IPU_IRQ_27	Cortex-M4 INTC	Interrupt generated by ISS to Cortex-M4
	ISS_IRQ_1	IPU_IRQ_28	Cortex-M4 INTC	Interrupt generated by ISS to Cortex-M4
	ISS_IRQ_2	IPU_IRQ_29	Cortex-M4 INTC	Interrupt generated by ISS to Cortex-M4
	ISS_IRQ_3	IPU_IRQ_30	Cortex-M4 INTC	Interrupt generated by ISS to Cortex-M4
	ISS_IRQ_4	IPU_IRQ_31	Cortex-M4 INTC	Interrupt generated by ISS to Cortex-M4
	ISS_IRQ_5	IPU_IRQ_32	Cortex-M4 INTC	Interrupt generated by ISS to Cortex-M4
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
ISS	ISS_DREQ_1	DMA_SYSTEM_DREQ_8	DMA_SYSTEM	Signal connected to the DMA_SYSTEM directly provided by ISP.
	ISS_DREQ_2	DMA_SYSTEM_DREQ_9	DMA_SYSTEM	Signal connected to the DMA_SYSTEM directly provided by ISP
	ISS_DREQ_3	DMA_SYSTEM_DREQ_11	DMA_SYSTEM	Signal connected to the DMA_SYSTEM directly provided by ISP
	ISS_DREQ_4	DMA_SYSTEM_DREQ_12	DMA_SYSTEM	Signal connected to the DMA_SYSTEM directly provided by ISP
	ISS_DREQ_5	DMA_SYSTEM_DREQ_30	DMA_SYSTEM	Signal connected to the DMA_SYSTEM directly provided by BYS_A
	ISS_DREQ_6	DMA_SYSTEM_DREQ_31	DMA_SYSTEM	Signal connected to the DMA_SYSTEM directly provided by BYS_A
	ISS_DREQ_7	DMA_SYSTEM_DREQ_125	DMA_SYSTEM	Signal connected to the DMA_SYSTEM directly provided by BYS_B
	ISS_DREQ_8	DMA_SYSTEM_DREQ_126	DMA_SYSTEM	Signal connected to the DMA_SYSTEM directly provided by BYS_B

8.1.1.1 ISS PRCM Interface Integration

8.1.1.1.1 ISS Clock Domains

The ISS has five asynchronous clock domains. Most of the logic uses ISS_MAIN_FLCK; the other clock domains are used for interfaces.

Table 8-4 provides a high-level view of clocks. The frequencies provided are maximum values.

Table 8-4. ISS Local Clock Domains

Name	Description
PCLK	Parallel interface (CPI) pixel clock provided by the camera external sensor. The CSI2_A, CSI2_B, CSI2_C and CCP2 modules also have video port outputs, each having its own pixel clock. These pixel clocks are generated from the functional clock (ISS_MAIN_FCLK). Then all five pixel clock sources are multiplexed into one clock provided to the ISP. Up to 304 MHz for OPP_NOM.
CSI_A_BC	Byte clock sourced from the CSI2_A complex I/O (CSI_PHY_A) clock RXBYTECLKHS_A. Used by the CSI2_A protocol engine. Up to 187.5 MHz for OPP_NOM.

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Table 8-4. ISS Local Clock Domains (continued)

Name	Description
CSI_B_BC	Byte clock sourced from the CSI2_B complex I/O (CSI_PHY_B) clock RXBYTECLKHS_B. Used by the CSI2_B protocol engine. Up to 187.5 MHz for OPP_NOM.
CSI_C_BC	Byte clock sourced from the CSI2_C complex I/O (CSI_PHY_C) clock RXBYTECLKHS_C. Used by the CSI2_C protocol engine. Up to 187.5 MHz for OPP_NOM.
CCP2_BC	Clock provided by the CCP2 complex I/O (CSI_PHY_B or CSI_PHY_C, depending on configuration). Used by the CCP2 protocol engine. Up to 21 MHz for OPP_NOM.
ISS_MAIN_FLCK	Functional clock provided by the PRCM module. It is used by all ISS submodules and ISS top-level resources. Up to 304 MHz for OPP_NOM.
CSI_PHY_CTRL_FCLK	Functional clock provided by the PRCM module. It is used by the CSI2_A, CSI2_B/CCP2 and CSI2_C/CCP2 complex I/Os. Up to 96 MHz for OPP_NOM.

To save power, the ISS can divide the received functional clock (ISS_MAIN_FLCK) by 2 or 4 using the ISS_CTRL[5:4] ISS_CLK_DIV register bit-field. The PCLK must always be less or equal to the ISS_MAIN_FLCK. The internal configuration clock (CFGCLK, used for the internal ISS configuration network) is always half the ISS_MAIN_FLCK. The ISS_BOOST_FCLK is not affected by the ISS_CLK_DIV bit-field.

The functional clock of some submodules can be cut by software to reduce power consumption by cutting off or turning on the modules from the ISS_CLKCTRL register. Also, the pixel clocks sent by submodules to ISP can be cut off from the corresponding ISS_CLKCTRL[] VPORT*x*_CLK bit-fields.

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8.1.2 ISS Functional Description

This section provides only a top-level overview of the ISS. The ISS submodules are described in: Section 8.2.1, *ISS:interfaces*, Section 8.3.1, *ISS:ISP*, and Section 8.4, *ISS:SIMCOP*.

8.1.2.1 ISS Interrupts

Table 8-5 lists the events generated by the submodules and the top level of the ISS.

Each event that generates an interrupt can be individually enabled by setting the appropriate bit in the ISS_HL_IRQENABLE_SET_i register. The interrupt is disabled by setting the appropriate bit in the ISS_HL_IRQENABLE_CLR_i register.

When an event occurs, the corresponding bit in the ISS_HL_IRQSTATUS_RAW_i register is set regardless of whether or not the event is enabled. Bits in the ISS_HL_IRQSTATUS_i registers are set only when an enabled event occurs.

Software can clear a pending HS_VS_IRQ event by setting the ISS_HL_IRQSTATUS_i[17] HS_VS_IRQ bit. Events generated by submodules are automatically cleared at the ISS level when they are cleared at the submodule level.

8.1.2.1.1 ISS Interrupt Merger

The ISS merges the following eleven interrupt sources into six physical interrupt lines. All six lines support level and pulse modes.

Table 8-5. ISS Interrupts

Interrupt	Source	Description
ISP_IRQ[3:0]	ISP	Interrupt generated by the ISP (1)
CSIA_IRQ	CSI2_A	Interrupt generated by the CSI2_A receiver(1)
CSIB_IRQ	CSI2_B	Interrupt generated by the CSI2_B receiver (1)
CSIC_IRQ	CSI2_C	Interrupt generated by the CSI2_C receiver (1)
CCP2_IRQ[3:0]	CCP2	Interrupt generated by the CCP2 receiver(1)
CCP2_IRQ[8]	CCP2	Interrupt generated by the CCP2 receiver(1)
CBUFF_IRQ	CBUFF	Interrupt generated by the circular buffer(1)
BTE_IRQ	BTE	Interrupt generated by the BTE (1)
SIMCOP_IRQ[3:0]	SIMCOP	Interrupt generated by SIMCOP
HS_VS_IRQ	ISS	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal. The rising or falling edge and the HS or VS signal selection are chosen using the ISP_CTRL[0:1] SYNC_DETECT bit field.
BYSA_IRQ	BYS_A	Interrupt generated by the BYS_A module (1)
BYSB_IRQ	BYS_B	Interrupt generated by the BYS_B module (1)

(1) For more information, see Section 8.1.2.1.2, *ISS Submodule Interrupts*.

Software can select which interrupt sources are routed to each output line (ISS_IRQ_[0:5]). All six physical interrupt outputs have equivalent functions. Software can use different interrupt lines to group events together by type and therefore reduce interrupt latencies. Typically, one interrupt line is used for low-priority events (errors), and the other interrupt lines are used for high-priority events (for example, SIMCOP sequencing and end-of-frame events to trigger configuration load). The ISS internal interrupt request (IRQ) merger (see Figure 8-3) relies only on level interrupts provided by submodules. Pulse interrupts provided by submodules are ignored. Typically, all of the interrupts are routed to the Cortex-M4 IPU running the camera driver. In addition, one interrupt is routed to Cortex-A15 MPU, which may run the imaging software. Software does not need to clear events from submodules at the ISS level: it clears only the events at the submodule level. The IRQ merger automatically clears the IRQ at ISS level (events generated by sub-modules are automatically cleared at ISS level when they are cleared at sub-module level).

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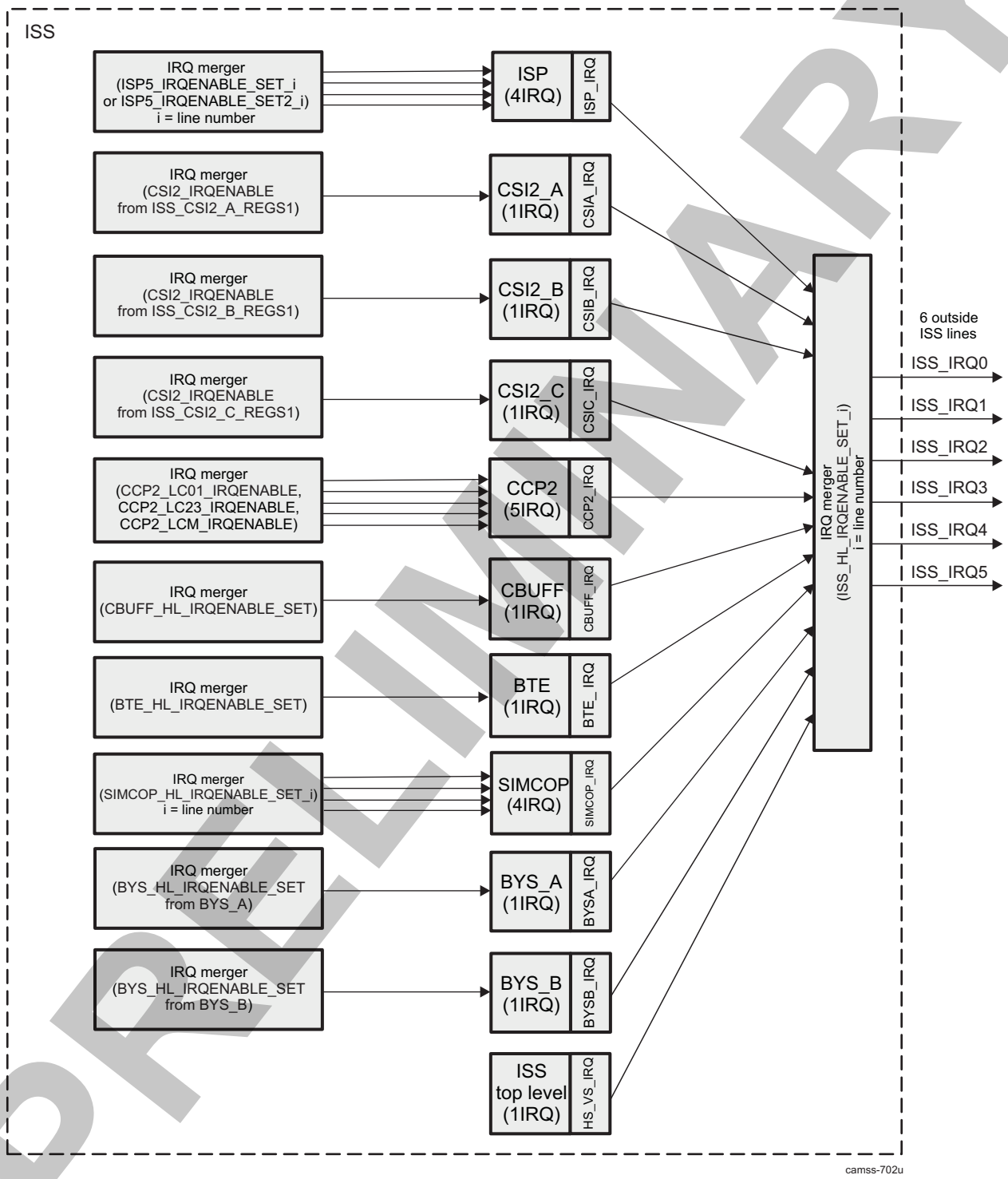
NOTE: Only the HS_VS_IRQ top-level event is cleared at the ISS level.

Figure 8-3. ISS Interrupt Merger



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NOTE: For more information about mapping the six lines to the device modules outside ISS, see Table 8-3.

Only the ISP, SIMCOP, and HL ISS merger IRQ lines are configurable. Each interrupt can be mapped to the required line. This is not the case with CCP2 where, for example, LC01 is hardwired to line0 and line1.

8.1.2.1.2 ISS Submodule Interrupts

The ISS shown in Figure 8-3 and listed in Table 8-3 can generate six interrupts.

8.1.2.1.2.1 ISS ISP Interrupts

Table 8-6 summarizes events that cause ISP interrupts.

Table 8-6. ISS ISP Interrupts

Event and Register[1]	Description
ISP5_IRQENABLE_SET_i[[31] OCP_ERR_IRQ	An interface port error has been received on the ISP master port.
ISP5_IRQENABLE_SET_i[29] IPIPE_INT_DPC_RNEW1	HD interrupt signal to indicate the need to renew the defect pixel correction (DPC) table with new entries. The second 128 entries in the DPC table must be updated when this event triggers. This event is triggered when the 255th entry in the look-up table (LUT) is used. This interrupt is not synchronous to the HD signal.
ISP5_IRQENABLE_SET_i[28] IPIPE_INT_DPC_RNEW0	VD interrupt signal to indicate the need to renew the DPC table with new entries. The first 128 entries in the DPC table must be updated when the event triggers. This event is triggered when the 127th entry in the LUT is used. This interrupt is not synchronous to the HD signal.
ISP5_IRQENABLE_SET_i[27] IPIPE_INT_DPC_INI	Interrupt to signal the need to initialize the DPC table. The DPC table contains two tables of 128 entries. When this signal is used, software must ensure that the 256 table entries are updated with the DPC information.
ISP5_IRQENABLE_SET_i[25] IPIPE_INT_EOF	End of frame interrupt signal
ISP5_IRQENABLE_SET_i[24] H3A_INT_EOF	End of frame interrupt signal
ISP5_IRQENABLE_SET_i[22] RSZ_INT_EOF1	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[23] RSZ_INT_EOF0	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[19] RSZ_FIFO_IN_BLK_ERR	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[18] RSZ_FIFO_IN_OVF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[17] RSZ_INT_CYC_RZB	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[16] RSZ_INT_CYC_RZA	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[15] RSZ_INT_DMA	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[14] RSZ_INT_LAST_PIX	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[13] RSZ_INT_REG	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[12] H3A_INT	Interrupt generated by the AF and AE/AWB blocks inside the H3A module. It indicates the end of processing a frame and is active high for one configuration bus clock cycle.
ISP5_IRQENABLE_SET_i[11] AF_INT	AF inside generates an interrupt at the end of processing frame; a third interrupt is generated at the same time as the last process to finish.
ISP5_IRQENABLE_SET_i[10] AEW_INT	AEW inside generates an interrupt at the end of processing frame; a third interrupt is generated at the same time as the last process to finish.

(1) i = 0 to 3

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Table 8-6. ISS ISP Interrupts (continued)

Event and Register[(1)]	Description
ISP5_IRQENABLE_SET_i[9] IPIPEIF_IRQ	IPIPEIF module interrupt is generated at the start position of a frame and is active high for one configuration bus clock cycle.
ISP5_IRQENABLE_SET_i[8] IPIPE_INT_HST	IPIPE module interrupt is generated when histogram is done.
ISP5_IRQENABLE_SET_i[7] IPIPE_INT_BSC	IPIPE module interrupt is generated when boundary signal calculation is done.
ISP5_IRQENABLE_SET_i[6] IPIPE_INT_DMA	IPIPE module interrupt is issued when the SDRAM transfer of boxcar is done. At this time, IPIPE EOF is sent to buffer logic.
ISP5_IRQENABLE_SET_i[5] IPIPE_INT_LAST_PIX	IPIPE module interrupt is issued when the last pixel of a frame comes into IPIPE.
ISP5_IRQENABLE_SET_i[4] IPIPE_INT_REG	IPIPE module interrupt is issued when the register update of the module is allowed.
ISP5_IRQENABLE_SET_i[3] ISIF_INT_3	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[2] ISIF_INT_2	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[1] ISIF_INT_1	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET_i[0] ISIF_INT_0	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[0] H3A_OVF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[1] IPIPEIF_UDF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[2] IPIPE_BOXCAR_OVF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[3] ISIF_OVF	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.
ISP5_IRQENABLE_SET2_i[4] IPIPE_HST_ERR	See Section 8.1.3, *ISS Register Manual*, and Section 8.3.5, *ISS ISP Register Manual*.

8.1.2.1.2.2 ISS CSI2_A, CSI2_B and CSI2_C Complex I/O Interrupts

Table 8-7 lists the event generation of the CSI2_A, CSI2_B and CSI2_C receivers through the CSI2 interrupt status and interrupt enable registers. The events are checked for status using the CSI2_IRQSTATUS and CSI2_IRQENABLE registers.

Table 8-7. ISS CSI2_A, CSI2_B and CSI2_C Interrupts

Event and Register	Description
CSI2_IRQENABLE[14] OCP_ERR_IRQ	Interface port error
CSI2_IRQENABLE[13] SHORT_PACKET_IRQ	Short packet reception (other than sync events: line start, line end, frame start, and frame end; only data types from 0x8 to 0xF are considered)
CSI2_IRQENABLE[12] ECC_CORRECTION_IRQ	ECC was used to correct a 1-bit error (short packet only).
CSI2_IRQENABLE[11] ECC_NO_CORRECTION_IRQ	ECC was not used to correct the header because the error is larger than 1 bit (short and long packets).
CSI2_IRQENABLE[9] COMPLEXIO_ERR_IRQ	Error signaling from complex I/O: This interrupt is triggered when any error is received from the complex I/O (events are defined in CSI2_COMPLEXIO_IRQSTATUS [see Table 8-8]).
CSI2_IRQENABLE[8] FIFO_OVF_IRQ	FIFO overflow error: This interrupt is triggered when a FIFO overflow is detected. An overflow can occur if there is a mismatch between the data input and output rates. In case of an overflow the module properly finishes the burst that has been started and does not issue any new OCP transactions on the master port. A reset of the module is required to restart correctly.
CSI2_IRQENABLE[7] CONTEXT7	At least one interrupt event enabled from Context 7 occurred (see Table 8-9).

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Table 8-7. ISS CSI2_A, CSI2_B and CSI2_C Interrupts (continued)

Event and Register	Description
CSI2_IRQENABLE[6] CONTEXT6	At least one interrupt event enabled from Context 6 occurred (see Table 8-9).
CSI2_IRQENABLE[5] CONTEXT5	At least one interrupt event enabled from Context 5 occurred (see Table 8-9).
CSI2_IRQENABLE[4] CONTEXT4	At least one interrupt event enabled from Context 4 occurred (see Table 8-9).
CSI2_IRQENABLE[3] CONTEXT3	At least one interrupt event enabled from Context 3 occurred (see Table 8-9).
CSI2_IRQENABLE[2] CONTEXT2	At least one interrupt event enabled from Context 2 occurred (see Table 8-9).
CSI2_IRQENABLE[1] CONTEXT1	At least one interrupt event enabled from Context 1 occurred (see Table 8-9).
CSI2_IRQENABLE[0] CONTEXT0	At least one interrupt event enabled from Context 0 occurred (see Table 8-9).

Table 8-8 lists CSI2 receiver event generation through the CSI2_A/CSI2_B/CSI2_C complex I/O interrupt status and interrupt enable registers. The events are checked and controlled from the CSI2_COMPLEXIO_IRQSTATUS and CSI2_COMPLEXIO_IRQENABLE registers.

Table 8-8. ISS CSI2_A, CSI2_B and CSI2_C Receivers Complex I/O Interrupts

Event and Register	Description
CSI2_COMPLEXIO_IRQENABLE[0] ERRSOTHS1	Start of transmission error for lane 1
CSI2_COMPLEXIO_IRQENABLE[1] ERRSOTHS2	Start of transmission error for lane 2
CSI2_COMPLEXIO_IRQENABLE[2] ERRSOTHS3	Start of transmission error for lane 3
CSI2_COMPLEXIO_IRQENABLE[5] ERRSOTSYNCHS1	Start of transmission sync error for lane 1
CSI2_COMPLEXIO_IRQENABLE[6] ERRSOTSYNCHS2	Start of transmission sync error for lane 2
CSI2_COMPLEXIO_IRQENABLE[7] ERRSOTSYNCHS3	Start of transmission sync error for lane 3
CSI2_COMPLEXIO_IRQENABLE[10] ERRESC1	Escape entry error for lane 1
CSI2_COMPLEXIO_IRQENABLE[11] ERRESC2	Escape entry error for lane 2
CSI2_COMPLEXIO_IRQENABLE[12] ERRESC3	Escape entry error for lane 3
CSI2_COMPLEXIO_IRQENABLE[15] ERRCONTROL1	Control error for lane 1
CSI2_COMPLEXIO_IRQENABLE[16] ERRCONTROL2	Control error for lane 2
CSI2_COMPLEXIO_IRQENABLE[17] ERRCONTROL3	Control error for lane 3
CSI2_COMPLEXIO_IRQENABLE[20] STATEULPM1	Lane 1 in ULPM
CSI2_COMPLEXIO_IRQENABLE[21] STATEULPM2	Lane 2 in ULPM
CSI2_COMPLEXIO_IRQENABLE[22] STATEULPM3	Lane 3 in ULPM
CSI2_COMPLEXIO_IRQENABLE[25] STATEALLULPMENTER	All active lanes are entering the ULPM.
CSI2_COMPLEXIO_IRQENABLE[26] STATEALLULPMEXIT	At least one active lane exited the ULPM.

Because the CSI2_A/CSI2_B/CSI2_C receivers support eight contexts, the CSI2_CTX_IRQSTATUS_i and CSI2_CTX_IRQENABLE_i registers are present eight times (one time per context).

The events are generated only for the enabled context(s). Table 8-9 describes the generation of the CSI2 receiver event through the CSI2_CTX_IRQSTATUS_i and CSI2_CTX_IRQENABLE_i registers.

Table 8-9. ISS CSI2_A/CSI2_B/CSI2_C Receivers CONTEXT Interrupts

Event[(1)]	Description
CSI2_CTX_IRQENABLE_i[0] FS_IRQ	Frame start: This interrupt is triggered when a frame-start synchronization code is detected in the CSI2 data stream.

(1) i = 0 to 7

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Table 8-9. ISS CSI2_A/CSI2_B/CSI2_C Receivers CONTEXT Interrupts (continued)

Event[1]	Description
CSI2_CTX_IRQENABLE_i[1] FE_IRQ	Frame end: This interrupt is triggered when a frame-end synchronization code is detected in the CSI2 data stream.
CSI2_CTX_IRQENABLE_i[2] LS_IRQ	Line start: This interrupt is triggered when a line-start synchronization code is detected in the CSI2 data stream.
CSI2_CTX_IRQENABLE_i[3] LE_IRQ	Line end: This interrupt is triggered when a line-end synchronization code is detected in the CSI2 data stream.
CSI2_CTX_IRQENABLE_i[5] CS_IRQ	CS error: This interrupt is triggered when a mismatch between the transmitter and receiver checksums (payload) is detected.
CSI2_CTX_IRQENABLE_i[6] FRAME_NUMBER_IRQ	Frame counter reached: This interrupt is triggered when the frame counter reaches its programmable target value.
CSI2_CTX_IRQENABLE_i[7] LINE_NUMBER_IRQ	Line number reached: The programmable line number is received. The modulo feature can be selected (CSI2_CTX_CTRL1_i.LINE_MODULO). When selected, the interrupt is generated for each line number multiple of the programmed line number (CSI2_CTX_CTRL3_i.LINE_NUMBER); otherwise, the interrupt is generated only for the line number.
CSI2_CTX_IRQENABLE_i[8] ECC_CORRECTION_IRQ	ECC was used to correct a 1-bit error (long packets only).

8.1.2.1.2.3 ISS CCP2 Interrupts

Table 8-10 summarizes the CCP2 receiver interrupts.

Table 8-10. ISS CCP2 Receiver Interrupts

Event and Register	Description
CCP2_LC01_IRQENABLE[31] LC1_OCPERROR_IRQ	CCP2 write master interface port error on logical channel 1
CCP2_LC01_IRQENABLE[27] LC1_FS_IRQ	CCP2 frame-start synchronization code detection on logical channel 1. This interrupt is triggered when a frame-start synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[26] LC1_LE_IRQ	CCP2 line-end synchronization code detection on logical channel 1. This interrupt is triggered when a line-end synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[25] LC1_LS_IRQ	CCP2 line-start synchronization code detection on logical channel 1. This interrupt is triggered when a line-start synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[24] LC1_FE_IRQ	CCP2 frame-end synchronization code detection on logical channel 1. This interrupt is triggered when a frame-end synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[23] LC1_COUNT_IRQ	CCP2 frame counter reached on logical channel 1. This interrupt is triggered when the frame counter reaches its programmable target value.
CCP2_LC01_IRQENABLE[21] LC1_FIFO_OVF_IRQ	CCP2 FIFO overflow error for logical channel 1. An overflow can occur if there is a mismatch between the data input and output rates.
CCP2_LC01_IRQENABLE[20] LC1_CRC_IRQ	CCP2 CRC error for logical channel 1. This interrupt is triggered when a mismatch between the transmitter and receiver checksums is detected.
CCP2_LC01_IRQENABLE[19] LC1_FSP_IRQ	CCP2 false-synchronization protection code error for logical channel 1. This interrupt is triggered by the FSP decoder if an illegal combination is detected, but 0xA5 is not present in the bitstream.
CCP2_LC01_IRQENABLE[18] LC1_FW_IRQ	CCP2 frame-width error for logical channel 1. This interrupt is generated if the frame width constraints associated with the current data type are not respected.
CCP2_LC01_IRQENABLE[17] LC1_FSC_IRQ	CCP2 false-synchronization code error for logical channel 1. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver finite state-machine (FSM).
CCP2_LC01_IRQENABLE[15] LC0_OCPERROR_IRQ	CCP2 write master interface port error on logical channel 1
CCP2_LC01_IRQENABLE[11] LC0_FS_IRQ	CCP2 frame-start synchronization code detection on logical channel 0. This interrupt is triggered when a frame-start synchronization code is detected in the CCP2 data stream.

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Table 8-10. ISS CCP2 Receiver Interrupts (continued)

Event and Register	Description
CCP2_LC01_IRQENABLE[10] LC0_LE_IRQ	CCP2 line-end synchronization code detection on logical channel 0. This interrupt is triggered when a line-end synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[9] LC0_LS_IRQ	CCP2 line-start synchronization code detection on logical channel 0. This interrupt is triggered when a line-start synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[8] LC0_FE_IRQ	CCP2 frame-end synchronization code detection on logical channel 0. This interrupt is triggered when a frame-end synchronization code is detected in the CCP2 data stream.
CCP2_LC01_IRQENABLE[7] LC0_COUNT_IRQ	CCP2 frame counter reached on logical channel 0. This interrupt is triggered when the frame counter reaches its programmable target value.
CCP2_LC01_IRQENABLE[5] LC0_FIFO_OVF_IRQ	CCP2 FIFO overflow error for logical channel 0. An overflow can occur if there is a mismatch between the data input and output rates.
CCP2_LC01_IRQENABLE[4] LC0_CRC_IRQ	CCP2 CRC error for logical channel 0. This interrupt is triggered when a mismatch between the transmitter and receiver checksums is detected.
CCP2_LC01_IRQENABLE[3] LC0_FSP_IRQ	CCP2 false-synchronization code error for logical channel 0. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC01_IRQENABLE[2] LC0_FW_IRQ	CCP2 frame-width error for logical channel 0. This interrupt is generated if the frame-width constraints associated with the current data type are not respected.
CCP2_LC01_IRQENABLE[1] LC0_FSC_IRQ	CCP2 false-synchronization code error for logical channel 0. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC23_IRQENABLE[31] LC3_OCPERROR_IRQ	CCP2 write master interface port error on logical channel 3
CCP2_LC23_IRQENABLE[27] LC3_FS_IRQ	CCP2 frame-start synchronization code detection on logical channel 3. This interrupt is triggered when a frame-start synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[26] LC3_LE_IRQ	CCP2 line-end synchronization code detection on logical channel 3. This interrupt is triggered when a line-end synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[25] LC3_LS_IRQ	CCP2 line-start synchronization code detection on logical channel 3. This interrupt is triggered when a line-start synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[24] LC3_FE_IRQ	CCP2 frame-end synchronization code detection on logical channel 3. This interrupt is triggered when a frame-end synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[23] LC3_COUNT_IRQ	CCP2 frame counter reached on logical channel 3. This interrupt is triggered when the frame counter reaches its programmable target value.
CCP2_LC23_IRQENABLE[21] LC3_FIFO_OVF_IRQ	CCP2 FIFO overflow error for logical channel 3. An overflow can occur if there is a mismatch between the data input and output rates.
CCP2_LC23_IRQENABLE[20] LC3_CRC_IRQ	CCP2 CRC error for logical channel 3. This interrupt is triggered when a mismatch between the transmitter and receiver checksums is detected.
CCP2_LC23_IRQENABLE[19] LC3_FSP_IRQ	CCP2 false-synchronization code error for logical channel 3. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC23_IRQENABLE[18] LC3_FW_IRQ	CCP2 frame-width error for logical channel 3. This interrupt is generated if the frame-width constraints associated with the current data type are not respected.
CCP2_LC23_IRQENABLE[17] LC3_FSC_IRQ	CCP2 false-synchronization code error for logical channel 3. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC23_IRQENABLE[11] LC2_FS_IRQ	CCP2 frame-start synchronization code detection on logical channel 2. This interrupt is triggered on the detection of a frame-start synchronization code into the CCP2 data stream.
CCP2_LC23_IRQENABLE[10] LC2_LE_IRQ	CCP2 line-end synchronization code detection on logical channel 2. This interrupt is triggered on the detection of a line-end synchronization code into the CCP2 data stream.

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Table 8-10. ISS CCP2 Receiver Interrupts (continued)

Event and Register	Description
CCP2_LC23_IRQENABLE[9] LC2_LS_IRQ	CCP2 line-start synchronization code detection on logical channel 2. This interrupt is triggered when a line-start synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[8] LC2_FE_IRQ	CCP2 frame-end synchronization code detection on logical channel 2. This interrupt is triggered when a frame-end synchronization code is detected in the CCP2 data stream.
CCP2_LC23_IRQENABLE[7] LC2_COUNT_IRQ	CCP2 frame counter reached on logical channel 2. This interrupt is triggered when the frame counter reaches its programmable target value.
CCP2_LC23_IRQENABLE[5] LC2_FIFO_OVF_IRQ	CCP2 FIFO overflow error for logical channel 2. An overflow can occur if there is a mismatch between the data input and output rates.
CCP2_LC23_IRQENABLE[4] LC2_CRC_IRQ	CCP2 CRC error for logical channel 2. This interrupt is triggered when a mismatch is detected between the transmitter and receiver checksums.
CCP2_LC23_IRQENABLE[3] LC2_FSP_IRQ	CCP2 false-synchronization code error for logical channel 2. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LC23_IRQENABLE[2] LC2_FW_IRQ	CCP2 frame-width error for logical channel 2. This interrupt is generated if the frame-width constraints associated with the current data type are not respected.
CCP2_LC23_IRQENABLE[1] LC2_FSC_IRQ	CCP2 false-synchronization code error for logical channel 2. This interrupt is triggered if the synchronization code order is not respected. This state is shown in the CCP2 receiver FSM.
CCP2_LCM_IRQENABLE[1] LCM_OCPERROR	CCP2 an interface error occurred on the master read port. This interrupt is triggered when an OCP error is detected on the master read port.
CCP2_LCM_IRQENABLE[0] LCM_EOF	Memory read channel – end of frame: This interrupt is triggered when a frame is read completely from memory.

8.1.2.1.2.4 ISS CBUFF Interrupts

Table 8-11 summarizes the CBUFF interrupts.

Table 8-11. ISS CBUFF Interrupts

Event and Register	Description
CBUFF_HL_IRQENABLE_SET[27] IRQ_CTX3_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[26] IRQ_CTX2_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[25] IRQ_CTX1_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[24] IRQ_CTX0_OVR	CBUFF overflow
CBUFF_HL_IRQENABLE_SET[19] IRQ_CTX3_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[18] IRQ_CTX2_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[17] IRQ_CTX1_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[16] IRQ_CTX0_INVALID	CBUFF invalid access
CBUFF_HL_IRQENABLE_SET[11] IRQ_CTX3_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[10] IRQ_CTX2_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[9] IRQ_CTX1_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[8] IRQ_CTX0_READY	CBUFF WB physical window ready for access by the CPU
CBUFF_HL_IRQENABLE_SET[0] IRQ_OCP_ERR	CBUFF master interface port error

8.1.2.1.2.5 ISS BTE Interrupts

Table 8-12 summarizes the BTE interrupts.

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Table 8-12. ISS BTE Interrupts

Event and Register	Description
BTE_HL_IRQENABLE_SET[27] IRQ_CTX3_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 3 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[26] IRQ_CTX2_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 2 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[25] IRQ_CTX1_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 1 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[24] IRQ_CTX0_ERR	Writes enable notification for read request before enough data is prefetched. Reads notify when a read request that requires translation on Context 0 is received, but not enough frame lines have been prefetched in the buffer. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[19] IRQ_CTX3_INVALID	Writes enable invalid access to Context 3. Reads notify when access to an unexpected location in Context 3 is requested, or the start context location access is valid, but the burst length exceeds the Context 3 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[18] IRQ_CTX2_INVALID	Writes enable invalid access to Context 2. Reads notify when access to an unexpected location in Context 2 is requested, or the start context location access is valid, but the burst length exceeds the Context 2 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[17] IRQ_CTX1_INVALID	Writes enable invalid access to Context 1. Reads notify when access to an unexpected location in Context 1 is requested, or the start context location access is valid, but the burst length exceeds the Context 1 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[16] IRQ_CTX0_INVALID	Writes enable invalid access to Context 0. Reads notify when access to an unexpected location in Context 0 is requested, or the start context location access is valid, but the burst length exceeds the Context 0 end. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[11] IRQ_CTX3_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 3 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[10] IRQ_CTX2_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 2 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[9] IRQ_CTX1_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 1 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.

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Table 8-12. ISS BTE Interrupts (continued)

Event and Register	Description
BTE_HL_IRQENABLE_SET[8] IRQ_CTX0_DONE	Writes enable notification for context that has been fully and successfully transferred to TILER. Reads notify when enough frame lines have been prefetched into the buffer and Context 0 is translated to TILER. This interrupt is triggered when flushing completes (if enabled) in one-shot mode. It is triggered once per frame in continuous mode. See Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.
BTE_HL_IRQENABLE_SET[1] IRQ_INVALID	Writes enable Invalid virtual space access notification. Reads notify when access falls into a translated from the BTE region, but it is 2D access or it does not map to an active context. See Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
BTE_HL_IRQENABLE_SET[1] IRQ_OCP_ERR	Writes enable notification for error on the master output interface. Reads notify when an error has occurred on the master output interface.

8.1.2.1.2.6 ISS SIMCOP Interrupts

Table 8-13 summarizes the SIMCOP high-level interrupts mapped to the outer boundaries of the SIMCOP. For more information about interrupts generated from inside the SIMCOP modules, see Section 8.4, *ISS Still Image Coprocessor*.

Table 8-13. ISS SIMCOP High-Level Interrupts

Event and Register	Description
SIMCOP_HL_IRQENABLE_SET_i[19] CPU_PROC_START_IRQ	Interrupt used when CPU data processing is used in a macroblock processing pipeline. When the CPU receives this IRQ, data is ready to be processed. When the CPU finishes processing the data, it acknowledges by setting the SIMCOP_HWSEQ_CTRL.CPU_PROC_DONE bit.
SIMCOP_HL_IRQENABLE_SET_i[18] SIMCOP_DMA_IRQ1	Interrupt triggered by SIMCOP DMA
SIMCOP_HL_IRQENABLE_SET_i[16] OCP_ERR_IRQ	SIMCOP master port interface error
SIMCOP_HL_IRQENABLE_SET_i[15] VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module.
SIMCOP_HL_IRQENABLE_SET_i[14] DONE_IRQ	Event triggered when hardware sequencer finishes the sequence: • The sequence step counter has reached the limit. • All accelerator and DMA events for the last sequence step have been received.
SIMCOP_HL_IRQENABLE_SET_i[13] STEP3_IRQ	Event triggered when a SIMCOP Context 3 is activated by the hardware sequencer.
SIMCOP_HL_IRQENABLE_SET_i[12] STEP2_IRQ	Event triggered when a SIMCOP Context 2 is activated by the hardware sequencer.
SIMCOP_HL_IRQENABLE_SET_i[11] STEP1_IRQ	Event triggered when a SIMCOP Context 1 is activated by the hardware sequencer.
SIMCOP_HL_IRQENABLE_SET_i[10] STEP0_IRQ	Event triggered when a SIMCOP Context 0 is activated by the hardware sequencer.
SIMCOP_HL_IRQENABLE_SET_i[9] LDC_BLOCK_IRQ	A macroblock has been processed.
SIMCOP_HL_IRQENABLE_SET_i[8] NSF3_IRQ	Event triggered by the NSF3 imaging accelerator when processing of a block is complete
SIMCOP_HL_IRQENABLE_SET_i[7] ROT_A	Rotational engine interrupt
SIMCOP_HL_IRQENABLE_SET_i[6] IMX_B_IRQ	Event triggered when iMX has executed a SLEEP instruction
SIMCOP_HL_IRQENABLE_SET_i[5] IMX_A_IRQ	Event triggered when iMX has executed a SLEEP instruction
SIMCOP_HL_IRQENABLE_SET_i[4] NSF_IRQ	Event triggered by the NSD2 imaging accelerator when processing of a block is complete
SIMCOP_HL_IRQENABLE_SET_i[3] VLCDJ_BLOC_IRQ	A macroblock has been processed (that is, encode and decode).
SIMCOP_HL_IRQENABLE_SET_i[2] DCT_IRQ	DCT operating is complete (configured number of MCUs for YUV4:2:0/4:2:2 mode, or number of blocks for sequential block mode).

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Table 8-13. ISS SIMCOP High-Level Interrupts (continued)

Event and Register	Description
SIMCOP_HL_IRQENABLE_SET_i[1] LDC_FRAME_IRQ	A full frame has been processed.
SIMCOP_HL_IRQENABLE_SET_i[0] SIMCOP_DMA_IRQ0	Interrupt triggered by SIMCOP DMA

8.1.2.1.2.7 ISS BYS Interrupts

Table 8-14 lists the event generation of the BYS_A and BYS_B modules through the BYS interrupt enable register. The events are checked for status using the BYS_HL_IRQSTATUS and BYS_HL_IRQENABLE_SET registers. The interrupts can be disabled using BYS_HL_IRQENABLE_CLR register.

Table 8-14. ISS BYS Interrupts

Event and Register	Description
BYS_HL_IRQENABLE_SET[8] VPO_EOF	Video port end of frame event. Triggered when the last pixel of a frame has been sent to the output video port.
BYS_HL_IRQENABLE_SET[5] EOF1	End of frame event of BSC pipe #1. Triggered when the last active bin had been updated.
BYS_HL_IRQENABLE_SET[4] EOF0	End of frame event of BSC pipe #0. Triggered when the last active bin had been updated.
BYS_HL_IRQENABLE_SET[3] H2V_OVR	H2V FIFO overflow event. This event occurs when data written by the horizontal stage arrives at a higher rate than what the vertical stage can process. This error is due to wrong configuration.
BYS_HL_IRQENABLE_SET[2] OB_OVR	Output buffer overflow event. This event occurs when the chosen buffer readout rate is too low for the incoming pixel rate. The pixels and BSC statistics for the frame are corrupted and must be discarded when this event has occurred. Software must reset the module and configure it properly (this overflow will be systematic failure and occur on every frame, if the configuration is not fixed).
BYS_HL_IRQENABLE_SET[1] LINE	Line event. Triggered when the input line number before the cropping stage matches the BYS_LINE[12:0] LINE register bit-field value. The input line number is reset when a VS pulse is received and incremented by one on every HS pulse. The event is triggered at the beginning of the line (i.e. when the first pixel of the line is received). This feature is typically used to synchronize BYS with other downstream processing. NOTE: LINE and VPI_SOF events will by triggered in the same time when BYS_LINE[12:0] LINE = 0.
BYS_HL_IRQENABLE_SET[0] VPI_SOF	Start of frame event. Triggered when the first pixel is received on the input video port. Matches the moment where shadow registers are swapped.

8.1.2.2 ISS Clocks

The clocks of ISS submodules can be cut individually using the ISS_CLKCTRL register. Software can poll the module status reading the appropriate bit in the ISS_CLKSTAT register.

When software wants to enable a submodule:

- Software sets the appropriate bit in the ISS_CLKCTRL register.
- Hardware enables the submodule functional and interface clocks (expected to take a few cycles).
- Hardware sets the appropriate bit in the ISS_CLKSTAT register.

Software must enable the modules in the correct order. The hardware imposes no particular constraint. For example, when data must be provided by the CSI2_A/CSI2_B receiver and processed by the ISP, both modules must be enabled and correctly configured before data arrives. An example of configuration order is: enabling the CSI2_A receiver powers up the complex I/O connected to the external sensor. Additionally, the ISP must be configured and the source interface must be selected. For details and the order of configuration, see the programming module of the particular submodule.

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When software wants to shut down a submodule:

- Software ensures that the submodule is idle. Mainly:
  - The submodule must not generate new events.
  - The submodule must not have any pending events.
  - For initiators: The submodule must stop the generation of an interface bridge transaction.
- Software clears the appropriate bit in the ISS_CLKCTRL register.
- For modules having only a master port: Hardware waits until the submodule to be disconnected asserts the MStandBy signal on its master port. It asserts MWait of the submodule.

NOTE: The ISS does not assert the MWait signal when a shutdown of the module is not requested by software.

- Hardware cuts the submodule clocks.
- Hardware clears the appropriate bit in the ISS_CLKSTAT register.

Table 8-15 describes the clock gating of the ISS submodule.

Table 8-15. ISS Submodule Clock Gating

ISS Resource	Feature On/Off Control
ISS top-level resources	Not applicable. ISS top-level resources cannot be cut. However, top-level resources support the autogating feature.
SIMCOP	ISS_CLKCTRL[0] SIMCOP
ISP	ISS_CLKCTRL[1] ISP
CSI2_A	ISS_CLKCTRL[2] CSI2_A
CSI2_B	ISS_CLKCTRL[3] CSI2_B
CSI2_C	ISS_CLKCTRL[6] CSI2_C
CCP2	ISS_CLKCTRL[4] CCP2
BYS_A	ISS_CLKCTRL[5] BYS_A
BYS_B	ISS_CLKCTRL[7] BYS_B
ISS interconnect BTE CBUFF TCTRL	These modules cannot be switched off individually. They are required for any processing performed by SIMCOP because they are on the main data path. However, they support autogating to reduce power consumption when activity is low.

When the clock of a submodule is cut and an interface bridge request for this module is received from the ISS configuration interconnect, the ISS clock manager temporarily enables the module clock to handle the access properly.

All ISS submodules are off after reset; software must enable them before they can be used.

8.1.2.3 ISS Reset

The ISS can accept a general software reset, propagated through all the hierarchy. This reset can be done to initialize the module and has the same effect as the hardware reset.

1. Set the ISS_HL_SYSCONFIG[0] SOFTRESET bit to 1.
2. Read the ISS_HL_SYSCONFIG[0] SOFTRESET bit to check whether it equals 0, which means the reset occurred.

If after five reads, ISS_HL_SYSCONFIG[0] SOFTRESET still returns 1, it can be assumed that an error occurred during the reset stage.

A software reset must not reset the power manager protocols (must not reset the IDLE and STANDBY generic IPs).

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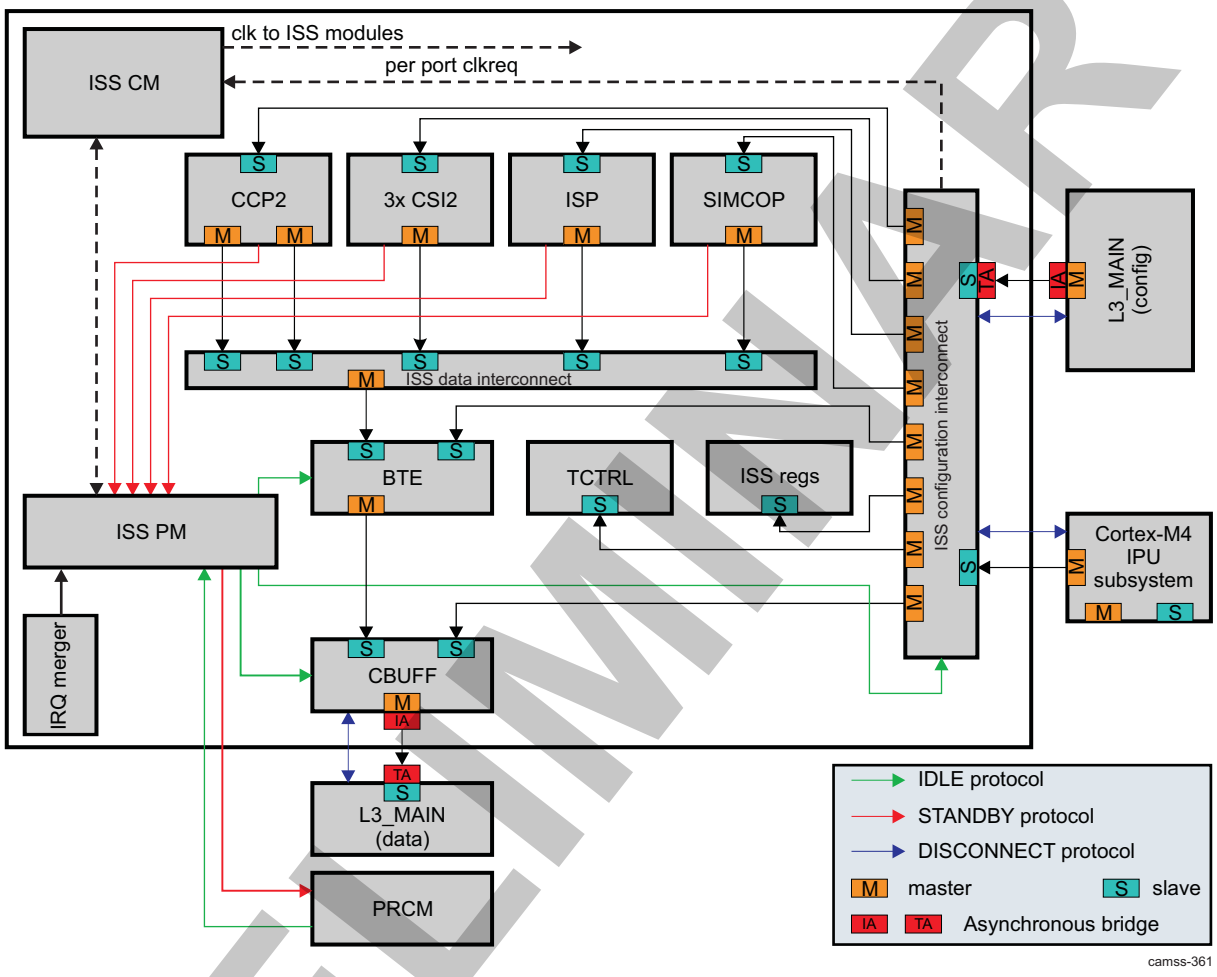
8.1.2.4 ISS Power Management

8.1.2.4.1 ISS Power-Management Infrastructure Overview

Figure 8-4 is an overview of the ISS power management.

Figure 8-4. ISS Power Management



NOTE: For power savings, the PRCM module can request idle mode from the ISS. When the ISS is not functional, software must decide when the PRCM module can send the request. For more information, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management.*

8.1.2.4.2 ISS STANDBY Mechanism

The power manager receives STANDBY information from the CCP2, CSI2_A, CSI2_B, CSI2_C, ISP, and SIMCOP modules. These modules assert a standby signal when they have no more transactions to perform. The ISS power manager acknowledges by asserting a wait signal.

When those five modules are in standby mode, the ISS power manager initiates a STANDBY sequence for the ISS:

1. The ISS waits while the CCP2, CSI2_A, CSI2_B, CSI2_C, ISP, and SIMCOP MStandby is asserted.
2. The ISS power manager acknowledges by asserting the CCP2, CSI2_A, CSI2_B, CSI2_C, ISP, and SIMCOP MWait signal.
3. The ISS initiators assert only the MStandBy signal when they receive responses to all sent requests.

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Therefore, when all initiators have asserted MStandBy, the ISS interconnect has no more pending traffic (although configurable, only nonposted writes must be used for error reporting).

4. The ISS power manager sends an IDLE request to the BTE. This IDLE request is used to drain BTE data. It does not affect the configuration port.
5. The BTE drains all transactions.
6. The BTE acknowledges the IDLE request.
7. The ISS power manager sends an IDLE request to the CBUFF. This IDLE request is used to drain CBUFF data. It does not affect the configuration port.
8. CBUFF drains all transactions.
9. CBUFF disconnects the interface master port connected to the L3 interconnect.
10. CBUFF acknowledges the IDLE request.
11. The ISS power manager asserts the MStandBy signals connected to the system PRCM module.
12. The PRCM module acknowledges by asserting the MWait signal.

A functional standby transition can be aborted when one of the CCP2, CSI2_A, CSI2_B, CSI2_C, ISP, or SIMCOP modules deasserts the MStandBy signal. The corresponding MWait signal is deasserted only when the ISS interconnect, BTE, CBUFF, and ISS interface master port are ready to receive requests.

When one of the CCP2, CSI2_A, CSI2_B, CSI2_C, ISP, or SIMCOP modules must perform accesses to the ISS interface master port, it deasserts the MStandBy signal. The ISS power manager executes the following sequence to leave the STANDBY state:

1. The ISS power manager deasserts the MStandby signal.
2. The ISS waits until the PRCM module deasserts the MWait signal.
3. The ISS power manager requests CBUFF to go into functional mode.
4. CBUFF connects the interface port.
5. The ISS power manager requests the BTE to go into functional mode.
6. The ISS power manager waits until CBUFF and BTE acknowledge functional mode.
7. The ISS deasserts the MWait signal of the module requesting access.

Abort of the standby-to-functional mode transition is not supported. The ISS power manager completes the standby-to-functional transition and then allows a new functional-to-standby transition.

Typically, the MStandby signal is used for two purposes. Software chooses one of the following behaviors through PRCM configuration:

- During blanking periods: The ISS asserts the MStandBy signal between frames when it has no more data to send. The PRCM module can use this information to switch off the L3 interconnect and save some dynamic power. However, the PRCM module is not allowed to cut the ISS functional clock in that case, because it is needed to receive the next frame.
- For ISS shutdown: The ISS asserts MStandBy when it has no more transactions to perform. The PRCM module then initiates an IDLE sequence. Once the ISS acknowledges the transition into idle mode, the PRCM module can cut the ISS clock and power.

The internal standby mode can be reached only when CCP2, CSI2_A, CSI2_B, CSI2_C, SIMCOP, ISP, ISS data interconnect, BTE, and CBUFF are in IDLE or STANDBY state. Choosing no-idle or no-standby mode for any of these modules prevents the ISS from going into STANDBY state.

Four modes for standby control are supported, configured through the ISS_HL_SYSCONFIG [5:4] STANDBYMODE register bit-field:

- Smart-standby-wakeup mode [STANDBYMODE = 0x3]: This is the mode normally used. When in this mode, the ISS asserts the MStandBy signal when the MStandBy of all ISS internal initiators is asserted and the ISS data interconnect, BTE, and CBUFF are in IDLE state.
- Smart-standby mode (default) [STANDBYMODE = 0x2]: The ISS has no wake-up event. This mode is equivalent to smart-standby-wakeup mode.
- Force-standby mode [STANDBYMODE = 0x0]: This is a backup mode intended to be used only if smart-standby mode is bugged. When in this mode, the ISS asserts MStandBy unconditionally. Software must ensure that the ISS is in a correct quiet state before programming this mode.

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- No-standby mode [STANDBYMODE = 0x1]: This is a backup mode intended to be used only if smart-standby mode is bugged. When in this mode, the ISS never asserts the MStandBy signal.

8.1.2.4.3 ISS IDLE Mechanism

The PRCM module can request the ISS to go into IDLE state when the ISS has asserted its MStandBy output.

In a normal case, software must ensure that the ISS is in a quiet state before allowing the PRCM module to send an IDLE request to the ISS:

- The ISS has no more traffic to generate.
- The ISS cannot generate any new interrupts.
- The ISS has no pending interrupts.

When an IDLE request is received from the PRCM module, the ISS power manager verifies that the ISS MWait input has been asserted and that all ISS interrupt outputs are deasserted. It then starts the STANDBY-to-IDLE transition:

1. Send IDLE request to the ISS configuration interconnect.
2. The ISS configuration interconnect requests disconnection of both ISS interface slave ports. Disconnection is done by the master:
   - It stops accepting new requests and drains currently ongoing ones.
   - It waits for completion of all ongoing transactions.
3. The ISS configuration interconnect acknowledges the IDLE transition.
4. The ISS power manager acknowledges the IDLE request from the PRCM module.
5. The PRCM module can cut the ISS clock and power.

The PRCM module first enables the ISS power and clock before requesting the ISS to go into functional state by deasserting the SIdleReq signal. The ISS power manager then executes the wake-up sequence:

1. Request the ISS interconnect to go into functional state.
2. The ISS interconnect connects the ISS slave ports.
3. The ISS interconnect acknowledges transition into functional mode.
4. The ISS power manager acknowledges transition into functional mode (ISS output SIdleAck = 00).

Four modes for IDLE control are supported, controlled through the ISS_HL_SYSCONFIG[3:2] IDLEMODE register bit-field:

- Smart-idle-wakeup mode [IDLEMODE = 0x3]: This is the mode normally used. When in this mode, the ISS acknowledges a request to go idle from the power manager after having performed all hardware operations necessary for the IAF to be in a correct quiet state.
- Smart-idle mode (default) [IDLEMODE = 0x2]: This is equivalent to smart-idle-wakeup mode.
- Force-idle mode [IDLEMODE = 0x0]: This is a backup mode intended to be used only if smart-idle mode is bugged. When in this mode, the ISS acknowledges a request to go idle from the power manager with no hardware condition. Software must ensure that the ISS is in a correct quiet state before requesting a force-idle transition.
- No-idle mode [IDLEMODE = 0x1]: When in this mode, the ISS disregards any request to go idle from the power manager.

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8.1.3 ISS Register Manual

8.1.3.1 ISS Instance Summary

Table 8-16 is the ISS instance.

Table 8-16. ISS Instance Summary

Module Name	Module Base Address	Size
ISS_TOP	0x5200 0000	256 bytes

NOTE: This section contains the ISS TOP registers only. For submodule register details, see the register manual of the particular submodule.

8.1.3.2 ISS Registers

8.1.3.2.1 ISS TOP Register Summary

Table 8-17 summarizes the ISS TOP register mapping.

Table 8-17. ISS TOP Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_TOP Base Address
ISS_HL_REVISION	R	32	0x0000 0000	0x5200 0000
RESERVED	R	32	0x0000 0004	0x5200 0004
ISS_HL_SYSCONFIG	RW	32	0x0000 0010	0x5200 0010
RESERVED	RW	32	0x0000 001C	0x5200 001C
ISS_HL_IRQSTATUS_RAW_i (1)	RW	32	0x0000 0020 + (0x10 * i)	0x5200 0020 + (0x10 * i)
ISS_HL_IRQSTATUS_i (1)	RW	32	0x0000 0024 + (0x10 * i)	0x5200 0024 + (0x10 * i)
ISS_HL_IRQENABLE_SET_i (1)	RW	32	0x0000 0028 + (0x10 * i)	0x5200 0028 + (0x10 * i)
ISS_HL_IRQENABLE_CLR_i (1)	RW	32	0x0000 002C + (0x10 * i)	0x5200 002C + (0x10 * i)
ISS_CTRL	RW	32	0x0000 0080	0x5200 0080
ISS_CLKCTRL	W	32	0x0000 0084	0x5200 0084
ISS_CLKSTAT	R	32	0x0000 0088	0x5200 0088
ISS_PM_STATUS	R	32	0x0000 008C	0x5200 008C
ISS_BYS	RW	32	0x0000 0090	0x5200 0090

(1) i = 0 to 5

8.1.3.2.2 ISS TOP Register Description

through describe the ISS TOP registers.

Table 8-18. ISS_HL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 0000	**Instance**	ISS_TOP
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 8-19. Register Call Summary for Register ISS_HL_REVISION

ISS Overview
- ISS TOP Register Summary: [0]

Table 8-20. ISS_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5200 0010	**Instance**	ISS_TOP
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		IDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBYMODE	Master interface power management, standby/Wait control 0x0: Force-standby. MStandby is asserted unconditionally. 0x1: No-standby. MStandby is never asserted. 0x3: Smart-standby Wake up 0x2: Smart-standby	RW	0x2
3:2	IDLEMODE	IDLE protocol configuration 0x0: Force-idle 0x1: No-idle 0x3: Smart-idle Wake up 0x2: Smart-idle	RW	0x2
1	RESERVED		R	0
0	SOFTRESET	Software reset. Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0

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Table 8-21. Register Call Summary for Register ISS_HL_SYSCONFIG

ISS Overview

- ISS Reset: [0] [1] [2]
- ISS STANDBY Mechanism: [3]
- ISS IDLE Mechanism: [4]
- ISS TOP Register Summary: [5]

Table 8-22. ISS_HL_IRQSTATUS_RAW_i

Address Offset	0x0000 0020 + (0x10 * i)	**Index**	i = 0 to 5
Physical Address	0x5200 0020 + (0x10 * i)	**Instance**	ISS_TOP
Description	Per-event raw interrupt status vector, line 0. Raw status is set even if event is not enabled by setting the ISS_HL_IRQENABLE_SET_i register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											BYS_B_IRQ	CSIC_IRQ	BYS_A_IRQ	HS_VS_IRQ	CCP2_IRQ8	SIMCOP_IRQ3	SIMCOP_IRQ2	SIMCOP_IRQ1	SIMCOP_IRQ0	BTE_IRQ	CBUFF_IRQ	CCP2_IRQ3	CCP2_IRQ2	CCP2_IRQ1	CCP2_IRQ0	CSIB_IRQ	CSIA_IRQ	ISP_IRQ3	ISP_IRQ2	ISP_IRQ1	ISP_IRQ0

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	BYS_B_IRQ	Event generated by BYS_B Read 0x1: Event pending Read 0x0: No event pending	R	0
19	CSIC_IRQ	Event generated by the CSI2_C receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
18	BYS_A_IRQ	Event generated by BYS_A Read 0x1: Event pending Read 0x0: No event pending	R	0
17	HS_VS_IRQ	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal (after the video port mux). The rising or falling edge and the HS or VS signal selection is chosen with the ISS_CTRL[1:0] SYNC_DETECT bit field. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW	0
16	CCP2_IRQ8	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
15	SIMCOP_IRQ3	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No event pending	R	0
14	SIMCOP_IRQ2	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No event pending	R	0

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Bits	Field Name	Description	Type	Reset
13	SIMCOP_IRQ1	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No event pending	R	0
12	SIMCOP_IRQ0	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No event pending	R	0
11	BTE_IRQ	Event generated by the burst translation engine Read 0x1: Event pending Read 0x0: No event pending	R	0
10	CBUFF_IRQ	Event generated by the circular buffer Read 0x1: Event pending Read 0x0: No event pending	R	0
9	CCP2_IRQ3	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
8	CCP2_IRQ2	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
7	CCP2_IRQ1	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
6	CCP2_IRQ0	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
5	CSIB_IRQ	Event generated by the CSI2_B receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
4	CSIA_IRQ	Event generated by the CSI2_A receiver Read 0x1: Event pending Read 0x0: No event pending	R	0
3	ISP_IRQ3	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No event pending	R	0
2	ISP_IRQ2	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No event pending	R	0
1	ISP_IRQ1	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No event pending	R	0
0	ISP_IRQ0	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No event pending	R	0

Table 8-23. Register Call Summary for Register ISS_HL_IRQSTATUS_RAW_i

ISS Overview

- ISS Interrupts: [0]
- ISS TOP Register Summary: [1]

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Table 8-24. ISS_HL_IRQSTATUS_i

Address Offset	0x0000 0024 + (0x10 * i)	**Index**	i = 0 to 5
Physical Address	0x5200 0024 + (0x10 * i)	**Instance**	ISS_TOP
Description	Per-event "enabled" interrupt status vector, line 0. Enabled status is not set unless event is enabled by setting the ISS_HL_IRQENABLE_SET_i register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											BYS_B_IRQ	CSIC_IRQ	BYS_A_IRQ	HS_VS_IRQ	CCP2_IRQ8	SIMCOP_IRQ3	SIMCOP_IRQ2	SIMCOP_IRQ1	SIMCOP_IRQ0	BTE_IRQ	CBUFF_IRQ	CCP2_IRQ3	CCP2_IRQ2	CCP2_IRQ1	CCP2_IRQ0	CSIB_IRQ	CSIA_IRQ	ISP_IRQ3	ISP_IRQ2	ISP_IRQ1	ISP_IRQ0

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	BYS_B_IRQ	Event generated by BYS_B Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
19	CSIC_IRQ	Event generated by the CSI2_C receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
18	BYS_A_IRQ	Event generated by BYS_A Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
17	HS_VS_IRQ	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal (after the video port mux). The rising or falling edge and the HS or VS signal selection is chosen with the ISS_CTRL[1:0] SYNC_DETECT bit field. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toSet	0
16	CCP2_IRQ8	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
15	SIMCOP_IRQ3	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
14	SIMCOP_IRQ2	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
13	SIMCOP_IRQ1	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
12	SIMCOP_IRQ0	Event generated by SIMCOP Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0

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Bits	Field Name	Description	Type	Reset
11	BTE_IRQ	Event generated by the burst translation engine Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
10	CBUFF_IRQ	Event generated by the circular buffer Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
9	CCP2_IRQ3	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
8	CCP2_IRQ2	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
7	CCP2_IRQ1	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
6	CCP2_IRQ0	Event generated by the CCP2 receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
5	CSIB_IRQ	Event generated by the CSI2_B receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
4	CSIA_IRQ	Event generated by the CSI2_A receiver Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
3	ISP_IRQ3	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
2	ISP_IRQ2	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
1	ISP_IRQ1	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0
0	ISP_IRQ0	Combined interrupt event provided by the ISP. Read 0x1: Event pending Read 0x0: No (enabled) event pending	R	0

Table 8-25. Register Call Summary for Register ISS_HL_IRQSTATUS_i

ISS Overview

- ISS Interrupts: [0] [1]
- ISS TOP Register Summary: [2]

Table 8-26. ISS_HL_IRQENABLE_SET_i

Address Offset	0x0000 0028 + (0x10 * i)	**Index**	i = 0 to 5
Physical Address	0x5200 0028 + (0x10 * i)	**Instance**	ISS_TOP
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding ISS_HL_IRQENABLE_CLR_i register bit.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											BYS_B_IRQ	CSIC_IRQ	BYS_A_IRQ	HS_VS_IRQ	CCP2_IRQ8	SIMCOP_IRQ3	SIMCOP_IRQ2	SIMCOP_IRQ1	SIMCOP_IRQ0	BTE_IRQ	CBUFF_IRQ	CCP2_IRQ3	CCP2_IRQ2	CCP2_IRQ1	CCP2_IRQ0	CSIB_IRQ	CSIA_IRQ	ISP_IRQ3	ISP_IRQ2	ISP_IRQ1	ISP_IRQ0

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	BYS_B_IRQ	Event generated by BYS_B Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
19	CSIC_IRQ	Event generated by the CSI2_C receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
18	BYS_A_IRQ	Event generated by BYS_A Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
17	HS_VS_IRQ	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal (after the video port mux). The rising or falling edge and the HS or VS signal selection is chosen with the ISS_CTRL[1:0] SYNC_DETECT bit field. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
16	CCP2_IRQ8	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15	SIMCOP_IRQ3	Event generated by SIMCOP Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
14	SIMCOP_IRQ2	Event generated by SIMCOP Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
13	SIMCOP_IRQ1	Event generated by SIMCOP Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
12	SIMCOP_IRQ0	Event generated by SIMCOP Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
11	BTE_IRQ	Event generated by the burst translation engine Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
10	CBUFF_IRQ	Event generated by the circular buffer Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
9	CCP2_IRQ3	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
8	CCP2_IRQ2	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
7	CCP2_IRQ1	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
6	CCP2_IRQ0	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
5	CSIB_IRQ	Event generated by the CSI2_B receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
4	CSIA_IRQ	Event generated by the CSI2_A receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
3	ISP_IRQ3	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
2	ISP_IRQ2	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
1	ISP_IRQ1	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
0	ISP_IRQ0	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

Table 8-27. Register Call Summary for Register ISS_HL_IRQENABLE_SET_i

ISS Overview

- ISS Interrupts: [0]
- ISS TOP Register Summary: [1]
- ISS TOP Register Description: [2] [3] [4]

Table 8-28. ISS_HL_IRQENABLE_CLR_i

Address Offset	0x0000 002C + (0x10 * i)	**Index**	i = 0 to 5
Physical Address	0x5200 002C + (0x10 * i)	**Instance**	ISS_TOP
Description	Per-event interrupt enable bit vector Write 1 to clear (disable interrupt). Readout equal to corresponding ISS_HL_IRQENABLE_SET_i register bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											BYS_B_IRQ	CSIC_IRQ	BYS_A_IRQ	HS_VS_IRQ	CCP2_IRQ8	SIMCOP_IRQ3	SIMCOP_IRQ2	SIMCOP_IRQ1	SIMCOP_IRQ0	BTE_IRQ	CBUFF_IRQ	CCP2_IRQ3	CCP2_IRQ2	CCP2_IRQ1	CCP2_IRQ0	CSIB_IRQ	CSIA_IRQ	ISP_IRQ3	ISP_IRQ2	ISP_IRQ1	ISP_IRQ0

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Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	BYS_B_IRQ	Event generated by BYS_B Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
19	CSIC_IRQ	Event generated by the CSI2_C receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
18	BYS_A_IRQ	Event generated by BYS_A Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
17	HS_VS_IRQ	HS or VS synchronization event. This event is triggered if a rising or falling edge is detected on the HS or VS signal (after the video port mux). The rising or falling edge and the HS or VS signal selection is chosen with the ISS_CTRL[1:0] SYNC_DETECT bit field. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
16	CCP2_IRQ8	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15	SIMCOP_IRQ3	Event generated by SIMCOP Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
14	SIMCOP_IRQ2	Event generated by SIMCOP Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
13	SIMCOP_IRQ1	Event generated by SIMCOP Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
12	SIMCOP_IRQ0	Event generated by SIMCOP Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
11	BTE_IRQ	Event generated by the BTE Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
10	CBUFF_IRQ	Event generated by the CBUFF Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
9	CCP2_IRQ3	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
8	CCP2_IRQ2	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
7	CCP2_IRQ1	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
6	CCP2_IRQ0	Event generated by the CCP2 receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
5	CSIB_IRQ	Event generated by the CSI2_B receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
4	CSIA_IRQ	Event generated by the CSI2_C receiver Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
3	ISP_IRQ3	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	ISP_IRQ2	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
1	ISP_IRQ1	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
0	ISP_IRQ0	Combined interrupt event provided by the ISP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

Table 8-29. Register Call Summary for Register ISS_HL_IRQENABLE_CLR_i

ISS Overview
- ISS Interrupts: [0]
- ISS TOP Register Summary: [1]
- ISS TOP Register Description: [2]

Table 8-30. ISS_CTRL

Address Offset	0x0000 0080		
Physical Address	0x5200 0080	**Instance**	ISS_TOP
Description	ISS control register		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2	1 0
CSI2_B_TAG_CNT	CSI2_A_TAG_CNT	CCP2W_TAG_CNT	CCP2R_TAG_CNT	RESERVED	CSI2_C_TAG_CNT	RESERVED	INPUT_SEL2	ISS_CLK_DIV	INPUT_SEL	SYNC_DETECT

Bits	Field Name	Description	Type	Reset
31:28	CSI2_B_TAG_CNT	Defines the maximum number of tags that could be used by the CSI2_B write bridge. Note: Tag count must be set to 16 for best performance.	RW	0x0
27:24	CSI2_A_TAG_CNT	Defines the maximum number of tags that could be used by the CSI2_A write bridge. Note: Tag count must be set to 16 for best performance.	RW	0x0
23:20	CCP2W_TAG_CNT	Defines the maximum number of tags that could be used by the CCP2 write bridge Note: Tag count must be set to 16 for best performance.	RW	0x0
19:16	CCP2R_TAG_CNT	Defines the maximum number of tags that could be used by the CCP2 read bridge Note: Tag count must be set to 16 for best performance.	RW	0x0
15:13	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
12:9	CSI2_C_TAG_CNT	Defines the maximum number of tags that could be used by the CSI2_C write bridge.	RW	0x0
8	RESERVED		R	0
7:6	INPUT_SEL2	Selects ISP input 0x0: Input selected by the [3:2] INPUT_SEL register bit-field in this register 0x1: CSI2_C 0x3: reserved 0x2: reserved	RW	0x0
5:4	ISS_CLK_DIV	ISS functional clock division CLK refers to the input clock provided to the ISS. FCLK is the functional clock provided to ISS top level and submodules. CFGCLK is the clock used for the configuration network. 0x0: FCLK=CLK CFGCLK=CLK/2 0x1: FCLK=CLK/2 CFGCLK=CLK/4 0x3: Reserved 0x2: FCLK=CLK/4 CFGCLK=CLK/8	RW	0x0
3:2	INPUT_SEL	Selects ISP input 0x0: CSI2_A 0x1: CSI2_B 0x2: CCP2 0x3: Parallel interface	RW	0x0
1:0	SYNC_DETECT	Chooses among rising and falling edge for the HS_VS_IRQ synchronization event 0x0: HS falling edge 0x1: HS raising edge 0x3: VS raising edge 0x2: VS falling edge	RW	0x0

Table 8-31. Register Call Summary for Register ISS_CTRL

ISS Overview

- ISS Clock Domains: [0]
- ISS TOP Register Summary: [2]
- ISS TOP Register Description: [3] [4] [5] [6]

Table 8-32. ISS_CLKCTRL

Address Offset	0x0000 0084		
Physical Address	0x5200 0084	**Instance**	ISS_TOP
Description	ISS clock control register. Use to enable/disable the interface and functional clock of ISS submodules.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VPORT3_CLK	VPORT2_CLK	VPORT1_CLK	VPORT0_CLK	VPORT4_CLK	RESERVED	RESERVED																		BYS_B	CSI2_C	BYS_A	CCP2	CSI2_B	CSI2_A	ISP	SIMCOP

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Bits	Field Name	Description	Type	Reset
31	VPORT3_CLK	Enables the pixel clock from the parallel interface 0x0: Disabled 0x1: Enabled	RW	1
30	VPORT2_CLK	Enables the pixel clock from the CCP2 protocol engine 0x0: Disabled 0x1: Enabled	RW	1
29	VPORT1_CLK	Enables the pixel clock from the CSI2_B protocol engine 0x0: Disabled 0x1: Enabled	RW	1
28	VPORT0_CLK	Enables the pixel clock from the CSI2_A protocol engine 0x0: Disabled 0x1: Enabled	RW	1
27	VPORT4_CLK	Enables the pixel clock from the CSI2_C protocol engine 0x0: Disabled 0x1: Enabled	RW	1
26	RESERVED		R	1
25:8	RESERVED		R	0x0 0000
7	BYS_B	BYS_B Write 0x0: Request shutdown of the sub-module. No effect if the sub-module clock is already off. Write 0x1: Request enable of the sub-module. No effect if the sub-module clock is already on.	W	0
6	CSI2_C	CSI2_C Write 0x0: Request shutdown of the sub-module. No effect if the sub-module clock is already off. Write 0x1: Request enable of the sub-module. No effect if the sub-module clock is already on.	W	0
5	BYS_A	BYS_A Write 0x0: Request shutdown of the sub-module. No effect if the sub-module clock is already off. Write 0x1: Request enable of the sub-module. No effect if the sub-module clock is already on.	W	0
4	CCP2	CCP2 Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.	W	0
3	CSI2_B	CSI2_B Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.	W	0
2	CSI2_A	CSI2_A Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.	W	0
1	ISP	ISP Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.	W	0

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Bits	Field Name	Description	Type	Reset
0	SIMCOP	SIMCOP Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.	W	0

Table 8-33. Register Call Summary for Register ISS_CLKCTRL

ISS Overview

- ISS Clock Domains: [0] [1]
- ISS Clocks: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
- ISS TOP Register Summary: [13]

Table 8-34. ISS_CLKSTAT

Address Offset	0x0000 0088		
Physical Address	0x5200 0088	**Instance**	ISS_TOP
Description	ISS clock status register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VPORT3_CLK	VPORT2_CLK	VPORT1_CLK	VPORT0_CLK	VPORT4_CLK	RESERVED	RESERVED																		BYS_B	CSI2_C	BYS_A	CCP2	CSI2_B	CSI2_A	ISP	SIMCOP

Bits	Field Name	Description	Type	Reset
31	VPORT3_CLK	Status of the pixel clock from the parallel interface Read 0x1: Enabled Read 0x0: Disabled	R	1
30	VPORT2_CLK	Status of the pixel clock from the CCP2 protocol engine Read 0x1: Enabled Read 0x0: Disabled	R	1
29	VPORT1_CLK	Status of the pixel clock from the CSI2_B protocol engine Read 0x1: Enabled Read 0x0: Disabled	R	1
28	VPORT0_CLK	Status of the pixel clock from the CSI2_A protocol engine Read 0x1: Enabled Read 0x0: Disabled	R	1
27	VPORT4_CLK	Status of the pixel clock from the CSI2_C protocol engine Read 0x1: Enabled Read 0x0: Disabled	R	1
26	RESERVED		R	1
25:8	RESERVED		R	0x0 0000
7	BYS_B	BYS_B Read 0x1: The sub-module is on Read 0x0: The sub-module is off	R	0
6	CSI2_C	CSI2_C Read 0x1: The sub-module is on Read 0x0: The sub-module is off	R	0

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Bits	Field Name	Description	Type	Reset
5	BYS_A	BYS_A Read 0x1: The sub-module is on Read 0x0: The sub-module is off	R	0
4	CCP2	CCP2 Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
3	CSI2_B	CSI2_B Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
2	CSI2_A	CSI2_A Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
1	ISP	ISP Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
0	SIMCOP	SIMCOP Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0

Table 8-35. Register Call Summary for Register ISS_CLKSTAT

ISS Overview

- ISS Clocks: [0] [1] [2]
- ISS TOP Register Summary: [3]

Table 8-36. ISS_PM_STATUS

Address Offset	0x0000 008C		
Physical Address	0x5200 008C	**Instance**	ISS_TOP
Description	ISS power manager status register. Software could know what modules are in functional or STANDBY/IDLE state. This feature could be particularly useful to debug when ISS does not go into STANDBY mode		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSI2_C_PM		CBUFF_PM		BTE_PM		SIMCOP_PM		ISP_PM		CCP2_PM		CSI2_B_PM		CSI2_A_PM	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	CSI2_C_PM	Power status of the CSI2_C module Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0
13:12	CBUFF_PM	Power status of the CBUFF. Read 0x2: Functional Read 0x1: Transition Read 0x0: Idle	R	0x0

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Bits	Field Name	Description	Type	Reset
11:10	BTE_PM	Power status of the BTE. Read 0x2: Functional Read 0x1: Transition Read 0x0: Idle	R	0x0
9:8	SIMCOP_PM	Power status of the SIMCOP. Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0
7:6	ISP_PM	Power status of the ISP. Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0
5:4	CCP2_PM	Power status of the CCP2. Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0
3:2	CSI2_B_PM	Power status of the CSI2_B module Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0
1:0	CSI2_A_PM	Power status of the CSI2_A module Read 0x2: Functional Read 0x1: Transition Read 0x0: Standby	R	0x0

Table 8-37. Register Call Summary for Register ISS_PM_STATUS

ISS Overview

- ISS TOP Register Summary: [0]

Table 8-38. ISS_BYS

Address Offset	0x0000 0090		
Physical Address	0x5200 0090	**Instance**	ISS_TOP
Description	BYS IO selection		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	RESERVED	CSI2C_IN	RESERVED	CSI2B_IN	RESERVED	CSI2A_IN	RESERVED	BYSB_IN				RESERVED	BYSA_IN		

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x0 0000
14	RESERVED		R	0
13	RESERVED		R	0
12	CSI2C_IN	Selects input of CSI2_C BYS input 0x0: BYS_A 0x1: BYS_B	RW	0

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Bits	Field Name	Description	Type	Reset
11	RESERVED		R	0
10	CSI2B_IN	Selects input of CSI2_B BYS input 0x0: BYS_A 0x1: BYS_B	RW	0
9	RESERVED		R	0
8	CSI2A_IN	Selects input of CSI2_A BYS input 0x0: BYS_A 0x1: BYS_B	RW	0
7	RESERVED		R	0
6:4	BYSB_IN	Selects BYS_B input 0x0: Disabled 0x1: CSI2_A 0x3: CSI2_C 0x4: Reserved 0x2: CSI2_B	RW	0x0
3	RESERVED		R	0
2:0	BYSA_IN	Selects BYS_A input 0x0: Disabled 0x1: CSI2_A 0x3: CSI2_C 0x4: Reserved 0x2: CSI2_B	RW	0x0

Table 8-39. Register Call Summary for Register ISS_BYS

ISS Overview

- ISS TOP Register Summary: [0]

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8.2 ISS Interfaces

8.2.1 ISS Interfaces Overview

Along with the submodules, the ISS has three serial camera interfaces (primary, secondary and tertiary) and a parallel interface within the ISS boundary. The primary serial interface (CSI2_A) supports MIPI® CSI2 protocol with four data lanes, the secondary serial interface (CSI2_B/CCP2) supports CSI2 protocol with two data lanes or CCP2 protocol, and the third serial interface (CSI2_C/CCP2) supports CSI2 protocol with one data lane or CCP2 protocol. The parallel interface (CPI) supports up to 16 data lanes. All interfaces can use the image signal processor (ISP), but not concurrently. When one interface uses the ISP, the other must send data to memory. However, the ISP can still be used to process this data in memory-to-memory. Time multiplex processing is also possible.

Figure 8-5 shows the ISS interfaces and interconnects.

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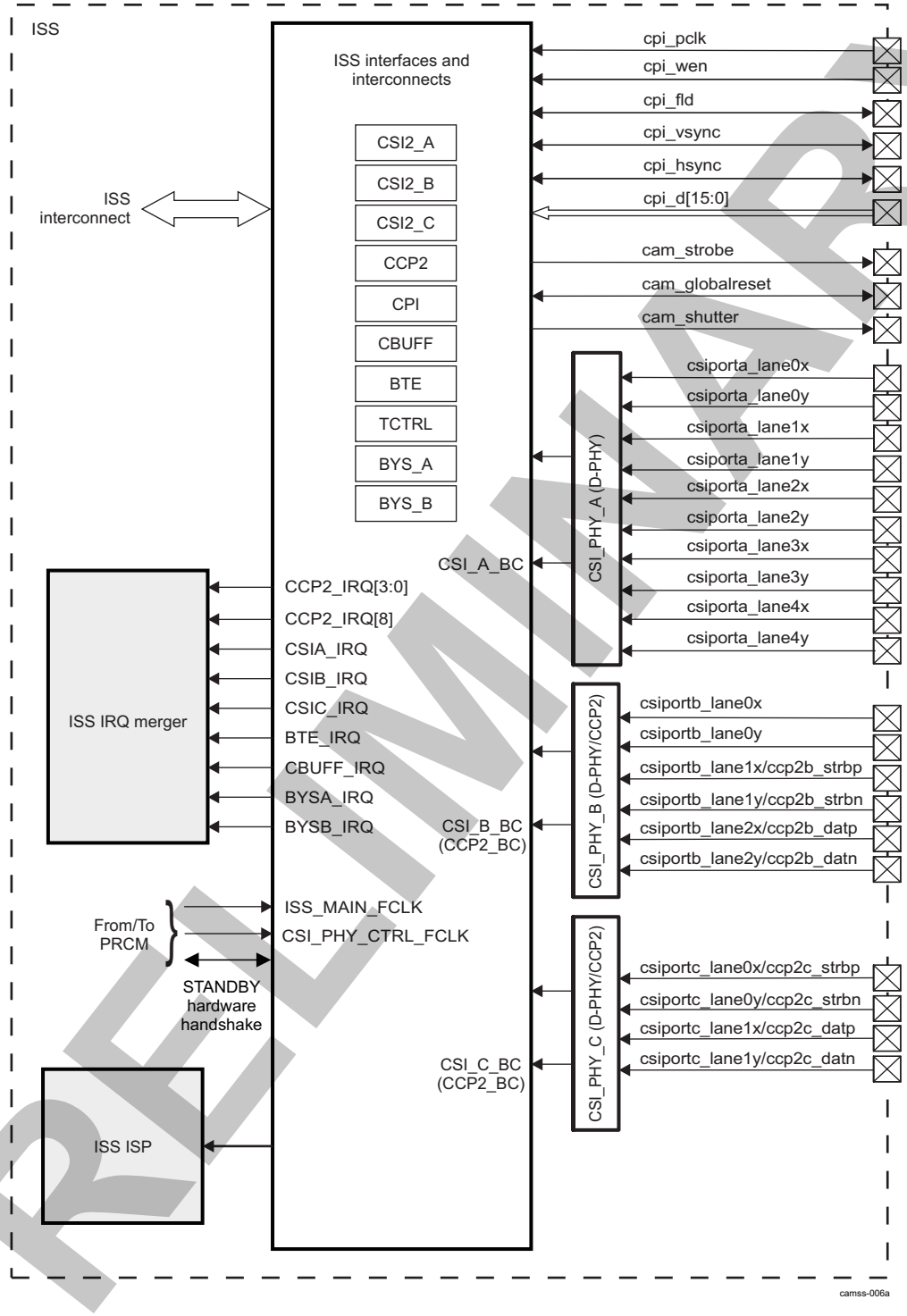
Figure 8-5. ISS Interfaces and Interconnects Highlight



8.2.1.1 ISS Interface Features

The camera subsystem supports the following features:

- System interfaces and interconnects:
  - Two 32-bit-wide configuration interfaces:
    - Interface to Cortex™-M4 microprocessor unit (IPU): Synchronous to the functional clock

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- Interface to Cortex™-A15 MPU and system direct memory access (DMA_SYSTEM): Asynchronous from the functional clock

– 128-bit-wide data interface to level 3 (L3_MAIN) interconnect: Asynchronous from the functional clock
  - Shared interface level 2 (L2) in IVA-HD module for hardware encoding
  - Outside connection using the L3_MAIN interconnect through the TILER to the synchronous dynamic random access memory (SDRAM) controller (SDRC), which acts as the primary interface between the SDRAM and the ISS functional block
– The ISS has a local interconnect that connects all modules inside the ISS
– BTE:
  - Tightly coupled with the TILER to support efficient rotation
– CBUFF:
  - Maps a linear space into a circular buffer
  - The buffer is physically located in system memory.
– TCTRL:
  - Camera global reset control
  - Control signal generation for flash prestrobe and strobe
– Two BYS modules:
  - Stabilization statistics collection (piece wise interpolated gamma correction, polynomial lens shading correction)
  - Down scaler (horizontal and vertical cropping, defect pixel correction)

- Camera interfaces:

– Three CSI2 camera interfaces: CSI2_A (primary), CSI2_B (secondary) and CSI2_C (tertiary)
  - Transfer pixels and data received by the three digital physical layer receivers (CSI_PHY_A/B/C in D-PHY mode) to the system memory or to the ISP
  - Use unidirectional data link
  - CSI2_A supports four configurable data links in addition to the clock signaling
  - CSI2_B supports two configurable data links in addition to the clock signaling

NOTE: The cameras on the CSI2_A and CSI2_B interfaces must be of the same type to form a dual camera set supporting half-resolution stereoscopic applications.

  - CSI2_C supports one configurable data link in addition to the clock signaling
  - Maximum data rate of 1.5 Gbps per data lane
  - Data merger for 2-, 3-, or 4-data lane configuration
  - Error detection and correction by the protocol engine
  - Direct memory access (DMA) engine integrated with dedicated first in first out (FIFO)
  - One-dimensional (1D) and two-dimensional (2D) addressing mode
  - Burst support
  - Streaming burst support (64- or 32-bit)
  - Eight contexts to support eight dedicated configurations of virtual channel ID and data types
  - Ping-pong mechanism for double-buffering
  - All primary and secondary MIPI-defined formats are supported.
  - Conversion of the RGB formats
  - On-the-fly differential pulse code modulation (DPCM) decompression
  - On-the-fly image cropping and A-law/DPCM compression
  - Configuration of the complex input/output (I/O) physical layers (CSI_PHY_A/B/C):
    - MIPI D-PHY compliant receiver PHY solution (D-PHY mode)

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- SMIA CCP2 compatible receiver PHY solution (CCP2 mode)

– One CCP2 camera interface
  - Four logical channels
  - Transfer pixels and data received by two complex I/O physical layers (CSI_PHY_B/C in CCP2 mode) to the system memory or the ISP
  - Use unidirectional data link
  - Maximum data rate of 650 Mbps
  - DMA engine integrated with dedicated FIFO
  - 1D and 2D addressing mode
  - False synchronization code protection
  - Ping-pong mechanism for double-buffering
  - RGB, RAW, YUV, and JPEG formats supported
  - On-the-fly DPCM decompression
  - On-the-fly image cropping and A-Law/DPCM compression
– One Parallel interface (CPI)
  - 8/12/16 bits wide
  - Up to 148.5 MPix/s
  - BT656 and SYNC mode (HS, VS, FIELD, WEN)
– System memory data read back port (supported by the CCP2 protocol engine)
  - RAW 6, 7, 8, 10, 12, 14, 16 formats supported
  - DPCM and A-law decompression
  - Supports image cropping for compressed or uncompressed data

NOTE: Rotated DPCM data is not supported.

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8.2.2 ISS Interfaces Environment

8.2.2.1 ISS Interfaces Signal Descriptions

Table 8-40 summarizes the ISS I/O signals and corresponding interface modes.

Table 8-40. ISS I/O Description

Signal Name	I/O[1]	Description	Serial Mode CCP2	Serial Mode CSI2	Parallel Mode CPI
cam_strobe	O	Flash strobe control signal	x	x	x
cam_shutter	O	Mechanical shutter control signal	x	x	x
cam_globalreset	I/O	Global reset release shutter signal	x	x	x
csiporta_lane0x	I	Serial CSI2_A mode: Differential clock positive input		x	
csiporta_lane0y	I	Serial CSI2_A mode: Differential clock negative input		x	
csiporta_lane1x	I	Serial CSI2_A mode: Differential data lane positive input		x	
csiporta_lane1y	I	Serial CSI2_A mode: Differential data lane negative input		x	
csiporta_lane2x	I	Serial CSI2_A mode: Differential data lane positive input		x	
csiporta_lane2y	I	Serial CSI2_A mode: Differential data lane negative input		x	
csiporta_lane3x	I	Serial CSI2_A mode: Differential data lane positive input		x	
csiporta_lane3y	I	Serial CSI2_A mode: Differential data lane negative input		x	
csiporta_lane4x	I	Serial CSI2_A mode: Differential data lane positive input		x	
csiporta_lane4y	I	Serial CSI2_A mode: Differential data lane negative input		x	
csiportb_lane0x	I	Serial CSI2_B mode: Differential clock lane positive input		x	
csiportb_lane0y	I	Serial CSI2_B mode: Differential clock lane negative input		x	
csiportb_lane1x	I	Serial CSI2_B mode: Differential data lane positive input		x	
csiportb_lane1y	I	Serial CSI2_B mode: Differential data lane negative input		x	
csiportb_lane2x	I	Serial CSI2_B mode: Differential data lane positive input		x	

(1) I = Input; O = Output

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Table 8-40. ISS I/O Description (continued)

Signal Name	I/O[1]	Description	Serial Mode CCP2	Serial Mode CSI2	Parallel Mode CPI
csiportb_lane2y	I	Serial CSI2_B mode: Differential data lane negative input		x	
csiportc_lane0x	I	Serial CSI2_C mode: Differential data lane positive input		x	
csiportc_lane0y	I	Serial CSI2_C mode: Differential data lane negative input		x	
csiportc_lane1x	I	Serial CSI2_C mode: Differential data lane positive input		x	
csiportc_lane1y	I	Serial CSI2_C mode: Differential data lane negative input		x	
ccp2b_strbp	I	Serial CCP2 mode: Differential clock positive input	x		
ccp2b_strbn	I	Serial CCP2 mode: Differential clock negative input	x		
ccp2b_datp	I	Serial CCP2 mode: Differential data positive input	x		
ccp2b_datn	I	Serial CCP2 mode: Differential data negative input	x		
ccp2c_strbp	I	Serial CCP2 mode: Differential clock positive input	x		
ccp2c_strbn	I	Serial CCP2 mode: Differential clock negative input	x		
ccp2c_datp	I	Serial CCP2 mode: Differential data positive input	x		
ccp2c_datn	I	Serial CCP2 mode: Differential data negative input	x		
cpi_pclk	I	Parallel mode pixel clock input			x
cpi_wen	I	Parallel mode write enable signal input			x
cpi_fld	I/O	Parallel mode pixel clock field signal			x
cpi_vsync	I/O	Parallel mode vertical frame synchronization			x
cpi_hsync	I/O	Parallel mode horizontal frame synchronization			x
cpi_data[15:0]	I	Parallel mode data lanes (16 signals)			x

NOTE: Lane polarity can be changed in complex I/O. For more information, see Section 8.2.2.2, *ISS Interface Modes*.

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NOTE: At least one data lane must be configured for using the CSI2_A and CSI2_B interfaces. The CSI2_C provides only one data lane. The signals are also configurable from the device Control Module. Thus, they are not required to be at a certain location to act as clock or data; this can be configured.

NOTE: The Parallel interface (CPI), CCP2, and CSI2_A/B/C interfaces share pins. Their modes are not supported as a pin configuration mux option. The modes are configured from the CSI_PHYs configured from the device Control Module (see Chapter 18, *Control Module*).

NOTE: The TCTRL cam_strobe and cam_shutter signals are available on a second pair of alternative device pads. See Chapter 18, *Control Module*, for more details.

8.2.2.2 ISS Interfaces Modes

The camera subsystem can manage a parallel interface and up to four serial image sensors. Depending on the configuration of the shared pins, four of the interfaces can be active at the same time. However, only one data flow can use the ISP. Moreover, if the parallel interface is used, the data from it goes to ISP and the other used interfaces must send it to memory. Figure 8-6 shows an example block diagram of the interface configuration (CSI2_C is not shown). Each serial port clock lane is configurable. The MIPI CSI2 protocol requires only a clock lane setup. The data lane configuration is optional. For more information, see Section 8.2.5.1.1, *ISS CSI2 Protocol and Data Format*.

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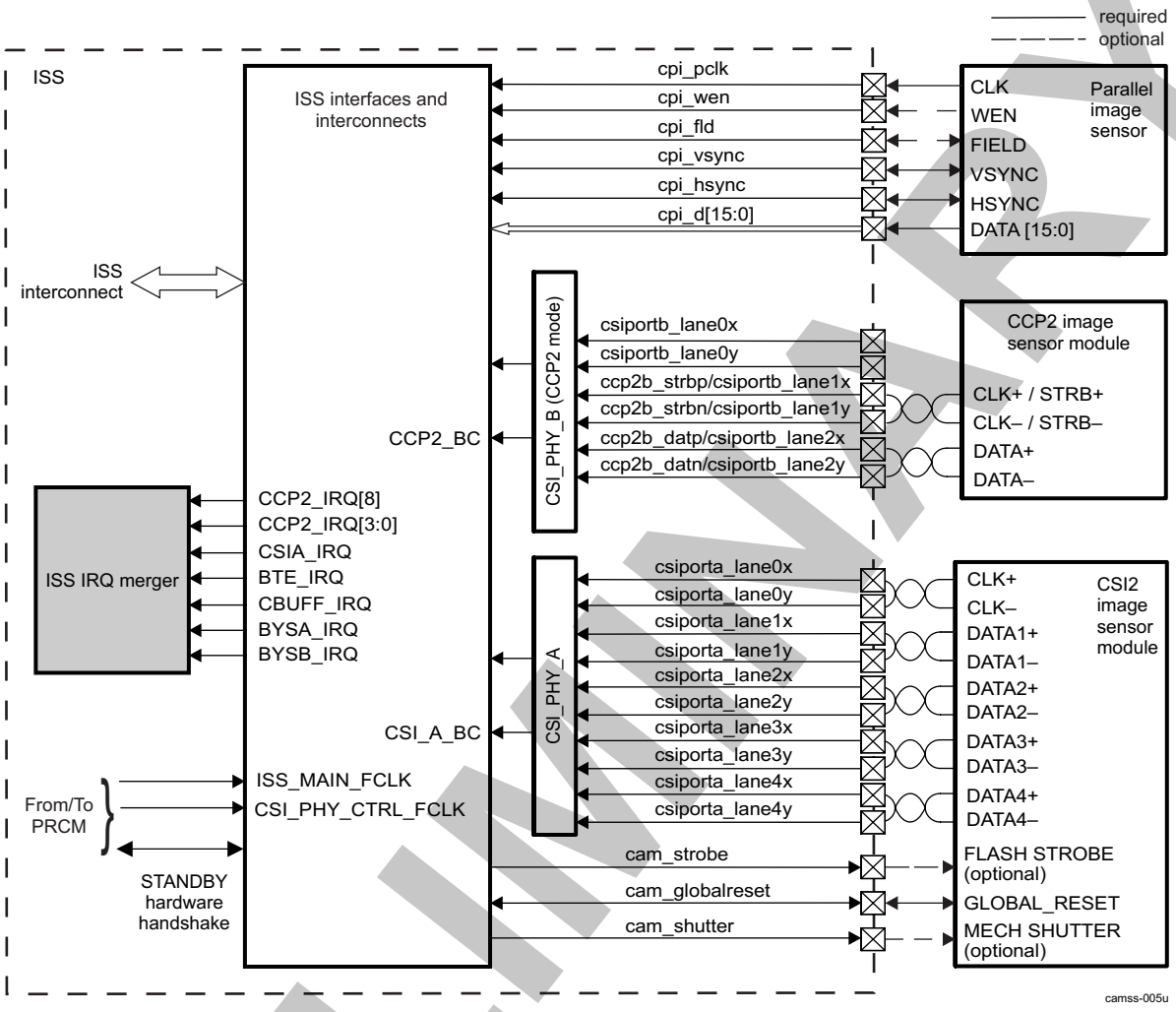
Figure 8-6. ISS CSI2_A, CSI2_B/CCP2 Serial Interface Configuration



NOTE: Depending on the needs, cam_strobe, cam_globalreset, and cam_shutter can be connected to the image sensor module rather than the CSI2 image sensor module.

NOTE: Dedicated Power, Reset, and Clock Management (PRCM) module pins for power and ground are provided for external sensors: vdda_csiporta, vdda_csiportb, vdda_csiportc, vssa_csiporta, vssa_csiportb and vssa_csiportc.

A graphical representation of the pins for connecting external sensors to the ISS shows a variety of connectivity configurations that are possible by setting the CSI_PHYs immediately before the receivers, and a variety of output paths, including some sensor data through the receivers to memory or the ISP. Table 8-41 lists some of the connectivity possibilities; the ISP can take only one input lane at a time. For more information about the operating properties and configuration of the CSI_PHY modules, see Section 8.2.3, *ISS CSI PHY*.

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Table 8-41. ISS Interfaces Connectivity Scheme Example Scenarios

	Serial Cameras Only			Serial + Parallel Cameras			
Camera 1	CSI2_B with 2 Data Lanes on CSI_PHY_B	CSI2_A with 4 Data Lanes on CSI_PHY_A	CSI2_A with 4 Data Lanes on CSI_PHY_A	CPI 16-bit	CPI 16-bit	CPI 12-bit	CPI 8-bit
Camera 2	CCP2 on CSI_PHY_C	CSI2_B with 2 Data Lanes on CSI_PHY_B	CSI2_B with 2 Data Lanes on CSI_PHY_B	CSI2_B with 2 Data Lanes on CSI_PHY_B	CCP2 on CSI_PHY_B	CSI2_B with 2 Data Lanes on CSI_PHY_B	CCP2 on CSI_PHY_C
Camera 3	-	CCP2 on CSI_PHY_C	CSI2_C with 1 Data Lanes on CSI_PHY_C	-	-	-	CSI2_B with 2 Data Lanes on CSI_PHY_B
Signals	Simultaneous	Simultaneous	Simultaneous	Simultaneous	Simultaneous	Simultaneous	Simultaneous
cam_strobe	x	x	x	x	x	x	x
cam_globalreset	x	x	x			x	x
cam_shutter	x	x	x	x	x	x	x
csiporta_lane0x		x	x				
csiporta_lane0y		x	x				
csiporta_lane1x		x	x				
csiporta_lane1y		x	x				
csiporta_lane2x		x	x				
csiporta_lane2y		x	x				
csiporta_lane3x		x	x				
csiporta_lane3y		x	x				
csiporta_lane4x		x	x				
csiporta_lane4y		x	x				
csiportb_lane0x	x	x	x	x		x	x
csiportb_lane0y	x	x	x	x		x	x
csiportb_lane1x / ccp2b_strbp	x	x	x	x	x	x	x
csiportb_lane1y / ccp2b_strbn	x	x	x	x	x	x	x
csiportb_lane2x / ccp2b_datp	x	x	x	x	x	x	x
csiportb_lane2y / ccp2b_datn	x	x	x	x	x	x	x
csiportc_lane0x / ccp2c_strbp	x	x	x				x
csiportc_lane0y / ccp2c_strbn	x	x	x				x
csiportc_lane1x / ccp2c_datp	x	x	x				x
csiportc_lane1y / ccp2c_datn	x	x	x				x
cpi_pclk				x	x	x	x
cpi_wen				x	x	x	x
cpi_fld				x	x	x	x
cpi_vsync				x	x	x	x

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Table 8-41. ISS Interfaces Connectivity Scheme Example Scenarios (continued)

	Serial Cameras Only			Serial + Parallel Cameras			
cpi_hsync				x	x	x	x
cpi_d[15:0]				x	x	x	x

NOTE: The ISP can take only one input at a time. The other inputs must go to memory and then be processed after the ISP processes the input that was received first.

NOTE: The cameras on the CSI2_A and CSI2_B interfaces must be of the same type to form a dual camera set supporting half-resolution stereoscopic applications.

In looking at the sample connections between the ISS through the receivers and external sensors, it is apparent that the lanes of the input can be adjusted for certain needs. For example, it is not necessary that the CSI2_A has four data lanes connected at the same time. The restriction is that CSI2_B is limited to two data lanes and CSI2_C to one data lane. Because CSI2_B/C and CCP2 share CSI_PHYs pins, they cannot be used simultaneously. CSI2_A, CSI2_B/CCP2 and CSI2_C/CCP2 can function at the same time by sending data to memory. In this manner, external sensors can be connected any way possible for best performance and results.

8.2.2.3 ISS Interfaces CPI Data Formats

8.2.2.3.1 ISS Interfaces CPI Generic Configuration Protocol and Data Format (8, 10, 12, 16 Bits)

The SYNC mode implements a generic parallel interface with the image sensor. The SYNC mode supports 8- to 16-bit-wide data signals.

In this configuration, no assumptions are made about the data format of pixels, but the dynamic range is limited to 8, 10, 12, and 16 bits (data can be pure Luminance for black and white sensor, RGB444, Bayer RGB, etc.). The pixel data is presented on cpi_data[15:0], where 1 pixel is sampled for every cpi_pclk rising edge (or falling edge, depending on the configuration of cpi_pclk polarity).

Additional pixel times between rows represent blanking periods. Active pixels are identified by a combination of two additional timing signals: horizontal synchronization (cpi_hsync) and vertical synchronization (cpi_vsync). During the image-sensor readout, these signals define when a row of valid data begins and ends, and when a frame starts and ends.

NOTE: For correct operation, the clock cpi_pclk must run during blanking periods (cpi_hsync and cpi_vsync inactive). The cpi_pclk must start before sending cpi_data[15:0] and start cpi_vsync and cpi_hsync.

Figure 8-7 and Figure 8-8 show the frame and data timing, based on synchronization signals in the parallel No BT configuration.

Figure 8-7. ISS Interfaces CPI Synchronization Signals and Frame Timing in SYNC Mode

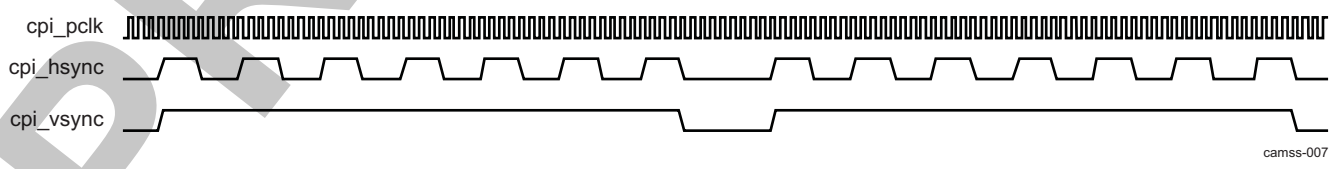

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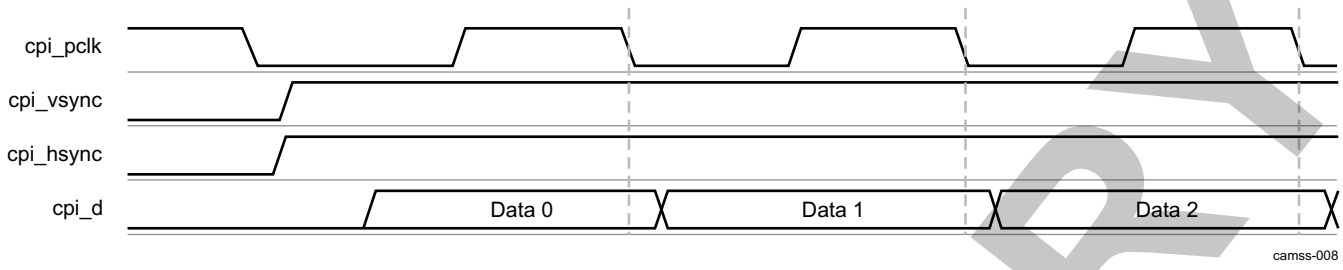
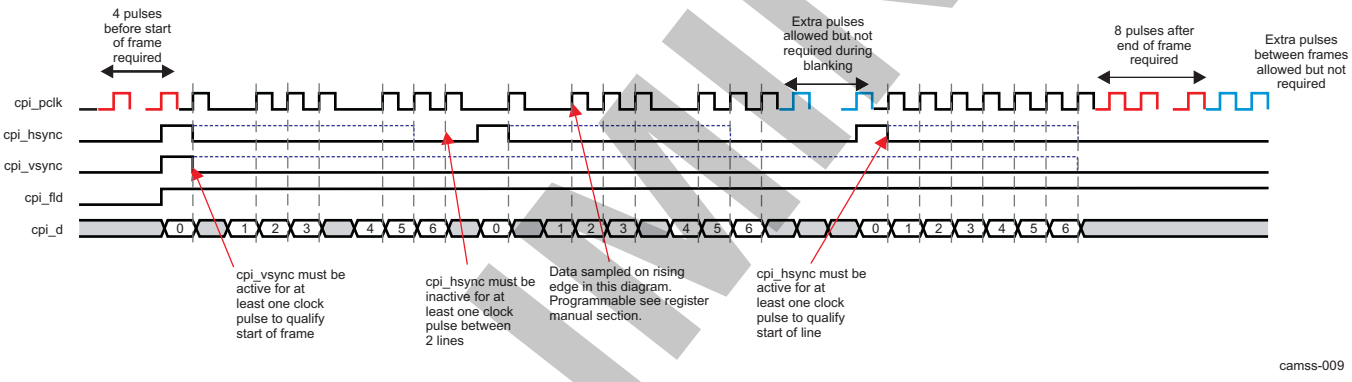
Figure 8-8. ISS Interfaces CPI Synchronization Signals and Data Timing in SYNC Mode



NOTE: The pixel clock can be gated to qualify valid pixels. It can also be gated during blanking periods to reduce power consumption. However, at least four clock pulses are required before sending active image data and synchronization information; eight clock pulses are required after the end of active video. Extra-clock pulses are allowed but not required during the line blanking periods.

Figure 8-9 shows the timing diagram of the SYNC move clock gating.

Figure 8-9. ISS Interfaces CPI SYNC Mode Clock Gating

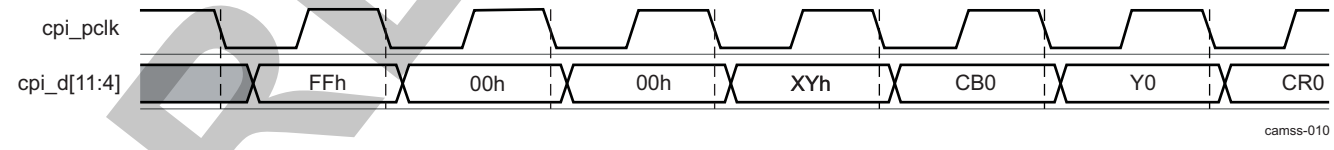


8.2.2.3.2 ISS Interfaces CPI ITU-R BT.656/1120 422 Protocol and Data Formats (8, 10 Bits)

The ISS CPI supports data in ITU-R BT.656 format. The ITU-R BT.656 standard specifies a method of transferring YUV4:2:2 data over an 8- or 10-bit video interface.

Figure 8-10 shows the data timing diagram with embedded synchronization signals.

Figure 8-10. ISS Interfaces CPI Data Timing With Embedded Synchronization Signals (8-Bit Case)



In BT.656, the data words (8- or 10-bit) in which the 8 most-significant bits (MSBs) are all set to 1, or all set to 0, are reserved.

NOTE: The ITU-R BT.656 specification is for 525-line and 625-line, digital component video signals in compliance with ITU-R BT.601. See the CCIR document Rec. 656-1 for detailed information about the interface.

The data is multiplexed in the following order: Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3, etc., where the byte sequence Cb2n Y2n Cr2n refers to interleaved Luminance and Chroma samples and the following byte Y2n + 1 corresponds to the next Luminance sample.

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The BT.656 protocol uses unique timing reference signals embedded in the video stream. The synchronization signals cpi_hsync and cpi_vsync are not needed. This reduces the number of wires required for a BT.656 video interface.

There are two timing reference codes: The start of active video (SAV) reference code precedes each video data block, and the end of active video (EAV) follows each video data block. Each timing reference signal consists of a 4-byte sequence in the following hexadecimal format: FF 00 00 XY. The first 3 bytes are a fixed preamble (see the ITU-R BT.656 specification). The fourth byte (XY) contains information defining field identification (F), blanking (V), and SAV/EAV information (H), and 4 parity bits calculated as a function of F, V, and H (see the ITU-R BT.656 specification).

Table 8-42 lists the video timing reference codes for SAV and EAV.

Table 8-42. ISS Interfaces CPI Video Timing Reference Codes for SAV and EAV

Data Bit Number	First Word (FF)	Second Word (00)	Third Word (00)	Fourth Word (XY)
9 (MSB)	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H
5	1	0	0	P3
4	1	0	0	P2
3	1	0	0	P1
2	1	0	0	P0
1	1	0	0	0
0	1	0	0	0

Table 8-43 describes the F, V, and H signals.

Table 8-43. ISS Interfaces CPI F, V, H Signal Descriptions

Signal	Value	Command
F	0	Field 1
	1	Field 2
V	0	0
	1	Vertical blank
H	0	SAV
	1	EAV

The resulting Hamming distance between any two code words is four, allowing two error detections and one error correction. To enable or disable the error-correcting capability, configure the ISIF_REC656IF[0] ECCFVH bit.

NOTE: The 2-bit errors are detected, but not flagged or corrected. Errors of more than 2 bits are not corrected or flagged.

Table 8-44 lists the F, V, and H protection (error-correction) bits.

Table 8-44. ISS Interfaces CPI F, V, H Protection (Error-Correction) Bits

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1

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Table 8-44. ISS Interfaces CPI F, V, H Protection (Error-Correction) Bits (continued)

F	V	H	P3	P2	P1	P0
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

When operating in ITU-R BT.656 mode, data is stored in SDRAM according to the format listed in Table 8-45 when the ISIF_REC656IF[1] R656ON bit is enabled.

Table 8-45. ISS Interfaces CPI ITU-R BT.656 Mode Data Format in SDRAM

b31			b0
Pixel3 (Y1)	Pixel2 (Cr0)	Pixel1 (Y0)	Pixel0 (Cb0)

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8.2.3 ISS CSI PHY

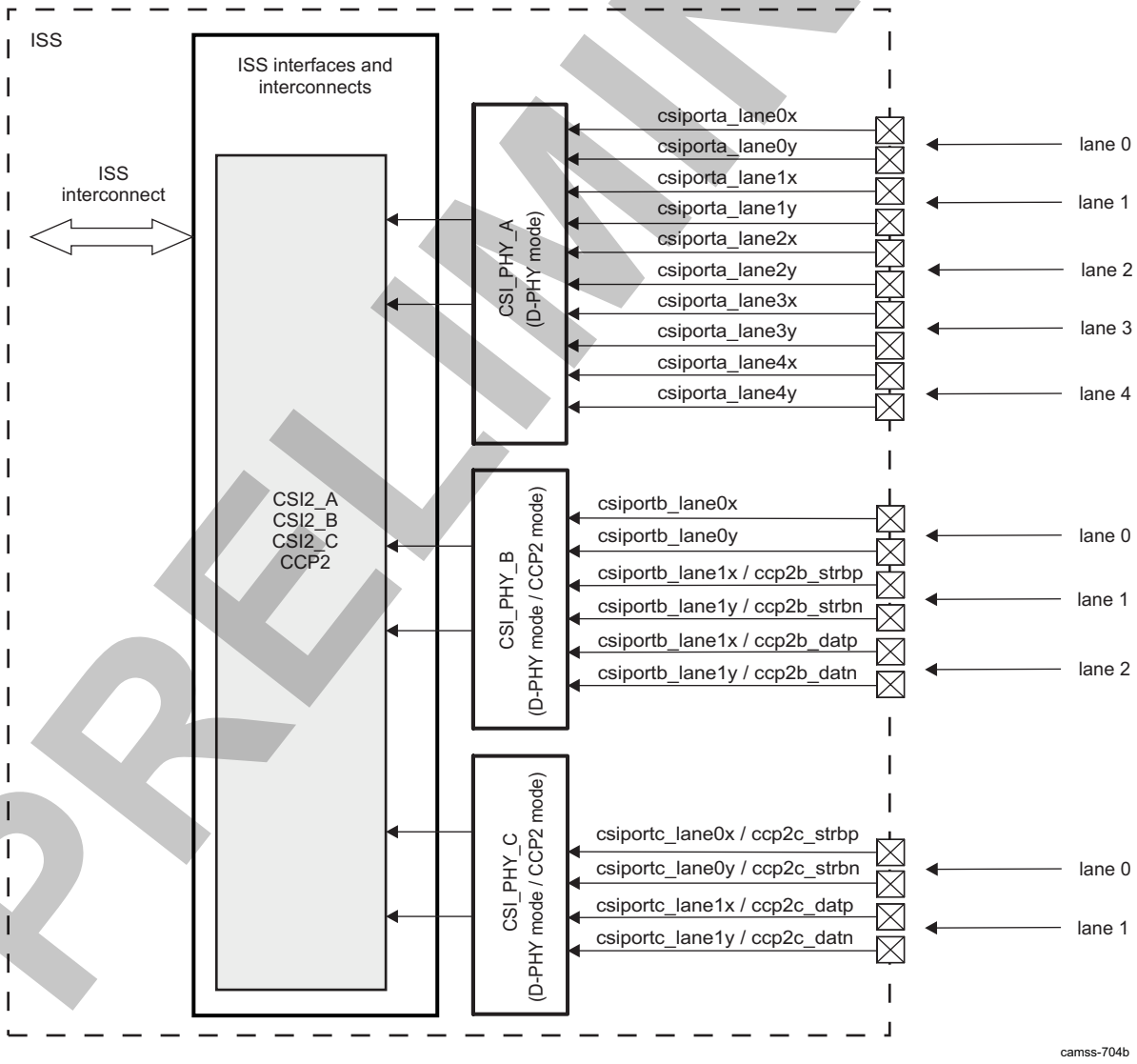
8.2.3.1 ISS CSI PHY Overview

Three MIPI D-PHY / SMIA CCP2 compliant PHY receivers (CSI_PHY_A, CSI_PHY_B and CSI_PHY_C, or generally referenced to as CSI_PHY) immediately before the ISS interfaces (CSI2_A, CSI2_B, CSI2_C and CCP2) act as a physical connection and configuration of clock/data lanes with external sensors. A CSI_PHY supports up to four configurations, depending on the required number of D-PHY data lane external sensors. The receivers are compatible with the *MIPI D-PHY Specification v1.00.00*. The selection of a CSI_PHY in D-PHY mode, parallel mode, or CCP2 mode must be done before reset and not on the fly.

The CSI_PHY is controlled and must be configured first from the device Control Module for pad configuration. The differential data/clock lanes coming into the CSI2_A, CSI2_B and CSI2_C CSI_PHYs are configured from registers explained in (see register CONTROL_CAMERA_RX).

There are three CSI_PHYs integrated in the device. As shown in Figure 8-11, the CSI_PHY_A contains four data lane; CSI_PHY_B is the same, except that it has two data lanes plus a clock/strobe lane; CSI_PHY_C has one data lanes plus a clock/strobe lane. The figure below shows the three CSI_PHY cases, with their signals listed in Table 8-41.

Figure 8-11. ISS Interfaces CSI_PHYs Diagram



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NOTE: If CCP2 mode is chosen for use in the CSI2_B/CCP2 CSI_PHY_B, then only LANE 1 and LANE 2 are used, as strbp/strbn and datp/datn respectively.

NOTE: LANE 4 of CSI2_A CSI_PHY_A can be used only as a data lane, never as a clock lane. All other configurations are possible.

NOTE: Depending on the selected mux mode from the Control Module, the Parallel Interface (CPI) signals can also be going through one of the CSI_PHYs.

CSI2_A, CSI2_B/CCP2 and CSI2_C/CCP2 CSI_PHYs represent the overall PHY solution for connecting external sensors to feed the ISS. The MIPI D-PHY function can support up to four data lane modules and one clock lane module. Reverse direction escape mode is not supported. The lane module polarity and positions are configurable; that is, any lane module can be chosen as the clock lane module, and the DX/DY data pad for each lane module can be configured as DP or DN pins defined. The configuration and the selection of D-PHY mode, data/clock, or data/strobes are done through the device Control Module (see Chapter 18, *Control Module*). The only exception is the four-data-lane use case, in which one corner lane is allowed to be only a data lane. For the CCP2 function, the CSI_PHY solution support two data/strobe or data/clock lane modules. The data lane module and strobe lane modules must be physically adjacent. CSI_PHY supports serial configuration protocol for the configuration interface.

8.2.3.2 ISS CSI PHY Functional Description

8.2.3.2.1 ISS CSI PHY Functional Configuration

The CSI_PHY converts the bitstream, divided into 1 up to 4 serial data lanes, and one clock lane, into a bitstream compatible with the CSI2/CCP2 receivers.

The CSI2_COMPLEXIO_IRQSTATUS register logs complex I/O events of the following types:

- Line power-state change (all lanes in ultralow-power mode [ULPM], at least one lane exits ULPM, etc.)
- Error on one lane

The CSI2 receiver embeds two registers to configure/read some complex I/O parameters:

- The REG0 register detects clock miss with respect to the *MIPI D-PHY Specification v1.00.00* and control timing.
- The REG0 register reports completion of reset on the different parts of the module and configures the timing parameters.
- The CSI2_COMPLEXIO_CFG registers contain the PWR_AUTO and PWR_CMD bit fields, which affect the power management of the three complex I/Os.

The complex I/O has three power modes: on, off, and ultralow power (ULP). These modes can reflect the ON or ULP states of the five differential lines if the CSI2_COMPLEXIO_CFG[24] PWR_AUTO bit is set to 1. If the PWR_AUTO bit is at reset value (0), the complex I/O power state is controlled by the CSI2_COMPLEXIO_CFG[28:27] PWR_CMD bit field, which directly defines the power state. Figure 8-12 shows the complex I/O power finite state-machine (FSM).

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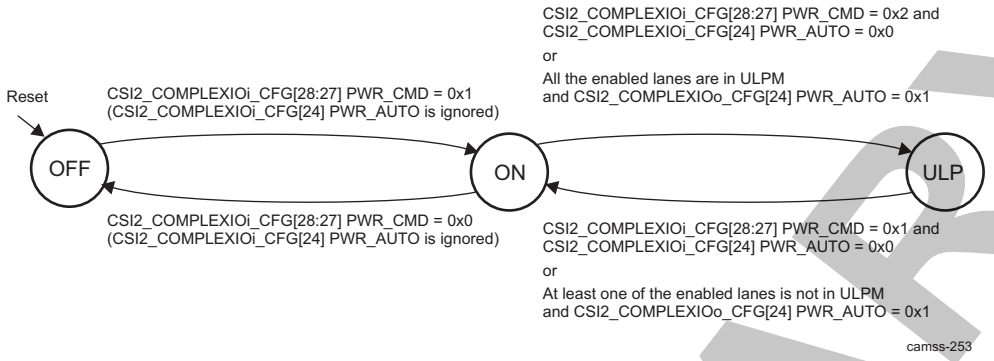
Figure 8-12. ISS CSI Complex I/O Power FSM



Another register, CSI2_TIMING, is used to control the power state of the complex I/O modules with regard to the differential line state. This register controls the mode of the three complex I/Os (RxMode and NoRxMode) and the delay between the differential lanes in STOP state and the complex I/O on NoRxMode. The CSI2_TIMING[15] FORCE_RX_MODE_IO1 bit sets the complex I/O in RxMode or NoRxMode (stopped mode). The FORCE_RX_MODE_IO bit is automatically reset to 0 by hardware when the counter ends and the FSM returns to NoRxMode. Three bits (CSI2_TIMING[14] STOP_STATE_X16_IO1, CSI2_TIMING[13] STOP_STATE_X4_IO1, and the CSI2_TIMING[12:0] STOP_STATE_COUNTER_IO1 bit field) configure the delay between line stop mode and complex I/O stop mode. The delay represents the number of functional clock (ISS_MAIN_FCLK) cycles and can be calculated as follows:

Total delay in ISS_MAIN_FCLK cycle = CSI2_TIMING.STOP_STATE_COUNTER_IO x (1+CSI2_TIMING.STOP_STATE_X16_IO x 15) x (1+CSI2_TIMING.STOP_STATE_X4_IO x 3).

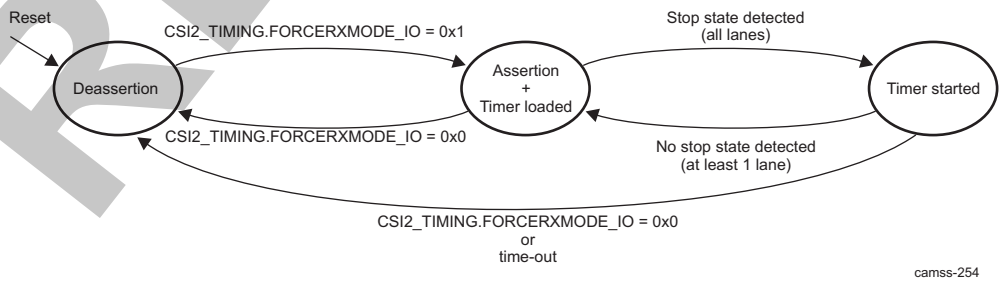
Table 8-46 lists the possible values of the delay, in terms of the ISS_MAIN_FCLK cycles, depending on the values of the STOP_STATE_X16_IO and STOP_STATE_X4_IO bits.

Table 8-46. ISS CSI2 Possible Time-Out Value for RxMode Counter

STOP_STATE_X16_IO	STOP_STATE_X4_IO	Possible Delay Value (in Functional Clock Cycles)
0x0	0x0	8191 (with step of 1)
0x0	0x1	32764 (with step of 4)
0x1	0x0	131056 (with step of 16)
0x1	0x1	524224 (with step of 64)

The FORCERXMODE signal is used at initialization time (complex I/O). Figure 8-13 describes the ForceRxMode and StopState FSM to assert and deassert the FORCERXMODE signal and to monitor STOPSTATE from the complex I/O.

Figure 8-13. ISS CSI2 RxMode and StopState FSM



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8.2.3.2.2 ISS CSI PHY (D-PHY Mode) and Link Initialization Sequence

The MIPI D-PHY initialization sequence is not implemented within CSI_PHY. The CSI2_A/B/C receiver is expected to coordinate the PHY initialization. The controller must ensure that the CSI_PHY is held in RESET/WAIT for RX mode until the D-PHY transmitter is powered up and the link comes to the defined state. The controller can use the STOPSTATE and FORCERXMODE signals of CSI_PHY for this purpose. STOPSTATE indicates the line states, while FORCERXMODE forces the receiver state-machine into "wait for stop state." One possible initialization sequence is:

To fully initialize the CSI_PHY, perform the following steps:

1. Configure all CSI2 receiver registers to be ready to receive signals/data from the CSI_PHY:
   (a) Configure all needed CSI2 registers:
      (i) Set CSI2_COMPLEXIO_CFG[18:16] DATA4_POSITION.
      (ii) Set CSI2_COMPLEXIO_CFG[14:12] DATA3_POSITION.
      (iii) Set CSI2_COMPLEXIO_CFG[10:8] DATA2_POSITION.
      (iv) Set CSI2_COMPLEXIO_CFG[6:4] DATA1_POSITION.
      (v) Set CSI2_COMPLEXIO_CFG[2:0] CLOCK_POSITION.
      (vi) Set the CONTROL_CAMERA_RX[23:22] CSIPORTC_CAMMODE, CONTROL_CAMERA_RX[12:11] CSIPORTB_CAMMODE or CONTROL_CAMERA_RX[2:1] CSIPORTA_CAMMODE.

CAUTION

This must be done before the CSIPHY is active.

      (vii) A dedicated internal clock gate control is present for each PHY. Enable/disable the internal CTRLCLK from the CONTROL_CAMERA_RX register by setting the following bits:
         - [21] CSIPORTC_CTRLCLKEN for CSI_PHY_C
         - [10] CSIPORTB_CTRLCLKEN for CSI_PHY_B
         - [0] CSIPORTA_CTRLCLKEN for CSI_PHY_A
2. CSI_PHY and link initialization sequence:
   (a) Deassert the CSI_PHY reset.
      (i) Set CSI2_COMPLEXIO_CFG[30] RESET_CTRL to 0x1.

CAUTION

For the CSI2_COMPLEXIO_CFG[29] RESET_DONE bit to be set to 0x1 (reset completed), the external sensor must to be active and sending the MIPI HS BYTECLK.

   The following registers can be set only after deasserting the CSI_PHY reset and before asserting the FORCERXMODE signal:
   - REG0
   - REG1
   - REG2

   (b) Assert the FORCERXMODE signal:
      (i) Set CSI2_TIMING[15] FORCE_RX_MODE_IO1 to 0x1.
   (c) Connect pulldown on link (DP/DN) by asserting the respective PIPD* signals (PIPD* = 0):
   For CSI2_PHY_A pulldown on signals through padconf registers:
   - csiporta_lane4x:
     – CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[8]

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CSIPORTA_LANE4X_INPUTENABLE = 0x1

- CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[4] CSIPORTA_LANE4X_PULLTYPESELECT = 0x0
- CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[3] CSIPORTA_LANE4X_PULLUDENABLE = 0x1

- csiporta_lane4y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[24] CSIPORTA_LANE4Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[20] CSIPORTA_LANE4Y_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[19] CSIPORTA_LANE4Y_PULLUDENABLE = 0x1
- csiporta_lane3x:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[8] CSIPORTA_LANE3X_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[4] CSIPORTA_LANE3X_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[3] CSIPORTA_LANE3X_PULLUDENABLE = 0x1
- csiporta_lane3y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[24] CSIPORTA_LANE3Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[20] CSIPORTA_LANE3Y_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[19] CSIPORTA_LANE3Y_PULLUDENABLE = 0x1
- csiporta_lane2x:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[8] CSIPORTA_LANE2X_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[4] CSIPORTA_LANE2X_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[3] CSIPORTA_LANE2X_PULLUDENABLE = 0x1
- csiporta_lane2y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[24] CSIPORTA_LANE2Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[20] CSIPORTA_LANE2Y_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[19] CSIPORTA_LANE2Y_PULLUDENABLE = 0x1
- csiporta_lane1x:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[8] CSIPORTA_LANE1X_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[4] CSIPORTA_LANE1X_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[3] CSIPORTA_LANE1X_PULLUDENABLE = 0x1
- csiporta_lane1y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[24] CSIPORTA_LANE1Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[20]

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CSIPORTA_LANE1Y_PULLTYPESELECT = 0x0

– CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[19] CSIPORTA_LANE1Y_PULLUDENABLE = 0x1

- csiporta_lane0x:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[8] CSIPORTA_LANE0X_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[4] CSIPORTA_LANE0X_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[3] CSIPORTA_LANE0X_PULLUDENABLE = 0x1
- csiporta_lane0y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[24] CSIPORTA_LANE0Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[20] CSIPORTA_LANE0Y_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[19] CSIPORTA_LANE0Y_PULLUDENABLE = 0x1

For CSI_PHY_B pulldown on signals through padconf registers:

- csiportb_lane2x:
  - CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[8] CSIPORTB_LANE2X_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[4] CSIPORTB_LANE2X_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[3] CSIPORTB_LANE2X_PULLUDENABLE = 0x1
- csiportb_lane2y:
  - CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[24] CSIPORTB_LANE2Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[20] CSIPORTB_LANE2Y_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[19] CSIPORTB_LANE2Y_PULLUDENABLE = 0x1
- csiportb_lane1x:
  - CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[8] CSIPORTB_LANE1X_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[4] CSIPORTB_LANE1X_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[3] CSIPORTB_LANE1X_PULLUDENABLEE = 0x1
- csiportb_lane1y:
  - CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[24] CSIPORTB_LANE1Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[20] CSIPORTB_LANE1Y_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[19] CSIPORTB_LANE1Y_PULLUDENABLE = 0x1
- csiportb_lane0x:
  - CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[8] CSIPORTB_LANE0X_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[4] CSIPORTB_LANE0X_PULLTYPESELECT = 0x0

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– CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[3] CSIPORTB_LANE0X_PULLUDENABLE = 0x1

- csiportb_lane0y:
  - CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[24] CSIPORTB_LANE0Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[20] CSIPORTB_LANE0Y_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[19] CSIPORTB_LANE0Y_PULLUDENABLE = 0x1

For CSI_PHY_C pulldown on signals through padconf registers:

- csiportc_lane1x:
  - CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[8] CSIPORTC_LANE1X_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[4] CSIPORTC_LANE1X_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[3] CSIPORTC_LANE1X_PULLUDENABLE = 0x1
- csiportc_lane1y:
  - CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[24] CSIPORTC_LANE1Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[20] CSIPORTC_LANE1Y_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[19] CSIPORTC_LANE1Y_PULLUDENABLE = 0x1
- csiportc_lane0x:
  - CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[8] CSIPORTC_LANE0X_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[4] CSIPORTC_LANE0X_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[3] CSIPORTC_LANE0X_PULLUDENABLE = 0x1
- csiportc_lane0y:
  - CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[24] CSIPORTC_LANE0Y_INPUTENABLE = 0x1
  - CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[20] CSIPORTC_LANE0Y_PULLTYPESELECT = 0x0
  - CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[19] CSIPORTC_LANE0Y_PULLUDENABLE = 0x1

(d) Power up the CSI_PHY:

(i) Set CSI2_COMPLEXIO_CFG[28:27] PWR_CMD to 0x1.

(e) Check whether the state status reaches the ON state:

- CSI2_COMPLEXIO_CFG[26:25] PWR_STATUS = 0x1

(f) Wait for STOPSTATE = 1 (for all enabled lane modules):

(i) The timer is set through the CSI2_TIMING[14:0] bit field. The reset value can be kept.

(ii) Wait until CSI2_TIMING[15] FORCE_RX_MODE_IO1 = 0x0. It is automatically put at 0 when all enabled lanes are in STOPSTATE and the timer is finished.

(g) Release PIPD* (= 1).

For CSI_PHY_A pullup on signals through padconf registers:

- csiporta_lane4x:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[4]

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CSIPORTA_LANE4X_PULLTYPESELECT = 0x1

- csiporta_lane4y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[20] CSIPORTA_LANE4Y_PULLTYPESELECT = 0x1
- csiporta_lane3x:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[4] CSIPORTA_LANE3X_PULLTYPESELECT = 0x1
- csiporta_lane3y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[20] CSIPORTA_LANE3Y_PULLTYPESELECT = 0x1
- csiporta_lane2x:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[4] CSIPORTA_LANE2X_PULLTYPESELECT = 0x1
- csiporta_lane2y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[20] CSIPORTA_LANE2Y_PULLTYPESELECT = 0x1
- csiporta_lane1x:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[4] CSIPORTA_LANE1X_PULLTYPESELECT = 0x1
- csiporta_lane1y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[20] CSIPORTA_LANE1Y_PULLTYPESELECT = 0x1
- csiporta_lane0x:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[4] CSIPORTA_LANE0X_PULLTYPESELECT = 0x1
- csiporta_lane0y:
  - CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[20] CSIPORTA_LANE0Y_PULLTYPESELECT = 0x1

3. The CSI_PHY is initialized and ready/active in CSI2 (D-PHY) mode.

8.2.3.2.3 ISS CSI PHY (CCP2 Mode) and Link Initialization Sequence

The CSI2_B/C receiver is expected to coordinate the CSI_PHY initialization in CCP2 mode. The controller must ensure that the PHY is held in RESET state until the CCP transmitter is powered up and the link comes to the defined state. The controller can use the FORCERXMODE signals of CSI_PHY for this purpose. FORCERXMODE forces the receiver state-machine into RESET state, while the rest of common logic is powered up and functional. One possible initialization sequence is:

To fully initialize the CSI_PHY, perform the following steps:

1. Configure all CSI2_B/C receiver registers to be ready to receive signals/data from the CSI_PHY:

   (a) Configure all CCP2 registers:

   (i) Set CSI2_COMPLEXIO_CFG[10:8] DATA2_POSITION.

   (ii) Set CSI2_COMPLEXIO_CFG[6:4] DATA1_POSITION.

   (b) Set CONTROL_CAMERA_RX[12:11] CSIPORTB_CAMMODE or CONTROL_CAMERA_RX[23:22] CSIPORTC_CAMMODE.

> **CAUTION**
>
> This must be done before the CSI_PHY is active.

   (c) A dedicated internal clock gate control is present for each PHY. Enable/disable the internal

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CTRLCLK from the CONTROL_CAMERA_RX register by setting the following bits:

- [21] CSIPORTC_CTRLCLKEN for CSI_PHY_C
- [10] CSIPORTB_CTRLCLKEN for CSI_PHY_B
- [0] CSIPORTA_CTRLCLKEN for CSI_PHY_A

2. CSI_PHY and link initialization sequence:
   (a) Deassert the CSI_PHY reset:
      (i) Set CSI2_COMPLEXIO_CFG[30] RESET_CTRL to 0x1.
   (b) Assert the FORCERXMODE signal:
      (i) Set CSI2_TIMING[15] FORCE_RX_MODE_IO1 to 0x1.
   (c) Power up the CSI_PHY:
      (i) Set CSI2_COMPLEXIO_CFG[28:27] PWR_CMD to 0x1.
   (d) Check that the state status reaches the ON state:
      - CSI2_COMPLEXIO_CFG[26:25] PWR_STATUS = 0x1
   (e) Release the FORCERXMODE signal:
      (i) Set CSI2_TIMING[15] FORCE_RX_MODE_IO1 to 0x0.
3. The CSI_PHY is initialized and ready/active in CSI1/CCP2B mode.

8.2.3.2.4 ISS CSI PHY Error Signals

In D-PHY mode, the CSI_PHY supports the following error detection and signaling to the associated receiver:

- ERRSOTHS: Flags 1-bit errors in the HS start of transmission synchronization pattern. In this error scenario, the CSI_PHY continues to receive the data and pass it to the receiver, but confidence in the data may be low, because of the 1-bit error seen in sync. This signal, if asserted, is high for one cycle of RXBYTECLKHS.
- ERRSOTSYNCHS: Flags multiple bit errors in the HS start of transmission synchronization pattern. In this case, the CSI_PHY cannot achieve proper synchronization and does not pass the received data to the receiver. This signal, if asserted, is high for one cycle of RXBYTECLKHS.
- ERRCONTROL: Flags the control sequence error; that is, when the LP sequence observed on line is not recognized as a valid control sequence. This signal, if asserted, is high until the next change in the state of the LP line.
- ERRESC: Flags the escape entry error; that is, when the escape entry sequence is unrecognized. This signal, if asserted, is high until the next change in the state of the LP line.
- ERRSYNCESC: Flags the low-power data transmission synchronization error. This error is flagged if the number of bits received during a low-power data transmission is not a multiple of 8 bits. This signal, if asserted, is high until the next change in the state of the LP line. In case the number of received bits is 1 less than a multiple of 8, RXVALIDESC is also asserted together with ERRSYNCESC, and an erroneous data byte is output on RXDATAESC. In other cases of this error, RXVALIDESC is not asserted and an erroneous data byte is not sent out.

In CCP2 mode, the CSI_PHY supports the following error detection and signaling to the associated receiver:

- CCPERRRESYNC output is an error indicator to the receiver to flag the shifted synchronization error, if the new synchronization sequence is not aligned with a 32-bit word boundary compared to the previously received synchronization sequence. This error flag is asserted for 32 cycles (4 bytes/32 bits).

8.2.3.3 ISS CSI PHY Register Manual

8.2.3.3.1 ISS CSI PHY Instance Summary

Table 8-47 lists the ISS CSI PHY instance.

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Table 8-47. ISS CSI PHY Instance Summary

Module Name	L3_MAIN Base Address	Size
ISS_CAMERARX_CORE1	0x5200 1170	64 bytes
ISS_CAMERARX_CORE2	0x5200 1570	64 bytes
ISS_CAMERARX_CORE3	0x5200 2570	64 bytes

NOTE: ISS_CAMERARX_CORE1 is for CSI2_A CSI_PHY_A.

ISS_CAMERARX_CORE2 is for CSI2_B/CCP2 CSI_PHY_B.

ISS_CAMERARX_CORE3 is for CSI2_C/CCP2 CSI_PHY_C.

8.2.3.3.2 ISS CSI PHY Registers

8.2.3.3.2.1 ISS CSI PHY Register Summary

Table 8-48 summarizes the ISS CSI PHY register mapping.

Table 8-48. ISS CSI PHY Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CAMERARX_CORE1 Base Address	ISS_CAMERARX_CORE2 Base Address	ISS_CAMERARX_CORE3 Base Address
REG0	RW	32	0x0000 0000	0x5200 1170	0x5200 1570	0x5200 2570
REG1	RW	32	0x0000 0004	0x5200 1174	0x5200 1574	0x5200 2574
REG2	RW	32	0x0000 0008	0x5200 1178	0x5200 1578	0x5200 2578

8.2.3.3.2.2 ISS CSI PHY Register Description

through describe the ISS CSI PHY register bits.

Table 8-49. REG0

Address Offset	0x0000 0000		
Physical Address	0x5200 1170 0x5200 1570 0x5200 2570	**Instance**	ISS_CAMERARX_CORE1 ISS_CAMERARX_CORE2 ISS_CAMERARX_CORE3
Description	First register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							HSCLOCKCONFIG	RESERVED								THS_TERM								THS_SETTLE							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved fields	NA	0x00
24	HSCLOCKCONFIG	Disable clock missing detector	RW	0
23:16	RESERVED	Read returns zero	R	0x00

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Bits	Field Name	Description	Type	Reset
15:8	THS_TERM	THS_TERM timing parameter in multiples of DDR clock Effective time for enabling of termination = synchronizer delay + timer delay + LPRX delay + combinational routing delay ~ (1–2)* DDRCLK + THS-TERM + ~ (1 –15) ns Programmed value = ceil(12.5 / DDR clock period) –1 Default value : 4 (for 400 MHz)	RW	0x04
7:0	THS_SETTLE	THS_SETTLE timing parameter in multiples of DDR clock frequency Effective THS_SETTLE seen on line (starting to look for sync pattern) = synchronizer delay + timer delay + LPRX delay + combinational routing delay – pipeline delay in HS data path ~ (1–2)* DDRCLK + THS-SETTLE + ~ (1–15) ns –1*DDRCLK Programmed value = ceil(90 ns / DDR clock period) + 3 Default value : 39 (for 400 MHz) Minimum supported THS-SETTLE programmed value = 3	RW	0x27

Table 8-50. Register Call Summary for Register REG0

ISS Interfaces

- ISS CSI PHY Functional Configuration: [0] [1]
- ISS CSI PHY (D-PHY Mode) and Link Initialization Sequence: [2]
- ISS CSI PHY Registers: [3]

Table 8-51. REG1

Address Offset	0x0000 0004		
Physical Address	0x5200 1174 0x5200 1574 0x5200 2574	**Instance**	ISS_CAMERARX_CORE1 ISS_CAMERARX_CORE2 ISS_CAMERARX_CORE3
Description	Second register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESVD_READ_BIT		RESET_DONE_STATUS		RESERVED		CLOCK_MISS_DETECTOR_STATUS		TCLK_TERM								DPHY_HS_SYNC_PATTERN						CTRLCLK_DIV_FACTOR		TCLK_SETTLE							

Bits	Field Name	Description	Type	Reset
31:30	RESVD_READ_BIT	Reserved bit	NA	0x0
29:28	RESET_DONE_STATUS	Reset done read bits. 28: RESETDONERXBYTECLK **Note:** BYTECLK is provided to the ISS CSI2_A, CSI2_B, CSI2_C and CCP2 interfaces 29: RESETDONECTRLCLK **Note:** This is the CSI_PHY_CTRL_FCLK provided to the PHY from the PRCM module.	R	0x0
27:26	RESERVED	Write 0 for future compatibility.	RW	0x0

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Bits	Field Name	Description	Type	Reset
25	CLOCK_MISS_DETECTOR_STATUS	Clock missing detector status. Internal debug bit. 1: Error in clock missing detector. 0: Clock missing detector successful Note: CLKMISS detector is likely to malfunction, if tclk-trail spec (60ns) is not honoured.	R	0
24:18	TCLK_TERM	TCLK_TERM timing parameter in multiples of CTRLCLK (CSI_PHY_CTRL_FCLK) Effective time for enabling of termination = synchronizer delay + timer delay + LPRX delay + combinational routing delay ~ (1–2)* CTRLCLK + TCLK_TERM + ~ (1–15) ns Programmed value = ceil(9.5 / CTRLCLK period) – 1 Default value : 0 (for 96 MHz)	RW	0x00
17:10	DPHY_HS_SYNC_PATTERN	DPHY mode HS sync pattern in byte order (reverse of received order) See Section 8.2.3.2.4, *ISS CSI PHY Error Signals.*	RW	0xB8
9:8	TCLK_DIV	CTRLCLK_DIV_FACTOR Divide factor for CTRLCLK (CSI_PHY_CTRL_FCLK) for CLKMISS detector Programmed value = ceil (15ns/CTRLCLK Period) - 1 Default value: 1 (for 96 MHz) CLKMISS detection time = (5*TCLK_DIV+1)*(CTRLCLK period) < 60ns Note: Only the CTRLCLK frequencies that satisfie above relationship are allowed. Typically, 96MHz will be used at CTRLCLK.	RW	0x1
7:0	TCLK_SETTLE	TCLK_SETTLE timing parameter in multiples of CTRLCLK (CSI_PHY_CTRL_FCLK) Clock Effective TCLK_SETTLE = synchronizer delay + timer delay + LPRX delay + combinational routing delay ~ (1–2)* CTRLCLK + Tclk-settle + ~ (1 –15) ns Programmed value = max[3, ceil(155 ns/CTRLCLK period) –1] Default value: 14 (for 96 MHz)	RW	0x0E

Table 8-52. Register Call Summary for Register REG1

ISS Interfaces

- ISS CSI PHY (D-PHY Mode) and Link Initialization Sequence: [0]
- ISS CSI PHY Registers: [1]

Table 8-53. REG2

Address Offset	0x0000 0008		
Physical Address	0x5200 1178 0x5200 1578 0x5200 2578	**Instance**	ISS_CAMERARX_CORE1 ISS_CAMERARX_CORE2 ISS_CAMERARX_CORE3
Description	Third register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRIGGER_CMD_RXTRIGESC0				TRIGGER_CMD_RXTRIGESC1				TRIGGER_CMD_RXTRIGESC2				TRIGGER_CMD_RXTRIGESC3				CCP2_SYNC_PATTERN															

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Bits	Field Name	Description	Type	Reset
31:30	TRIGGER_CMD_RXTRIGESC0	Mapping of Trigger escape entry command to PPI output RXTRIGGERESC0 00 : "01100010" 01 : "01011101" 10: "00100001" 11: "10100000"	RW	0x0
29:28	TRIGGER_CMD_RXTRIGESC1	Mapping of Trigger escape entry command to PPI output RXTRIGGERESC1 00 : "01011101" 01 : "00100001" 10: "10100000" 11: "01100010"	RW	0x0
27:26	TRIGGER_CMD_RXTRIGESC2	Mapping of Trigger escape entry command to PPI output RXTRIGGERESC2 00 : "00100001" 01 : "01100010" 10: "01100010" 11: "01011101"	RW	0x0
25:24	TRIGGER_CMD_RXTRIGESC3	Mapping of Trigger escape entry command to PPI output RXTRIGGERESC3 00 : "10100000" 01 : "01100010" 10: "01011101" 11: "00100001"	RW	0x0
23:0	CCP2_SYNC_PATTERN	CCP2 mode sync pattern in byte order (reverse of received order) See Section 8.2.3.2.4, *ISS CSI PHY Error Signals*.	R	0x0000FF

Table 8-54. Register Call Summary for Register REG2

ISS Interfaces

- ISS CSI PHY (D-PHY Mode) and Link Initialization Sequence: [0]
- ISS CSI PHY Registers: [1]

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8.2.4 ISS CCP2

8.2.4.1 ISS CCP2 Environment

8.2.4.1.1 ISS CCP2 Protocol and Data Formats

This section describes the CCP2 protocol and data formats. The CCP2 receiver is compatible with the *SMIA CCP2 Specification v1.0* and the *MIPI CSI1 Specification*. Table 8-55 describes the I/O for serial interface CCP2.

Table 8-55. I/O Description for Serial Interface CCP2

Signal Name		I/O[1]	Description
ccp2b_datp / ccp2c_datp	CAM_S_DATA	I	Serial data input. Configurable.
ccp2b_datn / ccp2c_datn			
ccp2b_strbp / ccp2c_strbp	CAM_S_CLK	I	Serial clock or strobe input. Configurable.
ccp2b_strbn / ccp2c_strbn			

(1) I = Input; O = Output

From the device point of view, the CCP2 interface comprises four differential inputs representing two effective signals: the serial data and the clock.

The CCP2 receiver is a serial interface to an image sensor. Signals from the camera are serial input data (CAM_S_DATA) and a clock/strobe signal (CAM_S_CLK). For more details on signals connectivity to image sensors, see Section 8.2.4.3.2, *ISS CCP2 PHY*.

8.2.4.1.1.1 ISS CCP2 Synchronization Codes

Each frame is clearly identified by four unique 32-bit synchronization codes: frame start, frame end, line start, and line end, which are embedded in the serial bitstream. The logical channel identification number is also encoded in the synchronization codes.

- Frame-start code (FSC): Identifies the start of a new frame
- Line-start code (LSC): Identifies the start of a new line and is received for every line, except the first line, that starts with an FSC
- Line-end code (LEC): Identifies the end of a line and is received for every line, except the last line, that ends with an FEC
- Frame-end code (FEC): Identifies the end of the last line and the end of the current frame

8.2.4.1.1.2 ISS CCP2 False Synchronization Code Protection

CCP2 supports false synchronization protection (FSP). Additional bytes after the JPEG stream can be written to the SDRAM. They do not prevent JPEG encode and there is no need to preserve them.

8.2.4.1.1.3 ISS CCP2 Image Data Operating Modes and Alignment Constraints

The CCP2 receiver interface has several image data operating modes (see Table 8-56). The EXPx formats (where x = 8, 16, or 32) are used to expand data up to 8, 16, or 32 bits by padding data with zeros. The Data Size Increase in Memory column indicates memory overhead versus format without data expansion and/or DPCM compression.

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Table 8-56. ISS CCP2 Image Data Operating Modes and Alignment Constraints

CCP2_LCx_CTRL[7:2] Format	CCP2 Data Format	Bits per Pixel (bpp) (When sending data to memory, N/A when sending to VP)	Data Size Increase in Memory. (When negative, data compression present)	2D Mode Availability[1]	Comments
0x0	YUV4:2:2 big endian	16	0%	Yes	
0x1	YUV4:2:2 little endian	16	0%	Yes	
0x2	YUV4:2:0	12	0%	Yes	
0x3	YUV4:2:2 + VP	N/A, data are sent to VP, YUV4:2:2 + VP = RAW8 + VP	N/A	Yes	
0x3	RAW8 + VP	N/A, data are sent to VP, YUV4:2:2 + VP must be used to output RAW8 + VP to memory	N/A	Yes	
0x4	RGB444 + EXP16	16	50%	Yes	
0x5	RGB565	16	0%	Yes	
0x6	RGB888	24	0%	Yes	
0x7	RGB888 + EXP32	32	33%	Yes	
0x8	RAW6 + EXP8	8	33%	Yes	
0x9	RAW6 + DPCM10 + EXP16	16	167%	Yes	DPCM decompression
0xA	RAW6 + DPCM10 + VP	N/A, data are sent to VP	N/A	Yes	DPCM decompression
0xB	RAW10 -> RAW6 DPCM	6	–40%	Yes	DPCM compression
0xC	RAW7 + EXP8	8	14%	Yes	
0xD	RAW7 + DPCM10 + EXP16	16	128%	Yes	DPCM decompression
0xE	RAW7 + DPCM10 + VP	N/A, data are sent to VP	N/A	Yes	DPCM decompression
0xF	RAW10 -> RAW6 DPCM + EXP8	8	–25%	Yes	DPCM compression
0x10	RAW8, this mode can be used to output RAW6 and RAW7	8	0%	Yes	
0x11	RAW8 + DPCM10 + EXP16	16	100%	Yes	DPCM decompression
0x12	RAW8 + DPCM10 + VP	N/A, data are sent to VP	N/A	Yes	DPCM decompression
0x13	RAW10 -> RAW7 DPCM	7	–30%	Yes	DPCM compression
0x14	RAW10	10	0%	Yes	
0x15	RAW10 + EXP16	16	60%	Yes	
0x16	RAW10 + VP	N/A, data are sent to VP	N/A	Yes	
0x17	RAW10 -> RAW7 DPCM + EXP8	8	–20%	Yes	
0x18	RAW12	12	0%	Yes	
0x19	RAW12 + EXP16	16	33%	Yes	
0x1A	RAW12 + VP	N/A, data are sent to VP	N/A	Yes	

(1) If 2D mode is available, there are no supplementary constraints on data width. 2D mode does not apply when sending to the video port (VP).

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Table 8-56. ISS CCP2 Image Data Operating Modes and Alignment Constraints (continued)

CCP2_LCx_CTRL[7:2] Format	CCP2 Data Format	Bits per Pixel (bpp) (When sending data to memory, N/A when sending to VP)	Data Size Increase in Memory. (When negative, data compression present)	2D Mode Availability(1)	Comments
0x1B	RAW10 -> RAW8 DPCM	8	–20%	Yes	DPCM decompression
0x1C	JPEG, 8-bit data	N/A	0%	Yes	
0x1D	JPEG, 8-bit data + FSP	N/A	0%	Yes	
0x1E	RAW10 -> RAW8 DPCM	8	–20%	Yes	Data right shift
0x1F	RAW8 DPCM12-> RAW12 + VP	N/A, data are sent to VP	N/A	Yes	
0x20	RAW10 -> RAW8 ALAW	8	–20%	Yes	
0x21	RAW8 DPCM10 -> ALAW	8	–20%	Yes	

NOTE:

- Padding data of a 32-bit pixel data stream is handled the same way regardless of the programmed format. Therefore, there is no increase or decrease in storage because it is not compressed or decompressed.
- EXP8 = Data expansion to 8 bits, padding with zeros
- EXP16 = Data expansion to 16 bits, padding with alpha or zeros

  CCP2_LCx_CTRL[15:8] ALPHA can be used to set an alpha value.

  For RGB444 + EXP16:

  – data_out[31:28] = ALPHA [3:0]
  – data_out[15:12] = ALPHA [3:0]
- EXP32 = Data expansion to 32 bits, padding with alpha

  CCP2_LCx_CTRL[15:8] ALPHA can be used to set an alpha value.

  For RGB888 + EXP32: data_out[31:24] = ALPHA [7:0]
- FSP = False synchronization code protection decoding. Applies only to JPEG8 data format.
- VP = Output to the video-preprocessing hardware is enabled. Programmers must ensure that only one logical channel is enabled to the video preprocessing hardware. The behavior of the hardware is unpredictable if several logical channels to the video preprocessing hardware are enabled simultaneously.
- DPCM10 = Data decompression to 10 bits. Applies only to RAW6, RAW7, and RAW8 data formats; disabled if CCP2_CTRL[4] MODE = 0.
- Padding is handled the same way regardless of the programmed format.

NOTE: Data written by CSI2 can be read back by the CCP2 read channel. Some constrains apply (see Table 8-59).

8.2.4.1.1.4 ISS CCP2 Pixel Data Format

This section summarizes how the CCP2 pixel data formats are transmitted over the serial interface and how the pixels are reconstructed, stored in memory, or passed to the video port.

The CCP2 receiver can cope with all data formats if the data line length sent through the CS1/CCP2 physical protocol is a multiple of 32 bits. This condition is required for the CCP2 receiver to work correctly.

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However, some data formats impose stronger line-length constraints to finish pixel reconstruction correctly at the end of the lines. This is imposed by CCP2 protocol-specific requirements, and not the CCP2 receiver. If CCP2 protocol constraints are not respected:

- Only the pixels reconstructed last in every line are erroneous. The missing bits are replaced with zeros to perform pixel reconstruction.
- The FW_IRQ interrupt is triggered.

8.2.4.1.1.4.1 ISS CCP2 YUV Operating Modes

NOTE: Although there are different possibilities of endianness in the bitstream, the device as a whole typically works in little-endian format. Therefore, the use of little-endian format is recommended.

8.2.4.1.1.4.1.1 ISS CCP2 YUV4:2:2

The YUV4:2:2 data format can be stored to memory in little- or big-endian format. The line length sent through the CCP2 receiver protocol must be a multiple of 32 bits.

YUV4:2:2 data format can also be sent to the video port.

YUV4:2:2 + VP is used to output RAW8 data to the video port: YUV4:2:2 + VP is equivalent to RAW8 + VP. Figure 8-14 and Figure 8-15 show big-endian and little-endian YUV4:2:2 format, respectively. Set CCP2_LCx_CTRL[7:2] FORMAT to 0x0 to select YUV4:2:2 little-endian mode and to 0x1 for YUV4:2:2 big-endian mode.

Figure 8-14. ISS CCP2 YUV4:2:2 Big Endian

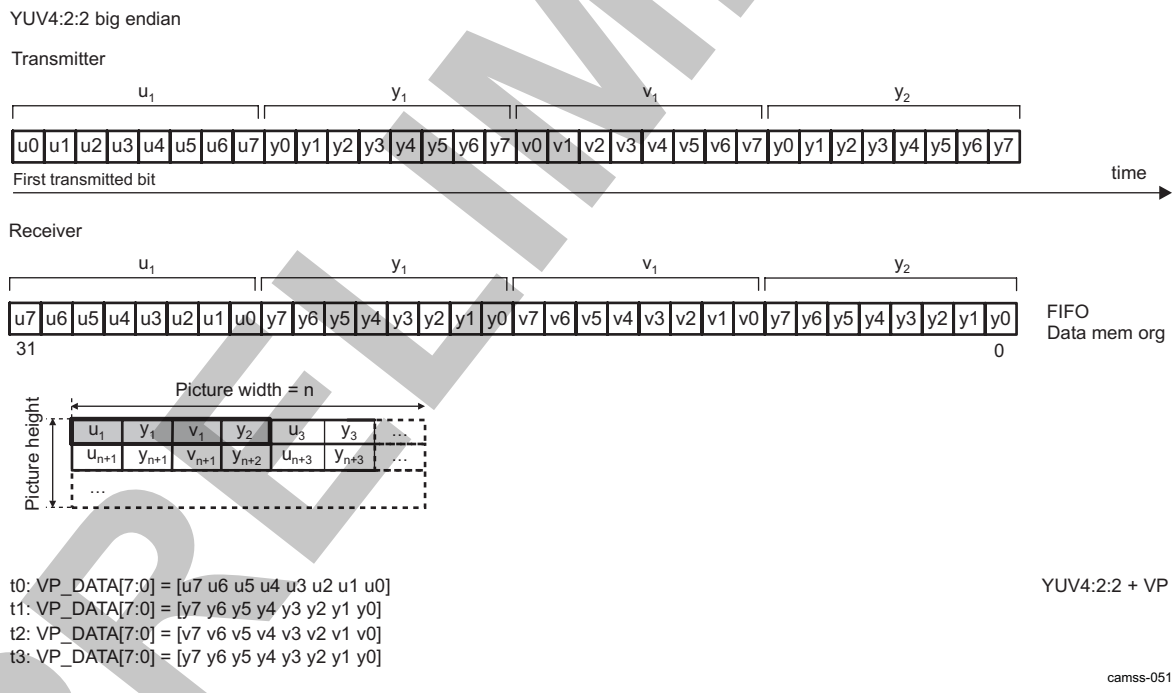

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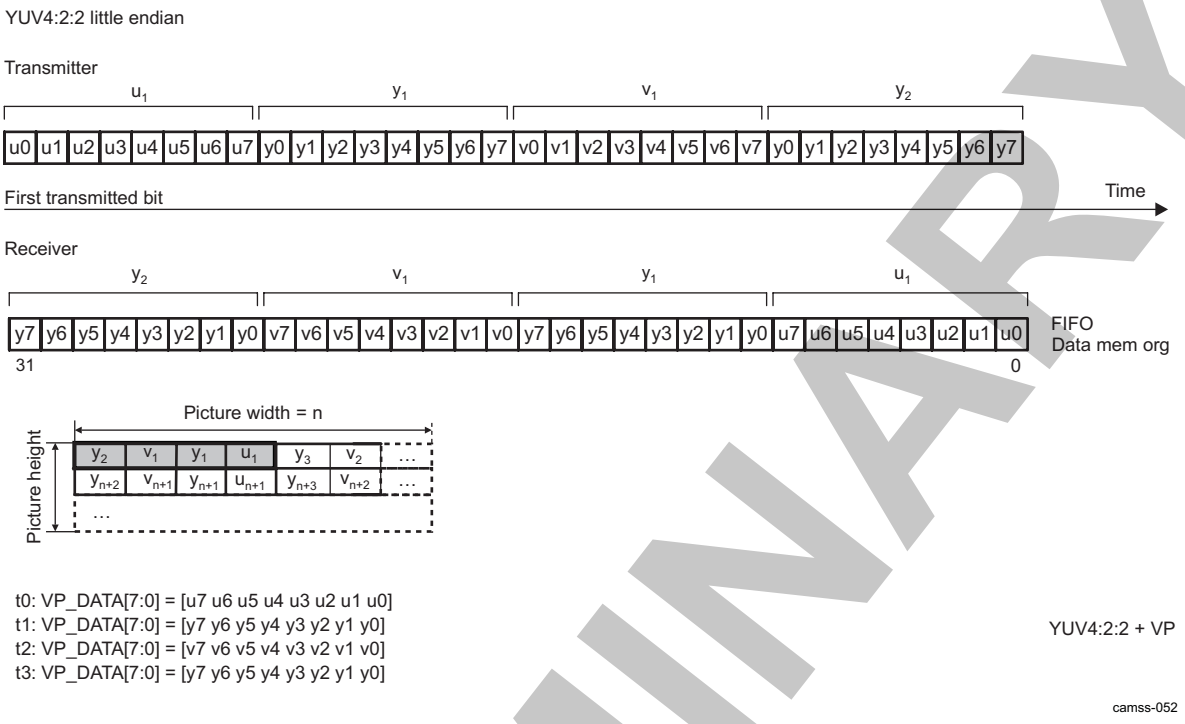
Figure 8-15. ISS CCP2 YUV4:2:2 Little Endian



8.2.4.1.1.4.1.2 ISS CCP2 YUV4:2:0

The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. Furthermore, the line length all together sent by the CCP2 receiver is a multiple of 3 x 32 bits and the number of lines is even to correctly finish the pixel reconstruction.

The line structure is different for odd and even lines. Odd lines transport the U component, while even lines contain the V component. This is shown in Figure 8-16. Set CCP2_LCx_CTRL[7:2] FORMAT to 0x3 to select YUV4:2:0 mode.

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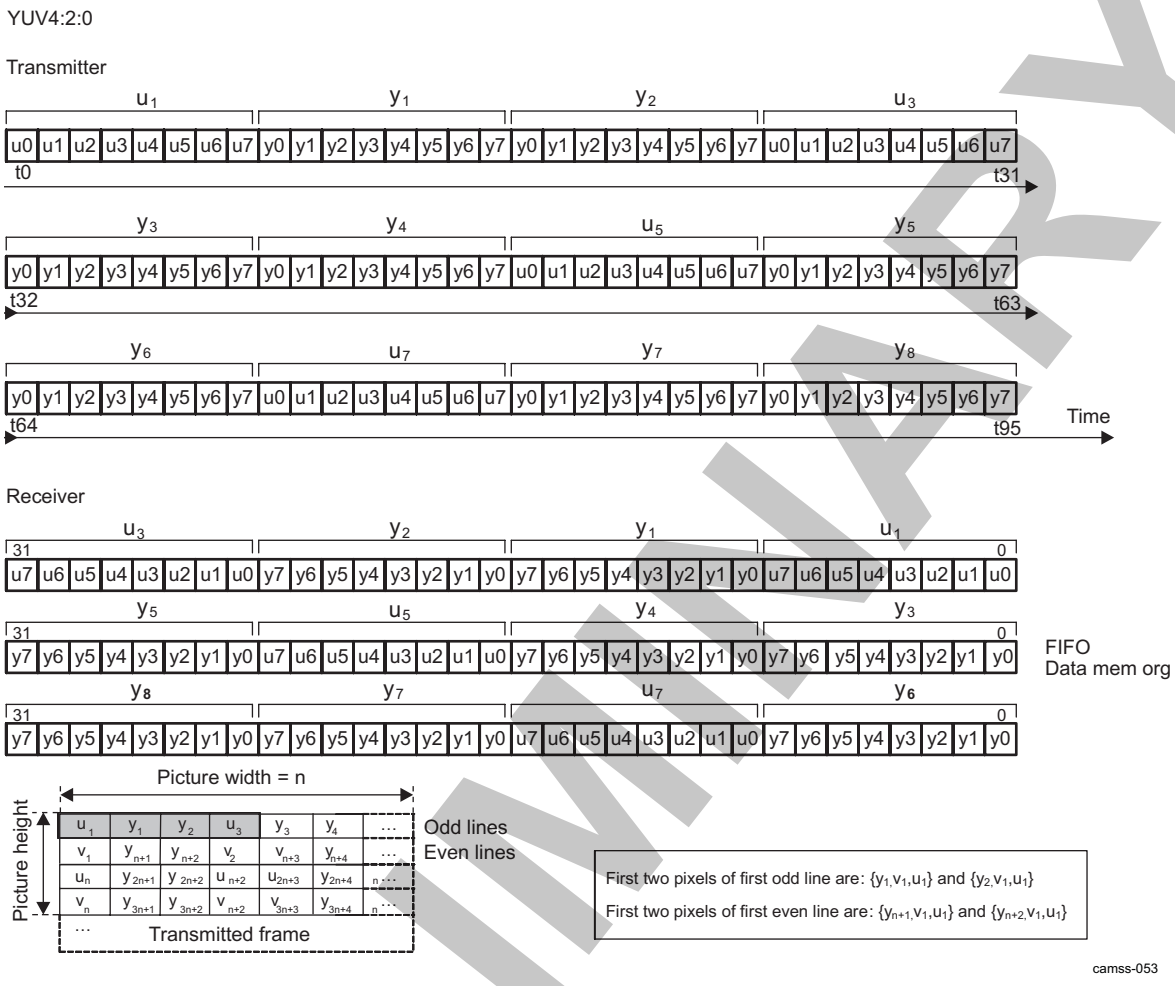
Figure 8-16. ISS CCP2 YUV4:2:0



8.2.4.1.1.4.2 ISS CCP2 RGB Operating Modes

8.2.4.1.1.4.2.1 ISS CCP2 RGB888

RGB888 data format can be output to memory in two formats: without data expansion and with data expansion.

If data expansion is used, the value of the 8 upper bits is programmable and can be set with an alpha value for computer graphics applications. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. The line length all together sent by the CCP2 receiver is a multiple of 3 x 32 bits to finish pixel reconstruction correctly.

Figure 8-17 is an example of RGB888 format. Set CCP2_LCx_CTRL[7:2] FORMAT to 0x6 to select RGB888 mode (24 bits) or to 0x7 to expand RGB888 over 32 bits.

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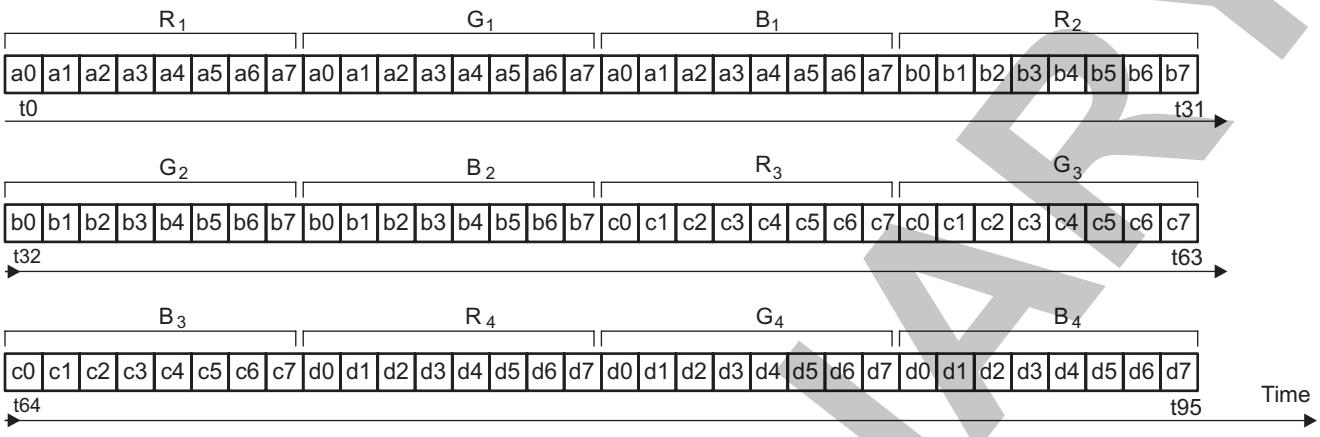
Figure 8-17. ISS CCP2 RGB888

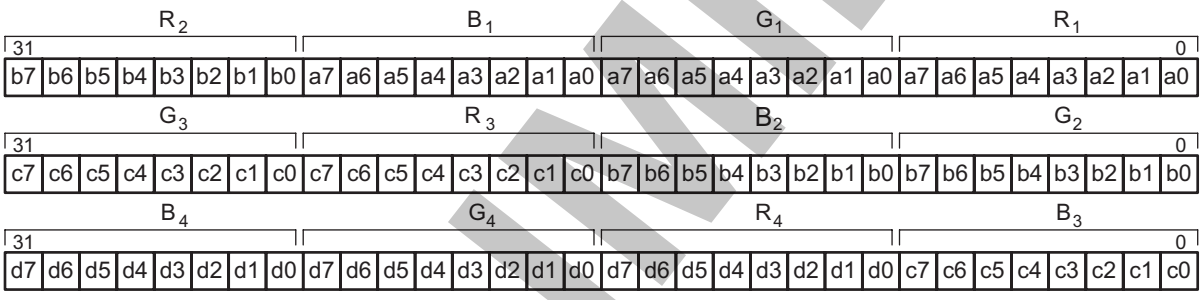
RGB888 Line width must be a multiple of three 32-bit words.

Transmitter

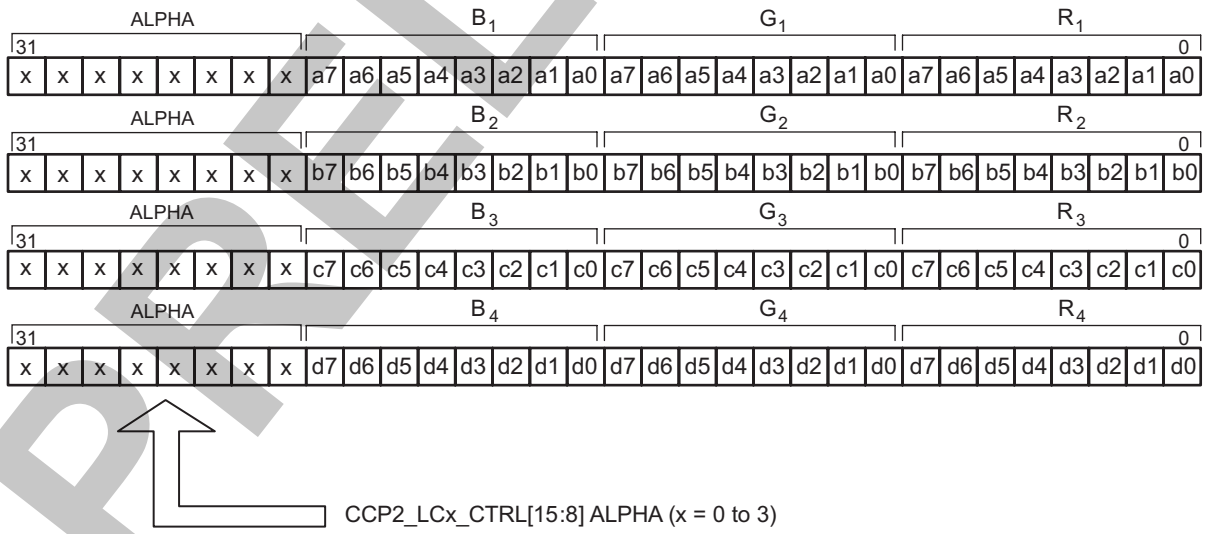


Receiver

Without data expansion



With data expansion



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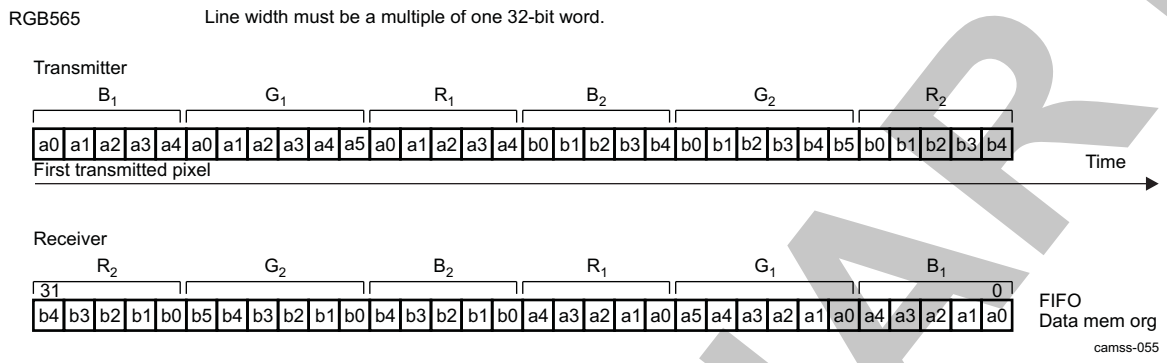
8.2.4.1.1.4.2.2 ISS CCP2 RGB565

For RGB565, the line length sent through the CCP2 receiver protocol is a multiple of 32 bits (see Figure 8-18). Set CCP2_LCx_CTRL[7:2] FORMAT to 0x6 to select RGB565 mode.

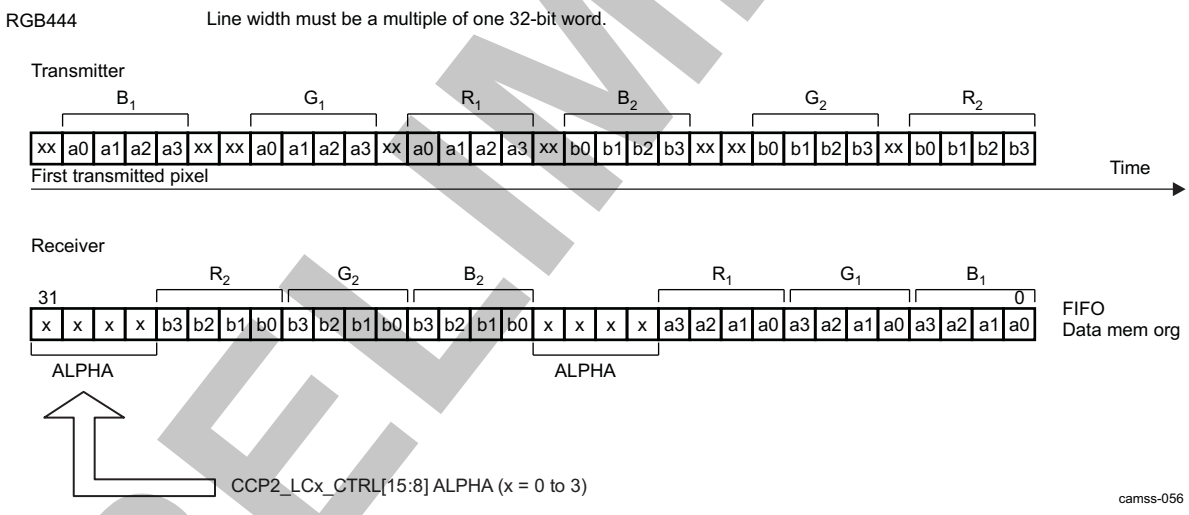
Figure 8-18. ISS CCP2 RGB565



8.2.4.1.1.4.2.3 ISS CCP2 RGB444

RGB444 data format is output to memory with data expansion. If data expansion is used, the value of the 4 upper bits is programmable and can be set with an alpha value for computer graphics applications. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits (see Figure 8-19). Set CCP2_LCx_CTRL[7:2] FORMAT to 0x4 to select RGB444 mode (12 bits expanded to 16).

Figure 8-19. ISS CCP2 RGB444



8.2.4.1.1.4.3 ISS CCP2 RAW Bayer Operating Modes

NOTE: For more information about packed RAW data, see Section 8.2.4.3.5.1, *ISS CCP2 Read Data From Memory*.

8.2.4.1.1.4.3.1 ISS CCP2 RAW6

RAW6 data format can be output to memory in two formats: without data expansion and with data expansion. The line length sent through the CSI receiver protocol is a multiple of 32 bits. The line all together sent by the CCP2 receiver is a multiple of 3 x 32 bits to finish pixel reconstruction correctly (the lowest common multiple of 32 and 6 is 96; that is, 3 x 32 bits).

Figure 8-20 shows the RAW6 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

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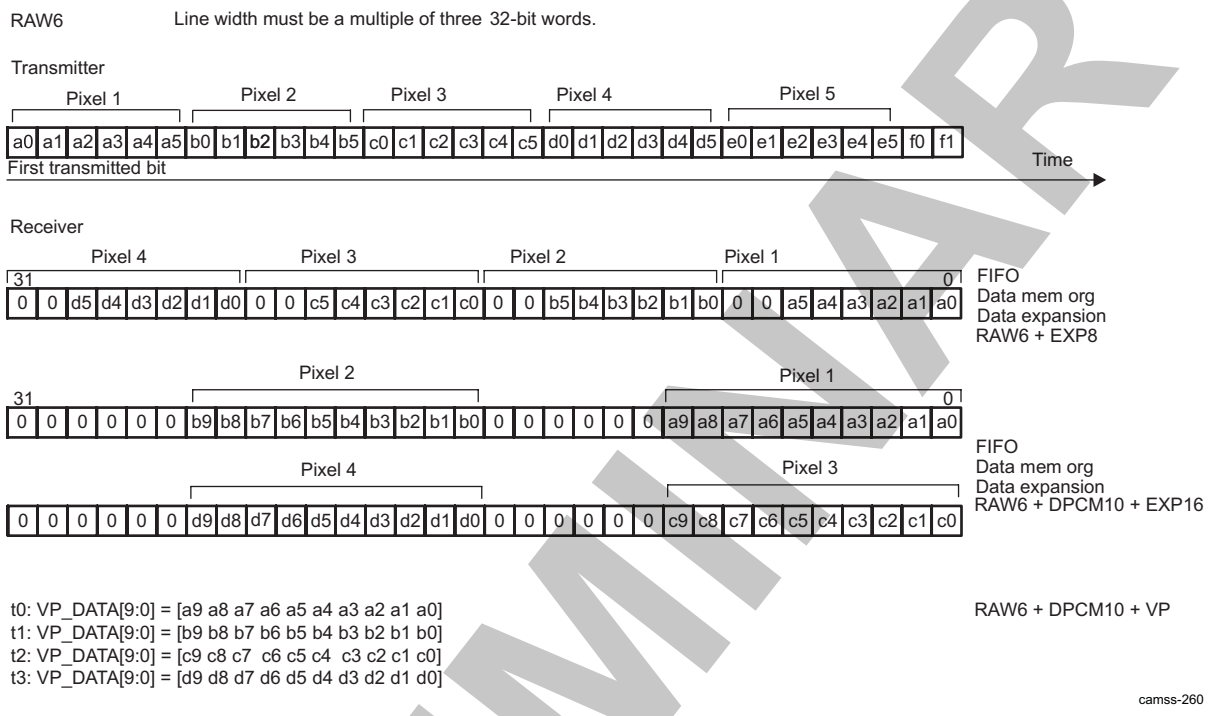
- 0x8 to select RAW6 mode expanded to 8-bit
- 0x9 to select RAW6 mode with DPCM decompression
- 10-bit and expansion to 16-bit
- 0xA to select RAW6 mode with DPCM decompression to 10-bit to video port

Figure 8-20. ISS CCP2 RAW6



NOTE: Use RAW8 data format to output RAW6 data format to memory.

8.2.4.1.1.4.3.2 ISS CCP2 RAW7

RAW7 data format can be output to memory in two formats: without data expansion and with data expansion. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. The line length all together sent by the CCP2 receiver is a multiple of 7 x 32 bits to finish the pixel reconstruction correctly (the lowest common multiple of 32 and 7 is 224; that is, 7 x 32 bits).

Figure 8-21 shows the RAW7 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

- 0xC to select RAW7 mode expanded to 8-bit
- 0xD to select RAW7 mode with DPCM decompression to 10-bit and expansion to 16-bit
- 0xE to select RAW7 mode with DPCM decompression to 10-bit to video port

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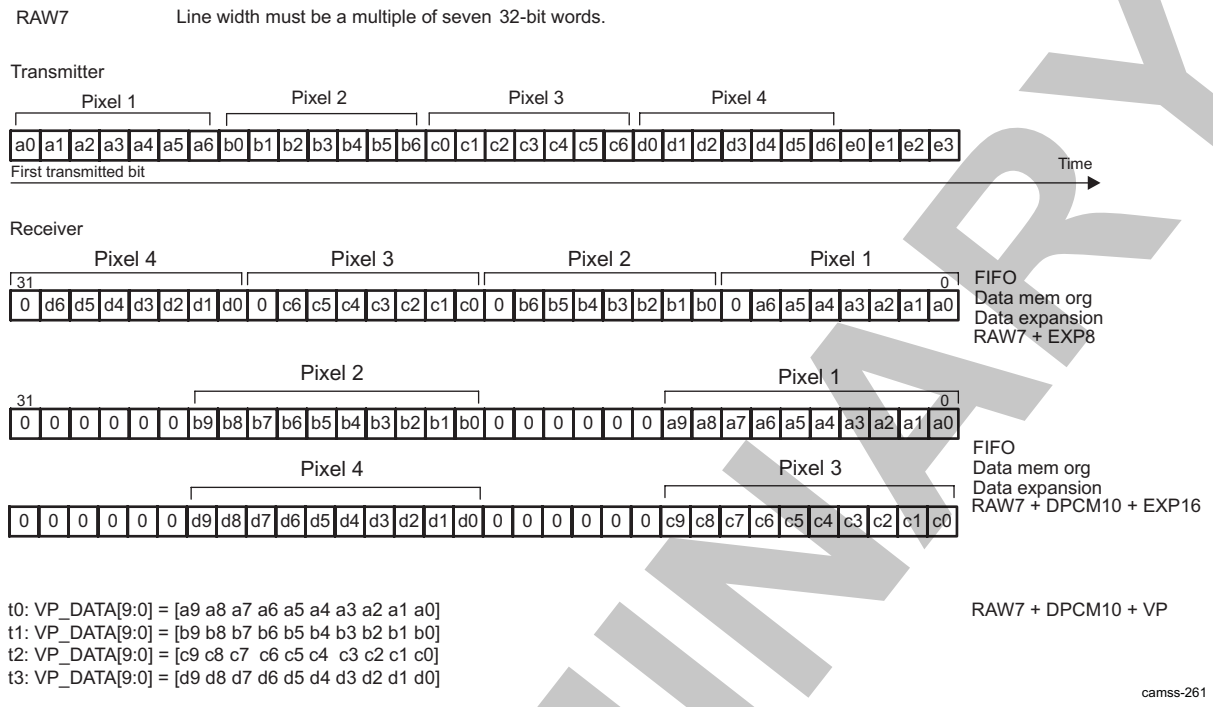
Figure 8-21. ISS CCP2 RAW7



NOTE: Use RAW8 data format to output RAW7 data format to memory.

8.2.4.1.1.4.3.3 ISS CCP2 RAW8

RAW8 data format can be output to memory. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits.

Figure 8-22 shows RAW8 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

- 0x10 to select RAW8
- 0x11 to select RAW8 mode with DPCM decompression to 10-bit and expansion to 16-bit
- 0x12 to select RAW8 mode with DPCM decompression to 10-bit to video port
- 0x20 to select RAW8 with A-Law decompression to RAW10

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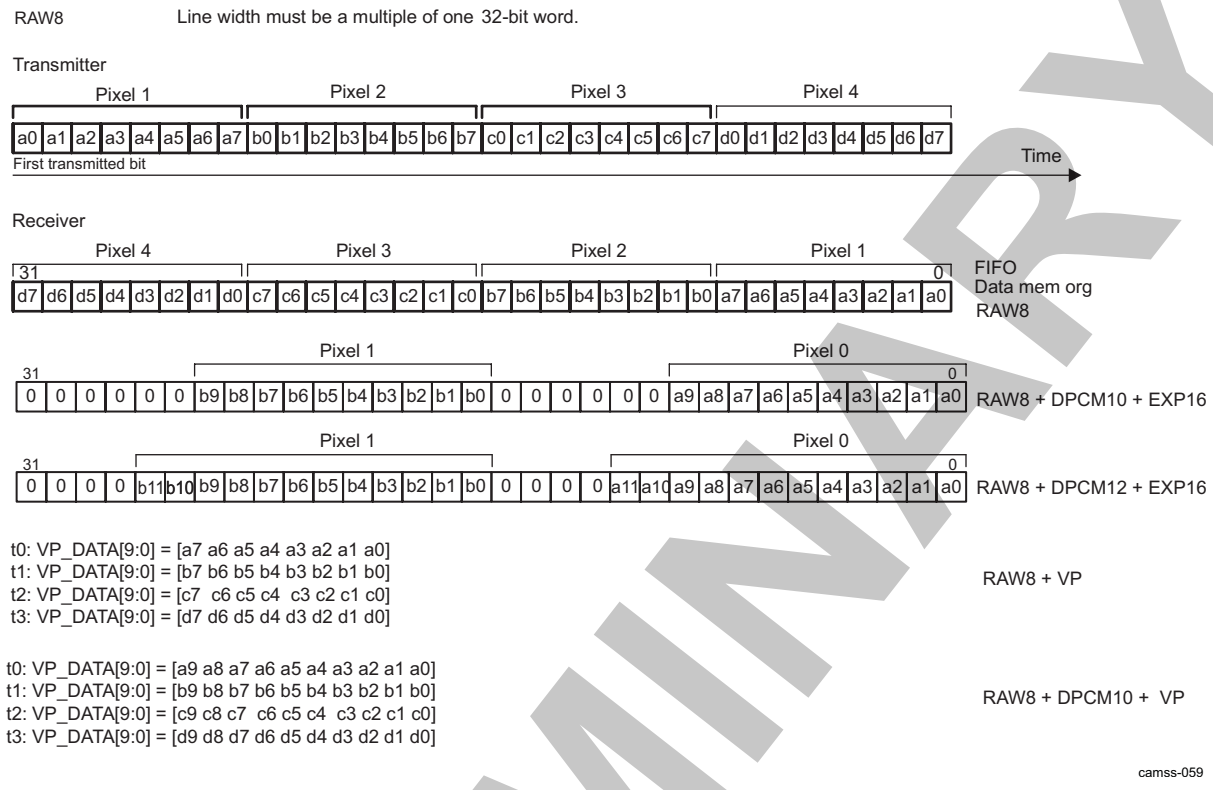
Figure 8-22. ISS CCP2 RAW8



NOTE: Use YUV4:2:2 + VP to output RAW8 data to the video port: YUV4:2:2 + VP is equivalent to RAW8 + VP.

8.2.4.1.1.4.3.4 ISS CCP2 RAW10

RAW10 data format can be output to memory in two formats: without data expansion and with data expansion. If data expansion is used, the 10-bit data are padded with 0s on a 16-bit word. The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. Furthermore, the line length all together sent by the CCP2 receiver is a multiple of 5 x 32 bits to finish pixel reconstruction correctly (the lowest common multiple of 32 and 10 is 320; that is, 10 x 32 bits).

RAW10 data format can be sent to the video port. Figure 8-23 shows the RAW10 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

- 0x14 to select RAW10
- 0x13 to select RAW10 mode with DPCM compression to 7-bit
- 0x16 to select RAW10 mode to video port
- 0x17 with DPCM compression to 7-bit with expansion to 8-bit
- 0x1B to select RAW10 compressed to 8-bit
- 0xB with DPCM compression to 6-bit
- 0xF to select RAW10 compressed to 6-bit with expansion to 8-bit
- 0x1E to select RAW10 compressed to 8-bit
- 0x20 to select RAW10 with A-Law compression to RAW8

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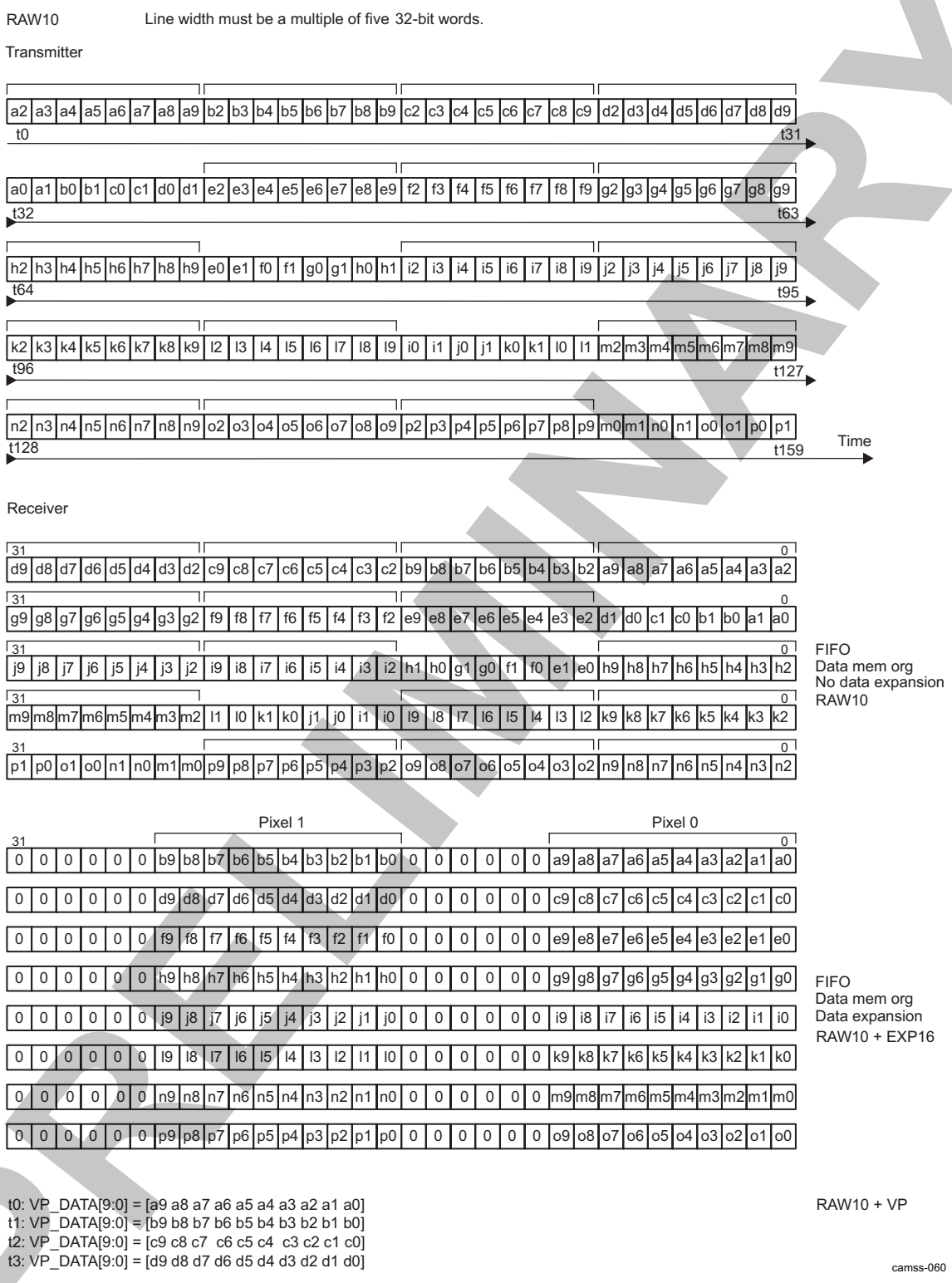
Figure 8-23. ISS CCP2 RAW10



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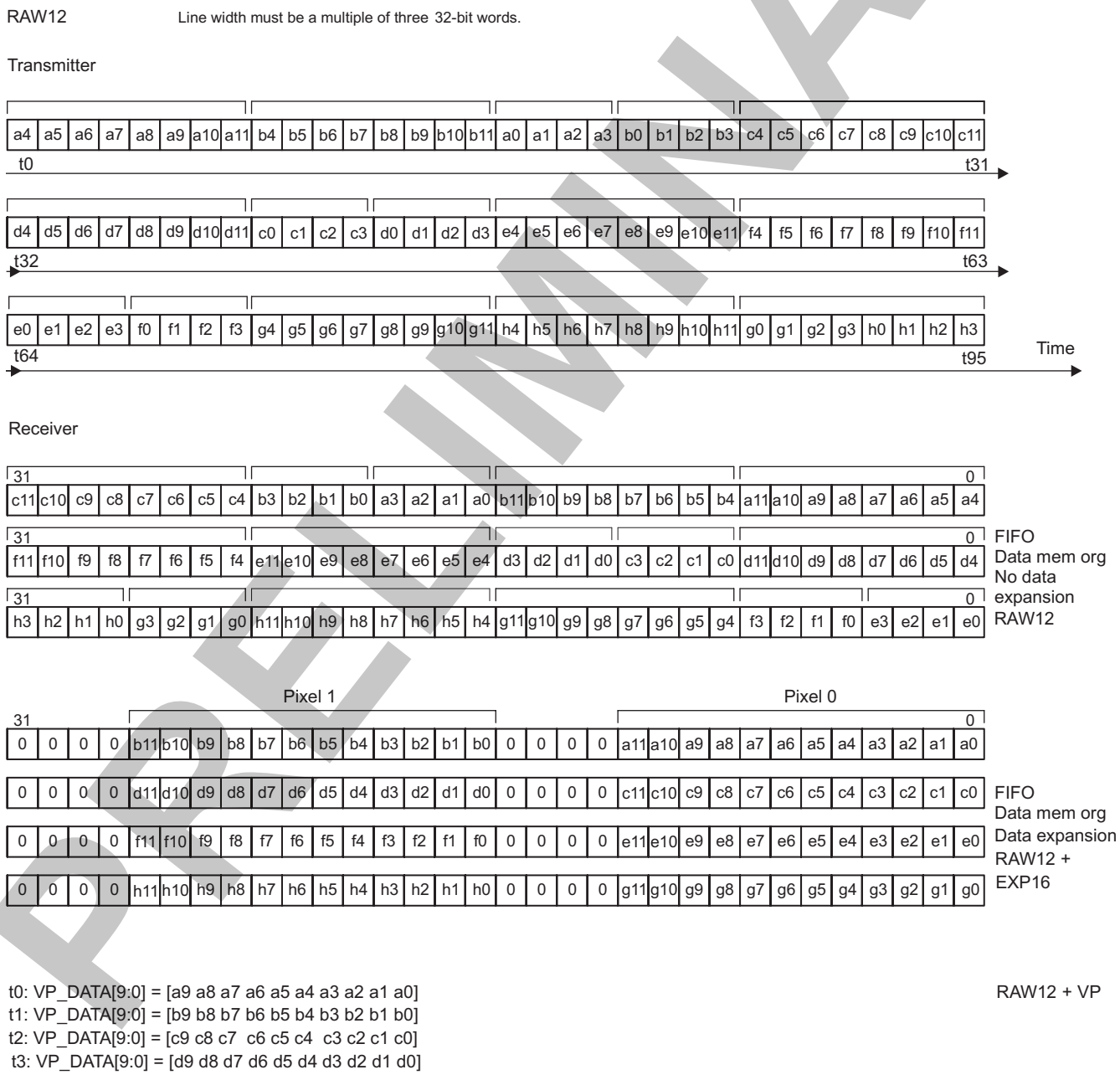
8.2.4.1.1.4.3.5 ISS CCP2 RAW12

RAW12 data format can be output to memory in two formats: without data expansion and with data expansion. If data expansion is used, the 12-bit data are padded with 0s on a 16-bit word. The line length sent through the CCP2 PHY is a multiple of 32 bits. The line length is a multiple of 3 x 32 bits to finish pixel reconstruction correctly (the lowest common multiple of 32 and 12 is 96; that is, 3 x 32 bits).

RAW12 data format can be sent to the video port. Figure 8-24 shows RAW12 format. Set CCP2_LCx_CTRL[7:2] FORMAT to:

- 0x18 to select RAW12
- 0x19 to select RAW12 mode with expansion to 16-bit
- 0x1A to select RAW12 mode to video port
- 0x17 with DPCM compression to 7-bit with expansion to 8-bit

Figure 8-24. ISS CCP2 RAW12



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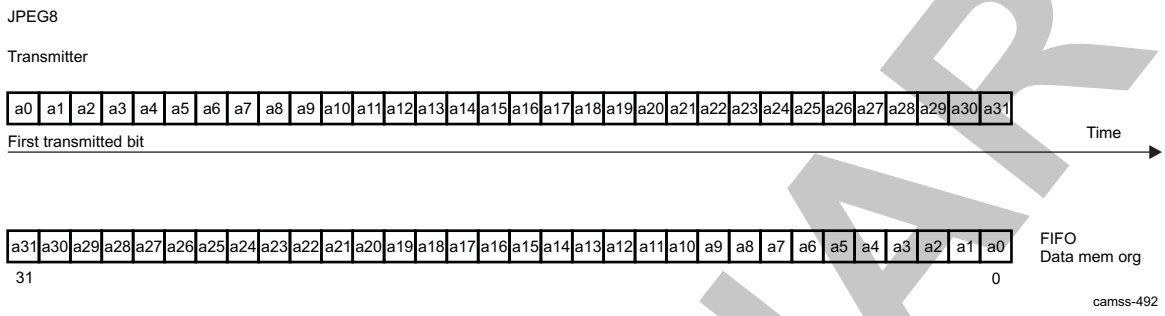
8.2.4.1.1.4.4 ISS CCP2 JPEG8 Operating Modes

The line length sent through the CCP2 receiver protocol is a multiple of 32 bits. The FSP code insertion on the transmitter side automatically ensures this line length. It is impossible to know in advance the size of a compressed stream. Figure 8-25 shows the JPEG8 and JPEG8 FSP format. Set CCP2_LCx_CTRL[7:2] FORMAT to 0x1C to select JPEG8 format, or to 0x1D to select JPEG8 format with FSP.

Figure 8-25. ISS CCP2 JPEG8 and JPEG8 FSP



In JPEG8 mode, the JPEG encoder on the sensor side must avoid generating data equal to the synchronization code and must deliver a synchronization-code-free bitstream for line-start and line-end before and after the transmitted data. For more information, see Section 8.2.4.1.1.2, *ISS CCP2 False Synchronization Protection Code*.

8.2.4.1.1.5 ISS CCP2 Data Transfer Through Write Master Port

The CCP2 receiver module uses its 64-bit master interface to transfer the data stored in the FIFO. The system can set the burst size to be used in the CCP2_CTRL BURST register. The recommended burst size is 128 bytes (0x4: 16 x 64-bit bursts are the most efficient for memory output); other sizes must be used only when issues are faced. The module tries to burst data whenever possible to increase system performance and save power. The module uses the appropriate register-selected burst size when the conditions (address is properly aligned, there is enough data in the FIFO to finish the line) are met; otherwise, it uses single requests.

For example, if the line consists of 50 pixels of 64-bit data and BURST = 0x4 (16 × 64-bit bursts), the module generates four times 16 x 64-bit bursts to transmit the whole line. The FIFO can have information about only two different lines.

The CCP2 engine supports tag count. The count is configurable through a register at the top level of the ISS (see Section 8.1.3, *ISS Register Manual*).

8.2.4.2 ISS CCP2 Integration

Figure 8-26 is an overview of the integration of the CCP2 interface in the ISS and device.

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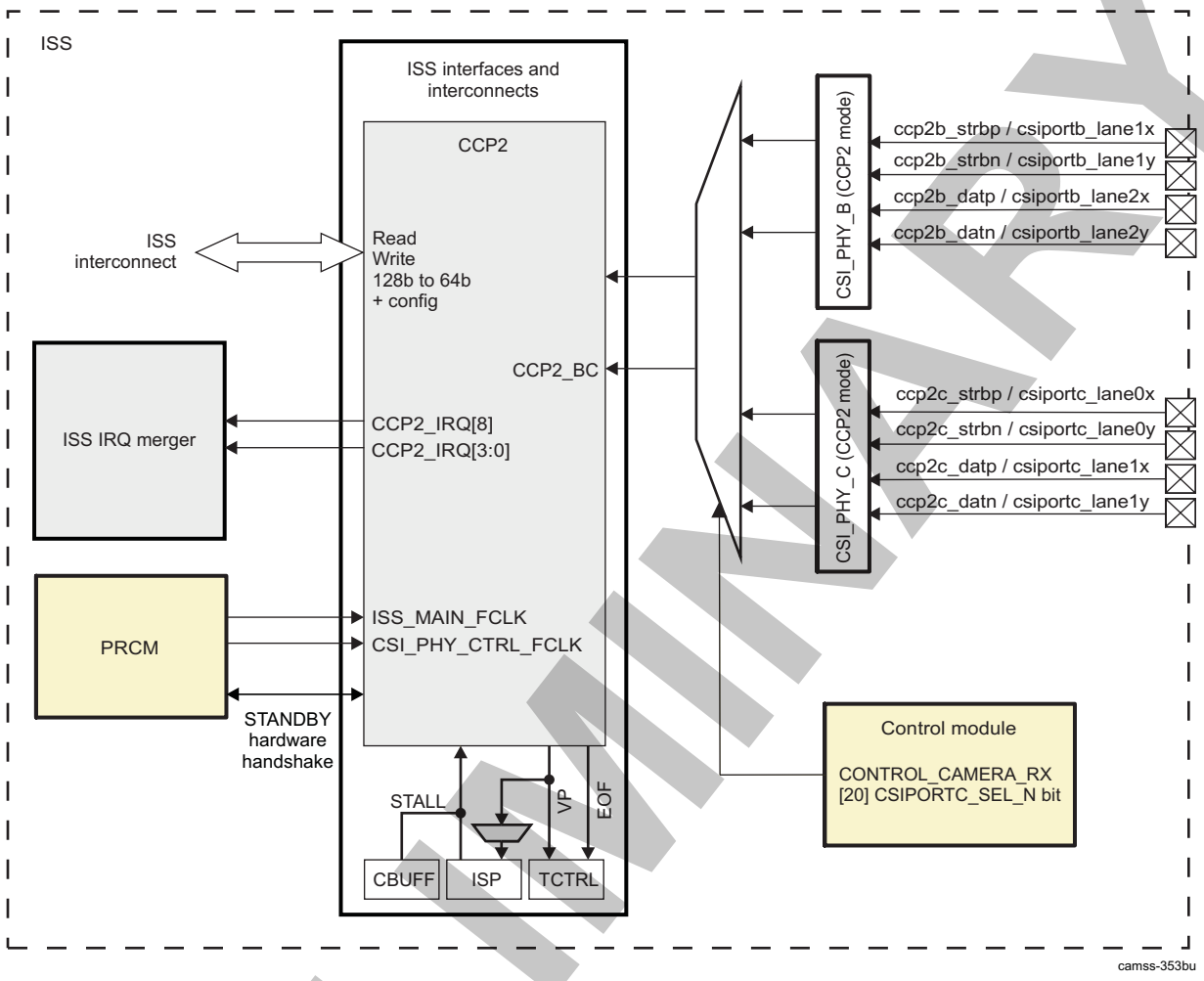
Figure 8-26. ISS CCP2 Integration



NOTE: Because CSI2_B/C and CCP2 receivers share CSI_PHY_B/C pins for camera interconnection, they cannot be used simultaneously. That is, for example, when CSI_PHY_C is configured for CCP2 mode, the CSI2_C receiver cannot use it at the same time in D-PHY mode. For ISP source select, see Section 8.1.1, *ISS Integration*, for ISP registers input selection and for top-level input select settings.

For power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

8.2.4.3 ISS CCP2 Functional Description

8.2.4.3.1 ISS CCP2 Overview

Figure 8-27 is the top-level block diagram of the CCP2 receiver. The CCP2 receiver receives serial data from a CCP2-compatible image sensor through one of the two CSI_PHYs (CSI_PHY_B or CSI_PHY_C), converts it to parallel data, extracts the logical channels, detects and extracts the synchronization codes, reformats the data, and outputs it through the VP interface (which is connected to the video preprocessing hardware [ISP]) or the ISS interconnect. The CCP2 can also read data from memory getting burst packets from the BTE when this feature has been enabled at compile time. For read data from memory, see Section 8.2.4.3.5, *ISS CCP2 Memory Read Channel*.

The CCP2 receiver video port interface is connected to the video preprocessing hardware (ISP).

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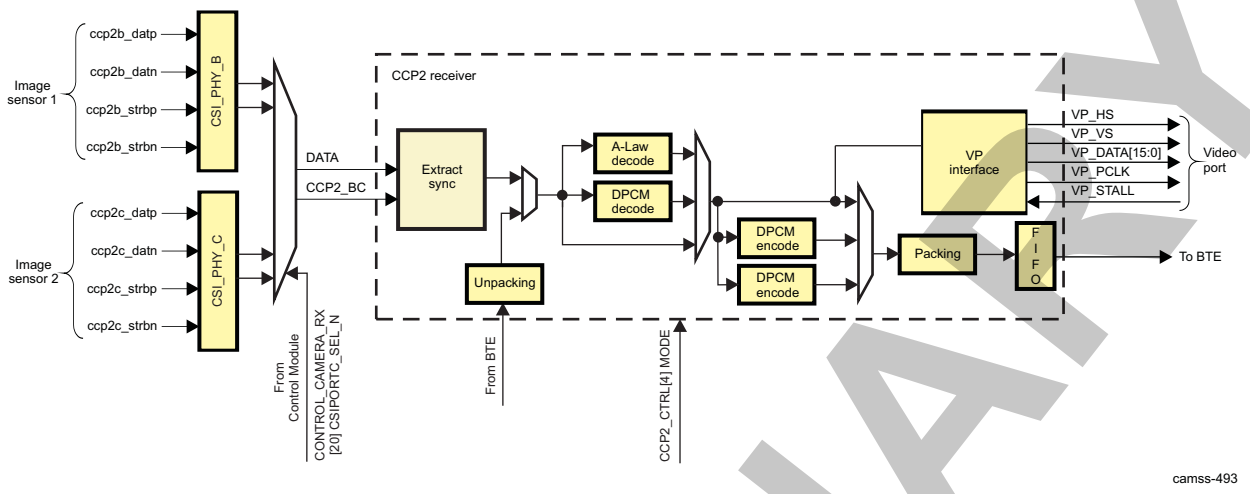
Figure 8-27. ISS CCP2 Receiver Block Diagram



8.2.4.3.2 ISS CCP2 PHY

The CCP2 receiver does not connect directly to a sensor (see Section 8.2.3, *ISS CSI PHY*). It uses a complex I/O physical layer. There are two CCP2 complex I/Os. One complex I/O (CSI_PHY_B) is shared with the CSI2_B receiver. Second complex I/O (CSI_PHY_C) is shared with the CSI2_C receiver. The CCP2 receiver can handle only one complex I/O traffic at a time. The selection of the complex I/O routed to the CCP2 receiver is done through the CONTROL_CAMERA_RX[20] CSIPORTC_SEL_N bit at the device Control Module level (see Figure 8-27, *ISS CCP2 Receiver Block Diagram* for more details). The CSI_PHYs are powered up by configuring the CSI2 receiver configuration register. For more information about the configuration of the CSI_PHYs, see Section 8.2.3.2.1, *ISS CSI PHY Functional Configuration*. The CCP2 serial interface is a unidirectional differential serial interface with two options for the PHYs: data/clock or data/strobe signals. After the CSI_PHYs are configured and initialization is done, the CCP2 mode can be selected and controlled by the CCP2_CTRL[4] MODE bit.

8.2.4.3.2.1 ISS CCP2 Data/Clock Signaling

Data/clock signaling consists of two parallel signals: data and data clock.

- The data signal carries bit serial data. The CCP2 transmitter writes the data on each falling edge of the clock. The data are usually transmitted bytewise, least-significant bit (LSB) first.
- The data clock signal carries the clock signal. The CCP2 transmitter writes the data on each falling edge of the clock. The CCP2 receiver reads the data on the rising edge of the clock.

8.2.4.3.2.2 ISS CCP2 Data/Strobe Signaling (CCP2 Only)

Data/strobe signaling consists of two parallel signals: data and data strobe.

- The data signal carries bit serial data.
- The data strobe signal carries the strobe signal. It toggles when the data signal does not change state.

The data signal or the strobe signal changes between 2 data bits. The data and strobe signals must not change simultaneously. The data and strobe signals are used in the receiver to reconstruct the transmission clock. Both fronts of the reconstructed clock are used to sample the data. Set the CCP2_CTRL[4] MODE bit and see Section 8.2.3, *ISS CSI PHY*, to set the data/clock or data/strobe function.

8.2.4.3.3 ISS CCP2 VP Interface

Table 8-57 summarizes the video interface signals. The video interface connects the CCP2 receiver module to the video preprocessing hardware (ISP). The interface is connected to a 16-bit video port. On the other side of the video port is the ISIF inside the ISP. The ISIF also uses the signals listed in Table 8-57 to synchronize pixel data sent to it by the CCP2 receiver.

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Table 8-57. ISS CCP2 Video interface Signals

Pin	Type[1]	Description
VP_HS	O	Line trigger output signal
VP_VS	O	Frame trigger output signal
VP_DATA[15:0]	O	Parallel output data: bits 0 to 15
VP_PCLK	O	Video port pixel clock. The frequency can be configured.
VP_STALL	I	Stalls data flow when data is read from memory

(1) I = Input; O = Output

When data is read from memory and sent to the video port, the data flow can be stalled by asserting the VP_STALL signal. Doing so does not overflow internal FIFOs: the CCP2 module adapts its read rate automatically.

The response time to the VP_STALL signal must not exceed two cycles: when VP_STALL is asserted, the CCP2 module can send 0, 1, or 2 pixels to the video port.

VP_STALL is asserted and deasserted synchronous to the functional clock.

NOTE: Stalling the video port for data received from the sensor may lead to internal overflows; VP_STALL must not be used for this purpose.

The pixel clock is generated from the functional clock. Clock pulses are gated based on the selected clock division factor and pixel availability. In other words, software must set the CCP2 receiver to ensure that the pixel clock:

- Never exceeds what the ISP can support: the top value set in the CCP2_CTRL[31:15] FRACDIV bit field
- Is sent only when valid pixels or blanking data must be sent

Also, software must set the number of clock pulses during horizontal blanking periods using the CCP2_CTRL1[1:0] BLANKING bit field.

- The CCP2 receiver stops generating horizontal blanking clock pulses when the number of pulses defined in the CCP2_CTRL1[1:0] BLANKING bit field are generated or when data for the next line arrives from the sensor.
- Free-running horizontal blanking can be selected only when data comes from the sensor.
- When data comes from memory, the CCP2 receiver ensures that the number of horizontal blanking pulses defined in the CCP2_CTRL1[1:0] BLANKING bit field is received. The CCP2 receiver stops generating horizontal blanking clock pulses when then number of pulses defined in the CCP2_CTRL1[1:0] BLANKING bit field is generated or when data for the next line arrives from the sensor.

NOTE: To work properly, the ISP requires a minimum of eight clock cycles in the horizontal blanking period and a minimum of 16 lines in the vertical blanking period. The pixel clock can be gated only when these intervals are respected. This is required to flush the pipeline of the different ISP modules. Figure 8-28 shows VP_PCLK gating during blanking periods.

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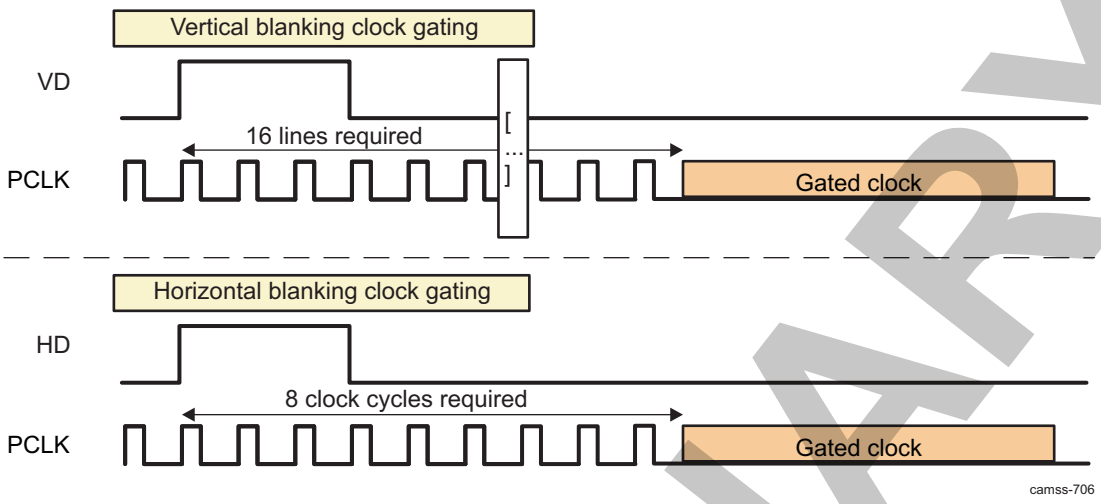
Figure 8-28. ISS CCP2 VP_PCLK Gating During Blanking Periods



Vertical blanking generation is controlled through the CCP2_CTRL[9] VP_CLK_FORCE_ON bit. The VP_PCLK clock is enabled during vertical blanking periods when this bit is set. This pushes pixels through the ISP processing pipe. It is needed, for example, when the ISP resizer uses the averager. Otherwise, hardware ensures only that at least four clock pulses are generated before the first pixel of each frame. It may be necessary for the clock to keep running after the frame end to flush internal pipelines. In that case, an interrupt request (IRQ) or status bit is typically present in the attached hardware that indicates when the VP_PCLK clock is no longer needed (for example, an end of processing interrupt). The module leaves the vertical blanking state when new data is received from the sensor or the memory read channel.

The configured pixel clock is used for active and blanking periods.

Table 8-58 shows how RAW and YUV data is sent over the video port. The data is sent to the ISIF if ISP is used. For the ISIF details about video port data, see Section 8.3.1 *ISS ISP*.

Table 8-58. ISS CCP2 Video Port Data Mapping

Format	Video Port DATA[15:0]															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW6	0	0	0	0	0	0	0	0	0	0	R5	R4	R3	R2	R1	R0
RAW7	0	0	0	0	0	0	0	0	0	R6	R5	R4	R3	R2	R1	R0
RAW8	0	0	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0
RAW10	0	0	0	0	0	0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
RAW12	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
RAW14	0	0	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
RAW16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
YUV4:2:2	0	0	0	0	0	0	0	0	U7	U6	U5	U4	U3	U2	U1	U0
	0	0	0	0	0	0	0	0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	0	0	0	0	0	0	0	0	V7	V6	V5	V4	V3	V2	V1	V0
	0	0	0	0	0	0	0	0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

8.2.4.3.4 ISS CCP2 Data Compression

The data compression technique used is DPCM and pulse code modulation (PCM).

The CCP2 receiver performs on-the-fly compression and decompression. The compressed/decompressed data is passed to the video preprocessing hardware or stored in memory.

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The data compression method is lossy and does not require any information outside the current encoded/decoded line. This means that all the image lines can be encoded and decoded separately.

Two different predictors are used:

- The simple predictor

  This predictor uses only the previous same color component value as a prediction value. Therefore, only 2-pixel memory is required.
- The advanced predictor

  This predictor uses four previous pixel values, when the prediction value is evaluated. This means that also the other color component values are used, when the prediction value is defined.

The preferable use is that the simple predictor is used with 10 bits to 8 bits or 12 bits to 8 bits conversion (10-8-10 or 12-8-12) and the advanced predictor is used with 10 bits to 7 bits and 10 bits to 6 bits conversions (10-7-10 and 10-6-10). The advanced predictor gives slightly better prediction for pixel value; thus, the image quality can be improved with it. Because the simple predictor is very simple, the processing power and memory requirements are reduced with it, when the image quality is already high enough.

Select the predictor with the CCP2_LCx_CTRL[18] DPCM_PRED bit.

8.2.4.3.5 ISS CCP2 Memory Read Channel

The memory channel can perform the following operations:

- Reads data from memory. It is unpacked and DPCM or A-Law decompressed if necessary.
- Sends data to the video preprocessing hardware
- Sends data back to memory. It can be DPCM or A-Law compressed and packed before it is sent to memory.

It cannot receive its input data directly from the sensor, and the logical channels are disabled when the memory channel is enabled.

Table 8-59 summarizes supported modes for memory-to-memory operations.

NOTE: Video port and memory destinations are mutually exclusive.

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Table 8-59. ISS CCP2 Memory-to-Memory Supported Operations

Memory Input	Memory Output																				
	RAW 6	RAW 6+PACK	RAW 6+DPCM	RAW 6+PACK+DPCM	RAW 6+DPCM_ADV	RAW 6+PACK+DPCM_ADV	RAW 7	RAW 7+PACK	RAW 7+DPCM	RAW 7+PACK+DPCM	RAW 7+DPCM_ADV	RAW 7+PACK+DPCM_ADV	RAW 8	RAW 8+DPCM	RAW 8+DPCM12	RAW 8+ALAW10	RAW 10	RAW 10+PACK	RAW 12	RAW 12+PACK	RAW 14	RAW 16
RAW6																						
RAW6 + PACK																						
RAW6 + DPCM																	X	X				
RAW6 + PACK + DPCM																	X	X				
RAW6 + DPCM_ ADV																	X	X				
RAW6 + PACK + DPMC_ ADV																	X	X				
RAW7																						
RAW7 + PACK																						
RAW7 + DPCM																	X	X				
RAW7 + PACK + DPCM																	X	X				
RAW7 + DPCM_ ADV																	X	X				
RAW7 + PACK + DPMC_ ADV																	X	X				
RAW8																						
RAW8 + DPCM																	X	X				
RAW8 + DPCM12																			X	X		

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Table 8-59. ISS CCP2 Memory-to-Memory Supported Operations (continued)

Memory Input	Memory Output																					
	RAW 6	RAW 6+PACK	RAW 6+DPCM	RAW 6+PACK+DPCM	RAW 6+DPCM_ADV	RAW 6+PACK+DPCM_ADV	RAW 7	RAW 7+PACK	RAW 7+DPCM	RAW 7+PACK+DPCM	RAW 7+DPCM_ADV	RAW 7+PACK+DPCM_ADV	RAW 8	RAW 8+DPCM	RAW 8+DPCM12	RAW 8+ALAW10	RAW 10	RAW 10+PACK	RAW 12	RAW 12+PACK	RAW 14	RAW 16
RAW8 + ALAW10																	X	X				
RAW10			X	X	X	X			X	X	X	X		X								
RAW10 + PACK			X	X	X	X			X	X	X	X		X								
RAW12																						
RAW12 + PACK																						
RAW14																						
RAW16																						

Table 8-60 summarizes supported modes for memory-to-video port operations.

Table 8-60. ISS CCP2 Memory-to-Video Port Supported Formats

Memory Input	Video Port Output						
	RAW6	RAW7	RAW8	RAW10	RAW12	RAW14	RAW16
RAW6	X						
RAW6 + PACK	X						
RAW6 +DPCM				X			
RAW6 + PACK + DPCM				X			
RAW6 + DPCM_ADV				X			
RAW6 + DPCM_ADV + PACK				X			
RAW7		X					
RAW7 + PACK		X					
RAW7 + DPCM				X			
RAW7 + PACK + DPCM				X			
RAW7 + DPCM_ADV				X			
RAW7 + DPCM_ADV + PACK				X			

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Table 8-60. ISS CCP2 Memory-to-Video Port Supported Formats (continued)

Memory Input	Video Port Output						
	RAW6	RAW7	RAW8	RAW10	RAW12	RAW14	RAW16
RAW8			X				
RAW8 + DPCM				X			
RAW8 + ALAW10				X			
RAW8 + DPCM12					X		
RAW10				X			
RAW10 + PACK				X			
RAW12					X		
RAW12 + PACK					X		
RAW14						X	
RAW16							X

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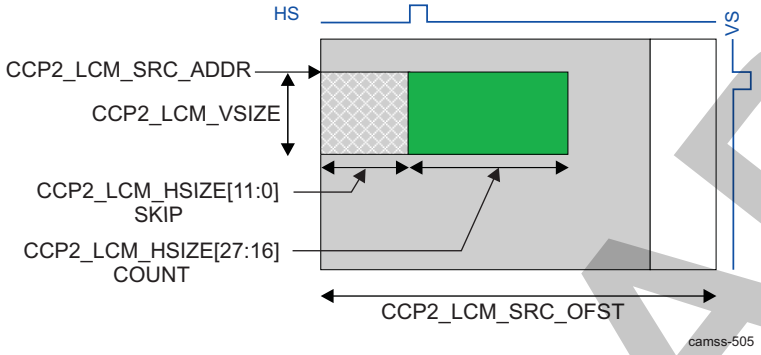
8.2.4.3.5.1 ISS CCP2 Read Data From Memory

Figure 8-29 shows the data organization in memory.

Figure 8-29. ISS CCP2 Data Organization in Memory



The user chooses the start address and the line length using the CCP2_LCM_SRC_ADDR and CCP2_LCM_SRC_OFST registers. The image start address normally must point to the beginning of a line because of packing constraints. However, it does not necessarily point to the first line of the frame in memory. The CCP2_LCM_VSIZE[27:16] COUNT bit field specifies the total line count to be read from memory.

It is also possible to skip a certain pixel count (CCP2_LCM_HSIZE[11:0] SKIP) from the start of the line. Thus, they are not sent to the video port or back to memory. The CCP2_LCM_HSIZE[27:16] COUNT bit field specifies the horizontal size of the image. The pixels after the right boundary of the image are not read from memory.

When data are sent to the video port, throughput is imposed by the selected VP_PCLK. Otherwise, it is imposed by the selected interconnect read port clock. The interconnect read rate can be throttled (limiting the maximum data read speed for memory-to-memory operation) using the CCP2_LCM_CTRL[4:3] READ_THROTTLE bit field. Therefore, it is possible to read the unused data at a higher rate than the used video port data rate. This provides better performance than framing the image in the video preprocessing hardware.

The data storage format in memory is defined by the CCP2_LCM_CTRL[18:16] SRC_FORMAT and CCP2_LCM_CTRL[23] SRC_PACK bit fields.

Not all I/O format combinations are valid. For more information, see Table 8-59 and Table 8-60.

Figure 8-30 shows how data are packed in memory. Pixel order (left to right in the image) is alphabetical (a, b, c). Therefore, data storage is little endian.

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Figure 8-30. ISS CCP2 Data Organization Packing in Memory

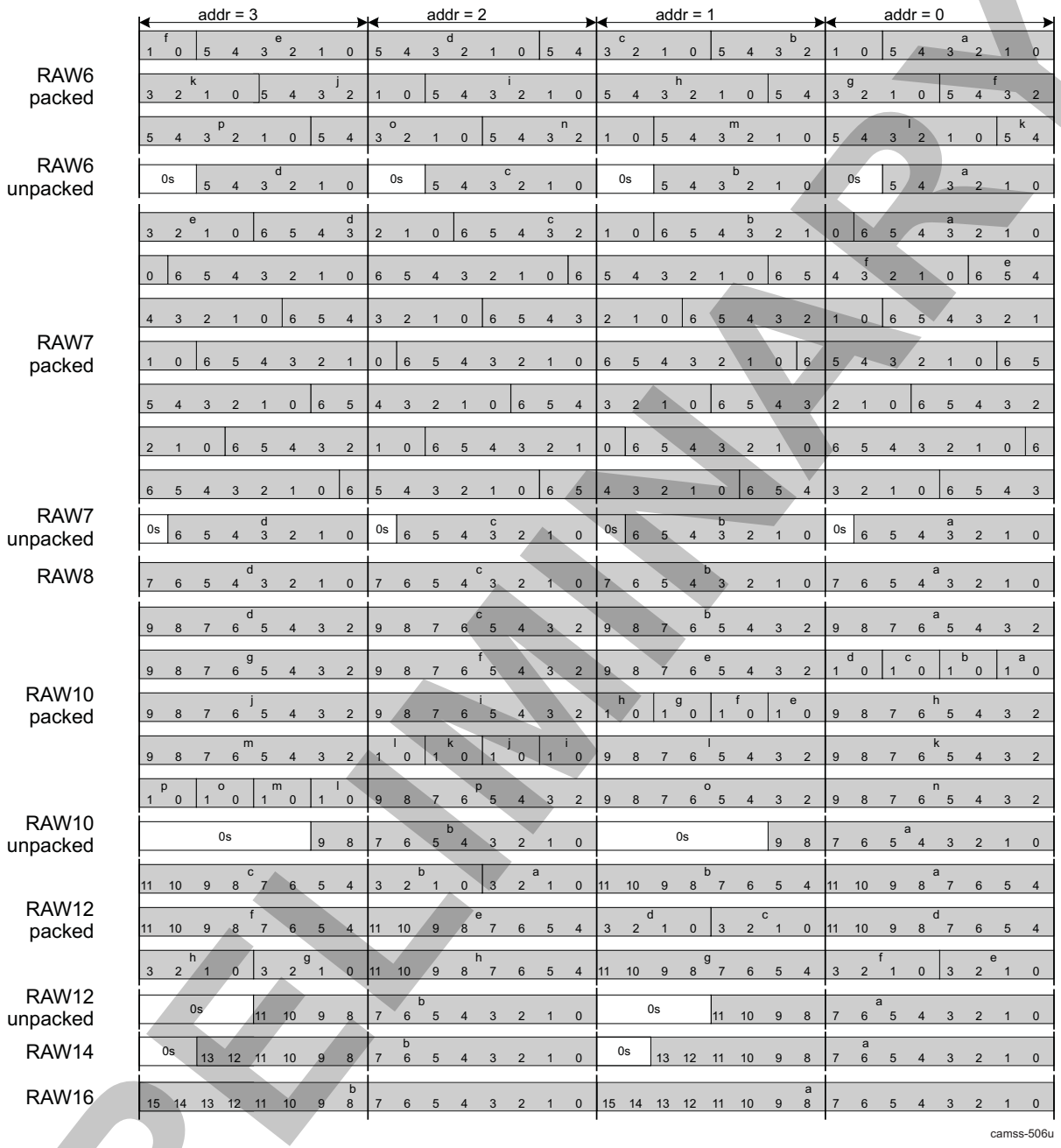

Table 8-61 summarizes the storage reduction versus unpacked format and image width restrictions when data packing is used. The image width applies to the data width multiple in pixels that must be stored to have storage reduction. Moreover, because each address is 8 bits long, the percentage shows how many bits out of 8 are to be packed in the empty space from another pixel address. A pixel is selected and split. One of the parts is put into another pixel address empty space. When unpacked, each pixel bit is stored continuously again.

Table 8-61. ISS CCP2 Data Packing Benefit and Constraints

	Bits Per Pixel		Storage Reduction	Width Multiple (Pixels)
	Packed	Unpacked		
RAW6	6	8	25%	16
RAW7	7	8	13%	3

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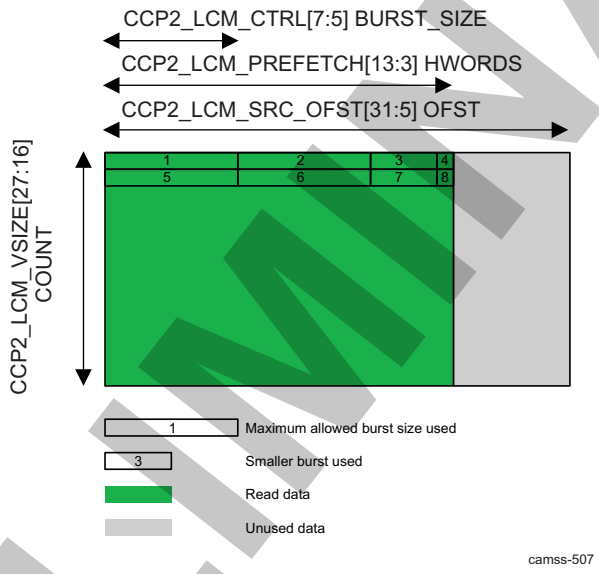
Table 8-61. ISS CCP2 Data Packing Benefit and Constraints (continued)

	Bits Per Pixel		Storage Reduction	Width Multiple (Pixels)
	Packed	Unpacked		
RAW8	8	8	0%	4
RAW10	10	16	38%	16
RAW12	12	16	25%	8

8.2.4.3.5.2 ISS CCP2 Memory Read Port Burst Generation

Hardware always uses the largest possible burst size according to the setup. The amount of data read from memory can be higher than what is actually used by the CCP2 receiver. Only full 64-bit burst words are read back from memory. Figure 8-31 shows the data organization and the relationship between the different parameters controlling the burst generation.

Figure 8-31. ISS CCP2 Data Organization in Memory



NOTE:

- A minimum burst size of 2 must be selected for correct operation.
- The HWORDS bit field must be even for correct operation.

The CCP2_LCM_SRC_ADDR register address of the first data to read is aligned to a 32-byte boundary. The read port fetches CCP2_LCM_PREFETCH[13:3] HWORDS of 64-bit words per line using the longest possible burst computed from the CCP2_LCM_CTRL[7:5] BURST_SIZE bit field and the remaining data to be fetched. Burst size of 128 bytes is preferred. When the CCP2 receiver is configured to fetch more data than required, extra data are dropped internally.

8.2.4.3.5.3 ISS CCP2 MFLAG Mechanism and Arbitration

The MFLAG mechanism allows a dynamic increase of the priority of CCP2 real-time traffic, when required, based on the fullness of the CCP2 DMA read and write buffers. Programmable buffer thresholds are used to indicate when the local MFLAG signal is generated, which is then provided to the L3 interconnect for granting or prioritizing OCP requests. The out band CCP2 MFLAG signal is asynchronous to any ongoing OCP transaction. The threshold corresponds to the fullness of DMA buffer, and is defined by the following threshold parameters:

- High threshold: When the corresponding pipeline buffer reaches the programmed value, the associated local MFLAG signal goes high (asserted). The value is set in the CCP2_CTRL1[30:24] LEVH register.

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- Low threshold: When the corresponding pipeline buffer reaches the programmed value, the associated local MFLAG signal goes low (deasserted). The value is set in the CCP2_CTRL1[22:16] LEVL register.

8.2.4.3.5.4 ISS CCP2 Video Port

The video port always receives unpacked data. It can be enabled using the CCP2_LCM_CTRL[2] DST_PORT bit. Its clock can be selected with the CCP2_CTRL[31:15] FRACDIV bit field and gated or not during frame blanking periods using the CCP2_CTRL[9] VP_CLK_FORCE_ON bit.

The data format used by the video port is defined by the CCP2_LCM_CTRL[26:24] DST_FORMAT bit field. For a list of supported modes, see Table 8-60.

8.2.4.3.5.5 ISS CCP2 Encode, Pack, and Store Data

This stage is used only when data are sent to memory. Memory destination is selected using the CCP2_LCM_CTRL[2] DST_PORT bit. The output data format is defined by the CCP2_LCM_CTRL[26:24] DST_FORMAT bit field and the CCP2_LCM_CTRL[31] DST_PACK bit. Not all possible combinations are supported; see Table 8-59 for details.

The destination address and offset for the output data of the memory channel are set by the CCP2_LCM_DST_ADDR and CCP2_LCM_DST_OFST registers.

Because of alignment constraints on the interconnect port, the output image width restrictions in Table 8-62 apply.

Table 8-62. ISS CCP2 Output Width Restrictions in Memory-to-Memory Operation

Format	Bits per Pixel	Width Multiple of(1)	Note
RAW6	8	1	Full 32-bit words are written at the end of the line. This last word can eventually include 0s.
RAW6 packed	6	1	
RAW7	8	1	
RAW7 packed	7	1	
RAW8	8	1	
RAW10	16	1	
RAW10 packed	10	16	
RAW12	16	1	Same constraints as RAW8
RAW12 packed	12	8	

(1) In continuous mode, lines must be multiples of 128 bits. In 2D mode, lines must start on 128-bit boundaries.

For example, when RAW6 packed data are written to memory, any output width is allowed. However, only full 32-bit words are written to memory. This eventually overwrites some data in memory at the end of a line.

The supported output width is restricted for packed RAW10 and RAW12 data because of the particular bit ordering in those formats (see Figure 8-30).

When the DST_OFST bit is set to 0, start of lines are aligned on 4-byte boundaries. When DST_OFST is not set to 0, data are aligned on 32-byte boundaries.

NOTE: The RAW6, RAW7, and DPCM data formats do not apply to the MIPI CSI1-compatible mode.

8.2.4.3.5.6 ISS CCP2 DPCM Decompression History

The DPCM compression algorithm can encode the difference between consecutive samples in a line instead of the actual samples value to reduce the amount of data to store. The drawback is that lines must always be decoded from the beginning (the first samples of a line are always encoded as PCM).

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The CCP2 receiver has a mechanism to preserve the DPCM decode history for each line to avoid decoding the same samples multiple times when vertical frame division mode is used.

The typical use case (also known as vertical frame division mode) is when an image is wider than the ISP can process on the fly, but the image must be processed. Therefore, the image is cut into multiple vertical slices that are processed sequentially by the ISP. The slices are stitched together in the SDRAM after ISP processing through proper address generation in the ISP. Because of various alignment constraints in the ISP, the slices sent to ISP must overlap. Without preserving the DPCM history, all lines from the beginning of the second (and other consecutive) vertical slice would have to be recoded, which would lead to performance degradation.

Writing DPCM history information into the system memory is enabled by setting the CCP2_LCM_HISTORY[16] EN_HIST_WR bit. The CCP2_LCM_HISTORY[15:0] HIST_EXPORT bit field defines the position at which history data is written to memory. The position is counted from the beginning line. The first decoded pixel has position 0. The last decoded pixel has position CCP2_LCM_HSIZE[14:0] SKIP + CCP2_LCM_HSIZE[30:16] COUNT - 1. The CCP2_LCM_HISTORY[15:0] HIST_EXPORT bit field is used to choose the resume position and allows support of overlapping vertical slices. The CCP2 receiver always writes 8 bytes of history data per line to the SDRAM regardless of the chosen DPCM format. The CCP2 receiver uses the interface bursts to send history data to memory.

DPCM history data holds the decoded value of four samples. The CCP2 receiver exports samples of positions:

- CCP2_LCM_HISTORY[15:0] HIST_EXPORT – 3
- CCP2_LCM_HISTORY[15:0] HIST_EXPORT – 2
- CCP2_LCM_HISTORY[15:0] HIST_EXPORT – 1
- CCP2_LCM_HISTORY[15:0] HIST_EXPORT

Every sample is coded on 16 bits, and several MSBs are unused. The valid range for CCP2_LCM_HISTORY[15:0] HIST_EXPORT is [3.. CCP2_LCM_HSIZE[14:0] SKIP + CCP2_LCM_HSIZE[30:16] COUNT – 1]. History data can be exported even when data is not sent to the video port or ISS interconnect port (i.e. the condition CCP2_LCM_HISTORY[15:0] HIST_EXPORT < CCP2_LCM_HSIZE[14:0] SKIP is valid).

The source and destination addresses for history and pixel data depend on the CCP2_LCM_HISTORY[18] HIST_DATA_DST bit:

- Memory to video port (CCP2_LCM_HISTORY[18] HIST_DATA_DST = 0)
  - Pixel data read: CCP2_LCM_SRC_ADDR + Y*CCP2_LCM_SRC_OFST
  - History data read: CCP2_LCM_DST_ADDR + Y*8
  - Pixel data write: (video port)
  - History data write: CCP2_LCM_DST_ADDR + Y*8
- Memory to memory (CCP2_LCM_HISTORY[18] HIST_DATA_DST = 1)
  - Pixel data read: CCP2_LCM_SRC_ADDR + Y*CCP2_LCM_SRC_OFST
  - History data read: CCP2_LCM_HIST_ADDR + Y*8
  - Pixel data write: CCP2_LCM_DST_ADDR + Y*CCP2_LCM_DST_OFST
  - History data write: CCP2_LCM_HIST_ADDR + Y*8,

where Y represents the line number in the image. It starts from 0 and is incremented by one for each line (i.e. Y = 0 for the 1st image line, Y = 1 for the 2nd image line, etc.).

Reading back history information is enabled by setting the CCP2_LCM_HISTORY[17] EN_HIST_RD register. The CCP2 receiver always reads 8 bytes of history data per line from SDRAM regardless of the chosen DPCM format. The CCP2 receiver uses single interface requests to read history data from memory. For each line, the DPCM decoder fetches 8 bytes of history data and CCP2_LCM_PREFETCH[15:3] HWORDS words of 64-bits of compressed pixel data from memory.

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NOTE: In memory to memory mode, new histogram data overwrites the old one when CCP2_LCM_HISTORY[16] EN_HIST_WR = 1 and CCP2_LCM_HISTORY[17] EN_HIST_RD = 1. However, as reads are done before writes, there is no risk of data corruption. Software must copy the history date before enabling the processing, if the same history data needs to be used multiple times and CCP2_LCM_HISTORY[16] EN_HIST_WR = 1 and CCP2_LCM_HISTORY[17] EN_HIST_RD = 1.

The values of CCP2_LCM_HISTORY[15:0] HIST_EXPORT bit field of the write pass and CCP_LCM_SRC_ADDR register of the read pass must match, in order to avoid generation of corrupted data. The CCP2_LCM_HSIZE[14:0] SKIP and CCP2_LCM_HSIZE[30:16] COUNT bit fields can be used to define with pixel accuracy what is sent to the video port (if CCP2_LCM_HISTORY[18] HIST_DATA_DST = 0) or ISS interconnect port (if CCP2_LCM_HISTORY[18] HIST_DATA_DST = 1).

8.2.4.4 ISS CCP2 Programming Model

This section describes the programming model of the CCP2 receiver.

8.2.4.4.1 ISS CCP2 Programming Hardware Setup/Initialization

This section discusses the configuration of the CCP2 receiver required before image capture can begin. Before using the receiver, a CSI_PHY initialization in CCP2 mode must be made for CSI_PHY_B or CSI_PHY_C, whichever is associated with the CCP2 receiver. See Section 8.2.3.2.3, *ISS CSI PHY (CCP2 Mode) and Link Initialization Sequence.*

NOTE: The setup/initialization previously explained is valid only when the external sensor is used. If the user plans to use the logical memory channel (LCM) or debug mode (CCP2_CTRL[13] DBG_EN = 0x1) instead of the external sensor, this setup/initialization is not necessary.

8.2.4.4.1.1 ISS CCP2 Reset Behavior

On hardware or software reset of the ISS, all registers in the CCP2 receiver are reset to their reset values.

The two sources for CCP2 software reset are:

- Global reset for the whole ISS through the ISS_HL_SYSCONFIG[0] SOFTRESET bit
- Local reset, affecting only the CCP2 module. The reset is initiated by writing 0x1 in the CCP2_SYSCONFIG[1] SOFT_RESET bit. The reset done status can be check by reading the CCP2_SYSSTATUS[0] RESET_DONE bit.

8.2.4.4.2 ISS CCP2 Programming Event and Status Checking

When an event occurs, the corresponding bit in the CCP2_LC01_IRQSTATUS, CCP2_LC23_IRQSTATUS, or CCP2_LCM_IRQSTATUS register is set. Each event can be individually masked using the CCP2_LC01_IRQENABLE, CCP2_LC23_IRQENABLE, or CCP2_LCM_IRQENABLE register. Masked events are not transmitted to the interrupt line, but the CCP2_LC01_IRQSTATUS, CCP2_LC23_IRQSTATUS, or CCP2_LCM_IRQSTATUS register is updated.

Events transmitted to the ISS interrupt merger can be mapped to the Cortex-A15 MPU or Cortex-M4 IPU subsystems, or DSP, by unmasking ISS_HL_IRQENABLE_SET_i[] CCP2_IRQj (where i = 0 to 5, j = 0, 1, 2, 3, and 8). Only the ISS_HL_IRQENABLE_SET_5 output line is connected to the Cortex-A15 MPU SS interrupt controller (INTC), and only the ISS_HL_IRQENABLE_SET_4 output line is connected to the DSP INTC. The Cortex-M4 MPU SS INTC, however, is connected to all six output lines of ISS_HL_IRQENABLE_SET_i (where i = 0 to 5). To clear an event, the following actions are required:

- Clear the event at the CCP2 receiver level by writing 1 to the corresponding bit in the CCP2_LC01_IRQSTATUS, CCP2_LC23_IRQSTATUS or CCP2_LCM_IRQSTATUS register.
- Events generated by the submodules and ISS top level clear it. Each event that generates an interrupt can be individually enabled by setting the appropriate bit in the ISS_HL_IRQENABLE_SET_i register. It is disabled by setting the appropriate bit in the ISS_HL_IRQENABLE_CLR_i register. When an event occurs, the corresponding bit in the ISS_HL_IRQSTATUS_i register is set, regardless of whether or not

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the event is enabled. Bits in the ISS_HL_IRQSTATUS_i registers are set only when an enabled event occurs. Software can clear a pending HS_VS_IRQ event by setting the appropriate bit ISS_HL_IRQSTATUS[17] HS_VS_IRQ. Events generated by submodules are automatically cleared at ISS top level when they are cleared at submodule level.

8.2.4.4.3 ISS CCP2 Programming Register Accessibility During Frame Processing

There are two types of register accesses in the CCP2 receiver:

- Shadowed registers:
  - These registers/fields can be read and written (if the field is writable) at any time. However, written values take effect only at the start of a frame. Reads return the most-recent write, even though the settings are not used until the next start of frame.
  - The shadowed registers are:
    - CCP2_LCx_CTRL
    - CCP2_LCx_CODE
    - CCP2_LCx_STAT_START
    - CCP2_LCx_STAT_SIZE
    - CCP2_LCx_SOF_ADDR
    - CCP2_LCx_EOF_ADDR
    - CCP2_LCx_DAT_SIZE
    - CCP2_LCx_DAT_PING_ADDR
    - CCP2_LCx_DAT_PONG_ADDR
    - CCP2_LCx_DAT_OFST
- Busy-locked registers:
  - These registers/fields must not be written if the module is busy.
  - All register fields not listed as shadowed are busy-writable registers.

8.2.4.4.4 ISS CCP2 Programming Enable/Disable the Hardware

The CCP2 receiver is globally controlled by the CCP2_CTRL register. The bit fields in this register must not be modified when the CCP2 interface is active (except CCP2_CTRL[0] IF_EN).

Table 8-63 and Table 8-64 list the procedures to enable and disable, respectively, the interface.

Table 8-63. ISS CCP2 Interface Enable

Step	Bit Field	Value
Clear the interface. Data acquisition starts on the following FSC synchronization code.	CCP2_CTRL[0] IF_EN	0x1
Reset the output FIFO of the module; the reset is caused by the 0-to-1 edge transition.	CCP2_CTRL[0] IF_EN	0x1

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Table 8-64. ISS CCP2 Interface Disable

Step	Bit Field	Value
Disable interface. • The interface is disabled immediately if CCP2_CTRL[3] FRAME = 0x0. • If CCP2_CTRL[3] FRAME = 0x1 and CCP2_LCx_CTRL[2] CRC_EN = 0x0, the interface is disabled after the FEC synchronization code is received. • If CCP2_CTRL[3] FRAME = 0x1 and CCP2_LCx_CTRL[2] CRC_EN = 0x1, the interface is disabled only after the 16-bit CRC checksum and 16-bit pad data is received. • Before disabling the interface (IF_EN = 0), it is advised to disable all active channels by writing CCP2_LCx_CTRL[0] CHAN_EN = 0x0. Otherwise, if IF_EN = 0 is set during a vertical blanking period, the reception continues until the FEC synchronization code is received for all active channels.	CCP2_CTRL[0] IF_EN	0x0

8.2.4.4.5 ISS CCP2 Programming Select the Signaling Scheme

Table 8-65 lists the procedure to select the signaling scheme.

Table 8-65. ISS CCP2 Select the Signaling Scheme

Step	Bit Field	Value
Selects whether the data/strobe or data/clock signaling scheme is used. For the correct settings as a function of the image sensor class, see Section 8.2.3, *ISS CSI PHY*. Setting CCP2_CTRL[1] PHY_SEL = 0x1 has no effect if CCP2_CTRL[4] MODE = 0x0 (CSI1 mode). This setting must also be configured in the control module.	See Section 8.2.3, *ISS CSI PHY*. For the register and bit field, see Chapter 18, *Control Module*.	0x0: Data/clock 0x1: Data/strobe

8.2.4.4.6 ISS CCP2 Programming Select the Mode: MIPI CSI1 or CCP2

Table 8-66 lists the procedure to select MIPI CSI1 or CCP2 mode.

Table 8-66. ISS CCP2 Select MIPI CSI1 or CCP2 Mode

Step	Bit Field	Value
Selects whether the CCP2 module works in MIPI CSI1 or CCP2-compatible mode	CCP2_CTRL[4] MODE	0x0: Disables the CCP2-specific features (data/strobe, CRC, logical channels, RAW6, RAW7, and DPCM data formats) 0x1: CCP2 mode

8.2.4.4.7 ISS CCP2 Programming Burst Settings

Table 8-67 lists the procedure to configure the burst settings.

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Table 8-67. ISS CCP2 Configure Burst Settings

Step	Bit Field	Value
The module can be forced to perform single 64-bit requests or bursts of 2x, 4x, 8x, and 16 x 64 bits. The module must always use 16 x 64. The FIFO size is 64 x 64 bits.	CCP2_CTRL[6:5] BURST CSI2_CTRL[16] BURST_SIZE_EXPAND	0x0: Single request. 0x1: 2 x 64-bit bursts 0x2: 4 x 64-bit bursts 0x3: 8 x 64-bit bursts 0x4: 16 x 64-bit bursts (with burst expand)
Enable 128 bytes (recommended setting) of the DMA CSI2/CCP DMA engine to burst 128 bytes over the L3_MAIN interconnect.	CSI2_CTRL[16] BURST_SIZE_EXPAND	0x0: Use the burst size defined in the BURST_SIZE bit field. 0x1: Allow generation of 16 x 64-bit bursts.

8.2.4.4.8 ISS CCP2 Programming Debug Mode

Table 8-68 lists the procedure to enable debug mode.

Table 8-68. ISS CCP2 Enable Debug Mode

Step	Bit Field	Value
Enable debug mode.	CCP2_CTRL[13] DBG_EN	0x1

- During debug mode, the input comes from the CCP2_DBG register, not from the CCP2 physical interface. The full CCP2 receiver function can be debugged in debug mode. Full 32-bit values must always be written to the CCP2_DBG register.
- The following bit has no effect during debug mode:
  - CCP2_CTRL[0] IF_EN
- The following examples apply to the CCP2_DBG register:
  - Synchronization codes: CCP2_DBG = 0xFF000000 (LSC) or 0xFF00001 (LEC) or 0xFF00002 (FSC) or 0xFF000003 (FEC)
  - To send the RAW12 pixels 0x673, 0x452, 0x01d, 0xefc, 0xab0, 0x891, 0x326, and 0x547, write CCP2_DBG = 0x01234567 followed by CCP2_DBG = 0x89abcdef and CCP2_DBG = 0x76543210.

NOTE: Each write to the CCP2_DBG register sends a full 32-bit word through the CCP2 receiver hardware. When 8- or 16-bit writes are performed to the register, the previous 32-bit value is merged with the newly written one. When the driver writes, for example, 0x01234567 followed by 0x0000 00FF the MPU subsystem informs that only 8 bits are written), the CCP2 receiver pipeline gets 0x01234567 followed by 0x012345FF.

8.2.4.4.9 ISS CCP2 Programming Video Port

Table 8-69 lists the procedure to configure the video port.

Table 8-69. ISS CCP2 Configure Video Port

Step	Bit Field	Value
Set the video port output frequency. It varies from ISS_MAIN_FLCK down to ISS_MAIN_FLCK / 65,536 MHz.	CCP2_CTRL[31:15] FRACDIV	From 1 to 65,536
Enable video port clock during vertical blanking periods or not.	CCP2_CTRL[9] VP_CLK_FORCE_ON	0x0: The video port clock is gated during vertical blanking periods. 0x1: The video port clock is free-running during vertical blanking periods.

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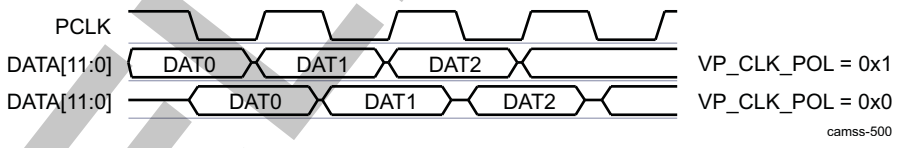
Table 8-69. ISS CCP2 Configure Video Port (continued)

Step	Bit Field	Value
Controls whether the video-port output is the only output interface enabled and applies for all channels. When CCP2_CTRL[11] VP_ONLY_EN = 0x1, the data are output only to the video port; the interface master port is not used. The two parts of the frame (embedded data and pixel data) are output to the video port (instead of pixel data to the video port and embedded data to the interconnect). • The video port outputs the embedded data defined by the CCP2_LCx_STAT_START and CCP2_LCx_STAT_SIZE registers without decompression. • The video port outputs the pixel data defined by the CCP2_LCx_DAT_START and CCP2_LCx_DAT_SIZE registers.	CCP2_CTRL[11] VP_ONLY_EN	
Control the video port pixel clock polarity: (Recommended setting: rising edge)	CCP2_CTRL[12] VP_CLK_POL	0x0: The CCP2 receiver writes the data on the video port on the pixel-clock falling edge. The module connected to the video port samples the data on the pixel clock rising edge. 0x1: The CCP2 receiver writes the data on the video port on the pixel-clock rising edge. The module connected to the video port samples the data on the pixel clock falling edge. Figure 8-32 shows the settings for CCP2_CTRL[12] VP_CLK_POL.

Figure 8-32 shows the settings for CCP2_CTRL[12] VP_CLK_POL.

Figure 8-32. CCP2_CTRL[12] VP_CLK_POL Settings



8.2.4.4.10 ISS CCP2 Programming Logical Channels

The CCP2 receiver supports simultaneous logical channels. Each logical channel is controlled independently with its own set of registers. The four sets of registers are identical, but some reset values are different.

The same description applies to all four logical channels (LCx, where x = 0 to 3).

All the registers in Section 8.2.4.4.11, *ISS CCP2 Programming Controls* through Section 8.2.4.4.18, *ISS CCP2 Programming Pixel Data Region* can be modified at any time. However, the modifications apply only from the start of the following frame.

8.2.4.4.11 ISS CCP2 Programming Controls

Table 8-70 lists the procedure to enable the logical channels.

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Table 8-70. ISS CCP2 Enable Logical Channels

Step	Bit Field	Value
Enable logical channels. It has no effect if CCP2_CTRL[4] MODE = 0x0. By default, all logical channels except logical channel 0 are disabled. Only the pixel data of one logical channel can go to the video preprocessing hardware; the SOF and EOF lines are always sent to memory through the interconnect interface.	CCP2_LCx_CTRL[0] CHAN_EN	0x1

8.2.4.4.12 ISS CCP2 Programming Region-of-Interest

Table 8-71 lists the procedure to enable the region-of-interest.

Table 8-71. ISS CCP2 Enable Region-of-Interest

Step	Bit Field	Value
Enables the region-of-interest feature (SOF lines, pixel data, and EOF lines): • If enabled, register settings set the position and size of each region; all data not in a region of interest are ignored. • If disabled, all data in the frame are output. CCP2_LCx_CTRL[1] REGION_EN is set to 0x0 for a JPEG bitstream.	CCP2_LCx_CTRL[1] REGION_EN	0x1

8.2.4.4.13 ISS CCP2 Programming CRC

Table 8-72 lists the procedure to enable the CRC.

Table 8-72. ISS CCP2 Enable the CRC

Step	Bit Field	Value
Enable the CRC. If the received checksum and the computed checksum do not match, an interrupt is triggered: the corresponding event is LCx_CRC_IRQ. Setting CCP2_LCx_CTRL[2] CRC_EN = 0x1 has no effect, if CCP2_CTRL[4] MODE = 0x0.	CCP2_LCx_CTRL[2] CRC_EN	0x1

8.2.4.4.14 ISS CCP2 Programming Destination Format

Control the destination format:

- The CCP2 receiver reformats received data to store it in memory or to send it to the video preprocessing.
- The CCP2_LCx_CTRL[7:3] FORMAT bit field controls the destination-data format:
  - EXP8 = Data expansion to 8 bits, padding with zeros
  - EXP16 = Data expansion to 16 bits, padding with alpha or zeros. The CCP2_CTRL[15:8] ALPHA bit field can be used to set an alpha value. For RGB444 + EXP16:
    - data_out [31:28] = ALPHA [3:0]
    - data_out [15:12] = ALPHA [3:0]
  - EXP32 = Data expansion to 32 bits, padding with alpha. The CCP2_CTRL[15:8] ALPHA bit field can be used to set an alpha value. For RGB888 + EXP32: data_out [31:24] = ALPHA [7:0]
  - FSP = False synchronization protection code decoding. Applies only to JPEG8 data format.
  - VP = Output to video preprocessing is enabled.

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8.2.4.4.15 ISS CCP2 Programming Frame Acquisition

Table 8-73 lists the procedure to acquire frames.

Table 8-73. ISS CCP2 Frame Acquisition

Step	Bit Field	Value
Program the number of frames that the CCP2 receiver acquires. The value of COUNT is decremented after each frame received.	CCP2_LCx_CTRL[31:24] COUNT	0: The counter is free-running (default value). 1255: Remaining frames to be acquired
Writes to the COUNT bit field are controlled by the COUNT_UNLOCK bit.	CCP2_LCx_CTRL[16] COUNT_UNLOCK	
Configures PING and PONG addresses	CCP2_LCx_DAT_PING_ADDR and CCP2_LCx_DAT_PONG_ADDR	
Indicates whether the PING address or PONG address was used to store the pixel data of the last frame. After reset or after a 0-to-1 edge transition in CCP2_CTRL[0] IF_EN, the pixel data are written in the PING buffer and CCP2_LCx_CTRL[17] PING_PONG = 0x1 (PONG). After the first FEC synchronization code is received, the pixel data are written in the PONG buffer and CCP2_LCx_CTRL[17] PING_PONG = 0x0 (PING). CCP2_LCx_CTRL[17] PING_PONG toggles after every FEC synchronization code.	CCP2_LCx_CTRL[17] PING_PONG	

After the correct number of frames is received, acquisition is automatically disabled (CCP2_LCx_CTRL[0] CHAN_EN = 0x0) and the COUNT_IRQ interrupt is triggered. The programmer can re-enable the acquisition by resetting the CCP2_LCx_CTRL[0] CHAN_EN bit to 0x1.

8.2.4.4.16 ISS CCP2 Programming Synchronization Codes

The FSC, FEC, LSC, and LEC synchronization codes have default values given by the *SMIA CCP2 Specification v1.0*. Also, each logical channel is identified by a default identifier.

The CCP2_LCx_CODE register enables overwriting of the default values: CCP2_LCx_CODE[11:8] FSC, CCP2_LCx_CODE[15:12] FEC, CCP2_LCx_CODE[3:0] LSC, and CCP2_LCx_CODE[7:4] LEC overwrite the 4 LSBs of the 32-bit synchronization codes. The default values must not be modified.

8.2.4.4.17 ISS CCP2 Programming Status Data

The SOF and EOF status lines can be output to memory.

The SOF and EOF status lines always cover full lines. No register settings enable the setting of width.

The CCP2_LCx_STAT_START register enables the setting of the vertical start position of the SOF and EOF status lines. Because the SOF status line comes first in the CCP2 frame, CCP2_LCx_STAT_START[11:0] SOF = 0x0.

The CCP2_LCx_STAT_SIZE register enables the setting of the numbers of SOF and EOF status lines. If CCP2_LCx_STAT_SIZE[11:0] SOF = 0x0 and CCP2_LCx_STAT_SIZE[27:16] EOF = 0x0, no status data are output.

Figure 8-33 shows the SOF and EOF region settings. The SOF and EOF status lines and the pixel data must not overlap, but can be consecutive.

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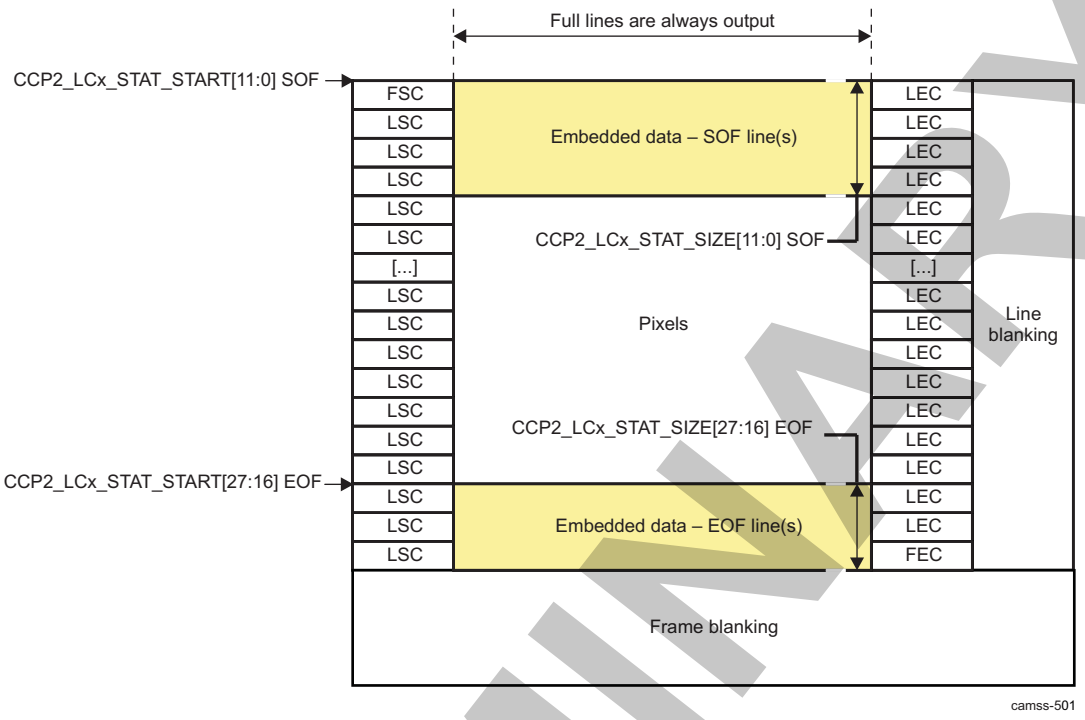
Figure 8-33. ISS CCP2 SOF and EOF Region Settings



The 32-bit destination addresses of the SOF status lines are set by the CCP2_LCx_SOF_ADDR register.

NOTE: The destination addresses of the SOF status lines must be aligned on a 32-byte boundary; the 5 LSBs of the address are ignored. The SOF lines are packed together at the destination address.

The 32-bit destination addresses of the EOF status lines are set by the CCP2_LCx_EOF_ADDR register.

NOTE: The destination addresses of the EOF status lines must be aligned on a 32-byte boundary; the 5 LSBs of the address are ignored. The EOF lines are packed together at the destination address.

NOTE: The CCP2 receiver does not modify the data in the SOF and EOF status lines. The data are received and written with no modifications.

8.2.4.4.18 ISS CCP2 Programming Pixel Data Region

Pixel data can be output to memory or to the video-preprocessing hardware.

The pixel data region covers full lines. The CCP2_LCx_DAT_SIZE register sets the horizontal size of the pixel region. The vertical size is expressed in lines.

The CCP2_LCx_DAT_START register enables the setting of the vertical start position of the pixel data. The vertical start position is expressed in lines.

Figure 8-34 shows the pixel region settings.

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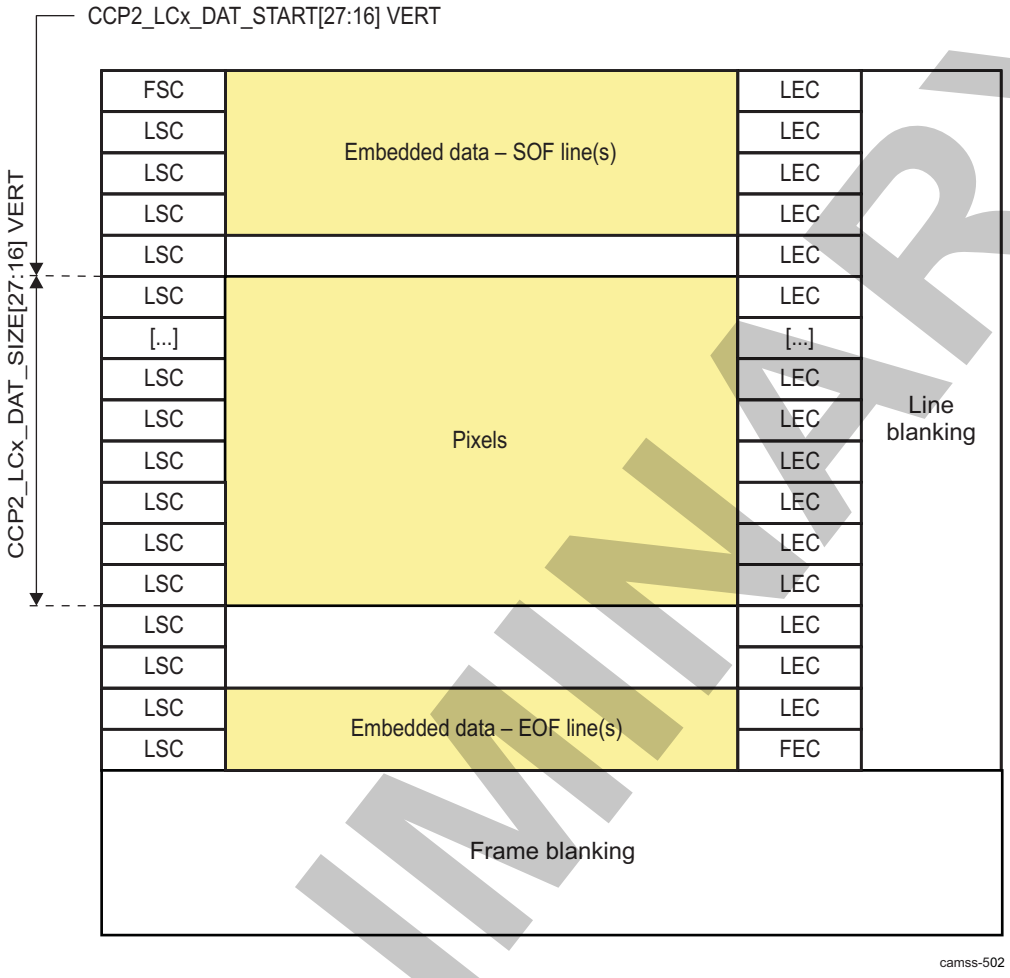
Figure 8-34. ISS CCP2 Pixel Data Region Settings



The 32-bit destination addresses of the pixel data are set by the CCP2_LCx_DAT_PING_ADDR and CCP2_LCx_DAT_PONG_ADDR registers.

NOTE: The destination address must be aligned on a 32-byte boundary; the 5 LSBs of the address are ignored. The pixel data lines are packed together at the destination address.

It is possible to perform double-buffering (ping-ponging) at the destination by setting different addresses in the CCP2_LCx_DAT_PING_ADDR and CCP2_LCx_DAT_PONG_ADDR registers. It is possible to disable double-buffering by setting up the same address in both registers. The CCP2_LCx_CTRL[17] PING_PONG bit must be used by software to determine which address contains the latest frame.

A destination pitch controls the address jump between the address of the first pixel of the previous line and the address of the first pixel of the current line. The destination pitch is set in bytes with the CCP2_LCx_DAT_OFST register. It applies for CCP2_LCx_DAT_PING_ADDR and CCP2_LCx_DAT_PONG_ADDR.

NOTE: The destination pitch must be a multiple of 32 bytes; the 5 LSBs of the address are ignored.

The destination data format is set with the CCP2_LCx_CTRL[7:2] FORMAT bit field.

For the PING frame:

- @Line0 = CCP2_LCx_DAT_PING_ADDR
- @Line1 = @Line0 + CCP2_LCx_DAT_OFST

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- @Line2 = @Line1 + CCP2_LCx_DAT_OFST

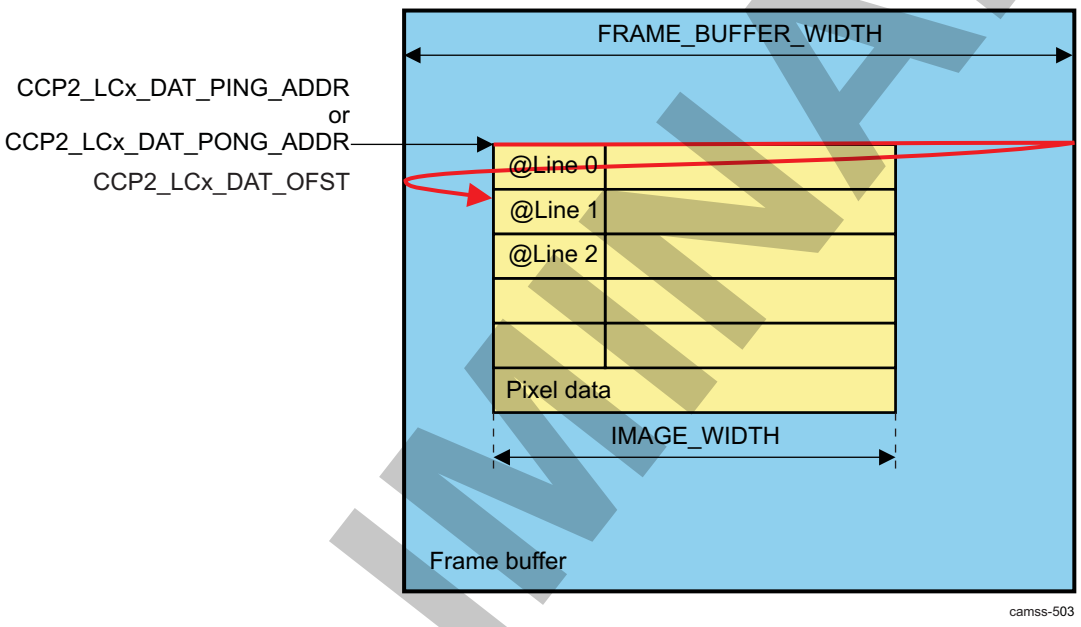
For the PONG frame:

- @Line0 = CCP2_LCx_DAT_PONG_ADDR
- @Line1 = @Line0 + CCP2_LCx_DAT_OFST
- @Line2 = @Line1 + CCP2_LCx_DAT_OFST

When CCP2_LCx_DAT_OFST = 0x0, the lines are written contiguously in memory. The destination pitch enables 2D transfers; it is required to write the pixel data directly in the frame buffer, for instance.

In such cases, CCP2_LCx_DAT_OFST = FRAME_BUFFER_WIDTH. Figure 8-35 shows the pixel data destination settings.

Figure 8-35. ISS CCP2 Pixel Data Destination Settings



8.2.4.4.19 ISS CCP2 Programming Memory Read Channel

8.2.4.4.19.1 ISS CCP2 Write Data From Sensor to Memory

Data can be captured from the sensor using any logical channel. To keep the native data format, the channel format must be set to YUV4:2:2 little-endian format.

8.2.4.4.19.2 ISS CCP2 Read Data From Memory

Table 8-74 lists the procedure to configure read data from memory.

Table 8-74. ISS CCP2 Configure Read Data From Memory

Step	Bit Field	Value
Disable all logical channels.	CCP2_CTRL[0] IF_EN	0x0
Wait until disabling of the physical interface is effective before enabling the memory read channel.	CCP2_CTRL[3] FRAME	0x1
Configure the burst siz .The recommended value for best performance is 0x4 (16 × 64-bit burst).	CCP2_LCM_CTRL[7:5] BURST_SIZE	–

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Table 8-74. ISS CCP2 Configure Read Data From Memory (continued)

Step	Bit Field	Value
Configure the source data format, location, and framing. In addition to the CCP2_LCM_HSIZE[11:0] SKIP and CCP2_LCM_HSIZE[27:16] COUNT bit fields, firmware must specify the amount of data to be fetched from memory. This value is set in 64-bit word steps and must be a multiple of 32 bytes (four words of 64 bits). The value is computed with the following formula: HWORDS = 4 × ceil(((SKIP + COUNT) x bits_per_pixel)/(8 × 32)) (3) The CCP2_LCM_SRC_ADDR and CCP2_LCM_SRC_OFST registers must be aligned on 32-byte boundaries for correct operation. For best performance, both registers must be aligned on 256-byte boundaries. See the example following this table.	CCP2_LCM_CTRL, CCP2_LCM_HSIZE, CCP2_LCM_VSIZE, CCP2_LCM_PREFETCH, CCP2_LCM_SRC_ADDR, CCP2_LCM_SRC_OFST	
Select destination.	CCP2_LCM_CTRL[2] DST_PORT	0x0: Video port 0x1: Memory
If destination = video port, configure clock frequency and its gating during frame blanking periods.	CCP2_CTRL[31:15] FRACDIV, CCP2_CTRL[9] VP_CLK_FORCE_ON	
If needed, configure READ_THROTTLE to reduce the bandwidth in memory-to-memory operation to prevent system overload. It has no effect when data are sent to the video port (controlled by video port clock in this case).	CCP2_LCM_CTRL[4:3] READ_THROTTLE	
If the memory write port is used, the destination format and address must be configured.	CCP2_LCM_DST_ADDR, CCP2_LCM_DST_OFST	
Enable memory read channel. After processing a full frame, this bit is automatically cleared by hardware and an EOF event is triggered.	CCP2_LCM_CTRL[0] CHAN_EN	0x1

Example:

- CCP2_LCM_CTRL[7:5] BURST_SIZE is set to 16 × 64 bits
- CCP2_LCM_HSIZE[11:0] SKIP = 0
- CCP2_LCM_HSIZE[27:16] COUNT = 1000
- CCP2_LCM_CTRL[23] SRC_PACK = YES
- CCP2_LCM_CTRL[18:16] SRC_FORMAT = RAW6
- CCP2_LCM_PREFETCH[13:3] HWORDS = 96 (>=94)

  Setting the size to 94 produces the following burst sequence: 16, 16, 16, 16, 16, 8, and 4 (7 interconnect requests). However, when it is set to 96, the burst sequence is 6 × 16 (6 interconnect requests).

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Table 8-75 summarizes the expected settings for all possible modes of the LCM feature, when data is sent to the video port (bit CCP2_LCM_CTRL[2] DST_PORT = 0x0).

Table 8-76 summarizes the expected settings for all possible modes of the LCM feature, when data is sent to memory through the interface port (bit CCP2_LCM_CTRL[2] DST_PORT = 0x1).

Table 8-75. LCM Settings for Video Port Destination

Input	Output	Settings for CCP2_LCM_CTRL register bits								
		[19:16]SRC_FORMAT	[21:20]SRC_DECOMPR	[22]SRC_DPCM_PRED	[23]SRC_PACK	[26:24]DST_FORMAT	[29:28]DST_COMPR	[30]DST_DPCM_PRED	[31]DST_PACK	[2]DST_PORT
RAW6	RAW6	RAW6	DISABLE	NA	NO	RAW6	NA	NA	NA	VPORT
RAW6 + PACK	RAW6	RAW6	DISABLE	NA	YES	RAW6	NA	NA	NA	VPORT
RAW6 + DPCM	RAW10	RAW6	DPCM	SIMPLE	NO	RAW10	NA	NA	NA	VPORT
RAW6 + PACK + DPCM	RAW10	RAW6	DPCM	SIMPLE	YES	RAW10	NA	NA	NA	VPORT
RAW6 + DPCM_ADV	RAW10	RAW6	DPCM	ADVANCED	NO	RAW10	NA	NA	NA	VPORT
RAW6 + PACK + DPCM_ADV	RAW10	RAW6	DPCM	ADVANCED	YES	RAW10	NA	NA	NA	VPORT
RAW7	RAW7	RAW7	DISABLE	NA	NO	RAW7	NA	NA	NA	VPORT
RAW7 + PACK	RAW7	RAW7	DISABLE	NA	YES	RAW7	NA	NA	NA	VPORT
RAW7 + DPCM	RAW10	RAW7	DPCM	SIMPLE	NO	RAW10	NA	NA	NA	VPORT
RAW7 + PACK + DPCM	RAW10	RAW7	DPCM	SIMPLE	YES	RAW10	NA	NA	NA	VPORT
RAW7 + DPCM_ADV	RAW10	RAW7	DPCM	ADVANCED	NO	RAW10	NA	NA	NA	VPORT
RAW7 + PACK + DPCM_ADV	RAW10	RAW7	DPCM	ADVANCED	YES	RAW10	NA	NA	NA	VPORT
RAW8	RAW8	RAW8	DISABLE	NA	NO	RAW8	NA	NA	NA	VPORT
RAW8 + DPCM	RAW10	RAW8	DPCM	SIMPLE	NO	RAW10	NA	NA	NA	VPORT
RAW8 + ALAW10	RAW10	RAW8	ALAW	ALAW	NO	RAW10	NA	NA	NA	VPORT
RAW8 + DPCM12	RAW12	RAW8	DPCM12	SIMPLE	NO	RAW12	NA	NA	NA	VPORT
RAW10	RAW10	RAW10	DISABLE	NA	NO	RAW10	NA	NA	NA	VPORT
RAW10 + PACK	RAW10	RAW10	DISABLE	NA	YES	RAW10	NA	NA	NA	VPORT
RAW12	RAW12	RAW12	DISABLE	NA	NO	RAW12	NA	NA	NA	VPORT
RAW12 + PACK	RAW12	RAW12	DISABLE	NA	NO	RAW12	NA	NA	NA	VPORT
RAW14	RAW14	RAW14	DISABLE	NA	NO	RAW14	NA	NA	NA	VPORT
RAW16	RAW16	RAW16	DISABLE	NA	NO	RAW16	NA	NA	NA	VPORT

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Table 8-76. LCM Settings for Memory Destination

Input	Output	Settings for CCP2_LCM_CTRL register bits								
		[19:16]SRC_FORMAT	[21:20]SRC_DECOMPR	[22]SRC_DPCM_PRED	[23]SRC_PACK	[26:24]DST_FORMAT	[29:28]DST_COMPR	[30]DST_DPCM_PRED	[31]DST_PACK	[2]DST_PORT
RAW6	RAW10	RAW6	DISABLE	NA	NO	RAW10	DISABLE	NA	NO	OCP
RAW6	RAW10 + PACK	RAW6	DISABLE	NA	NO	RAW10	DISABLE	NA	YES	OCP
RAW6 + PACK	RAW10	RAW6	DISABLE	NA	YES	RAW10	DISABLE	NA	NO	OCP
RAW6 + PACK	RAW10 + PACK	RAW6	DISABLE	NA	YES	RAW10	DISABLE	NA	YES	OCP
RAW6 + DPCM	RAW10	RAW6	DPCM	SIMPLE	NO	RAW10	DISABLE	NA	NO	OCP
RAW6 + DPCM	RAW10 + PACK	RAW6	DPCM	SIMPLE	NO	RAW10	DISABLE	NA	YES	OCP
RAW6 + PACK + DPCM	RAW10	RAW6	DPCM	SIMPLE	YES	RAW10	DISABLE	NA	NO	OCP
RAW6 + PACK + DPCM	RAW10 + PACK	RAW6	DPCM	SIMPLE	YES	RAW10	DISABLE	NA	YES	OCP
RAW6 + DPCM_ADV	RAW10	RAW6	DPCM	ADVANCED	NO	RAW10	DISABLE	NA	NO	OCP
RAW6 + DPCM_ADV	RAW10 + PACK	RAW6	DPCM	ADVANCED	NO	RAW10	DISABLE	NA	YES	OCP
RAW6 + PACK + DPCM_ADV	RAW10	RAW6	DPCM	ADVANCED	YES	RAW10	DISABLE	NA	NO	OCP
RAW6 + PACK + DPCM_ADV	RAW10 + PACK	RAW6	DPCM	ADVANCED	YES	RAW10	DISABLE	NA	YES	OCP
RAW7	RAW10	RAW7	DISABLE	NA	NO	RAW10	DISABLE	NA	NO	OCP
RAW7	RAW10 + PACK	RAW7	DISABLE	NA	NO	RAW10	DISABLE	NA	YES	OCP
RAW7 + PACK	RAW10	RAW7	DISABLE	NA	YES	RAW10	DISABLE	NA	NO	OCP
RAW7 + PACK	RAW10 + PACK	RAW7	DISABLE	NA	YES	RAW10	DISABLE	NA	YES	OCP
RAW7 + DPCM	RAW10	RAW7	DPCM	SIMPLE	NO	RAW10	DISABLE	NA	NO	OCP
RAW7 + DPCM	RAW10 + PACK	RAW7	DPCM	SIMPLE	NO	RAW10	DISABLE	NA	YES	OCP
RAW7 + PACK + DPCM	RAW10	RAW7	DPCM	SIMPLE	YES	RAW10	DISABLE	NA	NO	OCP
RAW7 + PACK + DPCM	RAW10 + PACK	RAW7	DPCM	SIMPLE	YES	RAW10	DISABLE	NA	YES	OCP
RAW7 + DPCM_ADV	RAW10	RAW7	DPCM	ADVANCED	NO	RAW10	DISABLE	NA	NO	OCP
RAW7 + DPCM_ADV	RAW10 + PACK	RAW7	DPCM	ADVANCED	NO	RAW10	DISABLE	NA	YES	OCP

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Table 8-76. LCM Settings for Memory Destination (continued)

Input	Output	Settings for CCP2_LCM_CTRL register bits								
RAW7 + PACK + DPCM_ADV	RAW10	RAW7	DPCM	ADVANCED	YES	RAW10	DISABLE	NA	NO	OCP
RAW7 + PACK + DPCM_ADV	RAW10 + PACK	RAW7	DPCM	ADVANCED	YES	RAW10	DISABLE	NA	YES	OCP
RAW8	RAW10	RAW8	DISABLE	NA	NO	RAW10	DISABLE	NA	NO	OCP
RAW8	RAW10 + PACK	RAW8	DISABLE	NA	NO	RAW10	DISABLE	NA	YES	OCP
RAW8 + DPCM	RAW10	RAW8	DPCM	SIMPLE	NO	RAW10	DISABLE	NA	NO	OCP
RAW8 + DPCM	RAW10 + PACK	RAW8	DPCM	SIMPLE	NO	RAW10	DISABLE	NA	YES	OCP
RAW8 + DPCM12	RAW12	RAW8	DPCM12	SIMPLE	NO	RAW12	DISABLE	NA	NO	OCP
RAW8 + DPCM12	RAW12 + PACK	RAW8	DPCM12	SIMPLE	NO	RAW12	DISABLE	NA	YES	OCP
RAW8 + ALAW10	RAW10	RAW8	ALAW	NA	NO	RAW10	DISABLE	NA	NO	OCP
RAW8 + ALAW10	RAW10 + PACK	RAW8	ALAW	NA	NO	RAW10	DISABLE	NA	YES	OCP
RAW10	RAW6 + DPCM	RAW10	DISABLE	NA	NO	RAW6	DPCM	SIMPLE	NO	OCP
RAW10	RAW6 + DPCM + PACK	RAW10	DISABLE	NA	NO	RAW6	DPCM	SIMPLE	YES	OCP
RAW10	RAW6 + DPCM_ADV	RAW10	DISABLE	NA	NO	RAW6	DPCM	ADVANCED	NO	OCP
RAW10	RAW6 + DPCM_ADV + PACK	RAW10	DISABLE	NA	NO	RAW6	DPCM	ADVANCED	YES	OCP
RAW10	RAW7 + DPCM	RAW10	DISABLE	NA	NO	RAW7	DPCM	SIMPLE	NO	OCP
RAW10	RAW7 + DPCM + PACK	RAW10	DISABLE	NA	NO	RAW7	DPCM	SIMPLE	YES	OCP
RAW10	RAW7 + DPCM_ADV	RAW10	DISABLE	NA	NO	RAW7	DPCM	ADVANCED	NO	OCP
RAW10	RAW7 + DPCM_ADV + PACK	RAW10	DISABLE	NA	NO	RAW7	DPCM	ADVANCED	YES	OCP
RAW10	RAW8 + DPCM	RAW10	DISABLE	NA	NO	RAW8	DPCM	SIMPLE	NA	OCP

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Table 8-76. LCM Settings for Memory Destination (continued)

Input	Output	Settings for CCP2_LCM_CTRL register bits								
RAW10 + PACK	RAW6 + DPCM	RAW10	DISABLE	NA	YES	RAW6	DPCM	SIMPLE	NO	OCP
RAW10 + PACK	RAW6 + DPCM + PACK	RAW10	DISABLE	NA	YES	RAW6	DPCM	SIMPLE	YES	OCP
RAW10 + PACK	RAW6 + DPCM_ ADV	RAW10	DISABLE	NA	YES	RAW6	DPCM	ADVANCED	NO	OCP
RAW10 + PACK	RAW6 + DPCM_ ADV + PACK	RAW10	DISABLE	NA	YES	RAW6	DPCM	ADVANCED	YES	OCP
RAW10 + PACK	RAW7 + DPCM	RAW10	DISABLE	NA	YES	RAW7	DPCM	SIMPLE	NO	OCP
RAW10 + PACK	RAW7 + DPCM + PACK	RAW10	DISABLE	NA	YES	RAW7	DPCM	SIMPLE	YES	OCP
RAW10 + PACK	RAW7 + DPCM_ ADV	RAW10	DISABLE	NA	YES	RAW7	DPCM	ADVANCED	NO	OCP
RAW10 + PACK	RAW7 + DPCM_ ADV + PACK	RAW10	DISABLE	NA	YES	RAW7	DPCM	ADVANCED	YES	OCP
RAW10 + PACK	RAW8 + DPCM	RAW10	DISABLE	NA	YES	RAW8	DPCM	SIMPLE	NA	OCP

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The following constraints on the register settings apply, when the writing of DPCM history information into system memory is enabled (see Section 8.2.4.3.5.6, *ISS CCP2 DPCM Decompression History*, for more details):

- CCP2_LCM_CTRL[26:24] DST_FORMAT = RAW10 or RAW12
- CCP2_LCM_CTRL[29:28] DST_COMPR = 0
- CCP2_LCM_CTRL[30] DST_DPCM_PRED = 0
- CCP2_LCM_CTRL[31] DST_PACK = 0
- CCP2_LCM_CTRL[23] SRC_PACK = 0 or 1
- CCP2_LCM_CTRL[22] SRC_DPCM_PRED = 0 or 1
- CCP2_LCM_CTRL[21:20] SRC_DECOMPR = 0x2 or 0x3
- CCP2_LCM_CTRL[19:16] SRC_FORMAT = RAW6, RAW7 or RAW8
- CCP2_LCM_CTRL[2] DST_PORT = 0 or 1
- CCP2_LCM_DST_OFST = OFST, when destination is OCP (CCP2_LCM_CTRL[2] DST_PORT = 1)
- CCP2_LCM_DST_ADDR = SDRAM address of:
  - Pixels, when CCP2_LCM_CTRL[2] DST_PORT = 1
  - History data, when CCP2_LCM_CTRL[2] DST_PORT = 0
- CCP2_LCM_HIST_ADDR = SDRAM address of history data when CCP2_LCM_CTRL[2] DST_PORT = 1

8.2.4.5 ISS CCP2 Register Manual

8.2.4.5.1 ISS CCP2 Instance Summary

Table 8-77 summarizes the CCP2 instance.

Table 8-77. ISS CCP2 Instance Summary

Module Name	L3_MAIN Base Address	Size
ISS_CCP2	0x5200 1C00	512 bytes

8.2.4.5.2 ISS CCP2 Registers

8.2.4.5.2.1 ISS CCP2 Register Summary

Table 8-78 lists the CCP2 registers.

Table 8-78. ISS CCP2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CCP2 L3_MAIN Physical Address
CCP2_REVISION	R	32	0x0000 0000	0x5200 1C00
CCP2_SYSCONFIG	RW	32	0x0000 0004	0x5200 1C04
CCP2_SYSSTATUS	R	32	0x0000 0008	0x5200 1C08
CCP2_LC01_IRQENABLE	RW	32	0x0000 000C	0x5200 1C0C
CCP2_LC01_IRQSTATUS	RW	32	0x0000 0010	0x5200 1C10
CCP2_LC23_IRQENABLE	RW	32	0x0000 0014	0x5200 1C14
CCP2_LC23_IRQSTATUS	RW	32	0x0000 0018	0x5200 1C18
CCP2_LCM_IRQENABLE	RW	32	0x0000 002C	0x5200 1C2C
CCP2_LCM_IRQSTATUS	RW	32	0x0000 0030	0x5200 1C30

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Table 8-78. ISS CCP2 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CCP2 L3_MAIN Physical Address
CCP2_CTRL	RW	32	0x0000 0040	0x5200 1C40
CCP2_DBG	W	32	0x0000 0044	0x5200 1C44
CCP2_GNQ	R	32	0x0000 0048	0x5200 1C48
CCP2_CTRL1	RW	32	0x0000 004C	0x5200 1C4C
CCP2_LCx_CTRL (1)	RW	32	0x0000 0050 + (x * 0x30)	0x5200 1C50 + (x * 0x30)
CCP2_LCx_CODE (1)	RW	32	0x0000 0054 + (x * 0x30)	0x5200 1C54 + (x * 0x30)
CCP2_LCx_STAT_START (1)	RW	32	0x0000 0058 + (x * 0x30)	0x5200 1C58 + (x * 0x30)
CCP2_LCx_STAT_SIZE (1)	RW	32	0x0000 005C + (x * 0x30)	0x5200 1C5C + (x * 0x30)
CCP2_LCx_SOF_ADDR (1)	RW	32	0x0000 0060 + (x * 0x30)	0x5200 1C60 + (x * 0x30)
CCP2_LCx_EOF_ADDR (1)	RW	32	0x0000 0064 + (x * 0x30)	0x5200 1C64 + (x * 0x30)
CCP2_LCx_DAT_START (2)	RW	32	0x0000 0068 + (x * 0x30)	0x5200 1C68 + (x * 0x30)
CCP2_LCx_DAT_SIZE (2)	RW	32	0x0000 006C + (x * 0x30)	0x5200 1C6C + (x * 0x30)
CCP2_LCx_DAT_PING_ADDR (2)	RW	32	0x0000 0070 + (x * 0x30)	0x5200 1C70 + (x * 0x30)
CCP2_LCx_DAT_PONG_ADDR (2)	RW	32	0x0000 0074 + (x * 0x30)	0x5200 1C74 + (x * 0x30)
CCP2_LCx_DAT_OFST (2)	RW	32	0x0000 0078 + (x * 0x30)	0x5200 1C78 + (x * 0x30)
CCP2_LCM_CTRL	RW	32	0x0000 01D0	0x5200 1DD0
CCP2_LCM_VSIZE	RW	32	0x0000 01D4	0x5200 1DD4
CCP2_LCM_HSIZE	RW	32	0x0000 01D8	0x5200 1DD8
CCP2_LCM_PREFETCH	RW	32	0x0000 01DC	0x5200 1DDC
CCP2_LCM_SRC_ADDR	RW	32	0x0000 01E0	0x5200 1DE0
CCP2_LCM_SRC_OFST	RW	32	0x0000 01E4	0x5200 1DE4
CCP2_LCM_DST_ADDR	RW	32	0x0000 01E8	0x5200 1DE8
CCP2_LCM_DST_OFST	RW	32	0x0000 01EC	0x5200 1DEC
CCP2_LCM_HISTORY	RW	32	0x0000 01F0	0x5200 1DF0
CCP2_LCM_HIST_ADDR	RW	32	0x0000 01F4	0x5200 1DF4

(1) x = 0 to 3
(2) x = 0 to 3

8.2.4.5.2.2 ISS CCP2 Register Description

through describe the CCP2 registers.

Table 8-79. CCP2_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 1C00	**Instance**	ISS_CCP2
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1)

(1) TI internal data

Table 8-80. Register Call Summary for Register CCP2_REVISION

ISS Interfaces
- ISS CCP2 Registers: [0]

Table 8-81. CCP2_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x5200 1C04	**Instance**	ISS_CCP2
Description	SYSTEM CONFIGURATION REGISTER This register is the OCP-socket system configuration register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MSTANDBY_MODE		RESERVED										SOFT_RESET	AUTO_IDLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:12	MSTANDBY_MODE	Sets the behavior of the master port power management signals. 0x0: Force-standby. MStandby is only asserted when the module is disabled. 0x1: No-standby. MStandby is never asserted. 0x2: Smart-standby: MStandby is asserted based on the activity of the module. The module will try to go to standby during the vertical blanking period.	RW	0x0
11:2	RESERVED		R	0x000
1	SOFT_RESET	Software reset. Set the bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads return 0. 0x0: Normal mode. 0x1: The module is reset	RW	0
0	AUTO_IDLE	Internal OCP clock gating strategy. 0x0: OCP clock is free-running. 0x1: Automatic OCP clock gating strategy is applied based on the OCP interface activity.	RW	1

Table 8-82. Register Call Summary for Register CCP2_SYSCONFIG

ISS Interfaces
- ISS CCP2 Programming Hardware Setup/Initialization: [0]
- ISS CCP2 Registers: [1]

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Table 8-83. CCP2_SYSSTATUS

Address Offset	0x0000 0008		
Physical Address	0x5200 1C08	**Instance**	ISS_CCP2
Description	SYSTEM STATUS REGISTER This register provides status information about the module, excluding the interrupt status register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESET_DONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility. Reads returns 0.	R	0x0000 0000
0	RESET_DONE	Internal reset monitoring Read 0x1: Reset completed. Read 0x0: Internal module reset is on going.	R	1

Table 8-84. Register Call Summary for Register CCP2_SYSSTATUS

ISS Interfaces

- ISS CCP2 Programming Hardware Setup/Initialization: [0]
- ISS CCP2 Registers: [1]

Table 8-85. CCP2_LC01_IRQENABLE

Address Offset	0x0000 000C		
Physical Address	0x5200 1C0C	**Instance**	ISS_CCP2
Description	INTERRUPT ENABLE REGISTER - LOG CHAN 0 & 1 This register regroups all the events related to logical channel 0 and logical channel 1. The events related to logical channel 0 trigger SINTERRUPTN[0]. The events related to logical channel 1 trigger SINTERRUPTN[1]. The channel must be enabled for events to be generated on that channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LC1_OCPERROR_IRQ	RESERVED			LC1_FS_IRQ	LC1_LE_IRQ	LC1_LS_IRQ	LC1_FE_IRQ	LC1_COUNT_IRQ	RESERVED	LC1_FIFO_OVF_IRQ	LC1_CRC_IRQ	LC1_FSP_IRQ	LC1_FW_IRQ	LC1_FSC_IRQ	RESERVED	LC0_OCPERROR_IRQ	RESERVED			LC0_FS_IRQ	LC0_LE_IRQ	LC0_LS_IRQ	LC0_FE_IRQ	LC0_COUNT_IRQ	RESERVED	LC0_FIFO_OVF_IRQ	LC0_CRC_IRQ	LC0_FSP_IRQ	LC0_FW_IRQ	LC0_FSC_IRQ	RESERVED

Bits	Field Name	Description	Type	Reset
31	LC1_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
30:28	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
27	LC1_FS_IRQ	Logical channel 1 - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
26	LC1_LE_IRQ	Logical channel 1 - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
25	LC1_LS_IRQ	Logical channel 1 - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
24	LC1_FE_IRQ	Logical channel 1 - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
23	LC1_COUNT_IRQ	Logical channel 1 - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
22	RESERVED		R	0
21	LC1_FIFO_OVF_IRQ	Logical channel 1 - FIFO overflow error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
20	LC1_CRC_IRQ	Logical channel 1 - CRC error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
19	LC1_FSP_IRQ	Logical channel 1 - FSP error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
18	LC1_FW_IRQ	Logical channel 1 - Frame width error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
17	LC1_FSC_IRQ	Logical channel 1 - False sync code error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
16	RESERVED	Reserved	RW	0
15	LC0_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
14:12	RESERVED		R	0x0
11	LC0_FS_IRQ	Logical channel 0 - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	LC0_LE_IRQ	Logical channel 0 - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
9	LC0_LS_IRQ	Logical channel 0 - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	LC0_FE_IRQ	Logical channel 0 - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
7	LC0_COUNT_IRQ	Logical channel 0 - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	RESERVED		R	0
5	LC0_FIFO_OVF_IRQ	Logical channel 0 - FIFO overflow error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	LC0_CRC_IRQ	Logical channel 0 - CRC error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	LC0_FSP_IRQ	Logical channel 0 - FSP error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	LC0_FW_IRQ	Logical channel 0 - Frame width error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	LC0_FSC_IRQ	Logical channel 0 - False sync code error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	RESERVED	Reserved	RW	0

Table 8-86. Register Call Summary for Register CCP2_LC01_IRQENABLE

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0]
- ISS CCP2 Registers: [1]

Table 8-87. CCP2_LC01_IRQSTATUS

Address Offset	0x0000 0010		
Physical Address	0x5200 1C10	**Instance**	ISS_CCP2
Description	INTERRUPT STATUS REGISTER - LOG CHAN 0 & 1 This register regroups all the events related to logical channel 0 and logical channel 1. The events related to logical channel 0 trigger SINTERRUPTN[0]. The events related to logical channel 1 trigger SINTERRUPTN[1]. The channel must be enabled for events to be generated on that channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LC1_OCPERROR_IRQ	RESERVED			LC1_FS_IRQ	LC1_LE_IRQ	LC1_LS_IRQ	LC1_FE_IRQ	LC1_COUNT_IRQ	RESERVED	LC1_FIFO_OVF_IRQ	LC1_CRC_IRQ	LC1_FSP_IRQ	LC1_FW_IRQ	LC1_FSC_IRQ	RESERVED	LC0_OCPERROR_IRQ	RESERVED			LC0_FS_IRQ	LC0_LE_IRQ	LC0_LS_IRQ	LC0_FE_IRQ	LC0_COUNT_IRQ	RESERVED	LC0_FIFO_OVF_IRQ	LC0_CRC_IRQ	LC0_FSP_IRQ	LC0_FW_IRQ	LC0_FSC_IRQ	RESERVED

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Bits	Field Name	Description	Type	Reset
31	LC1_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
30:28	RESERVED		R	0x0
27	LC1_FS_IRQ	Logical channel 1 - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
26	LC1_LE_IRQ	Logical channel 1 - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
25	LC1_LS_IRQ	Logical channel 1 - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
24	LC1_FE_IRQ	Logical channel 1 - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
23	LC1_COUNT_IRQ	Logical channel 1 - Frame counter reached status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
22	RESERVED		R	0
21	LC1_FIFO_OVF_IRQ	Logical channel 1 - FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
20	LC1_CRC_IRQ	Logical channel 1 - CRC error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
19	LC1_FSP_IRQ	Logical channel 1 - FSP error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
18	LC1_FW_IRQ	Logical channel 1 - Frame width error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
17	LC1_FSC_IRQ	Logical channel 1 - False sync code error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
16	RESERVED	Reserved	RW	0
15	LC0_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
14:12	RESERVED		R	0x0
11	LC0_FS_IRQ	Logical channel 0 - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	LC0_LE_IRQ	Logical channel 0 - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
9	LC0_LS_IRQ	Logical channel 0 - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
8	LC0_FE_IRQ	Logical channel 0 - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
7	LC0_COUNT_IRQ	Logical channel 0 - Frame counter reached status 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
6	RESERVED		R	0
5	LC0_FIFO_OVF_IRQ	Logical channel 0 - FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	LC0_CRC_IRQ	Logical channel 0 - CRC error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
3	LC0_FSP_IRQ	Logical channel 0 - FSP error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	LC0_FW_IRQ	Logical channel 0 - Frame width error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
1	LC0_FSC_IRQ	Logical channel 0 - False sync code error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	RESERVED	Reserved	RW	0

Table 8-88. Register Call Summary for Register CCP2_LC01_IRQSTATUS

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0] [1] [2]
- ISS CCP2 Registers: [3]

Table 8-89. CCP2_LC23_IRQENABLE

Address Offset	0x0000 0014		
Physical Address	0x5200 1C14	**Instance**	ISS_CCP2
Description	INTERRUPT ENABLE REGISTER - LOG CHAN 2 & 3 This register regroups all the events related to logical channel 2 and logical channel 3. The events related to logical channel 2 trigger SINTERRUPTN[2]. The events related to logical channel 3 trigger SINTERRUPTN[3]. The channel must be enabled for events to be generated on that channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LC3_OCPERROR_IRQ	RESERVED			LC3_FS_IRQ	LC3_LE_IRQ	LC3_LS_IRQ	LC3_FE_IRQ	LC3_COUNT_IRQ	RESERVED	LC3_FIFO_OVF_IRQ	LC3_CRC_IRQ	LC3_FSP_IRQ	LC3_FW_IRQ	LC3_FSC_IRQ	RESERVED	LC2_OCPERROR_IRQ	RESERVED			LC2_FS_IRQ	LC2_LE_IRQ	LC2_LS_IRQ	LC2_FE_IRQ	LC2_COUNT_IRQ	RESERVED	LC2_FIFO_OVF_IRQ	LC2_CRC_IRQ	LC2_FSP_IRQ	LC2_FW_IRQ	LC2_FSC_IRQ	RESERVED

Bits	Field Name	Description	Type	Reset
31	LC3_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
30:28	RESERVED		R	0x0
27	LC3_FS_IRQ	Logical channel 3 - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
26	LC3_LE_IRQ	Logical channel 3 - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
25	LC3_LS_IRQ	Logical channel 3 - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
24	LC3_FE_IRQ	Logical channel 3 - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
23	LC3_COUNT_IRQ	Logical channel 3 - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
22	RESERVED		R	0
21	LC3_FIFO_OVF_IRQ	Logical channel 3 - FIFO overflow error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
20	LC3_CRC_IRQ	Logical channel 3 - CRC error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
19	LC3_FSP_IRQ	Logical channel 3 - FSP error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
18	LC3_FW_IRQ	Logical channel 3 - Frame width error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
17	LC3_FSC_IRQ	Logical channel 3 - False sync code error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
16	RESERVED	Reserved	RW	0
15	LC2_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
14:12	RESERVED		R	0x0
11	LC2_FS_IRQ	Logical channel 2 - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	LC2_LE_IRQ	Logical channel 2 - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
9	LC2_LS_IRQ	Logical channel 2 - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	LC2_FE_IRQ	Logical channel 2 - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	LC2_COUNT_IRQ	Logical channel 2 - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	RESERVED		R	0
5	LC2_FIFO_OVF_IRQ	Logical channel 2 - FIFO overflow error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
4	LC2_CRC_IRQ	Logical channel 2 - CRC error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	LC2_FSP_IRQ	Logical channel 2 - FSP error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	LC2_FW_IRQ	Logical channel 2 - Frame width error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	LC2_FSC_IRQ	Logical channel 2 - False sync code error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	RESERVED	Reserved	RW	0

Table 8-90. Register Call Summary for Register CCP2_LC23_IRQENABLE

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0]
- ISS CCP2 Registers: [1]

Table 8-91. CCP2_LC23_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5200 1C18	**Instance**	ISS_CCP2
Description	INTERRUPT STATUS REGISTER - LOG CHAN 2 & 3 This register regroups all the events related to logical channel 2 and logical channel 3. The events related to logical channel 2 trigger SINTERRUPTN[2]. The events related to logical channel 3 trigger SINTERRUPTN[3]. The channel must be enabled for events to be generated on that channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LC3_OCPERROR_IRQ	RESERVED			LC3_FS_IRQ	LC3_LE_IRQ	LC3_LS_IRQ	LC3_FE_IRQ	LC3_COUNT_IRQ	RESERVED	LC3_FIFO_OVF_IRQ	LC3_CRC_IRQ	LC3_FSP_IRQ	LC3_FW_IRQ	LC3_FSC_IRQ	RESERVED	LC2_OCPERROR_IRQ	RESERVED			LC2_FS_IRQ	LC2_LE_IRQ	LC2_LS_IRQ	LC2_FE_IRQ	LC2_COUNT_IRQ	RESERVED	LC2_FIFO_OVF_IRQ	LC2_CRC_IRQ	LC2_FSP_IRQ	LC2_FW_IRQ	LC2_FSC_IRQ	RESERVED

Bits	Field Name	Description	Type	Reset
31	LC3_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
30:28	RESERVED		R	0x0
27	LC3_FS_IRQ	Logical channel 3 - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
26	LC3_LE_IRQ	Logical channel 3 - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
25	LC3_LS_IRQ	Logical channel 3 - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
24	LC3_FE_IRQ	Logical channel 3 - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
23	LC3_COUNT_IRQ	Logical channel 3 - Frame counter reached status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
22	RESERVED		R	0
21	LC3_FIFO_OVF_IRQ	Logical channel 3 - FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
20	LC3_CRC_IRQ	Logical channel 3 - CRC error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
19	LC3_FSP_IRQ	Logical channel 3 - FSP error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
18	LC3_FW_IRQ	Logical channel 3 - Frame width error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
17	LC3_FSC_IRQ	Logical channel 3 - False sync code error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
16	RESERVED	Reserved	RW	0
15	LC2_OCPERROR_IRQ	An OCP error occurred on the master write port. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
14:12	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
11	LC2_FS_IRQ	Logical channel 2 - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	LC2_LE_IRQ	Logical channel 2 - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
9	LC2_LS_IRQ	Logical channel 2 - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
8	LC2_FE_IRQ	Logical channel 2 - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
7	LC2_COUNT_IRQ	Logical channel 2 - Frame counter reached status 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
6	RESERVED		R	0
5	LC2_FIFO_OVF_IRQ	Logical channel 2 - FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	LC2_CRC_IRQ	Logical channel 2 - CRC error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
3	LC2_FSP_IRQ	Logical channel 2 - FSP error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
2	LC2_FW_IRQ	Logical channel 2 - Frame width error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
1	LC2_FSC_IRQ	Logical channel 2 - False sync code error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	RESERVED	Reserved	RW	0

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Table 8-92. Register Call Summary for Register CCP2_LC23_IRQSTATUS

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0] [1] [2]
- ISS CCP2 Registers: [3]

Table 8-93. CCP2_LCM_IRQENABLE

Address Offset	0x0000 002C		
Physical Address	0x5200 1C2C	**Instance**	ISS_CCP2
Description	INTERRUPT ENABLE REGISTER - Memory channel This register regroups all the events related to the memory channel 2. The events related to memory channel trigger SINTERRUPTN[8]. The channel must be enabled for events to be generated on that channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LCM_OCPERROR	LCM_EOF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LCM_OCPERROR	An interconnect error has been returned for a read (interconnect read master) or write (interconnect write master) transaction related to LCM operation 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	LCM_EOF	Memory read channel - End of frame 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 8-94. Register Call Summary for Register CCP2_LCM_IRQENABLE

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0]
- ISS CCP2 Registers: [1]

Table 8-95. CCP2_LCM_IRQSTATUS

Address Offset	0x0000 0030		
Physical Address	0x5200 1C30	**Instance**	ISS_CCP2
Description	INTERRUPT STATUS REGISTER - Memory channel This register regroups all the events related to memory channel. The events related to memory channel trigger SINTERRUPTN[8]. The channel must be enabled for events to be generated on that channel.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														LCM_OCPERROR	LCM_EOF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	LCM_OCPERROR	An interconnect error has been returned for a read (interconnect read master) or write (interconnect write master) transaction related to LCM operation 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	LCM_EOF	Memory read channel - End of frame 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

Table 8-96. Register Call Summary for Register CCP2_LCM_IRQSTATUS

ISS Interfaces

- ISS CCP2 Programming Event and Status Checking: [0] [1] [2]
- ISS CCP2 Registers: [3]

Table 8-97. CCP2_CTRL

Address Offset	0x0000 0040		
Physical Address	0x5200 1C40	**Instance**	ISS_CCP2
Description	GLOBAL CONTROL REGISTER This register controls the CCP2 receiver. This register must not be modified dynamically (except IF_EN bit field).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRACDIV																POSTED	DBG_EN	VP_CLK_POL	VP_ONLY_EN	RESERVED	VP_CLK_FORCE_ON	RESERVED	BURST			MODE	FRAME	RESERVED	RESERVED	IF_EN	

Bits	Field Name	Description	Type	Reset
31:15	FRACDIV	Fractional clock divider control for the video port. The mean video port clock is VPBASECLOCK * FRACDIV/65536. Valid range: 1-65536	RW	0x10000
14	POSTED	Selects between posted and non posted writes. 0x0: Non posted 0x1: Posted	RW	0

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Bits	Field Name	Description	Type	Reset
13	DBG_EN	Enables the debug mode. 0x0: Disable 0x1: Enable	RW	0
12	VP_CLK_POL	VP clock polarity 0x0: The CCP2 receiver writes the data on the VP on the L3 falling edge before the next falling PCLK edge. 0x1: The CCP2 receiver writes the data on the VP on the L3 rising edge before the next rising PCLK edge.	RW	0
11	VP_ONLY_EN	VP only enable. 0x0: The VP is enabled and the OCP master port are enabled. 0x1: The VP is enabled and the OCP master port is disabled. The embedded data and pixel data are output on the VP.	RW	0
10	RESERVED	Read returns reset value	RW	0
9	VP_CLK_FORCE_ON	Controls VP_PCLK gating during frame blanking periods. 0x0: The VP_PCLK is gated during vertical blanking periods. 0x1: The VP_PCLK is free-running during vertical blanking periods.	RW	0
8	RESERVED		R	0
7:5	BURST	Forces the write burst size used by the module. The write burst size must never exceed the output FIFO size. The output FIFO size can be read with the CCP2_GNQ.FIFODEPTH bit field. 0x0: 1x 64-bit burst = single request. 0x1: 2x 64-bit bursts. 0x3: 8x 64-bit bursts. 0x4: 16x 64-bit bursts. 0x2: 4x 64-bit bursts.	RW	0x0
4	MODE	Selects the receiver operating mode. This bit is only writable when the CCP2MODE input is 1. 0x0: MIPI CSI1 compatible mode. When this bit is set all CCP2 settings are ignored. If the settings are not set correctly to MIPI CSI1 values, the behavior of the receiver is unpredictable. 0x1: CCP2 compatible mode	RW	0
3	FRAME	Set the modality in which IF_EN works. 0x0: When software writes IF_EN = 0 the interface is disabled immediately. 0x1: When software writes IF_EN = 0 the interface is disabled after the next FEC sync code.	RW	0
2	RESERVED	Read returns reset value	RW	0
1	RESERVED	Read returns reset value	RW	0
0	IF_EN	Enables the physical interface to the module. 0x0: The interface is disabled. If FRAME = 0, it is disabled immediately. If FRAME = 1, it is disabled on the next FEC sync code. If FRAME=1, it is advised to disable the logical channels first (CCP2_LCx_CTRL.CHAN_EN=0) before writing IF_EN=0. 0x1: The interface is enabled immediately, the data acquisition starts on the next FSC sync code. Writing 1 to this register when the current value is 0 has the effect to clear the output FIFO. The pixel data of the following frame will be written in the PING buffer, that is, the CCP2_LCx_CTRL.PING_PONG bits are reset to 1 as well.	RW	0

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Table 8-98. Register Call Summary for Register CCP2_CTRL

ISS Interfaces

- ISS CCP2 Protocol and Data Formats: [0] [1]
- ISS CCP2 PHY: [2] [3]
- ISS CCP2 VP Interface: [4] [5]
- ISS CCP2 Memory Read Channel: [6] [7]
- ISS CCP2 Programming Hardware Setup/Initialization: [8]
- ISS CCP2 Programming Enable/Disable the Hardware: [9] [10] [11] [12] [13] [14] [15] [16]
- ISS CCP2 Programming Select the Signaling Scheme: [17] [18]
- ISS CCP2 Programming Select the Mode: MIPI CSI1 or CCP2: [19]
- ISS CCP2 Programming Burst Settings: [20]
- ISS CCP2 Programming Debug Mode: [21] [22]
- ISS CCP2 Programming Video Port: [23] [24] [25] [26] [27] [28] [29]
- ISS CCP2 Programming Controls: [30]
- ISS CCP2 Programming CRC: [31]
- ISS CCP2 Programming Destination Format: [32] [33]
- ISS CCP2 Programming Frame Acquisition: [34]
- ISS CCP2 Programming Memory Read Channel: [35] [36] [37] [38]
- ISS CCP2 Registers: [39] [40]
- ISS CSI2 REGS1 Registers: [41]

Table 8-99. CCP2_DBG

Address Offset	0x0000 0044		
Physical Address	0x5200 1C44	**Instance**	ISS_CCP2
Description	DEBUG REGISTER This register provides a way to debug the CCP2 receiver with no image sensor connected to the module. The debug mode is enabled by CCP2_CTRL.DBG_EN. Each write to this register provides a full 32bit word to the CCP2 receiver, even when only 8 or 16 bits are written. The newly written value is merged with the previous value (check the example in the programming model section).		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBG																															

Bits	Field Name	Description	Type	Reset
31:0	DBG	32-bit input value. Write only register. Reads return 0.	W	0x0000 0000

Table 8-100. Register Call Summary for Register CCP2_DBG

ISS Interfaces

- ISS CCP2 Programming Debug Mode: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS CCP2 Registers: [8]

Table 8-101. CCP2_GNQ

Address Offset	0x0000 0048		
Physical Address	0x5200 1C48	**Instance**	ISS_CCP2
Description	GENERIC PARAMETER REGISTER This register provide a way to read the generic parameters used in the design.		
Type	R		

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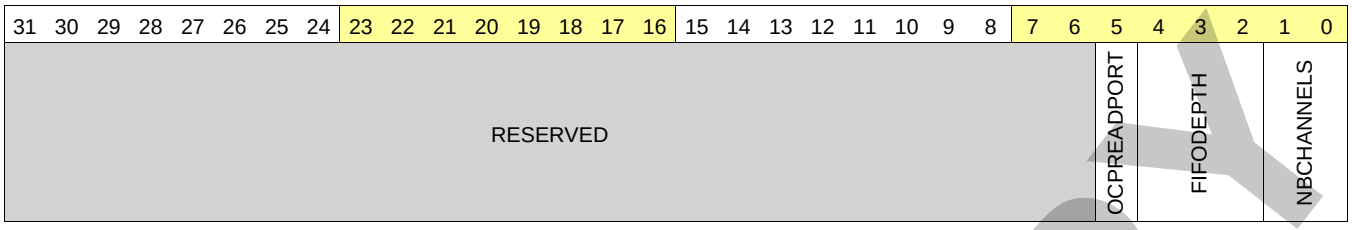


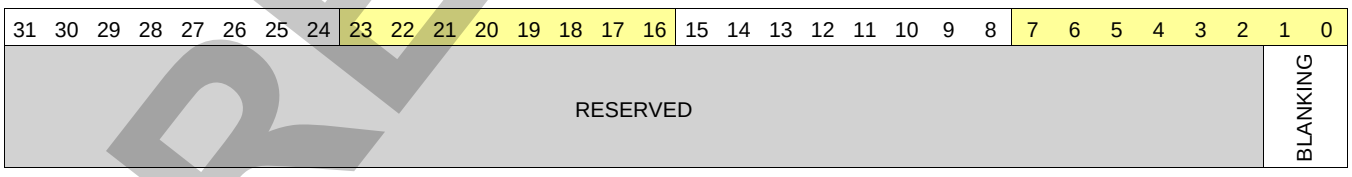
Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	OCPREADPORT	The OCP master read port, the DPCM encoder and ALAW decompression are only present when this bit is set.	R	1
4:2	FIFODEPTH	Output FIFO size in multiple of 64 bits. Read 0x3: 16 x 64 bits Read 0x4: 32 x 64 bits Read 0x2: 8 x 64 bits Read 0x0: 2 x 64 bits Read 0x1: 4 x 64 bits Read 0x5: 64 x 64 bits	R	0x5
1:0	NBCHANNELS	Number of logical channels supported by the module. Read 0x3: 8 logical channels Read 0x2: 4 logical channels Read 0x1: 2 logical channels Read 0x0: 1 logical channel	R	0x2

Table 8-102. Register Call Summary for Register CCP2_GNQ

ISS Interfaces
- ISS CCP2 Registers: [0] [1]

Table 8-103. CCP2_CTRL1

Address Offset	0x0000 004C		
Physical Address	0x5200 1C4C	**Instance**	ISS_CCP2
Description	GLOBAL CONTROL REGISTER (2) This register controls the CCP2 receiver.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	RO Rreturns 0s	0
1:0	BLANKING	Controls the number of clock pulses provided during vertical and horizontal clock periods. When the blanking period provided by the camera is lower than the value set here, the blanking period is shortened by the CCP2 to prevent internal FIFO overflow. Software must increase the sensor blanking period in that case.	RW	0x0

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Bits	Field Name	Description	Type	Reset
		0x0: 4 video port clock cycles 0x1: 16 video port clock cycles 0x2: 64 video port clock cycles 0x3: Free running		

Table 8-104. Register Call Summary for Register CCP2_CTRL1

ISS Interfaces

- ISS CCP2 VP Interface: [0] [1] [2] [3]
- ISS CCP2 Memory Read Channel: [4] [5]
- ISS CCP2 Registers: [6]

Table 8-105. CCP2_LCx_CTRL

Address Offset	0x0000 0050 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C50 + (x * 0x30)	**Instance**	ISS_CCP2
Description	CONTROL REGISTER - LOG CHAN 0 This register controls the logical channel 0. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20	19	18	17	16	15 14 13 12 11 10 9 8	7 6 5 4 3 2	1	0
COUNT	RESERVED	CRC_EN	DPCM_PRED	PING_PONG	COUNT_UNLOCK	ALPHA	FORMAT	REGION_EN	CHAN_EN

Bits	Field Name	Description	Type	Reset
31:24	COUNT	Sets the number of frame to acquire. Once the frame acquisition starts, the COUNT value is decremented after every frame. When COUNT reaches 0, the COUNT_IRQ interrupt is triggered and CHAN_EN is set to 0. Writes to this bit field are controlled by the COUNT_UNLOCK bit. COUNT can be overwritten dynamically with a new count value. 0: Infinite number of frames (no count). 1: 1 frame to acquire ... 255: 255 frames to acquire.	RW	0x00
23:20	RESERVED		R	0x0
19	CRC_EN	Enables the cyclic redundancy check. 0x0: Disabled 0x1: Enabled	RW	0
18	DPCM_PRED	Selects the DPCM predictor to be used for the RAW6+DPCM10, RAW7+DPCM10 and RAW8+DPCM12 data formats. The RAW8+DPCM10 data format always use the simple predictor. 0x0: The advanced predictor is used 0x1: The simple predictor is used.	RW	0

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Bits	Field Name	Description	Type	Reset
17	PING_PONG	Indicates whether the PING or PONG destination address (CCP2_LC0_DAT_PING_ADDR or CCP2_LC0_DAT_PONG_ADDR) was used to write the last frame. This bit field toggles after every FEC sync code. Read 0x1: PONG buffer Read 0x0: PING buffer	R	1
16	COUNT_UNLOCK	Unlock writes to the COUNT bit field. Write 0x0: COUNT bit field is locked. Writes have no effect Write 0x1: COUNT bit field is unlocked. Writes are possible.	W	0
15:8	ALPHA	Alpha value for RGB888 and RBG444.	RW	0x00

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Bits	Field Name	Description	Type	Reset
7:2	FORMAT	Data format selection. 0xD: RAW7 + DPCM10 + EXP16 0x15: RAW10 + EXP16 0x1E: RAW10 -> RAW8 RAW10 data from sensor is right shifted to produce RAW8 before it is send to memory 0x8: RAW6 + EXP8 0x5: RGB565 0x1B: RAW10 -> RAW8 DPCM RAW10 data from sensor is DPCM compressed into RAW8 before it is send to memory. 0x2: YUV4:2:0 0x4: RGB444 + EXP16 0x6: RGB888 0x1: YUV4:2:2 LITTLE ENDIAN 0x1D: JPEG8 0x0: YUV4:2:2 BIG ENDIAN 0xB: RAW10 -> RAW6 DPCM RAW10 data from sensor is DPCM compressed into RAW6 before it is send to memory. Used predictor is selected by the DPCM_PRED bit. 0x20: RAW10 -> RAW8 ALAW 0x3: YUV4:2:2 + VP or RAW8 + VP 0x17: RAW10 -> RAW7 DPCM + EXP8 RAW10 data from sensor is DPCM compressed into RAW7 and expanded to 8 bits before it is send to memory. Used predictor is selected by the DPCM_PRED bit. 0x11: RAW8 + DPCM10 + EXP16 0xA: RAW6 + DPCM10 + VP 0x9: RAW6 + DPCM10 + EXP16 0x10: RAW8 This mode can be used to output RAW6 and RAW7 as well. 0x21: RAW8 DPCM10 -> ALAW 0x12: RAW8 + DPCM10 + VP 0x13: RAW10 -> RAW7 DPCM RAW10 data from sensor is DPCM compressed into RAW7 before it is send to memory. Used predictor is selected by the DPCM_PRED bit. 0x18: RAW12 0x14: RAW10 0xE: RAW7 + DPCM10 + VP 0x16: RAW10 + VP 0x1C: JPEG8 + FSP 0x7: RGB888 + EXP32 0x19: RAW12 + EXP16 0x1F: RAW8 DPCM12 -> RAW12 + VP Used predictor is selected by the DPCM_PRED bit. 0x1A: RAW12 + VP 0xF: RAW10 -> RAW6 DPCM + EXP8 RAW10 data from sensor is DPCM compressed into RAW6 and expanded to 8 bits before it is send to memory. Used predictor is selected by the DPCM_PRED bit. 0xC: RAW7 + EXP8	RW	0x00

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Bits	Field Name	Description	Type	Reset
1	REGION_EN	Enables the setting of regions of interest in the frame: SOF region, EOF region and DAT region. 0x0: Disabled 0x1: Enabled	RW	0
0	CHAN_EN	Enables the logical channel 0x0: Disabled 0x1: Enabled	RW	0x1 for LC0 0x0 for LC1 0x0 for LC2 0x0 for LC3

Table 8-106. Register Call Summary for Register CCP2_LCx_CTRL

ISS Interfaces

- ISS CCP2 Protocol and Data Formats: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- ISS CCP2 Data Compression: [16]
- ISS CCP2 Programming Register Accessibility During Frame Processing: [17]
- ISS CCP2 Programming Enable/Disable the Hardware: [18] [19] [20]
- ISS CCP2 Programming Controls: [21]
- ISS CCP2 Programming Region-of-Interest: [22] [23]
- ISS CCP2 Programming CRC: [24] [25]
- ISS CCP2 Programming Destination Format: [26]
- ISS CCP2 Programming Frame Acquisition: [27] [28] [29] [30] [31] [32] [33] [34]
- ISS CCP2 Programming Pixel Data Region: [35] [36]
- ISS CCP2 Registers: [37] [38] [39]

Table 8-107. CCP2_LCx_CODE

Address Offset	0x0000 0054 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C54 + (x * 0x30)	**Instance**	ISS_CCP2
Description	CODE REGISTER - LOG CHAN 0 This register sets the codes that are used in the 32-bit synchronization codes to recognize the logical channel, frame start, frame end, line start and line end codes. This register applies for logical channel 0 only. The default values are usually not supposed to be modified. Updating this register with new codes under a flowing serial transmission on that channel will cause unexpected result.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CHAN_ID				FEC				FSC				LEC				LSC			

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:16	CHAN_ID	Log chan 0 identifier. The channel identifier is located between bits 4 to 7 in the 32-bit synchronization codes.	RW	0x0
15:12	FEC	Log chan 0 frame end sync code identifier. The sync code identifier is located between bits 0 to 3 in the 32-bit synchronization codes.	RW	0x3
11:8	FSC	Log chan 0 frame start sync code identifier. The sync code identifier is located between bits 0 to 3 in the 32-bit synchronization codes.	RW	0x2
7:4	LEC	Log chan 0 line end sync code identifier. The sync code identifier is located between bits 0 to 3 in the 32-bit synchronization codes.	RW	0x1
3:0	LSC	Log chan 0 line start sync code identifier. The sync code identifier is located between bits 0 to 3 in the 32-bit synchronization codes.	RW	0x0

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Table 8-108. Register Call Summary for Register CCP2_LCx_CODE

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Synchronization Codes: [1] [2] [3] [4] [5]
- ISS CCP2 Registers: [6]

Table 8-109. CCP2_LCx_STAT_START

Address Offset	0x0000 0058 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C58 + (x * 0x30)	**Instance**	ISS_CCP2
Description	STATUS LINE START REGISTER - LOG CHAN 0 This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOF								RESERVED								SOF							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	EOF	Sets the vertical position of the EOF status lines in regards of the FSC sync code. From 0 to 4095.	RW	0x000
15:12	RESERVED		R	0x0
11:0	SOF	Sets the vertical position of the EOF status lines in regards of the FSC sync code. Should always be 0.	RW	0x000

Table 8-110. Register Call Summary for Register CCP2_LCx_STAT_START

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Video Port: [1]
- ISS CCP2 Programming Status Data: [2] [3]
- ISS CCP2 Registers: [4]

Table 8-111. CCP2_LCx_STAT_SIZE

Address Offset	0x0000 005C + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C5C + (x * 0x30)	**Instance**	ISS_CCP2
Description	STATUS LINE SIZE REGISTER - LOG CHAN 0 This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOF								RESERVED								SOF							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	EOF	Sets the number of EOF status lines From 0 to 4095	RW	0x000
15:12	RESERVED		R	0x0
11:0	SOF	Sets the number of SOF status line(s) From 0 to 4095	RW	0x000

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Table 8-112. Register Call Summary for Register CCP2_LCx_STAT_SIZE

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Video Port: [1]
- ISS CCP2 Programming Status Data: [2] [3] [4]
- ISS CCP2 Registers: [5]

Table 8-113. CCP2_LCx_SOF_ADDR

Address Offset	0x0000 0060 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C60 + (x * 0x30)	**Instance**	ISS_CCP2
Description	SOF STATUS LINE MEM ADDRESS REGISTER - LOG CHAN 0 This register sets the 32-bit memory address where the SOF data are stored. The 5 LSBs are ignored: the address must be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-114. Register Call Summary for Register CCP2_LCx_SOF_ADDR

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Status Data: [1]
- ISS CCP2 Registers: [2]

Table 8-115. CCP2_LCx_EOF_ADDR

Address Offset	0x0000 0064 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C64 + (x * 0x30)	**Instance**	ISS_CCP2
Description	EOF STATUS LINE MEM ADDRESS REGISTER - LOG CHAN 0 This register sets the 32-bit memory address where the EOF data are stored. The 5 LSBs are ignored: the address must be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-116. Register Call Summary for Register CCP2_LCx_EOF_ADDR

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Status Data: [1]
- ISS CCP2 Registers: [2]

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Table 8-117. CCP2_LCx_DAT_START

Address Offset	0x0000 0068 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C68 + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA START REGISTER - LOG CHAN 0 This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERT								RESERVED															

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	VERT	Sets the vertical position of the data in regards of the FSC sync code. From 0 to 4095 lines.	RW	0x000
15:0	RESERVED		R	0x0000

Table 8-118. Register Call Summary for Register CCP2_LCx_DAT_START

ISS Interfaces

- ISS CCP2 Programming Video Port: [0]
- ISS CCP2 Programming Pixel Data Region: [1]
- ISS CCP2 Registers: [2]

Table 8-119. CCP2_LCx_DAT_SIZE

Address Offset	0x0000 006C + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C6C + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA SIZE REGISTER - LOG CHAN 0 This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERT								RESERVED															

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	VERT	Sets the vertical size of the data window. From 0 to 4095 lines. If VERT = "0", no data is output.	RW	0x000
15:0	RESERVED		R	0x0000

Table 8-120. Register Call Summary for Register CCP2_LCx_DAT_SIZE

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Video Port: [1]
- ISS CCP2 Programming Pixel Data Region: [2]
- ISS CCP2 Registers: [3]

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Table 8-121. CCP2_LCx_DAT_PING_ADDR

Address Offset	0x0000 0070 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C70 + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA MEM PING ADDRESS REGISTER - LOG CHAN 0 This register sets the 32-bit memory address where the pixel data are stored. The destination is double buffered: this register sets the PING address. Double buffering is enabled when the addresses CCP2_LC0_DAT_PING_ADDR and CCP2_LC0_DAT_PONG_ADDR are different. The 5 LSBs are ignored: the address must be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-122. Register Call Summary for Register CCP2_LCx_DAT_PING_ADDR

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Frame Acquisition: [1]
- ISS CCP2 Programming Pixel Data Region: [2] [3] [4] [5]
- ISS CCP2 Registers: [6]

Table 8-123. CCP2_LCx_DAT_PONG_ADDR

Address Offset	0x0000 0074 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C74 + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA MEM PONG ADDRESS REGISTER - LOG CHAN 0 This register sets the 32-bit memory address where the pixel data are stored. The destination is double buffered: this register sets the PONG address. Double buffering is enabled when the addresses CCP2_LC0_DAT_PING_ADDR and CCP2_LC0_DAT_PONG_ADDR are different. The 5 LSBs are ignored: the address must be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-124. Register Call Summary for Register CCP2_LCx_DAT_PONG_ADDR

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Frame Acquisition: [1]
- ISS CCP2 Programming Pixel Data Region: [2] [3] [4] [5]
- ISS CCP2 Registers: [6]

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Table 8-125. CCP2_LCx_DAT_OFST

Address Offset	0x0000 0078 + (x * 0x30)	**Index**	x = 0 to 3
Physical Address	0x5200 1C78 + (x * 0x30)	**Instance**	ISS_CCP2
Description	DATA MEM ADDRESS OFFSET REGISTER - LOG CHAN 0 This register sets the offset, which is applied on the destination address after each line is written to memory. This register applies for both CCP2_LC0_DAT_PING_ADDR and CCP2_LC0_DAT_PONG_ADDR. For example, it enables to perform 2D data transfers of the pixel data into a frame buffer. In such case, the pixel data and frame buffer data must have the same data format. The 5 LSBs are ignored: the offset must be a multiple of 32 bytes. Only full 64-bits words are written to memory at the end of lines. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFST																											RESERVED					

Bits	Field Name	Description	Type	Reset
31:5	OFST	Line offset programmed in bytes. If OFST = 0, the data is written contiguously in memory. Otherwise, OFST sets the destination offset between the first pixel of the previous line and the first pixel of the current line. NOTE: An OCP access (read/write) is required to properly update the CCP2_LCx_DAT_OFST register	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-126. Register Call Summary for Register CCP2_LCx_DAT_OFST

ISS Interfaces

- ISS CCP2 Programming Register Accessibility During Frame Processing: [0]
- ISS CCP2 Programming Pixel Data Region: [1] [2] [3] [4] [5] [6] [7]
- ISS CCP2 Registers: [8] [9]

Table 8-127. CCP2_LCM_CTRL

Address Offset	0x0000 01D0		
Physical Address	0x5200 1DD0	**Instance**	ISS_CCP2
Description	Control register for the memory channel. It defines the data format of the source frame stored in memory and how this frame is processed.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST_PACK	DST_DPCM_PRED	DST_COMPR		RESERVED		DST_FORMAT		SRC_PACK	SRC_DPCM_PRED	SRC_DECOMPR		SRC_FORMAT				RESERVED								BURST_SIZE			READ_THROTTLE			DST_PORT	RESERVED	CHAN_EN

Bits	Field Name	Description	Type	Reset
31	DST_PACK	Data is packed before it is send to memory. Applies to RAW6, RAW7, RAW10, and RAW12 only. 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
30	DST_DPCM_PRED	Selects the DPCM predictor to be used for the RAW6+DPCM10 and RAW7+DPCM10 data formats. The RAW8+DPCM10 data format always use the simple predictor. 0x0: The advanced predictor is used 0x1: The simple predictor is used.	RW	0
29:28	DST_COMPR	Enables data compression of data sent to memory 0x0: No compression 0x1: A-Law compression RAW10 -> RAW8 A-Law when DST_FORMAT=RAW8 other destination formats are invalid. 0x2: DPCM compression RAW10 -> RAW6 DPCM when DST_FORMAT=RAW6 RAW10 -> RAW7 DPCM when DST_FORMAT=RAW7 RAW10 -> RAW8 DPCM when DST_FORMAT=RAW8 other destination formats are invalid.	RW	0x0
27	RESERVED		R	0
26:24	DST_FORMAT	Output format selection. Not every combination between input and output formats are possible. 0x6: RAW16 0x1: RAW7 0x0: RAW6 0x2: RAW8 0x4: RAW12 0x5: RAW14 0x3: RAW10	RW	0x0
23	SRC_PACK	Data stored in memory is packed and must be unpacked. 0x0: Disabled 0x1: Enabled	RW	0
22	SRC_DPCM_PRED	Selects the DPCM predictor to be used for the RAW6+DPCM10, RAW7+DPCM10 and RAW8+DPCM12 data formats. The RAW8+DPCM10 and RAW6 + DPCM12 data format always use the simple predictor. 0x0: The advanced predictor is used 0x1: The simple predictor is used.	RW	0
21:20	SRC_DECOMPR	Enable decompression of incoming data 0x0: No decompression 0x1: A-Law decompression RAW8 A-Law -> RAW10 when SRC_FORMAT=RAW8 other source formats are invalid. 0x3: DPCM decompression RAW6 DPCM -> RAW12 when SRC_FORMAT=RAW6 RAW8 DPCM -> RAW12 when SRC_FORMAT=RAW8 other source formats are invalid. 0x2: DPCM decompression RAW6 DPCM -> RAW10 when SRC_FORMAT=RAW6 RAW7 DPCM -> RAW10 when SRC_FORMAT=RAW7 RAW8 DPCM -> RAW10 when SRC_FORMAT=RAW8 other source formats are invalid.	RW	0x0

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Bits	Field Name	Description	Type	Reset
19:16	SRC_FORMAT	Data format of the data stored in memory. As there is no header embedded in the data sent to memory the user is responsible of choosing the adequate format. 0x6: RAW16 0x1: RAW7 0xA: Reserved 0x7: Reserved 0xD: Reserved 0x0: RAW6 0x2: RAW8 0x8: Reserved 0x9: Reserved 0xB: Reserved 0x4: RAW12 0x5: RAW14 0xF: Reserved 0xC: Reserved 0x3: RAW10 0xE: Reserved	RW	0x0
15:8	RESERVED		R	0x00
7:5	BURST_SIZE	Defines the burst size of the master read port 0x0: 1x 64-bit burst = single request. 0x1: 2x 64-bit bursts. 0x3: 8x 64-bit bursts. 0x4: 16x 64-bit bursts. 0x2: 4x 64-bit bursts.	RW	0x0
4:3	READ_THROTTLE	Limit maximum data read speed for memory to memory operation 0x0: Full speed. Throughput is limited by internal processing capabilities. 0x1: 1/2 speed 0x3: 1/8 speed 0x2: 1/4 speed	RW	0x0
2	DST_PORT	Select the destination port 0x0: Data is send to video port, it is always send without compression or packing. The DST_COMPR, DST_DPCM_PRED, DST_PACK, CCP2_LCM_DST_WRITE, and CCP2_LCM_DST_OFST registers have no effect. 0x1: Data is send to memory.	RW	0
1	RESERVED		R	0
0	CHAN_EN	Enables the read from memory channel. Before enabling the memory read channel software must: - disable the physical interface using the IF_EN bit - wait until disabling of the physical interface is effective (depends on the FRAME bit) Read from memory starts as soon as this bit is set, therefore all CCP2_LCM_x registers must be configured correctly before. This bit is cleared by hardware at the end of the frame. 0x0: Disabled 0x1: Enabled	RW	0

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Table 8-128. Register Call Summary for Register CCP2_LCM_CTRL

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- ISS CCP2 Programming Memory Read Channel: [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33]
- ISS CCP2 Registers: [34]

Table 8-129. CCP2_LCM_VSIZE

Address Offset	0x0000 01D4		
Physical Address	0x5200 1DD4	**Instance**	ISS_CCP2
Description	Memory channel vertical framing register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT								RESERVED															

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	COUNT	Defines the line count to be read from memory. From 1 to 8191 lines.	RW	0x0001
15:0	RESERVED		R	0x0000

Table 8-130. Register Call Summary for Register CCP2_LCM_VSIZE

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0]
- ISS CCP2 Programming Memory Read Channel: [1]
- ISS CCP2 Registers: [2]

Table 8-131. CCP2_LCM_HSIZE

Address Offset	0x0000 01D8		
Physical Address	0x5200 1DD8	**Instance**	ISS_CCP2
Description	Memory read channel horizontal framing register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT								RESERVED								SKIP							

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0x0
30:16	COUNT	Horizontal count of samples to output after the skipped pixels. Valid values: 1 to 32767.	RW	0x0001
15	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
14:0	SKIP	Horizontal count of samples to skip after the start of the line. When DPCM compressed data is read from memory using this feature is the only valid way to set a horizontal starting position. Valid values: 0 to 32767. 0 disables pixel skipping	RW	0x0000

Table 8-132. Register Call Summary for Register CCP2_LCM_HSIZE

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- ISS CCP2 Programming Memory Read Channel: [9] [10] [11] [12] [13]
- ISS CCP2 Registers: [14] [15]

Table 8-133. CCP2_LCM_PREFETCH

Address Offset	0x0000 01DC		
Physical Address	0x5200 1DDC	**Instance**	ISS_CCP2
Description	This register defines the amount of data to be fetched from memory. It must be consistent with the CCP2_LCM_HSIZE register (check programming model).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HWORDS														RESERVED	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:3	HWORDS	64 bit words to read from memory for each line of the image. Possible values 1..8191	RW	0x0001
2:0	RESERVED		R	0x0

Table 8-134. Register Call Summary for Register CCP2_LCM_PREFETCH

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0] [1]
- ISS CCP2 Programming Memory Read Channel: [2] [3]
- ISS CCP2 Registers: [4]

Table 8-135. CCP2_LCM_SRC_ADDR

Address Offset	0x0000 01E0		
Physical Address	0x5200 1DE0	**Instance**	ISS_CCP2
Description	Memory channel source address register This register sets the 32-bit memory address where the pixel data are stored. The 5 LSBs are ignored: the address must be aligned on a 32-byte boundary.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

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Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most-significant bits of the 32-bit address	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-136. Register Call Summary for Register CCP2_LCM_SRC_ADDR

ISS Interfaces
- ISS CCP2 Memory Read Channel: [0] [1] [2] [3]
- ISS CCP2 Programming Memory Read Channel: [4] [5]
- ISS CCP2 Registers: [6]

Table 8-137. CCP2_LCM_SRC_OFST

Address Offset	0x0000 01E4		
Physical Address	0x5200 1DE4	**Instance**	ISS_CCP2
Description	Memory channel source offset register. This register sets the offset, which is applied on the source address after each line is read from memory. For example, it enables to perform 2D data transfers of the pixel data from a frame buffer. In such case, the pixel data and frame buffer data must have the same data format. The 5 LSBs are ignored: the offset must be a multiple of 32 bytes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFST																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	OFST	Line offset programmed in bytes. If OFST = 0, the data is read contiguously from memory. Otherwise, OFST sets the source offset between the first pixel of the previous line and the first pixel of the current line.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-138. Register Call Summary for Register CCP2_LCM_SRC_OFST

ISS Interfaces
- ISS CCP2 Memory Read Channel: [0] [1] [2]
- ISS CCP2 Programming Memory Read Channel: [3] [4]
- ISS CCP2 Registers: [5]

Table 8-139. CCP2_LCM_DST_ADDR

Address Offset	0x0000 01E8		
Physical Address	0x5200 1DE8	**Instance**	ISS_CCP2
Description	Memory channel destination address. This register sets the 32-bit memory address where the pixel data are stored. The 5 LSBs are ignored: the address must be aligned on a 32-byte boundary.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

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Table 8-140. Register Call Summary for Register CCP2_LCM_DST_ADDR

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0] [1] [2] [3]
- ISS CCP2 Programming Memory Read Channel: [4] [5]
- ISS CCP2 Registers: [6]

Table 8-141. CCP2_LCM_DST_OFST

Address Offset	0x0000 01EC		
Physical Address	0x5200 1DEC	**Instance**	ISS_CCP2
Description	Memory channel destination offset register. This register sets the offset, which is applied on the destination address after each line is written to memory. For example, it enables to perform 2D data transfers of the pixel data into a frame buffer. In such case, the pixel data and frame buffer data must have the same data format. The 5 LSBs are ignored: the offset must be a multiple of 32 bytes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFST																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	OFST	Line offset programmed in bytes. If OFST = 0, the data is written contiguously to memory if possible. At the end of a line only full 32 bit words will be written, creating eventually gaps at the end of lines. Otherwise, OFST sets the destination offset between the first pixel of the previous line and the first pixel of the current line.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-142. Register Call Summary for Register CCP2_LCM_DST_OFST

ISS Interfaces

- ISS CCP2 Memory Read Channel: [0] [1]
- ISS CCP2 Programming Memory Read Channel: [2] [3]
- ISS CCP2 Registers: [4] [5]

Table 8-143. CCP2_LCM_HISTORY

Address Offset	0x0000 01F0		
Physical Address	0x5200 1DF0	**Instance**	ISS_CCP2
Description	Controls operation of the DPCM history read/write feature		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EN_HIST_RD	EN_HIST_WR	HIST_EXPORT															

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Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	HIST_DATA_DST	Selects destination of pixel data 0x0: History data is send to OCP port Pixel data is send to video port 0x1: History data is send to OCP port Pixel data is send to OCP port	RW	0
17	EN_HIST_RD	Enable DPCM history read 0x0: Disable 0x1: Enable	RW	0
16	EN_HIST_WR	Enable DPCM history write 0x0: Disable 0x1: Enable	RW	0
15:0	HIST_EXPORT	Defines the horizontal position at which DPCM history information is written. The first decoded sample of a line has position 0 The last decoded sample has position SKIP+COUNT–1 Valid range [3..SKIP+COUNT–1]	RW	0x0000

Table 8-144. Register Call Summary for Register CCP2_LCM_HISTORY

ISS Interfaces
- ISS CCP2 Memory Read Channel: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19]
- ISS CCP2 Registers: [20] [21] [22]

Table 8-145. CCP2_LCM_HIST_ADDR

Address Offset	0x0000 01F4		
Physical Address	0x5200 1DF4	**Instance**	ISS_CCP2
Description	Source and destination address in SDRAM of HISTORY data when CCP2_LCM_HISTORY[18] HIST_DATA_DST=1 Unused when CCP2_LCM_HISTORY[18] HIST_DATA_DST=0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most significant bits of the 32-bit address.	RW	0x000 0000
4:0	RESERVED		R	0x00

Table 8-146. Register Call Summary for Register CCP2_LCM_HIST_ADDR

ISS Interfaces
- ISS CCP2 Memory Read Channel: [0] [1]
- ISS CCP2 Programming Memory Read Channel: [2]
- ISS CCP2 Registers: [3]

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8.2.5 ISS CSI2

8.2.5.1 ISS CSI2 Environment

8.2.5.1.1 ISS CSI2 Protocol and Data Format

The CSI2 supports MIPI CSI2 multiple data type formats. This section describes MIPI CSI2 protocol and data formats. The CSI2 is compatible with the *MIPI CSI2 Specification v1.0-01-00 r0.03*. Table 8-147 lists the MIPI CSI2 supported by CSI2 formats in addition to JPEG8. Shading in the primary and secondary MIPI CSI2_defined formats indicates special format extensions of the CSI2 receiver.

Table 8-147 summarizes the pixel formats supported by the CSI2 receiver interface.

Table 8-147. ISS CSI2 Pixel Format Modes

CSI2_CTX_CTRL2_i[9:0] Format	CSI2 Data Format	Bits per Pixel (BPP)	Data Size Increases in Memory	2D Mode Availability[1]	Comments
0x18	YUV4:2:0 8 bit	12	0%	Yes	
0x19	YUV4:2:0 10 bit	12	0%	Yes	
0x1E	YUV4:2:2 8 bit	16	0%	Yes	
0x1F	YUV4:2:2 10 bit	16	0%	Yes	
0x22	RGB565	16	0%	Yes	
0x24	RGB888	24	0%	Yes	
0x29	RAW7	7	0%	Yes	
0x2A	RAW8	8	8%	Yes	
0x2B	RAW10	10	0%	Yes	
0x2C	RAW12	12	0%	Yes	
0x2D	RAW14	14	0%	Yes	
0xA3	RGB666 + EXP32	32	77%	Yes	
0x68	RAW6 + EXP8	8	33%	Yes	
0x69	RAW7 + EXP8	8	14%	Yes	
0xA0	RGB444 + EXP16	16	33%	Yes	
0xA1	RGB555 + EXP16	16	6%	Yes	
0xAB	RAW10 + EXP16	16	60%	Yes	
0xAC	RAW12 + EXP16	16	33%	Yes	
0xAD	RAW14 + EXP16	16	14%	Yes	
0xE3	RGB666 + EXP32	32	77%	Yes	
0xE4	RGB888 + EXP32	32	33%	Yes	
0x2A8	RAW6 + DPCM10 + EXP16	16	166%	Yes	DPCM decompression
0x229	RAW7 + DPCM10 + EXP16	16	128%	Yes	DPCM decompression
0x2AA	RAW8 + DPCM10 + EXP16	16	100%	Yes	DPCM decompression
0x369	RAW7 + DPCM12 + EXP16	16	128%	Yes	DPCM decompression
0x36A	RAW8 + DPCM12 + EXP16	16	100%	Yes	DPCM decompression
0x3A8	RAW6 + DPCM12 + EXP16	16	166%	Yes	DPCM decompression
0x12	JPEG8	8	0%		

(1) If 2D mode is available, there are no supplementary constraints on data width. 2D mode does not apply when sending to the video port (VP).

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For more information about how the data formats are transmitted and how the data are stored in memory, see Section 8.2.5.1.1.4, *CSI2 Operating Modes*.

NOTE: The VP formats are not included in Table 8-147, because they are not sent to memory; instead they are sent to the ISP for further processing.

NOTE: Data written by CSI2 can be read back by the CCP2 read channel. CCP2 can get data from a sensor or memory. For more information about supported memory operations, see Table 8-59.

8.2.5.1.1.1 ISS CSI2 Physical Layer

The CSI2_A/CSI2_B/CSI2_C receivers (also generally referenced to as CSI2_RECEIVER) are tightly connected to a PHY layer (for more information about the PHY, see Section 8.2.3, *ISS CSI PHY*). Table 8-148 lists the CSI2_A receiver I/O signals, Table 8-149 lists the CSI2_B receiver I/O and Table 8-150 lists the CSI2_C receiver I/O. The CSI2_RECEIVER provides access to the complex I/O configuration through a serial configuration port (SCP) interface from the CSI2_COMPLEXIO_CFG register. The CSI2_RECEIVER can access up to 2x8 32-bit registers in the complex I/O. The 16 registers in the complex I/O are handled as two banks of 8 registers each. Software must select a bank, prior to doing registers accesses, using the CSI2_COMPLEXIO_CFG[31] PHY_REG_BANK register bit.

Table 8-148. ISS CSI2_A I/O Description

Signal Name		I/O[1]	Description
csiporta_lane0x	lane 0 (position 1)	I	Serial data/clock input
csiporta_lane0y			
csiporta_lane1x	lane 1 (position 2)	I	Serial data/clock input
csiporta_lane1y			
csiporta_lane2x	lane 2 (position 3)	I	Serial data/clock input
csiporta_lane2y			
csiporta_lane3x	lane 3 (position 4)	I	Serial data/clock input
csiporta_lane3y			
csiporta_lane4x	lane 4 (position 5)	I	Serial data input only
csiporta_lane4y			

(1) I = Input

Table 8-149. ISS CSI2_B I/O Description

Signal Name		I/O[1]	Description
csiportb_lane0x	line 0 (position 1)	I	Serial data/clock input
csiportb_lane0y			
csiportb_lane1x	line 1 (position 2)	I	Serial data/clock input
csiportb_lane1y			
csiportb_lane2x	line 2 (position 3)	I	Serial data/clock input
csiportb_lane2y			

(1) I = Input

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Table 8-150. ISS CSI2_C I/O Description

Signal Name		I/O[1]	Description
csiportc_lane0x	lane 0 (position 1)	I	Serial data/clock input
csiportc_lane0y			
csiportc_lane1x	lane 1 (position 2)	I	Serial data/clock input
csiportc_lane1y			

(1) I = Input

NOTE: The serial lane can be used as clock lane or data lane (excluding lane 4 on the CSI2_A I/O). The MIPI CSI2 protocol requires one clock lane (others are data lane or unused lane).

Lanes support the two operating modes:

- HS mode: High-speed transmit mode
- Off mode: Lane is off.

8.2.5.1.1.2 ISS CSI2 Lane Merger

The layer consists of lane merger logic to merge the incoming serial stream into a byte stream. The lane merger can merge up to four lanes (CSI2_A) into a single byte stream. The bits are sent with the LSB first. The order of the lanes at the CSI2_A and CSI2_B receiver cores depends on the lane configuration. The merger is not used for a single lane.

The number of lanes and their configuration can be changed only in ULPM or when all data lanes are in off mode.

Figure 8-36 to Figure 8-39 show the byte position into each serial link for one to four data lane configurations. The byte stream always starts from lane 1. It finishes on one of the lanes, depending on the number of bytes to receive and the number of lanes.

Figure 8-36. ISS CSI2 One Data-Lane Configuration

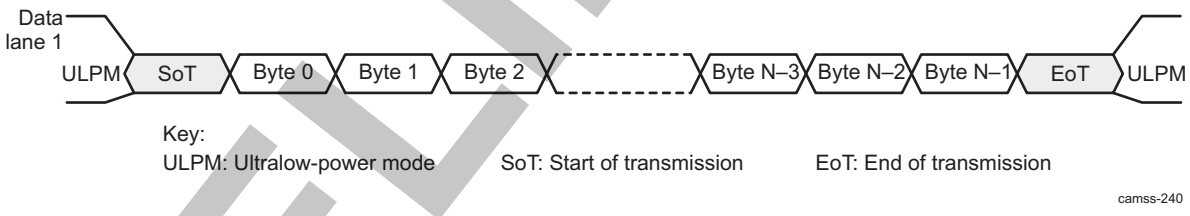

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Figure 8-37. ISS CSI2 Two Data-Lane Merger Configuration

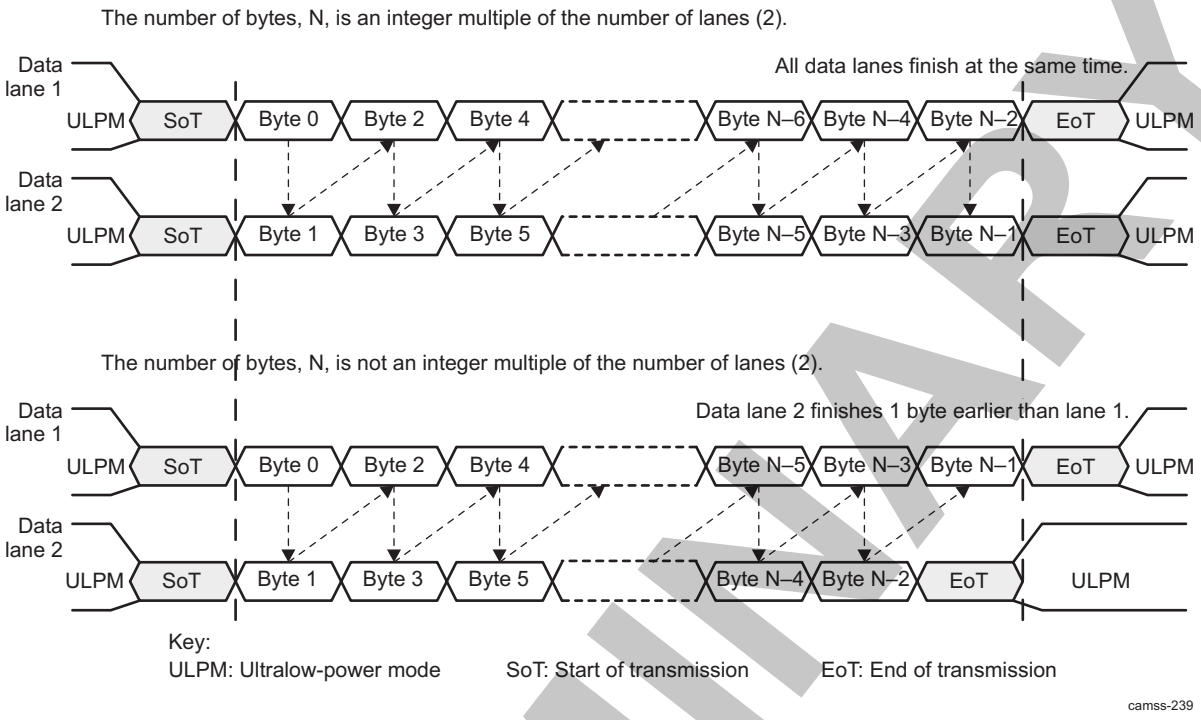

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Figure 8-38. ISS CSI2 Three Data-Lane Merger Configuration

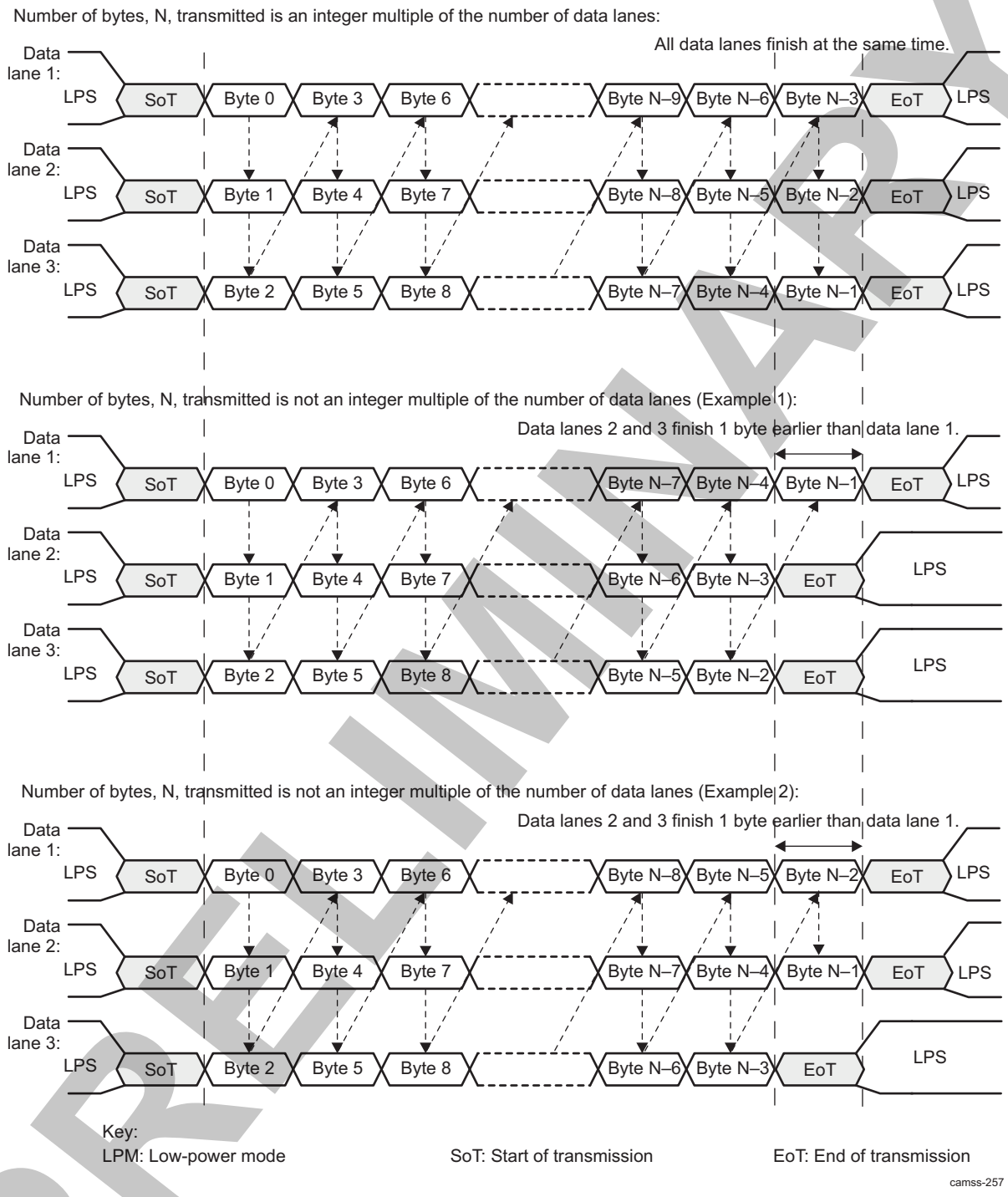

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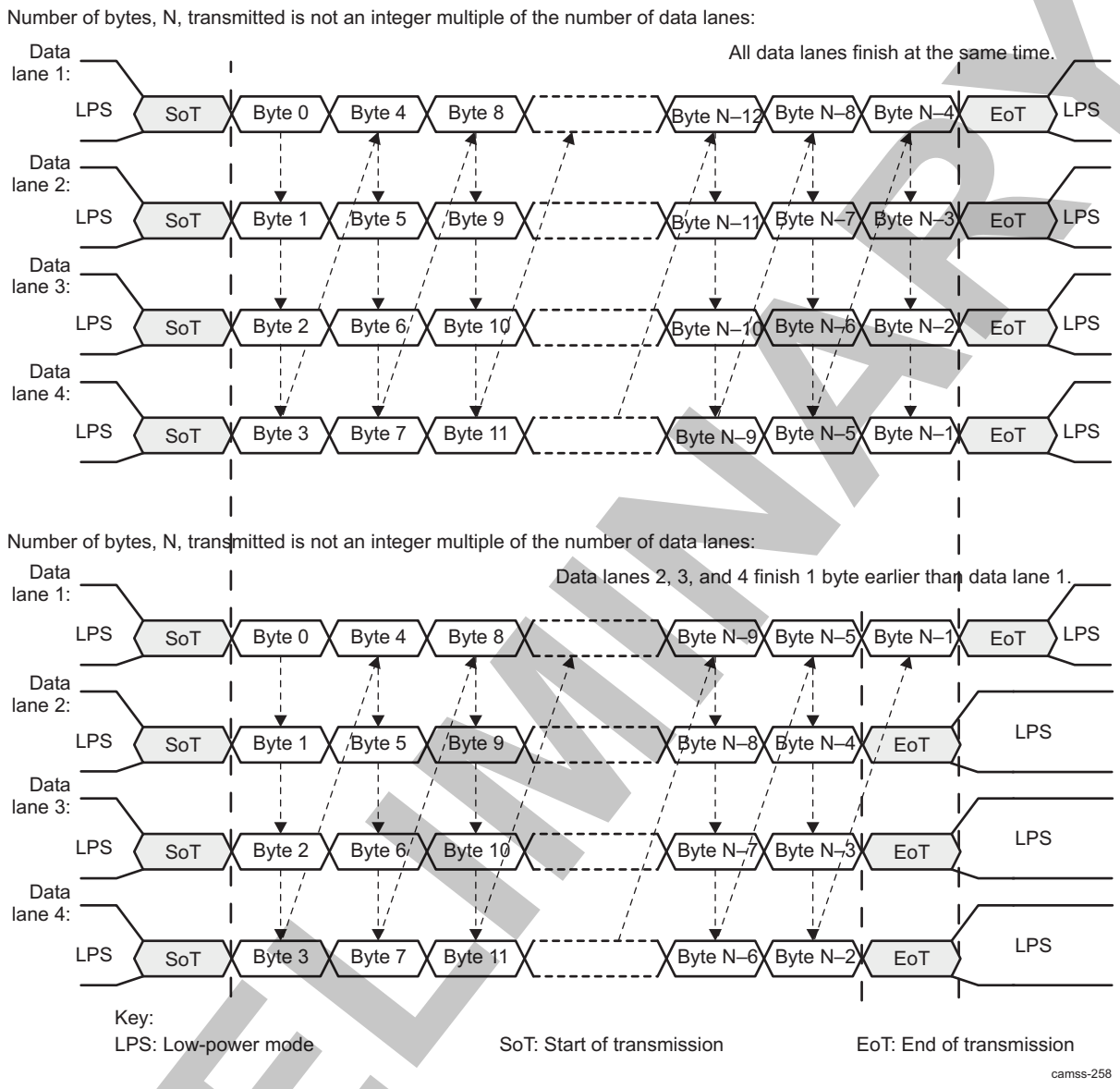
Figure 8-39. ISS CSI2 Four Data-Lane Merger Configuration



8.2.5.1.1.3 ISS CSI2 Protocol Layer

The low-level protocol (LLP) is a byte-oriented protocol from the lane merger layer. It supports short and long packet formats.

The CSI2 protocol layer defines how image-sensor data is transported onto the physical layer.

The feature set of the protocol layer implemented by the CSI2 receiver is:

- Transport of arbitrary data (payload-independent)
- 8-bit word size
- Support for up to four interleaved virtual channels on the same link
- Special packets for frame-start, frame-end, line-start, and line-end information
- Descriptor for the type, pixel depth, and format of application-specific payload data
- Error-correction code (ECC) for 1-bit error correction or 2-bit error detection in the header
- 16-bit checksum code for payload error detection

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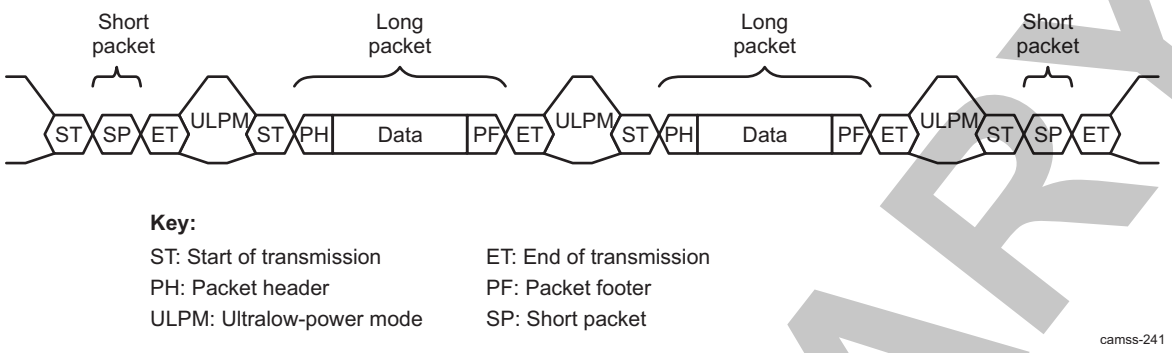
Figure 8-40 shows the CSI2 protocol layer with short and long packets.

Figure 8-40. ISS CSI2 Protocol Layer With Short and Long Packets

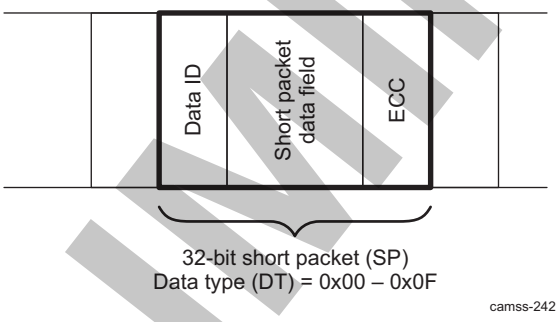


Two packets are always separated from each other with a sequence of ET, ULPM, and ST.

8.2.5.1.1.3.1 ISS CSI2 Short Packet

A short packet is identified by data types 0x00 to 0x0F. A short packet can be used for frame or line synchronization or for generic data. Figure 8-41 shows the structure of a short packet.

Figure 8-41. ISS CSI2 Short Packet Structure



For frame-synchronization data types, the short packet data field is the frame number. For line-synchronization data types, the short packet data field is the line number. For generic short packet data types, the content of the short packet data field is user-defined.

The 16-bit frame number, when used, is always nonzero to distinguish it from the use case where the frame number is inoperative and remains set to 0. The behavior of the 16-bit frame number is one of the following:

- The frame number is always 0 and is inoperative.
- The frame number increments by 1 for every FS packet within the same virtual channel and is periodically reset to 1 (1, 2, 1, 2, 1, 2, 1, 2 or 1, 2, 3, 4, 1, 2, 3, 4).

For LSC and LEC synchronization packets, the short packet data field contains a 16-bit line number. This line number is the same for the LS and LE packets corresponding to a given line. Line numbers are logical line numbers and do not necessarily equal physical line numbers. The 16-bit line number, when used, is always nonzero to distinguish it from the use case where the line number is inoperative and remains set to 0.

The behavior of the 16-bit line number is one of the following:

- The line number is always 0 and is inoperative.
- The line number increments by 1 for every LS packet within the same virtual channel and the same data type. The line number is periodically reset to 1 for the first LS packet after an FS packet. The intended use is for progressive scan (noninterlaced) video data streams. The line number must be a nonzero value.
- The line number increments by the same arbitrary step value greater than 1 for every LS packet within the same virtual channel and the same data type. The line number is periodically reset to a nonzero

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arbitrary start value for the first LS packet after an FS packet. The arbitrary start value can be different between successive frames. The intended use is for interlaced video data streams.

The ECC byte allows single-bit errors to be corrected and 2-bit errors to be detected in the short packet.

Short packets apply to all contexts using the same virtual channel ID (up to eight contexts support eight dedicated configurations of virtual channel ID and data types). The data type associated with the context is not used to distinguish which context is used when receiving short packets.

8.2.5.1.1.3.2 ISS CSI2 Long Packet

A long packet is identified by data types 0x10 to 0x37. A long packet consists of three elements:

- A 32-bit packet header (PH)
- An application-specific data payload with a variable number of 8-bit data words
- A 16-bit packet footer (PF)

The packet header is composed of three elements:

- An 8-bit data identifier
- A 16-bit word count field
- An 8-bit ECC

The packet footer has one element, a 16-bit checksum.

Figure 8-42 and Table 8-151 show the structure of a long packet.

Figure 8-42. ISS CSI2 Long Packet Structure

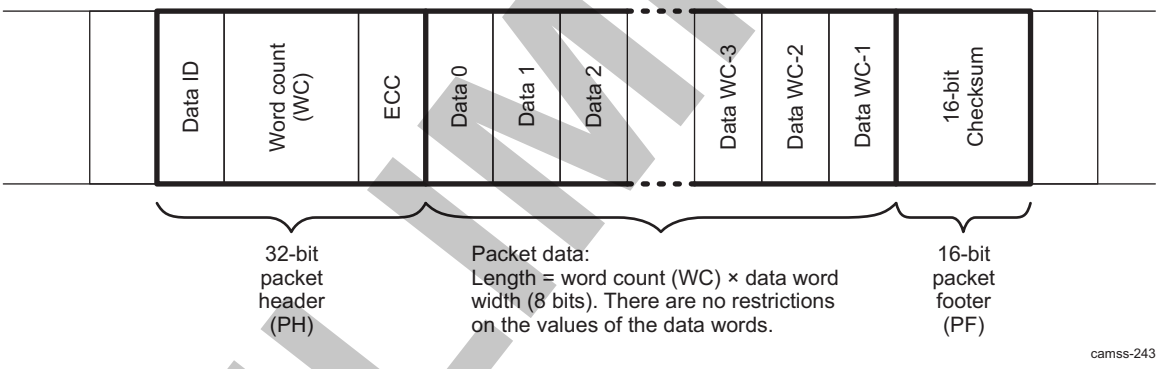

Table 8-151. ISS CSI2 Long Packet Structure Description

Packet Part	Field Name	Size (Bits)	Description
Header	Data ID	8	Contains the virtual channel identifier and the data-type information
	Word count	16	Number of data words in the packet data. A word is 8 bits.
	ECC	8	ECC for data ID and WC field. Allows 1-bit error recovery and 2-bit error detection.
Data	Data	WC-8	Application-specific payload (WC words of 8 bits)
Footer	Checksum	16	16-bit CRC for packet data

There are no restrictions on the size of the packet data, but each data format can impose additional restrictions on the length of the payload data (for example, a multiple of 4 bytes).

8.2.5.1.1.3.3 ISS CSI2 Data Identifier

The data identifier byte contains the virtual channel (VC) value and the data-type (DT) value, as shown in Figure 8-43. The VC value is in the 2 MSBs of the data identifier byte. The DT value is in the 6 LSBs of the data identifier byte.

Figure 8-43 shows the data identifier structure.

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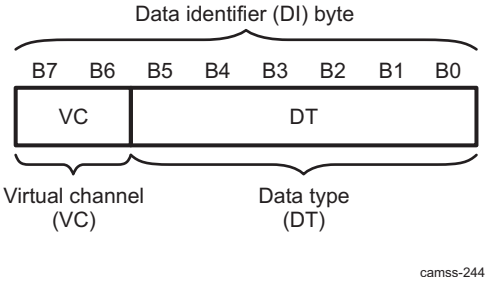
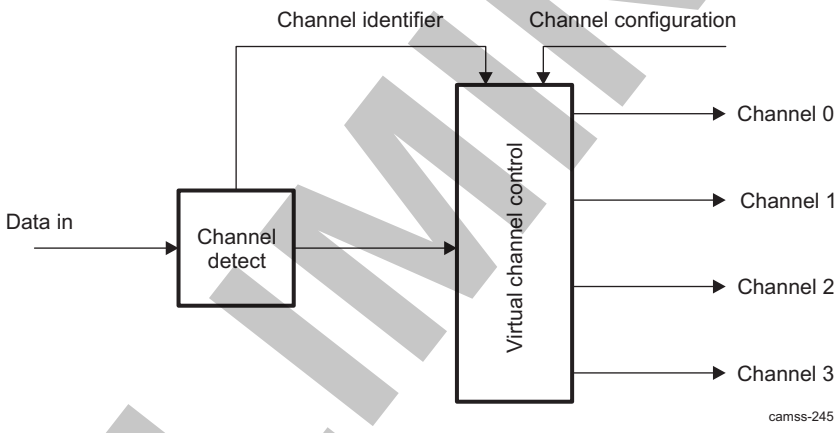
Figure 8-43. ISS CSI2 Data Identifier Structure



Virtual Channel

The CSI2 protocol layer transports virtual channels. Virtual channels are built of frames. A frame can comprise embedded data and image-sensor data. Two contexts are used to send the two types of data separately. Each frame is identified by unique mandatory synchronization codes: frame start and frame end. Line start and line end synchronization codes are optional for the transmitter. A set of registers is associated with each context defined by the virtual channel ID and the data type. Figure 8-44 shows a virtual channel.

Figure 8-44. ISS CSI2 Virtual Channel



Pixel Formats

8.2.5.1.1.3.4 ISS CSI2 Synchronization Codes

Data reception from the image-sensor module uses four synchronization codes embedded in the serial bitstream:

- FSC: Identifies the start of a new frame
- LSC: Identifies the start of a new line; received for every line
- LEC: Identifies the end of a line; received for every line
- FEC: Identifies the end of the last line and the end of the current frame

Table 8-152 summarizes the synchronization code values.

Table 8-152. ISS CSI2 Synchronization Codes

Synchronization Code	Value	Comments
FSC	0x0	Mandatory
FEC	0x1	Mandatory
LSC	0x2	Optional
LEC	0x3	Optional
Reserved	0x4 to 0x7	Not used

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8.2.5.1.1.3.5 ISS CSI2 Generic Short Packet Codes

When the synchronization code value is from 0x8 to 0xF, the short packet is called a generic short packet. Short packets are not processed by the camera interface hardware. A generic short packet is stored in a register without the ECC and an interrupt can be generated. Therefore, generic short packets must be handled by software.

8.2.5.1.1.3.6 ISS CSI2 Generic Long Packet Codes

The code value 0x10 indicates null packets, which can be received at any time. They are discarded by the protocol engine.

The code value 0x11 indicates blanking packets, which can be received at any time. They are discarded by the protocol engine.

The code value 0x12 indicates embedded 8-bit nonimage data typically used for JPEG.

Code values from 0x13 to 0x17 are reserved.

8.2.5.1.1.3.7 ISS CSI2 Frame Structure

Each frame consists of short packets to indicate SOF and EOF. Optional short packets for start of line and end of line can be sent by the image sensor.

Some information before and after the picture data can be sent as SOF and EOF information by the image sensor to the memory through the L3 port.

For each frame, the pixel data (arbitrary data or user-defined byte data) are valid only after an SOF short packet. If the data are invalid, they are discarded by the protocol engine.

A frame contains embedded data and image-sensor data. Figure 8-45 shows where the embedded data and image-sensor data are in the frame. The frame is scanned in raster order starting from the top-left corner, as shown in Figure 8-45 and Figure 8-46. The following definitions for a frame apply:

- Zero or more SOF status lines (SOF lines) can be embedded at the beginning of a CSI2 frame.
- The image embedded data is carried using separate data types and virtual channels (see Section 8.2.4.1.1, *ISS CCP2 Protocol and Data Formats*, and Section 8.2.5.3.3.4, *ISS CSI2 Virtual Channel and Context*).
- Zero or more EOF status lines (EOF lines) can be embedded at the end of a CSI2 frame.
- The SOF lines, pixel data, and EOF lines do not overlap.

The CSI2 receiver does not use the information in the status lines. However, it extracts it and stores it in memory for use by software.

Because the data types are different, the data is carried using separate data types called virtual channels. Those must be mapped to the adequate context. The CSI2 receiver uses a different context for embedded data and image-sensor data. See Section 8.2.5.3.3.4, *ISS CSI2 Virtual Channel and Context*.

Embedded data is supported as a context by the CSI2 receiver; therefore, there is no specific hardware support for embedded data.

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Figure 8-45. ISS CSI2 General Frame Structure (Informative)

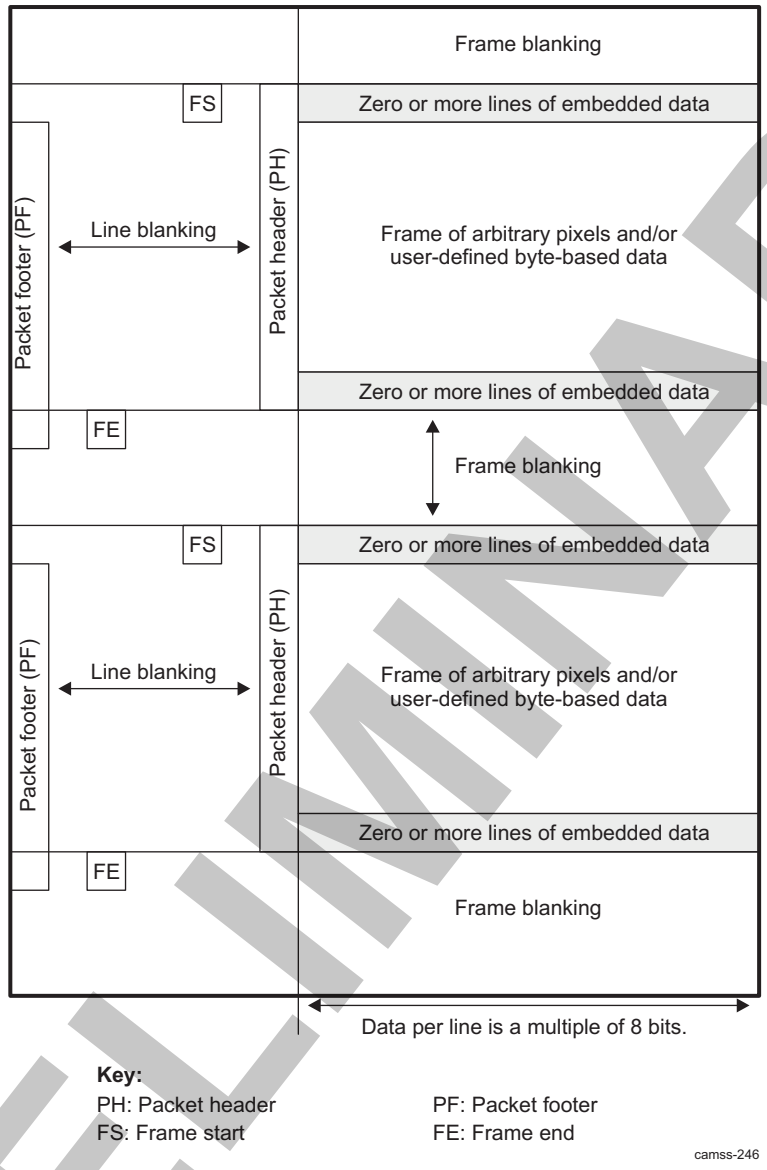

Figure 8-46 shows the frame structure of a YUV4:2:2 interlaced video frame without embedded data.

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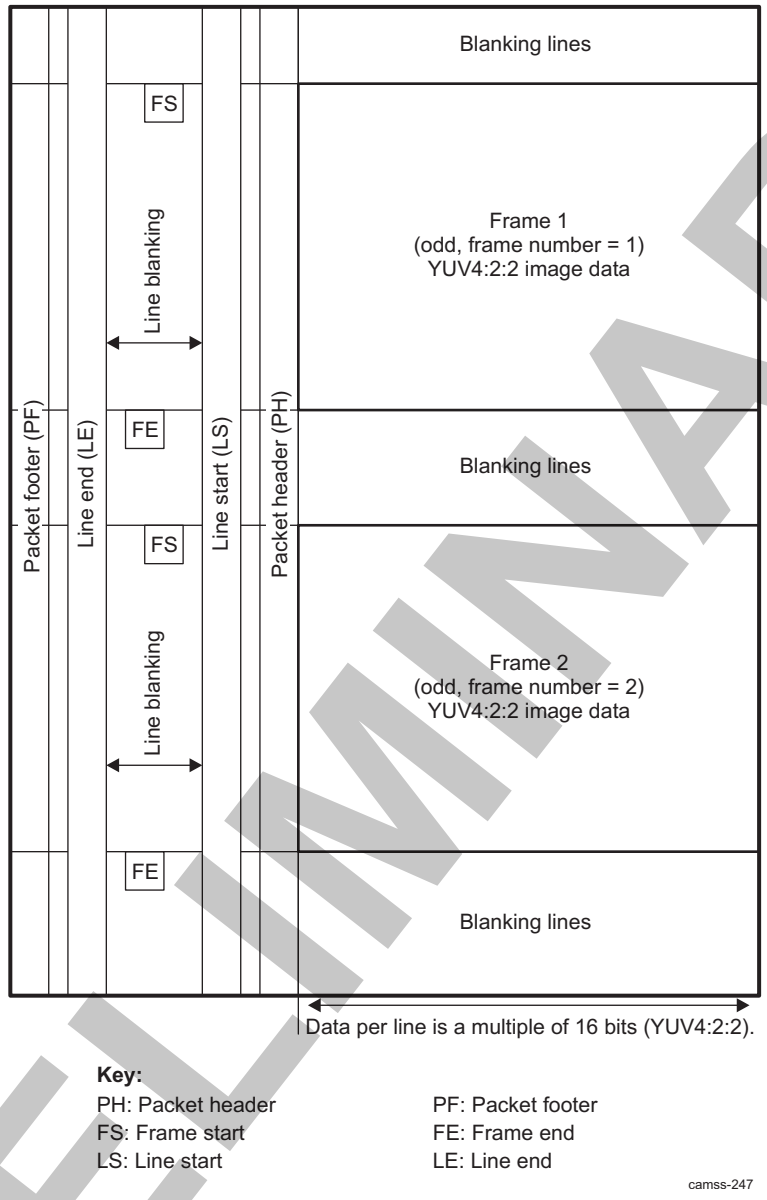
Figure 8-46. ISS CSI2 Digital Interlaced Video Frame (Informative)



The period between the LEC and the new LSC is the line blanking period. The time between the FEC and the new FSC is the frame blanking period. The receiver works with the line blanking period set to 0. The image data is stored in memory by selecting one of the various operating modes. Section 8.2.5.1.1.4, *ISS CSI2 Operating Modes*, explains storing image data frames into memory.

8.2.5.1.1.4 ISS CSI2 Operating Modes

8.2.5.1.1.4.1 ISS CSI2 YUV Operating Modes

8.2.5.1.1.4.1.1 ISS CSI2 YUV4:2:0 8-Bit

YUV4:2:0 8-bit data can be stored to memory in little-endian and big-endian format. To set the endianness for YUV4:2:0 use the CSI2_CTRL[4] ENDIANNESS bit. The line length sent through the CSI2 physical protocol is a multiple of 16 bits for odd lines and 32 bits for even lines.

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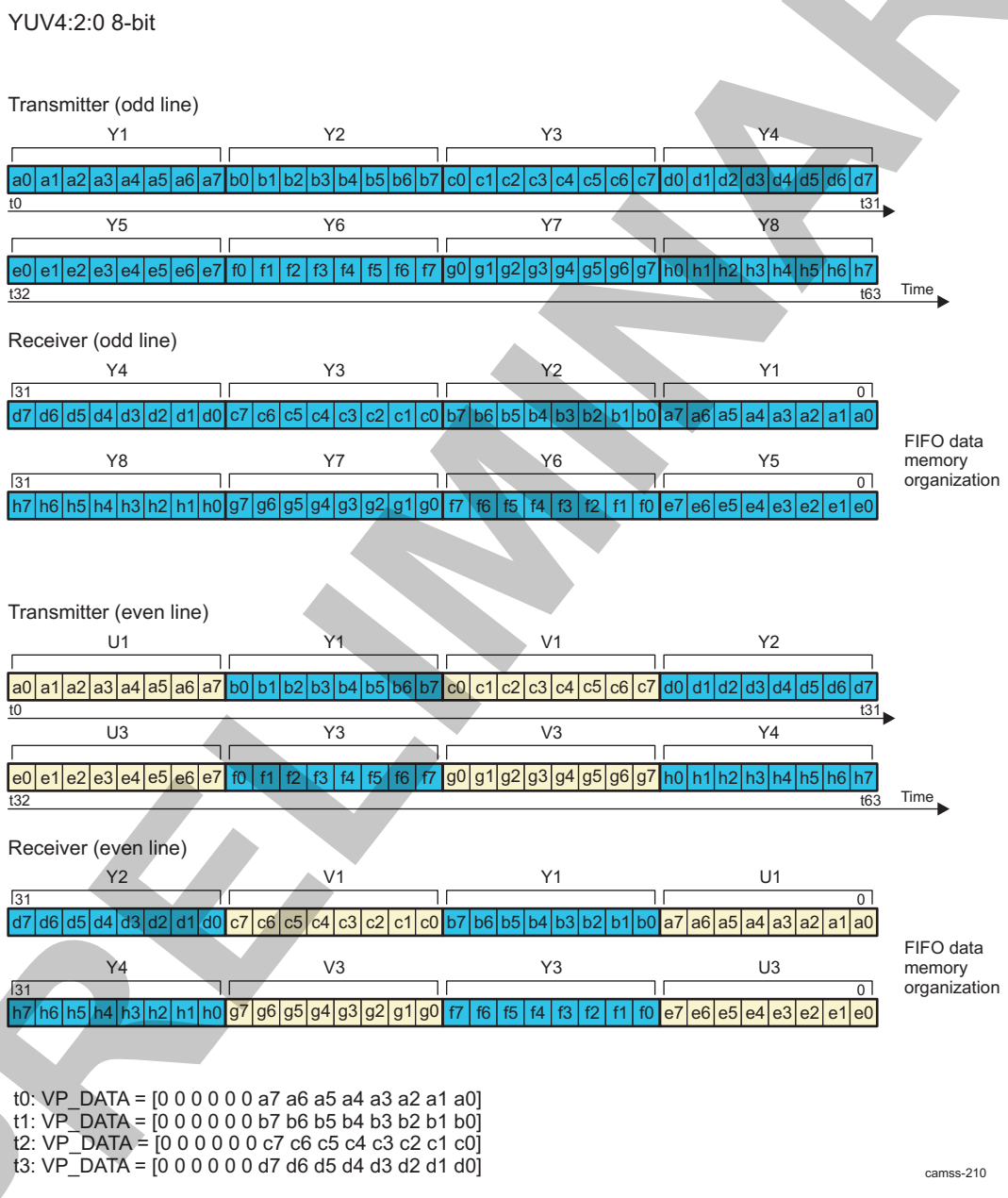
For correct pixel reconstruction, the line length must be a multiple of 32 bits and the number of lines must be even. Figure 8-47 shows the storage format for YUV4:2:0 8-bit data. It is shown as little endian. If the data format is big endian, the figure changes accordingly. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x18 to select YUV4:2:0 8-bit mode. Even and odd lines do not have the same length. Offset must be set accordingly with the CSI2_CTX_DAT_OFST_i[16:5] OFST bit field; for example, if the offset is 0, the data is written in a contiguous way (bit-to-bit of odd and even lines). If the data has an offset, set the destination offset between the first pixel of the previous line and the first pixel of the current line being written to memory.

Figure 8-47. ISS CSI2 YUV4:2:0 8-Bit



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8.2.5.1.1.4.1.2 ISS CSI2 YUV4:2:0 10-Bit

YUV4:2:0 10-bit data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 40 bits for odd lines and 80 bits for even lines. Figure 8-48 shows the storage format for YUV4:2:0 10-bit data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x19 to select YUV4:2:0 10-bit mode. Even and odd lines do not have the same length. Offset must be set accordingly with the CSI2_CTX_DAT_OFST_i[16:5] OFST bit field.

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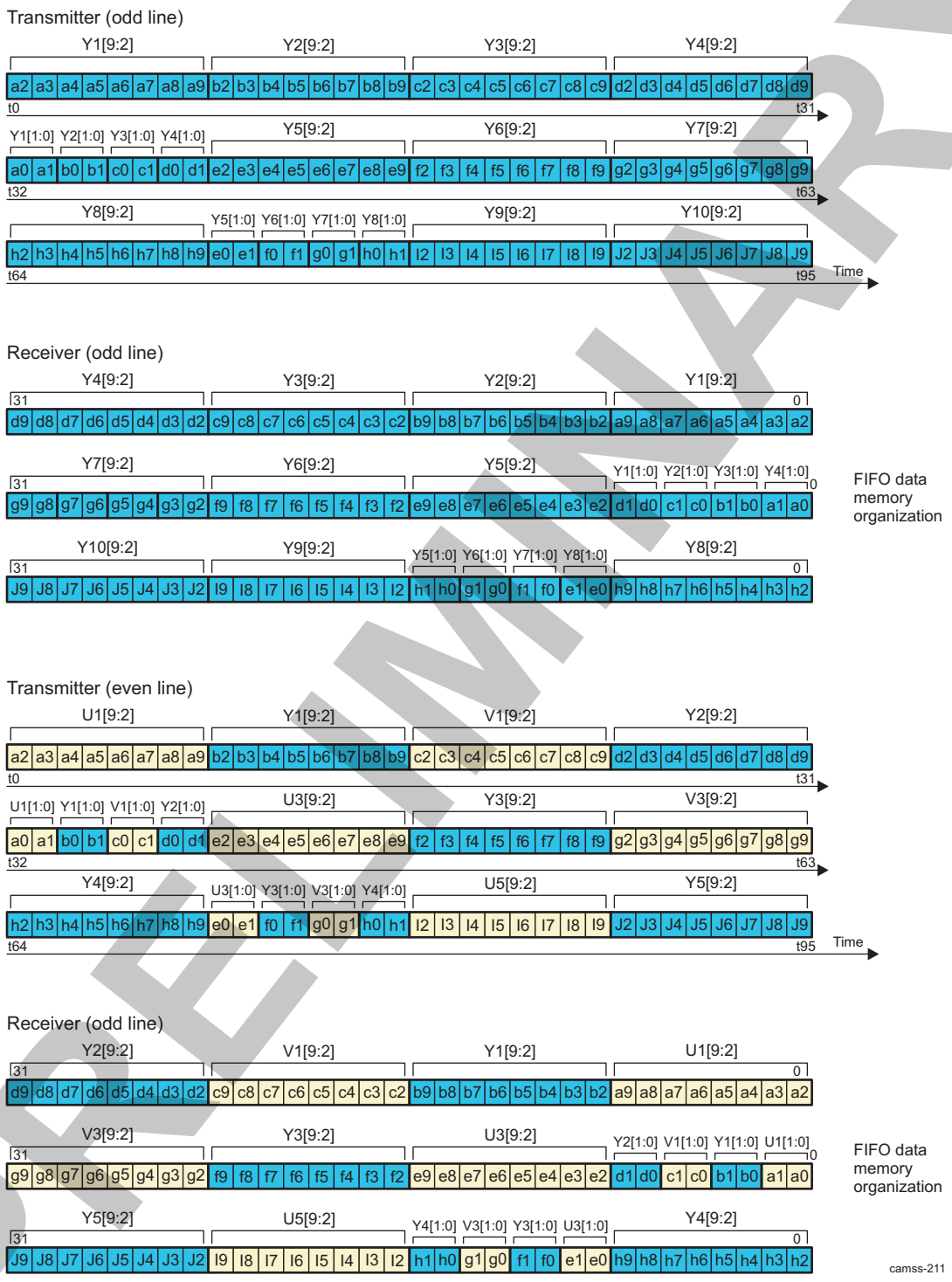
Figure 8-48. ISS CSI2 YUV4:2:0 10-Bit



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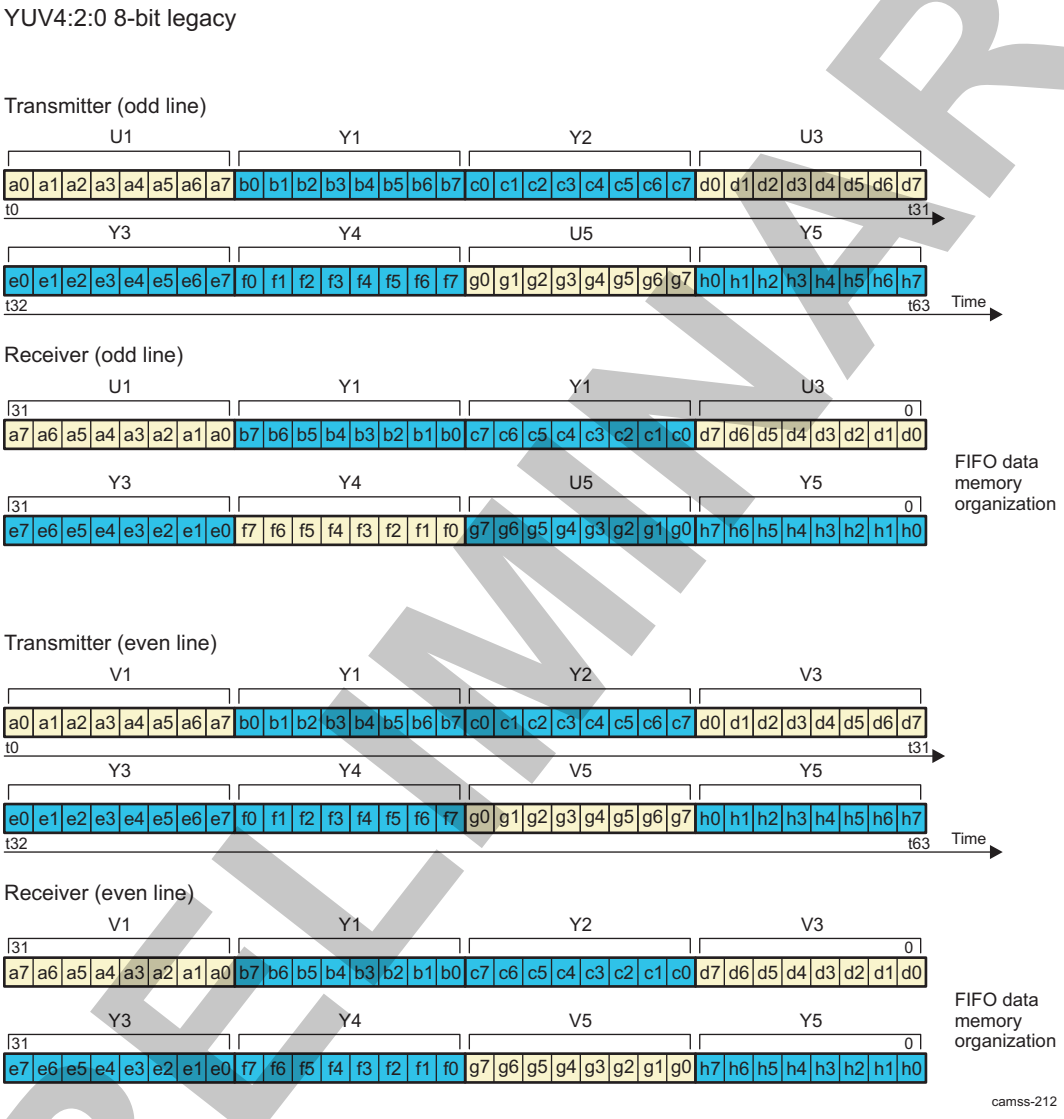
8.2.5.1.1.4.1.3 CSI2 YUV4:2:0 8-Bit Legacy

YUV4:2:0 8-bit legacy data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 4 bytes. Figure 8-49 shows the storage format for YUV4:2:0 8-bit legacy data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1A to select YUV4:2:0 8-bit legacy mode.

Figure 8-49. ISS CSI2 YUV4:2:0 8-Bit Legacy



8.2.5.1.1.4.1.4 ISS CSI2 YUV4:2:0 8-Bit + CSPS

YUV4:2:0 8-bit CSPS data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 16 bits for odd lines and 32 bits for even lines.

For correct pixel reconstruction, the line length must be a multiple of 3 32 bits and the number of lines must be even. Figure 8-50 shows the storage format for YUV4:2:0 8-bit + CSPS data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1C to select YUV4:2:0 8-bit + CSPS mode.

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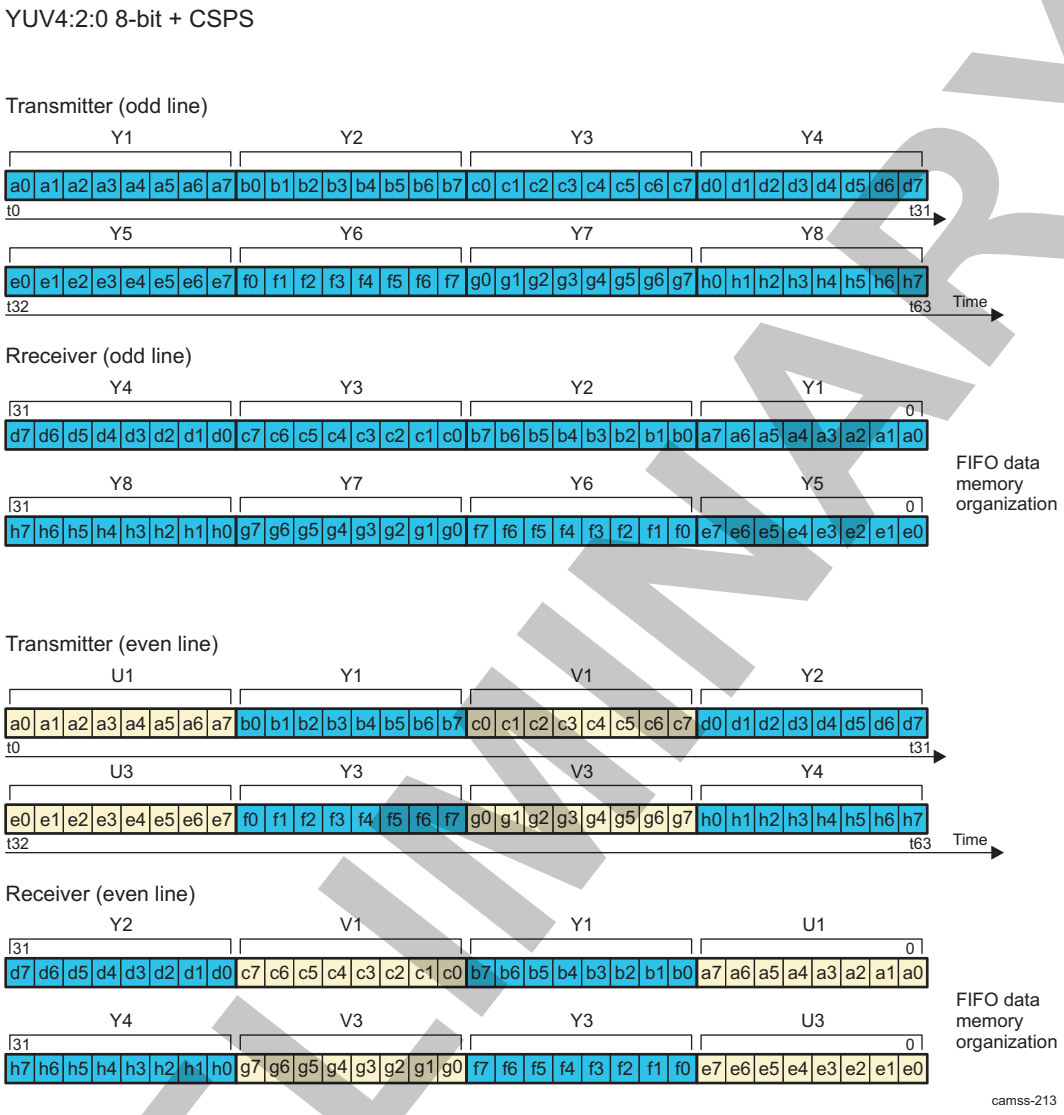
Figure 8-50. ISS CSI2 YUV4:2:0 8-Bit + CSPS



8.2.5.1.1.4.1.5 Camera ISP CSI2 Byte Swap

The CSI2 receiver incorporates a byte-swapping function. Software can optionally enable byte-swapping of the payload data by setting the CSI2_CTx_CTRL1[31] BYTESWAP bit. This feature must be used only when the amount of payload data per packet is a multiple of 16 bits. The byte-swapping is performed before pixel reconstruction.

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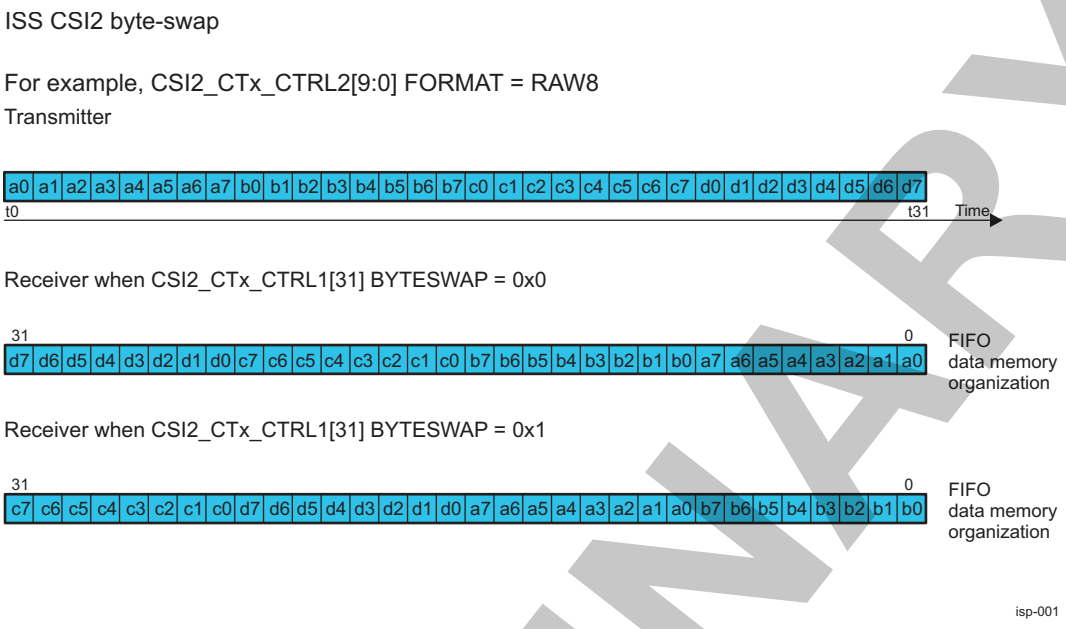
Figure 8-51. Camera ISP CSI2 Byte Swap



8.2.5.1.1.4.1.6 ISS CSI2 YUV4:2:0 10-Bit + CSPS

YUV4:2:0 10-bit CSPS data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 40 bits for odd lines and 80 bits for even lines.

For correct pixel reconstruction, the line length must be a multiple of 3 32 bits and the number of lines must be even. Figure 8-52 shows the storage format for YUV4:2:0 10-bit + CSPS data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1D to select YUV4:2:0 10-bit + CSPS mode.

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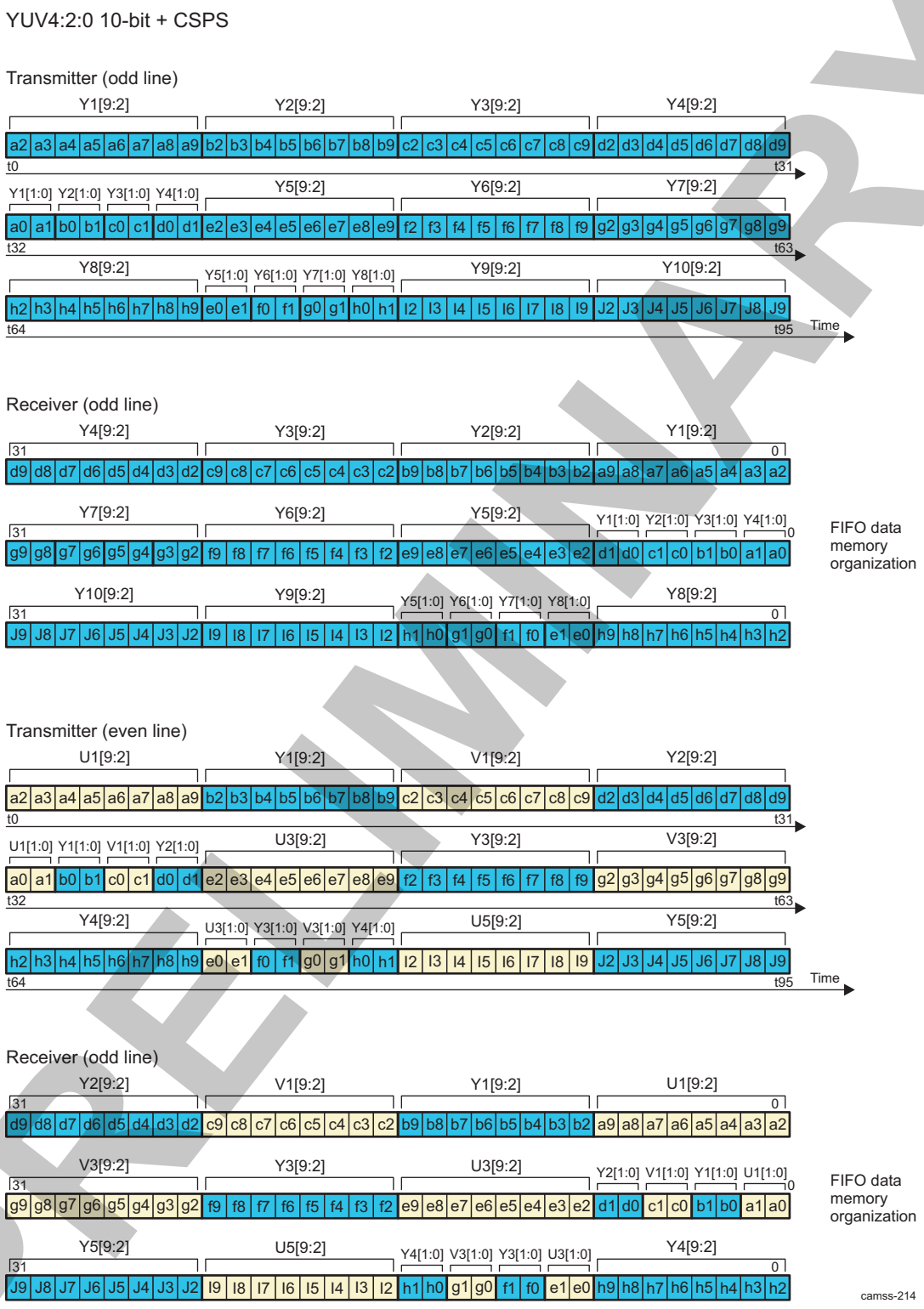
Figure 8-52. ISS CSI2 YUV4:2:0 10-Bit + CSPS



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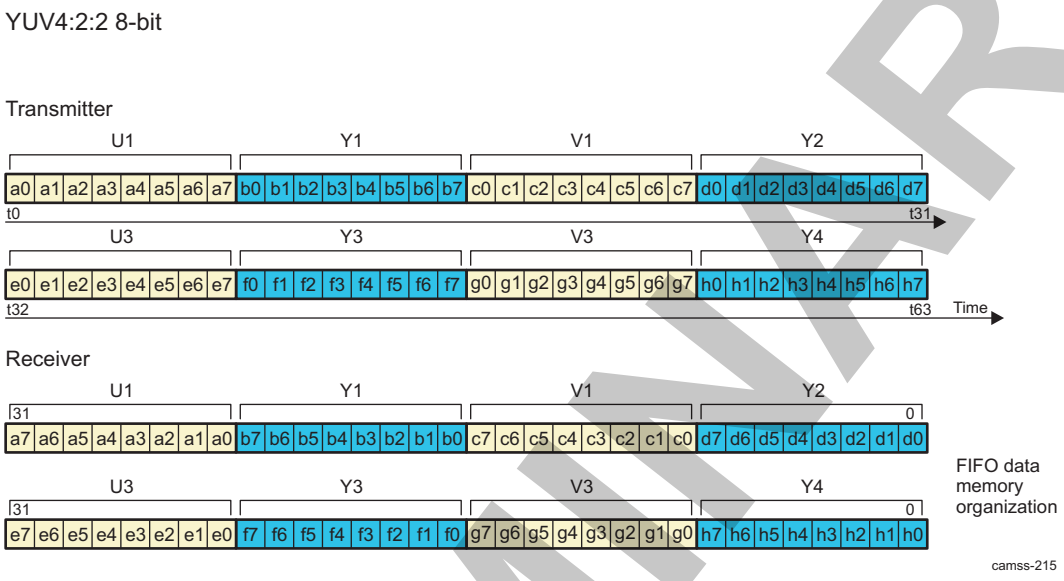
8.2.5.1.1.4.1.7 ISS CSI2 YUV4:2:2 8-Bit

YUV4:2:2 data can be stored to memory in little-endian and big-endian format. To set the endianness for YUV4:2:2 use the CSI2_CTRL[4] ENDIANNESS bit. The line length sent through the CSI2 physical protocol is a multiple of 32 bits. Figure 8-53 shows the storage format for YUV4:2:2 8-bit data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1E to select YUV4:2:2 8-bit mode.

Figure 8-53. ISS CSI2 YUV4:2:2 8-Bit



8.2.5.1.1.4.1.8 CSI2 YUV4:2:2 10-Bit

YUV4:2:2 data can be stored to memory in little-endian and big-endian format. The line length sent through the CSI2 physical protocol is a multiple of 40 bits. Figure 8-54 shows the storage format for YUV4:2:2 10-bit data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x1F to select YUV4:2:2 10-bit mode.

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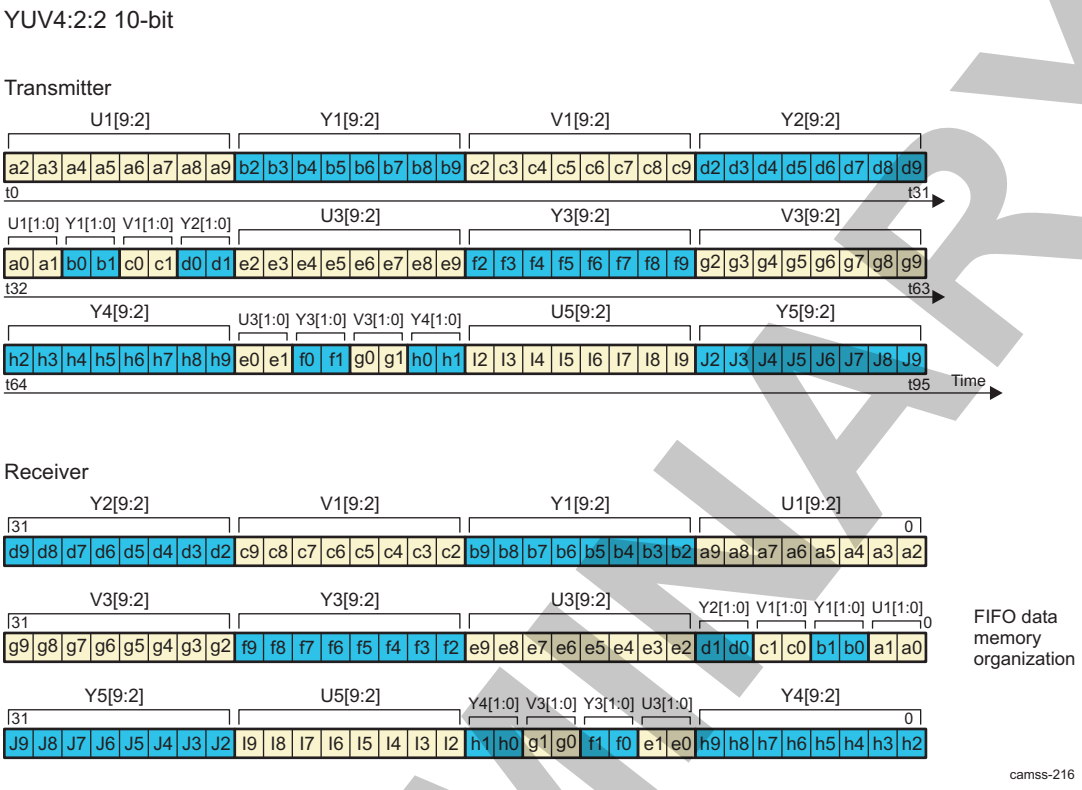
Figure 8-54. ISS CSI2 YUV4:2:2 10-Bit



8.2.5.1.1.4.2 ISS CSI2 RGB Operating Modes

8.2.5.1.1.4.2.1 ISS CSI2 RGB565

RGB565 data is output to memory without data expansion. The line length sent through the CSI2 physical layer is always a multiple of 16 bits. Figure 8-55 shows the storage format for RGB565 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x22 to select RGB565 mode.

Figure 8-55. ISS CSI2 RGB565

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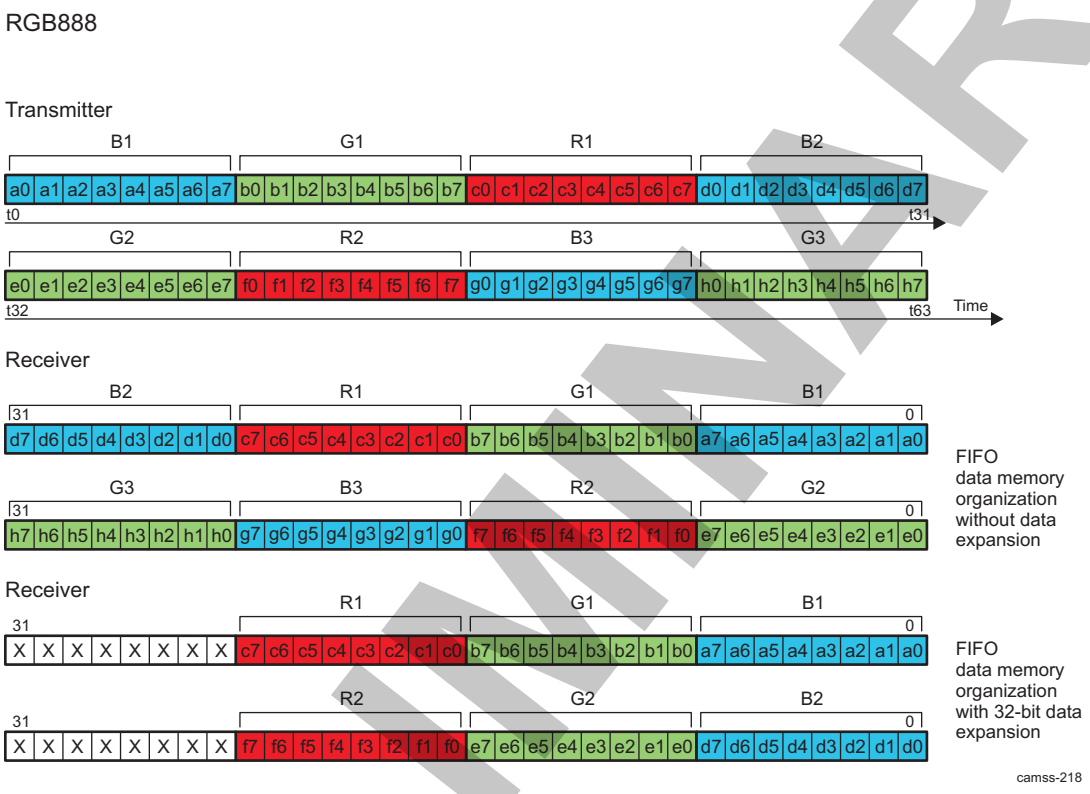
8.2.5.1.1.4.2.2 ISS CSI2 RGB888

RGB888 data can be output to memory in two formats: with or without data expansion. If data expansion is used, the value of the 8 upper bits is programmable and can be set with an alpha value for computer graphics applications (the CSI2_CTX_CTRL3_i[29:16] ALPHA bit field). Figure 8-56 shows the storage format for RGB888 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x24 to select RGB888 mode.

Figure 8-56. ISS CSI2 RGB888



8.2.5.1.1.4.2.3 ISS CSI2 RGB666

RGB666 data is always output to memory with data expansion. The value of the 14 upper bits is programmable and can be set with an alpha value for computer graphics applications (the CSI2_CTX_CTRL3_i[29:16] ALPHA bit field). The line length sent through the CSI2 physical protocol is a multiple of 8 bits. Furthermore, the line length is a multiple of 9 × 8 bits to finish the pixel reconstruction correctly. Figure 8-57 shows the storage format for RGB666 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0x33 to select RGB666 mode.

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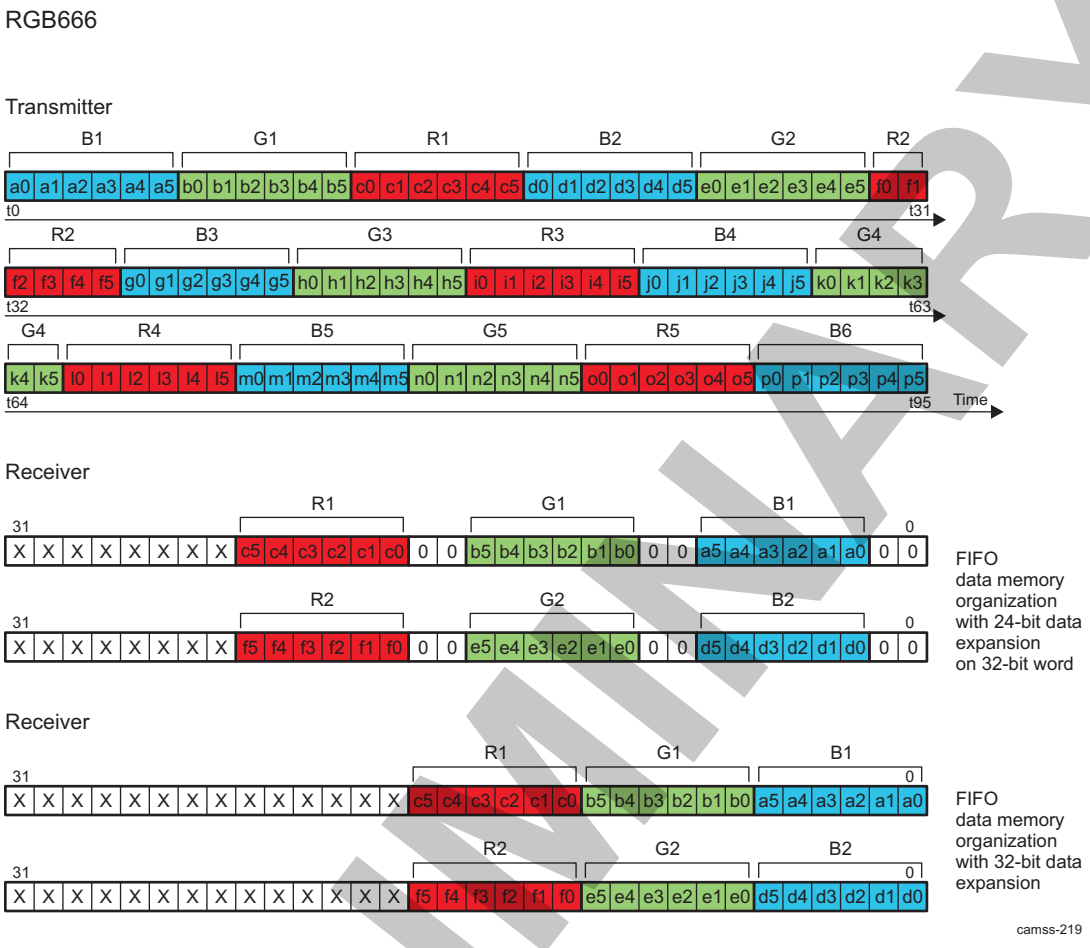
Figure 8-57. ISS CSI2 RGB666



8.2.5.1.1.4.2.4 ISS CSI2 RGB444

RGB444 data is output to memory with data expansion. When data expansion is used, the value of the 4 upper bits is programmable and can be set with an alpha value for computer graphics applications (the CSI2_CTX_CTRL3_i[29:16] ALPHA bit field). Figure 8-58 shows the storage format for RGB444 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0xA0 to select RGB444 mode.

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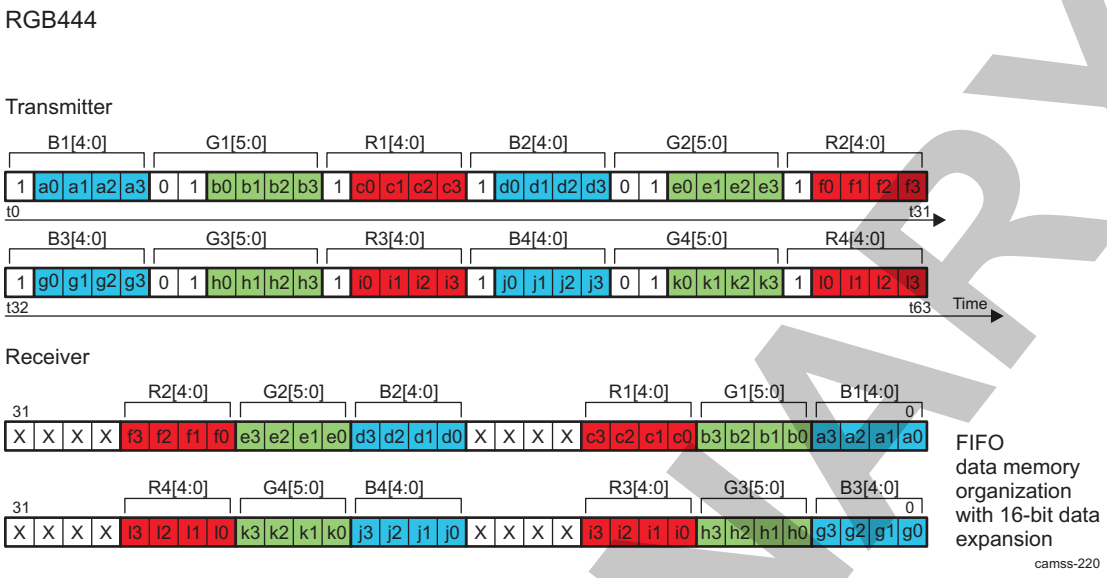
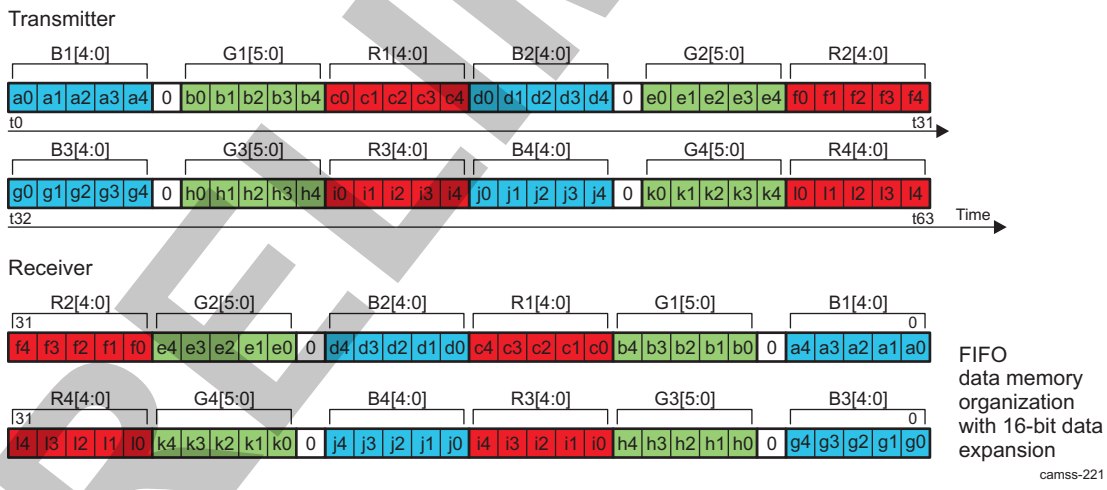
Figure 8-58. ISS CSI2 RGB444



8.2.5.1.1.4.2.5 ISS CSI2 RGB555

RGB555 data is output to memory with data expansion. Figure 8-59 shows the storage format for RGB555 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field to 0xA1 to select RGB555 mode.

Figure 8-59. ISS CSI2 RGB555



8.2.5.1.1.4.3 ISS CSI2 RAW Bayer RGB Operating Modes

8.2.5.1.1.4.3.1 ISS CSI2 RAW6

RAW6 data can be output to memory with or without data expansion. The line length sent through the CSI2 physical layer is a multiple of 8 bits (6-bit image data + 2-bit expansion). Furthermore, the line length is a multiple of 3 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 6 is 24, so 3 × 8 bits). Figure 8-60 shows the storage format for RAW6 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x28 to select RAW6 mode

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- To 0x68 for RAW6 + 8-bit expansion
- To 0xE8 for RAW6 + DPCM decompression to 10-bit to video port
- To 0x2A8 for RAW6 + DPCM decompression to 10-bit expanded to 16-bit
- To 0x3A8 for RAW6 + DPCM decompression to 12-bit expanded to 16-bit
- To 0x368 for RAW6 + DPCM decompression to 12-bit to video port

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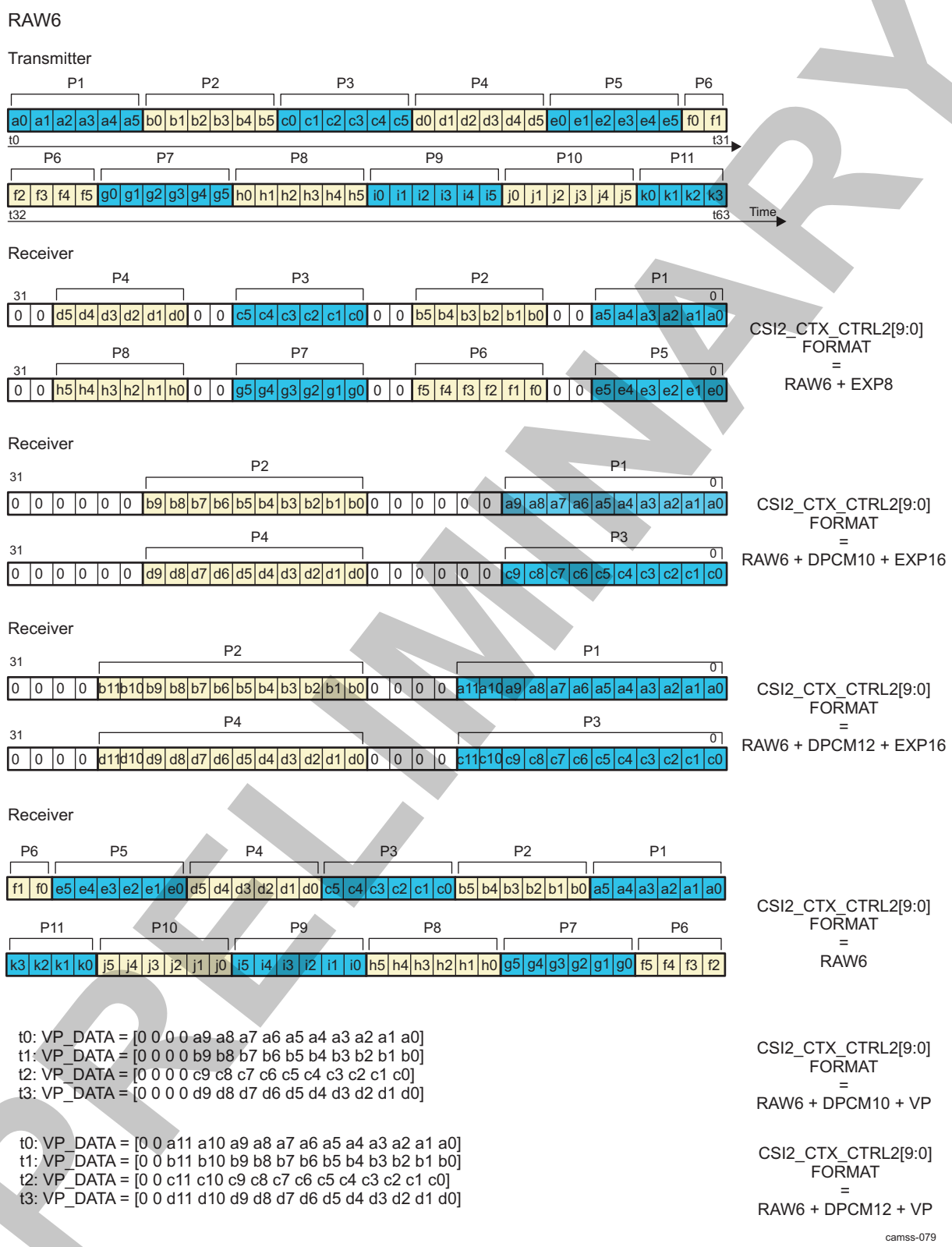
Figure 8-60. ISS CSI2 RAW6



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8.2.5.1.1.4.3.2 ISS CSI2 RAW7

RAW7 data can be output to memory with or without data expansion. The line length sent through the CSI2 physical layer is a multiple of 8 bits. Furthermore, the line length is a multiple of 7 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 7 is 56, so 7 × 8 bits). Figure 8-61 shows the storage format for RAW7 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x29 to select RAW7 mode
- To 0x69 for RAW7 + 8-bit expansion
- To 0x329 for RAW7 + DPCM decompression to 10-bit to video port
- To 0x229 for RAW7 + DPCM decompression to 10-bit expanded to 16-bit
- To 0x369 for RAW7 + DPCM decompression to 12-bit expanded to 16-bit
- To 0x3A9 for RAW7 + DPCM decompression to 12-bit to video port

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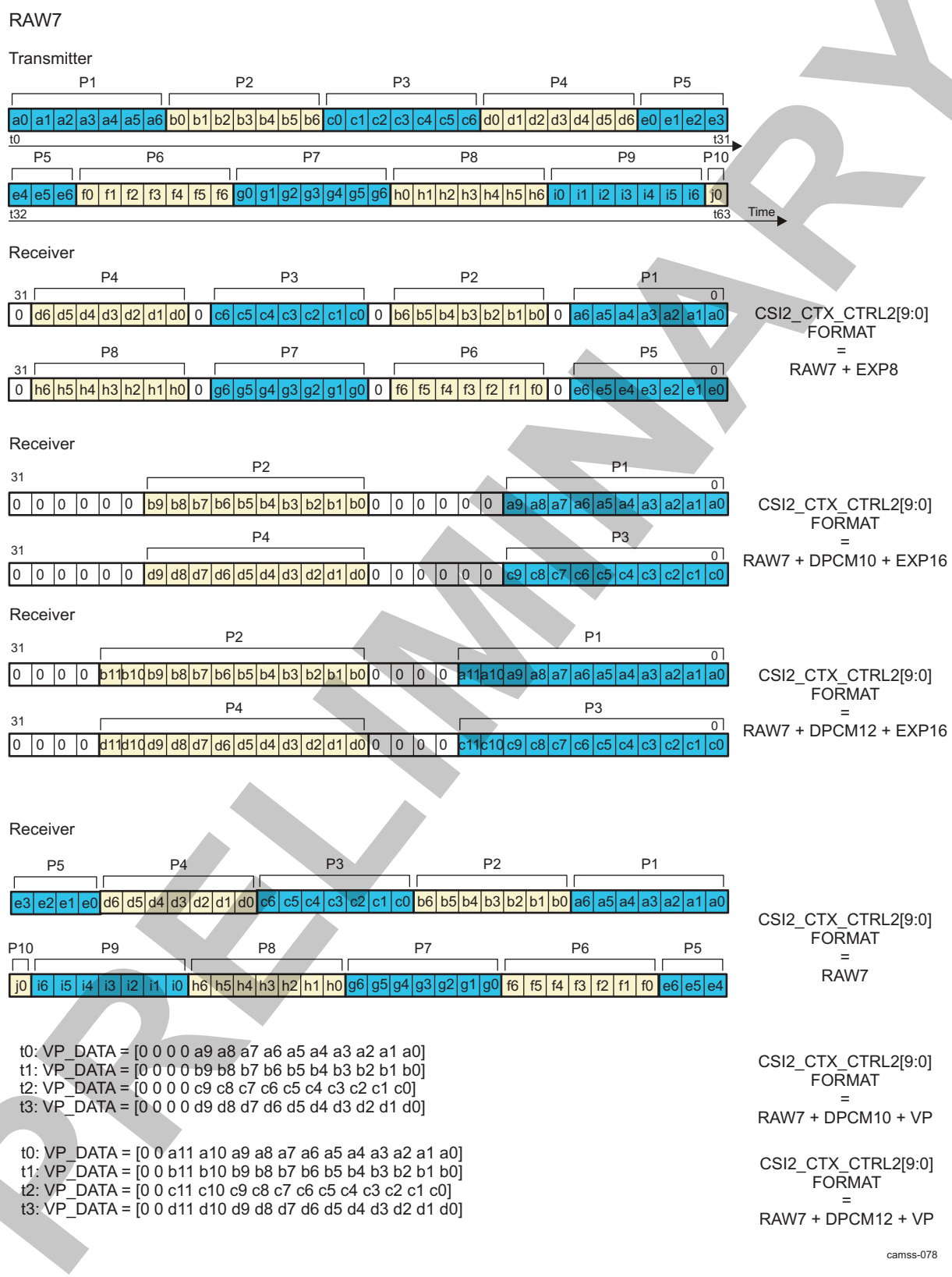
Figure 8-61. ISS CSI2 RAW7



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8.2.5.1.1.4.3.3 ISS CSI2 RAW8

RAW8 data can be output to memory with or without data expansion. The line length sent through the CSI2 physical layer is always a multiple of 8 bits. Figure 8-62 shows the storage format for RAW8 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x2A to select RAW8 mode
- To 0x12A for RAW8 to video port
- To 0x32A for RAW8 + DPCM decompression to 10-bit to video port
- To 0x2AA for RAW8 + DPCM decompression to 10-bit expanded to 16-bit
- To 0x36A for RAW8 + DPCM decompression to 12-bit expanded to 16-bit
- To 0x3AA for RAW8 + DPCM decompression to 12-bit to video port

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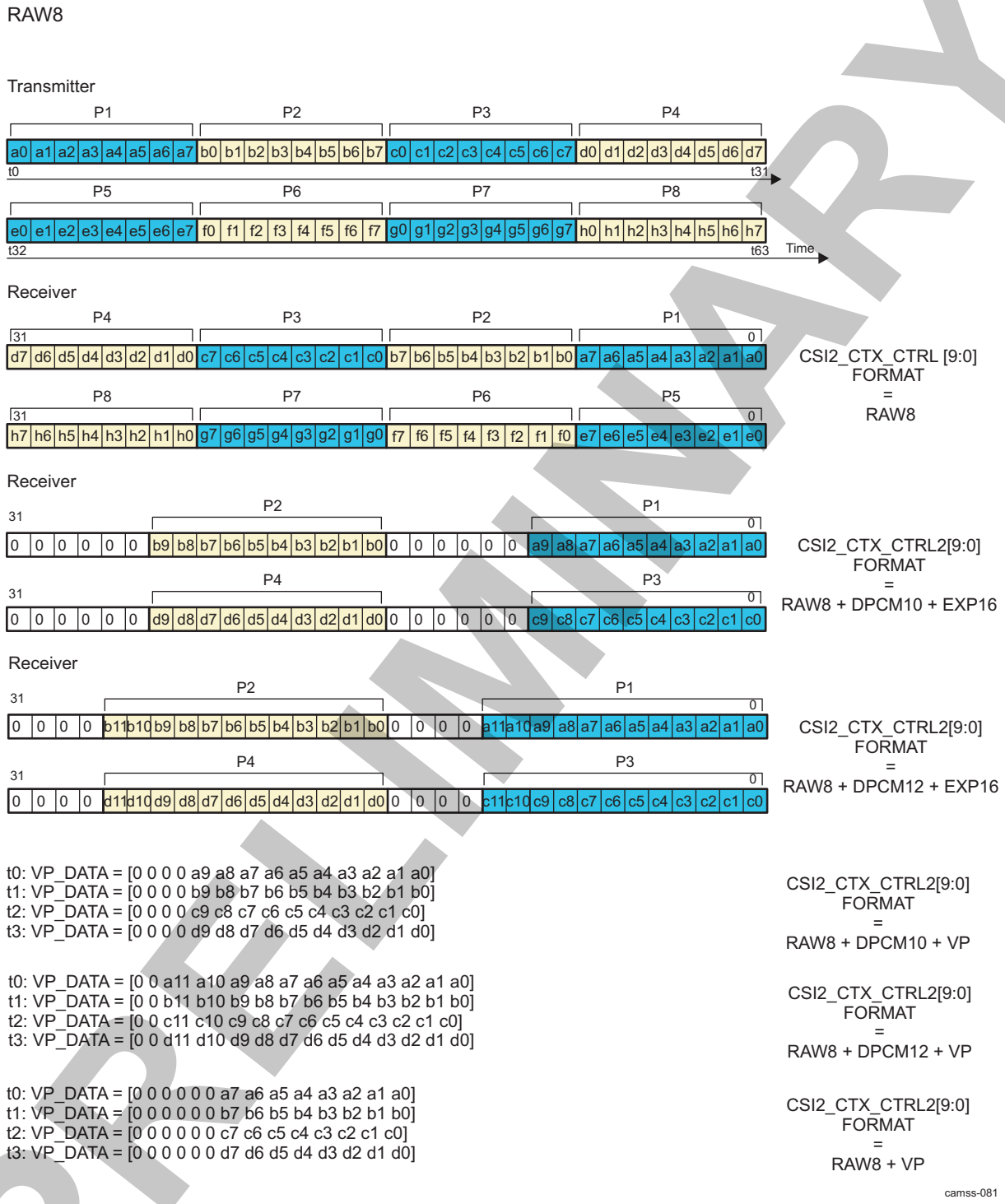
Figure 8-62. ISS CSI2 RAW8



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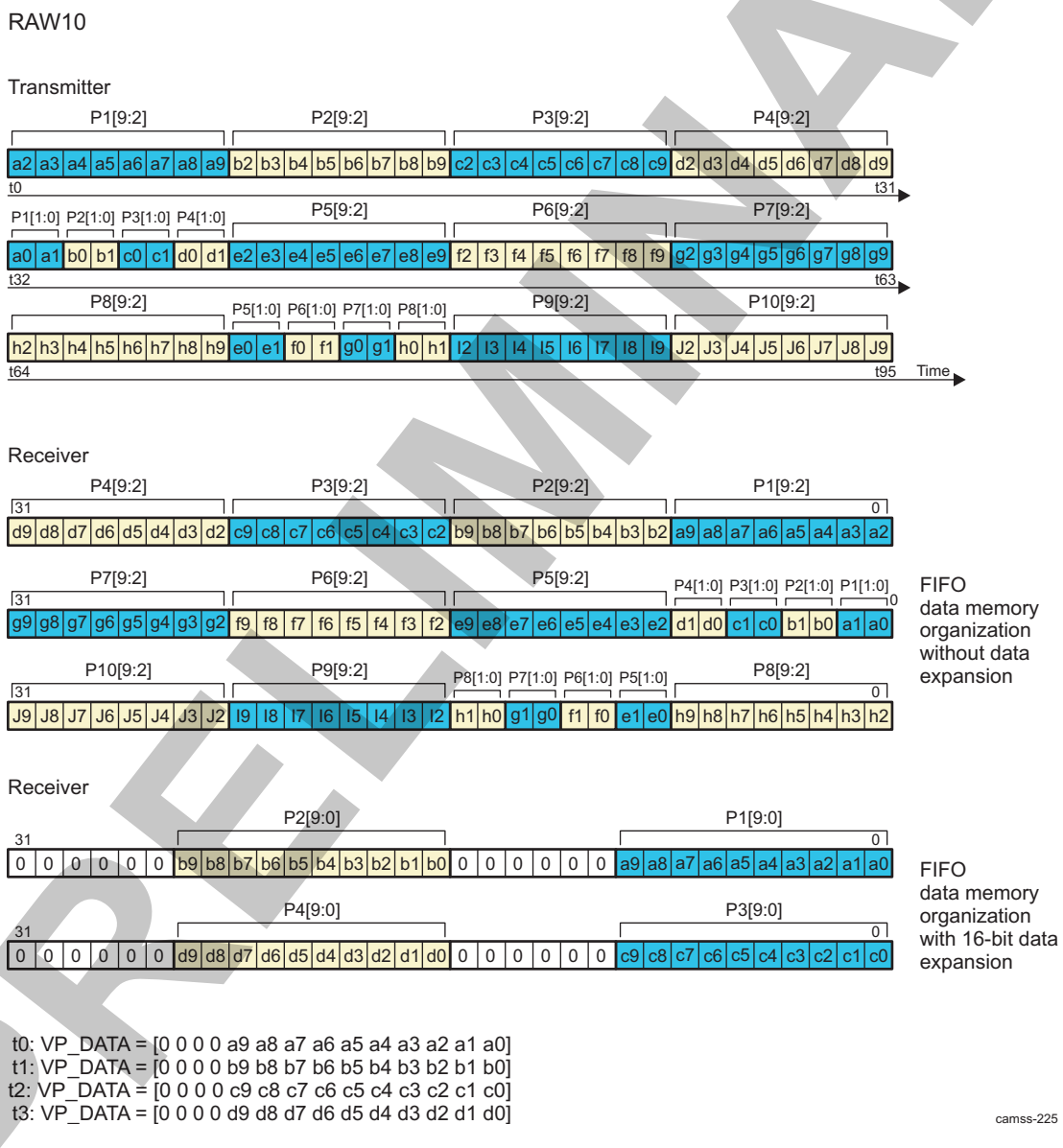
8.2.5.1.1.4.3.4 ISS CSI2 RAW10

RAW10 data can be output memory in two formats: with or without data expansion. It can also be sent to the video port. If data expansion is used, the 10-bit data are padded with 0s on a 16-bit word. The line length sent through the CSI2 physical layer is a multiple of 8 bits. Furthermore, the line length is a multiple of 5 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 10 is 40, so 5 × 8 bits). Figure 8-63 shows the storage format for RAW10 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x2B to select RAW10 mode
- To 0xAB for RAW10 + 16-bit expansion
- To 0x12F for RAW10 to video port

Figure 8-63. ISS CSI2 RAW10



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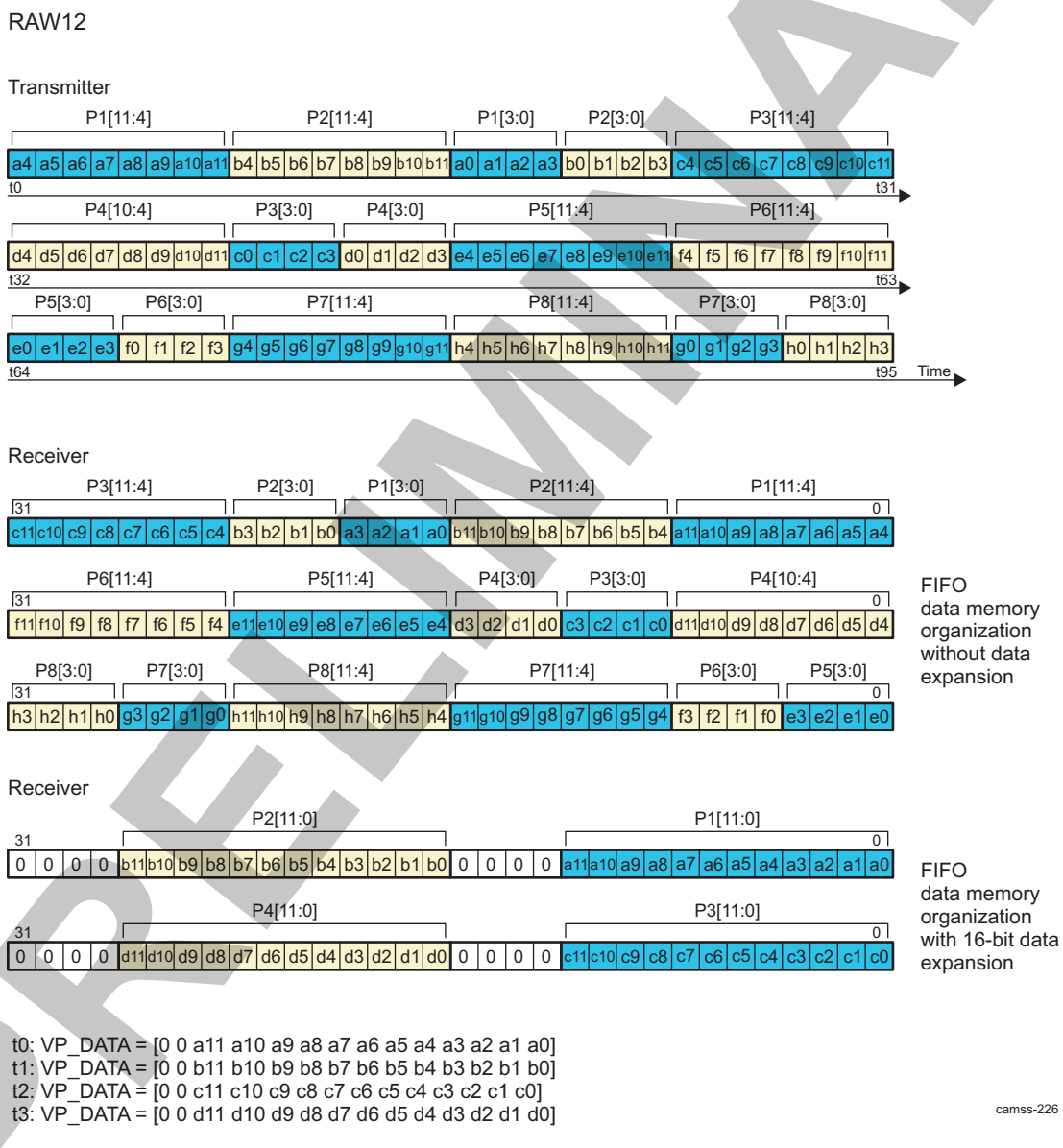
8.2.5.1.1.4.3.5 ISS CSI2 RAW12

RAW12 data can be output to memory in two formats: with or without data expansion. It can also be sent to the video port. If data expansion is used, the 12-bit data are padded with 0s on a 16-bit word. The line length sent through the CSI2 physical layer is a multiple of 8 bits. Furthermore, the line length is a multiple of 3 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 12 is 24, so 3 × 8 bits). Figure 8-64 shows the storage format for RAW12 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x2C to select RAW12 mode
- To 0xAC for RAW12 + 16-bit expansion
- To 0x12C for RAW12 to video port

Figure 8-64. ISS CSI2 RAW12



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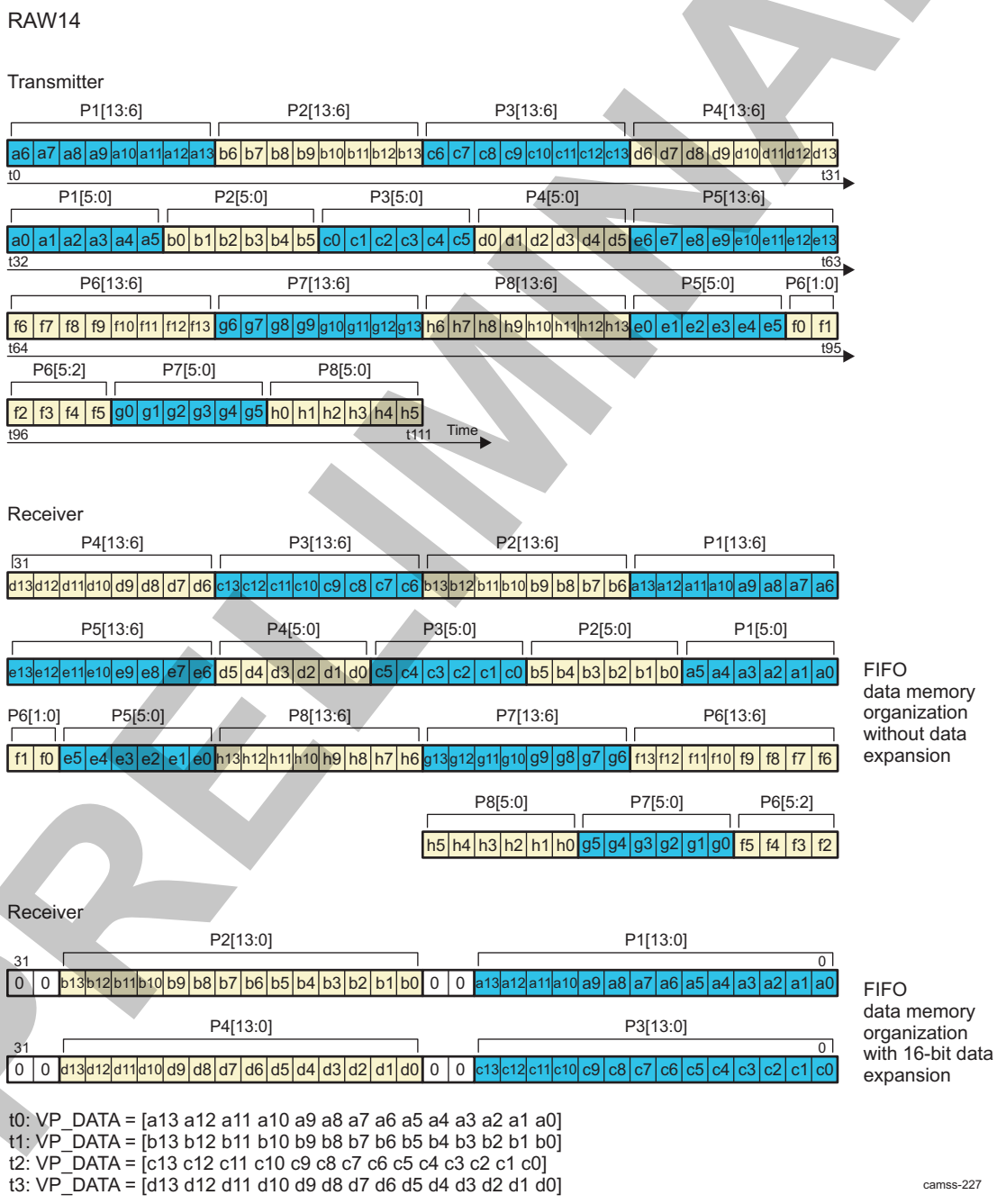
8.2.5.1.1.4.3.6 ISS CSI2 RAW14

RAW14 data can be output to memory in two formats: with or without data expansion. It can also be sent to the video port. If data expansion is used, the 14-bit data are padded with 0s on a 16-bit word. The line length sent through the CSI2 physical layer is a multiple of 8 bits. Furthermore, the line length is a multiple of 7 × 8 bits to complete the pixel reconstruction correctly (the lowest common multiple of 8 and 14 is 56, so 7 × 8 bits). Figure 8-65 shows the storage format for RAW14 data. Set the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field as follows:

- To 0x2D to select RAW14 mode
- To 0xAD for RAW14 + 16-bit expansion
- To 0x12D for RAW12 to video port

Figure 8-65. ISS CSI2 RAW14



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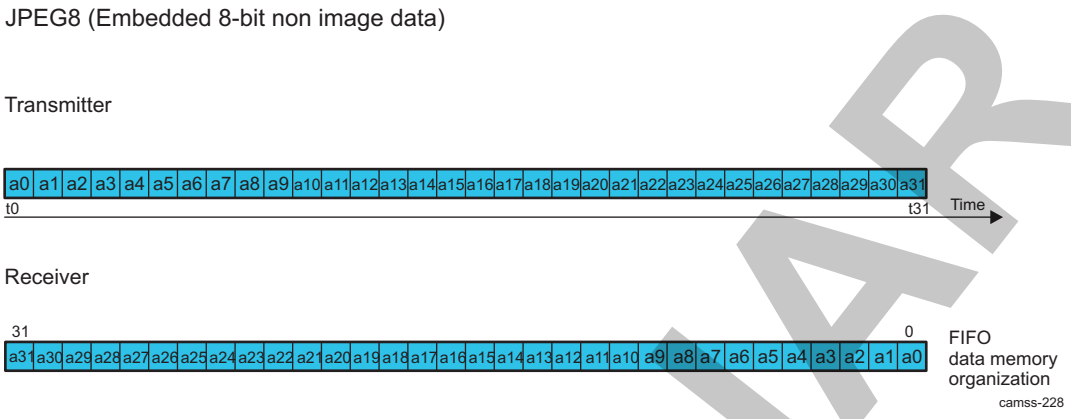
8.2.5.1.1.4.4 ISS CSI2 JPEG8 Operating Modes

The size of a compressed stream can be known in advance. Figure 8-66 shows the format for storing JPEG8 data.

Figure 8-66. ISS CSI2 JPEG8

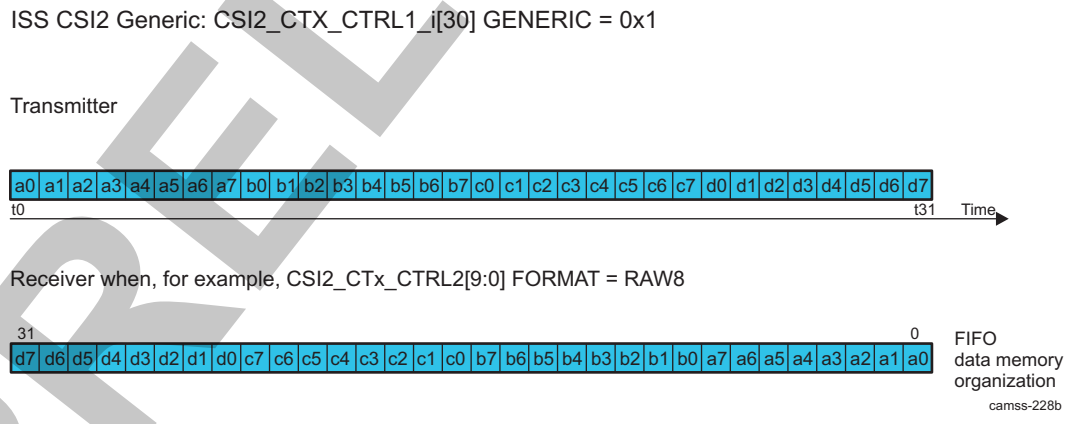


8.2.5.1.1.4.5 ISS CSI2 Generic Format

The CSI2 receiver supports a generic format to send data to memory and/or the video port. The generic mode is entered by setting the CSI2_CTX_CTRL1_i[30] GENERIC bit. The CSI2_CTX_CTRL2_i[9:0] FORMAT bit field defines how the data stream is decoded. When generic mode is enabled (GENERIC = 1), the MIPI data type code is ignored and data is decoded using the FORMAT bit. Whatever the MIPI data type code, it is ignored (the data stream is processed even if the FORMAT bit does not match the MIPI data type code.) When generic mode is not used (GENERIC = 0), the data stream is processed only when the MIPI data type code matches the FORMAT setting of the enabled context. If not matched, the data stream is not processed by the CSI2 engine. Only the virtual channel information is used to map a received data stream to a context. Software must ensure that a MIPI virtual channel used in generic mode is mapped only to a single context.

Figure 8-67 shows the ISS CSI2 generic format.

Figure 8-67. ISS CSI2 Generic Format



8.2.5.1.1.4.6 ISS CSI2 MIPI Format Supported Summary

Table 8-153 summarizes the CSI2 MIPI-supported formats and their output category. By setting the CSI2_CTX_CTRL2_i register format, the CSI2 outputs certain types of pixel packet data.

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Table 8-153. ISS CSI2 MIPI Format Supported by the Protocol Engine

MIPI			CSI2 Protocol Engine Support
Category	**Abbreviation**	**Register Setting Format Description**	**Configuration Value for CSI2_CTX_CTRL2_i[9:0] FORMAT**
Sync short packet data types[1]	Short packet sync code	Mandatory FSC	0x000
	Short packet sync code	Mandatory FEC	0x001
	Short packet sync code	Optional LSC	0x002
	Short packet sync code	Optional LEC	0x003
			0x004
			0x005
			0x006
			0x007
Generic short packet data types[1]	Short packet	32-bit without ECC is stored in a register with code value 0x008.	0x008
	Short packet	32-bit without ECC is stored in a register with code value 0x009.	0x009
	Short packet	32-bit without ECC is stored in a register with code value 0x00A.	0x00A
	Short packet	32-bit without ECC is stored in a register with code value 0x00B.	0x00B
	Short packet	32-bit without ECC is stored in a register with code value 0x00C.	0x00C
	Short packet	32-bit without ECC is stored in a register with code value 0x00D.	0x00D
	Short packet	32-bit without ECC is stored in a register with code value 0x00E.	0x00E
	Short packet	32-bit without ECC is stored in a register with code value 0x00.	0x00F
Generic Long packet data types[2]	Null	Discarded	0x010
	Blanking data	Discarded	0x011
	Embedded 8-bit nonimage data (for example, JPEG)	0x12: Embedded 8-bit nonimage data (for example, JPEG)	0x012
		Send to memory when FORMAT = 0	0x013
		Send to memory when FORMAT = 0	0x014
		Send to memory when FORMAT = 0	0x015
		Send to memory when FORMAT = 0	0x016
		Send to memory when FORMAT = 0	0x017
YUV data	YUV4:2:0 8-bit	YUV4:2:0 8-bit	0x018
	YUV4:2:0 10-bit	YUV4:2:0 10-bit	0x019
	YUV4:2:0 8-bit legacy	YUV4:2:0 8-bit legacy	0x01A
	Reserved	Send to memory when FORMAT = 0	0x01B
	YUV4:2:0 8-bit + CSPS	YUV4:2:0 8 bit + CSPS	0x01C
	YUV4:2:0 10-bit + CSPS	YUV4:2:0 10 bit + CSPS	0x01D
	YUV4:2:2 8-bit	YUV4:2:2 8-bit	0x01E
		YUV4:2:2 8-bit + VP	0x09E

(1) To understand ISS synchronization codes and short packets, see Section 8.2.5.3.3.3, *ISS CSI2 Short Packet*.
(2) To understand ISS synchronization codes and long packets, see Section 8.2.5.1.1.3.2, *ISS CSI2 Long Packet*.

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Table 8-153. ISS CSI2 MIPI Format Supported by the Protocol Engine (continued)

MIPI			CSI2 Protocol Engine Support
Category	**Abbreviation**	**Register Setting Format Description**	**Configuration Value for CSI2_CTX_CTRL2_i[9:0] FORMAT**
		YUV4:2:2 8-bit + VP16	0x0DE
	YUV4:2:2 10-bit	YUV4:2:2 10-bit	0x01F
RGB data	RGB444	RGB444 + EXP16	0x0A0
	RGB555	RGB555 + EXP16	0x0A1
	RGB565	RGB565	0x022
	RGB666	RGB666 + EXP32	0x0E3
		RGB666 + EXP32_24	0x033
	RGB888	RGB888	0x024
		RGB888 + EXP32	0x0E4
	Reserved	Send to memory when FORMAT = 0	0x025
	Reserved	Send to memory when FORMAT = 0	0x026
	Reserved	Send to memory when FORMAT = 0	0x027
RAW data	RAW6	RAW6	0x028
		RAW6 + EXP8	0x068
		RAW6 + DPCM10 + VP	0x0E8
		RAW6 + DPCM10 + EXP16	0x2A8
		RAW6 + DPCM12 + VP	0x368
		RAW6 + DPCM12 + EXP16	0x3A8
	RAW7	RAW7	0x029
		RAW7 + EXP8	0x069
		RAW7 + DPCM10 + EXP16	0x229
		RAW7 + DPCM10 + VP	0x329
		RAW7 + DPCM12 + EXP16	0x369
		RAW7 + DPCM12 + VP	0x3A9
	RAW8	RAW8	0x02A
		RAW8 + VP	0x12A
		RAW8 + DPCM10 + EXP16	0x2AA
		RAW8 + DPCM10 + VP	0x32A
		RAW8 + DPCM12 + EXP16	0x36A
		RAW8 + DPCM12 + VP	0x3AA
	RAW10	RAW10	0x02B
		RAW10 + EXP16	0x0AB
		RAW10 + VP	0x12F
	RAW12	RAW12	0x02C
		RAW12 + EXP16	0x0AC
		RAW12 + VP	0x12C
	RAW14	RAW14	0x02D
		RAW14 + EXP16	0x0AD
		RAW14 + VP	0x12D
	Reserved	Send to memory when FORMAT = 0	0x02E
	Reserved	Send to memory when FORMAT = 0	0x02F
User-defined byte-based data		USER_DEFINED_BYTE_DATA	0x040
		USER_DEFINED_BYTE_DATA + EXP8	0x080
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C0

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Table 8-153. ISS CSI2 MIPI Format Supported by the Protocol Engine (continued)

MIPI			CSI2 Protocol Engine Support
Category	Abbreviation	Register Setting Format Description	Configuration Value for CSI2_CTX_CTRL2_i[9:0] FORMAT
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x340
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C0
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x140
		USER_DEFINED_BYTE_DATA	0x041
		USER_DEFINED_BYTE_DATA + EXP8	0x081
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C1
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x341
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C1
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x141
		USER_DEFINED_BYTE_DATA	0x042
		USER_DEFINED_BYTE_DATA + EXP8	0x082
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C2
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x342
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C2
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x142
		USER_DEFINED_BYTE_DATA	0x043
		USER_DEFINED_BYTE_DATA + EXP8	0x083
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C3
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x343
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C3
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x143
		USER_DEFINED_BYTE_DATA	0x044
		USER_DEFINED_BYTE_DATA + EXP8	0x084
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C4
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x344
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C4
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x144
		USER_DEFINED_BYTE_DATA	0x045
		USER_DEFINED_BYTE_DATA + EXP8	0x085
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C5
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x345

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Table 8-153. ISS CSI2 MIPI Format Supported by the Protocol Engine (continued)

MIPI			CSI2 Protocol Engine Support
Category	**Abbreviation**	**Register Setting Format Description**	**Configuration Value for CSI2_CTX_CTRL2_i[9:0] FORMAT**
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C5
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x145
		USER_DEFINED_BYTE_DATA	0x046
		USER_DEFINED_BYTE_DATA + EXP8	0x086
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C6
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x346
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C6
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x146
		USER_DEFINED_BYTE_DATA	0x047
		USER_DEFINED_BYTE_DATA + EXP8	0x087
		USER_DEFINED_BYTE_DATA + DPCM10 + EXP16	0x2C7
		USER_DEFINED_BYTE_DATA + DPCM10 + VP	0x347
		USER_DEFINED_BYTE_DATA + DPCM12 + EXP16	0x1C7
		USER_DEFINED_BYTE_DATA + DPCM12 + VP	0x147
Reserved		Send to memory when FORMAT = 0	0x038
		Send to memory when FORMAT = 0	0x039
		Send to memory when FORMAT = 0	0x03A
		Send to memory when FORMAT = 0	0x03B
		Send to memory when FORMAT = 0	0x03C
		Send to memory when FORMAT = 0	0x03D
		Send to memory when FORMAT = 0	0x03E
		Send to memory when FORMAT = 0	0x03F

8.2.5.2 ISS CSI2 Integration

Figure 8-68 is an overview of the integration of the CSI2_A/CSI2_B/CSI2_C interface in the device. The figure is the top-level block diagram of the CSI2_A/CSI2_B/CSI2_C receiver. The CSI2_A/CSI2_B/CSI2_C receiver receives the serial data coming from a CSI2 compatible image sensor, converts it to parallel data, extracts the logical channels, detects and extracts the synchronization codes, reformats the data, and outputs it through the video port or the ISS interconnect interface. A direct connection to both bayer scaler modules (BYS_A and BYS_B) is provided.

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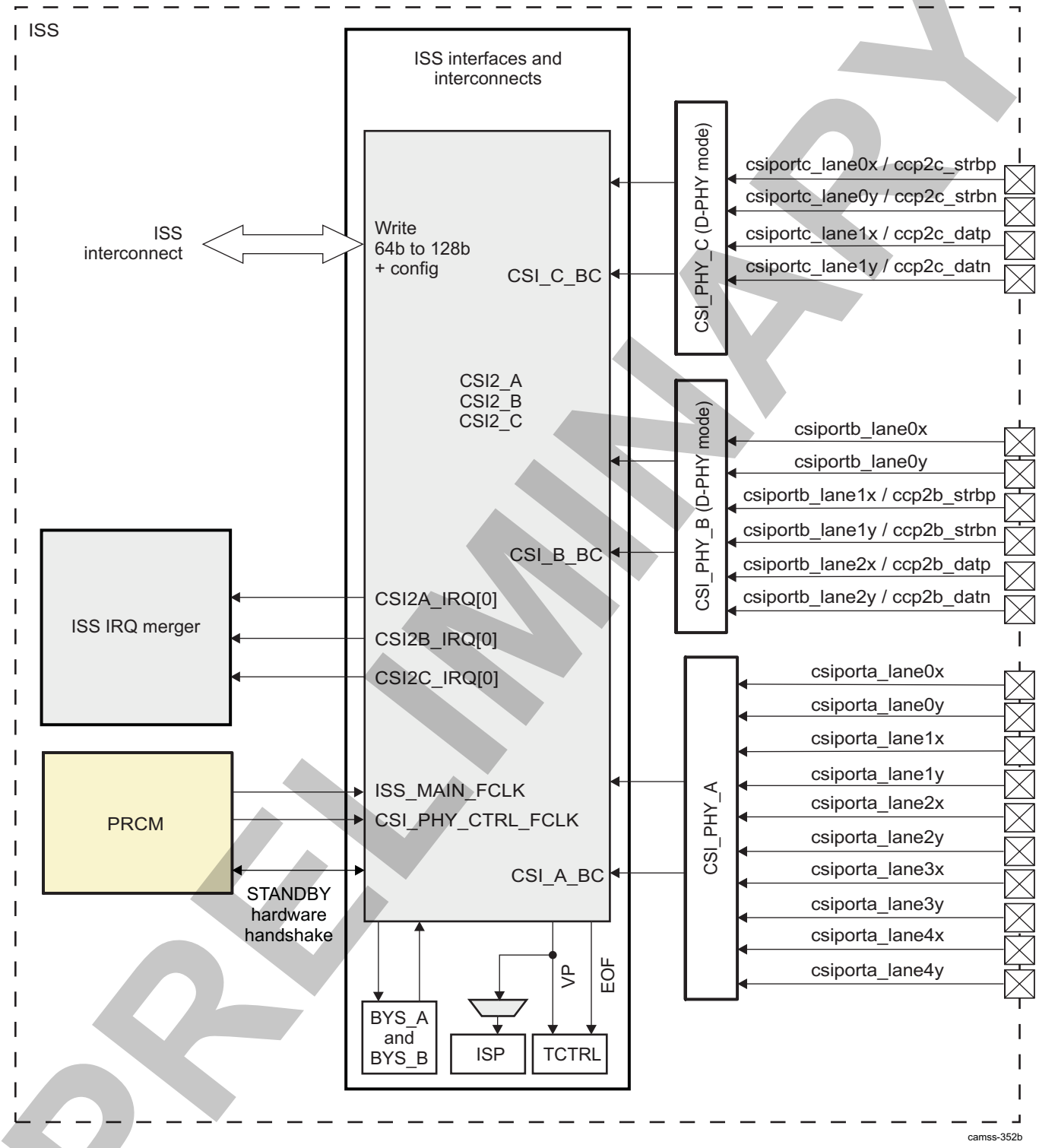
Figure 8-68. ISS CSI2_A/CSI2_B/CSI2_C Integration



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The CSI2_A/CSI2_B/CSI2_C receiver can send data directly to system memory using the master port or send it to the camera ISP using the video port.

For power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

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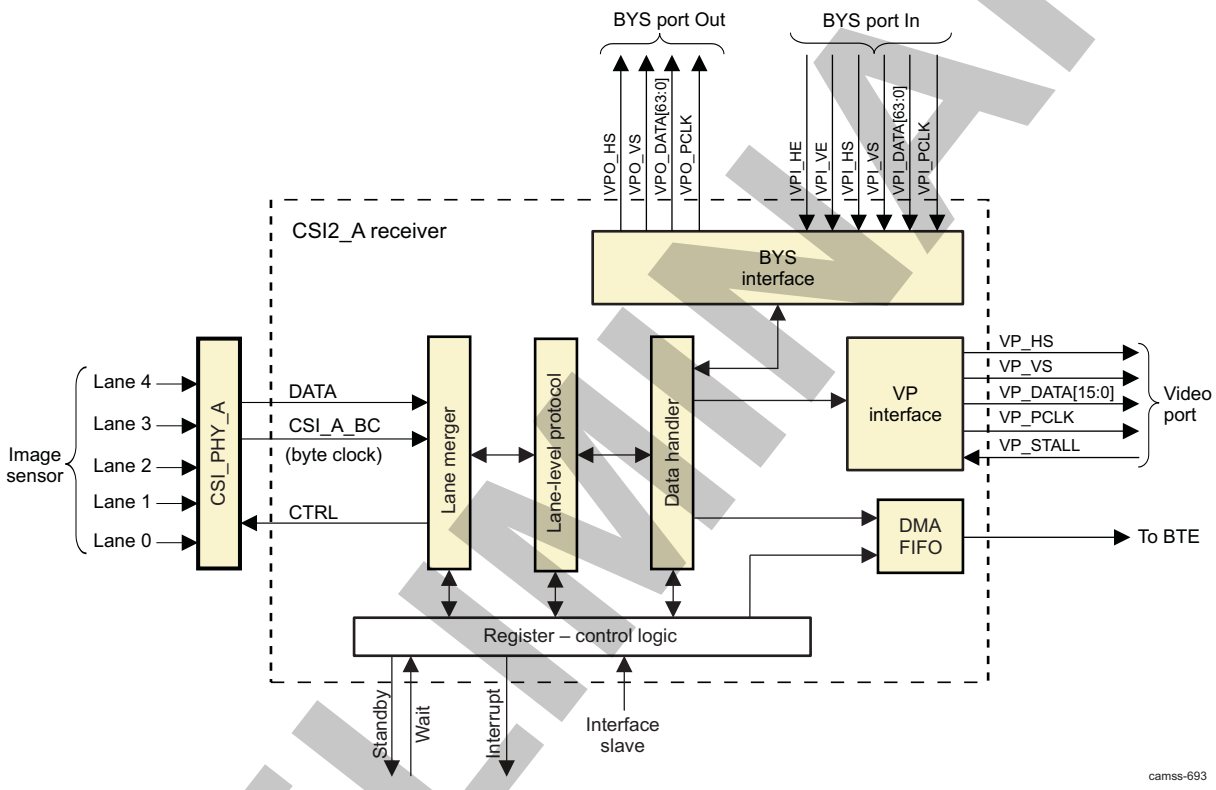
8.2.5.3 ISS CSI2 Functional Description

8.2.5.3.1 ISS CSI2 Overview

Figure 8-69 is the CSI2_A receiver block diagram (it assumes there are four CSI2 image sensor data lines). The only difference for CSI2_B and CSI2_C is the number of lanes coming into the complex I/O. The CSI2 receiver receives the byte data coming from a CSI2 D-PHY receiver CSI_PHY_A (up to four data pairs), converts it to byte stream, detects and corrects errors, extracts the virtual channel ID, detects and extracts the synchronization codes, reformats the data, and outputs it through the video port or the ISS interconnect interface. Data communication between CSI2 and ISP is done through the video port.

Figure 8-69. ISS CSI2_A Receiver Block Diagram



8.2.5.3.2 ISS CSI2 Features

The CSI2 receiver is a master on the L3_MAIN interconnect for storing data in memory and a slave on the level 4 (L4) interconnect for register access.

The main features of the CSI2 receiver are:

- Transfer pixels and data received by the CSI2 PHY to the system memory or video processor
- Unidirectional data link
- Supports up to four data-configurable links in addition to the clock signaling (minimum of one data link and maximum of four depending on the speed)
- Data merger for two, three, or four data lane configurations
- Error detection and correction by the protocol engine
- DMA engine integrated with dedicated FIFO
- 1D and 2D addressing modes
- Up to eight contexts to support eight dedicated configurations of virtual channel ID and data types
- Ping-pong mechanism for double-buffering
- JPEG support for unknown length transfer (no extraction of the thumbnail)

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- Supports all primary and secondary MIPI-defined formats (RGB, RAW, and YUV)
- Storage in progressive mode for interlaced stream (using line numbering)
- Conversion to the RGB formats
- Decompressions of the RAW formats
- RAW frame transcoding, including DPCM and A-Law compression
- Fully configurable interface of the complex PHY I/O: position of the clock and data and order of ± differential signals for each pair

8.2.5.3.3 ISS CSI2 Functional Description

8.2.5.3.3.1 ISS CSI2 Physical Layer Lane Configuration

The CSI2 serial interface is a unidirectional differential serial interface with data/clock for the physical layer.

The maximum CSI2 receiver data transfer capacity is 1000 Mbps per data lane.

Data-clock signaling consists of two to five differential signal pairs: from one to four data lanes and one clock lane:

- The data signal carries the bit-serial data. The CSI2 transmitter in the image sensor sends the data in-quadrature with the dual-data rate (DDR) clock in HS mode; otherwise, the clock is extracted from the received data in LS mode. Data is transmitted byte-wise, LSB first. The CSI2 complex I/O receives the data and sends the byte stream to the CSI2 receiver.
- The clock signal carries the DDR clock signal.

Each physical lane can be a data or clock lane with a restriction to the fourth line, which can only be data (see Section 8.2.3.1, *ISS CSI PHY Overview*). The clock/data lane must be configured before transmission to indicate the byte order, while merging the received bytes into a byte stream shows the reachable speed per data lane function of data lane numbers.

Lanes are configured through the CSI2_COMPLEXIO_CFG registers. The CSI2_COMPLEXIO_CFG[2:0] CLOCK_POSITION bit field and the CSI2_COMPLEXIO_CFG[3] CLOCK_POL bit configure which lane transmits the clock and define its polarity. DATAl_POSITION and DATAl_POL configure the data lanes and their polarity, where l is the number of the data lane (l = 1 to 4). When the DATAl_POSITION field is set to 0, data lane l is not used.

CAUTION

Lane 4 (position 5) supports only data. The CLOCK_POSITION must not be set at position 5.

8.2.5.3.3.2 ISS CSI2 ECC and Checksum Generation

The CSI2 receiver includes an ECC in the packet header and a checksum in the packet footer for long-packet transmission. These two fields can be used to detect and/or correct errors in the received packet.

8.2.5.3.3.2.1 ISS CSI2 ECC

To detect and correct transmission errors of the header of short and long packets, an 8-bit ECC is included in the header of packets (short and long packet).

The ECC concerns all the fields for a short packet (data ID and short-packet data field) and the packet header for a long packet (data ID and word count). The ECC can only correct one error. Additional errors cannot be repaired, but they are flagged.

The CSI2 receiver ECC is compared against the CSI2 transmitter ECC embedded in the bitstream. If the ECC does not match, an interrupt is triggered to the host central processing unit (CPU).

For long and short packets, the correction is always done if there is only one error per packet header.

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An ECC error with or without correction can be reported at two levels, depending on the type of packet. Table 8-154 describes the field in which events are logged. Logging cannot be disabled, but users can set the corresponding bit in the CSI2_IRQENABLE and CSI2_CTX_IRQENABLE_i registers to prevent event generation at a higher level.

Table 8-154. ISS CSI2 ECC Event Logging

	Short Packet	Long Packet
With correction	Global CSI2_IRQSTATUS[12] ECC_CORRECTION_IRQ	Context CSI2_CTX_IRQSTATUS_i[8] ECC_CORRECTION_IRQ
Without correction	Global CSI2_IRQSTATUS[11] ECC_NO_CORRECTION_IRQ	Global CSI2_IRQSTATUS[11] ECC_NO_CORRECTION_IRQ

The ECC check can be disabled (short and long packet) by setting the CSI2_CTRL[2] ECC_EN bit to 0. Setting the bit to 1 enables the ECC check.

8.2.5.3.3.2.2 ISS CSI2 Checksum

To detect errors in transmission of the payload of long packets, a 16-bit CRC checksum is computed on the payload of the long packets in the transmitter. This CRC is stored in the packet footer. A CRC is also computed in the CSI2 receiver. If the checksums do not match, an interrupt is triggered to the host CPU.

CRC errors are logged in the CS_IRQ field of the corresponding context register, CSI2_CTX_IRQSTATUS_i. Logging cannot be disabled, but users can set the corresponding bit in the CSI2_CTX_IRQENABLE_i register to prevent event generation at a higher level.

The CRC can be disabled for a specific context by setting the CSI2_CTRL[5] CS_EN bit to 0. Setting the bit to 1 enables the CRC.

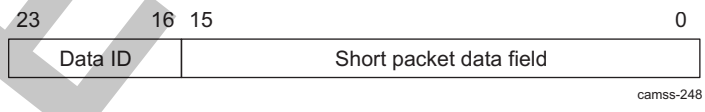
8.2.5.3.3.3 ISS CSI2 Short Packet

There are two types of short packets in the CSI2 receiver:

- Synchronization short packet: Used by the protocol engine to synchronize frame and line (data ID from 0x0 to 0x7)
- Generic short packet: User-dependent; not treated by the protocol engine (data ID from 0x8 to 0xF)

When a generic short packet is received by the CSI2 receiver, the ECC check is performed if it is enabled. Then, the short packet is written in the CSI2_SHORT_PACKET[23:0] SHORT_PACKET bit field. The ECC field is deleted from the short packet. Figure 8-70 shows the SHORT_PACKET bit field format.

Figure 8-70. ISS CSI2 SHORT_PACKET Bit Field Format



When a short packet is stored, an event is logged in the CSI2_IRQSTATUS[13] SHORT_PACKET_IRQ bit. Logging cannot be disabled, but users can set the corresponding bit in the CSI2_IRQENABLE register to prevent event generation at a higher level.

The application reads the CSI2_SHORT_PACKET register before the next short packet with a code from 0x8 to 0xF. There is a single register for capturing the generic short packet, because no data type in it is associated with context.

8.2.5.3.3.4 ISS CSI2 Virtual Channel and Context

The CSI2 protocol layer transports virtual channels. The virtual channels separate different data flows interleaved in the same data stream. Each virtual channel is identified by a unique channel identification number in the packet header. This channel identification number is encoded in the 2-bit code.

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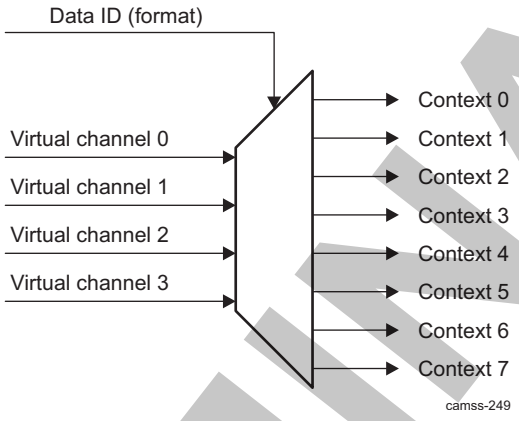
The CSI2 receiver monitors the channel identifier number and demultiplexes the interleaved data streams. The CSI2 receiver supports up to four concurrent virtual channels.

The CSI2 receiver supports eight contexts with their events to control the four possible virtual channels and the different data transmitted through them. A context is linked to a specific data type transported by a given virtual channel. The following bit fields permit configuration of a context:

- CSI2_CTX_CTRL2_i[12:11] VIRTUAL_ID: Configures the virtual ID linked to the current context
- CSI2_CTX_CTRL2_i[9:0] FORMAT: Configures the data format linked to the current context

Figure 8-71 shows the relationships between virtual channels and contexts.

Figure 8-71. ISS CSI2 Virtual Channel to Context



Each context consists of eight registers: six registers to control the corresponding context and two to log and enable events from the context. All registers in a context can be modified at any time; however, modifications apply only from the start of the following frame.

A context can be enabled independently by setting the CSI2_CTX_CTRL1_i[0] CTX_EN bit to 1; setting this bit to 0 disables the corresponding context.

When acquiring frames on a context, users can write the number of frames to capture in the CSI2_CTX_CTRL1_i[15:8] COUNT bit field. Acceptable values are 0 to 255; 0 stands for infinite capture (no count). After each frame is acquired, the count value is decremented by 1. When the count value reaches 0, the CSI2_CTX_IRQSTATUS_i[6] FRAME_NUMBER_IRQ event is set and the CTX_EN bit is set to 0. To write a value in the COUNT bit field, the CSI2_CTX_CTRL1_i[4] COUNT_UNLOCK bit must be set to 1. If the value of the COUNT_UNLOCK bit is 0, a write in the COUNT bit field has no effect.

The CSI2_CTX_CTRL3_i[15:0] LINE_NUMBER bit field configures the generation of the CSI2_CTX_IRQSTATUS_i[7] LINE_NUMBER_IRQ event. The CSI2_CTX_CTRL1_i[1] LINE_MODULO bit configures how the LINE_NUMBER event is generated:

- 0: The event is generated one time by frame.
- 1: The event is generated modulo LINE_NUMBER (the event can be generated more than once in a frame).

During a frame capture, the CSI2_CTX_CTRL2_i[31:16] FRAME_NUMBER bit field shows the number that identifies the frame received.

8.2.5.3.3.5 ISS CSI2 DMA Engine

The CSI2 receiver integrates its own DMA engine with dedicated FIFO.

Global DMA configuration is common to the eight channels and is defined in the CSI2_CTRL register. Configuration of the ping-pong address and the offset between lines is specific for a given context; therefore, each context has its own DMA configuration registers.

The DMA engine supports:

- 1D addressing mode (no address line offset, CSI2_CTX_DAT_OFST_i = 0)
- 2D addressing mode (address line offset different than 0, CSI2_CTX_DAT_OFST_i = 0)

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The burst size is defined in the CSI2_CTRL[6:5] BURST_SIZE bit field and the CSI2_CTRL[16] BURST_SIZE_EXPAND bit. The DMA uses the burst size or smaller sizes down to single open-core protocol (OCP) writes depending on the alignment at the end of lines. The DMA engine can handle burst requests. When the burst requests can be used, as soon as one burst of data is present in the FIFO, the DMA engine initiates a burst write. The burst size is defined in the CSI2_CTRL[6:5] BURST_SIZE bit field and the CSI2_CTRL[16] BURST_SIZE_EXPAND bit.

NOTE: Unless there are specific requirements, CSI2 (also applies to all other ISS initiators) must be configured to use only a burst size of 128 bytes and nonposted writes.

The CSI-2 receiver issues single request at the end of lines, when there is not enough data to generate the programmed burst size. Other burst sizes than a single request and the programmed burst size are not used.

When single requests must be used, as soon as one element (the size depends on the data type and the post-processing: DPCM, EXT, etc.) is present in the FIFO, the DMA engine initiates a single write.

Interleave mode is dedicated by the CSI2 receiver only when the line numbers are received (short packets). The line number is used to calculate the start address of the line.

The DMA starts to write in memory using the CSI2_CTX_DAT_PING_ADDR_i[31:5] ADDR bit field for the first frame to be transferred, and then uses the CSI2_CTX_DAT_PONG_ADDR_i[31:5] ADDR bit field and the ping address alternately. Thus, the first frame uses the ping address, the second frame uses the pong address, the third frame uses the ping address, and so on.

The CSI2_CTX_CTRL1_i[3] PING_PONG status bit indicates whether the ping address (CSI2_CTX_DAT_PING_ADDR_i) or the pong address (CSI2_CTX_DAT_PONG_ADDR_i) was used to store the pixel data of the last frame. After reset or after a 0-to-1 edge transition in the CSI2_CTRL[0] IF_EN bit, the pixel data is written in the ping buffer and the CSI2_CTX_CTRL1_i[3] PING_PONG bit = PONG. When the number of FECs received equals the value programmed in the CSI2_CTX_CTRL1_i[23:16] FEC_NUMBER bit field, the pixel data are written in the pong buffer and CSI2_CTX_CTRL1_i[3] PING_PONG = PING. CSI2_CTX_CTRL1_i[3] PING_PONG toggles after the CSI2_CTX_CTRL1_i[23:16] FEC_NUMBER FEC sync code with the virtual channel ID defined is received in the CSI2_CTX_CTRL2_i[12:11] VIRTUAL_ID bit field.

The CSI2_CTX_CTRL1_i[23:16] FEC_NUMBER bit field must be set as follows:

- In progressive mode, set to 1.
- In interlaced mode, set to the number of interlaced frames to recreate a progressive image in the PING_PONG buffer.

8.2.5.3.3.5.1 ISS CSI2 Progressive Frame to Progressive Storage

After each line, a new start line address is computed, depending on the value of the CSI2_CTX_DAT_OFST_i[31:5] OFST bit field:

- If OFST = 0, the new line starts immediately after the last pixel (data are written contiguously in memory).
- Otherwise, the value of OFST sets the offset between the first pixel of the previous line and the first pixel of the current line in memory.

For the ping frame:

```
@Line0 = CSI2_CTX_DAT_PING_ADDR_i@Line1 = @Line0 + CSI2_CTX_DAT_OFST_i@Line2 = @Line1 +
CSI2_CTX_DAT_OFST_i
```

For the pong frame:

```
@Line0 = CSI2_CTX_DAT_PONG_ADDR_i@Line1 = @Line0 + CSI2_CTX_DAT_OFST_i@Line2 = @Line1 +
CSI2_CTX_DAT_OFST_i
```

8.2.5.3.3.5.2 ISS CSI2 Interlaced Frame to Progressive Storage

The mode is functional only when the line numbers are transmitted. It is automatically enabled without setting.

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For the ping frame:

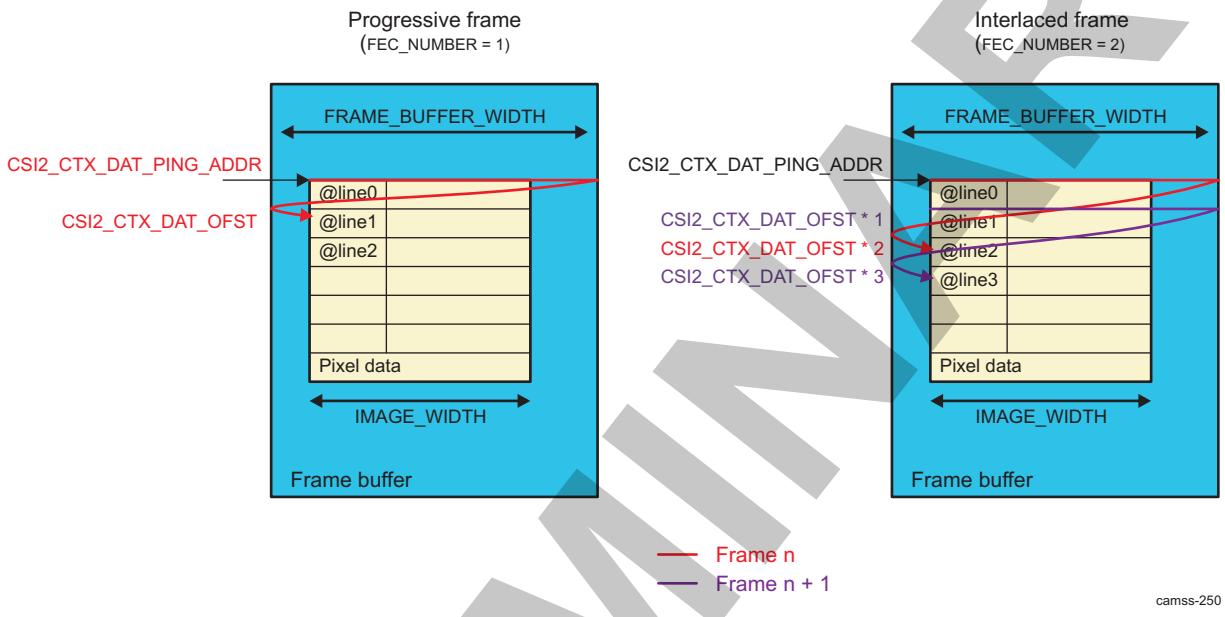
```
@LineX = CSI2_CTX_DAT_PING_ADDR_i + CSI2_CTX_DAT_OFST_i * Line_Number
```

For the pong frame:

```
@LineX = CSI2_CTX_DAT_PONG_ADDR_i + CSI2_CTX_DAT_OFST_i * Line_Number
```

Figure 8-72 shows how data are stored in memory regarding the DMA configuration.

Figure 8-72. ISS CSI2 Pixel Data Destination Setting in Progressive and Interlaced Mode



The burst size is defined in the CSI2_CTRL[6:5] BURST_SIZE bit field for bursts up to 16 × 64 bits or the CSI2_CTRL[16] BURST_SIZE_EXPAND bit for 16 × 128-bit bursts. It can be changed only while the CSI2_CTRL[0] IF_EN bit is reset to 0. The recommended value is the CSI2_CTRL[16] BURST_SIZE_EXPAND bit set to 1, which defines a burst of 16 × 64 bits (the maximum value); otherwise, by default it is set to 8 × 64 bits. When the BURST_SIZE_EXPAND bit is set, the BURST_SIZE setting has no effect. The DMA uses nonposted writes by default. The CSI2_CTRL[13] NON_POSTED_WRITE bit must be set to 1 to match DMA default configuration. It can be changed only while the CSI2_CTRL[0] IF_EN bit is reset to 0.

8.2.5.3.3.6 ISS CSI2 MFLAG Mechanism and Arbitration

The MFLAG mechanism allows a dynamic increase of the priority of CSI2 real-time traffic, when required, based on the fullness of the CSI2 DMA read and write buffers. Programmable buffer thresholds are used to indicate when the local MFLAG signal is generated, which is then provided to the L3 interconnect for granting or prioritizing OCP requests. The out band CSI2 MFLAG signal is asynchronous to any on-going OCP transaction. The threshold corresponds to the fullness of DMA buffer, and is defined by the following threshold parameters:

- High threshold: When the corresponding pipeline buffer reaches the programmed value, the associated local MFLAG signal goes high (asserted). The value is set in the CSI2_CTRL[22:20] MFLAG_LEVH register.
- Low threshold: When the corresponding pipeline buffer reaches the programmed value, the associated local MFLAG signal goes low (deasserted). The value is set in the CSI2_CTRL[19:17] MFLAG_LEVL register.

8.2.5.3.3.7 ISS CSI2 Transcoding

Image transcoding is used mainly to reduce memory footprint and bandwidth when:

- The sensor does not support DPCM compression. In fact, A-Law and DPCM compressed pixels occupy only 6, 7, or 8 BPP of storage.

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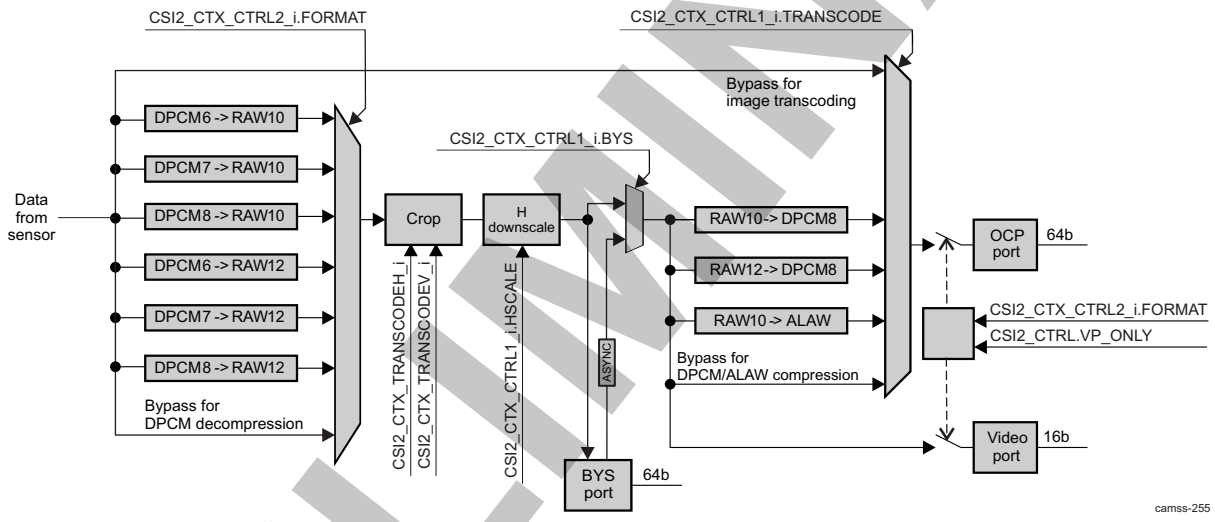
- Digital zoom is used
  - Data that is not going to be used by further processing does not need to the stored in system memory.
  - Pixels cannot be accessed from random locations in a DPCM-compressed frame. Transcoding avoids memory-to-memory processing of unused pixels.

Figure 8-73 shows the logical representation of the image transcoding operation.

- Data is extracted from the CSI2 stream by the protocol engine.
- It is DPCM decompressed if necessary. That is the case when the received stream is DPCM-compressed and transcoding has been enabled using the CSI2_CTX_CTRL1_i[27:24] TRANSCODE bit field.
- Data sent to the video port cannot be compressed: it is intended to be processed by the ISS ISP. Data sent to system memory can be optionally compressed.
- Internal data are aligned on MSB when they enter the cropping stage. For example:
  - 4 LSBs are 0s when RAW10 data are handled.
  - 2 LSBs are 0s when RAW12 data are handled.

Figure 8-73. ISS CSI2 Frame Processing



Only one context can use the BYS port at the time. Software must ensure that the CSI2_CTX_CTRL1_i[29] BYS is set only for one of the contexts. The BYS port can only be used for progressive formats. No field information is transmitted over the BYS port. See Section 8.2.5.3.3.10, *ISS CSI2 BYS Interface*, for more information on the BYS interface ports.
Data from the sensor can not go through the transcoding stage when data is received on BYS input port. Both sources are not necessarily synchronized and therefore resource (DPCM encoder, OCP port, video port, etc.) conflicts may occur, if data arrives simultaneously from BYS input port and the CSI-2 camera device. Software must ensure that this condition does not occur. The hardware does not perform any particular verification, if that condition is met.

Table 8-155 shows the input format provided to the cropping engine for a given pixel format provided by the sensor. Formats not listed in the table are not supported for transcoding. The FORMAT and Corresponding Setting Value column corresponds to the value set in the CSI2_CTX_CTRL2_i[9:0] FORMAT register. The last column shows the formats for which the horizontal downscaling of RAW data is supported.

Table 8-155. ISS CSI2 Supported Transcoding Input Formats

CSI2_CTX_CTRL2_i[9:0] FORMAT and Corresponding Setting Value		Cropping Engine Input Format	DPCM Decomposition Enabled	Video Port Enabled	Horizontal Downscale Supported
0x028	RAW6	RAW6			

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Table 8-155. ISS CSI2 Supported Transcoding Input Formats (continued)

CSI2_CTX_CTRL2_i[9:0] FORMAT and Corresponding Setting Value		Cropping Engine Input Format	DPCM Decomposition Enabled	Video Port Enabled	Horizontal Downscale Supported
0x068	RAW6 + EXP8				
0x029	RAW7	RAW7			
0x069	RAW7 + EXP8				
0x02A	RAW8	RAW8			
0x12A	RAW8 + VP			Yes	
0x02B	RAW10	RAW10			Yes
0x0AB	RAW10 + EXP16				Yes
0x0E8	RAW6 + DPCM10 + VP		Yes	Yes	Yes
0x12F	RAW10 + VP			Yes	Yes
0x229	RAW7 + DPCM10 + EXP16		Yes		Yes
0x2A8	RAW6 + DPCM10 + EXP16		Yes		Yes
0x2AA	RAW8 + DPCM10 + EXP16		Yes		Yes
0x329	RAW7 + DPCM10 + VP		Yes	Yes	Yes
0x32A	RAW8 + DPCM10 + VP		Yes	Yes	Yes
0x2Cn	USER_DEFINED_BYTE_DATA + DPCM10 + EXP16		Yes		Yes
0x34n	USER_DEFINED_BYTE_DATA + DPCM10 + VP		Yes	Yes	Yes
0x02C	RAW12	RAW12			Yes
0x0AC	RAW12 + EXP16				Yes
0x12C	RAW12 + VP			Yes	Yes
0x36A	RAW8 DPCM12 + EXP16		Yes		Yes
0x3AA	RAW8 DPCM12 + VP		Yes	Yes	Yes
0x1Cn	USER_DEFINED_BYTE_DATA + DPCM12 + EXP16		Yes		Yes
0x14n	USER_DEFINED_BYTE_DATA + DPCM12 + VP		Yes	Yes	Yes
0x3A8	RAW6 + DPCM12 + EXP16		Yes		Yes
0x368	RAW6 + DPCM12 + VP		Yes	Yes	Yes
0x369	RAW7 + DPCM12 + EXP16		Yes		Yes
0x3A9	RAW7 + DPCM12 + VP		Yes	Yes	Yes
0x02D	RAW14	RAW14			Yes
0x0AD	RAW14 + EXP16				Yes
0x12D	RAW14 + VP			Yes	Yes

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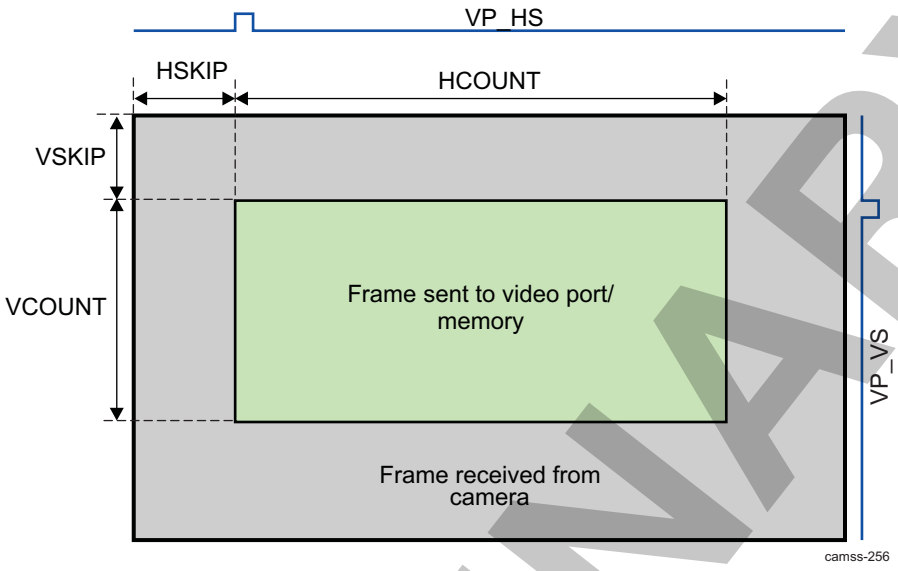
Image cropping parameters are controlled by software. Figure 8-74 shows the cropping operation.

Figure 8-74. ISS CSI2 Frame Cropping



CAUTION

Hardware does not check for validity of the settings. The following rules must be respected:

- CSI2_CTX_TRANSCODEH_i[12:0] HSKIP + CSI2_CTX_TRANSCODEH_i[28:16] HCOUNT <= image width
- CSI2_CTX_TRANSCODEV_i[12:0] VSKIP + CSI2_CTX_TRANSCODEV_i[28:16] VCOUNT <= image height

Furthermore, the CSI2_CTX_TRANSCODEH_i[28:16] HCOUNT bit field must comply with the following alignment constraints; otherwise, undefined behavior occurs. Table 8-156 shows the transcode alignment constraints

Table 8-156. ISS CSI2 Transcode Alignment Constraints

CSI2_CTX_CTRLi[27:24] TRANSCODE Value	Transcode	HCOUNT Must Be Multiple of
0x0	Disabled	1
0x1	DPCM10 RAW8	1
0x2	DPCM12 RAW8	1
0x3	ALAW10 RAW8	1
0x4	RAW8	1
0x5	RAW10 + EXP16	1
0x6	RAW10	4
0x7	RAW12 + EXP16	1
0x8	RAW12	2
0x9	RAW10 + EXP16	4

The CSI2_CTX_CTRL1_i[28] HSCALE configuration register enables horizontal downscaling of RAW data. It reduces the horizontal size and pixel clock by a factor of 2. The scaler uses a 2-tap horizontal filter operating on samples of the same color plane. The coefficients are: [1/2 ; 0 ; 1/2]. The formats that support horizontal downscaling are shown in Table 8-155, *ISS CSI2 Supported Transcoding Input Formats*.

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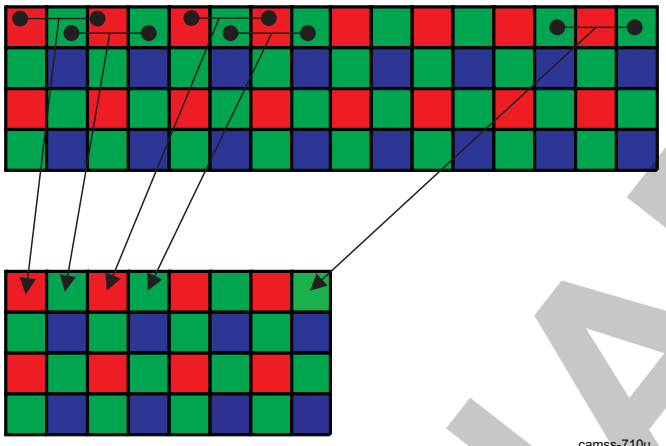
Figure 8-75 shows the scaler operation.

Figure 8-75. ISS CSI2 Horizontal Scaler



The scaler can send data to the video port or the interface port. When data goes to the video port, no additional alignment constraints apply. But when data goes to the interface port, HCOUNT/2 must comply with the constraints from Table 8-156 (for example, for RAW10, HCOUNT must be a multiple of 8).

Table 8-157 lists possible combinations of input and output formats supported by the transcoding engine. The Transcode column corresponds to the CSI2_CTX_CTRL1_i[27:24] TRANSCODE bit field of a context.

Table 8-157. ISS CSI2_Supported Transcoding Output Formats

Cropping Engine Output	Transcode		Supported	Cropping Engine Output	Transcode		Supported
RAW6	0	Disabled	Yes	RAW10	0	Disabled	Yes
	1	DPCM10 RAW8			1	DPCM10 RAW8	Yes
	2	DPCM12 RAW8			2	DPCM12 RAW8	
	3	ALAW10 RAW8			3	ALAW10 RAW8	Yes
	4	RAW8			4	RAW8	
	5	RAW10 + EXP16			5	RAW10 + EXP16	Yes
	6	RAW10			6	RAW10	Yes
	7	RAW12 + EXP16			7	RAW12 + EXP16	
	8	RAW12			8	RAW12	
	9	RAW14			9	RAW14	
RAW7	0	Disabled	Yes	RAW12	0	Disabled	Yes
	1	DPCM10 RAW8			1	DPCM10 RAW8	
	2	DPCM12 RAW8			2	DPCM12 RAW8	Yes
	3	ALAW10 RAW8			3	ALAW10 RAW8	
	4	RAW8			4	RAW8	
	5	RAW10 + EXP16			5	RAW10 + EXP16	
	6	RAW10			6	RAW10	
	7	RAW12 + EXP16			7	RAW12 + EXP16	Yes
	8	RAW12			8	RAW12	Yes
	9	RAW14			9	RAW14	
RAW8	0	Disabled	Yes	RAW14	0	Disabled	Yes
	1	DPCM10 RAW8			1	DPCM10 RAW8	
	2	DPCM12 RAW8			2	DPCM12 RAW8	
	3	ALAW10 RAW8			3	ALAW10 RAW8	
	4	RAW8	Yes		4	RAW8	

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Table 8-157. ISS CSI2_Supported Transcoding Output Formats (continued)

Cropping Engine Output	Transcode		Supported	Cropping Engine Output	Transcode		Supported
	5	RAW10 + EXP16			5	RAW10 + EXP16	
	6	RAW10			6	RAW10	
	7	RAW12 + EXP16			7	RAW12 + EXP16	
	8	RAW12			8	RAW12	
	9	RAW14			9	RAW14	Yes

RAW pixels are packed into 64-bit words sent to the OCP master port, as defined in:

- Section 8.2.5.1.1.4.3.3, *ISS CSI2 RAW8*
- Section 8.2.5.1.1.4.3.4, *ISS CSI2 RAW10*
- Section 8.2.5.1.1.4.3.5, *ISS CSI2 RAW12*
- Section 8.2.5.1.1.4.3.6, *ISS CSI2 RAW14*

For RAW10 and RAW12, software can choose among packed and nonpacked storage. A-Law and DPCM-compressed pixels are stored as RAW8 data: each RAW8 container holds a compressed data point.

Similarly, RAW data is sent over the video port, as described in:

- Section 8.2.5.1.1.4.3.3, *ISS CSI2 RAW8*
- Section 8.2.5.1.1.4.3.4, *ISS CSI2 RAW10*
- Section 8.2.5.1.1.4.3.5, *ISS CSI2 RAW12*
- Section 8.2.5.1.1.4.3.6, *ISS CSI2 RAW14*

Enabling of the OCP/video port is controlled by the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field and the CSI2_CTRL[11] VP_ONLY_EN and CSI2_CTX_CTRL1_i[2] VP_FORCE bits.

To enable transcoding, software configures the context normally and also configures the framing using the CSI2_CTX_TRANSCODEV_i and CSI2_CTX_TRANSCODEH_i registers. Software defines the after transcoding with the CSI2_CTX_CTRL1_i[27:24] TRANSCODE bit field.

8.2.5.3.3.8 ISS CSI2 EndOfFrame and EndOfLine (EOF and EOL) Pulses

The CSI2 receiver generates two signals to qualify the last pixel of a frame and the last pixel of a line to the TCTRL. It is active during or after the adequate interface bridge transaction and becomes inactive before the first transaction of the next line. Software can enable/disable generation of those signals for each context using the CSI2_CTX_CTRL1_i[7] EOF_EN and CSI2_CTX_CTRL1_i[6] EOL_EN bits. When data is sent to both OCP and video ports, the EOL/EOF timing defined for the OCP port is used.

8.2.5.3.3.9 ISS CSI2 Data Decompression

The data compression technique used is DPCM and PCM.

To select the DPCM decompression predictor for the CSI2 Interface, set the CSI2_CTX_CTRL2_i[10] DPCM_PRED bit to 1 for simple predictor or to 0 for advanced predictor.

8.2.5.3.3.10 ISS CSI2 BYS Interface

The module has one BYS port for data input and another one for data output. See Figure 8-69, *ISS CSI2_A Receiver Block Diagram*, and Figure 8-73, *ISS CSI2 Frame Processing*. The input video port is asynchronous from the functional clock. The output video port is synchronous to the functional clock and the data rate is controlled through software configuration.

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The BYS ports are 4 pixels x 16 bits wide and carry 4 or 0 pixels per cycle. Pixels are LSB aligned inside 16-bit containers on the bus. Only RAW12 can be exchanged. Additional bits on the bus are provided for future compatibility. The CSI2_RECEIVER internally converts from the received format to RAW12 (decompression and left shift) before sending data to the BYS port. Data received on the BYS input port is converted according to the settings of the transcoding engine before it is send to the OCP port. See Section 8.2.5.3.3.7, *ISS CSI2 Transcoding*, for more details on image transcoding.

Table 8-158 shows an example of a typical bus transaction on the output port to BYS module, where the width is not a multiple of 4.

Table 8-158. BYS Port Transaction

Cycle Number	HS	VS	DATA[11:0]	DATA[15:12]	DATA[27:16]	DATA[31:28]	DATA[43:32]	DATA[47:44]	DATA[59:48]	DATA[63:60]
1	0	0	Any Data							
2	0	0	Any Data							
3	0	0	Any Data							
4	0	0	Any Data							
5	1	1	Pixel #0	0's	Pixel #1	0's	Pixel #2	0's	Pixel #3	0's
6	0	0	Pixel #4	0's	Pixel #5	0's	Pixel #6	0's	Pixel #7	0's
N	0	0	Last pixel	0's	0's	0's	0's	0's	0's	0's

Input and output BYS ports are independent. It is possible that:

- Data is sent to the BYS output port, but no data is received on the BYS input port;
- No data is sent to the BYS output port, but data is received on the BYS input port;
- Data is sent to the BYS output port and data is received on the BYS input port (not necessarily the same size and/or pixel rate).

The PCLK pulses are not necessarily regularly spaced.

On both video ports there must be at least 4 PCLK pulses before the 1st pixel of a frame (i.e. after reset) and there must be at least 4 PCLK cycles of vertical blanking between frames.

The software can control gating and speed of the pixel clock sent to the BYS output port using the CSI2_CTRL[24:23] BYS_CLK_CTRL bit. Software must ensure that the peak pixel clock provided to the BYS port is superior or equal to ¼ of the peak pixel clock from the sensor. The hardware automatically suppresses unneeded clock pulses to align the mean pixel clock of the BYS port with the mean pixel clock of the sensor. The BYS clock must be turned off when it is not needed, to save power, by setting the CSI2_CTRL[24:23] BYS_CLK_CTRL bit to 0x0 (default state).

The duration (in time units) of blanking periods on the output BYS port is imposed by the camera sensor. The number of PCLK pulses sent by the CSI2_RECEIVER module is defined by the chosen pixel clock and the blanking duration from the sensor.

The timings on the BYS input port are imposed by the BYS module. There is no signal indicating the line end. Software must set the number of pixels to acquire per line in the CSI2_CTX_CTRL3_i[31:16] ALPHA bit field. The configured value must be less of equal to the number of pixels provided by the BYS module. The CSI2_RECEIVER will discard additional pixels. There is no indication of the frame end on the BYS input port. The CSI2_RECEIVER flushes the data in the FIFO to the memory at every line end.

Software must ensure that all data of frame "n" has been received on BYS input port before the camera sends the frame start code of the next frame.

For more information on BYS modules functionality, see Section 8.2.9, *ISS BYS*.

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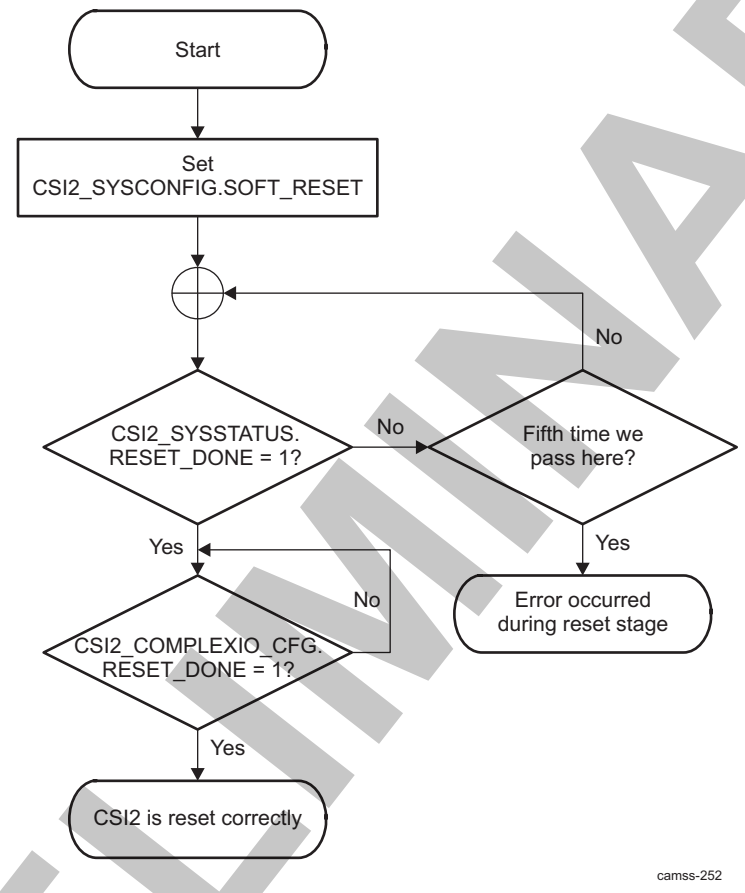
8.2.5.4 ISS CSI2 Programming Model

8.2.5.4.1 ISS CSI2 Programming Reset Management

The CSI2_RECEIVER accepts a general software reset, propagated throughout the hierarchy. This reset can be done to initialize the CSI2 receiver and the complex I/O (CSI_PHY_A, B or C) and has the same effect as a hardware reset. Figure 8-76 shows how to reset CSI2 globally.

Figure 8-76. ISS CSI2 Receiver Global Reset Flow Chart



NOTE: Before setting the software reset bit to 1 in the CSI2_SYSCONFIG register, the user must have access to a CSI2 receiver register.

NOTE: The CSI2_COMPLEXIO_CFG[29] RESET_DONE bit is set to 1 only after the initialization of the CSI2 receiver, CSI2 complex I/O, and external camera completes.

8.2.5.4.2 ISS CSI2 Programming Enable Video/Picture Acquisition

Before using the receiver, a PHY initialization in D-PHY mode must be made for CSI_PHY_A, B or C which is associated with the CSI2 receiver. See Section 8.2.3.2.2, *ISS CSI PHY (D-PHY Mode) and Link Initialization Sequence.* To start a video/picture acquisition, perform the steps listed in Table 8-159.

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Table 8-159. ISS CSI2 Global Initialization

Step	Register/Bit Field/Programming Model	Value
Reset the CSI2 receiver.	See Section 8.2.5.4.1, *Reset Management.*	
Configure the module power management. The module tries to enter smart-standby mode during the vertical blanking period. The CSI2_SYSCONFIG[0] AUTO_IDLE bit keeps its reset value; by default, an automatic port clock gating strategy is applied based on port interface activity.	CSI2_SYSCONFIG[13:12] MSTANDBY_MODE	0x2
Configure the interrupt generation as required. To enable context and/or complex I/O event reporting, enable the corresponding bit field in the CSI2_IRQENABLE register. If the enable bit is at 0, logging is still effective if an event occurs, but is not reported to a higher level.	CSI2_IRQSTATUS and CSI2_IRQENABLE	
Configure the complex I/O interrupt generation as required. If the enable bit is at 0, logging is still effective if an event occurs, but is not reported to a higher level.	CSI2_COMPLEXIO_IRQSTATUS and CSI2_COMPLEXIO_IRQENABLE)	
Start complex I/O: Set the CSI2_COMPLEXIO_CFG[28:27] PWR_CMD bit field to 0x1 to pass the complex I/O to the ON state, and then check that the state status reaches the ON state (CSI2_COMPLEXIO_CFG[26:25] PWR_STATUS = 0x1) (for complex I/O A).	CSI2_COMPLEXIO_CFG[28:27] PWR_CMD	0x1
Configure the complex I/O: • The complex I/O is fully functional with CSI2_COMPLEX_CFG set at its reset value. • CSI2_COMPLEX_CFG must be changed according to the data rate being used.	CSI2_COMPLEXIO_CFG	
Set RXMODE and STOPSTATE FSM to RXMODE state. Users can also configure the delay for the FSM to return from RXMODE to NORXMODE when all lines reach STOPSTATE.	CSI2_TIMING[15] FORCE_RX_MODE_IO1	0x1
Activate ECC correction and error detection on short packets and packet headers. The ECC check corrects the packet if there is one error and generates an error if there is more than one error (unrecoverable error).	CSI2_CTRL[2] ECC_EN	0x1
Start the CSI2 receiver.	CSI2_CTRL[0] IF_EN	0x1
Configure the different contexts to be used.		
Link the context to a virtual channel and a data type.	See Section 8.2.5.4.6, *Linking a Context to a Virtual Channel and a Data Type.*	
Set the FEC_NUMBER bit field to 0x1 for a progressive video and to 0x2 for an interlaced video. For more information, see Section 8.2.5.3.3.5, *DMA Engine.*	CSI2_CTX_CTRL1_i[26:23] FEC_NUMBER	0x1 or 0x2
Capture an infinite number of frames (until the interface or the context is disabled).	CSI2_CTX_CTRL1_i[15:8] COUNT and CSI2_CTX_CTRL1_i[4] COUNT_UNLOCK	0x0
Enable the CRC checksum on long packet payload. This allows detection of errors, but cannot correct errors like the ECC for header and short packet. On error detection, an event is triggered (the CSI2_CTX_IRQSTATUS_i[5] CS_IRQ bit).	CSI2_CTX_CTRL1_i[5] CS_EN	
Configure the DMA engine for the current channel: Configure the ping and pong addresses.	CSI2_CTX_DAT_PING_ADDR_i[31:5] ADDR and CSI2_CTX_DAT_PING_ADDR_i[31:5] ADDR	
Set the CSI2_CTx_DAT_OFST_i[15:5] OFST bit field to 0x0 so consecutive lines are stored consecutively in memory (image width and frame-buffer width are equal).	CSI2_CTX_DAT_OFST_i[15:5] OFST	
Keep the ALPHA setting at its reset value (0x0) for RGB padding.	CSI2_CTX_CTRL3_i[29:16] ALPHA	

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Table 8-159. ISS CSI2 Global Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Enable the contexts.	CSI2_CTX_CTRL1_i[0] CTX_EN	0x1

8.2.5.4.3 ISS CSI2 Programming Disable Video/Picture Acquisition

There are two ways to end picture acquisition:

- Disable the corresponding context by setting the CSI2_CTX_CTRL1_i[0] CTX_EN bit to 0. This stops the acquisition for the current context. Other enabled contexts are still capturing frames and writing them in memory.
- Disable the CSI2 receiver interface by setting the CSI2_CTRL[0] IF_EN bit to 0. This can have an immediate effect if the CSI2_CTRL[3] FRAME bit is set to 0, or it can be effective after all the enabled contexts receive the FEC if the CSI2_CTRL[3] FRAME bit is set to 1.

8.2.5.4.4 ISS CSI2 Programming Capture a Finite Number of Frames

The CSI2 receiver can be configured to capture a finite number of frames. To configure the CSI2 receiver in this mode, perform the steps listed in Table 8-160.

Table 8-160. ISS CSI2 Capture a Finite Number of Frames

Step	Bit Field	Value
Enable a write to the COUNT bit field.	CSI2_CTX_CTRL1_i[4] COUNT_UNLOCK	0x1
Set the bit field to the number of frames the CSI2 receiver must capture.	CSI2_CTX_CTRL1_i[15:8] COUNT	Valid values are 0 to 255; 0 is infinite capture and 1 to 255 defines the number of frames to capture.
Disable a write to the COUNT bit field.	CSI2_CTX_CTRL1_i[4] COUNT_UNLOCK	0x0

During frame capture, the COUNT bit field is decremented by 1 at each frame capture. Software reads the COUNT bit field to know how many frames must still be captured.

The COUNT bit can be updated during capture if the COUNT_UNLOCK bit is set to 1.

8.2.5.4.5 ISS CSI2 Programming a Periodic Event During Frame Acquisition

The CSI2 receiver can generate a periodic event. This line number is defined in the CSI2_CTX_CTRL3_i[15:0] LINE_NUMBER bit field. The event can be generated once or multiple times per frame, depending on the value of the CSI2_CTX_CTRL1_i[1] LINE_MODULO bit:

- If the LINE_MODULO bit = 0, the event is generated when the line number corresponding to the LINE_NUMBER bit field is received.
- If the LINE_MODULO bit = 1, the event is generated when the line number received corresponds to a multiple of the LINE_NUMBER value (LINE_NUMBER is used as a modulo).

8.2.5.4.6 ISS CSI2 Programming a Context to a Virtual Channel and a Data Type

The CSI2 receiver supports eight contexts and the CSI2 protocol defines four virtual channels. Therefore, a CSI2 receiver context can be associated with a virtual channel and a data type. Virtual channels are defined by a 2-bit field. Valid data types for the CSI2 receiver with their associated values are described in the CSI2_CTX_CTRL2_i[9:0] FORMAT bit field.

For each context, a CSI2_CTX_CTRL2_i register defines with which channel and data type the context is associated:

- The VIRTUAL_ID bit field defines the associated virtual ID transported by the CSI2 protocol from the camera sensor.
- The FORMAT bit field defines the associated data type. The data type is a combination of the data type transported by the CSI2 protocol and the type of storage in memory. A given data type (RGB888)

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can be stored in memory in different ways (RGB888 or RGB888 + EXP32). Therefore, the FORMAT bit field also defines how DMA stores data in memory.

For example, for the current context to capture a frame from virtual channel 2 and data type RAW12 with data expansion (RAW12 + EXP16), write the value 0x10AC (0x2 11 + 0xAC) in the 16 LSBs of the CSI2_CTX_CTRL2_i register.

8.2.5.4.7 ISS CSI2 Programming Progressive and Interleaved Frame Configuration

The CSI2 receiver can treat progressive and interlaced frames. There is no progressive or interleaved mode, but the CSI2_CTX_CTRL1_i[23:16] FEC_NUMBER bit field controls the number of FECs before swapping to the other (ping or pong) buffer. Therefore, two modes are possible:

- FEC_NUMBER = 1: This is equivalent to progressive mode. After a FEC on the context, the current buffer is switched (ping to pong or pong to ping). The image in the memory buffer consists of one transmitted frame.
- FEC_NUMBER 1: The current buffer is switched (ping to pong or pong to ping) after the FEC_NUMBER FEC is received for the context. The image in the memory buffer consists of the FEC_NUMBER transmitted frame.

For more information about how data is stored in memory through the DMA, see Section 8.2.5.3.3.5, *DMA Engine*.

NOTE: If FEC_NUMBER 1, the camera sensor must send the line number information with the current line. Otherwise, the CSI2 receiver cannot calculate each line address.

8.2.5.4.8 ISS CSI2 Programming Progressive and Interleaved Frame Configuration

Table 8-161 lists the procedure to enable debug mode.

Table 8-161. ISS CSI2 Enable Debug Mode

Step	Bit	Value
Enable debug mode.	CSI2_CTRL[7] DBG_EN	0x1

- During debug mode the input does not come from the CSI2 receiver interface but from the CSI2_DBG_H and CSI2_DBG_P registers. The full CSI2 receiver function can be debugged in debug mode. Full 32-bit values must always be written to the CSI2_DBG_H register. The CSI2_CTRL[0] IF_EN bit has no affect during debug mode. To reset the FIFO in case of overflow, the CSI2_CTRL[7] DBG_EN bit must be reset to 0, and the interface must be enabled by setting the CSI2_CTRL[0] IF_EN bit to 0x1.
- The CSI2_DBG_H register is used to provide short packet and long packet headers.
- The CSI2_DBG_P register is used to provide long packet payload.

The following examples apply to the CSI2_DBG_H register:

- The sync codes for virtual channel 0 are written as CSI2_DBG_H = 0xFF00 0000 or 0xFF00 0001, or 0xFF00 0002 or 0xFF00 0003. To send the RAW12 pixels 0x673, 0x452, 0x01d, 0xefc, 0xab0, 0x891, 0x326, 0x547, write CSI2_DBG_H = 0x0123 4567, followed by CSI2_DBG_H = 0x89abcdef, and CSI2_DBG_H = 0x7654 3210.

8.2.5.5 ISS CSI2 Register Manual

8.2.5.5.1 ISS CSI2 Instance Summary

Table 8-162 summarizes the CSI2 instance.

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Table 8-162. ISS CSI2 Instance Summary

Module Name	L3_MAIN Base Address	Size
ISS_CSI2_A_REGS1	0x5200 1000	368 bytes
ISS_CSI2_A_REGS2	0x5200 11C0	64 bytes
ISS_CSI2_B_REGS1	0x5200 1400	368 bytes
ISS_CSI2_B_REGS2	0x5200 15C0	64 bytes
ISS_CSI2_C_REGS1	0x5200 2400	368 bytes
ISS_CSI2_C_REGS2	0x5200 25C0	64 bytes

8.2.5.5.2 ISS CSI2 REGS1 Registers

8.2.5.5.2.1 ISS CSI2 REGS1 Register Summary

Table 8-163 summarizes the CSI2 REGS1 registers.

Table 8-163. ISS CSI2 REGS1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CSI2_A_REGS1 Base Address	ISS_CSI2_B_REGS1 Base Address	ISS_CSI2_C_REGS1 Base Address
CSI2_REVISION	R	32	0x0000 0000	0x5200 1000	0x5200 1400	0x5200 2400
CSI2_SYSCONFIG	RW	32	0x0000 0010	0x5200 1010	0x5200 1410	0x5200 2410
CSI2_SYSSTATUS	R	32	0x0000 0014	0x5200 1014	0x5200 1414	0x5200 2414
CSI2_IRQSTATUS	RW	32	0x0000 0018	0x5200 1018	0x5200 1418	0x5200 2418
CSI2_IRQENABLE	RW	32	0x0000 001C	0x5200 101C	0x5200 141C	0x5200 241C
CSI2_CTRL	RW	32	0x0000 0040	0x5200 1040	0x5200 1440	0x5200 2440
CSI2_DBG_H	W	32	0x0000 0044	0x5200 1044	0x5200 1444	0x5200 2444
RESERVED	R	32	0x0000 0048	0x5200 1048	0x5200 1448	0x5200 2448
RESERVED	RW	32	0x0000 004C	0x5200 104C	0x5200 144C	0x5200 244C
CSI2_COMPLEXIO_CFG	RW	32	0x0000 0050	0x5200 1050	0x5200 1450	0x5200 2450
CSI2_COMPLEXIO_IRQSTATUS	RW	32	0x0000 0054	0x5200 1054	0x5200 1454	0x5200 2454
RESERVED	RW	32	0x0000 0058	0x5200 1058	0x5200 1458	0x5200 2458
CSI2_SHORT_PACKET	R	32	0x0000 005C	0x5200 105C	0x5200 145C	0x5200 245C
CSI2_COMPLEXIO_IRQENABLE	RW	32	0x0000 0060	0x5200 1060	0x5200 1460	0x5200 2460

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Table 8-163. ISS CSI2 REGS1 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CSI2_A_REGS1 Base Address	ISS_CSI2_B_REGS1 Base Address	ISS_CSI2_C_REGS1 Base Address
RESERVED	RW	32	0x0000 0064	0x5200 1064	0x5200 1464	0x5200 2464
CSI2_DBG_P	W	32	0x0000 0068	0x5200 1068	0x5200 1468	0x5200 2468
CSI2_TIMING	RW	32	0x0000 006C	0x5200 106C	0x5200 146C	0x5200 246C
CSI2_CTX_CTRL1_i (1)	RW	32	0x0000 0070 + (0x20 * i)	0x5200 1070 + (0x20 * i)	0x5200 1470 + (0x20 * i)	0x5200 2470 + (0x20 * i)
CSI2_CTX_CTRL2_i (1)	RW	32	0x0000 0074 + (0x20 * i)	0x5200 1074 + (0x20 * i)	0x5200 1474 + (0x20 * i)	0x5200 2474 + (0x20 * i)
CSI2_CTX_DAT_OFST_i (1)	RW	32	0x0000 0078 + (0x20 * i)	0x5200 1078 + (0x20 * i)	0x5200 1478 + (0x20 * i)	0x5200 2478 + (0x20 * i)
CSI2_CTX_DAT_PING_ADDR_i (2)	RW	32	0x0000 007C + (0x20 * i)	0x5200 107C + (0x20 * i)	0x5200 147C + (0x20 * i)	0x5200 247C + (0x20 * i)
CSI2_CTX_DAT_PONG_ADDR_i (2)	RW	32	0x0000 0080 + (0x20 * i)	0x5200 1080 + (0x20 * i)	0x5200 1480 + (0x20 * i)	0x5200 2480 + (0x20 * i)
CSI2_CTX_IRQENABLE_i (2)	RW	32	0x0000 0084 + (0x20 * i)	0x5200 1084 + (0x20 * i)	0x5200 1484 + (0x20 * i)	0x5200 2484 + (0x20 * i)
CSI2_CTX_IRQSTATUS_i (2)	RW	32	0x0000 0088 + (0x20 * i)	0x5200 1088 + (0x20 * i)	0x5200 1488 + (0x20 * i)	0x5200 2488 + (0x20 * i)
CSI2_CTX_CTRL3_i (2)	RW	32	0x0000 008C + (0x20 * i)	0x5200 108C + (0x20 * i)	0x5200 148C + (0x20 * i)	0x5200 248C + (0x20 * i)

(1) i = 0 to 7
(2) i = 0 to 7

8.2.5.5.2.2 ISS CSI2 REGS1 Register Description

through describe the CSI2 REGS1 registers.

Table 8-164. CSI2_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 1000 0x5200 1400 0x5200 2400	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 8-165. Register Call Summary for Register CSI2_REVISION

ISS Interfaces
- ISS CSI2 REGS1 Registers: [0]

Table 8-166. CSI2_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5200 1010 0x5200 1410 0x5200 2410	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	SYSTEM CONFIGURATION REGISTER This register is the OCP-socket system configuration register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MSTANDBY_MODE		RESERVED										SOFT_RESET	AUTO_IDLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:12	MSTANDBY_MODE	Sets the behavior of the master port power management signals. 0x0: Force-standby. MStandby is only asserted when the module is disabled. 0x1: No-standby. MStandby is never asserted. 0x2: Smart-standby: MStandby is asserted based on the activity of the module. The module will try to go to standby during the vertical blanking period.	RW	0x0
11:2	RESERVED		R	0x000
1	SOFT_RESET	Software reset. Set the bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads return 0. 0x0: Normal mode. 0x1: The module is reset Note: Before setting the software reset bit to 1 in CSI2_SYSCONFIG register, the user must have access to a CSI2 receiver register.	RW	0
0	AUTO_IDLE	Internal OCP gating strategy 0x0: OCP clock is free-running. 0x1: Automatic OCP clock gating strategy is applied based on the OCP interface activity.	RW	1

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Table 8-167. Register Call Summary for Register CSI2_SYSCONFIG

ISS Interfaces

- ISS CSI2 Programming Reset Management: [0]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [1] [2]
- ISS CSI2 REGS1 Registers: [3] [4]

Table 8-168. CSI2_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5200 1014 0x5200 1414 0x5200 2414	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	SYSTEM STATUS REGISTER This register provides status information about the module, excluding the interrupt status register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESET_DONE
R-0																															R-1

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	R	0x0000 0000
0	RESET_DONE	Internal reset monitoring Read 0x1: Reset completed. Read 0x0: Internal module reset is on going.	R	1

Table 8-169. Register Call Summary for Register CSI2_SYSSTATUS

ISS Interfaces

- ISS CSI2 REGS1 Registers: [0]

Table 8-170. CSI2_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5200 1018 0x5200 1418 0x5200 2418	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	INTERRUPT STATUS REGISTER - All contexts This register associates one bit for each context in order to determine which context has generated the interrupt. The context must be enabled for events to be generated on that context. If the context is disabled, the interrupt is not generated.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	OCP_ERR_IRQ	SHORT_PACKET_IRQ	ECC_CORRECTION_IRQ	ECC_NO_CORRECTION_IRQ	RESERVED	COMPLEXIO_ERR_IRQ	FIFO_OVF_IRQ	CONTEXT7	CONTEXT6	CONTEXT5	CONTEXT4	CONTEXT3	CONTEXT2	CONTEXT1	CONTEXT0

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	OCP_ERR_IRQ	OCP Error Interrupt 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
13	SHORT_PACKET_IRQ	Short packet reception status (other than synch events: Line Start, Line End, Frame Start, and Frame End: data type between 0x8 and x0F only must be considered). 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
12	ECC_CORRECTION_IRQ	ECC has been used to do the correction of the only 1-bit error status (short packet only). 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
11	ECC_NO_CORRECTION_IRQ	ECC error status (short and long packets). No correction of the header because of more than 1-bit error. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	RESERVED	Reserved	R	0
9	COMPLEXIO_ERR_IRQ	Error signaling from complex I/O: status of the PHY errors received from the complex I/O (events are defined in CSI2_COMPLEXIO_IRQSTATUS for the complex I/O). Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
8	FIFO_OVF_IRQ	FIFO overflow error status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
7	CONTEXT7	Context 7 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
6	CONTEXT6	Context 6 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0

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Bits	Field Name	Description	Type	Reset
5	CONTEXT5	Context 5 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
4	CONTEXT4	Context 4 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
3	CONTEXT3	Context 3 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
2	CONTEXT2	Context 2 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
1	CONTEXT1	Context 1 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0
0	CONTEXT0	Context 0 Read 0x1: READS: Event is true (pending). Read 0x0: READS: Event is false.	R	0

Table 8-171. Register Call Summary for Register CSI2_IRQSTATUS

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1] [2] [3]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [4]
- ISS CSI2 REGS1 Registers: [5]

Table 8-172. CSI2_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x5200 101C 0x5200 141C 0x5200 241C	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	INTERRUPT ENABLE REGISTER - All contexts This register associates one bit for each context in order to enable/disable each context individually.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OCP_ERR_IRQ	SHORT_PACKET_IRQ	ECC_CORRECTION_IRQ	ECC_NO_CORRECTION_IRQ	RESERVED	COMPLEXIO_ERR_IRQ	FIFO_OVF_IRQ	CONTEXT7	CONTEXT6	CONTEXT5	CONTEXT4	CONTEXT3	CONTEXT2	CONTEXT1	CONTEXT0	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	OCP_ERR_IRQ	OCP Error Interrupt 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
13	SHORT_PACKET_IRQ	Short packet reception (other than synch events: Line Start, Line End, Frame Start, and Frame End: data type between 0x8 and x0F only must be considered). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
12	ECC_CORRECTION_IRQ	ECC has been used to correct the only 1-bit error (short packet only). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
11	ECC_NO_CORRECTION_IRQ	ECC error (short and long packets). No correction of the header because of more than 1-bit error. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	RESERVED	Reserved	RW	0
9	COMPLEXIO_ERR_IRQ	Error signaling from complex I/O: the interrupt is triggered when any error is received from the complex I/O (events are defined in CSI2_COMPLEXIO_IRQSTATUS for the complex I/O). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	FIFO_OVF_IRQ	FIFO overflow enable 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	CONTEXT7	Context 7 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	CONTEXT6	Context 6 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
5	CONTEXT5	Context 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	CONTEXT4	Context 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	CONTEXT3	Context 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	CONTEXT2	Context 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	CONTEXT1	Context 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	CONTEXT0	Context 0 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Table 8-173. Register Call Summary for Register CSI2_IRQENABLE

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [2] [3]
- ISS CSI2 REGS1 Registers: [4]

Table 8-174. CSI2_CTRL

Address Offset	0x0000 0040		
Physical Address	0x5200 1040 0x5200 1440 0x5200 2440	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	GLOBAL CONTROL REGISTER This register controls the CSI2 RECEIVER module. This register must not be modified dynamically (except IF_EN bit field).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															BURST_SIZE_EXPAND	VP_CLK_EN	RESERVED	NON_POSTED_WRITE	RESERVED	VP_ONLY_EN	STREAMING_32_BIT	VP_OUT_CTRL		DBG_EN	BURST_SIZE		ENDIANNESS	FRAME	ECC_EN	RESERVED	IF_EN

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved	R	0x000
24:23	BYS_CLK_CTRL	Controls the pixel clock sent to the BYS output port 0x0: Clock disabled (tied to 0) 0x1: PCLK=FCLK 0x3: reserved. 0x2: PCLK=FCLK/2	RW	0x0
22:17	RESERVED	Reserved	R	0x0000
16	BURST_SIZE_EXPAND	Sets the DMA burst size on the L3 interconnect. 0x0: Use the burst size defined in the BURST_SIZE register 0x1: Allow generation of 16x64-bit bursts	RW	0
15	VP_CLK_EN	VP clock enable. 0x0: The VP clock is disabled. 0x1: The VP clock is enabled.	RW	0
14	RESERVED	Read returns reset value	RW	0
13	NON_POSTED_WRITE	Not posted writes 0x0: Disable 0x1: Enable	RW	0
12	PWRSCPCLK	Controls autogating of the PWRSCP clock 0x0: PWRSCP clock is automatically cut when it isn't needed. 0x1: PWRSCP clock is free running	RW	0

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Bits	Field Name	Description	Type	Reset
11	VP_ONLY_EN	VP only enable. 0x0: The VP is enabled and the OCP master port is enabled. 0x1: The VP is enabled and the OCP master port is disabled.	RW	0
10	STREAMING_32_BIT	Indicates if 64-bit or 32-bit streaming burst is used. Valid only if CSI2_CTRL.STREAMING=1 0x0: 64-bit streaming burst is used; byte enable pattern is 0xFF 0x1: 32-bit streaming burst is used; byte enable pattern is 0x0F	RW	0
9:8	VP_OUT_CTRL	VP_PCLK control. Sets the VP_PCLK as a function of the ISS interconnect interface clock (OCPCLK). 0x0: No division: VP_PCLK = OCPCLK. 0x1: Division by 2: VP_PCLK = OCPCLK / 2. 0x3: Division by 4: VP_PCLK = OCPCLK / 4. 0x2: Division by 3: VP_PCLK = OCPCLK / 3. Example scenarios: - Low VP_PCLK, Memory -> VP: Same as typical memory -> VP, but VP_PCLK = OCPCLK/2 - Typical sensor -> VP: Autoidle enabled, FCLK at optimal rate, sensor provides DPCM compressed RAW12 data at 650 Mbps. Image timings VP_PCLK = (OCPCLK/2) and CCP2_CTRL[31:15] FRACDIV = 0xD000 2600 active pixels/line, 128 blanking pixels, no vertical blanking. (This scenario corresponds to the OTF operation at maximum CCP2 speed.)	RW	0x0
7	DBG_EN	Enables the debug mode. 0x0: Disable 0x1: Enable	RW	0
6:5	BURST_SIZE	Sets the DMA burst size on the L3 interconnect. 0x0: 1x64 OCP writes 0x1: 2x64 OCP writes 0x3: 8x64 OCP writes 0x2: 4x64 OCP writes	RW	0x0
4	ENDIANNESS	Select endianness for YUV4:2:2 8 bit and YUV4:2:0 legacy formats. 0x0: Use native MIPI CSI2 endianness: Little endian for all formats except for YUV4:2:2 8b and YUV4:2:0 Legacy which a big endian. 0x1: Store all pixel formats little endian.	RW	0
3	FRAME	Set the modality in which IF_EN works. 0x0: If IF_EN = 0 the interface is disabled immediately. 0x1: If IF_EN = 1 the interface is disabled after all FEC sync code have been received for the active contexts.	RW	0
2	ECC_EN	Enables the Error Correction Code check for the received header (short and long packets for all virtual channel ids). 0x0: Disabled 0x1: Enabled	RW	0
1	RESERVED	Read returns reset value	RW	0

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Bits	Field Name	Description	Type	Reset
0	IF_EN	Enables the physical interface to the module. 0x0: The interface is disabled. If FRAME = 0, it is disabled immediately. If FRAME = 1, it is disabled when each context has received the FEC sync code. 0x1: The interface is enabled immediately, the data acquisition starts on the next FSC sync code. Writing 1 to this register when the current value is 0 has the effect to clear the output FIFO. The pixel data of the following frame will be written in the PING buffer, that is, the CSI2_CTX_CTRL1_i.PING_PONG bits are reset to 0 as well.	RW	0

Table 8-175. Register Call Summary for Register CSI2_CTRL

ISS Interfaces

- ISS CCP2 Programming Burst Settings: [0] [1]
- ISS CSI2 Protocol and Data Format: [2] [3]
- ISS CSI2 Functional Description: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [23] [24]
- ISS CSI2 Programming Disable Video/Picture Acquisition: [25] [26] [27]
- ISS CSI2 Programming Progressive and Interleaved Frame Configuration: [28] [29] [30] [31]
- ISS CSI2 REGS1 Registers: [32] [33] [34] [35] [36] [37]

Table 8-176. CSI2_DBG_H

Address Offset	0x0000 0044		
Physical Address	0x5200 1044 0x5200 1444 0x5200 2444	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	DEBUG REGISTER (Header) This register provides a way to debug the CSI2 RECEIVER module with no image sensor connected to the module. The debug mode is enabled by CSI2_CTRL.DBG_EN. Only full 32-bit values must be written. The register is used to write short packets and header of long packets.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBG																															

Bits	Field Name	Description	Type	Reset
31:0	DBG	32-bit input value.	W	0x0000 0000

Table 8-177. Register Call Summary for Register CSI2_DBG_H

ISS Interfaces

- ISS CSI2 Programming Progressive and Interleaved Frame Configuration: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS CSI2 REGS1 Registers: [8]

Table 8-178. CSI2_COMPLEXIO_CFG

Address Offset	0x0000 0050		
Physical Address	0x5200 1050 0x5200 1450 0x5200 2450	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	COMPLEXIO CONFIGURATION REGISTER for the complex I/O This register contains the lane configuration for the order and position of the lanes (clock and data) and the polarity order for the control of the PHY differential signals in addition to the control bit for the power FSM.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESET_CTRL	RESET_DONE	PWR_CMD		PWR_STATUS		PWR_AUTO	RESERVED				DATA4_POL	DATA4_POSITION			DATA3_POL	DATA3_POSITION			DATA2_POL	DATA2_POSITION			DATA1_POL	DATA1_POSITION			CLOCK_POL	CLOCK_POSITION		

Bits	Field Name	Description	Type	Reset
31	PHY_REG_BANK	Selects among registers 0÷7 and 8÷15 when accessing PHY registers via the SCP bus. 0x0: 0÷7 0x1: 8÷15	RW	0
30	RESET_CTRL	Controls the reset of the complex I/O 0x0: Complex I/O reset active. 0x1: Complex I/O reset deasserted.	RW	0
29	RESET_DONE	Internal reset monitoring of the power domain using the byte clock provided by the associated CSIPHY (see Section 8.1.1.1.1, *ISS Clock Domains*. **Caution:** For the CSI2_COMPLEXIO_CFG[29] RESET_DONE bit to be set to 0x1 (reset completed), the external sensor must to be active and sending the MIPI HS BYTECLK. Read 0x1: Reset completed. Read 0x0: Internal module reset is ongoing.	R	0
28:27	PWR_CMD	Command for power control of the complex I/O 0x0: Command to change to OFF state 0x1: Command to change to ON state 0x2: Command to change to Ultralow-Power state	RW	0x0
26:25	PWR_STATUS	Status of the power control of the complex I/O Read 0x2: Complex I/O in Ultralow-Power state Read 0x1: Complex I/O in ON state Read 0x0: Complex I/O in OFF state	R	0x0
24	PWR_AUTO	Automatic switch between ULP and ON states based on ULPM signals from complex I/O 0x0: Disable 0x1: Enable	RW	0
23:20	RESERVED		R	0x0
19	DATA4_POL	+/- differential pin order of data lane 4. 0x0: +/- pin order 0x1: -/+ pin order	RW	0

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Bits	Field Name	Description	Type	Reset
18:16	DATA4_POSITION	Position and order of the data lane 4. The values 6 and 7 are reserved. This lane is not available for CSI2_B and CSI2_C receivers. 0x0: This data lane is not used. 0x1: Data lane 4 is at position 1. This position is not available to the CSI2_B and CSI2_C receivers. 0x2: Data lane 4 is at position 2. This position is not available to the CSI2_B and CSI2_C receivers. 0x3: Data lane 4 is at position 3. This position is not available to the CSI2_B and CSI2_C receivers. 0x4: Data lane 4 is at position 4. This position is not available to the CSI2_B and CSI2_C receivers. 0x5: Data lane 4 is at position 5. This position is not available to the CSI2_B and CSI2_C receivers. 0x6: Reserved 0x7: Reserved	RW	0x0
15	DATA3_POL	+/- differential pin order of data lane 3. 0x0: +/- pin order 0x1: -/+ pin order	RW	0
14:12	DATA3_POSITION	Position and order of the data lane 3. The values 6 and 7 are reserved. This lane is not available for CSI2_B and CSI2_C receivers. 0x0: This data lane is not used. 0x1: Data lane 3 is at position 1. This position is not available to the CSI2_B and CSI2_C receivers. 0x2: Data lane 3 is at position 2. This position is not available to the CSI2_B and CSI2_C receivers. 0x3: Data lane 3 is at position 3. This position is not available to the CSI2_B and CSI2_C receivers. 0x4: Data lane 3 is at position 4. This position is not available to the CSI2_B and CSI2_C receivers. 0x5: Data lane 3 is at position 5. This position is not available to the CSI2_B and CSI2_C receivers. 0x6: Reserved 0x7: Reserved	RW	0x0
11	DATA2_POL	+/- differential pin order of DATA lane 2. 0x0: +/- pin order (csi2_dx=+ and csi2_dy=-) 0x1: -/+ pin order (csi2_dx=- and csi2_dy=+)	RW	0
10:8	DATA2_POSITION	Position and order of the data lane 2. The values 6 and 7 are reserved. This lane is not available for the CSI2_C receiver. 0x0: This data lane is not used. 0x1: Data lane 2 is at position 1. This position is not available to the CSI2_C receiver. 0x2: Data lane 2 is at position 2. This position is not available to the CSI2_C receiver. 0x3: Data lane 2 is at position 3. This position is not available to the CSI2_C receiver. 0x4: Data lane 2 is at position 4. This position is not available to the CSI2_B and CSI2_C receivers. 0x5: Data lane 2 is at position 5. This position is not available to the CSI2_B and CSI2_C receivers. 0x6: Reserved 0x7: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
7	DATA1_POL	+/- differential pin order of data lane 1. 0x0: +/- pin order (csi2_dx=+ and csi2_dy=-) 0x1: -/+ pin order (csi2_dx=- and csi2_dy=+)	RW	0
6:4	DATA1_POSITION	Position and order of the DATA lane 1. The values 6 and 7 are reserved. When CSI2 is used, the data lane 1 position must be different from 0, 6, or 7. 0x0: This data lane is not used. 0x1: Data lane 1 is at position 1. x2: Data lane 1 is at position 2. 0x3: Data lane 1 is at position 3. This position is not available to the CSI2_C receiver. 0x4: Data lane 1 is at position 4. This position is not available to the CSI2_B and CSI2_C receivers. 0x5: Data lane 1 is at position 5. This position is not available to the CSI2_B and CSI2_C receivers. 0x6: Reserved 0x7: Reserved	RW	0x0
3	CLOCK_POL	+/- differential pin order of clock lane. 0x0: +/- pin order (csi2_dx=+ and csi2_dy=-) 0x1: -/+ pin order (csi2_dx=- and csi2_dy=+)	RW	0
2:0	CLOCK_POSITION	Position and order of the clock lane. The values 5, 6, and 7 are reserved. When CSI2 is used, the clock lane position must be different from 0, 5, 6, or 7. 0x0: This data lane is not used. 0x1: Clock lane is at position 1. 0x2: Clock lane is at position 2. 0x3: Clock lane is at position 3. This position is not available to the CSI2_C receiver. 0x4: Clock lane is at position 4. This position is not available to the CSI2_B and CSI2_C receivers. 0x5: Reserved 0x6: Reserved 0x7: Reserved	RW	0x0

Table 8-179. Register Call Summary for Register CSI2_COMPLEXIO_CFG

ISS Interfaces

- ISS CSI PHY Functional Configuration: [0] [1] [2]
- ISS CSI PHY (D-PHY Mode) and Link Initialization Sequence: [3] [4] [5] [6] [7] [8] [9] [10] [11]
- ISS CSI PHY (CCP2 Mode) and Link Initialization Sequence: [12] [13] [14] [15] [16]
- ISS CSI2 Protocol and Data Format: [17] [18]
- ISS CSI2 Functional Description: [19] [20] [21]
- ISS CSI2 Programming Reset Management: [22]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [23] [24] [25] [26]
- ISS CSI2 REGS1 Registers: [27] [28]

Table 8-180. CSI2_COMPLEXIO_IRQSTATUS

Address Offset	0x0000 0054		
Physical Address	0x5200 1054 0x5200 1454 0x5200 2454	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	INTERRUPT STATUS REGISTER - All errors from complex I/O #1		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					STATEALLULPMEXIT	STATEALLULPMENTER	STATEULPM5	STATEULPM4	STATEULPM3	STATEULPM2	STATEULPM1	ERRCONTROL5	ERRCONTROL4	ERRCONTROL3	ERRCONTROL2	ERRCONTROL1	ERRESC5	ERRESC4	ERRESC3	ERRESC2	ERRESC1	ERRSOTSYNCHS5	ERRSOTSYNCHS4	ERRSOTSYNCHS3	ERRSOTSYNCHS2	ERRSOTSYNCHS1	ERRSOTHS5	ERRSOTHS4	ERRSOTHS3	ERRSOTHS2	ERRSOTHS1

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	STATEALLULPMEXIT	At least one of the active lanes has exit the ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
25	STATEALLULPMENTER	All active lanes are entering in ULPM. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
24	STATEULPM5	Lane 5 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
23	STATEULPM4	Lane 4 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
22	STATEULPM3	Lane 3 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
21	STATEULPM2	Lane 2 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
20	STATEULPM1	Lane 1 in ULPM 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
19	ERRCONTROL5	Control error for lane 5 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
18	ERRCONTROL4	Control error for lane 4 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
17	ERRCONTROL3	Control error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
16	ERRCONTROL2	Control error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
15	ERRCONTROL1	Control error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
14	ERRESC5	Escape entry error for lane 5 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
13	ERRESC4	Escape entry error for lane 4 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
12	ERRESC3	Escape entry error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
11	ERRESC2	Escape entry error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	ERRESC1	Escape entry error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
9	ERRSOTSYNCHS5	Start of transmission sync error for lane 5 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
8	ERRSOTSYNCHS4	Start of transmission sync error for lane 4 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
7	ERRSOTSYNCHS3	Start of transmission sync error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
6	ERRSOTSYNCHS2	Start of transmission sync error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
5	ERRSOTSYNCHS1	Start of transmission sync error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	ERRSOTHS5	Start of transmission error for lane 5 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
3	ERRSOTHS4	Start of transmission error for lane 4 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
2	ERRSOTHS3	Start of transmission error for lane 3 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
1	ERRSOTHS2	Start of transmission error for lane 2 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	ERRSOTHS1	Start of transmission error for lane 1 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

Table 8-181. Register Call Summary for Register CSI2_COMPLEXIO_IRQSTATUS

ISS Interfaces

- ISS CSI PHY Functional Configuration: [0]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [1]
- ISS CSI2 REGS1 Registers: [2] [3] [4]

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Table 8-182. CSI2_SHORT_PACKET

Address Offset	0x0000 005C		
Physical Address	0x5200 105C 0x5200 145C 0x5200 245C	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	SHORT PACKET INFORMATION - This register sets the 24-bit DATA_ID + Short Packet Data Field when the data type is between 0x8 and x0F		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SHORT_PACKET																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reads returns 0.	R	0x00
23:0	SHORT_PACKET	Short Packet information: DATA ID + DATA FIELD	R	0x000000

Table 8-183. Register Call Summary for Register CSI2_SHORT_PACKET

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 REGS1 Registers: [2]

Table 8-184. CSI2_COMPLEXIO_IRQENABLE

Address Offset	0x0000 0060		
Physical Address	0x5200 1060 0x5200 1460 0x5200 2460	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	INTERRUPT ENABLE REGISTER - All errors from complex I/O		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					STATEALLULPMEXIT	STATEALLULPMENTER	STATEULPM5	STATEULPM4	STATEULPM3	STATEULPM2	STATEULPM1	ERRCONTROL5	ERRCONTROL4	ERRCONTROL3	ERRCONTROL2	ERRCONTROL1	ERRESC5	ERRESC4	ERRESC3	ERRESC2	ERRESC1	ERRSOTSYNCHS5	ERRSOTSYNCHS4	ERRSOTSYNCHS3	ERRSOTSYNCHS2	ERRSOTSYNCHS1	ERRSOTHS5	ERRSOTHS4	ERRSOTHS3	ERRSOTHS2	ERRSOTHS1

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	STATEALLULPMEXIT	At least one of the active lanes has exit the ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
25	STATEALLULPMENTER	All active lanes are entering in ULPM. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
24	STATEULPM5	Lane 5 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
23	STATEULPM4	Lane 4 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
22	STATEULPM3	Lane 3 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
21	STATEULPM2	Lane 2 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
20	STATEULPM1	Lane 1 in ULPM 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
19	ERRCONTROL5	Control error for lane 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
18	ERRCONTROL4	Control error for lane 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
17	ERRCONTROL3	Control error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
16	ERRCONTROL2	Control error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
15	ERRCONTROL1	Control error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
14	ERRESC5	Escape entry error for lane 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
13	ERRESC4	Escape entry error for lane 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
12	ERRESC3	Escape entry error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
11	ERRESC2	Escape entry error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	ERRESC1	Escape entry error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
9	ERRSOTSYNCHS5	Start of transmission sync error for lane 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	ERRSOTSYNCHS4	Start of transmission sync error for lane 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
7	ERRSOTSYNCHS3	Start of transmission sync error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	ERRSOTSYNCHS2	Start of transmission sync error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
5	ERRSOTSYNCHS1	Start of transmission sync error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	ERRSOTHS5	Start of transmission error for lane 5 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	ERRSOTHS4	Start of transmission error for lane 4 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	ERRSOTHS3	Start of transmission error for lane 3 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	ERRSOTHS2	Start of transmission error for lane 2 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	ERRSOTHS1	Start of transmission error for lane 1 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 8-185. Register Call Summary for Register CSI2_COMPLEXIO_IRQENABLE

ISS Interfaces

- ISS CSI2 Programming Enable Video/Picture Acquisition: [0]
- ISS CSI2 REGS1 Registers: [1]

Table 8-186. CSI2_DBG_P

Address Offset	0x0000 0068		
Physical Address	0x5200 1068 0x5200 1468 0x5200 2468	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	DEBUG REGISTER (Payload) This register provides a way to debug the CSI2 RECEIVER module with no image sensor connected to the module. The debug mode is enabled by CSI2_CTRL.DBG_EN. Only full 32-bit values must be written. The register is used to write payload of long packets.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBG																															

Bits	Field Name	Description	Type	Reset
31:0	DBG	32-bit input value.	W	0x0000 0000

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Table 8-187. Register Call Summary for Register CSI2_DBG_P

ISS Interfaces

- ISS CSI2 Programming Progressive and Interleaved Frame Configuration: [0] [1]
- ISS CSI2 REGS1 Registers: [2]

Table 8-188. CSI2_TIMING

Address Offset	0x0000 006C		
Physical Address	0x5200 106C 0x5200 146C 0x5200 246C	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	TIMING REGISTER This register controls the CSI2 RECEIVER module. This register must not be modified while CSI2_CTRL.IF_EN is set to 1. It is used to indicate the number of L3 cycles for the Stop State monitoring.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			RESERVED													FORCE_RX_MODE_IO1	STOP_STATE_X16_IO1	STOP_STATE_X4_IO1	STOP_STATE_COUNTER_IO1														

Bits	Field Name	Description	Type	Reset
31	RESERVED	Read returns reset value	RW	0
30	RESERVED	Read returns reset value	RW	1
29	RESERVED	Read returns reset value	RW	1
28:16	RESERVED	Read returns reset value	RW	0x1FFF
15	FORCE_RX_MODE_IO1	Control of ForceRxMode signal 0x0: Deassertion of ForceRxMode. The hardware reset the bit at the end of the Force RX Mode assertion. The software can reset the bit in order to stop the assertion of the ForceRXMode signal prior to the completion of the period. 0x1: Assertion of ForceRxMode	RW	0
14	STOP_STATE_X16_IO1	Multiplication factor for the number of L3 cycles defined in STOP_STATE_COUNTER bit field 0x0: The number of L3 cycles defined in STOP_STATE_COUNTER is multiplied by 1x 0x1: The number of L3 cycles defined in STOP_STATE_COUNTER is multiplied by 16x	RW	1
13	STOP_STATE_X4_IO1	Multiplication factor for the number of L3 cycles defined in STOP_STATE_COUNTER bit field 0x0: The number of L3 cycles defined in STOP_STATE_COUNTER is multiplied by 1x 0x1: The number of L3 cycles defined in STOP_STATE_COUNTER is multiplied by 4x	RW	1
12:0	STOP_STATE_COUNTER_IO1	Stop State counter for monitoring. It indicates the number of L3 to monitor for Stop State before deasserting ForceRxMode (complex I/O 1). The value is from 0 to 8191.	RW	0x1FFF

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Table 8-189. Register Call Summary for Register CSI2_TIMING

ISS Interfaces

- ISS CSI PHY Functional Configuration: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS CSI PHY (D-PHY Mode) and Link Initialization Sequence: [8] [9] [10]
- ISS CSI PHY (CCP2 Mode) and Link Initialization Sequence: [11] [12]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [13]
- ISS CSI2 REGS1 Registers: [14]

Table 8-190. CSI2_CTX_CTRL1_i

Address Offset	0x0000 0070 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1070 + (0x20 * i) 0x5200 1470 + (0x20 * i) 0x5200 2470 + (0x20 * i)	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	CONTROL REGISTER - Context This register controls the Context. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTESWAP	GENERIC	BYS	HSCALE	TRANSCODE				FEC_NUMBER								COUNT								EOF_EN	EOL_EN	CS_EN	COUNT_UNLOCK	PING_PONG	VP_FORCE	LINE_MODULO	CTX_EN

Bits	Field Name	Description	Type	Reset
31	BYTESWAP	Allows swapping bytes two by two in the payload data. It does not affect: - short packets - long packet header or footers - CRC calculation The purpose is to by swap data send to the OCP port and/or video port 0x0: Disabled 0x1: Enabled	RW	0
30	GENERIC	Enables the generic mode. 0x0: Disabled. Data is received according to CSI2_CTX_CTRL2_i.FORMAT and the long packet code transmitted in the MIPI stream is used. 0x1: Enabled. Data is received according to CSI2_CTX_CTRL2_i.FORMAT and the long packet code transmitted in the MIPI stream is ignored.	RW	0
29	BYS	Controls BYS port. Must be 0 when TRANSCODE=0 0x0: Disabled. Data from the HSCALER is forwarded to the video port and/or OCP port 0x1: Enabled Data from the HSCALER is send to the BYS output port. Data received on the BYS input port is forwarded to the video port and/or OCP port	RW	0

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Bits	Field Name	Description	Type	Reset
28	HSCALE	Enable horizontal downscaling by a factor of two. Applies to RAW data when transcoding is enabled. Must be disabled when transcoding is disabled. 0x0: Disable 0x1: Enable	RW	0x0
27:24	TRANSCODE	Enables image transcoding. When this features is enabled: - the data format from the camera is defined by the FORMAT register - the format after transcode is defined by the TRANSCODE register. The memory storage / video port formats is defined by the TRANSCODE register 0x6: Outputs uncompressed RAW10 data. Data in memory is organized as regular packed RAW10 data 0x1: Outputs DPCM compressed RAW10 data. After compression, pixels are coded on 8 bits. Data in memory is organized as regular RAW8 data 0x7: Outputs uncompressed RAW12 data. Data in memory is organized as regular RAW12+EXP16 data 0x0: Feature disabled. 0x2: Outputs DPCM compressed RAW12 data. After compression, pixels are coded on 8 bits. Data in memory is organized as regular RAW8 data 0x8: Outputs uncompressed RAW12 data. Data in memory is organized as regular packed RAW12 data 0x9: Outputs uncompressed RAW14 data. 0x4: Outputs uncompressed RAW8 data. Data in memory is organized as regular RAW8 data 0x5: Outputs uncompressed RAW10 data. Data in memory is organized as regular RAW10+EXP16 data 0x3: Outputs A-Law compressed RAW10 data. After compression, pixels are coded on 8 bits. Data in memory is organized as regular RAW8 data.	RW	0x0
23:16	FEC_NUMBER	Number of FEC to receive between using swap of CSI2_CTX_DAT_PING_ADDR_i and CSI2_CTX_DAT_PONG_ADDR_i for the calculation of the address in memory (must be used only in interlace mode, otherwise set to 1).	RW	0x01
15:8	COUNT	Sets the number of frame to acquire. Once the frame acquisition starts, the COUNT value is decremented after every frame. When COUNT reaches 0, the FRAME_NUMBER_IRQ interrupt is triggered and CTX_EN bit is set to 0. Writes to this bit field are controlled by the COUNT_UNLOCK bit. During the same OCP write access, the bit field COUNT_UNLOCK must be written in addition to COUNT bit field in order to change the COUNT value. COUNT can be overwritten dynamically with a new count value. 0: Infinite number of frames (no count). 1: 1 frame to acquire ... 255: 255 frames to acquire	RW	0x00
7	EOF_EN	Indicates if the end of frame signal must be asserted at the end of the line. Read 0x1: The end of frame signal is asserted at the end of each frame. Read 0x0: The end of frame signal is not asserted at the end of each frame.	RW	0

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Bits	Field Name	Description	Type	Reset
6	EOL_EN	Indicates if the end of line signal must be asserted at the end of the line. Read 0x1: The end of line signal is asserted at the end of each frame. Read 0x0: The end of line signal is not asserted at the end of each frame.	RW	0
5	CS_EN	Enables the checksum check for the received payload (long packet only). 0x0: Disabled 0x1: Enabled	RW	0
4	COUNT_UNLOCK	Unlock writes to the COUNT bit field. Write 0x0: COUNT bit field is locked. Writes have no effect Write 0x1: COUNT bit field is unlocked. Writes are possible.	W	0
3	PING_PONG	Indicates whether the PING or PONG destination address (CSI2_CTX_DAT_PING_ADDR_i or CSI2_CTX_DAT_PONG_ADDR_i) was used to write the last frame. This bit field toggles after every FEC_NUMBER FEC sync code received for the current context. Read 0x1: PONG buffer Read 0x0: PING buffer	R	1
2	VP_FORCE	Forces sending of the data to both VPORT and OCP. Only applies to formats that existing in two versions: - One sending data to OCP port only - One sending data to VPORT only (tagged with the +VP extension) The format version sending data only to OCP should be chosen. When VP_FORCE is set, the data is sent to video port and to OCP port, no matter is format +VP or not (RAW8 + DPCM10 + VP or RAW8 + DPCM10 + EXP16). If this bit is cleared, data is only sent to one destination, so if the format is RAW8 + DPCM10 + VP, the data will be sent only to video port and if the format is RAW8 + DPCM10 + EXP16, the data will be sent only to OCP port. If CSI2_CTRL[11] VP_ONLY_EN bit is set, no data will be send to the OCP port although VP_FORCE is set. 0x0: Disabled 0x1: Enabled	RW	0
1	LINE_MODULO	Line modulo configuration 0x0: CSI2_CTX_CTRL3_i.LINE_NUMBER is used once per frame for the generation of the LINE_NUMBER_IRQ. 0x1: CSI2_CTX_CTRL3_i.LINE_NUMBER is used as a modulo number for the generation of the LINE_NUMBER_IRQ (multiple times the interrupt can be generated for each frame)	RW	0
0	CTX_EN	Enables the context 0x0: Disabled 0x1: Enabled	RW	0

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Table 8-191. Register Call Summary for Register CSI2_CTX_CTRL1_i

ISS Interfaces

- ISS CSI2 Protocol and Data Format: [0]
- ISS CSI2 Functional Description: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [20] [21] [22] [23] [24]
- ISS CSI2 Programming Disable Video/Picture Acquisition: [25]
- ISS CSI2 Programming Capture a Finite Number of Frames: [26] [27] [28]
- ISS CSI2 Programming a Periodic Event During Frame Acquisition: [29]
- ISS CSI2 Programming Progressive and Interleaved Frame Configuration: [30]
- ISS CSI2 REGS1 Registers: [31] [32] [33] [34] [35]

Table 8-192. CSI2_CTX_CTRL2_i

Address Offset	0x0000 0074 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1074 + (0x20 * i) 0x5200 1474 + (0x20 * i) 0x5200 2474 + (0x20 * i)	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	CONTROL REGISTER - Context This register controls the Context. This register is shadowed: modifications are taken into account after the next FSC sync code (except for VIRTUAL_ID and FORMAT fields). The change of VIRTUIAL_ID and FORMAT has to occur only when the context is disabled (CSI2_CTX_CTRL1_i.CTX_EN).		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14 13	12 11	10	9 8	7 6 5 4 3 2 1 0
FRAME		RESERVED	USER_DEF_MAPPING	VIRTUAL_ID	DPCM_PRED		FORMAT

Bits	Field Name	Description	Type	Reset
31:16	FRAME	Frame number The CSI-2 protocol engine extracts the frame number from the SOF short packet sent by the camera.	R	0x0000
15	RESERVED		R	0
14:13	USER_DEF_MAPPING	Selects the pixel format of USER_DEFINED in FORMAT 0x0: RAW6 0x1: RAW7 0x2: RAW8 (not valid if FORMAT is USER_DEFINED_8_BIT_DATA_TYPE_x_EXP8 with x from 1 to 8)	RW	0x0
12:11	VIRTUAL_ID	Virtual channel ID 0x0: Virtual Channel ID 0 0x1: Virtual Channel ID 1 0x3: Virtual Channel ID 3 0x2: Virtual Channel ID 2	RW	0x0
10	DPCM_PRED	Selects the DPCM predictor. 0x0: The advanced predictor is used. Not supported for 10- 8- 10 algorithm. Performance limited to 1 pixel/cycle. 0x1: The simple predictor is used.	RW	0
9:0	FORMAT	Data format selection. 0x3A9: RAW7 DPCM12 + VP	RW	0x000

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Bits	Field Name	Description	Type	Reset
		0x80: USER_DEFINED_8_BIT_DATA_TYPE_1 + EXP8		
		0x84: USER_DEFINED_8_BIT_DATA_TYPE_5 + EXP8		
		0x346: USER_DEFINED_8_BIT_DATA_TYPE_7 + DPCM10 + VP		
		0x1D: YUV4:2:0 10bit + CSPS		
		0x2C6: USER_DEFINED_8_BIT_DATA_TYPE_7 + DPCM10 + EXP16		
		0x41: USER_DEFINED_8_BIT_DATA_TYPE_2		
		0x1C5: USER_DEFINED_8_BIT_DATA_TYPE_6_DPCM12_EXP16		
		0xAC: RAW12 + EXP16		
		0x145: USER_DEFINED_8_BIT_DATA_TYPE_6_DPCM12_VP		
		0x12: Embedded 8-bit nonimage data (that is, JPEG)		
		0x46: USER_DEFINED_8_BIT_DATA_TYPE_7		
		0x83: USER_DEFINED_8_BIT_DATA_TYPE_4 + EXP8		
		0x2B: RAW10		
		0x9E: YUV4:2:2 8bit + VP		
		0x1C0: USER_DEFINED_8_BIT_DATA_TYPE_1_DPCM12_EXP16		
		0x140: USER_DEFINED_8_BIT_DATA_TYPE_1_DPCM12_VP		
		0x329: RAW7 + DPCM10 + VP		
		0x22: RGB565		
		0x68: RAW6 + EXP8		
		0x43: USER_DEFINED_8_BIT_DATA_TYPE_4		
		0xE3: RGB666 + EXP32		
		0x1C7: USER_DEFINED_8_BIT_DATA_TYPE_8_DPCM12_EXP16		
		0x143: USER_DEFINED_8_BIT_DATA_TYPE_4_DPCM12_VP		
		0xA0: RGB444 + EXP16		
		0x87: USER_DEFINED_8_BIT_DATA_TYPE_8 + EXP8		
		0x85: USER_DEFINED_8_BIT_DATA_TYPE_6 + EXP8		
		0x0: OTHERS (except NULL and BLANKING packets)		
		0x341: USER_DEFINED_8_BIT_DATA_TYPE_2 + DPCM10 + VP		
		0xAD: RAW14 + EXP16		
		0x2C3: USER_DEFINED_8_BIT_DATA_TYPE_4 + DPCM10 + EXP16		
		0xE4: RGB888 + EXP32		
		0x343: USER_DEFINED_8_BIT_DATA_TYPE_4 + DPCM10 + VP		
		0x368: RAW6 DPCM12 + VP		
		0x12C: RAW12 + VP		
		0x42: USER_DEFINED_8_BIT_DATA_TYPE_3		
		0xA1: RGB555 + EXP16		
		0x12D: RAW14 + VP		
		0x144: USER_DEFINED_8_BIT_DATA_TYPE_5_DPCM12_VP		

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Bits	Field Name	Description	Type	Reset
		0x1C4: USER_DEFINED_8_BIT_DATA_TYPE_5_DPCM12_EXP16		
		0x2A: RAW8		
		0x3AA: RAW8 DPCM12 + VP		
		0x2C1: USER_DEFINED_8_BIT_DATA_TYPE_2 + DPCM10 + EXP16		
		0x1C3: USER_DEFINED_8_BIT_DATA_TYPE_4_DPCM12_EXP16		
		0x342: USER_DEFINED_8_BIT_DATA_TYPE_3 + DPCM10 + VP		
		0x142: USER_DEFINED_8_BIT_DATA_TYPE_3_DPCM12_VP		
		0x1A: YUV4:2:0 8bit legacy		
		0x36A: RAW8 DPCM12 + EXP16		
		0x32A: RAW8 + DPCM10 + VP		
		0x229: RAW7 + DPCM10 + EXP16		
		0x12A: RAW8 + VP		
		0x28: RAW6		
		0x1C1: USER_DEFINED_8_BIT_DATA_TYPE_2_DPCM12_EXP16		
		0x2A8: RAW6 + DPCM10 + EXP16		
		0x45: USER_DEFINED_8_BIT_DATA_TYPE_6		
		0xDE: Same as YUV4:2:2 8bit + VP but data is send as 16-bit wide words to video port. Could be used together with the GENERIC and BYTESWAP features.		
		0x340: USER_DEFINED_8_BIT_DATA_TYPE_1 + DPCM10 + VP		
		0x40: USER_DEFINED_8_BIT_DATA_TYPE_1		
		0x19: YUV4:2:0 10 bit		
		0x344: USER_DEFINED_8_BIT_DATA_TYPE_5 + DPCM10 + VP		
		0x2C2: USER_DEFINED_8_BIT_DATA_TYPE_3 + DPCM10 + EXP16		
		0x141: USER_DEFINED_8_BIT_DATA_TYPE_2_DPCM12_VP		
		0x369: RAW7 DPCM12 + EXP16		
		0x69: RAW7 + EXP8		
		0x2C4: USER_DEFINED_8_BIT_DATA_TYPE_5 + DPCM10 + EXP16		
		0x1C: YUV4:2:0 8 bit + CSPS		
		0x347: USER_DEFINED_8_BIT_DATA_TYPE_8 + DPCM10 + VP		
		0x146: USER_DEFINED_8_BIT_DATA_TYPE_7_DPCM12_VP		
		0x82: USER_DEFINED_8_BIT_DATA_TYPE_3 + EXP8		
		0x47: USER_DEFINED_8_BIT_DATA_TYPE_8		
		0x2AA: RAW8 + DPCM10 + EXP16		
		0x1E: YUV4:2:2 8 bit		
		0x33: RGB666 + EXP32_24		
		0x2C: RAW12		

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Bits	Field Name	Description	Type	Reset
		0x2C7: USER_DEFINED_8_BIT_DATA_TYPE_8 + DPCM10 + EXP16 0x147: USER_DEFINED_8_BIT_DATA_TYPE_8_DPCM12_VP 0x81: USER_DEFINED_8_BIT_DATA_TYPE_2 + EXP8 0x24: RGB888 0x2D: RAW14 0x345: USER_DEFINED_8_BIT_DATA_TYPE_6 + DPCM10 + VP 0xAB: RAW10 + EXP16 0x3A8: RAW6 DPCM12 + EXP16 0x44: USER_DEFINED_8_BIT_DATA_TYPE_5 0x2C0: USER_DEFINED_8_BIT_DATA_TYPE_1 + DPCM10 + EXP16 0x18: YUV4:2:0 8 bit 0x12F: RAW10 + VP 0xE8: RAW6 + DPCM10 + VP 0x1F: YUV4:2:2 10 bit 0x2C5: USER_DEFINED_8_BIT_DATA_TYPE_6 + DPCM10 + EXP16 0x1C2: USER_DEFINED_8_BIT_DATA_TYPE_3_DPCM12_EXP16 0x1C6: USER_DEFINED_8_BIT_DATA_TYPE_7_DPCM12_EXP16 0x29: RAW7 0x86: USER_DEFINED_8_BIT_DATA_TYPE_7 + EXP8		

Table 8-193. Register Call Summary for Register CSI2_CTX_CTRL2_i

ISS Interfaces

- ISS CSI2 Protocol and Data Format: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]
- ISS CSI2 Functional Description: [22] [23] [24] [25] [26] [27] [28] [29]
- ISS CSI2 Programming a Context to a Virtual Channel and a Data Type: [30] [31] [32]
- ISS CSI2 REGS1 Registers: [33] [34] [35]

Table 8-194. CSI2_CTX_DAT_OFST_i

Address Offset	0x0000 0078 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1078 + (0x20 * i) 0x5200 1478 + (0x20 * i) 0x5200 2478 + (0x20 * i)	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	DATA MEM ADDRESS OFFSET REGISTER - Context This register sets the offset, which is applied on the destination address after each line is written to memory. This register applies for both CSI2_CTX_DAT_PING_ADDR_i and CSI2_CTX_DAT_PONG_ADDR_i. For example, it enables to perform 2D data transfers of the pixel data into a frame buffer. In such case, the pixel data and frame buffer data must have the same data format. The 5 LSBs are ignored: the offset must be a multiple of 32 bytes. This register is shadowed: modifications are taken into account after the next FSC sync code. Only full 32-bit values must be written.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OFST														RESERVED	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:5	OFST	Line offset programmed in bytes (signed value 2's complement). If OFST = 0, the data is written contiguously in memory. Otherwise, OFST sets the destination offset between the first pixel of the previous line and the first pixel of the current line. Valid range: - 2^{17} ÷ (2^{17} - 1)	RW	0x0000
4:0	RESERVED		R	0x00

Table 8-195. Register Call Summary for Register CSI2_CTX_DAT_OFST_i

ISS Interfaces

- ISS CSI2 Protocol and Data Format: [0] [1]
- ISS CSI2 Functional Description: [2] [3] [4]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [5]
- ISS CSI2 REGS1 Registers: [6]

Table 8-196. CSI2_CTX_DAT_PING_ADDR_i

Address Offset	0x0000 007C + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 107C + (0x20 * i) 0x5200 147C + (0x20 * i) 0x5200 247C + (0x20 * i)	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	DATA MEM PING ADDRESS REGISTER - Context This register sets the 32-bit memory address where the pixel data are stored. The destination is double buffered: this register sets the PING address. Double buffering is enabled when the addresses CSI2_CTX_DAT_PING_ADDR_i and CSI2_CTX_DAT_PONG_ADDR_i are different. The 5 LSBs are ignored: the address must be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code. Only full 32-bit values must be written.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most-significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-197. Register Call Summary for Register CSI2_CTX_DAT_PING_ADDR_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [2] [3]
- ISS CSI2 REGS1 Registers: [4] [5] [6] [7] [8] [9]

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Table 8-198. CSI2_CTX_DAT_PONG_ADDR_i

Address Offset	0x0000 0080 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1080 + (0x20 * i) 0x5200 1480 + (0x20 * i) 0x5200 2480 + (0x20 * i)	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	DATA MEM PONG ADDRESS REGISTER - Context This register sets the 32-bit memory address where the pixel data are stored. The destination is double-buffered: this register sets the PONG address. Double-buffering is enabled when the addresses CSI2_CTX_DAT_PING_ADDR_i and CSI2_CTX_DAT_PONG_ADDR_i are different. The 5 LSBs are ignored: the address must be aligned on a 32-byte boundary. This register is shadowed: modifications are taken into account after the next FSC sync code. Only full 32-bit values must be written.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	27 most-significant bits of the 32-bit address.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-199. Register Call Summary for Register CSI2_CTX_DAT_PONG_ADDR_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 REGS1 Registers: [2] [3] [4] [5] [6] [7]

Table 8-200. CSI2_CTX_IRQENABLE_i

Address Offset	0x0000 0084 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1084 + (0x20 * i) 0x5200 1484 + (0x20 * i) 0x5200 2484 + (0x20 * i)	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	INTERRUPT ENABLE REGISTER - Context This register regroups all the events related to context.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_CORRECTION_IRQ	LINE_NUMBER_IRQ	FRAME_NUMBER_IRQ	CS_IRQ	RESERVED	LE_IRQ	LS_IRQ	FE_IRQ	FS_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ECC_CORRECTION_IRQ	Context - ECC has been used to correct the only 1-bit error (long packet only). 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
7	LINE_NUMBER_IRQ	Context - Line number is reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	FRAME_NUMBER_IRQ	Context - Frame counter reached. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
5	CS_IRQ	Context - Check-Sum of the payload mismatch detection 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	RESERVED		R	0
3	LE_IRQ	Context - Line end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	LS_IRQ	Context - Line start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	FE_IRQ	Context - Frame end sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
0	FS_IRQ	Context - Frame start sync code detection. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 8-201. Register Call Summary for Register CSI2_CTX_IRQENABLE_i

ISS Interfaces
- ISS CSI2 Functional Description: [0] [1]
- ISS CSI2 REGS1 Registers: [2]

Table 8-202. CSI2_CTX_IRQSTATUS_i

Address Offset	0x0000 0088 + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 1088 + (0x20 * i) 0x5200 1488 + (0x20 * i) 0x5200 2488 + (0x20 * i)	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	INTERRUPT STATUS REGISTER - Context This register regroups all the events related to Context.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ECC_CORRECTION_IRQ	LINE_NUMBER_IRQ	FRAME_NUMBER_IRQ	CS_IRQ	RESERVED	LE_IRQ	LS_IRQ	FE_IRQ	FS_IRQ

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	ECC_CORRECTION_IRQ	Context - ECC has been used to do the correction of the only 1-bit error status (long packet only). 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
7	LINE_NUMBER_IRQ	Context - Line number reached status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
6	FRAME_NUMBER_IRQ	Context - Frame counter reached status 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
5	CS_IRQ	Context - Check-Sum mismatch status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	RESERVED		R	0
3	LE_IRQ	Context - Line end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
2	LS_IRQ	Context - Line start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
1	FE_IRQ	Context - Frame end sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	FS_IRQ	Context - Frame start sync code detection status. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

Table 8-203. Register Call Summary for Register CSI2_CTX_IRQSTATUS_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1] [2] [3]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [4]
- ISS CSI2 REGS1 Registers: [5]

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Table 8-204. CSI2_CTX_CTRL3_i

Address Offset	0x0000 008C + (0x20 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 108C + (0x20 * i) 0x5200 148C + (0x20 * i) 0x5200 248C + (0x20 * i)	**Instance**	ISS_CSI2_A_REGS1 ISS_CSI2_B_REGS1 ISS_CSI2_C_REGS1
Description	CONTROL REGISTER - Context This register controls the Context. This register is shadowed: modifications are taken into account after the next FSC sync code.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ALPHA								LINE_NUMBER															

Bits	Field Name	Description	Type	Reset
31:16	ALPHA	When bit field CSI2_CTX_CTRL1_i[27:24] TRANSCODE = 0 Alpha value for RGB888, RGB666 and RBG444. When bit fields CSI2_CTX_CTRL1_i[27:24] TRANSCODE = 1 and [29] BYS=1 Image width, in pixels, acquired from the BYS port.	RW	0x0000
15:0	LINE_NUMBER	Line number for the interrupt generation	RW	0x0000

Table 8-205. Register Call Summary for Register CSI2_CTX_CTRL3_i

ISS Interfaces

- ISS CSI2 Protocol and Data Format: [0] [1] [2]
- ISS CSI2 Functional Description: [3] [4]
- ISS CSI2 Programming Enable Video/Picture Acquisition: [5]
- ISS CSI2 Programming a Periodic Event During Frame Acquisition: [6]
- ISS CSI2 REGS1 Registers: [7] [8] [9]

8.2.5.5.3 ISS CSI2 REGS2 Registers

8.2.5.5.3.1 ISS CSI2 REGS2 Register Summary

Table 8-206 summarizes the CSI2 REGS2 registers.

Table 8-206. ISS CSI2 REGS2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CSI2_A_REGS2 Base Address	ISS_CSI2_B_REGS2 Base Address	ISS_CSI2_C_REGS2 Base Address
CSI2_CTX_TRANSCODEH_i (1)	RW	32	0x0000 0000 + (0x8 * i)	0x5200 11C0 + (0x8 * i)	0x5200 15C0 + (0x8 * i)	0x5200 25C0 + (0x8 * i)
CSI2_CTX_TRANSCODEV_i (1)	RW	32	0x0000 0004 + (0x8 * i)	0x5200 11C4 + (0x8 * i)	0x5200 15C4 + (0x8 * i)	0x5200 25C4 + (0x8 * i)

(1) i = 0 to 7

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8.2.5.5.3.2 ISS CSI2 REGS2 Register Description

and describe the CSI2 REGS2 registers.

Table 8-207. CSI2_CTX_TRANSCODEH_i

Address Offset	0x0000 0000 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 11C0 + (0x8 * i) 0x5200 15C0 + (0x8 * i) 0x5200 25C0 + (0x8 * i)	**Instance**	ISS_CSI2_A_REGS2 ISS_CSI2_B_REGS2 ISS_CSI2_C_REGS2
Description	Transcode configuration register: defines horizontal frame cropping		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HCOUNT								RESERVED								HSKIP							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	HCOUNT	Pixels to output per line when the values is between 1 and 8191. Pixels HSKIP-WIDTH pixels are output when HCOUNT=0. WIDTH corresponds to the image width provided by the sensor.	RW	0x0000
15:13	RESERVED		R	0x0
12:0	HSKIP	Pixel to skip horizontally. Valid values: 0-8191	RW	0x0000

Table 8-208. Register Call Summary for Register CSI2_CTX_TRANSCODEH_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1] [2] [3]
- ISS CSI2 REGS2 Registers: [4]

Table 8-209. CSI2_CTX_TRANSCODEV_i

Address Offset	0x0000 0004 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5200 11C4 + (0x8 * i) 0x5200 15C4 + (0x8 * i) 0x5200 25C4 + (0x8 * i)	**Instance**	ISS_CSI2_A_REGS2 ISS_CSI2_B_REGS2 ISS_CSI2_C_REGS2
Description	Transcode configuration register: defines vertical frame cropping		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VCOUNT								RESERVED								VSKIP							

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	VCOUNT	Lines to output per frame when the values is between 1 and 8191. Pixels VSKIP-HEIGHT pixels are output when VCOUNT=0. HEIGHT corresponds to the image height provided by the sensor.	RW	0x0000
15:13	RESERVED		R	0x0
12:0	VSKIP	Pixel to skip vertically Valid values: 0-8191	RW	0x0000

Table 8-210. Register Call Summary for Register CSI2_CTX_TRANSCODEV_i

ISS Interfaces

- ISS CSI2 Functional Description: [0] [1] [2]
- ISS CSI2 REGS2 Registers: [3]

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8.2.6 ISS TCTRL

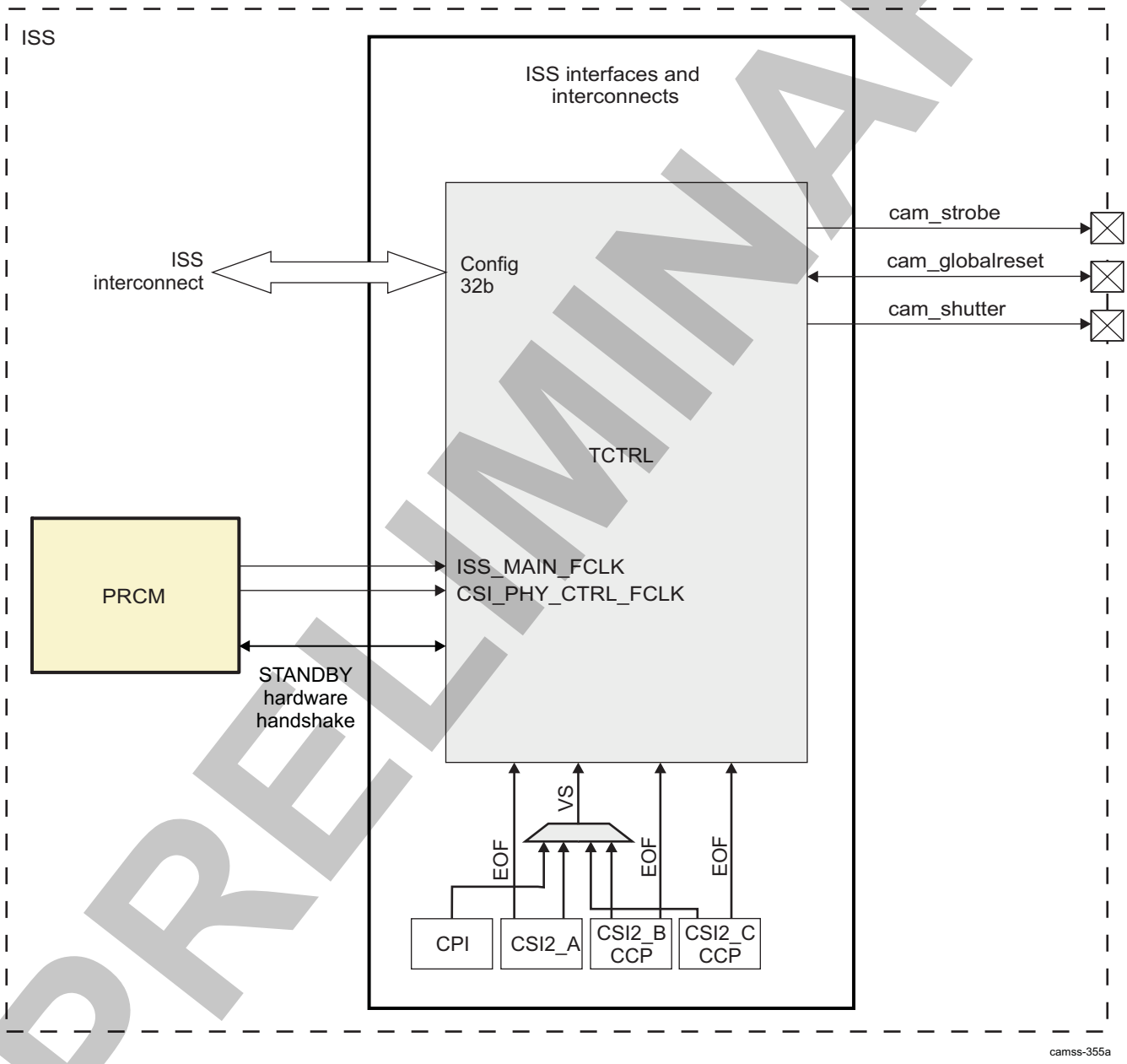
8.2.6.1 ISS TCTRL Environment

There are no particular environment attributes. See Section 8.2.2, *ISS Interfaces Environment*.

8.2.6.2 ISS TCTRL Integration

Figure 8-77 shows the integration of the TCTRL.

Figure 8-77. ISS TCTRL Integration



For information about the power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

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8.2.6.3 ISS TCTRL Functional Description

8.2.6.3.1 ISS TCTRL Features

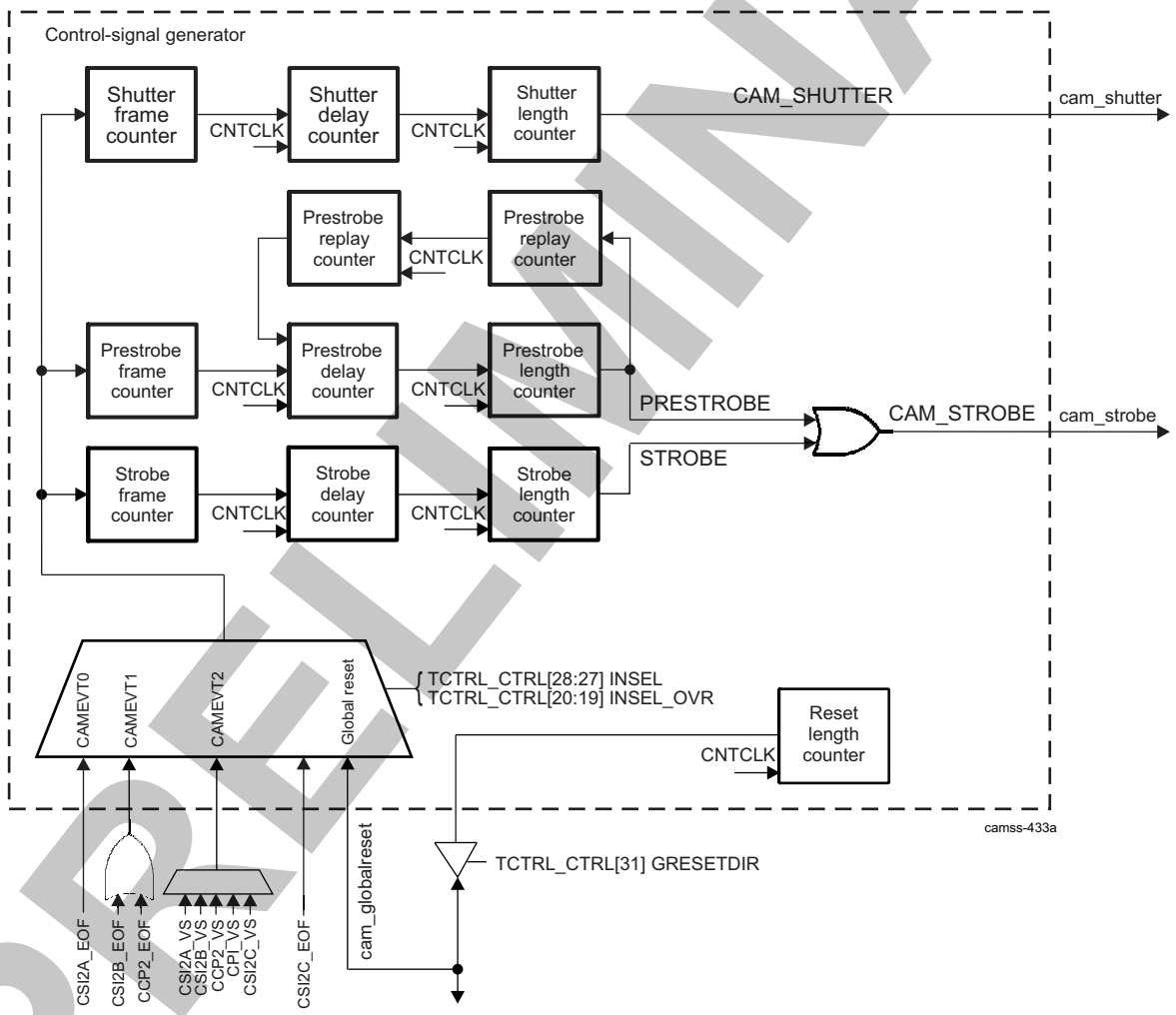
The TCTRL module receives synchronization events from one or multiple cameras and from an external global reset control mechanism. The synchronization event to be used is software configurable. The TCTRL generates the control signals (cam_strobe and cam_shutter) for the flash prestrobe, flash strobe, and mechanical shutters. It also provides a global reset output to erase sensor data before opening the mechanical shutter.

The TCTRL includes a timing generator and a control-signal generator.

8.2.6.3.2 ISS TCTRL Control-Signal Generator

The control-signal generator generates the prestrobe, strobe, and shutter signals: cam_strobe and cam_shutter. Figure 8-78 shows the principle of control-signal generation.

Figure 8-78. TCTRL Control-Signal Generation



The control-signal generator gathers precise timings for the cam_strobe and cam_shutter signals, to assert and deassert the signals at known times. The timing control-signal generator can be synchronized on the vertical synchronization signal coming from the CSI2_A, CSI2_B, CSI2_C, CCP2, Parallel interface (CPI), or on an externally generated cam_globalreset signal.

A multiplexer controls which of the CSI2_A, CSI2_B, CSI2_C, CCP2, or Parallel interfaces drives control-signal generation. This multiplexer can also select the externally generated cam_globalreset signal as the trigger event. The TCTRL_CTRL[31] GRESETDIR bit defines the direction of cam_globalreset.

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- The externally generated cam_globalreset is used as a trigger when TCTRL_CTRL[31] GRESETDIR = 0 and TCTRL_CTRL[28:27] INSEL = 3 and TCTRL_CTRL[20:19] INSEL_OVR = 0.
- The internally generated cam_globalreset is used as a trigger when TCTRL_CTRL[31] GRESETDIR = 1 and TCTRL_CTRL[28:27] INSEL = 3 and TCTRL_CTRL[20:19] INSEL_OVR = 0.

The cam_globalreset signal can also be generated internally by the control-signal generator under software control. In this case, the prestrobe and shutter signals are synchronized on internally generated cam_globalreset . The multiplexer controls whether control-signal generation must be triggered by the internal or external cam_globalreset.

The prestrobe-, strobe-, and shutter-control signals can be individually enabled at any time. These signals must not be disabled by software.

The clock divider generates the CNTCLK clock based on the functional clock (ISS_MAIN_FCLK). The clock divider is programmable. Table 8-211 lists the possible frequencies as a function of the divisor values.

Table 8-211. ISS TCTRL Control-Signal Generator: CNTCLK Frequencies

Divisor Value TCTRL_CTRL[18:10] DIVC	CNTCLK Clock	CNTCLK Precision (ns)
0 (default)	Clock gated. No clock.	N/A
1	304 MHz	3.29
2	152 MHz	6.58
3	101.333 MHz	9.87
4	76 MHz	13.16
...	...	...
510	0.596 MHz	1677.63
511	0.595 MHz	1680.92

There are three counters per control signal, plus three counters to control the pre-strobe generation, for a total of twelve counters. Each counter is programmable.

- The frame counter is decreased each time a full new frame is received.
  - A new frame is detected by the TCTRL module when CAMEVTx is received.
  - The frame counter determines how many whole frames must be ignored before the delay counter is triggered. The frame counters can be set to 0 to bypass the frame counters.
- The delay counter determines the control-signal activation delay. The counter is decreased at every CNTCLK clock cycle. When the counter reaches 0, the control signal is asserted. If the delay counter is set to 0, the control signal is asserted immediately.
- The activation-length counter determines the length of control-signal assertion. The counter is decreased at every CNTCLK clock cycle. When the counter reaches 0, the signal is deasserted and the control-signal enable bit is disabled. If the activation length is set to 0, the control signal is not asserted and the control-signal enable bit is disabled.

The polarity of the following signals can be individually selected:

- TCTRL_CTRL[26] STRBPSTRBPOL for the cam_strobe signals
- TCTRL_CTRL[24] SHUTPOL for the cam_shutter signal
- TCTRL_CTRL[30] GRESETPOL for cam_globalreset signal

Software can trigger the generation of cam_globalreset to the camera module. The length of signal-activation is programmable. The counter is decreased at every CNTCLK clock cycle. When the counter reaches 0, the signal is deasserted and the global reset enable bit is disabled (the TCTRL_CTRL[29] GRESETEN bit). If the activation length is set to 0, the control signal is not asserted and the control-signal enable bit is disabled. The polarity of cam_globalreset can be selected (the TCTRL_CTRL[30] GRESETPOL bit).

Figure 8-79 shows the use of cam_globalreset set as an input or output signal. The cam_globalreset is asynchronous, edge-sensitive, and asserted for at least one interconnect clock cycle.

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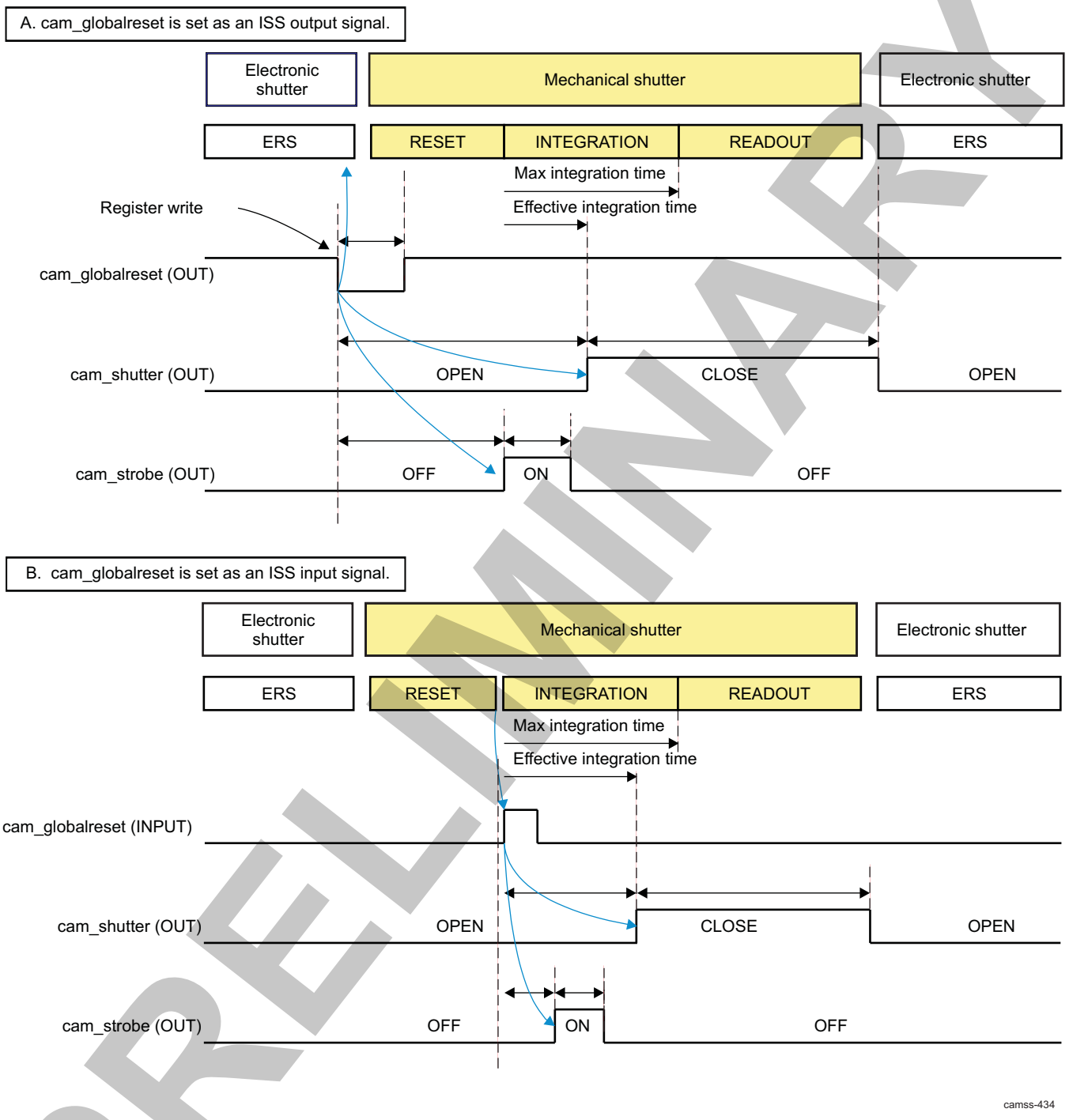
Figure 8-79. ISS TCTRL Use of cam_globalreset With Global Reset Release Camera Modules



There are two types of shutter mechanisms: mechanical and electronic. A mechanical shutter is used only for high-resolution sensors. The three control signals (cam_globalreset, cam_shutter, and cam_strobe) are useful with a mechanical shutter. High frame rates can be achieved only with an electronic shutter. When an electronic shutter is used, none of the three control signals is used.

- Mechanical shutter mechanism:
  - Reset: All pixels of the sensor are reset to their black value. When the sensor has a global reset feature, the mechanical shutter can be open during reset.
  - Integration: The light received by the sensor is transformed into electrical charges that are stored inside pixels. At the end of the integration time, the shutter must be closed. Exposure time is

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defined by the time between reset release and shutter close.
  - Readout: The charges accumulated in pixels are converted to digital values that are sent to the camera receiver.
- Electronic rolling shutter (ERS) mechanism:
  - Each line of the sensor is reset separately and read after a fixed amount of time. Exposure time is defined by the time between reset and read.

8.2.6.4 ISS TCTRL Programming Model

The following settings must be done before enabling the TCTRL.

8.2.6.4.1 ISS TCTRL Camera-Control Signal Generator

Two configurations apply:

- First configuration: The control signals are based on the vertical synchronization information coming from the camera module or from externally generated cam_globalreset.
- Second configuration: The control signals are based on internally generated cam_globalreset.

8.2.6.4.1.1 ISS TCTRL Vertical Sync-Based Control-Signal Generation or Externally Generated cam_globalreset

To enable control-signal generation in the first configuration, follow the procedure listed in Table 8-212.

Table 8-212. ISS TCTRL Enabling the Control-Signal Generation in First Configuration

Step	Bit Field	Value
Select the input that triggers the control signals. The trigger signal can come from the CSI2_A, CSI2_B/CCP2, CSI2_C/CCP2, Parallel interface (CPI) or the externally generated cam_globalreset signal.	TCTRL_CTRL[28:27] INSEL	0x0: CSI2A 0x1: CSI2B or CCP2 0x2: VS signal 0x3: Global reset
	TCTRL_CTRL[20:19] INSEL_OVR	0x0: Use settings defined in INSEL 0x1: CSI2C or CCP2
Set the global reset as input signal. Writes to the TCTRL_CTRL[29] GRESETEN bit do not trigger the CAM_STROBE and CAM_SHUTTER signals and do not generate the CAM_GLOBALRESET signal.	TCTRL_CTRL[31] GRESETDIR	0x0
The following bits are cleared automatically to 0 after the signal assertion:	• TCTRL_CTRL[21] SHUTEN • TCTRL_CTRL[22] PSTRBEN • TCTRL_CTRL[23] STRBEN	
Set the polarity of the CAM_SHUTTER, CAM_STROBE, and CAM_GLOBALRESET signals.	• TCTRL_CTRL[24] SHUTPOL • TCTRL_CTRL[26] STRBPSTRBPOL • TCTRL_CTRL[30] GRESETPOL	
Set the clock divisor value, which generates the CNTCLK clock The clock is set by CNTCLK = ISS_MAIN_FCLK / TCTRL_CTRL[18:10] DIVC.	TCTRL_CTRL[18:10] DIVC	0x0: Disable CNTCLK 0 to 511: Divider
Set the frame counters.	• TCTRL_FRAME[5:0] SHUT • TCTRL_FRAME[11:6] PSTRB • TCTRL_FRAME[17:12] STRB	0: TCTRL does not delay any frame in input. 1 to 63

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Table 8-212. ISS TCTRL Enabling the Control-Signal Generation in First Configuration (continued)

Step	Bit Field	Value
Set the delay counters.	• TCTRL_SHUT_DELAY • TCTRL_PSTRB_DELAY • TCTRL_STRB_DELAY	The possible values are 0 to 2^{25} - 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration is (2^{25} - 1) x 511/304 MHz = 56.40234948 s (TCTRL_CTRL[18:10] DIVC = 511).
Set the signal durations.	• TCTRL_SHUT_LENGTH • TCTRL_PSTRB_LENGTH • TCTRL_STRB_LENGTH	The possible values are 0 to 2^{24} - 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration for a 304 MHz input clock is (2^{24} - 1) x 511/304 MHz = 28.201173898 s (TCTRL_CTRL.DIVC = 511).
Enable the SHUTTER signal.	TCTRL_CTRL[21] SHUTEN	0x1
Enable the PRESTROBE signal.	TCTRL_CTRL[22] PSTRBEN	0x1
Enable the STROBE signal.	TCTRL_CTRL[23] STRBEN	0x1

8.2.6.4.1.2 ISS TCTRL Internally Generated cam_globalreset-Based Control-Signal Generation

To enable control-signal generation in the second configuration, follow the procedure listed in Table 8-213.

Table 8-213. ISS TCTRL Enabling the Control-Signal Generation in Second Configuration

Step	Bit Field	Value
Select the input to global reset, to loop back the internally generated CAM_GLOBALRESET. Vertical synchronization events do not trigger the CAM_STROBE and CAM_SHUTTER signals.	TCTRL_CTRL[28:27] INSEL TCTRL_CTRL[20:19] INSEL_OVR	0x3: Global reset 0x0: Use settings defined in INSEL
Set the global reset as output signal.	TCTRL_CTRL[31] GRESETDIR	0x1
The following bits are cleared automatically to 0 after the signal assertion:	• TCTRL_CTRL[21] SHUTEN • TCTRL_CTRL[22] PSTRBEN • TCTRL_CTRL[23] STRBEN • TCTRL_CTRL[29] GRESETEN	0x0
Set the polarity of the CAM_SHUTTER, CAM_STROBE, and CAM_GLOBALRESET signals.	• TCTRL_CTRL[24] SHUTPOL • TCTRL_CTRL[26] STRBPSTRBPOL • TCTRL_CTRL[30] GRESETPOL	
Set the clock divisor value, which generates the CNTCLK clock The clock is set by CNTCLK = ISS_MAIN_FCLK / TCTRL_CTRL[18:10] DIVC.	TCTRL_CTRL[18:10] DIVC	0x0: Disable CNTCLK 0 to 511: Divider
Set the frame counters.	• TCTRL_FRAME[5:0] SHUT • TCTRL_FRAME[11:6] PSTRB • TCTRL_FRAME[17:12] STRB	0: TCTRL does not delay any frame in input. 1 to 63

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Table 8-213. ISS TCTRL Enabling the Control-Signal Generation in Second Configuration (continued)

Step	Bit Field	Value
Set the delay counters.	• TCTRL_SHUT_DELAY • TCTRL_PSTRB_DELAY • TCTRL_STRB_DELAY	The possible values are 0 to 2^{25} - 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration is (2^{25} - 1) x 511/304 MHz = 56.40234948 s (TCTRL_CTRL[18:10] DIVC = 511).
Set the signal durations.	• TCTRL_SHUT_LENGTH • TCTRL_PSTRB_LENGTH • TCTRL_STRB_LENGTH	The possible values are 0 to 2^{24} 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration for a 304 MHz input clock is (2^{24} - 1) x 511/304 MHz = 28.201173898 s (TCTRL_CTRL[18:10] DIVC = 511).
Set the cam_global_reset assertion time.	TCTRL_GRESET_LENGTH	The possible values are 0 to 2^{24} - 1 cycles. The cycles are at the CNTCLK clock frequency. The maximum signal duration for a 304 MHz input clock is (2^{24} 1) x 511/304 MHz = 28.201173898 s (TCTRL_CTRL[18:10] DIVC = 511).
Enable the CAM_SHUTTER signal.	TCTRL_CTRL[21] SHUTEN	0x1
Enable the PRESTROBE signal.	TCTRL_CTRL[22] PSTRBEN	0x1
Enable the CAM_STROBE signal.	TCTRL_CTRL[23] STRBEN	0x1
Enable the CAM_GLOBALRESET control-signal generation.	TCTRL_CTRL[29] GRESETEN	0x1

NOTE: Setting the following bits to 1 simultaneously leads to unpredictable behavior:

- TCTRL_CTRL[21] SHUTEN
- TCTRL_CTRL[22] PSTRBEN
- TCTRL_CTRL[23] STRBEN
- TCTRL_CTRL [29] GRESETEN

The following bits must be set before TCTRL_CTRL[29] GRESETEN is enabled:

- TCTRL_CTRL[21] SHUTEN
- TCTRL_CTRL[22] PSTRBEN
- TCTRL_CTRL[23] STRBEN

8.2.6.4.1.3 ISS TCTRL cam_strobe Signal Generation for Red-Eye Removal

The cam_strobe signal generation enables a strobe flash for red-eye removal. The process is shown in Figure 8-80. The dotted line corresponds to known timings from which the delay counters start decreasing: cam_globalreset event.

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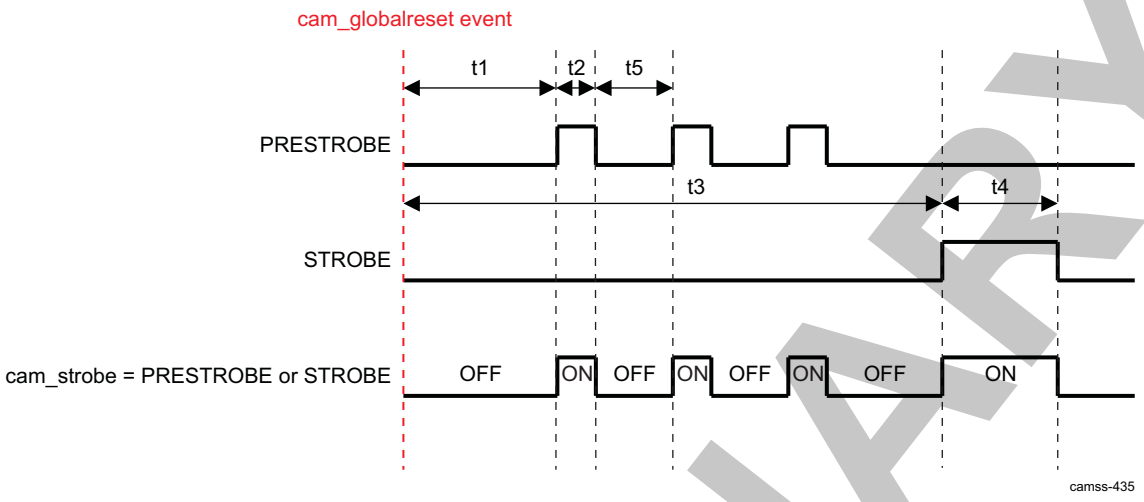
Figure 8-80. cam_strobe Signal-Generation for Red-Eye Removal



- t1: Set by the TCTRL_PSTRB_DELAY register
- t2: Set by the TCTRL_PSTRB_LENGTH register
- t5: Set by the TCTRL_PSTRB_REPLAY[24:0] DELAY bit field. The number of times the pulse is repeated is controlled by the TCTRL_PSTRB_REPLAY[31:25] COUNTER bit field.

  In the previous example, TCTRL_PSTRB_REPLAY[31:25] COUNTER = 2.
  - The possible delay values are 0 to 2^{25} - 1 cycle. The cycles are at the CNTCLK clock frequency. The maximum signal duration is (2^{25} - 1) x 511/304 MHz = 56.402351158 s (TCTRL_CTRL[18:11] DIVC = 511).
  - The possible count values are 0 to 127 additional pulses.
- t3: Set by the TCTRL_STRB_DELAY register
- t4: Set by the TCTRL_STRB_LENGTH register

8.2.6.5 ISS TCTRL Register Manual

8.2.6.5.1 ISS TCTRL Instance Summary

Table 8-214 summarizes the TCTRL instance.

Table 8-214. ISS TCTRL Instance Summary

Module Name	L3 Base Address	Size
ISS_TCTRL	0x5200 0400	256 bytes

8.2.6.5.2 ISS TCTRL Registers

8.2.6.5.2.1 ISS TCTRL Register Summary

Table 8-215 summarizes the TCTRL registers.

Table 8-215. ISS TCTRL Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_TCTRL Base Address
TCTRL_REVISION	R	32	0x0000 0000	0x5200 0400
TCTRL_SYSCONFIG	RW	32	0x0000 0004	0x5200 0404
TCTRL_SYSSTATUS	R	32	0x0000 0008	0x5200 0408
TCTRL_STRB_LENGTH	RW	32	0x0000 0010	0x5200 0410

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Table 8-215. ISS TCTRL Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_TCTRL Base Address
TCTRL_PSTRB_LENGTH	RW	32	0x0000 0014	0x5200 0414
TCTRL_SHUT_LENGTH	RW	32	0x0000 0018	0x5200 0418
TCTRL_GRESET_LENGTH	RW	32	0x0000 001C	0x5200 041C
TCTRL_STRB_DELAY	RW	32	0x0000 0020	0x5200 0420
TCTRL_PSTRB_DELAY	RW	32	0x0000 0024	0x5200 0424
TCTRL_SHUT_DELAY	RW	32	0x0000 0028	0x5200 0428
TCTRL_CTRL	RW	32	0x0000 0030	0x5200 0430
TCTRL_PSTRB_REPLAY	RW	32	0x0000 0034	0x5200 0434
TCTRL_FRAME	RW	32	0x0000 0038	0x5200 0438

8.2.6.5.2.2 ISS TCTRL Register Description

through describe the TCTRL registers.

Table 8-216. TCTRL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 0400	**Instance**	ISS_TCTRL
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1)

(1) TI internal data

Table 8-217. Register Call Summary for Register TCTRL_REVISION

ISS Interfaces

- ISS TCTRL Registers: [0]

Table 8-218. TCTRL_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x5200 0404	**Instance**	ISS_TCTRL
Description	OCP-SOCKET SYSTEM CONFIGURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SOFT_RESET	AUTO_IDLE

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	SOFT_RESET	Software reset. Set the bit to 1 to trigger the module reset. The bit is automatically reset be the hardware. During reads return 0. 0x0: Normal mode. 0x1: The module is reset.	RW	0
0	AUTO_IDLE	Internal OCP and functional clock gating strategy 0x0: OCP and functional clocks are free-running 0x1: Automatic clock gating strategy is applied, based on the OCP interface activity for interface clock and on the functional activity for functional clocks.	RW	1

Table 8-219. Register Call Summary for Register TCTRL_SYSCONFIG

ISS Interfaces
- ISS TCTRL Registers: [0]

Table 8-220. TCTRL_SYSSTATUS

Address Offset	0x0000 0008		
Physical Address	0x5200 0408	**Instance**	ISS_TCTRL
Description	OCP-SOCKET SYSTEM STATUS REGISTER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESET_DONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RESET_DONE	Internal reset monitoring Read 0x1: Reset completed. Read 0x0: Internal module reset is ongoing.	R	0

Table 8-221. Register Call Summary for Register TCTRL_SYSSTATUS

ISS Interfaces
- ISS TCTRL Registers: [0]

Table 8-222. TCTRL_STRB_LENGTH

Address Offset	0x0000 0010		
Physical Address	0x5200 0410	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - STROBE LENGTH REGISTER This register is used by the TIMING CTRL module to generate the STROBE signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LENGTH																							

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	LENGTH	Sets the length of the CAM_STROBE signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL[18:10] DIVC bit field. After signal assertion, the TCTRL_CTRL.STRBEN bit is automatically cleared. The possible values are 0 to 2^{24}-1 cycles.	RW	0x000000

Table 8-223. Register Call Summary for Register TCTRL_STRB_LENGTH

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2]
- ISS TCTRL Registers: [3] [4]

Table 8-224. TCTRL_PSTRB_LENGTH

Address Offset	0x0000 0014		
Physical Address	0x5200 0414	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - PRESTROBE LENGTH REGISTER This register is used by the TIMING CTRL module to generate the PRESTROBE signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LENGTH																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	LENGTH	Sets the length of the CAM_PRESTROBE signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. After signal assertion, the TCTRL_CTRL[22] PSTRBEN bit is automatically cleared. The possible values are 0 to 2^{24}-1 cycles.	RW	0x000000

Table 8-225. Register Call Summary for Register TCTRL_PSTRB_LENGTH

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2]
- ISS TCTRL Registers: [3] [4] [5] [6] [7]

Table 8-226. TCTRL_SHUT_LENGTH

Address Offset	0x0000 0018		
Physical Address	0x5200 0418	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - SHUTTER LENGTH REGISTER This register is used by the TIMING CTRL module to generate the CAM_SHUTTER signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LENGTH																							

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	LENGTH	Sets the length of the CAM_SHUTTER signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. After signal assertion, the TCTRL_CTRL.SHUTEN bit is automatically cleared. The possible values are 0 to 2^{24}-1 cycles.	RW	0x000000

Table 8-227. Register Call Summary for Register TCTRL_SHUT_LENGTH

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1]
- ISS TCTRL Registers: [2] [3]

Table 8-228. TCTRL_GRESET_LENGTH

Address Offset	0x0000 001C		
Physical Address	0x5200 041C	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - GLOBAL SHUTTER LENGTH REGISTER This register is used by the TIMING CTRL module to generate the CAM_GLOBALRESET signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LENGTH																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	LENGTH	Sets the length of the CAM_GLOBALRESET signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. After signal assertion, the TCTRL_CTRL.GRESETEN bit is automatically cleared. The possible values are 0 to 2^{24}-1 cycles. The polarity of the CAM_GLOBALRESET signal is set by the TCTRL_CTRL.GRESETPOL bit.	RW	0x000000

Table 8-229. Register Call Summary for Register TCTRL_GRESET_LENGTH

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0]
- ISS TCTRL Registers: [1] [2]

Table 8-230. TCTRL_STRB_DELAY

Address Offset	0x0000 0020		
Physical Address	0x5200 0420	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - STROBE DELAY REGISTER This register is used by the TIMING CTRL module to generate the STROBE signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELAY																							

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Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:0	DELAY	Sets the delay for the CAM_STROBE signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. The possible values are 0 to 2^{25}-1 cycles.	RW	0x0000000

Table 8-231. Register Call Summary for Register TCTRL_STRB_DELAY

ISS Interfaces • ISS TCTRL Camera-Control Signal Generator: [0] [1] [2] • ISS TCTRL Registers: [3] [4]

Table 8-232. TCTRL_PSTRB_DELAY

Address Offset	0x0000 0024		
Physical Address	0x5200 0424	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - PRE STROBE DELAY REGISTER This register is used by the TIMING CTRL module to generate the PRESTROBE signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELAY																							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:0	DELAY	Sets the delay for the PRESTROBE signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. The possible values are 0 to 2^{25}-1 cycles.	RW	0x0000000

Table 8-233. Register Call Summary for Register TCTRL_PSTRB_DELAY

ISS Interfaces • ISS TCTRL Camera-Control Signal Generator: [0] [1] [2] • ISS TCTRL Registers: [3] [4] [5]

Table 8-234. TCTRL_SHUT_DELAY

Address Offset	0x0000 0028		
Physical Address	0x5200 0428	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - SHUTTER DELAY REGISTER This register is used by the TIMING CTRL module to generate the CAM_SHUTTER signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELAY																							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:0	DELAY	Sets the delay for the CAM_SHUTTER signal assertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. The possible values are 0 to 2^{25}-1 cycles.	RW	0x0000000

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Table 8-235. Register Call Summary for Register TCTRL_SHUT_DELAY

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1]
- ISS TCTRL Registers: [2] [3]

Table 8-236. TCTRL_CTRL

Address Offset	0x0000 0030		
Physical Address	0x5200 0430	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - CONTROL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRESETDIR	GRESETPOL	GRESETEN	INSEL		STRBPSTRBPOL	RESERVED	SHUTPOL	STRBEN	PSTRBEN	SHUTEN	INSEL_OVR	DIVC										RESERVED									

Bits	Field Name	Description	Type	Reset
31	GRESETDIR	Sets the direction of the CAM_GLOBAL_RESET signal. 0x0: INPUT – CAM_GLOBALRESET is an input to the TIMING CONTROL module. The CAM_GLOBALRESET is externally generated. 0x1: OUTPUT – CAM_GLOBALRESET is an output of the TIMING CONTROL module. CAM_GLOBALRESET is internally generated. If GRESETEN is set to 1, the internally generated CAM_GLOBALRESET will trigger the generation of the PRESTROBE, STROBE and SHUTTER signals. The frame counters are ignored.	RW	0
30	GRESETPOL	Sets the polarity of the global reset signal: CAM_GLOBALRESET. It applies whatever the direction of the CAM_GLOBALRESET signal: input or output. 0x0: active high 0x1: active low	RW	0
29	GRESETEN	Triggers the generation of the CAM_GLOBALRESET signal. The signal is asserted immediately. If enabled, the CAM_GLOBALRESET signal will be asserted for TCTRL_GRESET_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. The polarity of the CAM_GLOBALRESET signal is set with TCTRL_CTRL.GRESETPOL. Enabling this bit triggers the generation of the CAM_SHUTTER and CAM_STROBE signals (if previously enabled). The frame counters must be set to 0 when this bit is set to 1 and GRESETDIR is set a OUTPUT.	RW	0

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Bits	Field Name	Description	Type	Reset
28:27	INSEL	Sets the mode that will trigger the SHUTTER, PRESTROBE and STROBE signals. 0x0: Synchronization event from camera 0 0x1: Synchronization event from camera 1 0x2: Synchronization event from camera 2 (serial interfaces muxed with the camera Parallel interface (CPI)) 0x3: GRESET – The CAM_GLOBALRESET input signal will trigger the SHUTTER, PRESTROBE and STROBE signals. In this mode, there are no frame counters. The delay counters start decrementing as soon as the CAM_GLOBALRESET signal is asserted. The polarity of the CAM_GLOBALRESET signal is set with TCTRL_CTRL.GRESETPOL.	RW	0x0
26	STRBPSTRBPOL	Sets the polarity of the strobe and prestrobe signals. 0x0: Active high 0x1: Active low	RW	0
25	RESERVED		R	0
24	SHUTPOL	Sets the polarity of the mechanical shutter signal: CAM_SHUTTER 0x0: Active high 0x1: Active low	RW	0
23	STRBEN	Flash strobe signal enable. If enabled, the STROBE signal will be asserted after TCTRL_FRAME.STRB frames have been received and a delay of TCTRL_STRB_DELAY cycles have passed. The STROBE signal is asserted for TCTRL_STRB_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. This signal must not be disabled by software.	RW	0
22	PSTRBEN	Flash prestrobe signal enable. If enabled, the PRESTROBE signal will be asserted after TCTRL_FRAME.PSTRB frames have been received and a delay of TCTRL_PSTRB_DELAY cycles have passed. The PRESTROBE signal is asserted for TCTRL_PSTRB_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. This signal must not be disabled by software.	RW	0
21	SHUTEN	Mechanical shutter signal enable. If enabled, the SHUTTER signal will be asserted after TCTRL_FRAME.SHUT frames have been received and a delay of TCTRL_SHUT_DELAY cycles have passed. The SHUTTER signal is asserted for TCTRL_SHUT_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. This signal must not be disabled by software.	RW	0
20:19	INSEL_OVR	Sets the mode that will trigger the SHUTTER, PRESTROBE and STROBE signals. 0x0: Use settings defined in INSEL 0x1: Synchronization event from camera 3 0x2: Reserved	RW	0x0
18:10	DIVC	Sets the clock divisor value for the CNTCLK clock generation based on the CLK input clock. CNTCLK is an internal clock used by the TIMING CTRL module counters. Usually, CNTCLK = ISS_MAIN_FCLK / DIVC, except for some particular values shown hereafter. 0x0: No clock. CNTCLK is gated.	RW	0x000
9:0	RESERVED		R	0x000

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Table 8-237. Register Call Summary for Register TCTRL_CTRL

ISS Interfaces

- ISS TCTRL Control-Signal Generator: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
- ISS TCTRL Camera-Control Signal Generator: [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57]
- ISS TCTRL Registers: [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74] [75] [76]

Table 8-238. TCTRL_PSTRB_REPLAY

Address Offset	0x0000 0034		
Physical Address	0x5200 0434	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - PRESTROBE REPLAY REGISTER This register is used by the TIMING CTRL module to generate the prestrobe signal.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER								DELAY																							

Bits	Field Name	Description	Type	Reset
31:25	COUNTER	Sets the number of PRESTROBE pulses after the original pulse. If this bit is set to 0, the PRESTROBE signal behavior is only controlled by TCTRL_FRAME.STRB, TCTRL_PSTRB_DELAY, and TCTRL_PSTRB_LENGTH. If TCTRL_PSTRB_LENGTH=0, there is no replay. This bit is useful when one wants to enable red-eye removal.	RW	0x00
24:0	DELAY	Sets the delay for the PRESTROBE signal reassertion in cycles of the CNTCLK clock. The CNTCLK frequency is generated with the TCTRL_CTRL.DIVC bit field. The possible values are 0 to 2^{25}-1 cycles. If TCTRL_PSTRB_LENGTH=0, there is no replay. This bit field must not be set to 0 if the COUNTER is set to a value different of 0. This bit is useful when one wants to enable red-eye removal.	RW	0x0000000

Table 8-239. Register Call Summary for Register TCTRL_PSTRB_REPLAY

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2]
- ISS TCTRL Registers: [3]

Table 8-240. TCTRL_FRAME

Address Offset	0x0000 0038		
Physical Address	0x5200 0438	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - FRAME REGISTER This register is used by the TIMING CTRL module to generate the SHUTTER, PRESTROBE, and STROBE signals.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																STRB				PSTRB				SHUT							

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Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:12	STRB	Frame counter for the STROBE signal generation. From 0 to 63 frames. This bit field is ignored if TCTRL.INSEL=GRESET and TCTRL_CTRL.INSEL_OVR=0	RW	0x00
11:6	PSTRB	Frame counter for the PRESTROBE signal generation. From 0 to 63 frames. This bit field is ignored if TCTRL.INSEL=GRESET and TCTRL_CTRL.INSEL_OVR=0	RW	0x00
5:0	SHUT	Frame counter for the SHUTTER signal generation. From 0 to 63 frames. This bit field is ignored if TCTRL.INSEL=GRESET and TCTRL_CTRL.INSEL_OVR=0	RW	0x00

Table 8-241. Register Call Summary for Register TCTRL_FRAME

ISS Interfaces

- ISS TCTRL Camera-Control Signal Generator: [0] [1] [2] [3] [4] [5]
- ISS TCTRL Registers: [6] [7] [8] [9] [10]

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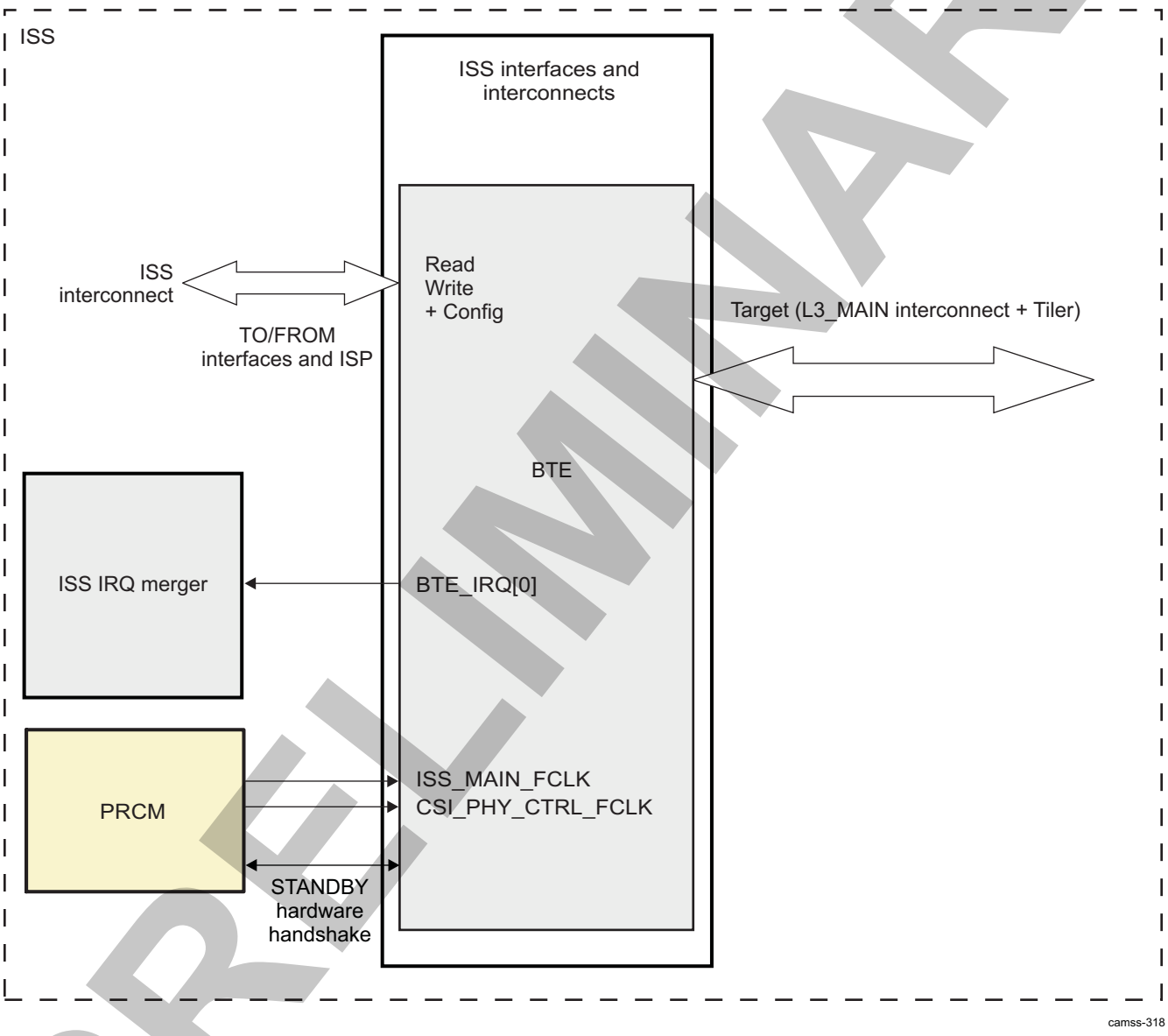
8.2.7 ISS BTE

8.2.7.1 ISS BTE Environment

There are no particular environment attributes (see Section 8.2.2, *ISS Interfaces Environment*).

8.2.7.2 ISS BTE Integration

Figure 8-81. ISS BTE Integration



For power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

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8.2.7.2.1 ISS BTE PRCM Interface

8.2.7.2.1.1 ISS BTE Power Management

8.2.7.2.1.1.1 ISS BTE PRCM Handshake

The BTE supports the IDLE protocol to flush outstanding transactions. When an IDLE request is received, the BTE:

- Completes ongoing requests on OCPI (request, data and response phases) and stalls the port (SCmdAccept = 0)
- Flushes all contexts (same behavior than when the BTE_CONTEXT_CTRL_i[2] FLUSH bit is set by software) when the BTE_CONTEXT_CTRL_i[11] AUTOFLUSH bit is set. Otherwise, no context flushing is triggered by an IDLE request.
- Completes ongoing requests on OCPO (request, data and response phases)
- Acknowledges the IDLE request.

8.2.7.3 ISS BTE Functional Description

8.2.7.3.1 ISS BTE Features

The BTE increases access efficiency of raster initiators to tiled SDRAM. In fact, the TILER expects 2D-bursts corresponding to a row or column of subtiles for maximal efficiency. For more information about SDRAM and TILER, see Section 15.2, *Dynamic Memory Manager*.

The BTE is connected between one or multiple raster initiators. It can translate reads and writes. For reads, BTE prefetches sufficient data from tiled memory to translate raster requests. For writes, BTE buffers raster requests until is has sufficient data to generate requests to tiled memory. The features of the BTE are:

- Interfaces:
  - 32-bit-wide configuration interface (OCPC)
  - 128-bit-wide slave data port (OCPI)
  - 128-bit-wide master data port (OCPO)
- Incrementing to 2D burst translation for read and writes:
  - Four contexts. A context is a virtual frame buffer attached to a data flow requiring translation.
  - One-shot and continuous mode
- Local memories for temporal storage:
  - Cannot use external memories for temporal data storage
- Transparent for accesses that do not require translation. Requests are forwarded from OCPI to OCPO without modification.
- Local buffer

8.2.7.3.2 ISS BTE Functional Description Details

The main tasks and capabilities of the BTE are:

- Forward OCP transactions that do not need translation.
- For OCP writes requiring translation:
  - Store data received from OCPI to local buffers.
  - Read data from local buffers and send it to OCPO.
- For OCP read requiring translation:
  - Store data received from OCPO to local buffers.
  - Read data from local buffers and send it to OCPI.
- BTE DMA capability

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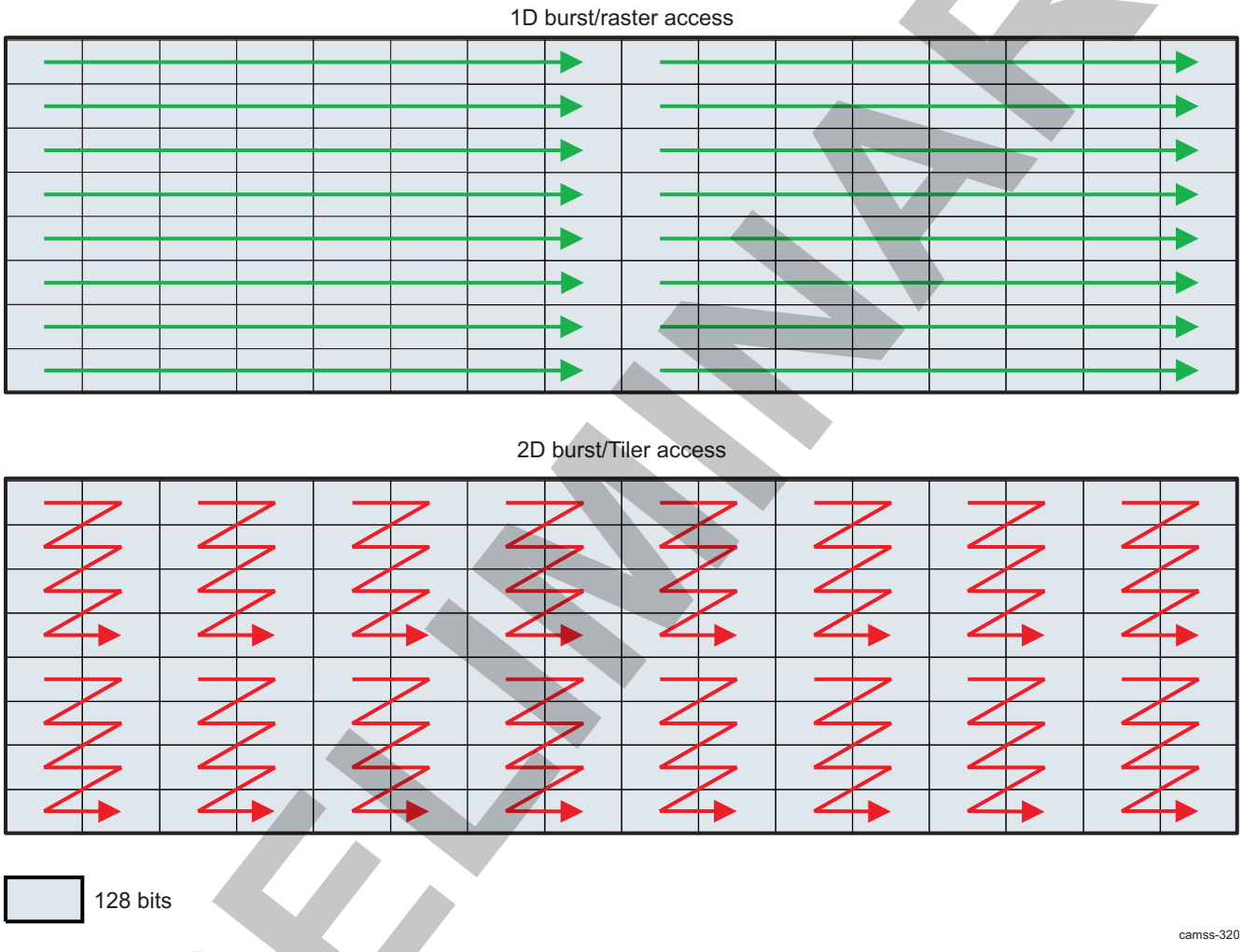
8.2.7.3.2.1 ISS BTE Burst Translation Principle

The BTE receives raster accesses from the OCPI port and generates TILER accesses on OCPO.

The BTE keeps track of the amount of data written into the local memories. For translated writes, 2D bursts are sent to OCPO when there is sufficient data in the local memory to generate TILER accesses. For translated reads, 2D burst are generated to fill the local memory with data that is returned when raster accesses are received on OCPI. Figure 8-82 shows the BTE burst translation principle.

Figure 8-82. ISS BTE Burst Translation Principle



In the following sections, three address spaces are described:

- Virtual: Corresponds to the translated address region on OCPI. Accesses performed to this address space are translated by the BTE. It can be seen as a 64 KiB x 8 k lines frame buffer. Locations in this space are expressed as byte addresses for OCP compliance. However, the access granularity is 128-bit (4 LSBs expected to be zeros). For more information about this space, see Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
- Physical: Corresponds to the addresses used to access the physical buffer of the BTE. The physical space is addressed in 128-bit-wide words. However, this document refers to byte addresses to preserve homogeneity.
- Tiler: Corresponds to addresses used by translated accesses. Locations in this space are expressed as byte addresses for OCP compliance. However, the access granularity is 128-bit (4 LSBs expected to be zeros). For more information about this space, see Section 8.2.7.3.2.5, *ISS BTE TILER Space Accesses: 2D Burst Generation*.

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8.2.7.3.2.2 ISS BTE Virtual Address Space and Context Mapping

The location of the virtual space in the address map of OCPI is set by the BTE_CTRL[11:8] BASE bit field. It always occupies 64 KiB × 8k lines = 512 MiB. Software must map a virtual space into an unused region (a region, for example, that the ISS top level cannot access).

The virtual space is decomposed into contexts. A context corresponds to a 2D region in the virtual space that requires burst translation. It can also be seen as a virtual frame buffer.

Accesses to different contexts can be interleaved at OCP transaction level. OCP transactions spanning multiple contexts are not allowed.

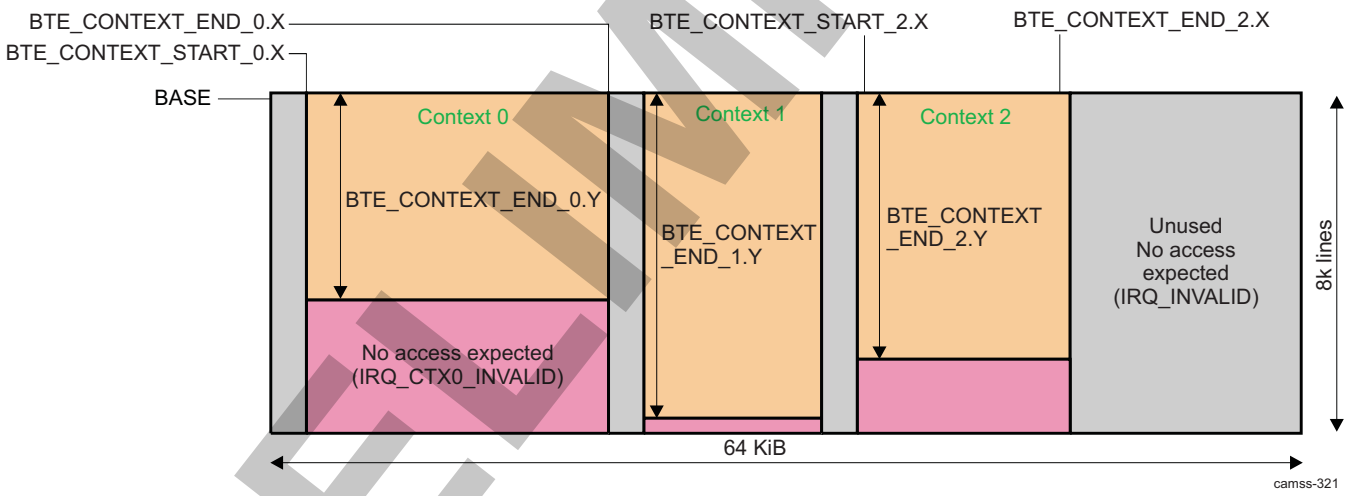
When the BTE receives an access from the OCPI port, it performs the following checks:

- If the access address is not between BASE 512 MiB and (BASE + 1) 512 MiB 1, it is handled as a transparent: request and data phases are simply forwarded to the OCPO without modification.
- If the access falls into the translated region:
  - If the access is a 2D burst, an IRQ_INVALID event is generated.
  - If the access does not map to an active context, an IRQ_INVALID event is generated. The BTE ignores bits [28:16] for this test.
  - Otherwise, context mapping is performed (see Figure 8-83).

Invalid requests are not forwarded to the OCPO.

Software must ensure that contexts do not overlap. The BTE hardware does not check for this condition. Wrong setup is likely to lead to corrupted data.

Figure 8-83. ISS BTE Context Mapping



The BTE internally keeps track of every context where the next access is expected. It internally maintains a 2D pointer, referred to as (SX_i, SY_i) in the remainder of this document. The expected byte address for an access into context x is:

ADDR = BTE_CTRL[11:8] BASE 512 MiB +
SX_i 16 bytes + SY_i 64 KiB

If an access to an unexpected location in a given context is received from OCPI, the BTE generates an IRQ_CTXx_INVALID event. The BTE provides a valid response on OCPI but does not store any data into the internal buffer. Subsequent accesses are handled normally: in other words, the BTE does not enter any specific error mode. When this happens, typically an initiator configuration is not aligned with the BTE context configuration.

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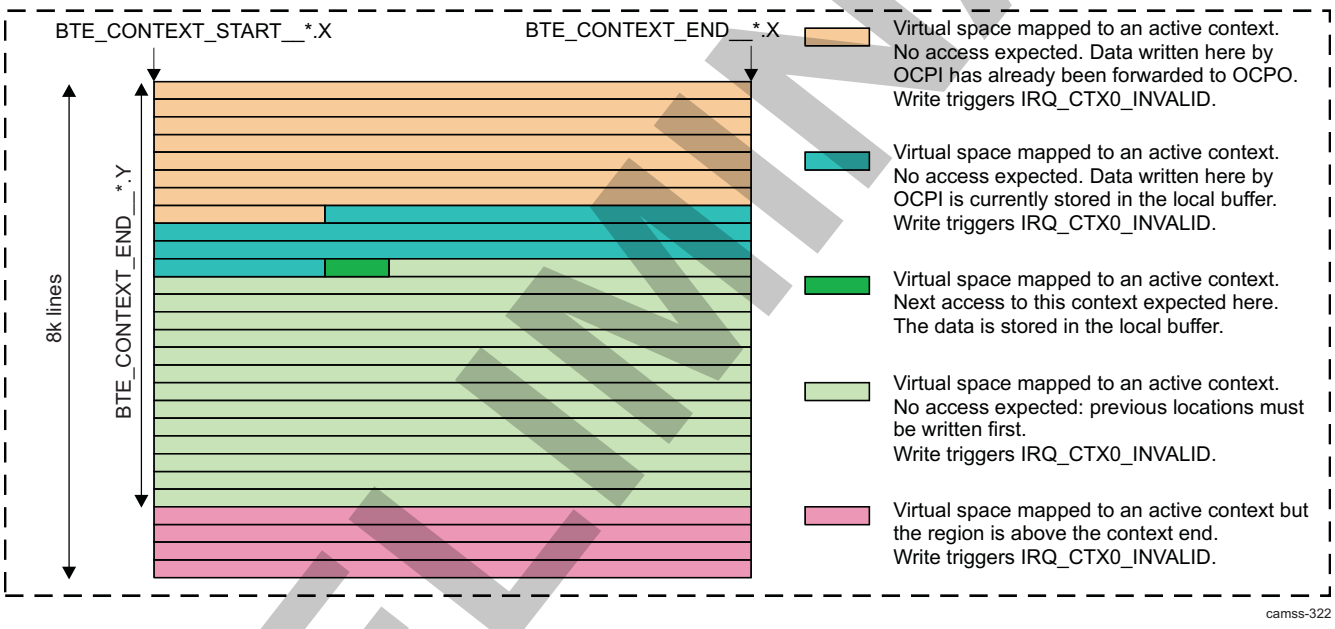
The (SX_i, SY_i) pointer of a context is updated on every access to this context. It is reset to SX_i = BTE_CONTEXT_START_i[15:7] X and SY_x = 0 when a context is enabled. SX_i is incremented by 1 for every received 16-byte word, except when it equals BTE_CONTEXT_END_i[15:4] X. In that case it is reset to BTE_CONTEXT_START_i[15:7] X and SY_i is incremented. SY_i is reset when it reaches the bottom-right corner of the context.

Therefore, the BTE can only translate raster accesses:

- Image data must be provided line by line, starting from the top-left corner of the context.
- A line stride of 64 KiB is expected.
- The maximum supported image height is 8k lines.

Figure 8-84 is an example of an active context. There is only one location in an active context where an access from OCPI is expected (green). Accesses to any other location trigger an IRQ_CTXx_INVALID event. Reads to contexts in write mode (BTE_CONTEXT_CTRL_i[7:6] MODE = 0) or writes to contexts in read mode (BTE_CONTEXT_CTRL_i[7:6] MODE = 1) trigger an IRQ_CTXx_INVALID event. When an access to an expected location is received but the burst length exceeds the context end, an IRQ_CTXx_INVALID event is triggered.

Figure 8-84. ISS BTE Expected Access Locations in the Virtual Space



Some alignment constraints are summarized as follows and are shown in Figure 8-85. They apply only to translated accesses.

- The context start addresses are aligned on 16-byte boundaries.
- The context width is aligned on 16-byte boundaries.
- The OCPI initiator must not use BYTEEN to qualify subwords in the middle of lines. The BTE interprets each BYTEEN as 0xFFFF. Access of partial words triggers an IRQ_CTXx_INVALID error.
- The line length sent by the initiator can be 1-byte aligned. The initiator can use BYTEEN to qualify valid data for the last access of the line. The BTE treats those accesses as full 16-byte writes and writes 0 data into its local buffers to complete the access. Those 0s are forwarded to OCPO when burst translation is performed. Software must ensure this data is discarded when the buffer is read back.
- The BTE does not impose any specific constraint on vertical alignment on the TILER tile and subtile grids. However, it is strongly recommended to configure the burst generation in such a way the requests performed to the TILER do not cross tile or subtile boundaries. For more information, see Section 8.2.7.3.2.5, *ISS BTE TILER Space Accesses: 2D Burst Generation*.
- The BTE accepts only one outstanding transaction per OCP tag on the OCPI port. When an initiator

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tries to generate an OCP request on a tag ID that is already used (no response has been returned on OCPI), the OCPI port is stalled.

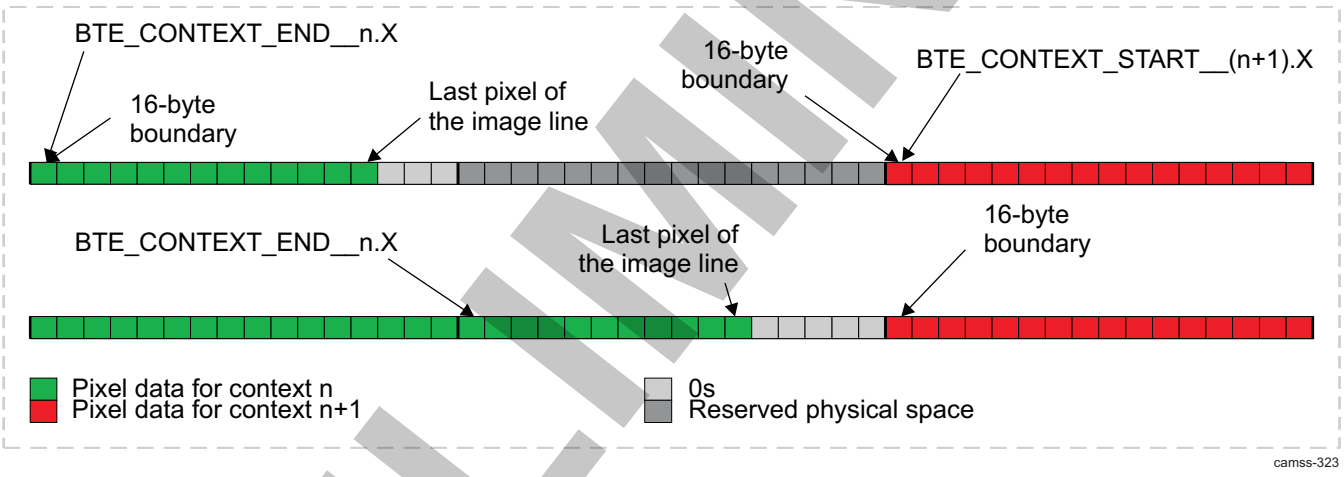
- The amount of memory allocated for each context must be a multiple of 512 bytes. Software must leave mod(BTE_CONTEXT_END_i BTE_CONTEXT_START_i + 1, 8) unused locations between the end of the context and the start of the next one. No accesses to this space from OCPI are allowed, but the BTE can use it to store data.
- While programming a BTE context, the BTE context End X value of all contexts must be less than MEMORY/64 in 128-bit address (equals MEMORY/4 in byte address)

NOTE: The generic BTE MEMORY size can be found by reading the BTE_HL_HWINFO[18:0] MEMORY bit field.

- While reading from a BTE-translated location, the CCP2 read burst size must be greater than or equal to (>=) 16 bytes (128 bits) for correct operation. Bus width translation is performed in the ISS. Therefore, 64-bit accesses lead to 128-bit accesses with BYTEEN = 0x00FF. On the BTE side, BYTEEN is always processed as 0xFFFF; thus, access to a BTE-translated 128-bit location is not correct if software uses 64-bit access.

Figure 8-85 shows the BTE context alignment constraints.

Figure 8-85. ISS BTE Context Alignment Constraints



8.2.7.3.2.3 ISS BTE TILER Context Configuration Example

Global configuration and context configuration must be done before traffic from the master can be enabled.

This section provides a configuration example used to write YUV4:2:0 data into a 90-degree rotated buffer (S = 1,/Y = 1,/X = 0). The YUV frame is made up of two objects: Y data (8 bits) and UV data (16 bits).

The BTE provides data orientation and format information to the TILER using a 33-bit address. It can be controlled by software using the BTE_CONTEXT_BASE_i and BTE_CONTEXT_CTRL_i[12] ADDR32 bits. ADDR32 must be set to 1. Bits [31:27] of the address control the accessed view format. Table 8-242 is an example of a BTE TILER context configuration.

Figure 8-86 shows BTE TILER mode addressing in 90- or 270-degree orientation.

Table 8-242. ISS BTE TILER Context Configuration Example

32	31	30	29	28	27	26 ... 4	3 ... 0
T	Orientation			Mode		Virtual Address	
1	S	/Y	/X	M1	M0	A26 ... A4	0

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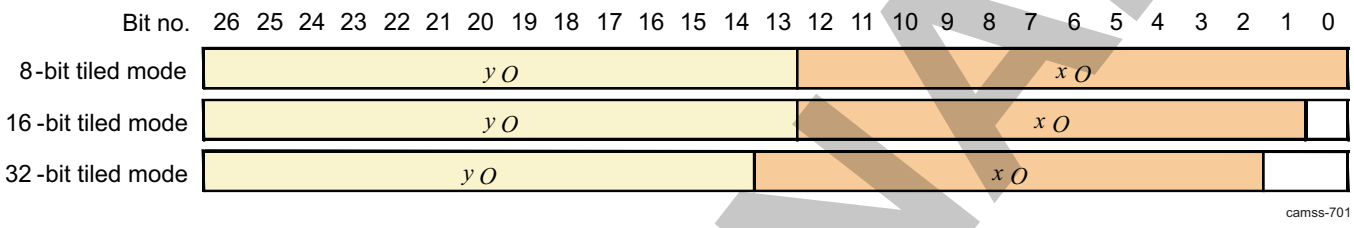
For the example described here, the following settings are used:

90-degree view, 8-bit data	ADDR[32:27] = 0b1 110 00
90-degree view, 16-bit data	ADDR[32:27] = 0b1 110 01

Software must also configure the BTE_CONTEXT_CTRL_i[9:8] GRID bit field to match the view and format set by the base address:

90-degree view, 8-bit data	GRID = 1	Stride = 8k
90-degree view, 16-bit data	GRID = 1	Stride = 8k

Figure 8-86. ISS BTE TILER Mode Addressing in 90- or 270-Degree Orientation



Bits [26:0] of the BTE_CONTEXT_BASE_i register are used to address a pixel in the virtual space of TILER. It must point to the top-left corner of the 2D object.

Software must also configure the other context register before it can start it by setting the BTE_CONTEXT_CTRL_i[0] START bit.

8.2.7.3.2.4 ISS BTE Local Memory Management

8.2.7.3.2.4.1 ISS BTE Introduction

The amount of data buffered is defined by the BTE_CONTEXT_CTRL_i[29:16] TRIGGER bit field. In write mode, translated 2D writes to OCPO are issued when the buffer fill level is greater than or equal to the value of the BTE_CONTEXT_CTRL_i[29:16] TRIGGER bit field. In read mode, translated 2D reads are sent to OCPO when the buffer level is less than the value of the BTE_CONTEXT_CTRL_i[29:16] TRIGGER bit field.

8.2.7.3.2.4.2 ISS BTE Buffer Flushing

8.2.7.3.2.4.2.1 ISS BTE One-Shot Mode

One-shot mode is enabled by setting the BTE_CONTEXT_CTRL_i[10] ONESHOT bit.

During normal operation, a data transfer from local memory to the TILER is automatically triggered when sufficient data is available in the buffer.

Three lines of data remain in the buffer once the OCPI initiator stops sending data into the context.

The BTE supports two ways to flush data remaining in the buffer:

- The last data (bottom-right corner) in a context is written. The last data is defined by the BTE_CONTEXT_END_i[15:4] X and BTE_CONTEXT_END_i[28:16] Y bit fields.
- Software writes the BTE_CONTEXT_CTRL_i[2] FLUSH bit. This is typically done when the context has been stopped before the full frame has been written.

An autoflush mode controls automatic context flushing when an IDLE request is received. It can be activated by setting the BTE_CONTEXT_CTRL_i[11] AUTOFLUSH bit to 1.

During a context flush, all remaining data in the buffer are written to the TILER.

Buffer flushing has lower priority than burst translation active contexts or forwarding transparent accesses. This prevents performance degradation.

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If software wants to abort context operation at a random location, it must disable the context.

8.2.7.3.2.4.2.2 ISS BTE Continuous Mode

When continuous mode is selected (the BTE_CONTEXT_CTRL_i[10] ONESHOT bit set to 0), reception of frame n pushes the data remaining from frame 1 out of the memory to OCPO. This mode is particularly useful when vertical blanking periods are too short to perform a buffer flush at the end of the frame. Also, it avoids creating traffic peaks due to buffer flushing.

The frame height must be a multiple of eight lines and the BTE_CONTEXT_CTRL_i[14:13] INITSY bit field must be 0x0 in continuous mode.

8.2.7.3.2.4.3 ISS BTE Buffer Prefetch

The buffer must be prefilled before read requests requiring translation can be accepted. Buffer prefetch starts with the top-left corner of the frame when a context is enabled by setting the BTE_CONTEXT_CTRL_i[0] START bit. When enough lines have been prefetched, an IRQ_CTXx_DONE event is triggered to inform software that the context is ready to perform request translation. Typically, software enables the data flow requiring translation in response to this event. Context ready for transaction and last transaction can be controlled by BTE_CONTEXT_START and BTE_CONTEXT_END, respectively.

When a read request requiring translation is received while prefetch is ongoing, an IRQ_CTXx_ERR event is triggered. It informs software that the read traffic was enabled too early. The BTE returns 0s to OCPI for the failing request (it does not hold the response until real data is available).

After prefetch completion, when a request requiring translation is received but the required data is missing (the BTE is waiting for a response from OCPO), the BTE delays the response on OCPI until the missing data is received on OCPI.

This behavior avoids stalling the OCPI port for too long (that is, a prefetch of up to 3.25 lines of data). However, it avoids getting errors because of slow OCPI responses.

8.2.7.3.2.4.4 ISS BTE Bandwidth Limiter

Translated and transparent traffic has higher priority than prefetch and flushing traffic. However, overall system bandwidth is limited. Requesting too much bandwidth for prefetch and flushing traffic may increase latencies for higher priority traffic. That could affect higher priority traffic.

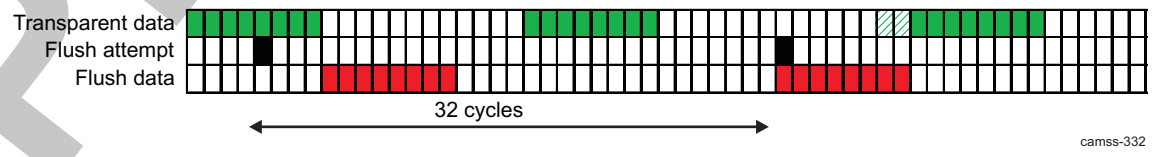
Software can limit the speed of prefetching and buffer flushing by using the BTE_CTRL[31:22] BW_LIMITER bit field. Typically, this register is used to avoid the buffer prefetch and flush traffic using all the available system bandwidth. This register does not slow down the translated or transparent traffic.

The example in Figure 8-87 assumes:

- 200-MHz functional clock
- 800 Mbps of transparent traffic = one 8 × 128-bit burst every 32 cycles

Without the bandwidth limiter, prefetch and flush traffic may use up to 3.2 0.8 = 2.4Gbps. Using BTE_CTRL[31:22] BW_LIMITER = 24 ensures that at a maximum one flush/prefetch request is issued every 32 cycles. A prefetch/flush request may be delayed by higher priority traffic of OCP port stalls. To avoid excessive traffic slowdown, the BTE tries to catch up by requesting the next flush/prefetch transaction earlier.

Figure 8-87. BTE Bandwidth Limiter Example



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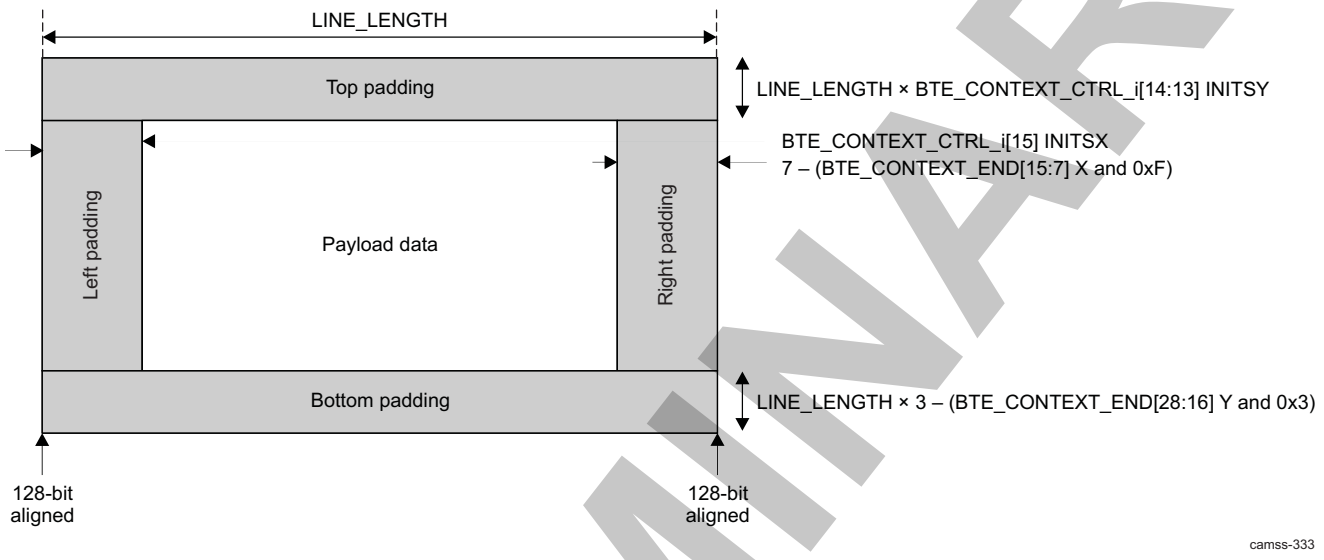
8.2.7.3.2.5 ISS BTE TILER Space Accesses: 2D Burst Generation

8.2.7.3.2.5.1 ISS BTE Buffer Fill Level

The BTE maintains an internal counter to keep track of the buffer fill level. This internal counter is used to detect when a translated OCP request is sent to the OCPO port. The counter also accounts for padding data. Figure 8-88 shows the BTE buffer fill-level padding.

Figure 8-88. ISS BTE Buffer Fill-Level Padding



In BTE context, the preferred parameter to be used is128-bit word as unit. The BTE_CONTEXT_START_i and BTE_CONTEXT_END_i registers are usually written as byte-aligned; however, the BTE_CONTEXT_START_i.X and BTE_CONTEXT_END_i.X bit fields are more readily understood (nominally) as (128 bytes = 8 x 128 bits = 8 words).

The (lower half) BTE_CONTEXT_END_i register must be written as byte-aligned, but the BTE_CONTEXT_END_i.X bit field is understood (nominally) as (128 bits = 1 word).

The BTE TRIGGER is based on word size (128 bits), but the related register (upper half) BTE_BTE_CONTEXT_CTRL_i register is not byte-aligned; it is word-aligned (128-bits).

LINE_LENGTH = ((BTE_CONTEXT_END_i[15:4] X) – BTE_CONTEXT_START_i[15:7] X) 4) & 0xFF8 + 8

NOTE: LINE_LENGTH is measured as a 128-bit word and can be used directly for TRIGGER calculation (3 * LINE_LENGTH + x)

Example 1: 64 x 15 pixels line = 64 x 15 Nb bytes in a line

(Nb bytes in a line – 16(128-bit word)) 4 = 0x3B

LINE_LENGTH = (0x3B & 0xFF8) + 8 = 0x40

TRIGGER = 0x40 * 3 + 2 = 0xC2

Example 2: 64 x 11 pixel line = 64 x 11 Nb bytes in a line

(Nb bytes in a line – 16(128-bit word)) 4 = 0x2B

LINE_LENGTH = (0x2B & 0xFF8) + 8 = 0x30

TRIGGER = 0x30 * 3 + 2 = 0x92

Figure 8-88 is a visual representation of the following explanation about how read or write events are triggered determined by the internal buffer size.

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When context is started, the buffer fill level is initialized to LINE_LENGTH × BTE_CONTEXT_CTRL_i[14:13] INITSY + BTE_CONTEXT_CTRL_i[15] INITSX (see the previous equation for the LINE_LENGTH calculation). If the BTE reads or writes, the level of the internal buffer is incremented or decremented, respectively, by the burst size. Here, only full 16-byte accesses are performed. Other OCP BYTEEN patterns are forced to 0xFF.

The BTE_CONTEXT_CTRL_i [29:16] TRIGGER bit field triggers a buffer level read or write even. In write mode, if flushing, the data level is greater than 0; if not flushing, the BTE translates to OCPO when the level is greater than or equal to the value set by the register. If the level is smaller than the BTE_CONTEXT_CTRL_i[29:16] TRIGGER software setup, then the BTE reads data.

8.2.7.3.2.5.2 ISS BTE OCP Request Generation

Except on borders:

- TILER bursts are 32 bytes × 4 lines of data blocks.
- Bursts are aligned on subtile boundaries.

The BTE maintains an internal 2D pointer (DX_i, DY_i) that corresponds to the top-left corner of the next access to be issued to the TILER. It is initialized to (0, 0) when a context is enabled or wraps around. It is updated each time an access to the TILER is performed.

Table 8-243 lists all supported TILER formats and views.

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Table 8-243. ISS BTE Supported TILER Formats and Views

Modes	View			Description	OFST	Subtile Grid		1 KiB Tile Grid		X		Y		GRID	Subtile Aligned		Tile Aligned	
	S	/Y	/X			X	Y	X	Y	LSB	MSB	LSB	MSB		X	Y	X	Y
8-bit	0	0	0	0-degree view	16384	4	4	32	32	0	13	14	26	0	[1:0]	[15:14]	[4:0]	[18:14]
	0	0	1	0-degree view with vertical mirror														
	0	1	0	0-degree view with horizontal mirror														
	0	1	1	180-degree view														
	1	0	0	90-degree view with vertical mirror	8192	4	4	32	32	0	12	13	26	1	[1:0]	[14:13]	[4:0]	[17:13]
	1	0	1	270-degree view														
	1	1	0	90-degree view														
	1	1	1	90-degree view with horizontal mirror														
16-bit	0	0	0	0-degree view	32768	8	2	64	16	0	14	15	26	2	[2:0]	[15]	[5:0]	[18:15]
	0	0	1	0-degree view with vertical mirror														
	0	1	0	0-degree view with horizontal mirror														
	0	1	1	180-degree view														
	1	0	0	90-degree view with vertical mirror	8192	4	4	32	32	0	12	13	26	1	[1:0]	[14:13]	[4:0]	[17:13]
	1	0	1	270-degree view														
	1	1	0	90-degree view														
	1	1	1	90-degree view with horizontal mirror														
32-bit	0	0	0	0-degree view	32768	8	2	64	16	0	14	15	26	2	[2:0]	[15]	[5:0]	[18:15]
	0	0	1	0-degree view with vertical mirror														
	0	1	0	0-degree view with horizontal mirror														
	0	1	1	180-degree view														
	1	0	0	90-degree view with vertical mirror	16384	8	2	64	16	0	13	14	26	3	[2:0]	[14]	[5:0]	[17:14]
	1	0	1	270-degree view														
	1	1	0	90-degree view														
	1	1	1	90-degree view with horizontal mirror														

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The BTE_CONTEXT_BASE_i and BTE_CONTEXT_CTRL_i[9:8] GRID registers must the configured by software to choose the format and view. The format must match the data stored into the virtual space. The choice of the view depends on the desired behavior.

The GRID bit field controls the used OCP stride and OCP address generation. The OCP address is generated using the following formula:

OCP_ADDR = BTE_CONTEXT_BASE_n + DX_x + DY_x << Y_LSB

Y_LSB corresponds to the Y LSB column of Table 8-243.

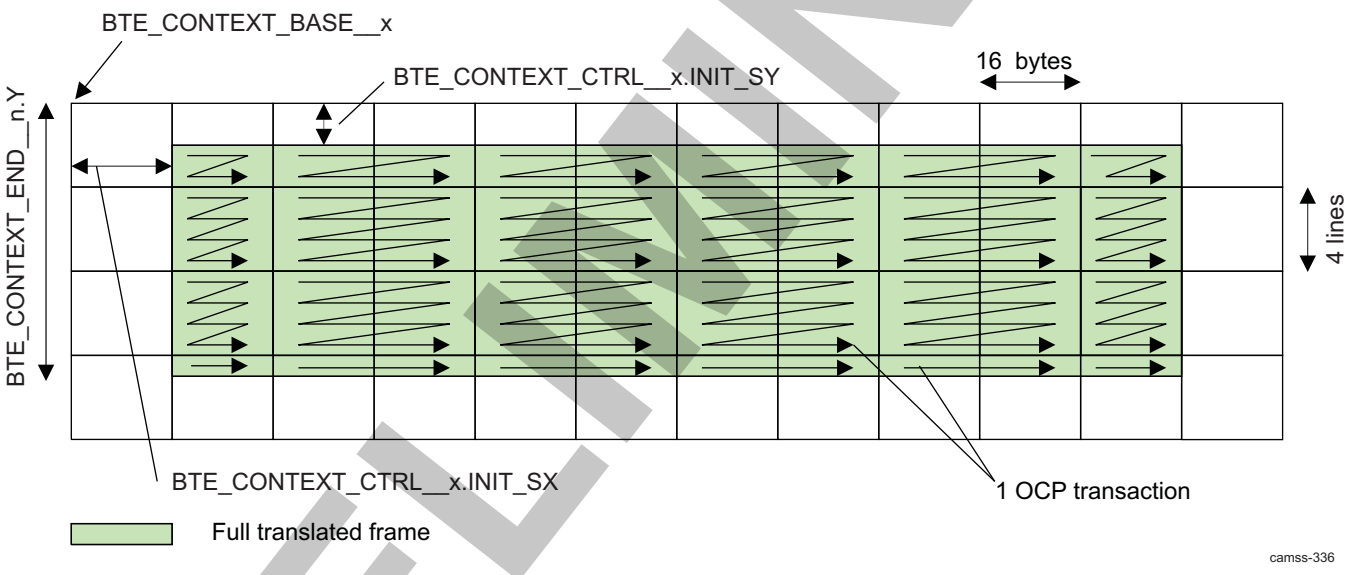
The OCP stride corresponds to the OFST column of Table 8-243. The tile and subtile grid information is currently not used by hardware.

The BTE does not automatically realign 2D bursts on tile or subtile boundaries. However, software can force the (SX_i, SY_i) (see Section 8.2.7.3.2.4, *ISS BTE Local Memory Management*, for the definition of SY_i) reset value to be used. It is set through the BTE_CONTEXT_CTRL_i[15] INITSX bit and the BTE_CONTEXT_CTRL_i[14:13] INITSY bit field.

The length and height of the 2D burst is adapted by the BTE to avoid sending dummy data to the TILER.

Figure 8-89 is an example of BTE 2D burst generation. The vertical start and end of the full 2D frame are not vertically aligned on the grid.

Figure 8-89. ISS BTE 2D Burst Generation



8.2.7.3.2.6 ISS BTE Posted and Nonposted Write Support

The BTE can handle posted and nonposted writes received on OCPI. Normally, only nonposted writes will be used.

For transparent accesses, posted and nonposted writes are forwarded to OCPO. The response provided by OCPO is returned to OCPI.

For translated accesses, the response to posted and nonposted writes is provided by the BTE. It does not wait for the response of the translated request that is sent to the TILER. In other words, the BTE has no true nonposted write support for translated accesses. The BTE does not ensure that the data has effectively been written to the destination memory when it returns the response to a nonposted translated write.

True nonposted write support is ensured for transparent accesses. Only nonposted writes must be used. Select nonposted write mode through the BTE_CTRL[5] POSTED bit.

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8.2.7.3.2.7 ISS BTE Error Reporting

Unexpected accesses are flagged using interrupts. Also, when an SResp = ERR is received on OCPO, an interrupt is triggered. If the response corresponds to a transparent access, it is forwarded to OCPI.

The BTE is not an OCP checker: It expects only valid and supported transactions from the external world.

Also, it is not intended to detect all types of software errors; few cases are detected. Those cases are described in the functional description sections.

8.2.7.3.2.8 ISS BTE Interrupts

All events generated by the module are merged into a single event at ISS level. This event can be enabled from ISS level by the ISS_HL_IRQENABLE_SET_i[11] BTE_IRQ bit. Table 8-244 lists the BTE interrupt events.

Table 8-244. ISS BTE Interrupt Events

Event	Description
IRQ_OCP_ERR	OCP error received from OCPO master port
IRQ_INVALID	An access to a location that is not mapped to any context has been performed. For more information, see Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
IRQ_CTXx_DONE	Context has been fully transferred to the TILER. This interrupt is triggered when flushing completes in one-shot mode. It is triggered once per frame in continuous mode.
IRQ_CTXx_INVALID	Unexpected address sequence or access direction (read of a context in write mode or write of a context in read mode). For more information, see Section 8.2.7.3.2.2, *ISS BTE Virtual Address Space and Context Mapping*.
IRQ_CTXx_ERR	Can occur only when a context is configured in read mode. This request triggers when a read request is received but insufficient data is buffered to perform the translation. For more information, see Section 8.2.7.3.2.4.3, *ISS BTE Buffer Prefetch*.

8.2.7.3.2.9 ISS BTE Debug Support

The BTE has no specific debug support.

8.2.7.4 ISS BTE Programming Model

8.2.7.4.1 ISS BTE Reset

The BTE can accept a general software reset, propagated through all the hierarchy. This reset can be done to initialize the module and has the same effect as the hardware reset.

1. Set the BTE_HL_SYSCONFIG[0] SOFTRESET bit to 1.
2. Read the BTE_HL_SYSCONFIG[0] SOFTRESET bit to check whether it is set to 1, which means the reset occurred.

If after five reads, the BTE_HL_SYSCONFIG[0] SOFTRESET bit still returns 0, assume that an error occurred during the reset stage.

Programmers must not set the BTE_HL_SYSCONFIG[0] SOFTRESET bit to 1 if the BTE is integrated in a subsystem; it is safer to use the software reset at subsystem level.

NOTE: A software reset does not reset the IDLE protocol signals.

8.2.7.4.2 ISS BTE Interrupts

All events are mapped to a single interrupt output, BTE_IRQ. Table 8-245 lists the procedure to configure or manage the BTE interrupts.

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Table 8-245. ISS BTE Configure/Manage Interrupts

Step	Bit Field	Value
Each event that generates an interrupt can be individually enabled by setting the appropriate bit.	BTE_HL_IRQENABLE_SET	
Each event that generates an interrupt can be individually disabled by setting the adequate bit.	BTE_HL_IRQENABLE_CLR	
When an event occurs, the corresponding bit in the BTE_HL_IRQSTATUS_RAW register is set, regardless of whether or not the event is enabled. Bits in the BTE_HL_IRQSTATUS registers are set only when an enabled event occurs.	BTE_HL_IRQSTATUS_RAW and BTE_HL_IRQSTATUS	
Software can clear a pending event by setting the adequate bit in the BTE_HL_IRQSTATUS register.	BTE_HL_IRQSTATUS	

8.2.7.4.3 ISS BTE Context Configuration

Global configuration and context configuration must be done before traffic from the master can be enabled.

This section provides a configuration example used to write YUV4:2:0 data into a 90-degree rotated buffer (S = 1,/Y = 1,/X = 0). The YUV frame consists of two objects: Y data (8 bits) and UV data (16 bits).

The BTE provides data orientation and format information to the TILER using a 33-bit address. It can be controlled by software using the BTE_CONTEXT_BASE_i and BTE_CONTEXT_CTRL_i[12] ADDR32 registers.

ADDR32 must be set to 1. Bits [31:27] of the address control the accessed view and data format. Table 8-246 gives the format of the TILER address. Figure 8-90 shows BTE tiled mode addressing in 90- or 270-degree orientation.

Table 8-. TILER Address Format

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T	Orientation			Mode		Virtual Address																										
1	S	⊳	⊱	M1	M0	A26 ... A4																			0							

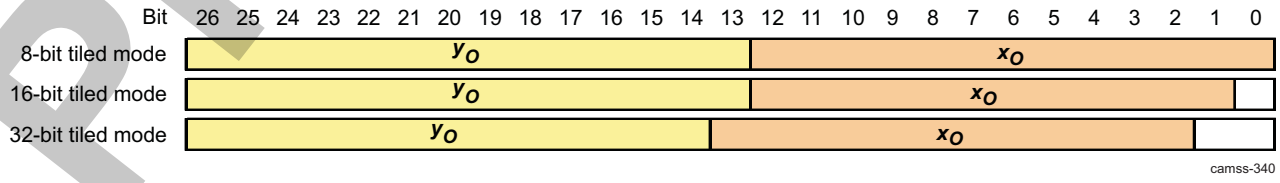
For the example described here, the following settings are used.

90-degree view, 8-bit data ADDR[32:27] = 0b1 110 00
90-degree view, 16-bit data ADDR[32:27] = 0b1 110 01

Software must also configure the BTE_CONTEXT_CTRL_i[9:8] GRID bit field to match the view and format set by the base address:

90-degree view, 8-bit data GRID = 1 Stride = 8k
90-degree view, 16-bit data GRID = 1 Stride = 8k

Figure 8-90. ISS BTE Tiled Mode Addressing in 90- or 270-Degree Orientation (S = 1)



Bits [26:0] of the BTE_CONTEXT_BASE_i register are used to address a pixel in the virtual space of the TILER. It must point to the top-left corner of the 2D object.

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Software must also configure the other context registers before it can start it by setting the BTE_CONTEXT_CTRL_i[0] START bit.

8.2.7.4.4 ISS BTE Change Context Configuration

All contexts operate independently. Software can change the configuration of an inactive context while other contexts are active and perform request translation.

When software must change the configuration of an active context, it must follow the sequence in Table 8-247.

Table 8-247. ISS BTE Change Context Configuration

Step	Bit Field	Value
Ensure that the initiator does not send any more data to this context until it is re-enabled.		
Disable the context. • The STOP condition is considered on a valid OCP boundary. • It preserves the internal states so that buffer flushing can be done. • The BTE no longer translates requests received for this context. Any transactions received for an inactive context trigger error interrupts. • The BTE completes all outstanding transactions on OCPO.	BTE_CONTEXT_CTRL_i[1] STOP	0x1
Flush all remaining data for the context, if needed. If software simply wants to abort the transfer to recover from some error condition, flushing is not needed. The context is automatically reset when it is enabled again.	BTE_CONTEXT_CTRL_i[2] FLUSH	0x1
Wait until the context completes pending OCP transaction and buffer flush (if enabled). It sets the IRQ_CTXx_DONE when it becomes idle.	BTE_HL_IRQSTATUS. IRQ_CTXx_DONE	Read 0x0
Change the context configuration.		
Enable the context by setting the BTE_CONTEXT_CTRL_i[0] START bit. Setting the START bit resets the internal state-machine of the context.	BTE_CONTEXT_CTRL_i[0] START	0x1

Alternatively, software can change the context mode to one-shot and wait until the CTXx_DONE_IRQ is triggered.

NOTE: Once a context is disabled it cannot be resumed simply by writing the START bit. In fact, doing so resets the internal FSM. If data is lost in the buffer, it will be lost.

8.2.7.5 ISS BTE Register Manual

8.2.7.5.1 ISS BTE Instance Summary

Table 8-248 lists the BTE instance.

Table 8-248. ISS BTE Instance Summary

Module Name	L3 Base Address	Size
ISS_BTE	0x5200 2000	512 bytes

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8.2.7.5.2 ISS BTE Registers

8.2.7.5.2.1 ISS BTE Register Summary

Table 8-249 summarizes the BTE registers.

Table 8-249. ISS BTE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_BTE Base Address
BTE_HL_REVISION	R	32	0x0000 0000	0x5200 2000
BTE_HL_HWINFO	R	32	0x0000 0004	0x5200 2004
BTE_HL_SYSCONFIG	RW	32	0x0000 0010	0x5200 2010
RESERVED	RW	32	0x0000 001C	0x5200 201C
BTE_HL_IRQSTATUS_RAW	RW	32	0x0000 0020	0x5200 2020
BTE_HL_IRQSTATUS	RW	32	0x0000 0024	0x5200 2024
BTE_HL_IRQENABLE_SET	RW	32	0x0000 0028	0x5200 2028
BTE_HL_IRQENABLE_CLR	RW	32	0x0000 002C	0x5200 202C
BTE_CTRL	RW	32	0x0000 0030	0x5200 2030
BTE_CTRL1	RW	32	0x0000 0034	0x5200 2034
BTE_CONTEXT_CTRL_i (1)	RW	32	0x0000 0040 + (0x20 * i)	0x5200 2040 + (0x20 * i)
BTE_CONTEXT_BASE_i (1)	RW	32	0x0000 0044 + (0x20 * i)	0x5200 2044 + (0x20 * i)
BTE_CONTEXT_START_i (1)	RW	32	0x0000 0048 + (0x20 * i)	0x5200 2048 + (0x20 * i)
BTE_CONTEXT_END_i (1)	RW	32	0x0000 004C + (0x20 * i)	0x5200 204C + (0x20 * i)

(1) i = 0 to 3

8.2.7.5.2.2 ISS BTE Register Description

through describe the BTE registers.

Table 8-250. BTE_HL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 2000	**Instance**	ISS_BTE
Description	IP revision identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See (1)

(1) TI internal data

Table 8-251. Register Call Summary for Register BTE_HL_REVISION

ISS Interfaces

- ISS BTE Registers: [0]

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Table 8-252. BTE_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5200 2004	**Instance**	ISS_BTE
Description	Information about the hardware configuration of the IP module; that is, typically, the HDL generics (if any) of the module.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESPFIFO			CONTEXTS					RESERVED															

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:21	RESPFIFO	Response FIFO size Read 0x3: 64 x 128 bits Read 0x4: 128 x 128 bits Read 0x2: 32 x 128 bits Read 0x0: Reserved Read 0x6: Reserved Read 0x1: 16 x 128 bits Read 0x7: Reserved Read 0x5: Reserved	R	0x2
20:19	CONTEXTS	Number of contexts Read 0x3: Reserved Read 0x2: 8 contexts Read 0x1: 4 contexts Read 0x0: 2 contexts	R	0x1
18:0	RESERVED	Reserved	R	0x056A0

Table 8-253. Register Call Summary for Register BTE_HL_HWINFO

ISS Interfaces

- ISS BTE Functional Description Details: [0]
- ISS BTE Registers: [1]

Table 8-254. BTE_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5200 2010	**Instance**	ISS_BTE
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IDLEMODE		RESERVED	SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: An IDLE request is acknowledged unconditionally 0x1: An IDLE request is never acknowledged 0x3: Reserved. Do not use 0x2: Smart-idle mode. Acknowledgment to an IDLE request is given based on the internal activity of the module.	RW	0x2
1	RESERVED		R	0
0	SOFTRESET	Software reset. Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0

Table 8-255. Register Call Summary for Register BTE_HL_SYSCONFIG

ISS Interfaces
- ISS BTE Reset: [0] [1] [2] [3]
- ISS BTE Registers: [4]

Table 8-256. BTE_HL_IRQSTATUS_RAW

Address Offset	0x0000 0020		
Physical Address	0x5200 2020	**Instance**	ISS_BTE
Description	Per-event raw interrupt status vector Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_ERR	IRQ_CTX6_ERR	IRQ_CTX5_ERR	IRQ_CTX4_ERR	IRQ_CTX3_ERR	IRQ_CTX2_ERR	IRQ_CTX1_ERR	IRQ_CTX0_ERR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_DONE	IRQ_CTX6_DONE	IRQ_CTX5_DONE	IRQ_CTX4_DONE	IRQ_CTX3_DONE	IRQ_CTX2_DONE	IRQ_CTX1_DONE	IRQ_CTX0_DONE	RESERVED						IRQ_INVALID	IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x0
27	IRQ_CTX3_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
26	IRQ_CTX2_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
25	IRQ_CTX1_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
24	IRQ_CTX0_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
23:20	RESERVED	Reserved	R	0x0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
15:12	RESERVED	Reserved	R	0
11	IRQ_CTX3_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
10	IRQ_CTX2_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
9	IRQ_CTX1_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
8	IRQ_CTX0_DONE	Write mode: Context has been fully transferred to the TILER Read mode: Context prefetch has completed. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
7:2	RESERVED		R	0x00
1	IRQ_INVALID	Invalid access to the virtual space Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
0	IRQ_OCP_ERR	OCP error received from OCP master port. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

Table 8-257. Register Call Summary for Register BTE_HL_IRQSTATUS_RAW

ISS Interfaces

- ISS BTE Interrupts: [0] [1]
- ISS BTE Registers: [2]

Table 8-258. BTE_HL_IRQSTATUS

Address Offset	0x0000 0024		
Physical Address	0x5200 2024	**Instance**	ISS_BTE
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_ERR	IRQ_CTX6_ERR	IRQ_CTX5_ERR	IRQ_CTX4_ERR	IRQ_CTX3_ERR	IRQ_CTX2_ERR	IRQ_CTX1_ERR	IRQ_CTX0_ERR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_DONE	IRQ_CTX6_DONE	IRQ_CTX5_DONE	IRQ_CTX4_DONE	IRQ_CTX3_DONE	IRQ_CTX2_DONE	IRQ_CTX1_DONE	IRQ_CTX0_DONE	RESERVED						IRQ_INVALID	IRQ_OCP_ERR

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0
27	IRQ_CTX3_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
26	IRQ_CTX2_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
25	IRQ_CTX1_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
24	IRQ_CTX0_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
23:20	RESERVED	Reserved	R	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
15:12	RESERVED	Reserved	R	0

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Bits	Field Name	Description	Type	Reset
11	IRQ_CTX3_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
10	IRQ_CTX2_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
9	IRQ_CTX1_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
8	IRQ_CTX0_DONE	Write mode: Context has been fully transferred to the TILER Read mode: Context prefetch has completed. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
7:2	RESERVED		R	0x00
1	IRQ_INVALID	Invalid access to the virtual space Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
0	IRQ_OCP_ERR	OCP error received from OCP master port. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

Table 8-259. Register Call Summary for Register BTE_HL_IRQSTATUS

ISS Interfaces

- ISS BTE Interrupts: [0] [1] [2] [3]
- ISS BTE Change Context Configuration: [4]
- ISS BTE Registers: [5]

Table 8-260. BTE_HL_IRQENABLE_SET

Address Offset	0x0000 0028		
Physical Address	0x5200 2028	**Instance**	ISS_BTE
Description	Per-event interrupt enable bit vector Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_ERR	IRQ_CTX6_ERR	IRQ_CTX5_ERR	IRQ_CTX4_ERR	IRQ_CTX3_ERR	IRQ_CTX2_ERR	IRQ_CTX1_ERR	IRQ_CTX0_ERR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_DONE	IRQ_CTX6_DONE	IRQ_CTX5_DONE	IRQ_CTX4_DONE	IRQ_CTX3_DONE	IRQ_CTX2_DONE	IRQ_CTX1_DONE	IRQ_CTX0_DONE	RESERVED						IRQ_INVALID	IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0
27	IRQ_CTX3_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
26	IRQ_CTX2_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
25	IRQ_CTX1_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
24	IRQ_CTX0_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
23:20	RESERVED	Reserved	R	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15:12	RESERVED	Reserved	R	0
11	IRQ_CTX3_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
10	IRQ_CTX2_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
9	IRQ_CTX1_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
8	IRQ_CTX0_DONE	Write mode: Context has been fully transferred to the TILER Read mode: Context prefetch has completed. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
7:2	RESERVED		R	0x00
1	IRQ_INVALID	Invalid access to the virtual space Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
0	IRQ_OCP_ERR	OCP error received from OCP master port. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

Table 8-261. Register Call Summary for Register BTE_HL_IRQENABLE_SET

ISS Interfaces

- ISS BTE Interrupts: [0]
- ISS BTE Registers: [1]

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Table 8-262. BTE_HL_IRQENABLE_CLR

Address Offset	0x0000 002C		
Physical Address	0x5200 202C	**Instance**	ISS_BTE
Description	Per-event interrupt enable bit vector Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_ERR	IRQ_CTX6_ERR	IRQ_CTX5_ERR	IRQ_CTX4_ERR	IRQ_CTX3_ERR	IRQ_CTX2_ERR	IRQ_CTX1_ERR	IRQ_CTX0_ERR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_DONE	IRQ_CTX6_DONE	IRQ_CTX5_DONE	IRQ_CTX4_DONE	IRQ_CTX3_DONE	IRQ_CTX2_DONE	IRQ_CTX1_DONE	IRQ_CTX0_DONE	RESERVED						IRQ_INVALID	IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0
27	IRQ_CTX3_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
26	IRQ_CTX2_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
25	IRQ_CTX1_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
24	IRQ_CTX0_ERR	Read request received before sufficient data has been prefetched. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
23:20	RESERVED	Reserved	R	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
15:12	RESERVED	Reserved	R	0
11	IRQ_CTX3_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
10	IRQ_CTX2_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
9	IRQ_CTX1_DONE	Context has been fully transferred to the TILER Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
8	IRQ_CTX0_DONE	Write mode: Context has been fully transferred to the TILER Read mode: Context prefetch has completed. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
7:2	RESERVED		R	0x00
1	IRQ_INVALID	Invalid access to the virtual space Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
0	IRQ_OCP_ERR	OCP error received from OCP master port. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Table 8-263. Register Call Summary for Register BTE_HL_IRQENABLE_CLR

ISS Interfaces

- ISS BTE Interrupts: [0]
- ISS BTE Registers: [1]

Table 8-264. BTE_CTRL

Address Offset	0x0000 0030		
Physical Address	0x5200 2030	**Instance**	ISS_BTE
Description	BTE control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BW_LIMITER								RESERVED								BASE								RESERVED		POSTED	RESERVED	TAG_CNT			

Bits	Field Name	Description	Type	Reset
31:22	BW_LIMITER	Minimum number of OCP cycles between two consecutive buffer flushing or prefetch requests. Used to limit the bandwidth used to fill/empty buffers. 0: Maximum speed. Up to 1 request every 8 cycles (3.2GB @ 200 MHz) 1: Up to 1 request every 9 cycles. 1023: Minimum speed. Up to 1 request every 1031 cycles (24MB @ 200 MHz)	RW	0x000
21:12	RESERVED		R	0x000
11:8	BASE	Base address of the virtual space translated by the BTE. Start address = BASE*512MB End address = (BASE+1)*512MB – 1 For example: BASE=3 => 0x 0 6000 0000 - 0x 0 7FFF FFFF	RW	0x0
7:6	RESERVED		R	0x0
5	POSTED	Select among posted and nonposted writes for translated requests. 0x0: Use non posted writes 0x1: Use posted writes	RW	0
4	RESERVED		R	0
3:0	TAG_CNT	BTE could use up to TAG_CNT+1 tags on OCPO. There could only be one outstanding request per tag. TAG_CNT does not control the number of requests it could handle on OCPI. This register is internally shadowed. Modifications are taken into account when there are no outstanding transactions on OCPO. TAG ID 0 to TAG_CNT are used on OCPO.	RW	0xF

Table 8-265. Register Call Summary for Register BTE_CTRL

ISS Interfaces

- ISS BTE Functional Description Details: [0] [1] [2] [3] [4]
- ISS BTE Registers: [5]

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Table 8-266. BTE_CTRL1

Address Offset	0x0000 0034		
Physical Address	0x5200 2034	**Instance**	ISS_BTE
Description	BTE control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESP_FIFO_THR							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	RESP_FIFO_THR	The BTE stops accepting new requests from OCPI (on a clean burst boundary) when the response FIFO contains more than RESP_FIFO_THR words. The reset value is FIFO_SIZE - 16 - 1. FIFO_SIZE = 8 * $2^{RESPFIFO}$	RW	0x0F

Table 8-267. Register Call Summary for Register BTE_CTRL1

ISS Interfaces

- ISS BTE Registers: [0]

Table 8-268. BTE_CONTEXT_CTRL_i

Address Offset	0x0000 0040 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 2040 + (0x20 * i)	**Instance**	ISS_BTE
Description	Context control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRIGGER								INITSX	INITSY		ADDR32	AUTOFLUSH	ONESHOT	GRID		MODE	RESERVED					FLUSH	STOP	START

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	TRIGGER	Threshold used to trigger translated requests to OCPO. Unit: words or 16 bytes Valid range: 3 lines + 2 ... 4 lines WRITE: a 2D write is issued to OCPO when the internal buffer level (including masked accesses) is superior or equal to TRIGGER READ: a 2D read is issued to OCPO when the internal buffer level (including masked accesses) is inferior to TRIGGER.	RW	0x0000
15	INITSX	Reset value to be used for SX__x. Check the section describing the local buffer management for details.	RW	0
14:13	INITSY	Reset value to be used for SY__x. Check the section describing the local buffer management for details. Must be =0 when ONESHOT=0	RW	0x0

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Bits	Field Name	Description	Type	Reset
12	ADDR32	Controls the value of the OCP address bit 32 to be used for translated accesses	RW	1
11	AUTOFLUSH	Controls automatic context flushing when an IDLE request is received 0x0: Disabled 0x1: Enabled	RW	0
10	ONESHOT	Selects one-shot or continuous mode 0x0: The context is automatically re-enabled when its end is reached. 0x1: The context is disabled when the end of a frame has been reached.	RW	0
9:8	GRID	Grid used to access the TILER 0x0: Stride = 16k Subtile = 4x4 bytes Tile = 32x32 bytes 0x1: Stride = 8k Subtile = 4x4 bytes Tile = 32x32 bytes 0x3: Stride = 16k Subtile = 8x2 bytes Tile = 64x16 bytes 0x2: Stride = 32k Subtile = 8x2 bytes Tile = 64x16 bytes	RW	0x0
7:6	MODE	Select the translation mode for the context 0x0: Write translation 0x1: Read translation 0x3: reserved 0x2: Direct access to local buffer	RW	0x0
5:3	RESERVED		R	0x0
2	FLUSH	Flushes all remaining data of the context to the TILER. Write 0x0: No effect Write 0x1: Flush	W	0
1	STOP	Stops the context on a clean OCP transaction boundary. Write 0x0: No effect Write 0x1: Stop the context	W	0
0	START	Resets the contexts internal state and enables the context on a clean OCP transaction boundary. Write 0x0: No effect Write 0x1: Reset + Enable	W	0

Table 8-269. Register Call Summary for Register BTE_CONTEXT_CTRL_i

ISS Interfaces

- ISS BTE PRCM Interface: [0] [1]
- ISS BTE Functional Description Details: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [17] [18] [19] [20] [21] [22] [23]
- ISS BTE Context Configuration: [24] [25] [26]
- ISS BTE Change Context Configuration: [27] [28] [29] [30]
- ISS BTE Registers: [31]

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Table 8-270. BTE_CONTEXT_BASE_i

Address Offset	0x0000 0044 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 2044 + (0x20 * i)	**Instance**	ISS_BTE
Description	Address of the frame buffer in the TILER address space.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																											RESERVED			

Bits	Field Name	Description	Type	Reset
31:5	ADDR	Address	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-271. Register Call Summary for Register BTE_CONTEXT_BASE_i

ISS Interfaces

- ISS BTE Functional Description Details: [0] [1] [2]
- ISS BTE Context Configuration: [3] [4]
- ISS BTE Registers: [5]

Table 8-272. BTE_CONTEXT_START_i

Address Offset	0x0000 0048 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 2048 + (0x20 * i)	**Instance**	ISS_BTE
Description	Top-left corner of the context.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																X									RESERVED							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:7	X	Address, in 128-byte words	RW	0x000
6:0	RESERVED		R	0x00

Table 8-273. Register Call Summary for Register BTE_CONTEXT_START_i

ISS Interfaces

- ISS BTE Functional Description Details: [0] [1] [2] [3] [4] [5]
- ISS BTE Registers: [6]

Table 8-274. BTE_CONTEXT_END_i

Address Offset	0x0000 004C + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 204C + (0x20 * i)	**Instance**	ISS_BTE
Description	Bottom-right corner of the context.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								Y								X												RESERVED			

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	Y	Last line number for the context (0 corresponds to a context of 1 line) Must be = 7 when ONESHOT=0	RW	0x0000
15:4	X	Address, in 128-bit words, of the last column of the context	RW	0x000
3:0	RESERVED		R	0x0

Table 8-275. Register Call Summary for Register BTE_CONTEXT_END_i

ISS Interfaces

- ISS BTE Functional Description Details: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- ISS BTE Registers: [9]

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8.2.8 ISS CBUFF

8.2.8.1 ISS CBUFF Environment

There are no particular environment attributes. See Section 8.2.2, *ISS Interfaces Environment*.

8.2.8.2 ISS CBUFF Integration

Figure 8-91 shows the integration of the CBUFF in the ISS. Because the CBUFF maps a virtual memory space from the physical memory, it therefore communicates with the ISS ISP and ISS interface modules for data to and from memory. This figure shows the normal data flow for further processing by the ISP and/or still-image coprocessor (SIMCOP) (in green) and the stall functionality of CBUFF (in red), which stall the data for a certain amount of time. An example of stalling is when the ISP processes the data faster than the input from CCP2 to memory. The CBUFF then must stall the data flow until a sufficient amount of data can be read from memory by the ISP.

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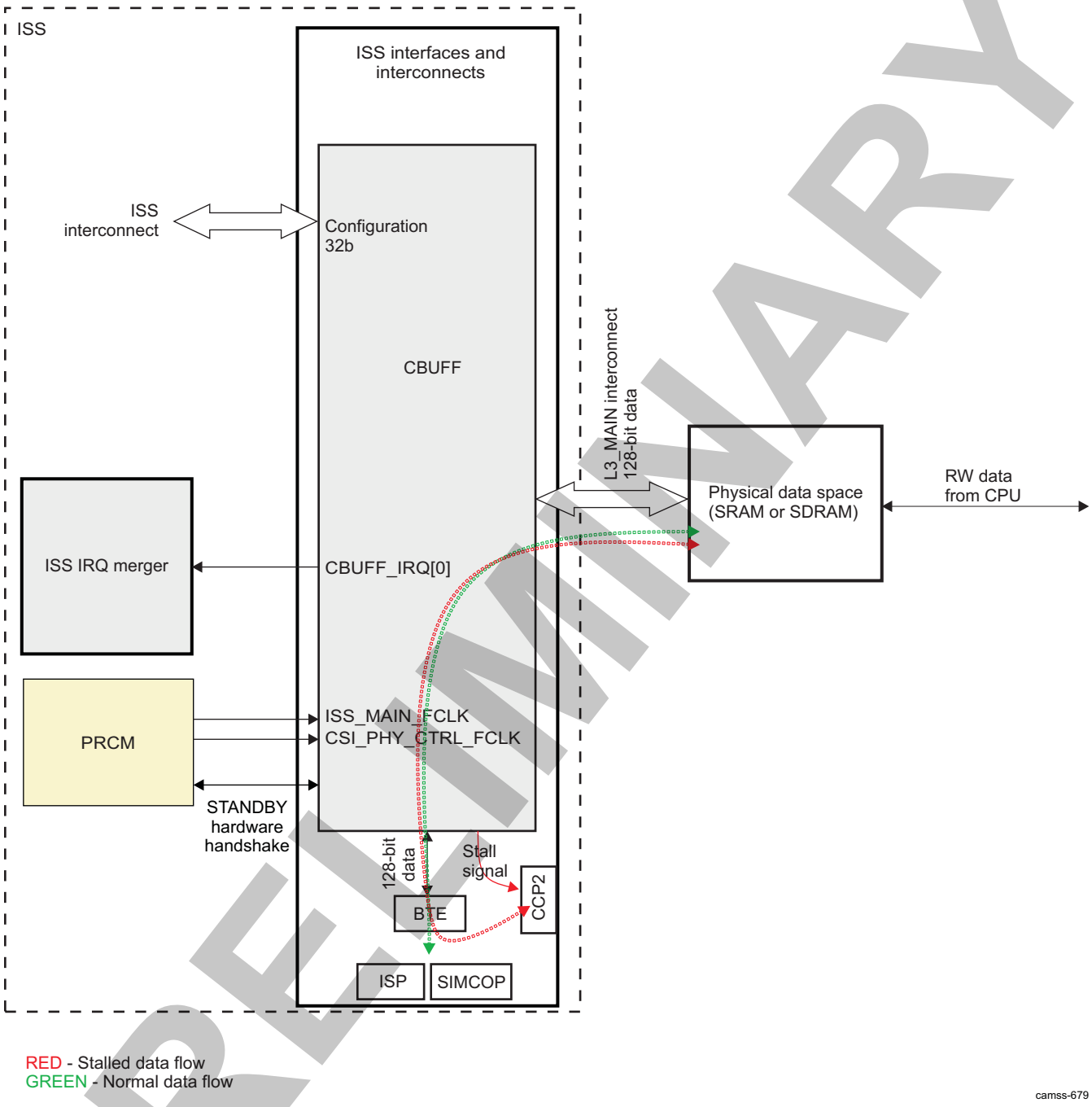
Figure 8-91. ISS CBUFF Integration



For power domain, clocks, reset, and hardware requests, see Section 8.1.2.4, *ISS Power Management*.

8.2.8.2.1 ISS CBUFF PRCM Interface

8.2.8.2.1.1 ISS CBUFF Reset and Idle Mechanism

A reset signal is provided by the PRCM module to the top-level ISS power and clock-management module.

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For standby, when none of the ISS modules require CBUFF execution actions, ISS PM executes the standby sequence, which reaches the CBUFF. When an IDLE request arrives, the CBUFF data is drained. After all transactions are drained, the CBUFF acknowledges the IDLE request to the ISS PM/CM. The IDLE request/acknowledge steps are:

When an IDLE request is received in smart-idle mode:

1. CBUFF stops accepting any new OCP requests on a clean OCP transaction boundary.
2. Waits until the interrupt output becomes inactive (no more enabled event pending)
3. Waits until all outstanding OCP transactions are complete on OCPO and OCPI. CBUFF keeps track of issued requests, data phases, and responses for that purpose.
4. CBUFF disconnects the OCPO port.
5. CBUFF acknowledges the IDLE request.

When a wake-up request is received in smart-idle mode:

1. CBUFF connects the OCPO port.
2. Starts accepting new requests from OCPI
3. Acknowledges the functional state

Idle mode is controlled through the CBUFF_HL_SYSCONFIG[3:2] IDLEMODE bit field. For software reset, it is recommended to use the global ISS reset; if a reset is required, it can be set from the CBUFF_HL_SYSCONFIG[0] SOFTRESET bit.

8.2.8.2.2 ISS CBUFF Interrupts

All events generated by the module are merged into a single event at ISS level. This event can be mapped to the MPU subsystem by enabling the ISS_HL_IRQENABLE_SET_i[10] CBUFF_IRQ bit. Table 8-276 lists the procedure to manage CBUFF interrupts.

Table 8-276. ISS CBUFF Interrupt Management

Description	Bit Field	Value
Each event that generates an interrupt can be individually enabled by setting the appropriate bit.	CBUFF_HL_IRQENABLE_SET	
Each event that generates an interrupt can be individually disabled by setting the appropriate bit.	CBUFF_HL_IRQENABLE_CLR	
When an event occurs, the corresponding bit in the CBUFF_HL_IRQSTATUS_RAW register is set regardless of whether or not the event is enabled. Bits in the CBUFF_HL_IRQSTATUS registers are only set only when an enabled event occurs	CBUFF_HL_IRQSTATUS_RAW and CBUFF_HL_IRQSTATUS	
Software can clear a pending event by setting the appropriate bit in the CBUFF_HL_IRQSTATUS register.	CBUFF_HL_IRQSTATUS	

The CBUFF can generate three events per context and one global event. All events are merged into one physical interrupt line. Table 8-277 describes the CBUFF-generated events.

Table 8-277. ISS CBUFF-Generated Events

Event	Description
IRQ_CTXx_READY	Read mode: CPU can write data to the physical window pointed by CBUFF_CTX_STATUS_i[3:0] WB.
	Write mode: CPU can read data from the physical window pointed by CBUFF_CTX_STATUS_i[3:0] WB.
	Read/write mode: The OCPI initiator has completed writing a physical window.
IRQ_CTXx_INVALID	Invalid access
	OCPI writes the virtual space of context i in read mode.
	OCPI reads the virtual space of context i in write mode.
	OCPI writes the virtual space of context i outside the CBUFF_CTX_STATUS_i[11:8] WA window in write or read/write mode.

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Table 8-277. ISS CBUFF-Generated Events (continued)

Event	Description
	OCPI reads the virtual space of context i outside the CBUFF_CTX_STATUS_i[11:8] WA window in read mode.
	OCPI reads the virtual space of context i outside the CBUFF_CTX_STATUS_i[3:0] WB window in read/write mode.
	CPU writes the DONE bit when physical windows are not ready for the CPU.
	This event indicates a wrong configuration of the CBUFF, the OCPI initiator or bogus software. When it happens, context i goes into an error state. In this state all accesses to the virtual space of context i are cancelled: they are not forwarded to the physical space. The purpose is to prevent corruption of the physical memory. Of course, the CBUFF still returns OCP responses to OCPI to ensure the integrity of the OCP.
	The error state can be left by disabling the context i and re-enabling it. Before doing so, software must ensure that there are no more outstanding requests to the virtual space of context i.
IRQ_CTXx_OVR	Physical space overflow or underflow event This event indicates a bandwidth mismatch between data producer and data consumer. When it happens, context i does not go into error state. However, the data in the physical space is likely to be corrupted.
IRQ_OCP_ERR	OCP error received in the OCPO master port. The OCP response is forwarded to OCPI normally.

8.2.8.3 ISS CBUFF Functional Description

The CBUFF maps a virtual space to a physical space by address translation. It does not change the data or store it locally.

8.2.8.3.1 ISS CBUFF Features

The ISS CBUFF features are:

- Fully transparent for accesses out of the configured virtual space
- Three functional modes:
  - Read mode: Read requests received from OCPI and forwarded after translation to OCPO. Writes are handled by an external process and acknowledged by the CPU.
  - Write mode: Write request received from OCPI and forwarded after translation to OCPO. Reads are handled by an external process and acknowledged by the CPU.
  - Read/write mode: Read and write requests received from OCPI and forwarded after translation to OCPO
- Four independent contexts
- Virtual address space (linear) mapped into a physical space (circular)
- Maximum physical buffer size of 16 × 16 MiB:
  - Physical space consists of 2, 4, 8, or 16 windows.
  - Maximum allowed window size is 16 MiB.
- Support of 2D addressing modes
- Strong error detection mechanisms to prevent data corruption caused by bogus configuration
- Addresses are 128-bit aligned, but window fill level managing is byte accurate
- Bandwidth control feedback loop to stall in initiator connected to OCPI

8.2.8.3.2 ISS CBUFF Functional Description

The CBUFF maps a virtual address space to a physical space also called circular buffer.

The CBUFF can handle up to eight contexts. For most data formats, primarily four contexts are used. In cases where YUV4:2:0 data is exchanged, two contexts are consumed by the SIMCOP (JPEG encode) coming from the resizer module, which is the ISP output module. Moreover, a context is a virtual full-frame buffer that maps to a configurable number of physical windows.

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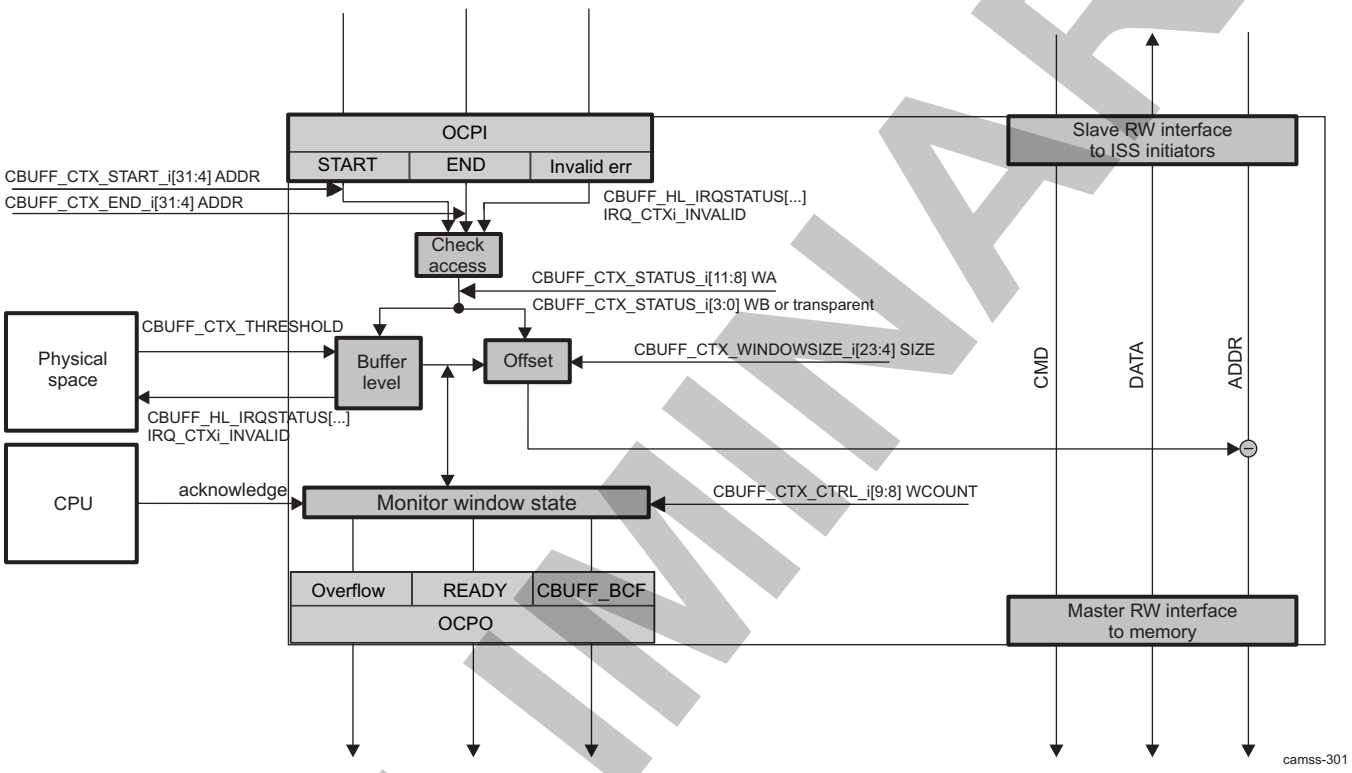
This section gives an overview of typical uses of the CBUFF.

8.2.8.3.2.1 ISS CBUFF Top-Level Diagram

Figure 8-92 shows the functional principle diagram. It does not include an exhaustive list of the interface signals or internal status registers.

A more detailed functional description is provided in the following sections.

Figure 8-92. ISS CBUFF Top-Level Diagram



8.2.8.3.2.2 ISS CBUFF Functional Modes

The CBUFF supports three functional modes (see Table 8-278).

Table 8-278. ISS CBUFF Functional Modes

Mode	Data Written by	Data Read by
Write mode	ISS initiator	CPU-controlled process
Read mode	CPU-controlled process	ISS initiator
Read/write mode	ISS initiator	ISS initiator

8.2.8.3.2.2.1 ISS CBUFF Write Mode

In write mode, the physical space is written by the CBUFF and it is read by the CPU. An IRQ_CTXx_READY event is set each time a physical window is available to be read by the CPU. This happens when the CBUFF_CTX_STATUS_i[11:8] WA pointer is moved by the CBUFF.

The CBUFF sets an IRQ_CTXx_READY event to inform the CPU that it can access the CBUFF_CTX_STATUS_i[3:0] WB physical window. The CBUFF cannot monitor CPU accesses to the physical window. The CPU must indicate when it has completed the processing of the CBUFF_CTX_STATUS_i[3:0] WB window by setting the CBUFF_CTX_CTRL_i[2:1] DONE bit field. This increments the window index CBUFF_CTX_STATUS_i[3:0] WB by one modulo the window count (defined by the CBUFF_CTX_CTRL_i[9:8] WCOUNT bit field).

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The CBUFF ensures that one IRQ_CTXx_READY event is sent to the CPU per physical window to be read. In other words, when a new IRQ_CTXx_READY event occurs before the previous one(s) is acknowledged by the CPU, it is not lost. The CBUFF memorizes the event and triggers the interrupt line again when the CPU clears it.

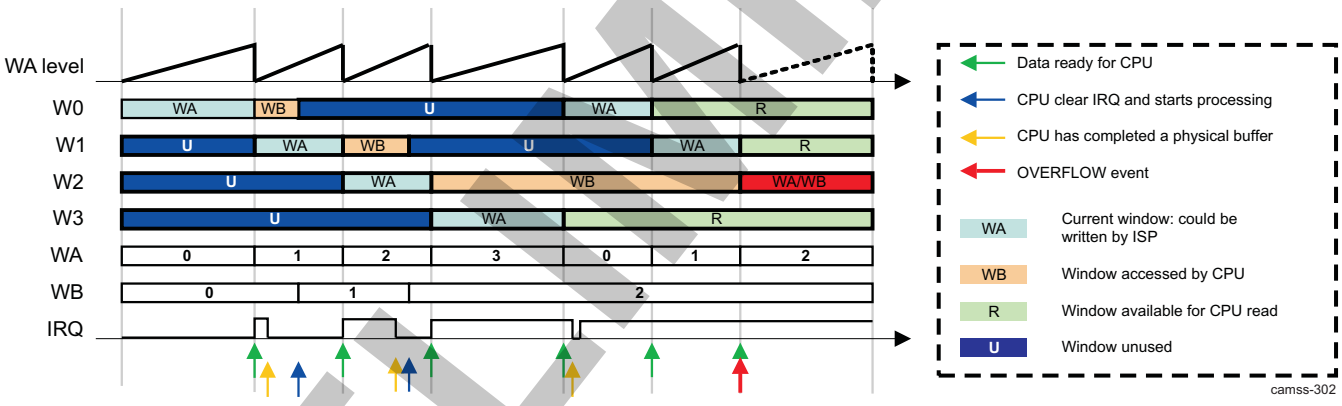
When the CPU reads the physical space too slowly, the CBUFF_CTX_STATUS_i[11:8] WA window pointer falls into the CBUFF_CTX_STATUS_i[3:0] WB window. This generates an IRQ_CTXx_OVR event when the OCPI initiator performs an access to that window. The CPU receives the IRQ_CTXx_READY event only if it is allowed to access a physical window. Therefore, it cannot generate an IRQ_CTXx_OVR event in a normal case. The OCPI initiator accesses are tracked based on activity on the OCP port.

When an IRQ_CTXx_OVR event occurs, the buffer content is likely to be corrupted. However, the CBUFF context continues processing data normally; it does not go into error state. Software must reset data generation and the CBUFF in a clean manner.

Figure 8-93 shows an example scenario with CBUFF_CTX_CTRL_i[9:8] WCOUNT = 1 (four windows). In normal operation, the CPU processes data at least at the same speed as it is written to the physical space. When this is not true, the number of windows to be read by the CPU increases. When no more physical windows are available for OCPI writes, an overflow occurs.

In the previous example, the CPU takes more time than expected to read the third buffer. Therefore, physical windows are not freed up. The OPCI initiator continues to write data into the physical window. That leads to an overflow when the OCPI initiator writes into the physical window that is read by the CPU (CBUFF_CTX_STATUS_i[11:8] WA = CBUFF_CTX_STATUS_i[3:0] WB and writes into CBUFF_CTX_STATUS_i[11:8] WA detected).

Figure 8-93. ISS CBUFF Write Mode CPU Interaction Example



(1) When there is no physical window available to be read by the CPU and the CPU writes the DONE bit, an IRQ_CTXx_INVALID event occurs.

(2) The bandwidth control feedback (BCF) feature can be used to prevent overflow. It must be supported by the module writing data into the virtual space (typically, an ISS).

8.2.8.3.2.2.2 ISS CBUFF Read Mode

In read mode, the physical space is read by the CBUFF and it is written by the CPU. An IRQ_CTXx_READY event is set each time a physical window is available to be written by the CPU. This is true until all free buffers are used.

The CBUFF sets an IRQ_CTXx_READY event to inform the CPU that it can write the CBUFF_CTX_STATUS_i[3:0] WB window. The CBUFF cannot monitor CPU accesses to the physical space. It must indicate when it completes writing the CBUFF_CTX_STATUS_i[3:0] WB window by setting the CBUFF_CTX_CTRL_i[2:1] DONE bit field. This increments the CPU window index CBUFF_CTX_STATUS_i[3:0] WB by one modulo the window count (defined by the CBUFF_CTX_CTRL_i[9:8] WCOUNT bit field).

The CBUFF ensures that one IRQ_CTXx_READY event is sent to the CPU per physical window to be written. In other words, when a new IRQ_CTXx_READY event occurs before the previous one(s) is acknowledged by the CPU, it is not lost. The CBUFF memorizes the event and triggers the interrupt line again when the CPU clears it.

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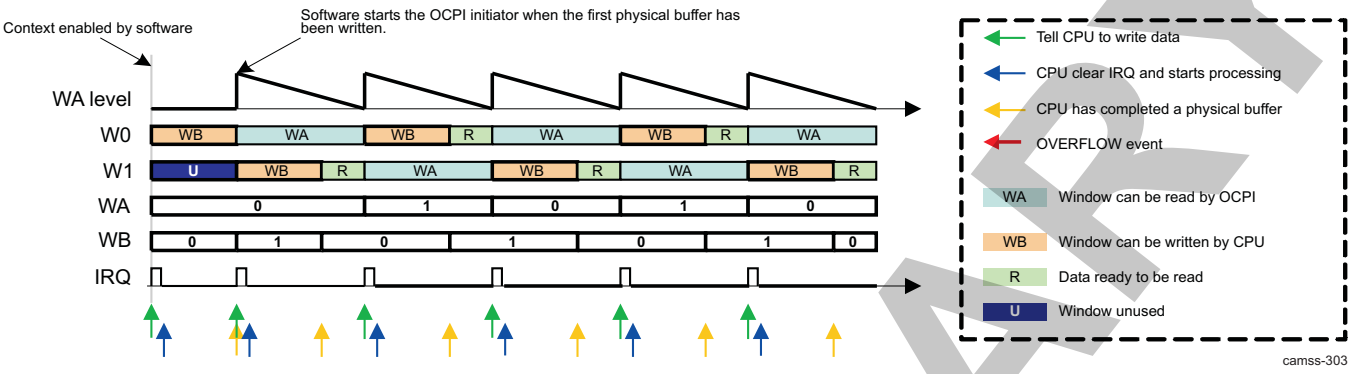
The following is an example of a normal operation in which the CPU writes data faster than it is read by the OCPI initiator. Figure 8-94 uses two physical windows (CBUFF_CTX_CTRL_i[9:8] WCOUNT = 0).

Figure 8-94. ISS CBUFF CPU Writes Data Faster Than it Is Read by the OCPI Initiator



Software must enable the ISS initiator only when at least one window is written by the CPU. Otherwise, an OVERFLOW event occurs when BCF is not used.

The CPU receives an interrupt each time a physical window is available to receive data. It clears the interrupt and then starts filling the physical window. When the buffer is completely written, it sets the CBUFF_CTX_CTRL_i[2:1] DONE bit field. This happens before the OCPI initiator has read all data from the previous physical window: the CPU must wait until the next IRQ_CTXx_READY event is received before it can write again to the physical space.

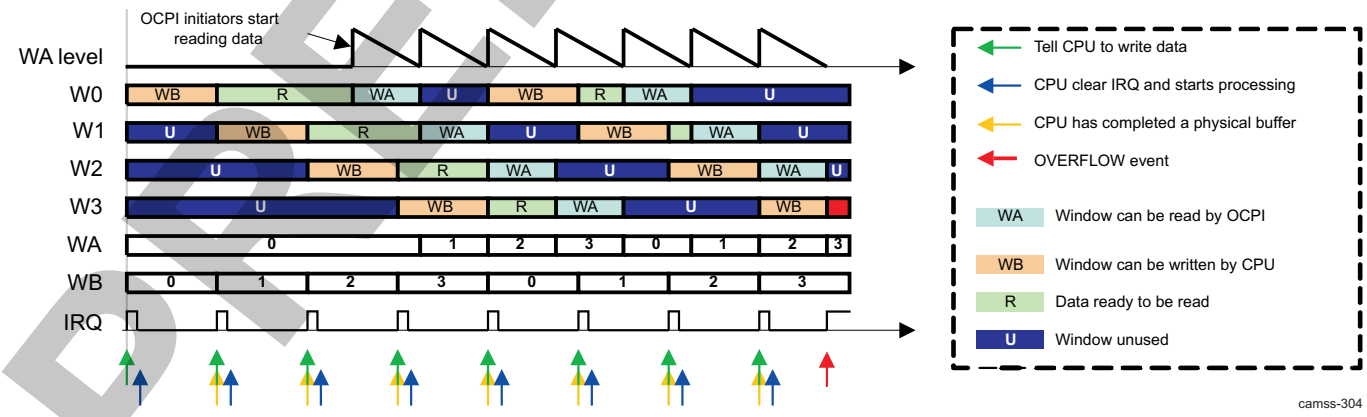
When the CPU writes buffers too slowly, the CBUFF_CTX_STATUS_i[11:8] WA window falls into the CBUFF_CTX_STATUS_i[3:0] WB window. This generates an IRQ_CTXx_OVR event only when the OCPI initiator performs reads to that window. The CPU receives the IRQ_CTXx_READY event only if it is allowed to access a physical window. Therefore, it does not generate an IRQ_CTXx_OVR event in a normal case. ISS accesses are tracked based on activity on the OCPI port.

When no buffer is available to be written by the CPU and the CPU writes the DONE bit, an IRQ_CTXx_INVALID event occurs.

When an IRQ_CTXx_OVR event occurs, the OPCI initiator reading the virtual space is likely to receive dummy data. However, the CBUFF context continues to process data normally; it does not go into error state. Software must reset the data consumer (OCPI initiator) and CBUFF context in a clean manner.

Figure 8-95 is an example of CBUFF read mode CPU interaction.

Figure 8-95. CBUFF Read Mode CPU Interaction Example



The BCF feature can be used to prevent overflow. It must be supported by the module reading data from the virtual space (typically, an ISS).

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8.2.8.3.2.2.3 ISS CBUFF Read/Write Mode

Reads and writes are performed by OCPI initiators such as a camera interface, ISP, or SIMCOP. Address translation is performed for read and write data flows. The WA pointer is used for the write data flow, and the WB pointer is used for the read data flow. Therefore, address translation for the write data flow is the same as for write mode.

In this mode, the OCPI read data flow is stalled when there is not enough data to read in the physical space. A typical application is to store data from the camera in a CBUFF and to read it back by the ISP. When the camera is slower than the ISP, the ISP stalls.

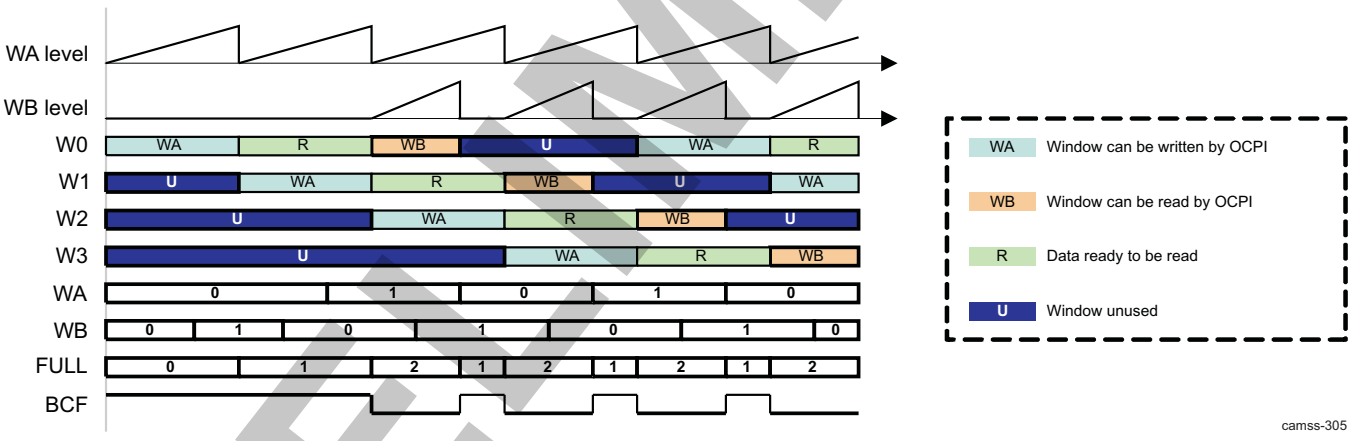
This mode does not rely on CPU synchronization. Synchronization is always performed using the BCF hardware mechanism. IRQ_CTXx_READY events are triggered in this mode when the OPCI write initiator has filled a physical window. Software can use this event for debug or performance bench marking purposes. Writes to the CBUFF_CTX_CTRL_i[2:1] DONE bit field are ignored in this mode.

The IRQ_CTXx_OVR event is triggered when an underflow occurs. In a normal case this will not occur, because the BCF signal is used to stall the read data flow when insufficient data is available in the physical space.

Figure 8-96 assumes:

- Read/write mode
- Four physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the OCPI write initiator. The BCF feature is used to stall the read initiator. CBUFF_CTX_CTRL_i[7:4] BCF = 2

Figure 8-96. ISS CBUFF Read/Write Mode Example



8.2.8.3.2.3 ISS CBUFF Events and Status Checking

8.2.8.3.2.3.1 ISS CBUFF Operations

A CBUFFx_READY_IRQ event is generated each time the CPU can read data from the CBUFF. The CPU can clear the event when it starts processing the data to avoid masking other events. The CPU can keep track of the location on the data internally or use the CBUFF registers to compute it.

The formula used is: ADDR = CBUFF_CTX_STATUS_i[3:0] WB CBUFF_CTX_WINDOWSIZE_i + CBUFF_CTX_PHY_i

When the CPU is done with processing, it must free the buffer by setting the CBUFF_CTX_CTRL_i[10] DONE bit. Otherwise, an overflow event may occur.

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The CBUFF does not keep track of EOF events. They must be managed by the CPU using the EOF event of the module that writes into the CBUFF. At the EOF, data may remain in the current write windows. For example, when the window size is set to 8 lines and the image size is 20 lines, only two window-ready events are generated for a linear addressing scheme. The remaining four lines can be read after the EOF event.

No automatic reset of the CBUFF FSM occurs at the end of the image frame. Software must reset the context by clearing the CBUFF_CTX_CTRL_i[0] ENABLEABLE bit when the frame is completely processed. A new frame can start only when the CBUFF_CTX_CTRL_i[0] ENABLEABLE bit is set.

8.2.8.3.2.3.2 ISS CBUFF Status Checking

The CBUFF provides read-only access to the CBUFF_CTX_STATUS_i[11:8] WA and CBUFF_CTX_STATUS_i[3:0] WB pointers through the CBUFF_CTX_STATUS_i register. For example, the CBUFF_CTX_STATUS_i[3:0] WB index can be used by the CPU to compute the address of a physical window. Those indexes can also be used to evaluate latency margins.

8.2.8.3.2.3.3 ISS CBUFF Register Accessibility During Frame Processing

All registers are busy-writeable registers. These registers/fields can be read or written even if the module is busy. Changes to the underlying settings occur instantly. However, module behavior is unpredictable when registers are changed during processing.

For correct operation, software must:

1. Disable all accesses to the virtual space managed by the context.
2. Disable the context by clearing the CBUFF_CTX_CTRL_i[0] ENABLEABLE bit.
3. Change the configuration.
4. Re-enable CBUFFx by setting the CBUFF_CTX_CTRL_i[0] ENABLEABLE bit.

8.2.8.3.2.4 ISS CBUFF Memory-to-Memory Operation BCF

The BCF mechanism matches the bandwidth between two processes.

The BCF feature can be used in all three CBUFF modes:

- Read mode: A CPU-controlled process writes data into physical space. The BCF signal is deasserted when the physical space contains enough data to start the read initiator connected to OCPI.
- Write mode: The BCF signal controls the write initiator connected to OCPI. When the CPU-controlled process does not read the data fast enough from the physical space, the BCF signal is asserted to stall filling of the buffer. It is deasserted when enough space is available in the physical space.
- Read/write mode: The BCF signal controls the read initiator connected to OCPI. Another initiator connected to OCPI fills the physical space. The BCF signal is deasserted when the physical space contains data that can be read by the read initiator. It is deasserted when insufficient data is available in the physical space.

The CBUFF_BCF output is controlled based on two factors:

- The window count available for the OCPI initiator to read/write
- The amount of data in the last available window (pretrigger)

The CBUFF_BCF signal is enabled by the CBUFF_CTX_CTRL_i[7:4] BCF bit field. It defines:

- Write mode: The amount of required free windows to allow writing from the ISS. In other words, when less than the required amount of BCF windows is available for ISS writes, the stall mechanism is triggered. The number of free windows is initialized to the total window count of the context. It is decreased by 1 each time the OCPI initiator finishes writing a window. It is increased by 1 each time the CPU finishes reading a window.
- Read and read/write modes: The minimum amount of required full windows to allow reading from the OCPI. When fewer than CBUFF_CTX_CTRL_i[7:4] BCF windows are available for ISS read, the stall mechanism is triggered. The number of full windows is initialized to 0. It is decreased by 1 each time the OCPI initiator completes reading a window. It is increased by 1 each time the CPU/OCPI initiator finishes writing a window.

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Figure 8-97 is an example of BCF use. It assumes:

- Write mode: OCPI writes data into physical space and the CPU reads it.
- Two physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI write initiator is faster than the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 1

Figure 8-97. ISS CBUFF Write Mode CPU Interaction Example BCF Used

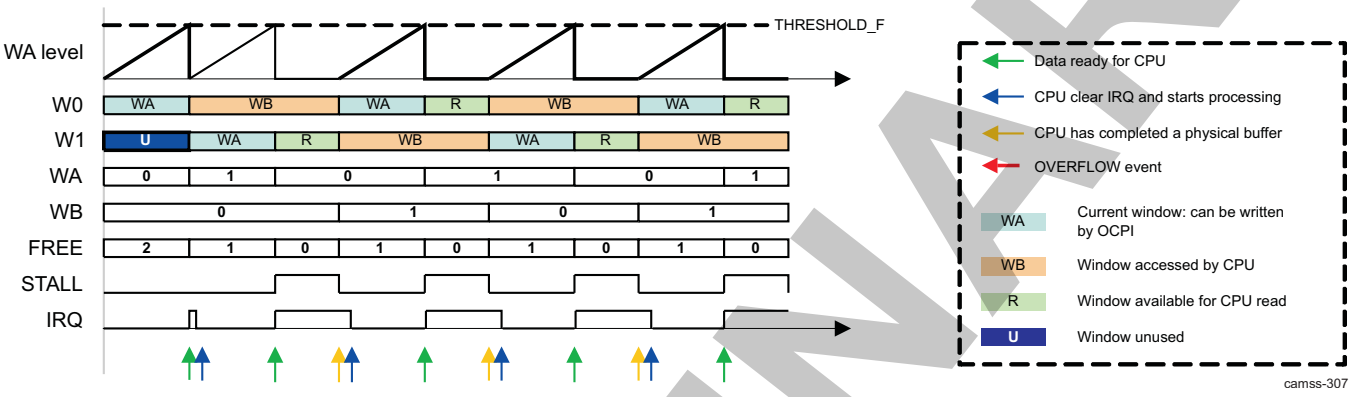

Figure 8-98 is another example. It assumes:

- Read mode: The CPU writes data into physical space and the OCPI reads it.
- Four physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the CPU. It starts after the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 2

Figure 8-98. ISS CBUFF Read Mode CPU Interaction Example (1)

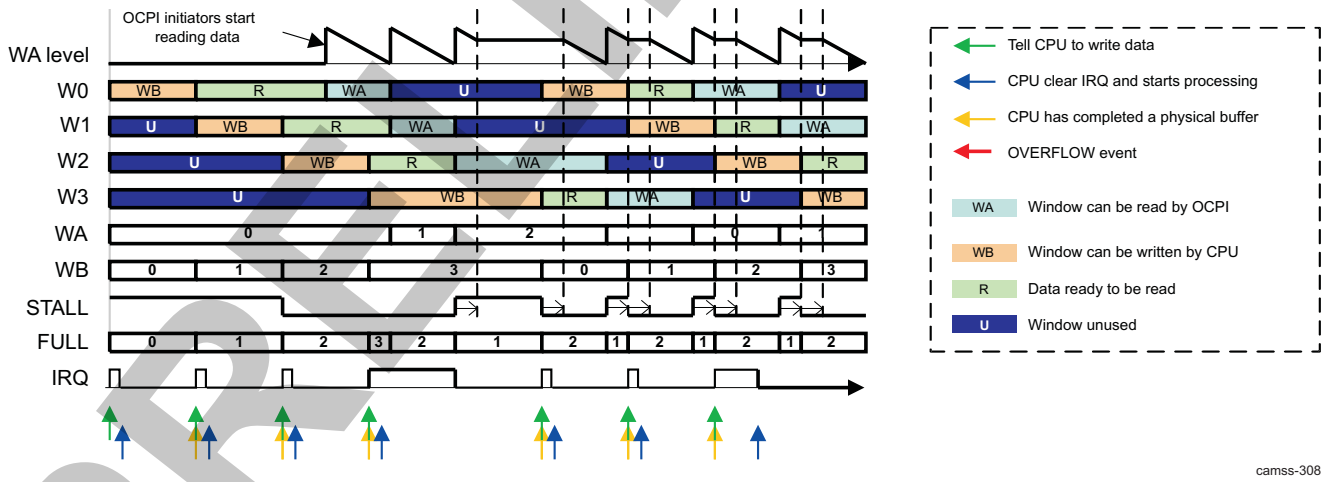

Figure 8-99 is another example. It assumes:

- Read mode: The CPU writes data into physical space and the OCPI reads it.
- Two physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the CPU. It starts after the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 1

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Figure 8-99. ISS CBUFF Read Mode CPU Interaction Example (2)

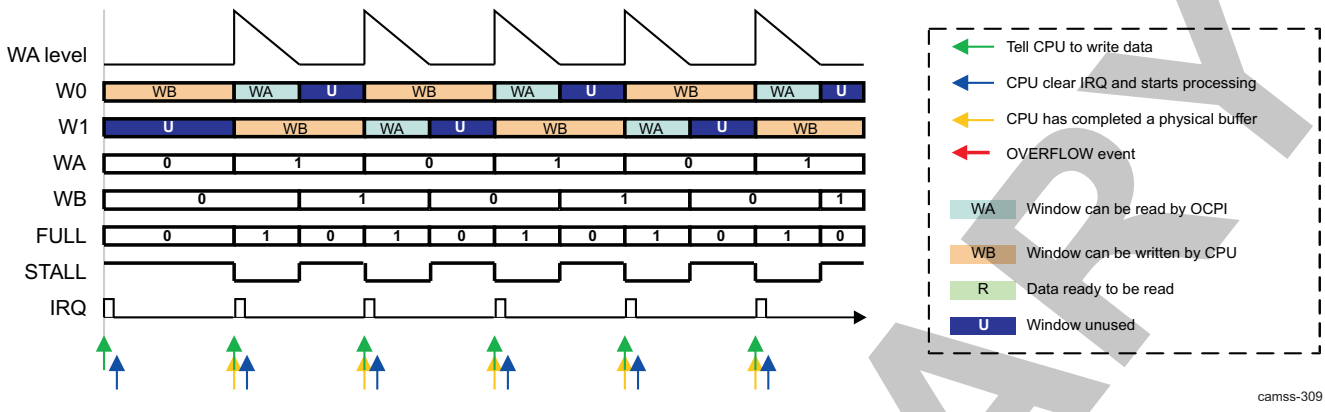

Figure 8-100 is another example. It assumes:

- Read mode: The CPU writes data into physical space and the OCPI reads it.
- Four physical windows
- CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the CPU. It starts after the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 1

CBUFF supports pretriggering the BCF signal for finer latency compensation control. This mechanism is active only for the last window available for OCPI access. It typically improves the physical space use, which is particularly useful when on-chip SRAM is used as a ping-pong buffer.

Pretriggering is controlled through the CBUFF_CTX_THRESHOLD_S_i register. It defines:

- Write mode: When the fill level of the last window available for ISS writes is greater than or equal to CBUFF_CTX_THRESHOLD_S_i, the CBUFF_BCF signal is asserted.
- Read mode: When the amount of data in the last window available for ISS reads is less than CBUFF_CTX_THRESHOLD_F_i/CBUFF_CTX_THRESHOLD_S_i, the CBUFF_BCF signal is asserted.

BCF pretriggering is disabled by setting CBUFF_CTX_THRESHOLD_S_i = CBUFF_CTX_THRESHOLD_F_i.

Figure 8-100 is an example of BCF pretriggering, assuming the following:

- Write mode: The CPU reads data from the physical space and the OCPI writes it.
- Two physical windows
- CBUFF_CTX_THRESHOLD_S_i = 1/3 CBUFF_CTX_THRESHOLD_F_i
- CBUFF_CTX_CTRL_i[7:4] BCF = 1

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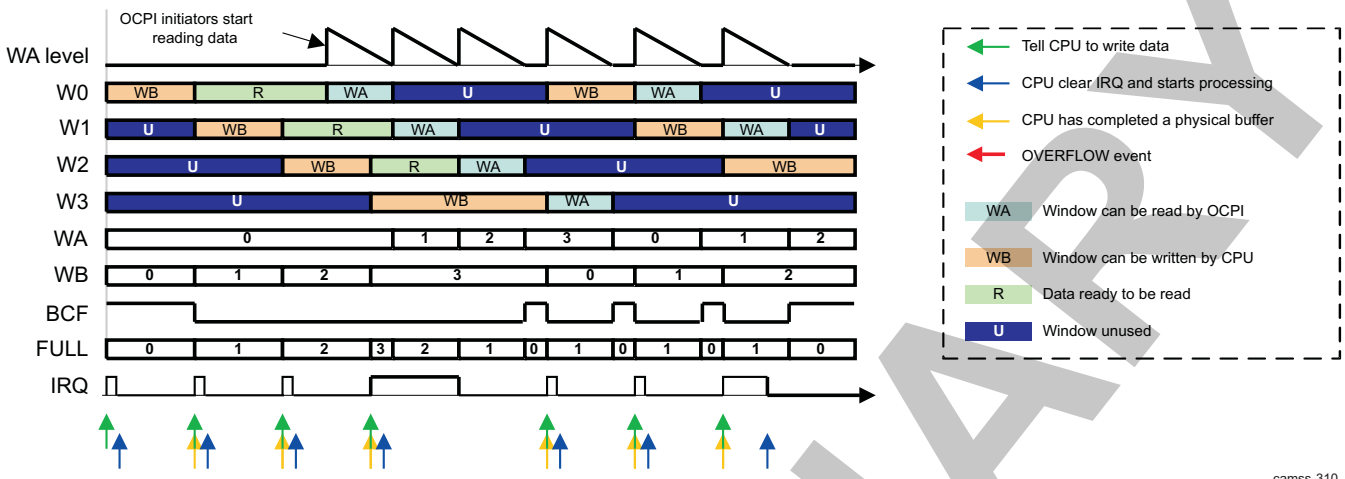
Figure 8-100. ISS CBUFF BCF Pretrigger Example: Write Mode

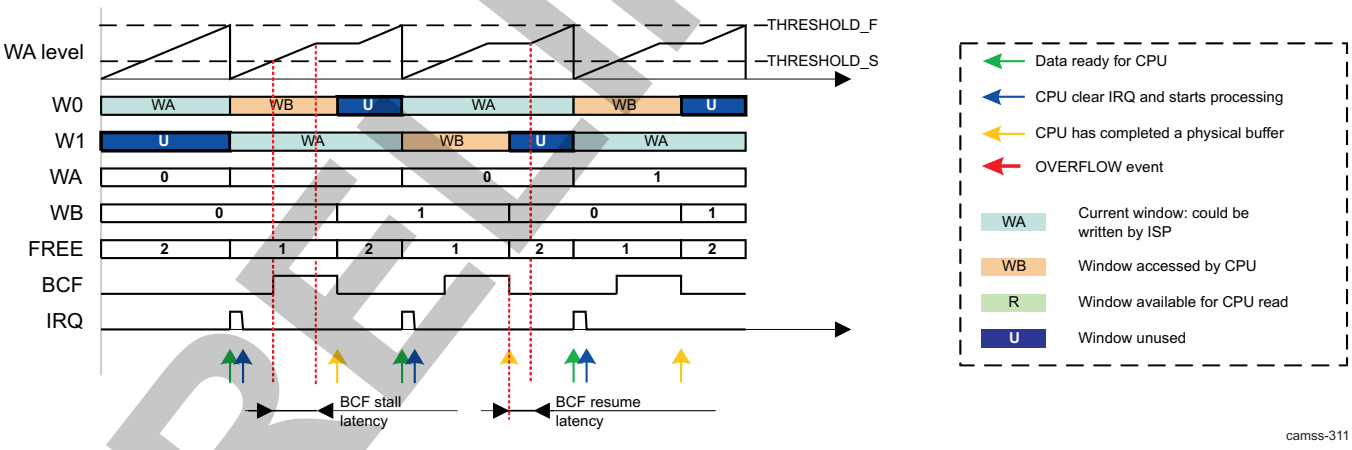


The CBUFF_BCF output signal is a logical OR of all internal BCF signals of CBUFF contexts. For example, when contexts 0 and 1 have enabled the BCF feature, both contexts can request a data flow stall.

Figure 8-101 is an example of pretriggering in read mode:

- Read mode: CPU writes data into the physical space and the OCPI reads it.
- Four physical windows
- CBUFF_CTX_THRESHOLD_S_i = 2/3 CBUFF_CTX_THRESHOLD_F_i
- The OCPI read initiator is faster than the CPU. It starts after the CPU.
- CBUFF_CTX_CTRL_i[7:4] BCF = 2

Figure 8-101. ISS CBUFF BCF Pretrigger Example: Read Mode



8.2.8.3.2.5 ISS CBUFF TILER Support

The CBUFF can translate 2D (BLOCK) bursts intended for the TILER. However, software must ensure that a given burst fits in a window.

The expected value for ADDR[32] is defined by the CBUFF_CTX_CTRL_i[11] TILERMODE bit.

- When ADDR[32] = CBUFF_CTX_CTRL_i[11] TILERMODE, the access is processed normally. ADDR[32] is not used for further processing.
- Otherwise, the access is treated as transparent.

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8.2.8.3.2.6 ISS CBUFF Window Management and Address Remapping Details

This section explains the internal address remapping and windows management algorithm. Internally, the module maintains some variables in addition to the configuration registers. The module manages multiple contexts in parallel. Table 8-279 lists the CBUFF internal variables.

Table 8-279. ISS CBUFF Internal Variables

Variable	Description
WAx	Current window index for context x. Possible values are 0 to allowed window count. The current value can be read using the CBUFF_CTX_STATUS_i[11:8] WA bit field.
WBx	Window in the physical space that can be accessed by the CPU in read/write modes. Window that is read from OCPI in read/write mode. Possible values are 0 to allowed window count. The current value can be read using the CBUFF_CTX_STATUS_i[3:0] WB bit field.
VPAx	Start address, in the virtual space, of the CBUFF_CTX_STATUS_i[11:8] WA window
	Used as a base pointer for the read (read mode) or write data flow (write, read/write modes)
	This is an internal quantity that cannot be accessed by software.
VPBx	Start address, in the virtual space, of the CBUFF_CTX_STATUS_i[3:0] WB window
	Used as a base pointer for the read data flow.
	This is an internal quantity that cannot be accessed by software.
OFFSETAx	This is an internal quantity that cannot be accessed by software.
OFFSETBx	Address offset used when WAx or WBx is accessed
LEVELAx	This is an internal quantity that cannot be accessed by software.
LEVELBx	Address offset used when WAx or WBx is accessed

8.2.8.3.2.6.1 ISS CBUFF Startup

The status of a CBUFF context is reset when it is disabled. This does not affect the configuration registers or the CBUFF_IRQSTATUS register. Table 8-280 lists the internal state after reset.

Table 8-280. ISS CBUFF Internal State After Reset

Variable	Description
WAx	0
WBx	0
VPAx VPBx	CBUFF_CTX_START_i
OFFSETAx OFFSETBx	CBUFF_CTX_START_i – CBUFF_CTX_PHY_i
LEVELAx LEVELBx	0

8.2.8.3.2.6.2 ISS CBUFF Access Identification

For each access to the virtual space (OCPI slave port), the CBUFF first checks the address to classify the transaction into one of the categories listed in Table 8-281.

Table 8-281. ISS CBUFF Address identification

Address ID	Variable	Condition
0+2*x	WA_CBUFFx	CBUFF_CTX_CTRL_i[0] ENABLE = 1 and ADDR >= VPAx and ADDR < VPAx + CBUFF_CTX_WINDOWSIZE_i and ADDR <= CBUFF_CTX_END_i and Access type = write when read/write mode is selected
1+2*x	WB_CBUFFx	CBUFF_CTX_CTRL_i[0] ENABLE = 1 and CBUFF_CTX_CTRL_i[2:1] MODE = 2 and

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Table 8-281. ISS CBUFF Address identification (continued)

Address ID	Variable	Condition
		Access type = read and ADDR>=VPBx and ADDR<VPBx + CBUFF_CTX_WINDOWSIZE_i and ADDR<= CBUFF_CTX_END_i
16+x	ERR_CBUFFx	CBUFF_CTX_CTRL_i[0] ENABLE = 1 and ADDR>= CBUFF_CTX_START_i and ADDR<= CBUFF_CTX_END_i
24	TRANSPARENT	Always true

Lower IDs correspond to higher priorities if multiple conditions are true. For example, when the current virtual window of CBUFF 0 is accessed, at least the tests for categories WA_CBUFFx and ERR_CBUFFx are true. The final category is WA_CBUFFx, because it has a higher priority.

NOTE: Tests must be performed in parallel to match the desired performance.

Further processing depends on the category:

- TRANSPARENT: Accesses flow though the module without changing its internal state or any translation.
- ERR_CBUFFx: The module goes into error state for the concerned context and sets the CBUFF_HL_IRQSTATUS.IRQ_CTXx_INVALID bit. When the module is in error state for CBUFFx, all accesses to that buffer are cancelled. In other words, any access that has an address between CBUFF_CTX_START_i and CBUFF_CTX_END_i is not transmitted to the OCPO master port. There are two ways to leave the error state:
  - Hardware reset
  - Disable and re-enable the context in error state.

    Accesses outside of the virtual space from the context in error state are not affected.
- WA_CBUFFx and WB_CBUFFx: The internal state is updated and address translation is performed when the performed access type (read or write) is compatible with the current mode (read, write, or read/write mode). Otherwise, a CBUFF_HL_IRQSTATUS.IRQ_CTXx_INVALID event is set and CBUFFx goes into the error state.

8.2.8.3.2.6.3 ISS CBUFF Address Translation

An offset is selected depending on the access category (see Section 8.2.8.3.2.6.1, *ISS CBUFF Startup*) and the internal state of the accessed buffer. Table 8-282 lists possible cases.

Table 8-282. ISS CBUFF Address Translation

Condition	Address Translation
CBUFF_CTX_CTRL_i[0] ENABLE = 1 and ADDR >= CBUFF_CTX_START_i and ADDR <= CBUFF_CTX_END_i and CBUFFx in error state	Access cancelled
Category = WA_CBUFFx	ADDROUT = ADDRIN-OFFSETAx
Category = WB_CBUFFx	Read/write mode only ADDROUT = ADDRIN-OFFSETBx
Category = ERR_CBUFFx	Access cancelled
Category = TRANSPARENT	ADDROUT = ADDRIN

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8.2.8.3.2.6.4 ISS CBUFF Window Fill Level

Each time an access is performed into an active window (WA_CBUFFx when context x is enabled) the window level is updated. The corresponding LEVELy is incremented according to the BYTEEN input of the OCPI slave port. All possible BYTEEN patterns, including nonaligned ones, are supported. Table 8-283 shows some examples. The basic idea is to count the number of 1s in the BYTEEN input for each 128-bit word and to sum the values.

Table 8-283. ISS CBUFF Window-Level Increment

BYTEEN	LEVELy Increment	Comment
0x0000	0	No access
0x0001	1	8-bit access
0x0002	1	8-bit access
0x0003	2	16-bit access
...	...	...
0x0007	3	24-bit access
...	...	...
0x000F	4	32-bit access
...	...	...
0x00F0	4	32-bit access
...	...	...
0xFFFF	16	128-bit access

The window level is compared to CBUFFx_THRESHOLD. Table 8-284 lists the situations that may occur:

Table 8-284. ISS CBUFF Window-Level Comparison(1)

Condition	Description
LEVELAx >= CBUFF_CTX_THRESHOLD_F_i	The CBUFF_CTX_STATUS_i[11:8] WA bit field of context x is full (write mode) or empty (read mode). Internal window indexes, levels, and offsets are updated.
LEVELBx >= CBUFF_CTX_THRESHOLD_F_i	Read/write mode only Window used to handle the read flow of context x is empty. Internal window indexes, levels, and offsets are updated.

(1) All situations described in Table 8-284 are mutually exclusive because only one level is updated each cycle.

8.2.8.3.2.6.5 ISS CBUFF Window Pointer and Offset Update

The following description refers to the update of WA in write mode:

When the current window of a context is full:

- A new window is opened. The update is done in a circular manner: the first physical window in is reused after the last one.
  - WA (WA + 1) modulo the number defined by CBUFF_CTX_CTRL_i[9:8] WCOUNT
  - LEVELA <- 0
  - VPA <- VPA + CBUFF_CTX_WINDOWSIZE_i
- When the window is moved from the last buffer to the first:
  - OFFSETA <- OFFSETA + CBUFF_CTX_WINDOWSIZE_i << (CBUFF_CTX_CTRL_i[9:8] WCOUNT + 1)
- Otherwise, OFFSETA does not change.

The algorithm used to update WA in read mode is the same, except that *full* refers to *all data of the window has been read* or *window empty*.

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For read/write mode, the same algorithm is used to translate reads to the WBx window. Make the following changes:

- Replace WA with WB.
- Replace LEVELA with LEVELB.
- Replace VPA with VPB.
- Replace OFFSETA with OFFSETB.

8.2.8.3.2.7 ISS CBUFF Error State

Contexts may go into error state when they receive unexpected accesses. In that case, the CBUFF does not send dummy transactions to the OCPO port. It does not forward the failing transactions to OCPO and returns valid responses (SResp = DVA) on OCPI to preserve the integrity of the OCP.

Responses may be received on OCPO while the CBUFF responds to failing transactions on OCPI. The OCPO response phase is stalled (MRespAccept = 0) during that time to prevent corruption. OCPO cannot be stalled longer than one full OCP transaction. Responses received on OCPO are handled before another internally generated response can be sent back to the OCPI. In that case, command and data phases are eventually stalled. Not stalling OCPO for too long is required to avoid affecting system performance.

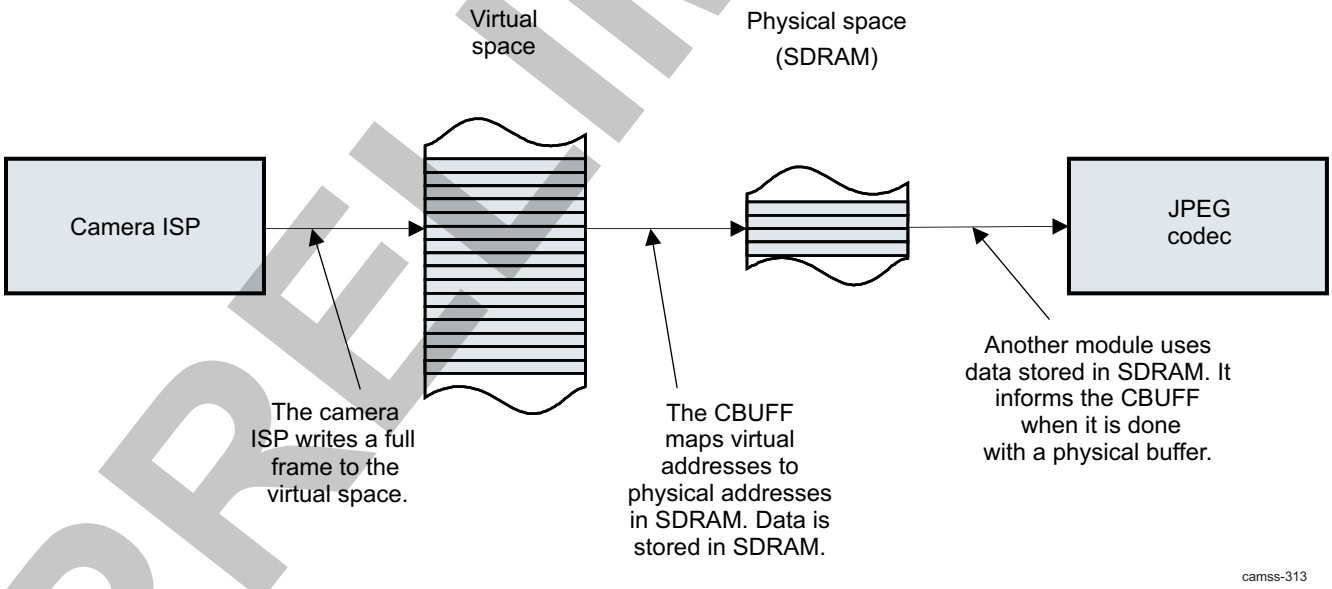
During normal operation (that is, no context is in error state), the OCPO response phase is never stalled.

8.2.8.3.2.8 ISS CBUFF Typical Configurations

8.2.8.3.2.8.1 ISS CBUFF Single-Slice Buffer

An OCP master (typically, the ISS) writes data with an incremental addressing scheme to the virtual space. The physical space is smaller than the virtual space. Therefore, physical space locations are read and written multiple times. Figure 8-102 shows the CBUFF single-slice buffer in write mode.

Figure 8-102. ISS CBUFF Single-Slice Buffer (Write Mode)



Physically, this CBUFF is in on-chip SRAM or SDRAM. The virtual space is defined by a start and end addresses. The physical space is defined by a start address, a window size, and a window count. It is contiguous in memory. When the CPU accesses physical memory for processing, it must know if the SDRAM is available for it to access and if the CBUFF is not using it. The CPU and CBUFF cannot track each other. For example, an interrupt must be triggered from the SIMCOP to the CBUFF to notify it when the processor is done working with SDRAM. For more information about the software configuration for these interrupts, see Section 8.2.8.3.2.2.1, *ISS CBUFF Write Mode*.

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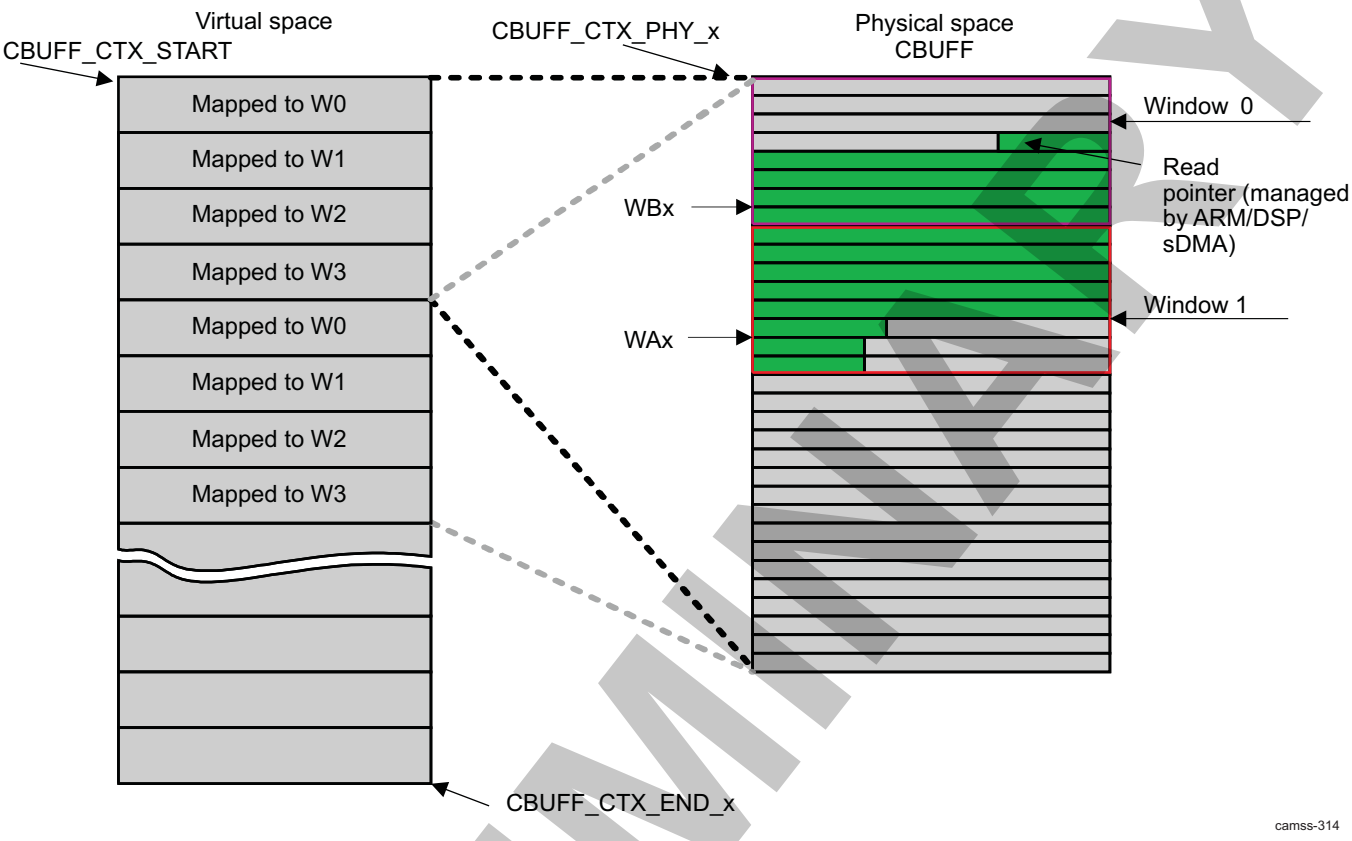
Figure 8-103 shows the buffer organization for a 4-window buffer.

Figure 8-103. ISS CBUFF Single-Slice Buffer Example (Write Mode)

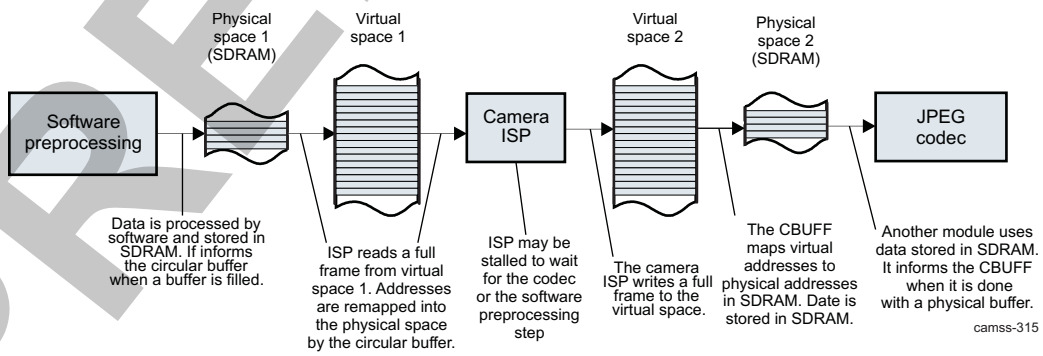


The CBUFF can manage multiple contexts in single-slice mode.

8.2.8.3.2.8.2 ISS CBUFF Extended-Slice Buffer

In extended-slice mode, at least two contexts managed by the CBUFF are used together. The two contexts provide address translation, one for the read data flow and the other for a write data flow. Figure 8-104 is an example of the CBUFF extended-slice buffer.

Figure 8-104. ISS CBUFF Extended-Slice Buffer Example



8.2.8.3.2.9 ISS CBUFF FIFO Mode

The CBUFF can behave like a FIFO to buffer data between two initiators connected to the OCPI. A typical use case is a camera interface writing data to the FIFO and an ISP reading data from the FIFO. Figure 8-105 shows the CBUFF FIFO mode.

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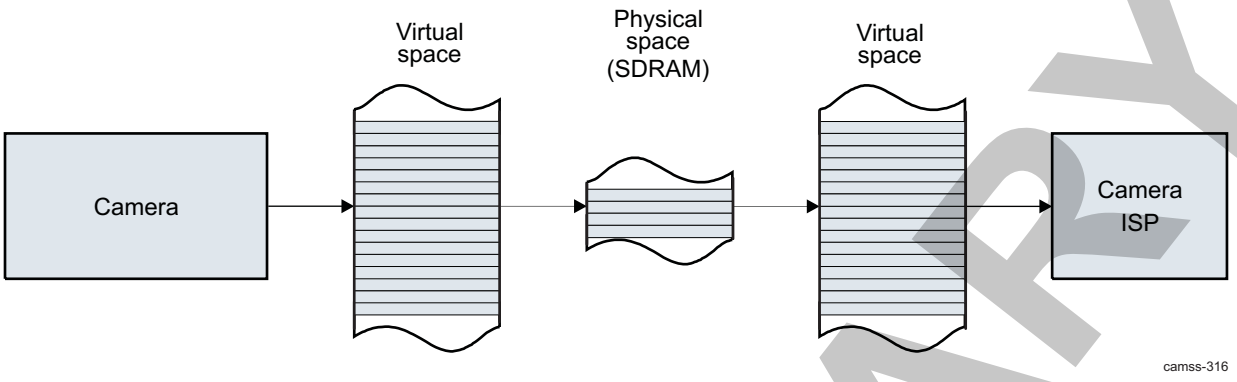
Figure 8-105. ISS CBUFF FIFO Mode

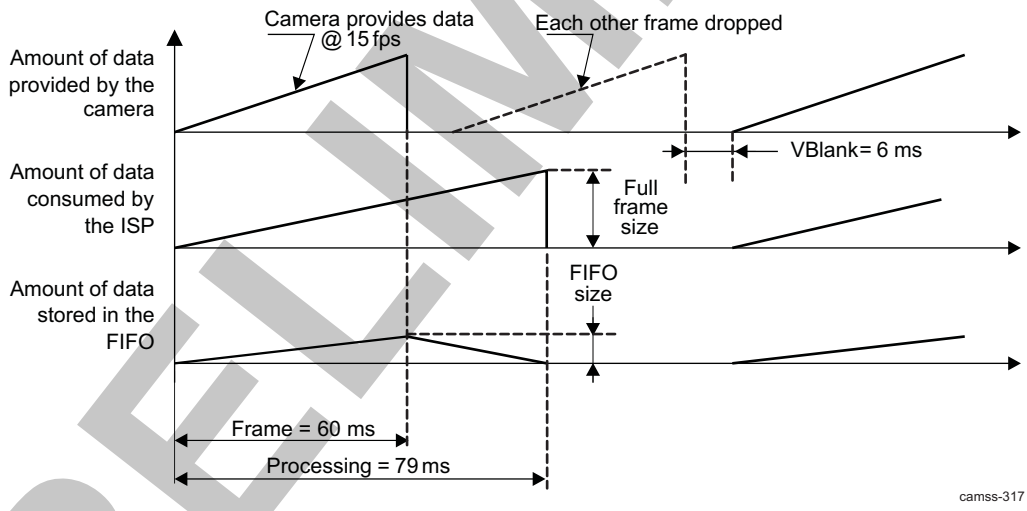


The CBUFF is used as a FIFO when the camera provides data at a higher rate than the ISP can process. To avoid storing one or multiple full-frame buffers, a FIFO buffer is used to store the data that cannot be processed immediately.

For this example, assume that the camera provides 24 MPix at 15 frames per second. A new frame is provided every 66 ms. The ISP needs 79 ms to process this frame. Therefore, the processing cannot be done on the fly, and each other frame must be dropped.

Figure 8-106 shows the accumulated amount of data provided by the camera since the start of the frame; the amount of data consumed by the ISP since it has started processing the frame; and the difference between the two, which must be stored in the FIFO.

Figure 8-106. ISS CBUFF FIFO Use Example



The FIFO is emulated as 16 windows (CBUFF_CTX_CTRL_i[9:8] WCOUNT = 0x3). The ISP is started by software when a few kilobytes of data are written to the physical space. Alternatively, the BCF mechanism can be used, but the minimum FIFO size is more complex to calculate.

The FIFO level reaches its maximum when the camera performs the last write of the frame. The camera provides the data at 1 byte/pixel 24 MPix/60 ms = 400 MBytes/s. The ISP reads data at 1 byte/pixel × 24 MPix/79 ms = 304 MBytes/s. Therefore, the minimum FIFO size is 60 ms × (400 MBytes/s – 304 MBytes/s) = 5.76 MBytes, which is four times less than a full-frame buffer.

Each window holds 256 KB of data. The camera starts writing to a new physical window every 256 KB/364 MBytes/s = 703 µs. The ISP starts reading from a new physical window every 842 µs.

The FIFO mode can also be used when the ISP is slower than the camera. In that case, the ISP is stalled when insufficient data is available in the physical space.

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8.2.8.4 ISS CBUFF Programming Model

8.2.8.4.1 ISS CBUFF Reset Behavior

Upon hardware or software reset of the CBUFF, all registers in the CBUFF are reset to their reset values

This software reset has the same effect as a hardware reset. ISS high-level software reset ensures that traffic is stopped on clear boundary because the CBUFF is sending data to and from other modules. ISS top-level reset is preferred. For more information about ISS software reset, see Section 8.1.2.3, *ISS Reset*. Submodule reset is not preferred but is available through the following registers:

1. Set the CBUFF_HL_SYSCONFIG[0] SOFTRESET bit to 1.
2. Read the CBUFF_HL_SYSCONFIG[0] SOFTRESET bit to check whether it is set to 1, which means the reset occurred.

The reset is performed without waiting until all OCP traffic stops. To avoid OCP corruption, software must ensure there is no more ongoing traffic before performing a reset.

8.2.8.4.2 ISS CBUFF Register Setup

All registers of the context to be used must be initialized for correct operation. Table 8-285 lists the procedure for the CBUFF register setup.

Table 8-285. ISS CBUFF Setup Register

Step	Bit Field	Value
Set operation mode.	CBUFF_CTX_CTRL_i[2:1] MODE	0x0: Write mode 0x1: Read mode 0x2: Read/write mode 0x3: Reserved
Define the virtual address range managed by the CBUFF. It usually corresponds to the address region where one image frame is written by the OCPI initiator.	CBUFF_CTX_START_i and CBUFF_CTX_END_i	
Define the start address of the physical buffer.	CBUFF_CTX_PHY_i	
Set the window count and size. The window size usually depends on the use of the buffer. Eight or 16 video lines correspond to a current size for JPEG video compression. A higher window count provides better latency-related overflow protection.	CBUFF_CTX_CTRL_i[9:8] WCOUNT and CBUFF_CTX_WINDOWSIZE_i	
When the 2D addressing capability is not used, set to the window size in CBUFF_CTX_THRESHOLD_F_i. Otherwise, it is set to a smaller value depending on the buffer organization. For example, when each window corresponds to lines by 4096 pixels, but the ISP sends lines of only 2560 pixels, CBUFF_CTX_WINDOWSIZE_i = 8 4096 and CBUFF_CTX_THRESHOLD_F_i = 8 2560.	CBUFF_CTX_THRESHOLD_F_i	
BCF signal-generation configuration is optional.	CBUFF_CTX_THRESHOLD_S_i and CBUFF_CTX_CTRL_i[7:4] BCF	
Enable the module. It can be disabled by clearing the ENABLE bit. This must be done only when there are no more outstanding requests to the virtual space managed by CBUFFx. All internal FSMs and counters of the CBUFF are reset when it is disabled. Pending interrupts are not affected.	CBUFF_CTX_CTRL_i[0] ENABLE	

8.2.8.5 ISS CBUFF Register Manual

8.2.8.5.1 ISS CBUFF Instance Summary

Table 8-286 lists the CBUFF instance.

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Table 8-286. ISS CBUFF Instance Summary

Module Name	L3 Base Address	Size
ISS_CBUFF	0x5200 1800	512 bytes

8.2.8.5.2 ISS CBUFF Registers

8.2.8.5.2.1 ISS CBUFF Register Summary

Table 8-287 summarizes the CBUFF registers.

Table 8-287. ISS CBUFF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CBUFF Base Address
CBUFF_HL_REVISION	R	32	0x0000 0000	0x5200 1800
CBUFF_HL_HWINFO	R	32	0x0000 0004	0x5200 1804
CBUFF_HL_SYSCONFIG	RW	32	0x0000 0010	0x5200 1810
RESERVED	RW	32	0x0000 001C	0x5200 181C
CBUFF_HL_IRQSTATUS_RAW	RW	32	0x0000 0020	0x5200 1820
CBUFF_HL_IRQSTATUS	RW	32	0x0000 0024	0x5200 1824
CBUFF_HL_IRQENABLE_SET	RW	32	0x0000 0028	0x5200 1828
CBUFF_HL_IRQENABLE_CLR	RW	32	0x0000 002C	0x5200 182C
CBUFF_CTX_CTRL_i (1)	RW	32	0x0000 0100 + (0x20 * i)	0x5200 1900 + (0x20 * i)
CBUFF_CTX_START_i (1)	RW	32	0x0000 0104 + (0x20 * i)	0x5200 1904 + (0x20 * i)
CBUFF_CTX_END_i (1)	RW	32	0x0000 0108 + (0x20 * i)	0x5200 1908 + (0x20 * i)
CBUFF_CTX_WINDOWSIZE_i (1)	RW	32	0x0000 010C + (0x20 * i)	0x5200 190C + (0x20 * i)
CBUFF_CTX_THRESHOLD_F_i (1)	RW	32	0x0000 0110 + (0x20 * i)	0x5200 1910 + (0x20 * i)
CBUFF_CTX_THRESHOLD_S_i (1)	RW	32	0x0000 0114 + (0x20 * i)	0x5200 1914 + (0x20 * i)
CBUFF_CTX_STATUS_i (1)	R	32	0x0000 0118 + (0x20 * i)	0x5200 1918 + (0x20 * i)
CBUFF_CTX_PHY_i (1)	RW	32	0x0000 011C + (0x20 * i)	0x5200 191C + (0x20 * i)

(1) i = 0 to 3

8.2.8.5.2.2 ISS CBUFF Register Description

through describe the CBUFF registers.

Table 8-288. CBUFF_HL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 1800	**Instance**	ISS_CBUFF
Description	IP revision identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 8-289. Register Call Summary for Register CBUFF_HL_REVISION

ISS Interfaces
- ISS CBUFF Registers: [0]

Table 8-290. CBUFF_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5200 1804	**Instance**	ISS_CBUFF
Description	Information about the IP module's hardware configuration.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													CONTEXTS		ENABLE_FRAGMENTATION

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:1	CONTEXTS	Number of contexts Read 0x3: Reserved Read 0x2: 8 contexts Read 0x1: 4 contexts Read 0x0: 2 contexts	R	0x1
0	ENABLE_FRAGMENTATION	Provides information to software if fragmentation support is available Read 0x1: Yes Read 0x0: No	R	0

Table 8-291. Register Call Summary for Register CBUFF_HL_HWINFO

ISS Interfaces
- ISS CBUFF Registers: [0]

Table 8-292. CBUFF_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5200 1810	**Instance**	ISS_CBUFF
Description	Clock management configuration		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters IDLE state. Backup mode, for debug only. 0x3: Reserved 0x2: Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's IDLE requests, depending on the IP module's internal requirements. IP module must not generate (IRQ- or DMA-request-related) wake-up events.	RW	0x2
1	RESERVED		R	0
0	SOFTRESET	Software reset Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0

Table 8-293. Register Call Summary for Register CBUFF_HL_SYSCONFIG

ISS Interfaces

- ISS CBUFF PRCM Interface: [0] [1]
- ISS CBUFF Reset Behavior: [2] [3]
- ISS CBUFF Registers: [4]

Table 8-294. CBUFF_HL_IRQSTATUS_RAW

Address Offset	0x0000 0020		
Physical Address	0x5200 1820	**Instance**	ISS_CBUFF
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ_CTX7_OVR	IRQ_CTX6_OVR	IRQ_CTX5_OVR	IRQ_CTX4_OVR	IRQ_CTX3_OVR	IRQ_CTX2_OVR	IRQ_CTX1_OVR	IRQ_CTX0_OVR	IRQ_CTX7_INVALID	IRQ_CTX6_INVALID	IRQ_CTX5_INVALID	IRQ_CTX4_INVALID	IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	IRQ_CTX7_READY	IRQ_CTX6_READY	IRQ_CTX5_READY	IRQ_CTX4_READY	IRQ_CTX3_READY	IRQ_CTX2_READY	IRQ_CTX1_READY	IRQ_CTX0_READY	RESERVED							IRQ_OCP_ERR

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0
27	IRQ_CTX3_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
26	IRQ_CTX2_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
25	IRQ_CTX1_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
24	IRQ_CTX0_OVR	Buffer overflow event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
23:20	RESERVED	Reserved	R	0
19	IRQ_CTX3_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
18	IRQ_CTX2_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
17	IRQ_CTX1_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
16	IRQ_CTX0_INVALID	Invalid access. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
15:12	RESERVED	Reserved	R	0
11	IRQ_CTX3_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
10	IRQ_CTX2_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
9	IRQ_CTX1_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
8	IRQ_CTX0_READY	The WB physical window is ready to be accessed by the CPU. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
7:1	RESERVED		R	0x00
0	IRQ_OCP_ERR	OCP error received in the master port. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

Table 8-295. Register Call Summary for Register CBUFF_HL_IRQSTATUS_RAW

ISS Interfaces

- ISS CBUFF Interrupts: [0] [1]
- ISS CBUFF Registers: [2]

Table 8-296. CBUFF_HL_IRQSTATUS

Address Offset	0x0000 0024		
Physical Address	0x5200 1824	**Instance**	ISS_CBUFF
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				IRQ_CTX3_OVR	IRQ_CTX2_OVR	IRQ_CTX1_OVR	IRQ_CTX0_OVR	RESERVED				IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	RESERVED				IRQ_CTX3_READY	IRQ_CTX2_READY	IRQ_CTX1_READY	IRQ_CTX0_READY	RESERVED							IRQ_OCP_ERR

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27	IRQ_CTX3_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
26	IRQ_CTX2_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
25	IRQ_CTX1_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
24	IRQ_CTX0_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
23:20	RESERVED		R	0x0
19	IRQ_CTX3_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
18	IRQ_CTX2_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
17	IRQ_CTX1_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
16	IRQ_CTX0_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
15:12	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
11	IRQ_CTX3_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
10	IRQ_CTX2_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
9	IRQ_CTX1_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
8	IRQ_CTX0_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
7:1	RESERVED		R	0x00
0	IRQ_OCP_ERR	OCP error received in the master port. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

Table 8-297. Register Call Summary for Register CBUFF_HL_IRQSTATUS

ISS Interfaces

- ISS CBUFF Interrupts: [0] [1] [2] [3]
- ISS CBUFF Functional Description: [4] [5]
- ISS CBUFF Registers: [6]

Table 8-298. CBUFF_HL_IRQENABLE_SET

Address Offset	0x0000 0028		
Physical Address	0x5200 1828	**Instance**	ISS_CBUFF
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				IRQ_CTX3_OVR	IRQ_CTX2_OVR	IRQ_CTX1_OVR	IRQ_CTX0_OVR	RESERVED				IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	RESERVED				IRQ_CTX3_READY	IRQ_CTX2_READY	IRQ_CTX1_READY	IRQ_CTX0_READY	RESERVED							IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27	IRQ_CTX3_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
26	IRQ_CTX2_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
25	IRQ_CTX1_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
24	IRQ_CTX0_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
23:20	RESERVED		R	0x0
19	IRQ_CTX3_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
18	IRQ_CTX2_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
17	IRQ_CTX1_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
16	IRQ_CTX0_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15:12	RESERVED		R	0x0
11	IRQ_CTX3_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
10	IRQ_CTX2_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
9	IRQ_CTX1_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
8	IRQ_CTX0_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
7:1	RESERVED		R	0x00
0	IRQ_OCP_ERR	OCP error received in the master port. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

Table 8-299. Register Call Summary for Register CBUFF_HL_IRQENABLE_SET

ISS Interfaces

- ISS CBUFF Interrupts: [0]
- ISS CBUFF Registers: [1]

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Table 8-300. CBUFF_HL_IRQENABLE_CLR

Address Offset	0x0000 002C		
Physical Address	0x5200 182C	**Instance**	ISS_CBUFF
Description	Per-event interrupt enable bit vector, line 0. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				IRQ_CTX3_OVR	IRQ_CTX2_OVR	IRQ_CTX1_OVR	IRQ_CTX0_OVR	RESERVED				IRQ_CTX3_INVALID	IRQ_CTX2_INVALID	IRQ_CTX1_INVALID	IRQ_CTX0_INVALID	RESERVED				IRQ_CTX3_READY	IRQ_CTX2_READY	IRQ_CTX1_READY	IRQ_CTX0_READY	RESERVED							IRQ_OCP_ERR

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27	IRQ_CTX3_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
26	IRQ_CTX2_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
25	IRQ_CTX1_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
24	IRQ_CTX0_OVR	Buffer overflow event. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
23:20	RESERVED		R	0x0
19	IRQ_CTX3_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
18	IRQ_CTX2_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
17	IRQ_CTX1_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
16	IRQ_CTX0_INVALID	Invalid access. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
15:12	RESERVED		R	0x0
11	IRQ_CTX3_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
10	IRQ_CTX2_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
9	IRQ_CTX1_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
8	IRQ_CTX0_READY	The WB physical window is ready to be accessed by the CPU. Check the functional specification for more details. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
7:1	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
0	IRQ_OCP_ERR	OCP error received in the master port. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

Table 8-301. Register Call Summary for Register CBUFF_HL_IRQENABLE_CLR

ISS Interfaces
- ISS CBUFF Interrupts: [0]
- ISS CBUFF Registers: [1]

Table 8-302. CBUFF_CTX_CTRL_i

Address Offset	0x0000 0100 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 1900 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Context control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				TILERMODE	DONE	WCOUNT		BCF				RESERVED	MODE		ENABLE

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	TILERMODE	Sets the expected value for ADDR[32]. If ADDR[32]=TILERMODE, ADDR[31:4] is processed and eventually translated. Otherwise, the access is handled as transparent, regardless of the other address bits.	RW	0
10	DONE	Write this bit to 1 to indicate the CPU has finished processing its physical buffer. This bit is automatically cleared by hardware, reads always return 0. This bit has no effect when MODE=2 (read/write) Write 0x0: No effect. Write 0x1: The CPU has completely processed the WB physical buffer.	W	0
9:8	WCOUNT	Window count 0x0: 2 windows 0x1: 4 windows 0x3: 16 windows 0x2: 8 windows	RW	0x0
7:4	BCF	This register controls the bandwidth control feedback loop output. 0: Control loop disabled. 1-15: The control feedback loop enabled. Behavior depends on functional mode, see Section 8.2.8.3.2.4, *ISS CBUFF Memory-to-Memory Operation BCF*.	RW	0x0
3	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
2:1	MODE	Selects the functional mode of this context 0x0: Write mode. ISS writes and CPU reads the physical space. CPU accesses are out of the scope of the CBUFF module; therefore, only writes are permitted between CBUFF_CTX_START_i and CBUFF_CTX_END_i. 0x1: Read mode. Hardware reads and CPU writes the physical space. CPU accesses are out of the scope of the CBUFF module; therefore, only reads are permitted between CBUFF_CTX_START_i and CBUFF_CTX_END_i. 0x2: Read/Write mode. Read and writes are monitored by the CBUFF. WB is used to track current read positions WA is used to track current write position.	RW	0x0
0	ENABLE	Enable/disable 0x0: Disables the context. This resets the internal state of the context. All accesses received on OCPI are transmitted to OCPO without modification. Disabling the context takes effect immediately. Software must ensure that no more accesses to the context are outstanding before disabling it. Otherwise memory corruption may occur. 0x1: Enable the context. All accesses between CBUFF_CTX_START_i and CBUFF_CTX_END_i are processed by the CBUFF.	RW	0

Table 8-303. Register Call Summary for Register CBUFF_CTX_CTRL_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- ISS CBUFF Register Setup: [32] [33] [34] [35]
- ISS CBUFF Registers: [36] [37]

Table 8-304. CBUFF_CTX_START_i

Address Offset	0x0000 0104 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 1904 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Start address of the virtual space managed by the context		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Address, in 128-bit words	RW	0x0000000
3:0	RESERVED		R	0x0

Table 8-305. Register Call Summary for Register CBUFF_CTX_START_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1] [2] [3] [4]
- ISS CBUFF Register Setup: [5]
- ISS CBUFF Registers: [6] [7] [8] [9]

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Table 8-306. CBUFF_CTX_END_i

Address Offset	0x0000 0108 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 1908 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	End address of the virtual space managed by the context		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Address, in 128-bit words	RW	0x0000000
3:0	RESERVED		R	0x0

Table 8-307. Register Call Summary for Register CBUFF_CTX_END_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1] [2] [3] [4]
- ISS CBUFF Register Setup: [5]
- ISS CBUFF Registers: [6] [7] [8] [9]

Table 8-308. CBUFF_CTX_WINDOWSIZE_i

Address Offset	0x0000 010C + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 190C + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Defines the size of a window		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZE																				RESERVED			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:4	SIZE	Size, in 128-bit words	RW	0x00000
3:0	RESERVED		R	0x0

Table 8-309. Register Call Summary for Register CBUFF_CTX_WINDOWSIZE_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1] [2] [3] [4]
- ISS CBUFF Register Setup: [5] [6]
- ISS CBUFF Registers: [7]

Table 8-310. CBUFF_CTX_THRESHOLD_F_i

Address Offset	0x0000 0110 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 1910 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Threshold value used to check if a write window is full		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRESHOLD																							

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	THRESHOLD	Threshold value, in bytes	RW	0x000000

Table 8-311. Register Call Summary for Register CBUFF_CTX_THRESHOLD_F_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- ISS CBUFF Register Setup: [11] [12] [13]
- ISS CBUFF Registers: [14]

Table 8-312. CBUFF_CTX_THRESHOLD_S_i

Address Offset	0x0000 0114 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 1914 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Threshold value used to control the BCF synchronization mechanism		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRESHOLD																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	THRESHOLD	Threshold value, in bytes	RW	0x000000

Table 8-313. Register Call Summary for Register CBUFF_CTX_THRESHOLD_S_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- ISS CBUFF Register Setup: [11]
- ISS CBUFF Registers: [12]

Table 8-314. CBUFF_CTX_STATUS_i

Address Offset	0x0000 0118 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 1918 + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				WA				RESERVED				WB			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:8	WA	Valid values depend on the CBUFF_CTX_CTRL_i[9:8] WCOUNT bit field.	R	0x0
7:4	RESERVED		R	0x0
3:0	WB	Valid values depend on the CBUFF_CTX_CTRL_I[9:8] WCOUNT bit field.	R	0x0

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Table 8-315. Register Call Summary for Register CBUFF_CTX_STATUS_i

ISS Interfaces

- ISS CBUFF Interrupts: [0] [1] [2] [3] [4]
- ISS CBUFF Functional Description: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28]
- ISS CBUFF Registers: [29]

Table 8-316. CBUFF_CTX_PHY_i

Address Offset	0x0000 011C + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5200 191C + (0x20 * i)	**Instance**	ISS_CBUFF
Description	Start address of the first physical buffer managed by the context when fragmentation support is disabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Address, in 128 bit words.	RW	0x0000000
3:0	RESERVED		R	0x0

Table 8-317. Register Call Summary for Register CBUFF_CTX_PHY_i

ISS Interfaces

- ISS CBUFF Functional Description: [0] [1]
- ISS CBUFF Register Setup: [2]
- ISS CBUFF Registers: [3]

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8.2.9 ISS BYS

8.2.9.1 ISS BYS Overview

There are two Bayer scaler modules (BYS_A and BYS_B) in the device ISS. Each BYS module enables low-latency still image capture, as well as power and SDRAM bandwidth optimization for video record use cases by scaling the resolution provided by the sensor down to the required video resolution.

The BYS modules enable faster image capture latencies by avoiding sensor mode switches. Some image sensors can continuously output full resolution at viewfinder refresh rate. BYS receives full resolution at viewfinder rate and outputs either full resolution or viewfinder resolution. Either case can be selected with minimal latencies because only ISP internal parameters are changed. Therefore, the time-consuming sensor mode switch is avoided.

The BYS modules also collect statistics that can be used for translational video stabilization in the Bayer domain. Stabilization in the Bayer domain is more efficient from a system point of view (SDRAM bandwidth and power consumption) than stabilization in the YUV domain by performing the stabilization before the ISP processing.

Each BYS module provides the following list of features:

- Functional clock up to 304 MHz
- Interfaces:
  - Configuration interface
  - Input video port:
    - Four pixels wide (up to four pixels per functional clock cycle)
    - Asynchronous from the functional clock
    - HS/VS synchronization signaling
    - 12 bits per pixel
    - Up to 6532 × 8191 pixels for input image size
  - Output video port:
    - One pixel wide (up to one pixel per functional clock cycle)
    - Synchronous to the functional clock
    - HS/VS synchronization signaling
    - 12 bits per pixel
    - Up to 2982 × 1940 pixels for output image size
- Binning artifact correction (pixel shift with subpixel precision to compensate phase errors introduced by sensor binning)
- Down scaler:
  - Horizontal and vertical cropping
  - Defect pixel correction
  - Separable filter
  - Scaling range, down to 1/4x
  - Upscaling not supported
  - Traffic smoothing FIFOs:
    - FIFO between the horizontal and vertical scalers (1500 elements × 12 bits)
    - FIFO between the vertical scaler and the video port/LSC engine (2982 elements × 12 bits)
- Stabilization statistics collection after the down scaler:
  - Piece-wise interpolated gamma correction
  - Polynomial lens shading correction
  - Two independent accumulator engines (ACC0 and ACC1):
    - Configurable bin size, count and offset

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- ACC0: 1968 bins of 23 bits
- ACC1: 3456 bins of 22 bits

8.2.9.2 ISS BYS Environment

There are no particular environment attributes. See Section 8.2.2, *ISS Interfaces Environment*.

8.2.9.3 ISS BYS Integration

Figure 8-107 shows the BYS_A and BYS_B interconnection within the ISS and device. Each BYS module implements a slave port to ISS interconnect. There are no master ports, and the BYS modules cannot send data directly to memory (SDRAM). The BYS modules interface with the MIPI CSI-2 receivers using two separate parallel video ports for data input and data output, capable of supporting up to 4 pixels per functional clock cycle throughput. For exact details about BYS tap in/tap out points within the CSI2 receivers, see Section 8.2.5.3.3.7, *ISS CSI2 Transcoding*. Both BYS modules are integrated the same way and software chooses which camera interface is attached to a given BYS module. The configuration of BYS ports connectivity is made through the ISS_BYS register on ISS top level (see Section 8.1.3, *ISS Register Manual*) as follows:

- ISS_BYS[2:0] BYSA_IN bit field selects which CSI engine output is connected to the BYS_A input video port
- ISS_BYS[6:4] BYSB_IN bit field selects which CSI engine output is connected to the BYS_B input video port
- ISS_BYS[8] CSI2A_IN bit selects which BYS module output is connected to the CSI2_A input BYS video port
- ISS_BYS[10] CSI2B_IN bit selects which BYS module output is connected to the CSI2_B input BYS video port
- ISS_BYS[12] CSI2C_IN bit selects which BYS module output is connected to the CSI2_C input BYS video port

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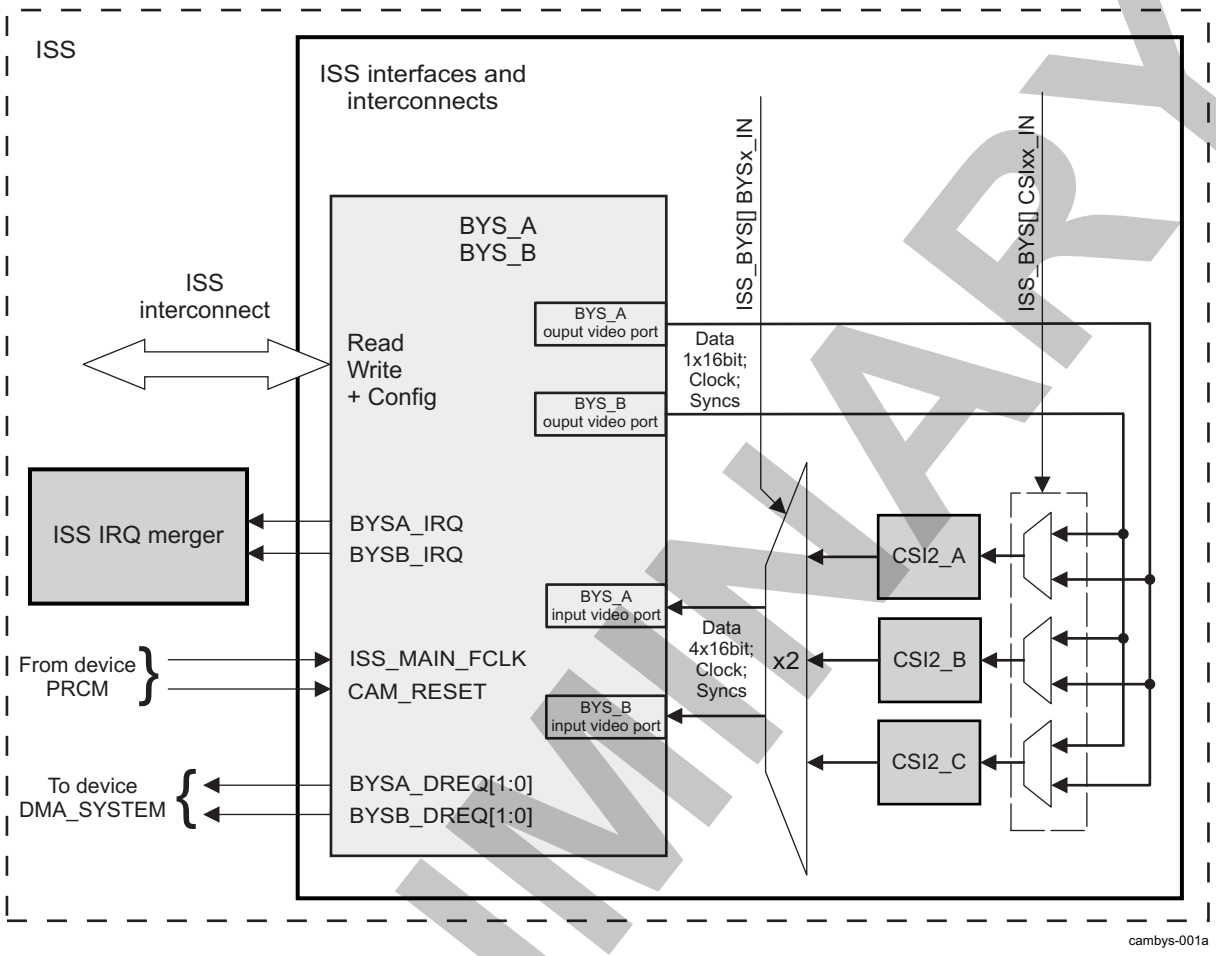
Figure 8-107. ISS BYS Integration



For additional details on power domain, clocks, reset, and hardware requests, see Section 8.1.2, *ISS Functional Description*.

8.2.9.3.1 ISS BYS Interrupt Requests

Each BYS module provides a single interupt request to the ISS top level (BYSA_IRQ and BYSB_IRQ). For more information on BYS interrupt signals mapping on the ISS top level, see Section 8.1.1, *ISS Integration*, and Section 8.1.2.1, *ISS Interrupts*.

8.2.9.3.2 ISS BYS DMA Requests

Each BYS module can generate two DMA request signals to the ISS top level (respectively to device DMA_SYSTEM module), using early deassertion. See also Section 8.1.1, *ISS Integration*, in Section 8.1, *ISS Overview*, for DMA request signals mapping on ISS top level:

- For BYS_A: BYSA_DREQ_0 is mapped to ISS_DREQ_5, and BYSA_DREQ_1 is mapped to ISS_DREQ_6
- For BYS_B: BYSB_DREQ_0 is mapped to ISS_DREQ_7, and BYSA_DREQ_1 is mapped to ISS_DREQ_8

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The selection of one or multiple events (up to four events per DMA request signal) that trigger the DMA request is made by using the BYS_DMAENABLE_SET and BYS_DMAENABLE_CLR registers. The BSC_PAGE[] ACCn bit for the associated Boundary Signal Calculator (BSC) accumulator (n = 0 or 1, BSC accumulator index) is reset when the selected event is triggered. That also asserts the corresponding DMA request signal. Therefore, the first access from DMA_SYSTEM always accesses Page 0, as there is some delay from assertion of a DMA request to the first access. Refer to Section 8.2.9.4.7, *ISS BYS Boundary Signal Calculator*, for more information on BSC functionality.

The DMA request signal is deasserted when the first memory-mapped location of the accumulator is accessed (read or write):

- For BYS_A:
  - BYSA_DREQ_0 is cleared by an access to 0x5200 A000.
  - BYSA_DREQ_1 is cleared by an access to 0x5200 A800.
- For BYS_B:
  - BYSB_DREQ_0 is cleared by an access to 0x5200 E000.
  - BYSB_DREQ_1 is cleared by an access to 0x5200 E800.

The DMA request is reasserted when the last location of the accumulator is accessed:

- For BYS_A:
  - BYSA_DREQ_0 is cleared by an access to 0x5200 A7FC.
  - BYSA_DREQ_1 is cleared by an access to 0x5200 AFFC.
- For BYS_B:
  - BYSB_DREQ_0 is cleared by an access to 0x5200 E7FC.
  - BYSB_DREQ_1 is cleared by an access to 0x5200 EFFC.

, and BSC_PAGE[] ACCn < BSC_DMA_REQS[] ACCn. The value of BSC_PAGE[] ACCn is also incremented by 1 in that case.

This mechanism is used to trigger the DMA requests up to 16x each time one of the selected events occurs (the number of times a DMA request is triggered can be configured in the BSC_DMA_REQS[] ACCn bit field). It allows to completely readout the accumulator without software intervention and using a single DMA channel.

8.2.9.3.3 ISS BYS Reset

An active low asynchronous hardware reset (CAM_RESET) is provided by the PRCM module and propagated from ISS top level.

Software must ensure that there is no active traffic on the slave port and input/output video ports before requesting a hardware reset.

Alternatively, the BYS modules support a software reset, through the BYS_HL_SYSCONFIG[0] SOFTRESET bit.

When a BYS module comes out of reset, it starts accepting data only from a clean frame boundary. The same is expected for the camera interface engines connected to the output video port.

8.2.9.3.4 ISS BYS Clock Domains

Each BYS module has two clock domains:

- Functional clock (ISS_MAIN_FCLK) domain – up to 304 MHz.
- Input video port pixel clock (BYSIN_PCLK) – up to 304 MHz for interconnection with CSI2 engines.
- Output video port pixel clock (BYSOUT_PCLK) - up to 304 MHz.

Both clock domains are asynchronous. Most of the internal logic is in the functional clock domain. Data received on the input video port is resynchronized to the functional clock domain in early stages of the pipeline. The slave port interface to the ISS interconnect runs at half the functional clock (up to 152 MHz).

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8.2.9.3.5 ISS BYS Power Management

No PRCM interface is implemented. Each BYS module implements an efficient autogating, so that the power consumption of unused logic is minimal. By default, the pixel clock on the output video port (BYSOUT_PCLK) is enabled four cycles before the first pixel is sent, active while the pixels are being sent, and disabled 4 pixels after the last pixel has been sent.

The functional clock for each BYS module can be cut by software to reduce power consumption, by switching off the modules from the ISS_CLKCTRL register on ISS top level, through bit [5] BYS_A and bit [7] BYS_B (see Section 8.1.3, *ISS Register Manual*). This should be done only when the BYS modules are not in use.

8.2.9.3.6 ISS BYS Video Ports

Each BYS module has one video port for data input (see Table 8-318) and another video port for data output (see Table 8-319).

Table 8-318. BYS Input Video Port Signals

Signal Name	I/O[1]	Description
BYSIN_PCLK	I	Pixel clock received from the CSI2 engines. Asynchronous from the functional clock
BYSIN_VS	I	Active during the first pixel of the frame
BYSIN_HS	I	Active during the first pixel of any line
BYSIN_DATA[15:0]	I	Input pixel 1 data. MSBs padded with 0s when less than 16 bits are used.
BYSIN_DATA[31:16]	I	Input pixel 2 data. MSBs padded with 0s when less than 16 bits are used.
BYSIN_DATA[47:32]	I	Input pixel 3 data. MSBs padded with 0s when less than 16 bits are used.
BYSIN_DATA[63:48]	I	Input pixel 4 data. MSBs padded with 0s when less than 16 bits are used.

(1) I = Input; O = Output

Table 8-319. BYS Output Video Port Signals

Signal Name	I/O[1]	Description
BYSOUT_PCLK	O	Pixel clock provided to the CSI2 engines. Synchronous to the functional clock. Mean clock rate defined by the BYS_FIFO_BW[31:16] OB bit field.
BYSOUT_VS	O	Active during the first pixel of the frame
BYSOUT_VE	O	Active during the last pixel of the frame
BYSOUT_HS	O	Active during the first pixel of any line
BYSOUT_HE	O	Active during the last pixel of any line
BYSOUT_DATA[15:0]	O	Output pixel 1 data. MSBs padded with 0s when less than 16 bits are used.

(1) I = Input; O = Output

The input video port is asynchronous from the functional clock (ISS_MAIN_FCLK). The output video port is synchronous to the functional clock and the data rate is controlled through software configuration (refer to Section 8.2.9.4.6, *ISS BYS Output Buffer*, for more information)

The input video port is 4 pixels × 16 bits wide and carry 4 or 0 pixels per pixel clock cycle. The output video port is 1 pixel × 16 bits wide and carry 1 or 0 pixels per pixel clock cycle. Pixels are LSB-aligned inside 16-bit containers on the bus. For example, when PIX_DEPTH = 12 bits, the following mapping is implemented for the BYS input video port:

Table 8-320. BYS Input Video Port Transaction

Cycle Number	HS	VS	DATA [11:0]	DATA [15:12]	DATA [27:16]	DATA [31:28]	DATA [43:32]	DATA [47:44]	DATA [59:48]	DATA [63:60]
1	1	1	Pixel 0	0s	Pixel 1	0s	Pixel 2	0s	Pixel 3	0s
2	0	0	Pixel 4	0s	Pixel 5	0s	Pixel 6	0s	Pixel 7	0s
…										

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Table 8-320. BYS Input Video Port Transaction (continued)

Cycle Number	HS	VS	DATA [11:0]	DATA [15:12]	DATA [27:16]	DATA [31:28]	DATA [43:32]	DATA [47:44]	DATA [59:48]	DATA [63:60]
Last pixel of a line (but not last line)	0	0	Last pixel of the line	0s	0s	0s	0s	0s	0s	0s
…										
Last pixel of the frame (example where the width is not a multiple of 4)	0	0	Last pixel of the frame	0s	0s	0s	0s	0s	0s	0s

The output video port pixel clock may be free-running or gated during horizontal and vertical blanking times (control provided in the BYS_CTRL[5] VPORT_FORCEON bit). HS/VS are pulses and the BYS module counts pixels and lines to detect valid image areas.

On both video ports there must be at least four PCLK pulses before the first pixel of a frame (that is, after reset). There must be at least four PCLK cycles of vertical blanking between frames.

The minimum horizontal blanking on the input video port is eight functional clock cycles. It can be artificially created by cropping a few pixels, if the data source connected to this video port does not provide enough blanking.

Software does not need to provide the size of the image received from the camera. It can specify cropping settings. However, software must ensure that the image size received on the input video port is equal to or larger than what the bayer scaler expects:

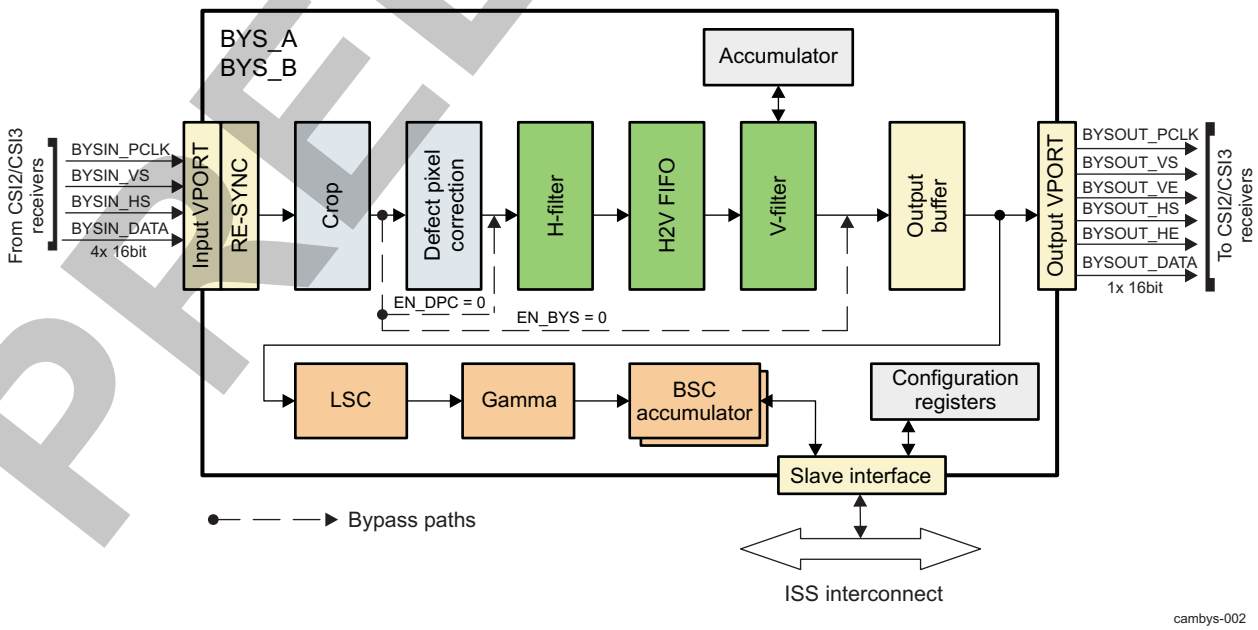
- Input image width >= BSC_SKIP_i[12:0] HSKIP + BSC_CNT_i[12:0] HCNT
- Input image height >= BSC_SKIP_i[28:16] VSKIP + BSC_CNT_i[28:16] VCNT

8.2.9.4 ISS BYS Functional Description

8.2.9.4.1 ISS BYS Block Diagram

Figure 8-108 shows a top-level overview of the BYS modules.

Figure 8-108. BYS Block Diagram



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The following must be considered for the bypass paths from Figure 8-108:

- When BYS_CTRL[4] EN_BYS bit: 0x0
  - The bayer scaler is disabled and the processing logic is bypassed.
  - Cropping of the input image can still be performed.
  - Input and output bandwidth is limited to 1 pixel per functional clock cycle.
  - Data on the output video port is the same as data on the input video port (if no cropping is performed).
- When the BYS_CTRL[1] EN_DPC bit = 0x0:
  - Only the Defect Pixel Correction block is bypassed.
  - The EN_DPC bit is ignored, when the EN_BYS bit is set to 0x0.

8.2.9.4.2 ISS BYS Interrupt Events

All events generated by each BYS module are merged into single events at ISS top level (one event per BYS module, BYSA_IRQ and BYSB_IRQ). Each event at ISS top level can be enabled by the ISS_HL_IRQENABLE_SET_i[18] BYS_A_IRQ and/or [20] BYS_B_IRQ bits. For more information on ISS interrupts, see ISS Interrupts.

Table 8-321 lists the BYS modules interrupt events. Software control over each event is provided through the BYS_HL_IRQENABLE_SET, BYS_HL_IRQENABLE_CLR, and BYS_HL_IRQSTATUS registers.

Table 8-321. BYS Interrupts

Event	Description
VPI_SOF	Start of frame event. Triggered when the first pixel is received on the input video port. Matches the moment where shadow registers are swapped. Refer to Section 8.2.9.4.8, *BYS Registers Shadowing*, for more details on shadowing mechanism.
VPO_EOF	Video port end of frame event. Triggered when the last pixel of a frame has been sent to the output video port.
EOFx (x = 0, 1)	End of frame event of Boundary Signal Calculator (BSC) pipeline "x". Triggered when the last active bin has been updated.
LINE	Line event. Triggered when the input line number before the cropping stage matches the BYS_LINE[12:0] LINE bit field value. The input line number is reset when a VS pulse is received on th input video port and incremented by one on every HS pulse. The event is triggered at the beginning of the line (that is, when the first pixel of the line is received). This feature is typically used to synchronize BYS with other downstream processing. NOTE: LINE and VPI_SOF events will by triggered in the same time when BYS_LINE[12:0] LINE = 0.
OB_OVR	Output buffer overflow event. This event occurs when the chosen buffer readout rate is too low for the incoming pixel rate. The pixels and BSC statistics for the frame are corrupted and must be discarded when this event has occurred. Software must reset the module and configure it properly (this overflow will be systematic failure and occur on every frame, if the configuration is not fixed).
H2V_OVR	Scaler H2V FIFO overflow event. This event occurs when data written by the horizontal filter stage arrives at a higher rate than what the vertical filter stage can process. This error is due to wrong configuration.

8.2.9.4.3 ISS BYS Cropping

The image received from the input video port can be cropped in the X and Y directions before any further processing is done. This technique is typically used when the full field of view is not required and digital zoom is enabled. Figure 8-109 shows an example of image cropping.

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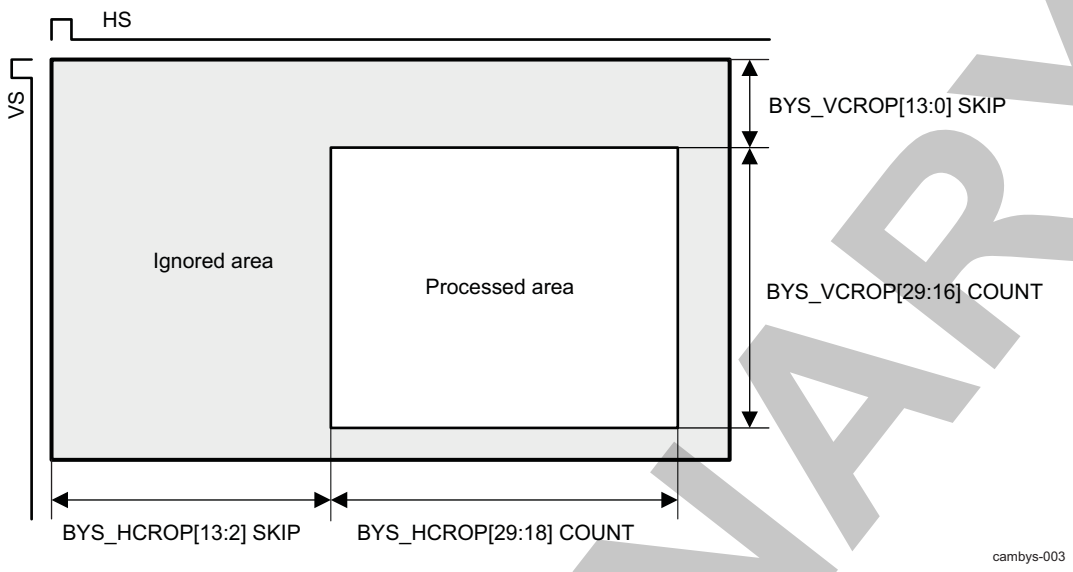
Figure 8-109. BYS Image Cropping



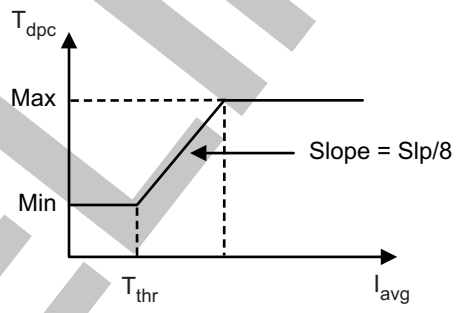
The settings for horizontal cropping are defined in the BYS_HCROP register. The vertical cropping settings are defined in the BYS_VCROP register.

8.2.9.4.4 ISS BYS Defect Pixel Correction

The main purpose of the defect pixel correction (DPC) block is to detect defects and avoid spreading them.

Figure 8-110 shows how the defect pixel threshold is computed.

Figure 8-110. BYS DPC Threshold Computation



I_{avg} = Average (pixels in the neighborhood)
T_{dpc}= Computed threshold to determine defects
Slp = Slope of threshold increase
T_{thr}= Minimum brightness level to begin increasing threshold
Min = Minimum DPC threshold value
Max = Maximum DPC threshold value

The sensitivity of the DPC algorithm is controlled by the BYS_DPCBRT and BYS_DPCTHR registers:

- The Slp parameter is controlled by the BYS_DPCBRT[23:16] SLP bit field.
- The T_{thr} parameter is controlled by the BYS_DPCBRT[11:0] THR bit field.
- The Min parameter is controlled by the BYS_DPCTHR[11:0] MIN bit field.
- The Max parameter is controlled by the BYS_DPCTHR[27:16] MAX bit field.

The DPC block is disabled by default. It can be enabled by setting the BYS_CTRL[1] EN_DPC bit to 0x1.

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8.2.9.4.5 ISS BYS Scaler and H2V FIFO

The scaler consists of two independant horizontal and vertical stages with intermediate H2V FIFO, implemented to smooth the data traffic.

The **horizontal scaler** receives and processes 4 pixels per functional clock cycle. The output pixel rate depends on the input pixel rate and the selected horizontal scaling factor. Faulty pixels do not change the throughput.

The output of the horizontal scaler is stored in the H2V FIFO to smooth the data rate for the vertical scaler.

- Data is written into the FIFO at data production rate and the readout speed from the FIFO is controlled by the BYS_FIFO_BW[15:0] H2V register bit field. Typically, software must choose the lowest possible readout rate. No data is read when the buffer is empty (when the chosen rate is too high or during blanking periods).
- Software must choose such data rate, so that the internal buffer does not overflow. If misconfiguration causes an overflow, a H2V_OVR event occurs (see Section 8.2.9.4.2, *ISS BYS Interrupt Events*).
- The vertical scaler input pixel clock can be calculated as: BYS_FIFO_BW[15:0] H2V × ISS_MAIN_FCLK

The **vertical scaler** can process up to one input pixel per functional clock cycle. The output image of the vertical scaler is first cropped to the size defined by the BYS_OSIZE register, and the data is then sent to the output buffer FIFO.

8.2.9.4.5.1 Scaler Output Image Size Configuration

The output image size, set through the BYS_OSIZE register, must be aligned with other register settings. The BYS_OSIZE register can be used to crop the image after the scaling operation. That is mainly useful when the exact size cannot be chosen through the input size and scaling factor, or if odd and even lines do not have the same size because of different initial phases (refer to Section 8.2.9.4.5.2, *Scaler Phase Initialization Tables*, for more details).

BYS_OSIZE[] xSIZE <=
floor((BYS_xINIT[13:0] INI0 + (BYS_xCROP[] COUNT / 2 - 1) × BYS_SCALE[] xSCALE) / 8192, 1) +
floor((BYS_xINIT[29:16] INI1 + (BYS_xCROP[] COUNT / 2 - 1) × BYS_SCALE[] xSCALE) / 8192, 1)
where x = H or V.

8.2.9.4.5.2 Scaler Phase Initialization Tables

Software must choose properly the initial horizontal phase (through the BYS_HINIT register) and initial vertical phase (through the BYS_VINIT register), to get a correct image. The following constraint applies for correct operation:

BYS_HINIT[13:0] INI0 >= BYS_HINIT[29:16] INI1

The following formulas and tables explain how to set the BYS_HINIT and BYS_VINIT registers for a given scaling factor. Phase initialization parameters are different for normal mode (in Table 8-322 and Table 8-323) and 2x2 binning mode (in Table 8-324 and Table 8-325). The table indexes (ih, iv) start from 1.

ih = round((8192/BYS_SCALE[13:0] HSCALE)*256 - 256 + 1)

iv = round((8192/BYS_SCALE[29:16] VSCALE)*256 - 256 + 1)

The initial horizontal (HINIT) and vertical (VINIT) phases for normal mode (no binning) can be calculated as follows:

- For even line: BYS_HINIT[13:0] INI0 = Table 8-322 (ih)
- For even line: BYS_VINIT[13:0] INI0 = Table 8-322 (iv)
- For odd line: BYS_HINIT[29:16] INI1 = Table 8-323 (ih)
- For odd line: BYS_VINIT[29:16] INI1 = Table 8-323 (iv)

The initial horizontal (HINIT) and vertical (VINIT) phases for 2x2 binning mode can be calculated as follows:

- For even line: BYS_HINIT[13:0] INI0 = Table 8-324 (ih)

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- For even line: BYS_VINIT[13:0] INI0 = Table 8-324 (iv)
- For odd line: BYS_HINIT[29:16] INI1 = Table 8-325 (ih)
- For odd line: BYS_VINIT[29:16] INI1 = Table 8-325 (iv)

Table 8-322. Even Line Initial Phases for Normal Mode (no Binning)

8192	8066	7919	7794	7668	8357	8232	8107	7982	7857	7732	7607	7482	8173	8048	7945
7821	7708	7592	7469	7366	7242	7954	7830	7727	7625	7522	7398	7296	7193	7091	6989
7701	7599	7497	7395	7293	7191	7090	6988	6886	6806	7518	7418	7336	7236	7133	7052
6951	6870	6770	6691	6588	6507	7243	7141	7060	6983	6899	6812	6720	6639	6560	6481
6405	6319	7036	6955	6875	6814	6736	6655	6577	6497	6418	6337	6258	6199	6120	6855
6776	6716	6637	6557	6498	6419	6360	6281	6222	6143	6065	6006	5946	6683	6625	6545
6471	6427	6349	6290	6232	6153	6095	6035	5977	5898	5840	5781	5723	6480	6422	6343
6285	6227	6168	6109	6051	5993	5935	5877	5818	5760	5703	5644	5588	5548	6302	6243
6279	6131	6073	6033	5976	5917	5850	5821	5762	5705	5647	5610	5551	5494	5455	5397
6155	6117	6060	6021	5964	5926	5869	5829	5772	5715	5676	5638	5581	5543	5486	5447
5390	5352	5314	5257	5219	5977	5939	5901	5844	5805	5767	5711	5673	5635	5597	5537
5502	5464	5426	5371	5331	5294	5255	5218	5180	5123	5086	5863	5826	5788	5750	5712
5676	5617	5580	5542	5505	5467	5429	5391	5354	5317	5280	5242	5203	5167	5128	5092
5054	5017	4998	4961	4923	5700	5663	5626	5588	5550	5513	5494	5457	5420	5382	5345
5308	5289	5252	5214	5177	5140	5122	5084	5047	5010	4991	4954	4917	4880	4861	4824
4787	5583	5546	5510	5490	5453	5416	5397	5361	5323	5305	5268	5231	5212	5175	5157
5120	5083	5065	5028	5009	4972	4954	4917	4880	4862	4825	4806	4770	4751	4714	4696
4659	5455	5418	5400	5363	5345	5308	5290	5253	5235	5216	5179	5161	5124	5106	5069
5052	5033	4996	4978	4941	4923	4904	4868	4850	4831	4795	4777	4740	4722	4703	4667
4649	4631	4594	4575	4557	5335	5317	5299	5280	5244	5226	5208	5171	5153	5135	5116
5081	5062	5044	5026	4990	4971	4953	4935	4898	4880	4862	4844	4826	4789	4771	4753
4735	4717	4681	4663	4645	4627	4606	4571	4553	4535	4518	4499	4481	4463	4426	5223
5205	5187	5169	5151	5133	5115	5079	5061	5043	5025	5006	4989	4971	4952	4934	4916
4898	4862	4844	4826	4808	4790	4771	4754	4736	4718	4700	4682	4664	4646	4628	4609
4588	4575	4557	4538	4520	4503	4484	4466	4448	4430	4413	4395	4376	4359	4341	4323
5119	5101	5084	5065	5048	5030	5012	4994	4976	4958	4940	4922	4904	4904	4886	4869
4851	4833	4815	4797	4779	4761	4743	4726	4708	4690	4690	4670	4654	4636	4619	4601
4583	4565	4547	4547	4529	4512	4494	4476	4458	4440	4440	4422	4404	4387	4369	4351
4333	4333	4315	4298	4280	4262	4245	4245	4227	5023	5006	4988	4988	4970	4952	4935
4917	4899	4899	4881	4863	4846	4828	4828	4810	4793	4775	4775	4757	4739	4722	4704
4704	4686	4669	4651	4651	4633	4615	4598	4598	4579	4562	4545	4545	4527	4509	4492
4492	4474	4456	4439	4439	4421	4403	4386	4386	4368	4350	4350	4333	4315	4297	4297
4280	4262	4262	4244	4227	4209	4209	4191	4174	4174	4156	4138	4138	4936	4918	4918
4900	4883	4883	4865	4847	4847	4830	4812	4812	4795	4777	4777	4759	4742	4742	4724
4707	4707	4689	4671	4671	4654	4636	4636	4619	4601	4601	4584	4584	4566	4548	4548
4531	4513	4513	4494	4494	4478	4461	4461	4443	4426	4426	4408	4408	4391	4373	4373
4355	4355	4338	4321	4321	4303	4303	4286	4268	4268	4251	4251	4233	4216	4216	4199
4199	4181	4181	4164	4146	4146	4128	4128	4111	4111	4094	4076	4076	4059	4059	4855
4855	4838	4820	4820	4803	4803	4785	4785	4768	4768	4751	4733	4733	4716	4716	4698
4698	4681	4681	4664	4664	4646	4646	4629	4611	4611	4594	4594	4577	4577	4559	4559
4541	4541	4524	4524	4507	4507	4489	4489	4472	4472	4455	4455	4437	4437	4421	4421
4403	4403	4385	4385	4368	4368	4351	4351	4333	4333	4316	4316	4298	4298	4281	4281
4264	4264	4246	4246	4229	4229	4212	4212	4194	4194	4178	4178	4160	4160	4160	4142
4142	4125	4125	4108	4108	4091	4091	4073	4073	4056	4056	4039	4039	4039	4021	4021

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Table 8-322. Even Line Initial Phases for Normal Mode (no Binning) (continued)

4004	4004	3987	3987	4783	4783	4766	4766	4766	4749	4749	4732	4732	4714	4714	4714
4697	4697	4680	4680	4662	4662	4645	4645	4645	4628	4628	4610	4610	4593	4593	4593
4576	4576	4559	4559	4541	4541	4541	4524	4524	4507	4507	4507	4490	4490	4473	4473
4455	4455	4455	4438	4438	4421	4421	4421	4404	4404	4386	4386	4386	4369	4369	4352
4352															

Table 8-323. Odd Line Initial Phases for Normal Mode (no Binning)

8192	8051	7887	7746	7605	8280	8139	7999	7859	7719	7579	7438	7299	7974	7835	7719
7578	7439	7324	7185	7069	6930	7630	7491	7376	7261	7145	7006	6892	6776	6662	6547
7249	7132	7018	6902	6789	6674	6559	6445	6331	6240	6941	6827	6735	6623	6507	6418
6304	6213	6100	6008	5896	5805	6529	6416	6325	6238	6144	6017	5942	5851	5761	5671
5578	5492	6194	6103	6014	5947	5855	5766	5678	5589	5497	5409	5320	5253	5162	5888
5800	5733	5643	5555	5487	5399	5332	5243	5176	5087	4998	4931	4866	5590	5524	5436
5377	5302	5216	5149	5083	4994	4928	4861	4795	4707	4641	4575	4508	5258	5191	5103
5038	4972	4905	4840	4774	4708	4642	4577	4511	4445	4379	4314	4249	4204	4955	4890
4777	4756	4691	4649	4582	4518	4455	4408	4344	4277	4213	4170	4104	4039	3995	3931
4679	4636	4573	4528	4463	4420	4354	4312	4247	4182	4138	4095	4030	3987	3923	3879
3814	3772	3728	3663	3621	4371	4328	4285	4220	4177	4134	4070	4027	3984	3941	3883
3834	3790	3747	3682	3640	3597	3555	3510	3469	3405	3362	4134	4091	4049	4006	3963
3918	3857	3814	3771	3728	3686	3643	3613	3557	3515	3472	3430	3387	3345	3301	3259
3217	3174	3153	3111	3068	3841	3798	3756	3714	3671	3629	3608	3566	3523	3480	3438
3396	3374	3336	3290	3247	3205	3184	3142	3099	3057	3036	2994	2952	2909	2888	2846
2804	3598	3556	3514	3493	3451	3409	3388	3345	3303	3282	3240	3198	3177	3135	3114
3072	3030	3009	2967	2946	2904	2883	2841	2799	2778	2736	2715	2673	2652	2610	2589
2548	3342	3300	3280	3238	3217	3175	3154	3112	3091	3070	3029	3008	2966	2945	2903
2878	2862	2823	2799	2758	2736	2715	2674	2653	2632	2591	2569	2528	2507	2487	2445
2423	2403	2362	2341	2320	3094	3074	3053	3032	2990	2970	2949	2907	2887	2865	2845
2803	2783	2762	2741	2700	2679	2658	2638	2596	2585	2555	2534	2514	2472	2452	2431
2411	2390	2349	2328	2308	2288	2264	2224	2204	2183	2163	2142	2122	2101	2060	2854
2834	2813	2792	2772	2751	2730	2688	2668	2648	2627	2607	2586	2566	2545	2524	2504
2484	2442	2422	2402	2381	2361	2344	2319	2299	2278	2258	2237	2217	2196	2176	2156
2136	2114	2094	2073	2053	2032	2012	1991	1971	1951	1930	1910	1890	1869	1849	1828
2622	2602	2581	2561	2540	2520	2500	2479	2459	2438	2418	2398	2377	2377	2357	2336
2316	2296	2275	2254	2234	2214	2194	2173	2153	2132	2132	2126	2092	2071	2051	2031
2010	1990	1970	1970	1949	1929	1908	1888	1868	1847	1847	1827	1806	1786	1766	1745
1726	1726	1705	1685	1664	1644	1624	1624	1603	2399	2378	2358	2358	2339	2318	2297
2277	2257	2257	2236	2216	2196	2176	2176	2155	2135	2115	2115	2094	2074	2054	2034
2034	2013	1993	1973	1973	1953	1933	1912	1912	1892	1872	1852	1852	1831	1811	1791
1791	1771	1751	1730	1730	1710	1690	1670	1670	1649	1629	1629	1609	1589	1569	1569
1549	1528	1528	1508	1488	1468	1468	1448	1428	1428	1407	1387	1387	2183	2163	2163
2143	2122	2122	2102	2082	2082	2062	2042	2042	2022	2002	2002	1981	1961	1961	1941
1921	1921	1901	1881	1881	1861	1841	1841	1821	1800	1800	1780	1780	1760	1740	1740
1720	1700	1700	1682	1682	1660	1640	1640	1620	1600	1600	1580	1580	1560	1539	1539
1520	1520	1499	1479	1479	1459	1459	1439	1419	1419	1399	1399	1379	1359	1359	1339
1339	1319	1319	1299	1279	1279	1259	1259	1240	1240	1219	1199	1199	1180	1180	1975
1975	1955	1935	1935	1915	1915	1894	1894	1875	1875	1855	1835	1835	1815	1815	1795

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Table 8-323. Odd Line Initial Phases for Normal Mode (no Binning) (continued)

1795	1775	1775	1755	1755	1735	1735	1715	1695	1695	1675	1675	1655	1655	1635	1635
1616	1616	1595	1595	1576	1576	1556	1556	1536	1536	1516	1516	1496	1496	1475	1475
1456	1456	1436	1436	1417	1417	1397	1397	1377	1377	1357	1357	1337	1337	1317	1317
1297	1297	1277	1277	1257	1257	1237	1237	1217	1217	1199	1199	1178	1178	1178	1158
1158	1138	1138	1117	1117	1098	1098	1078	1078	1059	1059	1039	1039	1039	1019	1019
999	999	979	979	1775	1775	1755	1755	1755	1735	1735	1716	1716	1696	1696	1696
1676	1676	1656	1656	1636	1636	1616	1616	1616	1597	1597	1577	1577	1557	1557	1557
1537	1537	1517	1517	1498	1498	1498	1478	1478	1458	1458	1458	1438	1438	1418	1418
1399	1399	1399	1379	1379	1359	1359	1359	1339	1339	1320	1320	1320	1300	1300	1280
1280															

Table 8-324. Even Line Initial Phases for 2x2 Binning Mode

9216	9146	9075	9005	9318	9248	9178	9108	9037	8967	8897	8828	8757	9116	9046	8976
8909	8843	8767	8720	8650	8580	8918	8872	8800	8731	8684	8615	8566	8499	8430	8382
8721	8673	8597	8556	8487	8441	8395	8326	8280	8210	8569	8528	8455	8407	8362	8293
8246	8201	8156	8110	8040	7994	8354	8307	8262	8193	8149	8085	8057	8011	7962	7917
7859	7827	8192	8140	8095	8049	8003	7958	7912	7864	7820	7775	7727	7682	7635	8025
7975	7929	7885	7838	7791	7769	7724	7677	7635	7585	7562	7519	7475	7856	7809	7765
7720	7696	7650	7603	7583	7537	7514	7468	7423	7399	7354	7310	7286	7646	7629	7580
7557	7512	7494	7442	7421	7377	7352	7306	7285	7240	7217	7170	7146	7511	7489	7444
7373	7395	7351	7328	7284	7260	7238	7193	7169	7147	7102	7080	7051	7013	6991	6966
7329	7306	7283	7239	7216	7193	7171	7124	7103	7080	7023	7013	6990	6967	6945	6901
6875	6855	6833	6809	7171	7149	7129	7105	7082	7058	7012	6993	6970	6946	6924	6902
6879	6835	6814	6798	6767	6744	6722	6700	6677	6654	6629	6610	6973	6949	6928	6906
6881	6859	6837	6815	6793	6770	6748	6735	6703	6681	6655	6636	6613	6590	6569	6547
6524	6502	6479	6457	6841	6818	6797	6797	6772	6753	6730	6708	6685	6663	6640	6618
6596	6574	6551	6528	6528	6506	6484	6462	6439	6418	6395	6373	6373	6350	6328	6306
6284	6669	6646	6646	6624	6602	6579	6557	6535	6535	6513	6490	6468	6446	6446	6424
6401	6379	6357	6357	6335	6312	6290	6268	6268	6246	6223	6201	6201	6179	6157	6135
6135	6520	6498	6475	6475	6453	6431	6409	6409	6386	6364	6364	6342	6320	6298	6298
6272	6254	6254	6231	6209	6209	6187	6165	6143	6143	6120	6099	6099	6076	6054	6054
6030	6010	6010	5989	5964	5964	6351	6329	6329	6307	6284	6284	6262	6262	6240	6219
6219	6196	6174	6174	6153	6153	6129	6107	6107	6078	6063	6063	6041	6041	6019	5997
5997	5975	5975	5953	5932	5932	5908	5908	5886	5886	5864	5843	5843	5820	5820	6206
6206	6186	6162	6162	6140	6140	6110	6110	6095	6095	6073	6051	6051	6032	6032	6007
6007	5986	5986	5963	5963	5941	5941	5920	5920	5897	5875	5875	5853	5853	5831	5831
5809	5809	5787	5787	5765	5765	5743	5743	5722	5722	5700	5700	5677	5677	5656	5656
6041	6041	6018	6018	6018	5997	5997	5975	5975	5951	5951	5931	5931	5909	5909	5887
5887	5865	5865	5843	5843	5843	5821	5821	5799	5799	5773	5773	5755	5755	5755	5733
5733	5712	5712	5689	5689	5668	5668	5668	5646	5646	5624	5624	5602	5602	5602	5579
5579	5558	5558	5536	5536	5536	5514	5514	5900	5900	5900	5878	5878	5856	5856	5856
5834	5834	5812	5812	5812	5788	5788	5768	5768	5768	5746	5746	5724	5724	5724	5703
5703	5681	5681	5681	5659	5659	5659	5637	5637	5615	5615	5615	5593	5593	5593	5572
5572	5550	5550	5550	5528	5528	5528	5506	5506	5506	5484	5484	5463	5463	5463	5442
5442	5442	5420	5420	5420	5398	5398	5398	5377	5377	5377	5355	5355	5739	5739	5739
5717	5717	5717	5695	5695	5695	5673	5673	5673	5651	5651	5651	5630	5630	5630	5608

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Table 8-324. Even Line Initial Phases for 2x2 Binning Mode (continued)

5608	5608	5586	5586	5586	5566	5566	5566	5566	5544	5544	5544	5522	5522	5522	5501
5501	5501	5477	5477	5477	5457	5457	5457	5457	5435	5435	5435	5413	5413	5413	5392
5392	5392	5370	5370	5370	5370	5348	5348	5348	5326	5326	5326	5326	5305	5305	5305
5283	5283	5283	5261	5261	5261	5261	5239	5239	5239	5218	5218	5218	5218	5603	5603
5603	5581	5581	5581	5581	5560	5560	5560	5560	5538	5538	5538	5516	5516	5516	5516
5494	5494	5494	5494	5473	5473	5473	5473	5451	5451	5451	5429	5429	5429	5429	5407
5407	5407	5407	5386	5386	5386	5386	5364	5364	5364	5364	5343	5343	5343	5343	5321
5321	5321	5321	5300	5300	5300	5300	5277	5277	5277	5277	5256	5256	5256	5256	5234
5234	5234	5234	5212	5212	5212	5212	5191	5191	5191	5191	5169	5169	5169	5169	5169
5147	5147	5147	5147	5126	5126	5126	5126	5104	5104	5104	5104	5104	5082	5082	5082
5082	5061	5061	5061	5061	5446	5446	5446	5446	5446	5424	5424	5424	5424	5403	5403
5403	5403	5403	5381	5381	5381	5381	5381	5359	5359	5359	5359	5338	5338	5338	5338
5338	5316	5316	5316	5316	5316	5295	5295	5295	5295	5273	5273	5273	5273	5273	5251
5251	5251	5251	5251	5230	5230	5230	5230	5230	5208	5208	5208	5208	5208	5187	5187
5187															

Table 8-325. Odd Line Initial Phases for 2x2 Binning Mode

7168	7090	7012	6934	7237	7159	7082	7003	6926	6848	6770	6693	6615	6971	6893	6816
6728	6673	6582	6530	6452	6375	6704	6654	6577	6499	6447	6370	6316	6244	6166	6112
6441	6390	6306	6261	6184	6132	6082	6006	5954	5877	6232	6184	6104	6050	6000	5925
5873	5823	5774	5726	5642	5591	5949	5894	5845	5768	5719	5690	5615	5567	5514	5464
5415	5361	5716	5666	5615	5563	5515	5462	5411	5360	5308	5259	5207	5157	5106	5487
5437	5386	5334	5285	5234	5209	5158	5107	5057	5005	4981	4930	4879	5260	5210	5159
5108	5083	5032	4986	4956	4907	4882	4830	4779	4754	4704	4653	4629	4985	4957	4908
4884	4834	4809	4758	4732	4686	4656	4606	4581	4531	4506	4454	4427	4788	4763	4714
4641	4659	4612	4584	4535	4511	4483	4436	4409	4384	4335	4309	4292	4234	4208	4184
4540	4515	4491	4440	4415	4390	4364	4314	4290	4265	4271	4189	4163	4139	4116	4064
4041	4014	3989	3963	4320	4295	4272	4245	4221	4196	4146	4121	4096	4071	4046	4022
3995	3946	3921	3905	3871	3846	3821	3785	3773	3747	3723	3697	4053	4028	4003	3978
3955	3929	3904	3879	3854	3830	3805	3783	3755	3730	3704	3680	3655	3629	3606	3580
3555	3530	3506	3481	3863	3837	3813	3813	3789	3762	3739	3714	3689	3664	3640	3615
3590	3565	3540	3517	3517	3490	3466	3441	3416	3391	3366	3342	3342	3317	3292	3268
3242	3625	3600	3600	3575	3550	3526	3501	3476	3476	3451	3427	3402	3377	3377	3352
3328	3303	3278	3278	3253	3229	3204	3179	3179	3154	3130	3105	3105	3081	3056	3031
3031	3413	3389	3364	3364	3339	3314	3289	3289	3264	3240	3240	3216	3191	3166	3166
3142	3117	3117	3092	3068	3068	3043	3018	2993	2993	2969	2944	2944	2919	2894	2894
2871	2846	2846	2821	2796	2796	3179	3154	3154	3129	3105	3105	3080	3080	3054	3030
3030	3006	2981	2981	2958	2958	2931	2908	2908	2881	2858	2858	2834	2834	2809	2785
2785	2760	2760	2736	2712	2712	2686	2686	2662	2662	2639	2613	2613	2588	2588	2971
2971	2945	2922	2922	2897	2897	2873	2873	2848	2848	2824	2799	2799	2773	2773	2749
2749	2725	2725	2701	2701	2677	2677	2652	2652	2628	2603	2603	2579	2579	2554	2554
2530	2530	2505	2505	2481	2481	2456	2456	2432	2432	2407	2407	2383	2383	2358	2358
2741	2741	2716	2716	2716	2691	2691	2667	2667	2643	2643	2618	2618	2595	2595	2569
2569	2545	2545	2521	2521	2521	2496	2496	2472	2472	2451	2451	2423	2423	2423	2399
2399	2374	2374	2350	2350	2325	2325	2325	2301	2301	2277	2277	2252	2252	2252	2228
2228	2203	2203	2179	2179	2179	2154	2154	2537	2537	2537	2513	2513	2489	2489	2489

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Table 8-325. Odd Line Initial Phases for 2x2 Binning Mode (continued)

2464	2464	2440	2440	2440	2413	2413	2391	2391	2391	2366	2366	2342	2342	2342	2318
2318	2294	2294	2294	2269	2269	2269	2245	2245	2220	2220	2220	2196	2196	2196	2172
2172	2147	2147	2147	2123	2123	2123	2099	2099	2099	2074	2074	2050	2050	2050	2026
2026	2026	2001	2001	2001	1977	1977	1977	1953	1953	1953	1928	1928	2311	2311	2311
2287	2287	2287	2262	2262	2262	2238	2238	2238	2214	2214	2214	2190	2190	2190	2165
2165	2165	2141	2141	2141	2117	2117	2117	2117	2092	2092	2092	2068	2068	2068	2043
2043	2043	2016	2016	2016	1995	1995	1995	1995	1971	1971	1971	1946	1946	1946	1921
1921	1921	1898	1898	1898	1898	1874	1874	1874	1850	1850	1850	1850	1826	1826	1826
1801	1801	1801	1777	1777	1777	1777	1753	1753	1753	1728	1728	1728	1728	2111	2111
2111	2087	2087	2087	2087	2062	2062	2062	2062	2038	2038	2038	2014	2014	2014	2014
1990	1990	1990	1990	1966	1966	1966	1966	1942	1942	1942	1917	1917	1917	1917	1893
1893	1893	1893	1869	1869	1869	1869	1845	1845	1845	1845	1820	1820	1820	1820	1796
1796	1796	1796	1772	1772	1772	1772	1748	1748	1748	1748	1724	1724	1724	1724	1700
1700	1700	1700	1676	1676	1676	1676	1651	1651	1651	1651	1627	1627	1627	1627	1627
1603	1603	1603	1603	1579	1579	1579	1579	1555	1555	1555	1555	1555	1531	1531	1531
1531	1506	1506	1506	1506	1889	1889	1889	1889	1889	1865	1865	1865	1865	1841	1841
1841	1841	1841	1817	1817	1817	1817	1817	1793	1793	1793	1793	1768	1768	1768	1768
1768	1744	1744	1744	1744	1744	1720	1720	1720	1720	1696	1696	1696	1696	1696	1672
1672	1672	1672	1672	1648	1648	1648	1648	1648	1624	1624	1624	1624	1624	1600	1600
1600															

8.2.9.4.6 ISS BYS Output Buffer

The scaler filter typically generates heavy burst traffic and output FIFO is implemented to smooth this traffic.

Data is written into the output FIFO at data production rate and the readout speed from the FIFO is controlled by the BYS_FIFO_BW[31:16] OB bit field. Software must choose the lowest possible readout rate. No data is read when the buffer is empty (when the chosen rate is too high or during blanking periods).

Software must choose such data rate, so that the internal buffer does not overflow. If misconfiguration causes an overflow, an OB_OVR event occurs (see Section 8.2.9.4.2, *ISS BYS Interrupt Events*).

- The output video port pixel clock (BYSOUT_PCLK) can be calculated as: BYS_FIFO_BW[31:16] OB × ISS_MAIN_FCLK

8.2.9.4.7 ISS BYS Boundary Signal Calculator

8.2.9.4.7.1 BSC Polynomial Radial Lens Shading Compensation

In camera applications, optical elements often leave an artifact that reduces image intensity as pixels are farther from the center of the image. Stabilization quality is reduced when the corners of image are too dark. The lens shading compensation (LSC) feature solves this problem.

NOTE: LSC does not impact pixel data sent to the output video port.

The shading gain calculation is performed in the LSC_CORE submodule. Figure 8-111, *BYS LSC_CORE Algorithm*, shows approximate calculation details. Only one instance of the shading gain is computed per pixel received from the output buffer and sent to the gamma correction engine. The LSC algorithm is not applied to pixels sent to the output video port.

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NOTE: Figure 8-111 and Figure 8-112 show the computation precision using the [SU]n.m notation for pixel depth of 12 bits, where:

- [SU]: Either S for a signed number or U for an unsigned number
- N: Number of integer bits
- M: Number of fractional bits

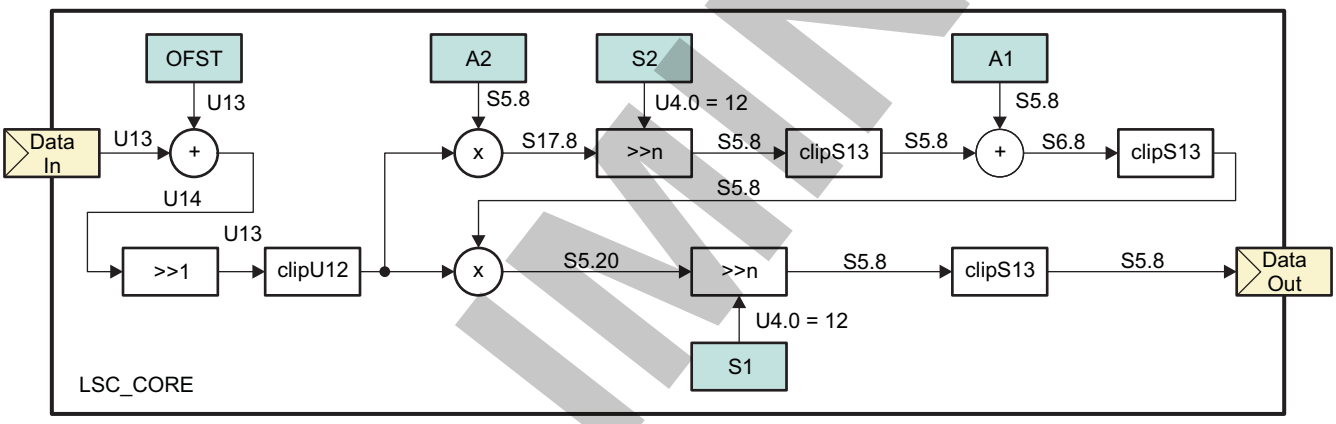
Some arithmetic notation examples are provided in the following table:

Notation	Signed?	Int/frac	Coding	Min	Max	Step
U16.0	Unsigned	Integer	16	0	65535	1
S16.0	Signed	Integer	16	–32768	32767	1
U10.5	Unsigned	Fractional	15	0	1023.96875	0.03125
U13.4	Unsigned	Fractional	17	0	8191.9375	0.0625
S13.4	Signed	Fractional	17	65536	4095.9375	0.0625

cambys-005

The position of the fractional point is configurable at some processing stages using the S0, S1, and S2 parameters. The position of the fractional point provided in Figure 8-111 is an example corresponding to the shown values of the Sx parameters.

Figure 8-111. BYS LSC_CORE Algorithm



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The LSC_CORE is instantiated two times. One LSC_CORE instance is operating on the horizontal position and the other one is operating on the vertical position. The pixel position ranges from 0…8191 (i.e. U13). The algorithm details and precision requirements shown on Figure 8-112, *BYS LSC Algorithm*, below, are informative.

The LSC algorithm receives the pixel position and as well the pixel value from the output buffer. It executes the LSC_CORE algorithm on the horizontal and vertical coordinates. The results are combined together to compute a gain for each pixel received from the output buffer. The pixel is then multiplied by the gain and forwarded to the gamma correction stage.

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Figure 8-112. BYS LSC Algorithm

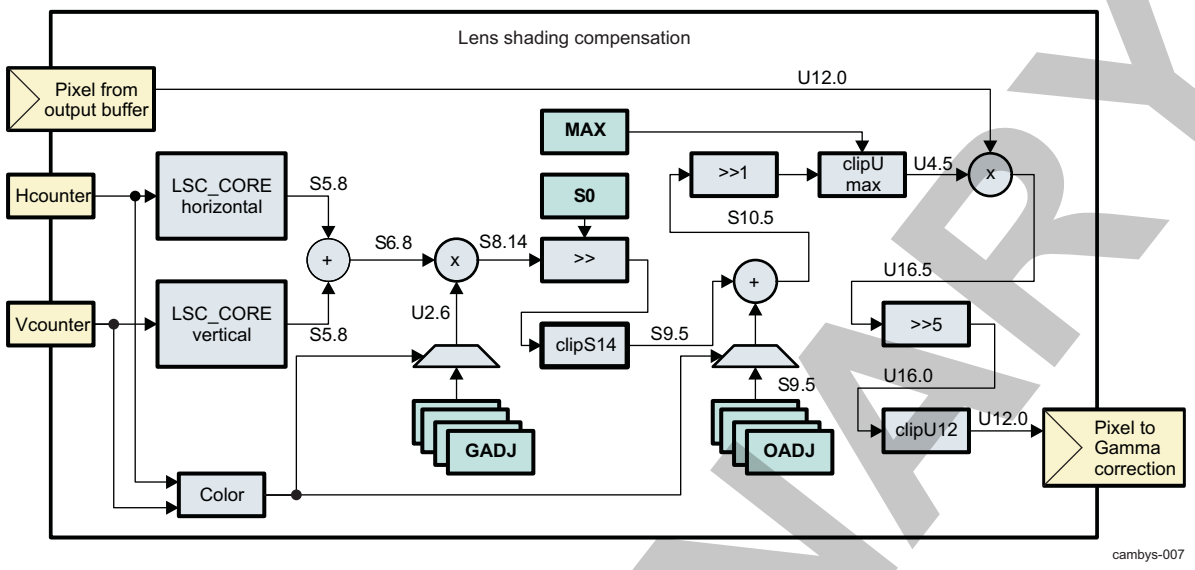

Table 8-326 lists the mapping of BYS module registers to the parameters used in Figure 8-111 and Figure 8-112.

Table 8-326. LSC Parameters Summary

Parameter	Description	Precision	Horizontal	Vertical
OFST	Initial X (horizontal) and Y (vertical) coordinates	U13	BSC_LSC_OFT[12:0] HOFST	BSC_LSC_OFT[28:16] VOFST
A2	X2 term coefficient, fixed point integer	S13	BSC_LSC_A2[12:0] HA2	BSC_LSC_A2[28:16] VA2
S2	X2 term coefficient, radix point position	U4	BSC_LSC_S[7:4] HS2	BSC_LSC_S[23:20] VS2
A1	X term coefficient, fixed point integer	S13	BSC_LSC_A1[12:0] HA1	BSC_LSC_A1[28:16] VA1
S1	X term coefficient, radix point position	U4	BSC_LSC_S[3:0] HS1	BSC_LSC_S[19:16] VS1
GADJ	Gain adjust	U8	BSC_LSC_GAN_0X[7:0] GAN_00 BSC_LSC_GAN_0X[23:16] GAN_01 BSC_LSC_GAN_1X[7:0] GAN_10 BSC_LSC_GAN_1X[23:16] GAN_11	
S0	Gain adjust, radix point position	U4	BSC_LSC_SHF[3:0] VAL	
OADJ	Offset adjust	S14 Valid range = (-4096 to +4095)	BSC_LSC_OFT_0X[13:0] OFT_00 BSC_LSC_OFT_0X[29:16] OFT_01 BSC_LSC_OFT_1X[13:0] OFT_10 BSC_LSC_OFT_1X[29:16] OFT_11	
MAX	Maximum gain	U9	BSC_LSC_MAX[8:0] VAL	

The software can configure different GADJ and OADJ parameters for each of the four color planes (Gb, B, Gr, and R). During LSC algorithm execution, the BSC selects the appropriate bit field for the GADJ and OADJ parameters to be used, based on the position of the pixel after the cropping and scaling operation. The following equations are used:

- GADJ(algorithm parameter) = GADJ(register setting)[Vcounter][Hcounter]
- OADJ(algorithm parameter) = OADJ(register setting)[Vcounter][Hcounter],

where Hcounter and Vcounter indicate the position of the pixel after the cropping and scaling operations (the top-left corner position is (0,0)).

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By default, the LSC module is disabled (bypassed). Software must set the BSC_GLOBAL_CTRL[0] EN_LSC register bit to 0x1 to enable it.

8.2.9.4.7.2 BSC Gamma Correction

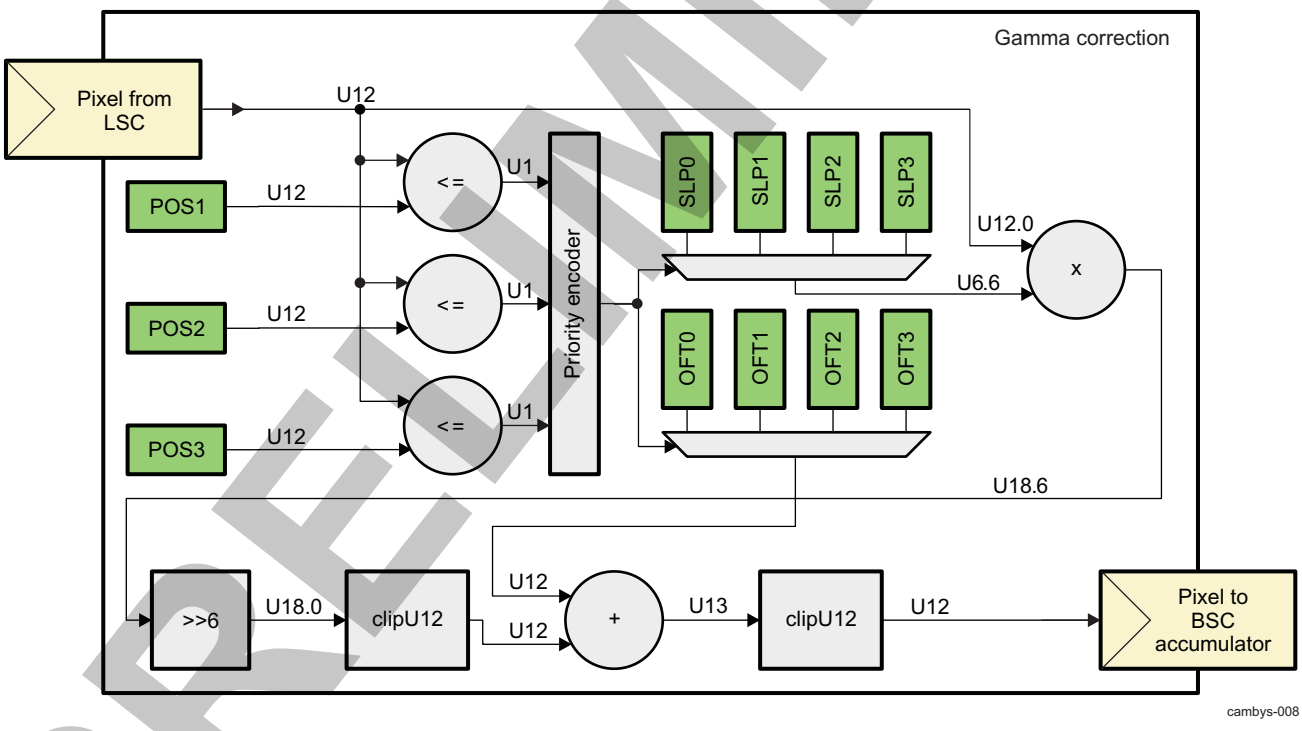
To prevent dark regions from contributing to statistics, gamma correction is applied before the BSC statistics are computed. Sensors typically have high gamma values (for example, 2.2) that produce dark images.

NOTE: Gamma correction does not impact pixel data sent to the output video port.

Gamma correction is implemented as a linear interpolation with four segments. Software can control the three inner control points. The two outer control points are fixed to (0,0) and (4095,4095). Figure 8-113, *BYS Gamma Internal Architecture*, shows the internal architecture of the gamma correction stage. The inner control points are defined by three parameters (assuming a 12-bit pixel depth):

- Position (U12.0 precision): controlled by the POSn bit field (n = 0 to 3, segment index) in the BSC_GAMMA_POS01 and BSC_GAMMA_POS23 registers
- Offset (U12.0 precision): controlled by the OFTn bit field (n = 0 to 3, segment index) in the BSC_GAMMA_OFT01 and BSC_GAMMA_OFT23 registers
- Slope (U12.6 precision): controlled by the SLPn bit field (n = 0 to 3, segment index) in the BSC_GAMMA_SLP01 and BSC_GAMMA_SLP23 registers

Figure 8-113. BYS Gamma Internal Architecture



The gamma correction algorithm first checks to which segment (n) of the gamma curve the input pixel (pixin) belongs:
If (pixin < POS1) then n = 0 (first segment);
else if (pixin < POS2) then n = 1 (second segment);
else if (pixin < POS3) then n = 2 (third segment);
else n = 3 (fourth segment);
Then it computes the output pixel value using the formula below:
$pix_{out} = SLP_n \times pix_{in} + OFT_n$

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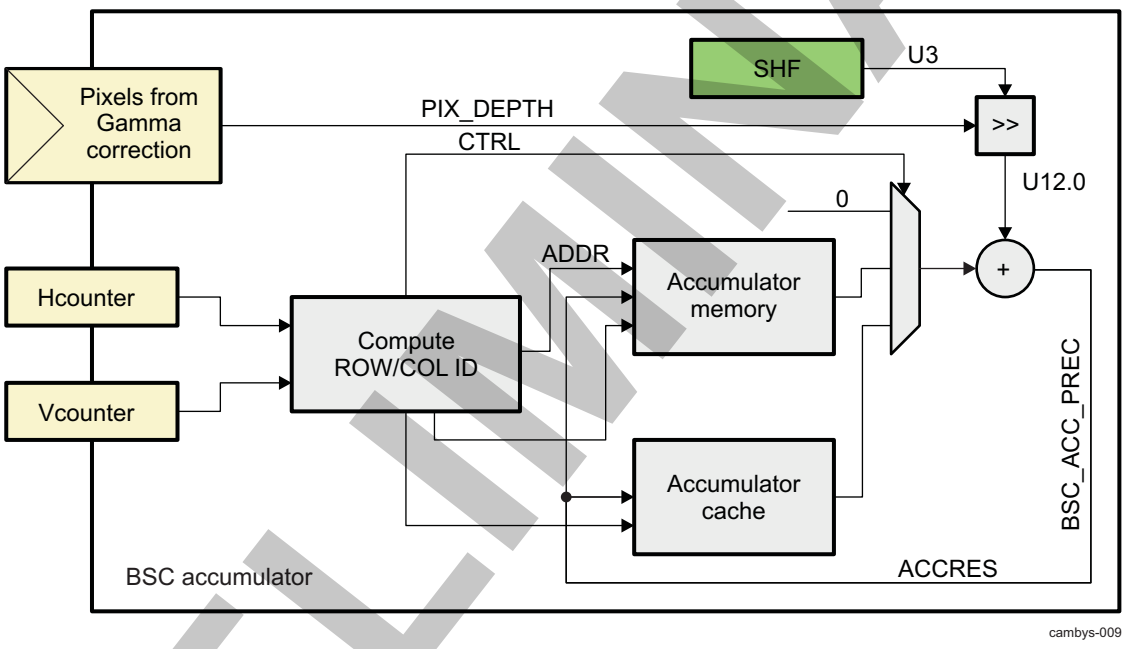
NOTE: The BSC_GAMMA_POS01[11:0] POS0 bit field is not required to implement a pure gamma function. However, it allows adding an offset to the curve. In some cases this may provide better noise robustness than multiplying low-intensity values by high gains.

By default, the Gamma Correction module is disabled (bypassed). Software must set the BSC_GLOBAL_CTRL[1] EN_GAMMA register bit to 0x1 to enable it.

8.2.9.4.7.3 BSC Accumulator

BSC decomposes the image into paxels (rectangular regions of the image) and accumulates pixel values for each paxel. The BSC accumulator module has two independent pipelines, Pipe 0 and Pipe 1, each with one with associated accumulators, ACC0 and ACC1 respectively, which can operate on the same pixel. Figure 8-114 shows a logical representation of one processing pipeline. It receives RAW12 data from the gamma correction engine and stores accumulation results in an on-chip memory. Software can read this memory using the MMR interface.

Figure 8-114. BYS BSC Accumulator Overview



Hcounter and Vcounter correspond to the pixel coordinates (after cropping and scaling operations).

The BSC accumulator computes the bin ID (= ADDR in the accumulator memory) for each incoming pixel. It also determines, if the new data is used as it is, if it is accumulated to data already in the accumulator cache, or if it is accumulated with data stored in the memory. Then the accumulation operation is performed and the result is stored in either the accumulator memory or the accumulator cache.

When BSC is used for translational stabilization, one of the processing pipelines is typically used for row summations and the other one for column summations. However, hardware does not impose any particular restrictions and software may chose to use both pipelines for row summations or to have square bins.

Figure 8-115 shows a possible configuration. BSC pipe 0 (ACC0) computes row sums using wide rectangle bins (when BSC_CTRL_i[1] SEL regietsr bit is set to 0x1) and pipe 1 (ACC1) computes column sums using tall rectangle bins (when BSC_CTRL_i[1] SEL bit is set to 0x0). Both pipes operate independently and therefore, bins from both pipes can spatially overlap. The numbers in the bins represent the accumulator ID (that is, the address offset in the BSC accumulator memory).

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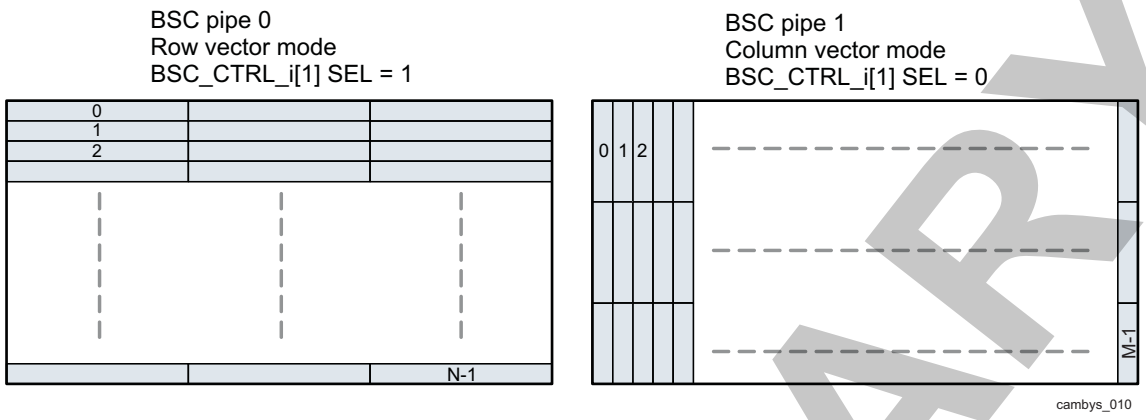
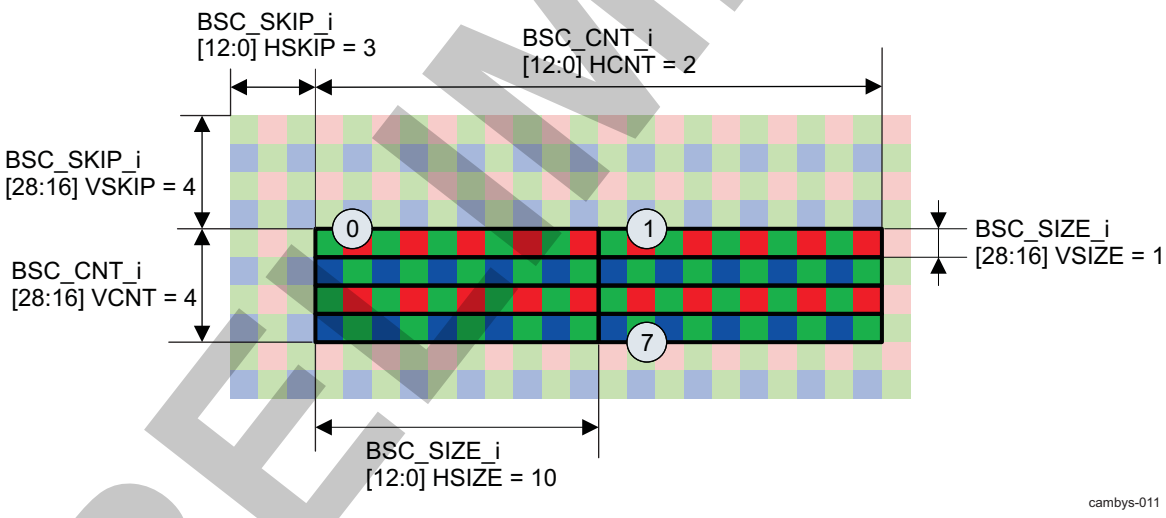
Figure 8-115. BYS BSC Bin Mapping for Row and Column Sums



Software chooses the bin size using BSC_SIZE_i[12:0] HSIZE and BSC_SIZE_i[28:16] VSIZE bit fields. The offset from the top left image corner to the first bin is defined by the BSC_SKIP_i[12:0] HSKIP and BSC_SKIP_i[28:16] VSKIP bit fields. Software also defines the numbers of bins in each direction using the BSC_CNT_i[12:0] HCNT and BSC_CNT_i[28:16] VCNT bit fields.

Figure 8-116 and Figure 8-117 show how the framing and bin size parameters, controlled by software, map to the pixels in the images when row accumulation is selected (BSC_CTRL_i[1] SEL bit = 0x1). In these two figures, only pixels shown with saturated colors are considered for the accumulation operation. All pixels in a given bin are summed together and stored in the accumulator.

Figure 8-116. BYS BSC Bin Dimensions and Framing - Example 1



NOTE: In Figure 8-116, the number of rows per bin is odd. This typically leads to irregular vectors (that is, one sums Gb+B, the next one sums R+Gr). Software can compute luminance vectors with pixel resolution by summing vectors two by two.

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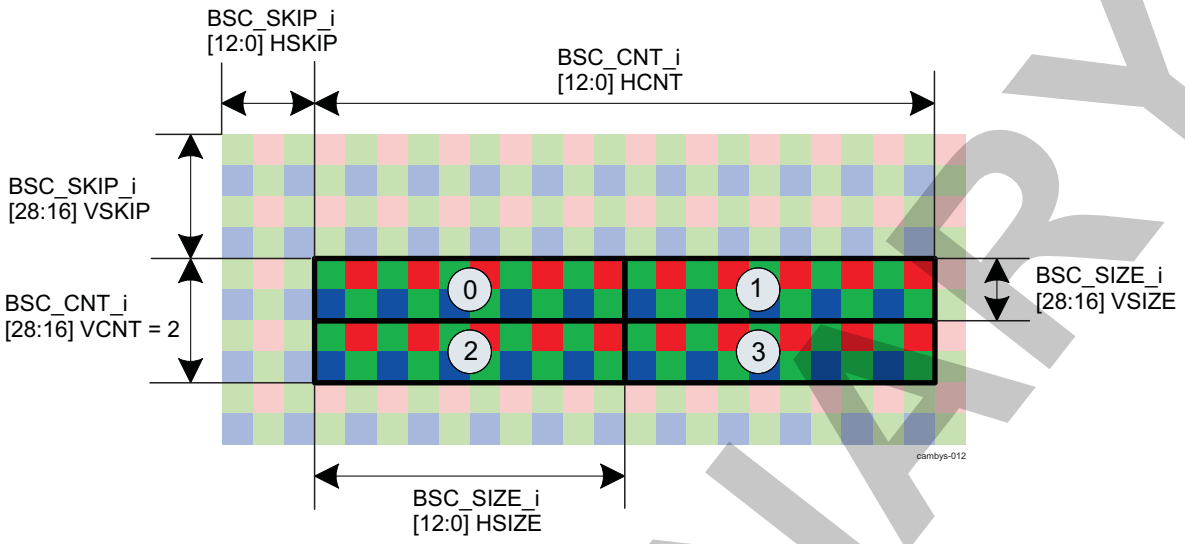
Figure 8-117. BYS BSC Bin Dimensions and Framing - Example 2



The following formulas are used to compute the bin ID for a given input pixel, located at coordinates (H,V) in the image provided by the gamma correction module.

- Hardware first checks, if the incoming pixel is in the valid image region. That is the case when all of the following four conditions below are valid:
  - H >= BSC_SKIP_i[12:0] HSKIP
  - H < BSC_SKIP_i[12:0] HSKIP + (BSC_CNT_i[12:0] HCNT * BSC_SIZE_i[12:0] HSIZE)
  - V > BSC_SKIP_i[28:16] VSKIP
  - V < BSC_SKIP_i[28:16] VSKIP + (BSC_CNT_i[28:16] VCNT * BSC_SIZE_i[28:16] VSIZE)
- If the incoming pixel is in the valid image region, the accumulator ID is computed as follows by the hardware:
  - When BSC_CTRL_i[1] SEL = 0x0, then ID = floor((H – HSKIP) / HSIZE) + HCNT × floor((V - VSKIP) / VSIZE)
  - When BSC_CTRL_i[1] SEL = 0x1, then ID = VCNT × floor((H – HSKIP) / HSIZE) + floor((V - VSKIP) / VSIZE)

Hardware does not perform the accumulation operation, when the computed accumulator ID is higher than the implemented BSC buffer size (1968 bins for ACC0, and 3456 bins for ACC1). Accumulated values are clipped to the accumulator size: 23 bits for ACC0, and 22 bits for ACC1. Therefore, no accumulator overflow can occur.

By default, BSC accumulators are initialized to 0 when the first pixel of a bin is processed. This feature can be disabled by setting the BSC_CTRL_i[2] NOINIT register bit to 0x1. Not resetting the accumulators between frames allows cumulating data over multiple frames. Software may also choose to shift pixel values before accumulation to avoid saturation, by using the BSC_CTRL_i[10:8] SHF register bit field.

Software can access the BSC accumulator during memory cycles left unused by hardware. Internal accesses performed by the hardware have higher priority than external accesses done by software. Therefore, software accesses are stalled until the memory becomes available. Software must properly synchronize its accesses with hardware operations. See Section 8.2.9.4.7.4, *BSC Memory Bandwidth Availability*, and Section 8.2.9.4.7.5, *BSC Memory Synchronization*, for more details.

The following constraints apply to BSC configuration:

- When BSC_CTRL_i[1] SEL = 0x0
  - Up to two accesses per functional clock cycle can be performed to the memory.
  - The value set in BSC_CNT_i[12:0] HCNT register bit field must be an even number.
  - The value set in BSC_SIZE_i[12:0] HSIZE register bit filed must be >= 1.
- When BSC_CTRL_i[1] SEL = 0x1

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- Only one memory access per functional clock cycle can be performed (that is, half of the BSC memory bus bandwidth).
- The value set in BSC_SIZE_i[12:0] HSIZE register bit field must be >= 2.

8.2.9.4.7.4 BSC Memory Bandwidth Availability

The hardware accesses the BSC accumulators on the left and the right border of every bin. Hardware can accommodate two accesses per functional clock cycle. Therefore, the BSC memory load (BYS_MEM_LOAD) can be computed using the formula

BYS_MEM_LOAD = PCLK / (ISS_MAIN_FCLK × BSC_SIZE_i[12:0] HSIZE),

where PCLK is the pixel readout rate from the output buffer (refer to Section 8.2.9.4.6, *ISS BYS Output Buffer*, for more details). Software can use the available BSC memory bandwidth to access the memory. Only one software access every two functional clock cycles is possible because the slave interface to the ISS interconnect runs at half the functional clock speed. Software and hardware accesses cannot be shared in the same slave interface clock cycle (that is, one software access accounts for two hardware accesses).

For example, when BSC_SIZE_i[12:0] HSIZE = 2 and PCLK = ISS_MAIN_FCLK, it is possible to perform one software access every two slave interface clock cycles, which corresponds to the maximum bandwidth supported by the slave interface to the ISS interconnect.

8.2.9.4.7.5 BSC Memory Synchronization

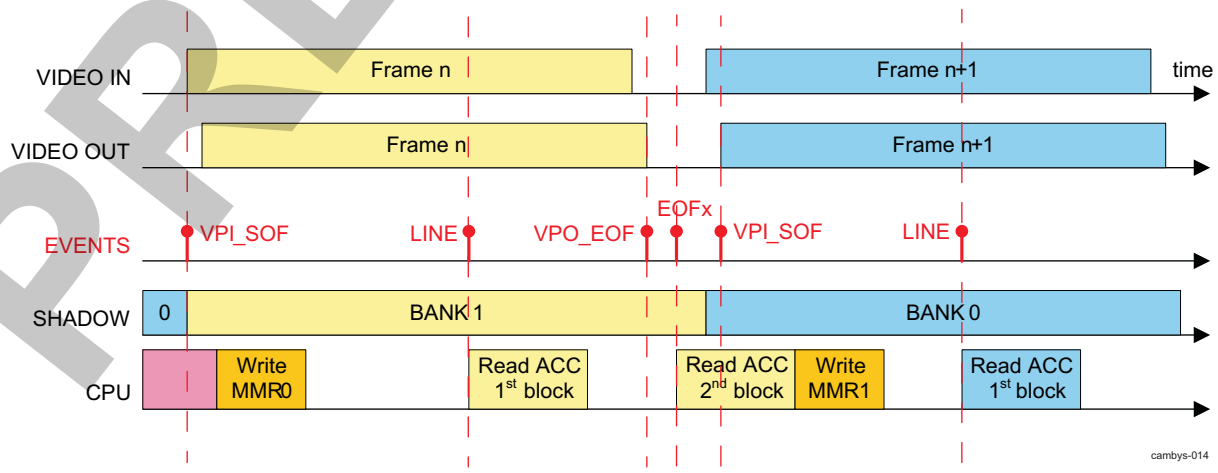
Accumulator bins are updated as pixels are received. When all pixels have been received for a given bin, the accumulator memory is ready to be read by software. Software can determine when to read out the BSC data by configuring and receiving the appropriate interrupt events.

Software can simply readout statistics for BSC accumulator pipe “x” when they have been collected for the full frame (indicated by EOFx event, see Section 8.2.9.4.2 *ISS BYS Interrupt Events*), and there is enough vertical blanking between frames.

This is not possible with small vertical blanking, because hardware may already be updating BSC accumulators before software has read all the data. In this case, it is preferred to configure the hardware to trigger two interrupt events (EOFx + LINE): one event when half of the accumulators are updated and another event when the second half of the accumulators are updated. This gives time equal to a half frame for reading half the accumulators.

Figure 8-118 below shows an example:
The software reads accumulator results and updates registers settings on a frame by frame basis. Synchronization relies on the VPI_SOF interrupt event (for MMR updates), LINE event (to readout the first block of accumulators) and EOFx event (to readout the second block of accumulator data). The VPO_EOF event is shown for reference, but not used in this example. For more details on registers shadowing mechanism, refer to Section 8.2.9.4.8, *BYS Registers Shadowing*.

Figure 8-118. BYS Hardware – Software Memory Synchronization Example



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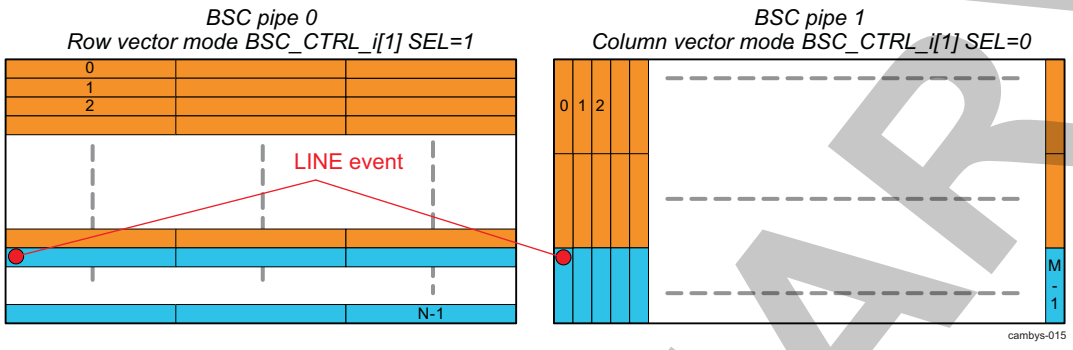
The LINE event is triggered when a significant amount of accumulated data is ready. Ideally, it will be triggered in the middle of the active image, but that is not always possible. Figure 8-119 shows an example where the LINE event is triggered after approximately two-thirds of the image.

Figure 8-119. BYS BSC Partial Readout



NOTE: Accumulators colored with orange in Figure 8-119 can be read after the LINE event. Accumulators colored with cyan can be read after EOFx events. The accumulator IDs are not contiguous in row vector mode (three separate regions).

8.2.9.4.7.6 BSC Memory DMA Requests

Each BYS module handles up to two physical DMA request signals (one per BSC accumulator pipeline). These request signals can be propagated to the device DMA_SYSTEM module to transfer accumulator content without software intervention during timing-critical periods. Refer to , *ISS BYS DMA Requests*, for more information on DMA signals mapping and configuration.

The device DMA_SYSTEM must be configured as presented in Table 8-327.

Table 8-327. BYS Configuration for DMA_SYSTEM

Setting	Read Operation	Write Operation
Address mode	Double indexed	Post incremented
Start address	Memory location of the accumulator pipes for BYS_A: • 0x5200 A000 for ACC0 • 0x5200 A800 for ACC1 Memory location of the accumulator pipes for BYS_B: • 0x5200 E000 for ACC0 • 0x5200 E800 for ACC1	Destination address in the device SDRAM memory
Element size	4 bytes	32 bit
Element index	0 bytes	N/A
Element numbers per frame	512 (2 KiB per DMA request)	512 (2 KiB per DMA request)
Frame number	BSC_DMA_REQS[] ACCn + 1 (n = 0 or 1, BSC accumulator index)	BSC_DMA_REQS[] ACCn + 1 (n = 0 or 1, BSC accumulator index)
Frame index	– 2 KiB	N/A

The BYS module is typically configured to read the complete accumulator content when it has been updated.

- BSC_DMA_REQS[] ACCn = ceil(ENTRIES_TO_READ / 512) – 1, where n = 0 or 1 is the BSC accumulator index, and ENTRIES_TO_READ is up to 1968 for ACC0, and up to 3456 for ACC1.
- Trigger event = EOFx (all data has been updated, see Section 8.2.9.4.2, *ISS BYS Interrupt Events*).

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It is also possible to read out the buffer in two halves, when column mode is selected (when BSC_CTRL_i[1] SEL = 0x0) and vertical blanking is low. That is done by enabling the follwong two trigger events (see Section 8.2.9.4.2, *ISS BYS Interrupt Events*):

- LINE: when the first half of the buffer has been updated
- EOFx: when the second half of the buffer has been updated

In that case, the value of BSC_DMA_REQS[] ACCn register bit field must correspond to the first half of the buffer (with adequate rounding to the 2 KiB boundaries).

NOTE: Readout in two halves for row mode (when BSC_CTRL_i[1] SEL = 0x1) must be done using software. The implemented hardware DMA request generation mechanism is not designed for that.

Software may use interrupts generated by the device DMA_SYSTEM to detect when all data has been transferred. Refer to *System DMA* chapter for more information.

8.2.9.4.8 ISS BYS Registers Shadowing

Table 8-328 shows which BYS registers are shadowed. All registers that are expected to be changed on a frame-by-frame basis are shadowed to remove register updates from the critical software timing path.

Table 8-328. BYS Shadow Registers

Register	Shadowed ?	Register	Shadowed ?
BYS_HL_REVISION	NO	BSC_GLOBAL_CTRL	YES
BYS_HL_HWINFO	NO	BSC_LSC_OFT	YES
BYS_HL_HWINFO2	NO	BSC_LSC_A1	YES
BYS_HL_SYSCONFIG	NO	BSC_LSC_A2	YES
BYS_HL_IRQSTATUS_RAW	NO	BSC_LSC_S	YES
BYS_HL_IRQSTATUS	NO	BSC_LSC_GAN_0X	YES
BYS_HL_IRQENABLE_SET	NO	BSC_LSC_GAN_1X	YES
BYS_HL_IRQENABLE_CLR	NO	BSC_LSC_OFT_0X	YES
BYS_DMAENABLE_SET	NO	BSC_LSC_OFT_1X	YES
BYS_DMAENABLE_CLR	NO	BSC_LSC_SHF	YES
BYS_CTRL[3:2] EN_SHADOW	NO	BSC_LSC_MAX	YES
BYS_CTRL [all other bits]	YES	BSC_GAMMA_POS01	NO
BYS_HCROP	YES	BSC_GAMMA_POS23	NO
BYS_VCROP	YES	BSC_GAMMA_OFT01	NO
BYS_SCALE	YES	BSC_GAMMA_OFT23	NO
BYS_HINIT	YES	BSC_GAMMA_SLP01	NO
BYS_VINIT	YES	BSC_GAMMA_SLP23	NO
BYS_OSIZE	YES	BSC_CTRL_i	YES
BYS_FIFO_BW	YES	BSC_SKIP_i	YES
BYS_DPCBRT	YES	BSC_SIZE_i	YES
BYS_DPCTHR	YES	BSC_CNT_i	YES
BYS_LINE	YES		

Two instances exist for each shadow register. Software can choose which instance is accessed by hardware and which one is accessed by software. In automatic mode, register banks are swapped just before the first pixel of a new frame is received at the input video port. Software has a complete frame to update registers without interfering with hardware operation.

The following four shadowing modes are supported and can be selected by the BYS_CTRL[3:2] EN_SHADOW bit field:

1. EN_SHADOW = 0x0: No shadowing; hardware and software access bank 0

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2. EN_SHADOW = 0x1: No shadowing; hardware and software access bank 1
3. EN_SHADOW = 0x2: Shadowing; hardware access bank 0 and software bank 1
4. EN_SHADOW = 0x3: Shadowing; hardware access bank 1 and software bank 0

Software can monitor the BYS_CTRL[8:7] SHADOW_STATE bit-field to check which mode is currently being used by HW.

Hardware automatically swaps between mode 2 and mode 3, when the first pixel of a valid frame is received on the input video port. The VPI_SOF interrupt event also notifies software of reception of the first pixel . Software may use this event to preload shadowed registers for the next frame.

NOTE: Hardware first swaps banks and then processes the first pixel, so that the same settings apply to all pixels of the frame. The BYS module implements a global shadowing mechanism: all settings are modified in the same time. Therefore, software must ensure that no more processing is ongoing when banks are swapped. Practically, this implies that there is enough vertical blanking between frames so that the VPO_EOF and EOFx interrupt events are triggered before the VPI_SOF event of the next frame.

After reset, registers shadowing and data processing are disabled, and both software and hardware access bank 0. Software must program all registers belonging to used functions except the BYS_CTRL register. The BYS module ignores incoming pixels during the configuration phase because after reset the BYS_CTRL[4] EN_BYS register bit is 0x0. Therefore, no side effects can occur, even if the input video stream is active.

After the new settings have been written by software into bank 0, the next step is to set the BYS_CTRL[4] EN_BYS bit to 0x1 and BYS_CTRL[3:2] EN_SHADOW bit field to 0x3. Hardware continues to see EN_BYS = 0, as it now accesses bank 1 which still contains reset values. Hardware swaps banks when the first pixel of the next valid frame is received on the input video port. Hardware now accesses bank 0 (EN_BYS = 1) and therefore processes the frame with proper settings.

CAUTION

The above mechanism ensures that new settings can only be applied on clean frame boundaries. Changing settings in the middle of a frame (that is, without using the shadowing mechanism) can lead to unpredictable behavior of hardware.

8.2.9.5 ISS BYS Register Manual

8.2.9.5.1 ISS BYS Instance Summary

Table 8-329. BYS Instance Summary

Module Name	L3_MAIN Base Address	Size
BYS_B	0x5200 8000	512 bytes
BYS_A	0x5200 C000	512 bytes

8.2.9.5.2 ISS BYS Registers

8.2.9.5.2.1 ISS BYS Register Summary

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Table 8-330. BYS Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	BYS_B L3_MAIN Physical Address	BYS_A L3_MAIN Physical Address
BYS_HL_REVISION	R	32	0x0000 0000	0x5200 8000	0x5200 C000
BYS_HL_HWINFO	R	32	0x0000 0004	0x5200 8004	0x5200 C004
BYS_HL_HWINFO2	R	32	0x0000 0008	0x5200 8008	0x5200 C008
RESERVED	R	32	0x0000 000C	0x5200 800C	0x5200 C00C
BYS_HL_SYSCONFIG	RW	32	0x0000 0010	0x5200 8010	0x5200 C010
RESERVED	R	32	0x0000 001C	0x5200 801C	0x5200 C01C
BYS_HL_IRQSTATUS_RAW	RW	32	0x0000 0020	0x5200 8020	0x5200 C020
BYS_HL_IRQSTATUS	RW	32	0x0000 0024	0x5200 8024	0x5200 C024
BYS_HL_IRQENABLE_SET	RW	32	0x0000 0028	0x5200 8028	0x5200 C028
BYS_HL_IRQENABLE_CLR	RW	32	0x0000 002C	0x5200 802C	0x5200 C02C
BYS_DMAENABLE_SET	RW	32	0x0000 0030	0x5200 8030	0x5200 C030
BYS_DMAENABLE_CLR	RW	32	0x0000 0034	0x5200 8034	0x5200 C034
BYS_CTRL	RW	32	0x0000 0040	0x5200 8040	0x5200 C040
BYS_HCROP	RW	32	0x0000 0044	0x5200 8044	0x5200 C044
BYS_VCROP	RW	32	0x0000 0048	0x5200 8048	0x5200 C048
BYS_SCALE	RW	32	0x0000 004C	0x5200 804C	0x5200 C04C
BYS_HINIT	RW	32	0x0000 0050	0x5200 8050	0x5200 C050
BYS_VINIT	RW	32	0x0000 0054	0x5200 8054	0x5200 C054
BYS_OSIZE	RW	32	0x0000 0058	0x5200 8058	0x5200 C058
BYS_FIFO_BW	RW	32	0x0000 005C	0x5200 805C	0x5200 C05C
BYS_DPCBRT	RW	32	0x0000 0060	0x5200 8060	0x5200 C060
BYS_DPCTHR	RW	32	0x0000 0064	0x5200 8064	0x5200 C064
BYS_LINE	RW	32	0x0000 006C	0x5200 806C	0x5200 C06C
BSC_GLOBAL_CTRL	RW	32	0x0000 0070	0x5200 8070	0x5200 C070
BSC_LSC_OFT	RW	32	0x0000 0074	0x5200 8074	0x5200 C074
BSC_LSC_A1	RW	32	0x0000 0078	0x5200 8078	0x5200 C078
BSC_LSC_A2	RW	32	0x0000 007C	0x5200 807C	0x5200 C07C
BSC_LSC_S	RW	32	0x0000 0080	0x5200 8080	0x5200 C080
BSC_LSC_GAN_0X	RW	32	0x0000 0084	0x5200 8084	0x5200 C084
BSC_LSC_GAN_1X	RW	32	0x0000 008C	0x5200 808C	0x5200 C08C
BSC_LSC_OFT_0X	RW	32	0x0000 0090	0x5200 8090	0x5200 C090
BSC_LSC_OFT_1X	RW	32	0x0000 0094	0x5200 8094	0x5200 C094
BSC_LSC_SHF	RW	32	0x0000 0098	0x5200 8098	0x5200 C098
BSC_LSC_MAX	RW	32	0x0000 009C	0x5200 809C	0x5200 C09C
BSC_GAMMA_POS01	RW	32	0x0000 00A0	0x5200 80A0	0x5200 C0A0
BSC_GAMMA_POS23	RW	32	0x0000 00A4	0x5200 80A4	0x5200 C0A4
BSC_GAMMA_OFT01	RW	32	0x0000 00B0	0x5200 80B0	0x5200 C0B0

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Table 8-330. BYS Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	BYS_B L3_MAIN Physical Address	BYS_A L3_MAIN Physical Address
BSC_GAMMA_OFT23	RW	32	0x0000 00B4	0x5200 80B4	0x5200 C0B4
BSC_GAMMA_SLP01	RW	32	0x0000 00C0	0x5200 80C0	0x5200 C0C0
BSC_GAMMA_SLP23	RW	32	0x0000 00C4	0x5200 80C4	0x5200 C0C4
BSC_PAGE	RW	32	0x0000 00C8	0x5200 80C8	0x5200 C0C8
BSC_DMA_REQS	RW	32	0x0000 00CC	0x5200 80CC	0x5200 C0CC
BSC_CTRL_i (1)	RW	32	0x0000 0100 + (0x20 * i)	0x5200 8100 + (0x20 * i)	0x5200 C100 + (0x20 * i)
BSC_SKIP_i (1)	RW	32	0x0000 0104 + (0x20 * i)	0x5200 8104 + (0x20 * i)	0x5200 C104 + (0x20 * i)
BSC_SIZE_i (1)	RW	32	0x0000 0108 + (0x20 * i)	0x5200 8108 + (0x20 * i)	0x5200 C108 + (0x20 * i)
BSC_CNT_i (1)	RW	32	0x0000 010C + (0x20 * i)	0x5200 810C + (0x20 * i)	0x5200 C10C + (0x20 * i)

(1) i = 0 to 1

8.2.9.5.2.2 ISS BYS Register Description

Table 8-331. BYS_HL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5200 8000 0x5200 C000	**Instance**	BYS_B BYS_A
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See (1)

(1) TI internal data

Table 8-332. Register Call Summary for Register BYS_HL_REVISION

ISS Interfaces

- ISS BYS Registers Shadowing: [0]
- ISS BYS Registers: [1]

Table 8-333. BYS_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5200 8004 0x5200 C004	**Instance**	BYS_B BYS_A
Description	Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any).		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MAX_HEIGHT								MAX_OWIDTH														PIX_DEPTH	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:15	MAX_OHEIGHT	Maximum output height	R	0x0794
14:2	MAX_OWIDTH	Maximum output width	R	0x0BA6
1:0	PIX_DEPTH	Number of bits per pixel Read 0x3: 16 Read 0x2: 14 Read 0x1: 12 Read 0x0: 10	R	0x1

Table 8-334. Register Call Summary for Register BYS_HL_HWINFO

ISS Interfaces
- ISS BYS Registers Shadowing: [0]
- ISS BYS Registers: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]

Table 8-335. BYS_HL_HWINFO2

Address Offset	0x0000 0008		
Physical Address	0x5200 8008 0x5200 C008	**Instance**	BYS_B BYS_A
Description	Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACC1_COUNT												ACC1_PREC				ACC0_COUNT												ACC0_PREC			

Bits	Field Name	Description	Type	Reset
31:20	ACC1_COUNT	Number of entries = value*2	R	0x6C0
19:16	ACC1_PREC	Precision of accumulator 0 Number of Bits = value + 20	R	0x2
15:4	ACC0_COUNT	Number of entries = value*2	R	0x3D8
3:0	ACC0_PREC	Precision of accumulator 0 Number of Bits = value + 20	R	0x3

Table 8-336. Register Call Summary for Register BYS_HL_HWINFO2

ISS Interfaces
- ISS BYS Registers Shadowing: [0]
- ISS BYS Registers: [1] [2]

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Table 8-337. BYS_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5200 8010 0x5200 C010	**Instance**	BYS_B BYS_A
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SOFTRESET

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	SOFTRESET	Software reset Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0

Table 8-338. Register Call Summary for Register BYS_HL_SYSCONFIG

ISS Interfaces

- ISS BYS Reset: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

Table 8-339. BYS_HL_IRQSTATUS_RAW

Address Offset	0x0000 0020		
Physical Address	0x5200 8020 0x5200 C020	**Instance**	BYS_B BYS_A
Description	Per-event raw interrupt status vector, line #0. Raw status is set even if event is not enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VPO_EOF	EOF3	EOF2	EOF1	EOF0	H2V_OVR	OB_OVR	LINE	VPI_SOF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	VPO_EOF	Output video port end of frame event. Read 0x1: Event pending Read 0x0: No event pending	RW	0
7	EOF3	Read 0x1: Event pending Read 0x0: No event pending	RW	0
6	EOF2	Read 0x1: Event pending Read 0x0: No event pending	RW	0

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Bits	Field Name	Description	Type	Reset
5	EOF1	End of frame event of BSC pipe #1 Read 0x1: Event pending Read 0x0: No event pending	RW	0
4	EOF0	End of frame event of BSC pipe #0 Read 0x1: Event pending Read 0x0: No event pending	RW	0
3	H2V_OVR	H2V FIFO overflow Read 0x1: Event pending Read 0x0: No event pending	RW	0
2	OB_OVR	Output buffer overflow Read 0x1: Event pending Read 0x0: No event pending	RW	0
1	LINE	Line event. Read 0x1: Event pending Read 0x0: No event pending	RW	0
0	VPI_SOF	Start of frame event. Read 0x1: Event pending Read 0x0: No event pending	RW	0

Table 8-340. Register Call Summary for Register BYS_HL_IRQSTATUS_RAW

ISS Interfaces

- ISS BYS Registers Shadowing: [0]
- ISS BYS Registers: [1]

Table 8-341. BYS_HL_IRQSTATUS

Address Offset	0x0000 0024		
Physical Address	0x5200 8024 0x5200 C024	**Instance**	BYS_B BYS_A
Description	Per-event "enabled" interrupt status vector, line #0. Enabled status isn't set unless event is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							VPO_EOF	EOF3	EOF2	EOF1	EOF0	H2V_OVR	OB_OVR	LINE	VPI_SOF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	VPO_EOF	Output video port end of frame event. Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW	0
7	EOF3	Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW	0
6	EOF2	Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW	0

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Bits	Field Name	Description	Type	Reset
5	EOF1	End of frame event of BSC pipe #1 Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW	0
4	EOF0	End of frame event of BSC pipe #0 Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW	0
3	H2V_OVR	H2V FIFO overflow Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW	0
2	OB_OVR	Output buffer overflow Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW	0
1	LINE	Line event. Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW	0
0	VPI_SOF	Start of frame event. Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW	0

Table 8-342. Register Call Summary for Register BYS_HL_IRQSTATUS

ISS Interfaces

- ISS BYS Interrupt Events: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

Table 8-343. BYS_HL_IRQENABLE_SET

Address Offset	0x0000 0028		
Physical Address	0x5200 8028 0x5200 C028	**Instance**	BYS_B BYS_A
Description	Per-event interrupt enable bit vector Write 1 to set (enable interrupt). Readout equal to corresponding BYS_HL_IRQENABLE_CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							VPO_EOF	EOF3	EOF2	EOF1	EOF0	H2V_OVR	OB_OVR	LINE	VPI_SOF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	VPO_EOF	Output video port end of frame event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
7	EOF3	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
6	EOF2	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
5	EOF1	End of frame event of BSC pipe #1 Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
4	EOF0	End of frame event of BSC pipe #0 Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
3	H2V_OVR	H2V FIFO overflow Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
2	OB_OVR	Output buffer overflow Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
1	LINE	Line event Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
0	VPI_SOF	Start of frame event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

Table 8-344. Register Call Summary for Register BYS_HL_IRQENABLE_SET

ISS Interfaces

- ISS BYS Interrupt Events: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2] [3]

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Table 8-345. BYS_HL_IRQENABLE_CLR

Address Offset	0x0000 002C		
Physical Address	0x5200 802C 0x5200 C02C	**Instance**	BYS_B BYS_A
Description	Per-event interrupt enable bit vector Write 1 to clear (disable interrupt). Readout equal to corresponding BYS_HL_IRQENABLE_SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							VPO_EOF	EOF3	EOF2	EOF1	EOF0	H2V_OVR	OB_OVR	LINE	VPI_SOF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	VPO_EOF	Output video port end of frame event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
7	EOF3	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
6	EOF2	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
5	EOF1	End of frame event of BSC pipe #1 Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
4	EOF0	End of frame event of BSC pipe #0 Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
3	H2V_OVR	H2V FIFO overflow Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
2	OB_OVR	Output buffer overflow. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
1	LINE	Line event Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
0	VPI_SOF	Start of frame event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

Table 8-346. Register Call Summary for Register BYS_HL_IRQENABLE_CLR

ISS Interfaces

- ISS BYS Interrupt Events: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2] [3]

Table 8-347. BYS_DMAENABLE_SET

Address Offset	0x0000 0030		
Physical Address	0x5200 8030 0x5200 C030	**Instance**	BYS_B BYS_A
Description	DMAREQUEST[0] Bits 7..0 DMAREQUEST[1] Bits 15..8 DMAREQUEST[2] Bits 23..16 DMAREQUEST[3] Bits 31..24 Write 1 to set (enable DMA request generation). Readout equal to corresponding BYS_DMAENABLE_CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		CH3_VPO_EOF	CH3_EOF3	CH3_H2V_OVR	CH3_OB_OVR	CH3_LINE	CH3_VPI_SOF	RESERVED		CH2_VPO_EOF	CH2_EOF2	CH2_H2V_OVR	CH2_OB_OVR	CH2_LINE	CH2_VPI_SOF	RESERVED		CH1_VPO_EOF	CH1_EOF1	CH1_H2V_OVR	CH1_OB_OVR	CH1_LINE	CH1_VPI_SOF	RESERVED		CH0_VPO_EOF	CH0_EOF0	CH0_H2V_OVR	CH0_OB_OVR	CH0_LINE	CH0_VPI_SOF

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	CH3_VPO_EOF	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
28	CH3_EOF3	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0

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Bits	Field Name	Description	Type	Reset
27	CH3_H2V_OVR	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
26	CH3_OB_OVR	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
25	CH3_LINE	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
24	CH3_VPI_SOF	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
23:22	RESERVED		R	0x0
21	CH2_VPO_EOF	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
20	CH2_EOF2	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
19	CH2_H2V_OVR	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
18	CH2_OB_OVR	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
17	CH2_LINE	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
16	CH2_VPI_SOF	Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
15:14	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
13	CH1_VPO_EOF	Output video port end of frame event. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
12	CH1_EOF1	End of frame event of BSC pipe #1 Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
11	CH1_H2V_OVR	H2V FIFO overflow Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
10	CH1_OB_OVR	Output buffer overflow. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
9	CH1_LINE	Line event Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
8	CH1_VPI_SOF	Start of frame event. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
7:6	RESERVED		R	0x0
5	CH0_VPO_EOF	Output video port end of frame event. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
4	CH0_EOF0	End of frame event of BSC pipe #0 Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
3	CH0_H2V_OVR	H2V FIFO overflow Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0

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Bits	Field Name	Description	Type	Reset
2	CH0_OB_OVR	Output buffer overflow. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
1	CH0_LINE	Line event Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
0	CH0_VPI_SOF	Start of frame event. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0

Table 8-348. Register Call Summary for Register BYS_DMAENABLE_SET

ISS Interfaces
- ISS BYS DMA Requests: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2] [3]

Table 8-349. BYS_DMAENABLE_CLR

Address Offset	0x0000 0034		
Physical Address	0x5200 8034 0x5200 C034	**Instance**	BYS_B BYS_A
Description	DMAREQUEST[0] Bits 7..0 DMAREQUEST[1] Bits 15..8 DMAREQUEST[2] Bits 23..16 DMAREQUEST[3] Bits 31..24 Write 1 to clear (disable DMA request generation). Readout equal to corresponding BYS_DMAENABLE_SET register.		
Type	RW		

31 30	29	28	27	26	25	24	23 22	21	20	19	18	17	16	15 14	13	12	11	10	9	8	7 6	5	4	3	2	1	0
RESERVED	CH3_VPO_EOF	CH3_EOF3	CH3_H2V_OVR	CH3_OB_OVR	CH3_LINE	CH3_VPI_SOF	RESERVED	CH2_VPO_EOF	CH2_EOF2	CH2_H2V_OVR	CH2_OB_OVR	CH2_LINE	CH2_VPI_SOF	RESERVED	CH1_VPO_EOF	CH1_EOF1	CH1_H2V_OVR	CH1_OB_OVR	CH1_LINE	CH1_VPI_SOF	RESERVED	CH0_VPO_EOF	CH0_EOF0	CH0_H2V_OVR	CH0_OB_OVR	CH0_LINE	CH0_VPI_SOF

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	CH3_VPO_EOF	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0

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Bits	Field Name	Description	Type	Reset
28	CH3_EOF3	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
27	CH3_H2V_OVR	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
26	CH3_OB_OVR	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
25	CH3_LINE	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
24	CH3_VPI_SOF	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
23:22	RESERVED		R	0x0
21	CH2_VPO_EOF	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
20	CH2_EOF2	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
19	CH2_H2V_OVR	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
18	CH2_OB_OVR	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
17	CH2_LINE	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
16	CH2_VPI_SOF	Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0

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Bits	Field Name	Description	Type	Reset
15:14	RESERVED		R	0x0
13	CH1_VPO_EOF	Output video port end of frame event. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
12	CH1_EOF1	End of frame event of BSC pipe #1 Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
11	CH1_H2V_OVR	H2V FIFO overflow Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
10	CH1_OB_OVR	Output buffer overflow. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
9	CH1_LINE	Line event Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
8	CH1_VPI_SOF	Start of frame event Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
7:6	RESERVED		R	0x0
5	CH0_VPO_EOF	Output video port end of frame event. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
4	CH0_EOF0	End of frame event of BSC pipe #0 Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
3	CH0_H2V_OVR	H2V FIFO overflow Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0

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Bits	Field Name	Description	Type	Reset
2	CH0_OB_OVR	Output buffer overflow. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
1	CH0_LINE	Line event Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0
0	CH0_VPI_SOF	Start of frame event Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW	0

Table 8-350. Register Call Summary for Register BYS_DMAENABLE_CLR

ISS Interfaces
- ISS BYS DMA Requests: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2] [3]

Table 8-351. BYS_CTRL

Address Offset	0x0000 0040		
Physical Address	0x5200 8040 0x5200 C040	**Instance**	BYS_B BYS_A
Description	Global control of the BYS module		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SHADOW_STATE		NO_AUTOGATING	VPORT_FORCEON	EN_BYS	EN_SHADOW		EN_DPC	EN

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8:7	SHADOW_STATE	Indicates the shadow register currently in use by the hardware. Register written by hardware. Software must check this before writing the BYS_CTRL register when BYS is active, so that a write into EN_SHADOW bit-field does not unintentionally swap banks. Read 0x0: No shadowing. Hardware and software access bank 0. Read 0x1: No shadowing. Hardware and software access bank 1. Read 0x2: Shadowing. Hardware access bank 0 and software access bank 1. Read 0x3: Shadowing. Hardware access bank 1 and software access bank 0.	R	0x0

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Bits	Field Name	Description	Type	Reset
6	NO_AUTOGATING	Control internal autogating. ** DEBUG FEATURE ** 0x0: Autogating enabled. This is the recommended behavior 0x1: Autogating disabled Power consumption is increased. Only for debug purposes.	RW	0
5	VPORT_FORCEON	Controls gating of the output video port clock 0x0: Auto-gating. The video port clock is - enabled when pixels are sent - enabled 4 cycles before the 1st pixel is sent - disabled 4 pixels after the last pixel has been sent - disabled otherwise 0x1: The pixel clock is free-running during blanking	RW	0
4	EN_BYS	Enable bayer scaler 0x0: Disabled. Bayer scaler processing is bypassed (i.e. the output of the bayer scaler is the same than the bayer scaler input) 0x1: Bayer scaler enabled	RW	0
3:2	EN_SHADOW	Controls register shadowing. Register written by software. 0x0: No shadowing. Hardware and software access bank 0 0x1: No shadowing. Hardware and software access bank 1 0x3: Shadowing. Hardware access bank 1 and software access bank 0. 0x2: Shadowing. Hardware access bank 0 and software access bank 1.	RW	0x0
1	EN_DPC	Enable defect pixel correction 0x0: Defect pixel correction bypassed 0x1: Defect pixel correction enabled	RW	0
0	EN	Enable the BYS module 0x0: Module disabled. Incoming pixels are ignored. 0x1: Enabled Incoming pixels will be processed.	RW	0

Table 8-352. Register Call Summary for Register BYS_CTRL

ISS Interfaces

- ISS BYS Video Ports: [0]
- ISS BYS Block Diagram: [1] [2]
- ISS BYS Defect Pixel Correction: [3]
- ISS BYS Registers Shadowing: [4] [5] [6] [7] [8] [9] [10] [11]
- ISS BYS Registers: [12] [13]

Table 8-353. BYS_HCROP

Address Offset	0x0000 0044		
Physical Address	0x5200 8044 0x5200 C044	**Instance**	BYS_B BYS_A
Description	Horizontal cropping settings. SKIP and COUNT positions must be multiples of 4 pixels.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT								RESERVED								SKIP							RESERVED

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:18	COUNT	In steps of 4 pixels (i.e. write number of pixels to count divided by 4 into this register)	RW	0x000
17:14	RESERVED		R	0x0
13:2	SKIP	In steps of 4 pixels (i.e. write number of pixels to skip divided by 4 into this register)	RW	0x000
1:0	RESERVED		R	0x0

Table 8-354. Register Call Summary for Register BYS_HCROP

ISS Interfaces
- ISS BYS Cropping: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

Table 8-355. BYS_VCROP

Address Offset	0x0000 0048		
Physical Address	0x5200 8048 0x5200 C048	**Instance**	BYS_B BYS_A
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT								RESERVED								SKIP							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	COUNT	Vertical pixel count to be sent through	RW	0x0000
15:14	RESERVED		R	0x0
13:0	SKIP	Number of vertical skip of pixels	RW	0x0000

Table 8-356. Register Call Summary for Register BYS_VCROP

ISS Interfaces
- ISS BYS Cropping: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

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Table 8-357. BYS_SCALE

Address Offset	0x0000 004C		
Physical Address	0x5200 804C 0x5200 C04C	**Instance**	BYS_B BYS_A
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VSCALE								RESERVED								HSCALE							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	VSCALE	Vertical down scaling	RW	0x0000
15:14	RESERVED		R	0x0
13:0	HSCALE	Horizantal down scaling	RW	0x0000

Table 8-358. Register Call Summary for Register BYS_SCALE

ISS Interfaces

- ISS BYS Scaler and H2V FIFO: [0] [1] [2] [3]
- ISS BYS Registers Shadowing: [4]
- ISS BYS Registers: [5]

Table 8-359. BYS_HINIT

Address Offset	0x0000 0050		
Physical Address	0x5200 8050 0x5200 C050	**Instance**	BYS_B BYS_A
Description	Initial phase - horizontal scaler		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								INI1								RESERVED								INI0							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	INI1	Horizantal Phase init for odd line	RW	0x0000
15:14	RESERVED		R	0x0
13:0	INI0	Horizantal Phase init for even line	RW	0x0000

Table 8-360. Register Call Summary for Register BYS_HINIT

ISS Interfaces

- ISS BYS Scaler and H2V FIFO: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS BYS Registers Shadowing: [8]
- ISS BYS Registers: [9]

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Table 8-361. BYS_VINIT

Address Offset	0x0000 0054		
Physical Address	0x5200 8054 0x5200 C054	**Instance**	BYS_B BYS_A
Description	Initial phase - vertical scaler		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								INI1								RESERVED								INI0							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	INI1	vertical Phase init for odd line	RW	0x0000
15:14	RESERVED		R	0x0
13:0	INI0	vertical Phase init for even line	RW	0x0000

Table 8-362. Register Call Summary for Register BYS_VINIT

ISS Interfaces

- ISS BYS Scaler and H2V FIFO: [0] [1] [2] [3] [4] [5]
- ISS BYS Registers Shadowing: [6]
- ISS BYS Registers: [7]

Table 8-363. BYS_OSIZE

Address Offset	0x0000 0058		
Physical Address	0x5200 8058 0x5200 C058	**Instance**	BYS_B BYS_A
Description	Image size writen by the bayer scaler into the output FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VSIZE								RESERVED								HSIZE							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	VSIZE	Max output number of lines size Valid range: 1.. BYS_HL_HWINFO[27:15] MAX_OHEIGHT	RW	0x0000
15:13	RESERVED		R	0x0
12:0	HSIZE	Max output line size Valid range: 1.. BYS_HL_HWINFO[14:2] MAX_OWIDTH	RW	0x0000

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Table 8-364. Register Call Summary for Register BYS_OSIZE

ISS Interfaces
- ISS BYS Scaler and H2V FIFO: [0] [1] [2] [3]
- ISS BYS Registers Shadowing: [4]
- ISS BYS Registers: [5]

Table 8-365. BYS_FIFO_BW

Address Offset	0x0000 005C		
Physical Address	0x5200 805C 0x5200 C05C	**Instance**	BYS_B BYS_A
Description	Controls the data readout rate from the H2V and OUTPUT FIFOs		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OB																H2V															

Bits	Field Name	Description	Type	Reset
31:16	OB	Output buffer readout speed. U1.15 Valid range: 0.000030517578125 .. 1	RW	0x0000
15:0	H2V	H2V buffer readout speed. U1.15 Valid range: 0.000030517578125 .. 1	RW	0x0000

Table 8-366. Register Call Summary for Register BYS_FIFO_BW

ISS Interfaces
- ISS BYS Video Ports: [0]
- ISS BYS Scaler and H2V FIFO: [1] [2]
- ISS BYS Output Buffer: [3] [4]
- ISS BYS Registers Shadowing: [5]
- ISS BYS Registers: [6]

Table 8-367. BYS_DPCBRT

Address Offset	0x0000 0060		
Physical Address	0x5200 8060 0x5200 C060	**Instance**	BYS_B BYS_A
Description	Sets threshold adaptation based on brightness of neighborhood. This is a linear function		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SLP								RESERVED				THR											

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	SLP	U8Q3 Slope of threshold increase	RW	0x00
15:12	RESERVED		R	0x0
11:0	THR	U12 Minimum brightness level to begin increasing threshold	RW	0x000

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Table 8-368. Register Call Summary for Register BYS_DPCBRT

ISS Interfaces

- ISS BYS Defect Pixel Correction: [0] [1] [2]
- ISS BYS Registers Shadowing: [3]
- ISS BYS Registers: [4]

Table 8-369. BYS_DPCTHR

Address Offset	0x0000 0064		
Physical Address	0x5200 8064 0x5200 C064	**Instance**	BYS_B BYS_A
Description	Sets DPC detection threshold limits		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MAX								RESERVED								MIN							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	MAX	Maximum DPC threshold value	RW	0x000
15:12	RESERVED		R	0x0
11:0	MIN	Minimum DPC threshold value.	RW	0x000

Table 8-370. Register Call Summary for Register BYS_DPCTHR

ISS Interfaces

- ISS BYS Defect Pixel Correction: [0] [1] [2]
- ISS BYS Registers Shadowing: [3]
- ISS BYS Registers: [4]

Table 8-371. BYS_LINE

Address Offset	0x0000 006C		
Physical Address	0x5200 806C 0x5200 C06C	**Instance**	BYS_B BYS_A
Description	Line number for the LINE IRQ.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				LINE											

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x0 0000
12:0	LINE	Valid range 0.. BYS_HL_HWINFO[27:15] MAX_OHEIGHT	RW	0x0000

Table 8-372. Register Call Summary for Register BYS_LINE

ISS Interfaces

- ISS BYS Interrupt Events: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

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Table 8-373. BSC_GLOBAL_CTRL

Address Offset	0x0000 0070		
Physical Address	0x5200 8070 0x5200 C070	**Instance**	BYS_B BYS_A
Description	Global control of the BSC pipe		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EN_GAMMA	EN_LSC

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	EN_GAMMA	Enable gamma correction 0x0: Disabled. The module is bypassed: PIXOUT=PIXIN 0x1: Enabled.	RW	0
0	EN_LSC	Enable lens shading correction 0x0: Disabled The module is bypassed: PIXOUT=PIXIN 0x1: Enabled	RW	0

Table 8-374. Register Call Summary for Register BSC_GLOBAL_CTRL

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

Table 8-375. BSC_LSC_OFT

Address Offset	0x0000 0074		
Physical Address	0x5200 8074 0x5200 C074	**Instance**	BYS_B BYS_A
Description	LSC OFT		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			VOFST													RESERVED			HOFST												

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	VOFST	Vertical offset	RW	0x0000
15:13	RESERVED		R	0x0
12:0	HOFST	Horizontal offset	RW	0x0000

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Table 8-376. Register Call Summary for Register BSC_LSC_OFT

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

Table 8-377. BSC_LSC_A1

Address Offset	0x0000 0078		
Physical Address	0x5200 8078 0x5200 C078	**Instance**	BYS_B BYS_A
Description	Linear coefficients		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VA1								RESERVED								HA1							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	VA1	A1 Vertical linear coefficient	RW	0x0000
15:13	RESERVED		R	0x0
12:0	HA1	A1 Horizontal linear coefficient	RW	0x0000

Table 8-378. Register Call Summary for Register BSC_LSC_A1

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

Table 8-379. BSC_LSC_A2

Address Offset	0x0000 007C		
Physical Address	0x5200 807C 0x5200 C07C	**Instance**	BYS_B BYS_A
Description	Quadratic coefficients		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VA2								RESERVED								HA2							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	VA2	A2 Vertical quadratic coefficient	RW	0x0000
15:13	RESERVED		R	0x0
12:0	HA2	A2 Horizontal quadratic coefficient	RW	0x0000

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Table 8-380. Register Call Summary for Register BSC_LSC_A2

ISS Interfaces
- ISS BYS Boundary Signal Calculator: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

Table 8-381. BSC_LSC_S

Address Offset	0x0000 0080		
Physical Address	0x5200 8080 0x5200 C080	**Instance**	BYS_B BYS_A
Description	Shift lenghts		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VS2				VS1				RESERVED								HS2				HS1			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:20	VS2	S2 Vertical quadratic shift length	RW	0x0
19:16	VS1	S1 Vertical linear shift length	RW	0x0
15:8	RESERVED		R	0x00
7:4	HS2	S2 Horizontal quadratic shift length	RW	0x0
3:0	HS1	S1 Horizontal linear shift length	RW	0x0

Table 8-382. Register Call Summary for Register BSC_LSC_S

ISS Interfaces
- ISS BYS Boundary Signal Calculator: [0] [1] [2] [3]
- ISS BYS Registers Shadowing: [4]
- ISS BYS Registers: [5]

Table 8-383. BSC_LSC_GAN_0X

Address Offset	0x0000 0084		
Physical Address	0x5200 8084 0x5200 C084	**Instance**	BYS_B BYS_A
Description	Gain Adjustments 0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GAN_01								RESERVED								GAN_00							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	GAN_01	Gain Adjustment 01	RW	0x00
15:8	RESERVED		R	0x00
7:0	GAN_00	Gain Adjustment 00	RW	0x00

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Table 8-384. Register Call Summary for Register BSC_LSC_GAN_0X

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

Table 8-385. BSC_LSC_GAN_1X

Address Offset	0x0000 008C		
Physical Address	0x5200 808C 0x5200 C08C	**Instance**	BYS_B BYS_A
Description	Gain Adjustments 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GAN_11								RESERVED								GAN_10							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	GAN_11	Gain Adjustment 11	RW	0x00
15:8	RESERVED		R	0x00
7:0	GAN_10	Gain Adjustment 10	RW	0x00

Table 8-386. Register Call Summary for Register BSC_LSC_GAN_1X

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

Table 8-387. BSC_LSC_OFT_0X

Address Offset	0x0000 0090		
Physical Address	0x5200 8090 0x5200 C090	**Instance**	BYS_B BYS_A
Description	Total offsets 0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OFT_01								RESERVED								OFT_00							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	OFT_01	Total Offset for 01 Valid range = -4096..+4095	RW	0x0000
15:14	RESERVED		R	0x0
13:0	OFT_00	Total Offset for 00 Valid range = -4096..+4095	RW	0x0000

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Table 8-388. Register Call Summary for Register BSC_LSC_OFT_0X

ISS Interfaces
- ISS BYS Boundary Signal Calculator: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

Table 8-389. BSC_LSC_OFT_1X

Address Offset	0x0000 0094		
Physical Address	0x5200 8094 0x5200 C094	**Instance**	BYS_B BYS_A
Description	Total offsets 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OFT_11								RESERVED								OFT_10							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	OFT_11	Total Offset for 11 Valid range = -4096..+4095	RW	0x0000
15:14	RESERVED		R	0x0
13:0	OFT_10	Total Offset for 10 Valid range = -4096..+4095	RW	0x0000

Table 8-390. Register Call Summary for Register BSC_LSC_OFT_1X

ISS Interfaces
- ISS BYS Boundary Signal Calculator: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

Table 8-391. BSC_LSC_SHF

Address Offset	0x0000 0098		
Physical Address	0x5200 8098 0x5200 C098	**Instance**	BYS_B BYS_A
Description	S0 Gain Shift Length		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												VAL			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	VAL	LSC SHF	RW	0x0

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Table 8-392. Register Call Summary for Register BSC_LSC_SHF

ISS Interfaces
- ISS BYS Boundary Signal Calculator: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

Table 8-393. BSC_LSC_MAX

Address Offset	0x0000 009C		
Physical Address	0x5200 809C 0x5200 C09C	**Instance**	BYS_B BYS_A
Description	Gain Maximum Value		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VAL							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8:0	VAL	LSC MAX	RW	0x000

Table 8-394. Register Call Summary for Register BSC_LSC_MAX

ISS Interfaces
- ISS BYS Boundary Signal Calculator: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

Table 8-395. BSC_GAMMA_POS01

Address Offset	0x0000 00A0		
Physical Address	0x5200 80A0 0x5200 C0A0	**Instance**	BYS_B BYS_A
Description	Pixel positions		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POS1								RESERVED				POS0											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	POS1	Second segment position parameter	RW	0x000
15:12	RESERVED		R	0x0
11:0	POS0	First segment position parameter	R	0x000

Table 8-396. Register Call Summary for Register BSC_GAMMA_POS01

ISS Interfaces
- ISS BYS Boundary Signal Calculator: [0] [1]
- ISS BYS Registers Shadowing: [2]
- ISS BYS Registers: [3]

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Table 8-397. BSC_GAMMA_POS23

Address Offset	0x0000 00A4		
Physical Address	0x5200 80A4 0x5200 C0A4	**Instance**	BYS_B BYS_A
Description	Pixel positions		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POS3								RESERVED								POS2							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	POS3	Fourth segment position parameter	RW	0x000
15:12	RESERVED		R	0x0
11:0	POS2	Third segment position parameter	RW	0x000

Table 8-398. Register Call Summary for Register BSC_GAMMA_POS23

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

Table 8-399. BSC_GAMMA_OFT01

Address Offset	0x0000 00B0		
Physical Address	0x5200 80B0 0x5200 C0B0	**Instance**	BYS_B BYS_A
Description	Pixel offsets		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OFT1								RESERVED								OFT0							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	OFT1	Pixel offset for POS1	RW	0x000
15:12	RESERVED		R	0x0
11:0	OFT0	Pixel offset for POS0	RW	0x000

Table 8-400. Register Call Summary for Register BSC_GAMMA_OFT01

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

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Table 8-401. BSC_GAMMA_OFT23

Address Offset	0x0000 00B4		
Physical Address	0x5200 80B4 0x5200 C0B4	**Instance**	BYS_B BYS_A
Description	Pixel offsets		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OFT3								RESERVED								OFT2							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	OFT3	Pixel offset for POS3	RW	0x000
15:12	RESERVED		R	0x0
11:0	OFT2	Pixel offset for POS2	RW	0x000

Table 8-402. Register Call Summary for Register BSC_GAMMA_OFT23

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

Table 8-403. BSC_GAMMA_SLP01

Address Offset	0x0000 00C0		
Physical Address	0x5200 80C0 0x5200 C0C0	**Instance**	BYS_B BYS_A
Description	Pixel slopes		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SLP1								RESERVED								SLP0							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	SLP1	Pixel slope for POS1	RW	0x000
15:12	RESERVED		R	0x0
11:0	SLP0	Pixel slope for POS0	RW	0x000

Table 8-404. Register Call Summary for Register BSC_GAMMA_SLP01

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

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Table 8-405. BSC_GAMMA_SLP23

Address Offset	0x0000 00C4		
Physical Address	0x5200 80C4 0x5200 C0C4	**Instance**	BYS_B BYS_A
Description	Pixel slopes		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SLP3								RESERVED				SLP2											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	SLP3	Pixel slope for POS3	RW	0x000
15:12	RESERVED		R	0x0
11:0	SLP2	Pixel slope for POS2	RW	0x000

Table 8-406. Register Call Summary for Register BSC_GAMMA_SLP23

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0]
- ISS BYS Registers Shadowing: [1]
- ISS BYS Registers: [2]

Table 8-407. BSC_PAGE

Address Offset	0x0000 00C8		
Physical Address	0x5200 80C8 0x5200 C0C8	**Instance**	BYS_B BYS_A
Description	Controls access to BSC memories. Only 512 accumulator values per pipe are mapped into the addres space. The page ID is automatically incremented when the last location of a page is accesses. Alternatively, software directly chose the page number for each accumulator.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RESERVED				RESERVED				ACC1				ACC0				RESERVED	RESERVED	AUTOINCR1	AUTOINCR0

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:16	RESERVED		R	0x0
15:12	RESERVED		R	0x0
11:8	ACC1	Page for accumulator pipe #1	RW	0x0
7:4	ACC0	Page for accumulator pipe #0	RW	0x0
3	RESERVED		R	0
2	RESERVED		R	0
1	AUTOINCR1	Enables automatic page increment for the corresponding accumulator pipe #1 when the last location has been accessed 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	AUTOINCR0	Enables automatic page increment for the corresponding accumulator pipe #0 when the last location has been accessed 0x0: Disabled 0x1: Enabled	RW	0

Table 8-408. Register Call Summary for Register BSC_PAGE

ISS Interfaces
- ISS BYS DMA Requests: [0] [1] [2]
- ISS BYS Registers: [3]

Table 8-409. BSC_DMA_REQS

Address Offset	0x0000 00CC		
Physical Address	0x5200 80CC 0x5200 C0CC	**Instance**	BYS_B BYS_A
Description	Number of DMA requests to generate per pipeline minus 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				RESERVED				ACC1				ACC0			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:8	RESERVED		R	0x0
7:4	ACC1	Number of DMA requests for accumulator pipe #1	RW	0x0
3:0	ACC0	Number of DMA requests for accumulator pipe #0	RW	0x0

Table 8-410. Register Call Summary for Register BSC_DMA_REQS

ISS Interfaces
- ISS BYS DMA Requests: [0] [1]
- ISS BYS Boundary Signal Calculator: [2] [3] [4] [5]
- ISS BYS Registers: [6]

Table 8-411. BSC_CTRL_i

Address Offset	0x0000 0100 + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x5200 8100 + (0x20 * i) 0x5200 C100 + (0x20 * i)	**Instance**	BYS_B BYS_A
Description	Global control of the BSC module		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					SHF			RESERVED					NOINIT	SEL	EN

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x00 0000
10:8	SHF	The down shift value before accumulation. Range: 0-7	RW	0x0

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Bits	Field Name	Description	Type	Reset
7:3	RESERVED		R	0x00
2	NOINIT	Don't initialize accumulators when set. 0x0: Reset accumulators every frame 0x1: Don't reset accumulators. Add new data to data already in the memory	RW	0
1	SEL	Select accumulator organization in the memory 0x0: Column vector mode. ID = floor((h-HSKIP)/HSIZE)+HCNT*floor((v-VSKIP)/VSIZE) 0x1: Row vector mode ID = VCNT*floor((h-HSKIP)/HSIZE)+floor((v-VSKIP)/VSIZE)	RW	0
0	EN	Enable statistics collection 0x0: Disabled. No statistics are collected for this pipeline. The memory content is left unchanged. 0x1: Enabled.	RW	0

Table 8-412. Register Call Summary for Register BSC_CTRL_i

ISS Interfaces
- ISS BYS Boundary Signal Calculator: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- ISS BYS Registers Shadowing: [11]
- ISS BYS Registers: [12] [13] [14]

Table 8-413. BSC_SKIP_i

Address Offset	0x0000 0104 + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x5200 8104 + (0x20 * i) 0x5200 C104 + (0x20 * i)	**Instance**	BYS_B BYS_A
Description	Position of the top left corner analyzed by BSC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			VSKIP													RESERVED			HSKIP												

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	VSKIP	The V position of left-top of the sampled frame Valid range: 0.. (BYS_HL_HWINFO[27:15] MAX_OHEIGHT - 1)	RW	0x0000
15:13	RESERVED		R	0x0
12:0	HSKIP	The H position of left-top of the sampled frame Valid range: 0.. (BYS_HL_HWINFO[14:2] MAX_OWIDTH - 1)	RW	0x0000

Table 8-414. Register Call Summary for Register BSC_SKIP_i

ISS Interfaces
- ISS BYS Video Ports: [0] [1]
- ISS BYS Boundary Signal Calculator: [2] [3] [4] [5] [6] [7]
- ISS BYS Registers Shadowing: [8]
- ISS BYS Registers: [9]

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Table 8-415. BSC_SIZE_i

Address Offset	0x0000 0108 + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x5200 8108 + (0x20 * i) 0x5200 C108 + (0x20 * i)	**Instance**	BYS_B BYS_A
Description	Bin size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VSIZE								RESERVED								HSIZE							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	VSIZE	The height of the rectangle Valid range: 1.. BYS_HL_HWINFO[27:15] MAX_OHEIGHT	RW	0x0000
15:13	RESERVED		R	0x0
12:0	HSIZE	The width of the rectangle Valid range: If BSC_CTRL_i[1] SEL = 0: 1.. BYS_HL_HWINFO[14:2] MAX_OWIDTH If BSC_CTRL_i[1] SEL = 1: 2.. BYS_HL_HWINFO[14:2] MAX_OWIDTH	RW	0x0000

Table 8-416. Register Call Summary for Register BSC_SIZE_i

ISS Interfaces

- ISS BYS Boundary Signal Calculator: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS BYS Registers Shadowing: [8]
- ISS BYS Registers: [9]

Table 8-417. BSC_CNT_i

Address Offset	0x0000 010C + (0x20 * i)	**Index**	i = 0 to 1
Physical Address	0x5200 810C + (0x20 * i) 0x5200 C10C + (0x20 * i)	**Instance**	BYS_B BYS_A
Description	Number of bins in each direction software must ensure that HCNT*VCNT <= BYS_HL_HWINFO2[] ACCi_COUNT, where i = 0 to 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VCNT								RESERVED								HCNT							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	VCNT	Number of bins in the vertical direction (the vertical number of rectangles in the frame) Valid range: 1.. BYS_HL_HWINFO[27:15] MAX_OHEIGHT	RW	0x0000
15:13	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
12:0	HCNT	Number of bins in the horizontal direction (the horizontal number of rectangles in the frame) Valid range: 1.. BYS_HL_HWINFO[14:2] MAX_OWIDTH	RW	0x0000

Table 8-418. Register Call Summary for Register BSC_CNT_i

ISS Interfaces

- ISS BYS Video Ports: [0] [1]
- ISS BYS Boundary Signal Calculator: [2] [3] [4] [5] [6]
- ISS BYS Registers Shadowing: [7]
- ISS BYS Registers: [8]

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8.3 ISS ISP

This section describes the image signal processor.

8.3.1 ISS ISP Overview

The image signal processor (ISP) is part of the image subsystem (ISS) of the device and is a key component for imaging and video applications. It describes all ISP modules in the multimedia device; that is, the video port (VP), image pipe interface (IPIPEIF), image pipe module (IPIPE), resizer (RSZ), hardware 3A (H3A), image sensor interface (ISIF), and buffer logic (BL). For better understanding, see the first top-level ISS diagram and feature list in Section 8.1, *ISS Overview*.

8.3.1.1 ISS ISP Features

The video-processing hardware removes the need for expensive camera modules to perform processing functions. The ISS can support the following features:

- On-the-fly or memory-to-memory processing
- Up to 304-MHz pixel throughput
- Statistic data collection:
  - On-the-fly or memory-to-memory operation
  - Data collection for auto exposure
  - Data collection for auto white balance
  - Data collection for auto focus
  - Boundary signal calculation for video stabilization
- IPIPE front end: RAW data processing:
  - On-the-fly or memory-to-memory processing
  - 16-bit-wide RAW Bayer data path between image and sensor linearization module
  - 12-bit-wide RAW Bayer data path between sensor linearization module and gamma correction module. Gamma correction module outputs 10-bit data.
  - Programmable Bayer RGB positions
  - Sensor data linearization for dynamic range extension
  - Programmable 2D lens shading compensation (LSC) correction
  - Per-pixel gain and offset control
  - Black level compensation
  - Boxcar filter
  - Data collection for histogram generation
  - Defect pixel correction (LUT_DPC) with look-up table (LUT)
  - Defect pixel correction (OTF_DPC) with on-the-fly detection and correction
  - 2D noise filtering
  - Green imbalance correction (GIC)
  - Digital gains and offset
  - 8- to 10-bit A-law decompression and 10- to 8-bit A-law compression
- IPIPE back end: RGB and YUV data processing:
  - RGB-to-RGB color correction
  - Gamma correction (GC)
  - RGB -> YUV4:2:2: Color conversion, cosited Chroma filtering and downsampling
  - 2D edge enhancement (EE)
  - 3D LUT for color correction
  - False Chroma suppression (FCS)
- Two resizers:

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- Performance: input and output rates up to 304 MPix/s
- YUV4:2:2 to RGB56, ARGB888, YUV4:2:2, and YUV4:2:0 data output
- YUV4:2:0 to YUV4:2:0 data output
- RAW to RAW data output
- Range from x1/4096 to x20. Supports memory-to-memory rescaling.

The ISP comprises the following modules:

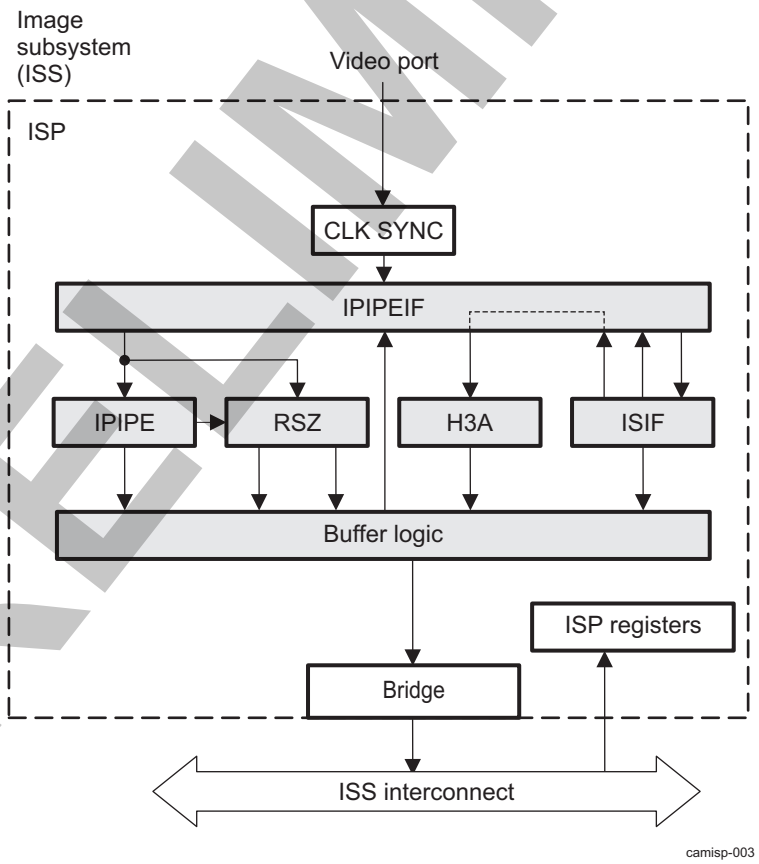
- IPIPE interface (IPIPEIF)
- Image sensor interface (ISIF) accelerator
- Auto exposure, auto white balance, and auto focus engine (H3A)
- Image pipe accelerator (IPIPE)
- Two resizer (RSZ) accelerators
- Buffer logic (BL): Receives module requests, performs arbitration, and creates read/write bursts to the memory subsystem

8.3.1.2 ISS ISP Block Diagram

Figure 8-120 is the ISP top-level block diagram. The ISS supports five simultaneous pixel flows (CCP2, CSI2_A, CSI2_B, CSI2_C and parallel interface [CPI]), but only one of them at a time can use the video-processing hardware; the others can go directly to memory (CPI must always use ISP).

The ISP 128-bit master port and 32-bit slave port are connected to the level 3 interconnect (L3_MAIN).

Figure 8-120. ISS ISP Block Diagram



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8.3.2 ISS ISP Integration

This section describes the integration of the ISP modules in the ISP and includes information about clocks, resets, and hardware requests.

The ISP is part of the ISS of the device and is a key component for imaging and video applications such as camera viewfinder, video record, and still image capture.

The ISS is coupled with a low-interrupt-latency imaging processor unit subsystem (Cortex-M4 IPU) running a real-time operating system to reach optimal performance. Primarily, the IPU can quickly change the ISS configuration during frame blanking periods and run some sequencing tasks. The ISS can also be configured using the main micro-processor unit subsystem (Cortex-A15 MPU) or the system DMA controller (DMA_SYSTEM). Typically, the MPU can run some less latency-sensitive tasks, and the DMA_SYSTEM can be used to transfer large configuration tables used by the ISS (for example, Gamma tables).

8.3.2.1 ISS ISP PRCM Interface

The ISP and its internal modules, as integrated in the ISS, use the same power and clock management details. See Section 8.1.2, *ISS Functional Description*, for the ISP top-level power, reset, and clock management (PRCM) interface.

8.3.2.1.1 ISS ISP Clocks

The PRCM module, through the local power and clock management inside the ISS, provides a unique PCLK that can be enabled from the ISP5_CTRL register.

The modules inside the ISP require three clocks:

- PCLK: This clock is asynchronous to the other clocks. It is provided by the module sending the data to the IPIPEIF module on the VP. The frequency is up to 304 MHz.
- ISP_FCLK: This clock is sourced from ISS_MAIN_FCLK and is synchronous with the configuration clock domain. This is the clock used for the MTC interface. The frequency is up to 304 MHz.
- GCK_MMR: This is the clock for the configuration bus. It is created from the ISP_FCLK and runs at half the speed of the ISP_FCLK. The frequency is up to 152 MHz.

8.3.2.1.2 ISS ISP Reset

The ISP supports global software reset along with internal hardware reset, if needed.

Software reset is done through the ISP5_SYSCONFIG[1] SOFTRESET bit. Before issuing a software reset, the ISP must be in standby mode. The following must be done:

1. Ensure that the interfaces are stopped from sending data and/or the ISP modules are disabled. Before reset, the last interrupt triggered by the ISP when the frame processing completes is RSZ_INT_DMA. RSZ_INT_DMA must be used to enable clean termination of the processing. Software must wait a few hundred cycles to trigger a soft reset after RSZ_INT_DMA is asserted; this is to ensure that the BL is completely drained.
2. Ensure that ISP5_SYSCONFIG[5:4] STANDBYMODE = 2 (smart standby). Set the ISP5_CTRL[24] MSTANDBY bit to 1 and poll for ISP5_CTRL[20] MSTANDBY_WAIT = 1. Then, the soft reset can be applied (ISP5_SYSCONFIG[1] SOFTRESET = 1).

In case an ISP overflow or underflow event happens (for example, RSZ_FIFO_OVF, ISIF_OVF, etc.), it is not sufficient to reset the ISP. In that case a reset must occur at the ISS level.

8.3.2.2 ISS ISP Interrupt Tree

There are four ISP output interrupt lines that are mapped to the ISS top interrupt request (IRQ) merger (for more information, see Section 8.1.2.1.1, *ISS Interrupt Merger*). Table 8-419 summarizes the ISP submodule interrupt events that can be mapped to the four ISP interrupt lines. An interrupt event can be enabled on any of the four interrupt lines through the ISP5_IRQENABLE_SET_i and ISP5_IRQENABLE_SET2_i registers (i = 0 to 3, one register per interrupt line). Each event must be enabled on only one interrupt line.

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Table 8-419. ISS ISP Interrupt Tree Table

Register	Module	Destination	Comments
ISP5_IRQENABLE_SET_i[9] IPIPEIF_IRQ	IPIPEIF	ISP to ISS merger four IRQ lines	See Section 8.3.2.3.1.
ISP5_IRQENABLE_SET2_i[1] IPIPEIF_UDF			
ISP5_IRQENABLE_SET_i[29] IPIPE_INT_DPC_RNEW1	IPIPE		See Section 8.3.2.4.1.
ISP5_IRQENABLE_SET_i[28] IPIPE_INT_DPC_RNEW0			
ISP5_IRQENABLE_SET_i[27] IPIPE_INT_DPC_INI			
ISP5_IRQENABLE_SET_i[8] IPIPE_INT_HST			
ISP5_IRQENABLE_SET_i[7] IPIPE_INT_BSC			
ISP5_IRQENABLE_SET_i[6] IPIPE_INT_DMA			
ISP5_IRQENABLE_SET_i[5] IPIPE_INT_LAST_PIX			
ISP5_IRQENABLE_SET_i[4] IPIPE_INT_REG			
ISP5_IRQENABLE_SET_i[25] IPIPE_INT_EOF			
ISP5_IRQENABLE_SET2_i[4] IPIPE_HST_ERR			
ISP5_IRQENABLE_SET2_i[2] IPIPE_BOXCAR_OVF			
ISP5_IRQENABLE_SET_i[12] H3A_INT	H3A		See Section 8.3.2.6.
ISP5_IRQENABLE_SET_i[24] H3A_INT_EOF			
ISP5_IRQENABLE_SET2_i[0] H3A_OVF			
ISP5_IRQENABLE_SET_i[23] RSZ_INT_EOF1	RSZ		See Section 8.3.2.5.2.
ISP5_IRQENABLE_SET_i[22] RSZ_INT_EOF0			
ISP5_IRQENABLE_SET_i[19] RSZ_FIFO_IN_BLK_ERR			
ISP5_IRQENABLE_SET_i[18] RSZ_FIFO_OVF			
ISP5_IRQENABLE_SET_i[17] RSZ_INT_CYC_RZB			
ISP5_IRQENABLE_SET_i[16] RSZ_INT_CYC_RZA			
ISP5_IRQENABLE_SET_i[15] RSZ_INT_DMA			
ISP5_IRQENABLE_SET_i[14] RSZ_INT_LAST_PIX			
ISP5_IRQENABLE_SET_i[13] RSZ_INT_REG			
ISP5_IRQENABLE_SET_i[3] ISIF_INT_3	ISIF		See Section 8.3.2.7.1.
ISP5_IRQENABLE_SET_i[2] ISIF_INT_2			
ISP5_IRQENABLE_SET_i[1] ISIF_INT_1			
ISP5_IRQENABLE_SET_i[0] ISIF_INT_0			
ISP5_IRQENABLE_SET2_i[3] ISIF_OVF			

8.3.2.3 ISS ISP IPIPEIF Integration

8.3.2.3.1 ISS ISP IPIPEIF Interrupts

The IPIPEIF module generates two interrupts:

- IPIPEIF_IRQ: This event is triggered to the BL module when a new frame starts (VS signal). The interrupt is active high and is asserted for one GCK_MMR clock cycle.
- IPIPEIF_UDF: Interrupt generated when an underflow occurs in the IPIPEIF module.

The interrupts are enabled from the ISP5_IRQENABLE_SET_i[9] IPIPEIF_IRQ and ISP5_IRQENABLE_SET2_i[1] IPIPEIF_UDF bits (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from the ISP is sent to the ISS top level, where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2,*ISS Functional Description*.

For additional information on IPIPEIF events see Section 8.3.3.2.15, *ISS ISP IPIPEIF Module Events and Status Checking*.

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8.3.2.4 ISS ISP IPIPE Integration

8.3.2.4.1 ISS ISP IPIPE Interrupts

IPIPE can generate several interrupts:

- IPIPE_INT_DPC_RNEW: This event is triggered when there is permission to initialize LUT-DPC table lines 0 and 1.
- IPIPE_INT_DPC_INI: This event is triggered when the defect pixel correction (DPC) table is initialized.
- IPIPE_INT_HST: This event is triggered when the histogram is done.
- IPIPE_INT_BSC: This event is triggered when boundary signal calculation is done.
- IPIPE_INT_DMA: This event is triggered when the boxcar SDRAM transfer is done. On this timing, IPIPE_INT_EOF is sent to the BL. This event is active high for one GCK_MMR clock cycle.
- IPIPE_INT_LAST_PIX: This event is triggered when the last pixel of a frame comes into IPIPE. This event is active high for one GCK_MMR clock cycle.
- IPIPE_INT_EOF: This event is triggered for end of frame.
- IPIPE_BOXCAR_OVF: This event is generated when an overflow occurs in the IPIPE-BOXCAR output buffer. The interrupt avoids polling the IPIPE_SRC_STA[0] VAL0 bit for errors. Overflow events are nonrecoverable at the ISP level and a soft reset is required at the ISS level.
- IPIPE_HST_ERR: This event is triggered when the MPU/IPU or system direct memory access controller (DMA_SYSTEM) is still reading the memory that is being used by the module. This is an indication that the read operation was not fast enough.

The interrupts are enabled from the ISP5_IRQENABLE_SET_i and ISP5_IRQENABLE_SET2_i registers (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from the ISP is sent to the ISS top level, where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2, *ISS Functional Description*.

8.3.2.4.2 ISS ISP DMA Requests

The ISP generally outputs four direct memory access (DMA) requests, which can be used to read or write memories inside the IPIPE module. These memories are:

- BSC memory: This memory must be read during a vertical blanking period. It is used by the video stabilization application.
- HIST memory: This memory must be read during a vertical blanking period. It is used by the 3A application. The HIST data is double-buffered from frame-to-frame. Software must select the memory that is to be used by setting the IPIPE_HST_TBL[0] SEL bit.
- GAMMA memory: This memory must be set during a vertical blanking period. The imaging application typically uses multiple gamma tables.
- DPC memory: This memory must be set during a frame acquisition. The memory is not big enough to store all faulty pixels for a given frame.

To generate the DMA requests, the following events must be used:

- The IPIPE_INT_BSC event is used to generate the DMA request for the BSC memory. It maps on DMA line 1, ISS_DREQ_1.
- The IPIPE_INT_HST event is used to generate the DMA request for the HIST memory. It maps on DMA line 2, ISS_DREQ_2. The HIST data is double-buffered from frame-to-frame. Software must select the memory that is to be used by setting the IPIPE_HST_TBL[0] SEL bit. When the DMA request is set, it is required to read 4 KiB from the ping buffer address (0x2000) or the pong buffer address (0x3000). Software must ensure that when one buffer is selected no other accesses (for example, IPU) occur in the other buffer.
- The IPIPE_INT_LAST_PIX event is used to generate the DMA request for the GAMMA memory. This same event can also be used to initialize the DPC LUT (not the preferred method; it is better to use IPIPE_INT_DPC_INI). Basically, when the last pixel is output from the IPIPE module, it is safe to modify the IPIPE memories. It maps on DMA line 4, ISS_DREQ_4.
- The IPIPE_INT_DPC_INI event signals that DPC table memory initialization can occur. IPIPE_INT_DPC_INI is used to generate two back-to-back DMA requests, the first one mapping on

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IPIPE_INT_DPC_RNEW0 and the second one mapping on IPIPE_INT_DPC_RNEW1. After initialization (steady state), the IPIPE_INT_DPC_RNEW0 and IPIPE_INT_DPC_RNEW1 events are used to generate the DMA request for the DPC LUT renewal. It maps on DMA line 3, ISS_DREQ_3. To select which event is used to initialize the DPC (IPIPE_INT_LAST_PIX or IPIPE_INT_DPC_INI), set the ISP5_CTRL[25] DPC_EVT_INI bit.

NOTE: The size of the DPC table in SDRAM must be a multiple of the number of DMA requests. It ensures that during burst capture mode the DMA always loads the correct data from frame-to-frame. The DMA automatically warps back to the start of the table after all expected DMA requests are received. There is a total of ceil(nb_faulty_pixel/128) + 2 DMA requests per frame when the IPIPE_INT_DPC_INI EVENT is used. Hence, the size of the DPC table in the SDRAM is (ceil(nb_faulty_pixel/128) + 2) × 128 × 32 bits.

NOTE: If DMA channels are not used but the MPU/IPU is used, an error check must be performed for IPIPE HST. See ISP5_CTRL[26] HST_RD_CHK for details.

The DMA request assertion and deassertion to the DMA_SYSTEM is automatic and no software intervention is needed. The ISP contains two registers (ISP5_DMAENABLE_SET and ISP5_DMAENABLE_CLR) that must be used to enable or disable generation of the DMA requests.

The DMA request deassertion is based on late deassertion; that is, the DMA request is disabled only when all the data corresponding to the transfer size have been read or written. To deassert the DMA request and generate the hw_eoi signal, hardware counts the number of 32-bit accesses that are done in the memory range of the corresponding DMA request through the ISP slave port. When the number of accesses corresponding to the DMA request is done, the DMA request is cleared. Multiple DMA requests can be active simultaneously.

Software must not attempt to read or write in the memory range of the DMA requests that are enabled because CPU accesses, instead of DMA_SYSTEM accesses, will be counted. Software can freely access ISP memories for which the DMA request is disabled, and can access registers while the DMA_SYSTEM performs the transfers.

8.3.2.5 ISS ISP RSZ Integration

8.3.2.5.1 ISS ISP RSZ PRCM Interface

8.3.2.5.1.1 ISS ISP RSZ Reset

The RSZ module has no stand-alone software reset. RSZ must be reset at the ISP level. See Section 8.3.2.1.2, *ISS ISP Reset*.

8.3.2.5.2 ISS ISP RSZ Interrupts

RSZ can generate several interrupts:

- RSZ_INT_EOF0: This event is triggered for end of frame.
- RSZ_INT_EOF1: This event is triggered for end of frame.
- RSZ_FIFO_IN_BLK_ERR: This event is triggered when the minimum vertical blanking period has not been respected, thus causing errors in the input data buffering submodule. This event is triggered when the RSZ_INT_REG event of frame N is triggered before RSZ_INT_DMA of frame N + 1. This event typically occurs at the transition between two frames because there is not enough vertical blanking between frames. Hardware cannot recover from this error. It requires a reset. It is a requirement that despite the error the RSZ module must finish correctly: ongoing requests are completed and further requests are blocked.
- RSZ_FIFO_OVF: This event typically occurs while processing a frame, because the VP pixel clock is too high. Because hardware cannot recover from this error, a reset is required. It is a requirement that despite the error the RSZ module must finish correctly: ongoing requests are completed and further requests are blocked.

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This event signifies overflow in two different scenarios:

- In Bypass or Operating (normal/downscale) modes, the RSZ_FIFO_OVF event is triggered when an overflow occurs in the input circular data buffer. The rsz_stall_input signal can be asserted by programming appropriate thresholds to prevent input FIFO overflow.
- In Pass-through mode, the RSZ_FIFO_OVF event is triggered when an overflow occurs in the output MTC buffer. There is no hardware mechanism to prevent overflow in Pass-through mode.

- RSZ_INT_CYC_RZA/RSZ_INT_CYC_RZB: This event is triggered as circular interrupt every time that RSZ_IRQ_RZA/RSZ_IRQ_RZB output lines are written to the RZA_SDR_Y/RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value must be such that the circular buffer vertical size (set by the RZBA_SDR_Y_PTR_E/RZBB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZA/RSZ_IRQ_RZA.
- RSZ_INT_DMA: This event is triggered when the last EOF (of the two MTC interfaces) is sent to the BL and the RSZ core returns to idle. This event is active high for one GCK_MMR clock cycle.
- RSZ_INT_LAST_PIX: This event is triggered when the last pixel of the valid area is received. This event is active high for one GCK_MMR clock cycle.
- RSZ_INT_REG: This event is triggered when the new value of the shadowed registers, if updated, takes effect on the next RSZ_INT_REG event. Then again, shadowed registers can be updated for the next frame after the RSZ_INT_REG event is triggered. This event is active high for one GCK_MMR clock cycle.

The interrupts are enabled from the ISP5_IRQENABLE_SET_i register (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from the ISP is sent to the ISS top level, where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2, *ISS Functional Description*.

8.3.2.6 ISS ISP H3A Integration

8.3.2.6.1 ISS ISP H3A Interrupts

H3A can generate the following interrupts:

- H3A_INT: This event is triggered at the end of the last window or last paxel, whichever completes last. This always triggers at the same time as H3A_INT_EOF.
- H3A_INT_EOF: This event is triggered and generated at the end of the last window. This event is active high for one GCK_MMR clock cycle.
- H3A_OVF: This interrupt is generated when an overflow happens in the H3A output buffer. The interrupt avoids polling the H3A_PCR[21] OVF bit for errors. Overflow events are nonrecoverable at the ISP level and a soft reset is required at the ISS level. The event is active high for one GCK_MMR clock cycle.

The interrupts are enabled from ISP5_IRQENABLE_SET_i and ISP5_IRQENABLE_SET2_i (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from the ISP is sent to the ISS top level, where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2, *ISS Functional Description*.

8.3.2.7 ISS ISP ISIF Integration

8.3.2.7.1 ISS ISP ISIF Interrupts

The ISIF can generate several interrupts:

- ISIF_INT_0: This event is triggered when the VD0 interrupt on line 0 is configured. The VD0 interrupt can be configured based on the VD position. It is asserted after receiving the number of horizontal lines (horizontal pulse signals) set in VDINT0. For more information, see Section 8.3.3.6.19.1.
- ISIF_INT_1: This event is triggered when the VD1 interrupt on line 1 is configured. The VD1 interrupt can be configured based on the VD position. It is asserted after receiving the number of horizontal lines (horizontal pulse signals) set in VDINT1. For more information, see Section 8.3.3.6.19.1.
- ISIF_INT_2: This event is triggered when the VD2 interrupt on line 2 is configured. The VD2 interrupt can be configured based on the VD position. It is asserted after receiving the number of horizontal

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lines (horizontal pulse signals) set in VDINT2. SFor more information, see Section 8.3.3.6.19.1.

- ISIF_INT_3: This event is triggered LSC interrupt is an interrupt issued by the 2D-LSC block. For more information, see Section 8.3.3.6.10.1.5.
- ISIF_OVF: This Interrupt is generated when an overflow happens in the ISIF module. The interrupt avoids polling the ISIF_MODESET[11] OVF bit for errors.

The interrupts are enabled from the ISP5_IRQENABLE_SET_i and ISP5_IRQENABLE_SET2_i registers (where i = 0 to 3 for the line that will be mapped to the four lines of the ISP). Then, each line from ISP is sent to the ISS top level where it is muxed with other ISS modules for a total output of six interrupt lines. See Section 8.1.2, *ISS Functional Description*.

8.3.2.8 ISS ISP BL Integration

See Section 8.3.2, *ISS ISP Integration*.

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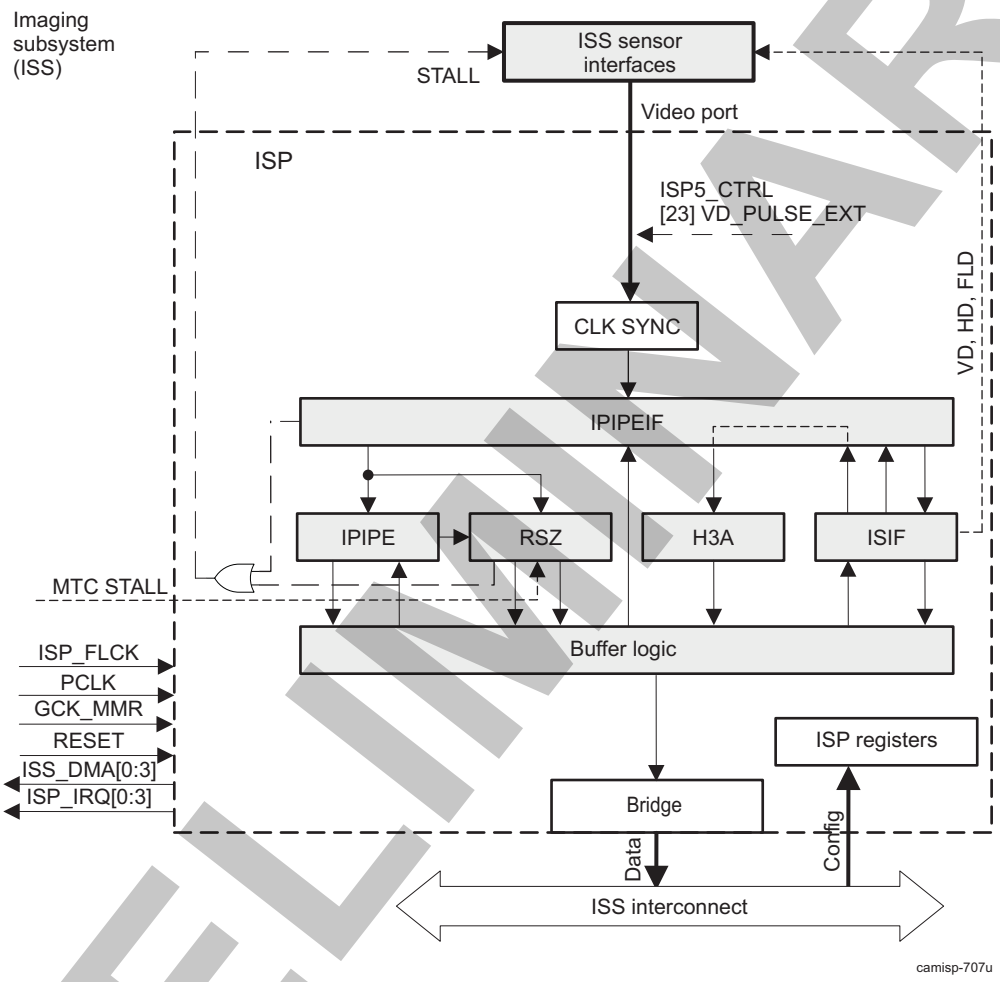
8.3.3 ISS ISP Functional Description

The functionality of the ISP is part of the overall performance of the ISS. For the top-level ISS diagram with ISP inside and for a features list, see Section 8.1, *ISS Overview*. Figure 8-121 is an overview of the ISP module. It outputs DMA and interrupt requests, has clocks coming in, and a stall signal to the CCP2 interface receiver from the resizer. It also shows the top-level configuration for input to IPIPEIF. For the scaled-in functional details of each submodule inside the ISP, see its functional description section.

Figure 8-121. ISS ISP High-Level Diagram



8.3.3.1 ISS ISP VP Functional Description

8.3.3.1.1 ISS ISP VP Overview

The VP supports a parallel interface that is used for interfacing with image sensors. The ISP VP can transport 8- to 16-bit RAW data and 8-/16-bit YCbCr data.

Figure 8-122 shows the VP module connections to other submodules of the ISP.

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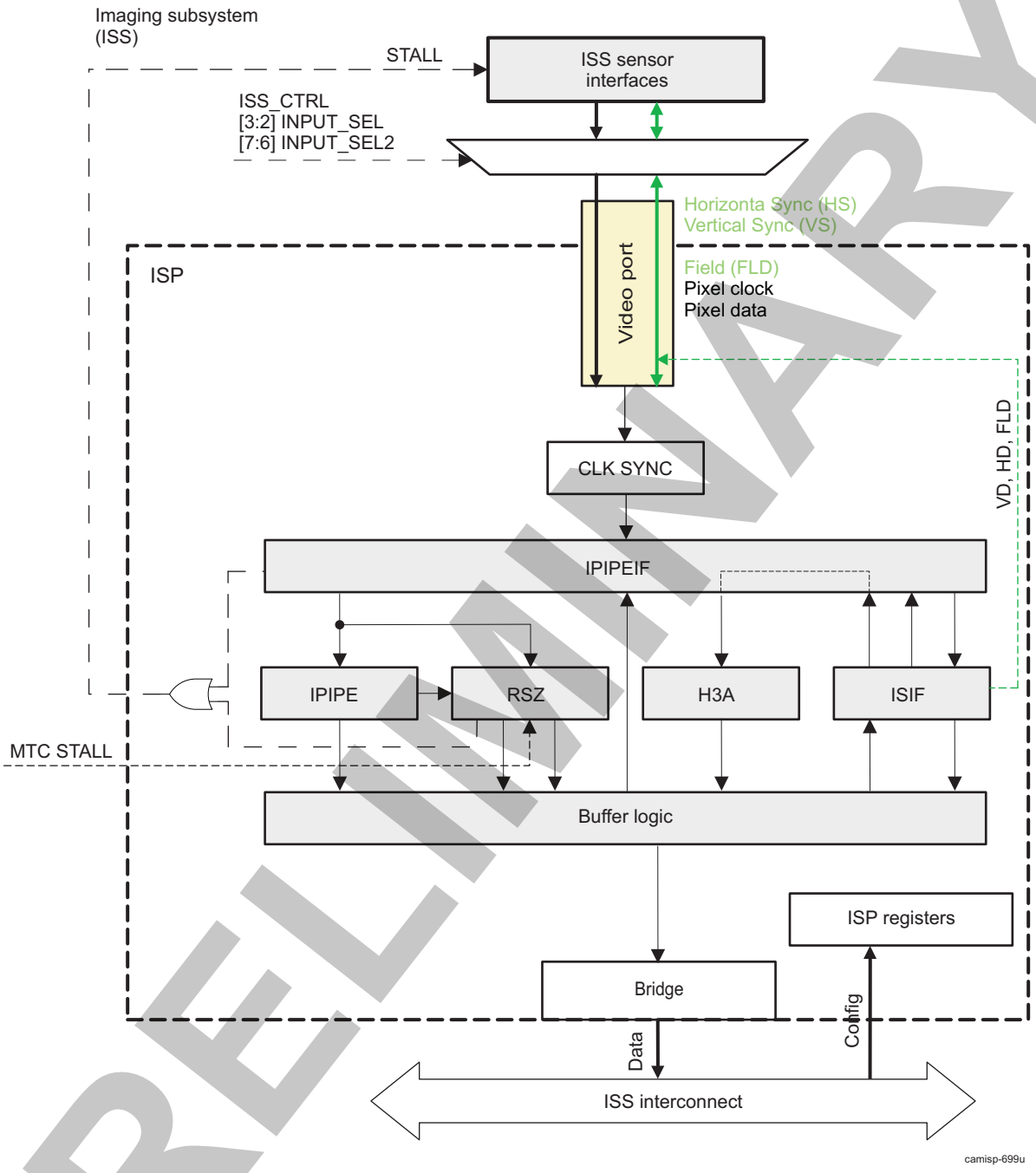
Figure 8-122. ISS ISP VP High-Level Diagram



8.3.3.1.2 ISS ISP VP Data Formats

The VP can be used to connect external camera receivers to the ISS. Data paths inside the ISP hardware depend on the image format sourced by the sensor (RAW RGB, YUV4:2:2, JPEG, etc.). Table 8-420 shows how the CCP2/CSI2 modules are connected to the VP in function of the image format.

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Table 8-420. ISS ISP VP Format Mapping

Source		Format	Connected to																ISIF	Data Provided to ISIF Linearization Engine															
CCP2	CSI2		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	GWDI	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	RAW16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
X	X	RAW14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0
			0	0	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	1	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0
X	X	RAW12	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0
			0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	1	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0
			R11	R10	R9	R8	R7	R5	R5	R4	R3	R2	R1	R0	0	0	0	0	2	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0
X	X	RAW10	0	0	0	0	0	0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0
			0	0	0	0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0
			0	0	R9	R8	R7	R5	R5	R4	R3	R2	R1	R0	0	0	0	0	2	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0
			R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	3	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0
X	X	RAW8								R8	R7	R6	R5	R4	R3	R2	R1	R0	0	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
									R7	R6	R5	R4	R3	R2	R1	R0			1	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
							R7	R6	R5	R4	R3	R2	R1	R0					2	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
					R7	R6	R5	R4	R3	R2	R1	R0							3	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
			R7	R5	R5	R4	R3	R2	R1	R0									4	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0	0	0	0	0
		YUV 16-bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	C7	C6	C5	C4	C3	C2	C1	C0	0																
		YUV 8-bit									YC7	YC6	YC5	YC4	YC3	YC2	YC1	YC0	0																

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8.3.3.1.3 ISS ISP VP Top-Level Communication With CCP2 RX and CSI2 RX

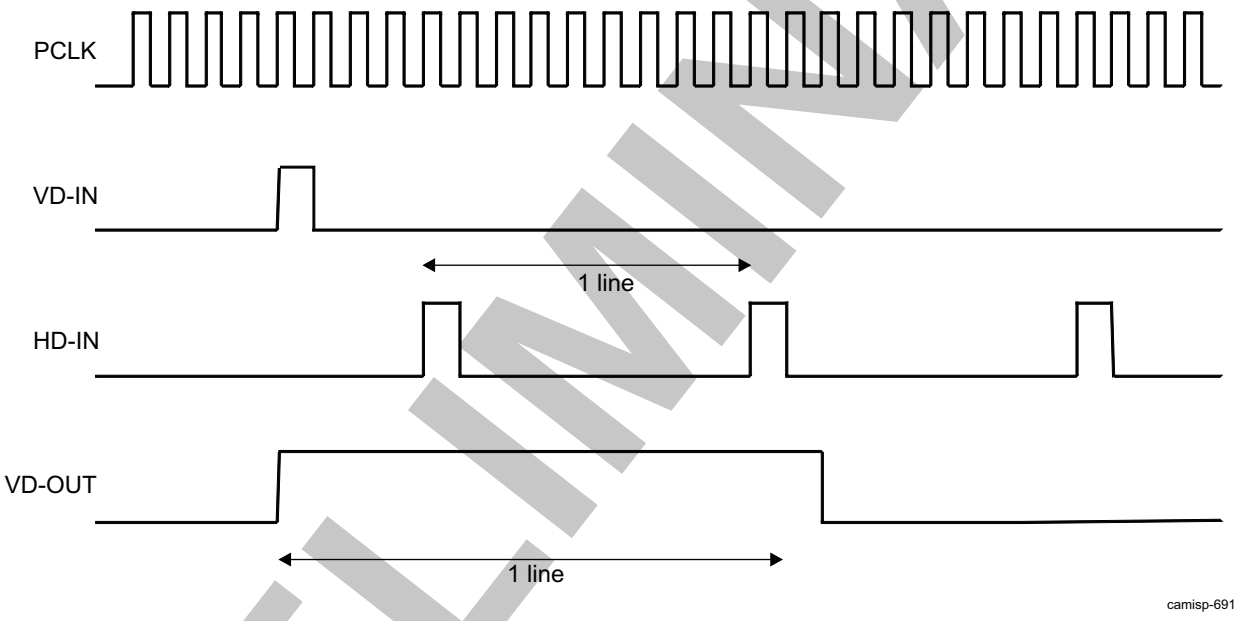
At the ISS level, the VP is connected to the VP of the CCP2 RX and CSI2 RX interface modules. The selection, which interface VP is connected to the ISP is done on ISS top level through ISS_CTRL[3:2] INPUT_SEL and [7:6] INPUT_SEL2 register bit fields.

VP implementation differences force the introduction of a bridge between the CCP2 RX/CIS2 RX modules and the VP. The role of the bridge is to perform VD pulse extension. The CCP2 RX module assumes that the VD signal is active for at least one pixel clock cycle, and the CSI2 RX module assumes that the VD signal is asserted for four pixel clock cycles. However, the ISP assumes that the VD pulse is active on at least one line.

Figure 8-123 shows how the VD pulse extension works. Assume that VD-IN is the VD signal at the input of the pulse extension bridge, and VD-OUT is the VD signal at the output of the pulse extension bridge.

VD-OUT is asserted at the same time as VD-IN. VD-OUT is kept high until one full line is received. A line is delimited by two rising edges of the HD signal. VD-OUT is deasserted on the next cycle after the falling edge of the HD signal.

Figure 8-123. ISS ISP VP VD Pulse



The ISP5_CTRL[23] VD_PULSE_EXT bit controls whether the VD extension bridge is enabled or disabled. By default, the bridge is enabled. When the bridge is disabled, the VD pulse must be unmodified: VD-OUT = VD-IN. At the ISS level, it is expected that ISP5_CTRL[23] VD_PULSE_EXT = 1 when the VP gets data from the CSI2 RX modules and ISP5_CTRL[23] VD_PULSE_EXT = 0 when the VP gets data from the parallel interface or the CCP2 RX module.

CAUTION

A minimum of four lines per frame is required on the VP when the VD pulse extension bridge is enabled; therefore, the VD extension bridge is not functional if a 1-/2-/3-line frame is sent to the VP.

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8.3.3.1.4 ISS ISP VP Pixel Clock Inversion

The ISP always uses the rising edge of the pixel clock to sample the pixel data. The ISP provides the capability to invert the pixel clock so it can shift the resampling of a pixel clock period by half. This is controlled by the ISP5_CTRL[22] PCLK_INV bit. By default, the inversion is disabled. The pixel clock must be disabled at ISS level before setting the PCLK_INV bit to 0x1. This can be done through the proper ISS_CLKCTRL[] VPORTx_CLK register bit on ISS top level, depending on the interface (CCP2 or CSI2) that is sending data on the ISP video port.

The 4 bits in Table 8-421 are resynchronized from the GCK_MMR clock domain to the PCLK clock domain. There must be at least three clock cycles between the time these bits are modified and the HD/VD pulse for start of frame comes.

Table 8-421. ISS ISP VP GCK_MMR to PCLK Clock Resynchronization

Module	Register	Bit Field
ISP	ISP5_CTRL	VD_PULSE_EXT
ISIF	ISIF_MODESET	HDVDD
ISIF	ISIF_MODESET	FIDD
ISP	ISP5_CTRL	ISIF_CLK_ENABLE

8.3.3.2 ISS ISP IPIPEIF Functional Description

8.3.3.2.1 ISS ISP IPIPEIF Overview

The IPIPEIF module provides data and synchronization signals (HD, VD) for the ISIF, IPIPE, RSZ, and H3A modules. The data source of this module is the VP, ISIF, or SDRAM using BL, and the selected data is output to ISIF, IPIPE, H3A, and RSZ. This module supports:

- Up to 16-bpp data on the VP
- Up to 304-MHz pixel clock on the VP, up to 8K × 8K imaging resolution
- RAW and YUV data formats on the VP and BL ports
- Dark-frame subtract of 8-bit RAW image stored in SDRAM from image from VP
- Dark-frame subtract of 8-bit RAW image stored in SDRAM from image from ISIF
- Dark-frame subtract of 8-bit RAW image from VP from image read from SDRAM through the BL
- Simple defect correction to prevent the subtraction of defect pixels
- 8-10, 8-12 DPCM of 10-8, 12-8 DPCM compressed data in SDRAM
- Simple and advanced DPCM predictor
- Inverse A-Law decompression of RAW data 10-8 A-Law compressed from SDRAM
- 8-bit, 12-bit unpacking of 8-bit,12-bit packed SDRAM data
- Gain multiply for output data to the IPIPE module
- Horizontal Bayer rescaler in the data paths to the IPIPE and H3A modules: Supports (1, 2, 1) averager filter and supports horizontal pixel decimation
- Data rate control when reading data from SDRAM: Fraction clock divider
- (1, 2, 1) averager filter and supports horizontal pixel decimation in the data path to the IPIPE for YUV data.

Figure 8-124 show the IPIPEIF module connections to other submodules of the ISP.

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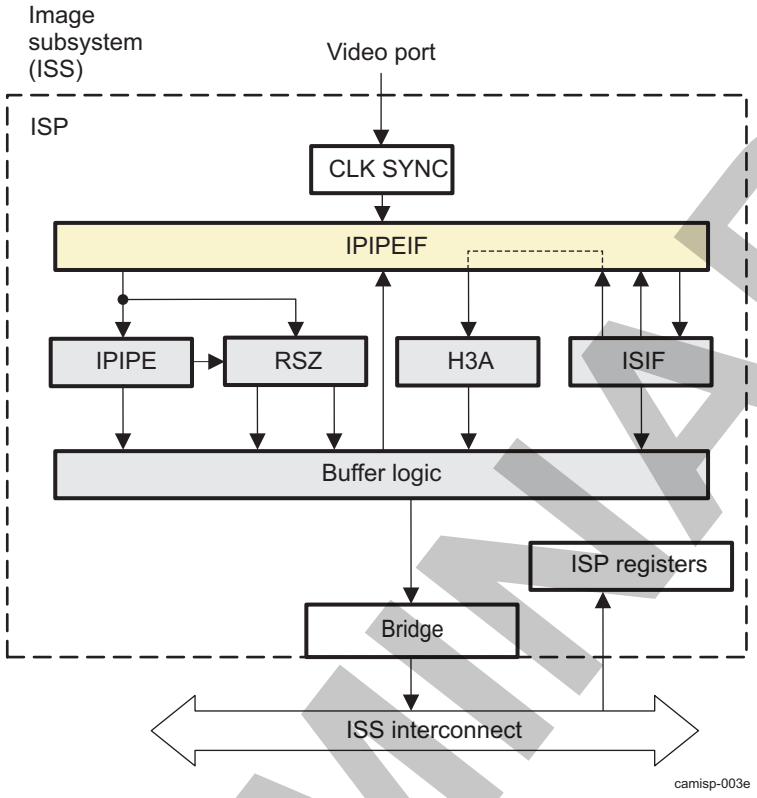
Figure 8-124. ISS ISP IPIPEIF High-Level Diagram



8.3.3.2.2 ISS ISP IPIPEIF Top-Level Block Diagram

The following sections describe the function of each subblock in the IPIPEIF, as shown in Figure 8-125.

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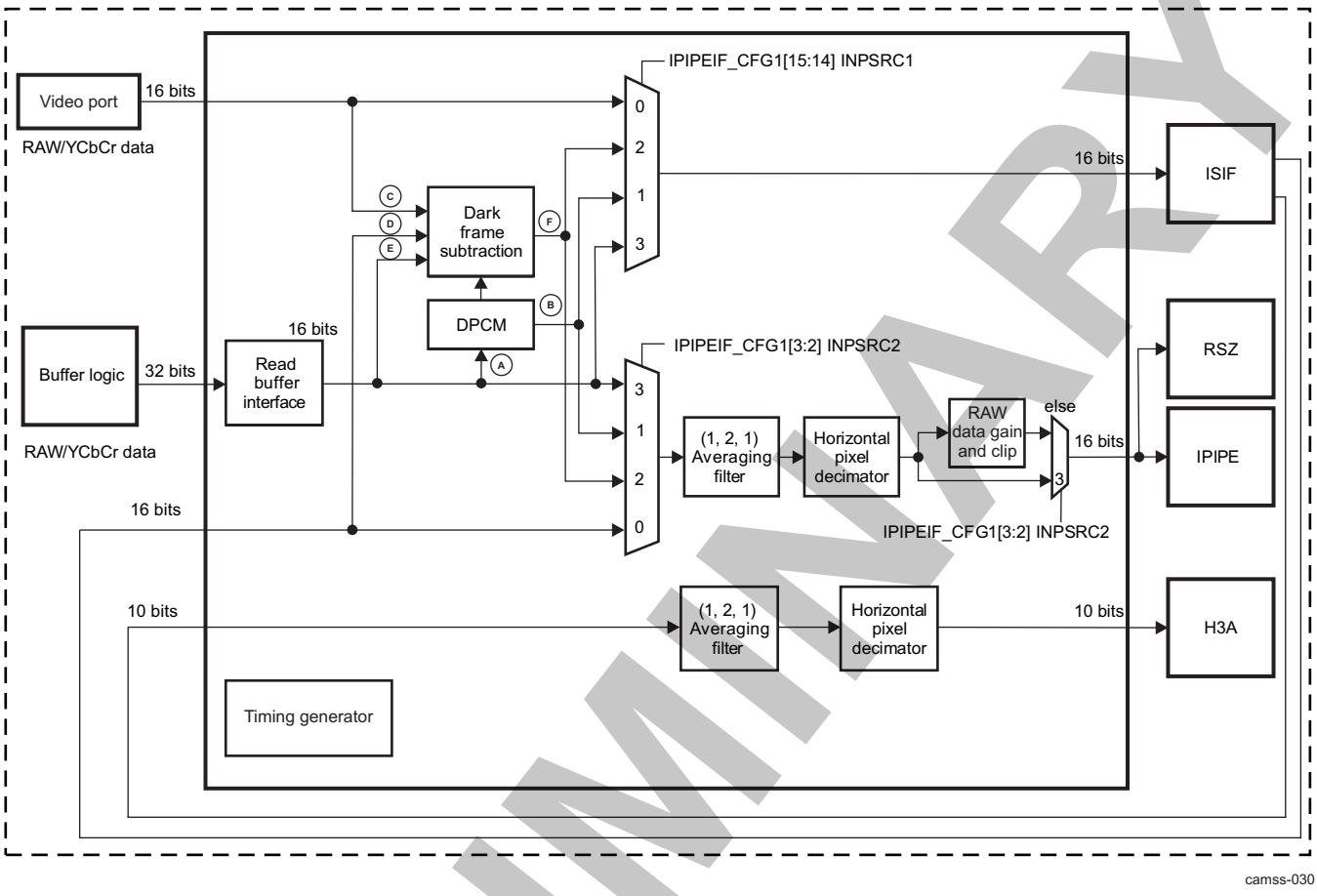
Figure 8-125. ISS ISP IPIPEIF Top-Level Block Diagram



camss-030

NOTE: When the IPIPEIF receives data from the VP, the timing generator must be configured for HD, VD, and WEN. For more information, see Section 8.3.3.2.5, *ISS ISP IPIPEIF Timing Generation.*

8.3.3.2.3 ISS ISP IPIPEIF Input Interface

The IPIPEIF module comprises two major interface blocks: VP and BL. The data types can be RAW or YUV.

8.3.3.2.3.1 ISS ISP IPIPEIF Input From VP

The VP typically receives data from the image sensor. At the ISS level, it is connected to the serial interface receivers.

8.3.3.2.3.2 ISS ISP IPIPEIF Input From BL

The BL is the interface with the memory (SDRAM). In that case, the SDRAM address and line offset registers must be programmed in units of 32 bytes.

- SDRAM start address (byte) = (IPIPEIF_ADDRU[10:0] ADDRU) << 16 + (IPIPEIF_ADDRL[15:0] ADDRL)
- SDRAM address offset (byte) = IPIPEIF_ADOFS[11:0] ADOFS

Two types of data can be stored in memory: pixel data and dark frame data.

For pixel data, the HD and VD signals are reconstructed with:

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- IPIPEIF_HNUM
- IPIPEIF_VNUM
- IPIPEIF_LPFR
- IPIPEIF_PPLN

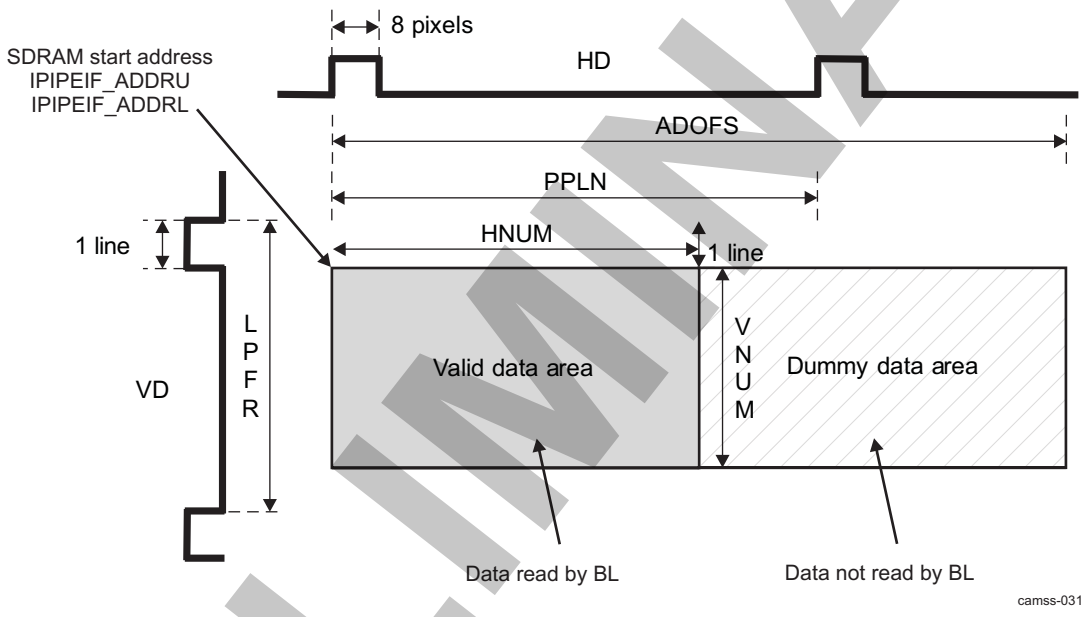
The IPIPEIF_HNUM and IPIPEIF_VNUM registers define the number of pixels per line and lines per frame to read from the SDRAM, and the IPIPEIF_LPFR and IPIPEIF_PPLN registers define the interval of VD and HD, respectively.

Vertical blanking for the frame is defined with the following equation: IPIPEIF_LPFR – IPIPEIF_VNUM – 1.

Horizontal blanking for the frame must be at least eight ISP_FCLK cycles, and is defined with the following equation: IPIPEIF_PPLN – IPIPEIF_HNUM > 7.

Figure 8-126 shows the global frame definition for all SDRAM input modes, except for dark frame subtract.

Figure 8-126. ISS ISP IPIPEIF Global Frame Definition in SDRAM Input Modes (Except Dark Frame)



For dark frame data, the HD and VD signals come from the VP through the ISIF. The IPIPEIF_PPLN and IPIPEIF_LPFR registers must be used to indicate the horizontal and vertical start position of the subtraction from the ISIF data, as shown in Figure 8-127. The value of the IPIPEIF_LPFR[12:0] LPFR bit field must be greater than 0 because the first line from the VP or ISIF cannot be subtracted from. The IPIPEIF_HNUM and IPIPEIF_VNUM registers must be used to set the number of valid pixels horizontally and the number of valid lines vertically.

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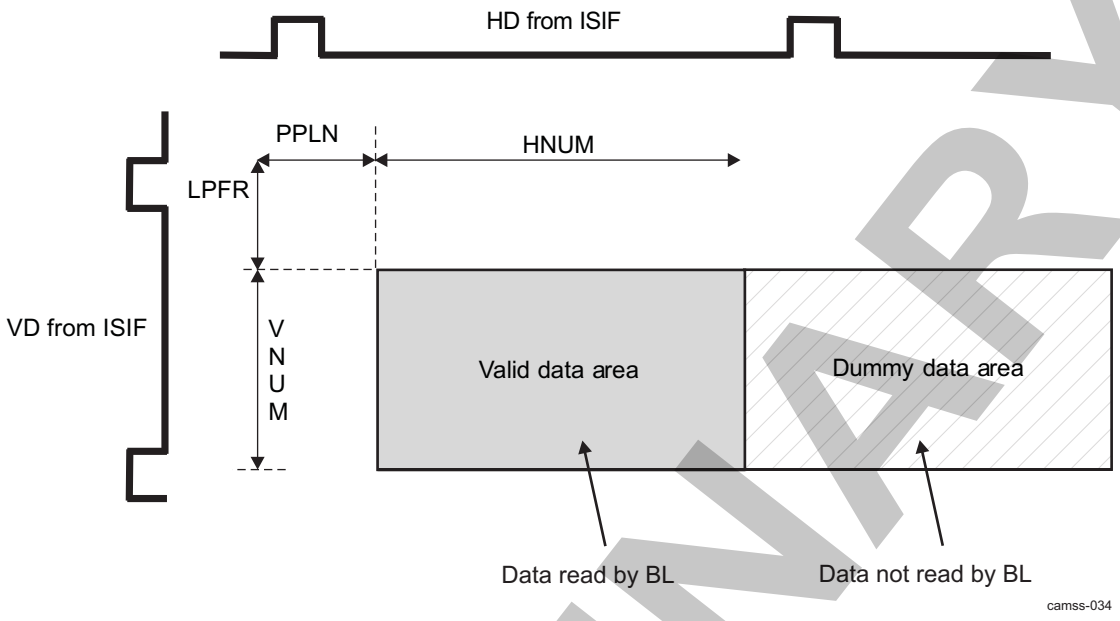
Figure 8-127. ISS ISP IPIPEIF Global Frame Definition in Dark Frame Subtract Mode



8.3.3.2.3.2.1 ISS ISP IPIPEIF Double-Buffer Input Function When Reading From BL

The IPIPEIF module supports a double-buffer input function. This feature is most useful when SDRAM space is limited, because it enables to read continuously from two buffers and to push data to the rest of the ISP (ISIF, H3A, etc.) for further processing.

Consider the following configuration where data are read from two buffers, A and B. The intent is not only to read continuously from these buffers but also to ensure that the ISP modules consider the data as being from the same frame; that is, VD is generated the first time buffer A is read, but it must not toggle until all the frames are read.

The IPIPEIF module can mask the VD sync signal by setting the IPIPEIF_ENABLE[1] SYNCOFF bit such that the IPIPEIF module drives the data to the ISP modules as if it is a continuous frame data.

In the following example, there are 16 lines per trigger and input circular addressing. VNUM = 16 (see Figure 8-126), and the VD signal is generated only for the first frame (see Figure 8-128).

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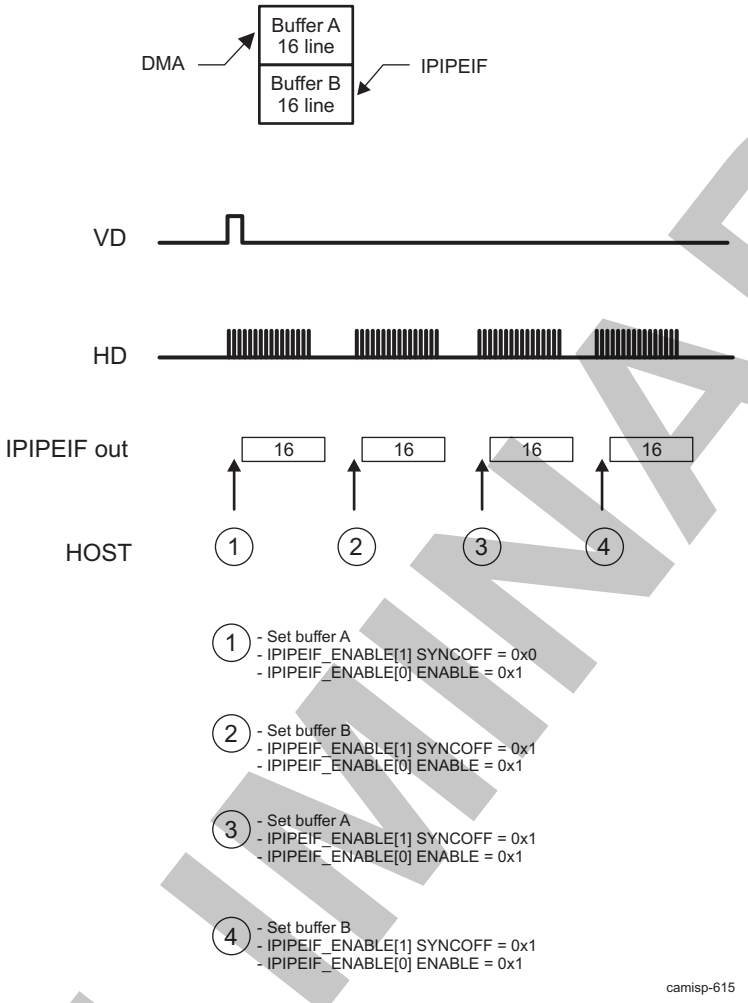
Figure 8-128. ISS ISP IPIPEIF Double-Buffer Functionality



8.3.3.2.4 ISS ISP IPIPEIF Data Path Selection

The data path configuration through the IPIPEIF module is set with the IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 bit fields. Table 8-422 lists the possible combinations for these two bit fields.

Table 8-422. ISS ISP IPIPEIF IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 Possible Combinations

IPIPEIF_CFG1[15:14] INPSRC1	IPIPEIF_CFG1[3:2] INPSRC2	Description	Common Use
0	0	This data path is described in Section 8.3.3.2.4.1, *ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 0*.	Video record, view finder, on-the-fly still image capture applications
0	1	This data path is described in Section 8.3.3.2.4.2, *ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 1*.	Memory-to-IPIPE-to-memory operation
0	2	This data path is described in Section 8.3.3.2.4.3, *ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 2*.	Image capture with on-the-fly dark frame subtraction

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Table 8-422. ISS ISP IPIPEIF IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 Possible Combinations (continued)

IPIPEIF_CFG1[15:14] INPSRC1	IPIPEIF_CFG1[3:2] INPSRC2	Description	Common Use
0	3	This data path is described in Section 8.3.3.2.4.4, *ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 3*.	On-the-fly data acquisition done in VP, forwarded to the ISIF, and then to the H3A through IPIPEIF while data from memory is processed and forwarded to the IPIPE module and then stored in memory YUV4:2:2 or RAW data processing with the IPIPE and RSZ modules from memory to memory fetched by IPIPEIF
1	0	This data path is described in Section 8.3.3.2.4.5, *ISS ISP IPIPEIF INPSRC1 = 1 and INPSRC2 = 0*.	Memory-to-ISIF-to-memory operation
1	1	This data path is possible but there is no use case associated.	N/A
1	2	This data path is not supported.	N/A
1	3	This data path is not supported.	N/A
2	0	This data path is described in Section 8.3.3.2.4.6, *ISS ISP IPIPEIF INPSRC1 = 2 and INPSRC2 = 0*.	Dark frame subtraction is performed and data sent to the ISIF module for further processing, back to IPIPEIF, and then to IPIPE and RSZ.
2	1	This data path is not supported.	N/A
2	2	This data path is not supported.	N/A
2	3	This data path is not supported.	N/A
3	0	This data path is described in Section 8.3.3.2.4.7, *ISS ISP IPIPEIF INPSRC1 = 3 and INPSRC2 = 0*.	Memory-to-ISIF-to-memory operation
3	1	This data path is not supported.	N/A
3	2	This data path is not supported.	N/A
3	3	This data path is possible but there is no use case associated.	N/A

8.3.3.2.4.1 ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 0

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 0 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 0.

This configuration can be used for the video record, viewfinder, and on-the-fly still image capture applications. The full ISP processing capability is used in a single pass.

Figure 8-129 shows the data path.

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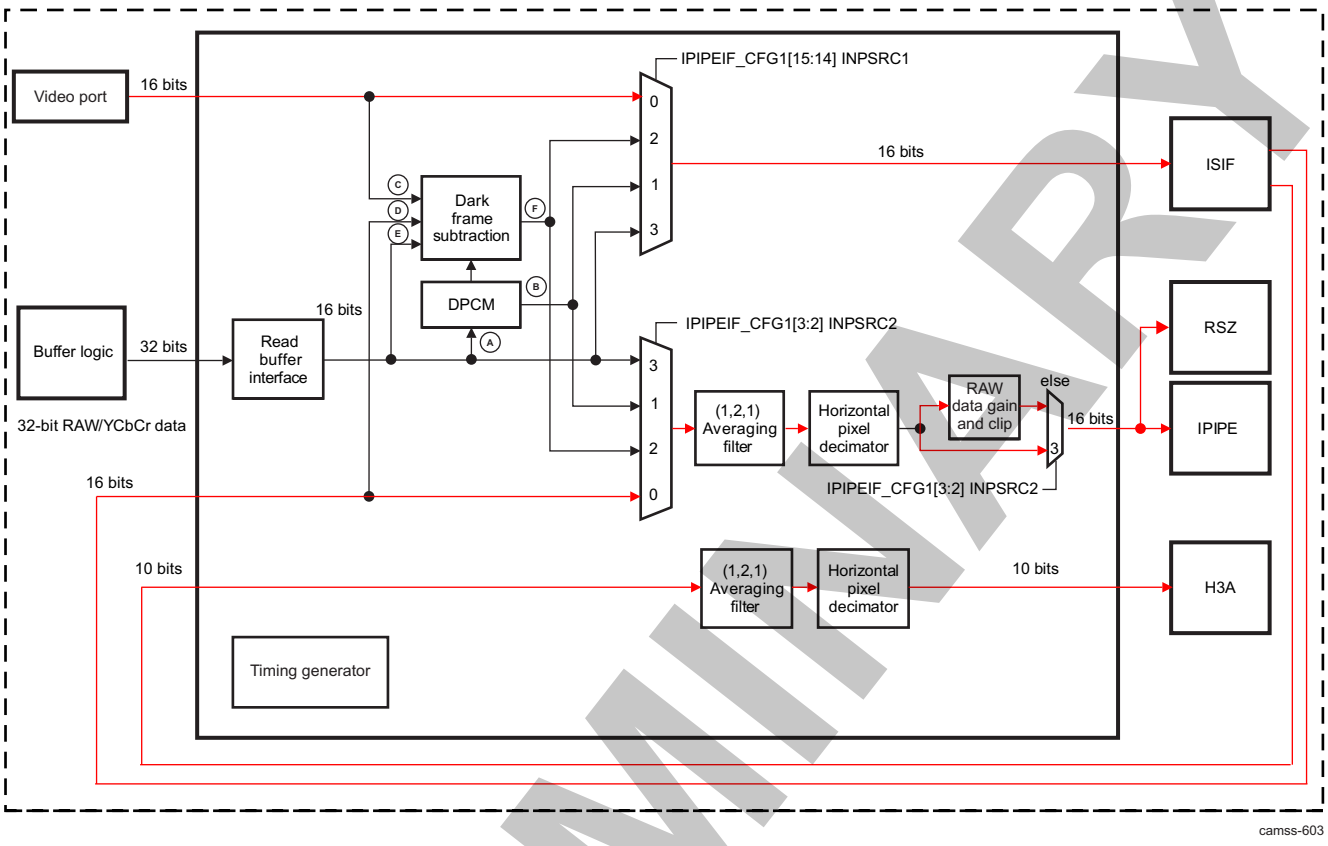
Figure 8-129. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 0 Data Path



8.3.3.2.4.2 ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 1

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 0 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 1.

This configuration can be used to process data with the IPIPE module from memory to memory. The data stored in SDRAM can be decompressed (A-law or DPCM) before being forwarded to the IPIPE module.

NOTE: In this configuration, the ISIF and H3A modules are assumed to be disabled.

Figure 8-130 shows the data path.

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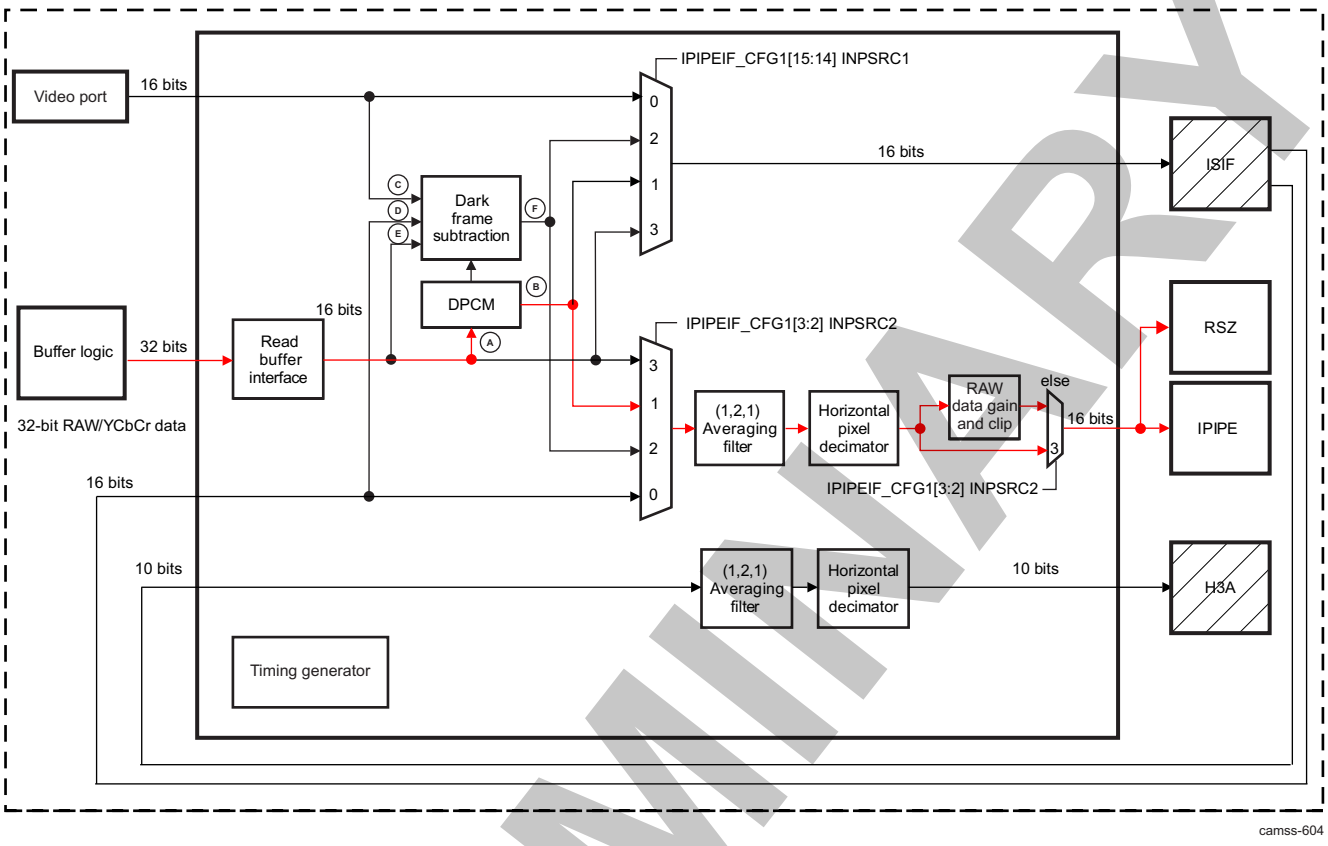
Figure 8-130. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 1 Data Path



8.3.3.2.4.3 ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 2

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 0 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 2.

This configuration can be used for image capture with on-the-fly dark-frame subtraction. In the first case, the dark frame can come from BL and data from the ISIF. In the second case, the dark frame can come from the VP and data from BL.

Figure 8-131 shows the data path.

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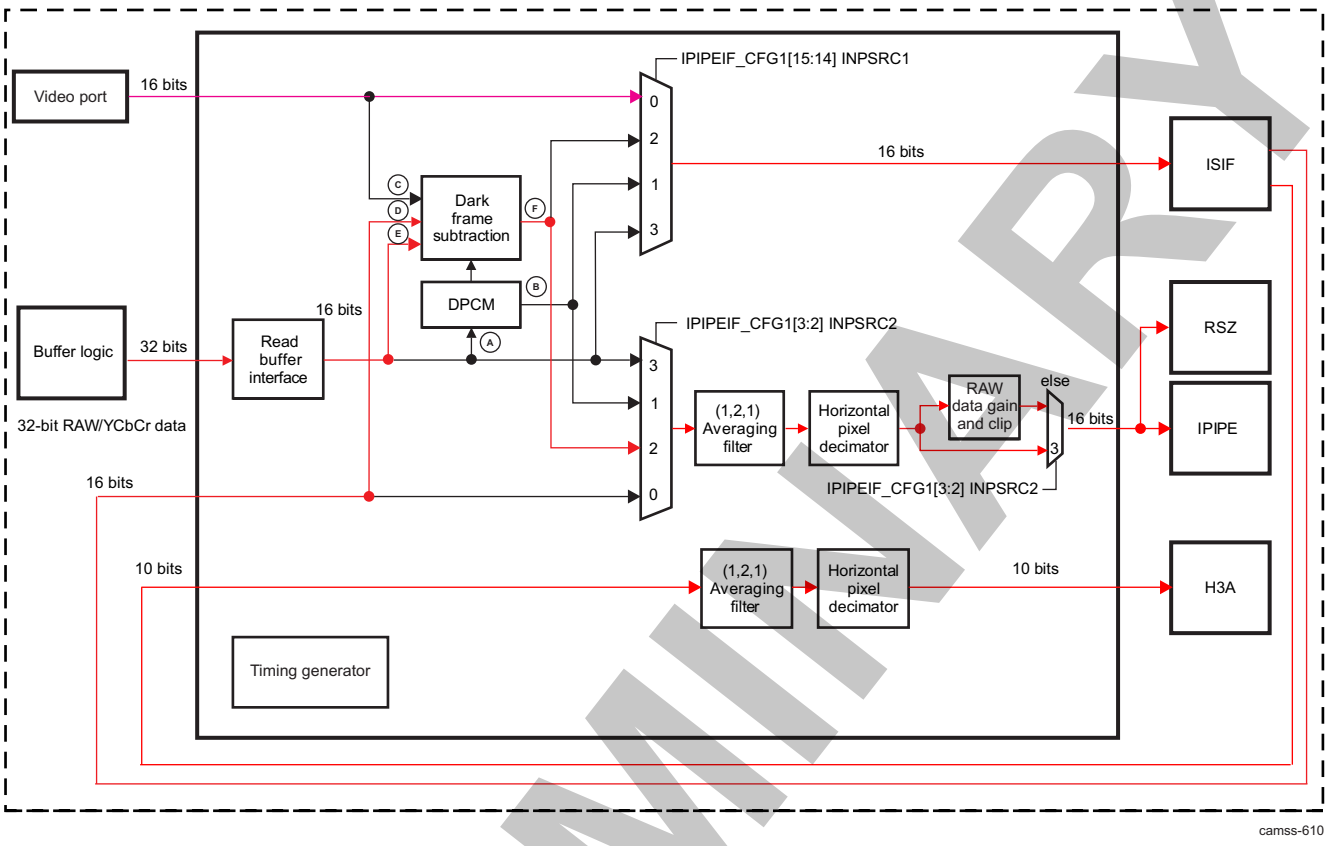
Figure 8-131. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 2 Data Paths



8.3.3.2.4.4 ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 3

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 0 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 3.

In the first case, on-the-fly data acquisition is done with the VP, forwarded to the ISIF, and then sent to the H3A through the IPIPEIF while data from memory is processed and forwarded to the IPIPE module and then stored in memory.

In the second case, the configuration can be used to process YUV4:2:2 or RAW data with the IPIPE and RSZ modules from memory-to-memory. The YUV4:2:2 or RAW data stored in the SDRAM is fetched and forwarded to the IPIPE and RSZ modules. ISIF and H3A are assumed to be disabled in this configuration.

Figure 8-132 and Figure 8-133 show the two possible data paths.

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Figure 8-132. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 3 Data Paths: First Case

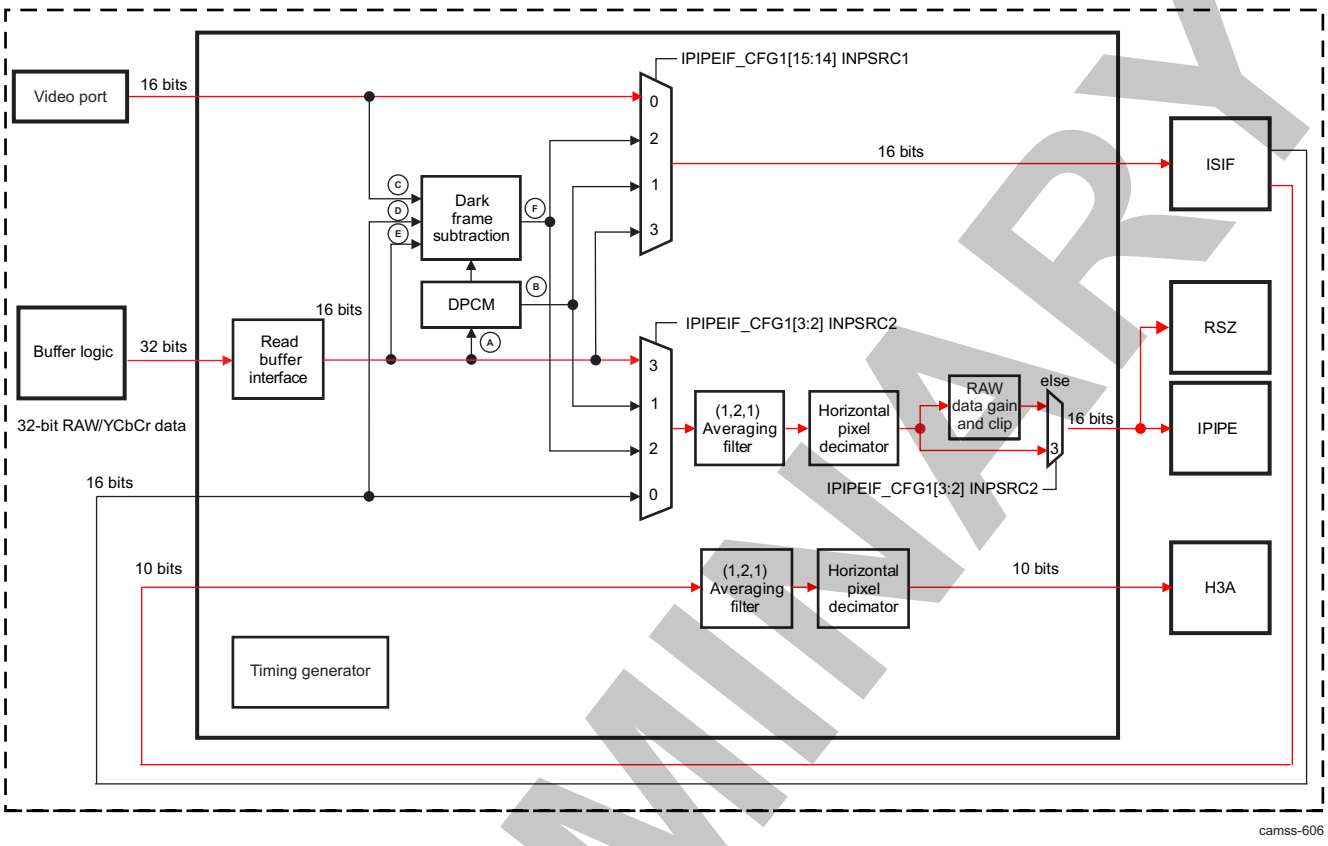

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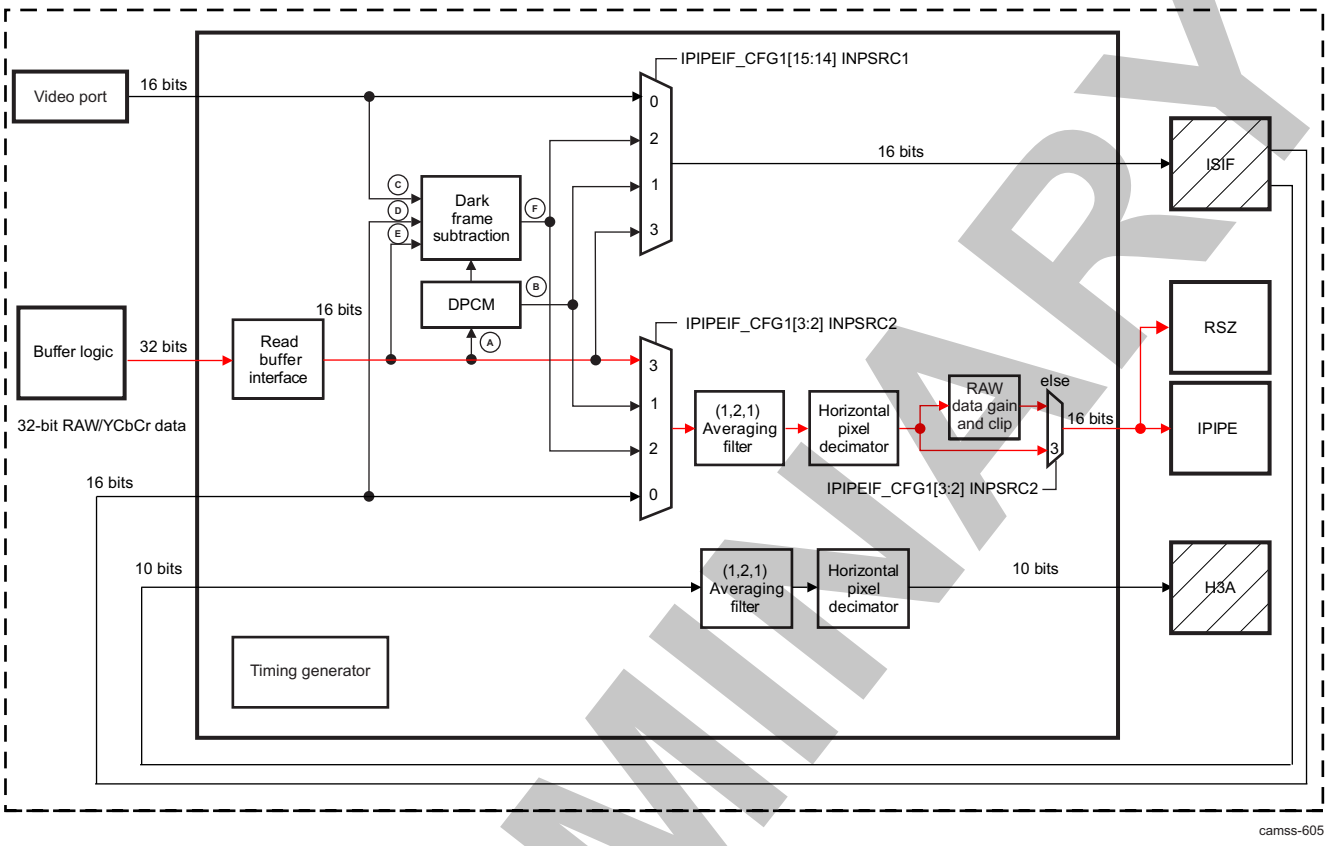
Figure 8-133. ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 3 Data Paths: Second Case



8.3.3.2.4.5 ISS ISP IPIPEIF INPSRC1 = 1 and INPSRC2 = 0

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 1 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 0.

This configuration is a memory-to-memory operation. RAW data is read by the BL interface, decompressed, and pushed to the ISIF. The ISIF processes the data and sends it back to the IPIPEIF module before the data is pushed to the IPIPE and H3A modules.

Figure 8-134 shows the data path.

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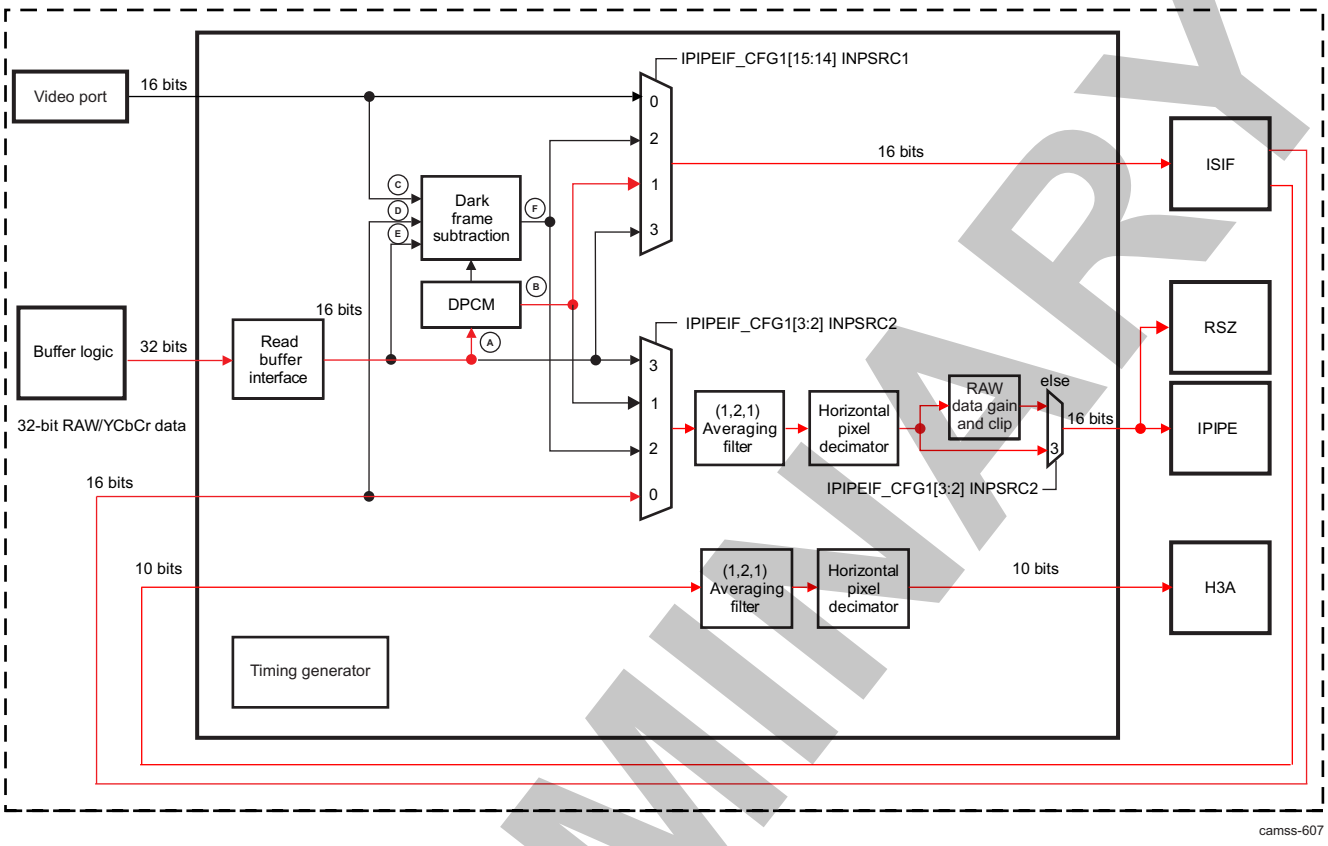
Figure 8-134. ISS ISP IPIPEIF INPSRC1 = 1 and INPSRC2 = 0 Data Path



8.3.3.2.4.6 ISS ISP IPIPEIF INPSRC1 = 2 and INPSRC2 = 0

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 2 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 0.

In this configuration, dark frame subtraction is performed and data is sent to the ISIF module. The ISIF processes the data and sends it back to the IPIPEIF module before the data is pushed to the IPIPE or RSZ modules. There are two possible dark frame subtractions: the first is with data coming from the VP and the dark frame coming from BL; the second is with data coming from BL and the dark frame coming from the VP.

Figure 8-135 shows the data path.

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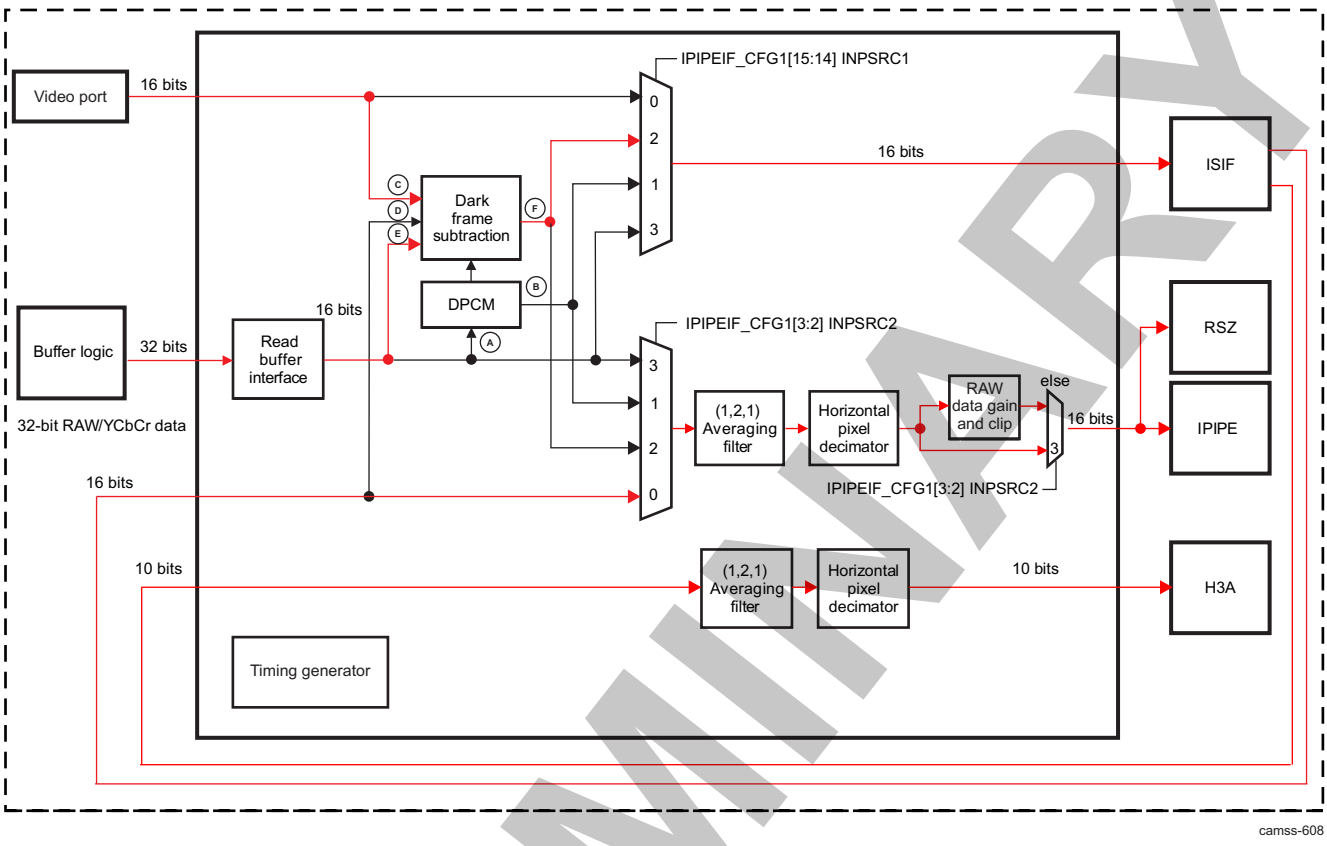
Figure 8-135. ISS ISP IPIPEIF INPSRC1 = 2 and INPSRC2 = 0 Data Path



8.3.3.2.4.7 ISS ISP IPIPEIF INPSRC1 = 3 and INPSRC2 = 0

Set the IPIPEIF_CFG1[15:14] INPSRC1 bit field to 3 and the IPIPEIF_CFG1[3:2] INPSRC2 bit field to 0.

This configuration is a memory-to-memory operation. Data is loaded from the SDRAM. Input data is expected as 16 bpp. The ISIF processes the data and sends it back to the IPIPEIF module before the data is pushed to the IPIPE or RSZ module.

In this configuration data is assumed to be YUV only, and H3A and RAW data gain are assumed to be disabled.

Figure 8-136 shows the data path.

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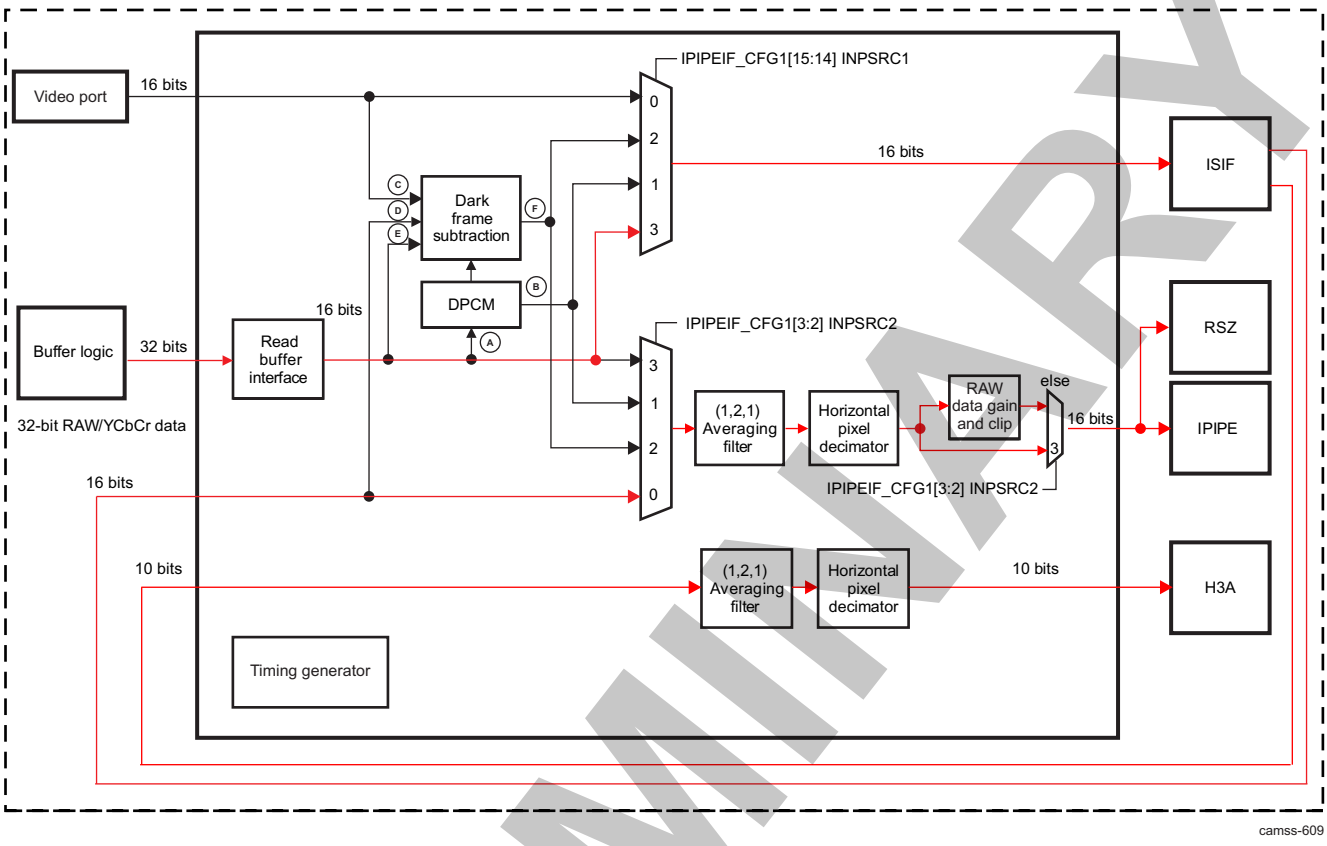
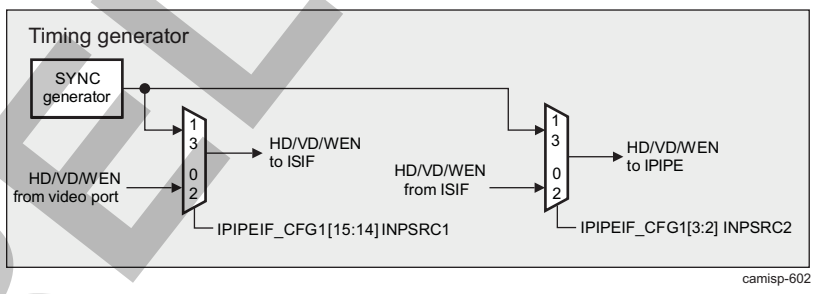
Figure 8-136. ISS ISP IPIPEIF INPSRC1 = 3 and INPSRC2 = 0 Data Path



8.3.3.2.5 ISS ISP IPIPEIF Timing Generation

Figure 8-137 shows the ISS ISP IPIPEIF timing generator submodule.

Figure 8-137. ISS ISP IPIPEIF Timing Generator Submodule



When the IPIPEIF module input source is from the VP (IPIPEIF_CFG1[15:14] INPSRC1 = 0 or 2) or the ISIF (IPIPEIF_CFG1[3:2] INPSRC2 = 0 or 2), the IPIPEIF_CFG1[10] CLKSEL bit must be set to 0 so that data is latched using the PCLK, HD, and VD signals from the VP.

When the IPIPEIF module input source is not from the VP (IPIPEIF_CFG1[15:14] INPSRC1 = 1 or 3), the IPIPEIF_CFG1[10] CLKSEL bit must be set to 1 so that the IPIPEIF module generates its proper PCLK, HD, and VD signals (through the use of the SYNC generator). The IPIPEIF_CLKDIV register is then used to select a divide ratio of the SDRAM (DMA) clock for the pixel clock frequency, which is used to clock the data into the PCLK. See Section 8.3.3.2.5.1, *ISS ISP IPIPEIF Fractional Clock Divider*.

When the IPIPEIF_CFG1[15:14] INPSRC1 or IPIPEIF_CFG1[3:2] INPSRC2 bit field is not set to 0, the IPIPEIF SDRAM data reading and timing generation can be enabled (IPIPEIF_ENABLE[0] ENABLE) in one-shot mode or continuous mode (IPIPEIF_CFG1[0] ONESHOT).

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8.3.3.2.5.1 ISS ISP IPIPEIF Fractional Clock Divider

When the input data of the IPIPEIF module does not come from the VP but from memory, it is useful to have control of the rate at which the data is fetched from memory to avoid overflow conditions or to avoid peak bandwidth requirements. The IPIPEIF_CFG1[10] CLKSEL bit is equal to 1 for fractional divider use.

The ISP clock ISP_FCLK is divided to generate the pixel clock, which goes to the ISIF and IPIPE modules when data is read from memory (IPIPEIF_CFG1[15:14] INPSRC1 = IPIPEIF_CFG1[3:2] INPSRC2 = 1 or 3). The IPIPEIF_CLKDIV register selects the divider ratio: M and N values in the IPIPEIF_CLKDIV[15:0] CLKDIV bit field.

Given an input clock of clock rate ISP_FCLK, the fractional clock divider generates an output clock with average clock rate f_{OUT}.

Where f_{OUT} = ISP_FCLK x M/N, and M = 1 through 256, and N = 1 through 256.

The fractional clock divider logic is synchronous and uses only the positive clock edge of the input clock.

8.3.3.2.6 ISS ISP IPIPEIF Decompression (DPCM) Subblock: Unpack and Decompression Function

The IPIPEIF module can read RAW data from memory. The RAW data can be previously packed/compressed into memory. Unpack, A-Law decompression, and DPCM decompression are available in the IPIPEIF module.

Figure 8-138 shows the DPCM subblock.

Figure 8-138. ISS ISP IPIPEIF DPCM Subblock

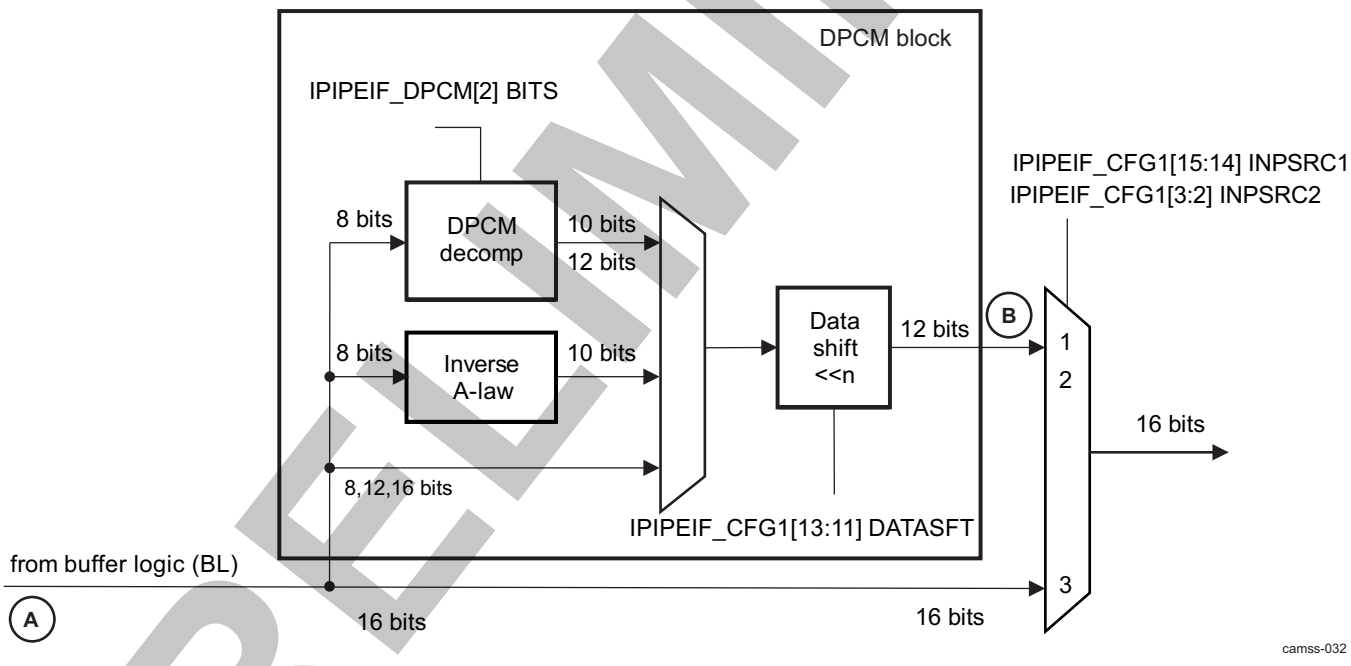

Table 8-423 provides the possible configuration of the DPCM block.

Table 8-423. ISS ISP IPIPEIF DPCM Block Possible Configuration

Number of Bits per Pixel at DPCM Block Input	Number of Bits per Pixel at DPCM Block Output	Description	Registers
16	16	It can correspond to YUV4:2:2 or RAW16 data.	IPIPEIF_CFG1[9:8] UNPACK = 0x0 In this configuration, IPIPEIF_CFG1[3:2] INPSRC2 = 0x3. In this configuration data bypasses the DPCM block.

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Table 8-423. ISS ISP IPIPEIF DPCM Block Possible Configuration (continued)

Number of Bits per Pixel at DPCM Block Input	Number of Bits per Pixel at DPCM Block Output	Description	Registers
8	8	PACK8: YUV	IPIPEIF_CFG1[9:8] UNPACK = 0x1 IPIPEIF_DPCM[0] ENA = 0x0 IPIPEIF_CFG1[13:11] DATASFT = 0x01 In this configuration an 8-bit packed RAW data is used in DFS mode or YUV4:2:0 pass through. (See Section 8.3.3.2.13, *ISS ISP IPIPEIF YUV4:2:2 8-bits Packed Data Input Coming From ISIF Module*.)
8	10	DPCM10: The 8-bit input data are DPCM-decompressed in 10 bits.	IPIPEIF_CFG1[9:8] UNPACK = 0x1 IPIPEIF_DPCM[0] ENA = 0x1 IPIPEIF_DPCM[2] BITS = 0x0 Set the IPIPEIF_DPCM[1] PRED(1) (2) IPIPEIF_CFG1[13:11] DATASFT = 0x2
8	12	DPCM12: The 8-bit input data are DPCM-decompressed in 12 bits.	IPIPEIF_CFG1[9:8] UNPACK = 0x1 IPIPEIF_DPCM[0] ENA = 0x1 IPIPEIF_DPCM[2] = 0x1 Set the IPIPEIF_DPCM[1] PRED(1) (2) IPIPEIF_CFG1[13:11] DATASFT = 0x0
8	10	ALAW10: The 8-bit input data were previously A-law compressed. The 8 bits are A-law decompressed and padded with 0.	IPIPEIF_CFG1[9:8] UNPACK = 0x2 IPIPEIF_CFG1[13:11] DATASFT = 0x2
12	12	PACK12: The input is coded on 12 bits and is packed in the SDRAM. This mode is compatible with the ISIF module packing capability. If inverse A-law and DPCM decompression are not enabled, the data read from the SDRAM can be shifted by the IPIPEIF_CFG1[13:11] DATASFT bit field to select which 12 bits to use. MSB input data bit must be shifted such that it corresponds to bit 11 after the shift.	IPIPEIF_CFG1[9:8] UNPACK = 0x3 Set the IPIPEIF_CFG1[13:11] DATASFT

(1) The simple predictor uses only the value of the previous same color component as a prediction value. Therefore, only 2-pixel memory is required. It is typically used for 10–8–10 or 12–8–12 bit conversions.

(2) The advanced predictor uses four previous pixel values, when the prediction value is evaluated. This means that the values of the other color components are also used, when the prediction value is defined. Therefore, the advanced predictor is slightly better than the simple predictor but consumes more power and memory. It can, however, improve image quality. It is typically used for 10–7–10 and 10–6–10 bit conversions.

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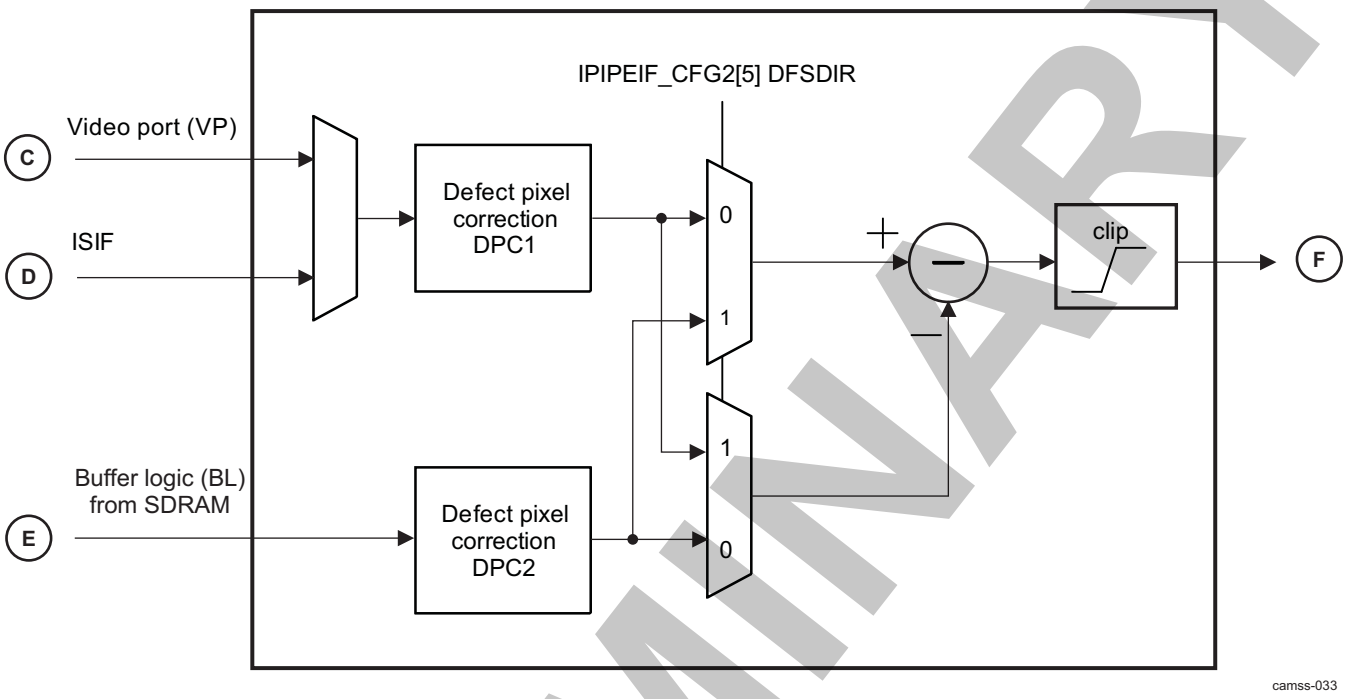
8.3.3.2.7 ISS ISP IPIPEIF Dark-Frame Subtraction Functionality

Figure 8-139 shows the ISS ISP IPIPEIF dark-frame subtraction subblock.

Figure 8-139. ISS ISP IPIPEIF Dark-Frame Subtraction Subblock



The dark-frame subtract (DFS) function is used to remove fixed pattern baseline noise from the sensor for a high-quality still image capture use case, where there is a mechanical shutter. Typically, the ISIF module previously writes a dark frame (frame captured when the shutter is closed) to SDRAM using 8 bits of linear data packed into 2 pixels per 16 bits.

In this mode, RAW data from the ISIF and SDRAM is used. Data can also be read from SDRAM with the IPIPEIF_CFG1[9:8] UNPACK bit field set to 1. Each pixel read from SDRAM is subtracted from each pixel sent from the VP or ISIF.

The mux at the input of the dark-frame subtraction subblock is implicitly controlled by the selection of the IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 bit fields:

- When IPIPEIF_CFG1[15:14] INPSRC1 = 0x2, the selected input ports are VP and BL. Therefore, the dark frame operation can be:
  - Dark frame = VP – BL
  - Dark frame = BL – VP
- When IPIPEIF_CFG1[3:2] INPSRC2 = 0x2, the selected input ports are ISIF and BL. Therefore, the dark frame operation can be:
  - Dark frame = ISIF – BL
  - Dark frame = BL – ISIF

The output of the DFS operation is 12 bits wide (U12Q0). There must be adequate SDRAM bandwidth if this feature is enabled. If the data fetched from memory arrives late, an underflow bit (IPIPEIF_DTUF) must be triggered to know it.

When SDRAM data underflow occurs, the data from SDRAM is coming in at a lower rate than the rate at which it is being read/requested by the IPIPEIF. In DFS operation mode, IPIPEIF reads data from both SDRAM and the VP/ISIF. To ensure not corrupting subsequent data processing downstream in the case of SDRAM data underflow, the IPIPEIF stalls the input data, storing remaining sensor data into an internal FIFO (16-deep), and then stops sending new data downstream. The IPIPEIF recommences DFS processing when data from SDRAM becomes available, by using the pixel data from the FIFO and that from SDRAM for processing. To avoid an overflow of the internal FIFO, the IPIPEIF deasserts the stall

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only when the number of FIFO slots indicated by the IPIPEIF_DTUDF[5:2] FIFOWMRKLVL register bit field are free. A safe number of free locations can be configured taking into consideration the pixel clock frequency with respect to that of the functional clock, as the pixel clock speed is allowed to vary up to the functional clock speed. When the pixel clock and functional clock are equal, the stall deassertion can be programmed to occur when the 16-deep FIFO is empty.

When receiving data from CCP2 and there is underflow from obtaining dark frame data through an IPIPEIF SDRAM read, the CCP2 read interface should be stalled to maintain pixel-to-pixel match between sensor image and dark frame data; otherwise, out-of-sync behavior can cause corrupted dark frame subtraction output.

- When the IPIPEIF_DTUDF[1] ENM2MSTALL register bit is set to 1, and an SDRAM read underflow has been detected, IPIPEIF immediately stops sending data to downstream modules. Simultaneously, the IPIPIEIF requests the CCP2 to stop sending sensor image data through an IPIPEIF_STALL signal (similar the ISP resizer CCP2 stall signal) as well to avoid data corruption (see Figure 8-122 for more information, both RSZ and IPIPEIF stall signals are OR-ed within ISP boundary to provide a single STALL signal to CCP2). There is a latency period from underflow detection until final data stalling at IPIPEIF boundary, during which period the sensor data is stored internally through a FIFO in IPIPEIF video port interface path.
- When the IPIPEIF_DTUDF[1] ENM2MSTALL bit is set to 0, and at reset, this stall mechanism is disabled

8.3.3.2.7.1 ISS ISP IPIPEIF Defect Pixel Correction

NOTE: For DPC memory access locations, see Section 8.3.3.8, *ISS ISP Memory Mapping*.

A simple DPC can be applied to the ISIF or VP input data path and SDRAM input data path, respectively. This DPC algorithm is intended to correct hot pixels during RAW dark frame acquisition or dark frame readout from SDRAM before dark frame subtraction.

The following code describes DPC algorithm:

```
If (image(n) < TH) || ((image(–2)  TH)&&(image(n+2)>TH)
 image(n) = image(n)
Else if image(–2) > TH
 image(n) = image(n+2)
Else if image(n+2) > TH
 image(n) = image(–2)
Else
 image(n) = (image(–2)+ image(n+2))/2

// Where TH is equal to IPIPEIF_DPC1[11:0] TH for DPC1
// Where TH is equal to IPIPEIF_DPC2[11:0] TH for DPC2
```

The IPIPEIF_DPC1[12] ENA bit enables DPC for the VP/ISIF input path, and the IPIPEIF_DPC2[12] ENA bit enables DPC for the SDRAM input path. The algorithm requires a threshold value that is set by the IPIPEIF_DPC1[11:0] TH or IPIPEIF_DPC2[11:0] TH bit field that is a 12-bit unsigned value.

8.3.3.2.7.2 ISS ISP IPIPEIF DFS Subtraction Direction

The IPIPEIF_CFG2[5] DFSDIR bit selects how the DFS subtraction is performed.

- Set the IPIPEIF_CFG2[5] DFSDIR bit to 0 when the RAW data is coming from the VP/ISIF and the dark frame is stored in SDRAM.
- Set the IPIPEIF_CFG2[5] DFSDIR bit to 1 when the RAW data is coming from SDRAM and the dark frame is coming from the VP/ISIF.

After subtraction, a clip ensures that the value is not negative.

Table 8-424 lists the different modes supported in DFS.

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Table 8-424. ISS ISP IPIPEIF DFS Modes Supported

Description	DFDIR Value
DFS of 8-bit RAW image stored in SDRAM from image from VP	IPIPEIF_CFG2[5] DFSDIR = 0x0
DFS of 8-bit RAW image stored in SDRAM from image from ISIF	IPIPEIF_CFG2[5] DFSDIR = 0x0
DFS of 8-bit RAW image from VP from image read from SDRAM through the BL	IPIPEIF_CFG2[5] DFSDIR = 0x1

NOTE: DFS input depends on the settings of INPSRC1 and INPSRC2.

8.3.3.2.8 ISS ISP IPIPEIF (1, 2, 1) Averaging Filter for IPIPE Data Path

The averaging filter acts as an anti-aliasing low-pass filter for the horizontal pixel decimator. Usually, when horizontal pixel decimation is enabled (IPIPEIF_CFG1[1] DECIM), the averaging filter must also be enabled to avoid aliasing artifacts. The averaging filter can be enabled by setting the IPIPEIF_CFG1[7] AVGFILT bit. It operates on every other pixel (same color) in RAW Bayer input or every Y component in YCbCr data in the following equation:

output = (input[i – 1] + 2 × input[i] + input[i + 1]) >> 2

The averaging filter operates on every other pixel (same color) in RAW Bayer input or YUV data.

If the data is YUV4:2:2, the option to average and decimate is given under the conditions listed in Table 8-425.

Table 8-425. ISS ISP IPIPEIF Averaging Filter Conditions for YUV4:2:2 Data

IPIPEIF_CFG1[3:2] INPSRC2	IPIPEIF_CFG2[3] YUV16	Comments
0	1	YUV4:2:2 data is coming from the ISIF module. Averager and decimation is possible on the data path to the IPIPE module.
1	1	YUV4:2:2 data is read from SDRAM. Averager and decimation is possible on the data path to the IPIPE module.
3		YUV4:2:2 data is read from SDRAM. Averager and decimation is possible on the data path to the IPIPE module.
Other value	Other value	For YUV4:2:2 data, averager and decimation is not possible on the data path to the IPIPE module.

The averager implements a (1, 2, 1) FIR filter on Luma and Chroma. The following registers have a part in the behavior of the YUV data averaging and decimation:

- IPIPEIF_INIRSZ[12:0] INIRSZ
- IPIPEIF_CFG1[7] AVGFILT
- IPIPEIF_CFG1[1] DECIM

8.3.3.2.9 ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for IPIPE Data Path

The IPIPE input is limited to 5376 pixels per horizontal line due to restrictions in the line memory width in the IPIPE.

To process image sensor resolutions with more than 5376 pixels per line with no resolution loss, vertical frame division mode (FDM) must be used; that is, the image must be divided into vertical chunks of less than 5376 pixels, and each chunk must be processed sequentially by the ISP. FDM is memory-to-memory processing and is not supported on the fly.

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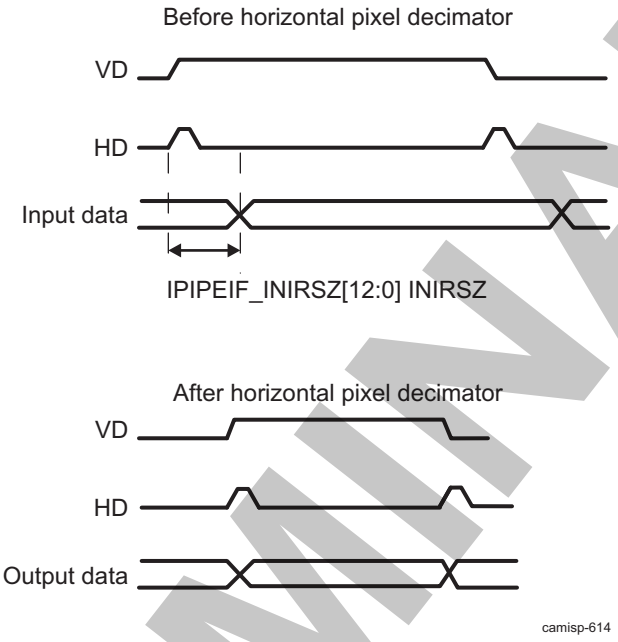
Alternatively, if a loss in resolution is acceptable, the line width decimator (the IPIPEIF_CFG1[1] DECIM bit) can be enabled to downsample the input lines to a width equal to or less than the 5376 pixel maximum. The resize ratio (16/RSZ) can be configured by programming the IPIPEIF_RSZ[6:0] RSZ bit field to be within the range from 16 to 112 to give a resampling range from 1x to 1/7x.

When ALNSYNC is enabled (IPIPEIF_INIRSZ[13] ALNSYNC = 0x1), the IPIPEIF_INIRSZ[12:0] INIRSZ pixels are skipped (from the HD position) before the horizontal pixel decimator, as shown in Figure 8-140.

Figure 8-140. ISS ISP IPIPEIF Resizer Offset Definition



8.3.3.2.10 ISS ISP IPIPEIF RAW Data Gain for IPIPE Data Path

A gain factor ranging from 0.00195(1/512) to 1.99805(1023/512) is multiplied to the RAW output of the IPIPEIF. The gain is not applied if the input data is YCbCr. The gain constant is set in the IPIPEIF_GAIN[9:0] GAIN bit field using U10Q9 format.

The output value is clipped after gain control through the value of the IPIPEIF_OCLIP[11:0] OCLIP bit field.

8.3.3.2.11 ISS ISP IPIPEIF (1, 2 ,1) Averaging Filter for H3A Data Path

The averaging filter acts as an anti-aliasing low-pass filter for the horizontal pixel decimator. Usually, when horizontal pixel decimation is enabled (the IPIPEIF_RSZ3A[9] DECIM bit), the averaging filter must also be enabled to avoid aliasing artifacts. The averaging filter can also be used to reduce noise before H3A statistics generation. It operates on every other pixel (the same color) in a RAW Bayer input or every Y component in YCbCr data. The averaging filter can be enabled by setting the IPIPEIF_RSZ3A[8] AVGFILT bit, and it operates with the following equation:

output = (input[i – 1] + 2 × input[i] + input[i + 1]) >> 2

8.3.3.2.12 ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for H3A Data Path

The H3A input is limited to 3008 pixels per horizontal line due to restrictions in the line memory width in the H3A.

To process image-sensor resolutions with more than 3008 pixels per line with no resolution loss, vertical FDM must be used; that is, the image must be divided into vertical chunks of less than 3008 pixels, and each chunk must be processed sequentially by the ISP. FDM is memory-to-memory processing and is not supported on the fly.

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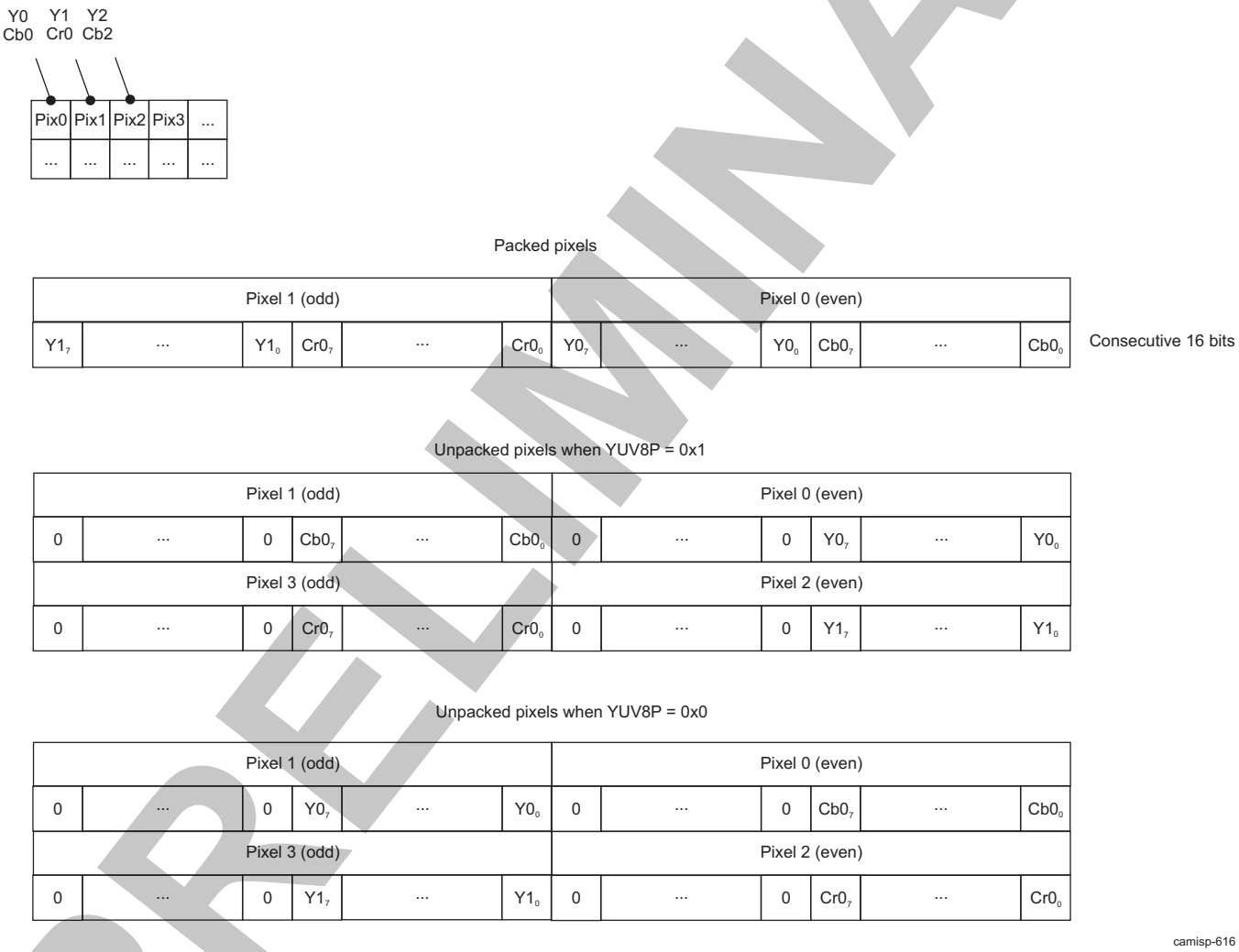
Alternatively, if loss of resolution is acceptable, the line width decimator (the IPIPEIF_RSZ3A[9] DECIM bit) can be enabled to downsample the input lines to a width equal to or less than the 3008 pixel maximum. The resize ratio (16/RSZ) can be configured by programming the IPIPEIF_RSZ3A[6:0] RSZ bit field to be within the range from 16 to 112 to give a resampling range from 1x to 1/7x.

When ALNSYNC is enabled (IPIPEIF_INIRSZ3A[13] ALNSYNC = 0x1), the IPIPEIF_INIRSZ3A[12:0] INIRSZ pixels are skipped (from the HD position) before the horizontal pixel decimator (see Figure 8-140).

8.3.3.2.13 ISS ISP IPIPEIF YUV4:2:2 8-bit Packed Data Input Coming From ISIF Module

This section applies when data coming from the ISIF is 8 bits (IPIPEIF_CFG2[6] YUV8 = 0x1). When IPIPEIF_CFG1[3:2] INPSRC2 = 0 and IPIPEIF_CFG2[3] YUV16 = 1, the 8-bit YUV data are transformed into 16-bit YUV data. The way the data are unpacked from 8 bits to 16 bits is controlled by the IPIPEIF_CFG2[7] YUV8P bit. See Figure 8-141.

Figure 8-141. ISS ISP IPIPEIF YUV8P Settings



8.3.3.2.14 ISS ISP IPIPEIF YUV4:2:0 Data Input for Memory-to-Memory Resize Operations

The ISP RSZ module can resize YUV4:2:0 data. The YUV4:2:0 data can come from the memory (through BL) or from the VP through the CCP2 RX module, which reads data from SDRAM and pushes it to the IPIPEIF module VP. The possible data paths are:

- SDRAM → IPIPEIF (BL) → RESIZER → SDRAM
- SDRAM → CCP2 RX → IPIPEIF (VP) → RESIZER → SDRAM

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- SDRAM → IPIPEIF (BL) → IPIPE → RESIZER → SDRAM
- SDRAM → CCP2 RX → IPIPEIF (BL) → IPIPE → RESIZER → SDRAM

When the data comes from BL, the IPIPEIF module must be set up to process the Luma data first, and then the Chroma data.

- For 420Y (first pass):
  - IPIPEIF_CFG1[15:14] INPSRC1 = 0x1 (SDRAM data input)
  - IPIPEIF_CFG1[3:2] INPSRC2 = 0x1 (SDRAM data input)
  - IPIPEIF_CFG1[13:11] DATASFT = 0x0 (no data shift)
  - IPIPEIF_CFG1[9:8] UNPACK = 0x1 (data packed on 8 bits)
  - IPIPEIF_CFG2[3] YUV16 = 0x1 (data_input[7:0] = 0 and data_input[15:8] = valid)
- For 420C (second pass):
  - IPIPEIF_CFG1[15:14] INPSRC1 = 0x1 (SDRAM data input)
  - IPIPEIF_CFG1[3:2] INPSRC2 = 0x1 (SDRAM data input)
  - IPIPEIF_CFG1[13:11] DATASFT = 0x0 (no data shift)
  - IPIPEIF_CFG1[9:8] UNPACK = 0x1 (data packed on 8 bits)
  - IPIPEIF_CFG2[3] YUV16 = 0x0 (data_input[7:0] = valid and data_input[15:8] = 0)

8.3.3.2.15 ISS ISP IPIPEIF Module Events and Status Checking

The IPIPEIF module generates an IPIPEIF event through the IPIPEIF_IRQ interrupt at the end of each frame. This interrupt is set through the ISP5_IRQENABLE_SET_i[9] IPIPEIF_IRQ bit. The input interrupt source generation is selected through the IPIPEIF_CFG2[0] INTSW bit in a certain configuration. The following pseudo code describes INTSW.

```
if (IPIPEIF_CFG2[0] INTSW==0) // Interrupt source from VP
 if (IPIPEIF_CFG1[15:14] INPSRC1==1,2 or 3)
 if (CFG1.ONESHOT==1) // In one shot mode
 Interrupt happens at the end of frame
 else // In continuous mode
 Interrupt is the start position of VD which is generated by IPIPEIF timing generator
 else // IPIPEIF_CFG1[15:14] INPSRC1==0, data is from VP
 Interrupt is the start position of VD from VP

else // Interrupt source from ISIF: IPIPEIF_CFG2[0] INTSW==1
 if (IPIPEIF_CFG1[3:2] INPSRC2==1,2 or 3)
 if (CFG1.ONESHOT==1) // In one shot mode
 Interrupt happens at the end of frame
 else
 Interrupt is the start position of VD which is generated by IPIPEIF timing generator
 else // IPIPEIF_CFG1[3:2] INPSRC2==0, data is from ISIF
 Interrupt is the start position of VD from ISIF
```

In addition to this interrupt, the host must check the IPIPEIF_DTUF status flag of the ISP5_IRQSTATUS_RAW2_i[1] IPIPEIF_UDF bit (if this is enabled and mapped to the ISP IRQ lines) to see if an underflow occurred. For more information, see Section 8.3.4.2.4, *ISS ISP IPIPEIF Interframe Operations*.

If IPIPEIF reads image data from memory, IPIPEIF stalls data output by masking the clock at underflow. When the next data is available at the input side, IPIPEIF restarts sending data. Underflow does not occur in this operation.

In DFS operation (see Section 8.3.3.2.7, *ISS ISP IPIPEIF Dark-Frame Subtraction Functionality* for more information), if the data read from memory are not available before they are required, the behavior of IPIPEIF is as follows:

- If image data is being received from the parallel port (CPI), then underflow occurs. The event is flagged by IPIPEIF_UDF IRQ. The ISP5_IRQSTATUS_RAW2_i[1] IPIPEIF_UDF bit is also set.
- If image data is being received through CCP2, then IPIPEIF raises IPIPEIF_STALL signal to stall CCP2_RD. The IPIPEIF_DTUDF[1] ENM2MSTALL bit controls whether the IPIPEIF raises

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IPIPEIF_STALL signal at underflow event or not.

8.3.3.3 ISS ISP IPIPE Functional Description

8.3.3.3.1 ISS ISP IPIPE Overview

- The input interface extracts the valid region from the Bayer RAW data:
  - Up to 12-bit input pixel resolution
  - Requires at least 8 pixels for horizontal blanking and four lines for vertical blanking. In one-shot mode; 16 blanking lines after processing area are required.
  - The maximum horizontal and vertical offset of IPIPE processing area from synchronous signal is 65534.
  - Supports RGB Bayer pattern for input
- The DPC module fixes defect pixels using two methods: LUT-based and on-the-fly adaptive.
- The 2D noise-filter module reduces noise in RAW data.
- The green-imbalance-correction (GIC) module reduces Gb/Gr difference to remove line crawl noise.
- The white balance module applies offset and gain adjustments to each color.
- The color filter array (CFA) interpolation module implements CFA interpolation. The output from the CFA interpolation module is RGB-4:4:4 formatted data. CFA also reduces aliasing caused by undersampling by digital anti-aliasing (DAA).
- The RGB2RGB blending module applies a 3 × 3 matrix transform to the RGB data generated by the CFA interpolation module.
- The gamma correction module independently applies gamma correction to each RGB component. Gamma is implemented using a piece-wise linear interpolation approach with a 512-entry LUT for each color.
- The second RGB2RGB blending module applies a 3 × 3 matrix transform to the RGB data after gamma correction.
- 3D-LUT converts RGB data to RGB data using 9 × 9 × 9 table and tetrahedral interpolation.
- The RGB2YCbCr conversion module applies 3 × 3 matrix transformation to the RGB data to convert it to YCbCr data. This module also implements offset. The global brightness and contrast enhancement module fixes brightness and contrast tone.
- The 4:2:2 conversion module applies the Chroma low-pass filter and downsampling to Cb and Cr to convert 4:4:4 data to 4:2:2 data.
- The 2D edge-enhancer module improves image clarity with a Luma nonlinear filter.
- The Chroma artifact reduction module reduces color artifacts using gain control and a 2D median filter.
- The output interface module transfers data from IPIPE to SDRAM in the form of one YCbCr (4:2:2 or 4:2:0), RGB (32/16 bits), or Bayer data.
- The histogram function can record histograms of up to four distinct areas into up to 256 bins.
- The boxcar function makes 1/8 or 1/16 size (1/64 or 1/256 in area) images.
- The boundary signal calculator (BSC) makes vectors of row and column summations.

IPIPE has four processing paths:

- Case 1: IPIPE reads CCD RAW data and applies all IPIPE functions and stores the YCbCr (or RGB) data to SDRAM.
- Case 2: IPIPE reads CCD RAW data and stores the Bayer data after white balance to SDRAM.
- Case 3: IPIPE reads YCbCr-4:2:2 data and applies edge enhance, Chroma suppression, and resize to output YCbCr data to SDRAM.
- Case 4: IPIPE reads YCbCr-4:2:0 data and applies resize to output YCbCr data to SDRAM.

Figure 8-142 shows the connections from the IPIPE module to other submodules of the ISP.

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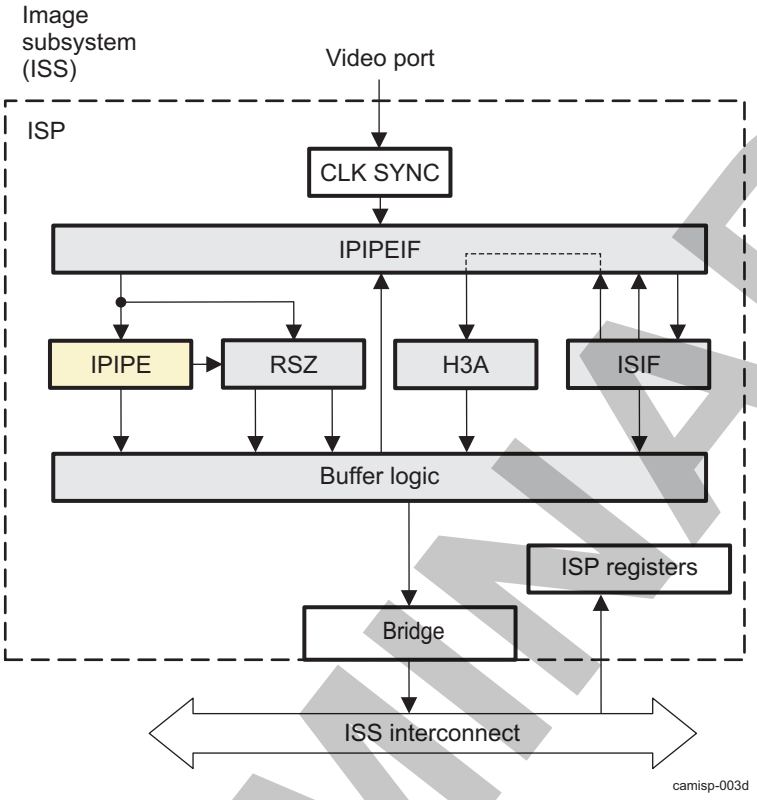
Figure 8-142. ISS ISP IPIPE High-Level Diagram

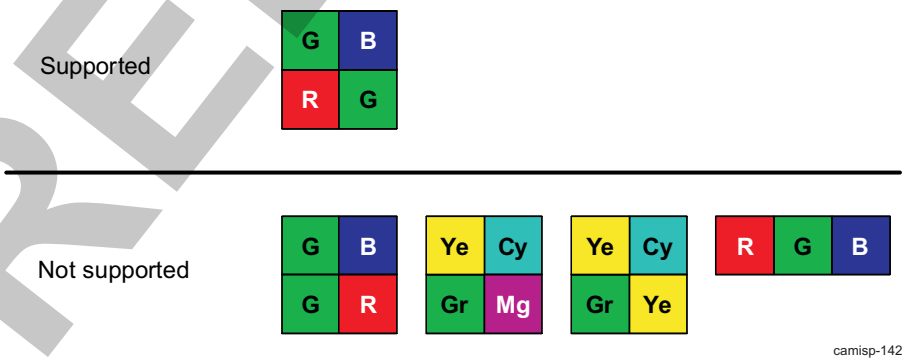


8.3.3.3.2 ISS ISP IPIPE Top-Level Block Diagram

The IPIPE is a programmable hardware image-processing module that generates image data in YCbCr-4:2:2 or YCbCr-4:2:0 format from RAW CCD/CMOS data. The IPIPE module supports output of Bayer data.

The IPIPE module supports RAW data in Bayer format, as shown in Figure 8-143. Other RGB formats or complementary color formats are not supported.

Figure 8-143. ISS ISP IPIPE Supported CFA Format



As shown in Figure 8-144, many internal modules are used to process Bayer data into YCbCr data.

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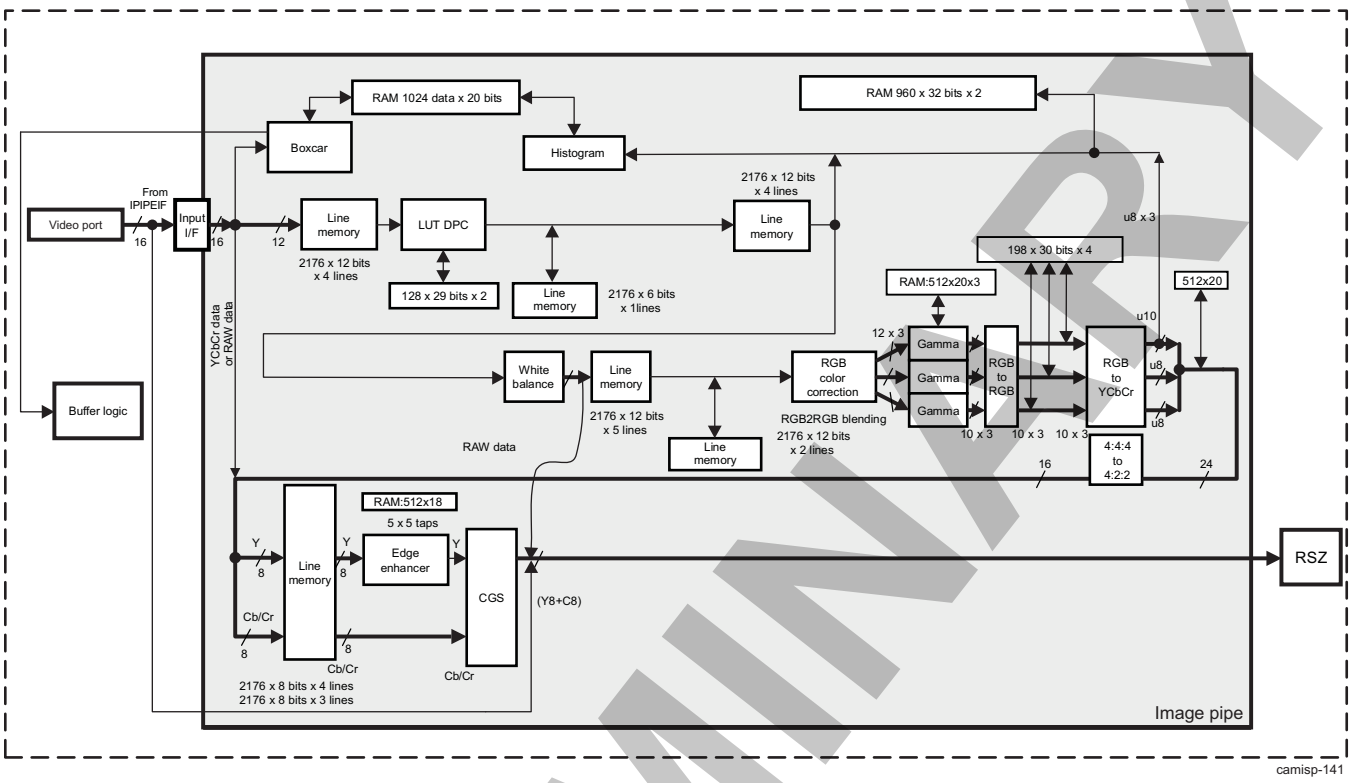
Figure 8-144. ISS ISP IPIPE Module Block Diagram



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8.3.3.3.3 ISS ISP IPIPE Input Interface

The IPIPE module receives 16-bit input data through the IPIPEIF module, which can be 12-bit RAW image data or 16-bit YCbCr data.. The IPIPE module can work with up to 5376 pixels in each horizontal line, except in RAW pass-through mode. If the image width is larger than 5376, the image must be scaled down at the IPIPEIF module level. Otherwise, the input image must be split into several blocks.

If the input data is YCbCr, all RGB processing modules are skipped, and only edge enhancer and Chroma suppression are applied to the input data.

If the input data is YCbCr-4:2:0, only Y or C can be processed at a time, and only the resizer process can be applied. Because the RSZ module is outside the ISIF module, the data is passed to it directly by skipping the RGB and YCbCr processing modules.

In RAW pass-through mode, images up to 8190 pixels per line can be processed. In RAW pass-through mode, the input data is written out directly to SDRAM.

The IPIPE module is enabled through the IPIPE_SRC_EN[0] EN bit.

The IPIPEIF module must be selected as the IPIPE module source with the IPIPE_SRC_MODE[1] WRT bit set to 1 from the input port of the IPIPEIF. This is required to enable and transfer data properly from the interface to the IPIPE.

The IPIPE module has two processing modes, which can be selected through the IPIPE_SRC_MODE[0] OST bit:

- One-shot mode: IPIPE_SRC_MODE[0] OST = 0x1
- Free-run mode: IPIPE_SRC_MODE[0] OST = 0x0

The input and output formats are selected in the IPIPE_SRC_FMT[1:0] FMT bit field (see Table 8-426).

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Table 8-426. ISS ISP IPIPE Input and Output Selections

IPIPE_SRC_FMT[1:0] FMT	IPIPE Module Input	IPIPE Module Output
0x0	RAW Bayer	YCbCr or RGB
0x1	RAW Bayer	RAW Bayer
0x2	RAW Bayer	Disabled
0x3	YCbCr 16 bits	YCbCr

The 16-bit data input to the IPIPE module is in the formats (YCbCr-8bit is not allowed) shown in Figure 8-145.

Figure 8-145. ISS ISP IPIPE Module Input Format

IPIPE input	RAW	LOW	LOW	LOW	LOW	RAW11	RAW10	RAW9	RAW8	RAW7	RAW6	RAW5	RAW4	RAW3	RAW2	RAW1	RAW0
	YCbCr 16b	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0
	Y 8bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
	CbCr 8bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0

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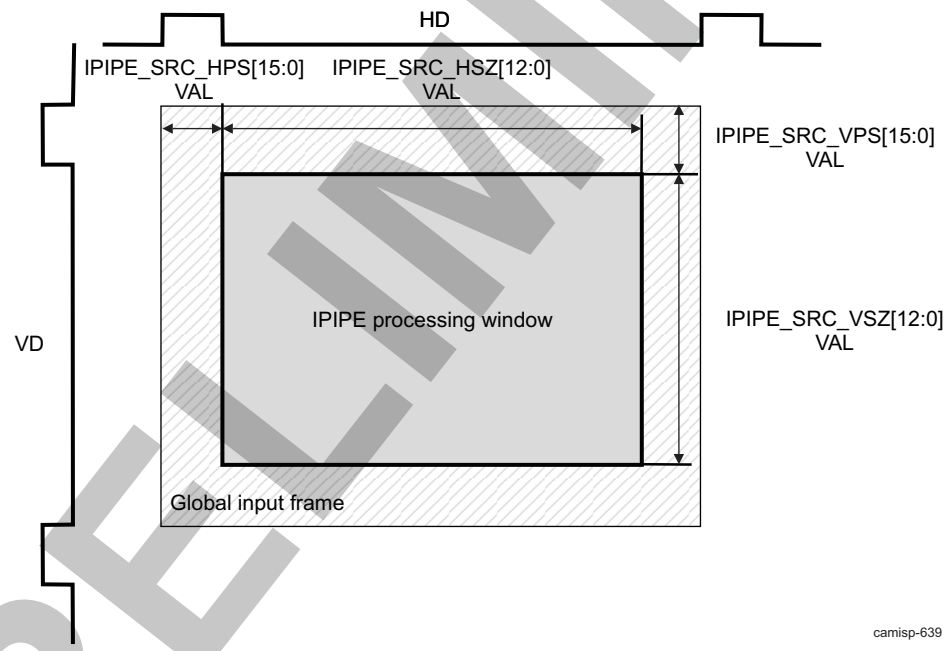
The window to process can be defined by its vertical and horizontal start position (IPIPE_SRC_VPS and IPIPE_SRC_HPS, respectively) and vertical and horizontal size (IPIPE_SRC_VSZ and IPIPE_SRC_HSZ, respectively). Figure 8-146 shows the window settings for processing.

Figure 8-146. ISS ISP IPIPE Module Processing Window Settings



8.3.3.3.4 ISS ISP IPIPE Defect Pixel Correction

The DPC module corrects defect pixels using two methods:LUT-based method (LUT DPC) and on-the-fly adaptive method (OTF DPC). Figure 8-147 shows defect pixel correction.

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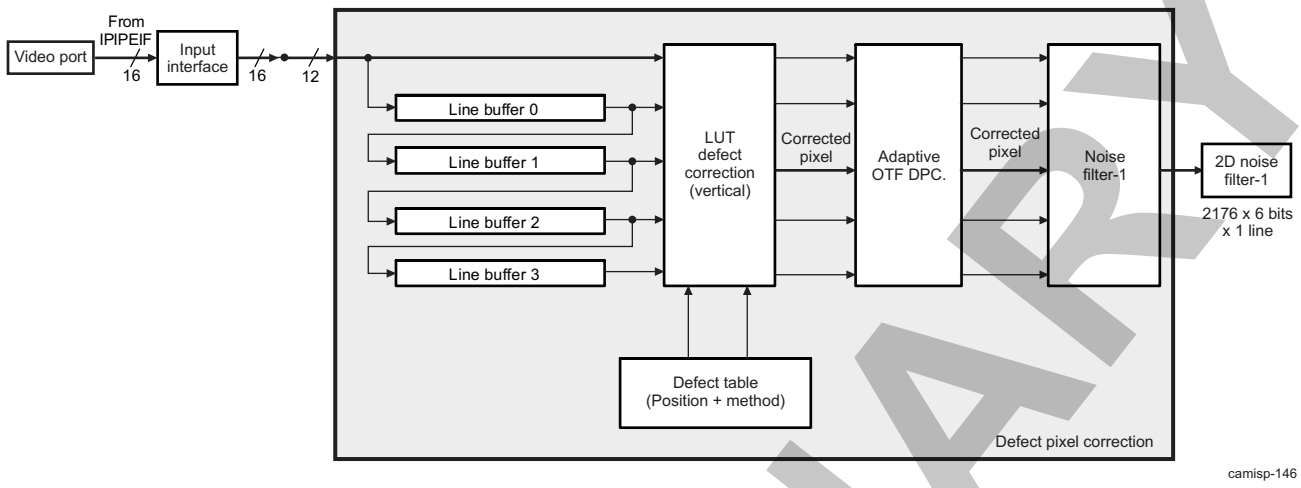
Figure 8-147. ISS ISP IPIPE Defect Pixel Correction



8.3.3.3.4.1 ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC)

LUT DPC is the first stage of the IPIPE image-processing pipeline. The LUT DPC module corrects defects in input data. It supports up to a 256-defect point table. However, the table can be renewed as required during image processing. Therefore, the maximum amount of defect information is limited only by system-level performance.

The module uses two sets of 128 × 29 memories to hold defect information. The table contains the information of horizontal position (13 bits), vertical position (13 bits), and correction method (3 bits), as shown in Table 8-427. The LUT DPC is enabled through the IPIPE_DPC_LUT_EN[0] EN bit.

Table 8-427. ISS ISP IPIPE Defect Information Packing

Correction Method	Vertical Position	Horizontal Position
28…26	25…13	12…0

The information must be listed from left to right and from the top to bottom. The first position in the defect information table and the number of defects that are used can be specified. The address of the table must be programmed in the IPIPE_DPC_LUT_ADR[9:0] ADR bit field. Thus, the address of the first valid data is stated.

The LUT type can be:

- With a finite number of entries:
  - IPIPE_DPC_LUT_SEL[1] TBL = 0x0
  - The size of the LUT is set in the IPIPE_DPC_LUT_SIZ[9:0] SIZ bit field.
- With an infinite number of entries:
  - IPIPE_DPC_LUT_SEL[1] TBL = 0x1

The correction methods, set in Table 8-427, are described in Table 8-428.

Table 8-428. ISS ISP IPIPE Correction Method Description

Correction Method	d0 =	Comment
0	Black or white dot	Replace with a black (or white) dot to force OTF-DPC to work on the pixel. White or black dot replacement can be selected through the IPIPE_DPC_LUT_SEL[0] DOT field.
1	d4	Copy from left
2	d5	Copy from right

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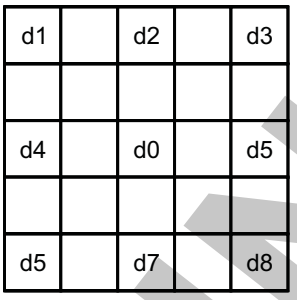
Table 8-428. ISS ISP IPIPE Correction Method Description (continued)

Correction Method	d0 =	Comment
3	(d4 + d5)/2	Horizontal interpolation
4	(d2 + d7)/2	Vertical interpolation
5	d2	Copy from top
6	d7	Copy from bottom
7	(d2 + d4 + d5 + d7)/2	2D interpolation

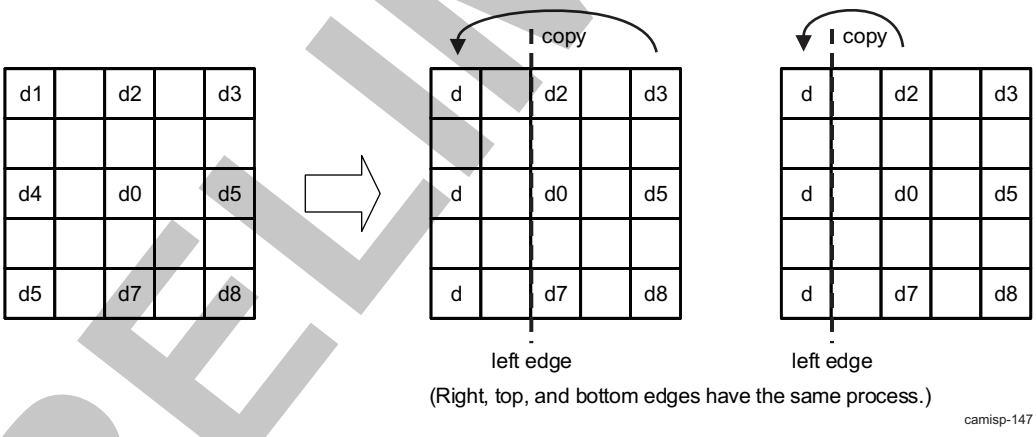
The pixels in the defect correction algorithm are numbered as shown in Figure 8-148.

Figure 8-148. ISS ISP IPIPE Pixel Numbering in Defect Correction Algorithm



The pixels at the edges are mirrored as way described in Figure 8-149. The figure shows the typical correction by overwriting far-edge pixels and mirroring them with other edge pixels. The example shows how by using a noise filter the correct-by-definition pixels are copied over bad pixels.

Figure 8-149. ISS ISP IPIPE Mirroring in Defect Correction and Noise Filter



8.3.3.3.5 ISS ISP IPIPE White Balance

The white balance module executes white balance to each color component. White balance gain adjusts the ratio of each color existing in a CFA pattern. An offset can be applied before white balance correction (IPIPE_WB2_OFT_R, GR, Gb, or B registers).

Figure 8-150 is a block diagram of the white balance module. In the white balance gain adjuster, the RAW data is multiplied by a selected gain (IPIPE_WB2_WGN_R, Gr, Gb, or B registers) corresponding to the color. The white balance gain can be selected from four 13-bit values. Firmware can assign any combination of 4 pixels in horizontal and vertical directions. The precision of each gain is shown in the figure.

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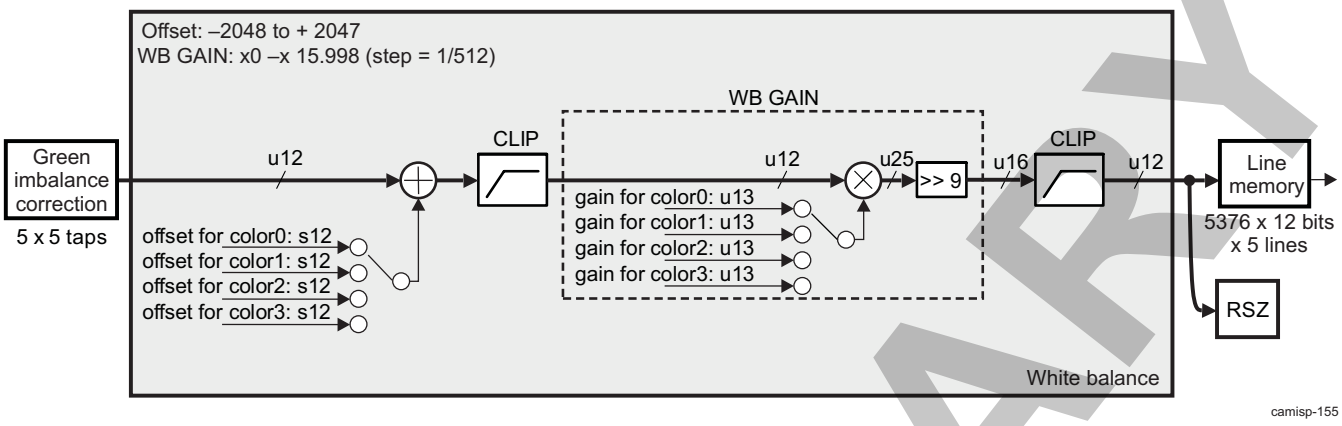
Figure 8-150. ISS ISP IPIPE White Balance



8.3.3.3.6 ISS ISP IPIPE RGB2RGB Blending Module

The RGB2RGB blending module transforms the RGB data generated by the CFA interpolation module using a 3 × 3 square matrix transformation in combination with an added offset. The RGB-to-RGB blending is calculated using the formula shown in Figure 8-151. Each gain range is from –8 to +7.996 with step 1/256 = 0.004, and is set in the IPIPE_RGB1_MUL_RR to IPIPE_RGB1_MUL_BB registers. The offset range for each component is from –4096 to 4095, and is set in the IPIPE_RGB1_OFT_OR to IPIPE_RGB1_OFT_OB registers.

Figure 8-151. ISS ISP IPIPE RGB2RGB Conversion Formula

$$\begin{pmatrix} R\_out \\ G\_out \\ B\_out \end{pmatrix} = \begin{pmatrix} gain\_RR & gain\_GR & gain\_BR \\ gain\_RG & gain\_GG & gain\_BG \\ gain\_RB & gain\_GB & gain\_BB \end{pmatrix} \begin{pmatrix} R\_in \\ G\_in \\ B\_in \end{pmatrix} + \begin{pmatrix} offset\_R \\ offset\_G \\ offset\_B \end{pmatrix}$$

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8.3.3.3.7 ISS ISP IPIPE Gamma Correction Module

NOTE: For the memory access locations of the gamma correction module, see Section 8.3.3.8, *ISS ISP Memory Mapping*.

The gamma correction module performs gamma correction independently for each color in the RGB color space by using a piece-wise linear interpolation. ROM tables and RAM tables are selectable through the IPIPE_GMM_CFG[4] TBL bit. Each ROM table and RAM table has 512 entries, and each entry accommodates a 10-bit offset and 10-bit slope. The range of slope value is from –512 to +511. The ROM table has 1024 entries and an output 8-bit value.

Figure 8-152 is a block diagram of the gamma correction module. It is composed of two tables and one selector. When the BYPASS bit is asserted, the input data is divided by 16 (the IPIPE_GMM_CFG[0] BYPR, IPIPE_GMM_CFG[1] BYPG, and IPIPE_GMM_CFG[2] BYPB bits).

Figure 8-153 shows an example of the gamma curve. Figure 8-154 shows offset and slope packing.

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Figure 8-152. ISS ISP IPIPE Gamma Correction Module Block Diagram

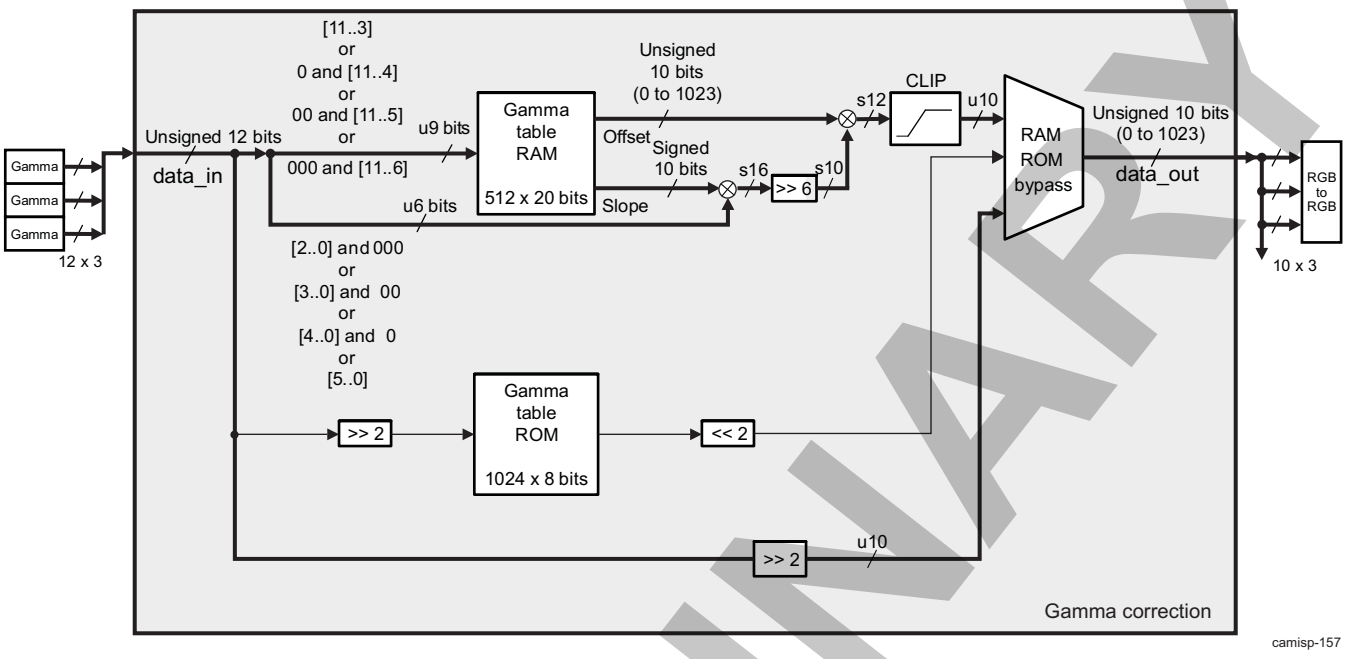


Figure 8-153. ISS ISP IPIPE Gamma Curve Example

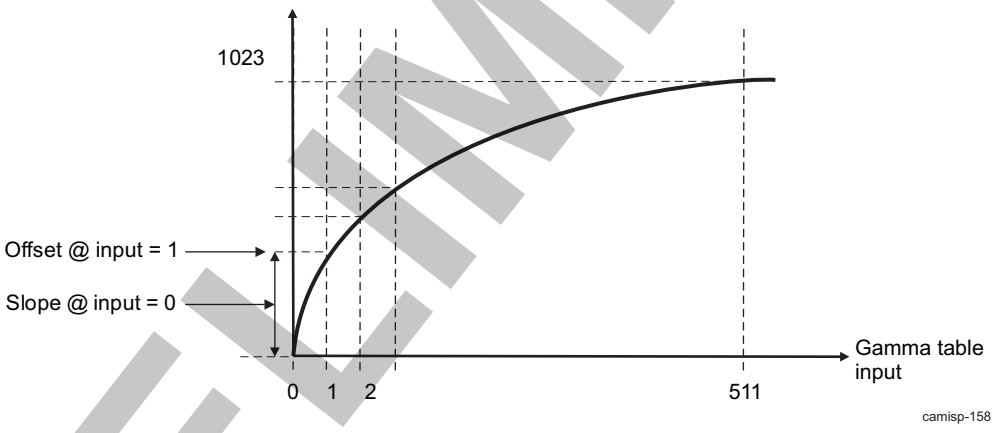
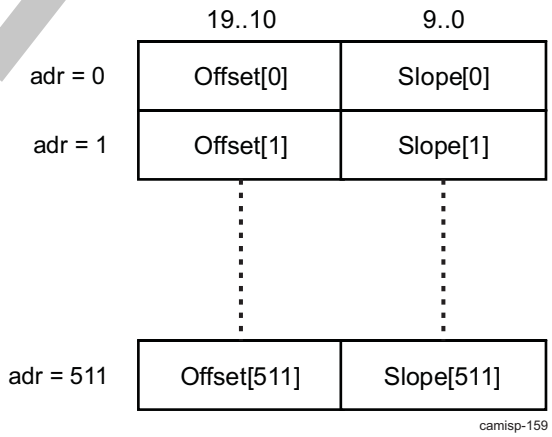


Figure 8-154. ISS ISP IPIPE Gamma Table Offset and Slope Packing



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8.3.3.3.8 ISS ISP IPIPE Second RGB2RGB Conversion Matrix

The second RGB2RGB blending module transforms the RGB data after gamma correction using the 3 × 3 square matrix transformation in combination with an added offset. The RGB-to-RGB blending is calculated using the formula shown in Figure 8-155. Each gain range is from –4 to +3.996 with step 1/256 = 0.004 (s3.8), and is set in the IPIPE_RGB2_MUL_RR to IPIPE_RGB2_MUL_BB registers. The offset is –1024 to 1023 (s11), and is set in the IPIPE_RGB2_OFT_OR to IPIPE_RGB2_OFT_OB registers.

Figure 8-155. ISS ISP IPIPE RGB2RGB Second Conversion Formula

$$\begin{pmatrix} R\_out \\ G\_out \\ B\_out \end{pmatrix} = \begin{pmatrix} gain\_RR & gain\_GR & gain\_BR \\ gain\_RG & gain\_GG & gain\_BG \\ gain\_RB & gain\_GB & gain\_BB \end{pmatrix} \begin{pmatrix} R\_in \\ G\_in \\ B\_in \end{pmatrix} + \begin{pmatrix} offset\_R \\ offset\_G \\ offset\_B \end{pmatrix}$$

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8.3.3.3.9 ISS ISP IPIPE RGB2YCbCr Conversion Matrix

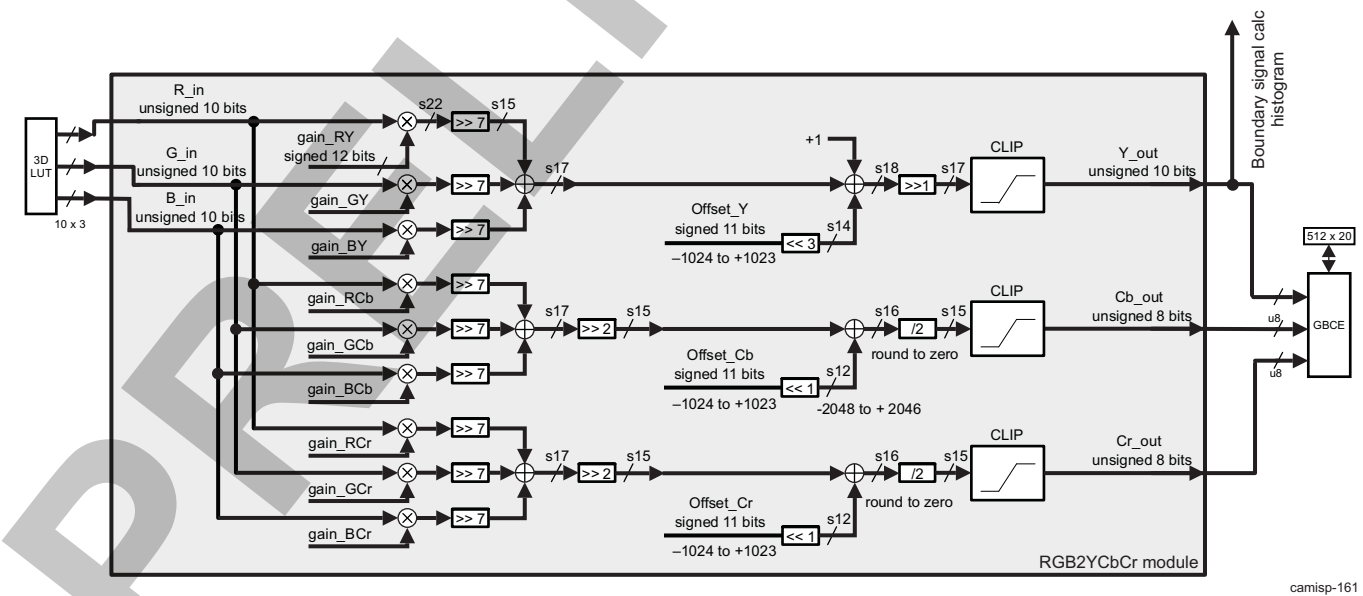
This module transforms the RGB data to YCbCr data format using a 3 × 3 matrix transformation in combination with an added offset. While transferring, the brightness control and contrast control can be adjusted using the IPIPE_YUV_ADJ[15:8] BRT and IPIPE_YUV_ADJ[15:8] CRT bit fields, respectively. Then, the transform is calculated using the formula shown in Figure 8-156. Each gain range is from –8 to +7.996 with step 1/256 = 0.004, configured in the IPIPE_YUV_MUL_RY to IPIPE_YUV_MUL_BCR registers. The offset is –1024 to +1023 for Y, Cb, and Cr, configured in the IPIPE_YUV_OFT_Y to IPIPE_YUV_OFT_CR registers. Figure 8-157 is the block diagram of the RGB to YCbCr blending module. The output is calculated by the equation.

Figure 8-156. ISS ISP IPIPE RGB2YCbCr Conversion Formula

$$\begin{pmatrix} Y\_out \\ Cb\_out \\ Cr\_out \end{pmatrix} = \begin{pmatrix} gain\_RY & gain\_GY & gain\_BY \\ gain\_RCb & gain\_GCb & gain\_BCb \\ gain\_RCr & gain\_GCr & gain\_BCr \end{pmatrix} \begin{pmatrix} R\_in \\ G\_in \\ B\_in \end{pmatrix} + \begin{pmatrix} offset\_Y \\ offset\_Cb \\ offset\_Cr \end{pmatrix}$$

camisp-655

Figure 8-157. ISS ISP IPIPE RGB2YCbCr Module Block Diagram



camisp-161

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8.3.3.3.10 ISS ISP IPIPE 4:2:2 Conversion Module

The 4:2:2 conversion module converts the image data to YCbCr-4:2:2 format by taking the average of every two Cb and Cr components. Y and Cb/Cr sampling point of spatial cosited or spatial centering are selectable using the IPIPE_YUV_PHS[0] POS bit. Horizontal 3 taps and 4- or 2-tap filters are used for spatial cosited and spatial centering, respectively. The module is enabled from the IPIPE_YUV_PHS[1] PLF bit.

Figure 8-158. ISS ISP IPIPE Chroma Subsampling Position

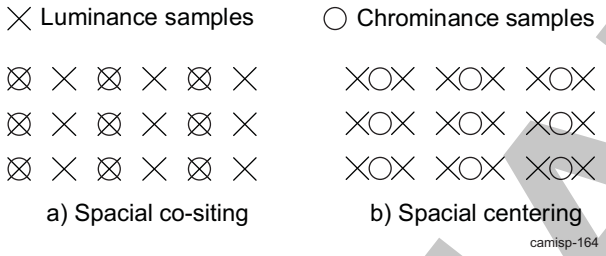
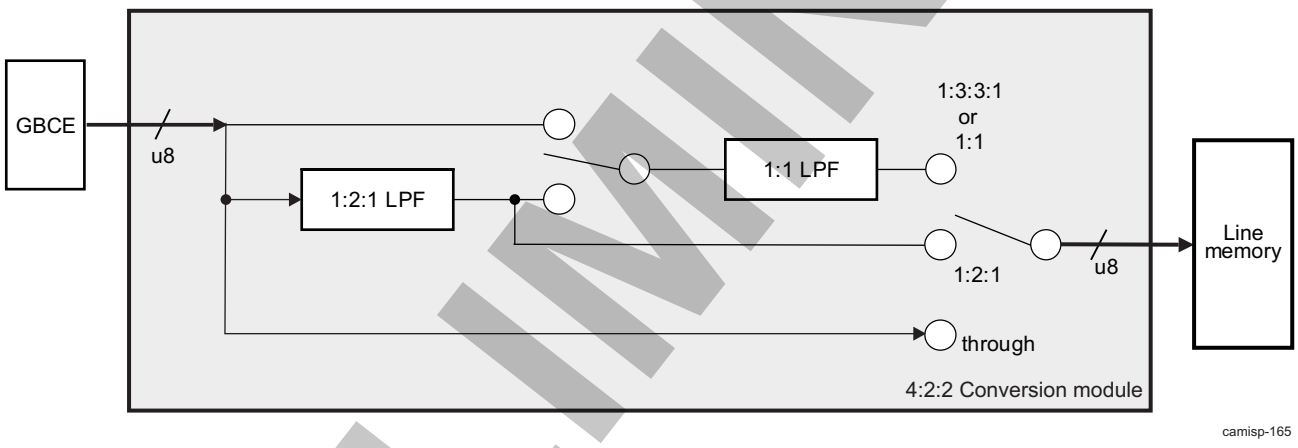


Figure 8-159 is a block diagram of the 4:2:2 conversion module.

Figure 8-159. ISS ISP IPIPE 4:2:2 Conversion Module Block Diagram



8.3.3.3.11 ISS ISP IPIPE 2D Edge-Enhancer

NOTE: For the location of 2D edge-enhancer memory accesses, see Section 8.3.3.8, *ISS ISP Memory Mapping*.

The edge-enhancer module operates on the Luma (Y data) component of images to improve the image quality and can be enabled from the IPIPE_YEE_EN[0] EN bit. Edges in input images are detected by a 2D high-pass filter, and its sharpness is increased by the value from a nonlinear table. Figure 8-161 shows a block diagram of the Luma nonlinear edge-enhancer. Entry for the nonlinear table is 10-bit and the output is in signed 9-bit.

In edge-enhancer mode when IPIPE_YEE_TYP[0] SEL is set to 0, linear filter with programmable coefficient is applied to the Y input. Here, M is a 5 × 5 matrix with programmable coefficients (IPIPE_YEE_MUL_xx, where xx = 00, 01, 02, 10, 11, 12, 20, 21, 22). A down shift of high-pass filter is applied to the edge-enhancer from the IPIPE_YEE_SHF[3:0] SHF bit field (shf_{HFP} in the formula in Figure 8-160).

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Figure 8-160. ISS ISP IPIPE 2D Edge-Enhancer Linear Filter

$$HPF(h,v)=\left(\sum_{j=-2}^{2}\sum_{i=-2}^{2}M_{i,j}Y(h+i,v+j)\right)>>shf_{HPF}$$

$$M=\begin{pmatrix} M_{2,2} & M_{1,2} & M_{0,2} & M_{1,2} & M_{2,2} \\ M_{2,1} & M_{1,1} & M_{0,1} & M_{1,1} & M_{2,1} \\ M_{2,0} & M_{1,0} & M_{0,0} & M_{1,0} & M_{2,0} \\ M_{2,1} & M_{1,1} & M_{0,1} & M_{1,1} & M_{2,1} \\ M_{2,2} & M_{1,2} & M_{0,2} & M_{1,2} & M_{2,2} \end{pmatrix}$$

camisp-801

Then, the HPF value is shrunk by a threshold value (u6) specified by the IPIPE_YEE_THR register ($threshold_{HPF}$ in the formula), and clipped to signed 10 bits to get the index for the LUT.

Figure 8-161. ISS ISP IPIPE 2D Edge-Enhancer Indexing

$$index = clip(shrink(HPF, threshold_{HPF}), -512, 511)$$

$$clip(x, limit_{LOW}, limit_{HIGH}) = \begin{cases} -limit_{LOW} & x < -limit_{LOW} \\ x & -limit_{LOW} \le x \le limit_{HIGH} \\ limit_{HIGH} & limit_{HIGH} < x \end{cases}$$

$$shrink(x, threshold) = \begin{cases} x + threshold & x < -threshold \\ 0 & -threshold \le x \le threshold \\ x - threshold & threshold < x \end{cases}$$

camisp-661

Moreover, the edge-enhancement intensity is looked up from the LUT through the formula shown in Figure 8-162 and in Table 8-429.

Figure 8-162. ISS ISP IPIPE 2D Edge Intensity LUT Formula

$$E_{int} = LUT[index]$$

camisp-662

Table 8-429. ISS ISP IPIPE Edge-Enhancer LUT Mapping

Address (32-bit Word Address)	Bit Position	LUT Index
0x00000h	[8:0]	1
	[17:9]	2
0x00001h	[8:0]	2
	[17:9]	3
0x00002h	[8:0]	4
	[17:9]	5
0x00003h	[8:0]	6
	[17:9]	7

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Table 8-429. ISS ISP IPIPE Edge-Enhancer LUT Mapping (continued)

Address (32-bit Word Address)	Bit Position	LUT Index
. . .	. . .	. . .
0x000FFh	[8:0]	510
	[17:9]	511
0x00100h	[8:0]	–512
	[17:0]	–511
0x00101h	[8:0]	–510
	[17:9]	–509
. . .	. . .	. . .
0x001FD	[8:0]	–6
	[17:9]	–5
0x001FE	[8:0]	–4
	[17:9]	–3
0x001FFh	[8:0]	–2
	[17:9]	–1

Figure 8-163 shows the LUT packing, and Figure 8-164 shows the 2D edge-enhancer block diagram.

Figure 8-163. ISS ISP IPIPE 2D Edge-Enhancer LUT Packing

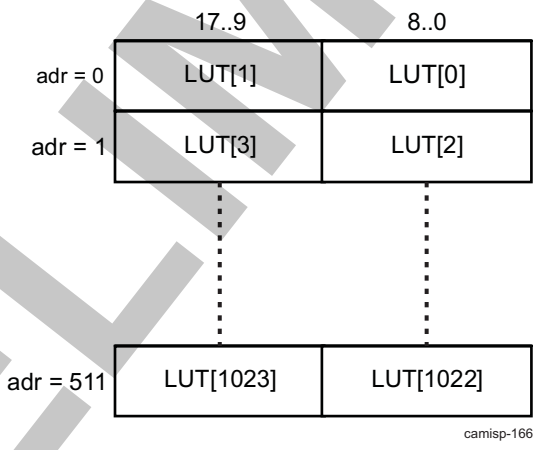

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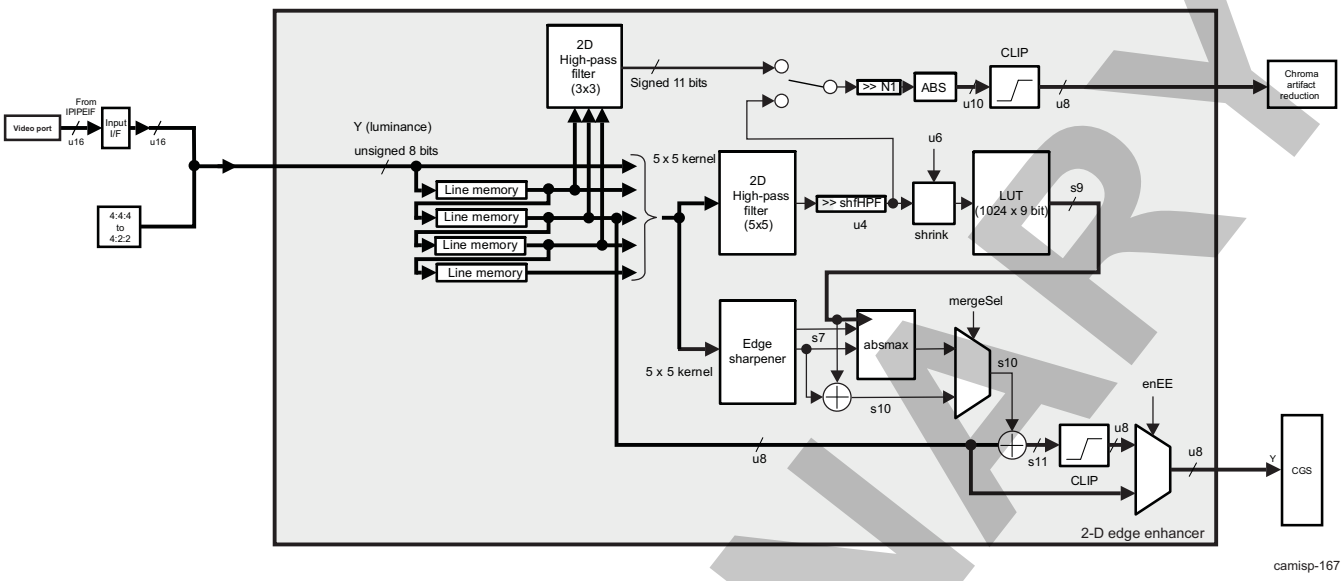
Figure 8-164. ISS ISP IPIPE 2D Edge-Enhancer Block Diagram



camisp-167

In edge sharpener mode, enabled when IPIPE_YEE_TYP[0] SEL = 1, edge clarity is enhanced without producing a halo artifact. In this module, edge intensity is derived by the 2D linear filter with fixed coefficients shown in Figure 8-165.

Figure 8-165. ISS ISP IPIPE Edge Sharpener Details

$$S_{i,j} = \begin{pmatrix} 0 & -1 & -2 & -1 & 0 \\ -1 & 0 & 2 & 0 & -1 \\ -2 & 2 & 8 & 2 & -2 \\ -1 & 0 & 2 & 0 & -1 \\ 0 & -1 & -2 & -1 & 0 \end{pmatrix}$$

$$sharpness(h,v) = \text{clip}\left(\text{shrink}\left(g \times \left(\left(\sum_{j=-2}^{2} \sum_{i=-2}^{2} S_{i,j} Y(h+i, v+j) \right) >> 3 \right), threshold_{LOW} \right) >> 6, -threshold_{HIGH}, threshold_{HIGH} \right)$$

camisp-663

The gain (g) and threshold values for the shrink/clip function ($threshold_{LOW}$, $threshold_{HIGH}$) are determined by the IPIPE_YEE_E_GAN, IPIPE_YEE_E_THR_1, and IPIPE_YEE_E_THR_2 registers. The bit width of g and $threshold_{HIGH}$ is in U6, and $threshold_{LOW}$ is in U12Q6.

This edge intensity is then clipped by a threshold value in the formula shown in Figure 8-166.

Figure 8-166. ISS ISP IPIPE 2D Edge-Intensity Clipping Formula

$$S_{\text{int}} = \begin{cases} clip(sharpness, -grad, grad) & \text{Halo reduction on} \\ sharpness & \text{Halo reduction off} \end{cases}$$

camisp-664

The threshold value (grad) is a function of the activity around the target pixel, which is derived from gradient values. Gain and offset are specified by IPIPE_YEE_G_GAN and IPIPE_YEE_G_OFT

Capping with gradient value prevents overly enhancing edges, and suppresses halo artifacts around edges.

The output from edge-enhancer and edge sharpener are merged with the function shown in Figure 8-167.

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Figure 8-167. ISS ISP IPIPE 2D Edge Enhancer and Sharpener Merger Formula

$$E_{merge} = \begin{cases} E_{\text{int}} + S_{\text{int}} & IPIPE\_YEE\_TYP[0]SEL = 0 \\ \text{absmax}(E_{\text{int}}, S_{\text{int}}) & IPIPE\_YEE\_TYP[0]SEL = 1 \end{cases}$$

$$\text{absmax}(x, y) = \begin{cases} x & abs(y) \le abs(x) \\ y & otherwise \end{cases}$$

camisp-666

The E_{merge} value is added to the Y input value to make the final output.

For Chroma suppression, another 2D high-pass filter (HPF) is implemented. One of the four coefficient sets shown in Figure 8-168 is selectable.

Figure 8-168. ISS ISP IPIPE 2D Edge Chroma-Suppression Coefficient Sets

$$\begin{pmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{pmatrix}, \begin{pmatrix} 0 & 0 & 0 \\ 1 & -2 & 1 \\ 0 & 0 & 0 \end{pmatrix}, \begin{pmatrix} 0 & 1 & 0 \\ 0 & -2 & 0 \\ 0 & 1 & 0 \end{pmatrix}, \text{ or } \begin{pmatrix} 0 & 1 & 0 \\ 1 & -4 & 1 \\ 0 & 1 & 0 \end{pmatrix}$$

camisp-667

At the end of the edge-enhancer process, brightness and contrast adjustment are applied to the Y signal. The formula shown in Figure 8-169 describes the process.

Figure 8-169. ISS ISP IPIPE 2D Edge-Brightness and Contrast Adjustments Formula

$$Y_{ctr\_brt} = \text{clip8}(\text{clip8}((Y_{EE} \times CTR) >> 4) + BRT)$$

$$\text{clip8}(x) = \begin{cases} x & x \le 255 \\ 255 & 255 < x \end{cases}$$

camisp-668

In the formula from Figure 8-169, Y_{EE} is the output (Y) of the Edge-Enhancer, as shown in Figure 8-164. CTR is a U8Q4 contrast enhancement factor (configured through the IPIPE_YUV_ADJ[7:0] CTR bit field), BRT is a U8 brightness enhancement factor (configured through the IPIPE_YUV_ADJ[15:8] BRT bit field), and Y_{CTR_BRT} is the output with brightness and contrast adjustment applied.

8.3.3.3.12 ISS ISP IPIPE Histogram

NOTE: The boxcar function can be used simultaneously with the histogram function if needed.

NOTE: For the locations of histogram memory access, see Section 8.3.3.8, *ISS ISP Memory Mapping*.

The histogram module counts the number of pixels that have a value in a region and can be enabled from the IPIPE_HST_EN[0] EN bit. Moreover, if enabled, the IPIPE_HST_MODE register can be set to work constantly or one time. If the IPIPE_HST_MODE[0] OST bit is set to 1, the histogram is disabled by clearing the IPIPE_HST_EN[0] EN bit to 0 after one run (one-shot mode).

After enabling the module, the following features are available:

- The data to be summed is taken from the DPC memory or RGB2YCbCr module. The choice is made in the IPIPE_HST_SEL[2] SEL bit.
- When data are collected from the DPC memory, the sampled colors are R/G/B/Y. Y is derived in the following method:

  Y = (HST_MUL_R*R + HST_MUL_GR*Gr + HST_MUL_GB*Gb + HST_MUL_B*B) (4)

  For the G histogram, Gb, Gr, or the average is used, through the IPIPE_HST_SEL[1:0] TYP bit field.
- Two sets of 512 × 20-bit memory are used.

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- The number of bins can be set from 32 to 256 in the IPIPE_HST_PARA[13:12] BIN bit field.
- The number of regions (areas) from 1 to 4; each region can be enabled through IPIPE_HST_PARA[x] RGNx (where x = 0 to 3). The positions of the regions are defined in IPIPE_HST_x_VPS and IPIPE_HST_x_HPS, and the vertical and horizontal size are defined by IPIPE_HST_x_VSZ and IPIPE_HST_x_HSZ, respectively (where x = 0 to 3).
- The number of regions × the number of bins <= 256.
- Each region can be turned on/off counting.
- The regions have priority orders.
- Each region has its own start coordinate X/Y (12 bits) and horizontal/vertical sizes (12 bits)
- When regions are overlapped, the value in the overlapped region is accumulated only in the region with the highest priority.
- The number of colors to be counted is from 1 to 4. Each color in all regions can be turned off counting (the IPIPE_HST_PARA[7:4] bit field).
- The value of each pixel is down-shifted (0–11) before counting using the IPIPE_HST_PARA[11:8] SHF bit field.
- When the value of a bin reaches (2^{20} – 1), the value is saturated until the memory is cleared.
- Number of bins: 32, 64, 128, or 256

The histogram memory can be cleared at the VD signal. When the memory is cleared, the first line of each frame cannot be sampled by the histogram if the width of the frame is larger than 512. If the width of the frame is smaller than 512, the first ceil (512/width) lines cannot be collected, where ceil(x) is the smallest integer value above x. If the clearing function is not enabled, the histogram bins are accumulated over the previous values.

The histogram has two banks of memories, which can be switched alternatively. The two memory banks are slipped into four histogram memory tables. Only two tables can be used at a time: output memory tables 0 and 1, or tables 2 and 3. To initialize tables, set the IPIPE_HST_TBL[1] CLR bit to 1, and to select which set of tables to uses, switch the IPIPE_HST_TBL[0] SEL bit between 0 and 1.

A gain for each color can be applied using the IPIPE_HST_MUL_x registers, where x = R, GR, GB, or B.

8.3.3.3.13 ISS ISP IPIPE Boxcar

The boxcar module generates a boxcar by taking mosaic image data and averaging the red, green, and blue pixels in an 8 × 8 or 16 × 16 block to produce one red, green, and blue output, as shown in Figure 8-170 and in Figure 8-171. Here, similar to the histogram module, the boxcar is enabled from the IPIPE_BOX_EN[0] EN bit, and if the mode is set to run once (one shot) (IPIPE_BOX_MODE[0] OST = 1), the enable bit is cleared after the run. The size of the blocks is determined from the IPIPE_BOX_SHF[0] SEL bit, where if set to 0 = 8 × 8, and 1 = 16 × 16.

The result of this operation is a full-color image with (1/64) or (1/256) area of the original image. The maximum input horizontal width is 8190 pixels when a 16 × 16 block is used; the width is 4096 when an 8 × 8 block is used. Also, the image size (width and height) must be a multiple of 16 for a 16 × 16 block, and a multiple of 8 for an 8 × 8 block. Boxcar operation works on 12-bit Bayer data and outputs 16-bit data. The output data is 48-bit RGB data for each 8 × 8 or 16 × 16 block. The 48-bit data is aligned in 64-bit format in SDRAM as shown in Figure 8-172. The first address of SDRAM access is specified by the IPIPE_BOX_SDR_SAD_H and IPIPE_BOX_SDR_SAD_L registers. The output data are written to SDRAM continuously line by line; there is no address offset between lines. After the image transfer of each frame completes, the ipipe_eof signal is sent to buffer logic. This signal is issued at the same timing as ipipe_int_dma.

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Figure 8-170. ISS ISP IPIPE Boxcar Operation (8 × 8 Block)

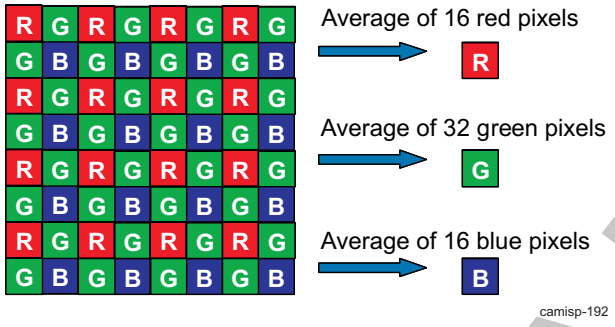


Figure 8-171. ISS ISP IPIPE Boxcar Operation (16 × 16 Block)

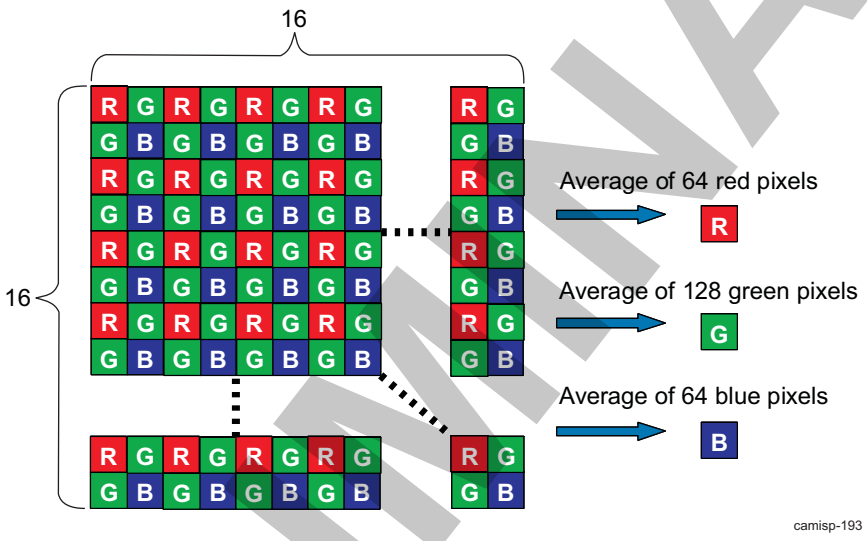
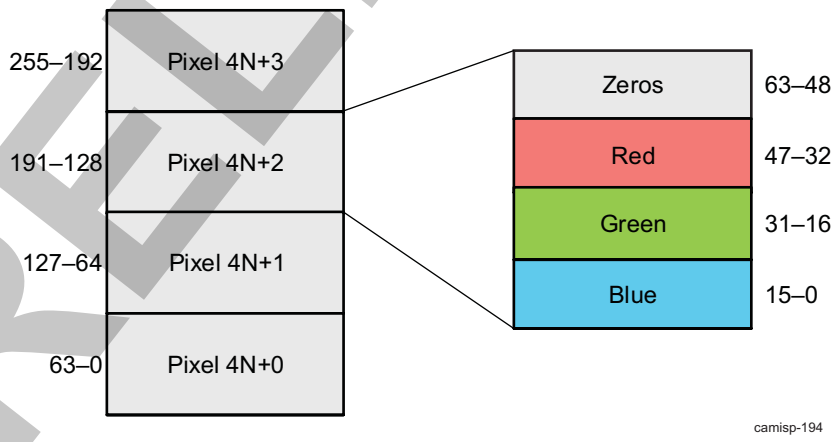


Figure 8-172. ISS ISP IPIPE Boxcar Data Packing in SDRAM



The right-shift value is specified by the IPIPE_BOX_SHF register, which has a range of 0 to 4. (The shift down is performed to fit the 20-bit accumulated value into 16-bit output.) For green signal processing, a divide-by-two operation rounds off the LSB.

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8.3.3.4 ISS ISP RSZ Functional Description

8.3.3.4.1 ISS ISP RSZ Overview

The RSZ module rescales images into various sizes ranging from x1/4096 scale-down to x16 scale-up. It also works in conjunction with the rotational engine (ROT) in SIMCOP for rotating images. The RSZ data slave interfaces support a parallel VP. The RSZ module can produce two output images simultaneously, because there are two independent resizer engines. The input data used by the two resizer engines is the same.

The RSZ module has the following capabilities:

- Input/output data formats:
  - Common input data for the two resizer engines
  - Independent output data formats for the two resizer engines
  - Supports YUV4:2:2 input and then supports YUV4:2:2/YUV4:2:0 or RGB5:6:5/ARGB32 output:
    - Output rates up to 304 MPix/s for YUV4:2:2/YUV4:2:0 or RGB5:6:5 output:
    - Output rates up to 243 MPix/s for ARGB32 output
  - Supports YUV4:2:0 input data and then supports only YUV4:2:0
    - YUV4:2:0 input format not supported natively:
      - Two passes required: Luma followed by Chroma or vice versa
        - Input and output rates up to 152 MPix/s in this configuration (YUV4:2:0)
      - Only supported from memory to memory
  - Supports RAW Bayer input and RAW Bayer output:
    - RAW format invariant. Takes whichever RAW format at the input and writes it out unmodified: 16 bits are read, 16 bits are written out.
    - No resizing can take place on RAW data.
- Resizer capabilities:
  - Input image cropping:
    - Common for the two resizer engines: Same input data before and after cropping
    - Supported on YUV4:2:2 and RAW data formats
    - Supported on pass-through mode data path
    - Supported on bypass mode data path
  - Dual resizer engines: RSZ-A and RSZ-B:
    - Up to x20 upsampling and x1/4096 downsampling on both engines
    - Up to 304-MHz pixel throughput on both resizer engines
    - Programmable data rate control to smooth the peak memory bandwidth
  - RSZ-A: Horizontal resolution of up to 8K pixels on RSZ-A
  - RSZ-B: Horizontal resolution of up to 8K pixels on RSZ-B
  - Independent Y and Cb/Cr phases on horizontal and vertical axis:
    - Enables to take care of different YUV4:2:0 phases used in different video formats
    - Enables frame division mode: Images can be stitched together with the right phase.
  - Rescaling: two modes supported:
    - Normal mode for upscale and downscale: Higher flexibility but lower downscale quality
    - Downscale mode for downscale only: Lower flexibility but higher downscale quality
  - Filtering: two modes supported:
    - Independent settings for the horizontal and vertical directions
    - 3-tap low-pass filter with 2-tap linear interpolation
    - 4-tap cubic interpolation
  - Flip support of the output image:

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    - Horizontal flip
    - Vertical flip
  - Pixel duplication on the top/bottom, left/right sides: Avoids losing pixels at the image boundaries because of the filtering
  - Support pass-through and bypass modes: Resizer engines bypassed:
    - Pass-through mode
      - RAW and YUV4:2:2 data support
      - Lower power consumption mode to transfer data to memory
      - Can transfer images larger than 8K pixels to memory
    - Bypass mode
    - RAW and YUV4:2:2 data support
    - Input buffer used. Can benefit from additional buffering in case the BL module memory is not big enough and back pressure occurs.
- Slave data interface: VP interface:
  - Two VP interfaces: The programming model selects which VP is used to input data to the RSZ module. Both VPs cannot be active simultaneously.
    - VP 1: Typically connected to the IPIPE module.
    - VP 2: Typically connected to the IPIPEIF module.
  - Up to 304-MHz pixel clock
- Master data interface:
  - Two interfaces to the BL module:
    - Up to 304 MHz
    - 32-bit-wide, 32-byte-long requests
    - Accesses are aligned on 32-byte boundaries.
    - Used to transfer data to memory
    - Each interface is dedicated to a single output image.
  - Addressing modes:
    - Linear
    - Circular
- Configuration interface:
  - Up to 152 MHz
  - 32 bits wide
  - Used to configure the resizer registers
- Power management: Independent clock domains for the two resizers (Each resizer engine can be gated off separately)
- Error management: FIFO overflow detection on the input buffers

Figure 8-173 show the RSZ module connections to other submodules of the ISP.

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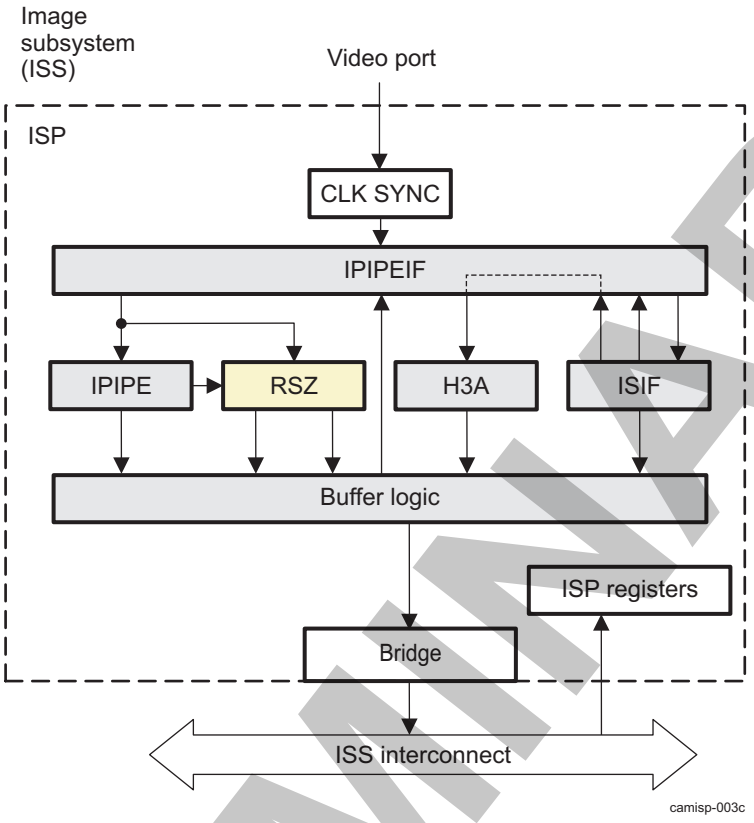
Figure 8-173. ISS ISP RSZ High-Level Diagram



8.3.3.4.2 ISS ISP RSZ Top-Level Block Diagram

Figure 8-174 is the top-level block diagram of the RSZ module. The RSZ module comprises the following submodules: cropping, input data buffering, data requestor, averager, data saturation, and resizer interpolation (comprised of horizontal rescaler, vertical rescaler, color conversion, and output interface) (see the following sections for more information).

The RSZ module comprises two independent resizer engines with the same capabilities (except for the memory line size). The input data can come from VP 1 or VP 2. Software must determine and control which interface is selected.

The RSZ module includes one VBUSP slave port, which is used to control the RSZ registers. It also includes two MTC master ports, which are used to pass the pixels to the BL. The BL in turn creates the burst requests to the memory subsystem (see Section 8.3.3.4.3, *ISS ISP RSZ Interfaces*).

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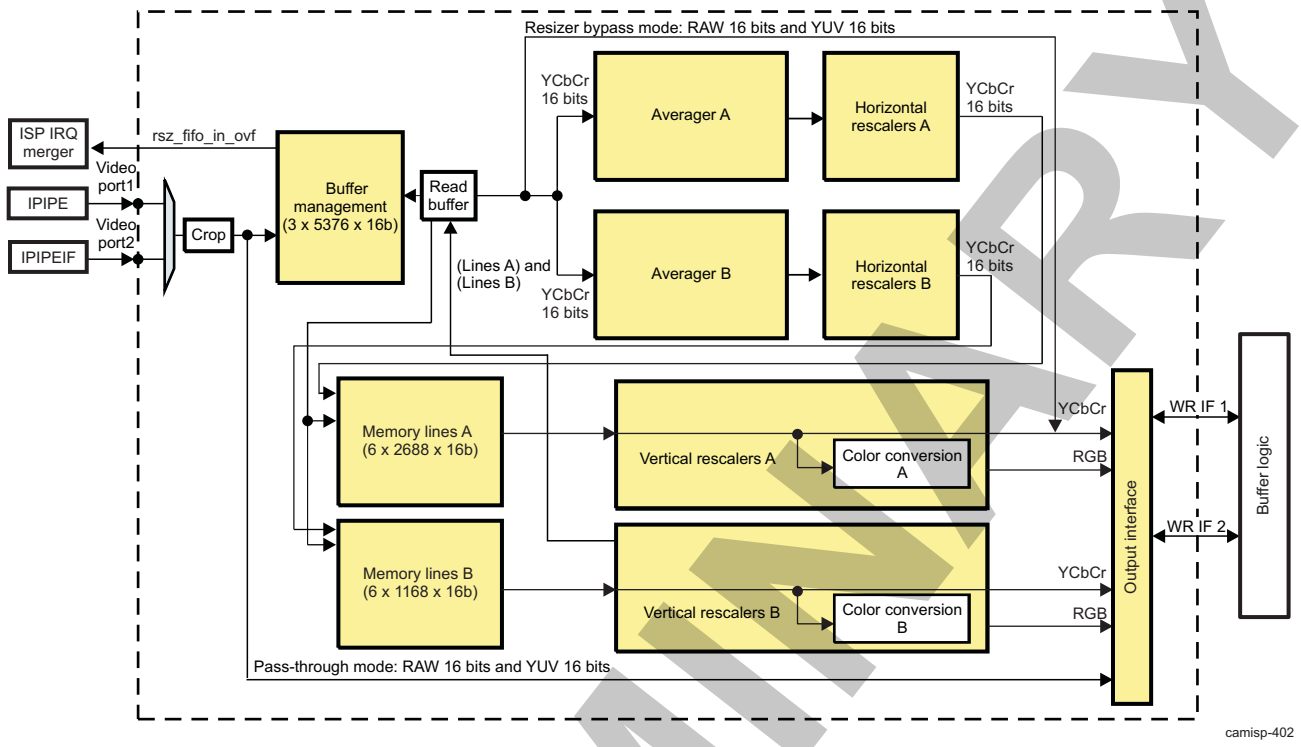
Figure 8-174. ISS ISP RSZ Top-Level Block Diagram



8.3.3.4.3 ISS ISP RSZ Interfaces

The RSZ module has the following data interfaces:

- One 32-bit read/write point-to-point pending VBUSP interface
- Two slave VP interfaces for transport YUV and RAW data
- Two MTC interfaces to BL for RSZ-A and RSZ-B, with only write capabilities

8.3.3.4.3.1 ISS ISP RSZ VBUSP Interface

The VBUSP interface is a 32-bit read/write capable interface. The VBUSP interface must be programmed in a way that back-to-back requests are possible for read and write. The RSZ_GCK_MMR[0] MMR bit enables the memory register access from the VBUSP interface to enable transfer and signal such as MMR request, direction, enable write/read data can be enabled.

8.3.3.4.3.2 ISS ISP RSZ Video Port Interfaces

The VP interfaces are slave interfaces; one is connected to IPIPE, and the other to IPIPEIF. These interfaces are for data transfer. Table 8-430 lists the format supported across IPIPE/IPIPEIF and RSZ. Signals coming from IPIPE and IPIPEIF can be write-enable signals. The RSZ_SRC_MODE[1] WRT bit is set whether or not the write enable signals are considered. This is a line-valid qualifier. This signal is sampled on the rising edge of HD, and the value is used for the full line.

Table 8-430. ISS ISP RSZ VP Supported Formats

	VP Signals: From IPIPE and IPIPEIF Modules (dat[15:0] Register)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
YUV4:2:2 16 bits	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cb7 Cr7	Cb6 Cr6	Cb5 Cr5	Cb4 Cr4	Cb3 Cr3	Cb2 Cr2	Cb1 Cr1	Cb0 Cr0

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Table 8-430. ISS ISP RSZ VP Supported Formats (continued)

YUV4:2:0 Y data	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Low	Low	Low	Low	Low	Low	Low	Low
YUV4:2:0 Cb/Cr data	Low	Low	Low	Low	Low	Low	Low	Low	Cb7 Cr7	Cb6 Cr6	Cb5 Cr5	Cb4 Cr4	Cb3 Cr3	Cb2 Cr2	Cb1 Cr1	Cb0 Cr0

NOTE: The formats are set from the IPIPE and IPIPEIF registers. For more information, see Section 8.3.3.3, *ISS ISP IPIPE Functional Description*, and Section 8.3.3.2, *ISS ISP IPIPEIF Functional Description*.

8.3.3.4.3.3 ISS ISP RSZ MTC Interfaces

The RSZ module includes two write-only MTC interfaces. Their implementation enables passing a maximum of eight 32-byte requests in 10 clock cycles. The RSZ must be programmed to obtain smooth and average bandwidth to buffer logic module by setting a minimum interval between two successive requests (set the RSZ_DMA_RZA[15:0] RZA and RSZ_DMA_RZB[15:0] RZB bit fields for the A and B resizers as appropriate). This setting is not expected to be dynamic. It can be a fixed setting from request to request and frame to frame. When the bandwidth is set appropriately, between the first valid translated pixel and the EOF signal sent to buffer logic, the RSZ_DMA_STA[0] STATUS bit can be seen, and it is high if the transfer over the MTC interfaces is active. Figure 8-175 shows how RSZ_DMA_RZx for resizers A and B affects the MTC data request generator.

Figure 8-175. ISS ISP RSZ MTC DMA Bandwidth Control

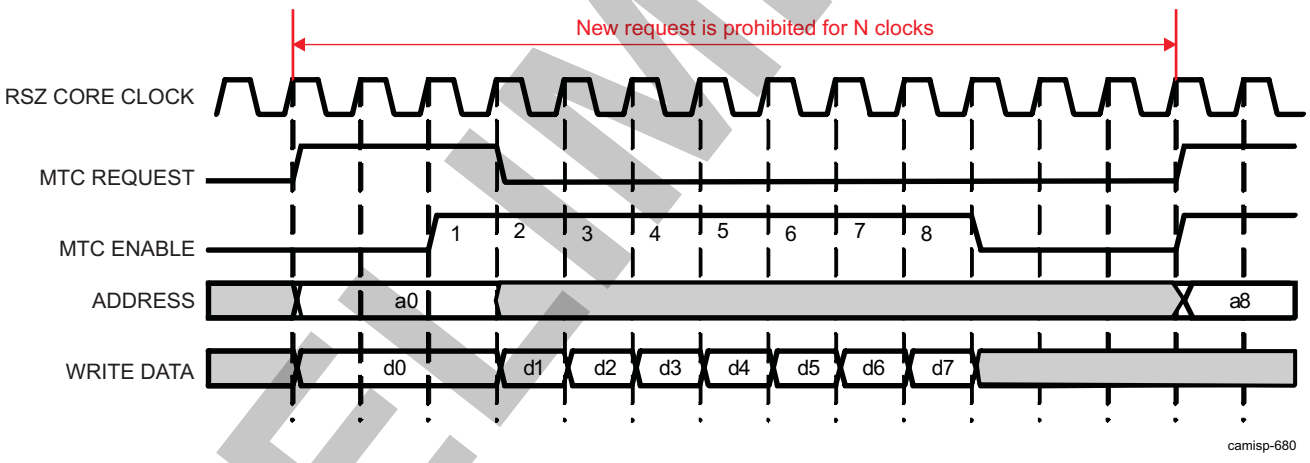

Figure 8-176 shows the pixel order in memory written by the MTC. The arrows do not represent the order in which data is written. Data are always written from left to right, whether horizontal reversal is enabled or not.

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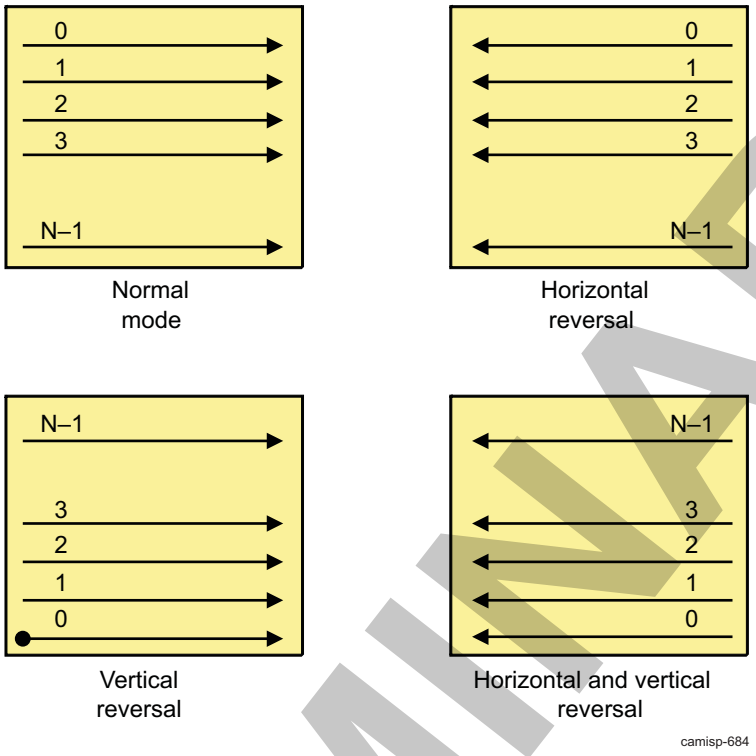
Figure 8-176. ISS ISP RSZ MTC Image Data Storage Pixel Order



The RSZ MTC interfaces can be stalled by the input MTC STALL signal. The assertion of the MTC STALL signal is a result of a hardware mechanism that monitors the CBUFF module to prevent its overflow. When this signal is asserted, the current 32-byte MTC request is finished and then the RSZ MTC output ports are stalled. For further details on the output ports, see Section 8.3.3.4.5.7, *ISS ISP RSZ Output Interface*.

8.3.3.4.4 ISS ISP RSZ Integration

Figure 8-177 shows how the VP and interfaces of the RSZ module are connected to surrounding modules at the ISP level. The RSZ module gets data from the IPIPEIF module or IPIPE module.

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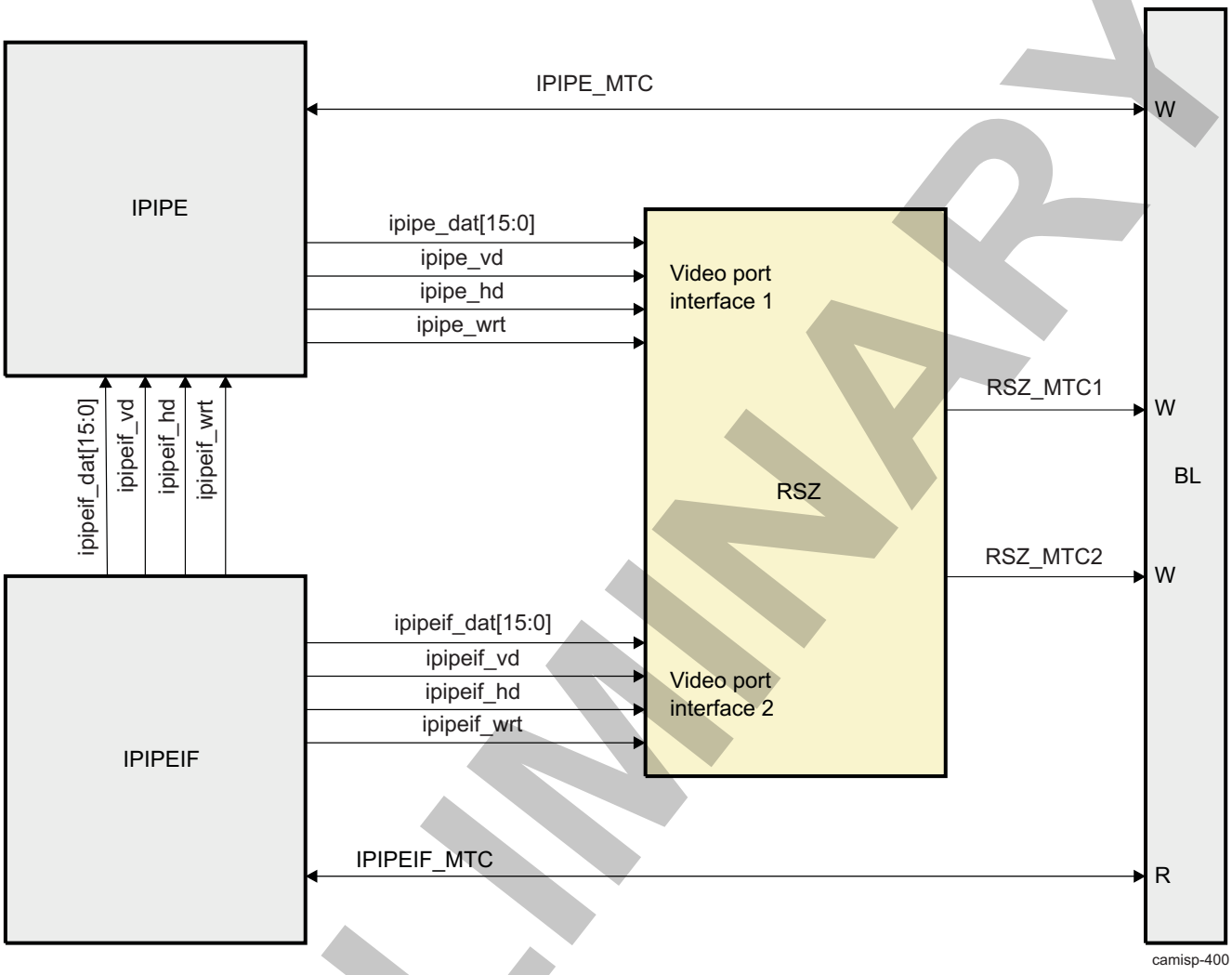
Figure 8-177. ISS ISP RSZ Typical Module Integration: High-Level Summary



The following constraints apply to the RSZ module:

- The data coming from the IPIPEIF module can be RAW or YUV4:2:2 data. Because the RSZ module can rescale only YUV4:2:2 data, the RSZ module must be configured in pass-through mode when RAW data is received on VP 2. It is possible to bypass the resizer engine if YUV4:2:2 data is sent but rescaling is not needed (bypass mode).
- The data coming from the IPIPE module can be RAW or YUV4:2:2 data. Eventually, YUV4:2:0 data can be sent through this path, but the data must be sent in two passes. Because the RSZ module can rescale only YUV4:2:2 data, the RSZ module must be configured in pass-through mode when RAW data is received on VP 1. It is possible to bypass the resizer engine if YUV4:2:2 data is sent but rescaling is not needed (bypass mode).

VP 2 provides a way to bypass the IPIPE module when YUV4:2:2 data is received from the images sensor or when YUV4:2:2 is read back from memory with the CCP2 RX or ISIF module.

Table 8-431 summarizes the different RSZ configuration possibilities as a function of the input data format.

Table 8-431. ISS ISP RSZ Data Flow vs. Input Data Format Constraints

VP 1 Data Format	VP 2 Data Format	RSZ-A Configuration	RSZ-B Configuration	Comments
RAW	N/A	Disabled	Disabled	RSZ module in pass-through mode or bypass mode

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Table 8-431. ISS ISP RSZ Data Flow vs. Input Data Format Constraints (continued)

VP 1 Data Format	VP 2 Data Format	RSZ-A Configuration	RSZ-B Configuration	Comments
N/A	RAW	Disabled	Disabled	RSZ module in pass-through mode or bypass mode
YUV4:2:2	N/A	Disabled	Disabled	RSZ module in pass-through mode or bypass mode
YUV4:2:2	N/A	Enabled	Disabled	One output image
YUV4:2:2	N/A	Disabled	Enabled	One output image
YUV4:2:2	N/A	Enabled	Enabled	Two output images
N/A	YUV4:2:2	Disabled	Disabled	RSZ module in pass-through mode or bypass mode
N/A	YUV4:2:2	Enabled	Disabled	One output image
N/A	YUV4:2:2	Disabled	Enabled	One output image
N/A	YUV4:2:2	Enabled	Enabled	Two output images

8.3.3.4.5 ISS ISP RSZ Functional Description

To start up, the RSZ configuration can be set from the RSZ_SYSCONFIG register, which provides enabling the RSZ-A and RSZ-B clocks. The RSZ module does not have stand-alone reset and status check. Software reset must be done at the ISP level. Moreover, when enabled, the RSZ module can control the input data buffer, and when the rsz_stall_input signals are set from the RSZ_IN_FIFO_CTRL register, the RSZ module generates a stall signal that can be used by the master module sending data to the RSZ module when the data threshold is too high.

The RSZ_SRC_EN[0] EN bit starts the resizer processing. If the processing mode is set to one shot (one run and then turn off) from the RSZ_SRC_MODE[0] OST bit, the EN bit is cleared to 0.

The RSZ module can be configured to be bypassed in certain cases (see Figure 8-177 for the module constraints) from the RSZ_SRC_FMT0[1] BYPASS bit. The data can be sent directly from here to the output interface (bypass mode) or imported to the module buffer, but not manipulated and sent to the output interface (pass-through mode). The master device sending data to the RSZ can be switched between IPIPEIF and IPIPE using the RSZ_SRC_FMT0[0] SEL bit. The RSZ understanding of the data input is set from the RSZ_SRC_FMT1 register (for more information, see Table 8-433). The RSZ_SEQ.VRVX and RSZ_SEQ.HRVX registers can be set to flip the image horizontally or vertically, respectively (see Figure 8-176).

Depending on the mode to which the RSZ is set, the core clock can be enabled from the RSZ_GCK_SDR register. Table 8-432 summarizes the behavior of the RSZ module for the different settings.

Table 8-432. ISS ISP RSZ Module Modes: Register Settings

Configuration Number	RSZ_SRC_EN	RZA_EN	RZA_CLK_EN	RZB_EN	RZB_CLK_EN	RSZ_GCK_SDR.CORE	RSZ_SRC_FMT0.BYPASS	Comments
0	0	X	X	X	X	X	X	Data cannot go through the RSZ module.
								Interrupts are not issued.
1	1	0	X	0	X	1	0	RSZ-A is disabled.
								RSZ-B is disabled.
								It is best to have RZA_EN = RZB_EN = 0 to save power, but RZA_EN = RZB_EN = 1 is also supported.
								This configuration is supported but does not make sense because data cannot go through the module.
2	1	1	1	0	X	1	0	RSZ-A is enabled.
								RSZ-B is disabled.

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Table 8-432. ISS ISP RSZ Module Modes: Register Settings (continued)

								It is best to have RZB_EN = 0 to save power, but RZB_EN = 1 is supported as well.
3	1	0	X	1	1	1	0	RSZ-A is disabled.
								RSZ-B is enabled.
								It is best to have RZA_EN = 0 to save power, but RZA_EN = 1 is also supported.
4	1	1	1	1	1	1	0	Resizer A is enabled.
								Resizer B is enabled.
5	1	X	X	X	X	0	0	Bypass mode is enabled.
								Resizer core functional clock is disabled.
6	1	X	X	X	X	0	1	Pass-through mode enabled.
								Resizer core functional clock is disabled.
7	1	X	X	X	X	1	1	Pass-through mode is enabled.
								Resizer core functional clock is enabled.
								Not a preferred configuration. Configuration 6 saves power.

Table 8-433. ISS ISP RSZ Module Input Control: Register Settings

RSZ_SRC_FMT1.IN420	RSZ_SRC_FMT1.COL	Comments
0	X	YUV4:2:2 input. Chroma is co-sited.
1	0	YUV4:2:0 input. Valid data is Y, C is dummy. On the VP, YUV4:2:2 data is always assumed.
1	1	YUV4:2:0 input. Valid data is C, Y is dummy. On the VP, YUV4:2:2 data is always assumed.

The RSZ_YUV_PHS[0] POS bit sets the Chroma output. The RSZ module does not change the relative position of the Chroma samples versus the Luma samples between the input and output, and the Chroma position at the output of the IPIPE module and at the output of the RSZ module must be identical. In other words, RSZ_YUV_PHS.POS = IPIPE_YUV_PHS.POS.

Settings are common for both resizer engines inside the RSZ module. Each engine (RSZ-A or RSZ-B) can be enabled from the RZx_EN register: select the mode from RZx_MODE, and select the input and output in the YUV color scheme from the RZx_420 register (valid only if YUV4:2:2 is the input set from RSZ_SRC_FMT1.IN420). Table 8-434 summarizes the combination of settings available in the RZx_420 register.

Table 8-434. ISS ISP RSZ-A/RSZ-B Output Format Selection

RZx_420.YEN	RZx_420.CEN	Comments
0	0	Input is YUV4:2:2. Output is YUV4:2:2 if RZX_RGB_EN = 0 and RGB if RZB_RGB_EN = 1.
0	1	Input is YUV4:2:2. Output is the Chroma of YUV4:2:0. RZX_RGB_EN is ignored. Must be used to rescale YUV4:2:0 data: First/second pass
1	0	Input is YUV4:2:2. Output is the Luma of YUV4:2:0. RZX_RGB_EN is ignored. Must be used to rescale YUV4:2:0 data: Second/first pass
1	1	Input is YUV4:2:2. Output is YUV4:2:0. RZX_RGB_EN is ignored.

8.3.3.4.5.1 ISS ISP RSZ Operating Modes

The RSZ module offers two basic rescaling modes. These modes are not built-in but are particular configurations, which means that other hybrid modes can be programmed. The normal mode provides more flexibility (the rescale ratio granularity is smaller) than downscale mode, but downscale mode produces better image quality (averager performs anti-aliasing):

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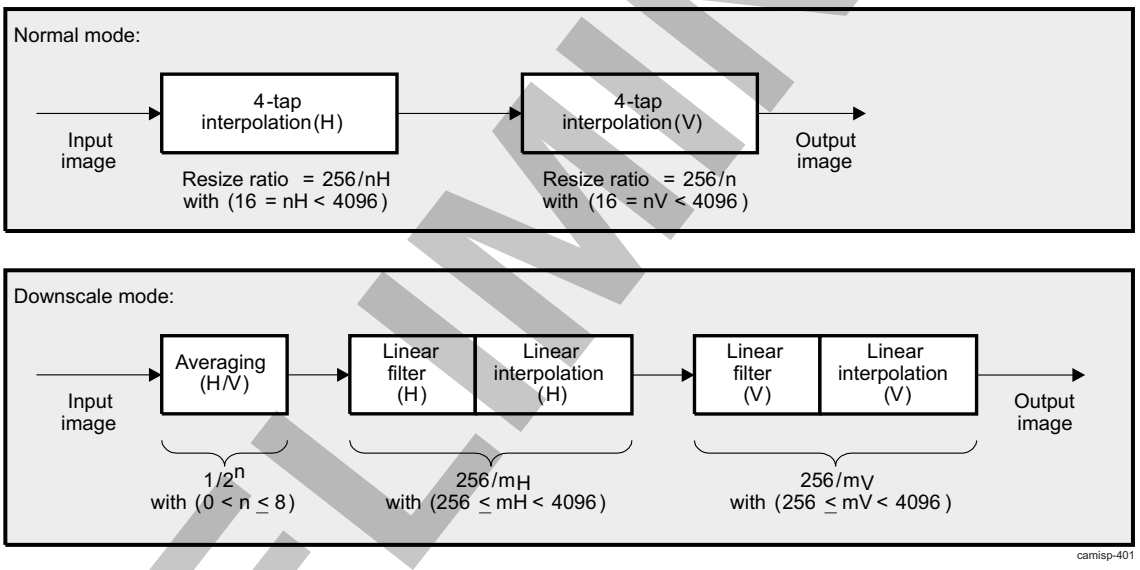
- Normal mode: The scaling process is carried out using interpolation with a 4-tap filter. The interpolation method is a 4-tap cubic convolution or a 3-tap linear filter + 2-tap linear interpolation. The user controls the type of interpolation that is used. The possible rescale ratios range from 1/16x to 20x.
- Downscale mode: The scaling process is the same as for normal mode, but an averaging function is placed before. It enables reaching much higher reduction factors while avoiding anti-aliasing artifacts. The interpolation method is a 4-tap cubic convolution or a 3-tap linear filter + 2-tap linear interpolation. The possible rescale ratios range from 1/4096x to 1x.

NOTE: The selection of the mode is independent for each resizer engine. One resizer engine can be configured in normal mode, while another is configured in downscale mode.

The RSZ module can produce two output images simultaneously, because there are two independent resizer engines. The input data used by the two resizer engines is the same. The RSZ output image sizes are limited to RSZ_GNC[12:0] RSZA_MEM_LINE_SIZE pixels/line for RSZ-A (5376 pixels/line) and RSZB_MEM_LINE_SIZE[28:16] for RSZ-B (2336 pixels/line).

Figure 8-178 shows the RSZ operating modes. Nothing prevents the use of linear interpolation in normal mode or bicubic interpolation in downscale mode; similarly, it is possible to mix the interpolation modes for horizontal and vertical filtering. This is fully programmable.

Figure 8-178. ISS ISP RSZ Operating Modes



8.3.3.4.5.1.1 ISS ISP RSZ Operating Modes and Maximum Input Clock

The maximum output pixel clock on both resizers is 304 MHz (OPP_NOM); that is, a pixel throughput of 304 MPix/s. Moreover, hardware takes care of the following constraints:

- When both resizer engines are configured to perform downscaling, there is no particular constraint on the VP pixel clock. The VP pixel clock can be as high as 304 MHz.
- When one resizer engine is configured to perform upscaling and the second resizer engine is configured to perform downscaling, the VP pixel clock must be limited. The VP must be lower than:

clk_pix <= (304 MHz/(Vertical Upscale Ratio × Horizontal Upscale Ratio)) (5)

For example, if a 4x upscale ratio happens horizontally and vertically, then the input pixel clock must be lower than 304/(4 × 4) = 19 MHz.

It is the reason why it is not possible to perform digital zoom upscaling on the fly. It is necessary to acquire the pixels to memory first and to read them back at a pace that does not exceed the previously discussed constraints. At the ISS level, data can be read back from memory from the CCP2 RX or ISIF module.

- When the two resizer engines are configured to perform upscaling, the VP pixel clock must be limited.

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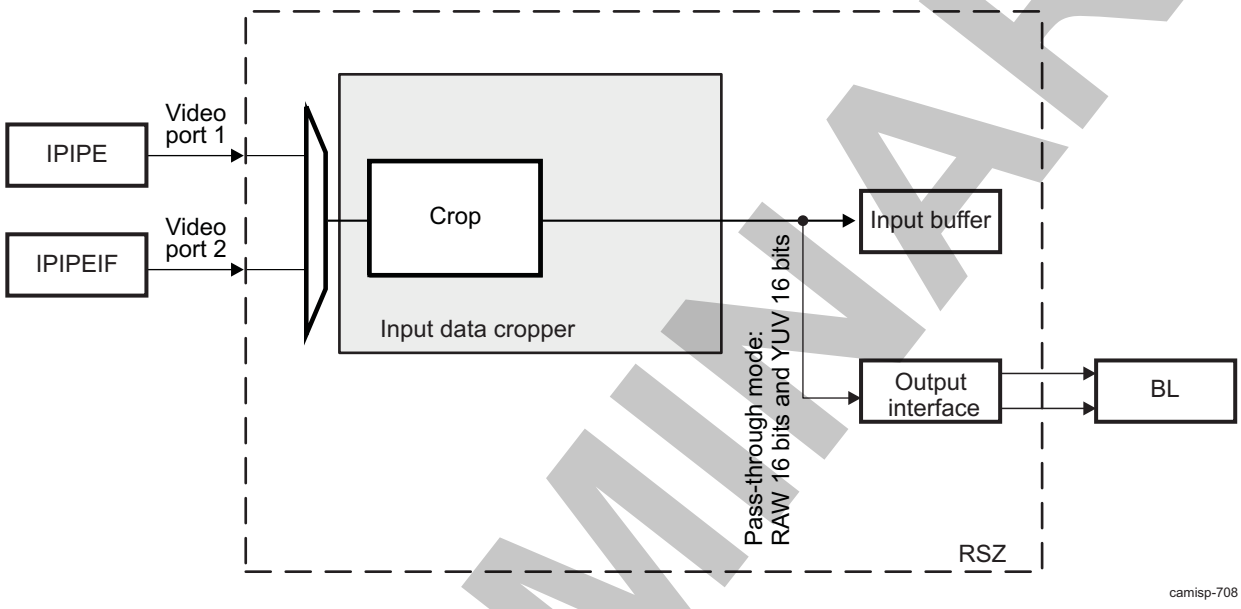
In that case, the VP frequency is limited by the resizer engine having the larger rescale ratios.

8.3.3.4.5.2 ISS ISP RSZ Input Data Cropper

The data coming from the VPs into the RSZ module can be cropped: this applies to RAW and YUV4:2:2 data. It is mandatory to crop the data as early as possible in the RSZ processing pipeline to reduce power consumption. It is mandatory to crop the data before storing it in the input data buffer. Figure 8-179 is the block diagram of the RSZ input data cropper.

Figure 8-179. ISS ISP RSZ Input Data Cropper Block Diagram



The input data are in YUV4:2:2 interleaved format or RAW format.

For YUV4:2:2 format, the data come as Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc. Y denotes the Luma component value and Cb/Cr denotes the Chroma component values. There are as many Y components as Cb/Cr components per line.

Figure 8-180 shows input data cropping. Only the cropped data is stored in the input data buffer. The names used in the figure correspond to the register names. If no cropping is desired, the RSZ_SRC_HPS and RSZ_SRC_VPS registers, which set the horizontal and vertical positions, respectively, must be set to 0; the start size from the RSZ_SRC_HSZ register must be set to the input image width minus 1, and the RSZ_SRC_VSZ register must be set to the input image height minus 1. These are common settings for both resize engines inside the RSZ module. After setting, more flexibility is present through the RZx_i_VPS and RZx_i_HPS registers for vertical and horizontal positioning, respectively, of the input/output (where x = A or B, i = I or O).

NOTE: After the RSZ second level cropping (defined by RZA_I_VPS and RZB_I_VPS register settings), the height of the image frame must be two lines or larger. A one-line image is not allowed.

Depending on the input data format, different constraints apply to the registers that set the cropping parameters:

- For YUV4:2:2 format, the vertical start positions of the cropped frame can be even or odd. However, the horizontal start position must be even: the reason is to always start with the same pattern: Cb_{2n}, Y_{2n}, Cr_{2n}, Y_{2n+1},etc. For the same reason, the horizontal size of the cropped frame (RSZ_SRC_HSZ + 1) must be an even number. Finally, the vertical size of the cropped frame can be odd or even.
- For RAW format, the vertical start position of the cropped frame can be even or odd. The vertical size can be even or odd. The horizontal resolution must be even.

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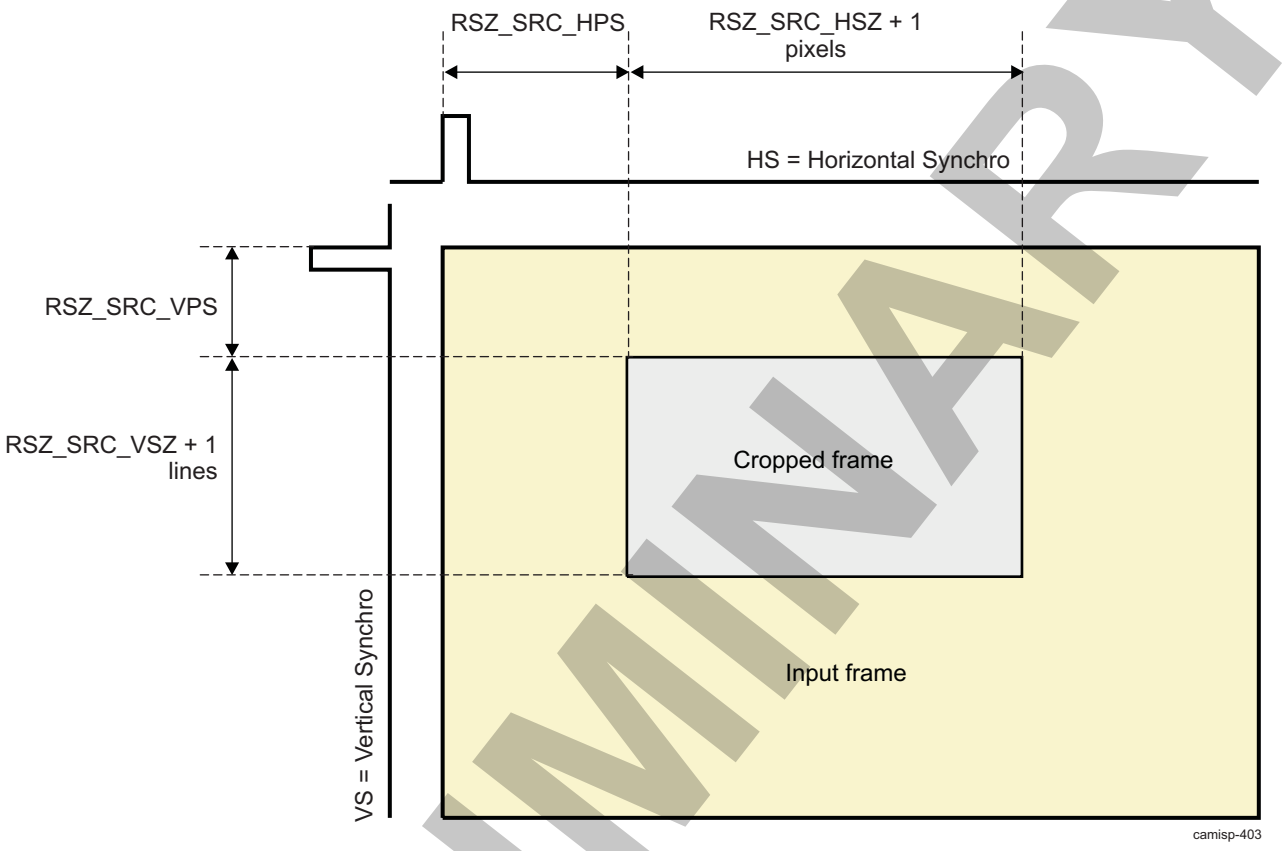
These features and constraints are common for both resizer engines inside the RSZ module. Figure 8-180 shows the input data cropping.

Figure 8-180. ISS ISP RSZ Input Data Cropping



8.3.3.4.5.3 ISS ISP RSZ Averager

8.3.3.4.5.3.1 ISS ISP RSZ Use Cases

The two resizer engines can have independent averager settings:

- Both resizers can use the averager.
- One resizer can bypass it and the other can use the averager.
- Both resizers can bypass the averager.

8.3.3.4.5.3.2 ISS ISP RSZ Memory Use

Vertical averaging requires memory to perform pixel data accumulation. It shares the vertical memory lines that are used for vertical filtering: this is the reason why the vertical memory lines are organized as two banks of half lines.

- The averagers output lines that are at most half the size of the input image in one memory bank.
- The horizontal resizers write their output data in the second memory banks.

Figure 8-181 shows the use of memory when the averager is enabled or disabled.

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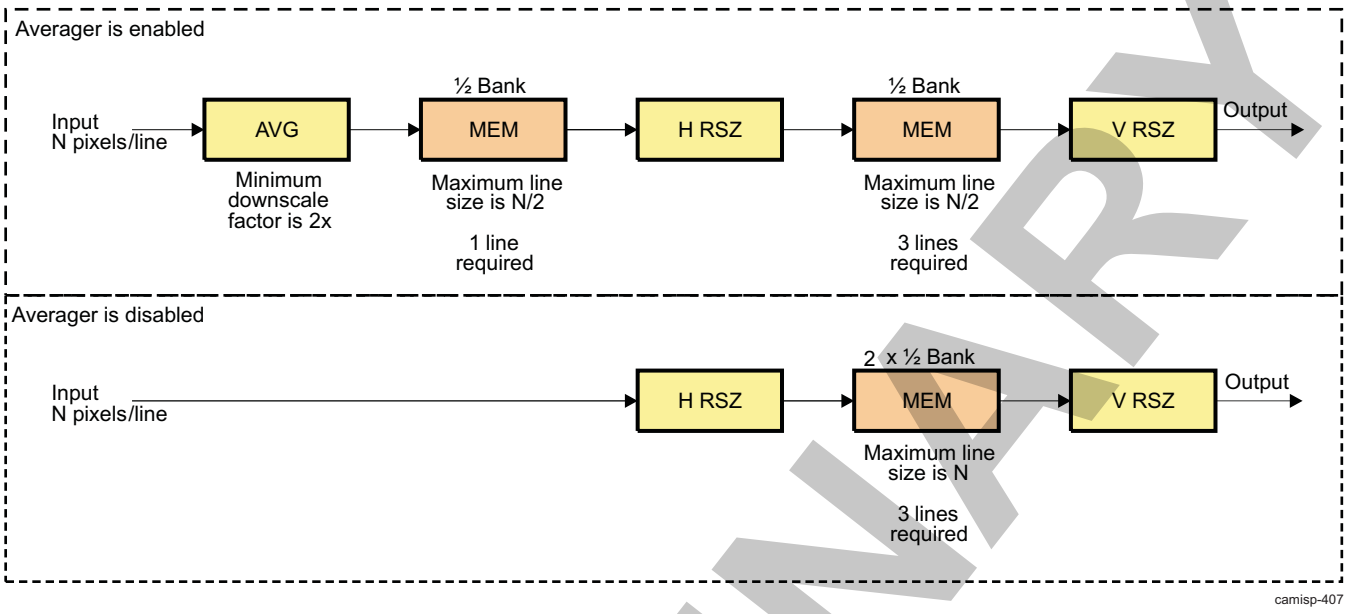
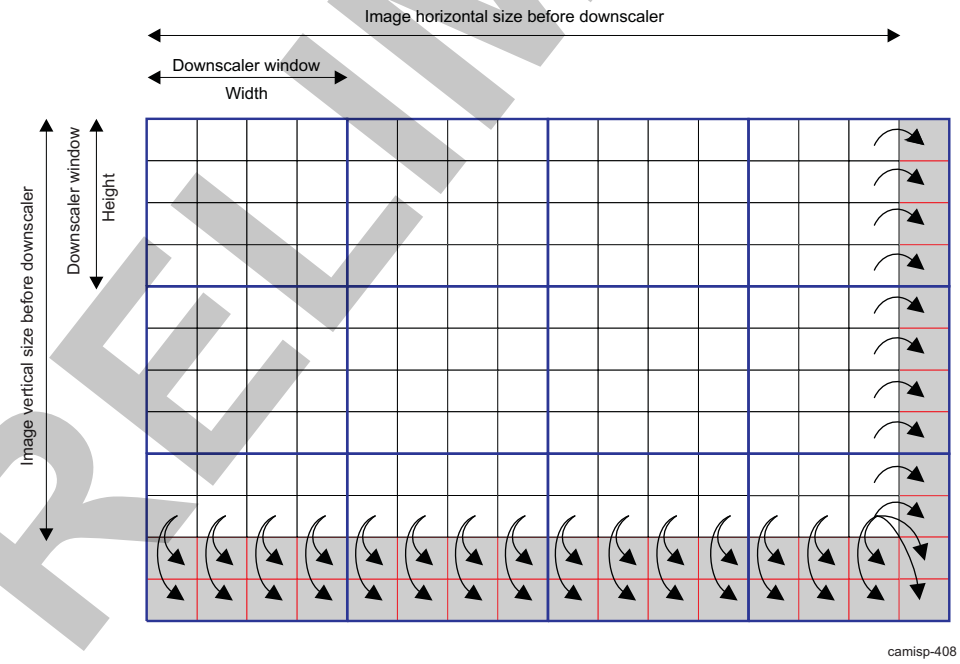
Figure 8-181. ISS ISP RSZ Averager Memory Utilization



8.3.3.4.5.3.3 ISS ISP RSZ Border Conditions

Figure 8-182 shows the averager behavior for border conditions. If the input image is not big enough, border duplication must occur.

Figure 8-182. ISS ISP RSZ Averager Border Conditions



Downscaling is enabled from the RZi_DWN_EN register. Moreover, the vertical averaging size is set by the RZA_DWN_AV[5:3] V bit field. The actual downscale ratio is given by $1/2^{(RZA\_DWN\_AV[5:3]\ V\ +1)}$. The range is from 1/2 to 1/256 in power of 2. The horizontal averaging size is set by the RZA_DWN_AV[0:2] H bit field. The actual downscale ratio is given by $1/2^{(RZA\_DWN\_AV[5:3]\ H\ +1)}$. The equations are the same for RSZ-B. The range goes from 1/2 to 1/256 in power of 2.

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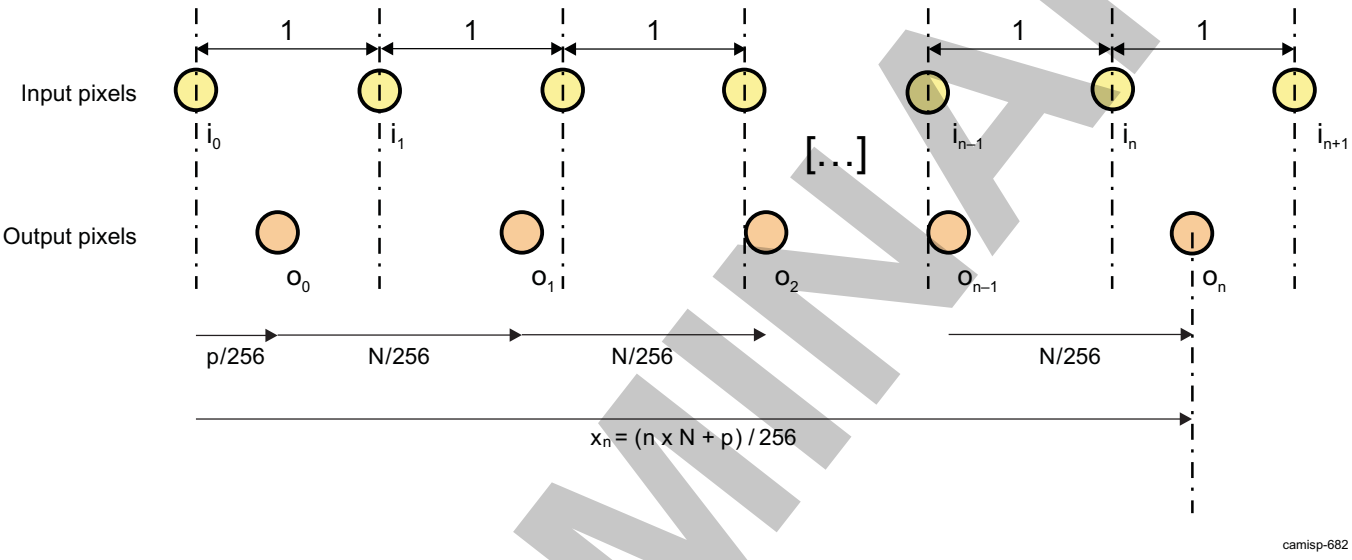
8.3.3.4.5.4 ISS ISP RSZ Interpolation

Figure 8-183 shows the basic interpolation method used in the RSZ module. The following assumptions are made:

- The distance between each input pixel is 1.
- The magnification ration is given by 256/N and p/256 is the initial phase of the output data.

The output pixels are also evenly spaced. The distance between each output pixel is given by N/256. In the example in Figure 8-183, N is greater than 256. The position of the nth output pixel is given by (n × N + p) / 256.

Figure 8-183. ISS ISP RSZ Basic Interpolation Method



Assuming the intensity of input pixels is i_0, i_1, i_2, etc. and the resized (output) pixels are o_0, o_1, o_2, etc., the nth output pixel (o_n) is determined using the nearest 4 input pixels as follows:

$o_n = h(1 + d) \times i_1 + h(d) \times i_m + h(d - 1) \times i_{m+1} + h(d - 2) \times i_{m+2}$

In the previous equation h(x) is the interpolation main function. The RSZ module supports linear and bicubic convolution interpolation functions.

Figure 8-184 shows the interpolation principle at the nth output pixel (o_n) at position x_n. Furthermore, the m and d parameters are as follows:

m = floor((n × N + p) / 256) and d = ((n × N + p) / 256) – m

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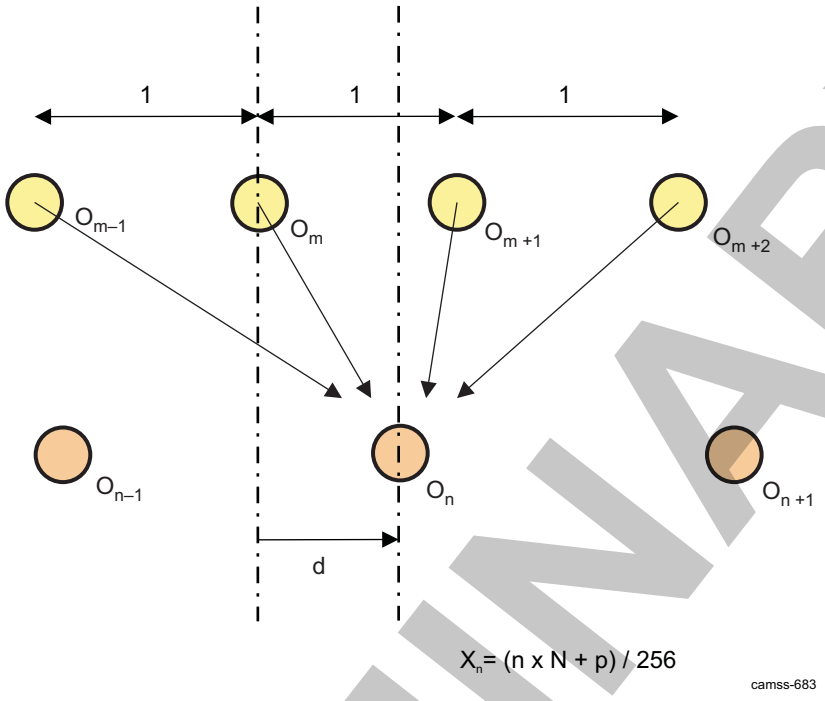
Figure 8-184. ISS ISP RSZ Interpolation Filtering



For each resizer (RSZ-A or RSZ-B), and for Chroma and Luma, the interpolation method for vertical interpolation can be a 2-tap linear interpolation or a 4-tap cubic convolution (default) method. The choice is made in RZi_V_TYP[0] Y for Luma and RZi_V_TYP[1] C for Chroma, where i = A or B and is the resizer number. It is similar for horizontal interpolation from RZi_H_TYP[0] Y for Luma and RZi_H_TYP[1] C for Chroma, where i = A or B and is the resizer number.

8.3.3.4.5.4.1 ISS ISP RSZ Liner Interpolation Input Data

Before data interpolation, a low pass filtering (LPF) operation is required on the input data. The following equation gives the LPF function. The equation is evaluated at pixel position d_i but neighbor pixels d_{i-1} and d_{i+1} are required. The gain value g is set up by the register RZi_V_LPF and RZi_H_LPF. Different gains are possible horizontally and vertically as well as for Luma and Chroma.

$LPF_g (d_{i-1}, d_i, d_{i+1}) = d_i + g \times (d_{i-1} - 2d_{i+1} + d_{i+2})/128$

8.3.3.4.5.4.1.1 ISS ISP RSZ Cubic Convolution Mode

The input data is not modified in bicubic mode. The input is equal to the output.

8.3.3.4.5.4.1.2 ISS ISP RSZ Phase Settings

The initial value for the phase value for vertical resizing is set by the RZi_V_PHS_Y for Luma and RZi_V_PHS_C for Chroma. These values are in the U14Q8 fractional format (values in the range [0 – 63.996]). When YUV4:2:2 data are output, the phase value for Luma and Chroma must be aligned; that is, RZi_V_PHS_Y = RZi_V_PHS_C.

The following constraint equation applies: | RZi_V_PHS_Y –RZx_V_PHS_C | <= RZi_V_DIF. This constraint means that at most the distance between the initial phases for Luma and Chroma is not expected to exceed the distance between two Luma pixels. The absolute value is used; therefore, the initial Luma phase can be greater than the initial Chroma phase or vice versa. As a reminder, the distance between two output pixels for Luma is given by RZi_V_DIF.

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The initial value for the phase value for horizontal resizing is set by the RZi_H_PHS register. The RZi_H_PHS_ADJ register enables adjusting the horizontal phase for the Luma component when averaging is enabled (the averager disrupts the relative sampling point between Luma and Chroma when YUV4:2:2 co-sited data is input). The relative phase between Luma and Chroma is different before and after the horizontal averager. The vertical phase is not affected by the averager. Figure 8-185 shows the effect of the averager on the phases. RZi_H_PHS_ADJ is expected to be equal to 0 if the averager is disabled.

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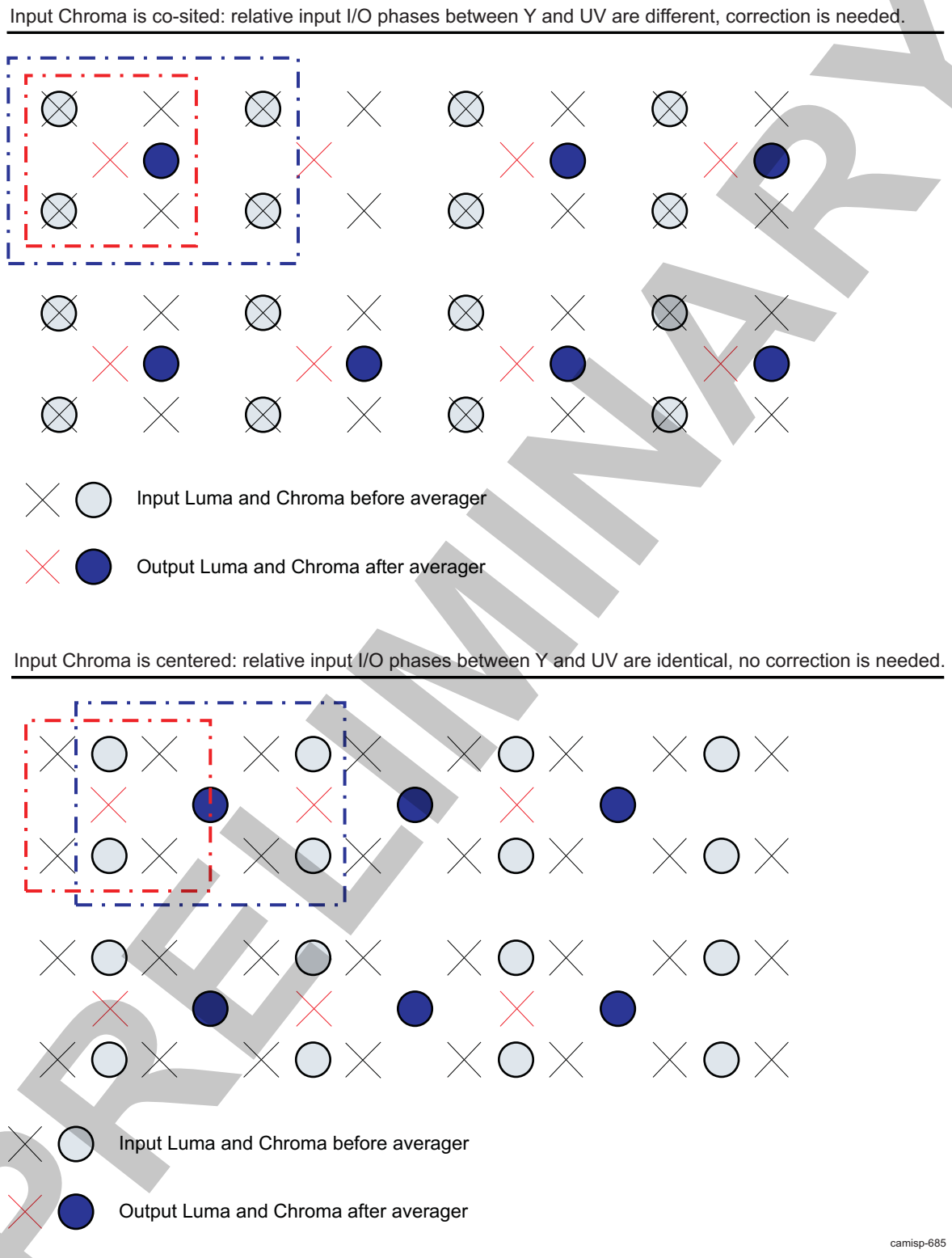
Figure 8-185. ISS ISP RSZ-A/RSZ-B Phase Averager Effect



8.3.3.4.5.5 ISS ISP RSZ Data Saturator

After vertical rescaling and before color conversion, the output data is saturated (clipped) to programmable values that are given by the following registers:

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- RSZ_YUV_Y_MIN
- RSZ_YUV_Y_MAX
- RSZ_YUV_C_MIN
- RSZ_YUV_C_MAX

The maximum Y value is set up with the RSZ_YUV_Y_MAX register. If the input Y value is greater than the MAX value, it is clipped to MAX.

The minimum Y value is set up with the RSZ_YUV_Y_MIN register. If the input Y value is smaller than the MIN value, it is clipped to MIN.

The maximum Cb/Cr value is set up with the RSZ_YUV_C_MAX register. If the input Cb/Cr value is greater than the MAX value, it is clipped to MAX.

The minimum Cb/Cr value is set up with the RSZ_YUV_C_MIN register. If the input Cb/Cr value is smaller than the MIN value, it is clipped to MIN.

8.3.3.4.5.6 ISS ISP RSZ Color Converter

As mentioned previously, the resizer can support RAW, YUV4:2:0, and YUV4:2:2 formats. The resizer engines can also support RGB output: RGB5:6:5 and ARGB32.

The RGB5:6:5 data is 16 bits wide and consists of 5 bits for red, 6 bits for green, and 5 bits for blue.

The following table shows the way RGB5:6:5 is stored to memory. This data format is compatible with the display controller. Only the little-endian memory representation is supported.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R1					G1						B1					R0					G0							B0				

The ARGB32 data is 32 bits wide and consists of 8 bits for alpha, 8 bits for red, 8 bits for green, and 8 bits for blue. The alpha value is global and is set for the entire frame; registers control the alpha value: the RZx_RGB_BLD register controls the alpha values of resizer A and resizer B.

The following table shows the way ARGB32 is stored to memory. This data format is compatible with the display controller. This representation is endiannism invariant: it is the same for little endian and big endian.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A								R								G								B							

The RGB output is enabled by setting the RZx_RGB_EN[0] RGB_EN bit to 1.

The RGB format is set by the RZx_RGB_TYP[0] TYP bit (0 for ARGB32 format and 1 for RGB5:6:5).

To handle the horizontal border conditions, the left-most Chroma sample or the right-most Chroma sample is duplicated on the left or the right.

Software must make it possible to remove 2 pixels on the left and/or right to take care of the issues that Chroma duplication introduces on the borders. The RZx_RGB_TYP[1] MSK0 and RZx_RGB_TYP[2] MSK1 bits control this feature.

Figure 8-186 shows the ISS ISP RSZ chroma position and upsampling.

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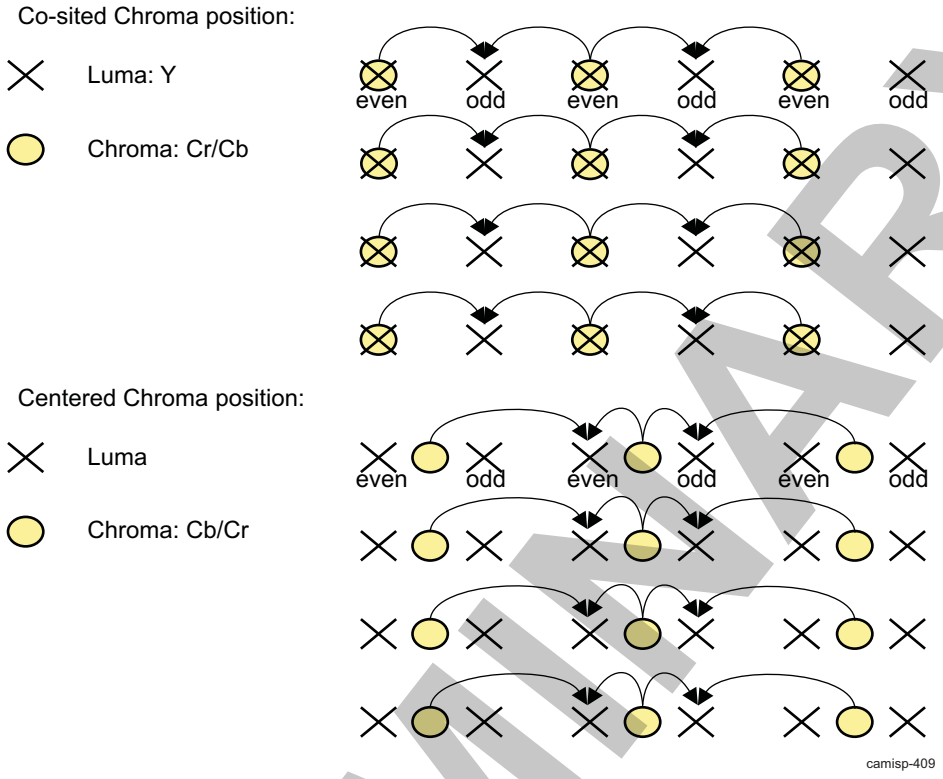
Figure 8-186. ISS ISP RSZ Chroma Position and Upsampling



NOTE: In case Cb/Cr in the input image is flipped, the RSZ_SRC_FMT1[3] CHR bit must be set to 1 to assure correct color conversion. This setting restores the right order in YUV to RGB conversion, and generates correct RGB colors.

8.3.3.4.5.7 ISS ISP RSZ Output Interface

The output interface receives the data generated by the two resizer engines and generates the addresses and the port requests to the BL module.

- The port 1 interface is dedicated to the RSZ-A module. If the RSZ module is set up in pass-through mode, then the data is output on the port 1 interface. This interface can transfer RAW, YUV4:2:2, YUV4:2:0, and RGB data
- The port 2 interface is dedicated to the RSZ-B module. This interface can transfer RAW, YUV4:2:2, YUV4:2:0, and RGB data.

The YUV4:2:0 data format is handled differently from the other formats because the output data are written at two different memory locations: Luma in one buffer and Chroma in a second buffer. For all other formats the data are written in the same buffer.

Each data format must be stored in memory in a dedicated manner, which is summarized in Table 8-435.

Table 8-435. ISS ISP RSZ Output Interface: Data Formats

Output Format	Bytes per Pixel	Output Buffers per Image	Interface Supporting the Data Format
RAW	2	1	MTC port 1
YUV4:2:2	2 average	1	MTC port 1 port 2
YUV4:2:0	1.5 average	2	MTC port 1 port 2
RGB16	2	1	MTC port 1 port 2
ARGB32	4	1	MTC port 1 port 2

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8.3.3.4.5.7.1 ISS ISP RSZ Circular Buffer

Figure 8-187 shows the parameters that are required to set up the circular buffers. As mentioned previously, there can be up to four circular buffers in case the two resizer engines are outputting YUV4:2:0 data.

The circular buffer management requires the following parameters (RSZ-A or RSZ-B A or B,Chroma or Luma Y or C, low or high part of the address, L or H. Sets the base address of the circular buffer):

- Baseline address (BAD, in registers, where x is the resizer A or B, and i is Y or C)
- Start address (SAD, in RZx_SDR_i_SAD_j registers)
- Start pointer (PTR_S, in RZx_SDR_i_PTR_S registers)
- End pointer (PTR_E, in RZx_SDR_i_PTR_E registers)
- Line offset (OFT, in RZx_SDR_i_OFT registers)

Table 8-436. ISS ISP RSZ Circular Buffer

Circular Buffer Parameter	Register (for RSZ-A and RSZ-B)	Description
Baseline address	RZA_SDR_Y_BAD_H RZA_SDR_Y_BAD_L RZA_SDR_C_BAD_H RZA_SDR_C_BAD_L RZB_SDR_Y_BAD_H RZB_SDR_Y_BAD_L RZB_SDR_C_BAD_H RZB_SDR_C_BAD_L	Sets the base address of the circular buffer
Start address	RZA_SDR_Y_SAD_H RZA_SDR_Y_SAD_L RZA_SDR_C_SAD_H RZA_SDR_C_SAD_L RZB_SDR_Y_SAD_H RZB_SDR_Y_SAD_L RZB_SDR_C_SAD_H RZB_SDR_C_SAD_L	Sets the start address of the circular buffer. The first data output is written to this address. If the first line of a frame must be written at the beginning of the circular buffer memory, then SAD = BAD and PTR_S = 0.
Start pointer	RZA_SDR_Y_PTR_S RZA_SDR_C_PTR_S RZB_SDR_Y_PTR_S RZB_SDR_C_PTR_S	Sets the initial value of the circular buffer internal counter. It must be set up as PTR_S = (SAD – BAD)/OFT. PTR_S is expressed in the number of lines.
End pointer	RZA_SDR_Y_PTR_E RZA_SDR_C_PTR_E RZB_SDR_Y_PTR_E RZB_SDR_C_PTR_E	Sets the size of the circular buffer. PTR_E is expressed in the number of lines. The circular buffer can contain up to PTR_E lines.
Line offset	RZA_SDR_Y_OFT RZA_SDR_C_OFT RZB_SDR_Y_OFT RZB_SDR_C_OFT	This is the offset expressed in bytes between two lines in the circular buffer. Here: Line 0 = SAD, Line 1 = SAD + 1 × OFT, Line 2 = SAD + 2 × OFT, etc. OFT does not necessarily correspond to the size of a line in a frame; it can be bigger.

More generally, the following equations hold:

- SAD = BAD + (PTR_S × OFT) and PTR_S < PTR_E

Interrupts can be triggered every time a certain number of lines are written to the circular buffer. There are independent settings for each RSZ and for each possible output of each RSZ.

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Figure 8-187. ISS ISP RSZ and Circular Buffer Settings

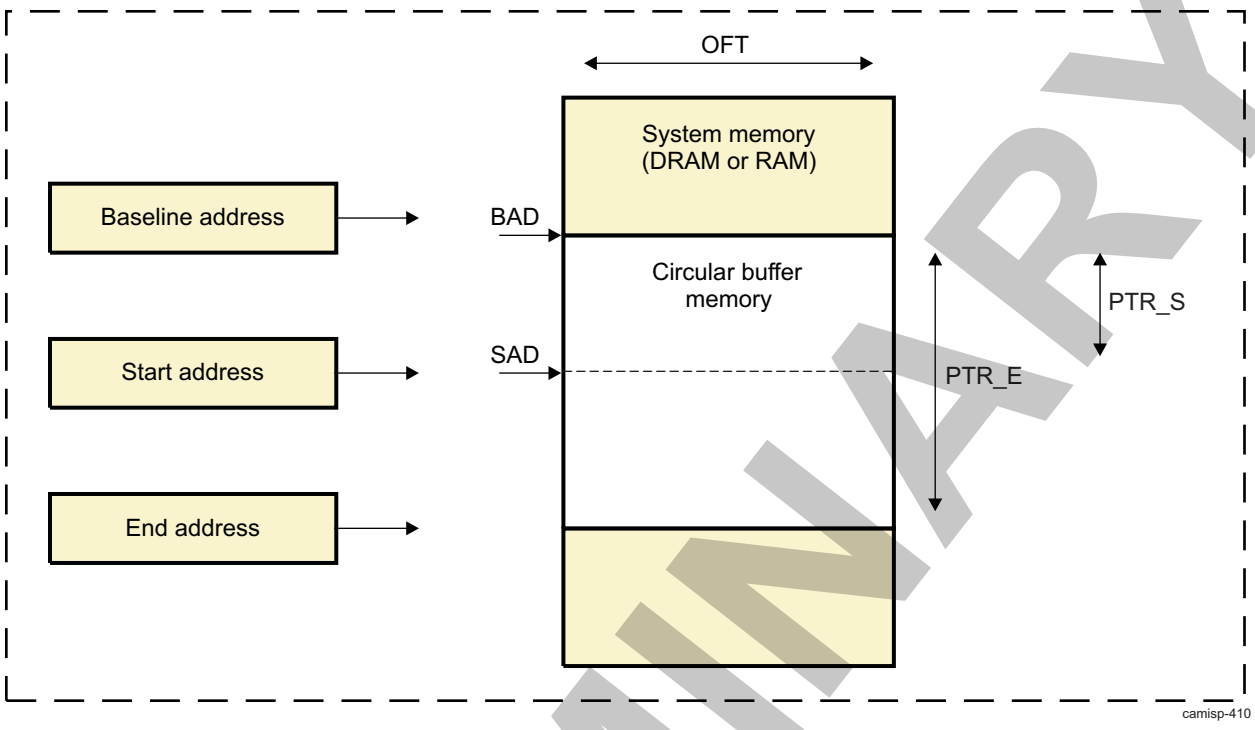
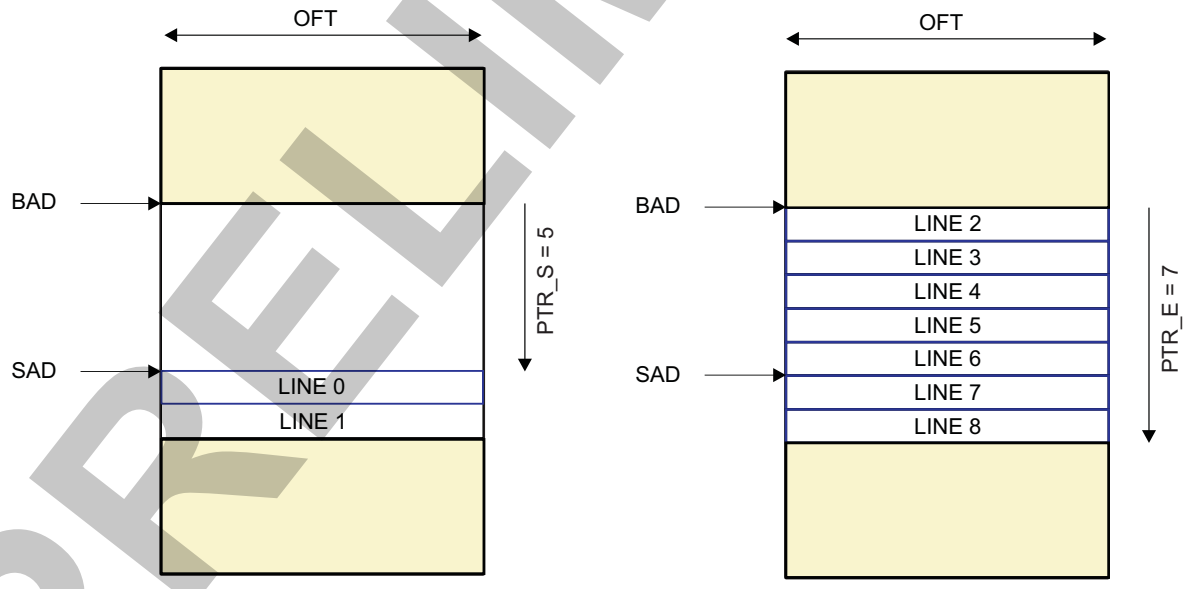


Figure 8-188 shows how the data are stored in the circular buffer over time when vertical flip is disabled. In this example, PTR_S = 5 and PTR_E = 7. There can be up to PTR_E = 7 lines in the circular buffer.

Figure 8-188. ISS ISP RSZ and Circular Buffer Settings – Example 1



Vertical flip enabled:

1. Start from SAD.
2. Output PTR_E – PTR_S lines.
3. Wrap to BAD.
4. Output PTR_E lines and continue wrapping to BAD.

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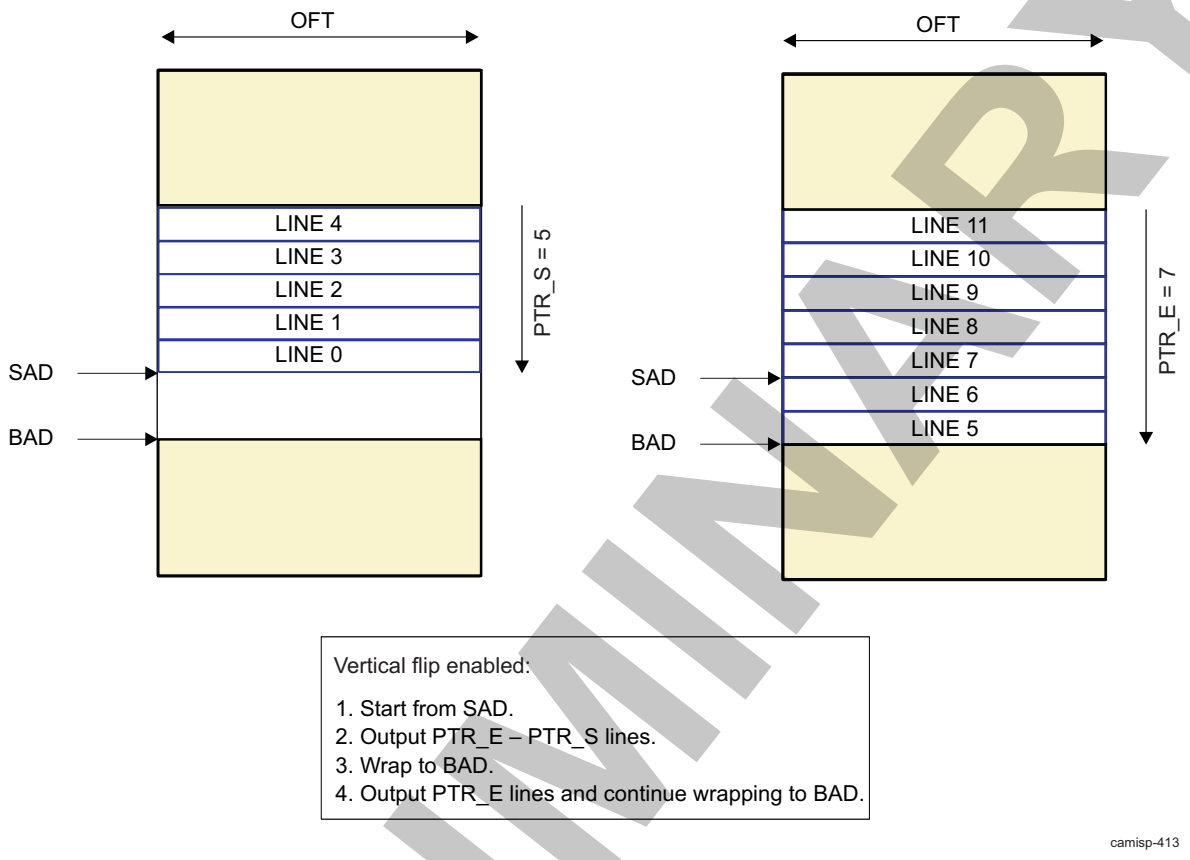
Figure 8-189 shows how the data are stored in the circular buffer over time when vertical flip is enabled. In this example, PTR_S = 5 and PTR_E = 7. There can be up to PTR_E = 7 lines in the circular buffer.

Figure 8-189. ISS ISP RSZ and Circular Buffer Settings – Example 2



8.3.3.5 ISS ISP H3A Functional Description

8.3.3.5.1 ISS ISP H3A Overview

The H3A module supports the control loops for autofocus, auto white balance, and auto exposure by collecting metrics about the imaging/video data. The metrics are used to adjust parameters for processing the imaging/video data. There are two main blocks in the H3A module:

- Autofocus (AF) engine:

  The AF submodule extracts and filters the red, green, and blue data from input image data and provides the accumulation or peaks of the data in a specified region. The specified region is a 2D block of data referred to as a paxel. The AF engine supports the following features:

  – Peak mode in a paxel: Accumulation of the maximum focus value (FV) of each line in a paxel
  – Accumulation mode in a paxel
  – Accumulation of horizontal and vertical focus value in a paxel
  – Up to 12 paxels in the horizontal direction and up to 12 paxels in the vertical direction with vertical focus
  – Up to 36 paxels in the horizontal direction and up to 128 paxels in the vertical direction with horizontal focus only
  – Programmable width and height for the paxel/window
  – Programmable red, green, and blue position within a 2 × 2 matrix
  – Separate horizontal start for paxel and filtering
  – Programmable vertical and horizontal line increments within a paxel

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  - Horizontal FV uses parallel infinite impulse response (IIR) filters configured in a dual-biquad configuration with individual coefficients (two filters with 11 coefficients each). The filters are intended to compute the sharpness/peaks in the frame on which to focus.
  - Vertical FV uses a 5-tap FIR filter with 8-bit coefficients. With horizontal steps each paxel has up to 32 columns to be maintained for vertical FV calculation.
- Auto exposure and auto white balance (AE/AWB) engine:

  The AE/AWB engine accumulates values and checks for saturated values in a subsampling of the video data. In the case of the AE/AWB, the 2D block of data is referred to as a window. Thus, other than having different names, paxels and windows are essentially the same. However, the numbers, dimensions, and starting positions of AF paxels and AE/AWB windows are programmable separately. AE/AWB supports the following features:
  - Accumulate clipped pixels along with all nonsaturated pixels in each window per color
  - Accumulate the sum of squared pixels in each window per color
  - Minimum and maximum pixel values in each window per color
  - Support for up to 36 horizontal windows with sum + { sum_sq or min+max} output
  - Support for up to 56 horizontal windows with sum output
  - Support for up to 128 vertical windows
  - Programmable width and height for the windows. All windows in the frame are the same size.
  - Separate vertical start coordinate and height for a black row of paxels that is different than the remaining color paxels
  - Programmable horizontal sampling points in a window
  - Programmable vertical sampling points in a window
- Maximum pixel throughput of 304 MPix/s
- Double-buffer for paxel/window accumulation
- H3A data path is 10 bits.
- Maximum input size is 3008 pixels.

Figure 8-190 shows the H3A module connections to other submodules of the ISP.

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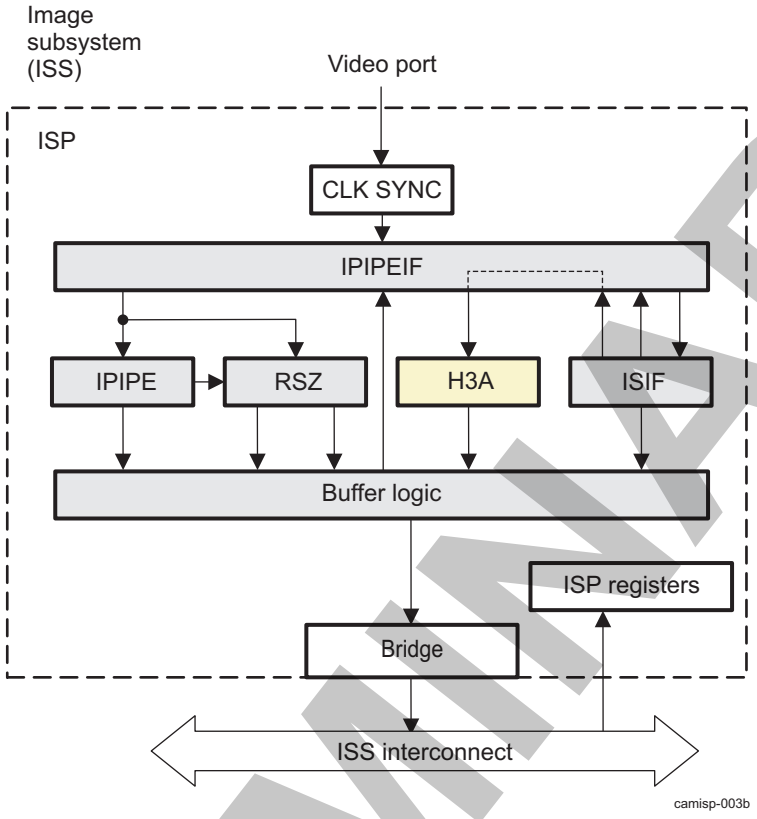
Figure 8-190. ISS ISP H3A High-Level Diagram



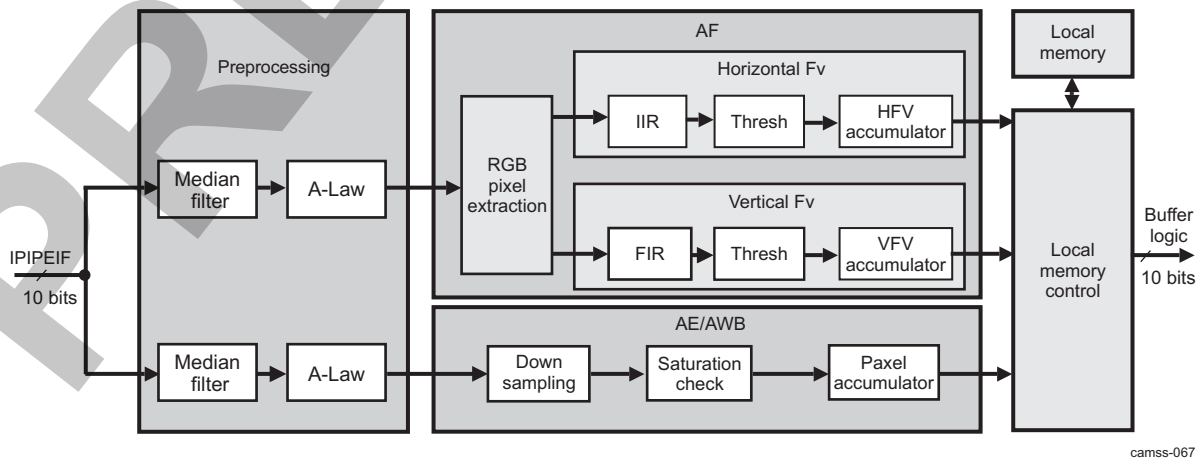
8.3.3.5.2 ISS ISP H3A Top-Level Block Diagram

The block diagram in Figure 8-191 shows the process of the AF and AE/AWB data paths through the H3A module.

The data flow before H3A is:

1. Data comes from the VP or BL.
2. The data is processed by the ISIF.
3. The data is processed by the IPIPEIF.
4. The data is 10 bits from the IPIPEIF at H3A input.

Figure 8-191. ISS ISP H3A Top-Level Block Diagram



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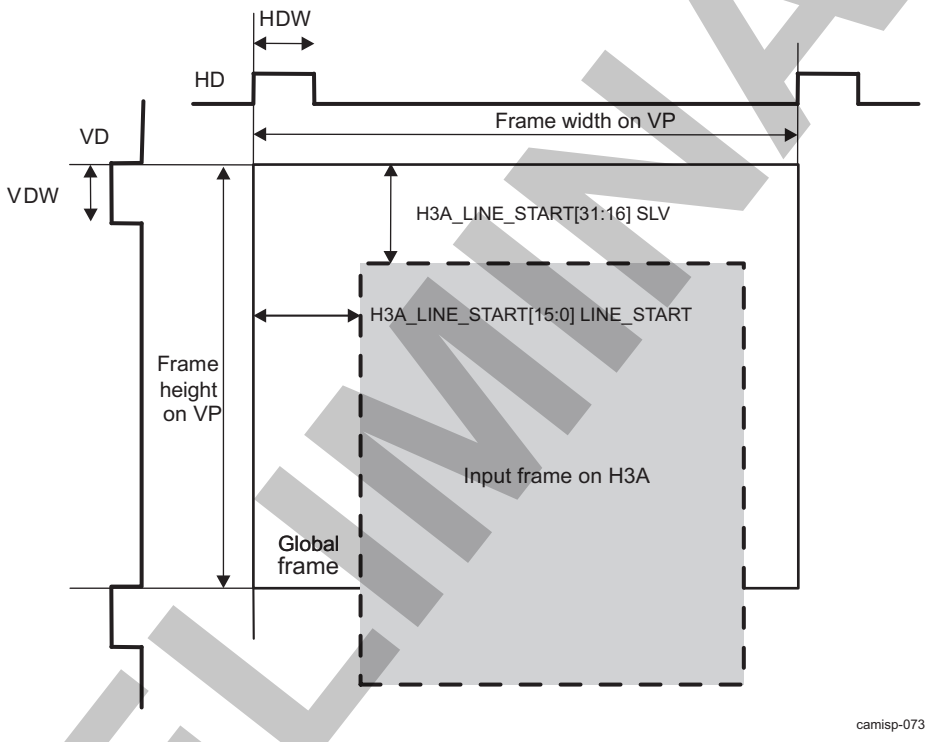
8.3.3.5.3 ISS ISP H3A Line Framing Logic

In certain cases the number of clock cycles between HD pulses is greater than the line buffer included in the H3A. To solve this problem a framing module was added before the line buffer. The framing module uses the H3A_LINE_START register to find the position of the first pixel to place into the line buffer. All other registers reference this point as the 0 pixel for their start positions. The line size is 3008 pixels. After 3008 clock cycles the framing logic disables the line buffer and waits until the next HD. If the next HD comes before 3008 clock cycles, then the active region ends immediately and the counter waits for the H3A_LINE_START register count to be reached again. For the vertical position the H3A_LINE_START[31:16] SLV bit field can be used to determine where the start point of the frame is relative to the rising edge of VD. This logic allows for an active frame to cross VD boundaries and remain in the same frame.

Figure 8-192 shows the ISS ISP H3A frame format settings.

Figure 8-192. ISS ISP H3A Frame Format Settings



NOTE: (Frame width on VP) - (H3A_LINE_START[15:0] LINE_START) must be less than or equal to 3008, because the H3A memory lines are limited to 3008 pixels.

8.3.3.5.4 ISS ISP H3A Optional Preprocessing

The input to the H3A module is 10-bit RAW data from the IPIPEIF. A 10-bit to 8-bit A-Law compression step can be enabled and disabled separately for the AF engine (the H3A_PCR[1] AF_ALAW_EN bit) and the AE/AWB engine (the H3A_PCR[17] AEW_ALAW_EN bit). A-Law compression offers added protection against overflowing the accumulators.

If the A-Law table is enabled, the output is 10 bits, with the upper two bits filled with 0.

For the AF process, a horizontal median filter can be enabled and disabled (the H3A_PCR[2] AF_MED_EN bit) before A-Law compression. This filter is useful for reducing temperature-induced noise. The horizontal median filter calculates the absolute difference between the current pixel (i) and pixel (i – 2), and between the current pixel (i) and pixel (i + 2). If the absolute difference exceeds a threshold, and the sign of the differences is the same, the average of pixel (i – 2) and pixel (i + 2) replaces pixel (i). The threshold of the horizontal median filter can be set in the H3A_PCR[10:3] MED_TH bit field.

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8.3.3.5.5 ISS ISP H3A Autofocus Engine

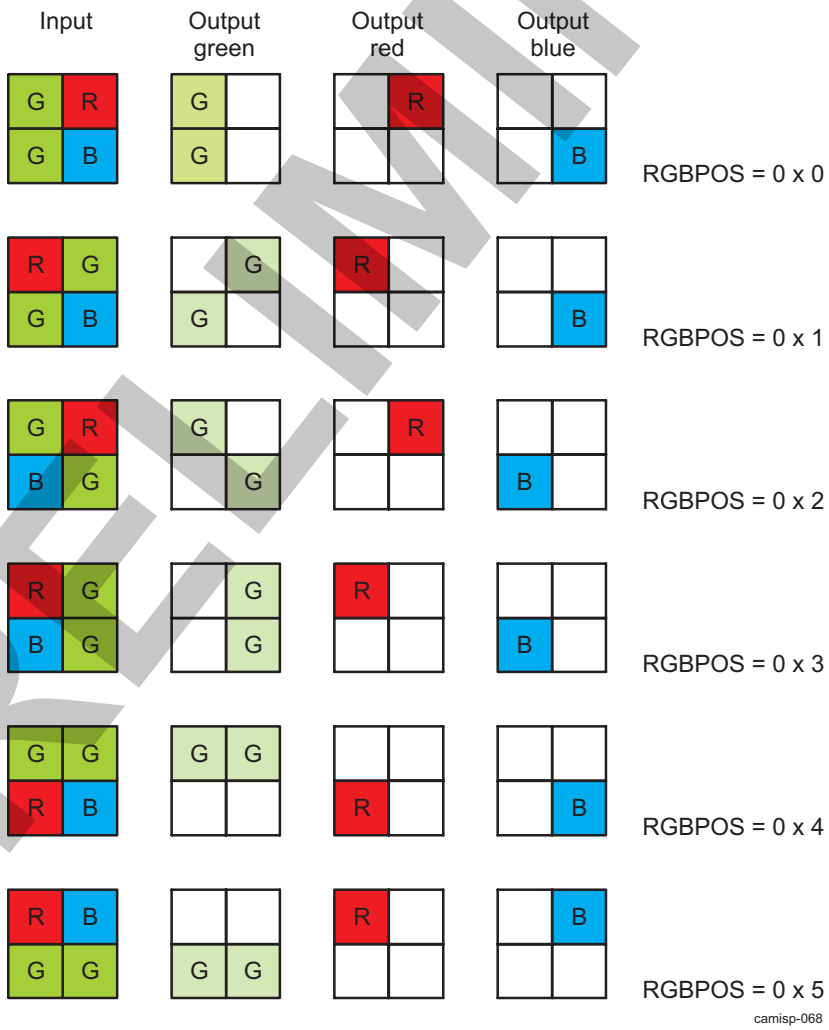
The AF engine works by extracting each green (Gr or Gb) pixel from the video stream and subtracts a fixed offset of 128 or 512 (depending of whether A-Law is enabled or disabled) from the pixel value. The offset value is then passed through an IIR filter and the absolute value of the filter output is the focus value (FV). Both FV and FV^2 are produced. The FV and FV^2 values can be accumulated or the maximum for each line/column can be accumulated. The following sections describe this process in more detail.

8.3.3.5.5.1 ISS ISP H3A Paxel Extraction

From the paxel starting coordinate (the H3A_AFPAXSTART[27:16] PAXSH and H3A_AFPAXSTART[11:0] PAXSV bit fields) specifies the starting point of the paxel grid, with respect to first pixel of the input image frame.

The paxel starting coordinate also indicates which color pixels are extracted if VF is enabled (that is, if H3A_PCR[20] AF_VF_EN = 1). Normally, either Gr or Gb is used for AF, but it is not important to the hardware whether it is red, green, or blue. If VF is not enabled, then the red, green, and blue pixel extraction is controlled by the H3A_PCR[13:11] RGBPOS bit field to extract the correct colors from the input stream. Figure 8-193 shows the available options for this bit field. The red and blue pixel positions are interchangeable. For each 2 × 2 grid, the green pixels are summed to create a single value. Because of this, the amplitude of the green output contains 2 pixels, while the red and blue outputs each contain 1 pixel.

Figure 8-193. ISS ISP H3A Red, Green, and Blue Pixel Extraction Examples



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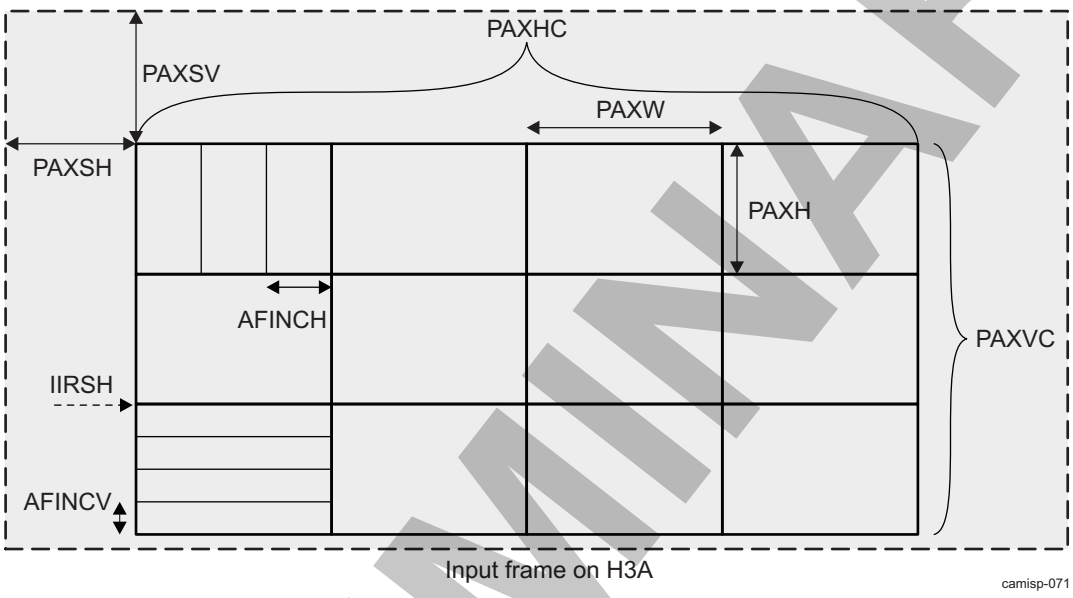
Each paxel is H3A_AFPAX1[23:16] PAXW × H3A_AFPAX1[7:0] PAXH (width × height) pixels. Inside each paxel, horizontal FV can skip lines, operating on one every H3A_AFPAX2[16:13] AFINCV lines. Vertical FV can skip columns, operating on one every H3A_AFPAX2[20:17] AFINCH columns. Up to 32 columns are supported for each paxel. If floor (PAXW/AFINCH) >= 32, only the first 32 designated columns are operated on. Because PAXW, PAXH, AFINCV, and AFINCH are all even numbers, AF always operates on the same green color, Gr or Gb. IIR filters for the horizontal FVs start operation at column H3A_AFIIRSH[11:0] IIRSH.

Figure 8-194 shows the ISS ISP H3A horizontal/vertical fv paxel configuration.

Figure 8-194. ISS ISP H3A Horizontal/Vertical FV Paxel Configuration



NOTE: (H3A_AFPAXSTART[27:16] PAXSH) + (H3A_AFPAX2[5:0] PAXHC) × (H3A_AFPAX1[23:16] PAXW) <= [(Frame width on VP) – (H3A_LINE_START[15:0] LINE_START)] <= 3008

Table 8-437 lists the bit fields that configure the size and number of paxels.

Table 8-437. ISS ISP H3A Paxel Register Field Descriptions

Bit Field	Bit Width	Description
H3A_AFPAX1[23:16] PAXW	8	Paxel width (in pixels)
H3A_AFPAX1[7:0] PAXH	8	Paxel height (in lines)
H3A_AFPAX2[5:0] PAXHC	6	Paxel count for horizontal direction
H3A_AFPAX2[12:6] PAXVC	7	Paxel count for vertical direction
H3A_AFPAX2[16:13] AFINCV	4	Line increments in a paxel
H3A_AFPAX2[20:17] AFINCH	4	Column increments in a paxel
H3A_AFPAXSTART[27:16] PAXSH	12	Paxel start position H
H3A_AFPAXSTART[11:0] PAXSV	12	Paxel start position V
H3A_AFIIRSH[11:0] IIRSH	12	IIR filter start position

The H3A AF engine also has an option for an advanced or normal stats collection mode. When 0xCA00 is written to the H3A_ADVANCED[31:15] ID bit field, then H3A_ADVANCED[0] AF_MODE can be used to toggle between normal and advanced AF stats collection mode. When the advanced AF stats collection mode is enabled, the ZEROS section of the AF paxel packet is filled with the sum of the maximum FVs, regardless of the color, from HFV_1 and HFV_2.

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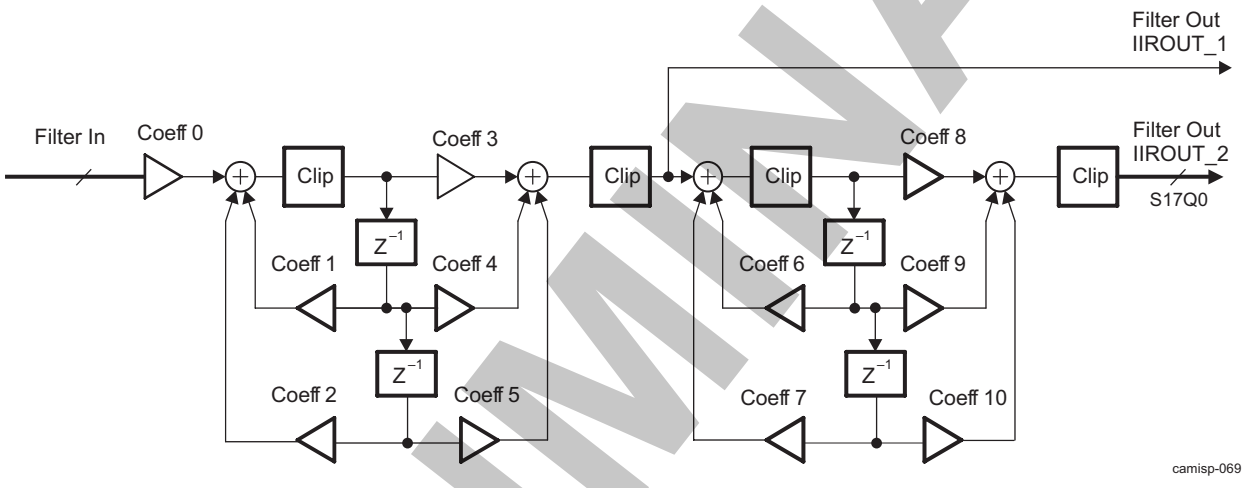
8.3.3.5.5.2 ISS ISP H3A Horizontal FV Calculator

The FV calculator takes the unsigned red/green/blue extracted data and subtracts 128 or 512 (depending on whether A-Law is enabled) to place the data in the range –128 to 127 or –512 to 511.

After removing the offset, the data is sent through two parallel IIR filters configured in a dual-biquad configuration. Each filter uses a unique set of 11 programmable coefficients. Each coefficient is 12-bits-wide with 6 bits of decimal, S12Q6 (H3A_AFCOEF010 to H3A_AFCOEF0010 for SET0, and H3A_AFCOEF110 to H3A_AFCOEF1010 for SET1). The filter-shift registers are cleared on each horizontal line at the position set by the register IIR horizontal start register (the H3A_AFIIRSH[11:0] IIRSH bit field). The absolute values of the output (16 bits wide with 4 bits of decimal, U16Q4) of both filters are then sent to the AF accumulator module. Signed clipping is performed during the FV calculation. If the input value is m bits (signed) and the required output value is n bits, clipping transforms the input to between -2^1 and 2^1. Values lower than -2^1 are set to -2^1, and values higher than 2^1 are set to 2^1.

Figure 8-195 shows the IIR filter model.

Figure 8-195. ISS ISP H3A IIR Filter Model



8.3.3.5.5.3 ISS ISP H3A HFV Accumulator

The horizontal focus value (HFV) accumulator takes the output of the horizontal IIR filter and accumulates values for each paxel. The size and number of paxels is configurable by registers.

Table 8-437 lists the register fields that configure the size and number of paxels:

- In peak mode (H3A_PCR[14] FVMODE = 0x1), the maximum value is accumulated.
- In sum mode (H3A_PCR[14] FVMODE = 0x0), all HFV_n are accumulated in a paxel.

The following equations detail the calculation for:

- Sum of pixel values used in HFV: The pixel values that are used for filtering and accumulation of HFV are also accumulated in this sum of pixel values.
- HFV_n (HFV_n_peak for peak mode or HFV_n_sum for sum mode)
- HFV_count_n
- HFV_sq_n (HFV_sq_n_peak for peak mode or HFV_sq_n_sum for sum mode)

n = 1 or 2 for IIR1 and IIR2, respectively.

For each paxel, these six values are available for each R, G, and B component.

```
for (k=0; k<PAXH) // Loop on paxel rows
{
 rowpeak_n = 0;

 for (l=0; l<PAXW; l++) // Loop on values within a row
 {
 aIIRout_n = ABS(IIRout_n);
```

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```
if (aIIRout_n >= threshold_n)
{
hfval = aIIRout_n - threshold_n;
HFV_count_n++;
}
else hfval = 0;
if (hfval > rowpeak_n)
{
rowpeak_n = HFV_n;
}
HFV_n_sum += hfval;
HFV_sq_n_sum += (hfval* hfval + RNDADD) >> RNDSHIFT;
} // Finished looping on values in a row
HFV_n_peak += rowpeak_n;
HFV_sq_n_peak += (rowpeak_n * rowpeak_n + RNDADD) >> RNDSHIFT;

}
```

- threshold_n is H3A_HVF_THR[15:0] HTHR1 and H3A_HVF_THR[31:16] HTHR2, respectively.
- IIRout_n is the IIRout_1 and IIRout_2 outputs, respectively.
- HFV_count_n and HFV_sq_n are not sent to the DMA interface if VF is disabled.
- RNDADD and RNDSHIFT depend on whether input pixels are 8-bit or 10-bit, and achieves rounding. This is automatically performed by the module.
- If VF is enabled, only the green color channel values are output to the DMA interface.
- In sum mode:
  - HFV_n = HFV_n_sum
  - HFV_sq_n = HFV_sq_n_sum
- In peak mode:
  - HFV_n = HFV_n_peak
  - HFV_sq_n = HFV_sq_n_peak

8.3.3.5.5.4 ISS ISP H3A VFV Calculator

The VFV calculator takes the unsigned extracted data through two FIR filters, each with a set of five coefficients (VCOEF1_x, where x = 0 to 4, in the H3A_VFV_CFG1 and H3A_VFV_CFG2 registers for FIR 1, and VCOEF2_x, where x = 0 to 4, in the H3A_VFV_CFG3 and H3A_VFV_CFG4 registers). Each coefficient is 8 bits wide with 4 bits of decimal (S8Q4). The filter outcome is downshifted by 4 bits and takes an absolute value to produce a 16-bit unsigned value. This is then sent to threshold H3A_VFV_CFG2[31:16] VTHR1 for FIR 1, and H3A_VFV_CFG4[31:16] VTHR2 for FIR 2, and square logic to produce VFV_n and VFV_sq_n.

8.3.3.5.5.5 ISS ISP H3A VFV Accumulator

The VFV accumulator takes the output of the vertical FIR filters and accumulates values for each paxel. The size and number of paxels is configurable by registers.

Table 8-437 lists the bitfields that configure the size and number of paxels.

The following equations detail the calculation for:

- VFV_n
- VFV_count_n
- VFV_sq_n

n = 1 or 2 for FIR1 and FIR2, respectively.

For each paxel, these six values are available for each R, G, and B component.

```
FIR_coef_n = [VCOEFn_0, VCOEFn_1, VCOEFn_2, VCOEFn_3, VCOEFn_4]; /* coefficient values in S8.4
format */
aFIRout_n = (ABS(inner_product(extracted_G, FIR_coef_n)) + 8) >> 4;
```

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```
if (aFIRout_n >= threshold_n)
{
 VFV_n = aFIRout_n - threshold_n
 VFV_count_n++;
}
else VFV_n = 0;

VFV_sq_n = (VFV_n * VFV_n + RNDADD) >> RNDSHIFT;
```

- threshold_n is H3A_VFV_CFG2[31:16] VTHR1 and H3A_VFV_CFG4[31:16] VTHR2, respectively.
- FIRout_n is the FIRout_1 and FIRout_2 outputs, respectively.
- RNDADD and RNDSHIFT depend on whether the input pixels are 8-bit or 10-bit, and achieves rounding. This is automatically performed by the module.

8.3.3.5.6 ISS ISP H3A AE/AWB Engine

The AE/AWB engine starts by dividing the frames into windows, and then subsamples each window into 2 × 2 blocks. For each subsampled 2 × 2 block, each pixel is accumulated. Also, each pixel is compared to a limit set in a register. If any pixels in a 2 × 2 block are greater than or equal to the limit, the block is not counted in the unsaturated block counter. Pixels greater than the limit are replaced by the limit, and the value of the pixel is accumulated.

The AE/AWB module has three output format modes, which are set through the H3A_AEWCFG[9:8] AEFMT bit field:

- Sum of square mode: H3A_AEWCFG[9:8] AEFMT = 0x0
- Min/max mode: H3A_AEWCFG[9:8] AEFMT = 0x1
- Sum-only mode: H3A_AEWCFG[9:8] AEFMT = 0x2

8.3.3.5.6.1 ISS ISP H3A Subsampler

The subsampler partitions the frame into windows using the size, count, and starting location parameters shown on the left in Figure 8-196. Each window is further sampled down to a set of 2 × 2 blocks. The horizontal and vertical distances between the start of blocks within a window is programmable using the parameters shown on the right in Figure 8-196.

Figure 8-196. ISS ISP H3A AE/AWB Window Configurations

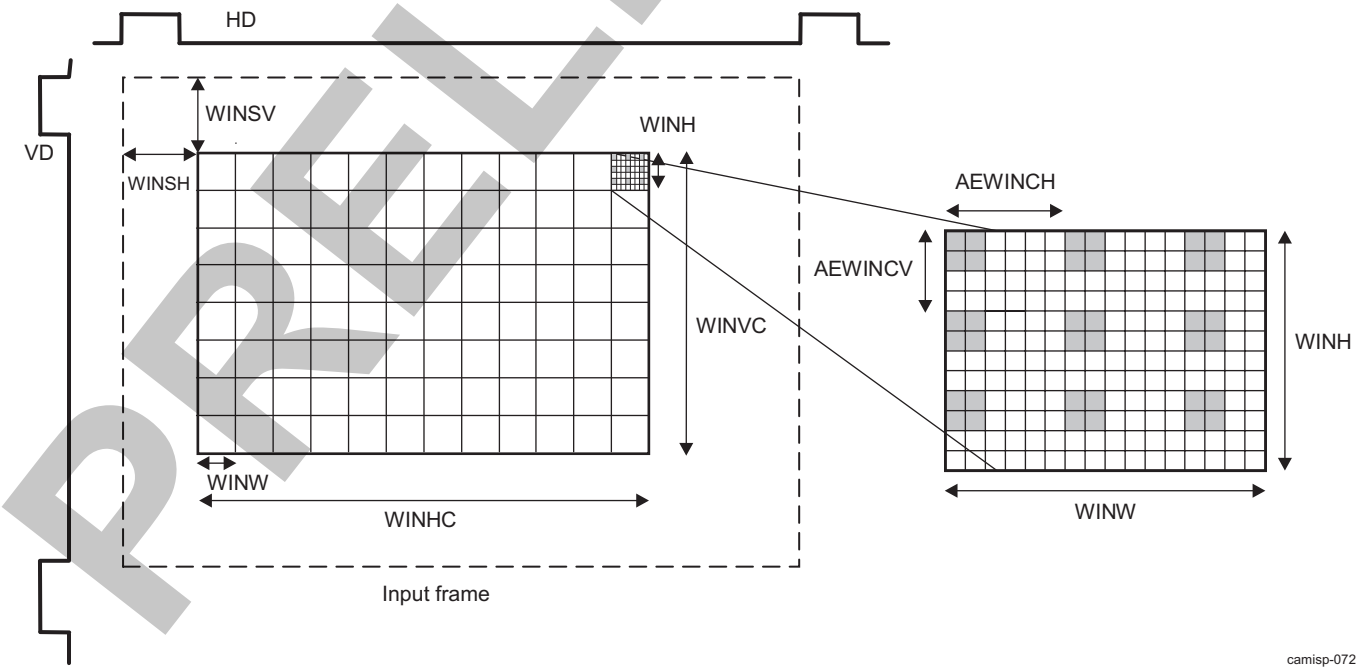

Table 8-438 lists the bit fields that configure the window and block sizes, counts, and starting positions.

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Table 8-438. ISS ISP H3A AE/AWB Window Register Field Descriptions

Bit Field	Bit Width	Description
H3A_AEWWIN1[20:13] WINW	7	Window width (in pixels)
H3A_AEWWIN1[31:24] WINH	7	Window height (in lines)
H3A_AEWWIN1[5:0] WINHC	6	Window count for horizontal direction
H3A_AEWWIN1[12:6] WINVC	7	Window count for vertical direction
H3A_AEWINSTART[11:0] WINSH	12	Window start position H
H3A_AEWINSTART[27:16] WINSV	12	Window start position V
H3A_AEWSUBWIN[3:0] AEWINCH	4	Horizontal distance between subsamples
H3A_AEWSUBWIN[11:8] AEWINCV	4	Vertical distance between subsamples

8.3.3.5.6.2 ISS ISP H3A Additional Black Row of AE/AWB Windows

In addition to the 128 rows of windows, the AE/AWB module provides support for an additional row of windows for black data. This data may be useful in determining the DC offset noise of the rest of the data. The black row of windows can be before or after the regular rows of windows. The vertical start line for the black row of windows is specified in the H3A_AEWINBLK[27:16] WINSV bit field, and the height is specified in the H3A_AEWINBLK[6:0] WINH bit field. The horizontal starting pixel and horizontal width of the black row of windows are the same as for the regular rows of windows.

Figure 8-197 shows a black row of windows before rows of windows.

Figure 8-197. ISS ISP H3A Black Row of Windows Before Regular Rows of Windows

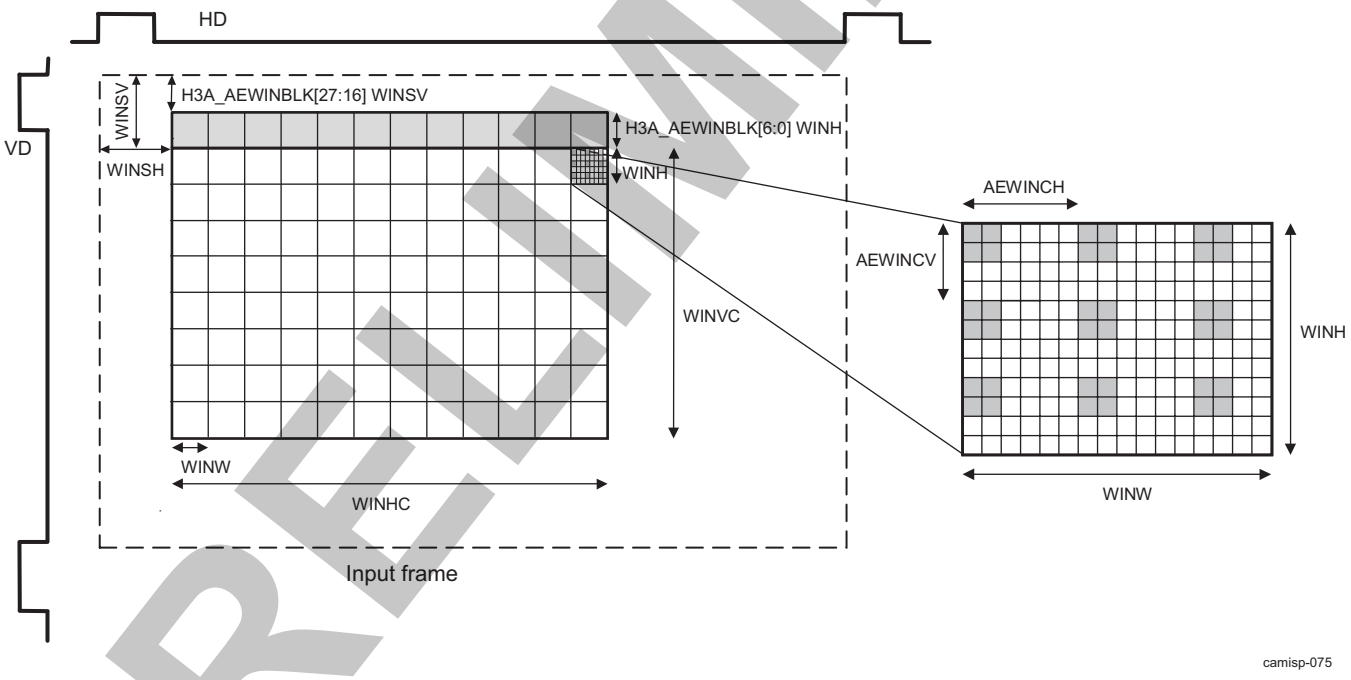

Table 8-439 lists the bit fields that configure the window and block sizes, counts, and starting positions.

Table 8-439. ISS ISP H3A AE/AWB Window With Additional Black Row Register Field Descriptions

Bit Field	Bit Width	Description
H3A_AEWWIN1[20:13] WINW	7	Window width (in pixels)
H3A_AEWWIN1[31:24] WINH	7	Window height (in lines)
H3A_AEWWIN1[5:0] WINHC	6	Window count for horizontal direction
H3A_AEWWIN1[12:6] WINVC	7	Window count for vertical direction
H3A_AEWINSTART[11:0] WINSH	12	Window start position H

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Table 8-439. ISS ISP H3A AE/AWB Window With Additional Black Row Register Field Descriptions (continued)

Bit Field	Bit Width	Description
H3A_AEWINSTART[27:16] WINSV	12	Window start position V
H3A_AEWSUBWIN[3:0] AEWINCH	4	Horizontal distance between subsamples
H3A_AEWSUBWIN[11:8] AEWINCV	4	Vertical distance between subsamples
H3A_AEWINBLK[27:16] WINSV	12	Window start position H for single black line
H3A_AEWINBLK[6:0] WINH	7	Window height (in lines) for single black line

8.3.3.5.6.3 ISS ISP H3A Saturation Check

The saturation check module compares the data from the subsampler to the value programmed in the H3A_PCR[31:22] AVE2LMT bit field. This value is the maximum clipping value. If all 4 pixels in the 2 × 2 block are less than the AVE2LMT value, the value of the unsaturated block counter is incremented. There is one unsaturated block counter per window. The unsaturated block counters are later written to memory.

8.3.3.5.6.4 ISS ISP H3A AE/AWB Accumulators

The output from the saturation check module and the subsampler module are separately accumulated for each pixel in every 2 × 2 pixel block for each window. Therefore, there are eight accumulators per window (one accumulator for each pixel in a 2 × 2 pixel block, times two sets of accumulators: clipped/saturated data and presaturated data). Each of the 4 pixels in the 2 × 2 pixel grid is associated with a color (R, Gr, B, Gb); however, the output of these accumulators is referenced by position in the grid, not color.

The accumulators are 16 bits wide, and the accumulated data is 10 bits wide. Therefore, when a window contains more than 64 pixels of the same color, an overflow risk exists. This risk can be reduced by enabling the A-Law conversion in the preprocessing stage. See Section 8.3.3.5.4 for details.

The AE/AWB module has a shift value for the accumulation of pixel values that is set in the H3A_AEWCFG[3:0] SUMSHFT bit field.

8.3.3.5.7 ISS ISP H3A DMA Interface

The DMA interface module takes the data from the AF engine and AE/AWB engine and builds packets to be sent to the memory through the BL module.

The data interface has separate start pointers for the AF and AE/AWB engines.

- The starting address for the AF engine is the H3A_AFBUFST[31:5] AFBUFST bit field.
- The starting address for the AE/AWB engine is the H3A_AEWBUFST[31:5] AEWBUFST bit field.

The DMA interface module continuously loops through this data as it builds the packets. To optimize the transfer sizes, the DMA interface sends out an AF or AE transfer for each row of paxels or windows. This requires that each horizontal row of paxels or windows starts and ends on a 32-byte boundary. If a horizontal row of paxels or windows ends on a non-32 byte boundary, the hardware packs zeroes. The counts for the AEW that occur every eight windows is sent in the row with the eighth consecutive window.

Table 8-440 lists the packet formats for AF with vertical AF disabled.

Table 8-440. ISS ISP H3A AF Packet Format With Vertical AF Disabled

Buffer Start Address (Byte Address) H3A_AFBUFST	31 16	15 0
	Sum of pixel values used in HFV	(Paxel 0)
	HFV_1 (peak or sum)	(Paxel 0)
	HFV_2 (peak or sum)	(Paxel 0)
	Zeroes	(Paxel 0)
	Sum of pixel values used in HFV	(Paxel 0)

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Table 8-440. ISS ISP H3A AF Packet Format With Vertical AF Disabled (continued)

Buffer Start Address (Byte Address) H3A_AFBUFST	31 16	15 0
	HFV_1 (peak or sum)	(Paxel 0)
	HFV_2 (peak or sum)	(Paxel 0)
	Zeroes	(Paxel 0)
	Sum of pixel values used in HFV	(Paxel 0)
	HFV_1 (peak or sum)	(Paxel 0)
	HFV_2 (peak or sum)	(Paxel 0)
	Zeroes	(Paxel 0)
	Sum of pixel values used in HFV	(Paxel 1)
	HFV_1 (peak or sum)	(Paxel 1)
	HFV_2 (peak or sum)	(Paxel 1)
	Zeroes	(Paxel 1)
	...	

Table 8-441 shows the packet formats for AF with vertical AF enabled.

Table 8-441. ISS ISP H3A AF Packet Format With Vertical AF Enabled

Buffer Start Address (Byte Address) H3A_AFBUFST	31 16	15 0
	Sum of pixel values used in HFV	(Paxel 0)
	HFV_1 (peak or sum)	(Paxel 0)
	HFV_sq_1 (peak or sum)	(Paxel 0)
	HFV_count_1	(Paxel 0)
	HFV_2 (peak or sum)	(Paxel 0)
	HFV_sq_2 (peak or sum)	(Paxel 0)
	HFV_count_2	(Paxel 0)
	Zeroes	(Paxel 0)
	VFV_1	(Paxel 0)
	VFV_sq_1	(Paxel 0)
	VFV_count_1	(Paxel 0)
	Zeroes	(Paxel 0)
	VFV_2	(Paxel 0)
	VFV_sq_2	(Paxel 0)
	VFV_count_2	(Paxel 0)
	Zeroes	(Paxel 0)
	Sum of pixel values used in HFV	(Paxel 1)
	HFV_1 (peak or sum)	(Paxel 1)
	HFV_sq_1 (peak or sum)	(Paxel 1)
	HFV_count_1	(Paxel 1)
	...	

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Figure 8-198 shows the windows and subsample definition used in tables.

Figure 8-198. ISS ISP H3A AE/AWB Window and Subsample Definition

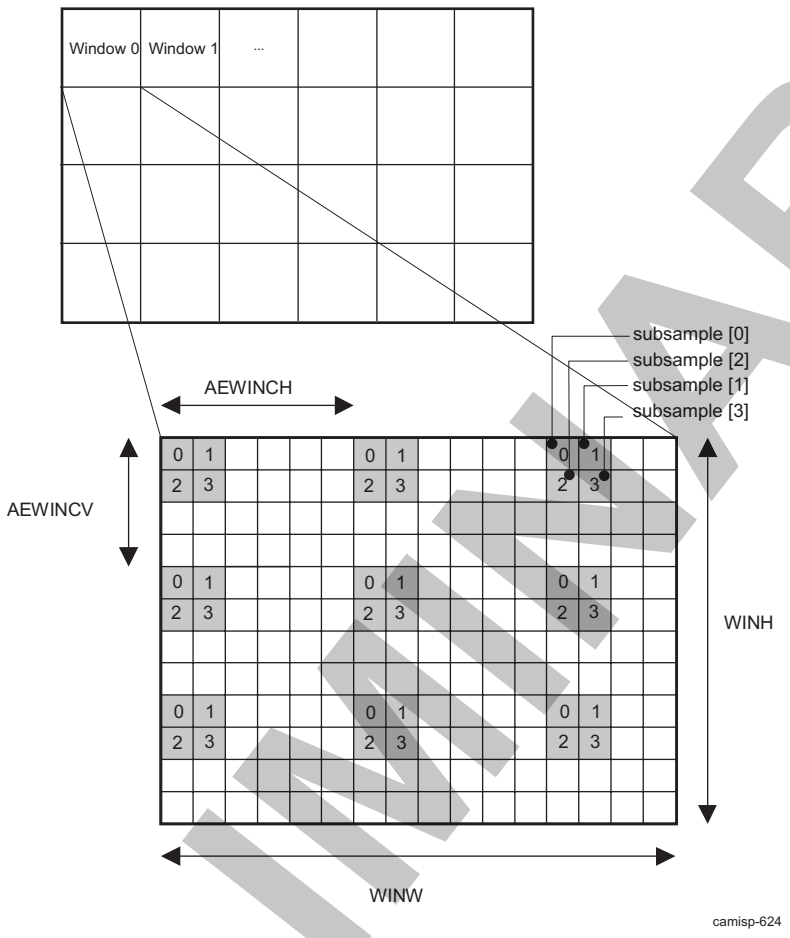

Table 8-442 lists the packet formats for AE/AWB for sum of square mode (H3A_AEWCFG[9:8] AEFMT = 0x0) .

Table 8-442. ISS ISP H3A AE/AWB Packet Format for Sum of Square Mode

	31 16	15 0	
Buffer address (byte address) H3A_AEWBUFST	Subsample Accum[1]	Subsample Accum[0]	Window 0 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 32 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 1 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Sum of squares[0]		

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Table 8-442. ISS ISP H3A AE/AWB Packet Format for Sum of Square Mode (continued)

	31 16	15 0	
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 64 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 2 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 96 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 3 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 128 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 4 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 160 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 5 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 192 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 6 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		

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Table 8-442. ISS ISP H3A AE/AWB Packet Format for Sum of Square Mode (continued)

	31 16	15 0	
H3A_AEWBUFST + 224 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 7 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
H3A_AEWBUFST + 256 bytes	Unsaturated count, win 1	Unsaturated count, win 0	Unsaturated block count for the above 8 windows
	Unsaturated count, win 3	Unsaturated count, win 2	
	Unsaturated count, win 5	Unsaturated count, win 4	
	Unsaturated count, win 7	Unsaturated count, win 6	
	Data for next eight windows, and so on. If the total number of windows is not a multiple of 8, the unsaturated counters are written immediately following the last window data. For example, if the total number of windows (including the black row) is 43, the first 40 windows are written out as per the 272-byte boundary above. Then the remaining three windows are written at +0, +32, and +64 bytes. The counts are written out at +96 instead of +256-byte boundary.		

Table 8-443 lists the packet formats for AE/AWB in minimum-maximum mode (H3A_AEWCFG[9:8] AEFMT = 0x1).

Table 8-443. ISS ISP H3A AE/AWB Packet Format for Minimum-Maximum Mode

	31 16	15 0	
Buffer address (byte address) H3A_AEWBUFST	Subsample Accum[1]	Subsample Accum[0]	Window 0 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 32 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 1 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 64 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 2 data

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Table 8-443. ISS ISP H3A AE/AWB Packet Format for Minimum-Maximum Mode (continued)

	31 16	15 0	
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 96 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 3 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 128 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 4 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 160 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 5 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 192 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 6 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 224 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 7 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	

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Table 8-443. ISS ISP H3A AE/AWB Packet Format for Minimum-Maximum Mode (continued)

	31 16	15 0	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
H3A_AEWBUFST + 256 bytes	Unsaturated count, win 1	Unsaturated count, win 0	Unsaturated block count for the above 8 windows
	Unsaturated count, win 3	Unsaturated count, win 2	
	Unsaturated count, win 5	Unsaturated count, win 4	
	Unsaturated count, win 7	Unsaturated count, win 6	
	Data for next eight windows, and so on. If the total number of windows is not a multiple of 8, the unsaturated counters are written immediately following the last window data. For example, if the total number of windows (including the black row) is 43, the first 40 windows are written out as per the 272-byte boundary above. Then the remaining three windows are written at +0, +32, and +64 bytes. The counts are written out at +96 instead of +256-byte boundary.		

Table 8-444 lists the packet formats for AE/AWB in sum-only mode (H3A_AEWCFG[9:8] AEFMT = 0x2).

Table 8-444. ISS ISP H3A AE/AWB Packet Format for Sum-Only Mode

	31 16	15 0	
Buffer address (byte address) H3A_AEWBUFST	Subsample Accum[1]	Subsample Accum[0]	Window 0 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
H3A_AEWBUFST + 32 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 1 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
H3A_AEWBUFST + 64 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 2 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
H3A_AEWBUFST + 96 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 3 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
H3A_AEWBUFST + 128 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 4 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	

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Table 8-444. ISS ISP H3A AE/AWB Packet Format for Sum-Only Mode (continued)

	31 16	15 0	
H3A_AEWBUFST + 160 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 5 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
H3A_AEWBUFST + 192 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 6 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
H3A_AEWBUFST + 224 bytes	Subsample Accum[1]	Subsample Accum[0]	Window 7 data
	Subsample Accum[3]	Subsample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum[3]	Saturator Accum[2]	
H3A_AEWBUFST + 256 bytes	Unsaturated count, win 1	Unsaturated count, win 0	Unsaturated block count for the above 8 windows
	Unsaturated count, win 3	Unsaturated count, win 2	
	Unsaturated count, win 5	Unsaturated count, win 4	
	Unsaturated count, win 7	Unsaturated count, win 6	
	Data for next eight windows, and so on. If the total number of windows is not a multiple of 8, the unsaturated counters are written immediately following the last window data. For example, if the total number of windows (including black row) is 43, the first 40 windows are written out as per the 272-byte boundary above. Then the remaining three windows are written at +0, +32, and +64 bytes. The counts are written out at +96 instead of +256-byte boundary.		

8.3.3.5.8 ISS ISP H3A Events and Status Checking

The AF and AEW engines generate an interrupt event at the end of processing each frame. However, these two interrupts are internally tied together so that only one H3A interrupt signal is generated. If the AF engine and AEW engine do not process the same frame concurrently, this should not be an issue. However, if they do run concurrently, one of two outcomes may occur:

- The H3A interrupt may seem to trigger only once for each frame. This can happen when the processing for the AF and AEW engines finishes at or near the same time. The interrupt service routine (ISR) does not have enough time to clear the interrupt flag for the first interrupt before the second interrupt occurs.
- The H3A interrupt may trigger twice for each frame. This can happen when the AF engine or the AEW engine finishes processing the frame much earlier than the other engine. In this case, the ISR does have enough time to clear the interrupt flag for the first interrupt by the time the second interrupt occurs.

The outcome depends on the difference in location of the last paxel/window in the frame (determines when processing is finished), the frequency of the relative clocks in the system, the occurrence and triggering of other interrupts in the system, and the latencies of the context switching and ISR execution.

The H3A_PCR[15] BUSYAF and/or H3A_PCR[18] BUSYAEAWB status bits are set when the start of frame occurs (if the H3A_PCR[0] AF_EN and/or H3A_PCR[16] AEW_EN bits are 1 at that time). They are automatically reset to 0 at the end of processing a frame. The H3A_PCR[15] BUSYAF and/or H3A_PCR[18] BUSYAEAWB status bits may be polled to determine the end of frame status.

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8.3.3.6 ISS ISP ISIF Functional Description

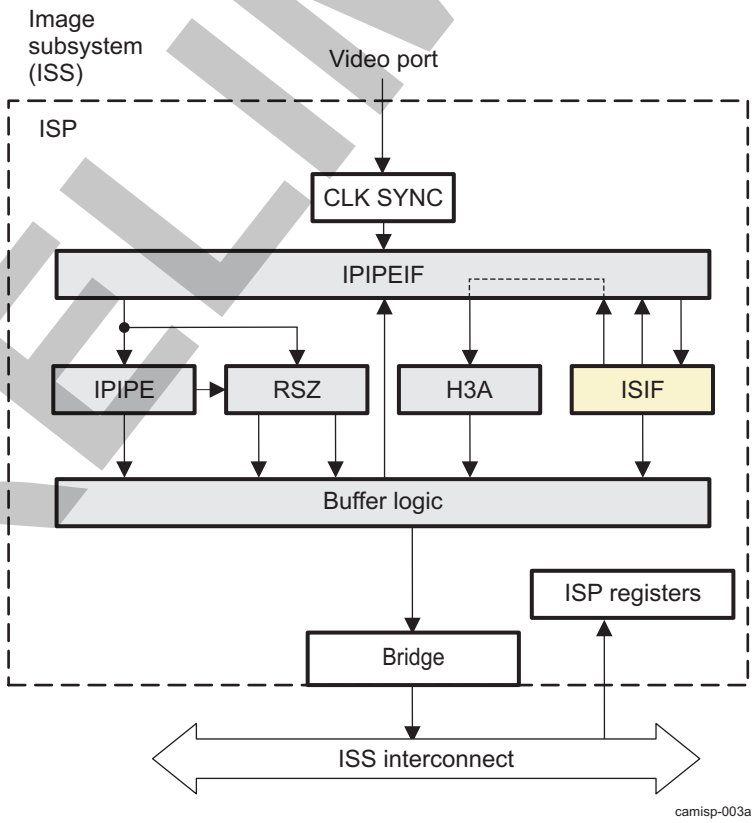
8.3.3.6.1 ISS ISP ISIF Overview

The ISIF module receives RAW or YUV4:2:2 data from the IPIPEIF module. The module outputs data back to the IPIPEIF module and can also output data to memory though the BL module. The ISIF module can process the incoming data and supports the following functions:

- Maximum supported image size is 32,768 × 32,768
- Supports up to 16-bit analog front end
- Sensor data linearization
- Supports Bayer and Foveon® input data format (RGB and CMYG color support)
- Supports VGA read out mode
- Supports various image data format
- Color space conversion
- Digital clamp with horizontal/vertical offset drift compensation
- Vertical line defect correction
- Programmable 2D-matrix LSC
- Gain and offset control
- Programmable horizontal/vertical culling pattern
- Maximum pixel rate clock of 304 MPix/s on the VP interface.
- 10-to-8-bit A-Law compression table inside
- 12-bit pack supported when written to memory

Figure 8-199 show the ISIF module connections to other submodules of the ISP.

Figure 8-199. ISS ISP ISIF High-Level Diagram



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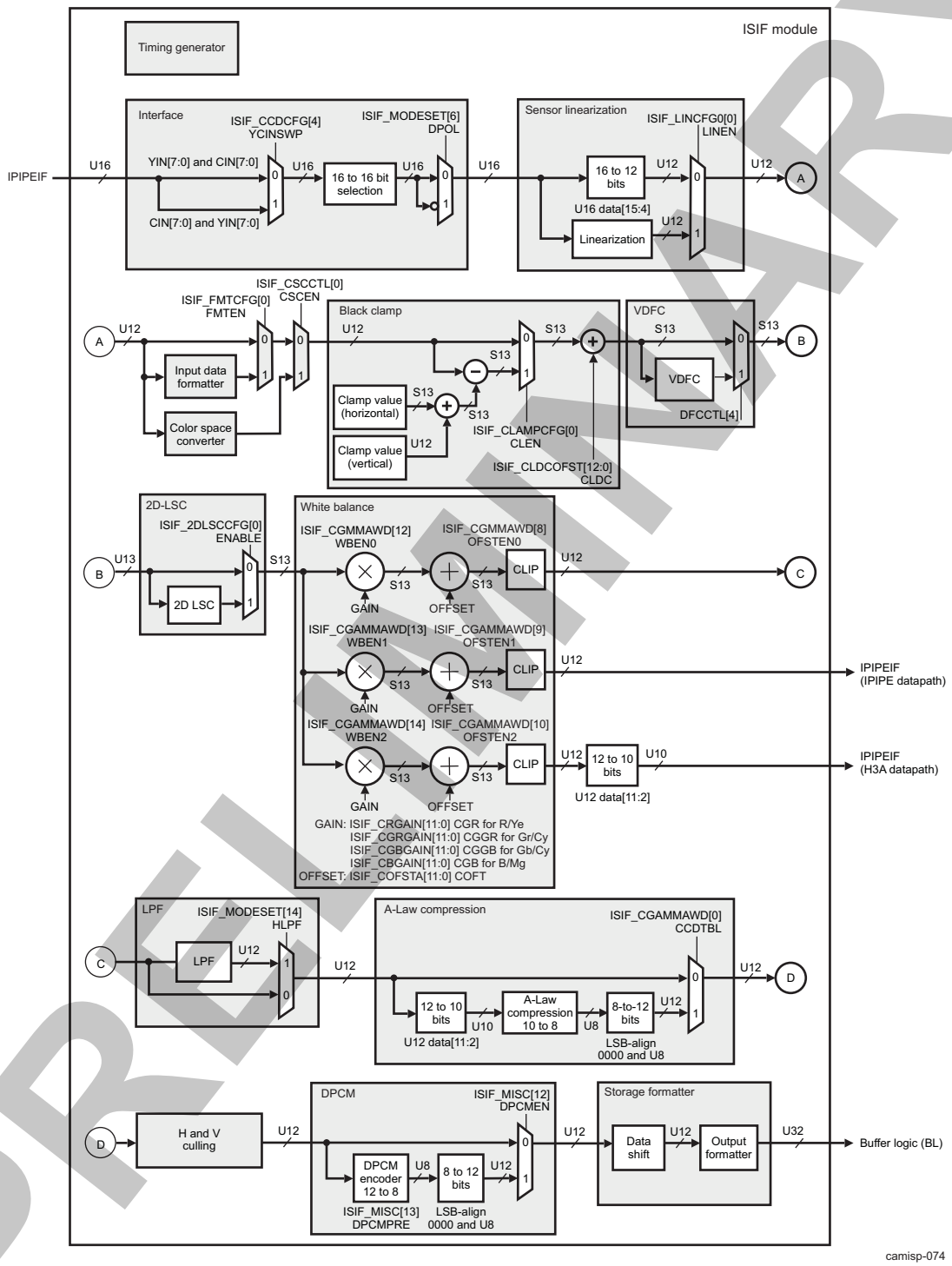
8.3.3.6.2 ISS ISP ISIF Top-Level Block Diagram

Figure 8-200 shows the different blocks of the ISIF module.

Figure 8-200. ISS ISP ISIF Top-Level Block Diagram



The following sections describe the blocks in the ISIF module.

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8.3.3.6.3 ISS ISP ISIF Input Interface

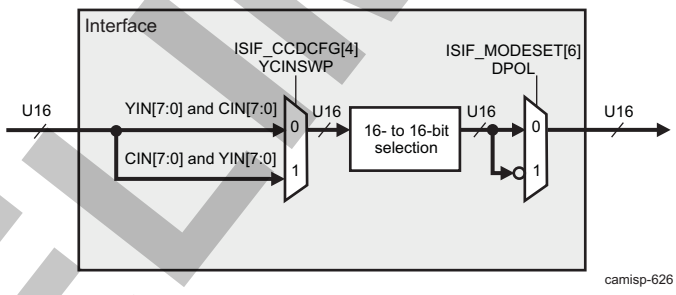
The input interface is a video interface. It comprises the horizontal (HD) and vertical (VD) synchronization signal, pixel clock (PCLK), and data (DATA). Table 8-445 gives more information about these different signals. The ISIF uses the HD and VD signals provided by the sensor through the VP and IPIPEIF. The pixel clock clocks data into the ISIF at a maximum rate of 304 MHz.

Table 8-445. ISS ISP ISIF Input Interface Signals

Name	I/O	Function
VD	I	Vertical sync signal
HD	I	Horizontal sync signal
PCLK	I	Pixel clock. This signal is the pixel clock used to load image data into the ISIF. The clock controller can configure to trigger on the rising or falling edge of the PCLK signal.
DATA	I	Data. The data interface is a 16-bit interface. When the ISIF is configured to write data to SDRAM, the write-enable signal allows an external device to control which data is to be written to SDRAM. The data input can be configured from the ISIF_MODESET.INPMOD register where it can be set to RAW, YCbCr (16 bits and 8 bits). The polarity of the data can be changed from the ISIF_MODESET.DPOL as shown in Figure 8-201.

8.3.3.6.4 ISS ISP ISIF Interface

Figure 8-201. ISS ISP ISIF Interface Block Diagram



The ISIF supports 8- to 16-bit-wide RAW data signals and 8-/16-bit YCbCr signals, as described in Table 8-446. The interface can be set in the three different modes from the ISIF_MODESET[13:12] INPMOD bit field. The ISIF_CCDCFG[11] Y8POS bit selects the y signal positioning whenever YUV4:2:2 is input. Moreover, if CCIR656 input is used the width of selected bit can be set through the ISIF_CCDCFG[5] BT656 bit.

Table 8-446. ISS ISP ISIF Data Input Formats

ISIF Input Port Name	RAW Data	16-bit YCbCr	8-bit YCbCr
YI7	C_DATA15	Y7	
YI6	C_DATA14	Y6	
YI5	C_DATA13	Y5	
YI4	C_DATA12	Y4	
YI3	C_DATA11	Y3	
YI2	C_DATA10	Y2	
YI1	C_DATA9	Y1	
YI0	C_DATA8	Y0	

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Table 8-446. ISS ISP ISIF Data Input Formats (continued)

ISIF Input Port Name	RAW Data	16-bit YCbCr	8-bit YCbCr
CI7	C_DATA7	Cb7,Cr7	Y7,Cb7,Cr7
CI6	C_DATA6	Cb6,Cr6	Y6,Cb6,Cr6
CI5	C_DATA5	Cb5,Cr5	Y5,Cb5,Cr5
CI4	C_DATA4	Cb4,Cr4	Y4,Cb4,Cr4
CI3	C_DATA3	Cb3,Cr3	Y3,Cb3,Cr3
CI2	C_DATA2	Cb2,Cr2	Y2,Cb2,Cr2
CI1	C_DATA1	Cb1,Cr1	Y1,Cb1,Cr1
CI0	C_DATA0	Cb0,Cr0	Y0,Cb0,Cr0

Y and C input signals can be swapped through the ISIF_CCDCFG[4] YCINSWP bit.

In case of RAW data at ISIF input, a 16- to-16-bit selection can be done: when the number of RAW data lines is less than 16, data can be connected to the upper or lower lines of C_DATA[15:0]. Lines not connected must be tied low. As shown in Table 8-447, the ISIF_CGAMMAWD[4:1] GWDI bit field must be configured correctly so that the MSB of the input is connected to the MSB of the 16-bit data bus in ISIF.

Table 8-447. ISS ISP ISIF Raw Data Connection: Selects MSB Position of Input Data

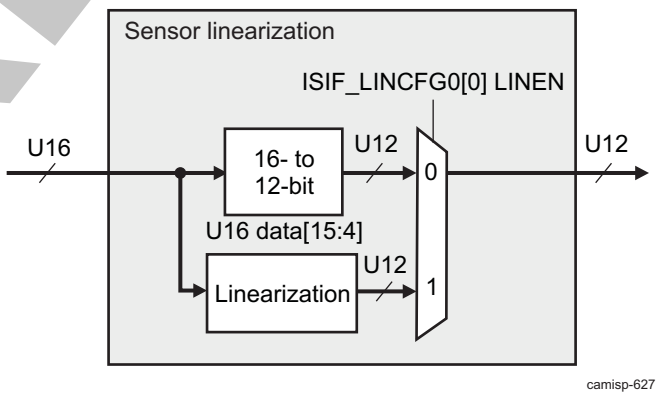
ISIF_CGAMMAWD[4:1] GWDI	16-to-16-bit Selection
0	C_DATA[15:0] = C_DATA[15:0]
1	C_DATA[15:0] = C_DATA[14:0] &0
2	C_DATA[15:0] = C_DATA[13:0] &00
3	C_DATA[15:0] = C_DATA[12:0] &000
4	C_DATA[15:0] = C_DATA[11:0] &0000
5	C_DATA[15:0] = C_DATA[10:0] &00000
6	C_DATA[15:0] = C_DATA[9:0] &000000
7	C_DATA[15:0] = C_DATA[8:0] &0000000
8	C_DATA[15:0] = C_DATA[7:0] &00000000

The polarity of the input image data can be switched through the ISIF_MODESET[6] DPOL bit.

8.3.3.6.5 ISS ISP ISIF Sensor Linearization

NOTE: For the memory access locations of the sensor linearization table, see Section 8.3.3.8, *ISS ISP Memory Mapping*.

Figure 8-202. ISS ISP ISIF Sensor Linearization Block Diagram



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The sensor linearization module can correct for the nonlinear response of image sensors. A LUT is programmed with an offset value to add to the original pixel value based on the original pixel value.

The LUT is a sampling of the linearization correction curve based on calibration of the image sensor. Intermediate values between sampling points are computed using linear interpolation. The entire correction curve is divided into seven regions, as listed in Table 8-448. The regions for the darkest part and the brightest part of the response curve have dense sampling. The linearization mode can be a uniform or a nonuniform sampling and can be set through the ISIF_LINCFG0[1] LINMD bit.

Table 8-448. ISS ISP ISIF Linearization LUT

Region	Number of Sample Points	LUT Address
table_in[15:11] == 00000	32	table_in[10:6]
table_in[15:11] == 00001	4	table_in[10:9] + 32
table_in[15:12] == 0001	4	table_in[11:10] + 36
table_in[15:13] == 001	4	table_in[12:11] + 40
table_in[15:14] == 01	4	table_in[13:12] + 44
table_in[15:14] == 10	16	table_in[13:10] + 48
table_in[15:14] == 01	128	table_in[13:7] + 64

The LUT has 192 entries and is split into two 96 × 10-bit memories, as shown in Figure 8-203. Table 8-449 is mapped in the memory map. The LUT entries are interleaved between memory 0 and memory 1.

Figure 8-203. ISS ISP ISIF Linearization LUT Memories

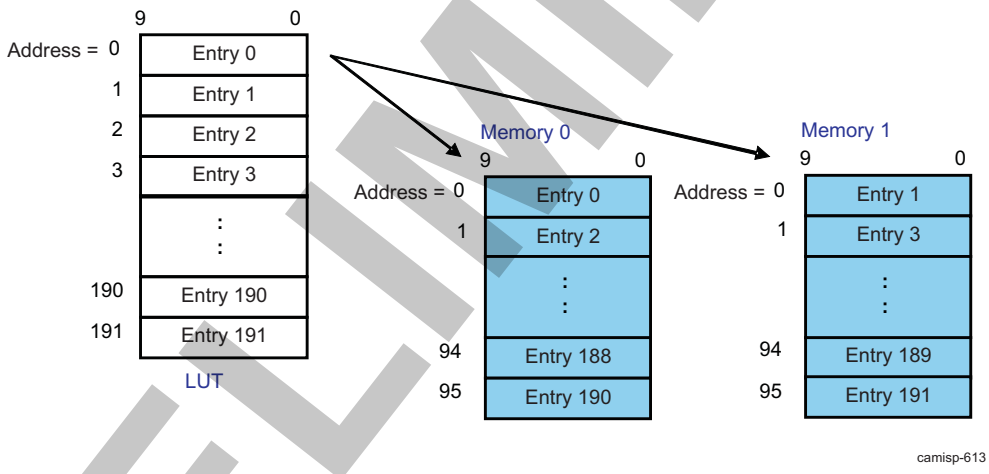

Table 8-449. ISS ISP ISIF LUT Memory Region

Memory Region	Address Range	Description
Memory 0	0xC000 – 0xC17F	ISIF linearity compensation LUT 0
Memory 1	0xC400 – C57F	ISIF linearity compensation LUT 1

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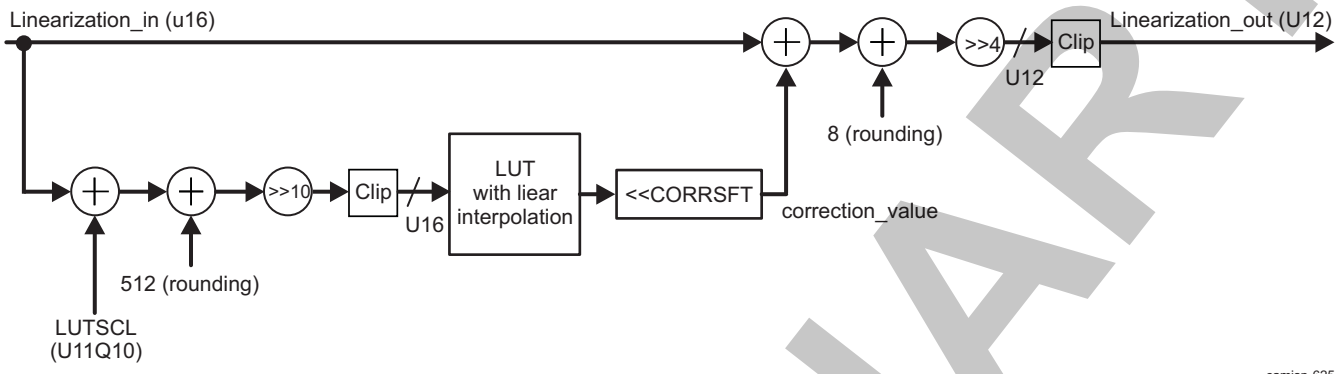
A scale factor is applied to the input before lookup through the ISIF_LINCFG1[10:0] LUTSCL bit field. The LUT entries are signed 10-bit data (u16). After linear interpolation, the correction value is left-shifted by a programmable amount (the ISIF_LINCFG0[6:4] CORRSFT bit field), and then added to the input. This is then converted to unsigned 12-bit by right shift, followed by clipping.

Figure 8-204. ISS ISP ISIF Linearization Block Diagram



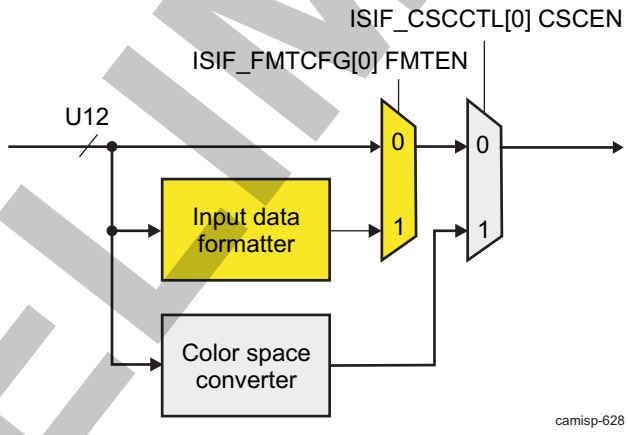
To enable the linearization module, set the ISIF_LINCFG0[0] LINEN bit to 1.

If the linearization module is disabled (ISIF_LINCFG0[0] LINEN = 0x0), a 16- to-12-bit transformation is done, and the upper 12 bits of U16 input are sent to the next block.

8.3.3.6.6 ISS ISP ISIF Input Data Formatter

Figure 8-205 shows the ISS ISP ISIF input data formatter block diagram.

Figure 8-205. ISS ISP ISIF Input Data Formatter Block Diagram



There are two functional blocks: input data formatter and color space converter, which use two 5376 × 12-bit memories (corresponds to one line of maximum 5376 pixels with each pixel equal to 12 bits). Only one of the function blocks can be enabled.

The input data formatter block allows the ISIF to handle a wide variety of current and future readout schemes other than Bayer format. Two line memories and a programmable address generator are used to translate those patterns into a standard Bayer pattern (or any other pattern). This allows the back-end processing (noise filters, interpolation, histogram, 3A statistics) to remain unchanged.

The input data formatter block also supports divided input lines. In case an input line is divided into multiple lines and fed to the ISIF, the formatter gathers the divided lines and organizes a single line. Up to four divided lines can be supported.

The input data formatter is enabled through the ISIF_FMTCFG[0] FMTEN bit.

The input data formatter can split an input line into one, two, three, or four output lines, or can combine the divided by one, two, three, or four input lines into a single line.

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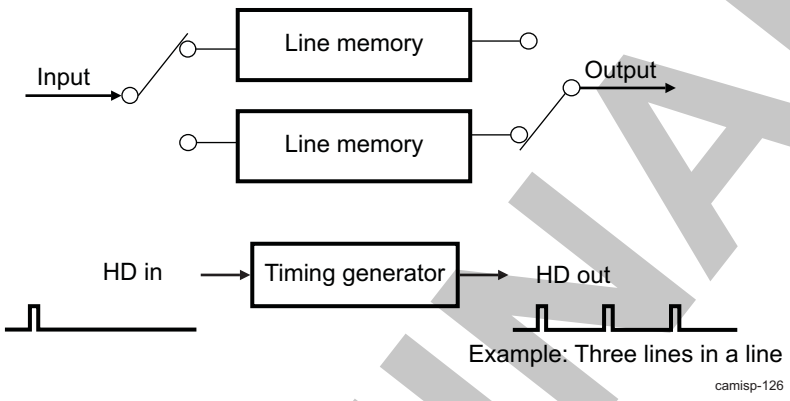
- Set the ISIF_FMTCFG[1] FMTCBL bit to 0 for split mode.
- Set the ISIF_FMTCFG[1] FMTCBL bit to 1 for combine mode.
- Select the number of lines in the ISIF_FMTCFG[5:4] LNUM bit field.

The input data formatter can work in normal or line alternative mode. The choice is done through the ISIF_FMTCFG[2] LNALT bit.

Figure 8-206 shows an example of generating three output lines from an input line with a new, internally generated HD signal.

Figure 8-206. ISS ISP ISIF Splits an Input Line Into Three Output Lines



This HD signal then gates the downstream processing rather than the original sensor HD signal. Descriptions of how to configure the formatter are provided in the following sections.

Because the size of the line memories is 5376 × 12 bits, the following restrictions apply for the data formatter:

- Split mode:
  - The maximum number of pixels that can be supported in an output line if the input line is transformed into one output line is 5376.
  - The maximum number of pixels that can be supported in an output line if the input line is transformed into two output lines is 2688.
  - The maximum number of pixels that can be supported in an output line if the input line is transformed into three output lines is 1792.
  - The maximum number of pixels that can be supported in an output line if the input line is transformed into four output lines is 1344.
- Combine mode:
  - The maximum number of pixels that can be supported in an input line if one input line is transformed into an output line is 5376.
  - The maximum number of pixels that can be supported in an input line if two input lines are transformed into an output line is 2668.
  - The maximum number of pixels that can be supported in an input line if three input lines are transformed into an output line is 1792.
  - The maximum number of pixels that can be supported in an input line if four input lines are transformed into an output line is 1344.

8.3.3.6.6.1 ISS ISP ISIF Formatter Area Settings

As shown in Figure 8-207, the following registers are used to set the formatter area:

- ISIF_FMTSPH
- ISIF_FMTLNH
- ISIF_FMTLSV
- ISIF_FMTLNV

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Figure 8-207. ISS ISP ISIF Input Data Formatter Area Settings

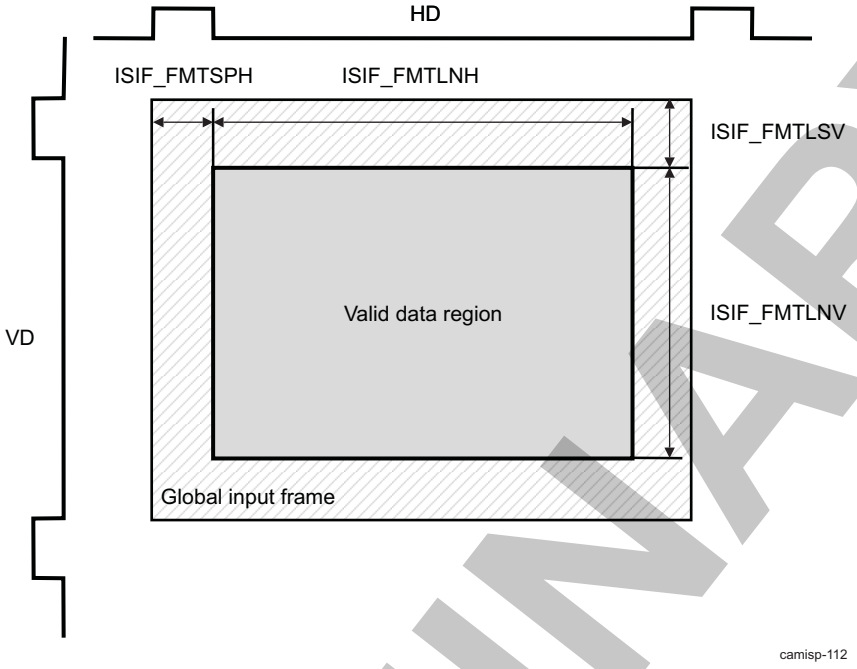

Table 8-450 and Table 8-451 describe these registers. The input line is input to the formatter, and the output line is output from the formatter.

Table 8-450. ISS ISP ISIF Input Data Formatter Area Setting Registers

Register	Description
ISIF_FMTSPH	The first valid pixel of an input line
ISIF_FMTLNH	Valid length of a input line = FMTLNH + 1
ISIF_FMTLSV	The first valid input line
ISIF_FMTLNV	The number of the valid input lines = FMTLNV + 1

Table 8-451. ISS ISP ISIF Output Data Formatter Area Setting Registers

Register	Description
ISIF_FMTRLEN	The length of an output line
ISIF_FMTHCNT	HD interval for output lines
ISIF_SPH	The first pixel in an output line to be stored to SDRAM
ISIF_LNH	The number of pixels in an output line to be stored to SDRAM = LNH + 1
ISIF_LNV	The number of the output lines to be stored to SDRAM = LNV + 1

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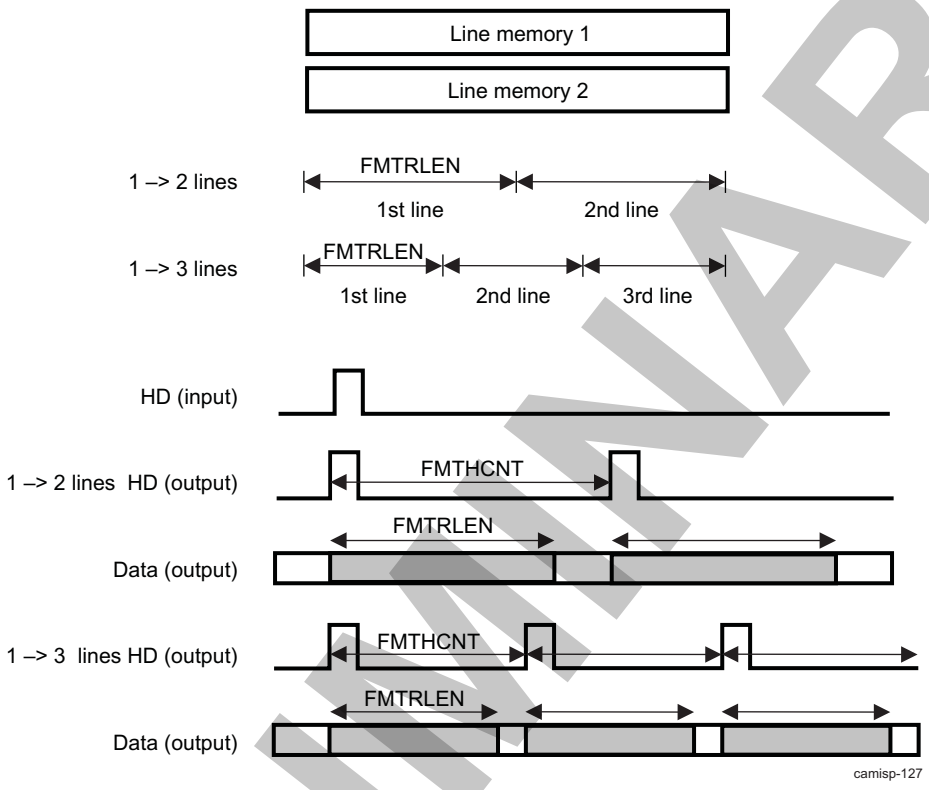
The number of pixels in an output line must be set to the ISIF_FMTRLEN register, and the HD output interval must be set to the ISIF_FMTHCNT register. It is not necessary to set the ISIF_FMTHCNT register if multiple input lines are combined into a single line.

Figure 8-208 shows an example of splitting an input line into two or three output lines.

Figure 8-208. ISS ISP ISIF Data Formatter Output Control Example



8.3.3.6.6.2 ISS ISP ISIF Formatter Programming

The data formatter derives its flexibility by supporting up to 16 different addresses and a program that can contain up to 32 entries.

Address pointer

There are 16 address pointer registers (ISIF_FMTAPTR0 to ISIF_FMTAPTR15), which contain:

- The ISIF_FMTAPTRx[14:13] LINE bit field: 2-bit line number to specify the output line to which it belongs: 0, 1, 2, or 3. It is valid only for the line splitting.
- The ISIF_FMTAPTRx[12:0] INIT bit field: 13-bit initial address for pointer x (where x = 0 to 15)

Each address value is auto-incremented or auto-decremented by a programmable value (the ISIF_FMTCFG[11:8] FMTAINC bit field).

Program

There are 32 program entry registers, which contain:

- In the ISIF_FMTPGMVF0 and ISIF_FMTPGMVF1 registers: The PGMxxEN fields set the program entry valid flag (where xx = 00 to 31) .
- In the ISIF_FMTPGMAPS0 to ISIF_FMTPGMAPS7 registers: The PGMxxAPTR fields specify the program xx address pointer (where xx = 00 to 31).
- In the ISIF_FMTPGMAPU0 and ISIF_FMTPGMAPU1 registers: The PGMxxUPDT fields set the program xx address update (increment or decrement) (where xx = 00 to 31).

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Because each program entry has a valid flag, the formatter can also support images larger than the memory limit (length: 4480) by not choosing some of the entries.

The total program memory of 32 entries is divided into two or four sets:

- Program memory of 16 entries each for odd and even lines to split the line:
  - SET0 for even input line: Program entry 015
  - SET1 for odd input line: Program entry 1631
- Program memory of eight entries for up to four input lines to combine the lines:
  - SET0 for first input line: Program entry 07
  - SET1 for second input line: Program entry 815
  - SET2 for third input line: Program entry 1623
  - SET3 for fourth input line: Program entry 2431

The number of program entries per set must be specified by the ISIF_FMTPLEN register as follows:

- Number of program entries for SET0: ISIF_FMTPLEN[3:0] FMTPLEN0
- Number of program entries for SET1: ISIF_FMTPLEN[7:4] FMTPLEN1
- Number of program entries for SET2: ISIF_FMTPLEN[10:8] FMTPLEN2
- Number of program entries for SET3: ISIF_FMTPLEN[14:12] FMTPLEN3

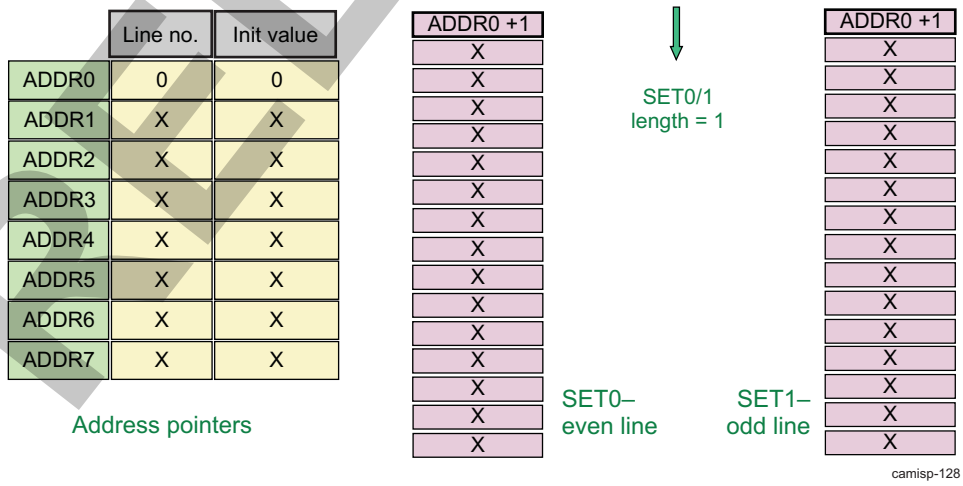
The program entry must be set from the lower registers within a set. For instance, start from program entry 16 for odd input lines.

The following examples show the programmability of the data formatter:

- Register settings:
  - ISIF_FMTCFG[0] FMTEN = 0x1
  - ISIF_FMTCFG[1] FMTCBL = 0x0
  - ISIF_FMTCFG[11:8] FMTAINC = 0x0 (add or subtract 1)
- 1 input line –> 1 output line

NOTE: ADDR0 is set to an example value. Addresses with no value in the following example are marked with X.

Figure 8-209. ISS ISP ISIF Conventional Read-Out Pattern



The following examples show the programmability of the data formatter with a 2-tap analog front end (AFE):

- Register settings:
  - ISIF_FMTCFG[0] FMTEN = 0x1

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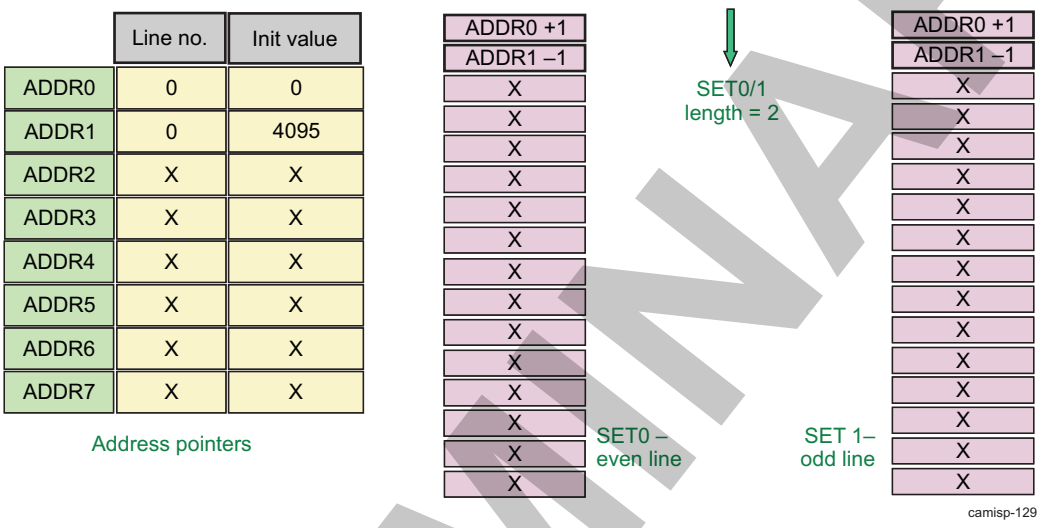
  - ISIF_FMTCFG[1] FMTCBL = 0x0
  - ISIF_FMTCFG[11:8] FMTAINC = 0x0 (add or subtract 1)
  - ISIF_FMTCFG[5:4] LNUM = 0x0
- One input line (4096): one output line with left and right read-out
- Input: First pixel, last pixel, first pixel + 1, last pixel – 1, and so on
- Input: 0, 4095, 1, 4094, 2, 4093, 3, 4092, ..., 2047 and 2048
- Output: 0, 1, 2, 3, ..., 4094 and 4095

Figure 8-210. ISS ISP ISIF Conventional Read-Out Pattern With 2-tap AFE



8.3.3.6.6.3 ISS ISP ISIF Combine the Divided Input Lines

The formatter can gather the divided input lines and organize a single line. Figure 8-211 shows an example generating a single output line from three input lines and masking two out of three HD input pulses.

Figure 8-211. ISS ISP ISIF Combine Three Input Lines Into Single Line

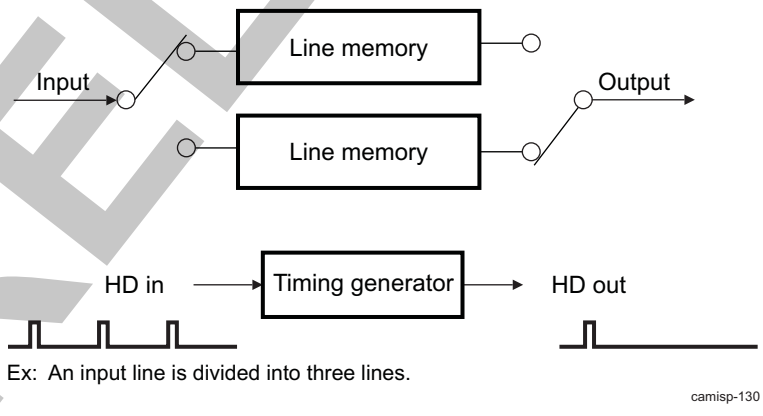


Figure 8-212 is an example that shows the register setting.

- Multiple input lines combined into one output line (use three input lines to one output line in this example)
- Input: 4, 5, 10, 11, ..., 2, 3, 8, 9, ..., 0, 1, 6, 7, ... (three lines read from sensor)
- Output: 0, 1, 2, 3, ... (1 line output)
- Register settings:

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- ISIF_FMTCFG[0] FMTEN = 0x1
- ISIF_FMTCFG[1] FMTCBL = 0x1
- ISIF_FMTCFG[11:8] FMTAINC = 0x5 (add or subtract 6)
- ISIF_FMTCFG[5:4] LNUM = 0x2
- Sets recycled based on LNUM

Figure 8-212. ISS ISP ISIF Example of Combining Three Input Lines Into a Single Line

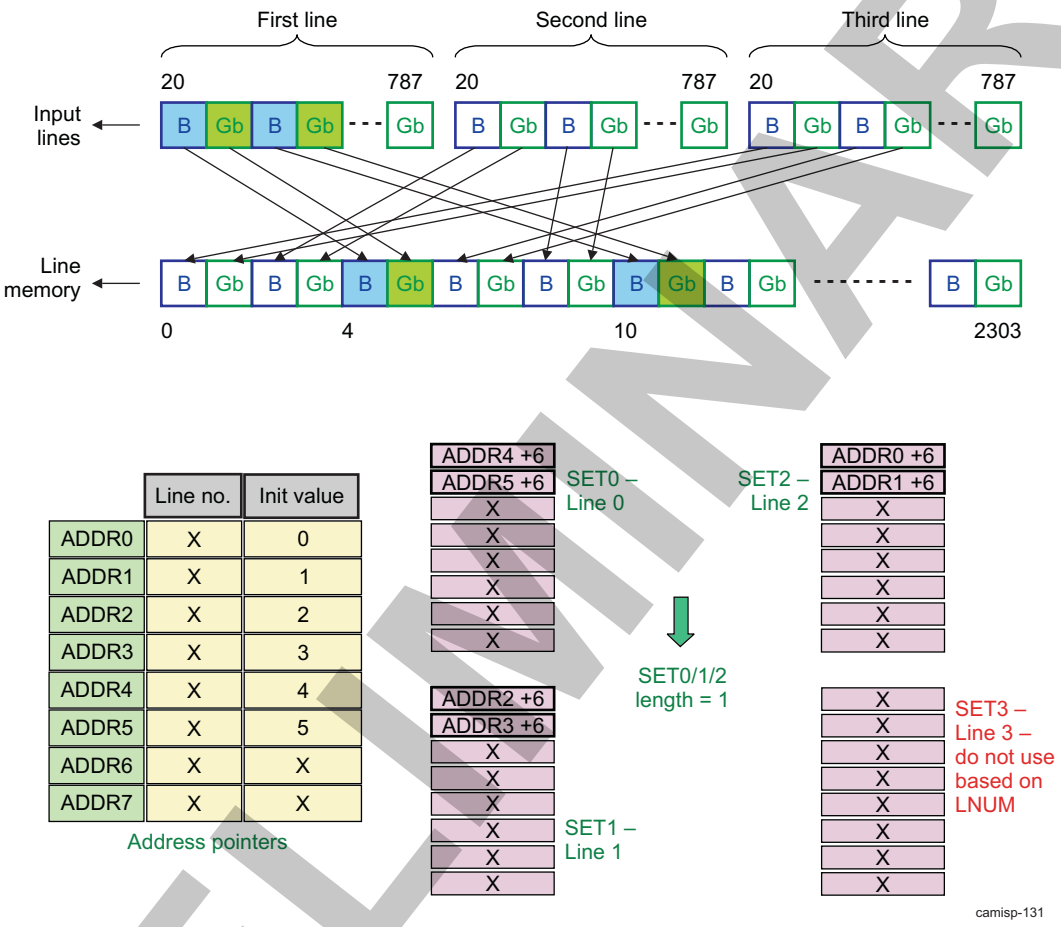

Table 8-452 lists an example of the ISS ISP ISIF combining three input lines into a single line.

Table 8-452. ISS ISP ISIF Example of Combining Three Input Lines Into a Single Line: Register Setting Example

Step	Configuration Required	Size
Formatter enable	ISIF_FMTCFG[0] FMTEN	1
Combine input lines.	ISIF_FMTCFG[1] FMTCBL	1
Address increment = FMTAINC + 1 = 6	ISIF_FMTCFG[11:8] FMTAINC	5
The first valid pixel of a divided line	ISIF_FMTSPH[12:0] FMTSPH	20
Valid length of a divided line = FMTLNH + 1 = 768	ISIF_FMTLNH[12:0] FMTLNH	767
The first valid divided line	ISIF_FMTLSV[12:0] FMTSLV	16
The number of the valid divided lines = FMTLNV + 1 = 4590	ISIF_FMTLNV[14:0] FMTLNV	4589
The length of an organized line = (FMTLNH + 1) x (LNUM + 1) = 2304	ISIF_FMTRLEN[12:0] FMTRLEN	2304
Split/combine line number = LNUM + 1 = 3	ISIF_FMTCFG[5:4] LNUM	2
Number of PGM entries for SET0 = FMTPLEN0 + 1 = 2	ISIF_FMTPLEN[3:0] FMTPLEN0	1

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Table 8-452. ISS ISP ISIF Example of Combining Three Input Lines Into a Single Line: Register Setting Example (continued)

Step	Configuration Required	Size
Number of PGM entries for SET1 = FMTPLEN1 + 1 = 2	ISIF_FMTPLEN[7:4] FMTPLEN1	1
Number of PGM entries for SET2 = FMTPLEN2 + 1 = 2	ISIF_FMTPLEN[10:8] FMTPLEN2	1
Address pointer 0, INIT = 0	ISIF_FMTAPTR0[12:0] INIT	0
Address pointer 1, INIT = 1	ISIF_FMTAPTR1[12:0] INIT	1
Address pointer 2, INIT = 2	ISIF_FMTAPTR2[12:0] INIT	2
Address pointer 3, INIT = 3	ISIF_FMTAPTR3[12:0] INIT	3
Address pointer 4, INIT = 4	ISIF_FMTAPTR4[12:0] INIT	4
Address pointer 5, INIT = 5	ISIF_FMTAPTR5[12:0] INIT	5
Program 0 valid flag	ISIF_FMTPGMVF0[0] PGM00EN	1
Program 1 valid flag	ISIF_FMTPGMVF0[1] PGM01EN	1
Program 8 valid flag	ISIF_FMTPGMVF0[8] PGM08EN	1
Program 9 valid flag	ISIF_FMTPGMVF0[9] PGM09EN	1
Program 16 valid flag	ISIF_FMTPGMVF1[0] PGM16EN	1
Program 17 valid flag	ISIF_FMTPGMVF1[1] PGM17EN	1
Increment address pointer = 0x0 Program 0 address pointer = ADDR4 + 6	ISIF_FMTPGMAPU0[0] PGM0UPDT ISIF_FMTPGMAPS0[3:0] PGM0APTR	4
Increment address pointer = 0x0 Program 1 address pointer = ADDR5 + 6	ISIF_FMTPGMAPU0[1] PGM1UPDT ISIF_FMTPGMAPS0[7:4] PGM1APTR	5
Increment address pointer = 0x0 Program 8 address pointer = ADDR2 + 6	ISIF_FMTPGMAPU0[8] PGM8UPDT ISIF_FMTPGMAPS2[3:0] PGM8APTR	2
Increment address pointer = 0x0 Program 9 address pointer = ADDR3 + 6	ISIF_FMTPGMAPU0[9] PGM9UPDT ISIF_FMTPGMAPS2[7:4] PGM9APTR	3
Increment address pointer = 0x0 Program 16 address pointer = ADDR0 + 6	ISIF_FMTPGMAPU1[1] PGM17UPDT ISIF_FMTPGMAPS4[3:0] PGM16APTR	0
Increment address pointer = 0x0 Program 17 address pointer = ADDR1 + 6	ISIF_FMTPGMAPU1[0] PGM16UPDT ISIF_FMTPGMAPS4[7:4] PGM17APTR	1

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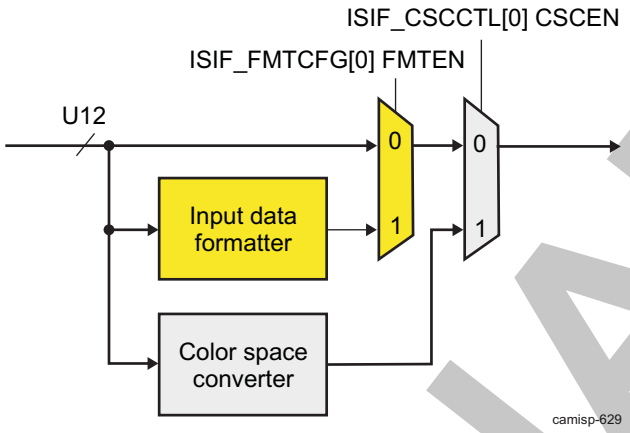
8.3.3.6.7 ISS ISP ISIF Color Space Converter

Figure 8-213 shows the ISS ISP ISIF Color Space Converter Block Diagram.

Figure 8-213. ISS ISP ISIF Color Space Converter Block Diagram



The color space converter (CSC) includes four 8-bit × 12-bit multipliers and one adder for the color space conversion. These multiplier/adder units are used for the operation described in Figure 8-214. Data are taken from two input lines during the operation.

Coefficients are signed 8-bit (decimal is 5 bits). Coefficients are set through the following registers:

- Coefficient M00: ISIF_CSCM0[7:0] CSCM00
- Coefficient M01: ISIF_CSCM0[15:8] CSCM01
- Coefficient M02: ISIF_CSCM1[7:0] CSCM02
- Coefficient M03: ISIF_CSCM1[15:8] CSCM03
- Coefficient M10: ISIF_CSCM2[7:0] CSCM10
- Coefficient M11: ISIF_CSCM2[15:8] CSCM11
- Coefficient M12: ISIF_CSCM3[7:0] CSCM12
- Coefficient M13: ISIF_CSCM3[15:8] CSCM13
- Coefficient M20: ISIF_CSCM4[7:0] CSCM20
- Coefficient M21: ISIF_CSCM4[15:8] CSCM21
- Coefficient M22: ISIF_CSCM5[7:0] CSCM22
- Coefficient M23: ISIF_CSCM5[15:8] CSCM23
- Coefficient M30: ISIF_CSCM6[7:0] CSCM30
- Coefficient M31: ISIF_CSCM6[15:8] CSCM31
- Coefficient M32: ISIF_CSCM7[7:0] CSCM32
- Coefficient M33: ISIF_CSCM7[15:8] CSCM33

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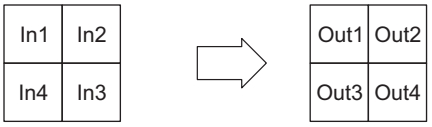
Figure 8-214. ISS ISP ISIF Color Space Converter Operation



$$\begin{pmatrix} Out1 \\ Out2 \\ Out3 \\ Out4 \end{pmatrix} = \begin{pmatrix} M00 & M01 & M02 & M03 \\ M10 & M11 & M12 & M13 \\ M20 & M21 & M22 & M23 \\ M30 & M31 & M32 & M33 \end{pmatrix} \begin{pmatrix} In1 \\ In2 \\ In3 \\ In4 \end{pmatrix}$$

M00–M33: Signed 8-bit data with 5-bit decimal
the value range –4=< Mxx<4

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The CSC can convert CMYG filtered CCD data to Bayer matrix (RGBG) data, as shown in Figure 8-215.

Figure 8-215. ISS ISP ISIF Color Space Converter Operation: CMYG to RGBG

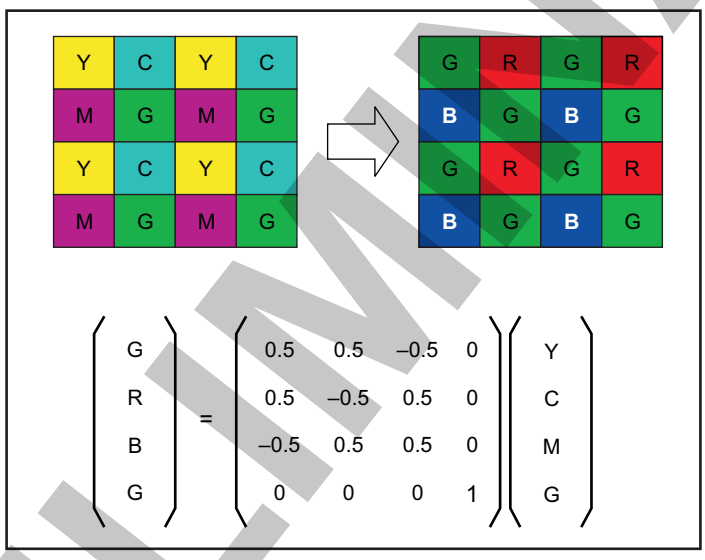

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Figure 8-216 through Figure 8-218 show which input pixels are used for the operation. There is 1line latency between the input and the output.

Figure 8-216. ISS ISP ISIF Color Space Conversion Example

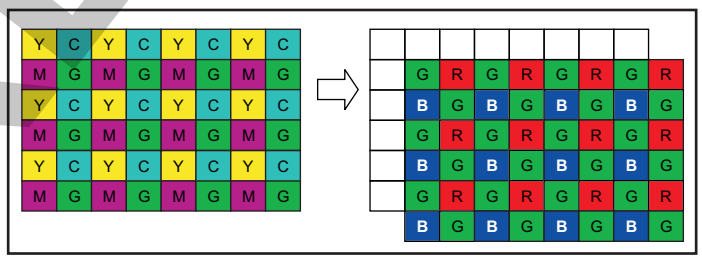

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Figure 8-217. ISS ISP ISIF First Pixel/First Line Generation

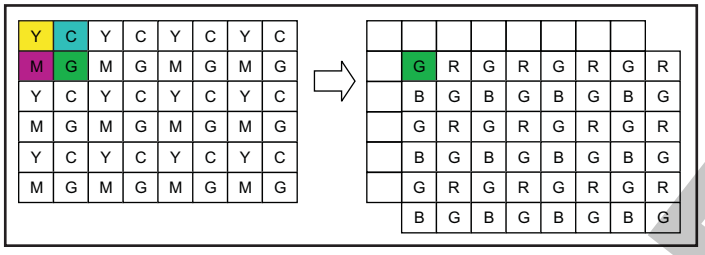
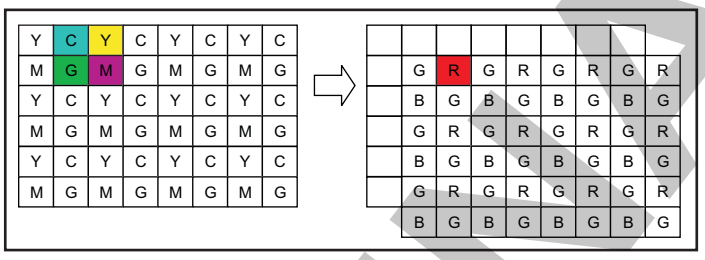


Figure 8-218. ISS ISP ISIF Second Pixel/First Line Generation



As shown inFigure 8-219 through Figure 8-222, the operation for the last pixel and the second last pixel uses the same input data.

Figure 8-219. ISS ISP ISIF Second Last Pixel/First Line Generation

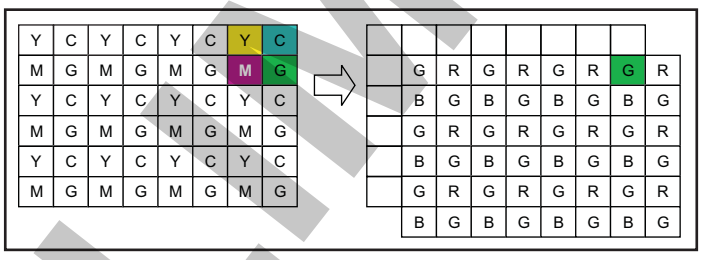


Figure 8-220. ISS ISP ISIF Last Pixel/First Line Generation

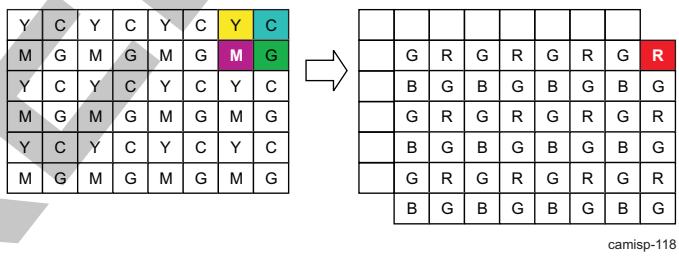


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Figure 8-221. ISS ISP ISIF First Pixel/Last Line Generation

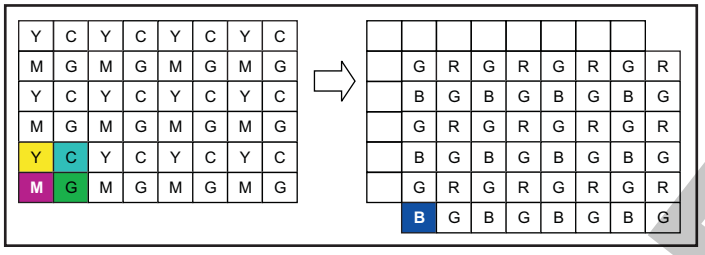
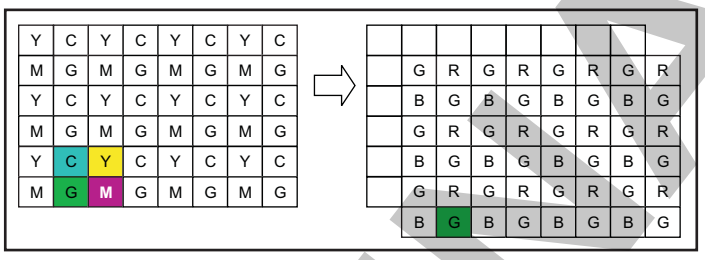


Figure 8-222. ISS ISP ISIF Second Pixel/Last Line Generation



Also, the operation for the last line and the second last line uses the same input data (see Figure 8-223 and Figure 8-224).

Figure 8-223. ISS ISP ISIF Second Last Pixel/Last Line Generation

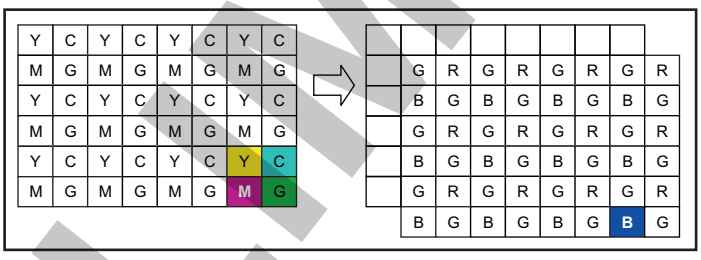
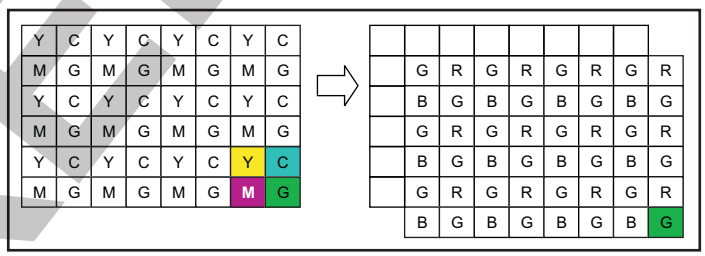


Figure 8-224. ISS ISP ISIF Last Pixel/Last Line Generation



In addition to the registers specific to the CSC, some of the registers are shared with the input data formatter to configure the valid area:

- ISIF_FMTSPH
- ISIF_FMTLNH
- ISIF_FMTLSV
- ISIF_FMTLNV

There must be at least 1 invalid pixel at the end of the line and one invalid line at the end of the frame.

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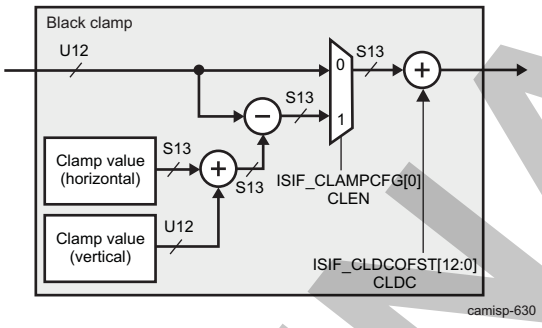
To enable the color space conversion, set the ISIF_CSCCTL[0] CSCEN bit to 1.

8.3.3.6.8 ISS ISP ISIF Black Clamp

NOTE: For the memory access locations of the ISIF clamp, see Section 8.3.3.8, *ISS ISP Memory Mapping*.

Figure 8-225 shows the ISS ISP ISIF black clamp block diagram.

Figure 8-225. ISS ISP ISIF Black Clamp Block Diagram



The clamp value is calculated based on the pixel value of the OB region of the sensor. The clamp value is calculated separately for horizontal and vertical directions to compensate the offset drift in the horizontal and vertical directions. The sum of the horizontal and vertical clamp values is subtracted from the image data, and then the additional DC offset is added (the ISIF_CLDCOFST[12:0] CLDC bit field, an S13Q0 value). This value is added whether the black clamp module is enabled or not.

The horizontal clamp is disabled through the ISIF_CLAMPCFG[2:1] CLHMD bit field.

To enable the black clamp module, set the ISIF_CLAMPCFG[0] CLEN bit to 1. The ISIF_PPLN[15:0] PPLN bit field sets the pixel per line, and the number of pixel clock periods in one line HD period equals PPLN + 1 pixel clock. The ISIF_PPLN[15:0] bit field is not used when the input is are already HD/VD.

8.3.3.6.8.1 ISS ISP ISIF Clamp Value for Horizontal Direction

The clamp value for horizontal direction is calculated using the pixel values at the upper OB region.

The maximum pixel value to be used for the clamp value calculation can be limited to 1023 if the pixel value limitation is enabled (ISIF_CLHWIN0[6] CLHLMT = 1).

Clamp value calculation for horizontal direction can be disabled if there is no upper OB region. The operating modes are:

- The horizontal clamp value calculation is enabled. The calculated horizontal clamp value is subtracted from the image data along with the vertical clamp value (ISIF_CLAMPCFG[2:1] CLHMD = 0x1).
- The horizontal clamp value is not updated. The horizontal clamp value used for the previous image is subtracted from the image data along with the vertical clamp value (ISIF_CLAMPCFG[2:1] CLHMD = 0x2).
- The horizontal clamp value is not updated. Only the vertical clamp value is subtracted from the image data (ISIF_CLAMPCFG[2:1] CLHMD = 0x0).

The number of windows in a row is set with the ISIF_CLHWIN0[4:0] CLHWC bit field.

Up to 32 windows in a row can be set for clamp value calculation. All the windows have the same size in a format [$2^{(ISIF\_CLHWIN0[9:8]\ CLHWM+5)}$] pixels by [$2^{(ISIF\_CLHWIN0[13:12]\ CLHWN+1)}$] lines.

The ISIF_CLHWIN2[12:0] CLHSV and ISIF_CLHWIN1[12:0] CLHSH bit fields enable setting the position of the first optical black clamp window in the frame. The pixel and line offset are in a range 0 to 8191. The ISIF_HDW register sets the width of the HD.

Figure 8-226 shows the ISS ISP ISIF clamp value for the horizontal direction.

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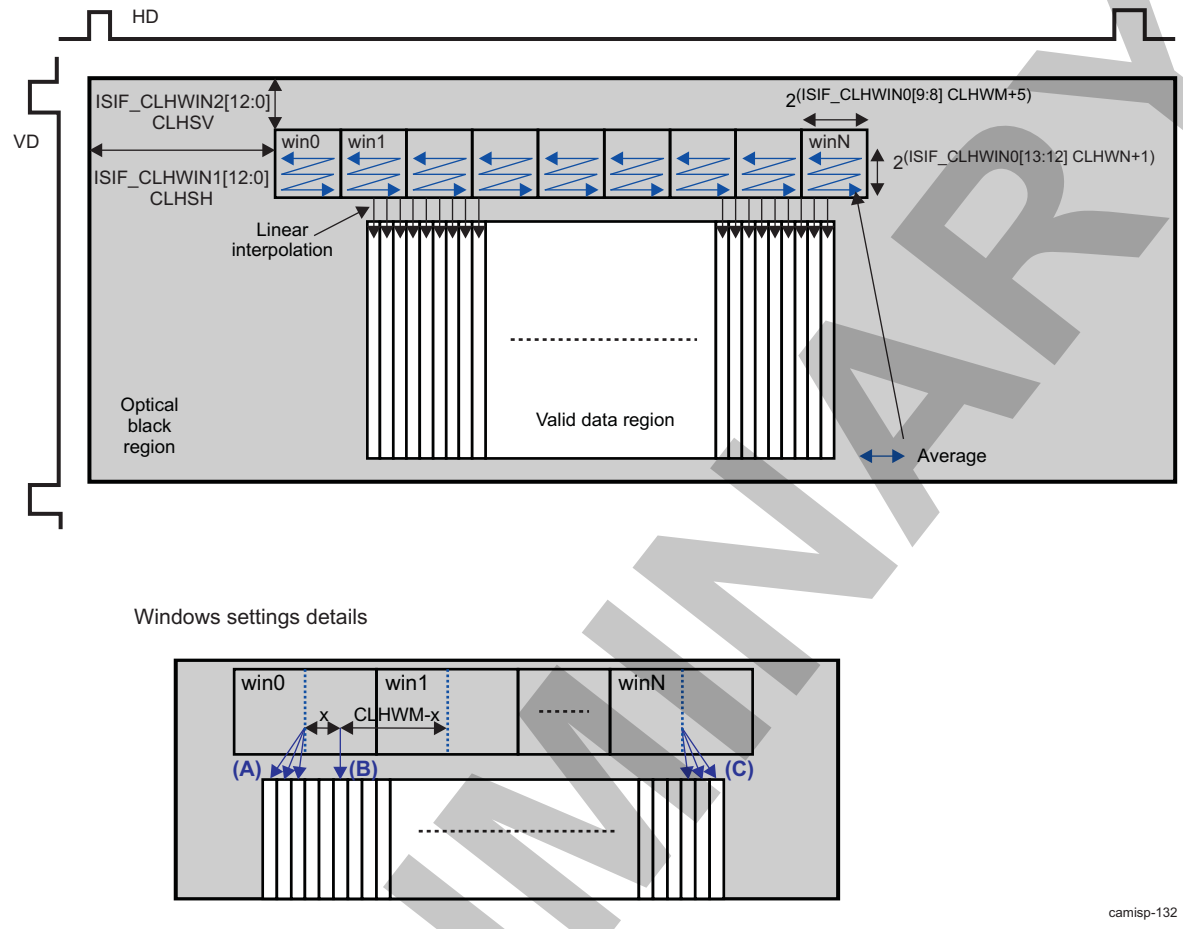
Figure 8-226. ISS ISP ISIF Clamp Value for Horizontal Direction



The clamp value for horizontal direction calculation steps is:

1. Calculate the average of the pixel value in each window (ave_win_0 to ave_win_N).

Calculation Steps	win0	win1	win2	...	wini	wini + 1	...	winN
Average of the pixel value	ave_win_0	ave_win_1	ave_win_2		ave_win_i	ave_win_{i+1}		ave_win_N

2. Set the average of the left-most window or the right-most window as the base value B_V:
   - B_V = ave_win_0 (if ISIF_CLHWIN0[5] CLHWBS = 0x0, case 1)
   - B_V = ave_win_N (if ISIF_CLHWIN0[5] CLHWBS = 0x1, case 2)
3. Subtract the base value from the average of each window. Use this value as a clamp value for each window.

Calculation Steps	win0	...	wini	wini+1	...	winN
Clamp value for each window	$clamp\_win_0 = ave\_win_0 - B\_V$		$clamp\_win_i = ave\_win_i - B\_V$	$clamp\_win_{i+1} = ave\_win_{i+1} - B\_V$		$clamp\_win_N = ave\_win_N - B\_V$

4. Acquire the horizontal distance (X and CLHWM – X) from the valid pixel to be processed to the center of the closest two windows.
5. Calculate the clamp value of the valid pixel by linear interpolation, using the clamp value of the closest two windows (i and i + 1).
   - Case 1: $interpolated\_clamp\_win_X = (clamp\_win_{i+1} - clamp\_win_i) \times X / CLHWM$
   - Case 2: $interpolated\_clamp\_win_X = (clamp\_win_i - clamp\_win_N) \times (CLHWM - X) / CLHWM +$

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$(clamp\_win_{i+1} – clamp\_win_N) \times X / CLHWM$

6. If the valid pixel is on the left of the center of the left-most window, the clamp value of the left-most window is applied. If the valid pixel is on the right of the center of the right-most window, the clamp value of the right-most window is applied.

The clamp values calculated (A), (B), and (C) are:

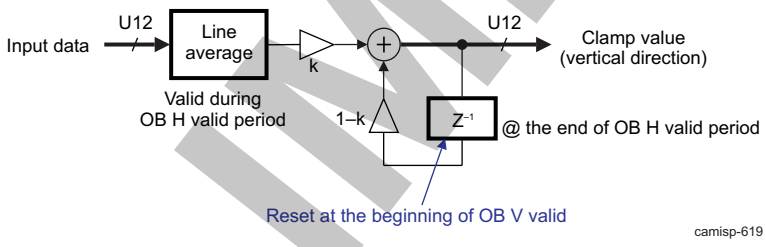
- Case1: Base is win_0 (Left-most window: ISIF_CLHWIN0[5] CLHWBS = 0x0)
  - (A): zero
  - (B): $(clamp\_win_{i+1} – clamp\_win_i) \times X / CLHWM$
  - (C): $(clamp\_win_N – clamp\_win_0)$
- Case2: Base is win_N (Right-most window: ISIF_CLHWIN0[5] CLHWBS = 0x1)
  - (A): $(clamp\_win_0 – clamp\_win_N)$
  - (B): $(clamp\_win_i – clamp\_win_N) \times (CLHWM – X) / CLHWM + (clamp\_win_{i+1} – clamp\_win_N) \times X / CLHWM$
  - (C): zero

Each interpolated value $interpolated\_clamp\_win_X$ is then subtracted to the associated column.

8.3.3.6.8.2 ISS ISP ISIF Clamp Value for Vertical Direction

The clamp value for vertical direction is calculated using the pixel values at the left or right OB region. Line average is calculated for the OB H valid period ($2^{(ISIF\_CLVWIN0[2:0]\ CLVOBH\ +\ 1)}$). The averages for the previous lines are also added back to reduce the difference between the lines, as shown in Figure 8-227.

Figure 8-227. ISS ISP ISIF Clamp Value for Vertical Direction Calculation



- Clamp Value (V_n) = Line Average (V_n) * k + Clamp Value (V_1) * (1-k)
- k = ISIF_CLVWIN0[15:8] CLVCOEF

The position of the first vertical black clamp window is set with the ISIF_CLVWIN2[12:0] CLVSV and ISIF_CLVWIN1[12:0] CLVSH bit fields. The number of vertical windows is set with the ISIF_CLVWIN3[12:0] CLVOBV bit field. ISIF_VDW sets the width of the VD.

The accumulator, which holds the vertical clamp value for the previous line, is reset at the beginning of the OB V valid. The reset value can be selected through the ISIF_CLVWIN0[5:4] CLVRVSL bit field:

- ISIF_CLVWIN0[5:4] CLVRVSL = 0x0: The base value is calculated for horizontal direction (left-most window win_0 or right-most win_n set with ISIF_CLHWIN0[5] CLHWBS).
- ISIF_CLVWIN0[5:4] CLVRVSL = 0x1: The base value is set through the configuration register (ISIF_CLVRV[11:0] CLVRV).
- ISIF_CLVWIN0[5:4] CLVRVSL = 0x2: No update (same as the previous image)

The following figures show the OB valid settings and associated vertical clamp value calculation when OB region is at the left (see Figure 8-228) and when OB region is at the right (see Figure 8-229). Each line average value is subtracted from the associated line valid region data.

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Figure 8-228. ISS ISP ISIF Clamp Value for Vertical Direction With OB Region at the Left

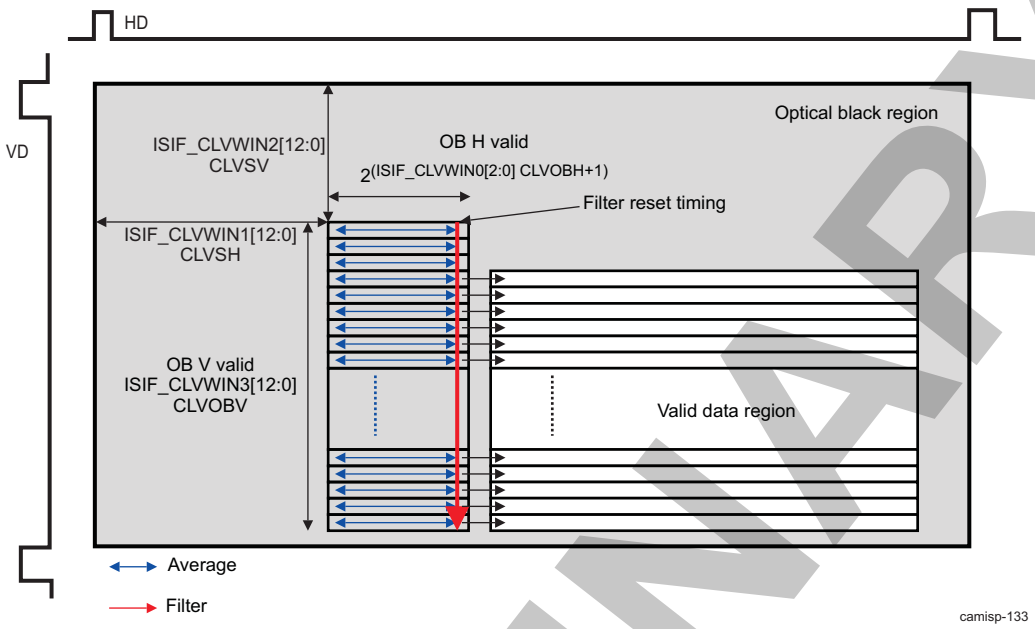
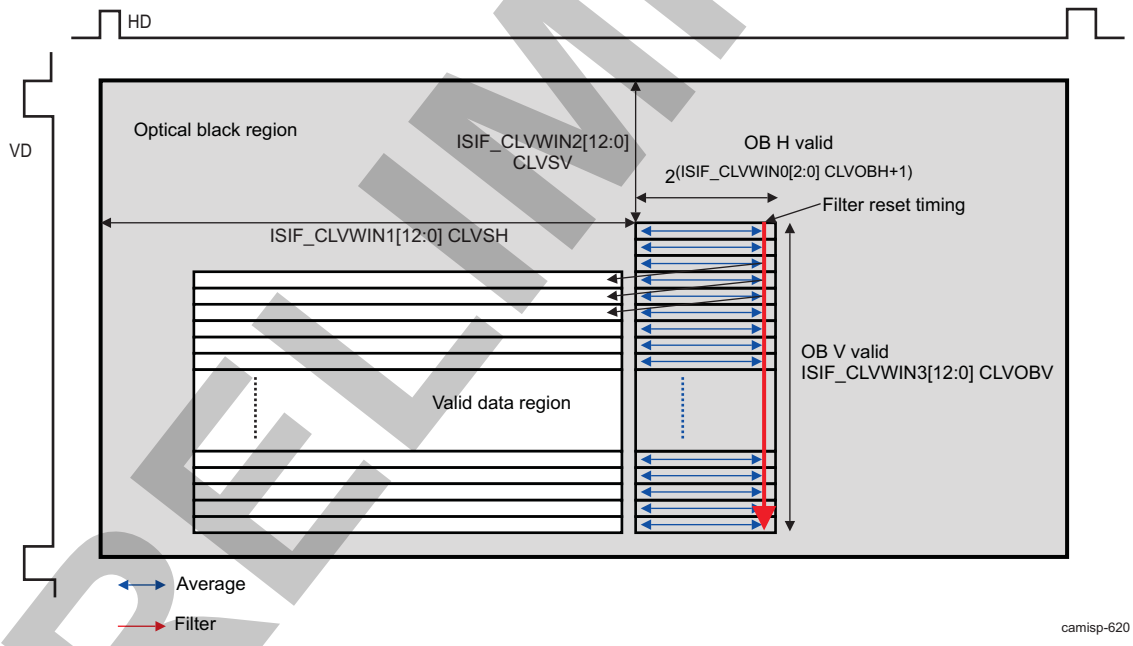


Figure 8-229. ISS ISP ISIF Clamp Value for Vertical Direction With OB Region at the Right



8.3.3.6.9 ISS ISP ISIF Vertical Line Defect Correction (VDFC)

Figure 8-230 shows the block diagram of the vertical line defect (VDFC) correction.

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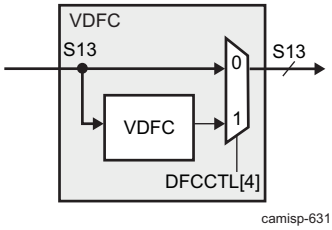
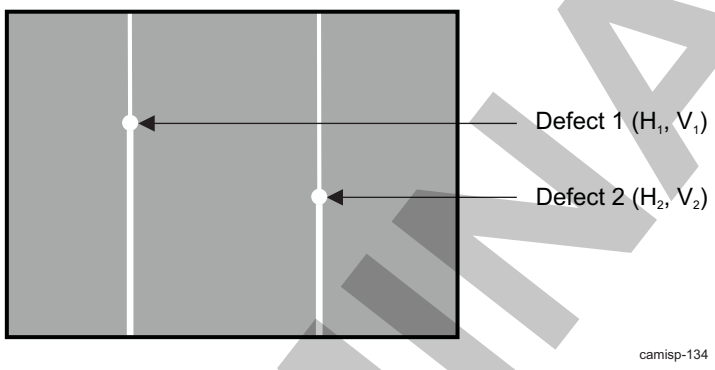
Figure 8-230. ISS ISP ISIF Vertical Line Defect Correction Block Diagram



The VDFC block can correct up to eight vertical line defects (see Figure 8-231).

Figure 8-231. ISS ISP ISIF Vertical Line Defects



The correction method is common to all the defects and can be selected through the ISIF_DFCCTL[6:5] VDFCSL bit field.

There are two different methods to correct vertical line defects (ISIF_DFCCTL[6:5] VDFCSL):

- Method 1: Data is replaced by an average (ISIF_DFCCTL[6:5] VDFCSL = 0x2):
  - The defect is replaced by the average of pixel (i – 2) and pixel (i + 2).
- Method 2: Data is subtracted by a defect level (ISIF_DFCCTL[6:5] VDFCSL = 0x0 or 0x1):
  - A saturation level is defined in the ISIF_VDFSATLV[11:0] VDFSLV bit field.
  - The coordinates of the defect:
    - Are defined in the ISIF_DFCMEM0[12:0] DFCMEM0 and ISIF_DFCMEM1[12:0] DFCMEM1 bit fields
    - Are 13 bits wide for horizontal and vertical direction, so an image size up to 8192 × 8192 is supported
  - If the data is not saturated (data < VDFSLV):
    - The defect is corrected by subtracting the defect level. A different defect level is defined for:
      - The point of the defect (V = Vdefect): SUB1 defect level is defined in the ISIF_DFCMEM2[7:0] DFCMEM2 bit field.
      - The pixels lower than the defect (V < Vdefect): SUB2 defect level is defined in the ISIF_DFCMEM3[7:0] DFCMEM3 bit field.
      - The pixels above the defect (V > Vdefect): Defect level is defined in the ISIF_DFCMEM4[7:0] DFCMEM4 bit field.
    - Each defect level (value to be subtracted from the data) described previously can be up-shifted through the ISIF_DFCCTL[10:8] VDFLSFT bit field.
    - Vertical line defect correction for upper pixels can be disabled through the ISIF_DFCCTL[7] VDFCUDA bit.
  - If the data is saturated (VDFSLV), there are two possibilities:
    - ISIF_DFCCTL[6:5] VDFCSL = 0x0: Data is simply fed through (not subtracted).
    - ISIF_DFCCTL[6:5] VDFCSL = 0x1: Horizontal interpolation ((i 2) + (i + 2)) / 2 (data is replaced

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by interpolation or data is subtracted with interpolation)

The ISIF_LPFR register sets the number of half lines per frame or field: VD period = (L PFR+ 1) / 2 lines. LPFR is not used when HD and VD are inputs.

The following paragraphs concern only method 2 correction.

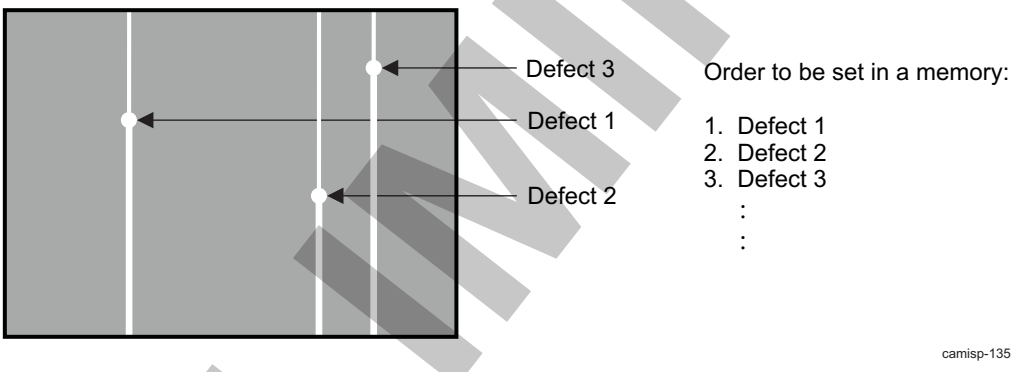
The coordinates of the defects and the defect levels to be subtracted from the data must be set to the processing listed in Table 8-453.

Table 8-453. ISS ISP ISIF Vertical Line Defect Table in Memory

Bit	Defect Information
12:0	Vertical position of the defects
25:13	Horizontal position of the defects
33:26	Defect level of the vertical line defect position (V = Vdefect)
41:34	Defect level of the pixels above the vertical line defect (V < Vdefect)
49:42	Defect level of the pixels below the vertical line defect (V > Vdefect)

The defect must be set from left to right, as shown in Figure 8-232.

Figure 8-232. ISS ISP ISIF Vertical Line Defects



Vertical line defect correction is enable by setting the ISIF_DFCCTL[4] VDFCEN bit to 1, but the procedure in Section 8.3.3.6.9.1, *ISS ISP ISIF Vertical Line Defect Table Update Procedure*, must be followed.

8.3.3.6.9.1 ISS ISP ISIF Vertical Line Defect Table Update Procedure

This procedure must be followed to write the vertical line defect table in memory.

1. ISIF_DFCMEMCTL[4] DFCMCLR = 0x1
2. Ensure that ISIF_DFCCTL[4] VDFCEN is disabled (0x0).
3. Write the V coordinate of the first defect to the ISIF_DFCMEM0[12:0] DFCMEM0 bit field.
4. Write the H coordinate of the first defect to the ISIF_DFCMEM1[12:0] DFCMEM1 bit field.
5. Set the defect level to:
   - ISIF_DFCMEM2[7:0] DFCMEM2
   - ISIF_DFCMEM3[7:0] DFCMEM3
   - ISIF_DFCMEM4[7:0] DFCMEM4
6. Set the ISIF_DFCMEMCTL[0] DFCMWR bit to 1 with the ISIF_DFCMEMCTL[2] DFCMARST bit set to 1.
7. Wait until the ISIF_DFCMEMCTL[0] DFCMWR bit is cleared.
8. Write the next data to:
   - ISIF_DFCMEM0[12:0] DFCMEM0

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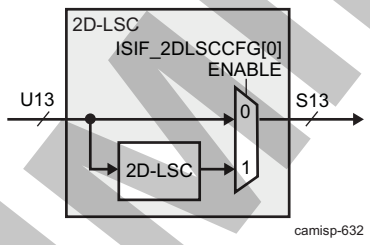
- ISIF_DFCMEM1[12:0] DFCMEM1
- ISIF_DFCMEM2[7:0] DFCMEM2
- ISIF_DFCMEM3[7:0] DFCMEM3
- ISIF_DFCMEM4[7:0] DFCMEM4

9. Set the ISIF_DFCMEMCTL[0] DFCMWR bit to 1 with the ISIF_DFCMEMCTL[2] DFCMARST bit cleared.
10. Repeat four or five times until all entries (up to eight) are written to the vertical line defect table.
11. If the defect entry is less than eight, an extra write cycle is required to fill the next table location with a certain value.
12. Clear the ISIF_DFCMEM0[12:0] DFCMEM0 bit field to all 0's, set the ISIF_DFCMEM1[12:0] DFCMEM1 to all 1's, and set the ISIF_DFCMEMCTL[0] DFCMWR bit to 1 with the ISIF_DFCMEMCTL[2] DFCMARST bit cleared.
13. Enable VDFC by setting the ISIF_DFCCTL[1] VDFCEN bit.

8.3.3.6.10 ISS ISP ISIF Lens Shading Correction Module (2D-LSC)

NOTE: For the memory access locations of the 2D-LSC table, see Section 8.3.3.8, *ISS ISP Memory Mapping*.

Figure 8-233. ISS ISP ISIF 2D-LSC Block Diagram



Lens shading correction (LSC) is useful for correcting optical artifacts that cause image brightness to decrease starting at the center of the image and going to the edges.

The LSC implements a per-pixel offset and gain adjustment in the RAW Bayer domain (2 × 2 color pattern).

- In 8-bit gain mode, when the ISIF_2DLSCCFG[6] GAIN_RANGE bit is set to 0, the offset is applied before gain multiplication.
- In 16-bit gain mode, when the ISIF_2DLSCCFG[6] GAIN_RANGE bit is set to 1, the offset function is disabled, and the loaded offset value is used to constitute the lower 8 bits of the 16-bit gain table offset table.

The offset and gains are stored in a LUT, which is stored in SDRAM and is loaded in real time. The submodule prefetches the data from SDRAM such that no underflow occurs. Underflow occurs when the offset and gain data required for the current pixel are not available.

The data stored in the LUT is downsampled; that is, there is no gain or offset per pixel. The downsampling factor is programmable. High downsampling ratios lead to a smaller LUT, lower accuracy, and lower memory bandwidth. A low downsampling ratio leads to a bigger LUT, higher accuracy, and higher memory bandwidth.

When the offset and gain values are loaded, they are upscaled to the incoming image resolution. The missing table values are computed through bilinear interpolation.

To enable the 2D-LSC module, set the ISIF_2DLSCCFG[0] ENABLE bit to 1.

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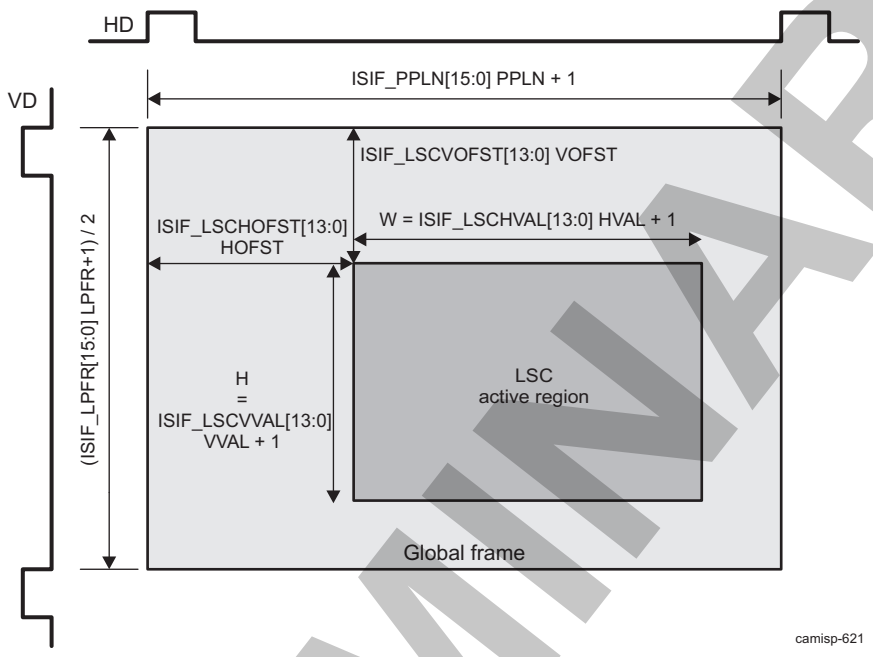
8.3.3.6.10.1 ISS ISP ISIF 2D-LSC Active Region Settings

The gain and offset maps are internally upsampled to full resolution before being applied to the image. To account for all the possible cropping schemes and zoom ratios, the 2D-LSC can be configured to store a single gain map in memory that maps to sensor lens. Figure 8-234 shows the 2D-LSC active region.

Figure 8-234. ISS ISP ISIF 2D-LSC Active Region for ISIF Input Frame



8.3.3.6.10.1.1 ISS ISP ISIF 2D-LSC Gain and Offset Tables

The gain and offset map are M × N downsampled:

- M is the horizontal sampling factor.
- N is the vertical sampling factor.
- M and N are {8, 16, 32, 64, 128} independently.
- N = M. M is set in the ISIF_2DLSCCFG[14:12] GAIN_MODE_M bit field.
- N is set in the ISIF_2DLSCCFG[10:8] GAIN_MODE_N bit field.

The starting point of the preconfigured lens shading map can be modified in software to align with the ISIF input image frame. The location of the gain and offset mask data in memory is specified as follows:

- For gain map:
  - Table base address: ISIF_2DLSCGRBU[15:0] BASE31_16 and ISIF_2DLSCGRBL[15:0] BASE15_0
- For offset map:
  - Table base address: ISIF_2DLSCORBU[15:0] BASE and ISIF_2DLSCORBL[15:0] BASE

The input address must be aligned to a 4-byte boundary.

In the full resolution case, the address is set to the beginning of the map. When the LSC active region is defined over a cropped region of the full image, the SDRAM input address can be set to the upper-left corner of the grid closest to the beginning of the active region, and the ISIF_2DLSCINI[6:0] X and ISIF_2DLSCINI[14:8] Y bit fields mark the offset into the upsampled gain and offset map where the active region begins. Figure 8-235 shows the LSC active region with respect to the gain and offset map grid. Because (X, Y) deals with the pixel phase inside a gain and offset map grid, X and Y must each be less than M and N, respectively.

Before applying the gain or offset table, the table is internally upsampled and interpolated back to full resolution via bilinear interpolation.

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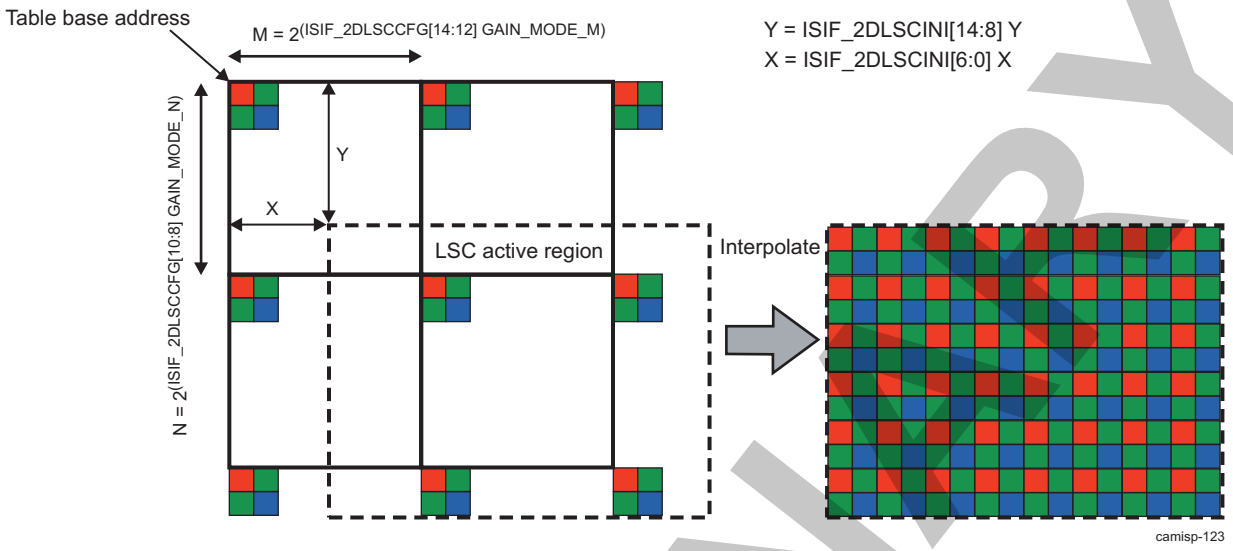
Figure 8-235. ISS ISP ISIF Gain and Offset Mask Upsampling via Bilinear Interpolation



The gain table format is set in the ISIF_2DLSCCFG[4:1] GAIN_FORMAT bit field. Eight-bit entries are supported in the gain map (in U8Q8, U8Q7, U8Q6, and U8Q5 format with an optional base of 1.0 to shift the range up).

Eight-bit entries are supported in the offset map (in S8Q0 format). An optional shifting up for offsets is possible. The shift-up value is selected through the ISIF_2DLSCOFST[6:4] OFSTSFT bit field. A scaling factor for offsets is defined in the ISIF_2DLSCOFST[15:8] OFSTSF bit field.

A 16-bit gain map is supported by combining the gain map and offset map (in U16Q16, U16Q15, U16Q14, U16Q13, U16Q12, U16Q11, U16Q10, and U16Q9 format with an optional base of 1.0 to shift the range up). This function is exclusive to offset control function, and can be configured through the ISIF_2DLSCCFG[6] GAIN_RANGE bit.

The offset control in the 2D-LSC module can be enabled or disabled through the ISIF_2DLSCOFST[0] OFSTEN bit.

For an LSC active region size of W × H (the output and input are the same size), and the gain and offset maps are M × N downsampled, a table with the following values is needed:

- (ceil[(X + W) / M] + 1) x (ceil[(Y + H) / N] + 1) × 4 bytes data in external memory organized as:
  - (ceil[(InitX + W) / M] +1) lines of data
  - Each line having at least (ceil[(InitY + H) / N] + 1) × 4 data points

  Extra data at end of each line can be skipped by the line offset register parameter:
  - For gain map:
    - Line offset: ISIF_2DLSCGROF[15:0] OFFSET
  - For offset map:
    - Line offset: ISIF_2DLSCOROF[15:0] OFFSET
  - Each line offset must start at a 32-bit aligned boundary.

8.3.3.6.10.1.2 ISS ISP ISIF 2D-LSC Gain and Offset Table Upsampling

Upsampling of the pixel-by-pixel gains is performed by locating the four same-color anchors for each destination gain value and applying bilinear interpolation.

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The gain and offset mask function is neutral to color pattern. The starting color of the gain and offset mask must be consistent with the starting color of the image, and can be any color. To align starting colors, the X and Y values must be even. The 2D-LSC engine upsamples each phase of the mask data as a separate plane and applies the upsampled mask to the image with the same color phasing. In other words, the red gains are interpolated with red gains, and applied to the red input pixels. The same process is done for the other three colors in the color pattern. The 2D-LSC module is designed to work with Bayer CFA data, having the R/Gr/Gb/B color pattern. For the purpose of functional description, assume red is the starting color, but any other starting color or other 2 × 2 pattern can be used by placing color gains in the appropriate order.

8.3.3.6.10.1.3 ISS ISP ISIF Application of Gain and Offset to Image Pixels

The gain value interpolated for each pixel is multiplied with a corresponding input pixel. An offset is applied before the gain. The product is rounded to the nearest integer and then clipped or saturated to the valid range of 13 bits.

The following equation describes the operation of the LSC in terms of offset and gain:

$$out[x,y] = (in[x,y] + a \times (ofst[x,y] << T)) \times gain[x,y] \quad (6)$$

- in[x, y] are the input pixels, 13 bits signed.
- ofst[x, y] are the upsampled offset points.
- T is the upshift value applied to the result of the offset interpolation points (0–5) set through the ISIF_2DLSCOFST[6:4] OFSTSFT bit field.
- a is the offset gain value in U8Q7 format set through the ISIF_2DLSCOFST[15:8] OFSTSF bit field.
- gain[x, y] are the upsampled gain points.
- out[x, y] are the resulting output pixels, 13 bits signed.

8.3.3.6.10.1.4 ISS ISP ISIF Enabling and Disabling the 2D-LSC Module

LSC operates on a single frame or continuously, depending on the firmware programming.

Upon power-on reset (POR), the 2D-LSC module is disabled and input pixels are copied to the output, thus bypassing any shading operation.

When enabling or disabling the 2D-LSC, caution must be taken on the timing of register modifications. To avoid causing a prefetch error or other unexpected behavior, the following safeguards must be implemented:

1. While configuring the 2D-LSC registers, the input clock into the ISIF should be toggling.
2. All of the 2D-LSC registers must be configured appropriately before enabling the ISIF_2DLSCCFG[0] ENABLE bit.
3. After setting the ENABLE bit to 1, the hardware immediately begins fetching the first two rows of gain and offset data entries from external memory. When this is complete, the ISIF_2DLSCIRQST[2] PREFETCH_COMPETED status flag is set.

NOTE: If the ENABLE bit is disabled before the ISIF_2DLSCIRQST[3] SOF status flag is set, the ISIF_2DLSCIRQST[1] PREFETCH_ERROR flag is set and the state of the 2D-LSC module may lead to unexpected errors. Therefore, the ENABLE bit must not be disabled until after the ISIF_2DLSCIRQST[3] SOF status flag is set.

4. Appropriate gains and offsets are applied to the image pixels. Pixels outside the LSC active region are passed through unaltered. When the 2D-LSC operation on the active region completes, the ISIF_2DLSCIRQST[0] DONE status flag is set.
5. At this point:
   - If the ENABLE bit is still set to 1, the hardware immediately begins to prefetch the gain and offset data entries for the next frame and waits for the active region of the next frame to arrive.
   - If the ENABLE bit is set to 0, it stops LSC operation once the active region is passed, and goes into idle mode until the ENABLE bit is reset to 1.

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NOTE: To provide a mechanism for firmware to recover from the LSC module waiting indefinitely for the input image, if the LSC_ENABLE bit is set to 0 after it has started gain/offset map prefetching, but before the LSC gets to the next active region, the LSC operation is aborted and turned idle, and any prefetched gain/offset entries are discarded. This can happen before or after the next start-of-frame.

NOTE: Therefore, because of the constraints set in point 3, the ENABLE bit must be disabled only after the ISIF_2DLSCIRQST[3] SOF status flag is set and before the ISIF_2DLSCIRQST[0] DONE status flag is set for that same frame.

It is suggested that when the 2D-LSC or the whole ISIF must be disabled for switching modes, the ISIF_2DLSCIRQST[3] SOF interrupt be enabled so that software knows when it is safe to disable the 2D-LSC. Then the ISIF can be disabled after the ISIF_2DLSCIRQST[0] DONE status signal is set for that frame.

NOTE: The LSC_ENABLE bit, once set to 1, must not be cleared until at least one vpi_clk clock cycle after start-of-frame, to ensure correct processing.

8.3.3.6.10.1.5 ISS ISP ISIF 2D-LSC Events and Status Checking

The 2D-LSC module can generate events on a single interrupt line. These events are further remapped at the ISP level in the ISP5_IRQENABLE_SET_i[3] ISIF_INT_3 bit, where i = 0 to 3.

Four 2D-LSC events can be generated:

- DONE: LSC done. This event triggers when the LSC submodules transition from ACTIVE state to IDLE state.
- PREFETCH_ERROR: Gain table prefetch error. This event triggers when the tables stored in SDRAM are read too slowly. After this event is asserted, the LSC disables the LSC computation until the beginning of the next frame.
- PREFETCH_COMPLETE: Gain table prefetch complete. This event triggers when data prefetching from SDRAM completes. Data prefetching must complete by the time the first pixel of a frame arrives. The event triggers when the buffer contains three full rows of data.
- SOF: This event signals the start of the LSC valid region. The LSC configuration registers for the next frame can be updated after the LSC SOF triggers.

The ISIF_2DLSCIRQEN register can be configured to select which events are masked and which are propagated to the LSC interrupt signal. The ISIF_2DLSCIRQST register can be read and cleared to identify which events have occurred.

In addition, the 2D-LSC module provides the following status bit:

- BUSY: This indicates that LSC has entered the active region vertically. This bit remains on during horizontal blanking, and turns off only after the entire active region of the current frame is processed.

8.3.3.6.10.1.6 ISS ISP ISIF Supported On-the-Fly 2D-LSC Configurations

The 2D-LSC prefetch memory is equal to 2 × 1536 × 32 bits. This memory is sized to fetch three lines of 8-bit gain and 8-bit offset × four color components per paxel. Given an image sensor of horizontal resolution H, there are floor [(H / ISIF_2DLSCCFG[14:12] GAIN_MODE_M) + 1] paxels per line, where M is the horizontal LSC paxel size.

Table 8-454 shows the LSC horizontal paxel size, which can be supported for different image sensor resolutions. When M = 8, some resolutions cannot be supported on the fly (orange-shaded cells in the table); the way to process such large images is to use vertical frame division.

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Table 8-454. ISS ISP ISIF Supported On-the-Fly LSC Configurations

MPix	Aspect Ratio		Line Size	Horizontal LSC Paxel Size: M = 2[ISIF_2DLSCCFG[14:12] GAIN_MODE_M]				
				8	16	32	64	128
Maximum	–	–	5376	2019	1011	507	255	129
16	16	9	5333	2003	1003	503	253	128
16	4	3	4619	1735	869	436	220	111
16	3	2	4899	1840	922	462	233	118
12	16	9	4619	1735	869	436	220	111
12	4	3	4000	1503	753	378	191	97
12	3	2	4243	1594	798	401	202	102
10	16	9	4216	1584	794	398	201	102
10	4	3	3651	1372	688	345	174	89
10	3	2	3873	1455	729	366	185	94
8	16	9	3771	1417	710	357	180	91
8	4	3	3266	1228	615	309	156	80
8	3	2	3464	1302	653	328	165	84

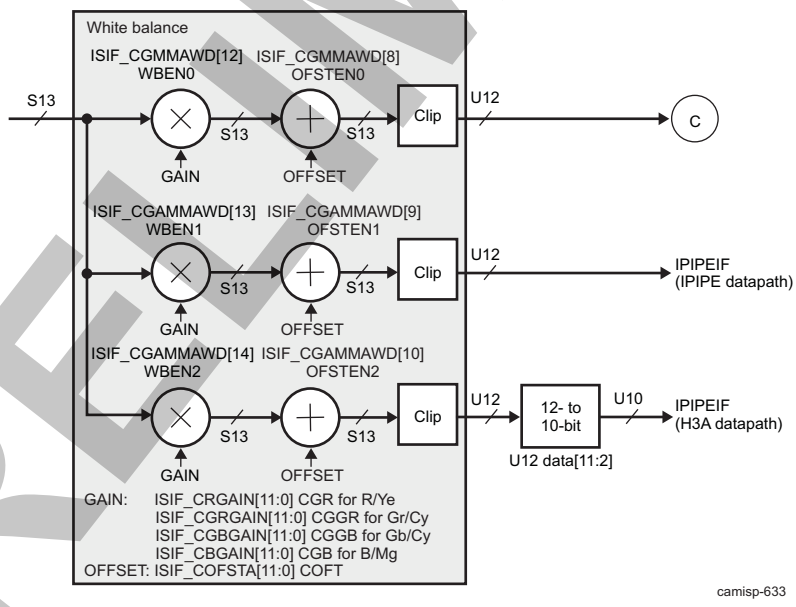
8.3.3.6.10.1.7 ISS ISP ISIF Bandwidth Requirements on BL Read Port

For details, see Section 8.3.3.6.18.2, *ISS ISP ISIF Read Port*.

8.3.3.6.11 ISS ISP ISIF White Balance

Figure 8-236 shows the white balance block diagram.

Figure 8-236. ISS ISP ISIF White Balance Block Diagram



Color pattern settings are set through the ISIF_CCOLP register. Moreover, through this register the pixel position from 0 to 3 can be set to the needed Bayer universal camera filter color pattern (RGB/CYGM).

The CFA pattern can be in two modes, stripe or mosaic, and is set through the ISIF_CGAMMAWD[5] CFAP bit.

There are color-dependent gain controls for the three outputs:

- BL output
- IPIPEIF (IPIPE path) output

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- IPIPEIF (H3A path) output

The gain applied to each data is selected according to the pixel position and the color pattern settings. Gain factors are common for the three data paths. Gain is in U11Q9 format, which ranges from 0 to 3 + 511/512. The gain factor is set through the following registers:

- R/Ye gain: ISIF_CRGAIN[11:0] CGR
- Gr/Cy gain: ISIF_CGRGAIN[11:0] CGGR
- Gb/Cy gain: ISIF_CGBGAIN[11:0] CGGB
- B/Mg gain: ISIF_CBGAIN[11:0] CGB

Gain control can be enabled or disabled individually for each path.

- Enable or disable gain for the BL path: ISIF_CGAMMAWD[12] WBEN0
- Enable or disable gain for the IPIPEIF (IPIPE) path: ISIF_CGAMMAWD[13] WBEN1
- Enable or disable gain for the IPIPEIF (H3A) path: ISIF_CGAMMAWD[14] WBEN2

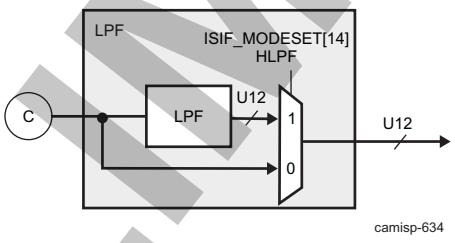
After the gain control, a single offset value can be added to each path individually. This offset is common for the three paths and is set through the ISIF_COFSTA[11:0] COFT bit field. The offset value is U12, which ranges from 0 to 4095. Data (S13) are then truncated to U12.

- Enable or disable offset for the BL path: ISIF_CGAMMAWD[8] OFSTEN0
- Enable or disable offset for the IPIPEIF (IPIPE) path: ISIF_CGAMMAWD[9] OFSTEN1
- Enable or disable offset for the IPIPEIF (H3A) path: ISIF_CGAMMAWD[10] OFSTEN2

8.3.3.6.12 ISS ISP ISIF Low-Pass Filter

Figure 8-237 shows the low-pass filter (LPF) block diagram.

Figure 8-237. ISS ISP ISIF Low-Pass Filter Block Diagram



An optional horizontal low-pass anti-aliasing filter (LPF) can be applied (the ISIF_MODESET[14] HLPF bit) after reframing. The LPF consists of a simple 3-tap (1/4, 1/2, and 1/4) filter. Two pixels on the left and two pixels on the right of each line are cropped if the filter is enabled. Use of the LPF is intended for bandwidth reduction if culling is enabled.

NOTE: For YUV data, the LPF must be disabled (ISIF_MODESET[14] HLPF = 0x0).

8.3.3.6.13 ISS ISP ISIF A-Law Compression

Figure 8-238 shows the A-Law compression block diagram.

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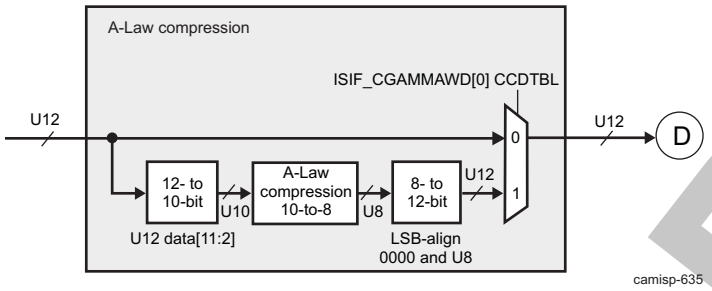
Figure 8-238. ISS ISP ISIF A-Law Compression Block Diagram



An optional 10-to-8-bit A-Law compression using a fixed A-Law table can be applied (the ISIF_CGAMMAWD[0] CCDTBL bit) as the final processing stage. Using this compression causes the data width to be reduced to 8 bits and allows packing to 8 bits/pixel when saving to memory. Because data resolution can be greater than 10 bits at this stage, the 10 bits for input to the A-Law operation must be selected (the ISIF_CGAMMAWD[4:1] GWDI bit field).

The IPIPEIF module has an inverse A-Law table (A-Law decompression) option so that this nonlinear operation can be reversed if this saved data is to be read back in for further processing.

NOTE: Do not use A-Law compression (ISIF_CGAMMAWD[0] CCDTBL = 0) with YUV data.

Figure 8-239 shows the A-Law table diagram, and Figure 8-240 shows the A-Law table values.

Figure 8-239. ISS ISP ISIF A-Law Table Diagram

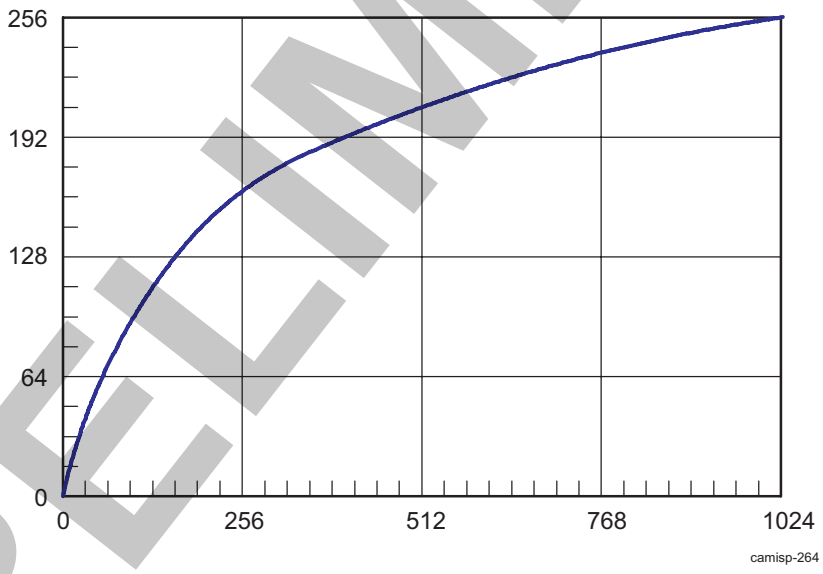


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Figure 8-240. ISS ISP ISIF A-Law Table Values

Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law
0	0	64	64	128	112	192	140	256	161	320	176	384	189	448	200
1	1	65	65	129	113	193	141	257	161	321	176	385	189	449	200
2	2	66	66	130	113	194	141	258	161	322	177	386	189	450	200
3	3	67	67	131	114	195	142	259	161	323	177	387	189	451	200
4	4	68	68	132	114	196	142	260	162	324	177	388	190	452	200
5	5	69	69	133	115	197	142	261	162	325	177	389	190	453	200
6	6	70	70	134	115	198	143	262	162	326	177	390	190	454	201
7	7	71	71	135	116	199	143	263	162	327	178	391	190	455	201
8	8	72	72	136	116	200	143	264	163	328	178	392	190	456	201
9	9	73	73	137	117	201	144	265	163	329	178	393	190	457	201
10	10	74	74	138	117	202	144	266	163	330	178	394	191	458	201
11	11	75	75	139	118	203	144	267	163	331	178	395	191	459	201
12	12	76	76	140	118	204	145	268	164	332	179	396	191	460	201
13	13	77	77	141	119	205	145	269	164	333	179	397	191	461	202
14	14	78	78	142	119	206	145	270	164	334	179	398	191	462	202
15	15	79	78	143	120	207	146	271	164	335	179	399	191	463	202
16	16	80	79	144	120	208	146	272	165	336	179	400	192	464	202
17	17	81	80	145	121	209	146	273	165	337	180	401	192	465	202
18	18	82	81	146	121	210	147	274	165	338	180	402	192	466	202
19	19	83	82	147	122	211	147	275	166	339	180	403	192	467	202
20	20	84	83	148	122	212	147	276	166	340	180	404	192	468	203
21	21	85	84	149	123	213	148	277	166	341	181	405	193	469	203
22	22	86	84	150	123	214	148	278	166	342	181	406	193	470	203
23	23	87	85	151	124	215	148	279	167	343	181	407	193	471	203
24	24	88	86	152	124	216	149	280	167	344	181	408	193	472	203
25	25	89	87	153	125	217	149	281	167	345	181	409	193	473	203
26	26	90	88	154	125	218	149	282	167	346	182	410	193	474	204
27	27	91	88	155	125	219	150	283	168	347	182	411	194	475	204
28	28	92	89	156	126	220	150	284	168	348	182	412	194	476	204
29	29	93	90	157	126	221	150	285	168	349	182	413	194	477	204
30	30	94	91	158	127	222	151	286	168	350	182	414	194	478	204
31	31	95	91	159	127	223	151	287	168	351	183	415	194	479	204
32	32	96	92	160	128	224	151	288	169	352	183	416	194	480	204
33	33	97	93	161	128	225	152	289	169	353	183	417	195	481	205
34	34	98	93	162	129	226	152	290	169	354	183	418	195	482	205
35	35	99	94	163	129	227	152	291	169	355	183	419	195	483	205
36	36	100	95	164	129	228	152	292	170	356	184	420	195	484	205
37	37	101	96	165	130	229	153	293	170	357	184	421	195	485	205
38	38	102	96	166	130	230	153	294	170	358	184	422	195	486	205
39	39	103	97	167	131	231	153	295	170	359	184	423	196	487	205
40	40	104	98	168	131	232	154	296	171	360	184	424	196	488	206
41	41	105	98	169	132	233	154	297	171	361	185	425	196	489	206
42	42	106	99	170	132	234	154	298	171	362	185	426	196	490	206
43	43	107	100	171	132	235	155	299	171	363	185	427	196	491	206
44	44	108	100	172	133	236	155	300	172	364	185	428	196	492	206
45	45	109	101	173	133	237	155	301	172	365	185	429	197	493	206
46	46	110	102	174	134	238	155	302	172	366	185	430	197	494	206
47	47	111	102	175	134	239	156	303	172	367	186	431	197	495	207
48	48	112	103	176	134	240	156	304	173	368	186	432	197	496	207
49	49	113	103	177	135	241	156	305	173	369	186	433	197	497	207
50	50	114	104	178	135	242	157	306	173	370	186	434	197	498	207
51	51	115	105	179	136	243	157	307	173	371	186	435	198	499	207
52	52	116	105	180	136	244	157	308	173	372	187	436	198	500	207
53	53	117	106	181	136	245	157	309	174	373	187	437	198	501	207
54	54	118	106	182	137	246	158	310	174	374	187	438	198	502	208
55	55	119	107	183	137	247	158	311	174	375	187	439	198	503	208
56	56	120	108	184	137	248	158	312	174	376	187	440	198	504	208
57	57	121	108	185	138	249	159	313	175	377	188	441	198	505	208
58	58	122	109	186	138	250	159	314	175	378	188	442	199	506	208
59	59	123	109	187	139	251	159	315	175	379	188	443	199	507	208
60	60	124	110	188	139	252	159	316	175	380	188	444	199	508	208
61	61	125	110	189	139	253	160	317	175	381	188	445	199	509	208
62	62	126	111	190	140	254	160	318	176	382	188	446	199	510	209
63	63	127	112	191	140	255	160	319	176	383	189	447	199	511	209

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Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law
512	209	576	217	640	224	704	231	768	237	832	243	896	248	960	253
513	209	577	217	641	225	705	231	769	237	833	243	897	248	961	253
514	209	578	217	642	225	706	231	770	237	834	243	898	248	962	253
515	209	579	217	643	225	707	231	771	237	835	243	899	248	963	253
516	209	580	218	644	225	708	232	772	238	836	243	900	248	964	253
517	210	581	218	645	225	709	232	773	238	837	243	901	248	965	253
518	210	582	218	646	225	710	232	774	238	838	243	902	248	966	253
519	210	583	218	647	225	711	232	775	238	839	243	903	249	967	253
520	210	584	218	648	225	712	232	776	238	840	243	904	249	968	253
521	210	585	218	649	225	713	232	777	238	841	244	905	249	969	253
522	210	586	218	650	226	714	232	778	238	842	244	906	249	970	254
523	210	587	218	651	226	715	232	779	238	843	244	907	249	971	254
524	211	588	219	652	226	716	232	780	238	844	244	908	249	972	254
525	211	589	219	653	226	717	232	781	238	845	244	909	249	973	254
526	211	590	219	654	226	718	233	782	238	846	244	910	249	974	254
527	211	591	219	655	226	719	233	783	239	847	244	911	249	975	254
528	211	592	219	656	226	720	233	784	239	848	244	912	249	976	254
529	211	593	219	657	226	721	233	785	239	849	244	913	249	977	254
530	211	594	219	658	226	722	233	786	239	850	244	914	249	978	254
531	211	595	219	659	227	723	233	787	239	851	244	915	249	979	254
532	212	596	220	660	227	724	233	788	239	852	244	916	250	980	254
533	212	597	220	661	227	725	233	789	239	853	245	917	250	981	254
534	212	598	220	662	227	726	233	790	239	854	245	918	250	982	254
535	212	599	220	663	227	727	233	791	239	855	245	919	250	983	254
536	212	600	220	664	227	728	233	792	239	856	245	920	250	984	255
537	212	601	220	665	227	729	234	793	239	857	245	921	250	985	255
538	212	602	220	666	227	730	234	794	240	858	245	922	250	986	255
539	212	603	220	667	227	731	234	795	240	859	245	923	250	987	255
540	213	604	220	668	227	732	234	796	240	860	245	924	250	988	255
541	213	605	221	669	228	733	234	797	240	861	245	925	250	989	255
542	213	606	221	670	228	734	234	798	240	862	245	926	250	990	255
543	213	607	221	671	228	735	234	799	240	863	245	927	250	991	255
544	213	608	221	672	228	736	234	800	240	864	245	928	250	992	255
545	213	609	221	673	228	737	234	801	240	865	246	929	250	993	255
546	213	610	221	674	228	738	234	802	240	866	246	930	251	994	255
547	214	611	221	675	228	739	235	803	240	867	246	931	251	995	255
548	214	612	221	676	228	740	235	804	240	868	246	932	251	996	255
549	214	613	221	677	228	741	235	805	240	869	246	933	251	997	255
550	214	614	222	678	229	742	235	806	241	870	246	934	251	998	255
551	214	615	222	679	229	743	235	807	241	871	246	935	251	999	255
552	214	616	222	680	229	744	235	808	241	872	246	936	251	1000	255
553	214	617	222	681	229	745	235	809	241	873	246	937	251	1001	255
554	214	618	222	682	229	746	235	810	241	874	246	938	251	1002	255
555	215	619	222	683	229	747	235	811	241	875	246	939	251	1003	255
556	215	620	222	684	229	748	235	812	241	876	246	940	251	1004	255
557	215	621	222	685	229	749	235	813	241	877	246	941	251	1005	255
558	215	622	222	686	229	750	236	814	241	878	247	942	251	1006	255
559	215	623	223	687	229	751	236	815	241	879	247	943	252	1007	255
560	215	624	223	688	230	752	236	816	241	880	247	944	252	1008	255
561	215	625	223	689	230	753	236	817	242	881	247	945	252	1009	255
562	215	626	223	690	230	754	236	818	242	882	247	946	252	1010	255
563	216	627	223	691	230	755	236	819	242	883	247	947	252	1011	255
564	216	628	223	692	230	756	236	820	242	884	247	948	252	1012	255
565	216	629	223	693	230	757	236	821	242	885	247	949	252	1013	255
566	216	630	223	694	230	758	236	822	242	886	247	950	252	1014	255
567	216	631	223	695	230	759	236	823	242	887	247	951	252	1015	255
568	216	632	224	696	230	760	236	824	242	888	247	952	252	1016	255
569	216	633	224	697	230	761	237	825	242	889	247	953	252	1017	255
570	216	634	224	698	231	762	237	826	242	890	247	954	252	1018	255
571	217	635	224	699	231	763	237	827	242	891	248	955	252	1019	255
572	217	636	224	700	231	764	237	828	242	892	248	956	252	1020	255
573	217	637	224	701	231	765	237	829	243	893	248	957	253	1021	255
574	217	638	224	702	231	766	237	830	243	894	248	958	253	1022	255
575	217	639	224	703	231	767	237	831	243	895	248	959	253	1023	255

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8.3.3.6.14 ISS ISP ISIF Culling

Figure 8-241 shows the culling block diagram.

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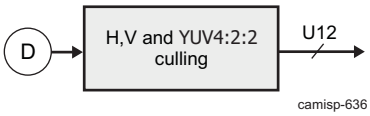
Figure 8-241. ISS ISP ISIF Culling Block Diagram



The culling block performs a programmable decimation function for horizontal, vertical, and YUV4:2:2 data directions. The horizontal and vertical decimation of image data can be controlled by two registers.

The horizontal culling operation allows selected pixel data to be culled (deleted) from a line. The ISIF_CULH register specifies the horizontal culling pattern for even and odd lines:

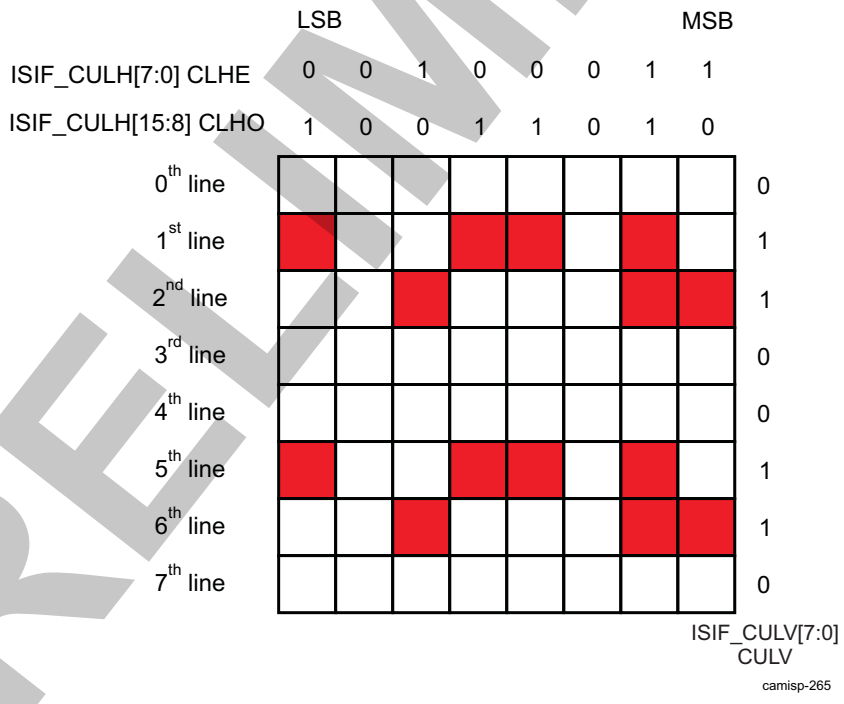
- Even lines: ISIF_CULH[15:8] CLHE
- Odd lines: ISIF_CULH[16:0] CLHO

The vertical culling operation allows selected lines to be culled from a frame. The ISIF_CULV register specifies the pattern for the vertical direction. The LSBs of CULV represent the top line of the CCD; the MSB is the seventh line.

Figure 8-242 is an example of how register values apply the decimation pattern to the data. The red pixels are saved to memory and the white pixels are discarded. In this example, CULH = 0x59C4 and CULV = 0x0066.

NOTE: Culling can be used with YUV data, but care must be taken to preserve the YUV4:2:2 output format.

Figure 8-242. ISS ISP ISIF Example for Decimation Pattern



8.3.3.6.15 ISS ISP ISIF 12-to-8-Bit DPCM Compression Block

In the ISIF, a DPCM compression block is between the culling module and the storage formatter module. This block can compress 12-bit image data to 8 bits for bandwidth reduction in transmission between the ISIF and SDRAM. An 8-to-12-bit DPCM decoder at the IPIPEIF decompresses data for IPIPE processing.

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Two different predictors are used for the compression system. The first predictor is simple (simple predictor), and the second predictor is slightly more complex (advanced predictor). Because the advanced predictor gives a slightly better prediction for the pixel value, the image quality can be improved using it. Because the simple predictor is very basic, the processing power and memory requirements are reduced using it, when the image quality is already sufficiently high.

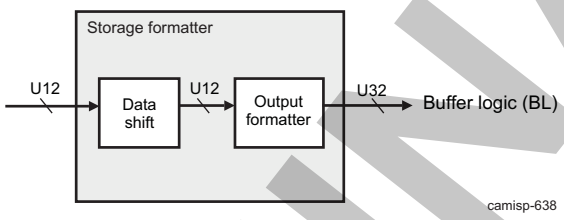
- Advanced predictor: This predictor uses only the previous same color component value as a prediction value. Therefore, only 2-pixel memory is required.
- This predictor uses four previous pixel values when the prediction value is evaluated. This means that the other color component values are also used when the prediction value is defined.

The function is controlled from the ISIF_MISC[12] DPCMEN and ISIF_MISC[13] DPCMPRE bits.

8.3.3.6.16 ISP ISIF Storage Formatter

Figure 8-243 shows the storage formatter block diagram.

Figure 8-243. ISS ISP ISIF Storage Formatter Block Diagram



Data are stored to the lower bits of a 16-bit SDRAM word, or can be 8- or 12-bit packed. The ISIF_HSIZE[11:0] HSIZE bit field can specify the memory address offsets between lines of memory (offset in 32-byte units). If set, the ISIF_HSIZE[12] ADCR bit can decrement the memory address line and the line can be horizontally flipped in memory.

In case of RAW data, a data shift module is used: data to be stored can be right-shifted according to the value set at the ISIF_MODESET[10:8] CCDW bit field, as described in Table 8-455.

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Table 8-455. ISS ISP ISIF RAW Data Shifting

ISIF_MODESET[10:8] CCDW	Output Format	
	MSB	LSB
000	0000 &U12 data[11:0]	
001	00000 &U12 data[11:1]	
010	000000 &U12 data[11:2]	
011	0000000 &U12 data[11:3]	
100	00000000 &U12 data[11:4]	

Table 8-456 shows the format where data are stored to the lower bits of a 16-bit word and the format where data are packed to 8 bits. The unused bits are filled with zeros.

Table 8-456. ISS ISP ISIF SDRAM Data Format

	Upper Word				Lower Word			
	MSB(31)			LSB(16)	MSB(15)			LSB(0)
12 bit	0	Pixel 1			0	Pixel 0		
11 bit	0	Pixel 1			0	Pixel 0		
10 bit	0	Pixel 1			0	Pixel 0		
9 bit	0	Pixel 1			0	Pixel 0		
8 bit	0	Pixel 1			0	Pixel 0		
8-bit packed	Pixel 3	Pixel 2			Pixel 1	Pixel 0		

Table 8-457 shows the format where data are packed to 12 bits.

Table 8-457. ISS ISP ISIF SDRAM Data Format for 12-bit Packed

	Upper Word				Lower Word			
	MSB(31)			LSB(16)	MSB(15)			LSB(0)
12 bit	Pixel2[7:0]	Pixel1			Pixel 0			
	Pixel5[3:0]	Pixel4			Pixel3			Pixel2[11:8]
	Pixel7		Pixel6			Pixel5[11:4]		

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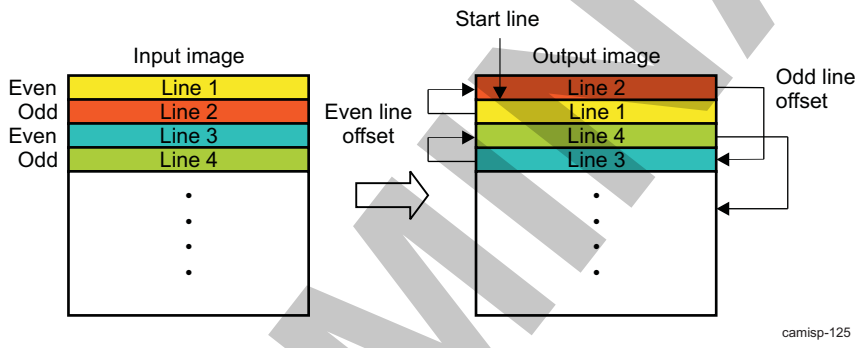
In case of YUV, YUV data is stored in memory in packed YUV4:2:2 mode, using 2 pixels per 32 bits, as shown in Table 8-458.

The output formatter can configure to any image format by using the SDRAM line offset register and offset control registers. Figure 8-244 shows how to construct a frame format in SDRAM. The ISIF_CADU[10:0] CADU bit field specifies the memory destination (upper 11 bits) to SDRAM (the address is the value of the set bit multiplied by 32 bytes). On the other hand, the ISIF_CADL[15:0] CADL bit field sets the memory destination to SDRAM (lower 16 bits) (the address is the value of the set bit multiplied by 32 bytes).

- ISIF_SPH defines the first pixel in a line to be stored to memory.
- ISIF_LNH defines the number of pixels in an line to be stored to memory.
- ISIF_LNV defines the number of lines to be stored to memory.
- ISIF_SLV0 sets line at which data output to SDRAM will begin.
- ISIF_SLV1 sets line at which data output to SDRAM will begin, measured from the start of VD.
- ISIF_SDOFST, ISIF_MODESET[15] MDFS, and ISIF_MODESET[4] FIPOL sets the setting for line FID polarity and the offset of even/odd lines in SDRAM.

Figure 8-244. ISS ISP ISIF Frame Image Format Conversion



8.3.3.6.17 ISS ISP ISIF YCbCr Signal Processing

The ISIF accepts 4:2:2 sampled YCbCr input data. The Luma and color difference signals are 8 bits each, scaled 0 to 255. The color difference signals are multiplexed into one 8-bit bus beginning with a Cb sample. The Y and CbCr buses can be input parallel (16-bit mode) or time-multiplexed and input as a single bus (8-bit mode).

The 16- or 8-bit YCbCr data is stored in SDRAM as 4:2:2 format. Table 8-458 lists the data format in SDRAM. Y data typically has a range of 16 to 235; however, it is possible to subtract a DC value from the Y signal.

Table 8-458. ISS ISP ISIF Memory Output Format for YUV Data

Memory Address	Upper Word		Lower Word	
	MSB(31)	LSB(16)	MSB(15)	LSB(0)
N	Y1	Cr0	Y0	Cb0
N + 1	Y3	Cr1	Y2	Cb1
N + 2	Y5	Cr2	Y4	Cb2

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8.3.3.6.18 ISS ISP ISIF Expected Bandwidth on BL Ports

The ISIF has a write port and a read port connected to the BL. This section summarizes the expected bandwidth on these ports.

8.3.3.6.18.1 ISS ISP ISIF Write Port

The write port is used to write pixels to memory after the data have passed through the storage formatter. Data storage to SDRAM is controlled by the ISIF_SYNCEN[1] DWEN bit. The ISIF allows writing the data as 16, 12, and 8 bpp. The bit width is controlled by the ISIF_CCDCFG[1:0] SDRPACK bit field.

The write port generates a burst of 32 bytes on the MTC interface. The delay between consecutive bursts is proportional to the input pixel clock. Hence, the write port does not request peak bandwidth traffic.

Table 8-459 lists the estimated delay between 32-byte MTC requests for different pixel clock frequencies and assumes the L3_MAIN clock is 200 MHz.

Table 8-459. ISP ISIF ISIF Module: Write Port Bandwidth

Pixel Clock	Maximum Bandwidth 2 Bytes/s Pixel MB/s	Expected Delay Between MTC Requests
200	400	16 cycles = 80 ns
100	200	32 cycles = 160 ns
10	20	320 cycles = 1600 ns

8.3.3.6.18.2 ISS ISP ISIF Read Port

The read port is used to read gain and offset data from SDRAM required for the LSC computation. When LSC is enabled, 8-bit gain values are read and 8-bit offset values can optionally also be read. The LSC gain computation can be enabled or disabled by setting the ISIF_2DLSCCFG[0] ENABLE bit. The LSC offset computation can be enabled by setting the ISIF_2DLSCOFST[0] OFSTEN bit.

LSC fetches four 8-bit gain values per paxel and optionally four 8-bit offset values per paxel. This is a maximum 8 bytes per paxel.

The bandwidth that is generated by the LSC module is also proportional to the paxel size. The paxel size is set up by the ISIF_2DLSCCFG[14:12] GAIN_MODE_M and ISIF_2DLSCCFG[10:8] GAIN_MODE_N bit fields. The possible values are 8, 16, 32, 64, and 128. Smaller values lead to higher memory bandwidth requirements. Hence, the worst case is achieved by setting an 8 × 8 paxel size.

When LSC is enabled it automatically prefetches two lines of gain values and two lines of offset values (if this is enabled). When the first VD comes, it again requests one line of gain values and one line of offset values (if this is enabled). Then, it again fetches one line of gain values and one line of offset values (if this is enabled) after ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines. It continues to do so until the last row of paxels. For the last row of paxels, it fetch two lines of gain values and two lines of offset values (if this is enabled), which are used for the following frame.

By default, LSC creates peak bandwidth requirements. To avoid this, the MTC bandwidth limiter must be used to space the request over time.

The MTC bandwidth limiter must be used to smooth the bandwidth requirements of the LSC module. The MTC bandwidth limiter can be set with the ISP5_BL_MTC_1.ISIF_R register.

The principle is that instead of reading the gain and offset data as fast as possible, use the time that it takes for ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines to pass through the ISP to read the data.

Table 8-460 gives the estimated delay between 32-byte MTC requests for different pixel clock frequencies and assumes the L3_MAIN clock at 200 MHz.

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Table 8-460. ISS ISP ISIF Read Port Bandwidth

Pixel Clock	Max Bandwidth MB/s	Expected Delay Between MTC Requests
200	25.07	255 cycles = 1275 ns
100	12.5	510 cycles = 2550 ns
10	1.25	5103 cycles = 2515 ns

When the bandwidth limiter is used, ensure that there is enough time for the data prefetching.

- LSC must be enabled at least 2 × ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines before the first VD.
- There must be at least ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines of blanking. If there is not enough blanking, multiply the bandwidth requirement by 2 (that is, ensure two lines of gain and offset data can be fetched within the time of ISIF_2DLSCCFG[10:8] GAIN_MODE_N lines.

8.3.3.6.19 ISS ISP ISIF Events and Status Checking

The ISIF module can generate four different interrupts: VDINT0, VDINT1, VDINT2, and 2DLSCINT. The ISIF_SYNCEN[0] SYEN bit must be enabled to receive any of the ISIF interrupts.

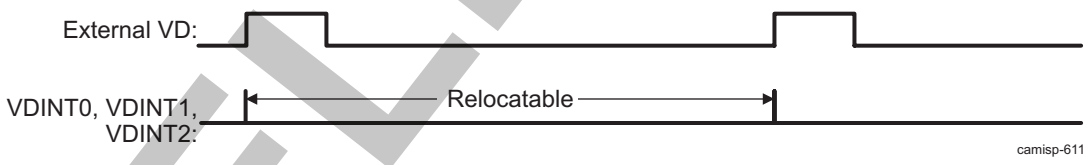
8.3.3.6.19.1 ISS ISP ISIF VDINT0, VDINT1, and VDINT2 Interrupts

As shown in Figure 8-245, the VDINT0, VDINT1, and VDINT2 interrupts occur relative to the VD pulse. The trigger timing is selected by using the ISIF_MODESET[2] VDPOL bit setting. VDINT0, VDINT1, and VDINT2 occur after receiving the number of horizontal lines (HD pulse signals) set in the ISIF_VDINT0[14:0] CDV0, ISIF_VDINT1[14:0] CDV1, and ISIF_VDINT2[14:0] CDV2 register fields, respectively.

NOTE: In the case of BT.656 input mode, there is a VD at the beginning of each field. Therefore, there are two interrupts for each frame (that is, one for each field).

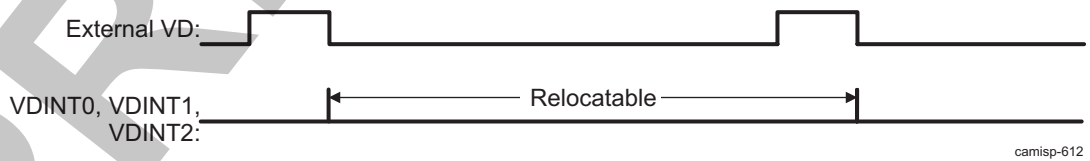
If the ISIF_MODESET[2] VDPOL bit is set to 0, the VDINT0, VDINT1, and VDINT2 HD counters begin counting HD pulses from the rising edge of the external VD.

Figure 8-245. ISS ISP ISIF VDINT0/VDINT1/VDINT2 Interrupt Behavior When VDPOL = 0



If the ISIF_MODESET[2] VDPOL bit is set to 1, the VDINT0, VDINT1, and VDINT2 HD counters begin counting HD pulses from the falling edge of the external VD.

Figure 8-246. ISS ISP ISIF VDINT0/VDINT1/VDINT2 Interrupt Behavior When VDPOL = 1



8.3.3.6.19.2 ISS ISP ISIF 2DLSCINT Interrupt

For more information, see Section 8.3.3.6.10.1.5, *ISS ISP ISIF 2D-LSC Events and Status Checking*.

8.3.3.6.19.3 ISS ISP ISIF Status Checking

The ISIF_MODESET[15] MDFS bit is set when the field status is on an even field, and it is cleared when the field status is on an odd field.

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The 2D-LSC has a register that monitors the status of the LSC. For more information, see Section 8.3.3.6.10.1.5, ISS ISP ISIF 2D-LSC Events and Status Checking.

8.3.3.7 ISS ISP BL Functional Description

8.3.3.7.1 ISS ISP BL Overview

The BL module arbitrates and merges the memory requests of the ISP master module. The BL module also generates interrupts upon frame completion for the following modules. The interrupt generation is delayed until the transfer completes (acknowledge signal is returned). The following interrupts are delayed by the BL module:

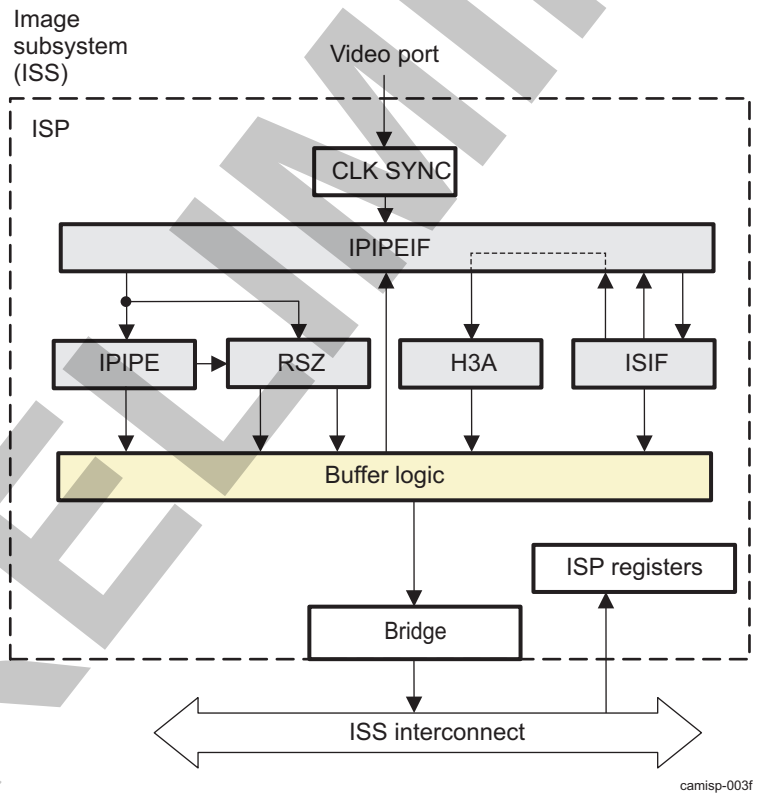
- RSZ module resizer RSZ-A EOF
- RSZ module resizer RSZ-B EOF
- H3A module EOF
- IPIPE module EOF

The BL uses two different types of interfaces:

- MTC protocol is used between the ISP modules and the BL.
- VBUSM is use on the BL master port interface.

Figure 8-247 show the BL module connections to other submodules of the ISP.

Figure 8-247. ISS ISP BL High-Level Diagram



8.3.3.7.2 ISS ISP BL Functional Description

The BL merges the memory requests of the ISP master module to memory (read/write). The BL interfaces with all the ISP modules through a 32-bit-wide bus.

The ISP modules make memory requests of 32 bytes. Additional signals, SOF for read and EOF for write, are included to deal with boundary conditions in frame transitions.

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The BL arbitration is divided into two parts: a bus hog and a fixed priority arbitration. Bus hog refers to the property of the buffer logic that gives higher priority to the module that last sent or received data. RSZ module MTC write port 0 and RSZ module MTC write port 1 are excluded from the bus hog.

The buffer logic is to be programmed to maximize the memory bandwidth: it makes maximum burst requests of 128 bytes (8 × 128 bits) for reads and writes. The BL can generate burst sizes of 2 × 128, 4 × 128, 6 × 128, and 8 × 128 bits.

NOTE: The ISP interface supports burst sizes of only 1, 2, 4, and 8 × 128 bits. If the BL generates a 6 × 128-bit request, it is divided into a 4 × 128-bit request, followed by a 2 × 128-bit request.

To use the memory bandwidth efficiently, the BL interfaces with the memory through a high-bandwidth bus (128 bits wide).

The BL handles memory requests for the following modules:

- IPIPEIF module read port
- ISIF-LSC module read port
- ISIF module write port
- IPIPE-BOXCAR module write port
- H3A module write port
- RSZ module write port 0
- RSZ module write port 1

From a use case point of view, the following sharing and priority arrangement is used. All reads have higher priority than writes; for reads: IPIPEIF > ISIF-LSC, and for writes: ISIF > IPIPE-BOXCAR > RSZ 0 > RSZ 1 > H3A.

NOTE: The BL can generate a static or a dynamic MFlag signal. The MFlag signal is used by the ISS arbitration to consider the urgency of the requests coming from the ISP. The dynamic MFlag feature is enabled from the ISP5_CTRL[21] MFLAG bit.

Figure 8-248 shows the BL top-level block diagram. The figure highlights the two clock domains that are used.

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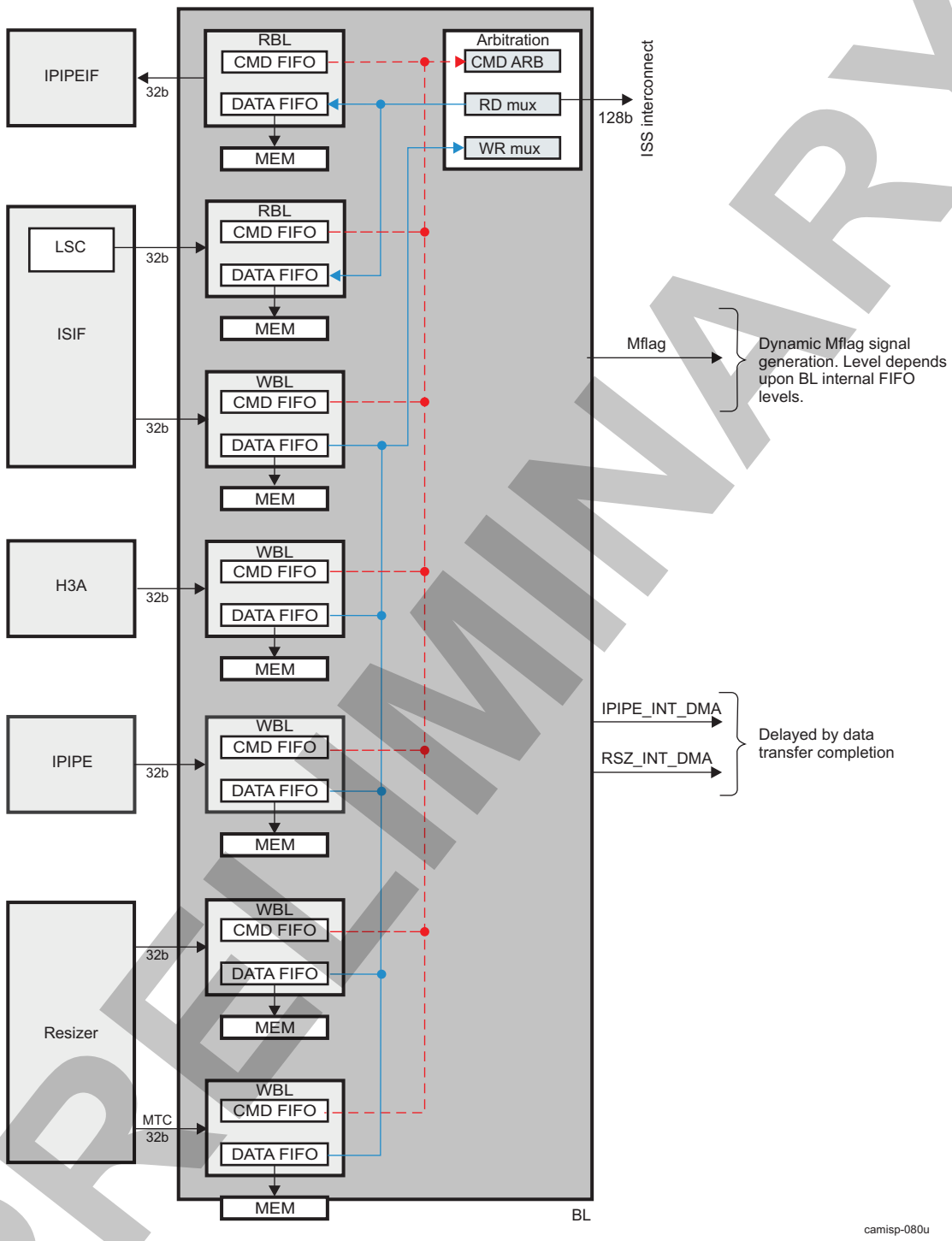
Figure 8-248. ISS ISP BL Block Diagram



NOTE: The BL module has no registers. The configurations come from the top level of the ISP. See Table 8-501 for register details.

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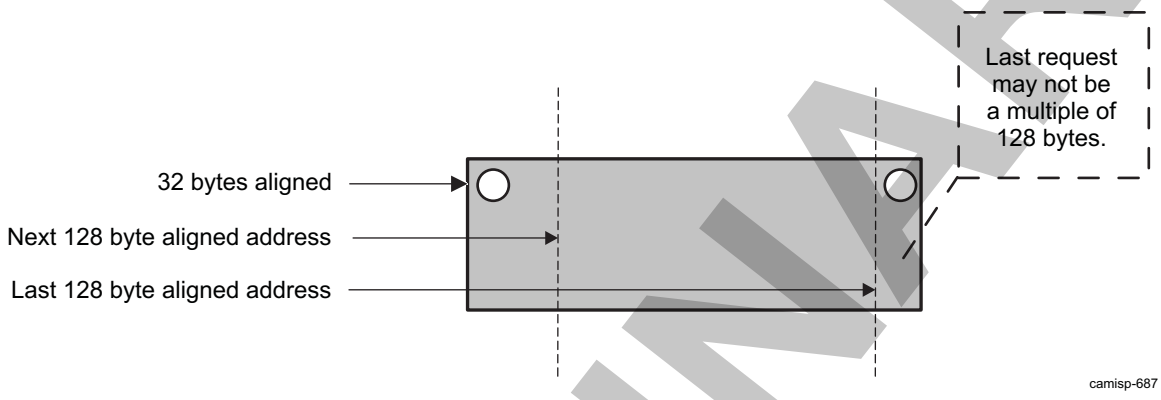
8.3.3.7.3 ISS ISP BL Address Alignment

The BL module ensures maximum memory efficiency by realigning data to a 128-byte address boundary. In all cases, the BL accesses are 32-byte-aligned: address [4:0] is always 0.

This is required when the input address is a multiple of 32 bytes, not 128 bytes. The BL issues a nonaligned burst until it reaches a 128-byte boundary, and then keeps making a 128-byte request until the end of the line. Eventually, although the last burst in a line may not be a multiple of 128 bytes, it will always be a multiple of 32 bytes, as shown in Figure 8-249.

Figure 8-249. ISS ISP BL Address Alignment



8.3.3.7.4 ISS ISP BL Out-of-Order Responses

BL supports out-of-order responses. The out-of-order response is handled by having up to 16 outstanding CIDs (reads and writes). The maximum number of outstanding CIDs is set up by the ISP5_CTRL[7:4] VBUSM_CIDS bit field. There is one outstanding request per CID.

If any of the CIDs are not outstanding, a command is accepted from the highest prioritized buffer with a request. The CID availability is cleared when status complete is received. The outstanding commands can be all reads or all writes or any combination. The CID that is allocated is the lowest number of the 16 that are available when the command is accepted. As soon as a CID is released it is used if a command is available.

The VBUSM2OCP module transforms the VBUMS CIDs into OCP MFlag signals. There can be only one outstanding CID per tag. It is not authorized to make a new request on a tag which is already waiting for a response.

8.3.3.7.5 ISS ISP BL Stalling

The BL can stall the requests from the initiator modules for reads and writes

8.3.3.7.5.1 ISS ISP BL Stalling Write Requests

One reason for the BL to stall write requests is that because back pressure usually exists on the system memory and requests cannot be issued as fast as required. In that case the BL must stall requests from the initiator modules. The BL module cannot know whether stalling the request will lead to an initiator overflow or not. The RSZ module can support back pressure from the BL module when it is configured in bypass mode. The input buffer memory can be used to store data from the IPIPE and IPIPEIF modules. If the RSZ input buffer overflows, an interrupt is issued.

8.3.3.7.5.2 ISS ISP BL Stalling Read Requests

The BL may also stall read requests from the ISIF-LSC and IPIPEIF modules. When data comes from an image sensor, there is no way to stop the sensor. If the read request is stalled too long, the LSC module may eventually underflow. When the IPIPEIF reads all its data from memory, the IPIPEIF stalls transfers to successive modules by masking the clock.

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8.3.3.7.6 ISS ISP BL Dynamic and Static MFlag Generation

NOTE: The following applies when ISP5_CTRL[21] MFLAG = 1. The MFlag value is static.

The BL outputs cpriority[2:0] and cepriority[2:0] signals on its VBUS master port interface. On the VBUSM side, these signals are aligned with the request (creq). Both values actually repeat register input signals. The lower value (0) corresponds to the higher priority.

The MFlag signal does not need to be aligned with the request. The signal can change value anytime.

In the ISP VBUSM2 interface bridge, the cepriority signal is ignored and only the cpriority signal is used. Because the priority value is set up by a register setting, the value is not dynamically modified. Table 8-461 shows how the cpriority values are mapped to the interface MFlag signal, which is present on the ISP master interface and set in the ISP5_CTRL[3:1] VBUSM_CPRIORITY bit field.

Table 8-461. ISS ISP BL cpriority to MFlag With ISP5_CTRL[21] MFLAG = 1

MFlag[1:0]	Description
00	Normal priority cpriority[2:0] = 4, 5, 6, 7
01	Medium priority cpriority[2:0] = 2, 3
10	Reserved
11	High priority cpriority[2:0] = 0, 1

NOTE: The following applies when the ISP5_CTRL[21] MFLAG = 0. The MFlag value is dynamic.

This feature is enabled at reset. The purpose for dynamic MFlag generation is to monitor the FIFO levels. Thresholds are used to increase or decrease the MFlag values. There are different implementations for read and write requestors.

An individual MFlag value is generated for each FIFO and then ORed altogether and exported at the BL boundary. The MFlag signal generation does not affect the BL arbitration scheme.

- Writes: To prevent overflows in the BL, dynamic MFlag signal generation gives higher priority to FIFOs that are almost full:
  - Low FIFO level = 50 percent
  - High FIFO level = 75 percent
  - FIFOs with more than 75 percent fill level have high priority: MFlag = 11
  - FIFOs between 50 and 75 percent fill level have medium priority: MFlag = 01
  - FIFOs below 50 percent fill level have low priority: MFlag = 00

Table 8-462 gives the low- and high-level priority thresholds for write initiators.

Table 8-462. ISS ISP BL MFlag Write Low- and High-Level Priority Thresholds

	ISIF	H3A	IPIPE	RSZ
Access type	Write	Write	Write	Write
Buffer size	64 × 128	64 × 128	48 × 128	64 × 136
50% low level	32 × 128	32 × 128	24 × 128	32 × 136
75% high level	48 × 128	48 × 128	36 × 128	48 × 128

- Reads: The dynamic MFlag signal generation depends on the reserved data units in the initiator data FIFO. The reserved data units correspond to read commands waiting to be sent on the interface bus, plus the read commands that have been sent on the interface bus and for which data responses have not yet arrived.
- The total FIFO size in bytes can be expressed as reserved data units (bytes) + data bytes stored (bytes) + empty space (bytes). By definition, empty space is lower than a burst size (128 bytes).
  - Low FIFO level = 25 percent

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- High FIFO level = 50 percent
- Data bytes stored + empty space (bytes) = 50 percent of FIFO size: MFlag = 00
- Data bytes stored + empty space (bytes) = 50 percent of FIFO size: MFlag = 01
- Data bytes stored + empty space (bytes) = 25 percent of FIFO size: MFlag = 11

Table 8-463 gives the low- and high-level priority thresholds for read initiators

Table 8-463. ISS ISP BL MFlag Read Low- and High-Level Priority Thresholds

	IPIPEIF	ISIF-LSC
Access type	Read	Read
Buffer size	64 × 128	32 × 128
25% buffer size	16 × 128	8 × 128
50% buffer size	32 × 128	16 × 128

8.3.3.7.7 ISS ISP BL VBUSM2OCP Last Beat Command Delay

The VBUSM2OCP module bridge implements the following function to work around a limitation of the BL module, which does not send back-to-back requests to the ISS, thereby leading to possible situations where the ISP loses arbitration at the ISS level.

To fully benefit from dynamic MFlag generation (see Section 8.3.3.7.6, *ISS ISP BL Dynamic and Static MFlag Generation*), the following function is present in the VBUSM2OCP module bridge:

- The delay occurs only if BL MFflag = ISP5_BL_VBUSM[5] MFLAG_THRES.
- The MFlag value used is whatever is available when the last beat comes on the interface bus.
- The last beat of the interface request (read or write) is held until one cycle before a new command (read or write). This is achieved by masking the last beat of the interface command at the ISP interface.

  The last beat is unmasked on the first event of one cycle before a new interface command, or the delay counter that uses the value counter of the ISP5_BL_VBUSM[4:0] LASTCMD_DLY bit field expires (has decremented to 0). The ISP5_BL_VBUSM[4:0] LASTCMD_DLY bit field must be set before the request on the BL starts. If the value of the ISP5_BL_VBUSM[4:0] LASTCMD_DLY bit field is changed during the pending requests, the delay counter is not updated.

8.3.3.7.8 ISS ISP BL Peak Memory Bandwidth Reduction

To limit the peak memory bandwidth generated by the IPIPEIF (read port), ISIF (read port), and H3A (write port) modules, a bandwidth limiter is placed between the modules and the BL. The RSZ module has this function built in and therefore does not need a bandwidth limiter.

The bandwidth limiter enables control of the minimum interval between two consecutive memory requests.

This function is controlled by the ISP5_BL_MTC_1 and ISP5_BL_MTC_2 registers. When the registers are set to 0, the function is not modified (that is, the bandwidth limiter is disabled). For the RSZ module, it is controlled by the RSZ_DMA_RZA and RSZ_DMA_RZB registers.

8.3.3.8 ISS ISP Memory Mapping

A total of 64 KiB is reserved for the ISP registers and memories. Table 8-464 describes the memory map.

Table 8-464. ISS ISP Memory Mapping

Memory Mapping	Start	End	Size	Comments
ISS ISP5 SYS1	0x5201 0000	0x5201 009F	160	ISP5 configuration registers (set 1)
ISS ISP5 SYS2	0x5201 00A0	0x5201 03FF	864	ISP5 configuration registers (set 2)
ISS RESIZER registers	0x5201 0400	0x5201 07FF	1024	RSZ configuration registers

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Table 8-464. ISS ISP Memory Mapping (continued)

Memory Mapping	Start	End	Size	Comments
ISS IPIPE registers	0x5201 0800	0x5201 0FFF	2048	IPIPE configuration registers
ISS ISIF registers	0x52011000	0x5201 11FF	512	ISIF configuration registers
ISS IPIPEIF registers	0x5201 1200	0x5201 13FF	512	IPIPEIF configuration registers
ISS H3A registers	0x5201 1400	0x5201 15FF	512	H3A configuration registers
Reserved	0x5201 1600	0x5201 17FF	512	Reserved
Reserved	0x5201 1800	0x5201 1BFF	1024	Reserved
Reserved	0x5201 1C00	0x5201 1DFF	512	Reserved
Reserved	0x5201 1E00	0x5201 1FFF	512	Reserved
HST memory 0	0x5201 2000	0x5201 27FF	2048	IPIPE histogram
HST memory 1	0x5201 2800	0x5201 2FFF	2048	IPIPE histogram
HST memory 2	0x5201 3000	0x5201 37FF	2048	IPIPE histogram
HST memory 3	0x5201 3800	0x5201 3FFF	2048	IPIPE histogram
Reserved	0x5201 4000	0x5201 6EFF	16384	Reserved
DPC table 0	0x5201 8000	0x5201 81FF	1024	IPIPE defect (fault) pixel correction address table
DPC table 1	0x5201 8400	0x5201 85FF	1024	IPIPE defect (fault) pixel correction address table
YEE table	0x5201 8800	0x5201 8FFF	2048	IPIPE Y-data edge enhance table
Reserved	0x5201 9000	0x5201 A6FF	6144	Reserved
GAMR table	0x5201 A800	0x5201 AFFF	2048	IPIPE gamma correction table (R)
GAMG table	0x5201 B000	0x5201 B7FF	2048	IPIPE gamma correction table (G)
GAMB table	0x5201 B800	0x5201 BFFF	2048	IPIPE gamma correction table (B)
LIN table 0	0x5201 C000	0x5201 C17F	1024	ISIF linearization table
LIN table 1	0x5201 C400	0x5201 C57F	1024	ISIF linearization table
DCCLAMP	0x5201 C800	0x5201 C9FF	2048	ISIF digital clamp
LSC table 0	0x5201 D000	0x5201 E7FF	6144	ISIF lens shading gain table
LSC table 1	0x5201 E800	0x5201 FFFF	6144	ISIF lens shading gain table

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8.3.4 ISS ISP Programming Model

NOTE: The preferred way to perform memory-to-memory processing with ISP is to use the CCP2 receiver module at the ISS level (see Section 8.2.1, *ISS Interfaces*). It is possible to use the IPIPEIF read port for memory-to-memory processing, but it is not the preferred way because it does not provide enough granularity on the fractional clock divider for up to 20x digital zoom.

8.3.4.1 ISS ISP ISIF Programming Model

This section discusses issues related to the software control of the ISIF. It lists the registers that must be programmed in different modes, describes how to enable and disable the ISIF and how to check the status of the ISIF, discusses the different register access types, and enumerates several programming constraints.

8.3.4.1.1 ISS ISP ISIF Hardware Setup/Initialization

This section discusses the configuration of the ISIF required before image processing can begin.

8.3.4.1.1.1 ISS ISP ISIF Reset Behavior

Upon hardware reset of the ISP, all of the registers in the ISIF, except the defect table registers, are reset to their reset values. Because the defect table registers are stored in internal RAM, they do not have reset values. If the reset is a chip-level POR (reset after power is applied), the values of the defect table register are unknown. If the reset is an ISP module reset (when power remains active), the contents of this memory remain the same as before the reset.

8.3.4.1.1.2 ISS ISP ISIF Register Setup

Before enabling the ISIF, the hardware must be properly configured through register writes. Figure 8-250 and Figure 8-251 show the sequence to be used for RAW and YUV data before enabling the ISIF. The register settings for each process in the following sequence are described in Table 8-465.

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Figure 8-250. ISS ISP ISIF Initialization Flow Chart – Part One

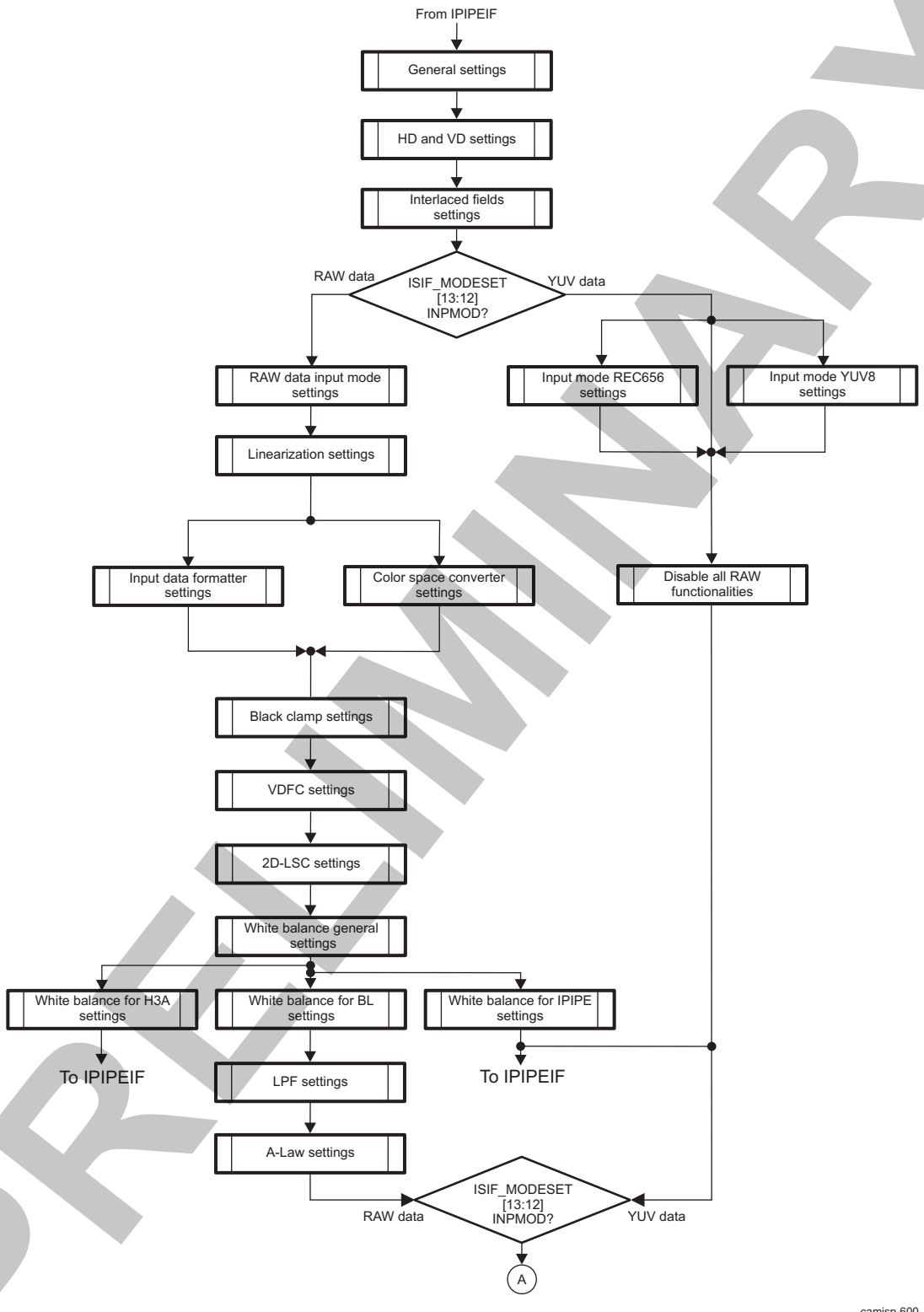

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Figure 8-251. ISS ISP ISIF Initialization Flow Chart – Part Two

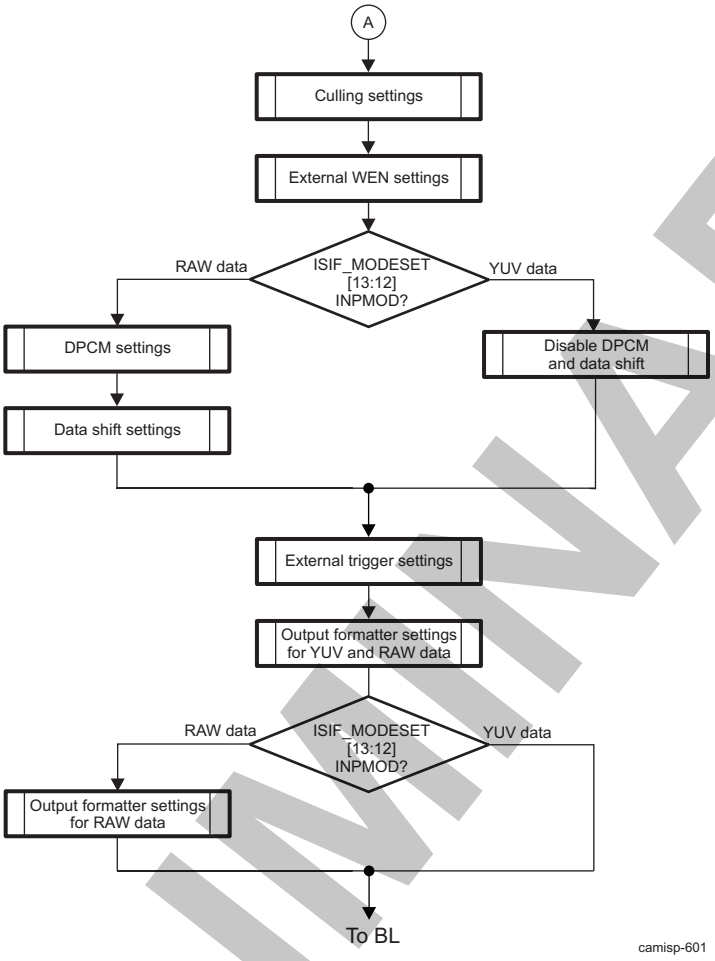

Table 8-465. ISS ISP ISIF Required Configuration Parameters

Step	Configuration Required	Value
General settings		
Set the Field Indicator signal direction.	ISIF_MODESET[1] FIDD	
Set the VD signal polarity.	ISIF_MODESET[2] VDPOL	
Set the HD signal polarity.	ISIF_MODESET[3] HDPOL	
Set the Field Indicator signal polarity.	ISIF_MODESET[4] FIPOL	
HD and VD settings		
Set the HD and VD signal directions.	ISIF_MODESET[0] HDVDD	
If: HD and VD are set as output (HDVDD = 0x1):		
Set the HD width.	ISIF_HDW[11:0] HDW	
Set the VD width.	ISIF_VDW[11:0] VDW	
Set the HD period.	ISIF_PPLN[15:0] PPLN	
Set the VD period.	ISIF_LPFR[15:0] LPFR	
End		
Interlaced fields settings		
Select the type of image sensor (progressive or interlaced)	ISIF_MODESET[7] CCDMD	
Input mode settings		
Set the data input mode.	ISIF_MODESET[13:12] INPMOD	

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Table 8-465. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Input mode settings for REC656 data		
Select CCIR Rec.656 interface or not.	ISIF_REC656IF[1] R656ON	
If: Input is REC656 (R656ON = 0x1)		
Set error correction of FVH code.	ISIF_REC656IF[0] ECCFVH	
Select bit width of CCIR656.	ISIF_CCDCFG[5] BT656	
End		
Input mode settings for YCC 8 bit data (if INPMOD = 0x2)		
Selects Y position signal	ISIF_CCDCFG[11] Y8POS	
RAW data processing: input settings		
Enable or disable MSB inverse of CIN port (YUV format).	ISIF_CCDCFG[13] MSBINVI	
Select Y and C swapping.	ISIF_CCDCFG[4] YCINSWP	
Select MSB position of input data (16 bits to 16 bits)	ISIF_CGAMMAWD[4:1] GWDI	
Set the image sensor data polarity.	ISIF_MODESET[6] DPOL	
Select the CFA pattern mode.	ISIF_CGAMMAWD[5] CFAP	
Specifies the color pattern	ISIF_CCOLP[7:6] CP0_F0	
	ISIF_CCOLP[5:4] CP1_F0	
	ISIF_CCOLP[3:2] CP2_F0	
	ISIF_CCOLP[1:0] CP3_F0	
Linearization settings		
Enable linearization or not.	ISIF_LINCFG0[0] LINEN	
If: Linearization enabled (LINEN = 0x1)		
Select linearization mode.	ISIF_LINCFG0[1] LINMD	
Select the shift value.	ISIF_LINCFG0[6:4] CORRSFT	
Set the scale factor for LUT.	ISIF_LINCFG1[10:0] LUTSCL	
Set up linearization LUT.		
End		
Input data formatter settings		
Enable data formatter or not.	ISIF_FMTCFG[0] FMTEN	
If: Data formatter is enabled (FMTEN = 0x1)		
Select the combine input lines.	ISIF_FMTCFG[1] FMTCBL	
Select the mode normal or alternative.	ISIF_FMTCFG[2] LNALT	
Select the split/combine number of lines.	ISIF_FMTCFG[5:4] LNUM	
Set the address increment.	ISIF_FMTCFG[11:8] FMTAINC	
Set the number of program entries per set.	ISIF_FMTPLEN[3:0] FMTPLEN0	
	ISIF_FMTPLEN[7:4] FMTPLEN1	
	ISIF_FMTPLEN[10:8] FMTPLEN2	
	ISIF_FMTPLEN[14:12] FMTPLEN3	
Set the first pixel in a line.	ISIF_FMTSPH[12:0] FMTSPH	
Set the number of pixels in a line.	ISIF_FMTLNH[12:0] FMTLNH	
Set the start line vertical.	ISIF_FMTLSV[12:0] FMTSLV	
Set the number of lines in a vertical.	ISIF_FMTLNV[14:0] FMTLNV	
Set the number of pixels in an output line.	ISIF_FMTRLEN[12:0] FMTRLEN	
Set the HD interval for output lines.	ISIF_FMTHCNT[12:0] FMTHCNT	
Set up to 16 address pointers.	ISIF_FMTAPTRx[14:13] LINE (x = 0 to 15)	
	ISIF_FMTAPTRx[12:0] INIT (x = 0 to 15)	

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Table 8-465. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Set the 32 possible program entry valid flag.	ISIF_FMTPGMVF0	
	ISIF_FMTPGMVF1	
Set the 32 possible address pointers.	ISIF_FMTPGMAPS0	
	ISIF_FMTPGMAPS1	
	ISIF_FMTPGMAPS2	
	ISIF_FMTPGMAPS3	
	ISIF_FMTPGMAPS4	
	ISIF_FMTPGMAPS5	
	ISIF_FMTPGMAPS6	
	ISIF_FMTPGMAPS7	
Set the 32 possible address update (increment or decrement).	ISIF_FMTPGMAPU0	
	ISIF_FMTPGMAPU1	E
End		
Color space converter settings		
Enable or disable color space converter.	ISIF_CSCCTL[0] CSCEN	
If: Color space converter is enabled (CSCEN = 0x1)		
Set the color space converter coefficients.	ISIF_CSCM0	
	ISIF_CSCM1	
	ISIF_CSCM2	
	ISIF_CSCM3	
	ISIF_CSCM4	
	ISIF_CSCM5	
	ISIF_CSCM6	
	ISIF_CSCM7	
End		
Black clamp settings		
Enable or disable black clamp.	ISIF_CLAMPCFG[0] CLEN	
If: Black clamp is enabled (CLEN = 0x1)		
Set the DC offset for black clamp.	ISIF_CLDCOFST[12:0] CLDC	
[Horizontal Black Clamp]		
Set the horizontal clamp mode.	ISIF_CLAMPCFG[2:1] CLHMD	
Set the vertical dimension of a window.	ISIF_CLHWIN0[13:12] CLHWN	
Set the horizontal dimension of a window.	ISIF_CLHWIN0[9:8] CLHWM	
Enable or disable limitation for horizontal.	ISIF_CLHWIN0[6] CLHLMT	
Select base window.	ISIF_CLHWIN0[5] CLHWBS	
Set the window count per color.	ISIF_CLHWIN0[4:0] CLHWC	
Set the window start position (H).	ISIF_CLHWIN1[12:0] CLHSH	
Set the window start position (V).	ISIF_CLHWIN2[12:0] CLHSV	
[Vertical Black Clamp]		
Set the black clamp start position.	ISIF_CLSV[12:0] CLSV	
Set the vertical black clamp reset value.	ISIF_CLVRV[11:0] CLVRV	
Set the line average coefficient.	ISIF_CLVWIN0[15:8] CLVCOEF	
Select the reset value for the clamp value of the previous line.	ISIF_CLVWIN0[5:4] CLVRVSL	
Select the optical black H valid.	ISIF_CLVWIN0[2:0] CLVOBH	
Set the window start position (H).	ISIF_CLVWIN1[12:0] CLVSH	
Set the window start position (V).	ISIF_CLVWIN2[12:0] CLVSV	
Select the optical black V valid.	ISIF_CLVWIN3[12:0] CLVOBV	

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Table 8-465. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
End		
Set the DC offset for black clamp (RAW data only).	ISIF_CLDCOFST[12:0] CLDC	DC offset available for YUV
Vertical line defect correction (VDFC) settings		
Disable vertical line defect correction.	ISIF_DFCCTL[4] VDFCEN	0x0
If: Vertical line defect correction will be enabled (VDFCEN = 0x1)		
Select the mode.	ISIF_DFCCTL[6:5] VDFCSL	
Select upper pixels correction enable or disable.	ISIF_DFCCTL[7] VDFCUDA	
Set the shift value.	ISIF_DFCCTL[10:8] VDFLSFT	
Set the saturation level.	ISIF_VDFSATLV[11:0] VDFSLV	
Clear memories.	ISIF_DFCMEMCTL[4] DFCMCLR	0x1
Vertical line defect table update procedure	See Section 8.3.3.6.9.1 for details.	
	Use the following registers:	
	ISIF_DFCMEMCTL[2] DFCMARST	
	ISIF_DFCMEMCTL[0] DFCMWR	
	ISIF_DFCMEM0	
	ISIF_DFCMEM1	
	ISIF_DFCMEM2	
	ISIF_DFCMEM3	
	ISIF_DFCMEM4	
End		
Enable vertical line defect correction.	ISIF_DFCCTL[4] VDFCEN	0x1
2D Lens Shading Compensation (LSC) settings		
Disable lens shading compensation.	ISIF_2DLSCCFG[0] ENABLE	0x0
If: 2D-LSC will be enabled (ENABLE = 0x1)		
Set the H direction data offset.	ISIF_LSCHOFST[13:0] HOFST	
Set the V direction data offset.	ISIF_LSCVOFST[13:0] VOFST	
Set the number of valid pixels in H direction.	ISIF_LSCHVAL[13:0] HVAL	
Set the number of valid lines in V direction.	ISIF_LSCVVAL[13:0] VVAL	
Define the horizontal dimension of a paxel.	ISIF_2DLSCCFG[14:12] GAIN_MODE_M	
Define the vertical dimension of a paxel.	ISIF_2DLSCCFG[10:8] GAIN_MODE_N	
Set gain format table.	ISIF_2DLSCCFG[4:1] GAIN_FORMAT	
Enable or disable offset control.	ISIF_2DLSCOFST[0] OFSTEN	
Select shift up value for offsets.	ISIF_2DLSCOFST[6:4] OFSTSFT	
Set scaling factor for offset.	ISIF_2DLSCOFST[15:8] OFSTSF	
Set the initial Y position.	ISIF_2DLSCINI[14:8] Y	
Set the initial X position.	ISIF_2DLSCINI[6:0] X	
Set the gain table base address.	ISIF_2DLSCGRBU[15:0] BASE31_16	
	ISIF_2DLSCGRBL[15:0] BASE15_0	
Set the gain table offset (length of one row).	ISIF_2DLSCGROF[15:0] OFFSET	
Set the offset table base address.	ISIF_2DLSCORBU[15:0] BASE	
	ISIF_2DLSCORBL[15:0] BASE	
Set the offset table offset (length of one row).	ISIF_2DLSCOROF	

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Table 8-465. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Enable useful interrupts.	ISIF_2DLSCIRQEN[3] SOF	
	ISIF_2DLSCIRQEN[2] PREFETCH_COMPLETED	
	ISIF_2DLSCIRQEN[1] PREFETCH_ERROR	
	ISIF_2DLSCIRQEN[0] DONE	
Set up LSC gain table and offset table in SDRAM. See Figure 8-237 for details.		
Wait seven clock periods before enabling LSC.		
Enable lens shading compensation.	ISIF_2DLSCCFG[0] ENABLE	0x1
End		
White balance color settings		
Set R/Ye gain.	ISIF_CRGAIN[11:0] CGR	
Set Gr/Cy gain.	ISIF_CGRGAIN[11:0] CGGR	
Set Gr/Cy gain.	ISIF_CGBGAIN[11:0] CGGB	
Set B/Mg gain.	ISIF_CBGAIN[11:0] CGB	
Set offset.	ISIF_COFSTA[11:0] COFT	
[For BL output]		
Enable or disable white balance for BL path.	ISIF_CGAMMAWD[12] WBNEN0	
Enable or disable offset control for BL path.	ISIF_CGAMMAWD[8] OFSTEN0	
[For IPIPE (through IPIPEIF) output]		
Enable or disable white balance for IPIPE path.	ISIF_CGAMMAWD[13] WBEN1	
Enable or disable offset control for IPIPE path.	ISIF_CGAMMAWD[9] OFSTEN1	
[For H3A (through IPIPEIF) output]		
Enable or disable white balance for H3A path.	ISIF_CGAMMAWD[14] WBEN2	
Enable or disable offset control for H3A path.	ISIF_CGAMMAWD[10] OFSTEN2	
LPF settings (for BL output only) (RAW data only)		
Enable or disable low-pass filter.	ISIF_MODESET[14] HLPF	
A-Law compression settings (for BL output only) (RAW data only)		
Enable or disable A-Law compression.	ISIF_CGAMMAWD[0] CCDTBL	
Culling settings (for BL output only) (RAW or YUV data)		
Set the culling pattern in odd lines.	ISIF_CULH[15:8] CLHO	
Set the culling pattern in even lines.	ISIF_CULH[7:0] CLHE	
Set the culling pattern in vertical lines.	ISIF_CULV[7:0] CULV	
External WEN settings (for BL output only)		
Select external WEN use or not.	ISIF_MODESET[5] SWEN	
If: External WEN is used (SWEN = 0x1):		
Specifies the CCD valid area	ISIF_CCDCFG[8] WENLOG	
End		
DPCM settings (for BL output only) (RAW data only)		
Select the predictor for DPCM encoder.	ISIF_MISC[13] DPCMPRE	

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Table 8-465. ISS ISP ISIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Enable or disable DPCM encoding.	ISIF_MISC[12] DPCMEN	
Data shift settings (for BL output only) (RAW data only)		
Select the data shift value when image is written to memory.	ISIF_MODESET[10:8] CCDW	
External trigger settings (for BL output only)		
If: External trigger is selected (EXTRG = 0x1):		
Select the trigger source signal.	ISIF_CCDCFG[9] TRGSEL	
End		
Output formatter (for BL output only) RAW and YUV		
Set the memory address decrement.	ISIF_HSIZE[12] ADCR	
Set the memory address offset between lines.	ISIF_HSIZE[11:0] HSIZE	
Set the first pixel in a line to be stored in memory.	ISIF_SPH[14:0] SPH	
Set the number of pixels in a line to be stored in memory.	ISIF_LNH[14:0] LNH	
Set the start line vertical for field 0.	ISIF_SLV0[14:0] SLV0	
Set the start line vertical for field 1.	ISIF_SLV1[14:0] SLV1	
Set the number of lines to be stored in memory.	ISIF_LNV[14:0] LNV	
Enable or disable the storage of image in memory.	ISIF_SYNCEN[1] DWEN	
Set the memory destination address.	ISIF_CADU[10:0] CADU	
	ISIF_CADL[10:0] CADL	
Enable or disable MSB inverse of COUT port.	ISIF_CCDCFG[14] MSBINVO	
Enable or disable byte swap when SDRAM capturing.	ISIF_CCDCFG[12] BSWD	
Select Y and C swapping.	ISIF_CCDCFG[2] YCOUNTSWP	
Select SDRAM pack mode.	ISIF_CCDCFG[1:0] SDRPACK	
Enable or disable VD/HD output.	ISIF_SYNCEN[0] SYEN	

8.3.4.1.2 ISS ISP ISIF Enable/Disable Hardware

The ISIF is enabled by setting the ISIF_SYNCEN[0] SYEN bit. This is done after all the required registers discussed in the previous section are programmed.

With respect to the write-enable bit and output address, the following procedure must be followed:

1. Set the data output address (ISIF_CADU and ISIF_CADL).
2. Enable HD and VD and WEN at the same time (ISIF_MODESET[1] DWEN and ISIF_SYNCEN[0] SYEN).

If the ISIF_SYNCEN[0] SYEN bit is written before the output address and the SDRAM write-enable bit (not recommended but may be required for a particular mode), data begins to be written to the old address value and not the one recently programmed. The desired response can be achieved if the following procedure is followed:

1. Enable HD and VD (ISIF_SYNCEN[0] SYEN).
2. Set the output address (ISIF_CADU and ISIF_CADL).
3. Wait for the next VD.

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4. Enable WEN (ISIF_MODESET[1] DWEN).

The ISIF always operates in continuous mode. In other words, after enabling the ISIF, it continues to process sequential frames until software clears the ISIF_SYNCEN[0] SYEN bit. When this happens, the frame being processed is disabled immediately and does not continue to process the current frame.

When the HD and VD signals are set to outputs (ISIF_MODESET[0] HDVDD = 0x1), fetching and processing of the frame begin immediately upon setting the ISIF_SYNCEN[0] SYEN bit.

When the HD and VD signals are set to inputs (ISIF_MODESET[0] HDVDD = 0x0), processing of the frame is dependent on the input timing of the external sensor/decoder. To ensure that data from the external device is not missed, the ISIF must be enabled before data transmission from the external device. In this way, the ISIF waits for data from the external device.

8.3.4.1.3 ISS ISP ISIF Register Accessibility During Frame Processing

There are two types of register access in the ISIF:

- Shadowed registers (event latched registers)

  Shadowed registers are those that can be read and written at any time. However, the written values take effect (are latched) only at certain times based on some event. Reads still return the most-recent write even though the settings are not used until the specific event occurs.

- Busy-writable registers

  These registers/fields can be read or written even if the module is busy. Changes to the underlying settings occur instantly.

The following registers/fields can be set as shadow registers, or optionally set as busy-writable registers. When the ISIF_CCDCFG[15] VDLC bit is set to 0, these registers are shadowed; when the ISIF_CCDCFG[15] VDLC bit is set to 1, these registers are busy-writable. All other ISIF registers not included in this list are always busy-writable.

ISIF_SYNCEN[1] DWEN		ISIF_CGRGAIN	ISIF_FMTLSV
ISIF_MODESET[14] HLPF	ISIF_CULH	ISIF_CGBGAIN	ISIF_FMTLNV
ISIF_HDW	ISIF_CULV	ISIF_CBGAIN	ISIF_LSCHOFST
ISIF_VDW	ISIF_HSIZE	ISIF_COFSTA	ISIF_LSCVOFST
ISIF_PPLN		ISIF_CLAMPCFG[0] CLEN	ISIF_DFCCTL
ISIF_LPFR	ISIF_CADU	ISIF_MISC	ISIF_VDFSATLV
ISIF_SPH	ISIF_CADL	ISIF_CGAMMAWD	
ISIF_LNH	ISIF_CCOLP	ISIF_FMTSPH	
	ISIF_CRGAIN	ISIF_FMTLNH	
ISIF_SLV0	ISIF_SLV1	ISIF_SDOFST	

8.3.4.1.4 ISS ISP ISIF Interframe Operations

Between frames, it may be necessary to enable or disable functions or to modify the memory pointers. Because the ISIF_SYNCEN[1] DWEN bit and the memory pointer registers are shadowed, these modifications can occur any time before the end of the frame and the data will be latched in for the next frame. Likewise, the 2D-LSC registers can be changed after receiving the LSC SOF interrupt but before it starts to prefetch the gain values for the next frame (the end of the LSC active region is reached). The host controller can perform these changes when it receives an interrupt.

8.3.4.1.5 ISS ISP ISIF Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the ISIF. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- PCLK cannot be higher than 304 MHz.

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- If SDRAM output port is enabled:
  - The memory output line offset and address must be on 32-byte boundaries.
  - ISIF_LNH[14:0] LNH – 1 must be a multiple of 32 bytes.
  - ISIF_SPH, ISIF_LNH, ISIF_SLV0, ISIF_SLV1, and ISIF_LNV must be cleared to 0 within the same VD period in which the ISIF_SYNCEN[1] DWEN bit is cleared to 0.
  - ISIF_SPH, ISIF_LNH, ISIF_SLV0, ISIF_SLV1, and ISIF_LNV must be set from 0 to the appropriate values within the same VD period in which the ISIF_SYNCEN[1] DWEN bit is set to 1.
- In RAW input mode: The ISIF_CCDCFG[4] YCINSWP must be set to 0.
- If DPCM compression is enabled: The horizontal culling must not be used. Use the input formatter instead.
- For 2D-LSC:
  - N <= M (where M = horizontal downsampling factor, N = vertical downsampling factor)
  - The ISIF_2DLSCINI register values must be even numbers.
  - Maximum widths with respect to selected M value (see Table 8-466)

Table 8-466. ISS ISP ISIF Maximum Line Width Versus M Value

M	Maximum Line Width
8	2040
16	4080
32	8160
64	16,320
128	16,384

8.3.4.2 ISS ISP IPIPEIF Programming Model

This section discusses issues related to the software control of the IPIPEIF module. It lists the registers that are required to be programmed in different modes, describes how to enable and disable the IPIPEIF module and how to check the status of the IPIPEIF module, discusses the different register access types, and enumerates several programming constraints.

8.3.4.2.1 ISS ISP IPIPEIF Hardware Setup/Initialization

This section discusses the configuration of the IPIPEIF module required before image processing can begin.

8.3.4.2.1.1 ISS ISP IPIPEIF Reset Behavior

Upon hardware reset of the ISP (ISP5_SYSCONFIG[1] SOFTRESET = 0x1), all the registers in the IPIPEIF are reset to their reset values.

8.3.4.2.1.2 ISS ISP IPIPEIF Register Setup

Before enabling the IPIPEIF, the hardware must be properly configured through register writes. Table 8-467 identifies the register parameters that must be programmed before enabling the IPIPEIF module (depending on the functions needed).

Table 8-467. ISS ISP IPIPEIF Required Configuration Parameters

Step	Configuration Required	Value
General settings		
Select the input sources for IPIPEIF.	IPIPEIF_CFG1[15:14] INPSRC1	
	IPIPEIF_CFG1[3:2] INPSRC2	
Select VD sync polarity.	IPIPEIF_CFG2[2] VDPOL	
Select HD sync polarity.	IPIPEIF_CFG2[1] HDPOL	

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Table 8-467. ISS ISP IPIPEIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Select the interrupt source.	IPIPEIF_CFG2[0] INTSW	
Select the input clock source.	IPIPEIF_CFG1[10] CLKSEL	
Set the clock divider value.	IPIPEIF_CLKDIV[15:0] CLKDIV	
Set the data type: YUV or RAW.	IPIPEIF_CFG2[3] YUV16	
Settings to perform if data is from BL		
Set HD setting.	IPIPEIF_PPLN[12:0] PPLN	
Set VD setting.	IPIPEIF_LPFR[12:0] LPFR	
Set the number of valid pixels in a line.	IPIPEIF_HNUM[12:0] HNUM	
Set the number of valid lines.	IPIPEIF_VNUM[12:0] VNUM	
Set memory address information.	IPIPEIF_ADDRU[10:0] ADDRU	
	IPIPEIF_ADDRL[15:0] ADDRL	
	IPIPEIF_ADOFS[11:0] ADOFS	
Set one-shot mode, if needed.	IPIPEIF_CFG1[0] ONESHOT	
Use SYNCOFF function only for double-buffering. See Section 8.3.3.2.3.2.1 for details.	IPIPEIF_ENABLE[1] SYNCOFF	
Settings to perform for RAW data from ISIF or BL		
Select the unpack function.	IPIPEIF_CFG1[9:8] UNPACK	
Settings to perform for YUV data from ISIF		
Set the data type to YUV.	IPIPEIF_CFG2[3] YUV16	
If YUV16 = 0x1, enables or not the conversion from 8 bits to 16 bits	IPIPEIF_CFG2[6] YUV8	
If YUV16 = 0x1, set the way the data is unpacked.	IPIPEIF_CFG2[7] YUV8P	
DPCM function	RAW data from BL	
Enable or disable DPCM decompression.	IPIPEIF_DPCM[0] ENA	
Select DPCM prediction mode.	IPIPEIF_DPCM[1] PRED	
Select DPCM bit mode.	IPIPEIF_DPCM[2] BITS	
Select inverse A-Law function.	IPIPEIF_CFG1[9:8] UNPACK	
Select SDRAM read data shift. - For RAW data - DPCM enabled and A- Law disabled - or DPCM disabled	IPIPEIF_CFG1[13:11] DATASFT	
Dark frame subtraction (DFS) function	RAW data from (VP, BL, SDRAM) or ISIF	
Set defect pixel correction (DPC1) for VP or ISIF inputs.	IPIPEIF_DPC1[12] ENA	
Set the associated threshold for DPC1.	IPIPEIF_DPC1[11:0] TH	
Set defect pixel correction (DPC2) for BL inputs.	IPIPEIF_DPC2[12] ENA	
Set the associated threshold for DPC1.	IPIPEIF_DPC2[11:0] TH	
Set the direction of subtraction.	IPIPEIF_CFG2[5] DFSDIR	
Set the averaging filter, horizontal pixel decimator, and gain function for IPIPE data path.		
Enable averaging filter function.	IPIPEIF_CFG1[7] AVGFILT	
Enable horizontal pixel decimation function.	IPIPEIF_CFG1[1] DECIM	
Set horizontal resizing value.	IPIPEIF_RSZ[6:0] RSZ	
Set the resizer initial position.	IPIPEIF_INIRSZ[13] ALNSYNC	
	IPIPEIF_INIRSZ[12:0] INIRSZ	

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Table 8-467. ISS ISP IPIPEIF Required Configuration Parameters (continued)

Step	Configuration Required	Value
Set the data gain (only for RAW data).	IPIPEIF_GAIN[9:0] GAIN	
Set the output clipping value.	IPIPEIF_OCLIP[11:0] OCLIP	
Set the averaging filter and horizontal pixel decimator function for H3A data path.		
Enable averaging filter function.	IPIPEIF_RSZ3A[8] AVGFILT	
Enable horizontal pixel decimation function.	IPIPEIF_RSZ3A[9] DECIM	
Set horizontal resizing value.	IPIPEIF_RSZ3A[6:0] RSZ	
Set the resizer initial position.	IPIPEIF_RSZ3A[13] ALNSYNC	
	IPIPEIF_RSZ3A[12:0] INIRSZ	

For information about YUV data coming and unpacking from the ISIF module, see Section 8.3.3.2.13, *ISS ISP IPIPEIF YUV4:2:2 8-bit Packed Data Input Coming From ISIF Module*.

8.3.4.2.2 ISS ISP IPIPEIF Enable/Disable Hardware

When IPIPEIF_CFG1[15:14] INPSRC1 or IPIPEIF_CFG1[3:2] INPSRC2 = 0, the IPIPEIF does not need to be enabled: it receives data from the VP and pushes it to the ISIF, H3A, IPIPE, and RESIZER modules.

If IPIPEIF_CFG1[15:14] INPSRC1 or IPIPEIF_CFG1[3:2] INPSRC2 ≠ 0, the IPIPEIF module begins to fetch data from the BL by setting the IPIPEIF_ENABLE[0] ENABLE bit. Writing the enable bit must be the last step of the configuration.

When the input source is the BL, the IPIPEIF can optionally operate in one-shot mode or continuous mode by setting the IPIPEIF_CFG1[0] ONESHOT bit. If one-shot mode is enabled, then after enabling the IPIPEIF, the IPIPEIF_ENABLE[0] ENABLE bit is automatically turned off (set to 0) and only a single frame is processed from memory. In this mode, fetching and processing of the frame begins immediately upon setting the IPIPEIF_ENABLE[0] ENABLE bit.

When the input source is the ISIF, processing of the frame depends on the timing of the ISIF. To ensure that data from the ISIF is not missed, the IPIPEIF must be enabled before the ISIF. In this way, the IPIPEIF waits for data from the ISIF.

When the IPIPEIF is in continuous mode, it can be disabled by clearing the IPIPEIF_ENABLE[0] ENABLE bit after processing of the last frame. The disable occurs immediately because it is a busy-writable register.

An EOF interrupt can indicate to other modules that the frame treatment is finished. For more information, see Section 8.3.3.2.15, *ISS ISP IPIPEIF Module Events and Status Checking*.

8.3.4.2.3 ISS ISP IPIPEIF Register Accessibility During Frame Processing

There are two types of register accesses in the IPIPEIF:

- Shadow registers

  These registers/fields can be read and written (if the field is writable) at any time. However, the written values take effect only at the start of a frame (VD rising edge). Reads still return the most-recent write even though the settings are not used until the next start of frame. The following are the shadowed registers in the IPIPEIF:

IPIPEIF_PPLN
IPIPEIF_HNUM
IPIPEIF_VNUM
IPIPEIF_GAIN
IPIPEIF_RSZ3A[6:0] RSZ
IPIPEIF_ADDRU
IPIPEIF_ADOFS
IPIPEIF_ENABLE[1] SYNCOFF
IPIPEIF_RSZ3A[9] DECIM
IPIPEIF_CFG1[1] DECIM
IPIPEIF_CFG1[7] AVGFILT
IPIPEIF_RSZ
IPIPEIF_RSZ3A[8] AVGFILT

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- Busy-writable registers

  These registers/fields can be read or written even if the module is busy. Changes to the underlying settings occurs instantaneously. Registers that are not shadowed are busy-writable.

Only for busy-writable registers, the ideal procedure for changing the IPIPEIF registers is if (PCR.BUSY == 0) or if (EOF interrupt occurs):

1. Disable IPIPEIF (IPIPEIF_ENABLE[0] ENABLE = 0x0).
2. Change registers.
3. Enable IPIPEIF (IPIPEIF_ENABLE[0] ENABLE = 0x1).

8.3.4.2.4 ISS ISP IPIPEIF Interframe Operations

Between frames, it may be necessary to enable or disable functions or to modify the memory pointers. Because several of the registers are shadowed, these modifications can take place any time before the end of the frame, and the data is latched in for the next frame. The host controller can perform these changes when it receives an interrupt.

When reading input data from the BL, the host must check IPIPEIF_DTUF or the ISP5_IRQSTATUS_RAW2_i[1] IPIPEIF_UDF bit (if this event is enabled and mapped to the ISP IRQ lines) during vertical blanking to see if an underflow occurred.

If an underflow occurs it means the system is congested because too much bandwidth is being generated. Most likely, the scenario being passed is too memory bandwidth-intensive. If the bit is set, software must clear the bit. If the process is taking place from memory-to-memory, software may try to reinitiate the data flow. Software must decide the sequence to execute after an underflow.

8.3.4.2.5 ISS ISP IPIPEIF Summary of Constraints

Adhere to the following list of register configuration constraints when programming the IPIPEIF module. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- If BL is the source for the IPIPEIF:
  - The memory output line offset and address must be on 32-byte boundaries.
  - In DFS block, IPIPEIF_LPFR must be > 0, because the first line cannot be fetched.
  - IPIPEIF_PPLN > IPIPEIF_HNUM
  - IPIPEIF_LPFR > IPIPEIF_VNUM + 1
- There are restrictions on IPIPEIF_CFG1[15:14] INPSRC1 and IPIPEIF_CFG1[3:2] INPSRC2 combinations. See Table 8-422 for details.

8.3.4.3 ISS ISP IPIPE Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the ISS ISP IPIPE module.

8.3.4.3.1 Global Initialization

8.3.4.3.1.1 Surrounding Modules Global Initialization

This initialization of surrounding modules is based on the integration of the ISS ISP.

8.3.4.3.1.2 ISS ISP IPIPE Global Initialization

8.3.4.3.1.2.1 Main Sequence – ISS ISP IPIPE Global Initialization

The procedure in Table 8-468 initializes the ISS ISP IPIPE modules after a POR or software reset.

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Table 8-468. ISS Global Initialization

Step	Register/Bit Field/Programming Model	Value
Set the IPIPE processing modes.	IPIPE_SRC_MODE[0] OST	0x-
Select the IPIPEIF module as a source.	IPIPE_SRC_MODE[1] WRT	0x1
Set the vertical start position of the window to process.	IPIPE_SRC_VPS[15:0] VAL	0x-
Set the horizontal start position of the window to process.	IPIPE_SRC_HPS[15:0] VAL	0x-
Set the vertical size of the processing area.	IPIPE_SRC_VSZ[12:0] VAL	0X-
Set the horizontal size of the processing area.	IPIPE_SRC_HSZ[12:1] VAL	0x-
Enable clk_arm_g0.	IPIPE_GCK_MMR[0] REG	0x-
Enable clk_pix_g3.	IPIPE_GCK_PIX[3] G3	0x-
Enable clk_pix_g2.	IPIPE_GCK_PIX[2] G2	0x-
Enable clk_pix_g1.	IPIPE_GCK_PIX[1] G1	0x-
Enable clk_pix_g0.	IPIPE_GCK_PIX[0] G0	0x-
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.3.1.2.2 Subsequence – ISS ISP IPIPE Defect Pixel Correction Initialization

8.3.4.3.1.2.2.1 Subsequence – ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC)

The procedure in Table 8-469 initializes the ISS ISP IPIPE LUT defect pixel correction (LUT DPC).

Table 8-469. ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC)

Step	Register/Bit Field/Programming Model	Value
Set the address of the first valid data in the LUT.	IPIPE_DPC_LUT_ADR[9:0] ADR	0x-
Set the LUT type.	IPIPE_DPC_LUT_SEL[1] TBL	0x-
Set the size of the LUT.	IPIPE_DPC_LUT_SIZ[9:0] SIZ	0x-
Set the dot replacement correction method.	IPIPE_DPC_LUT_SEL[0] DOT	0x-
Enable LUT DPC.	IPIPE_DPC_LUT_EN[0] EN	0x1

8.3.4.3.1.2.3 Subsequence – ISS ISP IPIPE White Balance Initialization

The procedure in Table 8-470 initializes the ISS ISP IPIPE white balance.

Table 8-470. ISS ISP IPIPE White Balance Initialization

Step	Register/Bit Field/Programming Model	Value
Set the offset before white balance.	IPIPE_WB2_OFT_R[11:0] VAL IPIPE_WB2_OFT_GR[11:0] VAL IPIPE_WB2_OFT_GB[11:0] VAL IPIPE_WB2_OFT_B[11:0] VAL	0x-
Set the white balance gain.	IPIPE_WB2_WGN_R[12:0] VAL IPIPE_WB2_WGN_GR[12:0] VAL IPIPE_WB2_WGN_GB[12:0] VAL IPIPE_WB2_WGN_B[12:0] VAL	0x-

8.3.4.3.1.2.4 Subsequence – ISS ISP IPIPE RGB2RGB Blending Module Initialization

The procedure in Table 8-471 initializes the ISS ISP IPIPE RGB2RGB blending module.

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Table 8-471. ISS ISP IPIPE RGB2RGB Blending Module Initialization

Step	Register/Bit Field/Programming Model	Value
Set gain range.	IPIPE_RGB1_MUL_RR[11:0] VAL IPIPE_RGB1_MUL_GR[11:0] VAL IPIPE_RGB1_MUL_BR[11:0] VAL IPIPE_RGB1_MUL_RG[11:0] VAL IPIPE_RGB1_MUL_GG[11:0] VAL IPIPE_RGB1_MUL_BG[11:0] VAL IPIPE_RGB1_MUL_RB[11:0] VAL IPIPE_RGB1_MUL_GB[11:0] VAL IPIPE_RGB1_MUL_BB[11:0] VAL	0x-
Se the offset range for each component.	IPIPE_RGB1_OFT_OR[12:0] VAL IPIPE_RGB1_OFT_OG[12:0] VAL IPIPE_RGB1_OFT_OB[12:0] VAL	0x-

8.3.4.3.1.2.5 Subsequence – ISS ISP IPIPE Gamma Correction Module Initialization

The procedure in Table 8-472 initializes the ISS ISP IPIPE gamma correction module.

Table 8-472. ISS ISP IPIPE Gamma Correction Module Initialization

Step	Register/Bit Field/Programming Model	Value
Select the gamma table.	IPIPE_GMM_CFG[4] TBL	0x-
Set the size of the gamma table.	IPIPE_GMM_CFG[6:5] SIZ	0x-
(optional) Insert bypass bit for each color.	IPIPE_GMM_CFG[0] BYPR IPIPE_GMM_CFG[1] BYPG IPIPE_GMM_CFG[2] BYPB	0x1

8.3.4.3.1.2.6 Subsequence – ISS ISP IPIPE 2nd RGB2RGB Conversion Matrix Initialization

The procedure in Table 8-473 initializes the Second ISS ISP IPIPE RGB2RGB conversion matrix.

Table 8-473. ISS ISP IPIPE Second RGB2RGB Conversion Matrix Initialization

Step	Register/Bit Field/Programming Model	Value
Set the gain range.	IPIPE_RGB2_MUL_RR[10:0] VAL IPIPE_RGB2_MUL_GR[10:0] VAL IPIPE_RGB2_MUL_BR[10:0] VAL IPIPE_RGB2_MUL_RG[10:0] VAL IPIPE_RGB2_MUL_GG[10:0] VAL IPIPE_RGB2_MUL_BG[10:0] VAL IPIPE_RGB2_MUL_RB[10:0] VAL IPIPE_RGB2_MUL_GB[10:0] VAL IPIPE_RGB2_MUL_BB[10:0] VAL	0x-
Set the offset.	IPIPE_RGB2_OFT_OR[10:0] VAL IPIPE_RGB2_OFT_OG[10:0] VAL IPIPE_RGB2_OFT_OB[10:0] VAL	0x-

8.3.4.3.1.2.7 Subsequence – ISS ISP IPIPE RGB2YCbCr Conversion Matrix Initialization

The procedure in Table 8-474 initializes the ISS ISP IPIPE RGB2YCbCr conversion matrix.

Table 8-474. ISS ISP IPIPE RGB2YCbCr Conversion Matrix Initialization

Step	Register/Bit Field/Programming Model	Value
Set the brightness control.	IPIPE_YUV_ADJ[15:8] BRT	0x-
Set the contrast control.	IPIPE_YUV_ADJ[7:0] CRT	0x-

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Table 8-474. ISS ISP IPIPE RGB2YCbCr Conversion Matrix Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Configure the gain range.	IPIPE_YUV_MUL_RY[11:0] VAL IPIPE_YUV_MUL_GY[11:0] VAL IPIPE_YUV_MUL_BY[11:0] VAL IPIPE_YUV_MUL_RCB[11:0] VAL IPIPE_YUV_MUL_GCB[11:0] VAL IPIPE_YUV_MUL_BCB[11:0] VAL IPIPE_YUV_MUL_RCR[11:0] VAL IPIPE_YUV_MUL_GCR[11:0] VAL IPIPE_YUV_MUL_BCR[11:0] VAL	0x-
Set the output offset value for Y.	IPIPE_YUV_OFT_Y[10:0] VAL	0x-
Set the output offset value for Cr.	IPIPE_YUV_OFT_CR[10:0] VAL	0x-
Set the output offset value for Cb.	IPIPE_YUV_OFT_CB[10:0] VAL	0x-

8.3.4.3.1.2.8 Subsequence – ISS ISP IPIPE 4:2:2 Conversion Module Initialization

The procedure in Table 8-475 initializes the ISS ISP IPIPE 4:2:2 conversion module.

Table 8-475. ISS ISP IPIPE 4:2:2 Conversion Module Initialization

Step	Register/Bit Field/Programming Model	Value
If: RAW BAYER data set as an input?	IPIPE_SRC_FMT[1:0] FMT	= 0x0
Select the Y and Cb/Cr sampling point.	IPIPE_YUV_PHS[0] POS	0x-
Enable 4:2:2 conversion module.	IPIPE_YUV_PHS[1] PLF	0x-
ELSE		

8.3.4.3.1.2.9 Subsequence – ISS ISP IPIPE 2D Edge-Enhancer Initialization

The procedure in Table 8-476 initializes the ISS ISP IPIPE 2D edge enhancer.

Table 8-476. ISS ISP IPIPE 2D Edge-Enhancer Initialization

Step	Register/Bit Field/Programming Model	Value
Set the merging method.	IPIPE_YEE_TYP[0] SEL	0x-
Set the downshift length of HPF in the edge-enhancer.	IPIPE_YEE_SHF[3:0] SHF	0x-
Set the edge-enhancer lower threshold before referring to the LUT.	IPIPE_YEE_THR[5:0] VAL	0x-
Set the multiplier coefficient in the HPF.	IPIPE_YEE_MUL_00[9:0] VAL IPIPE_YEE_MUL_01[9:0] VAL IPIPE_YEE_MUL_02[9:0] VAL IPIPE_YEE_MUL_10[9:0] VAL IPIPE_YEE_MUL_11[9:0] VAL IPIPE_YEE_MUL_12[9:0] VAL IPIPE_YEE_MUL_20[9:0] VAL IPIPE_YEE_MUL_21[9:0] VAL IPIPE_YEE_MUL_22[9:0] VAL	0x-
Set the edge sharpener HPF value lower limit.	IPIPE_YEE_E_THR_1[11:0] VAL	0x-
Set the edge sharpener HPF value upper limit.	IPIPE_YEE_E_THR_2[5:0] VAL	0x-
Set the edge sharpener gain value on gradient.	IPIPE_YEE_G_GAN[7:0] VAL	0x-
Set the edge sharpener gain value.	IPIPE_YEE_E_GAN[7:0] VAL	0x-
Set the edge sharpener offset value on gradient.	IPIPE_YEE_G_OFT[5:0] VAL	0x-
Enable the 2D edge-enhancer.	IPIPE_YEE_EN[0] EN	0x1

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8.3.4.3.1.2.10 Subsequence – ISS ISP IPIPE Histogram Initialization

The procedure in Table 8-477 initializes the ISS ISP IPIPE histogram.

Table 8-477. ISS ISP IPIPE Histogram Initialization

Step	Register/Bit Field/Programming Model	Value
Select input source.	IPIPE_HST_SEL[2] SEL	0x-
Select the Bayer mode.	IPIPE_HST_SEL[1:0] TYP	0x-
Set the number of bins.	IPIPE_HST_PARA[13:12] BIN	0x-
Enable region(area) 0.	IPIPE_HST_PARA[0] RGN0	0x-
Enable region(area) 1.	IPIPE_HST_PARA[1] RGN1	0x-
Enable region(area) 2.	IPIPE_HST_PARA[2] RGN2	0x-
Enable region(area) 3.	IPIPE_HST_PARA[3] RGN3	0x-
Set the vertical position of region 0.	IPIPE_HST_0_VPS[12:1] VAL	0x-
Set the vertical position of region 1.	IPIPE_HST_1_VPS[12:1] VAL	0x-
Set the vertical position of region 2.	IPIPE_HST_2_VPS[12:1] VAL	0x-
Set the vertical position of region 3.	IPIPE_HST_3_VPS[12:1] VAL	0x-
Set the horizontal position of region 0.	IPIPE_HST_0_HPS[12:1] VAL	0x-
Set the horizontal position of region 1.	IPIPE_HST_0_HPS[12:1] VAL	0x-
Set the horizontal position of region 2.	IPIPE_HST_0_HPS[12:1] VAL	0x-
Set the horizontal position of region 3.	IPIPE_HST_0_HPS[12:1] VAL	0x-
Set the vertical size of region 0.	IPIPE_HST_0_VSZ[12:1] VAL	0x-
Set the vertical size of region 1.	IPIPE_HST_1_VSZ[12:1] VAL	0x-
Set the vertical size of region 2.	IPIPE_HST_2_VSZ[12:1] VAL	0x-
Set the vertical size of region 3.	IPIPE_HST_3_VSZ[12:1] VAL	0x-
Set the horizontal size of region 0.	IPIPE_HST_0_HSZ[12:1] VAL	0x-
Set the horizontal size of region 1.	IPIPE_HST_1_HSZ[12:1] VAL	0x-
Set the horizontal size of region 2.	IPIPE_HST_2_HSZ[12:1] VAL	0x-
Set the horizontal size of region 3.	IPIPE_HST_3_HSZ[12:1] VAL	0x-
Enable selection of the color pattern 0 (R).	IPIPE_HST_PARA[4] COL0	0x-
Enable selection of the color pattern 1 (G).	IPIPE_HST_PARA[5] COL1	0x-
Enable selection of the color pattern 2 (B).	IPIPE_HST_PARA[6] COL2	0x-
Enable selection of the color pattern 3 (Y).	IPIPE_HST_PARA[7] COL3	0x-
Set the shift length of the input data.	IPIPE_HST_PARA[11:8] SHF	0x-
Enable/disable histogram memory clear.	IPIPE_HST_TBL[1] CLR	0x-
Select table for store the histogram data.	IPIPE_HST_TBL[1] CLR	0x-
IF: Is input from noise filter?	IPIPE_HST_SEL[2] SEI	0x0
Gain for color for R.	IPIPE_HST_MUL_R[7:0] GAIN	0x-
Gain for color for GR.	IPIPE_HST_MUL_GR[7:0] GAIN	0x-
Gain for color for GB.	IPIPE_HST_MUL_GB[7:0] GAIN	0x-
Gain for color for B.	IPIPE_HST_MUL_B[7:0] GAIN	0x-
ENDIF		
Select processing mode.	IPIPE_HST_MODE[0] OST	0x-
Enable histogram.	IPIPE_HST_EN[0] EN	0x1

8.3.4.3.1.2.11 Subsequence – ISS ISP IPIPE Boxcar Initialization

The procedure in Table 8-478 initializes the ISS ISP IPIPE boxcar.

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Table 8-478. ISS ISP IPIPE Boxcar Initialization

Step	Register/Bit Field/Programming Model	Value
Select the processing mode.	IPIPE_BOX_MODE[0] OST	0x-
Set the size of blocks.	IPIPE_BOX_TYP[0] SEL	0x-
Set the higher 16 bits of the first address of output in memory.	IPIPE_BOX_SDR_SAD_H[15:0] VAL	0x-
Set the lower 16 bits of the first address of output in memory.	IPIPE_BOX_SDR_SAD_L[15:5] VAL	0x-
Set the downshift value.	IPIPE_BOX_SHF[2:0] VAL	0x-
Enable boxcar.	IPIPE_BOX_EN[0] EN	0x1

8.3.4.3.2 ISS ISP IPIPE Operational Modes Configuration

8.3.4.3.2.1 ISS ISP IPIPE Processing Path: Case 1 Configuration

Table 8-479 lists the ISS ISP IPIPE processing path: case 1 configuration procedures.

Table 8-479. ISS ISP IPIPE Processing Path: Case 1 Configuration

Step	Register/Bit Field/Programming Model	Value
Select processing path: Case 1	IPIPE_SRC_FMT[1:0] FMT	0x0
Configure IPIPE DPC.	See Section 8.3.4.3.1.2.2, *Subsequence – ISS ISP IPIPE Defect Pixel Correction Initialization*.	
Configure IPIPE white balance.	See Section 8.3.4.3.1.2.3, *Subsequence – ISS ISP IPIPE White Balance Initialization*.	
Configure IPIPE RGB2RGB blending module.	See Section 8.3.4.3.1.2.4, *Subsequence – ISS ISP IPIPE RGB2RGB Blending Module Initialization*.	
Configure IPIPE gamma correction module.	See Section 8.3.4.3.1.2.5, *Subsequence – ISS ISP IPIPE Gamma Correction Module Initialization*.	
Configure IPIPE second RGB2RGB conversion matrix.	See Section 8.3.4.3.1.2.6, *Subsequence – ISS ISP IPIPE Second RGB2RGB Conversion Matrix Initialization*.	
Configure IPIPE RGB2YCbCr conversion matrix.	See Section 8.3.4.3.1.2.7, *Subsequence – ISS ISP IPIPE RGB2YCbCr Conversion Matrix Initialization*.	
Configure IPIPE 2D edge-enhancer.	See Section 8.3.4.3.1.2.9, *Subsequence – ISS ISP IPIPE 2D Edge Enhancer Initialization*.	
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.3.2.2 ISS ISP IPIPE Processing Path: Case 2 Configuration

Table 8-480 lists the ISS ISP IPIPE processing path: case 2 configuration procedures.

Table 8-480. ISS ISP IPIPE Processing Path: Case 2 Configuration

Step	Register/Bit Field/Programming Model	Value
Select processing path: Case 2.	IPIPE_SRC_FMT[1:0] FMT	0x1
Configure IPIPE DPC.	See Section 8.3.4.3.1.2.2, *Subsequence – ISS ISP IPIPE Defect Pixel Correction Initialization*.	
Configure IPIPE white balance.	See Section 8.3.4.3.1.2.3, *Subsequence – ISS ISP IPIPE White Balance Initialization*.	
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.3.2.3 ISS ISP IPIPE Processing Path: Case 3 Configuration

Table 8-481 lists the ISS ISP IPIPE processing path: case 3 configuration procedures.

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Table 8-481. ISS ISP IPIPE Processing Path: Case 3 Configuration

Step	Register/Bit Field/Programming Model	Value
Select processing path: Case 3.	IPIPE_SRC_FMT[1:0] FMT	0x3
Configure IPIPE 2D edge enhancer.	See Section 8.3.4.3.1.2.9, *Subsequence - ISS ISP IPIPE 2D Edge Enhancer Initialization*.	
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.3.2.4 ISS ISP IPIPE Processing Path: Case 4 Configuration

Table 8-482 lists the ISS ISP IPIPE processing path: case 4 configuration procedures.

Table 8-482. ISS ISP IPIPE Processing Path: Case 4 Configuration

Step	Register/Bit Field/Programming Model	Value
Select processing path: Case 4.	IPIPE_SRC_FMT[1:0] FMT	0x2
Configure IPIPE boxcar.	See Section 8.3.4.3.1.2.11, *Subsequence – ISS ISP IPIPE Boxcar Initialization*.	
Configure IPIEE histogram.	See Section 8.3.4.3.1.2.10, *Subsequence – ISS ISP IPIPE Histogram Initialization*.	
Enable IPIPE module.	IPIPE_SRC_EN[0] EN	0x1

8.3.4.4 ISS ISP RSZ Programming Model

This section discusses programming configuration steps related to software control of the RSZ. It lists the registers that must be programmed in different modes, describes how to enable and disable the RSZ and how to check the status of the image resizing procedure, and discusses the different register access types and several programming constraints.

8.3.4.4.1 ISS ISP RSZ Hardware Setup/Initialization

This section discusses the configuration of the RSZ required before image processing can begin.

8.3.4.4.1.1 ISS ISP RSZ Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the RSZ module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the RSZ. For more information, see Section 8.3.3.4.4, *ISS ISP RSZ Integration.*

Table 8-483 lists the ISS ISP RSZ surrounding modules global initialization.

Table 8-483. ISS ISP RSZ Surrounding Modules Global Initialization

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. RSZ is part of ISP, which is part of ISS. To enable the clocks for ISS, see Chapter 3, *Power, Reset, and Clock Management*. Also see Section 8.3.2.1.1, *ISS ISP Clocks*.
(optional) MPU/IPU INTC	The MPU/IPU INTC must be configured to enable interrupts from the RSZ. For information about how to configure the local ISS interrupt channels, see Section 8.3.2.2, *ISS ISP Interrupt Tree*, and Section 8.1.2.1.1, *ISS Interrupt Merger*. Then, to configure the outside ISS boundary channels, see Chapter 17, *Interrupt Controllers*.
(optional) IPIPE	Configure the IPIPE module to process and pass data to the RSZ module. See Section 8.3.4.3, *ISS ISP IPIPE Programming Model*.
(optional) IPIPEIF	Configure the IPIPEIF module to process and pass data to the RSZ module. See Section 8.3.4.2, *ISS ISP IPIPEIF Programming Model*.

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Table 8-483. ISS ISP RSZ Surrounding Modules Global Initialization (continued)

Surrounding Modules	Comments
(optional) BL	Configure the BL for reading back data from memory. See Section 8.3.4.6, *ISS ISP BL Programming Model*.
(optional) CSI2	If the data comes from the sensor, configure the CSI2-A interface. See Section 8.2.5.4, *ISS CSI2 Programming Model*.
(optional) CCP2	If the data comes from the sensor, configure the CCP2 interface. See Section 8.2.4.4, *ISS CCP2 Programming Model*.

NOTE: The MPU/IPU INTC configurations are necessary if the interrupt-based communication modes are used. The IPIPE or IPIPEIF configuration is also necessary for putting data into the RSZ. Moreover, if data comes from memory, the BL must be configured. If data comes from the image sensor CSI2 or CCP2, the interface must be configured.

8.3.4.4.1.2 ISS ISP RSZ Initial Register Setup

Before enabling the RSZ, the hardware must be properly configured through register writes. Table 8-484 identifies the sequence to be used before enabling the hardware.

Table 8-484. ISS ISP RSZ Initial Register Setup

Step	Register/Bit Field/Programming Model	Value
Set the MMR clock to enable RSZ register read/write access.	RSZ_GCK_MMR[0] MMR	0x1
Determine whether or not a bypass mode will be used and set the RSZ core functional clock accordingly.	RSZ_GCK_SDR[0] CORE	0x-
IF: Is the core clock enabled?	RSZ_GCK_SDR[0] CORE	= 0x1
Enable RSZ engine clocks.	RSZ_SYSCONFIG[8] RSZA_CLK_EN RSZ_SYSCONFIG[9] RSZB_CLK_EN	0x1
ELSE: The input data buffer is not used?	RSZ_GCK_SDR[0] CORE	= 0x0
Set the bypass mode accordingly.	RSZ_SRC_FMT0[1] BYPASS	0x-
ENDIF		
Enable the RSZ core clock.	RSZ_GCK_SDR[0] CORE	0x1
Determine the upscale ratio and functional clock, and adjust the fractional clock divider as appropriate.	RSZ_FRACDIV[15:0] RSZ_FRACDIV	0x-
Set the low threshold of the RSZ input data buffer as appropriate.	RSZ_IN_FIFO_CTRL[28:16] THRLD_LOW	0x-
Set the high threshold of the RSZ input data buffer as appropriate.	RSZ_IN_FIFO_CTRL[12:0] THRLD_HIGH	0x-
Determine whether IPIPE or IPIPEIF will be the source of input and set this bit accordingly.	RSZ_SRC_FMT0[0] SEL	0x-
Determine whether the RSZ will process as long as data is present in the input buffer, or whether it will wait for a WEN signal from the input source (IPIPE or IPIPEIF) to process lines arrived only during WEN high state.	RSZ_SRC_MODE[1] WRT	0x-
Select the processing mode (one shot or free running). This bit controls the RSZ module. There are also additional mode settings for the two RSZ engines within. After RSZ reset, the mode is automatically set to free running.	RSZ_SRC_MODE[0] OST	0x-

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Table 8-484. ISS ISP RSZ Initial Register Setup (continued)

Step	Register/Bit Field/Programming Model	Value
Configure the number of interrupt intervals for writing lines into CBUFF for the two RSZ engines.	RSZ_IRQ_RZA[12:0] RZA RSZ_IRQ_RZB[12:0] RZB	0x-
Enable the RSZ module.	RSZ_SRC_EN[0] EN	0x1
Enable resizer engine A.	RZA_EN[0] EN	0x1
Enable resizer engine B.	RZB_EN[0] EN	0x1

NOTE: RSZ-A or RSZ-B must be enabled after setting all needed configuration parameters.

8.3.4.4.1.3 ISS ISP RSZ Reset Behavior

Because the RSZ module has no software reset, software can issue one at the ISP level. Moreover, upon hardware reset, all the registers in the RSZ are reset to their reset values. Table 8-485 identifies the proper software sequence before and after RSZ reset issues at the ISP level.

Table 8-485. ISS ISP RSZ Reset Behavior

Step	Register/Bit Field/Programming Model	Value
ELSE IF: Is FIFO overflow or blanking error present?	ISP5_IRQSTATUS_i[18] RSZ_FIFO_IN_OVF or ISP5_IRQSTATUS_i[19] RSZ_FIFO_IN_BLK_ERR	= 0x1
Clear the FIFO blanking event.	ISP5_IRQENABLE_CLR_i[19] RSZ_FIFO_IN_BLK_ERR	0x1
Clear the overflow event.	ISP5_IRQENABLE_CLR_i[18] RSZ_FIFO_IN_OVF	0x1
ELSE: No FIFO overflow or blanking error is present?		
Wait until there is no DMA process and the module ready for reset.	ISP5_SYSCONFIG[1] SOFTRESET and ISP5_IRQSTATUS_i[15] RSZ_INT_DMA	= 0x0
ENDIF		
Disable the source data.	RSZ_SRC_EN[0] EN	0x0
Reset the RSZ at the ISP level.	ISP5_SYSCONFIG[1] SOFTRESET	0x1
Check whether the RSZ has been reset properly.	ISP5_SYSCONFIG[1] SOFTRESET	0x-

8.3.4.4.2 ISS ISP RSZ Global Image Processing Settings

This section discusses the configuration of the RSZ global settings before and during image frame processing. Table 8-486 identifies the global RSZ functional sequence, which includes global control, frame settings, bandwidth control, and reversal output image frames.

Table 8-486. ISS ISP RSZ Global Image Processing Settings

Step	Register/Bit Field/Programming Model	Value
Initialize the RSZ module.	See Section 8.3.4.4.1.	
Determine input data type and configure the source parameters.	See Section 8.3.4.4.2.1.	
Determine if vertical flip of the output image will be performed by the two resizer engines and set accordingly.	RSZ_SEQ[1] VRVA	0x-
	RSZ_SEQ[3] VRVB	

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Table 8-486. ISS ISP RSZ Global Image Processing Settings (continued)

Step	Register/Bit Field/Programming Model	Value
Determine if horizontal flip of the output image will be performed by the two resizer engines and set accordingly.	RSZ_SEQ[0] HRVA	0x-
	RSZ_SEQ[2] HRVB	
Set the baseline address of the RSZ output to CBUFF. Best performance can be achieved by assigning address on a 128-byte boundary.	RZA_SDR_Y_BAD_H[15:0] Y_BAD_H	0x-
	RZA_SDR_Y_BAD_L[15:0] Y_BAD_L	
	RZB_SDR_Y_BAD_H[15:0] Y_BAD_H	
	RZB_SDR_Y_BAD_L[15:0] Y_BAD_L	
	RZA_SDR_C_BAD_H[15:0] C_BAD_H	
	RZA_SDR_C_BAD_L[15:0] C_BAD_L	
	RZB_SDR_C_BAD_H[15:0] C_BAD_H	
	RZB_SDR_C_BAD_L[15:0] C_BAD_L	
Set the start address of the RSZ output to CBUFF. The first data output will be written to this address. If the first line of a frame is written at the beginning of the CBUFF memory, then SAD = BAD and PTR_S = 0. It is strongly advised to set up this address on a 128-byte boundary, which leads to the best performance.	RZA_SDR_Y_SAD_H[15:0] Y_SAD_H	0x-
	RZA_SDR_Y_SAD_L[15:0] Y_SAD_L	
	RZB_SDR_Y_SAD_H[15:0] Y_SAD_H	
	RZB_SDR_Y_SAD_L[15:0] Y_SAD_L	
	RZA_SDR_C_SAD_H[15:0] C_SAD_H	
	RZA_SDR_C_SAD_L [15:0] C_SAD_L	
	RZB_SDR_C_SAD_H[15:0] C_SAD_H	
	RZB_SDR_C_SAD_L[15:0] C_SAD_L	
Set the start pointer of the CBUFF internal counter. It must be set up as PTR_S = (SAD – BAD) / OFT. PTR_S is expressed in number of lines.	RZA_SDR_Y_PTR_S[12:0] Y_PTR_S	0x-
	RZB_SDR_Y_PTR_S[12:0] Y_PTR_S	
	RZA_SDR_C_PTR_S[12:0] C_PTR_S	
	RZB_SDR_C_PTR_S[12:0] C_PTR_S	
Set the end pointer of the CBUFF internal counter. PTR_E is expressed in number of lines. The CBUFF can contain up to PTR_E lines.	RZA_SDR_Y_PTR_E[12:0] Y_PTR_E	0x-
	RZB_SDR_Y_PTR_E[12:0] Y_PTR_E	
	RZA_SDR_C_PTR_E[12:0] C_PTR_E	
	RZB_SDR_C_PTR_E[12:0] C_PTR_E	
Set the line of offset expressed in bytes between two lines in the CBUFF (Line 0 = SAD, Line 1 = SAD + 1 x OFT, Line 2 = SAD + 2 x OFT). PTR_E is expressed in number of lines. The CBUFF can contain up to PTR_E lines. Note: OFT does not necessarily correspond to the size of a line in a frame; it can be much bigger. The line offset must be a multiple of 128 bytes.	RZA_SDR_Y_OFT[16:0] Y_OFT	0x-
	RZB_SDR_Y_OFT[16:0] Y_OFT	
	RZA_SDR_C_OFT[16:0] C_OFT	

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Table 8-486. ISS ISP RSZ Global Image Processing Settings (continued)

Step	Register/Bit Field/Programming Model	Value
	RZB_SDR_C_OFT[16:0] C_OFT	
Determine output data type, whether it will be flipped, and configure the output memory addresses.	See Section 8.3.4.4.2.2.	

NOTE: When data output is 4:2:2 or 4:2:0-Y only, the following values are not needed:

- RZx_SDR_C_BAD_x
- RZx_SDR_C_SAD_x
- RZx_SDR_C_PTR_S
- RZx_SDR_C_PTR_E
- RZx_SDR_C_OFT

When output is 4:2:0-C only, the following values are not needed:

- RZx_SDR_Y_BAD_x
- RZx_SDR_Y_SAD_x
- RZx_SDR_Y_PTR_S
- RZx_SDR_Y_PTR_E
- RZx_SDR_Y_OFT

8.3.4.4.2.1 ISS ISP RSZ Global Image Processing Settings – Subsequence 1

The procedure shown in Figure 8-252 determines which of the RSZ engines is enabled and the type of input data, and configures the source data parameters.

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Figure 8-252. ISS ISP RSZ Global Image Processing Settings – Subsequence 1

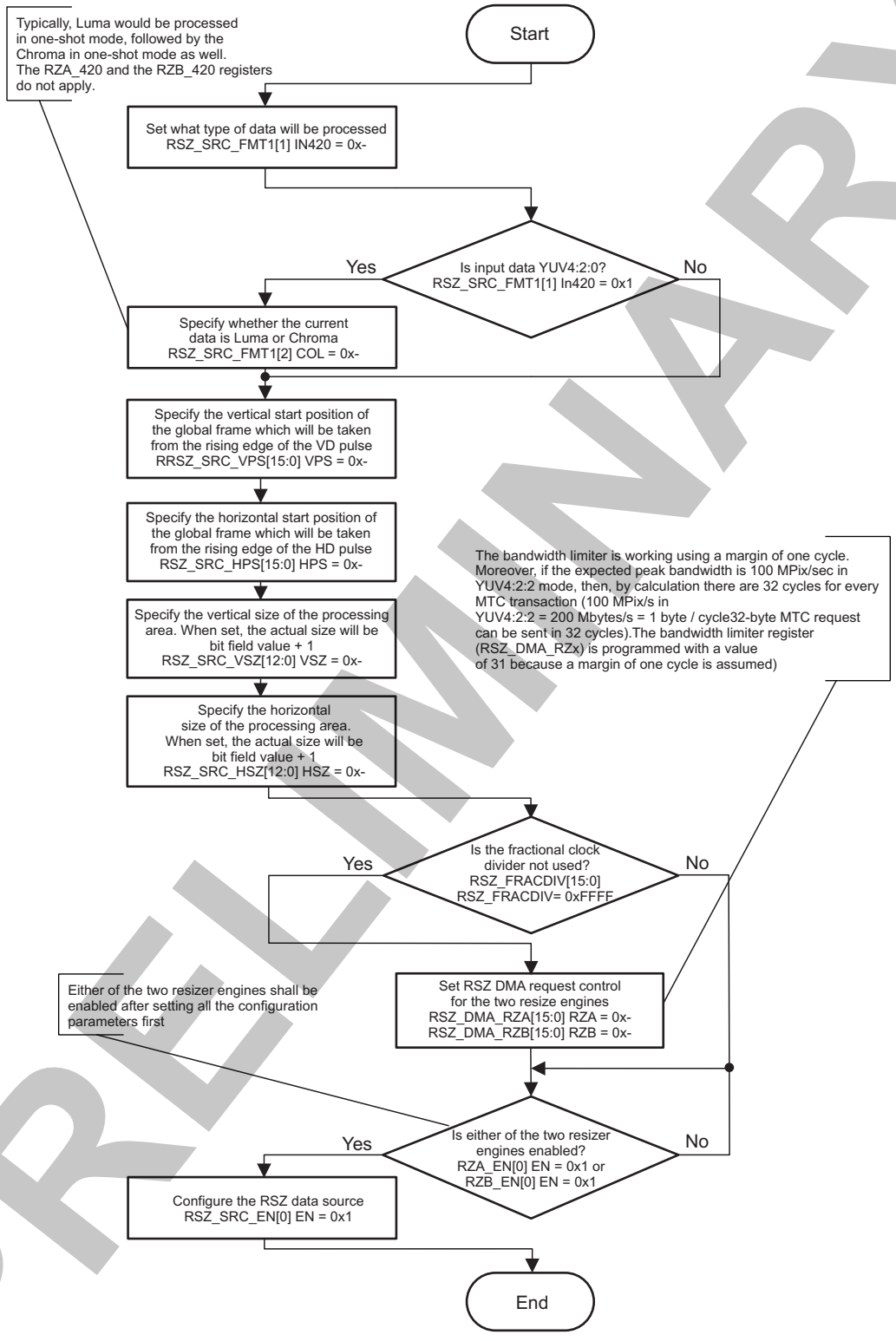

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Table 8-487. Register Call Summary for ISS ISP RSZ Global Image Processing Settings – Subsequence 1

Register Name	Register Name	Register Name
RZA_420[1] CEN	RZA_420[0] YEN	RSZ_SRC_FMT1[1] IN420
RZB_420[0] CEN	RZB_420[1] YEN	RSZ_SRC_FMT1[2] COL
RSZ_SRC_EN[0] EN	RSZ_SRC_VPS[15:0] VPS	RSZ_SRC_HPS[15:0] HPS
RSZ_SRC_VSZ[12:0] VSZ	RSZ_SRC_HSZ[12:0] HSZ	RSZ_FRACDIV[15:0] RSZ_FRACDIV
RSZ_DMA_RZA[15:0] RZA	RSZ_DMA_RZB[15:0] RZB	

8.3.4.4.2.2 ISS ISP RSZ Global Image Processing Settings – Subsequence 2

The procedure shown in Figure 8-253 determines the type of output data and whether it will be flipped. Then it configures the RSZ engines accordingly.

Figure 8-253. ISS ISP RSZ Global Image Processing Settings – Subsequence 2

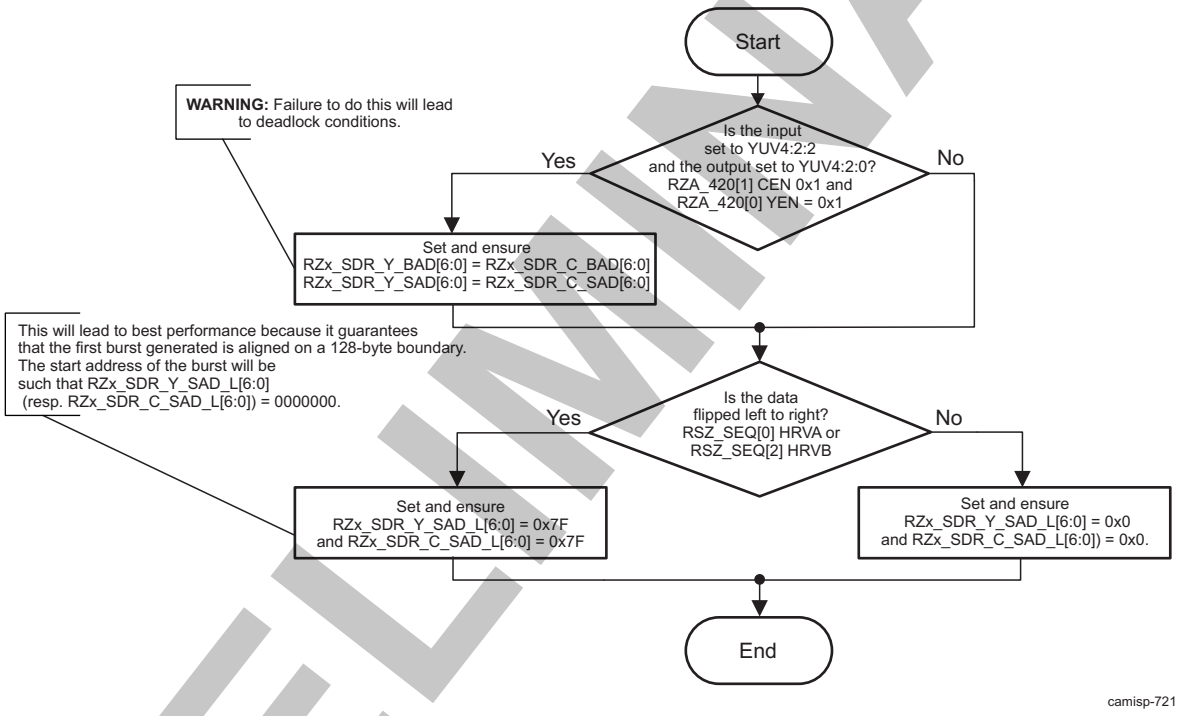

Table 8-488. Register Call Summary for ISS ISP RSZ Global Image Processing Settings – Subsequence 2

Register Name	Register Name	Register Name
RZA_420[1] CEN	RZA_420[0] YEN	RZB_420[1] CEN
RZB_420[0] YEN	RZA_SDR_Y_SAD_L	RZA_SDR_C_SAD_L
RZB_SDR_Y_SAD_L	RZB_SDR_C_SAD_L	RSZ_SEQ[0] HRVA
RSZ_SEQ[2] HRVB		

8.3.4.4.3 ISS ISP RSZ Engines Interframe Image Processing Settings

This section discusses the configuration of the RSZ interframe image processing. Table 8-489 identifies the setup sequence for the two different engines within the RSZ module.

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Table 8-489. ISS ISP RSZ Engines Interframe Image Processing Settings

Step	Register/Bit Field/Programming Model	Value
IF: Is the RSZ module set to free-running mode?	RSZ_SRC_MODE[0] OST	= 0x0
Set either of the engines to free-running mode to keep popping data out of the internal buffer. Otherwise, it will lead to an overflow event after the first frame.	RZA_MODE[0] MODE RZB_MODE[0] MODE	0x0
ELSE: Is the RSZ module set to one-shot mode?		
Set both resizer engines to one-shot mode.	RZA_MODE[0] MODE RZB_MODE[0] MODE	0x1
ENDIF		
Set the output format. See Table 8-434.	RZA_420[0] YEN RZA_420[1] CEN RZB_420[0] YEN RZB_420[1] CEN	0x-
On the side of the RSZ_SRC_VPS, RSZ_SRC_HPS, RSZ_SRC_VSZ, and RSZ_SRC_HSZ registers, set the engine complementary function to crop within the global frame and assign proper vertical start position (start line) of the input frame.(1)	RZA_I_VPS[12:0] VPS RZB_I_VPS[12:0] VPS	0x-
Assign proper horizontal start position (start pixel) of the input frame.	RZA_I_HPS[12:0] HPS RZB_I_HPS[12:0] HPS	0x-
Assign proper vertical size of the output frame.	RZA_O_VSZ[12:0] VPS RZB_O_VSZ[12:0] VPS	0x-
Assign proper horizontal size of the output frame.	RZA_O_HSZ[12:1] HPS RZB_O_HSZ[12:1] HPS	0x-
Set the phase position for the Chroma and Luma element and configure the averager.	See Section 8.3.4.4.3.1	
Set the vertical resize value for the two engines (vertical resize ration = 256 / RZx_V_DIF).	RZA_V_DIF[13:0] V RZB_V_DIF[13:0] V	0x-
Set the horizontal resize value for the two engines (horizontal resize ration = 256 / RZx_H_DIF).	RZA_H_DIF[13:0] H RZB_H_DIF[13:0] H	0x-
Select vertical method of resizing filtering (linear or cubic interpolation) for the Luma and Chroma elements.	RZA_V_TYP[0] Y RZB_V_TYP[0] Y RZA_V_TYP[1] C RZB_V_TYP[1] C	0x-
Select horizontal method of resizing filtering (linear or cubic interpolation) for the Luma and Chroma elements.	RZA_H_TYP[0] Y RZB_H_TYP[0] Y RZA_H_TYP[1] C RZB_H_TYP[1] C	0x-
IF: Is the interpolation method linear?	RZx_V_TYP[0] Y and RZx_V_TYP[1] C RZx_H_TYP[0] Y and RZx_H_TYP[1] C	= 0x1
Set the needed vertical LPF intensity for the Luma and Chroma elements.	RZA_V_LPF[5:0] Y RZA_V_LPF[11:6] C RZB_V_LPF[5:0] Y RZB_V_LPF[11:6] C	0x-
Set the needed horizontal LPF intensity for the Luma and Chroma elements.	RZA_H_LPF[5:0] Y RZA_H_LPF[11:6] C RZB_H_LPF[5:0] Y RZB_H_LPF[11:6] C	0x-
ENDIF		
Set the Chroma saturation MAX and MIN values.	RSZ_YUV_C_MAX[7:0] MAX RSZ_YUV_C_MIN[7:0] MIN	0x-
Set the Luma saturation MAX and MIN values.	RSZ_YUV_Y_MAX[7:0] MAX RSZ_YUV_Y_MIN[7:0] MIN	0x-

(1) The size of the frame (height of the image) after the cropping must be two lines or larger.

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Table 8-489. ISS ISP RSZ Engines Interframe Image Processing Settings (continued)

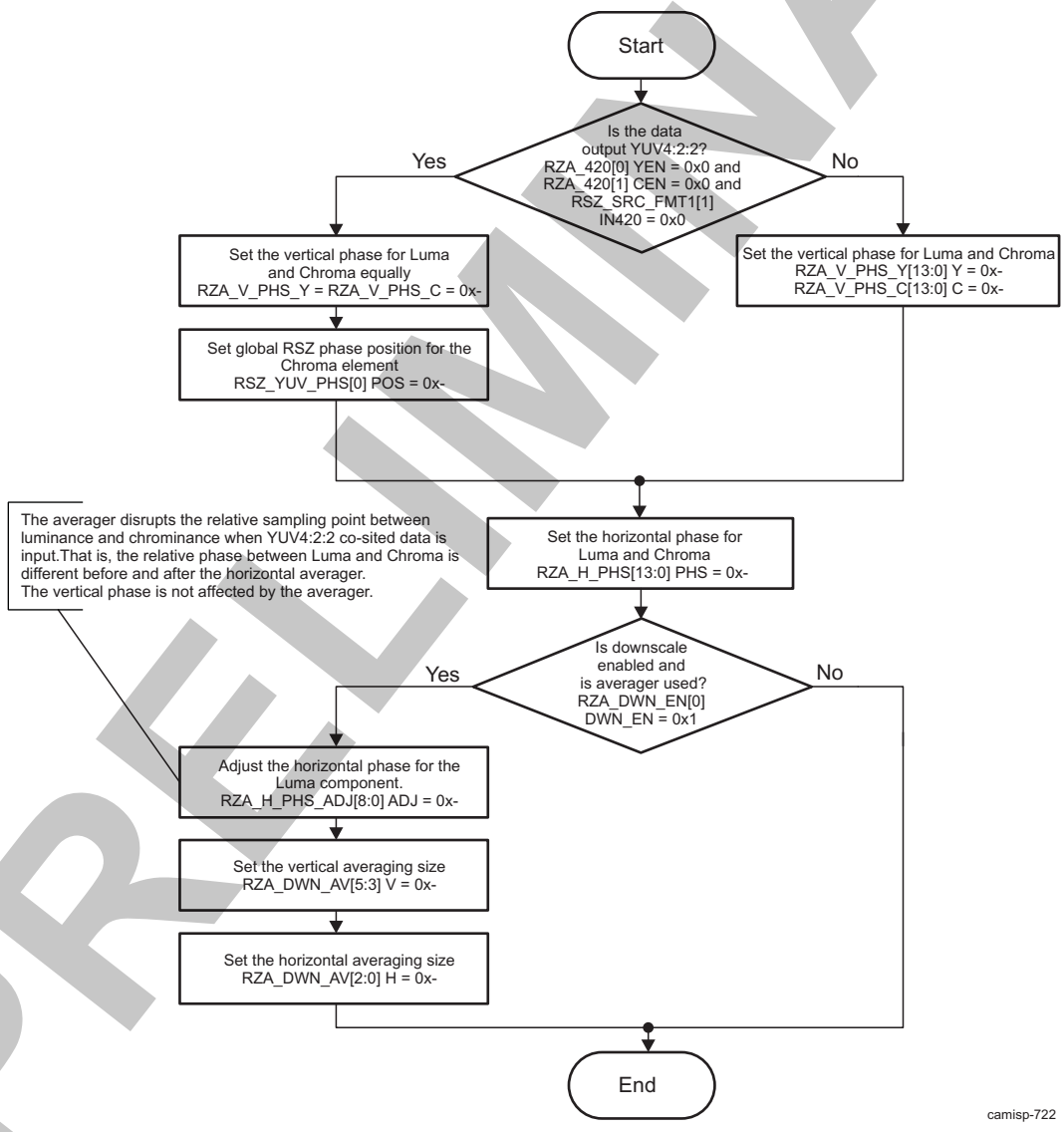
Step	Register/Bit Field/Programming Model	Value
(optional) Set the mode to RGB conversion, configure the alpha value, and set additional pixel masking.	See Section 8.3.4.4.3.2.	

8.3.4.4.3.1 ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1

The procedure shown in Figure 8-254 sets the phase position for the Chroma and Luma elements and configures the averager.

NOTE: This procedure configures RSZ-A. The procedure for RSZ-B is identical.

Figure 8-254. ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1



NOTE: When masking is used, boundaries affect the leftmost/rightmost 2 pixels in up-conversion.

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Table 8-490. Register Call Summary for ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1

Register Name	Register Name	Register Name
RZA_420[0] YEN	RZA_420[1] CEN	RSZ_SRC_FMT1[1] IN420
RZA_V_PHS_Y	RZA_V_PHS_C	RSZ_YUV_PHS[0] POS
RZA_V_PHS_Y[13:0] Y	RZA_V_PHS_C[13:0] C	RZA_H_PHS [13:0] PHS
RZA_DWN_EN[0] DWN_EN	RZA_H_PHS_ADJ[8:0] ADJ	RZA_DWN_AV[5:3] V
RZA_DWN_AV[2:0] H		

8.3.4.4.3.2 ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2

The procedure shown in Figure 8-255 sets the mode to RGB conversion, configures the alpha value, and sets additional pixel masking.

NOTE: This procedure configures RSZ-A. The procedure for RSZ-B is identical.

Figure 8-255. ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2

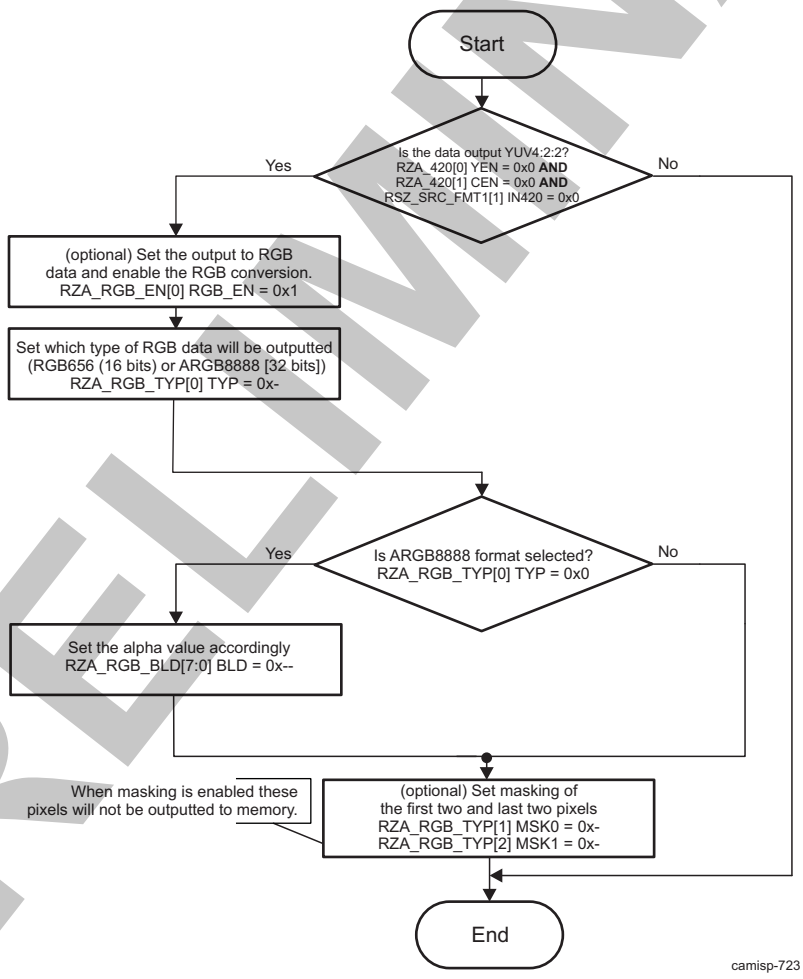

Table 8-491. Register Call Summary for ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2

Register Name	Register Name	Register Name
RZA_420[0] YEN	RZA_420[1] CEN	RSZ_SRC_FMT1[1] IN420

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Table 8-491. Register Call Summary for ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2 (continued)

Register Name	Register Name	Register Name
RZA_RGB_EN[0] RGB_EN	RZA_RGB_TYP[0] TYP	RZA_RGB_BLD[7:0] BLD
RZA_RGB_TYP[1] MSK0	RZA_RGB_TYP[2] MSK1	

8.3.4.4.4 ISS ISP RSZ Programming Constraints

The RSZ module contains shadowed and nonshadowed registers. Shadowed registers can be updated anytime during the resizing operation, but the new setting does not take effect until the next rsz_int_reg event. Shadowed registers can be updated for the next frame after the rsz_int_reg event triggers.

Nonshadowed registers must be programmed before enabling the RSZ module or between frames (that is, after the rsz_int_dma and the entire frame have come on the VPORT interface, and before the VD of the next frame). Table 8-492 lists the nonshadowed registers.

Table 8-492. ISS ISP RSZ Nonshadowed Registers

Nonshadowed Registers
RSZ_SYSCONFIG
RSZ_IN_FIFO_CTRL
RSZ_GCK_MMR
RSZ_GCK_SDR
RSZ_SRC_MODE
RSZ_SRC_FMT0
RSZ_SRC_VPS
RSZ_SRC_HPS
RSZ_SRC_EN

8.3.4.5 ISS ISP H3A Programming Model

This section discusses issues related to the software control of the H3A module. It lists the registers that must be programmed in different modes, how to enable and disable the H3A, how to check the status of the H3A, discusses the different register access types, and enumerates several programming constraints.

8.3.4.5.1 ISS ISP H3A Hardware Setup/Initialization

This section discusses the configuration of the H3A required before image processing can begin.

8.3.4.5.1.1 ISS ISP H3A Reset Behavior

Upon hardware reset of the ISP, all the registers in the H3A are reset to their reset values.

8.3.4.5.1.2 ISS ISP H3A Register Setup

For register configuration purposes, the AF and AEW engines of the H3A can be configured independently. Because there are separate enable bits for each engine, this section is divided into the AF engine and the AEW engine.

8.3.4.5.1.2.1 ISS ISP H3A AF Engine

Before enabling the AF engine, the hardware must be properly configured through register writes. Table 8-493 lists the register parameters that must be programmed before enabling the AF engine of the H3A.

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Table 8-493. ISS ISP H3A AF Engine Required Configuration Parameters

Step	Configuration Required	Value
AF optional preprocessing settings		
Note: A suggestion is to use the averaging filter in the IPIPEIF to reduce noise before generating AF statistics.		
Enable or disable the median filter.	H3A_PCR[2] AF_MED_EN	
Set the median filter threshold, if the filter is enabled.	H3A_PCR[10:3] MED_TH	
Enable or disable A-Law compression.	H3A_PCR[1] AF_ALAW_EN	
Set AF general settings.		
Set the focus value accumulation mode.	H3A_PCR[14] FVMODE	
Set the input start information.	H3A_LINE_START[31:16] SLV H3A_LINE_START[15:0] LINE_START	
Set the output SDRAM destination start address.	H3A_AFBUFST[31:5] AFBUFST	
RGB pixel extraction and paxel settings		
Set the RGB positions in the pixel.	H3A_PCR[13:11] RGBPOS	
Set the paxel width.	H3A_AFPAX1[23:16] PAXW	
Set the paxel height.	H3A_AFPAX1[7:0] PAXH	
Set the paxel horizontal start position.	H3A_AFPAXSTART[27:16] PAXSH	
Set the paxel vertical start position.	H3A_AFPAXSTART[11:0] PAXSV	
Set the column increment.	H3A_AFPAX2[20:17] AFINCH	
Set the line increment.	H3A_AFPAX2[16:13] AFINCV	
Set the vertical paxel count.	H3A_AFPAX2[12:6] PAXVC	
Set the horizontal paxel count.	H3A_AFPAX2[5:0] PAXHC	
Horizontal focus value calculator settings		
Set the horizontal threshold for the two IIR.	H3A_HVF_THR[31:16] HTHR2 H3A_HVF_THR[15:0] HTHR1	
Set the IIR horizontal start position.	H3A_AFIIRSH[11:0] IIRSH	
Set the coefficients for the SET 0 IIR.	H3A_AFCOEF010 H3A_AFCOEF032 H3A_AFCOEF054 H3A_AFCOEF076 H3A_AFCOEF098 H3A_AFCOEF0010	
Set the coefficients for the SET 1 IIR.	H3A_AFCOEF110 H3A_AFCOEF132 H3A_AFCOEF154 H3A_AFCOEF176 H3A_AFCOEF198 H3A_AFCOEF1010	
Vertical focus value calculator settings		
Enable or disable vertical AF focus value calculation.	H3A_PCR[20] AF_VF_EN	
Set the vertical FIR 1 coefficients and threshold.	H3A_VFV_CFG1 H3A_VFV_CFG2	
Set the vertical FIR 2 coefficients and threshold.	H3A_VFV_CFG3 H3A_VFV_CFG4	

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The following references offer guidelines on how to program the filter coefficients and make use of the H3A output.

- V. Peddigari, M. Gamadia, and N. Kehtarnavaz, *Real-time implementation issues in passive automatic focusing for digital still cameras*, Journal of Imaging Science and Technology, vol. 49, no. 2, pp. 114–123, Mar/Apr 2005.
- M. Gamadia and N. Kehtarnavaz, *A real-time continuous automatic focus algorithm for digital cameras*, in Proceedings of IEEE Southwest Symposium on Image Analysis and Interpretation 2006, pp. 163–167, Mar. 2006.
- M. Gamadia, N. Kehtarnavaz, and K. Roberts-Hoffman, *Low-light auto-focus enhancement for digital and cell-phone camera image pipelines*, IEEE Transactions on Consumer Electronics, vol. 53, no. 2, pp. 249–257, May 2007.

8.3.4.5.1.2.2 ISS ISP H3A AEW Engine

Before enabling the AEW engine, the hardware must be properly configured through register writes. Table 8-494 lists the register parameters that must be programmed before enabling the AEW engine of the H3A.

Table 8-494. ISS ISP H3A AEW Engine Required Configuration Parameters

Step	Configuration Required	Value
AEW optional preprocessing settings		
Enable or disable the median filter.	H3A_PCR[19] AEW_MED_EN	
Set the median filter threshold.	H3A_PCR[10:3] MED_TH	
Enable or disable A-Law compression.	H3A_PCR[17] AEW_ALAW_EN	
Set AEW general settings.		
Set the saturation limit.	H3A_PCR[31:22] AVE2LMT	
Set the AE/AWB output format.	H3A_AEWCFG[9:8] AEFMT	
Set the AE/AWB shift value for sum of pixels.	H3A_AEWCFG[3:0] SUMFST	
Set the input start information.	H3A_LINE_START[31:16] SLV H3A_LINE_START[15:0] LINE_START	
Set the output SDRAM destination start address.	H3A_AEWBUFST[31:5] AEWBUFST	
Set the AE/AWB window configuration settings.		
Set the window width (in pixels).	H3A_AEWWIN1[20:13] WINW	
Set the window height (in lines).	H3A_AEWWIN1[31:24] WINH	
Set the window count for horizontal direction.	H3A_AEWWIN1[5:0] WINHC	
Set the window count for vertical direction.	H3A_AEWWIN1[12:6] WINVC	
Set the window start position H.	H3A_AEWINSTART[11:0] WINSH	
Set the window start position V.	H3A_AEWINSTART[27:16] WINSV	
Set the horizontal distance between subsamples.	H3A_AEWSUBWIN[3:0] AEWINCH	
Set the vertical distance between subsamples.	H3A_AEWSUBWIN[11:8] AEWINCV	
Set the vertical start position for single black line of windows.	H3A_AEWINBLK[27:16] WINSV	
Set the height for the single black line of windows.	H3A_AEWINBLK[6:0] WINH	

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8.3.4.5.2 ISS ISP H3A Enable/Disable Hardware

Setting the H3A_PCR[0] AF_EN bit enables the AF engine, and setting the H3A_PCR[16] AEW_EN bit enables the AEW engine. This is done after all of the required registers discussed in the previous section are programmed.

The H3A operates in continuous mode. Processing of the frame is dependent on the timing of the IPIPEIF. To ensure that data from the IPIPEIF is not missed, the H3A must be enabled before the IPIPEIF. In this way, the H3A waits for data from the IPIPEIF. The AF engine or the AEW engine can be disabled by clearing the H3A_PCR[0] AF_EN or H3A_PCR[16] AEW_EN bit, respectively, during the processing of the last frame. The disable is latched in at the end of the frame in which it was written.

8.3.4.5.3 ISS ISP H3A Register Accessibility During Frame Processing

There are two types of register accesses in the H3A module:

- Shadow registers

  These registers/fields can be read and written (if the field is writable) at any time. However, the written values take effect only at the start of a frame. Reads still return the most-recent write even though the settings are not used until the next start of frame.

  The only shadowed registers in the H3A module are:

  – H3A_AFPAX1
  – H3A_AFPAX2
  – H3A_AFPAXSTART
  – H3A_AFIIRSH
  – H3A_AEWWIN1
  – H3A_AEWINSTART
  – H3A_AEWINBLK
  – H3A_AEWSUBWIN
  – H3A_AEWCFG
  – H3A_AEWBUFST

- Busy-lock registers

  All other registers, except those described previously, belong to this category.

  Busy-lock registers cannot be written when the module is busy (H3A_PCR[15] BUSYAF == 1 or H3A_PCR[18] BUSYAEAWB == 1). Writes are allowed to occur, but no change occurs in the registers (blocked writes from the hardware perspective, but allowed write from the software perspective). Once the busy bit in the H3A_PCR register (H3A_PCR[15] BUSYAF or H3A_PCR[18] BUSYAEAWB bit) is reset to 0, the busy-lock registers can be written.

The ideal procedure for changing the H3A registers if (H3A_PCR[15] BUSYAF == 0 or H3A_PCR[18] BUSYAEAWB == 0) or if (EOF interrupt occurs) is:

1. Disable AF or AE/AWB.
2. Change registers.
3. Enable AF or AE/AWB.

8.3.4.5.4 ISS ISP H3A Interframe Operations

Between frames, it may be necessary to modify the memory pointers before processing the next frame. Because the H3A_PCR register and memory pointer registers are shadowed, these modifications can take place any time before the end of the frame, and the data will be latched in for the next frame. The host controller can perform these changes upon receiving an interrupt.

8.3.4.5.5 ISS ISP H3A Summary of Constraints

Adhere to the following list of register configuration constraints when programming the H3A. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

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- The output addresses (H3A_AFBUFST[31:5] AFBUFST) must be on 64-byte boundaries.
- Each horizontal row of paxels () or windows () starts on a 32-byte boundary.
- If the pixel clock frequency is less than ISP_FCLK / 2 and vertical focus is enabled, the constraints listed in Table 8-495 apply.

Table 8-495. ISS ISP H3A Constraints When PCLK < ISP_FCLK / 2 and Vertical Focus Enabled

Field	Constraint
H3A_AEWWIN1[20:13] WINW	>7
H3A_AFPAX1[23:16] PAXW	>7
H3A_AFIIRSH[11:0] IIRSH	None
H3A_AFPAXSTART[27:16] PAXSH	>= H3A_AFIIRSH[11:0] IIRSH + 2
H3A_AFPAX2[20:17] AFINCH	None
H3A_AFPAX2[5:0] PAXHC	<=11

- If the pixel clock frequency is less than ISP_FCLK / 2 and vertical focus is disabled, the constraints listed in Table 8-496 apply.

Table 8-496. ISS ISP H3A Constraints When PCLK < ISP_FCLK / 2 and Vertical Focus Disabled

Field	Constraint
H3A_AEWWIN1[20:13] WINW	>7
H3A_AFPAX1[23:16] PAXW	>7
H3A_AFIIRSH[11:0] IIRSH	Must be even
H3A_AFPAXSTART[27:16] PAXSH	>= H3A_AFIIRSH[11:0] IIRSH + 2 and must be even
H3A_AFPAX2[20:17] AFINCH	(1+ H3A_AFPAX1[23:16] PAXW / H3A_AFPAX2[20:17] AFINCH) * H3A_AFPAX2[5:0] PAXHC must be between 4 and 384
H3A_AFPAX2[5:0] PAXHC	<=35

- If the pixel clock frequency is greater than or equal to ISP_FCLK / 2 and vertical focus is enabled, the constraints listed in Table 8-497 apply.

Table 8-497. ISS ISP H3A Constraints When PCLK >= ISP_FCLK / 2 and Vertical Focus Enabled

Field	Constraint
H3A_AEWWIN1[20:13] WINW	>15
H3A_AFPAX1[23:16] PAXW	>15
H3A_AFIIRSH[11:0] IIRSH	None
H3A_AFPAXSTART[27:16] PAXSH	>= H3A_AFIIRSH[11:0] IIRSH + 2
H3A_AFPAX2[20:17] AFINCH	None
H3A_AFPAX2[5:0] PAXHC	<= 11

- If the pixel clock frequency is greater than or equal to ISP_FCLK / 2 and vertical focus is disabled, the constraints in Table 8-498 apply.

Table 8-498. ISS ISP H3A Constraints When PCLK >= ISP_FCLK / 2 and Vertical Focus Disabled

Field	Constraint
H3A_AEWWIN1[20:13] WINW	>15
H3A_AFPAX1[23:16] PAXW	>15
H3A_AFIIRSH[11:0] IIRSH	Must be even
H3A_AFPAXSTART[27:16] PAXSH	>= H3A_AFIIRSH[11:0] IIRSH + 2 and must be even
H3A_AFPAX2[20:17] AFINCH	(1 + H3A_AFPAX1[23:16] PAXW / H3A_AFPAX2[20:17] AFINCH) * H3A_AFPAX2[5:0] PAXHC must be between 4 and 384 and H3A_AFPAX2[20:17] AFINCH modulo H3A_AFPAX1[23:16] PAXW !=1

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Table 8-498. ISS ISP H3A Constraints When PCLK >= ISP_FCLK / 2 and Vertical Focus Disabled (continued)

Field	Constraint
H3A_AFPAX2[5:0] PAXHC	<= 35

AF engine

- The paxel horizontal start value must be greater than or equal to the IIR horizontal start position.
- The paxel start/end and IIR filter start positions must not be set within the first 2 and the last 2 pixels (to check).
- The width (H3A_AFPAX1[23:16] PAXW) and height (H3A_AFPAX1[7:0] PAXH) of the paxels must be an even number.
- The minimum width of the paxel (H3A_AFPAX1[23:16] PAXW) must be 16 pixels, if pixel clock is half or less of the ISP_FCLK clock. If pixel clock is equal to ISP_FCLK, then the minimum width is 32 pixels.
- The value of H3A_AFPAX2[20:17] AFINCH bit-field should be higher than 0, irrespective of the ratio of the pixel clock to the ISP_FCLK.
- The number of columns to increment in a paxel (H3A_AFPAX2[20:17] AFINCH) must be even and is restricted to 2 to 32.
- The number of lines to increment in a paxel (H3A_AFPAX2[16:13] AFINCV) must be even and is restricted to 0 to 30.
- The maximum number of vertical paxels in a frame (H3A_AFPAX2[12:6] PAXVC) must not exceed 128.
- The number of paxels in the horizontal direction (H3A_AFPAX2[5:0] PAXHC) has a valid range from 1 to 35.
- If vertical mode is enabled:
  - The paxel horizontal start position (H3A_AFPAXSTART[27:16] PAXSH) must be even.
  - The lower bit of the H3A_AFPAXSTART[27:16] PAXSH bit field and the lower bit of the H3A_AFIIRSH[11:0] IIRSH bit field must be equal.
  - The H3A_AFPAXSTART[11:0] PAXSV bit field must be >= 8.
- If vertical mode is not enabled, the H3A_AFIIRSH[11:0] IIRSH bit field must be even.
- Paxels cannot overlap the last pixel in a line.
- Paxels must be adjacent to one another.

AEW engine

- The width (H3A_AEWWIN1[20:13] WINW) and height (H3A_AEWWIN1[31:24] WINH) of the windows must be an even number.
- The minimum width of the window (H3A_AEWWIN1[20:13] WINW) must be 16 pixels, if the pixel clock is half or less of the ISP_FCLK clock. If the pixel clock is equal to ISP_FCLK, then the minimum width is 32 pixels.
- The window height (H3A_AEWWIN1[31:24] WINH) has a valid range from 2 to 512.
- The maximum number of vertical windows in a frame (H3A_AEWWIN1[12:6] WINVC) must not exceed 128.
- The number of horizontal windows (H3A_AEWWIN1[5:0] WINHC) has a valid range from 1 to 35.
- The vertical and horizontal window start position (H3A_AEWWINSTART) has a valid range from 0 to 4095.
- The vertical window start position for single black lines (H3A_AEWINBLK[27:16] WINSV) has a valid range from 0 to 4095.
- The horizontal window start position for single black lines (H3A_AEWINBLK[6:0] WINH) must be even and has a valid range from 2 to 256.
- The subsampling windows can start only on even numbers.

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- The vertical and horizontal sampling point increment (H3A_AEWSUBWIN) has a valid range from 2 to 32.

8.3.4.6 ISS ISP BL Programming Model

The procedure listed in Table 8-499 initializes the buffer logic.

Table 8-499. ISS ISP BL Settings

Step	Register/Bit Field/Programming Model	Value
Set the memory access priority registers.	ISP5_MPSR	
Set the minimum interval between two memory requests for ISIF read port.	ISP5_BL_MTC_1[31:16] ISIF_R	
Set the minimum interval between two memory requests for IPIPEIF read port.	ISP5_BL_MTC_1[15:0] IPIPEIF_R	
Set the minimum interval between two memory requests for H3A write port.	ISP5_BL_MTC_1[31:16] H3A_W	
Set the maximum number of CIDs/tags that the BL can use.	ISP5_CTRL[7:4] VBUSM_CIDS	
Set the BL VBUSM priority setting.	ISP5_CTRL[3:1] VBUSM_CPRIORITY	
Set write-posted/nonposted.	ISP5_CTRL[0] OCP_WRNP	
Enable the BL clock.	ISP5_CTRL[15] BL_CLK_ENABLE	0x1

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8.3.5 ISS ISP Register Manual

8.3.5.1 ISS ISP Instance Summary

Table 8-500. ISS ISP Instance Summary

Module Name	Module Base Address	Size
ISS_ISP5_SYS1	0x5201 0000	160 bytes
ISS_ISP5_SYS2	0x5201 00A0	864 bytes
ISS_RESIZER	0x5201 0400	1 KiB
ISS_IPIPE	0x5201 0800	2 KiB
ISS_ISIF	0x5201 1000	512 bytes
ISS_IPIPEIF	0x5201 1200	128 bytes
ISS_H3A	0x5201 1400	512 bytes

8.3.5.2 ISS ISP5 SYS1 Registers

8.3.5.2.1 ISS ISP5 SYS1 Register Summary

Table 8-501. ISS ISP5 SYS1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISP5_SYS1 Base Address
ISP5_REVISION	R	32	0x0000 0000	0x5201 0000
ISP5_HWINFO1	R	32	0x0000 0004	0x5201 0004
ISP5_HWINFO2	R	32	0x0000 0008	0x5201 0008
ISP5_SYSCONFIG	RW	32	0x0000 0010	0x5201 0010
RESERVED	RW	32	0x0000 0020	0x5201 0020
ISP5_IRQSTATUS_RAW_i (1)	RW	32	0x0000 0024 + (0x10 * i)	0x5201 0024 + (0x10 * i)
ISP5_IRQSTATUS_i (1)	RW	32	0x0000 0028 + (0x10 * i)	0x5201 0028 + (0x10 * i)
ISP5_IRQENABLE_SET_i (1)	RW	32	0x0000 002C + (0x10 * i)	0x5201 002C + (0x10 * i)
ISP5_IRQENABLE_CLR_i (1)	RW	32	0x0000 0030 + (0x10 * i)	0x5201 0030 + (0x10 * i)
ISP5_DMAENABLE_SET	RW	32	0x0000 0064	0x5201 0064
ISP5_DMAENABLE_CLR	RW	32	0x0000 0068	0x5201 0068
ISP5_CTRL	RW	32	0x0000 006C	0x5201 006C
RESERVED	R	32	0x0000 0070	0x5201 0070
RESERVED	R	32	0x0000 0074	0x5201 0074
RESERVED	R	32	0x0000 0078	0x5201 0078
ISP5_MPSR	RW	32	0x0000 007C	0x5201 007C
ISP5_BL_MTC_1	RW	32	0x0000 0080	0x5201 0080
ISP5_BL_MTC_2	RW	32	0x0000 0084	0x5201 0084
ISP5_BL_VBUSM	RW	32	0x0000 0088	0x5201 0088

(1) i = 0 to 3

8.3.5.2.2 ISS ISP5 SYS1 Register Description

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Table 8-502. ISP5_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5201 0000	**Instance**	ISS_ISP5_SYS1
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See[(1)]

(1) TI internal data

Table 8-503. Register Call Summary for Register ISP5_REVISION

ISS ISP

- ISS ISP5 SYS1 Register Summary: [0]

Table 8-504. ISP5_HWINFO1

Address Offset	0x0000 0004		
Physical Address	0x5201 0004	**Instance**	ISS_ISP5_SYS1
Description	GENERIC PARAMETER REGISTER Information about the hardware configuration of the IP module.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ISIF_RFM_LINE_SIZE								RESERVED								IPIPE_LINE_SIZE							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	ISIF_RFM_LINE_SIZE	Memory line size for the data reformatter in the ISIF module.	R	0x1500
15:13	RESERVED		R	0x0
12:0	IPIPE_LINE_SIZE	Memory line size for the IPIPE module	R	0x1500

Table 8-505. Register Call Summary for Register ISP5_HWINFO1

ISS ISP

- ISS ISP5 SYS1 Register Summary: [0]

Table 8-506. ISP5_HWINFO2

Address Offset	0x0000 0008		
Physical Address	0x5201 0008	**Instance**	ISS_ISP5_SYS1
Description	GENERIC PARAMETER REGISTER Information about the hardware configuration of the IP module.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			H3A_LINE_SIZE												

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	H3A_LINE_SIZE	Memory line size for the H3A module	R	0x0BC0

Table 8-507. Register Call Summary for Register ISP5_HWINFO2

ISS ISP
- ISS ISP5 SYS1 Register Summary: [0]

Table 8-508. ISP5_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5201 0010	**Instance**	ISS_ISP5_SYS1
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		RESERVED		SOFTRESET	AUTO_IDLE

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x3: Reserved 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. IP module must not generate (initiator-related) wake-up events. Generation of the MStandby signal must be initiated by the firmware by writing ISP5_CTRL.MSTANDBY = 1.	RW	0x2
3:2	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
1	SOFTRESET	Software reset. The soft reset will cause the MStandby to be asserted as the reset value of the ISP5_CTRL.MSTANDBY bit is 1. After a soft reset, the software must ensure not to perform any access for 16 clock cycles (OCP-slave port frequency) after writing this bit. The OCP slave port is running at half the frequency of the functional clock. Before issuing a soft reset, the software must ensure that no more traffic is being generated by the ISP. Basically, it means that the camera module must be stopped from sending data and/or that the ISP modules are disabled. The last interrupt triggered by the ISP design upon completion of the frame processing is rsz_int_dma. This rsz_int_dma event must be used to enable clean termination of the processing. The software must wait a few hundred cycles to trigger the soft reset after upon assertion of the rsz_int_dma, this is to ensure that the BL is completely drained. Software must set the ISP in standby mode before issuing the soft reset: Set ISP5_SYSCONFIG.STANDBYMODE = 2 (smart standby). Set ISP5_CTRL.MSTANDBY to 1. Poll for ISP5_CTRL.MSTANDBY_WAIT = 1. Then, the soft reset can be applied (ISP5_SYSCONFIG.SOFTRESET = 1). Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0
0	AUTO_IDLE	Auto clock gating. Always enabled.	R	1

Table 8-509. Register Call Summary for Register ISP5_SYSCONFIG

ISS ISP

- ISS ISP Reset: [0] [1] [2]
- ISS ISP IPIPEIF Reset Behavior: [3]
- ISS ISP RSZ Reset Behavior: [4] [5] [6]
- ISS ISP5 SYS1 Register Summary: [7]
- ISS ISP5 SYS1 Register Description: [8] [9]

Table 8-510. ISP5_IRQSTATUS_RAW_i

Address Offset	0x0000 0024 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 0024 + (0x10 * i)	**Instance**	ISS_ISP5_SYS1
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug. The ISP outputs four interrupt lines, ISP_IRQ0 to ISP_IRQ3. Any internal ISP event can be merged on the four lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCP_ERR_IRQ	RESERVED	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	RESERVED	IPIPE_INT_EOF	H3A_INT_EOF	RSZ_INT_EOF1	RSZ_INT_EOF0	RESERVED		RSZ_FIFO_IN_BLK_ERR	RSZ_FIFO_OVF	RSZ_INT_CYC_RZB	RSZ_INT_CYC_RZA	RSZ_INT_DMA	RSZ_INT_LAST_PIX	RSZ_INT_REG	H3A_INT	AF_INT	AEW_INT	IPIPEIF_IRQ	IPIPE_INT_HST	IPIPE_INT_BSC	IPIPE_INT_DMA	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT_3	ISIF_INT_2	ISIF_INT_1	ISIF_INT_0

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Bits	Field Name	Description	Type	Reset
31	OCP_ERR_IRQ	An OCP error has been received on the ISP master port. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
30	RESERVED		R	0
29	IPIPE_INT_DPC_RNEW1	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
28	IPIPE_INT_DPC_RNEW0	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
27	IPIPE_INT_DPC_INI	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
26	RESERVED		R	0
25	IPIPE_INT_EOF	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
24	H3A_INT_EOF	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
23	RSZ_INT_EOF1	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer B engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
22	RSZ_INT_EOF0	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer A engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
21:20	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
19	RSZ_FIFO_IN_BLK_ERR	This event signals that the minimum vertical blanking period has not been respected causing errors in the input data buffering submodule. This event will be triggered when the rsz_int_reg event of frame N is triggered before the rsz_int_dma of frame N + 1. This event would typically happen at the transition between two frames because there is not enough vertical blanking between frames: the firmware must take care to ensure enough vertical blanking. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
18	RSZ_FIFO_OVF	This event signals that overflow happened in the input data buffering submodule. This event would typically happen while processing a frame because the video port pixel clock is too high: the firmware must take care to use a lower pixel clock at the input of the resizer module. Depending on the mode being used, the overflow can happen at different places: 1. Bypass mode: overflow happened in the input circular buffer. 2. Pass through mode: overflow happened on the module output interface (MTC) 3. Normal resize mode: overflow happened in the input circular buffer. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
17	RSZ_INT_CYC_RZB	RESIZER module event: This event is the circular interrupt for RESIZER #B. An event can be triggered every time that RSZ_IRQ_RZB output lines have been written out to the RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value should be such that the circular buffer vertical size (set by the RZB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZB. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
16	RSZ_INT_CYC_RZA	RESIZER module event: This event is the circular interrupt for RESIZER #A. An event can be triggered every time that RSZ_IRQ_RZA output lines have been written out to the RZA_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, the circular buffer vertical size (set by the RZA_SDR_Y_PTR_E register) should be a multiple of RSZ_IRQ_RZA. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
15	RSZ_INT_DMA	This event is triggered when the last EOF (of the two MTC interfaces) is sent out to the BL and that the resizer core has returned to idle. rsz_int_dma is a true indication that all processing is finished for the particular frame on both resizer engines. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
14	RSZ_INT_LAST_PIX	This event is triggered when the last pixel of the valid area is received. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
13	RSZ_INT_REG	This event is triggered when the first pixel of the valid area is received. Shadowed registers can be updated at any time but the new value will take effect on the next rsz_int_reg event. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
12	H3A_INT	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
11	AF_INT	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
10	AEW_INT	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
9	IPIPEIF_IRQ	IPIPEIF module interrupt Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
8	IPIPE_INT_HST	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
7	IPIPE_INT_BSC	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
6	IPIPE_INT_DMA	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
5	IPIPE_INT_LAST_PIX	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
4	IPIPE_INT_REG	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
3	ISIF_INT_3	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
2	ISIF_INT_2	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
1	ISIF_INT_1	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
0	ISIF_INT_0	Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

Table 8-511. Register Call Summary for Register ISP5_IRQSTATUS_RAW_i

ISS ISP

- ISS ISP5 SYS1 Register Summary: [0]

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Table 8-512. ISP5_IRQSTATUS_i

Address Offset	0x0000 0028 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 0028 + (0x10 * i)	**Instance**	ISS_ISP5_SYS1
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). The ISP outputs four interrupt lines, ISP_IRQ0 to ISP_IRQ3. Any internal ISP event can be merged on the four lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCP_ERR_IRQ	RESERVED	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	RESERVED	IPIPE_INT_EOF	H3A_INT_EOF	RSZ_INT_EOF1	RSZ_INT_EOF0	RESERVED		RSZ_FIFO_IN_BLK_ERR	RSZ_FIFO_OVF	RSZ_INT_CYC_RZB	RSZ_INT_CYC_RZA	RSZ_INT_DMA	RSZ_INT_LAST_PIX	RSZ_INT_REG	H3A_INT	AF_INT	AEW_INT	IPIPEIF_IRQ	IPIPE_INT_HST	IPIPE_INT_BSC	IPIPE_INT_DMA	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT_3	ISIF_INT_2	ISIF_INT_1	ISIF_INT_0

Bits	Field Name	Description	Type	Reset
31	OCP_ERR_IRQ	An OCP error has been received on the ISP master port. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
30	RESERVED		R	0
29	IPIPE_INT_DPC_RNEW1	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
28	IPIPE_INT_DPC_RNEW0	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
27	IPIPE_INT_DPC_INI	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
26	RESERVED		R	0
25	IPIPE_INT_EOF	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
24	H3A_INT_EOF	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
23	RSZ_INT_EOF1	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer B engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
22	RSZ_INT_EOF0	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer A engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
21:20	RESERVED		R	0x0
19	RSZ_FIFO_IN_BLK_ERR	This event signals that the minimum vertical blanking period has not been respected causing errors in the input data buffering submodule. This event will be triggered when the rsz_int_reg event of frame N is triggered before the rsz_int_dma of frame N + 1. This event would typically happen at the transition between two frames because there is not enough vertical blanking between frames: the firmware must take care to ensure enough vertical blanking. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
18	RSZ_FIFO_OVF	This event signals that overflow happened in the input data buffering submodule or in the RSZ output interface. This event would typically happen while processing a frame because the video port pixel clock is too high: the firmware must take care to use a lower pixel clock at the input of the resizer module. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
17	RSZ_INT_CYC_RZB	RESIZER module event: This event is the circular interrupt for RESIZER #B. An event can be triggered every time that RSZ_IRQ_RZB output lines have been written out to the RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value should be such that the circular buffer vertical size (set by the RZB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZB. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
16	RSZ_INT_CYC_RZA	RESIZER module event: This event is the circular interrupt for RESIZER #A. An event can be triggered every time that RSZ_IRQ_RZA output lines have been written out to the RZA_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, the circular buffer vertical size (set by the RZA_SDR_Y_PTR_E register) should be a multiple of RSZ_IRQ_RZA. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
15	RSZ_INT_DMA	This event is triggered when the last EOF (of the two MTC interfaces) is sent out to the BL and that the resizer core has returned to idle. rsz_int_dma is a true indication that all processing is finished for the particular frame on both resizer engines. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
14	RSZ_INT_LAST_PIX	This event is triggered when the last pixel of the valid area is received. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
13	RSZ_INT_REG	This event is triggered when the first pixel of the valid area is received. Shadowed registers can be updated at any time but the new value will take effect on the next rsz_int_reg event. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
12	H3A_INT	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
11	AF_INT	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
10	AEW_INT	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
9	IPIPEIF_IRQ	IPIPEIF module interrupt Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
8	IPIPE_INT_HST	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
7	IPIPE_INT_BSC	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
6	IPIPE_INT_DMA	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
5	IPIPE_INT_LAST_PIX	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
4	IPIPE_INT_REG	Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
3	ISIF_INT_3	LSC interrupt issued by 2D-LSC block. Four types of 2D-LSC can be generated and mapped to the INT_3 line. For more information, see Section 8.3.3.6.10.1.5, *ISS ISP ISIF 2D-LSC Events and Status Checking.* Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
2	ISIF_INT_2	VD interrupt 2 event. Read this bit to check the interrupt mapped to the INT_2 line. This interrupt is also set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.6.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
1	ISIF_INT_1	VD interrupt 1 event. Read this bit to check the interrupt mapped to the INT_1 line. This interrupt is also set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.6.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
0	ISIF_INT_0	VD interrupt 0 event. Read this bit to check the interrupt mapped to the INT_0 line. This interrupt is also set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.6.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

Table 8-513. Register Call Summary for Register ISP5_IRQSTATUS_i

ISS ISP

- ISS ISP RSZ Reset Behavior: [0] [1] [2]
- ISS ISP5 SYS1 Register Summary: [3]

NOTE: ISP submodule interrupts are mapped to ISP top-level lines. Moreover, ISP top-level lines are mapped to the ISS top interrupt merger level. For information about how IRQ lines are handled at the ISP level, see Table 8-419. For information about how IRQs are handled at the ISS top-level before the signals leave ISS boundaries, see Section 8.1.2.1.1, *ISS Interrupt Merger.*

Table 8-514. ISP5_IRQENABLE_SET_i

Address Offset	0x0000 002C + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 002C + (0x10 * i)	**Instance**	ISS_ISP5_SYS1
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register. The ISP outputs four interrupt lines, ISP_IRQ0 to ISP_IRQ3. Any internal ISP event can be merged on the four lines. A same event must be enabled on only one interrupt line.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCP_ERR_IRQ	RESERVED	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	RESERVED	IPIPE_INT_EOF	H3A_INT_EOF	RSZ_INT_EOF1	RSZ_INT_EOF0	RESERVED		RSZ_FIFO_IN_BLK_ERR	RSZ_FIFO_OVF	RSZ_INT_CYC_RZB	RSZ_INT_CYC_RZA	RSZ_INT_DMA	RSZ_INT_LAST_PIX	RSZ_INT_REG	H3A_INT	AF_INT	AEW_INT	IPIPEIF_IRQ	IPIPE_INT_HST	IPIPE_INT_BSC	IPIPE_INT_DMA	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT_3	ISIF_INT_2	ISIF_INT_1	ISIF_INT_0

Bits	Field Name	Description	Type	Reset
31	OCP_ERR_IRQ	An OCP error has been received on the ISP master port. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
30	RESERVED		R	0
29	IPIPE_INT_DPC_RNEW1	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
28	IPIPE_INT_DPC_RNEW0	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
27	IPIPE_INT_DPC_INI	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
26	RESERVED		R	0
25	IPIPE_INT_EOF	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
24	H3A_INT_EOF	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
23	RSZ_INT_EOF1	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer B engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
22	RSZ_INT_EOF0	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer A engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
21:20	RESERVED		R	0x0
19	RSZ_FIFO_IN_BLK_ERR	This event signals that the minimum vertical blanking period has not been respected causing errors in the input data buffering submodule. This event will be triggered when the rsz_int_reg event of frame N is triggered before the rsz_int_dma of frame N + 1. This event would typically happen at the transition between two frames because there is not enough vertical blanking between frames: the firmware must take care to ensure enough vertical blanking. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
18	RSZ_FIFO_OVF	This event signals that overflow happened in the input data buffering submodule or in the RSZ output interface. This event would typically happen while processing a frame because the video port pixel clock is too high: the firmware must take care to use a lower pixel clock at the input of the resizer module. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
17	RSZ_INT_CYC_RZB	RESIZER module event: This event is the circular interrupt for RESIZER #B. An event can be triggered every time that RSZ_IRQ_RZB output lines have been written out to the RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value should be such that the circular buffer vertical size (set by the RZB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZB. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
16	RSZ_INT_CYC_RZA	RESIZER module event: This event is the circular interrupt for RESIZER #A. An event can be triggered every time that RSZ_IRQ_RZA output lines have been written out to the RZA_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, the circular buffer vertical size (set by the RZA_SDR_Y_PTR_E register) should be a multiple of RSZ_IRQ_RZA. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
15	RSZ_INT_DMA	This event is triggered when the last EOF (of the two MTC interfaces) is sent out to the BL and that the resizer core has returned to idle. rsz_int_dma is a true indication that all processing is finished for the particular frame on both resizer engines. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
14	RSZ_INT_LAST_PIX	This event is triggered when the last pixel of the valid area is received. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
13	RSZ_INT_REG	This event is triggered when the first pixel of the valid area is received. Shadowed registers can be updated at any time but the new value will take effect on the next rsz_int_reg event. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
12	H3A_INT	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
11	AF_INT	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
10	AEW_INT	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
9	IPIPEIF_IRQ	IPIPEIF module interrupt Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
8	IPIPE_INT_HST	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
7	IPIPE_INT_BSC	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
6	IPIPE_INT_DMA	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
5	IPIPE_INT_LAST_PIX	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
4	IPIPE_INT_REG	Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
3	ISIF_INT_3	LSC interrupt issued by the 2D-LSC block. Four types of 2D-LSC can be generated and mapped to the INT_3 line. For more information, see Section 8.3.3.6.10.1.5, *ISS ISP ISIF 2D-LSC Events and Status Checking.* Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
2	ISIF_INT_2	VD interrupt 2 event. Set this bit to enable the interrupt and map it to the INT_2 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.6.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
1	ISIF_INT_1	VD interrupt 1 event. Set this bit to enable the interrupt and map it to the INT_1 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.6.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0
0	ISIF_INT_0	VD interrupt 0 event. Set this bit to enable the interrupt mapped to INT_0 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.6.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toSet	0

Table 8-515. Register Call Summary for Register ISP5_IRQENABLE_SET_i

ISS ISP

- ISS ISP Interrupt Tree: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- ISS ISP IPIPEIF Interrupts: [26]
- ISS ISP IPIPE Interrupts: [27]
- ISS ISP RSZ Interrupts: [28]
- ISS ISP H3A Interrupts: [29]
- ISS ISP ISIF Interrupts: [30]
- ISS ISP IPIPEIF Module Events and Status Checking: [31]
- ISS ISP ISIF 2D-LSC Active Region Settings: [32]
- ISS ISP5 SYS1 Register Summary: [33]

NOTE: Setting the ISP submodule interrupts and mapping them to the ISP lines requires a configuration to receive the IRQ events at a higher ISS interrupt merger level. For information about how IRQ lines are handled at the ISP level, see Table 8-419. For information about how IRQs are handled at the ISS top-level before the signals leave ISS boundaries, see Section 8.1.2.1.1, *ISS Interrupt Merger.*

Table 8-516. ISP5_IRQENABLE_CLR_i

Address Offset	0x0000 0030 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 0030 + (0x10 * i)	**Instance**	ISS_ISP5_SYS1
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register. The ISP outputs four interrupt lines, ISP_IRQ0 to ISP_IRQ3. Any internal ISP event can be merged on the four lines. A same event must be enabled on only one interrupt line.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCP_ERR_IRQ	RESERVED	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	RESERVED	IPIPE_INT_EOF	H3A_INT_EOF	RSZ_INT_EOF1	RSZ_INT_EOF0	RESERVED		RSZ_FIFO_IN_BLK_ERR	RSZ_FIFO_OVF	RSZ_INT_CYC_RZB	RSZ_INT_CYC_RZA	RSZ_INT_DMA	RSZ_INT_LAST_PIX	RSZ_INT_REG	H3A_INT	AF_INT	AEW_INT	IPIPEIF_IRQ	IPIPE_INT_HST	IPIPE_INT_BSC	IPIPE_INT_DMA	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT_3	ISIF_INT_2	ISIF_INT_1	ISIF_INT_0

Bits	Field Name	Description	Type	Reset
31	OCP_ERR_IRQ	An OCP error has been received on the ISP master port. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
30	RESERVED		R	0
29	IPIPE_INT_DPC_RNEW1	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
28	IPIPE_INT_DPC_RNEW0	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
27	IPIPE_INT_DPC_INI	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
26	RESERVED		R	0
25	IPIPE_INT_EOF	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW	0
24	H3A_INT_EOF	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW	0
23	RSZ_INT_EOF1	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer B engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW	0

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Bits	Field Name	Description	Type	Reset
22	RSZ_INT_EOF0	RESIZER module event: This event signals that the BL has received the EOF signal from the resizer A engine which happens one the last transfer in the frame has happened. Note that because the BL has FIFOs it may take some additional time before true data transfer completion to memory. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW	0
21:20	RESERVED		R	0x0
19	RSZ_FIFO_IN_BLK_ERR	This event signals that the minimum vertical blanking period has not been respected causing errors in the input data buffering submodule. This event will be triggered when the rsz_int_reg event of frame N is triggered before the rsz_int_dma of frame N + 1. This event would typically happen at the transition between two frames because there is not enough vertical blanking between frames: the firmware must take care to ensure enough vertical blanking. The hardware cannot recover from this error. It will be required to perform a reset of the IP. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
18	RSZ_FIFO_OVF	RESIZER module event: This event signals that overflow happened in the input data buffering submodule or in the RSZ output interface.. This event would typically happen because the video port pixel clock is too high. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
17	RSZ_INT_CYC_RZB	RESIZER module event: This event is the circular interrupt for RESIZER #B. An event can be triggered every time that RSZ_IRQ_RZB output lines have been written out to the RZB_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, this value should be such that the circular buffer vertical size (set by the RZB_SDR_Y_PTR_E register) is a multiple of RSZ_IRQ_RZB. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
16	RSZ_INT_CYC_RZA	RESIZER module event: This event is the circular interrupt for RESIZER #A. An event can be triggered every time that RSZ_IRQ_RZA output lines have been written out to the RZA_SDR_Y buffer. The range can go from 1 to 8192 lines. Usually, the circular buffer vertical size (set by the RZA_SDR_Y_PTR_E register) should be a multiple of RSZ_IRQ_RZA. Note that at the time the interrupt is triggered, the actual data write has not taken place. It may take a few hundred of cycles to complete the data write into system memory. This is not an issue since the start of the buffer is read first. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
15	RSZ_INT_DMA	RESIZER module event: This event is triggered when the last EOF (of the two MTC interfaces) is sent out to the BL and that the resizer core has returned to idle. rsz_int_dma is a true indication that all processing is finished for the particular frame on both resizer engines. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
14	RSZ_INT_LAST_PIX	RESIZER module event: This event is triggered when the last pixel of the valid area is received. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
13	RSZ_INT_REG	RESIZER module event: This event is triggered when the first pixel of the valid area is received. Shadowed registers can be updated at any time but the new value will take effect on the next rsz_int_reg event. Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
12	H3A_INT	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
11	AF_INT	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
10	AEW_INT	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
9	IPIPEIF_IRQ	IPIPEIF module interrupt Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
8	IPIPE_INT_HST	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
7	IPIPE_INT_BSC	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
6	IPIPE_INT_DMA	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
5	IPIPE_INT_LAST_PIX	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
4	IPIPE_INT_REG	Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
3	ISIF_INT_3	Set this bit to disable the LSC interrupt issued by the 2D-LSC block. Four types of 2D-LSC can be generated and mapped to the INT_3 line. For more information, see Section 8.3.3.6.10.1.5, *ISS ISP ISIF 2D-LSC Events and Status Checking.* Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
2	ISIF_INT_2	VD interrupt 2 event. Set this bit to disable the interrupt mapped to the INT_2 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.6.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
1	ISIF_INT_1	VD interrupt 1 event. Set this bit to disable the interrupt mapped to the INT_1 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.6.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0
0	ISIF_INT_0	VD interrupt 0 event. Set this bit to disable the interrupt mapped to the INT_0 line. This interrupt is set based on the VD pulse position after receiving a configured number of horizontal pulse signals. For more information, see Section 8.3.3.6.19.1, *ISS ISP ISIF VDINT0, VDINT1 and VDINT2 Interrupts.* Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled (masked)	RW W1toClr	0

Table 8-517. Register Call Summary for Register ISP5_IRQENABLE_CLR_i

ISS ISP

- ISS ISP RSZ Reset Behavior: [0] [1]
- ISS ISP5 SYS1 Register Summary: [2]

NOTE: Setting or disabling the ISP submodule interrupts mapped to the ISP lines requires a configuration to receive or disable the IRQ events at a higher ISS interrupt merger level. For information about how IRQ lines are handled at the ISP level, see Table 8-419. For information about how IRQs are handled at the ISS top-level before the signals leave ISS boundaries, see Section 8.1.2.1.1, *ISS Interrupt Merger.*

Table 8-518. ISP5_DMAENABLE_SET

Address Offset	0x0000 0064		
Physical Address	0x5201 0064	**Instance**	ISS_ISP5_SYS1
Description	Per-line DMA enable bit vector Write 1 to set (enable DMA request generation). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IPIPE_INT_DPC_RNEW1	IPIPE_INT_LAST_PIX	IPIPE_INT_DPC_RNEW0	IPIPE_INT_HST	IPIPE_INT_BSC

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	IPIPE_INT_DPC_RNEW1	Enable for ISP DMA request generation on line #2 This DMA request must be set to transfer the DPC data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0
3	IPIPE_INT_LAST_PIX	Enable for ISP DMA request generation on line #3 This DMA request must be set to transfer the GAMMA data from memory to the IPIPE internal RAM or to initialize the DPC table. One must set the ISP5_CTRL.DMA3_CFG register before enabling this DMA request. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0
2	IPIPE_INT_DPC_RNEW0	Enable for ISP DMA request generation on line #2 This DMA request must be set to transfer the DPC data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0
1	IPIPE_INT_HST	Enable for ISP DMA request generation on line #1 This DMA request must be set to transfer the HIST data from the IPIPE internal RAM to memory. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0
0	IPIPE_INT_BSC	Enable for ISP DMA request generation on line #0 This DMA request must be set to transfer the BSC data from the IPIPE internal RAM to memory. Write 0x0: No action Write 0x1: Enable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toSet	0

Table 8-519. Register Call Summary for Register ISP5_DMAENABLE_SET

ISS ISP

- ISS ISP DMA Requests: [0]
- ISS ISP5 SYS1 Register Summary: [1]

Table 8-520. ISP5_DMAENABLE_CLR

Address Offset	0x0000 0068		
Physical Address	0x5201 0068	**Instance**	ISS_ISP5_SYS1
Description	Per-line DMA clear bit vector Write 1 to clear (disable DMA request generation). Readout equal to corresponding _SET register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IPIPE_INT_DPC_RNEW1	IPIPE_INT_LAST_PIX	IPIPE_INT_DPC_RNEW0	IPIPE_INT_HST	IPIPE_INT_BSC

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	IPIPE_INT_DPC_RNEW1	Clear for ISP DMA request generation on line ISS_DREQ_3. This DMA request must be set to transfer the DPC data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0
3	IPIPE_INT_LAST_PIX	Clear for ISP DMA request generation on ISS_DREQ_4. This DMA request must be set to transfer the GAMMA data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0
2	IPIPE_INT_DPC_RNEW0	Clear for ISP DMA request generation on ISS_DREQ_3. This DMA request must be set to transfer the DPC data from memory to the IPIPE internal RAM. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0
1	IPIPE_INT_HST	Clear for ISP DMA request generation on ISS_DREQ_2. This DMA request must be set to transfer the HIST data from the IPIPE internal RAM to memory. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0
0	IPIPE_INT_BSC	Clear for ISP DMA request generation on ISS_DREQ_1. This DMA request must be set to transfer the BSC data from the IPIPE internal RAM to memory. Write 0x0: No action Write 0x1: Disable DMA Read 0x1: DMA enabled Read 0x0: DMA disabled	RW W1toClr	0

Table 8-521. Register Call Summary for Register ISP5_DMAENABLE_CLR

ISS ISP

- ISS ISP DMA Requests: [0]
- ISS ISP5 SYS1 Register Summary: [1]

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Table 8-522. ISP5_CTRL

Address Offset	0x0000 006C		
Physical Address	0x5201 006C	**Instance**	ISS_ISP5_SYS1
Description	ISP5 CONTROL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA3_CFG		RESERVED		RESERVED	HST_RD_CHK	DPC_EVT_INI	MSTANDBY	VD_PULSE_EXT	PCLK_INV	MFLAG	MSTANDDBY_WAIT	RESERVED				BL_CLK_ENABLE	ISIF_CLK_ENABLE	H3A_CLK_ENABLE	RSZ_CLK_ENABLE	IPIPE_CLK_ENABLE	IPIPEIF_CLK_ENABLE	SYNC_ENABLE	PSYNC_CLK_SEL	VBUSM_CIDS				VBUSM_CPRIORITY			OCP_WRNP

Bits	Field Name	Description	Type	Reset
31:30	DMA3_CFG	This bit field selects the DMA transfer configuration which is used with the ISS_DRE_4 DMA request signal. This DMA request is generated from IPIPE_INT_LAST_PIXEL event. One can choose to use this DMA request to transfer the DPC initialization data, the gamma table, or both. 0x0: No DMA request associated with ISS_DREQ_4. 0x1: DPC DMA request associated with ISS_DREQ_4. Expected DMA transfer size is 2 KiB in the range 0x8000-0x87FF. DPC_EVT_INI must be set to 0. 0x3: DPC + GAMMA DMA request associated with ISS_DREQ_4. Expected DMA transfer size is 8 KiB in the range 0x8000-0x87FF and 0xA800-0xBFFF. DPC_EVT_INI must be set to 0. 0x2: GAMMA DMA request associated with ISS_DREQ_4. Expected DMA transfer size is 6 KiB in the range 0xA800-0xBFFF.	RW	0x0
29:28	RESERVED		R	0x0
27	RESERVED		R	0x0
26	HST_RD_CHK	When the HISTOGRAM computation is enabled and the HST DMA request is not used to read out the data, this register ensures that the data is read fast enough, else an interrupt ISP5_IRQSTATUS2_i[5] IPIPE_HST_ERR is triggered. The hardware sets automatically this bit to 1 when software can start reading the memory.	RW	0

CAUTION

Software must set this bit to 0 after reading the data. Once the MPU/IPU has read the histogram data, it must clear this register, else the ISP5_IRQSTATUS2_i[5] IPIPE_HST_ERR will occur.

Write 0x0: Clears the signal to avoid error generation. The software must write this bit to 0 after the last data read.

Write 0x1: Reserved

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Bits	Field Name	Description	Type	Reset
		Read 0x1: The MPU/IPU can read the data from the memory. Needs to complete fast enough to avoid the interrupt generation.		
		Read 0x0: No interrupt generation can happen		
25	DPC_EVT_INI	Select the IPIPE module event to be used to generate the DMA requests for the DPC submodule. 0x0: IPIPE_INT_LAST_PIX event is selected. 0x1: IPIPE_INT_DPC_INI event is selected.	RW	0
24	MSTANDBY	MStandby signal assertion and de-assertion control for power management transitions. After software reset, this bit is asserted. Write "1" to transition from normal mode to idle mode. The firmware needs to ensure that no more ISP processing is ongoing before setting up this bit. Write "0" to transition from idle mode to normal mode. The software should poll ISP5_CTRL.MSTANDBY_WAIT = 0 after writing ISP5_CTRL.MSTANDBY = 0 in a transition from idle to normal mode. 0x0: De-assert MStandby signal. May not be immediate due to power management handshaking btw the MStandby and Wait signals. 0x1: Assert MStandby signal	RW	1
23	VD_PULSE_EXT	VD pulse extension enable This bit enables or disables the VD extension bridge. By default, the bridge is enabled. At ISS level, it is expected that ISP5_CTRL.VD_PULSE_EXT = 1 when the VPORT gets data from the CSI2 RX module and ISP5_CTRL.VD_PULSE_EXT = 0 when the VPORT gets data from the parallel interface or the CCP2 RX module. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for start of frame comes. 0x0: Disabled 0x1: Enabled	RW	1
22	PCLK_INV	Pixel clock inversion This bit enables or disables pixel clock inversion. The ISP always samples the data on the rising edge of the pixel clock. Enabling the inversion shifts the resampling period by 1/2 a pixel clock period. PCLK needs to be disabled at ISS level before setting to 0x1 this bit. This can be done through the proper ISS_CLKCTRL[] VPORTx_CLK register bit on ISS top level, depending on the interface (CCP2 or CSI2) that is sending data on the ISP video port. 0x0: Normal 0x1: Inversed	RW	0
21	MFLAG	MFlag signal generation control This bit controls how the OCP MFlag signal is generated on the ISS NOC. 0x0: The MFlag value is dynamic. 0x1: The MFlag value is static. The value is set with the ISP5_CTRL[3:1] VBUSM_CPRIORITY.	RW	0
20	MSTANDBY_WAIT	MStandby / Wait power management status bit. The power management framework of the ISP is based on the handshaking of the MStandby and Wait signals. The software is not supposed to write inside the ISP slave port and initiate traffic when ISP5_CTRL.MSTANDBY bit is written. The software can poll this bit to know when Wait signal is deasserted. Read 0x1: MStandby signal is asserted. Read 0x0: MStandby signal is deasserted.	R	-
19:16	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
15	BL_CLK_ENABLE	BL clock enable 0x0: Disable 0x1: Enable	RW	0
14	ISIF_CLK_ENABLE	ISIF clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for start of frame comes. 0x0: Disable 0x1: Enable	RW	0
13	H3A_CLK_ENABLE	H3A clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. 0x0: Disable 0x1: Enable	RW	0
12	RSZ_CLK_ENABLE	RESIZER clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. 0x0: Disable 0x1: Enable	RW	0
11	IPIPE_CLK_ENABLE	IPIPE clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. 0x0: Disable 0x1: Enable	RW	0
10	IPIPEIF_CLK_ENABLE	IPIPEIF clock enable The ISP will return OCP_ERROR if one tries to program the module MMR or memory when the clock is disabled. 0x0: Disable 0x1: Enable	RW	0
9	SYNC_ENABLE	PCLK Sync module enable. This bit may only be modified when the video port is not receiving data such as when data is read from the IPIPEIF module memory read port. 0x0: Disable 0x1: Enable	RW	0
8	PSYNC_CLK_SEL	PCLK Sync clock select. This bit selects the clock which is used to resynchronize the input pixel clock. 0x0: GCK_MMR. Can be used if the input pixel clock is always lower than 152 MHz. 0x1: ISP_FCLK. Must be used if the pixel clock is higher than 152 MHz.	RW	0
7:4	VBUSM_CIDS	BL MAX VBUSM CIDs The BL module supports up to 16 CIDs/tags. This bit field sets up the maximum number of CISs/tags that the BL can use. The actual number of CIDs/tags is setup by VBUSM_CIDS + 1. Tag number 0 to VBUSM_CIDS are used.	RW	0xF

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Bits	Field Name	Description	Type	Reset
3:1	VBUSM_CPRIORITY	BL VBUSM priority setting 0x6: Normal Priority VBUSM cpriority[2:0] = 6 0x1: High Priority VBUSM cpriority[2:0] = 1 0x7: Normal Priority VBUSM cpriority[2:0] = 7 0x0: High Priority VBUSM cpriority[2:0] = 0 0x2: Medium Priority VBUSM cpriority[2:0] = 2 0x4: Normal Priority VBUSM cpriority[2:0] = 4 0x5: Normal Priority VBUSM cpriority[2:0] = 5 0x3: Medium Priority VBUSM cpriority[2:0] = 3	RW	0x4
0	OCP_WRNP	ISP OCP master port non-posted write control. 0x0: All writes are non posted. 0x1: All writes are posted.	RW	0

Table 8-523. Register Call Summary for Register ISP5_CTRL

ISS ISP

- ISS ISP Clocks: [0]
- ISS ISP Reset: [1] [2]
- ISS ISP DMA Requests: [3] [4]
- ISS ISP VP Top-Level Communication With CCP2 RX and CSI2 RX: [6] [7] [8]
- ISS ISP VP Pixel Clock Inversion: [9] [10] [11]
- ISS ISP BL Functional Description: [12]
- ISS ISP BL Out-of-Order Responses: [13]
- ISS ISP BL Dynamic and Static MFlag Generation: [14] [15] [16]
- ISS ISP BL Programming Model: [17] [18] [19] [20]
- ISS ISP5 SYS1 Register Summary: [21]
- ISS ISP5 SYS1 Register Description: [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32]
- ISS ISP5 SYS2 Register Description: [34]

Table 8-524. ISP5_MPSR

Address Offset	0x0000 007C		
Physical Address	0x5201 007C	**Instance**	ISS_ISP5_SYS1
Description	ISP memory access register. One need to pay attention when setting the bit fields in this register such that there is no conflict between the CPU and module accesses. Usually, the ISP modules must have access to the memories and it is only when the ISP is idle (vertical blanking period or module disabled that the CPU can access the memories.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							IPIPE_GAMMA_RGB_COPY	RESERVED			IPIPE_BSC_TB1	IPIPE_BSC_TB0	IPIPE_HST_TB3	IPIPE_HST_TB2	IPIPE_HST_TB1	IPIPE_HST_TB0	IPIPE_D3L_TB3	IPIPE_D3L_TB2	IPIPE_D3L_TB1	IPIPE_D3L_TB0	IPIPE_GBC_TB	IPIPE_YEE_TB	IPIPE_GMM_TBR	IPIPE_GMM_TBG	IPIPE_GMM_TBB	IPIPE_DPC_TB	ISIF_DCLAMP	ISIF_LSC_TB1	ISIF_LSC_TB0	ISIF_LIN_TB	RESERVED

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	IPIPE_GAMMA_RGB_COPY	GAMMA table RGB Copy This bit must be enable when one wants to use the same Gamma table for the R, G and B color components. When the CPU writes the R table, it is automatically copied to the G and B tables if this bit is set. 0x0: Copy disable Independent RGB gamma table 0x1: Copy enable Common RGB Gamma table	RW	0
23:21	RESERVED		R	0x0
20	IPIPE_BSC_TB1	IPIPE BSC TB1 memory access priority This memory is expected to be read by the CPU or the DMA to get BSC information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
19	IPIPE_BSC_TB0	IPIPE BSC TB0 memory access priority This memory is expected to be read by the CPU or the DMA to get BSC information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
18	IPIPE_HST_TB3	IPIPE histogram memory #3 access priority This memory is expected to be read by the CPU or the DMA to get HST information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
17	IPIPE_HST_TB2	IPIPE histogram memory #2 access priority This memory is expected to be read by the CPU or the DMA to get HST information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
16	IPIPE_HST_TB1	IPIPE histogram memory #1 access priority This memory is expected to be read by the CPU or the DMA to get HST information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0

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Bits	Field Name	Description	Type	Reset
15	IPIPE_HST_TB0	IPIPE histogram memory #0 access priority This memory is expected to be read by the CPU or the DMA to get HST information during vertical blanking period. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
14	IPIPE_D3L_TB3	D3L TB3 memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
13	IPIPE_D3L_TB2	D3L TB2 memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
12	IPIPE_D3L_TB1	D3L TB1 memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
11	IPIPE_D3L_TB0	D3L TB0 memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
10	IPIPE_GBC_TB	IPIPE GBC TB memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
9	IPIPE_YEE_TB	YEE TB memory access priority This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
8	IPIPE_GMM_TBR	IPIPE Gamma LUT R memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
7	IPIPE_GMM_TBG	IPIPE Gamma LUT G memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0

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Bits	Field Name	Description	Type	Reset
6	IPIPE_GMM_TBB	IPIPE Gamma LUT B memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
5	IPIPE_DPC_TB	IPIPE defect pixel memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
4	ISIF_DCLAMP	ISIF DC accumulation memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
3	ISIF_LSC_TB1	ISIF LSC memory 1 access This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE has memory access When the module has memory access, the potential concurrent CPU accesses (on the ISP memory map) to read the memory are stalled. The CPU will eventually get back the data during the horizontal or vertical blanking periods when the module is not making access anymore. 0x1: CPU has memory access When the CPU has memory access (read or write), it will cause data corruption if the module tries to perform concurrent memory accesses. The module cannot know that the read or write access has not taken place because of CPU accesses.	RW	0
2	ISIF_LSC_TB0	ISIF LSC memory 0 access This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE has memory access. When the module has memory access, the potential concurrent CPU accesses (on the ISP memory map) to read the memory are stalled. The CPU will eventually get back the data during the horizontal or vertical blanking periods when the module is not making access anymore. 0x1: CPU has memory access When the CPU has memory access (read or write), it will cause data corruption if the module tries to perform concurrent memory accesses. The module cannot know that the read or write access has not taken place because of CPU accesses.	RW	0
1	ISIF_LIN_TB	ISIF linearity compensation memory arbitration This memory is expected to be written during ISP initialization and potentially updated during vertical blanking periods. 0x0: MODULE access has higher priority 0x1: CPU access has higher priority.	RW	0
0	RESERVED		R	0

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Table 8-525. Register Call Summary for Register ISP5_MPSR

ISS ISP

- ISS ISP BL Programming Model: [0]
- ISS ISP5 SYS1 Register Summary: [1]

Table 8-526. ISP5_BL_MTC_1

Address Offset	0x0000 0080		
Physical Address	0x5201 0080	**Instance**	ISS_ISP5_SYS1
Description	MEMORY REQUEST MINIMUM INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISIF_R																IPIPEIF_R															

Bits	Field Name	Description	Type	Reset
31:16	ISIF_R	Sets the minimum interval btw two consecutive memory requests for the ISIF-Read port. Specified in number of interface clock cycles.	RW	0x0000
15:0	IPIPEIF_R	Sets the minimum interval btw two consecutive memory requests for the IPIPEIF-Read port. Specified in number of interface clock cycles.	RW	0x0000

Table 8-527. Register Call Summary for Register ISP5_BL_MTC_1

ISS ISP

- ISS ISP ISIF Read Port: [0]
- ISS ISP BL Peak Memory Bandwidth Reduction: [1]
- ISS ISP BL Programming Model: [2] [3] [4]
- ISS ISP5 SYS1 Register Summary: [5]

Table 8-528. ISP5_BL_MTC_2

Address Offset	0x0000 0084		
Physical Address	0x5201 0084	**Instance**	ISS_ISP5_SYS1
Description	MEMORY REQUEST MINIMUM INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H3A_W																RESERVED															

Bits	Field Name	Description	Type	Reset
31:16	H3A_W	Sets the minimum interval btw two consecutive memory requests for the H3A-Write port. Specified in number of interface clock cycles.	RW	0x0000
15:0	RESERVED		R	0x0000

Table 8-529. Register Call Summary for Register ISP5_BL_MTC_2

ISS ISP

- ISS ISP BL Peak Memory Bandwidth Reduction: [0]
- ISS ISP5 SYS1 Register Summary: [1]

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Table 8-530. ISP5_BL_VBUSM

Address Offset	0x0000 0088		
Physical Address	0x5201 0088	**Instance**	ISS_ISP5_SYS1
Description	BL VBUSM TUNING REGISTER The settings in the register are static and not expected to be modified dynamically.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										MFLAG_THRES	LASTCMD_DLY				

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	MFLAG_THRES	MFLAG Threshold value The value of this bit field is a threshold which is compared to the MFlag output of the ISP5. If the BL MFlag signal is greater or equal to this threshold the last beat of the VBUSM command is delayed by ISP5_BL_VBUSM[4:0] LASTCMD_DLY cycles. Only values 0, 1 are valid, the least significant bit is tied off to 1 to make a 2-bit field. 0x0: Thres = 1 0x1: Thres = 3	RW	1
4:0	LASTCMD_DLY	The value of this bit field represents a delay expressed in cycles (L3_MAIN clock). This value is used to delay the last beat of the VBUSM command such that the ISP does not loose arbitration at the ISS level because the BL does not generate back to back requests by default. The last beat is delayed until the counter expires or the new request is accepted. This delay is used when the MFlag output of the ISP is greater or equal to ISP5_BL_VBUSM[5] MFLAG_THRES. One can set this value to 0 to disable the last command beat delay.	RW	0x04

Table 8-531. Register Call Summary for Register ISP5_BL_VBUSM

ISS ISP

- ISS ISP BL VBUSM2OCP Last Beat Command Delay: [0] [1] [2] [3]
- ISS ISP5 SYS1 Register Summary: [4]
- ISS ISP5 SYS1 Register Description: [5] [6]

8.3.5.3 ISS ISP5 SYS2 Registers

CAUTION

The ISS ISP5 SYS2 registers are limited to 32 bit and 16 bit data accesses; 8bit data access is not allowed and can corrupt register content.

8.3.5.3.1 ISS ISP5 SYS2 Register Summary

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Table 8-532. ISS ISP5 SYS2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISP5_SYS2 Base Address
ISP5_KEY_EN1	R	32	0x0000 0000	0x5201 00A0
ISP5_KEY_EN2	R	32	0x0000 0004	0x5201 00A4
ISP5_KEY_EN3	R	32	0x0000 0008	0x5201 00A8
ISP5_KEY_EN4	R	32	0x0000 000C	0x5201 00AC
ISP5_KEY_EN5	R	32	0x0000 0010	0x5201 00B0
ISP5_KEY_EN6	R	32	0x0000 0014	0x5201 00B4
ISP5_IRQSTATUS_RAW2_i (1)	RW	32	0x0000 0018 + (0x10 * i)	0x5201 00B8 + (0x10 * i)
ISP5_IRQSTATUS2_i (1)	RW	32	0x0000 001C + (0x10 * i)	0x5201 00BC + (0x10 * i)
ISP5_IRQENABLE_SET2_i (1)	RW	32	0x0000 0020 + (0x10 * i)	0x5201 00C0 + (0x10 * i)
ISP5_IRQENABLE_CLR2_i (1)	RW	32	0x0000 0024 + (0x10 * i)	0x5201 00C4 + (0x10 * i)

(1) i = 0 to 3

8.3.5.3.2 ISS ISP5 SYS2 Register Description

Table 8-533. ISP5_KEY_EN1

Address Offset	0x0000 0000		
Physical Address	0x5201 00A0	**Instance**	ISS_ISP5_SYS2
Description	IPIPE eFuse enable.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															KEY1_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY1_EN	eFuse enable Equals 1 when ISP5_EFUSE3_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0

Table 8-534. Register Call Summary for Register ISP5_KEY_EN1

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

Table 8-535. ISP5_KEY_EN2

Address Offset	0x0000 0004		
Physical Address	0x5201 00A4	**Instance**	ISS_ISP5_SYS2
Description	ISIF eFuse enable.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															KEY1_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY1_EN	eFuse enable Equals 1 when ISP5_EFUSE1_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	1

Table 8-536. Register Call Summary for Register ISP5_KEY_EN2

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

Table 8-537. ISP5_KEY_EN3

Address Offset	0x0000 0008		
Physical Address	0x5201 00A8	**Instance**	ISS_ISP5_SYS2
Description	ISIF eFuse enable.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															KEY_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY_EN	eFuse enable Equals 1 when ISP5_EFUSE3_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0

Table 8-538. Register Call Summary for Register ISP5_KEY_EN3

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

Table 8-539. ISP5_KEY_EN4

Address Offset	0x0000 000C		
Physical Address	0x5201 00AC	**Instance**	ISS_ISP5_SYS2
Description	IPIPEIF eFuse enable.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														KEY2_EN	KEY1_EN

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	KEY2_EN	eFuse enable Equals 1 when ISP5_EFUSE4_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0
0	KEY1_EN	eFuse enable Equals 1 when ISP5_EFUSE1_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	1

Table 8-540. Register Call Summary for Register ISP5_KEY_EN4

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

Table 8-541. ISP5_KEY_EN5

Address Offset	0x0000 0010		
Physical Address	0x5201 00B0	**Instance**	ISS_ISP5_SYS2
Description	H3A eFuse enable.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															KEY_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY_EN	eFuse enable Equals 1 when ISP5_EFUSE2_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0

Table 8-542. Register Call Summary for Register ISP5_KEY_EN5

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

Table 8-543. ISP5_KEY_EN6

Address Offset	0x0000 0014		
Physical Address	0x5201 00B4	**Instance**	ISS_ISP5_SYS2
Description	H3A eFuse enable.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															KEY_EN

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	KEY_EN	eFuse enable Equals 1 when ISP5_EFUSE3_EN = 1 or 0 otherwise. Read 0x1: Enable Read 0x0: Disable	R	0

Table 8-544. Register Call Summary for Register ISP5_KEY_EN6

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

Table 8-545. ISP5_IRQSTATUS_RAW2_i

Address Offset	0x0000 0018 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 00B8 + (0x10 * i)	**Instance**	ISS_ISP5_SYS2
Description	Per-event raw interrupt status vector. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug. Overflow / underflow errors are not recoverable at ISP level, a software reset is required at ISS level. The ISP outputs 4 interrupt lines ISP5_IRQ0 to ISP5_IRQ3. Any internal ISP event can be merged on the 4 lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										RESERVED	IPIPE_HST_ERR	ISIF_OVF	IPIPE_BOXCAR_OVF	IPIPEIF_UDF	H3A_OVF

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	RESERVED		R	0x0
4	IPIPE_HST_ERR	IPIPE HISTOGRAM memory read error This error will happen when the histogram data is not read fast enough by the MPU/IPU or the DMA_SYSTEM. When the data is read with the MPU/IPU, one need to pay attention to clear the ISP5_CTRL[26] HST_RD_CHK bit immediately after reading the last data, else this event will be set. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
3	ISIF_OVF	ISIF module overflow Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
2	IPIPE_BOXCAR_OVF	IPIPE BOXCAR module overflow Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
1	IPIPEIF_UDF	IPIPEIF module underflow interrupt Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0
0	H3A_OVF	H3A module overflow interrupt. Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending Read 0x0: No event pending	RW W1toSet	0

Table 8-546. Register Call Summary for Register ISP5_IRQSTATUS_RAW2_i

ISS ISP

- ISS ISP IPIPEIF Module Events and Status Checking: [0] [1]
- ISS ISP IPIPEIF Interframe Operations: [2]
- ISS ISP5 SYS2 Register Summary: [3]

Table 8-547. ISP5_IRQSTATUS2_i

Address Offset	0x0000 001C + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 00BC + (0x10 * i)	**Instance**	ISS_ISP5_SYS2
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Overflow / underflow errors are not recoverable at ISP level, a software reset is required at ISS level. The ISP outputs 4 interrupt lines ISP5_IRQ0 to ISP5_IRQ3. Any internal ISP event can be merged on the 4 lines. A same event must be enabled on only one interrupt line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										RESERVED	IPIPE_HST_ERR	ISIF_OVF	IPIPE_BOXCAR_OVF	IPIPEIF_UDF	H3A_OVF

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	RESERVED		R	0x0
4	IPIPE_HST_ERR	IPIPE HISTOGRAM memory read error This error will happen when the histogram data is not read fast enough by either the MPU/IPU or the DMA_SYSTEM. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
3	ISIF_OVF	ISIF module overflow Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
2	IPIPE_BOXCAR_OVF	IPIPE BOXCAR module overflow Overflow errors are not recoverable at ISP level, a software reset is required at ISS level. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
1	IPIPEIF_UDF	IPIPEIF module underflow interrupt Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0
0	H3A_OVF	H3A module overflow interrupt. Overflow errors are not recoverable at ISP level, a software reset is required at ISS level. Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending Read 0x0: No (enabled) event pending	RW W1toClr	0

Table 8-548. Register Call Summary for Register ISP5_IRQSTATUS2_i

ISS ISP

- ISS ISP DMA Requests:
- ISS ISP5 SYS1 Register Description: [4] [5]
- ISS ISP5 SYS2 Register Summary: [6]

Table 8-549. ISP5_IRQENABLE_SET2_i

Address Offset	0x0000 0020 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 00C0 + (0x10 * i)	**Instance**	ISS_ISP5_SYS2
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register. Overflow / underflow errors are not recoverable at ISP level, a software reset is required at ISS level. The ISP outputs 4 interrupt lines ISP5_IRQ0 to ISP5_IRQ3. Any internal ISP event can be merged on the 4 lines. A same event must be enabled on only one interrupt line.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										RESERVED	IPIPE_HST_ERR	ISIF_OVF	IPIPE_BOXCAR_OVF	IPIPEIF_UDF	H3A_OVF

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	RESERVED		R	0x0
4	IPIPE_HST_ERR	IPIPE HISTOGRAM memory read error This error will happen when the histogram data is not read fast enough by either the MPU/IPU or the DMA_SYSTEM.	RW W1toSet	0
3	ISIF_OVF	ISIF module overflow	RW W1toSet	0
2	IPIPE_BOXCAR_OVF	IPIPE BOXCAR module overflow	RW W1toSet	0
1	IPIPEIF_UDF	IPIPEIF module underflow interrupt	RW W1toSet	0
0	H3A_OVF	H3A module overflow interrupt. Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toSet	0

Table 8-550. Register Call Summary for Register ISP5_IRQENABLE_SET2_i

ISS ISP

- ISS ISP Interrupt Tree: [0] [1] [3] [4] [5] [6]
- ISS ISP IPIPEIF Interrupts: [7]
- ISS ISP IPIPE Interrupts: [8]
- ISS ISP H3A Interrupts: [9]
- ISS ISP ISIF Interrupts: [10]
- ISS ISP5 SYS2 Register Summary: [11]

Table 8-551. ISP5_IRQENABLE_CLR2_i

Address Offset	0x0000 0024 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x5201 00C4 + (0x10 * i)	**Instance**	ISS_ISP5_SYS2
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register. Overflow / underflow errors are not recoverable at ISP level, a software reset is required at ISS level. The ISP outputs 4 interrupt lines ISP5_IRQ0 to ISP5_IRQ3. Any internal ISP event can be merged on the 4 lines. A same event must be enabled on only one interrupt line.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										RESERVED	IPIPE_HST_ERR	ISIF_OVF	IPIPE_BOXCAR_OVF	IPIPEIF_UDF	H3A_OVF

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5	RESERVED		R	0x0
4	IPIPE_HST_ERR	IPIPE HISTOGRAM memory read error This error will happen when the histogram data is not read fast enough by either the MPU/IPU or the DMA_SYSTEM. Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0
3	ISIF_OVF	ISIF module overflow Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0
2	IPIPE_BOXCAR_OVF	IPIPE BOXCAR module overflow Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0
1	IPIPEIF_UDF	IPIPEIF module underflow interrupt Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0
0	H3A_OVF	H3A module overflow interrupt. Write 0x0: No action Write 0x1: Disable Interrupt Read 0x1: Interrupt enabled Read 0x0: Interrupt disabled	RW W1toClr	0

Table 8-552. Register Call Summary for Register ISP5_IRQENABLE_CLR2_i

ISS ISP

- ISS ISP5 SYS2 Register Summary: [0]

8.3.5.4 ISS RESIZER Registers

8.3.5.4.1 ISS RESIZER Register Summary

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Table 8-553. ISS RESIZER Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_RESIZER Base Address
RSZ_REVISION	R	32	0x0000 0000	0x5201 0400
RSZ_SYSCONFIG	RW	32	0x0000 0004	0x5201 0404
RESERVED	R	32	0x0000 0008	0x5201 0408
RSZ_IN_FIFO_CTRL	RW	32	0x0000 000C	0x5201 040C
RSZ_GNC	R	32	0x0000 0010	0x5201 0410
RSZ_FRACDIV	RW	32	0x0000 0014	0x5201 0414
RSZ_SRC_EN	RW	32	0x0000 0020	0x5201 0420
RSZ_SRC_MODE	RW	32	0x0000 0024	0x5201 0424
RSZ_SRC_FMT0	RW	32	0x0000 0028	0x5201 0428
RSZ_SRC_FMT1	RW	32	0x0000 002C	0x5201 042C
RSZ_SRC_VPS	RW	32	0x0000 0030	0x5201 0430
RSZ_SRC_VSZ	RW	32	0x0000 0034	0x5201 0434
RSZ_SRC_HPS	RW	32	0x0000 0038	0x5201 0438
RSZ_SRC_HSZ	RW	32	0x0000 003C	0x5201 043C
RSZ_DMA_RZA	RW	32	0x0000 0040	0x5201 0440
RSZ_DMA_RZB	RW	32	0x0000 0044	0x5201 0444
RSZ_DMA_STA	R	32	0x0000 0048	0x5201 0448
RSZ_GCK_MMR	RW	32	0x0000 004C	0x5201 044C
RESERVED	R	32	0x0000 0050	0x5201 0450
RSZ_GCK_SDR	RW	32	0x0000 0054	0x5201 0454
RSZ_IRQ_RZA	RW	32	0x0000 0058	0x5201 0458
RSZ_IRQ_RZB	RW	32	0x0000 005C	0x5201 045C
RSZ_YUV_Y_MIN	RW	32	0x0000 0060	0x5201 0460
RSZ_YUV_Y_MAX	RW	32	0x0000 0064	0x5201 0464
RSZ_YUV_C_MIN	RW	32	0x0000 0068	0x5201 0468
RSZ_YUV_C_MAX	RW	32	0x0000 006C	0x5201 046C
RSZ_YUV_PHS	RW	32	0x0000 0070	0x5201 0470
RSZ_SEQ	RW	32	0x0000 0074	0x5201 0474
RZA_EN	RW	32	0x0000 0078	0x5201 0478
RZA_MODE	RW	32	0x0000 007C	0x5201 047C
RZA_420	RW	32	0x0000 0080	0x5201 0480
RZA_I_VPS	RW	32	0x0000 0084	0x5201 0484
RZA_I_HPS	RW	32	0x0000 0088	0x5201 0488
RZA_O_VSZ	RW	32	0x0000 008C	0x5201 048C
RZA_O_HSZ	RW	32	0x0000 0090	0x5201 0490
RZA_V_PHS_Y	RW	32	0x0000 0094	0x5201 0494
RZA_V_PHS_C	RW	32	0x0000 0098	0x5201 0498
RZA_V_DIF	RW	32	0x0000 009C	0x5201 049C
RZA_V_TYP	RW	32	0x0000 00A0	0x5201 04A0
RZA_V_LPF	RW	32	0x0000 00A4	0x5201 04A4
RZA_H_PHS	RW	32	0x0000 00A8	0x5201 04A8
RZA_H_PHS_ADJ	RW	32	0x0000 00AC	0x5201 04AC
RZA_H_DIF	RW	32	0x0000 00B0	0x5201 04B0
RZA_H_TYP	RW	32	0x0000 00B4	0x5201 04B4
RZA_H_LPF	RW	32	0x0000 00B8	0x5201 04B8
RZA_DWN_EN	RW	32	0x0000 00BC	0x5201 04BC
RZA_DWN_AV	RW	32	0x0000 00C0	0x5201 04C0

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Table 8-553. ISS RESIZER Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_RESIZER Base Address
RZA_RGB_EN	RW	32	0x0000 00C4	0x5201 04C4
RZA_RGB_TYP	RW	32	0x0000 00C8	0x5201 04C8
RZA_RGB_BLD	RW	32	0x0000 00CC	0x5201 04CC
RZA_SDR_Y_BAD_H	RW	32	0x0000 00D0	0x5201 04D0
RZA_SDR_Y_BAD_L	RW	32	0x0000 00D4	0x5201 04D4
RZA_SDR_Y_SAD_H	RW	32	0x0000 00D8	0x5201 04D8
RZA_SDR_Y_SAD_L	RW	32	0x0000 00DC	0x5201 04DC
RZA_SDR_Y_OFT	RW	32	0x0000 00E0	0x5201 04E0
RZA_SDR_Y_PTR_S	RW	32	0x0000 00E4	0x5201 04E4
RZA_SDR_Y_PTR_E	RW	32	0x0000 00E8	0x5201 04E8
RZA_SDR_C_BAD_H	RW	32	0x0000 00EC	0x5201 04EC
RZA_SDR_C_BAD_L	RW	32	0x0000 00F0	0x5201 04F0
RZA_SDR_C_SAD_H	RW	32	0x0000 00F4	0x5201 04F4
RZA_SDR_C_SAD_L	RW	32	0x0000 00F8	0x5201 04F8
RZA_SDR_C_OFT	RW	32	0x0000 00FC	0x5201 04FC
RZA_SDR_C_PTR_S	RW	32	0x0000 0100	0x5201 0500
RZA_SDR_C_PTR_E	RW	32	0x0000 0104	0x5201 0504
RZB_EN	RW	32	0x0000 0108	0x5201 0508
RZB_MODE	RW	32	0x0000 010C	0x5201 050C
RZB_420	RW	32	0x0000 0110	0x5201 0510
RZB_I_VPS	RW	32	0x0000 0114	0x5201 0514
RZB_I_HPS	RW	32	0x0000 0118	0x5201 0518
RZB_O_VSZ	RW	32	0x0000 011C	0x5201 051C
RZB_O_HSZ	RW	32	0x0000 0120	0x5201 0520
RZB_V_PHS_Y	RW	32	0x0000 0124	0x5201 0524
RZB_V_PHS_C	RW	32	0x0000 0128	0x5201 0528
RZB_V_DIF	RW	32	0x0000 012C	0x5201 052C
RZB_V_TYP	RW	32	0x0000 0130	0x5201 0530
RZB_V_LPF	RW	32	0x0000 0134	0x5201 0534
RZB_H_PHS	RW	32	0x0000 0138	0x5201 0538
RZB_H_PHS_ADJ	RW	32	0x0000 013C	0x5201 053C
RZB_H_DIF	RW	32	0x0000 0140	0x5201 0540
RZB_H_TYP	RW	32	0x0000 0144	0x5201 0544
RZB_H_LPF	RW	32	0x0000 0148	0x5201 0548
RZB_DWN_EN	RW	32	0x0000 014C	0x5201 054C
RZB_DWN_AV	RW	32	0x0000 0150	0x5201 0550
RZB_RGB_EN	RW	32	0x0000 0154	0x5201 0554
RZB_RGB_TYP	RW	32	0x0000 0158	0x5201 0558
RZB_RGB_BLD	RW	32	0x0000 015C	0x5201 055C
RZB_SDR_Y_BAD_H	RW	32	0x0000 0160	0x5201 0560
RZB_SDR_Y_BAD_L	RW	32	0x0000 0164	0x5201 0564
RZB_SDR_Y_SAD_H	RW	32	0x0000 0168	0x5201 0568
RZB_SDR_Y_SAD_L	RW	32	0x0000 016C	0x5201 056C
RZB_SDR_Y_OFT	RW	32	0x0000 0170	0x5201 0570
RZB_SDR_Y_PTR_S	RW	32	0x0000 0174	0x5201 0574
RZB_SDR_Y_PTR_E	RW	32	0x0000 0178	0x5201 0578
RZB_SDR_C_BAD_H	RW	32	0x0000 017C	0x5201 057C

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Table 8-553. ISS RESIZER Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_RESIZER Base Address
RZB_SDR_C_BAD_L	RW	32	0x0000 0180	0x5201 0580
RZB_SDR_C_SAD_H	RW	32	0x0000 0184	0x5201 0584
RZB_SDR_C_SAD_L	RW	32	0x0000 0188	0x5201 0588
RZB_SDR_C_OFT	RW	32	0x0000 018C	0x5201 058C
RZB_SDR_C_PTR_S	RW	32	0x0000 0190	0x5201 0590
RZB_SDR_C_PTR_E	RW	32	0x0000 0194	0x5201 0594

8.3.5.4.2 ISS RESIZER Register Description

Table 8-554. RSZ_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5201 0400	**Instance**	ISS_RESIZER
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See(1)

(1) TI internal data

Table 8-555. Register Call Summary for Register RSZ_REVISION

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-556. RSZ_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x5201 0404	**Instance**	ISS_RESIZER
Description	SYSTEM CONFIGURATION REGISTER This register is not shadowed. There is no standalone software reset for the resizer module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						RSZB_CLK_EN	RSZA_CLK_EN	RESERVED							AUTOGATING

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9	RSZB_CLK_EN	Resizer B clock enable This bit enable to enable / disable the RESIZER B clock. Note that it is a second level clock enable. This bit has effect only if RSZ_GCK_SDR is set to 1. 0x0: off 0x1: on	RW	0
8	RSZA_CLK_EN	Resizer A clock enable This bit enable to enable / disable the RESIZER A clock. Note that it is a second level clock enable. This bit has effect only if RSZ_GCK_SDR is set to 1. 0x0: off 0x1: on	RW	0
7:1	RESERVED		R	0x00
0	AUTOGATING	Internal Clock Gating Strategy Enables or disables auto clock gating. **NOTE:** This is only for debug purposes. When this bit is set to "0" autogating is not performed on any of the clocks, thus the clocks stay free running. Though, they are still controlled by the clock enable bit fields RSZA_CLK_EN and RSZB_CLK_EN. 0x0: Clocks are free running 0x1: Automatic clock gating strategy.	RW	1

Table 8-557. Register Call Summary for Register RSZ_SYSCONFIG

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Initial Register Setup: [1] [2]
- ISS ISP RSZ Programming Constraints: [3]
- ISS RESIZER Register Summary: [4]

Table 8-558. RSZ_IN_FIFO_CTRL

Address Offset	0x0000 000C		
Physical Address	0x5201 040C	**Instance**	ISS_RESIZER
Description	INPUT DATA BUFFER CONTROL REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRLD_LOW								RESERVED								THRLD_HIGH							

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	THRLD_LOW	When RSZ_IN_FIFO_CTRL.THRLD_HIGH = RSZ_IN_FIFO_CTRL.THRLD_LOW, the rsz_stall_input is not asserted. The only purpose of the RSZ_IN_FIFO_CTRL.THRLD_LOW register is to prevent rsz_stall_input signal assertion.	RW	0x0000
15:13	RESERVED		R	0x0
12:0	THRLD_HIGH	High threshold value. The rsz_stall_input signal is asserted if 2 lines of circular buffer are full and the third line has more pixels than RSZ_IN_FIFO_CTRL.THRLD_HIGH. The rsz_stall_input signal stays high as long as one full line is not free for receiving further data. THRLD_HIGH is in terms of line size and can at max be programmed equal to the input line size (RSZ_SRC_HSZ).	RW	0x0000

Table 8-559. Register Call Summary for Register RSZ_IN_FIFO_CTRL

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Initial Register Setup: [3] [4]
- ISS ISP RSZ Programming Constraints: [5]
- ISS RESIZER Register Summary: [6]
- ISS RESIZER Register Description: [7] [8] [9] [10]

Table 8-560. RSZ_GNC

Address Offset	0x0000 0010		
Physical Address	0x5201 0410	**Instance**	ISS_RESIZER
Description	GENERIC PARAMETER REGISTER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RSZB_MEM_LINE_SIZE								RESERVED								RSZA_MEM_LINE_SIZE							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	RSZB_MEM_LINE_SIZE	Resizer #B memory line size (pixels). The output image cannot exceed this size.	R	0x0920
15:13	RESERVED		R	0x0
12:0	RSZA_MEM_LINE_SIZE	Resizer #A memory line size (pixels). The output image cannot exceed this size.	R	0x1500

Table 8-561. Register Call Summary for Register RSZ_GNC

ISS ISP

- ISS ISP RSZ Operating Modes: [0]
- ISS RESIZER Register Summary: [3]

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Table 8-562. RSZ_FRACDIV

Address Offset	0x0000 0014		
Physical Address	0x5201 0414	**Instance**	ISS_RESIZER
Description	Fractional clock divider settings		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	RSZ_FRACDIV	Fractional clock divider value. The fractional clock divider gates the read requests made to the input data buffer such that the input data buffer is read at an average frequency equal to FFCLK instead of FCLK. The value of FFCLK depends upon the upscaling ratios as well as the input pixel clock: We have FFCLK = FCLK / FRACDIV MHz and RSZ_FRACDIV = 65536 / FRACDIV. When RSZ_ FRACDIV = 65536, we have: FFCLK = FCLK.	RW	0xFFFF

Table 8-563. Register Call Summary for Register RSZ_FRACDIV

ISS ISP

- ISS ISP RSZ Initial Register Setup: [0] [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [2] [3]
- ISS RESIZER Register Summary: [4]
- ISS RESIZER Register Description: [5] [6]

Table 8-564. RSZ_SRC_EN

Address Offset	0x0000 0020		
Physical Address	0x5201 0420	**Instance**	ISS_RESIZER
Description	RESIZER ENABLE REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	EN	Resizer module enable The start flag of the RESIZER module. When EN is set to 1, the RESIZER module starts the processing from the next rising edge of the VD pulse. If the processing mode of the RESIZER module is set to "one shot", the EN bit is cleared to 0 after the end of the processing. One has to pay attention that when this bit is enabled and 0x0: Disable 0x1: Enable	RW	0

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Table 8-565. Register Call Summary for Register RSZ_SRC_EN

ISS ISP

- ISS ISP RSZ Functional Description: [0]
- ISS ISP RSZ Initial Register Setup: [1]
- ISS ISP RSZ Reset Behavior: [2]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [3]
- ISS ISP RSZ Programming Constraints: [4]
- ISS RESIZER Register Summary: [5]

Table 8-566. RSZ_SRC_MODE

Address Offset	0x0000 0024		
Physical Address	0x5201 0424	**Instance**	ISS_RESIZER
Description	This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														WRT	OST

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	WRT	Video port WEN signal selection This bit selects whether the WEN signal which is present on the IPIPE and IPIPEIF video port is used or not to select the input data. If WRT is 0, the RESIZER module ignores the WEN signal and processes all image frame while RESIZER is enabled. If WRT is 1, the RESIZER module only processes the lines that arrived while the WEN is high. HD is used to sample the WEN signal. 0x0: Disable 0x1: Enable	RW	0
0	OST	The processing mode selection of the RESIZER module. Value 0 indicates the mode of free run, value 1 indicates the mode of one shot. 0x0: Free running 0x1: One shot	RW	0

Table 8-567. Register Call Summary for Register RSZ_SRC_MODE

ISS ISP

- ISS ISP RSZ Video Port Interfaces: [0]
- ISS ISP RSZ Functional Description: [1]
- ISS ISP RSZ Initial Register Setup: [2] [3]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [4]
- ISS ISP RSZ Programming Constraints: [5]
- ISS RESIZER Register Summary: [6]

Table 8-568. RSZ_SRC_FMT0

Address Offset	0x0000 0028		
Physical Address	0x5201 0428	**Instance**	ISS_RESIZER
Description	This register is not shadowed		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														BYPASS	SEL

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	BYPASS	Pass Through This bit enables or disables the RESIZER module pass through mode. The pass through mode can transfer images which are 8K pixel wide. When it is enabled, the input data buffer and the resizer engines are bypassed. 0x0: Pass through off = normal output mode, the input data buffer is used. 0x1: Pass through on = normal output mode, the input data buffer is bypassed.	RW	0
0	SEL	Input selection This bit selects which of the two video port is selected to push data through the RESIZER module. 0x0: IPIPE 0x1: IPIPEIF	RW	0

Table 8-569. Register Call Summary for Register RSZ_SRC_FMT0

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1] [2]
- ISS ISP RSZ Initial Register Setup: [3] [4]
- ISS ISP RSZ Programming Constraints: [5]
- ISS RESIZER Register Summary: [6]
- ISS RESIZER Register Description: [7] [8] [9] [10] [11]

Table 8-570. RSZ_SRC_FMT1

Address Offset	0x0000 002C		
Physical Address	0x5201 042C	**Instance**	ISS_RESIZER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CHR	COL	IN420	RAW

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000 0000
3	CHR	Cb/Cr order This bit indicates if Cb/Cr is flipped. This bit is referred by RGB output function. 0: Normal. Cb/Cr is in normal order. 1: Flipped. Cb/Cr is flipped. RGB output modules flips back Cb/Cr before applying YUV to RGB matrix.	RW	0
2	COL	Y/C selection This bit is valid only if the input data is YUV4:2:0 (IN420 = 1). It enables to specify where the data which is input to the RESIZER module is Luma or Chroma data. 0x0: Y data is input 0x1: Chroma data is input	RW	0

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Bits	Field Name	Description	Type	Reset
1	IN420	Chroma Format Selection This bit sets the chroma undersampling when YUV data is input to the RESIZER module. 0x0: YUV4:2:2 is input 0x1: YUV4:2:0 is input	RW	0
0	RAW	Pass-through mode input data format selection This bit affects the horizontal reversal (flipping) process. 0x0: Flipping preserves YCbCr format 0x1: Flipping preserves RAW format	RW	0

Table 8-571. Register Call Summary for Register RSZ_SRC_FMT1

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1] [2] [3]
- ISS ISP RSZ Color Converter: [4]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [5] [6]
- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1: [7]
- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2: [8]
- ISS RESIZER Register Summary: [9]

Table 8-572. RSZ_SRC_VPS

Address Offset	0x0000 0030		
Physical Address	0x5201 0430	**Instance**	ISS_RESIZER
Description	VERTICAL POSITION REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VPS															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	VPS	Vertical Start Position Sets the vertical position of the global frame from the rising edge of the VD. The RSZ module will start the image processing from the VPS'th line. This value can be odd or even whatever the input data format.	RW	0x0000

Table 8-573. Register Call Summary for Register RSZ_SRC_VPS

ISS ISP

- ISS ISP RSZ Input Data Cropper: [0]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS ISP RSZ Programming Constraints: [3]
- ISS RESIZER Register Summary: [4]

Table 8-574. RSZ_SRC_VSZ

Address Offset	0x0000 0034		
Physical Address	0x5201 0434	**Instance**	ISS_RESIZER
Description	VERTICAL SIZER REGISTER		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VSZ							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VSZ	Vertical Processing Size Sets the vertical size of the processing area. The RSZ module will process (VSZ+1) lines. This value can be odd or even whatever the input data format.	RW	0x0000

Table 8-575. Register Call Summary for Register RSZ_SRC_VSZ

ISS ISP

- ISS ISP RSZ Input Data Cropper: [0]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]
- ISS RESIZER Register Description: [4] [5]

Table 8-576. RSZ_SRC_HPS

Address Offset	0x0000 0038		
Physical Address	0x5201 0438	**Instance**	ISS_RESIZER
Description	HORIZONTAL POSITION REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HPS															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	HPS	Horizontal Start Position The RSZ_SRC_HPS register has two functions: The first function is to compensate for possible delay between the HD pulse and the first valid data. It is possible for this delay to be different than 0 when the RESIZER module gets its input data from the VP connected to the IPIPEIF module (the offset value can be odd or even). When data are coming from the IPIPE module, it is not required to resynchronize HD and the first valid data. The second function is to crop the data in the horizontal direction. When used for cropping, only RSZ_SRC_HPS must be even or null.	RW	0x0000

Table 8-577. Register Call Summary for Register RSZ_SRC_HPS

ISS ISP

- ISS ISP RSZ Input Data Cropper: [0]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS ISP RSZ Programming Constraints: [3]
- ISS RESIZER Register Summary: [4]
- ISS RESIZER Register Description: [5] [6]

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Table 8-578. RSZ_SRC_HSZ

Address Offset	0x0000 003C		
Physical Address	0x5201 043C	**Instance**	ISS_RESIZER
Description	HORIZONTAL SIZE REGISTER The HSZ value is given by HSZ concatenated with HSZ_LSB		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSZ															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	HSZ	Horizontal size Sets the horizontal size of the processing area. The RSZ module processes (HSZ+1) pixels. (HSZ+1) must be even for YUV4:2:2 and RAW data. The valid available values for HSZ are 1~xxxx.	RW	0x0000

Table 8-579. Register Call Summary for Register RSZ_SRC_HSZ

ISS ISP

- ISS ISP RSZ Input Data Cropper: [0] [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [2]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [3]
- ISS RESIZER Register Summary: [4]
- ISS RESIZER Register Description: [5]

Table 8-580. RSZ_DMA_RZA

Address Offset	0x0000 0040		
Physical Address	0x5201 0440	**Instance**	ISS_RESIZER
Description	RESIZER A - MEMORY REQUEST MINIMUM INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RZA															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	RZA	Sets the minimum interval btw two consecutive memory request for resizer #A. Specified in number of interface clock cycles. Values of 0, 1, and 2 are used as a condition to keep the bandwidth limiter off. When this function is enabled, this value must be greater than 10 cycles.	RW	0x0000

Table 8-581. Register Call Summary for Register RSZ_DMA_RZA

ISS ISP

- ISS ISP RSZ MTC Interfaces: [0]
- ISS ISP BL Peak Memory Bandwidth Reduction: [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [2]
- ISS RESIZER Register Summary: [3]

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Table 8-582. RSZ_DMA_RZB

Address Offset	0x0000 0044		
Physical Address	0x5201 0444	**Instance**	ISS_RESIZER
Description	RESIZER B - MEMORY REQUEST MINIMUM INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RZB															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	RZB	Sets the minimum interval btw two consecutive memory request for resizer #B. Specified in number of interface clock cycles. Values of 0, 1, and 2 are used as a condition to keep the bandwidth limiter off. When this function is enabled, this value must be greater than 10 cycles.	RW	0x0000

Table 8-583. Register Call Summary for Register RSZ_DMA_RZB

ISS ISP

- ISS ISP RSZ MTC Interfaces: [0]
- ISS ISP BL Peak Memory Bandwidth Reduction: [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [2]
- ISS RESIZER Register Summary: [3]

Table 8-584. RSZ_DMA_STA

Address Offset	0x0000 0048		
Physical Address	0x5201 0448	**Instance**	ISS_RESIZER
Description	RESIZER STATUS REGISTER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STATUS

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STATUS	Resizer process status This bit is set in the time window from rsz_int_reg to rsz_int_dma. Read 0x1: Active Read 0x0: Not active	R	0

Table 8-585. Register Call Summary for Register RSZ_DMA_STA

ISS ISP

- ISS ISP RSZ MTC Interfaces: [0]
- ISS RESIZER Register Summary: [1]

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Table 8-586. RSZ_GCK_MMR

Address Offset	0x0000 004C		
Physical Address	0x5201 044C	**Instance**	ISS_RESIZER
Description	MMR CLOCK CONTROL REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MMR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MMR	The on/off selection of the MMR interface clock which is used for MMR register access. 0x0: Off 0x1: On	RW	0

Table 8-587. Register Call Summary for Register RSZ_GCK_MMR

ISS ISP

- ISS ISP RSZ VBUSP Interface: [0]
- ISS ISP RSZ Initial Register Setup: [1]
- ISS ISP RSZ Programming Constraints: [2]
- ISS RESIZER Register Summary: [3]

Table 8-588. RSZ_GCK_SDR

Address Offset	0x0000 0054		
Physical Address	0x5201 0454	**Instance**	ISS_RESIZER
Description	CORE CLOCK CONTROL REGISTER This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CORE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	CORE	RSZ Core Clock Enable. This bit enables or disables the resizer core functional clock. When this bit is off, the resizer core (interpolator) is automatically bypassed (resizer-bypass mode of pass-through mode is selected depending on RSZ_SRC_FMT0 value). In resizer-bypass mode or pass-through mode, no up-scaling or downscaling process is operated. 0x0: Resizer core clock disabled. Resizer in bypass mode if RSZ_SRC_FMT0.BYPASS = 0 Resizer in pass-through if RSZ_SRC_FMT0.BYPASS = 1 0x1: Resizer core clock enabled. Resizer in rescaling mode if RSZ_SRC_FMT0.BYPASS = 0 Resizer in pass-through if RSZ_SRC_FMT0.BYPASS = 1	RW	0

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Table 8-589. Register Call Summary for Register RSZ_GCK_SDR

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Initial Register Setup: [2] [3] [4] [5]
- ISS ISP RSZ Programming Constraints: [6]
- ISS RESIZER Register Summary: [7]
- ISS RESIZER Register Description: [8] [9]

Table 8-590. RSZ_IRQ_RZA

Address Offset	0x0000 0058		
Physical Address	0x5201 0458	**Instance**	ISS_RESIZER
Description	RESIZER A - CIRCULAR BUFFER INTERRUPT INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RZA							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	RZA	Resizer A circular buffer interval Sets the circular buffer interval for Resizer A. The interrupt is triggered every time (RZA+1) lines are written to the circular buffer (Y buffer). The range goes from 1 to 8192 lines. Usually, the circular buffer vertical size should be a multiple of RZA.	RW	0x0000

Table 8-591. Register Call Summary for Register RSZ_IRQ_RZA

ISS ISP

- ISS ISP RSZ Interrupts: [0] [1] [2]
- ISS ISP RSZ Initial Register Setup: [3]
- ISS ISP5 SYS1 Register Description: [4] [5] [6] [7] [8] [9] [10] [11]
- ISS RESIZER Register Summary: [12]

Table 8-592. RSZ_IRQ_RZB

Address Offset	0x0000 005C		
Physical Address	0x5201 045C	**Instance**	ISS_RESIZER
Description	RESIZER B - CIRCULAR BUFFER INTERRUPT INTERVAL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RZB							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	RZB	Resizer B circular buffer interval Sets the circular buffer interval for Resizer B. The interrupt is triggered every time (RZB+1) lines are written to the circular buffer (Y buffer). The range goes from 1 to 8192 lines. Usually, the circular buffer vertical size should be a multiple of RZB.	RW	0x0000

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Table 8-593. Register Call Summary for Register RSZ_IRQ_RZB

ISS ISP

- ISS ISP RSZ Interrupts: [0]
- ISS ISP RSZ Initial Register Setup: [1]
- ISS ISP5 SYS1 Register Description: [2] [3] [4] [5] [6] [7] [8] [9]
- ISS RESIZER Register Summary: [10]

Table 8-594. RSZ_YUV_Y_MIN

Address Offset	0x0000 0060		
Physical Address	0x5201 0460	**Instance**	ISS_RESIZER
Description	LUMINANCE SATURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MIN							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	MIN	The minimum value of Luminance (8bits unsigned). If the value of the Luminance is smaller than VAL, it will be clipped to VAL. This bit field must be set to its default values when the resizer is set in pass-though mode.	RW	0x00

Table 8-595. Register Call Summary for Register RSZ_YUV_Y_MIN

ISS ISP

- ISS ISP RSZ Data Saturator: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

Table 8-596. RSZ_YUV_Y_MAX

Address Offset	0x0000 0064		
Physical Address	0x5201 0464	**Instance**	ISS_RESIZER
Description	LUMINANCE SATURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MAX							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	MAX	The maximum value of Luminance (8bits unsigned). If the value of the Luminance is larger than VAL, it will be clipped to VAL. This bit field must be set to its default values when the resizer is set in pass-through mode.	RW	0xFF

Table 8-597. Register Call Summary for Register RSZ_YUV_Y_MAX

ISS ISP

- ISS ISP RSZ Data Saturator: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

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Table 8-598. RSZ_YUV_C_MIN

Address Offset	0x0000 0068		
Physical Address	0x5201 0468	**Instance**	ISS_RESIZER
Description	CHROMINANCE SATURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MIN							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	MIN	The minimum value of Chrominance (8bits unsigned). If the value of the Chrominance is smaller than VAL, it will be clipped to VAL. This bit field must be set to its default values when the resizer is set in pass-though mode.	RW	0x00

Table 8-599. Register Call Summary for Register RSZ_YUV_C_MIN

ISS ISP

- ISS ISP RSZ Data Saturator: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

Table 8-600. RSZ_YUV_C_MAX

Address Offset	0x0000 006C		
Physical Address	0x5201 046C	**Instance**	ISS_RESIZER
Description	CHROMINANCE SATURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MAX							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	MAX	The maximum value of Chrominance (8bits unsigned). If the value of the Chrominance is larger than VAL, it will be clipped to VAL. This bit field must be set to its default values when the resizer is set in pass-through mode.	RW	0xFF

Table 8-601. Register Call Summary for Register RSZ_YUV_C_MAX

ISS ISP

- ISS ISP RSZ Data Saturator: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [2]
- ISS RESIZER Register Summary: [3]

Table 8-602. RSZ_YUV_PHS

Address Offset	0x0000 0070		
Physical Address	0x5201 0470	**Instance**	ISS_RESIZER
Description	The phase position of the output of the Chrominance		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															POS

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	POS	The phase position of the output of the chrominance. The RESIZER module does not change the relative position of the chroma samples vs. the luma samples between the input and output and the chroma position at the output of the IPIPE module and at the output of the RESIZER module must be identical. In other words, we must have RSZ_YUV_PHS.POS = IPIPE_YUV_PHS.POS. 0x0: Same position with Luminance: cosited 0x1: The middle of the luminance: centered	RW	0

Table 8-603. Register Call Summary for Register RSZ_YUV_PHS

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1: [2]
- ISS RESIZER Register Summary: [3]
- ISS RESIZER Register Description: [4]
- ISS IPIPE Register Description: [5]

Table 8-604. RSZ_SEQ

Address Offset	0x0000 0074		
Physical Address	0x5201 0474	**Instance**	ISS_RESIZER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											CRV	VRVB	HRVB	VRVA	HRVA

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	CRV	Chroma sampling point change 0x0: Chroma sampling point is not changed 0x1: Chroma sampling point is changed from odd-numbered pixels to even-number pixels. The pixel at the left end is removed and the pixel at the right end is duplicated.	RW	0
3	VRVB	Resizer B - Vertical reversal of output image 0x0: Processed pixels are output in the order of input (normal operation) in vertical direction. 0x1: The order of output data is flipped top to bottom.	RW	0
2	HRVB	Resizer B -Horizontal reversal of output image 0x0: Processed pixels are output in the order of input (normal operation) in horizontal direction. 0x1: The order of output data is flipped left to right.	RW	0

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Bits	Field Name	Description	Type	Reset
1	VRVA	Resizer A - Vertical reversal of output image 0x0: Processed pixels are output in the order of input (normal operation) in vertical direction. 0x1: The order of output data is flipped top to bottom.	RW	0
0	HRVA	Resizer A - Horizontal reversal of output image 0x0: Processed pixels are output in the order of input (normal operation) in horizontal direction. 0x1: The order of output data is flipped left to right.	RW	0

Table 8-605. Register Call Summary for Register RSZ_SEQ

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1]
- ISS ISP RSZ Global Image Processing Settings: [2] [3] [4] [5]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 2: [6] [7]
- ISS RESIZER Register Summary: [8]

Table 8-606. RZA_EN

Address Offset	0x0000 0078		
Physical Address	0x5201 0478	**Instance**	ISS_RESIZER
Description	RESIZER A - ENABLE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	EN	Enable resizer #A This bit is latched on video port VD input. The reason is that the resizer must only starts the processing on a clean frame boundary. In one-shot mode, this bit is negated on VD. 0x0: Disable 0x1: Enable	RW	0

Table 8-607. Register Call Summary for Register RZA_EN

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1] [2] [3] [4]
- ISS ISP RSZ Initial Register Setup: [5]
- ISS RESIZER Register Summary: [6]

Table 8-608. RZA_MODE

Address Offset	0x0000 007C		
Physical Address	0x5201 047C	**Instance**	ISS_RESIZER
Description	RESIZER #A MODE REGISTER		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MODE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MODE	Select "Free Run mode" or "One Shot Mode" 0x0: Free run 0x1: One shot	RW	0

Table 8-609. Register Call Summary for Register RZA_MODE

ISS ISP
- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-610. RZA_420

Address Offset	0x0000 0080		
Physical Address	0x5201 0480	**Instance**	ISS_RESIZER
Description	YEN/CEN: 0/0: in = YUV4:2:2 input, out = YUV4:2:2 output 0/1: in = YUV4:2:2 input, out = Chrominance of YUV4:2:0 output 1/0: in = YUV4:2:2 input, out = Luminance of YUV4:2:0 output 1/1: in = YUV4:2:2 input, out = YUV4:2:0 output		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CEN	YEN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	CEN	Output Enable for Chrominance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422 0x0: C output disable 0x1: C output enable and 422to420 conversion enabled	RW	0
0	YEN	Output Enable for Luminance. This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422 0x0: Y output disable 0x1: Y output enable and 422to420 conversion enabled	RW	0

Table 8-611. Register Call Summary for Register RZA_420

ISS ISP
- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [0] [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 2: [2] [3]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [4] [5]
- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1: [6] [7]
- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2: [8] [9]
- ISS RESIZER Register Summary: [10]
- ISS RESIZER Register Description: [11] [12]

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Table 8-612. RZA_I_VPS

Address Offset	0x0000 0084		
Physical Address	0x5201 0484	**Instance**	ISS_RESIZER
Description	RESIZER A - INPUT VERTICAL START REGISTER The height of the image after the second level crop must be 2 or larger.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VPS							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VPS	Input Vertical Position Sets the vertical start position of the input image within the global frame. It enables to crop data into the global frame. After SRC_VPS, the Vps'th line is processed as the first line in each image. After the second level crop, the height of the image area must be two lines or larger; that is, a one-line image is not allowed. (RSZ_SRC_VSZ – RZA_I_VPS > 0).	RW	0x0000

Table 8-613. Register Call Summary for Register RZA_I_VPS

ISS ISP

- ISS ISP RSZ Input Data Cropper: [0]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]
- ISS RESIZER Register Description: [3]

Table 8-614. RZA_I_HPS

Address Offset	0x0000 0088		
Physical Address	0x5201 0488	**Instance**	ISS_RESIZER
Description	RESIZER A - INPUT HORIZONTAL START REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								HPS							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	HPS	Input Horizontal Position Sets the horizontal position of the first pixel for each line within the global frame. After SRC_HPS, the pixel at the VAL'th position is processed as the first pixel. This value must be even.	RW	0x0000

Table 8-615. Register Call Summary for Register RZA_I_HPS

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

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Table 8-616. RZA_O_VSZ

Address Offset	0x0000 008C		
Physical Address	0x5201 048C	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT VERTICAL SIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VSZ							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VSZ	The target output size of the resized image. The number of output lines is (VSZ+1). Set 479, when 480 lines of output is required.	RW	0x0000

Table 8-617. Register Call Summary for Register RZA_O_VSZ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-618. RZA_O_HSZ

Address Offset	0x0000 0090		
Physical Address	0x5201 0490	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT HORIZONTAL SIZE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								HSZ							HSZ_LSB

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:1	HSZ	The horizontal size of output image. The number of pixel in each line is (HSZ+1). Set 479, when 480 pixels are required. This value must be lower than the max memory line size supported by the resizer engine, except in RAW pass through mode. Note that the LSB of the 13-bit HSZ value is fixed to 1 such that the horizontal size is always even.	RW	0x000
0	HSZ_LSB	The least significant bit of HSZ is forced to 1.	R	1

Table 8-619. Register Call Summary for Register RZA_O_HSZ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

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Table 8-620. RZA_V_PHS_Y

Address Offset	0x0000 0094		
Physical Address	0x5201 0494	**Instance**	ISS_RESIZER
Description	RESIZER A - INITIAL LUMINANCE PHASE OF VERTICAL RESIZING PROCESS When YUV4:2:2 data are output, the phase values for luma and chroma should typically be equal, that is, RZX_V_PHS_Y= RZX_V_PHS_C. The following constraints apply when setting the initial vertical phases ABS(RZX_V_PHS_Y - RZX_V_PHS_C) RZX_V_DIF. This constraint means that at most the distance between the initial phases for luminance and chrominance is not expected to exceed the distance between two luma pixels. Note that the absolute value is used, hence, the initial luma phase can be greater than the initial chroma phase or the other way around. As a reminder, the distance between two output pixels for luma is given by RZX_V_DIF.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								Y							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	Y	The initial value for the luma phase in vertical resizing process. This value is in U14Q8 fractional format.	RW	0x0000

Table 8-621. Register Call Summary for Register RZA_V_PHS_Y

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-622. RZA_V_PHS_C

Address Offset	0x0000 0098		
Physical Address	0x5201 0498	**Instance**	ISS_RESIZER
Description	RESIZER A - INITIAL CHROMINANCE PHASE OF VERTICAL RESIZING PROCESS When YUV4:2:2 data are output, the phase values for luma and chroma should typically be equal, that is, RZX_V_PHS_Y= RZX_V_PHS_C. The following constraints apply when setting the initial vertical phases ABS(RZX_V_PHS_Y - RZX_V_PHS_C) RZX_V_DIF. This constraint means that at most the distance between the initial phases for luminance and chrominance is not expected to exceed the distance between two luma pixels. Note that the absolute value is used, hence, the initial luma phase can be greater than the initial chroma phase or the other way around. As a reminder, the distance between two output pixels for luma is given by RZX_V_DIF.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	C	The initial value for the chroma phase in vertical resizing process. This value is in U14Q8 fractional format.	RW	0x0000

Table 8-623. Register Call Summary for Register RZA_V_PHS_C

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1: [0] [1]
- ISS RESIZER Register Summary: [2]

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Table 8-624. RZA_V_DIF

Address Offset	0x0000 009C		
Physical Address	0x5201 049C	**Instance**	ISS_RESIZER
Description	RESIZER A - VERTICAL RESIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								V							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	V	The parameter for vertical resize. The actual resizing ratio is 256/RZA_V_DIF. In normal mode: 16 <= RZA_V_DIF <= 4096. In down-scale mode: 256 <= RZA_V_DIF <= 4096.	RW	0x0000

Table 8-625. Register Call Summary for Register RZA_V_DIF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]
- ISS RESIZER Register Description: [2] [3] [4]

Table 8-626. RZA_V_TYP

Address Offset	0x0000 00A0		
Physical Address	0x5201 04A0	**Instance**	ISS_RESIZER
Description	RESIZER A - INTERPOLATION METHOD FOR VERTICAL RESIZING		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														C	Y

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	C	Selection of resizing method for chrominance: vertical 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0
0	Y	Selection of resizing method for luminance: vertical 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0

Table 8-627. Register Call Summary for Register RZA_V_TYP

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

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Table 8-628. RZA_V_LPF

Address Offset	0x0000 00A4		
Physical Address	0x5201 04A4	**Instance**	ISS_RESIZER
Description	RESIZER A - VERTICAL LPF INTENSITY REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				C						Y					

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:6	C	The intensity parameter for chroma vertical low pass filtering.	RW	0x00
5:0	Y	The intensity parameter for luma vertical low pass filtering.	RW	0x00

Table 8-629. Register Call Summary for Register RZA_V_LPF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-630. RZA_H_PHS

Address Offset	0x0000 00A8		
Physical Address	0x5201 04A8	**Instance**	ISS_RESIZER
Description	RESIZER A - INITIAL PHASE OF HORIZONTAL RESIZING PROCESS		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PHS							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	PHS	Initial value for the phase in horizontal resizing process, that is, the sampling position is shifted. This value is in U14Q8 fractional format. Example: If RZX_H_PHS = 128, the first output pixel is sampled at the center of the first two valid input pixels. If RZX_I_HPS=100 and RZX_H_PHS=128, the first output pixel is resampled at the center of the 100-th and the 101-st input pixels.	RW	0x0000

Table 8-631. Register Call Summary for Register RZA_H_PHS

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1: [0]
- ISS RESIZER Register Summary: [1]

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Table 8-632. RZA_H_PHS_ADJ

Address Offset	0x0000 00AC		
Physical Address	0x5201 04AC	**Instance**	ISS_RESIZER
Description	RESIZER A - LUMINANCE HORIZONTAL PHASE ADJUSTMENT The RZA_H_PHS_ADJ register enables to adjust the horizontal phase for the luma component when averaging is enabled (the horizontal averaging disrupts the relative sampling point between luminance and chrominance when YUV4:2:2 cosited data is input), that is, the relative phase between luma and chroma is different before and after the horizontal averager.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADJ							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8:0	ADJ	Horizontal phase adjustment value. This value is in U9Q8 fractional format. This value is expected to be equal to zero if the averager is disabled or if input chroma is centered.	RW	0x000

Table 8-633. Register Call Summary for Register RZA_H_PHS_ADJ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1: [0]
- ISS RESIZER Register Summary: [1]
- ISS RESIZER Register Description: [2] [3]
- ISS IPIPE Register Description: [4]

Table 8-634. RZA_H_DIF

Address Offset	0x0000 00B0		
Physical Address	0x5201 04B0	**Instance**	ISS_RESIZER
Description	RESIZER A - HORIZONTAL RESIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								H							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	H	The parameter for horizontal resizing process. The actual resizing ratio is 256/VAL. In normal mode 16<= RSZ_RZA_H_DIF<=4096 In down-scale mode 256<=RSZ_RZA_H_DIF<=4096	RW	0x0000

Table 8-635. Register Call Summary for Register RZA_H_DIF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]
- ISS RESIZER Register Description: [2] [3] [4] [5]

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Table 8-636. RZA_H_TYP

Address Offset	0x0000 00B4		
Physical Address	0x5201 04B4	**Instance**	ISS_RESIZER
Description	Resize-A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														C	Y

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	C	Selection of resizing method for chrominance: horizontal 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0
0	Y	Selection of resizing method for luminance: horizontal 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0

Table 8-637. Register Call Summary for Register RZA_H_TYP

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-638. RZA_H_LPF

Address Offset	0x0000 00B8		
Physical Address	0x5201 04B8	**Instance**	ISS_RESIZER
Description	RESIZER A - HORIZONTAL LPF INTENSITY REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				C				Y							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:6	C	Horizontal LPF Intensity for Chrominance	RW	0x00
5:0	Y	Selection of resizing method for Luminance in horizontal direction	RW	0x00

Table 8-639. Register Call Summary for Register RZA_H_LPF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-640. RZA_DWN_EN

Address Offset	0x0000 00BC		
Physical Address	0x5201 04BC	**Instance**	ISS_RESIZER
Description	RESIZER #A - DOWNSCALE ENABLE REGISTER		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DWN_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DWN_EN	Resizer downscale enable 0x0: Off. Normal operation: upscale and downscale are allowed. 0x1: On. Downscale mode.	RW	0

Table 8-641. Register Call Summary for Register RZA_DWN_EN

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1: [0]
- ISS RESIZER Register Summary: [1]

Table 8-642. RZA_DWN_AV

Address Offset	0x0000 00C0		
Physical Address	0x5201 04C0	**Instance**	ISS_RESIZER
Description	Resize-A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											V			H	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:3	V	Vertical averaging size : $1/2^{(VWT+1)}$ The range goes from 1/2 to 1/256 in power of two. 0:_DIV2 1/2 down scale 1:_DIV4 1/4 down scale 2:_DIV8 1/8 down scale 3:_DIV16 1/16 down scale 4:_DIV32 1/32 down scale 5:_DIV64 1/64 down scale 6:_DIV128 1/128 down scale 7:_DIV256 1/256 down scale	RW	0x0
2:0	H	Horizontal averaging size : $1/2^{(HWT+1)}$ The range goes from 1/2 to 1/256 in power of two. 0:_DIV2 1/2 down scale 1:_DIV4 1/4 down scale 2:_DIV8 1/8 down scale 3:_DIV16 1/16 down scale 4:_DIV32 1/32 down scale 5:_DIV64 1/64 down scale 6:_DIV128 1/128 down scale 7:_DIV256 1/256 down scale	RW	0x0

Table 8-643. Register Call Summary for Register RZA_DWN_AV

ISS ISP

- ISS ISP RSZ Averager: [0] [1]
- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 1: [2] [3]
- ISS RESIZER Register Summary: [4]

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Table 8-644. RZA_RGB_EN

Address Offset	0x0000 00C4		
Physical Address	0x5201 04C4	**Instance**	ISS_RESIZER
Description	RESIZER #A - RGB OUTPUT ENABLE		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RGB_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RGB_EN	Enable of RGB output In pass through mode, this register must be 0. This bit can only be set to 1 when YUV4:2:2 data are output. YUV4:2:2 data output is selected when SRC_FMT1.IN420 = 0 and RZA_420.YEN = RZA_420.CEN = 0 0x0: Off (YCbCr output) 0x1: On (RGB output)	RW	0

Table 8-645. Register Call Summary for Register RZA_RGB_EN

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2: [0]
- ISS RESIZER Register Summary: [1]

Table 8-646. RZA_RGB_TYP

Address Offset	0x0000 00C8		
Physical Address	0x5201 04C8	**Instance**	ISS_RESIZER
Description	RESIZER A - RGB OUTPUT CONTROL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MSK1	MSK0	TYP

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	MSK1	Enables masking of the last 2 pixels This bit is used to mask the 2 last pixels at the image boundary which are affected by the YUV4:2:2 to YUV4:4:4 conversion. 0x0: output the last 2 pixels 0x1: mask the last 2 pixels (Resizer do not output them.)	RW	0
1	MSK0	Enables masking of the first 2 pixels This bit is used to mask the 2 first pixels at the image boundary which are affected by the YUV4:2:2 to YUV4:4:4 conversion. 0x0: output the first 2 pixels 0x1: mask the first 2 pixels (Resizer do not output them.)	RW	0

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Bits	Field Name	Description	Type	Reset
0	TYP	16bit/32bit output selection 0x0: 32-bit output: alpha + R + G + B (8 bit each) This mode comes with performance degradation. The maximum input frequency in this mode is 160 MHz. This due to the fact that the output is 4 bytes / pixel. 0x1: 16-bit output: R(5 bit) + G (6 bit) + B (5 bit)	RW	0

Table 8-647. Register Call Summary for Register RZA_RGB_TYP

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2: [0] [1] [2]
- ISS RESIZER Register Summary: [3]

Table 8-648. RZA_RGB_BLD

Address Offset	0x0000 00CC		
Physical Address	0x5201 04CC	**Instance**	ISS_RESIZER
Description	RESIZER A - RGB BLEND REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BLD							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	BLD	The alpha value used in 32-bit RGBA output mode	RW	0x00

Table 8-649. Register Call Summary for Register RZA_RGB_BLD

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings – Subsequence 2: [0]
- ISS RESIZER Register Summary: [1]

Table 8-650. RZA_SDR_Y_BAD_H

Address Offset	0x0000 00D0		
Physical Address	0x5201 04D0	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY BASE ADDRESS REGISTER (HIGH) This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_BAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_BAD_H	Memory Base Address Sets the 16 upper bits of the 32-bit base address of the circular buffer in memory.	RW	0x0000

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Table 8-651. Register Call Summary for Register RZA_SDR_Y_BAD_H

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-652. RZA_SDR_Y_BAD_L

Address Offset	0x0000 00D4		
Physical Address	0x5201 04D4	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY BASE ADDRESS REGISTER (LOW) This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_BAD_L															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_BAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit base address of the circular buffer in memory. It is a byte address. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RAW, RGB5:6:5 and YUV4:2:2 formats (output data on 16 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RGBA format (output data on 32 bits): The three least significant bits must be set to "000" when horizontal reversal mode is off. The three least significant bits must be set to "111" when horizontal reversal mode is on.	RW	0x0000

Table 8-653. Register Call Summary for Register RZA_SDR_Y_BAD_L

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-654. RZA_SDR_Y_SAD_H

Address Offset	0x0000 00D8		
Physical Address	0x5201 04D8	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER (HIGH) This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_SAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_SAD_H	Memory Start Address Sets the 16 upper bits of the 32-bit start address in memory.	RW	0x0000

Table 8-655. Register Call Summary for Register RZA_SDR_Y_SAD_H

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-656. RZA_SDR_Y_SAD_L

Address Offset	0x0000 00DC		
Physical Address	0x5201 04DC	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER (LOW) This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_SAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_SAD_L	Memory Start Address Sets 16 lower bits of the 32-bit start address in memory. It is a byte address. For every frame, the first line of data will be written to this address. We have: SAD = BAD + (PTR_S x OFT) and PTR_S < PTR_E If the first line must be written at the beginning of the circular buffer memory then SAD = BAD and PTR_S = 0. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RAW, RGB5:6:5 and YUV4:2:2 formats (output data on 16 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RGBA format (output data on 32 bits): The three least significant bits must be set to "000" when horizontal reversal mode is off. The three least significant bits must be set to "111" when horizontal reversal mode is on.	RW	0x0000

Table 8-657. Register Call Summary for Register RZA_SDR_Y_SAD_L

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 2: [2]
- ISS RESIZER Register Summary: [3]

Table 8-658. RZA_SDR_Y_OFT

Address Offset	0x0000 00E0		
Physical Address	0x5201 04E0	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY OFFSET REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_OFT															

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16:0	Y_OFT	Memory Line Offset Sets the size of each line in the circular buffer. It is expressed in bytes and unsigned. Note that OFT does not necessary corresponds to the size of a line in a frame, it can be much bigger. The line offset must be a multiple of 128 bytes (bits [6:0] of RZX_SDR_Y_OFT and RZX_SDR_C_OFT must be set to 0). Example: line 0 address = SAD line 1 address = SAD + 1 x OFT line 2 address = SAD + 2 x OFT	RW	0x00000

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Table 8-659. Register Call Summary for Register RZA_SDR_Y_OFT

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-660. RZA_SDR_Y_PTR_S

Address Offset	0x0000 00E4		
Physical Address	0x5201 04E4	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			Y_PTR_S												

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	Y_PTR_S	Start Line of Memory Pointer Sets the vertical position of the first output line in the output memory space. This value is expressed in number of lines. The hardware uses it to set up the initial value of the circular buffer. It must be set up such as PTR_S = (SAD - BAD) / OFT. This value must be set to 0 when RSZ_RZA_SDR_Y_BAD = RSZ_RZA_SDR_Y_SAD.	RW	0x0000

Table 8-661. Register Call Summary for Register RZA_SDR_Y_PTR_S

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-662. RZA_SDR_Y_PTR_E

Address Offset	0x0000 00E8		
Physical Address	0x5201 04E8	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY END ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			Y_PTR_E												

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	Y_PTR_E	End Line of Memory Pointer Sets the maximum number of lines to be stored in the output memory space. This value is expressed in number of lines. When the number of output lines exceeds this value, the address restarts from the first address in the output memory space (BAD).	RW	0x0000

Table 8-663. Register Call Summary for Register RZA_SDR_Y_PTR_E

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP5 SYS1 Register Description: [2] [3] [4] [5]
- ISS RESIZER Register Summary: [6]

Table 8-664. RZA_SDR_C_BAD_H

Address Offset	0x0000 00EC		
Physical Address	0x5201 04EC	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY BASE ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_BAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_BAD_H	Memory Base Address Sets the 16 higher bits of the 32-bit base address of the circular buffer in memory.	RW	0x0000

Table 8-665. Register Call Summary for Register RZA_SDR_C_BAD_H

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-666. RZA_SDR_C_BAD_L

Address Offset	0x0000 00F0		
Physical Address	0x5201 04F0	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY BASE ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_BAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_BAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit base address of the circular buffer in memory. It is a byte address. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on.	RW	0x0000

Table 8-667. Register Call Summary for Register RZA_SDR_C_BAD_L

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-668. RZA_SDR_C_SAD_H

Address Offset	0x0000 00F4		
Physical Address	0x5201 04F4	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_SAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_SAD_H	Memory Base Address Sets the 16 higher bits of the 32-bit start address in memory.	RW	0x0000

Table 8-669. Register Call Summary for Register RZA_SDR_C_SAD_H

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-670. RZA_SDR_C_SAD_L

Address Offset	0x0000 00F8		
Physical Address	0x5201 04F8	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_SAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_SAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit start address in memory. It is a byte address. For every frame, the first line of data will be written to this address. We have: SAD = BAD + (PTR_S x OFT) and PTR_S PTR_E If the first line must be written at the beginning of the circular buffer memory then SAD = BAD and PTR_S = 0. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on.	RW	0x0000

Table 8-671. Register Call Summary for Register RZA_SDR_C_SAD_L

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 2: [2]
- ISS RESIZER Register Summary: [3]

Table 8-672. RZA_SDR_C_OFT

Address Offset	0x0000 00FC		
Physical Address	0x5201 04FC	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY OFFSET REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_OFT															

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16:0	C_OFT	Memory Line Offset Sets the size of each line in the circular buffer. It is expressed in bytes and unsigned. Note that OFT does not necessary corresponds to the size of a line in a frame, it can be much bigger. The line offset must be a multiple of 128 bytes (bits [6:0] of RZX_SDR_Y_OFT and RZX_SDR_C_OFT must be set to 0). Example: line 0 address = SAD line 1 address = SAD + 1 x OFT line 2 address = SAD + 2 x OFT	RW	0x00000

Table 8-673. Register Call Summary for Register RZA_SDR_C_OFT

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-674. RZA_SDR_C_PTR_S

Address Offset	0x0000 0100		
Physical Address	0x5201 0500	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C_PTR_S							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	C_PTR_S	Start Line of Memory Pointer Sets the vertical position of the first output line in the output memory space. This value is expressed in number of lines. The hardware uses it to set up the initial value of the circular buffer. It must be set up such as PTR_S = (SAD - BAD) / OFT. This value must be set to 0 when RSZ_RZA_SDR_C_BAD = RSZ_RZA_SDR_C_SAD.	RW	0x0000

Table 8-675. Register Call Summary for Register RZA_SDR_C_PTR_S

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-676. RZA_SDR_C_PTR_E

Address Offset	0x0000 0104		
Physical Address	0x5201 0504	**Instance**	ISS_RESIZER
Description	RESIZER A - OUTPUT MEMORY END ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C_PTR_E							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	C_PTR_E	End Line of Memory Pointer Sets the maximum number of lines to be stored in the output memory space. This value is expressed in number of lines. When the number of output lines exceeds this value, the address restarts from the first address in the output memory space (BAD).	RW	0x0000

Table 8-677. Register Call Summary for Register RZA_SDR_C_PTR_E

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-678. RZB_EN

Address Offset	0x0000 0108		
Physical Address	0x5201 0508	**Instance**	ISS_RESIZER
Description	RESIZER B - ENABLE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	EN	Enable resizer #A This bit is latched on the video port VD input signal. The reason is that the resizer must only starts the processing on a clean frame boundary. In one-shot mode, this bit is negated on VD. 0x0: Disable 0x1: Enable	RW	0

Table 8-679. Register Call Summary for Register RZB_EN

ISS ISP

- ISS ISP RSZ Functional Description: [0] [1] [2] [3] [4]
- ISS ISP RSZ Initial Register Setup: [5]
- ISS RESIZER Register Summary: [6]

Table 8-680. RZB_MODE

Address Offset	0x0000 010C		
Physical Address	0x5201 050C	**Instance**	ISS_RESIZER
Description	RESIZER B MODE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MODE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MODE	Select "Free Run mode" or "One Shot Mode" 0x0: Free run 0x1: One shot	RW	0

Table 8-681. Register Call Summary for Register RZB_MODE

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

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Table 8-682. RZB_420

Address Offset	0x0000 0110		
Physical Address	0x5201 0510	**Instance**	ISS_RESIZER
Description	YEN/CEN: 0/0: in = YUV4:2:2 input, out = YUV4:2:2 output 0/1: in = YUV4:2:2 input, out = Chrominance of YUV4:2:0 output 1/0: in = YUV4:2:2 input, out = Luminance of YUV4:2:0 output 1/1: in = YUV4:2:2 input, out = YUV4:2:0 output		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														CEN	YEN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	CEN	Output Enable for Chrominance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422 0x0: C output disable 0x1: C output enable and 422to420 conversion enabled	RW	0
0	YEN	Output Enable for Luminance. This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422 0x0: Y output disable 0x1: Y output enable and 422to420 conversion enabled	RW	0

Table 8-683. Register Call Summary for Register RZB_420

ISS ISP

- ISS ISP RSZ Global Image Processing Settings – Subsequence 1: [0] [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 2: [2] [3]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [4] [5]
- ISS RESIZER Register Summary: [6]
- ISS RESIZER Register Description: [7] [8]

Table 8-684. RZB_I_VPS

Address Offset	0x0000 0114		
Physical Address	0x5201 0514	**Instance**	ISS_RESIZER
Description	RESIZER B - INPUT VERTICAL START REGISTER The height of the image after the second level crop must be 2 or larger.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VPS							

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VPS	Input Vertical Position Sets the vertical start position of the input image within the global frame. It enables to crop data into the global frame. After SRC_VPS, the Vps'th line is processed as the first line in each image. After the second level crop, the height of the image area must be two lines or larger; that is, a one-line image is not allowed. (RSZ_SRC_VSZ – RZB_I_VPS > 0).	RW	0x0000

Table 8-685. Register Call Summary for Register RZB_I_VPS

ISS ISP

- ISS ISP RSZ Input Data Cropper: [0]
- ISS ISP RSZ Engines Interframe Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]
- ISS RESIZER Register Description: [3]

Table 8-686. RZB_I_HPS

Address Offset	0x0000 0118		
Physical Address	0x5201 0518	**Instance**	ISS_RESIZER
Description	RESIZER B - INPUT HORIZONTAL START REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HPS												

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	HPS	Input Horizontal Position Sets the horizontal position of the first pixel for each line within the global frame. After SRC_HPS, the pixel at the VAL'th position is processed as the first pixel. This value must be even.	RW	0x0000

Table 8-687. Register Call Summary for Register RZB_I_HPS

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-688. RZB_O_VSZ

Address Offset	0x0000 011C		
Physical Address	0x5201 051C	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT VERTICAL SIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			VSZ												

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VSZ	The target output size of the resized image. The number of output lines is (VSZ+1). Set 479, when 480 lines of output is required.	RW	0x0000

Table 8-689. Register Call Summary for Register RZB_O_VSZ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-690. RZB_O_HSZ

Address Offset	0x0000 0120		
Physical Address	0x5201 0520	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT HORIZONTAL SIZE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSZ															HSZ_LSB

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:1	HSZ	The horizontal size of output image. The number of pixel in each line is (HSZ+1). Set 479, when 480 pixels are required. This value must be lower than the max memory line size supported by the resizer engine, except in RAW pass through mode. Note that the LSB of the 13-bit HSZ value is fixed to 1 such that the horizontal size is always even.	RW	0x000
0	HSZ_LSB	The least significant bit of HSZ is forced to 1.	R	1

Table 8-691. Register Call Summary for Register RZB_O_HSZ

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-692. RZB_V_PHS_Y

Address Offset	0x0000 0124		
Physical Address	0x5201 0524	**Instance**	ISS_RESIZER
Description	RESIZER B - INITIAL LUMINANCE PHASE OF VERTICAL RESIZING PROCESS When YUV4:2:2 data are output, the phase values for luma and chroma should typically be equal, that is, RZX_V_PHS_Y= RZX_V_PHS_C. The following constraints apply when setting the initial vertical phases ABS(RZX_V_PHS_Y - RZX_V_PHS_C) RZX_V_DIF. This constraint means that at most the distance between the initial phases for luminance and chrominance is not expected to exceed the distance between two luma pixels. Note that the absolute value is used, hence, the initial luma phase can be greater than the initial chroma phase or the other way around. As a reminder, the distance between two output pixels for luma is given by RZX_V_DIF.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								Y							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	Y	The initial value for the luma phase in vertical resizing process. This value is in U14Q8 fractional format.	RW	0x0000

Table 8-693. Register Call Summary for Register RZB_V_PHS_Y

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-694. RZB_V_PHS_C

Address Offset	0x0000 0128		
Physical Address	0x5201 0528	**Instance**	ISS_RESIZER
Description	RESIZER B - INITIAL CHROMINANCE PHASE OF VERTICAL RESIZING PROCESS When YUV4:2:2 data are output, the phase values for luma and chroma should typically be equal, that is, RZX_V_PHS_Y= RZX_V_PHS_C. The following constraints apply when setting the initial vertical phases ABS(RZX_V_PHS_Y - RZX_V_PHS_C) RZX_V_DIF. This constraint means that at most the distance between the initial phases for luminance and chrominance is not expected to exceed the distance between two luma pixels. Note that the absolute value is used, hence, the initial luma phase can be greater than the initial chroma phase or the other way around. As a reminder, the distance between two output pixels for luma is given by RZX_V_DIF.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	C	The initial value for the chroma phase in vertical resizing process. This value is in U14Q8 fractional format.	RW	0x0000

Table 8-695. Register Call Summary for Register RZB_V_PHS_C

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-696. RZB_V_DIF

Address Offset	0x0000 012C		
Physical Address	0x5201 052C	**Instance**	ISS_RESIZER
Description	RESIZER B - VERTICAL RESIZER REGISTERR		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								V							

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Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	V	The parameter for vertical resize. The actual resizing ratio is 256/RZB_V_DIF. In normal mode: 16 <= RZB_V_DIF <= 4096. In down-scale mode: 256 <= RZB_V_DIF <= 4096.	RW	0x0000

Table 8-697. Register Call Summary for Register RZB_V_DIF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]
- ISS RESIZER Register Description: [2] [3] [4]

Table 8-698. RZB_V_TYP

Address Offset	0x0000 0130		
Physical Address	0x5201 0530	**Instance**	ISS_RESIZER
Description	RESIZER B - INTERPOLATION METHOD FOR VERTICAL RESIZING		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														C	Y

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	C	Selection of resizing method for chrominance: vertical 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0
0	Y	Selection of resizing method for luminance: vertical 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0

Table 8-699. Register Call Summary for Register RZB_V_TYP

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-700. RZB_V_LPF

Address Offset	0x0000 0134		
Physical Address	0x5201 0534	**Instance**	ISS_RESIZER
Description	RESIZER B - VERTICAL LPF INTENSITY REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				C				Y							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:6	C	The intensity parameter for chroma vertical low pass filtering.	RW	0x00

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Bits	Field Name	Description	Type	Reset
5:0	Y	The intensity parameter for luma vertical low pass filtering.	RW	0x00

Table 8-701. Register Call Summary for Register RZB_V_LPF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-702. RZB_H_PHS

Address Offset	0x0000 0138		
Physical Address	0x5201 0538	**Instance**	ISS_RESIZER
Description	RESIZER B - INITIAL PHASE OF HORIZONTAL RESIZING PROCESS		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PHS							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	PHS	Initial value for the phase in horizontal resizing process, that is, the sampling position is shifted. This value is in U14Q8 fractional format. Example: If RZX_H_PHS = 128, the first output pixel is sampled at the center of the first two valid input pixels. If RZX_I_HPS=100 and RZX_H_PHS=128, the first output pixel is resampled at the center of the 100-th and the 101-st input pixels.	RW	0x0000

Table 8-703. Register Call Summary for Register RZB_H_PHS

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-704. RZB_H_PHS_ADJ

Address Offset	0x0000 013C		
Physical Address	0x5201 053C	**Instance**	ISS_RESIZER
Description	RESIZER B - LUMINANCE HORIZONTAL PHASE ADJUSTMENT The RZA_H_PHS_ADJ register enables to adjust the horizontal phase for the luma component when averaging is enabled (the horizontal averaging disrupts the relative sampling point between luminance and chrominance when YUV4:2:2 cosited data is input), that is, the relative phase between luma and chroma is different before and after the horizontal averager.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADJ							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8:0	ADJ	Horizontal phase adjustment value. This value is in U9Q8 fractional format. This value is expected to be equal to zero if the averager is disabled or if input chroma is centered.	RW	0x000

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Table 8-705. Register Call Summary for Register RZB_H_PHS_ADJ

ISS ISP
- ISS RESIZER Register Summary: [0]
- ISS IPIPE Register Description: [1]

Table 8-706. RZB_H_DIF

Address Offset	0x0000 0140		
Physical Address	0x5201 0540	**Instance**	ISS_RESIZER
Description	RESIZER B - HORIZONTAL RESIZER REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																H															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	H	The parameter for horizontal resizing process. The actual resizing ratio is 256/VAL. In normal mode 16 <= RSZ_RZA_H_DIF<=4096 In down-scale mode 256<=RSZ_RZA_H_DIF<=4096	RW	0x0000

Table 8-707. Register Call Summary for Register RZB_H_DIF

ISS ISP
- ISS ISP RSZ Engines Interframe Image Processing Settings: [0]
- ISS RESIZER Register Summary: [1]

Table 8-708. RZB_H_TYP

Address Offset	0x0000 0144		
Physical Address	0x5201 0544	**Instance**	ISS_RESIZER
Description	RESIZER B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														C	Y

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	C	Selection of resizing method for chrominance: horizontal 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0
0	Y	Selection of resizing method for luminance: horizontal 0x0: 4-tap cubic convolution (default) 0x1: 2-tap linear interpolation	RW	0

Table 8-709. Register Call Summary for Register RZB_H_TYP

ISS ISP
- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

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Table 8-710. RZB_H_LPF

Address Offset	0x0000 0148		
Physical Address	0x5201 0548	**Instance**	ISS_RESIZER
Description	RESIZER B - HORIZONTAL LPF INTENSITY REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				C				Y							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:6	C	Horizontal LPF Intensity for Chrominance	RW	0x00
5:0	Y	Selection of resizing method for Luminance in horizontal direction	RW	0x00

Table 8-711. Register Call Summary for Register RZB_H_LPF

ISS ISP

- ISS ISP RSZ Engines Interframe Image Processing Settings: [0] [1]
- ISS RESIZER Register Summary: [2]

Table 8-712. RZB_DWN_EN

Address Offset	0x0000 014C		
Physical Address	0x5201 054C	**Instance**	ISS_RESIZER
Description	RESIZER B - DOWNSCALE ENABLE REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DWN_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DWN_EN	Resizer downscale enable 0x0: Off. Normal operation: upscale and downscale are allowed. 0x1: On. Downscale mode.	RW	0

Table 8-713. Register Call Summary for Register RZB_DWN_EN

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-714. RZB_DWN_AV

Address Offset	0x0000 0150		
Physical Address	0x5201 0550	**Instance**	ISS_RESIZER
Description	RESIZER B		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										V			H		

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:3	V	Vertical averaging size : $1/2^{(VWT+1)}$ The range goes from 1/2 to 1/256 in power of two. 0:_DIV2 1/2 down scale 1:_DIV4 1/4 down scale 2:_DIV8 1/8 down scale 3:_DIV16 1/16 down scale 4:_DIV32 1/32 down scale 5:_DIV64 1/64 down scale 6:_DIV128 1/128 down scale 7:_DIV256 1/256 down scale	RW	0x0
2:0	H	Horizontal averaging size : $1/2^{(HWT+1)}$ The range goes from 1/2 to 1/256 in power of two. 0:_DIV2 1/2 down scale 1:_DIV4 1/4 down scale 2:_DIV8 1/8 down scale 3:_DIV16 1/16 down scale 4:_DIV32 1/32 down scale 5:_DIV64 1/64 down scale 6:_DIV128 1/128 down scale 7:_DIV256 1/256 down scale	RW	0x0

Table 8-715. Register Call Summary for Register RZB_DWN_AV

ISS ISP
- ISS RESIZER Register Summary: [0]

Table 8-716. RZB_RGB_EN

Address Offset	0x0000 0154		
Physical Address	0x5201 0554	**Instance**	ISS_RESIZER
Description	RESIZER B - RGB OUTPUT ENABLE		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RGB_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RGB_EN	Enable of RGB output In pass through mode, this register must be 0. This bit can only be set to 1 when YUV4:2:2 data are output. YUV4:2:2 data output is selected when SRC_FMT1.IN420 = 0 and RZB_420.YEN = RZB_420.CEN = 0 0x0: Off (YCbCr output) 0x1: On (RGB output)	RW	0

Table 8-717. Register Call Summary for Register RZB_RGB_EN

ISS ISP
- ISS ISP RSZ Functional Description: [0]
- ISS RESIZER Register Summary: [1]

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Table 8-718. RZB_RGB_TYP

Address Offset	0x0000 0158		
Physical Address	0x5201 0558	**Instance**	ISS_RESIZER
Description	RESIZER B - RGB OUTPUT CONTROL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MSK1	MSK0	TYP

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	MSK1	Enables masking of the last 2 pixels This bit is used to mask the 2 last pixels at the image boundary which are affected by the YUV4:2:2 to YUV4:4:4 conversion. 0x0: output the last 2 pixels 0x1: mask the last 2 pixels (Resizer do not output them.)	RW	0
1	MSK0	Enables masking of the first 2 pixels This bit is used to mask the 2 first pixels at the image boundary which are affected by the YUV4:2:2 to YUV4:4:4 conversion. 0x0: output the first 2 pixels 0x1: mask the first 2 pixels (Resizer do not output them.)	RW	0
0	TYP	16bit/32bit output selection 0x0: 32-bit output: alpha + R + G + B (8 bit each) This mode comes with performance degradation. The maximum input frequency in this mode is 160 MHz. This due to the fact that the output is 4 bytes / pixel. 0x1: 16-bit output: R(5 bit) + G (6 bit) + B (5 bit)	RW	0

Table 8-719. Register Call Summary for Register RZB_RGB_TYP

ISS ISP

- ISS RESIZER Register Summary: [0]

Table 8-720. RZB_RGB_BLD

Address Offset	0x0000 015C		
Physical Address	0x5201 055C	**Instance**	ISS_RESIZER
Description	RESIZER B - RGB BLEND REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BLD							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	BLD	The alpha value used in 32-bit RGBA output mode	RW	0x00

Table 8-721. Register Call Summary for Register RZB_RGB_BLD

ISS ISP

- ISS RESIZER Register Summary: [0]

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Table 8-722. RZB_SDR_Y_BAD_H

Address Offset	0x0000 0160		
Physical Address	0x5201 0560	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY BASE ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_BAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_BAD_H	Memory Base Address Sets 16 upper bits of the 32-bit base address of the circular buffer in memory.	RW	0x0000

Table 8-723. Register Call Summary for Register RZB_SDR_Y_BAD_H

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-724. RZB_SDR_Y_BAD_L

Address Offset	0x0000 0164		
Physical Address	0x5201 0564	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY BASE ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_BAD_L															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_BAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit base address of the circular buffer in memory. It is a byte address. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RAW, RGB5:6:5 and YUV4:2:2 formats (output data on 16 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RGBA format (output data on 32 bits): The three least significant bits must be set to "000" when horizontal reversal mode is off. The three least significant bits must be set to "111" when horizontal reversal mode is on.	RW	0x0000

Table 8-725. Register Call Summary for Register RZB_SDR_Y_BAD_L

ISS ISP
- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-726. RZB_SDR_Y_SAD_H

Address Offset	0x0000 0168		
Physical Address	0x5201 0568	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_SAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_SAD_H	Memory Start Address Sets 16 upper bits of the 32-bit start address in memory.	RW	0x0000

Table 8-727. Register Call Summary for Register RZB_SDR_Y_SAD_H

ISS ISP
- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-728. RZB_SDR_Y_SAD_L

Address Offset	0x0000 016C		
Physical Address	0x5201 056C	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0, RGB5:6:5, RGBA. RAW: RAW data is written to this address YUV4:2:2: YUV data is written to this address YUV4:2:0: Y data is written to this address RGB5:6:5: 16-bit RGB data is written to this address RGBA: 32-bit RGBA data is written to this address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_SAD_L															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	Y_SAD_L	Memory Start Address Sets the 16 lower bits of the 32-bit start address in memory. It is a byte address. For every frame, the first line of data will be written to this address. We have: SAD = BAD + (PTR_S x OFT) and PTR_S < PTR_E If the first line must be written at the beginning of the circular buffer memory then SAD = BAD and PTR_S = 0. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RAW, RGB5:6:5 and YUV4:2:2 formats (output data on 16 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on. RGBA format (output data on 32 bits): The three least significant bits must be set to "000" when horizontal reversal mode is off. The three least significant bits must be set to "111" when horizontal reversal mode is on.	RW	0x0000

Table 8-729. Register Call Summary for Register RZB_SDR_Y_SAD_L

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 2: [2]
- ISS RESIZER Register Summary: [3]

Table 8-730. RZB_SDR_Y_OFT

Address Offset	0x0000 0170		
Physical Address	0x5201 0570	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY OFFSET REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_OFT															

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16:0	Y_OFT	Memory Line Offset Sets the size of each line in the circular buffer. It is expressed in bytes and unsigned. Note that OFT does not necessary corresponds to the size of a line in a frame, it can be much bigger. The line offset must be a multiple of 128 bytes (bits [6:0] of RZX_SDR_Y_OFT and RZX_SDR_C_OFT must be set to 0). Example: line 0 address = SAD line 1 address = SAD + 1 x OFT line 2 address = SAD + 2 x OFT	RW	0x00000

Table 8-731. Register Call Summary for Register RZB_SDR_Y_OFT

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-732. RZB_SDR_Y_PTR_S

Address Offset	0x0000 0174		
Physical Address	0x5201 0574	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4;2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			Y_PTR_S												

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	Y_PTR_S	Start Line of Memory Pointer Sets the vertical position of the first output line in the output memory space. This value is expressed in number of lines. The hardware uses it to set up the initial value of the circular buffer. It must be set up such as PTR_S = (SAD - BAD) / OFT. This value must be set to 0 when RSZ_RZA_SDR_Y_BAD = RSZ_RZA_SDR_Y_SAD.	RW	0x0000

Table 8-733. Register Call Summary for Register RZB_SDR_Y_PTR_S

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-734. RZB_SDR_Y_PTR_E

Address Offset	0x0000 0178		
Physical Address	0x5201 0578	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY END ADDRESS REGISTER This register is used if the output data format is one of the following: RAW, YUV4:2:2, YUV4:2:0 or RGBA.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																Y_PTR_E															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	Y_PTR_E	End Line of Memory Pointer Sets the maximum number of lines to be stored in the output memory space. This value is expressed in number of lines. When the number of output lines exceeds this value, the address restarts from the first address in the output memory space (BAD).	RW	0x0000

Table 8-735. Register Call Summary for Register RZB_SDR_Y_PTR_E

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP5 SYS1 Register Description: [2] [3] [4] [5]
- ISS RESIZER Register Summary: [6]

Table 8-736. RZB_SDR_C_BAD_H

Address Offset	0x0000 017C		
Physical Address	0x5201 057C	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY BASE ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_BAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_BAD_H	Memory Base Address Sets the 16 upper bits of the 32-bit base address of the circular buffer in memory.	RW	0x0000

Table 8-737. Register Call Summary for Register RZB_SDR_C_BAD_H

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-738. RZB_SDR_C_BAD_L

Address Offset	0x0000 0180		
Physical Address	0x5201 0580	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY BASE ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_BAD_L															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_BAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit base address of the circular buffer in memory. It is a byte address. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on.	RW	0x0000

Table 8-739. Register Call Summary for Register RZB_SDR_C_BAD_L

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-740. RZB_SDR_C_SAD_H

Address Offset	0x0000 0184		
Physical Address	0x5201 0584	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_SAD_H															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_SAD_H	Memory Base Address Sets the 16 upper bits of the 32-bit start address in memory.	RW	0x0000

Table 8-741. Register Call Summary for Register RZB_SDR_C_SAD_H

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

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Table 8-742. RZB_SDR_C_SAD_L

Address Offset	0x0000 0188		
Physical Address	0x5201 0588	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0. U and V data are written into this buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_SAD_L															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	C_SAD_L	Memory Base Address Sets the 16 lower bits of the 32-bit start address in memory. It is a byte address. For every frame, the first line of data will be written to this address (C_SAD_H/C_SAD_L). We have: SAD = BAD + (PTR_S x OFT) and PTR_S < PTR_E If the first line must be written at the beginning of the circular buffer memory then SAD = BAD and PTR_S = 0. YUV4:2:0 format (output data on 8 bits): The two least significant bits must be set to 00 when horizontal reversal mode is off. The two least significant bits must be set to 11 when horizontal reversal mode is on.	RW	0x0000

Table 8-743. Register Call Summary for Register RZB_SDR_C_SAD_L

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS ISP RSZ Global Image Processing Settings – Subsequence 2: [2]
- ISS RESIZER Register Summary: [3]

Table 8-744. RZB_SDR_C_OFT

Address Offset	0x0000 018C		
Physical Address	0x5201 058C	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY OFFSET REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																C_OFT															

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16:0	C_OFT	Memory Line Offset Sets the size of each line in the circular buffer. It is expressed in bytes and unsigned. Note that OFT does not necessary corresponds to the size of a line in a frame, it can be much bigger. The line offset must be a multiple of 128 bytes (bits [6:0] of RZX_SDR_Y_OFT and RZX_SDR_C_OFT must be set to 0). Example: line 0 address = SAD line 1 address = SAD + 1 x OFT line 2 address = SAD + 2 x OFT	RW	0x00000

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Table 8-745. Register Call Summary for Register RZB_SDR_C_OFT

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-746. RZB_SDR_C_PTR_S

Address Offset	0x0000 0190		
Physical Address	0x5201 0590	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY START ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C_PTR_S							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	C_PTR_S	Start Line of Memory Pointer Sets the vertical position of the first output line in the output memory space. This value is expressed in number of lines. The hardware uses it to set up the initial value of the circular buffer. It must be set up such as PTR_S = (SAD - BAD) / OFT. This value must be set to 0 when RSZ_RZA_SDR_C_BAD = RSZ_RZA_SDR_C_SAD.	RW	0x0000

Table 8-747. Register Call Summary for Register RZB_SDR_C_PTR_S

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

Table 8-748. RZB_SDR_C_PTR_E

Address Offset	0x0000 0194		
Physical Address	0x5201 0594	**Instance**	ISS_RESIZER
Description	RESIZER B - OUTPUT MEMORY END ADDRESS REGISTER FOR CHROMA DATA (YUV4:2:0) This register is used if the output data format is YUV4:2:0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								C_PTR_E							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	C_PTR_E	End Line of Memory Pointer Sets the maximum number of lines to be stored in the output memory space. This value is expressed in number of lines. When the number of output lines exceeds this value, the address restarts from the first address in the output memory space (BAD).	RW	0x0000

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Table 8-749. Register Call Summary for Register RZB_SDR_C_PTR_E

ISS ISP

- ISS ISP RSZ Output Interface: [0]
- ISS ISP RSZ Global Image Processing Settings: [1]
- ISS RESIZER Register Summary: [2]

8.3.5.5 ISS IPIPE registers

8.3.5.5.1 ISS IPIPE Register Summary

Table 8-750. ISS IPIPE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPE Base Address
IPIPE_SRC_EN	RW	32	0x0000 0000	0x5201 0800
IPIPE_SRC_MODE	RW	32	0x0000 0004	0x5201 0804
IPIPE_SRC_FMT	RW	32	0x0000 0008	0x5201 0808
IPIPE_SRC_COL	RW	32	0x0000 000C	0x5201 080C
IPIPE_SRC_VPS	RW	32	0x0000 0010	0x5201 0810
IPIPE_SRC_VSZ	RW	32	0x0000 0014	0x5201 0814
IPIPE_SRC_HPS	RW	32	0x0000 0018	0x5201 0818
IPIPE_SRC_HSZ	RW	32	0x0000 001C	0x5201 081C
IPIPE_SEL_SBU	RW	32	0x0000 0020	0x5201 0820
IPIPE_SRC_STA	R	32	0x0000 0024	0x5201 0824
IPIPE_GCK_MMR	RW	32	0x0000 0028	0x5201 0828
IPIPE_GCK_PIX	RW	32	0x0000 002C	0x5201 082C
RESERVED	R	32	0x0000 0030	0x5201 0830
IPIPE_DPC_LUT_EN	RW	32	0x0000 0034	0x5201 0834
IPIPE_DPC_LUT_SEL	RW	32	0x0000 0038	0x5201 0838
IPIPE_DPC_LUT_ADR	RW	32	0x0000 003C	0x5201 083C
IPIPE_DPC_LUT_SIZ	RW	32	0x0000 0040	0x5201 0840
RESERVEDa[1]	RW	32	0x0000 0044 + (b * 4)	0x5201 0844 + (b * 4)
IPIPE_LSC_VOFT	RW	32	0x0000 0090	0x5201 0890
IPIPE_LSC_VA2	RW	32	0x0000 0094	0x5201 0894
IPIPE_LSC_VA1	RW	32	0x0000 0098	0x5201 0898
IPIPE_LSC_VS	RW	32	0x0000 009C	0x5201 089C
IPIPE_LSC_HOFT	RW	32	0x0000 00A0	0x5201 08A0
IPIPE_LSC_HA2	RW	32	0x0000 00A4	0x5201 08A4
IPIPE_LSC_HA1	RW	32	0x0000 00A8	0x5201 08A8
IPIPE_LSC_HS	RW	32	0x0000 00AC	0x5201 08AC
IPIPE_LSC_GAN_R	RW	32	0x0000 00B0	0x5201 08B0
IPIPE_LSC_GAN_GR	RW	32	0x0000 00B4	0x5201 08B4
IPIPE_LSC_GAN_GB	RW	32	0x0000 00B8	0x5201 08B8
IPIPE_LSC_GAN_B	RW	32	0x0000 00BC	0x5201 08BC
IPIPE_LSC_OFT_R	RW	32	0x0000 00C0	0x5201 08C0
IPIPE_LSC_OFT_GR	RW	32	0x0000 00C4	0x5201 08C4

(1) a = 0 to 18
b = 0 to 55
c = 0 to 5
d = 0 to 14
e = 0 to 1
f = 0 to 24
g = 0 to 18

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Table 8-750. ISS IPIPE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPE Base Address
IPIPE_LSC_OFT_GB	RW	32	0x0000 00C8	0x5201 08C8
IPIPE_LSC_OFT_B	RW	32	0x0000 00CC	0x5201 08CC
IPIPE_LSC_SHF	RW	32	0x0000 00D0	0x5201 08D0
IPIPE_LSC_MAX	RW	32	0x0000 00D4	0x5201 08D4
RESERVEDb[1]	RW	32	0x0000 00D8 + (b * 0x4)	0x5201 08D8 + (b * 0x4)
RESERVEDc[1]	RW	32	0x0000 01B8 + (c * 0x4)	0x5201 09B8 + (c * 0x4)
IPIPE_WB2_OFT_R	RW	32	0x0000 01D0	0x5201 09D0
IPIPE_WB2_OFT_GR	RW	32	0x0000 01D4	0x5201 09D4
IPIPE_WB2_OFT_GB	RW	32	0x0000 01D8	0x5201 09D8
IPIPE_WB2_OFT_B	RW	32	0x0000 01DC	0x5201 09DC
IPIPE_WB2_WGN_R	RW	32	0x0000 01E0	0x5201 09E0
IPIPE_WB2_WGN_GR	RW	32	0x0000 01E4	0x5201 09E4
IPIPE_WB2_WGN_GB	RW	32	0x0000 01E8	0x5201 09E8
IPIPE_WB2_WGN_B	RW	32	0x0000 01EC	0x5201 09EC
RESERVEDd[1]	RW	32	0x0000 01F0 + (d * 0x4)	0x5201 09F0 + (d * 0x4)
IPIPE_RGB1_MUL_RR	RW	32	0x0000 022C	0x5201 0A2C
IPIPE_RGB1_MUL_GR	RW	32	0x0000 0230	0x5201 0A30
IPIPE_RGB1_MUL_BR	RW	32	0x0000 0234	0x5201 0A34
IPIPE_RGB1_MUL_RG	RW	32	0x0000 0238	0x5201 0A38
IPIPE_RGB1_MUL_GG	RW	32	0x0000 023C	0x5201 0A3C
IPIPE_RGB1_MUL_BG	RW	32	0x0000 0240	0x5201 0A40
IPIPE_RGB1_MUL_RB	RW	32	0x0000 0244	0x5201 0A44
IPIPE_RGB1_MUL_GB	RW	32	0x0000 0248	0x5201 0A48
IPIPE_RGB1_MUL_BB	RW	32	0x0000 024C	0x5201 0A4C
IPIPE_RGB1_OFT_OR	RW	32	0x0000 0250	0x5201 0A50
IPIPE_RGB1_OFT_OG	RW	32	0x0000 0254	0x5201 0A54
IPIPE_RGB1_OFT_OB	RW	32	0x0000 0258	0x5201 0A58
IPIPE_GMM_CFG	RW	32	0x0000 025C	0x5201 0A5C
IPIPE_RGB2_MUL_RR	RW	32	0x0000 0260	0x5201 0A60
IPIPE_RGB2_MUL_GR	RW	32	0x0000 0264	0x5201 0A64
IPIPE_RGB2_MUL_BR	RW	32	0x0000 0268	0x5201 0A68
IPIPE_RGB2_MUL_RG	RW	32	0x0000 026C	0x5201 0A6C
IPIPE_RGB2_MUL_GG	RW	32	0x0000 0270	0x5201 0A70
IPIPE_RGB2_MUL_BG	RW	32	0x0000 0274	0x5201 0A74
IPIPE_RGB2_MUL_RB	RW	32	0x0000 0278	0x5201 0A78
IPIPE_RGB2_MUL_GB	RW	32	0x0000 027C	0x5201 0A7C
IPIPE_RGB2_MUL_BB	RW	32	0x0000 0280	0x5201 0A80
IPIPE_RGB2_OFT_OR	RW	32	0x0000 0284	0x5201 0A84
IPIPE_RGB2_OFT_OG	RW	32	0x0000 0288	0x5201 0A88
IPIPE_RGB2_OFT_OB	RW	32	0x0000 028C	0x5201 0A8C
RESERVED	RW	32	0x0000 0290	0x5201 0A90
IPIPE_YUV_ADJ	RW	32	0x0000 0294	0x5201 0A94
IPIPE_YUV_MUL_RY	RW	32	0x0000 0298	0x5201 0A98
IPIPE_YUV_MUL_GY	RW	32	0x0000 029C	0x5201 0A9C
IPIPE_YUV_MUL_BY	RW	32	0x0000 02A0	0x5201 0AA0
IPIPE_YUV_MUL_RCB	RW	32	0x0000 02A4	0x5201 0AA4
IPIPE_YUV_MUL_GCB	RW	32	0x0000 02A8	0x5201 0AA8

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Table 8-750. ISS IPIPE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPE Base Address
IPIPE_YUV_MUL_BCB	RW	32	0x0000 02AC	0x5201 0AAC
IPIPE_YUV_MUL_RCR	RW	32	0x0000 02B0	0x5201 0AB0
IPIPE_YUV_MUL_GCR	RW	32	0x0000 02B4	0x5201 0AB4
IPIPE_YUV_MUL_BCR	RW	32	0x0000 02B8	0x5201 0AB8
IPIPE_YUV_OFT_Y	RW	32	0x0000 02BC	0x5201 0ABC
IPIPE_YUV_OFT_CB	RW	32	0x0000 02C0	0x5201 0AC0
IPIPE_YUV_OFT_CR	RW	32	0x0000 02C4	0x5201 0AC4
IPIPE_YUV_PHS	RW	32	0x0000 02C8	0x5201 0AC8
RESERVEDe[2]	RW	32	0x0000 02CC + (e * 0x4)	0x5201 0ACC + (e * 0x4)
IPIPE_YEE_EN	RW	32	0x0000 02D4	0x5201 0AD4
IPIPE_YEE_TYP	RW	32	0x0000 02D8	0x5201 0AD8
IPIPE_YEE_SHF	RW	32	0x0000 02DC	0x5201 0ADC
IPIPE_YEE_MUL_00	RW	32	0x0000 02E0	0x5201 0AE0
IPIPE_YEE_MUL_01	RW	32	0x0000 02E4	0x5201 0AE4
IPIPE_YEE_MUL_02	RW	32	0x0000 02E8	0x5201 0AE8
IPIPE_YEE_MUL_10	RW	32	0x0000 02EC	0x5201 0AEC
IPIPE_YEE_MUL_11	RW	32	0x0000 02F0	0x5201 0AF0
IPIPE_YEE_MUL_12	RW	32	0x0000 02F4	0x5201 0AF4
IPIPE_YEE_MUL_20	RW	32	0x0000 02F8	0x5201 0AF8
IPIPE_YEE_MUL_21	RW	32	0x0000 02FC	0x5201 0AFC
IPIPE_YEE_MUL_22	RW	32	0x0000 0300	0x5201 0B00
IPIPE_YEE_THR	RW	32	0x0000 0304	0x5201 0B04
IPIPE_YEE_E_GAN	RW	32	0x0000 0308	0x5201 0B08
IPIPE_YEE_E_THR_1	RW	32	0x0000 030C	0x5201 0B0C
IPIPE_YEE_E_THR_2	RW	32	0x0000 0310	0x5201 0B10
IPIPE_YEE_G_GAN	RW	32	0x0000 0314	0x5201 0B14
IPIPE_YEE_G_OFT	RW	32	0x0000 0318	0x5201 0B18
RESERVEDf[3]	RW	32	0x0000 031C + (f * 0x4)	0x5201 0B1C + (f * 0x4)
IPIPE_BOX_EN	RW	32	0x0000 0380	0x5201 0B80
IPIPE_BOX_MODE	RW	32	0x0000 0384	0x5201 0B84
IPIPE_BOX_TYP	RW	32	0x0000 0388	0x5201 0B88
IPIPE_BOX_SHF	RW	32	0x0000 038C	0x5201 0B8C
IPIPE_BOX_SDR_SAD_H	RW	32	0x0000 0390	0x5201 0B90
IPIPE_BOX_SDR_SAD_L	RW	32	0x0000 0394	0x5201 0B94
RESERVED	R	32	0x0000 0398	0x5201 0B98

(2) a = 0 to 18
b = 0 to 55
c = 0 to 5
d = 0 to 14
e = 0 to 1
f = 0 to 24
g = 0 to 18

(3) a = 0 to 18
b = 0 to 55
c = 0 to 5
d = 0 to 14
e = 0 to 1
f = 0 to 24
g = 0 to 18

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Table 8-750. ISS IPIPE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPE Base Address
IPIPE_HST_EN	RW	32	0x0000 039C	0x5201 0B9C
IPIPE_HST_MODE	RW	32	0x0000 03A0	0x5201 0BA0
IPIPE_HST_SEL	RW	32	0x0000 03A4	0x5201 0BA4
IPIPE_HST_PARA	RW	32	0x0000 03A8	0x5201 0BA8
IPIPE_HST_0_VPS	RW	32	0x0000 03AC	0x5201 0BAC
IPIPE_HST_0_VSZ	RW	32	0x0000 03B0	0x5201 0BB0
IPIPE_HST_0_HPS	RW	32	0x0000 03B4	0x5201 0BB4
IPIPE_HST_0_HSZ	RW	32	0x0000 03B8	0x5201 0BB8
IPIPE_HST_1_VPS	RW	32	0x0000 03BC	0x5201 0BBC
IPIPE_HST_1_VSZ	RW	32	0x0000 03C0	0x5201 0BC0
IPIPE_HST_1_HPS	RW	32	0x0000 03C4	0x5201 0BC4
IPIPE_HST_1_HSZ	RW	32	0x0000 03C8	0x5201 0BC8
IPIPE_HST_2_VPS	RW	32	0x0000 03CC	0x5201 0BCC
IPIPE_HST_2_VSZ	RW	32	0x0000 03D0	0x5201 0BD0
IPIPE_HST_2_HPS	RW	32	0x0000 03D4	0x5201 0BD4
IPIPE_HST_2_HSZ	RW	32	0x0000 03D8	0x5201 0BD8
IPIPE_HST_3_VPS	RW	32	0x0000 03DC	0x5201 0BDC
IPIPE_HST_3_VSZ	RW	32	0x0000 03E0	0x5201 0BE0
IPIPE_HST_3_HPS	RW	32	0x0000 03E4	0x5201 0BE4
IPIPE_HST_3_HSZ	RW	32	0x0000 03E8	0x5201 0BE8
IPIPE_HST_TBL	RW	32	0x0000 03EC	0x5201 0BEC
IPIPE_HST_MUL_R	RW	32	0x0000 03F0	0x5201 0BF0
IPIPE_HST_MUL_GR	RW	32	0x0000 03F4	0x5201 0BF4
IPIPE_HST_MUL_GB	RW	32	0x0000 03F8	0x5201 0BF8
IPIPE_HST_MUL_B	RW	32	0x0000 03FC	0x5201 0BFC
RESERVEDg[4]	RW	32	0x0000 0400 + (g * 0x4)	0x5201 0C00 + (g * 0x4)

(4) a = 0 to 18
b = 0 to 55
c = 0 to 5
d = 0 to 14
e = 0 to 1
f = 0 to 24
g = 0 to 18

8.3.5.5.2 ISS IPIPE Register Description

Table 8-751. IPIPE_SRC_EN

Address Offset	0x0000 0000		
Physical Address	0x5201 0800	**Instance**	ISS_IPIPE
Description	This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	The start flag of the IPIPE module. When EN is 1, the IPIPE module starts a processing from the next rising edge of the VD. If the processing mode of the IPIPE module is one shot, the EN is cleared to 0 immediately after the processing has started. 0x0: waiting 0x1: start/busy	RW	0

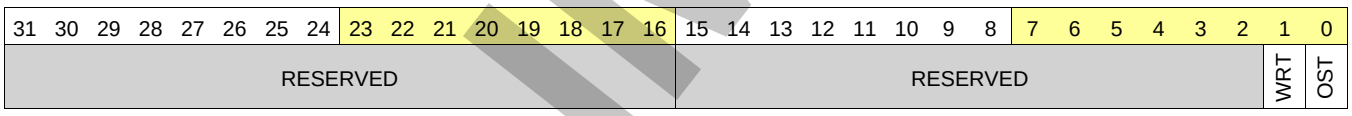
Table 8-752. Register Call Summary for Register IPIPE_SRC_EN

ISS ISP

- ISS ISP IPIPE Input Interface: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS ISP IPIPE Processing Path: Case 1 Configuration: [2]
- ISS ISP IPIPE Processing Path: Case 2 Configuration: [3]
- ISS ISP IPIPE Processing Path: Case 3 Configuration: [4]
- ISS ISP IPIPE Processing Path: Case 4 Configuration: [5]
- ISS IPIPE Register Summary: [6]

Table 8-753. IPIPE_SRC_MODE

Address Offset	0x0000 0004		
Physical Address	0x5201 0804	**Instance**	ISS_IPIPE
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	WRT	The mode selection of the ipipeif_wrt which is an input port of the IPIPE module. If WRT is 0, the IPIPE module does not use the ipipeif_wrt. Else the IPIPE module uses it. 0x0: Disable 0x1: Enable	RW	0
0	OST	The processing mode selection of the IPIPE module. Value 0 indicates the mode of free run, value 1 indicates the mode of one shot. 0x0: Free run 0x1: One shot	RW	0

Table 8-754. Register Call Summary for Register IPIPE_SRC_MODE

ISS ISP

- ISS ISP IPIPE Input Interface: [0] [1] [2] [3]
- ISS ISP IPIPE Global Initialization: [4] [5]
- ISS IPIPE Register Summary: [6]

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Table 8-755. IPIPE_SRC_FMT

Address Offset	0x0000 0008		
Physical Address	0x5201 0808	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														FMT	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1:0	FMT	IPIPE module data path selection 0x0: IN: RAW BAYER OUT: YUV4:2:2 Note that the IPIPE YUV4:2:2 output goes to the RESIZER module where it can be further be converted in YUV4:2:0 or RGB format. 0x1: IN: RAW BAYER OUT: RAW BAYER The data are output after the White Balance module. It enables to bypass a large part of the IPIPE module. 0x3: IN: YUV4:2:2 OUT: YUV4:2:2 Note that the IPIPE YUV4:2:2 output goes to the RESIZER module where it can be further be converted in YUV4:2:0 or RGB format. 0x2: IN: RAW BAYER OUT: DISABLED The data are only going to BOXCAR and HISTOGRAM modules.	RW	0x0

Table 8-756. Register Call Summary for Register IPIPE_SRC_FMT

ISS ISP

- ISS ISP IPIPE Input Interface: [0] [1]
- ISS ISP IPIPE Global Initialization: [2]
- ISS ISP IPIPE Processing Path: Case 1 Configuration: [3]
- ISS ISP IPIPE Processing Path: Case 2 Configuration: [4]
- ISS ISP IPIPE Processing Path: Case 3 Configuration: [5]
- ISS ISP IPIPE Processing Path: Case 4 Configuration: [6]
- ISS IPIPE Register Summary: [7]
- ISS IPIPE Register Description: [8] [9] [10]

Table 8-757. IPIPE_SRC_COL

Address Offset	0x0000 000C		
Physical Address	0x5201 080C	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								OO			OE			EO			EE

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:6	OO	The color pattern of the odd line and odd pixel. This parameter is valid when IPIPE_SRC[FMT] is 0,1,2. 0x0: R 0x1: Gr 0x3: B 0x2: Gb	RW	0x3
5:4	OE	The color pattern of the odd line and even pixel. This parameter is valid when IPIPE_SRC[FMT] is 0,1,2. 0x0: R 0x1: Gr 0x3: B 0x2: Gb	RW	0x2
3:2	EO	The color pattern of the even line and odd pixel. This parameter is valid when IPIPE_SRC[FMT] is 0,1,2. 0x0: R 0x1: Gr 0x3: B 0x2: Gb	RW	0x1
1:0	EE	The color pattern of the even line and even pixel. This parameter is valid when IPIPE_SRC[FMT] is 0,1,2. 0x0: R 0x1: Gr 0x3: B 0x2: Gb	RW	0x0

Table 8-758. Register Call Summary for Register IPIPE_SRC_COL

ISS ISP
- ISS IPIPE Register Summary: [0]

Table 8-759. IPIPE_SRC_VPS

Address Offset	0x0000 0010		
Physical Address	0x5201 0810	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	VAL	The vertical position of the global frame from the rising edge of the VD. The IPIPE module will start an image processing from VAL line.	RW	0x0000

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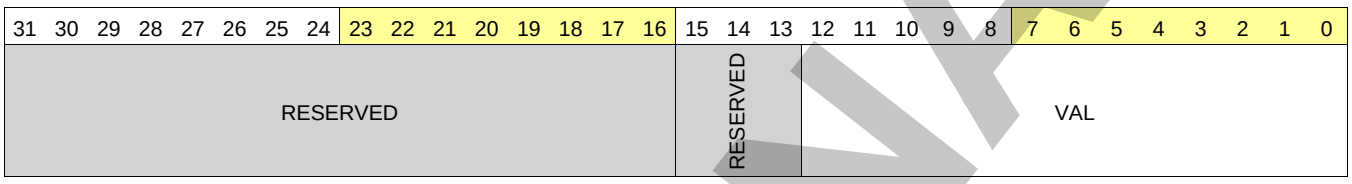
Table 8-760. Register Call Summary for Register IPIPE_SRC_VPS

ISS ISP

- ISS ISP IPIPE Input Interface: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3] [4] [5] [6] [7] [8] [9] [10]

Table 8-761. IPIPE_SRC_VSZ

Address Offset	0x0000 0014		
Physical Address	0x5201 0814	**Instance**	ISS_IPIPE
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	The vertical size of the processing area. The VAL0 can not be written. The IPIPE module will process (VAL+1) lines.	RW	0x0000

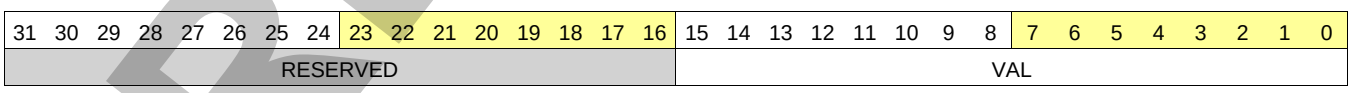
Table 8-762. Register Call Summary for Register IPIPE_SRC_VSZ

ISS ISP

- ISS ISP IPIPE Input Interface: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-763. IPIPE_SRC_HPS

Address Offset	0x0000 0018		
Physical Address	0x5201 0818	**Instance**	ISS_IPIPE
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	VAL	The horizontal position of the global frame from the rising edge of the HD. The IPIPE module will start an image processing from VAL clock.	RW	0x0000

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Table 8-764. Register Call Summary for Register IPIPE_SRC_HPS

ISS ISP

- ISS ISP IPIPE Input Interface: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3] [4] [5] [6] [7] [8] [9] [10]

Table 8-765. IPIPE_SRC_HSZ

Address Offset	0x0000 001C		
Physical Address	0x5201 081C	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VAL							VAL_0

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:1	VAL	The horizontal size of the processing area. The VAL0 is fixed. The IPIPE module processes (VAL+1) clocks.	RW	0x000
0	VAL_0	This is the LSB of the VAL[12:0]. This bit is read only.	R	1

Table 8-766. Register Call Summary for Register IPIPE_SRC_HSZ

ISS ISP

- ISS ISP IPIPE Input Interface: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-767. IPIPE_SEL_SBU

Address Offset	0x0000 0020		
Physical Address	0x5201 0820	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EDOF

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EDOF	EDOF port selection This bit must not be enabled since the EDOF module is not implemented. This is a provision for a future revision of the IP. 0x0: Not used 0x1: Used	RW	0

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Table 8-768. Register Call Summary for Register IPIPE_SEL_SBU

ISS ISP

- ISS IPIPE Register Summary: [0]

Table 8-769. IPIPE_SRC_STA

Address Offset	0x0000 0024		
Physical Address	0x5201 0824	**Instance**	ISS_IPIPE
Description	IPIPE STATUS REGISTER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED											VAL4	VAL3	VAL2	VAL1	VAL0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:5	RESERVED		R	0x000
4	VAL4	Status of Histogram Process (busy status).	R	0
3	VAL3	Status of Histogram bank select.	R	0
2	VAL2	Status of BSC process (busy status).	R	0
1	VAL1	Status of Boxcar process (busy status).	R	0
0	VAL0	Status of Boxcar process (error status). This bit will be triggered when an overflow happens while transferring the boxcar data to memory. Instead of polling for this register, it is preferable to use the IPIPE_BOXCAR_OVF interrupt. Overflow errors are non recoverable at ISP level and require a software reset at ISS level.	R	0

Table 8-770. Register Call Summary for Register IPIPE_SRC_STA

ISS ISP

- ISS ISP IPIPE Interrupts: [0]
- ISS IPIPE Register Summary: [1]

Table 8-771. IPIPE_GCK_MMR

Address Offset	0x0000 0028		
Physical Address	0x5201 0828	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															REG

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	REG	The on/off selection of the clk_arm_g0 which is used for some ARM register access. 0x0: Off 0x1: On	RW	0

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Table 8-772. Register Call Summary for Register IPIPE_GCK_MMR

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-773. IPIPE_GCK_PIX

Address Offset	0x0000 002C		
Physical Address	0x5201 082C	**Instance**	ISS_IPIPE
Description	This register is not shadowed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED												G3	G2	G1	G0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3	G3	The on/off selection of the clk_pix_g3 which is use for the IPIPE processes of EE . 0x0: Disable 0x1: Enable	RW	0
2	G2	The on/off selection of the clk_pix_g2 which is use for the IPIPE processes of RGB2RGB blending to "422", "Histogram(YCbCr input)". 0x0: Disable 0x1: Enable	RW	0
1	G1	The on/off selection of the clk_pix_g1 which is used for the IPIPE processes of "DefectCorrection" to "WhiteBalance", and "Histogram(RAW input)". 0x0: Disable 0x1: Enable	RW	0
0	G0	The on/off selection of the clk_pix_g0 which is used for the IPIPE processing of "Boxcar". 0x0: Disable 0x1: Enable	RW	0

Table 8-774. Register Call Summary for Register IPIPE_GCK_PIX

ISS ISP

- ISS ISP IPIPE Global Initialization: [0] [1] [2] [3]
- ISS IPIPE Register Summary: [4]

Table 8-775. IPIPE_DPC_LUT_EN

Address Offset	0x0000 0034		
Physical Address	0x5201 0834	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	Enable of LUT defect pixel correction. 0x0: Off 0x1: On	RW	0

Table 8-776. Register Call Summary for Register IPIPE_DPC_LUT_EN

ISS ISP

- ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC): [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-777. IPIPE_DPC_LUT_SEL

Address Offset	0x0000 0038		
Physical Address	0x5201 0838	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														TBL	DOT

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	TBL	LUT table type selection. 0x0: Up to 1024 entries. (use IPIPE_DPC_LUT_SIZ) 0x1: infinity number of entries. (not use IPIPE_DPC_LUT_SIZ)	RW	0
0	DOT	Replace dot selection on processing method 0. 0x0: Replace with black dot 0x1: Replace with white dot	RW	0

Table 8-778. Register Call Summary for Register IPIPE_DPC_LUT_SEL

ISS ISP

- ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC): [0] [1] [2]
- ISS ISP IPIPE Global Initialization: [3] [4]
- ISS IPIPE Register Summary: [5]

Table 8-779. IPIPE_DPC_LUT_ADR

Address Offset	0x0000 003C		
Physical Address	0x5201 083C	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								ADR							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	ADR	The address of the first valid data in look-up-table	RW	0x000

Table 8-780. Register Call Summary for Register IPIPE_DPC_LUT_ADR

ISS ISP

- ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC): [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-781. IPIPE_DPC_LUT_SIZ

Address Offset	0x0000 0040		
Physical Address	0x5201 0840	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								SIZ							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	SIZ	The number of valid data in look-up-table. (SIZ+1)	RW	0x000

Table 8-782. Register Call Summary for Register IPIPE_DPC_LUT_SIZ

ISS ISP

- ISS ISP IPIPE LUT Defect Pixel Correction (LUT DPC): [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3] [4]

Table 8-783. IPIPE_LSC_VOFT

Address Offset	0x0000 0090		
Physical Address	0x5201 0890	**Instance**	ISS_IPIPE
Description	LSC VOFT		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								LSC_VOFT							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	LSC_VOFT		RW	0x0000

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Table 8-784. Register Call Summary for Register IPIPE_LSC_VOFT

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-785. IPIPE_LSC_VA2

Address Offset	0x0000 0094		
Physical Address	0x5201 0894	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC VA2	RW	0x0000

Table 8-786. Register Call Summary for Register IPIPE_LSC_VA2

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-787. IPIPE_LSC_VA1

Address Offset	0x0000 0098		
Physical Address	0x5201 0898	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC VA1	RW	0x0000

Table 8-788. Register Call Summary for Register IPIPE_LSC_VA1

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [2]

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Table 8-789. IPIPE_LSC_VS

Address Offset	0x0000 009C		
Physical Address	0x5201 089C	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VS2				VS1			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:4	VS2	LSC VS1	RW	0x0
3:0	VS1	LSC VS1	RW	0x0

Table 8-790. Register Call Summary for Register IPIPE_LSC_VS

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [3]

Table 8-791. IPIPE_LSC_HOFT

Address Offset	0x0000 00A0		
Physical Address	0x5201 08A0	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC HOFT	RW	0x0000

Table 8-792. Register Call Summary for Register IPIPE_LSC_HOFT

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-793. IPIPE_LSC_HA2

Address Offset	0x0000 00A4		
Physical Address	0x5201 08A4	**Instance**	ISS_IPIPE
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC HA2	RW	0x0000

Table 8-794. Register Call Summary for Register IPIPE_LSC_HA2

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-795. IPIPE_LSC_HA1

Address Offset	0x0000 00A8		
Physical Address	0x5201 08A8	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	LSC HA1	RW	0x0000

Table 8-796. Register Call Summary for Register IPIPE_LSC_HA1

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-797. IPIPE_LSC_HS

Address Offset	0x0000 00AC		
Physical Address	0x5201 08AC	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								HS2				HS1			

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:4	HS2	LSC HS1	RW	0x0
3:0	HS1	LSC HS1	RW	0x0

Table 8-798. Register Call Summary for Register IPIPE_LSC_HS

ISS ISP
- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [3]

Table 8-799. IPIPE_LSC_GAN_R

Address Offset	0x0000 00B0		
Physical Address	0x5201 08B0	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	GAN R	RW	0x00

Table 8-800. Register Call Summary for Register IPIPE_LSC_GAN_R

ISS ISP
- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-801. IPIPE_LSC_GAN_GR

Address Offset	0x0000 00B4		
Physical Address	0x5201 08B4	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	GAN GR	RW	0x00

Table 8-802. Register Call Summary for Register IPIPE_LSC_GAN_GR

ISS ISP
- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [1]

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Table 8-803. IPIPE_LSC_GAN_GB

Address Offset	0x0000 00B8		
Physical Address	0x5201 08B8	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	GAN GB	RW	0x00

Table 8-804. Register Call Summary for Register IPIPE_LSC_GAN_GB

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-805. IPIPE_LSC_GAN_B

Address Offset	0x0000 00BC		
Physical Address	0x5201 08BC	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	GAN B	RW	0x00

Table 8-806. Register Call Summary for Register IPIPE_LSC_GAN_B

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-807. IPIPE_LSC_OFT_R

Address Offset	0x0000 00C0		
Physical Address	0x5201 08C0	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	LSC OFT R	RW	0x00

Table 8-808. Register Call Summary for Register IPIPE_LSC_OFT_R

ISS ISP
- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-809. IPIPE_LSC_OFT_GR

Address Offset	0x0000 00C4		
Physical Address	0x5201 08C4	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	LSC OFT GR	RW	0x00

Table 8-810. Register Call Summary for Register IPIPE_LSC_OFT_GR

ISS ISP
- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-811. IPIPE_LSC_OFT_GB

Address Offset	0x0000 00C8		
Physical Address	0x5201 08C8	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	LSC OFT GB	RW	0x00

Table 8-812. Register Call Summary for Register IPIPE_LSC_OFT_GB

ISS ISP
- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [1]

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Table 8-813. IPIPE_LSC_OFT_B

Address Offset	0x0000 00CC		
Physical Address	0x5201 08CC	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	LSC OFT B	RW	0x00

Table 8-814. Register Call Summary for Register IPIPE_LSC_OFT_B

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [1]

Table 8-815. IPIPE_LSC_SHF

Address Offset	0x0000 00D0		
Physical Address	0x5201 08D0	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED													VAL		

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3:0	VAL	LSC SHV	RW	0x0

Table 8-816. Register Call Summary for Register IPIPE_LSC_SHF

ISS ISP

- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-817. IPIPE_LSC_MAX

Address Offset	0x0000 00D4		
Physical Address	0x5201 08D4	**Instance**	ISS_IPIPE
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:9	RESERVED		R	0x00
8:0	VAL	LSC MAX	RW	0x000

Table 8-818. Register Call Summary for Register IPIPE_LSC_MAX

ISS ISP
- ISS ISP IPIPE Global Initialization:
- ISS IPIPE Register Summary: [2]

Table 8-819. IPIPE_WB2_OFT_R

Address Offset	0x0000 01D0		
Physical Address	0x5201 09D0	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Offset before white balance (S12) -2048 to +2047	RW	0x000

Table 8-820. Register Call Summary for Register IPIPE_WB2_OFT_R

ISS ISP
- ISS ISP IPIPE White Balance: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-821. IPIPE_WB2_OFT_GR

Address Offset	0x0000 01D4		
Physical Address	0x5201 09D4	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Offset before white balance (S12) -2048 to +2047	RW	0x000

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Table 8-822. Register Call Summary for Register IPIPE_WB2_OFT_GR

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-823. IPIPE_WB2_OFT_GB

Address Offset	0x0000 01D8		
Physical Address	0x5201 09D8	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Offset before white balance (S12) -2048 to +2047	RW	0x000

Table 8-824. Register Call Summary for Register IPIPE_WB2_OFT_GB

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-825. IPIPE_WB2_OFT_B

Address Offset	0x0000 01DC		
Physical Address	0x5201 09DC	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Offset before white balance (S12) -2048 to +2047	RW	0x000

Table 8-826. Register Call Summary for Register IPIPE_WB2_OFT_B

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-827. IPIPE_WB2_WGN_R

Address Offset	0x0000 01E0		
Physical Address	0x5201 09E0	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	White balance gain for R in U4.9 format 0 to +15.998	RW	0x0200

Table 8-828. Register Call Summary for Register IPIPE_WB2_WGN_R

ISS ISP

- ISS ISP IPIPE White Balance: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-829. IPIPE_WB2_WGN_GR

Address Offset	0x0000 01E4		
Physical Address	0x5201 09E4	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	White balance gain for Gr in U4.9 format 0 to +15.998	RW	0x0200

Table 8-830. Register Call Summary for Register IPIPE_WB2_WGN_GR

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-831. IPIPE_WB2_WGN_GB

Address Offset	0x0000 01E8		
Physical Address	0x5201 09E8	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	White balance gain for Gb in U4.9 format 0 to +15.998	RW	0x0200

Table 8-832. Register Call Summary for Register IPIPE_WB2_WGN_GB

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-833. IPIPE_WB2_WGN_B

Address Offset	0x0000 01EC		
Physical Address	0x5201 09EC	**Instance**	ISS_IPIPE
Description	White Balance Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	White balance gain for B in U4.9 format 0 to +15.998	RW	0x0200

Table 8-834. Register Call Summary for Register IPIPE_WB2_WGN_B

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-835. IPIPE_RGB1_MUL_RR

Address Offset	0x0000 022C		
Physical Address	0x5201 0A2C	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient. 011111111111 = 2047/256 = 7.99609375 011111111110 = 2046/256 [...] 000011111111 = 255/256 000100000000 = 256/256 = 1 000100000001 = 257/256 [...] 000000000001 = 1/256 000000000000 = 0/256 = 0 111111111111 = -1/256 = -0.00390625 111111111110 = -2/256 [...] 100000000001 = -2047/256 100000000000 = -2048/256 = -8.	RW	0x100

Table 8-836. Register Call Summary for Register IPIPE_RGB1_MUL_RR

ISS ISP

- ISS ISP IPIPE RGB2RGB Blending Module: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-837. IPIPE_RGB1_MUL_GR

Address Offset	0x0000 0230		
Physical Address	0x5201 0A30	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-838. Register Call Summary for Register IPIPE_RGB1_MUL_GR

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-839. IPIPE_RGB1_MUL_BR

Address Offset	0x0000 0234		
Physical Address	0x5201 0A34	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-840. Register Call Summary for Register IPIPE_RGB1_MUL_BR

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-841. IPIPE_RGB1_MUL_RG

Address Offset	0x0000 0238		
Physical Address	0x5201 0A38	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-842. Register Call Summary for Register IPIPE_RGB1_MUL_RG

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-843. IPIPE_RGB1_MUL_GG

Address Offset	0x0000 023C		
Physical Address	0x5201 0A3C	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x100

Table 8-844. Register Call Summary for Register IPIPE_RGB1_MUL_GG

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-845. IPIPE_RGB1_MUL_BG

Address Offset	0x0000 0240		
Physical Address	0x5201 0A40	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-846. Register Call Summary for Register IPIPE_RGB1_MUL_BG

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-847. IPIPE_RGB1_MUL_RB

Address Offset	0x0000 0244		
Physical Address	0x5201 0A44	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-848. Register Call Summary for Register IPIPE_RGB1_MUL_RB

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-849. IPIPE_RGB1_MUL_GB

Address Offset	0x0000 0248		
Physical Address	0x5201 0A48	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x000

Table 8-850. Register Call Summary for Register IPIPE_RGB1_MUL_GB

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-851. IPIPE_RGB1_MUL_BB

Address Offset	0x0000 024C		
Physical Address	0x5201 0A4C	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x100

Table 8-852. Register Call Summary for Register IPIPE_RGB1_MUL_BB

ISS ISP

- ISS ISP IPIPE RGB2RGB Blending Module: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-853. IPIPE_RGB1_OFT_OR

Address Offset	0x0000 0250		
Physical Address	0x5201 0A50	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	The output offset value for R. (s13) -4096 to +4095	RW	0x0000

Table 8-854. Register Call Summary for Register IPIPE_RGB1_OFT_OR

ISS ISP

- ISS ISP IPIPE RGB2RGB Blending Module: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-855. IPIPE_RGB1_OFT_OG

Address Offset	0x0000 0254		
Physical Address	0x5201 0A54	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	The output offset value for G. (s13) -4096 to +4095	RW	0x0000

Table 8-856. Register Call Summary for Register IPIPE_RGB1_OFT_OG

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-857. IPIPE_RGB1_OFT_OB

Address Offset	0x0000 0258		
Physical Address	0x5201 0A58	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	VAL	The output offset value for B. (s13) -4096 to +4095	RW	0x0000

Table 8-858. Register Call Summary for Register IPIPE_RGB1_OFT_OB

ISS ISP

- ISS ISP IPIPE RGB2RGB Blending Module: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-859. IPIPE_GMM_CFG

Address Offset	0x0000 025C		
Physical Address	0x5201 0A5C	**Instance**	ISS_IPIPE
Description	RGB to RGB Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								SIZ		TBL	RESERVED	BYPB	BYPG	BYPR	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:7	RESERVED		R	0x000
6:5	SIZ	The size of the gamma table. 0x0: 64 words 0x1: 128 words 0x3: 512 words 0x2: 256 words	RW	0x3
4	TBL	Selection of Gamma table. 0x0: RAM 0x1: ROM	RW	0
3	RESERVED		RW	0
2	BYPB	Gamma correction mode for B 0x0: Not bypassed 0x1: Bypassed	RW	1
1	BYPG	Gamma correction mode for G 0x0: Not bypassed 0x1: Bypassed	RW	1

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Bits	Field Name	Description	Type	Reset
0	BYPR	Gamma correction mode for R 0x0: Not bypassed 0x1: Bypassed	RW	1

Table 8-860. Register Call Summary for Register IPIPE_GMM_CFG

ISS ISP
- ISS ISP IPIPE Gamma Correction Module: [0] [1] [2] [3]
- ISS ISP IPIPE Global Initialization: [4] [5] [6] [7] [8]
- ISS IPIPE Register Summary: [9]

Table 8-861. IPIPE_RGB2_MUL_RR

Address Offset	0x0000 0260		
Physical Address	0x5201 0A60	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient. 011111111111 = 2047/256 = 7.99609375 011111111110 = 2046/256 000011111111 = 255/256 000100000000 = 256/256 = 1 000100000001 = 257/256 000000000001 = 1/256 000000000000 = 0/256 = 0 111111111111 = -1/256 = -0.00390625 111111111110 = -2/256 100000000001 = -2047/256 100000000000 = -2048/256 = -8.	RW	0x100

Table 8-862. Register Call Summary for Register IPIPE_RGB2_MUL_RR

ISS ISP
- ISS ISP IPIPE Second RGB2RGB Conversion Matrix: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-863. IPIPE_RGB2_MUL_GR

Address Offset	0x0000 0264		
Physical Address	0x5201 0A64	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-864. Register Call Summary for Register IPIPE_RGB2_MUL_GR

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-865. IPIPE_RGB2_MUL_BR

Address Offset	0x0000 0268		
Physical Address	0x5201 0A68	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-866. Register Call Summary for Register IPIPE_RGB2_MUL_BR

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-867. IPIPE_RGB2_MUL_RG

Address Offset	0x0000 026C		
Physical Address	0x5201 0A6C	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-868. Register Call Summary for Register IPIPE_RGB2_MUL_RG

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-869. IPIPE_RGB2_MUL_GG

Address Offset	0x0000 0270		
Physical Address	0x5201 0A70	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x100

Table 8-870. Register Call Summary for Register IPIPE_RGB2_MUL_GG

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-871. IPIPE_RGB2_MUL_BG

Address Offset	0x0000 0274		
Physical Address	0x5201 0A74	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-872. Register Call Summary for Register IPIPE_RGB2_MUL_BG

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-873. IPIPE_RGB2_MUL_RB

Address Offset	0x0000 0278		
Physical Address	0x5201 0A78	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-874. Register Call Summary for Register IPIPE_RGB2_MUL_RB

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-875. IPIPE_RGB2_MUL_GB

Address Offset	0x0000 027C		
Physical Address	0x5201 0A7C	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x000

Table 8-876. Register Call Summary for Register IPIPE_RGB2_MUL_GB

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-877. IPIPE_RGB2_MUL_BB

Address Offset	0x0000 0280		
Physical Address	0x5201 0A80	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The matrix coefficient.	RW	0x100

Table 8-878. Register Call Summary for Register IPIPE_RGB2_MUL_BB

ISS ISP
- ISS ISP IPIPE Second RGB2RGB Conversion Matrix: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

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Table 8-879. IPIPE_RGB2_OFT_OR

Address Offset	0x0000 0284		
Physical Address	0x5201 0A84	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for R S10 number: -1024 to + 1023	RW	0x000

Table 8-880. Register Call Summary for Register IPIPE_RGB2_OFT_OR

ISS ISP

- ISS ISP IPIPE Second RGB2RGB Conversion Matrix: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-881. IPIPE_RGB2_OFT_OG

Address Offset	0x0000 0288		
Physical Address	0x5201 0A88	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for G S10 number: -1024 to + 1023	RW	0x000

Table 8-882. Register Call Summary for Register IPIPE_RGB2_OFT_OG

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-883. IPIPE_RGB2_OFT_OB

Address Offset	0x0000 028C		
Physical Address	0x5201 0A8C	**Instance**	ISS_IPIPE
Description	RGB to RGB conversion after gamma		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for B S10 number: -1024 to + 1023	RW	0x000

Table 8-884. Register Call Summary for Register IPIPE_RGB2_OFT_OB

ISS ISP

- ISS ISP IPIPE Second RGB2RGB Conversion Matrix: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-885. IPIPE_YUV_ADJ

Address Offset	0x0000 0294		
Physical Address	0x5201 0A94	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BRT								CRT							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	BRT	The offset value for brightness control.	RW	0x00
7:0	CRT	The multiplier coefficient value for contrast control. 00000000 = 0/16 = 0 00000001 = 1/16 00001111 = 15/16 00010000 = 16/16 = 1 00010001 = 17/16 11111110 = 254/16 11111111 = 255/16 = 15.9375	RW	0x10

Table 8-886. Register Call Summary for Register IPIPE_YUV_ADJ

ISS ISP

- ISS ISP IPIPE RGB2YCbCr Conversion Matrix: [0] [1]
- ISS ISP IPIPE 2D Edge-Enhancer: [2] [3]
- ISS ISP IPIPE Global Initialization: [4] [5]
- ISS IPIPE Register Summary: [6]

Table 8-887. IPIPE_YUV_MUL_RY

Address Offset	0x0000 0298		
Physical Address	0x5201 0A98	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Matrix Coefficient for RY (S4.8 = -8 - +7.996)	RW	0x04D

Table 8-888. Register Call Summary for Register IPIPE_YUV_MUL_RY

ISS ISP

- ISS ISP IPIPE RGB2YCbCr Conversion Matrix: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-889. IPIPE_YUV_MUL_GY

Address Offset	0x0000 029C		
Physical Address	0x5201 0A9C	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Matrix Coefficient for GY (S4.8 = -8 - +7.996)	RW	0x096

Table 8-890. Register Call Summary for Register IPIPE_YUV_MUL_GY

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-891. IPIPE_YUV_MUL_BY

Address Offset	0x0000 02A0		
Physical Address	0x5201 0AA0	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Matrix Coefficient for BY (S4.8 = -8 - +7.996)	RW	0x01D

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Table 8-892. Register Call Summary for Register IPIPE_YUV_MUL_BY

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-893. IPIPE_YUV_MUL_RCB

Address Offset	0x0000 02A4		
Physical Address	0x5201 0AA4	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0xFD5

Table 8-894. Register Call Summary for Register IPIPE_YUV_MUL_RCB

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-895. IPIPE_YUV_MUL_GCB

Address Offset	0x0000 02A8		
Physical Address	0x5201 0AA8	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0xFAB

Table 8-896. Register Call Summary for Register IPIPE_YUV_MUL_GCB

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-897. IPIPE_YUV_MUL_BCB

Address Offset	0x0000 02AC		
Physical Address	0x5201 0AAC	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x080

Table 8-898. Register Call Summary for Register IPIPE_YUV_MUL_BCB

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-899. IPIPE_YUV_MUL_RCR

Address Offset	0x0000 02B0		
Physical Address	0x5201 0AB0	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0x080

Table 8-900. Register Call Summary for Register IPIPE_YUV_MUL_RCR

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-901. IPIPE_YUV_MUL_GCR

Address Offset	0x0000 02B4		
Physical Address	0x5201 0AB4	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0xF95

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Table 8-902. Register Call Summary for Register IPIPE_YUV_MUL_GCR

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-903. IPIPE_YUV_MUL_BCR

Address Offset	0x0000 02B8		
Physical Address	0x5201 0AB8	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	The matrix coefficient.	RW	0xFEB

Table 8-904. Register Call Summary for Register IPIPE_YUV_MUL_BCR

ISS ISP

- ISS ISP IPIPE RGB2YCbCr Conversion Matrix: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-905. IPIPE_YUV_OFT_Y

Address Offset	0x0000 02BC		
Physical Address	0x5201 0ABC	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED					VAL										

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for Y	RW	0x000

Table 8-906. Register Call Summary for Register IPIPE_YUV_OFT_Y

ISS ISP

- ISS ISP IPIPE RGB2YCbCr Conversion Matrix: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

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Table 8-907. IPIPE_YUV_OFT_CB

Address Offset	0x0000 02C0		
Physical Address	0x5201 0AC0	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for Cb For Cb/Cr, set (0x80 + offset value) here. (0x80 for zero offset.)	RW	0x080

Table 8-908. Register Call Summary for Register IPIPE_YUV_OFT_CB

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-909. IPIPE_YUV_OFT_CR

Address Offset	0x0000 02C4		
Physical Address	0x5201 0AC4	**Instance**	ISS_IPIPE
Description	RGB to YUV Conversion Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	VAL	The output offset value for Cr For Cb/Cr, set (0x80 + offset value) here. (0x80 for zero offset.)	RW	0x080

Table 8-910. Register Call Summary for Register IPIPE_YUV_OFT_CR

ISS ISP

- ISS ISP IPIPE RGB2YCbCr Conversion Matrix: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

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Table 8-911. IPIPE_YUV_PHS

Address Offset	0x0000 02C8		
Physical Address	0x5201 0AC8	**Instance**	ISS_IPIPE
Description	YUV4:2:2 down sampling register. This register controls the YUV4:4:4 to YUV4:2:2 chroma downsampling. This register is valid if IPIPE_SRC_FMT.FMT = 0 (RAW input and YUV output). IPIPE_YUV_PHS = 0 leads to pure subsampling, no filtering, cosited chroma output. IPIPE_YUV_PHS = 1 leads to (1, 1) >> 1 filtering, centered chroma output. IPIPE_YUV_PHS = 2 leads to (1, 2, 1) >> 1 filtering, cosited chroma output. IPIPE_YUV_PHS = 3 leads to (1, 3, 3, 1) >> 3 filtering, centered chroma output. When the chroma output is cosited, and that downsampling is enabled in the RESIZER module, one need to take care that the averager disrupts the relative phase for luma and chroma color components. The RZA_H_PHS_ADJ and RZB_H_PHS_ADJ registers need to be used to fix the disruption.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														LPF	POS

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	LPF	121-LPF enable for chrominance samples. This register is valid if IPIPE_SRC_FMT.FMT = 0 (RAW input and YUV output). 0x0: off 0x1: on	RW	0
0	POS	This bit sets the output position of the chrominance sample with regards to the luma sample positions. One can choose between centered and cosited. This register is valid if IPIPE_SRC_FMT.FMT = 0 (RAW input and YUV output). The RESIZER module does not change the relative position of the chroma samples vs. the luma samples between the input and output and the chroma position at the output of the IPIPE module and at the output of the RESIZER module must be identical. In other words, we must have RSZ_YUV_PHS.POS = IPIPE_YUV_PHS.POS. 0x0: Cosited = same position with luminance 0x1: Centered = middle of the luminance	RW	0

Table 8-912. Register Call Summary for Register IPIPE_YUV_PHS

ISS ISP

- ISS ISP IPIPE 4:2:2 Conversion Module: [0] [1]
- ISS ISP RSZ Functional Description: [2]
- ISS ISP IPIPE Global Initialization: [3] [4]
- ISS RESIZER Register Description: [5]
- ISS IPIPE Register Summary: [6]
- ISS IPIPE Register Description: [7] [8] [9] [10] [11]

Table 8-913. IPIPE_YEE_EN

Address Offset	0x0000 02D4		
Physical Address	0x5201 0AD4	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	The on/off selection of the Edge enhancer. 0x0: Disable 0x1: Enable	RW	0

Table 8-914. Register Call Summary for Register IPIPE_YEE_EN

ISS ISP
- ISS ISP IPIPE 2D Edge-Enhancer: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-915. IPIPE_YEE_TYP

Address Offset	0x0000 02D8		
Physical Address	0x5201 0AD8	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														HAL	SEL

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	HAL	Halo reduction in Edge Sharpener module	RW	0
0	SEL	Merging method between Edge Enhancer and Edge Sharpener 0x0: EE + ES 0x1: Maximum (EE, ES)	RW	0

Table 8-916. Register Call Summary for Register IPIPE_YEE_TYP

ISS ISP
- ISS ISP IPIPE 2D Edge-Enhancer: [0] [1]
- ISS ISP IPIPE Global Initialization: [2]
- ISS IPIPE Register Summary: [3]

Table 8-917. IPIPE_YEE_SHF

Address Offset	0x0000 02DC		
Physical Address	0x5201 0ADC	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								SHF							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3:0	SHF	Down shift length of high pass filter (HPF) in edge enhancer.	RW	0x0

Table 8-918. Register Call Summary for Register IPIPE_YEE_SHF

ISS ISP

- ISS ISP IPIPE 2D Edge-Enhancer: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-919. IPIPE_YEE_MUL_00

Address Offset	0x0000 02E0		
Physical Address	0x5201 0AE0	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED						VAL									

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF. 0111111111 = 511 0111111110 = 510 0000000001 = 1 0000000000 = 0 1111111111 = -1 1000000001 = -511 1000000000 = -512	RW	0x000

Table 8-920. Register Call Summary for Register IPIPE_YEE_MUL_00

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-921. IPIPE_YEE_MUL_01

Address Offset	0x0000 02E4		
Physical Address	0x5201 0AE4	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED						VAL									

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-922. Register Call Summary for Register IPIPE_YEE_MUL_01

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-923. IPIPE_YEE_MUL_02

Address Offset	0x0000 02E8		
Physical Address	0x5201 0AE8	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-924. Register Call Summary for Register IPIPE_YEE_MUL_02

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-925. IPIPE_YEE_MUL_10

Address Offset	0x0000 02EC		
Physical Address	0x5201 0AEC	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-926. Register Call Summary for Register IPIPE_YEE_MUL_10

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-927. IPIPE_YEE_MUL_11

Address Offset	0x0000 02F0		
Physical Address	0x5201 0AF0	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-928. Register Call Summary for Register IPIPE_YEE_MUL_11

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-929. IPIPE_YEE_MUL_12

Address Offset	0x0000 02F4		
Physical Address	0x5201 0AF4	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-930. Register Call Summary for Register IPIPE_YEE_MUL_12

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-931. IPIPE_YEE_MUL_20

Address Offset	0x0000 02F8		
Physical Address	0x5201 0AF8	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-932. Register Call Summary for Register IPIPE_YEE_MUL_20

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-933. IPIPE_YEE_MUL_21

Address Offset	0x0000 02FC		
Physical Address	0x5201 0AFC	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-934. Register Call Summary for Register IPIPE_YEE_MUL_21

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-935. IPIPE_YEE_MUL_22

Address Offset	0x0000 0300		
Physical Address	0x5201 0B00	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9:0	VAL	Multiplier coefficient in HPF.	RW	0x000

Table 8-936. Register Call Summary for Register IPIPE_YEE_MUL_22

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-937. IPIPE_YEE_THR

Address Offset	0x0000 0304		
Physical Address	0x5201 0B04	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:6	RESERVED		R	0x000
5:0	VAL	Edge Enhancer lower threshold before referring to LUT. If HPF <IPIPE_YEE_THR -> output is HPF + IPIPE_YEE_THR If HPF >IPIPE_YEE_THR -> output is HPF - IPIPE_YEE_THR Otherwise, output is zero.	RW	0x00

Table 8-938. Register Call Summary for Register IPIPE_YEE_THR

ISS ISP

- ISS ISP IPIPE 2D Edge-Enhancer: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3] [4] [5] [6]

Table 8-939. IPIPE_YEE_E_GAN

Address Offset	0x0000 0308		
Physical Address	0x5201 0B08	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Edge sharpener gain	RW	0x000

Table 8-940. Register Call Summary for Register IPIPE_YEE_E_GAN

ISS ISP

- ISS ISP IPIPE 2D Edge-Enhancer: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

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Table 8-941. IPIPE_YEE_E_THR_1

Address Offset	0x0000 030C		
Physical Address	0x5201 0B0C	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VAL											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VAL	Edge sharpener HPF value lower limit	RW	0x000

Table 8-942. Register Call Summary for Register IPIPE_YEE_E_THR_1

ISS ISP

- ISS ISP IPIPE 2D Edge-Enhancer: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-943. IPIPE_YEE_E_THR_2

Address Offset	0x0000 0310		
Physical Address	0x5201 0B10	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:6	RESERVED		R	0x000
5:0	VAL	Edge sharpener HPF value upper limit (after 6 bit right shift)	RW	0x00

Table 8-944. Register Call Summary for Register IPIPE_YEE_E_THR_2

ISS ISP

- ISS ISP IPIPE 2D Edge-Enhancer: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-945. IPIPE_YEE_G_GAN

Address Offset	0x0000 0314		
Physical Address	0x5201 0B14	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	Edge sharpener, gain value on gradient	RW	0x00

Table 8-946. Register Call Summary for Register IPIPE_YEE_G_GAN

ISS ISP

- ISS ISP IPIPE 2D Edge-Enhancer: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-947. IPIPE_YEE_G_OFT

Address Offset	0x0000 0318		
Physical Address	0x5201 0B18	**Instance**	ISS_IPIPE
Description	Edge Enhancer Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:6	RESERVED		R	0x000
5:0	VAL	Edge sharpener, offset value on gradient	RW	0x00

Table 8-948. Register Call Summary for Register IPIPE_YEE_G_OFT

ISS ISP

- ISS ISP IPIPE 2D Edge-Enhancer: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	VAL	The threshold of the gain function for HPF value	RW	0x00

Table 8-949. IPIPE_BOX_EN

Address Offset	0x0000 0380		
Physical Address	0x5201 0B80	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	This bit enables or disables the BOXCAR functionality. The BOXCAR output is written to SDRAM. One need to set the IPIPE_BOX_SDR_SAD_H and IPIPE_BOX_SDR_SAD_L registers with the appropriate address. 0x0: Disable 0x1: Enable	RW	0

Table 8-950. Register Call Summary for Register IPIPE_BOX_EN

ISS ISP
- ISS ISP IPIPE Boxcar: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-951. IPIPE_BOX_MODE

Address Offset	0x0000 0384		
Physical Address	0x5201 0B84	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															OST

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	OST	The processing mode selection of the Boxcar function. A 0 indicates the mode of the free run, a 1 indicates the mode of the one shot. 0x0: Free run 0x1: One shot	RW	0

Table 8-952. Register Call Summary for Register IPIPE_BOX_MODE

ISS ISP
- ISS ISP IPIPE Boxcar: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]

Table 8-953. IPIPE_BOX_TYP

Address Offset	0x0000 0388		
Physical Address	0x5201 0B88	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															SEL

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	SEL	Block size in boxcar sampling 0x0: 8x8 0x1: 16x16	RW	0

Table 8-954. Register Call Summary for Register IPIPE_BOX_TYP

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-955. IPIPE_BOX_SHF

Address Offset	0x0000 038C		
Physical Address	0x5201 0B8C	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															VAL

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:3	RESERVED		R	0x0000
2:0	VAL	The down shift value applied to the boxcar computation result. R out = SUM (Rij) >> SHF G out = (SUM (Gr ij)/2 + SUM (Gr ij)/2) >> SHF B out = SUM (Gij) >> SHF	RW	0x0

Table 8-956. Register Call Summary for Register IPIPE_BOX_SHF

ISS ISP
- ISS ISP IPIPE Boxcar: [0] [1]
- ISS ISP IPIPE Global Initialization: [2]
- ISS IPIPE Register Summary: [3]

Table 8-957. IPIPE_BOX_SDR_SAD_H

Address Offset	0x0000 0390		
Physical Address	0x5201 0B90	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	VAL	The higher 11 bits of the first address of output in memory.	RW	0x0000

Table 8-958. Register Call Summary for Register IPIPE_BOX_SDR_SAD_H

ISS ISP

- ISS ISP IPIPE Boxcar: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3]

Table 8-959. IPIPE_BOX_SDR_SAD_L

Address Offset	0x0000 0394		
Physical Address	0x5201 0B94	**Instance**	ISS_IPIPE
Description	Boxcar Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL														VAL_RESERVED			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:5	VAL	The lower 16 bits of the first address of output in memory.	RW	0x000
4:0	VAL_RESERVED	Ensures 32-byte alignment.	R	0x00

Table 8-960. Register Call Summary for Register IPIPE_BOX_SDR_SAD_L

ISS ISP

- ISS ISP IPIPE Boxcar: [0]
- ISS ISP IPIPE Global Initialization: [1]
- ISS IPIPE Register Summary: [2]
- ISS IPIPE Register Description: [3]

Table 8-961. IPIPE_HST_EN

Address Offset	0x0000 039C		
Physical Address	0x5201 0B9C	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															EN

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	EN	This bit enables or disables the HISTOGRAM functionality. When enabled, the HISTOGRAM computation will start the processing from the next rising edge of the VD pulse. If the processing mode of the HISTOGRAM is one shot, the enable bit will be cleared to 0 immediately after the processing has started. 0x0: disable 0x1: start/busy	RW	0

Table 8-962. Register Call Summary for Register IPIPE_HST_EN

ISS ISP

- ISS ISP IPIPE Histogram: [0] [1]
- ISS ISP IPIPE Global Initialization: [2]
- ISS IPIPE Register Summary: [3]

Table 8-963. IPIPE_HST_MODE

Address Offset	0x0000 03A0		
Physical Address	0x5201 0BA0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															OST

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	OST	The processing mode selection of the Histogram module. A 0 indicates the mode of the free run, a 1 indicates the mode of the one shot. 0x0: Free run 0x1: One shot	RW	0

Table 8-964. Register Call Summary for Register IPIPE_HST_MODE

ISS ISP

- ISS ISP IPIPE Histogram: [0] [1]
- ISS ISP IPIPE Global Initialization: [2]
- ISS IPIPE Register Summary: [3]

Table 8-965. IPIPE_HST_SEL

Address Offset	0x0000 03A4		
Physical Address	0x5201 0BA4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED													SEL	TYP	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:3	RESERVED		R	0x0000
2	SEL	Input selection. When SEL0=0, RGBY are sampled from the output of the line buffer in noise filter-2. When SEL0=1, YCbCr are sampled at the output of RGB2YCbCr module. Y is sampled twice. 0x0: From noise filter input 0x1: From RGBtoYUV	RW	0
1:0	TYP	G selection in Bayer mode (SEL0=0) 0x0: Gb 0x1: Gr 0x3: Reserved 0x2: (Gb+Gr)/2	RW	0x0

Table 8-966. Register Call Summary for Register IPIPE_HST_SEL

ISS ISP

- ISS ISP IPIPE Histogram: [0] [1]
- ISS ISP IPIPE Global Initialization: [2] [3] [4]
- ISS IPIPE Register Summary: [5]

Table 8-967. IPIPE_HST_PARA

Address Offset	0x0000 03A8		
Physical Address	0x5201 0BA8	**Instance**	ISS_IPIPE
Description	Histogram COL0, COL1, COL2, and COL3 should be set to 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		BIN		SHF				COL3	COL2	COL1	COL0	RGN3	RGN2	RGN1	RGN0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:12	BIN	The number of the bins. 0x0: 32 0x1: 64 0x3: 256 0x2: 128	RW	0x0
11:8	SHF	The shift length of the input data. data = (INPUT >> SHF)	RW	0x0
7	COL3	The on/off selection of the color pattern 3 (Y). 0x0: Disable 0x1: Enable	RW	0

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Bits	Field Name	Description	Type	Reset
6	COL2	The on/off selection of the color pattern 2 (B). 0x0: Disable 0x1: Enable	RW	0
5	COL1	The on/off selection of the color pattern 1 (G). 0x0: Disable 0x1: Enable	RW	0
4	COL0	The on/off selection of the color pattern 0 (R). 0x0: Disable 0x1: Enable	RW	0
3	RGN3	The on/off selection of the region 3. 0x0: Disable 0x1: Enable	RW	0
2	RGN2	The on/off selection of the region 2. 0x0: Disable 0x1: Enable	RW	0
1	RGN1	The on/off selection of the region 1. 0x0: Disable 0x1: Enable	RW	0
0	RGN0	The on/off selection of the region 0. 0x0: Disable 0x1: Enable	RW	0

Table 8-968. Register Call Summary for Register IPIPE_HST_PARA

ISS ISP

- ISS ISP IPIPE Histogram: [0] [1] [2] [3]
- ISS ISP IPIPE Global Initialization: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- ISS IPIPE Register Summary: [14]

Table 8-969. IPIPE_HST_0_VPS

Address Offset	0x0000 03AC		
Physical Address	0x5201 0BAC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 0 will start the Histogram processing from VAL line. VAL[0] can not be written.	RW	0x000

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Bits	Field Name	Description	Type	Reset
0	VAL_RESERVED	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 0 will start the Histogram processing from VAL line. VAL[0] can not be written.	R	0

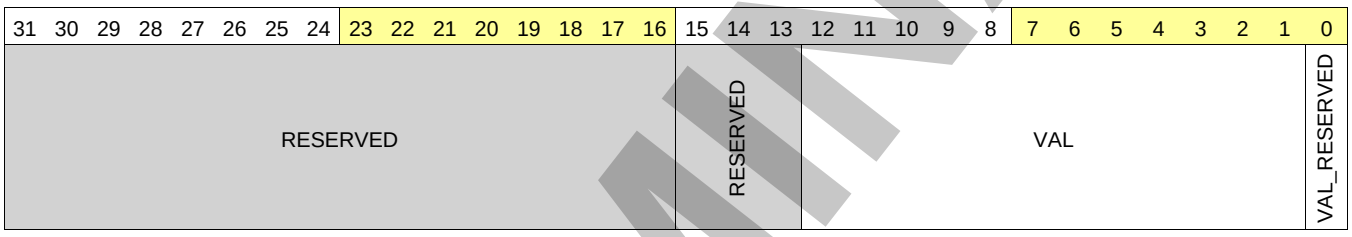
Table 8-970. Register Call Summary for Register IPIPE_HST_0_VPS

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-971. IPIPE_HST_0_VSZ

Address Offset	0x0000 03B0		
Physical Address	0x5201 0BB0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical size of the region 0. The Histogram processing of the region 0 will process (VAL+1) lines.	RW	0x000
0	VAL_RESERVED	The vertical size of the region 0. The Histogram processing of the region 0 will process (VAL+1) lines. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-972. Register Call Summary for Register IPIPE_HST_0_VSZ

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-973. IPIPE_HST_0_HPS

Address Offset	0x0000 03B4		
Physical Address	0x5201 0BB4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 0 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 0 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	R	0

Table 8-974. Register Call Summary for Register IPIPE_HST_0_HPS

ISS ISP

- ISS ISP IPIPE Global Initialization: [0] [1] [2] [3]
- ISS IPIPE Register Summary: [4]

Table 8-975. IPIPE_HST_0_HSZ

Address Offset	0x0000 03B8		
Physical Address	0x5201 0BB8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VAL							VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal size of the region 0. The Histogram processing of the region 0 will process (VAL+1) clocks. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The horizontal size of the region 0. The Histogram processing of the region 0 will process (VAL+1) clocks. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-976. Register Call Summary for Register IPIPE_HST_0_HSZ

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-977. IPIPE_HST_1_VPS

Address Offset	0x0000 03BC		
Physical Address	0x5201 0BBC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 1 will start the Histogram processing from VAL line. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 1 will start the Histogram processing from VAL line. VAL[0] can not be written.	R	0

Table 8-978. Register Call Summary for Register IPIPE_HST_1_VPS

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-979. IPIPE_HST_1_VSZ

Address Offset	0x0000 03C0		
Physical Address	0x5201 0BC0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical size of the region 1. The Histogram processing of the region 1 will process (VAL+1) lines. VAL[0] cannot be written.	RW	0x000

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Bits	Field Name	Description	Type	Reset
0	VAL_RESERVED	The vertical size of the region 1. The Histogram processing of the region 1 will process (VAL+1) lines. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-980. Register Call Summary for Register IPIPE_HST_1_VSZ

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-981. IPIPE_HST_1_HPS

Address Offset	0x0000 03C4		
Physical Address	0x5201 0BC4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 1 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 1 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	R	0

Table 8-982. Register Call Summary for Register IPIPE_HST_1_HPS

ISS ISP

- ISS IPIPE Register Summary: [0]

Table 8-983. IPIPE_HST_1_HSZ

Address Offset	0x0000 03C8		
Physical Address	0x5201 0BC8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

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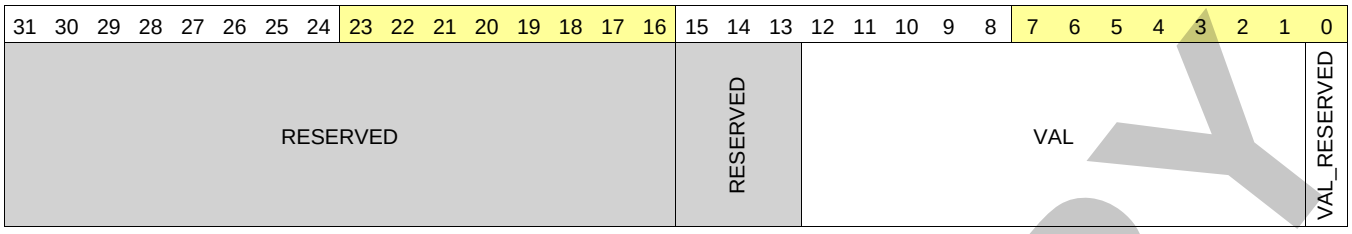


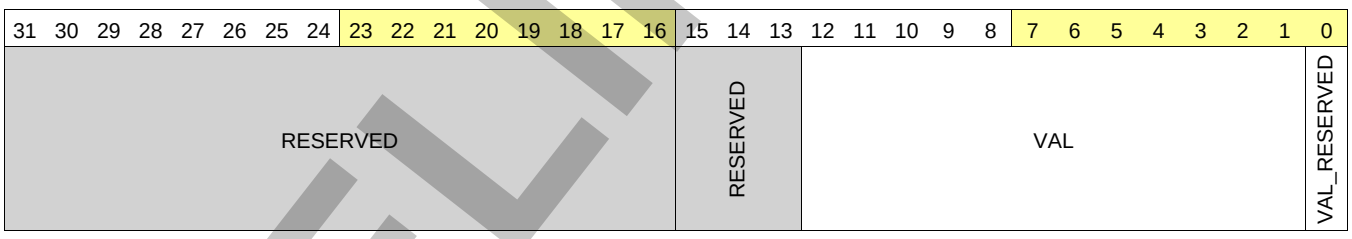
Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal size of the region 1. The Histogram processing of the region 1 will process (VAL+1) clocks. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The horizontal size of the region 1. The Histogram processing of the region 1 will process (VAL+1) clocks. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-984. Register Call Summary for Register IPIPE_HST_1_HSZ

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-985. IPIPE_HST_2_VPS

Address Offset	0x0000 03CC		
Physical Address	0x5201 0BCC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 2 will start the Histogram processing from VAL line. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 2 will start the Histogram processing from VAL line. VAL[0] can not be written.	R	0

Table 8-986. Register Call Summary for Register IPIPE_HST_2_VPS

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-987. IPIPE_HST_2_VSZ

Address Offset	0x0000 03D0		
Physical Address	0x5201 0BD0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical size of the region 2. The Histogram processing of the region 2 will process (VAL+1) lines. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The vertical size of the region 2. The Histogram processing of the region 2 will process (VAL+1) lines. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-988. Register Call Summary for Register IPIPE_HST_2_VSZ

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-989. IPIPE_HST_2_HPS

Address Offset	0x0000 03D4		
Physical Address	0x5201 0BD4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 2 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	RW	0x000

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Bits	Field Name	Description	Type	Reset
0	VAL_RESERVED	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 2 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	R	0

Table 8-990. Register Call Summary for Register IPIPE_HST_2_HPS

ISS ISP
- ISS IPIPE Register Summary: [0]

Table 8-991. IPIPE_HST_2_HSZ

Address Offset	0x0000 03D8		
Physical Address	0x5201 0BD8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal size of the region 2. The Histogram processing of the region 2 will process (VAL+1) clocks. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The horizontal size of the region 2. The Histogram processing of the region 2 will process (VAL+1) clocks. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-992. Register Call Summary for Register IPIPE_HST_2_HSZ

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-993. IPIPE_HST_3_VPS

Address Offset	0x0000 03DC		
Physical Address	0x5201 0BDC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 3 will start the Histogram processing from VAL line. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The vertical position of the region 0 from the IPIPE_SRC_VPS. The region 3 will start the Histogram processing from VAL line. VAL[0] can not be written.	R	0

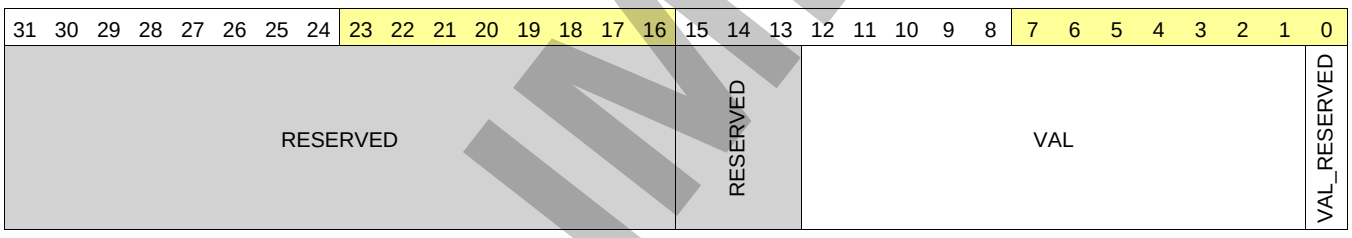
Table 8-994. Register Call Summary for Register IPIPE_HST_3_VPS

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-995. IPIPE_HST_3_VSZ

Address Offset	0x0000 03E0		
Physical Address	0x5201 0BE0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The vertical size of the region 3. The Histogram processing of the region 3 will process (VAL+1) lines. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The vertical size of the region 3. The Histogram processing of the region 3 will process (VAL+1) lines. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-996. Register Call Summary for Register IPIPE_HST_3_VSZ

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-997. IPIPE_HST_3_HPS

Address Offset	0x0000 03E4		
Physical Address	0x5201 0BE4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 3 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	RW	0x000
0	VAL_RESERVED	The horizontal position of the region 0 from the IPIPE_SRC_HPS. The region 3 will start the Histogram processing from VAL clocks. VAL[0] can not be written.	R	0

Table 8-998. Register Call Summary for Register IPIPE_HST_3_HPS

ISS ISP

- ISS IPIPE Register Summary: [0]

Table 8-999. IPIPE_HST_3_HSZ

Address Offset	0x0000 03E8		
Physical Address	0x5201 0BE8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			VAL												VAL_RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:1	VAL	The horizontal size of the region 3. The Histogram processing of the region 3 will process (VAL+1) clocks. VAL[0] cannot be written.	RW	0x000
0	VAL_RESERVED	The horizontal size of the region 3. The Histogram processing of the region 3 will process (VAL+1) clocks. VAL[0] cannot be written.	R Rreturns 1s	1

Table 8-1000. Register Call Summary for Register IPIPE_HST_3_HSZ

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

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Table 8-1001. IPIPE_HST_TBL

Address Offset	0x0000 03EC		
Physical Address	0x5201 0BEC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														CLR	SEL

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	CLR	Histogram memory clear. The histogram can be cleared before the start of operations. However, the clear takes 512 cycles and therefore: + if line size > 512, the first line must not be used for histogram computation. + if line size < 512, ceil (512/line size) lines must not be used for histogram computation. It's the programmer's responsibility to set the histogram computation area outside the "clear" area. 0x0: Disable 0x1: Enable	RW	0
0	SEL	This bit must be used to select which memory is used to store the histogram data. By selecting alternatively one or the other bit, one can double buffer the histogram output buffer. The 4-KiB memory can either be read by the CPU or a DMA request. 0x0: Use Table 0 and 1 = 4 KiB in the memory ISP map. 0x1: Use Table 2 and 3 = 4 KiB in the memory ISP map.	RW	0

Table 8-1002. Register Call Summary for Register IPIPE_HST_TBL

ISS ISP

- ISS ISP DMA Requests: [0] [1]
- ISS ISP IPIPE Histogram: [2] [3]
- ISS ISP IPIPE Global Initialization: [4] [5]
- ISS IPIPE Register Summary: [6]

Table 8-1003. IPIPE_HST_MUL_R

Address Offset	0x0000 03F0		
Physical Address	0x5201 0BF0	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								GAIN							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	GAIN	Gain	RW	0x00

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Table 8-1004. Register Call Summary for Register IPIPE_HST_MUL_R

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-1005. IPIPE_HST_MUL_GR

Address Offset	0x0000 03F4		
Physical Address	0x5201 0BF4	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								GAIN							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	GAIN	Gain	RW	0x00

Table 8-1006. Register Call Summary for Register IPIPE_HST_MUL_GR

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-1007. IPIPE_HST_MUL_GB

Address Offset	0x0000 03F8		
Physical Address	0x5201 0BF8	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								GAIN							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	GAIN	Gain	RW	0x00

Table 8-1008. Register Call Summary for Register IPIPE_HST_MUL_GB

ISS ISP

- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

Table 8-1009. IPIPE_HST_MUL_B

Address Offset	0x0000 03FC		
Physical Address	0x5201 0BFC	**Instance**	ISS_IPIPE
Description	Histogram		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								GAIN							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	GAIN	Gain	RW	0x00

Table 8-1010. Register Call Summary for Register IPIPE_HST_MUL_B

ISS ISP
- ISS ISP IPIPE Global Initialization: [0]
- ISS IPIPE Register Summary: [1]

8.3.5.6 ISS ISIF Registers

CAUTION

The ISS ISIF registers are limited to 32 bit and 16 bit data accesses; 8bit data access is not allowed and can corrupt register content.

8.3.5.6.1 ISS ISIF Register Summary

Table 8-1011. ISS ISIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISIF Base Address
ISIF_SYNCEN	RW	32	0x0000 0000	0x5201 1000
ISIF_MODESET	RW	32	0x0000 0004	0x5201 1004
ISIF_HDW	RW	32	0x0000 0008	0x5201 1008
ISIF_VDW	RW	32	0x0000 000C	0x5201 100C
ISIF_PPLN	RW	32	0x0000 0010	0x5201 1010
ISIF_LPFR	RW	32	0x0000 0014	0x5201 1014
ISIF_SPH	RW	32	0x0000 0018	0x5201 1018
ISIF_LNH	RW	32	0x0000 001C	0x5201 101C
ISIF_SLV0	RW	32	0x0000 0020	0x5201 1020
ISIF_SLV1	RW	32	0x0000 0024	0x5201 1024
ISIF_LNV	RW	32	0x0000 0028	0x5201 1028
ISIF_CULH	RW	32	0x0000 002C	0x5201 102C
ISIF_CULV	RW	32	0x0000 0030	0x5201 1030
ISIF_HSIZE	RW	32	0x0000 0034	0x5201 1034
ISIF_SDOFST	RW	32	0x0000 0038	0x5201 1038
ISIF_CADU	RW	32	0x0000 003C	0x5201 103C
ISIF_CADL	RW	32	0x0000 0040	0x5201 1040
ISIF_LINCFG0	RW	32	0x0000 0044	0x5201 1044
ISIF_LINCFG1	RW	32	0x0000 0048	0x5201 1048
ISIF_CCOLP	RW	32	0x0000 004C	0x5201 104C
ISIF_CRGAIN	RW	32	0x0000 0050	0x5201 1050
ISIF_CGRGAIN	RW	32	0x0000 0054	0x5201 1054
ISIF_CGBGAIN	RW	32	0x0000 0058	0x5201 1058
ISIF_CBGAIN	RW	32	0x0000 005C	0x5201 105C
ISIF_COFSTA	RW	32	0x0000 0060	0x5201 1060

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Table 8-1011. ISS ISIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISIF Base Address
RESERVED	R	32	0x0000 0064	0x5201 1064
RESERVED	R	32	0x0000 0068	0x5201 1068
RESERVED	R	32	0x0000 006C	0x5201 106C
ISIF_VDINT0	RW	32	0x0000 0070	0x5201 1070
ISIF_VDINT1	RW	32	0x0000 0074	0x5201 1074
ISIF_VDINT2	RW	32	0x0000 0078	0x5201 1078
ISIF_MISC	RW	32	0x0000 007C	0x5201 107C
ISIF_CGAMMAWD	RW	32	0x0000 0080	0x5201 1080
ISIF_REC656IF	RW	32	0x0000 0084	0x5201 1084
ISIF_CCDCFG	RW	32	0x0000 0088	0x5201 1088
ISIF_DFCCTL	RW	32	0x0000 008C	0x5201 108C
ISIF_VDFSATLV	RW	32	0x0000 0090	0x5201 1090
ISIF_DFCMEMCTL	RW	32	0x0000 0094	0x5201 1094
ISIF_DFCMEM0	RW	32	0x0000 0098	0x5201 1098
ISIF_DFCMEM1	RW	32	0x0000 009C	0x5201 109C
ISIF_DFCMEM2	RW	32	0x0000 00A0	0x5201 10A0
ISIF_DFCMEM3	RW	32	0x0000 00A4	0x5201 10A4
ISIF_DFCMEM4	RW	32	0x0000 00A8	0x5201 10A8
ISIF_CLAMPCFG	RW	32	0x0000 00AC	0x5201 10AC
ISIF_CLDCOFST	RW	32	0x0000 00B0	0x5201 10B0
ISIF_CLSV	RW	32	0x0000 00B4	0x5201 10B4
ISIF_CLHWIN0	RW	32	0x0000 00B8	0x5201 10B8
ISIF_CLHWIN1	RW	32	0x0000 00BC	0x5201 10BC
ISIF_CLHWIN2	RW	32	0x0000 00C0	0x5201 10C0
ISIF_CLVRV	RW	32	0x0000 00C4	0x5201 10C4
ISIF_CLVWIN0	RW	32	0x0000 00C8	0x5201 10C8
ISIF_CLVWIN1	RW	32	0x0000 00CC	0x5201 10CC
ISIF_CLVWIN2	RW	32	0x0000 00D0	0x5201 10D0
ISIF_CLVWIN3	RW	32	0x0000 00D4	0x5201 10D4
ISIF_LSCHOFST	RW	32	0x0000 00D8	0x5201 10D8
ISIF_LSCVOFST	RW	32	0x0000 00DC	0x5201 10DC
ISIF_LSCHVAL	RW	32	0x0000 00E0	0x5201 10E0
ISIF_LSCVVAL	RW	32	0x0000 00E4	0x5201 10E4
ISIF_2DLSCCFG	RW	32	0x0000 00E8	0x5201 10E8
ISIF_2DLSCOFST	RW	32	0x0000 00EC	0x5201 10EC
ISIF_2DLSCINI	RW	32	0x0000 00F0	0x5201 10F0
ISIF_2DLSCGRBU	RW	32	0x0000 00F4	0x5201 10F4
ISIF_2DLSCGRBL	RW	32	0x0000 00F8	0x5201 10F8
ISIF_2DLSCGROF	RW	32	0x0000 00FC	0x5201 10FC
ISIF_2DLSCORBU	RW	32	0x0000 0100	0x5201 1100
ISIF_2DLSCORBL	RW	32	0x0000 0104	0x5201 1104
ISIF_2DLSCOROF	RW	32	0x0000 0108	0x5201 1108
ISIF_2DLSCIRQEN	RW	32	0x0000 010C	0x5201 110C
ISIF_2DLSCIRQST	RW	32	0x0000 0110	0x5201 1110
ISIF_FMTCFG	RW	32	0x0000 0114	0x5201 1114
ISIF_FMTPLEN	RW	32	0x0000 0118	0x5201 1118
ISIF_FMTSPH	RW	32	0x0000 011C	0x5201 111C

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Table 8-1011. ISS ISIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISIF Base Address
ISIF_FMTLNH	RW	32	0x0000 0120	0x5201 1120
ISIF_FMTLSV	RW	32	0x0000 0124	0x5201 1124
ISIF_FMTLNV	RW	32	0x0000 0128	0x5201 1128
ISIF_FMTRLEN	RW	32	0x0000 012C	0x5201 112C
ISIF_FMTHCNT	RW	32	0x0000 0130	0x5201 1130
ISIF_FMTAPTR0	RW	32	0x0000 0134	0x5201 1134
ISIF_FMTAPTR1	RW	32	0x0000 0138	0x5201 1138
ISIF_FMTAPTR2	RW	32	0x0000 013C	0x5201 113C
ISIF_FMTAPTR3	RW	32	0x0000 0140	0x5201 1140
ISIF_FMTAPTR4	RW	32	0x0000 0144	0x5201 1144
ISIF_FMTAPTR5	RW	32	0x0000 0148	0x5201 1148
ISIF_FMTAPTR6	RW	32	0x0000 014C	0x5201 114C
ISIF_FMTAPTR7	RW	32	0x0000 0150	0x5201 1150
ISIF_FMTAPTR8	RW	32	0x0000 0154	0x5201 1154
ISIF_FMTAPTR9	RW	32	0x0000 0158	0x5201 1158
ISIF_FMTAPTR10	RW	32	0x0000 015C	0x5201 115C
ISIF_FMTAPTR11	RW	32	0x0000 0160	0x5201 1160
ISIF_FMTAPTR12	RW	32	0x0000 0164	0x5201 1164
ISIF_FMTAPTR13	RW	32	0x0000 0168	0x5201 1168
ISIF_FMTAPTR14	RW	32	0x0000 016C	0x5201 116C
ISIF_FMTAPTR15	RW	32	0x0000 0170	0x5201 1170
ISIF_FMTPGMVF0	RW	32	0x0000 0174	0x5201 1174
ISIF_FMTPGMVF1	RW	32	0x0000 0178	0x5201 1178
ISIF_FMTPGMAPU0	RW	32	0x0000 017C	0x5201 117C
ISIF_FMTPGMAPU1	RW	32	0x0000 0180	0x5201 1180
ISIF_FMTPGMAPS0	RW	32	0x0000 0184	0x5201 1184
ISIF_FMTPGMAPS1	RW	32	0x0000 0188	0x5201 1188
ISIF_FMTPGMAPS2	RW	32	0x0000 018C	0x5201 118C
ISIF_FMTPGMAPS3	RW	32	0x0000 0190	0x5201 1190
ISIF_FMTPGMAPS4	RW	32	0x0000 0194	0x5201 1194
ISIF_FMTPGMAPS5	RW	32	0x0000 0198	0x5201 1198
ISIF_FMTPGMAPS6	RW	32	0x0000 019C	0x5201 119C
ISIF_FMTPGMAPS7	RW	32	0x0000 01A0	0x5201 11A0
ISIF_CSCCTL	RW	32	0x0000 01A4	0x5201 11A4
ISIF_CSCM0	RW	32	0x0000 01A8	0x5201 11A8
ISIF_CSCM1	RW	32	0x0000 01AC	0x5201 11AC
ISIF_CSCM2	RW	32	0x0000 01B0	0x5201 11B0
ISIF_CSCM3	RW	32	0x0000 01B4	0x5201 11B4
ISIF_CSCM4	RW	32	0x0000 01B8	0x5201 11B8
ISIF_CSCM5	RW	32	0x0000 01BC	0x5201 11BC
ISIF_CSCM6	RW	32	0x0000 01C0	0x5201 11C0
ISIF_CSCM7	RW	32	0x0000 01C4	0x5201 11C4
ISIF_CLKCTL	RW	32	0x0000 01F8	0x5201 11F8

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8.3.5.6.2 ISS ISIF Register Description

Table 8-1012. ISIF_SYNCEN

Address Offset	0x0000 0000		
Physical Address	0x5201 1000	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														DWEN	SYEN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	DWEN	Controls the storage of image sensor RAW data in memory. This bit is loaded with the timing of the internal VD signal: it becomes active starting at the lead of the VD signal that comes after 1 is written in this bit. 0x0: Disable 0x1: Enable	RW	0
0	SYEN	Controls ON/OFF of VD/HD output. Internal timing generator becomes active and VD/HD output starts when 1 is written in this bit. In case of input, VD/HD loading begins. 0: Disable 1: Enable	RW	0

Table 8-1013. Register Call Summary for Register ISIF_SYNCEN

ISS ISP

- ISS ISP ISIF Write Port: [0]
- ISS ISP ISIF Events and Status Checking: [1]
- ISS ISP ISIF Register Setup: [2] [3]
- ISS ISP ISIF Enable/Disable Hardware: [4] [5] [6] [7] [8] [9]
- ISS ISP ISIF Register Accessibility During Frame Processing: [10]
- ISS ISP ISIF Interframe Operations: [11]
- ISS ISP ISIF Summary of Constraints: [12] [13]
- ISS ISIF Register Summary: [14]

Table 8-1014. ISIF_MODESET

Address Offset	0x0000 0004		
Physical Address	0x5201 1004	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MDFS	HLPF	INPMOD		OVF	CCDW			CCDMD	DPOL	SWEN	FIPOL	HDPOL	VDPOL	FIDD	HDVDD

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	MDFS	Field Status This bit indicates the status of the current FLD signal when the ISIF module is in interlaced mode. Read 0x1: Even field Read 0x0: Odd field	R	0
14	HLPF	Low pass filter enable. When this bit is enabled, a 3-tap (1/4 + 1/2 Z^{-2} + 1/4 Z^{4}) filtering process is performed on the sensor data. 0x0: Disable 0x1: Enable	RW	0
13:12	INPMOD	Data input mode: 0x0: RAW data 0x1: YCbCr 16bit 0x3: Reserved 0x2: YCbCr 8bit	RW	0x2
11	OVF	ISIF module write port overflow status bit If the write port of the ISIF module overflows when writing data to SDRAM, this bit will toggle. 0x0: No overflow pending (r) No action (w) 0x1: Overflow pending (r) Clear overflow (w)	RW	0
10:8	CCDW	This bit enables to shift right (divide) the up-to-12-bit RAW data value when writing out to SDRAM. The effect is that the dynamic of the output signal is decreased. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x6: Reserved 0x1: 1-bit right shift out[15:0] = 00000 & data[11:1] 0x7: Reserved 0x0: No shift out[15:0] = 0000 & data[11:0] 0x2: 2-bit right shift out[15:0] = 000000 & data[11:2] 0x4: 4-bit right shift out[15:0] = 00000000 & data[11:4] 0x5: Reserved 0x3: 3-bit right shift out[15:0] = 0000000 & data[11:3]	RW	0x0
7	CCDMD	Field mode: This bit selects the type of image sensor: interlaced or progressive 0x0: Progressive image sensor 0x1: Interlaced image sensor	RW	0
6	DPOL	Image sensor input data polarity 0x0: No change 0x1: One's complement	RW	0
5	SWEN	External WEN selection In case this bit and SYNCEN.DWEN are set to 1, the external WEN signal is used to store image sensor data to memory. 0x0: WEN not used 0x1: Use external WEN	RW	0

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Bits	Field Name	Description	Type	Reset
4	FIPOL	FLD Signal Polarity 0x0: Positive 0x1: Negative	RW	0
3	HDPOL	HD Sync Signal Polarity 0x0: Positive 0x1: Negative	RW	0
2	VDPOL	VD Sync Signal Polarity 0x0: Positive 0x1: Negative	RW	0
1	FIDD	FLD Signal Direction. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for the start of frame comes. 0x0: Input 0x1: Output	RW	0
0	HDVDD	VD,HD Sync Signal Direction. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for the start of frame comes. 0x0: Input 0x1: Output	RW	0

Table 8-1015. Register Call Summary for Register ISIF_MODESET

ISS ISP

- ISS ISP ISIF Interrupts: [0]
- ISS ISP VP Pixel Clock Inversion: [1] [2]
- ISS ISP ISIF Input Interface: [3] [4]
- ISS ISP ISIF Interface: [5] [6]
- ISS ISP ISIF Low-Pass Filter: [7] [8]
- ISP ISIF Storage Formatter: [9] [10] [11] [12]
- ISS ISP ISIF VDINT0, VDINT1, and VDINT2 Interrupts: [13] [14] [15]
- ISS ISP ISIF Status Checking: [16]
- ISS ISP ISIF Register Setup: [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27]
- ISS ISP ISIF Enable/Disable Hardware: [28] [29] [30] [31]
- ISS ISP ISIF Register Accessibility During Frame Processing: [32]
- ISS ISIF Register Summary: [33]
- ISS ISIF Register Description: [34] [35] [36] [37] [38]

Table 8-1016. ISIF_HDW

Address Offset	0x0000 0008		
Physical Address	0x5201 1008	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				HDW											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	HDW	HD width: Sets width of HD. HD width = HDW + 1 clock	RW	0x000

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Table 8-1017. Register Call Summary for Register ISIF_HDW

ISS ISP

- ISS ISP ISIF Clamp Value for Horizontal Direction: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-1018. ISIF_VDW

Address Offset	0x0000 000C		
Physical Address	0x5201 100C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VDW							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VDW	VD width : Sets width of VD. VD width = VDW + 1 line	RW	0x000

Table 8-1019. Register Call Summary for Register ISIF_VDW

ISS ISP

- ISS ISP ISIF Clamp Value for Vertical Direction: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-1020. ISIF_PPLN

Address Offset	0x0000 0010		
Physical Address	0x5201 1010	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PPLN															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	PPLN	Pixels per line Number of pixel clock periods in one line HD period = PPLN+1 pixel clocks. PPLN is not used when HD and VD are inputs, that is, when VDHDOUT in MODESET is cleared to 0. *This bit field is latched by VD.	RW	0x0000

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Table 8-1021. Register Call Summary for Register ISIF_PPLN

ISS ISP

- ISS ISP ISIF Black Clamp: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISP ISIF Register Accessibility During Frame Processing: [3]
- ISS ISIF Register Summary: [4]

Table 8-1022. ISIF_LPFR

Address Offset	0x0000 0014		
Physical Address	0x5201 1014	**Instance**	ISS_ISIF
Description	Line per Frame/Field		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LPFR															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	LPFR	Half lines per filed or frame Sets number of half lines per frame or field. VD period = (LPFR+1)/2 lines. LPFR is not used when HD and are inputs, that is, when VDHDOUT in MODESET is cleared to 0. *This bit field is latched by VD.	RW	0x0000

Table 8-1023. Register Call Summary for Register ISIF_LPFR

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-1024. ISIF_SPH

Address Offset	0x0000 0018		
Physical Address	0x5201 1018	**Instance**	ISS_ISIF
Description	Start Pixel Horizontal		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								SPH							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:0	SPH	The first pixel in a line to be stored to memory.	RW	0x0000

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Table 8-1025. Register Call Summary for Register ISIF_SPH

ISS ISP

- ISS ISP ISIF Formatter Area Settings: [0]
- ISP ISIF Storage Formatter: [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISP ISIF Register Accessibility During Frame Processing: [3]
- ISS ISP ISIF Summary of Constraints: [4] [5]
- ISS ISIF Register Summary: [6]

Table 8-1026. ISIF_LNH

Address Offset	0x0000 001C		
Physical Address	0x5201 101C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								LNH							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	RESERVED	Reserved	R	0
14:0	LNH	Number of pixels in an line to be stored to memory. Number of pixels = LNH + 1.	RW	0x0000

Table 8-1027. Register Call Summary for Register ISIF_LNH

ISS ISP

- ISS ISP ISIF Formatter Area Settings: [0]
- ISP ISIF Storage Formatter: [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISP ISIF Register Accessibility During Frame Processing: [3]
- ISS ISP ISIF Summary of Constraints: [4] [5] [6]
- ISS ISIF Register Summary: [7]

Table 8-1028. ISIF_SLV0

Address Offset	0x0000 0020		
Physical Address	0x5201 1020	**Instance**	ISS_ISIF
Description	SDRAM output vertical field 0 start line control.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SLV0															

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x0000
14:0	SLV0	Start Line, Vertical (Field 0) Sets line at which data output to SDRAM will begin, measured from the start of VD. *This bit field is latched by VD.	RW	0x0000

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Table 8-1029. Register Call Summary for Register ISIF_SLV0

ISS ISP

- ISP ISIF Storage Formatter: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISP ISIF Summary of Constraints: [3] [4]
- ISS ISIF Register Summary: [5]

Table 8-1030. ISIF_SLV1

Address Offset	0x0000 0024		
Physical Address	0x5201 1024	**Instance**	ISS_ISIF
Description	SDRAM output vertical field 1 start line control.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SLV1															

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x0000
14:0	SLV1	Start Line, Vertical (Field 1) Sets line at which data output to SDRAM will begin, measured from the start of VD. *This bit field is latched by VD.	RW	0x0000

Table 8-1031. Register Call Summary for Register ISIF_SLV1

ISS ISP

- ISP ISIF Storage Formatter: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISP ISIF Summary of Constraints: [3] [4]
- ISS ISIF Register Summary: [5]

Table 8-1032. ISIF_LNV

Address Offset	0x0000 0028		
Physical Address	0x5201 1028	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								LNV							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	RESERVED	The number of lines to be stored to SDRAM.	R	0
14:0	LNV	The number of lines to be stored to memory. Number of lines = LNV + 1	RW	0x0000

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Table 8-1033. Register Call Summary for Register ISIF_LNV

ISS ISP

- ISS ISP ISIF Formatter Area Settings: [0]
- ISP ISIF Storage Formatter: [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISP ISIF Summary of Constraints: [3] [4]
- ISS ISIF Register Summary: [5]

Table 8-1034. ISIF_CULH

Address Offset	0x0000 002C		
Physical Address	0x5201 102C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLHO								CLHE							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CLHO	Culling Pattern in ODD Line: Sets culling pattern when data is loaded into memory (odd lines). Example: 0xAA: 1 / 2 horizontal direction culling. LSB becomes left side on screen. 0x0: Pixel invalid 0x1: Pixel valid	RW	0xFF
7:0	CLHE	Culling Pattern in Even Line: Sets culling pattern when data is loaded into memory (even lines). 0x0: Pixel invalid 0x1: Pixel valid	RW	0xFF

Table 8-1035. Register Call Summary for Register ISIF_CULH

ISS ISP

- ISS ISP ISIF Culling: [0] [1] [2]
- ISS ISP ISIF Register Setup: [3] [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1036. ISIF_CULV

Address Offset	0x0000 0030		
Physical Address	0x5201 1030	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CULV							

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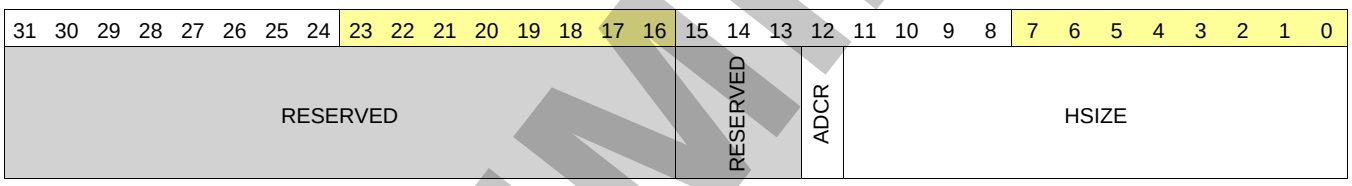
Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	CULV	Culling Pattern in Vertical Line Example: 0x88: 1/4 vertical direction culling. LSB becomes top side on screen. 0x0: Pixel invalid 0x1: Pixel valid	RW	0xFF

Table 8-1037. Register Call Summary for Register ISIF_CULV

ISS ISP
- ISS ISP ISIF Culling: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-1038. ISIF_HSIZE

Address Offset	0x0000 0034		
Physical Address	0x5201 1034	**Instance**	ISS_ISIF
Description	SDRAM output control register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12	ADCR	SDRAM address decrement. By setting this bit, memory address in a line is automatically decreased so that a line can be Horizontally flipped in memory. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x0: Address increment. 0x1: Address decrement.	RW	0
11:0	HSIZE	Memory address offset between the lines. Specify the offset in 32-byte units.	RW	0x000

Table 8-1039. Register Call Summary for Register ISIF_HSIZE

ISS ISP
- ISP ISIF Storage Formatter: [0] [1]
- ISS ISP ISIF Register Setup: [2] [3]
- ISS ISP ISIF Register Accessibility During Frame Processing: [4]
- ISS ISIF Register Summary: [5]
- ISS ISIF Register Description: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]

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Table 8-1040. ISIF_SDOFST

Address Offset	0x0000 0038		
Physical Address	0x5201 1038	**Instance**	ISS_ISIF
Description	SDRAM output control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIINV	FOFST			LOFSTEE				LOFSTOE				LOFSTEO			LOFSTOO

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x0000
14	FIINV	FID polarity: This bit inverse a FID polarity. 0x0: No change 0x1: Inverse FID	RW	0x0
13:12	FOFST	Field line offset value in odd (FID = 1) field 0x0: +1 line 0x1: +2 lines 0x3: +4 lines 0x2: +3 lines	RW	0x0
11:9	LOFSTEE	Field line offset value in even line, even field 0x0: +1 line 0x1: +2 lines 0x2: +3 lines 0x3: +4 lines 0x4: –1 line 0x5: –2 lines 0x6: –3 lines 0x7: –4 lines	RW	0x0
8:6	LOFSTOE	Field line offset value in odd line, even field 0x0: +1 line 0x1: +2 lines 0x2: +3 lines 0x3: +4 lines 0x4: –1 line 0x5: –2 lines 0x6: –3 lines 0x7: – 4 lines	RW	0x0
5:3	LOFSTEO	Field line offset value in even line, odd field 0x0: +1 line 0x1: +2 lines 0x2: +3 lines 0x3: +4 lines 0x4: –1 line 0x5: –2 lines 0x6: –3 lines 0x7: –4 lines	RW	0x0

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Bits	Field Name	Description	Type	Reset
2:0	LOFSTOO	Field line offset value in odd line, odd field 0x0: +1 line 0x1: +2 lines 0x2: +3 lines 0x3: +4 lines 0x4: –1 line 0x5: –2 lines 0x6: –3 lines 0x7: –4 lines	RW	0x0

Table 8-1041. Register Call Summary for Register ISIF_SDOFST

ISS ISP

- ISP ISIF Storage Formatter: [0]
- ISS ISP ISIF Register Accessibility During Frame Processing: [1]
- ISS ISIF Register Summary: [2]

Table 8-1042. ISIF_CADU

Address Offset	0x0000 003C		
Physical Address	0x5201 103C	**Instance**	ISS_ISIF
Description	SDRAM output control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED					CADU											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	CADU	Memory Address (Upper 11-bits): Specifies the memory destination address. The actual address is the value set here multiplied by 32bytes.	RW	0x000

Table 8-1043. Register Call Summary for Register ISIF_CADU

ISS ISP

- ISP ISIF Storage Formatter: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Enable/Disable Hardware: [2] [3]
- ISS ISP ISIF Register Accessibility During Frame Processing: [4]
- ISS ISIF Register Summary: [5]

Table 8-1044. ISIF_CADL

Address Offset	0x0000 0040		
Physical Address	0x5201 1040	**Instance**	ISS_ISIF
Description	SDRAM output control register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CADL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	CADL	Memory Address (Lower 16-bits): Specifies the memory destination address. The actual address is the value set here multiplied by 32bytes.	RW	0x0000

Table 8-1045. Register Call Summary for Register ISIF_CADL

ISS ISP

- ISP ISIF Storage Formatter: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Enable/Disable Hardware: [2] [3]
- ISS ISP ISIF Register Accessibility During Frame Processing: [4]
- ISS ISIF Register Summary: [5]

Table 8-1046. ISIF_LINCFG0

Address Offset	0x0000 0044		
Physical Address	0x5201 1044	**Instance**	ISS_ISIF
Description	INPUT LINEARIZATION CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CORRSFT				RESERVED		LINMD	LINEN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:7	RESERVED		R	0x000
6:4	CORRSFT	Shift up value for the correction value (S10). 0x6: 6-bit left shift 0x1: 1-bit left shift 0x7: Reserved 0x0: No shift 0x2: 2-bit left shift 0x4: 4-bit left shift 0x5: 5-bit left shift 0x3: 3-bit left shift	RW	0x0
3:2	RESERVED		R	0x0
1	LINMD	Linearization Mode: 0x0: Uniform sampling 0x1: Non-uniform sampling	RW	0
0	LINEN	Linearization Enable: 0x0: Disable 0x1: Enable	RW	0

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Table 8-1047. Register Call Summary for Register ISIF_LINCFG0

ISS ISP

- ISS ISP ISIF Sensor Linearization: [0] [1] [2] [3]
- ISS ISP ISIF Register Setup: [4] [5] [6]
- ISS ISIF Register Summary: [7]

Table 8-1048. ISIF_LINCFG1

Address Offset	0x0000 0048		
Physical Address	0x5201 1048	**Instance**	ISS_ISIF
Description	INPUT LINEARIZATION CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								LUTSCL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:0	LUTSCL	Scale factor (U11Q10) for LUT input. Range: 0 - 1+1023/1024 It is applied to the Input Data before looking up the correction factor. The scale factor is only applied to the table input. It is not applied when using the input value to compute the output.	RW	0x400

Table 8-1049. Register Call Summary for Register ISIF_LINCFG1

ISS ISP

- ISS ISP ISIF Sensor Linearization: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1050. ISIF_CCOLP

Address Offset	0x0000 004C		
Physical Address	0x5201 104C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CP0_F1		CP1_F1		CP2_F1		CP3_F1		CP0_F0		CP1_F0		CP2_F0		CP3_F0	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	CP0_F1	Specifies color pattern for pixel position 0 (Field 1) Pixel position 0 corresponds to pixel count=0 at even line in case of CFAP= 0, and to pixel count=0 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0

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Bits	Field Name	Description	Type	Reset
13:12	CP1_F1	Specifies color pattern for pixel position 1 (Field 1) Pixel position 1 corresponds to pixel count=1 at even line in case of CFAP= 0, and to pixel count=1 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
11:10	CP2_F1	Specifies color pattern for pixel position 2 (Field 1) Pixel position 2 corresponds to pixel count=0 at odd line in case of CFAP= 0, and to pixel count=2 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
9:8	CP3_F1	Specifies color pattern for pixel position 3 (Field 1) Pixel position 3 corresponds to pixel count=1 at odd line in case of CFAP= 0. Not applicable for CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
7:6	CP0_F0	Specifies color pattern for pixel position 0 (Field 0) Pixel position 0 corresponds to pixel count=0 at even line in case of CFAP= 0, and to pixel count=0 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
5:4	CP1_F0	Specifies color pattern for pixel position 1 (Field 0) Pixel position 1 corresponds to pixel count=1 at even line in case of CFAP= 0, and to pixel count=1 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
3:2	CP2_F0	Specifies color pattern for pixel position 2 (Field 0) Pixel position 2 corresponds to pixel count=0 at odd line in case of CFAP= 0, and to pixel count=2 in case of CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0
1:0	CP3_F0	Specifies color pattern for pixel position 3 (Field 0) Pixel position 3 corresponds to pixel count=1 at odd line in case of CFAP= 0. Not applicable for CFAP= 1. 0x0: R / Ye 0x1: Gr / Cy 0x3: B / Mg 0x2: Gb / G	RW	0x0

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Table 8-1051. Register Call Summary for Register ISIF_CCOLP

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Register Setup: [1] [2] [3] [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1052. ISIF_CRGAIN

Address Offset	0x0000 0050		
Physical Address	0x5201 1050	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CGR											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CGR	R/Ye gain: Performs gain adjustment on image sensor data. U12Q9. Range: 0 - 7+511/512	RW	0x200

Table 8-1053. Register Call Summary for Register ISIF_CRGAIN

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-1054. ISIF_CGRGAIN

Address Offset	0x0000 0054		
Physical Address	0x5201 1054	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CGGR											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CGGR	Gr/Cy gain: Performs gain adjustment on image sensor data. U12Q9. Range: 0 - 7+511/512	RW	0x200

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Table 8-1055. Register Call Summary for Register ISIF_CGRGAIN

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-1056. ISIF_CGBGAIN

Address Offset	0x0000 0058		
Physical Address	0x5201 1058	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CGGB											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CGGB	Gb/Cy gain: Performs gain adjustment on image sensor data. U12Q9. Range: 0 - 7+511/512	RW	0x200

Table 8-1057. Register Call Summary for Register ISIF_CGBGAIN

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-1058. ISIF_CBGAIN

Address Offset	0x0000 005C		
Physical Address	0x5201 105C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CGB											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CGB	B/Mg gain: Performs gain adjustment on image sensor data. U12Q9. Range: 0 - 7+511/512	RW	0x200

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Table 8-1059. Register Call Summary for Register ISIF_CBGAIN

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-1060. ISIF_COFSTA

Address Offset	0x0000 0060		
Physical Address	0x5201 1060	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				COFT											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	COFT	Image sensor offset: Performs offset value adjustment on image sensor data (0~4095).	RW	0x000

Table 8-1061. Register Call Summary for Register ISIF_COFSTA

ISS ISP

- ISS ISP ISIF White Balance: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

Table 8-1062. ISIF_VDINT0

Address Offset	0x0000 0070		
Physical Address	0x5201 1070	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	CVD0														

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:0	CVD0	VD0 Interrupt timing in a field (line number).	RW	0x0000

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Table 8-1063. Register Call Summary for Register ISIF_VDINT0

ISS ISP
- ISS ISP ISIF VDINT0, VDINT1, and VDINT2 Interrupts: [0]
- ISS ISIF Register Summary: [1]

Table 8-1064. ISIF_VDINT1

Address Offset	0x0000 0074		
Physical Address	0x5201 1074	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CVD1							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:0	CVD1	VD1 Interrupt timing in a field (line number).	RW	0x0000

Table 8-1065. Register Call Summary for Register ISIF_VDINT1

ISS ISP
- ISS ISP ISIF VDINT0, VDINT1, and VDINT2 Interrupts: [0]
- ISS ISIF Register Summary: [1]

Table 8-1066. ISIF_VDINT2

Address Offset	0x0000 0078		
Physical Address	0x5201 1078	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CVD2							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:0	CVD2	VD2 Interrupt timing in a field (line number).	RW	0x0000

Table 8-1067. Register Call Summary for Register ISIF_VDINT2

ISS ISP
- ISS ISP ISIF VDINT0, VDINT1, and VDINT2 Interrupts: [0]
- ISS ISIF Register Summary: [1]

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Table 8-1068. ISIF_MISC

Address Offset	0x0000 007C		
Physical Address	0x5201 107C	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		DPCMPRE	DPCMEN	RESERVED											RESERVED

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13	DPCMPRE	Selects Predictor for DPCM Encoder (12-8) 0x0: Predictor 1 0x1: Predictor 2	RW	0
12	DPCMEN	Enables DPCM Encoding (12-8) 0x0: Disable 0x1: Enable	RW	0
11:1	RESERVED		R	0x000
0	RESERVED		RW	0

Table 8-1069. Register Call Summary for Register ISIF_MISC

ISS ISP

- ISS ISP ISIF 12-to-8-Bit DCPM Compression Block: [0] [1]
- ISS ISP ISIF Register Setup: [2] [3]
- ISS ISP ISIF Register Accessibility During Frame Processing: [4]
- ISS ISIF Register Summary: [5]

Table 8-1070. ISIF_CGAMMAWD

Address Offset	0x0000 0080		
Physical Address	0x5201 1080	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	WBEN2	WBEN1	WBEN0	RESERVED	OFSTEN2	OFSTEN1	OFSTEN0	RESERVED		CFAP	GWDI				CCDTBL

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14	WBEN2	White Balance Enable for H3A 0x0: Disable 0x1: Enable	RW	0

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Bits	Field Name	Description	Type	Reset
13	WBEN1	White Balance Enable for IPIPE 0x0: Disable 0x1: Enable	RW	0
12	WBEN0	White Balance Enable for memory capture 0x0: Disable 0x1: Enable	RW	0
11	RESERVED		R	0
10	OFSTEN2	Offset control Enable for H3A 0x0: Disable 0x1: Enable	RW	0
9	OFSTEN1	Offset control Enable for IPIPE 0x0: Disable 0x1: Enable	RW	0
8	OFSTEN0	Offset control Enable for SDRAM capture 0x0: Disable 0x1: Enable	RW	0
7:6	RESERVED		R	0x0
5	CFAP	Selects CFA pattern 0x0: Mosaic color pattern. It should look like this. G R G R G R G R G R . . . B G B G B G B G B G . . . G R G R G R G R G R . . . . 0x1: Stripe color pattern. It should look like this. R G B R G B R G B . . . R G B R G B R G B . . . R G B R G B R G B	RW	0
4:1	GWDI	Selects MSB position of Input Data 0x6: bit 9 0x1: bit 14 0xA: Reserved 0x7: bit 8 0xD: Reserved 0x0: bit 15 0x2: bit 13 0x8: bit 7 0x9: Reserved 0xB: Reserved 0x4: bit 11 0x5: bit 10 0xF: Reserved 0xC: Reserved 0x3: bit 12 0xE: Reserved	RW	0x0
0	CCDTBL	On/Off control of A-law table for SDRAM capture 0x0: Disable 0x1: Enable	RW	0

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Table 8-1071. Register Call Summary for Register ISIF_CGAMMAWD

ISS ISP

- ISS ISP ISIF Interface: [0] [1]
- ISS ISP ISIF White Balance: [2] [3] [4] [5] [6] [7] [8]
- ISS ISP ISIF A-Law Compression: [9] [10] [11]
- ISS ISP ISIF Register Setup: [12] [13] [14] [15] [16] [17] [18] [19] [20]
- ISS ISP ISIF Register Accessibility During Frame Processing: [21]
- ISS ISIF Register Summary: [22]

Table 8-1072. ISIF_REC656IF

Address Offset	0x0000 0084		
Physical Address	0x5201 1084	**Instance**	ISS_ISIF
Description	INPUT CONFIG REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														R656ON	ECCFVH

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	R656ON	CCIR Rec.656 interface mode 0x0: Disable 0x1: Enable	RW	0
0	ECCFVH	Error correction of FVH code 0x0: Disable 0x1: Enable	RW	0

Table 8-1073. Register Call Summary for Register ISIF_REC656IF

ISS ISP

- ISS ISP ISIF Register Setup: [0] [1]
- ISS ISIF Register Summary: [2]
- ISS ISIF Register Description: [3]

Table 8-1074. ISIF_CCDCFG

Address Offset	0x0000 0088		
Physical Address	0x5201 1088	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VLDC	RESERVED	MSBINVI	BSWD	Y8POS	EXTRG	TRGSEL	WENLOG	FIDMD		BT656	YCINSWP	RESERVED	RESERVED	SDRPACK	

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	VLDC	On/off control of CPU registers resynchronize function by VSYNC. All the others are shadowed registers, where register values are updated at V-sync timing by default. If VDLC=1, ISIF register values are updated immediately after register write just like non-shadowed registers. 0x0: Enable 0x1: Disable	RW	0
14	RESERVED	Reserved. must always be set to 0.	RW	0
13	MSBINVI	MSB inverse of CIN port when the data are captured to SDRAM. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x0: Disable 0x1: Enable	RW	0
12	BSWD	On/off control of Byte SWAP function when SDRAM capturing. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x0: Disable 0x1: Enable (swap)	RW	0
11	Y8POS	Selects Y signal position when in 8bit input mode 0x0: even pixel 0x1: odd pixel	RW	0
10	EXTRG	Setting 1 to this register, the SDRAM address is initialized at the rising edge of FID input signal or DWEN register.	RW	0
9	TRGSEL	Select trigger source signal of SDRAM address initializing in case EXTRG=1. 0x0: DWEN register 0x1: FID input port	RW	0
8	WENLOG	Specifies the CCD valid area. 0x0: internal valid signal and WEN signal is ANDed logically. 0x1: internal valid signal and WEN signal is ORed logically.	RW	0
7:6	FIDMD	Specifies FID detection mode 0x0: latch the FID at the VSYNC timing 0x1: no latch the FID 0x3: Reserved 0x2: Reserved	RW	0x0
5	BT656	Selects bit width of CCIR656. This bit applies only if ISIF_REC656IF.R656ON = 1. 0x0: 8 bits 0x1: 10 bits	RW	0

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Bits	Field Name	Description	Type	Reset
4	YCINSWP	The ISIF module has a 16-bit interface. When 16-bit YUV data are input, the luma data (YIN7-0) are expected to be on the 8 MS bits and the chroma (CIN7-0) data are expected to be on the LS bits. This bit enables to swap the 8 MS bits with the 8 LS bits of the interface in case the luma and chroma do not come in the correct order. See Section 8.3.3.6.2, *ISS ISP ISIF Top-Level Block Diagram*. 0x0: YIN7-0 = Y signal / CIN7-0 = C signal 0x1: YIN7-0 = C signal / CIN7-0 = Y signal	RW	0
3	RESERVED	Reserved. must always be set to 0.	RW	0
2	RESERVED	Reserved. must always be set to 0.	RW	0
1:0	SDRPACK	This bit field selects how the data are stored to SDRAM. There can be 8, 12 or 16 bits per pixel. The ISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCDCFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x0: 16 bits / pixel 0x1: 12 bits / pixel 0x3: Reserved 0x2: 8 bits / pixel	RW	0x0

Table 8-1075. Register Call Summary for Register ISIF_CCDCFG

ISS ISP

- ISS ISP ISIF Interface: [0] [1] [2]
- ISS ISP ISIF Write Port: [3]
- ISS ISP ISIF Register Setup: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- ISS ISP ISIF Register Accessibility During Frame Processing: [14] [15]
- ISS ISP ISIF Summary of Constraints: [16]
- ISS ISIF Register Summary: [17]
- ISS ISIF Register Description: [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32]

Table 8-1076. ISIF_DFCCTL

Address Offset	0x0000 008C		
Physical Address	0x5201 108C	**Instance**	ISS_ISIF
Description	VERTICAL LINE DEFCT CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED					VDFLSFT			VDFCUDA	VDFCSL		VDFCEN	RESERVED			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:11	RESERVED		R	0x00
10:8	VDFLSFT	Vertical line Defect level shift value Defect Level (value to be subtracted from the data) is 8bit width, but can be up-shifted up to 6bits by VDFLSFT. Left shift value = VDFLSFT (Range: 0-6) Setting 7 to VDFLSFT is not allowed.	RW	0x0

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Bits	Field Name	Description	Type	Reset
7	VDFCUDA	Vertical line Defect Correction upper pixels disable. 0x0: The whole line is corrected. 0x1: Pixels upper than the defect are not corrected.	RW	0
6:5	VDFCSL	Vertical line Defect Correction mode select. 0x0: Defect level subtraction. Just fed through if data are saturating. 0x1: Defect level subtraction. Horizontal interpolation ((i-2)+(i+2))/2 if data are saturating. 0x3: Reserved 0x2: Horizontal interpolation ((i-2)+(i+2))/2.	RW	0x0
4	VDFCEN	Vertical line Defect Correction enable. This bit field is latched by VD. 0x0: Disable 0x1: Enable	RW	0
3:0	RESERVED		R	0x0

Table 8-1077. Register Call Summary for Register ISIF_DFCCTL

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0] [1] [2] [3] [4] [5] [6] [7] [8]
- ISS ISP ISIF Vertical Line Defect Table Update Procedure: [9] [10]
- ISS ISP ISIF Register Setup: [11] [12] [13] [14] [15]
- ISS ISP ISIF Register Accessibility During Frame Processing: [16]
- ISS ISIF Register Summary: [17]

Table 8-1078. ISIF_VDFSATLV

Address Offset	0x0000 0090		
Physical Address	0x5201 1090	**Instance**	ISS_ISIF
Description	VERTICAL LINE DEFCT CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				VDFSLV											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	VDFSLV	Vertical line Defect Correction saturation level. VDFSLV is U12 (Range: 0 - 4,095).	RW	0x000

Table 8-1079. Register Call Summary for Register ISIF_VDFSATLV

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISP ISIF Register Accessibility During Frame Processing: [2]
- ISS ISIF Register Summary: [3]

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Table 8-1080. ISIF_DFCMEMCTL

Address Offset	0x0000 0094		
Physical Address	0x5201 1094	**Instance**	ISS_ISIF
Description	VERTICAL LINE DEFCT CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED											DFCMCLR	RESERVED	DFCMARST	DFCMRD	DFCMWR

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:5	RESERVED		R	0x000
4	DFCMCLR	Defect correction. Memory clear. Writing 1 to this bit clears the memory contents to all zero. It will be automatically cleared to 0 when the memory clear is completed.	RW	0
3	RESERVED		R	0
2	DFCMARST	Defect correction. Memory address reset. Setting DFCMWR or DFCMRD with LSCMARST set starts memory access to address offset 0. DFCMARST is automatically cleared if data transfer completes. Setting DFCMWR or DFCMRD with LSCMARST cleared starts memory access to the next address. 0x0: Increment the memory address 0x1: Clear the memory address to offset 0	RW	0
1	DFCMRD	Defect correction. Memory read [for debug purpose] Writing 1 to this bit starts reading from the memory. It will be automatically cleared when the data transfer is completed, and the data can be read from DFCMEM4-0.	RW	0
0	DFCMWR	Defect correction. Memory write Writing 1 to this bit starts writing to the memory. It will be automatically cleared when the data transfer is completed. DFCMEM4-0 should be set prior to the memory access.	RW	0

Table 8-1081. Register Call Summary for Register ISIF_DFCMEMCTL

ISS ISP

- ISS ISP ISIF Vertical Line Defect Table Update Procedure: [0] [1] [2] [3] [4] [5] [6] [7]
- ISS ISP ISIF Register Setup: [8] [9] [10]
- ISS ISIF Register Summary: [11]

Table 8-1082. ISIF_DFCMEM0

Address Offset	0x0000 0098		
Physical Address	0x5201 1098	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			DFCMEM0												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	DFCMEM0	Defect correction memory 0 Sets V position of the defects.	RW	0x0000

Table 8-1083. Register Call Summary for Register ISIF_DFCMEM0

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0]
- ISS ISP ISIF Vertical Line Defect Table Update Procedure: [1] [2] [3]
- ISS ISP ISIF Register Setup: [4]
- ISS ISIF Register Summary: [5]

Table 8-1084. ISIF_DFCMEM1

Address Offset	0x0000 009C		
Physical Address	0x5201 109C	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			DFCMEM1												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	DFCMEM1	Defect correction memory 1 Sets H position of the defects.	RW	0x0000

Table 8-1085. Register Call Summary for Register ISIF_DFCMEM1

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0]
- ISS ISP ISIF Vertical Line Defect Table Update Procedure: [1] [2] [3]
- ISS ISP ISIF Register Setup: [4]
- ISS ISIF Register Summary: [5]

Table 8-1086. ISIF_DFCMEM2

Address Offset	0x0000 00A0		
Physical Address	0x5201 10A0	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								DFCMEM2							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	DFCMEM2	Defect correction Memory 2 Set SUB1: Defect level of the Vertical line defect position (V = Vdefect). DFCMEM2 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.	RW	0x00

Table 8-1087. Register Call Summary for Register ISIF_DFCMEM2

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0]
- ISS ISP ISIF Vertical Line Defect Table Update Procedure: [1] [2]
- ISS ISP ISIF Register Setup: [3]
- ISS ISIF Register Summary: [4]

Table 8-1088. ISIF_DFCMEM3

Address Offset	0x0000 00A4		
Physical Address	0x5201 10A4	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								DFCMEM3							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	DFCMEM3	<Defect correction> Memory 3 Set SUB2: Defect level of the pixels upper than the Vertical line defect (V < Vdefect). DFCMEM3 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.	RW	0x00

Table 8-1089. Register Call Summary for Register ISIF_DFCMEM3

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0]
- ISS ISP ISIF Vertical Line Defect Table Update Procedure: [1] [2]
- ISS ISP ISIF Register Setup: [3]
- ISS ISIF Register Summary: [4]

Table 8-1090. ISIF_DFCMEM4

Address Offset	0x0000 00A8		
Physical Address	0x5201 10A8	**Instance**	ISS_ISIF
Description	Defect correction memory		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								DFCMEM4							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	RESERVED		R	0x00
7:0	DFCMEM4	Memory 4 Set SUB3: Defect level of the pixels lower than the Vertical line defect (V > Vdefect). DFCMEM4 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.	RW	0x00

Table 8-1091. Register Call Summary for Register ISIF_DFCMEM4

ISS ISP

- ISS ISP ISIF Vertical Line Defect Correction (VDFC): [0]
- ISS ISP ISIF Vertical Line Defect Table Update Procedure: [1] [2]
- ISS ISP ISIF Register Setup: [3]
- ISS ISIF Register Summary: [4]

Table 8-1092. ISIF_CLAMPCFG

Address Offset	0x0000 00AC		
Physical Address	0x5201 10AC	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED											CLMD	RESERVED		CLHMD		CLEN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:5	RESERVED		R	0x000
4	CLMD	Black clamp mode Clamp value can be calculated regardless of the color or can be calculated separately for each 4 colors. 0x0: Clamp value calculated regardless of the pixel color. 0x1: Clamp value calculated separately for each 4 colors.	RW	0
3	RESERVED		R	0
2:1	CLHMD	Horizontal Clamp mode 0x0: Horizontal clamp disabled. Only the Vertical clamp value is subtracted from the Image data. 0x1: Horizontal clamp value calculation enabled. The calculated Horizontal clamp value is subtracted from the Image data along with the Vertical clamp value. 0x3: Reserved 0x2: Horizontal clamp value not updated. The Horizontal clamp value used for the previous image is subtracted from the Image data along with the Vertical clamp value.	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	CLEN	Black Clamp Enable Enables clamp value to be subtracted from Image data. 0x0: Disable 0x1: Enable	RW	0

Table 8-1093. Register Call Summary for Register ISIF_CLAMPCFG

ISS ISP

- ISS ISP ISIF Black Clamp: [0] [1]
- ISS ISP ISIF Clamp Value for Horizontal Direction: [2] [3] [4]
- ISS ISP ISIF Register Setup: [5] [6]
- ISS ISP ISIF Register Accessibility During Frame Processing: [7]
- ISS ISIF Register Summary: [8]
- ISS ISIF Register Description: [9] [10]

Table 8-1094. ISIF_CLDCOFST

Address Offset	0x0000 00B0		
Physical Address	0x5201 10B0	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CLDC							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLDC	DC offset for black clamp This value is added to the incoming pixels regardless whether optical black clamp is enabled (ISIF_CLAMPCFG.CLEN). This value is in S13Q0 format.	RW	0x0000

Table 8-1095. Register Call Summary for Register ISIF_CLDCOFST

ISS ISP

- ISS ISP ISIF Black Clamp: [0]
- ISS ISP ISIF Register Setup: [1] [2]
- ISS ISIF Register Summary: [3]

Table 8-1096. ISIF_CLSV

Address Offset	0x0000 00B4		
Physical Address	0x5201 10B4	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CLSV							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLSV	Black Clamp Start position (V). Sets the line number where clamp value subtraction starts. Range: 0 - 8191	RW	0x0000

Table 8-1097. Register Call Summary for Register ISIF_CLSV

ISS ISP

- ISS ISP ISIF Register Setup: [0]
- ISS ISIF Register Summary: [1]

Table 8-1098. ISIF_CLHWIN0

Address Offset	0x0000 00B8		
Physical Address	0x5201 10B8	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		CLHWN		RESERVED		CLHWM		RESERVED		CLHLMT		CLHWBS		CLHWC	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:12	CLHWN	Horizontal Black clamp - Vertical dimension of a Window (2^N). 0x0: Window is 2 pixels tall (N=1) 0x1: Window is 4 pixels tall (N=2) 0x3: Window is 16 pixels tall (N=4) 0x2: Window is 8 pixels tall (N=3)	RW	0x0
11:10	RESERVED		R	0x0
9:8	CLHWM	Horizontal Black clamp - Horizontal dimension of a Window (2^M). 0x0: Window is 32 pixels wide (M=5) 0x1: Window is 64 pixels wide (M=6) 0x3: Window is 256 pixels wide (M=8) 0x2: Window is 128 pixels wide (M=7)	RW	0x0
7	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
6	CLHLMT	Horizontal Black clamp - Pixel value limitation for the Horizontal clamp value calculation. If this bit is set, the maximum pixel value to be used for the clamp value calculation would be limited to 1023. By setting this bit, the pixel value greater than 1023 will be replaced by the last pixel value which was equal to or less than 1023. In case ISIF_CLAMPCFG.CLMD=1 (4-color mode), the pixel value greater than 1023 will be replaced by the last pixel value of the same color which was equal to or less than 1023. 0x0: Limitation disabled 0x1: Limitation enabled	RW	0
5	CLHWBS	Horizontal Black clamp - Base Window select 0x0: The most left window 0x1: The most right window	RW	0
4:0	CLHWC	Horizontal Black clamp - Window count per color Window count = CLHWC+1 Range: 1 - 32	RW	0x00

Table 8-1099. Register Call Summary for Register ISIF_CLHWIN0

ISS ISP
- ISS ISP ISIF Clamp Value for Horizontal Direction: [0] [1] [2] [3] [4] [5]
- ISS ISP ISIF Clamp Value for Vertical Direction: [6]
- ISS ISP ISIF Register Setup: [7] [8] [9] [10] [11]
- ISS ISIF Register Summary: [12]

Table 8-1100. ISIF_CLHWIN1

Address Offset	0x0000 00BC		
Physical Address	0x5201 10BC	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			CLHSH												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLHSH	Horizontal black clamp. Window Start position (H). Range: 0 - 8191	RW	0x0000

Table 8-1101. Register Call Summary for Register ISIF_CLHWIN1

ISS ISP
- ISS ISP ISIF Clamp Value for Horizontal Direction: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

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Table 8-1102. ISIF_CLHWIN2

Address Offset	0x0000 00C0		
Physical Address	0x5201 10C0	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CLHSV							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLHSV	Horizontal black clamp. Window Start position (V). Range: 0 - 8191	RW	0x0000

Table 8-1103. Register Call Summary for Register ISIF_CLHWIN2

ISS ISP

- ISS ISP ISIF Clamp Value for Horizontal Direction: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1104. ISIF_CLVRV

Address Offset	0x0000 00C4		
Physical Address	0x5201 10C4	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED				CLVRV											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	RESERVED		R	0x0
11:0	CLVRV	Vertical black clamp reset value. (U12) Range: 0 to 4095	RW	0x000

Table 8-1105. Register Call Summary for Register ISIF_CLVRV

ISS ISP

- ISS ISP ISIF Clamp Value for Vertical Direction: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

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Table 8-1106. ISIF_CLVWIN0

Address Offset	0x0000 00C8		
Physical Address	0x5201 10C8	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLVCOEF								RESERVED		CLVRVSL		RESERVED		CLVOBH	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CLVCOEF	Vertical Black clamp - Line average coefficient (k). Set a coefficient which is applied to the line average for clamp value calculation. (1-k) is applied to the clamp value of the previous line. Value in the U8Q8 format, the range is 0 to 255/256.	RW	0x00
7:6	RESERVED		R	0x0
5:4	CLVRVSL	Vertical Black clamp - reset value selection Select the reset value for the clamp value of the previous line 0x0: The base value calculated for Horizontal direction 0x1: Value set via the configuration register 0x3: Reserved 0x2: No update (same as the previous image)	RW	0x0
3	RESERVED		R	0
2:0	CLVOBH	Vertical Black clamp - Optical Black H valid (2^L). 0x6: Reserved 0x1: 4 pixels wide (L=2) 0x7: Reserved 0x0: 2 pixels wide (L=1) 0x2: 8 pixels wide (L=3) 0x4: 32 pixels wide (L=5) 0x5: 64 pixels wide (L=6) 0x3: 16 pixels wide (L=4)	RW	0x0

Table 8-1107. Register Call Summary for Register ISIF_CLVWIN0

ISS ISP

- ISS ISP ISIF Clamp Value for Vertical Direction: [0] [1] [2] [3] [4]
- ISS ISP ISIF Register Setup: [5] [6] [7]
- ISS ISIF Register Summary: [8]

Table 8-1108. ISIF_CLVWIN1

Address Offset	0x0000 00CC		
Physical Address	0x5201 10CC	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			CLVSH												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLVSH	Vertical black clamp. Window Start position (H). Range: 0 - 8191	RW	0x0000

Table 8-1109. Register Call Summary for Register ISIF_CLVWIN1

ISS ISP

- ISS ISP ISIF Clamp Value for Vertical Direction: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1110. ISIF_CLVWIN2

Address Offset	0x0000 00D0		
Physical Address	0x5201 10D0	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			CLVSV												

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLVSV	Vertical black clamp. Window Start position (V). Range: 0 - 8191	RW	0x0000

Table 8-1111. Register Call Summary for Register ISIF_CLVWIN2

ISS ISP

- ISS ISP ISIF Clamp Value for Vertical Direction: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1112. ISIF_CLVWIN3

Address Offset	0x0000 00D4		
Physical Address	0x5201 10D4	**Instance**	ISS_ISIF
Description	BLACK CLAMP CTRL REGISTER		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								CLVOBV							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	CLVOBV	Vertical black clamp. Optical black V valid (V). Range: 0 - 8191	RW	0x0000

Table 8-1113. Register Call Summary for Register ISIF_CLVWIN3

ISS ISP

- ISS ISP ISIF Clamp Value for Vertical Direction: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1114. ISIF_LSCHOFST

Address Offset	0x0000 00D8		
Physical Address	0x5201 10D8	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		HOFST													

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:0	HOFST	H direction Data offset for Lens Shading Correction. Range: 0-16,383 Not valid if the Formatter is enabled.	RW	0x0000

Table 8-1115. Register Call Summary for Register ISIF_LSCHOFST

ISS ISP

- ISS ISP ISIF Register Setup: [0]
- ISS ISP ISIF Register Accessibility During Frame Processing: [1]
- ISS ISIF Register Summary: [2]

Table 8-1116. ISIF_LSCVOFST

Address Offset	0x0000 00DC		
Physical Address	0x5201 10DC	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		VOFST													

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:0	VOFST	V direction Data offset for Lens Shading Correction. Range: 0-16,383	RW	0x0000

Table 8-1117. Register Call Summary for Register ISIF_LSCVOFST

ISS ISP

- ISS ISP ISIF Register Setup: [0]
- ISS ISP ISIF Register Accessibility During Frame Processing: [1]
- ISS ISIF Register Summary: [2]

Table 8-1118. ISIF_LSCHVAL

Address Offset	0x0000 00E0		
Physical Address	0x5201 10E0	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		HVAL													

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:0	HVAL	Number of valid pixels in H direction. HVAL is for LSC. Number of valid pixels = HVAL+ 1	RW	0x0000

Table 8-1119. Register Call Summary for Register ISIF_LSCHVAL

ISS ISP

- ISS ISP ISIF Register Setup: [0]
- ISS ISIF Register Summary: [1]

Table 8-1120. ISIF_LSCVVAL

Address Offset	0x0000 00E4		
Physical Address	0x5201 10E4	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								VVAL							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	RESERVED		R	0x0
13:0	VVAL	Number of valid lines in V direction. VVAL is for LSC. Number of valid lines = VVAL+ 1	RW	0x0000

Table 8-1121. Register Call Summary for Register ISIF_LSCVVAL

ISS ISP

- ISS ISP ISIF Register Setup: [0]
- ISS ISIF Register Summary: [1]

Table 8-1122. ISIF_2DLSCCFG

Address Offset	0x0000 00E8		
Physical Address	0x5201 10E8	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		GAIN_MODE_M		RESERVED		GAIN_MODE_N		BUSY	GAIN_RANGE	RESERVED		GAIN_FORMAT			ENABLE

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:12	GAIN_MODE_M	Define the horizontal dimension of a paxel. Possible values are listed below. 0x6: Paxel is 64 pixels tall (M=64) 0x1: Reserved 0x7: Paxel is 128 pixels tall (M=128) 0x0: Reserved 0x2: Reserved 0x4: Paxel is 16 pixels tall (M=16) 0x5: Paxel is 32 pixels tall (M=32) 0x3: Paxel is 8 pixels tall (M=8)	RW	0x6
11	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
10:8	GAIN_MODE_N	Define the vertical dimension of a paxel. Possible values are listed below. 0x6: Paxel is 64 pixels tall (N=64) 0x1: Reserved 0x7: Paxel is 128 pixels tall (N=128) 0x0: Reserved 0x2: Reserved 0x4: Paxel is 16 pixels tall (N=16) 0x5: Paxel is 32 pixels tall (N=32) 0x3: Paxel is 8 pixels tall (N=8)	RW	0x6
7	BUSY	Busy bit Read 0x1: Busy Read 0x0: Idle	R	0
6	GAIN_RANGE	Define the range of gain table values. 0: 8-bit gain mode, GAIN table represents unsigned 8bit values 1: 16-bit gain mode. GAIN table is combined with OFST table to constitute 16 bit gain values. GAIN table represents MSB 8 bits, and OFST table represents LSB 8 bits. In 16-bit, offset table is loaded from memory. Offset control function is disabled. (The ISIF_2DLSCOFST[0] OFSTEN bit is treated as zero in this mode).	RW	0
5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4:1	GAIN_FORMAT	Sets gain table format 0x6: In 8-bit mode, Coded as 3-bit integer, 5-bit fraction, Range from 0 to 7+31/32 In 16-bit mode, Coded as 3-bit integer, 13-bit fraction, Range from 0 to 7+8191/8192 0x1: In 8-bit mode, Coded as 8-bit fraction + 1.0 of base, Range from 1 to 1+255/256 in 16-bit mode, Coded as 16-bit fraction + 1.0 of base, Range from 1 to 1+65535/65536 0xA: In 8-bit mode, Coded as 1-bit integer, 7-bit fraction, Range from 0 to 1+127/128 In 16-bit mode, Coded as 5-bit integer and 11-bit fraction Range from 0 to 31+2047/2048 0x7: In 8-bit mode, Coded as 3-bit integer, 5-bit fraction + 1.0, Range from 1 to 8+31/32 In 16-bit mode, Coded as 3-bit integer, 13-bit fraction + 1.0, Range from 1 to 8+8191/8192 0xD: In 8-bit mode, Coded as 2-bit integer, 6-bit fraction + 1.0, Range from 1 to 4+63/64 In 16-bit mode, Coded as 6-bit integer and 10-bit fraction Range from 1 to 64+1023/1024 0x0: In 8-bit mode, Coded as 8-bit fraction Range from 0 to 255/256 In 16-bit mode, Coded as 16-bit fraction Range from 0 to 65535/65536 0x2: In 8-bit mode, Coded as 1-bit integer, 7-bit fraction, Range from 0 to 1+127/128 In 16-bit mode, Coded as 1-bit integer, 15-bit fraction, Range from 0 to 1+32767/32768 0x8: In 8-bit mode, Coded as 8-bit fraction Range from 0 to 255/256 In 16-bit mode, Coded as 4-bit integer and 12-bit fraction Range from 0 to 15+4095/4096 0x9: In 8-bit mode, Coded as 8-bit fraction + 1.0 of base, Range from 1 to 1+255/256 In 16-bit mode, Coded as 4-bit integer and 12-bit fraction Range from 1 to 16+4095/4096 0xB: In 8-bit mode, Coded as 1-bit integer, 7-bit fraction + 1.0, Range from 1 to 2+127/128 In 16-bit mode, Coded as 5-bit integer and 11-bit fraction + 1.0, Range from 1 to 32+2047/2048 0x4: In 8-bit mode, Coded as 2-bit integer, 6-bit fraction, Range from 0 to 3+63/64 In 16-bit mode, Coded as 2-bit integer, 14-bit fraction, Range from 0 to 3+16383/16384 0x5: In 8-bit mode, Coded as 2-bit integer, 6-bit fraction + 1.0, Range from 1	RW	0x0

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Bits	Field Name	Description	Type	Reset
		to 4+63/64 In 16-bit mode, Coded as 2-bit integer, 14-bit fraction + 1.0, Range from 1 to 4+16383/16384 0xF: In 8-bit mode, Coded as 3-bit integer, 5-bit fraction + 1.0, Range from 1 to 8+31/32 In 16-bit mode, Coded as 7-bit integer and 9-bit fraction + 1.0, Range from 1 to 128+511/512 0xC: In 8-bit mode, Coded as 2-bit integer, 6-bit fraction, Range from 0 to 3+63/64 In 16-bit mode, Coded as 6-bit integer and 10-bit fraction Range from 0 to 63+1023/1024 0x3: In 8-bit mode, Coded as 1-bit integer, 7-bit fraction + 1.0, Range from 1 to 2+127/128 In 16-bit mode, Coded as 1-bit integer, 15-bit fraction + 1.0, Range from 1 to 2+32767/32768 0xE: In 8-bit mode, Coded as 3-bit integer, 5-bit fraction, Range from 0 to 7+31/32 In 16-bit mode, Coded as 7-bit integer and 9-bit fraction Range from 0 to 127+511/512		
0	ENABLE	Enables/disables LSC 0x0: Disables the module at the end of the current frame. 0x1: Enables the module.	RW	0

Table 8-1123. Register Call Summary for Register ISIF_2DLSCCFG

ISS ISP

- ISS ISP ISIF Lens Shading Correction Module (2D-LSC): [0] [1] [2]
- ISS ISP ISIF 2D-LSC Active Region Settings: [3] [4] [5] [6] [7] [8]
- ISS ISP ISIF Read Port: [9] [10] [11] [12] [13] [14] [15] [16]
- ISS ISP ISIF Register Setup: [17] [18] [19] [20] [21]
- ISS ISIF Register Summary: [22]
- ISS ISIF Register Description: [23]

Table 8-1124. ISIF_2DLSCOFST

Address Offset	0x0000 00EC		
Physical Address	0x5201 10EC	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OFSTSF								RESERVED				OFSTSFT		RESERVED			OFSTEN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	OFSTSF	Scaling factor for Offsets (U8Q7) Range: 0 to 1+127/128	RW	0x80

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Bits	Field Name	Description	Type	Reset
7	RESERVED		R	0
6:4	OFSTSFT	Shift up value for Offsets (S8Q0) 0x6: Reserved 0x1: 1bit left shift 0x7: Reserved 0x0: No shift 0x2: 2bits left shift 0x4: 4bits left shift 0x5: 5bits left shift 0x3: 3bits left shift	RW	0x0
3:1	RESERVED		R	0x0
0	OFSTEN	Enables/disables Offset control in LSC This bit is ignored (treated as zero) in 16-bit gain mode (ISIF_2DLSCCFG[6] GAIN_RANGE = 1). In 16-bit, offset table is loaded from memory, and used as lower 8-bit of 16-bit gain table. 0x0: Disable 0x1: Enable	RW	0

Table 8-1125. Register Call Summary for Register ISIF_2DLSCOFST

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0] [1] [2] [3] [4]
- ISS ISP ISIF Read Port: [5]
- ISS ISP ISIF Register Setup: [6] [7] [8]
- ISS ISIF Register Summary: [9]
- ISS ISIF Register Description: [10]

Table 8-1126. ISIF_2DLSCINI

Address Offset	0x0000 00F0		
Physical Address	0x5201 10F0	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	Y							RESERVED	X						

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	RESERVED		R	0
14:8	Y	Initial Y Y position, in pixels, of the first active pixel in reference to the first active paxel. Must be an even number.	RW	0x00
7	RESERVED		R	0
6:0	X	Initial X X position, in pixels, of the first active pixel in reference to the first active paxel. Must be an even number.	RW	0x00

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Table 8-1127. Register Call Summary for Register ISIF_2DLSCINI

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0] [1]
- ISS ISP ISIF Register Setup: [2] [3]
- ISS ISP ISIF Summary of Constraints: [4]
- ISS ISIF Register Summary: [5]

Table 8-1128. ISIF_2DLSCGRBU

Address Offset	0x0000 00F4		
Physical Address	0x5201 10F4	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE31_16															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	BASE31_16	Gain Table address base (Upper 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.	RW	0x0000

Table 8-1129. Register Call Summary for Register ISIF_2DLSCGRBU

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1130. ISIF_2DLSCGRBL

Address Offset	0x0000 00F8		
Physical Address	0x5201 10F8	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE15_0															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	BASE15_0	Gain Table address base (Lower 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.	RW	0x0000

Table 8-1131. Register Call Summary for Register ISIF_2DLSCGRBL

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

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Table 8-1132. ISIF_2DLSCGROF

Address Offset	0x0000 00FC		
Physical Address	0x5201 10FC	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OFFSET															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	OFFSET	Gain Table offset Defines the length, in bytes, of one row of the table. Table is 32-bit aligned, so this value must be a multiple of 4. Note that the row in memory could be longer than what LSC uses.	RW	0x0000

Table 8-1133. Register Call Summary for Register ISIF_2DLSCGROF

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1134. ISIF_2DLSCORBU

Address Offset	0x0000 0100		
Physical Address	0x5201 1100	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	BASE	Offset Table address base (Upper 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.	RW	0x0000

Table 8-1135. Register Call Summary for Register ISIF_2DLSCORBU

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1136. ISIF_2DLSCORBL

Address Offset	0x0000 0104		
Physical Address	0x5201 1104	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	BASE	Offset Table address base (Lower 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.	RW	0x0000

Table 8-1137. Register Call Summary for Register ISIF_2DLSCORBL

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1138. ISIF_2DLSCOROF

Address Offset	0x0000 0108		
Physical Address	0x5201 1108	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OFFSET															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	OFFSET	Offset Table offset Defines the length, in bytes, of one row of the table. Table is 32-bit aligned, so this value must be a multiple of 4. Note that the row in memory could be longer than what LSC uses.	RW	0x0000

Table 8-1139. Register Call Summary for Register ISIF_2DLSCOROF

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1140. ISIF_2DLSCIRQEN

Address Offset	0x0000 010C		
Physical Address	0x5201 110C	**Instance**	ISS_ISIF
Description			
Type	RW		

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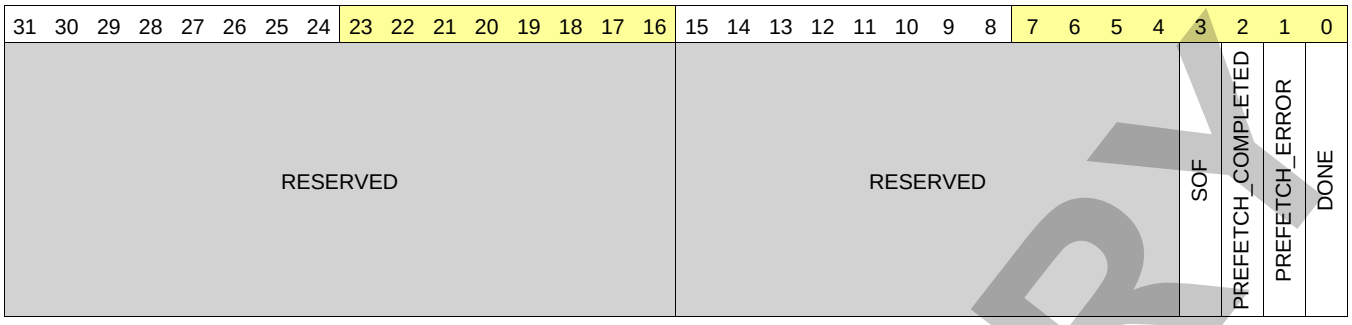

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3	SOF	Interrupt status for LSC SOF Indicates the start of the LSC valid region. LSC configuration registers can be updated after LSC SOF for the next frame. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
2	PREFETCH_COMPLETED	Interrupt enable for Prefetch Complete Indicates current state of the prefetch buffer. Could be used to start sending the data once the buffer is full to minimize the risk of an underflow. This event is triggered when the buffer contains 3 full paxel rows. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
1	PREFETCH_ERROR	Interrupt enable for Prefetch Error The prefetch error indicates when the gain table was read to slowly from SDRAM. When this event is pending the module goes into transparent mode (output=input). Normal operation can be resumed at the start of the next frame after clearing this event. Until the next pre-fetch completion, the image will be multiplied with previous gain values, and output image is not correct. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0
0	DONE	Interrupt enable for LSC Done The event is triggered when the internal state of LSC toggles from BUSY to IDLE. 0x0: Interrupt is masked 0x1: Interrupt is enabled	RW	0

Table 8-1141. Register Call Summary for Register ISIF_2DLSCIRQEN

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0]
- ISS ISP ISIF Register Setup: [1] [2] [3] [4]
- ISS ISIF Register Summary: [5]

Table 8-1142. ISIF_2DLSCIRQST

Address Offset	0x0000 0110		
Physical Address	0x5201 1110	**Instance**	ISS_ISIF
Description	2D Lens Shading Correction Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED												SOF	PREFETCH_COMPLETED	PREFETCH_ERROR	DONE

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:4	RESERVED		R	0x000
3	SOF	Interrupt status for LSC SOF Indicates the start of the LSC valid region. LSC configuration registers can be updated after LSC SOF for the next frame. 0x0: Event is not pending (r) Bit remains unchanged (w) 0x1: Event is pending (r) Event is cleared (w)	RW	0
2	PREFETCH_COMPLETED	Interrupt status for Prefetch Complete Indicates current state of the prefetch buffer. Could be used to start sending the data once the buffer is full to minimize the risk of an underflow. This event is triggered when the buffer contains 3 full paxel rows. It could be used to minimize buffer underflow risks. 0x0: Event is not pending (r) Bit remains unchanged (w) 0x1: Event is pending (r) Event is cleared (w)	RW	0
1	PREFETCH_ERROR	Interrupt status for Prefetch Error The prefetch error indicates when the gain table was read to slowly from SDRAM. When this event is pending the module goes into transparent mode (output=input). Normal operation can be resumed at the start of the next frame after clearing this event. Until the next pre-fetch completion, the image will be multiplied with previous gain values, and output image is not correct. 0x0: Event is not pending (r) Bit remains unchanged (w) 0x1: Event is pending (r) Event is cleared (w)	RW	0
0	DONE	Interrupt status for LSC Done The event is triggered when the internal state of LSC toggles from BUSY to IDLE. 0x0: Event is not pending (r) Bit remains unchanged (w) 0x1: Event is pending (r) Event is cleared (w)	RW	0

Table 8-1143. Register Call Summary for Register ISIF_2DLSCIRQST

ISS ISP

- ISS ISP ISIF 2D-LSC Active Region Settings: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- ISS ISIF Register Summary: [10]

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Table 8-1144. ISIF_FMTCFG

Address Offset	0x0000 0114		
Physical Address	0x5201 1114	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FMTAINC				RESERVED		LNUM		RESERVED		LNALT	FMTCBL	FMTEN

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:8	FMTAINC	Address increment Address increment = (FMTAINC + 1) Range (1-16) *This bit is latched by VD.	RW	0x0
7:6	RESERVED		R	0x0
5:4	LNUM	Split/Combine number of lines *This bit is latched by VD. 0x0: 1 output line 0x1: 1 input line -> 2 output lines (FMTCBL=0) 2 input lines -> 1 output line (FMTCBL=1) 0x3: 1 input line -> 4 output lines (FMTCBL=0) 4 input lines -> 1 output line (FMTCBL=1) 0x2: 1 input line -> 3 output lines (FMTCBL=0) 3 input lines -> 1 output line (FMTCBL=1)	RW	0x0
3	RESERVED		R	0
2	LNALT	Line alternating *This bit is latched by VD. 0x0: Normal mode 0x1: Line alternative mode	RW	0
1	FMTCBL	Combine Input lines *This bit is latched by VD. 0x0: Split 1 input line into multiple output lines 0x1: Combine multiple input lines into 1 output line	RW	0
0	FMTEN	CCD Formatter enable *This bit is latched by VD. 0x0: Disable 0x1: Enable	RW	0

Table 8-1145. Register Call Summary for Register ISIF_FMTCFG

ISS ISP

- ISS ISP ISIF Input Data Formatter: [0] [1] [2] [3] [4]
- ISS ISP ISIF Formatter Programming: [5] [6] [7] [8] [9] [10] [11] [12]
- ISS ISP ISIF Combine the Divided Input Lines: [13] [14] [15] [16] [17] [18] [19] [20]
- ISS ISP ISIF Register Setup: [21] [22] [23] [24] [25]
- ISS ISIF Register Summary: [26]

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Table 8-1146. ISIF_FMTPLEN

Address Offset	0x0000 0118		
Physical Address	0x5201 1118	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FMTPLEN3				RESERVED		FMTPLEN2		FMTPLEN1				FMTPLEN0			

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:12	FMTPLEN3	Number of program entries for SET3 Number of entries = (FMTPLEN3 + 1) Range: 1-8 Valid only if FMTCBL is set *This bit is latched by VD.	RW	0x0
11	RESERVED		R	0
10:8	FMTPLEN2	Number of program entries for SET2 Number of entries = (FMTPLEN2 + 1) Range: 1-8 Valid only if FMTCBL is set *This bit is latched by VD.	RW	0x0
7:4	FMTPLEN1	Number of program entries for SET1 Number of entries = (FMTPLEN1 + 1) Range: 1-16 (FMTCBL = 0) 1-8 (FMTCBL = 1) Setting a value greater than 7 to FMTPLEN1 is not allowed if FMTCBL is set *This bit is latched by VD.	RW	0x0
3:0	FMTPLEN0	Number of program entries for SET0 Number of entries = (PLEN0 + 1) Range: 1-16 (FMTCBL = 0) 1-8 (FMTCBL = 1) Setting a value greater than 7 to FMTPLEN1 is not allowed if FMTCBL is set *This bit is latched by VD.	RW	0x0

Table 8-1147. Register Call Summary for Register ISIF_FMTPLEN

ISS ISP

- ISS ISP ISIF Formatter Programming: [0] [1] [2] [3] [4]
- ISS ISP ISIF Combine the Divided Input Lines: [5] [6] [7]
- ISS ISP ISIF Register Setup: [8] [9] [10] [11]
- ISS ISIF Register Summary: [12]

Table 8-1148. ISIF_FMTSPH

Address Offset	0x0000 011C		
Physical Address	0x5201 111C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FMTSPH											

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTSPH	The first pixel in a line fed into the formatter	RW	0x0000

Table 8-1149. Register Call Summary for Register ISIF_FMTSPH

ISS ISP

- ISS ISP ISIF Formatter Area Settings: [0] [1]
- ISS ISP ISIF Combine the Divided Input Lines: [2]
- ISS ISP ISIF Color Space Converter: [3]
- ISS ISP ISIF Register Setup: [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1150. ISIF_FMTLNH

Address Offset	0x0000 0120		
Physical Address	0x5201 1120	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FMTLNH															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTLNH	Number of pixels in a line fed to the formatter. Number of pixels = FMTLNH + 1	RW	0x0000

Table 8-1151. Register Call Summary for Register ISIF_FMTLNH

ISS ISP

- ISS ISP ISIF Formatter Area Settings: [0] [1]
- ISS ISP ISIF Combine the Divided Input Lines: [2]
- ISS ISP ISIF Color Space Converter: [3]
- ISS ISP ISIF Register Setup: [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1152. ISIF_FMTLSV

Address Offset	0x0000 0124		
Physical Address	0x5201 1124	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FMTSLV															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTSLV	Start line vertical	RW	0x0000

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Table 8-1153. Register Call Summary for Register ISIF_FMTLSV

ISS ISP

- ISS ISP ISIF Formatter Area Settings: [0] [1]
- ISS ISP ISIF Combine the Divided Input Lines: [2]
- ISS ISP ISIF Color Space Converter: [3]
- ISS ISP ISIF Register Setup: [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1154. ISIF_FMTLNV

Address Offset	0x0000 0128		
Physical Address	0x5201 1128	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FMTLNV															

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:0	FMTLNV	Number of lines in vertical Number of lines = FMTLNV + 1	RW	0x0000

Table 8-1155. Register Call Summary for Register ISIF_FMTLNV

ISS ISP

- ISS ISP ISIF Formatter Area Settings: [0] [1]
- ISS ISP ISIF Combine the Divided Input Lines: [2]
- ISS ISP ISIF Color Space Converter: [3]
- ISS ISP ISIF Register Setup: [4]
- ISS ISP ISIF Register Accessibility During Frame Processing: [5]
- ISS ISIF Register Summary: [6]

Table 8-1156. ISIF_FMTRLEN

Address Offset	0x0000 012C		
Physical Address	0x5201 112C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FMTRLEN							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTRLEN	Number of pixels in an output line Maximum value = 4480	RW	0x0000

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Table 8-1157. Register Call Summary for Register ISIF_FMTRLEN

ISS ISP

- ISS ISP ISIF Formatter Area Settings: [0] [1]
- ISS ISP ISIF Combine the Divided Input Lines: [2]
- ISS ISP ISIF Register Setup: [3]
- ISS ISIF Register Summary: [4]

Table 8-1158. ISIF_FMTHCNT

Address Offset	0x0000 0130		
Physical Address	0x5201 1130	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FMTHCNT							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	FMTHCNT	HD interval for output lines Set all 0 to this register if combining multiple lines into a single line	RW	0x0000

Table 8-1159. Register Call Summary for Register ISIF_FMTHCNT

ISS ISP

- ISS ISP ISIF Formatter Area Settings: [0] [1] [2]
- ISS ISP ISIF Register Setup: [3]
- ISS ISIF Register Summary: [4]

Table 8-1160. ISIF_FMTAPTR0

Address Offset	0x0000 0134		
Physical Address	0x5201 1134	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 0 This address can not exceed FMTRLEN - 1	RW	0x0000

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Table 8-1161. Register Call Summary for Register ISIF_FMTAPTR0

ISS ISP

- ISS ISP ISIF Formatter Programming: [0]
- ISS ISP ISIF Combine the Divided Input Lines: [1]
- ISS ISIF Register Summary: [2]

Table 8-1162. ISIF_FMTAPTR1

Address Offset	0x0000 0138		
Physical Address	0x5201 1138	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 1 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1163. Register Call Summary for Register ISIF_FMTAPTR1

ISS ISP

- ISS ISP ISIF Combine the Divided Input Lines: [0]
- ISS ISIF Register Summary: [1]

Table 8-1164. ISIF_FMTAPTR2

Address Offset	0x0000 013C		
Physical Address	0x5201 113C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 2 This address can not exceed FMTRLEN - 1	RW	0x0000

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Table 8-1165. Register Call Summary for Register ISIF_FMTAPTR2

ISS ISP

- ISS ISP ISIF Combine the Divided Input Lines: [0]
- ISS ISIF Register Summary: [1]

Table 8-1166. ISIF_FMTAPTR3

Address Offset	0x0000 0140		
Physical Address	0x5201 1140	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 3 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1167. Register Call Summary for Register ISIF_FMTAPTR3

ISS ISP

- ISS ISP ISIF Combine the Divided Input Lines: [0]
- ISS ISIF Register Summary: [1]

Table 8-1168. ISIF_FMTAPTR4

Address Offset	0x0000 0144		
Physical Address	0x5201 1144	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 4 This address can not exceed FMTRLEN - 1	RW	0x0000

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Table 8-1169. Register Call Summary for Register ISIF_FMTAPTR4

ISS ISP

- ISS ISP ISIF Combine the Divided Input Lines: [0]
- ISS ISIF Register Summary: [1]

Table 8-1170. ISIF_FMTAPTR5

Address Offset	0x0000 0148		
Physical Address	0x5201 1148	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 5 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1171. Register Call Summary for Register ISIF_FMTAPTR5

ISS ISP

- ISS ISP ISIF Combine the Divided Input Lines: [0]
- ISS ISIF Register Summary: [1]

Table 8-1172. ISIF_FMTAPTR6

Address Offset	0x0000 014C		
Physical Address	0x5201 114C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 6 This address can not exceed FMTRLEN - 1	RW	0x0000

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Table 8-1173. Register Call Summary for Register ISIF_FMTAPTR6

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1174. ISIF_FMTAPTR7

Address Offset	0x0000 0150		
Physical Address	0x5201 1150	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 7 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1175. Register Call Summary for Register ISIF_FMTAPTR7

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1176. ISIF_FMTAPTR8

Address Offset	0x0000 0154		
Physical Address	0x5201 1154	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 8 This address can not exceed FMTRLEN - 1	RW	0x0000

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Table 8-1177. Register Call Summary for Register ISIF_FMTAPTR8

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1178. ISIF_FMTAPTR9

Address Offset	0x0000 0158		
Physical Address	0x5201 1158	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 9 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1179. Register Call Summary for Register ISIF_FMTAPTR9

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1180. ISIF_FMTAPTR10

Address Offset	0x0000 015C		
Physical Address	0x5201 115C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 10 This address can not exceed FMTRLEN - 1	RW	0x0000

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Table 8-1181. Register Call Summary for Register ISIF_FMTAPTR10

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1182. ISIF_FMTAPTR11

Address Offset	0x0000 0160		
Physical Address	0x5201 1160	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 11 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1183. Register Call Summary for Register ISIF_FMTAPTR11

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1184. ISIF_FMTAPTR12

Address Offset	0x0000 0164		
Physical Address	0x5201 1164	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 12 This address can not exceed FMTRLEN - 1	RW	0x0000

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Table 8-1185. Register Call Summary for Register ISIF_FMTAPTR12

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1186. ISIF_FMTAPTR13

Address Offset	0x0000 0168		
Physical Address	0x5201 1168	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 13 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1187. Register Call Summary for Register ISIF_FMTAPTR13

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1188. ISIF_FMTAPTR14

Address Offset	0x0000 016C		
Physical Address	0x5201 116C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 14 This address can not exceed FMTRLEN - 1	RW	0x0000

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Table 8-1189. Register Call Summary for Register ISIF_FMTAPTR14

ISS ISP

- ISS ISIF Register Summary: [0]

Table 8-1190. ISIF_FMTAPTR15

Address Offset	0x0000 0170		
Physical Address	0x5201 1170	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINE			INIT												

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14:13	LINE	The output line the address belongs to Valid only if FMTCBL is cleared 0x0: 1st line 0x1: 2nd line 0x3: 4th line 0x2: 3rd line	RW	0x0
12:0	INIT	Initial address value for address pointer 15 This address can not exceed FMTRLEN - 1	RW	0x0000

Table 8-1191. Register Call Summary for Register ISIF_FMTAPTR15

ISS ISP

- ISS ISP ISIF Formatter Programming: [0]
- ISS ISIF Register Summary: [1]

Table 8-1192. ISIF_FMTPGMVF0

Address Offset	0x0000 0174		
Physical Address	0x5201 1174	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM15EN	PGM14EN	PGM13EN	PGM12EN	PGM11EN	PGM10EN	PGM09EN	PGM08EN	PGM07EN	PGM06EN	PGM05EN	PGM04EN	PGM03EN	PGM02EN	PGM01EN	PGM00EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	PGM15EN	Program 15 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
14	PGM14EN	Program 14 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0

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Bits	Field Name	Description	Type	Reset
13	PGM13EN	Program 13 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
12	PGM12EN	Program 12 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
11	PGM11EN	Program 11 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
10	PGM10EN	Program 10 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
9	PGM09EN	Program 9 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
8	PGM08EN	Program 8 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
7	PGM07EN	Program 7 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
6	PGM06EN	Program 6 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
5	PGM05EN	Program 5 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
4	PGM04EN	Program 4 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
3	PGM03EN	Program 3 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
2	PGM02EN	Program 2 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
1	PGM01EN	Program 1 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
0	PGM00EN	Program 0 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0

Table 8-1193. Register Call Summary for Register ISIF_FMTPGMVF0

ISS ISP

- ISS ISP ISIF Formatter Programming: [0]
- ISS ISP ISIF Combine the Divided Input Lines: [1] [2] [3] [4]
- ISS ISP ISIF Register Setup: [5]
- ISS ISIF Register Summary: [6]

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Table 8-1194. ISIF_FMTPGMVF1

Address Offset	0x0000 0178		
Physical Address	0x5201 1178	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM31EN	PGM30EN	PGM29EN	PGM28EN	PGM27EN	PGM26EN	PGM25EN	PGM24EN	PGM23EN	PGM22EN	PGM21EN	PGM20EN	PGM19EN	PGM18EN	PGM17EN	PGM16EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	PGM31EN	Program 31 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
14	PGM30EN	Program 30 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
13	PGM29EN	Program 29 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
12	PGM28EN	Program 28 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
11	PGM27EN	Program 27 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
10	PGM26EN	Program 26 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
9	PGM25EN	Program 25 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
8	PGM24EN	Program 24 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
7	PGM23EN	Program 23 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
6	PGM22EN	Program 22 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
5	PGM21EN	Program 21 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
4	PGM20EN	Program 20 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0

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Bits	Field Name	Description	Type	Reset
3	PGM19EN	Program 19 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
2	PGM18EN	Program 18 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
1	PGM17EN	Program 17 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0
0	PGM16EN	Program 16 Valid Flag 0x0: Skip this pixel 0x1: This pixel is valid	RW	0

Table 8-1195. Register Call Summary for Register ISIF_FMTPGMVF1

ISS ISP

- ISS ISP ISIF Formatter Programming: [0]
- ISS ISP ISIF Combine the Divided Input Lines: [1] [2]
- ISS ISP ISIF Register Setup: [3]
- ISS ISIF Register Summary: [4]

Table 8-1196. ISIF_FMTPGMAPU0

Address Offset	0x0000 017C		
Physical Address	0x5201 117C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM15UPDT	PGM14UPDT	PGM13UPDT	PGM12UPDT	PGM11UPDT	PGM10UPDT	PGM9UPDT	PGM8UPDT	PGM7UPDT	PGM6UPDT	PGM5UPDT	PGM4UPDT	PGM3UPDT	PGM2UPDT	PGM1UPDT	PGM0UPDT

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	PGM15UPDT	Program 15 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
14	PGM14UPDT	Program 14 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
13	PGM13UPDT	Program 13 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
12	PGM12UPDT	Program 12 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0

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Bits	Field Name	Description	Type	Reset
11	PGM11UPDT	Program 11 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
10	PGM10UPDT	Program 10 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
9	PGM9UPDT	Program 9 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
8	PGM8UPDT	Program 8 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
7	PGM7UPDT	Program 7 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
6	PGM6UPDT	Program 6 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
5	PGM5UPDT	Program 5 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
4	PGM4UPDT	Program 4 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
3	PGM3UPDT	Program 3 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
2	PGM2UPDT	Program 2 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
1	PGM1UPDT	Program 1 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
0	PGM0UPDT	Program 0 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0

Table 8-1197. Register Call Summary for Register ISIF_FMTPGMAPU0

ISS ISP

- ISS ISP ISIF Formatter Programming: [0]
- ISS ISP ISIF Combine the Divided Input Lines: [1] [2] [3] [4]
- ISS ISP ISIF Register Setup: [5]
- ISS ISIF Register Summary: [6]

Table 8-1198. ISIF_FMTPGMAPU1

Address Offset	0x0000 0180		
Physical Address	0x5201 1180	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM31UPDT	PGM30UPDT	PGM29UPDT	PGM28UPDT	PGM27UPDT	PGM26UPDT	PGM25UPDT	PGM24UPDT	PGM23UPDT	PGM22UPDT	PGM21UPDT	PGM20UPDT	PGM19UPDT	PGM18UPDT	PGM17UPDT	PGM16UPDT

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	PGM31UPDT	Program 31 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
14	PGM30UPDT	Program 30 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
13	PGM29UPDT	Program 29 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
12	PGM28UPDT	Program 28 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
11	PGM27UPDT	Program 27 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
10	PGM26UPDT	Program 26 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
9	PGM25UPDT	Program 25 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
8	PGM24UPDT	Program 24 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
7	PGM23UPDT	Program 23 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
6	PGM22UPDT	Program 22 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
5	PGM21UPDT	Program 21 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
4	PGM20UPDT	Program 20 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
3	PGM19UPDT	Program 19 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
2	PGM18UPDT	Program 18 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0

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Bits	Field Name	Description	Type	Reset
1	PGM17UPDT	Program 17 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0
0	PGM16UPDT	Program 16 Address Pointer Update 0x0: APTR* + N (Auto increment) 0x1: APTR* - N (Auto decrement)	RW	0

Table 8-1199. Register Call Summary for Register ISIF_FMTPGMAPU1

ISS ISP
- ISS ISP ISIF Formatter Programming: [0]
- ISS ISP ISIF Combine the Divided Input Lines: [1] [2]
- ISS ISP ISIF Register Setup: [3]
- ISS ISIF Register Summary: [4]

Table 8-1200. ISIF_FMTPGMAPS0

Address Offset	0x0000 0184		
Physical Address	0x5201 1184	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM3APTR				PGM2APTR				PGM1APTR				PGM0APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM3APTR	Program 3 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM2APTR	Program 2 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM1APTR	Program 1 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM0APTR	Program 0 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1201. Register Call Summary for Register ISIF_FMTPGMAPS0

ISS ISP
- ISS ISP ISIF Formatter Programming: [0]
- ISS ISP ISIF Combine the Divided Input Lines: [1] [2]
- ISS ISP ISIF Register Setup: [3]
- ISS ISIF Register Summary: [4]

Table 8-1202. ISIF_FMTPGMAPS1

Address Offset	0x0000 0188		
Physical Address	0x5201 1188	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM7APTR				PGM6APTR				PGM5APTR				PGM4APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM7APTR	Program 7 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM6APTR	Program 6 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM5APTR	Program 5 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM4APTR	Program 0 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1203. Register Call Summary for Register ISIF_FMTPGMAPS1

ISS ISP

- ISS ISP ISIF Register Setup: [0]
- ISS ISIF Register Summary: [1]

Table 8-1204. ISIF_FMTPGMAPS2

Address Offset	0x0000 018C		
Physical Address	0x5201 118C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM11APTR				PGM10APTR				PGM9APTR				PGM8APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM11APTR	Program 11 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM10APTR	Program 10 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM9APTR	Program 9 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM8APTR	Program 8 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1205. Register Call Summary for Register ISIF_FMTPGMAPS2

ISS ISP

- ISS ISP ISIF Combine the Divided Input Lines: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

Table 8-1206. ISIF_FMTPGMAPS3

Address Offset	0x0000 0190		
Physical Address	0x5201 1190	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM15APTR				PGM14APTR				PGM13APTR				PGM12APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM15APTR	Program 15 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM14APTR	Program 14 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM13APTR	Program 13 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM12APTR	Program 12 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1207. Register Call Summary for Register ISIF_FMTPGMAPS3

ISS ISP

- ISS ISP ISIF Register Setup: [0]
- ISS ISIF Register Summary: [1]

Table 8-1208. ISIF_FMTPGMAPS4

Address Offset	0x0000 0194		
Physical Address	0x5201 1194	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM19APTR				PGM18APTR				PGM17APTR				PGM16APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM19APTR	Program 19 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM18APTR	Program 18 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM17APTR	Program 17 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM16APTR	Program 16 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1209. Register Call Summary for Register ISIF_FMTPGMAPS4

ISS ISP

- ISS ISP ISIF Combine the Divided Input Lines: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

Table 8-1210. ISIF_FMTPGMAPS5

Address Offset	0x0000 0198		
Physical Address	0x5201 1198	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM23APTR				PGM22APTR				PGM21APTR				PGM20APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM23APTR	Program 23 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM22APTR	Program 22 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM21APTR	Program 21 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM20APTR	Program 20 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1211. Register Call Summary for Register ISIF_FMTPGMAPS5

ISS ISP

- ISS ISP ISIF Register Setup: [0]
- ISS ISIF Register Summary: [1]

Table 8-1212. ISIF_FMTPGMAPS6

Address Offset	0x0000 019C		
Physical Address	0x5201 119C	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM27APTR				PGM26APTR				PGM25APTR				PGM24APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM27APTR	Program 27 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM26APTR	Program 26 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM25APTR	Program 25 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM24APTR	Program 24 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1213. Register Call Summary for Register ISIF_FMTPGMAPS6

ISS ISP

- ISS ISP ISIF Register Setup: [0]
- ISS ISIF Register Summary: [1]

Table 8-1214. ISIF_FMTPGMAPS7

Address Offset	0x0000 01A0		
Physical Address	0x5201 11A0	**Instance**	ISS_ISIF
Description	Input Data Formatter Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PGM31APTR				PGM30APTR				PGM29APTR				PGM28APTR			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PGM31APTR	Program 31 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
11:8	PGM30APTR	Program 30 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
7:4	PGM29APTR	Program 29 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0
3:0	PGM28APTR	Program 28 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)	RW	0x0

Table 8-1215. Register Call Summary for Register ISIF_FMTPGMAPS7

ISS ISP

- ISS ISP ISIF Formatter Programming: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1216. ISIF_CSCCTL

Address Offset	0x0000 01A4		
Physical Address	0x5201 11A4	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															CSCEN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:1	RESERVED		R	0x0000
0	CSCEN	Controls ON/OFF of Color Space converter. 0x0: Disable 0x1: Enable	RW	0

Table 8-1217. Register Call Summary for Register ISIF_CSCCTL

ISS ISP

- ISS ISP ISIF Color Space Converter: [0]
- ISS ISP ISIF Register Setup: [1]
- ISS ISIF Register Summary: [2]

Table 8-1218. ISIF_CSCM0

Address Offset	0x0000 01A8		
Physical Address	0x5201 11A8	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM01								CSCM00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM01	Color Space convert coefficient value M01: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM00	Color Space convert coefficient value M00: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1219. Register Call Summary for Register ISIF_CSCM0

ISS ISP
- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

Table 8-1220. ISIF_CSCM1

Address Offset	0x0000 01AC		
Physical Address	0x5201 11AC	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM03								CSCM02							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM03	Color Space convert coefficient value M03: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM02	Color Space convert coefficient value M02: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1221. Register Call Summary for Register ISIF_CSCM1

ISS ISP
- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

Table 8-1222. ISIF_CSCM2

Address Offset	0x0000 01B0		
Physical Address	0x5201 11B0	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM11								CSCM10							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM11	Color Space convert coefficient value M11: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM10	Color Space convert coefficient value M10: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1223. Register Call Summary for Register ISIF_CSCM2

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

Table 8-1224. ISIF_CSCM3

Address Offset	0x0000 01B4		
Physical Address	0x5201 11B4	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM13								CSCM12							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM13	Color Space convert coefficient value M13: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM12	Color Space convert coefficient value M12: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1225. Register Call Summary for Register ISIF_CSCM3

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

Table 8-1226. ISIF_CSCM4

Address Offset	0x0000 01B8		
Physical Address	0x5201 11B8	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM21								CSCM20							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM21	Color Space convert coefficient value M21: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM20	Color Space convert coefficient value M20: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

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Table 8-1227. Register Call Summary for Register ISIF_CSCM4

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

Table 8-1228. ISIF_CSCM5

Address Offset	0x0000 01BC		
Physical Address	0x5201 11BC	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM23								CSCM22							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM23	Color Space convert coefficient value M23: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM22	Color Space convert coefficient value M22: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1229. Register Call Summary for Register ISIF_CSCM5

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

Table 8-1230. ISIF_CSCM6

Address Offset	0x0000 01C0		
Physical Address	0x5201 11C0	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM31								CSCM30							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM31	Color Space convert coefficient value M31: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM30	Color Space convert coefficient value M30: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1231. Register Call Summary for Register ISIF_CSCM6

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

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Table 8-1232. ISIF_CSCM7

Address Offset	0x0000 01C4		
Physical Address	0x5201 11C4	**Instance**	ISS_ISIF
Description	Color Space Converter Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CSCM33								CSCM32							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	CSCM33	Color Space convert coefficient value M33: This value is signed 8-bit with the 5-bits decimal.	RW	0x00
7:0	CSCM32	Color Space convert coefficient value M32: This value is signed 8-bit with the 5-bits decimal.	RW	0x00

Table 8-1233. Register Call Summary for Register ISIF_CSCM7

ISS ISP

- ISS ISP ISIF Color Space Converter: [0] [1]
- ISS ISP ISIF Register Setup: [2]
- ISS ISIF Register Summary: [3]

Table 8-1234. ISIF_CLKCTL

Address Offset	0x0000 01F8		
Physical Address	0x5201 11F8	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED														CLKEN1	CLKEN2

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:2	RESERVED		R	0x0000
1	CLKEN1	Forces isif_clken1 to be active. (Test mode) 0x0: normal mode 0x1: force isif_clken1 to be active	RW	0
0	CLKEN2	Forces isif_clken2 to be active. (Test mode) 0x0: normal mode 0x1: force isif_clken2 to be active	RW	0

Table 8-1235. Register Call Summary for Register ISIF_CLKCTL

ISS ISP

- ISS ISIF Register Summary: [0]

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8.3.5.7 ISS IPIPEIF Registers

8.3.5.7.1 ISS IPIPEIF Register Summary

Table 8-1236. ISS IPIPEIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_IPIPEIF Base Address
IPIPEIF_ENABLE	RW	32	0x0000 0000	0x5201 1200
IPIPEIF_CFG1	RW	32	0x0000 0004	0x5201 1204
IPIPEIF_PPLN	RW	32	0x0000 0008	0x5201 1208
IPIPEIF_LPFR	RW	32	0x0000 000C	0x5201 120C
IPIPEIF_HNUM	RW	32	0x0000 0010	0x5201 1210
IPIPEIF_VNUM	RW	32	0x0000 0014	0x5201 1214
IPIPEIF_ADDRU	RW	32	0x0000 0018	0x5201 1218
IPIPEIF_ADDRL	RW	32	0x0000 001C	0x5201 121C
IPIPEIF_ADOFS	RW	32	0x0000 0020	0x5201 1220
IPIPEIF_RSZ	RW	32	0x0000 0024	0x5201 1224
IPIPEIF_GAIN	RW	32	0x0000 0028	0x5201 1228
IPIPEIF_DPCM	RW	32	0x0000 002C	0x5201 122C
IPIPEIF_CFG2	RW	32	0x0000 0030	0x5201 1230
IPIPEIF_INIRSZ	RW	32	0x0000 0034	0x5201 1234
IPIPEIF_OCLIP	RW	32	0x0000 0038	0x5201 1238
IPIPEIF_DTUDF	RW	32	0x0000 003C	0x5201 123C
IPIPEIF_CLKDIV	RW	32	0x0000 0040	0x5201 1240
IPIPEIF_DPC1	RW	32	0x0000 0044	0x5201 1244
IPIPEIF_DPC2	RW	32	0x0000 0048	0x5201 1248
IPIPEIF_RSZ3A	RW	32	0x0000 0054	0x5201 1254
IPIPEIF_INIRSZ3A	RW	32	0x0000 0058	0x5201 1258

8.3.5.7.2 ISS IPIPEIF Register Description

Table 8-1237. IPIPEIF_ENABLE

Address Offset	0x0000 0000		
Physical Address	0x5201 1200	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Enable.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SYNCOFF	ENABLE

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	SYNCOFF	VD output mask This register masks the VD output to the IPIPE module. This can be useful when one wants to read data from SDRAM which are stored in a double buffer. If the VD is not masked each time we start the module an new VD will be generated to the IPIPEIF module. Let's consider two buffers A and B of N lines each. *This bit field is latched by VD. 0x0: VD output mask is disabled. 0x1: VD output mask is enabled.	RW	0
0	ENABLE	IPIPE I/F Enable This register is used to start the operation of SDRAM buffer memory read and generates SYNC signals. This register is available when INPSRC1 or INPSCR2 = 1, 2 or 3. 0x0: disable 0x1: enable	RW	0

Table 8-1238. Register Call Summary for Register IPIPEIF_ENABLE

ISS ISP

- ISS ISP IPIPEIF Input From BL: [0]
- ISS ISP IPIPEIF Timing Generation: [1]
- ISS ISP IPIPEIF Register Setup: [2]
- ISS ISP IPIPEIF Enable/Disable Hardware: [3] [4] [5] [6]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [7] [8] [9]
- ISS IPIPEIF Register Summary: [10]

Table 8-1239. IPIPEIF_CFG1

Address Offset	0x0000 0004		
Physical Address	0x5201 1204	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Configuration #1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																INPSRC1		DATASFT			CLKSEL	UNPACK		AVGFILT	RESERVED				INPSRC2		DECIM	ONESHOT

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	INPSRC1	Selects the source for the mux (VPORT / ISIF / SDRAM) as well as the data format type. 0x0: VPORT_RAW 0x1: SDRAM_RAW 0x3: SDRAM_YUV 0x2: ISIF_DARKFM Input ports to DFS submodule are VPORT and SDRAM.	RW	0x0

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Bits	Field Name	Description	Type	Reset
13:11	DATASFT	SDRAM read data shift This register is available when INPSRC1 or INPSRC2 = 1 or 2, that is, when data are read from SDRAM. 0x6: Output data[11:0] = (read data[15:4] >> 4) & 0x0FFF 0x1: Output data[11:0] = (read data[11:0] << 1) & 0x0FFF 0x7: Output data[11:0] = (read data[15:4] >>4) & 0x0FFF 0x0: Output data[11:0] = (read data[11:0]) & 0x0FFF 0x2: Output data[11:0] = (read data[11:0] << 2) & 0x0FFF 0x4: Output data[11:0] = (read data[11:0] << 4) & 0x0FFF 0x5: Output data[11:0] = (read data[15:4] >> 4) & 0x0FFF 0x3: Output data[11:0] = (read data[11:0] << 3) & 0x0FFF	RW	0x0
10	CLKSEL	IPIPEIF and IPIPE module pixel clock selection. This register must be set to 1 when INPSRC1 or INPSRC2 = 1 or 3, that is, data are solely read from SDRAM (VPORT inactive). 0x0: Selects the pixel clock from the VPORT. 0x1: Selects the pixel clock from the fractional clock divider. The fractional clock divider value is setup with the IPIPEIF_CLKDIV register.	RW	0
9:8	UNPACK	8-Bit, 12-bit Packed Mode When sensor raw data are stored in 8-bit packed mode or 12-bit packed mode, this register should code 1 or 3. This register is effective when INPSRC = 1 or 2. 0x0: 16 bits / pixel 0x1: 8 bits / pixel 0x3: 12 bits / pixel 0x2: 8 bits / pixel + inverse A law (8 bits to 10 bits)	RW	0x0
7	AVGFILT	Averaging Filter It applies (1,2,1) filter for the RGB/YCbCr data. *This bit field is latched by VD. 0x0: disable 0x1: enable	RW	0
6:4	RESERVED		R	0x0
3:2	INPSRC2	Selects the source for the mux (ISIF / SDRAM) as well as the data format type. 0x0: ISIF 0x1: SDRAM_RAW 0x3: SDRAM_YUV 0x2: ISIF_DARKFM Input ports to DFS submodule are ISIF and SDRAM.	RW	0x0
1	DECIM	Pixel Decimation The decimation rate defined by RSZ register. *This bit field is latched by VD. 0x0: No decimation 0x1: Decimation	RW	0
0	ONESHOT	One Shot Mode This register is available when INPSRC = 1 or 3. 0x0: Continuous mode 0x1: One shot mode	RW	0

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Table 8-1240. Register Call Summary for Register IPIPEIF_CFG1

ISS ISP

- ISS ISP IPIPEIF Data Path Selection: [0] [1] [2] [3]
- ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 0: [4] [5]
- ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 1: [6] [7]
- ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 2: [8] [9]
- ISS ISP IPIPEIF INPSRC1 = 0 and INPSRC2 = 3: [10] [11]
- ISS ISP IPIPEIF INPSRC1 = 1 and INPSRC2 = 0: [12] [13]
- ISS ISP IPIPEIF INPSRC1 = 2 and INPSRC2 = 0: [14] [15]
- ISS ISP IPIPEIF INPSRC1 = 3 and INPSRC2 = 0: [16] [17]
- ISS ISP IPIPEIF Timing Generation: [18] [19] [20] [21] [22] [23] [24] [25]
- ISS ISP IPIPEIF Fractional Clock Divider: [26] [27] [28]
- ISS ISP IPIPEIF Decompression (DCPM) Subblock: Unpack and Decompression Function: [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41]
- ISS ISP IPIPEIF Dark-Frame Subtraction Functionality: [42] [43] [44] [45] [46]
- ISS ISP IPIPEIF (1, 2, 1) Averaging Filter for IPIPE Data Path: [47] [48] [49] [50] [51]
- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for IPIPE Data Path: [52]
- ISS ISP IPIPEIF YUV4:2:2 8-bit Packed Data Input Coming From ISIF Module: [53]
- ISS ISP IPIPEIF YUV4:2:0 Data Input for Memory-to-Memory Resize Operations: [54] [55] [56] [57] [58] [59] [60] [61]
- ISS ISP IPIPEIF Register Setup: [62] [63] [64] [65] [66] [67] [68] [69] [70]
- ISS ISP IPIPEIF Enable/Disable Hardware: [71] [72] [73] [74] [75]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [76] [77]
- ISS ISP IPIPEIF Summary of Constraints: [78] [79]
- ISS IPIPEIF Register Summary: [80]
- ISS IPIPEIF Register Description: [81] [82] [83] [84]

Table 8-1241. IPIPEIF_PPLN

Address Offset	0x0000 0008		
Physical Address	0x5201 1208	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Interval of HD / Start pixel in HD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								PPLN							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	PPLN	Case-1: Interval of Horizontal Sync (HD) Specifies the interval of horizontal sync. This register is available when INPSRC = 1 or 3. Case-2: Start Pixel in Horizontal Sync (HD) Specifies the start pixel in horizontal sync. This register is available when INPSRC = 2 *This bit field is latched by VD.	RW	0x0000

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Table 8-1242. Register Call Summary for Register IPIPEIF_PPLN

ISS ISP

- ISS ISP IPIPEIF Input From BL: [0] [1] [2] [3]
- ISS ISP IPIPEIF Register Setup: [4]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [5]
- ISS ISP IPIPEIF Summary of Constraints: [6]
- ISS IPIPEIF Register Summary: [7]

Table 8-1243. IPIPEIF_LPFR

Address Offset	0x0000 000C		
Physical Address	0x5201 120C	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Interval of VD / Start line in VD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								LPFR							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	LPFR	Case-1: Interval of Vertical Sync (VD) Specifies the interval of vertical sync. This register is available when INPSRC = 1 or 3. Case-2: Start Pixel in Vertical Sync (VD) Specifies the start line in vertical sync. This register is available when INPSRC = 2 *This bit field is latched by VD.	RW	0x0000

Table 8-1244. Register Call Summary for Register IPIPEIF_LPFR

ISS ISP

- ISS ISP IPIPEIF Input From BL: [0] [1] [2] [3] [4]
- ISS ISP IPIPEIF Register Setup: [5]
- ISS ISP IPIPEIF Summary of Constraints: [6] [7]
- ISS IPIPEIF Register Summary: [8]

Table 8-1245. IPIPEIF_HNUM

Address Offset	0x0000 0010		
Physical Address	0x5201 1210	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Number of valid pixels per line		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								HNUM							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12:0	HNUM	The Number of Valid Pixels in a Line Specifies the number of valid pixels in a horizontal line. This register is available when INPSRC = 1, 2 or 3 *This bit field is latched by VD.	RW	0x0000

Table 8-1246. Register Call Summary for Register IPIPEIF_HNUM

ISS ISP

- ISS ISP IPIPEIF Input From BL: [0] [1] [2] [3]
- ISS ISP IPIPEIF Register Setup: [4]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [5]
- ISS ISP IPIPEIF Summary of Constraints: [6]
- ISS IPIPEIF Register Summary: [7]

Table 8-1247. IPIPEIF_VNUM

Address Offset	0x0000 0014		
Physical Address	0x5201 1214	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Number of valid lines per frame		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VNUM							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12:0	VNUM	The Number of Valid Line in a Vertical Specifies the number of valid line in a vertical. This register is available when INPSRC = 1, 2 or 3 *This bit field is latched by VD.	RW	0x0000

Table 8-1248. Register Call Summary for Register IPIPEIF_VNUM

ISS ISP

- ISS ISP IPIPEIF Input From BL: [0] [1] [2] [3]
- ISS ISP IPIPEIF Register Setup: [4]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [5]
- ISS ISP IPIPEIF Summary of Constraints: [6]
- ISS IPIPEIF Register Summary: [7]

Table 8-1249. IPIPEIF_ADDRU

Address Offset	0x0000 0018		
Physical Address	0x5201 1218	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Memory Address (Upper)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDRU							

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Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:0	ADDRU	Memory Address - Upper Memory address upper 11-bits are specified in units of 32-bytes This register is available when INPSRC = 1, 2 or 3. *This bit field is latched by VD.	RW	0x000

Table 8-1250. Register Call Summary for Register IPIPEIF_ADDRU

ISS ISP

- ISS ISP IPIPEIF Input From BL: [0]
- ISS ISP IPIPEIF Register Setup: [1]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [2]
- ISS IPIPEIF Register Summary: [3]

Table 8-1251. IPIPEIF_ADDRL

Address Offset	0x0000 001C		
Physical Address	0x5201 121C	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Memory Address (Lower)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDRL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	ADDRL	Memory Address - Lower Memory address lower 16-bits are specified in units of 32-bytes. This register is available when INPSRC = 1, 2 or 3. *This bit field is latched by VD.	RW	0x0000

Table 8-1252. Register Call Summary for Register IPIPEIF_ADDRL

ISS ISP

- ISS ISP IPIPEIF Input From BL: [0]
- ISS ISP IPIPEIF Register Setup: [1]
- ISS IPIPEIF Register Summary: [2]

Table 8-1253. IPIPEIF_ADOFS

Address Offset	0x0000 0020		
Physical Address	0x5201 1220	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Address offset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				ADOFS											

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Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	ADOFS	Specifies the SDRAM stride for each line in units of 32-bytes. This register is available when reading data from SDRAM: INPSRC1 or INPSRC2 = 1, 2 or 3. Assuming that the first line is at position ADDR, the second line is at address ADDR+ ADOFS, etc. *This bit field is latched by VD.	RW	0x000

Table 8-1254. Register Call Summary for Register IPIPEIF_ADOFS

ISS ISP

- ISS ISP IPIPEIF Input From BL: [0]
- ISS ISP IPIPEIF Register Setup: [1]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [2]
- ISS IPIPEIF Register Summary: [3]

Table 8-1255. IPIPEIF_RSZ

Address Offset	0x0000 0024		
Physical Address	0x5201 1224	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Horizontal Resizing Parameter on IPIPE data path		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RSZ							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000000
6:0	RSZ	Horizontal Resizing Parameter for IPIPE data path Specifies the horizontal resizing parameter. The RSZ register can be configured within 16 to 112 range. This resizing ratio is determined by 16/RSZ (= 1/1 to 1/7) *This bit field is latched by VD.	RW	0x10

Table 8-1256. Register Call Summary for Register IPIPEIF_RSZ

ISS ISP

- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for IPIPE Data Path: [0]
- ISS ISP IPIPEIF Register Setup: [1]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [2]
- ISS IPIPEIF Register Summary: [3]

Table 8-1257. IPIPEIF_GAIN

Address Offset	0x0000 0028		
Physical Address	0x5201 1228	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Gain Parameter		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						GAIN									

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Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:0	GAIN	Gain Parameter Specifies the gain applied to RAW data before it is forwarded to the IPIPE module. The gain value is expressed using the U10Q9 fractional format. The range is from 0.00195 (1/512) to 1.99805(1023/512). By default the unity gain is applied, that is, IPIPEIF_GAIN.GAIN = 0x200. The gain is applied to RAW data only (IPIPEIF_CFG1.INPSRC2 != 3): the gain is not applied if the input data is YCbCr. *This bit field is latched by VD.	RW	0x200

Table 8-1258. Register Call Summary for Register IPIPEIF_GAIN

ISS ISP

- ISS ISP IPIPEIF RAW Data Gain for IPIPE Data Path: [0]
- ISS ISP IPIPEIF Register Setup: [1]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [2]
- ISS IPIPEIF Register Summary: [3]
- ISS IPIPEIF Register Description: [4]

Table 8-1259. IPIPEIF_DPCM

Address Offset	0x0000 002C		
Physical Address	0x5201 122C	**Instance**	ISS_IPIPEIF
Description	IPIPEIF DPCM configuration This register applies only if IPIPEIF_CFG1.UNPACK = 1, that is, RAW8 data is read from SDRAM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													BITS	PRED	ENA

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	BITS	DPCM bit mode for SDRAM data 0x0: 8bit to 10bit DPCM decompression 0x1: 8bit to 12bit DPCM decompression	RW	0
1	PRED	DPCM prediction mode for SDRAM data 0x0: Simple predictor 0x1: Advanced predictor	RW	0
0	ENA	DPCM decompression enable for SDRAM data. 0x0: DPCM off (no decompression) 0x1: DPCM on	RW	0

Table 8-1260. Register Call Summary for Register IPIPEIF_DPCM

ISS ISP

- ISS ISP IPIPEIF Decompression (DCPM) Subblock: Unpack and Decompression Function: [0] [1] [2] [3] [4] [5] [6]
- ISS ISP IPIPEIF Register Setup: [7] [8] [9]
- ISS IPIPEIF Register Summary: [10]

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Table 8-1261. IPIPEIF_CFG2

Address Offset	0x0000 0030		
Physical Address	0x5201 1230	**Instance**	ISS_IPIPEIF
Description	IPIPEIF Configuration #2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								YUV8P	YUV8	DFSDIR	RESERVED	YUV16	VDPOL	HDPOL	INTSW

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7	YUV8P	8-bit YUV data unpacking to 16 bits When IPIPEIF_CFG1.INPSRC2 = 0 and IPIPEIF_CFG2.YUV16 = 1, the 8-bit YUV data are transformed into 16-bit YUV data. The way the data are unpacked from 8 bits to 16 bits is controlled by the IPIPEIF_CFG2.YUV8P register. The upper 8 bits of the 16-bit output are set to 0. 0x0: Y output on even pixels C output on odd pixels 0x1: C output on even pixels Y output on odd pixels	RW	0
6	YUV8	YUV 8bit mode When ISIF_CFG1.INPSRC2 = 0 and YUV16 = 1, setting this bit to 1 enables the conversion from 8-bit YUV input to 16-bit YUV. This register is used when the input data from the ISIF module is 8-bit YUV data. 0x0: YUV16 0x1: YUV8 to 16	RW	0
5	DFSDIR	DFS direction Selects the direction of dark frame subtraction. 0x0: VPORT IF(capture frame) - SDRAM (dark frame) 0x1: SDRAM (capture frame) - VPORT IF(dark frame)	RW	0
4	RESERVED	Read returns reset value	RW	0

3	YUV16	Data type selection. The behavior of this bit field depends upon other register settings. The functionality is best explained with the following pseudo code:
		if ((CFG1.INPSRC2==0 && CFG2.YUV16) ||
		CFG1.INPSRC2==3) {
		data_out[15:0] = yuv[15:0]
		}
		else if (CFG1.INPSRC2==1 && CFG2.YUV16 &&
		CFG1.UNPACK=1) {
		data_out[15:8] = gain_clip[7:0];
		data_out[7:0] = 0;
		}
		else {
		data_out[15:12] = 0;
		data_out[11: 0] = gain_clip[11:0];
		}
		where:
		o data_out[15:0] = 16-bit YUV or 12-bit RAW data to ipipe
		o yuv[15:0] = 16-bit YUV data from "horizontal pixel decimator" block.
		o gain_clip[11:0] = 12-bit RAW data from "gain" block.
		0x0: 12-bit RAW data
		0x1: 16-bit YUV data
			RW	0

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Bits	Field Name	Description	Type	Reset
2	VDPOL	VD Sync Polarity When input VD is active low SYNC pulse, this bit needs to be set to 1. 0x0: Positive 0x1: Negative	RW	0
1	HDPOL	HD Sync Polarity When input HD is active low SYNC pulse, this bit needs to be set to 1. 0x0: Positive 0x1: Negative	RW	0
0	INTSW	IPIPEIF interrupt source selection. This register select the interrupt source. 0x0: Start position of VD from VPORT interface 0x1: Start position of VD from ISIF module	RW	0

Table 8-1262. Register Call Summary for Register IPIPEIF_CFG2

ISS ISP

- ISS ISP IPIPEIF DFS Subtraction Direction: [0] [1] [2] [3] [4] [5]
- ISS ISP IPIPEIF (1, 2, 1) Averaging Filter for IPIPE Data Path: [6]
- ISS ISP IPIPEIF YUV4:2:2 8-bit Packed Data Input Coming From ISIF Module: [7] [8] [9]
- ISS ISP IPIPEIF YUV4:2:0 Data Input for Memory-to-Memory Resize Operations: [10] [11]
- ISS ISP IPIPEIF Module Events and Status Checking: [12]
- ISS ISP IPIPEIF Register Setup: [13] [14] [15] [16] [17] [18] [19] [20]
- ISS IPIPEIF Register Summary: [21]
- ISS IPIPEIF Register Description: [22] [23]

Table 8-1263. IPIPEIF_INIRSZ

Address Offset	0x0000 0034		
Physical Address	0x5201 1234	**Instance**	ISS_IPIPEIF
Description	IPIPEIF resize initial position - IPIPE data path.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		ALNSYNC	INIRSZ												

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	ALNSYNC	Align the HSYNC, VSYNC to initial position defined by INIRSZ. 0x0: Disable 0x1: Enable	RW	0
12:0	INIRSZ	Offset used to re-initialize the HD/VD position after resizer. From 0 to 8191 PCLK cycles. Skips INIRSZ pixels for every line.	RW	0x0000

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Table 8-1264. Register Call Summary for Register IPIPEIF_INIRSZ

ISS ISP

- ISS ISP IPIPEIF (1, 2, 1) Averaging Filter for IPIPE Data Path: [0]
- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for IPIPE Data Path: [1] [2]
- ISS ISP IPIPEIF Register Setup: [3] [4]
- ISS IPIPEIF Register Summary: [5]

Table 8-1265. IPIPEIF_OCLIP

Address Offset	0x0000 0038		
Physical Address	0x5201 1238	**Instance**	ISS_IPIPEIF
Description	IPIPEIF output clipping value		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				OCLIP											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	OCLIP	Output clipping value after gain control on IPIPE data path. This value is in U12Q0 data format.	RW	0xFFF

Table 8-1266. Register Call Summary for Register IPIPEIF_OCLIP

ISS ISP

- ISS ISP IPIPEIF RAW Data Gain for IPIPE Data Path: [0]
- ISS ISP IPIPEIF Register Setup: [1]
- ISS IPIPEIF Register Summary: [2]

Table 8-1267. IPIPEIF_DTUDF

Address Offset	0x0000 003C		
Physical Address	0x5201 123C	**Instance**	ISS_IPIPEIF
Description	IPIPEIF data underflow detection		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								FIFOWMRKLVL						ENM2MSTALL	DTUDF

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:6	RESERVED		R	0x0000
5:2	FIFOWMRKLVL	To guarantee that the FIFO does not overflow, the stall request is deasserted only when a certain number of locations in the FIFO are free. The number of free locations is configurable. A safe number of mandatory free locations can be configured by taking into consideration the pixel clock frequency (PCLK) with respect to that of the functional clock (ISP_FCLK). The worst case occurs when PCLK = ISP_FCLK. In that case, value should be configured to 0 (i.e. 16 free locations), so that the stall will be deasserted only when the 16-deep FIFO is completely empty. 0: Stall deassertion when FIFO is empty (16 free locations) and SDRAM data available; 1: Stall deassertion when FIFO has not more than 1 valid entry and SDRAM data available; … 15: Stall deassertion when FIFO has not more than 15 valid entries and SDRAM data available;	RW	0x0
1	ENM2MSTAL	Enable memory-to-memory stall mechanism: 0: disable (no special stall mechanism for memory-to-memory use cases); 1: enable (stall mechanism for memory-to-memory use cases);	RW	0
0	DTUDF	Data under flow error status register. Reading 1 shows there is data under flow and at least one data is corrupted while reading from SDRAM. Writing 1 to this register clears (=0) the error (=1) status. Underflow errors are non recoverable at ISP level, need to do a soft reset at ISS level. The IPIPEIF_UDF interrupt is generated when an underflow happens. The interrupt avoids polling this register for errors. If bit [1] ENM2MSTAL = 1, then programmers need to ensure that the SW does not clear bit [0] DTUDF, as this would reset the MTC read interface. Bit DTUDF can be cleared only in the on-the-fly operation where the stall mechanism will not work.	RW	0

Table 8-1268. Register Call Summary for Register IPIPEIF_DTUDF

ISS ISP

- ISS ISP IPIPEIF Dark-Frame Subtraction Functionality: [0] [1] [2]
- ISS ISP IPIPEIF Module Events and Status Checking: [3]
- ISS IPIPEIF Register Summary: [4]

Table 8-1269. IPIPEIF_CLKDIV

Address Offset	0x0000 0040		
Physical Address	0x5201 1240	**Instance**	ISS_IPIPEIF
Description	IPIPEIF CLOCK DIVIDER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLKDIV															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	CLKDIV	IPIPEIF clock rate configuration IPIPE/IPIPEIF clock frequency = M/N x ISP_FCLK clock frequency. We have M = CLKDIV[15:8] + 1 and N = CLKDIV[7:0] + 1 This register is available when IPIPEIF_CFG1.CLKSEL = 1.	RW	0x0001

Table 8-1270. Register Call Summary for Register IPIPEIF_CLKDIV

ISS ISP

- ISS ISP IPIPEIF Timing Generation: [0]
- ISS ISP IPIPEIF Fractional Clock Divider: [1] [2]
- ISS ISP IPIPEIF Register Setup: [3]
- ISS IPIPEIF Register Summary: [4]
- ISS IPIPEIF Register Description: [5]

Table 8-1271. IPIPEIF_DPC1

Address Offset	0x0000 0044		
Physical Address	0x5201 1244	**Instance**	ISS_IPIPEIF
Description	IPIPEIF defect pixel correction #1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED			ENA	TH											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:13	RESERVED		R	0x0
12	ENA	DPC enable. Applies DPC for video port data, ISIF input path. 0x0: Disable 0x1: Enable	RW	0
11:0	TH	DPC threshold value	RW	0x000

Table 8-1272. Register Call Summary for Register IPIPEIF_DPC1

ISS ISP

- ISS ISP IPIPEIF Defect Pixel Correction: [0] [1]
- ISS ISP IPIPEIF Register Setup: [2] [3]
- ISS IPIPEIF Register Summary: [4]

Table 8-1273. IPIPEIF_DPC2

Address Offset	0x0000 0048		
Physical Address	0x5201 1248	**Instance**	ISS_IPIPEIF
Description	IPIPEIF defect pixel correction #2		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			ENA	TH											

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	ENA	DPC enable. Applies DPC for SDRAM input path. 0x0: Disable 0x1: Enable	RW	0
11:0	TH	DPC threshold value	RW	0x000

Table 8-1274. Register Call Summary for Register IPIPEIF_DPC2

ISS ISP

- ISS ISP IPIPEIF Defect Pixel Correction: [0] [1]
- ISS ISP IPIPEIF Register Setup: [2] [3]
- ISS IPIPEIF Register Summary: [4]

Table 8-1275. IPIPEIF_RSZ3A

Address Offset	0x0000 0054		
Physical Address	0x5201 1254	**Instance**	ISS_IPIPEIF
Description	IPIPEIF HORIZONTAL RESIZING PARAMETER FOR H3A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED						DECIM	AVGFILT	RESERVED							
																									RSZ						

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:10	RESERVED		R	0x00
9	DECIM	Pixel Decimation Enable The decimation rate defined by the RSZ bit field. *This bit field is latched by VD. 0x0: No Decimation 0x1: Decimate	RW	0
8	AVGFILT	Averaging Filter It applies a (1, 2, 1) filter for the RGB/YCbCr data. *This bit field is latched by VD. 0x0: Disable 0x1: Enable	RW	0
7	RESERVED		R	0
6:0	RSZ	Horizontal Resizing Parameter for H3A data path Specifies the horizontal resizing parameter. The RSZ register can be configured within 16 to 112 range. This resizing ratio is determined by 16/RSZ (= 1/1 to 1/7) *This bit field is latched by VD.	RW	0x10

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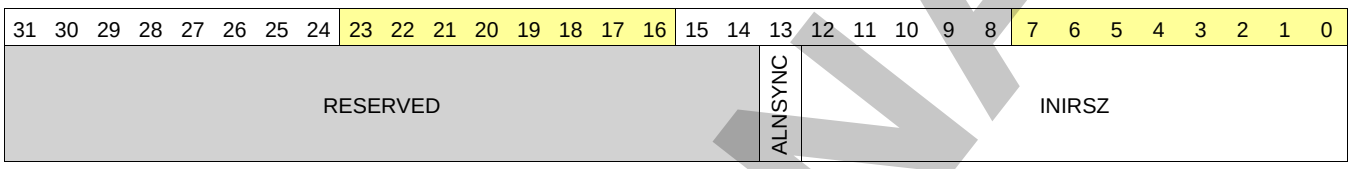
Table 8-1276. Register Call Summary for Register IPIPEIF_RSZ3A

ISS ISP

- ISS ISP IPIPEIF (1, 2 ,1) Averaging Filter for H3A Data Path: [0] [1]
- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for H3A Data Path: [2] [3]
- ISS ISP IPIPEIF Register Setup: [4] [5] [6] [7] [8]
- ISS ISP IPIPEIF Register Accessibility During Frame Processing: [9] [10] [11]
- ISS IPIPEIF Register Summary: [12]

Table 8-1277. IPIPEIF_INIRSZ3A

Address Offset	0x0000 0058		
Physical Address	0x5201 1258	**Instance**	ISS_IPIPEIF
Description	IPIPEIF resize initial position - H3A data path.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13	ALNSYNC	Align the HD, VD to initial position defined by the INIRSZ bit field. It means that HD and VD are effectively shifted by INIRSZ pixel clock cycles. 0x0: Disable 0x1: Enable	RW	0
12:0	INIRSZ	Offset used to re-initialize the HD/VD position after resizer. From 0 to 8191 PCLK cycles. Skips INIRSZ pixels for every line.	RW	0x0000

Table 8-1278. Register Call Summary for Register IPIPEIF_INIRSZ3A

ISS ISP

- ISS ISP IPIPEIF Horizontal Pixel Decimator (Downsizer) for H3A Data Path: [0] [1]
- ISS IPIPEIF Register Summary: [2]

8.3.5.8 ISS H3A Registers

8.3.5.8.1 ISS H3A Register Summary

Table 8-1279. ISS H3A Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_H3A Base Address
H3A_PID	R	32	0x0000 0000	0x5201 1400
H3A_PCR	RW	32	0x0000 0004	0x5201 1404
H3A_AFPAX1	RW	32	0x0000 0008	0x5201 1408
H3A_AFPAX2	RW	32	0x0000 000C	0x5201 140C
H3A_AFPAXSTART	RW	32	0x0000 0010	0x5201 1410
H3A_AFIIRSH	RW	32	0x0000 0014	0x5201 1414
H3A_AFBUFST	RW	32	0x0000 0018	0x5201 1418
H3A_AFCOEF010	RW	32	0x0000 001C	0x5201 141C

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Table 8-1279. ISS H3A Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_H3A Base Address
H3A_AFCOEF032	RW	32	0x0000 0020	0x5201 1420
H3A_AFCOEF054	RW	32	0x0000 0024	0x5201 1424
H3A_AFCOEF076	RW	32	0x0000 0028	0x5201 1428
H3A_AFCOEF098	RW	32	0x0000 002C	0x5201 142C
H3A_AFCOEF0010	RW	32	0x0000 0030	0x5201 1430
H3A_AFCOEF110	RW	32	0x0000 0034	0x5201 1434
H3A_AFCOEF132	RW	32	0x0000 0038	0x5201 1438
H3A_AFCOEF154	RW	32	0x0000 003C	0x5201 143C
H3A_AFCOEF176	RW	32	0x0000 0040	0x5201 1440
H3A_AFCOEF198	RW	32	0x0000 0044	0x5201 1444
H3A_AFCOEF1010	RW	32	0x0000 0048	0x5201 1448
H3A_AEWWIN1	RW	32	0x0000 004C	0x5201 144C
H3A_AEWINSTART	RW	32	0x0000 0050	0x5201 1450
H3A_AEWINBLK	RW	32	0x0000 0054	0x5201 1454
H3A_AEWSUBWIN	RW	32	0x0000 0058	0x5201 1458
H3A_AEWBUFST	RW	32	0x0000 005C	0x5201 145C
H3A_AEWCFG	RW	32	0x0000 0060	0x5201 1460
H3A_LINE_START	RW	32	0x0000 0064	0x5201 1464
H3A_VFV_CFG1	RW	32	0x0000 0068	0x5201 1468
H3A_VFV_CFG2	RW	32	0x0000 006C	0x5201 146C
H3A_VFV_CFG3	RW	32	0x0000 0070	0x5201 1470
H3A_VFV_CFG4	RW	32	0x0000 0074	0x5201 1474
H3A_HVF_THR	RW	32	0x0000 0078	0x5201 1478
H3A_ADVANCED	RW	32	0x0000 007C	0x5201 147C

8.3.5.8.2 ISS H3A Register Description

Table 8-1280. H3A_PID

Address Offset	0x0000 0000		
Physical Address	0x5201 1400	**Instance**	ISS_H3A
Description	Peripheral Revision and Class Information		
Type	R		

31 30	29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4 3 2 1 0
SCHEME	RESERVED	FUNC		RTL	MAJOR	RESERVED	MINOR

Bits	Field Name	Description	Type	Reset
31:30	SCHEME		R	0x1
29:28	RESERVED		R	0x0
27:16	FUNC		R	0xD01
15:11	RTL		R	0x00
10:8	MAJOR		R	0x0
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5:0	MINOR		R	0x00

Table 8-1281. Register Call Summary for Register H3A_PID

ISS ISP

- ISS H3A Register Summary: [0]

Table 8-1282. H3A_PCR

Address Offset	0x0000 0004		
Physical Address	0x5201 1404	**Instance**	ISS_H3A
Description	Peripheral Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AVE2LMT										OVF	AF_VF_EN	AEW_MED_EN	BUSYAEAWB	AEW_ALAW_EN	AEW_EN	BUSYAF	FVMODE	RGBPOS						MED_TH						AF_MED_EN	AF_ALAW_EN	AF_EN

Bits	Field Name	Description	Type	Reset
31:22	AVE2LMT	AE/AWB Saturation Limit This is the value that all sub sampled pixels in the AE/AWB engine are compared to. If the data is greater or equal to this data then the block is considered saturated.	RW	0x3FF
21	OVF	H3A module overflow status bit. If the H3A module overflows it will keep sending data. The software can read this status bit during vertical blanking period to ensure that no overflow happened while writing out the data to SDRAM. There is also an interrupt at ISP level (H3A_OVF) which can be used to monitor this. 0x0: Read 0: No overflow pending Write 0: Status bit unchanged 0x1: Read 1: Overflow happened while writing out the data. Output data likely to be corrupted. Write 1: Clear the status bit.	RW	0
20	AF_VF_EN	AF Vertical Focus Enable 0x0: 4 Color Horizontal FV only 0x1: 1 Color Horizontal FV and 1 Color Vertical FV	RW	0
19	AEW_MED_EN	AE/AWB Median filter Enable If the median filter is enabled, then the 1st 2 and last 2 pixels in the frame are not filtered. 0x0: Disable Auto Focus median filter 0x1: Enable Auto Focus median filter	RW	0
18	BUSYAEAWB	Busy bit for AE/AWB	R	0
17	AEW_ALAW_EN	AE/AWB A-law Enable 0x0: Disable Auto exposure/white balance A-law table 0x1: Enable Auto exposure/white balance A-law table.	RW	0
16	AEW_EN	AE/AWB enable 0x0: Disable Auto exposure/white balance 0x1: Enable Auto exposure/white balance	RW	0
15	BUSYAF	Busy bit for AF.	R	0

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Bits	Field Name	Description	Type	Reset
14	FVMODE	Focus Value Accumulation Mode 0x0: Sum mode. 0x1: Peak mode.	RW	0
13:11	RGBPOS	Red, Green, and blue pixel location in the AF windows RGBPOS(0): GR and GB as Bayer pattern RGBPOS(1): RG and GB as Bayer pattern RGBPOS(2): GR and BG as Bayer pattern RGBPOS(3): RG and BG as Bayer pattern RGBPOS(4): GG and RB as custom pattern RGBPOS(5): RB and GG as custom pattern 6 and 7 are reserved This Value is only used if VF is disabled	RW	0x0
10:3	MED_TH	Median filter threshold.	RW	0xFF
2	AF_MED_EN	Auto Focus Median filter Enable If the median filter is enabled, then the 1st 2 and last 2 pixels in the frame are not in the valid region. Therefore the paxel start/end and IIR filter start positions should not be set within the 1st and last 2 pixels. 0x0: Disable AF median filter. 0x1: Enable AF median filter.	RW	0
1	AF_ALAW_EN	AF A-law table enable 0x0: Disable Auto Focus A-law table 0x1: Enable Auto Focus A-law table	RW	0
0	AF_EN	AF enable 0x0: Disable Auto Focus Engine 0x1: Enable Auto Focus Engine	RW	0

Table 8-1283. Register Call Summary for Register H3A_PCR

ISS ISP

- ISS ISP H3A Interrupts: [0]
- ISS ISP H3A Optional Preprocessing: [1] [2] [3] [4]
- ISS ISP H3A Paxel Extraction: [5] [6]
- ISS ISP H3A HFV Accumulator: [7] [8]
- ISS ISP H3A Saturation Check: [9]
- ISS ISP H3A Events and Status Checking: [10] [11] [12] [13] [14] [15]
- ISS ISP H3A Register Setup: [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- ISS ISP H3A Enable/Disable Hardware: [26] [27] [28] [29]
- ISS ISP H3A Register Accessibility During Frame Processing: [30] [31] [32] [33] [34] [35] [36]
- ISS ISP H3A Interframe Operations: [37]
- ISS H3A Register Summary: [38]

Table 8-1284. H3A_AFPAX1

Address Offset	0x0000 0008		
Physical Address	0x5201 1408	**Instance**	ISS_H3A
Description	Setup for the AF Engine Paxel Configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PAXW								RESERVED								PAXH							

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	PAXW	AF Engine Paxel Width The width of the paxel is the value of this register plus 1 multiplied by 2. The minimum width is 16 pixels, if the pixel clock is half or less of the ISP_FCLK clock. If the pixel clock is equal to ISP_FCLK, then the minimum width is 32 pixels. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
15:8	RESERVED		R	0x00
7:0	PAXH	AF Engine Paxel Height The height of the paxel is the value of this register plus 1 multiplied by 2 with a final value of 2-256 (even) * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00

Table 8-1285. Register Call Summary for Register H3A_AFPAX1

ISS ISP

- ISS ISP H3A Paxel Extraction: [0] [1] [2] [3] [4]
- ISS ISP H3A Register Setup: [5] [6]
- ISS ISP H3A Register Accessibility During Frame Processing: [7]
- ISS ISP H3A Summary of Constraints: [8] [9] [10] [11] [12] [13] [14] [15] [16] [17]
- ISS H3A Register Summary: [18]

Table 8-1286. H3A_AFPAX2

Address Offset	0x0000 000C		
Physical Address	0x5201 140C	**Instance**	ISS_H3A
Description	Setup for the AF Engine Paxel Configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								AFINCH								AFINCV								PAXVC							
PAXHC																															

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20:17	AFINCH	AF Engine Column Increments Number of columns to increment in a paxel plus 1 multiplied by 2. Thus, the number of columns that can be skipped between two processed line pairs is 2-32 (even). The starting two columns in a paxel are first processed before this field is applied. This must be set so that there are at least 4 samples on a line when combined with the number of horizontal paxels. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x0
16:13	AFINCV	AF Engine Line Increments Number of lines to increment in a Paxel plus 1 multiplied by 2. Incrementing the line in a paxel is always done on a line pair due to the fact that the RGB pattern falls in two lines. If all the lines are to be processed, this field should be set to zero, and thus line count is incremented by 2 following a line pair. Thus, the number of lines that can be skipped between two processed line pairs is 0-30 (even). The starting two lines in a paxel are first processed before this field is applied. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x0

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Bits	Field Name	Description	Type	Reset
12:6	PAXVC	AF Engine Vertical Paxel Count The number of paxels in the vertical direction plus 1. The maximum number of vertical paxels in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
5:0	PAXHC	AF Engine Horizontal Paxel Count The number of paxels in the horizontal direction plus 1. It is illegal to set a number that is greater than 35 (total of 36 paxels in the horizontal direction). The minimum number of paxels should be 2 (valid range for the field is 1-35). * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00

Table 8-1287. Register Call Summary for Register H3A_AFPAX2

ISS ISP

- ISS ISP H3A Paxel Extraction: [0] [1] [2] [3] [4] [5] [6]
- ISS ISP H3A Register Setup: [7] [8] [9] [10]
- ISS ISP H3A Register Accessibility During Frame Processing: [11]
- ISS ISP H3A Summary of Constraints: [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29]
- ISS H3A Register Summary: [30]

Table 8-1288. H3A_AFPAXSTART

Address Offset	0x0000 0010		
Physical Address	0x5201 1410	**Instance**	ISS_H3A
Description	Start Position for AF Engine Paxels		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PAXSH								RESERVED				PAXSV											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	PAXSH	AF Engine Paxel Horizontal start position Range: 2-4094 PAXSH must be equal to or greater than (IIRSH + 2) This value must be even if Vertical mode is not enabled. If Vertical mode is enabled then the lower bit of PAXSH and IIRSH must be equal. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000
15:12	RESERVED		R	0x0
11:0	PAXSV	AF Engine Paxel Vertical start position Range: 0-4095 Sets the vertical line for the first paxel. This value must be greater then or equal to 8 if the vertical mode is enabled. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000

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Table 8-1289. Register Call Summary for Register H3A_AFPAXSTART

ISS ISP

- ISS ISP H3A Paxel Extraction: [0] [1] [2] [3] [4]
- ISS ISP H3A Register Setup: [5] [6]
- ISS ISP H3A Register Accessibility During Frame Processing: [7]
- ISS ISP H3A Summary of Constraints: [8] [9] [10] [11] [12] [13] [14]
- ISS H3A Register Summary: [15]

Table 8-1290. H3A_AFIIRSH

Address Offset	0x0000 0014		
Physical Address	0x5201 1414	**Instance**	ISS_H3A
Description	Start Position for IIRSH		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				IIRSH											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	IIRSH	AF Engine IIR Horizontal Start Position Range from 0-4094. When the horizontal position of a line equals this value the shift registers are cleared on the next pixel. This value must be even if Vertical mode is not enabled. If vertical mode is enabled then the lower bit must match the paxel horizontal start position. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000

Table 8-1291. Register Call Summary for Register H3A_AFIIRSH

ISS ISP

- ISS ISP H3A Paxel Extraction: [0] [1]
- ISS ISP H3A Horizontal FV Calculator: [2]
- ISS ISP H3A Register Setup: [3]
- ISS ISP H3A Register Accessibility During Frame Processing: [4]
- ISS ISP H3A Summary of Constraints: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- ISS H3A Register Summary: [15]

Table 8-1292. H3A_AFBUFST

Address Offset	0x0000 0018		
Physical Address	0x5201 1418	**Instance**	ISS_H3A
Description	SDRAM destination address for AF engine statistics		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFBUFST																														RESERVED	

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Bits	Field Name	Description	Type	Reset
31:5	AFBUFST	SDRAM destination address for AF engine statistics The SDRAM destination address for the AF statistics. The 6 LSBs are ignored, address must be on a 64-byte boundary. This field can be altered even when the AF is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.	RW	0x0000000
4:0	RESERVED		R	0x00

Table 8-1293. Register Call Summary for Register H3A_AFBUFST

ISS ISP

- ISS ISP H3A DMA Interface: [0] [1] [2]
- ISS ISP H3A Register Setup: [3]
- ISS ISP H3A Summary of Constraints: [4]
- ISS H3A Register Summary: [5]

Table 8-1294. H3A_AFCOEF010

Address Offset	0x0000 001C		
Physical Address	0x5201 141C	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF1								RESERVED				COEFF0											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF1	AF Engine IIR filter Coefficient #1 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF0	AF Engine IIR filter Coefficient #0 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1295. Register Call Summary for Register H3A_AFCOEF010

ISS ISP

- ISS ISP H3A Horizontal FV Calculator: [0]
- ISS ISP H3A Register Setup: [1]
- ISS H3A Register Summary: [2]

Table 8-1296. H3A_AFCOEF032

Address Offset	0x0000 0020		
Physical Address	0x5201 1420	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF3								RESERVED				COEFF2											

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF3	AF Engine IIR filter Coefficient #3 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF2	AF Engine IIR filter Coefficient #2 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1297. Register Call Summary for Register H3A_AFCOEF032

ISS ISP

- ISS ISP H3A Register Setup: [0]
- ISS H3A Register Summary: [1]

Table 8-1298. H3A_AFCOEF054

Address Offset	0x0000 0024		
Physical Address	0x5201 1424	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF5								RESERVED								COEFF4							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF5	AF Engine IIR filter Coefficient #5 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF4	AF Engine IIR filter Coefficient #4 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1299. Register Call Summary for Register H3A_AFCOEF054

ISS ISP

- ISS ISP H3A Register Setup: [0]
- ISS H3A Register Summary: [1]

Table 8-1300. H3A_AFCOEF076

Address Offset	0x0000 0028		
Physical Address	0x5201 1428	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF7								RESERVED								COEFF6							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF7	AF Engine IIR filter Coefficient #7 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
11:0	COEFF6	AF Engine IIR filter Coefficient #6 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1301. Register Call Summary for Register H3A_AFCOEF076

ISS ISP
- ISS ISP H3A Register Setup: [0]
- ISS H3A Register Summary: [1]

Table 8-1302. H3A_AFCOEF098

Address Offset	0x0000 002C		
Physical Address	0x5201 142C	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF9								RESERVED				COEFF8											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF9	AF Engine IIR filter Coefficient #9 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF8	AF Engine IIR filter Coefficient #8 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1303. Register Call Summary for Register H3A_AFCOEF098

ISS ISP
- ISS ISP H3A Register Setup: [0]
- ISS H3A Register Summary: [1]

Table 8-1304. H3A_AFCOEF0010

Address Offset	0x0000 0030		
Physical Address	0x5201 1430	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				COEFF10											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	COEFF10	AF Engine IIR filter Coefficient #10 (Set 0) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1305. Register Call Summary for Register H3A_AFCOEF0010

ISS ISP
- ISS ISP H3A Horizontal FV Calculator: [0]
- ISS ISP H3A Register Setup: [1]
- ISS H3A Register Summary: [2]

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Table 8-1306. H3A_AFCOEF110

Address Offset	0x0000 0034		
Physical Address	0x5201 1434	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF1								RESERVED								COEFF0							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF1	AF Engine IIR filter Coefficient #1 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF0	AF Engine IIR filter Coefficient #0 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1307. Register Call Summary for Register H3A_AFCOEF110

ISS ISP

- ISS ISP H3A Horizontal FV Calculator: [0]
- ISS ISP H3A Register Setup: [1]
- ISS H3A Register Summary: [2]

Table 8-1308. H3A_AFCOEF132

Address Offset	0x0000 0038		
Physical Address	0x5201 1438	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF3								RESERVED								COEFF2							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF3	AF Engine IIR filter Coefficient #3 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF2	AF Engine IIR filter Coefficient #2 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1309. Register Call Summary for Register H3A_AFCOEF132

ISS ISP

- ISS ISP H3A Register Setup: [0]
- ISS H3A Register Summary: [1]

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Table 8-1310. H3A_AFCOEF154

Address Offset	0x0000 003C		
Physical Address	0x5201 143C	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF5								RESERVED								COEFF4							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF5	AF Engine IIR filter Coefficient #5 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF4	AF Engine IIR filter Coefficient #4 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1311. Register Call Summary for Register H3A_AFCOEF154

ISS ISP

- ISS ISP H3A Register Setup: [0]
- ISS H3A Register Summary: [1]

Table 8-1312. H3A_AFCOEF176

Address Offset	0x0000 0040		
Physical Address	0x5201 1440	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF7								RESERVED								COEFF6							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF7	AF Engine IIR filter Coefficient #7 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF6	AF Engine IIR filter Coefficient #6 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1313. Register Call Summary for Register H3A_AFCOEF176

ISS ISP

- ISS ISP H3A Register Setup: [0]
- ISS H3A Register Summary: [1]

Table 8-1314. H3A_AFCOEF198

Address Offset	0x0000 0044		
Physical Address	0x5201 1444	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COEFF9								RESERVED								COEFF8							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	COEFF9	AF Engine IIR filter Coefficient #9 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000
15:12	RESERVED		R	0x0
11:0	COEFF8	AF Engine IIR filter Coefficient #8 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1315. Register Call Summary for Register H3A_AFCOEF198

ISS ISP
- ISS ISP H3A Register Setup: [0]
- ISS H3A Register Summary: [1]

Table 8-1316. H3A_AFCOEF1010

Address Offset	0x0000 0048		
Physical Address	0x5201 1448	**Instance**	ISS_H3A
Description	IIR filter coefficient data for SET 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				COEFF10											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	COEFF10	AF Engine IIR filter Coefficient #10 (Set 1) The range is signed -32 <= value <= 31 +63/64	RW	0x000

Table 8-1317. Register Call Summary for Register H3A_AFCOEF1010

ISS ISP
- ISS ISP H3A Horizontal FV Calculator: [0]
- ISS ISP H3A Register Setup: [1]
- ISS H3A Register Summary: [2]

Table 8-1318. H3A_AEWWIN1

Address Offset	0x0000 004C		
Physical Address	0x5201 144C	**Instance**	ISS_H3A
Description	Configuration for AE/AWB Windows.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WINH								RESERVED								WINW								WINVC							
																								WINHC							

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Bits	Field Name	Description	Type	Reset
31:24	WINH	AE/AWB Engine Window Height This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2-512 (even) * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
23:21	RESERVED		R	0x0
20:13	WINW	AE/AWB Engine Window Width This specifies the window width in an even number of pixels, the window width is the value plus 1 multiplied by 2. The minimum width is 16 pixels, if the pixel clock is half or less of the ISP_FCLK clock. If the pixel clock is equal to ISP_FCLK, then the minimum width is 32 pixels. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
12:6	WINVC	AE/AWB Engine Vertical Window Count The number of windows in the vertical direction plus 1. The maximum number of vertical windows in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00
5:0	WINHC	AE/AWB Engine Horizontal Window Count The number of horizontal windows plus 1. The maximum number of horizontal windows is 35 plus 1 (36). The minimum number of windows should be 2 (valid range for the field is 1-35). * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00

Table 8-1319. Register Call Summary for Register H3A_AEWWIN1

ISS ISP

- ISS ISP H3A Subsampler: [0] [1] [2] [3]
- ISS ISP H3A Additional Black Row of AE/AWB Windows: [4] [5] [6] [7]
- ISS ISP H3A Register Setup: [8] [9] [10] [11]
- ISS ISP H3A Register Accessibility During Frame Processing: [12]
- ISS ISP H3A Summary of Constraints: [13] [14] [15] [16] [17] [18] [19] [20] [21] [22]
- ISS H3A Register Summary: [23]

Table 8-1320. H3A_AEWINSTART

Address Offset	0x0000 0050		
Physical Address	0x5201 1450	**Instance**	ISS_H3A
Description	Start position for AE/AWB Windows.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WINSV								RESERVED								WINSH							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	WINSV	AE/AWB Engine Vertical Window Start Position Sets the first line for the first window. Range 0-4095 * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000
15:12	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
11:0	WINSH	AE/AWB Engine Horizontal Window Start Position Sets the horizontal position for the first window on each line. Range 0-4095 * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x000

Table 8-1321. Register Call Summary for Register H3A_AEWINSTART

ISS ISP

- ISS ISP H3A Subsampler: [0] [1]
- ISS ISP H3A Additional Black Row of AE/AWB Windows: [2] [3]
- ISS ISP H3A Register Setup: [4] [5]
- ISS ISP H3A Register Accessibility During Frame Processing: [6]
- ISS H3A Register Summary: [7]

Table 8-1322. H3A_AEWINBLK

Address Offset	0x0000 0054		
Physical Address	0x5201 1454	**Instance**	ISS_H3A
Description	Start position and height for black line of AE/AWB Windows		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WINSV								RESERVED								WINH							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	WINSV	AE/AWB Engine Vertical Window Start Position for single black line of windows Sets the first line for the single black line of windows. * This value is shadowed and latched on the rising edge of VSYNC. Range 0-4095 Note that the horizontal start and the horizontal number of windows will be similar to the regular windows	RW	0x000
15:7	RESERVED		R	0x000
6:0	WINH	AE/AWB Engine Window Height for the single black line of windows This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2-256 (even) * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x00

Table 8-1323. Register Call Summary for Register H3A_AEWINBLK

ISS ISP

- ISS ISP H3A Additional Black Row of AE/AWB Windows: [0] [1] [2] [3]
- ISS ISP H3A Register Setup: [4] [5]
- ISS ISP H3A Register Accessibility During Frame Processing: [6]
- ISS ISP H3A Summary of Constraints: [7] [8]
- ISS H3A Register Summary: [9]

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Table 8-1324. H3A_AEWSUBWIN

Address Offset	0x0000 0058		
Physical Address	0x5201 1458	**Instance**	ISS_H3A
Description	Configuration for subsample data in AE/AWB window.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				AEWINCV				RESERVED				AEWINCH			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:8	AEWINCV	AE/AWB Engine Vertical Sampling Point Increment Sets vertical distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x0
7:4	RESERVED		R	0x0
3:0	AEWINCH	AE/AWB Engine Horizontal Sampling Point Increment Sets horizontal distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32. * This value is shadowed and latched on the rising edge of VSYNC.	RW	0x0

Table 8-1325. Register Call Summary for Register H3A_AEWSUBWIN

ISS ISP

- ISS ISP H3A Subsampler: [0] [1]
- ISS ISP H3A Additional Black Row of AE/AWB Windows: [2] [3]
- ISS ISP H3A Register Setup: [4] [5]
- ISS ISP H3A Register Accessibility During Frame Processing: [6]
- ISS ISP H3A Summary of Constraints: [7]
- ISS H3A Register Summary: [8]

Table 8-1326. H3A_AEWBUFST

Address Offset	0x0000 005C		
Physical Address	0x5201 145C	**Instance**	ISS_H3A
Description	SDRAM destination address for AE/AWB engine statistics		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AEWBUFST																													RESERVED		

Bits	Field Name	Description	Type	Reset
31:5	AEWBUFST	SDRAM destination address for AE/AWB engine statistics The start location in SDRAM for the AE/AWB statistics. The 6 LSB are ignored, address should be on a 64-byte boundary This field can be altered even when the AE/AWB is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.	RW	0x0000000
4:0	RESERVED		R	0x00

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Table 8-1327. Register Call Summary for Register H3A_AEWBUFST

ISS ISP

- ISS ISP H3A DMA Interface: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27]
- ISS ISP H3A Register Setup: [28]
- ISS ISP H3A Register Accessibility During Frame Processing: [29]
- ISS H3A Register Summary: [30]

Table 8-1328. H3A_AEWCFG

Address Offset	0x0000 0060		
Physical Address	0x5201 1460	**Instance**	ISS_H3A
Description	Configuration for AE/AWB		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						AEFMT		RESERVED				SUMSHFT			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:8	AEFMT	AE/AWB output format 0 = sum of squares 1 = min/max 2 = sum only; no sum of squares or min/max * This value is shadowed and latched on the rising edge of VSYNC	RW	0x0
7:4	RESERVED		R	0x0
3:0	SUMSHFT	AE/AWB engine shift value for the accumulation of pixel values This bit field sets the right shift value which is applied on the result of the pixel accumulation before it is stored in the packet. The accumulation takes place on 26 bits which is enough for 10-bit data and a maximum widow size of 512 x 512 which results into the accumulation of 256 x 256 pixels of the same color. The shift value must be set such that the result fits on 16 bits. SUMSHFT = right shift value. Range: 0 -15 * This value is shadowed and latched on the rising edge of VSYNC	RW	0x0

Table 8-1329. Register Call Summary for Register H3A_AEWCFG

ISS ISP

- ISS ISP H3A AE/AWB Engine: [0] [1] [2] [3]
- ISS ISP H3A AE/AWB Accumulators: [4]
- ISS ISP H3A DMA Interface: [5] [6] [7]
- ISS ISP H3A Register Setup: [8] [9]
- ISS ISP H3A Register Accessibility During Frame Processing: [10]
- ISS H3A Register Summary: [11]

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Table 8-1330. H3A_LINE_START

Address Offset	0x0000 0064		
Physical Address	0x5201 1464	**Instance**	ISS_H3A
Description	Line Framing Logic Register In certain cases the number of clock cycles between HD pulses will be greater than the line buffer included in the H3A module. The framing module prior to the line buffer enables to control the data which is input to the line buffer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLV																LINE_START															

Bits	Field Name	Description	Type	Reset
31:16	SLV	Start Line Vertical Specifies how many lines after the VD rising edge the real frame starts.	W	0x0000
15:0	LINE_START	Line Start The framing module uses the LINE_START bit field to find the position of the first pixel to place into the line buffer. Range: 0-65535	RW	0x0000

Table 8-1331. Register Call Summary for Register H3A_LINE_START

ISS ISP

- ISS ISP H3A Line Framing Logic: [0] [1] [2] [3]
- ISS ISP H3A Paxel Extraction: [4]
- ISS ISP H3A Register Setup: [5] [6] [7] [8]
- ISS H3A Register Summary: [9]

Table 8-1332. H3A_VFV_CFG1

Address Offset	0x0000 0068		
Physical Address	0x5201 1468	**Instance**	ISS_H3A
Description	Vertical focus value configuration 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCOEF1_3								VCOEF1_2								VCOEF1_1								VCOEF1_0							

Bits	Field Name	Description	Type	Reset
31:24	VCOEF1_3	Vertical FV FIR 1 coefficient 3	RW	0x00
23:16	VCOEF1_2	Vertical FV FIR 1 coefficient 2	RW	0x00
15:8	VCOEF1_1	Vertical FV FIR 1 coefficient 1	RW	0x00
7:0	VCOEF1_0	Vertical FV FIR 1 coefficient 0	RW	0x00

Table 8-1333. Register Call Summary for Register H3A_VFV_CFG1

ISS ISP

- ISS ISP H3A VFV Calculator: [0]
- ISS ISP H3A Register Setup: [1]
- ISS H3A Register Summary: [2]

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Table 8-1334. H3A_VFV_CFG2

Address Offset	0x0000 006C		
Physical Address	0x5201 146C	**Instance**	ISS_H3A
Description	Vertical focus value configuration 2.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTHR1																RESERVED								VCOEF1_4							

Bits	Field Name	Description	Type	Reset
31:16	VTHR1	Threshold for vertical FV FIR 1	RW	0x0000
15:8	RESERVED		R	0x00
7:0	VCOEF1_4	Vertical FV FIR 1 coefficient 4	RW	0x00

Table 8-1335. Register Call Summary for Register H3A_VFV_CFG2

ISS ISP

- ISS ISP H3A VFV Calculator: [0] [1]
- ISS ISP H3A VFV Accumulator: [2]
- ISS ISP H3A Register Setup: [3]
- ISS H3A Register Summary: [4]

Table 8-1336. H3A_VFV_CFG3

Address Offset	0x0000 0070		
Physical Address	0x5201 1470	**Instance**	ISS_H3A
Description	Vertical focus value configuration 4.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCOEF2_3								VCOEF2_2								VCOEF2_1								VCOEF2_0							

Bits	Field Name	Description	Type	Reset
31:24	VCOEF2_3	Vertical FV FIR 2 coefficient 3	RW	0x00
23:16	VCOEF2_2	Vertical FV FIR 2 coefficient 2	RW	0x00
15:8	VCOEF2_1	Vertical FV FIR 2 coefficient 1	RW	0x00
7:0	VCOEF2_0	Vertical FV FIR 2 coefficient 0	RW	0x00

Table 8-1337. Register Call Summary for Register H3A_VFV_CFG3

ISS ISP

- ISS ISP H3A VFV Calculator: [0]
- ISS ISP H3A Register Setup: [1]
- ISS H3A Register Summary: [2]

Table 8-1338. H3A_VFV_CFG4

Address Offset	0x0000 0074		
Physical Address	0x5201 1474	**Instance**	ISS_H3A
Description	Vertical focus value configuration 4.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTHR2																RESERVED								VCOEF2_4							

Bits	Field Name	Description	Type	Reset
31:16	VTHR2	Threshold for vertical FV FIR 2	RW	0x0000
15:8	RESERVED		R	0x00
7:0	VCOEF2_4	Vertical FV FIR 2 coefficient 4	RW	0x00

Table 8-1339. Register Call Summary for Register H3A_VFV_CFG4

ISS ISP
- ISS ISP H3A VFV Calculator: [0] [1]
- ISS ISP H3A VFV Accumulator: [2]
- ISS ISP H3A Register Setup: [3]
- ISS H3A Register Summary: [4]

Table 8-1340. H3A_HVF_THR

Address Offset	0x0000 0078		
Physical Address	0x5201 1478	**Instance**	ISS_H3A
Description	Horizontal Focus Value Threshold		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HTHR2																HTHR1															

Bits	Field Name	Description	Type	Reset
31:16	HTHR2	Threshold for horizontal FV IIR 2	RW	0x0000
15:0	HTHR1	Threshold for horizontal FV IIR 1	RW	0x0000

Table 8-1341. Register Call Summary for Register H3A_HVF_THR

ISS ISP
- ISS ISP H3A HFV Accumulator: [0] [1]
- ISS ISP H3A Register Setup: [2] [3]
- ISS H3A Register Summary: [4]

Table 8-1342. H3A_ADVANCED

Address Offset	0x0000 007C		
Physical Address	0x5201 147C	**Instance**	ISS_H3A
Description	Normal and Advanced AF stats collection mode		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																RESERVED															AF_MODE

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Bits	Field Name	Description	Type	Reset
31:15	ID	0x0: This bit field must be set to 0xCA00 to enable AF advanced mode.	RW	0x00000
14:1	RESERVED		R	0x0000
0	AF_MODE	AF engine mode. 0x0: Normal Mode 0x1: Advanced mode. H3A_ADVANCED.ID must be set to 0xCA00 to enable this functionality.	RW	0

Table 8-1343. Register Call Summary for Register H3A_ADVANCED

ISS ISP

- ISS ISP H3A Paxel Extraction: [0] [1]
- ISS H3A Register Summary: [2]
- ISS H3A Register Description: [3]

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8.4 ISS Still Image Coprocessor

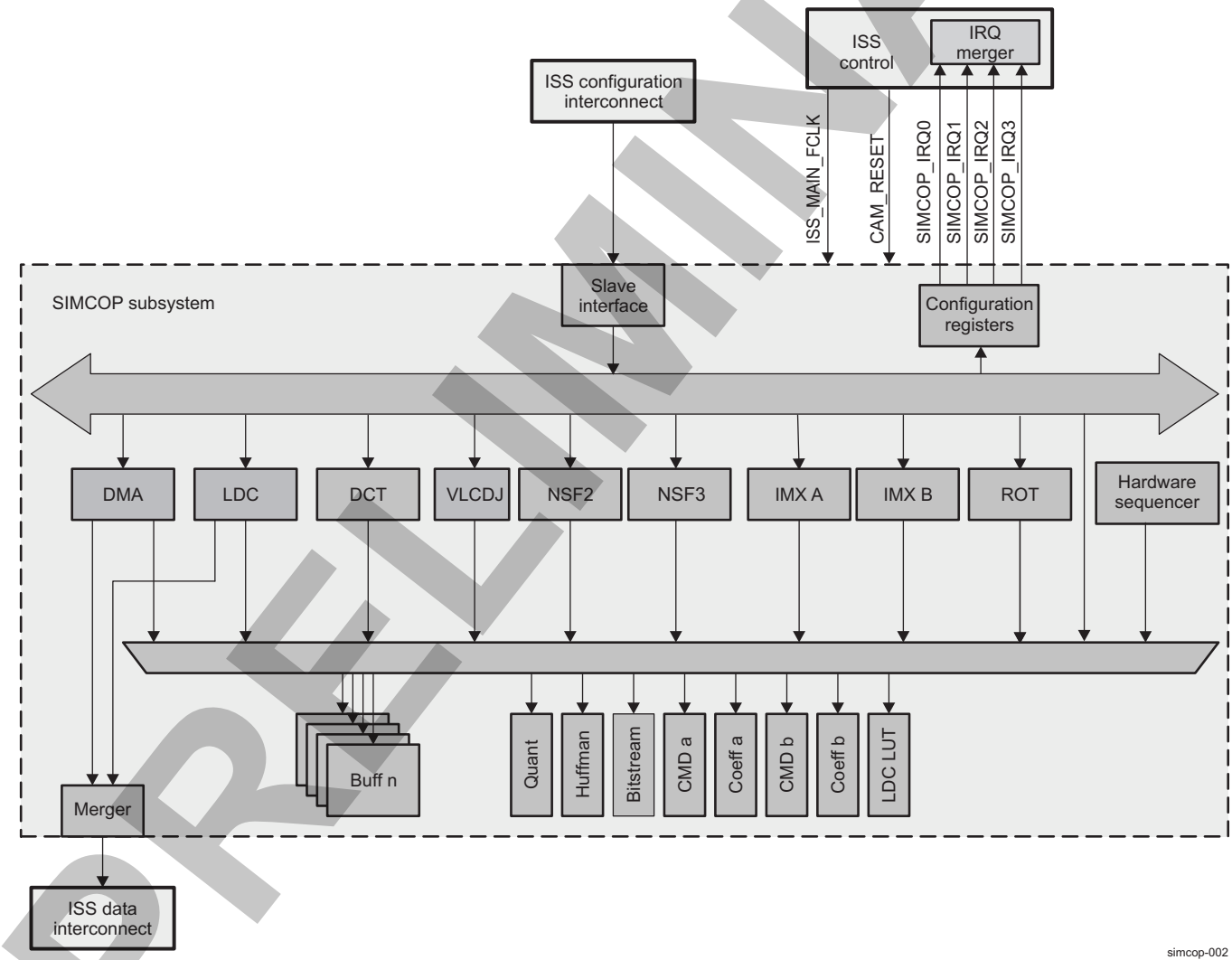
This section gives a high-level description of the ISS still iMage coprocessor (SIMCOP) in the device. For a high-level description of ISS level, see Section 8.1, *ISS:Overview*.

8.4.1 ISS SIMCOP Overview

The SIMCOP subsystem is designed to encode, decode, and process image data. SIMCOP is a macroblock-based memory-to-memory processing engine. It fetches macroblocks from system memory and stores them into local memories. Different accelerators take the fetched data, perform processing, and send the processing outcome back to local memories. From there the data could be further processed by other accelerators or sent back to system memory. The SIMCOP needs an external central processing unit (CPU) to perform high-level control tasks and configurations. SIMCOP is closely coupled to a CPU for that purpose.

Figure 8-256 shows a block diagram of the SIMCOP subsystem.

Figure 8-256. SIMCOP Subsystem Overview



The ISS SIMCOP subsystem consists of:

- Noise filter (NSF2 and NSF3) – For advanced noise filtering and an edge-enhancement
- Two image and video processing engines (IMXs) – Supplement various fixed-function processing blocks
- Variable-length coder/decoder for JPEG (VLCDJ) module – Handles quantization and variable length

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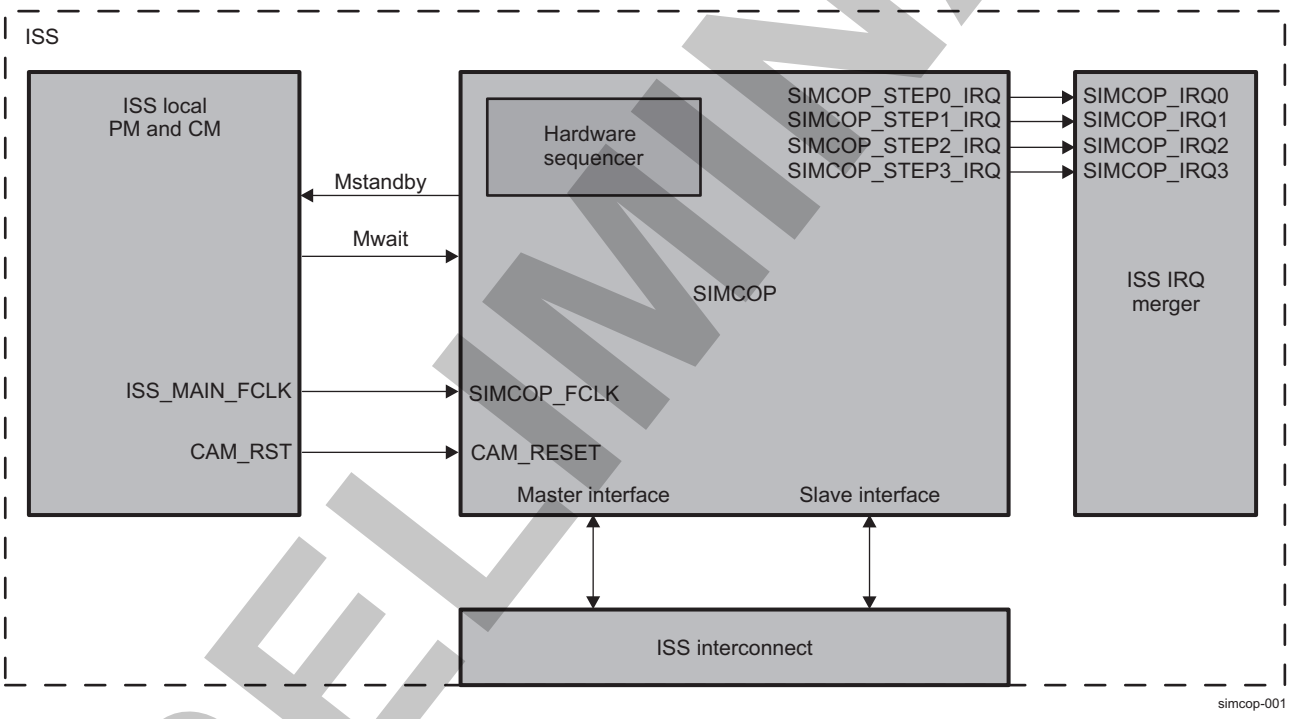
coding, decoding, and inverse quantization

- Discrete cosine transform (DCT) module – Implements method for transforming blocks of image during the compression flow.
- Lens distortion correction (LDC) module – Deals with lens geometric distortion issues in the camera subsystem
- Rotation accelerator (ROT) engine – Blocks data rotation and shifting from a SIMCOP local memory to another SIMCOP local memory
- Hardware sequencer and buffers – Controls SIMCOP modules and buffers to offload an external processor to perform low-level sequencing tasks
- Direct memory access (DMA) controller – Data transfers from SIMCOP memories to system memory or from system memory to SIMCOP memories

8.4.1.1 ISS SIMCOP Integration

The SIMCOP subsystem is connected to the rest of the system through the ISS local interconnect. Figure 8-257 shows the integration of the SIMCOP subsystem in the ISS.

Figure 8-257. SIMCOP Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1, *Clock Management* in Section 3.1.1 , *Power, Reset, and Clock Management*.

This section gives an overview of typical uses of the module. See Section 3.1.1, *Power, Reset, and Clock Management* for more information and settings of the PRCM relationship to ISS clocks and resets.

Table 8-1344 lists the Integration Attributes.

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Table 8-1344. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
SIMCOP	PD_CAM	

Table 8-1345 lists the Clocks and Resets values.

Table 8-1345. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SIMCOP	SIMCOP_FCLK	ISS_MAIN_FCLK	PRCM	Functional clock provided by CORE_ISS_MAIN_CLK from the PRCM. It is used by all ISS submodules and ISS top-level resources.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SIMCOP	CAM_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

Table 8-1346 lists the hardware resets.

Table 8-1346. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
SIMCOP	SIMCOP_STEP0_IRQ	SIMCOP_IRQ0	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
SIMCOP	SIMCOP_STEP1_IRQ	SIMCOP_IRQ1	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
SIMCOP	SIMCOP_STEP2_IRQ	SIMCOP_IRQ2	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
SIMCOP	SIMCOP_STEP3_IRQ	SIMCOP_IRQ3	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer

For more information about interrupt requests, see Section 8.1.2.1.1*Interrupt Merger*.

8.4.1.2 ISS SIMCOP Functional Description

8.4.1.2.1 ISS SIMCOP Local Power and Clock Management

8.4.1.2.1.1 ISS SIMCOP Local Clock Management

The ISS has five asynchronous clock domains. The SIMCOP belongs to the ISS_PCLK clock domain.

A clock-enable signal provided externally is used. Multiple subdomains exist internally to reduce dynamic power consumption. This feature does not require intervention by the PRCM module. For high-level description of the SIMCOP clock domain and configuration inside ISS, see Section 8.1.1.1.1, *ISS Clock Domains* and , *ISS Clocks*.

Moreover, at high level the functional clock of ISS SIMCOP submodules can be cut by software to reduce power consumption by cutting off or turning on the modules from the SIMCOP_CLKCTRL register (see Table 8-1347).

For software to enable a submodule:

- Software sets the appropriate bit in the SIMCOP_CLKCTRL register.
- Hardware enables the submodule functional and interface clocks.
- Hardware connects the configuration port of the submodule to the coprocessor bus.

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- Hardware sets the appropriate bit in the SIMCOP_CLKCTRL register. Software must check if this bit is set before accessing the submodule.

Table 8-1347 shows the ISS SIMCOP clock control register settings.

Table 8-1347. ISS SIMCOP Clock Control Register Settings

Module Name	Bit Field Name	Description
NSF3	SIMCOP_CLKCTRL[9] NSF3	Writing 0x1 enables the module
ROT	SIMCOP_CLKCTRL[7] ROT_A	Writing 0x1 enables the module
IMX_B	SIMCOP_CLKCTRL[6] IMX_B	Writing 0x1 enables the module
IMX_A	SIMCOP_CLKCTRL[5] IMX_A	Writing 0x1 enables the module
NSF2	SIMCOP_CLKCTRL[4] NSF2	Writing 0x1 enables the module
VLCDJ	SIMCOP_CLKCTRL[3] VLCDJ	Writing 0x1 enables the module
DCT	SIMCOP_CLKCTRL[2] DCT	Writing 0x1 enables the module
LDC	SIMCOP_CLKCTRL[1] LDC	Writing 0x1 enables the module
DMA	SIMCOP_CLKCTRL[0] DMA	Writing 0x1 enables the module

For software to shut down a submodule:

- Software ensures that the submodule is idle. Mainly:
  - The submodule must not generate new events.
  - The submodule must not have any pending events.
  - For initiators, the submodule must stop interconnect transaction generation.
- Software clears the appropriate bit in the SIMCOP_CLKCTRL register.
- Hardware disconnects the configuration port of the module from the coprocessor bus, no more accesses are routed to the submodule. Ongoing transactions are finished (hardware stays in this state as long as required).
- For initiators, hardware waits until there are no more outstanding transactions:
  - The SIMCOP DMA provides an MStandBy signal used for that purpose.
  - The LDC does not provide this information. Software must ensure that LDC is idle. SIMCOP hardware ensures that the internal MTC2OCP bridges have no outstanding transactions.
- Hardware cuts the submodules clock.
- Hardware clears the appropriate SIMCOP_CLKCTRL registers.

SIMCOP submodules support autogating. They can gate their functional and interface clock internally based on functional requirements. This feature can be disabled for debug or power consumption measurement purposes.

8.4.1.2.1.2 Local Clock Autogating

The SIMCOP subsystem modules support autogating. They can gate their functional and interface clock internally based on functional requirements. This feature can be disabled. Table 8-1348 summarizes what modules support autogating control and which control bit is used.

Table 8-1348. Autoclock Gating Bit Control

SIMCOP resource	Autogating override
SIMCOP top-level resources	NA
SIMCOP DMA	NA
LDC	NA
DCT	DCT_CFG[5] AUTOGATING
VLCDJ	VLCDJ_CTRL[3] AUTOGATING
NSF2	NA
NSF3	NA

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Table 8-1348. Autoclock Gating Bit Control (continued)

SIMCOP resource	Autogating override
IMX A	IMXa.IMX_CLKCNTRL[0] CLKCNTRL
IMX B	IMXb.IMX_CLKCNTRL[0] CLKCNTRL
ROT	ROT_CFG[9] AUTOGATING

8.4.1.2.1.3 ISS SIMCOP Power Management

The SIMCOP supports the STANDBY power management protocol. It is used by the SIMCOP to indicate when it has no more interconnect transactions to perform. This information is used at the ISS level to control the SIMCOP and ISS shut-down sequence. The SIMCOP does not have any internal wake-up events. DISCONNECT and IDLE protocols are not supported.

The typical SIMCOP shut-down sequence is:

- Software disables all SIMCOP submodules. This ensures the SIMCOP does not:
  - Generate any traffic on its master port; SIMCOP asserts the MStandby signal.
  - Generate new events (IRQs).
- Software clears all pending events at the SIMCOP level; all interrupt lines become inactive.
- Software initiates the SIMCOP shut-down sequence by writing the appropriate bit at the ISS level.
- ISS hardware:
  - Disconnects the SIMCOP configuration port. Any access attempts to the SIMCOP are blocked at the ISS level. The DISCONNECT protocol is handled at the ISS level; the SIMCOP does not provide any handshake signals to support it.
  - Waits until MStandby from SIMCOP is asserted (always true in a normal case because SIMCOP submodules are inactive)
  - Asserts the SWait input of SIMCOP
  - Cuts the SIMCOP clock

The typical SIMCOP enable sequence is:

- Software initiates the SIMCOP enable sequence by writing the appropriate bit at the ISS level.
- ISS hardware:
  - Enables the SIMCOP clock
  - Deasserts the SWait input of SIMCOP
  - Connects the SIMCOP configuration port

Three modes for MStandBy control are supported. The mode is selected using the SIMCOP_HL_SYSCONFIG[5:4] STANDBYMODE register.

- Smart-standby: This is the normal mode to be used. When in this mode, SIMCOP asserts the MStandBy signal when the MStandBy output of SIMCOP DMA is asserted, the LDC module is effectively disabled (SIMCOP_CLKCTRL[1] LDC = 0), and the MTCR2OCP bridge and the merger have no more outstanding transactions.
- Force-standby: This is a backup mode intended to be used only if smart-idle mode is bugged. When in this mode, SIMCOP asserts MStandBy unconditionally. Software must ensure that the SIMCOP is in a correct quiet state before programming this mode.
- No-standby: This is a backup mode intended to be used only if smart-idle mode is bugged. When in this mode, SIMCOP never asserts the MStandBy signal.

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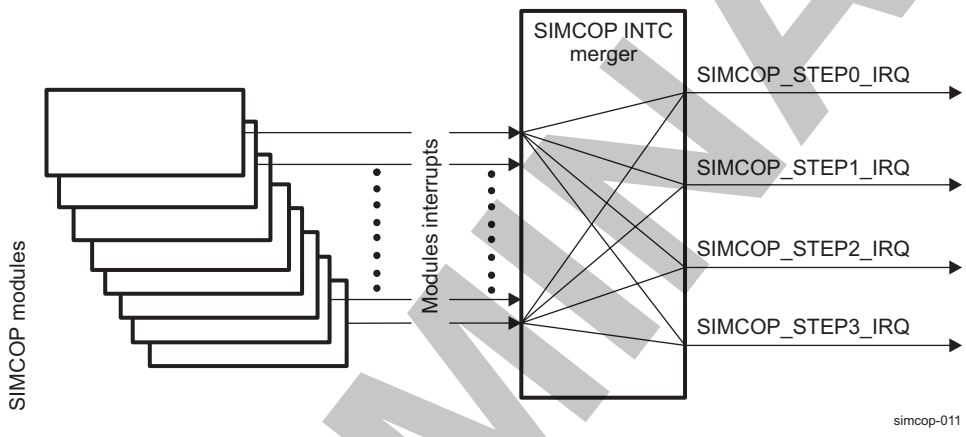
8.4.1.2.2 Software Reset

Software reset is intended to return the SIMCOP into a known state without requiring a complete device reset. A software reset at the SIMCOP level is seen as a hardware reset for SIMCOP submodules. To perform a software reset, set the SIMCOP_HL_SYSCONFIG[0] SOFTRESET bit to 1. The SIMCOP_HL_SYSCONFIG[0] SOFTRESET bit indicates that the software reset is ongoing when its value is 1. When the software reset completes, the SIMCOP_HL_SYSCONFIG[1] SOFTRESET bit is automatically reset. The software must ensure that the software reset completes before configuring hardware sequencer or buffers.

8.4.1.2.3 Interrupt Merger

SIMCOP interrupts are merged at the SIMCOP subsystem level into four interrupts as shown in Figure 8-258.

Figure 8-258. SIMCOP Interrupt Merger Overview



These four outputs interrupts can be configured using the SIMCOP_HL_IRQENABLE_SET_i and SIMCOP_HL_IRQENABLE_CLR_i (i = 0 to 3, corresponding to output interrupt) to enable or disable interrupt mask for each interrupt output. Software can poll the value of interrupt before masking SIMCOP_HL_IRQSTATUS_RAW_i and after masking SIMCOP_HL_IRQSTATUS_i.

Software can configure how outputs interrupts are generated by using the SIMCOP_CTRL[i] IRQi_MODE (i = 0 to 3) bit field(s):

- 0x0: OR – The interrupt is asserted when one of the selected events has occurred
- 0x1: AND – The interrupt is asserted when all selected events have occurred

Table 8-1349 shows how interrupts are mapped on the SIMCOP_HL_IRQSTATUS_RAW_i, SIMCOP_HL_IRQSTATUS_i, SIMCOP_HL_IRQENABLE_SET_i and SIMCOP_HL_IRQENABLE_CLR_i registers.

Table 8-1349. SIMCOP Interrupts

Bit	Name	Description
0	SIMCOP_DMA_IRQ0	Interrupt triggered by SIMCOP DMA
1	LDC_FRAME_IRQ	A full frame has been processed by LDC2 module
2	DCT_IRQ	DCT operation has been completed (configured number of MCUs for YUV4:2:0/YUV4:2:2 mode, or number of blocks for sequential block mode)
3	VLCDJ_BLOCK_IRQ	A macroblock has been processed (encode/decode)
4	NSF_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done.
5	IMX_A_IRQ	Event triggered when IMX has executed a SLEEP instruction.
6	IMX_B_IRQ	
7	ROT_A_IRQ	Event triggered by the ROT engine.
8	NSF3_IRQ	Event triggered by the NSF3 imaging accelerator when processing of a block is done.
9	LDC_BLOCK_IRQ	A macroblock has been processed by LDC2 module

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Table 8-1349. SIMCOP Interrupts (continued)

Bit	Name	Description
10	SIMCOP_STEP0_IRQ	Event triggered when a SIMCOP context is activated by the HW sequencer
11	SIMCOP_STEP1_IRQ	
12	SIMCOP_STEP2_IRQ	
13	SIMCOP_STEP3_IRQ	
14	DONE_IRQ	Event triggered when the HW sequencer finishes the sequence: - the sequence step counter has reached the limit - All accelerator and DMA events for the last sequence step have been received.
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port on L3 interconnect.
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. This event shall not trigger in a normal use case.
18	SIMCOP_DMA_IRQ1	Interrupt triggered by SIMCOP DMA
19	CPU_PROC_START_IRQ	This interrupt is used when CPU data processing is used in a macroblock processing pipeline. When CPU receives this IRQ, data for ready to be processed. When CPU is done with processing it acknowledges by setting the SIMCOP_HWSEQ_CTRL.CPU_PROC_DONE bit. The interrupt is cleared as usual.

8.4.1.2.4 ISS SIMCOP Modules Description

This section provides links to each subchapter for each submodule in the ISS SIMCOP module.

The ISS module provides a unique ISS_MAIN_FCLK for all the submodules inside the SIMCOP, see Section 8.4.1.2.1.1.

For information about hardware and software resets for each module, see Table 8-1349.

For interrupt request information for each module, see Table 8-1346.

The ISS SIMCOP consists of the following submodules:

- Hardware Sequencer and buffers, for more information, see Section 8.4.2.
- DMA, for more information, see Section 8.4.3.
- ROT, for more information, see Section 8.4.7.
- IMX, for detailed information about the IMX modules, contact your TI representative.
- NSF2, for detailed information about the NSF2 modules, contact your TI representative.
- NSF3, for detailed information about the NSF3 modules, contact your TI representative.
- VLCDJ, for more information please see Section 8.4.6
- DCT, for more information, see Section 8.4.5
- LDC, for more information, see Section 8.4.4

8.4.1.3 ISS SIMCOP Programming Models

8.4.1.3.1 Global Initialization

8.4.1.3.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the ISS SIMCOP module is to be used for the first time after a device reset. This initialization of the surrounding modules is based on the integration of the ISS SIMCOP.

Table 8-1350. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
ISS local PM and CM	Module interface and functional clocks must be enabled. For more information, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

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8.4.1.3.1.2 ISS SIMCOP Module Global Initialization

This procedure initializes the ISS SIMCOP module after a power-on or software reset.

Table 8-1351. ISS SIMCOP Global Initialization

Step	Register/ Bitfield / Programming Model	Value
Execute software reset	SIMCOP_HL_SYSCONFIG[0] SOFTRESET	0x1
Wait until reset completed?	SIMCOP_HL_SYSCONFIG[0] SOFTRESET	0x0
Configure standby mode	SIMCOP_HL_SYSCONFIG[5:4] STANDBYMODE	0x2
Configure submodules interface and functional clock	SIMCOP_CLKCTRL[7:0]	xxx
Interrupt configuration		
Set interrupt enable bit for the submodules	SIMCOP_HL_IRQENABLE_SET_i[7:0]	xxx

8.4.1.3.2 ISS SIMCOP Operational Modes Configuration

8.4.1.3.2.1 Interrupts

To unmask an interrupt for generation of the SIMCOP_IRQi output interrupts, software must set the corresponding bit of the SIMCOP_HL_IRQENABLE_SET_i (i = 0 to 3) register to 1.

Example 1:

SIMCOP_IRQ1 is generated when DCT_IRQ or VLCDJ_BLOCK_IRQ are generated:

- SIMCOP_HL_IRQENABLE_SET_i[2] DCT_IRQ = 0x1 (i = 1)
- SIMCOP_HL_IRQENABLE_SET_i[3] VLCDJ_BLOCK_IRQ = 0x1 (i = 1)
- SIMCOP_CTRL[1] IRQ1_MODE = 0x0

Example 2:

SIMCOP_IRQ3 is generated when IMX_A_IRQ and LDC_BLOCK_IRQ are generated:

- SIMCOP_HL_IRQENABLE_SET_i[5] IMX_A_IRQ = 0x1 (i = 3)
- SIMCOP_HL_IRQENABLE_SET_i[9] LDC_BLOCK_IRQ = 0x1 (i = 3)
- SIMCOP_CTRL[3] IRQ3_MODE = 0x1

To mask an interrupt for generation of the SIMCOP_IRQi output interrupts, software must clear the corresponding bit of the SIMCOP_HL_IRQENABLE_CLEAR_i (i = 0 to 3) register by setting it to 0.

When an event occurs, the corresponding bit in the SIMCOP_HL_IRQSTATUS_RAW_i (i = 0 to 3) register is set regardless of whether or not the event has been enabled. Bits in the SIMCOP_HL_IRQSTATUS_i (i = 0 to 3) registers are only set when an enabled event occurs. Software can clear a pending event by setting the appropriate bit in the SIMCOP_HL_IRQSTATUS_i (i = 0 to 3) register.

8.4.1.3.2.2 JPEG Encode Operational Mode Configuration

Figure 8-259 shows a typical JPEG encode macroblock pipeline.

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Figure 8-259. JPEG Encode Pipeline

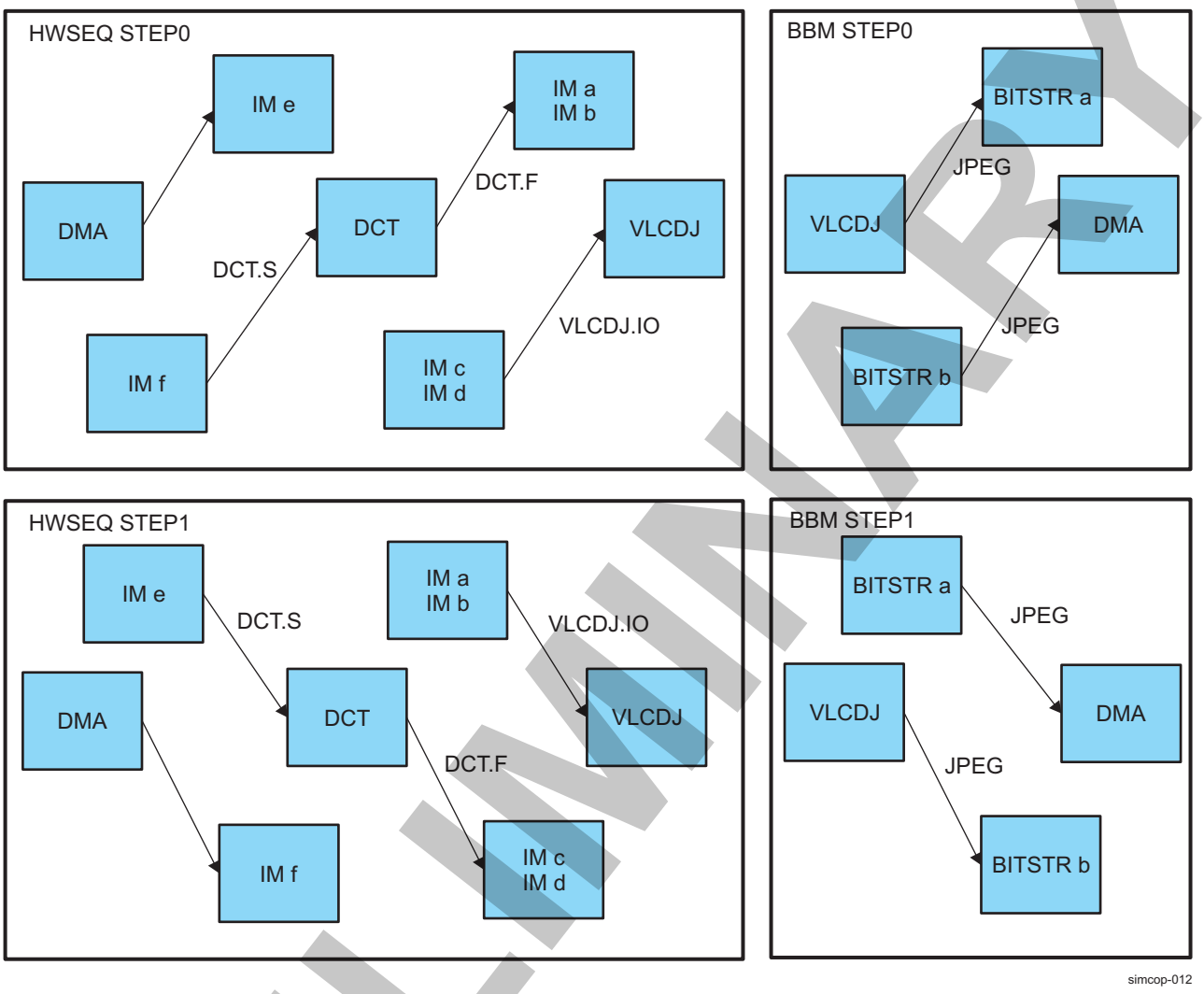

Table 8-1352. JPEG encode pipeline

Step	Register/ Bitfield / Programming Model	Value
Set SIMCOP DMA to fetch data from SDRAM and stored into an image buffer (IM e or IM f)	See DMA programming model, Section 8.4.3.4	xxx
Set DCT to reads data from an image buffer (IM E or IM F)	DCT_SPTR[12:5] ADDR	xxx
Set DCT to store data into sets of two image buffers (IM a + IM b or IM c+ IM d)	DCT_FPTR[12:4] ADDR	xxx
Set VLCDJ to read data from image buffers	See VLCDJ programming model, Section 8.4.6.4	xxx
Set VLCDJ to write the data to the BITSTREAM buffer	See VLCDJ programming model, Section 8.4.6.4	xxx
Set the SIMCOP DMA to send the data to SDRAM	See DMA programming model, Section 8.4.3.4	xxx

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8.4.1.4 ISS SIMCOP Registers Manual

8.4.1.4.1 SIMCOP Instance Summary

Table 8-1353 summarizes the SIMCOP instance.

Table 8-1353. SIMCOP Instance Summary

Module Name	L3_MAIN Base Address	IPU Base Address	Size
SIMCOP	0x5202 0000	0x5506 0000	256Bytes

8.4.1.4.2 SIMCOP Registers

8.4.1.4.2.1 SIMCOP Register Summary

Table 8-1354 is the SIMCOP register mapping summary. through describe the registers in detail.

Table 8-1354. SIMCOP Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address	IPU Physical Address
SIMCOP_HL_REVISION	R	32	0x0000 0000	0x5202 0000	0x5506 0000
SIMCOP_HL_HWINFO	R	32	0x0000 0004	0x5202 0004	0x5506 0004
SIMCOP_HL_SYSCONFIG	RW	32	0x0000 0010	0x5202 0010	0x5506 0010
RESERVED	RW	32	0x0000 001C	0x5202 001C	0x5506 001C
SIMCOP_HL_IRQSTATUS_RAW_i	RW	32	0x0000 0020 + (0x10 * I)	0x5202 0020 + (0x10 * I)	0x5506 0020 + (0x10 * I)
SIMCOP_HL_IRQSTATUS_i (1)	RW	32	0x0000 0024 + (0x10 * I)	0x5202 0024 + (0x10 * I)	0x5506 0024 + (0x10 * I)
SIMCOP_HL_IRQENABLE_SET_i (1)	RW	32	0x0000 0028 + (0x10 * I)	0x5202 0028 + (0x10 * I)	0x5506 0028 + (0x10 * I)
SIMCOP_HL_IRQENABLE_CLR_i (1)	RW	32	0x0000 002C + (0x10 * I)	0x5202 002C + (0x10 * I)	0x5506 002C + (0x10 * I)
SIMCOP_CTRL	RW	32	0x0000 0060	0x5202 0060	0x5506 0060
SIMCOP_CLKCTRL	RW	32	0x0000 0064	0x5202 0064	0x5506 0064
SIMCOP_CTRL2	RW	32	0x0000 00FC	0x5202 00FC	0x5506 00FC

(1) I = 0 to 3

8.4.1.4.2.2 SIMCOP_CONTROL Register Description

Table 8-1355. SIMCOP_HL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5202 0000 0x5506 0000	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	MODULE REVISION This register contains the IP revision code in binary coded digital. For example, we have: 0x01 = revision 0.1 and 0x21 = revision 2.1		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

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Bits	Field Name	Description	Type	Reset
31:0	REV	Revision ID	R	-[1]

[1] TI internal data

Table 8-1356. Register Call Summary for Register SIMCOP_HL_REVISION

ISS SIMCOP Overview

- SIMCOP Register Summary: [0]

Table 8-1357. SIMCOP_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5202 0004 0x5506 0004	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	Information about the IP module's hardware configuration. It provides information about the generic parameters.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LDCIMXNSF_BOOST		RY22_LDCMEM		LDCR_RESP_FIFO			IMAGE_BUFFERS								
																								NSF3_ENABLE	ROT_A_ENABLE	IMX_B_ENABLE	IMX_A_ENABLE	NSF_ENABLE	VLCDJ_ENABLE	DCT_ENABLE	LDC_ENABLE

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Read returns 0.	R	0x00000
15:14	LDCIMXNSF_BOOST	Read 0x2: SIMCOP receives a main clock at 304 MHz plus a clock at 426 MHz for NSF and iMX Read 0x1: SIMCOP receives a 400-Mhz clock. Some modules receive the 400-MHz clock and others receive 200MHz. Read 0x0: SIMCOP receives 200-MHz clock.	R	0x2
13	RY22_LDCMEM	Chooses the LDC working memory configuration Read 0x1: Working memory only populated for YUV4:2:0 operation Read 0x0: Working memory fully populated. Supports YUV4:2:2 operation	R	0x0
12:10	LDCR_RESP_FIFO	Defines the size of the LDC read master response FIFO in words of 128-bits. Read 0x2: 8x128 bits Read 0x3: 16x128 bits Read 0x4: 32x128 bits Read 0x5: 64x128 bits Read 0x6: 128x128 bits Read 0x7: 256x256 bits	R	0x4
9:8	IMAGE_BUFFERS	This parameter defines the image buffer count. Read 0x0: 4 Image buffers (e, f, g, and h) Read 0x1: 8 Image buffers	R	0x1
7	NSF3_ENABLE	The NSF3 module is present when this parameter is set Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1

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Bits	Field Name	Description	Type	Reset
6	ROT_A_ENABLE	The ROT A module is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
5	IMX_B_ENABLE	The IMX B module and the CMD b, COEFF b memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
4	IMX_A_ENABLE	The IMX A module and the CMD a, COEFF a memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
3	NSF_ENABLE	The NSF2 module is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
2	VLCDJ_ENABLE	The VLCD module and the QUANT, HUFFMAN, BITSTREAM memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
1	DCT_ENABLE	The DCT module is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
0	LDC_ENABLE	The LDC module and the LDC LUT are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1

Table 8-1358. Register Call Summary for Register SIMCOP_HL_HWINFO

ISS SIMCOP Overview

- SIMCOP Register Summary: [0]

Table 8-1359. SIMCOP_HL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5202 0010 0x5506 0010	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	This register controls the various parameters of the OCP interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		RESERVED			SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Read returns 0.	R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, i.e. the module's functional requirement from the initiator.	RW	0x0
3:1	RESERVED	Read returns 0.	R	0x0
0	SOFTRESET	Software reset Read 0x0: Reset done, no pending action Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing	RW	0

Table 8-1360. Register Call Summary for Register SIMCOP_HL_SYSCONFIG

ISS SIMCOP Overview

- ISS SIMCOP Power Management: [0]
- Software Reset: [1] [2] [3]
- ISS SIMCOP Module Global Initialization: [4] [5] [6]
- SIMCOP Register Summary: [7]

Table 8-1361. SIMCOP_HL_IRQSTATUS_RAW_i

Address Offset	0x0000 0020 + (0x10 * i)		
Physical Address	0x5202 0020 + (0x10 * I) 0x5506 0020 + (0x10 * I)	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	Per-event raw interrupt status vector Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CPU_PROC_START_IRQ	SIMCOP_DMA_IRQ1	LDC2BRIDGE_ERR_IRQ	ICNT_ERR_IRQ	VLCDJ_DECODE_ERR_IRQ	DONE_IRQ	STEP3_IRQ	STEP2_IRQ	STEP1_IRQ	STEP0_IRQ	LDC_BLOCK_IRQ	NSF3_IRQ	ROT_A	IMX_B_IRQ	IMX_A_IRQ	NSF_IRQ_IRQ	VLCDJ_BLOC_IRQ	DCT_IRQ	LDC_FRAME_IRQ	SIMCOP_DMA_IRQ0

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19	CPU_PROC_START_IRQ	Event triggered by the HW sequencer to instruct the CPU to process a macroblock Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
18	SIMCOP_DMA_IRQ1	Event triggered by the SIMCOP DMA. This event is automatically cleared at SIMCOP level when it is cleared at SIMCOP DMA level Check SIMCOP DMA IRQ registers. Read 0x0: No event pending Read 0x1: Event pending	R	0
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
14	DONE_IRQ	Event triggered when the HW sequencer finishes the sequence: - the sequence step counter has reached the limit - all accelerator and DMA events for the last sequence step have been received. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
13	STEP3_IRQ	Event triggered when STEP3 is activated by the HW sequencer Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
12	STEP2_IRQ	Event triggered when STEP2 is activated by the HW sequencer Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
11	STEP1_IRQ	Event triggered when STEP1 is activated by the HW sequencer Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
10	STEP0_IRQ	Event triggered when STEP0 is activated by the HW sequencer Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
9	LDC_BLOCK_IRQ	This event is triggered by LDC when a macroblock has been processed Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
8	NSF3_IRQ	Event triggered by NSF3 imaging accelerator when processing of a block is done Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
7	ROT_A	Event triggered by the ROT A engine Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
6	IMX_B_IRQ	Event triggered when IMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
5	IMX_A_IRQ	Event triggered when IMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
4	NSF_IRQ_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
3	VLCDJ_BLOC_IRQ	This event is triggered by VLCDJ when a macro-bloc has been processed (encode/decode) Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
2	DCT_IRQ	Event triggered when a block has been processed by the DCT module and the filter outcome has been stored to an image buffer. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
1	LDC_FRAME_IRQ	This event is triggered by LDC when a full frame has been processed Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
0	SIMCOP_DMA_IRQ0	Event triggered by the SIMCOP DMA. This event is automatically cleared at SIMCOP level when it is cleared at SIMCOP DMA level Check SIMCOP DMA IRQ registers. Read 0x0: No event pending Read 0x1: Event pending	R	0

Table 8-1362. Register Call Summary for Register SIMCOP_HL_IRQSTATUS_RAW_i

ISS SIMCOP Overview

- Interrupt Merger: [0] [1]
- Interrupts: [2]
- SIMCOP Register Summary: [3]

Table 8-1363. SIMCOP_HL_IRQSTATUS_i

Address Offset	0x0000 0024 + (0x10 * i)		
Physical Address	0x5202 0024 + (0x10 * I) 0x5506 0024 + (0x10 * I)	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	Per-event "enabled" interrupt status vector Enabled status isn't set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CPU_PROC_START_IRQ	SIMCOP_DMA_IRQ1	LDC2BRIDGE_ERR_IRQ	ICNT_ERR_IRQ	VLCDJ_DECODE_ERR_IRQ	DONE_IRQ	STEP3_IRQ	STEP2_IRQ	STEP1_IRQ	STEP0_IRQ	LDC_BLOCK_IRQ	NSF3_IRQ	ROT_A	IMX_B_IRQ	IMX_A_IRQ	NSF_IRQ_IRQ	VLCDJ_BLOC_IRQ	DCT_IRQ	LDC_FRAME_IRQ	SIMCOP_DMA_IRQ0

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19	CPU_PROC_START_IRQ	Event triggered by the HW sequencer to instruct the CPU to process a macroblock Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
18	SIMCOP_DMA_IRQ1	Event triggered by the SIMCOP DMA. This event is automatically cleared at SIMCOP level when it is cleared at SIMCOP DMA level Check SIMCOP DMA IRQ registers. Read 0x0: No (enabled) event pending Read 0x1: Event pending	R	0
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
14	DONE_IRQ	Event triggered when the HW sequencer finishes the sequence: - the sequence step counter has reached the limit - all accelerator and DMA events for the last sequence step have been received. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
13	STEP3_IRQ	Event triggered when STEP3 is activated by the HW sequencer Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
12	STEP2_IRQ	Event triggered when STEP2 is activated by the HW sequencer Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
11	STEP1_IRQ	Event triggered when STEP1 is activated by the HW sequencer Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
10	STEP0_IRQ	Event triggered when STEP0 is activated by the HW sequencer Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
9	LDC_BLOCK_IRQ	This event is triggered by LDC when a macroblock has been processed Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
8	NSF3_IRQ	Event triggered by the NSF3 imaging accelerator when processing of a block is done Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
7	ROT_A	Event triggered by the ROT A engine Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
6	IMX_B_IRQ	Event triggered when IMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
5	IMX_A_IRQ	Event triggered when IMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
4	NSF_IRQ_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
3	VLCDJ_BLOC_IRQ	This event is triggered by VLCDJ when a macro-bloc has been processed (encode/decode) Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
2	DCT_IRQ	Event triggered when a block has been processed by the DCT module and the filter outcome has been stored to an image buffer. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
1	LDC_FRAME_IRQ	This event is triggered by LDC when a full frame has been processed Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
0	SIMCOP_DMA_IRQ0	Event triggered by the SIMCOP DMA. This event is automatically cleared at SIMCOP level when it is cleared at SIMCOP DMA level Check SIMCOP DMA IRQ registers. Read 0x0: No (enabled) event pending Read 0x1: Event pending	R	0

Table 8-1364. Register Call Summary for Register SIMCOP_HL_IRQSTATUS_i

ISS SIMCOP Overview

- Interrupt Merger: [0] [1]
- Interrupts: [2] [3]
- SIMCOP Register Summary: [4]

Table 8-1365. SIMCOP_HL_IRQENABLE_SET_i

Address Offset	0x0000 0028 + (0x10 * i)		
Physical Address	0x5202 0028 + (0x10 * I) 0x5506 0028 + (0x10 * I)	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	Per-event interrupt enable bit vector Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CPU_PROC_START_IRQ	SIMCOP_DMA_IRQ1	LDC2BRIDGE_ERR_IRQ	ICNT_ERR_IRQ	VLCDJ_DECODE_ERR_IRQ	DONE_IRQ	STEP3_IRQ	STEP2_IRQ	STEP1_IRQ	STEP0_IRQ	LDC_BLOCK_IRQ	NSF3_IRQ	ROT_A	IMX_B_IRQ	IMX_A_IRQ	NSF_IRQ_IRQ	VLCDJ_BLOC_IRQ	DCT_IRQ	LDC_FRAME_IRQ	SIMCOP_DMA_IRQ0

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19	CPU_PROC_START_IRQ	Event triggered by the HW sequencer to instruct the CPU to process a macroblock Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
18	SIMCOP_DMA_IRQ1	Event triggered by the SIMCOP DMA. Check SIMCOP DMA IRQ registers. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
14	DONE_IRQ	Event triggered when the HW sequencer finishes the sequence: - the sequence step counter has reached the limit - all accelerator and DMA events for the last sequence step have been received. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
13	STEP3_IRQ	Event triggered when STEP3 is activated by the HW sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
12	STEP2_IRQ	Event triggered when STEP2 is activated by the HW sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
11	STEP1_IRQ	Event triggered when STEP1 is activated by the HW sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
10	STEP0_IRQ	Event triggered when STEP0 is activated by the HW sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
9	LDC_BLOCK_IRQ	This event is triggered by LDC when a macroblock has been processed Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
8	NSF3_IRQ	Event triggered by the NSF3 imaging accelerator when processing of a block is done Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
7	ROT_A	Event triggered by the ROT A engine Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
6	IMX_B_IRQ	Event triggered when IMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
5	IMX_A_IRQ	Event triggered when IMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
4	NSF_IRQ_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
3	VLCDJ_BLOC_IRQ	This event is triggered by VLCDJ when a macro-bloc has been processed (encode/decode) Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
2	DCT_IRQ	Event triggered when a block has been processed by the DCT module and the filter outcome has been stored to an image buffer. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
1	LDC_FRAME_IRQ	This event is triggered by LDC when a full frame has been processed Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
0	SIMCOP_DMA_IRQ0	Event triggered by the SIMCOP DMA. Check SIMCOP DMA IRQ registers. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

Table 8-1366. Register Call Summary for Register SIMCOP_HL_IRQENABLE_SET_i

ISS SIMCOP Overview

- Interrupt Merger: [0] [1]
- ISS SIMCOP Module Global Initialization: [2]
- Interrupts: [3] [4] [5] [6] [7]
- SIMCOP Register Summary: [8]

Table 8-1367. SIMCOP_HL_IRQENABLE_CLR_i

Address Offset	0x0000 002C + (0x10 * i)		
Physical Address	0x5202 002C + (0x10 * I) 0x5506 002C + (0x10 * I)	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	Per-event interrupt enable bit vector Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CPU_PROC_START_IRQ	SIMCOP_DMA_IRQ1	LDC2BRIDGE_ERR_IRQ	ICNT_ERR_IRQ	VLCDJ_DECODE_ERR_IRQ	DONE_IRQ	STEP3_IRQ	STEP2_IRQ	STEP1_IRQ	STEP0_IRQ	LDC_BLOCK_IRQ	NSF3_IRQ	ROT_A	IMX_B_IRQ	IMX_A_IRQ	NSF_IRQ_IRQ	VLCDJ_BLOC_IRQ	DCT_IRQ	LDC_FRAME_IRQ	SIMCOP_DMA_IRQ0

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Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19	CPU_PROC_START_IRQ	Event triggered by the HW sequencer to instruct the CPU to process a macroblock Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
18	SIMCOP_DMA_IRQ1	Event triggered by the SIMCOP DMA. Check SIMCOP DMA IRQ registers. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
17	LDC2BRIDGE_ERR_IRQ	The LDC2 bridge has generated an error. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
16	ICNT_ERR_IRQ	An error has been received on the SIMCOP master port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
15	VLCDJ_DECODE_ERR_IRQ	A decode error has been signaled by the VLCDJ module Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
14	DONE_IRQ	Event triggered when the HW sequencer finishes the sequence: - the sequence step counter has reached the limit - all accelerator and DMA events for the last sequence step have been received. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
13	STEP3_IRQ	Event triggered when STEP3 is activated by the HW sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
12	STEP2_IRQ	Event triggered when STEP2 is activated by the HW sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
11	STEP1_IRQ	Event triggered when STEP1 is activated by the HW sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
10	STEP0_IRQ	Event triggered when STEP0 is activated by the HW sequencer Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
9	LDC_BLOCK_IRQ	This event is triggered by LDC when a macroblock has been processed Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
8	NSF3_IRQ	Event triggered by the NSF3 imaging accelerator when processing of a block is done Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
7	ROT_A	Event triggered by the ROT A engine Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
6	IMX_B_IRQ	Event triggered when IMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
5	IMX_A_IRQ	Event triggered when IMX has executed a SLEEP instruction. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
4	NSF_IRQ_IRQ	Event triggered by the NSF2 imaging accelerator when processing of a block is done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
3	VLCDJ_BLOC_IRQ	This event is triggered by VLCDJ when a macro-bloc has been processed (encode/decode) Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
2	DCT_IRQ	Event triggered when a block has been processed by the DCT module and the filter outcome has been stored to an image buffer. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
1	LDC_FRAME_IRQ	This event is triggered by LDC when a full frame has been processed Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
0	SIMCOP_DMA_IRQ0	Event triggered by the SIMCOP DMA. Check SIMCOP DMA IRQ registers. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

Table 8-1368. Register Call Summary for Register SIMCOP_HL_IRQENABLE_CLR_i

ISS SIMCOP Overview
- Interrupt Merger: [0] [1]
- SIMCOP Register Summary: [2]

Table 8-1369. SIMCOP_CTRL

Address Offset	0x0000 0060		
Physical Address	0x5202 0060 0x5506 0060	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	SIMCOP control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NSF3_WMEM		RESERVED	LDC_R_BURST_BREAK	LDC_R_MAX_BURST_LENGHT		RESERVED		LDC_R_TAG_CNT			RESERVED		LDC_R_TAG_OFST			RESERVED	IMX_B_CMD	IMX_A_CMD		HUFF	QUANT	RESERVED	LDC_LUT	LDC_INPUT		NSF_WMEM		IRQ3_MODE	IRQ2_MODE	IRQ1_MODE	IRQ0_MODE

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Bits	Field Name	Description	Type	Reset
31:30	NSF3_WMEM	Selects working memory for NSF3. Memories attached to NSF3 as working memories cannot be used by any other accelerators. HWSEQ or HWSEQ SW override settings are ignored for those memories. 0x0: No working memory attached to NSF3. NSF3 cannot be used. 0x1: IMX A + B coefficient memories used. 0x2: Image buffers a, b, c, and d used. Those image buffers cannot be used for other purposes. This setting has higher priority than the context configuration	RW	0x0
29	RESERVED		R	0x0
28	LDC_R_BURST_BREAK	Controls if bursts issued by the LDC2 bridge could cross burst length boundaries. When this register is set, the LDC2 bridge only issues aligned bursts. Register can only be used when LDC_R_MAX_BURST_LENGHT is 32, 64 or 128 bytes. 0x0: Yes. 0x1: No. OCP transactions must be split	RW	0
27:26	LDC_R_MAX_BURST_LENGHT	Limits the maximum burst length that could be used by the LDC2 bridge 0x0: 8x128 0x1: 6x128 0x2: 4x128 0x3: 2x128	RW	0x0
25	RESERVED	Read returns 0.	R	0
24:21	LDC_R_TAG_CNT	Limits the maximum number of outstanding requests to LDC_R_TAG_CNT+1	RW	0x3
20	RESERVED	Read returns 0.	R	0
19:16	LDC_R_TAG_OFST	First OCP tag ID that can be used by LDC reads. It is SW's responsibility to prevent overlap with tags generated by the SIMCOP DMA Typically this value should be equal to SIMCP_DMA_CTRL.TAG_CNT+1	RW	0xC
15	RESERVED	Read returns 0.	R	0
14	IMX_B_CMD	Switch for IMX # command memory 0x0: Coprocessor bus 0x1: IMX B instruction read / write	RW	0
13:12	IMX_A_CMD	Switch for IMX A command memory 0x0: Coprocessor bus 0x1: IMX A instruction read / write 0x2: IMX B instruction read / write	RW	0x0
11	HUFF	Switch for Huffman table 0x0: Coprocessor 0x1: VLCDJ Huffman table read	RW	0
10	QUANT	Switch for quantization table 0x0: Coprocessor bus 0x1: VLCDJ quantization table read	RW	0
9	RESERVED	Read returns 0.	R	0
8	LDC_LUT	Switch for LDC LUT 0x0: Coprocessor bus 0x1: The LDC module could access the LDC LUT.	RW	0

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Bits	Field Name	Description	Type	Reset
7:6	LDC_INPUT	Selects input data buffer for LDC. Memories attached to LDC as working memories cannot be used by any other accelerators. HWSEQ or HWSEQ SW override settings are ignored for those memories. 0x0: No input memory attached 0x1: use image buffers a and b 0x2: use image buffers a, b, c, and d 0x3: Use LDC private input memory.	RW	0x0
5:4	NSF_WMEM	Selects working memory for NSF. Memories attached to NSF as working memories cannot be used by any other accelerators. HWSEQ or HWSEQ SW override settings are ignored for those memories. 0x0: No working memory attached to NSF2. NSF2 cannot be used. 0x1: IMX A coefficient memory used. 0x2: Image buffers a and b used. Those image buffers cannot be used for other purposes. This setting has higher priority than the context configuration 0x3: Image buffers a, b, c, d used. Those image buffers cannot be used for other purposes. This setting has higher priority than the context configuration	RW	0x0
3	IRQ3_MODE	Interrupt generation method 0x0: The interrupt line is asserted when one of the events enabled in SIMCOP_IRQENABLE_3 is pending 0x1: The interrupt line is asserted when all events enabled in SIMCOP_IRQENABLE_3 are pending	RW	0
2	IRQ2_MODE	Interrupt generation method 0x0: The interrupt line is asserted when one of the events enabled in SIMCOP_IRQENABLE_2 is pending 0x1: The interrupt line is asserted when all events enabled in SIMCOP_IRQENABLE_2 are pending	RW	0
1	IRQ1_MODE	Interrupt generation method 0x0: The interrupt line is asserted when one of the events enabled in SIMCOP_IRQENABLE_1 is pending 0x1: The interrupt line is asserted when all events enabled in SIMCOP_IRQENABLE_1 are pending	RW	0
0	IRQ0_MODE	Interrupt generation method 0x0: The interrupt line is asserted when one of the events enabled in SIMCOP_IRQENABLE_0 is pending 0x1: The interrupt line is asserted when all events enabled in SIMCOP_IRQENABLE_0 are pending	RW	0

Table 8-1370. Register Call Summary for Register SIMCOP_CTRL

ISS SIMCOP Overview

- Interrupt Merger: [0]
- Interrupts: [1] [2]
- SIMCOP Register Summary: [3]

Table 8-1371. SIMCOP_CLKCTRL

Address Offset	0x0000 0064		
Physical Address	0x5202 0064 0x5506 0064	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	SIMCOP clock control register. Use to enable/disable the interface and functional clock of SIMCOP submodules. Disabled modules cannot be accessed		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						NSF3	RESERVED	ROT_A	IMX_B	IMX_A	NSF2	VLCDJ	DCT	LDC	DMA

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Read returns 0.	R	0x000000
9	NSF3	NSF3	RW	0
		Write 0x0: Request shutdown of the sub-module. No effect if the sub-module clock is already off		
		Read 0x0: The sub-module is off		
		Read 0x1: The sub-module is on		
		Write 0x1: Request enable of the sub-module. No effect if the sub-module clock is already on		
8	RESERVED	Read returns 0.		0x000000
7	ROT_A	ROT A	RW	0
		Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off.		
		Read 0x0: The submodule is off		
		Read 0x1: The submodule is on		
		Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.		
6	IMX_B	IMX B	RW	0
		Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off.		
		Read 0x0: The submodule is off		
		Read 0x1: The submodule is on		
		Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.		
5	IMX_A	IMX A	RW	0
		Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off.		
		Read 0x0: The submodule is off		
		Read 0x1: The submodule is on		
		Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.		
4	NSF2	NSF2	RW	0
		Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off.		
		Read 0x0: The submodule is off		
		Read 0x1: The submodule is on		
		Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.		
3	VLCDJ	VLCDJ	RW	0
		Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off.		
		Read 0x0: The submodule is off		
		Read 0x1: The submodule is on		
		Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.		

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Bits	Field Name	Description	Type	Reset
2	DCT	DCT Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off Read 0x1: The submodule is on Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.	RW	0
1	LDC	LDC Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off Read 0x1: The submodule is on Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.	RW	0
0	DMA	DMA Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off Read 0x1: The submodule is on Write 0x1: Request enable of the submodule. No effect if the submodule clock is already on.	RW	0

Table 8-1372. Register Call Summary for Register SIMCOP_CLKCTRL

ISS SIMCOP Overview

- ISS SIMCOP Local Clock Management: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- ISS SIMCOP Power Management: [14]
- ISS SIMCOP Module Global Initialization: [15]
- SIMCOP Register Summary: [16]

Table 8-1373. SIMCOP_CTRL2

Address Offset	0xFC		
Physical Address	0x5202 00FC 0x5506 00FC	**Instance**	SIMCOP_MAIN_L3 SIMCOP_IPU
Description	Simcop control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				LDCR_BW_CTRL											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	RO Rreturns 0s	0x00000
11:0	LDCR_BW_CTRL	Limits the mean bandwidth (computed over 16 requests) that the LDC module can request for read from system memory 0: The BW limiter is bypassed 1..47: reserved 48..4095: LDCR_BW_CTRL/4 functional clock cycles between two consecutive requests of 32 bytes.	RW	0x000

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Table 8-1374. Register Call Summary for Register SIMCOP_CTRL2

ISS SIMCOP Overview

- SIMCOP Register Summary: [0]

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8.4.1.5 ISS SIMCOP Memory Mapping

Table 8-1375 shows the SIMCOP memory mapping seen by the L3_MAIN interconnect and the Cortex-M4 IPU subsystem. SIMCOP memory mapping has a 128-KiB address space.

Table 8-1375. SIMCOP Memory Mapping

Module	L3_MAIN Address		Cortex-M4 address		Size (bits)
	Begin	End	Begin	End	
Hardware sequencer/buffer registers	0x5202 0000	0x5202 00FF	0x5506 0000	0x5506 00FF	256
LDC registers	0x5202 0100	0x5202 017F	0x5506 0100	0x5506 017F	128
IMX a registers	0x5202 0180	0x5202 01BF	0x5506 0180	0x5506 01BF	64
IMX b registers	0x5202 01C0	0x5202 01FF	0x5506 01C0	0x5506 01FF	64
SIMCOP DMA registers	0x5202 0200	0x5202 03FF	0x5506 0200	0x5506 03FF	512
Reserved	0x5202 0400	0x5202 05FF	0x5506 0400	0x5506 05FF	512
VLCDJ registers	0x5202 0600	0x5202 067F	0x5506 0600	0x5506 067F	128
Reserved	0x5202 0680	0x5202 06FF	0x5506 0680	0x5506 06FF	128
ROT registers	0x5202 0700	0x5202 073F	0x5506 0700	0x5506 073F	64
Reserved	0x5202 0740	0x5202 077F	0x5506 0740	0x5506 077F	64
NSF2 registers	0x5202 0780	0x5202 07FF	0x5506 0780	0x5506 07FF	128
DCT registers	0x5202 0800	0x5202 081F	0x5506 0800	0x5506 081F	32
Reserved	0x5202 0820	0x5202 08FF	0x5506 0820	0x5506 08FF	224
NSF3 registers	0x5202 0900	0x5202 09FF	0x5506 0900	0x5506 09FF	256
Reserved	0x5202 0A00	0x5202 0FFF	0x5506 0A00	0x5506 0FFF	1536
Bitstream buffer	0x5202 1000	0x5202 1FFF	0x5506 1000	0x5506 1FFF	4096
Huffman tables	0x5202 2000	0x5202 2FFF	0x5506 2000	0x5506 2FFF	4096
Reserved	0x5202 3000	0x5202 3FFF	0x5506 3000	0x5506 3FFF	4096
IMX B command memory	0x5202 4000	0x5202 5FFF	0x5506 4000	0x5506 5FFF	8192
IMX A command memory	0x5202 6000	0x5202 6FFF	0x5506 6000	0x5506 6FFF	4096
Quantization tables	0x5202 7000	0x5202 71FF	0x5506 7000	0x5506 71FF	512
Reserved	0x5202 7200	0x5202 73FF	0x5506 7200	0x5506 73FF	512
LDC LUT	0x5202 7400	0x5202 75FF	0x5506 7400	0x5506 75FF	512
Reserved	0x5202 7600	0x5202 7FFF	0x5506 7600	0x5506 7FFF	2560
Image buffer a	0x5202 8000	0x5202 8FFF	0x5506 8000	0x5506 8FFF	4096
Image buffer b	0x5202 9000	0x5202 9FFF	0x5506 9000	0x5506 9FFF	4096
Image buffer c	0x5202 A000	0x5202 AFFF	0x5506 A000	0x5506 AFFF	4096
Image buffer d	0x5202 B000	0x5202 BFFF	0x5506 B000	0x5506 BFFF	4096
Image buffer e	0x5202 C000	0x5202 CFFF	0x5506 C000	0x5506 CFFF	4096
Image buffer f	0x5202 D000	0x5202 DFFF	0x5506 D000	0x5506 DFFF	4096
Image buffer g	0x5202 E000	0x5202 EFFF	0x5506 E000	0x5506 EFFF	4096
Image buffer h	0x5202 F000	0x5202 FFFF	0x5506 F000	0x5506 FFFF	4096
IMX A coeffficients memory	0x5203 0000	0x5203 3FFF	0x5507 0000	0x5507 3FFF	16,384
IMX B coeffficients memory	0x5203 4000	0x5203 7FFF	0x5507 4000	0x5507 7FFF	16,384

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8.4.2 ISS SIMCOP Hardware Sequencer and Buffers Module

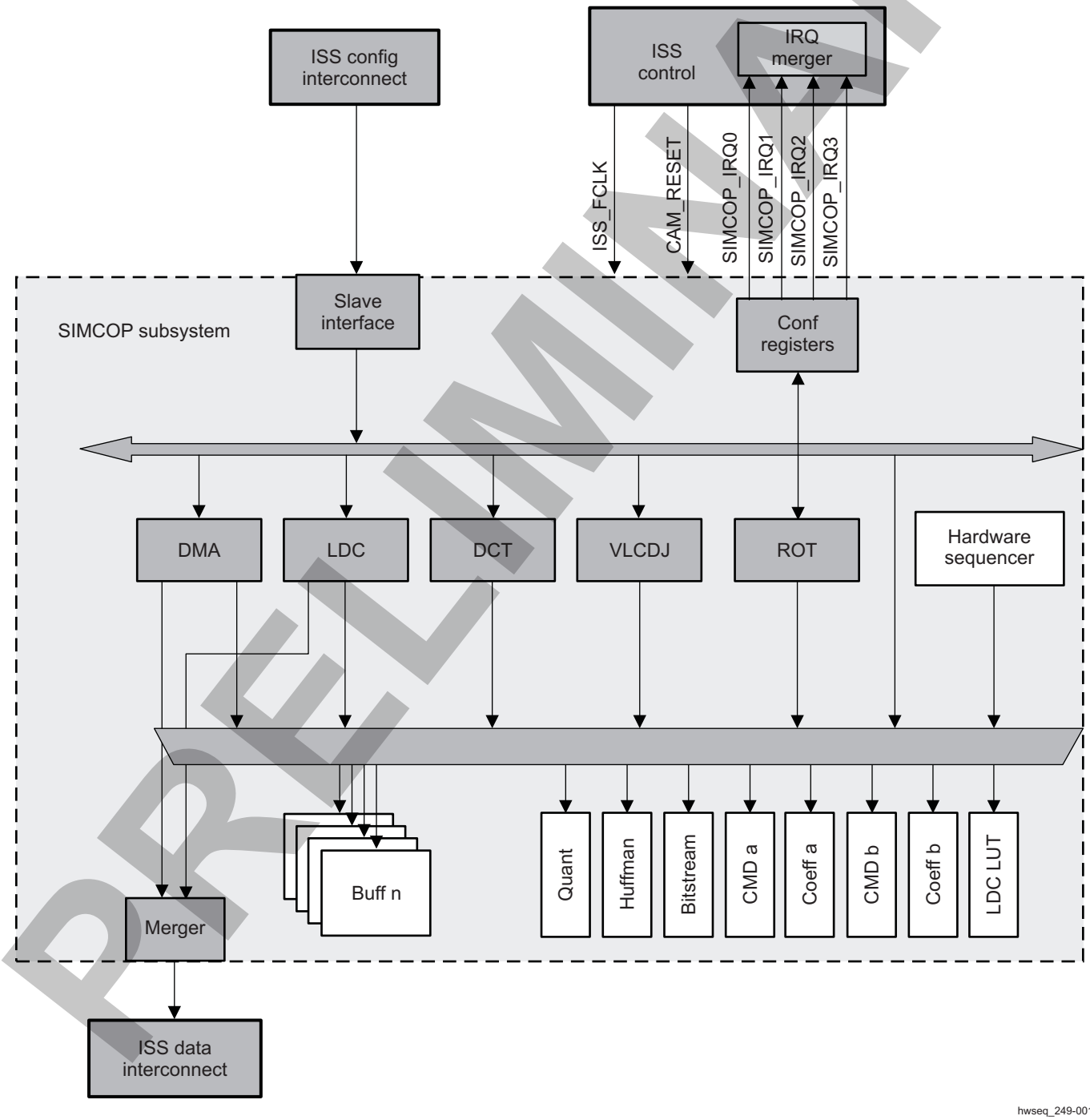
This section describes the hardware sequencer and buffers in the still image coprocessor (SIMCOP) subsystem.

8.4.2.1 ISS SIMCOP Hardware Sequencer and Buffers Overview

The SIMCOP hardware sequencer control all the modules included in the SIMCOP subsystem with their memories.

Figure 8-260 shows an overview of the hardware sequencer and buffers in the SIMCOP subsystem.

Figure 8-260. Hardware Sequencer and Buffers in the SIMCOP Subsystem



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- Hadrware acceleration for low-level sequencing tasks:
  - Synchronizes with DMA, DCT, VLCD, ROT, LDC
  - Supports 4 memory crossbar contexts
- On chip memories (RAM):
  - 8 image buffers, 4 KiB each
  - Quantization table storage: 512 bytes
  - Huffman table storage: 4 KiB
  - Bitstream buffer: 4 KiB
  - LDC look-up table storage: 256 entries
- Power management support

8.4.2.2 ISS SIMCOP Hardware Sequencer and Buffer Integration

The hardware sequencer and buffers module is part of the SIMCOP subsystem in the ISS.

Figure 8-261 shows the integration of the hardware sequencer and buffers in the SIMCOP subsystem.

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Figure 8-261. Hardware Sequencer and Buffer Integration

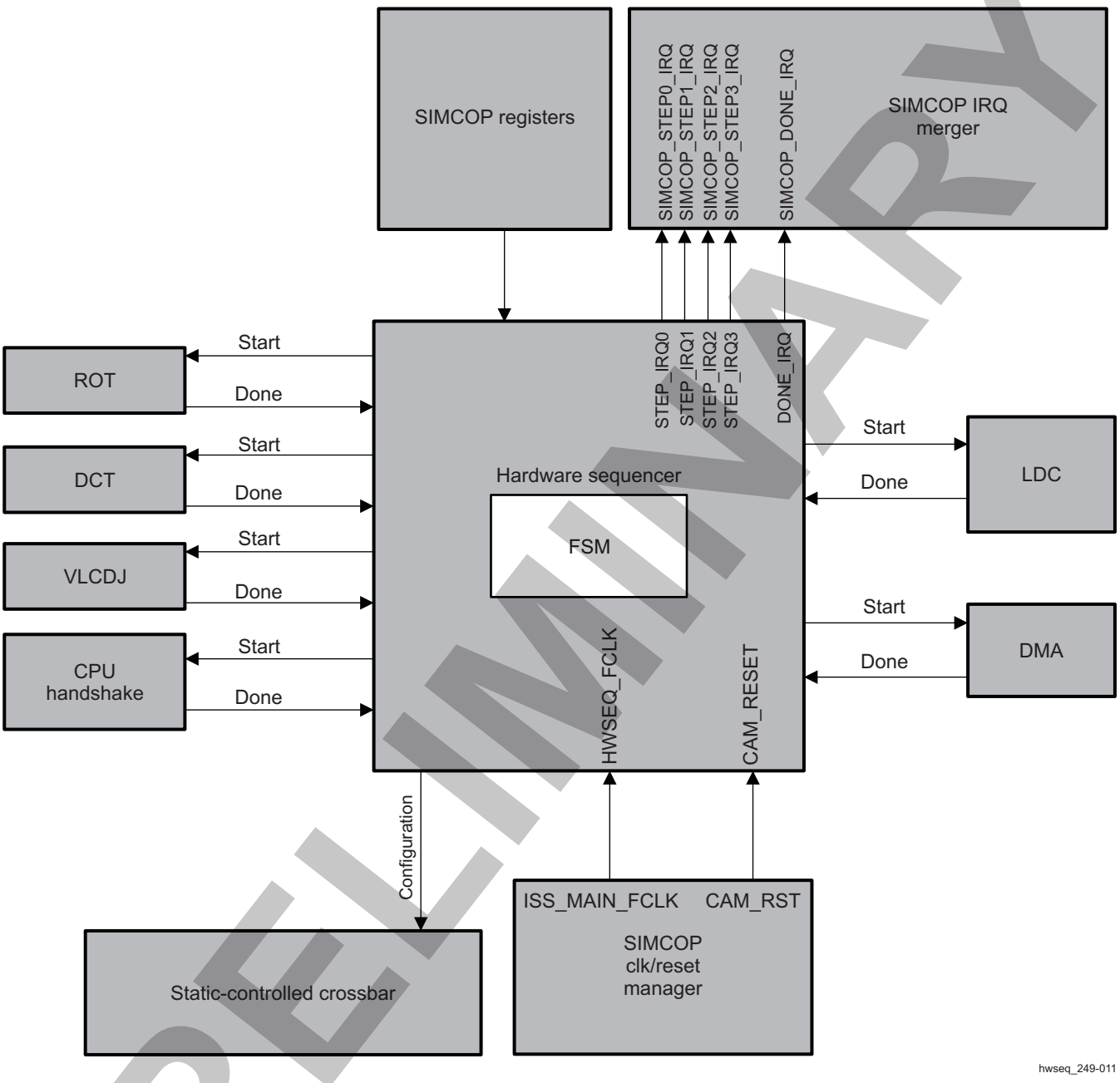

Table 8-1376 lists the integration attributes, Table 8-1377 lists the clocks and resets, and Table 8-1378 lists the hardware requests.

Table 8-1376. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
Hardware sequencer and buffers	PD_CAM	

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Table 8-1377. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
Hardware sequencer and buffers	HWSEQ_FCLK	ISS_MAIN_FCLK	ISS	Functional clock provided by CORE_ISS_MAIN_FCLK from PRCM . It is used by all ISS sub-modules and ISS top level resources.
Hardware sequencer and buffers	HWSEQ_ICLK	L3MAIN2_L3_GICLK	PRCM	Interface clock provided by L3MAIN2_L3_GICLK from PRCM. It is used by all ISS sub-modules and ISS top-level resources.
Resets				
Hardware sequencer and buffers	CAM_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

For information about clock and reset management, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

Table 8-1378. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
Hardware sequencer and buffers	STEP_IRQ0	SIMCOP_STEP0_IRQ	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
Hardware sequencer and buffers	STEP_IRQ1	SIMCOP_STEP1_IRQ	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
Hardware sequencer and buffers	STEP_IRQ2	SIMCOP_STEP2_IRQ	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
Hardware sequencer and buffers	STEP_IRQ3	SIMCOP_STEP3_IRQ	SIMCOP IRQ merger	Event triggered when a SIMCOP context is activated by the hardware sequencer
Hardware sequencer and buffers	DONE_IRQ	SIMCOP_DONE_IRQ	SIMCOP IRQ merger	Event triggered when the hardware sequencer finishes the sequence

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*

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8.4.2.3 ISS SIMCOP Hardware Sequencer and Buffers Functional Description

8.4.2.3.1 ISS SIMCOP Hardware Sequencer and Buffers Software Reset

For information about how to perform a software reset, see Section 8.4.1.2.2, *Software Reset*.

8.4.2.3.2 ISS SIMCOP Hardware Sequencer and Buffers Power Management

For more information about power management, see Section 8.4.1.2.1.3, *ISS SIMCOP Power Management*.

8.4.2.3.3 ISS SIMCOP Hardware Sequencer and Buffer Interrupt Requests

This module sends four interrupts to the ISS top level. For more information about interrupt management, see Section 8.4.1.2.3, *Interrupt Merger*.

8.4.2.3.4 ISS SIMCOP Hardware Sequencer Buffer Description

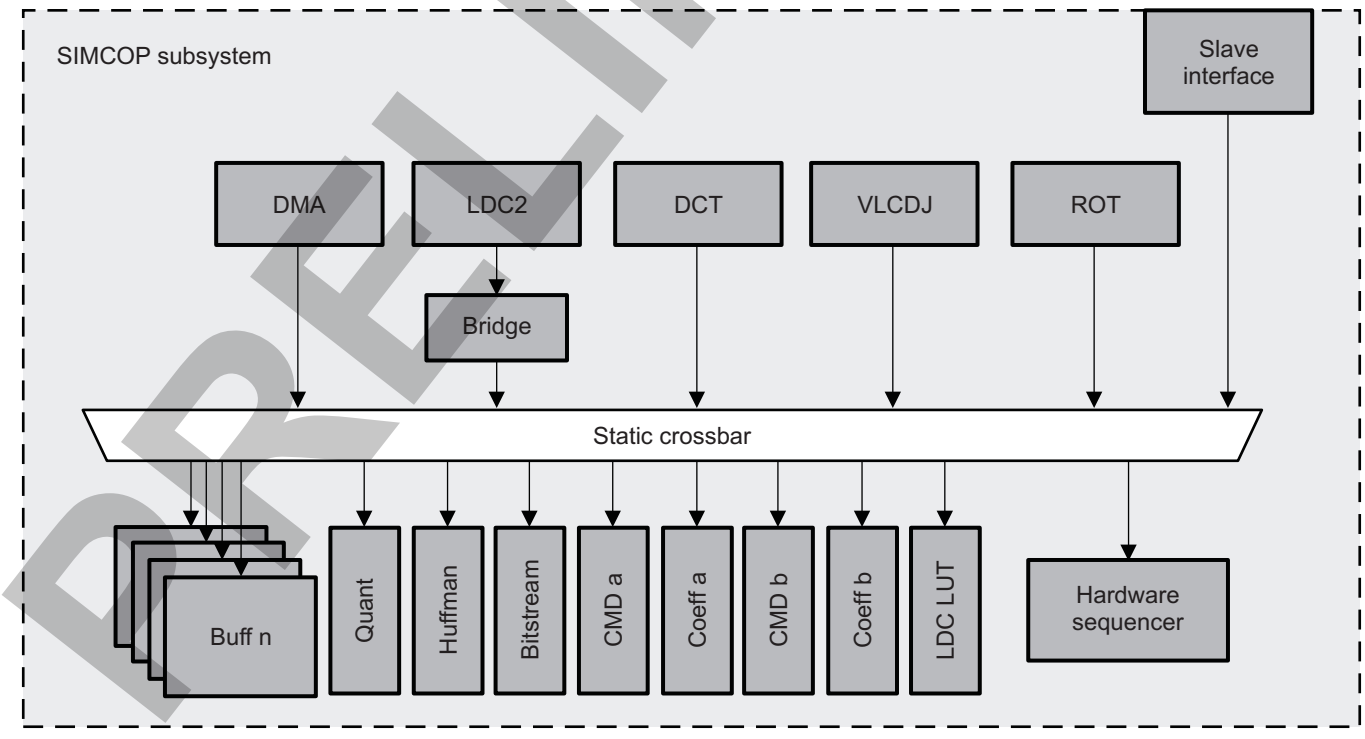
The SIMCOP subsystem includes the following memories:

- Eight image buffers: 4 KiB each
- Quantization table storage: 512 bytes
- Huffman table storage: 4 KiB
- Bitstream buffer: 4 KiB
- LDC lookup tables storage: 256 entries
- LDC private working memory

8.4.2.3.4.1 Static Crossbar

The static crossbar connect SIMCOP modules to the SIMCOP memories as shown in Figure 8-262.

Figure 8-262. SIMCOP Static Crossbar Overview



hwseq_249-002

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The buses for QUANT, HUFF, LDC LUT, CMD a, and CMD b are controlled by the CPU. Typically, those memories are initialized before the SIMCOP starts processing and the content remains unchanged until the full frame is processed. The amount of data transferred to those memories is low and transfer is not timing critical. Table 8-1379 shows how to connect these memories to the SIMCOP modules.

NOTE: The transfer can only be done through the slave interface (that is, the CPU or system DMA). The SIMCOP DMA can not access those memories.

Table 8-1379. Static Crossbar Control Summary

Memory	Register SIMCOP_CTRL	Value				
		Bus	VLCDJ HUFF	VLCDJ QUANT	LDC LUT	LDC INPUT
Quantization	[10] QUANT	0		1		
Huffman	[11] HUFF	0	1			
LDC LUT	[8] LDC_LUT	0			1	
LDC Priv	[7:6] LDC_INPUT					3

Image buffers and coefficient memories are used to store the data to be processed and processing results. Those memories can be accessed by the SIMCOP DMA, SIMCOP bus, and SIMCOP modules. Table 8-1380 shows possible connections in the SIMCOP static crossbar. For example, the DCT Freq port could access image buffer a when SIMCOP_HWSEQ_SWITCH_i[2:0] IMBUFF_A = 5 (i = 0, 1, 2, or 3 corresponds to the active context).

The SIMCOP supports multiple contexts for the configuration of those memories. Software or the hardware sequencer can activate different contexts.

The BITSTREAM data flow is asynchronous from the macroblock pipeline, therefore, it supports dynamic buffer switching logic.

Table 8-1380. Static Crossbar Control Summary (2/2)

Memory	Register (SIMCOP_HWSEQ_STEP_SWITCH_i and SIMCOP_HWSEQ_STEP_CTRL2_i)	Value									
		Bus	DMA	VLCDJ IO	VLCDJ BS	DCT Spatial	DCT Freq	LDC 0	LDC WMEM	ROT In	ROT Out
IMBUF a	[2:0] IMBUFF A	0	1	4			5		LDC_INPUT= 1 or 2	6	
IMBUF b	[6:4] IMBUFF B	0	1	4			5			6	
IMBUF c	[10:8] IMBUFF C	0	1	4			5		LDC_INPUT= 2	6	
IMBUF d	[14:12] IMBUFF D	0	1	4			5			6	
IMBUF e	[18:16] IMBUFF E	0	1			4		6			7
IMBUF f	[22:20] IMBUFF F	0	1			4		6			7
IMBUF g	[27:24] IMBUFF G	0	1	4		5	6	9			7
IMBUF h	[31:28] IMBUFF H	0	1	4		5	6	9			7
Bitstream	Handled by hardware	X	X				X				

8.4.2.3.4.2 Image Buffers

Image buffers are 4 banks × 256 × 32 bits (4K bytes) working memories used by the SIMCOP modules to perform image processing operations. Image buffers are shared between the DCT, LDC, VLCDJ, ROT, DMA, and SIMCOP bus accesses. All initiators cannot access the image buffers simultaneously.

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Switches are controlled by the hardware sequencer or an external initiator through register configuration. Data is always organized in little endian form.

One or multiple image buffers can be attached to a given accelerator port by configuring the appropriate bits in the SIMCOP_HWSEQ_STEP_SWITCH_i registers.

The image buffer address mapping to different busses shown in Table 8-1381 is controlled using the appropriate SIMCOP_HWSEQ_STEP_CTRL_i register bit fields.

Table 8-1381. Image Buffer Address Map

Port	OFST	0x0000	0x1000	0x2000	0x3000	0x4000	0x5000	0x6000	0x7000
DMA	0	A	B	C	D	E	F	G	H
	1	B	C	D	E	F	G	H	A
	2	C	D	E	F	G	H	A	B
	3	D	E	F	G	H	A	B	C
	4	E	F	G	H	A	B	C	D
	5	F	G	H	A	B	C	D	E
	6	G	H	A	B	C	D	E	F
	7	H	A	B	C	D	E	F	G
VLCDJ IO	0	A	B	C	D				
	1	B	C	D	G				
	2	C	D	G	H				
	3	D	G	H	A				
	4	G	H	A	B				
	5	H	A	B	C				
	6								
	7								
DCT Spatial	0	E	F						
	1	F	G						
	2	G	H						
	3	H	E						
DCT Freq	0	A	B	C	D				
	1	B	C	D	G				
	2	C	D	G	H				
	3	D	G	H	A				
	4	G	H	A	B				
	5	H	A	B	C				
	6								
	7								
LDC W	n/a	A	B	C	D				
ROT In	0	A	B	C	D				
	1	B	C	D	A				
	2	C	D	A	B				
	3	D	A	B	C				
ROT Out	0	E	F	G	H				
	1	F	G	H	E				
	2	G	H	E	F				
	3	H	E	F	G				

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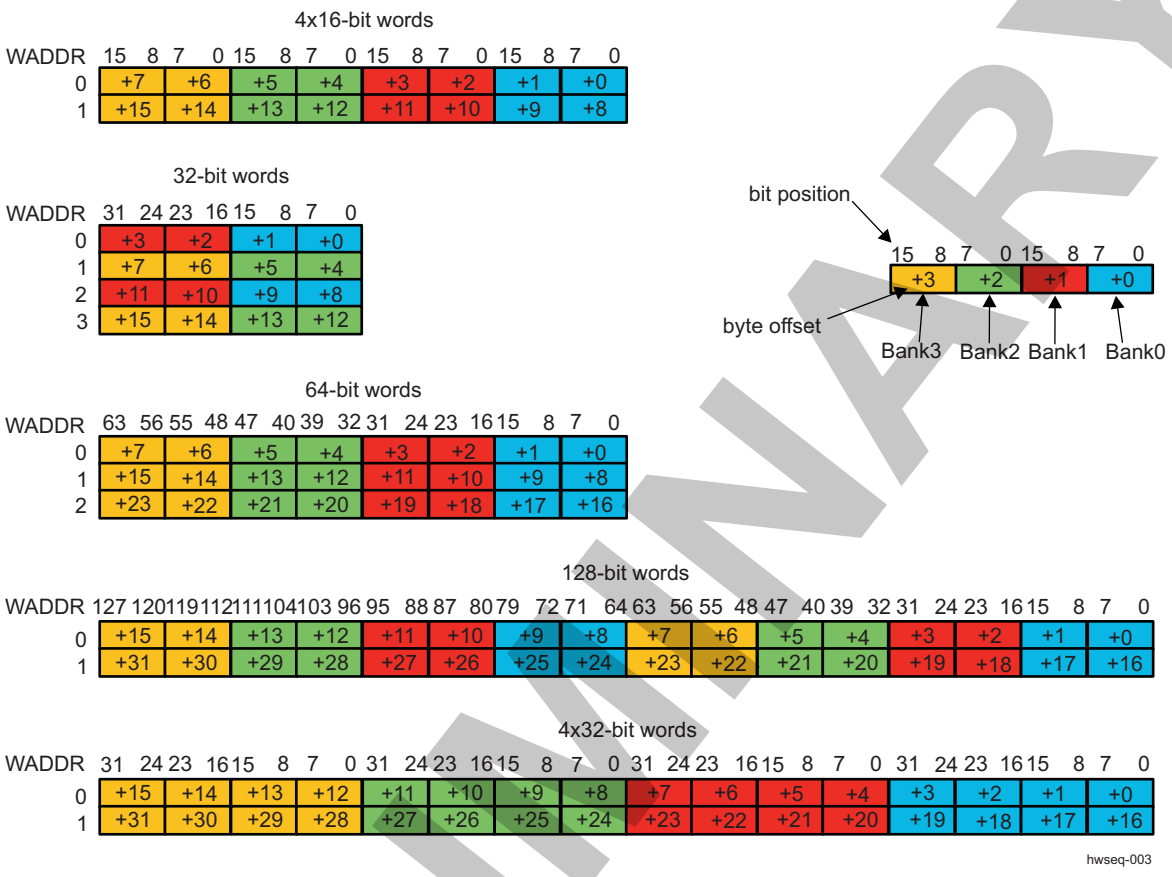
Figure 8-263 shows how width conversion and bank interleaving is performed, each colors correspond to a different physical bank.

Figure 8-263. Image Buffer Width Translation



8.4.2.3.4.3 Quantization Memories

The QUANT memory is used to store the quantization and dequantization tables for the VLCDJ module.

Coefficients are coded as 16-bit values. Every color component requires 8 × 8 quantization entries, therefore the QUANT memory of SIMCOP can hold up to four tables as shown in Table 8-1382.

Table 8-1382. Quantization Table Storage in QUANT Memory

Table	0	1	2	3
ADDR	0x000	0x0080	0x0100	0x0180
Encode only	Y quantization	UV quantization	Unused	Unused
Decode only	Unused	Unused	Y dequantization	UV dequantization
Encode and decode	Y quantization	UV quantization	Y dequantization	UV dequantization

The QUANT memory is shared between the VLCDJ and SIMCOP bus accesses. All initiators cannot access QUANT simultaneously.

The initiators access types to the QUANT memory are summarized in Table 8-1383. QUANT memory configuration depends on the initiators.

Table 8-1383. QUANT Memory Organization

VLCDJ	Coprocessor bus
128 words x 32 bit	128 words x 32 bits

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8.4.2.3.4.4 Huffman Tables

The HUFF memory is used to store the Huffman table for the VLCDJ module. Details about the Huffman table organization can be found in the VLCDJ module description, see Section 8.4.6, *VLCDJ* .

The HUFF memory is shared between the VLCDJ and SIMCOP bus accesses. All initiators cannot access the HUFF memory simultaneously.

The initiators access types to the HUFF memory are summarized in Table 8-1384. The HUFF memory configuration depends on the initiators.

Table 8-1384. HUFF Memory Organization

VLCDJ	Coprocessor bus
1024 words x 32 bits	1024 words x 32 bits

8.4.2.3.4.5 BITSTREAM Buffer

8.4.2.3.4.5.1 Overview

The BITSTREAM buffer is used to store the VLCDJ bit stream. The BITSTREAM buffer is shared between the VLCDJ, DMA, and SIMCOP bus accesses.

The BITSTREAM buffer can be used in manual or automatic mode.

In manual mode, software selects if the SIMCOP DMA, VLCDJ Bit Stream port, or SIMCOP bus can access the BITSTREAM buffer. Manual mode is typically used to interleave JPEG encode and decode, for example to support JPEG transcoding. .

In automatic mode (SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM = ENCODE or DECODE) the BITSTREAM buffer is handled as two banks to prevent access collision between the VLCDJ and SIMCOP DMA. A dedicated hardware engine (BBM) is used to guarantee that the VLCDJ and SIMCOP DMA access separate banks.

Automatic mode is disabled by writing SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM = COPR.

The BITSTREAM buffer mapping into the SIMCOP DMA address map depends on the SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM, SIMCOP_HWSEQ_CTRL[3:2] BITSTR_XFER_SIZE registers and the internal state of the BBM. Table 8-1385 shows the mapping of bitstream buffer for the SIMCOP DMA.

Table 8-1385. BITSTREAM Buffer Mapping to SIMCOP DMA

SIMCOP_HWSEQ_CTRL		Address Map		BBM count	Bitstream buffer	
BITSTREAM	XFER_SIZE					
0: COPR	N/A	0x1000	0x1FFF	N/A	0x000	0xFFF
5: ENCODE or 6: DECODE	2048 bytes	0x1000	0x17FF	N/A	0x000	0x7FF
				N/A	0x800	0xFFF
		0x1800	0x1FFF	N/A	N/A	N/A
	1024 bytes	0x1000	0x13FF	0	0x000	0x3FF
				1	0x400	0x7FF
		0x1400	0x1FFF	N/A	N/A	N/A
	512 bytes	0x1000	0x11FF	0	0x000	0x1FF
				1	0x200	0x3FF
				2	0x400	0x5FF
				3	0x600	0x7FF
		0x1200	0x1FFF	N/A	N/A	N/A
	256 bytes			0	0x000	0x0FF
				1	0x100	0x1FF
				2	0x200	0x2FF

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Table 8-1385. BITSTREAM Buffer Mapping to SIMCOP DMA (continued)

SIMCOP_HWSEQ_CTRL		Address Map		BBM count	Bitstream buffer	
BITSTREAM	XFER_SIZE					
		0x1000	0x10FF	3	0x300	0x3FF
				4	0x400	0x4FF
				5	0x500	0x5FF
				6	0x600	0x6FF
				7	0x700	0x7FF
		0x1100	0x1FFF	N/A	N/A	N/A

8.4.2.3.4.5.2 Automatic BITSTREAM Buffer Management

To enter automatic mode, software must write the following values into the BITSTREAM configuration register:

- SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM = COPR (required to reset BBM)
- SIMCOP_HWSEQ_CTRL[6:4] BITSTREAM = JPEG_ENCODE or JPEG_DECODE

8.4.2.3.4.6 LDC Lookup Table

The LDC_LUT memory is used to store lookup tables for the LDC module. The LDC_LUT is shared between the LDC and SIMCOP bus accesses. All initiators cannot access LDC_LUT simultaneously.

The initiators access types to the QUANT memory are summarized in Table 8-1386. QUANT memory configuration depends on the initiators.

Table 8-1386. LDC_LUT Memory Organization

LDC	Coprocessor bus
256 words x 14 bit	128 words x 32 bit (see Table 8-1387)

Table 8-. LUT Memory Format on 32-Bit Words

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LDC_LUT [2a+1]								RESERVED								LDC_LUT [2a+0]							

8.4.2.3.4.7 LDC Private Input Memory

The LDC has a private input memory that can be used when the LDC operates in YUV4:2:0 mode. For YUV4:2:2 and RAW operation, the LDC must use image buffers as input memories.

The LDC input memory is dedicated for LDC operation. It cannot be accessed from the SIMCOP bus or by any other SIMCOP module.

8.4.2.3.5 ISS SIMCOP Hardware Sequencer

The SIMCOP typically processes a full frame on a macroblock-by-macroblock basis. The SIMCOP modules and the DMA controller trigger an interrupt when they have completed a macroblock. This event can either trigger an interrupt to an external initiator (CPU) (manual mode) or trigger a context switch and resume DMA/SIMCOP module processing. Typically, initiator intervention is needed to fill the macroblock pipeline (called pipe-up, that is, the first n macroblocks of an image) and to flush the macroblock pipeline (called pipe-down, that is, the last n macro-blocks of an image). Automatic sequencing mode is typically used for the rest of the image.

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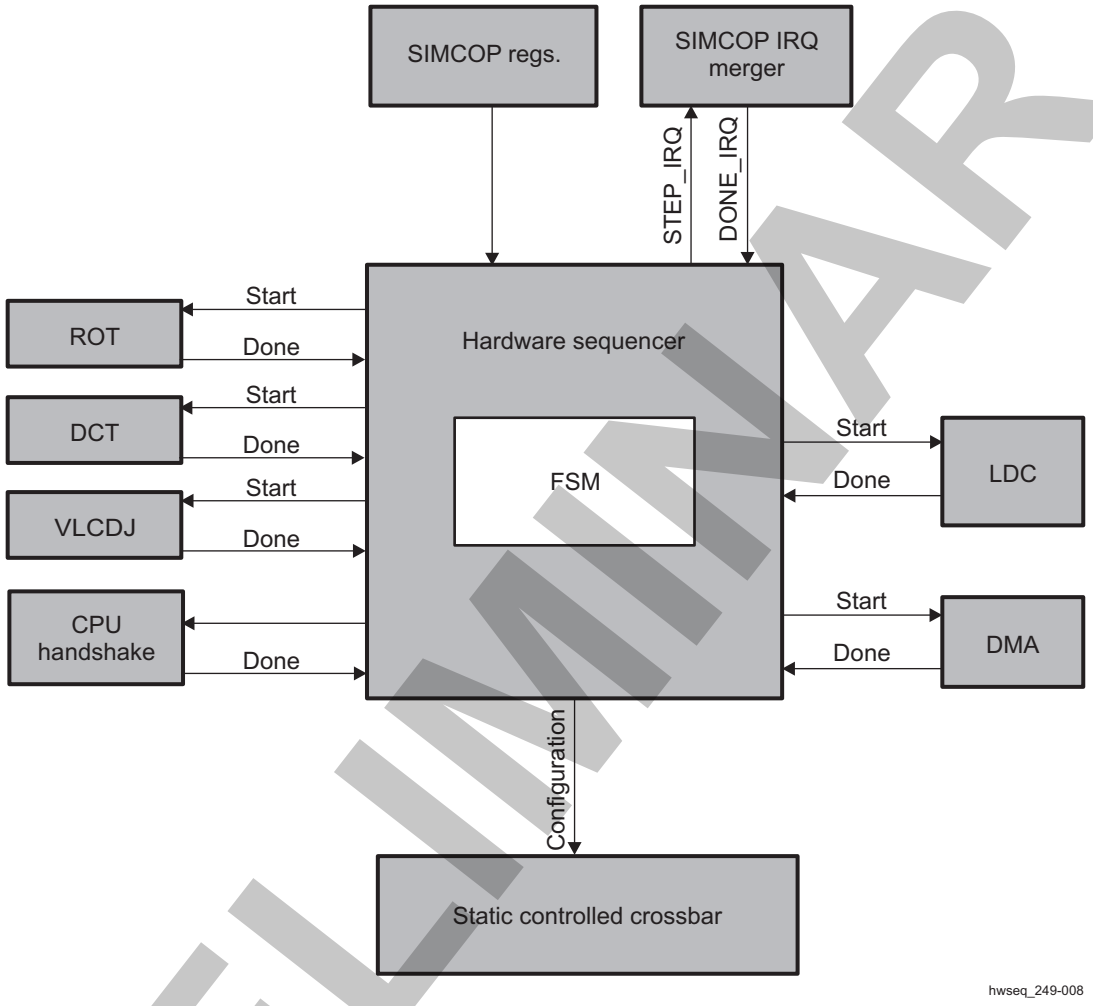
The hardware sequencer is particularly useful to offload the initiator during JPEG encoding/decoding, ROT or LDC processing.

Figure 8-264 depicts the SIMCOP hardware sequencer overview.

Figure 8-264. SIMCOP Hardware Sequencer Overview



The hardware sequencer can automatically execute a predefined number of sequencing steps without software intervention. This is called automatic operation. Automatic operation can also be used for pipeline filling and flushing with some limited software intervention. During automatic operation, the hardware sequencer controls the generation of START/DONE pulses and the connections in the static controlled crossbar. Software can take control over some resources while the hardware sequencer is running. This is called hardware sequencer override.

8.4.2.3.5.1 Automatic Operation

Figure 8-265 shows the flow diagram executed by the hardware sequencer.

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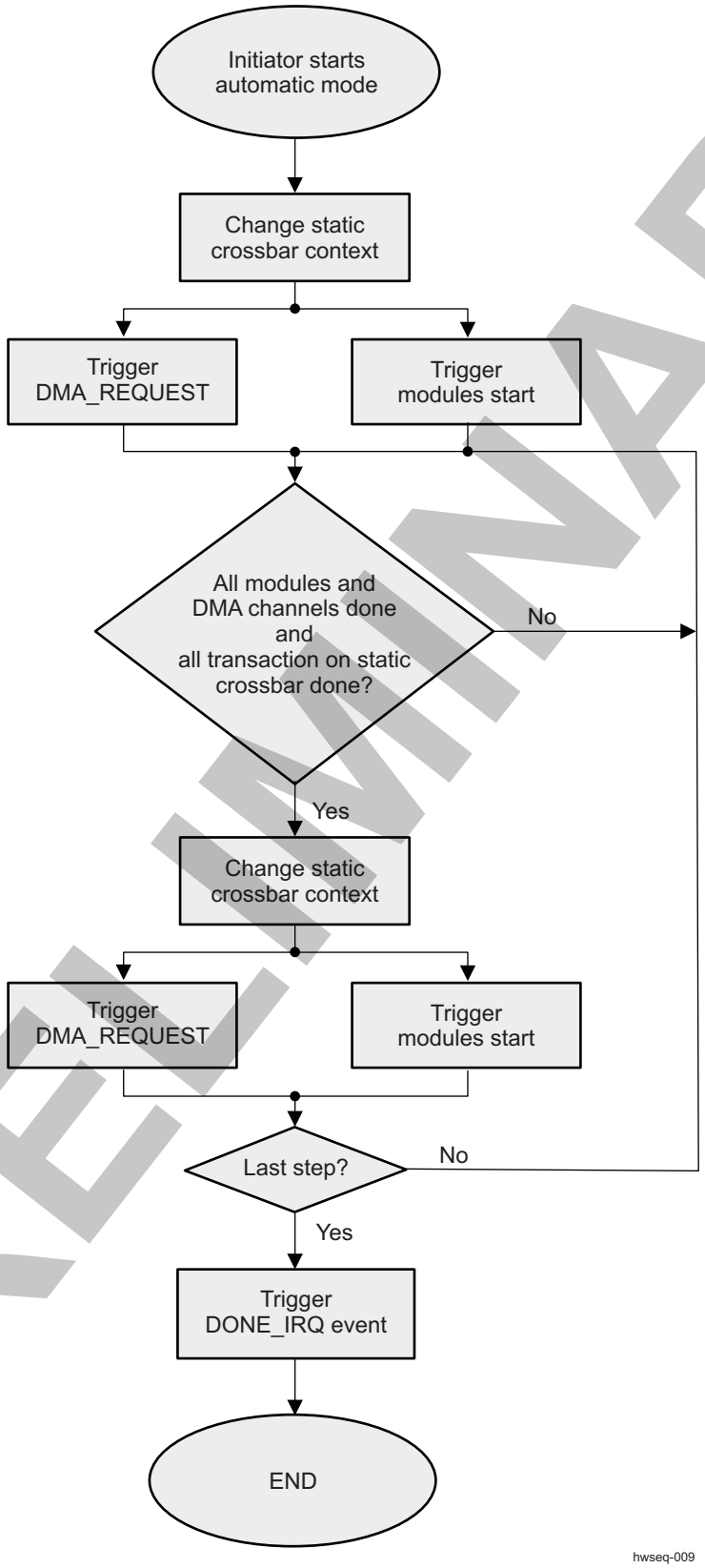
Figure 8-265. Hardware Sequencing Example



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The external initiator configures the different SIMCOP modules and DMA channels. When this is complete, it enables the hardware sequencer. This resets the internal state of the hardware sequencer (pending events and context switch counter).

It starts by running sequence step SIMCOP_HWSEQ_CTRL[12:11] STEP:

- Clear all pending completion events that have been selected for Step 0 in the hardware sequencer. Note: This does not affect the SIMCOP_IRQSTATUS register.
- Apply step SIMCOP_HWSEQ_CTRL[12:11] STEP configuration to the static crossbar
- Start DMA transfers. Multiple channels can be enabled sequentially (that is, YUV4:2:0 data transfers or SIMCOP-SDRAM followed by SDRAM-SIMCOP) by using the SIMCOP DMA linking feature.
- Start hardware accelerators. The list of accelerators to start can be selected by software using the SIMCOP_HWSEQ_STEP_CTRL_i[7:0] *_SYNC register

The hardware sequencer then waits for completion of events from the selected SIMCOP modules and SIMCOP DMA channels.

The hardware sequencer also ensures that all SIMCOP memory accesses requested by the accelerators and DMA channels enabled for the synchronization step have completed. This condition prevents data corruption due to early switching.

Steps can be chained to define the sequence to execute. Steps are started until the step counter reaches the limit defined by software. When the last step has completed, a DONE_IRQ event is triggered.

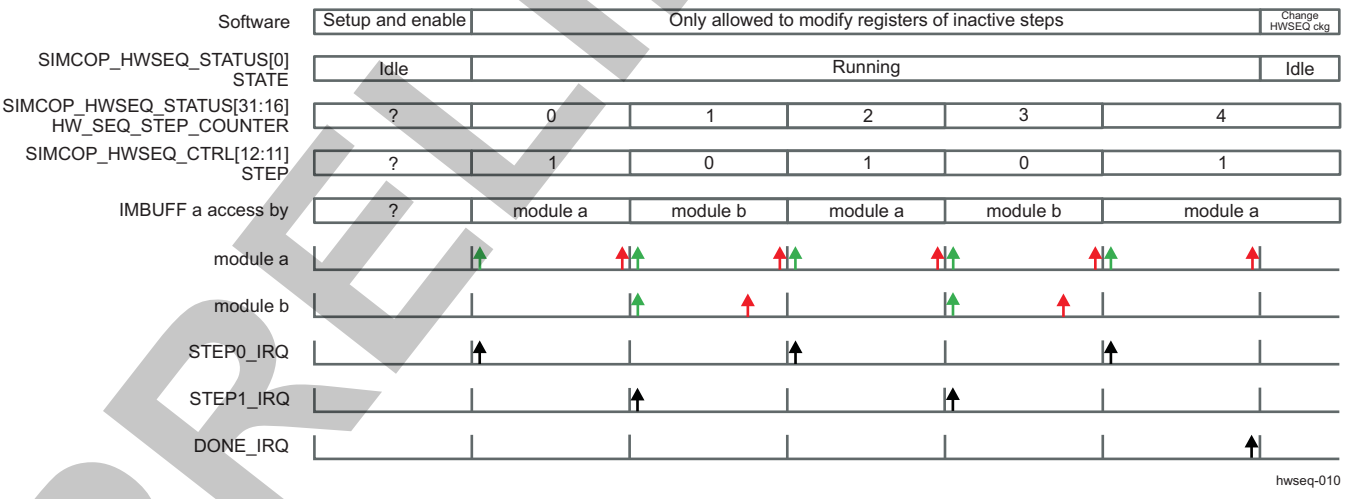
The SIMCOP can execute one hardware sequence at the time. However, software can be used to execute multiple independent sequences in parallel (that is, two unrelated macroblock pipelines) using the override feature.

The hardware sequencer has no specific support for macroblock pipeline filling (pipe-up) or flushing (pipe-down). It needs some software intervention.

The hardware sequencer supports sequences composed of up to four steps. Longer sequences require software intervention.

Figure 8-265 illustrates the hardware sequencer operation.

Figure 8-266. Hardware Sequencer Operation Example



The example involves utilization of two SIMCOP modules (or DMA channels) that are synchronized using the hardware sequencer. A total of five sequencing steps are executed (SIMCOP_HWSEQ_CTRL[31:6] HW_SEQ_STEP_COUNTER=5). The sequence is 2 steps long and starts with Step 1. Those two steps are configured using the SIMCOP_HWSEQ_STEP_*_i registers(where i = 0 and 1).

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The SIMCOP modules processing is started using START pulses (green). When the SIMCOP modules are done, they return a DONE pulse (red). Software can choose which accelerators to run for a given step using the SIMCOP_HWSEQ_STEP_CTRL_i[7:0] *_SYNC registers. They do not need to finish at the same time because the hardware sequencer waits for reception of all DONE pulses of used accelerators before moving to the next step.

The hardware sequencer also triggers a series of interrupts that can be used by software. It is possible, for example, for software to change the configuration of inactive sequencing steps. This can be particularly useful to run longer sequences than what is supported by hardware.

For example, software can setup a 4-step long looping sequence: Step 0 → 1 → 2 → 3 → 0 → 1 → .... When the STEP1_IRQ event is triggered, software can load the configuration to be used next time Step 0 becomes active in the SIMCOP_HWSEQ_STEP_*_i registers.

8.4.2.3.5.2 Hardware Sequencer Override

By default, the hardware sequencer controls START/DONE pulses of all SIMCOP modules as well as the static controlled crossbar. Software can take the control over some resources by setting the appropriate bits in the SIMCOP_HWSEQ_OVERRIDE register. Sequencing resources under software control are managed using the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE registers.

Changes done to the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE[27:11] *_OFST and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE registers have immediate effect. It is the responsibility of software to ensure there is no active traffic on the impacted connection in the static controlled crossbar.

For example, when software wants to alternatively attach image buffers a and b to SIMCOP_DMA while preserving the buffer start address in the SIMCOP DMA address map constant it sets:

- SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[2:0] IMBUFF_A = 1
- SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[6:4] IMBUFF_B = 1

for the full application duration. It then changes the SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[2:0] IMBUFF_A and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[6:4] IMBUFF_B registers to attach the image buffers to the correct SIMCOP submodule.

The settings in the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE registers for resources controlled by the hardware sequencer have no effect.

Synchronization with SIMCOP submodules is controlled using the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE[7:0] *_TRIGGER bit fields. For the ROT, VLCDJ, DCT, and LDC, a START pulse is sent to the module when a 1 is written into the appropriate bit field. Software can trigger one or multiple start pulses at the time. The *_TRIGGER bit field is cleared by writing 1. It is automatically set by hardware when a DONE pulse is received from the relevant SIMCOP submodule.

Software can poll the status of the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE[7:0] *_TRIGGER bit fields to detect when a SIMCOP module has completed its processing task. Alternatively, software can also use an interrupt. SIMCOP has the capability to merge one or multiple internal events into SIMCOP outgoing interrupts. Software can choose between two modes for each interrupt output (SIMCOP_CTRL[3:0] IRQx_MODE):

- 0x0 : OR, the interrupt is asserted when one of the selected events has occurred
- 0x1 : AND, the interrupt is asserted when all selected events have occurred

The AND mode leads to a lower initiator load. In fact, the initiator is only interrupted once per sequencing step even when events from multiple SIMCOP submodules are expected. Also, it does not need to poll the SIMCOP_HL_IRQSTATUS_i register to detect which events have occurred, it simply needs to write 0xFFFFFFF into the SIMCOP_HL_IRQSTATUS_i register to clear all pending events.

The SIMCOP DMA START/DONE control is slightly different. Software can trigger one or multiple DMA channels by writing into the SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE[7:5] DMA_TRIGGER bit field. The DMA_TRIGGER bit field returns the written value when all expected DONE pulses have been received from SIMCOP DMA.

Alternatively, SIMCOP modules (except the LDC) may be triggered by direct writes into their configuration registers. However, this approach lead to higher initiator load because multiple writes must be done.

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8.4.2.4 ISS SIMCOP Hardware Sequencer and Buffers Basic Programming Model

8.4.2.4.1 ISS SIMCOP Hardware Sequencer and Buffers Application Programming Principle

Software must first configure the SIMCOP access tag handling (SIMCOP_CTRL[24:21] LDC_R_TAG_CNT, SIMCOP_CTRL[19:16] LDC_R_TAG_OFST, and SIMCOP_DMA_CTRL[7:4] TAG_CNT). Software must ensure there is no active traffic on the SIMCOP master port before changing those registers.

Then it initializes the Huffman, Quantization, and LDC LUT if they are used. Those memories must first be attached to the SIMCOP bus so that they can be accessed from the slave port (SIMCOP_CTRL[11] HUFF, SIMCOP_CTRL[10] QUANT, and SIMCOP_CTRL[7:6] LDC_LUT). Then they can be preloaded using either an external CPU or an external DMA engine. SIMCOP DMA cannot preload those tables.

Similarly, software can also preload data like filter coefficients into image buffers. This can be handled by the SIMCOP DMA:

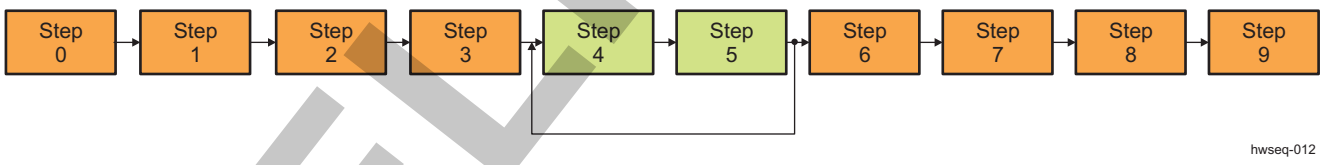
- The buffers must first be attached to the SIMCOP DMA using the SIMCOP_HWSEQ_OVERRIDE and SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE registers.
- Alternatively, software can use the SIMCOP_HWSEQ_STEP_*_0 registers instead of the override feature. The hardware sequencer ensures that the configuration of Step 0 is applied when the hardware sequencer is disabled.
- Software then configures and starts one or multiple data transfers using the SIMCOP DMA.
- Software monitors SIMCOP DMA events to know when DMA transfers are complete. Other configuration tasks may happen concurrently, but software must ensure that transfers have completed before attaching the memories to another module.

It must then enable the modules going to be used.

Typically, the first and last steps of the macroblock pipeline are different from those in the middle of the pipeline. The hardware sequencer has no specific support for pipe-up and pipe-down. However, software cancut the sequence into smaller ones to still benefit from the hardware sequencing and to avoid software sequencing.

Figure 8-267 shows an example of a 10-step sequence involving two DMA transfers and three modules.

Figure 8-267. Typical Hardware Sequencer Controlled Sequencer With Pipe-Up and Pipe-Down



The macroblock pipeline is composed of a chain of three accelerators. Data between modules is exchanged using ping-pong buffering.

Pipe-up and pipe-down require four sequencing steps each. The main processing can be done with two steps.

Software configures the hardware sequencer with the four step pipe-up sequence. Each step is executed once. When pipe-up is done, the SIMCOP triggers the DONE_IRQ event.

Software then reconfigures the hardware sequencer for the two step main sequence. The number of steps is defined by the amount of data to process. When the main pipe is done, the SIMCOP triggers the DONE_IRQ event.

Software finally reconfigures the hardware sequencer with the four step pipe-down sequence. Each step is executed once. When pipe-down is done, the SIMCOP triggers the DONE_IRQ event.

Figure 8-268 shows an example of pipe-up and pipe-done.

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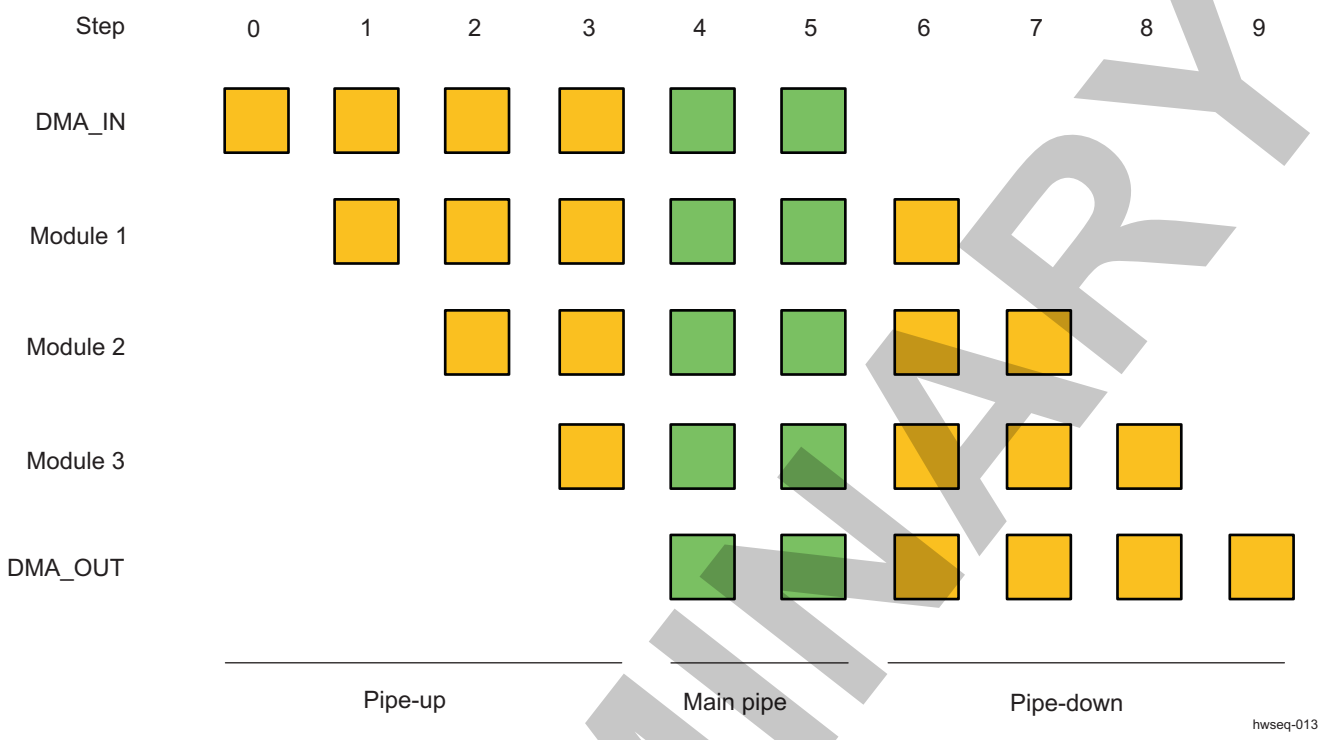
Figure 8-268. Pipe-Up and Pipe-Down



The hardware sequencer configuration determines which module can access a given SIMCOP memory for a sequence step.

8.4.2.4.2 External CPU Use for Data Processing

An external CPU can be used to perform some data processing as the SIMCOP hardware accelerators do. A similar mechanism to the START/DONE pulse interaction with the SIMCOP hardware accelerators is implemented.

The external CPU receives the request to start processing by the CPU_PROC_START_IRQ interrupt merged at the SIMCOP subsystem level. This interrupt is enabled and acknowledged as usual.

When processing has completed, the CPU generates the DONE pulse to the hardware sequencer by writing 1 into the SIMCOP_HWSEQ_CTRL[10] CPU_PROC_DONE register.

8.4.2.4.3 Rotation Operational Mode Configuration

The macroblock pipeline is controlled by a two step hardware sequence:

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Figure 8-269. Rotation Macroblock Pipeline

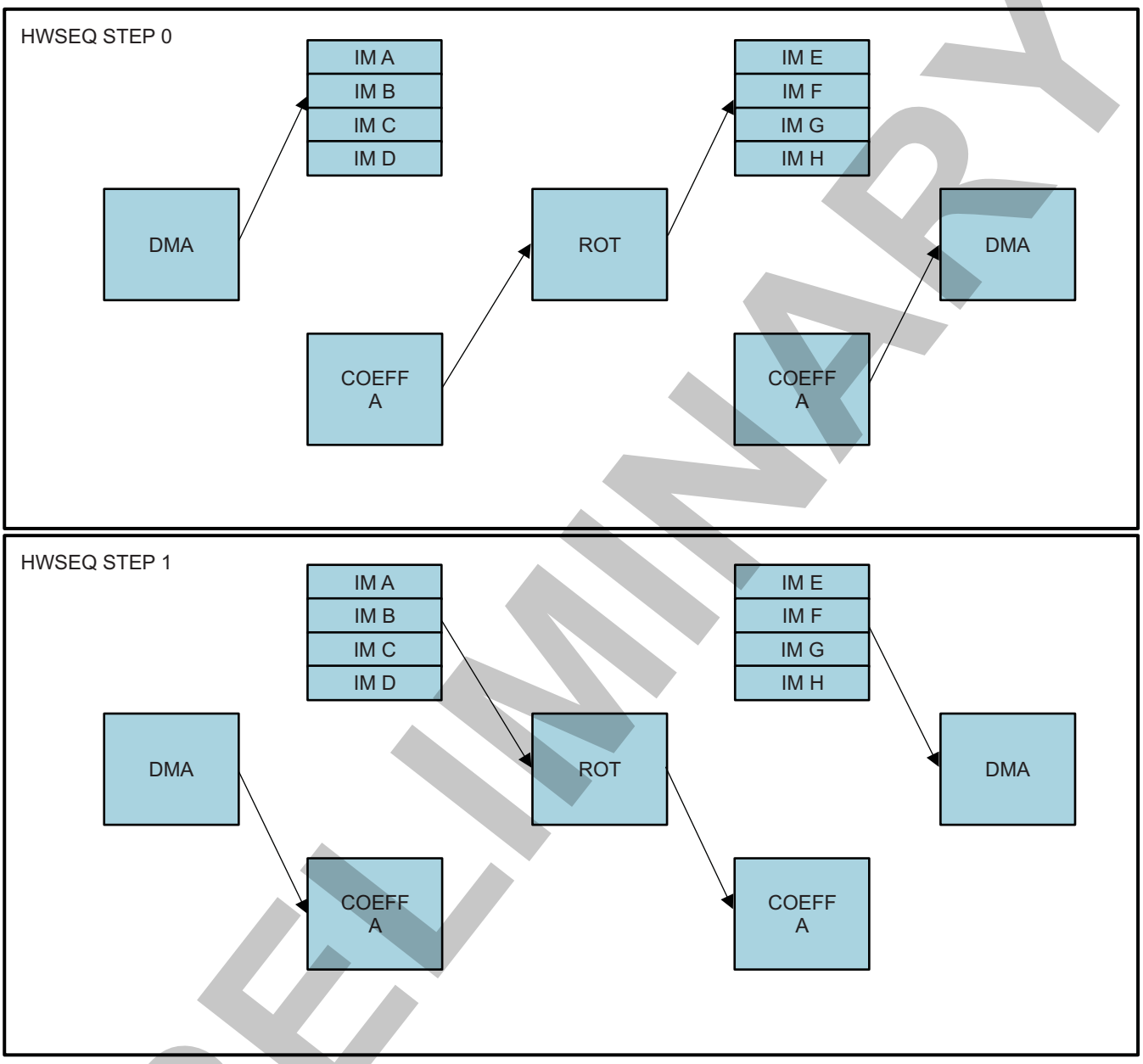

Table 8-1388. Rotation Macro-Block Pipeline

Step	Register/ Bitfield / Programming Model	Value
Set DMA to access IMBUFF_A	SIMCOP_HWSEQ_STEP_SWITCH_i[2:0] IMBUFF_A (i = 0)	0x1
Set ROT_A_O to access IMBUFF_E	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_E (i = 0)	0x7
Set ROT_A_I to access COEFF_A	SIMCOP_HWSEQ_STEP_CTRL2_i[2:0] = COEFF_A (i = 0)	0x6
Set DMA to access COEFF_B	SIMCOP_HWSEQ_STEP_CTRL2_i[6:4] COEFF_B (i = 0)	0x1
Set ROT_A_I to access IMBUFF_A	SIMCOP_HWSEQ_STEP_SWITCH_i[2:0] IMBUFF_A (i = 1)	0x6

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Table 8-1388. Rotation Macro-Block Pipeline (continued)

Step	Register/ Bitfield / Programming Model	Value
Set DMA to access IMBUFF_E	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_E (i = 1)	0x1
Set DMA to access COEFF_A	SIMCOP_HWSEQ_STEP_CTRL2_i[2:0] COEFF_A (i = 1)	0x1
Set ROT_A_O to access COEFF_B	SIMCOP_HWSEQ_STEP_CTRL2_i[6:4] COEFF_B (i = 1)	0x6

8.4.2.4.4 LDC Operational Mode Configuration

The LDC module fetches data from system memory, performs the transformation, and stores results into image buffers. The DCT and VLCDJ modules are used to JPEG compress this data and store the results to the BITSTREAM buffer. The SIMCOP DMA is used to transfer compressed data from the BITSTREAM buffer to system memory.

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Figure 8-270. LDC Transformation Pipeline

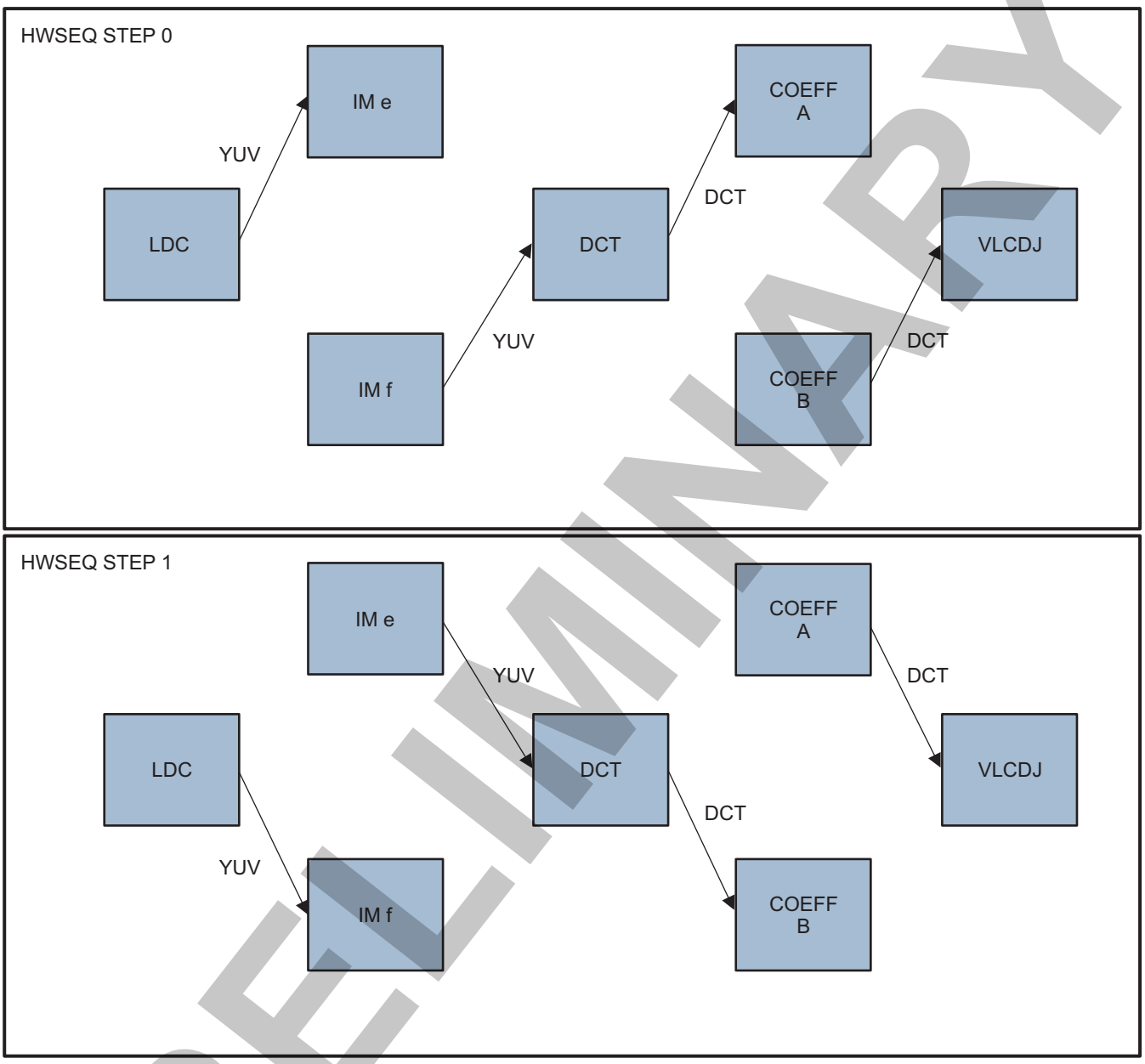

Table 8-1389. LDC Transformation

Step	Register/ Bitfield / Programming Model	Value
Set image buffers a and b as input buffer	SIMCOP_CTRL[7:6] LDC_INPUT	0x1
Set LDC to access the image buffer e	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_E	0x6
Set DCT to access coefficient buffer a	SIMCOP_HWSEQ_STEP_CTRL2_i[2:0] COEFF_A	0x5
Set VLCDJ_IO to access coefficient buffer b	SIMCOP_HWSEQ_STEP_CTRL2_i[6:4] COEFF_B	0x4
Set DCT to access the image buffer e	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_E	0x4
Set LDC to access the image buffer f	SIMCOP_HWSEQ_STEP_SWITCH_i[18:16] IMBUFF_F	0x6
Set VLCDJ_IO to access coefficient buffer a	SIMCOP_HWSEQ_STEP_CTRL2_i[2:0] COEFF_A	0x4

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Table 8-1389. LDC Transformation (continued)

Step	Register/ Bitfield / Programming Model	Value
Set DCT to access coefficient buffer b	SIMCOP_HWSEQ_STEP_CTRL2_i[6:4] COEFF_B	0x5

8.4.2.4.5 Concurrent Software and Hardware Sequencing

Software can perform sequencing tasks concurrently to hardware sequencing. This is supported through the hardware sequencer override registers:

- SIMCOP_HWSEQ_OVERRIDE
- SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE
- SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE
- SIMCOP_HWSEQ_STEP_CTRL2_OVERRIDE

  Software can select which hardware resources are controlled by the hardware sequencer and what resources are controlled by software. Configuration parameters for software-controlled resources are provided using those registers as well.

Table 8-1390. Concurrent Software and Hardware Sequencing

Step	Register/ Bitfield / Programming Model	Value
Set software to control IMBUFF_E	SIMCOP_HWSEQ_OVERRIDE[13] IMBUFF_E	0x1
Set DMA to access the image buffer e	SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[18:16] IMBUFF_E	0x1
Set software to control IMBUFF_F	SIMCOP_HWSEQ_OVERRIDE[14] IMBUFF_F	0x1
Set DCT_S to access the image buffer f	SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE[22:20] IMBUFF_F	0x4
Set software to control COEFF_A	SIMCOP_HWSEQ_OVERRIDE[17] COEFF_A	0x1
Set hardware sequencer to control COEFF_B	SIMCOP_HWSEQ_OVERRIDE[18] COEFF_B	0x0

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8.4.2.5 ISS SIMCOP Hardware Sequencer and Buffer Registers Manual

8.4.2.5.1 Hardware Sequencer Instance Summary

Table 8-1391 summarizes the Hardware Sequencer instance.

Table 8-1391. SIMCOP Instance Summary

Module Name	L3_MAIN Base Address	IPU Base Address	Size
HWSEQ	0x5202 0000	0x5506 0000	256 Bytes

8.4.2.5.2 Hardware Sequencer Registers

8.4.2.5.2.1 Hardware Sequencer Register Summary

Table 8-1392. HWSEQ Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address	IPU Physical Address
SIMCOP_HWSEQ_CTRL	RW	32	0x0000 0068	0x5202 0068	0x5506 0068
SIMCOP_HWSEQ_STATUS	RO	32	0x0000 006C	0x5202 006C	0x5506 006C
SIMCOP_HWSEQ_OVERRIDE	RW	32	0x0000 0070	0x5202 0070	0x5506 0070
SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE	RW	32	0x0000 0074	0x5202 0074	0x5506 0074
SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE	RW	32	0x0000 0078	0x5202 0078	0x5506 0078
SIMCOP_HWSEQ_STEP_CTRL2_OVERRIDE	RW	32	0x0000 007C	0x5202 007C	0x5506 007C
SIMCOP_HWSEQ_STEP_CTRL_i (1)	RW	32	0x0000 0080 + (0x10 * i)	0x5202 0080 + (0x10 * i)	0x5506 0080 + (0x10 * i)
SIMCOP_HWSEQ_STEP_SWITCH_i (1)	RW	32	0x0000 0084 + (0x10 * i)	0x5202 0084 + (0x10 * i)	0x5506 0084 + (0x10 * i)
SIMCOP_HWSEQ_STEP_CTRL2_i (1)	RW	32	0x0000 008C + (0x10 * i)	0x5202 008C + (0x10 * i)	0x5506 008C + (0x10 * i)

(1) i = 0 to 3

8.4.2.5.2.2 Hardware Sequencer Register Description

through describe the registers in detail.

Table 8-1393. SIMCOP_HWSEQ_CTRL

Address Offset	0x0000 0068		
Physical Address	0x5202 0068 0x5506 0068	**Instance**	HWSEQ_MAIN_L3 HWSEQ_IPU
Description	SIMCOP HW sequencer control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SEQ_STEP_COUNTER																RESERVED			STEP		CPU_PROC_DONE		BBM_SYNC_CHAN	BBM_STATUS			BITSTREAM				BITSTR_XFER_SIZE		HW_SEQ_STOP	HW_SEQ_START

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Bits	Field Name	Description	Type	Reset
31:16	HW_SEQ_STEP_COUNTER	Number of steps executed by the HW sequencer. HW_SEQ_STEP_COUNTER=0 corresponds to manual sequencing.	RW	0x0000
15:13	RESERVED	Read returns 0.	R	0x0
12:11	STEP	This register is automatically updated by the HW sequencer when it is active. Otherwise, SW could use it to activate the content of a given set of step registers (SIMCOP_HWSEQ_STEP_i).	RW	0x0
10	CPU_PROC_DONE	Used by the CPU to tell that it has completed data processing. This feature should be used together with the CPU_PROC_START_IRQ event Read's always return 0. Write 0x0: No effect. Write 0x1: CPU processing completed.	W	0
9:8	BBM_SYNC_CHAN	Defines the SIMCOP DMA HW synchronization channel to be used for BBM. This register is only used when BITSTREAM=ENCODE or DECODE. SW must ensure that the same DMA HW synchronization channel isn't used by the HW sequencer.	RW	0x0
7	BBM_STATUS	Status of the Bitstream buffer management HW. Used only during automatic mode [BITSTREAM=5 or 6] Equals 0 (IDLE) in manual mode [BITSTREAM=0..4]. Set when automatic mode is entered. Automatic encode mode: used to detect when all banks have been flushed after the processing has completed (i.e. but request bank signals have been de-asserted by BBM). Automatic decode mode (BITSTREAM=DECODE): returns to 0 (IDLE) when automatic mode is left (BITSTREAM=COPR). Read 0x1: BBM is busy. Read 0x0: BBM is idle	R	0
6:4	BITSTREAM	BITSTREAM buffer access control 0x0: Bank 0: coprocessor bus (0x1000-0x17FF) Bank 1: coprocessor bus (0x1800-0x1FFF) 0x1: Bank 0: DMA (0x1000-0x17FF) Bank 1: DMA (0x1800-0x1FFF) 0x2: Bank 0: VLCDJ.B (0x000-0x7FF) Bank 1: VLCDJ.B (0x800-0xFFF) 0x3: Bank 0: DMA (0x1000-0x17FF) Bank 1: VLCDJ.B (0x800-0xFFF) 0x4: Bank 0: VLCDJ.B (0x000-0x7FF) Bank 1: DMA (0x1800-0x1FFF) 0x5: The BITSTREAM buffer is managed by HW as a PING/PONG buffer to support JPEG encode use case. It could be accessed by the SIMCOP DMA or the VLCDJ module. The BITSTREAM HW sequence is reset when the mode is changed to COPR, VLCDJ or DMA. 0x6: The BITSTREAM buffer is managed by HW as a PING/PONG buffer to support JPEG decode use case. It could be accessed by the SIMCOP DMA or the VLCDJ module. The BITSTREAM HW sequence is reset when the mode is changed to COPR, VLCDJ or DMA.	RW	0x0

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Bits	Field Name	Description	Type	Reset
3:2	BITSTR_XFER_SIZE	Defines the amount of data to be transferred per HW request to the SIMCOP DMA. Bigger sizes lead to better SDRAM efficiency but prevents fine grained DMA transfer arbitration. This register is only used by HW when BITSTREAM=ENCODE or BITSTREAM=DECODE. 0x0: 2048 bytes 0x1: 1024 bytes 0x2: 512 bytes 0x3: 256 bytes	RW	0x0
1	HW_SEQ_STOP	Stop the HW sequencer. This feature is typically used to recover from an error condition. Read's always return 0. Write 0x0: No effect. Write 0x1: Stop the HW sequence immediately (don't wait for expected DONE events). Setting this bit while the sequencer is idle has no effect.	W	0
0	HW_SEQ_START	Start the HW sequencer. Read's always return 0. Write 0x0: No effect. Write 0x1: Start STEP0 of the HW sequence. Setting this bit while the sequencer is running has no effect.	W	0

Table 8-1394. Register Call Summary for Register SIMCOP_HWSEQ_CTRL

ISS SIMCOP Hardware Sequencer and Buffers Module

- Overview: [1] [2] [3] [4] [5]
- Automatic BITSTREAM Buffer Management: [6] [7]
- Automatic Operation: [11] [12] [13]
- External CPU Use for Data Processing: [14]
- Hardware Sequencer Register Summary: [15]

Table 8-1395. SIMCOP_HWSEQ_STATUS

Address Offset	0x0000 006C		
Physical Address	0x5202 006C 0x5506 006C	**Instance**	HWSEQ_MAIN_L3 HWSEQ_IPU
Description	HW sequencer status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SEQ_STEP_COUNTER																RESERVED															STATE

Bits	Field Name	Description	Type	Reset
31:16	HW_SEQ_STEP_COUNTER	Current step number	R	0x0000
15:1	RESERVED	Read returns 0.	R	0x0000
0	STATE	Current state Read 0x0: Idle Read 0x1: Running	R	0

Table 8-1396. Register Call Summary for Register SIMCOP_HWSEQ_STATUS

ISS SIMCOP Hardware Sequencer and Buffers Module

- Hardware Sequencer Register Summary: [0]

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Table 8-1397. SIMCOP_HWSEQ_OVERRIDE

Address Offset	0x0000 0070		
Physical Address	0x5202 0070 0x5506 0070	**Instance**	HWSEQ_MAIN_L3 HWSEQ_IPU
Description	HW sequencer override control register. Bits in this register select what configuration register control a resource. 0: Resource controlled by HW sequencer. HW uses the value from SIMCOP_HWSEQ_STEP_xx registers for the chosen resource 1: Resource controlled by SW HW uses the value from SIMCOP_HWSEQ_STEP_x_OVERRIDE registers for the chosen resource The bit field name matches the one of the resource.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													COEFF_B	COEFF_A	IMBUFF_H	IMBUFF_G	IMBUFF_F	IMBUFF_E	IMBUFF_D	IMBUFF_C	IMBUFF_B	IMBUFF_A	LDC_O_OFST_OVR	ROT_O_OFST_OVR	ROT_I_OFST_OVR	RESERVED	DCT_F_OFST_OVR	DCT_S_OFST_OVR	VLCDJ_IO_OFST_OVR	RESERVED		

Table 8-1398. Register Call Summary for Register SIMCOP_HWSEQ_OVERRIDE

ISS SIMCOP Hardware Sequencer and Buffers Module

- Hardware Sequencer Override: [0]
- ISS SIMCOP Hardware Sequencer and Buffers Application Programming Principle: [1]
- Concurrent Software and Hardware Sequencing: [2] [3] [4] [5] [6]
- Hardware Sequencer Register Summary: [7]

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Read returns 0.	R	0x0
18	COEFF_B	See register description	RW	0
17	COEFF_A	See register description	RW	0
16	IMBUFF_H	See register description	RW	0
15	IMBUFF_G	See register description	RW	0
14	IMBUFF_F	See register description	RW	0
13	IMBUFF_E	See register description	RW	0
12	IMBUFF_D	See register description	RW	0
11	IMBUFF_C	See register description	RW	0
10	IMBUFF_B	See register description	RW	0
9	IMBUFF_A	See register description	RW	0
8	LDC_O_OFST_OVR	See register description	RW	0
7	ROT_O_OFST_OVR	See register description	RW	0
6	ROT_I_OFST_OVR	See register description	RW	0
5	RESERVED	Read returns 0.	R	0
4	DCT_F_OFST_OVR	See register description	RW	0
3	DCT_S_OFST_OVR	See register description	RW	0
2	VLCDJ_IO_OFST_OVR	See register description	RW	0
1:0	RESERVED	Read returns 0.	R	0

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Table 8-1399. SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE

Address Offset	0x0000 0074		
Physical Address	0x5202 0074 0x5506 0074	**Instance**	HWSEQ_MAIN_L3 HWSEQ_IPU
Description	HW sequencer override register. Used to execute SW sequences in parallel to HW sequencing steps		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ROT_O_OFST		ROT_I_OFST		RESERVED		DCT_F_OFST		DCT_S_OFST		VLCDJ_IO_OFST		RESERVED								DMA_TRIGGER			ROT_A_TRIGGER	RESERVED		VLCDJ_TRIGGER	DCT_TRIGGER	LDC_TRIGGER

Table 8-1400. Register Call Summary for Register SIMCOP_HWSEQ_STEP_CTRL_OVERRIDE

ISS SIMCOP Hardware Sequencer and Buffers Module

- Hardware Sequencer Override: [0] [1] [2] [3] [4] [5]
- Concurrent Software and Hardware Sequencing: [6]
- Hardware Sequencer Register Summary: [7]
- Hardware Sequencer Register Description:

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:26	ROT_O_OFST	Controls ROT.O bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: EFGH 0x1: FGHE 0x2: GHEF 0x3: HEFG	RW	0x0
25:24	ROT_I_OFST	Controls ROT_I bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDA 0x2: CDAB 0x3: DABC	RW	0x0
23	RESERVED	Read returns 0.	R	0
22:20	DCT_F_OFST	Controls DCT.F bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDG 0x2: CDGH 0x3: DGHA 0x4: GHAB 0x5: HABC	RW	0x0
19:18	DCT_S_OFST	Controls DCT.S bus mapping to image buffers: 0x0000 0x1000 0x0: EF 0x1: FG 0x2: GH 0x3: HE	RW	0x0

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Bits	Field Name	Description	Type	Reset
17:15	VLCDJ_IO_OFST	Controls VLCDJ IO data bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDG 0x2: CDGH 0x3: DGHA 0x4: GHAB 0x5: HABC	RW	0x0
14:8	RESERVED	Read returns 0.	R	0x0
7:5	DMA_TRIGGER	SW controlled START/DONE synchronization Write 0x0: No effect Read 0x0: No done pulse have been received since last non zero write into the DMA_TRIGGER register Read 0x1: DONE pulses for channel 0 and 1 have been received Write 0x1: Trigger channel 0 and 1. Clears all memorized done pulses for DMA. Write 0x2: Trigger channel 0, 1, 2. Clears all memorized done pulses for DMA. Read 0x2: DONE pulses for channel 0, 1 and 2 have been received Read 0x3: DONE pulses for channel 0, 1, 2 and 3 have been received. Write 0x3: Trigger channel 0, 1, 2 and 3. Clears all memorized done pulses for DMA. Read 0x4: DONE pulse for channel 0 has been received Write 0x4: Trigger channel 0. Clears all memorized done pulses for DMA. Write 0x5: Trigger channel 1. Clears all memorized done pulses for DMA. Read 0x5: DONE pulse for channel 1 has been received Read 0x6: DONE pulse for channel 2 has been received Write 0x6: Trigger channel 2. Clears all memorized done pulses for DMA. Write 0x7: Trigger channel 3. Clears all memorized done pulses for DMA. Read 0x7: DONE pulse for channel 3 has been received	RW	0x0
4	ROT_A_TRIGGER	SW controlled START/DONE synchronization Write 0x0: No Effect Read 0x0: No DONE pulse received since the last START pulse has been sent Read 0x1: DONE pulse received Write 0x1: Send a start pulse and clears the memorized done pulse	RW	0
3	RESERVED	Read returns 0.	R	0
2	VLCDJ_TRIGGER	SW controlled START/DONE synchronization Write 0x0: No Effect Read 0x0: No DONE pulse received since the last START pulse has been sent Read 0x1: DONE pulse received Write 0x1: Send a start pulse and clears the memorized done pulse	RW	0

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Bits	Field Name	Description	Type	Reset
1	DCT_TRIGGER	SW controlled START/DONE synchronization Write 0x0: No Effect Read 0x0: No DONE pulse received since the last START pulse has been sent Read 0x1: DONE pulse received Write 0x1: Send a start pulse and clears the memorized done pulse	RW	0
0	LDC_TRIGGER	SW controlled START/DONE synchronization Write 0x0: No Effect Read 0x0: No DONE pulse received since the last START pulse has been sent Read 0x1: DONE pulse received Write 0x1: Send a start pulse and clears the memorized done pulse	RW	0

Table 8-1401. SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE

Address Offset	0x0000 0078		
Physical Address	0x5202 0078 0x5506 0078	**Instance**	HWSEQ_MAIN_L3 HWSEQ_IPU
Description	HW sequencer override register. Used to execute SW sequences in parallel to HW sequencing steps		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMBUFF_H				IMBUFF_G				RESERVED	IMBUFF_F			RESERVED	IMBUFF_E			RESERVED	IMBUFF_D			RESERVED	IMBUFF_C			RESERVED	IMBUFF_B			RESERVED	IMBUFF_A		

Bits	Field Name	Description	Type	Reset
31:28	IMBUFF_H	Switch for image buffer h 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: VLCDJ_IO 0x5: DCT_S 0x6: DCT_F 0x7: ROT_A_O 0x9: LDC_O	RW	0x0
27:24	IMBUFF_G	Switch for image buffer g 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: VLCDJ_IO 0x5: DCT_S 0x6: DCT_F 0x7: ROT_A_O 0x9: LDC_O	RW	0x0
23:20	IMBUFF_F	Switch for image buffer f 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: DCT_S 0x6: LDC_O	RW	0x0

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Bits	Field Name	Description	Type	Reset
		0x7: ROT_A_O		
19:16	IMBUFF_E	Switch for image buffer e	RW	0x0
		0x0: Coprocessor bus		
		0x1: SIMCOP DMA		
		0x4: DCT_S		
		0x6: LDC_O		
		0x7: ROT_A_O		
15	RESERVED	Read returns 0.	R	0
14:12	IMBUFF_D	Switch for image buffer d	RW	0x0
		0x0: Coprocessor bus		
		0x1: SIMCOP DMA		
		0x4: VLCDJ_IO		
		0x5: DCT_F		
		0x6: ROT_A_I		
		0x7: Reserved		
11	RESERVED	Read returns 0.	R	0
10:8	IMBUFF_C	Switch for image buffer c	RW	0x0
		0x0: Coprocessor bus		
		0x1: SIMCOP DMA		
		0x4: VLCDJ_IO		
		0x5: DCT_F		
		0x6: ROT_A_I		
		0x7: Reserved		
7	RESERVED	Read returns 0.	R	0
6:4	IMBUFF_B	Switch for image buffer b	RW	0x0
		0x0: Coprocessor bus		
		0x1: SIMCOP DMA		
		0x4: VLCDJ_IO		
		0x5: DCT_F		
		0x6: ROT_A_I		
		0x7: Reserved		
3	RESERVED	Read returns 0.	R	0
2:0	IMBUFF_A	Switch for image buffer a	RW	0x0
		0x0: Coprocessor bus		
		0x1: SIMCOP DMA		
		0x4: VLCDJ_IO		
		0x5: DCT_F		
		0x6: ROT_A_I		
		0x7: Reserved		

Table 8-1402. Register Call Summary for Register SIMCOP_HWSEQ_STEP_SWITCH_OVERRIDE

ISS SIMCOP Hardware Sequencer and Buffers Module

- Hardware Sequencer Override: [0] [1] [2] [3] [4] [5] [6]
- ISS SIMCOP Hardware Sequencer and Buffers Application Programming Principle: [7]
- Concurrent Software and Hardware Sequencing: [8] [9] [10]
- Hardware Sequencer Register Summary: [11]

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Table 8-1403. SIMCOP_HWSEQ_STEP_CTRL2_OVERRIDE

Address Offset	0x0000 007C		
Physical Address	0x5202 007C 0x5506 007C	**Instance**	HWSEQ_MAIN_L3 HWSEQ_IPU
Description	HW sequencer override register. Used to execute SW sequences in parallel to HW sequencing steps		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						LDC_O_OFST		RESERVED		COEFF_B			RESERVED		COEFF_A	

Table 8-1404. Register Call Summary for Register SIMCOP_HWSEQ_STEP_CTRL2_OVERRIDE

ISS SIMCOP Hardware Sequencer and Buffers Module

- Concurrent Software and Hardware Sequencing: [0]
- Hardware Sequencer Register Summary: [2]

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Read returns 0.	R	0x00000
9:8	LDC_O_OFST	Controls LDC.O bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: EFGH 0x1: FGHE 0x2: GHEF 0x3: HEFG	RW	0x0
7	RESERVED	Read returns 0.	R	0
6:4	COEFF_B	Coefficient buffer B switch 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: IMX A 0x3: IMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT A O 0x7: Reserved	RW	0x0
3	RESERVED	Read returns 0.	R	0
2:0	COEFF_A	Coefficient buffer a switch 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: IMX A 0x3: IMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT A I 0x7: Reserved	RW	0x0

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Table 8-1405. SIMCOP_HWSEQ_STEP_CTRL_i

Address Offset	0x0000 0080 + (0x10 * i)		
Physical Address	0x5202 0080 + (0x10 * i) 0x5506 0080 + (0x10 * i)	**Instance**	HWSEQ_MAIN_L3 HWSEQ_IPU
Description	HW sequencer step control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPU_SYNC	DMA_OFST			ROT_O_OFST		ROT_I_OFST		RESERVED	DCT_F_OFST			DCT_S_OFST		VLCDJ_IO_OFST		RESERVED					NEXT		RESERVED	DMA_SYNC			ROT_A_SYNC	RESERVED	VLCDJ_SYNC	DCT_SYNC	LDC_SYNC

Table 8-1406. Register Call Summary for Register SIMCOP_HWSEQ_STEP_CTRL_i

ISS SIMCOP Hardware Sequencer and Buffers Module

- Image Buffers: [0]
- Automatic Operation: [1] [2]
- Hardware Sequencer Register Summary: [3]
- Hardware Sequencer Register Description:

Bits	Field Name	Description	Type	Reset
31	CPU_SYNC	Enable HW synchronization with the CPU so that it could be used for some processing on in the macro-block pipeline. 0x0: Disabled 0x1: Enabled.	RW	0
30:28	DMA_OFST	Controls DMA bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x4000 0x5000 0x6000 0x7000 0x0: ABCDEFGH 0x1: BCDEFGHA 0x2: CDEFGHAB 0x3: DEFGHABC 0x4: EFGHABCD 0x5: FGHABCDE 0x6: GHABCDEF 0x7: HABCDEFG	RW	0x0
27:26	ROT_O_OFST	Controls ROT.O bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: EFGH 0x1: FGHE 0x2: GHEF 0x3: HEFG	RW	0x0
25:24	ROT_I_OFST	Controls ROT_I bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDA 0x2: CDAB 0x3: DABC	RW	0x0
23	RESERVED	Read returns 0.	R	0

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Bits	Field Name	Description	Type	Reset
22:20	DCT_F_OFST	Controls DCT.F bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDG 0x2: CDGH 0x3: DGHA 0x4: GHAB 0x5: HABC	RW	0x0
19:18	DCT_S_OFST	Controls DCT.S bus mapping to image buffers: 0x0000 0x1000 0x0: EF 0x1: FG 0x2: GH 0x3: HE	RW	0x0
17:15	VLCDJ_IO_OFST	Controls VLCDJ IO data bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: ABCD 0x1: BCDG 0x2: CDGH 0x3: DGHA 0x4: GHAB 0x5: HABC	RW	0x0
14:11	RESERVED	Read returns 0.	R	0x0
10:9	NEXT	Next channel in the sync chain 0x0: Step 0 0x1: Step 1 0x2: Step 2 0x3: Step 3	RW	0x0
8	RESERVED	Read returns 0.	R	0
7:5	DMA_SYNC	Enable HW synchronization with the SIMCOP DMA 0x0: Disabled 0x1: Channel 0 and 1 0x2: Channel 0, 1, 2 0x3: Channel 0, 1, 2 and 3 0x4: Channel 0 0x5: Channel 1 0x6: Channel 2 0x7: Channel 3	RW	0x0
4	ROT_A_SYNC	Enable HW synchronization with the ROT A module 0x0: Disabled 0x1: Enabled.	RW	0
3	RESERVED	Read returns 0.	R	0
2	VLCDJ_SYNC	Enable HW synchronization with the VLCDJ module 0x0: Disabled 0x1: Enabled.	RW	0
1	DCT_SYNC	Enable HW synchronization with the DCT module 0x0: Disabled 0x1: Enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
0	LDC_SYNC	Enable HW synchronization with the LDC module 0x0: Disabled 0x1: Enabled.	RW	0

Table 8-1407. SIMCOP_HWSEQ_STEP_SWITCH_i

Address Offset	0x0000 0084 + (0x10 * i)		
Physical Address	0x5202 0084 + (0x10 * i) 0x5506 0084 + (0x10 * i)	**Instance**	HWSEQ_MAIN_L3 HWSEQ_IPU
Description	Image buffer switch control. The configuration of Step 0 is used when HW sequencer is idle.		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
IMBUFF_H	IMBUFF_G	RESERVED IMBUFF_F	RESERVED IMBUFF_E	RESERVED IMBUFF_D	RESERVED IMBUFF_C	RESERVED IMBUFF_B	RESERVED IMBUFF_A

Bits	Field Name	Description	Type	Reset
31:28	IMBUFF_H	Switch for image buffer h 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: VLCDJ_IO 0x5: DCT_S 0x6: DCT_F 0x7: ROT_A_O 0x9: LDC_O	RW	0x0
27:24	IMBUFF_G	Switch for image buffer g 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: VLCDJ_IO 0x5: DCT_S 0x6: DCT_F 0x7: ROT_A_O 0x9: LDC_O	RW	0x0
23:20	IMBUFF_F	Switch for image buffer f 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: DCT_S 0x6: LDC_O 0x7: ROT_A_O	RW	0x0
19:16	IMBUFF_E	Switch for image buffer e 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: DCT_S 0x6: LDC_O 0x7: ROT_A_O	RW	0x0
15	RESERVED	Read returns 0.	R	0
14:12	IMBUFF_D	Switch for image buffer d 0x0: Coprocessor bus	RW	0x0

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Bits	Field Name	Description	Type	Reset
		0x1: SIMCOP DMA 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved		
11	RESERVED	Read returns 0.	R	0
10:8	IMBUFF_C	Switch for image buffer c 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved	RW	0x0
7	RESERVED	Read returns 0.	R	0
6:4	IMBUFF_B	Switch for image buffer b 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved	RW	0x0
3	RESERVED	Read returns 0.	R	0
2:0	IMBUFF_A	Switch for image buffer a 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT_A_I 0x7: Reserved	RW	0x0

Table 8-1408. Register Call Summary for Register SIMCOP_HWSEQ_STEP_SWITCH_i

ISS SIMCOP Hardware Sequencer and Buffers Module

- Static Crossbar: [1]
- Image Buffers: [2]
- Rotation Operational Mode Configuration: [3] [4] [5] [6]
- LDC Operational Mode Configuration: [7] [8] [9]
- Hardware Sequencer Register Summary: [10]

Table 8-1409. SIMCOP_HWSEQ_STEP_CTRL2_i

Address Offset	0x0000 008C + (0x10 * i)		
Physical Address	0x5202 008C + (0x10 * i) 0x5506 008C + (0x10 * i)	**Instance**	HWSEQ_MAIN_L3 HWSEQ_IPU
Description	HW sequencer step control register		
Type	RW		

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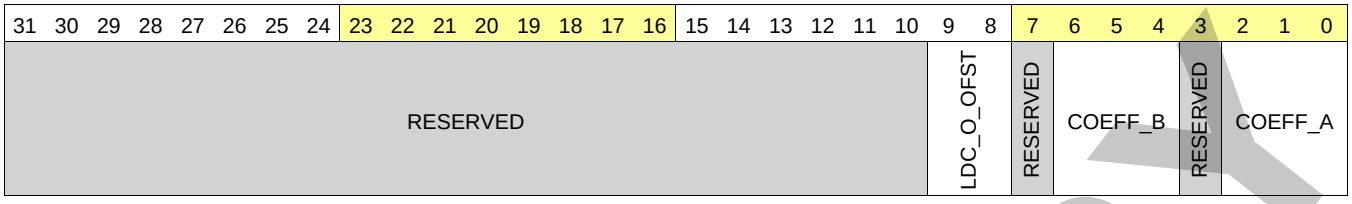

Table 8-1410. Register Call Summary for Register SIMCOP_HWSEQ_STEP_CTRL2_i

ISS SIMCOP Hardware Sequencer and Buffers Module

- Static Crossbar: [1]
- Rotation Operational Mode Configuration: [2] [3] [4] [5]
- LDC Operational Mode Configuration: [6] [7] [8] [9]
- Concurrent Software and Hardware Sequencing:
- Hardware Sequencer Register Summary: [11]

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Read returns 0.	R	0x00000
9:8	LDC_O_OFST	Controls LDC.O bus mapping to image buffers: 0x0000 0x1000 0x2000 0x3000 0x0: EFGH 0x1: FGHE 0x2: GHEF 0x3: HEFG	RW	0x0
7	RESERVED	Read returns 0.	R	0
6:4	COEFF_B	Coefficient buffer b switch 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: IMX A 0x3: IMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT A O 0x7: Reserved	RW	0x0
3	RESERVED	Read returns 0.	R	0
2:0	COEFF_A	Coefficient buffer a switch 0x0: Coprocessor bus 0x1: SIMCOP DMA 0x2: IMX A 0x3: IMX B 0x4: VLCDJ_IO 0x5: DCT_F 0x6: ROT A I 0x7: Reserved	RW	0x0

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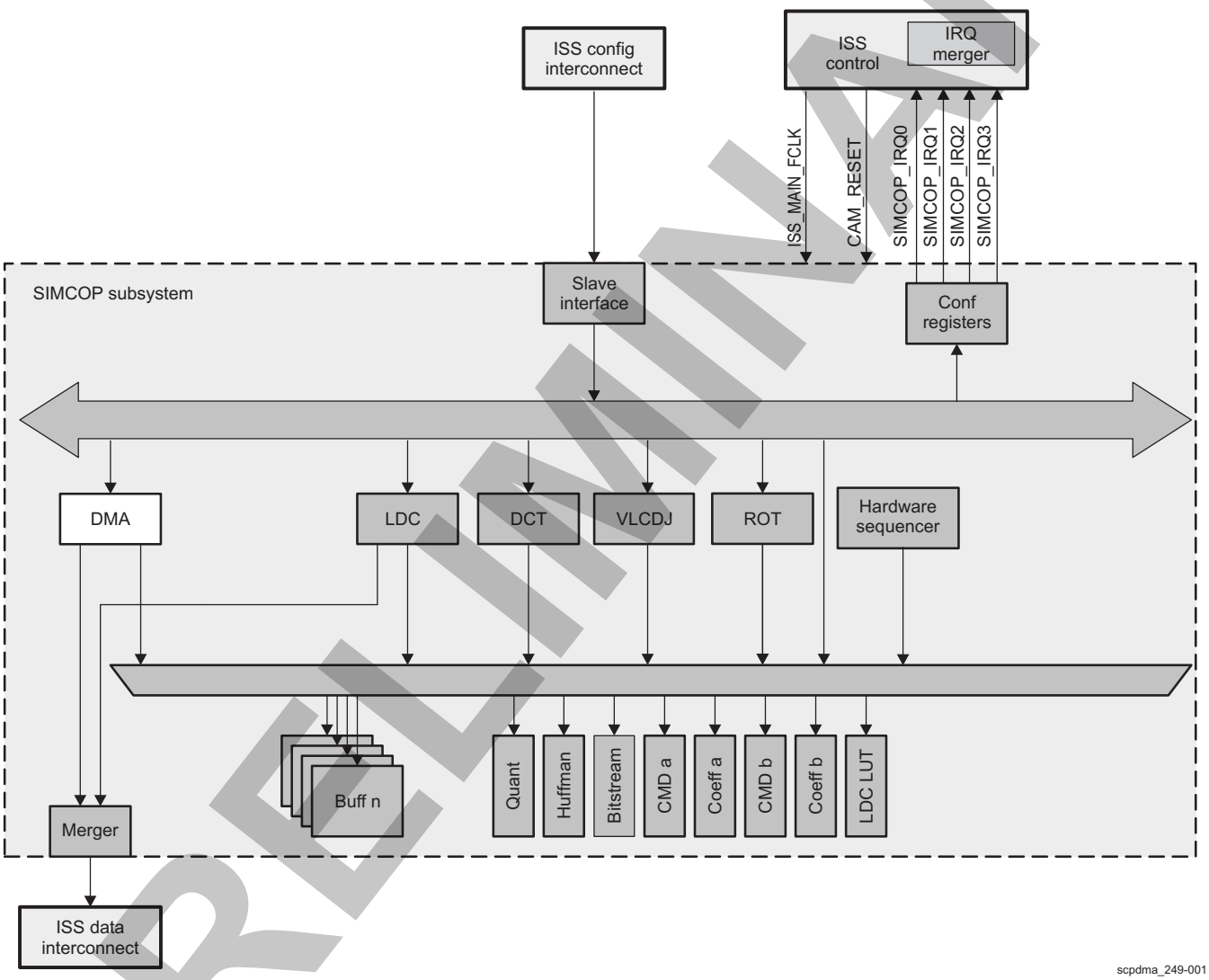
8.4.3 ISS SIMCOP DMA Module

This section describes the direct memory access (DMA) module in the still image coprocessor (SIMCOP) subsystem.

8.4.3.1 ISS SIMCOP DMA Overview

The direct memory access (DMA) module transfers data from system memory to the still image coprocessor (SIMCOP) memories and from SIMCOP memories. Figure 8-271 is an overview of the DMA module in the SIMCOP subsystem.

Figure 8-271. DMA in the SIMCOP Subsystem



The SIMCOP DMA supports the following features:

- Configuration interface, for register access
- Image subsystem (ISS) data interconnect master interface, for system memory access
  - Supports 1-dimensional (1D) and 2-dimensional (2D) burst
- SIMCOP crossbar master interface, for SIMCOP memories access
- Eight logical channels supported
- Hardware synchronization support
- 2-dimensional (2D) addressing transfers

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- 2D data block transfer (base address, stride, height, width)
- Array of 2D block transfer support
- Performance: Software-controllable bandwidth limiter

The SIMCOP DMA is not a general-purpose DMA. It can perform only 16-byte aligned transfers and does not have access to the ISS configuration interconnect. SDMA must be used instead.

8.4.3.2 ISS SIMCOP DMA Integration

The DMA module is part of the SIMCOP subsystem in the ISS. Figure 8-272 shows the integration of the DMA in the SIMCOP sybsystem.

Figure 8-272. DMA Engine Integration

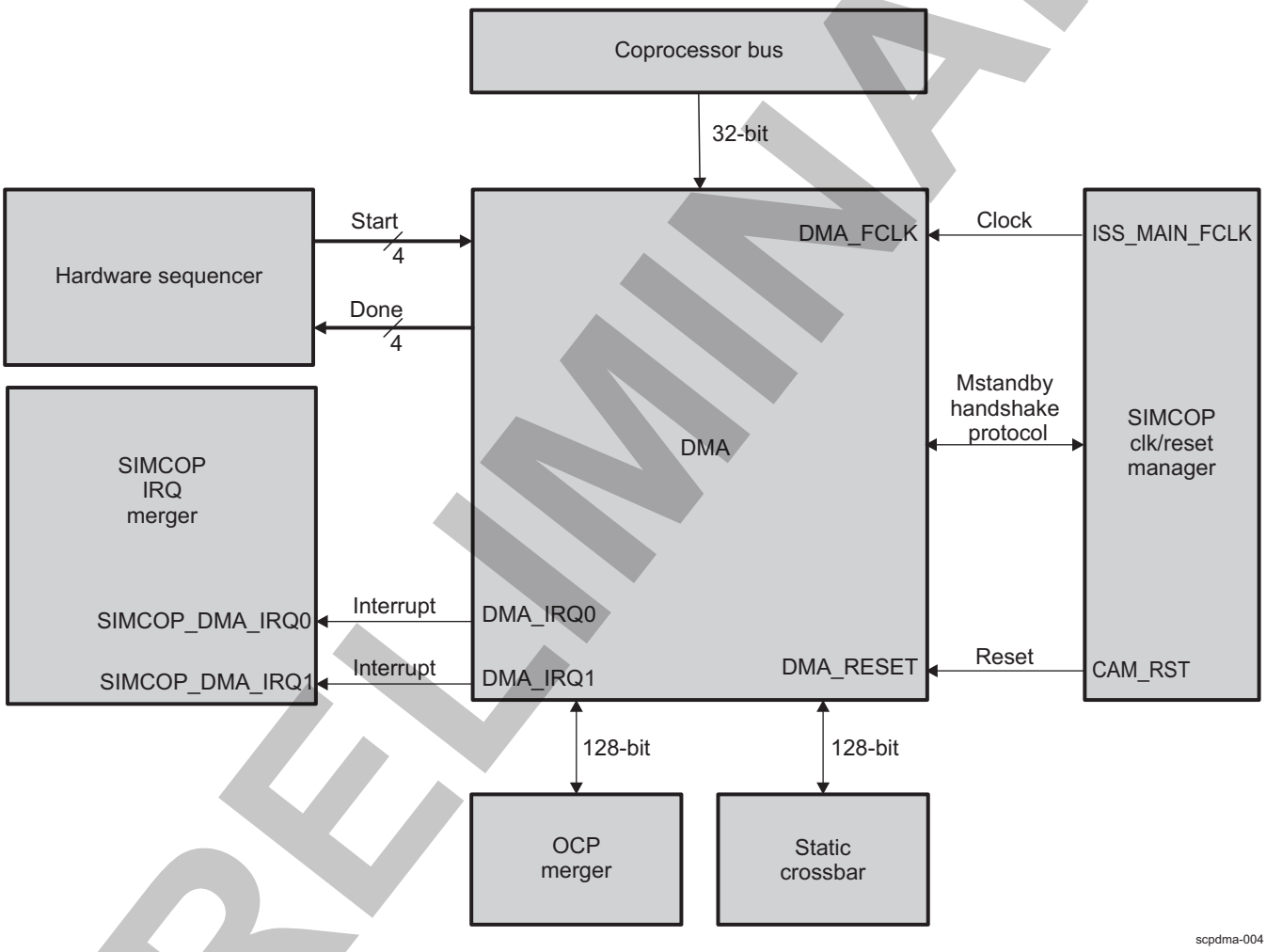

Table 8-1411. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
DMA	PD_CAM	

Table 8-1412. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description

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Table 8-1412. Clocks and Resets (continued)

DMA	DMA_FCLK	ISS_MAIN_FCLK	ISS	Functional clock provided by CORE_ISS_MAIN_CLK from PRCM . It is used by all ISS sub-modules and ISS top level resources.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMA	DMA_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

For information about clock and reset management, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

Table 8-1413. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DMA	DMA_IRQ0	SIMCOP_DMA_IRQ0	SIMCOP IRQ merger	Interrupt triggered by SIMCOP DMA
DMA	DMA_IRQ1	SIMCOP_DMA_IRQ1	SIMCOP IRQ merger	Interrupt triggered by SIMCOP DMA

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*.

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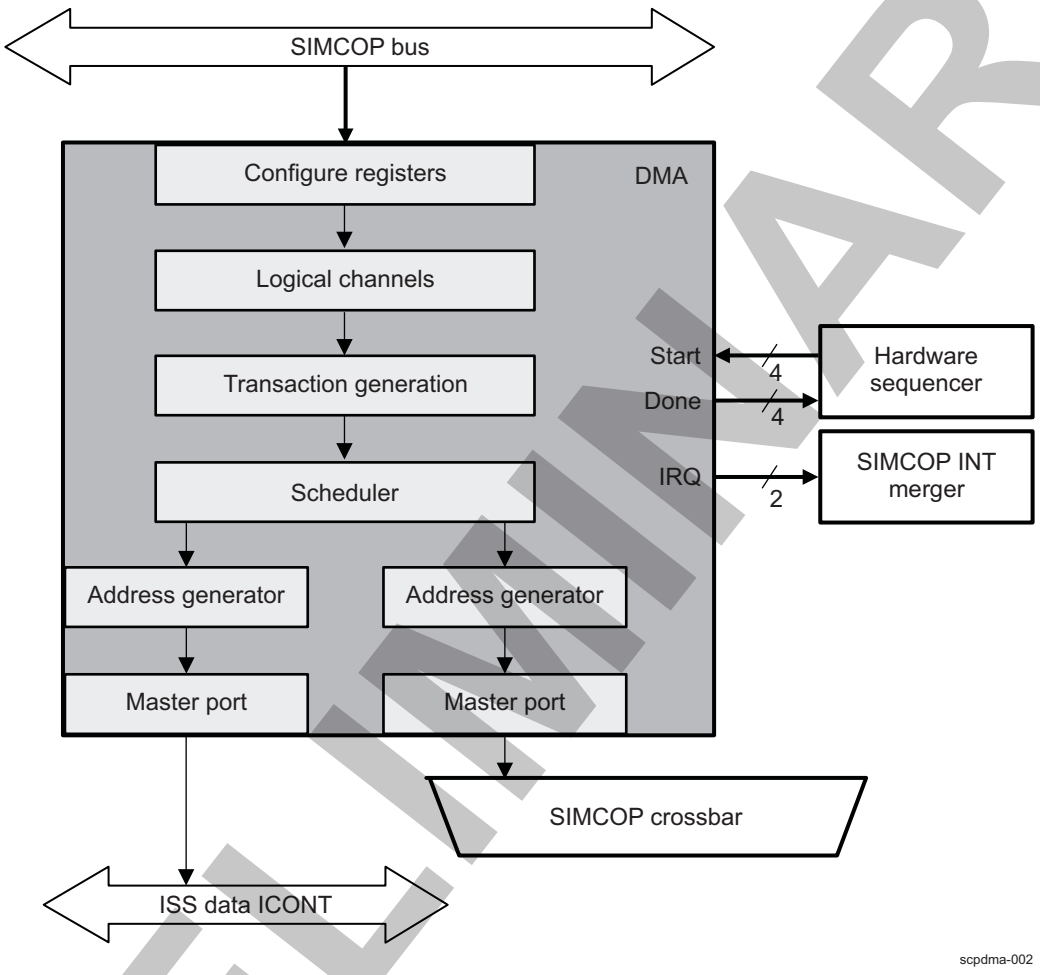
8.4.3.3 ISS SIMCOP DMA Functional Description

8.4.3.3.1 ISS SIMCOP DMA Block Diagram

Figure 8-273 is a block diagram of the SIMCOP DMA.

Figure 8-273. DMA Block Diagram



An external initiator sets up logical channels using the configuration interface.

When a logical channel becomes active, a transfer must be executed. A transfer corresponds to a 2D block of data copied from system memory to SIMCOP memory and vice versa.

A transfer is decomposed into one or multiple transactions by the transaction generation unit.

The scheduler issues transactions when tags are available. There can be one outstanding command per tag on the ISS data interconnect.

8.4.3.3.2 ISS SIMCOP DMA Power Management

Table 8-1414 lists the power-management features available in the DMA module.

Table 8-1414. Local Power-Management Features

Feature	Registers	Description
Master standby modes	SIMCOP_DMA_SYSCONFIG[5:4] STANDBYMODE	Force-standby, no-standby, and smart-standby modes are available.

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8.4.3.3.3 ISS SIMCOP DMA Interrupt Requests

The SIMCOP DMA module can generate two interrupts, SIMCOP_DMA_IRQ0 and SIMCOP_DMA_IRQ1. These two interrupts are controlled by four registers:

- SIMCOP_DMA_IRQSTATUS_RAW_j: The status of the interrupt before masking
- SIMCOP_DMA_IRQSTATUS_j: The status of the interrupt after masking
- SIMCOP_DMA_IRQENABLE_SET_j: Enable an interrupt to propagate to SIMCOP_DMA_IRQi signal (unmask)
- SIMCOP_DMA_IRQENABLE_CLR_j: Disable an interrupt to propagate to SIMCOP_DMA_IRQi signal (mask)

To clear an interrupt, software must write 1 in the corresponding bit of the SIMCOP_DMA_IRQSTATUS_j register even if the event is not enabled (SIMCOP_DMA_IRQSTATUS_RAW_j is also cleared).

Table 8-1415 list all the SIMCOP DMA events that can lead to an interrupt generation.

Table 8-1415. SIMCOP DMA Events List

Bit Name	Bit	Event
BUS_ERR	0	Error occurred on bus
CHAN0_BLOCK_DONE_IRQ	16	Channel 0 has completed transfer of one 2D block.
CHAN1_BLOCK_DONE_IRQ	17	Channel 1 has completed transfer of one 2D block.
CHAN2_BLOCK_DONE_IRQ	18	Channel 2 has completed transfer of one 2D block.
CHAN3_BLOCK_DONE_IRQ	19	Channel 3 has completed transfer of one 2D block.
CHAN4_BLOCK_DONE_IRQ	20	Channel 4 has completed transfer of one 2D block.
CHAN5_BLOCK_DONE_IRQ	21	Channel 5 has completed transfer of one 2D block.
CHAN6_BLOCK_DONE_IRQ	22	Channel 6 has completed transfer of one 2D block.
CHAN7_BLOCK_DONE_IRQ	23	Channel 7 has completed transfer of one 2D block.
CHAN0_FRAME_DONE_IRQ	24	Channel 0 has completed transfer of the full frame.
CHAN1_FRAME_DONE_IRQ	25	Channel 1 has completed transfer of the full frame.
CHAN2_FRAME_DONE_IRQ	26	Channel 2 has completed transfer of the full frame.
CHAN3_FRAME_DONE_IRQ	27	Channel 3 has completed transfer of the full frame.
CHAN4_FRAME_DONE_IRQ	28	Channel 4 has completed transfer of the full frame.
CHAN5_FRAME_DONE_IRQ	29	Channel 5 has completed transfer of the full frame.
CHAN6_FRAME_DONE_IRQ	30	Channel 6 has completed transfer of the full frame.
CHAN7_FRAME_DONE_IRQ	31	Channel 7 has completed transfer of the full frame.

8.4.3.3.4 ISS SIMCOP DMA Logical Channels

In the context of the SIMCOP, multiple logical channels are required to offload the external initiator. Typical uses of multiple contexts are:

- Run a read transfer followed by a write transfer. When this transfer is complete, new input data is fetched from system memory and stored in the image buffers.
- Read or write YUV4:2:0 data from system memory; YUV4:2:0 data is stored in two different system memory buffers.

8.4.3.3.4.1 Logical Channel States

The SIMCOP DMA supports up to eight ((SIMCOP_DMA_HWINFO[2] CHAN+1) × 4) logical channels. Each logical channel can be configured and triggered separately.

Idle logical channels must be configured and enabled (SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1) to be used.

Figure 8-274 shows the different states of a logical channel. Software can poll the current state from the SIMCOP_DMA_CHAN_CTRL_i[4:3] STATUS bit field.

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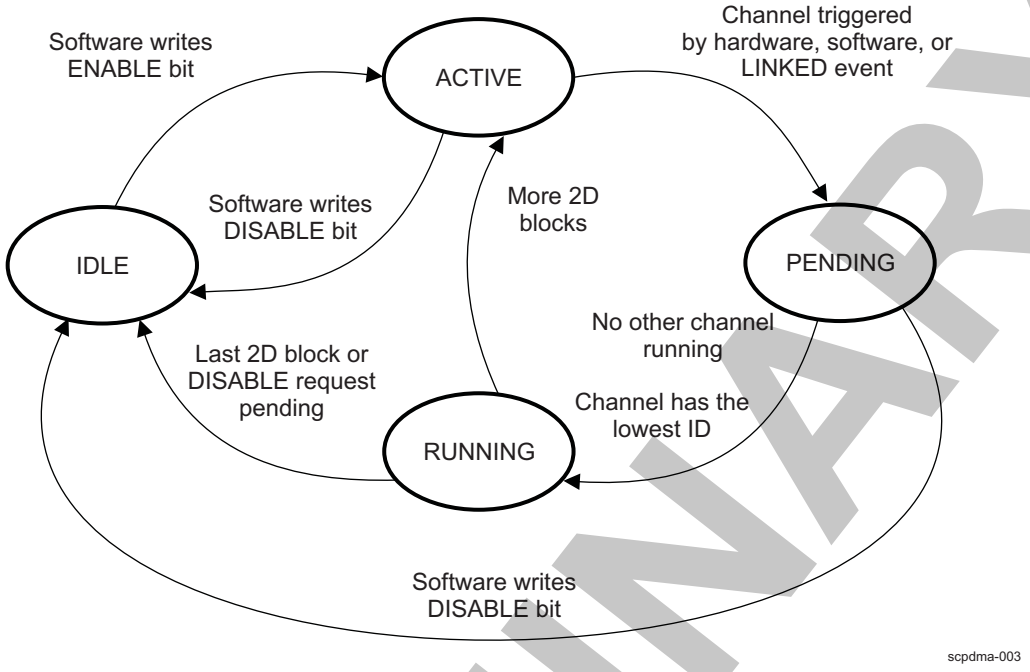
Figure 8-274. DMA Logical Channel States



When a trigger event is received by a channel in the ACTIVE state, it moves to the PENDING state. Trigger events received when the channel is in the IDLE, PENDING, or RUNNING state are discarded.

A logical channel is automatically disabled by hardware when a complete frame (all 2D blocks) is transferred. It can be disabled earlier by software by writing the SIMCOP_DMA_CHAN_CTRL_i[1] DISABLE bit. When a disable request occurs in the RUNNING state, it is memorized and executed when the channel leaves the RUNNING state. Pending disable requests have higher priority than channel trigger events.

When multiple logical channels are pending simultaneously, the following rules apply:

- An ongoing transfer of a 2D block is never stopped. It must complete before the next one starts.
- The logical channel with the lowest ID wins the arbitration (that is, CHAN0 has higher priority than CHAN1). Software can give higher priority to a channel by choosing a lower ID.

This situation can, for example, occur when software triggers a channel while a transfer is ongoing for another one. Two types of interrupts can be generated:

- CHANx_BLOCK_DONE_IRQ (where x = channel number): It is generated when the channel leaves the RUNNING state (RUNNING -> ACTIVE or RUNNING -> IDLE).
- CHANx_FRAME_DONE_IRQ (where x = channel number): It is generated when the channel enters the IDLE state.

8.4.3.3.4.2 Logical Channel Chaining, Trigger, and Hardware Synchronization

Active logical channels can be triggered:

- By software. Writes the SIMCOP_DMA_CHAN_CTRL_i[2] SWTRIGGER bit
- By a hardware DMA request. A channel can be made sensitive to a pulse on the START[y] input when SIMCOP_DMA_CHAN_CTRL_i[19:17] HWSTART = y has been configured by software.
- When the previous channel in the linked list finishes. This feature is enabled through the SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED bit field of the preceding channel in the chain.

When a channel completes, it can optionally send a pulse to the DONE[y] output. Software enables this feature by configuring SIMCOP_DMA_CHAN_CTRL_i[22:20] HWDONE = y.

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Typically, the START + DONE synchronization mechanism is used together with the SIMCOP hardware sequencer. The hardware sequencer sends a pulse to START[y] a data transfer and the SIMCOP DMA responds with a DONE[y] pulse when the transfer completes. A transfer can be composed of one or multiple logical channels. For example, a YUV4:2:0-NV12 block copy from system memory to SIMCOP local memories requires two chained logical channels.

CAUTION

Software must ensure that only one trigger event source is selected at a given time for a logical channel; otherwise, unpredictable behavior may occur.

Typically, the following combinations can be used:

- Single channel triggered by software: Hardware synchronization and linking are disabled. Software writes the SIMCOP_DMA_CHAN_CTRL_i[2] SWTRIGGER bit to start the transfer of one 2D block. Software must not trigger the channel again before the CHANx_BLOCK_DONE_IRQ (where x = channel number) event is generated by the DMA.
- Channels chain-triggered by software: Multiple channels are linked together using the SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED bit field. Software triggers the first one in the chain and monitors the CHANx_BLOCK_DONE_IRQ (where x = channel number) event to know when the chain can be triggered again.
- Single channel triggered by hardware synchronization: Sensitivity on START pulses is activated through the SIMCOP_DMA_CHAN_CTRL_i[19:17] HWSTART bit field. DONE pulse generation is activated using the SIMCOP_DMA_CHAN_CTRL_i[22:20] HWSTOP bit field.
- Channels chain-triggered by hardware: Multiple channels are linked together using the SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED bit field. Sensitivity on START pulses is activated for the first channel in the chain through the SIMCOP_DMA_CHAN_CTRL_i[19:17] HWSTART bit field. DONE pulse generation for the last channel in the chain is activated using the SIMCOP_DMA_CHAN_CTRL_i[22:20] HWDONE bit field.

8.4.3.3.4.3 Logical Channel Data Transfer

Each logical channel can handle 4D transfers from system memory to SIMCOP memory and vice versa.

A frame is composed of SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT * SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT 2D blocks of data. A single 2D block of data is transferred each time a logical channel is in the RUNNING state.

The size of a 2D block is SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM * SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM words of 128 bits. The SIMCOP DMA can transfer only full 128-bit words.

2D blocks may overlap in system memory. This feature is typically used for source data fetches from system memory to handle filter dependencies. If this feature is not used, software must set:

- SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP
- SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP

Figure 8-275 shows DMA addressing.

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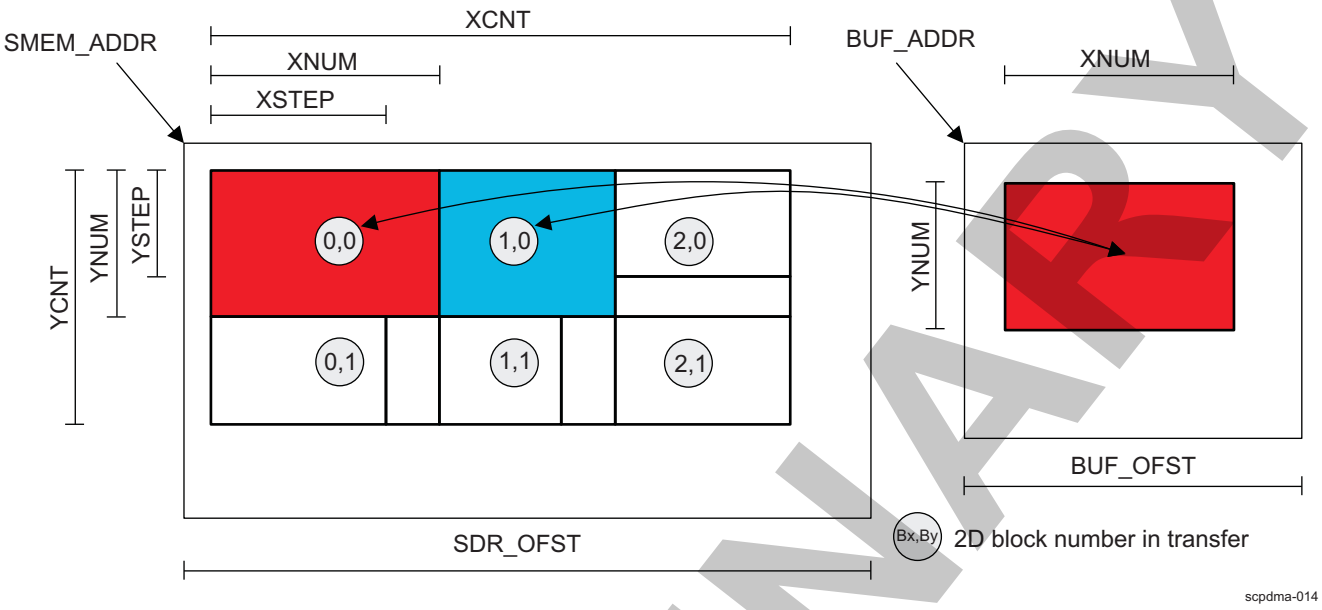
Figure 8-275. DMA Addressing



The base position of 2D blocks in system memory is automatically computed by the SIMCOP DMA. The base address is computed using the following formula:

SMEM_BASE = SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR +
Bx × SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP +
By × SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP ×
SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST

All 2D blocks of a logical channel have the same location in SIMCOP local memories:

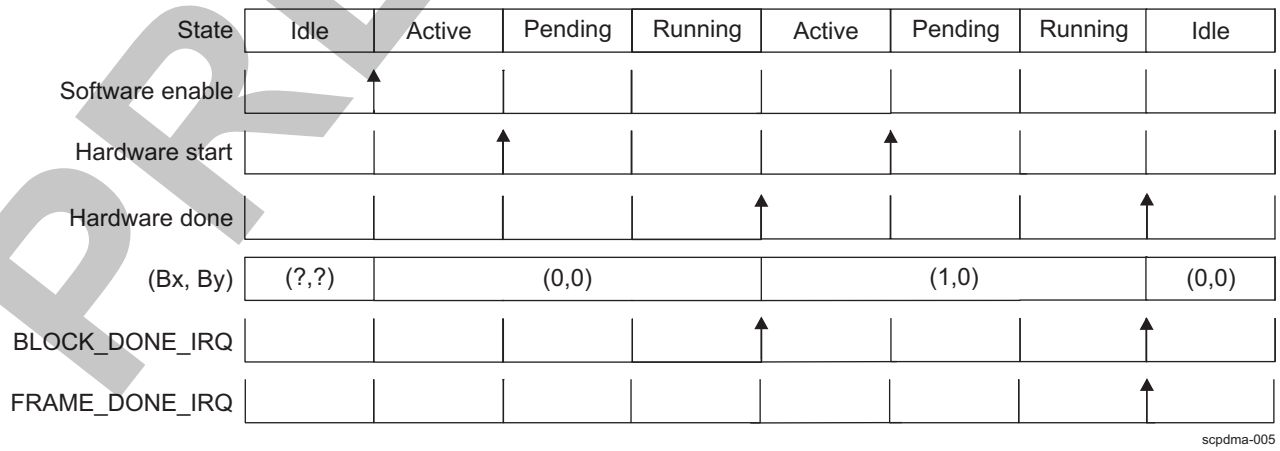
BUF_BASE = SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR

The same functionality can also be used to read or write sparse data from SDRAM. Typically, that is useful to split processing between two SIMCOP accelerators .

Software can poll the status of a channel using the SIMCOP_DMA_CHAN_CURRENT_BLOCK_i register. It holds the Bx, By values of the last-transferred 2D block. The Bx, By values are reset when a channel is enabled (set the SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE bit) and they are updated when a channel enters the RUNNING state.

Figure 8-276 shows an example of a 2-block large transfer.

Figure 8-276. 2-Block Large Transfer Example



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8.4.3.3.5 Transaction Generation

Each transfer is decomposed into one or multiple transactions by the DMA engine. The firmware can define:

- Burst generation for regular or tiled accesses (SIMCOP_DMA_CHAN_CTRL_i[6] TILERMODE). Additional parameters must be defined for tiled accesses. See Section 8.4.3.3.5.2, *Block Bursts for Tiled Transfers*.
- The maximum burst size (SIMCOP_DMA_CTRL[1:0] MAX_BURST_SIZE). It must be aligned with the interconnect configuration.
- Use of posted or nonposted writes (SIMCOP_DMA_CTRL[3] POSTED_WRITES). It must be aligned with the interconnect configuration. Mainly, in a multichannel system memory, system bursts must be issued nonposted.

8.4.3.3.5.1 Incrementing Bursts for Regular Transfers

Lines of 2D blocks are processed sequentially. The following transaction process is used for a given line:

1. Perform a single nonaligned burst from the start address to the next SIMCOP_DMA_CTRL[1:0] MAX_BURST_SIZE boundary (or less if the transfer is smaller).
2. Perform "n" aligned bursts (n can be 0).
3. Perform a single nonaligned burst up to the end address (if needed).

A transaction is aligned when the start address modulo burst length is 0.

8.4.3.3.5.2 Block Bursts for Tiled Transfers

The line stride is configured using the SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST bit field. The full register content is used for internal address computation. The SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST bit field must be a multiple of the SIMCOP_DMA_CTRL[1:0] MAX_BURST_SIZE bit field.

The SIMCOP DMA has the following alignment constraints:

- SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR is 128 bit-aligned.
- SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM is 128 bit-aligned.

Only the values in Table 8-1416 are allowed for the SIMCOP_DMA_CTRL[1:0] MAX_BURST_SIZE bit field. Other values lead to undefined behavior.

Table 8-1416. Allowed Max Burst Size

Minimum Burst Height	MAX_BURST_SIZE
2	2, 4, or 8 x 128 bits
4	4 or 8 x 128 bits

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8.4.3.4 ISS SIMCOP DMA Basic Programming Model

8.4.3.4.1 Initialization of Surrounding Modules

To initialize the DMA, the surrounding modules must be initialized. Table 8-1417 lists these modules.

Table 8-1417. Initialization of Surrounding Modules

Module	Minimum Required Setting	Optional Settings
CLKC	Enable SIMCOP clock	
Buffers	Configure DMA access to image buffer	
SIMCOP CTRL		Configure SIMCOP CTRL to handle DMA interrupts

8.4.3.4.2 ISS SIMCOP DMA Channel Configuration and Hardware Synchronization

Software must fully configure a DMA channel before enabling it. It then configures channel linking and the used synchronization method.

The following example shows four logical channels chained with hardware synchronization used to copy YUV4:2:0-NV12 data from SIMCOP local memories to system memory, and then to copy YUV4:2:0-NV12 data from system memory to SIMCOP local memories.

YUV4:2:0-NV12 data is stored in two separate buffers in SDRAM. Therefore, two channels are used for the SIMCOP -> system copy, and two channels are used for the system -> SIMCOP copy.

In this example, the intent is to transfer a 2 x 2 array of 64 x 32 pixel blocks. It is assumed that input data is stored contiguously in system memory and that the output buffer size in system memory is 256 x 32 pixels. In SIMCOP local memories, data is contiguously stored starting at address 0

The following configuration is used:

- Channel i = 0, input Y buffer:
  - SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR = Start address of Y input buffer
  - SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST = 16 (= 256 bytes)
  - SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR = 0
  - SIMCOP_DMA_CHAN_BUF_OFST_i[23:4] OFST = 8 (= 128 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = 32
  - SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT = 2
  - SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT = 2
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP = 32
- Channel i = 1, input UV buffer:
  - SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR = Start address of UV input buffer
  - SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST = 16 (= 256 bytes)
  - SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR = 128 (2 KiB)
  - SIMCOP_DMA_CHAN_BUF_OFST_i[23:4] OFST = 8 (= 128 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = 16
  - SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT = 2
  - SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT = 2
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP = 16
- Channel i = 2, output Y buffer:

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  - SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR = Start address of Y output buffer
  - SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST = 16 (= 256 bytes)
  - SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR = 0
  - SIMCOP_DMA_CHAN_BUF_OFST_i[23:4] OFST = 8 (= 128 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = 32
  - SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT = 2
  - SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT = 2
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP = 32
- Channel i = 3, output UV buffer
  - SIMCOP_DMA_CHAN_SMEM_ADDR_i[31:4] ADDR = Start address of UV output buffer
  - SIMCOP_DMA_CHAN_SMEM_OFST_i[19:4] OFST = 16 (= 256 bytes)
  - SIMCOP_DMA_CHAN_BUF_ADDR_i[23:4] ADDR = 128 (= 2 KiB)
  - SIMCOP_DMA_CHAN_BUF_OFST_i[23:4] OFST = 8 (= 128 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[13:4] XNUM = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_SIZE_i[28:16] YNUM = 16
  - SIMCOP_DMA_CHAN_FRAME_i[9:0] XCNT = 2
  - SIMCOP_DMA_CHAN_FRAME_i[25:16] YCNT = 2
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[14:4] XSTEP = 4 (= 64 bytes)
  - SIMCOP_DMA_CHAN_BLOCK_STEP_i[29:16] YSTEP = 16

Figure 8-277 shows the channel linking chain used. All four channels are executed sequentially. Doing so prevents access collision in SIMCOP local memories or system memories. Channel 0 is started by a START[0] pulse from SIMCOP. When Channel 3 completes the last transfer, a pulse to DONE[0] is sent back to SIMCOP.

Figure 8-278 shows the temporal channel sequence.

Figure 8-277. YUV4:2:0-NV12 Read/Write Chain

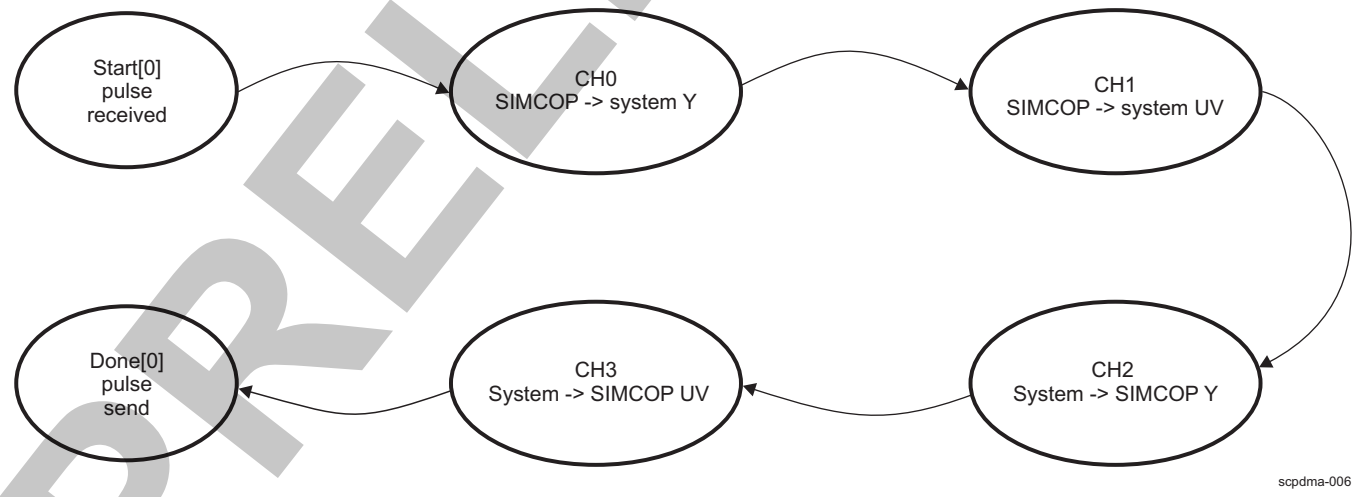

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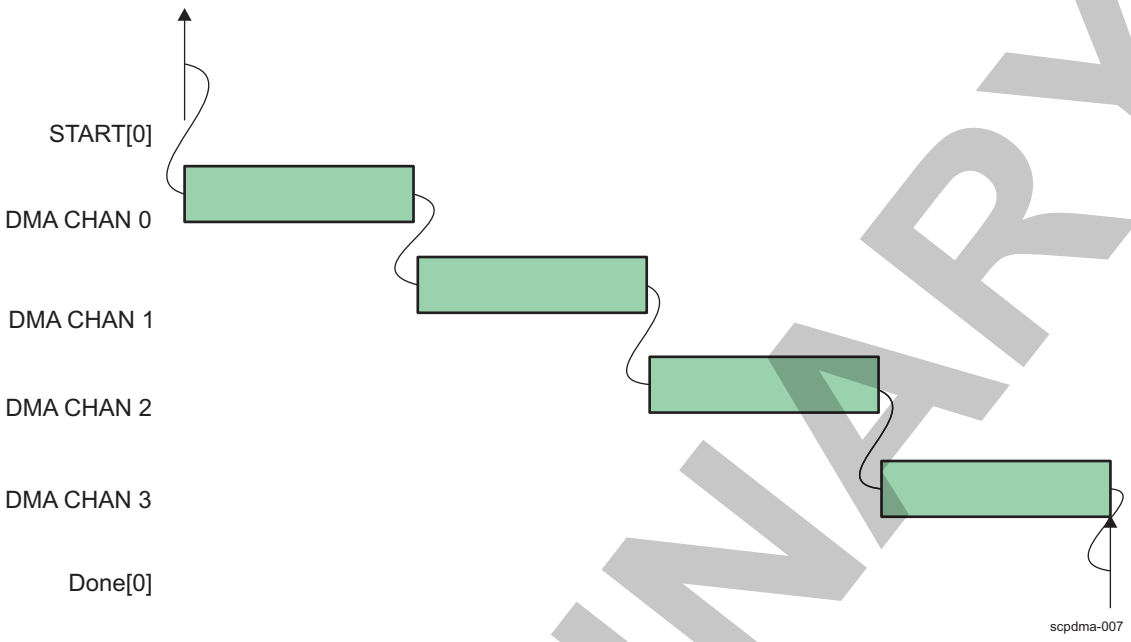
Figure 8-278. Temporal Channel Sequence



The following configuration is used for each channel:

- Channel i = 0, input Y buffer, first in sequence:
  - SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED = 0x11 (= CHAN 1)
  - SIMCOP_DMA_CHAN_CTRL_i[19:17] HWSTART = 0x4 (= CHAN 0)
  - SIMCOP_DMA_CHAN_CTRL_i[5] DIR = 1 (= SIMCOP buffers -> system memory)
  - SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1
- Channel i = 1, input UV buffer, second in sequence:
  - SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED = 0x12 (= CHAN 2)
  - SIMCOP_DMA_CHAN_CTRL_i[5] DIR = 1 (= SIMCOP buffers -> system memory)
  - SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1
- Channel i = 2, output Y buffer, third in sequence:
  - SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED = 0x13 (= CHAN 3)
  - SIMCOP_DMA_CHAN_CTRL_i[5] DIR = 0 (= system memory -> SIMCOP buffers)
  - SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1
- Channel i = 3, output UV buffer, last in sequence:
  - SIMCOP_DMA_CHAN_CTRL_i[16:12] LINKED = CHAN 1
  - SIMCOP_DMA_CHAN_CTRL_i[22:20] HWSTOP = 0x4 (= CHAN 0)
  - SIMCOP_DMA_CHAN_CTRL_i[5] DIR = 0 (= system memory -> SIMCOP buffers)
  - SIMCOP_DMA_CHAN_CTRL_i[0] ENABLE = 1

Software can read the status of a logical channel at any time. However, logical channel configuration registers can be changed only when the channel is in the IDLE state.

Software can disable a logical channel by writing the SIMCOP_DMA_CHAN_CTRL_i[1] DISABLE bit. A channel is effectively disabled when SIMCOP_DMA_CHAN_CTRL_i[4:3] STATUS = IDLE. In case of linked channels, software must disable all channels in the chain and wait until all of them are back in the IDLE state before channels can be reprogrammed.

8.4.3.4.3 Software Synchronization

Software performs the following sequence:

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1. Configures the channel
2. Enables the channel
3. Triggers the channel by writing the SIMCOP_DMA_CHAN_CTRL_i[2] SWTRIGGER bit
4. Waits for BLOCK_DONE_IRQ

Step 2 and Step 4 are repeated until all 2D blocks have been transferred.

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8.4.3.5 ISS SIMCOP DMA Register Manual

8.4.3.5.1 ISS SIMCOP DMA Instance Summary

Table 8-1418 summarizes the DMA instance.

Table 8-1418. DMA Instance Summary

Module Name	L3_MAIN Base Address	IPU Base Address	Size
DMA	0x00 5202 0200	0x5506 0200	512 Bytes

8.4.3.5.2 ISS SIMCOP DMA Registers

8.4.3.5.2.1 ISS SIMCOP DMA Register Summary

Table 8-1419 summarizes the SIMCOP_DMA register mapping.

Table 8-1419. DMA Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address	IPU Physical Address
SIMCOP_DMA_REVISION	R	32	0x0000 0000	0x00 5202 0200	0x5506 0200
SIMCOP_DMA_HWINFO	R	32	0x0000 0004	0x00 5202 0204	0x5506 0204
SIMCOP_DMA_SYSCONFIG	RW	32	0x0000 0010	0x00 5202 0210	0x5506 0210
RESERVED	-	-	0x0000 0018	0x00 5202 0218	0x5506 0218
SIMCOP_DMA_CTRL	RW	32	0x0000 001C	0x00 5202 021C	0x5506 0218
SIMCOP_DMA_IRQSTATUS_RAW_j [1]	RW	32	0x0000 0020 + (0x10 * j)	0x00 5202 0220 + (0x10 * j)	0x5506 0220 + (0x10 * j)
SIMCOP_DMA_IRQSTATUS_j [1]	RW	32	0x0000 0024 + (0x10 * j)	0x00 5202 0224 + (0x10 * j)	0x5506 0224 + (0x10 * j)
SIMCOP_DMA_IRQENABLE_SET_j [1]	RW	32	0x0000 0028 + (0x10 * j)	0x00 5202 0228 + (0x10 * j)	0x5506 0228 + (0x10 * j)
SIMCOP_DMA_IRQENABLE_CLR_j [1]	RW	32	0x0000 002C + (0x10 * j)	0x00 5202 022C + (0x10 * j)	0x5506 022C + (0x10 * j)
SIMCOP_DMA_CHAN_CTRL_i [2]	RW	32	0x0000 0080 + (0x30 * i)	0x00 5202 0280 + (0x30 * i)	0x5506 0280 + (0x30 * i)
SIMCOP_DMA_CHAN_SMEM_ADDR_i [2]	RW	32	0x0000 0084 + (0x30 * i)	0x00 5202 0284 + (0x30 * i)	0x5506 0284 + (0x30 * i)
SIMCOP_DMA_CHAN_SMEM_OFST_i [2]	RW	32	0x0000 0088 + (0x30 * i)	0x00 5202 0288 + (0x30 * i)	0x5506 0288 + (0x30 * i)
SIMCOP_DMA_CHAN_BUF_OFST_i [2]	RW	32	0x0000 008C + (0x30 * i)	0x00 5202 028C + (0x30 * i)	0x5506 028C + (0x30 * i)
SIMCOP_DMA_CHAN_BUF_ADDR_i [2]	RW	32	0x0000 0090 + (0x30 * i)	0x00 5202 0290 + (0x30 * i)	0x5506 0290 + (0x30 * i)
SIMCOP_DMA_CHAN_BLOCK_SIZE_i [2]	RW	32	0x0000 0094 + (0x30 * i)	0x00 5202 0294 + (0x30 * i)	0x5506 0294 + (0x30 * i)
SIMCOP_DMA_CHAN_FRAME_i [2]	RW	32	0x0000 0098 + (0x30 * i)	0x00 5202 0298 + (0x30 * i)	0x5506 0298 + (0x30 * i)
SIMCOP_DMA_CHAN_CURRENT_BLOCK_i [2]	R	32	0x0000 00A0 + (0x30 * i)	0x00 5202 02A0 + (0x30 * i)	0x5506 02A0 + (0x30 * i)
SIMCOP_DMA_CHAN_BLOCK_STEP_i [2]	RW	32	0x0000 00A4 + (0x30 * i)	0x00 5202 02A4 + (0x30 * i)	0x5506 02A4 + (0x30 * i)

(1) i = 0 to 7
(2) j = 0 to 1

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8.4.3.5.2.2 ISS SIMCOP DMA Register Description

through describe the registers in details.

Table 8-1420. SIMCOP_DMA_REVISION

Address Offset	0x0000 0000		
Physical Address	0x00 5202 0200 0x5506 0200	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	Revision ID	R	-(1)

(1) TI internal data

Table 8-1421. Register Call Summary for Register SIMCOP_DMA_REVISION

ISS SIMCOP DMA Module

- ISS SIMCOP DMA Register Summary: [0]

Table 8-1422. SIMCOP_DMA_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x00 5202 0204 0x5506 0204	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	Information about the IP module's hardware configuration, i.e. typically the module's HDL generics.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													CHAN	CONTEXT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	CHAN	Logical channels Read 0x0: 4 Read 0x1: 8	R	1
1:0	CONTEXT	Maximum outstanding OCP transactions Read 0x0: 4 Read 0x1: 8 Read 0x2: 16	R	0x2

Table 8-1423. Register Call Summary for Register SIMCOP_DMA_HWINFO

ISS SIMCOP DMA Module

- Logical Channel States: [0]
- ISS SIMCOP DMA Register Summary: [1]

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Table 8-1424. SIMCOP_DMA_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x00 5202 0210 0x5506 0210	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		RESERVED			

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x2: Smart standby mode. 0x3: Smart standby mode.	RW	0x2
3:0	RESERVED		R	0x0

Table 8-1425. Register Call Summary for Register SIMCOP_DMA_SYSCONFIG

ISS SIMCOP DMA Module

- ISS SIMCOP DMA Power Management: [0]
- ISS SIMCOP DMA Register Summary: [1]

Table 8-1426. SIMCOP_DMA_CTRL

Address Offset	0x0000 001C		
Physical Address	0x00 5202 021C 0x5506 0218	**Instance**	DMA_MAIN_L3 DMA_IPU
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BW_LIMITER																RESERVED								TAG_CNT				POSTED_WRITES	RESERVED	MAX_BURST_SIZE	

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Bits	Field Name	Description	Type	Reset
31:16	BW_LIMITER	SIMCOP DMA guarantees that there are at least BW_LIMITER functional clock cycles between two OCP requests. No IDLE cycles are inserted during an OCP transaction. This parameter could be used to reduce traffic generated by the SIMCOP DMA for non timing critical applications. Doing so leaves more BW for other system initiators. Default value corresponds to maximum performance.	RW	0x0000
15:8	RESERVED		R	0x00
7:4	TAG_CNT	Limits the outstanding transactions count. Only tags 0 - TAG_CNT will be used by SIMCOP DMA The maximum allowed value is $2^{(SIMCOCP\_DMA\_GNC.CONTEXT+2)-1}$	RW	0x3
3	POSTED_WRITES	Select write type. Setting depend on the used interconnect 0x0: Only non posted writes are generated 0x1: Only posted writes are generated	RW	0
2	RESERVED		R	0
1:0	MAX_BURST_SIZE	Defines the maximum burst length for INCR bursts. In case of 2D bursts, length x height is less or equal to this value. 0x0: Single requests only 0x1: less or equal to 2 0x2: less or equal to 4 0x3: less or equal to 8	RW	0x0

Table 8-1427. Register Call Summary for Register SIMCOP_DMA_CTRL

ISS SIMCOP DMA Module

- Transaction Generation: [0] [1]
- Incrementing Bursts for Regular Transfers: [2]
- Block Bursts for Tiled Transfers: [3] [5]
- ISS SIMCOP DMA Register Summary: [6]

Table 8-1428. SIMCOP_DMA_IRQSTATUS_RAW_j

Address Offset	0x0000 0020 + (0x10 * j)		
Physical Address	0x00 5202 0220 + (0x10 * j) 0x5506 0220 + (0x10 * j)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	Per-event raw interrupt status vector Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAN7_FRAME_DONE_IRQ	CHAN6_FRAME_DONE_IRQ	CHAN5_FRAME_DONE_IRQ	CHAN4_FRAME_DONE_IRQ	CHAN3_FRAME_DONE_IRQ	CHAN2_FRAME_DONE_IRQ	CHAN1_FRAME_DONE_IRQ	CHAN0_FRAME_DONE_IRQ	CHAN7_BLOCK_DONE_IRQ	CHAN6_BLOCK_DONE_IRQ	CHAN5_BLOCK_DONE_IRQ	CHAN4_BLOCK_DONE_IRQ	CHAN3_BLOCK_DONE_IRQ	CHAN2_BLOCK_DONE_IRQ	CHAN1_BLOCK_DONE_IRQ	CHAN0_BLOCK_DONE_IRQ	RESERVED															OCP_ERR

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Bits	Field Name	Description	Type	Reset
31	CHAN7_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
30	CHAN6_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
29	CHAN5_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
28	CHAN4_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
27	CHAN3_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
26	CHAN2_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
25	CHAN1_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
24	CHAN0_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
23	CHAN7_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
22	CHAN6_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
21	CHAN5_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
20	CHAN4_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
19	CHAN3_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
18	CHAN2_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
17	CHAN1_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
16	CHAN0_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW	0
15:1	RESERVED		R	0x0000
0	OCP_ERR	OCP error Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

Table 8-1429. Register Call Summary for Register SIMCOP_DMA_IRQSTATUS_RAW_j

ISS SIMCOP DMA Module

- ISS SIMCOP DMA Interrupt Requests: [0] [1]
- ISS SIMCOP DMA Register Summary: [2]

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Table 8-1430. SIMCOP_DMA_IRQSTATUS_j

Address Offset	0x0000 0024 + (0x10 * j)		
Physical Address	0x00 5202 0224 + (0x10 * j) 0x5506 0224 + (0x10 * j)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	Per-event "enabled" interrupt status vector Enabled status isn't set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAN7_FRAME_DONE_IRQ	CHAN6_FRAME_DONE_IRQ	CHAN5_FRAME_DONE_IRQ	CHAN4_FRAME_DONE_IRQ	CHAN3_FRAME_DONE_IRQ	CHAN2_FRAME_DONE_IRQ	CHAN1_FRAME_DONE_IRQ	CHAN0_FRAME_DONE_IRQ	CHAN7_BLOCK_DONE_IRQ	CHAN6_BLOCK_DONE_IRQ	CHAN5_BLOCK_DONE_IRQ	CHAN4_BLOCK_DONE_IRQ	CHAN3_BLOCK_DONE_IRQ	CHAN2_BLOCK_DONE_IRQ	CHAN1_BLOCK_DONE_IRQ	CHAN0_BLOCK_DONE_IRQ	RESERVED															BUS_ERR

Bits	Field Name	Description	Type	Reset
31	CHAN7_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
30	CHAN6_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
29	CHAN5_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
28	CHAN4_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
27	CHAN3_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
26	CHAN2_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
25	CHAN1_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
24	CHAN0_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
23	CHAN7_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
22	CHAN6_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
21	CHAN5_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
20	CHAN4_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
19	CHAN3_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
18	CHAN2_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
17	CHAN1_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
16	CHAN0_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
15:1	RESERVED		R	0x0000
0	BUS_ERR	BUS error Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

Table 8-1431. Register Call Summary for Register SIMCOP_DMA_IRQSTATUS_j

ISS SIMCOP DMA Module

- ISS SIMCOP DMA Interrupt Requests: [0] [1]
- ISS SIMCOP DMA Register Summary: [2]

Table 8-1432. SIMCOP_DMA_IRQENABLE_SET_j

Address Offset	0x0000 0028 + (0x10 * j)		
Physical Address	0x00 5202 0228 + (0x10 * j) 0x5506 0228 + (0x10 * j)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	Per-event interrupt enable bit vector Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAN7_FRAME_DONE_IRQ	CHAN6_FRAME_DONE_IRQ	CHAN5_FRAME_DONE_IRQ	CHAN4_FRAME_DONE_IRQ	CHAN3_FRAME_DONE_IRQ	CHAN2_FRAME_DONE_IRQ	CHAN1_FRAME_DONE_IRQ	CHAN0_FRAME_DONE_IRQ	CHAN7_BLOCK_DONE_IRQ	CHAN6_BLOCK_DONE_IRQ	CHAN5_BLOCK_DONE_IRQ	CHAN4_BLOCK_DONE_IRQ	CHAN3_BLOCK_DONE_IRQ	CHAN2_BLOCK_DONE_IRQ	CHAN1_BLOCK_DONE_IRQ	CHAN0_BLOCK_DONE_IRQ	RESERVED															OCP_ERR

Bits	Field Name	Description	Type	Reset
31	CHAN7_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
30	CHAN6_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
29	CHAN5_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
28	CHAN4_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
27	CHAN3_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
26	CHAN2_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
25	CHAN1_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
24	CHAN0_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
23	CHAN7_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
22	CHAN6_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
21	CHAN5_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
20	CHAN4_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
19	CHAN3_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
18	CHAN2_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
17	CHAN1_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
16	CHAN0_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
15:1	RESERVED		R	0x0000
0	OCP_ERR	OCP error Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

Table 8-1433. Register Call Summary for Register SIMCOP_DMA_IRQENABLE_SET_j

ISS SIMCOP DMA Module

- ISS SIMCOP DMA Interrupt Requests: [0]
- ISS SIMCOP DMA Register Summary: [1]

Table 8-1434. SIMCOP_DMA_IRQENABLE_CLR_j

Address Offset	0x0000 002C + (0x10 * j)		
Physical Address	0x00 5202 022C + (0x10 * j) 0x5506 022C + (0x10 * j)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	Per-event interrupt enable bit vector Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAN7_FRAME_DONE_IRQ	CHAN6_FRAME_DONE_IRQ	CHAN5_FRAME_DONE_IRQ	CHAN4_FRAME_DONE_IRQ	CHAN3_FRAME_DONE_IRQ	CHAN2_FRAME_DONE_IRQ	CHAN1_FRAME_DONE_IRQ	CHAN0_FRAME_DONE_IRQ	CHAN7_BLOCK_DONE_IRQ	CHAN6_BLOCK_DONE_IRQ	CHAN5_BLOCK_DONE_IRQ	CHAN4_BLOCK_DONE_IRQ	CHAN3_BLOCK_DONE_IRQ	CHAN2_BLOCK_DONE_IRQ	CHAN1_BLOCK_DONE_IRQ	CHAN0_BLOCK_DONE_IRQ	RESERVED														OCP_ERR	

Bits	Field Name	Description	Type	Reset
31	CHAN7_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
30	CHAN6_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
29	CHAN5_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
28	CHAN4_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
27	CHAN3_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
26	CHAN2_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
25	CHAN1_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
24	CHAN0_FRAME_DONE_IRQ	Channel has completed transfer of the full frame Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
23	CHAN7_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
22	CHAN6_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
21	CHAN5_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
20	CHAN4_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
19	CHAN3_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
18	CHAN2_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
17	CHAN1_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
16	CHAN0_BLOCK_DONE_IRQ	Channel has completed transfer of one 2D block Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
15:1	RESERVED		R	0x0000

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Bits	Field Name	Description	Type	Reset
0	OCP_ERR	OCP error Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

Table 8-1435. Register Call Summary for Register SIMCOP_DMA_IRQENABLE_CLR_j

ISS SIMCOP DMA Module

- ISS SIMCOP DMA Interrupt Requests: [0]
- ISS SIMCOP DMA Register Summary: [1]

Table 8-1436. SIMCOP_DMA_CHAN_CTRL_i

Address Offset	0x0000 0080 + (0x30 * i)		
Physical Address	0x00 5202 0280 + (0x30 * i) 0x5506 0280 + (0x30 * i)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	Logical channel control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HWSTOP				HWSTART				LINKED				RESERVED				TILERMODE	DIR	STATUS			SWTRIGGER	DISABLE	ENABLE

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x000
22:20	HWSTOP	DMA logical channel HW synchronization. Controls generation of the DONE pulse for the logical channel Only the values listed below are allowed. Other values lead to undefined behavior. 0x0: Disabled. 0x4: Use HW synchronization channel 0. 0x5: Use HW synchronization channel 1 0x6: Use HW synchronization channel 2 0x7: Use HW synchronization channel 3	RW	0x0
19:17	HWSTART	DMA logical channel HW synchronization. Controls sensitivity of the logical channel on a START pulse Only the values listed below are allowed. Other values lead to undefined behavior. 0x0: Disabled. 0x4: Use HW synchronization channel 0. 0x5: Use HW synchronization channel 1 0x6: Use HW synchronization channel 2 0x7: Use HW synchronization channel 3	RW	0x0

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Bits	Field Name	Description	Type	Reset
16:12	LINKED	DMA logical channel linking. Only the values listed below are allowed. Other values lead to undefined behavior. 0x0: Disabled. 0x10: Start channel 0 when this channel has completed transfer of one 2D block 0x11: Start channel 1 when this channel has completed transfer of one 2D block 0x12: Start channel 2 when this channel has completed transfer of one 2D block 0x13: Start channel 3 when this channel has completed transfer of one 2D block 0x14: Start channel 4 when this channel has completed transfer of one 2D block 0x15: Start channel 5 when this channel has completed transfer of one 2D block 0x16: Start channel 6 when this channel has completed transfer of one 2D block 0x17: Start channel 7 when this channel has completed transfer of one 2D block	RW	0x00
11:7	RESERVED		R	0x0
6	TILERMODE	Selects OCP transaction breakdown algorithm 0x0: Regular mode. INCR burst are used. ADDR[32]=0 for OCP transactions 0x1: Tiler mode. BLCK burst are used. ADDR[32]=1 for OCP transactions	RW	-
5	DIR	Transfer direction 0x0: System memory - SIMCOP buffers 0x1: SIMCOP buffers - system memory	RW	0
4:3	STATUS	SW could poll this bit to know the state of the channel Read 0x0: Idle Read 0x1: Active Read 0x2: Pending Read 0x3: Running	R	0x0
2	SWTRIGGER	Software trigger of the DMA channel. Read of this register always returns 0. Write 0x0: No effect Write 0x1: Change the logical channel state to PENDING if it is in ACTIVE state. No effect if the channel is in RUNNING, PENDING or IDLE state	W	0
1	DISABLE	Disable control of the logical channel. Read of this register always returns 0. Write 0x0: No effect. Write 0x1: Disable the channel. Changes the logical channel state to IDLE when it is in ACTIVE state. Memorize a disable request when the channel is in RUNNING or PENDING state.	W	0
0	ENABLE	Enable control of the logical channel. Read of this register always returns 0. Write 0x0: No effect Write 0x1: Enable the channel. Changes the state of the logical channel from IDLE to ACTIVE.	W	0

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Table 8-1437. Register Call Summary for Register SIMCOP_DMA_CHAN_CTRL_i

ISS SIMCOP DMA Module

- Logical Channel States: [0] [1] [2]
- Logical Channel Chaining, Trigger, and Hardware Synchronization: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- Logical Channel Data Transfer: [14]
- Transaction Generation: [15]
- Block Bursts for Tiled Transfers:
- ISS SIMCOP DMA Channel Configuration and Hardware Synchronization: [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33]
- Software Synchronization: [34]
- ISS SIMCOP DMA Register Summary: [35]

Table 8-1438. SIMCOP_DMA_CHAN_SMEM_ADDR_i

Address Offset	0x0000 0084 + (0x30 * i)		
Physical Address	0x00 5202 0284 + (0x30 * i) 0x5506 0284 + (0x30 * i)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	System memory address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Address in 128-bit words	RW	0x-------
3:0	RESERVED		R	0x0

Table 8-1439. Register Call Summary for Register SIMCOP_DMA_CHAN_SMEM_ADDR_i

ISS SIMCOP DMA Module

- Logical Channel Data Transfer: [0]
- Block Bursts for Tiled Transfers: [1]
- ISS SIMCOP DMA Channel Configuration and Hardware Synchronization: [2] [3] [4] [5]
- ISS SIMCOP DMA Register Summary: [6]

Table 8-1440. SIMCOP_DMA_CHAN_SMEM_OFST_i

Address Offset	0x0000 0088 + (0x30 * i)		
Physical Address	0x00 5202 0288 + (0x30 * i) 0x5506 0288 + (0x30 * i)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	System memory line offset in 128-bit words. Maximum stride = 1Mbyte		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												OFST																RESERVED			

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:4	OFST	Line offset. In 128-bit words.	RW	0x----
3:0	RESERVED		R	0x0

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Table 8-1441. Register Call Summary for Register SIMCOP_DMA_CHAN_SMEM_OFST_i

ISS SIMCOP DMA Module

- Logical Channel Data Transfer: [0]
- Block Bursts for Tiled Transfers: [1] [2]
- ISS SIMCOP DMA Channel Configuration and Hardware Synchronization: [3] [4] [5] [6]
- ISS SIMCOP DMA Register Summary: [7]

Table 8-1442. SIMCOP_DMA_CHAN_BUF_OFST_i

Address Offset	0x0000 008C + (0x30 * i)		
Physical Address	0x00 5202 028C + (0x30 * i) 0x5506 028C + (0x30 * i)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	SIMCOP memory line offset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OFST																				RESERVED			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:4	OFST	Line offset. In 128-bit words.	RW	0x-----
3:0	RESERVED		R	0x0

Table 8-1443. Register Call Summary for Register SIMCOP_DMA_CHAN_BUF_OFST_i

ISS SIMCOP DMA Module

- ISS SIMCOP DMA Channel Configuration and Hardware Synchronization: [0] [1] [2] [3]
- ISS SIMCOP DMA Register Summary: [4]

Table 8-1444. SIMCOP_DMA_CHAN_BUF_ADDR_i

Address Offset	0x0000 0090 + (0x30 * i)		
Physical Address	0x00 5202 0290 + (0x30 * i) 0x5506 0290 + (0x30 * i)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	SIMCOP memory address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ADDR																				RESERVED			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:4	ADDR	Address in 128-bit words.	RW	0x-----
3:0	RESERVED		R	0x0

Table 8-1445. Register Call Summary for Register SIMCOP_DMA_CHAN_BUF_ADDR_i

ISS SIMCOP DMA Module

- Logical Channel Data Transfer: [0]
- ISS SIMCOP DMA Channel Configuration and Hardware Synchronization: [1] [2] [3] [4]
- ISS SIMCOP DMA Register Summary: [5]

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Table 8-1446. SIMCOP_DMA_CHAN_BLOCK_SIZE_i

Address Offset	0x0000 0094 + (0x30 * i)		
Physical Address	0x00 5202 0294 + (0x30 * i) 0x5506 0294 + (0x30 * i)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	2D block size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								YNUM								RESERVED								XNUM							RESERVED

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:16	YNUM	Height, in lines, per 2D block Valid values are 1- 8191.	RW	0bxxxxxxxxxxxxx
15:14	RESERVED		R	0x0
13:4	XNUM	Width, in 128-bit words, per 2D block. Valid values are 1-1023, that corresponds to 16 bytes to 16kBytes.	RW	0bxxxxxxxxxx
3:0	RESERVED		R	0x0

Table 8-1447. Register Call Summary for Register SIMCOP_DMA_CHAN_BLOCK_SIZE_i

ISS SIMCOP DMA Module

- Logical Channel Data Transfer: [0] [1] [2] [3]
- Block Bursts for Tiled Transfers: [4]
- ISS SIMCOP DMA Channel Configuration and Hardware Synchronization: [5] [6] [7] [8] [9] [10] [11] [12]
- ISS SIMCOP DMA Register Summary: [13]

Table 8-1448. SIMCOP_DMA_CHAN_FRAME_i

Address Offset	0x0000 0098 + (0x30 * i)		
Physical Address	0x00 5202 0298 + (0x30 * i) 0x5506 0298 + (0x30 * i)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	Defines a frame. A frame is composed of 2D blocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								YCNT								RESERVED								XCNT							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved.	R	0x00
25:16	YCNT	Vertical count of 2D blocks per frame. Valid values are 1-1023	RW	0bxxxxxxxxxx
15:10	RESERVED	Reserved.	R	0x00
9:0	XCNT	Horizontal count of 2D blocks per frame. Valid values are 1-1023	RW	0bxxxxxxxxxx

Table 8-1449. Register Call Summary for Register SIMCOP_DMA_CHAN_FRAME_i

ISS SIMCOP DMA Module

- Logical Channel Data Transfer: [0] [1]
- ISS SIMCOP DMA Channel Configuration and Hardware Synchronization: [2] [3] [4] [5] [6] [7] [8] [9]
- ISS SIMCOP DMA Register Summary: [10]

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Table 8-1450. SIMCOP_DMA_CHAN_CURRENT_BLOCK_i

Address Offset	0x0000 00A0 + (0x30 * i)		
Physical Address	0x00 5202 02A0 + (0x30 * i) 0x5506 02A0 + (0x30 * i)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	SW could read the coordinates of the last transferred block. The status is reset when the channel is enabled (change the state of CTRL.ENABLE from 0 to 1).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BY								RESERVED								BX							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved.	R	0x00
25:16	BY	Vertical position of the last transferred 2D block in the frame.	R	0bxxxxxxxxxx
15:10	RESERVED	Reserved.	R	0x00
9:0	BX	Horizontal position of the last transferred 2D block in the frame.	R	0bxxxxxxxxxx

Table 8-1451. Register Call Summary for Register SIMCOP_DMA_CHAN_CURRENT_BLOCK_i

ISS SIMCOP DMA Module

- Logical Channel Data Transfer: [0]
- ISS SIMCOP DMA Register Summary: [1]

Table 8-1452. SIMCOP_DMA_CHAN_BLOCK_STEP_i

Address Offset	0x0000 00A4 + (0x30 * i)		
Physical Address	0x00 5202 02A4 + (0x30 * i) 0x5506 02A4 + (0x30 * i)	**Instance**	DMA_MAIN_L3 DMA_IPU
Description	Offset between 2D blocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								YSTEP								RESERVED								XSTEP							RESERVED

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:16	YSTEP	Vertical offset, in lines, between rows of 2D blocks. For contiguous 2D blocks YSTEP=YNUM Valid values are -8192 to +8191.	RW	0b0xxxxxxxxxxxxx
15	RESERVED		R	0
14:4	XSTEP	Horizontal offset, in 128-bit words, between 2D block columns. For contiguous 2D blocks XSTEP=XNUM Valid values are -1024 to +1023, that corresponds to 16 bytes to 16kBytes.	RW	0bxxxxxxxxxxx
3:0	RESERVED		R	0x0

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Table 8-1453. Register Call Summary for Register SIMCOP_DMA_CHAN_BLOCK_STEP_i

ISS SIMCOP DMA Module

- Logical Channel Data Transfer: [0] [1] [2] [3]
- ISS SIMCOP DMA Channel Configuration and Hardware Synchronization: [4] [5] [6] [7] [8] [9] [10] [11]
- ISS SIMCOP DMA Register Summary: [12]

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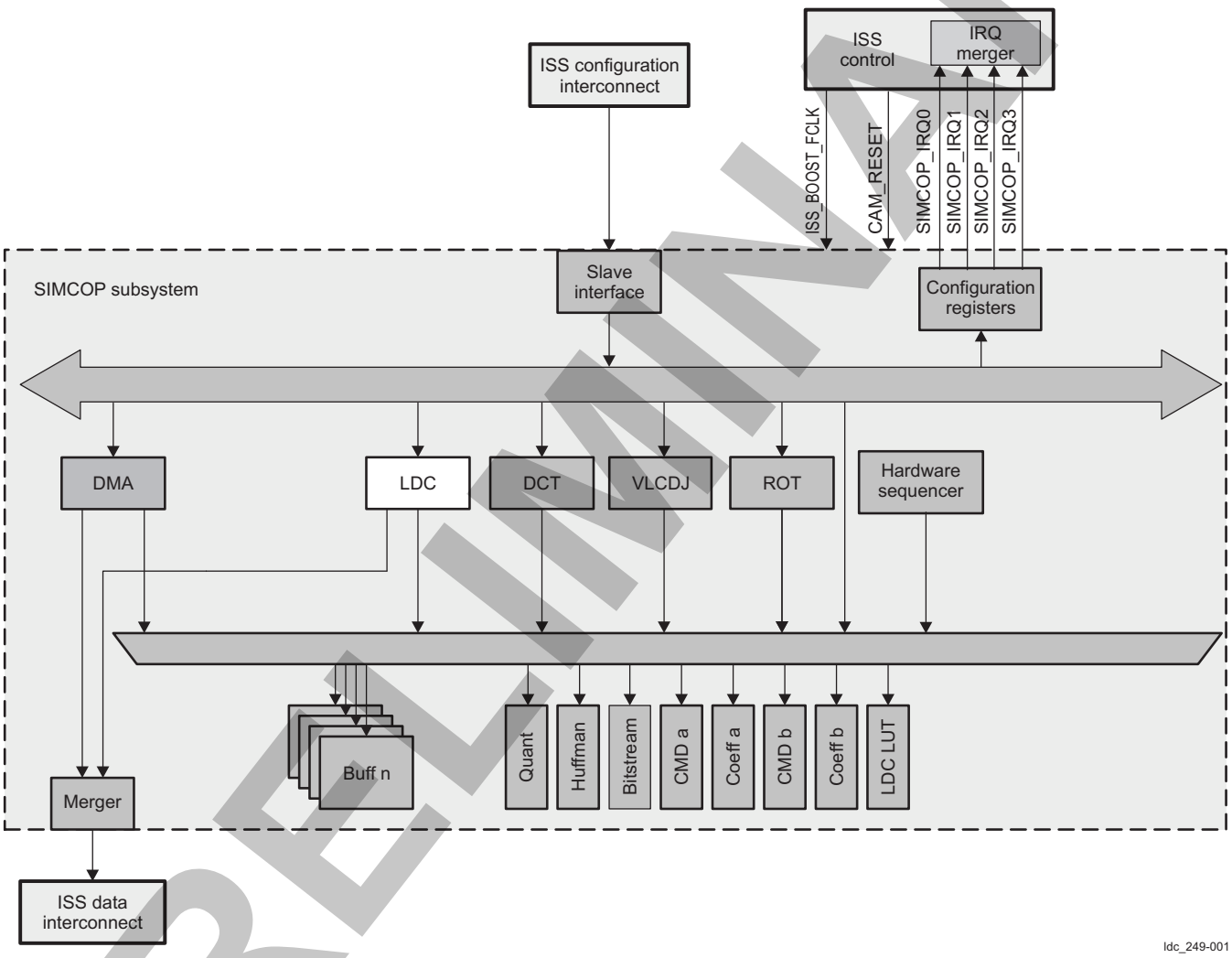
8.4.4 ISS SIMCOP LDC Module

This chapter describes the lens distortion correction (LDC) module in the still image coprocessor (SIMCOP) subsystem.

8.4.4.1 ISS SIMCOP LDC Overview

The lens distortion correction (LDC) module deals with lens geometric distortion issues, chromatic aberration, and affine transformation for camera images. Figure 8-279 is an overview of the LDC in the SIMCOP subsystem.

Figure 8-279. LDC in the SIMCOP Subsystem



For still image or video applications the LDC supports:

- Lens distortion correction:
  - YCbCr4:2:2/YCbCr4:2:0 data format input/output for post-image-pipe correction
  - Correct barrel distortion and pin-cushion distortion
  - Radius-to-magnification-factor table to accommodate various distortion functions through programming
  - Configurable center point and horizontal/vertical adjustment
  - One 256-entry lookup table for Y, Cb, and Cr
  - 8 bits for YCbCr

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  - Bicubic interpolation for Y and bilinear interpolation for Cb/Cr
  - Bilinear interpolation mode for Y to offer faster processing
  - Up to 16,383 x 16,383 image dimension
  - Format restriction:
    - YCbCr4:2:2 format: Tile width must be a multiple of 16.
    - YCbCr4:2:0 format: Tile width must be a multiple of 32.
- Image warping, scaling, and rotation:
  - Affine transformation for image warping, scaling, and rotation
  - 8 bits for YCbCr
  - Bicubic interpolation for Y and bilinear interpolation for Cb/Cr
  - Bilinear interpolation mode for Y to offer double throughput
  - Format restriction:
    - YCbCr4:2:2 format: Tile width must be a multiple of 16.
    - YCbCr4:2:0 format: Tile width must be a multiple of 32.
- Chromatic aberration correction:
  - Supports Bayer data in unpacked 12-bit per pixel, 8-bit per pixel A-Law, 8-bit per pixel unpacked, and 12-bit per pixel packed formats
  - Radius-to-magnification-factor table to accommodate various distortion functions through programming
  - Configurable center point and horizontal/vertical adjustment
  - Red and blue distortion only. Green pixels are copied to output.
  - Independent 128-entry lookup tables for red and blue
  - Bilinear interpolation
  - Up to 16,383 x 16,383 image dimension
  - Format restriction:
    - Unpacked 12-bit format: Tile width must be a multiple of 16.
    - A-Law 8-bit format: Tile width must be a multiple of 32.
    - Unpacked 8-bit format: Tile width must be a multiple of 32.
    - Packed 12-bit format: Tile width must be a multiple of 64.

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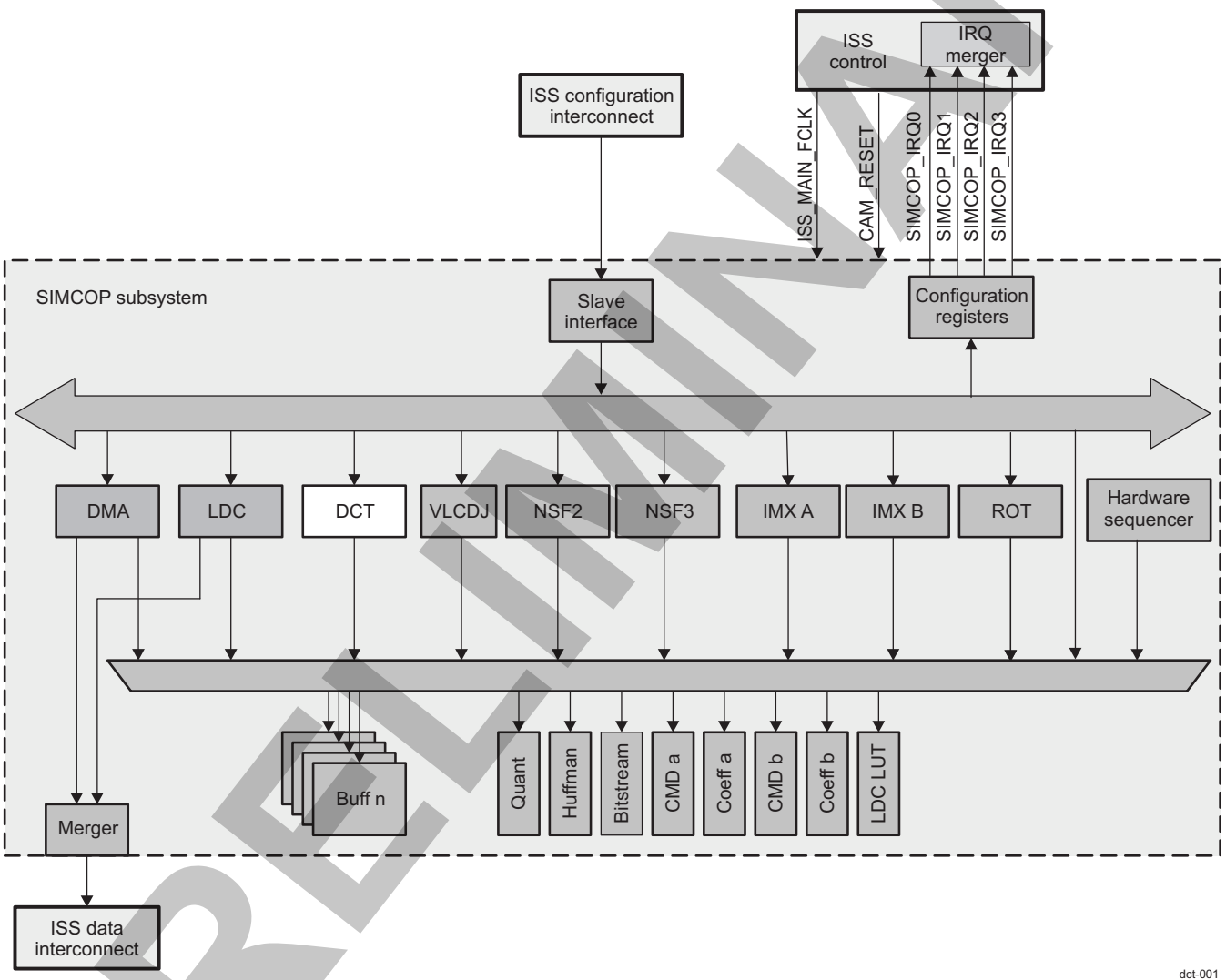
8.4.5 ISS SIMCOP Discrete Cosine Transform (DCT) Module

This section describes the discrete cosine transform (DCT) module in the still-image coprocessor (SIMCOP) subsystem.

8.4.5.1 ISS SIMCOP DCT Overview

The discrete cosine transform (DCT) module performs DCT and inverse DCT (IDCT) operations required for still-image coder/decoder (codec) applications. Figure 8-280 is an overview of the DCT in the still-image coprocessor (SIMCOP) subsystem.

Figure 8-280. DCT in the SIMCOP Subsystem



For still-image or video applications, the DCT supports:

- 8-bit data in the spatial domain (input to DCT or output of IDCT) with –128 offset on color components
- 16-bit data in the frequency domain
- Exact input/output (I/O) range:
  - DCT expected input range [0, 255], subtracting 128 offset before transform, output saturated to [–1024, 1023]
  - IDCT expected input range [–1280, 1079], adding 128 to inverse transform outcome and saturating to [0, 255]
  - IDCT input range is from DCT output range plus [–256, 256] worst-case quantization error

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- Configurable to process up to 32 microcontroller units (MCUs) at a time (21 MCUs for YUV4:2:0, and 32 MCUs for YUV4:2:2, because of memory size limitations
- The following formats are supported by the DCT:
  - 16 x 16-pixel block MCU for YUV4:2:0 format, spatial data storage follows NV12
  - 16 x 8-pixel block MCU for YUV4:2:2 format, spatial data storage follows UYVY
  - Sequential 8 x 8 block mode, other than YUV4:2:0 and YUV4:2:2, a color-neutral format to allow flexibility in color component configuration in MCU, processes up to 64 blocks per task
- JPEG baseline sequential is supported by sequential 8 x 8 block mode. Some post-processing to reorder data and color space conversion may be required.
- All frequency domain data are stored sequentially for each 8 x 8 block, 16 bits per data point.

8.4.5.2 ISS SIMCOP DCT Integration

The DCT is part of the SIMCOP subsystem in the imaging subsystem (ISS). Figure 8-281 shows the integration of the DCT in the SIMCOP subsystem.

Figure 8-281. DCT Engine Integration

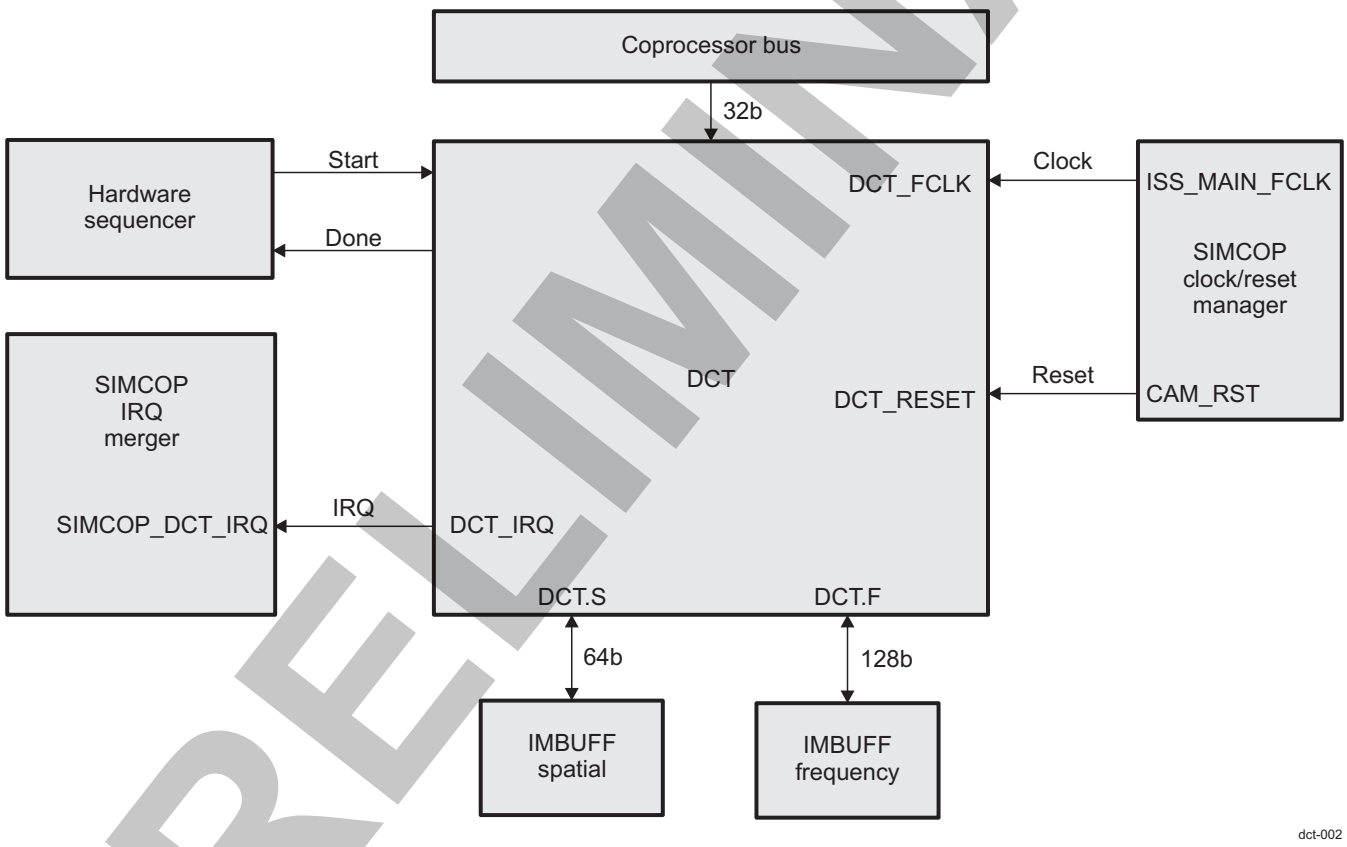

Table 8-1454 through Table 8-1456 list the integration attributes, clocks and resets, and hardware requests, respectively, for the DCT.

Table 8-1454. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
DCT	PD_CAM	

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Table 8-1455. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DCT	DCT_FCLK	ISS_MAIN_FCLK	ISS	Functional clock provided by CORE_ISS_MAIN_CLK from the power, reset, and clock management (PRCM) module . It is used by all ISS submodules and ISS top-level resources.
Resets				
DCT	DCT_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

For information about clock and reset management, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

Table 8-1456. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DCT	DCT_IRQ	SIMCOP_DCT_IRQ	SIMCOP IRQ merger	DCT operation is complete.

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*.

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8.4.5.3 ISS SIMCOP DCT Functional Description

8.4.5.3.1 ISS SIMCOP DCT Block Diagram

The DCT implements 8 × 8 2-dimensional (2D) DCT and IDCT specified in JPEG image coding standards:

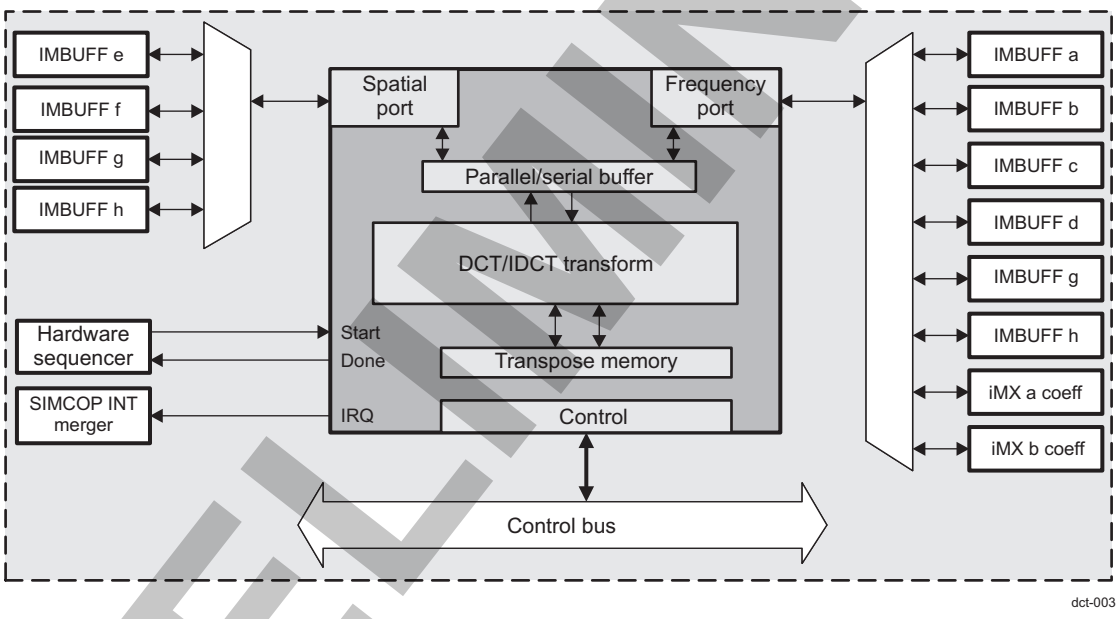
- In 4:2:0 mode, spatial domain data is organized in NV12 format. The frequency domain is organized as six blocks of 8 × 8.
- In 4:2:2 mode, spatial domain data is organized in UYVY format. The frequency domain is organized as four blocks of 8 × 8.
- In sequential 8 × 8 block mode, spatial and frequency domain data are organized as N blocks of 8 × 8 blocks.

NOTE:

- The spatial domain is the DCT input and IDCT output.
- The frequency domain is the DCT output and IDCT input.

Figure 8-282 is a block diagram of the DCT.

Figure 8-282. DCT Block Diagram



8.4.5.3.2 ISS SIMCOP DCT Power Management

Table 8-1457 describes the power-management features available for the DCT.

Table 8-1457. Local Power Management features

Feature	Registers	Description
Clock autogating	DCT_CFG[5] AUTOGATING	Free-running or autogating modes are available.

8.4.5.3.3 ISS SIMCOP DCT Interrupt Requests

Table 8-1458 lists the event flags, and their mask, that can cause module interrupts.

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Table 8-1458. Events

Event Flag	Event Mask	Map to	Description
N/A	DCT_CFG[3] INTEN	DCT_IRQ	End of processing

8.4.5.3.4 Control and Status

The DCT is controlled through the control registers accessed through the coprocessor bus by an external initiator. Before starting the DCT, the buffer memory must be configured for DCT access and initialized, and the control register must be set (for more information about DCT/IDCT processing, see Section 8.4.5.3.4.1, *DCT Configuration*).

The DCT_CFG[4] TRIG_SRC bit is used to select the DCT start source:

- If TRIG_SRC = 0, the DCT is started through the DCT_CTRL[0] EN bit.
- If TRIG_SRC = 1, the DCT is started by a hardware-start signal generated by the SIMCOP hardware sequencer.

When the DCT is configured for one trigger, the other trigger has no effect on the DCT.

An external initiator can read the state of the DCT (running or not running) by reading the DCT_CTRL[15] BUSY bit. When the BUSY bit goes back to 0, processing is complete (TRIG_SRC = 0 or 1).

Before starting the DCT, the DCT_SPTR and DCT_FPTR registers must be configured with spatial and frequency addresses. Figure 8-283 shows the use of spatial and frequency addresses.

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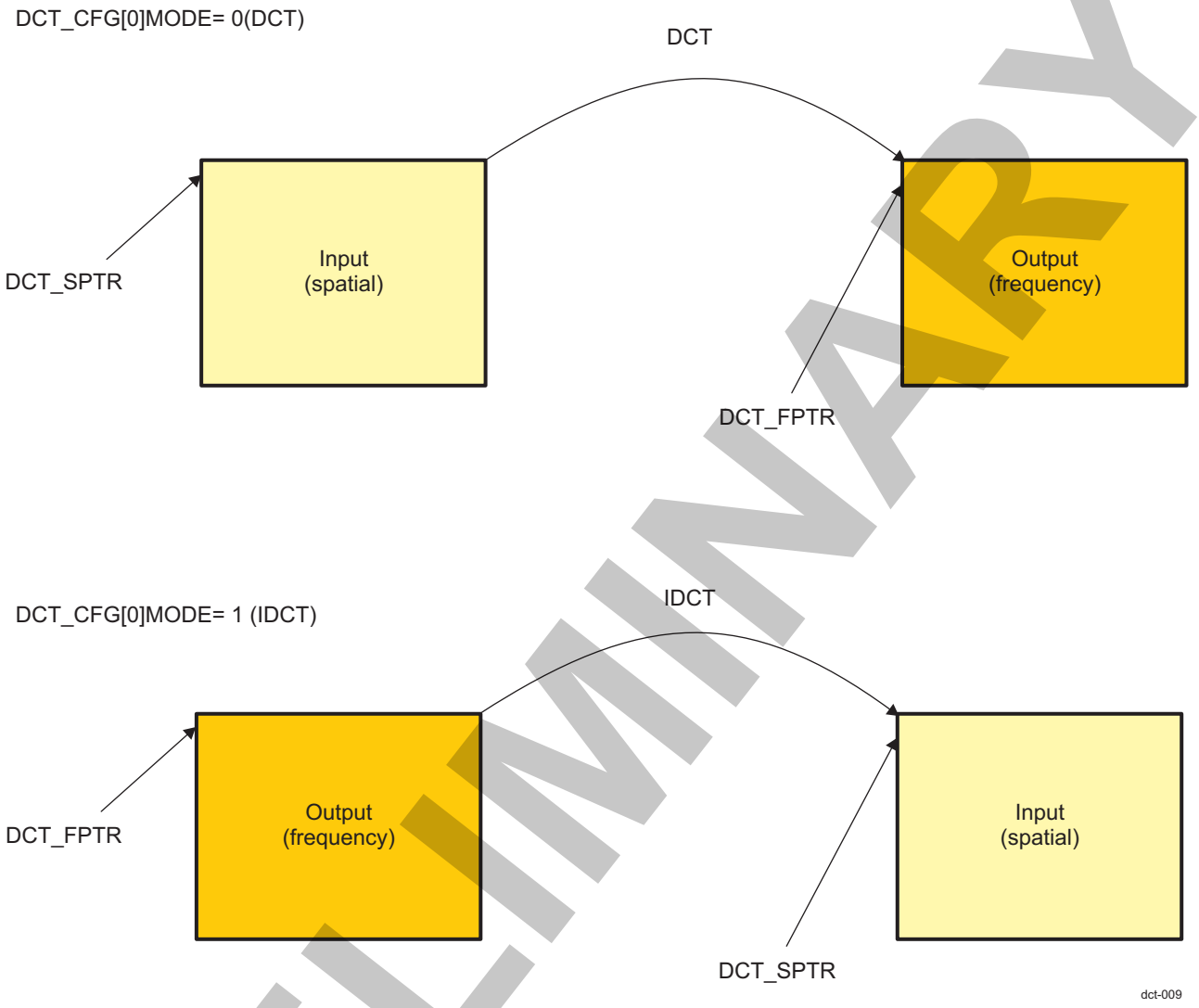
Figure 8-283. DCT I/O Address Configuration



An interrupt can be generated when DCT operation completes (the configured number of MCUs for YUV4:2:0/4:2:2 mode, or the number of blocks for sequential block mode). To enable interrupt generation, set the DCT_CFG[3] INTEN bit to 1.

When the DCT_CFG[3] INTEN bit is set to 0, no interrupt generation is performed.

8.4.5.3.4.1 DCT Configuration

The following features can be configured in the DCT register:

- DCT module operation: The DCT_CFG[0] MODE bit configures the processing:
  - MODE = 0: DCT processing
  - MODE = 1: IDCT processing
- Number of MCUs to process: The number of MCUs to process –1 is configured in the DCT_CFG[13:8] NMCUS bit field:
  - YUV4:2:0 maximum MCUs = 21 (memory limitation, 126 blocks)
  - YUV4:2:2 maximum MCUs = 32 (128 blocks)
  - Sequential maximum MCUs = 64 (64 blocks)

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8.4.5.3.5 Data Format

The DCT reads and writes data from and to image buffers. I/O format can be configured in the DCT_CFG[2:1] FMT bit field. The following formats can be configured:

- YUV4:2:0
- YUV4:2:2
- Sequential

8.4.5.3.5.1 YUV4:2:0 Format

In JPEG YUV4:2:0 format, each MCU is 16 × 16 pixels, and has 16 × 16 Y data points, 8 × 8 U data points, and 8 × 8 V data points. Each square array of 8 × 8 data points is called a block. Thus, an MCU with a YUV4:2:0 format has four Y blocks, one U block, and one V block.

This module follows the NV12 data storage format for YUV4:2:0 spatial data. For YUV4:2:0 format:

- line_offset_in_bytes = (DCT_CFG[13:8] NMCUS + 1) × 16
- starting_addr_uv = DCT_SPTR + (DCT_CFG[13:8] NMCUS + 1) × 256

Figure 8-284 shows the organization of the data for two MCUs in the spatial domain, when the DCT is configured to process two MCUs. To select the YUV4:2:0 format, write 0 x 0 in the DCT_CFG[2:1] FMT bit field. YUV4:2:0 processes six blocks (four Y, one U, and one V) during each MCU DCT processing.

Figure 8-284. YUV4:2:0 Format Data Order

Byte offset	0	1	2	3	...	15	16	17	...	31
0	Y(0,0)	Y(1,0)	Y(2,0)	Y(3,0)	...	Y(15,0)	Y(16,0)	Y(17,0)	...	Y(31,0)
32	Y(0,1)	Y(1,1)	Y(2,1)	Y(3,1)	...	Y(15,1)	Y(16,1)	Y(17,1)	...	Y(31,1)
64	Y(0,2)	Y(1,2)	Y(2,2)	Y(3,2)	...	Y(15,2)	Y(16,2)	Y(17,2)	...	Y(31,2)
	:									
480	Y(0,15)	Y(1,15)	Y(2,15)	Y(3,15)	...	Y(15,15)	Y(16,15)	Y(17,15)	...	Y(31,15)
512	U(0,0)	V(0,0)	U(2,0)	V(2,0)	...	V(14,0)	U(16,0)	V(16,0)	...	V(30,0)
544	U(0,2)	V(0,2)	U(2,2)	V(2,2)	...	V(14,2)	U(16,2)	V(16,2)	...	V(30,2)
	:									
736	U(0,14)	V(0,14)	U(2,14)	V(2,14)	...	V(14,14)	U(16,14)	V(16,14)	...	V(30,14)

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Each YUV4:2:0 has four Y blocks, one U block, and one V block. For the first MCU in Figure 8-284, the blocks are:

- Y_Block 0:
  - Y(0, 0), Y(1, 0), ..., Y(7, 0)
  - Y(0, 1), Y(1, 1), ..., Y(7, 1)
  - ....
  - Y(0, 7), Y(1, 7), ..., Y(7, 7)
- Y_Block 1:
  - Y(8, 0), Y(9, 0), ..., Y(15, 0)
  - Y(8, 1), Y(9, 1), ..., Y(15, 1)
  - ....
  - Y(8, 7), Y(9, 7), ..., Y(15, 7)
- Y_Block 2:
  - Y(0, 8), Y(1, 8), ..., Y(7, 8)
  - Y(0, 9), Y(1, 9), ..., Y(7, 9)
  - ....
  - Y(0, 15), Y(1, 15), ..., Y(7, 15)
- Y_Block 3:
  - Y(8, 8), Y(9, 8), ..., Y(15, 8)

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  - Y(8, 9), Y(9, 9), ..., Y(15, 9)
  - ....
  - Y(8, 15), Y(9, 15), ..., Y(15, 15)
- U_Block:
  - U(0, 0), U(2, 0), ..., U(14, 0)
  - U(0, 2), U(2, 2), ..., U(14, 2)
  - ....
  - U(0, 14), U(2, 14), ..., U(14, 14)
- V_Block:
  - V(0, 0), V(2, 0), ..., V(14, 0)
  - V(0, 2), V(2, 2), ..., V(14, 2)
  - ....
  - V(0, 14), V(2, 14), ..., V(14, 14)

8.4.5.3.5.2 YUV4:2:2 Format

In JPEG YUV4:2:2 format, each MCU is 16 x 8 pixels and has 16 x 8 Y data points, 8 x 8 U data points, and 8 x 8 V data points. Thus, an MCU with a 4:2:2 format has two Y blocks, one U block, and one V block.

This module follows the UYVY data storage format for YUV4:2:2 spatial data. For YUV4:2:2 format:

line_offset_in_bytes = (DCT_CFG[13:8] NMCUS + 1) × 16

starting_addr_uv=DCT_SPTR + (DCT_CFG[13:8] NMCUS+1) * 256

Figure 8-285 shows the organization of the data for two MCUs in the spatial domain, when the DCT is configured to process two MCUs. To select the YUV4:2:2 format, write 0 x 1 in the DCT_CFG[2:1] FMT bit field. YUV4:2:2 processes four blocks (two Y, one U, and one V) during each MCU DCT processing.

Figure 8-285. YUV4:2:2 Format Data Order

Byte Offset																
	0	1	2	3	4	5	6	7	...	31	32	33	34	35	...	63
0	U(0,0)	Y(0,0)	V(0,0)	Y(1,0)	U(2,0)	Y(2,0)	V(2,0)	Y(3,0)	...	Y(15,0)	U(16,0)	Y(16,0)	V(16,0)	Y(17,0)	...	Y(31,0)
64	U(0,1)	Y(0,1)	V(0,1)	Y(1,1)	U(2,1)	Y(2,1)	V(2,1)	Y(3,1)	...	Y(15,1)	U(16,1)	Y(16,1)	V(16,1)	Y(17,1)	...	Y(31,1)
128	U(0,2)	Y(0,2)	V(0,2)	Y(1,2)	U(2,2)	Y(2,2)	V(2,2)	Y(3,2)	...	Y(15,2)	U(16,2)	Y(16,2)	V(16,2)	Y(17,2)	...	Y(31,2)
	:															
448	U(0,7)	Y(0,7)	V(0,7)	Y(1,7)	U(2,7)	Y(2,7)	V(2,7)	Y(3,7)	...	Y(15,7)	U(16,7)	Y(16,7)	V(16,7)	Y(17,7)	...	Y(31,7)

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Each YUV4:2:2 has two Y blocks, one U block, and one V block. The four blocks of the first MCU are:

- Y_Block 0:
  - Y(0, 0), Y(1, 0), ..., Y(7, 0)
  - Y(0, 1), Y(1, 1), ..., Y(7, 1)
  - ....
  - Y(0, 7), Y(1, 7), ..., Y(7, 7)
- Y_Block 1:
  - Y(8, 0), Y(9, 0), ..., Y(15, 0)
  - Y(8, 1), Y(9, 1), ..., Y(15, 1)
  - ....
  - Y(8, 7), Y(9, 7), ..., Y(15, 7)

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8.4.5.3.5.3 Sequential Block Format

The sequential block format supports any color format other than YUV4:2:0 or YUV4:2:2. There is no notion of colors, and each 8 x 8 block is ordered sequentially. The DCT can be configured to process N blocks (versus N MCUs for YUV4:2:0 and YUV4:2:2, N is up to 64). In this format:

- Block i =
  - X(8*i, 0), X(8*i+1, 0), ..., X(8*i+7, 0)
  - X(8*i, 1), X(8*i+1, 1), ..., X(8*i+7, 1)
  - ....
  - X(8*i, 7), X(8*i+1, 7), ..., X(8*i+7, 7)

To select sequential block format, write 0 x 2 in the DCT_CFG[2:1] FMT bit field.

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8.4.5.4 ISS SIMCOP DCT Basic Programming Model

8.4.5.4.1 Initialization of Surrounding Modules

To initialize the DCT, the surrounding modules must be initialized. Table 8-1459 lists these modules.

Table 8-1459. Initialization of Surrounding Modules

Module	Minimum Required Setting	Optional Settings
CLKC	Enable the SIMCOP clock.	
Buffers	Configure DCT access to the image buffer.	
SIMCOP CTRL		Configure SIMCOP CTRL to handle DCT interrupts.

8.4.5.4.2 Using the DCT for DCT Processing

To configure the DCT for DCT processing, software must follow the procedure listed in Table 8-1460.

Table 8-1460. DCT Processing Procedure

Step	Register/Bit Field	Value
Prepare data in buffer memory.	SIMCOP buffers	
Switch buffer access to the DCT.	SIMCOP buffers	
Configure the start of the DCT input address (address must be in the memory buffer).	DCT_SPTR[12:5] ADDR	Start address (spatial domain)
Configure the start of the DCT output address (address must be in the memory buffer).	DCT_FPTR[13:4] ADDR	Start address (frequency domain)
Set the DCT_CFG register.	DCT_CFG[0] MODE	0 (DCT mode)
	DCT_CFG[2:1] FMT	Depends on data format
	DCT_CFG[3] INTEN	0: No interrupt 1: Interrupt at end of processing
	DCT_CFG[4] TRIG_SRC	1: Start controlled by hardware signal 0: Start controlled by a register
	DCT_CFG[13:8] NMCUS	Number of MCUs to process
IF: DCT_CFG[4] TRIG_SRC = 0		
Start DCT through the register.	DCT_CTRL[0] EN	1
ELSE		
Start the DCT using the hardware sequencer.	SIMCOP hardware sequencer	
ENDIF		

The DCT is now processing the blocks. To detect the end of DCT processing:

- If DCT_CFG[3] INTEN = 1, wait for the interrupt signal.
- If DCT_CFG[3] INTEN = 0, the processor must poll the DCT_CTRL[15] BUSY bit. When the BUSY bit is 0, processing is complete.

When DCT processing completes, the frequency output result is stored in the memory buffer at the address given by the DCT_FPTR[13:4] ADDR bit field.

8.4.5.4.3 Using the DCT for IDCT Processing

To configure the DCT for IDCT processing, software must follow the procedure listed in Table 8-1461.

Table 8-1461. IDCT Processing Procedure

Step	Register/Bit Field	Value
Prepare data in buffer memory.	SIMCOP buffers	
Switch buffer access to the DCT.	SIMCOP buffers	

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Table 8-1461. IDCT Processing Procedure (continued)

Step	Register/Bit Field	Value
Configure the start of the DCT output address (address must be in the memory buffer).	DCT_SPTR[12:5] ADDR	Start address (spatial domain)
Configure the start of the DCT input address (address must be in the memory buffer).	DCT_FPTR[13:4] ADDR	Start address (frequency domain)
Set the DCT_CFG register.	DCT_CFG[0] MODE	1 (IDCT mode)
	DCT_CFG[2:1] FMT	Depends on data format
	DCT_CFG[3] INTEN	0: No interrupt 1: Interrupt at end of processing
	DCT_CFG[4] TRIG_SRC	1: Start controlled by a hardware signal 0: Start controlled by a register
	DCT_CFG[13:8] NMCUS	Number of MCUs to process
IF: DCT_CFG[4] TRIG_SRC = 0		
Start the DCT through a register.	DCT_CTRL[0] EN	1
ELSE		
Start the DCT using hardware sequencer.	SIMCOP hardware sequencer	
ENDIF		

The DCT is now processing the blocks. To detect the end of DCT processing:

- If DCT_CFG[3] INTEN = 1, wait for the interrupt signal.
- If DCT_CFG[3] INTEN = 0, the processor must poll the DCT_CTRL[15] BUSY bit. When the BUSY bit is 0, processing is complete.

When IDCT processing completes, the spatial output result is stored in the memory buffer at the address given by the DCT_SPTR[12:5] ADDR bit field.

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8.4.5.5 ISS SIMCOP DCT Register Manual

8.4.5.5.1 ISS SIMCOP DCT Instance Summary

Table 8-1462 summarizes the DCT instance.

Table 8-1462. DCT Instance Summary

Module Name	L3_MAIN Base Address	IPU Base Address	Size
DCT	0x5202 0800	0x5506 0800	32 bytes

8.4.5.5.2 ISS SIMCOP DCT Registers

8.4.5.5.2.1 ISS SIMCOP DCT Register Summary

Table 8-1463 summarizes the DCT register mapping.

Table 8-1463. DCT Register Mapping Summary

Register	Type	Register Width (Bits)	Address Offset	DCT L3_MAIN Physical Address	DCT IPU Physical Address
DCT_REVISION	R	32	0 x 0000 0000	0 x 5202 0800	0 x 5506 0800
DCT_CTRL	RW	32	0 x 0000 0004	0 x 5202 0804	0 x 5506 0804
DCT_CFG	RW	32	0 x 0000 0008	0 x 5202 0808	0 x 5506 0808
DCT_SPTR	RW	32	0 x 0000 000C	0 x 5202 080C	0 x 5506 080C
DCT_FPTR	RW	32	0 x 0000 0010	0 x 5202 0810	0 x 5506 0810

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8.4.5.5.2.2 ISS SIMCOP DCT Register Description

Table 8-1464 through Table 8-1472 describe the registers in detail.

Table 8-1464. DCT_REVISION

Address Offset	0 x 0000 0000		
Physical Address	See Table 8-1463.	**Instance**	DCT
Description	IP Revision		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

	Bits	Field Name	Description	Type	Reset
(1)	31:0	REVISION	IP Revision	R	

(1) TI internal data

Table 8-1465. Register Call Summary for Register DCT_REVISION

ISS SIMCOP Discrete Cosine Transform (DCT) Module

- ISS SIMCOP DCT Register Summary: [0]

Table 8-1466. DCT_CTRL

Address Offset	0 x 0000 0004		
Physical Address	See Table 8-1463.	**Instance**	DCT
Description	DCT control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUSY	RESERVED														EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Read returns 0.	R	0 x 0000
15	BUSY	IDCT/busy status 0: Idle 1: Busy	R	0 x 0
14:1	RESERVED	Read returns 0.	R	0 x 0000
0	EN	Write 1 when DCT_CFG[4] TRIG_SRC = 0 to start module operation. Read returns 0.	W	0 x 0

Table 8-1467. Register Call Summary for Register DCT_CTRL

ISS SIMCOP Discrete Cosine Transform (DCT) Module

- Control and Status: [0] [1]
- Using the DCT for DCT Processing: [2] [3]
- Using the DCT for IDCT Processing: [4] [5]
- ISS SIMCOP DCT Register Summary: [6]

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Table 8-1468. DCT_CFG

Address Offset	0 x 0000 0008		
Physical Address	See Table 8-1463.	**Instance**	DCT
Description	DCT configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NMCUS								RESERVED		AUTOGATING	TRIG_SRC	INTEN	FMT		MODE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0 x 00000
13:8	NMCUS	Number of MCUs (for FMT = 0, 1) or blocks (for FMT = 2) 0 = 1 MCU or block 1 = 2 MCUs or blocks ... 63 = 64 MCUs or blocks	RW	0 x 00
7:6	RESERVED	Read returns 0.	R	0 x 0
5	AUTOGATING	Internal clock gating on interface and functional clocks 0: Clocks are free-running 1: Clocks are gated off in subblocks that are not required for operation.	RW	0 x 0
4	TRIG_SRC	Trigger source 0: Memory mapper register 1: Hardware start signal	RW	0 x 0
3	INTEN	0: Interrupt disabled 1: Interrupt enabled	RW	0 x 0
2:1	FMT	Data format 0: YUV4:2:0 format 1: YUV4:2:2 format 2: Sequential blocks format 3: Reserved	RW	0 x 0
0	MODE	0: DCT 1: IDCT	RW	0 x 0

Table 8-1469. Register Call Summary for Register DCT_CFG

ISS SIMCOP Discrete Cosine Transform (DCT) Module

- ISS SIMCOP DCT Power Management: [0]
- ISS SIMCOP DCT Interrupt Requests: [1]
- Control and Status: [2] [3] [4]
- DCT Configuration: [5] [6]
- Data Format: [7]
- YUV4:2:0 Format: [8] [9] [10]
- YUV4:2:2 Format: [11] [12] [13]
- Sequential Block Format: [14]
- Using the DCT for DCT Processing: [15] [16] [17] [18] [19] [20] [21] [22] [23]
- Using the DCT for IDCT Processing: [24] [25] [26] [27] [28] [29] [30] [31] [32]
- ISS SIMCOP DCT Register Summary: [33]
- ISS SIMCOP DCT Register Manual: [34]

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Table 8-1470. DCT_SPTR

Address Offset	0 x 0000 000C		
Physical Address	See Table 8-1463.	**Instance**	DCT
Description	Spatial-domain data pointer, byte address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR								RESERVED							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Read returns 0.	R	0 x 00000
12:5	ADDR	Address in 256-bit words Intention is that software write a byte address into the register. Hardware ignores the lowest 5 bits and bits 12..5 specifies the 256-bit/word memory address..	RW	0 x 00
4:0	RESERVED	Read returns 0.	R	0 x 00

Table 8-1471. Register Call Summary for Register DCT_SPTR

ISS SIMCOP Discrete Cosine Transform (DCT) Module

- Control and Status: [0]
- YUV4:2:0 Format: [1]
- YUV4:2:2 Format: [2]
- Using the DCT for DCT Processing: [3]
- Using the DCT for IDCT Processing: [4] [5]
- ISS SIMCOP DCT Register Summary: [6]

Table 8-1472. DCT_FPTR

Address Offset	0 x 0000 0008		
Physical Address	See Table 8-1463.	**Instance**	DCT
Description	Frequency-domain data pointer, byte address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR												RESERVED			

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0 x 00000
13:4	ADDR	Address in 128-bit words. Intention is that software write a byte address into the register. Hardware ignores the lowest 4 bits and bits 13..4 specifies the 128-bit/word memory address.	RW	0 x 000
3:0	RESERVED	Read returns 0.	R	0 x 0

Table 8-1473. Register Call Summary for Register DCT_FPTR

ISS SIMCOP Discrete Cosine Transform (DCT) Module

- Control and Status: [0]
- Using the DCT for DCT Processing: [1] [2]
- Using the DCT for IDCT Processing: [3]
- ISS SIMCOP DCT Register Summary: [4]

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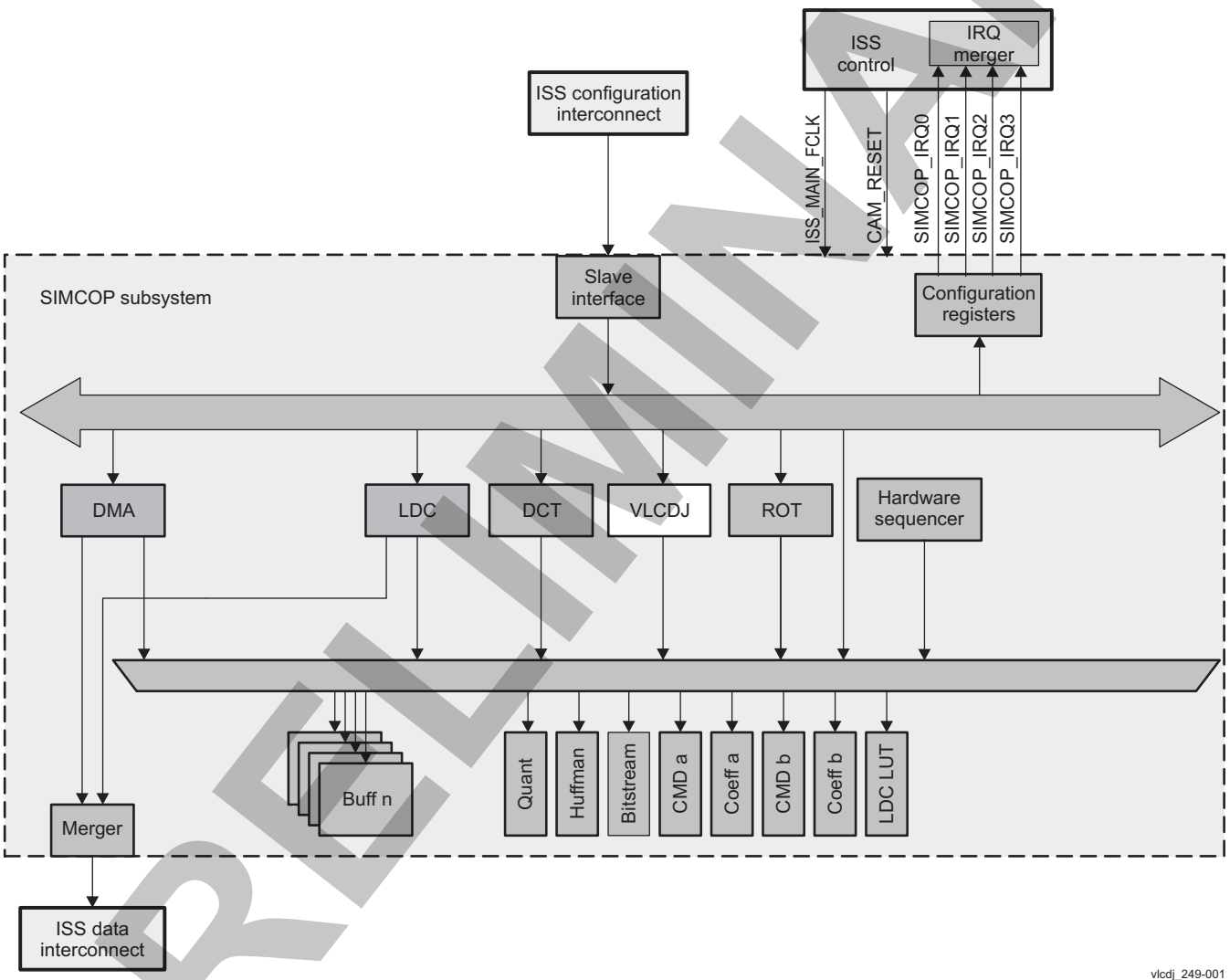
8.4.6 ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

This section describes the variable-length coder/decoder for JPEG (VLCDJ) module in the still-image coprocessor (SIMCOP) subsystem.

8.4.6.1 ISS SIMCOP VLCDJ Overview

The variable-length coder/decoder for JPEG (VLCDJ) module handles quantization (Q) and variable-length coding (VLC) in JPEG encoding, and variable-length decoding (VLD) and inverse quantization (IQ) in JPEG decoding. These operations are required for JPEG image compression and decompression. Figure 8-286 is an overview of the VLCDJ in the still-image coprocessor (SIMCOP) subsystem.

Figure 8-286. VLCDJ in the SIMCOP Subsystem



The VLCDJ supports the following operations:

- Q and VLC for JPEG encoding
- VLD and IQ for JPEG decoding
- Data formats:
  - YUV4:2:0 format in 16 × 16-pixel microcontroller unit (MCU)
  - YUV4:2:2 format in 16 × 8-pixel MCU
  - Sequential block mode to support arbitrary color component configuration within JPEG baseline sequential (software intervention required to context-switch among color components)

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- Configurable for number of MCUs per initiation (up to 21 MCUs for YUV4:2:0, 32 MCUs for YUV4:2:2, 64 8 × 8 blocks for sequential block mode)
- Discrete cosine transform (DCT) coefficients are stored sequentially for each 8 × 8 block, 16 bits per data point
- Stall processing for interface with bitstream data overrun/underrun protection
- Insertion of restart markers during encoding (YUV4:2:0, YUV4:2:2, sequential block modes)
- Record of restart marker locations during encoding (YUV4:2:0, YUV4:2:2 only)
- Processing of restart markers on the MCU boundary during decoding, reset of direct coefficient (DC) predictors as required by the JPEG standard (YUV4:2:0, YUV4:2:2, sequential block modes)

8.4.6.2 ISS SIMCOP VLCDJ Integration

The VLCDJ is part of the SIMCOP subsystem in the imaging subsystem (ISS). Figure 8-287 shows the integration of the VLCDJ in the SIMCOP subsystem.

Figure 8-287. VLCDJ Engine Integration

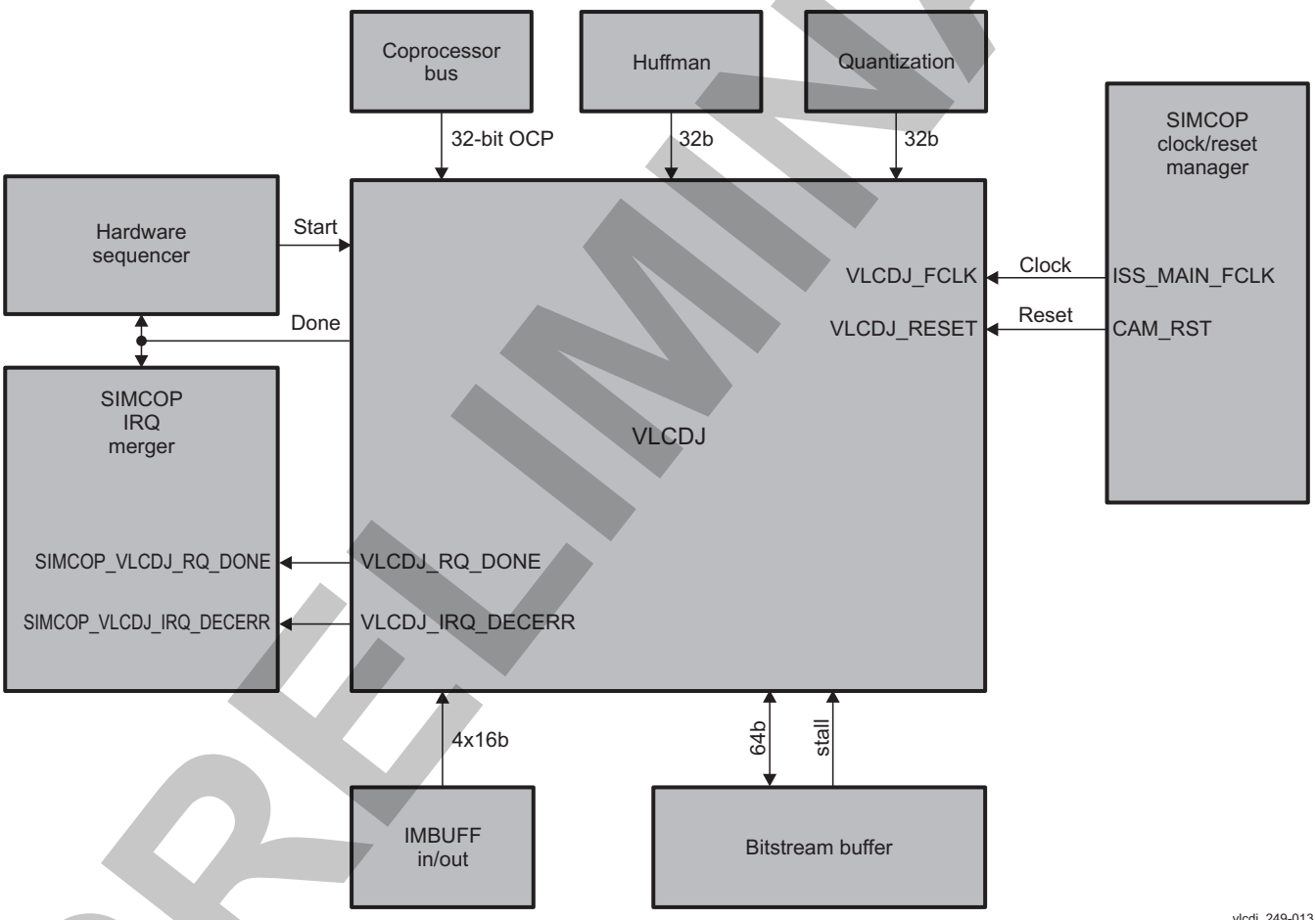

Table 8-1474 through Table 8-1476 list the integration attributes, clocks and resets, and hardware requests, respectively, for the VLCDJ.

Table 8-1474. Integration Attributes

Module Instance	Attributes
	Power Domain
VLCDJ	PD_CAM

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Table 8-1475. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
VLCDJ	VLCDJ_FCLK	ISS_MAIN_FCLK	ISS	Functional clock provided by CORE_ISS_MAIN_CLK from the power, reset, and clock management (PRCM) module. It is used by all ISS submodules and ISS top-level resources.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
VLCDJ	VLCDJ_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

For information about clock and reset management, see Section 8.4.1.2.2, *ISS SIMCOP Local Power and Clock Management*.

Table 8-1476. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
VLCDJ	VLCDJ_RQ_DONE	SIMCOP_VLCDJ_IRQ_DONE	SIMCOP IRQ merger	VLCDJ operation has been completed
VLCDJ	VLCDJ_IRQ_DECERR	SIMCOP_VLCDJ_IRQ_DECERR	SIMCOP IRQ merger	VLCDJ decode operation has encountered error.

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*.

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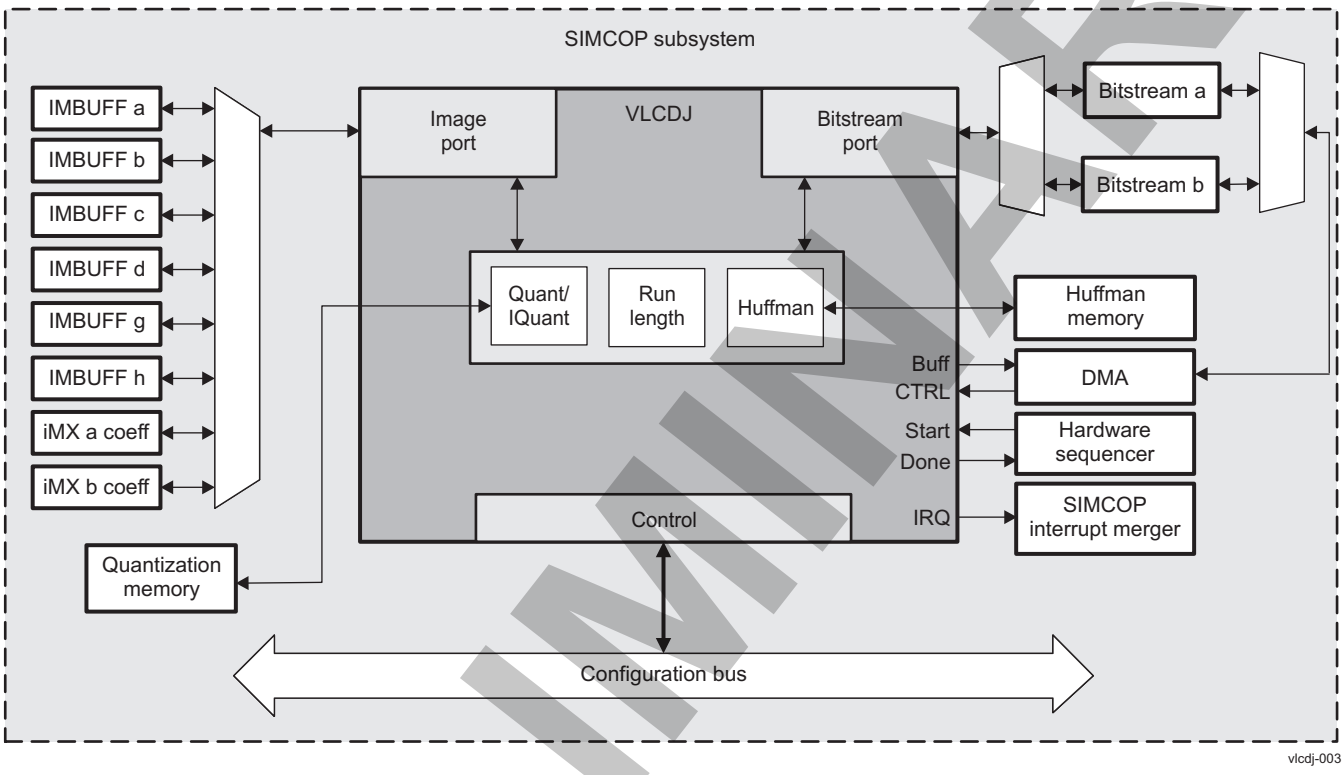
8.4.6.3 ISS SIMCOP VLCDJ Functional Description

8.4.6.3.1 ISS SIMCOP VLCDJ Block Diagram

The VLCDJ implements quantization, run-length encode, and Huffman encode stages of JPEG compression, and Huffman decode, run-length expansion, and dequantization stages of JPEG decompression. Figure 8-288 is a block diagram of the VLCDJ with connected memories and modules.

Figure 8-288. VLCDJ Block Diagram



8.4.6.3.2 ISS SIMCOP VLCDJ Power Management

The VLCDJ uses clock autogating to conserve power. When any substantial subblocks are not in use, the corresponding clock trees are gated off. Table 8-1477 describes the power-management feature available for the VLCDJ.

Table 8-1477. Local Power-Management Feature

Feature	Registers	Description
Clock autogating	VLCDJ_CTRL[3] AUTOGATING	Free-running or autogating modes are available.

8.4.6.3.3 ISS SIMCOP VLCDJ Interrupt Requests

Table 8-1478 lists the event flags and their masks that can cause module interrupts.

Table 8-1478. Events

Event Flag	Event Mask	Map to	Description
N/A	VLCDJ_CTRL[4] INTEN_DONE	VLCDJ_RQ_DONE	VLCDJ operation completed
N/A	VLCDJ_CTRL[5] INTEN_ERR	VLCDJ_IRQ_DECERR	Error occurred

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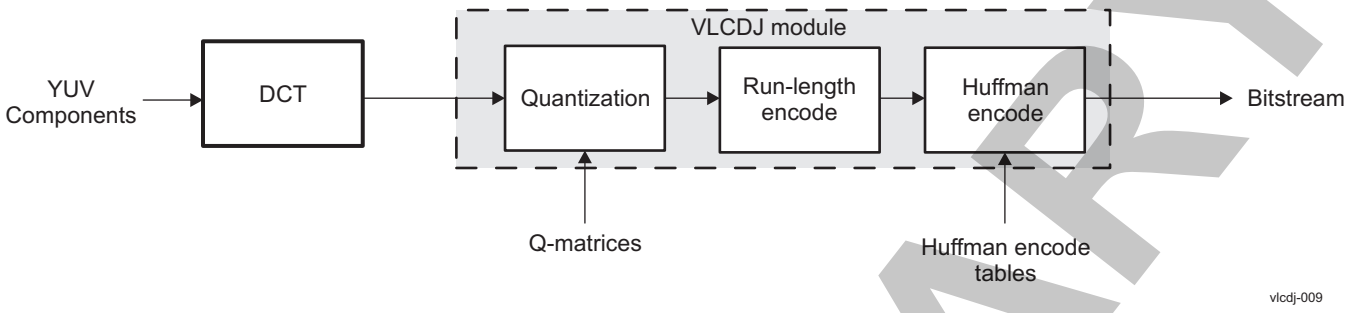
8.4.6.3.4 ISS SIMCOP VLCDJ in JPEG Encoding Flow

Figure 8-289 shows the JPEG compression or encoding flow.

Figure 8-289. JPEG Encoding Flow



The DCT coefficients are quantized by dividing each data point with a quantizer. The quantizers form an 8 × 8 matrix for Luma Y, and another 8 × 8 matrix for U and V, and the matrices are fixed in each image. The quantizer matrices can vary between images, and are sometimes fine-tuned in a multiple-pass process to regulate the compressed JPEG file size.

For quantization, VLCDJ reads a reciprocal of the quantizer values (16 bits per entry carrying 2^{15}/quant) so that hardware performs multiplications rather than divisions. The result is rounded to the nearest integer.

After quantization, the DC terms (the first term in each 8 × 8 block of DCT coefficients) are differentially coded within each color. Thus, three predictors are used for the common formats.

Next, the coefficients are scanned in a zigzag order (the same order for all colors) to form DC term + zero-run and nonzero level pairs for the alternative coefficient (AC) terms. The run-level pairs are then coded with a Huffman table.

The DC level is first categorized into size groups, basically the number of bits that represents the absolute value of the level. This size is translated to a bit segment using the Huffman table. Then, additional bits are appended to represent the exact DC level.

For AC run-level pairs, the process is similar. Each AC level is first categorized into size groups, basically the number of bits that represents the absolute value of the level. Then the size and the run are combined and translated to a bit segment using the Huffman table. Then, additional bits are appended to represent the exact AC level.

The number of additional bits to encode after the Huffman-coded segment, for DC or AC level, equals the size value. For example, coefficient values –3, –2, and 3 are of size 2, because 2 bits are required to represent the absolute values 2 and 3. There are four coefficient values in the size –2 category, so 2 additional bits are required to uniquely identify each value.

Some special symbols go with the AC run/size pairs. The ZRL symbol represents a run of 15 zeros, and is used to code unusually long zero runs. The EOB symbol represents end of block, meaning that there are only 0 AC coefficients at the end.

In the bitstream management level, after each byte of 0xFF, a byte of 0 is inserted to prevent the decoder from detecting special markers in the bitstream.

Because the VLCDJ handles multiple MCUs and allows restart marker insertion in MCU boundaries inside a task, the inserted flags are flagged to prevent the insertion of a 0 byte after 0xFF.

8.4.6.3.5 ISS SIMCOP VLCDJ in JPEG Decoding Flow

Decoding or decompression operates in the reverse order, as shown in Figure 8-290.

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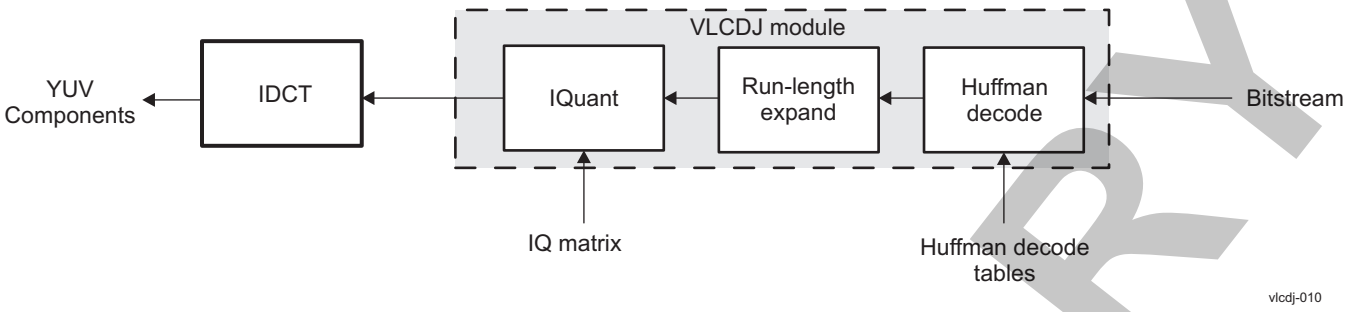
Figure 8-290. JPEG Decoding Flow



1. In decoding, in the MCU data section, when the VLCDJ recognizes the 0xFF byte in the bitstream, it detects whether the next byte is a 0 byte. If it is, the 0 byte is removed and decoding continues as if the 0 byte is not there (the 0xFF byte is kept). If the next byte is not a 0 byte, the VLCDJ flags this as a JPEG data error. This can be caused by an earlier bitstream error that causes the module to parse outside the MCU entropy data and into markers that are not supported by the module.
2. Because the VLCDJ decodes for multiple MCUs, restart markers can occur in MCU boundaries. Restart marker detection and processing work with the 0 byte removal logic to ensure that restart markers are detected and removed correctly. When the VLCDJ detects a restart marker, it resets the DC predictors in the IQ stage.
3. The VLCDJ looks up the Huffman table to convert a variable-length bit segment into a DC size or an AC run/size pair. The number of additional bits equal to the size is extracted and the DC/AC coefficient is reconstructed. Then, zero runs are expanded.
4. IQ is performed, which is simply multiplication of the coefficients with values in the quantizer matrices.

8.4.6.3.6 Memory Interfaces

The VLCDJ has four memory interfaces (all memories are inside the SIMCOP subsystem):

- Image buffer (input DCT coefficients for encoding and output DCT coefficients for decoding)
- Quantizer memory
- Huffman memory
- Bitstream memory (output for encoding and input for decoding)

8.4.6.3.6.1 Image Buffer

An image buffer stores DCT data in the context of the VLCDJ. This is an input in encode mode and an output in decode mode.

When multiple MCUs are configured, DCT coefficients for the MCUs are stored sequentially (MCU 0 is stored first, followed by MCU 1, and so on).

Blocks in an MCU are stored sequentially; that is, block 0 first, block 1 next, and so on. There are six blocks per MCU in YUV4:2:0 format, {Y0, Y1, Y2, Y3, U, V}, and four blocks per MCU in YUV4:2:2 format, {Y0, Y1, U, V}.

The 64 DCT coefficients for each block are stored in an 8 × 8 transposed format (the companion DCT module handles the transposed format). Each coefficient, up to [–2047, 2047] in range is stored on a 16-bit word. Table 8-1479 lists the data format in each 8 × 8 block of coefficients.

Table 8-1479. Image Buffer Block Format

Byte Offset								
0	1	2	3	4	5	...	14	15
c(0, 0)		c(0, 1)		c(0, 2)		...	c(0, 7)	
c(1, 0)		c(1, 1)		c(1, 2)		...	c(1, 7)	
c(2, 0)		c(2, 1)		c(2, 2)		...	c(2, 7)	

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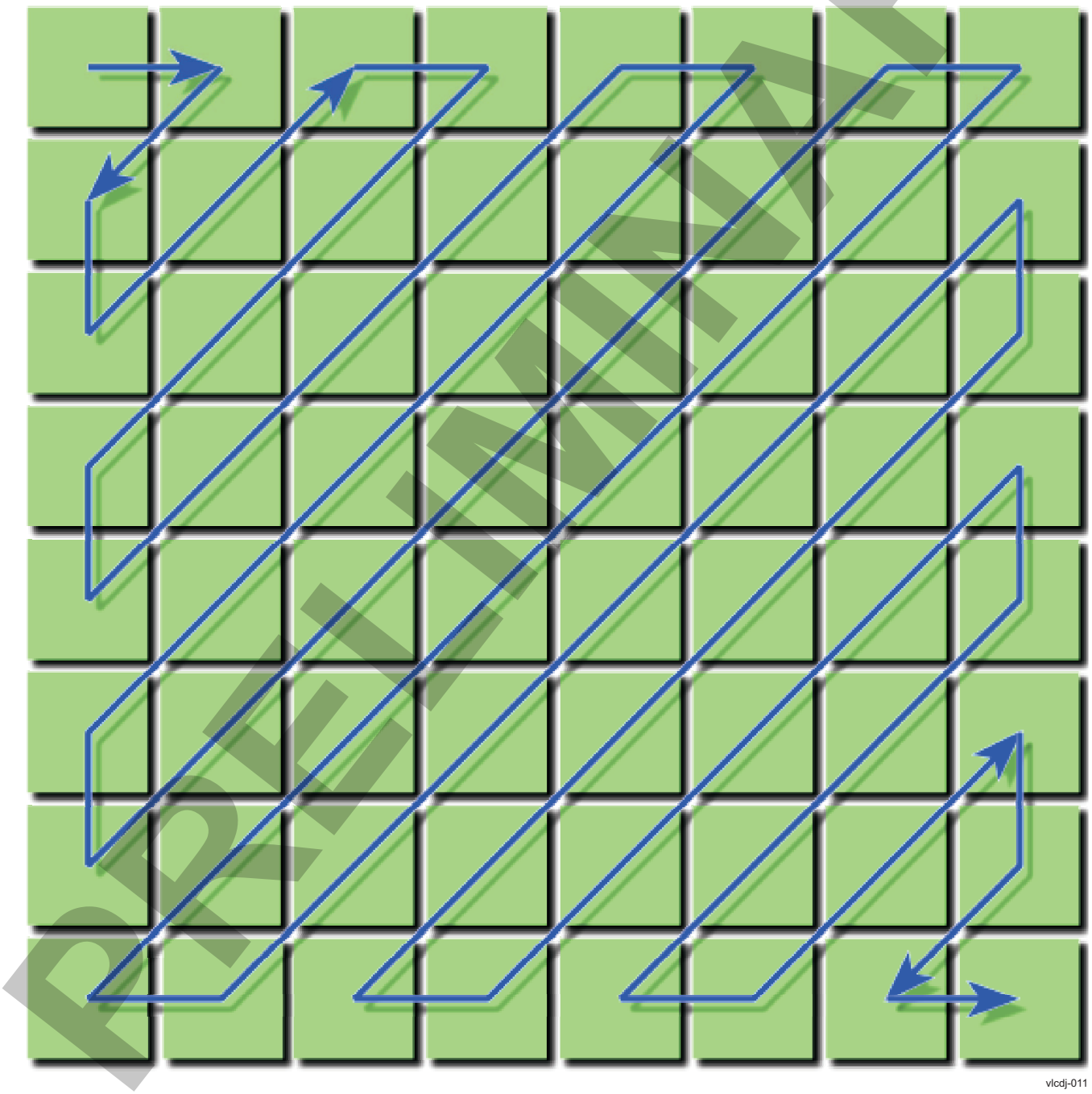
Table 8-1479. Image Buffer Block Format (continued)

Byte Offset								
0	1	2	3	4	5	...	14	15
:								
c(7, 0)		c(7, 1)		c(7, 2)		...	c(7, 7)	

The DCT coefficients are processed in zigzag order, as required by JPEG and shown in Figure 8-291.

Figure 8-291. JPEG Zigzag Order



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8.4.6.3.6.2 Quantizer Memory

The quantization memory stores the reciprocal of quantizers, 2^{15}/qmat[i][j] so that hardware performs multiplications rather than divisions. Each data point is stored in 16 bits.

The quantizer matrices have a fixed size, 64 16-bit elements each. The quantizer memory (QMEM) is sized to hold up to four matrices (for the recommended allocation for YUV4:2:0 and YUV4:2:2, see Table 8-1480).

Table 8-1480. Recommended QMEM Allocation for YUV4:2:0 and YUV4:2:2

Quadrant of QMEM	Address Offset (Bytes)	Contents
00	0x000	(Encode) Quantizer reciprocal for Y (2^{15}/qmat[i][j])
01	0x080	(Encode) Quantizer reciprocal for UV (2^{15}/qmat[i][j])
10	0x100	(Decode) Quantizer for Y (qmat[i][j])
11	0x180	(Decode) Quantizer for UV (qmat[i][j])

Each matrix is stored in zigzag order to make quantization and inverse quantization more efficient.

8.4.6.3.6.3 Huffman Memory

Huffman memories store Huffman encode tables and Huffman control/decode tables. For information about Huffman tables, see Section 8.4.6.3.7, *Huffman Table Organization*.

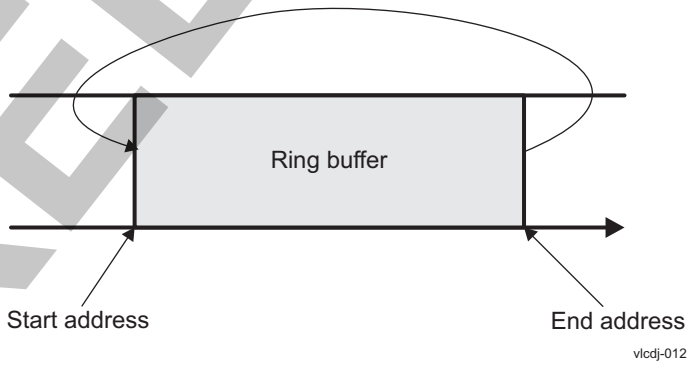
8.4.6.3.6.4 Bitstream Memory

Bitstream memory is for input/output (I/O) bitstream. Bitstream data is stored in little-endian format in the memory. Circular buffer start and end addresses are provided in registers to facilitate bitstream data management:

- VLCDJE_CBUF[11:10] START, start of ring buffer for encode mode (address must be 1 KiB aligned)
- VLCDJE_CBUF[27:26] END, end of ring buffer for encode mode (address must be 1 KiB aligned)
- VLCDJD_CBUF[11:10] START, start of ring buffer for decode mode (address must be 1 KiB aligned)
- VLCDJD_CBUF[27:26] END, end of ring buffer for decode mode (address must be 1 KiB aligned)

Figure 8-292 shows the start and end addresses of a ring buffer.

Figure 8-292. VLCDJ Ring Buffer



In encoding and decoding, a bit-level boundary defines bitstream data written (for encoding) or parsed (for decoding). To point to that boundary, bit and byte pointers are provided in the registers:

- VLCDJE_BSPTR[19:16] BITPTR (encoding)
- VLCDJE_BSPTR[11:0] BYTEPTR (encoding)
- VLCDJD_BSPTR[19:16] BITPTR (decoding)
- VLCDJD_BSPTR[11:0] BYTEPTR (decoding)

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BYTEPTR (byte pointer) points to the byte where the boundary lies, and BITPTR (bit pointer) specifies the number of available vacant data bits (for encoding) or remaining data bits (for decoding). BITPTR is always within the range from 1 to 8, where 8 indicates that an entire byte is available for writing or reading.

For example, for encoding, if BYTEPTR = 0 and BITPTR = 8, after the hardware encodes a specified number of MCUs that together generate 30 bits, or 3 full bytes and 6 bits, BYTEPTR = 3 and BITPTR = 2. The JPEG standard requires that at the end of MCU data, any remaining bits of the last byte are padded with 1s. For example, if the last byte has 4 bits written 0101, the last byte of MCU data in the JPEG data is 0x5F.

8.4.6.3.7 Huffman Table Organization

8.4.6.3.7.1 Huffman Table for Encode Mode

Because the Huffman encode tables are compact, they are fixed relative to a common pointer:

- The Luma DC table starts at VLCDJE_VLCTBL[11:2] ADDR (12 entries × 4 = 48 bytes)
- The Luma AC table starts at VLCDJE_VLCTBL[11:2] ADDR + 48 bytes (11 × 16 x 4 = 704 bytes)
- The Chroma DC table starts at VLCDJE_VLCTBL[11:2] ADDR + 752 bytes (12 entries × 4 = 48 bytes)
- The Chroma AC table starts at VLCDJE_VLCTBL[11:2] ADDR + 800 bytes (11 × 16 × 4 = 704 bytes)

For DC tables, the index of each table corresponds to the size of the absolute value of the DC coefficient.

For AC tables, the index of each table corresponds to a formula including the size (of absolute value of nonzero AC coefficients) and the zero run: Index = SIZE × 16 + run. Because the size cannot be 0, the first 16 entries hold special symbols. EOB is at entry 0, and ZRL is at entry 15.

The size of a non-negative value is the number of bits required to represent the value (for example, a size of 4..7 = 3).

Figure 8-293 shows the organization of the Huffman encode table.

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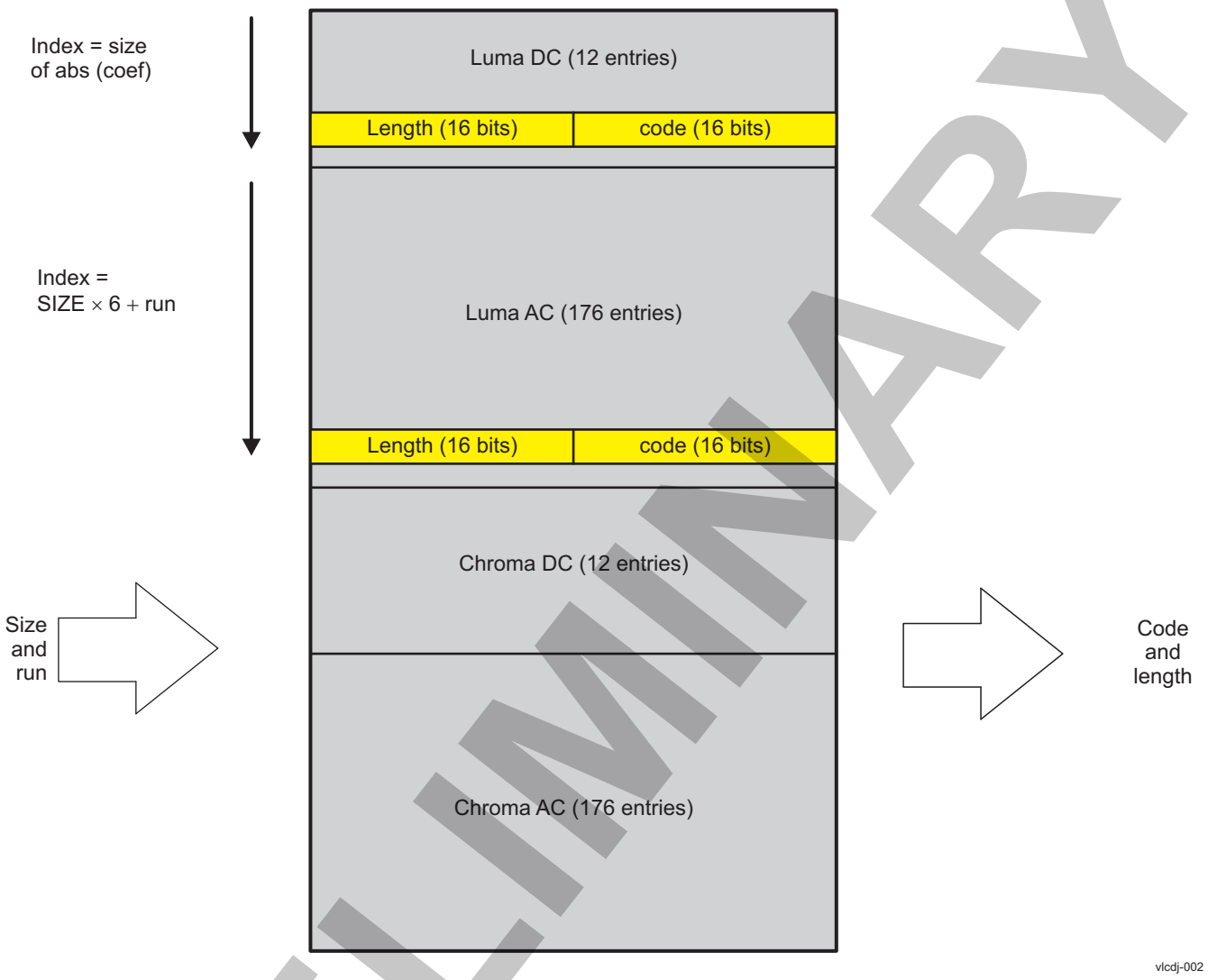
Figure 8-293. Huffman Encode Table Organization



8.4.6.3.8 Restart Marker

8.4.6.3.8.1 Restart Marker Insertion for Encode

As specified in the JPEG standard, the VLCDJ can insert a restart marker at a specified MCU interval (for information about restart markers, see Section 8.4.6.3.5, *VLDCJ in JPEG Decoding Flow*). Any remaining bits in the last partial byte are padded with 1s.

When enabled, the VLCDJ inserts a restart marker at the end of a group of MCUs. A partial byte is automatically padded with 1s.

8.4.6.3.8.2 Restart Marker Location Recording

To facilitate reordering of compressed JPEG data sections to achieve JPEG rotation, the VLCDJ also records the restart marker locations.

8.4.6.3.8.3 Restart Marker Handling for Decoding

Restart markers are handled automatically during MCU data decoding according to the JPEG standard. The DC predictors are reset at the MCU boundary where restart markers are present.

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Because the handling of restart markers is complex, there is no check of the consistency of restart marker value or existence/nonexistence with the restart interval (which is not part of the decoder register setting). Correct JPEG files are decoded correctly. Incorrect JPEG files can escape error detection.

To decode correctly, in spite of the presence of restart markers, software must configure the VLCDJ with the correct byte pointer for the VLCDJ. To reset DC predictors to occur before an MCU, the byte pointer must point to the restart marker before the MCU data in the bitstream data. In other words, the VLCDJ does not search for the correct marker and resume MCU decoding after the marker. The VLCDJ detects the presence of the marker only at the MCU boundaries.

8.4.6.3.9 Encode/Decode Context Switching

The bitstream memory is organized as two banks of memory. When the VLCDJ performs only encoding or only decoding, the two banks are used to achieve VLCDJ and DMA concurrence, and automatic bitstream data DMA is supported.

When the VLCDJ performs one encode and one decode concurrently, both contexts can coexist in the configuration registers, because encode and decode configurations are in separate registers. The bitstream memory must be partitioned half-and-half between encode and decode. For example:

- VLCDJE_CBUF[11:10] START = 0x0
- VLCDJE_CBUF[27:26] END = 0x7FF
- VLCDJD_CBUF[11:10] START = 0x800
- VLCDJD_CBUF[27:26] END = 0xFFF

The byte pointers and the bitstream data DMA must be set up accordingly.

When the VLCDJ is encoding, the decode half of bitstream memory can be refilled by DMA. When the VLCDJ is decoding, the encode half of bitstream memory can be transferred out by DMA. Hardware does not support automatic triggering of DMA; software must submit DMA based on the byte pointer value of each context. For good SDRAM efficiency, the DMA block must be aligned correctly.

8.4.6.3.10 Using Sequential Block Mode for YUV4:4:4 Encoding/Decoding

In sequential block mode, because it deals with only one color component, the VLCDJ does the following:

- Uses DCPREDY for the DC predictor
- Uses the first quantizer matrix pointed by QM/QMR
- Starts from the first block pointed to by DCT
- Uses the first VLC/VLD table

Thus, to encode/decode YUV4:4:4 format using sequential block mode, software must switch context among Y, U, and V between initiations of the VLCDJ. Memory organization and registers are designed so that QM/QMR, DCT, and VLC/VLD tables can be swapped by changing the corresponding pointers in the registers. The DC predictor must be saved and restored.

For more information, see Section 8.4.6.4.6, *Example of YUV4:4:4 Encoding*.

8.4.6.3.11 Error Reporting

The VLCDJ can report the following decode errors:

- Invalid Huffman code
- Block exceeding 64 coefficients

NOTE: Decoding of an 0xFF byte followed by a nonzero byte is not reported as an error (for more information, see Section 8.4.6.3.5, *VLCDJ in JPEG Decoding Flow*).

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When there is a decode error, VLCDJ operation is suspended immediately. Bit and byte pointers to the bitstream near where the error occurs are reflected in the VLCDJD_BSPTR[19:16] BITPTR and VLCDJD_BSPTR[11:0] BYTEPTR bit fields. The DCT coefficient index, in zigzag order of the task, near where the error occurs, is also reflected in a read-only bit field, VLCDJD_DCTERR[13:0] ERRPTR. For example, if decoding fails at the fifth coefficient of the third block of the VLCDJ task (which can be multiple MCUs), ERRPTR returns 2 × 64 + 4 = 195.

The IQ stage of the hardware does not stop and runs to completion. When there is a decode error, the DC predictor and decoded DCT coefficient outcomes are indeterminate.

Because the VLCDJ does not start in the middle of an MCU, software must recover from the error and configure the VLCDJ from an MCU boundary.

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8.4.6.4 ISS SIMCOP VLCDJ Basic Programming Model

8.4.6.4.1 Initialization of Surrounding Modules

To initialize the VLCDJ, surrounding modules must be initialized. Table 8-1481 lists these modules.

Table 8-1481. Initialization of Surrounding Modules

Module	Minimum Required Setting	Optional Settings
CLKC	Enable the SIMCOP clock.	
Buffers	Configure VLCDJ access to the image buffer.	
SIMCOP CTRL		Configure SIMCOP CTRL to handle VLCDJ interrupts.

8.4.6.4.2 ISS SIMCOP VLCDJ Start and Register Modification During Processing

The module operation can be started with two mechanisms, depending on the status of the VLCDJ_CTRL[2] TRIG_SRC bit.

When the VLCDJ_CTRL[2] TRIG_SRC bit is set to 0 and the module is idle (the VLCDJ_CTRL[16] BUSY bit is set to 0), the module is started by setting the VLCDJ_CTRL[0] EN bit to 1. Any hardware start pulses are ignored. To simplify software control, in the same register write, changing the VLCDJ_CTRL[2] TRIG_SRC bit from 1 to 0 and setting the VLCDJ_CTRL[0] EN bit to 1 is recognized as a valid starting condition.

When the VLCDJ_CTRL[2] TRIG_SRC bit is set to 1, and the module is idle (the VLCDJ_CTRL[16] BUSY bit is set to 0), the module is started by the START_PULSE signal going active. Any software write to the VLCDJ_CTRL[0] EN bit is ignored.

During encoding, encode configuration registers must not be modified by software, while decode configuration registers can be freely modified.

During decoding, decode configuration registers must not be modified by software, while encode configuration registers can be freely modified.

8.4.6.4.3 JPEG Encoding

For JPEG encoding of a YUV4:2:0 image, eight MCUs per task, software first composes the JPEG header, which includes image dimension, YUV4:2:0 format, Huffman tables, quantizer matrices, and the start-of-scan marker and scan header, all before the MCU data. Software then sets up the encoding task, once per image, with the procedure listed in Table 8-1482.

Table 8-1482. JPEG Encoding Procedure

Step	Register/Bit Field	Value
Configure the encode configuration register.	VLCDJE_CFG[1:0] FMT	0 (YUV4:2:0 mode)
	VLCDJE_CFG[13:8] NMCUS	7 (eight MCUs)
	VLCDJE_CFG[2] RSTEN	0 (no restart marker)
Configure the DC predictor.	VLCDJE_DCPREDY[11:0] PREDY	0 (reset DC predictor for Y)
	VLCDJE_DCPREDUV[11:0] PREDU	0 (reset DC predictors for U)
	VLCDJE_DCPREDUV[27:16] PREDV	0 (reset DC predictors for V)
Configure the input and output memories.	VLCDJE_BSPTR[11:0] BYTEPTR	0 (beginning of bitstream memory)
	VLCDJE_BSPTR[19:16] BITPTR	8 (initially empty byte, thus 8 free bits)
	VLCDJE_CBUF[11:10] START	0 (bitstream starts from beginning of first quadrant of bitstream memory)
	VLCDJE_CBUF[27:26] END	3 (bitstream ends at end of fourth quadrant of bitstream memory)
	VLCDJE_DCTQM[13:4] DCT	0 (DCT coefficients at beginning of image buffer)

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Table 8-1482. JPEG Encoding Procedure (continued)

Step	Register/Bit Field	Value
Configure Huffman and quantizer memory pointers.	VLCDJE_DCTQM[24:23] QMR	0 (quantizer matrix reciprocal at beginning of QMEM)
	VLCDJE_VLCTBL[11:2] ADDR	0 (VLC table at beginning of HUFMEM)
Start encode with automatic ring buffer management.	VLCDJ_CTRL[1] MODE	0 (encode mode)
	VLCDJ_CTRL[0] EN	1 (start VLCDJ operation)

For each group of eight MCUs (the VLCDJ does not care if these MCUs cross multiple MCU rows), software sets the VLCDJ_CTRL[0] EN bit to 1 (restart VLCDJ operation).

Alternately, the hardware sequencer can start the VLCDJ. Usually, DMA is also configured to bring in YUV4:2:0 image data as input to DCT, and DMA, DCT, and VLCDJ are all put under control of the hardware sequencer.

Bitstream data is managed automatically between the VLCDJ and DMA throughout JPEG encoding of MCUs.

NOTE: Many registers change during the encoding of a frame, but software is not required to access these registers, because the VLCDJ manages the status information between tasks.

The last hardware task may require a smaller number of MCUs (the VLCDJE_CFG[13:8] NMCUS bit field) to adjust for the number of MCUs in the last group.

After the last VLCDJ task for the image, software must disable the automatic bitstream buffer management and prepare for the next image by setting the following values (these can be issued as a single write):

- VLCDJ_CTRL[6] RBEN = 0 (disable automatic DMA interaction)
- VLCDJ_CTRL[7] CLRRB = 1

Finally, software must pad the last data byte with bit 1s, then place an end-of-image marker after the last data byte. The VLCDJE_BSPTR[11:0] BYTEPTR and VLCDJE_BSPTR[19:16] BITPTR bit fields indicate the locations of the last data byte and bit, respectively. Software must then set up DMA to transfer out the remaining data in bitstream memory.

The number of MCUs processed by hardware per task must be set according to image buffer allocation. For example, with 8 KiB available for DCT coefficient memory, and YUV4:2:0 format, it is possible to process 8K/(16 × 16× 1.5 × 2) = 10 MCUs. Because the bitstream DMA is automatic, bitstream data does not overflow bitstream memory for this many MCUs in densely coded JPEG.

8.4.6.4.4 JPEG Decoding

For JPEG decoding of an image, software first parses the JPEG header, which includes image dimension, YUV sampling, Huffman tables, quantizer matrices, and start-of-scan marker and scan header, before the MCU data. Software then sets up DMA to load bitstream data into the first half of bitstream memory.

The Huffman tables must be processed to generate hardware control tables and decode tables for a particular JPEG file, unless the Huffman tables match previously processed tables for which the hardware control and decode tables are known. The hardware control and decode tables must be transferred to HUFMEM.

If the JPEG file is YUV4:2:0, and image buffer memory is sufficient to process eight MCUs per hardware task, software must set up the decode task, once per image, with the procedure listed in Table 8-1483.

Table 8-1483. JPEG Decoding Procedure

Step	Register/Bit Field	Value
Configure the decode configuration register.	VLCDJD_CFG[1:0] FMT	0 (YUV4:2:0 mode)

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Table 8-1483. JPEG Decoding Procedure (continued)

Step	Register/Bit Field	Value
	VLCDJD_CFG[13:8] NMCUS	7 (eight MCUs)
	VLCDJD_CFG[2] RSTEN	0 (no restart marker)
Configure the DC predictor.	VLCDJD_DCPREDY[11:0] PREDY	0 (reset DC predictor for Y)
	VLCDJD_DCPREDUV[11:0] PREDU	0 (reset DC predictors for U)
	VLCDJD_DCPREDUV[27:16] PREDV	0 (reset DC predictors for V)
Configure the input and output memories.	VLCDJD_BSPTR[11:0] BYTEPTR	0 (beginning of bitstream memory)
	VLCDJD_BSPTR[19:16] BITPTR	8 (initially empty byte, thus 8 free bits)
	VLCDJD_CBUF[11:10] START	0 (bitstream starts from beginning of first quadrant of bitstream memory)
	VLCDJD_CBUF[27:26] END	3 (bitstream ends at end of fourth quadrant of bitstream memory)
	VLCDJD_DCTQM[13:4] DCT	0 (DCT coefficients at the beginning of the image buffer)
Configure Huffman and quantizer memory pointers.	VLCDJD_DCTQM[24:23] QM	0 (quantizer matrix at beginning of QMEM)
	VLCDJD_CTRLTBL[11:2] ADDR	0 (typically, control table is placed at the beginning of HUFMEM)
	VLCDJD_DCDTBL01[11:2] TBL0	30 (typically, the first decode table follows the control table, 60 shorts = 120 bytes = 30 words)
	VLCDJD_DCDTBL01[27:18] TBL1	? (where the second decode table starts)
	VLCDJD_DCDTBL23[11:2] TBL2	? (where the third decode table starts)
	VLCDJD_DCDTBL23[27:18] TBL3	? (where the fourth decode table starts)
Start decode with automatic ring buffer management.	VLCDJ_CTRL[1] MODE	1 (decode mode)
	VLCDJ_CTRL[0] EN	1 (start VLCDJ operation)

For each group of eight MCUs (the VLCDJ does not care if these MCUs cross multiple MCU rows), software sets the VLCDJ_CTRL[0] EN bit to 1 (start VLCDJ operation).

Alternately, the hardware sequencer can start the VLCDJ, as well as control buffer switches and coordinate among the VLCDJ, DCT, and DMA.

Bitstream data is managed automatically between the VLCDJ and DMA throughout JPEG encoding of MCUs.

NOTE: Many registers change during the decoding of a frame, but software is not required to access these registers, because the VLCDJ manages the status information between tasks.

The last hardware task may require a smaller number of MCUs (the VLCDJD_CFG[13:8] NMCUS bit field) to adjust for the number of MCUs in the last group.

After the last VLCDJ task for the image, software must disable the automatic bitstream buffer management and prepare for the next image by setting the following values (these can be issued as a single write):

- VLCDJ_CTRL[6] RBEN = 0 (disable automatic DMA interaction)
- VLCDJ_CTRL[7] CLRRB = 1

Any remaining bitstream data in bitstream memory afterward is harmless, because before the VLCDJ processes the next image decode, new bitstream data must be brought in, thereby overwriting the old data, and bit/byte pointers must be reset to the beginning of bitstream memory.

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The number of MCUs processed by hardware per task must be set according to image buffer allocation. For example, with 16 KiB available for DCT coefficient memory, and YUV4:2:0 format, it is possible to process 16K/(16 × 16 × 1.5 × 2) = 21 MCUs. Because the bitstream DMA is automatic, there is no bitstream data underrun for this many MCUs.

8.4.6.4.5 Concurrent JPEG Encoding and Decoding

For concurrent decoding and encoding, the two operations are configured separately but similarly.

Half of bitstream memory is used for encoding (for example, the first half), and the rest is used for decoding. Automatic bitstream DMA does not work in this case, so the number of MCUs must accommodate the worst-case bitstream size per MCU.

Theoretically, the worst case is 16 bits of Huffman code + 12 additional bits per coefficient, or 28 bits per coefficient. With natural images, there are typically about 8 bits per pixel when quantizers are minimal (that is, all 1s). With 16 bits per coefficient, or 768 bytes per MCU in YUV4:2:0 (this is 24 bits per pixel and three times the typical worst case), half of bitstream memory is 2 KiB, which can safely hold two MCUs.

In this case, half of QMEM is used for encoding and half is used for decoding. Encode and decode Huffman tables are placed so that they coexist in HUFFMEM.

The Huffman tables for encoding, decoding, and quantizer matrices must be placed accordingly in HUFMEM and QMEM. Bitstream data is filled at the second half of bitstream memory for decoding.

Register fields are configured as listed in Table 8-1484.

Table 8-1484. Concurrent JPEG Encoding and Decoding

Step	Register/Bit Field	Value
Configure the encode register.	VLCDJE_CFG[1:0] FMT	0 (YUV4:2:0 mode)
	VLCDJE_CFG[13:8] NMCUS	1 (two MCUs)
	VLCDJD_CFG[2] RSTEN	0 (no restart marker)
	VLCDJE_DCPREDY[11:0] PREDY	0 (reset DC predictor for Y)
	VLCDJE_DCPREDUV[11:0] PREDU	0 (reset DC predictors for U)
	VLCDJE_DCPREDUV[27:16] PREDV	0 (reset DC predictors for V)
	VLCDJE_BSPTR[19:16] BITPTR	8 (initially empty byte, thus 8 free bits)
	VLCDJE_DCTQM[13:4] DCT	0 (DCT coefficients at beginning of image buffer)
Configure the decode register.	VLCDJD_CFG[1:0] FMT	0 (YUV4:2:0 mode)
	VLCDJD_CFG[13:8] NMCUS	1 (two MCUs)
	VLCDJD_CFG[2] RSTEN	0 (no restart marker)
	VLCDJD_DCPREDY[11:0] PREDY	0 (reset DC predictor for Y)
	VLCDJD_DCPREDUV[11:0] PREDU	0 (reset DC predictors for U)
	VLCDJD_DCPREDUV[27:16] PREDV	0 (reset DC predictors for V)
	VLCDJD_BSPTR[19:16] BITPTR	8 (initially empty byte, thus 8 free bits)
	VLCDJD_DCTQM[13:4] DCT	0 (DCT coefficients at the beginning of the image buffer)
Configure the byte pointer to bitstream memory.	VLCDJE_BSPTR[11:0] BYTEPTR	0 (beginning of bitstream memory)
	VLCDJD_BSPTR[11:0] BYTEPTR	0x800 (beginning of bitstream memory second half)
Configure the bitstream memory partition.	VLCDJE_CBUF[11:10] START	0 (bitstream starts at beginning of first quadrant of bitstream memory)
	VLCDJE_CBUF[27:26] END	1 (bitstream ends at end of second quadrant of bitstream memory)
	VLCDJD_CBUF[11:10] START	2 (bitstream starts at beginning of third quadrant of bitstream memory)
	VLCDJD_CBUF[27:26] END	3 (bitstream ends at end of fourth quadrant of bitstream memory)

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Table 8-1484. Concurrent JPEG Encoding and Decoding (continued)

Step	Register/Bit Field	Value
Configure the quantizer matrix pointer.	VLCDJE_DCTQM[24:23] QMR	0 (quantizer matrix at beginning of QMEM)
	VLCDJD_DCTQM[24:23] QMR	2 (quantizer matrix at second half of QMEM)
Configure Huffman tables.	VLCDJE_VLCTBL[11:2] ADDR	0 (VLC table at beginning of HUFMEM)
	VLCDJD_CTRLTBL[11:2] ADDR	376 (after VLC table, 2 × (24 + 352) shorts = 376 words)
	VLCDJD_DCDTBL01[11:2] TBL0	406 (after control table of 30 words)
	VLCDJD_DCDTBL01[27:18] TBL1	? (where the second decode table starts)
	VLCDJD_DCDTBL23[11:2] TBL2	? (where the third decode table starts)
	VLCDJD_DCDTBL23[27:18] TBL3	? (where the fourth decode table starts)

Software sets the following values to start encoding:

- VLCDJ_CTRL[1] MODE = 0 (encode mode)
- VLCDJ_CTRL[0] EN = 1 (start VLCDJ operation)

When the VLCDJ completion interrupt is detected by software, encoding is complete and software must service the encoded bitstream data in the first half of bitstream memory, letting hardware access the second half of the bitstream for decoding. Software sets up bitstream writes to transfer the encoded bitstream from bitstream memory[0] to bitstream memory[128 × (VLCDJE_BSPTR[11:0] BYTEPTR/128)] (rounding down to 128-byte alignment improves SDRAM efficiency). Software must identify the bitstream data already transferred out, for the next round of servicing encoded bitstream data. Software must also service to-encode input data to the DCT.

After kicking off encode DMAs, without waiting for DMA completion, software must set the following values to start VLCDJ decoding in parallel with the DMA:

- VLCDJ_CTRL[1] MODE = 1 (decode mode)
- VLCDJ_CTRL[0] EN = 1 (start VLCDJ operation)

When the VLCDJ completion interrupt is detected by software, decoding is complete and software must service the decoded bitstream data in the second half of bitstream memory, letting hardware access the first half of the bitstream for encoding. Software sets up bitstream writes to transfer the bitstream to be decoded from bitstream memory[0] to bitstream memory[128 × (VLCDJD_BSPTR[11:0] BYTEPTR/128)] (rounding down to 128-byte alignment improves SDRAM efficiency). Software must identify the bitstream data already transferred in, for the next round of servicing bitstream data to be decoded. Software must also service decoded image data in the output image buffer of the DCT.

After kicking off decode DMAs, without waiting for DMA completion, software must start VLCDJ encoding in parallel with the DMA.

Software must continue to alternate between encoding and decoding until the image completes.

Figure 8-294 shows the concurrence schedule for JPEG encoding and decoding.

Figure 8-294. Concurrence Schedule for JPEG Encoding and Decoding

DMA	E[0]		E[1]		E[2]		E[3]					
in			D[0]		D[1]		D[2]		D[3]			
DCT		E[0]		E[1]	D[0]	E[2]	D[1]	E[3]	D[2]		D[3]	
VLCD			E[0]	D[0]	E[1]	D[1]	E[2]	D[2]	E[3]	D[3]		
DMA				E[0]		E[1]		E[2]		E[3]		
out						D[0]		D[1]		D[2]		D[3]

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Management of bitstream I/O and image I/O is heavy in intervals of only two MCUs. It is better to run only encoding for many MCUs, switch context, and then run decoding for many MCUs.

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When running JPEG transcoding, decoding a picture and re-encoding it, to adjust quantizers and/or remove/insert restart markers, it can be more efficient to run encode and decode concurrently in VLCDJ, skipping DCT and image I/O DMA altogether. In this case, software handles only bitstream data I/O, which is more manageable.

Figure 8-295 shows the concurrence schedule.

Figure 8-295. Concurrence Schedule for JPEG Transcoding

DMA in	D[0]		D[1]		D[2]		D[3]			
VLCD		D[0]	E[0]	D[1]	E[1]	D[2]	E[2]	D[3]	E[3]	
DMA out				E[0]		E[1]		E[2]		E[3]

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8.4.6.4.5.1 DMA and Buffer Manual Management

When the VLCDJ performs one encode and one decode concurrently, both contexts can coexist in the configuration registers, because encode and decode configurations are in separate registers. The bitstream memory must be partitioned half-and-half between encode and decode:

- VLCDJE_CBUF[11:10] START = 0 (0x0)
- VLCDJE_CBUF[27:26] END = 1 (0x7FF)
- VLCDJD_CBUF[11:10] START = 2 (0x800)
- VLCDJD_CBUF[27:26] END = 3 (0xFFF)

The byte pointers and the bitstream data DMA must be set up accordingly.

When the VLCDJ is encoding, the decode half of the bitstream memory can be refilled by DMA. When the VLCDJ is decoding, the encode half of the bitstream memory can be transferred out by DMA. Hardware does not support automatic triggering of DMA; software must submit DMA based on the byte pointer value of each context. For greater SDRAM efficiency, the DMA block must be aligned correctly. For example, the pseudo code that sets up the DMA for an encode task may appear as:

```
new_dma_ptr = VLCDJ_BSPTR.BYTEPTR & ~0x3F; // align to 64-byte

if (new_dma_ptr > saved_dma_ptr)
{
 setup_dma(saved_dma_ptr, new_dma_ptr - saved_dma_ptr);
 // start DMA at saved_dma_ptr, length = new_dma_ptr - saved_dma_ptr
}
else // wraps around, need to DMA 2 blocks
{
 setup_dma(saved_dma_ptr, 0x800 - saved_dma_ptr);
 setup_dma(saved_dma_ptr, new_dma_ptr);
}

saved_dma_ptr = new_dma_ptr;
```

This DMA setup can be carried out concurrently with VLCDJ operation; thus, this code is executed with each encode or decode task. When the VLCDJ is encoding, software can access the decode bit/byte points to set up DMA for decoding, and vice versa.

Because hardware stalling does not work in this case, the number of MCUs must be configured so that in the worst case there is no bitstream data overrun or underrun.

The bitstream buffer can be allocated at a quarter of bitstream memory granularity, or 1 KiB. This allows at most four separate buffers to coexist in bitstream memory.

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If multiple encode and/or decode threads are performed concurrently, software must save and restore the appropriate configuration registers. The register map has common registers in one group, encode registers in another group, and decode registers in a third group. Bitstream memory partitioning and corresponding DMA submission are left to software.

8.4.6.4.6 Example of YUV4:4:4 Encoding

The following pseudo code shows the general sequence involved in YUV4:4:4 encoding. Decoding can be similarly derived.

```
encode_yuv444()
{
 VLCDJ_CTRL[1] MODE = 0; /* encode */
 VLCDJE_CFG[1:0] FMT = 2; /* sequential block mode */
 VLCDJE_CFG[13:8] NMCUS = 0; /* 1 block at a time */
 pred_y = 0;
 pred_u = 0;
 pred_v = 0;

 for (i=0; i<num_mcus; i++)
 {
 VLCDJE_DCPREDY = pred_y; /* restore Y context */
 VLCDJE_DCT = DCT_Y;
 VLCDJE_QMR = QMR_Y;
 VLCDJE_VLCTBL = VLC_Y;

 VLCDJ_CTRL[0] EN = 1; /* kick off VLCDJ for Y */

 pred_y = VLCDJE_DCPREDY; /* save Y context */
 VLCDJE_DCPREDY = pred_u; /* restore U context */
 VLCDJE_DCT = DCT_U;
 VLCDJE_QMR = QMR_UV;
 VLCDJE_VLCTBL = VLC_UV;

 VLCDJ_CTRL[0] EN = 1; /* kick off VLCDJ for U */

 pred_u = VLCDJE_DCPREDY; /* save U context */
 VLCDJE_DCPREDY = pred_v; /* restore V context */
 VLCDJE_DCT = DCT_V;

 VLCDJ_CTRL[0] EN = 1; /* kick off VLCDJ for V */

 pred_v = VLCDJE_DCPREDY; /* save V context */
 }
}
```

8.4.6.4.7 Example of Huffman Encode and Decode Tables

8.4.6.4.7.1 Huffman Encode Table

Sample JPEG Luma DC encode table:

```
unsigned short jpeg_dc_y[24] =
{
 0x0000,0x0002,0x0002,0x0003,0x0003,0x0003,0x0004,0x0003,
 0x0005,0x0003,0x0006,0x0003,0x000e,0x0004,0x001e,0x0005,
 0x003e,0x0006,0x007e,0x0007,0x00fe,0x0008,0x01fe,0x0009
};
```

Table 8-1485 corresponds to Table 17 in the JPEG standard *ISO/IEC JTC1/SC29/WG10 Standard 10918-1 (JPEG), Information Technology – Digital Compression and Coding of Continuous-Tone Still Images – Requirements and Guidelines.*

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Table 8-1485. Sample Luma DC Huffman Code Table

Category	Code Length	Code Word
0	2	00
1	3	010
2	3	011
3	3	100
4	3	101
5	3	110
6	4	1110
7	5	11110
8	6	111110
9	7	1111110
10	8	11111110
11	9	111111110

For example if we want to code a DC coefficient value of –5:

Use abs(–5) = 5 to select a size of 3. Look up the encode table to find:

- jpeg_dc_y[2 × 3] = 4 (code)
- jpeg_dc_y[2 × 3 + 1] = 3 (length)

Thus, the VLCDJ adds 100 to the bitstream as the Huffman code of the size.

The additional bits for negative coefficients are ones complement of the absolute value, so for –5, this is 010, or 2. After the Huffman code of the size, the VLCDJ adds 010 to the bitstream.

The AC coefficient table is the same, except that the VLCDJ uses 16 × size + run to index the encode table.

8.4.6.4.7.2 Huffman Decode Tables

Sample JPEG Luma DC control and decode tables:

```
unsigned short jpeg_dc_y_ctl_tbl[13]=
{
 0x0000,0x0000,0x0000,0x0000,0x1800,0x2001,0x2802,0x3003,
 0x3804,0x4005,0x4806,0x4806,0x4806
};

unsigned short jpeg_dc_y_dcd_tbl[14]=
{
 0x0000,0x480b,0x400a,0x3809,0x3008,0x2807,0x2006,0x1805,
 0x1804,0x1803,0x1802,0x1801,0x1000,0x1000
};
```

These tables contain the same information as Table 8-1485, which complies with the JPEG standard.

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8.4.6.5 ISS SIMCOP VLCDJ Register Manual

8.4.6.5.1 ISS SIMCOP VLCDJ Instance Summary

Table 8-1486 summarizes the VLDCJ instance.

Table 8-1486. VLCDJ Instance Summary

Module Name	L3_MAIN Base Address	IPU Base Address	Size
VLCDJ	0x5202 0600	0x5506 0600	128 bytes

8.4.6.5.2 ISS SIMCOP VLCDJ Registers

8.4.6.5.2.1 ISS SIMCOP VLCDJ Register Summary

Table 8-1487 summarizes VLDCJ register mapping.

Table 8-1487. VLCDJ Register Mapping Summary

Register	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address	IPU Physical Address
VLCDJ_REVISION	RW	32	0x0000 0000	0x5202 0600	0x5506 0600
VLCDJ_CTRL	RW	32	0x0000 0004	0x5202 0604	0x5506 0604
VLCDJE_CFG	RW	32	0x0000 0008	0x5202 0608	0x5506 0608
VLCDJE_DCPREDY	RW	32	0x0000 000C	0x5202 060C	0x5506 060C
VLCDJE_DCPREDUV	RW	32	0x0000 0010	0x5202 0610	0x5506 0610
VLCDJE_BSPTR	RW	32	0x0000 0014	0x5202 0614	0x5506 0614
VLCDJE_CBUF	RW	32	0x0000 0018	0x5202 0618	0x5506 0618
VLCDJE_RSTCFG	RW	32	0x0000 001C	0x5202 061C	0x5506 061C
VLCDJE_DCTQM	RW	32	0x0000 0020	0x5202 0620	0x5506 0620
VLCDJE_VLCTBL	RW	32	0x0000 0024	0x5202 0624	0x5506 0624
VLCDJE_RSTPTR	RW	32	0x0000 0028	0x5202 0628	0x5506 0628
VLCDJE_RSTOFST	RW	32	0x0000 002C	0x5202 062C	0x5506 062C
VLCDJD_CFG	RW	32	0x0000 0040	0x5202 0640	0x5506 0640
VLCDJD_DCPREDY	RW	32	0x0000 0044	0x5202 0644	0x5506 0644
VLCDJD_DCPREDUV	RW	32	0x0000 0048	0x5202 0648	0x5506 0648
VLCDJD_BSPTR	RW	32	0x0000 004C	0x5202 064C	0x5506 064C
VLCDJD_CBUF	RW	32	0x0000 0050	0x5202 0650	0x5506 0650
VLCDJD_DCTQM	RW	32	0x0000 0054	0x5202 0654	0x5506 0654
VLCDJD_CTRLTBL	RW	32	0x0000 0058	0x5202 0658	0x5506 0658
VLCDJD_DCDTBL01	RW	32	0x0000 005C	0x5202 065C	0x5506 065C
VLCDJD_DCDTBL23	RW	32	0x0000 0060	0x5202 0660	0x5506 0660
VLCDJD_DCTERR	R	32	0x0000 0064	0x5202 0664	0x5506 0664

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8.4.6.5.2.2 ISS SIMCOP VLCDJ Register Description

through describe the individual registers.

Table 8-1488. VLCDJ_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5202 0600 0x5506 0600	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	IP Revision		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 8-1489. Register Call Summary for Register VLCDJ_REVISION

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- ISS SIMCOP VLCDJ Register Summary: [0]

Table 8-1490. VLCDJ_CTRL

Address Offset	0x0000 0004		
Physical Address	0x5202 0604 0x5506 0604	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Controls common to encoding and decoding		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															BUSY	RESERVED								CLRRB	RBEN	INTEN_ERR	INTEN_DONE	AUTOGATING	TRIG_SRC	MODE	EN

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Read returns 0.	R	0x00
16	BUSY	Idle/busy status 0: Idle 1: Busy	R	0
15:8	RESERVED	Read returns 0.	R	0x00
7	CLRRB	Write only; read returns 0.	W	0
6	RBEN	Enable RB signaling.	RW	0
5	INTEN_ERR	Interrupt enable for decode error 0: No interrupt generated on decode error 1: Interrupt generated on decode error	RW	0
4	INTEN_DONE	Interrupt enable for task completion. DONE_VLCD is not gated by this and is always asserted at task completion. 0: No interrupt generated on task completion 1: Interrupt generated on task completion	RW	0

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Bits	Field Name	Description	Type	Reset
3	AUTOGATING	Internal clock gating on OCP clock and functional clock 0: Clocks are free-running. 1: Clocks are gated off in sub-blocks that are not required for operation.	RW	1
2	TRIG_SRC	Which mechanism starts VLCDJ operation 0: MMR write to VLCDJ_CTRL.EN 1: Hardware start signal	RW	0
1	MODE	0: Encode 1: Decode	RW	0
0	EN	Module enable by software (write-only, read returns 0). When TRIG_SRC = 0 and BUSY = 0, set this field to 1 to start VLCDJ. When TRIG_SRC = 1, writes to this field are ignored. Setting TRIG_SRC = 0 and EN = 1 on the same register write is recognized.	W	0

Table 8-1491. Register Call Summary for Register VLCDJ_CTRL

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- ISS SIMCOP VLCDJ Power Management: [0]
- ISS SIMCOP VLCDJ Interrupt Requests: [1] [2]
- ISS SIMCOP VLCDJ Start and Register Modification During Processing: [6] [7] [8] [9] [10] [11] [12] [13] [14]
- JPEG Encoding: [15] [17] [18] [21] [22]
- JPEG Decoding: [23] [25] [26] [29] [30]
- Concurrent JPEG Encoding and Decoding: [32] [33] [34] [35]
- DMA and Buffer Manual Management:
- ISS SIMCOP VLCDJ Register Summary: [37]
- ISS SIMCOP VLCDJ Register Description: [38]

Table 8-1492. VLCDJE_CFG

Address Offset	0x0000 0008		
Physical Address	0x5202 0608 0x5506 0608	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Encode configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NMCUS								RESERVED				RLOCEN	RSTEN	FMT	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:8	NMCUS	Number of MCUs (FMT = 0, 1) or blocks (FMT = 2) to encode 0: 1 MCU 1: 2 MCUs, etc.	RW	0x00
7:4	RESERVED	Read returns 0.	R	0x0
3	RLOCEN	Restart marker location recording enable 0: Restart marker location recording disabled 1: Restart marker location recording enabled	RW	0
2	RSTEN	Restart marker insertion enable 0: Restart marker insertion disabled 1: Restart marker insertion enabled	RW	0
1:0	FMT	0: YUV4:2:0 1: YUV4:2:2 2 : Sequential blocks	RW	0x0

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Table 8-1493. Register Call Summary for Register VLCDJE_CFG

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Restart Marker Location Recording:
- JPEG Encoding: [1] [2] [3] [4]
- Concurrent JPEG Encoding and Decoding: [5] [6]
- ISS SIMCOP VLCDJ Register Summary: [9]

Table 8-1494. VLCDJE_DCPREDY

Address Offset	0x0000 000C		
Physical Address	0x5202 060C 0x5506 060C	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Encode DC predictor for Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				PREDY											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:0	PREDY	DC predictor for Y	RW	0x000

Table 8-1495. Register Call Summary for Register VLCDJE_DCPREDY

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Encoding: [0]
- Concurrent JPEG Encoding and Decoding: [1]
- ISS SIMCOP VLCDJ Register Summary: [2]

Table 8-1496. VLCDJE_DCPREDUV

Address Offset	0x0000 0010		
Physical Address	0x5202 0610 0x5506 0610	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Encode DC predictor for U and V		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PREDV												RESERVED				PREDU											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:16	PREDV	DC predictor for V	RW	0x000
15:12	RESERVED	Read returns 0.	R	0x0
11:0	PREDU	DC predictor for U	RW	0x000

Table 8-1497. Register Call Summary for Register VLCDJE_DCPREDUV

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Encoding: [0] [1]
- Concurrent JPEG Encoding and Decoding: [2] [3]
- ISS SIMCOP VLCDJ Register Summary: [4]

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Table 8-1498. VLCDJE_BSPTR

Address Offset	0x0000 0014		
Physical Address	0x5202 0614 0x5506 0614	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Encode bitstream pointer		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												BITPTR				RESERVED				BYTEPTR											

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19:16	BITPTR	Bit pointer, 1..8, indicates number of available bits	RW	0x8
15:12	RESERVED	Read returns 0.	R	0x0
11:0	BYTEPTR	Byte pointer (to BSMEM)	RW	0x000

Table 8-1499. Register Call Summary for Register VLCDJE_BSPTR

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Bitstream Memory: [0] [1]
- JPEG Encoding: [2] [3] [4] [5]
- Concurrent JPEG Encoding and Decoding: [6] [7] [8]
- ISS SIMCOP VLCDJ Register Summary: [9]

Table 8-1500. VLCDJE_CBUF

Address Offset	0x0000 0018		
Physical Address	0x5202 0618 0x5506 0618	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Encode bitstream circular buffer		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				END		RESERVED										RESERVED				START		RESERVED									

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:26	END	Ending quarter (1 KiB each unit) of bitstream buffer. Software can write a byte address into the upper 16 bits of the register.	RW	0x3
25:16	RESERVED	Read returns 0x3FF.	R; returns 1s	0x3FF
15:12	RESERVED	Read returns 0.	R	0x0
11:10	START	Starting quarter (1 KiB each unit) of bitstream buffer. Software can write a byte address to the lower 16 bits of the register.	RW	0x0
9:0	RESERVED	Read returns 0.	R	0x000

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Table 8-1501. Register Call Summary for Register VLCDJE_CBUF

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Bitstream Memory: [0] [1]
- Encode/Decode Context Switching: [2] [3]
- JPEG Encoding: [4] [5]
- Concurrent JPEG Encoding and Decoding: [6] [7]
- DMA and Buffer Manual Management: [8] [9]
- ISS SIMCOP VLCDJ Register Summary: [10]

Table 8-1502. VLCDJE_RSTCFG

Address Offset	0x0000 001C		
Physical Address	0x5202 061C 0x5506 061C	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Encode restart marker configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				INC				RESERVED				INIT				RESERVED				PHASE								RESERVED				INTRVL							

Bits	Field Name	Description	Type	Reset
31	RESERVED	Read returns 0.	R	0
30:28	INC	Restart count increment value	RW	0x1
27	RESERVED	Read returns 0.	R	0
26:24	INIT	Restart marker initial count	RW	0x0
23:22	RESERVED	Read returns 0.	R	0x0
21:12	PHASE	MCU count within the interval	RW	0x000
11:10	RESERVED	Read returns 0.	R	0x0
9:0	INTRVL	Restart interval (in MCUs)	RW	0x000

Table 8-1503. Register Call Summary for Register VLCDJE_RSTCFG

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Restart Marker Insertion for Encode:
- ISS SIMCOP VLCDJ Register Summary: [13]

Table 8-1504. VLCDJE_DCTQM

Address Offset	0x0000 0020		
Physical Address	0x5202 0620 0x5506 0620	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Encode DCT coefficient and quantizer matrix pointers		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QMR								RESERVED																DCT												RESERVED			

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Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24:23	QMR	Quarter (128 bytes/unit) of quantization matrix reciprocal. Software can write a byte address to the upper 16 bits of the register.	RW	0x0
22:14	RESERVED	Read returns 0.	R	0x000
13:4	DCT	128-bit/word address of DCT coefficients. Software can write a byte address to the lower 16 bits of the register.	RW	0x000
3:0	RESERVED	Read returns 0.	R	0x0

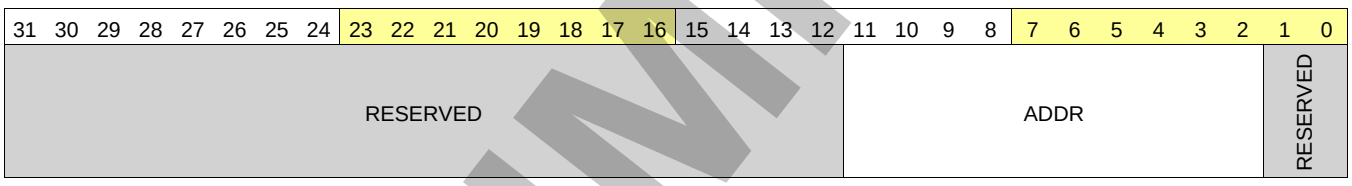
Table 8-1505. Register Call Summary for Register VLCDJE_DCTQM

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Encoding: [0] [1]
- Concurrent JPEG Encoding and Decoding: [2] [3]
- ISS SIMCOP VLCDJ Register Summary: [4]

Table 8-1506. VLCDJE_VLCTBL

Address Offset	0x0000 0024		
Physical Address	0x5202 0624 0x5506 0624	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Encode Huffman table pointer		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:2	ADDR	Encode Huffman table pointer, 32-bit word address. Software can write a byte address into the entire register.	RW	0x000
1:0	RESERVED	Read returns 0.	R	0x0

Table 8-1507. Register Call Summary for Register VLCDJE_VLCTBL

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Huffman Table for Encode Mode: [0] [1] [2] [3]
- JPEG Encoding: [4]
- Concurrent JPEG Encoding and Decoding: [5]
- ISS SIMCOP VLCDJ Register Summary: [6]

Table 8-1508. VLCDJE_RSTPTR

Address Offset	0x0000 0028		
Physical Address	0x5202 0628 0x5506 0628	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Encode restart marker locations		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR												RESERVED			

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:4	ADDR	Pointer to restart marker locations in image buffer, 128-bit/word address Software can write a byte address into the entire register.	RW	0x000
3:0	RESERVED	Read returns 0.	R	0x0

Table 8-1509. Register Call Summary for Register VLCDJE_RSTPTR

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Restart Marker Location Recording:
- ISS SIMCOP VLCDJ Register Summary: [2]

Table 8-1510. VLCDJE_RSTOFST

Address Offset	0x0000 002C		
Physical Address	0x5202 062C 0x5506 062C	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	SDRAM address to add to encode restart marker locations		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET																															

Bits	Field Name	Description	Type	Reset
31:0	OFFSET	SDRAM address of bitstream buffer, to be added to the restart marker locations	RW	0x0000 0000

Table 8-1511. Register Call Summary for Register VLCDJE_RSTOFST

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Restart Marker Location Recording:
- ISS SIMCOP VLCDJ Register Summary: [1]

Table 8-1512. VLCDJD_CFG

Address Offset	0x0000 0040		
Physical Address	0x5202 0640 0x5506 0640	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Decode configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NMCUS								RESERVED					RSTEN	FMT	

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Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:8	NMCUS	Number of MCUs (FMT = 0, 1) or blocks (FMT = 2) to decode 0: 1 MCU 1: 2 MCUs, etc.	RW	0x00
7:3	RESERVED	Read returns 0.	R	0x00
2	RSTEN	Restart marker detection/processing enable 0: Restart marker detection/processing disabled 1: Restart marker detection/processing enabled	RW	1
1:0	FMT	0: YUV4:2:0 1: YUV4:2:2 2: Sequential blocks	RW	0x0

Table 8-1513. Register Call Summary for Register VLCDJD_CFG

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Decoding: [0] [1] [2] [3]
- Concurrent JPEG Encoding and Decoding: [4] [5] [6] [7]
- ISS SIMCOP VLCDJ Register Summary: [8]

Table 8-1514. VLCDJD_DCPREDY

Address Offset	0x0000 0044		
Physical Address	0x5202 0644 0x5506 0644	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Decode DC predictor for Y		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PREDY															

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:0	PREDY	DC predictor for Y	RW	0x000

Table 8-1515. Register Call Summary for Register VLCDJD_DCPREDY

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Decoding: [0]
- Concurrent JPEG Encoding and Decoding: [1]
- ISS SIMCOP VLCDJ Register Summary: [2]

Table 8-1516. VLCDJD_DCPREDUV

Address Offset	0x0000 0048		
Physical Address	0x5202 0648 0x5506 0648	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Decode DC predictor for U and V		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PREDV								RESERVED				PREDU											

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:16	PREDV	DC predictor for V	RW	0x000
15:12	RESERVED	Read returns 0.	R	0x0
11:0	PREDU	DC predictor for U	RW	0x000

Table 8-1517. Register Call Summary for Register VLCDJD_DCPREDUV

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Decoding: [0] [1]
- Concurrent JPEG Encoding and Decoding: [2] [3]
- ISS SIMCOP VLCDJ Register Summary: [4]

Table 8-1518. VLCDJD_BSPTR

Address Offset	0x0000 004C		
Physical Address	0x5202 064C 0x5506 064C	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Decode bitstream pointer		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												BITPTR				RESERVED				BYTEPTR											

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Read returns 0.	R	0x000
19:16	BITPTR	Bit pointer, 1..8, indicates number of available bits	RW	0x8
15:12	RESERVED	Read returns 0.	R	0x0
11:0	BYTEPTR	Byte pointer (to BSMEM)	RW	0x000

Table 8-1519. Register Call Summary for Register VLCDJD_BSPTR

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Bitstream Memory: [0] [1]
- Error Reporting: [2] [3]
- JPEG Decoding: [4] [5]
- Concurrent JPEG Encoding and Decoding: [6] [7] [8]
- ISS SIMCOP VLCDJ Register Summary: [9]

Table 8-1520. VLCDJD_CBUF

Address Offset	0x0000 0050		
Physical Address	0x5202 0650 0x5506 0650	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Decode bitstream circular buffer		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				END				RESERVED								RESERVED				START		RESERVED									

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:26	END	Ending quarter (1 KiB each unit) of bitstream buffer. Software can write a byte address into the upper 16 bits of the register.	RW	0x3
25:16	RESERVED	Read returns 0x3FF.	R; returns 1s	0x3FF
15:12	RESERVED	Read returns 0.	R	0x0
11:10	START	Starting quarter (1 KiB each unit) of bitstream buffer. Software can write a byte address to the lower 16 bits of the register.	RW	0x0
9:0	RESERVED	Read returns 0.	R	0x000

Table 8-1521. Register Call Summary for Register VLCDJD_CBUF

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Bitstream Memory: [0] [1]
- Encode/Decode Context Switching: [2] [3]
- JPEG Decoding: [4] [5]
- Concurrent JPEG Encoding and Decoding: [6] [7]
- DMA and Buffer Manual Management: [8] [9]
- ISS SIMCOP VLCDJ Register Summary: [10]

Table 8-1522. VLCDJD_DCTQM

Address Offset	0x0000 0054		
Physical Address	0x5202 0654 0x5506 0654	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Decode DCT coefficient and quantizer matrix pointers		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								QM								RESERVED								DCT							
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24:23	QM	Quarter (128 bytes/unit) of quantization matrix. Software can write a byte address to the upper 16 bits of the register.	RW	0x0
22:14	RESERVED	Read returns 0.	R	0x000
13:4	DCT	128-bit/word address of DCT coefficients. Software can write a byte address to the lower 16 bits of the register.	RW	0x000
3:0	RESERVED	Read returns 0.	R	0x0

Table 8-1523. Register Call Summary for Register VLCDJD_DCTQM

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Decoding: [0] [1]
- Concurrent JPEG Encoding and Decoding: [2] [3]
- ISS SIMCOP VLCDJ Register Summary: [4]

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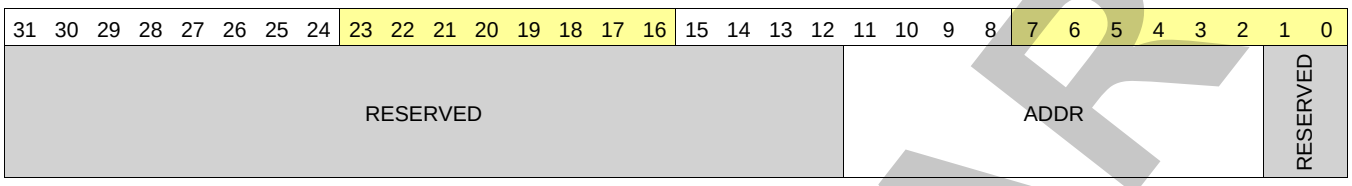
Table 8-1524. VLCDJD_CTRLTBL

Address Offset	0x0000 0058		
Physical Address	0x5202 0658 0x5506 0658	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Decode control table base		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Read returns 0.	R	0x00000
11:2	ADDR	Starting address of decode control table, 32-bit word. Software can write a byte address into the entire register.	RW	0x000
1:0	RESERVED	Read returns 0.	R	0x0

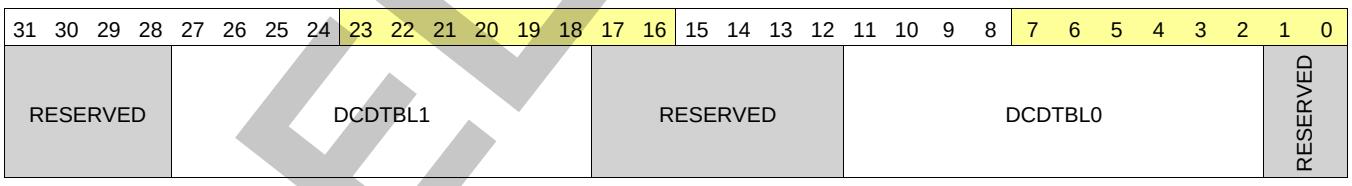
Table 8-1525. Register Call Summary for Register VLCDJD_CTRLTBL

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Decoding: [0]
- Concurrent JPEG Encoding and Decoding: [1]
- ISS SIMCOP VLCDJ Register Summary: [2]

Table 8-1526. VLCDJD_DCDTBL01

Address Offset	0x0000 005C		
Physical Address	0x5202 065C 0x5506 065C	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Decode Huffman tables 0 and 1		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:18	DCDTBL1	Starting byte address of decode table 1, 32-bit word. Software can write a byte address into the lower 16 bits of the register. This is for Luma AC.	RW	0x000
17:12	RESERVED	Read returns 0.	R	0x00
11:2	DCDTBL0	Starting byte address of decode table 0, 32-bit word. Software can write a byte address into the lower 16 bits of the register. This is for Luma DC.	RW	0x000
1:0	RESERVED	Read returns 0.	R	0x0

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Table 8-1527. Register Call Summary for Register VLCDJD_DCDTBL01

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Decoding: [2] [3]
- Concurrent JPEG Encoding and Decoding: [4] [5]
- ISS SIMCOP VLCDJ Register Summary: [6]

Table 8-1528. VLCDJD_DCDTBL23

Address Offset	0x0000 0060		
Physical Address	0x5202 0660 0x5506 0660	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description	Decode Huffman tables 2 and 3		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DCDTBL3								RESERVED								DCDTBL2							RESERVED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:18	DCDTBL3	Starting byte address of decode table 3, 32-bit word. Software can write a byte address into the lower 16 bits of the register. This is for Chroma AC.	RW	0x000
17:12	RESERVED	Read returns 0.	R	0x00
11:2	DCDTBL2	Starting byte address of decode table 2, 32-bit word. Software can write a byte address into the lower 16 bits of the register. This is for Chroma DC.	RW	0x000
1:0	RESERVED	Read returns 0.	R	0x0

Table 8-1529. Register Call Summary for Register VLCDJD_DCDTBL23

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- JPEG Decoding: [2] [3]
- Concurrent JPEG Encoding and Decoding: [4] [5]
- ISS SIMCOP VLCDJ Register Summary: [6]

Table 8-1530. VLCDJD_DCTERR

Address Offset	0x0000 0064		
Physical Address	0x5202 0664 0x5506 0664	**Instance**	VLCDJ_MAIN_L3 VLCDJ_IPU
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ERRPTR							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Read returns 0.	R	0x00000
13:0	ERRPTR	Byte address pointer to DCT coefficients, near where decode error occurs (read-only)	R	0x0000

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Table 8-1531. Register Call Summary for Register VLCDJD_DCTERR

ISS SIMCOP Variable Length Coder/Decoder for JPEG (VLCDJ) Module

- Error Reporting: [0]
- ISS SIMCOP VLCDJ Register Summary: [1]

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8.4.7 ISS SIMCOP Rotation Accelerator (ROT) Module

This section describes the rotation accelerator (ROT) module in the still-image coprocessor (SIMCOP) subsystem.

8.4.7.1 ISS SIMCOP ROT Overview

The rotation accelerator (ROT) module is intended to be used in the still-image coprocessor (SIMCOP) to perform block data rotation and data shifting from one SIMCOP local memory to another SIMCOP local memory. The following formats and operations are supported:

- YUV4:2:2 and generic 8-/16-/32-bit data block rotation by 90, 180, and 270 degrees
- YUV4:2:0 rotation by 90, 180, and 270 degrees
- Multiple-block rotation
- Data block shifting
- Data block horizontal circular shifting

The ROT supports a simple 1-block-per-initiation interaction, and includes a microcontroller unit (MCU) software-writable enable bit and hardware trigger signal to start the processing (see Section 8.4.7.3.7, *ISS SIMCOP ROT Synchronization*). It relies on external direct memory access (DMA) for transfers, and can work with the MCU or hardware sequencer to coordinate between transfer and computation.

The ROT has an input and output memory interface (see Figure 8-298). The rotation and horizontal-shifting operations read from the input memory and write to the output memory. The module connects to an input memory of up to 16 KiB (2048 × 64-bit), and an output memory of up to 16 KiB (2048 × 64-bit) using synchronous single-port memory interface.

Figure 8-296 is an overview of the ROT.

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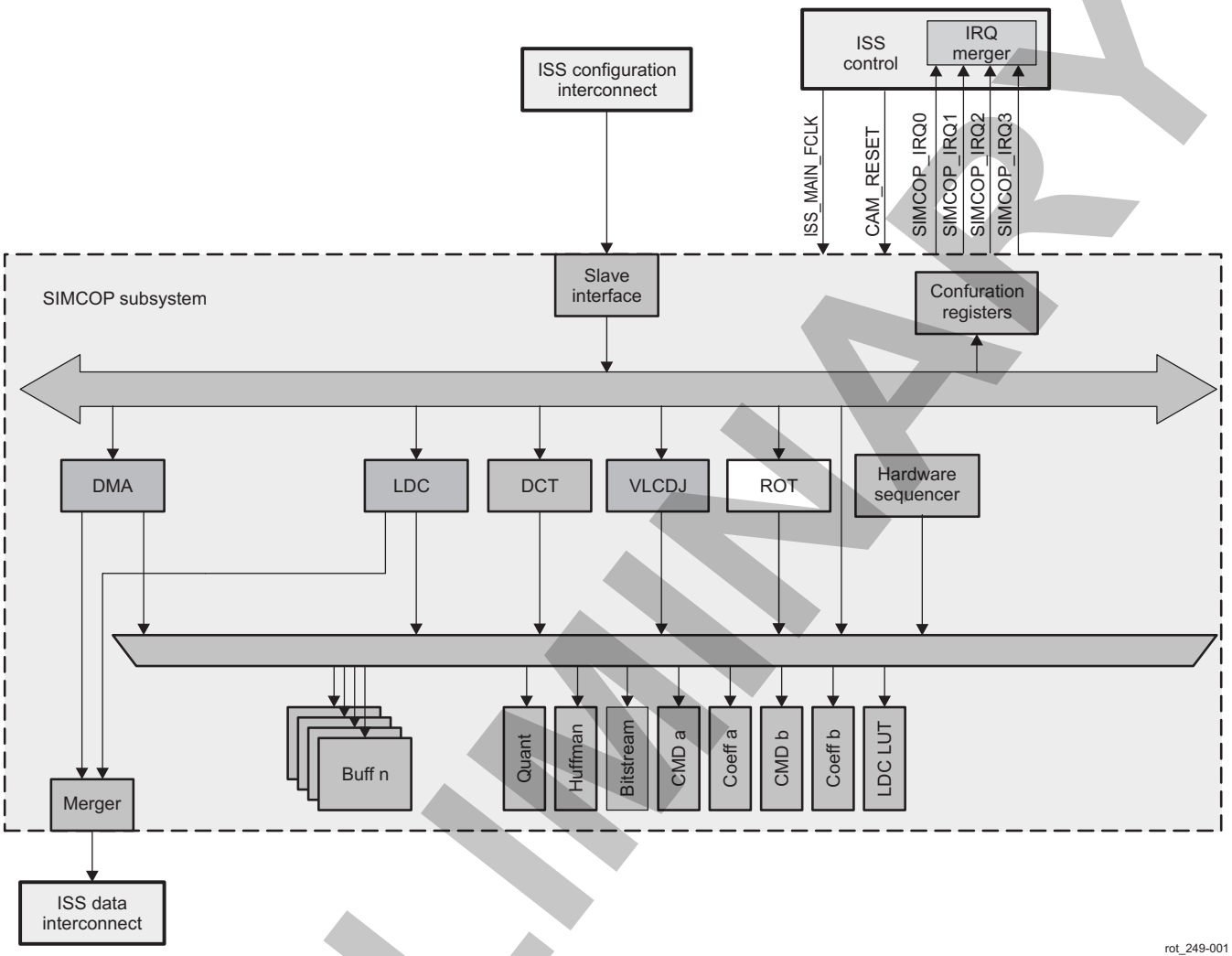
Figure 8-296. ISS SIMCOP ROT Module Overview



8.4.7.2 ISS SIMCOP ROT Integration

The ROT is part of the SIMCOP subsystem in the imaging subsystem (ISS). Figure 8-297 shows the integration of the ROT in the SIMCOP subsystem.

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Figure 8-297. ISS SIMCOP ROT Engine Integration

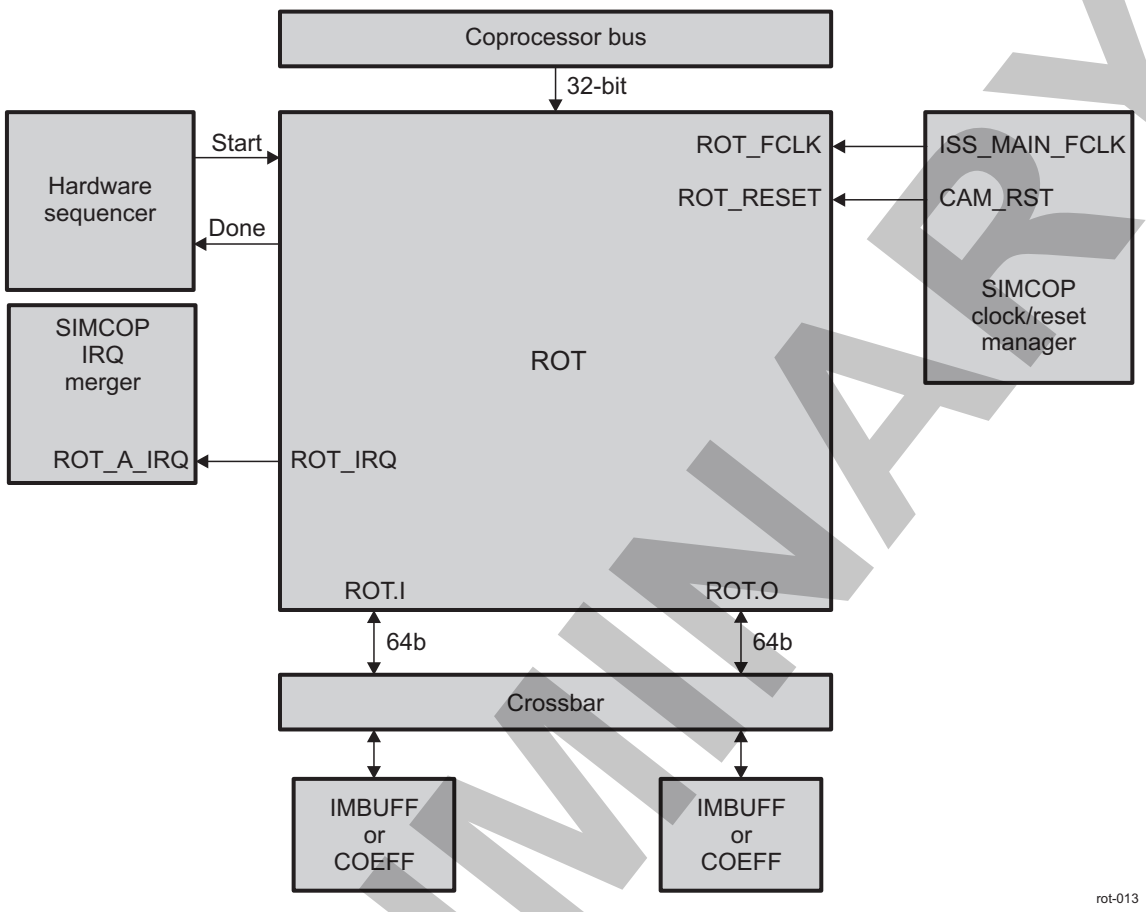

Table 8-1532 through Table 8-1534 list the integration attributes, clocks and resets, and hardware requests, respectively, of the SIMCOP ROT.

Table 8-1532. ISS SIMCOP ROT Integration Attributes

Module Instance	Attributes
	Power Domain
ROT	PD_CAM

Table 8-1533. ISS SIMCOP ROT Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
ROT	ROT_FCLK	ISS_MAIN_FCLK	ISS	Functional clock provided by CORE_ISS_MAIN_CLK from the power, reset, and clock management (PRCM) module. It is used by all ISS submodules and ISS top-level resources.
Resets				
ROT	ROT_RESET	CAM_RST	PRCM	ISS and SIMCOP global reset

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For information about clock and reset management, see Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management*.

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Table 8-1534. ISS SIMCOP ROT Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
ROT	ROT_IRQ	ROT_A_IRQ	SIMCOP IRQ merger	Event triggered by the ROT engine.

For more information about interrupt requests, see Section 8.4.1.2.3, *Interrupt Merger*.

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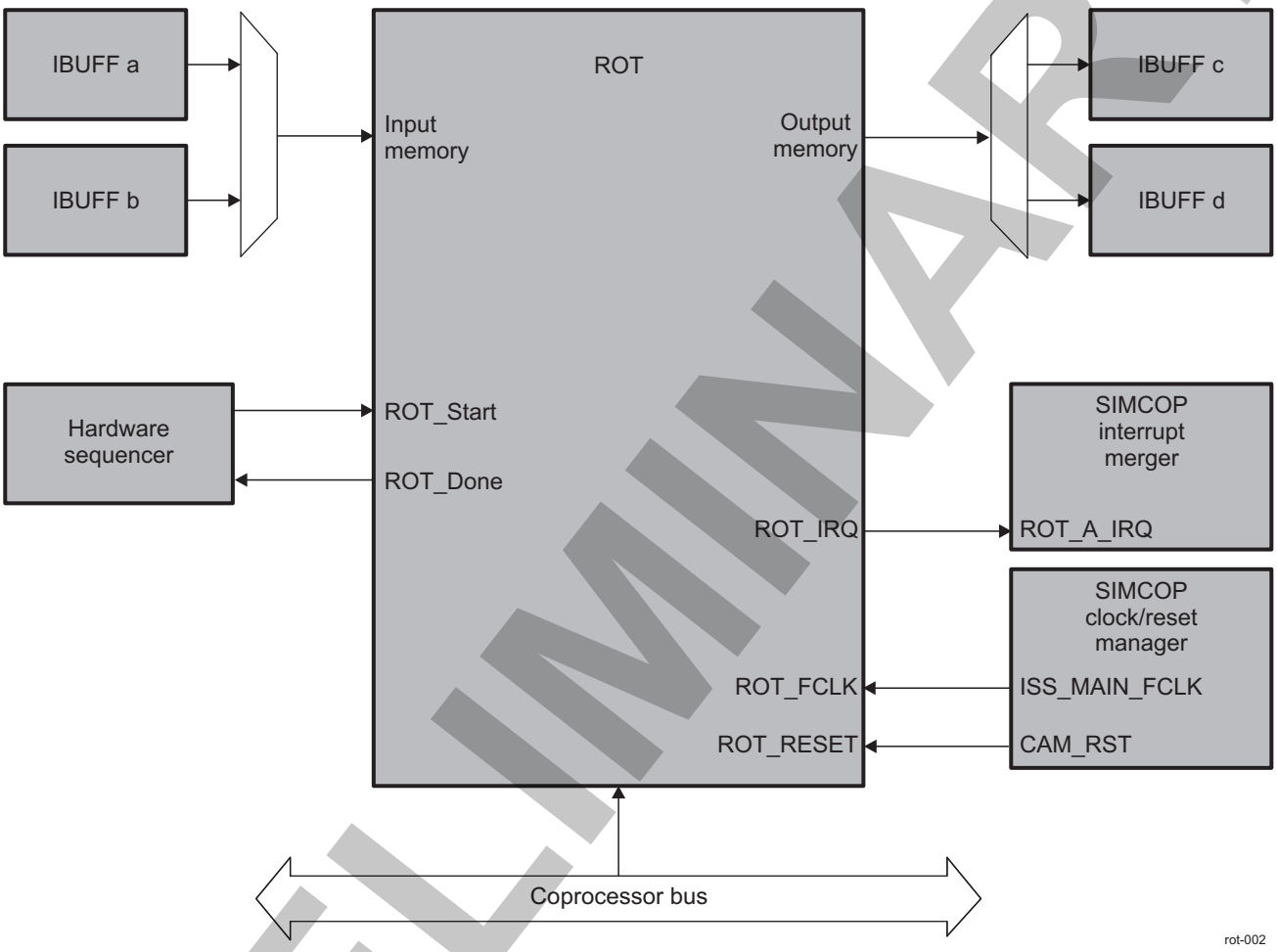
8.4.7.3 ISS SIMCOP ROT Module Functional Description

8.4.7.3.1 ISS SIMCOP ROT Module Block Diagram

Figure 8-298 shows the block diagram of the ROT.

Figure 8-298. ISS SIMCOP ROT Module Block Diagram



8.4.7.3.2 ISS SIMCOP ROT Module Clock Configuration

The ROT receives a functional clock (ISS_MAIN_FCLK) from the ISS SIMCOP. The configuration clock is derived from the functional clock and interconnect clock enable signal (the ROT_CFG[9] AUTOGATING bit).

8.4.7.3.3 ISS SIMCOP ROT Module Reset

The ROT receives an asynchronous hardware reset signal (CAM_RST) from the ISS SIMCOP.

8.4.7.3.4 ISS SIMCOP ROT Module Power Management

The ROT uses clock autogating to conserve power. When a subblock is not in use, the corresponding clock tree is gated. The ROT_CFG[9] AUTOGATING bit controls whether autogating is enabled.

8.4.7.3.5 ISS SIMCOP ROT Module Interrupt Requests

One interrupt output line, ROT_A_IRQ, is used as a sideband signal of the interconnect slave port. This signal is connected to the SIMCOP interrupt merger. See Section 8.1.2.1.1, *Interrupt Merger*.

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8.4.7.3.6 ISS SIMCOP ROT Module DMA Requests

The ROT has no DMA requests from the module.

8.4.7.3.7 ISS SIMCOP ROT Synchronization

The ROT has a simple one-block-per-task interaction with outside logic/microprocessor unit (MPU). The module can be started by setting the ROT_CTRL[0] EN bit to 0x1, or through the ROT_START signal of the hardware sequencer interface. When the ROT completes the specified rotation or data shift task, it sends a pulse on the ROT_DONE signal and, when the interrupt is enabled, sends a pulse on the ROT_A_IRQ interrupt output.

The ROT_CFG[8] TRIG_SRC bit specifies to which source the hardware must respond:

- When the module is idle and the ROT_CFG[8] TRIG_SRC bit is set to 0x0, hardware responds to the memory mapped register (MMR) mechanism, and any pulses on the start signal are ignored.
- When the module is idle and the ROT_CFG[8] TRIG_SRC bit is set to 0x1, hardware responds to the hardware start signal, and any write operation to the enable bit field is ignored.

When the module is busy, both triggering mechanisms are ignored.

8.4.7.3.8 ISS SIMCOP ROT Module Formats and Operations

The ROT module supports the formats and operations described in the following sections.

8.4.7.3.8.1 ISS SIMCOP ROT YUV4:2:0 and Generic 8-/16-/32-Bit Data Block Rotation

Rotation of YUV4:2:0 and generic 8-bit, 16-bit, 32-bit data blocks is straightforward. None of the data points are altered; each data point is copied to an appropriate address location. Zero-degree rotation is included for completeness of the programming model, and involves only data copy.

When YUV4:2:0 data have separate Y and UV processing and must be separately rotated, Y data can use generic 8-bit data rotation, and UV data can use generic 16-bit data rotation.

8.4.7.3.8.2 ISS SIMCOP ROT YUV4:2:2 Rotation

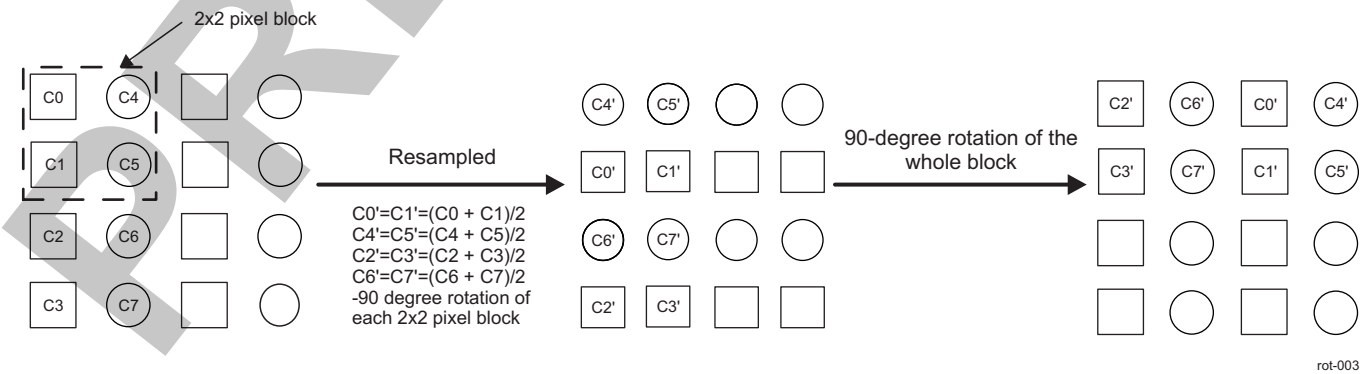
Various rotation cases of YUV4:2:2 data are described in the following and shown in Figure 8-299 through Figure 8-301 using 4 × 4-pixel block as an example.

The degree of rotation is defined as rotating clockwise. For 90-degree rotation:

- The two U samples in each 2 × 2-pixel input block are averaged and then replicated to provide the two U samples in the 2 × 2-pixel output block
- V samples - processed in the same way.

Thus, each 2N × 2N-pixel output block depends on only one 2N × 2N-pixel input block. After resampling every 2 × 2-pixel block, it is rotated –90 degrees, and then the whole 2N × 2N block is rotated 90 degrees.

Figure 8-299. ISS SIMCOP ROT 90-Degree Rotation of YUV4:2:2 Data



The same algorithm is used for 270-degree rotation.

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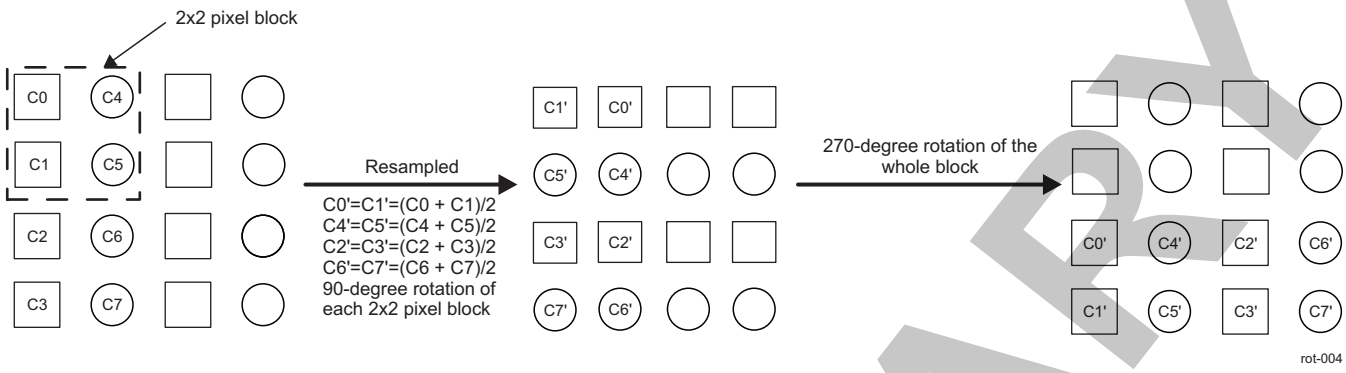
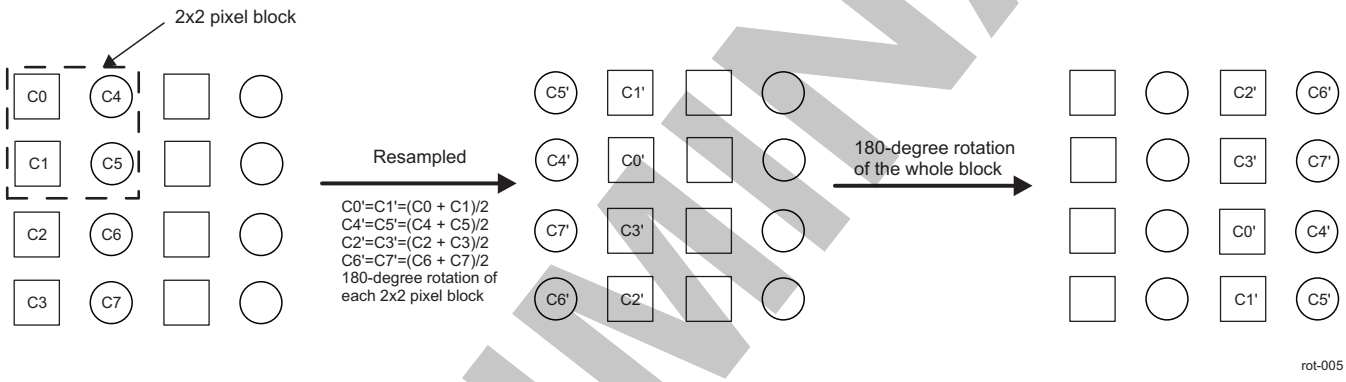
Figure 8-300. ISS SIMCOP ROT 270-Degree Rotation of YUV4:2:2 Data



For 180-degree rotation, there is no arithmetic operation; chroma values are simply shifted horizontally before being rotated.

Figure 8-301. ISS SIMCOP ROT 180-Degree Rotation of YUV4:2:2 Data



NOTE: The intermediate process of 2 × 2 pixel block rotation, represented in the middle section in Figure 8-299 through Figure 8-301, does not involve data storage and reading into memory. That middle section is for better visualization of the process. The whole process is performed with a single memory reading and writing.

Zero-degree rotation is included for completeness of programming model, and involves only data copy.

8.4.7.3.8.3 ISS SIMCOP ROT Multiple-Block Rotation

For generic 8-/16-/32-bit data rotation and YUV4:2:0/4:2:2 rotation, multiple-block operation per hardware task is supported.

Figure 8-302 through Figure 8-305 show the multiple-block rotation feature.

The multiple blocks are in the horizontal dimension, and the blocks are horizontally adjacent to one another. In other words, in the source data and 180-degree rotated data, address offset between blocks is the source block width times the data size.

In the 90-degree and 270-degree rotated data, address offset is the source block height times the data size. The source/destination line offsets must be sufficiently large to accommodate the multiple blocks.

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Figure 8-302. ISS SIMCOP ROT Block Representation Before Rotation

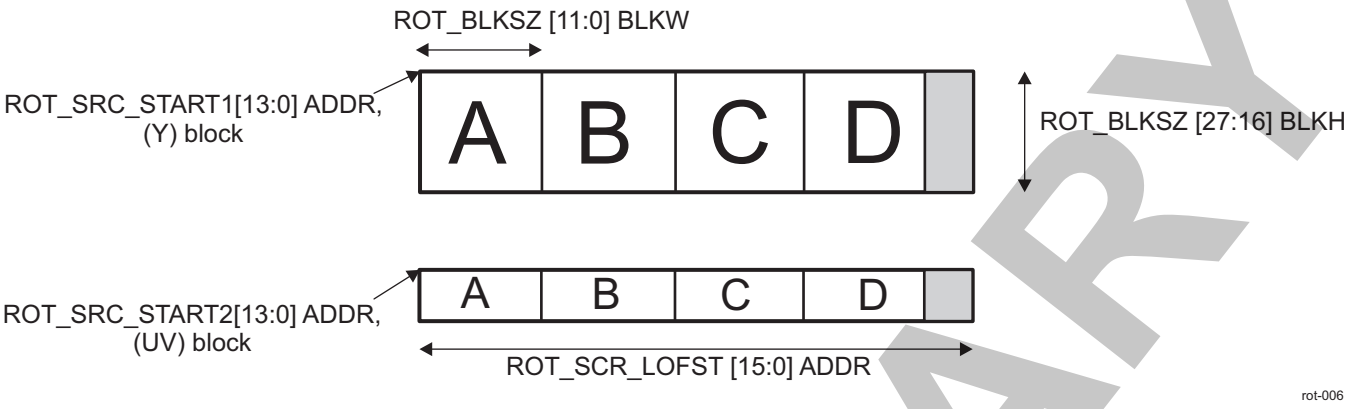

Figure 8-303. ISS SIMCOP ROT 90-Degree Block Rotation

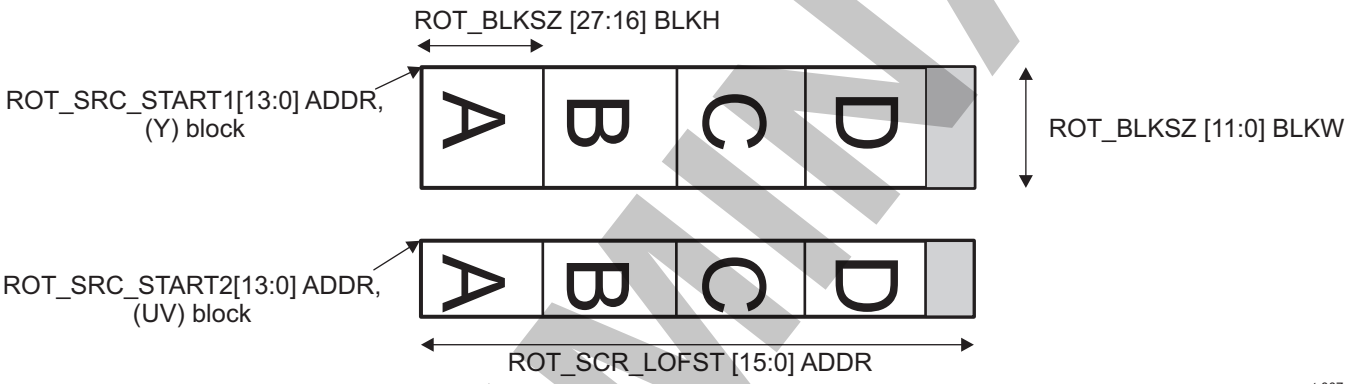

Figure 8-304. ISS SIMCOP ROT 180-Degree Block Rotation

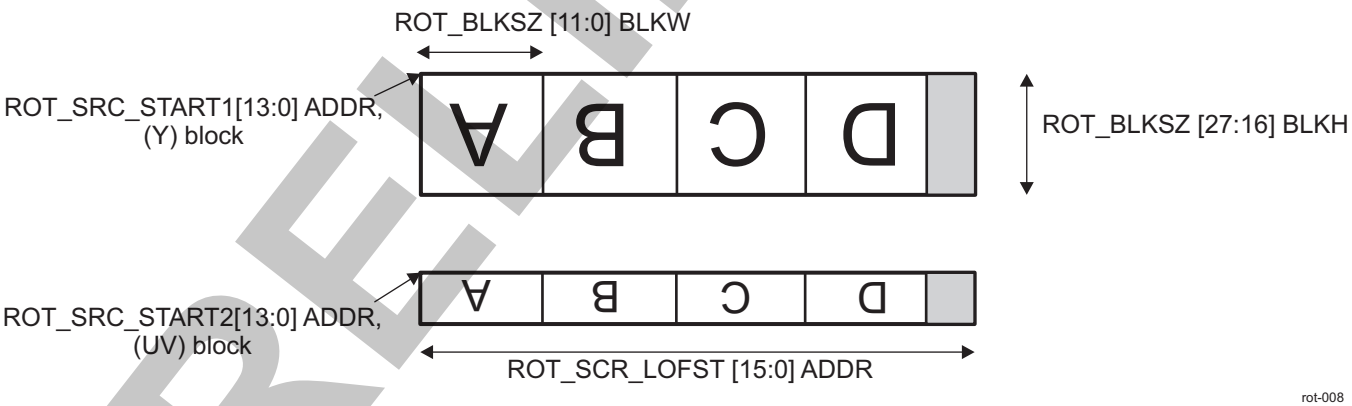

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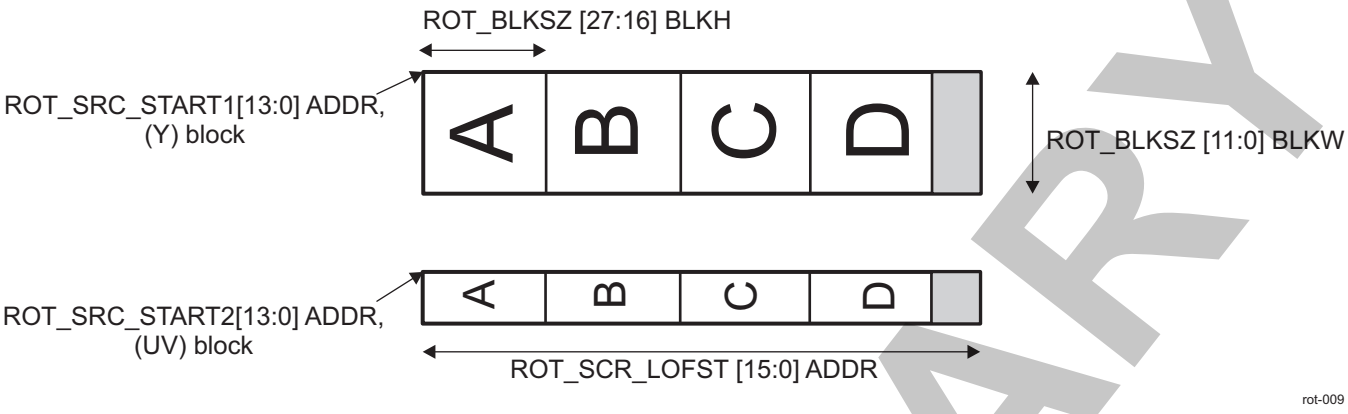
Figure 8-305. ISS SIMCOP ROT 270-Degree Block Rotation



The operation is configured with these parameters:

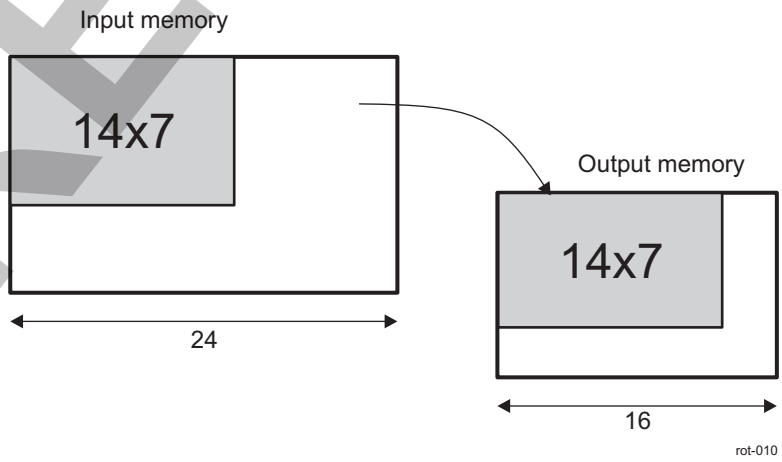
- ROT_CFG[2:0] OP (rotation orientation)
- ROT_CFG[6:4] FMT (data format)
- ROT_CFG[15:12] NBLKS (number of blocks minus 1; register value of 0 means one block, etc.)
- ROT_BLKSZ[11:0] BLKW (width of each block; all blocks are of the same width/height)
- ROT_BLKSZ[27:16] BLKH (height of each block)
- ROT_SRC_START1[13:0] ADDR (starting address of the first input block)
- ROT_SRC_LOFST[15:0] LOFST (line offset of input block)
- ROT_DST_START1[13:0] ADDR (starting address of the first output block)
- ROT_DST_LOFST[15:0]LOFST (line offset of output block)
- ROT_SRC_START2[13:0] ADDR (starting address of the first input UV block, if format is YUV4:2:0)
- ROT_DST_START2[13:0] ADDR (starting address of the first output UV block, if format is YUV4:2:0)

8.4.7.3.8.4 ISS SIMCOP ROT Data-Block Shifting

The ROT supports shifting of 2-dimensional (2D) data blocks in 8-bit granularity. This function is intended to supplement the SIMCOP DMA module, which operates on 128-bit alignment.

Figure 8-306 is an example of a 14 × 7-byte data block copied from one location in input memory to another location in output memory.

Figure 8-306. ISS SIMCOP ROT Data-Block Shifting Example



The following parameters are specified:

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- ROT_BLKSZ[11:0] BLKW = 14 (in bytes)
- ROT_BLKSZ[27:16] BLKH = 7 (in rows)
- ROT_SRC_LOFST[15:0] LOFST = 24 (in bytes)
- ROT_DST_LOFST[15:0] LOFST = 16 (in bytes)

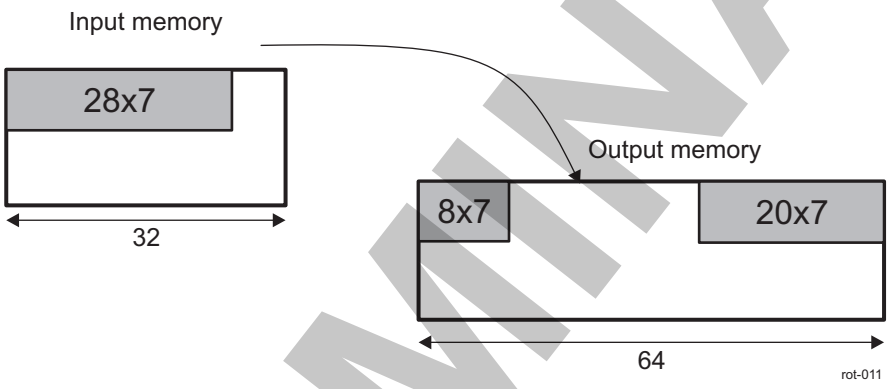
NOTE: This can be used to shift horizontally as well as vertically.

8.4.7.3.8.5 ISS SIMCOP ROT Data-Block Horizontal Circular Shifting

The ROT supports shifting of 2D data blocks in 8-bit granularity, with horizontal circular buffer addressing. This function is intended to supplement the SIMCOP DMA module, which operates on 128-bit alignment.

Figure 8-307 is an example of a 28 x 7-byte data block copied from one location in input memory to another location in output memory, and horizontal wrap-around occurs in the output memory.

Figure 8-307. ISS SIMCOP ROT Horizontal Circular Shifting Example



The following parameters are specified:

- ROT_BLKSZ[11:0] BLKW = 28 (in bytes)
- ROT_BLKSZ[27:16] BLKH = 7 (in rows)
- ROT_SRC_LOFST[15:0] LOFST = 32 (in bytes)
- ROT_DST_LOFST[15:0] LOFST = 64 (in bytes)

Wrapping around is allowed in the input memory, in the output memory, or in both. For this mode of operation, the line offset of the source and destination must be a power of 2, and at least 32 bytes. Source and destination line offsets can be different. This function is used to handle misaligned SDRAM data. The example that follows in this section shows that the line offset is at least the minimal transfer width, or the SDRAM burst. For target applications, 32 bytes is the minimal burst size to support.

NOTE: This can be used to shift horizontally as well as vertically. Input and output blocks can also have different line offsets.

This mode of operation is intended to be used to manage 2D data blocks that are out of SDRAM alignment (for example, to crop out the left-most 2 pixels of the ISP YUV4:2:2 output image before JPEG compression). Assume that the ISP output is 64-byte SDRAM burst-aligned; thus, the starting address for JPEG input is 4 bytes out of alignment. Without the horizontal circular shifting function, the best solution is to use wide data blocks (for example, 128 pixels = 256 bytes wide) to reduce the bandwidth penalty of misalignment (costing five bursts to get four bursts worth of data). With horizontal circular shifting, the bandwidth penalty can be eliminated. In this example, the SIMCOP DMA is configured to transfer aligned data, and the ROT is used to perform the crop-out. A memory transaction log would be:

- The DMA writes columns 0–63, starting at byte address 0.
- The DMA writes columns 64–127, starting at byte address 64.
- The ROT module reads columns 4–67, starting at byte address 4.

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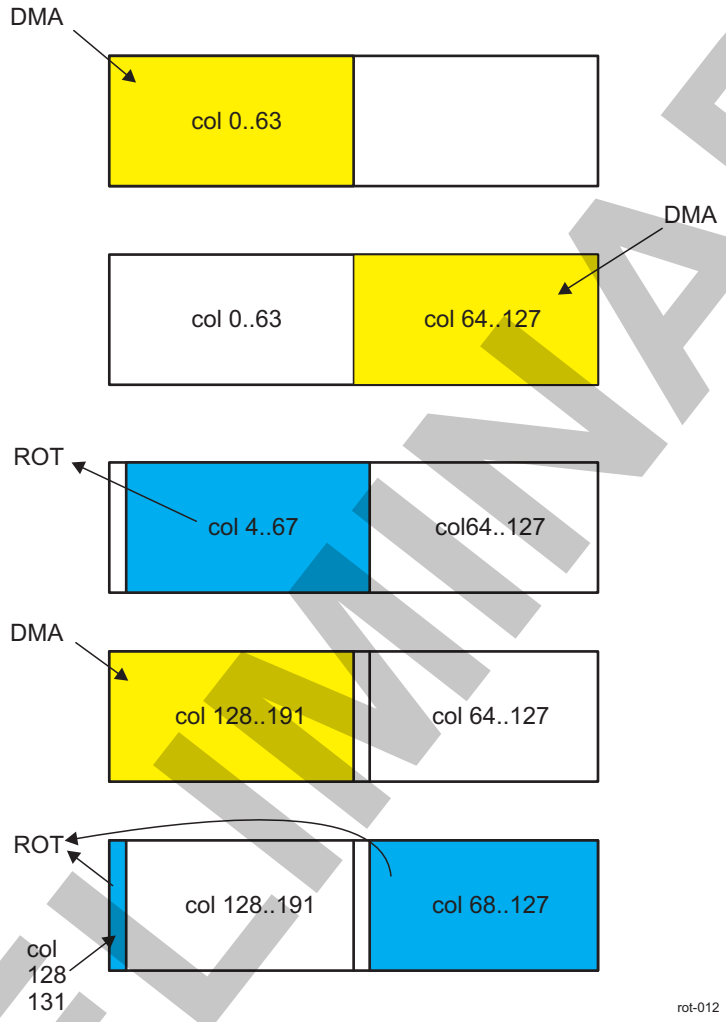
- The DMA writes columns 128–191, starting at byte address 0.
- The ROT module reads columns 68–131, starting at byte address 68, and so on.

Figure 8-308 shows the data movement by the DMA and the ROT.

Figure 8-308. ISS SIMCOP ROT Using Horizontal Circular Shifting to Manage Misaligned Data



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8.4.7.4 ISS SIMCOP ROT Module Programming Guide

8.4.7.4.1 ISS SIMCOP ROT Module Low-Level Programming Models

This section describes the low-level programming sequences for configuration and use of the ROT.

8.4.7.4.1.1 ISS SIMCOP ROT Global Initialization

8.4.7.4.1.1.1 ISS SIMCOP ROT Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the ROT is to be used for the first time after a device reset. Initialization of surrounding modules is based on the integration and environment of the module.

Table 8-1535 describes the global initialization of the surrounding modules.

Table 8-1535. ISS SIMCOP ROT Global Initialization of Surrounding Modules

Surrounding Modules	Comments
SIMCOP (clock management)	The ROT functional clock must be enabled. See Section 8.4.7.3.2, *ISS SIMCOP ROT Module Clock Configuration*.
SIMCOP (power management)	The ROT must be enabled (SIMCOP_CLKCTRL[7] ROT_A). See Section 8.4.1.2.1, *ISS SIMCOP Local Power and Clock Management* .
Buffers	Configure the ROT access to the image buffer inside the SIMCOP_HWSEQ_STEP_SWITCH_i register. See Section 8.4.2, *ISS SIMCOP Hardware Sequencer and Buffers Module*.
SIMCOP IRQ merger	Configure SIMCOP to handle the ROT interrupts. See Section 8.1.2.1.1, *Interrupt Merger*
SIMCOP hardware sequencer	Configure the hardware sequencer to activate the ROT. See Section 8.4.2,*ISS SIMCOP Hardware Sequencer and Buffers Module*.

8.4.7.4.1.1.2 ISS SIMCOP ROT Global Initialization

Table 8-1536 describes the global initialization of the ROT.

Table 8-1536. ISS SIMCOP ROT Global Initialization of the ROT

Step	Register/Bit Field/Programming Model	Value
Enable the ROT module.	ROT_CTRL[0] EN	0x0

8.4.7.4.1.2 ISS SIMCOP ROT Operational Modes Configuration

8.4.7.4.1.2.1 ISS SIMCOP ROT Rotation

The proper value for the trigger source bit (ROT_CFG[8] TRIG_SRC) is set depending on whether the operation is to be triggered by software, writing to MMR, or by the hardware sequencer. Table 8-1537 lists the procedure to set the value of the trigger source bit.

Table 8-1537. ISS SIMCOP ROT Trigger Source Bit Value

Step	Register/Bit Field/Programming Model	Value
Configure the degree of rotation.	ROT_CFG[2:0] OP	xxx
Configure the data format.	ROT_CFG[6:4] FMT	xxx
Specify the block width and height.	ROT_BLKSZ[11:0] BLKW ROT_BLKSZ[27:16] BLKH	xxx
Specify the input and output starting addresses.	ROT_SRC_START1[13:0] ADDR, ROT_DST_START1[13:0] ADDR	xxx
Specify the line offsets.	ROT_SRC_LOFST[15:0] LOFST, ROT_DST_LOFST[15:0] LOFST	xxx

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Table 8-1537. ISS SIMCOP ROT Trigger Source Bit Value (continued)

Step	Register/Bit Field/Programming Model	Value
For UV data of YUV4:2:0, input and output second starting addresses.	ROT_SRC_START2[13:0] ADDR, ROT_DST_START2[13:0] ADDR	xxx

8.4.7.4.1.2.2 ISS SIMCOP ROT Data-Block Shifting

Table 8-1538 lists the bit field values for data-block shifting.

Table 8-1538. ISS SIMCOP ROT Data-Block Shifting

Step	Register/Bit Field/Programming Model	Value
Configure shifting.	ROT_CFG[2:0] OP	xxx
Set the data shifting block.	ROT_CFG[6:4] FMT	xxx
Specify the block width and height.	ROT_BLKSZ[11:0] BLKW, ROT_BLKSZ[27:16] BLKH	xxx
Specify the input and output starting addresses.	ROT_SRC_START1[13:0] ADDR, ROT_DST_START1[13:0] ADDR	xxx
Specify the line offsets.	ROT_SRC_LOFST[15:0] LOFST, ROT_DST_LOFST[15:0] LOFST	xxx

Once the input data and output buffer are available, the ROT_CTRL[0] EN bit is set to 1 to trigger the operation through software. Alternatively, DMA transfer(s) and the hardware sequencer are configured to trigger the ROT with the hardware start signal when appropriate.

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8.4.7.5 ISS SIMCOP ROT Register Manual

8.4.7.5.1 ISS SIMCOP ROT Instance Summary

Table 8-1539 lists the ROT instance.

Table 8-1539. ISS SIMCOP ROT Instance Summary

Module Name	L3_MAIN Base Address	IPU Base Address	Size
ROT	0x5202 0700	0x5506 0700	64 bytes

8.4.7.5.2 ISS SIMCOP ROT Registers

8.4.7.5.2.1 ISS SIMCOP ROT Register Summary

Table 8-1540 summarizes the ROT registers.

Table 8-1540. ROT Module Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ROT L3_MAIN Physical Address	ROT IPU Physical Address Private Access
ROT_REVISION	R	32	0x0000 0000	0x5202 0700	0x5506 0700
ROT_CTRL	W	32	0x0000 0004	0x5202 0704	0x5506 0704
ROT_CFG	RW	32	0x0000 0008	0x5202 0708	0x5506 0708
ROT_BLKSZ	RW	32	0x0000 000C	0x5202 070C	0x5506 070C
ROT_SRC_START1	RW	32	0x0000 0010	0x5202 0710	0x5506 0710
ROT_SRC_LOFST	RW	32	0x0000 0014	0x5202 0714	0x5506 0714
ROT_DST_START1	RW	32	0x0000 0018	0x5202 0718	0x5506 0718
ROT_DST_LOFST	RW	32	0x0000 001C	0x5202 071C	0x5506 071C
ROT_SRC_START2	RW	32	0x0000 0020	0x5202 0720	0x5506 0720
ROT_DST_START2	RW	32	0x0000 0024	0x5202 0724	0x5506 0724

8.4.7.5.2.2 ISS SIMCOP ROT Register Description

through describe the ROT registers.

Table 8-1541. ROT_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5202 0700 0x5506 0700	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Module revision		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	IP Revision	R	TI Internal Data

Table 8-1542. Register Call Summary for Register ROT_REVISION

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Register Summary: [0]

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Table 8-1543. ROT_CTRL

Address Offset	0x0000 0004		
Physical Address	0x5202 0704 0x5506 0704	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Control		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUSY	RESERVED														EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	BUSY	Idle/busy status (read-only) 0 = Idle, 1 = Busy	R	0
14:1	RESERVED		R	0x0000
0	EN	Module enable, writing 1 starts the module; always reads as 0.	W	0

Table 8-1544. Register Call Summary for Register ROT_CTRL

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Synchronization: [0]
- ISS SIMCOP ROT Global Initialization: [1]
- ISS SIMCOP ROT Data-Block Shifting: [2]
- ISS SIMCOP ROT Register Summary: [3]

Table 8-1545. ROT_CFG

Address Offset	0x0000 0008		
Physical Address	0x5202 0708 0x5506 0708	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NBLKS				RESERVED		AUTOGATING	TRIG_SRC	RESERVED			FMT			RESERVED			OP

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	NBLKS	Number of blocks minus 1 0: 1 block, 1: 2 blocks, etc.	RW	0x0
11:10	RESERVED		R	0x0
9	AUTOGATING	Internal interconnect and functional clock gating 0: Interconnect and functional clocks are free-running. 1: Automatic clock gating is applied, based on the interface activity for the interface clock, and on the functional activity for the functional clocks.	RW	1
8	TRIG_SRC	Trigger source 0 = MMR write 1 = Hardware start signal	RW	0

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Bits	Field Name	Description	Type	Reset
7	RESERVED		R	0
6:4	FMT	Data format 0 = 8-bit data 1 = 16-bit data 2 = 32-bit data 3 = YUV4:2:2 data 4 = YUV4:2:0 data	RW	0x0
3	RESERVED		R	0
2:0	OP	Operation 0 = Rotate 0 degree 1 = Rotate 90 degrees 2 = Rotate 180 degrees 3 = Rotate 270 degrees 4 = Data shift (FMT = 0) 5 = Horizontal circular (FMT = 0) shift	RW	0x0

Table 8-1546. Register Call Summary for Register ROT_CFG

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Module Clock Configuration: [0]
- ISS SIMCOP ROT Module Power Management: [1]
- ISS SIMCOP ROT Synchronization: [2] [3] [4]
- ISS SIMCOP ROT Multiple-Block Rotation: [5] [6] [7]
- ISS SIMCOP ROT Rotation: [8] [9] [10]
- ISS SIMCOP ROT Data-Block Shifting: [11] [12]
- ISS SIMCOP ROT Register Summary: [13]

Table 8-1547. ROT_BLKSZ

Address Offset	0x0000 000C		
Physical Address	0x5202 070C 0x5506 070C	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Block size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BLKH								RESERVED				BLKW											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	BLKH	Block height, in pixels (YUV4:2:0/4:2:2) or number of rows (8-/16-/32-bit). Should be a multiple of 8, and at least 8, for rotation. Should be at least 1 for data shifting.	RW	0x000
15:12	RESERVED		R	0x0
11:0	BLKW	Block width, in pixels (YUV4:2:0/4:2:2) or data units (8-/16-/32-bit). Should be a multiple of 8, and at least 8, for rotation. Should be at least 4 for data shifting.	RW	0x000

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Table 8-1548. Register Call Summary for Register ROT_BLKSZ

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Multiple-Block Rotation: [0] [1]
- ISS SIMCOP ROT Data-Block Shifting: [2] [3]
- ISS SIMCOP ROT Data-Block Horizontal Circular Shifting: [4] [5]
- ISS SIMCOP ROT Rotation: [6] [7]
- ISS SIMCOP ROT Data-Block Shifting: [8] [9]
- ISS SIMCOP ROT Register Summary: [10]

Table 8-1549. ROT_SRC_START1

Address Offset	0x0000 0010		
Physical Address	0x5202 0710 0x5506 0710	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Source starting address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDR							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	ADDR	Byte address Should be a multiple of 8 for rotation. No constraint for data shifting.	RW	0x0000

Table 8-1550. Register Call Summary for Register ROT_SRC_START1

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Multiple-Block Rotation: [0]
- ISS SIMCOP ROT Rotation: [1]
- ISS SIMCOP ROT Data-Block Shifting: [2]
- ISS SIMCOP ROT Register Summary: [3]

Table 8-1551. ROT_SRC_LOFST

Address Offset	0x0000 0014		
Physical Address	0x5202 0714 0x5506 0714	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Source line offset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LOFST															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	LOFST	Line offset in bytes Should be a multiple of 8 for rotation and normal data shifting. Should be a power of 2 and at least 32 for horizontal circular shifting.	RW	0x0000

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Table 8-1552. Register Call Summary for Register ROT_SRC_LOFST

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Multiple-Block Rotation: [0]
- ISS SIMCOP ROT Data-Block Shifting: [1]
- ISS SIMCOP ROT Data-Block Horizontal Circular Shifting: [2]
- ISS SIMCOP ROT Rotation: [3]
- ISS SIMCOP ROT Data-Block Shifting: [4]
- ISS SIMCOP ROT Register Summary: [5]

Table 8-1553. ROT_DST_START1

Address Offset	0x0000 0018		
Physical Address	0x5202 0718 0x5506 0718	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Destination starting address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDR							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	ADDR	Byte address Should be a multiple of 8 for rotation. No constraint for data shifting.	RW	0x0000

Table 8-1554. Register Call Summary for Register ROT_DST_START1

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Multiple-Block Rotation: [0]
- ISS SIMCOP ROT Rotation: [1]
- ISS SIMCOP ROT Data-Block Shifting: [2]
- ISS SIMCOP ROT Register Summary: [3]

Table 8-1555. ROT_DST_LOFST

Address Offset	0x0000 001C		
Physical Address	0x5202 071C 0x5506 071C	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Destination line offset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LOFST															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	LOFST	Line offset in bytes Should be a multiple of 8 for rotation and normal data shifting. Should be a power of 2 and at least 32 for horizontal circular shifting.	RW	0x0000

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Table 8-1556. Register Call Summary for Register ROT_DST_LOFST

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Multiple-Block Rotation: [0]
- ISS SIMCOP ROT Data-Block Shifting: [1]
- ISS SIMCOP ROT Data-Block Horizontal Circular Shifting: [2]
- ISS SIMCOP ROT Rotation: [3]
- ISS SIMCOP ROT Data-Block Shifting: [4]
- ISS SIMCOP ROT Register Summary: [5]

Table 8-1557. ROT_SRC_START2

Address Offset	0x0000 0020		
Physical Address	0x5202 0720 0x5506 0720	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Source starting address 2 (only form YUV4:2:0 FMT = 2)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDR							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	ADDR	Byte address, should be a multiple of 8.	RW	0x0000

Table 8-1558. Register Call Summary for Register ROT_SRC_START2

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Multiple-Block Rotation: [0]
- ISS SIMCOP ROT Rotation: [1]
- ISS SIMCOP ROT Register Summary: [2]

Table 8-1559. ROT_DST_START2

Address Offset	0x0000 0024		
Physical Address	0x5202 0724 0x5506 0724	**Instance**	ROT_MAIN_L3 ROT_IPU
Description	Destination starting address 2 (only form YUV4:2:0 FMT = 2)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDR							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:0	ADDR	Byte address, should be a multiple of 8.	RW	0x0000

Table 8-1560. Register Call Summary for Register ROT_DST_START2

ISS SIMCOP Rotation Accelerator (ROT) Module

- ISS SIMCOP ROT Multiple-Block Rotation: [0]
- ISS SIMCOP ROT Rotation: [1]
- ISS SIMCOP ROT Register Summary: [2]

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Face Detect

This chapter describes the features and functions of the face detection interface (FDIF) module of the multimedia device.

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9.2	**FDIF Integration**	**2486**
9.3	**FDIF Functional Description**	**2488**
9.4	**FDIF Programming Guide**	**2494**
9.5	**FDIF Register Manual**	**2497**

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9.1 Face Detect Overview

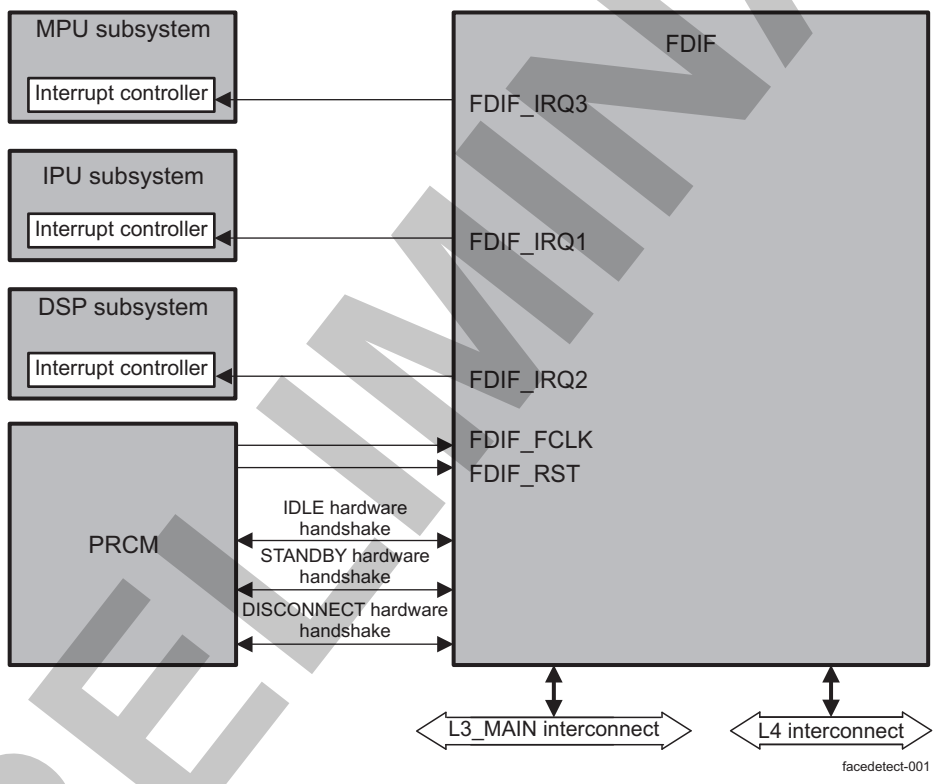
The FDIF module performs face detection within a picture stored in memory (QVGA luminance data resolution). This module is typically used for video encoding, face-based priority auto-focusing, or red-eye removal.

The face detect (FD) core is a stand-alone module: it embeds its own direct memory access (DMA) engine for accessing data in memory. The FD core is under microprocessor unit (MPU) control for its initialization and to start the processing operation.

The FD core supports single input resolution (QVGA) in a single format (8-bit Luma). The FD core requires that the input image is stored in synchronous dynamic random access memory (SDRAM). The core also requires working memory mapped in SDRAM. The input image data (320 × 240) requires 75KiB for the SDRAM and 51.25KiB for the working memory.

Figure 9-1 is an overview of the FDIF. Three interrupt lines go to the three central processing units (CPUs) to allow control of the FD core module by different processors, but only one interrupt at a time can be active. The three interrupt lines provide flexibility for controlling the module.

Figure 9-1. Face Detect Highlight



9.1.1 Main Features

The FDIF has the following features:

- Two interconnects interface:
  - 32-bit-wide level 4 (L4) interface for register configuration
  - 32-bit-wide level 3 (L3_MAIN) interface for command
- Supports the IDLE, STANDBY, and DISCONNECT protocols
- Asynchronous bridge (asynchronous master and slave interfaces)
- 60fps frame rate for FaceDetection processing
- Third-party IP features: For information about the input image features and detection capabilities, see Table 9-1.

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Table 9-1. Third-Party IP Features

Items	Description
Input image size	QVGA input image size H x V = 320 x 240
Input image data format	8-bit gray scale data in little-endian format (color pictures must be converted before FD can be applied) 0x00 = black and 0xFF = white
Face inclination	± 45 degrees
Face direction	Up or down: ± 30 degrees Left or right: ± 60 degrees
Maximum detection count	35 faces
Detection direction	The face orientation must be selected from the following possibilities: 0 degrees: Faces are vertical. + 90 degrees: Faces are rotated right by 90 degrees. – 90 degrees: Faces are rotated left by 90 degrees.
Detection minimum face size	Four grades are available: 20 pixels 25 pixels 32 pixels 40 pixels
Detection area	Detection start position: X = 0 to 160 Y = 0 to 120 Detection area size: X = 160 to 320 Y = 120 to 240
Detection result	The following information is provided by the module for each face: Size Position Angle Confidence level

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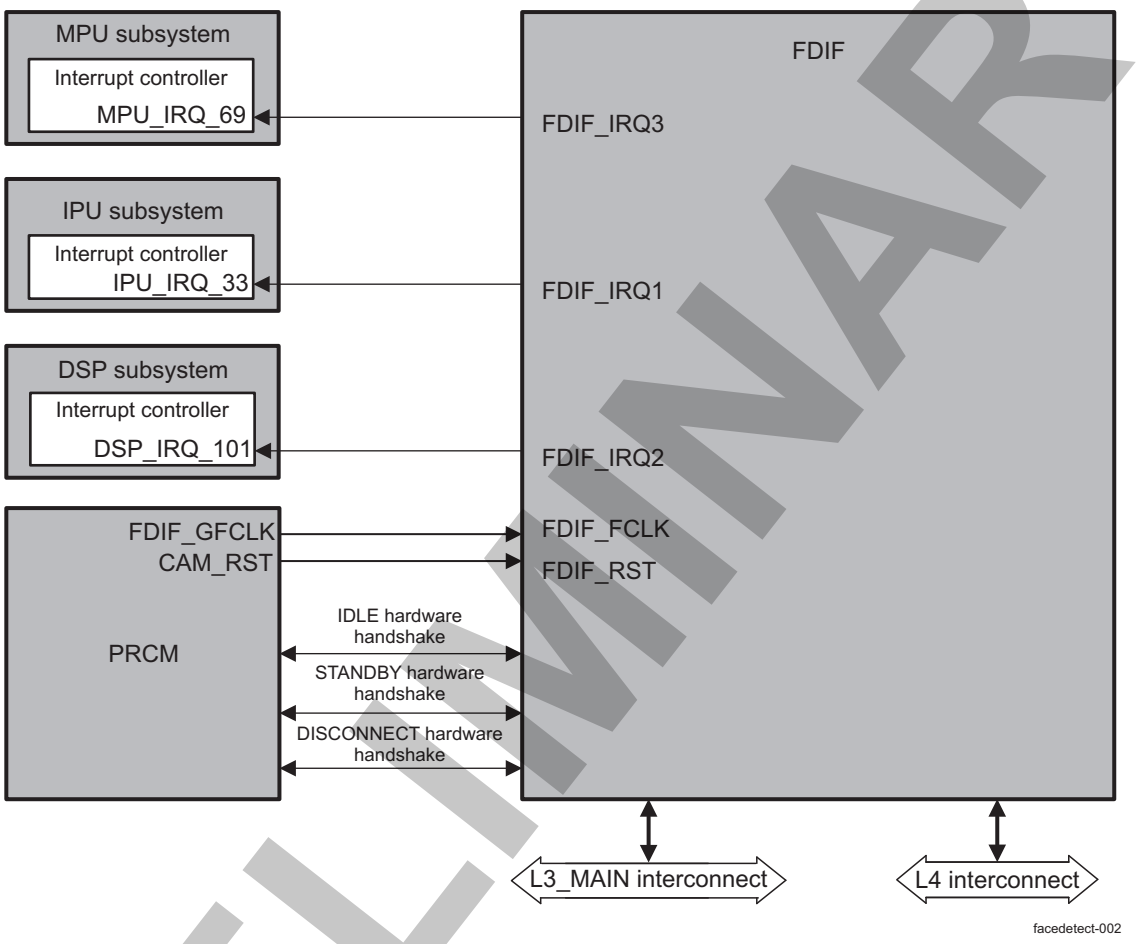
9.2 FDIF Integration

This section describes the integration of FDIF in the device, including information about clocks, resets, and hardware requests.

Figure 9-2 shows the integration of the module in the device.

Figure 9-2. FDIF Integration



NOTE: For more information about the IDLE, STANDBY, and DISCONNECT hardware handshakes, see Section 3.1.1, *Power, Reset, and Clock Management*.

Table 9-2 through Table 9-4 summarize the integration of the module in the device. For more information about the power domain or the clock and reset signals, see Section 3.1.1, *Power, Reset, and Clock Management*.

Table 9-2. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
Face detect	PD_CAM	No	L3_MAIN

Table 9-3. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description

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Table 9-3. Clocks and Resets (continued)

Face detect	FDIF_FCLK	FDIF_GFCLK	PRCM	For information about PRCM clock gating and management, see Section 3.6 *Clock Management Functional Description, in* Section 3.1.1, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
Face detect	FDIF_RST	CAM_RST	PRCM	For information about PRCM reset sources and distribution, see Section 3.5 *Reset Management Functional Description, in* Section 3.1.1, *Power, Reset, and Clock Management*.

Table 9-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
Face detect	FDIF_IRQ3	MPU_IRQ_69	MPU subsystem	FDIF interrupt to the MPU subsystem
Face detect	FDIF_IRQ1	IPU_IRQ_33	IPU subsystem	FDIF interrupt to the IPU subsystem
Face detect	FDIF_IRQ2	DSP_IRQ_101	DSP subsystem	FDIF interrupt to the digital signal processor (DSP) subsystem
No DMA Requests				

NOTE: For more information about interrupt sources, see Section 9.3.4, *Interrupts and Events*.

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9.3 FDIF Functional Description

9.3.1 FDIF Block Description

The FDIF is a stand-alone module. It has a port connected to the L4 interconnect, which is used for configuration, and a port connected to the L3_MAIN interconnect, which is used to read and write data to the system memory.

NOTE: These ports are accessible only in 32 bits.

The FD core contains the following submodules:

- FD IP core
- RAM and ROM memories

The FDIF module wraps the FD core for integration in the device. The following submodules are added:

- Clock generation
- Interrupt generation
- Power management
- L3_MAIN and L4 interface ports: Two ports required to decorrelate the FDIF clocks from other system clocks, one on the L3_MAIN port interface, and one on the L4 port interface.

Figure 9-3 shows the overall architecture of the FDIF.

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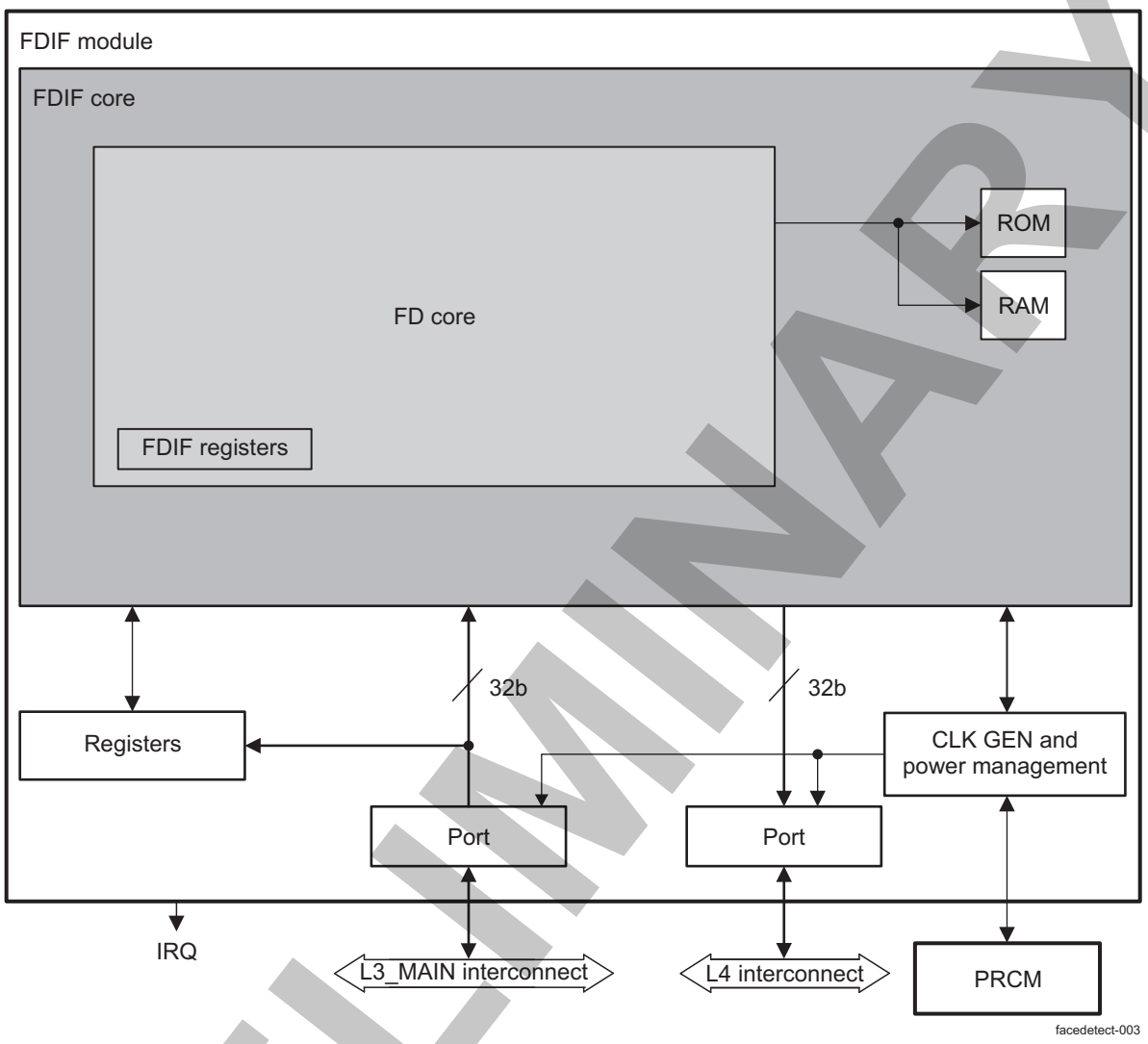
Figure 9-3. FDIF Block Diagram



9.3.2 Software Reset

The module is reset by setting the FDIF_SYSCONFIG[0] SOFTRESET bit to 1. The bit is automatically reset by hardware. During reads, it always returns 0.

The FD core also provides a software reset setup by the FD_CTRL[0] SRST bit, but it is strongly recommended to use only the FDIF_SYSCONFIG[0] SOFTRESET bit.

9.3.3 System Power Management

There is one clock domain in FDIF: the L4 port domain and L3_MAIN port domain are synchronized with the module functional clock domain, FDIF_FCLK.

Table 9-5 lists the power-management features available for FDIF.

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NOTE:

- For more information about source clock gating, see Section 3.1.1, *Power, Reset, and Clock Management*.
- For descriptions of idle mode and standby mode and the power, reset, and clock management (PRCM) power handshake, see Section 3.1.1, *Power, Reset, and Clock Management*.

Table 9-5. Local Power-Management Features

Feature	Registers	Description
Clock autogating	No software control for it.	It is always enabled.
Slave idle modes	FDIF_SYSCONFIG[3:2] IDLEMODE	Force-idle, no-idle, and smart-idle modes are available.
Clock activity	N/A	
Master standby modes	FDIF_SYSCONFIG[5:4] STANDBYMODE	Force-standby, no-standby, and smart-standby modes are available. For more information, see Section 9.3.3.2.1, *Protocol Transitions*.
Global wake-up enable	N/A	
Wake-up sources enable	N/A	

9.3.3.1 Autogating

The FDIF performs clock autogating whenever possible. There is no software control for the FDIF; it is always enabled.

9.3.3.2 PRCM Hardware Handshake

The FDIF supports the IDLE protocol between the L4 port and the PRCM module and the STANDBY protocol between the L3_MAIN port and the PRCM module. The FDIF also supports the DISCONNECT protocol on the L4 and L3_MAIN ports.

The FDIF first initiates the STANDBY protocol with the PRCM module, which in turn generates the IDLE protocol with the FDIF. The functional clock is gated by the PRCM module only when the IDLE and STANDBY power-management protocols are complete.

For more information about these protocols, see Section 3.1.1, *Power, Reset, and Clock Management*.

9.3.3.2.1 Protocol Transitions

The FDIF enters the IDLE state as soon as it is done processing and the MPU has read the results of the computation.

Figure 9-4 shows the principle. The 33-ms period corresponds to a 60 fps, which is usually the target for imaging applications. Time spent in the READ state (ON state) is always the same, and the time in OFF state depends on the time spent in ON state.

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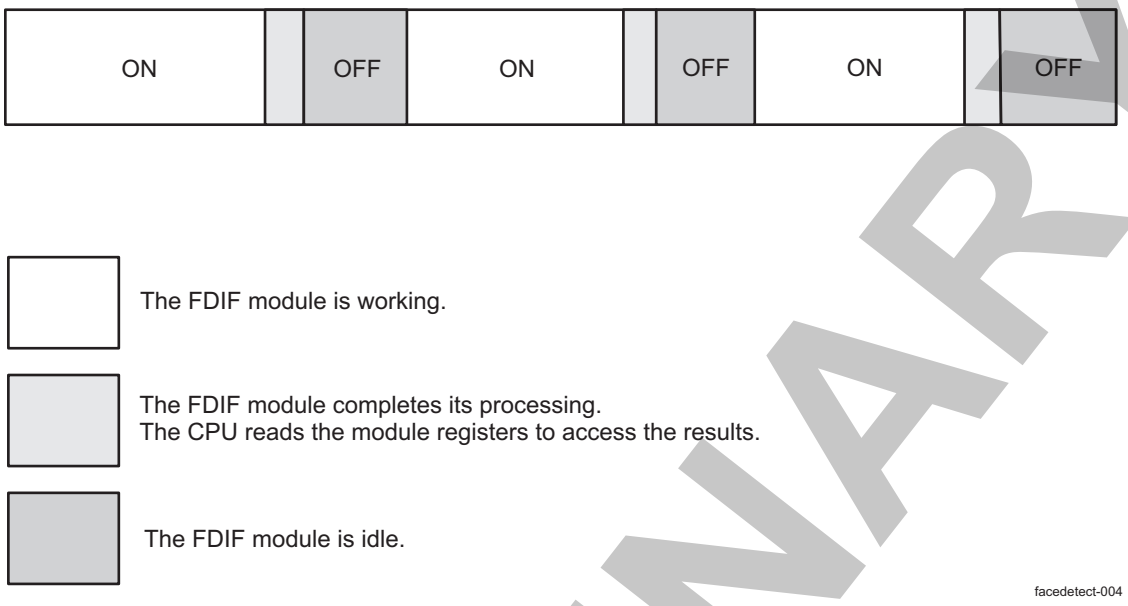
Figure 9-4. FDIF Power-Management Transitions



9.3.3.2.1.1 Normal Mode to Idle Mode

Software sets the FDIF_SYSCONFIG[5:4] STANDBYMODE bit field to 0x2 to program the power-management mode.

When its processing completes, the FD core generates the FINISH_IRQ event. At this time the FD_CTRL[1] RUN bit reflects that the FD core is idle.

Software running on the MPU reads the results of the FD algorithm. After software reads the results, it clears the FDIF_IRQSTATUS_RAW_j[8] FINISH_IRQ bit and sets the FDIF_CTRL[5] MSTANDBY bit to 1 to initiate the MStandby signal generation. For more information about the STANDBY and IDLE hardware handshakes, see Section 3.1.1, *Power, Reset, and Clock Management*.

The FDIF clock is gated only when the STANDBY and IDLE protocols are complete.

9.3.3.2.1.2 Idle Mode to Normal Mode

The PRCM module deasserts a signal to the FDIF under software control so that the module can switch back to normal mode. Then, the module functional clock is ensured and stable. Software disables the MStandby signal generation by setting the FDIF_CTRL[5] MSTANDBY bit to 0, and then polls for FDIF_CTRL[6] MSTANDBY_HDSHK = 1 to ensure that the power-management handshaking is complete. For more information about the standby and idle modes, see Section 3.1.1, *Power, Reset, and Clock Management*.

9.3.4 Interrupts and Events

The FDIF has three interrupt lines (FDIF_IRQ1, FDIF_IRQ2, and FDIF_IRQ3) to enable flexibility for controlling the module. Each event can be enabled to only a single interrupt line (that is, to only one interrupt controller [INTC]), because only one interrupt at a time can be active.

Table 9-6 lists the events the FDIF generates. The FDIF_IRQENABLE_SET_j register is used to enable an interrupt, and the FDIF_IRQENABLE_CLR_j register is used to disable an interrupt.

Table 9-6. Interrupts and Events Description

Event Name	Description
FDIF_IRQSTATUS_RAW_j / FDIF_IRQSTATUS_j[8] FINISH_IRQ	This event is generated by the FD IP core. It flags the completion of the processing by the IP.

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Table 9-6. Interrupts and Events Description (continued)

Event Name	Description
FDIF_IRQSTATUS_RAW_j / FDIF_IRQSTATUS_j[0] OCP_ERR_IRQ	This event flags that the L3_MAIN port has received an error.

The FDIF_IRQSTATUS_RAW_j and FDIF_IRQSTATUS_j registers give the interrupt status. The difference between them is that the FDIF_IRQSTATUS_RAW_j register is set even if events are not enabled.

The FDIF_IRQSTATUS_j register can be used to clear events.

9.3.5 Typical Use

Typically, FD processing is applied to buffers provided by the ISP module, already in the correct format.

To enable FD processing, the 32-bit address of the input image in memory must be set up in the FDIF_PICADDR register, and the 32-bit address of the working memory must be set up in the FDIF_WKADDR register.

The detection condition settings can be set with the following registers:

- FD_DCOND
- FD_STARTX
- FD_STARTY
- FD_SIZEX
- FD_SIZEY

For more information, see Section 9.4, *FDIF Programming Guide*.

When the FD_CTRL[1] RUN bit is set to 1, the process starts. When the process completes (FD_CTRL[2] FINISH = 1), the results are available in the following registers:

- FD_DNUM
- FD_CENTERX_i
- FD_CENTERY_i
- FD_CONFSIZE_i
- FD_ANGLE_i

For more information, see Section 9.4, *FDIF Programming Guide*.

9.3.6 Performance Parameters

Table 9-7 lists the register settings that affect performance.

Table 9-7. Performance Parameters

Parameter	Comments
FD_DCOND[1:0] MIN	Sets the minimum face size. The permitted values are 20x20, 25x25, 32x32, and 40x40. A high value leads to higher performance.
FD_DCOND[3:2] DIR	Sets the detection direction setting. The permitted values are UP, RIGHT, and LEFT. The UP value should lead to better performance than RIGHT and LEFT.
FD_LHIT[3:0] LHIT	Sets the detection threshold. The permitted values are in the range from 0 to 9. A low value increases the FD probability detection, but it also increases false detections.

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9.3.7 Error Reporting

Interconnect protocol errors on the FDIF modules slave port are reported usin eror response. Such response is returned when non supported byte enable patterns are used to address the FD core.

Accesses to reserved or unmapped locations in the FDIF memory address range will return 0's for reads, and writes will be ignored. When the master port makes an invalid request, error is returned to the port and FDIF triggers an interrupt(OCP_ERR_IRQ, see Section 9.3.4 Interrupts and Events).

For more information about the logged errors see Section 14.2.3.9 L3_MAIN Interconnect Error Handling and Section 14.3.3.4 L4 Error Detection and Reporting.

NOTE: In case of errors, it is software responsibility to take the appropriate actions.

9.3.8 L3_MAIN Interconnect Parameters

The FDIF is an initiator on the L3_MAIN interconnect. L3 accesses can be configured with the FDIF_CTRL[4:1] MAX_TAGS bit field and the FDIF_CTRL[0] WRNP bit. For more information about these parameters, see Section 14.2.1 *L3 Interconnect*.

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9.4 FDIF Programming Guide

9.4.1 FDIF Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the FDIF.

9.4.1.1 Global Initialization

9.4.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules the first time the FDIF is used after a device reset. This initialization of the surrounding modules is based on the integration of the FDIF. Table 9-8 describes the global initialization of surrounding modules.

For more information, see Section 9.2, *FDIF Integration*.

Table 9-8. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	FDIF_FCLK functional clock must be enabled. See Section 3.6.22, *CD_CAM Clock Domain*, in Section 3.1.1, *Power, Reset, and Clock Management*.
MPU INTC (or IPU INTC or DSP INTC)	The MPU (or IPU or DSP) INTC must be configured to enable the interrupt request generation to the MPU (or IPU or DSP) subsystem when interrupt requests are generated by the FDIF. See the respective Functional Description in Section 17.1, *Interrupt Controller*, for the MPUs Section 17.4.1, Section 17.4.2, and the DSP interrupt request lines in Section 5.1, *DSP Subsystem*, for the DSP.
Interconnect (L3 and L4)	For more information, see Section 14.2.1, *L3 Interconnect*, and Section 14.3.1, *L4 Interconnect*.

9.4.1.1.2 FDIF Global Initialization

9.4.1.1.2.1 Main Sequence – FDIF Global Initialization

Table 9-9 lists the procedure to initialize the FDIF after a poweron or software reset.

Table 9-9. FDIF Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	FDIF_SYSCONFIG[0] SOFTRESET	0x1
Wait until reset is finished.	FDIF_SYSCONFIG[0] SOFTRESET	0x0
Set the maximum interconnect tags.	FDIF_CTRL[4:1] OCP_MAX_TAGS	0xA
Enable ERROR type interrupt.	FDIF_IRQENABLE_SET_j[0] OCP_ERR_IRQ	0x1

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9.4.1.2 FD Operational Modes Configuration

9.4.1.2.1 FD Processing Modes

9.4.1.2.1.1 Main Sequence – FDIF Polling Method

Step	Register/Bit Field/Programming Model	Value
Set image parameters.	See Section 9.4.1.2.1.3, *Subsequence – Set Image Parameters*.	
Request the processing.	FD_CTRL[1] RUN	0x1
Wait until process is finished.	FD_CTRL[2] FINISH	0x1
Read the results.	See Section 9.4.1.2.1.4 *Subsequence - Read the Results*.	

9.4.1.2.1.2 Main Sequence – FDIF Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Set image parameters.	See Section 9.4.1.2.1.3, *Subsequence – Set Image Parameters*.	
Enable FINISH type interrupt.	FDIF_IRQENABLE_SET_j[8] FINISH_IRQ	0x1
Request the processing.	FD_CTRL[1] RUN	0x1

WHEN INTERRUPT OCCURS:

Step	Register/Bit Field/Programming Model	Value
IF: This is FD Process Complete Event?	FDIF_IRQSTATUS_j[8] FINISH_IRQ	0x1
Clear (Disable) FINISH type interrupt.	FDIF_IRQENABLE_CLR_j[8] FINISH IRQ	0x1
Read the results.	See Section 9.4.1.2.1.4, *Subsequence – Read the Results*.	
ELSE		
Clear (Disable) ERROR type interrupt.	FDIF_IRQENABLE_CLR_j[0] OCP_ERR_IRQ	0x1
Perform a software reset.	FDIF_SYSCONFIG[0] SOFTRESET	0x1
For possible errors and the explanations of them, see Section 14.2.1, *Interconnect*.		
ENDIF		

9.4.1.2.1.3 Subsequence – Set Image Parameters

Step	Register/Bit Field/Programming Model	Value
Set input image 32-bit address.	FDIF_PICADDR[31:5] ADDR	0x----
Set working memory 32-bit address.	FDIF_WKADDR[31:5] ADDR	0x----
Set the minimum face size.	FD_DCOND[1:0] MIN	0x-
Set the face direction.	FD_DCOND[3:2] DIR	0x-
Set the horizontal start position of the detection area.	FD_STARTX[7:0] STARTX	0x-
Set the vertical start position of the detection area.	FD_STARTY[6:0] STARTY	0x-
Set the horizontal start size of the detection area.	FD_SIZEX[8:0] SIZEX	0x–
Set the vertical start size of the detection area.	FD_SIZEY[7:0] SIZEY	0x-
Set the detection threshold.	FD_LHIT[3:0] LHIT	0x-

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9.4.1.2.1.4 Subsequence – Read the Results

Step	Register/Bit Field/Programming Model	Value
For each face detected, read the following parameters by processing loop until DNUM = 0:		
Read X_i coordinate	FD_CENTERX_i[8:0] CENTERX	0x–
Read Y_i coordinate	FD_CENTERY_i[7:0] CENTERY	0x-
Read confidence level	FD_CONFSIZE_i[11:8] CONF	0x-
For each face read size_i	FD_CONFSIZE_i[7:0] SIZE	0x-
For each face read the angle	FD_ANGLE_i[8:0] ANGLE	0x-

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9.5 FDIF Register Manual

9.5.1 FDIF Instance Summary

Table 9-10 is the FDIF instance.

Table 9-10. FDIF Instance Summary

Module Name	Base Address	Size
FDIF	0x4A10 A000	4 KiB

9.5.2 FDIF Registers

Table 9-11 summarizes the FDIF register mapping. Table 9-12 through Table 9-56 describe the register bits.

9.5.2.1 FDIF Register Summary

Table 9-11. FDIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	FDIF L4 Base Address
FDIF_REVISION	R	32	0x0000 0000	0x4A10 A000
FDIF_HWINFO	R	32	0x0000 0004	0x4A10 A004
FDIF_SYSCONFIG	RW	32	0x0000 0010	0x4A10 A010
RESERVED	R	32	0x0000 0020	0x4A10 A020
FDIF_IRQSTATUS_RAW_j (1)	RW	32	0x0000 0024 + (0x10 * j)	0x4A10 A024 + (0x10 * j)
FDIF_IRQSTATUS_j (1)	RW	32	0x0000 0028 + (0x10 * j)	0x4A10 A028 + (0x10 * j)
FDIF_IRQENABLE_SET_j (1)	RW	32	0x0000 002C + (0x10 * j)	0x4A10 A02C + (0x10 * j)
FDIF_IRQENABLE_CLR_j (1)	RW	32	0x0000 0030 + (0x10 * j)	0x4A10 A030 + (0x10 * j)
FDIF_PICADDR	RW	32	0x0000 0060	0x4A10 A060
FDIF_CTRL	RW	32	0x0000 0064	0x4A10 A064
FDIF_WKADDR	RW	32	0x0000 0068	0x4A10 A068
FDIF_TESTMON	R	32	0x0000 006C	0x4A10 A06C
FD_CTRL	RW	32	0x0000 0080	0x4A10 A080
FD_DNUM	R	32	0x0000 0084	0x4A10 A084
FD_DCOND	RW	32	0x0000 0088	0x4A10 A088
FD_STARTX	RW	32	0x0000 008C	0x4A10 A08C
FD_STARTY	RW	32	0x0000 0090	0x4A10 A090
FD_SIZEX	RW	32	0x0000 0094	0x4A10 A094
FD_SIZEY	RW	32	0x0000 0098	0x4A10 A098
FD_LHIT	RW	32	0x0000 009C	0x4A10 A09C
FD_CENTERX_i (2)	R	32	0x0000 0160 + (0x10 * i)	0x4A10 A160 + (0x10 * i)
FD_CENTERY_i (2)	R	32	0x0000 0164 + (0x10 * i)	0x4A10 A164 + (0x10 * i)
FD_CONFSIZE_i (2)	R	32	0x0000 0168 + (0x10 * i)	0x4A10 A168 + (0x10 * i)
FD_ANGLE_i (2)	R	32	0x0000 016C + (0x10 * i)	0x4A10 A16C + (0x10 * i)

(1) j = 0 to 2
(2) i = 0 to 34

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9.5.2.2 FDIF Register Description

Table 9-12. FDIF_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A10 A000	**Instance**	FDIF
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision number	R	0x---- ---- TI Internal Data

Table 9-13. Register Call Summary for Register FDIF_REVISION

FDIF Register Manual

- FDIF Register Summary: [0]

Table 9-14. FDIF_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A10 A004	**Instance**	FDIF
Description	Information about the IP module's hardware configuration, that is, typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												FDIF_TAGS			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	FDIF_TAGS	Hardware design value. This bit field reflects the value of the FDIF_TAG generic parameter. 0x0: 1 OCP tag supported 0x1: 2 OCP tags supported [...] 0xF: 16 OCP tags supported	R	0xF

Table 9-15. Register Call Summary for Register FDIF_HWINFO

FDIF Register Manual

- FDIF Register Summary: [0]

Table 9-16. FDIF_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A10 A010	**Instance**	FDIF
Description	Clock management configuration		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		IDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. IP module shall not generate (initiator-related) wake-up events. 0x3: Reserved	RW	0x2
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters idle state. Backup mode, for debug only. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Reserved	RW	0x2
1	RESERVED	Reserved	R	0
0	SOFTRESET	Software reset. Read 0x0: Reset done, no pending action Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing	RW	0

Table 9-17. Register Call Summary for Register FDIF_SYSCONFIG

FDIF Functional Description
- Software Reset: [0] [1]
- System Power Management: [2] [3]
- PRCM Hardware Handshake: [4]

FDIF Programming Guide
- Global Initialization: [5] [6]
- FD Operational Modes Configuration: [7]

FDIF Register Manual
- FDIF Register Summary: [8]
- FDIF Register Description: [9]

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Table 9-18. FDIF_IRQSTATUS_RAW_j

Address Offset	0x0000 0024 + (0x10 * j)		
Physical Address	0x4A10 A024 + (0x10 * j)	**Instance**	FDIF
Description	Per-event raw interrupt status vector, line #n. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							OCP_ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
7:1	RESERVED	Reserved	R	0x00
0	OCP_ERR_IRQ	OCP error received by the master port. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

Table 9-19. Register Call Summary for Register FDIF_IRQSTATUS_RAW_j

FDIF Functional Description
- PRCM Hardware Handshake: [0]
- Interrupts and Events: [1] [2] [3] [4]

FDIF Register Manual
- FDIF Register Summary: [5]

Table 9-20. FDIF_IRQSTATUS_j

Address Offset	0x0000 0028 + (0x10 * j)		
Physical Address	0x4A10 A028 + (0x10 * j)	**Instance**	FDIF
Description	Per-event "enabled" interrupt status vector, line #n. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							OCP_ERR_IRQ

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
7:1	RESERVED	Reserved	R	0x00
0	OCP_ERR_IRQ	OCP error received by the master port. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

Table 9-21. Register Call Summary for Register FDIF_IRQSTATUS_j

FDIF Functional Description • Interrupts and Events: [0] [1] [2] [3]
FDIF Programming Guide • FD Operational Modes Configuration: [4]
FDIF Register Manual • FDIF Register Summary: [5]

Table 9-22. FDIF_IRQENABLE_SET_j

Address Offset	0x0000 002C + (0x10 * j)		
Physical Address	0x4A10 A02C + (0x10 * j)	**Instance**	FDIF
Description	Per-event interrupt enable bit vector, line #n. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							OCP_ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
7:1	RESERVED	Reserved	R	0x00
0	OCP_ERR_IRQ	OCP error received by the master port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

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Table 9-23. Register Call Summary for Register FDIF_IRQENABLE_SET_j

FDIF Functional Description • Interrupts and Events: [0]
FDIF Programming Guide • Global Initialization: [1] • FD Operational Modes Configuration: [2]
FDIF Register Manual • FDIF Register Summary: [3]

Table 9-24. FDIF_IRQENABLE_CLR_j

Address Offset	0x0000 0030 + (0x10 * j)		
Physical Address	0x4A10 A030 + (0x10 * j)	**Instance**	FDIF
Description	Per-event interrupt enable bit vector, line #n. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							OCP_ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
7:1	RESERVED	Reserved	R	0x00
0	OCP_ERR_IRQ	OCP error received by the master port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

Table 9-25. Register Call Summary for Register FDIF_IRQENABLE_CLR_j

FDIF Functional Description • Interrupts and Events: [0]
FDIF Programming Guide • FD Operational Modes Configuration: [1] [2]
FDIF Register Manual • FDIF Register Summary: [3]

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Table 9-26. FDIF_PICADDR

Address Offset	0x0000 0060		
Physical Address	0x4A10 A060	**Instance**	FDIF
Description	Picture data store address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																											RESERVED			

Bits	Field Name	Description	Type	Reset
31:5	ADDR	Picture data store address. The 5 least-significant bits are forced to 0.	RW	0x0000000
4:0	RESERVED	Read returns 0.	R	0x00

Table 9-27. Register Call Summary for Register FDIF_PICADDR

FDIF Functional Description
- Typical Use: [0]

FDIF Programming Guide
- FD Operational Modes Configuration: [1]

FDIF Register Manual
- FDIF Register Summary: [2]

Table 9-28. FDIF_CTRL

Address Offset	0x0000 0064		
Physical Address	0x4A10 A064	**Instance**	FDIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									MSTANDBY_HDSHK	MSTANDBY	OCP_MAX_TAGS				OCP_WRNP

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6	MSTANDBY_HDSHK	MStandby / Wait power-management handshaking status bit The power-management framework of the FDIF module is based on the handshaking of the MSTANDBY and WAIT signals. When going from a idle to normal power-management transition, the software polls for FDIF_CTRL.MSTANDBY_HDSHK = 1 before starting the face detection processing. Read 0x0: Handshaking is not complete. Do not initiate traffic on L3. Read 0x1: Handshaking is complete. Can safely use the FDIF module.	R	0

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Bits	Field Name	Description	Type	Reset
5	MSTANDBY	MStandby signal generation. This bit shall be set to initiate a power-management transition from NORMAL to IDLE or IDLE to NORMAL. 0x0: Write: Clear MStandby signal. One polls FDIF_CTRL.MSTANDBY_HDSHK = 1 after writing this bit to ensure that the power-management handshaking is completed. 0x1: Write: Asserts MStandby signal	RW	1
4:1	OCP_MAX_TAGS	Max OCP tags. This bit field sets the maximum number of interconnect tags that the module shall use. This number is programmable between 1 (MAX_TAGS = 0) and FDIF_TAGS (MAX_TAGS = FDIF_TAGS – 1). The value of MAX_TAGS is reflected in the FIDIF_HWINFO register setting. This register setting is expected to have impact on performance. It shall be set once at initialization. Higher value gives more bandwidth to the initiator. Lower value gives less bandwidth to the initiator. This value shall be set as low as possible such that other system initiators are not penalized.	RW	0xF
0	OCP_WRNP	L3 port nonposted write control. Dynamic use of this feature is not supported. This bit shall be set at initialization and not modified hereafter until the processing completes. When nonposted writes are used, tags are used for best performance (MAX_TAGS > 1). 0x0: All writes are nonposted. 0x1: All writes are posted.	RW	0

Table 9-29. Register Call Summary for Register FDIF_CTRL

FDIF Functional Description • PRCM Hardware Handshake: [0] [1] [2] • L3 Interconnect Parameters: [3] [4]
FDIF Programming Guide • Global Initialization: [5]
FDIF Register Manual • FDIF Register Summary: [6] • FDIF Register Description: [7] [8]

Table 9-30. FDIF_WKADDR

Address Offset	0x0000 0068		
Physical Address	0x4A10 A068	**Instance**	FDIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	Work area address The 5 least-significant bits are forced to 0.	RW	0x0000000
4:0	RESERVED	Read returns 0.	R	0x00

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Table 9-31. Register Call Summary for Register FDIF_WKADDR

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Operational Modes Configuration: [1]
FDIF Register Manual • FDIF Register Summary: [2]

Table 9-32. FDIF_TESTMON

Address Offset	0x0000 006C		
Physical Address	0x4A10 A06C	**Instance**	FDIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TEST_MONITOR							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Read returns 0s	R	0x0000000
12:0	TEST_MONITOR	0x1000 = idle 0x0006 = waiting for memory	R	0x1000

Table 9-33. Register Call Summary for Register FDIF_TESTMON

FDIF Register Manual • FDIF Register Summary: [0]

Table 9-34. FD_CTRL

Address Offset	0x0000 0080		
Physical Address	0x4A10 A080	**Instance**	FDIF
Description	Control register Do not set more than two bits to 1 at the same time. Otherwise, operations cannot be guaranteed.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													FINISH	RUN	SRST

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	FINISH	Process Completion Flag Clear 0x0: Write: Read Disable: Process incomplete 0x1: Write: Process complete flag clear Read: Process complete	RW	0
1	RUN	Process Start Request 0x0 Write: Disable 0x0 Read: No processing 0x1 Write: Process start request 0x1 Read: Processing data	RW	0

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Bits	Field Name	Description	Type	Reset
0	SRST	Software Reset This bit shall not be used to reset the FDIF module. Instead, the FDIF_SYSCONFIG[0] SOFTRESET bit shall be used for complete soft reset. 0x0: Write: Disable Read: Reset cancel 0x1: Write: Reset Read: Under reset	RW	0

Table 9-35. Register Call Summary for Register FD_CTRL

FDIF Functional Description • Software Reset: [0] • PRCM Hardware Handshake: [1] • Typical Use: [2] [3]
FDIF Programming Guide • FD Operational Modes Configuration: [4] [5] [6]
FDIF Register Manual • FDIF Register Summary: [7]

Table 9-36. FD_DNUM

Address Offset	0x0000 0084		
Physical Address	0x4A10 A084	**Instance**	FDIF
Description	Face Detection Result Count register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DNUM							

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:0	DNUM	Face detection result count. Up to 35 faces can be detected. Number of faces detected: 0x0: 0 face detected 0x1: 1 face detected 0x2: 2 faces detected [...] 0x23: 35 faces detected 0x24 to 0x3F: unused	R	0x00

Table 9-37. Register Call Summary for Register FD_DNUM

FDIF Functional Description • Typical Use: [0]
FDIF Register Manual • FDIF Register Summary: [1]

Table 9-38. FD_DCOND

Address Offset	0x0000 0088		
Physical Address	0x4A10 A088	**Instance**	FDIF
Description	Detection Condition Setting register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DIR		MIN	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:2	DIR	Detection direction setting: 0x0: Executes only for UP 0x1: Executes only for RIGHT 0x2: Executes only for LEFT 0x3: Reserved	RW	0x0
1:0	MIN	Minimum face size settings: 0x0: Set the minimum face size to 20 pixels. 0x1: Set the minimum face size to 25 pixels. 0x2: Set the minimum face size to 32 pixels. 0x3: Set the minimum face size to 40 pixels.	RW	0x0

Table 9-39. Register Call Summary for Register FD_DCOND

FDIF Functional Description • Typical Use: [0] • Performance Parameters: [1] [2]
FDIF Programming Guide • FD Operational Modes Configuration: [3] [4]
FDIF Register Manual • FDIF Register Summary: [5]

Table 9-40. FD_STARTX

Address Offset	0x0000 008C		
Physical Address	0x4A10 A08C	**Instance**	FDIF
Description	Detection Area Setting register: X Start Coordinate.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STARTX							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STARTX	Starting X coordinates Permitted values are 0<=STARTX<=160. The setting of this register should be completed more than one clock cycle before the processing starts.	RW	0x00

Table 9-41. Register Call Summary for Register FD_STARTX

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Operational Modes Configuration: [1]
FDIF Register Manual • FDIF Register Summary: [2]

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Table 9-42. FD_STARTY

Address Offset	0x0000 0090		
Physical Address	0x4A10 A090	**Instance**	FDIF
Description	Detection Area Setting Register: Y Start Coordinate.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STARTY							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	STARTY	Starting Y coordinates Permitted values are 0 <= STARTY <= 120. The setting of this register should be completed more than one clock cycle before the processing starts.	RW	0x00

Table 9-43. Register Call Summary for Register FD_STARTY

FDIF Functional Description
- Typical Use: [0]

FDIF Programming Guide
- FD Operational Modes Configuration: [1]

FDIF Register Manual
- FDIF Register Summary: [2]

Table 9-44. FD_SIZEX

Address Offset	0x0000 0094		
Physical Address	0x4A10 A094	**Instance**	FDIF
Description	Detection Area Setting register: X Direction Size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SIZEX							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8:0	SIZEX	X Direction Size. When neither 160 ≤ SIZEX ≤ 320 nor STARTX + SIZEX ≤ 320 is met, operation cannot be guaranteed. The setting of this register should be completed more than one clock cycle before the processing starts.	RW	0x140

Table 9-45. Register Call Summary for Register FD_SIZEX

FDIF Functional Description
- Typical Use: [0]

FDIF Programming Guide
- FD Operational Modes Configuration: [1]

FDIF Register Manual
- FDIF Register Summary: [2]

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Table 9-46. FD_SIZEY

Address Offset	0x0000 0098		
Physical Address	0x4A10 A098	**Instance**	FDIF
Description	Detection Area Setting register: Y Direction Size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SIZEY							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SIZEY	Y Direction Size. When neither 120 ≤ SIZEY ≤ 240 nor STARTY + SIZEY ≤ 240 is met, operation cannot be guaranteed. The setting of this register should be completed more than one clock cycle before the processing starts.	RW	0xF0

Table 9-47. Register Call Summary for Register FD_SIZEY

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Operational Modes Configuration: [1]
FDIF Register Manual • FDIF Register Summary: [2]

Table 9-48. FD_LHIT

Address Offset	0x0000 009C		
Physical Address	0x4A10 A09C	**Instance**	FDIF
Description	Threshold Setting register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												LHIT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	LHIT	Threshold. Permitted values range from 0x0 to 0x9.	RW	0x5

Table 9-49. Register Call Summary for Register FD_LHIT

FDIF Functional Description • Performance Parameters: [0]
FDIF Programming Guide • FD Operational Modes Configuration: [1]
FDIF Register Manual • FDIF Register Summary: [2]

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Table 9-50. FD_CENTERX_i

Address Offset	0x0000 0160 + (0x10 * i)		
Physical Address	0x4A10 A160 + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: X Coordinate. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CENTERX							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved. Read returns reset value.	R	0x–
8:0	CENTERX	Face position: center X coordinate The coordinates given by (FD_CENTERX_i, FD_CENTERY_i) give the central coordinates of the face position. Permitted values are 0x0 to 0x13F.	R	0x–

Table 9-51. Register Call Summary for Register FD_CENTERX_i

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Operational Modes Configuration: [1]
FDIF Register Manual • FDIF Register Summary: [2] • FDIF Register Description: [3] [4]

Table 9-52. FD_CENTERY_i

Address Offset	0x0000 0164 + (0x10 * i)		
Physical Address	0x4A10 A164 + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: Y Coordinate. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CENTERY							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved. Read returns reset value.	R	0x–
7:0	CENTERY	Face position: center Y coordinate The coordinates given by (FD_CENTERX_i, FD_CENTERY_i) give the central coordinates of the face position. Permitted values are 0x0 to 0xEF.	R	0x–

Table 9-53. Register Call Summary for Register FD_CENTERY_i

FDIF Functional Description • Typical Use: [0]
FDIF Programming Guide • FD Operational Modes Configuration: [1]
FDIF Register Manual • FDIF Register Summary: [2] • FDIF Register Description: [3] [4]

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Table 9-54. FD_CONFSIZE_i

Address Offset	0x0000 0168 + (0x10 * i)		
Physical Address	0x4A10 A168 + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: Confidence Level and Size. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				CONF				SIZE							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved. Read returns reset value.	R	0x-
11:8	CONF	Confidence level: Permitted values range from 0x0 (high) to 0x9 (low)	R	0x-
7:0	SIZE	Detection result face size: Permitted values range from 0x14 to 0xF0	R	0x–

Table 9-55. Register Call Summary for Register FD_CONFSIZE_i

FDIF Functional Description
- Typical Use: [0]

FDIF Programming Guide
- FD Operational Modes Configuration: [1] [2]

FDIF Register Manual
- FDIF Register Summary: [3]

Table 9-56. FD_ANGLE_i

Address Offset	0x0000 016C + (0x10 * i)		
Physical Address	0x4A10 A16C + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: Angle. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ANGLE							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved. Read returns reset value.	R	0x-
8:0	ANGLE	Detection result face angle. Permitted values: When DIR = 0: 0x0 (0 degrees) to 0x1E (30 degrees) and 0x14A (330 degrees) to 0x167 (359 degrees) When DIR = 1: 0x03C (60 degrees) to 0x078 (120 degrees) When DIR = 2: 0x0F0 (240 degrees) to 0x12C (300 degrees)	R	0x–

Table 9-57. Register Call Summary for Register FD_ANGLE_i

FDIF Functional Description
- Typical Use: [0]

FDIF Programming Guide
- FD Operational Modes Configuration: [1]

FDIF Register Manual
- FDIF Register Summary: [2]

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Display Subsystem

This chapter describes the display subsystem for the device.

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10.2 Display Controller 2535
10.3 MIPI Display Serial Interface 2808
10.4 High-Definition Multimedia Interface 2993
10.5 Remote Frame Buffer Interface 2997

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10.1 Display Subsystem Overview

The display subsystem provides the logic to display a video frame from the memory frame buffer on a liquid-crystal display (LCD) panel or TV set.

The display subsystem can display different pictures simultaneously by using three LCD outputs (LCD1, LCD2, and LCD3), in addition to the TV output.

All three LCD outputs can use one of the following interfaces:

- Display serial interface (DSI) (MIPI® DSI)
- Remote frame buffer interface (RFBI) (MIPI DBI 2.0)
- Parallel CMOS output interface (DPI) (MIPI DPI 2.0, BT-656, or BT-1120)

NOTE: Because of device pad multiplexing, some restrictions may apply for simultaneous use of the RFBI and DP

The TV output can be one of the following:

- DPI composite signal
- High-definition multimedia interface (HDMI)

The modules integrated in the display subsystem are:

- Display controller (DISPC):
  - One direct memory access (DMA) engine
  - Three LCD outputs and one TV output, each with a dedicated overlay manager
  - One graphics pipeline (GFX), three video pipelines, and one write-back pipeline
- RFBI:
  - 8-, 9-, 12-, and 16-bit parallel interface
  - Programmable pixel memory formats
  - Programmable output formats on one or multiple cycles per pixel
- Two DSI protocol engines (DSI1_A and DSI1_C):
  - Four data-lane complex input/output (I/O) in addition to the clock lane
  - Bidirectional data link support (only one data lane is used in reverse direction in command mode)
  - Video mode and command mode support
  - Data interleaving support
- HDMI protocol engine:
  - HDMI 1.4 support at 1080p, 60 Hz (including 3D frame-packing support)
  - 36-bit RGB color
  - DES_HDCP 1.4 key protection
  - Deep color mode support (10- or 12-bit for 148.5-MHz pixel clock)

The necessary phase-locked loops (PLLs) with their control modules and the physical layers (PHYs) are outside the display subsystem. The PLLs and PHYs are paired as follows:

- DPLL_HDMI and HDMI_PHY
- DPLL_DSI1_A and DSI_PHY_DSS_A
- DPLL_DSI1_C and DSI_PHY_DSS_C

To ensure efficient bandwidth, the display subsystem integrates a connection between the level 3 (L3_MAIN) interconnect and the DISPC to exchange data with synchronous dynamic random access memory (SDRAM) and memory using the DISPC DMA engine. This connection is also used for configuration.

Figure 10-1 is a high-level diagram of the display subsystem.

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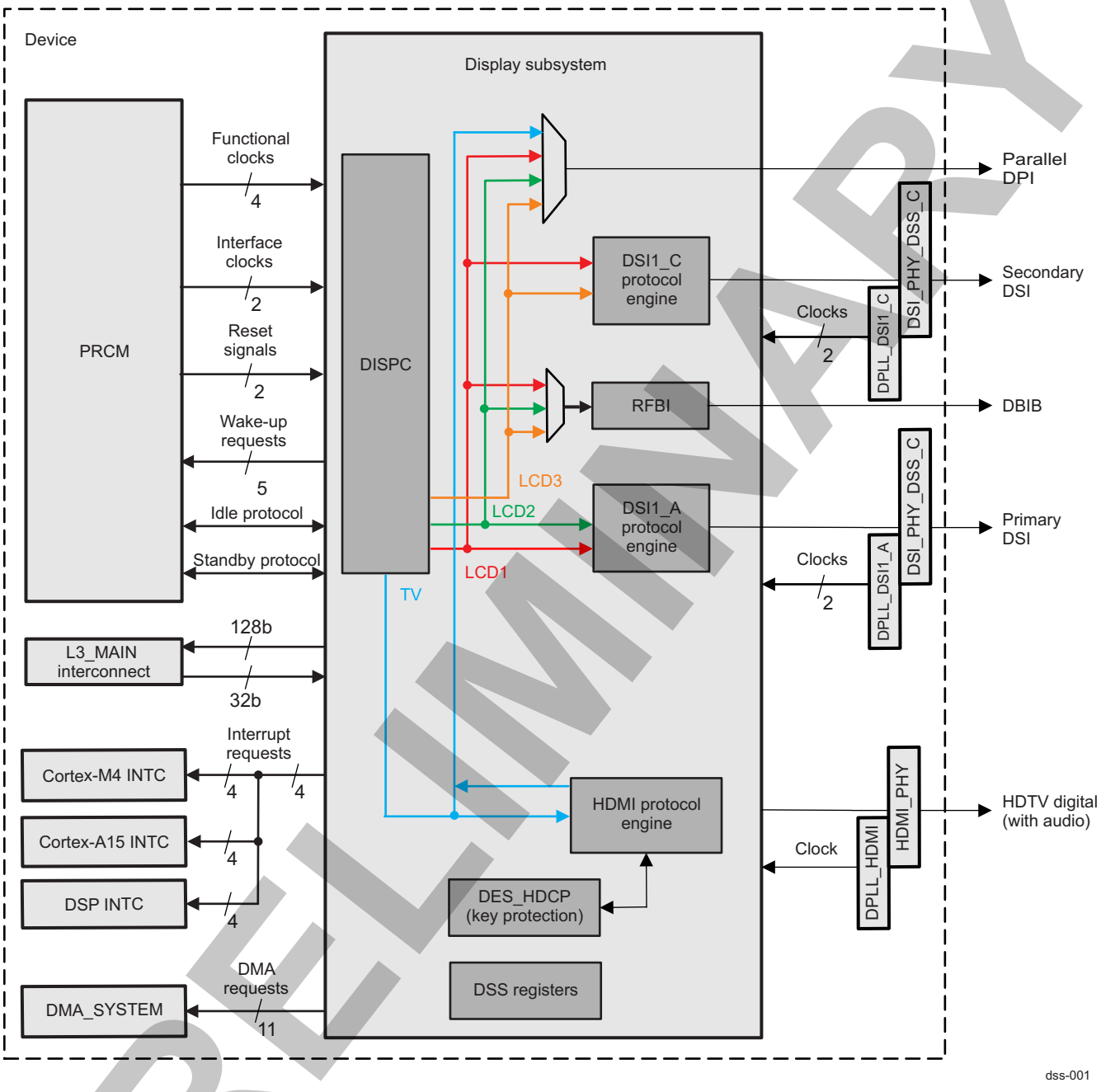
Figure 10-1. Display Subsystem Overview



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10.1.1 Display Subsystem Environment

This section describes the various outputs handled by the display subsystem:

- LCD support
- TV display support

Figure 10-2 is a diagram of the display subsystem environment.

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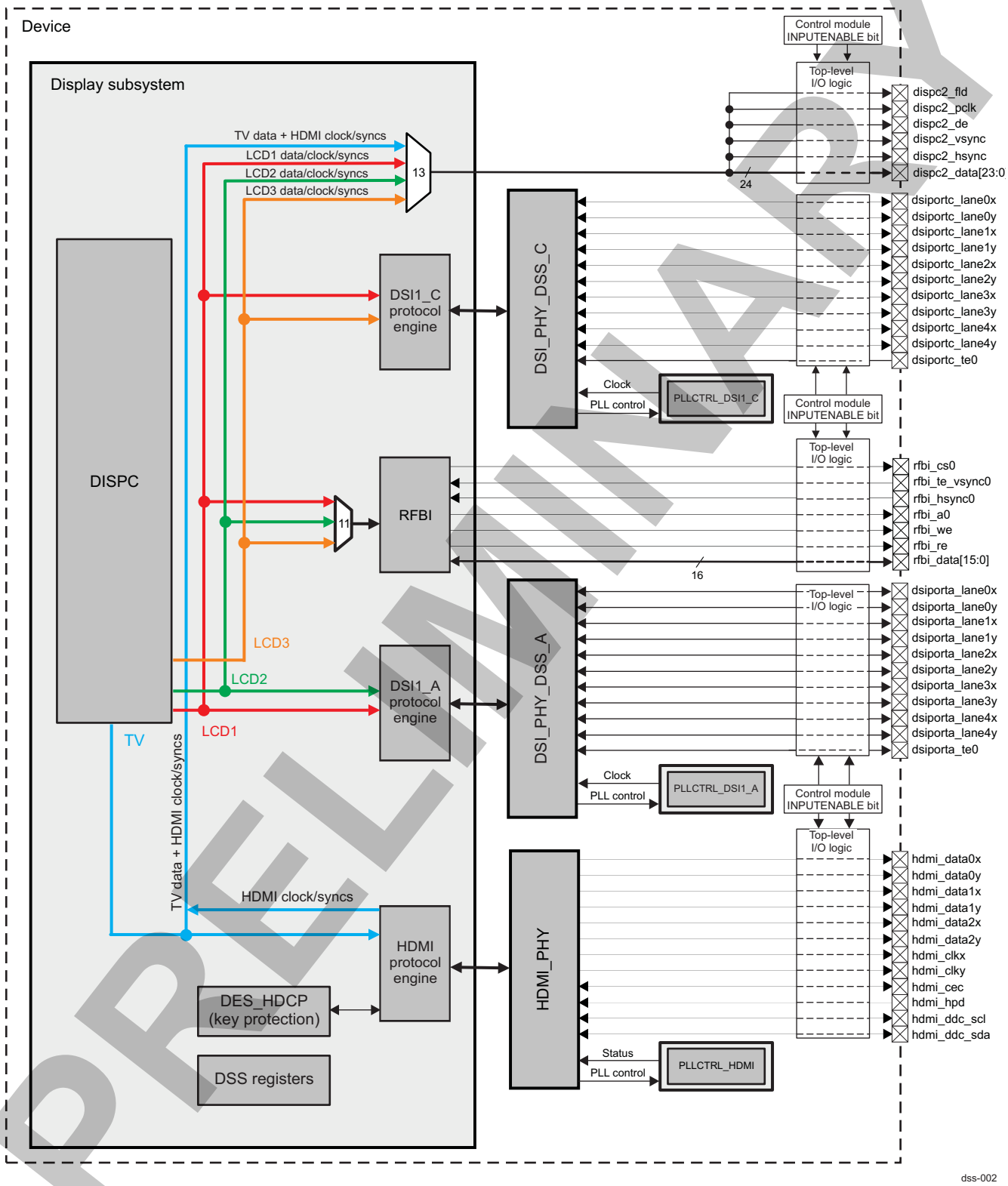
Figure 10-2. Display Subsystem Environment



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NOTE: The path from a module pin to device pad (or pads) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and is programmable in the control module registers and dedicated IP registers. For more information, see , *Pad Functional Multiplexing and Configuration*, and , *Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*.

10.1.1.1 Display Subsystem LCD Support

LCD panels must be connected to the display subsystem of the device using parallel and/or serial interfaces.

10.1.1.1.1 Display Subsystem LCD With Parallel Interfaces

Using parallel output mode, the modules of the display subsystem path are the DISPC and RFBI or DPI.

The DISPC is connected to the memory through the L3_MAIN interconnect and uses its own DMA (with embedded FIFO) to read data from the system memory.

The remote frame buffer (RFB) of the LCD panel is connected directly to the RFBI module of the device. The RFBI controls the reads and writes to and from the RFB. The RFBI receives the output data from the DISPC and generates the signals to control the LCD panel. Through the RFBI, the microprocessor unit (MPU) can send commands or parameter and display data to the LCD panel and directly set the DISPC registers to read or write the data to and from the memory in the LCD panel.

The RFBI can be connected to all LCD outputs of the DISPC, but only one output at a time can be used. The selection (multiplexer 11 in Figure 10-2) is done through the DSS_CTRL[14] RFBI_SWITCH and DSS_CTRL[20] RFBI_SWITCH2 bit. It is not allowed to change the configuration, when the DISPC or RFBI modules are active.

For more details, see DISPC Overview, *Display Controller*, and RFBI Overview, in *Remote Frame Buffer Interface*.

In synchronous parallel interface, the required data and control signals are provided directly to an external MIPI DPI-compatible parallel panel.

All three configuration options for the LCD outputs, LCS1 to LCD3, are available, selected through the DSS_CTRL[17:16] PARALLEL_SEL bit field (multiplexer 13 in Figure 10-2):

Table 10-1 lists the outgoing display subsystem signals on the device boundary pads.

Table 10-1. Display Subsystem LCD Parallel Interface Signals Mapping

Signal Names at Device Pads (See Figure 10-2.)	DSS_CTRL[17:16] PARALLEL_SEL = 1, 2, or 3 DISPC LCDx Channel Out (pixel data, clock, syncs) (where x = 1, 2, or 3)
dispc2_fid	DISPC_LCDx_FID
dispc2_pclk	DISPC_LCDx_PCLK
dispc2_de	DISPC_LCDx_DE
dispc2_vsync	DISPC_LCDx_VSYNC
dispc2_hsync	DISPC_LCDx_HSYNC
dispc2_data[23:0]	DISPC_LCDx_DATA[23:0]

For more details on LCD output pixel data formats for the parallel interface, see DISPC Environment, in *Display Controller*.

10.1.1.1.2 Display Subsystem LCD With Serial Interfaces

In serial interface, the DISPC and the two DSI modules with their associated PLLs are used in the data path. The DISPC is connected to the memory through the L3_MAIN interconnect and uses its own DMA to read the data from the system memory.

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The DSI module contains a PLL to multiply the pixel clock by an appropriate factor. The resulting serialized data is then transmitted on one to four differential data pairs and an additional clock pair that has a reference transition at the boundary between pixels.

For more details, see DSI Overview, in *MIPI Display Serial Interface*.

10.1.1.2 Display Subsystem TV Display Support

When TV data flow is needed from the display subsystem, the DPI or HDMI can be used.

10.1.1.2.1 Display Subsystem TV With Parallel Interfaces

In synchronous parallel interface, the required data is provided from the TV pipeline, and control signals are provided by the HDMI. Then they are merged and provided to the DPI.

This configurations option is available and can be selected through the DSS_CTRL[17:16] PARALLEL_SEL bit field (multiplexer 13 in Figure 10-2):

Table 10-2 lists the outgoing display subsystem signals on the device boundary pads.

Table 10-2. Display Subsystem TV Parallel Interface Signals Mapping

Signal Names at Device Pads (See Figure 10-2.)	**DSS_CTRL[17:16] PARALLEL_SEL = 0 DISPC TV Channel Out (pixel data) HDMI (pixel clock, syncs)**
dispc2_fid	HDMI_M_FID
dispc2_pclk	DSS_HDMI_PCLK
dispc2_de	HDMI_M_DE
dispc2_vsync	HDMI_M_VS
dispc2_hsync	HDMI_M_HS
dispc2_data[23:0]	DISPC_TV_DATA[29:0]

For more details on TV output pixel data formats for the parallel interface, see DISPC Environment, in *Display Controller*.

10.1.1.2.2 Display Subsystem TV With Serial Interfaces

In serial interface, the HDMI is used. The DISPC, HDMI, and DES_HDCP modules and the associated PLL modules are used in the data path. The HDMI module converts the RGB video into standard high-definition digital video format. The module has a PLL, which can multiply the pixel clock by an appropriate factor. The data is transmitted on three differential data pairs and an additional clock pair.

For more details, see HDMI Overview, in *High-Definition Multimedia Interface*.

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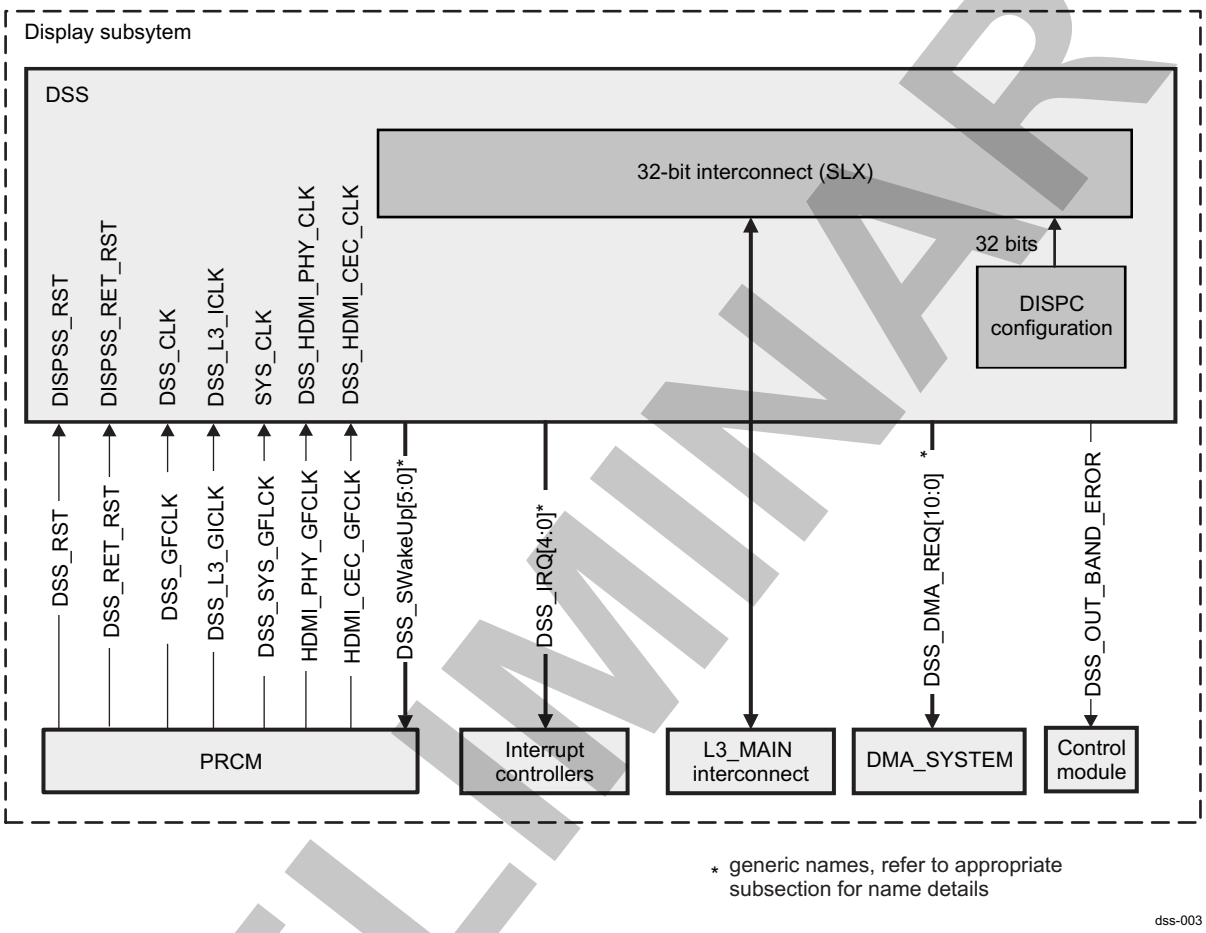
10.1.2 Display Subsystem Integration

This section describes the integration of the display subsystem module in the device, including information about clocks, resets, and hardware requests.

Figure 10-3 shows the integration of the display subsystem in the device.

Figure 10-3. Display Subsystem Integration



10.1.2.1 Display Subsystem Clocks

The power, reset, and clock management (PRCM) module provides clock signals to the display subsystem.

Figure 10-4 shows the details of the display subsystem clock tree.

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Figure 10-4. Display Subsystem Clock Tree

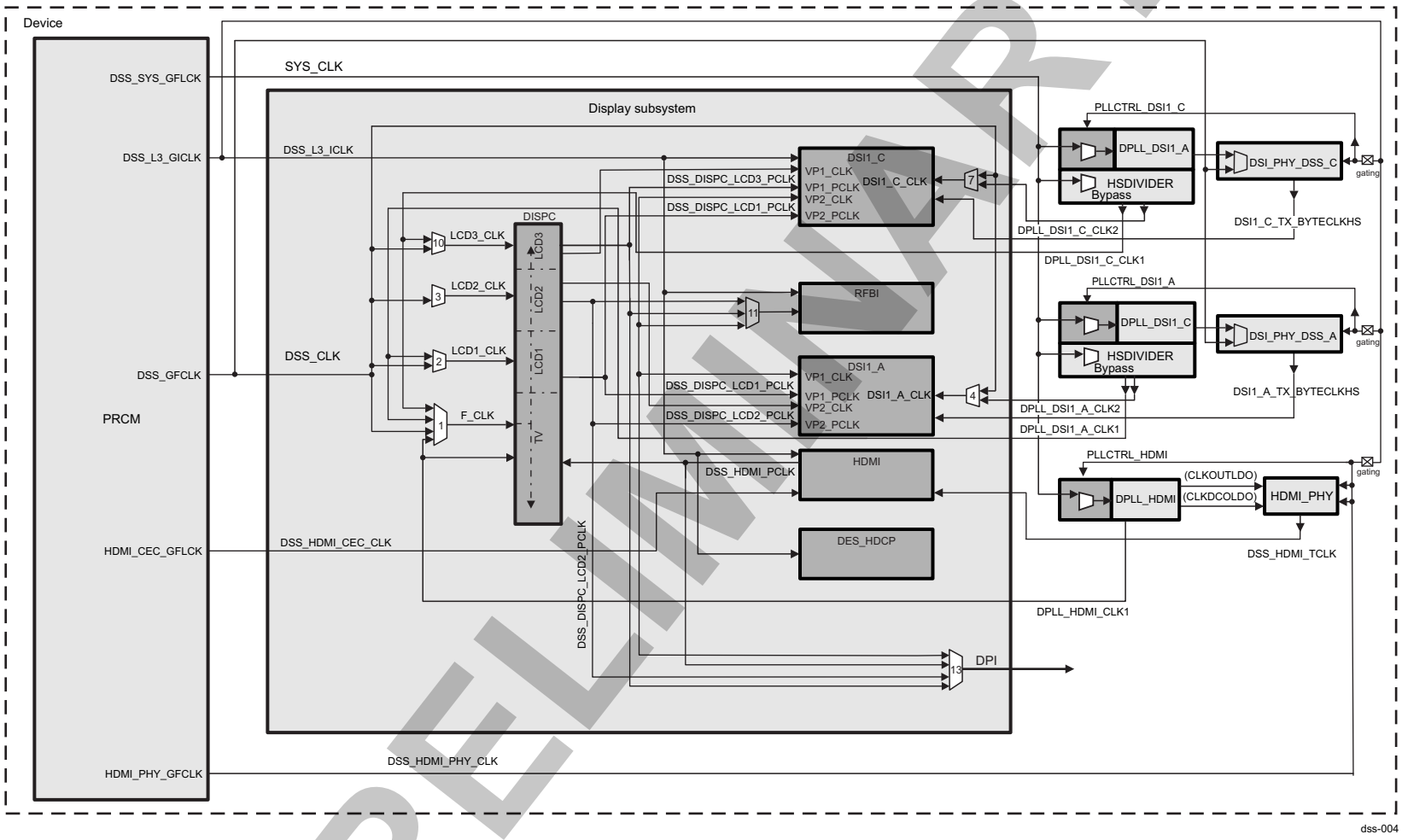

Table 10-3 lists the main DSS clocks and their sources.

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Table 10-3. Display Subsystem Clocks

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DSS	DSS_SYS_GFCLK	SYS_CLK	PRCM module	System clock
	DSS_L3_GICLK	DSS_L3_ICLK	PRCM module	Interface clock
	DSS_GFCLK	DSS_CLK	PRCM module	Main display subsystem functional clock
	HDMI_CEC_GFCLK	DSS_HDMI_CEC_CLK	PRCM module	HDMI core CEC engine clock
	HDMI_PHY_GFCLK	DSS_HDMI_PHY_CLK	PRCM module	HDMI_PHY clock

- The clock source for the L3 interface clock is DSS_L3_ICLK. All clocks can be gated at the PRCM level. See , *Module-Level Clock Management*, in *Chapter 3, Power, Reset and Clock Management*.
- Table 10-4 lists the clock sources for the display subsystem modules.

Table 10-4. Display Subsystem Modules Clock Sources

Destination	Source Signal Name	Source	Multiplexer Number	DSS_CTRL Bit Field
DISPC functional clock (F_CLK) (209.25 MHz at OPP_NOM)	DSS_CLK	PRCM external PER_PLL	1	[9:7] F_CLK_SWITCH
	DPLL_DSI1_A_CLK1	DPLL_DSI1_A		
	DPLL_DSI1_C_CLK1	DPLL_DSI1_C		
	DPLL_HDMI_CLK1	DPLL_HDMI		
DISPC LCD1 functional clock (LCD1_CLK) (209.25 MHz at OPP_NOM)	DSS_CLK	PRCM external PER_PLL	2	[0] LCD1_CLK_SWITCH
	DPLL_DSI1_A_CLK1	DPLL_DSI1_A		
DISPC LCD2 functional clock (LCD2_CLK) (209.25 MHz at OPP_NOM)	DSS_CLK	PRCM external DPLL_PER	3	[12] LCD2_CLK_SWITCH
DISPC LCD3 functional clock (LCD3_CLK) (209.25 MHz at OPP_NOM)	DSS_CLK	PRCM external DPLL_PER	10	[19] LCD3_CLK_SWITCH
	DPLL_DSI1_C_CLK1	DPLL_DSI1_C		
DISPC TV functional clock (186 MHz at OPP_NOM)	DPLL_HDMI_CLK1	DPLL_HDMI	N/A	N/A
DISPC TV pixel clock (186 MHz at OPP_NOM)	DSS_HDMI_PCLK	HDMI	N/A	N/A
DISPC internal functional clock (DISPC_CLK after diveder of F_CLK) (209.25 MHz at OPP_NOM)	F_CLK	DSS	N/A	N/A
DSI1_A protocol engine functional clock (DSI1_A_CLK) (209.25 MHz at OPP_NOM)	DSS_CLK	PRCM external DPLL_PER	4	[1] DSI1_A_CLK_SWITCH
	DPLL_DSI1_A_CLK2	DPLL_DSI1_A		
DSI1_A protocol engine interface clock (209.25 MHz at OPP_NOM)	DSS_L3_ICLK	PRCM external DPLL_CORE	N/A	N/A
DSI1_A protocol engine pixel clock (209.25 MHz at OPP_NOM)	DSS_DISPC_LCD1_PCLK	DISPC	N/A	N/A
DSI1_A protocol engine byte clock (157 MHz at OPP_NOM)	DSI1_A_TX_BYTECLKHS	DPLL_DSI1_A	N/A	N/A
DSI1_C protocol engine functional clock (DSI1_C_CLK) (209.25 MHz at OPP_NOM)	DSS_CLK	PRCM external DPLL_PER	7	[18] DSI1_C_CLK_SWITCH
	DPLL_DSI1_C_CLK2	DPLL_DSI1_C		
DSI1_C protocol engine interface clock (266 MHz at OPP_NOM)	DSS_L3_ICLK	PRCM external DPLL_CORE	N/A	N/A
DSI1_C protocol engine pixel clock (209.25 MHz at OPP_NOM)	DSS_DISPC_LCD3_PCLK	DISPC	N/A	N/A
DSI1_C protocol engine byte clock (157 MHz at OPP_NOM)	DSI1_C_TX_BYTECLKHS	DPLL_DSI1_C	N/A	N/A

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Table 10-4. Display Subsystem Modules Clock Sources (continued)

Destination	Source Signal Name	Source	Multiplexer Number	DSS_CTRL Bit Field
RFBI interface clock (266 MHz at OPP_NOM)	DSS_L3_ICLK	PRCM external DPLL_CORE	N/A	N/A
RFBI functional/pixel clock (209.25 MHz at OPP_NOM)	DSS_DISPC_LCD1_PCLK	DISPC	11	[14] RFBI_SWITCH and [20] RFBI_SWITCH2
	DSS_DISPC_LCD2_PCLK	DISPC		
	DSS_DISPC_LCD2_PCLK	DISPC		
DPI functional/pixel clock (170 MHz at OPP_NOM)	DSS_DISPC_LCD1_PCLK	DISPC	13	[17:16] PARALLEL_SEL
	DSS_DISPC_LCD2_PCLK	DISPC		
	DSS_DISPC_LCD2_PCLK	DISPC		
	DSS_HDMI_PCLK	HDMI		
HDMI timing clock (DSS_HDMI_TCLK) (186 MHz at OPP_NOM)	N/A	HDMI_PHY	N/A	N/A
HDMI PCLK to DISPC (DSS_HDMI_PCLK) (186 MHz at OPP_NOM)	N/A	HDMI	N/A	N/A

NOTE: For more information about the DSI1_A and DSI1_C video port clocks (VPn_PCLK and VPn_CLK, where n = 1 or 2), see Section 10.3.4.2, *DSI Clock Configuration*.

NOTE: 209.25 MHz is provided by DPLL_DSI1_A/ DPLL_DSI1_C, while frequencies provided by PRCM DPLLs have other OPP frequency restrictions. For more details, refer to the respective DPLL setting in the *Device Data Manual*.

10.1.2.2 Display Subsystem Resets

The PRCM module provides two reset signals to the display subsystem.

Figure 10-5 shows the details of the reset tree for the display subsystem.

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Figure 10-5. Display Subsystem Reset Scheme

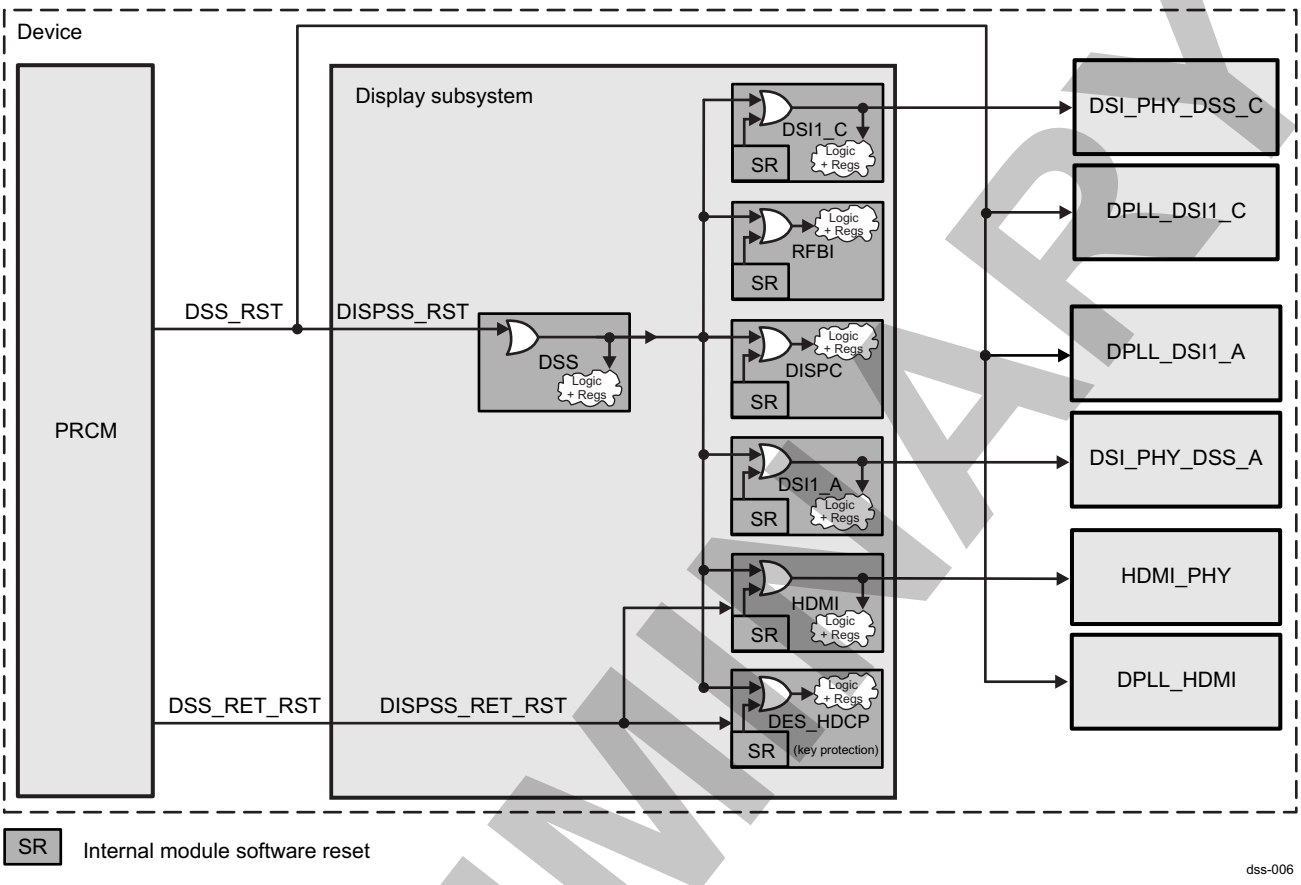

Table 10-5 lists the resets for the display subsystem.

Table 10-5. Display Subsystem Resets

Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DSS	DISPSS_RET_RST	DSS_RET_RST	PRCM module	Retention reset
	DISPSS_RST	DSS_RST	PRCM module	Nonretention reset

The display subsystem receives its DISPSS_RST reset signal (the reset signal of the display subsystem power domain) from the PRCM module. The DISPSS_RET_RST is used only for the DES_HDCP key protection module and HDMI.

10.1.2.3 Display Subsystem Power Management

The display subsystem modules are in the display subsystem power domain.

Table 10-6 lists the power domains in the display subsystem.

Table 10-6. Display Subsystem Power Domains

Module Instance	Attributes
	Power Domain
Display subsystem	PD_DSS
DISPC	For more details, see Section 10.2.1, *DISPC Overview*.
MIPI DSI1_A	For more details, see Section 10.3.1, *DSI Overview*.
MIPI DSI1_C	For more details, see Section 10.3.1, *DSI Overview*.

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Table 10-6. Display Subsystem Power Domains (continued)

Module Instance	Attributes
RFBI	For more details, see Section 10.5.1, *RFBI Overview*.
HDMI	For more details, see Section 10.4.1, *HDMI Overview*.

10.1.2.3.1 Display Subsystem Standby Mode

As part of the system-wide power-management scheme, the display subsystem supports the MStandby/MWait and SIdleReq/SIdleAck protocols:

- MStandby/MWait
  - DISPC
- SIdleReq/SIdleAck
  - DISPC
  - DSI1_A
  - DSI1_C
  - RFBI
  - HDMI
  - DES_HDCP (key protection)
  - DSS interconnect

The PRCM module asserts the MWait and received MStandby directly from DISPC. When the display subsystem initiates a standby procedure, it also initiates a standby/wait handshake protocol with the PRCM module that lets the PRCM module cut the display subsystem clocks. For information about the conditions that allow the subsystem to exit standby mode, see DISPC Overview, in *Display Controller*.

The PRCM also asserts the SIdleReq. Then, it is split at the display subsystem level and sent to the appropriate modules. Consequently, all SIdleAck are merged into one and sent back to the PRCM module.

Figure 10-6 shows the generation of SIdleAck/MStandby in the display subsystem.

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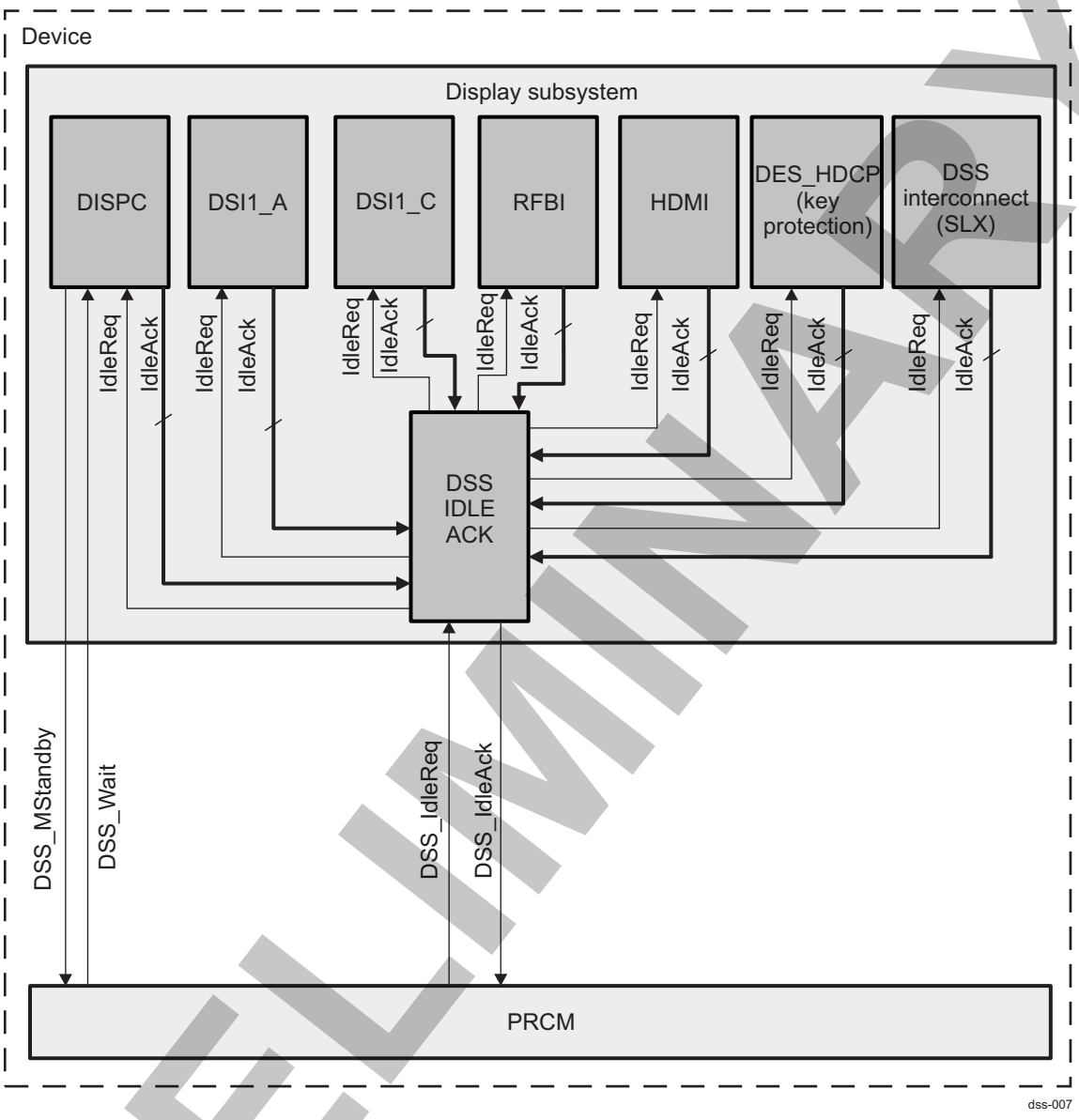
Figure 10-6. Display Subsystem SIdleAck/MStandby Generation



10.1.2.3.2 Display Subsystem Wake-Up Mode

The DISPC, DSI1_A, DSI1_C, and HDMI modules support the wake-up protocol. DSS_HDMI_SWakeUp is associated with DSS_HMDI_IRQ, which is generated by the HDMI module. For the events that generate an SWakeUp and the description and configuration of the registers, see the DISPC, DSI, and HDMI TRM chapters.

Figure 10-7 shows wake-up generation in the display subsystem.

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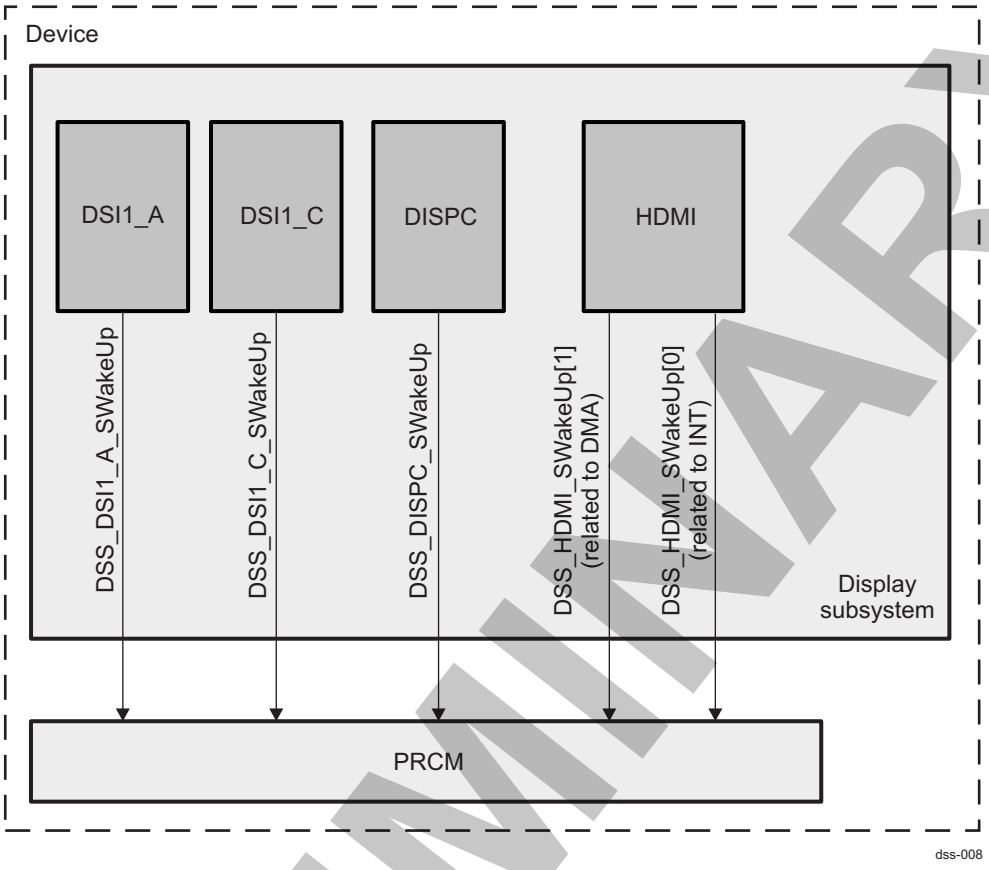
Figure 10-7. Display Subsystem Wake-Up Generation



10.1.2.4 Display Subsystem Interrupt Requests

The display subsystem has four interrupt lines. The interrupt signals are connected to the MPUs and digital signal processor (DSP) interrupt controller (INTC) modules. The interrupts are generated from the DISPC, DSI1_A, DSI1_C, and HDMI.

Figure 10-8 shows interrupt generation in the display subsystem.

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Figure 10-8. Display Subsystem Interrupt Generation

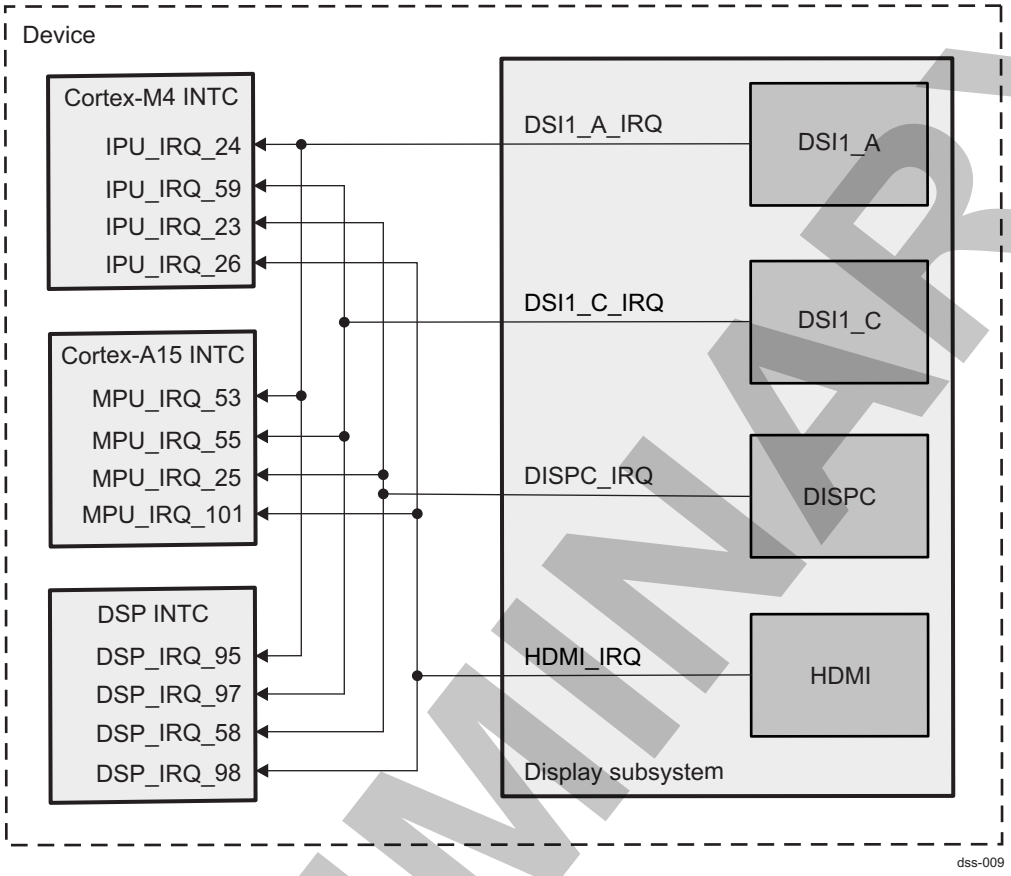

Table 10-7 lists the display subsystem interrupts.

Table 10-7. Display Subsystem Interrupts

		Interrupt Requests		
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DSS				
DISPC	DSS_DISPC_IRQ	DSP_IRQ_58	DSP INTC	DISPC interrupt request
		MPU_IRQ_25	Cortex™-A15 INTC	DISPC interrupt request
		IPU_IRQ_23	Cortex™-M4 INTC	DISPC interrupt request
MIPI DSI1_A	DSI1_A_IRQ	DSP_IRQ_95	DSP INTC	Display DSI1_A interrupt request
		MPU_IRQ_53	Cortex-A15 INTC	Display DSI1_A interrupt request
		IPU_IRQ_24	Cortex-M4 INTC	Display DSI1_A interrupt request
MIPI DSI1_C	DSI1_C_IRQ	DSP_IRQ_97	DSP INTC	Display DSI1_C interrupt request
		MPU_IRQ_55	Cortex-A15 INTC	Display DSI1_C interrupt request
		IPU_IRQ_59	Cortex-M4 INTC	Display DSI1_C interrupt request
HDMI	HDMI_IRQ	DSP_IRQ_98	DSP INTC	Display HDMI interrupt request
		MPU_IRQ_101	Cortex-A15 INTC	Display HDMI interrupt request
		IPU_IRQ_26	Cortex-M4 INTC	Display HDMI interrupt request

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10.1.2.5 Display Subsystem DMA Requests

Eleven DMA requests are connected to the DMA_SYSTEM.

The DMA_SYSTEM requests are:

- Four DMA request signals from each DSI protocol engine (data traffic: from SDRAM or IVA-HD SL2 to DSI protocol engine and from DSI protocol engine to SDRAM or IVA-HD SL2)
- One DMA request signal from RFBI module (data traffic: from SDRAM to RFBI)
- One DMA request signal from HDMI module (audio traffic: from SDRAM or IVA-HD SL2 to HDMI)
- One DMA request signal from DISPC module (used for synchronization of a logical channel in the DMA_SYSTEM for memory-to-memory transfers)

Figure 10-9 shows the details of DMA request generation in the display subsystem.

Figure 10-9. Display Subsystem DMA Request Generation

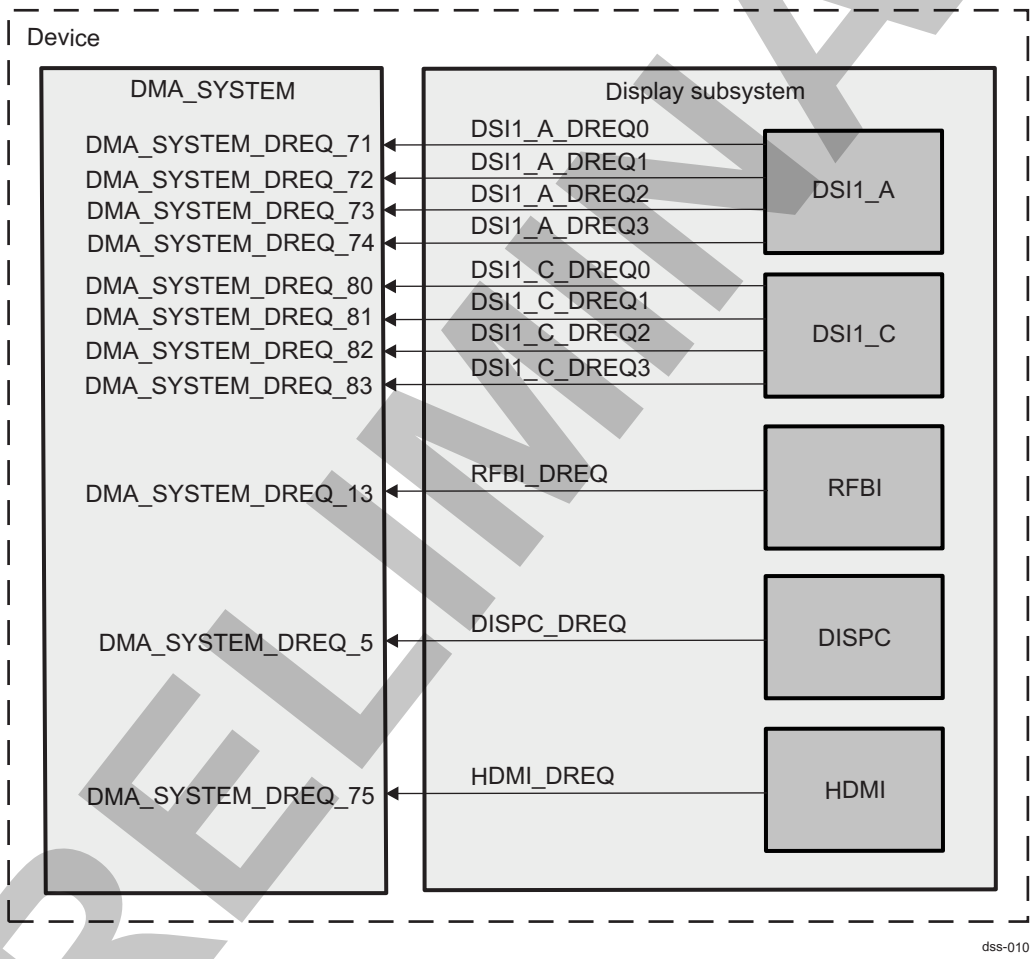

Table 10-8 lists the display subsystem DMA_SYSTEM requests.

Table 10-8. Display Subsystem DMA_SYSTEM Requests

DMA_SYSTEM Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
RFBI	RFBI_DREQ	DMA_SYSTEM_DREQ_13	DMA_SYSTEM	Display subsystem RFBI DMA request
DISPC	DISPC_DREQ	DMA_SYSTEM_DREQ_5	DMA_SYSTEM	The line trigger signal to synchronize a memory-to-memory logical channel in the DMA4 DMA_SYSTEM is generated by the DISPC IP.

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Table 10-8. Display Subsystem DMA_SYSTEM Requests (continued)

MIPI DSI1_A	DSI1_A_DREQ0	DMA_SYSTEM_DREQ_71	DMA_SYSTEM	Display subsystem DSI1_A DMA request 0
	DSI1_A_DREQ1	DMA_SYSTEM_DREQ_72	DMA_SYSTEM	Display subsystem DSI1_A DMA request 1
	DSI1_A_DREQ2	DMA_SYSTEM_DREQ_73	DMA_SYSTEM	Display subsystem DSI1_A DMA request 2
	DSI1_A_DREQ3	DMA_SYSTEM_DREQ_74	DMA_SYSTEM	Display subsystem DSI1_A DMA request 3
MIPI DSI1_C	DSI1_C_DREQ0	DMA_SYSTEM_DREQ_80	DMA_SYSTEM	Display subsystem DSI1_C DMA request 0
	DSI1_C_DREQ1	DMA_SYSTEM_DREQ_81	DMA_SYSTEM	Display subsystem DSI1_C DMA request 1
	DSI1_C_DREQ2	DMA_SYSTEM_DREQ_82	DMA_SYSTEM	Display subsystem DSI1_C DMA request 2
	DSI1_C_DREQ3	DMA_SYSTEM_DREQ_83	DMA_SYSTEM	Display subsystem DSI1_C DMA request 3
HDMI	HDMI_DREQ	DMA_SYSTEM_DREQ_75	DMA_SYSTEM	Display subsystem HDMI audio DMA request

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10.1.3 Display Subsystem Register Manual

10.1.3.1 Display Subsystem Instance Summary

Table 10-9. DSS Instance Summary

Module Name	L3_MAIN Base Address	Size
DSS	0x5800 0000	1 KiB

10.1.3.2 Display Subsystem Registers

10.1.3.2.1 Display Subsystem Registers Mapping Summary

Table 10-10 summarizes the display subsystem register mapping.

Table 10-10. DSS Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address
DSS_REVISION	R	32	0x0000 0000	0x5800 0000
RESERVED	R	32	0x0000 0010	0x5800 0010
DSS_SYSSTATUS	R	32	0x0000 0014	0x5800 0014
DSS_CTRL	RW	32	0x0000 0040	0x5800 0040
DSS_STATUS	R	32	0x0000 005C	0x5800 005C

10.1.3.2.2 Display Subsystem Register Description

Table 10-11 through Table 10-17 describe the register bits.

Table 10-11. DSS_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5800 0000	**Instance**	DSS
Description	This register contains the DSS revision number.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See (1)

(1) TI internal data

Table 10-12. Register Call Summary for Register DSS_REVISION

Display Subsystem Overview
- Display Subsystem Registers Mapping Summary: [0]

Table 10-13. DSS_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5800 0014	**Instance**	DSS
Description	This register provides status information about the module.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is ongoing. Read 0x1: Reset complete	R	0x1

Table 10-14. Register Call Summary for Register DSS_SYSSTATUS

Display Subsystem Overview

- Display Subsystem Registers Mapping Summary: [0]

Table 10-15. DSS_CTRL

Address Offset	0x0000 0040		
Physical Address	0x5800 0040	**Instance**	DSS
Description	This register contains the DSS control bits.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											RFBI_SWITCH2	LCD3_CLK_SWITCH	DSI1_C_CLK_SWITCH	PARALLEL_SEL		RESERVED	RFBI_SWITCH	RESERVED	LCD2_CLK_SWITCH	RESERVED		F_CLK_SWITCH		RESERVED					DSI1_A_CLK_SWITCH	LCD1_CLK_SWITCH

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	RFBI_SWITCH2	Selects the video port 3 from DISPC or select RFBI_SWITCH bit-field If RFBI_SWITCH2 is not set, the video port selectecion is done through the bit-field RFBI_SWITCH 0x0: The video port is selected using only RFBI_SWITCH bit-field. 0x1: Video port 3 (also named third LCD output or LCD3) is selected. The bit-field RFBI_SWITCH is ignored.	RW	0x0
19	LCD3_CLK_SWITCH	DSS_CLK/DPLL_DSI1_C_CLK1 clock switch (multiplexer 10) Selects the clock source for the DISPC LCD3_CLK clock 0x0: DSS_CLK selected (from PRCM) 0x1: DPLL_DSI1_C_CLK1 selected	RW	0x0

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Bits	Field Name	Description	Type	Reset
18	DSI1_C_CLK_SWITCH	DSS_CLK/DPLL14_DSI1_C_CLK2 clock switch (multiplexer 7) Selects the clock source for the DSI1_C functional clock DSI1_C_CLK 0x0: DSS_CLK selected (from PRCM) 0x1: DPLL_DSI1_C_CLK2 selected (from DPLL_DSI1_C)	RW	0x0
17:16	PARALLEL_SEL	Selection between LCD1, LCD2, LCD3 and TV channel out on the parallel output (multiplexer 13) 0x0: Select HDMI channel output. 0x1: Select LCD1 channel output. 0x3: Select LCD3 channel output. 0x2: Select LCD2 channel output.	RW	0x0
15	RESERVED	Reserved	R	0x0
14	RFBI_SWITCH	Selects the video port from DISPC between Video port 1 and Video port 2 (multiplexer 11). If RFBI_SWITCH2 is set, RFBI_SWITCH field is ignored. 0x0: Video port #1 (also named primary LCD output or LCD1) is selected (backward compatible mode) 0x1: Video port #2 (also named secondary LCD output or LCD2) is selected	RW	0x0
13	RESERVED	Reserved	R	0x0
12	LCD2_CLK_SWITCH	DSS_CLK clock switch (multiplexer 3) Selects the clock source for the DISPC LCD2_CLK clock 0x0: DSS_CLK selected (from PRCM) 0x1: Reserved	RW	0x0
11:10	RESERVED	Reserved	RW	0x0
9:7	F_CLK_SWITCH	Selects the clock source for the DISPC functional clock F_CLK 0x0: DSS_CLK selected (from PRCM) 0x1: DPLL_DSI1_A_CLK1 selected (from DPLL_DSI1_A) 0x3: DPLL_HDMI_CLK1 selected (from DPLL_HDMI) 0x4: DPLL_DSI1_C_CLK1 selected (from DPLL_DSI1_C) 0x2: Reserved	RW	0x0
6:2	RESERVED	Reserved	R	0x00
1	DSI1_A_CLK_SWITCH	DSS_CLK/DPLL_DSI1_A_CLK2 clock switch (multiplexer 4) Selects the clock source for the DSI1_A functional clock DSI1_A_CLK 0x0: DSS_CLK selected (from PRCM) 0x1: DPLL_DSI1_A_CLK2 selected (from DSI1_A PLL)	RW	0x0
0	LCD1_CLK_SWITCH	DSS_CLK/DPLL_DSI1_A_CLK1 clock switch (multiplexer 2) Selects the clock source for the DISPC LCD1_CLK clock 0x0: DSS_CLK selected (from PRCM) 0x1: DPLL_DSI1_A_CLK1 selected (from DSI1_A PLL)	RW	0x0

Table 10-16. Register Call Summary for Register DSS_CTRL

Display Subsystem Overview

- Display Subsystem LCD With Parallel Interfaces: [0] [1] [2] [3]
- Display Subsystem TV With Parallel Interfaces: [4] [5]
- Display Subsystem Clocks: [6]
- Display Subsystem Registers Mapping Summary: [7]

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Table 10-17. DSS_STATUS

Address Offset	0x0000 005C		
Physical Address	0x5800 005C	**Instance**	DSS
Description	This register contains the DSS status.		
Type	R		

31 30 29 28 27 26	25 24	23 22	21 20	19 18 17 16	15 14 13	12 11	10 9	8	7 6 5 4 3 2	1 0
RESERVED	LCD3_CLK_STATUS	DSI1_C_CLK_STATUS	RFBI_STATUS	F_CLK_STATUS	RESERVED	LCD2_CLK_STATUS	RESERVED	DSI1_A_CLK_STATUS	RESERVED	LCD1_CLK_STATUS

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved	R	0x00
25:24	LCD3_CLK_STATUS	LCD3_CLK clock selection status (multiplexer 10) indicates which clock is used by the glitch-free mux selecting the source of LCD3_CLK. It is required to have the current clock and the new selected clock being running in order to be able to switch. Both clocks are used at the same time while the switch is ongoing. Read 0x2: DPLL_DSI1_C_CLK1 is used by DISPC as LCD3_CLK clock Read 0x1: DSS_CLK is used as LCD3_CLK Read 0x0: LCD3_CLK clock switch is on-going	R	0x1
23:22	DSI1_C_CLK_STATUS	DSI1_C_CLK clock selection status (multiplexer 4) indicates which clock is used by the glitch-free mux selecting the source of DSI1_C_CLK. It is required to have the current clock and the new selected clock being running in order to be able to switch. Both clocks are used at the same time while the switch is ongoing. Read 0x2: DPLL_DSI1_C_CLK2 is used by DSI1_C as DSI1_C_CLK clock Read 0x1: DSS_CLK is used by DSI1_C as DSI1_C_CLK clock Read 0x0: DSI1_C_CLK clock switch is ongoing	R	0x1
21:20	RFBI_STATUS	Video port selection status (multiplexer 11) Indicates if video port 1 or video 2 from DISPC is used to provide data to the RFBI Read 0x2: Video port 3 (named also third LCD output or LCD3) used to provide data to RFBI Read 0x1: Video port 2 (named also secondary LCD output or LCD2) used to provide data to RFBI Read 0x0: Video port 1 (named also primary LCD output or LCD1) used to provide data to RFBI	R	0x0

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Bits	Field Name	Description	Type	Reset
19:15	F_CLK_STATUS	F_CLK clock selection status (multiplexer 1) indicates which clock is used by the glitch-free mux selecting the source of F_CLK. It is required to have the current clock and the new selected clock being running in order to be able to switch. Both clocks are used at the same time while the switch is ongoing. Read 0x4: Reserved Read 0x2: DPLL_DSI1_A_CLK1 is used by DISPC as F_CLK clock Read 0x0: DSS_CLK clock switch is on-going Read 0x1: DSS_CLK is used by DISPC as F_CLK clock Read 0x8: DPLL_HDMI_CLK1 is used by DISPC as F_CLK clock Read 0x10: DPLL_DSI1_C_CLK1 is used by DISPC as F_CLK clock	R	0x01
14:13	RESERVED	Reserved	R	0x0
12:11	LCD2_CLK_STATUS	LCD2_CLK clock selection status (multiplexer 3) indicates which clock is used by the glitch-free mux selecting the source of LCD2_CLK. It is required to have the current clock and the new selected clock being running in order to be able to switch. Both clocks are used at the same time while the switch is ongoing. Read 0x2: Reserved Read 0x1: DSS_CLK is used as LCD2_CLK Read 0x0: LCD2_CLK clock switch is on-going	R	0x1
10:9	RESERVED	Reserved	R	0x1
8:7	DSI1_A_CLK_STATUS	DSI1_A_CLK clock selection status (multiplexer 4) indicates which clock is used by the glitch-free mux selecting the source of DSI1_A_CLK. It is required to have the current clock and the new selected clock being running in order to be able to switch. Both clocks are used at the same time while the switch is ongoing. Read 0x2: DPLL_DSI1_A_CLK2 is used by DSI1_A as DSI1_A_CLK clock Read 0x1: DSS_CLK is used by DSI1_A as DSI1_A_CLK clock Read 0x0: DSI1_A_CLK clock switch is on-going	R	0x1
6:2	RESERVED	Reserved	R	0x0
1:0	LCD1_CLK_STATUS	LCD1_CLK clock selection status (multiplexer 2) indicates which clock is used by the glitch-free mux selecting the source of LCD1_CLK. It is required to have the current clock and the new selected clock being running in order to be able to switch. Both clocks are used at the same time while the switch is on going. Read 0x2: DPLL_DSI1_A_CLK1 is used by DISPC as LCD1_CLK clock Read 0x1: DSS_CLK is used as LCD1_CLK Read 0x0: LCD1_CLK clock switch is on-going	R	0x1

Table 10-18. Register Call Summary for Register DSS_STATUS

Display Subsystem Overview

- Display Subsystem Registers Mapping Summary: [0]

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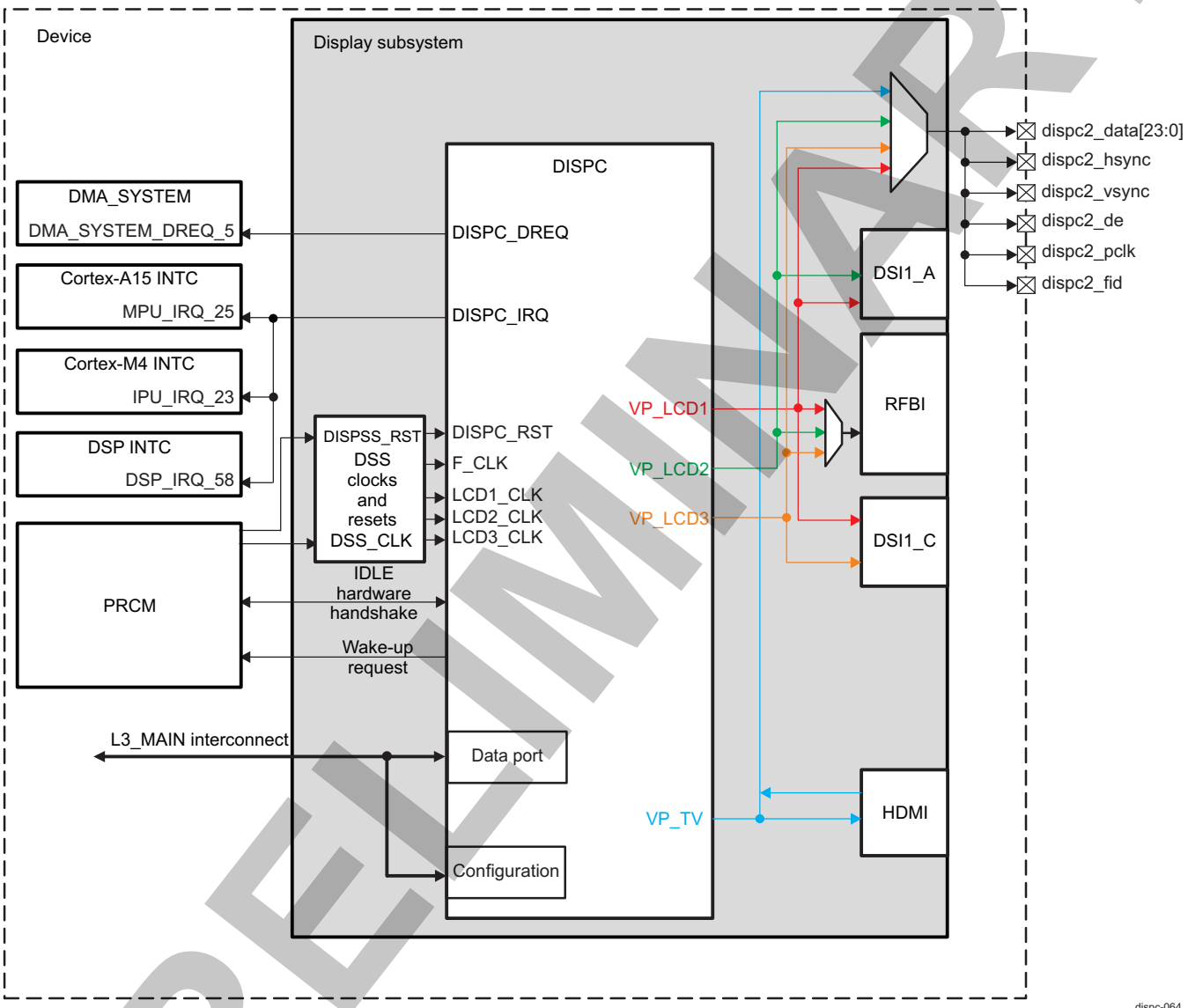
10.2 Display Controller

10.2.1 DISPC Overview

Figure 10-10 shows a block diagram of the display controller (DISPC) within the display subsystem.

Figure 10-10. DISPC Overview



The DISPC includes the following main features:

- Five pipelines for processing:
  - One GFX:
    - Pixel formats: ARGB16-4444, xRGB12-4444, RGBA16-4444, RGBx12-4444, RGB16-565, ARGB16-1555, xRGB16-1555, ARGB32-8888, RGBA32-8888, xRGB32-8888, RGBx32-8888, xRGB24-8888, RGBx24-8888, BGRA32-8888, RGB24-888 (packed), and BITMAP (1 2, 4, or 8 bits per pixel) (where x means that the corresponding bits in the container are not used)
    - Premultiplied ARGB and RGBA formats
    - Selection of the color depth expansion from ARGB16-4444, RGBA16-4444, and ARGB16-1555 to ARGB32-8888, and from xRGB12-4444, RGBx12-4444, and xRGB16-1555 to xRGB32-8888 (replication of the most significant bits [MSBs] or adding 0s)

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- Support for color look-up table (CLUT): 256 × 24-bit entries palette in RGB
- Support for antiflicker on RGB pixel formats using 3-tap filter

– Three video pipelines (VID1, VID2, and VID3):
  - Pixel formats: ARGB16-4444, xRGB12-4444, RGBx12-4444, RGBA12-3333, RGBA16-4444, RGB16-565, ARGB16-1555, xRGB16-1555, ARGB32-8888, RGBA32-8888, xRGB32-8888, RGBx32-8888, RGB24-888, BGRA32-8888, YUV4:2:2-UYVY, YUV4:2:2-YUV2, YUV4:2:0-NV12, and YUV4:2:0-NV21 (where x means that the corresponding bits in the container are not used)
  - Premultiplied ARGB and RGBA formats
  - Selection of the color depth expansion from ARGB16-4444, RGBA16-4444, and ARGB16-1555 to ARGB32-8888, and from xRGB12-4444, RGBx12-4444, and xRGB16-1555 to xRGB32-8888 (replication of the MSBs or adding 0s)
  - Programmable poly-phase filter:
    - Independent horizontal and vertical resampling: Upsampling (up to x8) and downsampling (down to 1/4)
    - Maximum input width of 1920 pixels
    - No limitation on the input height
    - Supported input formats are ARGB32-8888, YUV4:2:2-UYVY, YUV4:2:2-YUV2, YUV4:2:0-NV12, and YUV4:2:0-NV21
    - Alpha blending factor is rescaled like the R, G, and B color components.
  - Programmable color space conversion from YUV4:2:2 (YUV4:4:4, YUV4:2:0 after Chroma upsampling through the scaler) into ARGB32-8888. Images in YUV4:2:2 format with 90- or 270-degree rotation are preprocessed to YUV4:4:4 before the scaler, by duplicating the missing Chroma.
  - Programmable VC-1 range mapping

– One write-back (WB) pipeline: Allows the use of the hardware processing available inside the DISPC, such as color space conversion, rescaling, and compositing to perform memory-to-memory transfer with data processing or capturing a displayed frame
  - Programmable color space conversion RGB24 into YUV4:4:4 or to YUV4:2:2-UYVY, YUV4:2:2-YUV2, YUV4:2:0-NV12, or YUV4:2:0-NV21 using programmable poly-phase filter
  - Programmable color space conversion RGB24 into YUV4:2:2-UYVY, YUV4:2:2-YUV2, YUV4:2:0-NV12, or YUV4:2:0-NV21
  - Selection of the color depth reduction from RGB24 to RGB16
  - Programmable poly-phase filter:
    - Independent horizontal and vertical resampling: Upsampling (up to x8) and downsampling (down to 1/4)
    - Maximum input width of 1920 pixels
    - No limitation on the input height
    - Supported input formats are ARGB32-8888, YUV4:2:2-UYVY, YUV4:2:2-YUV2, YUV4:2:0-NV12, and YUV4:2:0-NV21
    - Alpha blending factor is rescaled like the R, G, and B color components.
  - Selection of the source of the data:
    - Overlay output:
      - Primary LCD output
      - Secondary LCD output
      - Third LCD output
      - TV output
    - Pipelines:
      - Graphic
      - Video 1

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    - Video 2
    - Video 3
- Three LCD outputs: primary (LCD1), secondary (LCD2), and tertiary (LCD3):
  - Input pixel format: ARGB32-8888
  - Output pixel format: RGB24-888 and YUV4:2:2 (YUV4:2:2 only available when Bluetooth mode output is enabled)
  - Overlay of graphic and video for one to four pipelines
  - Source and destination transparency color key
  - Global and pixel alpha blending (up to 8-bit blending factor)
  - Z-order programmable (full flexibility)
  - Displays supported:
    - Active matrix color: 12-, 16-, 18-, and 24-bit panel interface support (replicated or dithered encoded pixel values)
  - Independent programmable timing generators for LCD1, LCD2, and LCD3 to support:

Using DSI1_A interface	WUXGA (1920x1200) @ 60 fps with 24 bpp (VESA timing)
Using RFBI	WVGA @ 30 fps
Using DSI1_C interface	WUXGA (1920x1200) @ 60 fps with 24 bpp (VESA timing)
Using CMOS interface	SXGA VESA timing @ 60 fps, 1080i/720p @ 60 fps CEA-861-D, UXGA @ 60 fps

  - Configurable LCD output mode: progressive or interlace mode
  - Remote frame buffer support through the RFBI module
  - Partial display through the RFBI
  - Multiple-cycle output format on 8-, 9-, 12-, and 16-bit interface time division multiplexing (TDM)
- One TV output:
  - Input pixel format: ARGB40-10.10.10.10
  - Output pixel format: ARGB40-10.10.10.10
  - Overlay of graphic and video for one to four pipelines
  - Source and destination transparency color key
  - Global and pixel alpha blending (up to 10-bit blending factor)
  - Z-order programmable (full flexibility)
  - Slave mode support (no master mode support) with synchronization signals provided by HDMI TX:
    - HSYNC (horizontal synchronization signal)
    - VSYNC (vertical synchronization signal)
    - RE (data request signal)
    - FID (field ID: even and odd field information)
  - RGB30-10.10.10 data bus output for connection to HDMI TX and extended to 36 by duplication of the MSBs
  - HD-1080p, HD-1080i, HD-720p, SD-480p, SD-576p, SD-576i, and SD-480i using HDMI
  - HDMI deep color mode support, 30-bit data output to HDMI encoder
  - Pixel duplication capability (from one pixel clock cycle up to eight cycles)
- Panel support with MIPI DPI protocol:
  - 12-, 16-, 18-, and 24-bit active matrix panel interface support (replicated or dithered encoded pixel values)
- Common:
  - Rotation 0, 90, 180, and 270 degrees using DMM-TILER
  - Synchronized buffer update

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  - Hardware cursor (using the graphics pipeline or one of the video pipelines)
  - Independent gamma curve support on LCDs outputs and TV output
  - Multiple-buffer support
  - Mirroring/flip-flop support (using DMM-TILER)
  - Programmable color phase rotation (CPR)
  - Alpha blending support:
    - Embedded pixel factor (ARGB and RGBA)
    - Global alpha
- DMA (internal to the DISPC):
  - Support for accessing tiled structure through the TILER inside the dynamic memory management (DMM)
  - Support for accessing nontiled structure through the TILER or directly
  - Support for rotation, flip-flop, and mirroring though the TILER inside the DMM
  - Support for memory fragmentation though the TILER inside the DMM
  - Integrated shared buffers between DMA engine and pipelines
  - Programmable buffer thresholds
  - Bandwidth limiter on write request (insertion on idle cycles between requests)
- Advanced:
  - Mode outputting data on display only from the DMA buffer (self-refresh using the DMA FIFO)
  - DMA buffer hand-check in stall mode
  - Arbitration between high and low priority (GFX, VID1, VID2, VID3, and WB pipelines)
- Power modes:
  - Low-power saving modes
  - Support on-the-fly dynamic voltage and frequency scaling (DVFS)
  - Merge capability of the DMA buffers to support greater OFF period on the L3_MAIN interconnect
    - All buffers associated to a single pipeline
    - Reallocation of the buffers of the nonactive pipelines to the active pipelines

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10.2.2 DISPC Environment

The DISPC provides the required control signals to interface directly to an external parallel panel for the MIPI DPI protocol.

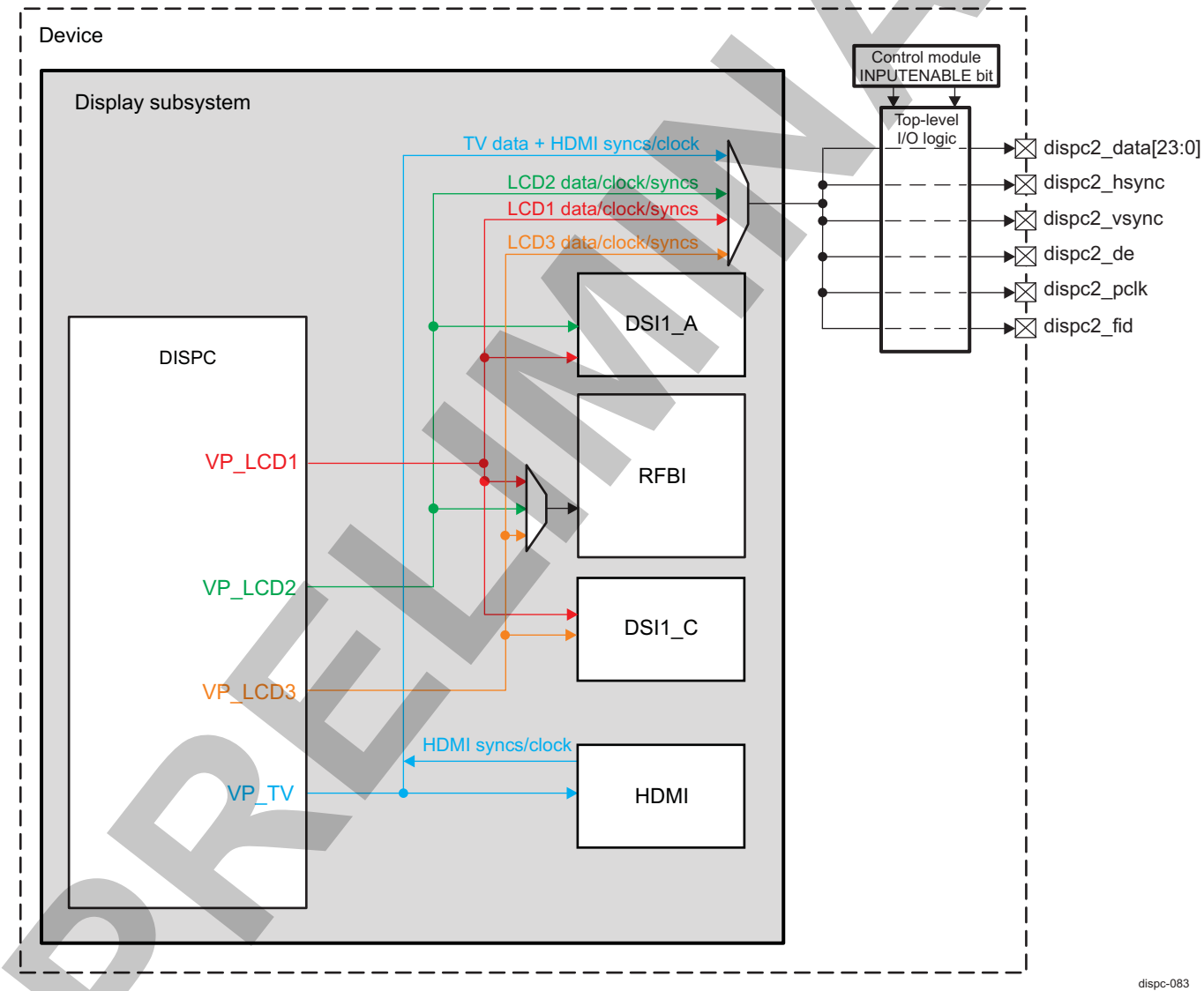
Figure 10-11 shows the LCD support parallel interface.

NOTE: Parallel interface is available through the LCD1, LCD2, LCD3, and TV outputs of the DISPC.

The LCD data and control signals are multiplexed with the TV output data, and control signals are provided by the HDMI module.

The selection can be done at the top level of the display subsystem. For further details and signal mapping, see Section 10.1.1, *Display Subsystem Environment*.

Figure 10-11. DISPC LCD Support Parallel Interface



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NOTE: The path from a module pin to device pad (or pads) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and is programmable in the control module registers and dedicated IP registers. For more information, see , *Pad Functional Multiplexing and Configuration*, and , *Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*.

Table 10-19 describes the interface signals to/from the LCD panel in bypass mode.

Table 10-19. DISPC Parallel Interface Signals

Signal Name	Type[1]	Description
dispc2_data[23:0]	O	Pixel data
dispc2_pclk	O	Pixel clock
dispc2_vsync	O	Vertical synchronization. The LCD frame clock (vsync) toggles after all the lines in a frame are transmitted to the LCD panel and a programmable number of line clock cycles has elapsed at the beginning and end of each frame.
dispc2_hsync	O	Horizontal synchronization. The LCD line clock (hsync) toggles after all pixels in a line are transmitted to the LCD panel and a programmable number of pixel clock wait-states has elapsed at the beginning and end of each line.
dispc2_de	O	In active matrix technology, the DE signal acts as an output-enable signal to indicate when data must be latched using the pixel clock.
dispc2_fid	O	The FID signal indicates the field identifier for the LCD output field: • 0 means even. • 1 means odd.

(1) I = Input, O = Output, I/O = Input/Output

10.2.2.1 DISPC LCD Output and Data Format for the Parallel Interface

This section describes the pixel data bus and shows timing diagrams of transactions and synchronizations.

Figure 10-12 through Figure 10-15 show the pixel data bus, depending on the use of 4-, 8-, 12-, 16-, 18-, or 24-pixel data output pins.

In the Active matrix display type, one pixel per pixel clock is displayed.

Active matrix technology:

Active matrix displays bypass the STN dithering logic block and the output FIFO. Each line represents one pixel.

Figure 10-12 through Figure 10-15 show 12-, 16-, 18-, and 24-active matrix displays, respectively.

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Figure 10-12. DISPC LCD Pixel Data Color12 Active Matrix

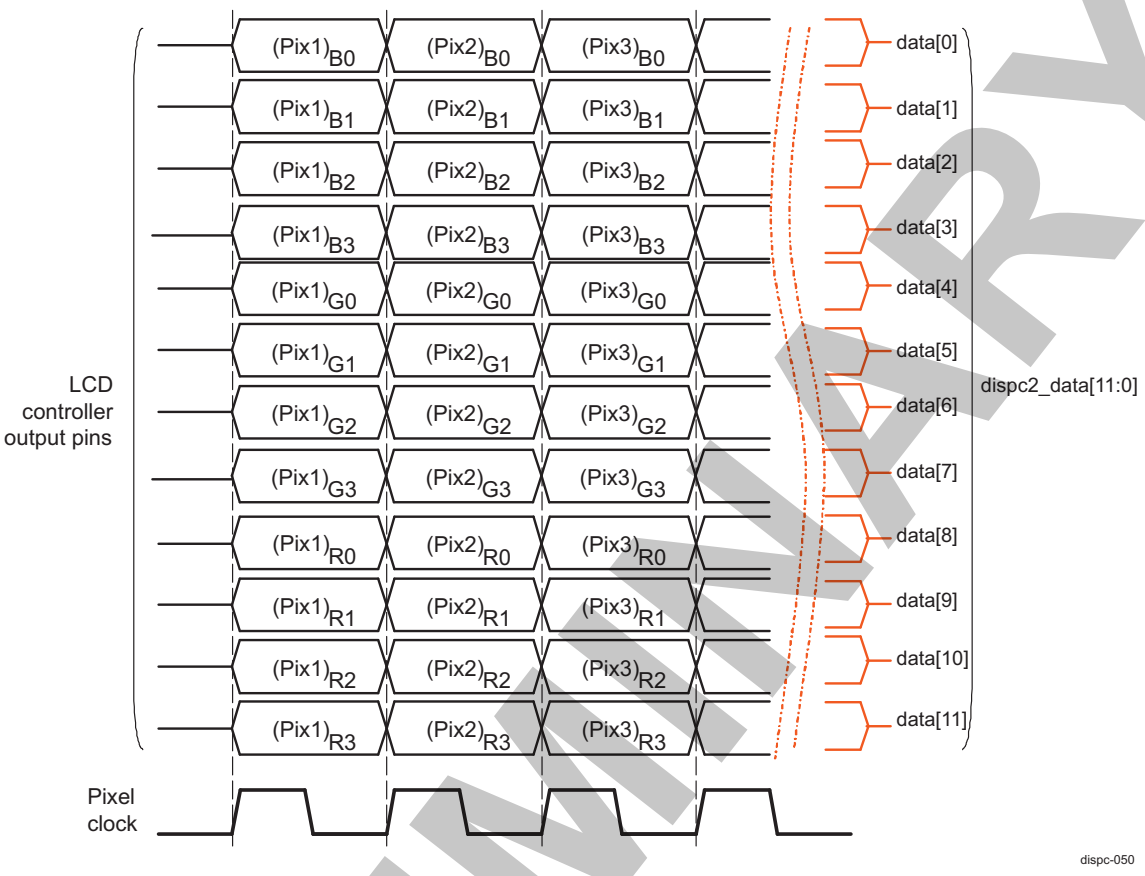

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Figure 10-13. DISPC LCD Pixel Data Color16 Active Matrix

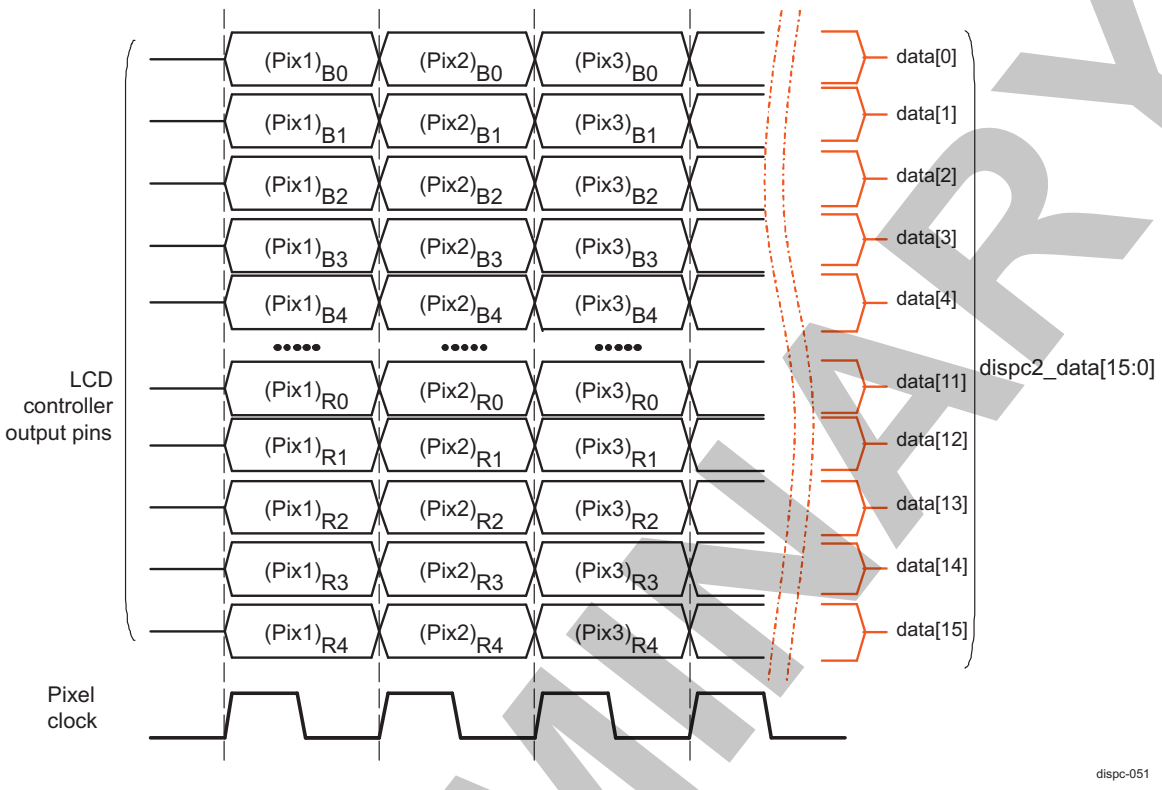

Figure 10-14. DISPC LCD Pixel Data Color18 Active Matrix

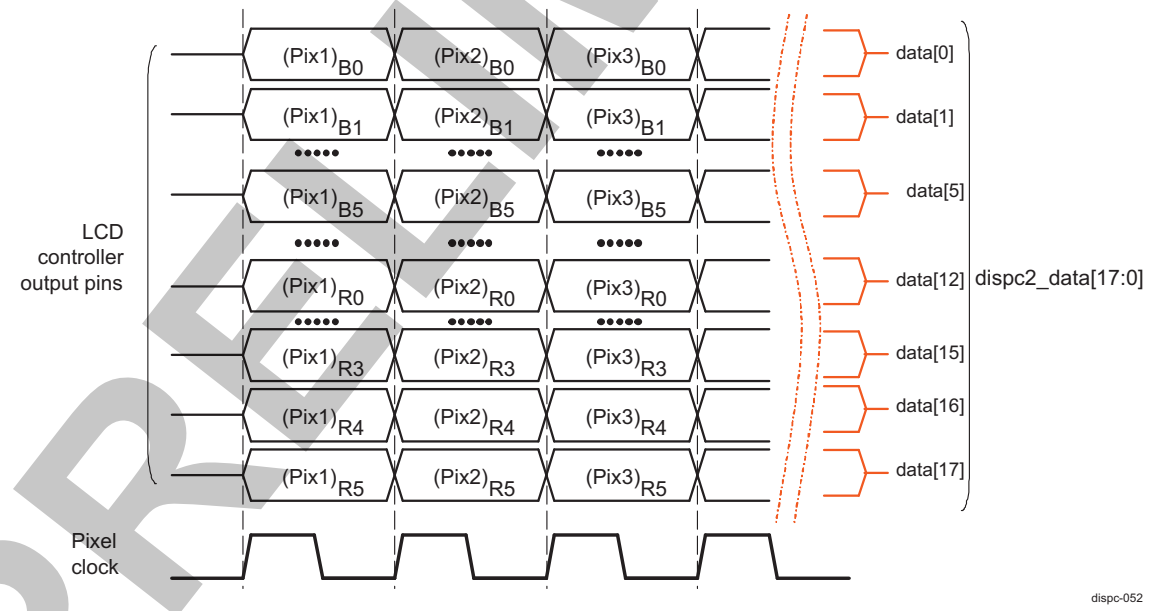

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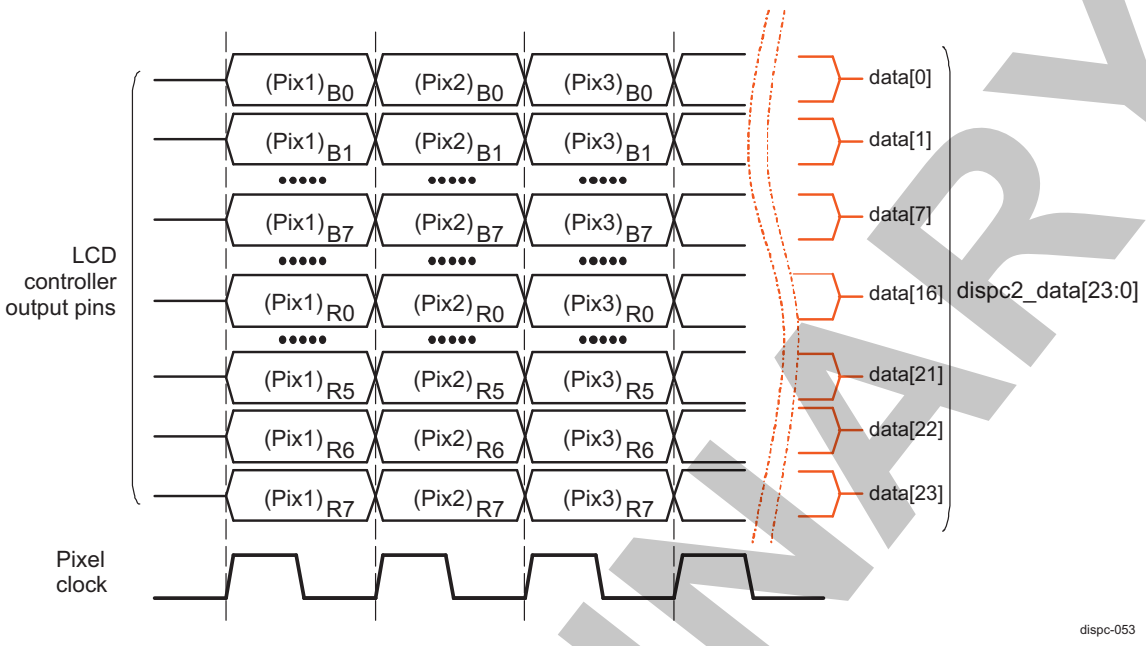
Figure 10-15. DISPC LCD Pixel Data Color24 Active Matrix



10.2.2.2 DISPC Transaction Timing Diagrams

Figure 10-16 through Figure 10-19 show timing diagrams of synchronization signals and pixel clocks for active matrix panels. The DISPC directly drives these signals, which are related to the programmable fields listed in Table 10-20.

Table 10-20. DISPC Programmable Fields in Bypass Mode

Name	Register	Description
PPL	DISPC_SIZE_LCDo[11:0] PPL value + 1	Pixels per line
LPP	DISPC_SIZE_LCDo[27:16] LPP value + 1	Lines per panel
HBP	DISPC_TIMING_Ho[31:20] HBP value + 1	Horizontal back porch
HFP	DISPC_TIMING_Ho[19:8] HFP value + 1	Horizontal front porch
HSW	DISPC_TIMING_Ho[7:0] HSW value + 1	Horizontal synchronization pulse width
VBP	DISPC_TIMING_Vo[31:20] VBP value	Vertical back porch
VFP	DISPC_TIMING_Vo[19:8] VFP value	Vertical front porch
VSW	DISPC_TIMING_Vo[7:0] VSW value + 1	Vertical synchronization pulse width
ONOFF	DISPC_POL_FREQo[17] ONOFF	DISPC_HSYNC and DISPC_VSYNC pixel clock control
RF	DISPC_POL_FREQo[16] RF	DISPC_HSYNC and DISPC_VSYNC pixel clock edge control
IEO	DISPC_POL_FREQo[15] IEO	Invert DISPC_ACBIAS
IPC	DISPC_POL_FREQo[14] IPC	Invert DISPC_PCLK
IHS	DISPC_POL_FREQo[13] IHS	Invert DISPC_HSYNC
IVS	DISPC_POL_FREQo[12] IVS	Invert DISPC_VSYNC

- Active matrix timing configuration 1:
  - DISPC_POL_FREQo[17] ONOFF = 0
  - DISPC_POL_FREQo[16] RF = 0

    The HSYNC and VSYNC signals are driven on the opposite edge of PCLK from the pixel data.
  - DISPC_POL_FREQo[15] IEO = 0

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The DE signal is active high.

– DISPC_POL_FREQo[14] IPC = 0

The pixel data are driven on the rising edge of PCLK.

– DISPC_POL_FREQo[13] IHS = 0

The HSYNC signal is active high.

– DISPC_POL_FREQo[12] IVS = 0

The VSYNC signal is active high.

Figure 10-16. DISPC Active Matrix Timing Diagram of Configuration 1 (Start of Frame)

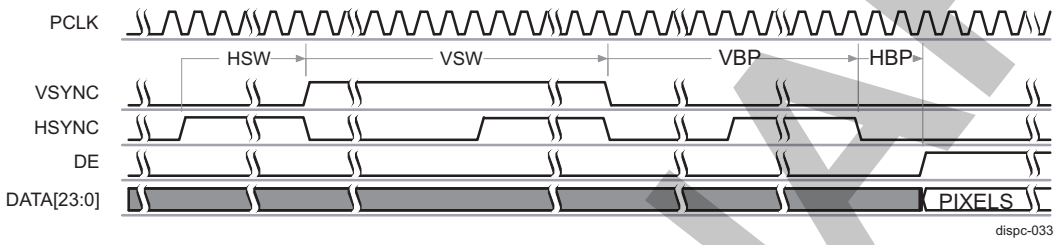


Figure 10-17. DISPC Active Matrix Timing Diagram of Configuration 1 (Between Lines)

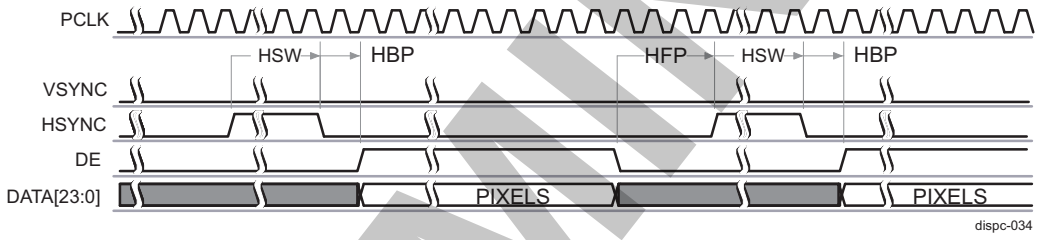


Figure 10-18. DISPC Active Matrix Timing Diagram of Configuration 1 (Between Frames)

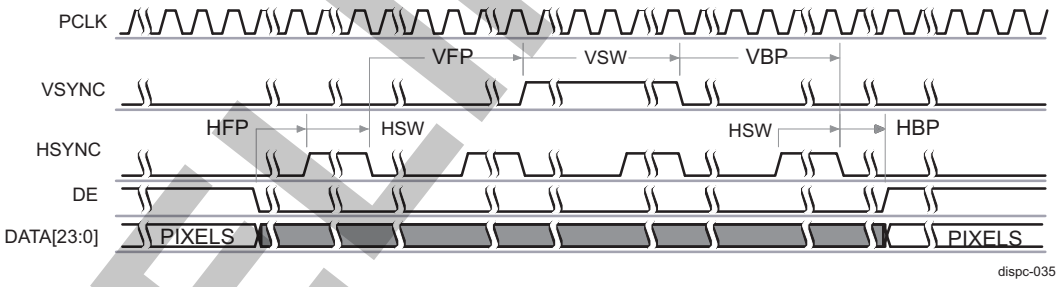
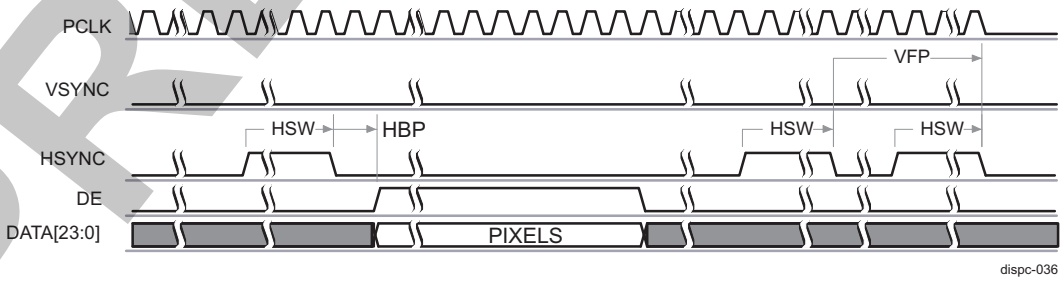


Figure 10-19. DISPC Active Matrix Timing Diagram of Configuration 1 (End of Frame)



- Active matrix timing configuration 2:
  – DISPC_POL_FREQo[17] ONOFF = 1
  – DISPC_POL_FREQo[16] RF = 1

The HSYNC and VSYNC signals are driven on the rising edge of PCLK.

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– DISPC_POL_FREQo[15] IEO = 1
  The DE signal is active low.
– DISPC_POL_FREQo[14] IPC = 1
  The pixel data is driven on the falling edge of PCLK.
– DISPC_POL_FREQo[13] IHS = 1
  The HSYNC signal is active low.
– DISPC_POL_FREQo[12] IVS = 1
  The VSYNC signal is active low.

Figure 10-20. DISPC Active Matrix Timing Diagram of Configuration 2 (Start of Frame)

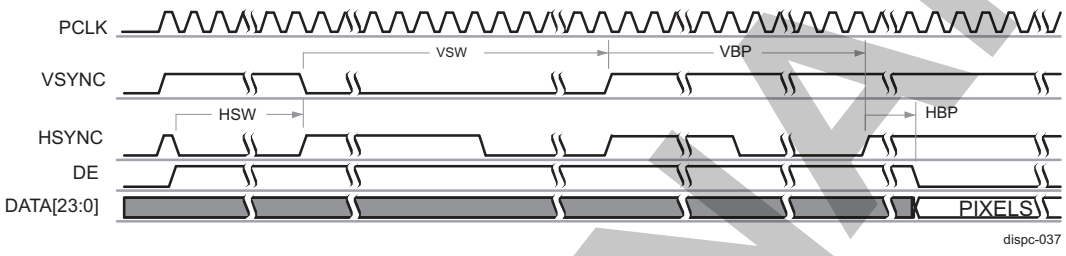


Figure 10-21. DISPC Active Matrix Timing Diagram of Configuration 2 (Between Lines)

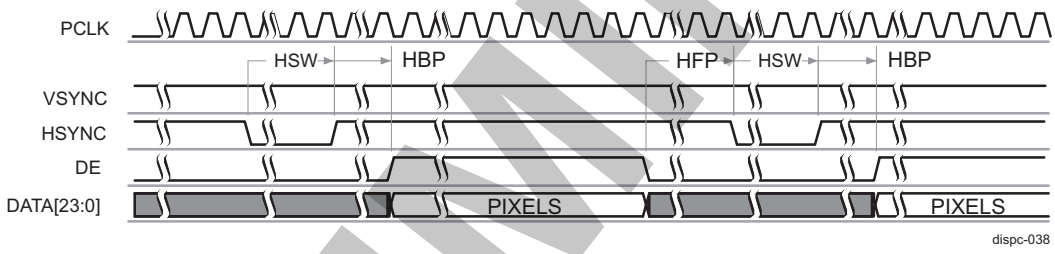


Figure 10-22. DISPC Active Matrix Timing Diagram of Configuration 2 (Between Frames)

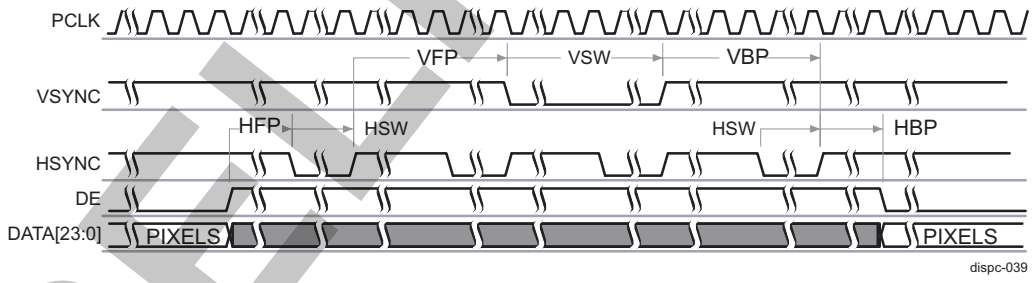
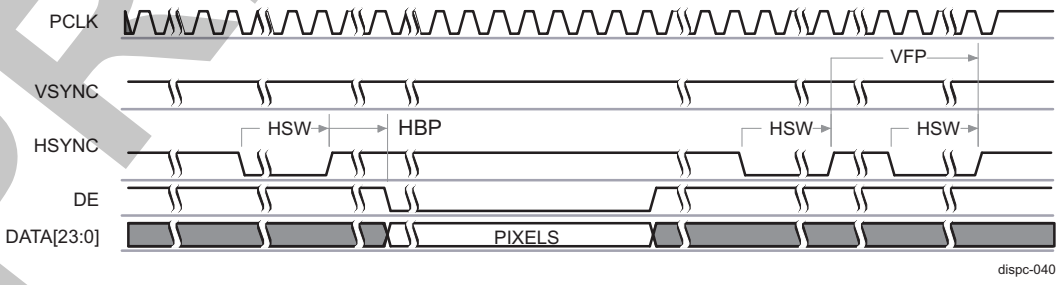


Figure 10-23. DISPC Active Matrix Timing Diagram of Configuration 2 (End of Frame)



- Active matrix timing configuration 3:
  – DISPC_POL_FREQo[17] ONOFF bit = 1
  – DISPC_POL_FREQo[16] RF bit = 1

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The HSYNC and VSYNC signals are driven on the rising edge of PCLK.

– DISPC_POL_FREQo[15] IEO = 0
  The DE signal is active high.
– DISPC_POL_FREQo[14] IPC = 0
  The pixel data are driven on the rising edge of PCLK.
– DISPC_POL_FREQo[13] IHS = 0
  The HSYNC signal is active high.
– DISPC_POL_FREQo[12] IVS = 0
  The VSYNC signal is active high.

Figure 10-24. DISPC Active Matrix Timing Diagram of Configuration 3 (Start of Frame)

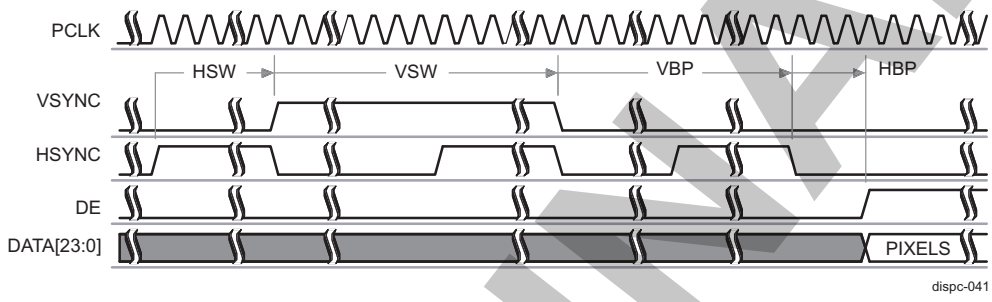

Figure 10-25. DISPC Active Matrix Timing Diagram of Configuration 3 (Between Lines)

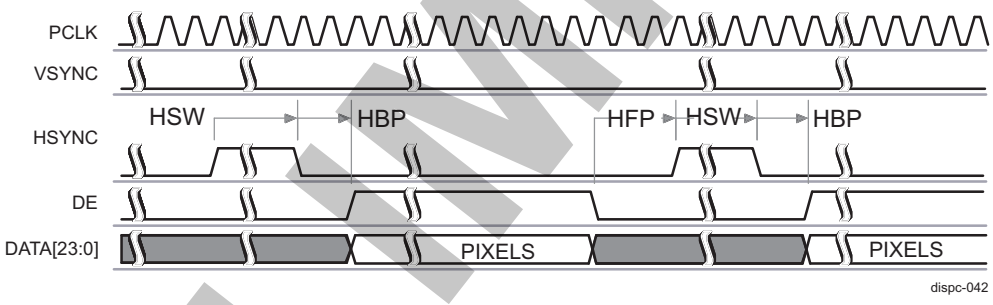

Figure 10-26. DISPC Active Matrix Timing Diagram of Configuration 3 (Between Frames)

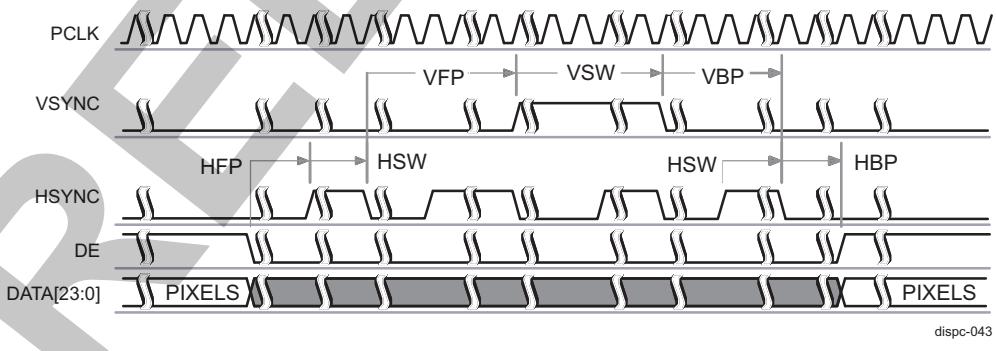

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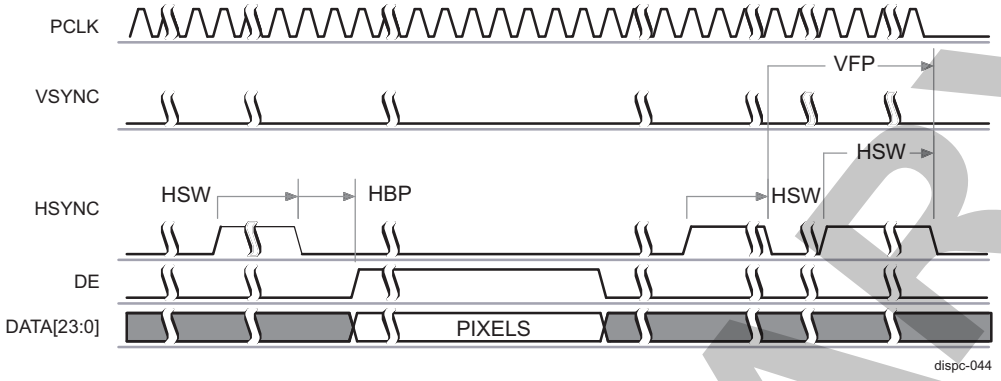
Figure 10-27. DISPC Active Matrix Timing Diagram of Configuration 3 (End of Frame)



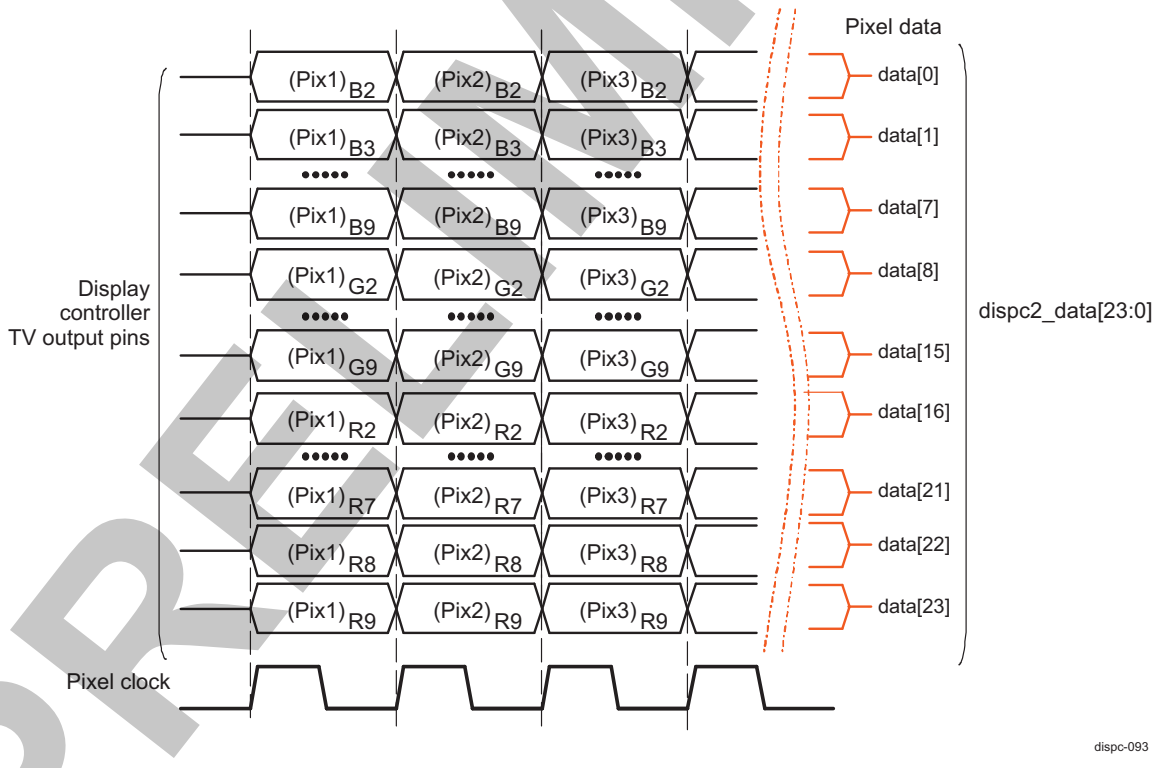
10.2.2.3 DISPC TV Output and Data Format for the Parallel Interface

This section describes the TV output pixel data bus for the parallel interface.

The TV pixel data interface is a 30-bit RGB interface. Only the MSB part of each color component is connected to the display subsystem boundary: R[9:2], G[9:2], B[9:2]. The output of the data is synchronized to the data request signal (HDMI_M_DE) from the HDMI encoder.

Figure 10-28 shows the format of the TV output pixel data.

Figure 10-28. DISPC TV Output Pixel Data



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10.2.3 DISPC Integration

This section describes the DISPC integration in the device (see Figure 10-29). For complete details about clocks and resets, see Section 10.1, *Display Subsystem Overview*.

Figure 10-29. DISPC Integration

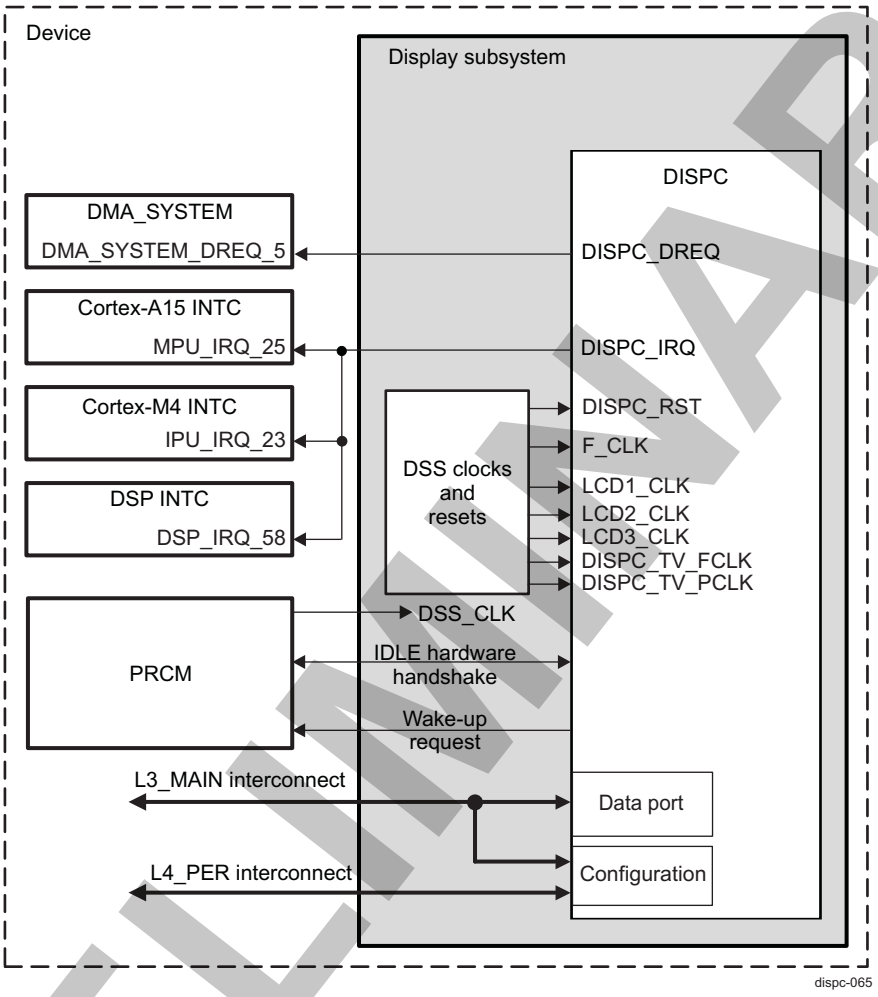

Table 10-21 and Table 10-22 list the integration attributes and clock and resets, respectively.

Table 10-23 summarizes the integration of the module in the device.

Table 10-21. DISPC Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
DISPC	PD_DSS	L3_MAIN for data transfer and configuration

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Table 10-22. DISPC Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DISPC	F_CLK	DSS_CLK, DPLL_DSI1_A_CLK1, DPLL_DSI1_C_CLK1, DPLL_HDMI_CLK1	PRCM, PLLs	Functional clock for the DISPC logic. For the multiplexing description, see Section 10.1.2, *Display Subsystem Integration*.
	LCD1_CLK	DSS_CLK, DPLL_DSI1_A_CLK1	PRCM, DPLL_DSI1_A	Clock used to generate the divided pixel clock for the primary LCD interface. For the multiplexing description, see Section 10.1.2, *Display Subsystem Integration*.
	LCD2_CLK	DSS_CLK	PRCM	Clock used to generate the divided pixel clock for the secondary LCD interface. For the multiplexing description, see Section 10.1.2, *Display Subsystem Integration*.
	LCD3_CLK	DSS_CLK, DPLL_DSI1_C_CLK1	PRCM, DPLL_DSI1_C	Clock used to generate the divided pixel clock for the third LCD interface. For the multiplexing description, see Section 10.1.2, *Display Subsystem Integration*.
	DISPC_TV_FCLK	F_CLK, DPLL_HDMI_CLK1	DSS, DPLL_HDMI	TV functional clock (this is either the F_CLK or a clock driven from the DPLL_HDMI). For the multiplexing description, see Section 10.1.2, *Display Subsystem Integration*.
	DISPC_TV_PCLK	DSS_HDMI_PCLK	HDMI	Pixel clock provided by the HDMI module. For the multiplexing description, see Section 10.1.2, *Display Subsystem Integration*.

Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DISPC	DISPC_RST	DSS_RST	PRCM	Hardware reset is coming from the PRCM module or through a software reset performed at the DSS level. For the tree reset description, see Section 10.1.2, *Display Subsystem Integration*. **NOTE:** The DSS_RST signal is provided to the entire display subystem. When inside the display subsystem boundaries, it is named DISPSS_RST, which on its end is provided to the DISPC and is named DISPC_RST.

Table 10-23. DISPC Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DISPC	DISPC_IRQ	IPU_IRQ_23	Cortex-M4	Display controller interrupt. For information about Cortex-M4 interrupt control, see , *Dual Cortex-M4 IPU Subsystem Overview*.
	DISPC_IRQ	DSP_IRQ_58	DSP	Display controller interrupt. For information about DSP interrupt control, see , *DSP Subsystem Overview*.
	DISPC_IRQ	MPU_IRQ_25	Cortex-A15	Display controller interrupt. For information about Cortex-A15 interrupt control, see , *Dual Cortex-A15 MPU Subsystem Overview*.

DMA_SYSTEM Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**

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Table 10-23. DISPC Hardware Requests (continued)

DISPC	DISPC_DREQ	DMA_SYSTEM_DREQ_5	DMA_SYSTEM	The line trigger signal informs the DMA_SYSTEM that a programmable number of lines is output to the LCD, and that the system memory can be updated. For more details, see Section 10.2.4.5, *DISPC DMA Requests*.

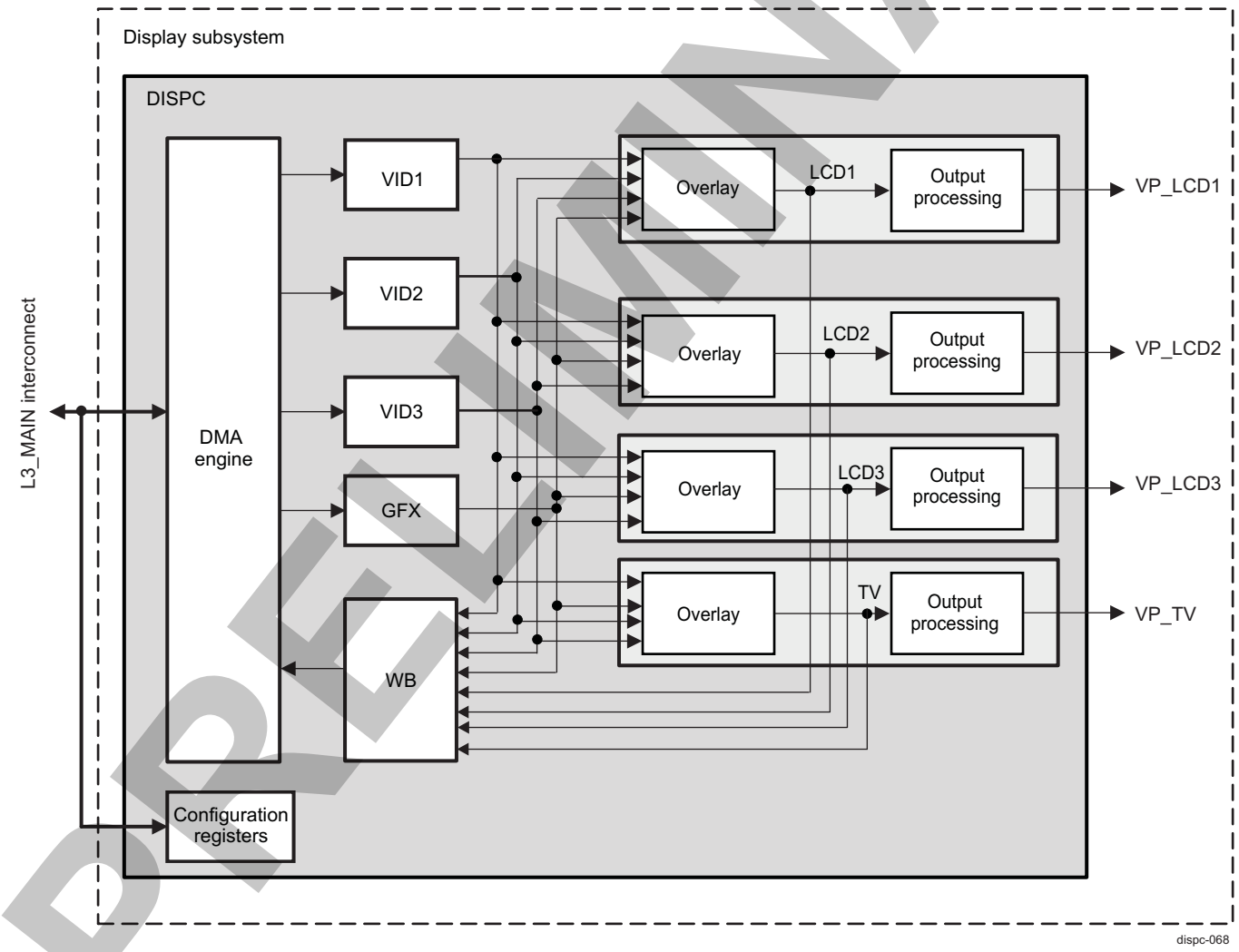
NOTE:

- For a description of interrupt sources, see Section 10.2.4.4, *DISPC Interrupt Requests*.
- For a description of DMA sources, see Section 10.2.4.5, *DISPC DMA Requests*.

10.2.4 DISPC Functional Description

The DISPC can read and display the encoded pixel data stored in memory (see Figure 10-30).

Figure 10-30. DISPC Architecture Overview



The DISPC can read and display the encoded pixel data stored in memory and write the output of one of the overlays or one of the pipelines into system memory.

Several processes can be configured to manage the graphics pipeline (palette, antiflicker) and video pipelines (VC-1, color space conversion, scaling, overlay, transparency, and so forth).

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The data coming out of a pipeline is sent to one of the four outputs, depending on the user configuration. An overlay manager manages inputs of multiple pipelines. User timing configurations for LCD and TV are available.

The DISPC allows the capturing of one output of the pipeline or overlay manager to redirect it into the WB pipeline. It allows the use of the hardware processing available inside the DISPC, such as color space conversion, rescaling, and compositing, and so forth to perform memory-to-memory transfer with data processing.

10.2.4.1 DISPC Clock Configuration

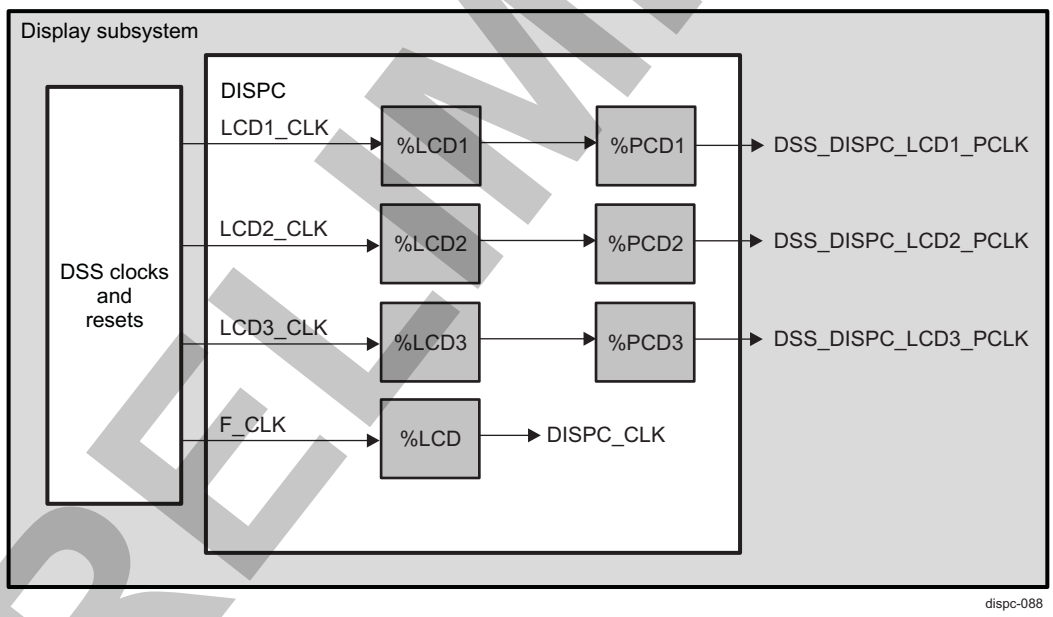
The PCLK frequency for each LCD output is derived from a dedicated input clock: LCD1_CLK, LCD2_CLK, or LCD3_CLK for the three LCD outputs, respectively. Each input clock is divided by the values of the DISPC_DIVISORo[23:16] LCD bit field and then the DISPC_DIVISORo[7:0] PCD bit field independently for each LCD pixel clock (see Figure 10-31). DSS_DISPC_LCD1_PCLK, DSS_DISPC_LCD2_PCLK, and DSS_DISPC_LCD3_PCLK are independent:

- DSS_DISPC_LCD1_PCLK = (LCD1_CLK/LCD1) / PCD1
- DSS_DISPC_LCD2_PCLK = (LCD2_CLK/LCD2) / PCD2
- DSS_DISPC_LCD3_PCLK = (LCD3_CLK/LCD3) / PCD3

The functional clock of the DISPC is derived from F_CLK by an independent divisor. The dividing value is set in the DISPC_DIVISORo[23:16] LCD bit field.

For backward compatibility, the divisor value LCD can be set to the value of LCD1. To enable this functionality, the DISPC_DIVISOR[0] ENABLE bit must be set to 1.

Figure 10-31. DISPC Clock Tree Overview



10.2.4.2 DISPC Software Reset

To perform a software reset on the DISPC, set the DISPC_SYSCONFIG[1] SOFTRESET bit to 0x1. The DISPC_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 0x1. When the software reset completes, the DISPC_SYSCONFIG[1] SOFTRESET bit is automatically reset. Software must ensure that the software reset completes before performing DISPC operations.

10.2.4.3 DISPC Power Management

The DISPC supports the MStandby/Wait, IdleReq/SidleAck, and wake-up protocols as defined in Chapter 3, *Power, Reset, and Clock Management*.

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10.2.4.3.1 DISPC Idle Mode

The DISPC supports no-idle mode, force-idle mode, and smart-idle mode. The mode can be selected by programming the appropriate value in the DISPC_SYSCONFIG[4:3] SIDLEMODE bit field.

Condition of assertion of the SIdleAck signal:

- In no-idle mode: SIdleAck is never asserted.
- In force-idle mode: SIdleAck is asserted unconditionally with a 1-configuration port interface clock cycle delay with respect to an IdleReq assertion.

NOTE: The proper use of force-idle mode assumes that no interrupt needs to be generated.

- In smart-idle mode: SIdleAck is asserted when at least the following conditions are satisfied:
  - No interrupt is pending.
  - The DISPC no longer uses the interface clock for the slave port.

Once SIdleAck is asserted, the DISPC interface lock used by the slave port can be shut down at any time.

The conditions of deassertion of the SIdleAck signal are:

- In force-idle mode: SIdleAck is deasserted with a 1-configuration port interface clock cycle delay with respect to an IdleReq deassertion.
- In smart-idle mode: SIdleAck is deasserted with a 1-configuration port interface clock cycle delay with respect to an IdleReq deassertion.

Once SIdleAck is released, the DISPC is fully operational and a DMA request can be processed normally.

10.2.4.3.2 DISPC StandBy Mode

The DISPC supports no-standby mode, force-standby mode, and a single smart-standby mode. The mode is set in the DISPC_SYSCONFIG[13:12] MIDLEMODE bit field. The functional clock is always active if the module is enabled. The L3_MAIN clock can be shut down at any time independently of the status of MStandby.

The conditions of assertion of the MStandby signal are:

- In no-standby mode: MStandby is never asserted.
- In force-standby mode: MStandby is asserted when the module is disabled.
- In smart-standby: In the case of one of the following conditions:
  - The GFX pipeline is disabled or enabled and the data fetch is complete for the GFX window, or the GFX pipeline is enabled but the data fetch did not complete and data in the DMA buffer is greater than the high threshold value.
  - The VID1 pipeline is disabled or enabled and the data fetch is complete for the VID1 window, or the VID1 pipeline is enabled but the data fetch did not complete and data in the DMA buffer is greater than the high threshold value.
  - The VID2 pipeline is disabled or enabled and the data fetch is complete for the VID2 window, or the VID2 pipeline is enabled but the data fetch did not complete and data in the DMA buffer is greater than the high threshold value.
  - The VID3 pipeline is disabled or enabled and the data fetch is complete for the VID3 window, or the VID3 pipeline is enabled but the data fetch did not complete and data in the DMA buffer is greater than the high threshold value.
  - The WB pipeline is disabled or enabled and the data store to memory is complete for the WB picture, or the WB pipeline is enabled but the data storage did not complete and data in the DMA buffer is lower than the low threshold value.

The MStandby signal asserts whenever all five events have occurred or the DISPC is disabled. While MStandby is asserted, the DISPC does not generate any transaction on the L3_MAIN master port.

The conditions of deassertion of the MStandby signal are:

- In force-standby mode: MStandby is deasserted only when the DISPC is enabled.

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- In smart-standby mode: In the case of one of the following conditions:
  - The GFX pipeline is enabled but the data fetch did not complete for the GFX window, and the data in the DMA buffer is less than the low threshold value.
  - The VID1 pipeline is enabled but the data fetch did not complete for the VID1 window, and the data in the DMA buffer is less than the low threshold value.
  - The VID2 pipeline is enabled but the data fetch did not complete for the VID2 window, and the data in the DMA buffer is less than the low threshold value.
  - The VID3 pipeline is enabled but the data fetch did not complete for the VID3 window, and the data in the DMA buffer is less than the low threshold value.
  - The WB pipeline is enabled but the data store did not complete for the WB picture, and the data in the DMA buffer more than the high threshold value.

Detection of the deassertion conditions assumes that the interface clocks are active.

10.2.4.3.3 DISPC Wakeup

The DISPC supports wake-up signaling. The mode can be selected by programming the appropriate value in the DISPC_SYSCONFIG[2] ENAWAKEUP bit. Because the SWakeUp signal is asynchronous, it does not require the interface clock.

The conditions of assertion of the SWakeUp signal are:

- The GFX pipeline is enabled but the data fetch did not complete for the GFX window, and the data in the DMA buffer is less than the low threshold value.
- The VID1 pipeline is enabled but the data fetch did not complete for the VID1 window, and the data in the DMA buffer is less than the low threshold value.
- The VID2 pipeline is enabled but the data fetch did not complete for the VID2 window, and the data in the DMA buffer is less than the low threshold value.
- The VID3 pipeline is enabled but the data fetch did not complete for the VID3 window, and the data in the DMA buffer is less than the low threshold value.
- The WB pipeline is enabled and the data in the DMA buffer is more than the high threshold value.
- The last pixel displayed into the LCD1 panel if it is not the last frame
- The last pixel displayed into the LCD2 panel if it is not the last frame
- The last pixel displayed into the LCD3 panel if it is not the last frame
- The last pixel displayed into the TV panel if it is not the last frame

The SWakeUp signal is asserted whenever any one of these nine events occurs and IdleAck is asserted.

When one of the active pipelines reaches the low threshold and must refill its DMA buffer for the current frame, all other pipelines refill their own DMA buffer even if their low threshold has not been reached. The DISPC_CONFIG1[17] BUFFERFILLING bit is used to increase the probability that the time increases, where there is no access to the L3_MAIN interconnect.

The condition of deassertion of the SWakeUp signal is:

- Immediately after deassertion of IdleReq

10.2.4.4 DISPC Interrupt Requests

The interrupt line, DISPC_DREQ, indicates when one or more events are detected by the hardware. Each event is independently maskable by setting the DISPC_IRQENABLE register.

To check when a particular interrupt event occurs and to reset a particular event, the DISPC_IRQSTATUS register must be accessed. This register regroups the status of internal events in the module that generate an interrupt (read 0: no interrupt occurred; read 1: interrupt occurred; write 1: status bit reset). For more information about checking and clearing interrupt events, see Section 10.1.3, *Display Subsystem Register Manual*.

Table 10-24 describes the interrupts generated for the DISPC.

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Table 10-24. DISPC Interrupts

Interrupt Name	Description
FLIPIMMEDIATEDONE_IRQ	Flip immediate done: Occurs when the DMA engine has acknowledged the immediate BA change, and software can write the new BA0.
FRAMEDONE1_IRQ	Frame done for LCD1 output: Active frame related to the LCD1 is complete and LCD1 output of the DISPC is disabled.
FRAMEDONE2_IRQ	Framedone for LCD2 output: Active frame related to the LCD2 is complete and LCD2 output of the DISPC is disabled.
FRAMEDONE3_IRQ	Frame done for LCD3 output: Active frame related to the LCD3 is complete and LCD3 output of the DISPC is disabled.
FRAMEDONETV_IRQ	Frame done for TV output: Active frame related to the TV output is complete and TV output of the DISPC is disabled.
FRAMEDONEWB_IRQ	Frame done for WB output: Active frame related to the WB is complete. First, it is used when the WB channel is connected to one of the pipelines to determine when the memory-to-memory transfer through DISPC is completed. Second, it is used when the WB channel is connected to one of the overlay output in nonreal-time mode to determine when the memory-to-memory transfer with overlay processing is completed.
VSYNC1_IRQ	VSYNC for primary LCD output: VSYNC interrupt for the primary LCD has occurred at the end of the frame.
VSYNC2_IRQ	VSYNC for secondary LCD output: VSYNC interrupt for the secondary LCD has occurred at the end of the frame.
VSYNC3_IRQ	VSYNC for third LCD output: VSYNC interrupt for the third LCD has occurred at the end of the frame.
EVSYNC_EVEN_IRQ	VSYNC for even field: EVSYNC_EVEN interrupt has occurred at the end of the frame (EVSYNC received and the field polarity is even) (HDMI)
EVSYNC_ODD_IRQ	VSYNC for odd field: EVSYNC_ODD interrupt has occurred at the end of the frame (EVSYNC received and the field polarity is odd) (HDMI)
ACBIASCOUNTSTATUS1_IRQ	AC bias count status for LCD1 output: AC bias transition counter has decremented to 0.
ACBIASCOUNTSTATUS2_IRQ	AC bias count status for LCD2 output: AC bias transition counter has decremented to 0.
ACBIASCOUNTSTATUS3_IRQ	AC bias count status for LCD3 output: AC bias transition counter has decremented to 0.
PROGRAMMEDLINENUMBER_IRQ	Programmed line number: The primary LCD has reached the user programmed line number.
VID1ENDWINDOW_IRQ	End of the VID1 window: The DMA engine has fetched all the data from memory for the VID1 for the current frame.
VID2ENDWINDOW_IRQ	End of the VID2 window: The DMA engine has fetched all the data from memory for the VID2 for the current frame.
VID3ENDWINDOW_IRQ	End of the VID3 window: The DMA engine has fetched all the data from memory for the VID3 for the current frame.
GFXENDWINDOW_IRQ	End of the graphics window: The DMA engine has fetched all the data from memory for the graphics for the current frame.
VID1BUFFERUNDERFLOW_IRQ	VID1 DMA buffer underflow: The input VID1 DMA buffer goes underflow.
VID2BUFFERUNDERFLOW_IRQ	VID2 DMA buffer underflow: The input VID2 DMA buffer goes underflow.
VID3BUFFERUNDERFLOW_IRQ	VID3 DMA buffer underflow: The input VID3 DMA buffer goes underflow.
WBBUFFEROVERFLOW_IRQ	WB DMA buffer overflow: The output WB DMA buffer goes overflow. It cannot occur when WB channel is used in memory-to-memory transfer mode but only in capture mode. In capture mode the timings are defined by the timer associated with the output. In memory-to-memory mode, there is timing constraint.
GFXBUFFERUNDERFLOW_IRQ	GFX DMA buffer underflow: The input graphics DMA buffer goes underflow.

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Table 10-24. DISPC Interrupts (continued)

Interrupt Name	Description
PALETTEGAMMALOADING_IRQ	Palette/gamma table loading: The palette/gamma table in the graphics pipeline has been loaded using the DISPC DMA engine.
WBUNCOMPLETEERROR_IRQ	The write-back buffer has been flushed before being fully drained. In WB capture mode, if the new frame starts before the WB DMA buffers are fully drained (onto external memory), then the contents of the WB DMA buffers are lost (implying last few pixels/lines are corrupted in the captured frame in memory). This interrupt is an indication of that, and will trigger every frame.
OCPERROR_IRQ	OCP error: L3_MAIN interconnect has sent SResp = ERR
SYNCLOST1_IRQ	Synchronization lost on LCD1 output: Occurs when VSYNC width/front or back porches are not wide enough to load the pipelines with data (LCD output).
SYNCLOST2_IRQ	Synchronization lost on LCD2 output: Occurs when VSYNC width/front or back porches are not wide enough to load the pipelines with data (LCD output).
SYNCLOST3_IRQ	Synchronization lost on LCD3 output: Occurs when VSYNC width/front or back porches are not wide enough to load the pipelines with data (LCD output).
SYNCLOSTTV_IRQ	Synchronization lost on TV output: Occurs when porches are not wide enough to load the pipelines with data (TV output connected to the HDMI).
WAKEUP_IRQ	Wakeup: Occurs when the SWakeUp signal is asserted.

10.2.4.5 DISPC DMA Requests

The DMA_SYSTEM synchronization line, DISPC_DREQ, is connected to the DMA_SYSTEM (DMA_SYSTEM_DREQ_5). This DMA request is not a classical one, but rather a synchronization signal between the DISPC and DMA_SYSTEM. The DMA_SYSTEM is informed that a programmable number of lines are output to the LCD and that a system memory can be updated. This request is related to the interrupt event PROGRAMMEDLINENUMBER_IRQ described in Table 10-24. This allows the DMA_SYSTEM channel to be synchronized with the internal DMA controller in the display subsystem.

In other words, it allows synchronizing a memory-to-memory frame buffer update based on the scan line of the frame buffer in system memory (SDRAM or SRAM) by the DISPC. The DISPC_DREQ request is generated at a programmable line number defined in the DISPC_LINE_NUMBER[11:0] LINENUMBER bit field. This process allows an application to use a single frame buffer and to update it after a certain number of lines are read by the DISPC.

10.2.4.6 DISPC DMA Engine

The DMA engine:

- Supplies data (encoded pixel data, palette, and gamma curve) from memories to the GFX, VID1, VID2, and VID3 pipelines through the interconnect based on the configuration of the DISPC and pipeline setting.
- Stores encoded pixel data from GFX/VID pipelines or overlays to memories through the WB pipeline and interconnect based on the configuration of the DISPC and WB pipeline setting.

Each pipeline has a dedicated buffer and a channel with independent settings. Table 10-25 lists the default size and allocation of the DMA buffer. Each DMA buffer is divided into two spaces, top and bottom. Depending on the application, a DMA buffer space can be associated to a pipeline or merged with other spaces. The total number of spaces for each pipeline is from 0 (pipeline inactive) to the number of pipelines × 2 (in that case, all the DMA buffers are associated to a single pipeline). The sum of the number of spaces allocated for each pipeline must not be greater than the maximum number of available spaces. The correct number of spaces must be allocated to ensure no underflow. The spaces allocated to each pipeline must be greater than or equal to the minimum number of spaces required to support the throughput and system latency. The space assignations are done in the DISPC_GLOBAL_BUFFER register.

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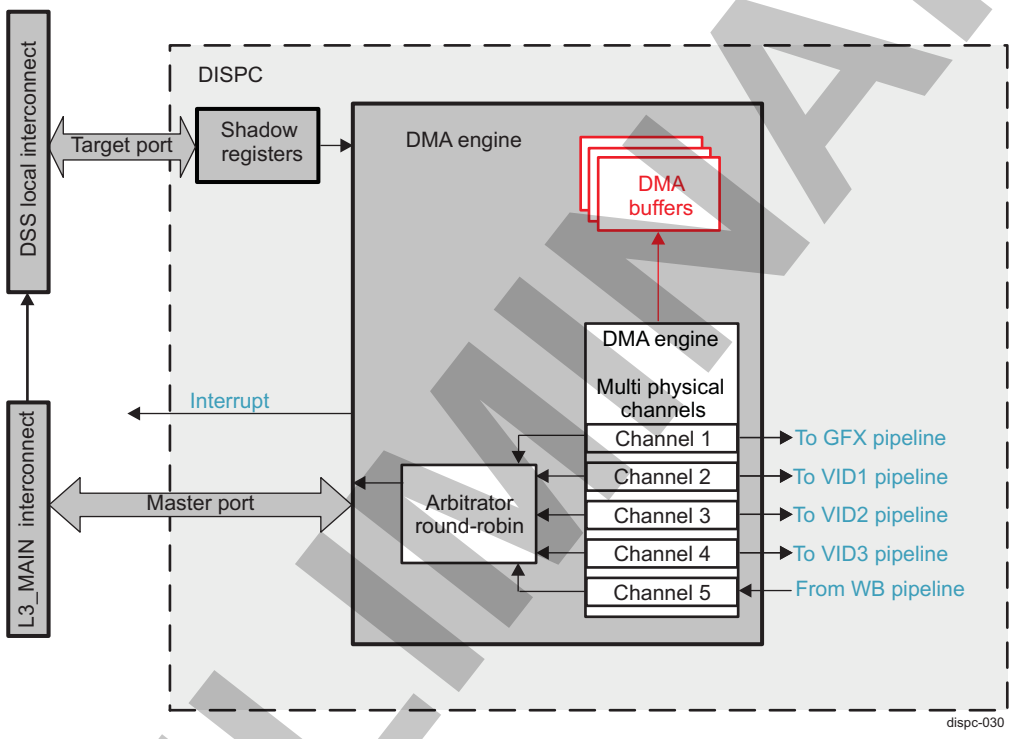
Table 10-25. DISPC DMA Buffer Size

Pipelines	DMA Buffer Size
GFX	2 lines × 640 × 128 bits
VID1	2 lines × 1024 × 128 bits
VID2	2 lines × 1024 × 128 bits
VID3	2 lines × 1024 × 128 bits
WB	2 lines × 1024 × 128 bits

Figure 10-32 is an overview of the DMA engine.

Figure 10-32. DISPC DMA Engine Overview



10.2.4.6.1 DISPC

For each line to be fetched/stored, the DMA engine:

- Calculates the pixel address
- Aligns the address
- Defines the burst structure:
  - Type of burst (1D- or 2D-burst structure)
  - Length of the burst

The DMA engine generates scan addresses to read and write data to and from system memory. The base address defines the start address of the first pixel, and then the address is incremented based on the number of pixels per line, offset between two consecutive lines and number of lines. The byte address of each pixel in the frame buffer in the system memory is determined by:

Pixel address = Base address + x × bpp + (y × ((width × bpp) + increment))

where:

- Base address corresponds to the base address (for YUV–NV12 or YUV4:2:0-NV21 format) defined by:
  - DISPC_GFX_BA_0[31:0] BA bit field
  - DISPC_GFX_BA_1[31:0] BA bit field

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  - DISPC_VIDp_BA_0[31:0] BA bit field
  - DISPC_VIDp_BA_1[31:0] BA bit field
  - DISPC_VIDp_BA_UV_0[31:0] BA bit field
  - DISPC_VIDp_BA_UV_1[31:0] BA bit field
- bpp corresponds to the number of bits per pixel defined by the DISPC_GFX_ATTRIBUTES[4:1] FORMAT bit field or the DISPC_VIDp_ATTRIBUTES[4:1] FORMAT bit field.
- width corresponds to the number of pixels per line defined by the DISPC_GFX_SIZE[11:0] SIZEX + 1 bit field or DISPC_VIDp_SIZE[11:0] SIZEX + 1 bit field.
- increment corresponds to the number of bytes to skip between two contiguous lines defined by the DISPC_GFX_ROW_INC[31:0] ROWINC – 1 bit field or the DISPC_VIDp_ROW_INC[31:0] ROWINC – 1 bit field.
- x corresponds to the pixel position on the x-axis.
- y corresponds to the pixel position on the y-axis.

NOTE: For YUV format, the pixel values are defined in two buffers (Y and UV). The base address of the Y buffers is defined in the DISPC_VIDp_BA_j[31:0] BA bit field. The base address of the UV buffers is defined in the DISPC_VIDp_BA_UV_j[31:0] BA bit field.

Table 10-26 summarizes the register settings for a simple access of a picture in the system memory.

Table 10-26. DISPC Register Settings for Accessing Image in Internal Memory

Registers	Value
DISPC_GFX_BA_j/DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA, the physical base address of image in the memory
DISPC_VIDp_BA_UV_j/DISPC_WB_BA_UV_j	PBA, the physical base address of UV buffers image in the memory
DISPC_GFX_PIXEL_INC/DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 or other in pixel incremental value
DISPC_GFX_ROW_INC/DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	1 or other in row incremental value

An interconnect request (128 bits) corresponds to one or several pixels, depending on the bits per pixel. Therefore, the DMA engine determines the appropriate burst sequence to optimize the fetching/storing of each new line. The DMA engine must prevent a single burst from crossing two lines. The DMA engine supports bursts of 2 × 128 bits, 4 × 128 bits, and 8 × 128 bits. The default burst size at reset time is 8 × 128 bits. The maximum burst size can be configured for each pipeline by setting the DISPC_GFX_ATTRIBUTES[7:6] BURSTSIZE or DISPC_VIDp_ATTRIBUTES[15:14] BURSTSIZE bit field. Because the burst size must be aligned to the burst boundary, in case of misalignment, the DMA engine may issue one request and/or smaller burst requests. Two types of burst are present which can be configured from the DISPC_GFX_ATTRIBUTES[29] BURSTTYPE or DISPC_VIDp_ATTRIBUTES[29] BURSTTYPE bit. Also, a force function is present configured from the DISPC_GFX_ATTRIBUTES[16] FORCE1DTILEDMODE or DISPC_VIDp_ATTRIBUTES[20] FORCE1DTILEDMODE or DISPC_WB_ATTRIBUTES[20] FORCE1DTILEDMODE bit for the following burst types:

- 1-D burst is used if the fetch/storage is linear in memory through the TILER. There is no rotation of the frame buffer. The frame buffer is not tiled.
- 2-D burst is used if the frame buffer is tiled.

Even if the DISPC_VIDp_ROW_INC register does not equal 1, the user can select 2-D burst. 2-D burst is used when the DISPC is configured to read one field of a frame by accessing only the even and odd lines.

NOTE: The burst size is initialized once at configuration and can be changed when the DISPC is disabled.

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10.2.4.6.2 DISPC Immediate Base Address Flip Mechanism

The Flip Immediate mechanism is used to change of the fly the content of the frame buffer which is currently being displayed. The mechanism allows multiple changes (flips) of the base address (BA) during a frame. The mechanism is available for all pipelines (VID1, VID2, VID3, and GFX). Changes to the BA can be applied during the same line, or during different lines.

The following considerations must be considered:

- Data fetching from a new immediate BA is aligned with the data fetch mechanism of the DISPC DMA engine itself, and not with HSYNC or any other DISPC timing signal. After new VSYNC frame pulse, new BA is taken by hardware, as soon as the first set of lines is sent to internal pipeline of the DMA engine.
  - If multiple new BAs are written during the same line (before DMA engine acknowledges the first BA change), then programming steps 1 and 2 must be applied for each new BA (see the programming sequence in this section). The DMA takes only the last BA provided within the current line scan.
  - If multiple new BAs are written during different lines within the current frame, then programming steps 1 and 2 must be applied for each new BA (see the programming sequence in this section). The DMA takes the new BA each time it is updated.
- Immediate BA change cannot be achieved synchronously for two or more pipelines.
- Immediate BA change is possible only for BA0; it is not possible for BA1. Interlaced mode using BA0 and BA1 is not supported.
- Immediate BA change is supported only in RGB color space.

The Flip Immediate mechanism programming sequence follows:

1. Software writes the new immediate BA to the DISPC_GFX_BA_j register (where j=0) for the GFX pipeline, or to the DISPC_VID1_BA_j / DISPC_VID2_BA_j / DISPC_VID3_BA_j register (where j=0) for the required VID pipeline.
2. Software sets to 0x1 the corresponding EN bit for the required pipeline in the DISPC_BA0_FLIPIMMEDIATE_EN register.
3. The DISPC DMA engine, after completing its current line (or set of lines) fetch, takes the new immediate BA.
4. Hardware resets the EN bit in DISPC_BA0_FLIPIMMEDIATE_EN register and asserts a flip immediate IRQ. The IRQ can be enabled through the DISPC_IRQENABLE[31] FLIPIMMEDIATEDONE_EN bit. The status of the event is available in the DISPC_IRQSTATUS[31] FLIPIMMEDIATEDONE_IRQ bit.

10.2.4.6.3 DISPC DMA Buffers

10.2.4.6.3.1 DISPC READ DMA Buffers (GFX and VID Pipelines)

When the vertical front porch (VFP) period starts after the last horizontal front porch (HFP) of the last line or the external VSYNC is received, the DMA buffers are flushed according to the selected output associated with the pipeline. The DMA engine restarts fetching data from the memory through the L3_MAIN interconnect. Enabling or disabling the DISPC flushes the DMA buffers (except the WB DMA buffers).

Programmable high and low thresholds, independent for each DMA buffer, are used by the DMA engine to start and stop requesting data to the L3_MAIN interconnect.

- When low threshold (set in the DISPC_GFX_BUF_THRESHOLD[15:0] BUFLOWTHRESHOLD or DISPC_VIDp_BUF_THRESHOLD[15:0] BUFLOWTHRESHOLD bit field) is reached, the DMA engine starts a request on the L3_MAIN interconnect to fill the DMA buffer.
- When high threshold (set in the DISPC_GFX_BUF_THRESHOLD[31:16] BUFHIGHTHRESHOLD or DISPC_VIDp_BUF_THRESHOLD[31:16] BUFHIGHTHRESHOLD bit field) is reached, the DMA engine stops requesting encoded pixels.

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To avoid underflow at the beginning of a frame and have sufficient encoded pixel data to start some processing, a preloading of the DMA buffer is configurable between a fixed value of bytes or the high threshold value. The preload ensures a minimum number of pixels present in the buffer. When the preload value is reached, the associated channel must start pulling pixels out of the DMA buffer. To enable the preload based on the value entered in the DISPC_GFX_PRELOAD[11:0] PRELOAD or DISPC_VIDp_PRELOAD[11:0] PRELOAD bit field, the DISPC_GFX_BUF_THRESHOLD[11] BUFPRELOAD bit, or the DISPC_VIDp_BUF_THRESHOLD[19] BUFPRELOAD bit must be set to 0x0.

NOTE: When self-refresh mode is selected, meaning the data in the DMA buffers are used for multiple frames, and at the end of each frame, the DMA buffers are not flushed.

10.2.4.6.3.2 DISPC WRITE DMA Buffer (WB Pipeline)

Two modes are supported by the WB channel, selectable through the DISPC_WB_ATTRIBUTES[19] WRITEBACKMODE bit:

- Capture mode, WRITEBACKMODE bit set to 0: One of the overlay outputs going to LCD or TV outputs is captured and at the same time the data are sent on the output. The WB timings are controlled by the LCD or TV timings.
- Memory-to-memory mode, WRITEBACKMODE bit set to 1: One of the overlay outputs or one of the pipelines is captured to perform a memory-to-memory transfer, with some processing by the DISPC (rescaling, overlaying, color space conversion, etc.).

In capture mode: The WB DMA buffers are flushed when the VFP period starts after the HFP following the last line, or when the external VSYNC is received, depending on which output (LCD/TV) the WB pipeline is capturing data, if the programmed value in DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field is set to 0. If the programmed value in DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field is set to N (1:255), the write buffers DMA are flushed N lines later. The DMA engine starts storing data to memory through the L3_MAIN-based interconnect as soon as enough data is available for the programmed burst size. When enabling/disabling the DISPC, the DMA buffers are flushed. The programmable thresholds low and high are used by the DMA engine to start and stop sending data to the L3_MAIN interconnect.

NOTE: If the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field is set to 0, the WB is reinitialized at the end of the last line of a frame at the beginning of the VFP signal. To let the WB complete the data write to the external memory, the highest possible value compatible with the vertical blanking period must be set.

NOTE: In WB capture mode, if a new frame starts before the WB DMA buffers contents are fully written onto external memory, then the contents of the WB DMA buffers are lost (implying last few pixels/lines are corrupted in the captured frame in memory). The DISPC_IRQSTATUS[26] WBUNCOMPLETEERROR_IRQ interrupt bit indicates this situation and triggers every frame. The WBUNCOMPLETEERROR interrupt can be enabled through the DISPC_IRQENABLE[26] WBUNCOMPLETEERROR_EN register bit.

Software can avoid this by delaying the flush of WB DMA buffers through proper programming of the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field.

In memory-to-memory mode: The WB pipeline is not synchronized to any internal or external timing generator. The WB pipeline stores the output of one of the overlay outputs or one of the pipelines. When enabling or disabling the DISPC, the DMA buffers are flushed. The programmable thresholds low and high are used by the DMA engine to start and stop sending data to the L3_MAIN interconnect.

Programmable high and low thresholds are used by the DMA engine to start and stop sending data to the L3_MAIN interconnect.

- When high threshold (set in the DISPC_WB_BUF_THRESHOLD[31:16] BUFHIGHTHRESHOLD bit field) is reached, the DMA engine starts sending data on the L3_MAIN interconnect to empty buffer.
- When low threshold (set in the DISPC_WB_BUF_THRESHOLD[15:0] BUFLOWTHRESHOLD bit field)

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is reached, the DMA engine stops sending encoded pixels.

At the end of the frame, to completely drain the DMA buffer, some smaller bursts (even single requests) must be issued. To limit the number of interconnect requests from the DISPC, a number of IDLE cycles between requests can be inserted. IDLE cycles can be inserted only when WB is used in memory-to-memory mode. It is ignored when WB is in capture mode.

The number of IDLE cycles between requests can be activated and determined by:

- Setting the DISPC_WB_ATTRIBUTES[27] IDLESIZE bit to 0x0 (default value) and entering the number of idles between requests in the DISPC_WB_ATTRIBUTES[31:28] IDLENUMBER bit field. Idle numbers vary from 0 to 15.
- Setting the DISPC_WB_ATTRIBUTES[27] IDLESIZE bit to 0x1, which considers the size of the burst (the DISPC_WB_ATTRIBUTES[15:14] BURSTSIZE bit field) to determine the number of IDLE cycles.
  - If BURSTSIZE = 0x0, then the number of IDLE cycles equals IDLENUMBER (0 to 15).
  - If BURSTSIZE = 0x1, then the number of IDLE cycles equals IDLENUMBER × 4 (0 to 60).
  - If BURSTSIZE = 0x2, then the number of IDLE cycles equals IDLENUMBER × 8 (0 to 120).

10.2.4.6.4 DISPC MFLAG Mechanism and Arbitration

The MFLAG mechanism allows a dynamic increase of the priority of DISPC real-time traffic, when required, based on the fullness of the DISPC DMA read and write buffers.

The mechanism is implemented for all DMA buffers (GFX, VID1, VID2, VID3 and WB). Only high-priority pipelines can contribute to the MFLAG mechanism.

Programmable buffer thresholds (hysteresis) for each pipeline are used to indicate when the local MFLAG signal for each pipeline is generated. All local MFLAG signals are ORed to generate a single DSS MFLAG out band signal, which is provided to the L3 interconnect for granting OCP requests. The out band DSS MFLAG signal is asynchronous to any ongoing OCP transaction.

The threshold for each pipeline corresponds to the fullness of the associated DMA buffer, and is defined by two threshold parameters:

- HT_MFLAG: High threshold.
  - For read access from the GFX, VID1, VID2, and VID3 pipelines, when the corresponding pipeline buffer reaches the programmed value, the associated local MFLAG signal goes low (deasserted).
  - For write access from the WB pipeline, when the corresponding pipeline buffer reaches the programmed value, the associated local MFLAG signal goes high (asserted).
  - This threshold can be programmed in the following bit fields:
    - For the GFX pipeline in the DISPC_GFX_MFLAG_THRESHOLD[31:16] HT_MFLAG bit field
    - For the VID1 pipeline in the DISPC_VID1_MFLAG_THRESHOLD[31:16] HT_MFLAG bit field
    - For the VID2 pipeline in the DISPC_VID2_MFLAG_THRESHOLD[31:16] HT_MFLAG bit field
    - For the VID3 pipeline in the DISPC_VID3_MFLAG_THRESHOLD[31:16] HT_MFLAG bit field
    - For the WB pipeline in the DISPC_WB_MFLAG_THRESHOLD[31:16] HT_MFLAG bit field
- LT_MFLAG: Low threshold.
  - For read access from the GFX, VID1, VID2, and VID3 pipelines, when the corresponding pipeline buffer reaches the programmed value, the associated local MFLAG signal goes high (asserted).
  - For write access from the WB pipeline, when the corresponding pipeline buffer reaches the programmed value, the associated local MFLAG signal goes low (deasserted).
  - This threshold can be programmed in the following bit fields:
    - For the GFX pipeline in the DISPC_GFX_MFLAG_THRESHOLD[15:0] LT_MFLAG bit field
    - For the VID1 pipeline in the DISPC_VID1_MFLAG_THRESHOLD[15:0] LT_MFLAG bit field
    - For the VID2 pipeline in the DISPC_VID2_MFLAG_THRESHOLD[15:0] LT_MFLAG bit field
    - For the VID3 pipeline in the DISPC_WB_MFLAG_THRESHOLD[15:0] LT_MFLAG bit field
    - For the WB pipeline in the DISPC_WB_MFLAG_THRESHOLD [15:0] LT_MFLAG bit field

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By default, the MFLAG mechanism is disabled (DISPC_GLOBAL_MFLAG_ATTRIBUTE[1:0] MFLAG_CTRL bit field = 0x0), and the DSS MFLAG out band signal is low (deasserted). The arbitration scheme for the DISPC pipelines is the same as described in Section 10.2.4.6.7, *DISPC Arbitration*. That is, round-robin either between high-priority pipelines, or between normal-priority pipelines (if all pipelines are of normal priority).

When the DISPC_GLOBAL_MFLAG_ATTRIBUTE[1:0] MFLAG_CTRL bit field is set to 0x2, the MFLAG mechanism is enabled, and the DSS MFLAG out band signal is dynamically set to 0 or 1, depending on DMA buffers fullness and programmed threshold levels, as explained previously in this section. In this case, the arbitration scheme for DISPC pipelines is round-robin between those high-priority pipelines, which have asserted local MFLAG signals. If there are no high-priority pipelines with asserted local MFLAG signals, then the arbitration scheme is the same as described in Section 10.2.4.6.7, *DISPC Arbitration*.

The DISPC_GLOBAL_MFLAG_ATTRIBUTE[2] MFLAG_START bit defines additional rules for the MFLAG mechanism:

- If the MFLAG_START bit is set to 0x0 (default value), then in the beginning of the frame when the DMA buffer is empty, the local MFLAG signal of each pipeline is kept at 0 until PRELOAD is reached (for more information on preloading, see Section 10.2.4.6.3.1, *DISPC READ DMA Buffers (GFX and VID Pipelines)*. Then, based on the setting of the DISPC_GLOBAL_MFLAG_ATTRIBUTE[1:0] MFLAG_CTRL bit field, the MFLAG signal is generated and internal logic is arbitrating between pipeline requests.
- If the MFLAG_START bit is set to 0x1, then even in the beginning of the frame when the DMA buffer is empty, the DISPC_GLOBAL_MFLAG_ATTRIBUTE[1:0] MFLAG_CTRL bit field defines the generation of the MFLAG signal for each pipeline.

10.2.4.6.5 DISPC Predecimation

The predecimation process consists of downscaling an image by fetching only the necessary pixels in the memory. Vertical and horizontal predecimation are possible:

- Vertical predecimation: The picture stored in memory can be predecimated vertically by skipping lines. Burst mode is used to fetch the data when skipping lines. Only the lines that will be used by the DISPC are fetched from memory; the other lines are skipped. The DMA engine sends requests only for the useful lines using 1-D or 2-D burst, depending on the setting. The base address indicates the first valid pixel to fetch from memory. The number of lines to skip is set in the DISPC_GFX_ROW_INC[31:0] ROWINC or DISPC_VIDp_ROW_INC[31:0] ROWINC bit field.

  NOTE: When 2-D burst mode is used, the access to data in memory is performed through the TILER module of DMM (for more details, see , *TILER Overview*, in Chapter 15, *Memory Subsystem*), and as a result a maximum of one line can be skipped.

- Horizontal predecimation: When fetching data from memory, it is possible to skip 1 of 2 pixel data containers, up to 1 of 16 pixel data containers, by setting the DISPC_GFX_PIXEL_INC[7:0] PIXELINC or DISPC_VIDp_PIXEL_INC[7:0] PIXELINC bit field to the number of pixel data containers to skip (n), multiplied by the size of a pixel data container (in bytes), + 1. See the following note for more details.

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NOTE: The restriction to horizontal predecimation is that there is at least one useful pixel per 128-bit request. In that case, the DMA engine uses burst mode instead of singles to optimize the requests in terms of latency and SDRAM efficiency.

No decimation is supported when the input format is 1, 2, 4, or 8 BITMAP.

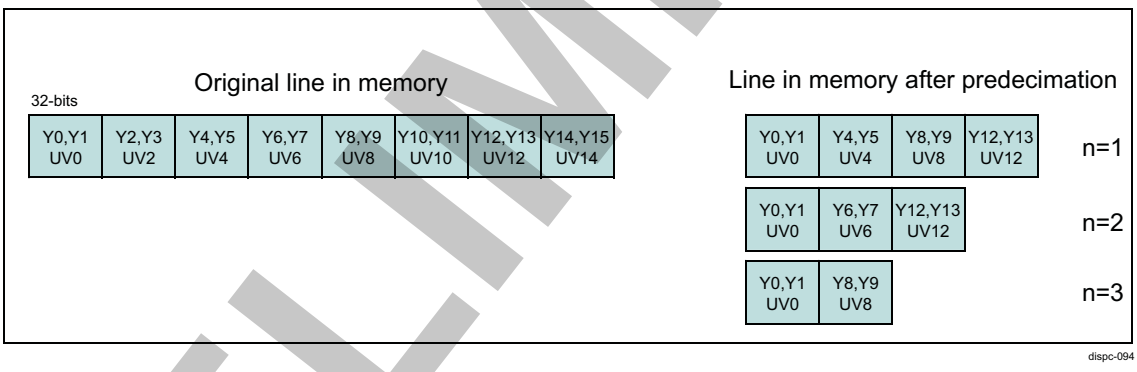
For RGB and YUV4:2:0 data formats, each pixel data container in memory holds 1 pixel. Thus, when configuring the PIXELINC bit field, the value of n equals the number of pixels to skip:

- For RGB format, one pixel data container = 32 bits = 1 pixel
- For YUV format:
  - One Y pixel data container = 8 bits = 1 pixel
  - One UV pixel data container = 16 bits = 1 pixel

For YUV4:2:2 format, each 32-bit pixel data container holds the Luma components for 2 pixels, and the Chrominance component of 1 pixel (see Figure 10-33). Therefore, for the valid values of the PIXELINC bit field in the case of the following YUV4:2:2 format, caution must be taken because n equals the number of pixel data containers to skip, not the number of pixels:

- For n = 1, PIXELINC = 5
- For n = 2, PIXELINC = 9
- For n = 3, PIXELINC = 13
- For n = 4, PIXELINC = 17, etc.

Figure 10-33. YUV4:2:2 Predecimation



10.2.4.6.6 DISPC Progressive-to-Interlaced Format Conversion

The DMA engine can be used to perform YUV4:2:0 NV12 and YUV4:2:0 NV21 progressive-to-interlaced data conversion with 0-degree orientation. This section provides generic approach details.

Two possible configurations are available, depending on the setting of the DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit, which defines the stride of each pixel value buffer for the YUV format. The following must be considered for both configurations:

- The DISPC_VIDn_BA_j[31:29] BA and DISPC_VIDn_BA_UV_j[31:29] BA bit fields, and the DISPC_VIDn_ATTRIBUTES[13:12] ROTATION bit field must be set to 0x0 to indicate 0-degree orientation.
- The DISPC_VIDn_BA_j[31:29] BA and DISPC_VIDn_BA_UV_j[31:29] BA bit fields must be set to 0x3, and the DISPC_VIDn_ATTRIBUTES[13:12] ROTATION bit field must be set to 0x2 to indicate 180-degree orientation.

Configuration 1 – YUV4:2:0 progressive to interlaced conversion

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The DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit is set to 0x1. The CbCr container is twice the size of the Y container. All Luma and Chroma lines for even and odd fields are fetched from memory. The scaler unit of the respective pipeline can be used to downscale by 2 (through filtering) the fetched data to create the interlaced output. For more information about the scaler configuration, see Section 10.2.4.10.4, *Scaler Unit*.

Configuration 2 – YUV4:2:0 progressive to YUV4:2:2 interlaced conversion

The DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit is set to 0x0. The CbCr container is the same size as the Y container. The DISPC_VIDn_ROW_INC register for the respective pipeline must be configured so that only the Y data is vertically predecimated by 2 (for more information, see Section 10.2.4.6.5, *Predecimation*). The CbCr data must not be predecimated. As a result, only the even Luma lines for the even field and the odd Luma lines for the odd field are fetched from memory. To create the interlaced output, all the Chroma lines are fetched from memory.

10.2.4.6.7 DISPC Arbitration

The requests (reads or writes) sent to the L3_MAIN interconnect are pipelined and arbitrated in a round-robin scheme. The default arbitration scheme must be modified by setting the priority attribute of each pipeline as defined in the following bits:

- DISPC_GFX_ATTRIBUTES[14] ARBITRATION
- DISPC_VIDp_ATTRIBUTES[14] ARBITRATION
- DISPC_WB_ATTRIBUTES[14] ARBITRATION

By default, all pipelines have the same priority (normal), which means all pipeline requests are treated in a round-robin order manner. If one or more pipelines require a higher number of requests going to the L3_MAIN interconnect, its priority can be moved up to high priority. In this case, the high-priority pipeline is granted access before any pipeline in normal priority. If more than one active pipeline is in high priority, the behavior is the same as all active pipelines in normal priority. Normal active pipelines are not treated until all high active pipelines are finished. The ARBITRATION bit cannot be modified during the entire frame.

This functionality balances the bandwidth of the pipeline depending on its constraint. It can be used to give higher priority to the pipelines with real-time constraints versus non-real-time pipelines. For example, pipelines associated with the LCD output in stall mode must have lower priority than pipelines associated with TV output.

10.2.4.6.8 DISPC DMA Power Modes

10.2.4.6.8.1 DISPC DMA Low-Power Mode

Each DMA buffer is divided into two spaces. Each space can be associated with the pipeline or merged with other DMA buffers. The total number of DMA buffers for each pipeline is from 0 (pipeline inactive) to the number of pipelines × 2 (in that case all the DMA buffers are associated with a single pipeline). The sum of the number of DMA buffers allocated for each pipeline must not be greater than the maximum available. The correct number of DMA buffers must be allocated to ensure no underflow. The number of DMA buffers allocated to each pipeline must be greater than or equal to the minimum required to support the throughput and the system latency.

NOTE: When the number of buffers is changed, the thresholds must be reprogrammed to reflect the new configuration of the DMA buffer.

10.2.4.6.8.2 DISPC DMA Ultralow-Power Mode

In low-power mode, the L3_MAIN interconnect is used to fill up the DMA buffers to store all the data required to display a full frame. The L3_MAIN interconnect is not used to fetch new pixels for the following frames. The data in the DMA buffer are reused to display on the screen.

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The setting of the mode is independent for each pipeline. One pipeline may have all the frame pixels in its DMA buffer and the other pipelines may have to refill their respective DMA buffers along the display scan because the frame buffer is too big to be stored in the DMA buffer.

The DMA buffers can be merged to optimize the L3_MAIN interconnect off time. Merging the DMA buffers into a single buffer can be used at the same time to improve ultralow-power mode (see Section 10.2.4.6.8.1, *Low-Power Mode*).

During the time in which the frames are fetched in the internal DMA buffer, MStandby must be asserted if the DISPC_SYSCONFIG[13:12] MIDLEMODE bit field is set to 0x2 (smart-standby mode).

Two ultralow-power modes can be entered manually or automatically:

- Self-refresh mode: Starting self-refresh mode is done manually by setting the DISPC_GFX_ATTRIBUTES[15] SELFREFRESH or DISPC_VIDp_ATTRIBUTES[15] SELFREFRESH bit to 0x1 after capturing a frame in the DMA buffers. Self-refresh mode is stopped by setting the SELFREFRESH bit to 0x0.
- Automatic self-refresh mode: By setting the DISPC_GFX_ATTRIBUTES[17] SELFREFRESHAUTO or DISPC_VIDp_ATTRIBUTES[17] SELFREFRESHAUTO bit to 0x1, the transition from off to on self-refresh mode is done by hardware after capturing the first frame. The hardware reflects the status of the self-refresh mode by setting the SELFREFRESH bit to 0x1, which means that the data are read inside the DMA buffer without accessing the interconnect and system memory during the frame. Setting the SELFREFRESH bit to 0x0 updates the DMA buffer.

NOTE: The WB pipeline does not support ultralow-power mode.

10.2.4.7 DISPC Rotation and Mirroring

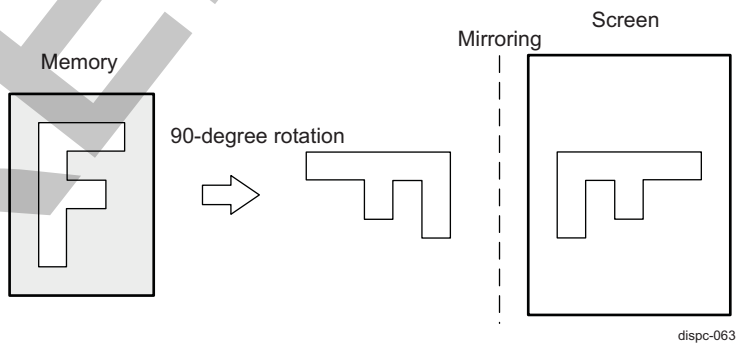
The DISPC provides flexible mechanisms for efficient implementation of rotation using the DISPC, its DMA engine, and the rotation engine of the TILER. The rotation is handled only through the TILER, which supplies the encoded pixels to the DISPC.

NOTE: No rotation or mirroring is supported when accessing internal SDRAM directly.

The TILER supports:

- Rotation: 0-, 90-, 180-, and 270-degree views
- Mirroring
- Any combination of rotation and mirroring (for example, Rot-90 + mirroring)

Figure 10-34. DISPC 90-Degree Rotation With Mirroring



When accessing YUV4:2:2 data, each 32-bit value loaded into the DMA buffer can represent either:

- Two consecutive pixels on the same line (for instance, 0- to 180-degree rotation)
- Two pixels adjacent vertically (for instance, 90- to 270-degree rotation)

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The reading from the DMA buffer supports the extraction of the two pixels, regardless of the rotation. When the pixels are not consecutive on the same line (90- to 270-degree rotation), the chrominance sample of the first pixel of each 32-bit value is duplicated for the second pixel in the same 32-bit value.

The rotation flag DISPC_VIDn_ATTRIBUTES[13:12] ROTATION and DISPC_VIDn_ATTRIBUTES[4:1] FORMAT bit fields define the processing to extract the pixels from YUV4:2:2 32-bit values. Software must ensure that the settings of the ROTATION and FORMAT bit fields are coherent with the rotation and mirroring defined through the address format in the TILER-specific address map. For more information, see , *Dynamic Memory Manager*, in *Chapter 15, Memory Subsystem*.

NOTE: For YUV4:2:0 NV12, 2D tiled memory access cases, the DISPC_VIDn_ATTRIBUTES[13:12] ROTATION bit field should be set properly to match with the intended rotation of the use case.

Table 10-27 describes the register settings of the DISPC when accessing, rotating, and mirroring an image using the TILER. A physical base address (PBA) for each rotation is determined and set as the buffer address (BA). The row incremental is determined and set in ROW_INC. The value of the pixel increment, PIXEL_INC, is set to 0x1 (contiguous pixels).

Table 10-27. DISPC Register Settings for Rotation Using TILER

Rotation	Registers	Rotation With and Without Mirroring
0 degree	DISPC_GFX_BA_j/DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA0
	DISPC_GFX_PIXEL_INC/DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 to 16
	DISPC_GFX_ROW_INC/DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	ROW0
90 degrees	DISPC_GFX_BA_j/DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA90
	DISPC_GFX_PIXEL_INC/ DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 to 16
	DISPC_GFX_ROW_INC/ DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	ROW90
180 degrees	DISPC_GFX_BA_j/DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA180
	DISPC_GFX_PIXEL_INC/DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 to 16
	DISPC_GFX_ROW_INC/ DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	ROW180
270 degrees	DISPC_GFX_BA_j/DISPC_VIDp_BA_j/DISPC_WB_BA_j	PBA270
	DISPC_GFX_PIXEL_INC/DISPC_VIDp_PIXEL_INC/DISPC_WB_PIXEL_INC	1 to 16
	DISPC_GFX_ROW_INC/ DISPC_VIDp_ROW_INC/DISPC_WB_ROW_INC	ROW270

NOTE: For YUV format, in addition to the DISPC_VIDp_BA_j register used for the Y component, the DISPC_VIDp_BA_UV_j register must be set to define the base address of the UV frame buffer in memory.

The PBA rotation is determined by:

- PBA0 = PBA | (mode << 27) | (orientation << 29) | (1<<32)
- PBA90 = PBA | (mode << 27) | (orientation << 29) | (1<<32)
- PBA180 = PBA | (mode << 27) | (orientation << 29) | (1<<32)
- PBA270 = PBA | (mode << 27) | (orientation << 29) | (1<<32)

Where PBA is the physical base address of the image in the memory.

The ROW rotation is determined by:

- If 8 bits per pixel:
  - ROW0 = 16384: Width of the video picture in memory (in bytes) + 1
  - ROW90 = 8192: Width of the video picture in memory (in bytes) + 1
  - ROW180 = 16384: Width of the video picture in memory (in bytes) + 1
  - ROW270 = 8192: Width of the video picture in memory (in bytes) + 1

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- If 16 bits per pixel:
  - ROW0 = 32768: Width of the video picture in memory (in bytes) + 1
  - ROW90 = 8192: Width of the video picture in memory (in bytes) + 1
  - ROW180 = 32768: Width of the video picture in memory (in bytes) + 1
  - ROW270 = 8192: Width of the video picture in memory (in bytes) + 1
- If 32 bits per pixel:
  - ROW0 = 32768: Width of the video picture in memory (in bytes) + 1
  - ROW90 = 16384: Width of the video picture in memory (in bytes) + 1
  - ROW180 = 32768: Width of the video picture in memory (in bytes) + 1
  - ROW270 = 16384: Width of the video picture in memory (in bytes) + 1

Table 10-28 and Table 10-29 list the DISPC rotation mode and rotation orientation definitions, respectively.

Table 10-28. DISPC Rotation Mode Definition

	8-Bit Tiled	16-Bit Tiled	32-Bit Tiled	Page Tiled
Mode	0	1	2	3

Table 10-29. DISPC Rotation Orientation Definition

Type of Orientation	Value
0-degree view	0x0
180-degree view with mirroring	0x1
0-degree view with mirroring	0x2
180-degree view	0x3
270-degree view with mirroring	0x4
270-degree view	0x5
90-degree view	0x6
90-degree view with mirroring	0x7

NOTE: For YUV4:2:0 progressive pixel format, because the value of the DISPC_VIDp_ROW_INC register is defined for the Y buffer, the DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit must be set to 1 when rotating the picture by 0 and 180 degrees, and must be reset to 0 when rotating the picture by 90 and 270 degrees.

For YUV4:2:0 interlaced pixel format, because the value of the DISPC_VIDp_ROW_INC register is defined for the Y buffer, the DISPC_VIDp_ATTRIBUTES[22] DOUBLESTRIDE bit must be set to 1 when rotating the picture by 0 and 180 degrees. Rotations of 90 and 270 degrees are not supported with this pixel format.

10.2.4.8 DISPC Memory Format

The graphic and video pipelines support various types of memory formats. Table 10-30 lists all supported formats for each pipeline. Nibble mode is enabled by setting the DISPC_GFX_ATTRIBUTES[9] NIBBLEMODE bit to 0x1 and applies only to BITMAP format for the GFX pipeline.

Table 10-30. DISPC Memory Formats Supported

Formats	GFX	VID1	VID2	VID3	WB
BITMAP 1-bpp	x				
BITMAP 2-bpp	x				
BITMAP 4-bpp	x				
BITMAP 8-bpp	x				

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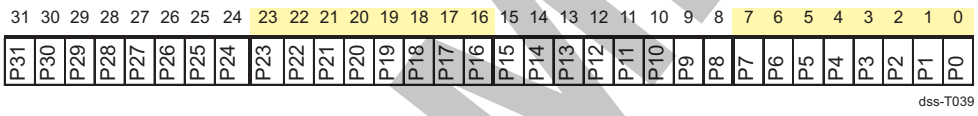
Table 10-30. DISPC Memory Formats Supported (continued)

Formats	GFX	VID1	VID2	VID3	WB
xRGB12-4444	x	x	x	x	x
RGBx12-4444	x	x	x	x	x
ARGB16-4444	x	x	x	x	x
RGBA16-4444	x	x	x	x	x
RGB16-565	x	x	x	x	x
xRGB16-1555	x	x	x	x	x
ARGB16-1555	x	x	x	x	x
xRGB24-8888	x	x	x	x	x
RGBx24-8888	x	x	x	x	
RGB24-888	x	x	x	x	x
ARGB32-8888	x	x	x	x	x
RGBA32-8888	x	x	x	x	x
BGRA32-8888	x	x	x	x	x
UYUV4:2:2		x	x	x	x
YUV2 4:2:2		x	x	x	x
YUV4:2:0 – NV12		x	x	x	x
YUV4:2:0 – NV21		x	x	x	x

- BITMAP 1-bpp data memory organization (CLUT)



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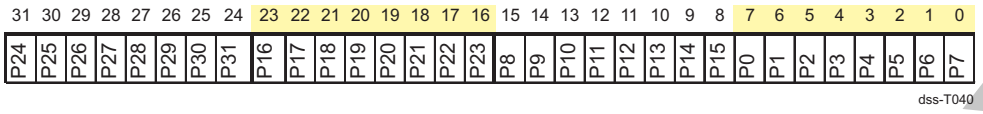
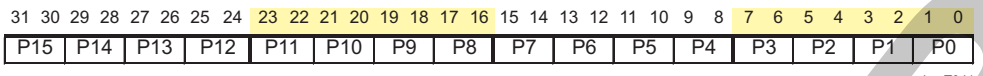
- BITMAP 1-bpp data memory organization (CLUT) in nibble mode



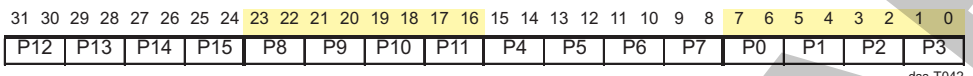
dss-T040

- BITMAP 2-bpp data memory organization (CLUT)



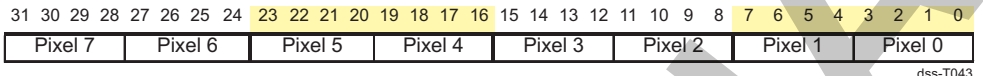
dss-T041

- BITMAP 2-bpp data memory organization (CLUT) in nibble mode



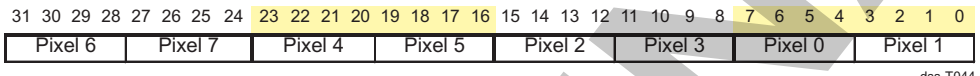
dss-T042

- BITMAP 4-bpp data memory organization (CLUT)



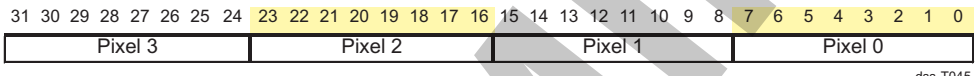
dss-T043

- BITMAP 4-bpp data memory organization (CLUT) in nibble mode



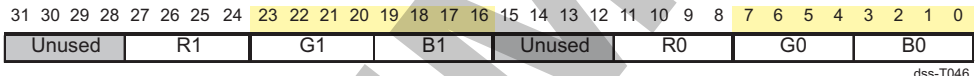
dss-T044

- BITMAP 8-bpp data memory organization (CLUT)



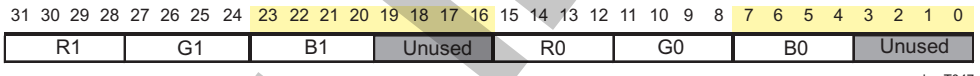
dss-T045

- xRGB12-4444 bpp data memory organization



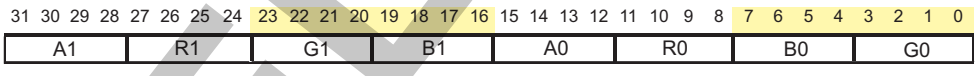
dss-T046

- RGBx12-4444 bpp data memory organization



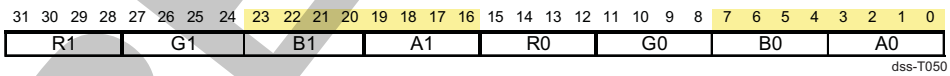
dss-T047

- ARGB16-4444 bpp data memory organization



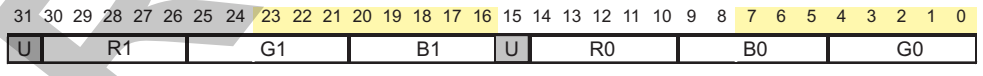
dss-T048

- RGBA16-4444 bpp data memory organization



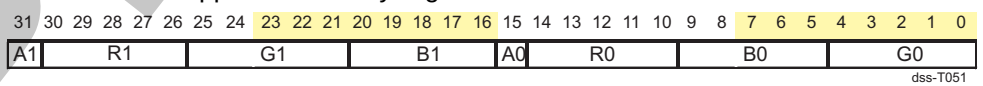
dss-T050

- xRGB16-1555 bpp data memory organization



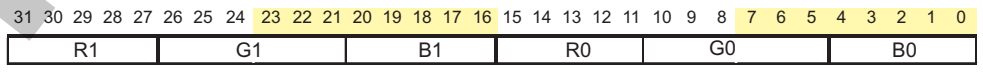
dss-T062

- ARGB16-1555 bpp data memory organization



dss-T051

- RGB16-565 bpp data memory organization



dss-T052

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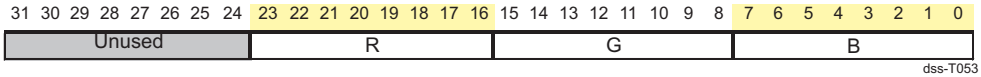
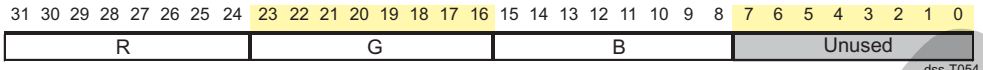
- xRGB24-8888 bpp data memory organization



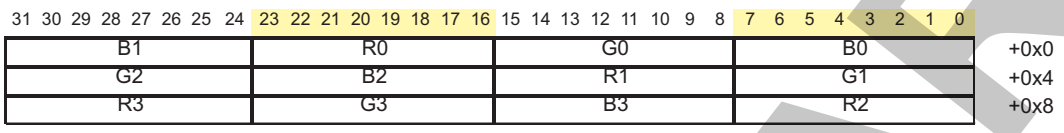
dss-T053

- RGBx24-8888 bpp data memory organization



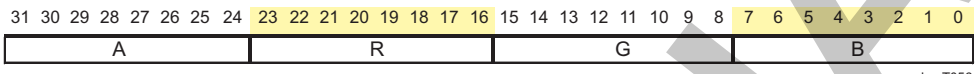
dss-T054

- RGB24-888 bpp packed data memory organization



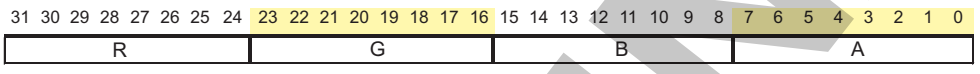
dss-T055

- ARGB32-8888 bpp data memory organization



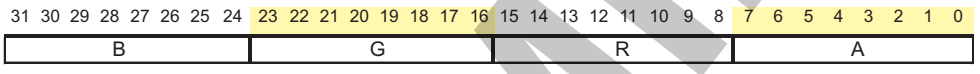
dss-T056

- RGBA32-8888 bpp data memory organization



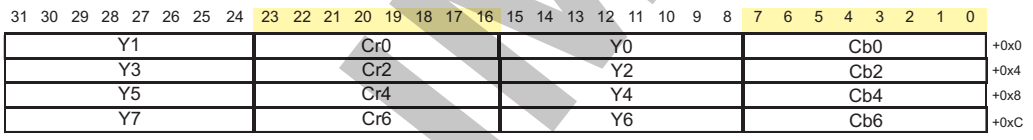
dss-T057

- BGRA32-8888 bpp data memory organization



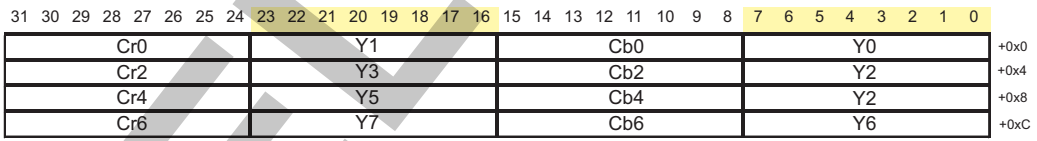
dss-T058

- UYVY4:2:2 data memory organization



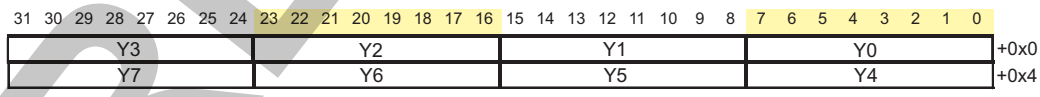
dss-T059

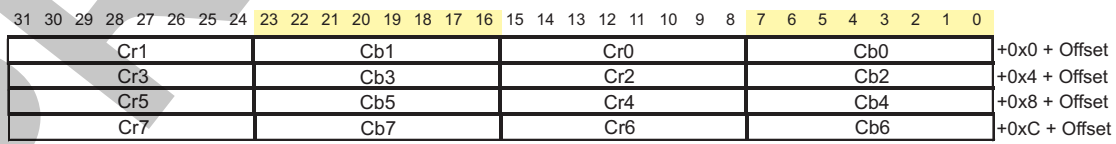
- YUV2 4:2:2 data memory organization



dss-T060

- YUV4:2:0-NV12 data memory organization (same for YUV4:2:0-NV12 with only UV in reverse order)





dss-T061

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10.2.4.9 DISPC Graphics Pipeline

The graphics pipeline is connected to the GFX FIFO for the input port and to the four overlay managers for the output or WB pipeline. The pixel output is directed to an LCD, TV, or WB path by setting the DISPC_GFX_ATTRIBUTES[8] CHANNELOUT bit and the DISPC_GFX_ATTRIBUTES[31:30] CHANNELOUT2 bit field. Table 10-48 lists the bit field settings to orient a pipeline to an LCD, TV, or WB output. The default value directs the GFX pipeline to LCD1. The GFX pipeline can be enabled by setting the DISPC_GFX_ATTRIBUTES[0] ENABLE bit to 0x1.

NOTE: It is not possible to change the direction of the GFX pipeline on the fly. If the graphics pipeline must be connected to an overlay manager different from the one to which it is currently connected, then the following steps must be performed:

1. Disable the GFX pipeline by setting the DISPC_GFX_ATTRIBUTES[0] ENABLE bit to 0x0.
2. Direct the GFX pipeline to the new overlay manager by modifying the DISPC_GFX_ATTRIBUTES[8] CHANNELOUT and [31:30] CHANNELOUT2 bits.
3. Disable the DISPC output which corresponds with the overlay manager to which the GFX pipeline will be connected next. This is done by setting the in the following bits to 0x0 for the listed outputs:
   - The DISPC_CONTROL1[0] LCDENABLE bit for LCD1 output
   - The DISPC_CONTROL2[0] LCDENABLE bit for LCD2 output
   - The DISPC_CONTROL3[0] LCDENABLE bit for LCD3 output
   - The DISPC_CONTROL1[1] TVENABLE bit for TV output
4. Enable the GFX pipeline by setting the DISPC_GFX_ATTRIBUTES[0] ENABLE bit to 0x1.
5. Enable the DISPC output that corresponds with the overlay manager to which the GFX pipeline will be connected. This is done by setting the following bits to 0x1 for the listed outputs:
   - The DISPC_CONTROL1[0] LCDENABLE bit for LCD1 output
   - The DISPC_CONTROL2[0] LCDENABLE bit for LCD2 output
   - The DISPC_CONTROL3[0] LCDENABLE bit for LCD3 output
   - The DISPC_CONTROL1[1] TVENABLE bit for TV output

The pipeline consists of programmable replication logic, an antiflicker filter, and one 256-entry palette table. The replication logic is used to convert the RGB pixel formats into an ARGB40-based format. The antiflicker filter processes the graphics data in RGB format to remove some of the vertical flicker. The 256-entry palette is used to convert bitmap formats into RGB formats or for gamma corrections when RGB format is inputted.

Table 10-30 lists the input formats supported by the graphics pipeline.

Figure 10-35 shows the graphics pipeline.

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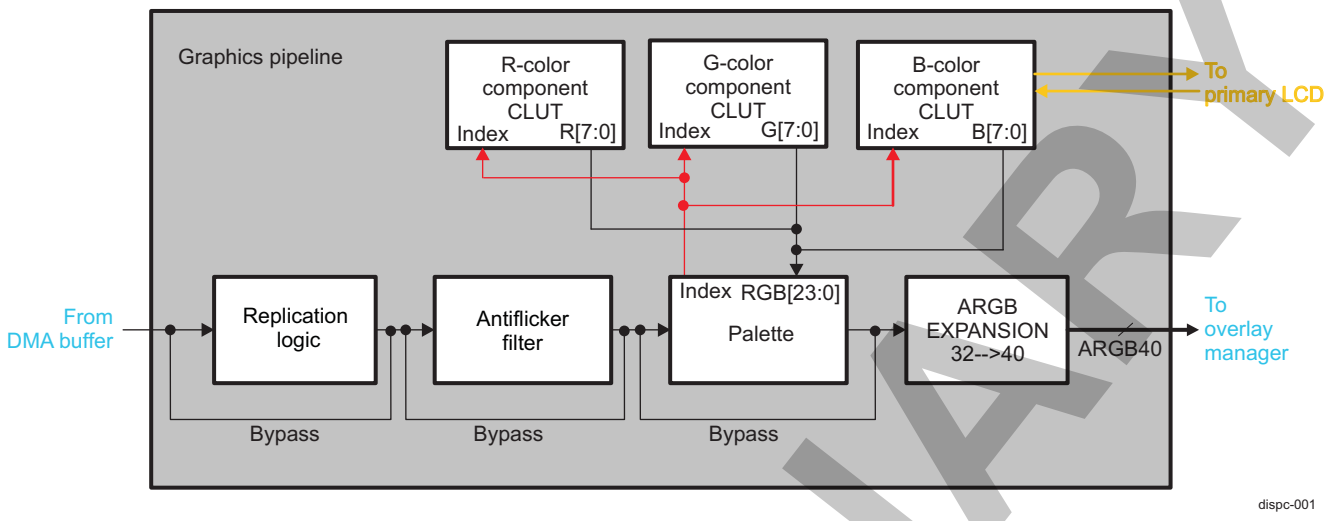
Figure 10-35. DISPC Graphics Pipeline



10.2.4.9.1 DISPC Replication Logic

The replication logic increases the color depth of the graphics-encoded pixels (from true color RGB 12, and 16 to 40 bpp).

- When the replication logic is enabled by setting the DISPC_GFX_ATTRIBUTES[5] REPLICATIONENABLE bit to 0x1, the MSBs are copied to the missing LSB. Table 10-31 describes the remapping of the RGB pixels into ARGB 40-bit values.

Table 10-31. DISPC Replication Enabled: RGB Pixel Formats Remapping Into ARGB40-10.10.10.10

	A[9:0]	R[9:0]	G[9:0]	B[9:0]
Format	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
xRGB12-4444	1111111111	R[3:0]R[3:0]R[3:2]	G[3:0]G[3:0]G[3:2]	B[3:0]B[3:0]B[3:2]
RGBx12-4444	1111111111	R[3:0]R[3:0]R[3:2]	G[3:0]G[3:0]G[3:2]	B[3:0]B[3:0]B[3:2]
RGB16-565	1111111111	R[4:0]R[4:0]	G[5:0]G[5:2]	B[4:0]B[4:0]
xRGB16-1555	1111111111	R[4:0]R[4:0]	G[4:0]G[4:0]	B[4:0]B[4:0]
ARGB16-1555	AAAAAAAAAA	R[4:0]R[4:0]	G[4:0]G[4:0]	B[4:0]B[4:0]
ARGB16-4444	A[3:0]A[3:0]A[3:2]	R[3:0]R[3:0]R[3:2]	G[3:0]G[3:0]G[3:2]	B[3:0]B[3:0]B[3:2]
RGBA16-4444	A[3:0]A[3:0]A[3:2]	R[3:0]R[3:0]R[3:2]	G[3:0]G[3:0]G[3:2]	B[3:0]B[3:0]B[3:2]

- When the replication logic is disabled by setting the DISPC_GFX_ATTRIBUTES[5] REPLICATIONENABLE bit to 0x0, the encoded pixel values are shifted to the MSB boundary of the 24-bit format. The missing bit values are filled with 0s. Table 10-32 describes the remapping of the RGB pixels into ARGB 40-bit values.

Table 10-32. DISPC Replication Disabled: RGB Pixel Formats Remapping Into ARGB40-10.10.10.10

	A[7:0]	R[7:0]	G[7:0]	B[7:0]
Format	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
xRGB12-4444	1111111111	R[3:0]000000	G[3:0]000000	B[3:0]000000
RGBx12-4444	1111111111	R[3:0]000000	G[3:0]000000	B[3:0]000000
RGB16-565	1111111111	R[4:0]00000	G[5:0]0000	B[4:0]00000
xRGB16-1555	1111111111	R[4:0]00000	G[4:0]00000	B[4:0]00000
ARGB16-1555	AAAAAAAAAA	R[4:0]00000	G[4:0]00000	B[4:0]00000
ARGB16-4444	A[3:0]A[3:0]A[3:2]	R[3:0]000000	G[3:0]000000	B[3:0]000000

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Table 10-32. DISPC Replication Disabled: RGB Pixel Formats Remapping Into ARGB40-10.10.10.10 (continued)

	A[7:0]	R[7:0]	G[7:0]	B[7:0]
Format	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
RGBA16-4444	A[3:0]A[3:0]A[3:2]	R[3:0]000000	G[3:0]000000	B[3:0]000000

10.2.4.9.2 DISPC Antiflicker Filter

The antiflicker filter processes the graphics data to remove some of the vertical flicker. It is based on a 3-tap FIR filter with fixed coefficients. For each pixel to be output from the graphics pipeline, the pixel above and below the current line must be read from the DMA graphics FIFO. Therefore, three lines of pixels must be stored in the DMA graphics FIFO.

The antiflickering equations for A, R, G, and B components are:

$A_{out}(x,y) = 0.25 \times A_{in}(x,y-1) + 0.5 \times A_{in}(x,y) + 0.25 \times A_{in}(x,y+1)$

$R_{out}(x,y) = 0.25 \times R_{in}(x,y-1) + 0.5 \times R_{in}(x,y) + 0.25 \times R_{in}(x,y+1)$

$G_{out}(x,y) = 0.25 \times G_{in}(x,y-1) + 0.5 \times G_{in}(x,y) + 0.25 \times G_{in}(x,y+1)$

$B_{out}(x,y) = 0.25 \times B_{in}(x,y-1) + 0.5 \times B_{in}(x,y) + 0.25 \times B_{in}(x,y+1)$

For the first line of processing, because there is no pixel above, the value (x,y) is duplicated.

$Out(x,y) = 0.25 \times In(x,y) + 0.5 \times In(x,y) + 0.25 \times In(x,y+1)$

For the last line of processing, because there is no pixel below, the value (x,y) is duplicated.

$Out(x,y) = 0.25 \times In(x,y-1) + 0.5 \times In(x,y) + 0.25 \times In(x,y)$

NOTE: Antiflicker filtering is supported only in RGB formats and not in BITMAP formats.

Antiflickering is not supported for pictures with fewer than two lines. In this case, the user must disable the antiflickering processing.

By default, the antiflicker filtering is disabled. It can be enabled by setting the DISPC_GFX_ATTRIBUTES[24] ANTIFLICKER bit to 0x1.

10.2.4.9.3 DISPC Color Look-Up Table (CLUT)

The graphics pipeline supports conversion of the BITMAP formats into RGB24 formats through a palette table. To enable palette mode, the DISPC_CONFIG1[3] PALETTEGAMMATABLE bit must be set to 0x0. Figure 10-36 shows the internal architecture of the color look-up/gamma table.

The palette is split into three memories of 256-bit × 8-bit entries. For bitmap (CLUT) indexes, the same value (1, 2, 4, or 8 bpp) indexes the three memories. The table can be reloaded every frame, once, or never (at the beginning of the frame before fetching pixels for the graphics). The table is loaded dynamically at the beginning of the frame by the DISPC DMA engine. The base address of the table buffer is set in the DISPC_GFX_TABLE_BA[31:0] TABLEBA bit field. It is possible to load the table for every frame or only for a specific frame by setting the DISPC_CONFIG1[2:1] LOADMODE bit field.

The table can be loaded without fetching data for the graphics pipeline. The DMA buffer associated with the graphics pipeline is used to fetch the table from memory. Regardless of the mode (color or monochrome) for each entry into the table, one 32-bit value is fetched from memory.

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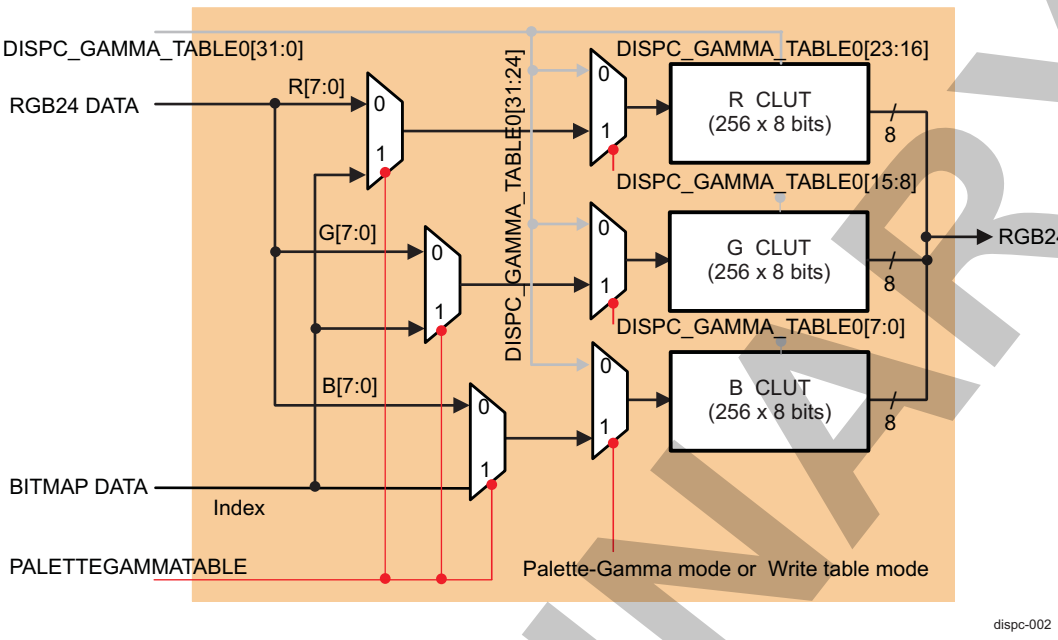
Figure 10-36. DISPC Palette/Gamma Correction Architecture



The palette mode uses the encoded pixel values from the input graphics FIFO as pointers to index the 24-bit-wide palette: 1-bpp pixel address 2 palette entries, 2-bpp pixel address 4 palette entries, 4-bpp pixel address 16 palette entries, and 8-bpp pixel address 256 palette entries. In color mode, the value within the palette consists of three 8-bit fields, one for each color component: red, green, and blue (see Figure 10-37). For a color operation, an individual frame is limited to a selection of 256 colors (the number of palette entries). In monochrome mode, only one 8-bit value is present; 256 grayscales and 16,777,216 colors are obtained after passing through the palette (see Figure 10-38)

Figure 10-37. DISPC Data Memory Organization: Color Mode

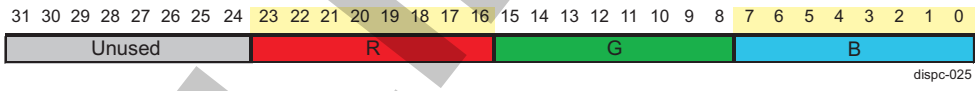
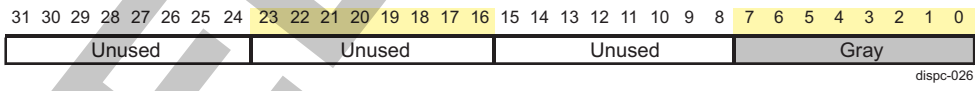


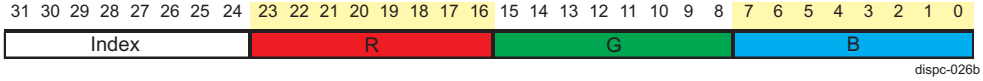
Figure 10-38. DISPC Data Memory Organization: Gray Mode



When a palette entry is selected by the encoded pixel value, the content of the entry and the index are sent to the LCD1 overlay manager.

In gamma curve mode, the selected encoded pixel values based on the color keys by the overlay manager from the video or grahics paths are sent to the gamma curve table. Each component of encoded pixel value is used as a pointer to index 1 out of 256 24-bit gamma curve entries in the table. Each 8-bit component is replaced with the 8-bit table value corresponding to the R, G, or B component. Figure 10-39 describes the format of one of the gamma curve values in the memory.

Figure 10-39. DISPC Data Memory Organization: Gamma Curve 24 BPP



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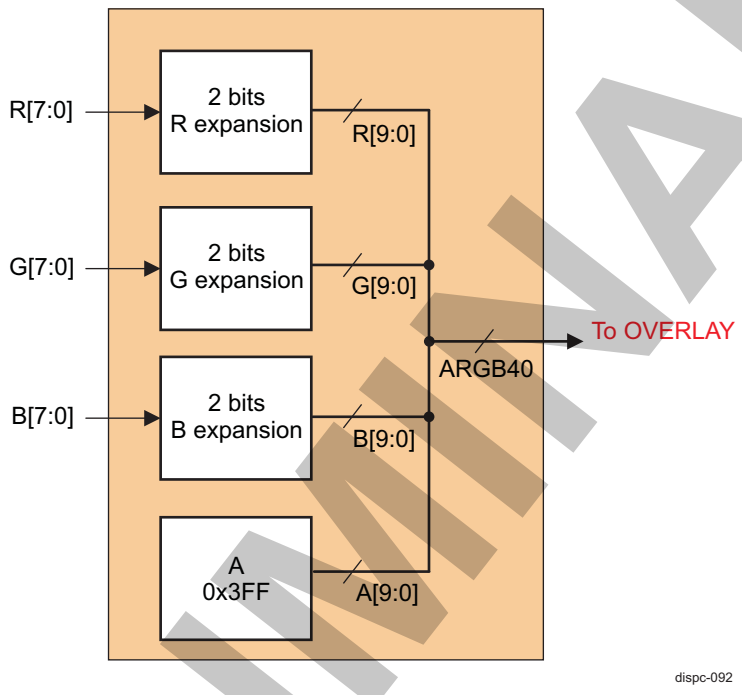
10.2.4.9.4 DISPC Expansion to ARGB40

When the GFX pipeline input data is in an RGB pixel format, the expansion to ARGB40 format is done as described in Section 10.2.4.10.1, *DISPC Replication Logic*.

When the GFX pipeline input data is in BITMAP format, the expansion module input receives the RGB24 pixel format output from the pallette module. The expansion module automatically replicates the 2 MSBs of each color component to create an ARGB40 pixel with the A component set to 0x3FF (see Figure 10-40).

Figure 10-40. DISPC Expansion to ARGB40



10.2.4.10 DISPC Video Pipelines

Three identical video pipelines are available, VID1, VID2, and VID3. Each video pipeline is connected to its video FIFO controller for the input port and to the four overlay managers, LCD1, LCD2, LCD3, and TV or WB pipeline. The pixel output is directed to the LCD, TV, or WB path by setting the DISPC_VIDp_ATTRIBUTES[16] CHANNELOUT bit and the DISPC_VIDp_ATTRIBUTES[31:30] CHANNELOUT2 bit field. Table 10-48 summarizes the bit field settings to orient a pipeline to LCD, TV, or WB output. The default value directs all video pipelines to LCD1.

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NOTE: It is not possible to change the direction of the video pipelines on the fly. If a video pipeline needs to be connected to a different overlay manager than what it is currently connected, then the following steps need to be performed:

1. Disable the VIDp pipeline by setting the DISPC_VIDp_ATTRIBUTES[0] ENABLE bit to 0x0.
2. Direct the VIDp pipeline to the new overlay manager by modifying the [16] CHANNELOUT bit and the [31:30] CHANNELOUT2 bit in the DISPC_VIDp_ATTRIBUTES register.
3. Disable the DISPC output that corresponds with the overlay manager to which the VIDp pipeline will be connected next. This is done by setting the following bits to 0x0 for the listed outputs:
   - The DISPC_CONTROL1[0] LCDENABLE bit for LCD1 output
   - The DISPC_CONTROL2[0] LCDENABLE bit for LCD2 output
   - The DISPC_CONTROL3[0] LCDENABLE bit for LCD3 output
   - The DISPC_CONTROL1[1] TVENABLE bit for TV output
4. Enable the VIDp pipeline by writing 0x1 to the DISPC_VIDp_ATTRIBUTES [0] ENABLE bit.
5. Enable the DISPC output that corresponds with the overlay manager to which the VIDp pipeline will be connected next. This is done by setting the following bits to 0x1 for the listed outputs:
   - The DISPC_CONTROL1[0] LCDENABLE bit for LCD1
   - The DISPC_CONTROL2[0] LCDENABLE bit for LCD2 output
   - The DISPC_CONTROL3[0] LCDENABLE bit for LCD3 output
   - The DISPC_CONTROL1[1] TVENABLE bit for TV output

A video pipeline consists of a scaler unit, color space conversion (CSC) unit, VC-1 range mapping unit, and some programmable replication logic. The order of the video pipeline unit can be configured in two manners (see Figure 10-41 and Figure 10-42):

- Configuration 1 (YUVCHROMARESAMPLING = 0): VC-1 range mapping unit followed by a CSC unit and then a scaler unit. The configuration is used to support RGB, ARGB, and RGBA formats and YUV4:2:2 in backward mode for both data types. Each block can be independently bypassed.
- Configuration 2 (YUVCHROMARESAMPLING = 1): VC-1 range mapping unit followed by a scaler unit and then a CSC unit. The configuration is used to support RGB, ARGB, and RGBA formats and YUV4:2:2, YUV420-NV12, and YUV420-NV21 formats, taking advantage of the scaler to resample the chrominance using five taps horizontally and three or five taps vertically. Each block can be independently bypassed.

The DISPC_VIDn_ATTRIBUTES2[8] YUVCHROMARESAMPLING bit controls the order of the scaler unit in the video pipeline:

- When the YUVCHROMARESAMPLING bit is set to 0x0, the video pipeline is in configuration 1, and the scaler comes after the CSC unit. In case of YUV input data in 4:2:2 format, the chrominance resampling (4:2:2 to 4:4:4 format) is done by averaging the chrominance adjacent samples for only 0 degrees (zero rotation), because other rotation (90/180/270 degrees) is not supported in this mode. For more information about the supported chrominance resampling methods, see Section 10.2.4.10.3.1, *Chrominance Resampling*.
- When the YUVCHROMARESAMPLING bit is set to 0x1, the video pipeline is in configuration 2, and the scaler comes before the CSC unit.
  - In case of YUV4:2:2 input data with 90-/270-degree rotation, the data is preprocessed by duplicating the missing chrominance samples.
  - In case of YUV4:2:2 input data with 0-/180-degree rotation, the Chroma upsampling is performed in the scaler unit.

Table 10-30 lists the input formats supported by the video pipelines.

The video pipeline is enabled by setting the DISPC_VIDp_ATTRIBUTES[0] ENABLE bit to 0x1.

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Figure 10-41. DISPC Configuration 1: Video Pipeline

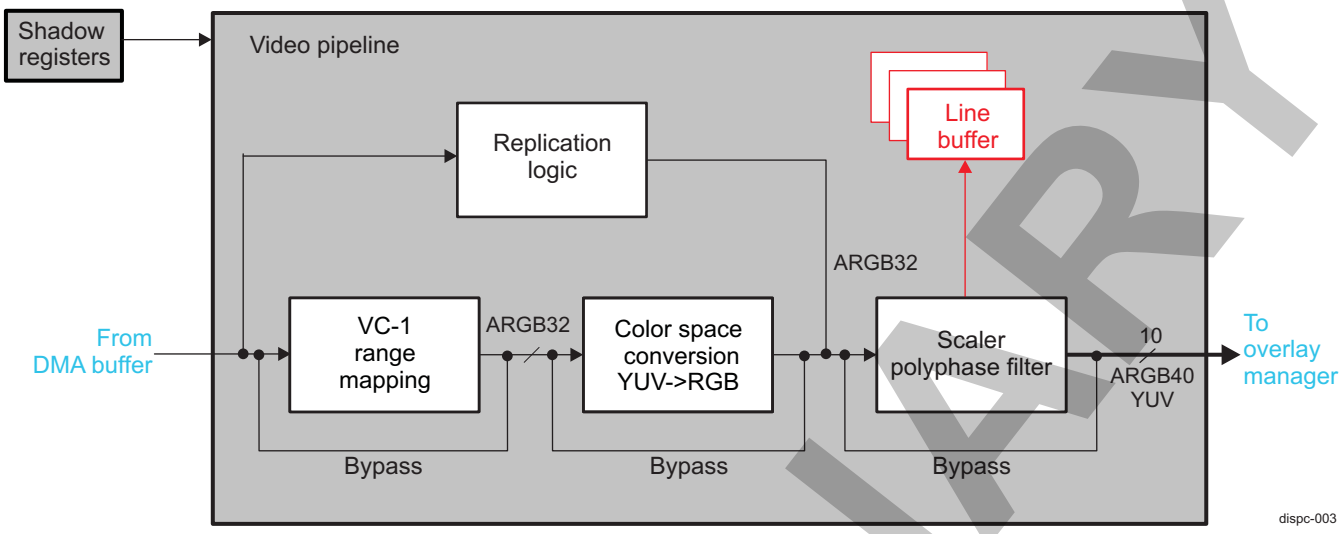
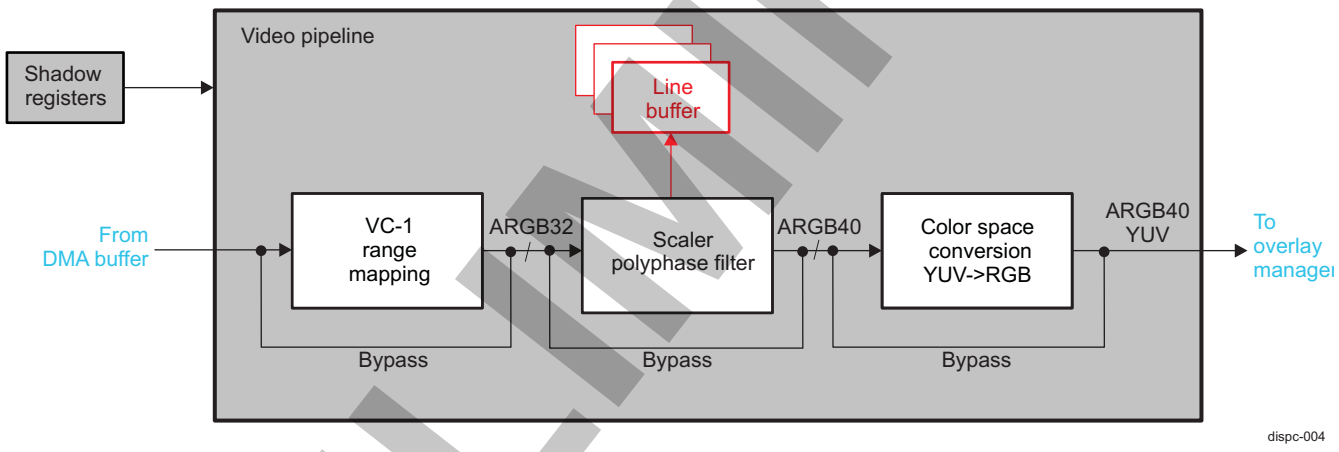


Figure 10-42. DISPC Configuration 2: Video Pipeline



10.2.4.10.1 DISPC Replication Logic

The replication logic increases the color depth of the video-encoded pixels (from true color RGB 12, and 16 to 32 bpp) available only in configuration 1.

The expansion from 8- to 10-bit color component is done by the following units:

- The CSC unit, when the scaler is after the CSC module and when the vertical scaler is disabled
- The vertical scaler, when the scaler is after the CSC unit and enabled
- The replication bit module, when the CSC unit and scaler are disabled
- When the replication logic is enabled by setting the DISPC_VIDp_ATTRIBUTES[10] REPLICATIONENABLE bit to 0x1, the MSBs are copied to the missing LSBs. Table 10-33 describes the remapping of the RGB pixels into ARGB 32-bit values.

Table 10-33. DISPC Replication Enabled: RGB Pixel Formats Remapping Into ARGB32-8888

	A[7:0]	R[7:0]	G[7:0]	B[7:0]
Formats	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
xRGB12-4444	11111111	R[3:0]R[3:0]	G[3:0]G[3:0]	B[3:0]B[3:0]
RGBx12-4444	11111111	R[3:0]R[3:0]	G[3:0]G[3:0]	B[3:0]B[3:0]

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Table 10-33. DISPC Replication Enabled: RGB Pixel Formats Remapping Into ARGB32-8888 (continued)

	A[7:0]	R[7:0]	G[7:0]	B[7:0]
Formats	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
RGB16-565	11111111	R[4:0]R[4:2]	G[5:0]G[5:4]	B[4:0]B[4:2]
xRGB16-1555	11111111	R[4:0]R[4:2]	G[4:0]G[4:2]	B[4:0]B[4:2]
ARGB16-1555	AAAAAAAA	R[4:0]R[4:2]	G[4:0]G[4:2]	B[4:0]B[4:2]
ARGB16-4444	A[3:0]A[3:0]	R[3:0]R[3:0]	G[3:0]G[3:0]	B[3:0]B[3:0]
RGBA16-4444	A[3:0]A[3:0]	R[3:0]R[3:0]	G[3:0]G[3:0]	B[3:0]B[3:0]

- When the replication logic is disabled by setting the DISPC_VIDp_ATTRIBUTES[10] REPLICATIONENABLE bit to 0x0, the encoded pixel values are shifted to the MSB boundary of the 24-bit format. The missing bit values are filled with 0s. Table 10-34 describes the remapping of the RGB pixels into ARGB 32-bit values.

Table 10-34. DISPC Replication Disabled: RGB Pixel Formats Remapping Into ARGB32-8888

	A[7:0]	R[7:0]	G[7:0]	B[7:0]
Formats	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
xRGB12-4444	11111111	R[3:0]0000	G[3:0]0000	B[3:0]0000
RGBx12-4444	11111111	R[3:0]0000	G[3:0]0000	B[3:0]0000
RGB16-565	11111111	R[4:0]000	G[5:0]00	B[4:0]000
xRGB16-1555	11111111	R[4:0]000	G[4:0]000	B[4:0]000
ARGB16-1555	AAAAAAAA	R[4:0]000	G[4:0]000	B[4:0]000
ARGB16-4444	A[3:0]A[3:0]	R[3:0]0000	G[3:0]0000	B[3:0]0000
RGBA16-4444	A[3:0]A[3:0]	R[3:0]0000	G[3:0]0000	B[3:0]0000

10.2.4.10.2 DISPC VC-1 Range Mapping Unit

The VC-1 range mapping unit is used when the video frame picture is decoded using a VC-1 codec by the video accelerator. It remaps the Y, Cb, and Cr components. The unit is used primarily for YUV4:2:0-NV12 and YUV4:2:0-NV21 pixel formats but also can be applied to YUV4:2:2 pixel formats (YUV2 and UYVY).

The VC-1 range mapping unit is enabled by setting the DISPC_VIDp_ATTRIBUTES2[0] VC1ENABLE bit to 0x1. The DISPC_VIDp_ATTRIBUTES2[3:1] VC1_RANGE_Y and DISPC_VIDp_ATTRIBUTES2[6:4] VC1_RANGE_CBCR bit fields are two 3-bit values programmed by the user and are independent for each video pipeline. The module is governed by the equations:

$Y_{out} = CLIP(((Y_{int} – 128) \times (VC1\_RANGE\_Y + 9) + 4) / 8) + 128)$

$C_b = CLIP(((C_b – 128) \times (VC1\_RANGE\_CBCR + 9) + 4) / 8) + 128)$

$C_r = CLIP(((C_r – 128) \times (VC1\_RANGE\_CBCR + 9) + 4) / 8) + 128)$

NOTE: The input and output pixel values are unsigned (Y, Cr, and Cb).

The function CLIP () clips to 0 or 255 when minimum or maximum, respectively, are reached; otherwise, the resulting output remains identical.

10.2.4.10.3 DISPC CSC Unit YUV to RGB

The CSC unit converts the video-encoded pixel values from YUV4:4:4 format into RGB24 or RGB30 format. The output format depends on the video pipeline configuration selected:

- Configuration 1: RGB24 output format, with 8-bit value per component: red, green, and blue
- Configuration 2: RGB30 output format, with 10-bit value per component: red, green, and blue

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In case of YUV4:2:0 or YUV4:2:2 formats, a chrominance resampling to YUV4:4:4 is required before converting the YUV into RGB values (see Section 10.2.4.10.3.1, *Chrominance Resampling*). YUV4:2:2 or YUV4:2:0 to YUV4:4:4 chrominance resampling is a preprocessing to the color space conversion.

Figure 10-43 through Figure 10-46 show the 3 × 3 11-bit coefficients used to convert from YUV4:4:4 into RGB24. The coefficients are set according to the standard used to encode the pixel data in YUV color space. Table 10-35 summarizes the coefficients with their respective bit fields.

Table 10-35. DISPC Color Space Conversion YUV to RGB Bit Field Setting

Coefficients	Bit Field Registers
R_Y	DISPC_VIDp_CONV_COEF0[10:0] RY
R_{Cr}	DISPC_VIDp_CONV_COEF0[26:16] RCR
R_{Cb}	DISPC_VIDp_CONV_COEF1[10:0] RCB
G_Y	DISPC_VIDp_CONV_COEF1[26:16] GY
G_{Cr}	DISPC_VIDp_CONV_COEF2[10:0] GCR
G_{Cb}	DISPC_VIDp_CONV_COEF2[26:16] GCB
B_Y	DISPC_VIDp_CONV_COEF3[10:0] BY
B_{Cr}	DISPC_VIDp_CONV_COEF3[26:16] BCR
B_{Cb}	DISPC_VIDp_CONV_COEF4[10:0] BCB

- For configuration 1 with an RGB24 output:

  If the active range for the luminance samples (Y) is [235:16] and [240:16] for the chrominance samples (Cb and Cr), the range selection is done by setting the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit to 0x0. The values of R, G, and B output components are clipped to the range [255:0].

NOTE: The scaling and CSC clipping is set by the same bit, DISPC_VIDp_ATTRIBUTES[11] FULLRANGE.

Figure 10-43. DISPC YCbCr to RGB Registers (FULLRANGE = 0), 8-Bit Outputs

$$\begin{bmatrix} R_{OUT} \\ G_{OUT} \\ B_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} R_Y & R_{cr} & R_{cb} \\ G_Y & G_{cr} & G_{cb} \\ B_Y & B_{cr} & B_{cb} \end{bmatrix} * \begin{bmatrix} Y_{IN} - 16 \\ Cr_{IN} - 128 \\ Cb_{IN} - 128 \end{bmatrix}$$

dispc-005

If the active range for the luminance samples (Y) and chrominance samples (Cb and Cr) is [255:0], the range selection is done by setting the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit to 0x1. The values of R, G, and B output components are clipped to the range [255:0].

Figure 10-44. DISPC YCbCr to RGB Registers (FULLRANGE = 1), 8-Bit Outputs

$$\begin{bmatrix} R_{OUT} \\ G_{OUT} \\ B_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} R_Y & R_{cr} & R_{cb} \\ G_Y & G_{cr} & G_{cb} \\ B_Y & B_{cr} & B_{cb} \end{bmatrix} * \begin{bmatrix} Y_{IN} \\ Cr_{IN} - 128 \\ Cb_{IN} - 128 \end{bmatrix}$$

dispc-006

- For configuration 2 with an RGB30 output:

  If the active range for the luminance samples (Y) is [940:64] and [960:64] for the chrominance samples (Cb and Cr), the range selection is done by setting the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit to 0x0. The values of R, G, and B output components are clipped to the range [1023:0].

NOTE: The scaling and CSC clipping is set by the same bit, DISPC_VIDp_ATTRIBUTES[11] FULLRANGE.

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Figure 10-45. DISPC YCbCr to RGB Registers (FULLRANGE = 0), 10-Bit Outputs

$$\begin{bmatrix} R_{OUT} \\ G_{OUT} \\ B_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} R_Y & R_{cr} & R_{cb} \\ G_Y & G_{cr} & G_{cb} \\ B_Y & B_{cr} & B_{cb} \end{bmatrix} * \begin{bmatrix} Y_{IN} - 64 \\ Cr_{IN} - 512 \\ Cb_{IN} - 512 \end{bmatrix}$$

dispc-074

If the active range for the luminance samples (Y) and chrominance samples (Cb and Cr) is [1023:0], the range selection is done by setting the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit to 0x1. The values of R, G, and B output components are clipped to the range [1023:0].

Figure 10-46. DISPC YCbCr to RGB Registers (FULLRANGE = 1), 10-Bit Outputs

$$\begin{bmatrix} R_{OUT} \\ G_{OUT} \\ B_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} R_Y & R_{cr} & R_{cb} \\ G_Y & G_{cr} & G_{cb} \\ B_Y & B_{cr} & B_{cb} \end{bmatrix} * \begin{bmatrix} Y_{IN} \\ Cr_{IN} - 512 \\ Cb_{IN} - 512 \end{bmatrix}$$

dispc-075

10.2.4.10.3.1 DISPC Chrominance Resampling

Two methods are supported to resample chrominance:

- Averaging of the chrominance is done by software, followed by hardware conversion when the video pipeline is in configuration 1.
- Filtering of the chrominance using the scaler unit (chrominance resampling and rescaling can be combined to support native rescaling of YUV format) when the video pipeline is in configuration 2.

To convert the YUV4:2:2 encoded pixel values into YUV4:4:4 format, the averaging of the chrominance technique can be used as shown in Figure 10-47. The missing chrominance samples (Cb and Cr) are interpolated using the average values of the two closest values on the same line (,) or are repeated from the second pixel in the same 32-bit container (see Figure 10-48). For the last pixel, the chrominance samples are duplicated using the values from the previous pixel; otherwise, the chrominance samples are averaged using the two adjacent values. Figure 10-49 shows the flow of the pixel.

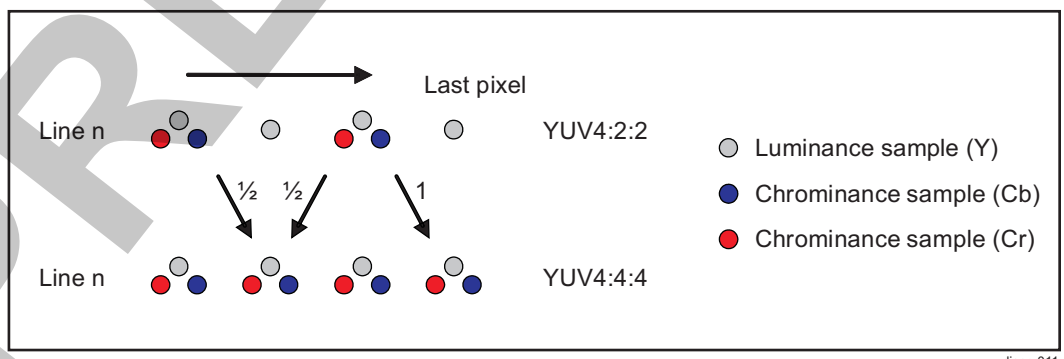
Figure 10-47. DISPC Averaging of the Chrominance Formula

$$Cb_n(YCbCr\ 444) = \frac{Cb_{n-1}(YCbCr\ 422) + Cb_{n+1}(YCbCr\ 422)}{2}\ (\text{n odd})$$

$$Cr_n(YCbCr\ 444) = \frac{Cr_{n-1}(YCbCr\ 422) + Cr_{n+1}(YCbCr\ 422)}{2}\ (\text{n odd})$$

dispc-010

Figure 10-48. DISPC Averaging of the Chrominance Representation



dispc-011

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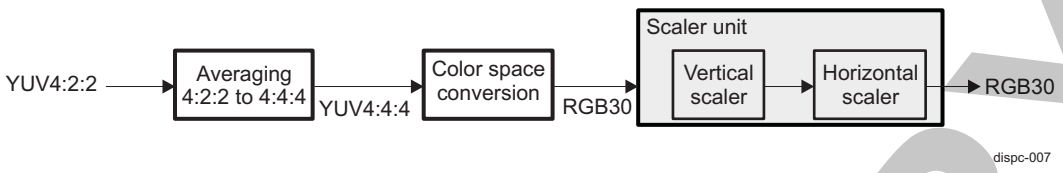
Figure 10-49. DISPC YUV4:2:2 to RGB30 Using Averaging of the Chrominance



The scaler unit can be used to resample the chrominance of YUV4:2:0 and YUV4:2:2, as shown in Figure 10-50 and Figure 10-51, respectively. The settings of the scaler unit to perform chrominance resampling are described in Section 10.2.4.10.4, *DISPC Scaler Unit*.

Figure 10-50. DISPC YUV4:2:0 to RGB30 Using Scaler Unit for Resampling Chrominance

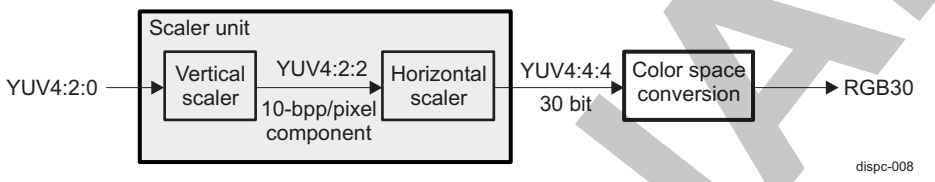
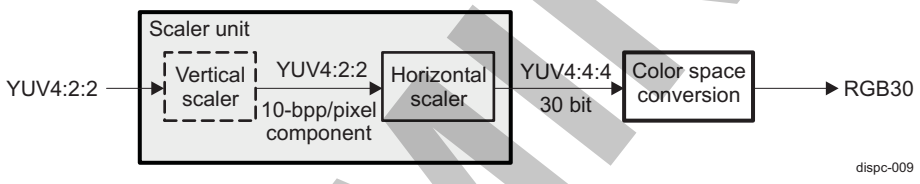


Figure 10-51. DISPC YUV4:2:2 to RGB30 Using Scaler Unit for Resampling Chrominance



NOTE: If rotation must be supported, YUV4:2:2 and YUV4:2:0 (0-/180-degree rotation) chrominance resampling is done as shown in Figure 10-51 and Figure 10-50, respectively.
For YUV4:2:2 (90-/270-degree rotation) data are preprocessed to present YUV4:4:4 on the scaler input (duplication of the missing chroma), as shown in Figure 10-49.

10.2.4.10.4 DISPC Scaler Unit

All video formats are supported, including formats with alpha blending. Alpha blending is scaled with the same parameters as RGB color components. For the YUV formats, Y and Cb/Cr are processed independently. The filter is based on a finite impulse response (FIR) filter. The filtering can be used for different processing:

- Upsampling of the picture
- Downsampling of the picture
- Antiflicker reduction
- De-interlacing using bob algorithm
- Chrominance resampling in case of YUV data formats

NOTE: The user must ensure that the resizing frame displays in the LCD/screen boundaries.

Figure 10-52 shows an example of video upsampling.

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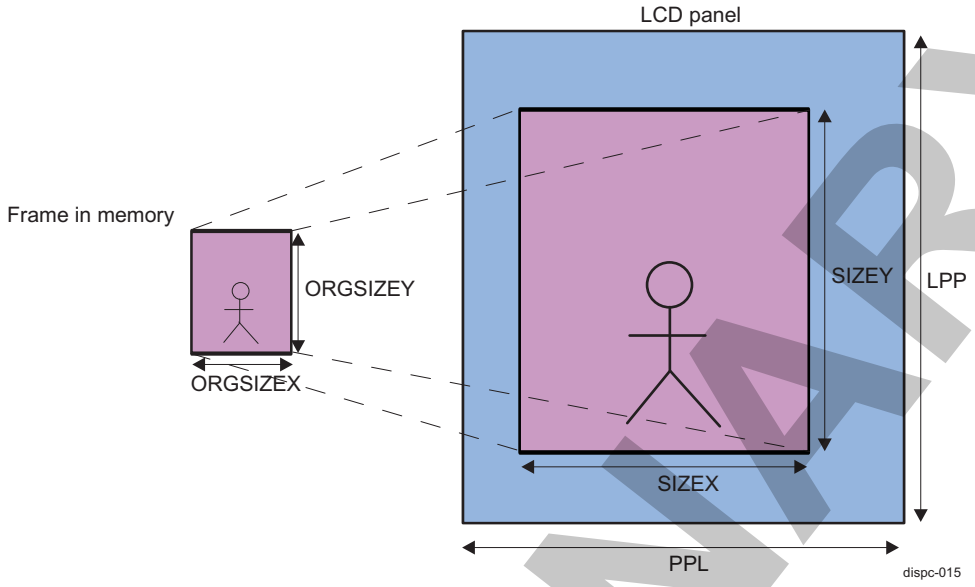
Figure 10-52. DISPC Video Upsampling



The upsampling and downsampling filter is a polyphase filter with five taps and eight phases for the horizontal filter, and a programmable number of taps (three or five) and eight phases for vertical filter. The input buffer has five input memory lines. The following limitations must be considered:

- The upsampling ratio is up to x8.
- The downsampling ratio using 3-tap configuration is down to x0.5 for RGB format.
- The downsampling ratio using 5-tap configuration is down to x0.25 for RGB format.
- If the input format is changed from YUV4:2:2 to YUV4:2:0 (WB pipeline), the downsampling ratio is further reduced:
  - Using 5-tap configuration, the ratio is down to x0.5 for RGB format.
  - Using 3-tap configuration, no downscaling is available.

For vertical upsampling and downsampling in a 3-tap configuration, the equations are:

For RGB formats

$$A_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi)*A_{in}(n+i))>>5$$

$$R_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi)*R_{in}(n+i))>>5$$

$$G_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi)*G_{in}(n+i))>>5$$

$$B_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi)*B_{in}(n+i))>>5$$

For YUV formats

$$Y_{out}(n)=(\sum_{i=-1}^{i=1} C_{vi}(\Phi_y)*Y_{in}(n+i))>>5$$

$$Cr_{out}(n)=(\sum_{i=-1}^{i=1} C_{vci}(\Phi_c)*Cb_{in}(n+i))>>5$$

$$Cb_{out}(n)=(\sum_{i=-1}^{i=1} C_{vci}(\Phi_c)*Cr_{in}(n+i))>>5$$

dispc-013

(7)

For vertical upsampling and downsampling in a 5-tap configuration, the equations are:

For RGB formats

$$A_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi)*A_{in}(n+i))>>5$$

$$R_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi)*R_{in}(n+i))>>5$$

$$G_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi)*G_{in}(n+i))>>5$$

$$B_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi)*B_{in}(n+i))>>5$$

For YUV formats

$$Y_{out}(n)=(\sum_{i=-2}^{i=2} C_{vi}(\Phi_y)*Y_{in}(n+i))>>5$$

$$Cb_{out}(n)=(\sum_{i=-2}^{i=2} C_{vci}(\Phi_c)*Cb_{in}(n+i))>>5$$

$$Cr_{out}(n)=(\sum_{i=-2}^{i=2} C_{vci}(\Phi_c)*Cr_{in}(n+i))>>5$$

dispc-012

(8)

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For horizontal upsampling and downsampling in a 5-tap configuration, the equations are:

For RGB formats

$$A_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi)*A_{in}(n+i)\right)>>7$$

$$R_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi)*R_{in}(n+i)\right)>>7$$

$$G_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi)*G_{in}(n+i)\right)>>7$$

$$B_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi)*B_{in}(n+i)\right)>>7$$

For YUV formats

$$Y_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hi}(\Phi_y)*Y_{in}(n+i)\right)>>7$$

$$Cb_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hci}(\Phi_c)*Cb_{in}(n+i)\right)>>7$$

$$Cr_{out}(n)=\left(\sum_{i=-2}^{i=2} C_{hci}(\Phi_c)*Cr_{in}(n+i)\right)>>7$$

dispc-014 (9)

NOTE: The pixel (n + 1) is the previous pixel with respect to pixel (n). The line (n + 1) is the previous line with respect to line (n).

The coefficients Ci() depend on the phase between input and output pixels.

NOTE: The coefficients are different for Y and Cr, Cb filtering because the calculations are independent due to the chrominance resampling for YUV4:2:2 and YUV4:2:0.

First, the vertical filter is applied to the encoded input pixel data, and then the horizontal filter is applied on the resulting pixel values to generate the output pixel values. The vertical input of the filter consists of five lines of 2048 × 32 bits for both 3-tap and 5-tap configurations (see Table 10-36).

Table 10-36. DISPC Line Buffer Width for Scaler Unit

Vertical Taps	Maximum Input Width (Pixels)
3, 5	2048 × 32 bits

At the beginning of frame scaling processing, the first line is duplicated to fill the first two lines in 3-tap configuration and the first three lines in 5-tap configuration.

At the end of frame scaling processing, the last line is duplicated if the scaling logic requires loading more lines and the last line has been reached.

The programmable coefficients of the polyphase filters are signed 8-bit values (except for the central coefficient, which is unsigned). The video scalers have an 8-bit input and a 10-bit output. The vertical scaling changes the 8-bit input into a 10-bit clipped output and the horizontal scaling takes the 10-bit input.

Figure 10-53 and Figure 10-54 show the scaler macro-architecture for the component A, R, G, B, and Y. Figure 10-55 and Figure 10-56 show the scaler macro-architecture for component Cr and Cb.

The scaling output can be clipped to an output range of [1023:0] or [960:64] by configuring the DISPC_VIDp_ATTRIBUTES[11] FULLRANGE bit.

NOTE: The scaling and CSC clipping is set by the same bit, DISPC_VIDp_ATTRIBUTES[11] FULLRANGE.

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Figure 10-53. DISPC Macro-Architecture of the Horizontal Scaling for A, R, G, B, and Y Components (5-tap Restriction)

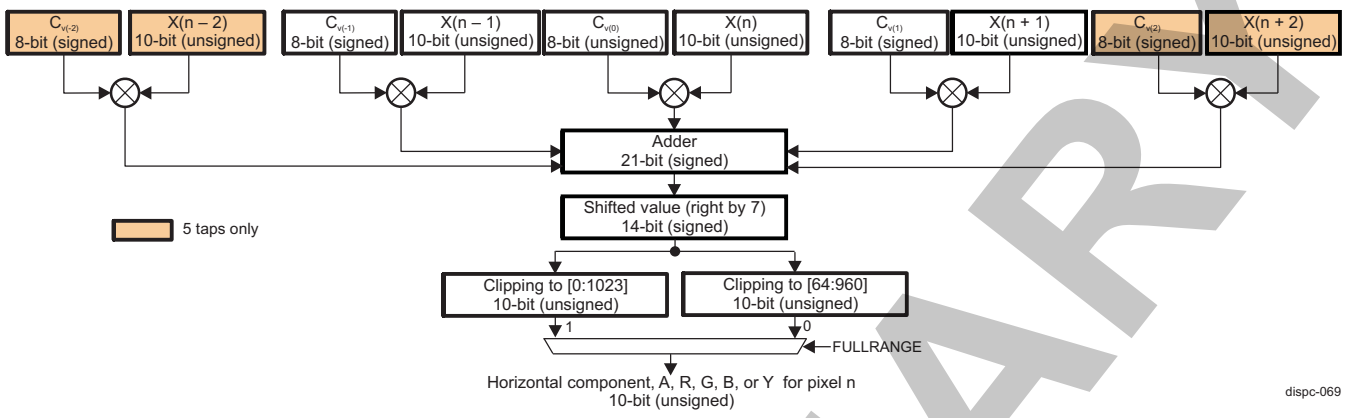

Figure 10-54. DISPC Macro-Architecture of the Vertical Scaling for A, R, G, B, and Y Components (5 and 3 taps)

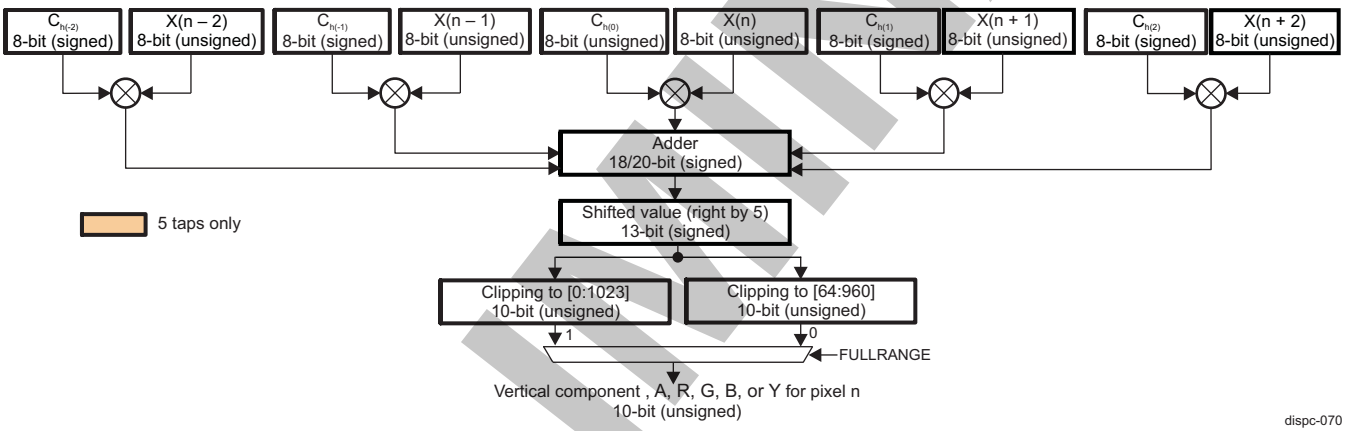

Figure 10-55. DISPC Macro-Architecture of the Horizontal Scaling for Cr and Cb Components (5-tap Restriction)

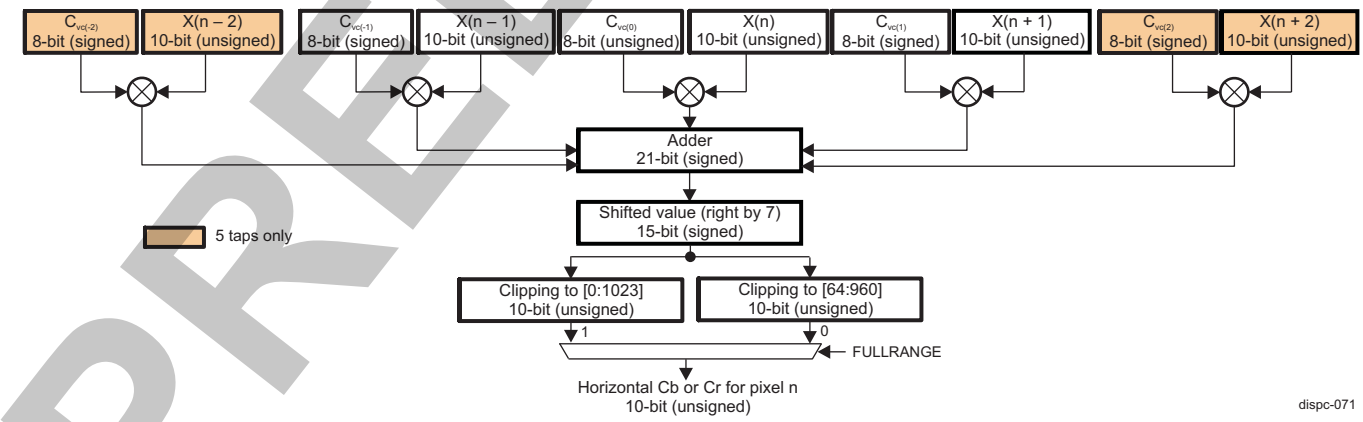

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Figure 10-56. DISPC Macro-Architecture of the Vertical Scaling for Cr and Cb Components (5 and 3 taps)

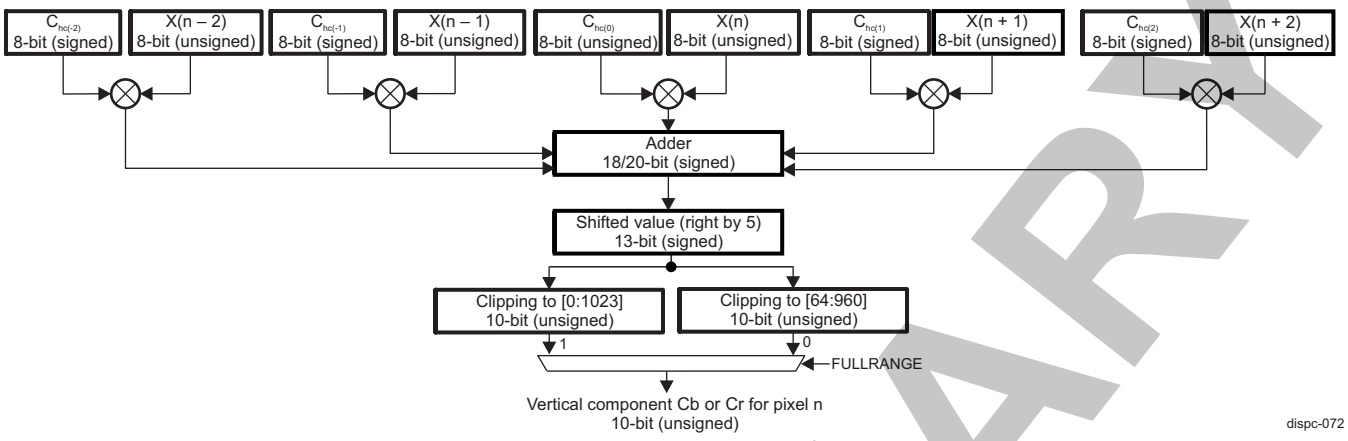

Table 10-37 and Table 10-38 list the bit fields in the function to set for each coefficient.

Table 10-37. DISPC Register Bit Field Associated to Coefficient for ARGB and Y Configuration in VIDp Scaler

Taps	Coefficient	3 Taps	5 Taps	Registers
		Bit Field	Bit Field	
Vertical	Cv(–2)		FIRVC22	DISPC_VIDp_FIR_COEF_V_i
	Cv(–1)	FIRVC2	FIRVC2	DISPC_VIDp_FIR_COEF_HV_i
	Cv(0)	FIRVC1	FIRVC1	DISPC_VIDp_FIR_COEF_HV_i
	Cv(1)	FIRVC0	FIRVC0	DISPC_VIDp_FIR_COEF_HV_i
	Cv(2)		FIRVC00	DISPC_VIDp_FIR_COEF_V_i
Horizontal	Ch(–2)	N/A	FIRHC4	DISPC_VIDp_FIR_COEF_HV_i
	Ch(–1)		FIRHC3	DISPC_VIDp_FIR_COEF_H_i
	Ch(0)		FIRHC2	DISPC_VIDp_FIR_COEF_H_i
	Ch(1)		FIRHC1	DISPC_VIDp_FIR_COEF_H_i
	Ch(2)		FIRHC0	DISPC_VIDp_FIR_COEF_H_i

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Table 10-38. DISPC Register Bit Field Associated to Coefficient for Cb and Cr Configuration in VIDp Scaler

Taps	Coefficient	3 Taps	5 Taps	Registers
		Bit Field	Bit Field	
Vertical	Cvc(–2)		FIRVC22	DISPC_VIDp_FIR_COEF_V2_i
	Cvc(–1)	FIRVC2	FIRVC2	DISPC_VIDp_FIR_COEF_HV2_i
	Cvc(0)	FIRVC1	FIRVC1	DISPC_VIDp_FIR_COEF_HV2_i
	Cvc(1)	FIRVC0	FIRVC0	DISPC_VIDp_FIR_COEF_HV2_i
	Cvc(2)		FIRVC00	DISPC_VIDp_FIR_COEF_V2_i
Horizontal	Chc(–2)		FIRHC4	DISPC_VIDp_FIR_COEF_HV2_i
	Chc(–1)		FIRHC3	DISPC_VIDp_FIR_COEF_H2_i
	Chc(0)	N/A	FIRHC2	DISPC_VIDp_FIR_COEF_H2_i
	Chc(1)		FIRHC1	DISPC_VIDp_FIR_COEF_H2_i
	Chc(2)		FIRHC0	DISPC_VIDp_FIR_COEF_H2_i

The VID scaler unit vertical or/and horizontal sampling is defined by setting/resetting the DISPC_VIDp_ATTRIBUTES[6:5] RESIZEENABLE bit field.

A set of configurations must be valid before enabling the video upsampling and downsampling block.

The following fields define the configuration of the video upsampling downsampling block for VIDp:

- Vertical upsampling and downsampling increments the value of the DISPC_VIDp_FIR[28:16] FIRVINC bit field. The unsigned integer value range is [4096:1]. Software calculates the value using the following equation:

$$FIRVINC = 1024 \times \left(\frac{MEMSIZEY}{SIZEY} \right)$$

dispc-066 (10)

NOTE:

- If the value of the DISPC_VIDp_FIR[28:16] FIRVINC bit field is greater than 4096, it is clipped to 4096.
- If the ISPC_VIDp_SIZE[27:16] SIZEY bit field equals 0x1, SIZEY is replaced by 0x2 in the previous equation.
- The values of the DISPC_VIDp_PICTURE_SIZE[27:16] MEMSIZEY and DISPC_VIDp_SIZE[27:16] SIZEY bit fields must be programmed with the value desired minus 1.

- Horizontal upsampling and downsampling increments the value of the DISPC_VIDp_FIR[12:0] FIRHINC bit field. The unsigned integer value range is [4096:1]. Software calculates the value using the following equation:

$$FIRHINC = 1024 \times \left(\frac{MEMSIZEX}{SIZEX} \right)$$

dispc-067 (11)

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NOTE:

- If the value of the DISPC_VIDp_FIR[12:0] FIRHINC bit field is greater than 4096, it is clipped to 4096.
- If the DISPC_VIDp_SIZE[11:0] SIZEX bit field equals 1, SIZEX is replaced by 2 in the previous equation.
- The values of the DISPC_VIDp_PICTURE_SIZE[10:0] MEMSIZEX and DISPC_VIDp_SIZE[11:0] SIZEX bit fields must be programmed with the value desired minus 1.

- Vertical up/downsampling accumulator value DISPC_VIDp_ACCU_j[26:16] VERTICALACCU bit field: The signed integer value range is [–1024:1023]. The accumulator value indicates on which phase the vertical filtering starts. The register DISPC_VIDp_ACCU_0 is used for progressive output and for interlace output; the DISPC_VIDp_ACCU_0 and DISPC_VIDp_ACCU_1 registers are used. Similarly, DISPC_VIDp_ACCU2_0 and DISPC_VIDp_ACCU2_1 are used in progressive or interlace output to set the accumulator value of the Cb and Cr components when scaling YUV format.
- Vertical upsampling and downsampling line buffer configuration DISPC_VIDp_ATTRIBUTES[21] VERTICALTAPS bit: The default value at reset time is 0x0 (3-tap configuration is used). If the bit field is reset, the 3-tap configuration is used.
- Horizontal upsampling and downsampling accumulator value DISPC_VIDp_ACCU_j[10:0] HORIZONTALACCU bit field: The signed integer value range is [–1024:1023]. The accumulator value indicates on which phase the horizontal filtering starts. The register DISPC_VIDp_ACCU_0 is used for progressive output and for interlace output; the DISPC_VIDp_ACCU_0 and DISPC_VIDp_ACCU_1 registers are used. Similarly, DISPC_VIDp_ACCU2_0 and DISPC_VIDp_ACCU2_1 are used in progressive or interlace output to set the accumulator value of the Cb and Cr components when scaling YUV format.

Table 10-39 lists the DISPC vertical and horizonatal accumulator values and phases.

Table 10-39. DISPC Vertical and Horizontal Accumulator Phase

Accumulator Value	Phases f
0	0
128 or –896	1
256 or –768	2
384 or –640	3
512 or –512	4
640 or –384	5
768 or –256	6
896 or –128	7

- Vertical upsampling and downsampling coefficients:
  - The 3-tap vertical upsampling and downsampling coefficients are defined in the DISPC_VIDp_FIR_COEF_HV_i registers. There are 8 registers for the 8 phases with 3 coefficients for each, or a total of 24 programmable coefficients for the vertical upsampling and downsampling block. Each register contains two 8-bit signed coefficients and one 8-bit unsigned coefficient (the central one).
  - The 5-tap vertical upsampling and downsampling coefficients: Two extra-tap vertical upsampling and downsampling coefficients are defined in the DISPC_VIDp_FIR_COEF_V_i registers. There are 8 registers for the 8 phases with 2 coefficients for each of them, so a total of 16 programmable coefficients for the vertical upsampling downsampling block are used in addition to the 3-tap registers previously defined.

  Four YUV vertical upsampling and downsampling coefficients are set in DISPC_VIDp_FIR_COEF_HV2_i and DISPC_VIDp_FIR_COEF_V2_i registers. Table 10-37 and Table 10-38 summarize all coefficients and their respective registers.
- Horizontal upsampling and downsampling coefficients:

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– The DISPC_VIDp_FIR_COEF_H_i and DISPC_VIDp_FIR_COEF_HV_i registers define the 5-tap horizontal up/downsampling coefficients. Each DISPC_VIDp_FIR_COEF_H_i register contains three 8-bit signed coefficients and one 8-bit unsigned coefficient (the central one). Each DISPC_VIDp_FIR_COEF_HV_i register contains one 8-bit signed coefficient. A total of 40 programmable coefficients for the horizontal upsampling and downsampling block are used.

Four YUV horizontal upsampling and downsampling coefficients are set in the DISPC_VIDp_FIR_COEF_HV2_i and DISPC_VIDp_FIR_COEF_H2_i registers. Table 10-37 and Table 10-38 summarize all coefficients and their respective registers.

Section 10.2.4.10.4.3, *DISPC Filter Coefficients*, provides reference tables with example values for filter coefficients.

10.2.4.10.4.1 DISPC Scaling Algorithms

Figure 10-57 and Figure 10-58 show details of the vertical and horizontal upsampling and downsampling finite state-machines (FSMs), respectively.

Figure 10-57. DISPC Vertical Upsampling and Downsampling Algorithm

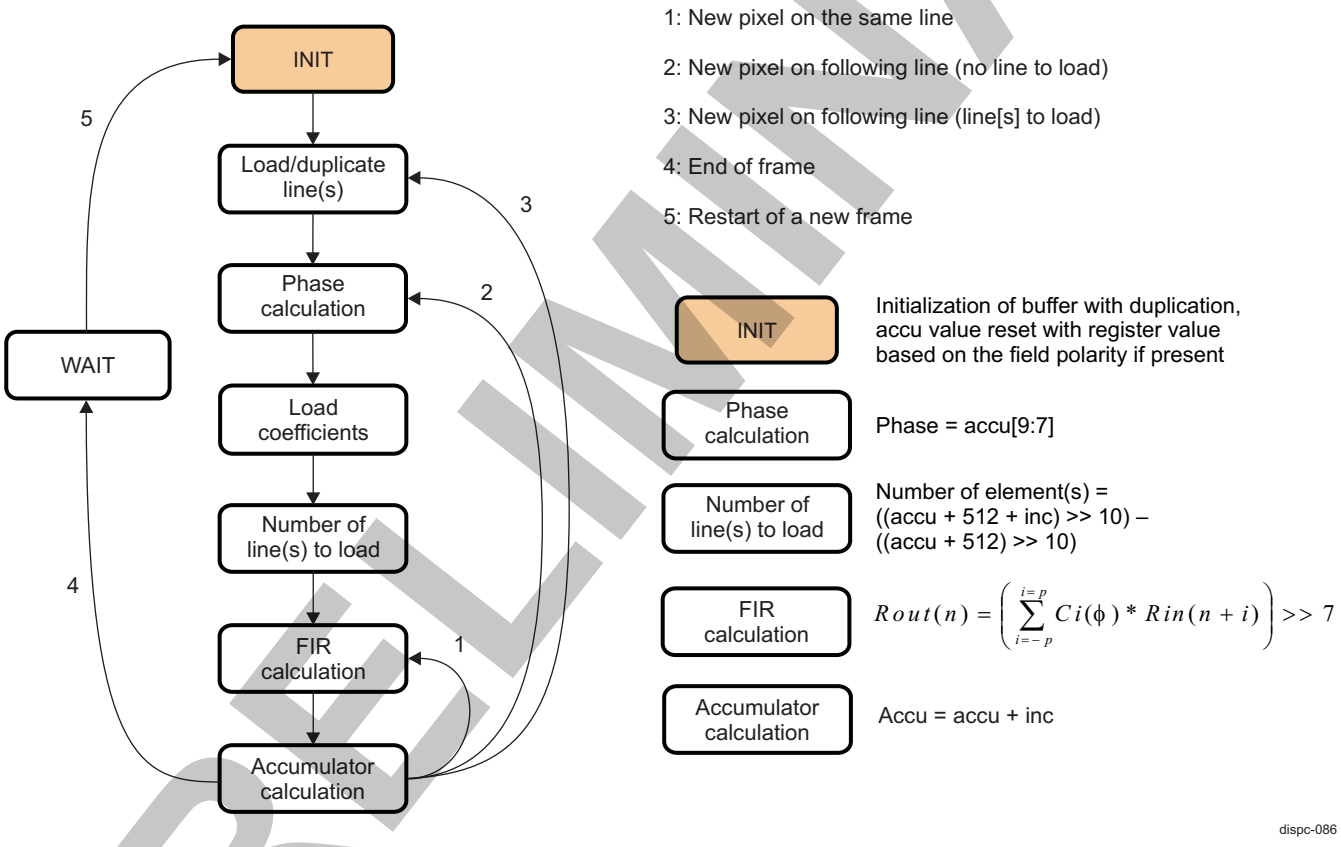

Figure 10-58 shows the horizontal up/downsampling FSM.

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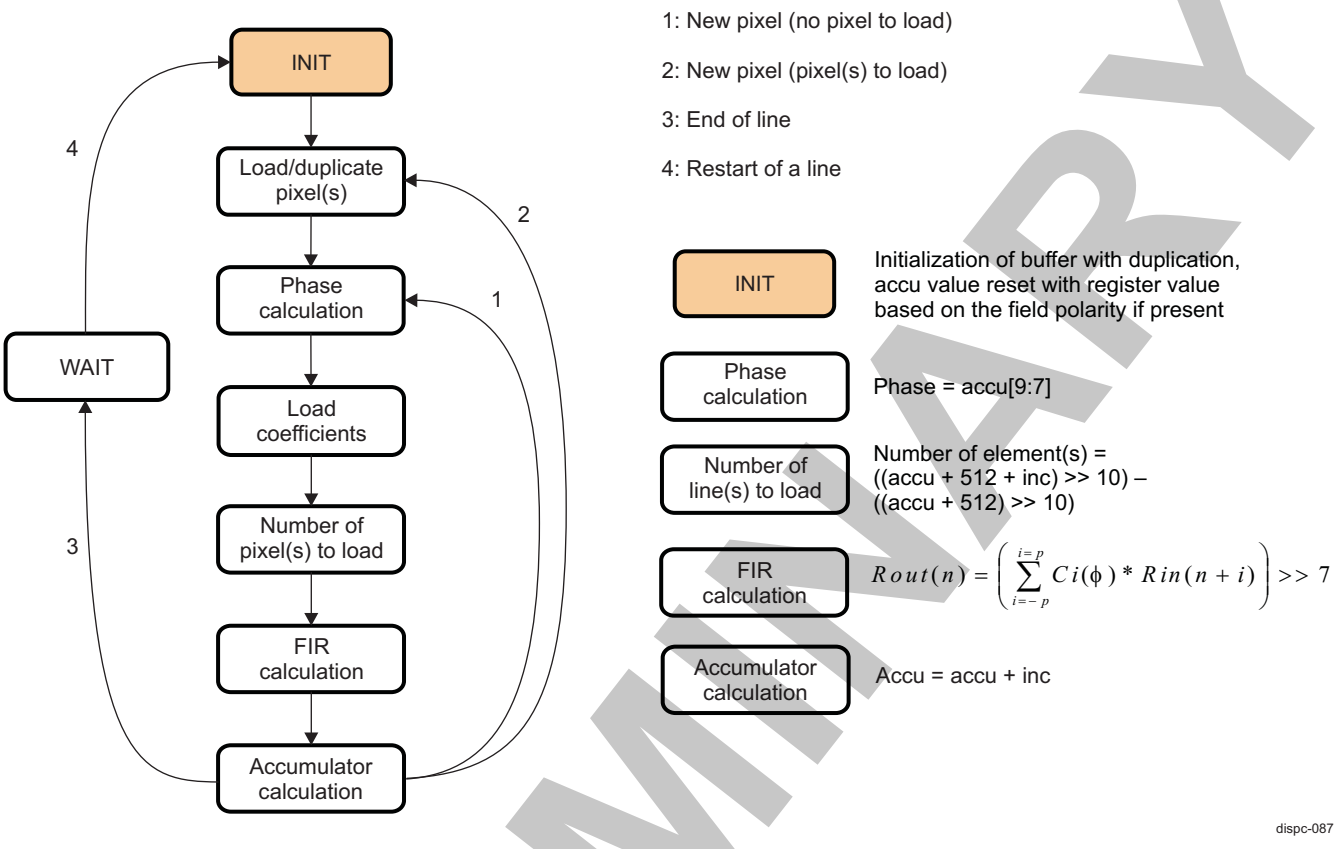
Figure 10-58. DISPC Horizontal Up/Downsampling Algorithm



10.2.4.10.4.2 DISPC Scaling limitations

Table 10-40 lists the minimum ratio between the pixel clock frequency (DSS_DISPC_LCDn_PCLK) and the functional clock (F_CLK) in the input pixel format when using the scaler unit. DSS_DISPC_LCDn_PCLK and F_CLK are asynchronous. For each LCD output, a dedicated LCD clock is programmable with the LCD and PCD divisor values in DISPC_DIVISORo[23:16][7:0].

NOTE: The F_CLK is derived from DSS_FCLK through the LCD divisor.

NOTE: The downscaling ratio is not an integer, it is the ratio F_CLK / DSS_DISPC_LCDn_PCLK, meaning if the ratio is 2.7, then the downscaling ratio is 2.7 and not 2.

Table 10-40. DISPC Pixel Clock Frequency Limitations (Any Pixel Format) – Active Matrix Display

F_CLK/DSS_DISPC_LCDn_PCLK Minimum Ratio	Horizontal Resampling				
	Off	Up	1:1–1:2	1:2–1:3	1:3–1:4
	2 or 1[(1)]	2 or 1[(1)])	2	3	4

(1) The minimum ratio can be 1 if the data are output on the rising edge of the PCLK (DISPC_POL_FREQo.IPC = 0); otherwise, the minimum ratio must be 2.

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10.2.4.10.4.3 DISPC Filter Coefficients

NOTE: This section provides reference tables with filter-coefficient example values obtained using the Lanczos window function.

All scaler coefficients and their corresponding registers are summarized in Table 10-37 and Table 10-38.

Table 10-41 gives the 40 coefficients for the 8 phases of 5-tap configuration for different values of the downsampling factor M.

Table 10-42 gives the 24 coefficients for the 8 phases of 3-tap configuration for different values of the downsampling factor M.

The selection of coefficients from Table 10-41 and Table 10-42 is based on the target scaling ratio:

- Dividing the scaling ratio by 8 gives the ideal FIR filter cut-off frequency (Fc) and matching decimation factor (M). For example, a scaling ratio of ½ gives an ideal cut-off frequency of 1/16 (in other words, the decimation factor M = 16).
- If a sharper image result is required, then the coefficients corresponding to lower M value than calculated should be selected. For example, a scaling ratio of 1/3 gives M = 24. For sharper image result, the coefficients for M = 22 should be selected. This is the preferred method when using the DISPC scaler unit.
- If a smoother image result is required, then the coefficients corresponding to higher M value than calculated should be selected. In the same example as above, a scaling ratio of 1/3 gives M = 24. For smoother image result, the coefficients for M = 26 should be selected.
- The coefficients for M = 8 could be used for any up-scaling ratio, but are preferred for up-scaling ratios up to 2.
- For up-scaling ratio > 2, in order to avoid possible blockiness and outlines around the image when using filter coefficients for M = 8, the following could be considered:
  - For calculated M = 3, the coefficient values for M = 11 should be used.
  - For calculated M = 2, the coefficient values for M = 16 should be used.
  - For calculated M = 0 to 1, the coefficient values for M = 19 should be used.

Table 10-41. Filter Coefficients (Five Taps)

Downsampling Factor M (range)	Coefficients	Phases							
		0	1	2	3	4	5	6	7
4-8	C(2)	0	1	2	1	–14	–10	–6	–2
	C(1)	0	–10	–15	–16	78	55	33	14
	C(0)	128	125	114	98	78	98	114	125
	C(–1)	0	14	33	55	–14	–16	–15	–10
	C(–2)	0	–2	–6	–10	0	1	2	1
9	C(2)	–3	–1	0	1	–12	–11	–8	–6
	C(1)	10	0	–7	–11	76	58	40	24
	C(0)	114	111	103	91	76	91	103	111
	C(–1)	10	24	40	58	–12	–11	–7	0
	C(–2)	–3	–6	–8	–11	0	1	0	–1
10	C(2)	–4	–3	–1	0	–8	–9	–8	–6
	C(1)	18	8	0	–5	72	58	44	30
	C(0)	100	99	93	84	72	84	93	99
	C(–1)	18	30	44	58	–8	–5	0	8
	C(–2)	–4	–6	–8	–9	0	0	–1	–3

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Table 10-41. Filter Coefficients (Five Taps) (continued)

Downsampling Factor M (range)	Coefficients	Phases							
		0	1	2	3	4	5	6	7
11	C(2)	–5	–3	–2	–1	–4	–6	–6	–6
	C(1)	23	13	6	0	68	57	45	34
	C(0)	92	90	85	78	68	78	85	90
	C(–1)	23	34	45	57	–4	0	6	13
	C(–2)	–5	–6	–6	–6	0	–1	–2	–3
12	C(2)	–4	–3	–2	–1	0	–3	–4	–5
	C(1)	26	18	10	5	64	55	46	36
	C(0)	84	82	78	72	64	72	78	82
	C(–1)	26	36	46	55	0	5	10	18
	C(–2)	–4	–5	–4	–3	0	–1	–2	–3
13	C(2)	–3	–3	–2	–1	3	0	–2	–3
	C(1)	28	21	14	8	61	53	45	37
	C(0)	78	76	73	68	61	68	73	76
	C(–1)	28	37	45	53	3	8	14	21
	C(–2)	–3	–3	–2	0	0	–1	–2	–3
14	C(2)	–2	–2	–2	–1	6	3	0	–1
	C(1)	30	23	16	10	58	52	45	37
	C(0)	72	71	69	64	58	64	69	71
	C(–1)	30	37	45	52	6	10	16	23
	C(–2)	–2	–1	0	3	0	–1	–2	–2
15-16	C(2)	0	–1	–1	0	10	6	3	1
	C(1)	31	25	20	14	54	49	44	38
	C(0)	66	65	62	59	54	59	62	65
	C(–1)	31	38	44	49	10	14	20	25
	C(–2)	0	1	3	6	0	0	–1	–1
17-19	C(2)	3	1	1	0	14	10	7	4
	C(1)	32	27	23	18	50	46	42	38
	C(0)	58	58	55	54	50	54	55	58
	C(–1)	32	38	42	46	14	18	23	27
	C(–2)	3	4	7	10	0	0	1	1
20-22	C(2)	4	3	1	0	16	12	9	6
	C(1)	33	28	24	20	48	45	41	37
	C(0)	54	54	53	51	48	51	53	54
	C(–1)	33	37	41	45	16	20	24	28
	C(–2)	4	6	9	12	0	0	1	3
23-26	C(2)	6	4	2	1	18	14	11	8
	C(1)	33	29	25	22	46	43	40	36
	C(0)	50	51	50	48	46	48	50	51
	C(–1)	33	36	40	43	18	22	25	29
	C(–2)	6	8	11	14	0	1	2	4

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Table 10-41. Filter Coefficients (Five Taps) (continued)

Downsampling Factor M (range)	Coefficients	Phases							
		0	1	2	3	4	5	6	7
27-32	C(2)	7	5	3	1	19	16	13	10
	C(1)	33	29	26	23	45	42	39	36
	C(0)	48	48	47	46	45	46	47	48
	C(–1)	33	36	39	42	19	23	26	29
	C(–2)	7	10	13	16	0	1	3	5

Table 10-42. Filter Coefficients (Three Taps)

Downsampling Factor M (range)	Coefficients	Phases							
		0	1	2	3	4	5	6	7
4-8	C(1)	0	9	24	43	0	–2	–4	–4
	C(0)	128	123	108	87	64	87	108	123
	C(–1)	0	–4	–4	–2	64	43	24	9
9	C(1)	6	16	30	47	0	–2	–2	0
	C(0)	116	112	100	83	64	83	100	112
	C(–1)	6	0	–2	–2	64	47	30	16
10	C(1)	10	21	34	49	0	–1	0	3
	C(0)	108	104	94	80	64	80	94	104
	C(-1)	10	3	0	-1	64	49	34	21
11	C(1)	14	24	36	50	0	0	2	6
	C(0)	100	98	90	78	64	78	90	98
	C(–1)	14	6	2	0	64	50	36	24
12	C(1)	16	26	38	51	0	1	4	9
	C(0)	96	93	86	76	64	76	86	93
	C(–1)	16	9	4	1	64	51	38	26
13	C(1)	18	28	40	52	0	1	5	10
	C(0)	92	90	83	75	64	75	83	90
	C(–1)	18	10	5	1	64	52	40	28
14	C(1)	20	30	41	52	0	2	6	12
	C(0)	88	86	81	74	64	74	81	86
	C(–1)	20	12	6	2	64	52	41	30
15-16	C(1)	22	32	42	53	0	3	8	14
	C(0)	84	82	78	72	64	72	78	82
	C(–1)	22	14	8	3	64	53	42	32
17-19	C(1)	24	33	43	54	0	4	9	16
	C(0)	80	79	76	70	64	70	76	79
	C(–1)	24	16	9	4	64	54	43	33
20-22	C(1)	25	34	44	54	0	5	10	17
	C(0)	78	77	74	69	64	69	74	77
	C(–1)	25	17	10	5	64	54	44	34
23-26	C(1)	26	35	45	54	0	5	11	19
	C(0)	76	74	72	69	64	69	72	74
	C(–1)	26	19	11	5	64	54	45	35

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Table 10-42. Filter Coefficients (Three Taps) (continued)

Downsampling Factor M (range)	Coefficients	Phases							
		0	1	2	3	4	5	6	7
27-32	C(1)	27	36	45	54	0	6	12	19
	C(0)	74	73	71	68	64	68	71	73
	C(–1)	27	19	12	6	64	54	45	36

10.2.4.11 DISPC Write-Back Pipeline

The write-back pipeline is used to store in the system memory the capture of the overlay output or the output of one of the pipelines. The WB pipeline consists of a CSC unit, a scaler unit, and an RGB truncation logic. Because the overlay works on ARGB32-8888 format and the video accelerator works on YUV format, the color space conversion from RGB to YUV is used to directly output to memory the format that can be encoded with no extra processing.

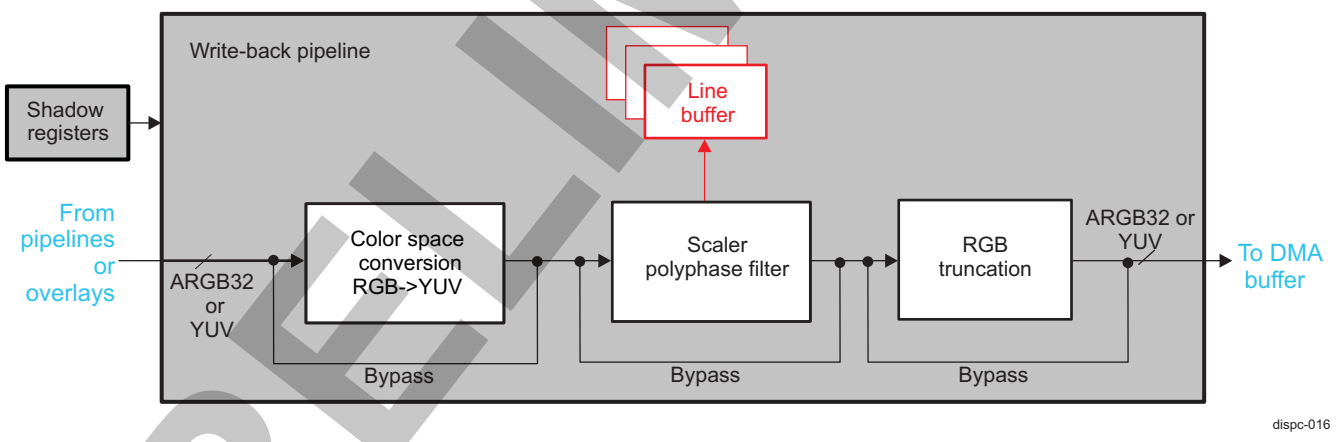
The write-back pipeline is connected to all the pipeline outputs (GFX, VD1, VID2, and VID3 pipelines) and to the output of the three overlay managers (LCD1, LCD2, LCD3, and TV). The input is selected by setting the DISPC_WB_ATTRIBUTES[18:16] CHANNELIN bit field, and the capture frame rate is set in the DISPC_WB_ATTRIBUTES[26:24] CAPTUREMODE bit field.

Because the output format of the TV overlay manager is ARGB40, the graphics pipeline output is ARGB40, the video pipeline outputs are YUV4:2:2, YUV4:2:0, or ARGB40, and the WB input is ARGB32, the WB input does not consider the 2 LSBs of each ARGB component.

The WB pipeline is enabled by setting the DISPC_WB_ATTRIBUTES[0] ENABLE bit to 0x1.

Figure 10-59 shows the graphics pipeline.

Figure 10-59. DISPC Write-Back Pipeline



10.2.4.11.1 DISPC CSC Unit RGB to YUV

The RGB-to-YUV CSC unit converts the encoded pixel values from RGB24 into YUV4:4:4 format. For YUV4:2:0 or YUV4:2:2 formats, a chrominance sub-sampling is required after converting the RGB into YUV values. Because of the subsampling, the following limitations must be considered:

- When converting RGB into YUV4:2:0 NV12 format:
  - Maximum horizontal downscale = x0.5
  - Maximum vertical downscale = x0.5
- When converting RGB into YUV4:2:2 format:
  - Maximum horizontal downscale = x0.5
  - Maximum vertical downscale = x0.25

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Figure 10-60 and Figure 10-61 show the 3 × 3 11-bit coefficients used to convert from RGB24 into YUV4:4:4. The user sets the coefficients according to the standard used to encode the pixel data in YUV color space. Table 10-43 lists the coefficients with their respective bit fields.

Table 10-43. DISPC CSC RGB to YUV Bit Field Setting

Coefficients	Bit Fields
Y_R	DISPC_WB_CONV_COEF0[10:0] YR
Y_G	DISPC_WB_CONV_COEF0[26:16] YG
Y_B	DISPC_WB_CONV_COEF1[10:0] YB
Cr_R	DISPC_WB_CONV_COEF1[26:16] CRR
Cr_G	DISPC_WB_CONV_COEF2[10:0] CRG
Cr_B	DISPC_WB_CONV_COEF2[26:16] CRB
Cb_R	DISPC_WB_CONV_COEF3[10:0] CBR
Cb_G	DISPC_WB_CONV_COEF3[26:16] CBG
Cb_B	DISPC_WB_CONV_COEF4[10:0] CBB

If the active range for the luminance samples (Y) is [16:235] and [16:240] for the chrominance samples (Cb and Cr), the values of Y, Cb, and Cr output components are clipped to the range [0:255]. The range selection is done by setting the DISPC_WB_ATTRIBUTES[11] FULLRANGE bit to 0x0.

Figure 10-60. DISPC RGB to YCbCr (FULLRANGE = 0)

$$\begin{bmatrix} Y_{OUT} \\ Cb_{OUT} \\ Cr_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} Y_R & Y_G & Y_B \\ Cb_R & Cb_G & Cb_B \\ Cr_R & Cr_G & Cr_B \end{bmatrix} * \begin{bmatrix} R_{IN} \\ G_{IN} \\ B_{IN} \end{bmatrix} + \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix}$$

dispc-017

If the active range for the luminance samples (Y) and or the chrominance samples (Cb and Cr)is [0:255], the values of Y, Cb, and Cr output components are clipped to the range [0:255]. The range selection is done by setting the DISPC_WB_ATTRIBUTES[11] FULLRANGE bit to 0x1.

Figure 10-61. DISPC RGB to YCbCr (FULLRANGE = 1)

$$\begin{bmatrix} Y_{OUT} \\ Cb_{OUT} \\ Cr_{OUT} \end{bmatrix} = \frac{1}{256} * \begin{bmatrix} Y_R & Y_G & Y_B \\ Cb_R & Cb_G & Cb_B \\ Cr_R & Cr_G & Cr_B \end{bmatrix} * \begin{bmatrix} R_{IN} \\ G_{IN} \\ B_{IN} \end{bmatrix} + \begin{bmatrix} 0 \\ 128 \\ 128 \end{bmatrix}$$

dispc-018

10.2.4.11.2 DISPC Scaler Unit

The functional aspect of the WB pipeline scaler unit is identical to the video pipeline scaler unit (see Section 10.2.4.10.4, *DISPC Scaler Unit*), except in the output width when scaling ARGB components. The resulting output format is ARGB32 instead of ARGB40.In addition, the scaling limitations described in Section 10.2.4.10.4.2 are relevant only to the video pipelines scaler units. In WB memory-to-memory mode there are no limitations on the F_CLK/DSS_DISPC_LCDn_PCLK ratio for horizontal resampling.

The programmable coefficients of the polyphase filters are signed 8-bit values (except for the central coefficient, which is unsigned). The WB scaler component has an 8-bit input and an 8-bit output.

Figure 10-62 and Figure 10-63 show the scaler macro-architecture for the component A, R, G, B, and Y. Figure 10-64 and Figure 10-65 show the scaler macro-architecture for component Cr and Cb.

The scaling output can be clipped to an output range of [0:255] or [16:240] by configuring the DISPC_WB_ATTRIBUTES[11] FULLRANGE bit.

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Figure 10-62. DISPC Macro-Architecture of the Vertical Scaling for A, R, G, B, and Y Components

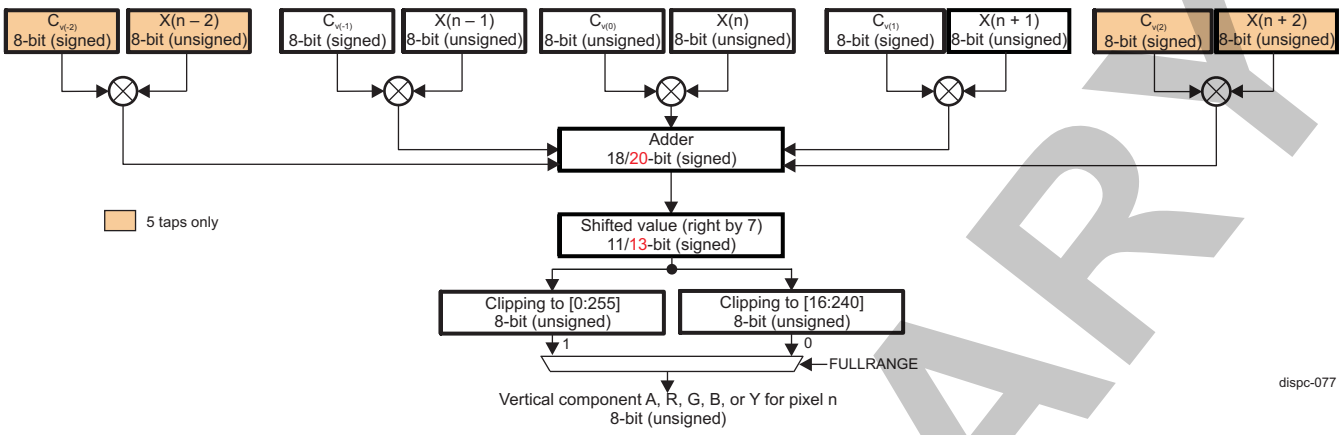

Figure 10-63. DISPC Macro-Architecture of the Horizontal Scaling for A, R, G, B, and Y Components

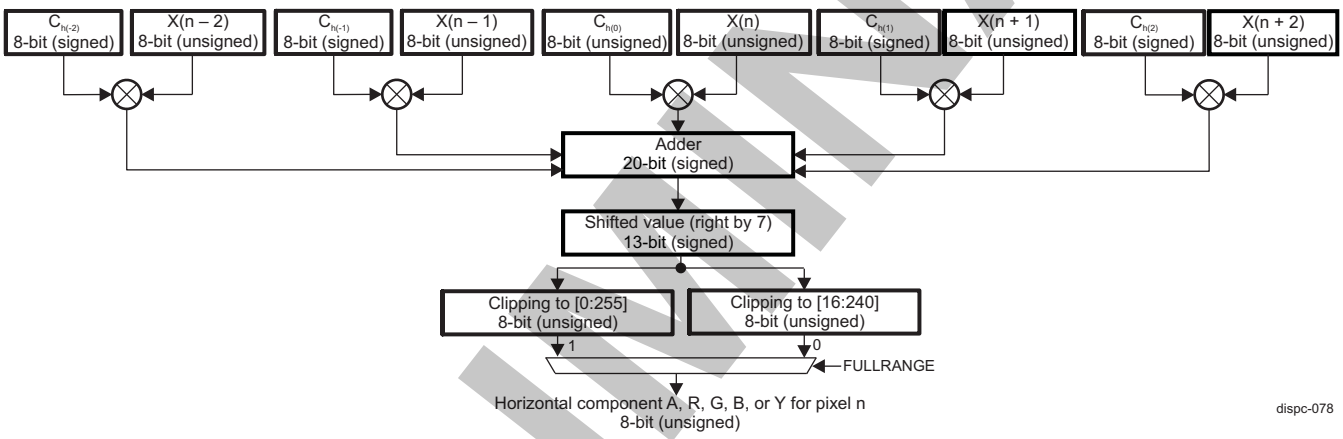

Figure 10-64. DISPC Macro-Architecture of the Vertical Scaling for Cr and Cb Components

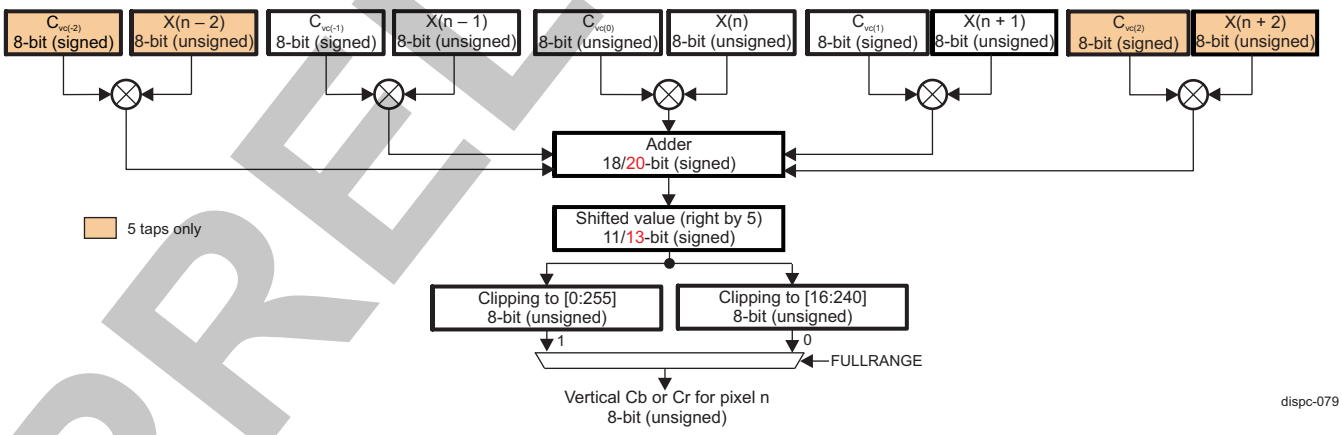

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Figure 10-65. DISPC Macro-Architecture of the Horizontal Scaling for Cr and Cb Components

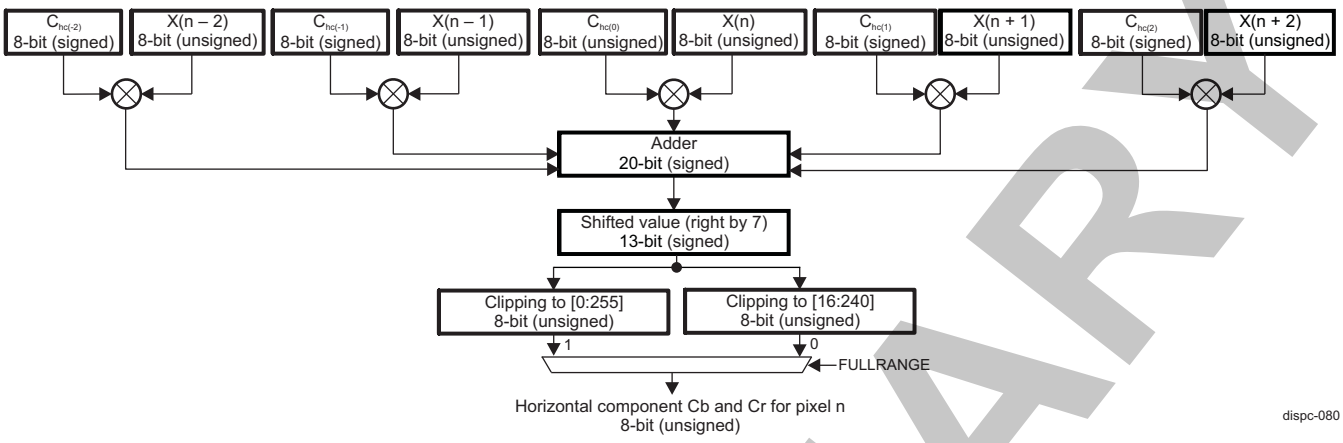

Table 10-44 and Table 10-45 list all the bit fields in the function to set each coefficient.

Table 10-44. DISPC Register Bit Field Associated With Coefficient for ARGB and Y Configuration in WB Scaler

Taps	Coefficient	3 Taps	5 Taps	Registers
		Bit Field	Bit Field	
Vertical	Cv(–2)		FIRVC22	DISPC_WB_FIR_COEF_V_i
	Cv(–1)	FIRVC2	FIRVC2	DISPC_WB_FIR_COEF_HV_i
	Cv(0)	FIRVC1	FIRVC1	DISPC_WB_FIR_COEF_HV_i
	Cv(1)	FIRVC0	FIRVC0	DISPC_WB_FIR_COEF_HV_i
	Cv(2)		FIRVC00	DISPC_WB_FIR_COEF_V_i
Horizontal	Ch(–2)	N/A	FIRHC4	DISPC_WB_FIR_COEF_HV_i
	Ch(–1)		FIRHC3	DISPC_WB_FIR_COEF_H_i
	Ch(0)		FIRHC2	DISPC_WB_FIR_COEF_H_i
	Ch(1)		FIRHC1	DISPC_WB_FIR_COEF_H_i
	Ch(2)		FIRHC0	DISPC_WB_FIR_COEF_H_i

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Table 10-45. DISPC Register Bit Field Associated With Coefficient for Cb and Cr Configuration in WB Scaler

Taps	Coefficient	3 Taps	5 Taps	Registers
		Bit Field	Bit Field	
Vertical	Cvc(–2)		FIRVC22	DISPC_WB_FIR_COEF_V2_i
	Cvc(–1)	FIRVC2	FIRVC2	DISPC_WB_FIR_COEF_HV2_i
	Cvc(0)	FIRVC1	FIRVC1	DISPC_WB_FIR_COEF_HV2_i
	Cvc(1)	FIRVC0	FIRVC0	DISPC_WB_FIR_COEF_HV2_i
	Cvc(2)		FIRVC00	DISPC_WB_FIR_COEF_V2_i
Horizontal	Chc(–2)		FIRHC4	DISPC_WB_FIR_COEF_HV2_i
	Chc(–1)		FIRHC3	DISPC_WB_FIR_COEF_H2_i
	Chc(0)	N/A	FIRHC2	DISPC_WB_FIR_COEF_H2_i
	Chc(1)		FIRHC1	DISPC_WB_FIR_COEF_H2_i
	Chc(2)		FIRHC0	DISPC_WB_FIR_COEF_H2_i

The WB scaler unit vertical or/and horizontal sampling is defined by setting/resetting the DISPC_WB_ATTRIBUTES[6:5] RESIZEENABLE bit field.

A set of configuration must be valid before enabling the video up/downsampling block.

The following fields define the configuration of the video up/downsampling block for WB:

- Vertical up/downsampling increments the value of the DISPC_WB_FIR[28:16] FIRVINC bit field. The unsigned integer value range is [1:4096]. Software calculates the value using the following equation:

$$FIRVINC = 1024 \times \left(\frac{MEMSIZEY}{SIZEY} \right)$$

dispc-066 (12)

NOTE:

- If the value of the DISPC_WB_FIR[28:16] FIRVINC bit field is greater than 4096, it is clipped to 4096.
- If the DISPC_WB_SIZE[27:16] SIZEY bit field equals 0x1, SIZEY is replaced by 0x2 in the previous equation.
- The values of the DISPC_WB_PICTURE_SIZE[27:16] MEMSIZEY and DISPC_WB_SIZE[27:16] SIZEY bit fields must be programmed with the value desired minus 1.

- Horizontal up/downsampling increments the value of the DISPC_WB_FIR[12:0] FIRHINC bit field: The unsigned integer value range is [1:4096]. Software calculates the value using the following equation:

$$FIRHINC = 1024 \times \left(\frac{MEMSIZEX}{SIZEX} \right)$$

dispc-067 (13)

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NOTE:

- If the value of the DISPC_WB_FIR[12:0] FIRHINC bit field is greater than 4096, it is clipped to 4096.
- If the DISPC_WB_SIZE[10:0] SIZEX bit field equals 1, the DISPC_WB_SIZE[10:0] SIZEX bit field is replaced by 2 in the previous equation.
- The value of the DISPC_WB_PICTURE_SIZE[10:0] MEMSIZEX and DISPC_WB_SIZE[10:0] SIZEX bit fields must be programmed with the value desired minus 1.

- Vertical up/downsampling accumulator value DISPC_WB_ACCU_j[26:16] VERTICALACCU bit field: The signed integer value range is [–1024:1023]. The accumulator value indicates on which phase the vertical filtering starts. The register DISPC_WB_ACCU_0 is used for progressive output and for interlace output the DISPC_WB_ACCU_0 and DISPC_WB_ACCU_1 registers are used. Similarly, DISPC_WB_ACCU2_0 and DISPC_WB_ACCU2_1 are used in progressive or interlace output to set the accumulator value of the Cb and Cr components when scaling YUV format.
- Vertical up/downsampling line buffer configuration DISPC_WB_ATTRIBUTES[21] VERTICALTAPS bit: The default value at reset time is 0x0 (3-tap configuration is used). If the bit field is reset, the 3-tap configuration is used.
- Horizontal up/downsampling accumulator value DISPC_WB_ACCU_j[10:0] HORIZONTALACCU bit field: The signed integer value range is [–1024:1023]. The accumulator value indicates on which phase the horizontal filtering starts. The register DISPC_WB_ACCU_0 is used for progressive output and for interlace output the DISPC_WB_ACCU_0 and DISPC_WB_ACCU_1 registers are used. Similarly, DISPC_WB_ACCU2_0 and DISPC_WB_ACCU2_1 are used in progressive or interlace output to set the accumulator value of Cb and Cr components when scaling YUV format.

Table 10-46 lists the DISPC vertical and horizontal accumulator values and phases.

Table 10-46. DISPC Vertical/Horizontal Accumulator Phase

Accumulator Value	Phases f
0	0
128 or –896	1
256 or –768	2
384 or –640	3
512 or –512	4
640 or –384	5
768 or –256	6
896 or –128	7

- Vertical up/downsampling coefficients:
  - The 3-tap vertical up/downsampling coefficients are defined in the DISPC_WB_FIR_COEF_HV_i registers. There are 8 registers for the 8 phases with 3 coefficients for each, or a total of 24 programmable coefficients for the vertical up/downsampling block. Each register contains two 8-bit signed coefficients and one 8-bit unsigned coefficient (the central one).
  - The 5-tap vertical up/downsampling coefficients: Two extra-tap vertical up/downsampling coefficients are defined in the DISPC_WB_FIR_COEF_V_i registers. There are 8 registers for the 8 phases with 2 coefficients for each of them, so a total of 16 programmable coefficients for the vertical up/downsampling block are used in addition to the 3-tap registers previously defined.

  Four YUV vertical up/downsampling coefficients are set in the DISPC_WB_FIR_COEF_HV2_i and DISPC_WB_FIR_COEF_V2_i registers. Table 10-44 and Table 10-45 summarize all coefficients and their respective registers.
- Horizontal up/downsampling coefficients:
  - The DISPC_WB_FIR_COEF_H_i and DISPC_WB_FIR_COEF_HV_i registers define the 5-tap horizontal up/downsampling coefficients. Each DISPC_WB_FIR_COEF_H_i register contains three 8-bit signed coefficients and one 8-bit unsigned coefficient (the central one). Each

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DISPC_WB_FIR_COEF_HV_i register contains one 8-bit signed coefficient. A total of 40 programmable coefficients for the horizontal up/downsampling block are used.

Four YUV horizontal up/downsampling coefficients are set in the DISPC_WB_FIR_COEF_HV2_i and DISPC_WB_FIR_COEF_H2_i registers. Table 10-44 and Table 10-45 summarize all coefficients and their respective registers.

NOTE: The values and selection criteria for programmable filter coefficients of the WB scaler unit is the same as for VID pipelines (see Section 10.2.4.10.4.3, *DISPC Filter Coefficients*).

10.2.4.11.3 DISPC RGB Truncation Logic

Truncation logic is used to convert a pixel from ARGB 32-bit format into a lower color depth: 12- or 16-bit format based. Setting the DISPC_WB_ATTRIBUTES[10] TRUNCATIONENABLE bit to 0x1 enables the truncation to the pixel format defined by the DISPC_WB_ATTRIBUTES[4:1] FORMAT bit field. The truncation is done by removing the necessary LSB of each component to match the output format. Table 10-47 describes the truncation done on each component of the pixel.

Table 10-47. DISPC Truncation Logic

	A[7:0]	R[7:0]	G[7:0]	B[7:0]
Output Formats	**MSB LSB**	**MSB LSB**	**MSB LSB**	**MSB LSB**
xRGB12-4444	Ignored	R[7:4]	G[7:4]	B[7:4]
RGBx12-4444	Ignored	R[7:4]	G[7:4]	B[7:4]
RGB16-565	Ignored	R[7:3]	G[7:2]	B[7:3]
xRGB16-1555	Ignored	R[7:3]	G[7:3]	B[7:3]
ARGB16-4444	A[7:4]	R[7:4]	G[7:4]	B[7:4]
RGBA16-4444	A[7:4]	R[7:4]	G[7:4]	B[7:4]
ARGB16-1555	A[7]	R[7:3]	G[7:3]	B[7:3]

NOTE: If there is no alpha field in the pixel format description, 0s or 1s must fill the container. 0s must be used for transparent and 1s for opaque. For example, in xRGB12 pixel format, the upper 4 bits are set to 0s because the RGB value is only 12 bits inside a 16-bit container.

10.2.4.12 DISPC LCD Outputs

The LCD1, LCD2, LCD3 output paths consist of several processing blocks (see Figure 10-66):

- Overlay manager
- Gamma correction unit
- Color phase rotation (CPR) (also used for RGB-to-YUV conversion)
- Active matrix dithering with TDM
- Synchronization buffer
- Timing generator

The display subsystem supports active matrix technologie (monochrome and color modes):

- Active matrix displays: the configuration of colors depends on the color depth:
  - 24 bpp supports 16,777,216 colors.
  - 18 bpp supports 262,144 colors.
  - 16 bpp supports 65,536 colors.
  - 12 bpp supports 4096 colors.

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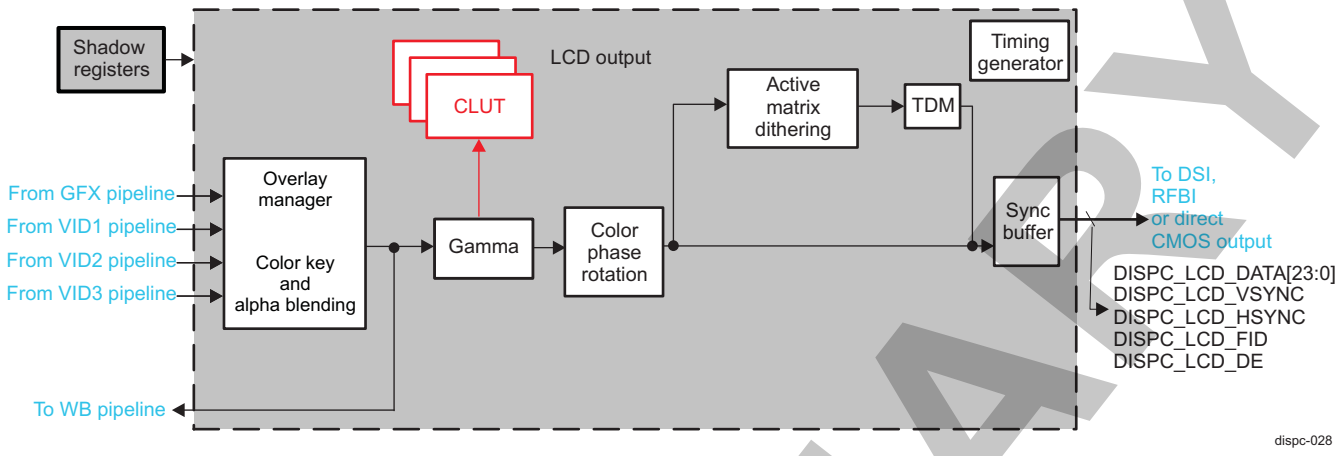
Figure 10-66. DISPC LCD Output Architecture



10.2.4.12.1 DISPC Overlay Manager

The overlay mechanism consists of displaying more than one layer (GFX, VID1 to VID3 layers) using:

- A priority rule based on a Z-order: Application can set the ordering layer of the frames.
- Transparency color keys: Destination and source transparency color keys can be set.
- Alpha blending values: Using the A component of a pixel or a blending set by the user for a layer, a level of transparency can be determined.

Each pipeline (GFX, VID1, VID2, and VID3) is assigned to a single overlay and, as a consequence, to a single display controller output, LCD1, LCD2, LCD3, TV, or WB pipeline. An overlay manager can be connected to all four pipelines outputs simultaneously. The pipeline output is directed using the DISPC_GFX_ATTRIBUTES[8] CHANNELOUT bit and the DISPC_VIDp_ATTRIBUTES[31:30] CHANNELOUT2 bit field. Table 10-48 summarizes the bit field settings to direct a pipeline to an LCD/TV or WB output. The default value directs all pipelines to LCD1.

Table 10-48. DISPC Pipeline Connection to LCD, TV, or WB Output

	DISPC_GFX_ATTRIBUTES/DISPC_VIDp_ATTRIBUTES	
Overlay Manager/Output	**CHANNELOUT Bit**	**CHANNELOUT2 Bit Field**
LCD1	0x0	0x0
LCD2	0x0	0x1
LCD3	0x0	0x2
WB	0x0	0x3
TV	0x1	0x0 (See the following note.)

NOTE: When CHANNELOUT = 0x1, the settings CHANNELOUT2 = 0x0, 0x1, 0x2, and 0x3 are reserved.

The output of each LCD overlay manager is connected to CPR block through the palette unit in the case of gamma correction.

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NOTE:

- When the pixel format is ARGB or RGBA, the color key match logic uses only the RGB value defined by ARGB or RGBA. The alpha blending factor is ignored.
- For LCD1 output, the same CLUT is used for BITMAP support by the graphics pipeline and for gamma correction. In case of BITMAP format for graphics, gamma correction is not available on the primary LCD output.

10.2.4.12.1.1 DISPC Priority Rule

The overlay manager is configured using the Z-order parameter. The Z-order value defined for each pipeline indicates the visibility order to the window on the screen. If the Z-order value of window A is lower than the Z-order to layer B, layer A is displayed below layer B. The transparency color keys and the alpha blending factors are then used to blend the layers together (see Section 10.2.4.12.1.2, *DISPC ALPHA Blender*, and Section 10.2.4.12.1.3, *DISPC Transparency Color Keys*). The Z-order is enabled by setting the DISPC_GFX_ATTRIBUTES[25] ZORDERENABLE bit or the DISPC_VIDp_ATTRIBUTES[25] ZORDERENABLE bit to 0x1 and by defining the Z-order in the DISPC_GFX_ATTRIBUTES[27:26] and DISPC_VIDp_ATTRIBUTES[27:26] ZORDER bit fields. Table 10-49 summarizes the register settings to enable and set the Z-order of a pipeline. Table 10-49 shows the default Z-order values when LCDALPHABLENDERENABLE and ZORDERENABLE are disabled.

Table 10-49. DISPC Z-Order Register Settings and Default Configuration

Pipeline	LCDALPHA BLENDERENABLE[1]	ZORDERENABLE	ZORDER	Resulting Z-Order Number
GFX	0	0	Don't care	0
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	3
VID1	0	0	Don't care	1
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	0
VID2	0	0	Don't care	2
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	1
VID3	0	0	Don't care	3
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	2

(1) Applies only to LCD1

Figure 10-67 shows the architecture of the priority rule.

NOTE:

- If ZORDERENABLE = 1, each Z-order must be different for each active pipeline. It is not possible to use the same value for more than one pipeline.
- Two modes are maintained for backward compatibility with legacy devices:
  - LCDALPHABLENDERENABLE = 0 and ZORDERENABLE = 0 equivalent to the normal mode overlay settings
  - LCDALPHABLENDERENABLE = 1 equivalent to the alpha mode overlay settings
- When OMAP3430 backward compatibility mode is to be used, the following must be considered:
  - If Z-order is disabled for the VID1 and VID2 pipelines, the pipeline data is output on the LCD1/LCD2/TV overlay.
  - If Z-order is disabled for the VID3 pipeline, the pipeline data is output only on the LCD2 overlay.

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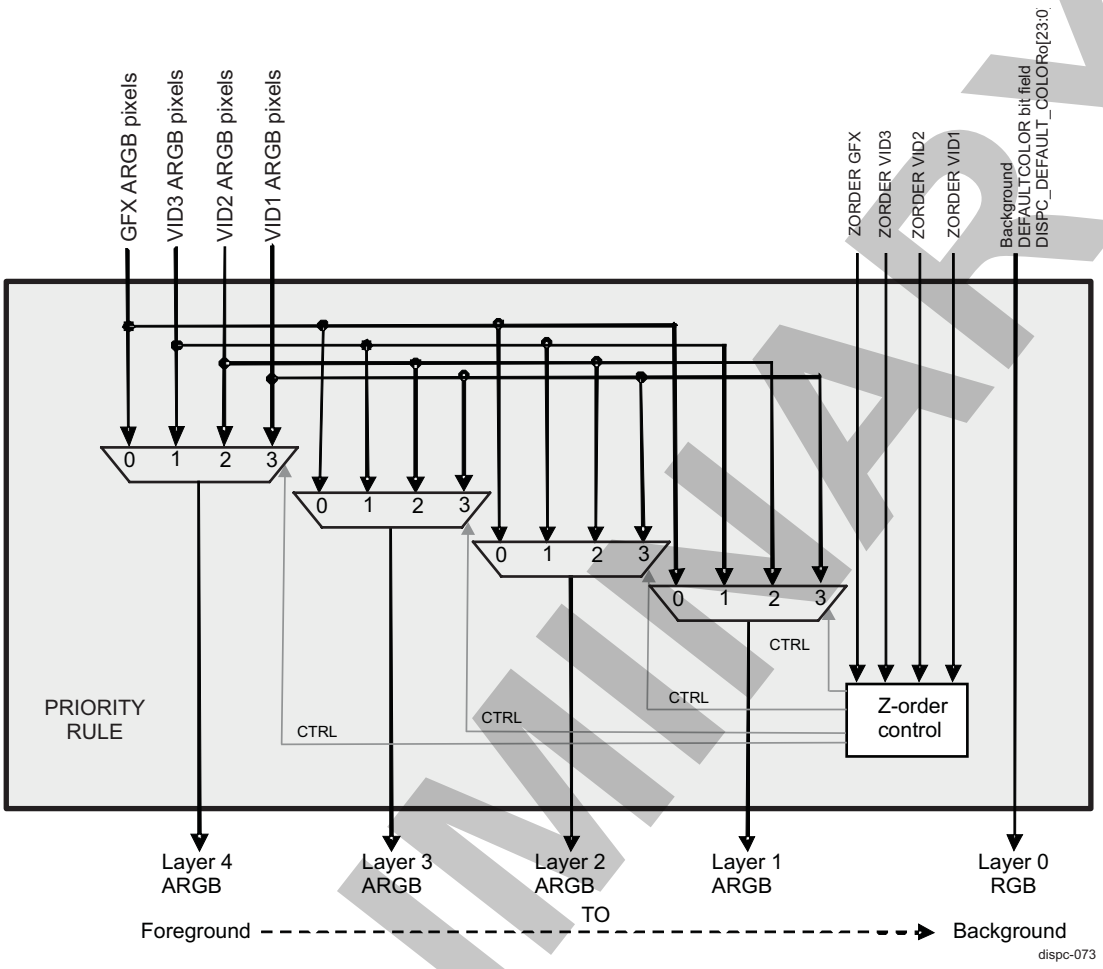
Figure 10-67. DISPC Priority Rule Architecture



The height and width of each enabled layer (pipeline) must be defined in the SIZEX and SIZEY bit fields DISPC_GFX_SIZE[27:16][11:0]/ DISPC_VIDp_SIZE[27:16][11:0], and its x and y positions defined in the POSX and POSY bit fields DISPC_GFX_POSITION[26:16][10:0]/DISPC_VIDp_POSITION[26:16][10:0]. If there are no graphics or video-encoded pixels at a specific position, the programmable, solid background color appears. The solid background color is set in the DISPC_DEFAULT_COLORo[23:0] DEFAULTCOLOR bit field. Figure 10-68 is an example of priority rule.

The Z-order reordering block must always map the pipelines to the blender logic in the same order—from background to foreground.

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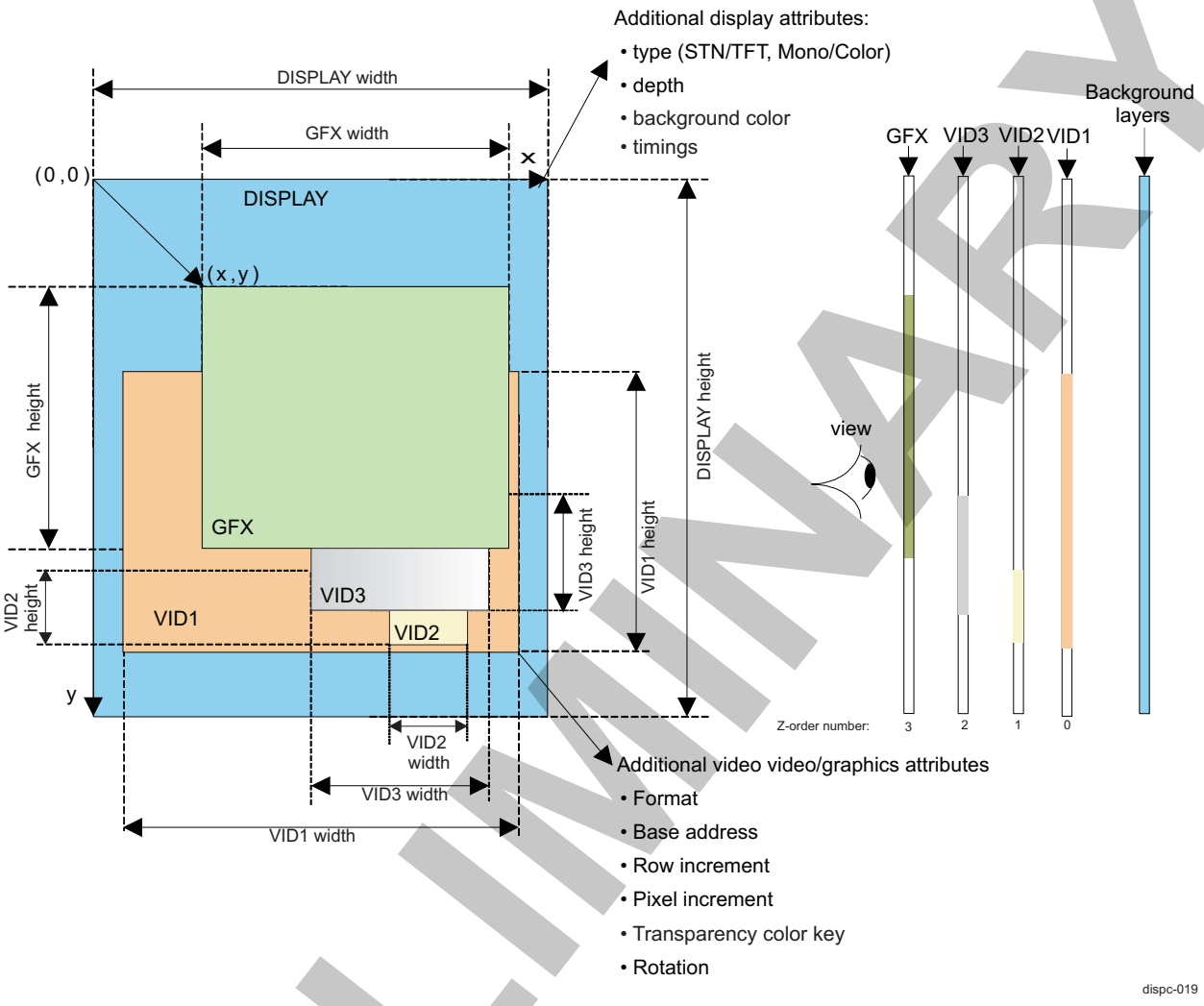
Figure 10-68. DISPC Example of Priority Rule: From Lower to Higher VID1, VID2, VID3, GFX



The DISPC is capable of outputting simultaniously two graphic/video windows in frame packing mode. Framepacking mode is enabled from DISPC_GFX_ATTRIBUTES[10] FRAMEPACKINGMODE / DISPC_VIDp_ATTRIBUTES[8] FRAMEPACKINGMODE. The position of the second graphic/video windows is defined in DISPC_GFX_POSITION2 / DISPC_VIDp_POSITION2 registers. The size is again defined in SIZEX and SIZEY bit fields of DISPC_GFX_SIZE[27:16][11:0]/ DISPC_VIDp_SIZE[27:16][11:0] registers.

10.2.4.12.1.2 DISPC Alpha Blender

Figure 10-69 shows the alpha blending processing in detail.

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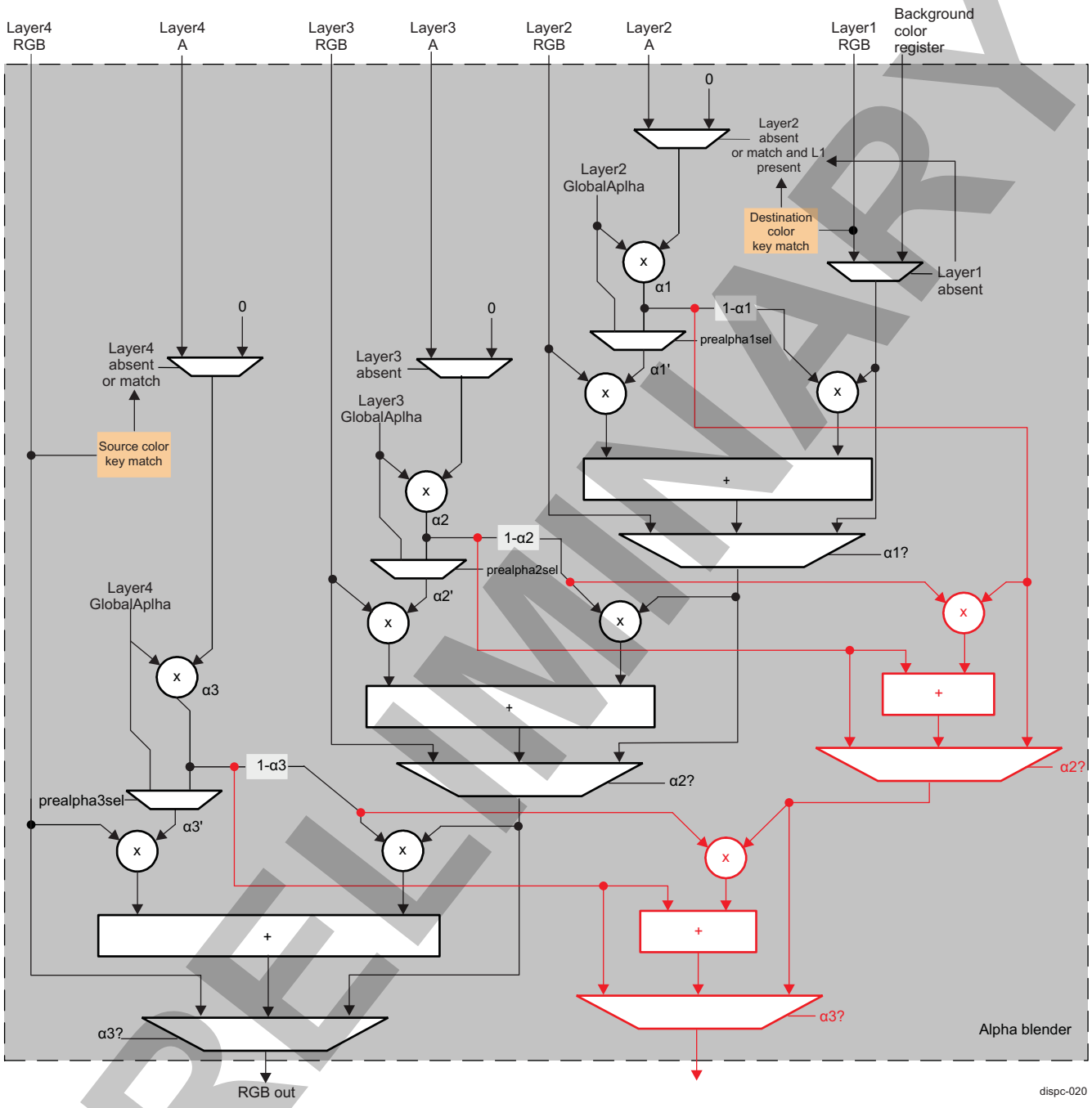
Figure 10-69. DISPC Alpha Blending Architecture With Premultiplied Alpha Support



CAUTION

The Z order of the Source Transparency Layer must have the value 3 (0x3: Z-order 3: layer above all the other layers).

NOTE: 1-alpha operator corresponds to the basic 1s-complement operation.

The alpha blending value is defined by:

- The component value A when using an ARGB or RGBA pixel format.

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  - For ARGB-1555, the alpha blending is defined using a 1-bit value. It is converted into an 8-bit value by duplicating the 1-bit value (see Table 10-50).
  - For ARGB-4444, the alpha blending is defined using a 4-bit value. It is converted into an 8-bit value by duplicating the 4-bit value (see Table 10-50).
  - If the pixel format contains no alpha blending value, the pixel alpha value is considered to be 0xFF and if alpha is equal to 0xFF, there is no multiplication.
  - For BITMAP or YUV formats, there is no alpha blending factor associated with each pixel value. Only the global alpha blending factor associated with the window displaying the BITMAP or YUV format is used.
- The global alpha blending value set in the individual bit fields of the DISPC_GLOBAL_ALPHA register for LCD:
  - VID3GLOBALALPHA
  - VID2GLOBALALPHA
  - VID1GLOBALALPHA
  - GFXGLOBALALPHA
- A total alpha blending value can be used when a combination of the pixel alpha blending value A and a global alpha blending is present. The resulting alpha value is determined as: Alpha = (Pixel Alpha × Global Alpha) / 256.

Table 10-50 lists the percentage of alpha blending in the function of the alpha blending value on 8 bits.

Table 10-50. DISPC Alpha Blending – ARGB

Alpha Blending 1-Bit Value	Alpha Blending 4-Bit Value	Alpha Blending 8-Bit Value (Converted Value or Resulting Alpha)	Percent Blending
0x0	0x0	0x00	100 (transparent)
N/A	0x1	0x11	93.33
N/A	0x2	0x22	86.6
N/A	...	...	...
N/A	0xE	0xEE	6.6
0x1	0xF	0xFF	0 (opaque)

Premultiplied Alpha

The image ARGB may have its RGB component already premultiplied with the alpha (ARGB) where:

- R = A*R
- G = A*G
- B = A*B

In that case, the processing is as follows:

- Color component of premultiplied layers are multiplied with the Global Alpha, if Global Alpha is not equal to 0.
- Color component of the composed underlying layers are multiplied with (1-A) × Global Alpha.

The additional premultiplied alpha option is associated with the pipelines GFX, VID1, VID2, and VID3. The option is accessible through the [28] PREMULTIPLYALPHA bit for the respective pipeline register:

- DISPC_GFX_ATTRIBUTES
- DISPC_VID1_ATTRIBUTES
- DISPC_VID2_ATTRIBUTES
- DISPC_VID3_ATTRIBUTES

The following settings are available:

- PREMULTIPLYALPHA bit = 0: Source is not premultiplied with alpha. Full blending is done in the DISPC.

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- PREMULTIPLYALPHA bit = 1: Source is premultiplied with alpha. Partial blending is done.

NOTE: The *prealphasel* controls in Figure 10-69, correspond to the PREMULTIPLYALPHA of the pipelines mapped on the respective layers.

The logic marked in red in Figure 10-69 corresponds to the alpha value, computed when the write-back channel copies back to memory the premultiplied color component: A (destination) = A (source) + (1-A (source) × A (destination))

When the DISPC_WB_ATTRIBUTES[7] ALPHAENABLE bit is cleared, or when the overlay channel is not selected for WB, the computation of the A(destination) is disabled. The default value for DISPC_WB_ATTRIBUTES[7] ALPHAENABLE bit is 0x0. When the WB is configured to copy back one of the output channels (output of overlay), the following configurations are available:

- The ALPHAENABLE bit is set to 0x1: The WB pipe copies back to memory the premultiplied alpha calculated through the overlay.
- The ALPHAENABLE bit is set to 0x0: The alpha value is not written back.

NOTE: The DISPC_WB_ATTRIBUTES[7] ALPHAENABLE bit is effective only when one of the output channels is written back, otherwise it is ignored.

10.2.4.12.1.3 DISPC Transparency Color Keys

The two transparency color keys are the source transparency color key and the destination transparency color key. The transparency color key can be used only with BITMAP formats (1-, 2-, 4-, and 8-bpp) and RGB formats (ARGB, RGB, RGBA, xRGB, and RGBx). in this case the A information is ignored for the comparison between the pixel value and the color key value. It is possible to use YUV formats with some care because the comparison is between the input pixel value of the overlay manager from pipeline (GFX or one of the VID pipelines depending on the Z-order) and the color key value. The YUV data is converted to RGB format. If the original format is YUV, the user must consider the color space conversion processing to define the RGB color key value used for the comparison.

The transparency color key is enabled by setting the following bits to 0x1:

- DISPC_CONFIG1[10] TCKLCDENABLE (for LCD1)
- DISPC_CONFIG2[10] TCKLCDENABLE (for LCD2)
- DISPC_CONFIG3[10] TCKLCDENABLE (for LCD3)
- DISPC_CONFIG1[12] TCKTVENABLE (for TV)

The transparency color key is determined in the following bit fields.

- DISPC_TRANS_COLOR0[23:0] TRANSCOLORKEY (for LCD1)
- DISPC_TRANS_COLOR2[23:0] TRANSCOLORKEY (for LCD2)
- DISPC_TRANS_COLOR3[23:0] TRANSCOLORKEY (for LCD3)
- DISPC_TRANS_COLOR1[23:0] TRANSCOLORKEY (for TV)

NOTE:

- The video source transparency color key and graphics destination transparency color key cannot be active at the same time.
- For CLUT bitmaps, the palette index is compared to the transparency color key and not to the palette value pointed out by the palette index.

- Video source transparency color key

  The value of the video source transparency color key defines the encoded pixel data considered as a transparent pixel. The encoded pixel values with the source color key value are not visible, and the encoded pixel values of the under layers or solid background color are visible (the pixel alpha blending value of layer 4 is forced to 0x00, fully transparent).

  The scaler can be enabled as a preprocessor in the VID pipeline, but it is necessary to consider the

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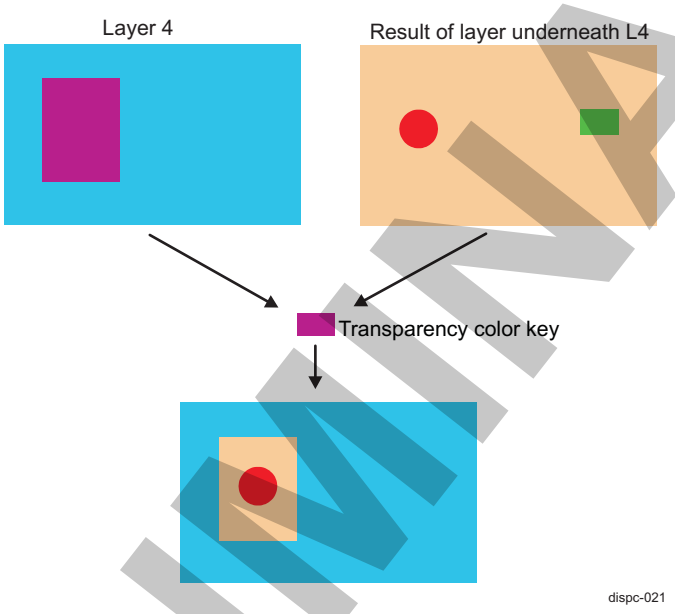
pixel scaling preprocessing in order to define the color key value to be used after the rescaling for the comparison between the input pixel value to the overlay manager and the color key value.

The source transparency color key mode is selected by setting the following bits to 0x1:

– DISPC_CONFIG1[11] TCKLCDSELECTION (for LCD1)
– DISPC_CONFIG2[11] TCKLCDSELECTION (for LCD2)
– DISPC_CONFIG3[11] TCKLCDSELECTION (for LCD3)
– DISPC_CONFIG1[13] TCKTVENABLE (for TV)

Figure 10-70 shows an example of source color key. The pixels with the transparency color key are not displayed; instead, pixels of the resulting layer underneath are shown.

Figure 10-70. DISPC Source Transparency Color Key Example



- Graphics destination transparency color key value

  The graphics destination transparency color key value defines the encoded pixels in layer 1, which are not displayed. Other layer 1 pixels (nonequal to destination transparency color key) are displayed over layer 2. The encoded pixel values with the destination color key value are pixels not visible on the screen because pixels at the same position in layer 2 are visible; otherwise, encoded pixels are visible above layer 2 . The destination transparency color key applies only if layer 1 overlaps layer 2 (see the Z-order section for details on layer position depending on the Z-order parameter in Section 10.2.4.12.1.1, *Priority Rule*); otherwise, the destination transparency color key is ignored.

  The scaler can be enabled as a preprocessor in the VID pipeline. It is necessary, however, to consider the pixel scaling preprocessing in order to define the color key value to be used after rescaling for the comparison between the input pixel value to the overlay manager and the color key value.

  The destination transparency color key mode is selected by setting the following bits to 0x0:

  – DISPC_CONFIG1[11] TCKLCDSELECTION (for LCD1)
  – DISPC_CONFIG2[11] TCKLCDSELECTION (for LCD2)
  – DISPC_CONFIG3[11] TCKLCDSELECTION (for LCD3)
  – DISPC_CONFIG1[13] TCKTVSELECTION (for TV)

  Figure 10-71 shows an example of the destination color key. The pixels, equal to the transparency color key, are not displayed and are replaced by layer 2 pixels. All other layer 1 pixels, different from the transparency color key, are displayed over layer 2.

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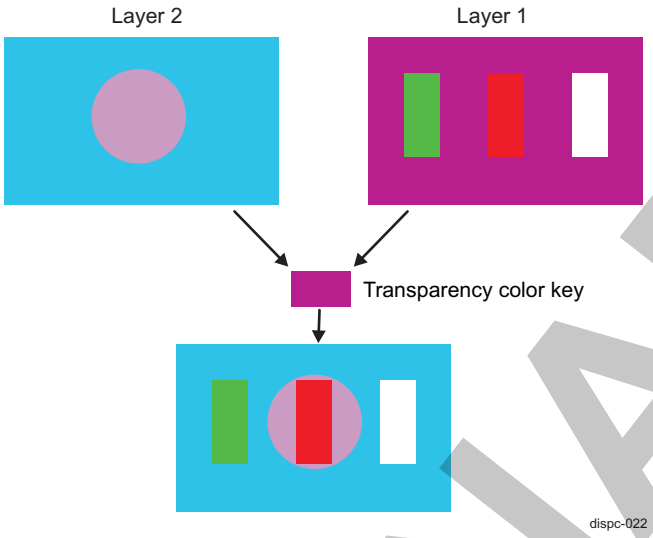
Figure 10-71. DISPC Destination Transparency Color Key Example



10.2.4.12.1.4 DISPC Overlay Optimization

The overlay optimization consists in fetching only the required pixels (that is, pixels that contribute to the final picture to be displayed [LCD1, LCD2, LCD3, or TV]). The decision to fetch the pixel from memory is based on the information available in the registers and on the following rules:

- The layer is enabled.
- The global alpha blending factor for the layer is different than 0x00.
- The current layer is behind an nonopaque layer (global alpha blending factor is different than 0xFF for the layer in the preceding).

The result of the overlay optimization is a reduction of the bandwidth by fetching only the mandatory pixels. The overlay mechanism is independent for each overlay: LCD1, LCD2, LCD3, and TV. Because each layer (GFX, VID1, VID2, and VID3) can be associated to only one overlay at a time, it is possible to optimize the fetch of the pixels for each layer based on the overlay information. The overlay optimization must be run on the DMA engine time window and not on the display time window. The pixels are fetched by the DMA engine before the display processing.

The overlay optimization is enabled by setting the following bits to 0x1:

- DISPC_CONTROL1[12] OVERLAYOPTIMIZATION (for LCD1)
- DISPC_CONTROL2[12] OVERLAYOPTIMIZATION (for LCD2)
- DISPC_CONTROL3[12] OVERLAYOPTIMIZATION (for LCD3)
- DISPC_CONTROL2[13] TVOVERLAYOPTIMIZATION (for TV)

NOTE:

- The overlay optimization is not functional when a layer is using BITMAP1, BITMAP2, BITMAP3, or BITMAP4 pixel formats.
- The pixel alpha blending factor in case of ARGB and RGBA formats cannot be used to take advantage of the pixel fully transparent (alpha blending factor equals 0x00).
- By default, the overlay optimization is disabled (OVERLAYOPTIMIZATION bits = 0x0 for all DISPC outputs), and all the data for all the enabled pipelines are fetched from memory regardless of the overlay or alpha blending configuration.

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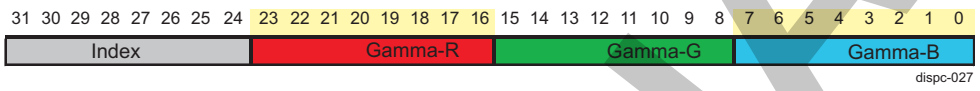
10.2.4.12.2 DISPC Gamma Correction Unit

In gamma curve mode, the selected encoded pixel values based on the color keys by the overlay manager from the video or graphics paths are sent to the gamma curve table. Each component of encoded pixel value is used as a pointer to index 1 out of 256 24-bit gamma curve entries in the table. Each 8-bit component is replaced with the 8-bit table value corresponding to R, G, or B component. The table is loaded by software. It is possible to load only part of the table. For each access to the table, the 24-bit value is associated with index in the table by concatenating the 24-bit value (LSB of 32-bit access) and the 8-bit index value (MSB of the 32-bit access). Figure 10-72 describes the format of one of the gamma curve values in the memory.

NOTE: If the CLUT is used in the GFX pipeline for palette, the gamma correction unit is not available on the primary LCD.

Figure 10-72. DISPC Data Memory Organization for Gamma Mode in LCD Output



10.2.4.12.3 DISPC Color Phase Rotation Unit

The CPR unit can be used to correct the LCD output colorimetry in case of nonpure white backlight.

The CPR is enabled by setting the DISPC_CONFIGo[15] CPR bit to 0x1. The coefficients are programmed in the following registers:

- Red 10-bit signed coefficients in DISPC_CPRo_COEF_R
- Green 10-bit signed coefficients in DISPC_CPRo_COEF_G
- Blue 10-bit signed coefficients in DISPC_CPRo_COEF_B

The CPR can be selected for active matrix panel. The logic is integrated after the LCD overlay manager or the palette while using the gamma correction and before the spatial/temporal dithering. The CPR can be selected to correct the nonpure white backlight of the LCD module by using a programmable matrix to convert the 24-bit RGB pixel value into a new 24-bit RGB pixel value. The matrix is programmed through a set of nine 10-bit signed coefficients. The output of the calculation is clipped to [0:255]. The CPR is processed by the equation shown in Figure 10-73. Table 10-51 lists all coefficients with their respective bit field registers for settings.

Figure 10-73. DISPC CPR Matrix

$$\begin{bmatrix} R_{out} \\ G_{out} \\ B_{out} \end{bmatrix} = \begin{bmatrix} Rr & Rg & Rb \\ Gr & Gg & Gb \\ Br & Bg & Bb \end{bmatrix} * \begin{bmatrix} R_{in} \\ G_{in} \\ B_{in} \end{bmatrix}$$

dispc-023

Table 10-51. DISPC CPR or RGB to YUV Coefficients With Associated Bit Fields

Registers	Bit Field	Color Space Conversion	RGB to YUV
DISPC_CPRo_COEF_R	RR	Rr	Yr
	RG	Rg	Yg
	RB	Rb	Yb
DISPC_CPRo_COEF_G	GR	Gr	Cbr
	GG	Gg	Cbg
	GB	Gb	Cbb

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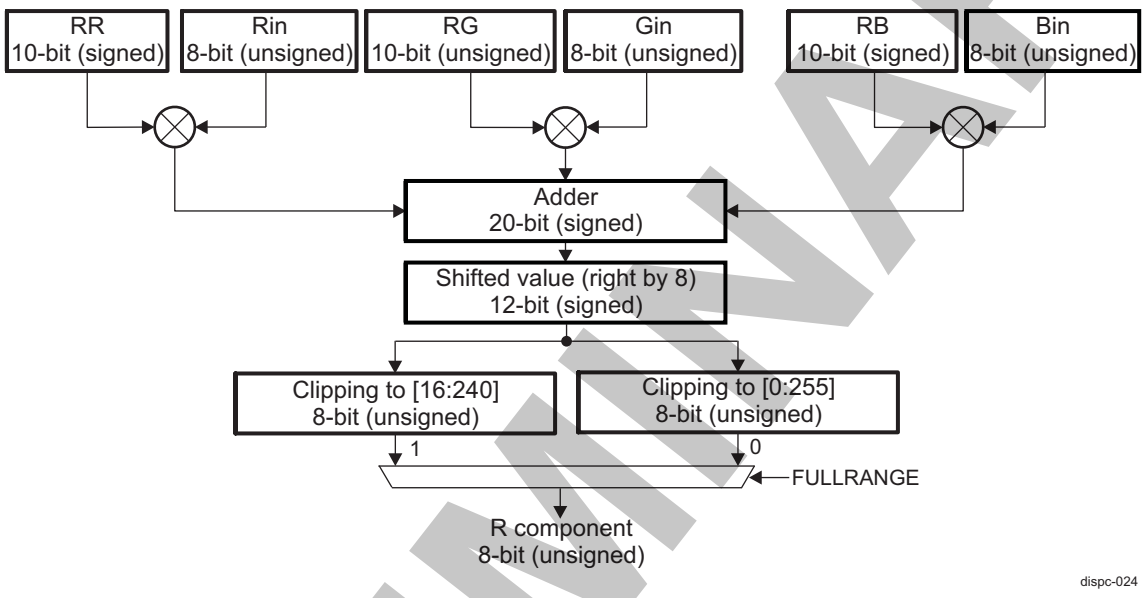
Table 10-51. DISPC CPR or RGB to YUV Coefficients With Associated Bit Fields (continued)

Registers	Bit Field	Color Space Conversion	RGB to YUV
DISPC_CPRo_COEF_B	BR	Br	Crr
	BG	Bg	Crg
	BB	Bb	Crb

Figure 10-74 shows the CPR macro-architecture.

Figure 10-74. DISPC CPR Macro-Architecture



10.2.4.12.4 DISPC Active Matrix

Depending on the color depth, the active matrix output:

- 24 bpp supports 16,777,216 colors.
- 18 bpp supports 262,144 colors.
- 16 bpp supports 65,536 colors.
- 12 bpp supports 4096 colors.

When in active matrix path configuration, after setting the DISPC_CONTROLo[3] STNTFT bit to 0x1, two submodules must be configured:

- Spatial/temporal dithering
- Multiple cycle output format (TDM)

10.2.4.12.4.1 DISPC Spatial/Temporal Dithering

When the active matrix path is used, the spatial/temporal dithering logic can be selected to enhance the quality of the active matrix outputs. The encoded pixel values are used by spatial/temporal dithering logic to display the data in a lower color depth on the LCD panel. The dithering logic is integrated after the CPR and before the TDM. The spatial/temporal dithering algorithm is based on the (x,y) pixel position and frame rate control. The dithering logic can process the pixels over one frame, two frames, or four frames. The number of frames is selected by setting the DISPC_CONTROLo[31:30] SPATIALTEMPORALDITHERINGFRAMES bit field. In the case of a single frame, only spatial processing is applied, and in multiple frames, spatial and temporal processing are applied to the pixels. The spatial/temporal dithering logic is enabled by setting the DISPC_CONTROLo[7] STDITHERENABLE bit to 0x1.

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NOTE:

- If the interface data bus is smaller than the pixel format size and spatial/temporal dithering is not enabled, the MSBs of the pixel color components are output on the interface data bus.
- If the interface data bus is larger than the pixel format size, by programming the pixel components replication active/inactive, the MSB is replicated to the LSB of the interface data bus or the LSB is filled with 0s.

10.2.4.12.4.2 DISPC Multiple Cycle Output Format (TDM)

The pixels, after the active matrix display processing, are formatted on one or multiple cycles (a maximum of three cycles). The number of bits for each cycle is set in the DISPC_DATAo_CYCLE1 register for the first cycle, the DISPC_DATAo_CYCLE2 register for the second cycle, and the DISPC_DATAo_CYCLE3 register for the third cycle. The interface data bus width can be 8, 9, 12, or 16 bits. The configuration of the data bus is done in the DIPSC_CONTROLo[9:8] TFTDATALINES bit field.

When the TDM is disabled, the DISPC outputs the pixels using the conventional formats: active matrix display monochrome/color.

Figure 10-75 through Figure 10-78 show various examples of TDM settings in the function of pixel data formats and the interface data bus width.

Figure 10-75. DISPC 8-Bit Interface Settings

	24-bpp		
	1st cycle	2nd cycle	3rd cycle
Data[7]	R0[7]	G0[7]	B0[7]
Data[6]	R0[6]	G0[6]	B0[6]
Data[5]	R0[5]	G0[5]	B0[5]
Data[4]	R0[4]	G0[4]	B0[4]
Data[3]	R0[3]	G0[3]	B0[3]
Data[2]	R0[2]	G0[2]	B0[2]
Data[1]	R0[1]	G0[1]	B0[1]
Data[0]	R0[0]	G0[0]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x2
DISPC_DATAo_CYCLE1 = 0x00000008
DISPC_DATAo_CYCLE2 = 0x00000008
DISPC_DATAo_CYCLE3 = 0x00000008

	18-bpp		
	1st cycle	2nd cycle	3rd cycle
Data[7]	R0[5]	G0[3]	x
Data[6]	R0[4]	G0[2]	x
Data[5]	R0[3]	G0[1]	x
Data[4]	R0[2]	G0[0]	x
Data[3]	R0[1]	B0[5]	x
Data[2]	R0[0]	B0[4]	x
Data[1]	G0[5]	B0[3]	B0[1]
Data[0]	G0[4]	B0[2]	B0[0]

DISPC_CONTROLo.TDMCycleFormat = 0x2
DISPC_DATAo_CYCLE1 = 0x00000008
DISPC_DATAo_CYCLE2 = 0x00000008
DISPC_DATAo_CYCLE3 = 0x00000002

	16-bpp	
	1st cycle	2nd cycle
Data[7]	R0[4]	G0[2]
Data[6]	R0[3]	G0[1]
Data[5]	R0[2]	G0[0]
Data[4]	R0[1]	B0[4]
Data[3]	R0[0]	B0[3]
Data[2]	G0[5]	B0[2]
Data[1]	G0[4]	B0[1]
Data[0]	G0[3]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000008
DISPC_DATAo_CYCLE2 = 0x00000008

	12-bpp	
	1st cycle	2nd cycle
Data[7]	R0[3]	x
Data[6]	R0[2]	x
Data[5]	R0[1]	x
Data[4]	R0[0]	x
Data[3]	G0[3]	B0[3]
Data[2]	G0[2]	B0[2]
Data[1]	G0[1]	B0[1]
Data[0]	G0[0]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000008
DISPC_DATAo_CYCLE2 = 0x00000004

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Figure 10-76. DISPC 9-Bit Interface Settings

	24-bpp		
	1st cycle	2nd cycle	3rd cycle
Data[8]	R0[7]	G0[6]	x
Data[7]	R0[6]	G0[5]	x
Data[6]	R0[5]	G0[4]	x
Data[5]	R0[4]	G0[3]	B0[5]
Data[4]	R0[3]	G0[2]	B0[4]
Data[3]	R0[2]	G0[1]	B0[3]
Data[2]	R0[1]	G0[0]	B0[2]
Data[1]	R0[0]	B0[7]	B0[1]
Data[0]	G0[7]	B0[6]	B0[0]

DISPC_CONTROLo.TDMCycleFormat = 0x2
DISPC_DATAo_CYCLE1 = 0x00000009
DISPC_DATAo_CYCLE2 = 0x00000009
DISPC_DATAo_CYCLE3 = 0x00000006

	18-bpp	
	1st cycle	2nd cycle
Data[8]	R0[5]	G0[2]
Data[7]	R0[4]	G0[1]
Data[6]	R0[3]	G0[0]
Data[5]	R0[2]	B0[5]
Data[4]	R0[1]	B0[4]
Data[3]	R0[0]	B0[3]
Data[2]	G0[5]	B0[2]
Data[1]	G0[4]	B0[1]
Data[0]	G0[3]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000009
DISPC_DATAo_CYCLE2 = 0x00000009

	16-bpp	
	1st cycle	2nd cycle
Data[8]	R0[4]	x
Data[7]	R0[3]	x
Data[6]	R0[2]	G0[1]
Data[5]	R0[1]	G0[0]
Data[4]	R0[0]	B0[4]
Data[3]	G0[5]	B0[3]
Data[2]	G0[4]	B0[2]
Data[1]	G0[3]	B0[1]
Data[0]	G0[2]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000009
DISPC_DATAo_CYCLE2 = 0x00000007

	12-bpp	
	1st cycle	2nd cycle
Data[8]	R0[3]	x
Data[7]	R0[2]	x
Data[6]	R0[1]	x
Data[5]	R0[0]	x
Data[4]	G0[3]	x
Data[3]	G0[2]	x
Data[2]	G0[1]	B0[2]
Data[1]	G0[0]	B0[1]
Data[0]	B0[3]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x00000009
DISPC_DATAo_CYCLE2 = 0x00000003

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Figure 10-77. DISPC 12-Bit Interface Settings

	24-bpp	
	1st cycle	2nd cycle
Data[11]	R0[7]	G0[3]
Data[10]	R0[6]	G0[2]
Data[9]	R0[5]	G0[1]
Data[8]	R0[4]	G0[0]
Data[7]	R0[3]	B0[7]
Data[6]	R0[2]	B0[6]
Data[5]	R0[1]	B0[5]
Data[4]	R0[0]	B0[4]
Data[3]	G0[7]	B0[3]
Data[2]	G0[6]	B0[2]
Data[1]	G0[5]	B0[1]
Data[0]	G0[4]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x0000000C
DISPC_DATAo_CYCLE2 = 0x0000000C

	18-bpp		
	1st cycle	2nd cycle	3rd cycle
Data[11]	R0[5]	B0[5]	G1[5]
Data[10]	R0[4]	B0[4]	G1[4]
Data[9]	R0[3]	B0[3]	G1[3]
Data[8]	R0[2]	B0[2]	G1[2]
Data[7]	R0[1]	B0[1]	G1[1]
Data[6]	R0[0]	B0[0]	G1[0]
Data[5]	G0[5]	R1[5]	B1[5]
Data[4]	G0[4]	R1[4]	B1[4]
Data[3]	G0[3]	R1[3]	B1[3]
Data[2]	G0[2]	R1[2]	B1[2]
Data[1]	G0[1]	R1[1]	B1[1]
Data[0]	G0[0]	R1[0]	B1[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x3
DISPC_DATAo_CYCLE1 = 0x0000000C
DISPC_DATAo_CYCLE2 = 0x00060606
DISPC_DATAo_CYCLE3 = 0x000C0000

	16-bpp	
	1st cycle	2nd cycle
Data[11]	R0[4]	x
Data[10]	R0[3]	x
Data[9]	R0[2]	x
Data[8]	R0[1]	x
Data[7]	R0[0]	x
Data[6]	G0[5]	x
Data[5]	G0[4]	x
Data[4]	G0[3]	x
Data[3]	G0[2]	B0[3]
Data[2]	G0[1]	B0[2]
Data[1]	G0[0]	B0[1]
Data[0]	B0[4]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x1
DISPC_DATAo_CYCLE1 = 0x0000000C
DISPC_DATAo_CYCLE2 = 0x00000004

	12-bpp
	1st cycle
Data[11]	R0[3]
Data[10]	R0[2]
Data[9]	R0[1]
Data[8]	R0[0]
Data[7]	G0[3]
Data[6]	G0[2]
Data[5]	G0[1]
Data[4]	G0[0]
Data[3]	B0[3]
Data[2]	B0[2]
Data[1]	B0[1]
Data[0]	B0[0]

DISPC_CONTROLo.TDMCYCLEFORMAT = 0x0
DISPC_DATAo_CYCLE1 = 0x0000000C

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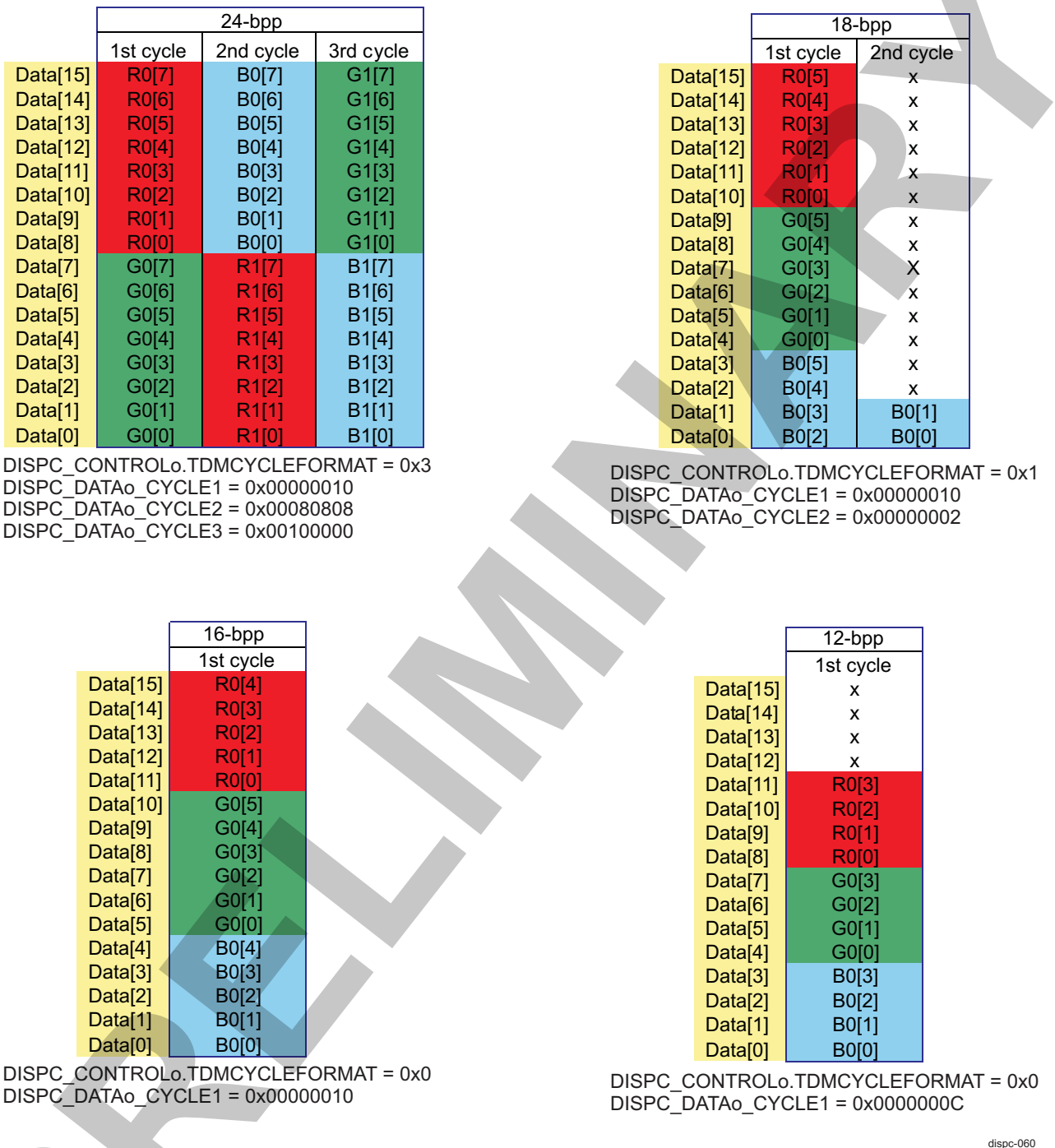
Figure 10-78. DISPC 16-Bit Interface Settings



10.2.4.12.5 DISPC Synchronized Buffer Update

A synchronization mismatch between the frame buffer and the display refreshes, named tearing effect, can lead to images that appear to be stretched on the screen. To avoid it, a synchronization mechanism is used between the DISPC and the process that updates the buffer. An interrupt is generated when the display reaches a predefined line number. The PROGRAMMEDLINENUMBER_IRQ interrupt (DISPC_IRQSTATUS and DISPC_IRQENABLE) is a level signal and stays active during the programmed line of the display.

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10.2.4.12.6 DISPC Timing Generator and Panel Settings

The size of and panel is defined by:

- Number of lines, DISPC_SIZE_LCDo[27:16] LPP bit field, with a value from 1 to 4096
- Number of pixels per line, DISPC_SIZE_LCDo[11:0]PPL bit field, with a value from 1 to 4096

Standard HSYNC/VSYNC timing generation are programmable for each LCD outputs independently:

- Horizontal front porch is set in the DISPC_TIMING_Ho[19:8] HFP bit field.
- Horizontal back porch is set in the DISPC_TIMING_Ho[31:20] HBP bit field.
- Horizontal synchronization pulse width is set in the DISPC_TIMING_Ho[7:0] HSW bit field.
- Vertical front porch is set in the DISPC_TIMING_Vo[19:8] VFP bit field.
- Vertical back porch is set in the DISPC_TIMING_Vo[31:20] VBP bit field.
- Vertical synchronization pulse width is set in the DISPC_TIMING_Vo[7:0] VSW bit field.

Horizontal/vertical synchronization and ACBIAS signals polarity are programmable by setting the DISPC_POL_FREQo[12] IVS, DISPC_POL_FREQo[13] IHS, and DISPC_POL_FREQo[15] IEO bits. These signals can be gated by setting the DISPC_CONFIGo[7] VSYNCGATED and DISPC_CONFIGo[6] HSYNCGATED bits.

The latch of data can be driven on the rising or falling edge of the pixel clock by setting the DISPC_POL_FREQo[14] IPC bit. The drive of the SYNC and VSYNC signals in the function of the pixel clock is done by setting the DISPC_POL_FREQo[16] RF bit.

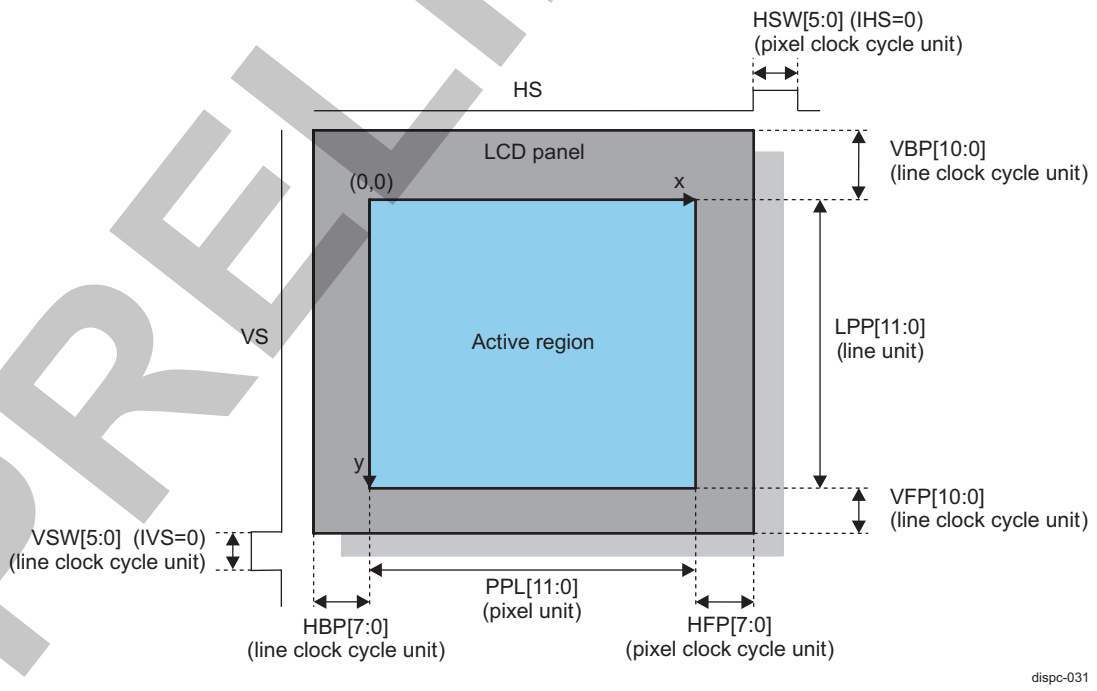
Table 10-52 describes the programming rules for LCD timing.

Table 10-52. DISPC Programming Rules

	No Downsampling	Downsampling H or V	Downsampling H + V
(HBP + HSW + HFP) × PCD	>8	>10	>20

Figure 10-79 shows the timing values description in the case of an active matrix display.

Figure 10-79. DISPC Timing Values (Active Matrix Display)



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The 8-bit pixel clock divider (the DISPC_DIVISORo[7:0] PCD bit field) selects the pixel clock frequency. This bit field generates a range of pixel clock frequencies from LC/2 to LC/256, where LC is the logic clock from the divided functional clock of the DISPC by the DISPC_DIVISOR[23:16] LCD bit field.

The pixel clock is defined by the following equation:

Pixel Clock = (FunctionalClock/LCD[7:0])/PCD[7:0]

The pixel clock can be gated by setting the DISPC_CONFIGo[5] PIXELCLOCKGATED bit to 0x1.

The LCD output can be configured in progressive output or interlace output. The selection is done by writing into the DISPC_CONFIGo[22] OUTPUTMODEENABLE bit. The reset value is 0x0, which means progressive mode. When progressive mode is selected, the FID signal associated to the LCD output is driven low (INACTIVE state). The selection can be changed only if the corresponding LCD output is disabled. The configuration is independent for each LCD output.

When in interlaced mode, the DISPC_CONFIGo[23] FIDFIRST bit indicates which field is output first:

- 0x0: Even field first (FID = 0)
- 0x1: Odd field first (FID = 1)

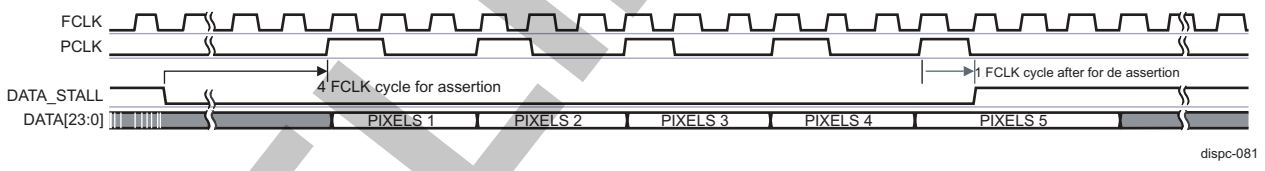
10.2.4.12.7 DISPC Stall Mode

Stall mode is used to indicate when the DISPC must stop sending data on the corresponding LCD output interface to avoid an overflow on the interface level. Stall mode is available when the RFBI and DSI interfaces are used. The Interface asserts the stall signal to stop data output by the DISPC. It is deasserted by the interface to indicate when new data must be output by the DISPC. Figure 10-80 shows the RFBI data stall mode activated.

Stall mode is selected by setting the DISPC_CONTROLo[11] STALLMODE bit.

NOTE: The DISPC_CONTROLo[5] GOLCD bit must not be set, but the DISPC configuration (DMA engine, pipelines associated with the LCD output) must be set before enabling the LCD output by setting the DISPC_CONTROLo[1] LCDENABLE bit.

Figure 10-80. DISPC RFBI Data Stall Signal Diagram



To avoid an underflow of the DMA buffer, the DMA buffer handshake must be enabled by setting the DISPC_CONFIGo[16] BUFFERHANDCHECK bit. The fullness of the buffers associated to the pipelines used for the LCD output is checked before providing data to the pipeline when the STALL signal is inactive. It prevents emptying the DMA buffer when the RFBI or DSI module requests data and there is not enough data in the DMA buffer of the DISPC. This feature must be enabled only when stall mode is used (the STALLMODE bit set to 0x1). When the DMA buffer handshake is activated, the pixel transfer to the RFBI or DSI module, outside a STALL period, can be stopped and restarted when there are enough data in the DMA buffer. The DMA buffer handshake ensures that the underflow does not occur for the pipelines associated with the LCD output when RFBI/DSI interfaces are used. The rate of the data transfer to the RFBI or DSI is, then, fully dependent on the state of the DMA buffer. Figure 10-81 shows the RFBI data stall with FIFO handcheck mode activated.

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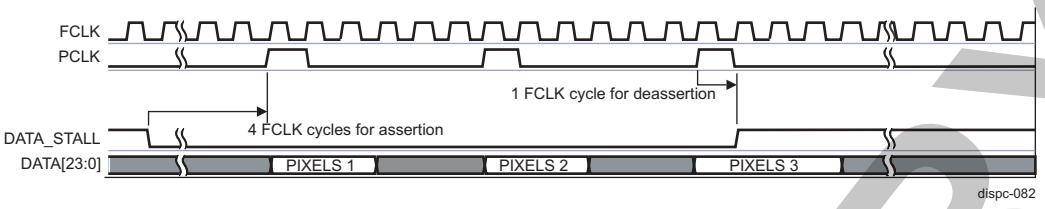
Figure 10-81. DISPC RFBI Data Stall Signal Diagram With Handcheck



Stall mode is independently used when the RFBI or DSI protocol engines are connected to the LCD outputs and receive the pixels to reformat the data.

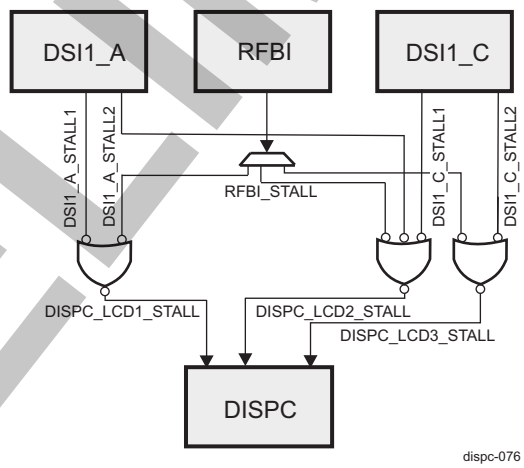
The STALL signals from the RFBI and DSI interfaces are merged into a single signal in the display subsystem. Only one signal for each LCD output is connected to the DISPC. Figure 10-82 shows the STALL signal implementation.

Two STALL signals are generated by the RFBI. The RFBI module asserts the STALL signal when no more data must be output by the DISPC. STALL is deasserted to indicate when new data must be output by the DISPC.

Two STALL signals are generated by the DSI1_A protocol engine. It is used by the DSI1_A protocol engine when data are provided from the DISPC to the DSI1_A protocol engine using the two video ports in command mode only. If one of the two video ports is in video mode, the STALL signal associated with the video port from the DSI1_A protocol engine is not used (it must be in INACTIVE state from the DSI1 protocol engine).

Two STALL signals are generated by the DSI1_C protocol engine. It is used by the DSI1_C protocol engine when data are provided from the DISPC to the DSI1_C protocol engine using the two video ports in command mode only. If one of the two video ports is in video mode, the STALL signal associated with the video port from the DSI1_C protocol engine is not used (it must be in INACTIVE state from the DSI1_C protocol engine).

Figure 10-82. DISPC STALL Signal



10.2.4.13 DISPC TV Output

The TV output paths consist of several processing blocks (see Figure 10-83):

- Overlay manager
- Gamma correction unit
- Synchronization buffer

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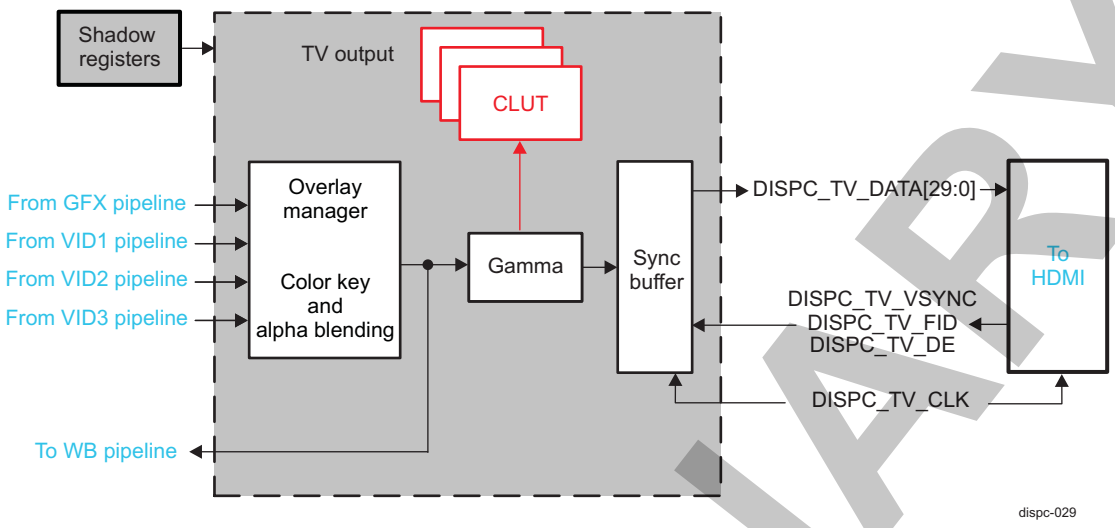
Figure 10-83. DISPC TV Output Architecture



The TV output is connected to the HDMI. In analog output or HDMI, the DISPC TV output receives an external clock, DISPC_TV_CLK, and based on the VSYNC generated by the HDMI, hold time, vertical offset, and horizontal offset, outputs the pixels synchronously. The size of the field/frame to output defines the number of pixels to output on each line and the number of lines for each field/frame.

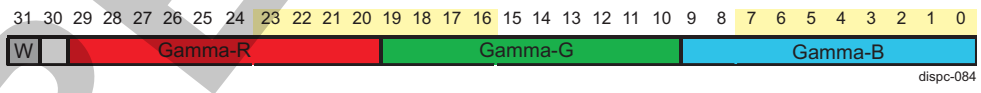
10.2.4.13.1 DISPC Overlay Manager

The overlay mechanism is identical in LCD1, LCD2, and LCD3 (see Section 10.2.4.12.1, *Overlay Manager*).

10.2.4.13.2 DISPC Gamma Correction Unit

The gamma correction unit works as described in Section 10.2.4.12.2, *Gamma Correction Unit*. The only difference is in the input pixel format RGB30. Each component of encoded pixel value is used as a pointer to index 1 out of 1024 30-bit gamma curve entries in the table. Each 10-bit component is replaced with the 10-bit table value corresponding to R, G, or B component. The table is loaded by software, through the DISPC_GAMMA_TABLE2 register. It is possible to load only part of the table. For each write access to the table, the 30-bit gamma value is associated with bit [31] INDEX to indicate that a new table is defined. Setting bit [31] INDEX to 0x1 for the first time, resets the internal index counter. All the following accesses are considered to be for incremented index addressing in the table (bit [31] INDEX is set to 0 for each subsequent access). Figure 10-84 shows the format of one of the gamma curve values in the memory.

Figure 10-84. DISPC Data Memory Organization for Gamma Mode in TV Output



10.2.4.13.3 DISPC Synchronized Buffer Update

The synchronized buffer update is identical in LCD1, LCD2, and LCD3 (see Section 10.2.4.12.5, *Synchronized Buffer Update*).

10.2.4.13.4 DISPC Timing and TV Format Settings

Figure 10-85 shows the TV formats supported.

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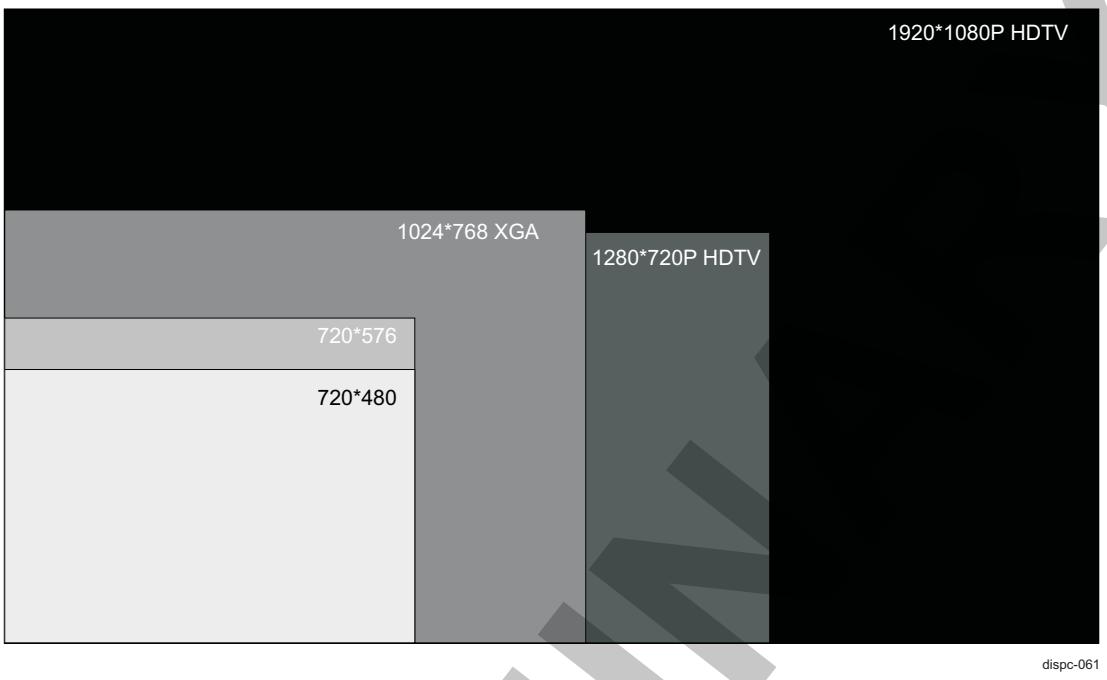
Figure 10-85. DISPC Example Timing TV Formats



The size of a TV output format is defined by:

- Number of lines, DISPC_SIZE_TV[27:16] LPP bit field, with a value from 1 to 4096
- Number of pixels per line, DISPC_SIZE_TV[11:0] PPL bit field, with a value from 1 to 4096
- Delta size between odd/even field, DISPC_SIZE_TV[15:14] DELTA_LPP bit field. This bit field controls only the output channel and not the size of the data field fetched from the frame buffer in memory.

The hold time of the pixels on the data bus is determined in clock cycles by the DISPC_CONTROL1[19:17] HT bit field. The default value at reset time is 0x0 (one cycle).

- When connected to the HDMI encoder, Table 10-53 indicates the DISPC_SIZE_TV (PPL and LPP) value for each HD standard.

Table 10-53. DISPC PPL and LLP Value for HD Standard

Standards		Active Pixels/Line	Active Lines	Digital Clock	DISPC_SIZE_TV
HDTV	720p	1280	720	74.25/74.125 MHz (60/59.99..frames/s)	0x02CF 04FF
	1080i	1920	540	74.25/74.125 MHz (60/59.99..frames/s)	0x021B 07FF
	1080p	1920	1080	148.5/148.25 MHz (60/59.99..frames/s)	0x0437 07FF
	720p 3D (frame packing)	1280	1470	148.5/148.35/148.5 MHz (60/59.94/50 frames/s)	0x05BD 04FF
	1080p 3D (frame packing)	1920	2205	148.5/148.35 MHz (24/23.98 frames/s)	0x089C 07FF
	1080p 3D (side-by-side half)	1920	1080	148.5 MHz (60 frames/s)	0x0437 07FF

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NOTE: When configuring the DISPC for outputting any supported 3D frame-packing format, the following generic details must be considered:

- As defined by the *HDMI v1.4 Specification*, Section 8.2.3.2, 3D frame-packing is a video format structure composed of two stereoscopic pictures: left and right.
- The stereoscopic pictures can be processed through the three video pipelines (VID1, VID2, or VID3). For more information about the configuration of video pipelines, see Section 10.2.4.10, *Video Pipelines*.
- The 3D frame is generated by setting the TV overlay manager to combine the outputs of the selected video pipelines that hold the pictures. One video pipeline (VID1 or VID3) must carry the top field of the 3D frame (left stereoscopic picture), and the other video (VID2) pipeline must always carry the bottom field of the frame (right stereoscopic picture). The top and bottom fields are separated by an active space area. For more information, see the *HDMI v1.4 Specification*, Section 8.2.3.2.
- The pipeline carrying each field (top and bottom) of the 3D frame must have its height and width parameters defined in the [27:16] SIZEY and [11:0] SIZEX bit fields of the DISPC_VIDp_SIZE register, and its Y and X positions defined in the [26:16] POSY and [10:0] POSX bit fields of the DISPC_VIDp_POSITION register. The active space area of the 3D frame can be encoded by setting the solid background color for the TV output (the DISPC_DEFAULT_COLOR1[23:0] DEFAULTCOLOR bit field). For more information about the overlay mechanism, see Section 10.2.4.13.1, *DISPC Overlay Manager*.

10.2.4.14 DISPC Extended 3D Support

The DISPC supports several formats to support 3D displays. The following three sections provide further details.

10.2.4.14.1 DISPC Extended 3D Support - Line Alternative Format

Line alternative format is defined by the HDMI Specification 1.4a. In general the the functionality is:

- Lines from the left and the right frames are interleaved alternatively on the screen to produce a 3D image.
- Required also to support interleaving column-wise to support all possible screen orientations.

The functionality is done in the overlay manager:

- The layers are grouped into two categories based on the z-order: Odd z-order may blend together and will interleave with even z-order pipes, which may blend together.
- Two types of interleaves are possible, line-based interleaving and pixel-based interleaving to support landscape and portrait screen orientations.

The configuration is done from the DISPC_CONFIG1[29:28] TVINTERLEAVE for the TV output, DISPC_CONFIG1[27:26] PLCDINTERLEAVE for the primary LCD, DISPC_CONFIG2[27:26] SLCDINTERLEAVE for the secondary LCD, and DISPC_CONFIG3[27:26] TLCDINTERLEAVE for the third LCD. The following values apply for the these bitfields:

- 0x0: If zero then no interleaving happens in the overlay manager.
- 0x1: Checkerboard pattern:
  - All even pixels on even lines have a contribution from even z-order pipes.
  - All odd pixels on even lines have a contribution from odd z-order pipes.
  - All even pixels on odd lines have a contribution from odd z-order pipes.
  - All odd pixels on odd lines have a contribution from even z-order pipes.
- 0x2: All even lines (all pixels) have a contribution from even z-order pipes. All odd lines (all pixels) have a contribution from the odd z-order pipes.
- 0x3: All even pixels (for all lines) have a contribution from even z-order pipes. All odd pixels (for all lines) have a contribution from the odd z-order pipes.

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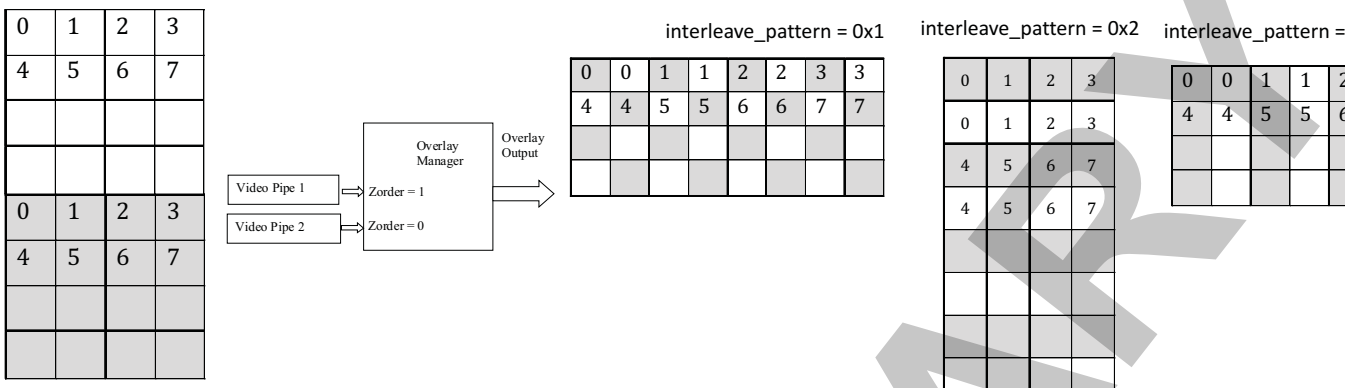
Figure 10-86. DISPC Illustration of 3D Interleaving

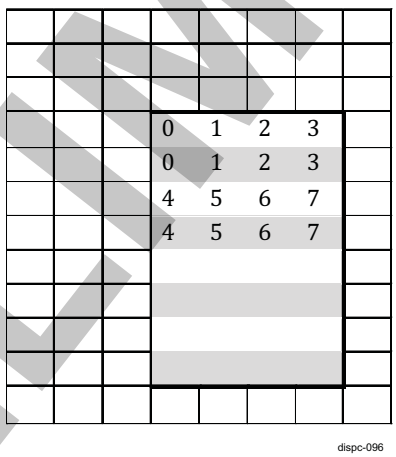


Moreover, from the above figure if interleave_pattern is programmed as 0x2, in this case the entire screen composited by the overlay manager (ppl x lpp) gets sub-divided into odd and even lines. It is possible for a 3D window created using the two pipes to have a non-zero position (i.e. posx and posy not equal to zero).

In such cases depending on the oddness or evenness of the posy setting, the first line in the window maybe from video pipe 1 or video pipe 2.

For instance if the posx =3, posy =3 (set in DISPC_GFX_POSITION, DISPC_VID1_POSITION, DISPC_VID2_POSITION, DISPC_VID3_POSITION registers), then the final composited screen with ppl =8, lpp =12 may look like below:

Figure 10-87. DISPC Illustration of a Non-zero Position of 3D Window



NOTE: In this case the first line comes from the odd-zorder pipe i.e. Video Pipe 1.

The following limitations apply to the 3D Line alternative format:

- Software must ensure that the left/right frames are of same size.
- Software must ensure that in case of line interleaving the sizey is not greater than lpp/2.
- Software must ensure that in case of pixel interleaving the sizex is not greater than ppl/2.
- Software must program PosX and PosY for both left and right frame to be the same.
- Color-keying is not available for 3D formats.
- Since each overlay manager can support 4k x 4k frames, max resolution of each left/right frame will be restricted to 2k x 2k.

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10.2.4.14.2 DISPC Extended 3D Support - Frame Packing Format Format

In this mode the pipe fetches two windows (of SizeX X SizeY) during a complete panel frame (ppl X lpp). The mode is enabled from DISPC_GFX_ATTRIBUTES[10] FRAMEPACKINGMODE and DISPC_VID1_ATTRIBUTES[8], DISPC_VID2_ATTRIBUTES[8], DISPC_VID3_ATTRIBUTES[8] FRAMEPACKINGMODE

The position for the first window is set in DISPC_GFX_POSITION, DISPC_VID1_POSITION, DISPC_VID2_POSITION, DISPC_VID3_POSITION, while the position for the second window is set in DISPC_GFX_POSITION2, DISPC_VID1_POSITION2, DISPC_VID2_POSITION2, DISPC_VID3_POSITION2

When it is detected that a pipe has finished sending the programmed number of lines to the overlay or write-back pipe, a reset is generated for the pipe as well as the DMA channel associated with the pipe. At the same instant, the base address configuration for the DMA channel is changed from the BA0 to the BA1.

Due to the reset the pipe and DMA starts fetching the data from BA1. At the end of the processing of BA1 data, the DMA channel and the pipe become idle and clock gated.

The overlay manager composes the final frame to be sent to the panel and uses the posx, posy coordinates for the first window and posx2, posy2 for the second window.

The following limitations apply to the 3D Frame Packing format:

- Only frame packing for progressive mode is supported. Frame packing of interlaced formats is not supported.
- End-of-window interrupts will be generated twice per outgoing-frame.
- Flip Immediate will not work as expected.
- It is software responsibility to calculate and program the posx2, posy2 as per the active space required by the panel.

10.2.4.14.3 DISPC Extended 3D Support - DLP 3D Format

The DLP 3D format sub-samples the left and right frames across the diagonal before interleaving the frames in a checker-board fashion.

The sub-sampling required on the left and the right frame is complementary. This sampling pattern is also defined in the HDMI 3D Specification 1.4a as two Quincunx matrices. The format is configured from DISPC_GFX_ATTRIBUTES[20:18] SUBSAMPLINGPATTERN, DISPC_VID1_ATTRIBUTES2[11:9], DISPC_VID2_ATTRIBUTES2[11:9], DISPC_VID3_ATTRIBUTES2[11:9] SUBSAMPLINGPATTERN with the following possible configuration:

- 0x0: All pixels from the pipes are used. No sub-sampling.
- 0x1: Quincunx Matrix Odd-position sub-sampling is used.
- 0x2: Quincunx Matrix Even-position sub-sampling is used.
- 0x3 to 0x7: Reserved

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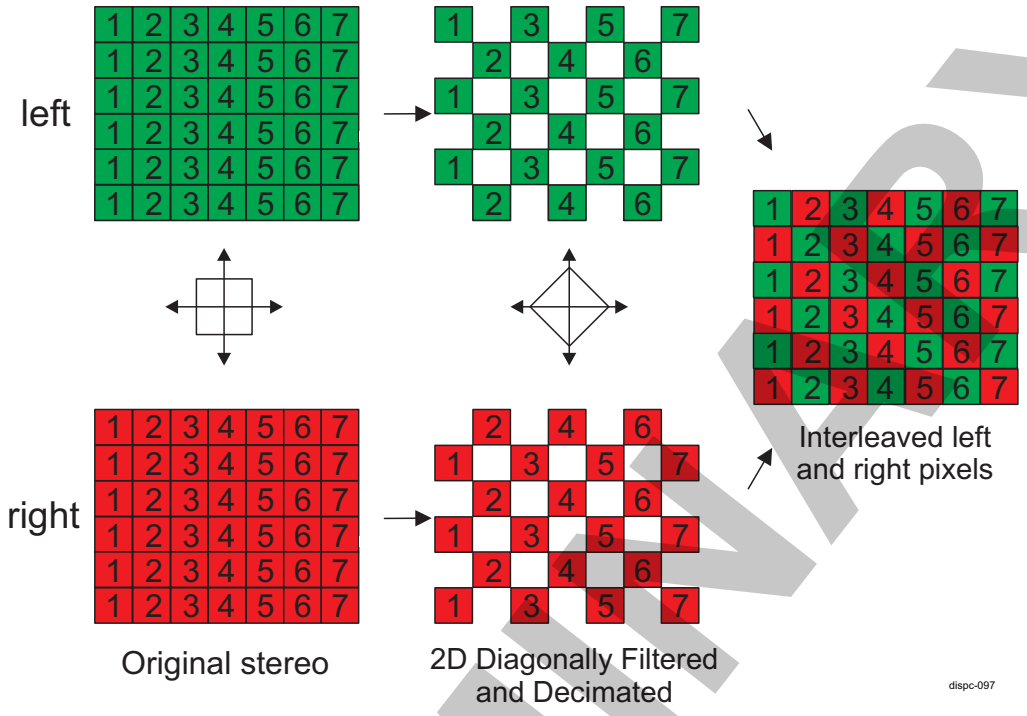
Figure 10-88. DISPC Illustration of DLP 3D Format



The following limitations apply to the DLP 3D Format :

- Even z-order pipes can have only sub-sampling = 0x1. Odd z-order pipes can only have sub-sampling = 0x2.

10.2.4.15 DISPC Shadow Registers

Some DISPC registers are termed *shadow registers*. A shadow register change has no direct effect on the configuration of the DISPC. The registers are shadow registers let software change the values of the registers at any time. When all the registers for a given configuration are into the registers, software must set 1 bit only to validate the configuration. When hardware reaches the end of the current frame and sees that the bit field has been set by software, the new configuration is now the configuration used by the hardware.

NOTE: As a general rule, all shadow registers are updated with the value of their shadows when:

- The interface is enabled.
- The GO bit field of the pipeline, with which the register is associated, is set and the output sync is active.

The bits enabling the hardware to use the new configuration are:

- DISPC_CONTROL1[5] GOLCD bit for all the registers associated to the LCD1 output, and for all registers of WB and DMA, if the LCD1 channel is captured. The update of the registers of the WB and DMA is further delayed by the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNTER bit field or done when the next frame is captured (the DISPC_WB_ATTRIBUTES[26:24] CAPTUREMODE bit field must be different from 0). The update of the registers occurs at the VFP start period.
- DISPC_CONTROL1[6] GOTV bit for all the registers associated to the TV output, and for all registers of WB and DMA, if the TV channel is captured. The update of the registers of the WB and DMA is further delayed by the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNTER bit field or done when the next frame is captured (the DISPC_WB_ATTRIBUTES[26:24] CAPTUREMODE bit field must be different from 0). The update of the registers occurs at the external EVSYNC.
- DISPC_CONTROL2[5] GOLCD bit for all the registers associated to the LCD2 output, and for all registers of WB and DMA, if the LCD2 channel is captured. The update of the registers of the WB and

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DMA is further delayed by the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNTER bit field or done when the next frame is captured (the DISPC_WB_ATTRIBUTES[26:24] CAPTUREMODE bit field must be different from 0). The update of the registers occurs at the VFP start period.

- DISPC_CONTROL3[5] GOLCD bit for all the registers associated to the LCD3 output, and for all registers of WB and DMA, if the LCD3 channel is captured. The update of the registers of the WB and DMA is further delayed by the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNTER bit field or done when the next frame is captured (the DISPC_WB_ATTRIBUTES[26:24] CAPTUREMODE bit field must be different from 0). The update of the registers occurs at the VFP start period.
- DISPC_WB_ATTRIBUTES[0] ENABLE bit for all the registers associated to the WB, if the transfer memory-to-memory is not associated with a channel out.
- The DISPC_CONTROL2[6] GOWB bit and the [5] GOLCD and [6] GOTV bits in the DISPC_CONTROL1/DISPC_CONTROL2 registers, combined with the synchronization event of the channel output selected for write back. This applies to all registers associated with the selected channel out and further delayed by the setting in the DISPC_WB_ATTRIBUTES2[7:0] WBDELAYCOUNT bit field, for all registers of the write back and DMA. The GOWB bit is required to be set only in WB capture mode; it is not required when WB memory-to-memory mode is used.

NOTE: Before setting the GOLCD, GOTV, or GOWB bits, the user must ensure that the bits are cleared. The hardware resets the bits when the update completes.

Table 10-54 lists the shadow registers. Registers that do not have a mark in any column are not shadowed.

Table 10-54. DISPC Shadow Registers

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on VFP Start Period (LCD3 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on END of Frame (WB Pipeline)
DISPC_REVISION					
DISPC_SYSCONFIG					
DISPC_SYSSTATUS					
DISPC_IRQSTATUS					
DISPC_IRQENABLE					
DISPC_CONTROL1	x			x	
DISPC_CONFIG1	x	x	x	x	x
DISPC_DEFAULT_COLOR0	x				
DISPC_DEFAULT_COLOR1				x	
DISPC_TRANS_COLOR0	x				
DISPC_TRANS_COLOR1				x	
DISPC_LINE_STATUS					
DISPC_LINE_NUMBER	x				
DISPC_TIMING_H1	x				
DISPC_TIMING_V1	x				
DISPC_POL_FREQ1	x				
DISPC_DIVISOR1	x				
DISPC_GLOBAL_ALPHA	x	x	x	x	x
DISPC_SIZE_TV				x	
DISPC_SIZE_LCD1	x				
DISPC_GFX_BA_j [(1)]	x	x	x	x	x
DISPC_GFX_POSITION	x	x	x	x	x
DISPC_GFX_SIZE	x	x	x	x	x

(1) j = 0 to 1

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Table 10-54. DISPC Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on VFP Start Period (LCD3 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on END of Frame (WB Pipeline)
DISPC_GFX_ATTRIBUTES	x	x	x	x	x
DISPC_GFX_BUF_THRESHOLD	x	x	x	x	x
DISPC_GFX_BUF_SIZE_STATUS					
DISPC_GFX_ROW_INC	x	x	x	x	x
DISPC_GFX_PIXEL_INC	x	x	x	x	x
DISPC_GFX_TABLE_BA	x	x	x	x	x
DISPC_VID1_BA_j (1)	x	x	x	x	x
DISPC_VID1_POSITION	x	x	x	x	x
DISPC_VID1_SIZE	x	x	x	x	x
DISPC_VID1_ATTRIBUTES	x	x	x	x	x
DISPC_VID1_BUF_THRESHOLD	x	x	x	x	x
DISPC_VID1_BUF_SIZE_STATUS					
DISPC_VID1_ROW_INC	x	x	x	x	x
DISPC_VID1_PIXEL_INC	x	x	x	x	x
DISPC_VID1_FIR	x	x	x	x	x
DISPC_VID1_PICTURE_SIZE	x	x	x	x	x
DISPC_VID1_ACCU_j (2)	x	x	x	x	x
DISPC_VID1_FIR_COEF_H_i (3)	x	x	x	x	x
DISPC_VID1_FIR_COEF_HV_i (3)	x	x	x	x	x
DISPC_VID1_CONV_COEF0	x	x	x	x	x
DISPC_VID1_CONV_COEF1	x	x	x	x	x
DISPC_VID1_CONV_COEF2	x	x	x	x	x
DISPC_VID1_CONV_COEF3	x	x	x	x	x
DISPC_VID1_CONV_COEF4	x	x	x	x	x
DISPC_VID2_BA_j (4)	x	x	x	x	x
DISPC_VID2_POSITION	x	x	x	x	x
DISPC_VID2_SIZE	x	x	x	x	x
DISPC_VID2_ATTRIBUTES	x	x	x	x	x
DISPC_VID2_BUF_THRESHOLD	x	x	x	x	x
DISPC_VID2_BUF_SIZE_STATUS					
DISPC_VID2_ROW_INC	x	x	x	x	x
DISPC_VID2_PIXEL_INC	x	x	x	x	x
DISPC_VID2_FIR	x	x	x	x	x
DISPC_VID2_PICTURE_SIZE	x	x	x	x	x
DISPC_VID2_ACCU_j (4)	x	x	x	x	x
DISPC_VID2_FIR_COEF_H_i (3)	x	x	x	x	x

(2) j = 0 to 1
(3) i = 0 to 7
(4) j = 0 to 1

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Table 10-54. DISPC Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on VFP Start Period (LCD3 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on END of Frame (WB Pipeline)
DISPC_VID2_FIR_COEF_HV_i [3]	x	x	x	x	x
DISPC_VID2_CONV_COEF0	x	x	x	x	x
DISPC_VID2_CONV_COEF1	x	x	x	x	x
DISPC_VID2_CONV_COEF2	x	x	x	x	x
DISPC_VID2_CONV_COEF3	x	x	x	x	x
DISPC_VID2_CONV_COEF4	x	x	x	x	x
DISPC_DATA1_CYCLE1	x				
DISPC_DATA1_CYCLE2	x				
DISPC_DATA1_CYCLE3	x				
DISPC_VID1_FIR_COEF_V_i [3]	x	x	x	x	x
DISPC_VID2_FIR_COEF_V_i [3]	x	x	x	x	x
DISPC_CPR1_COEF_R	x				
DISPC_CPR1_COEF_G	x				
DISPC_CPR1_COEF_B	x				
DISPC_GFX_PRELOAD	x	x	x	x	x
DISPC_VID1_PRELOAD	x	x	x	x	x
DISPC_VID2_PRELOAD	x	x	x	x	x
DISPC_CONTROL2		x		x	x
DISPC_VID3_ACCU_j [5]	x	x	x	x	x
DISPC_VID3_BA_j [5]	x	x	x	x	x
DISPC_VID3_FIR_COEF_H_i [5]	x	x	x	x	x
DISPC_VID3_FIR_COEF_HV_i [5]	x	x	x	x	x
DISPC_VID3_FIR_COEF_V_i [5]	x	x	x	x	x
DISPC_VID3_ATTRIBUTES	x	x	x	x	x
DISPC_VID3_CONV_COEF0	x	x	x	x	x
DISPC_VID3_CONV_COEF1	x	x	x	x	x
DISPC_VID3_CONV_COEF2	x	x	x	x	x
DISPC_VID3_CONV_COEF3	x	x	x	x	x
DISPC_VID3_CONV_COEF4	x	x	x	x	x
DISPC_VID3_BUF_SIZE_STATUS					
DISPC_VID3_BUF_THRESHOLD	x	x	x	x	x
DISPC_VID3_FIR	x	x	x	x	x
DISPC_VID3_PICTURE_SIZE	x	x	x	x	x
DISPC_VID3_PIXEL_INC	x	x	x	x	x
DISPC_VID3_POSITION	x	x	x	x	x
DISPC_VID3_PRELOAD	x	x	x	x	x
DISPC_VID3_ROW_INC	x	x	x	x	x
DISPC_VID3_SIZE	x	x	x	x	x

[5] i = 0 to 7

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Table 10-54. DISPC Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on VFP Start Period (LCD3 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on END of Frame (WB Pipeline)
DISPC_DEFAULT_COLOR2		x			
DISPC_TRANS_COLOR2		x			
DISPC_CPR2_COEF_B		x			
DISPC_CPR2_COEF_G		x			
DISPC_CPR2_COEF_R		x			
DISPC_DATA2_CYCLE1		x			
DISPC_DATA2_CYCLE2		x			
DISPC_DATA2_CYCLE3		x			
DISPC_SIZE_LCD2		x			
DISPC_TIMING_H2		x			
DISPC_TIMING_V2		x			
DISPC_POL_FREQ2		x			
DISPC_DIVISOR2		x			
DISPC_WB_ACCU_j [6]	x	x	x	x	x
DISPC_WB_BA_j [6]	x	x	x	x	x
DISPC_WB_FIR_COEF_H_i [5]	x	x	x	x	x
DISPC_WB_FIR_COEF_HV_i [7]	x	x	x	x	x
DISPC_WB_FIR_COEF_V_i [7]	x	x	x	x	x
DISPC_WB_ATTRIBUTES	x	x	x	x	x
DISPC_WB_CONV_COEF0	x	x	x	x	x
DISPC_WB_CONV_COEF1	x	x	x	x	x
DISPC_WB_CONV_COEF2	x	x	x	x	x
DISPC_WB_CONV_COEF3	x	x	x	x	x
DISPC_WB_CONV_COEF4	x	x	x	x	x
DISPC_WB_BUF_SIZE_STATUS	x	x	x	x	x
DISPC_WB_BUF_THRESHOLD	x	x	x	x	x
DISPC_WB_FIR	x	x	x	x	x
DISPC_WB_PICTURE_SIZE	x	x	x	x	x
DISPC_WB_PIXEL_INC	x	x	x	x	x
DISPC_WB_ROW_INC	x	x	x	x	x
DISPC_WB_SIZE	x	x	x	x	x
DISPC_VID1_BA_UV_j [8]	x	x	x	x	x
DISPC_VID2_BA_UV_j [8]	x	x	x	x	x
DISPC_VID3_BA_UV_j [8]	x	x	x	x	x
DISPC_WB_BA_UV_j [8]	x	x	x	x	x
DISPC_CONFIG2	x	x	x	x	x
DISPC_VID1_ATTRIBUTES2	x	x	x	x	x
DISPC_VID2_ATTRIBUTES2	x	x	x	x	x
DISPC_VID3_ATTRIBUTES2	x	x	x	x	x

[6] j = 0 to 1
[7] i = 0 to 7
[8] j = 0 to 1

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Table 10-54. DISPC Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on VFP Start Period (LCD3 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on END of Frame (WB Pipeline)
DISPC_GAMMA_TABLE0					
DISPC_GAMMA_TABLE1					
DISPC_GAMMA_TABLE2					
DISPC_VID1_FIR2	x	x	x	x	x
DISPC_VID1_ACCU2_j [8]	x	x	x	x	x
DISPC_VID1_FIR_COEF_H2_i [7]	x	x	x	x	x
DISPC_VID1_FIR_COEF_HV2_i [7]	x	x	x	x	x
DISPC_VID1_FIR_COEF_V2_i [7]	x	x	x	x	x
DISPC_VID2_FIR2	x	x	x	x	x
DISPC_VID2_ACCU2_j [8]	x	x	x	x	x
DISPC_VID2_FIR_COEF_H2_i [7]	x	x	x	x	x
DISPC_VID2_FIR_COEF_HV2_i [7]	x	x	x	x	x
DISPC_VID2_FIR_COEF_V2_i [7]	x	x	x	x	x
DISPC_VID3_FIR2	x	x	x	x	x
DISPC_VID3_ACCU2_j [9]	x	x	x	x	x
DISPC_VID3_FIR_COEF_H2_i [10]	x	x	x	x	x
DISPC_VID3_FIR_COEF_HV2_i [10]	x	x	x	x	x
DISPC_VID3_FIR_COEF_V2_i [10]	x	x	x	x	x
DISPC_WB_FIR2	x	x	x	x	x
DISPC_WB_ACCU2_j [9]	x	x	x	x	x
DISPC_WB_FIR_COEF_H2_i [10]	x	x	x	x	x
DISPC_WB_FIR_COEF_HV2_i [10]	x	x	x	x	x
DISPC_WB_FIR_COEF_V2_i [10]	x	x	x	x	x
DISPC_GLOBAL_BUFFER					
DISPC_DIVISOR					
DISPC_WB_ATTRIBUTES2	x	x	x	x	x
DISPC_DEFAULT_COLOR3			x		
DISPC_TRANS_COLOR3			x		
DISPC_CPR3_COEF_B			x		
DISPC_CPR3_COEF_G			x		
DISPC_CPR3_COEF_R			x		
DISPC_DATA3_CYCLE1			x		
DISPC_DATA3_CYCLE2			x		
DISPC_DATA3_CYCLE3			x		
DISPC_SIZE_LCD3			x		

[9] j = 0 to 1
[10] i = 0 to 7

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Table 10-54. DISPC Shadow Registers (continued)

Shadow Register Name	Updated on VFP Start Period (LCD1 Pipeline)	Updated on VFP Start Period (LCD2 Pipeline)	Updated on VFP Start Period (LCD3 Pipeline)	Updated on External VSYNC (TV Pipeline)	Updated on END of Frame (WB Pipeline)
DISPC_DIVISOR3			x		
DISPC_POL_FREQ3			x		
DISPC_TIMING_H3			x		
DISPC_TIMING_V3			x		
DISPC_CONTROL3			x		
DISPC_CONFIG3			x		
DISPC_GAMMA_TABLE3			x		
DISPC_BA0_FLIPIMMEDIATE_EN					
DISPC_GLOBAL_MFLAG_ATTRIBUTE					
DISPC_GFX_MFLAG_THRESHOLD	x	x	x	x	x
DISPC_VID1_MFLAG_THRESHOLD	x	x	x	x	x
DISPC_VID2_MFLAG_THRESHOLD	x	x	x	x	x
DISPC_VID3_MFLAG_THRESHOLD	x	x	x	x	x
DISPC_WB_MFLAG_THRESHOLD	x	x	x	x	x
DISPC_GFX_POSITION2	x	x	x	x	x
DISPC_VID1_POSITION2	x	x	x	x	x
DISPC_VID2_POSITION2	x	x	x	x	x
DISPC_VID3_POSITION2	x	x	x	x	x

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10.2.5 DISPC Programming Guide

10.2.5.1 DISPC Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

10.2.5.1.1 DISPC Global Initialization

10.2.5.1.1.1 DISPC Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the DISPC module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DISPC. For more information, see Section 10.2.3, *DISPC Integration*, and , *DISPC Environment*.

Table 10-55. DISPC Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. See , *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
Control module	Module-specific pad muxing and configuration must be set in the control module. See , *PAD Functional Multiplexing and Configuration*, in *Chapter 18, Control Module*.
MPU INTC or DSP INTC	MPU and/or DSP interrupt controller configuration must be done to enable the interrupts from the DISPC. See , *Interrupt Controllers Overview*, in Chapter 17, *Interrupt Controllers*.
Interconnect	For more information about interconnect configuration, see , L3 Interconnect, in Chapter 14, *Interconnects*.

10.2.5.1.2 DISPC Operational Modes Configuration

Table 10-56 lists the steps to configure the operational modes in the DISPC.

Table 10-56. DISPC Configuration

Step	Register/Bit Field/Programming Model
For a GFX pipeline configuration	
Configure the GFX DMA channel.	See Table 10-57.
Configure the GFX pipeline.	See Table 10-60.
Configure the LCD or TV output.	For LCD output, see Table 10-78.
	For TV output, see Table 10-85.
For a Video pipeline configuration	
Configure the video DMA channel.	See Table 10-58.
Configure the video pipeline.	See Table 10-65.
Configure the LCD or TV output.	For LCD output, see Table 10-78.
	For TV output, see Table 10-85.
For a WB pipeline configuration	
Configure the WB DMA channel.	See Table 10-59.
Configure the WB pipeline.	For video pipelines, see Table 10-73.

10.2.5.1.2.1 DISPC DMA Configuration

10.2.5.1.2.1.1 DISPC Main Sequence – DISPC DMA Channel Configuration

This procedure describes the parameters of the GFX, video, and WB DMA channel parameters (see Table 10-57 through Table 10-59, respectively).

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Table 10-57. DISPC Configure the GFX DMA Channel

Step	Register/Bit Field/Programming Model	Value
Set the base address for RGB pixel format or BITMAP component format according to memory access type, rotation, mirroring (see Section 10.2.4.6, *DISPC DMA Engine*).	DISPC_GFX_BA_j[31:0] BA	0x—
Set the rotation flag.	DISPC_GFX_ATTRIBUTES[13:12] ROTATION	0x–
Set the number of bytes to increment at the end of the row.	DISPC_GFX_ROW_INC[31:0] ROWINC	0x–
Set the number of bytes to increment between two pixels.	DISPC_GFX_PIXEL_INC[7:0] PIXELINC	0x–
Determine the FIFO preload mode.	DISPC_GFX_ATTRIBUTES[11] BUFPRELOAD	0x–
Set the preload value.	DISPC_GFX_PRELOAD[11:0] PRELOAD	0x–
Determine the burst type.	DISPC_GFX_ATTRIBUTES[29] BURSTTYPE	0x–
Set the burst size.	DISPC_GFX_ATTRIBUTES[7:6] BURSTSIZE	0x–
Set the high level of DMA FIFO threshold.	DISPC_GFX_BUF_THRESHOLD[31:16] BUFHIGHTRESHOLD	0x–
Set the low level of DMA FIFO threshold.	DISPC_GFX_BUF_THRESHOLD[15:0] BUFLOWTRESHOLD	0x–
Enable self-refresh.	DISPC_GFX_ATTRIBUTES[24] SELFREFRESH	0x–
Select priority over the other pipeline.	DISPC_GFX_ATTRIBUTES[23] ARBITRATION	0x–

Table 10-58. DISPC Configure the Video DMA Channel

Step	Register/Bit Field/Programming Model	Value
Set the base address for RGB pixel format or Y component format according to memory access type, rotation, mirroring (seeSection 10.2.4.6, *DISPC DMA Engine*).	DISPC_VIDp_BA_j[31:0] BA	0x—
Set the base address for Cb and Cr components according to memory access type, rotation, mirroring (seeSection 10.2.4.6, *DISPC DMA Engine*)[(1)].	DISPC_VIDp_BA_UV_j[31:0] BA	0x—
Set the rotation flag.	DISPC_VIDp_ATTRIBUTES[13:12] ROTATION	0x–
Set the number of bytes to increment at the end of the row.	DISPC_VIDp_ROW_INC[31:0] ROWINC	0x–
Set the number of bytes to increment between two pixels.	DISPC_VIDp_PIXEL_INC[7:0] PIXELINC	0x–
Set the X original image size.	DISPC_VIDp_PICTURE_SIZE[10:0] MEMSIZEX	0x–
Set the Y original image size.	DISPC_VIDp_PICTURE_SIZE[27:16] MEMSIZEY	0x–
Determine the FIFO preload mode.	DISPC_VIDp_ATTRIBUTES[19] BUFPRELOAD	0x–
Set the preload value.	DISPC_VIDp_PRELOAD[11:0] PRELOAD	0x–
Determine the burst type.	DISPC_VIDp_ATTRIBUTES[29] BURSTTYPE	0x–
Set the burst size.	DISPC_VIDp_ATTRIBUTES[15:14] BURSTSIZE	0x–
Set the high level of DMA FIFO threshold.	DISPC_VIDp_BUF_THRESHOLD[31:16] BUFHIGHTRESHOLD	0x–
Set the low level of DMA FIFO threshold.	DISPC_VIDp_BUF_THRESHOLD[15:0] BUFLOWTRESHOLD	0x–
Enable self-refresh.	DISPC_VIDp_ATTRIBUTES[24] SELFREFRESH	0x–
Select priority over the other pipeline.	DISPC_VIDp_ATTRIBUTES[23] ARBITRATION	0x–

(1) Applicable only for YUV pixel format

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Table 10-59. DISPC Configure the WB DMA Channel

Step	Register/Bit Field/Programming Model	Value
Set the base address for RGB pixel format or Y component format according to memory access type, rotation, mirroring (see Section 10.2.4.6, *DISPC DMA Engine*).	DISPC_WB_BA_j[31:0] BA	0x—
Set the base address for Cb and Cr components according to memory access type, rotation, mirroring (see Section 10.2.4.6, *DISPC DMA Engine*) (1).	DISPC_WB_BA_UV_j[31:0] BA	0x—
Set the stride of CbCr component (2).	DISPC_WB_ATTRIBUTES[22] DOUBLESTRIDE	0x–
Set the rotation flag.	DISPC_WB_ATTRIBUTES[13:12] ROTATION	0x–
Set the number of bytes to increment at the end of the row.	DISPC_WB_ROW_INC[31:0] ROWINC	0x–
Set the number of bytes to increment between two pixels.	DISPC_WB_PIXEL_INC[7:0] PIXELINC	0x–
Set the X final image size in system memory.	DISPC_WB_PICTURE_SIZE[10:0] ORGSIZEX	0x–
Set the Y final image size in system memory.	DISPC_WB_PICTURE_SIZE[27:16] ORGSIZEY	0x–
Set the burst size.	DISPC_WB_ATTRIBUTES[15:14] BURSTSIZE	0x–
Set the high level of DMA FIFO threshold.	DISPC_WB_BUF_THRESHOLD[31:16] BUFHIGHTRESHOLD	0x–
Set the low level of DMA FIFO threshold.	DISPC_WB_BUF_THRESHOLD[15:0] BUFLOWTRESHOLD	0x–
Select priority over the other pipeline.	DISPC_WB_ATTRIBUTES[23] ARBITRATION	0x–

(1) Applicable only for YUV pixel format
(2) Applicable only for YUV pixel format

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10.2.5.1.2.2 DISPC GFX Pipeline Configuration

10.2.5.1.2.2.1 DISPC Main Sequence – Configure the GFX Pipeline

This procedure details the steps for a GFX pipeline configuration (see Table 10-60).

Table 10-60. DISPC Configure the GFX Pipeline

Step	Register/Bit Field/Programming Model	Value
Configure the GFX window.	See Table 10-61.	
Configure the GFX pipeline processing.	See Table 10-62.	
Configure the GFX pipeline layer output.	See Table 10-64.	
Validate the GFX configuration according to outputs associated to the pipeline.	DISPC_CONTROL1[5] GOLCD	
	DISPC_CONTROL2[5] GOLCD	
	DISPC_CONTROL2[6] GOWB	
	DISPC_CONTROL1[6] GOTV	
Enable the GFX pipeline.	DISPC_GFX_ATTRIBUTES[0] ENABLE	0x1

10.2.5.1.2.2.2 DISPC Subsequence – Configure the GFX Window

This subsequence describes the parameters of the image to be displayed on the LCD panel (see Table 10-61).

Table 10-61. DISPC Configure the GFX Window

Step	Register/Bit Field/Programming Model	Value
Select the format of image.	DISPC_GFX_ATTRIBUTES[4:1] FORMAT	0x–
Set the X size of image to be displayed onto LCD panel.	DISPC_GFX_SIZE[11:0] SIZEX	0x–
Set the Y size of image to be displayed onto LCD panel.	DISPC_GFX_SIZE[27:16] SIZEY	0x–
Set the X position of image in respect to LCD panel.	DISPC_GFX_POSITION[10:0] POSX	0x–
Set the Y position of image in respect to LCD panel.	DISPC_GFX_POSITION[26:16] POSY	0x–

10.2.5.1.2.2.3 DISPC Subsequence – Configure the GFX Pipeline Processing

This subsequence describes the steps to configure the GFX pipeline processing in the DISPC (seeTable 10-62).

Table 10-62. DISPC Configure the GFX Pipeline Processing

Step	Register/Bit Field/Programming Model	Value
Enable replication logic.	DISPC_GFX_ATTRIBUTES[5] REPLICATIONENABLE	0x1
Enable nibble mode.	DISPC_GFX_ATTRIBUTES[9] NIBBLEMODE	0x1
Enable antiflicker filter.	DISPC_GFX_ATTRIBUTES[24] ANTIFLICKER	0x1
Configure the palette table.	See Table 10-63.	0x–

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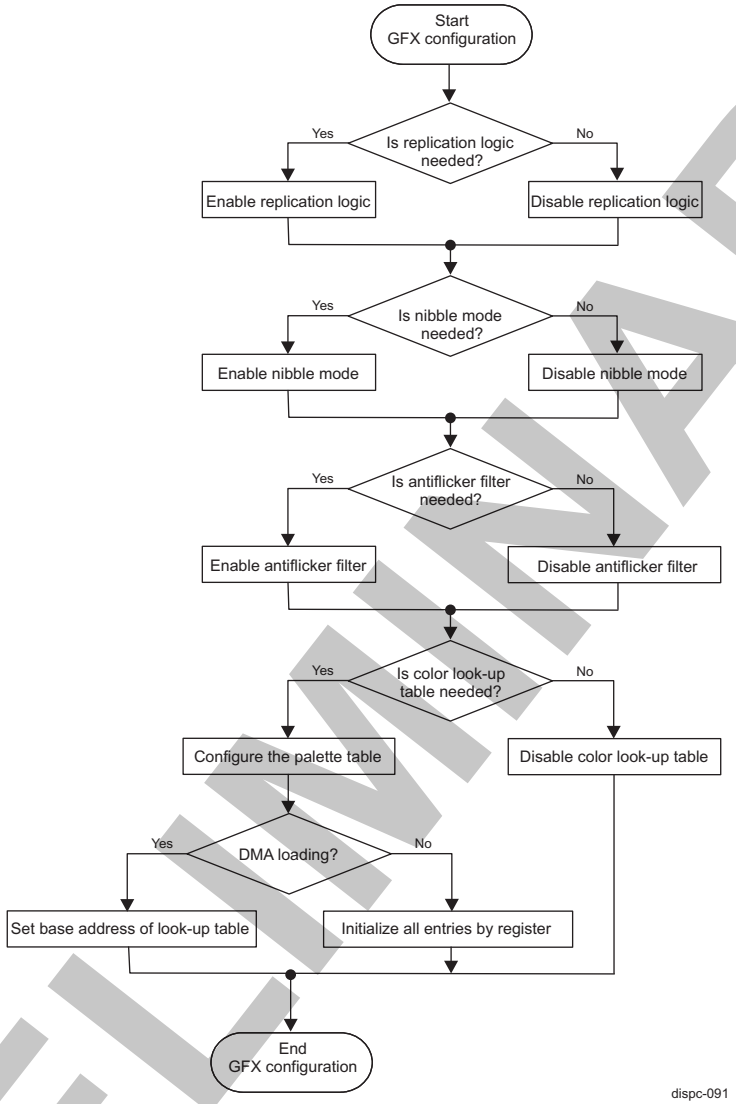
Figure 10-89 shows the configuration of the DISPC video pipeline processing.

Figure 10-89. DISPC Video Pipeline Processing Configuration



10.2.5.1.2.2.4 DISPC Subsequence – Configure the Palette Table

This subsequence describes the settings to configure the CLUT as a palette for the GFX pipeline (see Table 10-63).

NOTE:

- Software must ensure there is no visible effect when modifying the table because it is not under hardware control. The synchronization done using the DMA engine inside the DISPC to load the table when it is not used for displaying the picture on the screen is not present for this mode.
- If the GFX pipeline is in BITMAP pixel format, gamma corrections are not available for LCD1.

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Table 10-63. DISPC Configure the Palette Table

Step	Register/Bit Field/Programming Model	Value
Set look-up table as palette table.	DISPC_CONFIG1[3] PALETTEGAMMATABLE	0x0
Select the load mode of the palette look-up table.	DISPC_CONFIG1[2:1] LOADMODE	0x–
DMA loading		
Set base address of look-up table.	DISPC_GFX_TABLE_BA[31:0] TABLEBA	0x–
Initialize all entries by register		
Initialize all entries for the palette table by setting the table index and the RGB values associated to this index.	DISPC_GAMMA_TABLE0[31:24][23:16][15:8][7:0], INDEX, VALUE_R, VALUE_G, VALUE_B	0x–

10.2.5.1.2.5 DISPC Subsequence – Configure the GFX Pipeline Layer Output

This subsequence describes the video layer settings available at the pipeline level necessary when using the overlay manager (see Table 10-64).

Table 10-64. DISPC Configure the GFX Pipeline Layer Output

Step	Register/Bit Field/Programming Model	Value
Set the LCD/TV output.	DISPC_GFX_ATTRIBUTES[8] CHANNELOUT	0x–
If DISPC_GFX_ATTRIBUTES[8] = 0, set the LCD output.	DISPC_GFX_ATTRIBUTES[31:30] CHANNELOUT2	0x–
Set the Z-order priority of the layer for overlay manager.	DISPC_GFX_ATTRIBUTES[27:26] ZORDER	0x–
Enable the video pipeline Z-order.	DISPC_GFX_ATTRIBUTES[25] ZORDERENABLE	0x–
Set the Global Alpha value for the alpha blender unit.	DISPC_GLOBAL_ALPHA[7:0] GFXGLOBALALPHA	0x–

10.2.5.1.2.3 DISPC Video Pipeline Configuration

10.2.5.1.2.3.1 DISPC Main Sequence – Configure the Video Pipeline

This sequence describes the steps to configure the video pipeline (see Table 10-65).

Table 10-65. DISPC Configure the Video Pipeline

Step	Register/Bit Field/Programming Model	Value
Configure the video window.	See Table 10-66.	
Configure the video pipeline processing.	See Table 10-67.	
Configure the video pipeline layer output.	See Table 10-72.	
Validate the video configuration according to outputs associated to the pipeline.	DISPC_CONTROL1[5] GOLCD	
	DISPC_CONTROL2[5] GOLCD	
	DISPC_CONTROL2[6] GOWB	
	DISPC_CONTROL1[6] GOTV	
Enable video pipeline.	DISPC_VIDp_ATTRIBUTES[0] ENABLE	0x1

10.2.5.1.2.3.2 DISPC Subsequence – Configure the Video Window

This subsequence describes the parameters of the image to be displayed on the LCD panel (see Table 10-66).

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Table 10-66. DISPC Configure the Video Window

Step	Register/Bit Field/Programming Model	Value
Select the format of image.	DISPC_VIDp_ATTRIBUTES[4:1] FORMAT	0x–
Set the X size of image to be displayed onto LCD panel.	DISPC_VIDp_SIZE[11:0] SIZEX	0x–
Set the Y size of image to be displayed onto LCD panel.	DISPC_VIDp_SIZE[27:16] SIZEY	0x–
Set the X position of image in respect to LCD panel.	DISPC_VIDp_POSITION[10:0] POSX	0x–
Set the Y position of image in respect to LCD panel.	DISPC_VIDp_POSITION[26:16] POSY	0x–

10.2.5.1.2.3.3 DISPC Subsequence – Configure the Video Pipeline Processing

This subsequence describes the steps to configure video pipeline processing (see Table 10-67 and Figure 10-90).

Table 10-67. DISPC Configure the Video Pipeline Processing

Step	Register/Bit Field/Programming Model	Value
Select the video pipeline configuration 1 or 2.	DISPC_VIDp_ATTRIBUTES2[8] YUVCHROMARESAMPLING	0x–
Enable/disable replication logic(1).	DISPC_VIDp_ATTRIBUTES[10] REPLICATIONENABLE	0x1
Configure the VC-1 range mapping(1).	See Section 10.2.5.1.2.3.4.	
Configure the video color space conversion(1).	See Section 10.2.5.1.2.3.5.	
Configure the video scaler unit(1).	See Section 10.2.5.1.2.3.6.	

(1) This module configuration can be optional depending on:
- The video mode configuration selected. See Figure 10-90.
- The video format and application needs

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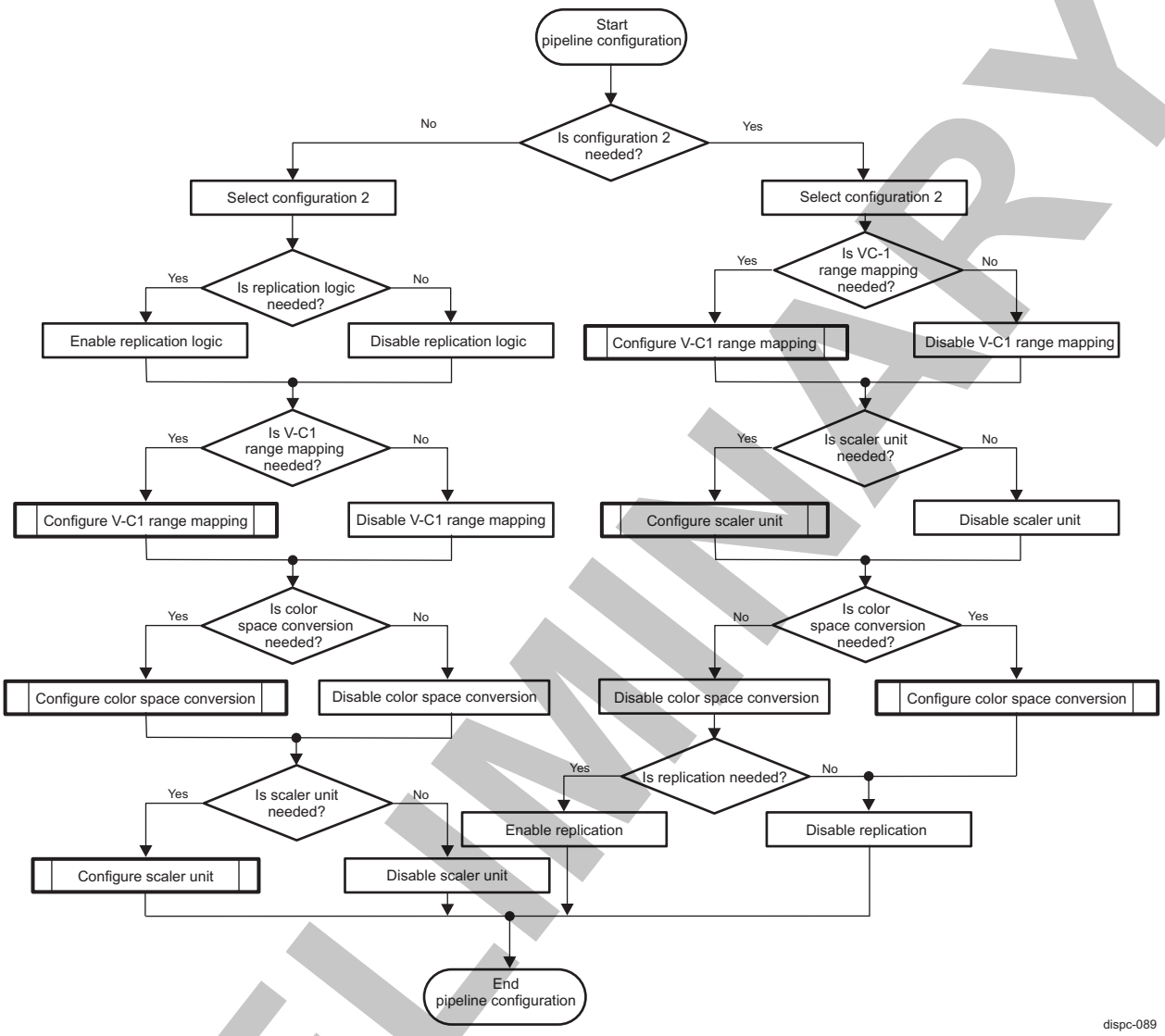
Figure 10-90. DISPC Video Pipeline Processing Configuration



10.2.5.1.2.3.4 DISPC Subsequence – Configure the VC-1 Range Mapping

This subsequence describes the steps to configure the VC-1 range mapping (see Table 10-68).

Table 10-68. DISPC Configure the VC-1 Range Mapping

Step	Register/Bit Field/Programming Model	Value
Set the Y component VC-1 range mapping.	DISPC_VIDp_ATTRIBUTES2[3:1] VC1_RANGE_Y	0x–
Set the Cb and Cr component VC-1 range mapping.	DISPC_VIDp_ATTRIBUTES2[6:4] VC1_RANGE_CBCR	0x–
Enable VC-1 range mapping.	DISPC_VIDp_ATTRIBUTES2[0] VC1ENABLE	0x1

10.2.5.1.2.3.5 DISPC Subsequence – Configure the Video Color Space Conversion

This subsequence describes the steps to configure the video color space conversion (see Table 10-69).

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Table 10-69. DISPC Configure the Video Color Space Conversion

Step	Register/Bit Field/Programming Model	Value
Select the range of the color space conversion.	DISPC_VIDp_ATTRIBUTES[11] FULLRANGE	0x–
Set the RCr and RY coefficients.	DISPC_VIDp_CONV_COEF0[26:16][10:0] RCR, RY	0x–
Set the GY and RCb coefficients.	DISPC_VIDp_CONV_COEF1[26:16][10:0] GY, RCB	0x–
Set the GCb and GCr coefficients.	DISPC_VIDp_CONV_COEF2[26:16][10:0] GCB, GCR	0x–
Set the BCr and BY coefficients.	DISPC_VIDp_CONV_COEF3[26:16][10:0] BCR, BY	0x–
Set the BCb coefficient.	DISPC_VIDp_CONV_COEF4[10:0] BCB	0x–
Enable color space conversion.	DISPC_VIDp_ATTRIBUTES[9] COLORCONVENABLE	0x1

10.2.5.1.2.3.6 DISPC Subsequence – Configure the Video Scaler Unit

This subsequence configures the video scaler unit. Table 10-70 is applicable for RGB pixel format. Table 10-70 and Table 10-71 are applicable for YUV pixel format.

Table 10-70. DISPC Configure the Video Scaler Unit for RGB Pixel Formats or Y Component

Step	Register/Bit Field/Programming Model	Value
Configure horizontal scaling		
Set the horizontal resizing ratio.	DISPC_VIDp_FIR[12:0] FIRHINC	0x–
Set the horizontal FIR coefficients.	DISPC_VIDp_FIR_COEF_H_i[31:24][23:16][15:8] [7:0] FIRHC3, FIRHC2, FIRHC1, FIRHC0	0x–
	DISPC_VIDp_FIR_COEF_HV_i[7:0] FIRHC4	0x–
Set the horizontal accumulators value.	DISPC_VIDp_ACCU_j[10:0] HORIZONTALACCU	0x–
Configure vertical scaling		
Select number of vertical taps.	DISPC_VIDp_ATTRIBUTES[21] VERTICALTAPS	0x–
Set the vertical resizing ratio.	DISPC_VIDp_FIR[28:16] FIRVINC	0x–
Set the vertical FIR coefficients for RGB pixel format or Y component.	DISPC_VIDp_FIR_COEF_HV_i[31:24][23:16][15:8] FIRVC2, FIRVC1, FIRVC0	0x–
	Only for 5-taps vertical: DISPC_VIDp_FIR_COEF_V_i[15:8][7:0] FIRVC22, FIRVC00	0x–
Set the vertical accumulators value for RGB pixel format or Y component.	DISPC_VIDp_ACCU_j[26:16] VERTICALACCU	0x–
Enable horizontal and vertical scaler unit.	DISPC_VIDp_ATTRIBUTES[6:5] RESIZEENABLE	0x–

Table 10-71. DISPC Configure the Video Scaler Unit for Cb and Cr Components

Step	Register/Bit Field/Programming Model	Value
Configure horizontal scaling		
Set the horizontal resizing ratio for Cb and Cr components.	DISPC_VIDp_FIR2[12:0] FIRHINC	0x–
Set the horizontal FIR coefficients for Cb and Cr components.	DISPC_VIDp_FIR_COEF_H2_i[31:24][23:16][15:8] [7:0] FIRHC3, FIRHC2, FIRHC1, FIRHC0	0x–
	DISPC_VIDp_FIR_COEF_HV2_i[7:0] FIRHC4	0x–
Set the horizontal accumulators value for Cb and Cr components.	DISPC_VIDp_ACCU2_j[10:0] HORIZONTALACCU	0x–
Configure vertical scaling		
Set the vertical resizing ratio for Cb and Cr components.	DISPC_VIDp_FIR2[28:16] FIRVINC	0x–
Set the vertical FIR coefficients for Cb and Cr components.	DISPC_VIDp_FIR_COEF_HV2_i[31:24][23:16][15:8] FIRVC2, FIRVC1, FIRVC0	0x–
	Only for 5-taps vertical: DISPC_VIDp_FIR_COEF_V2_i[15:8][7:0] FIRVC22, FIRVC00	0x–

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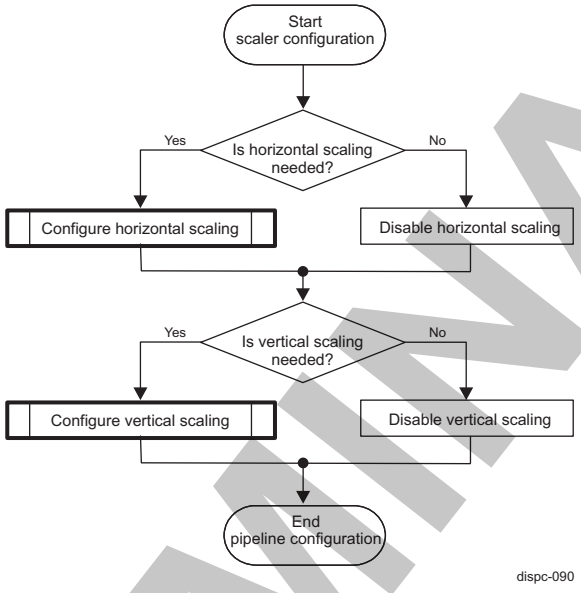
Table 10-71. DISPC Configure the Video Scaler Unit for Cb and Cr Components (continued)

Step	Register/Bit Field/Programming Model	Value
Set the vertical accumulators value for Cb and Cr components.	DISPC_VIDp_ACCU2_j[26:16] VERTICALACCU	0x–

Figure 10-91 shows the programming flow of the DISPC scaler unit.

Figure 10-91. DISPC Scaler Unit Programming Flow



10.2.5.1.2.3.7 DISPC Subsequence – Configure the Video Pipeline Layer Output

This subsequence describes the video layer settings available at the pipeline level necessary when using the overlay manager (see Table 10-72).

Table 10-72. DISPC Configure the Video Pipeline Layer Output

Step	Register/Bit Field/Programming Model	Value
Set the LCD/TV output.	DISPC_VIDp_ATTRIBUTES[16] CHANNELOUT	0x–
If DISPC_VIDp_ATTRIBUTES[16] = 0, set the LCD output.	DISPC_VIDp_ATTRIBUTES[31:30] CHANNELOUT2	0x–
Set the Z-order priority of the layer for overlay manager.	DISPC_VIDp_ATTRIBUTES[27:26] ZORDER	0x–
Enable the video pipeline Z-order.	DISPC_VIDp_ATTRIBUTES[25] ZORDERENABLE	0x–
Set the Global Alpha value for the alpha blender unit.	DISPC_GLOBAL_ALPHA[31:24][23:16][15:8] VID3GLOBALALPHA, VID2GLOBALALPHA, VID1GLOBALALPHA	0x–

10.2.5.1.2.4 DISPC WB Pipeline Configuration

10.2.5.1.2.4.1 DISPC Main Sequence – Configure the WB Pipeline

This procedure describes the steps to configure the WB pipeline (see Table 10-73).

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Table 10-73. DISPC Configure the WB Pipeline

Step	Register/Bit Field/Programming Model	Value
Configure the capture window.	See Table 10-74.	
Configure the WB scaler unit.	See Table 10-75.	
Enable truncation logic to match pixel size defined in the format of image DISPC_WB_ATTRIBUTES[4:1] FORMAT.	DISPC_WB_ATTRIBUTES[10] TRUNCATIONENABLE	0x–
If DISPC_WB_ATTRIBUTES[10] !=, configure the WB color space conversion unit.	See Table 10-77.	
Validate the configuration according to the registers modification.	DISPC_CONTROL2[6] GOWB	
Enable WB pipeline.	DISPC_WB_ATTRIBUTES[0] ENABLE	0x1

10.2.5.1.2.4.2 DISPC Subsequence – Configure the Capture Window

This subsequence describes the parameters of the image to be captured in the system memory (see Table 10-74).

Table 10-74. DISPC Configure the Capture Window

Step	Register/Bit Field/Programming Model	Value
Set the input source.	DISPC_WB_ATTRIBUTES[18:16] CHANNELIN	0x–
Select the format of image.	DISPC_WB_ATTRIBUTES[4:1] FORMAT	0x–
Set the X size of image to be captured.	DISPC_WB_SIZE[10:0] SIZEX	0x–
Set the Y size of image to be captured.	DISPC_WB_SIZE[10:0] SIZEY	0x–

10.2.5.1.2.4.3 DISPC Subsequence – Configure the WB Scaler Unit

This subsequence configures the scaler unit. Table 10-75 is applicable for RGB pixel format. Table 10-75 and Table 10-76 are applicable for YUV pixel format.

Table 10-75. DISPC Configure the WB Scaler Unit for RGB Pixel Formats or Y Component

Step	Register/Bit Field/Programming Model	Value
Configure horizontal scaling		
Set the horizontal resizing ratio.	DISPC_WB_FIR[12:0] FIRHINC	0x–
Set the horizontal FIR coefficients.	DISPC_WB_FIR_COEF_H_i[31:24][23:16][15:8][7:0] FIRHC3, FIRHC2, FIRHC1, FIRHC0	0x–
	DISPC_WB_FIR_COEF_HV_i[7:0] FIRHC4	0x–
Set the horizontal accumulators value.	DISPC_WB_ACCU_j[10:0] HORIZONTALACCU	0x–
Configure vertical scaling		
Select number of vertical taps.	DISPC_WB_ATTRIBUTES[21] VERTICALTAPS	0x–
Set the vertical resizing ratio.	DISPC_WB_FIR[28:16] FIRVINC	0x–
Set the vertical FIR coefficients for RGB pixel format or Y component.	DISPC_WB_FIR_COEF_HV_i[31:24][23:16][15:8] FIRVC2, FIRVC1, FIRVC0	0x–
	Only for 5-taps vertical: DISPC_WB_FIR_COEF_V_i[15:8][7:0] FIRVC22, FIRVC00	0x–
Set the vertical accumulators value for RGB pixel format or Y component.	DISPC_WB_ACCU_j[26:16] VERTICALACCU	0x–
Enable horizontal and vertical scaler unit.	DISPC_WB_ATTRIBUTES[6:5] RESIZEENABLE	0x–

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Table 10-76. DISPC Configure the WB Scaler Unit for Cb and Cr Components

Step	Register/Bit Field/Programming Model	Value
Configure horizontal scaling		
Set the horizontal resizing ratio for Cb and Cr components.	DISPC_WB_FIR2[12:0] FIRHINC	0x–
Set the horizontal FIR coefficients for Cb and Cr components.	DISPC_WB_FIR_COEF_H2_i[31:24][23:16][15:8][7:0] FIRHC3, FIRHC2, FIRHC1, FIRHC0	0x–
	DISPC_WB_FIR_COEF_HV2_i[7:0] FIRHC4	0x–
Set the horizontal accumulators value for Cb and Cr components.	DISPC_WB_ACCU2_j[10:0] HORIZONTALACCU	0x–
Configure vertical scaling		
Set the vertical resizing ratio for Cb and Cr components.	DISPC_WB_FIR2[28:16] FIRVINC	0x–
Set the vertical FIR coefficients for Cb and Cr components.	DISPC_WB_FIR_COEF_HV2_i[31:24][23:16][15:8] FIRVC2, FIRVC1, FIRVC0	0x–
	Only for 5-taps vertical: DISPC_WB_FIR_COEF_V2_i[15:8][7:0] FIRVC22, FIRVC00	0x–
Set the vertical accumulators value for Cb and Cr components.	DISPC_WB_ACCU2_j[26:16] VERTICALACCU	0x–

10.2.5.1.2.4.4 DISPC Subsequence – Configure the WB Color Space Conversion Unit

This subsequence describes the steps to configure the WB color space conversion unit (see Table 10-77).

Table 10-77. DISPC Configure the WB Color Space Conversion Unit

Step	Register/Bit Field/Programming Model	Value
Select the range of the color space conversion.	DISPC_WB_ATTRIBUTES[11] FULLRANGE	0x–
Set the RCr and RY coefficients.	DISPC_WB_CONV_COEF0[26:16][10:0] YG, YR	0x–
Set the GY and RCb coefficients	DISPC_WB_CONV_COEF1[26:16][10:0] CRR, YB	0x–
Set the GCb and GCr coefficients.	DISPC_WB_CONV_COEF2[26:16][10:0] CRB, CRG	0x–
Set the BCr and BY coefficients.	DISPC_WB_CONV_COEF3[26:16][10:0] CBG, CBR	0x–
Set the BCb coefficient.	DISPC_WB_CONV_COEF4[10:0] CBB	0x–
Enable color space conversion.	DISPC_WB_ATTRIBUTES[9] COLORCONVENABLE	0x1

10.2.5.1.2.5 DISPC LCD Output Configuration

10.2.5.1.2.5.1 DISPC Main Sequence – Configure the LCD Output

This procedure details the LCD output configuration (see Table 10-78).

Table 10-78. DISPC Configure the LCD Output

Step	Register/Bit Field/Programming Model
Configure the LCD overlay manager.	See Table 10-79.
Configure the gamma table for gamma correction.	See Section 10.2.5.1.2.5.3.
Configure the CPR.	See Table 10-83.
Configure the LCD panel timings and parameters.	See Table 10-84.
Validate the LCD output configuration according.	DISPC_CONTROL1[5] GOLCD
	DISPC_CONTROL2[5] GOLCD
Enable LCD output.	DISPC_CONTROL1[0] LCDENABLE
	DISPC_CONTROL2[0] LCDENABLE

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10.2.5.1.2.5.2 DISPC Subsequence – Configure the Overlay Manager

This subsequence describes the overlay manager settings and transparency color key configuration (see Table 10-79).

Table 10-79. DISPC Configure the LCD Overlay Manager

Step	Register/Bit Field/Programming Model	Value
Set the LCD panel background color.	DISPC_DEFAULT_COLORo[23:0] DEFAULTCOLOR	0x–
Enable/disable overlay optimization.	DISPC_CONTROLo[12] OVERLAYOPTIMIZATION	0x–
Enable the alpha blender(1).	DISPC_CONFIG1[18] LCDALPHABLENDERENABLE	0x1
Configure the transparency color key		
Set source or destination transparency color key mode.	DISPC_CONFIGo[11] TCKLCDSELECTION	0x–
Set the transparency color value.	DISPC_TRANS_COLORo[23:0] TRANSCOLORKEY	0x–
Enable transparency color key mode.	DISPC_CONFIGo[10] TCKLCDENABLE	0x–

(1) Backward compatibility with OMAP34xx available only for LCD1

10.2.5.1.2.5.3 DISPC Subsequence – Configure the Gamma Table for Gamma Correction

This subsequence describes the settings for configuring the gamma correction for LCD1, LCD2, and LCD3 (see Table 10-80 through Table 10-82, respectively).

NOTE:

- Software must ensure there is no visible effect when modifying the table because it is not under hardware control. The synchronization done using the DMA engine inside the DISPC to load the table when it is not used to display the picture on the screen is not present for this mode.
- If the GFX pipeline is in BITMAP pixel format, gamma corrections are not available for LCD1.

Table 10-80. DISPC Configure the Gamma Table for LCD1

Step	Register/Bit Field/Programming Model	Value
Initialize all entries for the gamma table by setting the table index and the RGB values associated to this index.	DISPC_GAMMA_TABLE0[31:24][23:16][15:8][7:0], INDEX, VALUE_R, VALUE_G, VALUE_B	0x–
Set look up table as gamma table.	DISPC_CONFIG1[3] PALETTEGAMMATABLE	0x1
Select the load mode of the gamma look-up table.	DISPC_CONFIG1[2:1] LOADMODE	0x–

Table 10-81. DISPC Configure the Gamma Table for LCD2

Step	Register/Bit Field/Programming Model	Value
Enable Gamma table for LCD2 and TV.	DISPC_CONFIG2[9] GAMATABLEENABLE	0x1
Initialize all entries for the gamma table by setting the table index and the RGB values associated to this index.	DISPC_GAMMA_TABLE2[31:24][23:16][15:8][7:0], INDEX, VALUE_R, VALUE_G, VALUE_B	0x–

Table 10-82. DISPC Configure the Gamma Table for LCD3

Step	Register/Bit Field/Programming Model	Value
Enable Gamma table for LCD3 and TV.	DISPC_CONFIG3[9] GAMATABLEENABLE	0x1
Initialize all entries for the gamma table by setting the table index and the RGB values associated to this index.	DISPC_GAMMA_TABLE3[31:24][23:16][15:8][7:0], INDEX, VALUE_R, VALUE_G, VALUE_B	0x–

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10.2.5.1.2.5.4 DISPC Subsequence – Configure the Color Phase Rotation

Table 10-83 describes the settings for the CPR unit (see Table 10-83).

Table 10-83. DISPC Configure the Color Phase Rotation

Step	Register/Bit Field/Programming Model	Value
Set the Red coefficients.	DISPC_CPRo_COEF_R [31:22][20:11][9:0] RR, RG, RB	0x–
Set the Green coefficients	DISPC_CPRo_COEF_G [31:22][20:11][9:0] GR, GG, GB	0x–
Set the Blue coefficients.	DISPC_CPRo_COEF_B [31:22][20:11][9:0] BR, BG, BB	0x–
Disable the CPR unit in RGB to YUV conversion.	DISPC_CONFIGo[24] COLORCONVENABLE	0x0
Enable the CPR unit.	DISPC_CONFIGo[15] CPR	0x1

10.2.5.1.2.5.5 DISPC Subsequence – Configure the LCD Panel Timings and Parameters

This subsequence describes the setting for horizontal and vertical synchronization and signal polarity (see Table 10-84).

Table 10-84. DISPC Configure the LCD Panel Timings and Parameters

Step	Register/Bit Field/Programming Model	Value
Configure spatial/temporal dithering		
Select spatial/temporal number of frames.	DISPC_CONTROLo[31:30] SPATIALTEMPORALDITHERINGFRAMES	0x–
Enable spatial/temporal dithering.	DISPC_CONTROLo[7] STDITHERENABLE	0x–
Configure AC-bias		
Configure the VSYNC, HSYNC and AC bias polarity.	DISPC_POL_FREQo	0x–
Configure the gating of AC bias polarity.	DISPC_CONFIGo[8] ACBIASGATED	0x–
Configure the AC bias polarity.	DISPC_POL_FREQo[15] IEO	0x–
Set the AC bias frequency.	DISPC_POL_FREQo[7:0] ACB	0x–
Set the number of AC bias transitions per interrupt.	DISPC_POL_FREQo[11:8] ACBI	0x–
Configure the pixel clock		
Set the DISPC logic clock divisor.	DISPC_DIVISORo[23:16] LCD	0x–
Set the pixel clock divisor.	DISPC_DIVISORo[7:0] PCD	0x–
Configure the gating of pixel clock.	DISPC_CONFIGo[5] PIXELCLOCKGATED	0x–
Configure the data		
Set the pixel clock edge to drive data output.	DISPC_POL_FREQo[14] IPC	0x–
Configure the gating of data output.	DISPC_CONFIGo[4] PIXELDATAGATED	0x–
Set the data output mode.	DISPC_CONFIGo[22] OUTPUTMODEENABLE	0x–
Configure the panel parameters		
Set the vertical TV size.	DISPC_SIZE_LCDo[27:16] LPP	0x–
Set the horizontal TV size.	DISPC_SIZE_LCDo[11:0] PPL	0x–
Set the panel type.	DISPC_CONTROLo[3] STNTFT	0x–
Configure the refresh rate and horizontal and vertical parameters		
Set the vertical synchronization timing.	DISPC_TIMING_Vo[31:20][19:8][7:0], VBP, VFP, VSW	0x–
Configure the VSYNC polarity.	DISPC_POL_FREQo[12] IVS	0x–
Configure the gating of VSYNC.	DISPC_CONFIGo[7] VSYNCGATED	0x–
Set the horizontal synchronization timing.	DISPC_TIMING_Ho[31:20][19:8][7:0], HBP, HFP, HSW	0x–
Configure the HSYNC polarity.	DISPC_POL_FREQo[13] IHS	0x–
Configure the gating of HSYNC.	DISPC_CONFIGo[6] HSYNCGATED	0x–
Set the opposition of HSYNC and VSYNC driving.	DISPC_POL_FREQo[17] ONOFF	0x–

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Table 10-84. DISPC Configure the LCD Panel Timings and Parameters (continued)

Step	Register/Bit Field/Programming Model	Value
If DISPC_POL_FREQo[17] = 1, set the pixel clock edge to drive HSYNC and VSYNC.	DISPC_POL_FREQo[16] RF	0x–
Set the alignment of HSYNC and VSYNC.	DISPC_POL_FREQo[18] ALIGN	0x–

10.2.5.1.2.6 DISPC TV Output Configuration

10.2.5.1.2.6.1 DISPC Main Sequence – Configure the TV Output

This procedure describes the TV output configuration (see Table 10-85).

Table 10-85. DISPC Configure the TV Output

Step	Register/Bit Field/Programming Model
Configure the TV overlay manager.	See Table 10-86.
Configure the gamma table for gamma correction.	See Table 10-87.
Configure the TV panel timings and parameters.	See Table 10-88.
Validate the TV output configuration accordingly.	DISPC_CONTROL1[6] GOTV
Enable the TV output.	DISPC_CONTROL1[1] TVENABLE

10.2.5.1.2.6.1.1 DISPC Subsequence – Configure the TV Overlay Manager

This subsequence describes the overlay manager settings and transparency color key configuration (see Table 10-86).

Table 10-86. DISPC Configure the TV Overlay Manager

Step	Register/Bit Field/Programming Model	Value
Set the TV panel background color.	DISPC_DEFAULT_COLOR1[23:0] DEFAULTCOLOR	0x–
Enable/disable overlay optimization.	DISPC_CONTROL2[13] TVOVERLAYOPTIMIZATION	0x–
Enable the alpha blender(1).	DISPC_CONFIG1[19] TVALPHABLENDERENABLE	0x1
Configure the transparency color key		
Set source or destination transparency color key mode.	DISPC_CONFIG1[13] TCKTVSELECTION	0x–
Set the transparency color value.	DISPC_TRANS_COLOR1[23:0] TRANSCOLORKEY	0x–
Enable transparency color key mode.	DISPC_CONFIG1[10] TCKTVENABLE	0x–

(1) Backward compatibility with OMAP34xx

10.2.5.1.2.6.1.2 DISPC Subsequence – Configure the Gamma Table for Gamma Correction

This subsequence describes the steps to configure the gamma table for gamma correction (see Table 10-87).

NOTE: Software must ensure there is no visible effect when modifying the table because it is not under hardware control. The synchronization done using the DMA engine inside the DISPC to load the table when it is not used for displaying the picture on the screen is not present for this mode.

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Table 10-87. DISPC Configure the Gamma Table for TV Output

Step	Register/Bit Field/Programming Model	Value
Enable Gamma table for LCD2 and TV.	DISPC_CONFIG1[9] GAMATABLEENABLE	0x1
Initialize all entries for the gamma table by setting the table index and the RGB values. For more information, see Section 10.2.4.13.2, *Gamma Correction Unit*.	DISPC_GAMMA_TABLE2[31][29:20][19:10][9:0] INDEX, VALUE_R, VALUE_G, VALUE_B	0x–

10.2.5.1.2.6.1.3 DISPC Subsequence – Configure the TV Panel Timings and Parameters

This subsequence describes the settings for horizontal and vertical synchronization and signal polarity (see Table 10-88).

Table 10-88. DISPC Configure the TV Panel Timings and Parameters

Step	Register/Bit Field/Programming Model	Value
Set the hold time for TV data outputs.	DISPC_CONFIG1[19:17]	0x–
Set the vertical TV size.	DISPC_SIZE_TV[27:16] LPP	See Table 10-53 for HD standards.
Set the horizontal TV size.	DISPC_SIZE_TV[11:0] PPL	

10.2.6 DISPC Use Cases and Tips

10.2.6.1 DISPC Hardware Cursor

The video layer or graphics layer can be used to display the hardware cursor. The encoded pixel data for the cursor image are in one of the following formats if the source transparency color key is used:

- xRGB12-4444
- ARGB16-4444
- RGBx12-4444
- RGBA16-4444
- ARGB16-1555
- RGB16-565
- RGB24-888
- xRGB24-88888
- RGBA32-8888
- BGRA32-8888
- ARGB32-8888

Otherwise, any pixel format can be used for the cursor image, considering the limitation in terms of pixels supported by the pipeline used to display the cursor image. To display a nonrectangle cursor, the transparency color key or alpha blending (pixel alpha blending) can be used (see Section 10.2.4.12.1.3, *DISPC Transparency Color Keys*). Global alpha blending can be used in addition to the transparency source color key to create a fading effect when the cursor (with a nonrectangle shape) appears and disappears on the screen. The image of the cursor can be stored entirely inside the DMA buffer to use the self-refresh mode (see Section 10.2.4.6.8.2, *DISPC DMA Ultralow-Power Mode*). In that case, the image is loaded once and then displayed without accessing the system memory for loading the image for each frame. This saves bandwidth on interconnect and memory.

10.2.7 DISPC Register Manual

10.2.7.1 DISPC Instance Summary

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Table 10-89. DISPC Instance Summary

Module Name	L3_MAIN Base Address	Size
DISPC	0x5800 1000	4 KiB

10.2.7.2 DISPC Logical Register Mapping

Table 10-90. DISPC_VIDp_BA_j Logical Register Mapping

Hardware Register	Description
DISPC_VID1_BA_j	Base address of video pipeline 1
DISPC_VID2_BA_j	Base address of video pipeline 2
DISPC_VID3_BA_j	Base address of video pipeline 3

Table 10-91. DISPC_VIDp_BA_UV_j Logical Register Mapping

Hardware Register	Description
DISPC_VID1_BA_UV_j	Base address of UV components for video pipeline 1
DISPC_VID2_BA_UV_j	Base address of UV components for video pipeline 2
DISPC_VID3_BA_UV_j	Base address of UV components for video pipeline 3

Table 10-92. DISPC_VIDp_POSITION Logical Register Mapping

Hardware Register	Description
DISPC_VID1_POSITION	Position of the video window 1
DISPC_VID2_POSITION	Position of the video window 2
DISPC_VID3_POSITION	Position of the video window 3

Table 10-93. DISPC_VIDp_SIZE Logical Register Mapping

Hardware Register	Description
DISPC_VID1_SIZE	Size of the video window 1
DISPC_VID2_SIZE	Size of the video window 2
DISPC_VID3_SIZE	Size of the video window 3

Table 10-94. DISPC_VIDp_ATTRIBUTES Logical Register Mapping

Hardware Register	Description
DISPC_VID1_ATTRIBUTES	Configuration of the video pipeline 1
DISPC_VID2_ATTRIBUTES	Configuration of the video pipeline 2
DISPC_VID3_ATTRIBUTES	Configuration of the video pipeline 3

Table 10-95. DISPC_VIDp_ATTRIBUTES2 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_ATTRIBUTES2	Configuration of the video pipeline 1
DISPC_VID2_ATTRIBUTES2	Configuration of the video pipeline 2
DISPC_VID3_ATTRIBUTES2	Configuration of the video pipeline 3

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Table 10-96. DISPC_VIDp_BUF_THRESHOLD Logical Register Mapping

Hardware Register	Description
DISPC_VID1_BUF_THRESHOLD	Configuration of the buffer for the video pipeline 1
DISPC_VID2_BUF_THRESHOLD	Configuration of the buffer for the video pipeline 2
DISPC_VID3_BUF_THRESHOLD	Configuration of the buffer for the video pipeline 3

Table 10-97. DISPC_VIDp_ROW_INC Logical Register Mapping

Hardware Register	Description
DISPC_VID1_ROW_INC	Configuration of the row increment for the video pipeline 1
DISPC_VID2_ROW_INC	Configuration of the row increment for the video pipeline 2
DISPC_VID3_ROW_INC	Configuration of the row increment for the video pipeline 3

Table 10-98. DISPC_VIDp_PIXEL_INC Logical Register Mapping

Hardware Register	Description
DISPC_VID1_PIXEL_INC	Configuration of the pixel increment for the video pipeline 1
DISPC_VID2_PIXEL_INC	Configuration of the pixel increment for the video pipeline 2
DISPC_VID3_PIXEL_INC	Configuration of the pixel increment for the video pipeline 3

Table 10-99. DISPC_VIDp_FIR Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR	Configuration of the scaler for the video pipeline 1
DISPC_VID2_FIR	Configuration of the scaler for the video pipeline 2
DISPC_VID3_FIR	Configuration of the scaler for the video pipeline 3

Table 10-100. DISPC_VIDp_PICTURE_SIZE Logical Register Mapping

Hardware Register	Description
DISPC_VID1_PICTURE_SIZE	Size of the video window 1 before processing
DISPC_VID2_PICTURE_SIZE	Size of the video window 2 before processing
DISPC_VID3_PICTURE_SIZE	Size of the video window 3 before processing

Table 10-101. DISPC_VIDp_ACCU_j Logical Register Mapping

Hardware Register	Description
DISPC_VID1_ACCU_j	Configuration of the accumulator for the video pipeline 1
DISPC_VID2_ACCU_j	Configuration of the accumulator for the video pipeline 2
DISPC_VID2_ACCU_j	Configuration of the accumulator for the video pipeline 3

Table 10-102. DISPC_VIDp_FIR_COEF_H_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_H_i	Configuration of the horizontal scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_H_i	Configuration of the horizontal scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_H_i	Configuration of the horizontal scaling coefficients or the video pipeline 3

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Table 10-103. DISPC_VIDp_FIR_COEF_HV_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_HV_i	Configuration of the horizontal scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_HV_i	Configuration of the horizontal scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_HV_i	Configuration of the horizontal scaling coefficients for the video pipeline 3

Table 10-104. DISPC_VIDp_FIR_COEF_V_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_V_i	Configuration of the vertical scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_V_i	Configuration of the vertical scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_V_i	Configuration of the vertical scaling coefficients for the video pipeline 3

Table 10-105. DISPC_VIDp_FIR_COEF_H2_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_H2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_H2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_H2_i	Configuration of the horizontal Cb and Cr scaling coefficients or the video pipeline 3

Table 10-106. DISPC_VIDp_FIR_COEF_HV2_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_HV2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_HV2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_HV2_i	Configuration of the horizontal Cb and Cr scaling coefficients for the video pipeline 3

Table 10-107. DISPC_VIDp_FIR_COEF_V2_i Logical Register Mapping

Hardware Register	Description
DISPC_VID1_FIR_COEF_V2_i	Configuration of the vertical Cb and Cr scaling coefficients for the video pipeline 1
DISPC_VID2_FIR_COEF_V2_i	Configuration of the vertical Cb and Cr scaling coefficients for the video pipeline 2
DISPC_VID3_FIR_COEF_V2_i	Configuration of the vertical Cb and Cr scaling coefficients for the video pipeline 3

Table 10-108. DISPC_VIDp_CONV_COEF0 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF0	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF0	Configuration of the Color Space Conversion coefficient for the video pipeline 2

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Table 10-108. DISPC_VIDp_CONV_COEF0 Logical Register Mapping (continued)

Hardware Register	Description
DISPC_VID3_CONV_COEF0	Configuration of the Color Space Conversion coefficient for the video pipeline 3

Table 10-109. DISPC_VIDp_CONV_COEF1 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF1	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF1	Configuration of the Color Space Conversion coefficient for the video pipeline 2
DISPC_VID3_CONV_COEF1	Configuration of the Color Space Conversion coefficient for the video pipeline 3

Table 10-110. DISPC_VIDp_CONV_COEF2 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF2	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF2	Configuration of the Color Space Conversion coefficient for the video pipeline 2
DISPC_VID3_CONV_COEF2	Configuration of the Color Space Conversion coefficient for the video pipeline 3

Table 10-111. DISPC_VIDp_CONV_COEF3 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF3	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF3	Configuration of the Color Space Conversion coefficient for the video pipeline 2
DISPC_VID3_CONV_COEF3	Configuration of the Color Space Conversion coefficient for the video pipeline 3

Table 10-112. DISPC_VIDp_CONV_COEF4 Logical Register Mapping

Hardware Register	Description
DISPC_VID1_CONV_COEF4	Configuration of the Color Space Conversion coefficients for the video pipeline 1
DISPC_VID2_CONV_COEF4	Configuration of the Color Space Conversion coefficient for the video pipeline 2
DISPC_VID3_CONV_COEF4	Configuration of the Color Space Conversion coefficient for the video pipeline 3

Table 10-113. DISPC_CONTROLo Logical Register Mapping

Hardware Register	Description
DISPC_CONTROL1	Configuration control of the LCD1 and TV.
DISPC_CONTROL2	Configuration control of the LCD2.
DISPC_CONTROL3	Configuration control of the LCD3.

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Table 10-114. DISPC_CONFIGo Logical Register Mapping

Hardware Register	Description
DISPC_CONFIG1	Configuration of the LCD1 and TV.
DISPC_CONFIG2	Configuration of the LCD2.
DISPC_CONFIG3	Configuration of the LCD3.

Table 10-115. DISPC_DEFAULT_COLORo Logical Register Mapping

Hardware Register	Description
DISPC_DEFAULT_COLOR0	Configuration of the background color for LCD1.
DISPC_DEFAULT_COLOR1	Configuration of the background color for TV.
DISPC_DEFAULT_COLOR2	Configuration of the background color for LCD2.
DISPC_DEFAULT_COLOR3	Configuration of the background color for LCD3.

Table 10-116. DISPC_TRANS_COLORo Logical Register Mapping

Hardware Register	Description
DISPC_TRANS_COLOR0	Configuration of the transparency color key for LCD1.
DISPC_TRANS_COLOR1	Configuration of the transparency color key for TV.
DISPC_TRANS_COLOR2	Configuration of the transparency color key for LCD2.
DISPC_DEFAULT_COLOR3	Configuration of the background color for LCD3.

Table 10-117. DISPC_GAMMA_TABLEo Logical Register Mapping

Hardware Register	Description
DISPC_GAMMA_TABLE0	Configuration of the palette table for GFX or the gamma table for LCD1.
DISPC_GAMMA_TABLE1	Configuration of the gamma table for LCD2.
DISPC_GAMMA_TABLE2	Configuration of the gamma table for TV output.
DISPC_GAMMA_TABLE3	Configuration of the gamma table for LCD3.

Table 10-118. DISPC_TIMING_Ho Logical Register Mapping

Hardware Register	Description
DISPC_TIMING_H1	Configuration of the horizontal timing for LCD1.
DISPC_TIMING_H2	Configuration of the horizontal timing for LCD2.
DISPC_TIMING_H3	Configuration of the horizontal timing for LCD3.

Table 10-119. DISPC_TIMING_Vo Logical Register Mapping

Hardware Register	Description
DISPC_TIMING_V1	Configuration of the vertical timing for LCD1.
DISPC_TIMING_V2	Configuration of the vertical timing for LCD2.
DISPC_TIMING_V3	Configuration of the vertical timing for LCD3.

Table 10-120. DISPC_POL_FREQo Logical Register Mapping

Hardware Register	Description
DISPC_POL_FREQ1	Configuration of the output signals for LCD1.
DISPC_POL_FREQ2	Configuration of the output signals for LCD2.
DISPC_POL_FREQ3	Configuration of the output signals for LCD3.

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Table 10-121. DISPC_DIVISORo Logical Register Mapping

Hardware Register	Description
DISPC_DIVISOR1	Configuration of the divisors for LCD1.
DISPC_DIVISOR2	Configuration of the divisors for LCD2.
DISPC_DIVISOR3	Configuration of the divisors for LCD3.

Table 10-122. DISPC_SIZE_LCDo Logical Register Mapping

Hardware Register	Description
DISPC_SIZE_LCD1	Configuration of the divisors for LCD1.
DISPC_SIZE_LCD2	Configuration of the divisors for LCD2.
DISPC_SIZE_LCD3	Configuration of the divisors for LCD3.

Table 10-123. DISPC_SIZE Logical Register Mapping

Hardware Register	Description
DISPC_SIZE_LCD1	Configuration of the LCD size on LCD1.
DISPC_SIZE_LCD2	Configuration of the LCD size on LCD2.
DISPC_SIZE_LCD3	Configuration of the LCD size on LCD3.

Table 10-124. DISPC_DATAo_CYCLE1 Logical Register Mapping

Hardware Register	Description
DISPC_DATA1_CYCLE1	Configuration of the output data format for first cycle on LCD1.
DISPC_DATA2_CYCLE1	Configuration of the output data format for first cycle on LCD2.
DISPC_DATA3_CYCLE1	Configuration of the output data format for first cycle on LCD3.

Table 10-125. DISPC_DATAo_CYCLE2 Logical Register Mapping

Hardware Register	Description
DISPC_DATA1_CYCLE2	Configuration of the output data format for second cycle on LCD1.
DISPC_DATA2_CYCLE2	Configuration of the output data format for second cycle on LCD2.
DISPC_DATA3_CYCLE2	Configuration of the output data format forsecond cycle on LCD3.

Table 10-126. DISPC_DATAo_CYCLE3 Logical Register Mapping

Hardware Register	Description
DISPC_DATA1_CYCLE3	Configuration of the output data format for third cycle on LCD1.
DISPC_DATA2_CYCLE3	Configuration of the output data format for third cycle on LCD2.
DISPC_DATA3_CYCLE3	Configuration of the output data format for third cycle on LCD3.

Table 10-127. DISPC_CPRo_COEF_R Logical Register Mapping

Hardware Register	Description
DISPC_CPR1_COEF_R	Configuration of the CPR matrix coefficients for the red component on LCD1.
DISPC_CPR2_COEF_R	Configuration of the CPR matrix coefficients for the red component on LCD2.
DISPC_CPR3_COEF_R	Configuration of the CPR matrix coefficients for the red component on LCD3

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Table 10-128. DISPC_CPRo_COEF_G Logical Register Mapping

Hardware Register	Description
DISPC_CPR1_COEF_G	Configuration of the CPR matrix coefficients for the green component on LCD1.
DISPC_CPR2_COEF_G	Configuration of the CPR matrix coefficients for the green component on LCD2.
DISPC_CPR3_COEF_G	Configuration of the CPR matrix coefficients for the green component on LCD3.

Table 10-129. DISPC_CPRo_COEF_B Logical Register Mapping

Hardware Register	Description
DISPC_CPR1_COEF_B	Configuration of the CPR matrix coefficients for the blue component on LCD1.
DISPC_CPR2_COEF_B	Configuration of the CPR matrix coefficients for the blue component on LCD2.
DISPC_CPR3_COEF_B	Configuration of the CPR matrix coefficients for the blue component on LCD3.

10.2.7.3 DISPC Registers

10.2.7.3.1 DISPC Register Summary

Table 10-130. DISPC Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address
DISPC_REVISION	R	32	0x0000 0000	0x5800 1000
DISPC_SYSCONFIG	RW	32	0x0000 0010	0x5800 1010
DISPC_SYSSTATUS	R	32	0x0000 0014	0x5800 1014
DISPC_IRQSTATUS	RW	32	0x0000 0018	0x5800 1018
DISPC_IRQENABLE	RW	32	0x0000 001C	0x5800 101C
DISPC_CONTROL1	RW	32	0x0000 0040	0x5800 1040
DISPC_CONFIG1	RW	32	0x0000 0044	0x5800 1044
RESERVED	R	32	0x0000 0048	0x5800 1048
DISPC_DEFAULT_COLOR0	RW	32	0x0000 004C	0x5800 104C
DISPC_DEFAULT_COLOR1	RW	32	0x0000 0050	0x5800 1050
DISPC_TRANS_COLOR0	RW	32	0x0000 0054	0x5800 1054
DISPC_TRANS_COLOR1	RW	32	0x0000 0058	0x5800 1058
DISPC_LINE_STATUS	R	32	0x0000 005C	0x5800 105C
DISPC_LINE_NUMBER	RW	32	0x0000 0060	0x5800 1060
DISPC_TIMING_H1	RW	32	0x0000 0064	0x5800 1064
DISPC_TIMING_V1	RW	32	0x0000 0068	0x5800 1068
DISPC_POL_FREQ1	RW	32	0x0000 006C	0x5800 106C
DISPC_DIVISOR1	RW	32	0x0000 0070	0x5800 1070
DISPC_GLOBAL_ALPHA	RW	32	0x0000 0074	0x5800 1074
DISPC_SIZE_TV	RW	32	0x0000 0078	0x5800 1078
DISPC_SIZE_LCD1	RW	32	0x0000 007C	0x5800 107C
DISPC_GFX_BA_j [(1)]	RW	32	0x0000 0080 + (0x4 * j)	0x5800 1080 + (0x4 * j)
DISPC_GFX_POSITION	RW	32	0x0000 0088	0x5800 1088
DISPC_GFX_SIZE	RW	32	0x0000 008C	0x5800 108C

(1) j = 0 to 1

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Table 10-130. DISPC Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address
DISPC_GFX_ATTRIBUTES	RW	32	0x0000 00A0	0x5800 10A0
DISPC_GFX_BUF_THRESHOLD	RW	32	0x0000 00A4	0x5800 10A4
DISPC_GFX_BUF_SIZE_STATUS	R	32	0x0000 00A8	0x5800 10A8
DISPC_GFX_ROW_INC	RW	32	0x0000 00AC	0x5800 10AC
DISPC_GFX_PIXEL_INC	RW	32	0x0000 00B0	0x5800 10B0
RESERVED	R	32	0x0000 00B4	0x5800 10B4
DISPC_GFX_TABLE_BA	RW	32	0x0000 00B8	0x5800 10B8
DISPC_VID1_BA_j [1]	RW	32	0x0000 00BC + (0x4 * j)	0x5800 10BC + (0x4 * j)
DISPC_VID1_POSITION	RW	32	0x0000 00C4	0x5800 10C4
DISPC_VID1_SIZE	RW	32	0x0000 00C8	0x5800 10C8
DISPC_VID1_ATTRIBUTES	RW	32	0x0000 00CC	0x5800 10CC
DISPC_VID1_BUF_THRESHOLD	RW	32	0x0000 00D0	0x5800 10D0
DISPC_VID1_BUF_SIZE_STATUS	R	32	0x0000 00D4	0x5800 10D4
DISPC_VID1_ROW_INC	RW	32	0x0000 00D8	0x5800 10D8
DISPC_VID1_PIXEL_INC	RW	32	0x0000 00DC	0x5800 10DC
DISPC_VID1_FIR	RW	32	0x0000 00E0	0x5800 10E0
DISPC_VID1_PICTURE_SIZE	RW	32	0x0000 00E4	0x5800 10E4
DISPC_VID1_ACCU_j [2]	RW	32	0x0000 00E8 + (0x4 * j)	0x5800 10E8 + (0x4 * j)
DISPC_VID1_FIR_COEF_H_i [3]	RW	32	0x0000 00F0 + (0x8 * i)	0x5800 10F0 + (0x8 * i)
DISPC_VID1_FIR_COEF_HV_i [3]	RW	32	0x0000 00F4 + (0x8 * i)	0x5800 10F4 + (0x8 * i)
DISPC_VID1_CONV_COEF0	RW	32	0x0000 0130	0x5800 1130
DISPC_VID1_CONV_COEF1	RW	32	0x0000 0134	0x5800 1134
DISPC_VID1_CONV_COEF2	RW	32	0x0000 0138	0x5800 1138
DISPC_VID1_CONV_COEF3	RW	32	0x0000 013C	0x5800 113C
DISPC_VID1_CONV_COEF4	RW	32	0x0000 0140	0x5800 1140
DISPC_VID2_BA_j [2]	RW	32	0x0000 014C + (0x4 * j)	0x5800 114C + (0x4 * j)
DISPC_VID2_POSITION	RW	32	0x0000 0154	0x5800 1154
DISPC_VID2_SIZE	RW	32	0x0000 0158	0x5800 1158
DISPC_VID2_ATTRIBUTES	RW	32	0x0000 015C	0x5800 115C
DISPC_VID2_BUF_THRESHOLD	RW	32	0x0000 0160	0x5800 1160
DISPC_VID2_BUF_SIZE_STATUS	R	32	0x0000 0164	0x5800 1164
DISPC_VID2_ROW_INC	RW	32	0x0000 0168	0x5800 1168
DISPC_VID2_PIXEL_INC	RW	32	0x0000 016C	0x5800 116C
DISPC_VID2_FIR	RW	32	0x0000 0170	0x5800 1170
DISPC_VID2_PICTURE_SIZE	RW	32	0x0000 0174	0x5800 1174
DISPC_VID2_ACCU_j [2]	RW	32	0x0000 0178 + (0x4 * j)	0x5800 1178 + (0x4 * j)
DISPC_VID2_FIR_COEF_H_i [3]	RW	32	0x0000 0180 + (0x8 * i)	0x5800 1180 + (0x8 * i)
DISPC_VID2_FIR_COEF_HV_i [3]	RW	32	0x0000 0184 + (0x8 * i)	0x5800 1184 + (0x8 * i)
DISPC_VID2_CONV_COEF0	RW	32	0x0000 01C0	0x5800 11C0
DISPC_VID2_CONV_COEF1	RW	32	0x0000 01C4	0x5800 11C4
DISPC_VID2_CONV_COEF2	RW	32	0x0000 01C8	0x5800 11C8
DISPC_VID2_CONV_COEF3	RW	32	0x0000 01CC	0x5800 11CC
DISPC_VID2_CONV_COEF4	RW	32	0x0000 01D0	0x5800 11D0
DISPC_DATA1_CYCLE1	RW	32	0x0000 01D4	0x5800 11D4

[2] j = 0 to 1
[3] i = 0 to 7

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Table 10-130. DISPC Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address
DISPC_DATA1_CYCLE2	RW	32	0x0000 01D8	0x5800 11D8
DISPC_DATA1_CYCLE3	RW	32	0x0000 01DC	0x5800 11DC
DISPC_VID1_FIR_COEF_V_i [3]	RW	32	0x0000 01E0 + (0x4 * i)	0x5800 11E0 + (0x4 * i)
DISPC_VID2_FIR_COEF_V_i [3]	RW	32	0x0000 0200 + (0x4 * i)	0x5800 1200 + (0x4 * i)
DISPC_CPR1_COEF_R	RW	32	0x0000 0220	0x5800 1220
DISPC_CPR1_COEF_G	RW	32	0x0000 0224	0x5800 1224
DISPC_CPR1_COEF_B	RW	32	0x0000 0228	0x5800 1228
DISPC_GFX_PRELOAD	RW	32	0x0000 022C	0x5800 122C
DISPC_VID1_PRELOAD	RW	32	0x0000 0230	0x5800 1230
DISPC_VID2_PRELOAD	RW	32	0x0000 0234	0x5800 1234
DISPC_CONTROL2	RW	32	0x0000 0238	0x5800 1238
DISPC_GFX_POSITION2	RW	32	0x0000 0240	0x5800 1240
DISPC_VID1_POSITION2	RW	32	0x0000 0244	0x5800 1244
DISPC_VID2_POSITION2	RW	32	0x0000 0248	0x5800 1248
DISPC_VID3_POSITION2	RW	32	0x0000 024C	0x5800 124C
DISPC_VID3_ACCU_j [2]	RW	32	0x0000 0300 + (0x4 * j)	0x5800 1300 + (0x4 * j)
DISPC_VID3_BA_j [4]	RW	32	0x0000 0308 + (0x4 * j)	0x5800 1308 + (0x4 * j)
DISPC_VID3_FIR_COEF_H_i [5]	RW	32	0x0000 0310 + (0x8 * i)	0x5800 1310 + (0x8 * i)
DISPC_VID3_FIR_COEF_HV_i [5]	RW	32	0x0000 0314 + (0x8 * i)	0x5800 1314 + (0x8 * i)
DISPC_VID3_FIR_COEF_V_i [5]	RW	32	0x0000 0350 + (0x4 * i)	0x5800 1350 + (0x4 * i)
DISPC_VID3_ATTRIBUTES	RW	32	0x0000 0370	0x5800 1370
DISPC_VID3_CONV_COEF0	RW	32	0x0000 0374	0x5800 1374
DISPC_VID3_CONV_COEF1	RW	32	0x0000 0378	0x5800 1378
DISPC_VID3_CONV_COEF2	RW	32	0x0000 037C	0x5800 137C
DISPC_VID3_CONV_COEF3	RW	32	0x0000 0380	0x5800 1380
DISPC_VID3_CONV_COEF4	RW	32	0x0000 0384	0x5800 1384
DISPC_VID3_BUF_SIZE_STATUS	R	32	0x0000 0388	0x5800 1388
DISPC_VID3_BUF_THRESHOLD	RW	32	0x0000 038C	0x5800 138C
DISPC_VID3_FIR	RW	32	0x0000 0390	0x5800 1390
DISPC_VID3_PICTURE_SIZE	RW	32	0x0000 0394	0x5800 1394
DISPC_VID3_PIXEL_INC	RW	32	0x0000 0398	0x5800 1398
DISPC_VID3_POSITION	RW	32	0x0000 039C	0x5800 139C
DISPC_VID3_PRELOAD	RW	32	0x0000 03A0	0x5800 13A0
DISPC_VID3_ROW_INC	RW	32	0x0000 03A4	0x5800 13A4
DISPC_VID3_SIZE	RW	32	0x0000 03A8	0x5800 13A8
DISPC_DEFAULT_COLOR2	RW	32	0x0000 03AC	0x5800 13AC
DISPC_TRANS_COLOR2	RW	32	0x0000 03B0	0x5800 13B0
DISPC_CPR2_COEF_B	RW	32	0x0000 03B4	0x5800 13B4
DISPC_CPR2_COEF_G	RW	32	0x0000 03B8	0x5800 13B8
DISPC_CPR2_COEF_R	RW	32	0x0000 03BC	0x5800 13BC
DISPC_DATA2_CYCLE1	RW	32	0x0000 03C0	0x5800 13C0
DISPC_DATA2_CYCLE2	RW	32	0x0000 03C4	0x5800 13C4
DISPC_DATA2_CYCLE3	RW	32	0x0000 03C8	0x5800 13C8
DISPC_SIZE_LCD2	RW	32	0x0000 03CC	0x5800 13CC

(4) j = 0 to 1
(5) i = 0 to 7

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Table 10-130. DISPC Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address
DISPC_TIMING_H2	RW	32	0x0000 0400	0x5800 1400
DISPC_TIMING_V2	RW	32	0x0000 0404	0x5800 1404
DISPC_POL_FREQ2	RW	32	0x0000 0408	0x5800 1408
DISPC_DIVISOR2	RW	32	0x0000 040C	0x5800 140C
DISPC_WB_ACCU_j [4]	RW	32	0x0000 0500 + (0x4 * j)	0x5800 1500 + (0x4 * j)
DISPC_WB_BA_j [4]	RW	32	0x0000 0508 + (0x4 * j)	0x5800 1508 + (0x4 * j)
DISPC_WB_FIR_COEF_H_i [5]	RW	32	0x0000 0510 + (0x8 * i)	0x5800 1510 + (0x8 * i)
DISPC_WB_FIR_COEF_HV_i [5]	RW	32	0x0000 0514 + (0x8 * i)	0x5800 1514 + (0x8 * i)
DISPC_WB_FIR_COEF_V_i [5]	RW	32	0x0000 0550 + (0x4 * i)	0x5800 1550 + (0x4 * i)
DISPC_WB_ATTRIBUTES	RW	32	0x0000 0570	0x5800 1570
DISPC_WB_CONV_COEF0	RW	32	0x0000 0574	0x5800 1574
DISPC_WB_CONV_COEF1	RW	32	0x0000 0578	0x5800 1578
DISPC_WB_CONV_COEF2	RW	32	0x0000 057C	0x5800 157C
DISPC_WB_CONV_COEF3	RW	32	0x0000 0580	0x5800 1580
DISPC_WB_CONV_COEF4	RW	32	0x0000 0584	0x5800 1584
DISPC_WB_BUF_SIZE_STATUS	R	32	0x0000 0588	0x5800 1588
DISPC_WB_BUF_THRESHOLD	RW	32	0x0000 058C	0x5800 158C
DISPC_WB_FIR	RW	32	0x0000 0590	0x5800 1590
DISPC_WB_PICTURE_SIZE	RW	32	0x0000 0594	0x5800 1594
DISPC_WB_PIXEL_INC	RW	32	0x0000 0598	0x5800 1598
DISPC_WB_ROW_INC	RW	32	0x0000 05A4	0x5800 15A4
DISPC_WB_SIZE	RW	32	0x0000 05A8	0x5800 15A8
DISPC_VID1_BA_UV_j [6]	RW	32	0x0000 0600 + (0x4 * j)	0x5800 1600 + (0x4 * j)
DISPC_VID2_BA_UV_j [6]	RW	32	0x0000 0608 + (0x4 * j)	0x5800 1608 + (0x4 * j)
DISPC_VID3_BA_UV_j [6]	RW	32	0x0000 0610 + (0x4 * j)	0x5800 1610 + (0x4 * j)
DISPC_WB_BA_UV_j [6]	RW	32	0x0000 0618 + (0x4 * j)	0x5800 1618 + (0x4 * j)
DISPC_CONFIG2	RW	32	0x0000 0620	0x5800 1620
DISPC_VID1_ATTRIBUTES2	RW	32	0x0000 0624	0x5800 1624
DISPC_VID2_ATTRIBUTES2	RW	32	0x0000 0628	0x5800 1628
DISPC_VID3_ATTRIBUTES2	RW	32	0x0000 062C	0x5800 162C
DISPC_GAMMA_TABLE0	W	32	0x0000 0630	0x5800 1630
DISPC_GAMMA_TABLE1	W	32	0x0000 0634	0x5800 1634
DISPC_GAMMA_TABLE2	W	32	0x0000 0638	0x5800 1638
DISPC_VID1_FIR2	RW	32	0x0000 063C	0x5800 163C
DISPC_VID1_ACCU2_j [6]	RW	32	0x0000 0640 + (0x4 * j)	0x5800 1640 + (0x4 * j)
DISPC_VID1_FIR_COEF_H2_i [7]	RW	32	0x0000 0648 + (0x8 * i)	0x5800 1648 + (0x8 * i)
DISPC_VID1_FIR_COEF_HV2_i [7]	RW	32	0x0000 064C + (0x8 * i)	0x5800 164C + (0x8 * i)
DISPC_VID1_FIR_COEF_V2_i [7]	RW	32	0x0000 0688 + (0x4 * i)	0x5800 1688 + (0x4 * i)
DISPC_VID2_FIR2	RW	32	0x0000 06A8	0x5800 16A8
DISPC_VID2_ACCU2_j [6]	RW	32	0x0000 06AC + (0x4 * j)	0x5800 16AC + (0x4 * j)
DISPC_VID2_FIR_COEF_H2_i [7]	RW	32	0x0000 06B4 + (0x8 * i)	0x5800 16B4 + (0x8 * i)
DISPC_VID2_FIR_COEF_HV2_i [7]	RW	32	0x0000 06B8 + (0x8 * i)	0x5800 16B8 + (0x8 * i)
DISPC_VID2_FIR_COEF_V2_i [7]	RW	32	0x0000 06F4 + (0x4 * i)	0x5800 16F4 + (0x4 * i)
DISPC_VID3_FIR2	RW	32	0x0000 0724	0x5800 1724

[6] j = 0 to 1
[7] i = 0 to 7

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Table 10-130. DISPC Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address
DISPC_VID3_ACCU2_j [6]	RW	32	0x0000 0728 + (0x4 * j)	0x5800 1728 + (0x4 * j)
DISPC_VID3_FIR_COEF_H2_i [7]	RW	32	0x0000 0730 + (0x8 * i)	0x5800 1730 + (0x8 * i)
DISPC_VID3_FIR_COEF_HV2_i [7]	RW	32	0x0000 0734 + (0x8 * i)	0x5800 1734 + (0x8 * i)
DISPC_VID3_FIR_COEF_V2_i [7]	RW	32	0x0000 0770 + (0x4 * i)	0x5800 1770 + (0x4 * i)
DISPC_WB_FIR2	RW	32	0x0000 0790	0x5800 1790
DISPC_WB_ACCU2_j [6]	RW	32	0x0000 0794 + (0x4 * j)	0x5800 1794 + (0x4 * j)
DISPC_WB_FIR_COEF_H2_i [7]	RW	32	0x0000 07A0 + (0x8 * i)	0x5800 17A0 + (0x8 * i)
DISPC_WB_FIR_COEF_HV2_i [7]	RW	32	0x0000 07A4 + (0x8 * i)	0x5800 17A4 + (0x8 * i)
DISPC_WB_FIR_COEF_V2_i [7]	RW	32	0x0000 07E0 + (0x4 * i)	0x5800 17E0 + (0x4 * i)
DISPC_GLOBAL_BUFFER	RW	32	0x0000 0800	0x5800 1800
DISPC_DIVISOR	RW	32	0x0000 0804	0x5800 1804
DISPC_WB_ATTRIBUTES2	RW	32	0x0000 0810	0x5800 1810
DISPC_DEFAULT_COLOR3	RW	32	0x0000 0814	0x5800 1814
DISPC_TRANS_COLOR3	RW	32	0x0000 0818	0x5800 1818
DISPC_CPR3_COEF_B	RW	32	0x0000 081C	0x5800 181C
DISPC_CPR3_COEF_G	RW	32	0x0000 0820	0x5800 1820
DISPC_CPR3_COEF_R	RW	32	0x0000 0824	0x5800 1824
DISPC_DATA3_CYCLE1	RW	32	0x0000 0828	0x5800 1828
DISPC_DATA3_CYCLE2	RW	32	0x0000 082C	0x5800 182C
DISPC_DATA3_CYCLE3	RW	32	0x0000 0830	0x5800 1830
DISPC_SIZE_LCD3	RW	32	0x0000 0834	0x5800 1834
DISPC_DIVISOR3	RW	32	0x0000 0838	0x5800 1838
DISPC_POL_FREQ3	RW	32	0x0000 083C	0x5800 183C
DISPC_TIMING_H3	RW	32	0x0000 0840	0x5800 1840
DISPC_TIMING_V3	RW	32	0x0000 0844	0x5800 1844
DISPC_CONTROL3	RW	32	0x0000 0848	0x5800 1848
DISPC_CONFIG3	RW	32	0x0000 084C	0x5800 184C
DISPC_GAMMA_TABLE3	W	32	0x0000 0850	0x5800 1850
DISPC_BA0_FLIPIMMEDIATE_EN	RW	32	0x0000 0854	0x5800 1854
DISPC_GLOBAL_MFLAG_ATTRIBUTE	RW	32	0x0000 085C	0x5800 185C
DISPC_GFX_MFLAG_THRESHOLD	RW	32	0x0000 0860	0x5800 1860
DISPC_VID1_MFLAG_THRESHOLD	RW	32	0x0000 0864	0x5800 1864
DISPC_VID2_MFLAG_THRESHOLD	RW	32	0x0000 0868	0x5800 1868
DISPC_VID3_MFLAG_THRESHOLD	RW	32	0x0000 086C	0x5800 186C
DISPC_WB_MFLAG_THRESHOLD	RW	32	0x0000 0870	0x5800 1870

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10.2.7.3.2 DISPC Register Description

Table 10-131. DISPC_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5800 1000	**Instance**	DISPC
Description	IP Revision		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1).

(1) TI internal data

Table 10-132. Register Call Summary for Register DISPC_REVISION

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-133. DISPC_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5800 1010	**Instance**	DISPC
Description	This register allows to control various parameters of the OCP interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MIDLEMODE		RESERVED		CLOCKACTIVITY		RESERVED		WARMRESET		SIDLEMODE		ENWAKEUP		SOFTRESET		AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Write 0s for future compatibility. Reads returns 0.	R	0x00000
13:12	MIDLEMODE	Master interface power management, standby/wait control 0x0: Force-standby. MStandby is only asserted when the module is disabled. MStandby is only asserted when the module is disabled. 0x1: No-Standby: MStandby is never asserted. 0x2: Smart-Standby. MStandby is asserted based on the internal activity of the module. 0x3: Reserved	RW	0x0
11:10	RESERVED	Write 0s for future compatibility. Reads returns 0	R	0x0

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Bits	Field Name	Description	Type	Reset
9:8	CLOCKACTIVITY	Clocks activity during wake up mode period 0x0: OCP and functional clocks can be switched off. 0x1: Functional clocks can be switched off and OCP clocks are maintained during wake up period. 0x2: OCP clocks can be switched off and Functional clocks are maintained during wake up period. 0x3: OCP and functional clocks are maintained during wake-up period.	RW	0x0
7:6	RESERVED	Write 0s for future compatibility. Reads returns 0	R	0x0
5	WARMRESET	Warm reset. Set this bit to 1 triggers a module warm reset. The bit is automatically reset by the hardware. During reads, it always returns 0. The warm reset keep the configuration registers unchanged. 0x0: Normal mode 0x1: The warm reset is set.	RW	0
4:3	SIDLEMODE	Slave interface power management, Idle req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged. 0x2: Smart-idle. Acknowledgment to an idle request is given based on the internal activity of the module. 0x3: Reserved	RW	0x0
2	ENWAKEUP	WakeUp feature control 0x0: Wakeup is disabled. 0x1: Wakeup is enabled.	RW	0
1	SOFTRESET	Software reset. Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads, it always returns 0. 0x0: Normal mode 0x1: The module is reset.	RW	0
0	AUTOIDLE	Internal interface clock gating strategy 0x0: Interface clock is free-running. 0x1: Automatic interface L3_MAIN gating strategy is applied, based on the OCP interface activity. Automatic functional clock gating is also applied to the functional clock based on the module activity (for instance DISPC_<pipe>_ATTRIBUTES.ENABLE).	RW	1

Table 10-134. Register Call Summary for Register DISPC_SYSCONFIG

Display Controller

- DISPC Software Reset: [0] [1]
- DISPC Idle Mode: [2]
- DISPC StandBy Mode: [3]
- DISPC Wakeup: [4]
- DISPC DMA Ultralow-Power Mode: [5]
- DISPC Shadow Registers: [6]
- DISPC Register Summary: [7]

Table 10-135. DISPC_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5800 1014	**Instance**	DISPC
Description	This register provides status information about the module, excluding the interrupt status information.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is on-going. Read 0x1: Reset completed	R	1

Table 10-136. Register Call Summary for Register DISPC_SYSSTATUS

Display Controller

- DISPC Software Reset: [0]
- DISPC Shadow Registers: [1]
- DISPC Register Summary: [2]

Table 10-137. DISPC_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5800 1018	**Instance**	DISPC
Description	This register regroups all the status of the module internal events that generate an interrupt. Write 1 to a given bit resets this bit		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLIPIMMEDIATEDONE_IRQ	FRAMEDONE3_IRQ	ACBIASCOUNTSTATUS3_IRQ	VSYNC3_IRQ	SYNCLOST3_IRQ	WBINCOMPLETEERROR_IRQ	WBBUFFEROVERFLOW_IRQ	FRAMEDONETV_IRQ	FRAMEDONEWB_IRQ	FRAMEDONE2_IRQ	ACBIASCOUNTSTATUS2_IRQ	VID3BUFFERUNDERFLOW_IRQ	VID3ENDWINDOW_IRQ	VSYNC2_IRQ	SYNCLOST2_IRQ	WAKEUP_IRQ	SYNCLOSTTV_IRQ	SYNCLOST1_IRQ	VID2ENDWINDOW_IRQ	VID2BUFFERUNDERFLOW_IRQ	VID1ENDWINDOW_IRQ	VID1BUFFERUNDERFLOW_IRQ	OCPERROR_IRQ	PALETTEGAMMALOADING_IRQ	GFXENDWINDOW_IRQ	GFXBUFFERUNDERFLOW_IRQ	PROGRAMMEDLINENUMBER_IRQ	ACBIASCOUNTSTATUS1_IRQ	EVSYNC_ODD_IRQ	EVSYNC_EVEN_IRQ	VSYNC1_IRQ	FRAMEDONE1_IRQ

Bits	Field Name	Description	Type	Reset
31	FLIPIMMEDIATEDONE_IRQ	Flip Immediate Done. The DMA engine has acknowledged the immediate BA change, and software can write the new BA0. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
30	FRAMEDONE3_IRQ	Frame done for the third LCD. The third LCD output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
29	ACBIASCOUNT STATUS3_IRQ	AC bias count status for the third LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
28	VSYNC3_IRQ	Vertical synchronization for the third LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
27	SYNCLOST3_IRQ	Synchronization lost on the third LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the third LCD output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
26	WBUNCOMPLETE ERROR_IRQ	Write-back DMA buffer is flushed before it is completely drained. In WB capture mode, if the new frame starts before the WB DMA buffers are fully drained (onto external memory), then the contents of the WB DMA buffers are lost (implying last few pixels/lines are corrupted in the captured frame in memory). This interrupt is an indication of that case and will trigger every frame 0x0: READS: Event is false. WRITES: Status bit unchanged 0x1: READS: Event is true (Pending) WRITES: Status bit is reset	RW W1toClr	0
25	WBBUFFER OVERFLOW_IRQ	Write-back DMA buffer overflow. The DMA buffer is full. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
24	FRAME DONETV_IRQ	Frame done for the TV. The TV output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
23	FRAME DONEWB_IRQ	Frame done for the write-back channel. The write-back channel has output the frame. All the data of the frame have been sent to the memory. There is no pending data inside the DMA engine for the write-back channel to be transferred to memory. It is available only when the write-back pipeline transfers back to memory the output of one of the pipelines. In case of overlay capture, the interrupt is not generated and the user shall use the FrameDone for the corresponding captured output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
22	FRAME DONE2_IRQ	Frame done for the secondary LCD. The secondary LCD output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
21	ACBIASCOUNT STATUS2_IRQ	AC bias count status for the secondary LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
20	VID3BUFFER UNDERFLOW_IRQ	Video 3 DMA buffer underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
19	VID3END WINDOW_IRQ	The end of the video 3 window has been reached. It is detected by the overlay manager when the full video 3 has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
18	VSYNC2_IRQ	Vertical synchronization for the secondary LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
17	SYNC LOST2_IRQ	Synchronization lost on the secondary LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the secondary LCD output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
16	WAKEUP_IRQ	Wakeup 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
15	SYNCLOST TV_IRQ	Synchronization lost on the TV output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the TV output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
14	SYNC LOST1_IRQ	Synchronizationl ost on the primary LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the primary LCD output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
13	VID2END WINDOW_IRQ	The end of the video 2 Window has been reached. It is detected by the overlay manager when the full video 2 has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
12	VID2BUFFER UNDERFLOW_IRQ	Video 2 DMA buffer underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
11	VID1END WINDOW_IRQ	The end of the video 1 Window has been reached. It is detected by the overlay manager when the full video 1 has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
10	VID1BUFFER UNDERFLOW_IRQ	Video 1 DMA buffer underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
9	OCPERROR_IRQ	OCP error. L3_MAIN Interconnect has sent SResp=ERR. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
8	PALETTEGAMMA LOADING_IRQ	Palette Gamma loading status. The palette used as Color Look Up Table (CLUT) for the graphics BITMAP formats (1-, 2-, 4-, or 4-bpp) or as gamma table for the overlay output for the primary LCD output has been loaded successfully. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
7	GFXEND WINDOW_IRQ	The end of the graphics wndow has been reached. It is detected by the overlay manager when the full graphics has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
6	GFXBUFFER UNDERFLOW_IRQ	Graphics DMA buffer underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
5	PROGRAMMED LINENUMBER_IRQ	Programmed line number. It indicates that the scan of the primary LCD has reached the programmed user line number. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
4	ACBIASCOUNT STATUS1_IRQ	AC bias count status for the primary LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
3	EVSYNC_ ODD_IRQ	VSYNC for odd field from the TV encoder (HDMI) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
2	EVSYNC_ EVEN_IRQ	VSYNC for even field from the TV encoder (HDMI) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
1	VSYNC1_IRQ	Vertical synchronization for the primary LCD. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
0	FRAME DONE1_IRQ	Frame done for the primary LCD. The primary LCD output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0

Table 10-138. Register Call Summary for Register DISPC_IRQSTATUS

Display Controller

- DISPC Interrupt Requests: [0]
- DISPC Immediate Base Address Flip Mechanism: [1]
- DISPC WRITE DMA Buffer (WB Pipeline): [2]
- DISPC Synchronized Buffer Update: [3]
- DISPC Shadow Registers: [4]
- DISPC Register Summary: [5]

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Table 10-139. DISPC_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x5800 101C	**Instance**	DISPC
Description	This register allows to mask/unmask the module internal sources of interrupt, on an event-by-event basis		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLIPIMMEDIATEDONE_EN	FRAMEDONE3_EN	ACBIASCOUNTSTATUS3_EN	VSYNC3_EN	SYNCLOST3_EN	WBUNCOMPLETEERROR_EN	WBBUFFEROVERFLOW_EN	FRAMEDONETV_EN	FRAMEDONEWB_EN	FRAMEDONE2_EN	ACBIASCOUNTSTATUS2_EN	VID3BUFFERUNDERFLOW_EN	VID3ENDWINDOW_EN	VSYNC2_EN	SYNCLOST2_EN	WAKEUP_EN	SYNCLOSTTV_EN	SYNCLOST1_EN	VID2ENDWINDOW_EN	VID2BUFFERUNDERFLOW_EN	ENDVID1WINDOW_EN	VID1BUFFERUNDERFLOW_EN	OCPERROR_EN	PALETTEGAMMA_EN	GFXENDWINDOW_EN	GFXBUFFERUNDERFLOW_EN	PROGRAMMEDLINENUMBER_EN	ACBIASCOUNTSTATUS1_EN	EVSYNC_ODD_EN	EVSYNC_EVEN_EN	VSYNC1_EN	FRAMEDONE_EN

Bits	Field Name	Description	Type	Reset
31	FLIPIMMEDIATEDONE_EN	Flip Immediate Done. The DMA engine has acknowledged the immediate BA change, and software can write the new BA0. 0x0: FrameDone for the primary LCD output is masked 0x1: FrameDone for the primary LCD output generates an interrupt when it occurs	RW	0
30	FRAME DONE3_EN	Frame done for the third LCD. The third LCD output has been disabled by user. All the data have been sent. 0x0: Frame Done for the secondary LCD is masked. 0x1: Frame Done for the secondary LCD generates an interrupt when it occurs.	RW	0
29	ACBIASCOUNT STATUS3_EN	AC Bias count status for the third LCD 0x0: ACBiasCountStatus for the secondary LCD output is masked 0x1: ACBiasCountStatus for the secondary LCD output generates an interrupt when it occurs	RW	0
28	VSYNC3_EN	Vertical synchronization for the third LCD 0x0: VSYNC for the secondary LCD output is masked. 0x1: VSYNC for the secondary LCD output generates an interrupt when it occurs.	RW	0
27	SYNC LOST3_EN	Synchronization lost on the third LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the third LCD output. 0x0: Synchronization Lost on the secondary LCD output is masked. 0x1: Synchronization Lost on the secondary LCD output generates an interrupt when it occurs.	RW	0
26	WBUNCOMPLETE ERROR_EN	The write back buffer has been flushed before been fully drained. Enable. 0x0: Interrupt is masked. 0x1: Interrupt is enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
25	WBBUFFER OVERFLOW_EN	Write-back DMA buffer overflow. The DMA buffer is full. 0x0: WBBufferOverflow is masked. 0x1: WBBufferOverflow generates an interrupt when it occurs.	RW	0
24	FRAME DONETV_EN	Frame done for the TV. The TV output has been disabled by user. All the data have been sent. 0x0: Frame Done for the TV output is masked. 0x1: Frame Done for the TV output generates an interrupt when it occurs.	RW	0
23	FRAME DONEWB_EN	Frame done for the write-back channel. The write-back channel has output the frame. All the data have been sent for the frame have been sent to the memory. There is no pending data inside the DMA engine for the write-back channel to be transferred to memory. 0x0: Frame done for the write-back is masked. 0x1: Frame done for the write-back generates an interrupt when it occurs.	RW	0
22	FRAME DONE2_EN	Frame done for the secondary LCD. The secondary LCD output has been disabled by user. All the data have been sent. 0x0: Frame done for the secondary LCD is masked. 0x1: Frame done for the secondary LCD generates an interrupt when it occurs.	RW	0
21	ACBIASCOUNT STATUS2_EN	AC Bias count status for the secondary LCD 0x0: ACBiasCountStatus for the secondary LCD output is masked. 0x1: ACBiasCountStatus for the secondary LCD output generates an interrupt when it occurs.	RW	0
20	VID3BUFFER UNDERFLOW_EN	Video 3 DMA Buffer Underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: Vid3BufferUnderflow is masked. 0x1: Vid3BufferUnderflow generates an interrupt when it occurs.	RW	0
19	VID3END WINDOW_EN	The end of the video 3 window has been reached. It is detected by the overlay manager when the full video 3 has been displayed. 0x0: Vid3EndWindow is masked. 0x1: Vid3EndWindow generates an interrupt when it occurs.	RW	0
18	VSYNC2_EN	Vertical synchronization for the secondary LCD 0x0: VSYNC for the secondary LCD output is masked. 0x1: VSYNC for the secondary LCD output generates an interrupt when it occurs.	RW	0
17	SYNC LOST2_EN	Synchronization lost on the secondary LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the secondary LCD output. 0x0: Synchronization Lost on the secondary LCD output is masked. 0x1: Synchronization Lost on the secondary LCD output generates an interrupt when it occurs.	RW	0
16	WAKEUP_EN	Wake up mask 0x0: WakeUp is masked. 0x1: WakeUp generates an interrupt when it occurs.	RW	0

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Bits	Field Name	Description	Type	Reset
15	SYNC LOSTTV_EN	Synchronization lost on the TV output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the TV output. 0x0: Synchronization Lost on the TV output is masked. 0x1: Synchronization Lost on the TV output generates an interrupt when it occurs.	RW	0
14	SYNC LOST1_EN	Synchronization lost for the primary LCD 0x0: SyncLost for the primary LCD output is masked. 0x1: SyncLost for the primary LCD output generates an interrupt when it occurs.	RW	0
13	VID2END WINDOW_EN	The end of the video 2 Window has been reached. It is detected by the overlay manager when the full video 2 has been displayed. 0x0: Vid2EndWindow is masked. 0x1: Vid2EndWindow generates an interrupt when it occurs.	RW	0
12	VID2BUFFER UNDERFLOW_EN	Video 2 DMA buffer underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: Vid2BufferUnderflow is masked. 0x1: Vid2BufferUnderflow generates an interrupt when it occurs.	RW	0
11	ENDVID1 WINDOW_EN	The end of the video 1 window has been reached. It is detected by the overlay manager when the full video 1 has been displayed. 0x0: EndVid1Window is masked. 0x1: EndVid1Window generates an interrupt when it occurs.	RW	0
10	VID1BUFFER UNDERFLOW_EN	Video 1 DMA buffer underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: Vid1bufferunderflow is masked. 0x1: Vid1bufferunderflow generates an interrupt when it occurs.	RW	0
9	OCPERROR_EN	OCP Error. L3_MAIN Interconnect has sent SResp=ERR. 0x0: OCPError is masked. 0x1: OCPError generates an interrupt when it occurs.	RW	0
8	PALETTE GAMMA_EN	Palette gamma loading mask. The palette used as Color Look Up Table (CLUT) for the graphics BITMAP formats (1-, 2-, 4-, or 4-bpp) or as gamma table for the overlay output for the primary LCD output has been loaded successfully. 0x0: PaletteGamma is masked. 0x1: PaletteGamma generates an interrupt when it occurs.	RW	0
7	GFXEND WINDOW_EN	The end of the graphics Window has been reached. It is detected by the overlay manager when the full graphics has been displayed. 0x0: GfxEndWindow is masked. 0x1: GfxEndWindow generates an interrupt when it occurs.	RW	0
6	GFXBUFFER UNDERFLOW_EN	Graphics DMA Buffer Underflow. The DMA buffer is not necessarily empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: GfxBufferUnderflow is masked. 0x1: GfxBufferUnderflow generates an interrupt when it occurs.	RW	0

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Bits	Field Name	Description	Type	Reset
5	PROGRAMMED LINENUMBER_EN	Programmed Line Number. It indicates that the scan of the primary LCD has reached the programmed user line number. 0x0: ProgrammedLineNumber is masked. 0x1: ProgrammedLineNumber generates an interrupt when it occurs.	RW	0
4	ACBIASCOUNT STATUS1_EN	AC Bias count status for the primary LCD 0x0: ACBiascountstatus for the primary LCD output is masked. 0x1: ACBiascountstatus for the primary LCD output generates an interrupt when it occurs.	RW	0
3	EVSYNC_ODD_EN	VSYNC for odd field from the TV encoder (HDMI) 0x0: EVSYNC_ODD for the TV output is masked. 0x1: EVSYNC_ODD for the TV output generates an interrupt when it occurs.	RW	0
2	EVSYNC_EVEN_EN	VSYNC for even field from the TV encoder (HDMI) 0x0: EVSYNC_EVEN for the TV output is masked. 0x1: EVSYNC_EVEN for the TV output generates an interrupt when it occurs.	RW	0
1	VSYNC1_EN	Vertical synchronization for the primary LCD. 0x0: VSYNC for the primary LCD output is masked. 0x1: VSYNC for the primary LCD output generates an interrupt when it occurs.	RW	0
0	FRAMEDONE_EN	Frame done for the primary LCD. The primary LCD output has been disabled by user. All the data have been sent. 0x0: Frame Done for the primary LCD output is masked. 0x1: FrameDone for the primary LCD output generates an interrupt when it occurs.	RW	0

Table 10-140. Register Call Summary for Register DISPC_IRQENABLE

Display Controller

- DISPC Interrupt Requests: [0]
- DISPC Immediate Base Address Flip Mechanism: [1]
- DISPC WRITE DMA Buffer (WB Pipeline): [2]
- DISPC Synchronized Buffer Update: [3]
- DISPC Shadow Registers: [4]
- DISPC Register Summary: [5]

Table 10-141. DISPC_CONTROL1

Address Offset	0x0000 0040		
Physical Address	0x5800 1040	**Instance**	DISPC
Description	The control register configures the Display Controller module for the primary LCD and TV outputs.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPATIALTEMPORALDITHERINGFRAMES		LCDENABLEPOL	LCDENABLESIGNAL	PCKFREEENABLE	TDMUNUSEDBITS		TDMCYCLEFORMAT	TDMPARALLELMODE			TDMENABLE	HT			GPOUT1	GPOUT0	GPIN1	GPIN0	OVERLAYOPTIMIZATION	STALLMODE	RESERVED	TFTDATALINES		STDITHERENABLE	GOTV	GOLCD	M8B	STNTFT	MONOCOLOR	TVENABLE	LCDENABLE

Bits	Field Name	Description	Type	Reset
31:30	SPATIALTEMPORAL DITHERINGFRAMES	Spatial/temporal dithering number of frames for the primary LCD output wr: VFP start period of primary LCD 0x0: Spatial only 0x1: Spatial and temporal over 2 frames 0x2: Spatial and temporal over 4 frames 0x3: Reserved	RW	0x0
29	LCDENABLEPOL	Write 0s for future compatibility. Reads return 0.	R	0
28	LCDENABLESIGNAL	Write 0s for future compatibility. Reads return 0.	R	0
27	PCKFREEENABLE	Write 0s for future compatibility. Reads return 0.	R	0
26:25	TDMUNUSEDBITS	State of unused bits (TDM mode only) for the primary LCD output. wr: VFP start period of primary LCD 0x0: Low level (0) 0x1: High level (1) 0x2: Unchanged from previous state 0x3: Reserved	RW	0x0
24:23	TDMCYCLEFORMAT	Cycle format (TDM mode only) for the primary LCD output WR: VFP start period of primary LCD 0x0: 1 cycle for 1 pixel 0x1: 2 cycles for 1 pixel 0x2: 3 cycles for 1 pixel 0x3: 3 cycles for 2 pixels	RW	0x0
22:21	TDMPARALLELMODE	Output interface width (TDM mode only) for the primary LCD output WR: VFP start period of primary LCD 0x0: 8-bit parallel output interface selected 0x1: 9-bit parallel output interface selected 0x2: 12-bit parallel output interface selected 0x3: 16-bit parallel output interface selected	RW	0x0
20	TDMENABLE	Enable the multiple cycle format (TDM mode only used for TFT mode with the RFBI enable bit off) for the primary LCD output. WR: VFP start period of primary LCD 0x0: TDM disabled 0x1: TDM enabled	RW	0

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Bits	Field Name	Description	Type	Reset
19:17	HT	Hold time for TV output WR: EVSYNC Encoded value (from 1 to 8) to specify the number of external digital clock periods to hold the data (programmed value = value minus 1)	RW	0x0
16	GPOUT1	General purpose output signal l WR: immediate 0x0: The GPout1 is reset. 0x1: The GPout1 is set.	RW	0
15	GPOUT0	General Purpose Output Signal WR:immediate 0x0: The GPout0 is reset. 0x1: The GPout0 is set.	RW	0
14	GPIN1	General purpose input signal WR: immediately Read 0x0: The GPin1 has been reset. Read 0x1: The GPin1 has been set.	R	0
13	GPIN0	General purpose input signal WR: immediately Read 0x0: The GPin0 has been reset. Read 0x1: The GPin0 has been set.	R	0
12	OVERLAYOPTIMIZATION	Overlay optimization for the primary LCD output WR: VFP start period of the primary LCD 0x0: All the data for all the enabled pipelines are fetched from memory regardless of the overlay/alpha blending configuration. 0x1: The data not used by the overlay manager because of overlap between layers with no alpha blending between them must not be fetched from memory in order to optimize the bandwidth.	RW	0
11	STALLMODE	STALL Mode for the primary LCD output WR: VFP start period of primary LCD 0x0: Normal mode selected 0x1: STALL mode selected. The Display Controller sends the data without considering the VSYNC/HSYNC. The LCD output is disabled at the end of the transfer of the frame. The S/W has to re-enable the LCD output in order to generate a new frame. The stall mode is used in RFBI and DSI command modes.	RW	0
10	RESERVED	Reserved	R	0
9:8	TFTDATALINES	Number of lines of the primary LCD interface WR: VFP start period of primary LCD 0x0: 12-bit output aligned on the LSB of the pixel data interface 0x1: 16-bit output aligned on the LSB of the pixel data interface 0x2: 18-bit output aligned on the LSB of the pixel data interface 0x3: 24-bit output aligned on the LSB of the pixel data interface	RW	0x0
7	STDITHERENABLE	Spatial temporal dithering enable for the primary LCD output WR: VFP start period of primary LCD 0x0: Spatial/temporal dithering logic disabled 0x1: Spatial/temporal dithering logic enabled	RW	0

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Bits	Field Name	Description	Type	Reset
6	GOTV	GO command for the TV output. It is used to synchronized the pipelines (graphics and/or video ones) associated with the TV output. WR: immediate 0x0: The hardware has finished updating the internal shadow registers of the pipeline(s) associated with the TV output using the user values. The hardware resets the bit when the update is completed. 0x1: The user has finished to program the shadow registers of the pipeline(s) associated with the TV output and the hardware can update the internal registers at the external VSYNC.	RW	0
5	GOLCD	GO command for the primary LCD output. It is used to synchronized the pipelines (graphics and/or video ones) associated with the primary LCD output. WR: immediate 0x0: The hardware has finished updating the internal shadow registers of the pipeline(s) connected to the LCD output using the user values. The hardware resets the bit when the update is completed. 0x1: The user has finished to program the shadow registers of the pipeline(s) associated with the LCD output and the hardware can update the internal registers at the VFP start period	RW	0
4	M8B	Mono 8-bit mode of the primary LCD wr: VFP start period of primary LCD output 0x0: Reserved 0x1: Reserved	RW	0
3	STNTFT	LCD Display type of the primary LCD WR: VFP start period of primary LCD output 0x0: STN display operation enabled. STN dither logic is enabled. 0x1: Active or TFT display operation enabled. STN Dither logic and output FIFO bypassed.	RW	0
2	MONOCOLOR	Monochrome/color selection for the primary LCD WR: VFP start period of primary LCD output 0x0: Color operation enabled (STN mode only) 0x1: Monochrome operation enabled (STN mode only)	RW	0
1	TVENABLE	Enable the TV output wr: immediate effect only occurs at the end of the current frame. 0x0: TV output disabled (at the end of the current field if interlace output when the bit is reset) 0x1: TV output enabled	RW	0
0	LCDENABLE	Enable the primary LCD outputs wr: immediate Effect only occurs at the end of the current frame 0x0: LCD output disabled (at the end of the frame when the bit is reset) 0x1: LCD output enabled	RW	0

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Table 10-142. Register Call Summary for Register DISPC_CONTROL1

Display Controller

- DISPC Graphics Pipeline: [0] [1] [2] [3]
- DISPC Video Pipelines: [4] [5] [6] [7]
- DISPC Overlay Optimization: [8]
- DISPC Timing and TV Format Settings: [9]
- DISPC Shadow Registers: [10] [11] [12] [13]
- DISPC GFX Pipeline Configuration: [14] [15]
- DISPC Video Pipeline Configuration: [16] [17]
- DISPC LCD Output Configuration: [18] [19]
- DISPC TV Output Configuration: [20] [21]
- DISPC Logical Register Mapping: [22]
- DISPC Register Summary: [23]

Table 10-143. DISPC_CONFIG1

Address Offset	0x0000 0044		
Physical Address	0x5800 1044	**Instance**	DISPC
Description	The control register configures the Display Controller module for the primary LCD output and TV output. Shadow register, updated on VFP start period of primary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TVINTERLEAVE		PLCDINTERLEAVE		FULLRANGE	COLORCONVENABLE	FIDFIRST	OUTPUTMODEENABLE	RESERVED		TVALPHABLENDERENABLE	LCDALPHABLENDERENABLE	BUFFERFILLING	BUFFERHANDCHECK	CPR	BUFFERMERGE	TCKTVSELECTION	TCKTVENABLE	TCKLCDSELECTION	TCKLCDENABLE	GAMATABLEENABLE	ACBIASGATED	VSYNCGATED	HSYNCGATED	PIXELCLOCKGATED	PIXELDATAGATED	PALETTEGAMMATABLE	LOADMODE		PIXELGATED

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
29:28	TVINTERLEAVE	TV Interleave Pattern	RW	0x0
27:26	PLCDINTERLEAVE	pLCD Interleave Pattern	RW	0x0
25	FULLRANGE	Color Space Conversion full range setting. wr: VFP start of primary LCD 0x0: Limited range selected. 0x1: Full range selected.	RW	0
24	COLORCONV ENABLE	Enable the color space conversion. It shall be reset when CPR bit field is set to 0x1. wr: VFP start of primary LCD 0x0: Disable Color Space Conversion RGB to YUV 0x1: Enable Color Space Conversion RGB to YUV	RW	0
23	FIDFIRST	Selects the first field to output in case of interlace mode. In case of progressive mode, the value is not used. wr: VFP start of primary LCD 0x0: First field is even. 0x1: Odd field is first.	RW	0

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Bits	Field Name	Description	Type	Reset
22	OUTPUTMODE ENABLE	Selects between progressive and interlace mode for the primary LCD output. wr: VFP start of primary LCD 0x0: Progressive mode selected. 0x1: Interlace mode selected.	RW	0
21:20	RESERVED	Write 0s for future compatibility. Reads return 0.	RW	0
19	TVALPHABLENDER ENABLE	Selects the alpha blender overlay manager for the TV output instead of the color key alpha blender (LCD output). The bit field is deprecated. It is present for software backward compatibility only. When it is enabled, the Z-order defined in each ATTRIBUTES registers for only the pipelines associated pipeline connected to the TV output are invalid and replaced by the following: graphics z-order = 3, video3 z-order = 2, video2 z-order =1 and video1 z-order=0 If it disabled, the z-order and z-order enable bit fields defined in each ATTRIBUTES register are used. wr: EVSYNC start of primary LCD 0x0: Alpha blender is disabled. 0x1: The alpha blender is enabled.	RW	0
18	LCDALPHABLENDER ENABLE	Selects the alpha blender overlay manager for the primary LCD output instead of the color key alpha blender (LCD output). The bit field is deprecated. It is present for software backward compatibility only. When it is enabled, the Z-order defined in each ATTRIBUTES registers for only the pipelines associated with the primary LCD output are invalid and replaced by the following: graphics z-order = 3, video3 z-order = 2, video2 z-order =1 and video1 z-order=0 If it disabled, the z-order and z-order enable bit fields defined in each ATTRIBUTES register are used. wr: VFP start of primary LCD 0x0: Alpha blender is disabled. The color key alpha blending is used. 0x1: The alpha blender is enabled.	RW	0
17	BUFFERFILLING	Controls if the DMA buffers are refilled only when the LOW threshold is reached or if all DMA buffers are refilled when at least one of them reaches the LOW threshold. wr: immediate 0x0: Each DMA buffer is refilled when it reaches LOW threshold. 0x1: All DMA buffers are refilled up to high threshold when at least one of them reaches the LOW threshold. (only active DMA buffers shall be considered and when reaching the end of the frame the DMA buffer goes to empty condition so no need to fill it again).	RW	0
16	BUFFERHAND CHECK	Controls the handcheck between DMA buffer and STALL signal in order to prevent from underflow. The bit shall be set to 0 when the module is not in STALL mode. (primary LCD output) wr: VFP start of primary LCD 0x0: Only the STALL signal (generated by RFBI, DSI1_A or DSI1_C depending on which IP uses the LCD output) is used regardless of the DMA buffer fullness information in order to provide data to the RFBI,DSI1_A or DS1_C module. 0x1: The STALL signal (generated by RFBI, DSI1_A or DSI1_C depending on which IP uses the LCD output) is used in combination with the DMA buffer fullness information in order to provide data to the RFBI, DSI1_A or DSI1_C module only when it does not generated buffer underflow.	RW	0

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Bits	Field Name	Description	Type	Reset
15	CPR	Color phase rotation control (primary LCD output). It shall be reset when ColorConvEnable bit field is set to 1 wr: VFP start period of primary LCD output 0x0: Color Phase Rotation Disabled 0x1: Color Phase Rotation Enabled	RW	0
14	BUFFERMERGE	Buffer merge control wr: EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory or VFP When enabled, the DISPC_GLOBAL_BUFFER register is ignored. This bit must be set to zero when the write back channel is used. When DISPC_CONTROL2.GOWB is used BUFFERMERGE MUST be zero. When DISPC_CONTROL2.GOWB is used BUFFERMERGE MUST be zero. WR: immediate 0x0: DMA buffer merge disabled Each DMA buffer is dedicated to one pipeline. 0x1: DMA buffer merge enabled All the DMA buffers are merged into a single one to be used by the single active pipeline.	RW	0
13	TCKTV SELECTION	Transparency color key selection (TV output) wr: EVSYNC 0x0: Destination transparency color key selected 0x1: Source transparency color key selected	RW	0
12	TCKTVENABLE	Transparency color key enabled (TV output) WR: EVSYNC 0x0: Disable the transparency color key for the TV output 0x1: Enable the transparency color key for the TV output	RW	0
11	TCKLCD SELECTION	Transparency color key selection (primary LCD output) wr: VFP start period of primary LCD output 0x0: Destination transparency color key selected 0x1: Source transparency color key selected	RW	0
10	TCKLCDENABLE	Transparency color key enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: Disable the transparency color key for the LCD 0x1: Enable the transparency color key for the LCD	RW	0
9	GAMATABLE ENABLE	For backward compatibility, an enable bit has been added on the 2 additional gamma tables (secondary display and TV). Gamma table of LCD1 is always enabled. 0x0: Gamma table LCD2 and TV are bypassed 0x1: Gamma table LCD2 and TV are enabled	RW	0
8	ACBIASGATED	ACBias Gated Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: AcBias gated disabled 0x1: AcBias gated enabled	RW	0
7	VSYNCGATED	VSYNC Gated Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: VSYNC gated disabled 0x1: VSYNC gated enabled	RW	0
6	HSYNCGATED	HSYNC Gated Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: HSYNC gated disabled 0x1: HSYNC gated enabled	RW	0

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Bits	Field Name	Description	Type	Reset
5	PIXELCLOCK GATED	Pixel Clock Gated Enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: Pixel clock gated disabled 0x1: Pixel clock gated enabled	RW	0
4	PIXELDATAGATED	Pixel data gated enabled (primary LCD output) wr: VFP start period of primary LCD output 0x0: Pixel data gated disabled 0x1: Pixel data gated enabled	RW	0
3	PALETTEGAMMA TABLE	Palette/gamma table selection wr: VFP start period of primary LCD output or VFP start period of secondary LCD output or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the graphics pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory. In case of the table is used as gamma table, it is used for the primary LCD output only. 0x0: LUT used as palette (only if graphics format is BITMAP1, 2, 4, and 8) 0x1: LUT used as gamma table (only if graphics format is NOT BITMAP1, 2, 4, and 8 or no graphics window present)	RW	0
2:1	LOADMODE	Loading mode for the palette/gamma table wr: VFP start period of primary LCD output or VFP start period of secondary LCD output or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory 0x0: Palette/Gamma Table and data are loaded every frame 0x1: Palette/Gamma Table to be loaded. The user sets the bit when the palette/gamma table has to be loaded. Hardware resets the bit to 0x2 when table has been loaded. (DISPC_GFX_ATTRIBUTES.ENABLE has to be set to 1). 0x2: Frame data only loaded every frame 0x3: Palette/Gamma Table and frame data loaded on first frame then switch to 0x2 (Hardware).	RW	0x0
0	PIXELGATED	Pixel gated enable (only for TFT) (primary LCD output) wr: VFP start period of primary LCD output 0x0: Pixel clock always toggles (only in TFT mode) 0x1: Pixel clock only toggles when there is valid data to display. (only in TFT mode)	RW	0

Table 10-144. Register Call Summary for Register DISPC_CONFIG1

Display Controller

- DISPC Wakeup: [0]
- DISPC Color Look-Up Table (CLUT): [1] [2]
- DISPC Transparency Color Keys: [3] [4] [5] [6] [7] [8]
- DISPC Extended 3D Support - Line Alternative Format: [9] [10]
- DISPC Shadow Registers: [11]
- DISPC GFX Pipeline Configuration: [12] [13]
- DISPC LCD Output Configuration: [14] [15] [16]
- DISPC TV Output Configuration: [17] [18] [19] [20] [21]
- DISPC Logical Register Mapping: [22]
- DISPC Register Summary: [23]

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Table 10-145. DISPC_DEFAULT_COLOR0

Address Offset	0x0000 004C		
Physical Address	0x5800 104C	**Instance**	DISPC
Description	The control register allows to configure the default solid background color for the primary LCD. Shadow register, updated on VFP start period of the primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEFAULTCOLOR																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	DEFAULTCOLOR	24-bit RGB color value to specify the default solid color to display when there is no data from the overlays.	RW	0x000000

Table 10-146. Register Call Summary for Register DISPC_DEFAULT_COLOR0

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-147. DISPC_DEFAULT_COLOR1

Address Offset	0x0000 0050		
Physical Address	0x5800 1050	**Instance**	DISPC
Description	The control register allows to configure the default solid background color for the TV output. Shadow register, updated on EVSYNC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEFAULTCOLOR																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	DEFAULTCOLOR	24-bit RGB color value to specify the default solid color to display when there is no data from the overlays.	RW	0x000000

Table 10-148. Register Call Summary for Register DISPC_DEFAULT_COLOR1

Display Controller

- DISPC Timing and TV Format Settings: [0]
- DISPC Shadow Registers: [1]
- DISPC TV Output Configuration: [2]
- DISPC Logical Register Mapping: [3]
- DISPC Register Summary: [4]

Table 10-149. DISPC_TRANS_COLOR0

Address Offset	0x0000 0054		
Physical Address	0x5800 1054	**Instance**	DISPC
Description	The register sets the transparency color value for the video/graphics overlays for the primary LCD output. Shadow register, updated on VFP start period of the primary LCD		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRANSCOLORKEY																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	TRANSCOLORKEY	Transparency color key value in RGB format [0] BITMAP 1 (CLUT), [23,1] set to 0s [1:0] BITMAP 2 (CLUT), [23,2] set to 0s [3:0] BITMAP 4 (CLUT), [23,4] set to 0s [7:0] BITMAP 8 (CLUT), [23,8] set to 0s [11:0] RGB 12, [23,12] set to 0s [15:0] RGB 16, [23,16] set to 0s [23:0] RGB 24	RW	0x000000

Table 10-150. Register Call Summary for Register DISPC_TRANS_COLOR0

Display Controller

- DISPC Transparency Color Keys: [0]
- DISPC Shadow Registers: [1]
- DISPC Logical Register Mapping: [2]
- DISPC Register Summary: [3]

Table 10-151. DISPC_TRANS_COLOR1

Address Offset	0x0000 0058		
Physical Address	0x5800 1058	**Instance**	DISPC
Description	The register sets the transparency color value for the video/graphics overlays for the TV output. Shadow register, updated on EVSYNC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRANSCOLORKEY																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	TRANSCOLORKEY	Transparency color key value in RGB format [0] BITMAP 1 (CLUT), [23,1] set to 0s [1:0] BITMAP 2 (CLUT), [23,2] set to 0s [3:0] BITMAP 4 (CLUT), [23,4] set to 0s [7:0] BITMAP 8 (CLUT), [23,8] set to 0s [11:0] RGB 12, [23,12] set to 0s [15:0] RGB 16, [23,16] set to 0s [23:0] RGB 24	RW	0x000000

Table 10-152. Register Call Summary for Register DISPC_TRANS_COLOR1

Display Controller

- DISPC Transparency Color Keys: [0]
- DISPC Shadow Registers: [1]
- DISPC TV Output Configuration: [2]
- DISPC Logical Register Mapping: [3]
- DISPC Register Summary: [4]

Table 10-153. DISPC_LINE_STATUS

Address Offset	0x0000 005C		
Physical Address	0x5800 105C	**Instance**	DISPC
Description	The control register indicates the current primary LCD panel display line number.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LINENUMBER							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	LINENUMBER	Current LCD panel line number Current display line number. The first active line has the value 0. During blanking lines the line number is not incremented.	R	0x000

Table 10-154. Register Call Summary for Register DISPC_LINE_STATUS

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-155. DISPC_LINE_NUMBER

Address Offset	0x0000 0060		
Physical Address	0x5800 1060	**Instance**	DISPC
Description	The control register indicates the primary LCD panel display line number for the interrupt and the DMA request. Shadow register, updated on VFP start period of primary LCD.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LINENUMBER							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	LINENUMBER	LCD panel line number programming LCD line number defines the line on which the programmable interrupt is generated and the DMA request occurs.	RW	0x000

Table 10-156. Register Call Summary for Register DISPC_LINE_NUMBER

Display Controller

- DISPC DMA Requests: [0]
- DISPC Shadow Registers: [1]
- DISPC Register Summary: [2]

Table 10-157. DISPC_TIMING_H1

Address Offset	0x0000 0064		
Physical Address	0x5800 1064	**Instance**	DISPC
Description	The register configures the timing logic for the HSYNC signal. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HBP																HFP								HSW							

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Bits	Field Name	Description	Type	Reset
31:20	HBP	Horizontal Back Porch. Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the beginning of a line transmission before the first set of pixels is output to the display (program to value minus 1). When in BT mode and interlaced, this field corresponds to the vertical field blanking No 2 for Even Field.	RW	0x000
19:8	HFP	Horizontal front porch. Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the end of a line transmission before line clock is asserted (program to value minus 1). When in BT mode and interlaced, this field corresponds to the vertical field blanking No 1 for Even Field.	RW	0x000
7:0	HSW	Horizontal synchronization pulse width Encoded value (from 1 to 256) to specify the number of pixel clock periods to pulse the line clock at the end of each line (program to value minus 1). When in BT mode, this field corresponds to the horizontal blanking	RW	0x00

Table 10-158. Register Call Summary for Register DISPC_TIMING_H1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-159. DISPC_TIMING_V1

Address Offset	0x0000 0068		
Physical Address	0x5800 1068	**Instance**	DISPC
Description	The register configures the timing logic for the VSYNC signal. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBP																VFP								VSW							

Bits	Field Name	Description	Type	Reset
31:20	VBP	Vertical back porch encoded value (from 0 to 4095) to specify the number of line clock periods to add to the beginning of a frame.	RW	0x000
19:8	VFP	Vertical front porch encoded value (from 0 to 4095) to specify the number of line clock periods to add to the end of each frame.	RW	0x000
7:0	VSW	Vertical synchronization pulse width In active mode, encoded value (from 1 to 256) to specify the number of line clock periods (program to value minus 1) to pulse the frame clock (VSYNC) pin at the end of each frame after the end of frame wait (VFP) period elapses. Frame clock uses as VSYNC signal in active mode.	RW	0x00

Table 10-160. Register Call Summary for Register DISPC_TIMING_V1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-161. DISPC_POL_FREQ1

Address Offset	0x0000 006C		
Physical Address	0x5800 106C	**Instance**	DISPC
Description	The register configures the signal configuration. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ALIGN	ONOFF	RF	IEO	IPC	IHS	IVS	ACBI				ACB							

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
18	ALIGN	Defines the alignment between HSYNC and VSYNC assertion. 0x0: VSYNC and HSYNC are not aligned 0x1: VSYNC and HSYNC assertions are aligned.	RW	0
17	ONOFF	HSYNC/VSYNC Pixel clock Control On/Off 0x0: HSYNC and VSYNC are driven on opposite edges of pixel clock than pixel data 0x1: HSYNC and VSYNC are driven according to bit 16	RW	0
16	RF	Program HSYNC/VSYNC Rise or Fall 0x0: HSYNC and VSYNC are driven on falling edge of pixel clock (if bit 17 set to 1) 0x1: HSYNC and VSYNC are driven on rising edge of pixel clock (if bit 17 set to 1)	RW	0
15	IEO	Invert output enable 0x0: Ac-bias is active high (active display mode) 0x1: Ac-bias is active low (active display mode)	RW	0
14	IPC	Invert pixel clock 0x0: Data is driven on the LCD data lines on the rising-edge of the pixel clock 0x1: Data is driven on the LCD data lines on the falling-edge of the pixel clock	RW	0
13	IHS	Invert HSYNC 0x0: Line clock pin is active high and inactive low 0x1: Line clock pin is active low and inactive high	RW	0
12	IVS	Invert VSYNC 0x0: Frame clock pin is active high and inactive low 0x1: Frame clock pin is active low and inactive high	RW	0
11:8	ACBI	AC Bias pin transitions per interrupt Value (from 0 to 15) used to specify the number of AC Bias pin transitions	RW	0x0
7:0	ACB	AC Bias pin frequency value (from 0 to 255) used to specify the number of line clocks to count before transitioning the AC Bias pin. This pin is used to periodically invert the polarity of the power supply to prevent DC charge build-up within the display.	RW	0x00

Table 10-162. Register Call Summary for Register DISPC_POL_FREQ1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-163. DISPC_DIVISOR1

Address Offset	0x0000 0070		
Physical Address	0x5800 1070	**Instance**	DISPC
Description	The register configures the divisors. It is used for the primary LCD output Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LCD								RESERVED								PCD							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:16	LCD	Display controller logic clock divisor value (from 1 to 255) to specify the intermediate pixel clock frequency based on the LCD1_CLK. The value 0 is invalid.	RW	0x04
15:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
7:0	PCD	Pixel clock divisor value (from 1 to 255) to specify the frequency of the pixel clock based on the LCD1_CLK divided by DISPC_DIVISOR1.LCD value. The values 0 is invalid.	RW	0x01

Table 10-164. Register Call Summary for Register DISPC_DIVISOR1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]
- DISPC Register Description: [3] [4] [5] [6]

Table 10-165. DISPC_GLOBAL_ALPHA

Address Offset	0x0000 0074		
Physical Address	0x5800 1074	**Instance**	DISPC
Description	The register defines the global alpha value for the graphics and three video pipelines. Shadow register, updated on VFP start period of primary LCD or VFP start period of the third LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory for each bit field depending on the association of the each pipeline with the primary LCD, secondary LCD or TV output.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VID3GLOBALALPHA								VID2GLOBALALPHA								VID1GLOBALALPHA								GFXGLOBALALPHA							

Bits	Field Name	Description	Type	Reset
31:24	VID3GLOBALALPHA	Global alpha value from 0 to 255. 0 corresponds to fully transparent and 255 to fully opaque.	RW	0xFF
23:16	VID2GLOBALALPHA	Global alpha value from 0 to 255. 0 corresponds to fully transparent and 255 to fully opaque.	RW	0xFF
15:8	VID1GLOBALALPHA	Global alpha value from 0 to 255. 0 corresponds to fully transparent and 255 to fully opaque.	RW	0xFF
7:0	GFXGLOBALALPHA	Global alpha value from 0 to 255. 0 corresponds to fully transparent and 255 to fully opaque.	RW	0xFF

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Table 10-166. Register Call Summary for Register DISPC_GLOBAL_ALPHA

Display Controller

- DISPC Alpha Blender: [0]
- DISPC Shadow Registers: [1]
- DISPC GFX Pipeline Configuration: [2]
- DISPC Video Pipeline Configuration: [3]
- DISPC Register Summary: [4]

Table 10-167. DISPC_SIZE_TV

Address Offset	0x0000 0078		
Physical Address	0x5800 1078	**Instance**	DISPC
Description	The register configures the size of the TV output field (interlace), frame (progressive) (horizontal and vertical). Shadow register, updated on EVSYNC. A delta value is used to indicate if the odd field has same vertical size as the even field or +/- one line.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				LPP												DELTA_LPP		RESERVED		PPL											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
27:16	LPP	Lines per panel encoded value (from 1 to 4096) to specify the number of lines per panel.	RW	0x000
15:14	DELTA_LPP	Indicates the delta size value of the odd field compared to the even field 0x0: Same size 0x1: Odd size = Even size +1 0x2: Odd size = Even Size –1	RW	0x0
13:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:0	PPL	Pixels per line encoded value (from 1 to 4096) to specify the number of pixels contains within each line on the display.	RW	0x000

Table 10-168. Register Call Summary for Register DISPC_SIZE_TV

Display Controller

- DISPC Timing and TV Format Settings: [0] [1] [2] [3] [4]
- DISPC Shadow Registers: [5]
- DISPC TV Output Configuration: [6] [7]
- DISPC Register Summary: [8]
- DISPC Register Description: [9]

Table 10-169. DISPC_SIZE_LCD1

Address Offset	0x0000 007C		
Physical Address	0x5800 107C	**Instance**	DISPC
Description	The register configures the panel size (horizontal and vertical). Shadow register, updated on VFP start period of primary LCD. A delta value is used to indicate if the odd field has same vertical size as the even field or +/- one line.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				LPP												DELTA_LPP		RESERVED		PPL											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
27:16	LPP	Lines per panel encoded value (from 1 to 4096) to specify the number of lines per panel (program to value minus 1).	RW	0x000
15:14	DELTA_LPP	Indicates the delta size value of the odd field compared to the even field 0x0: Same size 0x1: Odd size = Even size +1 0x2: Odd size = Even Size -1	RW	0x0
13:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:0	PPL	Pixels per line encoded value (from 1 to 4096) to specify the number of pixels contains within each line on the display (program to value minus 1). In STALL mode, any value is valid. In non STALL mode, only values multiple of 8 pixels are valid.	RW	0x000

Table 10-170. Register Call Summary for Register DISPC_SIZE_LCD1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1] [2]
- DISPC Register Summary: [3]
- DISPC Register Description: [4]

Table 10-171. DISPC_GFX_BA_j

Address Offset	0x0000 0080 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1080 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the base address of the graphics buffer displayed in the graphics window (0 and 1 :for ping-pong mechanism with external trigger, based on the field polarity, 0 only used when graphics pipeline on the LCD output and 0 and 1 when on the TV output). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

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Bits	Field Name	Description	Type	Reset
31:0	BA	Graphics base address Base address of the graphics buffer (aligned on pixel size boundary) (in case 1-, 2-, and 4-bpp, byte alignment is required, in case of RGB24 packed format, 4-pixel alignment is required) When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-172. Register Call Summary for Register DISPC_GFX_BA_j

Display Controller

- DISPC: [0]
- DISPC Immediate Base Address Flip Mechanism: [1]
- DISPC Rotation and Mirroring: [2] [3] [4] [5]
- DISPC Shadow Registers: [6]
- DISPC DMA Configuration: [7]
- DISPC Register Summary: [8]

Table 10-173. DISPC_GFX_POSITION

Address Offset	0x0000 0088		
Physical Address	0x5800 1088	**Instance**	DISPC
Description	The register configures the position of the graphics window. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	POSY	Y position of the graphics window. Encoded value (from 0 to 2047) to specify the Y position of the graphics window on the screen. The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	POSX	X position of the graphics window. Encoded value (from 0 to 2047) to specify the X position of the graphics window on the screen. The first pixel on the left of the screen has the X-position 0.	RW	0x000

Table 10-174. Register Call Summary for Register DISPC_GFX_POSITION

Display Controller

- DISPC Priority Rule: [0]
- DISPC Extended 3D Support - Line Alternative Format: [1]
- DISPC Extended 3D Support - Frame Packing Format Format: [2]
- DISPC Shadow Registers: [3]
- DISPC GFX Pipeline Configuration: [4] [5]
- DISPC Register Summary: [6]

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Table 10-175. DISPC_GFX_SIZE

Address Offset	0x0000 008C		
Physical Address	0x5800 108C	**Instance**	DISPC
Description	The register configures the size of the graphics window. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZEY								RESERVED				SIZEX											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
27:16	SIZEY	Number of lines of the graphics window. Encoded value (from 1 to 4096) to specify the number of lines of the graphics window (program to value minus 1).	RW	0x000
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
11:0	SIZEX	Number of pixels of the graphics window. Encoded value (from 1 to 4096) to specify the number of pixels per line of the graphics window (program to value minus 1).	RW	0x000

Table 10-176. Register Call Summary for Register DISPC_GFX_SIZE

Display Controller

- DISPC: [0]
- DISPC Priority Rule: [1] [2]
- DISPC Shadow Registers: [3]
- DISPC GFX Pipeline Configuration: [4] [5]
- DISPC Register Summary: [6]

Table 10-177. DISPC_GFX_ATTRIBUTES

Address Offset	0x0000 00A0		
Physical Address	0x5800 10A0	**Instance**	DISPC
Description	The register configures the graphics attributes. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNELOUT2		BURSTTYPE	PREMULTIPLYALPHA	ZORDER		ZORDERENABLE	ANTIFLICKER	RESERVED			SUBSAMPLINGPATTERN			SELFREFRESHAUTO	FORCE1DTILEDMODE	SELFREFRESH	ARBITRATION	ROTATION		BUFPRELOAD	FRAMEPACKINGMODE	NIBBLEMODE	CHANNELOUT	BURSTSIZE		REPLICATIONENABLE	FORMAT				ENABLE

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Bits	Field Name	Description	Type	Reset
31:30	CHANNELOUT2	It is not used if CHANNELOUT is set to TV. Reserved when CHANNELOUT = 1 (should set to zero) wr: immediate 0x0: Primary LCD output selected. 0x1: Secondary LCD output selected. 0x2: Third LCD output selected. 0x3: Write-back output to the memory selected.	RW	0x0
29	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. (It does not apply to the palette loading OCP requests using INCR burst only) 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0
28	PREMULTIPLYALPHA	The field configures the DISPC GFX to process incoming data as premultiplied alpha data or non premultiplied alpha data. Default setting is non premultiplied alpha data. 0x0: Non premultiplyalpha data color component 0x1: Premultiplyalpha data color component	RW	0
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the ZORDER bit field is ignored and replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3 0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3	RW	0x0
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is only used when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit field ZORDER (bits 26 and 27).	RW	0
24	ANTIFLICKER	Antiflicker filtering using a 3-tap filter with hardcoded coefficients (1/4, 1/2, 1/4) 0x0: Antiflicker disabled. 0x1: Antiflicker enabled.	RW	0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
20:18	SUBSAMPLINGPATTERN	Subsampling pattern setting.	RW	0x0
17	SELFREFRESHAUTO	Automatic self-refresh mode 0x0: The transition from Selfrefresh disabled to enabled is controlled by software 0x1: The transition from Selfrefresh disabled to enabled is controlled only by hardware	RW	0
16	FORCE1DTILEDMODE	Force TILED regions access to 1D or 2D. 0x0: 2D accesses for tiled regions 0x1: 1D accesses for tiled regions	RW	0x0

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Bits	Field Name	Description	Type	Reset
15	SELFREFRESH	Enables the self refresh of the graphics window from its own DMA buffer. This bit should be set only after having set the GO bit of the channel and read back a zero in its field. 0x0: The graphics pipeline accesses the interconnect to fetch data from the system memory. 0x1: The graphics pipeline does not need anymore to fetch data from memory. Only the graphics DMA buffer is used. It takes effect after the frame has been loaded in the DMA buffer.	RW	0
14	ARBITRATION	Determines the priority of the graphics pipeline. When the graphics pipeline is one of the high priority pipelines. The arbitration wheel gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The graphics pipeline is one of the normal priority pipeline. 0x1: The graphics pipeline is one of the high priority pipeline.	RW	0
13:12	ROTATION	Graphics rotation flag 0x0: No rotation 0x1: Rotation by 90 degrees 0x3: Rotation by 270 degrees 0x2: Rotation by 180 degrees	RW	0x0
11	BUFPRELOAD	Graphics preload value 0x0: Hardware prefetches pixels up to the preload value defined in the preload register 0x1: Hardware prefetches pixels up to high threshold value	RW	0
10	FRAMEPACKINGMODE	Frame packing mode control. 0x0: Frame Packing mode is disabled 0x1: Nibble mode is enabled	RW	0x0
9	NIBBLEMODE	Graphics nibble mode (only for 1-, 2- and 4 bpp) 0x0: Nibble mode is disabled 0x1: Nibble mode is enabled	RW	0
8	CHANNELOUT	Graphics Channel Out configuration: LCD, WB or TV. wr: immediate 0x0: LCD output or WB to the memory selected. bit fields 31 and 30 defines the output associated (primary, secondary or write-back). 0x1: TV output selected	RW	0
7:6	BURSTSIZE	Graphics DMA burst size 0x0: 2 × 128-bit bursts 0x1: 4 × 128-bit bursts 0x3: Reserved 0x2: 8 × 128-bit bursts	RW	0x2
5	REPLICATIONENABLE	Graphics replication enabled: RGB . ARGB, and RGBA formats are converted into ARGB32-8888 using replication of the MSBs or 0s 0x0: Disable graphics replication logic. The conversion to ARGB32-8888 is done by adding 0s for the LSBs 0x1: Enable graphics replication logic. The conversion to ARGB32-8888 is done by duplicating the MSBs for the LSBs	RW	1

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Bits	Field Name	Description	Type	Reset
4:1	FORMAT	Graphics format. It defines the pixel format when fetching the graphics picture into memory. 0x6: RGB16-565 0xA: RGBx12-4444 0x7: ARGB16-1555 0xD: RGBA32-8888 0x8: xRGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: RGBA12-4444 0x4: xRGB12-4444 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x3: BGRA32-8888 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	Graphics enable 0x0: Graphics disabled (graphics pipeline inactive and graphics window not present) 0x1: Graphics enabled (graphics pipeline active and graphics window present on the screen)	RW	0

Table 10-178. Register Call Summary for Register DISPC_GFX_ATTRIBUTES

Display Controller

- DISPC: [0] [1] [2] [3]
- DISPC Arbitration: [4]
- DISPC DMA Ultralow-Power Mode: [5] [6]
- DISPC Memory Format: [7]
- DISPC Graphics Pipeline: [8] [9] [10] [11] [12] [13]
- DISPC Replication Logic: [14] [15]
- DISPC Antiflicker Filter: [16]
- DISPC Overlay Manager: [17] [18]
- DISPC Priority Rule: [19] [20] [21]
- DISPC Alpha Blender: [22]
- DISPC Extended 3D Support - Frame Packing Format Format: [23]
- DISPC Extended 3D Support - DLP 3D Format: [24]
- DISPC Shadow Registers: [25]
- DISPC DMA Configuration: [26] [27] [28] [29] [30] [31]
- DISPC GFX Pipeline Configuration: [32] [33] [34] [35] [36] [37] [38] [39] [40] [41]
- DISPC Register Summary: [42]
- DISPC Register Description: [43]

Table 10-179. DISPC_GFX_BUF_THRESHOLD

Address Offset	0x0000 00A4		
Physical Address	0x5800 10A4	**Instance**	DISPC
Description	The register configures the graphics buffer. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	DMA buffer high threshold number of 128 bits defining the threshold value	RW	0x04FF
15:0	BUFLOWTHRESHOLD	DMA buffer low threshold number of 128bits defining the threshold value. The value put is this register must always be greater than zero.	RW	0x04F8

Table 10-180. Register Call Summary for Register DISPC_GFX_BUF_THRESHOLD

Display Controller

- DISPC READ DMA Buffers (GFX and VID Pipelines): [0] [1] [2]
- DISPC Shadow Registers: [3]
- DISPC DMA Configuration: [4] [5]
- DISPC Register Summary: [6]

Table 10-181. DISPC_GFX_BUF_SIZE_STATUS

Address Offset	0x0000 00A8		
Physical Address	0x5800 10A8	**Instance**	DISPC
Description	The register defines the Graphics buffer size		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	DMA buffer size in number of 128 bits	R	0x0500

Table 10-182. Register Call Summary for Register DISPC_GFX_BUF_SIZE_STATUS

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-183. DISPC_GFX_ROW_INC

Address Offset	0x0000 00AC		
Physical Address	0x5800 10AC	**Instance**	DISPC
Description	The register configures the number of bytes to increment at the end of the row. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

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Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded unsigned value to specify the number of bytes to increment at the end of the row in the graphics buffer. The value 0 is invalid. The value 1 means next pixel. The value 1+n*bpp means increment of n pixels. The value 1-(n+1)*bpp means decrement of n pixels.	RW	0x0000 0001

Table 10-184. Register Call Summary for Register DISPC_GFX_ROW_INC

Display Controller
- DISPC: [0] [1]
- DISPC Predecimation: [2]
- DISPC Rotation and Mirroring: [3] [4] [5] [6]
- DISPC Shadow Registers: [7]
- DISPC DMA Configuration: [8]
- DISPC Register Summary: [9]

Table 10-185. DISPC_GFX_PIXEL_INC

Address Offset	0x0000 00B0		
Physical Address	0x5800 10B0	**Instance**	DISPC
Description	The register configures the number of bytes to increment between two pixels. For more information, see Section 10.2.4.6.5, *Predecimation*. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Number of bytes to increment between two pixels. Encoded unsigned value (from 1 to 255) to specify the number of bytes between two pixels in the graphics buffer. The value 0 is invalid. The value 1 means next pixel. The value 1+n*bpp means increment of n pixels.	RW	0x01

Table 10-186. Register Call Summary for Register DISPC_GFX_PIXEL_INC

Display Controller
- DISPC: [0]
- DISPC Predecimation: [1]
- DISPC Rotation and Mirroring: [2] [3] [4] [5]
- DISPC Shadow Registers: [6]
- DISPC DMA Configuration: [7]
- DISPC Register Summary: [8]

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Table 10-187. DISPC_GFX_TABLE_BA

Address Offset	0x0000 00B8		
Physical Address	0x5800 10B8	**Instance**	DISPC
Description	The register configures the base address of the palette buffer or the gamma table buffer. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEBA																															

Bits	Field Name	Description	Type	Reset
31:0	TABLEBA	Base address of the palette/gamma table buffer (24-bit entries in 32-bit containers, aligned on 32-bit boundary).	RW	0x0000 0000

Table 10-188. Register Call Summary for Register DISPC_GFX_TABLE_BA

Display Controller

- DISPC Color Look-Up Table (CLUT): [0]
- DISPC Shadow Registers: [1]
- DISPC GFX Pipeline Configuration: [2]
- DISPC Register Summary: [3]

Table 10-189. DISPC_VID1_BA_j

Address Offset	0x0000 00BC + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 10BC + (0x4 * j)	**Instance**	DISPC
Description	The register configures the base address of the video buffer for the video window 1 (DISPC_VID1_BA_0 and DISPC_VID1_BA_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID1_BA_0 is used). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address Base address of the video buffer (aligned on pixel size boundary except in case of RGB24 packed format, 4-pixel alignment is required; in case of YUV4:2:2, 2-pixel alignment is required, and YUV4:2:0, byte alignment is supported)). It case of YUV4:2:0 format, it indicates the base address of the Y buffer. When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

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Table 10-190. Register Call Summary for Register DISPC_VID1_BA_j

Display Controller

- DISPC Immediate Base Address Flip Mechanism: [0]
- DISPC Shadow Registers: [1]
- DISPC Logical Register Mapping: [2]
- DISPC Register Summary: [3]

Table 10-191. DISPC_VID1_POSITION

Address Offset	0x0000 00C4		
Physical Address	0x5800 10C4	**Instance**	DISPC
Description	The register configures the position of the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	POSY	Y position of the video window 1 Encoded value (from 0 to 2047) to specify the Y position of the video window 1 .The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	POSX	X position of the video window 1 Encoded value (from 0 to 2047) to specify the X position of the video window 1. The first pixel on the left of the display screen has the X-position 0.	RW	0x000

Table 10-192. Register Call Summary for Register DISPC_VID1_POSITION

Display Controller

- DISPC Extended 3D Support - Line Alternative Format: [0]
- DISPC Extended 3D Support - Frame Packing Format Format: [1]
- DISPC Shadow Registers: [2]
- DISPC Logical Register Mapping: [3]
- DISPC Register Summary: [4]

Table 10-193. DISPC_VID1_SIZE

Address Offset	0x0000 00C8		
Physical Address	0x5800 10C8	**Instance**	DISPC
Description	The register configures the size of the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD, orEVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZEY								RESERVED								SIZEX							

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
27:16	SIZEY	Number of lines of the video 1 Encoded value (from 1 to 4096) to specify the number of lines of the video window 1. Program to value minus 1.	RW	0x000
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
11:0	SIZEX	Number of pixels of the video window 1 Encoded value (from 1 to 4096) to specify the number of pixels of the video window 1. Program to value minus 1.	RW	0x000

Table 10-194. Register Call Summary for Register DISPC_VID1_SIZE

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-195. DISPC_VID1_ATTRIBUTES

Address Offset	0x0000 00CC		
Physical Address	0x5800 10CC	**Instance**	DISPC
Description	The register configures the attributes of the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31 30	29	28	27 26	25	24	23	22	21	20	19	18	17	16	15 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNELOUT2	BURSTTYPE	PREMULTIPHYALPHA	ZORDER	ZORDERENABLE	SELFREFRESH	ARBITRATION	DOUBLESTRIDE	VERTICALTAPS	FORCE1DTILEDMODE	BUFPRELOAD	RESERVED	SELFREFRESHAUTO	CHANNELOUT	BURSTSIZE	ROTATION	FULLRANGE	REPLICATIONENABLE	COLORCONVENABLE	FRAMEPACKINGMODE	HRESIZECONF	RESIZEENABLE	FORMAT					ENABLE

Bits	Field Name	Description	Type	Reset
31:30	CHANNELOUT2	It is not used if CHANNELOUT is set to TV. Reserved when CHANNELOUT = 1 (should be set to zero) wr: immediate 0x0: Primary LCD output selected. 0x1: Secondary LCD output selected. 0x2: Third LCD output selected. 0x3: Write-back output to the memory selected.	RW	0x0
29	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0

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Bits	Field Name	Description	Type	Reset
28	PREMULTIPHYALPHA	The field configures the DISPC VID1 to process incoming data as premultiplied alpha data or non premultiplied alpha data. Default setting is non premultiplied alpha data. 0x0: Non premultiplyalpha data color component 0x1: Premultiplyalpha data color component	RW	0
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the ZORDER bit field is ignored and replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3 0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3	RW	0x0
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is only used when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit field ZORDER (bits 26 and 27).	RW	0
24	SELFREFRESH	Enables the self refresh of the video window from its own DMA buffer only. 0x0: The video pipeline accesses the interconnect to fetch data from the system memory. 0x1: The video pipeline does not need anymore to fetch data from memory. Only the DMA buffer associated with the video1 is used. It takes effect after the frame has been loaded in the DMA buffer.	RW	0
23	ARBITRATION	Determines the priority of the video pipeline. The video pipeline is one of the high priority pipeline. The arbitration gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The video pipeline is one of the normal priority pipeline. 0x1: The video pipeline is one of the high priority pipeline.	RW	0
22	DOUBLESTRIDE	Determines if the stride for CbCr buffer is the 1x or 2x of the Y buffer stride. It is only used in case of YUV4:2:0. 0x0: The CbCr stride value is equal to the Y stride. 0x1: The CbCr stride value is double to the Y stride.	RW	0
21	VERTICALTAPS	Video vertical resize tap number. The vertical polyphase filter can be configured in 3-tap or 5-tap configuration. According to the number of taps, the maximum input picture width is double while using 3-tap compared to 5-tap. 0x0: 3 taps are used for the vertical filtering logic. The 2 other taps are not used. The associated bit fields for the 2 other taps coefficients do not need to be initialized. 0x1: 5 taps are used for the vertical filtering logic.	RW	0
20	FORCE1DTILEDMODE	Force TILED regions access to 1D or 2D. 0x0: 2D accesses for tiled regions 0x1: 1D accesses for tiled regions	RW	0

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Bits	Field Name	Description	Type	Reset
19	BUFPRELOAD	Video Preload Value 0x0: Hardware prefetches pixels up to the preload value defined in the preload register 0x1: Hardware prefetches pixels up to high threshold value	RW	0
18	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
17	SELFREFRESHAUTO	Automatic self-refresh mode 0x0: The transition from SELFREFRESH disabled to enabled is controlled by SW. 0x1: The transition from SELFREFRESH disabled to enabled is controlled only by hardware.	RW	0
16	CHANNELOUT	Video channel out configuration: LCD, WB or TV. wr: immediate 0x0: LCD output or WB to the memory selected. bit fields 31 and 30 defines the output associated (primary, secondary or write-back). 0x1: TV output selected	RW	0
15:14	BURSTSIZE	Video DMA burst size 0x0: 2x128bit bursts 0x1: 4x128bit bursts 0x3: Reserved 0x2: 8x128bit bursts	RW	0x2
13:12	ROTATION	Video rotation flag 0x0: No rotation 0x1: Rotation by 90 degrees 0x3: Rotation by 270 degrees 0x2: Rotation by 180 degrees	RW	0x0
11	FULLRANGE	Color space conversion full range setting. 0x0: Limited range selected: 16 subtracted from Y before color space conversion 0x1: Full range selected: Y is not modified before the color space conversion	RW	0
10	REPLICATIONENABLE	Replication enable 0x0: Disable Video replication logic 0x1: Enable Video replication logic	RW	1
9	COLORCONVENABLE	Enable the color space conversion. The hardware does not enable/disable the conversion based on the pixel format. The bit field shall be reset when the format is not YUV. 0x0: Disable Color Space Conversion YUV to RGB 0x1: Enable Color Space Conversion YUV to RGB	RW	0
8	FRAMEPACKINGMODE	Frame packing mode control. 0x0: Frame Packing mode is disabled 0x1: Nibble mode is enabled	RW	0
7	HRESIZECONF	Write 0s for future compatibility. Reads return 0.	R	0
6:5	RESIZEENABLE	Video Resize Enable 0x0: Disable both horizontal and vertical resize processing 0x1: Enable the horizontal resize processing 0x3: Enable both horizontal and vertical resize processing 0x2: Enable the vertical resize processing	RW	0x0

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Bits	Field Name	Description	Type	Reset
4:1	FORMAT	Video Format. It defines the pixel format when fetching the video 1 picture into memory. 0x6: RGB16-565 0x1: RGB12x-4444 0xA: YUV2 4:2:2 co-sited 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: NV12 4:2:0 2 buffers (Y + UV) 0x2: RGBA12-4444 0x8: xRGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: UYVY 4:2:2 co-sited 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x4: xRGB12-4444 0x3: BGRA32-8888 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	Video Enable 0x0: Video disabled (video pipeline inactive and window not present) 0x1: Video enabled (video pipeline active and window present on the screen)	RW	0

Table 10-196. Register Call Summary for Register DISPC_VID1_ATTRIBUTES

Display Controller

- DISPC Alpha Blender: [0]
- DISPC Extended 3D Support - Frame Packing Format Format: [1]
- DISPC Shadow Registers: [2]
- DISPC Logical Register Mapping: [3]
- DISPC Register Summary: [4]
- DISPC Register Description: [5] [6] [7]

Table 10-197. DISPC_VID1_BUF_THRESHOLD

Address Offset	0x0000 00D0		
Physical Address	0x5800 10D0	**Instance**	DISPC
Description	The register configures the video buffer associated with the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

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Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	Video DMA buffer high threshold number of 128 bits defining the threshold value	RW	0x07FF
15:0	BUFLOWTHRESHOLD	DMA buffer low threshold number of 128 bits defining the threshold value	RW	0x07F8

Table 10-198. Register Call Summary for Register DISPC_VID1_BUF_THRESHOLD

Display Controller
- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-199. DISPC_VID1_BUF_SIZE_STATUS

Address Offset	0x0000 00D4		
Physical Address	0x5800 10D4	**Instance**	DISPC
Description	The register defines the Video buffer size for the video pipeline 1.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	Video 1 DMA buffer size in number of 128-bits	R	0x0800

Table 10-200. Register Call Summary for Register DISPC_VID1_BUF_SIZE_STATUS

Display Controller
- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-201. DISPC_VID1_ROW_INC

Address Offset	0x0000 00D8		
Physical Address	0x5800 10D8	**Instance**	DISPC
Description	The register configures the number of bytes to increment at the end of the row for the buffer associated with the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded signed value (from 2^{31}1 to 2^{31}) to specify the number of bytes to increment at the end of the row in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n * bpp means increment of n pixels. The value 1 (n + 1)* bpp means decrement of n pixels.	RW	0x0000 0001

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Table 10-202. Register Call Summary for Register DISPC_VID1_ROW_INC

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-203. DISPC_VID1_PIXEL_INC

Address Offset	0x0000 00DC		
Physical Address	0x5800 10DC	**Instance**	DISPC
Description	The register configures the number of bytes to increment between two pixels for the buffer associated with the video window 2. For more information, see Section 10.2.4.6.5, *Predecimation*.The register is used only when the TILER is not present in the system in order to perform low performance rotation. When the TILER IP is present it is highly recommended to use it for performing the rotation. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD orEVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Number of bytes to increment between two pixels. Encoded unsigned value (from 1 to 255) to specify the number of bytes between two pixels in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n * bpp means increment of n pixels. For YUV4:2:0, maximum supported value is 128.	RW	0x01

Table 10-204. Register Call Summary for Register DISPC_VID1_PIXEL_INC

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-205. DISPC_VID1_FIR

Address Offset	0x0000 00E0		
Physical Address	0x5800 10E0	**Instance**	DISPC
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 1. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			FIRVINC													RESERVED			FIRHINC												

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-206. Register Call Summary for Register DISPC_VID1_FIR

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-207. DISPC_VID1_PICTURE_SIZE

Address Offset	0x0000 00E4		
Physical Address	0x5800 10E4	**Instance**	DISPC
Description	The register configures the size of the video picture associated with the video layer 1 before up/down-scaling. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD, EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MEMSIZEY												RESERVED					MEMSIZEX											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:16	MEMSIZEY	Number of lines of the video picture. Encoded value (from 1 to 4096) to specify the number of lines of the video picture in memory (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded to 2^{11}.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	MEMSIZEX	Number of pixels of the video picture Encoded value (from 1 to 2048) to specify the number of pixels of the video picture in memory (program to value minus 1). The size is limited to the size of the line buffer of the vertical sampling block in case the video picture is processed by the vertical filtering unit. (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded to 2^{11}.	RW	0x000

Table 10-208. Register Call Summary for Register DISPC_VID1_PICTURE_SIZE

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-209. DISPC_VID1_ACCU_j

Address Offset	0x0000 00E8 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 10E8 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 1 (DISPC_VID1_ACCU_0 and DISPC_VID1_ACCU_1 for ping-pong mechanism with external trigger, based on the field polarity) It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accumulator value encoded value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accumulator value encoded value (from –1024 to 1023).	RW	0x000

Table 10-210. Register Call Summary for Register DISPC_VID1_ACCU_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-211. DISPC_VID1_FIR_COEF_H_i

Address Offset	0x0000 00F0 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 10F0 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VPF start pertiod of the third LCD, EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

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Table 10-212. Register Call Summary for Register DISPC_VID1_FIR_COEF_H_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-213. DISPC_VID1_FIR_COEF_HV_i

Address Offset	0x0000 00F4 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 10F4 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-214. Register Call Summary for Register DISPC_VID1_FIR_COEF_HV_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-215. DISPC_VID1_CONV_COEF0

Address Offset	0x0000 0130		
Physical Address	0x5800 1130	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RCR								RESERVED								RY							

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	RCR	RCr coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RY	RY coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-216. Register Call Summary for Register DISPC_VID1_CONV_COEF0

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-217. DISPC_VID1_CONV_COEF1

Address Offset	0x0000 0134		
Physical Address	0x5800 1134	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GY								RESERVED								RCB							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GY	GY coefficient encoded signed value (from -1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RCB	RCb coefficient encoded signed value (from -1024 to 1023).	RW	0x000

Table 10-218. Register Call Summary for Register DISPC_VID1_CONV_COEF1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-219. DISPC_VID1_CONV_COEF2

Address Offset	0x0000 0138		
Physical Address	0x5800 1138	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GCB								RESERVED								GCR							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GCB	GCb coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	GCR	GCr coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-220. Register Call Summary for Register DISPC_VID1_CONV_COEF2

Display Controller
- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-221. DISPC_VID1_CONV_COEF3

Address Offset	0x0000 013C		
Physical Address	0x5800 113C	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BCR								RESERVED								BY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	BCR	BCr coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	BY	BY coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-222. Register Call Summary for Register DISPC_VID1_CONV_COEF3

Display Controller
- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-223. DISPC_VID1_CONV_COEF4

Address Offset	0x0000 0140		
Physical Address	0x5800 1140	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					BCB										

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	BCB	BCb coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-224. Register Call Summary for Register DISPC_VID1_CONV_COEF4

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-225. DISPC_VID2_BA_j

Address Offset	0x0000 014C + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 114C + (0x4 * j)	**Instance**	DISPC
Description	The register configures the base address of the video buffer for the video window 2 (DISPC_VID2_BA_0 and DISPC_VID2_BA_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID2_BA_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address Base address of the video buffer (aligned on pixel size boundary except in case of RGB24 packed format, 4-pixel alignment is required; in case of YUV4:2:2, 2-pixel alignment is required, and YUV4:2:0, byte alignment is supported)). In case of YUV4:2:0 format, it indicates the base address of the Y buffer. When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

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Table 10-226. Register Call Summary for Register DISPC_VID2_BA_j

Display Controller

- DISPC Immediate Base Address Flip Mechanism: [0]
- DISPC Shadow Registers: [1]
- DISPC Logical Register Mapping: [2]
- DISPC Register Summary: [3]

Table 10-227. DISPC_VID2_POSITION

Address Offset	0x0000 0154		
Physical Address	0x5800 1154	**Instance**	DISPC
Description	The register configures the position of the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	POSY	Y position of the video window 2 encoded value (from 0 to 2047) to specify the Y position of the video window 2 .The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	POSX	X position of the video window 2 encoded value (from 0 to 2047) to specify the X position of the video window 2. The first pixel on the left of the display screen has the X-position 0.	RW	0x000

Table 10-228. Register Call Summary for Register DISPC_VID2_POSITION

Display Controller

- DISPC Extended 3D Support - Line Alternative Format: [0]
- DISPC Extended 3D Support - Frame Packing Format Format: [1]
- DISPC Shadow Registers: [2]
- DISPC Logical Register Mapping: [3]
- DISPC Register Summary: [4]

Table 10-229. DISPC_VID2_SIZE

Address Offset	0x0000 0158		
Physical Address	0x5800 1158	**Instance**	DISPC
Description	The register configures the size of the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZEY								RESERVED								SIZEX							

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
27:16	SIZEY	Number of lines of the video 2 encoded value (from 1 to 4096) to specify the number of lines of the video window 2. Program to value minus 1.	RW	0x000
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
11:0	SIZEX	Number of pixels of the video window 2 encoded value (from 1 to 4096) to specify the number of pixels of the video window 2. Program to value minus 1.	RW	0x000

Table 10-230. Register Call Summary for Register DISPC_VID2_SIZE

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-231. DISPC_VID2_ATTRIBUTES

Address Offset	0x0000 015C		
Physical Address	0x5800 115C	**Instance**	DISPC
Description	The register configures the attributes of the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31 30	29	28	27 26	25	24	23	22	21	20	19	18	17	16	15 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNELOUT2	BURSTTYPE	PREMULTIPLYALPHA	ZORDER	ZORDERENABLE	SELFREFFRESH	ARBITRATION	DOUBLESTRIDE	VERTICALTAPS	FORCE1DTILEDMODE	BUFPRELOAD	RESERVED	SELFREFRESHAUTO	CHANNELOUT	BURSTSIZE	ROTATION	FULLRANGE	REPLICATIONENABLE	COLORCONVENABLE	FRAMEPACKINGMODE	HRESIZECONF	RESIZEENABLE	FORMAT					ENABLE

Bits	Field Name	Description	Type	Reset
31:30	CHANNELOUT2	It is not used if CHANNELOUT is set to TV. Reserved when CHANNELOUT = 1 (must be set to zero) wr: immediate 0x0: Primary LCD output selected. 0x1: Secondary LCD output selected. 0x2: Third LCD output selected. 0x3: Write-back output to the memory selected.	RW	0x0
29	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0

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Bits	Field Name	Description	Type	Reset
28	PREMULTIPLYALPHA	The field configures the DISPC VID2 to process incoming data as premultiplied alpha data or non premultiplied alpha data. Default setting is non premultiplied alpha data. 0x0: Non premultiplyalpha data color component 0x1: Premultiplyalpha data color component	RW	0
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the ZORDER bit field is ignored and replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3 0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3	RW	0x0
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is only used when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit field ZORDER (bits 26 and 27).	RW	0
24	SELFREFRESH	Enables the self refresh of the video window from its own DMA buffer only. 0x0: The video pipeline accesses the interconnect to fetch data from the system memory. 0x1: The video pipeline does not need anymore to fetch data from memory. Only the DMA buffer associated with the video2 is used. It takes effect after the frame has been loaded in the DMA buffer.	RW	0
23	ARBITRATION	Determines the priority of the video pipeline. The video pipeline is one of the high priority pipeline. The arbitration gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The video pipeline is one of the normal priority pipeline. 0x1: The video pipeline is one of the high priority pipeline.	RW	0
22	DOUBLESTRIDE	Determines if the stride for CbCr buffer is the 1x or 2x of the Y buffer stride. It is only used in case of YUV4:2:0. 0x0: The CbCr stride value is equal to the Y stride. 0x1: The CbCr stride value is double to the Y stride.	RW	0
21	VERTICALTAPS	Video Vertical Resize Tap Number 0x0: 3 taps are used for the vertical filtering logic. The 2 other taps are not used. The associated bit fields for the 2 other taps coefficients do not need to be initialized. 0x1: 5 taps are used for the vertical filtering logic.	RW	0
20	FORCE1DTILEDMODE	Force TILED regions access to 1D or 2D. 0x0: 2D accesses for tiled regions 0x1: 1D accesses for tiled regions	RW	0

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Bits	Field Name	Description	Type	Reset
19	BUFPRELOAD	Video Preload Value 0x0: Hardware prefetches pixels up to the preload value defined in the preload register 0x1: Hardware prefetches pixels up to high threshold value	RW	0
18	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
17	SELFREFRESHAUTO	Automatic self-refresh mode 0x0: The transition from SELFREFRESH disabled to enabled is controlled by SW. 0x1: The transition from SELFREFRESH disabled to enabled is controlled only by hardware.	RW	0
16	CHANNELOUT	Video Channel Out configuration: LCD, WB or TV. wr: immediate 0x0: LCD output or WB to the memory selected. bit fields 31 and 30 defines the output associated (primary, secondary or write-back). 0x1: TV output selected	RW	0
15:14	BURSTSIZE	Video DMA burst size 0x0: 2 × 128-bit bursts 0x1: 4 × 128-bit bursts 0x3: Reserved 0x2: 8 × 128-bit bursts	RW	0x2
13:12	ROTATION	Video Rotation Flag 0x0: No rotation 0x1: Rotation by 90 degrees 0x3: Rotation by 270 degrees 0x2: Rotation by 180 degrees	RW	0x0
11	FULLRANGE	Color space conversion full range setting. 0x0: Limited range selected: 16 subtracted from Y before color space conversion 0x1: Full range selected: Y is not modified before the color space conversion	RW	0
10	REPLICATIONENABLE	Replication Enable 0x0: Disable Video replication logic 0x1: Enable Video replication logic	RW	1
9	COLORCONVENABLE	Enable the color space conversion. The hardware does not enable/disable the conversion based on the pixel format. The bit field shall be reset when the format is not YUV. 0x0: Disable color space conversion YUV to RGB 0x1: Enable color space conversion YUV to RGB	RW	0
8	FRAMEPACKINGMODE	Frame packing mode control. 0x0: Frame Packing mode is disabled 0x1: Nibble mode is enabled	RW	0
7	HRESIZECONF	Write 0s for future compatibility. Reads return 0.	R	0
6:5	RESIZEENABLE	Video Resize Enable 0x0: Disable both horizontal and vertical resize processing 0x1: Enable the horizontal resize processing 0x3: Enable both horizontal and vertical resize processing 0x2: Enable the vertical resize processing	RW	0x0

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Bits	Field Name	Description	Type	Reset
4:1	FORMAT	Video Format. It defines the pixel format when fetching the video 2 picture into memory. 0x6: RGB16-565 0x1: RGB12x-4444 0xA: YUV2 4:2:2 co-sited 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: NV12 4:2:0 2 buffers (Y + UV) 0x2: RGBA12-4444 0x8: xRGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: UYVY 4:2:2 co-sited 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x4: xRGB12-4444 0x3: BGRA32-8888 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	VidEnable 0x0: Video disabled (video pipeline inactive and window not present) 0x1: Video enabled (video pipeline active and window present on the screen)	RW	0

Table 10-232. Register Call Summary for Register DISPC_VID2_ATTRIBUTES

Display Controller

- DISPC Alpha Blender: [0]
- DISPC Extended 3D Support - Frame Packing Format Format: [1]
- DISPC Shadow Registers: [2]
- DISPC Logical Register Mapping: [3]
- DISPC Register Summary: [4]

Table 10-233. DISPC_VID2_BUF_THRESHOLD

Address Offset	0x0000 0160		
Physical Address	0x5800 1160	**Instance**	DISPC
Description	The register configures the DMA buffer associated with the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

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Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	DMA buffer high threshold number of 128 bits defining the threshold value	RW	0x07FF
15:0	BUFLOWTHRESHOLD	DMA buffer low threshold number of 128 bits defining the threshold value	RW	0x07F8

Table 10-234. Register Call Summary for Register DISPC_VID2_BUF_THRESHOLD

Display Controller
- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-235. DISPC_VID2_BUF_SIZE_STATUS

Address Offset	0x0000 0164		
Physical Address	0x5800 1164	**Instance**	DISPC
Description	The register defines the DMA buffer size for the video pipeline 2.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	DMA buffer size in number of 128 bits	R	0x0800

Table 10-236. Register Call Summary for Register DISPC_VID2_BUF_SIZE_STATUS

Display Controller
- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-237. DISPC_VID2_ROW_INC

Address Offset	0x0000 0168		
Physical Address	0x5800 1168	**Instance**	DISPC
Description	The register configures the number of bytes to increment at the end of the row for the buffer associated with the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded signed value (from $2^{31}1$ to 2^{31}) to specify the number of bytes to increment at the end of the row in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n * bpp means increment of n pixels. The value 1 (n + 1) * bpp means decrement of n pixels.	RW	0x0000 0001

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Table 10-238. Register Call Summary for Register DISPC_VID2_ROW_INC

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-239. DISPC_VID2_PIXEL_INC

Address Offset	0x0000 016C		
Physical Address	0x5800 116C	**Instance**	DISPC
Description	The register configures the number of bytes to increment between two pixels for the buffer associated with the video window 2. For more information, see Section 10.2.4.6.5, *Predecimation*.The register is used only when the TILER is not present in the system in order to perform low performance rotation. When the TILER IP is present it is highly recommended to use it for performing the rotation. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Number of bytes to increment between two pixels. Encoded unsigned value (from 1 to 255) to specify the number of bytes between2 pixels in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n * bpp means increment of n pixels. For YUV4:2:0, maximum supported value is 128.	RW	0x01

Table 10-240. Register Call Summary for Register DISPC_VID2_PIXEL_INC

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-241. DISPC_VID2_FIR

Address Offset	0x0000 0170		
Physical Address	0x5800 1170	**Instance**	DISPC
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 2. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			FIRVINC													RESERVED		FIRHINC													

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-242. Register Call Summary for Register DISPC_VID2_FIR

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-243. DISPC_VID2_PICTURE_SIZE

Address Offset	0x0000 0174		
Physical Address	0x5800 1174	**Instance**	DISPC
Description	The register configures the size of the video picture associated with the video layer 2 before up/down-scaling. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MEMSIZEY								RESERVED								MEMSIZEX							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
27:16	MEMSIZEY	Number of lines of the video picture Encoded value (from 1 to 4096) to specify the number of lines of the video picture in memory (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the maximum size of the unpredecimated image size in memory is still bounded 2^{11}.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	MEMSIZEX	Number of pixels of the video picture Encoded value (from 1 to 2048) to specify the number of pixels of the video picture in memory (program to value minus 1). The size is limited to the size of the line buffer of the vertical sampling block in case the video picture is processed by the vertical filtering unit. (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded 2^{11}.	RW	0x000

Table 10-244. Register Call Summary for Register DISPC_VID2_PICTURE_SIZE

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-245. DISPC_VID2_ACCU_j

Address Offset	0x0000 0178 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1178 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 2 (DISPC_VID2_ACCU_0 and DISPC_VID2_ACCU_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accumulator value encoded value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accumulator value encoded value (from –1024 to 1023).	RW	0x000

Table 10-246. Register Call Summary for Register DISPC_VID2_ACCU_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1] [2]
- DISPC Register Summary: [3]

Table 10-247. DISPC_VID2_FIR_COEF_H_i

Address Offset	0x0000 0180 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1180 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

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Table 10-248. Register Call Summary for Register DISPC_VID2_FIR_COEF_H_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-249. DISPC_VID2_FIR_COEF_HV_i

Address Offset	0x0000 0184 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1184 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-250. Register Call Summary for Register DISPC_VID2_FIR_COEF_HV_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-251. DISPC_VID2_CONV_COEF0

Address Offset	0x0000 01C0		
Physical Address	0x5800 11C0	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RCR								RESERVED								RY							

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	RCR	RCr coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RY	RY coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-252. Register Call Summary for Register DISPC_VID2_CONV_COEF0

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-253. DISPC_VID2_CONV_COEF1

Address Offset	0x0000 01C4		
Physical Address	0x5800 11C4	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GY								RESERVED								RCB							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GY	GY coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RCB	RCb coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-254. Register Call Summary for Register DISPC_VID2_CONV_COEF1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-255. DISPC_VID2_CONV_COEF2

Address Offset	0x0000 01C8		
Physical Address	0x5800 11C8	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GCB								RESERVED								GCR							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GCB	GCb coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	GCR	GCr coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-256. Register Call Summary for Register DISPC_VID2_CONV_COEF2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-257. DISPC_VID2_CONV_COEF3

Address Offset	0x0000 01CC		
Physical Address	0x5800 11CC	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BCR								RESERVED								BY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	BCR	BCr coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	BY	BY coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-258. Register Call Summary for Register DISPC_VID2_CONV_COEF3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-259. DISPC_VID2_CONV_COEF4

Address Offset	0x0000 01D0		
Physical Address	0x5800 11D0	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BCB							

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	BCB	BCb coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-260. Register Call Summary for Register DISPC_VID2_CONV_COEF4

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-261. DISPC_DATA1_CYCLE1

Address Offset	0x0000 01D4		
Physical Address	0x5800 11D4	**Instance**	DISPC
Description	The control register configures the output data format for 1st cycle. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				BITALIGNMENTPIXEL2				RESERVED			NBBITSPIXEL2					RESERVED				BITALIGNMENTPIXEL1				RESERVED			NBBITSPIXEL1				

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface.	RW	0x0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface.	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0

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Bits	Field Name	Description	Type	Reset
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-262. Register Call Summary for Register DISPC_DATA1_CYCLE1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-263. DISPC_DATA1_CYCLE2

Address Offset	0x0000 01D8		
Physical Address	0x5800 11D8	**Instance**	DISPC
Description	The control register configures the output data format for 2nd cycle. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED / NBBITSPIXEL2	RESERVED / BITALIGNMENTPIXEL1	RESERVED / NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface.	RW	0x0
23:21	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface.	RW	0x0
7:5	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-264. Register Call Summary for Register DISPC_DATA1_CYCLE2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-265. DISPC_DATA1_CYCLE3

Address Offset	0x0000 01DC		
Physical Address	0x5800 11DC	**Instance**	DISPC
Description	The control register configures the output data format for 3rd cycle. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				BITALIGNMENTPIXEL2				RESERVED			NBBITSPIXEL2					RESERVED				BITALIGNMENTPIXEL1				RESERVED			NBBITSPIXEL1				

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface.	RW	0x0
23:21	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface.	RW	0x0
7:5	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-266. Register Call Summary for Register DISPC_DATA1_CYCLE3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-267. DISPC_VID1_FIR_COEF_V_i

Address Offset	0x0000 01E0 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 11E0 + (0x4 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-268. Register Call Summary for Register DISPC_VID1_FIR_COEF_V_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-269. DISPC_VID2_FIR_COEF_V_i

Address Offset	0x0000 0200 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1200 + (0x4 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-270. Register Call Summary for Register DISPC_VID2_FIR_COEF_V_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-271. DISPC_CPR1_COEF_R

Address Offset	0x0000 0220		
Physical Address	0x5800 1220	**Instance**	DISPC
Description	The register configures the color phase rotation matrix coefficients for the Red component. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RR										RESERVED		RG									RESERVED			RB							

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Bits	Field Name	Description	Type	Reset
31:22	RR	RR coefficient encoded signed value (from –512 to 511)	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	RG	RG coefficient encoded signed value (from –512 to 511)	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	RB	RB coefficient encoded signed value (from –512 to 511)	RW	0x000

Table 10-272. Register Call Summary for Register DISPC_CPR1_COEF_R

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-273. DISPC_CPR1_COEF_G

Address Offset	0x0000 0224		
Physical Address	0x5800 1224	**Instance**	DISPC
Description	The register configures the color phase rotation matrix coefficients for the Green component. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GR										RESERVED						GG					RESERVED			GB							

Bits	Field Name	Description	Type	Reset
31:22	GR	GR coefficient encoded signed value (from –512 to 511)	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	GG	GG coefficient encoded signed value (from –512 to 511)	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	GB	GB coefficient encoded signed value (from –512 to 511)	RW	0x000

Table 10-274. Register Call Summary for Register DISPC_CPR1_COEF_G

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-275. DISPC_CPR1_COEF_B

Address Offset	0x0000 0228		
Physical Address	0x5800 1228	**Instance**	DISPC
Description	The register configures the color phase rotation matrix coefficients for the Blue component. It is used for the primary LCD output. Shadow register, updated on VFP start period of primary LCD		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR										RESERVED						BG					RESERVED			BB							

Bits	Field Name	Description	Type	Reset
31:22	BR	BR coefficient encoded signed value (from –512 to 511)	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	BG	BG coefficient encoded signed value (from –512 to 511	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	BB	BB coefficient encoded signed value (from –512 to 511)	RW	0x000

Table 10-276. Register Call Summary for Register DISPC_CPR1_COEF_B

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-277. DISPC_GFX_PRELOAD

Address Offset	0x0000 022C		
Physical Address	0x5800 122C	**Instance**	DISPC
Description	The register configures the graphics DMA buffer Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRELOAD							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	PRELOAD	DMA buffer preload value number of 128-bit words defining the preload value.	RW	0x100

Table 10-278. Register Call Summary for Register DISPC_GFX_PRELOAD

Display Controller

- DISPC READ DMA Buffers (GFX and VID Pipelines): [0]
- DISPC Shadow Registers: [1]
- DISPC DMA Configuration: [2]
- DISPC Register Summary: [3]

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Table 10-279. DISPC_VID1_PRELOAD

Address Offset	0x0000 0230		
Physical Address	0x5800 1230	**Instance**	DISPC
Description	The register configures the DMA buffer of the video 1 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PRELOAD															

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	PRELOAD	DMA buffer preload value number of 128-bit words defining the preload value.	RW	0x100

Table 10-280. Register Call Summary for Register DISPC_VID1_PRELOAD

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-281. DISPC_VID2_PRELOAD

Address Offset	0x0000 0234		
Physical Address	0x5800 1234	**Instance**	DISPC
Description	The register configures the DMA buffer of the video 2 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PRELOAD															

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	PRELOAD	DMA buffer preload value Number of 128-bit words defining the preload value.	RW	0x100

Table 10-282. Register Call Summary for Register DISPC_VID2_PRELOAD

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

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Table 10-283. DISPC_CONTROL2

Address Offset	0x0000 0238		
Physical Address	0x5800 1238	**Instance**	DISPC
Description	The control register configures the Display Controller module for the secondary LCD output. Shadow registers are updated during the VFP start period of the secondary LCD, EVSYNC, or when DISPC_CONTROL2.GOWB is set to 1 by software and the current WB frame is complete (that is, has no more data in the write-back pipeline).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPATIALTEMPORALDITHERINGFRAMES		RESERVED			TDMUNUSEDBITS		TDMCYCLEFORMAT		TDMPARALLELMODE		TDMENABLE	RESERVED						TVOVERLAYOPTIMIZATION	OVERLAYOPTIMIZATION	STALLMODE	RESERVED		TFTDATALINES		STDITHERENABLE	GOWB	GOLCD	M8B	STNTFT	MONOCOLOR	RESERVED	LCDENABLE

Bits	Field Name	Description	Type	Reset
31:30	SPATIALTEMPORAL DITHERINGFRAMES	Spatial/temporal dithering number of frames for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: Spatial only 0x1: Spatial and temporal over 2 frames 0x2: Spatial and temporal over 4 frames 0x3: Reserved	RW	0x0
29:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
26:25	TDMUNUSED BITS	State of unused bits (TDM mode only) for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: Low level (0) 0x1: High level (1) 0x2: Unchanged from previous state 0x3: Reserved	RW	0x0
24:23	TDMCYCLE FORMAT	Cycle format (TDM mode only) for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: 1 cycle for 1 pixel 0x1: 2 cycles for 1 pixel 0x2: 3 cycles for 1 pixel 0x3: 3 cycles for 2 pixels	RW	0x0
22:21	TDMPARALLEL MODE	Output Interface width (TDM mode only) for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: 8-bit parallel output interface selected 0x1: 9-bit parallel output interface selected 0x2: 12-bit parallel output interface selected 0x3: 16-bit parallel output interface selected	RW	0x0

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Bits	Field Name	Description	Type	Reset
20	TDMENABLE	Enable the multiple cycle format (TDM mode only used for Active Matrix mode with the RFBI enable bit off) for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: TDM disabled 0x1: TDM enabled	RW	0
19:14	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
13	TVOVERLAY OPTIMIZATION	Overlay optimization for the TV output wr: VFP or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory 0x0: All the data for all the enabled pipelines are fetched from memory regardless of the overlay/alpha blending configuration. 0x1: The data not used by the overlay manager because of overlap between layers with no alpha blending between them shall not be fetched from memory in order to optimize the bandwidth.	RW	0
12	OVERLAY OPTIMIZATION	Overlay optimization for the secondary LCD output wr: VFP or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory 0x0: All the data for all the enabled pipelines are fetched from memory regardless of the overlay/alpha blending configuration. 0x1: The data not used by the overlay manager because of overlap between layers with no alpha blending between them shall not be fetched from memory in order to optimize the bandwidth.	RW	0
11	STALLMODE	STALL mode for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: Normal mode selected 0x1: STALL mode selected. The Display Controller sends the data without considering the VSYNC/HSYNC. The LCD output is disabled at the end of the transfer of the frame. The S/W has to re-enable the LCD output in order to generate a new frame.	RW	0
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:8	TFTDATALINES	Number of lines of the secondary LCD interface wr: VFP start period of secondary LCD output 0x0: 12-bit output aligned on the LSB of the pixel data interface 0x1: 16-bit output aligned on the LSB of the pixel data interface 0x2: 18-bit output aligned on the LSB of the pixel data interface 0x3: 24-bit output aligned on the LSB of the pixel data interface	RW	0x0
7	STDITHER ENABLE	Spatial temporal dithering enable for the secondary LCD output wr: VFP start period of secondary LCD output 0x0: Spatial/Temporal dithering logic disabled 0x1: Spatial/Temporal dithering logic enabled	RW	0

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Bits	Field Name	Description	Type	Reset
6	GOWB	GO command for the write-back output. It is used to synchronized the pipelines (graphics and/or video ones) associated with the write-back output to the memory. wr:immediate 0x0: The hardware has finished updating the internal shadow registers of the pipeline(s) connected to the write-back pipeline using the user values. The hardware resets the bit when the update is completed. 0x1: The user has finished to program the shadow registers of the pipeline(s) associated with the write-back pipeline and the hardware can update the internal registers immediately	RW	0
5	GOLCD	GO command for the secondary LCD output. It is used to synchronized the pipelines (graphics and/or video ones) associated with the secondary LCD output. wr:immediate 0x0: The hardware has finished updating the internal shadow registers of the pipeline(s) connected to the LCD output using the user values. The hardware resets the bit when the update is completed. 0x1: The user has finished to program the shadow registers of the pipeline(s) associated with the LCD output and the hardware can update the internal registers at the VFP start period	RW	0
4	M8B	Mono 8-bit mode of the secondary LCD wr: VFP start period of secondary LCD output 0x0: Reserved 0x1: Reserved	RW	0
3	STNTFT	LCD Display type of the secondary LCD wr: VFP start period of secondary LCD output 0x0: Reserved 0x1: Active or TFT display operation enabled. STN Dither logic and output FIFO bypassed.	RW	0
2	MONOCOLOR	Monochrome/Color selection for the secondary LCD wr: VFP start period of secondary LCD output 0x0: Reserved 0x1: Reserved	RW	0
1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
0	LCDENABLE	Enable the secondary LCD output wr:immediate 0x0: LCD output disabled (at the end of the frame when the bit is reset) 0x1: LCD output enabled	RW	0

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Table 10-284. Register Call Summary for Register DISPC_CONTROL2

Display Controller

- DISPC Graphics Pipeline: [0] [1]
- DISPC Video Pipelines: [2] [3]
- DISPC Overlay Optimization: [4] [5]
- DISPC Shadow Registers: [6] [7] [8] [9]
- DISPC GFX Pipeline Configuration: [10] [11]
- DISPC Video Pipeline Configuration: [12] [13]
- DISPC WB Pipeline Configuration: [14]
- DISPC LCD Output Configuration: [15] [16]
- DISPC TV Output Configuration: [17]
- DISPC Logical Register Mapping: [18]
- DISPC Register Summary: [19]
- DISPC Register Description: [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74] [75] [76] [77] [78] [79] [80] [81] [82] [83] [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95] [96] [97] [98] [99] [100] [101] [102] [103] [104] [105] [106] [107] [108] [109] [110] [111] [112] [113] [114] [115] [116] [117] [118] [119] [120] [121] [122] [123] [124] [125] [126] [127] [128] [129] [130] [131] [132] [133] [134] [135] [136] [137] [138] [139] [140] [141] [142] [143] [144] [145] [146] [147] [148] [149]

Table 10-285. DISPC_GFX_POSITION2

Address Offset	0x0000 0240		
Physical Address	0x5800 1240	**Instance**	DISPC
Description	The register configures the position of the 2nd graphics window in FramePacking mode. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2[6] GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x00
26:16	POSY	Y position of the 2nd graphics window. Encoded value (from 0 to 2047) to specify the Y position of the graphics window on the screen. The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x00
10:0	POSX	X position of the 2nd graphics window. Encoded value (from 0 to 2047) to specify the X position of the graphics window on the screen. The first pixel on the left of the screen has the X-position 0.	RW	0x000

Table 10-286. Register Call Summary for Register DISPC_GFX_POSITION2

Display Controller

- DISPC Priority Rule: [0]
- DISPC Extended 3D Support - Frame Packing Format Format: [1]
- DISPC Shadow Registers: [2]
- DISPC Register Summary: [3]

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Table 10-287. DISPC_VID1_POSITION2

Address Offset	0x0000 0244		
Physical Address	0x5800 1244	**Instance**	DISPC
Description	The register configures the position of the 2nd video window #1 in FramePacking mode. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2[6] GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					POSY											RESERVED					POSX										

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x00
26:16	POSY	Y position of the 2nd video window #1 Encoded value (from 0 to 2047) to specify the Y position of the video window #1 .The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x00
10:0	POSX	X position of the 2nd video window #1 Encoded value (from 0 to 2047) to specify the X position of the video window #1. The first pixel on the left of the display screen has the X-position 0.	RW	0x000

Table 10-288. Register Call Summary for Register DISPC_VID1_POSITION2

Display Controller

- DISPC Extended 3D Support - Frame Packing Format Format: [0]
- DISPC Shadow Registers: [1]
- DISPC Register Summary: [2]

Table 10-289. DISPC_VID2_POSITION2

Address Offset	0x0000 0248		
Physical Address	0x5800 1248	**Instance**	DISPC
Description	The register configures the position of the 2nd video window #2 in FramePacking mode. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2[6] GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					POSY											RESERVED					POSX										

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x00
26:16	POSY	Y position of the 2nd video window #2 Encoded value (from 0 to 2047) to specify the Y position of the video window #2 .The line at the top has the Y-position 0.	RW	0x000

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Bits	Field Name	Description	Type	Reset
15:11	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x00
10:0	POSX	X position of the 2nd video window #2 Encoded value (from 0 to 2047) to specify the X position of the video window #2. The first pixel on the left of the display screen has the X-position 0.	RW	0x000

Table 10-290. Register Call Summary for Register DISPC_VID2_POSITION2

Display Controller

- DISPC Extended 3D Support - Frame Packing Format Format: [0]
- DISPC Shadow Registers: [1]
- DISPC Register Summary: [2]

Table 10-291. DISPC_VID3_POSITION2

Address Offset	0x0000 024C		
Physical Address	0x5800 124C	**Instance**	DISPC
Description	The register configures the position of the 2nd video window #3 in FramePacking mode. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2[6] GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x00
26:16	POSY	Y position of the 2nd video window #2 Encoded value (from 0 to 2047) to specify the Y position of the video window #2 .The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x00
10:0	POSX	X position of the 2nd video window #2 Encoded value (from 0 to 2047) to specify the X position of the video window #2. The first pixel on the left of the display screen has the X-position 0.	RW	0x000

Table 10-292. Register Call Summary for Register DISPC_VID3_POSITION2

Display Controller

- DISPC Extended 3D Support - Frame Packing Format Format: [0]
- DISPC Shadow Registers: [1]
- DISPC Register Summary: [2]

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Table 10-293. DISPC_VID3_ACCU_j

Address Offset	0x0000 0300 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1300 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 3 (DISPC_VID3_ACCU_0 and DISPC_VID3_ACCU_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from –1024 to 1023).	RW	0x000

Table 10-294. Register Call Summary for Register DISPC_VID3_ACCU_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-295. DISPC_VID3_BA_j

Address Offset	0x0000 0308 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1308 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the base address of the video buffer for the video window 3 (DISPC_VID3_BA_0 and DISPC_VID3_BA_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID3_BA_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

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Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address Base address of the video buffer (aligned on pixel size boundary except in case of RGB24 packed format, 4-pixel alignment is required; in case of YUV4:2:2, 2-pixel alignment is required, and YUV4:2:0, byte alignment is supported)). It case of YUV4:2:0 format, it indicates the base address of the Y buffer. When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-296. Register Call Summary for Register DISPC_VID3_BA_j

Display Controller

- DISPC Immediate Base Address Flip Mechanism: [0]
- DISPC Shadow Registers: [1]
- DISPC Logical Register Mapping: [2]
- DISPC Register Summary: [3]

Table 10-297. DISPC_VID3_FIR_COEF_H_i

Address Offset	0x0000 0310 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1310 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-298. Register Call Summary for Register DISPC_VID3_FIR_COEF_H_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-299. DISPC_VID3_FIR_COEF_HV_i

Address Offset	0x0000 0314 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1314 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-300. Register Call Summary for Register DISPC_VID3_FIR_COEF_HV_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-301. DISPC_VID3_FIR_COEF_V_i

Address Offset	0x0000 0350 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1350 + (0x4 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

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Table 10-302. Register Call Summary for Register DISPC_VID3_FIR_COEF_V_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-303. DISPC_VID3_ATTRIBUTES

Address Offset	0x0000 0370		
Physical Address	0x5800 1370	**Instance**	DISPC
Description	The register configures the attributes of the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31 30	29	28	27 26	25	24	23	22	21	20	19	18	17	16	15 14	13 12	11	10	9	8	7	6	5	4 3 2 1	0
CHANNELOUT2	BURSTTYPE	PREMULTIPLYALPHA	ZORDER	ZORDERENABLE	SELFREFRESH	ARBITRATION	DOUBLESTRIDE	VERTICALTAPS	FORCE1DTILEDMODE	BUFPRELOAD	RESERVED	SELFREFRESHAUTO	CHANNELOUT	BURSTSIZE	ROTATION	FULLRANGE	REPLICATIONENABLE	COLORCONVENABLE	FRAMEPACKINGMODE	HRESIZECONF	RESIZEENABLE	FORMAT		ENABLE

Bits	Field Name	Description	Type	Reset
31:30	CHANNELOUT2	It is not used if CHANNELOUT is set to TV. Reserved when CHANNELOUT = 1 (should be set to zero) wr: immediate 0x0: Primary LCD output selected. 0x1: Secondary LCD output selected. 0x2: Third LCD output selected. 0x3: Write-back output to the memory selected.	RW	0x0
29	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0
28	PREMULTIPLYALPHA	The field configures the DISPC VID3 to process incoming data as premultiplied alpha data or non premultiplied alpha data. Default setting is non premultiplied alpha data. 0x0: Non premultiplyalpha data color component 0x1: Premultiplyalpha data color component	RW	0

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Bits	Field Name	Description	Type	Reset
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the ZORDER bit field is ignored and replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3 0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3	RW	0x0
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is used only when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit field ZORDER (bits 26 and 27).	RW	0
24	SELFREFRESH	Enables the self refresh of the video window from its own DMA buffer only. 0x0: The video pipeline accesses the interconnect to fetch data from the system memory. 0x1: The video pipeline does not need anymore to fetch data from memory. Only the DMA buffer associated with the video3 is used. It takes effect after the frame has been loaded in the DMA buffer.	RW	0
23	ARBITRATION	Determines the priority of the video pipeline. The video pipeline is one of the high priority pipeline. The arbitration gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The video pipeline is one of the normal priority pipeline. 0x1: The video pipeline is one of the high priority pipeline.	RW	0
22	DOUBLESTRIDE	Determines if the stride for CbCr buffer is the 1x or 2x of the Y buffer stride. It is only used in case of YUV4:2:0. 0x0: The CbCr stride value is equal to the Y stride. 0x1: The CbCr stride value is double to the Y stride.	RW	0
21	VERTICALTAPS	Video vertical resize tap number 0x0: 3 taps are used for the vertical filtering logic. The 2 other taps are not used. The associated bit fields for the 2 other taps coefficients do not need to be initialized. 0x1: 5 taps are used for the vertical filtering logic.	RW	0
20	FORCE1DTILEDMODE	Force TILED regions access to 1D or 2D. 0x0: 2D accesses for tiled regions 0x1: 1D accesses for tiled regions	RW	0
19	BUFPRELOAD	Video Preload Value 0x0: Hardware prefetches pixels up to the preload value defined in the preload register 0x1: Hardware prefetches pixels up to high threshold value	RW	0
18	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0

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Bits	Field Name	Description	Type	Reset
17	SELFREFRESHAUTO	Automatic self-refresh mode 0x0: The transition from SELFREFRESH disabled to enabled is controlled by SW. 0x1: The transition from SELFREFRESH disabled to enabled is controlled only by hardware.	RW	0
16	CHANNELOUT	Video channel out configuration: LCD, WB or TV. wr: immediate 0x0: LCD output or WB to the memory selected. bit fields 31 and 30 defines the output associated (primary, secondary or write-back). 0x1: TV output selected	RW	0
15:14	BURSTSIZE	Video DMA burst size 0x0: 2 × 128-bit bursts 0x1: 4 × 128-bit bursts 0x3: Reserved 0x2: 8 × 128-bit bursts	RW	0x2
13:12	ROTATION	Video rotation flag 0x0: No rotation 0x1: Rotation by 90 degrees 0x3: Rotation by 270 degrees 0x2: Rotation by 180 degrees	RW	0x0
11	FULLRANGE	Color Space Conversion full range setting. 0x0: Limited range selected: 16 subtracted from Y before color space conversion 0x1: Full range selected: Y is not modified before the color space conversion	RW	0
10	REPLICATIONENABLE	Replication enable 0x0: Disable Video replication logic 0x1: Enable Video replication logic	RW	1
9	COLORCONVENABLE	Enable the color space conversion. The hardware does not enable/disable the conversion based on the pixel format. The bit field shall be reset when the format is not YUV. 0x0: Disable Color Space Conversion YUV to RGB 0x1: Enable Color Space Conversion YUV to RGB	RW	0
8	FRAMEPACKINGMODE	Frame packing mode control. 0x0: Frame Packing mode is disabled 0x1: Nibble mode is enabled	RW	0
7	HRESIZECONF	Write 0s for future compatibility. Reads return 0.	R	0
6:5	RESIZEENABLE	Video resize enable 0x0: Disable both horizontal and vertical resize processing 0x1: Enable the horizontal resize processing 0x3: Enable both horizontal and vertical resize processing 0x2: Enable the vertical resize processing	RW	0x0

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Bits	Field Name	Description	Type	Reset
4:1	FORMAT	Video format. It defines the pixel format when fetching the video 3 picture into memory. 0x6: RGB16-565 0x1: RGB12x-4444 0xA: YUV2 4:2:2 co-sited 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: NV12 4:2:0 2 buffers (Y + UV) 0x2: RGBA12-4444 0x8: RGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: UYVY 4:2:2 co-sited 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x4: xRGB12-4444 0x3: BGRA32-8888 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	Video Enable 0x0: Video disabled (video pipeline inactive and window not present) 0x1: Video enabled (video pipeline active and window present on the screen)	RW	0

Table 10-304. Register Call Summary for Register DISPC_VID3_ATTRIBUTES

Display Controller

- DISPC Alpha Blender: [0]
- DISPC Extended 3D Support - Frame Packing Format Format: [1]
- DISPC Shadow Registers: [2]
- DISPC Logical Register Mapping: [3]
- DISPC Register Summary: [4]

Table 10-305. DISPC_VID3_CONV_COEF0

Address Offset	0x0000 0374		
Physical Address	0x5800 1374	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RCR								RESERVED								RY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	RCR	RCr coefficient encoded signed value (from –1024 to 1023).	RW	0x000

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Bits	Field Name	Description	Type	Reset
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RY	RY coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-306. Register Call Summary for Register DISPC_VID3_CONV_COEF0

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-307. DISPC_VID3_CONV_COEF1

Address Offset	0x0000 0378		
Physical Address	0x5800 1378	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GY								RESERVED								RCB							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GY	GY coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	RCB	RCb coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-308. Register Call Summary for Register DISPC_VID3_CONV_COEF1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-309. DISPC_VID3_CONV_COEF2

Address Offset	0x0000 037C		
Physical Address	0x5800 137C	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								GCB								RESERVED								GCR							

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	GCB	GCb coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	GCR	GCr coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-310. Register Call Summary for Register DISPC_VID3_CONV_COEF2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-311. DISPC_VID3_CONV_COEF3

Address Offset	0x0000 0380		
Physical Address	0x5800 1380	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BCR								RESERVED								BY							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	BCR	BCr coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	BY	BY coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-312. Register Call Summary for Register DISPC_VID3_CONV_COEF3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-313. DISPC_VID3_CONV_COEF4

Address Offset	0x0000 0384		
Physical Address	0x5800 1384	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					BCB										

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	BCB	BCb coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-314. Register Call Summary for Register DISPC_VID3_CONV_COEF4

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-315. DISPC_VID3_BUF_SIZE_STATUS

Address Offset	0x0000 0388		
Physical Address	0x5800 1388	**Instance**	DISPC
Description	The register defines the DMA buffer size for the video pipeline 3.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	DMA buffer Size in number of 128 bits.	R	0x0800

Table 10-316. Register Call Summary for Register DISPC_VID3_BUF_SIZE_STATUS

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-317. DISPC_VID3_BUF_THRESHOLD

Address Offset	0x0000 038C		
Physical Address	0x5800 138C	**Instance**	DISPC
Description	The register configures the DMA buffer associated with the video pipeline 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	DMA buffer high threshold number of 128 bits defining the threshold value	RW	0x07FF
15:0	BUFLOWTHRESHOLD	DMA buffer low threshold number of 128 bits defining the threshold value	RW	0x07F8

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Table 10-318. Register Call Summary for Register DISPC_VID3_BUF_THRESHOLD

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-319. DISPC_VID3_FIR

Address Offset	0x0000 0390		
Physical Address	0x5800 1390	**Instance**	DISPC
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 3. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-320. Register Call Summary for Register DISPC_VID3_FIR

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-321. DISPC_VID3_PICTURE_SIZE

Address Offset	0x0000 0394		
Physical Address	0x5800 1394	**Instance**	DISPC
Description	The register configures the size of the video picture associated with the video layer 3 before up/down-scaling. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MEMSIZEY												RESERVED				MEMSIZEX											

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:16	MEMSIZEY	Number of lines of the video picture Encoded value (from 1 to 4096) to specify the number of lines of the video picture in memory (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded 2^{11}.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	MEMSIZEX	Number of pixels of the video picture Encoded value (from 1 to 2048) to specify the number of pixels of the video picture in memory (program to value minus 1). The size is limited to the size of the line buffer of the vertical sampling block in case the video picture is processed by the vertical filtering unit. (program to value minus 1). When predecimation is set, the value represents the size of the image after predecimation but the max size of the unpredecimated image size in memory is still bounded 2^{11}.	RW	0x000

Table 10-322. Register Call Summary for Register DISPC_VID3_PICTURE_SIZE

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-323. DISPC_VID3_PIXEL_INC

Address Offset	0x0000 0398		
Physical Address	0x5800 1398	**Instance**	DISPC
Description	The register configures the number of bytes to increment between two pixels for the buffer associated with the video window 3. For more information, see Section 10.2.4.6.5, *Predecimation*.The register is used only when the TILER is not present in the system in order to perform low performance rotation. When the TILER IP is present it is highly recommended to use it for performing the rotation. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Number of bytes to increment between two pixels. Encoded unsigned value (from 1 to 255) to specify the number of bytes between two pixels in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n * bpp means increment of n pixels. For YUV4:2:0, maximum supported value is 128.	RW	0x01

Table 10-324. Register Call Summary for Register DISPC_VID3_PIXEL_INC

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-325. DISPC_VID3_POSITION

Address Offset	0x0000 039C		
Physical Address	0x5800 139C	**Instance**	DISPC
Description	The register configures the position of the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								POSY								RESERVED								POSX							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	POSY	Y position of the video window 2 Encoded value (from 0 to 2047) to specify the Y position of the video window 2 .The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	POSX	X position of the video window 2 Encoded value (from 0 to 2047) to specify the X position of the video window 2. The first pixel on the left of the display screen has the X-position 0.	RW	0x000

Table 10-326. Register Call Summary for Register DISPC_VID3_POSITION

Display Controller

- DISPC Extended 3D Support - Line Alternative Format: [0]
- DISPC Extended 3D Support - Frame Packing Format Format: [1]
- DISPC Shadow Registers: [2]
- DISPC Logical Register Mapping: [3]
- DISPC Register Summary: [4]

Table 10-327. DISPC_VID3_PRELOAD

Address Offset	0x0000 03A0		
Physical Address	0x5800 13A0	**Instance**	DISPC
Description	The register configures the DMA buffer of the video 3 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRELOAD							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:0	PRELOAD	DMA buffer preload value Number of 128-bit words defining the preload value.	RW	0x100

Table 10-328. Register Call Summary for Register DISPC_VID3_PRELOAD

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

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Table 10-329. DISPC_VID3_ROW_INC

Address Offset	0x0000 03A4		
Physical Address	0x5800 13A4	**Instance**	DISPC
Description	The register configures the number of bytes to increment at the end of the row for the buffer associated with the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded signed value (from $2^{31}1$ to 2^{31}) to specify the number of bytes to increment at the end of the row in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n * bpp means increment of n pixels. The value 1 (n + 1) * bpp means decrement of n pixels.	RW	0x0000 0001

Table 10-330. Register Call Summary for Register DISPC_VID3_ROW_INC

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-331. DISPC_VID3_SIZE

Address Offset	0x0000 03A8		
Physical Address	0x5800 13A8	**Instance**	DISPC
Description	The register configures the size of the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZEY								RESERVED				SIZEX											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:16	SIZEY	Number of lines of the video 3 Encoded value (from 1 to 4096) to specify the number of lines of the video window 3. Program to value minus 1.	RW	0x000
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:0	SIZEX	Number of pixels of the video window 3 Encoded value (from 1 to 4096) to specify the number of pixels of the video window 3. Program to value minus 1.	RW	0x000

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Table 10-332. Register Call Summary for Register DISPC_VID3_SIZE

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-333. DISPC_DEFAULT_COLOR2

Address Offset	0x0000 03AC		
Physical Address	0x5800 13AC	**Instance**	DISPC
Description	The control register allows to configure the default solid background color for the secondary LCD Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEFAULTCOLOR																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	DEFAULTCOLOR	24-bit RGB color value to specify the default solid color to display when there is no data from the overlays.	RW	0x000000

Table 10-334. Register Call Summary for Register DISPC_DEFAULT_COLOR2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-335. DISPC_TRANS_COLOR2

Address Offset	0x0000 03B0		
Physical Address	0x5800 13B0	**Instance**	DISPC
Description	The register sets the transparency color value for the video/graphics overlays for the secondary LCD output. Shadow register, updated on VFP start period of the secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRANSCOLORKEY																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	TRANSCOLORKEY	Transparency Color Key Value in RGB format [0] BITMAP 1 (CLUT), [23,1] set to 0s [1:0] BITMAP 2 (CLUT), [23,2] set to 0s [3:0] BITMAP 4 (CLUT), [23,4] set to 0s [7:0] BITMAP 8 (CLUT), [23,8] set to 0s [11:0] RGB 12, [23,12] set to 0s [15:0] RGB 16, [23,16] set to 0s [23:0] RGB 24	RW	0x000000

Table 10-336. Register Call Summary for Register DISPC_TRANS_COLOR2

Display Controller

- DISPC Transparency Color Keys: [0]
- DISPC Shadow Registers: [1]
- DISPC Logical Register Mapping: [2]
- DISPC Register Summary: [3]

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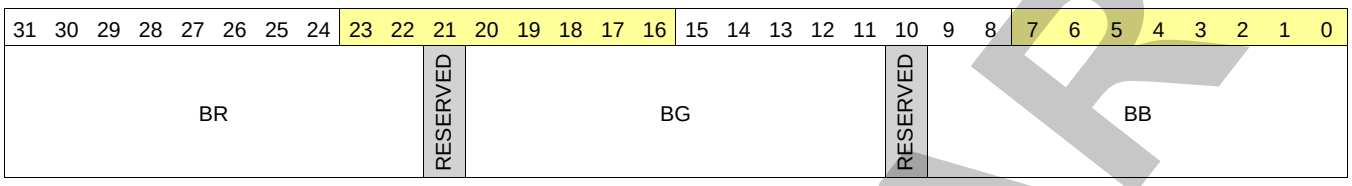
Table 10-337. DISPC_CPR2_COEF_B

Address Offset	0x0000 03B4		
Physical Address	0x5800 13B4	**Instance**	DISPC
Description	The register configures the color phase rotation matrix coefficients for the Blue component. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:22	BR	BR coefficient encoded signed value (from –512 to 511).	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	BG	BG coefficient encoded signed value (from –512 to 511).	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	BB	BB coefficient encoded signed value (from –512 to 511).	RW	0x000

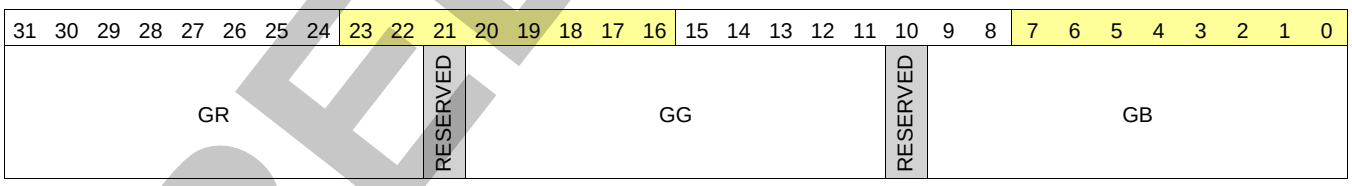
Table 10-338. Register Call Summary for Register DISPC_CPR2_COEF_B

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-339. DISPC_CPR2_COEF_G

Address Offset	0x0000 03B8		
Physical Address	0x5800 13B8	**Instance**	DISPC
Description	The register configures the color phase rotation matrix coefficients for the Green component. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:22	GR	GR coefficient encoded signed value (from –512 to 511).	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	GG	GG coefficient encoded signed value (from –512 to 511).	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	GB	GB coefficient encoded signed value (from –512 to 511).	RW	0x000

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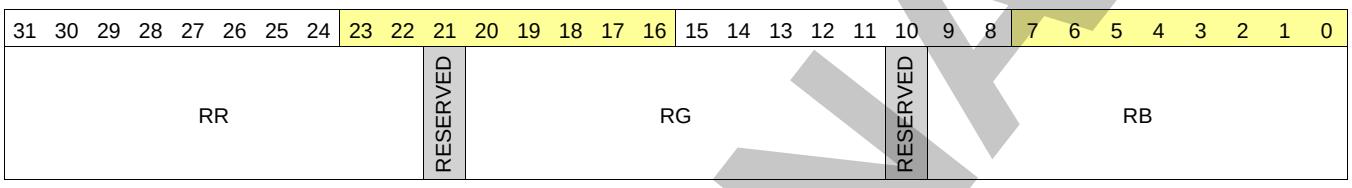
Table 10-340. Register Call Summary for Register DISPC_CPR2_COEF_G

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-341. DISPC_CPR2_COEF_R

Address Offset	0x0000 03BC		
Physical Address	0x5800 13BC	**Instance**	DISPC
Description	The register configures the color phase rotation matrix coefficients for the Red component. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:22	RR	RR coefficient encoded signed value (from –512 to 511).	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	RG	RG coefficient encoded signed value (from –512 to 511).	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	RB	RB coefficient encoded signed value (from –512 to 511).	RW	0x000

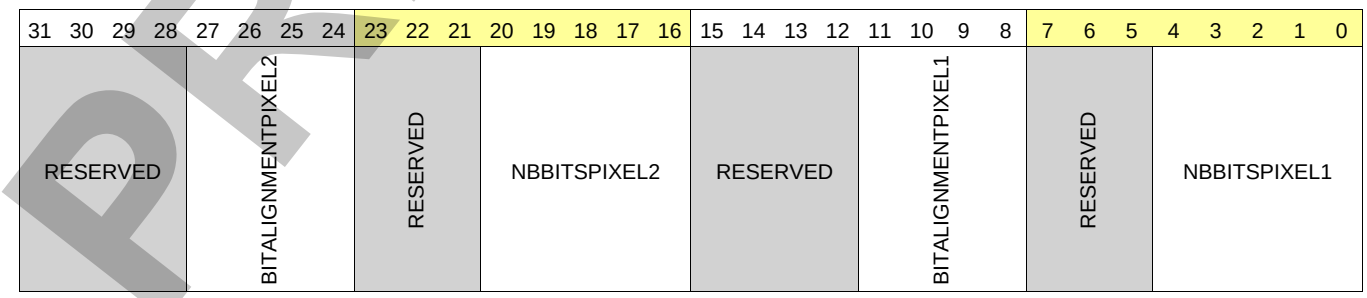
Table 10-342. Register Call Summary for Register DISPC_CPR2_COEF_R

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-343. DISPC_DATA2_CYCLE1

Address Offset	0x0000 03C0		
Physical Address	0x5800 13C0	**Instance**	DISPC
Description	The control register configures the output data format for 1st cycle. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-344. Register Call Summary for Register DISPC_DATA2_CYCLE1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-345. DISPC_DATA2_CYCLE2

Address Offset	0x0000 03C4		
Physical Address	0x5800 13C4	**Instance**	DISPC
Description	The control register configures the output data format for 2nd cycle. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED	NBBITSPIXEL2	RESERVED	BITALIGNMENTPIXEL1	RESERVED	NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

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Table 10-346. Register Call Summary for Register DISPC_DATA2_CYCLE2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-347. DISPC_DATA2_CYCLE3

Address Offset	0x0000 03C8		
Physical Address	0x5800 13C8	**Instance**	DISPC
Description	The control register configures the output data format for 3rd cycle. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED / NBBITSPIXEL2	RESERVED / BITALIGNMENTPIXEL1	RESERVED / NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment. Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment. Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-348. Register Call Summary for Register DISPC_DATA2_CYCLE3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-349. DISPC_SIZE_LCD2

Address Offset	0x0000 03CC		
Physical Address	0x5800 13CC	**Instance**	DISPC
Description	The register configures the panel size (horizontal and vertical). It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD. A delta value is used to indicate if the odd field has same vertical size as the even field or +/- one line.		
Type	RW		

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31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	LPP		DELTA_LPP	RESERVED	PPL	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
27:16	LPP	Lines per panel encoded value (from 1 to 4096) to specify the number of lines per panel (program to value minus 1).	RW	0x000
15:14	DELTA_LPP	Indicates the delta size value of the odd field compared to the even field 0x0: same size 0x1: odd size = even size +1 0x2: Odd size = even size –1	RW	0x0
13:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:0	PPL	Pixels per line encoded value (from 1 to 4096) to specify the number of pixels contains within each line on the display (program to value minus 1). In STALL mode, any value is valid. In non STALL mode, only values multiple of 8 pixels are valid.	RW	0x000

Table 10-350. Register Call Summary for Register DISPC_SIZE_LCD2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1] [2]
- DISPC Register Summary: [3]
- DISPC Register Description: [4]

Table 10-351. DISPC_TIMING_H2

Address Offset	0x0000 0400		
Physical Address	0x5800 1400	**Instance**	DISPC
Description	The register configures the timing logic for the HSYNC signal. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
HBP			HFP			HSW	

Bits	Field Name	Description	Type	Reset
31:20	HBP	Horizontal back porch. Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the beginning of a line transmission before the first set of pixels is output to the display (program to value minus 1).	RW	0x000
19:8	HFP	Horizontal front porch. Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the end of a line transmission before line clock is asserted (program to value minus 1).	RW	0x000
7:0	HSW	Horizontal synchronization pulse width encoded value (from 1 to 256) to specify the number of pixel clock periods to pulse the line clock at the end of each line (program to value minus 1).	RW	0x00

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Table 10-352. Register Call Summary for Register DISPC_TIMING_H2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-353. DISPC_TIMING_V2

Address Offset	0x0000 0404		
Physical Address	0x5800 1404	**Instance**	DISPC
Description	The register configures the timing logic for the VSYNC signal. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBP																VFP								VSW							

Bits	Field Name	Description	Type	Reset
31:20	VBP	Vertical back porch encoded value (from 0 to 4095) to specify the number of line clock periods to add to the beginning of a frame before the first set of pixels is output to the display.	RW	0x000
19:8	VFP	Vertical front porch encoded value (from 0 to 4095) to specify the number of line clock periods to add to the end of each frame.	RW	0x000
7:0	VSW	Vertical synchronization pulse width In active mode, encoded value (from 1 to 256) to specify the number of line clock periods (program to value minus 1) to pulse the frame clock (VSYNC) pin at the end of each frame after the end of frame wait (VFP) period elapses. Frame clock uses as VSYNC signal in active mode.	RW	0x00

Table 10-354. Register Call Summary for Register DISPC_TIMING_V2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-355. DISPC_POL_FREQ2

Address Offset	0x0000 0408		
Physical Address	0x5800 1408	**Instance**	DISPC
Description	The register configures the signal configuration. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ALIGN	ONOFF	RF	IEO	IPC	IHS	IVS	ACBI				ACB							

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Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
18	ALIGN	Defines the alignment between HSYNC and VSYNC assertion. 0x0: VSYNC and HSYNC are not aligned. 0x1: VSYNC and HSYNC assertions are aligned.	RW	0
17	ONOFF	HSYNC/VSYNC Pixel clock Control On/Off 0x0: HSYNC and VSYNC are driven on opposite edges of pixel clock than pixel data. 0x1: HSYNC and VSYNC are driven according to bit 16.	RW	0
16	RF	Program HSYNC/VSYNC Rise or Fall 0x0: HSYNC and VSYNC are driven on falling edge of pixel clock (if bit 17 set to 1). 0x1: HSYNC and VSYNC are driven on rising edge of pixel clock (if bit 17 set to 1).	RW	0
15	IEO	Invert output enable 0x0: Ac-bias is active high (active display mode). 0x1: Ac-bias is active low (active display mode).	RW	0
14	IPC	Invert pixel clock 0x0: Data is driven on the LCD data lines on the rising-edge of the pixel clock. 0x1: Data is driven on the LCD data lines on the falling-edge of the pixel clock.	RW	0
13	IHS	Invert HSYNC 0x0: Line clock pin is active high and inactive low. 0x1: Line clock pin is active low and inactive high.	RW	0
12	IVS	Invert VSYNC 0x0: Frame clock pin is active high and inactive low. 0x1: Frame clock pin is active low and inactive high.	RW	0
11:8	ACBI	AC Bias Pin transitions per interrupt Value (from 0 to 15) used to specify the number of AC Bias pin transitions	RW	0x0
7:0	ACB	AC Bias Pin Frequency Value (from 0 to 255) used to specify the number of line clocks to count before transitioning the AC Bias pin. This pin is used to periodically invert the polarity of the power supply to prevent DC charge build-up within the display.	RW	0x00

Table 10-356. Register Call Summary for Register DISPC_POL_FREQ2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-357. DISPC_DIVISOR2

Address Offset	0x0000 040C		
Physical Address	0x5800 140C	**Instance**	DISPC
Description	The register configures the divisors. It is used for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LCD								RESERVED								PCD							

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:16	LCD	Display controller logic clock divisor value (from 1 to 255) to specify the intermediate pixel clock frequency based on the LCD2_CLK. The value 0 is invalid.	RW	0x04
15:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
7:0	PCD	Pixel clock divisor value (from 1 to 255) to specify the frequency of the pixel clock based on the LCD2_CLK divided by DISPC_DIVISOR2.LCD value. The value 0 is invalid.	RW	0x01

Table 10-358. Register Call Summary for Register DISPC_DIVISOR2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]
- DISPC Register Description: [3] [4]

Table 10-359. DISPC_WB_ACCU_j

Address Offset	0x0000 0500 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1500 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the write back pipeline (DISPC_WB_ACCU_0 and DISPC_WB_ACCU_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for ARGB and Y setting. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					VERTICALACCU											RESERVED					HORIZONTALACCU										

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accumulator value Encoded value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accumulator value encoded value (from –1024 to 1023).	RW	0x000

Table 10-360. Register Call Summary for Register DISPC_WB_ACCU_j

Display Controller

- DISPC Scaler Unit: [0] [1]
- DISPC Shadow Registers: [2]
- DISPC WB Pipeline Configuration: [3] [4]
- DISPC Register Summary: [5]

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Table 10-361. DISPC_WB_BA_j

Address Offset	0x0000 0508 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1508 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the base address of the WB buffer (DISPC_WB_BA_0 and DISPC_WB_BA_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_WB_BA_0 is used). Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Write-back base address Base address of the WB buffer (aligned on pixel size boundary except in case of RGB24 packed format, 4-pixel alignment is required; in case of YUV4:2:2, 2-pixel alignment is required, and YUV4:2;0, byte alignment is supported)). It case of YUV4:2:0 format, it indicates the base address of the Y buffer. When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-362. Register Call Summary for Register DISPC_WB_BA_j

Display Controller

- DISPC: [0]
- DISPC Rotation and Mirroring: [1] [2] [3] [4]
- DISPC Shadow Registers: [5]
- DISPC DMA Configuration: [6]
- DISPC Register Summary: [7]

Table 10-363. DISPC_WB_FIR_COEF_H_i

Address Offset	0x0000 0510 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1510 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

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Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-364. Register Call Summary for Register DISPC_WB_FIR_COEF_H_i

Display Controller
- DISPC Scaler Unit: [0] [1] [2] [3] [4] [5]
- DISPC Shadow Registers: [6]
- DISPC WB Pipeline Configuration: [7]
- DISPC Register Summary: [8]

Table 10-365. DISPC_WB_FIR_COEF_HV_i

Address Offset	0x0000 0514 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1514 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-366. Register Call Summary for Register DISPC_WB_FIR_COEF_HV_i

Display Controller
- DISPC Scaler Unit: [0] [1] [2] [3] [4] [5] [6]
- DISPC Shadow Registers: [7]
- DISPC WB Pipeline Configuration: [8] [9]
- DISPC Register Summary: [10]

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Table 10-367. DISPC_WB_FIR_COEF_V_i

Address Offset	0x0000 0550 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1550 + (0x4 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for ARGB and Y setting. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-368. Register Call Summary for Register DISPC_WB_FIR_COEF_V_i

Display Controller

- DISPC Scaler Unit: [0] [1] [2]
- DISPC Shadow Registers: [3]
- DISPC WB Pipeline Configuration: [4]
- DISPC Register Summary: [5]

Table 10-369. DISPC_WB_ATTRIBUTES

Address Offset	0x0000 0570		
Physical Address	0x5800 1570	**Instance**	DISPC
Description	The register configures the attributes of the viwrite back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDLENUMBER				IDLESIZE	CAPTUREMODE			ARBITRATION	DOUBLESTRIDE	VERTICALTAPS	FORCE1DTILEDMODE	WRITEBACKMODE	CHANNELIN			BURSTSIZE		RESERVED		FULLRANGE	TRUNCATIONENABLE	COLORCONVENABLE	BURSTTYPE	ALPHAENABLE	RESIZEENABLE	FORMAT					ENABLE

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Bits	Field Name	Description	Type	Reset
31:28	IDLENUMBER	Determines the number of idles between requests on the L3_MAIN interconnect. It is only used when the write-back pipeline does data transfer from memory to memory. When the output of an overlay is stored in memory through the write-back pipeline in capture mode, the bit field IDLENUMBER is ignored since a timing generator is used to time the transfer. The number of IDLE cycles is IDLENUMBER (from 0 to 15) if IDLESIZE = 0. The number of IDLE cycles is IDLENUMBERx8 (from 0 to 120) if IDLESIZE = 1 and BURSTSIZE = 2. The number of IDLE cycles is IDLENUMBERx4 (from 0 to 60) if IDLESIZE = 1 and BURSTSIZE = 1. The number of IDLE cycles is IDLENUMBERx2 (from 0 to 30) if IDLESIZE = 1 and BURSTSIZE = 0.	RW	0x0
27	IDLESIZE	Determines if the IDLENUMBER corresponds to a number of bursts or singles. 0x0: The number of idles between requests is defined by IDLENUMBER as number of cycles. 0x1: The number of idles between requests is defined by IDLENUMBER multiplied by burst size as number of cycles.	RW	0
26:24	CAPTUREMODE	Defines the frame rate capture. 0x6: Only one out of six frames is captured. The first one is captured then the second one is skipped and so on. 0x1: Only one frame is captured. 0x7: Only one out of seven frames is captured. The first one is captured then the second one is skipped and so on. 0x0: All frames are captures until the write-back channel is disabled or there is no more data generated by the overlay or the pipeline attached to the write-back channel. 0x2: Only one out of two frames is captured. The first one is captured, and then the second one is skipped, and so on. 0x4: Only one out of four frames is captured. The first one is captured, and then the second one is skipped, and so on. 0x5: Only one out of five frames is captured. The first one is captured, and then the second one is skipped, and so on. 0x3: Only one out of three frames is captured. The first one is captured, and then the second one is skipped, and so on.	RW	0x0
23	ARBITRATION	Determines the priority of the write-back pipeline. The write-back pipeline is one of the high priority pipeline. The arbitration gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The write-back pipeline is one of the normal priority pipeline. 0x1: The write-back pipeline is one of the high priority pipeline.	RW	0
22	DOUBLESTRIDE	Determines if the stride for CbCr buffer is the 1x or 2x of the Y buffer stride. It is only used in case of YUV4:2:0. 0x0: The CbCr stride value is equal to the Y stride. 0x1: The CbCr stride value is double to the Y stride.	RW	0

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Bits	Field Name	Description	Type	Reset
21	VERTICALTAPS	Video Vertical Resize Tap Number 0x0: 3 taps are used for the vertical filtering logic. The 2 other taps are not used. 0x1: 5 taps are used for the vertical filtering logic.	RW	0
20	FORCE1DTILEDMODE	Force TILED regions access to 1D or 2D. 0x0: 2D accesses for tiled regions 0x1: 1D accesses for tiled regions	RW	0x0
19	WRITEBACKMODE	When connected to the overlay output of a channel the write back can operate as a simple transfer from memory to memory (composition engine) or as a capture channel. 0x0: Capture mode (default mode) 0x1: Memory-to-memory mode	RW	0x0
18:16	CHANNELIN	Video Channel In configuration WR: immediate 0x6: Video3 pipeline output 0x1: Secondary LCD output 0x0: Primary LCD overlay output 0x2: TV overlay output 0x4: Video1 pipeline output 0x5: Video2 pipeline output 0x3: Graphics pipeline output 0x7: Third LCD output	RW	0x0
15:14	BURSTSIZE	Write-back DMA Burst Size 0x0: 2 × 128-bit bursts 0x1: 4 × 128-bit bursts 0x3: Reserved 0x2: 8 × 128-bit bursts	RW	0x2
13:12	RESERVED	Reserved	RW	0x0
11	FULLRANGE	Color Space Conversion full range setting. 0x0: Limited range selected: 16 subtracted from Y before color space conversion 0x1: Full range selected: Y is not modified before the color space conversion	RW	0
10	TRUNCATIONENABLE	It applies only when the input format to the write-back pipeline from the overlay or directly from one of the pipelines is ARGB32. If the format is one of the YUV supported formats, the bit field is ignored. 0x0: Disable truncation logic 0x1: Enable truncation logic from ARGB32 to the pixel format defined in the field FORMAT.	RW	0
9	COLORCONVENABLE	Enable the color space conversion. The hardware does not enable/disable the conversion based on the pixel format. The bit field shall be reset when the format is not YUV. 0x0: Disable Color Space Conversion RGB to YUV 0x1: Enable Color Space Conversion RGB to YUV	RW	0
8	BURSTTYPE	The type of burst can be INCR (incremental) or BLCK (2D block). The 2D block is required when the TILER is targeted by the DMA engine. 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0

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Bits	Field Name	Description	Type	Reset
7	ALPHAENABLE	Premultiplied alpha enable Read 0x1: Enabled Read 0x0: Disabled. This bit also disable the logic present in the associated channel out that compute the alpha component sent to the WB pipe. When the WB is configured to copy back one of the output channels (output of overlay), the following configurations are available: 0x1: The WB pipe copies back to memory the premultiplied alpha calculated through the overlay. 0x0: The alpha value is not written back.	RW	0
6:5	RESIZEENABLE	Resize Enable 0x0: Disable the resize processing 0x1: Enable the horizontal resize processing 0x3: Enable both horizontal and vertical resize processing 0x2: Enable the vertical resize processing	RW	0x0
4:1	FORMAT	Write-back format. It defines the pixel format when storing the write-back picture into memory. 0x6: RGB16-565 0x1: RGB12x-4444 0xA: YUV2 4:2:2 co-sited 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: NV12 4:2:0 2 buffers (Y + UV) 0x2: RGBA12-4444 0x8: xRGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: UYVY 4:2:2 co-sited 0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x4: xRGB12-4444 0x3: BGRA32-8888 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)	RW	0x0
0	ENABLE	Write-back enable. wr: immediate 0x0: Write-back disabled 0x1: Write-back enabled	RW	0

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Table 10-370. Register Call Summary for Register DISPC_WB_ATTRIBUTES

Display Controller

- DISPC: [0]
- DISPC WRITE DMA Buffer (WB Pipeline): [1] [2] [3] [4] [5]
- DISPC Arbitration: [6]
- DISPC Write-Back Pipeline: [7] [8] [9]
- DISPC CSC Unit RGB to YUV: [10] [11]
- DISPC Scaler Unit: [12] [13] [14]
- DISPC RGB Truncation Logic: [15] [16]
- DISPC Alpha Blender: [17] [18] [19]
- DISPC Shadow Registers: [20] [21] [22] [23] [24] [25]
- DISPC DMA Configuration: [26] [27] [28] [29]
- DISPC WB Pipeline Configuration: [30] [31] [32] [33] [34] [35] [36] [37] [38] [39]
- DISPC Register Summary: [40]

Table 10-371. DISPC_WB_CONV_COEF0

Address Offset	0x0000 0574		
Physical Address	0x5800 1574	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the write back pipeline (YUV4:4:4 to RGB24) Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								YG								RESERVED								YR							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	YG	YG coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	YR	YR coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-372. Register Call Summary for Register DISPC_WB_CONV_COEF0

Display Controller

- DISPC CSC Unit RGB to YUV: [0] [1]
- DISPC Shadow Registers: [2]
- DISPC WB Pipeline Configuration: [3]
- DISPC Register Summary: [4]

Table 10-373. DISPC_WB_CONV_COEF1

Address Offset	0x0000 0578		
Physical Address	0x5800 1578	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the write back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CRR								RESERVED								YB							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	CRR	CrR coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	YB	YB coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-374. Register Call Summary for Register DISPC_WB_CONV_COEF1

Display Controller

- DISPC CSC Unit RGB to YUV: [0] [1]
- DISPC Shadow Registers: [2]
- DISPC WB Pipeline Configuration: [3]
- DISPC Register Summary: [4]

Table 10-375. DISPC_WB_CONV_COEF2

Address Offset	0x0000 057C		
Physical Address	0x5800 157C	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the write back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CRB								RESERVED								CRG							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	CRB	CrB coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	CRG	CrG coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-376. Register Call Summary for Register DISPC_WB_CONV_COEF2

Display Controller

- DISPC CSC Unit RGB to YUV: [0] [1]
- DISPC Shadow Registers: [2]
- DISPC WB Pipeline Configuration: [3]
- DISPC Register Summary: [4]

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Table 10-377. DISPC_WB_CONV_COEF3

Address Offset	0x0000 0580		
Physical Address	0x5800 1580	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the write back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CBG								RESERVED								CBR							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	CBG	CbG coefficient encoded signed value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	CBR	CbR coefficient encoded signed value (from –1024 to 1023).	RW	0x000

Table 10-378. Register Call Summary for Register DISPC_WB_CONV_COEF3

Display Controller

- DISPC CSC Unit RGB to YUV: [0] [1]
- DISPC Shadow Registers: [2]
- DISPC WB Pipeline Configuration: [3]
- DISPC Register Summary: [4]

Table 10-379. DISPC_WB_CONV_COEF4

Address Offset	0x0000 0584		
Physical Address	0x5800 1584	**Instance**	DISPC
Description	The register configures the color space conversion matrix coefficients for the write back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CBB							

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
10:0	CBB	CbB coefficient encoded signed value (from –1024 to 1023).	RW	0x000

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Table 10-380. Register Call Summary for Register DISPC_WB_CONV_COEF4

Display Controller

- DISPC CSC Unit RGB to YUV: [0]
- DISPC Shadow Registers: [1]
- DISPC WB Pipeline Configuration: [2]
- DISPC Register Summary: [3]

Table 10-381. DISPC_WB_BUF_SIZE_STATUS

Address Offset	0x0000 0588		
Physical Address	0x5800 1588	**Instance**	DISPC
Description	The register defines the DMA buffer size for the write back pipeline.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BUFSIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:0	BUFSIZE	DMA buffer Size in number of 128 bits	R	0x0800

Table 10-382. Register Call Summary for Register DISPC_WB_BUF_SIZE_STATUS

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-383. DISPC_WB_BUF_THRESHOLD

Address Offset	0x0000 058C		
Physical Address	0x5800 158C	**Instance**	DISPC
Description	The register configures the DMA buffer associated with the write-back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFHIGHTHRESHOLD																BUFLOWTHRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	BUFHIGHTHRESHOLD	DMA buffer high threshold number of 128 bits defining the threshold value	RW	0x07FF
15:0	BUFLOWTHRESHOLD	DMA buffer low threshold number of 128 bits defining the threshold value	RW	0x07F8

Table 10-384. Register Call Summary for Register DISPC_WB_BUF_THRESHOLD

Display Controller

- DISPC WRITE DMA Buffer (WB Pipeline): [0] [1]
- DISPC Shadow Registers: [2]
- DISPC DMA Configuration: [3] [4]
- DISPC Register Summary: [5]

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Table 10-385. DISPC_WB_FIR

Address Offset	0x0000 0590		
Physical Address	0x5800 1590	**Instance**	DISPC
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the write back pipeline. It is used for ARGB and Y setting. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-386. Register Call Summary for Register DISPC_WB_FIR

Display Controller

- DISPC Scaler Unit: [0] [1] [2] [3]
- DISPC Shadow Registers: [4]
- DISPC WB Pipeline Configuration: [5] [6]
- DISPC Register Summary: [7]

Table 10-387. DISPC_WB_PICTURE_SIZE

Address Offset	0x0000 0594		
Physical Address	0x5800 1594	**Instance**	DISPC
Description	The register configures the size of the write-back picture associated with the write back pipeline after up/down-scaling. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MEMSIZEY												RESERVED				MEMSIZEX											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
27:16	MEMSIZEY	Number of lines of the wb picture in memory. Encoded value (from 1 to 4096) to specify the number of lines of the picture in memory (program to value minus 1).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00

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Bits	Field Name	Description	Type	Reset
10:0	MEMSIZEX	Number of pixels of the wb picture in memory. Encoded value (from 1 to 2048) to specify the number of pixels of the picture in memory (program to value minus 1).	RW	0x000

Table 10-388. Register Call Summary for Register DISPC_WB_PICTURE_SIZE

Display Controller
- DISPC Scaler Unit: [0] [1]
- DISPC Shadow Registers: [2]
- DISPC DMA Configuration: [3] [4]
- DISPC Register Summary: [5]

Table 10-389. DISPC_WB_PIXEL_INC

Address Offset	0x0000 0598		
Physical Address	0x5800 1598	**Instance**	DISPC
Description	The register configures the number of bytes to increment between two pixels for the buffer associated with the write back pipeline. The register is used only when the TILER is not present in the system in order to perform low performance rotation. When the TILER IP is present it is highly recommended to use it for performing the rotation. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PIXELINC							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x000000
7:0	PIXELINC	Values other than 1 are invalid	RW	0x01

Table 10-390. Register Call Summary for Register DISPC_WB_PIXEL_INC

Display Controller
- DISPC: [0]
- DISPC Rotation and Mirroring: [1] [2] [3] [4]
- DISPC Shadow Registers: [5]
- DISPC DMA Configuration: [6]
- DISPC Register Summary: [7]

Table 10-391. DISPC_WB_ROW_INC

Address Offset	0x0000 05A4		
Physical Address	0x5800 15A4	**Instance**	DISPC
Description	The register configures the number of bytes to increment at the end of the row for the buffer associated with the vwrite back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROWINC																															

Bits	Field Name	Description	Type	Reset
31:0	ROWINC	Number of bytes to increment at the end of the row Encoded signed value (from 2^{31}1 to 2^{31}) to specify the number of bytes to increment at the end of the row in the video buffer. The value 0 is invalid. The value 1 means next pixel. The value 1 + n *bpp means increment of n pixels. The value 1 (n + 1) * bpp means decrement of n pixels.	RW	0x0000 0001

Table 10-392. Register Call Summary for Register DISPC_WB_ROW_INC

Display Controller

- DISPC: [0]
- DISPC Rotation and Mirroring: [1] [2] [3] [4]
- DISPC Shadow Registers: [5]
- DISPC DMA Configuration: [6]
- DISPC Register Summary: [7]

Table 10-393. DISPC_WB_SIZE

Address Offset	0x0000 05A8
Physical Address	0x5800 15A8 **Instance** DISPC
Description	The register configures the size of the output of overlay connected to the write-back pipeline when the overlay output is only used by the write-back pipeline. When the overlay is output on the primary LCD or secondary LCD or TV outputs, the size of the frame is defined in the DISPC_SIZE_LCD1, DISPC_SIZE_LCD2, and DISPC_SIZE_TV respectively. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SIZEY												RESERVED				SIZEX											

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
27:16	SIZEY	Number of lines of the Write-back picture Encoded value (from 1 to 4096) to specify the number of lines of the write-back picture from overlay or pipeline. Program to value minus 1.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	SIZEX	Number of pixels of the Write-back picture Encoded value (from 1 to 2048) to specify the number of pixels of the write-back picture from overlay or pipeline. Program to value minus 1.	RW	0x000

Table 10-394. Register Call Summary for Register DISPC_WB_SIZE

Display Controller

- DISPC Scaler Unit: [0] [1] [2] [3] [4]
- DISPC Shadow Registers: [5]
- DISPC WB Pipeline Configuration: [6] [7]
- DISPC Register Summary: [8]

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Table 10-395. DISPC_VID1_BA_UV_j

Address Offset	0x0000 0600 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1600 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the base address of the UV buffer for the video window 1. (DISPC_VID1_BA_UV_0 and DISPC_VID1_BA_UV_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID1_BA_UV_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address aligned on 16-bit boundary Base address of the UV video buffer used only in case of YUV4:2:0-NV12 When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-396. Register Call Summary for Register DISPC_VID1_BA_UV_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-397. DISPC_VID2_BA_UV_j

Address Offset	0x0000 0608 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1608 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the base address of the UV buffer for the video window 2. (DISPC_VID2_BA_UV_0 and DISPC_VID2_BA_UV_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID2_BA_UV_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

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Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address aligned on 16-bit boundary Base address of the UV video buffer used only in case of YUV4:2:0-NV12 When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-398. Register Call Summary for Register DISPC_VID2_BA_UV_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-399. DISPC_VID3_BA_UV_j

Address Offset	0x0000 0610 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1610 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the base address of the UV buffer for the video window 3. (DISPC_VID3_BA_UV_0 and DISPC_VID3_BA_UV_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_VID3_BA_UV_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address alinged on 16-bit boundary Base address of the UV video buffer used only in case of YUV4:2:0-NV12 When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-400. Register Call Summary for Register DISPC_VID3_BA_UV_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-401. DISPC_WB_BA_UV_j

Address Offset	0x0000 0618 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1618 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the base address of the UV buffer for the write-back pipeline. (DISPC_WB_BA_UV_0 and DISPC_WB_BA_UV_1 for ping-pong mechanism with external trigger, based on the field polarity otherwise only DISPC_WB_BA_UV_0 is used)). Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA																															

Bits	Field Name	Description	Type	Reset
31:0	BA	Video base address alinged on 16-bit boundary Base address of the UV video buffer used only in case of YUV4:2:0-NV12 When the TILER is addressed, the bits: [28:27] = 0x0 for 8-bit tiled [28:27] = 0x1 for 16-bit tiled [28:27] = 0x2 for 32-bit tiled [28:27] = 0x3 for page mode [31:29] = 0x0 for 0-degree view [31:29] = 0x1 for 180-degree view + mirroring [31:29] = 0x2 for 0-degree view + mirroring [31:29] = 0x3 for 180-degree view [31:29] = 0x4 for 270-degree view + mirroring [31:29] = 0x5 for 270-degree view [31:29] = 0x6 for 90-degree view [31:29] = 0x7 for 90-degree view + mirroring Otherwise the bits indicated the corresponding bit address to access the SDRAM.	RW	0x0000 0000

Table 10-402. Register Call Summary for Register DISPC_WB_BA_UV_j

Display Controller

- DISPC: [0]
- DISPC Shadow Registers: [1]
- DISPC DMA Configuration: [2]
- DISPC Register Summary: [3]

Table 10-403. DISPC_CONFIG2

Address Offset	0x0000 0620		
Physical Address	0x5800 1620	**Instance**	DISPC
Description	The control register configures the Display Controller module for the secondary LCD output. Shadow register, updated on VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SLCDINTERLEAVE	FULLRANGE	COLORCONVENABLE	FIDFIRST	OUTPUTMODEENABLE	RESERVED						BUFFERHANDCHECK	CPR	RESERVED			TCKLCDSELECTION	TCKLCDENABLE	RESERVED	ACBIASGATED	VSYNCGATED	HSYNCGATED	PIXELCLOCKGATED	PIXELDATAGATED	RESERVED			PIXELGATED

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:26	SLCDINTERLEAVE	sLCD Interleave Pattern	RW	0x0
25	FULLRANGE	Color space conversion full range setting. 0x0: Limited range selected. 0x1: Full range selected.	RW	0
24	COLORCONV ENABLE	Enable the color space conversion. It shall be reset when CPR bit field is set to 0x1. 0x0: Disable color space conversion RGB to YUV 0x1: Enable color space conversion RGB to YUV	RW	0
23	FIDFIRST	Selects the first field to output in case of interlace mode. In case of progressive mode, the value is not used. 0x0: First field is even. 0x1: Odd field is first.	RW	0
22	OUTPUTMODE ENABLE	Selects between progressive and interlace mode for the secondary LCD output. 0x0: Progressive mode selected. 0x1: Interlace mode selected.	RW	0
21:17	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
16	BUFFERHAND CHECK	Controls the handcheck between DMA buffer and STALL signal in order to prevent from underflow. The bit shall be set to 0 when the module is not in STALL mode. (secondary LCD output) 0x0: Only the STALL signal (generated by RFBI or DSI1_A depending on which IP uses the LCD output) is used regardless of the DMA buffer fullness information in order to provide data to the RFBI or DSI1_A module. 0x1: The STALL signal (generated by RFBI or DSI1_A depending on which IP uses the LCD output) is used in combination with the DMA buffer fullness information in order to provide data to the RFBI or DSI1_A module only when it does not generated buffer underflow.	RW	0
15	CPR	Color Phase Rotation Control secondary LCD output). It shall be reset when ColorConvEnable bit field is set to 1. wr: VFP start period of secondary LCD output 0x0: Color phase rotation disabled 0x1: Color phase rotation enabled	RW	0
14:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11	TCKLCD SELECTION	Transparency color key selection (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Destination transparency color key selected 0x1: Source transparency color key selected	RW	0
10	TCKLCDENABLE	Transparency color key enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Disable the transparency color key for the LCD 0x1: Enable the transparency color key for the LCD	RW	0
9	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
8	ACBIASGATED	ACBias gated enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: AcBias gated disabled 0x1: AcBias gated enabled	RW	0
7	VSYNCGATED	VSYNC gated enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: VSYNC gated disabled 0x1: VSYNC gated enabled	RW	0

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Bits	Field Name	Description	Type	Reset
6	HSYNCGATED	HSYNC gated enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: HSYNC gated disabled 0x1: HSYNC gated enabled	RW	0
5	PIXELCLOCK GATED	Pixel clock gated enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Pixel clock gated disabled 0x1: Pixel clock gated enabled	RW	0
4	PIXELDATA GATED	Pixel data gated enabled (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Pixel data gated disabled 0x1: Pixel data gated enabled	RW	0
3:1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
0	PIXELGATED	Pixel gated enable (only for active matrix) (secondary LCD output) wr: VFP start period of secondary LCD output 0x0: Pixel clock always toggles (only in active matrix mode). 0x1: Pixel clock only toggles when there is valid data to display (only in active matrix mode).	RW	0

Table 10-404. Register Call Summary for Register DISPC_CONFIG2

Display Controller

- DISPC Transparency Color Keys: [0] [1] [2]
- DISPC Extended 3D Support - Line Alternative Format: [3]
- DISPC Shadow Registers: [4]
- DISPC LCD Output Configuration: [5]
- DISPC Logical Register Mapping: [6]
- DISPC Register Summary: [7]

Table 10-405. DISPC_VID1_ATTRIBUTES2

Address Offset	0x0000 0624		
Physical Address	0x5800 1624	**Instance**	DISPC
Description	The register configures the attributes of the video window 1. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				SUBSAMPLINGPATTERN			YUVCHROMARESAMPLING	RESERVED		VC1_RANGE_CBCR			VC1_RANGE_Y			VC1ENABLE

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Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:9	SUBSAMPLINGPATTERN	Subsampling pattern setting.	RW	0x0
8	YUVCHROMARESAMPLING	The YUV chrominance can be resampled using averaging of the adjacent chrominance samples, without using the polyphase filter for 4:2:2 input or can be calculated using the polyphase filter for 4:2:2/4:2:0. The polyphase filter is mandatory for the 4:2:0 format. This bit controls the order in which the processing is done on the video pipe. 0x0: When input is 4:2:2, the missing chrominance samples are calculated by averaging the adjacent samples if DISPC_VID1_ATTRIBUTES. ROTATION=0 only. Other rotation configurations are not supported. 0x1: For 4:2:2 (or 4:2:0), the missing chrominance samples are calculated by filtering the adjacent samples (5-tap polyphase filter). See Figure 10-42, *Configuration 2: Video Pipeline*. All rotation configurations are supported.	RW	0
7	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
6:4	VC1_RANGE_CBCR	Defines the VC-1 range value for the CbCr component from 0 to 7.	RW	0x0
3:1	VC1_RANGE_Y	Defines the VC-1 range value for the Y component from 0 to 7.	RW	0x0
0	VC1ENABLE	Enable/disable the VC-1 range mapping processing. The bit field is ignored if the format is not one of the supported YUV formats. 0x0: VC-1 range mapping disabled 0x1: VC-1 range mapping enabled	RW	0

Table 10-406. Register Call Summary for Register DISPC_VID1_ATTRIBUTES2

Display Controller

- DISPC Extended 3D Support - DLP 3D Format: [0]
- DISPC Shadow Registers: [1]
- DISPC Logical Register Mapping: [2]
- DISPC Register Summary: [3]

Table 10-407. DISPC_VID2_ATTRIBUTES2

Address Offset	0x0000 0628		
Physical Address	0x5800 1628	**Instance**	DISPC
Description	The register configures the attributes of the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				SUBSAMPLINGPATTERN			YUVCHROMARESAMPLING	RESERVED	VC1_RANGE_CBCR			VC1_RANGE_Y			VC1ENABLE

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Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:9	SUBSAMPLINGPATTERN	Subsampling pattern setting.	RW	0x0
8	YUVCHROMARESAMPLING	The YUV chrominance can be resampled using averaging of the adjacent chrominance samples, without using the polyphase filter for 4:2:2 input or can be calculated using the polyphase filter for 4:2:2/4:2:0. The polyphase filter is mandatory for the 4:2:0 format. This bit controls the order in which the processing is done on the video pipe. 0x0: When input is in 4:2:2, the missing chrominance samples are calculated by averaging the adjacent samples if DISPC_VID1_ATTRIBUTES. ROTATION=0 only. Other rotation configurations are not supported. 0x1: For 4:2:2 (or 4:2:0), the missing chrominance samples are calculated by filtering the adjacent samples (5-tap polyphase filter). See Figure 10-42, *Configuration 2: Video Pipeline*. All rotation configurations are supported.	RW	0
7	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
6:4	VC1_RANGE_CBCR	Defines the VC-1 range value for the CbCr component from 0 to 7.	RW	0x0
3:1	VC1_RANGE_Y	Defines the VC-1 range value for the Y component from 0 to 7.	RW	0x0
0	VC1ENABLE	Enable/disable the VC-1 range mapping processing. The bit field is ignored if the format is not one of the supported YUV formats. 0x0: VC-1 range mapping disabled 0x1: VC-1 range mapping enabled	RW	0

Table 10-408. Register Call Summary for Register DISPC_VID2_ATTRIBUTES2

Display Controller

- DISPC Extended 3D Support - DLP 3D Format: [0]
- DISPC Shadow Registers: [1]
- DISPC Logical Register Mapping: [2]
- DISPC Register Summary: [3]

Table 10-409. DISPC_VID3_ATTRIBUTES2

Address Offset	0x0000 062C		
Physical Address	0x5800 162C	**Instance**	DISPC
Description	The register configures the attributes of the video window 3. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				SUBSAMPLINGPATTERN			YUVCHROMARESAMPLING	RESERVED			VC1_RANGE_CBCR			VC1_RANGE_Y		VC1ENABLE

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Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00000
11:9	SUBSAMPLINGPATTERN	Subsampling pattern setting.	RW	0x0
8	YUVCHROMARE SAMPLING	The YUV chrominance can be resampled using averaging of the adjacent chrominance samples, without using the polyphase filter for 4:2:2 input or can be calculated using the polyphase filter for 4:2:2/4:2:0. The polyphase filter is mandatory for the 4:2:0 format. This bit controls the order in which the processing is done on the video pipe. 0x0: When input is in 4:2:2, the missing chrominance samples are calculated by averaging the adjacent samples if DISPC_VID1_ATTRIBUTES. ROTATION=0 only. Other rotation configurations are not supported. 0x1: For 4:2:2 (or 4:2:0), the missing chrominance samples are calculated by filtering the adjacent samples (5-tap polyphase filter). See Figure 10-42, *Configuration 2: Video Pipeline*. All rotation configurations are supported.	RW	0
7	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
6:4	VC1_RANGE_ CBCR	Defines the VC-1 range value for the CbCr component from 0 to 7.	RW	0x0
3:1	VC1_RANGE_Y	Defines the VC-1 range value for the Y component from 0 to 7.	RW	0x0
0	VC1ENABLE	Enable/disable the VC-1 range mapping processing. The bit field is ignored if the format is not one of the supported YUV formats. 0x0: VC-1 range mapping disabled 0x1: VC-1 range mapping enabled	RW	0

Table 10-410. Register Call Summary for Register DISPC_VID3_ATTRIBUTES2

Display Controller

- DISPC Extended 3D Support - DLP 3D Format: [0]
- DISPC Shadow Registers: [1]
- DISPC Logical Register Mapping: [2]
- DISPC Register Summary: [3]

Table 10-411. DISPC_GAMMA_TABLE0

Address Offset	0x0000 0630		
Physical Address	0x5800 1630	**Instance**	DISPC
Description	The register configures the look up table used as color look up table for BITMAP formats (1-, 2-, 4, and 8-bpp) on the graphics pipeline or as gamma table on the primary LCD output.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDEX								VALUE_R								VALUE_G								VALUE_B							

Bits	Field Name	Description	Type	Reset
31:24	INDEX	Defines the location in the table where the bit field VALUE is stored.	W	0x00
23:16	VALUE_R	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX	W	0x00
15:8	VALUE_G	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX	W	0x00
7:0	VALUE_B	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX	W	0x00

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Table 10-412. Register Call Summary for Register DISPC_GAMMA_TABLE0

Display Controller

- DISPC Shadow Registers: [0]
- DISPC GFX Pipeline Configuration: [1]
- DISPC LCD Output Configuration: [2]
- DISPC Logical Register Mapping: [3]
- DISPC Register Summary: [4]

Table 10-413. DISPC_GAMMA_TABLE1

Address Offset	0x0000 0634		
Physical Address	0x5800 1634	**Instance**	DISPC
Description	The register configures the gamma table on the secondary LCD output.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDEX								VALUE_R								VALUE_G								VALUE_B							

Bits	Field Name	Description	Type	Reset
31:24	INDEX	Defines the location in the table where the bit field VALUE is stored.	W	0x00
23:16	VALUE_R	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX	W	0x00
15:8	VALUE_G	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX	W	0x00
7:0	VALUE_B	8-bit value used to defined the value to store at the location in the table defined by the bit field INDEX	W	0x00

Table 10-414. Register Call Summary for Register DISPC_GAMMA_TABLE1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-415. DISPC_GAMMA_TABLE2

Address Offset	0x0000 0638		
Physical Address	0x5800 1638	**Instance**	DISPC
Description	The register configures the gamma table on the TV output.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INDEX	RESERVED							VALUE_R								VALUE_G								VALUE_B							

Bits	Field Name	Description	Type	Reset
31	INDEX	Setting this bit to 1 resets the internal index counter to zero. Each subsequent access to the register (with the INDEX bit kept at 0) increments the address for the next storage location into the table memory.	W	0
30	RESERVED		W	0

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Bits	Field Name	Description	Type	Reset
29:20	VALUE_R	10-bit color component value to store in the table	W	0x000
19:10	VALUE_G	10-bit color component value to store in the table	W	0x000
9:0	VALUE_B	10-bit color component value to store in the table	W	0x000

Table 10-416. Register Call Summary for Register DISPC_GAMMA_TABLE2

Display Controller

- DISPC Gamma Correction Unit: [0]
- DISPC Shadow Registers: [1]
- DISPC LCD Output Configuration: [2]
- DISPC TV Output Configuration: [3]
- DISPC Logical Register Mapping: [4]
- DISPC Register Summary: [5]

Table 10-417. DISPC_VID1_FIR2

Address Offset	0x0000 063C		
Physical Address	0x5800 163C	**Instance**	DISPC
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 1. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-418. Register Call Summary for Register DISPC_VID1_FIR2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

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Table 10-419. DISPC_VID1_ACCU2_j

Address Offset	0x0000 0640 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1640 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 1 (DISPC_VID1_ACCU2_0 and DISPC_VID1_ACCU2_1 for ping-pong mechanism with external trigger, based on the field polarity) It is used for Cb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from –1024 to 1023).	RW	0x000

Table 10-420. Register Call Summary for Register DISPC_VID1_ACCU2_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-421. DISPC_VID1_FIR_COEF_H2_i

Address Offset	0x0000 0648 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1648 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00

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Bits	Field Name	Description	Type	Reset
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-422. Register Call Summary for Register DISPC_VID1_FIR_COEF_H2_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-423. DISPC_VID1_FIR_COEF_HV2_i

Address Offset	0x0000 064C + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 164C + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
FIRVC2	FIRVC1	FIRVC0	FIRHC4

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-424. Register Call Summary for Register DISPC_VID1_FIR_COEF_HV2_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-425. DISPC_VID1_FIR_COEF_V2_i

Address Offset	0x0000 0688 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1688 + (0x4 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 1 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-426. Register Call Summary for Register DISPC_VID1_FIR_COEF_V2_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-427. DISPC_VID2_FIR2

Address Offset	0x0000 06A8		
Physical Address	0x5800 16A8	**Instance**	DISPC
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 2. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			FIRVINC													RESERVED		FIRHINC													

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Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-428. Register Call Summary for Register DISPC_VID2_FIR2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-429. DISPC_VID2_ACCU2_j

Address Offset	0x0000 06AC + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 16AC + (0x4 * j)	**Instance**	DISPC
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 2 (DISPC_VID2_ACCU2_0 and DISPC_VID2_ACCU2_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for Cb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from –1024 to 1023).	RW	0x000

Table 10-430. Register Call Summary for Register DISPC_VID2_ACCU2_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

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Table 10-431. DISPC_VID2_FIR_COEF_H2_i

Address Offset	0x0000 06B4 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 16B4 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-432. Register Call Summary for Register DISPC_VID2_FIR_COEF_H2_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-433. DISPC_VID2_FIR_COEF_HV2_i

Address Offset	0x0000 06B8 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 16B8 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

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Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-434. Register Call Summary for Register DISPC_VID2_FIR_COEF_HV2_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-435. DISPC_VID2_FIR_COEF_V2_i

Address Offset	0x0000 06F4 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 16F4 + (0x4 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 2 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-436. Register Call Summary for Register DISPC_VID2_FIR_COEF_V2_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-437. DISPC_VID3_FIR2

Address Offset	0x0000 0724		
Physical Address	0x5800 1724	**Instance**	DISPC
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the video window 3. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIRVINC								RESERVED								FIRHINC							

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-438. Register Call Summary for Register DISPC_VID3_FIR2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-439. DISPC_VID3_ACCU2_j

Address Offset	0x0000 0728 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1728 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the video window 3 (DISPC_VID3_ACCU2_0 and DISPC_VID3_ACCU2_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for Cb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from –1024 to 1023).	RW	0x000

Table 10-440. Register Call Summary for Register DISPC_VID3_ACCU2_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Register Summary: [1]

Table 10-441. DISPC_VID3_FIR_COEF_H2_i

Address Offset	0x0000 0730 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1730 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-442. Register Call Summary for Register DISPC_VID3_FIR_COEF_H2_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-443. DISPC_VID3_FIR_COEF_HV2_i

Address Offset	0x0000 0734 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1734 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-444. Register Call Summary for Register DISPC_VID3_FIR_COEF_HV2_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-445. DISPC_VID3_FIR_COEF_V2_i

Address Offset	0x0000 0770 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 1770 + (0x4 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the video window 3 for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

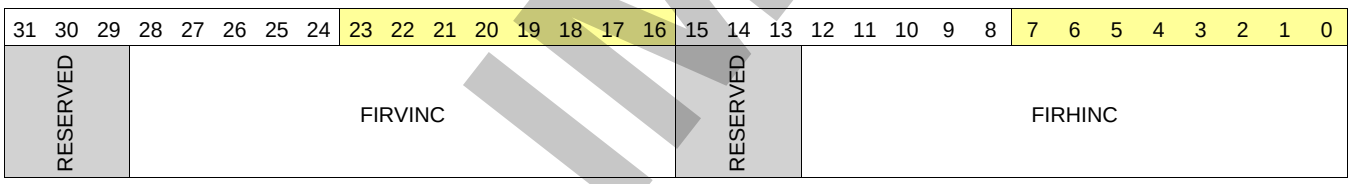
Table 10-446. Register Call Summary for Register DISPC_VID3_FIR_COEF_V2_i

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-447. DISPC_WB_FIR2

Address Offset	0x0000 0790		
Physical Address	0x5800 1790	**Instance**	DISPC
Description	The register configures the resize factors for horizontal and vertical up/downsampling of the write-back pipeline. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
28:16	FIRVINC	Vertical increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
12:0	FIRHINC	Horizontal increment of the up/downsampling filter for Cb and Cr. Encoded value (from 1 to 4096). The value 0 is invalid. The values greater than 4096 are invalid.	RW	0x0400

Table 10-448. Register Call Summary for Register DISPC_WB_FIR2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC WB Pipeline Configuration: [1] [2]
- DISPC Register Summary: [3]

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Table 10-449. DISPC_WB_ACCU2_j

Address Offset	0x0000 0794 + (0x4 * j)	**Index**	j = 0 to 1
Physical Address	0x5800 1794 + (0x4 * j)	**Instance**	DISPC
Description	The register configures the resize accumulator init values for horizontal and vertical up/downsampling of the write back pipeline (DISPC_WB_ACCU2_0 and DISPC_WB_ACCU2_1 for ping-pong mechanism with external trigger, based on the field polarity). It is used for Cb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VERTICALACCU								RESERVED								HORIZONTALACCU							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	VERTICALACCU	Vertical initialization accu value Encoded value (from –1024 to 1023).	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	HORIZONTALACCU	Horizontal initialization accu value Encoded value (from –1024 to 1023).	RW	0x000

Table 10-450. Register Call Summary for Register DISPC_WB_ACCU2_j

Display Controller

- DISPC Shadow Registers: [0]
- DISPC WB Pipeline Configuration: [1] [2]
- DISPC Register Summary: [3]

Table 10-451. DISPC_WB_FIR_COEF_H2_i

Address Offset	0x0000 07A0 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 17A0 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the up/down-scaling coefficients for the horizontal resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRHC3								FIRHC2								FIRHC1								FIRHC0							

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Bits	Field Name	Description	Type	Reset
31:24	FIRHC3	Signed coefficient C3 for the horizontal up/down-scaling with the phase n	RW	0x00
23:16	FIRHC2	Unsigned coefficient C2 for the horizontal up/down-scaling with the phase n	RW	0x00
15:8	FIRHC1	Signed coefficient C1 for the horizontal up/down-scaling with the phase n	RW	0x00
7:0	FIRHC0	Signed coefficient C0 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-452. Register Call Summary for Register DISPC_WB_FIR_COEF_H2_i

Display Controller

- DISPC Scaler Unit: [0] [1] [2] [3] [4]
- DISPC Shadow Registers: [5]
- DISPC WB Pipeline Configuration: [6]
- DISPC Register Summary: [7]

Table 10-453. DISPC_WB_FIR_COEF_HV2_i

Address Offset	0x0000 07A4 + (0x8 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 17A4 + (0x8 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical and horizontal resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRVC2								FIRVC1								FIRVC0								FIRHC4							

Bits	Field Name	Description	Type	Reset
31:24	FIRVC2	Signed coefficient C2 for the vertical up/down-scaling with the phase n	RW	0x00
23:16	FIRVC1	Unsigned coefficient C1 for the vertical up/down-scaling with the phase n	RW	0x00
15:8	FIRVC0	Signed coefficient C0 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRHC4	Signed coefficient C4 for the horizontal up/down-scaling with the phase n	RW	0x00

Table 10-454. Register Call Summary for Register DISPC_WB_FIR_COEF_HV2_i

Display Controller

- DISPC Scaler Unit: [0] [1] [2] [3] [4] [5]
- DISPC Shadow Registers: [6]
- DISPC WB Pipeline Configuration: [7] [8]
- DISPC Register Summary: [9]

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Table 10-455. DISPC_WB_FIR_COEF_V2_i

Address Offset	0x0000 07E0 + (0x4 * i)	**Index**	i = 0 to 7
Physical Address	0x5800 17E0 + (0x4 * i)	**Instance**	DISPC
Description	The bank of registers configure the down/up/down-scaling coefficients for the vertical resize of the video picture associated with the write back pipeline for the phases from 0 to 7. It is used for Crb and Cr setting. It is used only when the pixel format at the input of the filter is one of the YUV formats. If the pixel format at the input of the filter is ARGB (all ARGB, RGB, RGBA are converted to ARGB32-8888 by the color space conversion before going to the filter is the color space conversion is done before the filter). When the register is not used by the hardware, any value can be used for the bit fields. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline) when the WB pipeline is directly connected to one of the pipelines (graphics or video), otherwise updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FIRVC22								FIRVC00							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
15:8	FIRVC22	Signed coefficient C22 for the vertical up/down-scaling with the phase n	RW	0x00
7:0	FIRVC00	Signed coefficient C00 for the vertical up/down-scaling with the phase n	RW	0x00

Table 10-456. Register Call Summary for Register DISPC_WB_FIR_COEF_V2_i

Display Controller

- DISPC Scaler Unit: [0] [1] [2]
- DISPC Shadow Registers: [3]
- DISPC WB Pipeline Configuration: [4]
- DISPC Register Summary: [5]

Table 10-457. DISPC_GLOBAL_BUFFER

Address Offset	0x0000 0800		
Physical Address	0x5800 1800	**Instance**	DISPC
Description	The register configures the DMA buffers allocations to the pipeline (graphics, video1, video2, video3 and write-back). Both TOP and BOTTOM must be allocated to the same pipeline.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WB_BUFFER								VID3_BUFFER								VID2_BUFFER							
																								VID1_BUFFER							
																														GFX_BUFFER	

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Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x0
29:24	WB_BUFFER	Write-back DMA buffer allocation to one of the pipelines. By default to write-back pipeline. 0x24: DMA buffer allocated to the write-back pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x9: DMA buffer allocated to the video1 pipeline. 0x12: DMA buffer allocated to the vdieo2 pipeline. 0x1B: DMA buffer allocated to the vdieo3 pipeline.	RW	0x24
23:18	VID3_BUFFER	Video3 DMA buffer allocation to one of the pipelines. By default to video3 pipeline. 0x24: DMA buffer allocated to the write-back pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x9: DMA buffer allocated to the video1 pipeline. 0x12: DMA buffer allocated to the vdieo2 pipeline. 0x1B: DMA buffer allocated to the vdieo3 pipeline.	RW	0x1B
17:12	VID2_BUFFER	Video2 DMA buffer allocation to one of the pipelines. By default to video2 pipeline. 0x24: DMA buffer allocated to the write-back pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x9: DMA buffer allocated to the video1 pipeline. 0x12: DMA buffer allocated to the vdieo2 pipeline. 0x1B: DMA buffer allocated to the vdieo3 pipeline.	RW	0x12
11:6	VID1_BUFFER	Video1 DMA buffer allocation to one of the pipelines. By default to video 1 pipeline. 0x24: DMA buffer allocated to the write-back pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x9: DMA buffer allocated to the video1 pipeline. 0x12: DMA buffer allocated to the vdieo2 pipeline. 0x1B: DMA buffer allocated to the vdieo3 pipeline.	RW	0x09
5:0	GFX_BUFFER	Graphics DMA buffer allocation to one of the pipelines. By default to graphics pipeline. 0x24: DMA buffer allocated to the write-back pipeline. 0x0: DMA buffer allocated to the graphics pipeline. 0x9: DMA buffer allocated to the video1 pipeline. 0x12: DMA buffer allocated to the vdieo2 pipeline. 0x1B: DMA buffer allocated to the vdieo3 pipeline.	RW	0x00

Table 10-458. Register Call Summary for Register DISPC_GLOBAL_BUFFER

Display Controller

- DISPC DMA Engine: [0]
- DISPC Shadow Registers: [1]
- DISPC Register Summary: [2]
- DISPC Register Description: [3]

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Table 10-459. DISPC_DIVISOR

Address Offset	0x0000 0804		
Physical Address	0x5800 1804	**Instance**	DISPC
Description	The register configures the divisor value for generating the core functional clock. There is a backward compatibility mode enabled by default in order to use DISPC_DIVISOR1.LCD value instead of DISPC_DIVISOR.LCD bit field for generating the core functional clock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LCD								RESERVED															ENABLE

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:16	LCD	Display Controller Logic Clock Divisor Value (from 1 to 255) to specify the frequency of the Display Controller logic clock based on the function clock. The value 0 is invalid.	RW	0x4
15:1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
0	ENABLE	When the bit field is set to 1, the bit field LCD is used to generated the core functional clock from the input clock. When the bit field is set to 0, the value DISPC_DIVISOR1.LCD is used instead. 0x0: DISPC_DIVISOR1.LCD bit field is used 0x1: DISPC_DIVISOR.LCD bit field is used	RW	0

Table 10-460. Register Call Summary for Register DISPC_DIVISOR

Display Controller

- DISPC Clock Configuration: [0]
- DISPC Timing Generator and Panel Settings: [1] [2]
- DISPC Shadow Registers: [3]
- DISPC Register Summary: [4]
- DISPC Register Description: [5] [6]

Table 10-461. DISPC_WB_ATTRIBUTES2

Address Offset	0x0000 0810
Physical Address	0x5800 1810
Description	The register set the counter to control the delay to flush the WB pipe after the end of the frame in capture mode. Shadow register, updated on VFP start period of primary LCD or VFP start period of secondary LCD or VFP start period of the third LCD or EVSYNC depending on which overlay output is selected as an input to the WB pipeline
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WBDELAYCOUNT							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	WBDELAYCOUNT	Delays the WB pipe flush after the end of the frame.delay = n x (1/F_clk) n = 0:255	RW	0x00

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Table 10-462. Register Call Summary for Register DISPC_WB_ATTRIBUTES2

Display Controller

- DISPC WRITE DMA Buffer (WB Pipeline): [0] [1] [2] [3]
- DISPC Shadow Registers: [4] [5] [6] [7] [8] [9]
- DISPC Register Summary: [10]

Table 10-463. DISPC_DEFAULT_COLOR3

Address Offset	0x0000 0814
Physical Address	0x5800 1814
Description	The control register allows to configure the default solid background color for the third LCD. Shadow register, updated on VFP start period of third LCD
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEFAULTCOLOR																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	DEFAULTCOLOR	24-bit RGB color value to specify the default solid color to display when there is no data from the overlays	RW	0x00 0000

Table 10-464. Register Call Summary for Register DISPC_DEFAULT_COLOR3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1] [2]
- DISPC Register Summary: [3]

Table 10-465. DISPC_TRANS_COLOR3

Address Offset	0x0000 0818
Physical Address	0x5800 1818
Description	The register sets the transparency color value for the video/graphics overlays for the third LCD output. Shadow register, updated on VFP start period of the third LCD
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRANSCOLORKEY																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:0	TRANSCOLORKEY	Transparency color key value in RGB format [0] BITMAP 1 (CLUT), [23,1] set to 0s [1:0] BITMAP 2 (CLUT), [23,2] set to 0s [3:0] BITMAP 4 (CLUT), [23,4] set to 0s [7:0] BITMAP 8 (CLUT), [23,8] set to 0s [11:0] RGB 12, [23,12] set to 0s [15:0] RGB 16, [23,16] set to 0s [23:0] RGB 24	RW	0x00 0000

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Table 10-466. Register Call Summary for Register DISPC_TRANS_COLOR3

Display Controller

- DISPC Transparency Color Keys: [0]
- DISPC Shadow Registers: [1]
- DISPC Register Summary: [2]

Table 10-467. DISPC_CPR3_COEF_B

Address Offset	0x0000 081C
Physical Address	0x5800 181C
Description	The register configures the color phase rotation matrix coefficients for the blue component. It is used for the secondary LCD output. Shadow register, updated on VFP start period of third LCD
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR										RESERVED						BG					RESERVED			BB							

Bits	Field Name	Description	Type	Reset
31:22	BR	BR coefficient Encoded signed value (from –512 to 511)	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	BG	BG coefficient Encoded signed value (from –512 to 511)	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	BB	BB coefficient Encoded signed value (from –512 to 511)	RW	0x000

Table 10-468. Register Call Summary for Register DISPC_CPR3_COEF_B

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-469. DISPC_CPR3_COEF_G

Address Offset	0x0000 0820
Physical Address	0x5800 1820
Description	The register configures the color phase rotation matrix coefficients for the green component. It is used for the secondary LCD output. Shadow register, updated on VFP start period of third LCD
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GR										RESERVED						GG					RESERVED			GB							

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Bits	Field Name	Description	Type	Reset
31:22	GR	GRcoefficient Encoded signed value (from –512 to 511)	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	GG	GG coefficient Encoded signed value (from –512 to 511)	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	GB	GB coefficient Encoded signed value (from –512 to 511)	RW	0x000

Table 10-470. Register Call Summary for Register DISPC_CPR3_COEF_G

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-471. DISPC_CPR3_COEF_R

Address Offset	0x0000 0824
Physical Address	0x5800 1824
Description	The register configures the color phase rotation matrix coefficients for the red component. Shadow register, updated on VFP start period of third LCD
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RR										RESERVED						RG								RESERVED							
RB																															

Bits	Field Name	Description	Type	Reset
31:22	RR	RR coefficient Encoded signed value (from –512 to 511)	RW	0x000
21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
20:11	RG	RG coefficient Encoded signed value (from –512 to 511)	RW	0x000
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:0	RB	RB coefficient Encoded signed value (from –512 to 511)	RW	0x000

Table 10-472. Register Call Summary for Register DISPC_CPR3_COEF_R

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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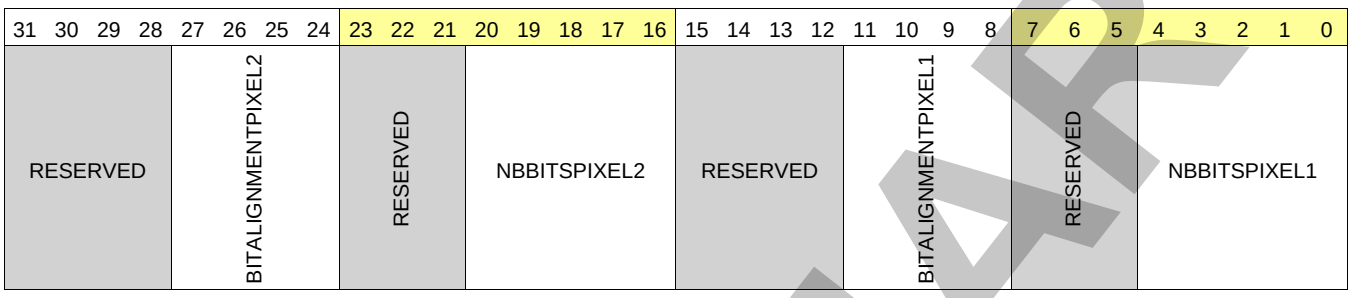
Table 10-473. DISPC_DATA3_CYCLE1

Address Offset	0x0000 0828
Physical Address	0x5800 1828
Description	The control register configures the output data format for the first cycle. Shadow register, updated on VFP start period of third LCD
Type	RW



Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-474. Register Call Summary for Register DISPC_DATA3_CYCLE1

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-475. DISPC_DATA3_CYCLE2

Address Offset	0x0000 082C
Physical Address	0x5800 182C
Description	The control register configures the output data format for the second cycle. Shadow register, updated on VFP start period of third LCD
Type	RW

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31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED / NBBITSPIXEL2	RESERVED / BITALIGNMENTPIXEL1	RESERVED / NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-476. Register Call Summary for Register DISPC_DATA3_CYCLE2

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-477. DISPC_DATA3_CYCLE3

Address Offset	0x0000 0830
Physical Address	0x5800 1830
Description	The control register configures the output data format for the third cycle. Shadow register, updated on VFP start period of third LCD
Type	RW

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED / NBBITSPIXEL2	RESERVED / BITALIGNMENTPIXEL1	RESERVED / NBBITSPIXEL1

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
27:24	BITALIGNMENTPIXEL2	Bit alignment Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
20:16	NBBITSPIXEL2	Number of bits Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11:8	BITALIGNMENTPIXEL1	Bit alignment Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
4:0	NBBITSPIXEL1	Number of bits Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

Table 10-478. Register Call Summary for Register DISPC_DATA3_CYCLE3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-479. DISPC_SIZE_LCD3

Address Offset	0x0000 0834
Physical Address	0x5800 1834
Description	The register configures the panel size (horizontal and vertical). It is used for the third LCD output. Shadow register, updated on VFP start period of the third LCD. A delta value is used to indicate if the odd field is the same vertical size as the even field or ± one line.
Type	RW

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	LPP		DELTA_LPP	RESERVED	PPL	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:16	LPP	Lines per panel Encoded value (from 1 to 4096) to specify the number of lines per panel (program to value minus 1).	RW	0x000
15:14	DELTA_LPP	Indicates the delta size value of the odd field compared to the even field 0x0: Same size 0x1: Odd size = even size +1 0x2: Odd size = even size –1	RW	0x0
13:12	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
11:0	PPL	Pixels per line Encoded value (from 1 to 4096) to specify the number of pixels contained within each line on the display (program to value minus 1). In STALL mode, any value is valid. In non-STALL mode, only values of multiples of 8 pixels are valiid.	RW	0x000

Table 10-480. Register Call Summary for Register DISPC_SIZE_LCD3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1] [2]
- DISPC Register Summary: [3]

Table 10-481. DISPC_DIVISOR3

Address Offset	0x0000 0838
Physical Address	0x5800 1838
Description	The register configures the divisors. It is used for the third LCD output. Shadow register, updated on VFP start period of the third LCD
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LCD								RESERVED								PCD							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
23:16	LCD	Display controller logic clock divisor Value (from 1 to 255) to specify the intermediate pixel clock frequency based on LCD2_CLK. The value 0 is invalid.	RW	0x04
15:8	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
7:0	PCD	Pixel clock divisor Value (from 1 to 255) to specify the frequency of the pixel clock based on LCD2_CLK divided by the value of DISPC_DIVISOR2.LCD. The value 0 is invalid.	RW	0x01

Table 10-482. Register Call Summary for Register DISPC_DIVISOR3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-483. DISPC_POL_FREQ3

Address Offset	0x0000 083C
Physical Address	0x5800 183C
Description	The register configures the signal configuration. It is used for the third LCD output. Shadow register, updated on VFP start period of the third LCD
Type	RW

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ALIGN	ONOFF	RF	IEO	IPC	IHS	IVS	ACBI				ACB							

Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000
18	ALIGN	Defines the alignment betwwen HSYNC and VSYNC assertion 0x0: VSYNC and HSYNC are not aligned. 0x1: VSYNC and HSYNC assertions are aligned.	RW	0
17	ONOFF	HSYNC/VSYNC pixel clock control on/off 0x0: HSYNC and VSYNC are driven on opposite edges of the pixel clock than pixel data. 0x1: HSYNC and VSYNC are driven according to bit 16.	RW	0
16	RF	Program HSYNC/VSYNC rise or fall 0x0: HSYNC and VSYNC are driven on the falling edge of the pixel clock (if bit 17 is set to 1). 0x1: HSYNC and VSYNC are driven onthe rising edge of the pixel clock (if bit 17 is set to 1).	RW	0
15	IEO	Invert output enable 0x0: Ac-bias is active high (active display mode). 0x1: Ac-bias is active low (active display mode).	RW	0
14	IPC	Invert pixel clock 0x0: Data is driven on the LCD data lines on the rising edge of the pixel clock. 0x1: Data is driven on the LCD data lines on the falling edge of the pixel clock.	RW	0
13	IHS	Invert HSYNC 0x0: Line clock pin is active high and inactive low. 0x1: Line clock pin is active low and inactive high.	RW	0
12	IVS	Invert VSYNC 0x0: Frame clock pin is active high and inactive low. 0x1: Frame clock pin is active low and inactive high.	RW	0
11:8	ACBI	AC bias pin transitions per interrupt Value (from 0 to 15) used to specify the number of AC bias pin transitions	RW	0x0
7:0	ACB	AC bias pin frequency Value (from 0 to 255) used to specify the number of line clocks to count before transitioning the AC bias pin. This pin is used to periodically invert the polarity of the power supply to prevent DC charge buildup within the display.	RW	0x00

Table 10-484. Register Call Summary for Register DISPC_POL_FREQ3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

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Table 10-485. DISPC_TIMING_H3

Address Offset	0x0000 0840
Physical Address	0x5800 1840
Description	The register configures the timing logic for the HSYNC signal. It is used for the third LCD output. Shadow register, updated on VFP start period of the third LCD
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HBP																HFP								HSW							

Bits	Field Name	Description	Type	Reset
31:20	HBP	Horizontal back porch Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the beginning of a line transmission before the first set of pixels is output to the display (program to value minus 1).	RW	0x000
19:8	HFP	Horizontal front porch Encoded value (from 1 to 4096) to specify the number of pixel clock periods to add to the end of a line transmissionbefore the line clock is asserted.	RW	0x000
7:0	HSW	Horizontal synchronization pulse width Encoded value (from 1 to 256) to specify the number of pixel clock periods to pulse the line clock at the end of each line (program to value minus 1).	RW	0x00

Table 10-486. Register Call Summary for Register DISPC_TIMING_H3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-487. DISPC_TIMING_V3

Address Offset	0x0000 0844
Physical Address	0x5800 1844
Description	The register configures the timing logic for the VSYNC signal. It is used for the third LCD output. Shadow register, updated on VFP start period of the third LCD
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBP																VFP								VSW							

Bits	Field Name	Description	Type	Reset
31:20	VBP	Vertical back porch Encoded value (from 0 to 4095) to specify the number of line clock periods to add to the beginning of a frame before the first set of pixels is output to the display	RW	0x000
19:8	VFP	Vertical front porch Encoded value (from 0 to 4095) to specify the number of line clock periods to add to the end of each frame	RW	0x000
7:0	VSW	Vertical synchronization pulse width In active mode, encoded value (from 1 to 256) to specify the number of line clock periods to pulse the frame clock (VSYNC) pin at the end of each frame after the end of frame wait (VFP) period elapses. Frame clock uses as VSYNC signal in active mode.	RW	0x00

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Table 10-488. Register Call Summary for Register DISPC_TIMING_V3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC Logical Register Mapping: [1]
- DISPC Register Summary: [2]

Table 10-489. DISPC_CONTROL3

Address Offset	0x0000 0848
Physical Address	0x5800 1848
Description	The control register configures the display controller module for the third LCD output.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPATIALTEMPORALDITHERINGFRAMES		RESERVED			TDMUNUSEDBITS		TDMCYCLEFORMAT		TDMPARALLELMODE		TDMENABLE	RESERVED						RESERVED	OVERLAYOPTIMIZATION	STALLMODE	RESERVED	TFTDATALINES		STDITHERENABLE	RESERVED	GOLCD	M8B	STNTFT	MONOCOLOR	RESERVED	LCDENABLE

Bits	Field Name	Description	Type	Reset
31:30	SPATIALTEMPORALDITHERINGFRAMES	Spatial/temporal dithering number of frames for the third LCD output wr: VFP start period of the third LCD output 0x0: Spatial only 0x1: Spatial and temporal over two frames 0x3: Reserved 0x2: Spatial and temporal over four frames	RW	0x0
29:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
26:25	TDMUNUSEDBITS	State of unused bits (TDM mode only) for the third LCD output wr: VFP start period of the third LCD output 0x0: Low level (0) 0x1: High level (1) 0x3: Reserved 0x2: Unchanged from previous state	RW	0x0
24:23	TDMCYCLEFORMAT	Cycle format (TDM mode only) for the third LCD output wr: VFP start period of third LCD output 0x0: One cycle for 1 pixel 0x1: Two cycles for 1 pixel 0x3:Three cycles for 2 pixels 0x2: Three cycles for 1 pixel	RW	0x0

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Bits	Field Name	Description	Type	Reset
22:21	TDMPARALLELMODE	Output interface width (TDM mode only) for the third LCD output wr: VFP start period of the third LCD output 0x0: 8-bit parallel output interface selected 0x1: 9-bit parallel output interface selected 0x3: 16-bit parallel output interface selected 0x2: 12-bit parallel output interface selected	RW	0x0
20	TDMENABLE	Enable the multiple cycle format (TDM mode only used for Active matrix mode with the RFBI enable bit off) for the third LCD output wr: VFP start period of third LCD output 0x0: TDM disabled 0x1: TDM enabled	RW	0
19:14	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
13	RESERVED	Reserved	R	0
12	OVERLAYOPTIMIZATION	Overlay optimization for the third LCD output wr: VFP or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output, or write-back to the memory. 0x0: All the data for all the enabled pipelines are fetched from memory regardless of the overlay/alpha blending configuration. 0x1: The data not used by the overlay manager because of overlap between layers with no alpha blending between them must not be fetched from memory to optimize the bandwidth.	RW	0
11	STALLMODE	STALL mode for the third LCD output wr: VFP start period of the third LCD output 0x0: Normal mode selected 0x1: STALL mode selected. The display controller sends the data without considering the VSYNC/HSYNC. The LCD output is disabled at the end of the transfer of the frame. Software must reenable the LCD output to generate a new frame.	RW	0
10	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
9:8	TFTDATALINES	Number of lines of the third LCD interface wr: VFP start period of the third LCD output 0x0: 12-bit output aligned on the LSB of the pixel data interface 0x1: 16-bit output aligned on the LSB of the pixel data interface 0x3: 24-bit output aligned on the LSB of the pixel data interface 0x2: 18-bit output aligned on the LSB of the pixel data interface	RW	0x0
7	STDITHERENABLE	Spatial temporal dithering enable for the third LCD output wr: VFP start period of the third LCD output 0x0: Spatial/temporal dithering logic disabled 0x1: Spatial/temporal dithering logic enabled	RW	0
6	RESERVED	Reserved	R	0

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Bits	Field Name	Description	Type	Reset
5	GOLCD	GO command for the third LCD output. It is used to synchronized the pipelines (graphics and/or video) associated with the third LCD output. wr: Immediate 0x0: The hardware has finished updating the internal shadow registers of the pipeline(s) connected to the LCD output using the user values. The hardware resets the bit when the update is complete. 0x1: The user has finished programming the shadow registers of the pipeline(s) associated with the LCD output, and the hardware can update the internal registers at the VFP start period.	RW	0
4	M8B	Mono 8-bit mode of the third LCD wr: VFP start period of the third LCD output 0x0: Reserved 0x1: Reserved	RW	0
3	STNTFT	LCD Display type of the third LCD wr: VFP start period of the third LCD output 0x0: Reserved 0x1: Active matrix display operation enabled	RW	0
2	MONOCOLOR	Monochrome/color selection for the third LCD wr: VFP start period of the third LCD output 0x0: Reserved 0x1: Reserved	RW	0
1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
0	LCDENABLE	Enable the third LCD output wr: Immediate 0x0: LCD output disabled (at the end of the frame when the bit is reset) 0x1: LCD output enabled	RW	0

Table 10-490. Register Call Summary for Register DISPC_CONTROL3

Display Controller

- DISPC Graphics Pipeline: [0] [1]
- DISPC Video Pipelines: [2] [3]
- DISPC Overlay Optimization: [4]
- DISPC Shadow Registers: [5] [6]
- DISPC Logical Register Mapping: [7]
- DISPC Register Summary: [8]

Table 10-491. DISPC_CONFIG3

Address Offset	0x0000 084C
Physical Address	0x5800 184C
Description	The control register configures the display controller module for the third LCD output. Shadow register, updated on VFP start period of the third LCD or EVSYNC
Type	RW

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31 30 29 28	27 26	25	24	23	22	21	20	19 18 17 16	15	14 13 12	11	10	9	8	7	6	5	4	3 2 1	0
RESERVED	TLCDINTERLEAVE	FULLRANGE	COLORCONVENABLE	FIDFIRST	OUTPUTMODEENABLE	BT1120ENABLE	BT656ENABLE	RESERVED	BUFFERHANDCHECK	CPR	RESERVED	TCKLCDSELECTION	TCKLCDENABLE	RESERVED	ACBIASGATED	VSYNCGATED	HSYNCGATED	PIXELCLOCKGATED	PIXELDATAGATED	RESERVED	PIXELGATED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x0
27:26	TLCDINTERLEAVE	tLCD interleave Pattern	RW	0x0
25	FULLRANGE	Color space conversion full range setting 0x0: Limited range selected 0x1: Full range selected	RW	0
24	COLORCONVENABLE	Enable the color space conversion. It must be reset when the CPR bit field is set to 0x1. 0x0: Disable color space conversion RGB to YUV. 0x1: Enable color space conversion RGB to YUV.	RW	0
23	FIDFIRST	Selects the first field to output in case of interlace mode. In case of progressive mode, the value is not used. 0x0: First field is even. 0x1: Odd field is first.	RW	0
22	OUTPUTMODEENABLE	Selects between progressive and interlace mode for the third LCD output 0x0: Progressive mode selected 0x1: Interlace mode selected	RW	0
21	BT1120ENABLE	Selects BT-1120 format on the third LCD output. It is not posssible to enable BT-656 and BT-1120 at the same time on the same LCD output. 0x0: BT-1120 is disabled. 0x1: BT-1120 is enabled.	RW	0
20	BT656ENABLE	Selects BT-656 format on the third LCD output. It is not posssible to enable BT656 and BT1120 at the same time on the same LCD output. 0x0: BT-656 is disabled. 0x1: BT-656 is enabled.	RW	0
19:17	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
16	BUFFERHANDCHECK	Controls the handscheck between the DMA buffer and the STALL signal to prevent from underflow. The bit must be set to 0 when the module is not in STALL mode (third LCD output). 0x0: Only the STALL signal (generated by RFBI or DSI1_C, depending on which IP uses the LCD output) is used regardless of the DMA buffer fullness information to provide data to the RFBI or DSI1_C module. 0x1: The STALL signal (generated by RFBI or DSI1_C depending on which IP uses the LCD output) is used in combination with the DMA buffer fullness information to provide data to the RFBI or DSI1_C module only when it does not generate buffer underflow.	RW	0

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Bits	Field Name	Description	Type	Reset
15	CPR	Color phase rotation control (third LCD output). It must be reset when the ColorConvEnable bit field is set to 1. wr: VFP start period of the third LCD output 0x0: Color phase rotation disabled 0x1: Color phase rotation enabled	RW	0
14:12	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
11	TCKLCDSELECTION	Transparency color key selection (third LCD output) wr: VFP start period of the third LCD output 0x0: Destination transparency color key selected 0x1: Source transparency color key selected	RW	0
10	TCKLCDENABLE	Transparency color key enabled (third LCD output) wr: VFP start period of the third LCD output 0x0: Disable the transparency color key for the LCD 0x1: Enable the transparency color key for the LCD	RW	0
9	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
8	ACBIASGATED	ACBias gated enabled (third LCD output) wr: VFP start period of the third LCD output 0x0: AcBias gated disabled 0x1: AcBias gated enabled	RW	0
7	VSYNCGATED	VSYNC gated enabled (third LCD output) wr: VFP start period of the third LCD output 0x0: VSYNC gated disabled 0x1: VSYNC gated enabled	RW	0
6	HSYNCGATED	HSYNC gated enabled (third LCD output) wr: VFP start period of the third LCD output 0x0: HSYNC gated disabled 0x1: HSYNC gated enabled	RW	0
5	PIXELCLOCKGATED	Pixel clock gated enabled (third LCD output) wr: VFP start period of the third LCD output 0x0: Pixel clock gated disabled 0x1: Pixel clock gated enabled	RW	0
4	PIXELDATAGATED	Pixel data gated enabled (third LCD output) wr: VFP start period of the third LCD output 0x0: Pixel data gated disabled 0x1: Pixel data gated enabled	RW	0
3:1	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0
0	PIXELGATED	Pixel gated enable (only for TFT) (third LCD output) wr: VFP start period of the third LCD output 0x0: Pixel clock always toggles (only in TFT mode). 0x1: Pixel clock toggles only when there is valid data to display (only in TFT mode).	RW	0

Table 10-492. Register Call Summary for Register DISPC_CONFIG3

Display Controller

- DISPC Transparency Color Keys: [0] [1] [2]
- DISPC Extended 3D Support - Line Alternative Format: [3]
- DISPC Shadow Registers: [4]
- DISPC LCD Output Configuration: [5]
- DISPC Logical Register Mapping: [6]
- DISPC Register Summary: [7]

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Table 10-493. DISPC_GAMMA_TABLE3

Address Offset	0x0000 0850
Physical Address	0x5800 1850
Description	The register configures the gamma table on the third LCD output.
Type	W

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
INDEX	VALUE_R	VALUE_G	VALUE_B

Bits	Field Name	Description	Type	Reset
31:24	INDEX	Defines the location in the table where the VALUE bit field is stored.	W	0x00
23:16	VALUE_R	8-bit value used to define the value to store at the location in the table defined by the INDEX bit field	W	0x00
15:8	VALUE_G	8-bit value used to define the value to store at the location in the table defined by the INDEX bit field	W	0x00
7:0	VALUE_B	8-bit value used to define the value to store at the location in the table defined by the INDEX bit field	W	0x00

Table 10-494. Register Call Summary for Register DISPC_GAMMA_TABLE3

Display Controller

- DISPC Shadow Registers: [0]
- DISPC LCD Output Configuration: [1]
- DISPC Logical Register Mapping: [2]
- DISPC Register Summary: [3]

Table 10-495. DISPC_BA0_FLIPIMMEDIATE_EN

Address Offset	0x0000 0854		
Physical Address	0x5800 1854	**Instance**	DISPC
Description	Thsi regster enables the flip immediate.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3	2	1	0
RESERVED				VID3	VID2	VID1	GFX

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved.	R	0x000 0000
3	VID3	Enable flip immediate for video3 pipeline	RW	0x0
2	VID2	Enable flip immediate for video2 pipeline	RW	0x0
1	VID1	Enable flip immediate for video1 pipeline	RW	0x0
0	GFX	Enable flip immediate for gfx pipeline	RW	0x0

Table 10-496. Register Call Summary for Register DISPC_BA0_FLIPIMMEDIATE_EN

Display Controller

- DISPC Immediate Base Address Flip Mechanism: [0] [1]
- DISPC Register Summary: [2]

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Table 10-497. DISPC_GLOBAL_MFLAG_ATTRIBUTE

Address Offset	0x0000 085C		
Physical Address	0x5800 185C	**Instance**	DISPC
Description	Global MFLAG atrribute control register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MFLAG_START	MFLAG_CTRL	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved.	R	0x0000 0000
2	MFLAG_START	MFLAG Start 0x0: When the DMA buffer is empty at the beginning of the frame, MFLAG signal of each pipeline is kept at 0 until PRELOAD is reached, then based on MFLAG_CTRL bitfield MFLAG is generated and internal logic is arbitrating between pipeline requests 0x1: Even at the beginning of the frame when the DMA buffer is empty, MFLAG_CTRL bitfield is used to determine how MFLAG signal for each pipeline shall be driven.	RW	0x0
1:0	MFLAG_CTRL	MFLAG control 0x0: MFLAG mechanism is disabled: MFLAG out of band signal is set to 0 0x1: MFLAG mechanism is enabled: MFLAG out of band signal is always set to 1 (force mode for debug) 0x2: MFLAG mechanism is enabled and MFLAG out of band signal is dynamically set and reset depending on MFLAG rules.	RW	0x0

Table 10-498. Register Call Summary for Register DISPC_GLOBAL_MFLAG_ATTRIBUTE

Display Controller

- DISPC MFLAG Mechanism and Arbitration: [0] [1] [2] [3] [4]
- DISPC Shadow Registers: [5]
- DISPC Register Summary: [6]

Table 10-499. DISPC_GFX_MFLAG_THRESHOLD

Address Offset	0x0000 0860		
Physical Address	0x5800 1860	**Instance**	DISPC
Description	MFLAG thresholds for graphics pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or external VSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT_MFLAG																LT_MFLAG															

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Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	High Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches HT_MFLAG level, MFLAG is reset to 0	RW	0x0000
15:0	LT_MFLAG	Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is set to 1	RW	0x0000

Table 10-500. Register Call Summary for Register DISPC_GFX_MFLAG_THRESHOLD

Display Controller

- DISPC MFLAG Mechanism and Arbitration: [0] [1]
- DISPC Shadow Registers: [2]
- DISPC Register Summary: [3]

Table 10-501. DISPC_VID1_MFLAG_THRESHOLD

Address Offset	0x0000 0864		
Physical Address	0x5800 1864	**Instance**	DISPC
Description	MFLAG thresholds for video1 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or external VSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT_MFLAG																LT_MFLAG															

Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	High Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches HT_MFLAG level, MFLAG is reset to 0	RW	0x0000
15:0	LT_MFLAG	Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is set to 1	RW	0x0000

Table 10-502. Register Call Summary for Register DISPC_VID1_MFLAG_THRESHOLD

Display Controller

- DISPC MFLAG Mechanism and Arbitration: [0] [1]
- DISPC Shadow Registers: [2]
- DISPC Register Summary: [3]

Table 10-503. DISPC_VID2_MFLAG_THRESHOLD

Address Offset	0x0000 0868		
Physical Address	0x5800 1868	**Instance**	DISPC
Description	MFLAG thresholds for video2 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or external VSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT_MFLAG																LT_MFLAG															

Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	High Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches HT_MFLAG level, MFLAG is reset to 0	RW	0x0000
15:0	LT_MFLAG	Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is set to 1	RW	0x0000

Table 10-504. Register Call Summary for Register DISPC_VID2_MFLAG_THRESHOLD

Display Controller

- DISPC MFLAG Mechanism and Arbitration: [0] [1]
- DISPC Shadow Registers: [2]
- DISPC Register Summary: [3]

Table 10-505. DISPC_VID3_MFLAG_THRESHOLD

Address Offset	0x0000 086C		
Physical Address	0x5800 186C	**Instance**	DISPC
Description	MFLAG thresholds for video3 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or external VSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT_MFLAG																LT_MFLAG															

Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	High Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches HT_MFLAG level, MFLAG is reset to 0	RW	0x0000
15:0	LT_MFLAG	Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is set to 1	RW	0x0000

Table 10-506. Register Call Summary for Register DISPC_VID3_MFLAG_THRESHOLD

Display Controller

- DISPC MFLAG Mechanism and Arbitration: [0]
- DISPC Shadow Registers: [1]
- DISPC Register Summary: [2]

Table 10-507. DISPC_WB_MFLAG_THRESHOLD

Address Offset	0x0000 0870		
Physical Address	0x5800 1870	**Instance**	DISPC
Description	MFLAG thresholds for write-back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline), when the WB pipeline is directly connected to one of the pipelines (graphics or video). Otherwise, updated on VFP start period of primary LCD or VFP start period of secondary LCD or external VSYNC, depending on which overlay output is selected as an input to the WB pipeline.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT_MFLAG																LT_MFLAG															

Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	High Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches HT_MFLAG level, MFLAG is reset to 0	RW	0x0000
15:0	LT_MFLAG	Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is set to 1	RW	0x0000

Table 10-508. Register Call Summary for Register DISPC_WB_MFLAG_THRESHOLD

Display Controller

- DISPC MFLAG Mechanism and Arbitration: [0] [1] [2]
- DISPC Shadow Registers: [3]
- DISPC Register Summary: [4]

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10.3 MIPI Display Serial Interface

This section describes the MIPI® display serial interface (DSI) module for the device.

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10.3.1 DSI Overview

The DSI module connects to a DSI display module directly or through an external DSI bridge. The DSI module is connected to DISPC and L3_MAIN interconnect.

Figure 10-92 is a block diagram of the DSI module.

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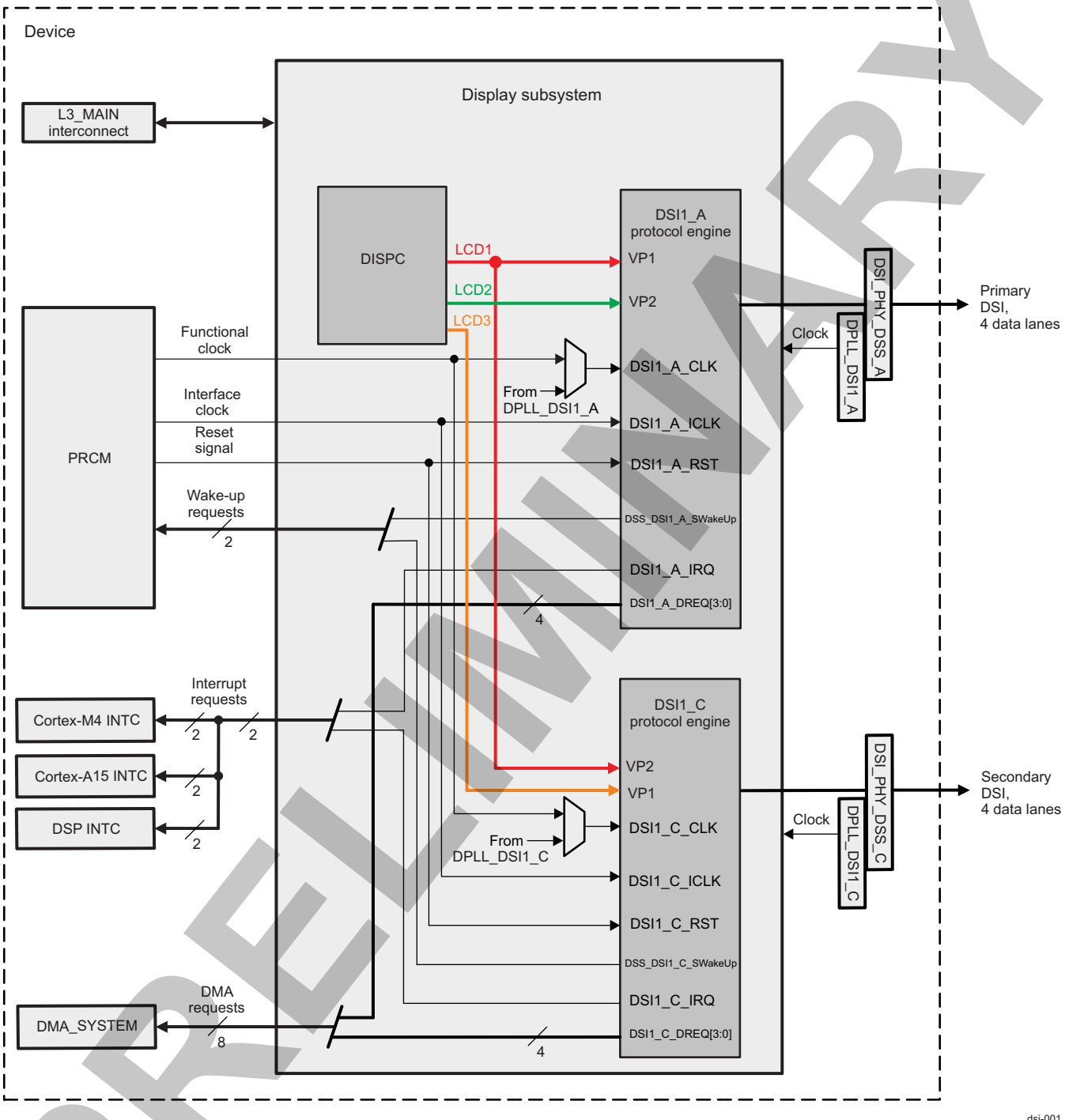
Figure 10-92. DSI Overview



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Two DSI modules in the display subsystem provide the following main features:

- MIPI-DSI support (up to four data lanes and one clock lane)
- Video mode and command mode support
- Multiple display (one video mode and one command mode) support. In command mode, pixel data are provided from the level 3 (L3_MAIN) interface or from one of the overlay manager outputs.
- Bidirectional data link support for command mode (only one data lane is used in reverse direction)
- RGB16, RGB18 nonpacked, and RGB24 format support for command mode

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- RGB16, RGB18 packed and nonpacked, and RGB24 format support for video mode
- Burst support for video mode
- Up to four data-configurable lane support, in addition to clock signaling
- Maximum data rate of 1256 Mbps per data pair for four-data lane configuration (627.75MHz at OPP_NOM.)
- Data splitter for 2-, 3-, and 4-data lane configurations
- Data interleaving support for one synchronous stream (video mode) from the DISPC and up to three asynchronous streams (command mode) from the interconnect concurrently, or up to four asynchronous streams (command mode) from the interconnect
- Transfer of pixels and data received on the video port or L3_MAIN interconnect to the display through DSI_PHY_DSS_x
- Serial configuration port (SCP) for the DSI_PHY_DSS_x complex input/output (I/O) and DSI phase-locked loop (PLL)
- Connection to the DSI_PHY_DSS_x DSI PHY through PPI (*MIPI D-PHY Specification v1.01.00 Revision 0.02 compliant*)
- Error-correction code (ECC) and checksum generation
- MIPI DCS support

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10.3.2 DSI Environment

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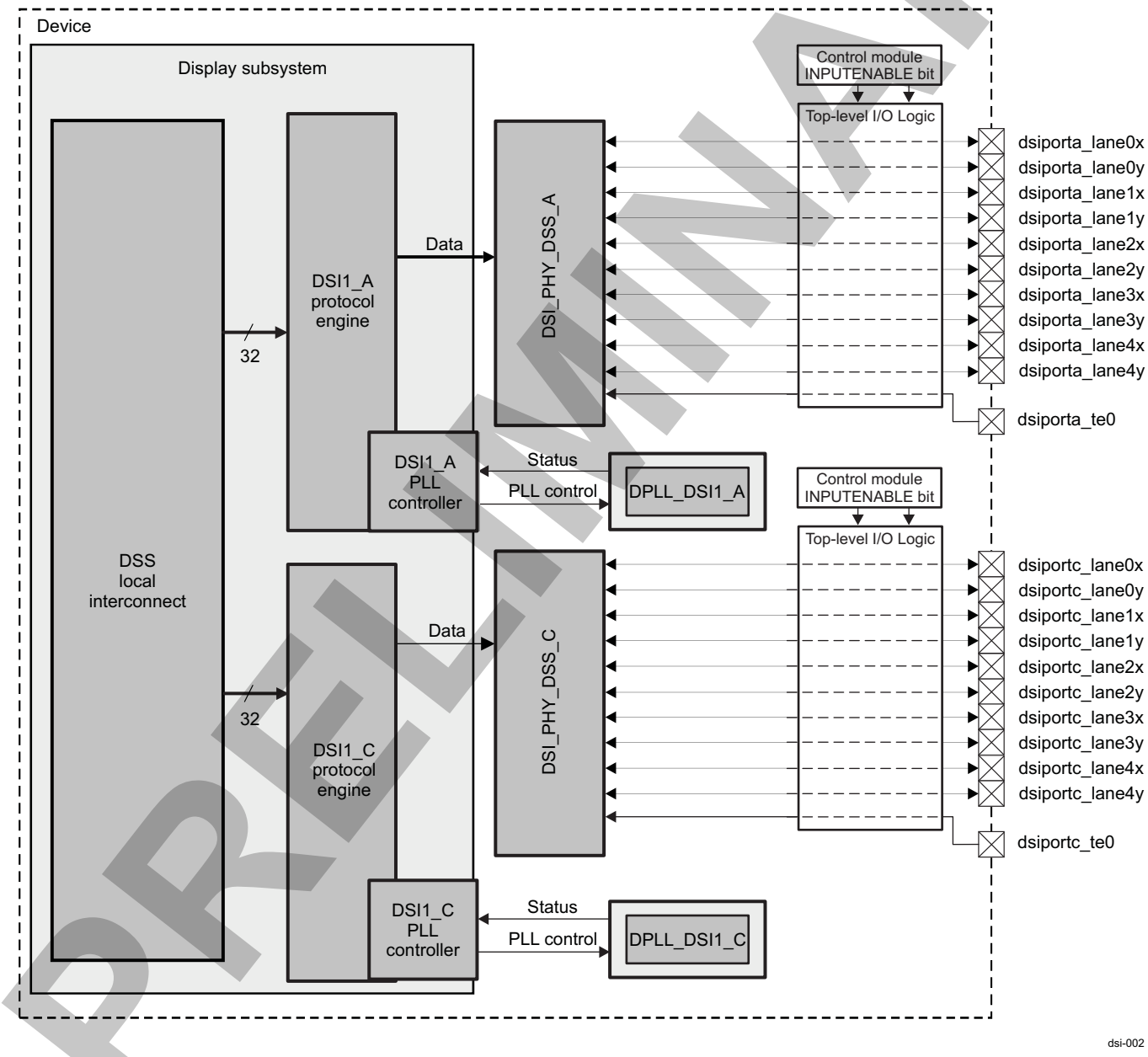
This section describes the DSI application fields from an environment point of view (external connections). It describes the DSI connectivity options, lists all possible interfaces, and describes the protocol and data format used in each case.

Figure 10-93 is a block diagram of the DSI environment.

Figure 10-93. DSI Environment



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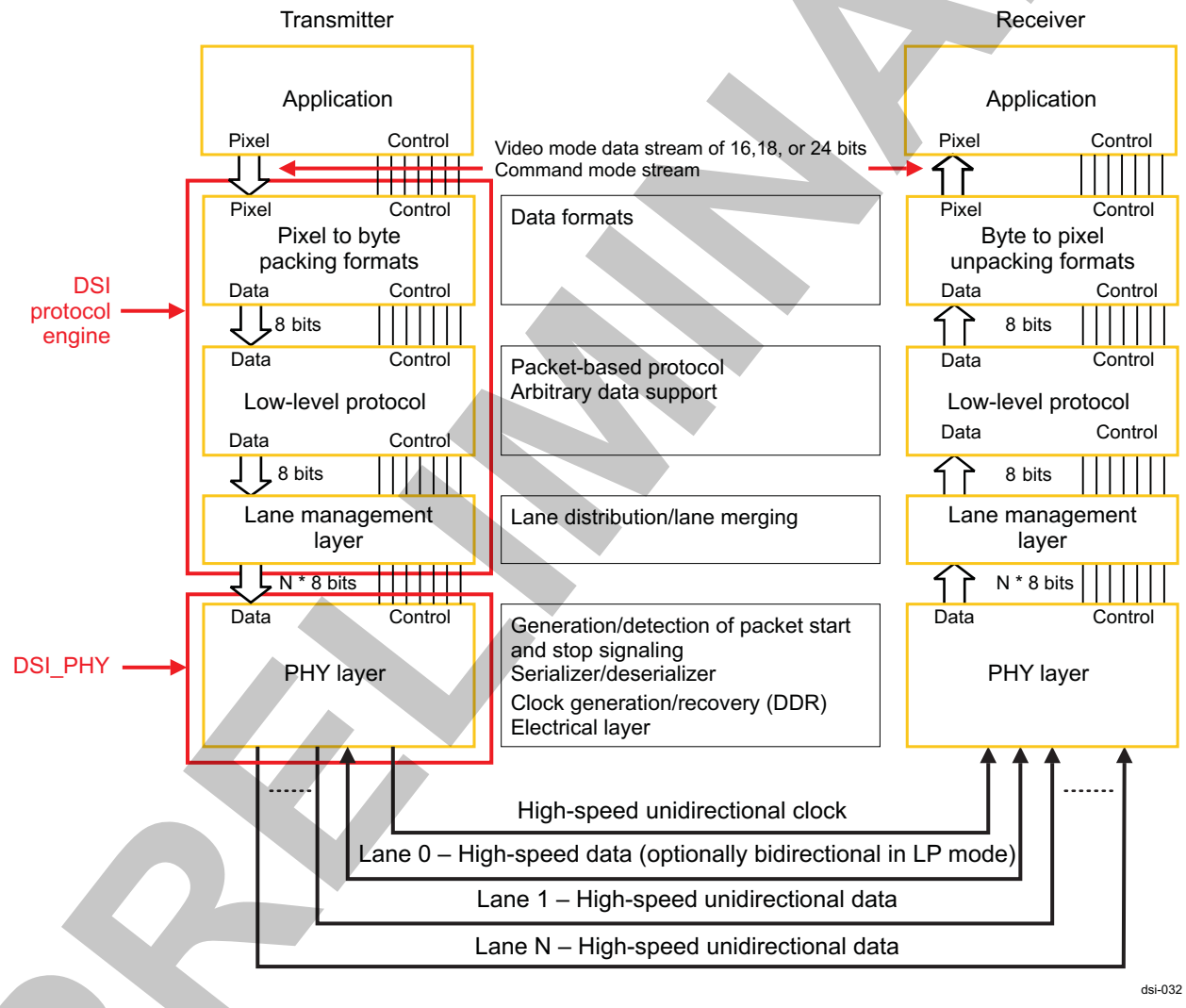
NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and is programmable in the control module registers and dedicated IP registers. For more information, see , *Pad Functional Multiplexing and Configuration*, and , *Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*.

The DSI is a bidirectional differential serial interface with data/clock for the PHY (configured in unidirectional link in case the display module is only unidirectional). The maximum capacity of a DSI data transfer is 1255.5 Mbps for four data lanes. The speed of the link can be configured by software only when the DSI_PHY_DSS_x is in STOP state or ultralow-power state (ULPS).

Figure 10-94 shows the high-level data flow of the DSI transmitter/receiver.

Figure 10-94. DSI Transmitter/Receiver Data Flow



10.3.2.1 DSI PHY

Table 10-509 lists the DSI1_A and DSI1_C I/Os.

Table 10-509. DSI I/O Description of DSI1_A and DSI1_C

Signal Name		I/O[1]	Description	Value at Reset
dsi1portx_dx0	first lane	I/O	Serial data/clock lane	N/A

(1) I = Input; O = Output; I/O = Bidirectional

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Table 10-509. DSI I/O Description of DSI1_A and DSI1_C (continued)

Signal Name		I/O[1]	Description	Value at Reset
dsi1portx_dy0				
dsi1portx_dx1 dsi1portx_dy1	second lane	I/O	Serial data/clock lane	N/A
dsi1portx_dx2 dsi1portx_dy2	third lane	I/O	Serial data/clock lane	N/A
dsi1portx_dx3 dsi1portx_dy3	fourth lane	I/O	Serial data/clock lane	N/A
dsi1portx_dx4 dsi1portx_dy4	fifth lane	I/O	Serial data lane only	N/A
dsi1portx_te0	te0	I	DSI1 tearing effect (TE) input 0	N/A

NOTE: Each serial lane can be used as a data lane. The first through fourth can be used as clock lanes (the fifth lane can never be the clock lane). All polarities on all lanes are supported. The MIPI DSI 1.01 protocol requires at least one clock lane and one data lane.

Lanes support four operating modes:

- HS mode: High-speed transmit mode
- LP mode: Low-power transmit mode (also called low-power state [LPS])
- ULPS: Ultralow-power state used between two transmissions
- Off mode: Lane is off.

NOTE: The CONTROL_DSIPHY register in the control module of the device provides the following control over the DSI lanes:

- Enable and disable each lane (the CONTROL_DSIPHY[28:24] DSIPORTA_LANEENABLE and CONTROL_DSIPHY[23:19] DSIPORTC_LANEENABLE bit fields).

For more information, see SYSCTRL_PADCONF_CORE Register Summary, in *Control Module*.

10.3.2.1.1 DSI Data/Clock Configuration

Data-clock signaling consists of one to four data pairs and one clock pair. The minimum configuration is one data pair and one clock pair.

- The data signal carries the bit serial data. The DSI transmitter in the host sends the data in-quadrature with the dual data rate (DDR) clock in HS mode; otherwise, the clock is extracted from the received data in LS mode. The data is transmitted byte-wise least-significant bit (LSB) first.
- The clock signal carries the DDR clock signal in HS transmission.
- Software users must configure the order of the data lanes to indicate the byte order while splitting the byte stream for each DSI_PHY_DSS_x into bytes.

Table 10-510 lists some of the DSI lane configurations.

NOTE: All combinations for the order of the clock and data lanes are supported (except clock cannot be on lane 5) but not explicitly described in Table 10-510.

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Table 10-510. DSI Lane Configuration

DSI_PHY_DSS_x Lane Configuration	Data/Clock Lane Position					Description
	1	2	3	4	5	
Mode CLK + DATA1						Single data lane
	CLK	DATA1				
	DATA1	CLK				
Mode CLK + DATA1 + DATA2						Two data lanes
	CLK	DATA1	DATA2			
	CLK	DATA2	DATA1			
	DATA1	CLK	DATA2			
	DATA2	CLK	DATA1			
	DATA1	DATA2	CLK			
	DATA2	DATA1	CLK			
Mode CLK + DATA1 + DATA2 + DATA3						Three data lanes
	CLK	DATA1	DATA2	DATA3		
	CLK	DATA3	DATA2	DATA1		
	DATA1	CLK	DATA2	DATA3		
	DATA1	CLK	DATA3	DATA2		
	DATA2	CLK	DATA1	DATA3		
	DATA2	CLK	DATA3	DATA1		
	DATA3	CLK	DATA1	DATA2		
	DATA3	CLK	DATA2	DATA1		
	DATA3	DATA1	CLK	DATA2		
	DATA3	DATA2	CLK	DATA1		
	DATA3	DATA2	CLK	DATA1		
	DATA1	DATA2	CLK	DATA3		
	DATA2	DATA3	CLK	DATA1		
	DATA1	DATA3	CLK	DATA2		
	DATA1	DATA2	DATA3	CLK		
	DATA3	DATA2	DATA1	CLK		
Mode CLK + DATA1 + DATA2 + DATA3 + DATA4						Four data lanes
	CLK	DATA1	DATA2	DATA3	DATA4	
	DATA3	DATA1	CLK	DATA2	DATA4	
	DATA4	DATA2	CLK	DATA1	DATA3	
	DATA2	DATA1	CLK	DATA3	DATA4	
	DATA4	DATA3	CLK	DATA1	DATA2	
	DATA3	DATA4	CLK	DATA2	DATA1	
	DATA1	DATA2	CLK	DATA4	DATA3	
	DATA1	DATA4	CLK	DATA3	DATA2	
	DATA1	DATA3	CLK	DATA4	DATA2	

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NOTE:

- The byte on Dn is sent before the byte on Dn + 1; all combinations of data and clock are supported through programming of the DSI_COMPLEXIO_CFG1 register. The CLOCK_POSITION and CLOCK_POL bit fields configure which lane transmits the clock and define its polarity. Eight bit fields (DATA1_POSITION and DATA1_POL, through DATA4_POSITION and DATA4_POL) configure the data lanes and their polarity. The DATA2_POSITION through DATA4_POSITION bit fields can be set to 0; in this case, only the data lane defined in the DATA1_POSITION bit field is used, and data is transmitted on only one clock lane and one data lane.
- Only DATA1 is bidirectional in command mode. The low-power received information is always sent by the display panel using DATA1. Because any lane of DSI_PHY_DSS_x can be configured as data lane DATA1, all lanes of the PHY are bidirectional.

10.3.2.1.2 DSI ULPS

Each lane can be put in ULPS by software configuration. ULPS requires the following conditions:

- The lane must be in ULPS.
- For data lanes, no data must be pending in the DSI module.
- For the first data lane, no bus turnaround (BTA) should have been sent. The DSI module must have control of the bus.

For more information about ULPS configuration, see Section 10.3.4.4.16, *DSI ULPS Configuration*.

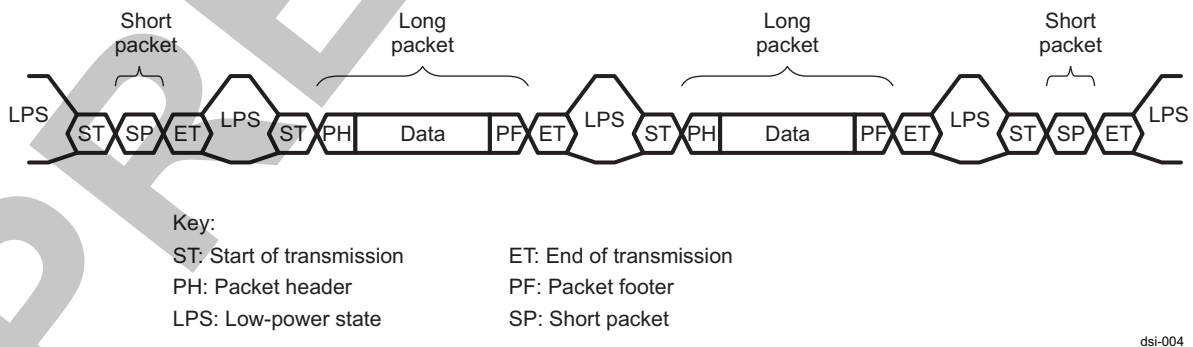
10.3.2.2 DSI Protocol Layer

Low-level protocol (LLP) is a byte-oriented protocol. It supports short and long packet formats. The DSI protocol layer defines how the display data is transported onto the PHY. Packets can be sent using HS mode or low-speed (LS) mode. LLP is selected through DSI registers. The DSI protocol layer features are:

- Transport of arbitrary data (payload independent)
- 8-bit word size
- Support for up to four interleaved VCs on the same link
- Special packets for frame start, frame end, line start, and line end information
- Descriptor for the type, pixel depth, and format of application-specific payload data
- ECC for 1-bit or 2-bit error detection in the header
- 16-bit checksum code for error detection

Figure 10-95 shows the protocol layer with short and long packets.

Figure 10-95. DSI Protocol Layer With Short and Long Packets



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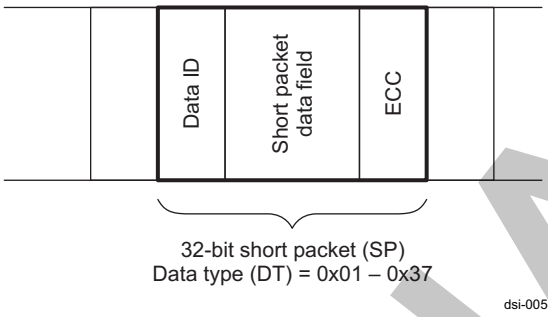
10.3.2.2.1 DSI Short Packet

Figure 10-96 shows the structure of the short packet. A short packet must contain an 8-bit data ID followed by two command or data bytes and an 8-bit ECC. No packet footer (PF) should be present. Short packets must be 4 bytes long. The ECC byte allows correction of single-bit errors and detection of 2-bit errors in the short packet.

Figure 10-96. DSI Short Packet Structure



NOTE: The short packets can be sent in LP mode or HS mode.

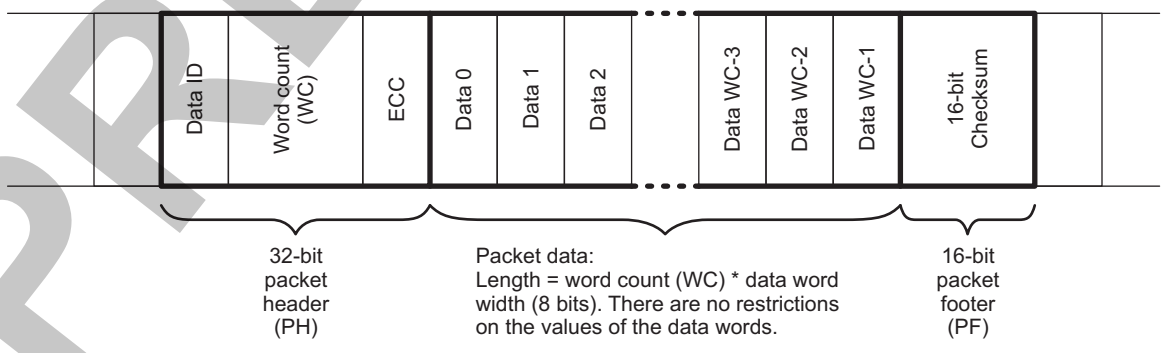
The DSI_VC_SHORT_PACKET_HEADER_i register is used to send only short packets (ECC can be calculated by hardware or by software users for debug purposes). This register is not used for video mode data because the short packets are generated by hardware based on the following events:

- Synchronization events received on the video port (assertion/deassertion of the HSYNC and VSYNC input signals)
- DSI_CTRL[18] VP_HSYNC_END
- DSI_CTRL[17] VP_HSYNC_START
- DSI_CTRL[16] VP_VSYNC_END
- DSI_CTRL[15] VP_VSYNC_START
- DSI_CTRL[11] VP_VSYNC_POL
- DSI_CTRL[10] VP_HSYNC_POL
- DSI_VC_CTRL_i[1] SOURCE

10.3.2.2.2 DSI Long Packet

Figure 10-97 shows the structure of the long packet. A long packet must consist of three elements: 32-bit packet header (PH), application-specific data payload with a variable number of bytes, and 16-bit PF.

Figure 10-97. DSI Long Packet Structure



The PH is further composed as follows:

- 8-bit data identifier: The data identifier defines the VC for the data and the DT for the application-

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specific payload data.

- 16-bit word count: The word count defines the number of bytes in the data payload between the end of the PH and the start of the PF. The PH and the PF must not be included in the word count.
- 8-bit ECC: The ECC byte allows single-bit errors to be corrected and 2-bit errors to be detected in the PH. This includes the data identifier and the word count fields.

After the end of the PH, the receiver reads the next word count × bytes of the data payload. There are no limitations on the value of a data word within the data payload block (that is, no embedded codes are used). Once the receiver has read the data payload, it reads the checksum in the PF. The host processor must always calculate and transmit a checksum in the PF. Peripherals are not required to calculate a checksum. In the special case of a 0-byte data payload, if the payload length is 0, the checksum calculation results in (0xFFFF). If the checksum is not calculated, the PF must consist of 2 bytes of 0s (0x0000). In the generic case, the length of the data payload must be a multiple of bytes. In addition, each data format can impose additional restrictions on the length of the payload data (that is, a multiple of 4 bytes). Each byte is transmitted LSB first. Payload data can be transmitted in any byte order, restricted only by data format requirements. Multibyte elements, such as word count and checksum, must be transmitted least-significant byte (LSByte) first.

NOTE: Long packets can be sent in LP or HS mode.

The DSI_VC_LONG_PACKET_HEADER_i register provides headers for long packets (ECC is always calculated by hardware). The register is used for video and command modes.

If video mode is enabled for a virtual channel, it is not possible to transfer data concurrently (interleaved in a frame) using long packets received on the video and L3_MAIN interconnect ports because the DSI_VC_LONG_PACKET_HEADER_i register is used by the video mode. The register can be unprogrammed by the user to send long packets received on the L3_MAIN interconnect port only when there is no expected data on the video port. Software must program the register correctly to send sequentially long packets in video and command modes.

The word count (WC) defined in the DSI_VC_LONG_PACKET_HEADER_i register for the VC associated with the video port indicates the number of bytes to receive (one line or two lines can be used, depending on the WC and the size of the line buffer). The total size defined in the WC of the header register cannot exceed the size of the line buffer multiplied by the number of buffer lines.

The DSI_VC_LONG_PACKET_PAYLOAD_i register is used to provide payload data for long packets (checksum is calculated by hardware when the DSI_VC_CTRL_i[7] CS_TX_EN bit is set to 1; otherwise, the value is 0x00). The register is not used in video mode because payload data are provided by the video port.

Software must ensure that the following sequence for write accesses to the header and payload registers (DSI_VC_LONG_PACKET_HEADER_i and DSI_VC_LONG_PACKET_PAYLOAD_i, respectively) is followed:

- A long PH value with WC = 0 written in the DSI_VC_LONG_PACKET_HEADER_i register can be followed by any access.
- A long PH value with WC > 0 written in the DSI_VC_LONG_PACKET_HEADER_i register must be followed by one or more writes to the DSI_VC_LONG_PACKET_PAYLOAD_i register defined by the WC value before writing again to the same DSI_VC_LONG_PACKET_HEADER_i register.

CAUTION

If this sequence is not followed, no error is generated. Access to other DSI registers during this sequence is allowed.

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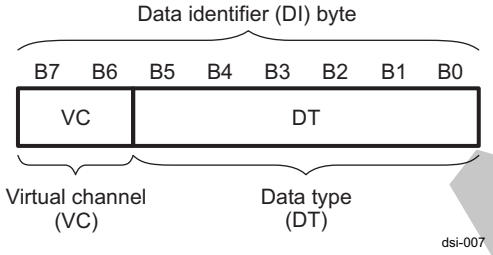
10.3.2.2.3 DSI Data Identifier

The data identifier byte contains the values for the virtual channel ID and data type, as shown in Figure 10-98. The virtual channel ID is contained in the 2 most-significant bits (MSBs) of the data identifier byte and identify the data as directed to one of four virtual channels. The value of the data type is contained in the 6 LSBs of the data identifier byte.

Figure 10-98. DSI Data Identifier Structure

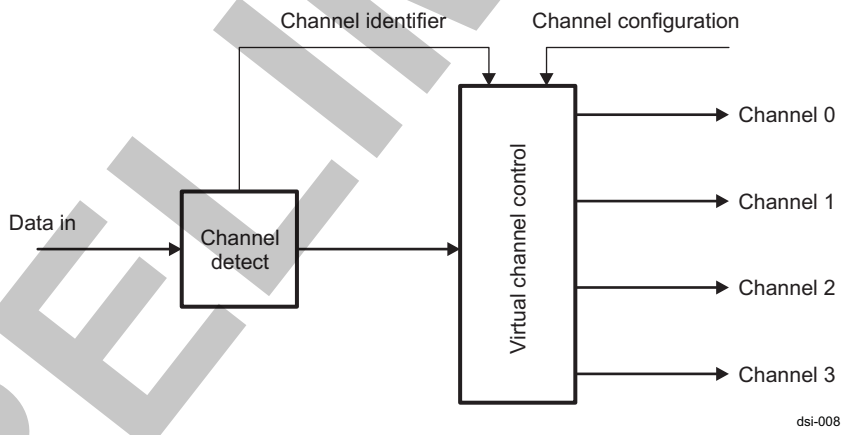


10.3.2.2.3.1 DSI VC ID – VC Field, DI[7:6]

The host can service up to four peripherals with tagged commands or blocks of data using the VC ID field of the header for packets targeted at different peripherals. The VC ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Each packet sent in a single transmission has its own VC assignment and can be directed to different peripherals. The VC ID is defined in the DSI_VC_SHORT_PACKET_HEADER_i and DSI_VC_LONG_PACKET_HEADER_i registers for short and long packets, respectively. It will not be modified by hardware. There is one set of registers for each VC. Each set of registers defines the characteristics of the traffic between the host and the display associated with the VC.

Figure 10-99 shows the VC controller.

Figure 10-99. DSI VC Controller



10.3.2.2.3.2 DSI Data Type Field DT[5:0]

The data type field specifies whether the packet is long or short and identifies the packet format. The data type field, and the word count field for long packets, informs the receiver about how many bytes to expect in the rest of the packet. This is necessary because the beginning and end of a packet are not indicated by special packet start/end sync codes. This permits packets to convey arbitrary data, but it also requires the PH to specify the size of the packet.

10.3.2.2.4 DSI Synchronization Codes

Each frame can be identified by two synchronization codes:

- For the start of the vertical synchronization (VSS) pulse

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- For the end of the vertical synchronization (VSE) pulse

Each line can be identified by two synchronization codes:

- For the start of the horizontal synchronization (HSS) pulse
- For the end of the horizontal synchronization (HSE) pulse

The synchronization events are not required by the display (peripheral): they are optional. Users can program which synchronization events are generated to the display from the timings received from the DISPC in video mode. When data are received on the L3_MAIN interconnect port, the synchronization codes are not automatically generated by the protocol engine. They can be provided on the L3_MAIN interconnect port by writing to the registers with limited timing control. It is highly recommended to use the video port from the DISPC to receive the synchronization events to automatically generate short synchronization packets to the peripheral.

When the DSI protocol engine detects that the VSYNC signal from the DISPC transitions from INACTIVE to ACTIVE state, the VSS short packet replaces the following HSS corresponding to the following HSYNC synchronization short packet (if the generation is enabled).

When the transition from ACTIVE to INACTIVE state is detected, the VSE short packet is generated (if the generation is enabled), replacing the HSE synchronization packet corresponding to the following HSYNC.

When the DSI protocol engine detects that the HSYNC signal from the DISPC transitions from INACTIVE to ACTIVE state, the HSS short packet is generated (if the generation is enabled).

When the transition from ACTIVE to INACTIVE state is detected, the HSE short packet is generated (if generation is enabled).

For the first frame, any HSYNC and data received on the video port before the first VSYNC must be ignored. Because the first VSYNC sent to the display is also recognized as an HSYNC for the first line, there is no HSYNC sent for the first line. To send the synchronization codes, the DSI protocol engine uses short packets. Table 10-511 lists the 6-bit DT synchronization code values.

Table 10-511. DSI Synchronization Codes

Synchronization Code	Value	Comments
Vertical sync start code (VSS)	0x1	Optional
Vertical sync end code (VSE)	0x11	Optional
Horizontal sync start code (HSS)	0x21	Optional
Horizontal sync end code (HSE)	0x31	Optional

10.3.2.2.5 DSI Blanking

To keep the DSI link in HS mode while using video mode during blanking periods, long blanking packets are sent to the display. The DSI_VM_TIMINGx (where x = 1 to 8) registers define the size of the long blanking packets after:

- Horizontal sync start code (short packet)
- Horizontal sync end code (short packet)
- Vertical sync start code (short packet)
- Vertical sync end code (short packet)
- Pixels (long packet)

Table 10-512 defines the short packet values for the synchronization packets:

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Table 10-512. DSI Sync Short Packet Values

VC ID	Sync Code	Header (First Byte)	Header (Second Byte): Data Field LSB	Header (Third Byte): Data Field MSB	Header (ECC)
0x0	0x1	0x1	0x0	0x0	See Note following this table.
	0x11	0x11			
	0x21	0x21			
	0x31	0x31			
0x1	0x1	0x41			
	0x11	0x51			
	0x21	0x61			
	0x31	0x91			
0x2	0x1	0x81			
	0x11	0x81			
	0x21	0xA1			
	0x31	0xB1			
0x3	0x1	0xC1			
	0x11	0xD1			
	0x21	0xC1			
	0x31	0xF1			

NOTE:

- If the ECC is enabled by setting the DSI_VC_CTRL_i[8] ECC_TX_EN bit to 1 for the VC in video mode, the ECC value is calculated; otherwise, 0x00 is used for the blanking long packets and sync short packets. If the CRC is enabled by setting the DSI_VC_CTRL_i[7] CS_TX_EN bit to 1 for the VC in video mode, the checksum value is calculated; otherwise, 0x00 is used for the blanking long packets.
- In other cases, when the DSI_VC_CTRL_i[7] CS_TX_EN bit is set to 0, the value 0x00 is always used for the CRC (long packets). When the DSI_VC_CTRL_i[8] ECC_TX_EN bit is set to 0, the value 0x00 is used for the ECC for short and long packets, except when the header is provided by the register, because the ECC field is available in the register. It can be used to generate invalid ECC values when the header is provided by the register.

The DSI link (lanes and clock separately) can be put in ULPS. While using the blanking values formerly defined, the packets (short and long) are considered in HS mode.

Timing parameters VSA, VBP, VFP, HSA, HBP, HFP, VACT, and t_L are defined in the DSI_VM_TIMING1 through DSI_VM_TIMING8 registers. HSA, HBP, HFP, and t_L are defined using the byte clock unit (TXBYTECLKHS – HS transmit byte clock generated by DSI_PHY_DSS_x) and also in low-power clock cycles (TxClkEsc). VSA, VBP, VFP, and VACT are defined by the number of lines. When the HS blanking packets are sent during the blanking periods, the parameters are used to determine the blanking packet payload size (considering the 4-byte header and the 2-byte checksum).

The configuration of the DISPC timing generator must be used when the DISPC timings are used to generate DSI HS video mode transfer.

Special care must be taken in the case of the last line of the frame. The LPS transition is required when the link is in HS mode for the whole frame.

When BTA is sent for the data packets, the following blanking period cannot be used to send any data from the TX FIFO. When the blanking period starts with one HS packet from one VC, it can be followed only by another HS packet from the same VC, or by a trigger (for example, BTA). When there is no more HS data to send for this VC, the lane is in LPS.

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When the blanking period starts with one LP packet from one VC, it can be followed only by another LP packet from the same VC, by another VC, by trigger (BTA, for example), or by extra LP NULL packets. If the trigger is sent, it is not possible to send any more data. When there is no more data from the TX FIFO to send in LP mode or the trigger has been sent, the lane is put into LPS. If the lanes must be kept in HS mode during blanking periods (except for the last blanking period of the frame), the HS blanking packets must be used. If one trigger is sent at the beginning of the blanking period, the rest of the blanking period is in LPS.

Figure 10-100 and Figure 10-101 show a nonburst transfer in DSI video mode with and without VE and HE, respectively. Figure 10-102 shows a burst transfer in DSI video mode without VE and HE.

Figure 10-100. DSI Video Mode: Nonburst Transfer With VE and HE

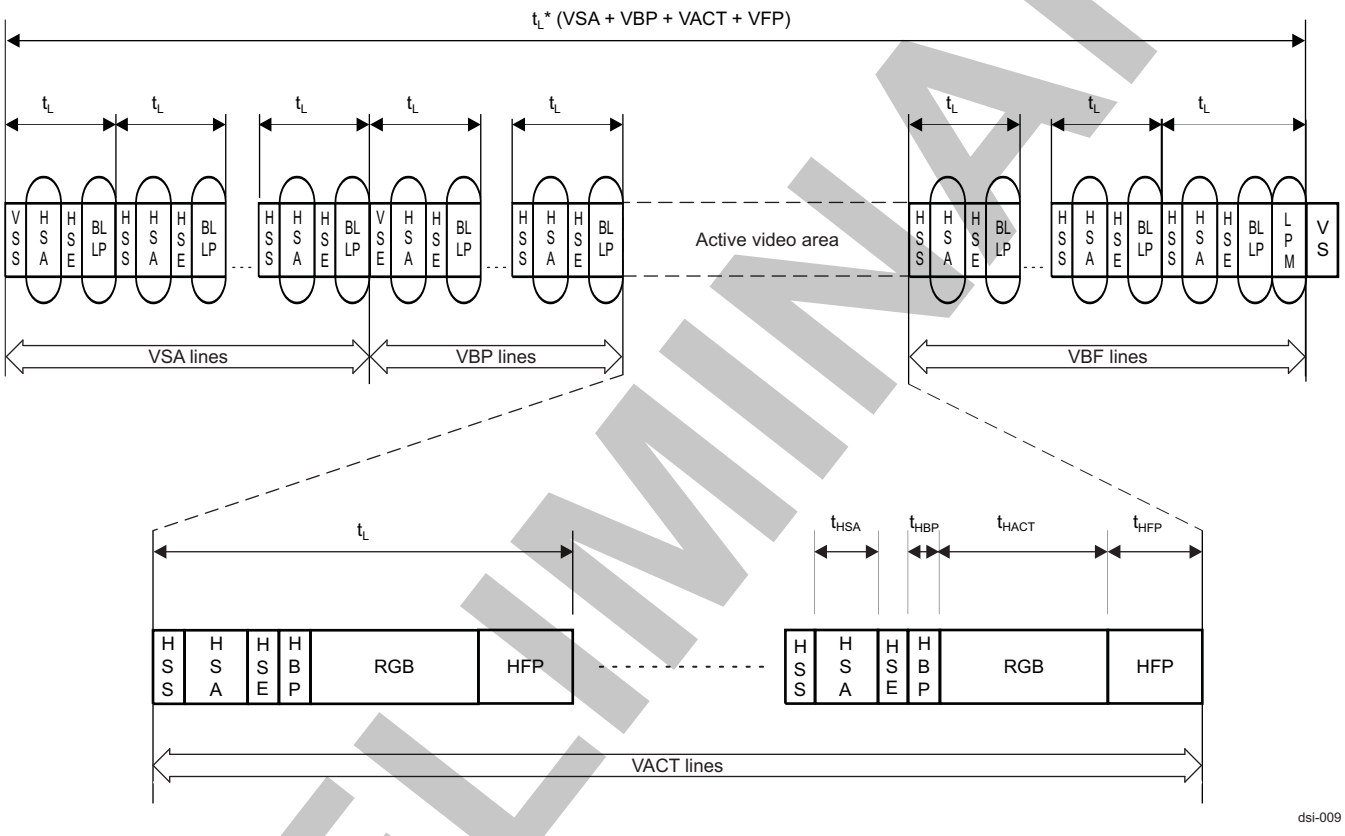

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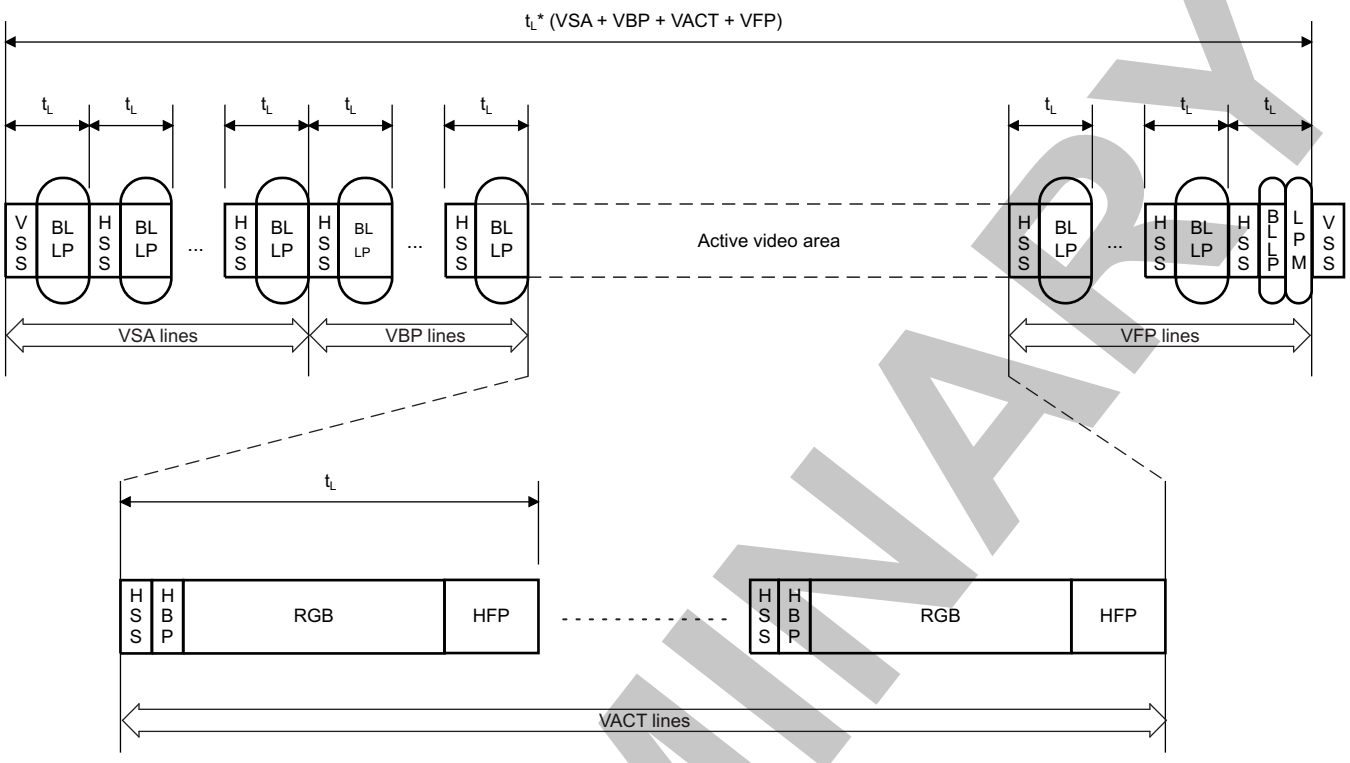
Figure 10-101. DSI Video Mode: Nonburst Transfer Without VE and HE



Legend:

- VSS – DSI Sync Event Packet: V sync start
- VSE – DSI Sync Event Packet: V Sync End
- BL LP – DSI Packet : Arbitrary sequence of nonrestricted DSI packets or low-power mode including optional BTA
- HSS – DSI Sync Event Packet: H sync start
- HSA – DSI Blanking Packet: Horizontal sync active or low-power mode, no data
- HSE – DSI Sync Event Packet: H sync end
- HFP – DSI Blanking Packet: Horizontal front porch or low-power mode
- HBP – DSI Blanking Packet: Horizontal back porch or low-power mode
- RGB – DSI Packet: Arbitrary sequence of pixel stream and null packets
- LPM – Low-power mode including optional BTA

NOTE: HSA timing is not used and does not have to be programmed when an HE short packet is not generated.

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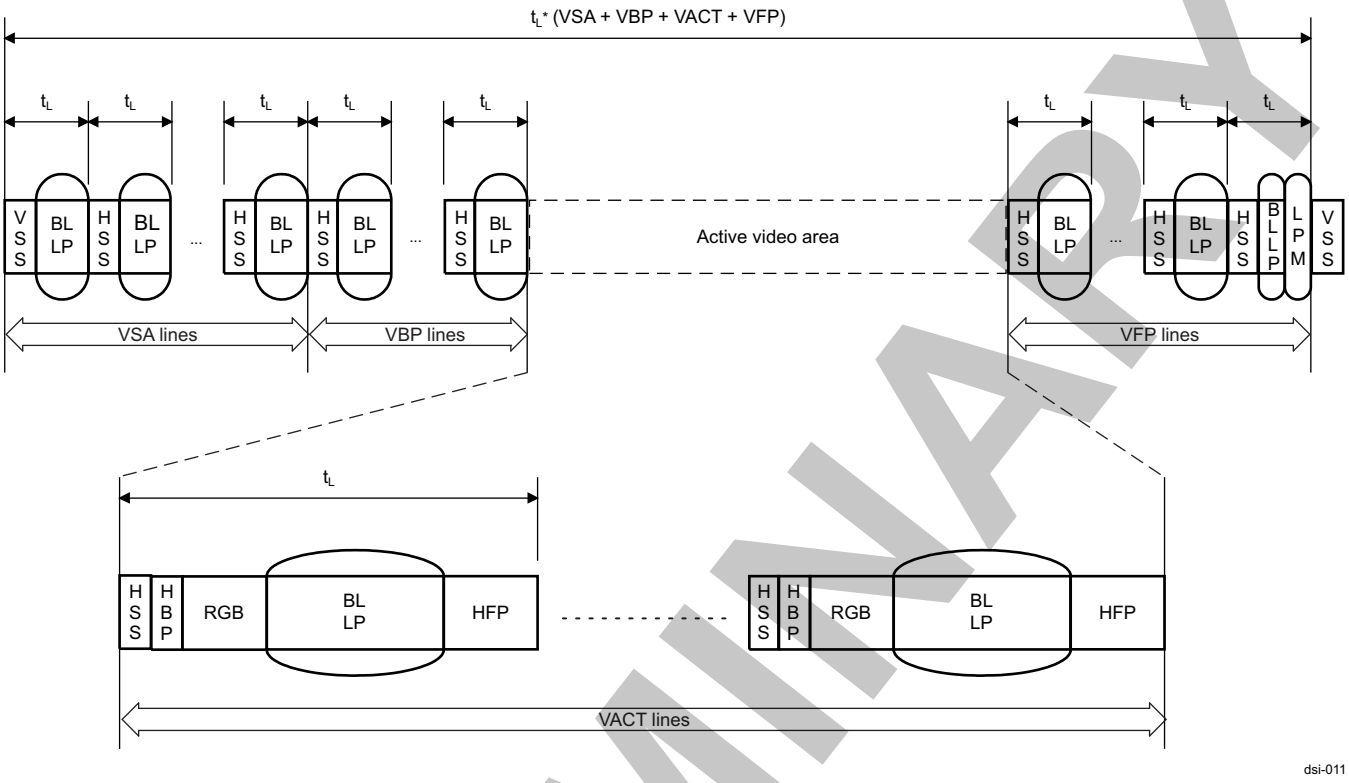
Figure 10-102. DSI Video Mode: Burst Transfer Without VE and HE



NOTE: HSA timing is not used and does not have to be programmed when an HE short packet is not generated.

In Figure 10-101 and Figure 10-102, if a HSYNC end short packet is not generated (HSA does not exist), HBP must not be 0.

10.3.2.2.6 DSI Frame Structures

NOTE: The figures in this section show only pixel packets and blanking periods; they do not show synchronization packets.

Figure 10-103 shows the DSI general frame structure.

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Figure 10-103. DSI General Frame Structure

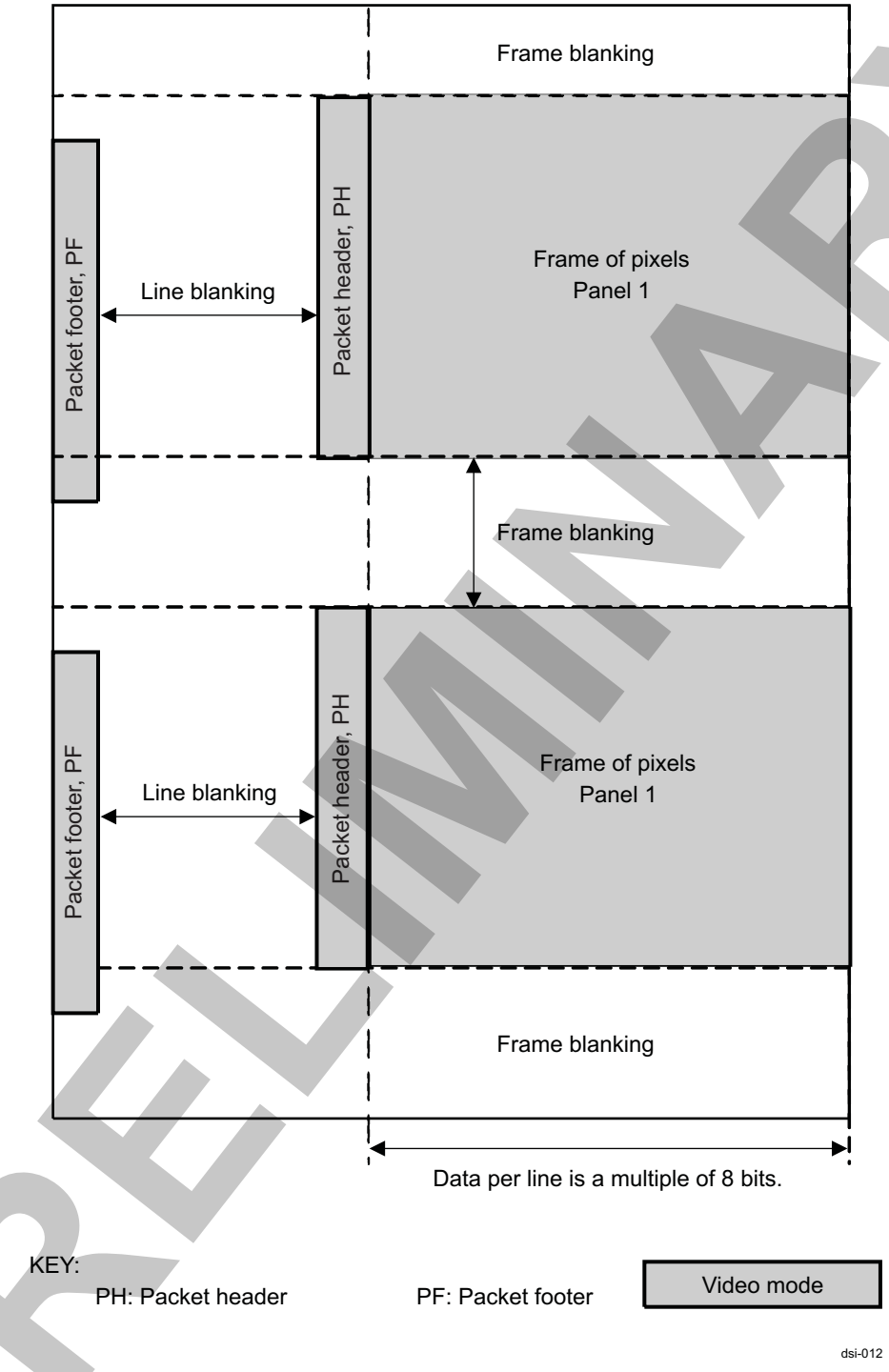

Figure 10-104 shows the general frame structure using burst mode.

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Figure 10-104. DSI General Frame Structure Using Burst Mode

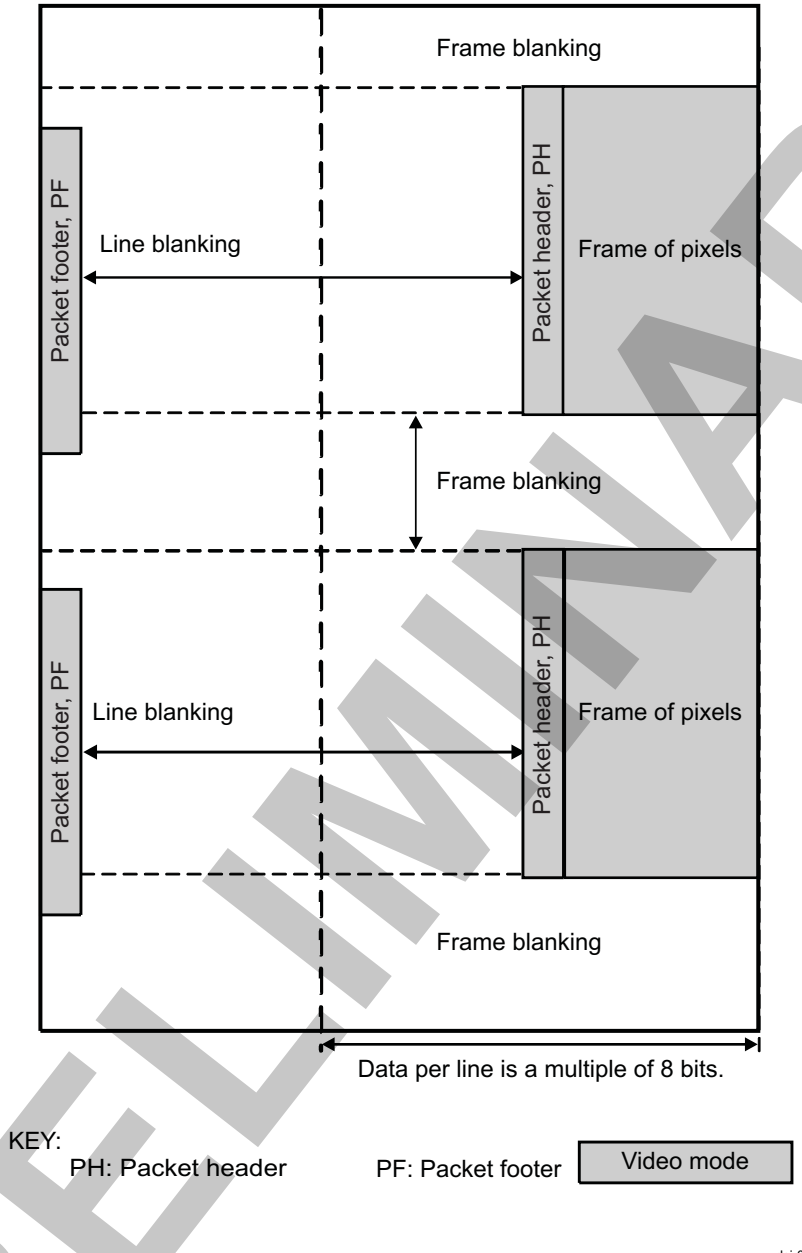

Figure 10-105 shows the general frame structure using burst mode and interleaving.

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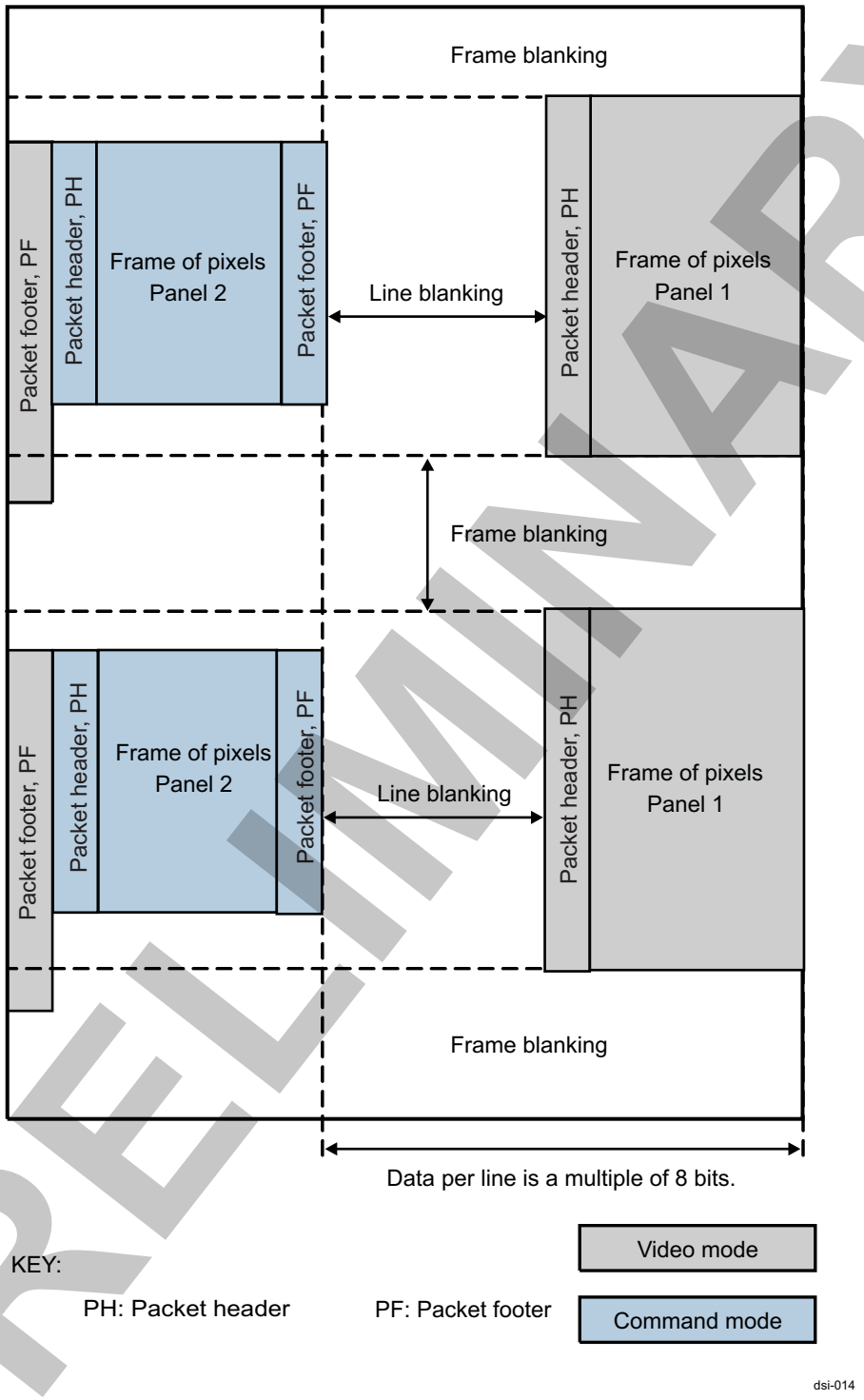
Figure 10-105. DSI General Frame Structure Using Burst Mode and Interleaving



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10.3.2.2.7 DSI VCs

The DSI protocol layer transports VCs. VCs separate different data flows, which are interleaved in the same data stream. Each VC is identified by a unique channel identification number in the PH. The channel identification number is encoded in 2 bits. The DSI protocol engine determines the channel identifier number to be used to generate the PH and multiplexes the interleaved data streams. The DSI protocol engine supports up to four concurrent VCs. Table 10-513 summarizes the VC values used for each channel.

Table 10-513. DSI VC Values

VC Number	Value
VC 0	0x0
VC 1	0x1
VC 2	0x2
VC 3	0x3

If multiple displays are connected to a single DSI port on the host, a hub can be used to route the data stream to the appropriate display based on the VC ID. Typically, VC ID 0x0 is used for the primary display and 0x1 is used for the secondary. The hub may have its own VC ID to provide communication capability between the host and the hub.

There is one set of registers for each VC. The attributes of the VC define the following characteristics:

- Transfer mode (DSI_VC_CTRL_i[4] MODE bit):
  - Video mode
  - Command mode
- Data type
- Source (DSI_VC_CTRL_i[1] SOURCE bit)
  - Video port
  - Slave interconnect port
- HS or LP forward transmission
- Automatic BTA generation
  - Short packets (DSI_VC_CTRL_i[2] BTA_SHORT_EN bit)
  - Long packets (DSI_VC_CTRL_i[3] BTA_LONG_EN bit)
- DMA request configurations for RX and TX
  - DMA request number (DSI_VC_CTRL_i[29:27] DMA_RX_REQ_NB bit field for RX FIFO and DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB bit field for TX FIFO)
  - DMA threshold (DSI_VC_CTRL_i[26:24] DMA_RX_THRESHOLD bit field for RX FIFO and DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD bit field for TX FIFO)
- Mode speed (DSI_VC_CTRL_i[9] MODE_SPEED bit)
- ECC transmission (DSI_VC_CTRL_i[8] ECC_TX_EN bit)
- CS transmission (DSI_VC_CTRL_i[7] CS_TX_EN bit)

NOTE: The VC ID is not calculated by the DSI module but is provided while writing into the DSI_VC_SHORT_PACKET_HEADER_i and DSI_VC_LONG_PACKET_HEADER_i registers.

10.3.2.3 DSI Multilane Layer

A layer consists of lane splitter logic to split the incoming byte stream into a serial stream. The bits are sent with the LSB first. The number of active lanes is configurable through a register. The order of the lanes is configurable. The number of lanes can be changed only in ULPS or when all data lanes are in STOP state.

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10.3.2.3.1 DSI SoT and EoT in Multilane Configurations

Because a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of lanes, some lanes may run out of data before others. Therefore, the lane management layer, as it buffers up the final set of less-than-N bytes, deasserts its valid data signal into lanes for which there is no further data. Although all lanes start simultaneously with parallel start-of-transmissions (SoTs), each lane operates independently and may complete the HS transmission before the other lanes, sending an end-of-transmission (EoT) one cycle (byte) earlier.

10.3.2.3.2 DSI Lane Splitter

The lane splitter can split the byte stream into two, three, or four lanes (for one lane, the splitter is bypassed). Figure 10-106 through Figure 10-109 show the byte position in each serial link for one-, two-, three-, and four-data lane configurations. The byte stream always starts from the first lane. It finishes on one of the lanes, depending on the number of bytes to send and the number of lanes. The splitter module is used only when packets are sent using HS mode. In LS mode, only the first data lane is used.

Figure 10-106. DSI Four-Data Lane Configuration

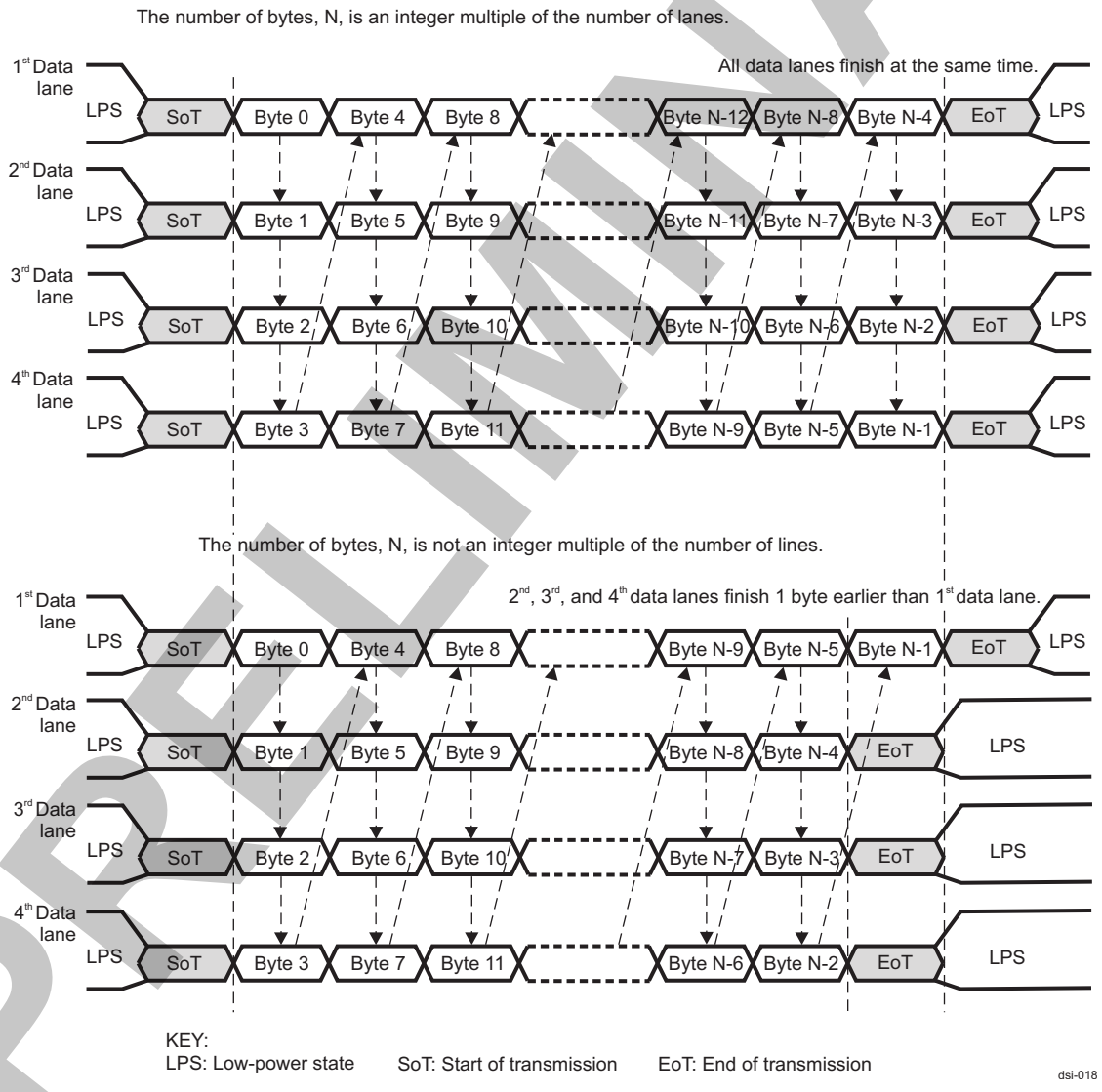

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Figure 10-107. DSI Three-Data Lane Configuration

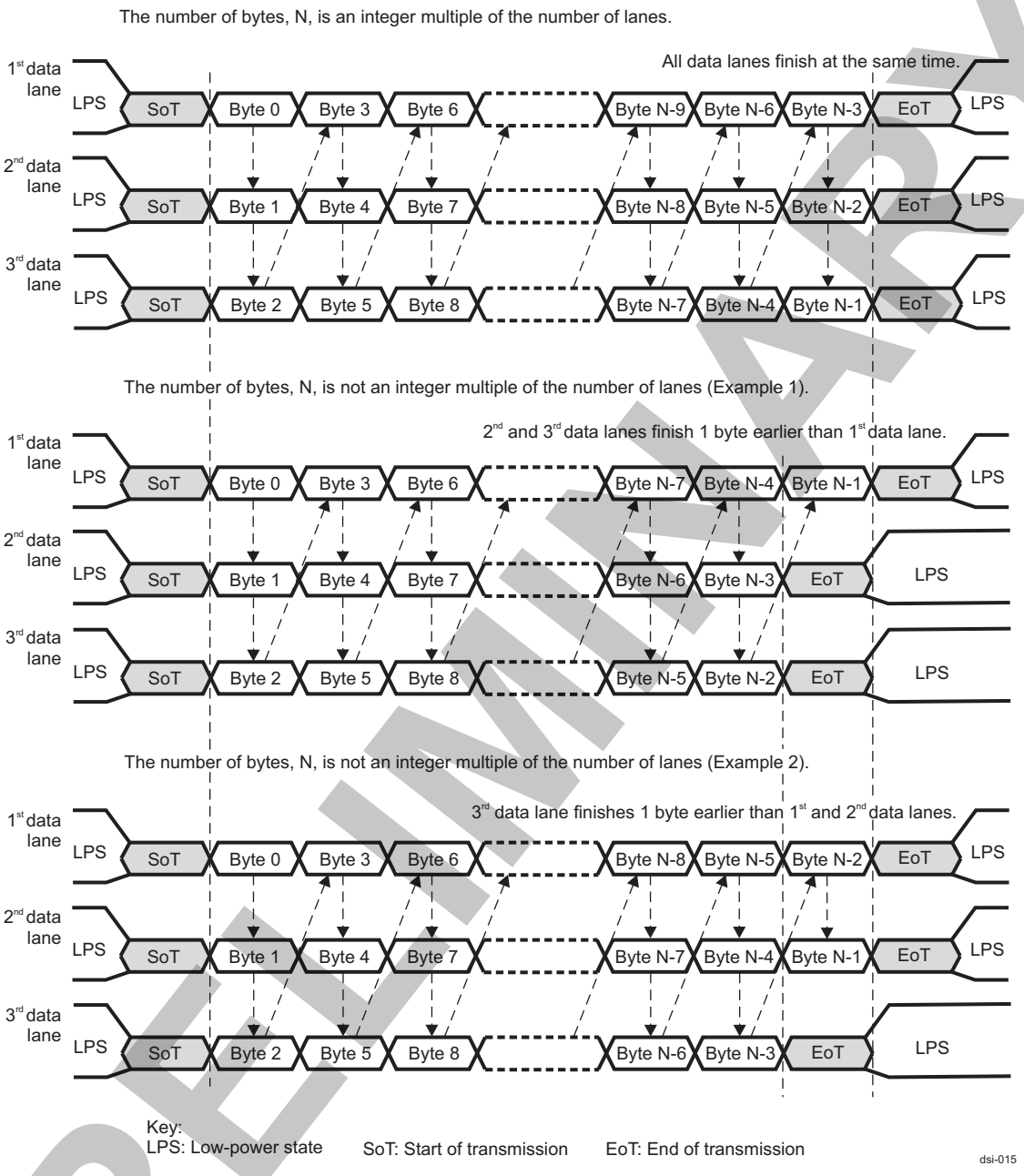

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Figure 10-108. DSI Two-Data Lane Configuration

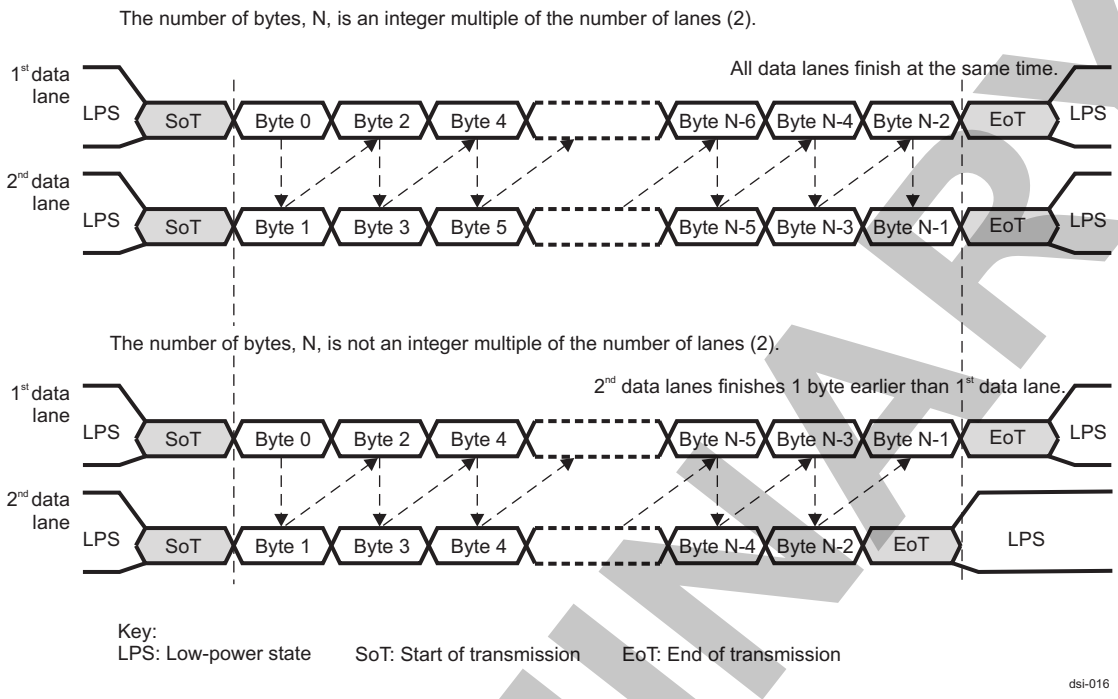
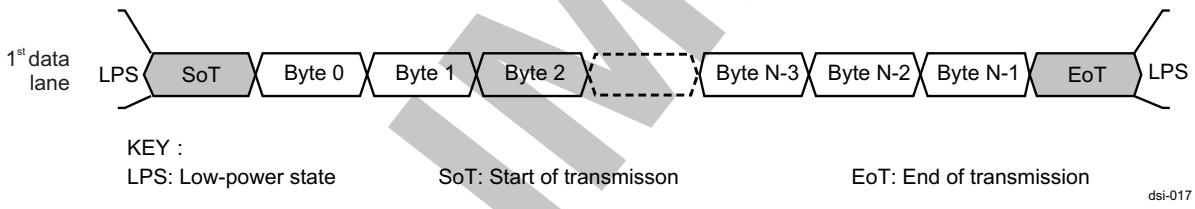
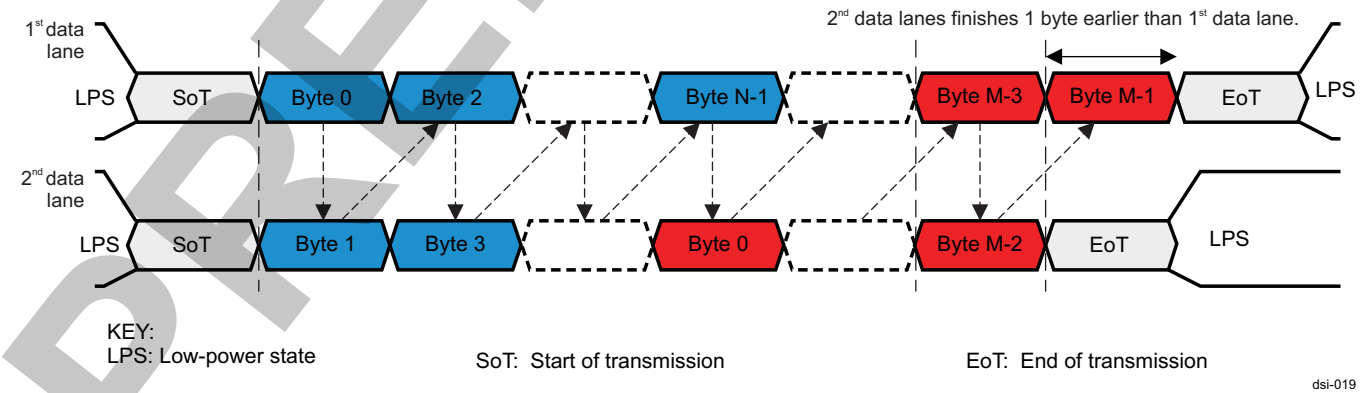


Figure 10-109. DSI One-Data Lane Configuration



For back-to-back packets, the byte stream is considered as a single packet by the splitter module. Figure 10-110 shows an example of two packets sent back-to-back. N bytes are used for the first packet and M bytes for the second packet.

Figure 10-110. DSI Two Packets Using Two-Data Lane Configuration (Example)



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10.3.2.4 DSI Pixel Data Formats

This section describes how the DSI-supported pixel data formats in video mode are transmitted over the serial interface. The DSI protocol engine can cope with all data formats if the data line length sent through the DSI physical protocol is a multiple of a pixel. This condition is required for the DSI protocol engine to work properly.

10.3.2.4.1 DSI Pixel Data Formats in Video Mode

The host can send different pixel formats in video mode. Table 10-514 lists the pixel formats supported by the DSI in video mode.

Table 10-514. DSI Pixel Data Format in Video Mode

Mode	Description
RGB888 (using 24-bit container)	RGB888
RGB666 (using 24-bit container)	RGB666
RGB666 (18-bit packet using 18-bit container)	RGB666_PACKET
RGB565 (using 16-bit container)	RGB565

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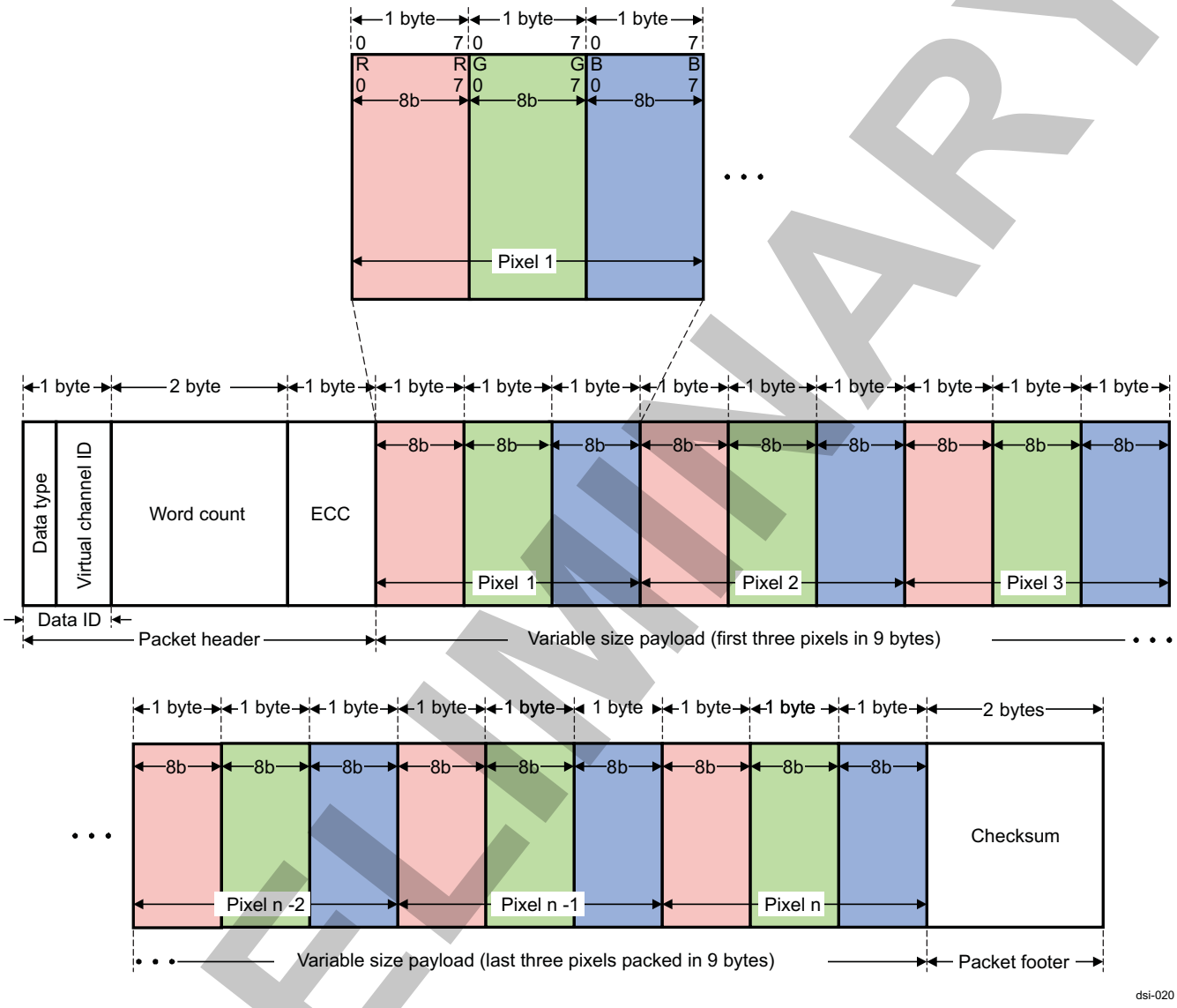
10.3.2.4.2 DSI 24 bpp – RGB Color Format, Long Packet (Video Mode)

Figure 10-111 shows the RGB888 format.

Figure 10-111. DSI 24-bpp RGB Color Format, Long Packet (Video Mode)



Packed-pixel stream, 24-bit format is a long packet used to transmit image data formatted as 24-bit pixels to a video mode display module. The packet consists of the data ID byte, a 2-byte WC, an ECC byte, a payload of length WC bytes, and a 2-byte checksum. The pixel format is R (8 bits), G (8 bits), and B (8 bits), in that order. Each color component occupies 1 byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first and the MSB last.

10.3.2.4.3 DSI 24 bpp - RGB Color Format, Long Packet (Command Mode)

Figure 10-112 shows the RGB888 format.

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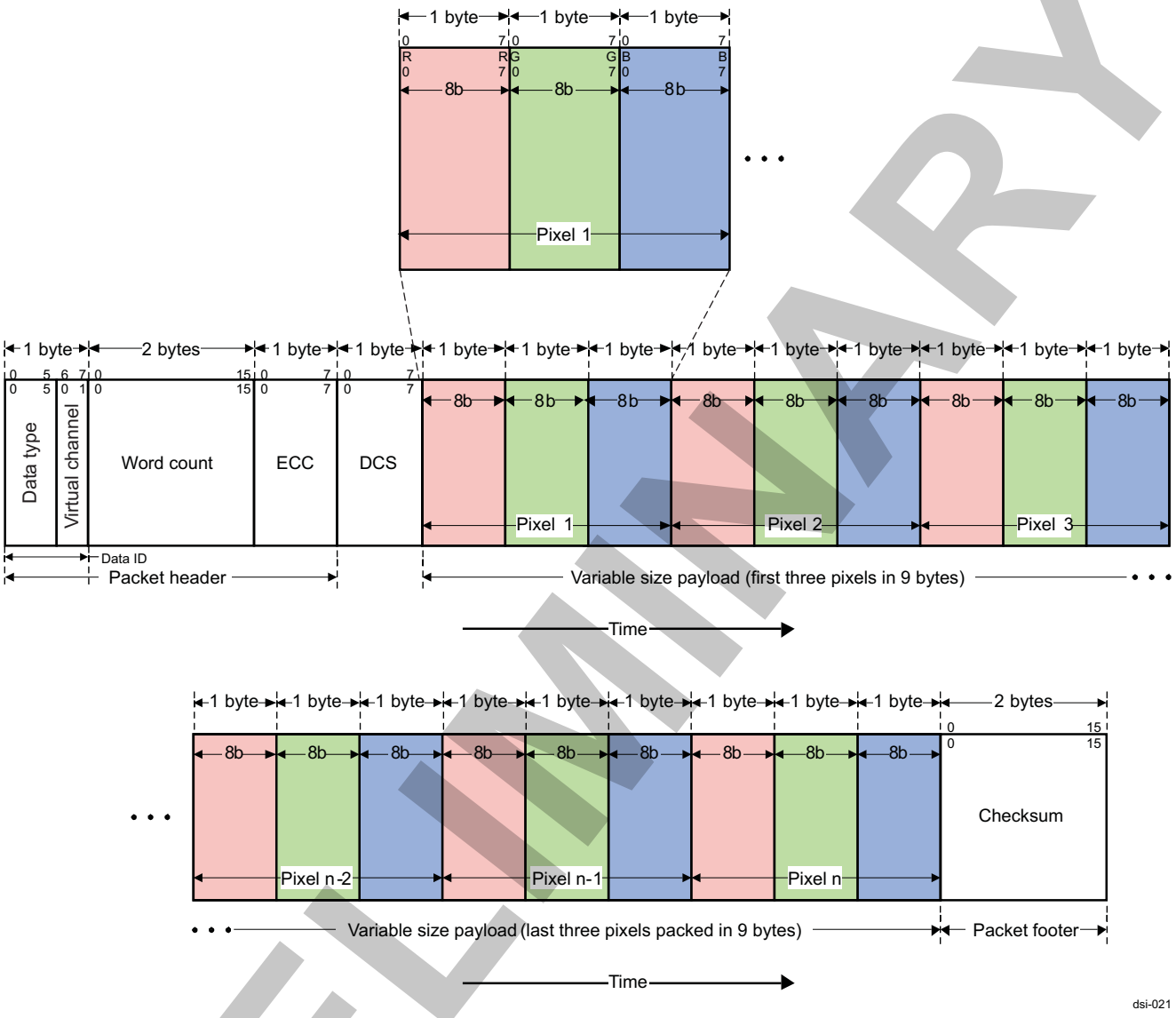
Figure 10-112. DSI 24-bpp RGB Color Format, Long Packet (Command Mode)



This format is the same as the packed pixel stream format.

10.3.2.4.4 DSI 18 bpp (Loosely Packed) – RGB Color Format, Long Packet (Transparent for DSI Protocol Engine) (Video Mode)

Figure 10-113 shows the RGB666 format.

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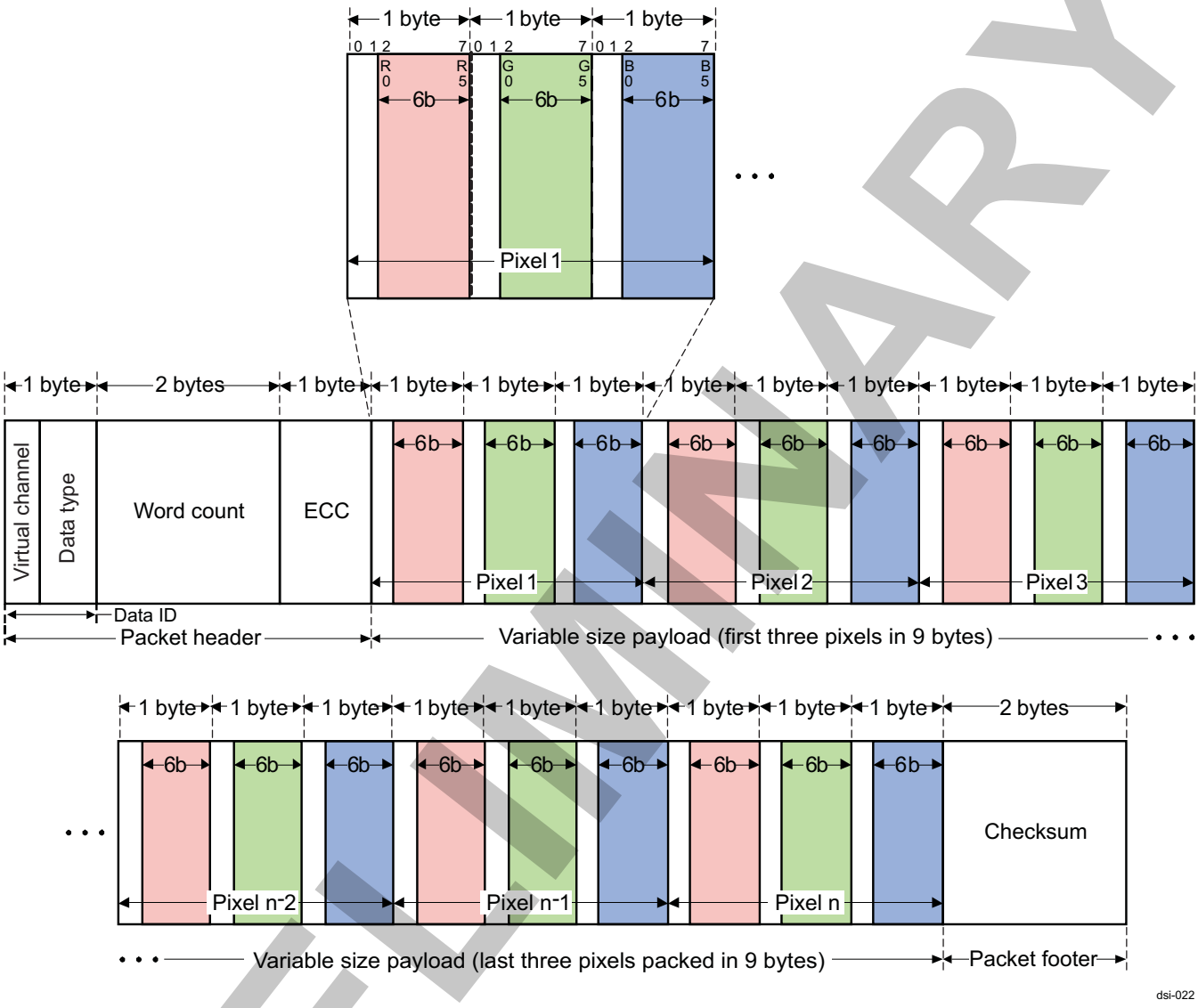
Figure 10-113. DSI 18-bpp (Loosely Packed) RGB Color Format, Long Packet (Transparent for DSI Protocol Engine) (Video Mode)



In 18-bit loosely packed pixel format, each R, G, and B color component is 6 bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires 3 bytes as it is transmitted across the link. This requires more bandwidth than packed format but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the link. This format is used to transmit RGB image data formatted as pixels to a video mode display module that displays 18-bit pixels. The packet consists of the data ID byte, a 2-byte WC, an ECC byte, a payload of length WC bytes, and a 2-byte checksum. The pixel format is R (6 bits), G (6 bits), and B (6 bits), in that order. Within a color component, the LSB is sent first and the MSB last.

10.3.2.4.5 DSI 18 bpp (Loosely Packed) – RGB Color Format, Long Packet (Command Mode)

Figure 10-114 shows the RGB666 format.

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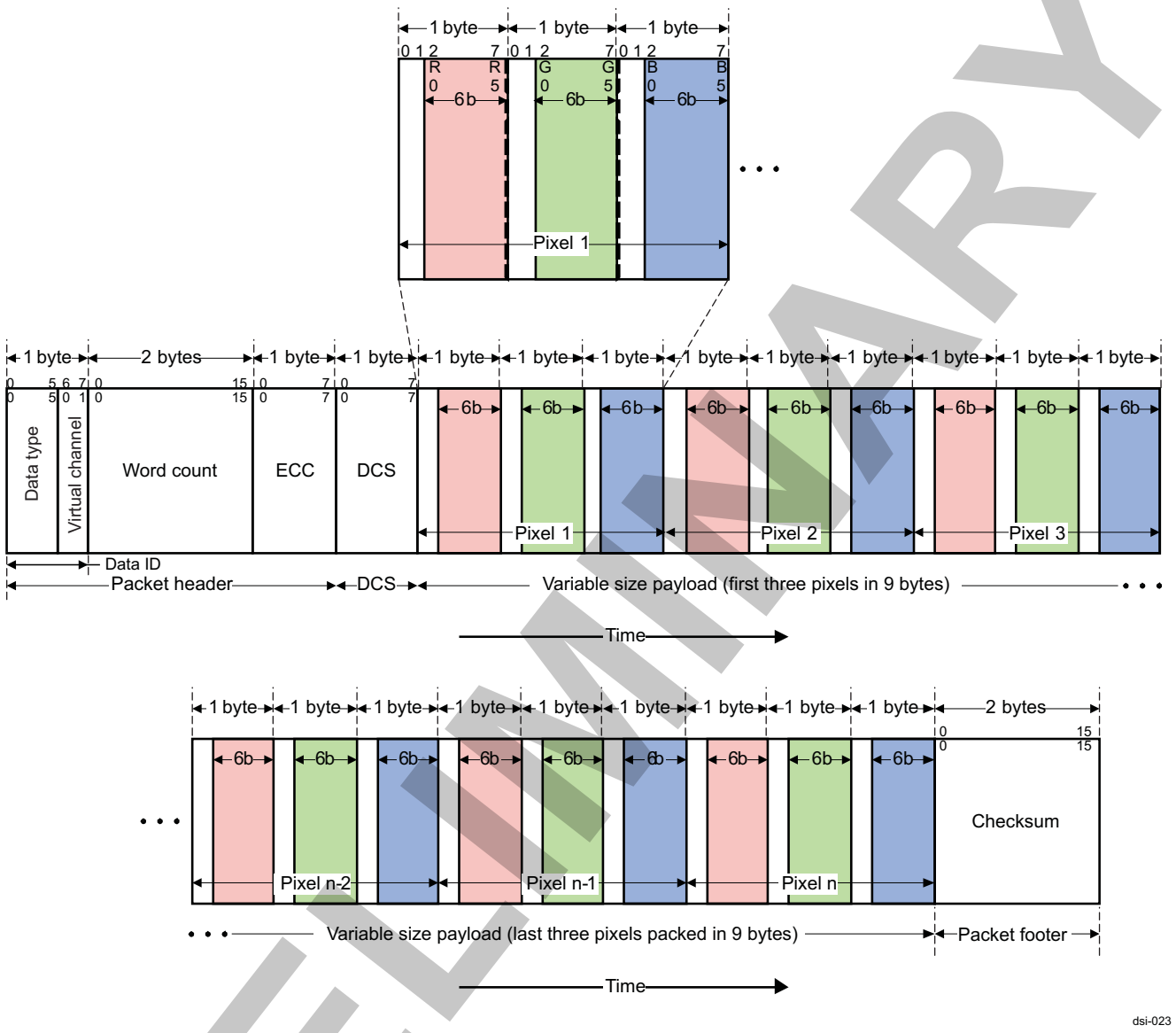
Figure 10-114. DSI 18-bpp (Loosely Packed) RGB Color Format, Long Packet (Command Mode)



This format is the same as the packed-pixel stream format.

10.3.2.4.6 DSI 18 bpp (Packed) – RGB Color Format, Long Packet (Video Mode)

Figure 10-115 shows the RGB666_PACKED format.

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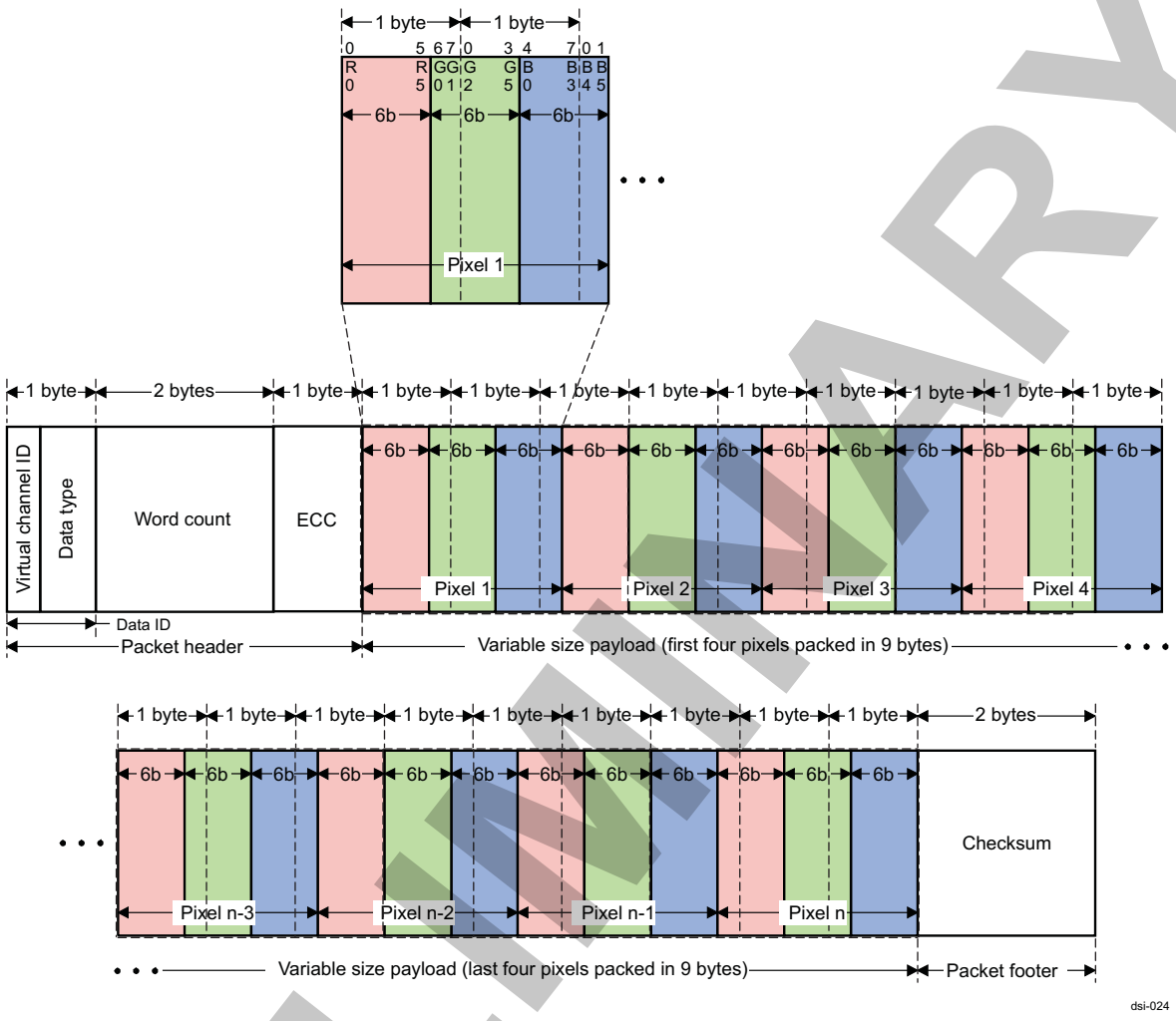
Figure 10-115. DSI 18-bpp (Packed) RGB Color Format, Long Packet (Video Mode)



Packed pixel stream 18-bit format is a long packet. It is used to transmit RGB image data formatted as pixels to a video mode display module that displays 18-bit pixels The packet consists of the data ID byte, a 2-byte WC, an ECC byte, a payload of length WC bytes, and a 2-byte checksum. The pixel format is R (6 bits), G (6 bits), and B (6 bits), in that order. Within a color component, the LSB is sent first and the MSB last. With this format, it is strongly recommended that the total line width be a multiple of 4 pixels (9 bytes). This format is not supported in command mode.

10.3.2.4.7 DSI 16 bpp – RGB Color Format, Long Packet (Video Mode)

Figure 10-116 shows the RGB565 format.

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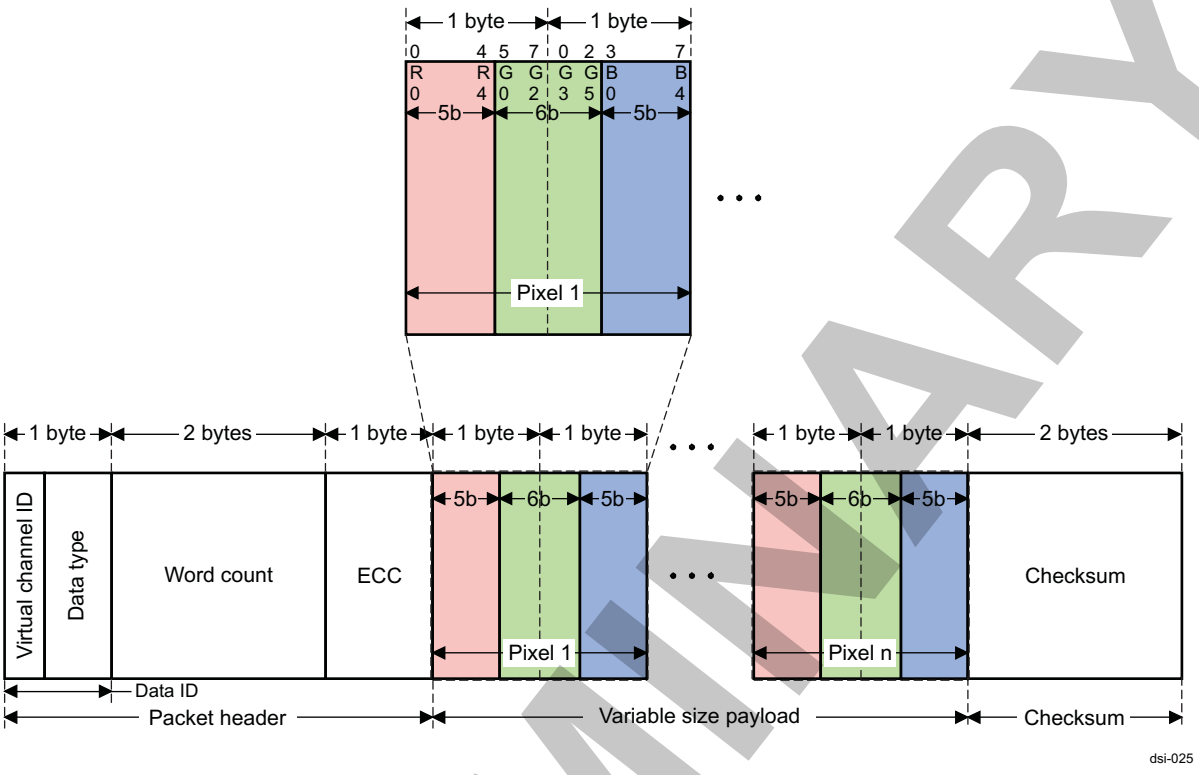
Figure 10-116. DSI 16-bpp RGB Color Format, Long Packet (Video Mode)



Packed-pixel stream, 16-bit format is a long packet used to transmit image data formatted as 16-bit pixels to a video mode display module. The packet consists of the data ID byte, a 2-byte WC, an ECC byte, a payload of length WC bytes, and a 2-byte checksum. The pixel format is R (5 bits), G (6 bits; split across 2 bytes), and B (5 bits), in that order. Within a color component, the LSB is sent first and the MSB last.

10.3.2.4.8 DSI 16 bpp – RGB Color Format, Long Packet (Command Mode)

Figure 10-117 shows the RGB565 format.

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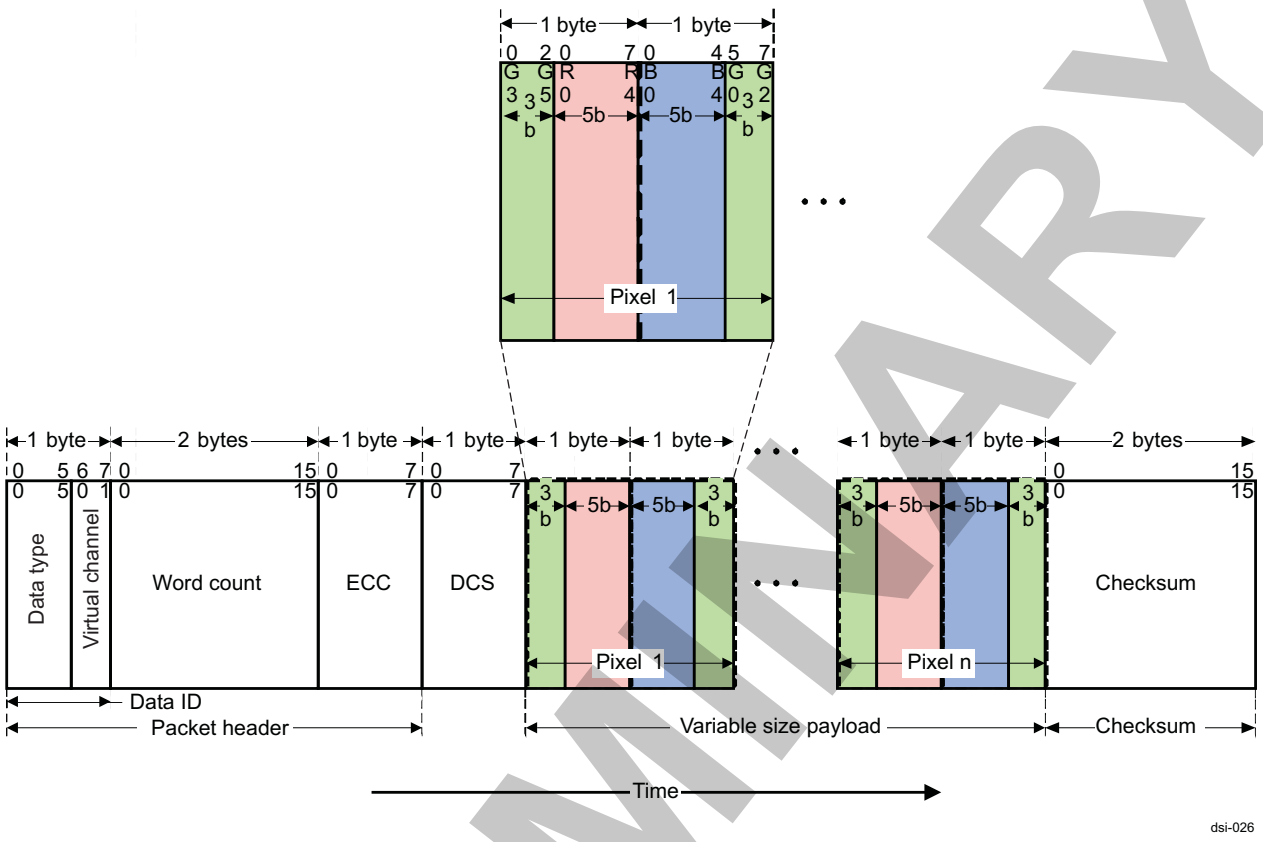
Figure 10-117. DSI 16-bpp RGB Color Format, Long Packet (Command Mode)



This is the opposite byte order from the packed pixel stream format. To retain flexibility, the byte order is made programmable using the DSI_VC_CTRL_i[12] RGB565_ORDER bit, with this order the default for command mode through the video port.

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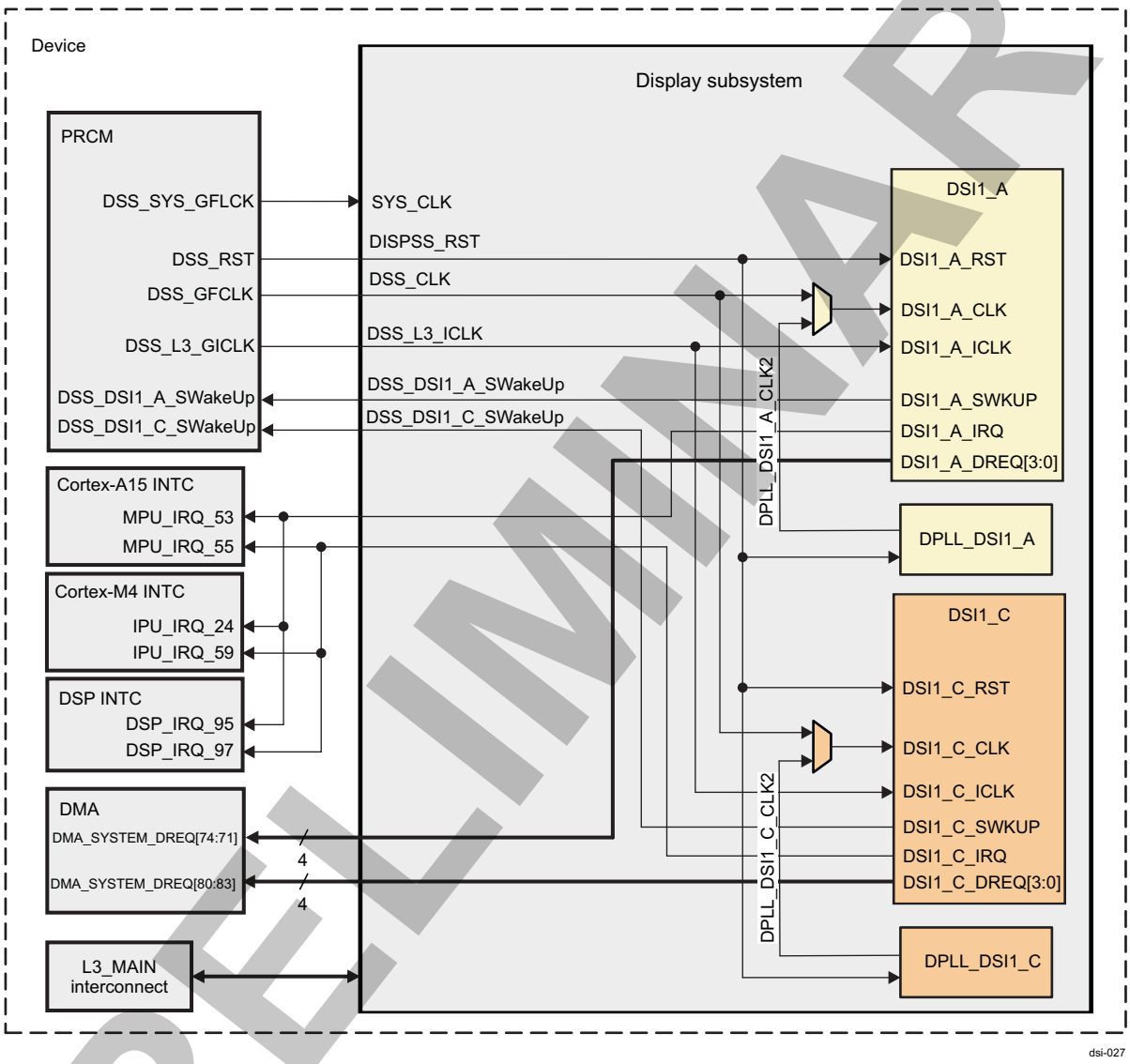
10.3.3 DSI Integration

This section describes the integration of the DSI in the device, including information about clocks, resets, and hardware requests.

Figure 10-118 shows the integration of the DSI in the device.

Figure 10-118. DSI Integration



NOTE: For more information about the wake-up request, see , *Module-Level Clock Management*, in *Chapter 3, Power, Reset, and Clock Management*.

Table 10-515 through Table 10-518 summarize the integration of the DSI module in the device.

Table 10-515. DSI Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
MIPI DSI1_A	PD_DSS	L3_MAIN for data and configuration
MIPI DSI1_C	PD_DSS	L3_MAIN for data and configuration

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Table 10-516. DSI Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
	SYS_CLK	DSS_SYS_GFLCK	PRCM module	Functional clock for the DSI PLLs
MIPI DSI1_A	DSI1_A_CLK	DSS_CLK DPLL_DSI1_A_CLK2	PRCM module DPLL_DSI1_A	Functional clock
	DSI1_A_ICLK	DSS_L3_MAIN_ICLK	PRCM module	Interface clock
MIPI DSI1_C	DSI1_C_CLK	DSS_CLK DPLL_DSI1_C_CLK2	PRCM module DPLL_DSI1_C	Functional clock
	DSI1_C_ICLK	DSS_L3_MAIN_ICLK	PRCM module	Interface clock
Resets				
MIPI DSI1_A	DSI1_A_RST	DISPSS_RST	PRCM module	Nonretention reset
MIPI DSI1_C	DSI1_C_RST	DISPSS_RST	PRCM module	Nonretention reset

NOTE: For information about clock distribution and configuration inside the module, see Section 10.3.4.2, *DSI Clock Configuration*.

Table 10-517. DSI Interrupt Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MIPI DSI1_A	DSI1_A_IRQ	DSP_IRQ_95	DSP INTC	Display DSI1_A interrupt request
	DSI1_A_IRQ	MPU_IRQ_53	Cortex-A15 INTC	Display DSI1_A interrupt request
	DSI1_A_IRQ	IPU_IRQ_24	Cortex-M4 INTC	Display DSI1_A interrupt request
MIPI DSI1_C	DSI1_C_IRQ	DSP_IRQ_97	DSP INTC	Display DSI1_C interrupt request
	DSI1_C_IRQ	MPU_IRQ_55	Cortex-A15 INTC	Display DSI1_C interrupt request
	DSI1_C_IRQ	IPU_IRQ_59	Cortex-M4 INTC	Display DSI1_C interrupt request

NOTE: For a description of the interrupt source, see Section 10.3.4.3, *DSI Interrupt Requests*.

Table 10-518. DSI DMA Requests

DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MIPI DSI1_A	DSI1_A_DREQ_0	DMA_SYSTEM_DREQ_71	DMA_SYSTEM	DSI1_A DMA request 0
	DSI1_A_DREQ_1	DMA_SYSTEM_DREQ_72	DMA_SYSTEM	DSI1_A DMA request 1
	DSI1_A_DREQ_2	DMA_SYSTEM_DREQ_73	DMA_SYSTEM	DSI1_A DMA request 2
	DSI1_A_DREQ_3	DMA_SYSTEM_DREQ_74	DMA_SYSTEM	DSI1_A DMA request 3
MIPI DSI1_C	DSI1_C_DREQ_0	DMA_SYSTEM_DREQ_80	DMA_SYSTEM	DSI1_C DMA request 0
	DSI1_C_DREQ_1	DMA_SYSTEM_DREQ_81	DMA_SYSTEM	DSI1_C DMA request 1
	DSI1_C_DREQ_2	DMA_SYSTEM_DREQ_82	DMA_SYSTEM	DSI1_C DMA request 2
	DSI1_C_DREQ_3	DMA_SYSTEM_DREQ_83	DMA_SYSTEM	DSI1_C DMA request 3

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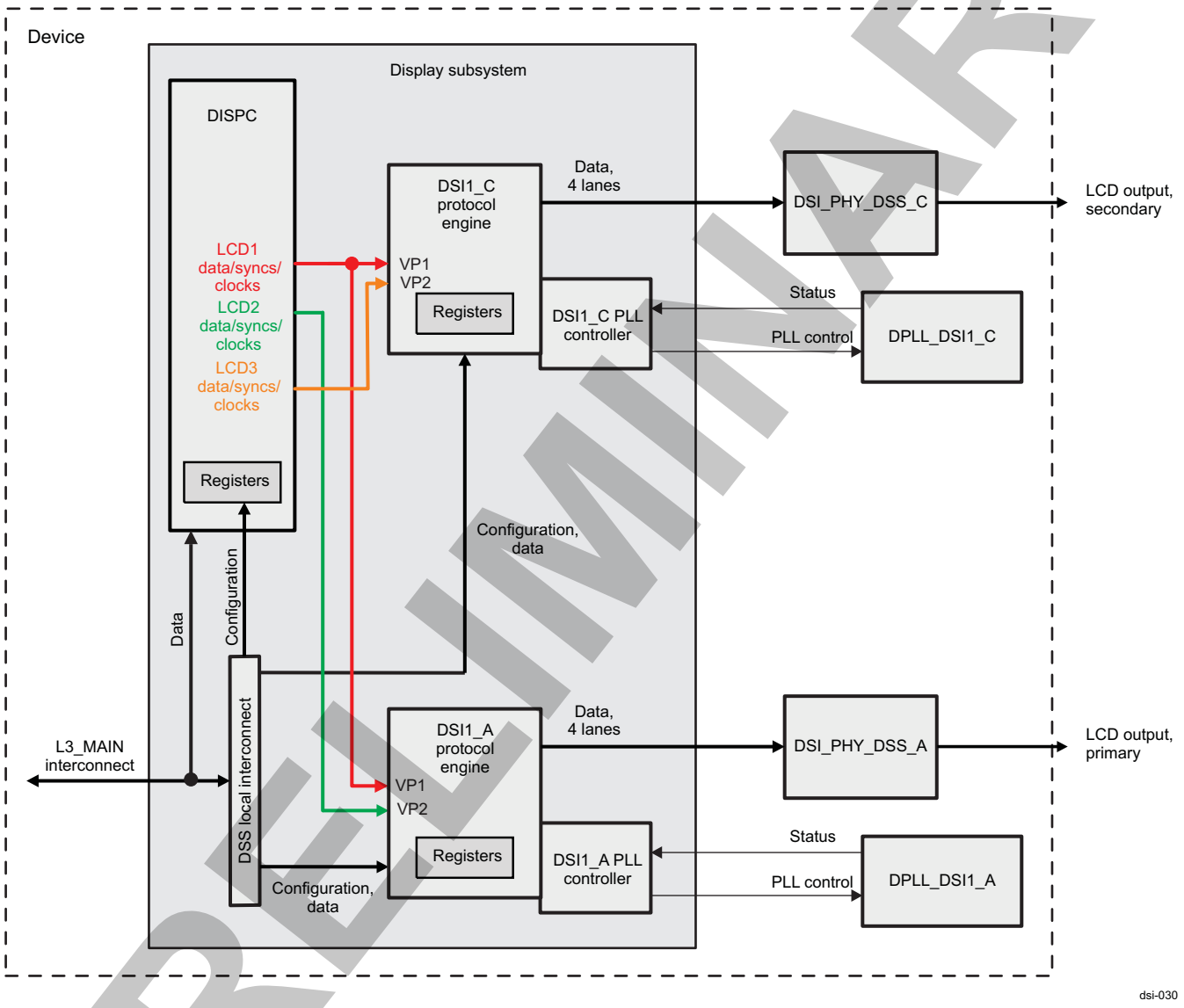
10.3.4 DSI Functional Description

This section describes the functions of the DSI1_A and DSI1_C modules.

10.3.4.1 DSI Block Diagram

Figure 10-119 is a schematic of DSI1_A and DSI1_C.

Figure 10-119. DSI Schematic



10.3.4.2 DSI Clock Configuration

Figure 10-120 shows the clock tree for DSI1_A and DSI1_C.

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Figure 10-120. DSI Clock Tree

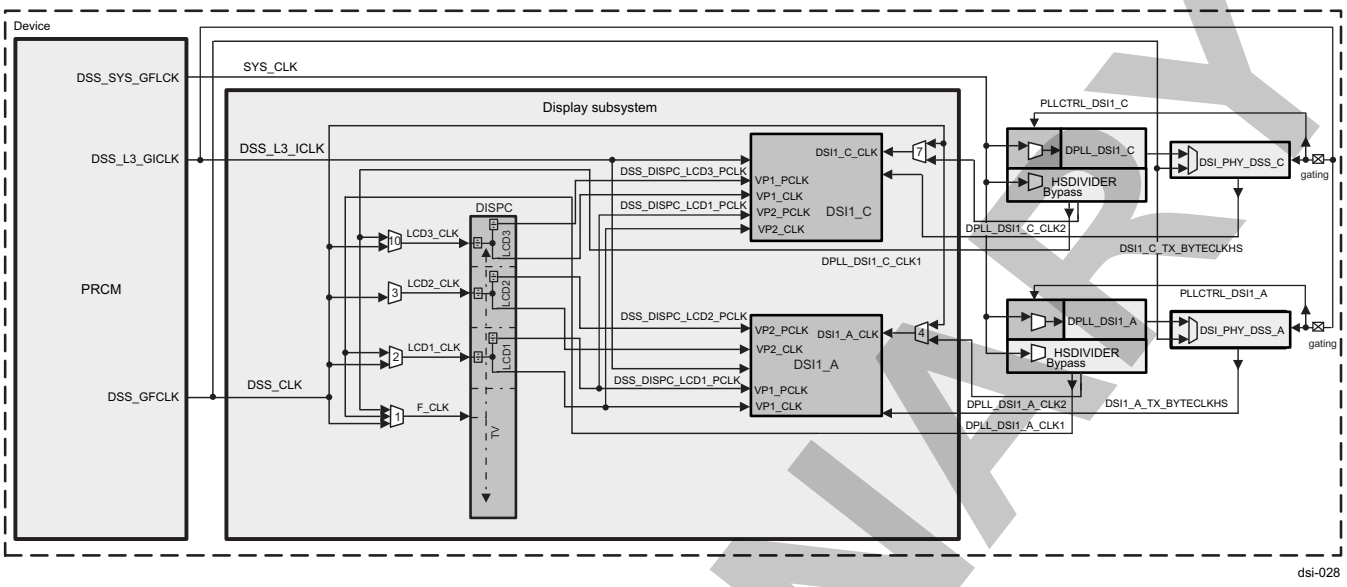

Table 10-519 shows the controls for clock multiplexers.

Table 10-519. DSI Multiplexer Controls

Destination	Source Signal Name	Source	Multiplexer Number	DSS_CTRL Bits
DISPC functional clock (F_CLK)	DSS_CLK	PRCM external PER_PLL	1	[9:7] FCK_CLK_SWITCH
	DPLL_DSI1_A_CLK1	DPLL_DSI1_A		
	DPLL_DSI1_C_CLK1	DPLL_DSI1_C		
	DPLL_HDMI_CLK1	DPLL_HDMI		
DISPC LCD1 functional clock (LCD1_CLK)	DSS_CLK	PRCM external PER_PLL	2	[0] LCD1_CLK_SWITCH
	DPLL_DSI1_A_CLK1	DPLL_DSI1_A		
DISPC LCD2 functional clock (LCD2_CLK)	DSS_CLK	PRCM external DPLL_PER	3	[12] LCD2_CLK_SWITCH
DISPC LCD3 functional clock (LCD3_CLK)	DSS_CLK	PRCM external DPLL_PER	10	[19] LCD3_CLK_SWITCH
	DPLL_DSI1_C_CLK1	DPLL_DSI1_C		
DSI1_A protocol engine functional clock (DSI1_A_CLK)	DSS_CLK	PRCM external DPLL_PER	4	[1] DSI1_A_CLK_SWITCH
	DPLL_DSI1_A_CLK2	DPLL_DSI1_A		
DSI1_A protocol engine interface clock (DSI1_A_ICLK)	DSS_L3_MAIN_ICLK	PRCM external DPLL_CORE	N/A	N/A
DSI1_A protocol engine pixel clock	DSS_DISPC_LCD1_PCLK	DISPC	N/A	N/A
DSI1_A protocol engine byte clock	DSI1_A_TX_BYTECLKHS	DPLL_DSI1_A	N/A	N/A
DSI1_C protocol engine functional clock (DSI1_C_CLK)	DSS_CLK	PRCM external DPLL_PER	7	[18] DSI1_C_CLK_SWITCH
	DPLL_DSI1_C_CLK2	DPLL_DSI1_C		
DSI1_C protocol engine interface clock (DSI1_C_ICLK)	DSS_L3_MAIN_ICLK	PRCM external DPLL_CORE	N/A	N/A
DSI1_C protocol engine pixel clock	DSS_DISPC_LCD3_PCLK	DISPC	N/A	N/A

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Table 10-519. DSI Multiplexer Controls (continued)

Destination	Source Signal Name	Source	Multiplexer Number	DSS_CTRL Bits
DSI1_C protocol engine byte clock	DSI1_C_TX_BYTECLKHS	DPLL_DSI1_C	N/A	N/A

NOTE: For more information about the DSI1_A and DSI1_C video port clocks (VPn_CLK and VPn_PCLK, where n = 1 or 2), see Section 10.3.4.4.5, *DSI Video Port Interface*

NOTE: For the frequency ratings of the various DSI clocks, see Display Subsystem Clocks, in *Display Subsystem*.

NOTE: To enable the bypass input for the DSI_PHY_DSS_A or DSI_PHY_DSS_C module, set the DSI_PLL_CONFIGURATION2[15] BYPASSEN bit to 1.

10.3.4.3 DSI Interrupt Requests

The DSI protocol engine requires a single interrupt line. The DSI_IRQSTATUS register indicates the general interrupt events. Each VC and PHY has a dedicated interrupt register: DSI_VC_IRQSTATUS_i and DSI_COMPLEXIO_IRQSTATUS, respectively.

Table 10-520 lists the DSI global interrupt events.

Table 10-520. DSI Global Interrupts

IRQ Name	Description
RESYNCHRONIZATION_IRQ	Resynchronization in video mode
TA_TO_IRQ	Turnaround timer expired
SYNC_LOST_IRQ	Synchronization with video port is lost (video mode only).
ACK_TRIGGER_IRQ	Acknowledge trigger is received.
TE_TRIGGER_IRQ	TE PHY trigger is received.
WAKEUP_IRQ	Occurs when the SWakeUp signal is asserted.
HS_TX_TO_IRQ	HS TX time-out interrupt
LP_RX_TO_IRQ	LS RX time-out interrupt
COMPLEXIO_ERR_IRQ	Error signaling from DSI PHY: The interrupt is triggered when an error is received from the DSI PHY (events are defined in DSI_COMPLEXIO_IRQSTATUS).
PLL_RECAL_IRQ	PLL recalibration event (assertion of DSIRecal signal from the DSI PLL control module)
PLL_UNLOCK_IRQ	PLL unlock event (deassertion of DSILock signal from the DSI PLL control module)
PLL_LOCK_IRQ	PLL lock event (assertion of DSILock signal from the DSI PLL control module)
VIRTUAL_CHANNEL3_IRQ	VC 3 error signaling from DSI VC 3: The interrupt is triggered when an error is received from DSI VC 3 (events are defined in DSI_VC_IRQENABLE_i where i = 3).
VIRTUAL_CHANNEL2_IRQ	VC 2 error signaling from DSI VC 2: The interrupt is triggered when an error is received from DSI VC 2 (events are defined in DSI_VC_IRQENABLE_i where i = 2).
VIRTUAL_CHANNEL1_IRQ	VC 1 error signaling from DSI VC 1: The interrupt is triggered when an error is received from DSI VC 1 (events are defined in DSI_VC_IRQENABLE_i where i = 1).
VIRTUAL_CHANNEL0_IRQ	VC 0 error signaling from DSI VC 0: The interrupt is triggered when an error is received from DSI VC 0 (events are defined in DSI_VC_IRQENABLE_i where i = 0).
TE0_LINE_IRQ	TE detected on TE0 CMOS input signal
TE1_LINE_IRQ	TE detected on TE1 CMOS input signal

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NOTE: For information about other internal DSI interrupt events, see Table 10-538 and Table 10-547 .

10.3.4.4 DSI Protocol Engine

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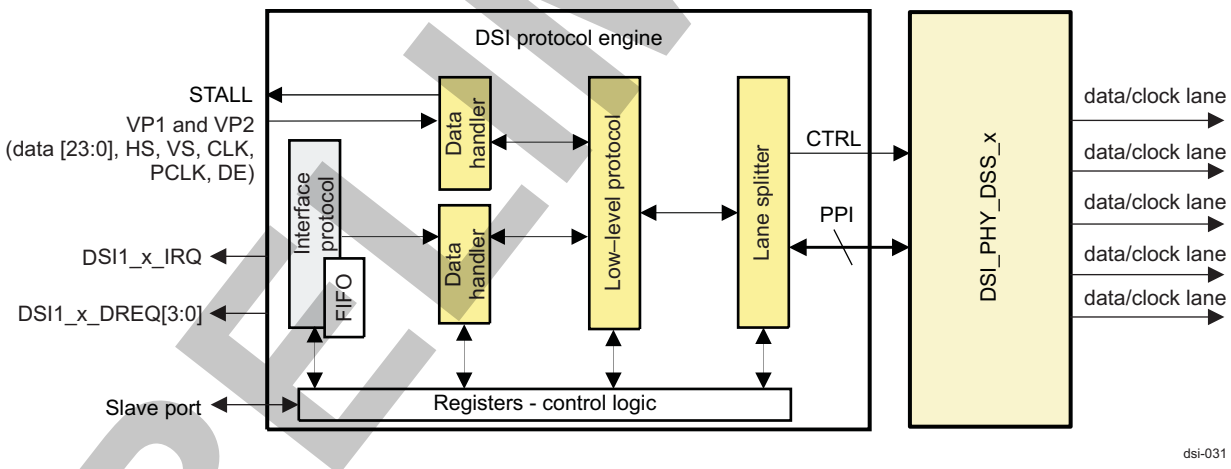
The DSI protocol engine integrates the DSI with the display through the DSI_PHY_DSS_x module, local interconnect interface, and video interface from the DISPC. The DSI_PHY_DSS_x module is described in Section 10.3.4.6, *DSI PHY*. The DSI transmitter (protocol engine + PHY) port can be connected to multiple displays using a single DSI host port. The DSI protocol engine controls the DSI PLL control module described in Section 10.3.4.5, *DSI PLL Controllers*. The DSI transmitter port can be used in video mode or/and command mode.

10.3.4.4.1 DSI Protocol Overview

The DSI protocol engine receives data from the DISPC video port and/or the L3_MAIN interconnect slave port, encapsulates them with the VC ID, generates the ECC and checksum, and splits the data into byte streams to the DSI_PHY_DSS_x to be sent using LS or HS protocol. The DSI protocol engine receives data and acknowledges from the panel using the same DSI link in case of bidirectional panel. Multiple data streams can be interleaved to support multiple panels connected to the same host DSI port. Figure 10-121 shows the DSI protocol engine, with an example of data lane and clock lane ordering. It is possible to configure other orders through registers as described in Section 10.3.2.1.1, *Data/Clock Configuration*.

Figure 10-121. DSI Protocol Engine



NOTE: The order of the PHY pairs (clock and data lanes) is informative. Each PHY pair can be clock or data. DSI PHY receives the configuration for the pin order and the differential ± in a pair from the settings in the DSI_COMPLEXIO_CFG1 register.

10.3.4.4.2 DSI Global Register Controls

Before receiving data from the DSI PHY, the DSI_PHY_DSS_x SCP registers in the DSI PHY must be configured. Table 10-521 lists the register access width limitations for all the DSI modules.

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Table 10-521. DSI Register Access Width Limitations

Register Name	Register Access Width
All DSI PHY registers (DSI_PHY_DSS_x SCP)	32-bit only
All DSI PLL control module registers	32-bit only
DSI_VC_LONG_PACKET_HEADER_i	32-bit only
DSI_VC_SHORT_PACKET_HEADER_i	32-bit only
DSI_VC_LONG_PACKET_PAYLOAD_i	16- and 32-bit
All other DSI protocol engine registers	8-, 16-, and 32-bit

CAUTION

If a different access width than listed in Table 10-521 is used, an interface error is generated in response to the write using SResp = ERR.

The DSI protocol engine is globally controlled by the DSI_CTRL register. The interface to the DSI PHY is enabled by setting the DSI_CTRL[0] IF_EN bit. When the interface is disabled, it is possible to provide data to the TX FIFO and read pending data in the RX FIFO. When the DSI_CTRL[0] IF_EN bit is set to 1, the pending packets are sent to the DSI PHY, and the data transfer from the video port is ignored until the first vertical sync event is received.

When the DSI_CTRL[0] IF_EN bit is reset by software, the DSI protocol engine must finish the transfer of the pending data in the TX FIFO and wait for a response if BTA has been sent (the protocol engine is in receive mode); hardware then resets the DSI_CTRL[0] IF_EN bit. When using video mode, the VC associated with the video port must be enabled before enabling the interface according to the following sequence:

1. The DSI_CTRL[0] IF_EN bit is equal to 0.
2. Enable the VC associated with video mode by setting the DSI_VC_CTRL_i[0] VC_EN bit.
3. Set the DSI_CTRL[0] IF_EN bit to 1.

10.3.4.4.3 DSI Transfer Modes

Two main transfer modes are supported by the DSI modules:

- Video mode: Pixels are received from the video port (VP1 or VP2.) There are some real-time constraints (pixels must be sent at the pixel frequency required by the panel module).
- Command mode: Pixels can be received from the video port or from the L3_MAIN interconnect slave port. There are no real-time constraints except that the TE must be avoided by starting the transfer at the correct time during the scan of the display and that it must be fast enough.

10.3.4.4.3.1 DSI Video Mode

Video mode refers to the MIPI display pixel interface (DPI) standard. The sync events and pixels must be sent according to the display mode timings. Data is received from the video ports. The DISPC fetches the data from the system memory and provides it to the DSI protocol engine through VP1 or VP2. The short packets used for the sync event use precalculated 32-bit values. The long packets are constructed using the header defined in the DSI_VC_LONG_PACKET_HEADER_i registers. In case of synchronization short packets for video mode, because hardware generates short packets without using the DSI_VC_SHORT_PACKET_HEADER_i register, if the DSI_VC_CTRL_i[8] ECC_TX_EN bit is set, the ECC is calculated; otherwise, 0 is used. This feature is used to generate incorrect ECC for debugging purposes and to ease the check of the link and peripheral error detection and correction.

The DSI_VM_TIMING1 through DSI_VM_TIMING8 registers define the timings of the video mode.

The DSI_VM_TIMING2[27:24] WINDOW_SYNC bit field defines the synchronization period. The recommended value is 0x4 based on the implementation of the resynchronization scheme.

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The DSI_CTRL[20] BLANKING_MODE bit defines whether long blanking packets or LPS are used during the blanking periods (except HFP, HBP, and HSA defined by other bits) when there is no pending data in TX FIFO ready to be sent. Software must ensure that there is no data in the TX FIFO, no BTA, no RESET trigger sent, and the DSI_VC_CTRL_i[9] MODE_SPEED bit is set to 1 (HS mode) to keep the video mode transfer in HS mode during blanking periods (except for the last blanking period, because it is required to go to LPS at least once per frame).

The following bits define whether during these blanking packets data from TX FIFO or long blanking packets are sent:

- DSI_CTRL[21] HFP_BLANKING_MODE
- DSI_CTRL[22] HBP_BLANKING_MODE
- DSI_CTRL[23] HSA_BLANKING_MODE

To ensure that the writes to the DSI_VC_LONG_PACKET_HEADER_i register are handled correctly as header information for video mode long packets, the following registers must be programmed:

- DSI_VC_CTRL_i[0] VC_EN bit set to 0
- DSI_VC_CTRL_i[4] MODE bit set to 1
- DSI_VC_LONG_PACKET_HEADER_i register access
- DSI_VC_CTRL_i[0] VC_EN bit set to 1

NOTE: The hardware ignores the DSI_VC_CTRL_i[1] SOURCE and DSI_VC_CTRL_i[9] MODE_SPEED bits when video mode is selected (the DSI_VC_CTRL_i[4] MODE bit is set to 1).

The SYNC_LOST_IRQ and RESYNCHRONIZATION_IRQ interrupt events indicate whether or not the DSI protocol engine has been able to resynchronize the video port timing to its own timing base. The RESYNCHRONIZATION_IRQ indicates to the software user that the video port works but the configuration of the timings for the DISPC and for DSI protocol engine may need to be modified to avoid the resynchronization. The SYNC_LOST_IRQ and RESYNCHRONIZATION_IRQ events, respectively, can be monitored in the DSI_IRQSTATUS[18] SYNC_LOST_IRQ and DSI_IRQSTATUS[5] RESYNCHRONIZATION_IRQ status bits.

10.3.4.4.3.2 DSI Command Mode

The command mode refers to the MIPI display command set (DCS) standard. The commands, parameters, and pixels are sent to the display module with limited real-time constraints (as defined in Section 10.3.4.4.3.1, *Video Mode*). The pixels can be provided on one of the two video ports by the DISPC or on the L3_MAIN interconnect slave port.

The DSI_VC_LONG_PACKET_HEADER_i registers are used for the header of long packets; the DSI_VC_SHORT_PACKET_HEADER_i registers are used for short packets.

For the payload, the DSI_VC_LONG_PACKET_PAYLOAD_i register is used. Each 32-bit payload data is written to the DSI_VC_LONG_PACKET_PAYLOAD_i register from the MPU subsystem or DMA_SYSTEM. It is buffered to send packets with a higher rate than the L3_MAIN interconnect frequency can provide. If the DSI_VC_CTRL_i[30] DCS_CMD_ENABLE bit is set to 1, the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register is used to determine the number of bytes to be sent using the DSI_VC_LONG_PACKET_PAYLOAD_i register minus the size of the DCS command header added by the protocol engine at the beginning of the payload (also sent using the DSI_VC_LONG_PACKET_PAYLOAD_i register). If the DSI_VC_CTRL_i[30] DCS_CMD_ENABLE bit is set to 0, the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register is used to determine the number of bytes to be sent using the DSI_VC_LONG_PACKET_PAYLOAD_i register.

The DSI_VC_CTRL_i[11:10] OCP_DATA_BUS_WIDTH bit field is used to define the size of the data on the L3_MAIN interconnect slave port for the write access (read access to the RX FIFO is not affected by the bit field value):

- 0x0: 16-bit data width (LSB of the 32-bit interface port data bus)
- 0x1: 24-bit data width (LSB of the 32-bit interface port data bus)

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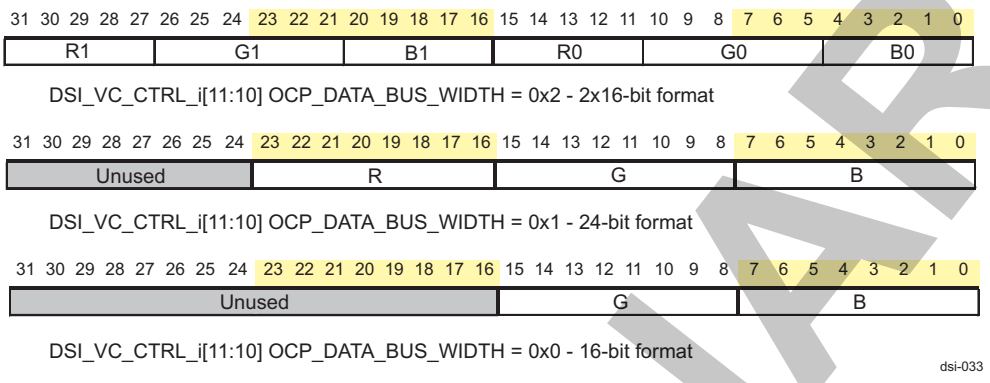
- 0x2: 2 × 16-bit data width (first pixel on the LSB of the 32-bit interface port data bus and second pixel on the MSB of the 32-bit interface port data bus for the same interface access)
- 0x3: 32-bit data width (no bit, no byte, no pixel manipulation)

Figure 10-122 shows the different data width configurations of the L3_MAIN interconnect slave port.

Figure 10-122. DSI Interface Data Configuration



NOTE: To provide 18-bit pixel loosely packed format to the L3_MAIN interconnect slave port, the DSI_VC_CTRL_i[11:10] OCP_DATA_BUS_WIDTH bit field must be set to 0x1. The 18-bit pixel packed format is not supported in case of command mode on the L3_MAIN interconnect slave port.

The write into the DSI_VC_LONG_PACKET_HEADER_i register is required before accessing the DSI_VC_LONG_PACKET_PAYLOAD_i register. The DSI protocol engine must extract the length of the payload and discard the extra data sent using the DSI_VC_LONG_PACKET_PAYLOAD_i register. Writes into the DSI_VC_LONG_PACKET_HEADER_i register are valid only if the VC is enabled; otherwise, the write is ignored. When receiving pixels on the video port, only the DSI_VC_LONG_PACKET_HEADER_i register is used. The video port pixels are used for the payload.

10.3.4.4.3.2.1 DSI Command Mode TX FIFO

The single TX FIFO is used to store data from the L3_MAIN interconnect before sending it to the panel. The configuration of the FIFO for a specific VC must be done only when the VC is disabled.

The VC must not be enabled when data is still pending in the TX FIFO for the corresponding space allocated for the VC from the previous active period. When the VC space in the TX FIFO is empty, the VC can be enabled.

For each VC, two dedicated registers (DSI_VC_LONG_PACKET_HEADER_i and DSI_VC_LONG_PACKET_PAYLOAD_i) are used to provide data for long packets. The DSI_VC_SHORT_PACKET_HEADER_i register is used to provide data for short packets (32 bits long).

For each long packet, the DSI_VC_LONG_PACKET_HEADER_i register must be written first, followed by the DSI_VC_LONG_PACKET_PAYLOAD_i register. The only exception is when the word count defined in the header equals 0. In that case, it is not required to write into the payload register. For consecutive long packets, the header must be written into the DSI_VC_LONG_PACKET_HEADER_i register even if the value remains the same.

The TX FIFO stores all the pending bytes to be sent to the peripheral(s). Multiple receivers can be addressed using the VC capability.

The 32-bit write requests for each VC to the TX FIFO are kept in order while sending the data to the DSI_PHY_DSS_x inside the VC requests. The only exception is the last 32-bit write for the last bytes of the payload data, because it can be 1, 2, 3, or 4 bytes.

When the last transfer is a 32-bit write, but the number of valid bytes is only 1, 2, or 3 (calculated using the header word count and the number of bytes are received for the payload), hardware stores the 32-bit value into the TX FIFO but the invalid bytes are not sent and are discarded.

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When the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register is not a multiple of the request threshold value defined in the DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD bit field, 32-bit requests and/or bytes are discarded by hardware to store in FIFO only the exact number of valid bytes.

The triggering event to send data to the DSI link is one of the following events:

- All bytes have been received in the FIFO (header + payload).
- The space of the FIFO allocated for the VC is full.
- The space of the FIFO allocated for the VC is not enough to request more data using DMA request (the threshold value is bigger than the space left in the TX FIFO for the VC).
- When the VC is disabled, the remaining bytes in the FIFO are sent to the DSI link.

NOTE: In case video mode is active, the blanking period must be large enough to allow the transfer of the packet(s).

Sequential arbitration must be set (DSI_CTRL[3] TX_FIFO_ARBITRATION = 0x1) if only one VC is used to send multiple packets during the same blanking period.

When consecutive packets must be sent to HS mode, to ensure that there is no LP transition between them, at least one of the following conditions must be valid:

- Packets from the same VC
- Short packets or long packets with a payload size multiple of 4 bytes

To stop a transfer immediately when packets are being transferred from the TX FIFO to DSI_PHY_DSS_x, a flush of the FIFO is necessary. It can be required in a dead-lock situation to flush the FIFO even if bytes are still in the FIFO. In that case, it is necessary to ensure having a known state of the whole DSI protocol engine module (software reset may be required) to the start of a new transfer through the TX FIFO.

To flush the FIFO (discard the data) for some pending bytes:

1. Change the size of the space of FIFO to 0 by writing DSI_TX_FIFO_VC_SIZE VCi_FIFO_SIZE bit fields (where i is the VC number from 0 to 3).
2. Disable the VC by resetting the DSI_VC_CTRL_i[0] VC_EN bit to 0.
3. Wait for DSI_VC_CTRL_i[15] VC_BUSY = 0 (VC_BUSY is set to 0 after TX FIFO flush is done).

It is necessary to check that there is no pending request before changing the size of the allocated FIFO for the VC by reading the relevant DSI_VC_CTRL_i[15] VC_BUSY bit or by using the interrupt PACKET_SENT_IRQ. This interrupt is monitored by reading the DSI_VC_IRQSTATUS_i[2] PACKET_SENT_IRQ status bit.

The DSI_CTRL[3] TX_FIFO_ARBITRATION bit defines the arbitration scheme:

- Round-robin between enabled VCs with pending ready requests (that is, all bytes for the packets are in the FIFO or the space of the FIFO for the VC is full) starting from the VC that has the lowest VC ID number.
- Sequential: All the pending ready requests for one VC are sent before moving to another VC. The condition of "space of the FIFO is full" is evaluated after the end of each packet.

To use in-order for all requests for all channels, a single VC must be used. (The VC ID defined in the header provided to the hardware using the DSI_VC_LONG_PACKET_HEADER_i or DSI_VC_SHORT_PACKET_HEADER_i register is not used and not modified by the DSI protocol engine.)

The DSI_TX_FIFO_VC_SIZE register defines the allocated number of 33-bit values for each VC in the TX FIFO and the start address for each VC. The size of the space allocated in the TX FIFO is defined by the DSI_TX_FIFO_VC_SIZE register VCi_FIFO_SIZE bit field. It must be a multiple of the threshold defined in the DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD bit field. To change the size of the space of the memory allocated for a specific VC, the VC must be disabled by setting the DSI_VC_CTRL_i[0] VC_EN bit to 0. The whole FIFO cannot be used by all the VCs at the same time because a VC can be disabled to change one or multiple parameters. Software users must configure the start address and size for each VC correctly.

Table 10-522 lists the corresponding values for the size of the space allocated in the FIFO.

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Table 10-522. DSI VC TX FIFO Size Values

DSI_TX_FIFO_VC_SIZE.VCi_FIFO_SIZE (where i = 0, 3)	Space Size (up to the size of the FIFO)
0	0 × 33 bits
1	32 × 33 bits
2	64 × 33 bits
3	96 × 33 bits
4	128 × 33 bits

NOTE: TX FIFO is 128 × 33 bits. Therefore, the sum of all VC FIFO allocations cannot exceed 128 × 33 bits.

CAUTION

Bit 32 of each location in the FIFO is used by the DSI protocol engine to tag the data in the TX FIFO. It is for internal use only.

Table 10-523 lists the start address of the space in the FIFO.

Table 10-523. DSI VC TX FIFO Start Address

DSI_TX_FIFO_VC_SIZE.VCx_FIFO_ADD (where x = 0, 2)	Start Address
0	0
1	32
2	64
3	96
4	128

CAUTION

The different VC spaces must not overlap.

When the TX FIFO is full:

- The overflow interrupt (FIFO_TX_OVF_IRQ) is generated in the DSI_VC_IRQSTATUS_i[3] FIFO_TX_OVF_IRQ status bit.
- There is no L3_MAIN interconnect error generated.
- The interface commands are accepted but the data are not written into the FIFO.

To ensure that all writes are stored correctly in the TX FIFO, the FIFO must not be full. The room in the space allocated for the VC in the TX FIFO is given in the DSI_TX_FIFO_VC_EMPTINESS register. When no space is allocated in the TX FIFO for the VC, the DSI_TX_FIFO_VC_EMPTINESS register indicates a value of 0 for the VC space emptiness.

While waiting to receive the first VSYNC event on the video port to start video mode on the DSI link, no command data from TX FIFO is sent on the interface. This is required to ensure that when receiving the VSYNC event there is no ongoing command mode transfer that could delay the start of video mode on the DSI link.

10.3.4.4.3.2.2 DSI Command Mode RX FIFO

The RX FIFO stores the data received from the DSI PHY. The data are always packed in the RX FIFO (single or multiple packets received during single or multiple BTA periods).

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The read requests (single or burst) can be less than, equal to, or greater than the packet size. If the packet size is smaller than the read request, the following packet(s) is also transferred. If the packet size is longer than the read request, only part of the packet is transferred. In that case, the logic keeps the VC information to provide the rest of the data during the next read request(s).

The DSI_RX_FIFO_VC_SIZE register defines the allocated number of 33-bit values for each VC in the RX FIFO and the start address for each VC. Only the enabled VCs are considered.

To change the size of the memory space allocated for a specific VC, the VC must be disabled by resetting the DSI_VC_CTRL_i[0] VC_EN bit to 0. The entire FIFO cannot be used by the entire VC at the same time because a VC can be disabled to change one or multiple parameters. Software users must configure the start address and size for each VC correctly.

Table 10-524 lists the corresponding values for the size of the space allocated in the FIFO:

Table 10-524. DSI VC RX FIFO Size Values

DSI_RX_FIFO_VC_SIZE.VCi_FIFO_SIZE (where i = 0, 3)	Space Size (up to the size of the FIFO)
0	0 × 33 bits
1	32 × 33 bits
2	64 × 33 bits
3	96 × 33 bits
4	128 × 33 bits

NOTE: RX FIFO is 128 × 33 bits. Therefore, the sum of all VC FIFO allocations cannot exceed 128 × 33 bits.

CAUTION

Bit 32 of each location in the FIFO is used by the DSI protocol engine to tag the data in the RX FIFO. It is for internal use only.

Table 10-525 lists the start address of the space in the FIFO.

Table 10-525. DSI VC RX FIFO Start Address

DSI_RX_FIFO_VC_SIZE.VCx_FIFO_ADD (where x = 0, 2)	Start Address
0	0
1	32
2	64
3	96
4	128

CAUTION

The different VC spaces must not overlap.

While reading the received bytes in the RX FIFO, only the DSI_VC_SHORT_PACKET_HEADER_i register is used, because hardware does not keep track of the header position for long packets and the start/end of each packet. Software must extract the information from the bytes read from the RX FIFO. There is no specific hardware to track the received bytes in the RX FIFO. The DSI_VC_LONG_PACKET_HEADER_i and DSI_VC_LONG_PACKET_PAYLOAD_i registers are not used.

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The ECC is used only by the first header when receiving multiple packets during the same LP RX transfer from the peripheral because the DSI protocol engine does not parse the header to identify the length of the packets. In case of multiple packets, the checksum is not enabled because hardware checks the checksum considering a single packet. The ECC in the first header is used to correct and check the header. For the following headers in the same LP RX transfer, hardware does not detect a header and cannot check and/or detect errors in the headers of the packets except for the first packet.

When the RX FIFO is empty:

- No interface error is generated.
- Commands are accepted and the data for the responses are 0s.

10.3.4.4.3.2.3 DSI Command Mode DMA Requests

The DMA requests (DSI_DMA_REQ) are used to allow automatic transfer by the DMA_SYSTEM or MPU (with less efficiency and throughput capability) from the DSI RX FIFO to the system memory and from the system memory to the DSI TX FIFO. Two independent DMA requests for RX FIFO and TX FIFO for the same VC are supported. The read and write accesses can use burst structure.

The thresholds used for requests for the TX FIFO and RX FIFO are programmable through the DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD and DSI_VC_CTRL_i[26:24] DMA_RX_THRESHOLD bit fields for TX FIFO and RX FIFO, respectively. DMA requests are asserted on the threshold value. The size of the space allocated in TX FIFO for each VC must be a multiple of the value of the DSI_VC_CTRL_i[19:17] DMA_TX_THRESHOLD bit field.

In the case of TX FIFO, if all the bytes defined by the word count field in the DSI_VC_LONG_PACKET_HEADER_i register are received, the DMA request is no longer asserted. Even during the last transfer, less than the DMA_TX_THRESHOLD number of bytes are received because the word count is not a multiple of the DMA_TX_THRESHOLD value.

In the case of RX FIFO, while the DMA request is used to transfer the data from the RX FIFO to the system memory, the DMA_SYSTEM must be programmed to read the exact number of received bytes in the FIFO. If users do not know the size of the received bytes, the direct access of the RX FIFO through the DSI_VC_SHORT_PACKET_HEADER_i register is performed until the DSI_VC_CTRL_i[20] RX_FIFO_NOT_EMPTY bit goes to 0.

The only exception is when the LP data transfer finishes and the threshold value is not reached. In this case, the DMA request is asserted. The drain of the FIFO is supported in that configuration to empty the FIFO even if the number of data received is not a multiple of the threshold value.

The use of each DMA request is programmable by software. The DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB bit field is dedicated to DMA request numbering for the TX FIFO. The DSI_VC_CTRL_i[29:27] DMA_RX_REQ_NB bit field is dedicated to DMA request numbering for the RX FIFO.

When the DMA request is used to indicate the number of 32-bit values ready in the RX FIFO that BTA has received from the peripheral, which indicates an end of the transfer from the peripheral to the host for a transfer to the system memory, the DMA request that corresponds to the VC ID is generated.

The DMA_SYSTEM transfers the number of 32-bit values defined in the threshold register or the exact number of bytes received from the peripheral (the user must know the number of expected received bytes to program the DMA_SYSTEM correctly). When the DMA_SYSTEM transfers a multiple number of threshold values, the DSI protocol engine sends 0s for the data when there is no more received data in the RX FIFO for the VC. Software users must parse the data and determine the valid bytes.

The size of the DMA transfer can be determined by reading the DSI_RX_FIFO_VC_FULLNESS register. The BTA interrupt (BTA_IRQ) must be used to determine when to read the number of received bytes. The BTA interrupt must be monitored by reading the DSI_VC_IRQSTATUS_i[5] BTA_IRQ status bit. The DMA request must not be enabled until the DMA_SYSTEM is programmed with the correct number of data to read from RX FIFO.

This method must also be used when the RX FIFO space for the VC is expected to overflow because the expected number of data to be received is greater than the space allocated for the VC. Instead, the DMA request is asserted as soon as the threshold is reached or when BTA is received.

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When the DMA request is used to indicate the number of 33-bit entries empty in the TX FIFO for a transfer from the system memory, the DMA request corresponding to the VC ID is generated.

NOTE: For the most efficient transfer, the size of the request (read or write, single or burst) must be aligned with the threshold value.

Concurrent access using interlaced requests (read/write) to the TX and RX FIFO is supported for the same VC ID or different VC IDs.

10.3.4.4.3.3 DSI Video + Command Mode

The two modes can be interlaced to send two DSI streams to two types of panels: video and command. The number of concurrent video streams is limited to one. The number of concurrent command mode streams is limited to four when there is no video stream, and three when there is a video stream.

- For DSI1_A and DSI1_C, which have two video ports (see Section 10.3.4.4.5, *DSI Video Port Interface*), it is possible to send video or command mode streams from DISPC to DSI1_x primary video port (VP1), and a command stream on the secondary VP (VP2) for interleaving. In addition, it is also possible to send concurrently a command mode stream on the L3_MAIN Interconnect slave port for interleaving.

10.3.4.4.3.4 DSI Burst Mode

Frequency and transparent burst modes are supported:

- Frequency burst mode is used to reduce the HS period by increasing the clock frequency on the DSI link. In some cases, it reduces power consumption on the link. The non-HS period used typically to drive the main panel can be used to send data to the secondary panel or to allow feedback (acknowledge) from the primary and secondary panels. The DSI protocol engine must buffer a full line before sending the HS packets for the line. A double-buffering mechanism is required to send a line while the following one is being received on the video port. For more information about double-buffering, see Section 10.3.4.4.5.4, *Ping-Pong Buffer*.
- The transparent burst mode is used by increasing the pixel clock frequency generated by the DISPC with an increase of the horizontal blanking period.

10.3.4.4.3.5 DSI Interleaving Mode

Video mode can output command mode packets, which are provided to DSI through the L3_MAIN interconnect during the blanking periods of the video stream sequence on the PPI link. These command mode packets can be programmed as HS packets or low-power packets.

During a video stream sequence on the PPI link, four types of gap exist:

- BLLP gap: Blanking period during VSA, VBP, and VFP lines
- HSA gap: Blanking period during VACT lines; always between HS and HE short packet
- HBP gap: Blanking period during VACT lines; always between HS/HE short packet and data pixel long packet
- HFP gap: Blanking period during VACT lines; always between data pixel long packet and the end of the current VACT line

To perform interleaving in a particular gap, video mode must be set to go into LPS during the blanking gap. Each type of gap has separate configurable register bits that determine whether a blanking long packet will be sent or the link will go into LPS during the gap on the PPI link. If LPS is set during a gap, the DSI module performs interleaving during that period.

Two sets of registers are available for:

- HS interleaving (when HS command mode packets must be sent during a video stream on the PPI link)
- Low-power interleaving (when low-power command mode packets must be sent during a video stream on the PPI link)

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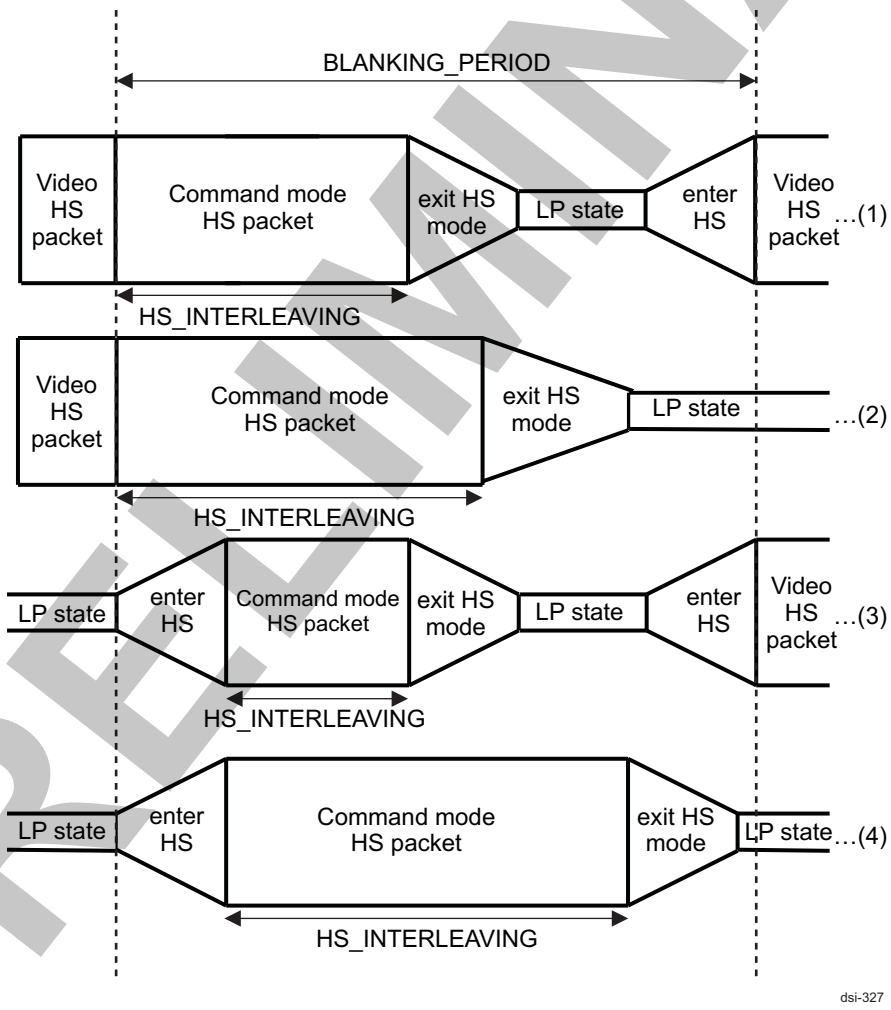
10.3.4.4.3.5.1 DSI HS Command Mode Interleaving

Figure 10-123 shows the various HS mode scenarios in interleaving mode during a blanking gap. For each type of blanking gap, a dedicated bit field determines the number of TXBYTECLKHS clock cycles used for interleaving in HS command mode packets.

- The DSI_VM_TIMING6[31:16] BL_HS_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during a BLLP gap.
- The DSI_VM_TIMING4[7:0] HBP_HS_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during an HBP gap.
- The DSI_VM_TIMING4[15:8] HFP_HS_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during an HFP gap.
- The DSI_VM_TIMING4[23:16] HSA_HS_INTERLEAVING bit field defines the number of TXBYTECLKHS clock cycles used to interleave HS command mode packets during an HSA gap.

These programmable values must be programmed to satisfy the timings for the clock and data lane to enter and exit HS mode latency. According to the scenario, different equations must be considered when calculating the register values.

Figure 10-123. DSI HS Command Mode Interleaving



NOTE: For calculations and equations, the following abbreviations are used: EXIT_CLK_HS_MODE represents the exit HS mode latency for the clock lane. There is no dedicated register for this value but the programmer must know this value for further calculations:

$$EXIT\_CLK\_HS\_MODE = T_{CLK\text{-}TRAIL} + TH_{S\text{-}EXIT}$$

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NOTE: For more information about other timing parameters used in the following equations, see Section 10.3.4.4.4.1, *Timing Parameters for an LP-to-HS Transaction*, and Section 10.3.4.4.4.2, *Timing Parameters for an HS-to-LP Transaction*.

For the following equations, BLANKING_PERIOD represents the BLLP, HSA, HBP, or HFP blanking periods. The HS_INTERLEAVING period represents the maximal period HS command mode packets. Its value is set in the following bit fields, depending on the blanking type:

- BL_HS_INTERLEAVING
- HSA_HS_INTERLEAVING
- HBP_HS_INTERLEAVING
- HFP_HS_INTERLEAVING

In each scenario, two calculations are present, depending on the value of the DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit:

- DDR_CLK_ALWAYS_ON = 1: Clock lane is always active.
- DDR_CLK_ALWAYS_ON = 0: Clock lane is activated only when there are HS packets to be sent on the PPI link.

CAUTION

When the DDR_CLK_ALWAYS_ON bit is programmed to 1, the following must be considered:

- LPS can be achieved on the PPI link only if the data lane has enough time to go out from HS mode and enter a new HS mode during a period inside which the PPI link is meant to be in LPS. This can be expressed with the following equation:

  EXIT_HS_MODE_LATENCY + max{ENTER_HS_MODE_LATENCY, 2} + 1 ≤ BLANKING_PERIOD
- If the equation cannot be satisfied, because the LPs period is too short, software must program the DSI module in a way that during this blanking period a HS blanking packet is sent.

When the DDR_CLK_ALWAYS_ON bit is programmed to 0, the following must be considered:

- LPS can be achieved on the PPI link only if the data and clock lanes have enough time to go out from HS mode and enter a new HS mode during a period inside which the PPI link is meant to be in LPs. This can be expressed with the following equations:

  EXIT_HS_MODE_LATENCY + max{ENTER_HS_MODE_LATENCY, 2} + 1 ≤ BLANKING_PERIOD

  DDR_CLK_POST + EXIT_CLK_HS_MODE + DDR_CLK_PRE + ENTER_HS_MODE_LATENCY(data lane) + 1 ≤ BLANKING_PERIOD
- If both equations cannot be satisfied, because the LPS period is too short, software must program the DSI module in a way that during this blanking period a HS blanking packet is sent.

- Scenario 1: The gap for interleaving starts and ends with a regular video stream HS packet.
  - DDR_CLK_ALWAYS_ON = 1

    HS_INTERLEAVING = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + max{ ENTER_HS_MODE_LATENCY, 2} + 1)
  - DDR_CLK_ALWAYS_ON = 0

    HS_INTER1 = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + max{

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ENTER_HS_MODE_LATENCY, 2} + 1)

HS_INTER2 = BLANKING_PERIOD – (DDR_CLK_POST + EXIT_CLK_HS_MODE + DDR_CLK_PRE + ENTER_HS_MODE_LATENCY + 1)

HS_INTERLEAVING = min{HS_INTER1, HS_INTER2}

- Scenario 2: The gap for interleaving starts with a regular video stream HS packet and ends in LPS.
  - DDR_CLK_ALWAYS_ON = 1

    HS_INTERLEAVING = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + 3)
  - DDR_CLK_ALWAYS_ON = 0

    HS_INTER1 = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + 3)

    HS_INTER1 = BLANKING_PERIOD – (DDR_CLK_POST + EXIT_CLK_HS_MODE + 3)

    HS_INTERLEAVING = min{HS_INTER1, HS_INTER2}
- Scenario 3: The gap for interleaving starts with LPS and ends with a regular video stream HS packet.
  - DDR_CLK_ALWAYS_ON = 1

    HS_INTERLEAVING = BLANKING_PERIOD – (ENTER_HS_MODE_LATENCY + EXIT_HS_MODE_LATENCY + max{ ENTER_HS_MODE_LATENCY, 2} + 1)
  - DDR_CLK_ALWAYS_ON = 0

    HS_INTER1 = BLANKING_PERIOD – (DDR_CLK_PRE + ENTER_HS_MODE_LATENCY + EXIT_HS_MODE_LATENCY + max{ENTER_HS_MODE_LATENCY, 2} + 1)

    HS_INTER2 = BLANKING_PERIOD – (DDR_CLK_PRE + ENTER_HS_MODE_LATENCY + DDR_CLK_POST + EXIT_CLK_HS_MODE + DDR_CLK_PRE+ ENTER_HS_MODE_LATENCY + 1)

    HS_INTERLEAVING = min{HS_INTER1, HS_INTER2}
- Scenario 4: The gap for interleaving starts with LPS and ends with a regular video stream HS packet.
  - DDR_CLK_ALWAYS_ON = 1

    HS_INTERLEAVING = BLANKING_PERIOD – (ENTER_HS_MODE_LATENCY + EXIT_HS_MODE_LATENCY + 3)
  - DDR_CLK_ALWAYS_ON = 0

    HS_INTER1 = BLANKING_PERIOD – (DDR_CLK_PRE + ENTER_HS_MODE_LATENCY + EXIT_HS_MODE_LATENCY + 3)

    HS_INTER2 = BLANKING_PERIOD – (DDR_CLK_PRE + ENTER_HS_MODE_LATENCY + DDR_CLK_POST + EXIT_CLK_HS_MODE + 1)

    HS_INTERLEAVING = min{HS_INTER1, HS_INTER2}

10.3.4.4.3.5.2 DSI LP Command Mode Interleaving

Figure 10-124 shows the various LP mode scenarios in interleaving mode during a blanking gap. For each type of blanking gap, a dedicated bit field determines the number of bytes of LP command mode packets that can be sent during a blanking period.

- The DSI_VM_TIMING6[15:0] BL_LP_INTERLEAVING bit field defines the number of bytes of LP command mode packets that can be sent during a BLLP gap.
- The DSI_VM_TIMING5[7:0] HBP_LP_INTERLEAVING bit field defines the number of bytes of LP command mode packets that can be sent during an HBP gap.
- The DSI_VM_TIMING5[15:8] HFP_LP_INTERLEAVING bit field defines the number of bytes of LP command mode packets that can be sent during an HFP gap.
- The DSI_VM_TIMING5[23:16] HSA_LP_INTERLEAVING bit field defines the number of bytes of LP command mode packets that can be sent during an HSA gap.

These values must be programmed to satisfy the timings for clock and data lane enter and exit LP mode latency. Clock lane timings do not affect LP command mode interleaving, because the clock lane can be controlled separately, compared with the data lane HS and low-power mutually exclusive control. Clock lanes can be in HS mode while the data lanes are in HS data transfer mode, low-power data transfer mode, or in LPS.

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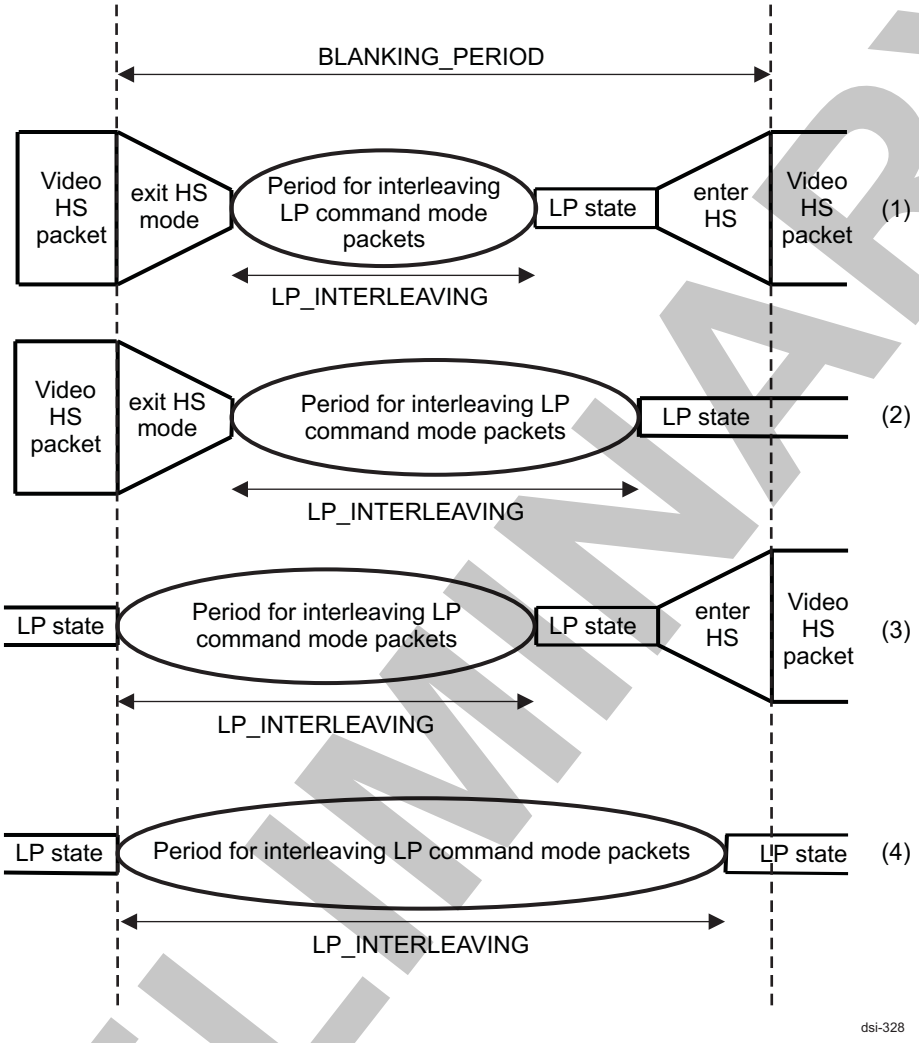
According to this scenario, different equations must be considered to calculate register values.

Figure 10-124. DSI LP Command Mode Interleaving



For the following equations, BLANKING_PERIOD represents the BLLP, HSA, HBP, or HFP blanking periods. The LP_INTERLEAVING period represents the maximal period in LP command mode packets. Its value is set in the following bit fields, depending on the blanking type.

- BL_LP_INTERLEAVING
- HSA_LP_INTERLEAVING
- HBP_LP_INTERLEAVING
- HFP_LP_INTERLEAVING

ALLOWED_HSBYTE_CLOCKS_FOR_LP represents the number of TXBYTECLKHS clock cycles during which LP interleaving can appear.

To calculate the LP_INTERLEAVING value:

1. Calculate how many TXBYTECLKHS clock cycles can be reserved for LP interleaving during the appropriate blanking video mode gap.
2. Calculate the value of LP_INTERLEAVING according to the results of Step 1.

Step 1:

- Scenario 1: The gap for interleaving starts and ends with a regular video stream HS packet.

  ALLOWED_HSBYTE_CLOCKS_FOR_LP = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY +

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max{ENTER_HS_MODE_LATENCY, 2} + 1)

- Scenario 2: The gap for interleaving starts with a regular video stream HS packet and ends in LPS.
  ALLOWED_HSBYTE_CLOCKS_FOR_LP = BLANKING_PERIOD – (EXIT_HS_MODE_LATENCY + 1)
- Scenario 3: The gap for interleaving starts with the LPS and ends with a regular video stream HS packet.
  ALLOWED_HSBYTE_CLOCKS_FOR_LP = BLANKING_PERIOD – (max{ENTER_HS_MODE_LATENCY, 2} + 1)
- Scenario 4: The gap for interleaving starts with LPS and ends with a regular video stream HS packet.
  ALLOWED_HSBYTE_CLOCKS_FOR_LP = BLANKING_PERIOD – 1

After finishing Step 1, the time period available for LP interleaving is known:

$T_{lp\_available}$ = ALLOWED_HSBYTE_CLOCKS_FOR_LP *T TXBYTECLKHS

Step 2:

The resulting value must be programmed in the appropriate video mode register for LP interleaving.

$$LP\_INTERLEAVING < \left[\frac{\frac{Tlp\_available - 8*Thsbyte\_clk - 5*Tdsif\_clk}{Ttxclkesc}}{16} - 26 \right]$$

dsi-E124

Thsbyte_clk: Period of TXBYTECLKHS clock of the DSI_PHY_DSS_x module

Tdsif_clk: Period of DSI functional clock

Ttxclkesc: Period of LP transmit escape clock

10.3.4.4.4 DSI Clock Requirements

The serial clock generated by the DSI host and sent to the display can be a continuous clock. The clock lane supports clock transmission even if there is no data to send for displays that require continuous clock. It is software-programmed through the DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit: This bit can be programmed only when the interface is disabled (the DSI_CTRL[0] IF_EN bit set to 0).

The peripheral can use two different kinds of clocks. The first is the DDR clock provided on the clock lane. The second clock is some transitions on the first data lane even if there is no valid data to send using LP mode.

The LP clock (TxClkEsc) frequency provided to the DSI PHY is from 67 percent to 150 percent of the peripheral low-power (LP) clock frequency. It is generated internally by the DSI protocol engine module using the DSI functional clock. The DSI functional clock is divided by 1, 2, 3, up to 8191 using the value programmed in the DSI_CLK_CTRL[12:0] LP_CLK_DIVISOR bit field. The LP clock generated from the DSI functional clock must be from 20 MHz to 32 kHz. The duty cycle must be 50/50 (minimum high time = 24 ns). LP clock frequency visible on the pads (DP x or DN) is half the frequency of TxClkEsc.

The DSI_CLK_CTRL[20] LP_CLK_ENABLE bit is used to enable or disable the clock. When disabled, the value of the DSI_CLK_CTRL[12:0] LP_CLK_DIVISOR bit field is ignored and does not have to be programmed by software users.

10.3.4.4.4.1 DSI Timing Parameters for an LP-to-HS Transaction

Figure 10-125 shows the timing requirement when switching the data and clock lane state from LP to HS. Table 10-526 lists the LP to HS timing parameters.

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Figure 10-125. DSI LP-to-HS Timing

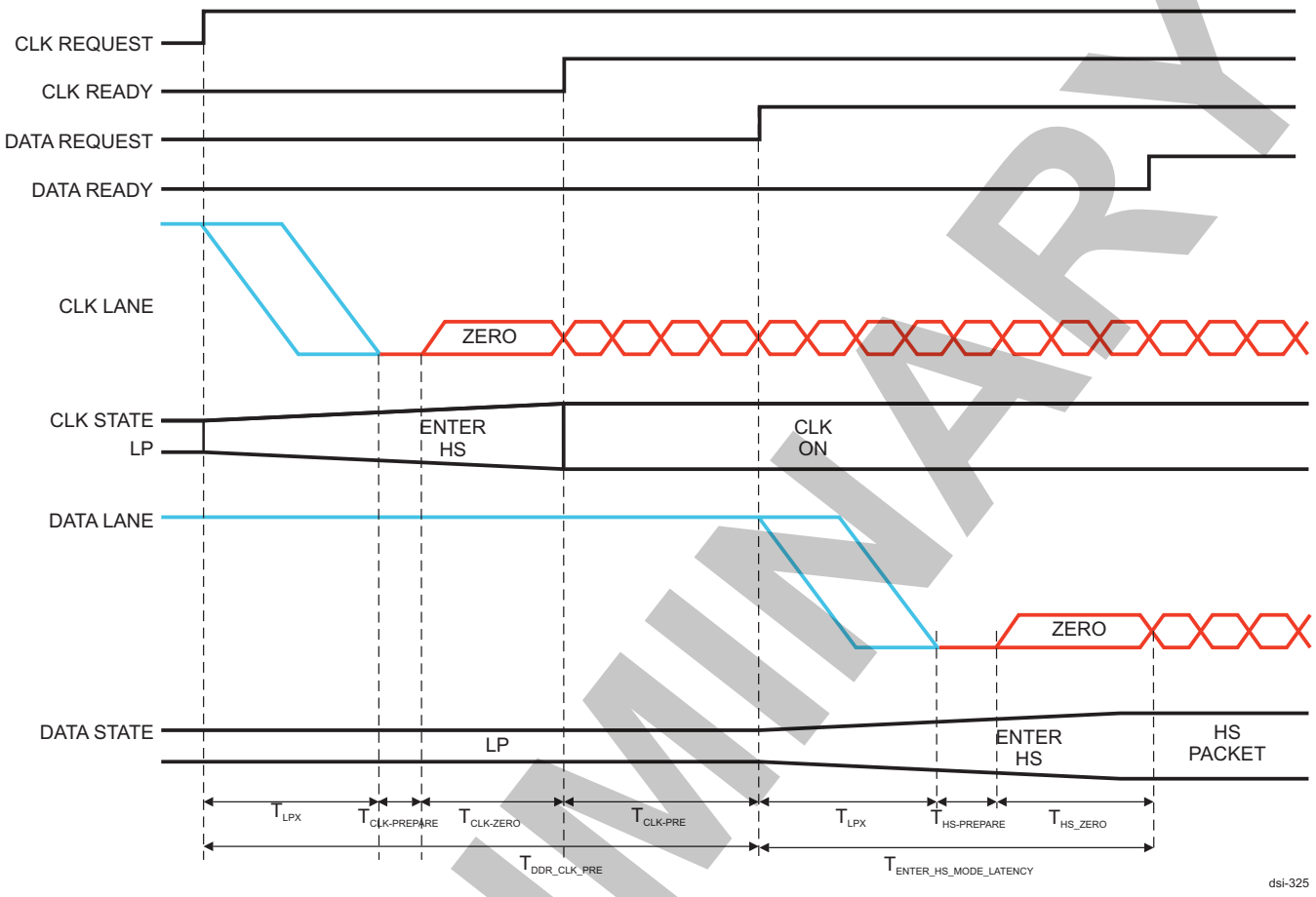

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Table 10-526. DSI LP-to-HS Timing Parameters

Timings	Description	Registers/Associated Bit Fields	Register Settings	Timing Seen on the Line
T_{LPX}	Length of any low-power state period	DSI_PHY_REGISTER1[20:16] REG_TLPXBY2 The value set in this bit field is half of the T_{LPX}	CEIL (25 ns / DDR_Clock_Period)	CEIL (2 * REG_TLPXBY2/4) * 4 * DDR_Clock_Period
$T_{CLK-PREPARE}$	Time to drive the CLK lane to LP-00 state, to prepare for HS clock transmission	DSI_PHY_REGISTER2[7:0] REG_TCLKPREPARE	CEIL (65 ns / DDR_Clock_Period)	REG_TCLKPREPARE * DDR_Clock_Period + (~–25– + 5 ns)
$T_{CLK-ZERO}$	Time to drive the CLK lane to HS-0 state, before starting the clock	DSI_PHY_REGISTER1[7:0] REG_TCLKZERO	CEIL (265 ns / DDR_Clock_Period)	{CEIL [(REG_TCLKZERO + 3)/4] * 4 + CEIL (REG_TCLKPREPARE/ 4) * 4 – REG_TCLKPREPARE + 2} * DDR_Clock_Period + (~ 0–+ 5 ns)
$T_{CLK-PRE}$	Time that the HS clock must be driven before any associated data lane begins the transition from LP to HS mode	N/A	N/A	DDR_CLK_PRE - T_{LPX} - $T_{CLK-PREPARE}$ - $T_{CLK-ZERO}$
$T_{HS-PREPARE}$	Time to drive the data lane to LP-00 state, to prepare for HS packet transmission	DSI_PHY_REGISTER0[31:24] REG_THSPREPARE	CEIL (70 ns / DDR_Clock_Period) + 2	REG_THSPREPARE * DDR_Clock_Period + (–26.5–+ 4 ns)
$T_{HS-ZERO}$ + $T_{HS-PREPARE}$	$T_{HS-ZERO}$: Time to drive the data lane to HS-0 state before the synchronous sequence	DSI_PHY_REGISTER0[23:16] REG_THSPRPR_THSZERO	CEIL (175 ns / DDR_Clock_Period) + 2	{CEIL [(N + 3)/4] * 4 + CEIL (M/4) * 4 + 3} * DDR_Clock_Period + (~ –29–0 ns). Where: N = REG_THSPREPARE_THSZERO – REG_THSPREPARE M = REG_THSPREPARE
$T_{DDR\_CLK\_PRE}$	Time between the CLK lane request assertion and the data request assertion to switch the data lanes to HS	DSI_CLK_TIMING[15:8] DDR_CLK_PRE	CEIL [(T_{LPX} + $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ + $T_{CLK-PRE}$) / $T_{TXBYTECLKHS}$] (1) (2)	
$T_{ENTER\_HS\_MODE\_LATENCY}$ (3)	Time to enter data lane into HS mode	DSI_VM_TIMING7[31:16] ENTER_HS_MODE_LATENCY	CEIL [(T_{LPX} + $T_{HS-PREPARE}$ + $T_{HS-ZERO}$) / $T_{TXBYTECLKHS}$] (1)	

(1) The timings seen on the line should be used to determine the register value.
(2) See the MIPI D-PHY specification for the $T_{CLK-PRE}$ value.
(3) ENTER_HS_MODE_LATENCY timing applies only to video mode. It does not need to be programmed in command mode.

In the example in Table 10-527, the DDR clock = 400 MHz; TxByteClkHS = 100 MHz.

Table 10-527. DSI LP-to-HS Timing Parameters Example for 400-MHz DDR Clock

Timings	Registers/Associated Bit Fields	Default Register Settings (Programmed at Reset)	Timing Seen on the Line
T_{LPX}	DSI_PHY_REGISTER1[20:16] REG_TLPXBY2	10	50 ns

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Table 10-527. DSI LP-to-HS Timing Parameters Example for 400-MHz DDR Clock (continued)

Timings	Registers/Associated Bit Fields	Default Register Settings (Programmed at Reset)	Timing Seen on the Line
$T_{CLK-PREPARE}$	DSI_PHY_REGISTER2[7:0] REG_TCLKPREPARE	26	40–70 ns
$T_{CLK-ZERO}$	DSI_PHY_REGISTER1[7:0] REG_TCLKZERO	106	280–285 ns
$T_{CLK-PRE}$ (1)	N/A	N/A	80 ns
$T_{HS-PREPARE}$	DSI_PHY_REGISTER0[31:24] REG_THSPREPARE	30	48.5–79 ns
$T_{HS-ZERO}$	DSI_PHY_REGISTER0[23:16] REG_THSPRPR_THSZERO	72	178.5–207.5 ns
$T_{DDR\_CLK\_PRE}$	DSI_CLK_TIMING[15:8] DDR_CLK_PRE	45–49 (2)	450–490 ns
$T_{ENTER\_HS\_MODE\_LATENCY}$	DSI_VM_TIMING7[31:16] ENTER_HS_MODE_LATENCY	24 * TXBYTECLKHS or 112 * DDR_CLOCK 34 * TXBYTECLKHS or 136 * DDR_CLOCK (2)	277–336.5 ns

(1) See the MIPI D-PHY specification for the $T_{CLK-PRE}$ value.
(2) Register setting calculated based on the values in the Timing Seen on the Line column.

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10.3.4.4.4.2 DSI Timing Parameters for an HS-to-LP Transaction

Figure 10-126 shows the timing requirement when switching the state of the data and clock lanes from HS to LP. Table 10-528 lists the HS-to-LP timing parameters.

Figure 10-126. DSI HS-to-LP Timing

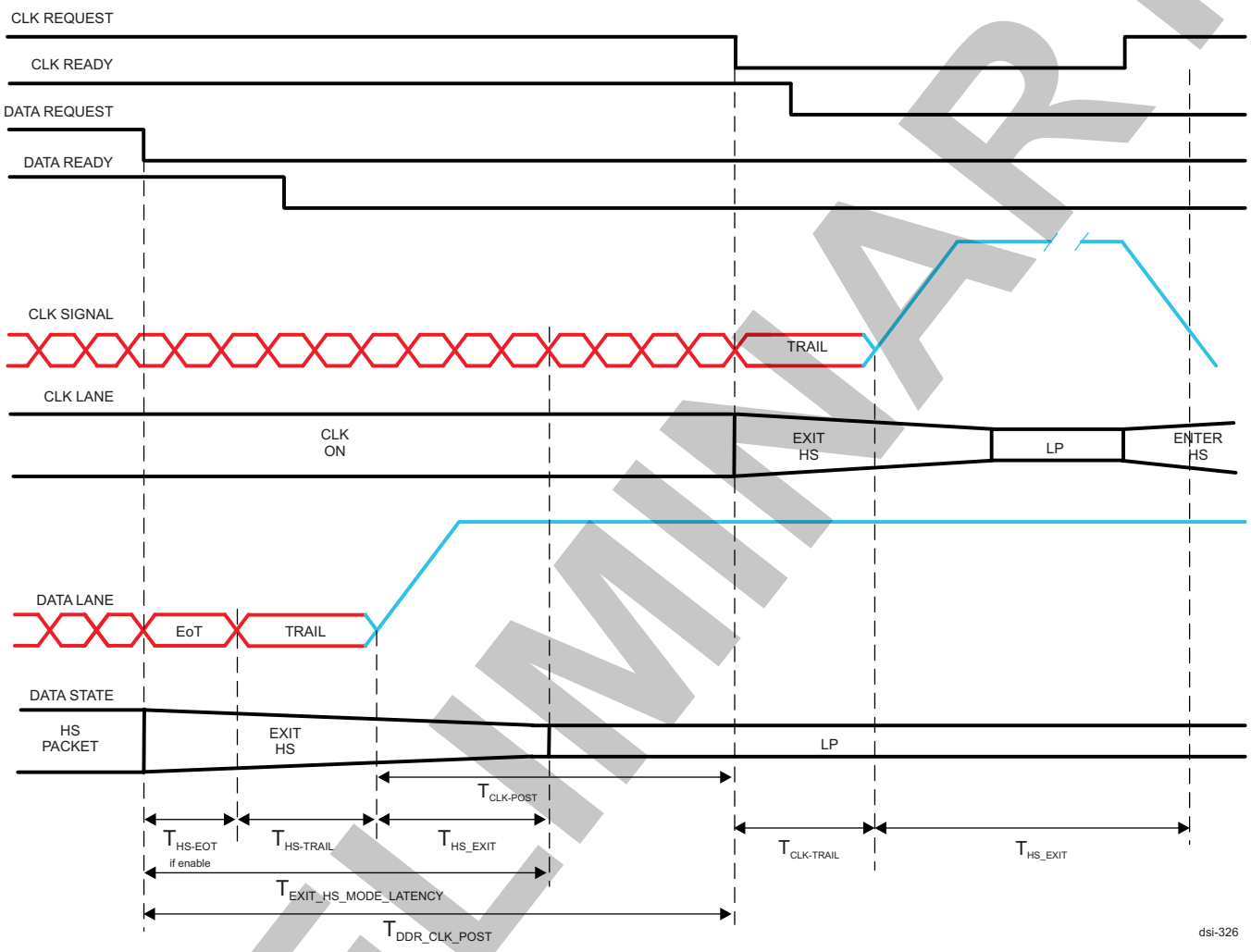

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Table 10-528. DSI HS-to-LP Timing Parameters

Timings	Description	Registers/Associated Bit Fields	Register Settings	Timing Seen on the Line
T_{HS-EOT}	If EoT is enabled, a delay is added to EXIT_HS_MODE_LATENCY to send the EoT packet. The EoT period depends on the number of data lanes.	N/A	N/A	DIVROUNDUP (4, NB_DATA_LANES) Thus: One data lane = Four DDR clocks Two data lanes = Two DDR clocks
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of an HS transmission burst	DSI_PHY_REGISTER0[15:8] REG_THSTRAIL	CEIL (60 ns / DDR_Clock_Period) + 5	{CEIL [(REG_THSTRAIL + 3)/4] * 4 – 2.75} * DDR_Clock_Period + (~ 0– 5 ns)
$T_{HS-EXIT}$	Time to drive data lane to LP-11 state, after HS burst	DSI_PHY_REGISTER0[7:0] REG_THSEXIT	CEIL (145 ns / DDR_Clock_Period)	[CEIL (REG_THSEXIT/4) * 4] * DDR_Clock_Period – (~ 3–45 ns)
$T_{CLK-POST}$	Time that the transmitter must continue sending HS clock after the last associated data lane has transitioned to LP mode	N/A	N/A	DDR_CLK_POST - T_{HS-EOT} (1) - $T_{HS-TRAIL}$
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of an HS transmission burst	DSI_PHY_REGISTER1[15:8] REG_TCLKTRAIL	CEIL (60 ns / DDR_Clock_Period) + 2	{CEIL [(REG_TCLKTRAIL + 3)/4] * 4 – 1.5} * DDR_Clock_Period + (~ 0– 5 ns)
$T_{DDR\_CLK\_POST}$	Time between the data lane request deassertion and the CLK request deassertion to switch the data lanes into LP mode. The DDR_CLK_POST value must follow the rule: DDR_CLK_POST ≥ $T_{HS-TRAIL}$ + T_{HS-EOT} + $T_{CLK-POST}$	DSI_CLK_TIMING[7:0] $T_{DDR\_CLK\_POST}$	CEIL [($T_{HS-TRAIL}$ + T_{HS-EOT} (1) + $T_{CLK-POST}$) / $T_{TXBYTECLKHS}$] (2) (3)	
$T_{EXIT\_HS\_MODE\_LATENCY}$ (4)	Time to exit HS mode	DSI_VM_TIMING7[15:0] EXIT_HS_MODE_LATENCY	CEIL [($T_{HS-TRAIL}$ + $T_{HS-EXIT}$ + T_{HS-EOT} (1)) / $T_{TXBYTECLKHS}$] (2)	

(1) If T_{HS-EOT} is enabled
(2) The timings seen on the line should be used to determine the register value.
(3) See the MIPI D-PHY specification for the$T_{CLK-POST}$ value.
(4) EXIT_HS_MODE_LATENCY timing applies only to video mode. It does not need to be programmed in command mode.

In the example in Table 10-529, the DDR clock = 400 MHz; TxByteClkHS = 100 MHz; two data lanes.

Table 10-529. DSI HS to LP Timing Parameters Example for 400-MHz DDR Clock and Two Data Lanes

Timings	Registers/Associated Bit Fields	Default Register Settings (Programmed at Reset)	Timing Seen on the Line (T_{HS-EOT} Enabled)	Timing Seen on the Line (T_{HS-EOT} Disabled)
T_{HS-EOT}	N/A	N/A	5 ns	N/A
$T_{HS-TRAIL}$	DSI_PHY_REGISTER0 [15:8] REG_THSTRAIL	29	73.125–78.125 ns	73.125–78.125 ns

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Table 10-529. DSI HS to LP Timing Parameters Example for 400-MHz DDR Clock and Two Data Lanes (continued)

Timings	Registers/Associated Bit Fields	Default Register Settings (Programmed at Reset)	Timing Seen on the Line (T_{HS-EOT} Enabled)	Timing Seen on the Line (T_{HS-EOT} Disabled)
$T_{HS-EXIT}$	DSI_PHY_REGISTER0 [7:0] REG_THSEXIT	58	105–147 ns	105–147 ns
$T_{CLK-POST}$ (1)	N/A	N/A	585 ns	580 ns
$T_{CLK-TRAIL}$	DSI_PHY_REGISTER1 [15:8] REG_TCLKTRAIL	26	76.25–81.25 ns	76.25–81.25 ns
DDR_CLK_POST	DSI_CLK_TIMING[7:0] DDR_CLK_POST	66 * TxByteClkHS or 264 * DDR_CLOCK	658.125–663.125 ns	653.125–658.125 ns
		67 * TxByteClkHS or 268 * DDR_CLOCK (2)		
EXIT_HS_MODE_ LATENCY	DSI_VM_TIMING7[15: 0] EXIT_HS_MODE_LAT ENCY	19 * TxByteClkHS or 76 * DDR_CLOCK	183.125–230.125 ns	178.125–225.125 ns
		24 * TxByteClkHS or 96 * DDR_CLOCK (2)		

(1) See the MIPI D-PHY specification.
(2) Register setting calculated based on the values in Timing Seen on the Line (T_{HS-EOT} Enabled) column.

10.3.4.4.4.3 DSI Extra LP Transitions

Some DSI receivers require extra clock cycles in LP mode to process the data. The DSI protocol engine can be programmed to send automatically one NULL long packet. It applies only when no more data are ready to be sent from the internal FIFO to the peripheral on the last LS transfer. The same value is used for all the VCs sending packets in LS mode.

The size of the payload is defined by the DSI_CLK_CTRL[17:16] LP_CLK_NULL_PACKET_SIZE bit field. The header value depends on the size of the payload as described in Table 10-530 and Table 10-531.

NOTE: In Table 10-530 and Table 10-531, ECC and checksum are enabled.

Table 10-530. DSI Extra NULL PH

VC ID	Payload Size (DSI_CLK_CTRL[17:16] LP_CLK_NULL_ PACKET_SIZE)	Header (1st Byte)	Header (2nd Byte): WC LSB	Header (3rd Byte): WC MSB	Header (ECC)
0x0	0	0x9	0x0	0x0	0x9
	1		0x1		0x13
	2		0x2		0x2F
	3		0x3		0x35
0x1	0	0x49	0x0		0x1F
	1		0x1		0x05
	2		0x2		0x39
	3		0x3		0x23
0x2	0	0x89	0x0		0x10
	1		0x1		0x0A
	2		0x2		0x36
	3		0x3		0x2C
0x3	0	0xC9	0x0		0x06
	1		0x1		0x1C

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Table 10-530. DSI Extra NULL PH (continued)

VC ID	Payload Size (DSI_CLK_CTRL[17:16] LP_CLK_NULL_ PACKET_SIZE)	Header (1st Byte)	Header (2nd Byte): WC LSB	Header (3rd Byte): WC MSB	Header (ECC)
	2		0x2		0x20
	3		0x3		0x3A

Table 10-531. DSI Extra NULL Packet Payload

Payload Size (DSI_CLK_CTRL[17:16] LP_CLK_NULL_PACKET_ SIZE)	Payload (1st Byte)	Payload (2nd Byte)	Payload (3rd Byte)	Payload (CRC) LSB	Payload (CRC) MSB
0	N/A(1)	N/A	N/A	0xFF	0xFF
1	0	N/A	N/A	0x87	0x0F
2	0	0	N/A	0xB8	0xF0
3	0	0	0	0x33	0x39

(1) N/A = Not available

10.3.4.4.5 DSI Video Port Interface

NOTE: The signals described in this section are internal and not bounded outside the device. This section describes the internal connections between the DISPC and the DSI protocol engine.

Table 10-532 and Table 10-533 summarize the video interface signals. DSI1_A and DSI1_C have two video ports (VP1 and VP2). These interfaces connect the DISPC outputs to the DSI protocol engine to send real-time data streams. For video mode, only the active matrix timings are supported by the DSI protocol engine.

- DSI1_A has two video ports (VP1 and VP2)
  - VP1 is connected to the LCD1 output of DISPC.
  - VP2 is connected to the LCD2 output of DISPC.
- DSI1_C has two video ports (VP1 and VP2)
  - VP1 is connected to the LCD1 output of DISPC.
  - VP2 is connected to the LCD3 output of DISPC.

Table 10-532. DSI Video Port 1 Signals for DSI1_A and DSI1_C Protocol Engines

Signal Name	Type(1)	Description
VP1_HSYNC	I	Horizontal synchronization signal
VP1_VSYNC	I	Vertical synchronization signal
VP1_DATA[23:0]	I	Parallel output data: Bits [23:0]
VP1_PCLK	I	Pixel clock. In case of STALL configuration, it is used to indicate when new data is on the data bus during the clock period of VP1_CLK. The VP1_PCLK is generated from VP1_CLK through division inside the DISPC. The clock ratio is indicated in the DSI_CTRL[4] VP_CLK_RATIO bit and must be aligned with the configuration of the clock divisor in the display controller (DISPC_DIVISOR1[7:0] PCD bit field for DISPC LCD1 output, and the DISPC_DIVISOR2[7:0] PCD bit field for DISPC LCD2 output). The source of the VP1_PCLK for DSI1_A is the DSS_DISPC_LCD1_PCLK. The source of the VP1_PCLK for DSI1_C is DSS_DISPC_LCD3_PCLK. For more information, see DISPC Clock Configurationin *Display Controller*, and , *DSI Clock Configuration*.
VP1_DE	I	Data enable
VP1_STALL	O	The STALL signal must be deasserted to receive pixel and asserted to stop receiving pixel. (It can be used only while the DISPC is configured in stall mode; in that mode, HSYNC and VSYNC are not generated.)

(1) I = Input; O = Output

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Table 10-532. DSI Video Port 1 Signals for DSI1_A and DSI1_C Protocol Engines (continued)

Signal Name	Type[1]	Description
VP1_CLK	I	DISPC internal clock. It is a free-running clock. The source of VP1_CLK for DSI1_A is LCD1_CLK, divided down. The source of VP1_CLK for DSI1_C is LCD3_CLK, divided down. For more information, see DISPC Clock Configurationin *Display Controller*, and , *DSI Clock Configuration*

Table 10-533. DSI Video Port 2 Signals for DSI1_A and DSI1_C Protocol Engines

Signal Name	Type[1]	Description
VP2_HSYNC	I	Horizontal synchronization signal
VP2_VSYNC	I	Vertical synchronization signal
VP2_DATA[23:0]	I	Parallel output data: Bits [23:0]
VP2_PCLK	I	Pixel clock. In case of STALL configuration, it is used to indicate when new data is on the data bus during the clock period of VP2_CLK. The VP2_PCLK is generated from VP2_CLK through division inside the DISPC. The clock ratio is indicated in the DSI_CTRL2[4] VP_CLK_RATIO bit and must be aligned with the configuration of the clock divisor in the display controller (DISPC_DIVISOR2[7:0] PCD bit field for DISPC LCD2 output). The source of the VP2_PCLK for DSI1_A is the DSS_DISPC_LCD2_PCLK. The source of the VP2_PCLK for DSI1_C is LCD1_PCLK. For more information, see DISPC Clock Configuration in *Display Controller*, and , *DSI Clock Configuration*.
VP2_DE	I	Data enable
VP2_STALL	O	The STALL signal must be deasserted to receive pixel and asserted to stop receiving pixel. (It can be used only while the DISPC is configured in stall mode; in that mode, HSYNC and VSYNC are not generated.)
VP2_CLK	I	DISPC internal clock. It is a free-running clock. The source of the VP2_CLK for DSI1_A is LCD2_CLK, divided down. The source of the VP2_CLK for DSI1_C is LCD1_CLK, divided down. For more information, see DISPC Clock Configuration in *Display Controller*, and , *DSI Clock Configuration*.

(1) I = Input; O = Output

NOTE:

- The polarities of VP_HSYNC and VP_VSYNC are programmable by setting the DSI_CTRL and DSI_CTRL2 registers.
- Clocks VP_CLK and VP_PCLK can have the same frequency.
- The number of bits to be captured on the video port (the width of the data bus) is defined in the DSI_CTRL[7:6] VP_DATA_BUS_WIDTH bit field.
- For the 18-bit pixel format using 24 bits on the DSI link, the format to be used by the DSI protocol engine is 24-bit, because the DISPC must convert the 18-bit pixels into 24-bit pixels. There is no logic inside the DSI protocol engine to convert from 18-bit format to 24-bit format.

The data received on the video port can be stored in the line buffer memories or sent directly on the DSI interface in two cases:

- The line buffer size is too small compared to the line from the DISPC.
- There is no line buffer instantiated. If there is no line buffer, the burst mode, defined as frequency burst mode, cannot be used. Only transparency burst mode is supported.

NOTE: The DSI_CTRL[13:12] LINE_BUFFER and DSI_CTRL2[13:12] LINE_BUFFER bit fields define the number of lines to be used for transferring data from the video port to the DSI1_A and DSI1_C links.

10.3.4.4.5.1 DSI Video Port Used for Video Mode

If the video port is used for video mode, VP_STALL is not used. Table 10-534 and Table 10-535 list the active signals on the video port.

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Table 10-534. DSI Video Port 1 for DSI1_A and DSI1_C in the Context of Video Mode

Signal Name	Type[1]	Description
VP1_HSYNC	I	Horizontal synchronization signal
VP1_VSYNC	I	Vertical synchronization signal
VP1_DATA[23:0]	I	Parallel output data: Bits [23:0]
VP1_PCLK	I	Pixel clock
VP1_DE	I	Data enable
VP1_CLK	I	A free-running clock used as the DISPC functional clock

(1) I = Input; O = Output

Table 10-535. DSI Video Port 2 for DSI1_A and DSI1_C in the Context of Video Mode

Signal Name	Type[1]	Description
VP2_HSYNC	I	Horizontal synchronization signal
VP2_VSYNC	I	Vertical synchronization signal
VP2_DATA[23:0]	I	Parallel output data: Bits [23:0]
VP2_PCLK	I	Pixel clock
VP2_DE	I	Data enable
VP2_CLK	I	A free-running clock used as the DISPC functional clock

(1) I = Input; O = Output

Three video modes are available:

- No-line buffer: The data received on the video port are directly output to the DSI port without buffering. The ratio of VP_PCLK and the DSI HS clock period must ensure the same throughput on the two ports (the two clocks must be generated using the same PLL; the subsystem must provide this configuration).
- One-line buffer:
  - The data can be transferred as described in the no-line buffer configuration.
  - The data are first stored in the line buffer; and then when all the data for one line are received, the DSI protocol engine sends the entire line. Software must adjust timings to let enough time for storing all line data into the line buffer before sending to DSI outputs. The synchronization packets are never stored in the line buffer.
- Two-line buffers:
  - The data can be transferred as described in the one-line buffer configuration.
  - One line is stored when the second line is output on the DSI port. This allows burst capability. While receiving the first line of the frame, no RGB packets are sent, because the line buffers are empty. To send the last line of the frame, a dummy line must be provided by the display controller to flush the line buffers. The synchronization packets are never stored in the line buffer.

NOTE: If more active lines are received on the video port than the number of lines defined in the DSI_VM_TIMING3[15:0] VACT bit field, the extra lines are discarded by the DSI protocol engine. These lines are treated as blanking lines.

Figure 10-127 through Figure 10-129 show these three video modes.

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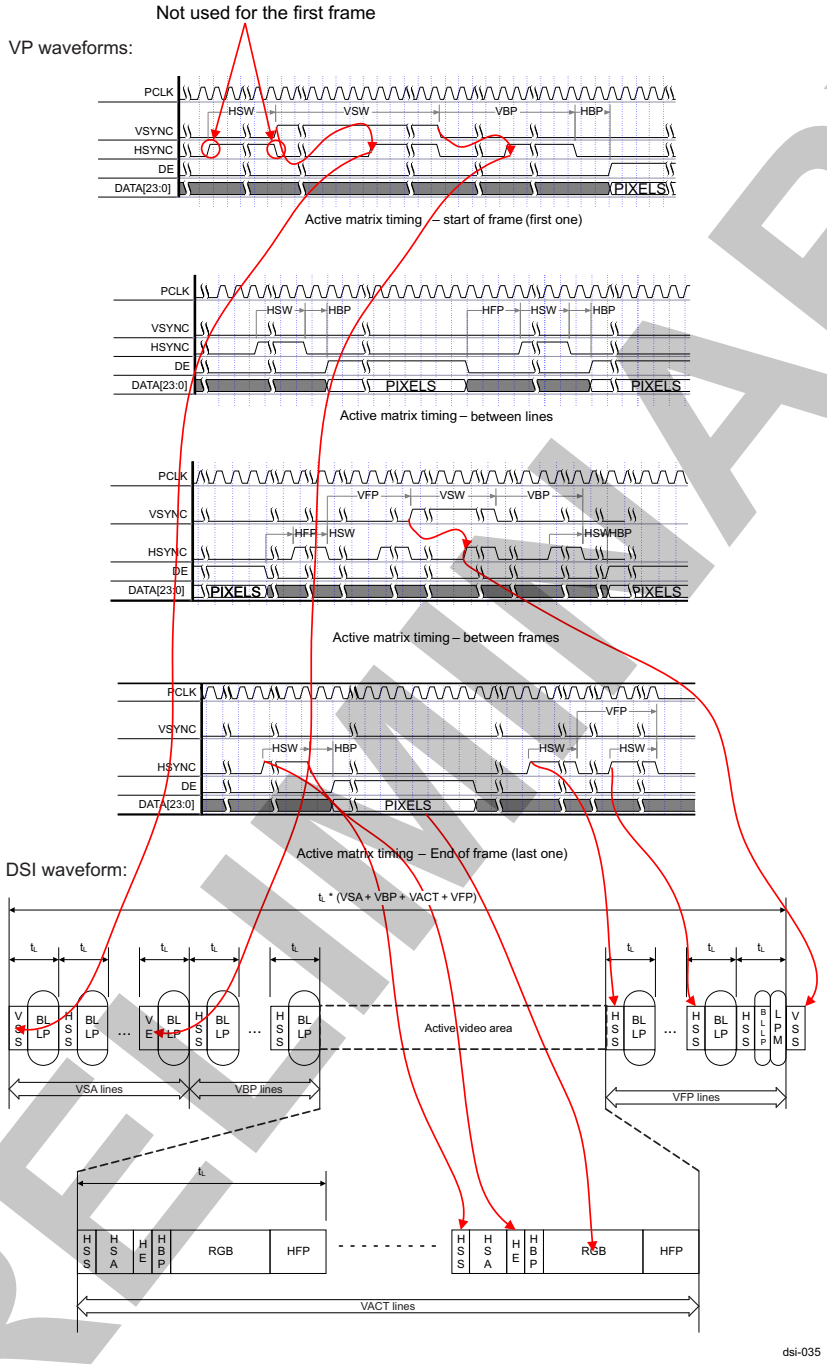
Figure 10-127. DSI Video Mode Without Burst (No-Line Buffer)



Legend:

- VSS – DSI Sync Event Packet: V sync start
- VSE – DSI Sync Event Packet: V Sync End
- BL LP – DSI Packet : Arbitrary sequence of nonrestricted DSI packets or low-power mode including optional BTA
- HSS – DSI Sync Event Packet: H sync start
- HSA – DSI Blanking Packet: Horizontal sync active or low-power mode, no data
- HSE – DSI Sync Event Packet: H sync end
- HFP – DSI Blanking Packet: Horizontal front porch or low-power mode
- HBP – DSI Blanking Packet: Horizontal back porch or low-power mode
- RGB – DSI Packet: Arbitrary sequence of pixel stream and null packets
- LPM – Low-power mode including optional BTA

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Figure 10-128. DSI Video Mode Without Burst (One-Line Buffer)

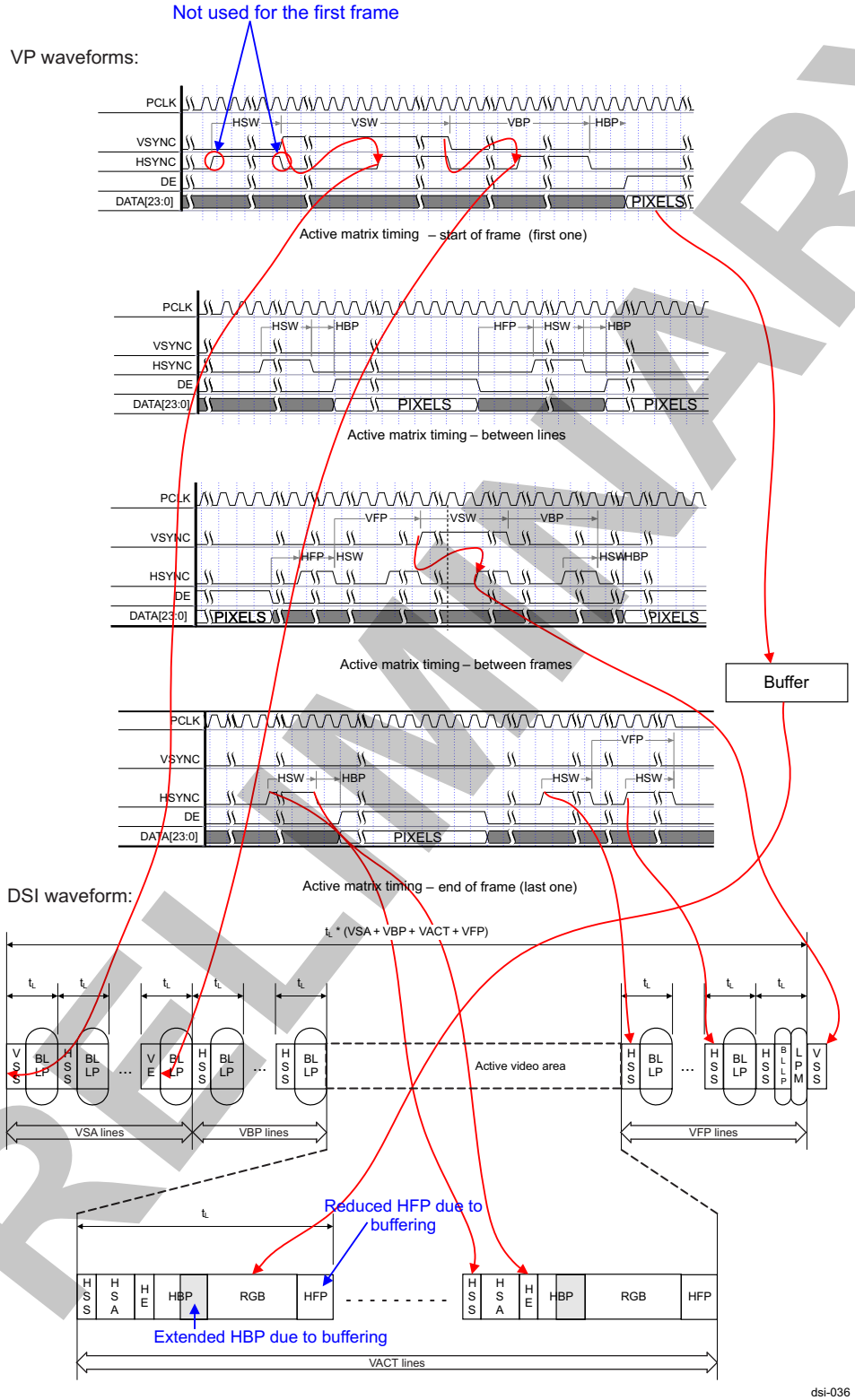

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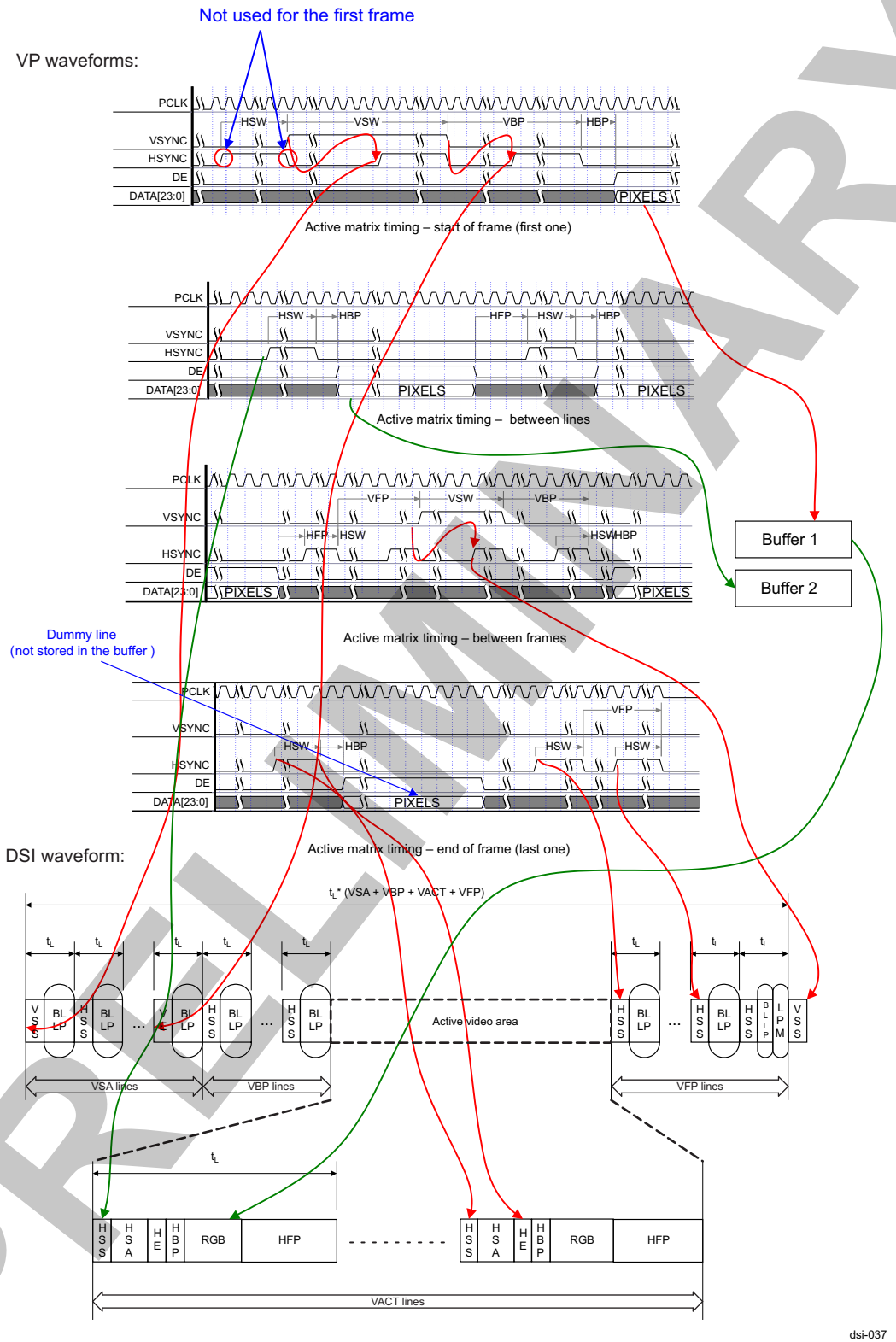
Figure 10-129. DSI Video Mode With Burst (Two-Line Buffers)



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NOTE: In Figure 10-127 through Figure 10-129:

- When HSYNC start and HSYNC end short packets are not generated (HSA does not exist), the HBP signal must not be 0.
- Software must ensure that VBP is always defined so that there is at least one HSYNC during VBP.
- In blanking low-power mode (BL-LP), two options are possible:
  - The lane remains in ULPS, and the DSI_CTRL[20] BLANKING_MODE bit is set to 0x0.
  - Dummy bytes are sent during LP with the DSI_CTRL[20] BLANKING_MODE bit set to 0x1; the number of sent bytes is determined by the DSI_VM_TIMING6[15:0] BL_LP_INTERLEAVING bit field.

In DSI video mode, if the VSA bit field in DSI_VM_TIMING2 is set to 0x0, no vertical synchronization packet will be sent, even if VP_VSYNC_START is set to 0x1 in DSI_CTRL.

If the VP_DE signal is not asserted during enough VP_PCLK cycles to be able to capture the number of bytes defined in the word count of the header, the module must send the valid data received on the video port followed by bytes of 0s to match the required number of bytes to transmit. The VP_PCLK must be present during all extra cycles where the DSI protocol engine is expecting pixels.

If the VP_DE signal is asserted for too many VP_PCLK cycles, the module stops capturing the data on the video port while the number of bytes to capture, as defined in the word count field of the header, is reached.

The HS checks that the received synchronization events on the video port (VSYNC and HSYNC) are within the synchronization window based on expected timings. If the timings (internal and received) are out of sync, the interrupt for out-of-sync is generated and the interface is disabled (the DSI_CTRL[0] IF_EN bit is automatically reset by hardware). The unsynchronization window is defined by the DSI_VM_TIMING2[27:24] WINDOW_SYNC bit field.

10.3.4.4.5.2 DSI Video Port Used for Command Mode

If the video port is used for command mode, the VP_HSYNC, VP_VSYNC, and VP_DE signals are not used. Table 10-536 and Table 10-537 describe the active signals on video port 1 and video port 2, respectively.

Table 10-536. DSI Video Port 1 for DSI1_A and DSI1_C in the Context of Command Mode

Signal Name	Type(1)	Description
VP1_DATA[23:0]	I	Parallel output data: Bits [23:0]
VP1_PCLK	I	One pulse is generated every time new data is output on the data bus.
VP1_STALL	O	The STALL signal must be deasserted to receive pixel and asserted to stop receiving pixel. (It can be used only while the DISPC is configured in stall mode; in that mode, HSYNC and VSYNC are not generated.)
VP1_CLK	I	DISPC internal clock. A free-running clock used as the DISPC functional clock.

(1) I = Input; O = Output

Table 10-537. DSI Video Port 2 for DSI1_A and DSI1_C in the Context of Command Mode

Signal Name	Type(1)	Description
VP2_DATA[23:0]	I	Parallel output data: Bits [23:0]
VP2_PCLK	I	One pulse is generated every time new data is output on the data bus.
VP2_STALL	O	The STALL signal must be deasserted to receive pixel and asserted to stop receiving pixel. (It can be used only while the DISPC is configured in stall mode; in that mode, HSYNC and VSYNC are not generated.)
VP2_CLK	I	DISPC internal clock. A free running-clock used as the DISPC functional clock.

(1) I = Input; O = Output

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NOTE: The STALL signal must be deasserted to receive pixels and asserted to stop receiving pixels.

Figure 10-130 and Figure 10-131 show the VP_STALL signal assertion and deassertion on rising and falling edges, respectively.

Figure 10-130. DSI Stall Timing With Pixel on Rising Edge

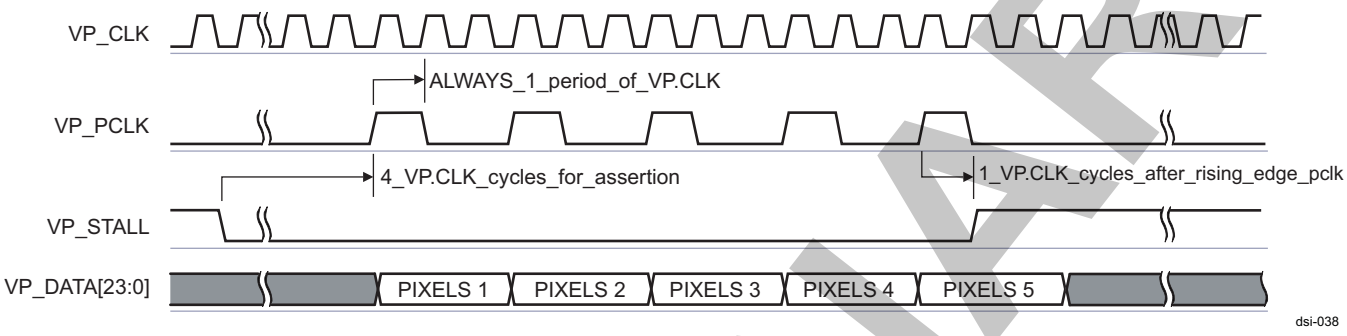
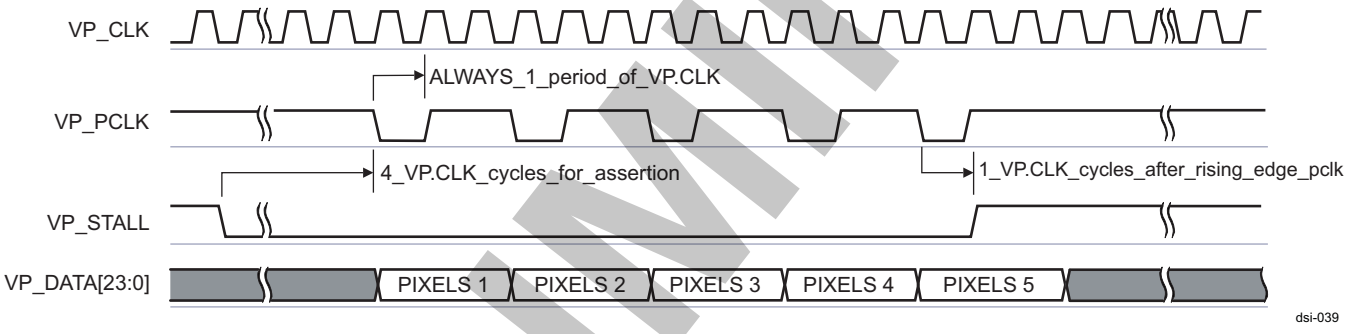


Figure 10-131. DSI Stall Timing With Pixel on Falling Edge



The VP_STALL signal is asserted to stop the transfer when the last data is output. The data can be output on the rising or falling edge of the VP_PCLK through registers in the DISPC. Data output on the falling edge of VP_PCLK is supported by the DSI protocol engine.

The VP_PCLK clock is generated from VP_CLK; these two clocks are balanced. Assertion and deassertion of VP_PCLK is done on the rising edge of VP_CLK. The width of the VP_PCLK pulse depends on the configuration of the clock divisor in the DISPC. For more information, see DISPC Overview, in *Display Controller*. In the DSI protocol engine, the information is defined in the DSI_CTRL[4] VP_CLK_RATIO bit and must be aligned with the DISPC configuration.

Deassertion of the VP_STALL signal occurs at least four VP_CLK cycles before assertion of VP_PCLK. Assertion of VP_STALL occurs one cycle VP_CLK after deassertion of VP_PCLK for the last pixel to be transferred. The VP_CLK clock is generated by the DISPC under software control. It can be kept running between assertion and deassertion of VP_STALL.

The stall assertion/deassertion depends on the number of bytes to be received considering the size of the video port bus defined in the DSI_CTRL[7:6] VP_DATA_BUS_WIDTH bit field for video port 1 and the DSI_CTRL2[7:6] VP_DATA_BUS_WIDTH bit field for video port 2.

Figure 10-132 shows the data flow in command mode using the video port.

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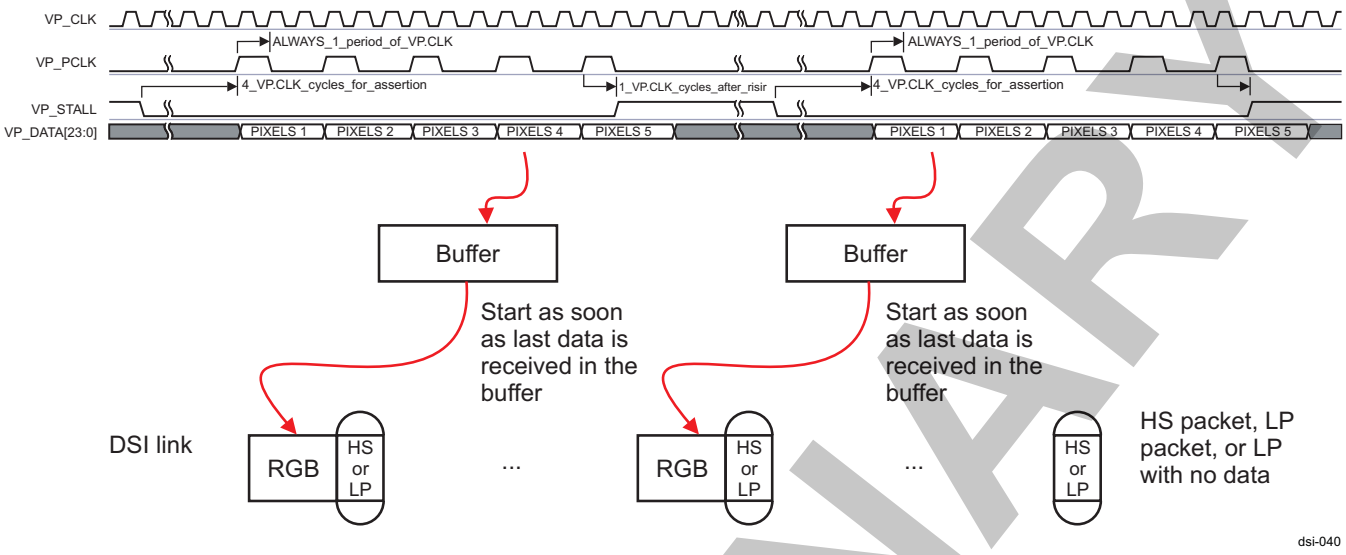
Figure 10-132. DSI Data Flow in Command Mode Using the Video Port



Two command modes are available:

- One-line buffer: The data are stored in the line buffer before being sent.
- Two-line buffers: The two lines are used if the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register is bigger than the line size; otherwise, one-line buffer must be used.

NOTE: In command mode, the video port can be used only in one- or two-line buffer configuration. No-line buffer configuration is not allowed.

The packets can be sent using high speed or low speed.

The DCS command in the payload can be inserted automatically using the DSI_VC_CTRL_i[30] DCS_CMD_ENABLE bit. If TE is used, hardware automatically inserts the DCS Write Start command for the first packet of the frame transfer and th DCS Write Continue command for all subsequent packets. The DSI_VC_CTRL_i[31] DCS_CMD_CODE bit is ignored.

10.3.4.4.5.3 DSI Burst Mode

When burst mode is enabled, the video port receives data from the DISPC at the pixel clock. The DSI protocol engine buffers the data in its own line FIFO (double-line buffer size). The read speed of the line can be twice the pixel clock to increase the blanking time of the video mode and to allow command mode traffic to be interleaved during the blanking period. Burst mode uses a dual-line buffer.

The DSI port can output data from one line buffer while the second line buffer is accessed by the video port. The two processes are concurrent but they do not access the same line at the same time. The DSI transfer can start only when the entire video port line is transferred into a line buffer. The switch is controlled by the VP_HS signal on the video port side and by an internal signal on the DSI port indicating that the last data for the current line has been written into the line buffer.

NOTE: The line buffers are used to store only the pixels. The synchronization codes are not stored in the line buffers; they must be sent according to the video port timings.

NOTE: The number of line buffers to be used while receiving data on the video port can be selected by setting the DSI_CTRL[13:12] LINE_BUFFER bit field.

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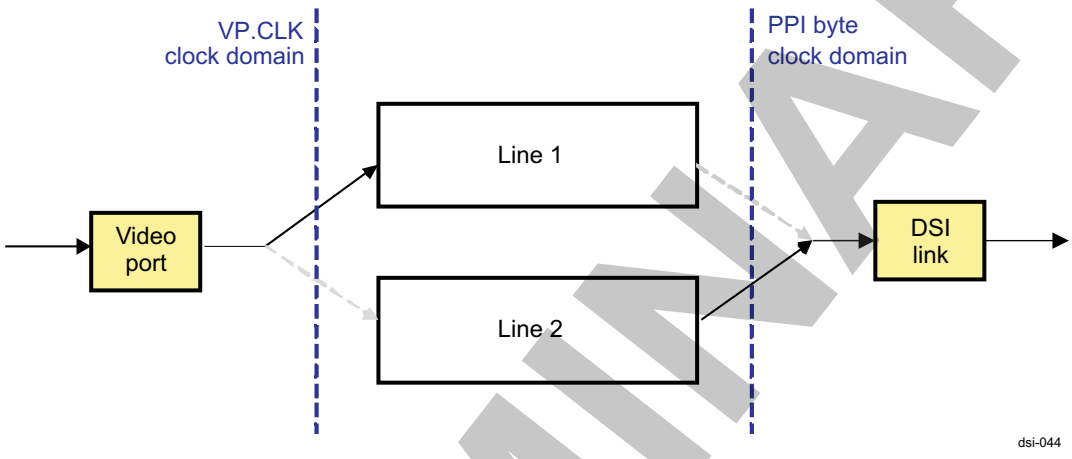
10.3.4.4.5.4 DSI Ping-Pong Buffer

The ping-pong buffer stores data incoming from the DISPC in one of the two line buffers. When one line buffer is used to store the pixels received on the video port, the other line buffer is used to provide data on the DSI link. The ping-pong buffer is supported in command mode, provided the size of the packet defined in the header register is less than the size of each line buffer (768 × 32 bits for VP2 of DSI1_A and DSI1_C, and 960 × 32 bits for VP1 of DSI1_A and DSI1_C). If the size of the packet is greater than the size of the line buffer, the ping-pong mechanism cannot be used (both lines are used as a single line).

Figure 10-133 shows the video port used in ping-pong mode .

Figure 10-133. DSI Ping-Pong Mode



The ping-pong buffer status can be checked by the DSI_VC_CTRL_i[14] PP_BUSY bit.

- When PP_BUSY equals 1, the ping-pong buffer is active and the line buffers are not ready to receive data; therefore, a new header cannot be updated.
- When PP_BUSY equals 0, at least one line buffer is empty; therefore, a new header can be updated. PP_BUSY is then set to 0x1. If both line buffers are empty, two headers can be written, one following the other. PP_BUSY remains at 0x0 after the first header is written, and is set to 0x1 after the second header is written.

An IRQ is available to update header on events. The IRQ is enabled by setting the DSI_VC_IRQENABLE_i[8] PP_BUSY_CHANGE_IRQ bit to 0x1, and its status is accessible on the DSI_VC_IRQSTATUS_i[8] PP_BUSY_CHANGE_IRQ bit.

10.3.4.4.6 DSI SCP Interface

The SCP interface is used to transfer register values from the DSI protocol engine to the DSI PLL control module and to the DSI PHY. It spends several cycles to serialize the data to be sent. Software users must consider the delay in processing the transfer of the data from/to the L3_MAIN interconnect slave port to/from the module.

10.3.4.4.6.1 DSI Shadowing Register

The first three SCP registers for the DSI PHY address map must be implemented as shadow registers. The shadowing mechanism is enabled and disabled using the DSI_COMPLEXIO_CFG1[31] SHADOWING bit:

- When setting the DSI_COMPLEXIO_CFG1[31] SHADOWING bit to 1, the transfer of the values from the three first local interconnect port registers into the first three registers of the DSI PHY (DSI_PHY_REGISTER0 through DSI_PHY_REGISTER2) is done only when the DISPC_UPDATE_SYNC signal from the DISPC is active and the DSI_COMPLEXIO_CFG1[30] GOBIT bit is set to 1. If there is no pending update for the three registers when the DISPC_UPDATE_SYNC signal is asserted, the DSI_COMPLEXIO_CFG1[30] GOBIT bit is reset by hardware and there is no SCP transfer.
  - If only one register needs to be updated, only the corresponding new value is transferred. The

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second and third registers in the DSI PHY are not updated. When the transfer completes, the DSI_COMPLEXIO_CFG1[30] GOBIT bit is reset by hardware.

– If two registers need to be updated, the register with the lower address is transferred first, followed by the second register. When the transfers complete, the DSI_COMPLEXIO_CFG1[30] GOBIT bit is reset by hardware.

– If three registers need to be updated, the register with the lowest address is transferred first, and then the other registers are transferred according to incremental address. When the transfers complete, the GOBIT bit is reset by hardware.

When there is an ongoing transfer (read or write) to any SCP register, the transfer must complete before updating the shadowing registers.

- When setting the DSI_COMPLEXIO_CFG1[31] SHADOWING bit to 0, if the transfer into the first two DSI PHY registers has already started, it should be finished.

NOTE: When reading the shadow registers, the local value stored in the DSI protocol engine is returned if the update is pending; otherwise, the values stored in the DSI PHY are returned.

10.3.4.4.6.2 DSI Busy Signal

The SCPBusy signal indicates there is still activity using the SCPClk clock provided by the PRCM module. The SCPClk clock is then divided by the DSS_L3_MAIN_ICLK/4 clock.

10.3.4.4.7 DSI Timers

NOTE: Among the timers described in this section, only the HS TX, LP RX, and TurnRequests timers generate interrupts immediately when the timer value is null. The ForceTxStopMode timer ends counting instantly and ForceTxStopMode is not asserted.

10.3.4.4.7.1 DSI T_{wakeup} Timer

The T_{WakeUp} timer is not implemented in the DSI protocol engine. The general-purpose (GP) timer must be used to handle wakeup. This timer is used for exiting ULPS for the active lanes (clock and/or data lanes). The sequence to exit ULPS is:

1. Change the state of TxULPSExit for each lane to ACTIVE.
2. Wait for the interrupt that indicates all lanes with TxULPSExit ACTIVE have acknowledged by asserting ULPSActiveNot. This is done by reading the ULPSACTIVENOT_ALLi_IRQ bit field (where i = 0 or 1) in the DSI_COMPLEXIO_IRQSTATUS register.
3. Start the application wake-up timer (GP timer).
4. Wait for the time-out.
5. Change the TxUlpsClk signals to INACTIVE state for the clock lane and/or TxRequestEsc INACTIVE state for the data lane(s).

NOTE: The minimum time for the wake-up period is 1 ms.

To enter ULPS for the clock lane, the state of TxUlpsClk must be changed to ACTIVE. To enter ULPS for the data lane, the state of TxRequestEsc must be changed to ACTIVE (also TxUlpsEsc, if it is not already in ACTIVE state).

10.3.4.4.7.2 DSI ForceTxStopMode FSM

The ForceTxStopMode signal is used at initialization time (DSI PHY). Figure 10-134 shows the ForceTxStopMode finite state-machine (FSM) to assert and deassert the ForceTxStopMode signal.

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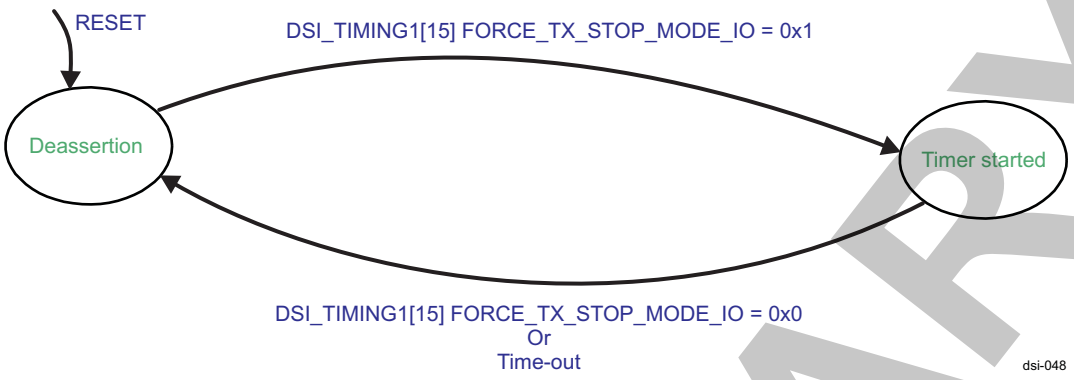
Figure 10-134. DSI ForceTxStopMode FSM



The DSI protocol engine asserts the ForceTxStopMode signal by setting the DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO bit to 1. Asserting the FORCE_TX_STOP_MODE_IO bit allows the lanes to be initialized. The lanes are in STOP state when the ForceTxStopMode signal is high.

No data can be sent before the ForceTxStopMode signal is deasserted. The deassertion time is defined by the STOP_STATE_COUNTER_IO, STOP_STATE_X4_IO, and STOP_STATE_X16_IO bit fields in DSI_TIMING1[14:0] register. The DSI_TIMING1[15:0] FORCE_TX_STOP_MODE_IO bit field is reset by hardware when the time is reached.

This bit can be reset by software.

The calculation of the number of DSI_CLK functional clock cycles assertion period is defined by:

Total period in DSI_FCLK cycles = STOP_STATE_COUNTER_IO × ((STOP_STATE_X16_IO x 15) + 1) × ((STOP_STATE_X4_IO × 3))

10.3.4.4.7.3 DSI TurnRequest FSM

The TurnRequest signal is used to request a turnaround. It is valid only for the first data lane, because the other data lanes cannot be used in reverse direction to receive data from the DSI receiver. When the TurnRequest signal is asserted, the TA_TO timer is started. Figure 10-135 shows the TurnRequest FSM to assert and deassert the TurnRequest signal.

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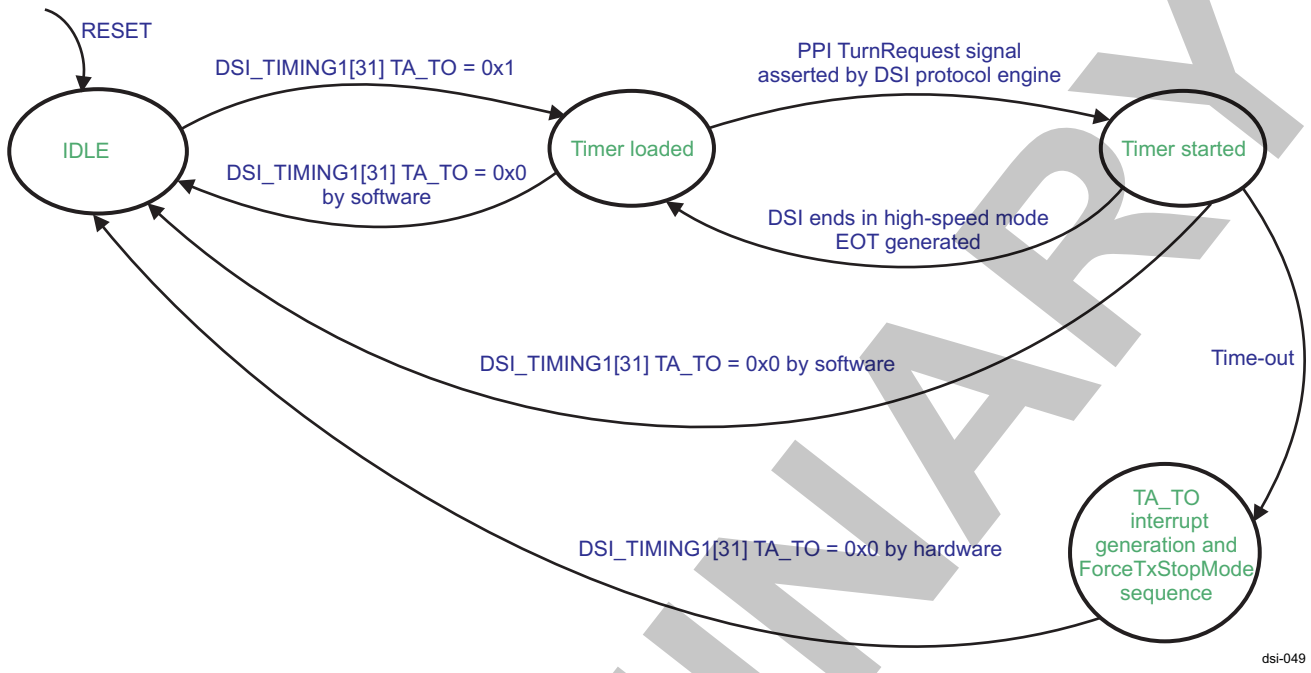
Figure 10-135. DSI TurnRequest FSM



The DSI protocol engine asserts the TurnRequest signal during one TxClkEsc cycle when turnaround is enabled through the DSI_VC_CTRL_i[6] BTA_EN bit (for more information, see Section 10.3.4.4.8, *Bus Turnaround*). The DSI_TIMING1[31] TA_TO bit is set/reset by software to enable or disable the timer for turnaround procedure failure. It can be reset by software or automatically by hardware when the time-out occurs.

The timer is loaded with the value in the number of DSI_FCLK cycles:

DSI_TIMING1[28:16] TA_TO_COUNTER × ((DSI_TIMING1[30] TA_TO_X16 × 15) + 1) × ((DSI_TIMING1[29] TA_TO_X8 × 7) + 1)

When the TA_TO_IRQ interrupt is generated (the turnaround timer expired and the procedure failed), hardware automatically resets the DSI_TIMING1[31] TA_TO bit and asserts the ForceTXStopMode signal (see Section 10.3.4.4.7.2, *ForceTxStopMode FSM*) for the DSI_PHY_DSS_x to drive the LP-11 STOP state. The ForceTXStopMode timer is used to define the minimum duration of the LP-11 state. The STOP state can be longer if there is no activity.

Hardware resets the DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO bit, followed by an internal logic reset except for all register values and TX FIFO content, and then resets the DSI_CTRL[0] IF_EN bit. Software must take action to recover (for example, by resetting the peripheral if it is not responding). It must wait for the DSI_CTRL[0] IF_EN bit to be reset to 0 before starting the recovery sequence.

10.3.4.4.7.4 DSI Peripheral Reset Timer

The peripheral reset timer is not implemented in the DSI protocol engine module. Instead, a GP timer must be used in case of reset of the peripheral to determine when the peripheral is ready to operate again.

10.3.4.4.7.5 DSI HS TX Timer

The HS TX timer is used to detect when the host is in TX mode too long. When time-out occurs, the EOT is forced. The timer is reloaded when a start of HS transmission occurs. It is enabled and disabled by software through the DSI_TIMING2[31] HS_TX_TO bit. The HS_TX_TO_IRQ interrupt is generated when the timer expires. The DSI_IRQSTATUS[14] HS_TX_TO_IRQ bit is set to 1 when the HS TX time-out occurs.

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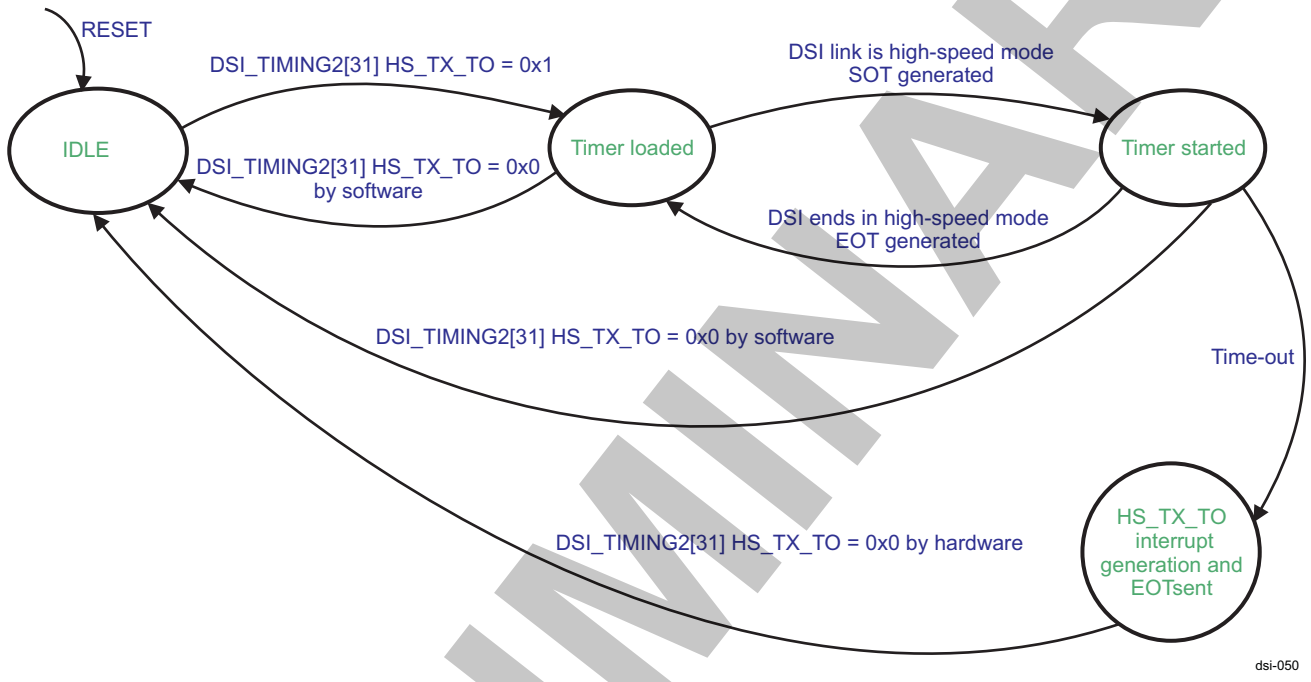
The maximum time supported is 20 ms. It can be used to determine that at least once per frame in video mode, the HS mode is stopped to enter ULPS.

The timer is loaded with the value in the number of TXBYTECLKHS:

DSI_TIMING2[28:16] HS_TX_TO_COUNTER × (1 + (DSI_TIMING2[30] HS_TX_TO_X64 × 63)) × (1 + (DSI_TIMING2[29] HS_TX_TO_X16 × 15))

Figure 10-136 shows the HS TX timer FSM.

Figure 10-136. DSI HS TX Timer FSM



When the time-out occurs, hardware sends an EOT request for the DSI PHY to drive LP-11 STOP state. This is followed by the generation of the interrupt. Hardware performs an internal logic reset including the TX FIFO content but excluding the register values, and then resets the DSI_CTRL[0] IF_EN bit.

Software must take action to recover (for example, by resetting the peripheral if it is not responding). It must wait for the DSI_CTRL[0] IF_EN bit to be reset to 0 before taking any recovery action.

10.3.4.4.7.6 DSI LP RX Timer

When the host is in low-power receive mode after a BTA, the LP RX timer is loaded. When the timer expires, the host requests the DSI PHY to drive LP-11. The LP_RX_TO_IRQ interrupt is generated when the timer expires. The DSI_IRQSTATUS[15] LP_RX_TO_IRQ bit is set to 1 when the LP RX time-out occurs.

The DSI_TIMING2[15] LP_RX_TO bit is set and reset by software to enable or disable the timer.

The timer is loaded with the value in the number of DSI_CLK functional clock cycles:

DSI_TIMING2[12:0] LP_RX_TO_COUNTER × ((DSI_TIMING2[14] LP_RX_TO_X16 × 15) + 1) × ((DSI_TIMING2[13] LP_RX_TO_X4 × 3) + 1)

Figure 10-137 shows the LP RX timer FSM.

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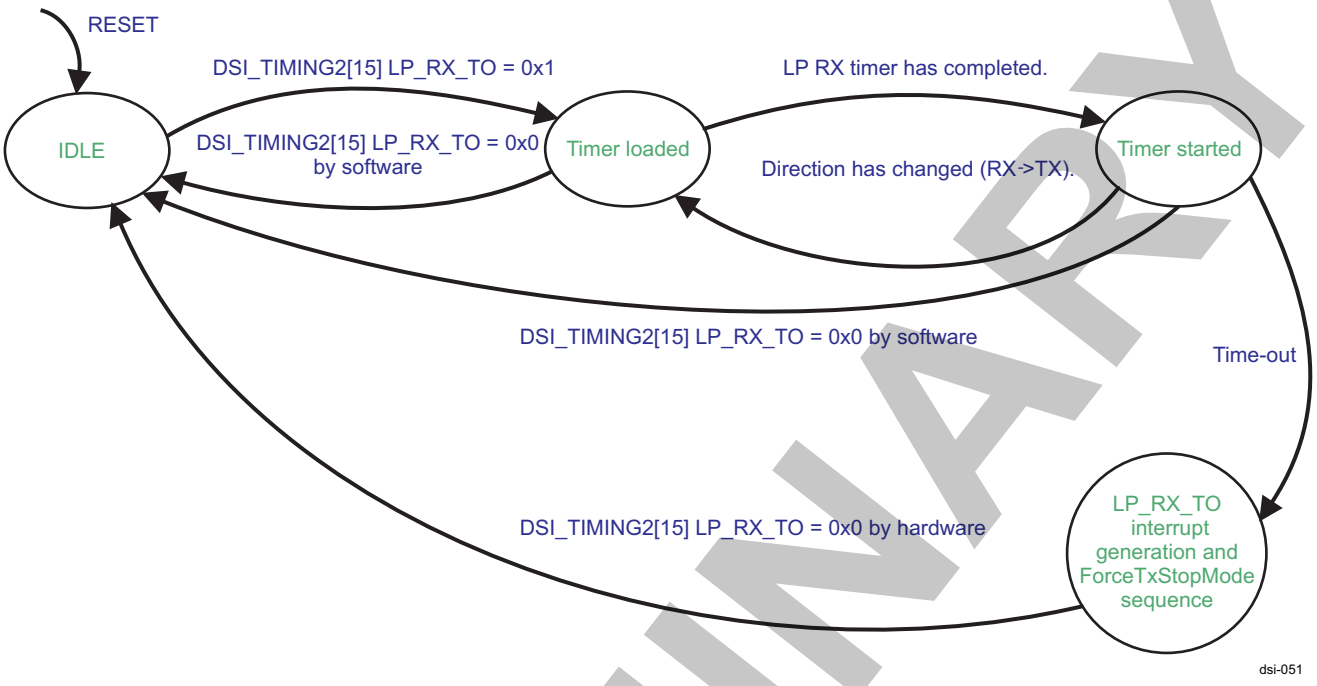
Figure 10-137. DSI LP RX Timer FSM



When the interrupt is generated, hardware automatically resets the DSI_TIMING2[15] LP_RX_TO bit and then asserts ForceTXStopMode for the DSI PHY to drive LP-11 STOP state. The ForceTXStopMode timer is used to define the minimum duration of the LP-11 state. The STOP state can be longer if there is no activity.

Hardware resets the FORCE_TX_STOP_MODE bit, followed by an internal logic reset except for all register values and TX FIFO content, and then resets the DSI_CTRL[0] IF_EN bit. Software must take action to recover (for example, by resetting the peripheral if it is not responding). It must wait for the DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO and DSI_CTRL[0] IF_EN bits to be reset before starting the recovery sequence. The TX FIFO is not flushed (the FIFO is flushed only when the DSI_VC_CTRL_i[0] VC_EN is set to 1).

10.3.4.4.8 DSI Bus Turnaround

The BTA is not automatically sent by default after each packet is sent to the panel(s). It is programmable independently for each VC ID. BTA generation can be enabled when the DSI_VC_CTRL_i[6] BTA_EN bit is set to 1 by software. Software must ensure that when the BTA is sent to the peripheral, enough time is allocated for the response and for the BTA from the peripheral to the host. For more information about possible DSI PHY timing adjustments during the turnaround procedure, see Section 10.3.4.6.5.3, *Turnaround Request in Transmit Mode*, and Section 10.3.4.6.5.4, *Turnaround Request in Receive Mode*.

When setting the DSI_VC_CTRL_i[6] BTA_EN bit to 1, one BTA is sent manually to the peripheral. This manual mode can be used for packets in command or video mode.

Acknowledgment from the peripheral for successful BTA is indicated by asserting the BTA_IRQ interrupt, if it is enabled in the DSI_VC_IRQENABLE_i[5] BTA_IRQ_EN bit. To monitor the BTA interrupt, the user must read the DSI_VC_IRQSTATUS_i[5] BTA_IRQ status bit.

CAUTION

The BTA should be sent when the RX FIFO is empty. Users must empty the RX FIFO before sending the BTA to the peripheral to ensure that when receiving new data from the peripheral, the allocated spaces for all the VCs are empty.

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In automatic mode, the BTA is sent automatically at the end of short or long packet transmission, if the DSI_VC_CTRL_i[2] BTA_SHORT_EN or DSI_VC_CTRL_i[3] BTA_LONG_EN bit is set to 1.

Two modes can be used for each VC ID:

- Automatic: After each packet, a BTA is sent. To determine the size of the long packet, the protocol engine on the host side reads the word count defined in the header (in the DSI_VC_LONG_PACKET_HEADER_i register) and uses it to determine the last data to be sent on the DSI link. For short packets, the size is always 4 bytes. The BTA is then sent to the peripheral. The word count is also used to determine how many bytes are to be transferred from the 32-bit write access to the payload register (DSI_VC_LONG_PACKET_PAYLOAD_i).
- Manual:
  - Data transfer through L3_MAIN interconnect: When transferring data using the L3_MAIN interconnect port, while all data have been provided to the DSI protocol engine, users can select the BTA for the last packet provided to the L3_MAIN interconnect port only by setting the DSI_VC_CTRL_i[6] BTA_EN bit, or for the last packets and the following ones by setting automatic mode.
  - Data transfer through video port: In the case of data transfer using the video port, the DSI_VC_CTRL_i[6] BTA_EN bit can be selected at any time during the transfer of the packet.
- For video mode packets (data and synchronization events), it is not possible to determine when the BTA is sent; therefore, it is highly recommended to use manual BTA mode only in command mode. It is possible, however, to use the BTA for a VC in video mode.

  For data provided on the video port, an interrupt for end of packet transfer PACKET_SENT_IRQ is provided to indicate when the packet is completely sent by the DSI PHY. PACKET_SENT_IRQ can be monitored in the DSI_VC_IRQSTATUS_i[2] PACKET_SENT_IRQ status bit. The BTA is available even if the space allocated in the TX FIFO for the corresponding VC is empty. It must be sent later even if no packet was sent before the BTA request. The DSI_VC_CTRL_i[6] BTA_EN bit must be reset if the BTA request was sent, even if automatic mode for this specific type of packets is enabled.

The BTA is supported for video and command mode packets. It is not possible to send the BTA during the blanking periods of video mode when HS blanking packets should be sent; that is, when one of the following bits is set to 1:

- DSI_CTRL[20] BLANKING_MODE
- DSI_CTRL[21] HFP_BLANKING_MODE
- DSI_CTRL[22] HBP_BLANKING_MODE
- DSI_CTRL[23] HSA_BLANKING_MODE

Therefore, in video mode, the BTA request is delayed until there is a blanking period without HS blanking packets.

When the TurnRequest signal is asserted (always only for the first data lane), the TA_TO timer is started. If the direction signal is not changed according to the turnaround request, the TA_TO interrupt is generated. When the direction signal is in output mode, any data on the input data bus is ignored because the DSI is in transmission mode (data and triggers must be ignored). For more information about the TA_TO timer, see Section 10.3.4.4.7.3, *TurnRequest FSM*.

10.3.4.4.9 DSI PHY Triggers

The DSI protocol engine uses three triggers that are supported only for the first data lane:

- Reset trigger from host to display
- TE trigger from display to host
- Acknowledge trigger from display to host

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CAUTION

Each trigger is associated with a dedicated user-configurable receive or transmit pattern, which is loaded in the DSI_PHY_REGISTER3 or DSI_PHY_REGISTER4 register. The default (reset) values of the bit fields are aligned with the *MIPI D-PHY Specification v1.01.00 Revision 0.02*. If any of these values need to be changed, the following must be considered:

- If any of the bit fields is written with a nondefault value, the other bit fields in the same register must also be configured with different values. This ensures that two different trigger bit fields are not programmed with the same pattern.
- If two or more bit fields are written with equal values, unpredictable behavior of the DSI PHY module may occur.

10.3.4.4.9.1 DSI Reset

The DSI protocol engine can use one of the triggers of the DSI_PHY_DSS_x to send a reset to the display. The reset trigger pattern is configurable through the DSI_PHY_REGISTER3[31:24] REG_TXTRIGGERESC3 bit field. To send the reset pattern to the peripheral, the DSI_CTRL[5] TRIGGER_RESET bit must be set to 1. When software requires the trigger reset pattern to be sent, the DSI protocol engine resets its own logic, but not the registers. Software can select between two reset modes:

- Immediate reset: All pending requests in TX FIFO not already considered for transfer scheduling, the RX FIFO requests, and the data from video port are ignored. Only the current transfer on the DSI link and those already scheduled are transmitted. All the other transfers are discarded.
- Synchronized reset: The mode is valid only if a VC is using the video mode and it is active. The principle is to wait for the current video frame to be transferred on the link. Any data on the video port after the current frame are ignored.

To select reset mode, the DSI_CTRL[14] TRIGGER_RESET_MODE bit must be programmed.

NOTE: For both reset modes, the DSI protocol engine flushes the FIFOs, synchronization buffers, and line buffers before resetting the DSI_CTRL[0] IF_EN bit.

10.3.4.4.9.2 DSI Tearing Effect

TE on the display is avoided by having synchronization information from the display. It is used only in command mode and is not functional in video mode.

The two types of TE triggers are:

- DSI PHY TE trigger
- CMOS TE line (one of the two input signals can be selected for the TE trigger of a VC; the signal is asynchronous)

Software must set and send the appropriate sequence to receive the TE trigger pattern from the peripheral on the DSI link, or use the CMOS TE line. The value of the expected TE trigger pattern can be configured through the DSI_PHY_REGISTER4[23:16] REG_RXTRIGGERESC2 bit field.

When the TE PHY trigger pattern is received, the DSI protocol engine generates the TE_TRIGGER_IRQ interrupt with a TE event if the interrupt is enabled. To enable the interrupt, the DSI_IRQENABLE[16] TE_TRIGGER_IRQ_EN bit must be set to 1. The DSI_IRQSTATUS[16] TE_TRIGGER_IRQ status bit indicates whether the interrupt event has been generated.

When using the TE CMOS signal, the DSI protocol engine generates the TE0_LINE or TE1_LINE interrupt, if it is enabled, depending on which line is used. One or multiple VCs can be synchronized using the same TE line. Both lines can be active at the same time for different VCs.

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The DSI_VC_TE_i[30] TE_EN bit must be set and the DSI_VC_TE_i[29] TE_LINE bit must be reset to indicate that hardware must use the TE PHY trigger to start the transfer of the data from the related VC. TE_EN is reset when all the data are sent to the peripheral.

The DSI_VC_TE_i[30] TE_EN, DSI_VC_TE_i[29] TE_LINE, and DSI_VC_TE_i[28] TE_LINE_NB bits must be set to select between the TE0 and TE1 line to indicate that hardware must use the TE0 or TE1 line to start the transfer of the data from the related VC. The bits are reset when all the data are sent to the peripheral.

The DSI_TE_VSYNC_WIDTH_j, DSI_TE_HSYNC_WIDTH_j, and DSI_TE_HSYNC_NUMBER_j registers indicate which mode is used to detect the start of the transfer:

- If DSI_TE_HSYNC_NUMBER_j[10:0] LINE_NUMBER = 0, DSI_TE_HSYNC_WIDTH_j is ignored. When a pulse on the TE line is detected to be wider than the DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH bit field, data transfer starts from the protocol engine to the peripheral at the falling edge of the TE CMOS line.
- If the DSI_TE_HSYNC_NUMBER_j[10:0] LINE_NUMBER bit field is greater than 0, DSI_TE_HSYNC_WIDTH_j is used. The DSI protocol engine waits until it detects a pulse wider than the DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH bit field, and then counts each pulse wider than DSI_TE_HSYNC_WIDTH_j[19:8] MIN_HSYNC_PULSE_WIDTH, but smaller than DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH. When the number of HSYNC pulses is reached, data transfer from the DSI protocol engine to the peripheral starts. In case the number of HSYNC pulses is not reached due to a new VSYNC pulse being detected, the counter of HSYNC pulses restarts from 0.

NOTE: The DSI_TE_HSYNC_WIDTH_j[19:8] MIN_HSYNC_PULSE_WIDTH is always programmed with a value smaller than the DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH bit field.

NOTE: The following must always be set before the DSI_VC_TE_i[30] TE_EN bit is enabled:

- DSI_TE_HSYNC_WIDTH_j[19:8] MIN_HSYNC_PULSE_WIDTH
- DSI_TE_VSYNC_WIDTH_j[19:8] MIN_VSYNC_PULSE_WIDTH
- DSI_VC_TE_i[29] TE_LINE
- DSI_VC_TE_i[28] TE_LINE_NB

The DSI_VC_TE_i[31] TE_START bit must be used when automatic mode is disabled (the DSI_VC_TE_i[30] TE_EN bit is set to 0). It lets users start the transfer manually based on application events or based on the TE trigger interrupt (TE_TRIGGER_IRQ).

The number of bytes to be transferred is defined by using the DSI_VC_TE_i[23:0] TE_SIZE bit field. The TE_SIZE bit field is decremented for each payload byte (it does not include checksum) sent on the DSI link. The register content must not be modified by software during a transfer. The DSI_VC_TE_i[23:0] TE_SIZE bit field must be set first to indicate that the following accesses to the DSI_VC_LONG_PACKET_HEADER_i register must be used for TE transfer.

The data can be provided from two sources (select by setting the DSI_VC_CTRL_i[1] SOURCE bit):

- L3_MAIN interconnect slave port using DMA request: The DMA request DSI_DMA_REQi must be asserted only when the TE trigger is received or when the DSI_VC_TE_i[31] TE_START bit is set by the user and must no longer be asserted when all the bytes defined in the DSI_VC_TE_i[23:0] TE_SIZE bit field are sent on the DSI link. The VC is associated with a DMA request by programming the number in the DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB bit field. The DSI_VC_LONG_PACKET_PAYLOAD_i register is used to provide the number of bytes defined by the DSI_VC_TE_i[23:0] TE_SIZE bit field (the checksum value is not provided in the DSI_VC_LONG_PACKET_PAYLOAD_i register). The size of the header is not considered in the number of bytes to transfer. The DSI_VC_SHORT_PACKET_HEADER_i register is not used.

NOTE: All DMA requests associated to a VC must be disabled when they are not used (DSI_VC_CTRLi[23:21] DMA_TX_REQ_NB = 0x4).

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- Video port: The DMA request is not asserted. The data are captured in the line buffer using the STALL mechanism. If no line buffer is instantiated (that is, the DSI_CTRL[13:12] LINE_BUFFER bit field is set to 0), it is not possible to use the video port to provide data. The line buffer is filled according to the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register header. The value must be written before the TE trigger event is received or before the DSI_VC_TE_i[31] TE_START bit is set to 1 by software. If the total number of bytes defined by the DSI_VC_TE_i[23:0] TE_SIZE bit field is not a multiple of the word count defined in the DSI_VC_LONG_PACKET_HEADER_i register, all the packets are the same size defined by the WC of the header, except the last transfer. The size of the last transfer is defined by the remaining bytes to send. Because the DSI_VC_TE_i[23:0] TE_SIZE bit field is modified after each packet transfer, the size of the last packet is equal to the value of the DSI_VC_TE_i[23:0] TE_SIZE bit field before the last transfer (the header and the payload checksum sizes are not included in the DSI_VC_TE_i[23:0] TE_SIZE bit field).

When the transfer completes, the value of the DSI_VC_TE_i[23:0] TE_SIZE bit field is equal to 0. Software must ensure that the pending data in the TX FIFO for the corresponding VC using TE are related to the TE transfer. Any data in the TX FIFO that must be sent before the reception of the TE trigger must be sent before the TE. This is done by not enabling the TE trigger until all data for the corresponding VC are sent to the peripheral. Software can check that the space allocated for the VC in the TX FIFO is empty by reading the DSI_VC_CTRL_i[5] TX_FIFO_NOT_EMPTY status bit.

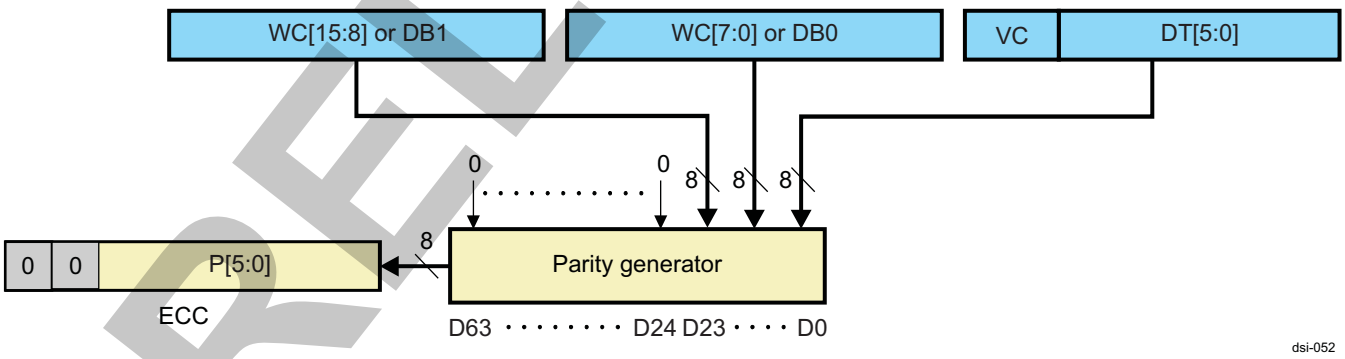
10.3.4.4.9.3 DSI Acknowledge

The corresponding acknowledge interrupt (ACK_TRIGGER_IRQ) is generated when the acknowledge trigger is received. The value of the expected acknowledge trigger pattern can be configured through the DSI_PHY_REGISTER4[15:8] REG_RXTRIGGERESC1 bit field. To enable the acknowledge interrupt, set the DSI_IRQENABLE[17] ACK_TRIGGER_IRQ_EN bit to 1. When the interrupt is generated, the DSI_IRQSTATUS[17] ACK_TRIGGER_IRQ status bit is set to 1.

10.3.4.4.10 DSI ECC Generation

The DSI protocol uses a 4-byte PH. Because ECC generation requires a fixed word length of 64-bits, the packet headers must be padded with additional bits to form a full 8-byte value for ECC generation and checking. The PH minus the ECC byte should occupy bits D[23:0], and the pad bits should occupy bits D[63:24]. All padding bits must be 0 to generate the ECC byte. ECC can be generated using a parallel approach, as shown in Figure 10-138.

Figure 10-138. DSI 64-Bit ECC Generation on TX Side



The ECC generation/check can be enabled and disabled by software. It is defined by a common bit for all the VCs:

- The DSI_CTRL[2] ECC_RX_EN bit enables and disables ECC generation in the receive direction.
- The DSI_VC_CTRL_i[8] ECC_TX_EN bit enables and disables ECC generation in the transmit direction

The ECC can be provided while writing the ECC value directly into the DSI_VC_LONG_PACKET_HEADER_i and DSI_VC_SHORT_PACKET_HEADER_i registers. The DSI_VC_CTRL_i[8] ECC_TX_EN bit indicates whether the ECC value will be calculated or whether the value written in the register will be used instead for command and video modes.

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10.3.4.4.11 DSI Checksum Generation for Long Packet Payloads

Long packets consist of a PH protected by an ECC byte and a payload of 0 to $2^{16} - 1$ bytes. To detect the errors during the transmission of long packets, a checksum is calculated over the payload portion of the data packet. For the special case of a 0-length payload, the 2-byte checksum is set to 0xFFFF. The checksum can indicate only the presence of one or more errors in the payload. Unlike ECC, the checksum does not enable error correction. For this reason, checksum calculation is not useful for some unidirectional DSI implementations, because the peripheral has no way to report errors to the host processor. Checksum generation and transmission is mandatory for host processors sending long packets to peripherals; it is optional for peripherals transmitting long packets to the host processor. However, the format of long packets is fixed; the peripherals that do not support checksum generation must transmit 2 bytes with a value of 0x0000 in place of the checksum bytes when sending long packets to the host processor. The host processor must disable checksum checking for received long packets from peripherals that do not support checksum generation.

Checksum must be realized as a 16-bit CRC with a generator polynomial of $x^{16} + x^{12} + x^5 + x^0$. The LSByte is sent first, followed by the MSByte. Within the byte, the LSB is sent first.

Figure 10-139 shows the checksum transmission.

Figure 10-139. DSI Checksum Transmission

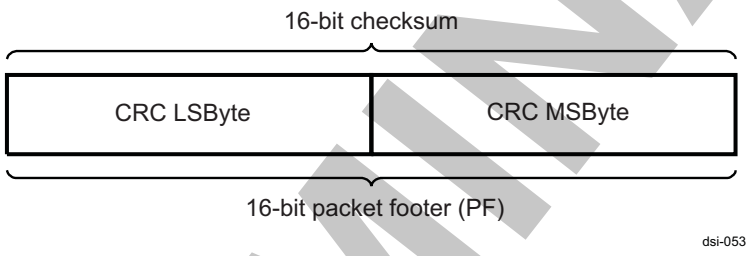
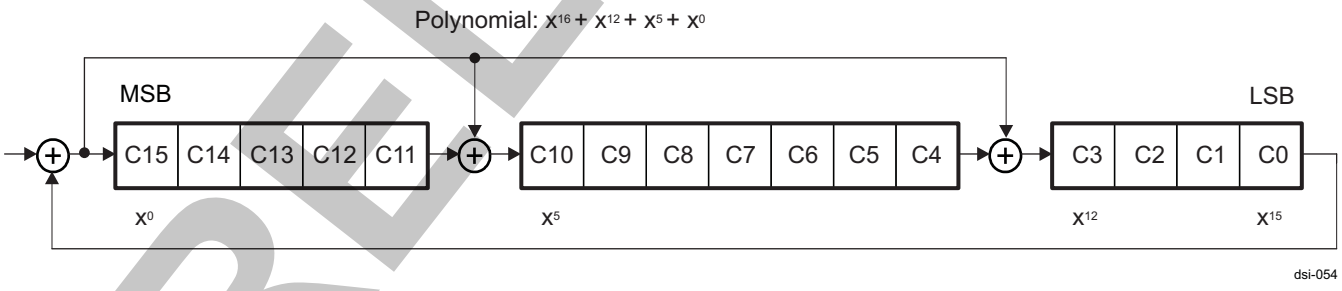


Figure 10-140 shows the CRC implementation. The CRC shift register is initialized to 0xFFFF before packet data enters. Packet data not including the PH then enters as a bitwise data stream from the left, LSB first. Each bit is fed through the CRC shift register before it is passed to the output for transmission to the peripheral. After all bytes in the packet payload have passed through the CRC shift register, the shift register contains the checksum. C15 contains the MSB of the checksum, and C0 contains the LSB of the 16-bit checksum. The checksum is then appended to the data stream and sent to the receiver.

Figure 10-140. DSI 16-Bit CRC Generation Using a Shift Register



Checksum generation/check can be enabled and disabled by software. It is defined by a common bit for all the VCs:

- The DSI_CTRL[1] CS_RX_EN bit enables and disables checksum generation in the receive direction.
- The DSI_VC_CTRL_i[7] CS_TX_EN bit enables and disables checksum generation in the transmit direction.

10.3.4.4.12 DSI EOT Packet

A new packet type allows the DSI protocol (rather than the DSI_PHY_DSS_x) at the display to detect the HS EOT. This is a fixed short packet (4 bytes) that is added at every HS-to-LP transition. This function is enabled by the DSI_CTRL[19] EOT_ENABLE bit.

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The EOT packet has a fixed format:

- Data Type = DI [5:0] = 0b001000
- Virtual Channel = DI [7:6] = 0b00
- Payload Data [15:0] = 0x0F0F
- ECC [7:0] = 0x01

When more that one data lane is used, the EOT packet bytes are distributed across the multiple lanes. EOT packet generation is supported only for the end of HS transmissions. No EOT packet is added at the end of LP transmissions. For LP reception, any EOT packet received is simply passed through as any other packet, but no internal decode or use is made of the EOT information.

10.3.4.4.13 DSI Software Reset

The DSI protocol engine can be reset by software. This reset can be done for debug purposes or after a protocol error and has the same effect as the hardware reset. The DSI protocol engine can be reset by setting the DSI_SYSCONFIG[1] SOFT_RESET bit to 1. Software can monitor the DSI_SYSSTATUS[0] RESET_DONE status bit to wait for the reset to complete. If after five reads the DSI_SYSSTATUS[0] RESET_DONE status bit still returns 0, it can be assumed that an error occurred during the reset stage.

NOTE: This software reset is optional because a hardware reset is always performed on the DSI protocol engine at device reset.

10.3.4.4.14 DSI Power Management

The power-management behavior of the DSI protocol engine is controlled by the DSI_SYSCONFIG register. This register controls the way the module interacts with the PRCM module. The DSI_SYSCONFIG[0] AUTO_IDLE bit must be set to 1 (default value) to enable automatic clock gating in the module.

The DSI protocol engine implements a handshake protocol on the L3_MAIN interconnect slave port with the PRCM module. The protocol engine provides control signal CIO_CLK_ICG to gate the SCPClk (DSS_L3_MAIN_ICLK/4). It allows the reduction of power consumption of the DSI PHY when the DSI link is not in use (the DSI_CLK_CTRL[14] CIO_CLK_ICG bit).

10.3.4.4.15 DSI Power Control of DSI PHY and DSI PLL

The DSI protocol engine can control and send power commands for the DSI PHY and DSI PLL controller modules.

10.3.4.4.15.1 DSI PHY Control Commands

10.3.4.4.15.1.1 DSI PHY Control Commands

The DSI PHY can be set in three modes:

- OFF: In this power state, the complete DSI_PHY_DSS_x circuit is powered down. The internal LDO is OFF.
- ON: In this power state, the complete DSI_PHY_DSS_x circuit is powered on and functional.
- ULPS: In this power state, the ULPS exit detection circuit power switch is ON for the lanes that are in receive ULPS. For the lanes that are in transmit ULPS, the circuitry for weak pulldown is ON. ULPS must be used only when all three lanes are in ULPS (transmit or receive).

10.3.4.4.15.1.2 DSI PHY Power FSM

Figure 10-141 shows the FSM to control the power state of the DSI PHY

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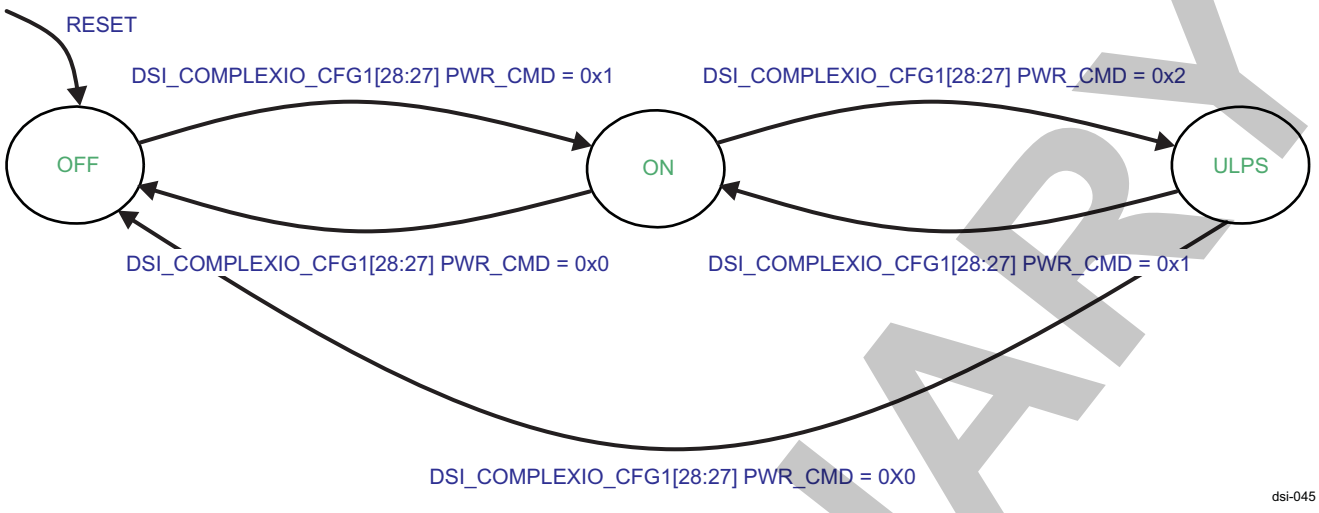
Figure 10-141. DSI PHY Power FSM



The following commands control the state transition of the DSI PHY:

- PwrCmdOff
- PwrCmdUlp
- PwrCmdOn

The DSI_COMPLEXIO_CFG1[28:27] PWR_CMD bit field allows the state to be modified. The allowed transitions are: OFF–ON, ON–ULPS, and ULPS–OFF. The DSI_COMPLEXIO_CFG1[26:25] PWR_STATUS bit field gives a status on the current state of the DSI PHY.

CAUTION

- In automatic mode, software must ensure that the DSI PHY is in ON state (that is, ON command already sent) before sending requests to the DSI PHY.
- In a command request to change to a state that is the current one (acknowledge has been received), the command is ignored (nothing is sent to the DSI PHY).
- To change the state to ULPS, all ULPSActiveNot signals must be low. The ULPSActiveNot_ALL0_IRQ interrupt indicates the state of the ULPSActiveNot signals. The change from ULPS to ON state is required before starting the ULP exit sequence (for more information, see Section 10.3.4.4.7.1, *T_{wakeup} Timer*).

10.3.4.4.15.2 DSI PLL Power Control Commands

The DSI PLL controller module can be set in four modes:

- OFF: DSI PLL and HSDIVIDER are OFF.
- ON ALL: DSI PLL and HSDIVIDER are ON. The CLKIN2DDR clock is provided to the DSI PHY, and the second clock output is provided to the HSDIVIDER.
- ON HSCLK: The DSI PLL is ON. The HSDIVIDER is OFF. The CLKIN2DDR clock is provided to the DSI PHY, but the second clock output is not provided to the HSDIVIDER.
- ON DIV: DSI PLL and HSDIVIDER are ON. The CLKIN2DDR clock is not provided to the DSI PHY, but the second clock output is provided to the HSDIVIDER.

10.3.4.4.15.2.1 DSI PLL Power FSM

Figure 10-142 shows the power state of the DSI PLL.

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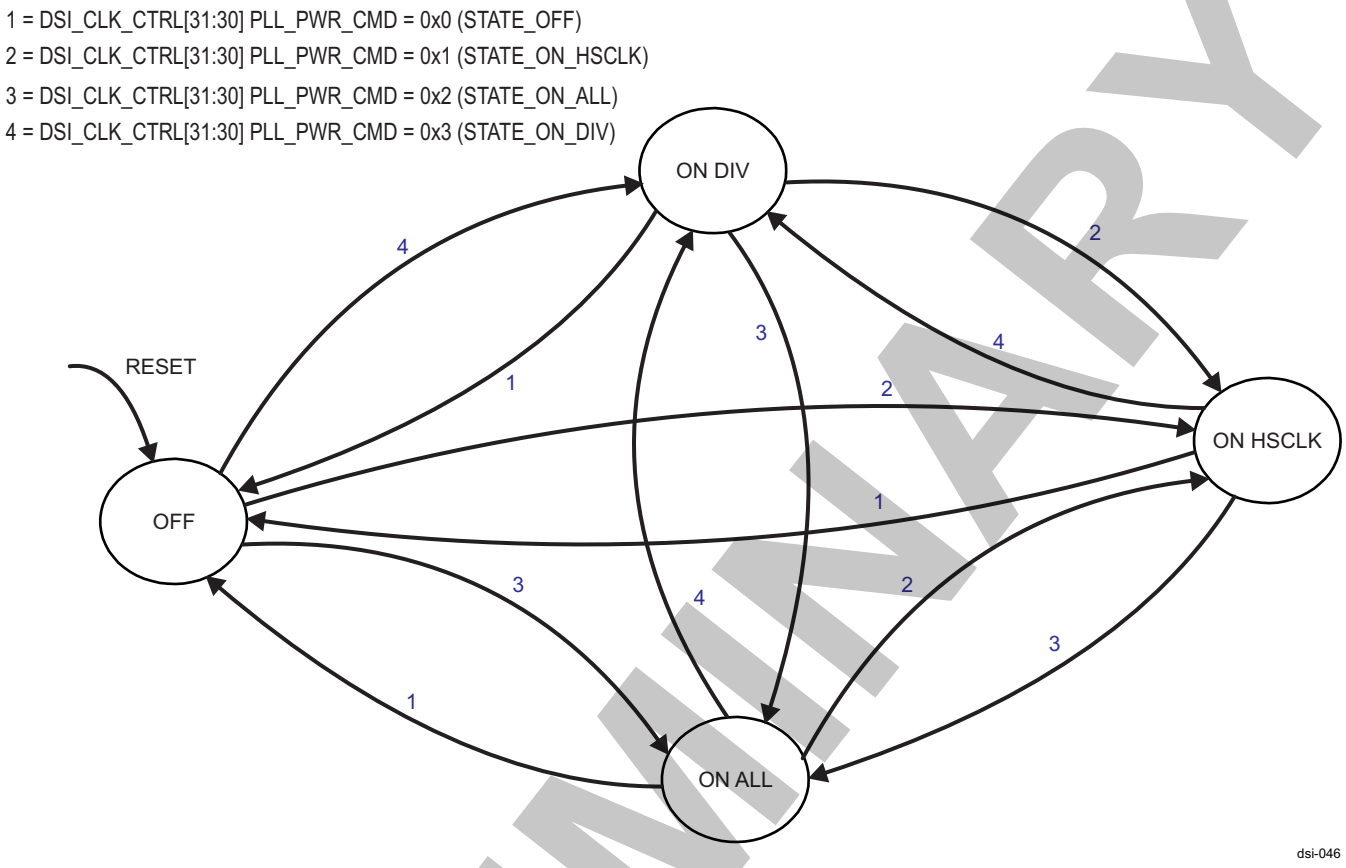
Figure 10-142. DSI PLL Power FSM



The following commands control the state transition of the DSI PLL control module:

- PLLPwrCmdOff
- PLLPwrCmdOnAll
- PLLPwrCmdOnDIV
- PLLPwrCmdOnHSClk

Setting the DSI_CLK_CTRL[31:30] PLL_PWR_CMD bit field modifies the state. The DSI_CLK_CTRL[29:28] PLL_PWR_STATUS bit field gives a status on the current state of the DSI PLL controller.

NOTE: If a command requests to change to a state that is the current one (acknowledge has been received), the command is ignored (nothing is sent to the DSI PLL control module).

10.3.4.4.15.2.1.1 DSI PLL HS Clock Signals

The DSIStopClk signal is provided to the DSI PLL control module. It indicates when the DSI protocol engine does not need to use HS mode and the PLL HS output (CLKIN2DDR clock) can be stopped. The following conditions must also be met when DISPC_UPDATE_SYNC may be generated by the DISPC, because that must result in the PLL HS output being stopped.

When the interface is disabled (the DSI_CTRL[0] IF_EN bit set to 0) and the clock lane is stopped (DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON = 0), the DSIStopClk signal is asserted.

Assertion of DSIStopClk depends on the following conditions:

- Clock lane TxRequestHS is deasserted (the DDR clock on the clock lane is no longer required). For deassertion of TxRequestHS, the following conditions are required:

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- The DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit must be reset to 0 and no HS data transfer must be ongoing or already scheduled.
- No VC ACTIVE in video mode. No VC using the video mode is enabled. If the VC is enabled, the mode is command mode only (the DSI_VC_CTRL_i[0] VC_EN bit set to 1 and the DSI_VC_CTRL_i[4] MODE bit set to 0).
- No command mode requiring HS transfer (one or more VCs using command mode can be active)
- Or the DSI_CTRL[0] IF_EN bit is reset to 0 (the previous conditions are not all required, except the DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit must be set to 0 after resetting the DSI_CTRL[0] IF_EN bit)

Deassertion of DSIStopClk depends on one of the following conditions (the DSI interface is enabled by setting the DSI_CTRL[0] IF_EN bit to 1):

- Clock lane TxRequestHS must be asserted (the DDR clock on the clock lane is required).
- One video mode VC ACTIVE
- At least one VC in command mode requiring HS transfer
- The DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit is set to 1 by software users (the DSI_CTRL[0] IF_EN bit must be reset to 0 for updating the value of the DDR_CLK_ALWAYS_ON bit).

Automatic assertion/deassertion is enabled by using the DSI_CLK_CTRL[18] HS_AUTO_STOP_ENABLE bit.

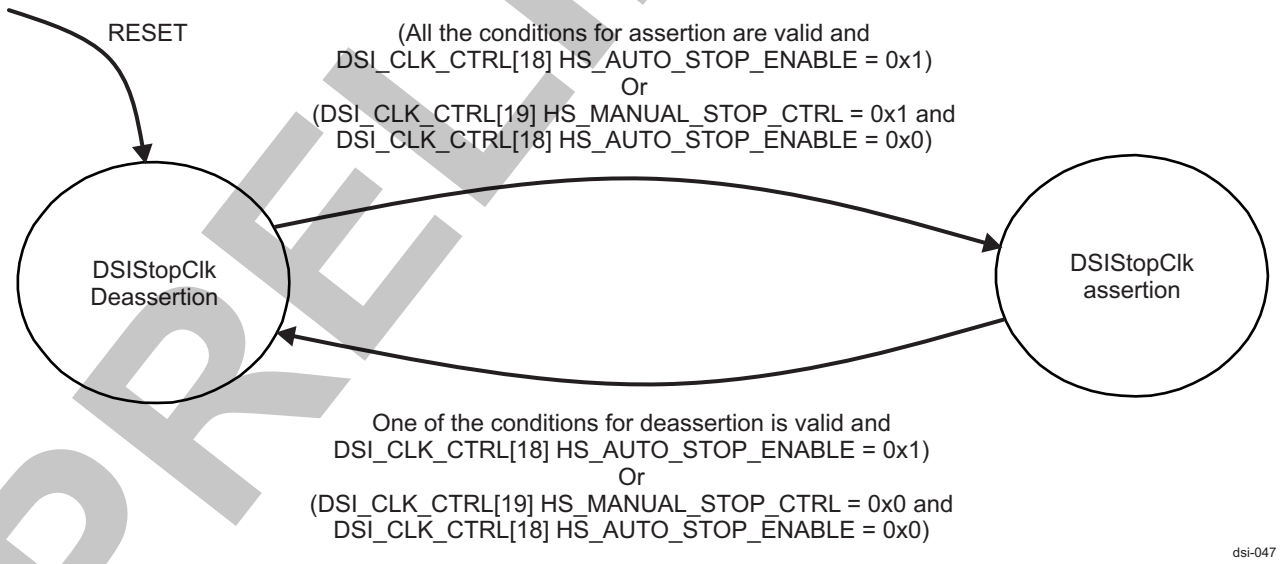
Manual mode can be used by setting and resetting the DSI_CLK_CTRL[19] HS_MANUAL_STOP_CTRL bit to assert or deassert the DSIStopClk signal.

NOTE: Setting the DSI_CTRL[24] DISPC_UPDATE _SYNC bit to 0x1 enables the use of the Dispc_Update_Sync signal to synchronize.

10.3.4.4.15.2.1.2 DSI PLL HS Clock FSM

Figure 10-143 shows the DSI PLL HS clock FSM.

Figure 10-143. DSI PLL HS Clock FSM



When DSIStopClk is used, there is a latency through other modules (DSI PLL controller and DSI_PHY_DSS_x) before TXBYTECLKHS is stopped. This latency must be considered to prevent any issue when DSIStopClk is deasserted soon after being asserted. This is done using a hardware timer programmed using the DSI_STOPCLK_TIMING[7:0] DSI_STOPCLK_LATENCY bit field. This timer is programmed in a number of periods of the DSI protocol functional clock (DSI_CLK). At the reset value, the timer is programmed with the value 0x80 (128).

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CAUTION

The programmed value in the DSI_STOPCLK_TIMING[7:0] DSI_STOPCLK_LATENCY bit field must be greater than ((3 × L3_MAIN_ICLK period) + (5 × CLKIN2DDR period)) / (DSI_CLK period).

10.3.4.4.16 DSI ULPS Configuration

This section describes how to enter and exit ULPS.

NOTE: The DSI_COMPLEXIO_CFG2[9:0] LANEx_ULPS_SIGy bit field (***where x*** = 1 to 5, corresponding to the five lanes of DSI1_A, and DSI1_C; ***and where y*** = 1 to 2) must be read back after writing to verify that the write operations are effective before proceeding to the next step. This considers low TxClkEsc frequencies.

10.3.4.4.16.1 DSI Entering ULPS

To enter ULPS for a clock lane, the following sequence is required:

1. Wait for the DSI_COMPLEXIO_CFG2[16] HS_BUSY and DSI_COMPLEXIO_CFG2[17] LP_BUSY bits to be reset to 0 and ensure that the DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON bit is 0.
2. The state of TxUlpsClk changes from INACTIVE to ACTIVE by setting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit field to 1.

To enter into ULPS for a data lane, the following sequence is required:

1. Wait until all TX_FIFOs for all VCs working in HS are empty, video mode is not active, and the DSI_COMPLEXIO_CFG2[16] HS_BUSY bit is reset to 0 (in addition for the first data lane, the DSI_COMPLEXIO_CFG2[17] LP_BUSY bit is reset to 0).
2. The state of TxRequestEsc changes from INACTIVE to ACTIVE by setting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit field to 1.

10.3.4.4.16.2 DSI Exiting ULPS

To exit ULPS for a clock lane, the following sequence is required:

1. Change the state of TxUlpsExit for each lane to ACTIVE by setting the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit field to 1.
2. Wait for the ULPSACTIVENOT_ALL1_IRQ interrupt indicating that all lanes with TxUlpsExit active have acknowledged by asserting UlpsActiveNot. This is done by monitoring the DSI_COMPLEXIO_IRQSTATUS[31] ULPSACTIVENOT_ALL1_IRQ status bit.
3. Start the wake-up timer (GP timer).
4. Wait for the time-out.
5. Change the state of the TxUlpsClk signals to INACTIVE for the clock lane by resetting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit field to 0.
6. Reset the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit to 0.

NOTE: When the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 and DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit fields are both being written to 0, they can be combined into one write. Both bit fields must be read back to confirm they are effective before proceeding.

To exit ULPS for a clock lane, in case the DSI PHY is in OFF state (the DSI protocol engine sends the DSI PHY to OFF state [PWROFF command] by setting DSI_COMPLEXIO_CFG1[28:27] PWR_CMD = 0x0), the sequence is:

1. Change the state of the TxUlpsClk signals to INACTIVE for the clock lane by resetting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit field to 0.

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2. Change the state of TxUlpsExit for clock lane to INACTIVE by resetting the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit field to 0. This step is necessary only when a PWROFF command (the command for power control of the DSI PHY) is issued while the sequence for exiting is in progress (the TxUlpsExit signal is already in ACTIVE state).

NOTE: When the DSI_COMPLEXIO_CFG2 LANEx_ULPS_SIG2[9:5] and DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit fields are both being written to 0, they can be combined into one write. Both bit fields must be read back to confirm they are effective before proceeding.

To exit ULPS for a data lane, the following sequence is required:

1. Change the state of TxUlpsExit for each lane to ACTIVE by setting the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit field to 1.
2. Wait for the ULPSACTIVENOT_ALL1_IRQ interrupt indicating that all lanes with TxUlpsExit ACTIVE have acknowledged by asserting UlpsActiveNot. This is done by monitoring the DSI_COMPLEXIO_IRQSTATUS[31] ULPSACTIVENOT_ALL1_IRQ status bit.
3. Start the application wake-up timer (GP timer).
4. Wait for the time-out.
5. Change the state of the TxRequestEsc signals to INACTIVE for the data lane by resetting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit field to 0.
6. Reset the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit field to 0.

NOTE: When the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 and DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit fields are both being written to 0, they can be combined into one write. Both bit fields must be read back to confirm they are effective before proceeding.

To exit ULPS for a data lane, in case the DSI PHY is in OFF state (the DSI protocol engine sends the DSI PHY into OFF state by setting DSI_COMPLEXIO_CFG1[28:27] PWR_CMD bit field to 0x0), the sequence is:

1. Change the state of the TxRequestEsc signals to INACTIVE by resetting the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 bit field to 0.
2. Change the state of TxUlpsExit to INACTIVE by resetting the DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit field to 0. This step is necessary only when a PWROFF command is issued while the sequence for exiting is in progress (the TxUlpsExit signal is already in ACTIVE state).

NOTE: When the DSI_COMPLEXIO_CFG2[9:5] LANEx_ULPS_SIG2 and DSI_COMPLEXIO_CFG2[4:0] LANEx_ULPS_SIG1 bit fields are both being written to 0, they can be combined into one write. Both bits must be read back to confirm they are effective before proceeding.

When the sequence for entering or exiting ULPS is started for specific lanes, users must wait for the completion of the sequence before changing the state of the same or other lanes.

10.3.4.4.17 DSI Interrupts

A single interrupt request (IRQ) is generated by each DSI: DSI_IRQ. This interrupt line is merged with another interrupt line from the DISPC_IRQ into a single IRQ. The DSI_IRQ events are generated only for the enabled VC(s). Two registers are used to enable and monitor the DSI interrupt events:

- DSI_IRQENABLE: This register enables and disables interrupt event reporting for the VCs. Each event for the VC is configured in the DSI_VC_IRQENABLE_i register dedicated to the VC number. In addition, it includes 1 bit to enable error reporting for the DSI PHY. The interrupt is triggered when any error is received from the DSI PHY.
- DSI_IRQSTATUS: The register flags which VC(s) have generated an interrupt. Based on the VC number, the DSI_VC_IRQSTATUS_i register indicates the event generating the interrupt. In addition, it

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includes 1 bit for the status of error reporting for the DSI PHY.

Table 10-538 lists the DSI VC interrupt events

Table 10-538. DSI VC Interrupts

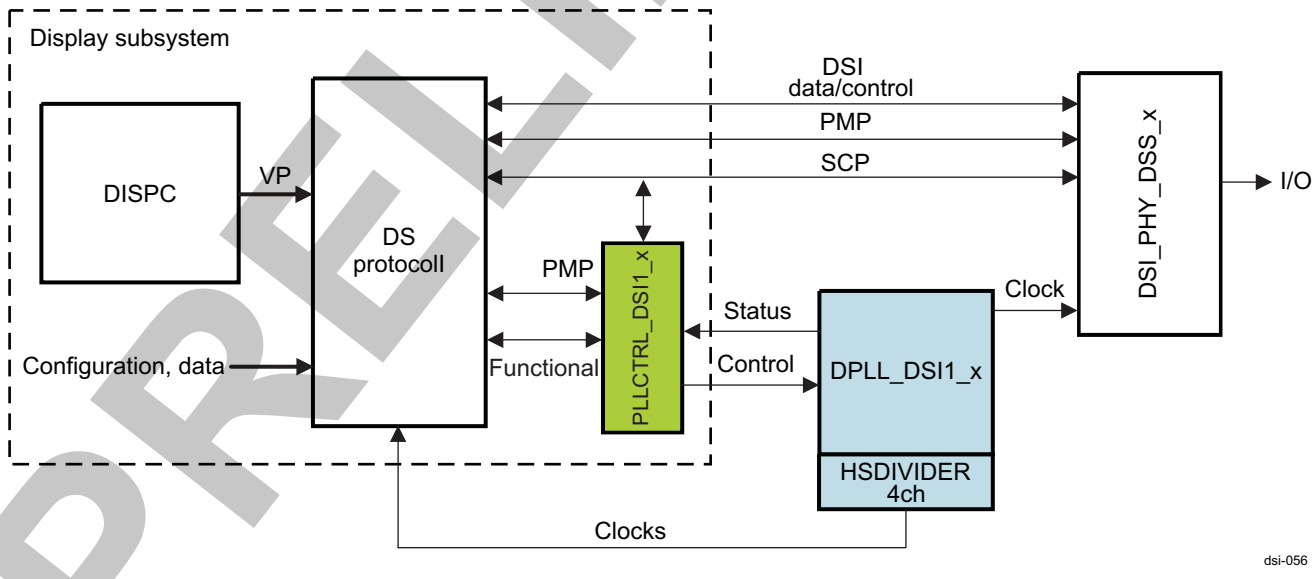
IRQ Name	Description
ECC_CORRECTION_IRQ	Indicates whether a 1-bit error correction has occurred using ECC (short and long packets)
PACKET_SENT_IRQ	Indicates that a packet has been sent. It is used when BTA manual mode is used.
CS_IRQ	Virtual channel. Checksum of the payload mismatch detection.
FIFO_RX_OVF_IRQ	RX FIFO overflow. The FIFO used on the L3_MAIN interconnect slave port for buffering the data received on the DSI link has overflowed.
FIFO_TX_OVF_IRQ	TX FIFO overflow. The FIFO used on the L3_MAIN interconnect slave port for buffering the data received on the interface slave port has overflowed.
BTA_IRQ	BTA is received from the peripheral (the VC ID used for the last BTA request transfer to the peripheral will be used to determine which VC will be used to flag the interrupt).
ECC_NO_CORRECTION_IRQ	ECC error (short and long packets). No correction of the header because of more than 1-bit error.
FIFO_TX_UDF_IRQ	TX FIFO underflow. The FIFO used on the slave port for buffering the data received on the L3_MAIN interconnect slave port has underflowed in the middle of a packet transfer.

10.3.4.5 DSI PLL Controllers

10.3.4.5.1 DSI PLL Controllers Overview

Two DSI PLL controller modules are part of the display subsystem. They use the SCP (see Section 10.3.4.4.6, *Serial Configuration Port Interface*) and power-management port (PMP) as the primary interfaces to the DSI protocol engines. The SCP interface sets the configuration of the digital phase-locked loop (DPLL) and HSDIVIDER modules, primarily the various counter values. The PMP controls the power state of the DPLL and HSDIVIDER modules. Figure 10-144 is an overview of a single DSI PLL controller module in the display subsystem.

Figure 10-144. DSI PLL Controller Overview



NOTE: The DSI PLL controller modules do not have an interface to L3_MAIN interconnect. The programmable features are managed by registers mapped into the DSI protocol engines.

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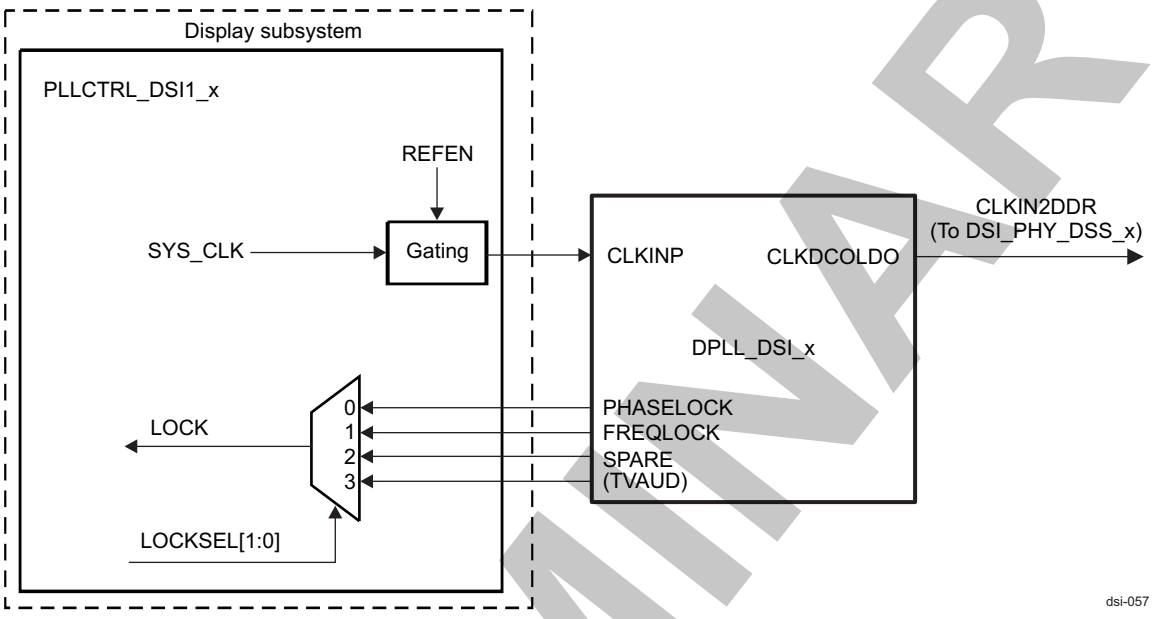
10.3.4.5.2 DSI PLL Controllers Architecture

The DSI PLLs use type-A instances of the DPLL modules. For information regarding DPLL types, see , *Generic DPLL Overview*, in Chapter 3, PRCM. The pixel clock (PCLK) frequency range is up to 103 MHz.

Figure 10-145 shows the internal reference diagram of a single DSI PLL.

Figure 10-145. DSI PLL Reference Diagram

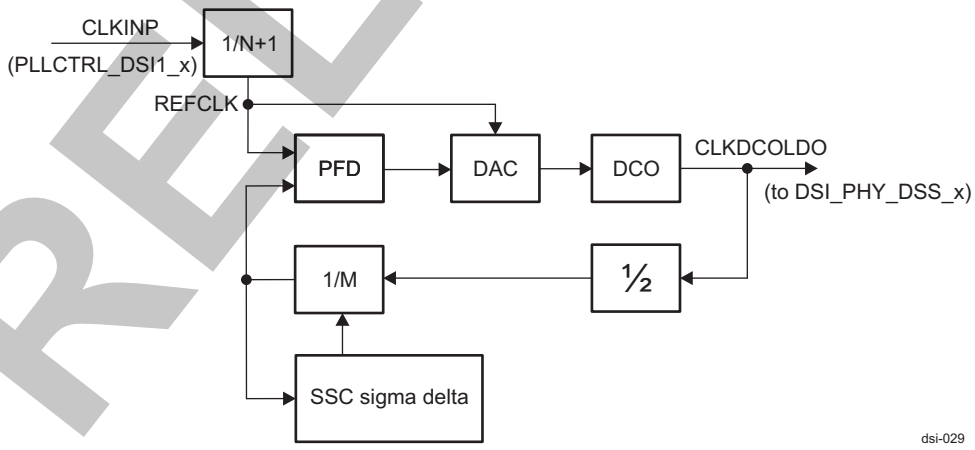


The DSI PLL clock output (CLKDCOLDO) corresponds to the CLKIN2DDR clock of a DSI PHY (DSI_PHY_DSS_x) module.

Only the SYS_CLK clock is used as an input reference clock for the DPLL. The DSI PLL controller can gate this clock by setting the DSI_PLL_CONFIGURATION2[13] PLL_REFEN bit.

Figure 10-146 is a simplified block diagram of the ADPLLM instance used for the DSI modules.

Figure 10-146. DSI DPLL Functional Block Diagram



The input clock CLKINP goes to a predivider N + 1. The entire loop runs on the REFCLK clock after this predivider. The value of N + 1 is controlled through the DSI_PLL_CONFIGURATION1[8:1] PLL_REGN bit field. The frequency range for the CLKINP and REFCLK clocks is as below:

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Table 10-539. DSI PLL CLKINP and REFCLK frequency range

Clock	Type	Min Frequency	Max Frequency
CLKINP	Input	0.032MHz	52MHz
REFCLK when DSI_PLL_CONFIGURATION2[5] PLL_PLLLPMODE	Input	0.15MHz	52MHz
REFCLK when DSI_PLL_CONFIGURATION2[5] PLL_PLLLPMODE	Input	0.032MHz	1MHz

The output clock CLKDCOLDO is synthesized by a digitally controlled oscillator (the DCO block) that automatically detects the frequency range. The CLKDCOLDO frequency can be given with CLKDCOLDO = CLKINP * 2 * M / (N + 1). For that purpose the feedback multiplier M must be configured through the DSI_PLL_CONFIGURATION1[20:9] PLL_REGM bit field.

The DPLL module also supports spread spectrum clocking (SSC) on its output clocks. SSC is used to spread the spectral peaking of the clock to reduce electromagnetic interference (EMI). When SSC is enabled, the clock spectrum is spread by the amount of frequency spread, and the attenuation is given by the ratio of the frequency spread (df) and the modulation frequency (fm), that is, $[\{10*\log_{10}(df/fm)\} - 10]$ dB.

The SSC is performed by changing the feedback divider (M) in a triangular pattern, which means the frequency of the output clock varies in a triangular pattern. The frequency of the triangular pattern is modulation frequency (fm). The peak (dM) or the amplitude of the triangular pattern as a percent of M is equal to the percent of the frequency spread (df) (that is, dM / M = df / Fout).

Since this is in band modulation for the DSI PLL, the modulation frequency (fm) is required to be within the bandwidth of the PLL loop (lowest BW of REFCLK/70; that is, REFCLK must be > fm*70). A higher modulation frequency results in less spreading in the output clock.

The SSC can be enabled and disabled by asserting the DSI_PLL_SSC_CONFIGURATION1[0] EN_SSC bit. The acknowledge signal SSCACK, observed by the DSI_PLL_STATUS[12] SSC_EN_ACK bit, notifies the exact start and end of SSC. When EN_SSC is deasserted, SSC is disabled only after completion of one full cycle of the triangular pattern given by the modulation frequency. This is done to maintain the average frequency.

The modulation frequency (fm) can be programmed as a ratio of REFCLK/4; that is, the value of ModFreqDivider programmed in the DSI_PLL_SSC_CONFIGURATION2[29:20] MODFREQDIVIDER bit field must be = REFCLK / (4 * fm). The ModFreqDivider is split into Mantissa and $2^{Exponent}$(ModFreqDivider = ModFreqDividerMantissa *$2^{ModFreqDividerExponent}$).

- The Mantissa is controlled by bits [29:23] of the MODFREQDIVIDER bit field.
- The Exponent is controlled by bits [22:20] of the MODFREQDIVIDER bit field.

Although the same value of ModFreqDivider could be obtained by different combinations of Mantissa and Exponent values, it is preferred to get the target ModFreqDivider by programming maximum Mantissa and minimum Exponent values.

To define the frequency spread (df), M must be controlled as previously explained. To define M, the step size of M for each REFCLK during the triangular pattern bust be programmed (that is, M = ModFreqDivider * DeltaMStep). DeltaMStep is controlled by the DSI_PLL_SSC_CONFIGURATION2[19:0] DELTAM bit field and the PLL_SSC_CONFIGURATION2[30] DELTAM2 bit. DeltaMStep is split into an integer part and a fractional part:

- The integer part is controlled by bits [19:18] of the DELTAM bit field.
- The fractional part is controlled by bits [17:0] of the DELTAM bit field.The frequency spread achieved, however, has an overshoot of 20% or an inaccuracy of +20%.

If the DSI_PLL_SSC_CONFIGURATION1[2] DOWNSPREAD bit is set to 1, the frequency spread on the lower side is twice the programmed value. The frequency spread on the higher side is 0 (except for the overshoot, as previously described).

NOTE: There is a restriction in the range of M values. The restriction is that (M – dM) must be >= 20.Also, M + dM should be <= 2045. If the DSI_PLL_SSC_CONFIGURATION1[2] DOWNSPREAD bit is set to 1, then (M – 2*dM) should be >= 20 and M <= 2045.

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10.3.4.5.3 DSI PLL Operations

The DSI PLL configuration signals operate according to Table 10-540, which indicates the operation when the PLLs are not locked.

Table 10-540. DSI PLL Operation Modes When Not Locked

DSI PLL Operation Mode	Stop Mode Low Power[1]	Stop Mode Fast Relock[1]	Idle Bypass
Mode Description	Output clocks stopped Lowest power standby	Output clocks stopped Fastest start-up time	Selects when PLL and HSDIVIDER bypass clocks are used
DSI_PLL_CONFIGURATION2[0] PLL_IDLE	0	0	1
DSI_PLL_CONFIGURATION2[6] PLL_LOWCURRSTBY	1	0	1

(1) This mode must be used for better performance.

When locked, the PLL output frequency is: Input frequency × 2 × M / (N + 1), where:

- M multiplier is programmed in the DSI_PLL_CONFIGURATION1[20:9] PLL_REGM bit field.
- N divider is programmed in the DSI_PLL_CONFIGURATION1[8:1] PLL_REGN bit field.

NOTE: When the PLL_REGM bit-field is set to 1, the PLL enters a MN-Bypass mode. This is a low power mode, where the PLL gates its internal clocks and powers down the analog blocks. The CLKDCOLDO clock output goes low and remains like that, until the PLL comes out of the MN-Bypass mode (by changing the PLL_REGM bit-field to a value other than 0 or 1).

10.3.4.5.4 DSI PLL Controllers Shadowing Mechanism

The configuration registers are accessed through the DSI protocol engine register spaces using the SCP interface. This includes all the configuration signals and returning status signals.

CAUTION

All writes must be 32-bit operations, because the SCP interface always transfers 32 bits; 16- or 8-bit operations may lead to unpredictable errors.

A shadow mechanism is implemented for appropriate register values so that configurations can optionally be updated in synchronization with the DISPC and DSI protocol engines. The front porch time from the DISPC indicates the time when making the update of the value. All the required updated values must be written before this signal is asserted. For more information, see Section 10.3.4.4.6.1, *Shadowing Register*.

10.3.4.5.5 DSI PLL Error Handling

The PLL lock and recalibration signals can be monitored to detect the loss of lock or the requirement to recalibrate (caused by a large temperature change since the last lock request):

- The DSI_PLL_STATUS[1] PLL_LOCK status bit gives the DSI PLL lock state.
- The DSI_PLL_STATUS[2] PLL_RECAL status bit informs whether the PLL must be uncalibrated.

These signals can also generate interrupts at the DSI protocol engine level:

- The PLL_LOCK_IRQ interrupt indicates that the DSI PLL control module has sent a lock request to the DSI PLL. To monitor this event, read the DSI_IRQSTATUS[7] PLL_LOCK_IRQ bit. Set this bit to 1 to clear the status bit.
- The PLL_UNLOCK_IRQ interrupt indicates that the DSI PLL control module has sent an unlock request to the DSI PLL. To monitor this event, read the DSI_IRQSTATUS[8] PLL_UNLOCK_IRQ bit. Set this bit to 1 to clear the status bit.

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- The PLL_RECAL_IRQ interrupt indicates that the DSI PLL control module has sent a recalibration request to the DSI PLL. To monitor this event, read the DSI_IRQSTATUS[9] PLL_RECAL_IRQ bit. Set this bit to 1 to clear the status bit.

The PLL reference loss and limp status signals can also be monitored:

- The DSI_PLL_STATUS[3] PLL_LOSSREF status bit informs whether the DSI PLL has lost the reference.

10.3.4.5.6 DSI PLL Software Reset

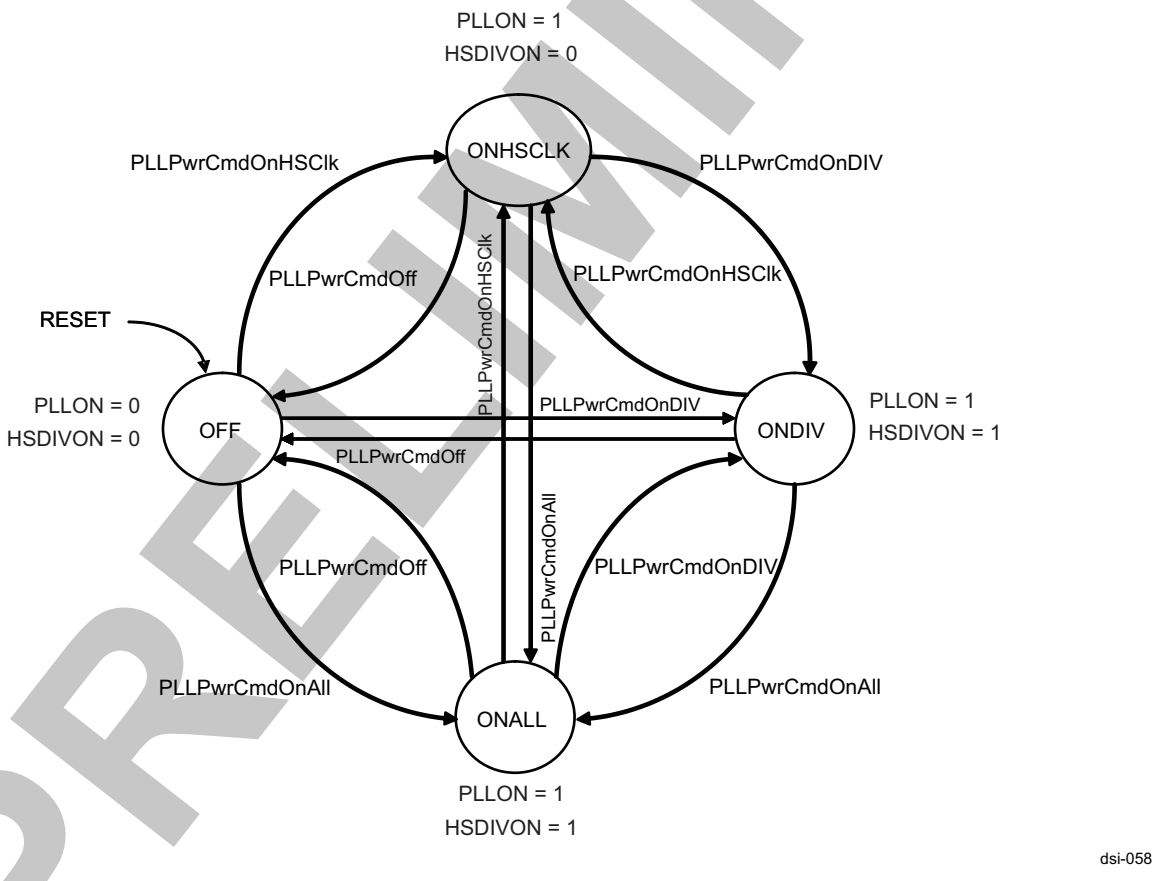
The DSI PLL control modules do not have their own software reset. They are reset by the global DSS_RST signal at PRCM module level. See Display Subsystem Resets, in *Display Subsystem*. Nevertheless, software users can monitor the reset statuses of the DSI PLL control modules by reading the DSI_PLL_STATUS[0] PLLCTRL_RESET_DONE status bits.

10.3.4.5.7 DSI PLL Power Management

PLLCTRL manages only the LDO power of the DPLL and HSDIVIDER; this is done by overriding the SYSRESET signals. All other power-management signals are integrated with the display subsystem power management.

Figure 10-147 shows the power states that are controlled through the PMP.

Figure 10-147. DSI PLL Power State Diagram



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10.3.4.5.8 DSI PLL HSDIVIDER Loading Operation

In manual mode (PLL_CONTROL[0] PLL_AUTOMODE = 0), it is possible to update the configuration values of HSDIVIDER without starting the DPLL locking sequence. Once all the configuration values have been programmed into the registers, the PLL_GO[1] HSDIVLOAD bit must be set. The TENABLEDIV output is driven high for six SCP clock periods while the TINITZ and TENABLE signals remain unchanged. The HSDIVLOAD bit is cleared at the end of the sequence.

The TENABLEDIV signal is shared with the DPLL and HSDIVIDER so the DPLL M2 divider is loaded at the same time. The SCPBUSY signal is high during the sequence until the HSDIVLOAD bit is cleared, thus indicating that there is pending activity in the SCPClk domain. SCPClk must be kept running while this signal is asserted.

The HSDIVIDER sequence and the GO sequence (Section 10.3.4.5.11, *DSI PLL Go Sequence*) cannot be performed at the same time. If one of the two sequences is running and the trigger bit of the other sequence is set, PLLCTRL finishes the first sequence and then immediately starts the other sequence.

10.3.4.5.9 DSI PLL Clock-Gating Sequence

Clock gating can be used to reduce system power consumption when the DSI protocol engine indicates that it does not need the clock. If the HSDIVIDER is not used, the PLL can also be stopped (at the cost of additional unstarting latency).

The DSI protocol engines must verify when the PLLs have restarted by inspecting the LOCK signal (the DSI_PLL_STATUS[1] PLL_LOCK status bit), because the TXBYTECLKHS clocks are stopped when the CLKIN2DDR clocks generated by the DSI PLL are stopped. This eliminates the need for any explicit feedback that the clock has restarted. This flow chart shown in Figure 10-148 should run even if the DSI_PLL_GO[0] PLL_GO bit is not set.

Figure 10-148 shows the DSI PLL gated mode sequence.

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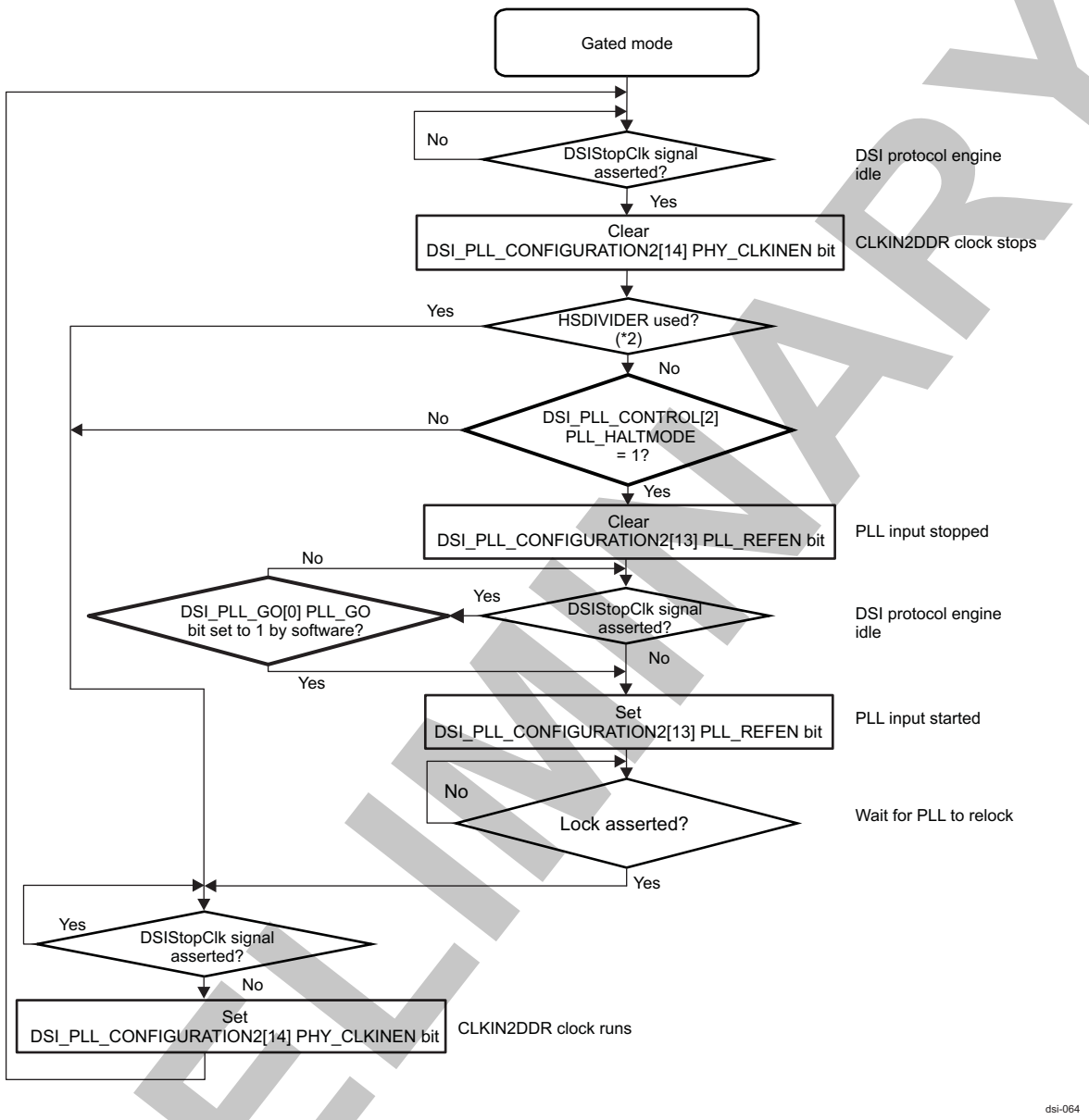
Figure 10-148. DSI PLL Gated Mode Sequence



(1) All thick-outlined blocks show operations performed by software. Other blocks show operations performed by hardware.

(2) HSDIVIDER is used if one of the following bits is set to 1:

- DSS_CTRL[12] LCD2_CLK_SWITCH
- DSS_CTRL[0] LCD1_CLK_SWITCH
- DSS_CTRL[18] DSI1_C_CLK_SWITCH
- DSS_CTRL[1] DSI1_A_CLK_SWITCH

(3) For more information, see Display Subsystem Overview, in *Display Subsystem*.

Table 10-541. DSI PLL Register Call Summary for Gated Mode Sequence

Register Name	Register Name	Register Name
DSI_PLL_CONFIGURATION2	DSI_PLL_CONTROL	DSI_PLL_GO

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10.3.4.5.10 DSI PLL Clock Sequence

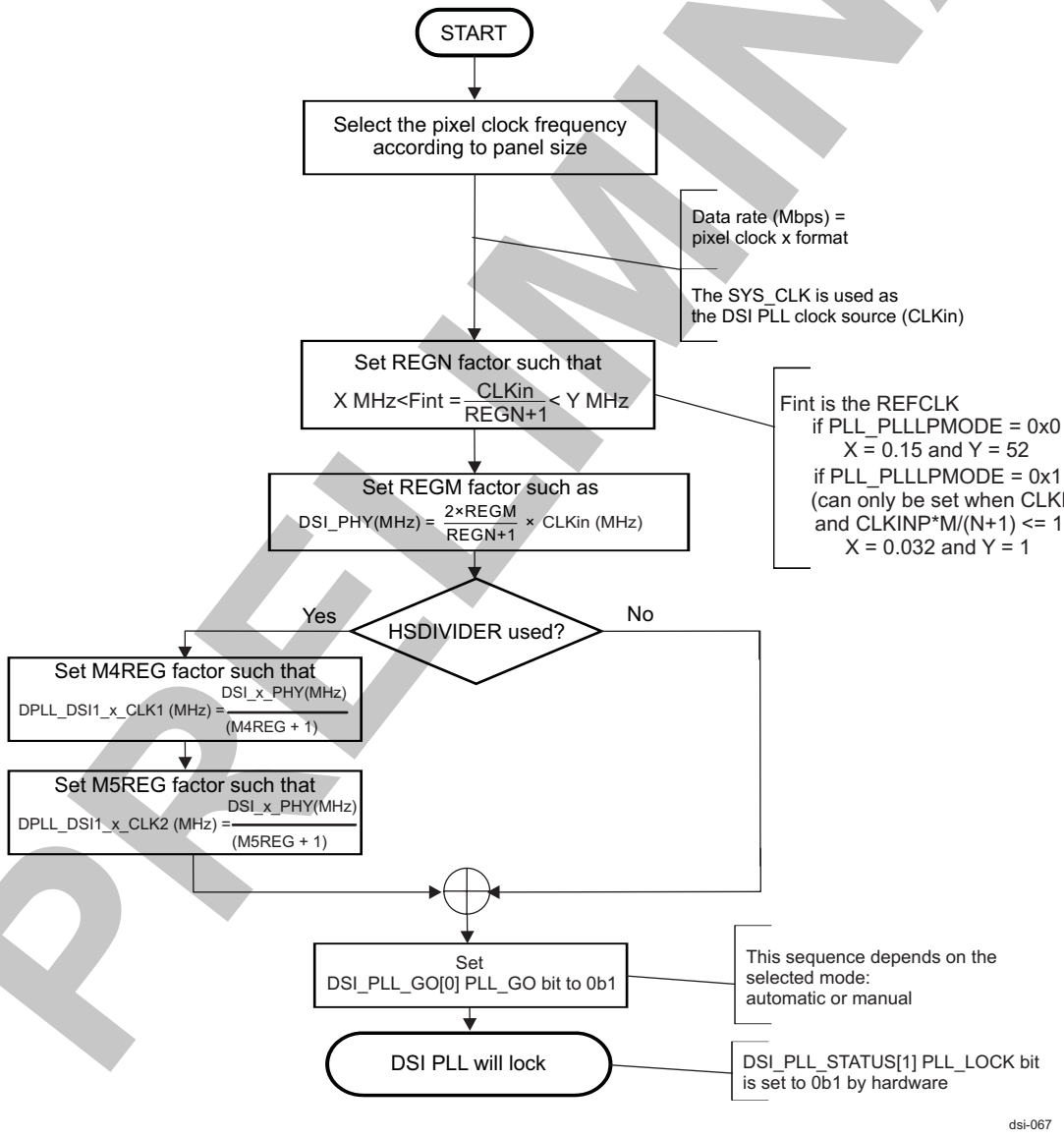
The two DSI PLLs generate the CLKIN2DDR clocks. Each HSDIVIDER outputs two clocks: DPLL_DSI1_x_CLK1, connected to the DISPC, and DPLL_DSI1_x_CLK2, connected to the DSI protocol engine (where x is the dedicated DSI PLLs [A or C]). If these two clocks are not used, the HSDIVIDER functions are not required.

The CLKIN2DDR clocks are twice the DSI output clock frequency, which is equal to the data rate. The DSI PLL factors must be calculated based on the required input and output frequencies, keeping the PLL internal reference frequency in the appropriate range:

- REGM factor is programmed by the DSI_PLL_CONFIGURATION1[20:9] PLL_REGM bit field.
- REGN factor is programmed by the DSI_PLL_CONFIGURATION1[8:1] PLL_REGN bit field.
- M4REG factor is programed by the DSI_PLL_CONFIGURATION1[25:21] M4_CLOCK_DIV bit field, and applies to DPLL_DSI1_x_CLK1.
- M5REG factor is programmed by the DSI_PLL_CONFIGURATION1[30:26] M5_CLOCK_DIV bit field, and applies to DPLL_DSI1_x_CLK2.

Figure 10-149 shows the programming sequence.

Figure 10-149. DSI PLL Programming Sequence



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NOTE:

- The M4REG and M5REG factors must be set respecting the following conditions:
  - The DPLL_DSI1_x_CLK1 frequency must be a multiple of PCLK frequency (for proper settings of the PCD and LCD factors in the DISPC).
  - The DPLL_DSI1_x_CLK1 and DPLL_DSI1_x_CLK2 frequencies must be lower than 200 MHz. For more information about clock frequency ratings, see Display Subsystem Clocks, in Chapter 10, *Display Subsystem*.
- Most of the other DSI PLL programming values are available for software flexibility, but it is not recommended to update the values in normal use. For the recommended DSI PLL values, see Section 10.3.4.5.12, *DSI PLL Recommended Values*.

Table 10-542. DSI Register Call Summary for DSI PLL Programming Sequence

Register Name	Register Name	Register Name
DSI_PLL_CONFIGURATION2	DSI_PLL_GO	DSI_PLL_STATUS

10.3.4.5.11 DSI PLL Go Sequence

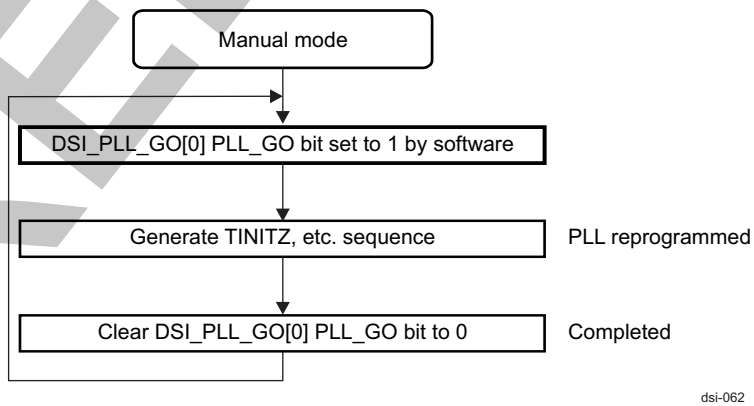
In manual mode (the DSI_PLL_CONTROL[0] PLL_AUTOMODE bit is set to 0), the DPLL requires a sequence on TINITZ, TENABLE, and TENABLEDIV to update the configuration values and start the locking sequence.

When all the configuration values are programmed into the registers, the GO bit must be set. The appropriate sequence is then sent on the TINITZ, TENABLE, and TENABLEDIV pins, respecting the timing requirements of the DPLL. The DSI_PLL_GO[0] PLL_GO bit is cleared to 0 at the end of the sequence.

The TENABLEDIV signal is shared with the HSDIVIDER module so that it is programmed at the same time. In this mode, software must deassert CLKINEN by setting the DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN bit to 0 and assert HSDIVBYPASS correctly by setting the DSI_PLL_CONFIGURATION2[20] HSDIVBYPASS bit to 1 to prevent uncontrolled frequencies affecting DSI_PHY_DSS_x and the display subsystem during PLL locking. In manual mode, the shadow register is updated anyway so that valid values are present when later selecting automatic mode.

Figure 10-150 shows the DSI PLL Go flow chart in manual mode (the DSI_PLL_CONTROL[0] PLL_AUTOMODE bit is set to 0).

Figure 10-150. DSI PLL Go Sequence (Manual Mode)



NOTE: All thick-outlined blocks show operations performed by software. Other blocks show operations performed by hardware.

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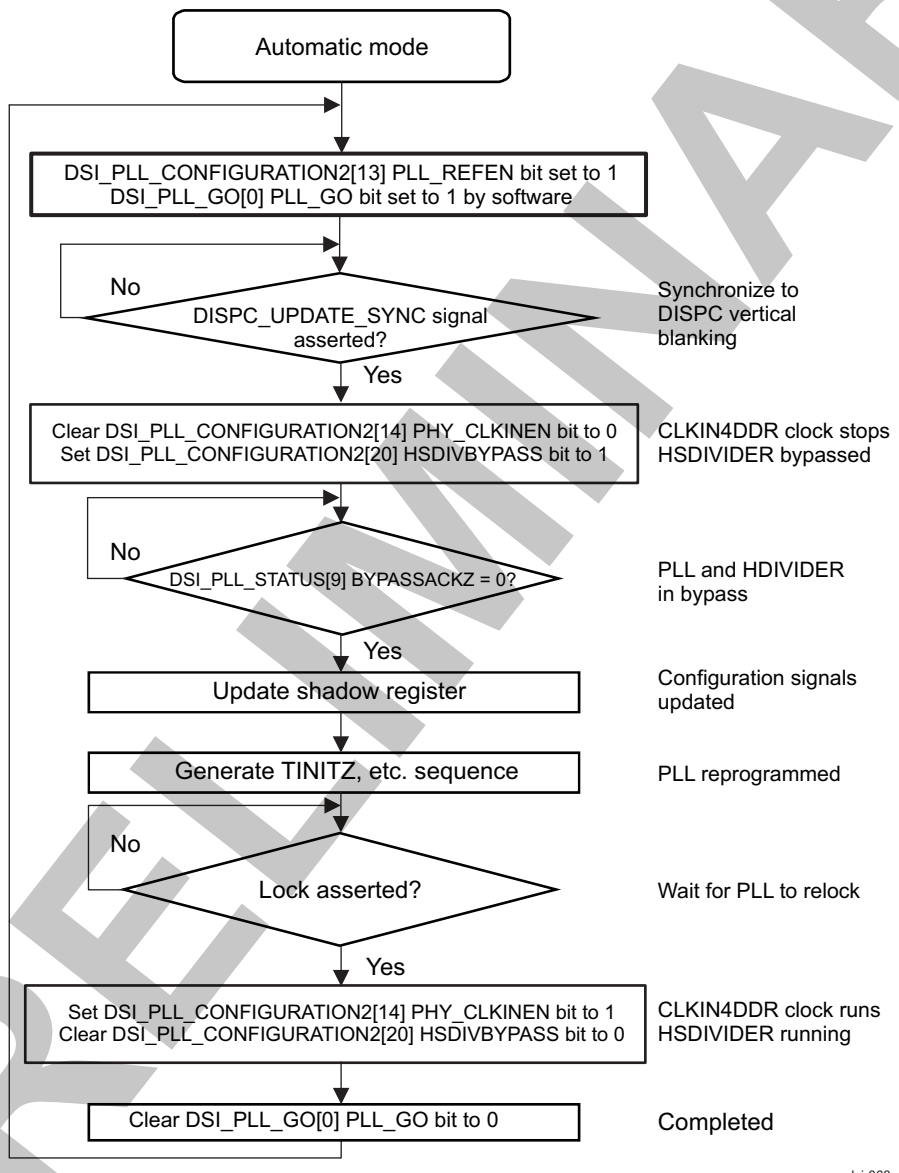
In automatic mode (the DSI_PLL_CONTROL[0] PLL_AUTOMODE bit is set to 1), the TINITZ, TENABLE, and TENABLEDIV sequence and the update of the PLL configuration from the DSI_PLL_CONFIGURATION2 register are deferred until the time of the front porch time signal sent by the DISPC module. This is intended to simplify the software to implement a configuration change (such as a frequency change to support a different link bandwidth). In this mode, CLKINEN, HSDIVBYPASS, and REFEN are automatically controlled and the register value is overridden.

Figure 10-151 shows the DSI PLL Go flow chart in automatic mode (the DSI_PLL_CONTROL[0] PLL_AUTOMODE bit is set to 1).

Figure 10-151. DSI PLL Go Sequence (Automatic Mode)



NOTE: All thick-outlined blocks show operations performed by software. Other blocks show operations performed by hardware.

Table 10-543. DSI Register Call Summary for DSI PLL Go Sequence (Automatic Mode)

Register Name	Register Name	Register Name
DSI_PLL_CONFIGURATION2	DSI_PLL_STATUS	DSI_PLL_GO

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10.3.4.5.12 DSI PLL Recommended Values

Table 10-544 shows the DSI PLL recommended values.

Table 10-544. DSI PLL Recommended Programming Values

Field Name	Value	Description
DSI_PLL_CONTROL[4] HSDIV_SYSRESET	0	Allow power FSM to control
DSI_PLL_CONTROL[3] PLL_SYSRESET	0	Allow power FSM to control
DSI_PLL_CONTROL[2] PLL_HALTMODE	–	For information, see Section 10.3.4.5.9, *DSI PLL Clock-Gating Sequence*.
DSI_PLL_CONTROL[1] PLL_GATEMODE	–	For information, see Section 10.3.4.5.9, *DSI PLL Clock-Gating Sequence*.
DSI_PLL_CONTROL[0] PLL_AUTOMODE	–	For information, see Section 10.3.4.5.9, *DSI PLL Clock-Gating Sequence*.
DSI_PLL_GO[0] PLL_GO	1–>0	Write 1 when PLL is to be (re)locked with new parameters. This bit is cleared by hardware when the PLL request completes.
DSI_PLL_CONFIGURATION1[30:36] M5_CLOCK_DIV	See (1).	DSI protocol engine clock divider
DSI_PLL_CONFIGURATION1[25:21] M4_CLOCK_DIV	See (1).	DSS clock divider
DSI_PLL_CONFIGURATION1[20:9] PLL_REGM	See (1).	Feedback clock divider
DSI_PLL_CONFIGURATION1[8:1] PLL_REGN	See (1).	Reference clock divider
DSI_PLL_CONFIGURATION2[20] HSDIVBYPASS	0	PLL controls HSDIVIDER bypass
DSI_PLL_CONFIGURATION2[18] M5_CLK_EN	1	If PLL/HSDIVIDER is used as the DSI protocol clock source
DSI_PLL_CONFIGURATION2[16] M4_CLOCK_EN	1	If PLL/HSDIVIDER is used as the clock source
DSI_PLL_CONFIGURATION2[15] BYPASSEN	0	To use PLL as the clock source. For small displays, it may be possible to use the display subsystem functional clock, DSS_CLK, in which case this bit must be set to 1. See Section 10.3.4.2, *DSI Clock Configuration*.
DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN	1	Enable CLKIN2DDR clock
DSI_PLL_CONFIGURATION2[13] PLL_REFEN	1	Enable PLL reference
DSI_PLL_CONFIGURATION2[10:9] PLL_LOCKSEL	0x0	Phase lock criteria to lock the PLL
DSI_PLL_CONFIGURATION2[8] PLL_DRIFTGUARDEN	0x0	The RECAL status/interrupt must be used to decide when to perform a PLL uncalibration. No automatic uncalibration is performed.
DSI_PLL_CONFIGURATION2[6] PLL_LOWCURRSTDBY	0/1	Set to 0 for fast PLL unlock, but higher standby current. Set to 1 for leakage level standby current, but longer unlock time.
DSI_PLL_CONFIGURATION2[5] PLL_PLLLPMODE	0	Normal operation. For smaller display sizes, it may be possible to set to 1.
DSI_PLL_CONFIGURATION2[0] PLL_IDLE	0	PLL active

(1) The value of the bit field must be set according to the desired clock frequency.

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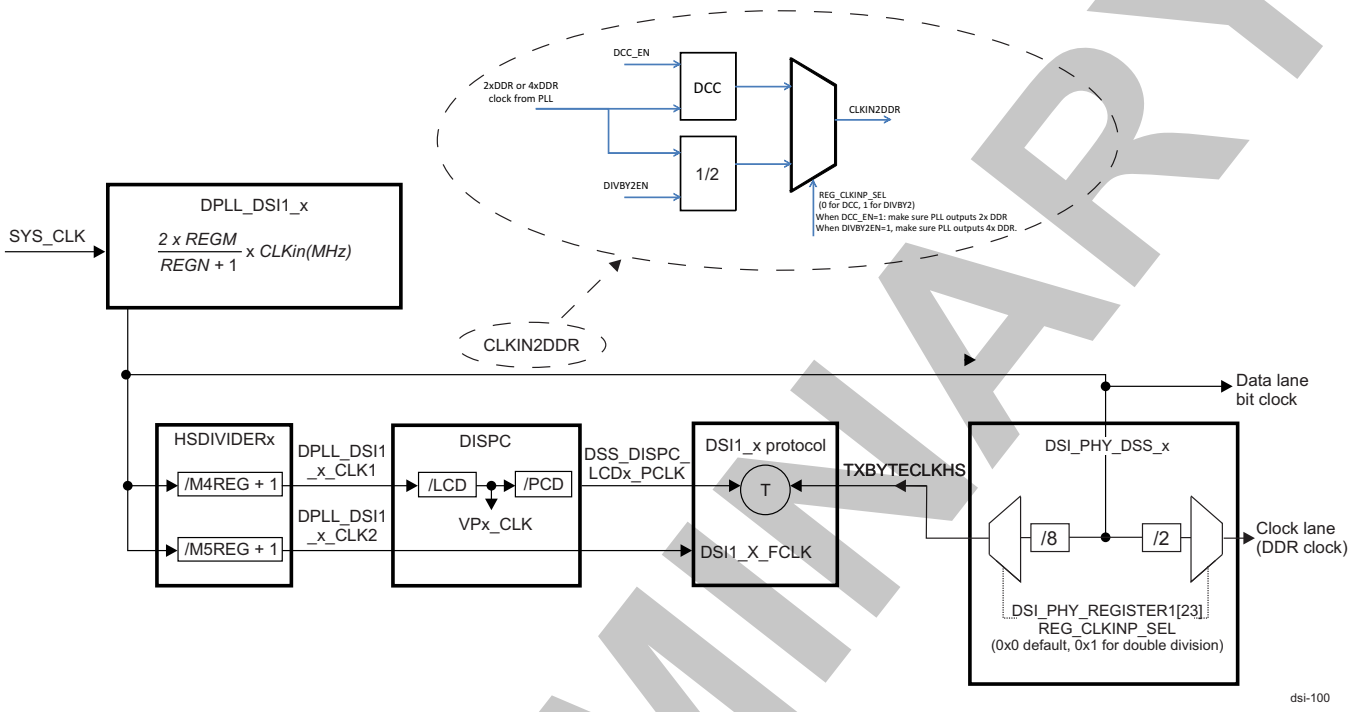
10.3.4.5.13 DSI How to Configure the DSI PLL in Video Mode

Figure 10-152 is a global overview of the DSI1_A and DSI1_C clock trees when used in video mode.

Figure 10-152. DSI Clock Tree in Video Mode



The settings of the DSI PLL registers can be summarized by the following equations.

Equation 1

$$N \times T_{VP\_CLK} = T_L \times T_{TXBYTECLKHS}$$

dsi-e101

where

- $T_L = T_{HS} + HSA_{DSI} + T_{HE} + HFP_{DSI} + ceiling((WC + 6) / NDL) + HBP_{DSI}$
- N is an integer.
- NDL: Number of data lanes
- WC: Word count or payload in bytes
- HSA_{DSI} is HSA period in video mode.
- HBP_{DSI} is HBP period in video mode.
- HFP_{DSI} is HFP period in video mode.

T_{HS} is the length of HSYNC start short packet in the number of byte clock cycles (TXBYTECLKHS).

- The generation of this packet can be enabled by setting the DSI_CTRL[17] VP_HSYNC_START bit to 1.
- T_{HS} is equal to ceiling(4 / NDL), if VP_HSYNC_START = 1; else, it is 0.

T_{HE} is the length of HSYNC end short packet in the number of byte clock cycles (TXBYTECLKHS).

- The generation of this packet can be enabled by setting the DSI_CTRL[18] VP_HSYNC_END bit to 1.
- T_{HE} is equal to 1, if (VP_HSYNC_START = 1, VP_HSYNC_END = 1, HSA_{DSI} = 0, and NDL = 3), else
- T_{HE} is equal to ceiling(4 / NDL), if (VP_HSYNC_START = 1 and VP_HSYNC_END = 1); else, it is 0.

NOTE: HSA_{DSI} timing is not used and does not have to be programmed when HE short packet is not generated.

Equation 2

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$$R = T_{TXBYTECLKHS} / T_{VP\_PCLK}$$
dsi-e102

To synchronize the DISPC and DSI protocol engines, users must follow the ratio R between TXBYTECLKHS and VP_PCLK, as listed in Table 10-545.

Table 10-545. DSI Ratio R

Number of Data Lanes (Up to 4 Data Lanes for DSI1_A and DSI1_C)	Pixel Format	Ratio R
1	16-bit pixel	1/2
1	18-bit pixel	4/9
1	24-bit pixel	1/3
2	16-bit pixel	1
2	18-bit pixel	8/9
2	24-bit pixel	2/3
3	16-bit pixel	3/2
3	18-bit pixel	4/3
3	24-bit pixel	1
4	16-bit pixel	2
4	18-bit pixel	16/9
4	24-bit pixel	4/3

All cases are covered by:

$$F_{VP\_PCLK} \times bits\_per\_pixel = F_{TXBYTECLKHS} \times NDL \times 8$$
dsi-e110

NOTE: Table 10-545 defines the strict ratio values to be used for no line buffer configuration (where DSI burst mode is not supported).

In case of two (or one) line buffers configuration (where DSI burst mode is supported), the ratio R = TTXBYTECLKHS / TVP _PCLK is not limited to the values in Table 10-545. It can be set to other values by ensuring that the line lengths on DISPC and DSI match Equation 3.

Equation 3

$$(HSA_{DISPC} + HFP_{DISPC} + PPL + HBP_{DISPC}) \times T_{VP\_PCLK} = (4/NDL + HFP_{DSI} + (WC+6)/NDL + HBP_{DSI}) \times T_{TXBYTECLKHS}$$
dsi-e103

Equation 4

$$HFP_{DSI} = ((HFP_{DISPC} \times bits\_per\_pixel)/(NDL \times 8)) - (2/NDL)$$
dsi-e109

Example

The desired performances are:

- Clock lane at 150 MHz
- RGB24-888
- 1-data lane
- LCD size 480 × 640 with $HSA_{DISP} = HFP_{DISP} = HBP_{DISP} = 20$, $VSA_{DISP} = VFP_{DISP} = VBP_{DISP} = 2$

Step 1. Determine REGM and REGN.

To obtain correct stability, F_{int} must be kept between 0.032 MHz and 52 MHz. In this case, F_{int} is maintained at 2 MHz. For more information, see Section 10.3.4.5.2, *DSI PLL Controllers Architecture*, Section 10.3.4.5.10, *DSI PLL Clock Sequence*, and Section 10.3.5.2.1.1, *Main Sequence – DSI PLL*

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Setup.

$$REGN = (F_{SYS\_CLK} / F_{int}) - 1$$
$$REGN = 12$$
$$REGM = (REGN + 1) \times F_{CLKIN2DDR} / (2 \times F_{SYS\_CLK})$$
$$REGM = 75$$

dsi-e113

where

- SYS_CLK = 26 MHz is used as a reference clock.

Step 2. Determine VP_PCLK and TXBYTECLKHS clocks.

TXBYTECLKHS frequency is equal to 37.5 MHz. With ratio R equal to 1/3, VP_PCLK frequency is equal to 12.5 MHz. The frame rate can be estimated by:

$$\text{Frame rate} = F_{VP\_PCLK} / (HSA_{DISPC} + HFP_{DISPC} + PPL + HBP_{DISPC}) \times (VSA_{DISPC} + LPP + VBP_{DISPC})$$
$$\text{Frame rate} = 12.5\ \text{MHz} / (540) \times (646)$$
$$\text{Frame rate} = 35.83\ \text{frame/sec}$$

dsi-e123

Step 3. Determine LCD, PCD, and M4REG.

$$T_{CLKIN2DDR} = T_{TXBYTECLKHS}/8 = T_{DSS\_DISPC\_LCDx\_PCLK}/((M4REG + 1) \times LCD \times PCD)$$
$$((M4REG + 1) \times LCD \times PCD) = 8 \times 3$$

dsi-e115

If LCD and PCD are set to 1 and 3, respectively, M4REG is equal to 7.

Step 4. Verify N as integer.

First, TL must be determined:

$$(HSA_{DISPC} + HFP_{DISPC} + PPL + HBP_{DISPC}) \times T_{VP\_PCLK} / T_{TXBYTECLKHS} = T_L = 1620$$

dsi-e116

From **Equation 1** follows:

$N \times T_{VP\_CLK} = T_L \times T_{TXBYTECLKHS}$

$N = T_{TXBYTECLKHS} \times T_L / T_{VP\_CLK} = T_L / (R \times PCD)$

$N = 14580$

N is an integer.

Step 5. Determine HFP and HBP of the DSI protocol engine.

From **Equation 3** follows:

$$((HSA_{DISPC} + HFP_{DISPC} + PPL + HBP_{DISPC}) \times T_{VP\_PCLK} / T_{TXBYTECLKHS}) - (4/NDL + (WC + 6)/NDL) = HFP_{DSI} + HBP_{DSI}$$
$$HFP_{DSI} + HBP_{DSI} = 170$$

dsi-e117

From **Equation 4** follows:

$$HFP_{DSI} = ((HFP_{DISP} \times bits\_per\_pixel)/NDL \times 8)) - (2/NDL)$$
$$HFP_{DSI} = 58$$
$$HBP_{DSI} = 170 - 58 = 112$$

dsi-e121

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10.3.4.6 DSI PHY

10.3.4.6.1 DSI PHY Overview

DSI_PHY_DSS_x is a DSI PHY with five unidirectional (HS) lane modules. This includes four data lane modules and one clock lane module. Each lane module has two data pads (DX, DY). These data pads are connected with a complementary lane module on the DSI receiver device using a point-to-point interconnect.

Lane modules support HS burst mode. Forward direction and reverse direction escape modes are also supported. Escape modes can be used for low-power data transmission, among other things.

The maximum data rate supported in HS mode is 1 Gbps for up to four data lanes. The lane module function and position are configurable; that is, any lane module can be chosen as a clock lane module, and the DX/DY data pad for each lane module can be configured as a DP or DN pin defined by the D-PHY specification.

DSI_PHY_DSS_x interacts with the higher layers of the DSI link through the PPI. DSI_PHY_DSS_x does not include a PLL; a high-frequency clock input is expected in HS mode (CLKIN2DDR). DSI_PHY_DSS_x also supports the SCP interface to set various configuration and control registers.

10.3.4.6.2 DSI PHY Software Reset

The clock domain using the TXBYTECLKHS byte clock from the DSI PHY has dedicated reset-done information in the DSI_COMPLEXIO_CFG1[29] RESET_DONE bit. The DSI_SYSCONFIG[1] SOFT_RESET bit is used to reset the byte clock power domain. A dummy read using the SCP interface to any DSI_PHY_DSS_x register is required after DSI_PHY_DSS_x reset to complete the reset of the DSI PHY.

10.3.4.6.3 DSI PHY Reset-Done Bits

The DSI PHY has several clock domains. The reset status for each clock domain is provided in the DSI_PHY_REGISTER5 register:

- DSI_PHY_REGISTER5[31] RESETDONETXBYTECLK bit: Reset done for the TXBYTECLK domain.
- DSI_PHY_REGISTER5[28:24] RESETDONETXCLKESCi bit field: Reset done for the TXCLKESC domain for lane i (where i = 0 to 4).
- DSI_PHY_REGISTER5[30] RESETDONESCPCLK bit: Reset done for the SCP clock domain. Software users must perform a dummy read on this bit to initiate the reset sequence of the SCP FSM. When the reset sequence completes, the RESETDONESCPCLK signal goes high, and software users can read again the DSI_PHY_REGISTER5[30] RESETDONESCPCLK bit to ensure that the value is now 1.

  NOTE: Software must not write in the DSI_PHY_DSS_x SCP registers before the DSI_PHY_REGISTER5[30] RESETDONESCPCLK bit is set to 1.

- DSI_PHY_REGISTER5[29] RESETDONEPWRCLK bit: Reset done for the PWR clock domain. The reset sequence of the PWR FSM is complete when the RESETDONEPWRCLK signal goes high.

10.3.4.6.4 DSI PHY Pad Configuration

The number of lanes is configurable through the DSI_COMPLEXIO_CFG1 register.

It is not allowed to change:

- The position on the fly (by modifying DATAx_POSITION, where x = 1 through 4, and CLOCK_POSITION fields)
- The P/N order (positive/negative order of the differential pair by modifying DATAy_POL, where y = 1 through 4, and CLOCK_POL)
- The number of active data lanes (by modifying the DSI_COMPLEXIO_CFG1[10:8] DATA2_POSITION, DSI_COMPLEXIO_CFG1[14:12] DATA3_POSITION, and DSI_COMPLEXIO_CFG1[18:16]

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DATA4_POSITION bit fields).

To add or remove the second, third, or fourth lanes, the DSI PHY must be in off mode.

The configuration of the DSI PHY (number of data lanes, position, differential order) must not be changed while the DSI_CLK_CTRL[20] LP_CLK_ENABLE bit is set to 1. For hardware to recognize a new configuration of the DSI PHY (done in the DSI_COMPLEXIO_CFG1 register), the following sequence must be followed. If the sequence is not followed, the DSI PHY configuration is undetermined.

1. Set the DSI_CTRL[0] IF_EN bit to 1.
2. Reset the DSI_CTRL[0] IF_EN bit to 0.
3. Set the DSI_CLK_CTRL[20] LP_CLK_ENABLE bit to 1.
4. Set the DSI_CTRL[0] IF_EN bit again to 1.

The minimum requirement for the number of lanes is one clock lane and one data lane. By default, the second, third, and fourth data lanes are not connected (the reset value of the DATAx_POSITION bit field is 0).

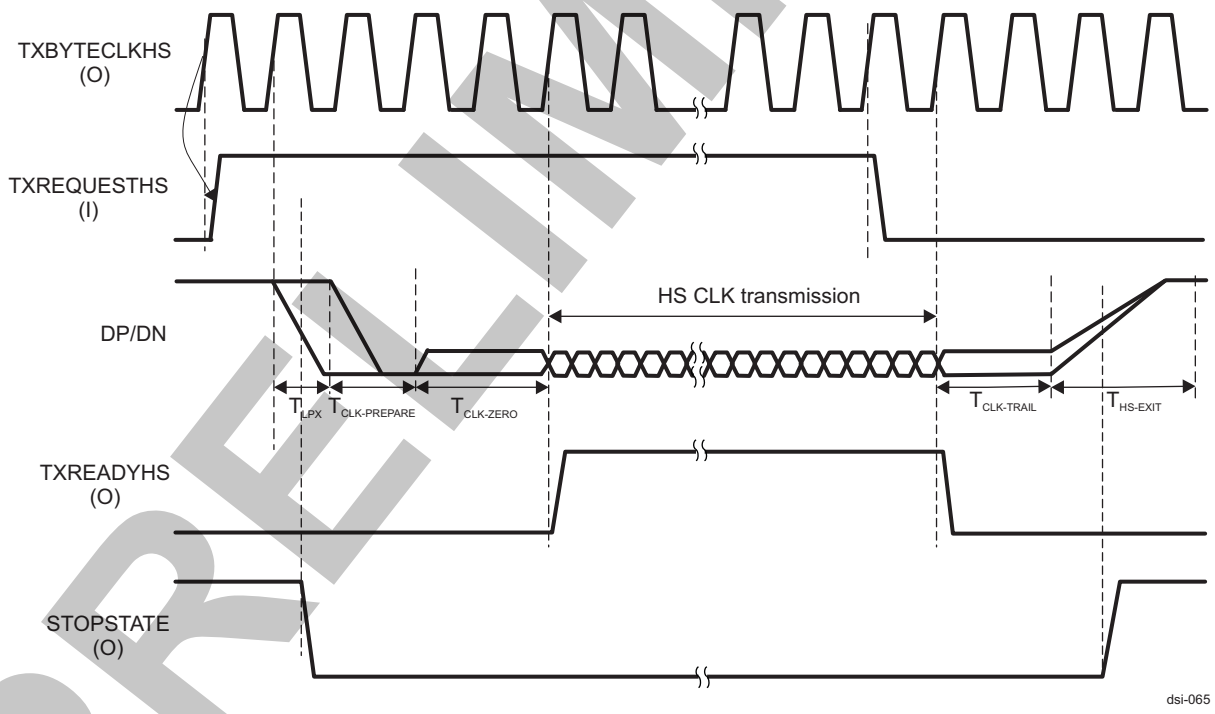
10.3.4.6.5 DSI PHY Display Timing Configuration

Depending on the CLKIN2DDR clock frequency settings programmed with the DSI PLL control module, software users must program accordingly the timing parameters in the DSI PHY registers.

10.3.4.6.5.1 DSI PHY HS Clock Transmission

Figure 10-153 shows an example of HS clock transmission.

Figure 10-153. DSI PHY HS Clock Transmission



TXBYTECLKHS is an output clock derived by dividing CLKIN2DDR by 8.

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NOTE: DSI_PHY_DSS_X can work with 2x DDR from PLL, compared to the 4x clock required in previous devices. The slower clock requirement saves power inside PLL and PHY. A duty cycle corrector (DCC) is used inside PHY to correct the duty cycle and allow use of 2x clock. 4x clock mode (legacy) is also supported. The default setting for the PHY is 2x clock. The 2x clock is only supported from data rate of 500Mbps to 1,255.5 Mbps. Below 500Mbps data rates, the DCC must be bypassed and PLL be programmed to 4x clock.

The TXBYTECLKHS clock is driven by DSI_PHY_DSS_x when:

- CLKIN2DDR is running and the DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN bit is set to 1.
- DSI_PHY_DSS_x is in ON power state (the DSI_COMPLEXIO_CFG1[28:27] PWR_CMD bit field is set to 1) and at least one lane is enabled.

To begin transmission, the protocol drives TXREQUESTHS high on a rising edge of TXBYTECLKHS. The PHY detects this signal on the next rising edge, after which it initiates the LP SoT procedure.

During an HS clock transmission, these parameters are defined in multiples of CLKIN2DDR and are programmed by the following bit fields:

- TLPX timing is programmed by DSI_PHY_REGISTER1[20:16] TLPXBY2.
- THS-PREPARE timing is programmed by DSI_PHY_REGISTER0[31:24] THSPREPARE.
- TCLK-ZERO timing is programmed by DSI_PHY_REGISTER1[7:0] TCLKZERO.

TCLK-ZERO is extended, if required, so that the entire LP SoT procedure lasts an integer number of TXBYTECLKHS cycles.

At the end of the SoT procedure, HS clock transmission begins. At the same time, TXREADYHS is made high.

To stop clock transmission, the protocol drives TXREQUESTHS low on a rising edge of TXBYTECLKHS. The DSI_PHY_DSS_x detects this change in TXREQUESTHS on the next edge and stops clock transmission. TXREADYHS is made low.

DSI_PHY_DSS_x then goes through the LP EoT procedure. The TCLK-TRAIL and THS-EXIT parameters are also multiples of CLKIN2DDR and are programmed by the following bit fields:

- TCLK-TRAIL timing is programmed by DSI_PHY_REGISTER1[15:8] TCLKTRAIL.
- THS-EXIT timing is programmed by DSI_PHY_REGISTER0[7:0] THSEXIT.

DSI_PHY_DSS_x completes the SoT and EoT procedures, once begun, regardless of any change in the PPI signals. If TXREQUESTHS goes low during the SoT procedure, the PHY starts the EoT procedure immediately after finishing the SoT procedure and no clock is transmitted.

STOPSTATE is high whenever the line is in LP-11 state, as determined by the outputs of the low-power receivers. This signal is not synchronized with TXBYTECLKHS.

The HS clock must be present for a period of time before (TCLK-PRE) and after (TCLK-POST) HS data transmission. The protocol must ensure that these timings are met by asserting and deasserting TXREQUESTHS appropriately.

The PHY ensures that the clock signal has a quadrature phase with respect to a toggling bit sequence on any data lane, and a rising edge in the center of the first transmitted bit of each data byte. These relations are not described in the timing diagram.

CLKIN2DDR can be shut off 300 ns after the clock lane goes to STOPSTATE. Alternatively, CLKIN2DDR can be shut down after TCLK-Trail + THS-Exit + 2 Txbyteclk periods after the TxRequestHS falling edge is received by DSI_PHY_DSS_x.

The DSI protocol engine must ensure that TXREQUESTESC, TXULPSCLK, and TURNREQUEST are low whenever TXREQUESTHS is asserted.

10.3.4.6.5.2 DSI PHY HS Data Transmission

Figure 10-154 shows an example of HS data transmission.

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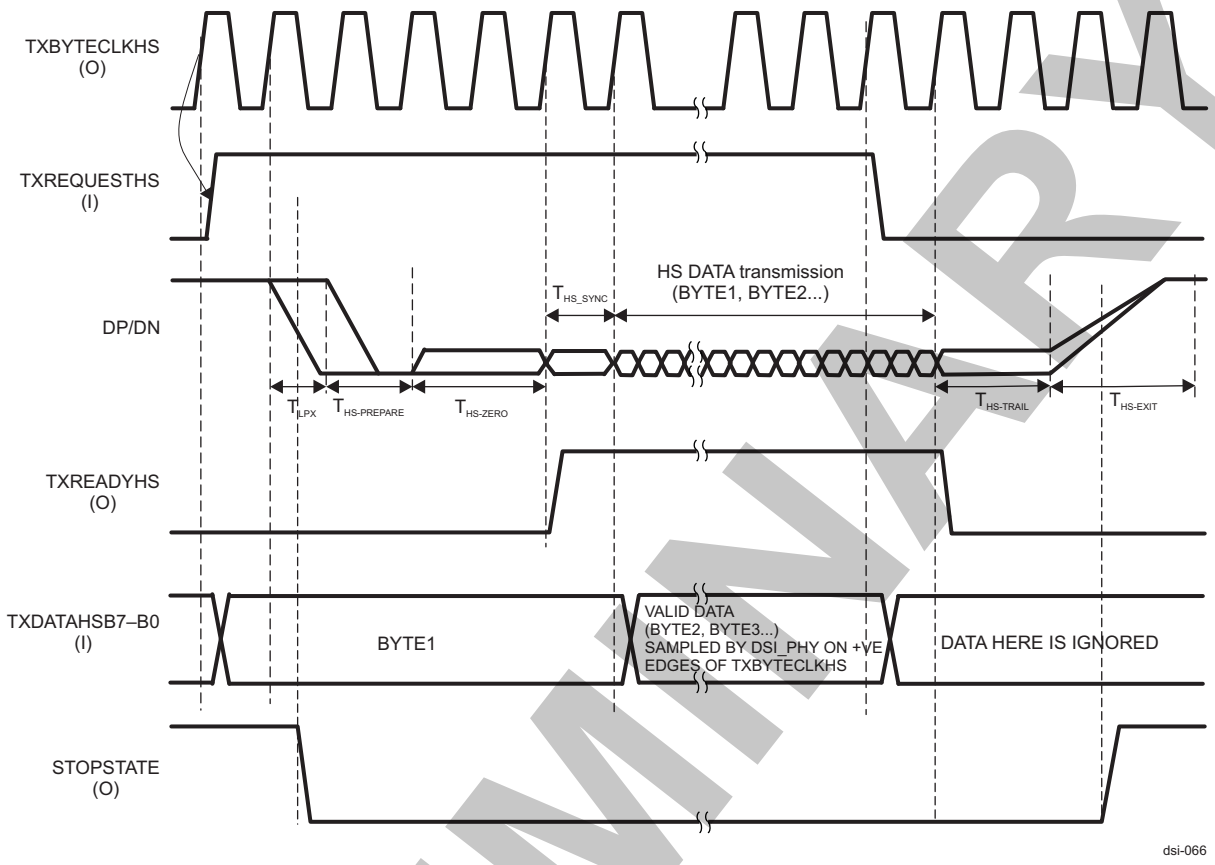
Figure 10-154. DSI PHY HS Data Transmission



To begin transmission, the protocol drives TXDATAHS with the first byte of data on a rising edge of TXBYTECLKHS. It also makes TXREQUESTHS high on the same rising edge. The PHY detects TXREQUESTHS going high on the next rising edge of TXBYTECLKHS, following which it initiates the LP SoT procedure.

During an HS data transmission, these timings are multiples of CLKIN2DDR and are programmed by the following bit fields:

- TLPX timing is programmed by DSI_PHY_REGISTER1[20:16] TLPXBY2.
- THS-PREPARE + THS-ZERO timing is programmed by DSI_PHY_REGISTER0[23:16] THSPRPR_THSZERO.

THS-ZERO is extended, if required, so that the entire LP SoT procedure lasts an integer number of TXBYTECLKHS cycles. THS-SYNC corresponds to the length of the sync pattern (8 HS bits), and can be configured through the DSI_PHY_REGISTER2[31:24] HSSYNCPATTERN bit field.

Toward the end of the SoT procedure, the PHY makes TXREADYHS high on a positive edge of TXBYTECLKHS and then starts accepting data from TXDATAHS from the next positive edge onward. The protocol is expected to provide (new) valid data on TXDATAHS on every positive edge of TXBYTECLKHS if TXREADYHS is high.

At the end of the SoT procedure, HS data transmission begins. HS data transmission happens LSB first.

To stop data transmission, the protocol drives TXREQUESTHS low on a rising edge of TXBYTECLKHS. The PHY detects this change in TXREQUESTHS on the next edge and stops data transmission. TXREADYHS is made low and data on TXDATAHS, from that point, is ignored.

The PHY then goes through the LP EoT procedure. THS-TRAIL and THS-EXIT are also multiples of CLKIN2DDR and are programmed by the following bit fields:

- THS-TRAIL timing is programmed by DSI_PHY_REGISTER0[15:8] THSTRAIL.
- THS-EXIT timing is programmed by DSI_PHY_REGISTER0[7:0] THSEXIT.

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The PHY completes the SoT and EoT procedures, once begun, regardless of any change in PPI signals. If TXREQUESTHS goes low during the SoT procedure, the PHY starts the EoT procedure immediately after finishing the SoT procedure and no data is transmitted.

STOPSTATE is high whenever the line is in LP-11 state, as determined by the outputs of the low-power receivers. This signal is not synchronized with TXBYTECLKHS.

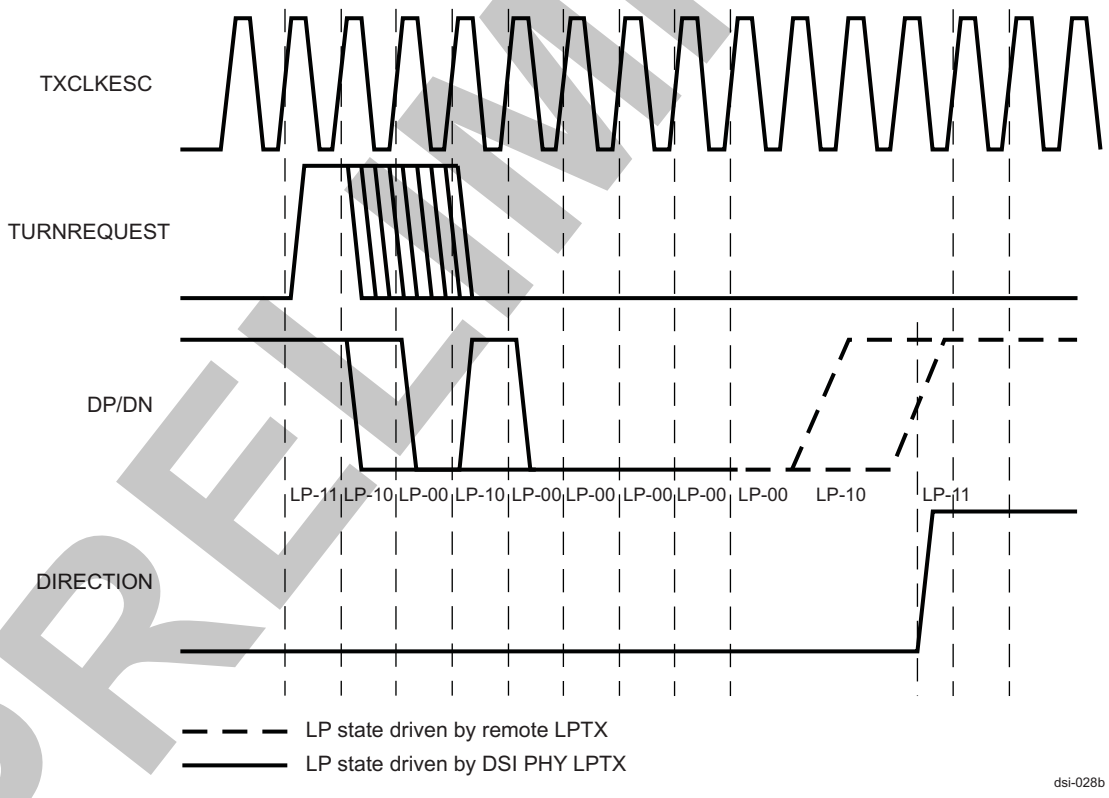
The protocol must ensure that TXREQUESTESC, TXULPSCLK, and TURNREQUEST are low whenever TXREQUESTHS is asserted.

10.3.4.6.5.3 DSI PHY Turnaround Request in Transmit Mode

When the DSI PHY is in transmit mode, the DSI protocol engine can request a turnaround by making the TurnRequest signal high for at least one clock cycle of TxClkEsc (see Section 10.3.4.4.7.3, *TurnRequest FSM*).

The DSI PHY transmits the turnaround request pattern (LP 11-10-00-10-00-00-00-00) (see Figure 10-155). The number of 00 states at the end of the pattern is defined by the T_{TA-GO} timing parameter and is programmable through the DSI_PHY_REGISTER1[31:29] REG_TTAGO bit field, in number of TxClkEsc clocks. Following the transmission of the pattern, the DSI PHY disables its LP transmitters and waits for an acknowledgment from the remote device. The remote device detects the turnaround request and acknowledges it by driving LP-10, followed by the STOP state. When this acknowledgment is received (BTA_IRQ is asserted, as described in Section 10.3.4.4.8, *DSI Bus Turnaround*), the DSI PHY switches to receive mode and indicates the completion of the turnaround procedure by changing the direction (BTA_EN = 0).

Figure 10-155. DSI PHY Turnaround Request in Transmit Mode



The DSI protocol engine must not stop TxClkEsc after the turnaround process completes (the DSI_CLK_CTRL[20] LP_CLK_ENABLE bit must be kept at 1), because TxClkEsc is also used in handling a turnaround request transmitted by a remote slave device (see Section 10.3.4.6.5.4, *Turnaround Request in Receive Mode*).

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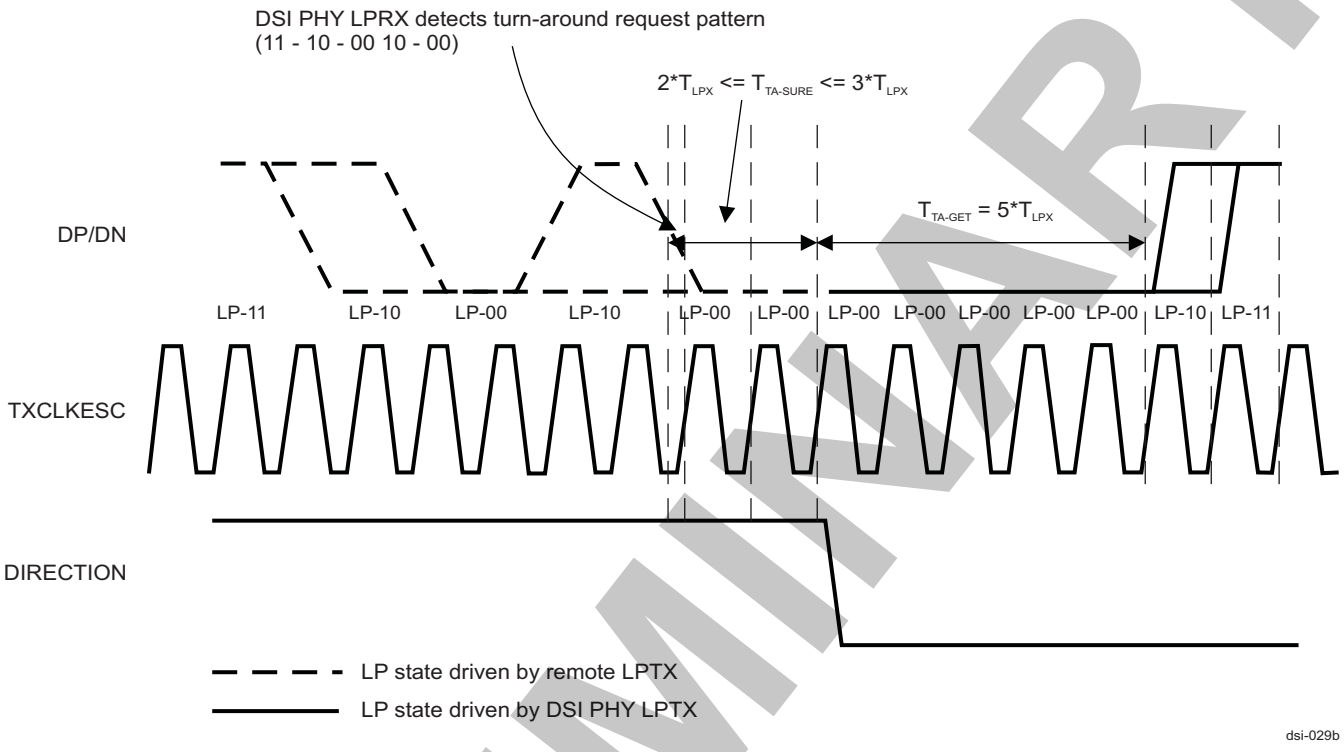
10.3.4.6.5.4 DSI PHY Turnaround Request in Receive Mode

When DSI PHY is in receive mode, an LP pattern of 11-10-00-10-00 on DP/DN lines indicates a turnaround request from the remote device (see Figure 10-156).

Figure 10-156. DSI PHY Turnaround Request in Receive Mode



If the line stays in LP-00 for a time $T_{TA-SURE}$, the DSI PHY accepts the turnaround request, changes the direction, transmits LP-00 for a time T_{TA-GET}, and then transmits the acknowledgment pattern LP-10, followed by the STOP state.

This completes the turnaround procedure. The $T_{TA-SURE}$ and T_{TA-GET} timing parameters are programmable through DSI_PHY_REGISTER1 in number of TxClkEsc clocks:

- $T_{TA-SURE}$ can be configured in the [28:27] REG_TTASURE bit field.
- T_{TA-GET} can be configured in the [26:24] REG_TTAGET bit field.

10.3.4.6.5.5 DSI PHY Transmission and Reception

The timings of the following sequences defined in the DSI_PHY_DSS_x protocol cannot be programed by the user:

- Low-power data transmission
- Escape mode trigger command transmission
- ULPS command transmission on data lanes
- ULPS transmission on clock lane
- Low-power data in receive mode
- Low-power trigger in receive mode
- ULPS command on clock lane in receive mode
- ULPS command on data lane in receive mode

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10.3.4.6.6 DSI PHY Power Management

Power management of the DSI_PHY_DSS_x analog circuitry is done through the internal power FSM, which is controlled by the subsystem. The control interface is a basic command and acknowledge protocol. The subsystem is the master of the interface. There is a dedicated command pin for each power state of DSI_PHY_DSS_x and a common acknowledge pin. The subsystem sends the power command and clock. The internal FSM does the sequencing and control generation of internal power domains. It then asserts the acknowledge, which signals the completion of the power state transition. The internal power control FSM is powered by a constant power supply.

The main features of the power control interface are:

- One dedicated command line per power state
- Only one command line can be asserted at a time.
- One acknowledge signal common to all command lines
- The command line cannot be cleared unless the acknowledge has been returned.
- All the command lines and the acknowledge signal must be cleared before triggering a new command.

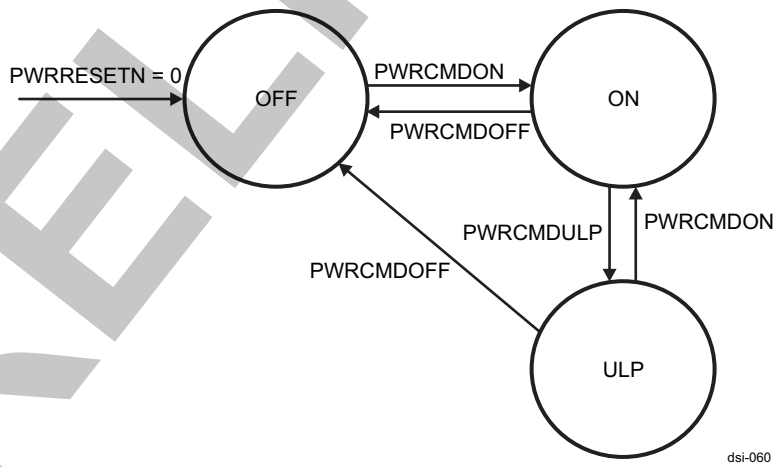
DSI_PHY_DSS_x supports three power states:

- OFF/GPIO mode (OFF): The entire analog circuit is powered down. Internal LDO is off. All analog circuitry on 1.8-V supply is powered down. The ULPS exit detection circuit power switch is off. DSI_PHY_DSS_x takes leakage level current.
- ON: Complete analog circuit is powered on and functional. LDO is on. (DSI_PHY_DSS_x calibrates every time the module enters power on state.)
- ULPS: Only the ULPS exit-detection circuit power switch in DSI_PHY_DSS_x mode is on. All the other analog circuitry is switched off. LDO is off.

NOTE: ULPS must be entered only when all used lane modules go into ULPS. The PHY power state must be returned to ON power state when any one of the used modules goes out of ULPS. No PPI signal except TXULPSEXIT must be toggled when in this power state.

Figure 10-157 shows the power states of the DSI PHY

Figure 10-157. DSI PHY Power State Diagram



10.3.4.6.6.1 DSI PHY Power Saving in DSIPHY From PLL Clock

DSIPHY can work with the 2X clock from PLL. A duty cycle corrector (DCC) is used inside DSIPHY to correct the duty cycle and allow the use of the 2X clock. Compared to legacy devices, a slower clock saves power in the PLL. Therefore, the default setting for DSIPHY is to use the 2X clock. The 2X clock is supported only from a data rate of 500 Mbps to 1,255.5 Mbps. For data rates less than 500 Mbps, the DCC must be bypassed and PLL must be programmed to the 4X clock. The DSI_PHY_DSS_x_REGISTER1 register setting for this is explained in Table 10-546.

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Table 10-546. DSI PHY PLL Clock Select Register Control

DSI_PHY_DSS_x_REGISTER1 Bits	Functionality	Comment
REG_DCCEN	Enable DCC.	For higher data rates, DCC must be enabled. The default value is 1 or DCC is enabled.
REG_CLKINP_SEL	Select DCC or divby2 output.	The default value is 0 or DCC output is selected.
REG_CLKPINP_DIVBY2EN	Enable divby2.	For lower data rates, 500 Mbps and below must be used.

10.3.4.6.7 DSI PHY Error Handling

A dedicated register for the DSI PHY (DSI_COMPLEXIO_IRQSTATUS) indicates the state of each error provided by the DSI PHY error signals. The DSI_PHY_DSS_x reports the following errors:

- DSI_COMPLEXIO_IRQSTATUS[9:5] ERRESCi_IRQ: ERRESC is asserted if an unrecognized Escape entry command is received. This remains high until the next change in the line state.
- DSI_COMPLEXIO_IRQSTATUS[4:0] ERRSYNCESCi_IRQ: If the number of bits received during a low-power data transmission is not a multiple of 8 when the transmission ends, ERRSYNCESC is made high and remains high until the next change in the line state.
- DSI_COMPLEXIO_IRQSTATUS[14:10] ERRCONTROLi_IRQ: ERRCONTROL is asserted if an incorrect line state sequence is detected. For example, if a turnaround request or escape mode request is immediately followed by a STOP state instead of the required bridge state, this signal is asserted and remains asserted until the next change in the line state.
- DSI_COMPLEXIO_IRQSTATUS ERRCONTENTIONLP0_i_IRQ: ERRCONTENTION0LPDX and ERRCONTENTION0LPDY are asserted when the lane module detects a contention situation on lines DX and DY, respectively, while trying to drive the lines low. Contention is detected only if it lasts at least 50 ns.
- DSI_COMPLEXIO_IRQSTATUS ERRCONTENTIONLP1_i_IRQ: ERRCONTENTION1LPDX and ERRCONTENTION1LPDY are asserted when the lane module detects a contention situation on lines DX and DY, respectively, while trying to drive the lines high. Contention is detected only if it lasts at least 50 ns.

The ULPSACTIVENOT signal goes low, which indicates to the protocol that the PHY has entered ULPS. When all the ULPSActiveNot signals are low, the DSI_COMPLEXIO_IRQSTATUS[30] ULPSACTIVENOT_ALL0_IRQ event is generated. When all the ULPSActiveNot signals are high, the DSI_COMPLEXIO_IRQSTATUS[31] ULPSACTIVENOT_ALL1_IRQ event is generated.

When any of the events defined in the DSI_COMPLEXIO_IRQSTATUS register occur, the DSI_IRQSTATUS[10] COMPLEXIO_ERR_IRQ bit is set to 1 at the DSI protocol engine level.

Table 10-547 lists the DSI PHY interrupt events.

Table 10-547. DSI PHY Interrupts

IRQ Name	Description
ULPSActiveNot_ALL0_IRQ	All ULPSActiveNOT signals are 0.
ULPSActiveNot_ALL1_IRQ	All ULPSActiveNOT signals corresponding to the lanes with TXULPSExit being high are high.
STATEULPM5_IRQ	Fifth lane n ULPS
STATEULPM4_IRQ	Fourth lane in ULPS
STATEULPM3_IRQ	Third lane in ULPS
STATEULPM2_IRQ	Second lane in ULPS
STATEULPM1_IRQ	First lane in ULPS
ERRCONTROL5_IRQ	Control error for fifth lane
ERRCONTROL4_IRQ	Control error for fourth lane
ERRCONTROL3_IRQ	Control error for third lane
ERRCONTROL2_IRQ	Control error for second lane

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Table 10-547. DSI PHY Interrupts (continued)

IRQ Name	Description
ERRCONTROL1_IRQ	Control error for first lane
ERRESC5_IRQ	Escape entry error for fifth lane (edge trigger interrupt)
ERRESC4_IRQ	Escape entry error for fourth lane (edge trigger interrupt)
ERRESC3_IRQ	Escape entry error for third lane (edge trigger interrupt)
ERRESC2_IRQ	Escape entry error for second lane (edge trigger interrupt)
ERRESC1_IRQ	Escape entry error for first lane (edge trigger interrupt)
ERRCONTENTIONLP1_1_IRQ	Contention LP1 error for first lane
ERRCONTENTIONLP0_1_IRQ	Contention LP0 error for first lane
ERRCONTENTIONLP1_2_IRQ	Contention LP1 error for second lane
ERRCONTENTIONLP0_2_IRQ	Contention LP0 error for second lane
ERRCONTENTIONLP1_3_IRQ	Contention LP1 error for third lane
ERRCONTENTIONLP0_3_IRQ	Contention LP0 error for third lane
ERRCONTENTIONLP1_4_IRQ	Contention LP1 error for fourth lane
ERRCONTENTIONLP0_4_IRQ	Contention LP0 error for fourth lane
ERRCONTENTIONLP1_5_IRQ	Contention LP1 error for fifth lane
ERRCONTENTIONLP0_5_IRQ	Contention LP0 error for fifth lane
ERRSYNCESC5_IRQ	Low-power data transmission synchronization error for fifth lane
ERRSYNCESC4_IRQ	Low-power data transmission synchronization error for fourth lane
ERRSYNCESC3_IRQ	Low-power data transmission synchronization error for third lane
ERRSYNCESC2_IRQ	Low-power data transmission synchronization error for second lane
ERRSYNCESC1_IRQ	Low-power data transmission synchronization error for first lane

Software must take appropriate action when receiving the interrupt indicating the error from the DSI PHY. The action can be:

- Reset the DSI protocol engine module.
- Reset the peripheral through the reset trigger or directly drive the hardware reset pin of the display module.
- Ignore the error.

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10.3.5 DSI Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the DSI module.

10.3.5.1 DSI Global Initialization

10.3.5.1.1 DSI Surrounding Modules Global Initialization

This section describes the requirements to initialize the surrounding modules when the DSI module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DSI. For more information, see Section 10.3.3, *DSI Integration*, and Section 10.3.2, *DSI Environment*.

Table 10-548 describes the global initialization of the surrounding modules.

Table 10-548. DSI Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	DSI module interface and functional clocks must be enabled. The module power management (idle and sleep modes) must be configured. For more information, see , *Module-Level Clock Management*, in *Chapter 3, Power, Reset, and Clock Management*.
MPU INTC	MPU interrupt controller (INTC) configuration must be done to enable interrupts from the DSI module. For more information about the module configuration, see , *Interrupt Controllers Overview*, in Chapter 17, *Interrupt Controllers*.
DSP INTC	DSP INTC configuration must be done to enable interrupts from the DSI module. For more information about the module configuration, see , *DSP Subsystem Overview*, in *Chapter 5, DSP Subsystem*.
DMA_SYSTEM	DMA configuration must be done to enable DSI module DMA channel requests. For more information about the configuration, see , *DMA_SYSTEM Module Overview*, in *Chapter 16, System DMA*.
L3_MAIN interconnect	For information about the interconnect configuration, see , *L3 Interconnect*, in *Chapter 14, Interconnects*.

10.3.5.1.2 DSI Global Initialization

10.3.5.1.2.1 DSI Main Sequence – DSI Global Initialization

This procedure initializes the DSI after a power on or software reset.

Table 10-549 summarizes the DSI global initialization.

Table 10-549. DSI Global Initialization

Steps	Registers	Value
Reset IRQ status.	DSI_IRQSTATUS[31:0]	0x0
Set clock activity.	DSI_SYSCONFIG[9:8] CLOCKACTIVITY	x
Configure power management.	DSI_SYSCONFIG[4:3] SIDLEMODE	x
Reset DSI protocol engine.	DSI_SYSCONFIG[1] SOFT_RESET	0x1
Wait until five reads of reset status?	Software test condition	
Read reset status.	DSI_SYSSTATUS[0] RESET_DONE	
IF: Is reset ongoing?	DSI_SYSSTATUS[0] RESET_DONE	= 0x0
Error occurred during reset stage		
ENDIF		

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10.3.5.2 DSI Operational Modes Configuration

10.3.5.2.1 DSI Video Mode Using the DISPC Video Port

10.3.5.2.1.1 DSI Main Sequence – DSI PLL Setup

Table 10-550 lists the steps required to configure the DSI PLL.

Table 10-550. DSI PLL Configuration Registers

Steps	Registers	Value
Turn on/off the PLL and HSDIVIDER.	DSI_CLK_CTRL[31:30] PLL_PWR_CMD	x
Wait until the status of the PLL is set (value according to the previous step)?	DSI_CLK_CTRL[29:28] PLL_PWR_STATUS	= x
Set the divider value for DSI protocol engine clock source M5REG.	DSI_PLL_CONFIGURATION1[30:26] M5_CLOCK_DIV	x
Set the divider value for clock source M4REG.	DSI_PLL_CONFIGURATION1[25:21] M4_CLOCK_DIV	x
Set the value for M divider for the PLL.	DSI_PLL_CONFIGURATION1[20:9] DSI_PLL_REGM	x
Set the value for N divider for the PLL.	DSI_PLL_CONFIGURATION1[8:1] DSI_PLL_REGN	x
Enable/disable DSI protocol engine clock divider.	DSI_PLL_CONFIGURATION2[18] M5_CLOCK_EN	x
Enable/disable M4 clock source divider.	DSI_PLL_CONFIGURATION2[16] M4_CLOCK_EN	x
Enable/disable DSI PHY clock.	DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN	x
Enable/disable PLL reference clock.	DSI_PLL_CONFIGURATION2[13] PLL_REFEN	x
Set PLL automatic update mode.	DSI_PLL_CONTROL[0] PLL_AUTOMODE	x
Request PLL locking sequence.	DSI_PLL_GO[0] PLL_GO	0x1
Read until PLL_GO bit = 0?	DSI_PLL_GO[0] PLL_GO	= 0x0
Wait until PLL is locked?	DSI_PLL_STATUS[1] PLL_LOCK	= 0x1
Set the ratio for the LP clock.	DSI_CLK_CTRL[12:0] LP_CLK_DIVISOR	x
Enable/disable DSS_L3_MAIN_ICLK clock gating to DSI_PHY_DSS_x and PLL module.	DSI_CLK_CTRL[14] CIO_CLK_ICG	x
Enable/disable the automatic assertion/deassertion of DSIStopClk.	DSI_CLK_CTRL[18] HS_AUTO_STOP_ENABLE	x
Configure the DSI functional clock synchronization and clock speed.	DSI_CLK_CTRL[21] LP_RX_SYNCHRO_ENABLE	x
Turn on/off PLL and HSDIVIDER.	DSI_CLK_CTRL[31:30] PLL_PWR_CMD	x

10.3.5.2.1.2 DSI Main Sequence – Set Up DSI Protocol Engine

10.3.5.2.1.2.1 DSI Set Up DSI Control Registers

Table 10-551 lists the steps to set up the DSI control registers. Table 10-552 lists the steps to set up the DSI PHY registers.

Table 10-551. DSI Control Registers

Steps	Registers	Value
Enable the interrupt event for lost synchronization with the video port.	DSI_IRQENABLE[18] SYNC_LOST_IRQ_EN	0x1
Enable interrupt event for sent packet on desired VC.	DSI_VC_IRQENABLE_i[2] PACKET_SENT_IRQ_EN	x
Enable HSYNC END pulse detection (short packet generation).	DSI_CTRL[17] VP_HSYNC_START	0x1
Enable VSYNC START pulse detection (short packet generation).	DSI_CTRL[15] VP_VSYNC_START	0x1
Select trigger reset mode.	DSI_CTRL[14] TRIGGER_RESET_MODE	x

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Table 10-551. DSI Control Registers (continued)

Steps	Registers	Value
Set the number of line buffers.	DSI_CTRL[13:12] LINE_BUFFER	x
Set video port HSYNC signal polarity.	DSI_CTRL[10] VP_HSYNC_POL	x
Set video port VSYNC signal polarity.	DSI_CTRL[11] VP_VSYNC_POL	x
Set video port data enable signal polarity.	DSI_CTRL[9] VP_DE_POL	x
Set the size of the video port data bus.	DSI_CTRL[7:6] VP_DATA_BUS_WIDTH	x
Set the arbitration scheme for granting the VC pending ready requests in the TX FIFO.	DSI_CTRL[3] TX_FIFO_ARBITRATION	x
Enable/disable the ECC check for the received header.	DSI_CTRL[2] ECC_RX_EN	0x1

Table 10-552. DSI PHY Registers

Steps	Registers	Value
Configure synchronized update on the shadow register.	DSI_COMPLEXIO_CFG1[30] GOBIT	x
Set the DSI PHY power state.	DSI_COMPLEXIO_CFG1[28:27] PWR_CMD	x
Set the position of the first data lane.	DSI_COMPLEXIO_CFG1[6:4] DATA1_POSITION	x
Set the position of the clock lane.	DSI_COMPLEXIO_CFG1[2:0] CLOCK_POSITION	x
Clear the interrupt status register.	DSI_COMPLEXIO_IRQSTATUS	0xFFFF FFFF
Disable all interrupt events.	DSI_COMPLEXIO_IRQENABLE	0x0
Enable the DSI protocol engine.	DSI_CTRL[0] IF_EN	0x1
Disable the DSI protocol engine.	DSI_CTRL[0] IF_EN	0x0
Wait until the interface is disabled?	DSI_CTRL[0] IF_EN	= 0x0
Enable the low-power clock (TXCLKESC).	DSI_CLK_CTRL[20] LP_CLK_ENABLE	0x1
Wait until reset is done?	DSI_COMPLEXIO_CFG1[29] RESET_DONE	= 0x1
Check if power control is ON?	DSI_COMPLEXIO_CFG1[26:25] PWR_STATUS	= 0x1
Wait until internal module reset is complete?	DSI_SYSSTATUS[0] RESETDONE	= 0x1

10.3.5.2.1.2.2 DSI Configure DSI Timing and VCs

Table 10-553 lists the steps to configure DSI timing and the VCs.

Table 10-553. DSI Timing Registers

Steps	Registers	Value
Determine the number of DSI_CLK clock cycles for the STOP-STATE counter.	DSI_TIMING1[12:0] STOP_STATE_COUNTER_IO	0x-
Determine the number of BYTE_CLK clock cycles for the HS RX timer.	DSI_TIMING2[28:16] HS_TX_TO_COUNTER	0x-
Enable/disable the multiplication factor of 16 for the number of BYTE_CLK clock cycles for the HS TX timer.	DSI_TIMING2[29] HS_TX_TO_X16	0x-
Determine the number of DSI_CLK clock cycles for the LP RX timer.	DSI_TIMING2[12:0] LP_RX_TO_COUNTER	0x-
Enable/disable the multiplication factor of 16 for the number of DSI_CLK clock cycles for the LP RX timer.	DSI_TIMING2[14] LP_RX_TO_X16	0x-
Set the horizontal sync active period.	DSI_VM_TIMING1[31:24] HSA	0x-
Set the horizontal front porch.	DSI_VM_TIMING1[23:12] HFP	0x-
Set the horizontal back porch.	DSI_VM_TIMING1[11:0] HBP	0x-
Set the number of BYTE clock cycles for the sync window.	DSI_VM_TIMING2[27:24] WINDOW_SYNC	0x-

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Table 10-553. DSI Timing Registers (continued)

Steps	Registers	Value
Set the vertical sync active period.	DSI_VM_TIMING2[23:16] VSA[(1)]	0x-
Set the vertical front porch.	DSI_VM_TIMING2[15:8] VFP	0x-
Set the vertical back porch.	DSI_VM_TIMING2[7:0] VBP	0x-
Set the line length.	DSI_VM_TIMING3[31:16] TL	0x-
Set the number of active lines.	DSI_VM_TIMING3[15:0] VACT	0x-
Set the number of TXBYTECLKHS clock cycles for entering HS mode.	DSI_VM_TIMING7[31:16] ENTER_HS_MODE_LATENCY	0x-
Set the number of TXBYTECLKHS clock cycles for exiting HS mode.	DSI_VM_TIMING7[15:0] EXIT_HS_MODE_LATENCY	0x-
Set the number of TXBYTECLKHS clock cycles between the start of the DDR clock and the assertion of the data request signal.	DSI_CLK_TIMING[15:8] DDR_CLK_PRE	0x-
Set the number of TXBYTECLKHS clock cycles after the data request signal is deasserted and the DDR clock is stopped.	DSI_CLK_TIMING[7:0] DDR_CLK_POST	0x-
Configure the RX FIFO DMA request.	DSI_VC_CTRL_i[29:27] DMA_RX_REQ_NB	0x-
Configure the TX FIFO DMA request.	DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB	0x-
Enable/disable the ECC generation for the transmit header.	DSI_VC_CTRL_i[8] ECC_TX_EN	0x-
Enable/disable the checksum generation for the transmit payload.	DSI_VC_CTRL_i[7] CS_TX_EN	0x-
Select video mode.	DSI_VC_CTRL_i[4] MODE	0x-

(1) In DSI video mode, if the VSA bit field in DSI_VM_TIMING2 is set to 0x0, no vertical synchronization packet will be sent, even if VP_VSYNC_START is set to 0x1 in DSI_CTRL.

10.3.5.2.1.3 DSI Main Sequence – Configure DSI_PHY_DSS_x

Table 10-554 summarizes the timing in the functions of DDR_CLK_P. For more information about the timing calculation, see Section 10.3.4.4.4, *DSI Clock Requirements*.

Table 10-554. DSI Calculate DSI_PHY_DSS_x Timing

Steps	Registers	Value
Settings of the DSI protocol timing. For a complete description of the timing specifications, see Section 10.3.4.4.4, *DSI Clock Requirements*.	DSI_PHY_REGISTER0[31:24] REG_THSPREPARE	ceil(70 ns/DDR clock period) + 2
	DSI_PHY_REGISTER0[23:16] REG_PRPR_THSZERO	ceil(175 ns/DDR clock period) + 2
	DSI_PHY_REGISTER0[7:0] REG_THSEXIT	ceil(145 ns/DDR clock period)
	DSI_PHY_REGISTER0[15:8] REG_THSTRAIL	ceil(60 ns/DDR clock period) + 5
	DSI_PHY_REGISTER2[7:0] REG_TCLKPREPARE	ceil(65 ns/DDR clock period)
	DSI_PHY_REGISTER1[7:0] REG_TCLKZERO	ceil(265 ns/DDR clock period)
	DSI_PHY_REGISTER1[15:8] REG_TCLKTRAIL	ceil(60 ns/DDR clock period) + 2
	DSI_PHY_REGISTER1[20:16] REG_TLPXBY2	ceil(25 ns/DDR clock period)

10.3.5.2.1.4 DSI Main Sequence – Drive STOP State

Table 10-555 lists the steps to drive STOP state.

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Table 10-555. DSI Drive STOP State

Steps	Registers	Value
Force TX stop mode.	DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO	0x1
Wait until FORCE_TX_STOP_MODE_IO = 0?	DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO	= 0x0

10.3.5.2.1.5 DSI Main Sequence – Enable Video Mode

Table 10-555 lists the steps to enable video mode.

Table 10-556. DSI Enable Video Mode

Steps	Registers	Value
Set up long packet header.	DSI_VC_LONG_PACKET_HEADER_i	0x-
Enable desired VC.	DSI_VC_CTRL_i[1] VC_EN	0x1
Enable DSI module.	DSI_CTRL[0] IF_EN	0x1
Wait until IF_EN = 1?	DSI_CTRL[0] IF_EN	= 0x1

10.3.5.2.2 DSI Command Mode Using the DISPC Video Port

This section explains the basic programming model of command mode using the DISPC video port.

10.3.5.2.2.1 DSI Main Sequence – Configure DSI PLL

Table 10-557 lists the steps required to configure the DSI PLL.

Table 10-557. DSI Configure DSI PLL

Steps	Register/Bit Field/Programming	Value
Set PLL and HSDIVIDER to ON state.	DSI_CLK_CTRL[31:30] PLL_PWR_CMD	0x2
Wait until PLL and HSDIVIDER are enabled?	DSI_CLK_CTRL[29:28] PLL_PWR_STATUS	= 0x2
Set the M5REG value.	DSI_PLL_CONFIGURATION1[30:26] M5_CLK_DIV	x
Set the M4REG value.	DSI_PLL_CONFIGURATION1[25:21] M4_CLOCK_DIV	x
Set the REGN value.	DSI_PLL_CONFIGURATION1[8:1] PLL_REGN	x
Set the REGM value.	DSI_PLL_CONFIGURATION1[20:9] PLL_REGM	x
Enable/disable PLL reference clock control.	DSI_PLL_CONFIGURATION2[13] PLL_REFEN	x
Enable/disable CLKIN2DDR control.	DSI_PLL_CONFIGURATION2[14] PHY_CLKINEN	x
Enable/disable DSS clock divider.	DSI_PLL_CONFIGURATION2[16] M4_CLOCK_EN	x
Enable/disable DSI protocol engine clock divider.	DSI_PLL_CONFIGURATION2[18] M5_CLOCK_EN	x
Configure synchronization of configuration update with DISPC_UPDATE_SYNC.	DSI_PLL_CONTROL[0] PLL_AUTOMODE	x
Start PLL locking sequence.	DSI_PLL_GO[0] PLL_GO	0x1
Wait until there is no pending action?	DSI_PLL_GO[0] PLL_GO	= 0x0
Check whether PLL is locked?	DSI_PLL_STATUS[1] PLL_LOCK	= 0x1
Set the LP mode clock ratio.	DSI_CLK_CTRL[12:0] LP_CLK_DIVISOR	x
Configure DSS_L3_MAIN_ICLK clock to the DSI PHY.	DSI_CLK_CTRL[14] CIO_CLK_ICG	x
Enable/disable the automatic assertion/deassertion of the DSIStopClk signal.	DSI_CLK_CTRL[18] HS_AUTO_STOP_ENABLE	x
Define the DSI functional clock value and synchronization.	DSI_CLK_CTRL[21] LP_RX_SYNCHRO_ENABLE	x
Turn on PLL and HSDIVIDER.	DSI_CLK_CTRL[31:30] PLL_PWR_CMD	0x2

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10.3.5.2.2.2 DSI Main Sequence – Switch to DSI PLL Clock Source

Table 10-558 lists the steps to switch the DSI and DISPC module clocks to DSI PLL clock source.

Table 10-558. DSI witch to DSI PLL Clock Source

Steps	Reference	Value
Switch DISPC clock to PLL1_CLK1.	For more information, see Display Subsystem Integration, in *Display Subsystem*.	
Switch DSI clock to DPLL_DSI1_A_CLK2.	For more information, see Display Subsystem Integration, in *Display Subsystem*.	

10.3.5.2.2.3 DSI Main Sequence – Configure DSI Protocol Engine

10.3.5.2.2.3.1 DSI Set Up DSI Control Registers

Table 10-559 lists the steps required to set up the DSI control registers. Table 10-560 lists the steps to set up the DSI PHY registers.

Table 10-559. DSI Control Registers

Steps	Register/Bit Field/Programming	Value
Enable IRQ for lost synchronization with video port.	DSI_IRQENABLE[18] SYNC_LOST_IRQ_EN	0x1
Enable IRQ to indicate that packet has been sent on desired VC.	DSI_VC_IRQENABLE_i[2] PACKET_SENT_IRQ_EN	0x1
Set the trigger reset mode.	DSI_CTRL[14] TRIGGER_RESET_MODE	x
Configure the number of active line buffers.	DSI_CTRL[13:12] LINE_BUFFER	x
Set the size of the video port data bus.	DSI_CTRL[7:6] VP_DATA_BUS_WIDTH	x
Define the ratio between VP_CLK and VP_PCLK.	DSI_CTRL[4] VP_CLK_RATIO	x
Set the arbitration scheme for granting the VC pending ready requests in the TX FIFO.	DSI_CTRL[3] TX_FIFO_ARBITRATION	x
Enable/disable the ECC check for the received header.	DSI_CTRL[2] ECC_RX_EN	x

Table 10-560. DSI PHY Registers

Steps	Register/Bit Field/Programming	Value
Determine the position of the clock lane.	DSI_COMPLEXIO_CFG1[2:0] CLOCK_POSITION	x
Set the position of data lane 1.	DSI_COMPLEXIO_CFG1[6:4] DATA1_POSITION	x
Configure the power state of the DSI PHY.	DSI_COMPLEXIO_CFG1[28:27] PWR_CMD	x
Enable the synchronization of the shadow registers with DISPC_UPDATE_SYNC.	DSI_COMPLEXIO_CFG1[30] GOBIT	0x1
Clear the DSI PHY IRQ status.	DSI_COMPLEXIO_IRQSTATUS	0xFFFF FFFF
Disable all DSI PHY IRQ events.	DSI_COMPLEXIO_IRQENABLE	0x0
Enable the DSI protocol engine interface.	DSI_CTRL[0] IF_EN	0x1
Disable the DSI protocol engine interface.	DSI_CTRL[0] IF_EN	0x0
Wait until interface is disabled?	DSI_CTRL[0] IF_EN	= 0x0
Enable the LP clock.	DSI_CLK_CTRL[20] LP_CLK_ENABLE	0x1
Check whether internal reset is complete?	DSI_COMPLEXIO_CFG1[29] RESET_DONE	= 0x1
Check whether power state of DSI PHY is ON?	DSI_COMPLEXIO_CFG1[26:25] PWR_STATUS	= 0x1
Check whether reset is complete?	DSI_SYSSTATUS[0] RESETDONE	= 0x1

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10.3.5.2.2.3.2 DSI Configure DSI Timing and VCs

Table 10-561 lists the steps to configure DSI timing and the VCs.

Table 10-561. DSI Timing Registers

Steps	Register/Bit Field/Programming	Value
Determine the number of DSI_FCLK clock cycles for the STOP-STATE counter.	DSI_TIMING1[12:0] STOP_STATE_COUNTER_IO	0x-
Enable/disable the multiplication factor of 4 for the number of DSI_FCLK clock cycles for the STOP-STATE counter.	DSI_TIMING1[13] STOP_STATE_X4_IO	0x-
Enable/disable the multiplication factor of 16 for the number of DSI_FCLK clock cycles for the STOP-STATE counter.	DSI_TIMING1[14] STOP_STATE_X16_IO	0x-
Clear turnaround timer settings.	DSI_TIMING1[30:16]	0x0
Determine the number of DSI_FCLK clock cycles for the LP RX timer.	DSI_TIMING2[12:0] LP_RX_TO_COUNTER	0x-
Enable/disable the multiplication factor of 4 for the number of DSI_FCLK clock cycles for the LP RX timer.	DSI_TIMING2[13] LP_RX_TO_X4	0x-
Enable/disable the multiplication factor of 16 for the number of DSI_FCLK clock cycles for the LP RX timer.	DSI_TIMING2[14] LP_RX_TO_X16	0x-
Determine the number of BYTE_CLK clock cycles for the HS RX timer.	DSI_TIMING2[28:16] HS_TX_TO_COUNTER	0x-
Enable/disable the multiplication factor of 16 for the number of BYTE_CLK clock cycles for the HS TX timer.	DSI_TIMING2[29] HS_TX_TO_X16	0x-
Enable/disable the multiplication factor of 64 for the number of BYTE_CLK clock cycles for the HS TX timer.	DSI_TIMING2[30] HS_TX_TO_X64	0x-
Set the number of TXBYTECLKHS clock cycles	DSI_CLK_TIMING[15:8] DDR_CLK_PRE and DSI_CLK_TIMING[7:0] DDR_CLK_POST	0x-
Configuration of VCi		
Select source of data and enable VP_STALL.	DSI_VC_CTRL_i[1] SOURCE	0x1
Enable/disable the checksum generation for the transmit payload.	DSI_VC_CTRL_i[7] CS_TX_EN	0x-
Enable/disable the ECC generation for the transmit header.	DSI_VC_CTRL_i[8] ECC_TX_EN	0x-
Enable/disable HS mode to send short and long packets to the peripheral.	DSI_VC_CTRL_i[9] MODE_SPEED	0x-
Configure DMA request for TX FIFO.	DSI_VC_CTRL_i[23:21] DMA_TX_REQ_NB	0x-
Configure DMA request for RX FIFO.	DSI_VC_CTRL_i[29:27] DMA_RX_REQ_NB	0x-
Configuration TX and RX FIFO		
Set size of the RX FIFO allocated for used VC.	DSI_RX_FIFO_VC_SIZE	0x-
Set size of the TX FIFO allocated for used VC.	DSI_TX_FIFO_VC_SIZE	0x-

10.3.5.2.2.4 DSI Main Sequence – Configure DSI_PHY_DSS_x Timing

Table 10-562 summarizes DSI_PHY_DSS_x timing settings. For more information about timing calculation, see Section 10.3.4.4.4, *DSI Clock Requirements*.

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Table 10-562. DSI Configure DSI_PHY_DSS_x Timing

Steps	Register/Bit Field/Programming	Value
Settings of the DSI protocol timing. For a complete description of timing specifications, see Section 10.3.4.4.4, *Clock Requirements*.	DSI_PHY_REGISTER0[31:24] REG_THSPREPARE	ceil(70 ns/DDR clock period) + 2
	DSI_PHY_REGISTER0[23:16] REG_THSPRPR_THSZERO	ceil(175 ns/DDR clock period) + 2
	DSI_PHY_REGISTER0[7:0] REG_THSEXIT	ceil(145 ns/DDR clock period)
	DSI_PHY_REGISTER0[15:8] REG_THSTRAIL	ceil(60n s/DDR clock period) + 5
	DSI_PHY_REGISTER2[7:0] REG_TCLKPREPARE	ceil(65 ns/DDR clock period)
	DSI_PHY_REGISTER1[7:0] REG_TCLKZERO	ceil(265 ns/DDR clock period)
	DSI_PHY_REGISTER1[15:8] REG_TCLKTRAIL	ceil(60 ns/DDR clock period) + 2
	DSI_PHY_REGISTER1[20:16] REG_TLPXBY2	ceil(25 ns/DDR clock period)

10.3.5.2.2.5 DSI Main Sequence – Drive STOP State

Table 10-563 lists the steps to drive the STOP state.

Table 10-563. DSI Drive STOP State

Steps	Register/Bit Field/Programming	Value
Force TX stop mode.	DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO	0x1
Wait until the end of TX stop mode assertion?	DSI_TIMING1[15] FORCE_TX_STOP_MODE_IO	= 0x1

10.3.5.2.2.6 DSI Main Sequence – Enable Command Mode Using DISPC Video Port

Table 10-564 lists the steps to enable DISPC to send frames continuously. Two BTAs must be generated:

- The first BTA gives bus possession to the display module.
- The second BTA obtains the TE trigger.

Table 10-564. DSI Enable Command Mode and Automatic TE

Steps	Register/Bit Field/Programming	Value
Insert DCS write memory continue/start code.	DSI_VC_CTRL_i[31] DCS_CMD_CODE	0x-
Enable/disable automatic insertion of DCS command codes when data is sourced by the video port.	DSI_VC_CTRL_i[30] DCS_CMD_ENABLE	0x-
Enable used VC.	DSI_VC_CTRL_i[0] VC_EN	0x1
Enable DSI protocol engine interface.	DSI_CTRL[0] IF_EN	0x1
Wait until interface is enabled?	DSI_CTRL[0] IF_EN	= 0x0
Send the sequence to receive the TE trigger from the peripheral.	DSI_VC_SHORT_PACKET_HEADER_i[31:0] HEADER	0x-
Wait until packet is sent?	DSI_VC_IRQSTATUS_i[2] PACKET_SENT_IRQ	= 0x1
Write 1 to reset the status bit.	DSI_VC_IRQSTATUS_i[2] PACKET_SENT_IRQ	0x1

NOTE: Keep reserved bits at reset value in DSI_PHY_REGISTER1 and DSI_PHY_REGISTER2.

10.3.5.2.2.7 DSI Main Sequence – Send Frame Data to LCD Panel Using Automatic TE

Table 10-565 summarizes the steps to send a frame data to the LCD panel using automatic TE.

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Table 10-565. DSI Send Frame Data to LCD Panel Using Automatic TE

Steps	Register/Bit Field/Programming	Value
Enable the transfer between DISPC and DSI. Reset after the transfer is done.	For more information, see DISPC Clock Configuration, in*Display Controller*.	
Specify the number of bytes to send. When DCS insertion is used, word count (WC) must include this one DCS byte.	DSI_VC_TE_i[23:0] TE_SIZE	(WC+1)*LPP
Set up long packet header.	DSI_VC_LONG_PACKET_HEADER_i[31:0] HEADER	0x-
Enable/disable TE control.	DSI_VC_TE_i[30] TE_EN	0x1
Wait until RX FIFO is empty?	DSI_VC_CTRL_i[20] RX_FIFO_NOT_EMPTY	= 0x0
Wait until TX FIFO is not full?	DSI_VC_CTRL_i[16] TX_FIFO_FULL	= 0x0
Enable first BTA to give bus possession to the display module.	DSI_VC_CTRL_i[6] BTA_EN	0x1
Wait until BTA IRQ event occurs?	DSI_VC_IRQSTATUS_i[5] BTA_IRQ	= 0x1
Write 1 to clear BTA IRQ status bit.	DSI_VC_IRQSTATUS_i[5] BTA_IRQ	0x1
Enable the second BTA to get the TE trigger.	DSI_VC_CTRL_i[6] BTA_EN	0x1
Wait until BTA IRQ event occurs?	DSI_VC_IRQSTATUS_i[5] BTA_IRQ	= 0x1
Write 1 to clear BTA IRQ status bit.	DSI_VC_IRQSTATUS_i[5] BTA_IRQ	0x1
Wait until transfer is complete?	DSI_VC_TE_i[30] TE_EN	= 0x0

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10.3.6 DSI Register Manual

This section describes the DSI module registers.

10.3.6.1 DSI Instance Summary

Table 10-566 summarizes the DSI module instances.

Table 10-566. DSI Instance Summary

Module Name	L3_MAIN Base Address	Size
DSI1_A	0x5800 4000	512 bytes
DSI_PHY_DSS_A	0x5800 4200	64 bytes
DPLL_DSI1_A	0x5800 4300	64 bytes
DSI1_C	0x5800 9000	512 bytes
DSI_PHY_DSS_C	0x5800 9200	64 bytes
DPLL_DSI1_C	0x5800 9300	64 bytes

10.3.6.2 DSI Registers

10.3.6.2.1 DSI Register Summary

Table 10-567. DSI1_A Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI1_A L3_MAIN Physical Address
DSI_REVISION	R	32	0x0000 0000	0x5800 4000
DSI_SYSCONFIG	RW	32	0x0000 0010	0x5800 4010
DSI_SYSSTATUS	R	32	0x0000 0014	0x5800 4014
DSI_IRQSTATUS	RW	32	0x0000 0018	0x5800 4018
DSI_IRQENABLE	RW	32	0x0000 001C	0x5800 401C
DSI_CTRL	RW	32	0x0000 0040	0x5800 4040
DSI_GNQ	R	32	0x0000 0044	0x5800 4044
DSI_COMPLEXIO_CFG1	RW	32	0x0000 0048	0x5800 4048
DSI_COMPLEXIO_IRQSTATUS	RW	32	0x0000 004C	0x5800 404C
DSI_COMPLEXIO_IRQENABLE	RW	32	0x0000 0050	0x5800 4050
DSI_CLK_CTRL	RW	32	0x0000 0054	0x5800 4054
DSI_TIMING1	RW	32	0x0000 0058	0x5800 4058
DSI_TIMING2	RW	32	0x0000 005C	0x5800 405C
DSI_VM_TIMING1	RW	32	0x0000 0060	0x5800 4060
DSI_VM_TIMING2	RW	32	0x0000 0064	0x5800 4064

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Table 10-567. DSI1_A Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DSI1_A L3_MAIN Physical Address
DSI_VM_TIMING3	RW	32	0x0000 0068	0x5800 4068
DSI_CLK_TIMING	RW	32	0x0000 006C	0x5800 406C
DSI_TX_FIFO_VC_SIZE	RW	32	0x0000 0070	0x5800 4070
DSI_RX_FIFO_VC_SIZE	RW	32	0x0000 0074	0x5800 4074
DSI_COMPLEXIO_CFG2	RW	32	0x0000 0078	0x5800 4078
DSI_RX_FIFO_VC_FULLNESS	R	32	0x0000 007C	0x5800 407C
DSI_VM_TIMING4	RW	32	0x0000 0080	0x5800 4080
DSI_TX_FIFO_VC_EMPTINESS	R	32	0x0000 0084	0x5800 4084
DSI_VM_TIMING5	RW	32	0x0000 0088	0x5800 4088
DSI_VM_TIMING6	RW	32	0x0000 008C	0x5800 408C
DSI_VM_TIMING7	RW	32	0x0000 0090	0x5800 4090
DSI_STOPCLK_TIMING	RW	32	0x0000 0094	0x5800 4094
DSI_CTRL2	RW	32	0x0000 0098	0x5800 4098
DSI_VM_TIMING8	RW	32	0x0000 009C	0x5800 409C
DSI_TE_HSYNC_WIDTH_j (1)	RW	32	0x0000 00A0 + (0xc * j)	0x5800 40A0 + (0xc * j)
DSI_TE_VSYNC_WIDTH_j (1)	RW	32	0x0000 00A4 + (0xc * j)	0x5800 40A4 + (0xc * j)
DSI_TE_HSYNC_NUMBER_j (1)	RW	32	0x0000 00A8 + (0xc * j)	0x5800 40A8 + (0xc * j)
DSI_VC_CTRL_i (2)	RW	32	0x0000 0100 + (0x20 * i)	0x5800 4100 + (0x20 * i)
DSI_VC_TE_i (2)	RW	32	0x0000 0104 + (0x20 * i)	0x5800 4104 + (0x20 * i)
DSI_VC_LONG_PACKET_HEADER_i (2)	W	32	0x0000 0108 + (0x20 * i)	0x5800 4108 + (0x20 * i)
DSI_VC_LONG_PACKET_PAYLOAD_i (2)	W	32	0x0000 010C + (0x20 * i)	0x5800 410C + (0x20 * i)
DSI_VC_SHORT_PACKET_HEADER_i (2)	RW	32	0x0000 0110 + (0x20 * i)	0x5800 4110 + (0x20 * i)

(1) j = 0 to 1
(2) i = 0 to 3

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Table 10-567. DSI1_A Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DSI1_A L3_MAIN Physical Address
DSI_VC_IRQSTATUS_i (2)	RW	32	0x0000 0118 + (0x20 * i)	0x5800 4118 + (0x20 * i)
DSI_VC_IRQENABLE_i (2)	RW	32	0x0000 011C + (0x20 * i)	0x5800 411C + (0x20 * i)

Table 10-568. DSI1_C Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI1_C L3_MAIN Physical Address
DSI_REVISION	R	32	0x0000 0000	0x5800 9000
DSI_SYSCONFIG	RW	32	0x0000 0010	0x5800 9010
DSI_SYSSTATUS	R	32	0x0000 0014	0x5800 9014
DSI_IRQSTATUS	RW	32	0x0000 0018	0x5800 9018
DSI_IRQENABLE	RW	32	0x0000 001C	0x5800 901C
DSI_CTRL	RW	32	0x0000 0040	0x5800 9040
DSI_GNQ	R	32	0x0000 0044	0x5800 9044
DSI_COMPLEXIO_CFG1	RW	32	0x0000 0048	0x5800 9048
DSI_COMPLEXIO_IRQSTATUS	RW	32	0x0000 004C	0x5800 904C
DSI_COMPLEXIO_IRQENABLE	RW	32	0x0000 0050	0x5800 9050
DSI_CLK_CTRL	RW	32	0x0000 0054	0x5800 9054
DSI_TIMING1	RW	32	0x0000 0058	0x5800 9058
DSI_TIMING2	RW	32	0x0000 005C	0x5800 905C
DSI_VM_TIMING1	RW	32	0x0000 0060	0x5800 9060
DSI_VM_TIMING2	RW	32	0x0000 0064	0x5800 9064
DSI_VM_TIMING3	RW	32	0x0000 0068	0x5800 9068
DSI_CLK_TIMING	RW	32	0x0000 006C	0x5800 906C
DSI_TX_FIFO_VC_SIZE	RW	32	0x0000 0070	0x5800 9070
DSI_RX_FIFO_VC_SIZE	RW	32	0x0000 0074	0x5800 9074
DSI_COMPLEXIO_CFG2	RW	32	0x0000 0078	0x5800 9078
DSI_RX_FIFO_VC_FULLNESS	R	32	0x0000 007C	0x5800 907C

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Table 10-568. DSI1_C Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DSI1_C L3_MAIN Physical Address
DSI_VM_TIMING4	RW	32	0x0000 0080	0x5800 9080
DSI_TX_FIFO_VC_EMPTINESS	R	32	0x0000 0084	0x5800 9084
DSI_VM_TIMING5	RW	32	0x0000 0088	0x5800 9088
DSI_VM_TIMING6	RW	32	0x0000 008C	0x5800 908C
DSI_VM_TIMING7	RW	32	0x0000 0090	0x5800 9090
DSI_STOPCLK_TIMING	RW	32	0x0000 0094	0x5800 9094
DSI_CTRL2	RW	32	0x0000 0098	0x5800 9098
DSI_VM_TIMING8	RW	32	0x0000 009C	0x5800 909C
DSI_TE_HSYNC_WIDTH_j (1)	RW	32	0x0000 00A0 + (0xc * j)	0x5800 90A0 + (0xc * j)
DSI_TE_VSYNC_WIDTH_j (1)	RW	32	0x0000 00A4 + (0xc * j)	0x5800 90A4 + (0xc * j)
DSI_TE_HSYNC_NUMBER_j (1)	RW	32	0x0000 00A8 + (0xc * j)	0x5800 90A8 + (0xc * j)
DSI_VC_CTRL_i (2)	RW	32	0x0000 0100 + (0x20 * i)	0x5800 9100 + (0x20 * i)
DSI_VC_TE_i (2)	RW	32	0x0000 0104 + (0x20 * i)	0x5800 9104 + (0x20 * i)
DSI_VC_LONG_PACKET_HEADER_i (2)	W	32	0x0000 0108 + (0x20 * i)	0x5800 9108 + (0x20 * i)
DSI_VC_LONG_PACKET_PAYLOAD_i (2)	W	32	0x0000 010C + (0x20 * i)	0x5800 910C + (0x20 * i)
DSI_VC_SHORT_PACKET_HEADER_i (2)	RW	32	0x0000 0110 + (0x20 * i)	0x5800 9110 + (0x20 * i)
DSI_VC_IRQSTATUS_i (2)	RW	32	0x0000 0118 + (0x20 * i)	0x5800 9118 + (0x20 * i)
DSI_VC_IRQENABLE_i (2)	RW	32	0x0000 011C + (0x20 * i)	0x5800 911C + (0x20 * i)

(1) j = 0 to 1
(2) i = 0 to 3

10.3.6.2.2 DSI Register Description

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Table 10-569. DSI_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5800 4000 0x5800 9000	**Instance**	DSI1_A DSI1_C
Description	IP Revision		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See (1)

(1) TI Internal data

Table 10-570. Register Call Summary for Register DSI_REVISION

MIPI Display Serial Interface

- DSI Register Summary: [0] [1]

Table 10-571. DSI_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5800 4010 0x5800 9010	**Instance**	DSI1_A DSI1_C
Description	System configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED				SIDLEMODE		ENWAKEUP	SOFT_RESET	AUTO_IDLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:8	CLOCKACTIVITY	Clock activity during wake-up mode period 0x0: Interface and functional clocks can be switched off. 0x1: Functional clocks can be switched off and Interface clocks are maintained during wake-up period. 0x2: Interface clocks can be switched off and functional clocks are maintained during wake-up period. 0x3: Interface and functional clocks are maintained during wake-up period.	RW	0x0
7:5	RESERVED		R	0x0
4:3	SIDLEMODE	Slave interface power management, Idle req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged. 0x2: Smart-idle. Acknowledgment to an idle request is given based on the internal activity of the module. 0x3: Reserved	RW	0x2

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Bits	Field Name	Description	Type	Reset
2	ENWAKEUP	Wake-up mode enable bit 0x0: Wakeup is disabled. 0x1: Wakeup is enabled.	RW	0
1	SOFT_RESET	Software reset. Set the bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads returns 0. 0x0: Normal mode 0x1: The module is reset.	RW	0
0	AUTO_IDLE	Internal interface gating strategy 0x0: Interface clock is free-running. 0x1: Automatic Interface clock-gating strategy is applied based on the interface activity.	RW	1

Table 10-572. Register Call Summary for Register DSI_SYSCONFIG

MIPI Display Serial Interface
- DSI Software Reset: [0]
- DSI Power Management: [1] [2]
- DSI PHY Software Reset: [3]
- DSI Global Initialization: [4] [5] [6]
- DSI Register Summary: [7] [8]

Table 10-573. DSI_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5800 4014 0x5800 9014	**Instance**	DSI1_A DSI1_C
Description	System status register . This register provides status information about the module, excluding the interrupt status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESET_DONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RESET_DONE	Internal reset monitoring Read 0x0: Internal module reset is ongoing. Read 0x1: Reset completed.	R	1

Table 10-574. Register Call Summary for Register DSI_SYSSTATUS

MIPI Display Serial Interface
- DSI Software Reset: [0] [1]
- DSI Global Initialization: [2] [3]
- DSI Video Mode Using the DISPC Video Port: [4]
- DSI Command Mode Using the DISPC Video Port: [5]
- DSI Register Summary: [6] [7]

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Table 10-575. DSI_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5800 4018 0x5800 9018	**Instance**	DSI1_A DSI1_C
Description	Interrupt status register – All virtual channels + DSI PHY + PLL This register associates 1 bit for each virtual channel to determine which virtual channel generated the interrupt. The virtual channel must be enabled for events to be generated on that virtual channel. If the virtual channel is disabled, the interrupt is not generated.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TE1_LINE_IRQ	TE0_LINE_IRQ	TA_TO_IRQ	RESERVED	SYNC_LOST_IRQ	ACK_TRIGGER_IRQ	TE_TRIGGER_IRQ	LP_RX_TO_IRQ	HS_TX_TO_IRQ	RESERVED			COMPLEXIO_ERR_IRQ	PLL_RECAL_IRQ	PLL_UNLOCK_IRQ	PLL_LOCK_IRQ	RESERVED	RESYNCHRONIZATION_IRQ	WAKEUP_IRQ	VIRTUAL_CHANNEL3_IRQ	VIRTUAL_CHANNEL2_IRQ	VIRTUAL_CHANNEL1_IRQ	VIRTUAL_CHANNEL0_IRQ	

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x000
22	TE1_LINE_IRQ	The VSYNC and corresponding HSYNC pulses defined in DSI_TE_HSYNC_NUMBER for the line TE1 have been received by the DSI protocol engine and have triggeedr the start of the data transfer to the peripheral. 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
21	TE0_LINE_IRQ	The VSYNC and corresponding HSYNC pulses defined in DSI_TE_HSYNC_NUMBER for the line TE0 have been received by the DSI protocol engine and have triggered the start of the data transfer to the peripheral. 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
20	TA_TO_IRQ	Turnaround time-out 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
19	RESERVED	Reserved. Keep at reset value.	RW	0
18	SYNC_LOST_IRQ	Synchronization with video port is lost (video mode only). 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
17	ACK_TRIGGER_IRQ	Acknowledge trigger 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
16	TE_TRIGGER_IRQ	Tearing effect trigger 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
15	LP_RX_TO_IRQ	Interrupt for low-power RX time-out 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
14	HS_TX_TO_IRQ	Interrupt for high-speed TX time-out 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
13:11	RESERVED		R	0x0
10	COMPLEXIO_ERR_IRQ	Error signaling from DSI PHY: status of the DSI PHY errors received from the DSI PHY (events are defined in DSI_COMPLEXIO_IRQSTATUS). Read 0x0: Reads: Event is false. Read 0x1: Reads: Event is true (pending).	R	0
9	PLL_RECAL_IRQ	PLL recal event (assertion of DSIRecal signal from the DSI PLL control module) 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
8	PLL_UNLOCK_IRQ	PLL unclock event (deassertion of DSILock signal from the DSI PLL control module) 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
7	PLL_LOCK_IRQ	PLL clock event (assertion of DSILock signal from the DSI PLL control module) 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
6	RESERVED		R	0
5	RESYNCHRONIZATION_IRQ	Video mode resynchronization indicates to software users that the video port works but the configuration of the timings for the display controller (DISPC) and DSI protocol engine may need to be modified to avoid resynchronization from occurring. 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
4	WAKEUP_IRQ	Wakeup 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
3	VIRTUAL_CHANNEL3_IRQ	Virtual channel 3 Read 0x0: Reads: Event is false. Read 0x1: Reads: Event is true (pending).	R	0

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Bits	Field Name	Description	Type	Reset
2	VIRTUAL_CHANNEL2_IRQ	Virtual channel 2 Read 0x0: Reads: Event is false. Read 0x1: Reads: Event is true (pending).	R	0
1	VIRTUAL_CHANNEL1_IRQ	Virtual channel 1 Read 0x0: Reads: Event is false. Read 0x1: Reads: Event is true (pending).	R	0
0	VIRTUAL_CHANNEL0_IRQ	Virtual channel 0 Read 0x0: Reads: Event is false. Read 0x1: Reads: Event is true (pending).	R	0

Table 10-576. Register Call Summary for Register DSI_IRQSTATUS

MIPI Display Serial Interface

- DSI Interrupt Requests: [0]
- DSI Transfer Modes: [1] [2]
- DSI Timers: [3] [4]
- DSI PHY Triggers: [5] [6]
- DSI Interrupts: [7]
- DSI PLL Error Handling: [8] [9] [10]
- DSI PHY Error Handling: [11]
- DSI Global Initialization: [12]
- DSI Register Summary: [13] [14]

Table 10-577. DSI_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x5800 401C 0x5800 901C	**Instance**	DSI1_A DSI1_C
Description	Interrupt enable register – This register associates 1 bit for each virtual channel to enable or disable each virtual channel individually.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TE1_LINE_IRQ_EN	TE0_LINE_IRQ_EN	TA_TO_IRQ_EN	RESERVED	SYNC_LOST_IRQ_EN	ACK_TRIGGER_IRQ_EN	TE_TRIGGER_IRQ_EN	LP_RX_TO_IRQ_EN	HS_TX_TO_IRQ_EN	RESERVED			PLL_RECAL_IRQ_EN	PLL_UNLOCK_IRQ_EN	PLL_LOCK_IRQ_EN	RESERVED	RESYNCHRONIZATION_IRQ_EN	WAKEUP_IRQ_EN	RESERVED				

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x000
22	TE1_LINE_IRQ_EN	The VSYNC and corresponding HSYNC pulses defined in DSI_TE_HSYNC_NUMBER for the line TE1 have been received by the DSI protocol engine and have triggered the start of the data transfer to the peripheral. 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0

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Bits	Field Name	Description	Type	Reset
21	TE0_LINE_IRQ_EN	The VSYNC and corresponding HSYNC pulses defined in DSI_TE_HSYNC_NUMBER for the line TE0 have been received by the DSI protocol engine and have triggered the start of the data transfer to the peripheral. 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
20	TA_TO_IRQ_EN	Turnaround time-out 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
19	RESERVED	Reserved. Keep at reset value.	RW	0
18	SYNC_LOST_IRQ_EN	Synchronization with video port is lost (video mode only) 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
17	ACK_TRIGGER_IRQ_EN	Acknowledge trigger 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
16	TE_TRIGGER_IRQ_EN	Tearing effect trigger 0x0: Event is masked.. 0x1: Event generates an interrupt when it occurs..	RW	0
15	LP_RX_TO_IRQ_EN	Interrupt for low-power RX time-out 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
14	HS_TX_TO_IRQ_EN	Interrupt for high-speed TX time-out 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
13:10	RESERVED		R	0x0
9	PLL_RECAL_IRQ_EN	PLL recal event (assertion of DSIRecal signal from the DSI PLL control module) 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
8	PLL_UNLOCK_IRQ_EN	PLL unclock event (deassertion of DSILock signal from the DSI PLL control module) 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
7	PLL_LOCK_IRQ_EN	PLL clock event (assertion of DSILock signal from the DSI PLL control module) 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
6	RESERVED		R	0
5	RESYNCHRONIZATION_IRQ_EN	Video mode resynchronization 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
4	WAKEUP_IRQ_EN	Wakeup 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
3:0	RESERVED		R	0x0

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Table 10-578. Register Call Summary for Register DSI_IRQENABLE

MIPI Display Serial Interface

- DSI PHY Triggers: [0] [1]
- DSI Interrupts: [2]
- DSI Video Mode Using the DISPC Video Port: [3]
- DSI Command Mode Using the DISPC Video Port: [4]
- DSI Register Summary: [5] [6]

Table 10-579. DSI_CTRL

Address Offset	0x0000 0040		
Physical Address	0x5800 4040 0x5800 9040	**Instance**	DSI1_A DSI1_C
Description	Global control register – This register controls the DSI protocol engine module. This register mustnot be modified dynamically (except IF_EN bit fields).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DISPC_UPDATE_SYNC	HSA_BLANKING_MODE	HBP_BLANKING_MODE	HFP_BLANKING_MODE	BLANKING_MODE	EOT_ENABLE	VP_HSYNC_END	VP_HSYNC_START	VP_VSYNC_END	VP_VSYNC_START	TRIGGER_RESET_MODE	LINE_BUFFER	VP_VSYNC_POL	VP_HSYNC_POL	VP_DE_POL	VP_CLK_POL	VP_DATA_BUS_WIDTH		TRIGGER_RESET	VP_CLK_RATIO	TX_FIFO_ARBITRATION	ECC_RX_EN	CS_RX_EN	IF_EN

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	DISPC_UPDATE_SYNC	Determines whether the Dispc_Update_Sync signal from the display controller is used 0x0: Dispc_Update_Sync signal is not used. 0x1: Dispc_Update_Sync signal is used.	RW	0
23	HSA_BLANKING_MODE	Blanking mode 0x0: Packets in TX FIFO are sent during HSA blanking period of video mode or LPS is used. 0x1: LONG BLANKING PACKETS only are used during HSA blanking period of video mode.	RW	0
22	HBP_BLANKING_MODE	Blanking mode 0x0: Packets in TX FIFO are sent during HBP blanking period of video mode or LPS is used. 0x1: LONG BLANKING PACKETS only are used during HBP blanking period of video mode.	RW	0
21	HFP_BLANKING_MODE	Blanking mode 0x0: Packets in TX FIFO are sent during HFP blanking period of video mode or LPS is used. 0x1: LONG BLANKING PACKETS only are used during HFP blanking period of video mode.	RW	0

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Bits	Field Name	Description	Type	Reset
20	BLANKING_MODE	Blanking mode 0x0: LPS is used during blanking periods of video mode (except HSA, HBP, HFP defined in HSA_BLANKING_MODE, HBP_BLANKING_MODE, and HFP_BLANKING_MODE, respectively) when there is no command mode data in TX FIFO ready to be sent. Thus, blanking periods can be different during the frame depending on the TX FIFO. 0x1: LONG BLANKING PACKETS are used during blanking periods of video mode (except HSA, HBP, HFP defined in HSA_BLANKING_MODE, HBP_BLANKING_MODE, and HFP_BLANKING_MODE, respectively) regardless of the packets present in the TX FIFO ready to be sent.	RW	0
19	EOT_ENABLE	Enable EOT packets at the end of HS transmission. 0x0: No EOT packets 0x1: EOT packet is sent at all HS-to-LP transitions.	RW	0
18	VP_HSYNC_END	HSYNC end pulse 0x0: Disabled. No HSYNC END short packet is generated. 0x1: Enabled. While the HSYNC END pulse is detected, the associated short packet HSYNC END is generated.	RW	0
17	VP_HSYNC_START	HSYNC start pulse. 0x0: Disabled. No HSYNC START short packet is generated. 0x1: Enabled. While the HSYNC start pulse is detected, the associated short packet HSYNC START is generated.	RW	0
16	VP_VSYNC_END	VSYNC end pulse 0x0: Disabled. No VSYNC END short packet is generated. 0x1: Enabled. While the VSYNC END pulse is detected, the associated short packet VSYNC END is generated.	RW	0
15	VP_VSYNC_START	VSYNC start pulse 0x0: Disabled. No VSYNC START short packet is generated. 0x1: Enabled. While the VSYNC START pulse is detected, the associated short packet VSYNC START is generated.(1)	RW	0
14	TRIGGER_RESET_MODE	Selection of the trigger reset mode 0x0: Synchronized: The mode is valid only if there is virtual channel using the video mode and it is active. The principal is to wait for the current video frame to be transferred on the link. Any data received after the VSYNC are ignored. 0x1: Immediate: All pending requests in TX FIFO are taken into account for transfer scheduling, the RX FIFO is ignored, and the data from video port are ignored as soon as possible. Only the current transfer on DSI link and already scheduled ones are transmitted. All the other transfers are discarded.	RW	0
13:12	LINE_BUFFER	Number of line buffers to be used while receiving data on the video port. The valid values are from 0 to DSI_GNQ[17:16] VP1_NB_LINE_BUFFER. 0x0: No line buffer 0x1: One line buffer 0x2: Two line buffers	RW	0x0

(1) In DSI video mode, if the VSA bit field in DSI_VM_TIMING2 is set to 0x0, no vertical synchronization packet will be sent, even if VP_VSYNC_START is set to 0x1 in DSI_CTRL.

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Bits	Field Name	Description	Type	Reset
11	VP_VSYNC_POL	VP vertical synchronization signal polarity 0x0: VSYNC signal on the video port is active low. 0x1: VSYNC signal on the video port is active high.	RW	0
10	VP_HSYNC_POL	VP horizontal synchronization signal polarity 0x0: HSYNC signal on the video port is active low. 0x1: HSYNC signal on the video port is active high.	RW	0
9	VP_DE_POL	VP data enable signal polarity 0x0: DE signal on the video port is active low. 0x1: DE signal on the video port is active high.	RW	0
8	VP_CLK_POL	VP pixel clock polarity 0x0: The DSI protocol engine module captures the data on the VP on the pixel clock falling edge. The module connected to the VP must drive the data on the pixel clock rising edge. 0x1: The DSI protocol engine module captures the data on the VP on the pixel clock raising edge. The module connected to the VP must drive the data on the pixel clock falling edge.	RW	1
7:6	VP_DATA_BUS_WIDTH	Defines the size of the video port data bus 0x0: 16-bit data width (LSB of the 24-bit video port data bus) 0x1: 18-bit data width (LSB of the 24-bit video port data bus) 0x2: 24-bit data width (LSB of the 24-bit video port data bus)	RW	0x0
5	TRIGGER_RESET	Send the reset trigger to the peripheral. 0x0: Reads: Reset trigger generation is complete. It is reset by hardware when it completes. Writes: Cancellation of the request for reset trigger generation (may be too late because it is already ongoing) 0x1: Reads: Generation of the reset trigger has been requested by the user (may be ongoing but not yet complete). Writes: Request for reset trigger to be sent to the peripheral	RW	0
4	VP_CLK_RATIO	The field indicates the clock ratio between VP_CLK and VP_PCLK. The clock VP_PCLK is generated from VP_CLK. It is divided down. The information is used only when the video port is used to provide data in command mode. In the case of video mode, it is not used. 0x0: The clock VP_PCLK is the clock VP_CLK divided by 2. The duty cycle of VP_PCLK is 50/50. 0x1: The clock VP_PCLK is the clock VP_CLK divided by 3 or more. The duty cycle of VP_PCLK is not 50/50 for odd ratio numbers (3 , 5, 7, ...).	RW	0
3	TX_FIFO_ARBITRATION	Defines the arbitration scheme for granting the virtual channel pending ready requests in the TX FIFO 0x0: Round-robin scheme is used. 0x1: Sequential scheme is used.	RW	0
2	ECC_RX_EN	Enables the Error Correction Code check for the received header (short and long packets for all virtual channel ids). 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
1	CS_RX_EN	Enables the checksum check for the received payload (long packet only for all virtual channel ids) 0x0: Disabled 0x1: Enabled	RW	0
0	IF_EN	Enables the module. When the module is disabled, the signals from the DSI PHY are gated (no updates of the interrupt status register). It is not possible to change the bit fields in the DSI_CTRL register except when IF_EN is enabled. All the other registers can be changed except those that require DSI_VC_CTRL_i[0] VC_EN to be equal to 0 to be modified. 0x0: The interface is disabled. If one of the virtual channels uses the video mode with the video port to receive data, the DSI protocol engine is disabled when the next VSYNC is received and all the data in the FIFO for the other virtual channels in command mode are sent to the peripherals (if BTA_EN is enabled, the DSI protocol must wait for the response and BTA from the peripheral before disabling all the internal logic, because an acknowledge is requested). 0x1: The interface is enabled immediately, and the data acquisition on the video port starts on the next VSYNC (video mode) or first data received in the slave port FIFO (command mode).	RW	0

Table 10-580. Register Call Summary for Register DSI_CTRL

MIPI Display Serial Interface

- DSI Short Packet: [0] [1] [2] [3] [4] [5]
- DSI Global Register Controls: [6] [7] [8] [9] [10] [11] [12]
- DSI Transfer Modes: [13] [14] [15] [16] [17] [18]
- DSI Clock Requirements: [19]
- DSI Video Port Interface: [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]
- DSI Timers: [31] [32] [33] [34] [35] [36]
- DSI Bus Turnaround: [37] [38] [39] [40]
- DSI PHY Triggers: [41] [42] [43] [44]
- DSI ECC Generation: [45]
- DSI Checksum Generation for Long Packet Payloads: [46]
- DSI EOT Packet: [47]
- DSI Power Control of DSI PHY and DSI PLL: [48] [49] [50] [51] [52] [53]
- DSI How to Configure the DSI PLL in Video Mode: [54] [55]
- DSI PHY Pad Configuration: [56] [57] [58]
- DSI Video Mode Using the DISPC Video Port: [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73]
- DSI Command Mode Using the DISPC Video Port: [74] [75] [76] [77] [78] [79] [80] [81] [82] [83] [84]
- DSI Register Summary: [85] [86]
- DSI Register Description: [87] [88] [89] [90] [91] [92] [93] [94]

Table 10-581. DSI_GNQ

Address Offset	0x0000 0044		
Physical Address	0x5800 4044 0x5800 9044	**Instance**	DSI1_A DSI1_C
Description	Generic parameter register – This register provide a way to read the generic parameters used in the design.		
Type	R		

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31 30 29 28 27 26 25 24	23 22	21	20 19 18	17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2 1 0
RESERVED	NB_VIDEO_PORTS	VP2_NB_LINE_BUFFER	RESERVED	VP2_LINE_BUFFER_SIZE	VP1_NB_LINE_BUFFER	RESERVED	VP1_LINE_BUFFER_SIZE	NB_DATA_LANES	NB_DMA_REQUEST	RX_FIFODEPTH	TX_FIFODEPTH

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved	R	0x00
24	NB_VIDEO_PORTS	Number of video ports Read 0x0: Only video port 1 is present. Read 0x1: Video port 1 and video port 2 are present.	R	1
23:22	VP2_NB_LINE_BUFFER	Determines the number of video buffer lines associated to video port 2 Read 0x0: No line buffer Read 0x1: One line buffer of the size defined in LINE_BUFFER_SIZE Read 0x2: Two line buffers of the size defined in LINE_BUFFER_SIZE	R	0x2
21	RESERVED	Reserved	R	0
20:18	VP2_LINE_BUFFER_SIZE	Determines the video line buffer size associated to video port 2 Read 0x1: 512 x 24 bits, 682 x 18 bits, 768 x 16 bits (memory of 384 x 32 bits) Read 0x2: 682 x 24 bits, 910 x 18 bits, 1024 x 16 bits (memory of 512 x 32 bits) Read 0x3: 853 x 24 bits, 1137 x 18 bits, 1280 x 16 bits (memory of 640 x 32 bits) Read 0x4: 1024 x 24 bits, 1365 x 18 bits, 1536 x 16 bits (memory of 768 x 32 bits) Read 0x5: 1194 x 24 bits, 1592 x 18 bits, 1792 x 16 bits (memory of 896 x 32 bits) Read 0x6: 1365 x 24 bits, 1820 x 18 bits, 2048 x 16 bits (memory of 1024 x 32 bits)	R	0x4
17:16	VP1_NB_LINE_BUFFER	Determines the number of video buffer lines associated to video port 1 Read 0x0: No line buffer Read 0x1: 1 line buffer of the size defined in LINE_BUFFER_SIZE Read 0x2: 2 line buffers of the size defined in LINE_BUFFER_SIZE	R	0x2
15	RESERVED	Reserved	R	0

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Bits	Field Name	Description	Type	Reset
14:12	VP1_LINE_BUFFER_SIZE	Determines the video line buffer size associated to video port 1 Read 0x1: 512 x 24 bits, 682 x 18 bits, 768 x16 bits (memory of 384 x 32 bits) Read 0x2: 682 x 24 bits, 910 x 18 bits, 1024 x16 bits (memory of 512 x 32 bits) Read 0x3: 853 x 24 bits, 1137 x 18 bits, 1280 x16 bits (memory of 640 x 32 bits) Read 0x4: 1024 x 24 bits, 1365 x 18 bits, 1536 x16 bits (memory of 768 x 32 bits) Read 0x5: 1194 x 24 bits, 1592 x 18 bits, 1792 x16 bits (memory of 896 x 32 bits) Read 0x6: 1365 x 24 bits, 1820 x 18 bits, 2048 x16 bits (memory of 1024 x 32 bits) Read 0x7: 1920 x 24 bits, 2560 x 18 bits, 2880 x16 bits (memory of 1440 x 32 bits)	R	0x7
11:9	NB_DATA_LANES	Determines the number of data lanes supported by the DSI protocol engine Read 0x1: One data lane Read 0x2: Two data lanes Read 0x3: Three data lanes Read 0x4: Four data lanes	R	0x4
8:6	NB_DMA_REQUEST	Determines the number of DMA_REQ signals Read 0x0: No DMA request Read 0x1: One DMA request Read 0x2: Two DMA requests Read 0x3: Three DMA requests Read 0x4: Four DMA requests	R	0x4
5:3	RX_FIFODEPTH	Determines the data RX FIFO depth (32-bit words) on the slave port Read 0x4: 32x 33 bits Read 0x5: 64x 33 bits Read 0x6: 128 x 33 bits Read 0x7: 256 x 33 bits	R	0x6
2:0	TX_FIFODEPTH	Determines the data TX FIFO depth (33-bit words) on the slave port Read 0x4: 32x 33 bits Read 0x5: 64x 33 bits Read 0x6: 128 x 33 bits Read 0x7: 256 x 33 bits	R	0x6

Table 10-582. Register Call Summary for Register DSI_GNQ

MIPI Display Serial Interface

- DSI Register Summary: [0] [1]
- DSI Register Description: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29]

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Table 10-583. DSI_COMPLEXIO_CFG1

Address Offset	0x0000 0048		
Physical Address	0x5800 4048 0x5800 9048	**Instance**	DSI1_A DSI1_C
Description	Complexio configuration register for the DSI PHY. This register contains the lane configuration for the order and position of the lanes (clock and data) and the polarity order for the control of the PHY differential signals and the control bit for the power FSM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHADOWING	GOBIT	RESET_DONE	PWR_CMD		PWR_STATUS		RESERVED					DATA4_POL	DATA4_POSITION			DATA3_POL	DATA3_POSITION			DATA2_POL	DATA2_POSITION			DATA1_POL	DATA1_POSITION			CLOCK_POL	CLOCK_POSITION		

Bits	Field Name	Description	Type	Reset
31	SHADOWING	Shadowing configuration 0x0: Disabled. The writes to the DSI_PHY_REGISTER0 through DSI_PHY_REGISTER2 registers are done like the other SCP registers. 0x1: Enabled. The writes to the DSI_PHY_REGISTER0 through DSI_PHY_REGISTER2 registers are done only when the GOBIT is set and when the signal DISPCUpdataSync from the display controller module is active.	RW	0
30	GOBIT	Allows the synchronized update of the shadow registers when the signal DISPCUpdateSync is active. 0x0: Resets the GOBIT. The hardware has finished the update of the shadow SCP registers. The bit is reset by hardware. The software can reset the bit if the user decides to abort it. There is no guarantee that the software reset is done before the transfer of the values to the DSI PHY. 0x1: Set the GOBIT. Only when the transfer of the new values for the three first registers is completed (3, 2, 1, or 0 transfers are performed based on the number of registers to update), the GOBIT is reset. The DISPCUpdateSync signal is used to synchronize the update. The bit must be set only when it is in reset state.	RW	0
29	RESET_DONE	Internal reset monitoring of the power domain using the TXBYTECLKHS clock from the DSI PHY Read 0x0: Internal module reset is ongoing. Read 0x1: Reset completed.	R	1
28:27	PWR_CMD	Command for power control of the DSI PHY 0x0: Command to change to OFF state 0x1: Command to change to ON state 0x2: Command to change to ULTRALOW-POWER state	RW	0x0
26:25	PWR_STATUS	Status of the power control of the DSI PHY Read 0x0: DSI PHY in OFF state Read 0x1: DSI PHY in ON state Read 0x2: DSI PHY in ULTRALOW-POWER state	R	0x0
24:20	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
19	DATA4_POL	± differential pin order of the fourth data lane 0x0: ± pin order (DSI.DX = + and DSi.DY = –) 0x1: ± pin order (DSI.DX= – and DSi.DY = +)	RW	0
18:16	DATA4_POSITION	Position and order of the fourth data lane 0x0: Not used/connected 0x1: The fourth data lane is at the first position (first lane is lane 0). 0x2: The fourth data lane is at the second position (second lane is lane 1). 0x3: The fourth data lane is at the third position (third lane is lane 2). 0x4: The fourth data lane is at the fourth position (fourth lane is lane 3). 0x5: The fourth data lane is at the fifth position (fifth lane is lane 4).	RW	0x0
15	DATA3_POL	± differential pin order of the third data lane 0x0: ± pin order (DSI.DX = + and DSi.DY = –) 0x1: ± pin order (DSI.DX = – and DSi.DY = +)	RW	0
14:12	DATA3_POSITION	Position and order of the third data lane 0x0: Not used/connected 0x1: The third data lane is at the first position (first lane is lane 0). 0x2: The third data lane is at the second position (second lane is lane 1). 0x3: The third data lane is at the third position (third lane is lane 2). 0x4: The third data lane is at the fourth position 4 (fourth lane is lane 3). 0x5: The third data lane is at the fifth position (fifth lane is lane 4).	RW	0x0
11	DATA2_POL	± differential pin order of the seond data lane 0x0: ± pin order (DSI.DX = + and DSi.DY = –) 0x1: ± pin order (DSI.DX = – and DSi.DY = +)	RW	0
10:8	DATA2_POSITION	Position and order of the second data lane 0x0: Not used/connected 0x1: The second data lane is at the first position (first lane is lane 0). 0x2: The second data lane is at the second position (second lane is lane 1). 0x3: The second data lane is at the third position (third lane is lane 2). 0x4: The second data lane is at the fourth position (fourth lane is lane 3). 0x5: The second data lane is at the fifth position (fifth lane is lane 4).	RW	0x0
7	DATA1_POL	± pin differential pin order of the first data lane 0x0: ± pin order (DSI.DX = + and DSi.DY = –) 0x1: ± pin order (DSI.DX = – and DSi.DY = +)	RW	0

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Bits	Field Name	Description	Type	Reset
6:4	DATA1_POSITION	Position and order of the first data lane. The first data lane s always present. 0x0: Not used/connected 0x1: The first data lane is at the first position (first lane is lane 0). 0x2: The first data lane is at the second position (second lane is lane 1). 0x3: The first data lane is at the third position (third lane is lane 2). 0x4: The first data lane is at the fourth position (fourth lane is lane 3). 0x5: The first data lane is at the fifth position (fifth lane is lane 4).	RW	0x0
3	CLOCK_POL	± differential pin order of the clock lane 0x0: ± pin order (DSI.DX = + and DSi.DY = –) 0x1: ± pin order (DSI.DX = – and DSi.DY = +)	RW	0
2:0	CLOCK_POSITION	Position and order of the clock lane; 0, 5, 6, and 7 are reserved. The clock lane is always present but cannot be at the fifth position even if the DSI PHY consists of five lanes. 0x0: Not used/connected 0x1: Clock lane is at the first position (first lane is lane 0). 0x2: Clock lane is at the second position (second lane is lane 1). 0x3: Clock lane is at the third position (third lane is lane 2). 0x4: Clock lane is at the fourth position (fourth lane is lane 3). 0x5: Reserved 0x6: Reserved 0x7: Reserved	RW	0x0

Table 10-584. Register Call Summary for Register DSI_COMPLEXIO_CFG1

MIPI Display Serial Interface

- DSI Data/Clock Configuration: [0]
- DSI Protocol Overview: [1]
- DSI SCP Interface: [2] [3] [4] [5] [6] [7] [8]
- DSI Power Control of DSI PHY and DSI PLL: [9] [10]
- DSI ULPS Configuration: [11] [12]
- DSI PHY Software Reset: [13]
- DSI PHY Pad Configuration: [14] [15] [16] [17] [18]
- DSI PHY Display Timing Configuration: [19]
- DSI Video Mode Using the DISPC Video Port: [20] [21] [22] [23] [24] [25]
- DSI Command Mode Using the DISPC Video Port: [26] [27] [28] [29] [30] [31]
- DSI Register Summary: [32] [33]

Table 10-585. DSI_COMPLEXIO_IRQSTATUS

Address Offset	0x0000 004C		
Physical Address	0x5800 404C 0x5800 904C	**Instance**	DSI1_A DSI1_C
Description	Interrupt status register – All errors from DSI PHY		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ULPSACTIVENOT_ALL1_IRQ	ULPSACTIVENOT_ALL0_IRQ	ERRCONTENTIONLP1_5_IRQ	ERRCONTENTIONLP0_5_IRQ	ERRCONTENTIONLP1_4_IRQ	ERRCONTENTIONLP0_4_IRQ	ERRCONTENTIONLP1_3_IRQ	ERRCONTENTIONLP0_3_IRQ	ERRCONTENTIONLP1_2_IRQ	ERRCONTENTIONLP0_2_IRQ	ERRCONTENTIONLP1_1_IRQ	ERRCONTENTIONLP0_1_IRQ	STATEULPS5_IRQ	STATEULPS4_IRQ	STATEULPS3_IRQ	STATEULPS2_IRQ	STATEULPS1_IRQ	ERRCONTROL5_IRQ	ERRCONTROL4_IRQ	ERRCONTROL3_IRQ	ERRCONTROL2_IRQ	ERRCONTROL1_IRQ	ERRESC5_IRQ	ERRESC4_IRQ	ERRESC3_IRQ	ERRESC2_IRQ	ERRESC1_IRQ	ERRSYNCESC5_IRQ	ERRSYNCESC4_IRQ	ERRSYNCESC3_IRQ	ERRSYNCESC2_IRQ	ERRSYNCESC1_IRQ

Bits	Field Name	Description	Type	Reset
31	ULPSACTIVENOT_ALL1_IRQ	All the ULPSActiveNOT signals corresponding to the lanes with TXULPSExit being high are high. 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
30	ULPSACTIVENOT_ALL0_IRQ	All signals ULPSActiveNOT are 0 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
29	ERRCONTENTIONLP1_5_IRQ	Contention LP1 error for the fifth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
28	ERRCONTENTIONLP0_5_IRQ	Contention LP0 error for the fifth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
27	ERRCONTENTIONLP1_4_IRQ	Contention LP1 error for the fourth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
26	ERRCONTENTIONLP0_4_IRQ	Contention LP0 error for the fourth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
25	ERRCONTENTIONLP1_3_IRQ	Contention LP1 error for the third lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
24	ERRCONTENTIONLP0_3_IRQ	Contention LP0 error for the third lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
23	ERRCONTENTIONLP1_2_IRQ	Contention LP1 error for the second lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
22	ERRCONTENTIONLP0_2_IRQ	Contention LP0 error for the second lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
21	ERRCONTENTIONLP1_1_IRQ	Contention LP1 error for the first lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
20	ERRCONTENTIONLP0_1_IRQ	Contention LP0 error for the first lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
19	STATEULPS5_IRQ	the fifth lane in ULTRALOW-POWER State 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
18	STATEULPS4_IRQ	the fourth lane in ultralow-power mode 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
17	STATEULPS3_IRQ	the third lane in ULTRALOW-POWER state 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
16	STATEULPS2_IRQ	the second lane in ULTRALOW-POWER state 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
15	STATEULPS1_IRQ	the first lane in ULTRALOW-POWER state 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
14	ERRCONTROL5_IRQ	Control error for the fifth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
13	ERRCONTROL4_IRQ	Control error for the fourth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
12	ERRCONTROL3_IRQ	Control error for the third lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
11	ERRCONTROL2_IRQ	Control error for the second lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
10	ERRCONTROL1_IRQ	Control error for the first lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
9	ERRESC5_IRQ	Escape entry error for the fifth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
8	ERRESC4_IRQ	Escape entry error for the fourth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
7	ERRESC3_IRQ	Escape entry error for the third lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
6	ERRESC2_IRQ	Escape entry error for the second lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
5	ERRESC1_IRQ	Escape entry error for the first lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
4	ERRSYNCESC5_IRQ	Low power Data transmission synchronization error for the fifth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
3	ERRSYNCESC4_IRQ	Low power Data transmission synchronization error for the fourth lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
2	ERRSYNCESC3_IRQ	Low power Data transmission synchronization error for the third lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
1	ERRSYNCESC2_IRQ	Low power Data transmission synchronization error for the second lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
0	ERRSYNCESC1_IRQ	Low power Data transmission synchronization error for the first lane 0x0: Reads: Event is false. Writes: Status bit unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0

Table 10-586. Register Call Summary for Register DSI_COMPLEXIO_IRQSTATUS

MIPI Display Serial Interface

- DSI Interrupt Requests: [0] [1]
- DSI Timers: [2]
- DSI ULPS Configuration: [3] [4]
- DSI PHY Error Handling: [5] [6] [7] [8] [9] [10] [11] [12] [13]
- DSI Video Mode Using the DISPC Video Port: [14]
- DSI Command Mode Using the DISPC Video Port: [15]
- DSI Register Summary: [16] [17]
- DSI Register Description: [18]

Table 10-587. DSI_COMPLEXIO_IRQENABLE

Address Offset	0x0000 0050		
Physical Address	0x5800 4050 0x5800 9050	**Instance**	DSI1_A DSI1_C
Description	INTERRUPT ENABLE REGISTER - All errors from DSI PHY		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ULPSACTIVENOT_ALL1_IRQ_EN	ULPSACTIVENOT_ALL0_IRQ_EN	ERRCONTENTIONLP1_5_IRQ_EN	ERRCONTENTIONLP0_5_IRQ_EN	ERRCONTENTIONLP1_4_IRQ_EN	ERRCONTENTIONLP0_4_IRQ_EN	ERRCONTENTIONLP1_3_IRQ_EN	ERRCONTENTIONLP0_3_IRQ_EN	ERRCONTENTIONLP1_2_IRQ_EN	ERRCONTENTIONLP0_2_IRQ_EN	ERRCONTENTIONLP1_1_IRQ_EN	ERRCONTENTIONLP0_1_IRQ_EN	STATEULPS5_IRQ_EN	STATEULPS4_IRQ_EN	STATEULPS3_IRQ_EN	STATEULPS2_IRQ_EN	STATEULPS1_IRQ_EN	ERRCONTROL5_IRQ_EN	ERRCONTROL4_IRQ_EN	ERRCONTROL3_IRQ_EN	ERRCONTROL2_IRQ_EN	ERRCONTROL1_IRQ_EN	ERRESC5_IRQ_EN	ERRESC4_IRQ_EN	ERRESC3_IRQ_EN	ERRESC2_IRQ_EN	ERRESC1_IRQ_EN	ERRSYNCSESC5_IRQ_EN	ERRSYNCSESC4_IRQ_EN	ERRSYNCSESC3_IRQ_EN	ERRSYNCSESC2_IRQ_EN	ERRSYNCSESC1_IRQ_EN

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Bits	Field Name	Description	Type	Reset
31	ULPSACTIVENOT_ALL1_IRQ_EN	All the ULPSActiveNOT signals corresponding to the lanes with TXULPSExit being high are high. 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
30	ULPSACTIVENOT_ALL0_IRQ_EN	All signals ULPSActiveNOT are 0 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
29	ERRCONTENTIONLP1_5_IRQ_EN	Contention LP1 error for the fifth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
28	ERRCONTENTIONLP0_5_IRQ_EN	Contention LP0 error for the fifth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
27	ERRCONTENTIONLP1_4_IRQ_EN	Contention LP1 error for the fourth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
26	ERRCONTENTIONLP0_4_IRQ_EN	Contention LP0 error for the fourth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
25	ERRCONTENTIONLP1_3_IRQ_EN	Contention LP1 error for the third lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
24	ERRCONTENTIONLP0_3_IRQ_EN	Contention LP0 error for the third lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
23	ERRCONTENTIONLP1_2_IRQ_EN	Contention LP1 error for the second lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
22	ERRCONTENTIONLP0_2_IRQ_EN	Contention LP0 error for the second lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
21	ERRCONTENTIONLP1_1_IRQ_EN	Contention LP1 error for the first lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
20	ERRCONTENTIONLP0_1_IRQ_EN	Contention LP0 error for the first lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
19	STATEULPS5_IRQ_EN	the fifth lane in ULTRALOW-POWER state 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
18	STATEULPS4_IRQ_EN	the fourth lane in ULTRALOW-POWER state 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
17	STATEULPS3_IRQ_EN	the third lane in ULTRALOW-POWER state 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
16	STATEULPS2_IRQ_EN	the second lane in ULTRALOW-POWER state 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
15	STATEULPS1_IRQ_EN	the first lane in ULTRALOW-POWER state 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
14	ERRCONTROL5_IRQ_EN	Control error for the fifth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
13	ERRCONTROL4_IRQ_EN	Control error for the fourth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
12	ERRCONTROL3_IRQ_EN	Control error for the third lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
11	ERRCONTROL2_IRQ_EN	Control error for the second lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
10	ERRCONTROL1_IRQ_EN	Control error for the first lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
9	ERRESC5_IRQ_EN	Escape entry error for the fifth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
8	ERRESC4_IRQ_EN	Escape entry error for the fourth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
7	ERRESC3_IRQ_EN	Escape entry error for the third lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
6	ERRESC2_IRQ_EN	Escape entry error for the second lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
5	ERRESC1_IRQ_EN	Escape entry error for the first lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
4	ERRSYNCSESC5_IRQ_EN	Low power Data transmission synchronization error for the fifth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
3	ERRSYNCSESC4_IRQ_EN	Low power Data transmission synchronization error for the fourth lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
2	ERRSYNCSESC3_IRQ_EN	Low power Data transmission synchronization error for the third lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0
1	ERRSYNCSESC2_IRQ_EN	Low power Data transmission synchronization error for the second lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

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Bits	Field Name	Description	Type	Reset
0	ERRSYNCSESC1_IRQ_EN	Low power Data transmission synchronization error for the first lane 0x0: Event is masked 0x1: Event generates an interrupt when it occurs	RW	0

Table 10-588. Register Call Summary for Register DSI_COMPLEXIO_IRQENABLE

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- DSI Video Mode Using the DISPC Video Port: [0]
- DSI Command Mode Using the DISPC Video Port: [1]
- DSI Register Summary: [2] [3]

Table 10-589. DSI_CLK_CTRL

Address Offset	0x0000 0054		
Physical Address	0x5800 4054 0x5800 9054	**Instance**	DSI1_A DSI1_C
Description	CLOCK CONTROL This register controls the CLOCK GENERATION. The register can be modified only when IF_EN is reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_PWR_CMD								RESERVED								LP_RX_SYNCHRO_ENABLE	LP_CLK_ENABLE	HS_MANUAL_STOP_CTRL	HS_AUTO_STOP_ENABLE	LP_CLK_NULL_PACKET_SIZE		LP_CLK_NULL_PACKET_ENABLE	CIO_CLK_ICG	DDR_CLK_ALWAYS_ON	LP_CLK_DIVISOR								
PLL_PWR_STATUS																															

Bits	Field Name	Description	Type	Reset
31:30	PLL_PWR_CMD	Command for power control of the DSI PLL Control module 0x0: Command to change to OFF state 0x1: Command to change to ON state for PLL only (HSDIVISER is OFF) 0x2: Command to change to ON state for both PLL and HSDIVISER 0x3: Command to change to ON state for both PLL and HSDIVISER (no clock output to the DSI PHY)	RW	0x0
29:28	PLL_PWR_STATUS	Status of the power control of the DSI PLL Control module Read 0x0: DSI PLL Control module in OFF state Read 0x1: DSI PLL Control module in ON state for PLL only (HSDIVISER is OFF) Read 0x2: DSI PLL Control module in ON state for both PLL and HSDIVISER Read 0x3: DSI PLL Control module in ON state for both PLL and HSDIVISER (no clock output to the DSI PHY)	R	0x0
27:22	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
21	LP_RX_SYNCHRO_ENABLE	Defines if the functional is higher or lower than 30 MHz. The information is used to define synchronization to be used for RxValidEsc. 0x0: The DSI functional clock is equal or slower than 30 MHz. The synchronization is falling/rising. 0x1: The DSI functional clock is higher than 30 MHz. The synchronization is rising/rising.	RW	0
20	LP_CLK_ENABLE	Controls the gating of the TXCLKESC clock. 0x0: Disabled. The clock is not generated. The value of LP_CLK_DIVISOR is not used and does not need to be programmed. 0x1: Enabled. The clock is generated. The value of LP_CLK_DIVISOR is used and needs to be programmed.	RW	0
19	HS_MANUAL_STOP_CTRL	In case HS_AUTO_STOP_ENABLE=0, the bit field allows manual control of the assertion/de-assertion of the signal DSIStopClk by the user. 0x0: DSIStopClk de-assertion unconditionally. 0x1: DSIStopClk assertion unconditionally.	RW	0
18	HS_AUTO_STOP_ENABLE	Enables the automatic assertion/de-assertion of DSIStopClk signal. 0x0: Auto mode disabled. 0x1: Auto mode enabled.	RW	0
17:16	LP_CLK_NULL_PACKET_SIZE	Indicates the size of LP NULL Packets to be sent automatically when after the last LP packet transfer. It is used by the receiver to drain its internal pipeline. The valid values are from 0 to 3 bytes for the payload size.	RW	0x0
15	LP_CLK_NULL_PACKET_ENABLE	Enables the generation of NULL packet in low speed. 0x0: Disabled. The NULL packet is not sent in LP mode after the last LP packet. 0x1: Enabled. The NULL packet is sent in LP mode after the last LP packet.	RW	0
14	CIO_CLK_ICG	Gates SCPClk clock provided to DSI_PHY_DSS_x and PLL-CTRL module. 0x0: Disabled. SCPClk is not generated. It remains at 0. 0x1: Enabled. SCPClk is generated (OCP_CLK/4)	RW	0
13	DDR_CLK_ALWAYS_ON	Defines if the DDR clock is also sent when there is no HS packets sent to the peripheral (low-power mode). So TXRequest for the clock lane is not de-asserted. 0x0: Disabled. The DDR clock is only provided when HS packets are sent. 0x1: Enabled. The DDR clock is always sent to the peripheral regardless of the state of the data lanes (HS or LS mode).	RW	0
12:0	LP_CLK_DIVISOR	Defines the ratio to be used for the generation of the low-power mode clock from DSI functional clock. The supported values are from 1 to 8191(the value 0 is invalid). The output frequency shall be in the range between 20 MHz and 32 kHz.	RW	0x0001

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Table 10-590. Register Call Summary for Register DSI_CLK_CTRL

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- DSI Transfer Modes: [0]
- DSI Clock Requirements: [1] [2] [3] [4] [5] [6] [7]
- DSI Power Management: [8]
- DSI Power Control of DSI PHY and DSI PLL: [9] [10] [11] [12] [13] [14] [15] [16]
- DSI ULPS Configuration: [17]
- DSI PHY Pad Configuration: [18] [19]
- DSI PHY Display Timing Configuration: [20]
- DSI Video Mode Using the DISPC Video Port: [21] [22] [23] [24] [25] [26] [27] [28]
- DSI Command Mode Using the DISPC Video Port: [29] [30] [31] [32] [33] [34] [35] [36]
- DSI Register Summary: [37] [38]
- DSI Register Description: [39] [40]

Table 10-591. DSI_TIMING1

Address Offset	0x0000 0058		
Physical Address	0x5800 4058 0x5800 9058	**Instance**	DSI1_A DSI1_C
Description	TIMING1 REGISTER This register controls the DSI Protocol Engine module timers. Any bit field can be modified while DSI_CTRL[0] IF_EN is set to '1'. It is used to indicate the number of DSI1_A_CLK and DSI1_A_CLK functional clocks cycles for the timers FORCE_TX_STOP_TIMER and TA_TO_TIMER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TA_TO	TA_TO_X16	TA_TO_X8	TA_TO_COUNTER													FORCE_TX_STOP_MODE_IO	STOP_STATE_X16_IO	STOP_STATE_X4_IO	STOP_STATE_COUNTER_IO												

Bits	Field Name	Description	Type	Reset
31	TA_TO	Enables the turn-around timer 0x0: Turn-around counter is disabled. 0x1: Turn-around counter is enabled (required to receive TA interrupt in case the turn-around procedure is not successful).	RW	0
30	TA_TO_X16	Multiplication factor for the number of DSI_CLK functional clocks cycles defined in TA_TO_COUNTER bit field 0x0: The number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER is multiplied by 1x 0x1: The number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER is multiplied by 16x	RW	1
29	TA_TO_X8	Multiplication factor for the number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER bit field 0x0: The number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER is multiplied by 1x 0x1: The number of DSI_CLK functional clock cycles defined in TA_TO_COUNTER is multiplied by 8x	RW	1

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Bits	Field Name	Description	Type	Reset
28:16	TA_TO_COUNTER	Turn around counter. It indicates the number of DSI_CLK function clock to wait for the change of the Direction PPI signal according to the TurnRequest signal The value is from 0 to 8191.	RW	0x1FFF
15	FORCE_TX_STOP_MODE_IO	Control of ForceTxStopMode signal 0x0: Deassertion of ForceTxStopMode. The hardware reset the bit at the end of the ForceTXStopMode assertion. The software can reset the bit in order to stop the assertion of the ForceTXStopMode signal prior to the completion of the period. 0x1: Assertion of ForceTxStopMode	RW	0
14	STOP_STATE_X16_IO	Multiplication factor for the number of DSI_CLK functional clock cycles defined in STOP_STATE_COUNTER_IO bit field 0x0: The number of DSI_CLK functional clock cycles defined in STOP_STATE _COUNTER_IO is multiplied by 1x 0x1: The number of DSI_CLK functional clock cycles defined in STOP_STATE _COUNTER_IO is multiplied by 16x	RW	1
13	STOP_STATE_X4_IO	Multiplication factor for the number of DSI_CLK functional clock cycles defined in STOP_STATE_COUNTER_IO bit field 0x0: The number of DSI_CLK functional clock cycles defined in STOP_STATE _COUNTER is multiplied by 1x 0x1: The number of DSI_CLK functional clock cycles defined in STOP_STATE _COUNTER_IO is multiplied by 4x	RW	1
12:0	STOP_STATE_COUNTER_IO	Stop state counter. It indicates the number of DSI_CLK function clock to assert ForceTXStopMode signal. The value is from 0 to 8191.	RW	0x1FFF

Table 10-592. Register Call Summary for Register DSI_TIMING1

MIPI Display Serial Interface

- DSI Timers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- DSI Video Mode Using the DISPC Video Port: [10] [11] [12]
- DSI Command Mode Using the DISPC Video Port: [13] [14] [15] [16] [17] [18]
- DSI Register Summary: [19] [20]

Table 10-593. DSI_TIMING2

Address Offset	0x0000 005C		
Physical Address	0x5800 405C 0x5800 905C	**Instance**	DSI1_A DSI1_C
Description	TIMING2 REGISTER This register controls the DSI Protocol Engine module timers. Any bit field can be modified while DSI_CTRL[0] IF_EN is set to '1'. It is used to indicate the number of DSI_FCLK clock cycles for the timer LP_RX_TIMER and the number of BYTE_CLK functional clock cycles for the timer HS_TX_TIMER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS_TX_TO	HS_TX_TO_X64	HS_TX_TO_X16	HS_TX_TO_COUNTER													LP_RX_TO	LP_RX_TO_X16	LP_RX_TO_X4	LP_RX_TO_COUNTER												

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Bits	Field Name	Description	Type	Reset
31	HS_TX_TO	Enables the HS TX timer. 0x0: Time-out counter is disabled. 0x1: Time-out counter is enabled (required to receive TA interrupt in case the turn-around procedure is not successful).	RW	0
30	HS_TX_TO_X64	Multiplication factor for the number of BYTE_CLK functional clock cycles defined in HS_TX_COUNTER bit field. BYTE_CLK is a high speed transmit byte clock signal generated by the DSI_PHY_DSS_x. 0x0: The number of BYTE_CLK functional clock cycles defined in HS_TX_TO_COUNTER is multiplied by 1x 0x1: The number of BYTE_CLK functional clock cycles defined in HS_TX_TO_COUNTER is multiplied by 64x	RW	1
29	HS_TX_TO_X16	Multiplication factor for the number of BYTE_CLK functional clock cycles defined in HS_TX_COUNTER bit 0x0: The number of BYTE_CLK functional clock cycles defined in HS_TX_TO_COUNTER is multiplied by 1x 0x1: The number of BYTE_CLK functional clock cycles defined in HS_TX_TO_COUNTER is multiplied by 16x	RW	1
28:16	HS_TX_TO_COUNTER	HS_TX_TIMER counter. It indicates the number of BYTE_CLK function clock for the HS TX timer. The value is from 0 to 8191.	RW	0x1FFF
15	LP_RX_TO	Enables the LP RX timer. 0x0: Turn-around counter is disabled. 0x1: Turn-around counter is enabled (required to receive TA interrupt in case the turn-around procedure is not successful).	RW	0
14	LP_RX_TO_X16	Multiplication factor for the number of DSI_FCLK clock cycles defined in LP_RX_COUNTER bit field 0x0: The number of DSI_FCLK clock cycles defined in LP_RX_TO_COUNTER is multiplied by 1x 0x1: The number of DSI_FCLK clock cycles defined in LP_RX_TO_COUNTER is multiplied by 16x	RW	1
13	LP_RX_TO_X4	Multiplication factor for the number of DSI_FCLK clock cycles defined in LP_RX_COUNTER bit 0x0: The number of DSI_FCLK clock cycles defined in LP_RX_TO_COUNTER is multiplied by 1x 0x1: The number of DSI_FCLK clock cycles defined in LP_RX_TO_COUNTER is multiplied by 4x	RW	1
12:0	LP_RX_TO_COUNTER	LP_RX_TIMER counter. It indicates the number of DSI_FCLK clock for the LP RX timer. The value is from 0 to 8191.	RW	0x1FFF

Table 10-594. Register Call Summary for Register DSI_TIMING2

MIPI Display Serial Interface

- DSI Timers: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- DSI Video Mode Using the DISPC Video Port: [9] [10] [11] [12]
- DSI Command Mode Using the DISPC Video Port: [13] [14] [15] [16] [17] [18]
- DSI Register Summary: [19] [20]

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Table 10-595. DSI_VM_TIMING1

Address Offset	0x0000 0060		
Physical Address	0x5800 4060 0x5800 9060	**Instance**	DSI1_A DSI1_C
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSA								HFP								HBP															

Bits	Field Name	Description	Type	Reset
31:24	HSA	Defines the horizontal Sync active period used in video mode in number of byte clock cycles (TXBYTECLKHS clock) The supported values are from 0 to 255.	RW	0x00
23:12	HFP	Defines the horizontal front porch used in video mode in number of byte clock cycles (TXBYTECLKHS clock) The supported values are from 0 to 4095	RW	0x000
11:0	HBP	Defines the horizontal back porch used in video mode in number of byte clock cycles (TXBYTECLKHS clock) The supported values are from 0 to 4095	RW	0x000

Table 10-596. Register Call Summary for Register DSI_VM_TIMING1

MIPI Display Serial Interface

- DSI Blanking: [0]
- DSI Transfer Modes: [1]
- DSI Video Mode Using the DISPC Video Port: [2] [3] [4]
- DSI Register Summary: [5] [6]

Table 10-597. DSI_VM_TIMING2

Address Offset	0x0000 0064		
Physical Address	0x5800 4064 0x5800 9064	**Instance**	DSI1_A DSI1_C
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOW_SYNC				VSA								VFP								VBP							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOW_SYNC	Number of BYTE clock cycles for the synchronization window. An interrupt for synchronization lost is generated when the received synchornization on video port is not inside the window. DSI does not change its own timings if the synch is inside the window. The valid values are from 4 to 15.	RW	0x0

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Bits	Field Name	Description	Type	Reset
23:16	VSA	Defines the vertical Sync active period used in video mode in number of lines. The supported values are from 0 to 255 It is used to generate the short packet for End of Vertical synchronization.(1)	RW	0x00
15:8	VFP	Defines the vertical front porch used in video mode in number of lines. The supported values are from 0 to 255	RW	0x00
7:0	VBP	Defines the vertical back porch used in video mode in number of lines. The supported values are from 0 to 255	RW	0x00

(1) In DSI video mode, if the VSA bit field in DSI_VM_TIMING2 is set to 0x0, no vertical synchronization packet will be sent, even if VP_VSYNC_START is set to 0x1 in DSI_CTRL.

Table 10-598. Register Call Summary for Register DSI_VM_TIMING2

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- DSI Transfer Modes: [0]
- DSI Video Port Interface: [1] [2]
- DSI Video Mode Using the DISPC Video Port: [3] [4] [5] [6]
- DSI Register Summary: [7] [8]

Table 10-599. DSI_VM_TIMING3

Address Offset	0x0000 0068		
Physical Address	0x5800 4068 0x5800 9068	**Instance**	DSI1_A DSI1_C
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TL																VACT															

Bits	Field Name	Description	Type	Reset
31:16	TL	Defines the number of length of the line in video mode in number of byte clock cycles (TXBYTECLKHS clock) The supported values are from 0 to 8192. The values from 8193 to 65535 are not supported.	RW	0x0000
15:0	VACT	Defines the number of active lines used in video mode. The supported values are from 0 to 65535	RW	0x0000

Table 10-600. Register Call Summary for Register DSI_VM_TIMING3

MIPI Display Serial Interface

- DSI Video Port Interface: [0]
- DSI Video Mode Using the DISPC Video Port: [1] [2]
- DSI Register Summary: [3] [4]

Table 10-601. DSI_CLK_TIMING

Address Offset	0x0000 006C		
Physical Address	0x5800 406C 0x5800 906C	**Instance**	DSI1_A DSI1_C
Description	CLOCK TIMING REGISTER This register controls the DSI Protocol Engine module timers. This register shall not be modified while DSI_CTRL.IF_EN is set to '1'.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DDR_CLK_PRE								DDR_CLK_POST							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	DDR_CLK_PRE	Indicates the number of TXBYTECLKHS clock cycles between the start of the DDR clock and the assertion of the data request signal. The values from 1 to 255 are valid. The value 0 is reserved. The value is not used if DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON is set to '1' since the DDR clock is always present.	RW	0x01
7:0	DDR_CLK_POST	Indicates the number of TXBYTECLKHS clock cycles after the de-assertion of the data request signal and the stop of the DDR clock. The values from 1 to 255 are valid. The value 0 is reserved. The value is not used if DSI_CLK_CTRL[13] DDR_CLK_ALWAYS_ON is set to '1' since the DDR clock is always present.	RW	0x01

Table 10-602. Register Call Summary for Register DSI_CLK_TIMING

MIPI Display Serial Interface

- DSI Clock Requirements: [0] [1] [2] [3]
- DSI Video Mode Using the DISPC Video Port: [4] [5]
- DSI Command Mode Using the DISPC Video Port: [6] [7]
- DSI Register Summary: [8] [9]

Table 10-603. DSI_TX_FIFO_VC_SIZE

Address Offset	0x0000 0070		
Physical Address	0x5800 4070 0x5800 9070	**Instance**	DSI1_A DSI1_C
Description	Defines the corresponding memory entries allocated for each virtual channel. The virtual channel shall be disabled in order to allocate/un-allocate some entries in the TX FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VC3_FIFO_SIZE				RESERVED	VC3_FIFO_ADD			VC2_FIFO_SIZE				RESERVED	VC2_FIFO_ADD			VC1_FIFO_SIZE				RESERVED	VC1_FIFO_ADD			VC0_FIFO_SIZE				RESERVED	VC0_FIFO_ADD		

Bits	Field Name	Description	Type	Reset
31:28	VC3_FIFO_SIZE	Size of the FIFO allocated for virtual channel 3. For a complete description, refer to Table 10-522, *Virtual Channel TX FIFO Size Values.*	RW	0x0
27	RESERVED		R	0
26:24	VC3_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 3. For a complete description, refer to Table 10-523, *Virtual Channel TX FIFO Start Address.*	RW	0x0
23:20	VC2_FIFO_SIZE	Size of the FIFO allocated for virtual channel 2. For a complete description, refer to Table 10-522, *Virtual Channel TX FIFO Size Values.*	RW	0x0
19	RESERVED		R	0
18:16	VC2_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 2. For a complete description, refer to Table 10-523, *Virtual Channel TX FIFO Start Address.*	RW	0x0

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Bits	Field Name	Description	Type	Reset
15:12	VC1_FIFO_SIZE	Size of the FIFO allocated for virtual channel 1. For a complete description, refer to Table 10-522, *Virtual Channel TX FIFO Size Values.*	RW	0x0
11	RESERVED		R	0
10:8	VC1_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 1. For a complete description, refer to Table 10-523, *Virtual Channel TX FIFO Start Address.*	RW	0x0
7:4	VC0_FIFO_SIZE	Size of the FIFO allocated for virtual channel 0. For a complete description, refer to Table 10-522, *Virtual Channel TX FIFO Size Values.*	RW	0x0
3	RESERVED		R	0
2:0	VC0_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 0. For a complete description, refer to Table 10-523, *Virtual Channel TX FIFO Start Address.*	RW	0x0

Table 10-604. Register Call Summary for Register DSI_TX_FIFO_VC_SIZE

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1] [2] [3] [4]
- DSI Command Mode Using the DISPC Video Port: [5]
- DSI Register Summary: [6] [7]

Table 10-605. DSI_RX_FIFO_VC_SIZE

Address Offset	0x0000 0074		
Physical Address	0x5800 4074 0x5800 9074	**Instance**	DSI1_A DSI1_C
Description	Defines the corresponding memory entries allocated for each virtual channel and the addresses. The virtual channel shall be disabled in order to allocate/un-allocate some entries in the RX FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VC3_FIFO_SIZE				RESERVED			VC3_FIFO_ADD				VC2_FIFO_SIZE				RESERVED		VC2_FIFO_ADD				VC1_FIFO_SIZE				RESERVED		VC1_FIFO_ADD				VC0_FIFO_SIZE				RESERVED		VC0_FIFO_ADD	

Bits	Field Name	Description	Type	Reset
31:28	VC3_FIFO_SIZE	Size of the FIFO allocated for virtual channel 3. For a complete description, refer to Table 10-524, *Virtual Channel RX FIFO Size Values.*	RW	0x0
27	RESERVED		R	0
26:24	VC3_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 3. For a complete description, refer to Table 10-525, *Virtual Channel RX FIFO Start Address.*	RW	0x0
23:20	VC2_FIFO_SIZE	Size of the FIFO allocated for virtual channel 2. For a complete description, refer to Table 10-524, *Virtual Channel RX FIFO Size Values.*	RW	0x0
19	RESERVED		R	0
18:16	VC2_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 2. For a complete description, refer to Table 10-525, *Virtual Channel RX FIFO Start Address.*	RW	0x0
15:12	VC1_FIFO_SIZE	Size of the FIFO allocated for virtual channel 1. For a complete description, refer to Table 10-524, *Virtual Channel RX FIFO Size Values.*	RW	0x0
11	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
10:8	VC1_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 1. For a complete description, refer to Table 10-525, *Virtual Channel RX FIFO Start Address.*	RW	0x0
7:4	VC0_FIFO_SIZE	Size of the FIFO allocated for virtual channel 0. For a complete description, refer to Table 10-524, *Virtual Channel RX FIFO Size Values.*	RW	0x0
3	RESERVED		R	0
2:0	VC0_FIFO_ADD	Address of the space allocated in the FIFO for virtual channel 0. For a complete description, refer to Table 10-525, *Virtual Channel RX FIFO Start Address.*	RW	0x0

Table 10-606. Register Call Summary for Register DSI_RX_FIFO_VC_SIZE

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1] [2]
- DSI Command Mode Using the DISPC Video Port: [3]
- DSI Register Summary: [4] [5]

Table 10-607. DSI_COMPLEXIO_CFG2

Address Offset	0x0000 0078		
Physical Address	0x5800 4078 0x5800 9078	**Instance**	DSI1_A DSI1_C
Description	COMPLEXIO CONFIGURATION REGISTER for the DSI PHY This register contains the lane configuration for the ULPS for each lane.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LP_BUSY	HS_BUSY	RESERVED						LANE5_ULPS_SIG2	LANE4_ULPS_SIG2	LANE3_ULPS_SIG2	LANE2_ULPS_SIG2	LANE1_ULPS_SIG2	LANE5_ULPS_SIG1	LANE4_ULPS_SIG1	LANE3_ULPS_SIG1	LANE2_ULPS_SIG1	LANE1_ULPS_SIG1

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	LP_BUSY	Indicates when there are still pending operations for VCs configured for LP mode. Forced to 1 when at least one VC is enabled and configured for LP mode. Read 0x0: LP logic is idle Read 0x1: LP logic is active	R	0
16	HS_BUSY	Indicates when there are still pending operations for VCs configured for HS mode. Forced to 1 when at least one VC is enabled and configured for HS mode. Read 0x0: HS logic is idle Read 0x1: HS logic is active	R	0
15:10	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
9	LANE5_ULPS_SIG2	Enables the ULPS for the lane 5. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 5 is a data lane. The state of the signal TxUlpsClk is changed if lane 5 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0
8	LANE4_ULPS_SIG2	Enables the ULPS for the lane 4. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 4 is a data lane. The state of the signal TxUlpsClk is changed if lane 4 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0
7	LANE3_ULPS_SIG2	Enables the ULPS for the lane 3. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 3 is a data lane. The state of the signal TxUlpsClk is changed if lane 3 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0

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Bits	Field Name	Description	Type	Reset
6	LANE2_ULPS_SIG2	Enables the ULPS for the lane 2. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 2 is a data lane. The state of the signal TxUlpsClk is changed if lane 2 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0
5	LANE1_ULPS_SIG2	Enables the ULPS for the lane 1. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxRequestEsc is changed if lane 1 is a data lane. The state of the signal TxUlpsClk is changed if lane 1 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc.	RW	0
4	LANE5_ULPS_SIG1	Enables the ULPS for the lane 5. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 5 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0

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Bits	Field Name	Description	Type	Reset
3	LANE4_ULPS_SIG1	Enables the ULPS for the lane 4. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 4 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0
2	LANE3_ULPS_SIG1	Enables the ULPS for the lane 3. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 3 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0
1	LANE2_ULPS_SIG1	Enables the ULPS for the lane 2. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 2 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective. WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0
0	LANE1_ULPS_SIG1	Enables the ULPS for the lane 1. The hardware shall change the state of the lane to ULPS only when it is in stop state and there is no data pending inside the DSI protocol engine and the DSI protocol engine has control of the bus (BTA has not been sent). The state of the signal TxULPSExit is changed if the lane 1 is a clock lane. There will be a latency depending on the frequency of TxClkExc. This bit should be read back to confirm a write has been effective. 0x0: READ: Inactive state effective. WRITE: Request to change to inactive state 0x1: READ: Active state effective WRITE: Change request to active. If the lane is a data lane, TxRequestEsc is asserted and synchronously TxUlpsEsc is asserted for one period of TxClkEsc	RW	0

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Table 10-608. Register Call Summary for Register DSI_COMPLEXIO_CFG2

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- DSI ULPS Configuration: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]
- DSI Register Summary: [25] [26]

Table 10-609. DSI_RX_FIFO_VC_FULLNESS

Address Offset	0x0000 007C		
Physical Address	0x5800 407C 0x5800 907C	**Instance**	DSI1_A DSI1_C
Description	Defines the fullness of each space allocated for each virtual channel.		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
VC3_FIFO_FULLNESS	VC2_FIFO_FULLNESS	VC1_FIFO_FULLNESS	VC0_FIFO_FULLNESS

Bits	Field Name	Description	Type	Reset
31:24	VC3_FIFO_FULLNESS	Fullness of the FIFO allocated for virtual channel 3.The valid values are from 0 to DSI_GNQ[5:3] RX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[5:3] RX_FIFODEPTH x33-bit.	R	0x00
23:16	VC2_FIFO_FULLNESS	Fullness of the FIFO allocated for virtual channel 2.The valid values are from 0 to DSI_GNQ[5:3] RX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[5:3] RX_FIFODEPTH x33-bit.	R	0x00
15:8	VC1_FIFO_FULLNESS	Fullness of the FIFO allocated for virtual channel 1.The valid values are from 0 to DSI_GNQ[5:3] RX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[5:3] RX_FIFODEPTH x33-bit.	R	0x00
7:0	VC0_FIFO_FULLNESS	Fullness of the FIFO allocated for virtual channel 0.The valid values are from 0 to DSI_GNQ[5:3] RX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[5:3] RX_FIFODEPTH x33-bit.	R	0x00

Table 10-610. Register Call Summary for Register DSI_RX_FIFO_VC_FULLNESS

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- DSI Transfer Modes: [0]
- DSI Register Summary: [1] [2]

Table 10-611. DSI_VM_TIMING4

Address Offset	0x0000 0080		
Physical Address	0x5800 4080 0x5800 9080	**Instance**	DSI1_A DSI1_C
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	HSA_HS_INTERLEAVING	HFP_HS_INTERLEAVING	HBP_HS_INTERLEAVING

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	HSA_HS_INTERLEAVING	Defines the number of TXBYTECLKHS clock cycles that can be used for interleaving High Speed command mode packet into Video Mode stream during HSA blanking period. The supported values are from 0 to 255.	RW	0x00
15:8	HFP_HS_INTERLEAVING	Defines the number of TXBYTECLKHS clock cycles that can be used for interleaving High Speed command mode packet into Video Mode stream during HFP blanking period. The supported values are from 0 to 255	RW	0x00
7:0	HBP_HS_INTERLEAVING	Defines the number of TXBYTECLKHS clock cycles that can be used for interleaving High Speed command mode packet into Video Mode stream during HBP blanking period. The supported values are from 0 to 255	RW	0x00

Table 10-612. Register Call Summary for Register DSI_VM_TIMING4

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1] [2]
- DSI Register Summary: [3] [4]

Table 10-613. DSI_TX_FIFO_VC_EMPTINESS

Address Offset	0x0000 0084		
Physical Address	0x5800 4084 0x5800 9084	**Instance**	DSI1_A DSI1_C
Description	Defines the emptiness of each space allocated for each virtual channel.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VC3_FIFO_EMPTINESS								VC2_FIFO_EMPTINESS								VC1_FIFO_EMPTINESS								VC0_FIFO_EMPTINESS							

Bits	Field Name	Description	Type	Reset
31:24	VC3_FIFO_EMPTINESS	Emptiness of the FIFO allocated for virtual channel 3.The valid values are from 0 to DSI_GNQ[2:0] TX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[2:0] TX_FIFODEPTH x33-bit.	R	0x00
23:16	VC2_FIFO_EMPTINESS	Emptiness of the FIFO allocated for virtual channel 2.The valid values are from 0 to DSI_GNQ[2:0] TX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[2:0] TX_FIFODEPTH x33-bit.	R	0x00
15:8	VC1_FIFO_EMPTINESS	Emptiness of the FIFO allocated for virtual channel 1.The valid values are from 0 to DSI_GNQ[2:0] TX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[2:0] TX_FIFODEPTH x33-bit.	R	0x00
7:0	VC0_FIFO_EMPTINESS	Emptiness of the FIFO allocated for virtual channel 0.The valid values are from 0 to DSI_GNQ[2:0] TX_FIFODEPTH-1 corresponding to 1x33-bit,...up to DSI_GNQ[2:0] TX_FIFODEPTH x33-bit.	R	0x00

Table 10-614. Register Call Summary for Register DSI_TX_FIFO_VC_EMPTINESS

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1]
- DSI Register Summary: [2] [3]

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Table 10-615. DSI_VM_TIMING5

Address Offset	0x0000 0088		
Physical Address	0x5800 4088 0x5800 9088	**Instance**	DSI1_A DSI1_C
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	HSA_LP_INTERLEAVING	HFP_LP_INTERLEAVING	HBP_LP_INTERLEAVING

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	HSA_LP_INTERLEAVING	Defines the number of bytes of Low Power command mode packets that can be sent on PPI link during HSA blanking period. The supported values are from 0 to 255.	RW	0x00
15:8	HFP_LP_INTERLEAVING	Defines the number of bytes of Low Power command mode packets that can be sent on PPI link during HFP blanking period. The supported values are from 0 to 255	RW	0x00
7:0	HBP_LP_INTERLEAVING	Defines the number of bytes of Low Power command mode packets that can be sent on PPI link during HBP blanking period. The supported values are from 0 to 255	RW	0x00

Table 10-616. Register Call Summary for Register DSI_VM_TIMING5

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1] [2]
- DSI Register Summary: [3] [4]

Table 10-617. DSI_VM_TIMING6

Address Offset	0x0000 008C		
Physical Address	0x5800 408C 0x5800 908C	**Instance**	DSI1_A DSI1_C
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
BL_HS_INTERLEAVING		BL_LP_INTERLEAVING	

Bits	Field Name	Description	Type	Reset
31:16	BL_HS_INTERLEAVING	Defines the number of TXBYTECLKHS clock cycles that can be used for interleaving High Speed command mode packet into Video Mode stream during blanking periods during VSA, VBP, VFP periods inside one video frame on PPI link. The supported values are from 0 to 65535 .	RW	0x0000
15:0	BL_LP_INTERLEAVING	Defines the maximum number of bytes of Low Power command mode packets that can be sent on PPI link during blanking periods during VSA, VBP or VFP periods inside one video frame on PPI link. The supported values are from 0 to 65535	RW	0x0000

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Table 10-618. Register Call Summary for Register DSI_VM_TIMING6

MIPI Display Serial Interface

- DSI Transfer Modes: [0] [1]
- DSI Video Port Interface: [2]
- DSI Register Summary: [3] [4]

Table 10-619. DSI_VM_TIMING7

Address Offset	0x0000 0090		
Physical Address	0x5800 4090 0x5800 9090	**Instance**	DSI1_A DSI1_C
Description	Defines the minimum number of HS bytes clock cycles that are required to allow for the delays in entering and exiting HS mode. The supported values are from 0 to 65535		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENTER_HS_MODE_LATENCY																EXIT_HS_MODE_LATENCY															

Bits	Field Name	Description	Type	Reset
31:16	ENTER_HS_MODE_LATENCY	Defines the number of TXBYTECLKHS clock cycles necessary for entering to HS mode. It corresponds to the delay in number of HS clock cycles from assertion of TxRequestHS signal to 1 until assertion of TxReadyHS signal to 1. The supported values are from 0 to 65535 .	RW	0x0000
15:0	EXIT_HS_MODE_LATENCY	Defines the number of TXBYTECLKHS clock cycles necessary for exiting from HS mode. It corresponds to the maximum delay in number of TXBYTECLKHS clock from de-assertion of TxRequestHS signal until PPI link is in LP-11 state from which a new entrance to HS mode can be initiated which does not take more than ENTER_HS_MODE_LATENCY clock cycles. The supported values are from 0 to 65535	RW	0x0000

Table 10-620. Register Call Summary for Register DSI_VM_TIMING7

MIPI Display Serial Interface

- DSI Clock Requirements: [0] [1] [2] [3]
- DSI Video Mode Using the DISPC Video Port: [4] [5]
- DSI Register Summary: [6] [7]

Table 10-621. DSI_STOPCLK_TIMING

Address Offset	0x0000 0094		
Physical Address	0x5800 4094 0x5800 9094	**Instance**	DSI1_A DSI1_C
Description	Number of functional clock cycles to wait for TXBYTECLKHS to stop/start after change in DSIStopClk signal		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DSI_STOPCLK_LATENCY							

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	DSI_STOPCLK_LATENCY	Clock gating latency from DSI Protocol to TXBYTECLKHS	RW	0x80

Table 10-622. Register Call Summary for Register DSI_STOPCLK_TIMING

MIPI Display Serial Interface

- DSI Power Control of DSI PHY and DSI PLL: [0] [1]
- DSI Register Summary: [2] [3]

Table 10-623. DSI_CTRL2

Address Offset	0x0000 0098		
Physical Address	0x5800 4098 0x5800 9098	**Instance**	DSI1_A DSI1_C
Description	Additional control bits for use with Video Port 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		LINE_BUFFER		VP_VSYNC_POL		VP_HSYNC_POL		VP_DE_POL		VP_CLK_POL		VP_DATA_BUS_WIDTH			RESERVED		VP_CLK_RATIO		RESERVED				

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:12	LINE_BUFFER	Number of line buffers to be used while receiving data on the video port. The valid values are from 0 to DSI_GNQ[23:22] VP2_NB_LINE_BUFFER. 0x0: No line buffer 0x1: 1 line buffer 0x2: 2 line buffers	RW	0x0
11	VP_VSYNC_POL	VP vertical synchronization signal polarity 0x0: VSYNC signal on the video port is active low. 0x1: VSYNC signal on the video port is active high.	RW	0
10	VP_HSYNC_POL	VP horizontal synchronization signal polarity 0x0: HSYNC signal on the video port is active low. 0x1: HSYNC signal on the video port is active high.	RW	0
9	VP_DE_POL	VP data enable signal polarity 0x0: DE signal on the video port is active low. 0x1: DE signal on the video port is active high.	RW	0
8	VP_CLK_POL	VP pixel clock polarity 0x0: The DSI Protocol Engine module captures the data on the VP on the pixel clock falling edge. The module connected to the VP shall drive the data on the pixel clock rising edge. 0x1: The DSI Protocol Engine module captures the data on the VP on the pixel clock raising edge. The module connected to the VP shall drive the data on the pixel clock falling edge.	RW	1

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Bits	Field Name	Description	Type	Reset
7:6	VP_DATA_BUS_WIDTH	Defines the size of the video port data bus 0x0: 16-bits data width (LSB of the 24-bit video port data bus) 0x1: 18-bits data width (LSB of the 24-bit video port data bus) 0x2: 24-bits data width (LSB of the 24-bit video port data bus)	RW	0x0
5	RESERVED		R	0
4	VP_CLK_RATIO	The field indicates the clock ratio between VP_CLK and VP_PCLK. The clock VP_PCLK is generated from VP_CLK. It is divided down. The information is only used when the video port is used to provide data in command mode. In the case of video mode, it is not used. 0x0: The clock VP_PCLK is the clock VP_CLK divided by 2. The duty cycle of VP_PCLK is 50/50. 0x1: The clock VP_PCLK is the clock VP_CLK divided by 3 or more. The duty cycle of VP_PCLK is not 50/50 for odd ratio numbers (3,5,7,...).	RW	0
3:0	RESERVED		R	0x0

Table 10-624. Register Call Summary for Register DSI_CTRL2

MIPI Display Serial Interface
- DSI Video Port Interface: [0] [1] [2] [3]
- DSI Register Summary: [4] [5]
- DSI Register Description: [6] [7] [8] [9]

Table 10-625. DSI_VM_TIMING8

Address Offset	0x0000 009C		
Physical Address	0x5800 409C 0x5800 909C	**Instance**	DSI1_A DSI1_C
Description	VIDEO MODE TIMING REGISTER This register defines the video mode timing.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														HFPX	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	HFPX	Extension to the HFP register. Additional bits added to MSB.	RW	0x0

Table 10-626. Register Call Summary for Register DSI_VM_TIMING8

MIPI Display Serial Interface
- DSI Blanking: [0]
- DSI Transfer Modes: [1]
- DSI Register Summary: [2] [3]

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Table 10-627. DSI_TE_HSYNC_WIDTH_j

Address Offset	0x0000 00A0 + (0xc * j)	**Index**	j = 0 to 1
Physical Address	0x5800 40A0 + (0xc * j) 0x5800 90A0 + (0xc * j)	**Instance**	DSI1_A DSI1_C
Description	The register configures the TE HSYNC minimum pulse width for TE0 and TE1 CMOS signals The input TE signal is asynchronous and needs to be resynchronizred to DSI_CLK clock domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MIN_HSYNC_PULSE_WIDTH																RESERVED							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:8	MIN_HSYNC_PULSE_WIDTH	Programmable min HSYNC pulse width Minimum HSYNC pulse width. Number of DSI_CLK clock cycles times 256 to determine when HSYNC pulse occurs. The value 0 is invalid.	RW	0x001
7:0	RESERVED		R	0x00

Table 10-628. Register Call Summary for Register DSI_TE_HSYNC_WIDTH_j

MIPI Display Serial Interface

- DSI PHY Triggers: [0] [1] [2] [3] [4] [5]
- DSI Register Summary: [6] [7]

Table 10-629. DSI_TE_VSYNC_WIDTH_j

Address Offset	0x0000 00A4 + (0xc * j)	**Index**	j = 0 to 1
Physical Address	0x5800 40A4 + (0xc * j) 0x5800 90A4 + (0xc * j)	**Instance**	DSI1_A DSI1_C
Description	The register configures the TE VSYNC minimum pulse width for TE0 and TE1 CMOS signals The input TE signal is asynchronous and needs to be resynchronizred to DSI_CLK clock domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MIN_VSYNC_PULSE_WIDTH																RESERVED							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:8	MIN_VSYNC_PULSE_WIDTH	Programmable min VSYNC pulse width Minimum VSYNC pulse width. Number of DSI_CLK cycles times 256 to determine when VSYNC pulse occurs. The value 0 is invalid. The value shall be greater than MIN_HSYNC_PULSE_WIDTH when DSI_TE_HSYNC_NUMBER is greater than 0	RW	0x001
7:0	RESERVED		R	0x00

Table 10-630. Register Call Summary for Register DSI_TE_VSYNC_WIDTH_j

MIPI Display Serial Interface

- DSI PHY Triggers: [0] [1] [2] [3] [4] [5]
- DSI Register Summary: [6] [7]

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Table 10-631. DSI_TE_HSYNC_NUMBER_j

Address Offset	0x0000 00A8 + (0xc * j)	**Index**	j = 0 to 1
Physical Address	0x5800 40A8 + (0xc * j) 0x5800 90A8 + (0xc * j)	**Instance**	DSI1_A DSI1_C
Description	The register configures the number of HSYNC to synchronize the beginning of the transfer on DSI link based on the number of HSYNC pulse received on the TE line. The input TE signal is asynchronous and needs to be resynchronizred to DSI_CLK clock domain.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LINE_NUMBER							

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:0	LINE_NUMBER	Programmable line number Line number from 0 to 2047. Number of HSYNC after the VSYNC occurs before the beginning of the transfer. Any HSYNC before VSYNC is ignored.	RW	0x000

Table 10-632. Register Call Summary for Register DSI_TE_HSYNC_NUMBER_j

MIPI Display Serial Interface

- DSI PHY Triggers: [0] [1] [2]
- DSI Register Summary: [3] [4]

Table 10-633. DSI_VC_CTRL_i

Address Offset	0x0000 0100 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4100 + (0x20 * i) 0x5800 9100 + (0x20 * i)	**Instance**	DSI1_A DSI1_C
Description	CONTROL REGISTER - Virtual channel This register controls the virtual channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCS_CMD_CODE	DCS_CMD_ENABLE	DMA_RX_REQ_NB				DMA_RX_THRESHOLD		DMA_TX_REQ_NB			RX_FIFO_NOT_EMPTY	DMA_TX_THRESHOLD			TX_FIFO_FULL	VC_BUSY	PP_BUSY	VP_SOURCE	RGB565_ORDER	OCP_DATA_BUS_WIDTH		MODE_SPEED	ECC_TX_EN	CS_TX_EN	BTA_EN	TX_FIFO_NOT_EMPTY	MODE	BTA_LONG_EN	BTA_SHORT_EN	SOURCE	VC_EN

Bits	Field Name	Description	Type	Reset
31	DCS_CMD_CODE	DCS command code value to insert between header and video port or Interface slave data when enabled by DCS_CMD_ENABLE (only when TE mechanism is not used otherwise the bit field DCS_CMD_CODE is ignored by DSI protocol engine). 0x0: DCS write memory continue code is inserted. 0x1: DCS write memory start code is inserted.	RW	0

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Bits	Field Name	Description	Type	Reset
30	DCS_CMD_ENABLE	Enables automatic insertion of DCS command codes when data is sourced by the video port. 0x0: DCS command code is NOT inserted when command mode traffic is coming from the Video Port or Interface slave port. 0x1: DCS command code is inserted automatically when command mode traffic is coming from the Video Port or Interface slave port.	RW	0
29:27	DMA_RX_REQ_NB	Selection of the use of the DMA request (associated to the RX FIFO) 0x0: DMA_req0 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 0) 0x1: DMA_req1 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 1) 0x2: DMA_req2 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 2) 0x3: DMA_req3 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is equal to 3) 0x4: No DMA req selected	RW	0x0
26:24	DMA_RX_THRESHOLD	Defines the threshold value for the DMA request (associated to the RX FIFO) 0x0: 1x 32 bits 0x1: 2 x 32 bits 0x2: 4 x 32 bits 0x3: 8 x 32 bits 0x4: 16 x 32 bits 0x5: 32 x 32 bits	RW	0x0
23:21	DMA_TX_REQ_NB	Selection of the use of the DMA request (associated to the TX FIFO) 0x0: DMA_req0 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 0) 0x1: DMA_req1 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 1) 0x2: DMA_req2 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is greater than 2) 0x3: DMA_req3 is selected (valid only if DSI_GNQ[8:6] NB_DMA_REQUEST is equal to 3) 0x4: No DMA req selected	RW	0x0
20	RX_FIFO_NOT_EMPTY	FIFO status in command mode. Otherwise, this bit can be ignored. Read 0x0: The RX FIFO is empty (the FIFO does not contain any data for the virtual channel) Read 0x1: The RX FIFO is not empty (the FIFO contains at least one byte for the virtual channel)	R	0
19:17	DMA_TX_THRESHOLD	Defines the threshold value for the DMA request (associated to the TX FIFO) 0x0: 1x 32 bits 0x1: 2 x 32 bits 0x2: 4 x 32 bits 0x3: 8 x 32 bits 0x4: 16 x 32 bits 0x5: 32 x 32 bits	RW	0x0

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Bits	Field Name	Description	Type	Reset
16	TX_FIFO_FULL	FIFO status in command mode. Otherwise, this bit can be ignored. Read 0x0: The TX FIFO is not full (the FIFO can accept at least one more 32-bit value) Read 0x1: The TX FIFO is full	R	0
15	VC_BUSY	Indicates if previously scheduled activities (packets, BTA) are still being processed. Forced to 1 if VC is enabled. Software should check this bit is 0 before changing channel configuration. Read 0x0: No pending operations for this VC Read 0x1: Pending operations for this VC	R	0
14	PP_BUSY	Ping-pong buffer busy status. Read 0x0: Software is permitted to write a new header for VP command mode traffic. Read 0x1: Software is NOT permitted to write a new header for VP command mode traffic.	R	0
13	VP_SOURCE	Selection between video port 1 and video port 2. If DSI_GNQ[24] NB_VIDEO_PORTS = 0, the bit field is ignored since only video port 1 is present. 0x0: The video port 1 is selected. 0x1: The video port 2 is selected.	RW	0
12	RGB565_ORDER	Byte order for RBG565 0x0: Byte order as for DBI compliance 0x1: Byte order as for video mode	RW	0
11:10	OCP_DATA_BUS_WIDTH	Defines the size of the Interface data bus 0x0: 16-bits data width (LSB of the 32-bit Interface port data bus) 0x1: 24-bits data width (LSB of the 32-bit Interface port data bus) 0x2: 2x16-bits data width (first pixel on the LSB of the 32-bit Interface port data bus and second pixel on the MSB of the 32-bit Interface port data bus for the same Interface access) 0x3: 32-bits data width	RW	0x0
9	MODE_SPEED	Selection of the mode. The information is used by hardware only if MODE=COMMAND_MODE otherwise it is ignored. 0x0: Low-power mode (CMOS) is used to send short and long packets to the peripheral. 0x1: High Speed mode (SLVS) is used to send short and long packets to the peripheral.	RW	0
8	ECC_TX_EN	Enables the Error Correction Code generation for the transmit header (short and long packets). 0x0: Disabled 0x1: Enabled	RW	0
7	CS_TX_EN	Enables the checksum generation for the transmit payload (long packet only). 0x0: Disabled. The value 0x00 is used. 0x1: Enabled. The checksum value is calculated by HW.	RW	0

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Bits	Field Name	Description	Type	Reset
6	BTA_EN	Send the bus turn around to the peripheral. It can be used when the automatic mode is enabled (BTA_SHORT_EN=1 or/and BTA_LONG_EN=1). In that case only one BTA is sent to the peripheral. The manual mode is used to allow the user to define for which packets, the turn around is required for example getting acknowledge from the peripheral. 0x0: Reads: BTA generation is completed. It is reset by hardware when it is completed. Writes: Cancellation of the BTA generation (not guarantee since it could already on going, shall not be used). 0x1: Reads: BTA generation has been requested by user (it could be on going but not completed). Writes: Request for BTA generation.	RW	0
5	TX_FIFO_NOT_EMPTY	FIFO status Read 0x0: The TX FIFO is empty (the FIFO does not contain any data for the virtual channel) Read 0x1: The TX FIFO is not empty (the FIFO contains at least one byte for the virtual channel)	R	0
4	MODE	Selection of the mode 0x0: Command mode. 0x1: Video mode. The bit fields MODE_SPEED and SOURCE are not used by hardware. The bit field VP_SOURCE is used to select between video port 1 and video port 2 when two video ports are present.	RW	0
3	BTA_LONG_EN	Enables the automatic bus turn-around after completion of each long packet transmission. 0x0: Disabled 0x1: Enabled	RW	0
2	BTA_SHORT_EN	Enables the automatic bus turn-around after completion of each short packet transmission. 0x0: Disabled 0x1: Enabled	RW	0
1	SOURCE	Selection of the source between Interface and the Video port(s) (used by the hardware only if MODE=COMMAND MODE (0x0) otherwise it is ignored). The number of available video ports is defined in DSI_GNQ[24] NB_VIDEO_PORTS bit. 0x0: All the data are provided by the slave port. Any transfer on the video port is ignored for this virtual channel. 0x1: If MODE=VIDEO_MODE. the data received on the video port 1 or video port 2, selected using VP_SOURCE (pixels and enabled synchronization events using DSI_CTRL[17] VP_HSYNC_START, DSI_CTRL[18] VP_HSYNC_END, DSI_CTRL[15] VP_VSYNC_START, DSI_CTRL[16] VP_VSYNC_END for video port 1 and DSI_CTRL2[] VP_HSYNC_START, DSI_CTRL2[] VP_HSYNC_END, DSI_CTRL2[] VP_VSYNC_START, DSI_CTRL2[] VP_VSYNC_END for video port 2) are sent on the virtual channel (only one virtual channel can be associated with the video port, it is the software responsibility to ensure that no more than one virtual channel is enabled with the video port as the main source for data). If MODE=COMMAND_MODE, the VP.STALL signal is used by the protocol engine to indicate when new data are required. The synchronization signals are not generated by the display controller. Regardless of the MODE, no data can be provided on the Interface slave port.	RW	0

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Bits	Field Name	Description	Type	Reset
0	VC_EN	Enables the virtual channel. 0x0: Disabled. The virtual channel shall be disabled for any register change in the DSI_VC_... registers to the corresponding VC ID (except for setting the DSI_VC_CTRL_i[6] BTA_EN, DSI_VC_TE_i[23:0] TE_SIZE and DSI_VC_TE_i[31] TE_START bit fields, and DSI_VC_LONG_,,, DSI_VC_SHORT_..., DSI_VC_IRQ... registers). 0x1: Enabled. No change is allowed to the virtual channel registers expect resetting the VC_EN.	RW	0

Table 10-634. Register Call Summary for Register DSI_VC_CTRL_i

MIPI Display Serial Interface

- DSI Short Packet: [0]
- DSI Long Packet: [1]
- DSI Blanking: [2] [3] [4] [5]
- DSI VCs: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]
- DSI 16 bpp – RGB Color Format, Long Packet (Command Mode): [17]
- DSI Global Register Controls: [18]
- DSI Transfer Modes: [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43]
- DSI Video Port Interface: [44] [45] [46]
- DSI Timers: [47] [48]
- DSI Bus Turnaround: [49] [50] [51] [52] [53] [54] [55]
- DSI PHY Triggers: [56] [57] [58]
- DSI ECC Generation: [59] [60]
- DSI Checksum Generation for Long Packet Payloads: [61]
- DSI Power Control of DSI PHY and DSI PLL: [62] [63]
- DSI Video Mode Using the DISPC Video Port: [64] [65] [66] [67] [68] [69]
- DSI Command Mode Using the DISPC Video Port: [70] [71] [72] [73] [74] [75] [76] [77] [78] [79] [80] [81] [82]
- DSI Register Summary: [83] [84]
- DSI Register Description: [85] [86]

Table 10-635. DSI_VC_TE_i

Address Offset	0x0000 0104 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4104 + (0x20 * i) 0x5800 9104 + (0x20 * i)	**Instance**	DSI1_A DSI1_C
Description	CONTROL REGISTER - Virtual channel This register controls the tearing effect logic. It defines the size of the transfer when TE occurs and enables the automatic TE mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TE_START	TE_EN	TE_LINE	TE_LINE_NB	RESERVED				TE_SIZE																							

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Bits	Field Name	Description	Type	Reset
31	TE_START	Manual control of the start of the transfer. The user can use the TE interrupt in order to know that the TE trigger has been received prior to set the TE_START bit field. It is not mandatory to use the TE interrupt. 0x0: Indicates the end of the transfer. The bit can be used by user to cancel the transfer if not already started. The FIFO shall be flushed by software to ensure there is no data remaining in it. 0x1: Starts the transfer of the data. The size is defined in TE_SIZE. The bit field is set until the transfer is completed. It is reset by hardware when the transfer is completed.	RW	0
30	TE_EN	Tearing Effect Control 0x0: Disables the automatic transfer. The user shall use the interruption in order to know when TE PHY trigger is received or when the TE is detected on the input CMOS signals. The hardware reset the bit field when the transfer is completed (TE_SIZE=0). 0x1: Enables the automatic transfer of the data using the TE PHY trigger or one of the TE input signals as a synchronization event. The bit field TE_LINE defines if the CMOS signal is used or if the PHY trigger is used.	RW	0
29	TE_LINE	0x0: Disabled the TE CMOS signaling for the automatic data transfer. The DSI PHY trigger is used for the automatic data transfer. 0x1: Enables the TE CMOS signaling for the automatic data transfer. The DSI PHY trigger is not used for the automatic data transfer.	RW	0
28	TE_LINE_NB	Selection between TE0 and TE1 CMOS signals. 0x0: TE0 CMOS input line is selected 0x1: TE1 CMOS input line is selected	RW	0
27:24	RESERVED		R	0x0
23:0	TE_SIZE	Defines the number of byte (payload data excluding the check -sum) to be sent. The write into the register DSI_VC_LONG_PACKET_HEADER_i shall be performed by the user before sending data from the register DSI_VC_LONG_PACKET_PAYLOAD_i. The register value is decremented for every byte sent of the DSI link. At the end of the transfer (TE_SIZE=0), the bit field TE_EN is reset by hardware. The DMA request will be asserted when the trigger is received in order to receive data in the TX FIFO. It should not be deasserted until all data (TE_SIZE) have been received in the FIFO.	RW	0x000000

Table 10-636. Register Call Summary for Register DSI_VC_TE_i

MIPI Display Serial Interface

- DSI PHY Triggers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
- DSI Command Mode Using the DISPC Video Port: [21] [22] [23]
- DSI Register Summary: [24] [25]
- DSI Register Description: [26] [27]

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Table 10-637. DSI_VC_LONG_PACKET_HEADER_i

Address Offset	0x0000 0108 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4108 + (0x20 * i) 0x5800 9108 + (0x20 * i)	**Instance**	DSI1_A DSI1_C
Description	LONG PACKET HEADER INFORMATION -Virtual channel This register sets the 32-bit DATA_ID + Word count + ECC (the virtual channel id can be different than VC). The ECC will be computed if ECC_TX_EN is set to 1. DATA_ID is located at bit[7:0] WC is located at bit[23:8] ECC is located at bit[31:24] (Least significant byte first and least significant bit first)		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HEADER																															

Bits	Field Name	Description	Type	Reset
31:0	HEADER	Packet header information: DATA ID + WORD COUNT +ECC	W	0x0000 0000

Table 10-638. Register Call Summary for Register DSI_VC_LONG_PACKET_HEADER_i

MIPI Display Serial Interface

- DSI Long Packet: [0] [1] [2] [3] [4] [5] [6]
- DSI Data Identifier: [7]
- DSI VCs: [8]
- DSI Global Register Controls: [9]
- DSI Transfer Modes: [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- DSI Video Port Interface: [26]
- DSI Bus Turnaround: [27]
- DSI PHY Triggers: [28] [29] [30]
- DSI ECC Generation: [31]
- DSI Video Mode Using the DISPC Video Port: [32]
- DSI Command Mode Using the DISPC Video Port: [33]
- DSI Register Summary: [34] [35]
- DSI Register Description: [36]

Table 10-639. DSI_VC_LONG_PACKET_PAYLOAD_i

Address Offset	0x0000 010C + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 410C + (0x20 * i) 0x5800 910C + (0x20 * i)	**Instance**	DSI1_A DSI1_C
Description	LONG PACKET PAYLOAD INFORMATION -Virtual channel This register sets the payload information (excluding checksum). The hardware shall capture the word count in the packet header (in DSI_VC_LONG_PACKET_HEADER) in order to determine the last valid data (the virtual channel id can be different than VC). Byte1 is bit[7:0] Byte2 is bit[15:8] Byte3 is bit[23:16] Byte4 is bit[31:24] Byten is sent before Byten+1 (Least significant byte first and least significant bit first)		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAYLOAD																															

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Bits	Field Name	Description	Type	Reset
31:0	PAYLOAD	Packet payload information (excluding checksum)	W	0x0000 0000

Table 10-640. Register Call Summary for Register DSI_VC_LONG_PACKET_PAYLOAD_i

MIPI Display Serial Interface
- DSI Long Packet: [0] [1] [2]
- DSI Global Register Controls: [3]
- DSI Transfer Modes: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- DSI Bus Turnaround: [14]
- DSI PHY Triggers: [15] [16]
- DSI Register Summary: [17] [18]
- DSI Register Description: [19]

Table 10-641. DSI_VC_SHORT_PACKET_HEADER_i

Address Offset	0x0000 0110 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4110 + (0x20 * i) 0x5800 9110 + (0x20 * i)	**Instance**	DSI1_A DSI1_C
Description	SHORT PACKET HEADER INFORMATION -Virtual channel This register sets the 24-bit DATA_ID + Short Packet Data Field + ECC (the virtual channel id can be different than VC). The ECC will be computed if ECC_TX_EN is set to 1. DATA_ID is located at bit[7:0] Short Packet Data field is located at bit[23:8] ECC is located at bit[31:24] (Least significant byte first and least significant bit first)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HEADER																															

Bits	Field Name	Description	Type	Reset
31:0	HEADER	Writes: Packet header information: DATA ID + DATA FIELD +ECC written into the TX FIFO Reads: 32-bit values read from the RX FIFO	RW	0x0000 0000

Table 10-642. Register Call Summary for Register DSI_VC_SHORT_PACKET_HEADER_i

MIPI Display Serial Interface
- DSI Short Packet: [0]
- DSI Data Identifier: [1]
- DSI VCs: [2]
- DSI Global Register Controls: [3]
- DSI Transfer Modes: [4] [5] [6] [7] [8] [9]
- DSI PHY Triggers: [10]
- DSI ECC Generation: [11]
- DSI Command Mode Using the DISPC Video Port: [12]
- DSI Register Summary: [13] [14]

Table 10-643. DSI_VC_IRQSTATUS_i

Address Offset	0x0000 0118 + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 4118 + (0x20 * i) 0x5800 9118 + (0x20 * i)	**Instance**	DSI1_A DSI1_C
Description	INTERRUPT STATUS REGISTER - Virtual channel This register regroups all the events related to the virtual channel.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							PP_BUSY_CHANGE_IRQ	FIFO_TX_UDF_IRQ	ECC_NO_CORRECTION_IRQ	BTA_IRQ	FIFO_RX_OVF_IRQ	FIFO_TX_OVF_IRQ	PACKET_SENT_IRQ	ECC_CORRECTION_IRQ	CS_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	PP_BUSY_CHANGE_IRQ	Video port ping-pong buffer busy status. PP_BUSY has changed from 1 to 0. 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
7	FIFO_TX_UDF_IRQ	FIFO underflow status. The FIFO used on the L3_MAIN interconnect slave port for buffering the data for the virtual channel has underflowed, which means that the data for the current packet have not been received in time because the transfer of the packets is already started (transfer started because the packet size is bigger than space allocated in the FIFO). 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
6	ECC_NO_CORRECTION_IRQ	ECC error status (short and long packets). No correction of the header because of more than 1-bit error. 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
5	BTA_IRQ	Virtual channel - BTA status. 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
4	FIFO_RX_OVF_IRQ	FIFO overflow error status. The FIFO used on the L3_MAIN interconnect slave port for buffering the data received on the DSI link for the virtual channel has overflowed. 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
3	FIFO_TX_OVF_IRQ	FIFO overflow error status. The FIFO used on the L3_MAIN interconnect slave port for buffering the data for the virtual channel has overflowed. 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
2	PACKET_SENT_IRQ	Indicates that a packet has been sent. It is used when BTA manual mode is used. 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
1	ECC_CORRECTION_IRQ	Virtual channel – ECC has been used to correct the only 1-bit error status (short and long packet). 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0
0	CS_IRQ	Virtual channel – Checksum mismatch status 0x0: Reads: Event is false. Writes: Status bit is unchanged. 0x1: Reads: Event is true (pending). Writes: Status bit is reset.	RW	0

Table 10-644. Register Call Summary for Register DSI_VC_IRQSTATUS_i

MIPI Display Serial Interface

- DSI Interrupt Requests: [0]
- DSI Transfer Modes: [1] [2] [3]
- DSI Video Port Interface: [4]
- DSI Bus Turnaround: [5] [6]
- DSI Interrupts: [7]
- DSI Command Mode Using the DISPC Video Port: [8] [9] [10] [11] [12] [13]
- DSI Register Summary: [14] [15]

Table 10-645. DSI_VC_IRQENABLE_i

Address Offset	0x0000 011C + (0x20 * i)	**Index**	i = 0 to 3
Physical Address	0x5800 411C + (0x20 * i) 0x5800 911C + (0x20 * i)	**Instance**	DSI1_A DSI1_C
Description	Interrupt enable register – Virtual channel This register regroups all the events related to the virtual channel.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							PP_BUSY_CHANGE_IRQ_EN	FIFO_TX_UDF_IRQ_EN	ECC_NO_CORRECTION_IRQ_EN	BTA_IRQ_EN	FIFO_RX_OVF_IRQ_EN	FIFO_TX_OVF_IRQ_EN	PACKET_SENT_IRQ_EN	ECC_CORRECTION_IRQ_EN	CS_IRQ_EN							

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x000000
8	PP_BUSY_CHANGE_IRQ_EN	Video port ping-pong buffer busy status 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
7	FIFO_TX_UDF_IRQ_EN	FIFO underflow enable. The FIFO used for buffering the data received on the L3_MAIN interface slave port for the virtual channel has underflowed which means that the data for the current packet have not been received in time since the transfer of the packet are already started (transfer started since the packet size is bigger than space allocated in the FIFO). 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
6	ECC_NO_CORRECTION_IRQ_EN	ECC error (short and long packets). No correction of the header because of more than 1-bit error. 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
5	BTA_IRQ_EN	Virtual channel -Bus turn around reception 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
4	FIFO_RX_OVF_IRQ_EN	FIFO overflow enable. The FIFO used on the L3_MAIN interconnect slave port for buffering the data received on the DSI link for the virtual channel has overflowed. 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
3	FIFO_TX_OVF_IRQ_EN	FIFO overflow enable. The FIFO used on the L3_MAIN interconnect slave port for buffering the data received on the Interface slave port for the virtual channel has overflowed. 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
2	PACKET_SENT_IRQ_EN	Indicates that a packet has been sent. It is used when BTA manual mode is used. 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
1	ECC_CORRECTION_IRQ_EN	Virtual channel - ECC has been used to correct the only 1-bit error (short and long packet). 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0
0	CS_IRQ_EN	Virtual channel - checksum of the payload mismatch detection 0x0: Event is masked. 0x1: Event generates an interrupt when it occurs.	RW	0

Table 10-646. Register Call Summary for Register DSI_VC_IRQENABLE_i

MIPI Display Serial Interface

- DSI Interrupt Requests: [0] [1] [2] [3]
- DSI Video Port Interface: [4]
- DSI Bus Turnaround: [5]
- DSI Interrupts: [6]
- DSI Video Mode Using the DISPC Video Port: [7]
- DSI Command Mode Using the DISPC Video Port: [8]
- DSI Register Summary: [9] [10]

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10.3.6.3 DSI PHY Registers

10.3.6.3.1 DSI PHY Register Summary

Table 10-647. DSI_PHY_DSS_A Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI_PHY_DSS_A L3_MAIN Physical Address
DSI_PHY_REGISTER0	RW	32	0x0000 0000	0x5800 4200
DSI_PHY_REGISTER1	RW	32	0x0000 0004	0x5800 4204
DSI_PHY_REGISTER2	RW	32	0x0000 0008	0x5800 4208
DSI_PHY_REGISTER3	RW	32	0x0000 000C	0x5800 420C
DSI_PHY_REGISTER4	RW	32	0x0000 0010	0x5800 4210
DSI_PHY_REGISTER5	W	32	0x0000 0014	0x5800 4214

Table 10-648. DSI_PHY_DSS_C Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSI_PHY_DSS_C L3_MAIN Physical Address
DSI_PHY_REGISTER0	RW	32	0x0000 0000	0x5800 9200
DSI_PHY_REGISTER1	RW	32	0x0000 0004	0x5800 9204
DSI_PHY_REGISTER2	RW	32	0x0000 0008	0x5800 9208
DSI_PHY_REGISTER3	RW	32	0x0000 000C	0x5800 920C
DSI_PHY_REGISTER4	RW	32	0x0000 0010	0x5800 9210
DSI_PHY_REGISTER5	W	32	0x0000 0014	0x5800 9214

10.3.6.3.2 DSI PHY Register Description

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Table 10-649. DSI_PHY_REGISTER0

Address Offset	0x0000 0000		
Physical Address	0x5800 4200 0x5800 9200	**Instance**	DSI_PHY_DSS_A DSI_PHY_DSS_C
Description	Configuration register for HS mode timings		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_THSPREPARE								REG_THSPRPR_THSZERO								REG_THSTRAIL								REG_THSEXIT							

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Bits	Field Name	Description	Type	Reset
31:24	REG_THSPREPARE	REG_THSPREPARE timing parameter in multiples of DDR clock period. DDR clock = CLKIN2DDR/2. D-PHY specification: 40 ns + 4 * UI ÷ 85 ns + 6 * UI. UI = Unit Interval, equal to the duration of any HS state on the clock lane. Default value is programmed for 400 MHz.	RW	0x1E
23:16	REG_THSPRPR_THSZERO	REG_THSPREPARE_THSZERO timing parameter in multiples of DDR clock period. DDR clock = CLKIN2DDR/2. D-PHY specification: > 145 ns + 10 * UI. Default value is programmed for 400 MHz.	RW	0x48
15:8	REG_THSTRAIL	REG_THSTRAIL timing parameter in multiples of DDR clock period. DDR clock = CLKIN2DDR/2. D-PHY specification: > 60 ns + 4 * UI. Default value is programmed for 400 MHz.	RW	0x1D
7:0	REG_THSEXIT	REG_THSEXIT timing parameter in multiples of DDR clock frequency. DDR clock = CLKIN2DDR/2. D-PHY specification: > 100 ns. Default value is programmed for 400 MHz.	RW	0x3A

Table 10-650. Register Call Summary for Register DSI_PHY_REGISTER0

MIPI Display Serial Interface

- DSI Clock Requirements: [0] [1] [2] [3] [4] [5] [6] [7]
- DSI SCP Interface: [8]
- DSI PHY Display Timing Configuration: [9] [10] [11] [12] [13]
- DSI Video Mode Using the DISPC Video Port: [14] [15] [16] [17]
- DSI Command Mode Using the DISPC Video Port: [18] [19] [20] [21]
- DSI Register Description: [22] [23]
- DSI PHY Register Summary: [24] [25]

Table 10-651. DSI_PHY_REGISTER1

Address Offset	0x0000 0004		
Physical Address	0x5800 4204 0x5800 9204	**Instance**	DSI_PHY_DSS_A DSI_PHY_DSS_C
Description	Configuration register for LP mode and HS mode timings		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_TTAGO			REG_TTASURE			REG_TTAGET		REG_CLKINP_SEL	REG_CLKPINP_DIVBY2EN	REG_DCCEN	REG_TLPXBY2					REG_TCLKTRAIL								REG_TCLKZERO							

Bits	Field Name	Description	Type	Reset
31:29	REG_TTAGO	TTA-GO timing in terms of number of TXCLKESC clocks. 0x0: 2 cycles 0x1: 3 cycles 0x2: 4 cycles	RW	0x2

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Bits	Field Name	Description	Type	Reset
		0x3: 5 cycles		
		0x4: 6 cycles		
		0x5: 7 cycles		
		0x6: 8 cycles		
		0x7: 9 cycles		
		Default value: 4 cycles		
28:27	REG_TTASURE	TTA-SURE timing in terms of number of TXCLKESC clocks.	RW	0x0
		0x0: 2 cycles		
		0x1: 1 cycles		
		0x2: 3 cycles		
		0x3: 4 cycles		
		Default value: 2 cycles		
26:24	REG_TTAGET	TTA-GET timing in terms of number of TXCLKESC clocks.	RW	0x2
		0x0: 3 cycles		
		0x1: 4 cycles		
		0x2: 5 cycles		
		0x3: 6 cycles		
		0x4: 7 cycles		
		0x5: 8 cycles		
		0x6: 9 cycles		
		0x7: 10 cycles		
		Default value: 5 cycles		
23	REG_CLKINP_SEL	0x0: Default Selects DCC Output	RW	0x0
		0x1: Selects Divby2 Output		
22	REG_CLKPINP_DIVBY2EN	0x0: Default	RW	0x0
		0x1: Enables DivBy2 in Clock Input Path		
21	REG_DCCEN	0x0: Default Enables Duty Cycle Corrector	RW	0x1
		0x1: Disable the DCC clock path		
20:16	REG_TLPXBY2	(TLPX)/2 timing parameter in multiples of DDR clock frequency. DDR clock = CLKIN2DDR/2.	RW	0x0A
		Default value is programmed for 400 MHz. This is the internal timer value. The value seen on line will have variance due to rise/fall mismatch effects.		
		Note: TLPX is used to define the length of LP-01 state in HS start of Transmission sequences on clock and data lanes. For all other purposes TLPX is defined by the period of TXLPESC		
15:8	REG_TCLKTRAIL	REG_TCLKTRAIL timing parameter in multiples of DDR clock frequency. DDR clock = CLKIN2DDR/2.	RW	0x1A
		D-PHY specification: > 60 ns.		
		Default value is programmed for 400 MHz		
7:0	REG_TCLKZERO	REG_TCLKZERO timing parameter in multiples of DDR clock period. DDR clock = CLKIN2DDR/2.	RW	0x6A
		D-PHY specification: (REG_TCLKPREPARE + REG_TCLKZERO) > 300 ns.		
		Derived specification for REG_TCLKZERO (Min REG_TCLKPREPARE = 38 ns): REG_TCLKZERO > 262 ns.		
		Default value is programmed for 400 MHz		

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Table 10-652. Register Call Summary for Register DSI_PHY_REGISTER1

MIPI Display Serial Interface

- DSI Clock Requirements: [0] [1] [2] [3] [4] [5]
- DSI PHY Display Timing Configuration: [6] [7] [8] [9] [10] [11]
- DSI Video Mode Using the DISPC Video Port: [12] [13] [14]
- DSI Command Mode Using the DISPC Video Port: [15] [16] [17] [18]
- DSI PHY Register Summary: [19] [20]

Table 10-653. DSI_PHY_REGISTER2

Address Offset	0x0000 0008		
Physical Address	0x5800 4208 0x5800 9208	**Instance**	DSI_PHY_DSS_A DSI_PHY_DSS_C
Description	Sync pattern		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSSYNCPATTERN								RESERVED							OVRRDULPMTX	REGULPMTX					RESERVED			REG_TCLKPREPARE							

Bits	Field Name	Description	Type	Reset
31:24	HSSYNCPATTERN	Default : 184 (10111000). MSB (last received bit of sync pattern), LSB (first received bit of sync pattern).	RW	0xB8
23:17	RESERVED	Reserved. Read returns zero. Write only zero for future compatibility.	R	0x00
16	OVRRDULPMTX	Global enable of the weak pulldown on the DSI lanes, configured through the [15:11] REGULPMTX bit field: 1: Enable weak pulldown on DSI lanes. 0: Disable weak pulldown on DSI lanes (default).	RW	0
15:11	REGULPMTX	Configuration of the weak pulldowns on the DSI lanes. For each bit, the following settings apply: 1: Enable weak pulldown on the lane. 0: Disable weak pulldown on the lane (default). Bit [15]: DSI lane 4 (applies only to DSI1_A and DSI1_C) Bit [14]: DSI lane 3 (applies only to DSI1_A and DSI1_C) Bit [13]: DSI lane 2 (applies to DSI1_A and DSI1_C) Bit [12]: DSI lane 1 (applies to DSI1_A and DSI1_C) Bit [11]: DSI lane 0 (applies to DSI1_A and DSI1_C)	RW	0x00
10:8	RESERVED	Reserved	RW	0x0
7:0	REG_TCLKPREPARE	TCLK-PREPARE timing parameter in multiples of DDR clock period. D-PHY specification: 38 ns ÷ 95 ns. Default value is programmed for 400 MHz.	RW	0x1A

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Table 10-654. Register Call Summary for Register DSI_PHY_REGISTER2

MIPI Display Serial Interface

- DSI Clock Requirements: [0] [1]
- DSI SCP Interface: [2]
- DSI PHY Display Timing Configuration: [3]
- DSI Video Mode Using the DISPC Video Port: [4]
- DSI Command Mode Using the DISPC Video Port: [5] [6]
- DSI Register Description: [7] [8]
- DSI PHY Register Summary: [9] [10]

Table 10-655. DSI_PHY_REGISTER3

Address Offset	0x0000 000C		
Physical Address	0x5800 420C 0x5800 920C	**Instance**	DSI_PHY_DSS_A DSI_PHY_DSS_C
Description	Transmitted pattern		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_TXTRIGGERESC3								REG_TXTRIGGERESC2								REG_TXTRIGGERESC1								REG_TXTRIGGERESC0							

Bits	Field Name	Description	Type	Reset
31:24	REG_TXTRIGGERESC3	Transmitted pattern when REG_TXTRIGGERESC3 is asserted (first bit transmitted to last bit transmitted). Default: 01100010	RW	0x62
23:16	REG_TXTRIGGERESC2	Default: 01011101	RW	0x5D
15:8	REG_TXTRIGGERESC1	Default: 00100001	RW	0x21
7:0	REG_TXTRIGGERESC0	Default: 10100000	RW	0xA0

Table 10-656. Register Call Summary for Register DSI_PHY_REGISTER3

MIPI Display Serial Interface

- DSI PHY Triggers: [0] [1]
- DSI PHY Register Summary: [2] [3]

Table 10-657. DSI_PHY_REGISTER4

Address Offset	0x0000 0010		
Physical Address	0x5800 4210 0x5800 9210	**Instance**	DSI_PHY_DSS_A DSI_PHY_DSS_C
Description	Received pattern		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_RXTRIGGERESC3								REG_RXTRIGGERESC2								REG_RXTRIGGERESC1								REG_RXTRIGGERESC0							

Bits	Field Name	Description	Type	Reset
31:24	REG_RXTRIGGERESC3	Received pattern for which REG_RXTRIGGERESC3 is asserted (first bit transmitted to last bit transmitted). Default: 01100010	RW	0x62
23:16	REG_RXTRIGGERESC2	Default: 01011101	RW	0x5D
15:8	REG_RXTRIGGERESC1	Default: 00100001	RW	0x21
7:0	REG_RXTRIGGERESC0	Default: 10100000	RW	0xA0

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Table 10-658. Register Call Summary for Register DSI_PHY_REGISTER4

MIPI Display Serial Interface

- DSI PHY Triggers: [0] [1] [2]
- DSI PHY Register Summary: [3] [4]

Table 10-659. DSI_PHY_REGISTER5

Address Offset	0x0000 0014		
Physical Address	0x5800 4214 0x5800 9214	**Instance**	DSI_PHY_DSS_A DSI_PHY_DSS_C
Description	Reset done bits		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESETDONETXBYTECLK	RESETDONESCPCLK	RESETDONEPWRCLK	RESETDONETXCLKESC4	RESETDONETXCLKESC3	RESETDONETXCLKESC2	RESETDONETXCLKESC1	RESETDONETXCLKESC0	RESERVED																							

Bits	Field Name	Description	Type	Reset
31	RESETDONETXBYTECLK	RESETDONETXBYTECLK 0x0: No reset 0x1: Reset done for the TXBYTECLK domain	R	0
30	RESETDONESCPCLK	RESETDONESCPCLK 0x0: No reset 0x1: Reset done for the SCP clock domain	R	0
29	RESETDONEPWRCLK	RESETDONEPWRCLK 0x0: No reset 0x1: Reset done for the PWR clock domain	R	0
28	RESETDONETXCLKESC4	RESETDONETXCLKESC4 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 4	R	0
27	RESETDONETXCLKESC3	RESETDONETXCLKESC3 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 3	R	0
26	RESETDONETXCLKESC2	RESETDONETXCLKESC2 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 2	R	0
25	RESETDONETXCLKESC1	RESETDONETXCLKESC1 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 1	R	0
24	RESETDONETXCLKESC0	RESETDONETXCLKESC0 0x0: No reset 0x1: Reset done for the TXCLKESC domain for lane 0	R	0
23:0	RESERVED	Read-Only register. Read returns zero.	R	0x000000

Table 10-660. Register Call Summary for Register DSI_PHY_REGISTER5

MIPI Display Serial Interface

- DSI PHY Reset-Done Bits: [0] [1] [2] [3] [4] [5] [6]
- DSI PHY Register Summary: [7] [8]

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10.3.6.4 DSI PLL Registers

10.3.6.4.1 DSI PLL Register Summary

Table 10-661. DPLL_DSI1_A Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DPLL_DSI1_A L3_MAIN Physical Address
DSI_PLL_CONTROL	RW	32	0x0000 0000	0x5800 4300
DSI_PLL_STATUS	R	32	0x0000 0004	0x5800 4304
DSI_PLL_GO	RW	32	0x0000 0008	0x5800 4308
DSI_PLL_CONFIGURATION1	RW	32	0x0000 000C	0x5800 430C
DSI_PLL_CONFIGURATION2	RW	32	0x0000 0010	0x5800 4310
DSI_PLL_CONFIGURATION3	RW	32	0x0000 0014	0x5800 4314
DSI_PLL_SSC_CONFIGURATION1	RW	32	0x0000 0018	0x5800 4318
DSI_PLL_SSC_CONFIGURATION2	RW	32	0x0000 001C	0x5800 431C

Table 10-662. DPLL_DSI1_C Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DPLL_DSI1_C L3_MAIN Physical Address
DSI_PLL_CONTROL	RW	32	0x0000 0000	0x5800 9300
DSI_PLL_STATUS	R	32	0x0000 0004	0x5800 9304
DSI_PLL_GO	RW	32	0x0000 0008	0x5800 9308
DSI_PLL_CONFIGURATION1	RW	32	0x0000 000C	0x5800 930C
DSI_PLL_CONFIGURATION2	RW	32	0x0000 0010	0x5800 9310
DSI_PLL_CONFIGURATION3	RW	32	0x0000 0014	0x5800 9314
DSI_PLL_SSC_CONFIGURATION1	RW	32	0x0000 0018	0x5800 9318
DSI_PLL_SSC_CONFIGURATION2	RW	32	0x0000 001C	0x5800 931C

10.3.6.4.2 DSI PLL Register Description

Table 10-663. DSI_PLL_CONTROL

Address Offset	0x0000 0000		
Physical Address	0x5800 4300 0x5800 9300	**Instance**	DPLL_DSI1_A DPLL_DSI1_C
Description	This register controls the PLL reset/power and modes		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											HSDIV_SYSRESET	PLL_SYSRESET	PLL_HALTMODE	PLL_GATEMODE	PLL_AUTOMODE

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reads as zero.	R	0x0000000
4	HSDIV_SYSRESET	Force HSDIVIDER SYSRESETN. Reserved when DBGSSV is 1. 0x0: HSDIVIDER SYSRESET forced active 0x1: HSDIVIDER SYSRESET controlled by power FSM	RW	1
3	PLL_SYSRESET	Force DPLL SYSRESETN. Reserved when DBGSSV is 1. 0x0: PLL SYSRESET forced active 0x1: PLL SYSRESET controlled by power FSM	RW	1
2	PLL_HALTMODE	Allow PLL to be halted if no activity. Reserved when DSI1_PLLCTRL_AUTO is 0. 0x0: PLL will not be halted 0x1: PLL will be halted based on activity	RW	0
1	PLL_GATEMODE	Allow PLL clock gating for power saving Reserved when DSI1_PLLCTRL_AUTO is 0. 0x0: PHY clock on 0x1: PHY clock gated by DSI Protocol Engine activity	RW	0
0	PLL_AUTOMODE	Automatic update mode. If this bit is set then the configuration updates will be synchronized to DISPCUpdateSync. If this bit is clear configuration updates will be done immediately. Reserved when DSI1_PLLCTRL_AUTO is 0. 0x0: Manual mode 0x1: Automatic mode	RW	0

Table 10-664. Register Call Summary for Register DSI_PLL_CONTROL

MIPI Display Serial Interface

- DSI PLL Clock-Gating Sequence: [0]
- DSI PLL Go Sequence: [1] [2] [3] [4]
- DSI PLL Recommended Values: [5] [6] [7] [8] [9]
- DSI Video Mode Using the DISPC Video Port: [10]
- DSI Command Mode Using the DISPC Video Port: [11]
- DSI PLL Register Summary: [12] [13]

Table 10-665. DSI_PLL_STATUS

Address Offset	0x0000 0004		
Physical Address	0x5800 4304 0x5800 9304	**Instance**	DPLL_DSI1_A DPLL_DSI1_C
Description	This register contains the status information		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PLL_TICOPWDN	PLL_LDOPWDN	BYPASSACKZ		SSC_EN_ACK	M7_CLOCK_ACK	M6_CLOCK_ACK	BYPASSACKZ_MERGED	M5_CLOCK_ACK	M4_CLOCK_ACK	PLL_BYPASS	PLL_HIGHJITTER	RESERVED	PLL_LOSSREF	PLL_RECAL	PLL_LOCK	PLLCTRL_RESET_DONE

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Reads as zero.	R	0x0000
16	PLL_TICOPWDN	PLL TICOPWDN status. Read 0x1: Internal oscillator power down Read 0x0: Internal oscillator power up	R	0
15	PLL_LDOPWDN	PLL LDOPWDN status. Read 0x1: PLL's internal LDO is power down Read 0x0: PLL's internal LDO is power up	R	0
14:13	BYPASSACKZ	State of bypass mode on PHY and HSDIVIDER. The status is shown separately for each source. Read 0x1: PLL outputs are still being used by the PHY or HSDIVIDER. Read 0x0: PHY or HSDIVIDER has switched to using the bypass clocks.	R	0x0
12	SSC_EN_ACK	Spread Spectrum Clocking acknowledge Read 0x1: Spread Spectrum Clocking active Read 0x0: Spread Spectrum Clocking inactive	R	0
11	M7_CLOCK_ACK	Acknowledge for enable of sub-system clock Verify the status before selecting this source in the sub-system clock mux Read 0x1: M7 clock active Read 0x0: M7 clock inactive	R	0
10	M6_CLOCK_ACK	Acknowledge for enable of sub-system clock Verify the status before selecting this source in the sub-system clock mux Read 0x1: M6 clock active Read 0x0: M6 clock inactive	R	0
9	BYPASSACKZ_MERGED	Merged state of bypass mode on PHY and HSDIVIDER Read 0x1: PLL outputs are still being used by the PHY or HSDIVIDER Read 0x0: PHY and HSDIVIDER have switched to using the bypass clocks.	R	0
8	M5_CLOCK_ACK	Acknowledge for enable of Protocol Engine clock Verify the status before selecting this source in the Protocol Engine clock mux Read 0x1: M5 Protocol Engine clock active Read 0x0: M5 Protocol Engine clock inactive	R	0
7	M4_CLOCK_ACK	Acknowledge for enable of sub-system clock Verify the status before selecting this source in the sub-system clock mux Read 0x1: M4 clock active Read 0x0: M4 clock inactive	R	0

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Bits	Field Name	Description	Type	Reset
6	PLL_BYPASS	PLL Bypass status Read 0x1: PLL bypass Read 0x0: PLL not bypassing	R	0
5	PLL_HIGHJITTER	PLL High Jitter status Read 0x1: PLL in high jitter condition: Phase error > 24% Read 0x0: PLL in normal jitter condition	R	0
4	RESERVED	Read returns zero.	R	0
3	PLL_LOSSREF	PLL Reference Loss status Read 0x1: Reference input inactive Read 0x0: Reference input active	R	0
2	PLL_RECAL	PLL re-calibration status If this bit is active, the PLL needs to be re-calibrated Read 0x1: Recalibration is required Read 0x0: Recalibration is not required	R	0
1	PLL_LOCK	PLL Lock status See the programming guide for the use of this bit Read 0x1: PLL is locked Read 0x0: PLL is not locked	R	0
0	PLLCTRL_RESET_DONE	PLLCTRL reset done status Read 0x1: Reset has completed Read 0x0: Reset is in progress	R	0

Table 10-666. Register Call Summary for Register DSI_PLL_STATUS

MIPI Display Serial Interface

- DSI PLL Controllers Architecture: [0]
- DSI PLL Error Handling: [1] [2] [3]
- DSI PLL Software Reset: [4]
- DSI PLL Clock-Gating Sequence: [5]
- DSI PLL Clock Sequence: [6]
- DSI PLL Go Sequence: [7]
- DSI Video Mode Using the DISPC Video Port: [8]
- DSI Command Mode Using the DISPC Video Port: [9]
- DSI PLL Register Summary: [10] [11]

Table 10-667. DSI_PLL_GO

Address Offset	0x0000 0008		
Physical Address	0x5800 4308 0x5800 9308	**Instance**	DPLL_DSI1_A DPLL_DSI1_C
Description	This register contains the GO bit		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														HSDIVLOAD	PLL_GO

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved. Write only zero for future compatibility. Reads return zero.	R	0x0000 0000
1	HSDIVLOAD	In manual mode start HSDIVIDER update sequence.	RW	0x0
0	PLL_GO	Request (re-)locking sequence of the PLL. If the AutoMode bit is set, then this will be deferred until DISPCUpdate Sync goes active 0x0: No pending action 0x1: Request PLL (re-)locking/locking pending	RW	0x0

Table 10-668. Register Call Summary for Register DSI_PLL_GO

MIPI Display Serial Interface

- DSI PLL Clock-Gating Sequence: [0] [1]
- DSI PLL Clock Sequence: [2]
- DSI PLL Go Sequence: [3] [4]
- DSI PLL Recommended Values: [5]
- DSI Video Mode Using the DISPC Video Port: [6] [7]
- DSI Command Mode Using the DISPC Video Port: [8] [9]
- DSI PLL Register Summary: [10] [11]

Table 10-669. DSI_PLL_CONFIGURATION1

Address Offset	0x0000 000C		
Physical Address	0x5800 430C 0x5800 930C	**Instance**	DPLL_DSI1_A DPLL_DSI1_C
Description	This register contains the latched PLL and HSDIVDER configuration bits		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	M5_CLOCK_DIV					M4_CLOCK_DIV		PLL_REGM												PLL_REGN											RESERVED

Bits	Field Name	Description	Type	Reset
31	RESERVED	Read returns zero.	R	0
30:26	M5_CLOCK_DIV	Divider value for Protocol Engine clock source M5REG	RW	0x00
25:21	M4_CLOCK_DIV	Divider value for clock source M4REG	RW	0x00
20:9	PLL_REGM	M Divider for PLL	RW	0x000
8:1	PLL_REGN	N Divider for PLL (Reference)	RW	0x00
0	RESERVED	Read returns zero.	R	0

Table 10-670. Register Call Summary for Register DSI_PLL_CONFIGURATION1

MIPI Display Serial Interface

- DSI PLL Controllers Architecture: [0] [1]
- DSI PLL Operations: [2] [3]
- DSI PLL Clock Sequence: [4] [5] [6] [7]
- DSI PLL Recommended Values: [8] [9] [10] [11]
- DSI Video Mode Using the DISPC Video Port: [12] [13] [14] [15]
- DSI Command Mode Using the DISPC Video Port: [16] [17] [18] [19]
- DSI PLL Register Summary: [20] [21]

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Table 10-671. DSI_PLL_CONFIGURATION2

Address Offset	0x0000 0010		
Physical Address	0x5800 4310 0x5800 9310	**Instance**	DPLL_DSI1_A DPLL_DSI1_C
Description	This register contains the unlatched PLL and HSDIVDER configuration bits These bits are "shadowed" when automatic mode is selected		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						M7_CLOCK_EN	RESERVED	M6_CLOCK_EN	REFSEL		HSDIVBYPASS	RESERVED	M5_CLOCK_EN	RESERVED	M4_CLOCK_EN	BYPASSEN	PHY_CLKINEN	PLL_REFEN	PLL_HIGHFREQ	PLL_CLKSEL	PLL_LOCKSEL		PLL_DRIFTGUARDEN	RESERVED	PLL_LOWCURRSTBY	PLL_PLLPMODE	RESERVED	PLL_SELFREQDCO		PLL_IDLE

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Read as zero.	R	0x00
25	M7_CLOCK_EN	Enable for M7 clock source 0x0: M7 clock divider is disabled 0x1: M7 clock divider is enabled	RW	0
24	RESERVED	Read returns zero.	R	0
23	M6_CLOCK_EN	Enable for M6 clock source 0x0: M6 clock divider is disabled 0x1: M6 clock divider is enabled	RW	0
22:21	REFSEL	Selects the reference clock with optional divide by 2 0x0: Select PCLK reference 0x1: Select REF1 reference 0x3: Select SYSCLK reference 0x2: Select REF2 Reference	RW	0x0
20	HSDIVBYPASS	Forces HSDIVIDER to bypass mode 0x0: HSDIVIDER in normal operation. Bypass controlled by PLL. 0x1: HSDIVIDER forced to bypass mode.	RW	0
19	RESERVED	Read returns zero.	R	0
18	M5_CLOCK_EN	Enable for Protocol Engine clock source 0x0: Protocol Engine clock divider is disabled 0x1: Protocol Engine clock divider is enabled	RW	0
17	RESERVED	Read returns zero	R	0
16	M4_CLOCK_EN	Enable for M4 clock source 0x0: Sub-system clock divider is disabled 0x1: Sub-system clock divider is enabled	RW	0
15	BYPASSEN	Selects sub-system functional clock as PHY clock source 0x0: PLL controls the PHY clock source: PLL DCO if PLL is locked Sub-system functional clock if not locked 0x1: Force sub-system functional clock to be used as the PHY clock source	RW	0
14	PHY_CLKINEN	PHY clock control 0x0: PHY clock is disabled 0x1: PHY clock is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	PLL_REFEN	PLL reference clock control 0x0: PLL reference clock disabled 0x1: PLL reference clock enabled	RW	1
12	PLL_HIGHFREQ	Enables a division of pixel clock by 2 before input to the PLL Required for pixel clock frequencies above 32 MHz (21 MHZ if N = 0) 0x0: Pixel clock is not divided 0x1: Pixel clock is divided by 2	RW	0
11	PLL_CLKSEL	Reference clock selection 0x0: Selects SYSCLK as PLL reference clock 0x1: Selects Pixel Clock (PCLK) as PLL reference clock	RW	0
10:9	PLL_LOCKSEL	Selects the lock criteria for the PLL 0x0: Phase Lock 0x1: Frequency Lock 0x2: Spare	RW	0x0
8	PLL_DRIFTGUARDEN	PLL DRIFTGUARDEN 0x0: Only RECAL flag is asserted in case of temperature drift. The programmer should take appropriate action. 0x1: Temperature drift will initiate automatic recalibration. RECAL flag will be asserted while this is taking place.	RW	0
7	RESERVED		R	0
6	PLL_LOWCURRSTBY	PLL LOW CURRENT STANDBY 0x0: LOWCURRSTBY is not selected 0x1: LOWCURRSTBY is selected	RW	0
5	PLL_PLLLPMODE	Select the power / performance of the PLL 0x0: Full performance, minimized jitter 0x1: Reduced power, increased jitter	RW	0
4	RESERVED	Reads as zero.	R	0
3:1	PLL_SELFREQDCO	DCO frequency range selector for DPLL 0x2 Set if DCO frequency is between 500MHz and 1000MHz 0x4 Set if DCO frequency is between 1000MHz and 2000MHz Others Reserved	RW	0x4
0	PLL_IDLE	PLL IDLE: 0x0: IDLE is not selected 0x1: IDLE is selected	RW	0

Table 10-672. Register Call Summary for Register DSI_PLL_CONFIGURATION2

MIPI Display Serial Interface

- DSI Clock Configuration: [0]
- DSI PLL Controllers Architecture: [1]
- DSI PLL Operations: [2] [3]
- DSI PLL Clock-Gating Sequence: [4]
- DSI PLL Clock Sequence: [5]
- DSI PLL Go Sequence: [6] [7] [8] [9]
- DSI PLL Recommended Values: [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
- DSI PHY Display Timing Configuration: [21]
- DSI Video Mode Using the DISPC Video Port: [22] [23] [24] [25]
- DSI Command Mode Using the DISPC Video Port: [26] [27] [28] [29]
- DSI PLL Register Summary: [30] [31]

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Table 10-673. DSI_PLL_CONFIGURATION3

Address Offset	0x0000 0014		
Physical Address	0x5800 4314 0x5800 9314	**Instance**	DPLL_DSI1_A DPLL_DSI1_C
Description	HSDIVIDER configuration bits for the M5 and M6 dividers		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED								M7_CLOCK_DIV								RESERVED							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:10	RESERVED	Reserved	R	0x000
9:5	M7_CLOCK_DIV	Divider value for M7 divider.	RW	0x00
4:0	RESERVED	Reserved	R	0x00

Table 10-674. Register Call Summary for Register DSI_PLL_CONFIGURATION3

MIPI Display Serial Interface

- DSI PLL Register Summary: [0] [1]

Table 10-675. DSI_PLL_SSC_CONFIGURATION1

Address Offset	0x0000 0018		
Physical Address	0x5800 4318 0x5800 9318	**Instance**	DPLL_DSI1_A DPLL_DSI1_C
Description	Configuration for PLL Spread Spectrum Clocking modulation		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													DOWNSPREAD	RESERVED	EN_SSC

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	RESERVED	R	0x0000 0000
2	DOWNSPREAD	Forces the clock spreading only in the down spectrum. 0x0: Clock spreading not forced. 0x1: Spectrum spreading only in down direction.	RW	0
1	RESERVED	Reserved. Reads return 0.	R	0
0	EN_SSC	Spread Spectrum Clocking enable 0x0: Spread Spectrum Clocking disabled 0x1: Spread Spectrum Clocking enabled	RW	0

Table 10-676. Register Call Summary for Register DSI_PLL_SSC_CONFIGURATION1

MIPI Display Serial Interface

- DSI PLL Controllers Architecture: [0] [1] [2]
- DSI PLL Register Summary: [3] [4]

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Table 10-677. DSI_PLL_SSC_CONFIGURATION2

Address Offset	0x0000 001C		
Physical Address	0x5800 431C 0x5800 931C	**Instance**	DPLL_DSI1_A DPLL_DSI1_C
Description	Configuration for PLL Spread Spectrum Clocking modulation		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DELTAM2	MODFREQDIVIDER														DELTAM															

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reads as zero	R	0x0
30	DELTAM2	MSB of DeltaM control bus.	RW	0x0
29:20	MODFREQDIVIDER	Modulation Frequency Divider (ModFreqDivider) control for SSC. The ModFreqDivider is split into Mantissa and 2^Exponent(ModFreqDivider = ModFreqDividerMantissa * 2^ModFreqDividerExponent). - Bits [29:23] define the Mantissa. - Bits [22:20] define the Exponent.	RW	0x000
19:0	DELTAM	DeltaM control for SSC. Split into integer and fractional parts. - Bits [19:18] define the integer part. - Bits [17:0] define the fractional part.	RW	0x00000

Table 10-678. Register Call Summary for Register DSI_PLL_SSC_CONFIGURATION2

MIPI Display Serial Interface

- DSI PLL Controllers Architecture: [0] [1]
- DSI PLL Register Summary: [2] [3]

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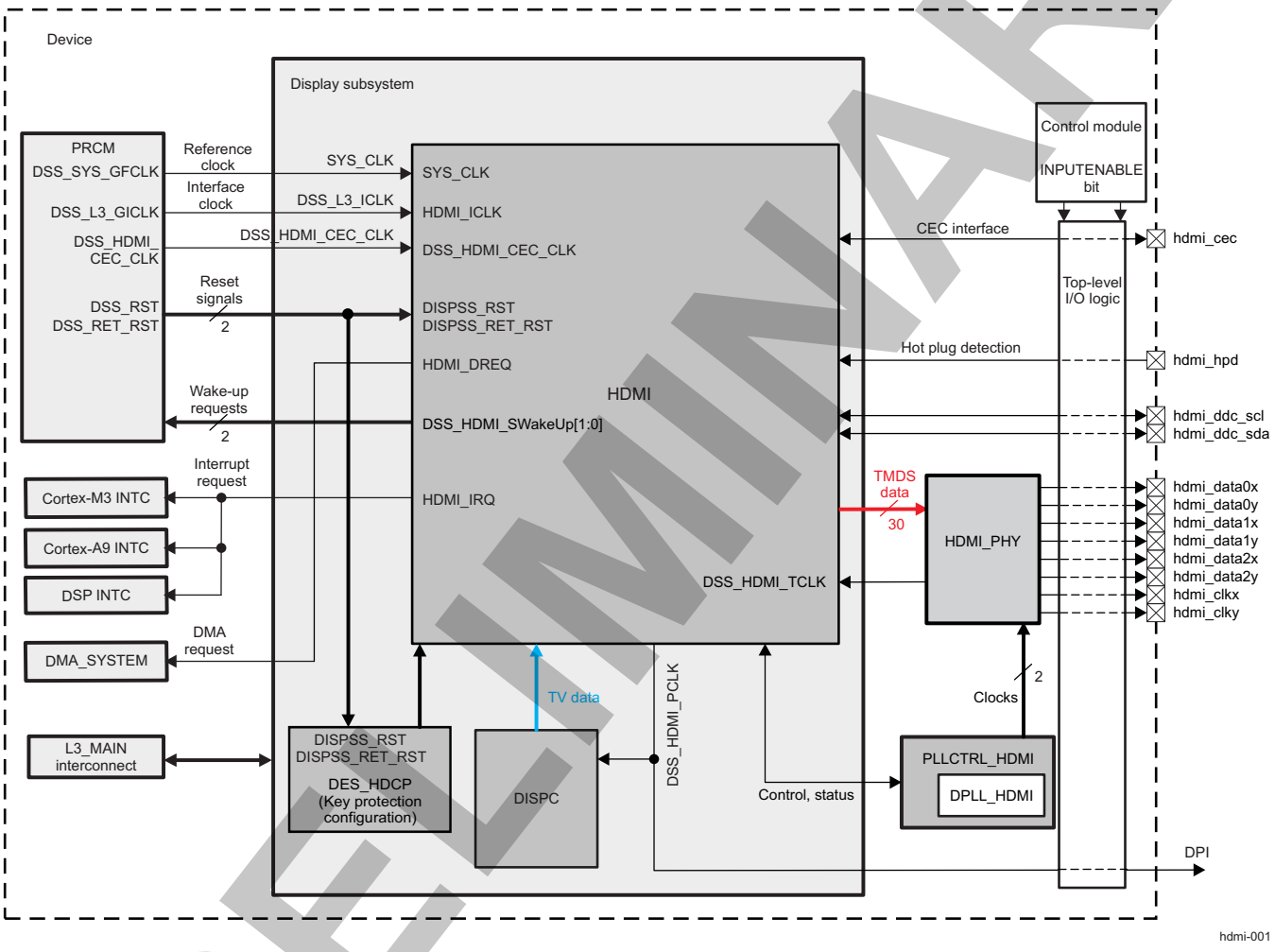
10.4 High-Definition Multimedia Interface

This section introduces the high-definition multimedia interface (HDMI) module and describes its main functions and connections in the device.

10.4.1 HDMI Overview

Figure 10-158 shows an overview of the HDMI module.

Figure 10-158. HDMI Overview



10.4.1.1 HDMI Main Features

The HDMI module provides the following main features:

- HDMI 1.4, HDCP 1.4, and DVI 1.0 compliant
  - Includes support for the 3D stereoscopic frame-packing formats of the HDMI v1.4 standard (1080p24Hz, 720p50Hz, 720p60Hz + side-by-side half structure: 1080p60Hz)
- EIA/CEA-861-D video format support (See Table 10-679 for more information.)
- VESA DMT video format support (See Table 10-680 for more information.)
- Support for deep-color mode:
  - 12-bit and 10 bit per color component deep-color modes up to 1080p @60Hz
- Supports up to 148.5-MHz pixel clock (1920 x 1080p @60Hz)
- Video formats:

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- ❑ 24/30/36-bit RGB/YCbCr 4:4:4 (deep color)
- ❑ 16/20/24-bit YCbCr 4:2:2

- Uncompressed multichannel (up to 8 channels) audio (L-PCM) support
- Master I2C interface for display data channel (DDC) connection
- Consumer electronic control (CEC) interface
- Integrated high-bandwidth digital content protection (DES_HDCP) encryption engine to transmit protected audio and video content (authentication performed by software)
- Integrated transition minimized differential signaling (TMDS) and TMDS error reduction coding (TERC4) encoders for data island support
- Integrated TMDS PHY (3 TMDS differential data lanes + TMDS differential clock lane)
  - Up to 2.97 Gbps per lane at (1080p @60Hz at 10 bits/component and 12 bits/component)

10.4.1.2 HDMI Video Formats and Timings

10.4.1.2.1 HDMI CEA-861-D Video Formats and Timings

Table 10-679 presents the video timings supported by the HDMI module, according to the CEA-861-D standard:

Table 10-679. HDMI Video Timings (CEA-861-D)

Refresh Rate	Resolution
24 Hz (Low field rate)	1920 x 1080p
50 Hz	1920 x 1080p 1920 x 1080i 2880 x 576p 2880 x 288p 1440 x 576p 1440 x 288p 1280x720p 720 x 576p
59.94 Hz	1920 x 1080p 1920 x 1080i 1280 x 720p 2880 x 480p 2880 x 240p 1440 x 480p 1440 x 480i 1440 x 240p 720 x 480p 640 x 480p

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Table 10-679. HDMI Video Timings (CEA-861-D) (continued)

Refresh Rate	Resolution
60 Hz	1920 x 1080p 1920 x 1080i 2880 x 480p 2880 x 240p 1280 x 720p 1440 x 480p 1440 x 480i 1440 x 240p 1280 x 720p 720 x 576p 720 x 480p 640 x 480p
200 Hz	720 x 576p
239 Hz	720 x 480p
240 Hz	720 x 480p

10.4.1.2.2 HDMI VESA DMT Video Formats and Timings

Table 10-680 presents the video timings supported by the HDMI module, according to the VESA DMT standard. Other various resolutions at 43 up to 120 Hz are also supported not included in Table 10-680.

Table 10-680. HDMI Video timings (VESA DMT)

Refresh Rate	Resolution
60 Hz	640 x 480p 800 x 600p 848 x 480p 1024 x 768p 1280 x 768p 1280 x 800p 1280 x 960p 1280 x 1024p 1360 x 768p 1366 x 768p 1400 x 1050p 1440 x 900p 1680 x 1200p 1680 x 1050p 1792 x 1344p 1856 x 1392p 1920 x 1200p 1920 x 1440p 1920 x 1080p

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Table 10-680. HDMI Video timings (VESA DMT) (continued)

Refresh Rate	Resolution
60 Hz (reduced blanking)	1280 x 768p 1280 x 800p 1400 x 1050p 1440 x 900p 1680 x 1050p 1920 x 1200p 2560 x 1600p

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10.5 Remote Frame Buffer Interface

This section describes the remote frame buffer interface (RFBI).

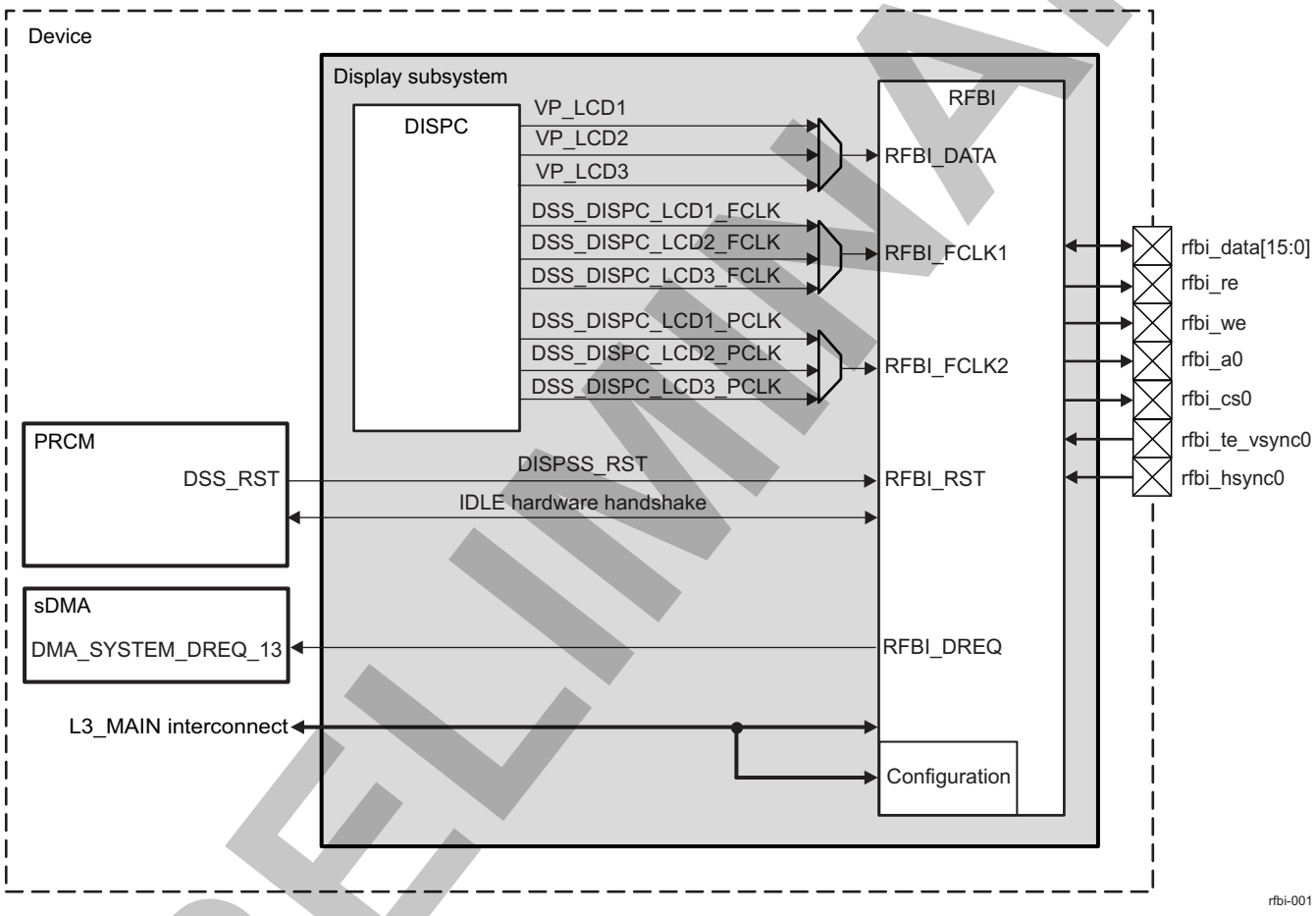
10.5.1 RFBI Overview

The RFBI module is part of the display subsystem that provides the logic to display a picture from the memory frame buffer (SDRAM or SRAM) on an LCD panel.

The RFBI is connected to the L3_MAIN interconnect through the display subsystem local interconnect.

Figure 10-159 shows an overview of the RFBI.

Figure 10-159. RFBI Highlight



The RFBI supports the MIPI DBI protocol with the following features:

- Access to RFB direct MPU interface
  - Sends commands to the RFB panel through the slave port interconnect
  - Sends data, received from the DISPC or from the MPU through the DISPC pixel data bus, to the RFB panel
  - Reads data/status from the RFB to the slave port interconnect
- RFB interface
  - 8-/9-/12-/16-bit parallel interface
  - Three programmable configuration (LCD1, 2, and 3) for an LCD connected to the RFBI
- Data formats
  - Programmable pixel modes (12-/16-/18-/24-bpp modes in RGB format)
  - Programmable output formats on one/multiple cycles per pixel (data from the DISPC and the

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L3_MAIN interconnect)

- FIFO
  - One slave port with DMA request and interconnect FIFO of 24 × 32-bit depth (for write access to the RFBI_DATA register only)
  - One video port FIFO of 8 × 24-bit depth receiving data from the DISPC through RFBI_DATA

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10.5.2 RFBI Environment

In the display subsystem, data are read by the DISPC from the memory frame buffer (SDRAM, SRAM, IVA-HD SL2, etc.), and sent through the RFBI to the external LCD/RFB.

The DISPC associated with the RFBI implements the MIPI DBI protocol.

The DISPC provides the required control signals to interface the memory frame buffer (SDRAM, SRAM or IVAHD-SL2) directly to the external displays. The RFBI is connected to the memory through the L3_MAIN interconnect and has its own DMA (with embedded FIFOs) to read data from the system memory. There is one master port (L3_MAIN interconnect) and one slave port.

The DISPC_CONTROL1[16] GPOUT[1] and DISPC_CONTROL1[15] GPOUT[0] bits control selection of the display subsystem modules (see Table 10-681).

Table 10-681. RFBI I/O Pad Mode Selection

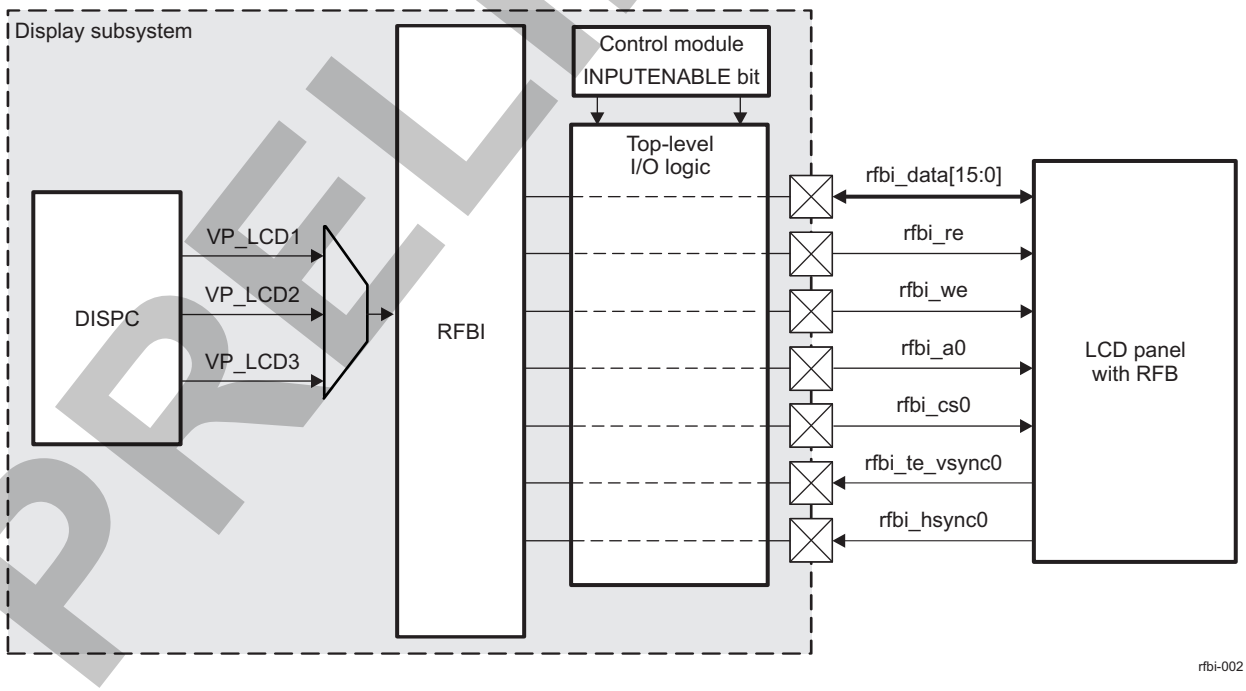
DSS.DISPC_CONTROL[16] GPOUT1	DSS.DISPC_CONTROL[15] GPOUT0	Mode
0	0	Reset
0	1	RFBI mode
1	0	Invalid
1	1	Bypass mode

The RFB of the LCD panel is directly connected to the RFBI of the device. The RFBI controls the reads/writes from/to the RFB. The RFBI receives data from its slave port or output from the DISPC and generates the signals to control the LCD panel. Through the RFBI, the MPU can send commands or parameter/display data to the LCD panel and directly set the DISPC registers to read/write data from/to the memory in the LCD panel. The RFBI can manage only one LCD panel at a time, although a sequential configuration is also possible.

10.5.2.1 RFBI Parallel Interface (MIPI DBI Protocol)

Figure 10-160 shows the LCD support parallel interface in RFBI mode.

Figure 10-160. RFBI LCD Support Interface



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NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and is programmable in the control module registers and dedicated IP registers. For more information, see , *Pad Functional Multiplexing and Configuration*, and , *Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*.

Table 10-682 describes the interface signals to/from the LCD panel.

Table 10-682. RFBI LCD Interface Signals

Signal Name	Type[1]	Description
rfbi_data[15:0]	I/O	RFBI I/O data
rfbi_re	O	Read access signal
rfbi_we	O	Write access signal
rfbi_a0	O	Command/data selection signal
rfbi_cs0	O	Chip-select (CS) signal for LCD
rfbi_te_vsync0	I	Tearing effect (TE) synchronization signal (TE or VSYNC for LCD panel 1)
rfbi_hsync0	I	HSYNC from LCD panel

(1) I = Input; O = Output; I/O = Input/Output

- rfbi_data[15:0]: The pixel data comprises the RFBI pixel data (bits 15:0). A write/read command must be sent to the LCD panel to send/read the data.

  Before any data access, the application must send commands and parameters when it is necessary to configure an LCD panel. The data is used as input in read operations during production test and also to read the status of the registers in the LCD panel and pixels from the embedded frame buffer in the LCD panel.
- rfbi_re: The read-enable signal indicates an ongoing read from the embedded memory in the LCD panel. The RFBI registers describe the behavior of the read signal (off/on/cycle time). The polarity of the read-enable signal is programmable. The read is used to obtain status/data information from the LCD panel.
- rfbi_we: The write-enable signal indicates an ongoing write. The RFBI registers allow flexible behavior of the write signal (programmable off/on/cycle times and signal polarity).
- rfbi_a0: The signal is asserted to indicate its status: Command or data. The polarity is programmable and the status of the signal depends on the RFBI registers written by the application (CMD/READ/STATUS/PARAM/PIXEL). The register in use by the hardware defines the status of rfbi_a0. The order of the writes/reads to the RFBI registers CMD/READ/STATUS/PARAM/PIXEL defines the transitions of A0.
- rfbi_cs0: The signal is the chip-select (CS0) asserted to indicate which LCD panel is selected and must be ready to receive/transmit commands and data. When RE or WE is on, CS0 must not be changed.

  To select the trigger mode, configure the RFBI_CONFIG[3:2] TRIGGERMODE bit field (0x0: Internal trigger mode with the RFBI_CONTROL[4] ITE bit; 0x1: External trigger mode with the TE signal rfbi_tevsync0; 0x2: External trigger mode with the rfbi_tevsync0 and rfbi_hsync0 signals with the programmable line counter).
- rfbi_te_vsync0 (used by RFBI only if RFBI_CONFIG[3:2] TRIGGERMODE = 0x1 or 0x2; otherwise, this signal is ignored): Based on the trigger mode selected, the signal is the TE pulse signal or the LCD panel vertical synchronization (VSYNC) pulse signal. TE logic uses rfbi_te_vsync0 as the synchronization signal to send the pixel to the LCD panel.
- rfbi_hsync0 (used by RFBI only if RFBI_CONFIG[3:2] TRIGGERMODE = 0x2, otherwise, this signal is ignored): The HSYNC pulse signals indicate to the RFBI when horizontal synchronization occurs. The polarity of the HSYNC signals is programmable. The minimum pulse width of the signal is two RFBI_ICLK clock cycles. TE logic uses rfbi_hsync0 as a synchronization signal to send the pixel to the LCD panel.

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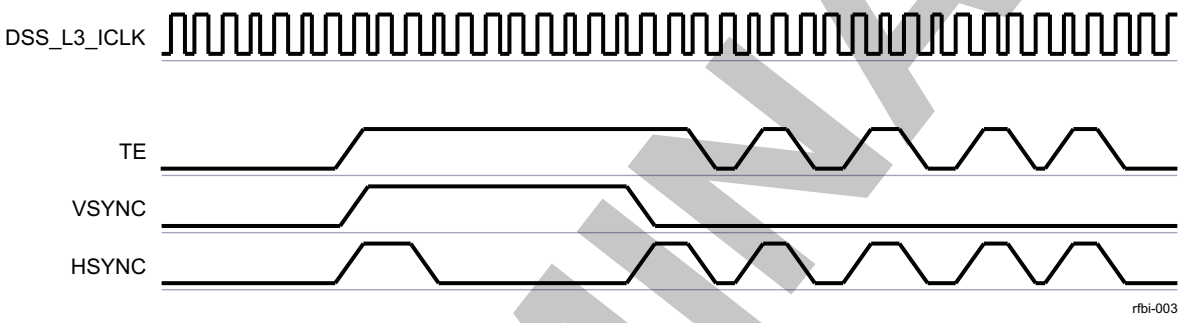
10.5.2.1.1 RFBI Description of the Tearing Effect Pulse Signal

The TE signal can be generated externally by the RFBI depending on the value of the RFBI_CONFIG[3:2] TRIGGERMODE bit field:

- TRIGGERMODE = 0x1: External trigger mode with the TE signal, which corresponds to the rfbi_te_vsync0 pad.
- TRIGGERMODE = 0x2: External trigger mode with the HSYNC/VSYNC signals. The HSYNC signal corresponds to the rfbi_hsync0 pad. The VSYNC signal corresponds to the rfbi_te_vsync0 pad.

The externally generated TE synchronization signal is a logical OR or AND operation between the HSYNC and VSYNC signals (see Figure 10-161). The logical operation (OR or AND) depends on the polarity of the HSYNC and VSYNC signals. The VSYNC signal indicates to the RFBI when vertical synchronization occurs. The HSYNC signal indicates to the RFBI when horizontal synchronization occurs.

Figure 10-161. RFBI External Generation of TE Signal Based on Logical OR Operation Between HSYNC and VSYNC (Active High)



- The TE signal is connected to the rfbi_te_vsync0 external pad when the RFBI_CONFIG[3:2] TRIGGERMODE bit field is set to 0x1.
- The HSYNC and VSYNC signals are connected to rfbi_hsync0 and rfbi_te_vsync0, respectively, when the RFBI_CONFIG[3:2] TRIGGERMODE bit field is set to 0x2.

The RFBI module detects the VSYNC and HSYNC pulses embedded in the received signal. VSYNC is detected based on the minimum pulse width defined by the RFBI_VSYNC_WIDTH register. VSYNC is not triggered by an inactive-to-active edge.

HSYNC is detected based on the minimum pulse width defined by the RFBI_HSYNC_WIDTH register. HSYNC is not triggered by an inactive-to-active edge.

The signal is generated from external logic based on VSYNC and HSYNC of the LCD panel. The automatic trigger can be programmed based on the external RFBI_TE signal or use the RFBI_CONTROL[4] ITE bit to start data capture (internal trigger mode).

The polarity of the TE signal is programmable in the RFBI_CONFIG register. HSYNC and VSYNC pulses embedded in the TE signal have the same polarity, which is active high for an ORed signal and active low for an ANDed signal. The minimum pulse width of the signal is two RFBI_ICLK clock cycles. Hardware resets the line counter when VSYNC occurs and increments it at every HSYNC. Transfer to the LCD panel begins when the line counter reaches the programmable line number.

10.5.2.2 RFBI Transaction Timing Diagrams

Table 10-683 lists the programmable timing fields. Figure 10-162 through Figure 10-164 show timing diagrams of read/write transactions to the LCD panel for the RFBI. In these figures, the polarity 0 (active low) describes the RFBI_A0, RFBI_CSi, RFBI_RE, and RFBI_WE signals.

Table 10-683. RFBI Programmable Timing Fields in RFBI Mode

Timing Name	Register Field	Description
CSOnTime	RFBI_ONOFF_TIME[3:0] CSONTIME bit field	CS assertion time from start access time
CSOffTime	RFBI_ONOFF_TIME[9:4] CSOFFTIME bit field	CS deassertion time from start access time

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Table 10-683. RFBI Programmable Timing Fields in RFBI Mode (continued)

Timing Name	Register Field	Description
WECycleTime	RFBI_CYCLE_TIME[5:0] WECYCLETIME bit field	The time when A0 becomes valid until write cycle completion
WEOnTime	RFBI_ONOFF_TIME[13:10] WEONTIME bit field	WE assertion delay time from start access time
WEOffTime	RFBI_ONOFF_TIME[19:14] WEOFFTIME bit field	WE deassertion delay time from start access time
RECycleTime	RFBI_CYCLE_TIME[11:6] RECYCLETIME bit field	The time when A0 becomes valid until read cycle completion
REOnTime	RFBI_ONOFF_TIME[23:20] REONTIME bit field	RE assertion delay time from start access time
REOffTime	RFBI_ONOFF_TIME[29:24] REOFFTIME bit field	RE deassertion delay time from start access time
CSPulseWidth	RFBI_CYCLE_TIME[17:12] CSPULSEWIDTH bit field	The time when write cycle time or read cycle time completes

Figure 10-162. RFBI Command Data Write

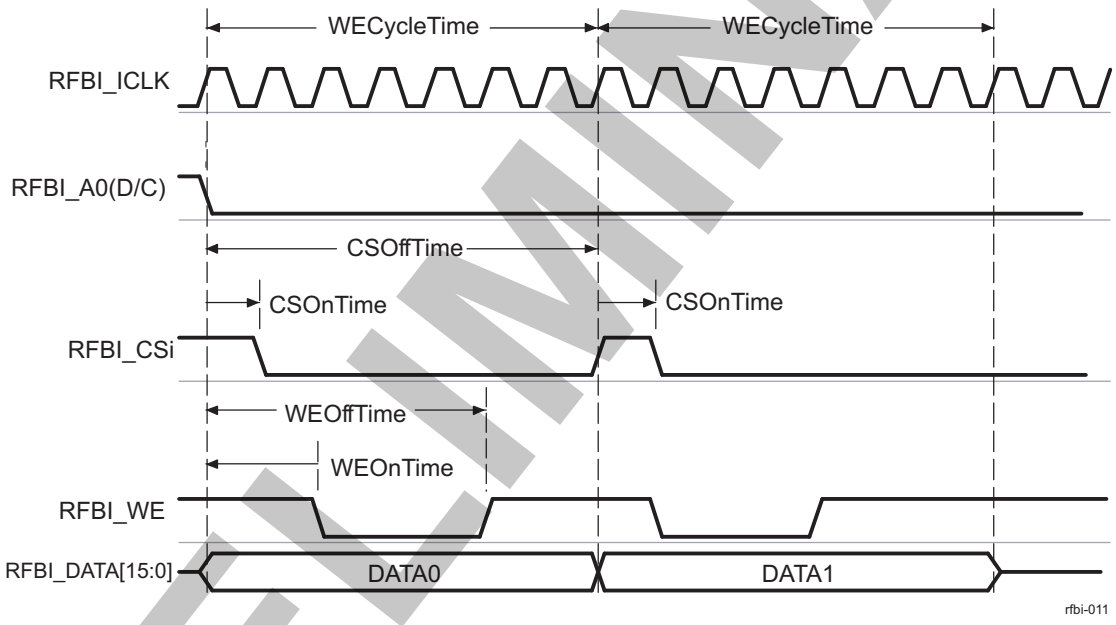

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Figure 10-163. RFBI Display Data Read

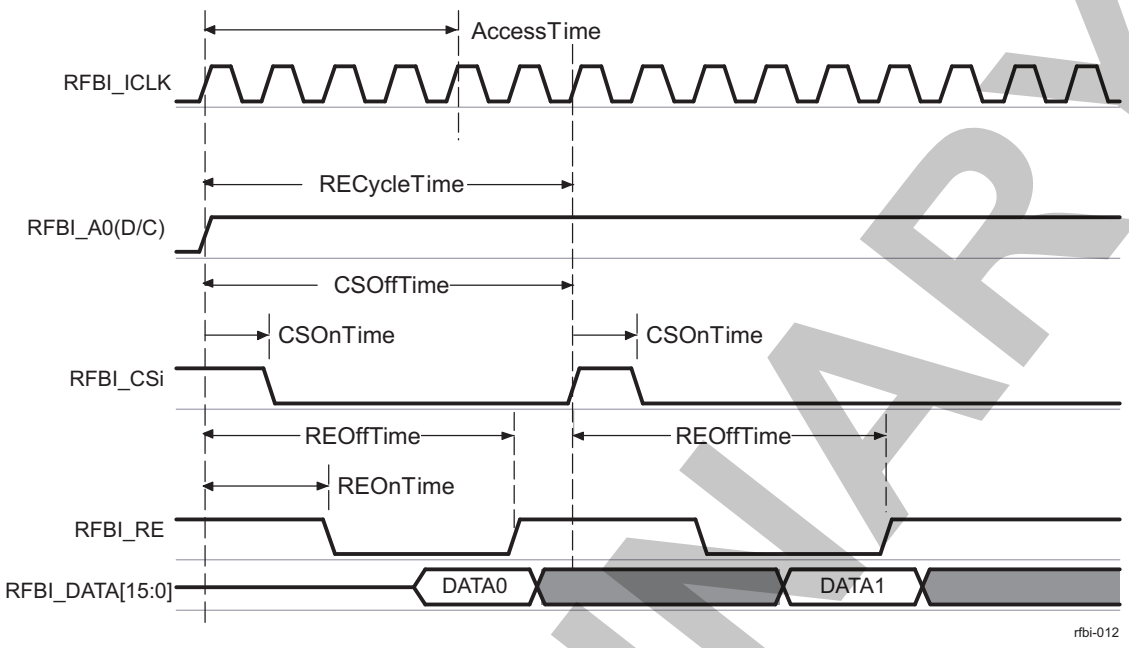
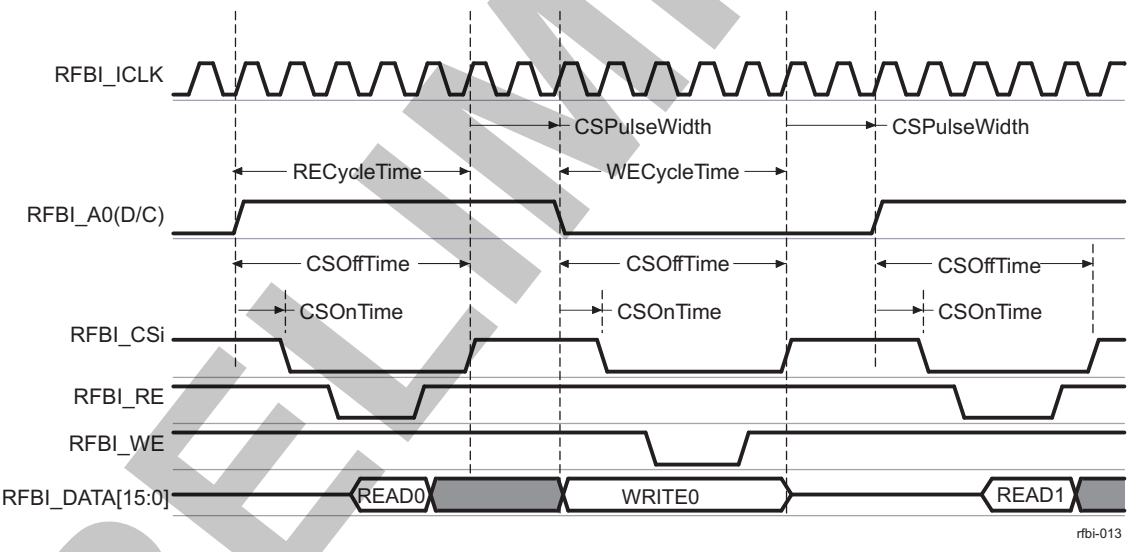


Figure 10-164. RFBI Read to Write and Write to Read



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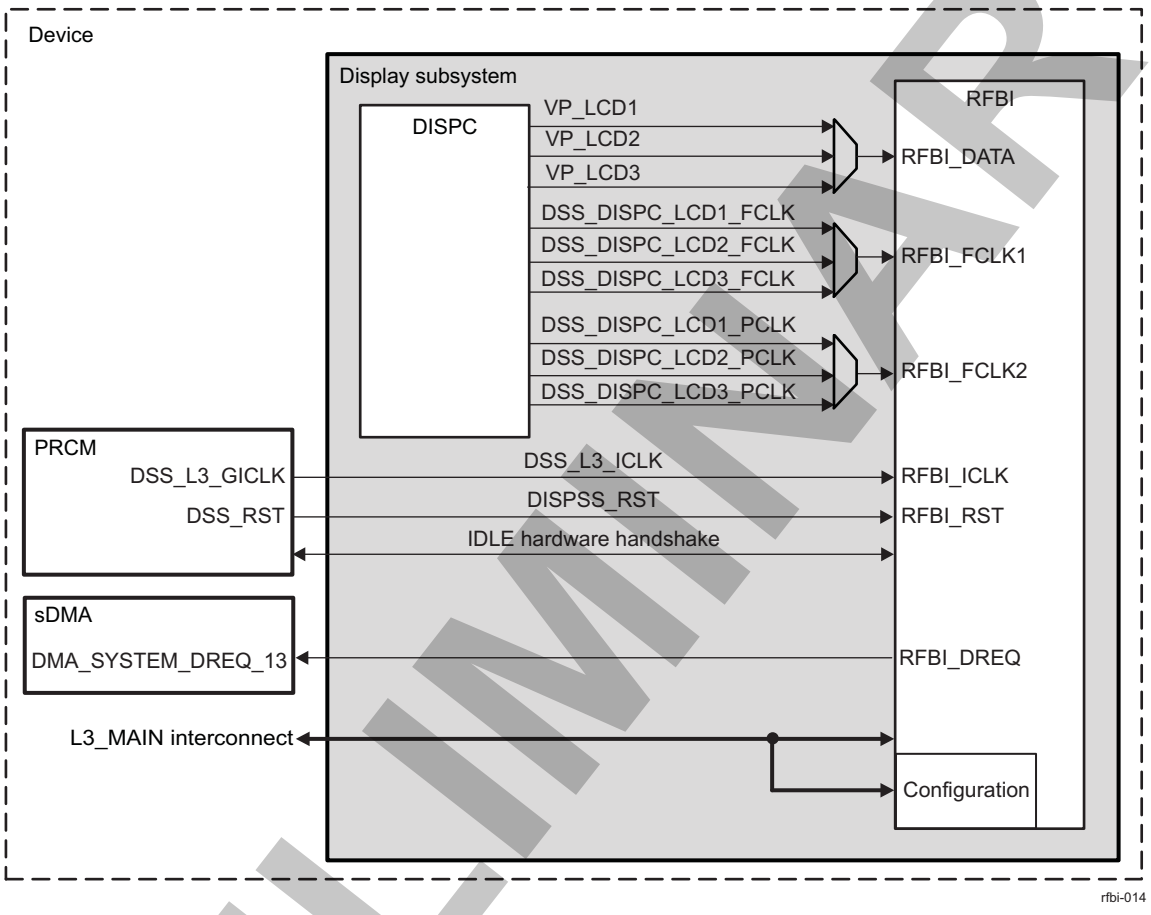
10.5.3 RFBI Integration

This section describes the RFBI integration in the device, including information about clocks, resets, and hardware requests.

Figure 10-165 shows the RFBI module integration.

Figure 10-165. RFBI Integration



NOTE: For more information about the IDLE hardware handshake, see , *Module-Level Clock Management*, in *Chapter 3, Power, Reset, and Clock Management*.

Table 10-684 through Table 10-686 summarize the integration of the module in the device.

Table 10-684. RFBI Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
RFBI	PD_DSS	No	L3_MAIN

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Table 10-685. RFBI Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
RFBI	RFBI_FCLK1	DSS_DISPC_LCDx_FCLK	DISPC	Logic clock used by the RFBI when capturing data on the video port and to generate the RFBI_DISPC_STALL signal
	RFBI_FCLK2	DSS_DISPC_LCDx_PCLK	DISPC	Pixel clock used by the RFBI to capture the pixels
	RFBI_ICLK	DSS_L3_MAIN_GICLK	PRCM	L3_MAIN interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
RFBI	RFBI_RST	DSS_RST	PRCM	Display subsystem global hardware reset

Table 10-686. RFBI Hardware Requests

DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
RFBI	RFBI_DREQ	DSS_SYSTEM_DREQ_13	DMA_SYSTEM	RFBI DMA request. The DMA request can be used to transfer data using the DMA_SYSTEM from memory to the RFBI interconnect slave FIFO. This request is a transition-sensitive (fixed in hardware), active-low request.

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10.5.4 RFBI Functional Description

This section describes the functions of the RFBI.

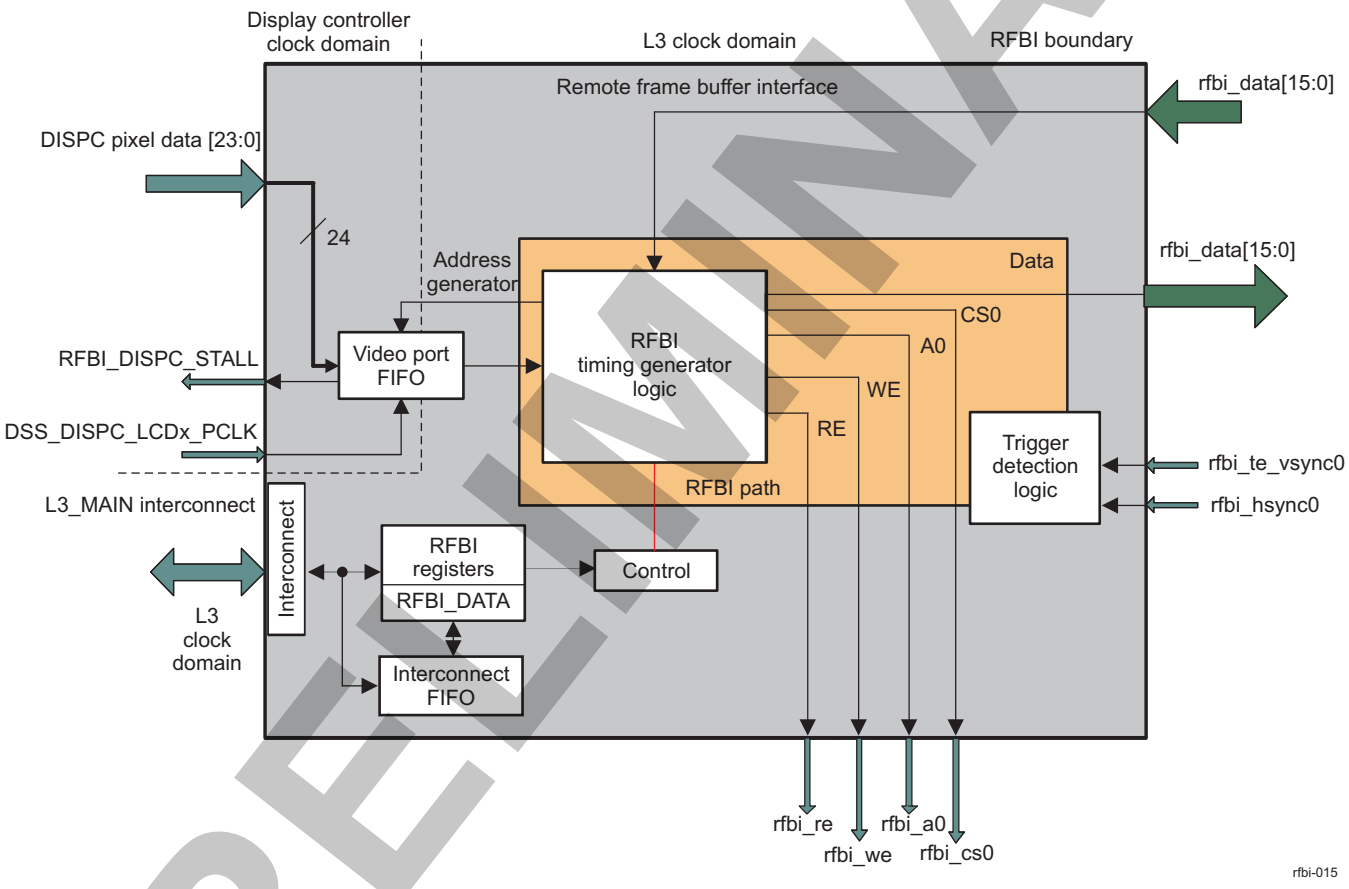
10.5.4.1 RFBI Block Diagram

The RFBI can capture the output pixel from the DISPC and send the data to the RFB in the LCD panel. The application configures the RFBI, sends commands, reads data, and configures the DISPC to send data fetched from the system memory by the DISPC DMA engine. The commands/data are sent using an 8-, 9-, 12- or 16-bit parallel interface.

The DISPC is configured to send the data in 12-, 16-, 18-, or 24-bpp format. In the video port FIFO, the encoded pixel values are in an LSB alignment independent of the endianness in system memory.

Figure 10-166 is an overview of the RFBI architecture.

Figure 10-166. RFBI Architecture Overview



10.5.4.2 RFBI Clock Configuration

The RFBI functional clocks (RFBI_FCLK1 and RFBI_FCLK2) are provided internally to the display subsystem by the DISPC. For more information about the DISPC clocks, see DISPC Clock Configuration, in *Display Controller*.

10.5.4.3 RFBI Software Reset

To perform a software reset, set the RFBI_SYSCONFIG[1] SOFTRESET bit to 1. The RFBI_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. When the software reset completes, the RFBI_SYSCONFIG[1] SOFTRESET bit is automatically reset. Software must ensure that the software reset completes before performing any RFBI operation.

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10.5.4.4 RFBI Power Management

Table 10-687 describes the power-management features available for the RFBI.

NOTE: For information about source clock gating description, see , *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 10-687. RFBI Local Power Management Features

Feature	Registers	Description
Clock autogating	RFBI_SYSCONFIG[0] AUTOIDLE bit	This bit allows a local power optimization inside the module by gating functional clocks (RFBI_FCLK1, RFBI_FCLK2) and interface clock (RFBI_ICLK) upon the internal activity.
Slave idle modes	RFBI_SYSCONFIG[4:3] SIDLEMODE bit field	Force-idle, no-idle, and smart-idle. For more information, see below.
Clock activity	N/A	Feature not available
Master standby modes	N/A	Feature not available
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	N/A	Feature not available

As shown in Table 10-687, the RFBI supports the no-idle, force-idle, and smart-idle modes.

The conditions of assertion of the SIdleAck signal are:

- No-idle mode: SIdleAck is never asserted.
- Force-idle mode: SIdleAck is asserted unconditionally after one RFBI_ICLK clock cycle delay with respect to assertion of IdleReq.
- Smart-idle mode: SIdleAck is asserted when the following conditions are satisfied: The RFBI stops using the RFBI_ICLK clock and all data have been sent to the RFB (LCD panel).

Once SIdleAck signal is asserted:

- The RFBI_ICLK (driven from DSS_L3_MAIN_ICLK) clock can shut down at any time.
- Any transaction on the RFBI configuration port is ignored

The conditions of deassertion of the SIdleAck signal are:

- Force-idle mode: SIdleAck is deasserted after one RFBI_ICLK clock cycle delay with respect to deassertion of IdleReq.
- Smart-idle mode: SIdleAck is deasserted after one RFBI_ICLK clock cycle delay with respect to deassertion of IdleReq.

Once SIdleAck is released, the RFBI is fully operational (guaranteed only in the case of the smart-idle mode).

10.5.4.5 RFBI Interrupt Requests

The RFBI does not generate interrupts but the following DISPC interrupts can be enabled depending on which LCD output of DISPC is currently used to connect to the RFBI:

- FRAMEDONE1_IRQ
- PROGRAMMEDLINENUMBER_IRQ
- GFXFIFOUNDERFLOW_IRQ
- GFXENDWINDOW_IRQ
- PALETTEGAMMALOADING_IRQ
- OCPERROR_IRQ
- VID1FIFOUNDERFLOW_IRQ

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- VID1ENDWINDOW_IRQ
- VID2FIFOUNDERFLOW_IRQ
- VID2ENDWINDOW_IRQ
- SYNCLOST1_IRQ
- WAKEUP_IRQ
- SYNCLOST2_IRQ
- VID3FIFOUNDERFLOW_IRQ
- VID3ENDWINDOW_IRQ
- FRAMEDONE2_IRQ

NOTE: For more information about DISPC interrupts, see DISPC Overview, in Chapter 10,*Display Controller*.

The other DISPC interrupts are not used in the RFBI.

10.5.4.6 RFBI DMA Requests

Table 10-688 lists event flags and their mask that can cause RFBI DMA requests.

Table 10-688. RFBI DMA Requests Events

DMA Request Name	DMA Request Mask	Map to	Description
RFBI_DREQ	RFBI_CONTROL[7] DISABLE_DMA_REQ	DSS_SYSTEM_DREQ_13	DMA request used to transfer data using the DMA_SYSTEM from memory to the RFBI interconnect FIFO

NOTE: For more information about DMA requests, see Figure 10-173.

10.5.4.7 RFBI Video Port FIFO

10.5.4.7.1 RFBI Video Port Description

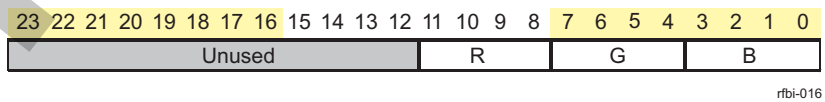
The input video port FIFO receives data from the DISPC at the pixel clock. The data in the video port FIFO are read by the RFBI and sent to the LCD panel. The video port FIFO is 24-bits wide and each pixel in 12-, 16-, 18-, and 24-bpp format is stored in the video port FIFO using one 24-bit value aligned on the 24-bit LSB. Section 10.5.4.9, *RFBI Output Parallel Modes*, provides examples of various output configurations based on the interface width (up to 16 bits) and pixel format output (up to 24 bits). Setting the RFBI_CONTROL[1] RFBIMODE bit to 0 directs the MPU to send commands, parameters, and data from the input video port FIFO.

10.5.4.7.2 RFBI Input Formats

The encoded pixel formats supported at the RFBI input interface connected to the DISPC are: RGB12-444, RGB16-565, RGB18-666, and RGB24-888. This input data width is controlled by the RFBI_CONFIG[6:5] DATATYPE bit field.

The following graphics describe the bit representation of each format in the video port FIFO. The output of the DISPC is aligned on the LSB of the interface. The pixels are then formatted in accordance with the configuration of the output interfaces (multiple cycles). For more information, see Section 10.5.4.9.1, *Cycle Mode Selection*.

- RGB12-444 format:



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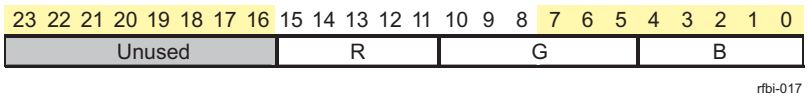
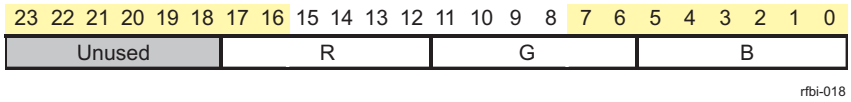
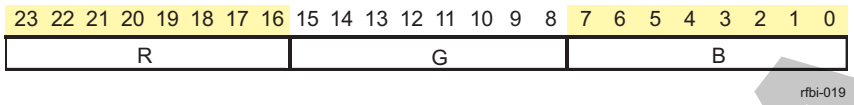
- RGB16-565 format:



- RGB18-666 format:



- RGB24-888 format:



NOTE: These pixel formats are also supported when data are provided from the slave port interconnect (for writing parameters).

10.5.4.7.3 RFBI Stall Mechanism

The stall signal (RFBI_DISPC_STALL) is generated by the video port FIFO to indicate when the DISPC must stop sending data on the corresponding LCD output interface. This stall signal is used for all three LCD outputs only when the DISPC is configured in stall mode. The stall mode is activated by setting the DISPC_CONTROLo[11] STALLMODE for the three LCD outputs.

NOTE: When the DISPC is configured in stall mode, the minimum transfer size is 1 byte.

The RFBI_DISPC_STALL signal allows the RFBI to reformat the data.

RFBI_DISPC_STALL is asserted when at least one of the following cases occurs:

- Default status when there is no data to capture from the DISPC
- High FIFO threshold reached
- End of transfer (number of data to output)
- RFBI reset
- RFBI_CONTROL[0] ENABLE bit reset to 0x0

RFBI_DISPC_STALL is deasserted when the RFBI_CONTROL[0] ENABLE bit is set to 0x1 and at least one of the following cases occurs:

- Low FIFO threshold reached
- External TE occurs and the RFBI_CONFIG[3:2] TRIGGERMODE bit field is set to 0x1 for automatic external trigger (start of the transfer, the FIFO pointers are reset, the FIFO is empty).
- RFBI_CONTROL[4] ITE bit set to 0x1 by users (start of transfer, the FIFO pointers are reset, the FIFO is empty)

NOTE: This stall mechanism is also used by the DSI protocol engines. When multiple modules are connected to the same LCD output (RFBI and DSI protocol engines), the STALL signals from the modules are merged into a single DSS_DISPC_LCDx_DATA_STALL signal inside the display subsystem. Only one signal for each LCD output is connected to the DISPC (three signals total for the three LCD outputs). In that case, only one module can control the STALL assertion/deassertion. The module that is not using the LCD output interface at that time is not disturbed because the STALL signal is asserted/deasserted by another module. For more information, see Chapter 10, *Display Subsystem* .

The RFBI asserts the STALL signal to stop data output by the DISPC. It is deasserted to indicate when new data must be output by the DISPC.

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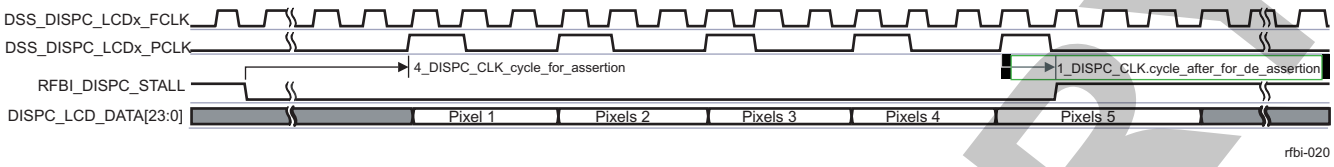
10.5.4.7.3.1 RFBI Data Stall Diagram Without DMA Buffer Handshake

Figure 10-167 shows the RFBI data stall diagram when the DISPC_DIVISOR[7:0] PCD bit field is set to 3.

Figure 10-167. RFBI Data Stall Signal Diagram With PCD = 3

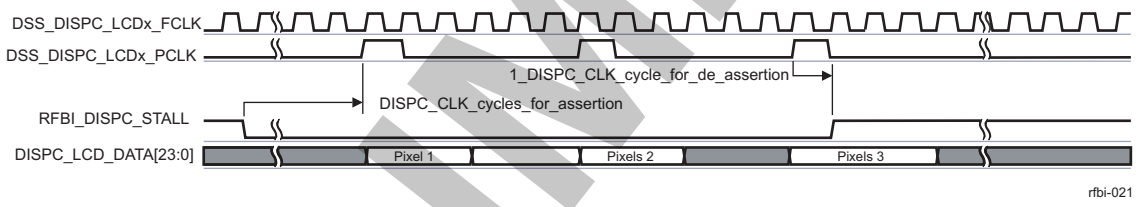


10.5.4.7.3.2 RFBI Data Stall Diagram With DMA Buffer Handshake

To avoid underflow of the DMA buffer, the DMA buffer handshake feature can be enabled by setting the DISPC_CONFIGo[16] BUFFERHANDCHECK bit to 1. The fullness of the FIFOs associated with the pipelines used for the LCD output is checked when the STALL signal is inactive before providing data to the pipeline. This prevents emptying the FIFO when the RFBI requests data and there is not enough data in the DISPC DMA buffer. This feature must be enabled only when the stall mode is used (DISPC_CONTROLo[11] STALLMODE bit set to 1).

When the DMA buffer handshake feature is activated, the pixel transfer to the RFBI during STALL inactivity period can be stopped (no DSS_DISPC_LCDx_PCLK pulse) and restarted when there is enough data in the DMA buffer. The DMA buffer handshake ensures that underflow cannot occur for the pipelines associated with the LCD output in stall mode. Figure 10-168 shows the RFBI data stall with the DMA buffer handshake mode activated (PCD = 3).

Figure 10-168. RFBI Data Stall Signal Diagram With Handshake With PCD = 3



10.5.4.8 RFBI Interconnect FIFO

10.5.4.8.1 RFBI Description

The interconnect FIFO receives the data from RFBI_DATA write requests to the slave port interconnect slave port. The data in the interconnect FIFO are read by the RFBI and sent to the LCD panel. The interconnect FIFO is 32-bits wide. The size of the interconnect FIFO is 24 words of 32 bits (that is, 24 words of RFBI_DATA). The address of the RFBI_DATA register is used to access the interconnect FIFO. The RFBI_DREQ DMA request can be used to transfer data using the DMA_SYSTEM from memory to the interconnect FIFO.

10.5.4.8.2 RFBI Using DMA Request With Interconnect FIFO

10.5.4.8.2.1 RFBI Threshold for DMA Request Generation

The RFBI_CONTROL[6:5] HIGHTHRESHOLD bit field defines the threshold to be used for the generation of the DMA request to receive data into the interconnect FIFO (24 × 32 FIFO depth) through the address of the register RFBI_DATA. The DMA_SYSTEM configuration regarding the size of the burst depends on the value of the RFBI_CONTROL[6:5] HIGHTHRESHOLD bit field. The supported values are 4 × 32, 8 × 32, and 16 × 32. For example, when 4 words of 32 bits are set for the threshold, the DMA_SYSTEM sends a burst of 4 × 32 bits only. The DMA_SYSTEM receives the DMA request and is in charge of providing the correct number of bytes.

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10.5.4.8.2.2 RFBI Disabling DMA Request

If the RFBI_CONTROL[7] DISABLE_DMA_REQ bit is reset, the DMA request is generated when there is enough room in the interconnect FIFO to accept the full burst. In case the RFBI receives writes slave port requests to the RFBI_DATA location when the interconnect FIFO is full, the request is not accepted. The RFBI waits for a free entry in the interconnect FIFO to accept the slave port request.

If the RFBI_CONTROL[7] DISABLE_DMA_REQ bit is set, the DMA request is not generated and the threshold value is ignored.

NOTE: Software users can access the RFBI_DATA location without using the DMA request and without programming the high threshold value (backward compatibility mode).

10.5.4.8.2.3 RFBI Smart DMA Request Mode

If the RFBI_CONTROL[8] SMART_DMA_REQ bit is reset (smart DMA mode disabled), the DMA request is asserted and deasserted depending on the interconnect FIFO space even if MIdlereq is high in smart-idle/no-idle mode and the entire burst gets error responses from the RFBI. The RFBI waits for a free entry in the interconnect FIFO to accept the burst request.

If the RFBI_CONTROL[8] SMART_DMA_REQ bit is set (smart DMA mode enabled), the DMA request is deasserted after two RFBI_ICLK clock cycles, if it has been asserted for more than or equal to two RFBI_ICLK clock cycles and MIdlereq is high in smart-idle or no-idle mode. If asserting time is less than two RFBI_ICLK clock cycles, no more burst requests are accepted even if space is available in the interconnect FIFO.

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10.5.4.9 RFBI Output Parallel Modes

10.5.4.9.1 RFBI Cycle Mode Selection

The RFBI_CONFIG[10:9] CYCLEFORMAT bit field defines the number of cycles to output a pixel. The number of cycles determines the number of registers used to format the data in the interconnect FIFO with the appropriate number of bits (starting from the LSB) and with the alignment on the interface. The data are formatted based on the configuration of the RFBI_DATA_CYCLEi registers.

- One cycle: RFBI_CONFIG[10:9] CYCLEFORMAT bit field = 0x00 and the RFBI_DATA_CYCLE1 register
- Two cycles: RFBI_CONFIG [10:9] CYCLEFORMAT bit field = 0x01 and the RFBI_DATA_CYCLE1 and RFBI_DATA_CYCLE2 registers
- Three cycles: RFBI_CONFIG[10:9] CYCLEFORMAT bit field = 0x10 and the RFBI_DATA_CYCLE1, RFBI_DATA_CYCLE2, and RFBI_DATA_CYCLE3 registers

Figure 10-169 through Figure 10-172 list the bits position of the pixel during the cycles for an 8-, 9-, and 16-bit parallel output, respectively.

Figure 10-169. 8-Bit Interface Settings

	24-bpp		
	1st cycle	2nd cycle	3rd cycle
Data[7]	R0[7]	G0[7]	B0[7]
Data[6]	R0[6]	G0[6]	B0[6]
Data[5]	R0[5]	G0[5]	B0[5]
Data[4]	R0[4]	G0[4]	B0[4]
Data[3]	R0[3]	G0[3]	B0[3]
Data[2]	R0[2]	G0[2]	B0[2]
Data[1]	R0[1]	G0[1]	B0[1]
Data[0]	R0[0]	G0[0]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x2
RFBI_DATA_CYCLE1 = 0x00000008
RFBI_DATA_CYCLE2 = 0x00000008
RFBI_DATA_CYCLE3 = 0x00000008

	18-bpp		
	1st cycle	2nd cycle	3rd cycle
Data[7]	R0[5]	G0[3]	x
Data[6]	R0[4]	G0[2]	x
Data[5]	R0[3]	G0[1]	x
Data[4]	R0[2]	G0[0]	x
Data[3]	R0[1]	B0[5]	x
Data[2]	R0[0]	B0[4]	x
Data[1]	G0[5]	B0[3]	B0[1]
Data[0]	G0[4]	B0[2]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x2
RFBI_DATA_CYCLE1 = 0x00000008
RFBI_DATA_CYCLE2 = 0x00000008
RFBI_DATA_CYCLE3 = 0x00000002

	16-bpp	
	1st cycle	2nd cycle
Data[7]	R0[4]	G0[2]
Data[6]	R0[3]	G0[1]
Data[5]	R0[2]	G0[0]
Data[4]	R0[1]	B0[4]
Data[3]	R0[0]	B0[3]
Data[2]	G0[5]	B0[2]
Data[1]	G0[4]	B0[1]
Data[0]	G0[3]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x00000008
RFBI_DATA_CYCLE2 = 0x00000008

	12-bpp	
	1st cycle	2nd cycle
Data[7]	R0[3]	x
Data[6]	R0[2]	x
Data[5]	R0[1]	x
Data[4]	R0[0]	x
Data[3]	G0[3]	B0[3]
Data[2]	G0[2]	B0[2]
Data[1]	G0[1]	B0[1]
Data[0]	G0[0]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x00000008
RFBI_DATA_CYCLE2 = 0x00000004

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Figure 10-170. 9-Bit Interface Settings

	24-bpp		
	1st cycle	2nd cycle	3rd cycle
Data[8]	R0[7]	G0[6]	x
Data[7]	R0[6]	G0[5]	x
Data[6]	R0[5]	G0[4]	x
Data[5]	R0[4]	G0[3]	B0[5]
Data[4]	R0[3]	G0[2]	B0[4]
Data[3]	R0[2]	G0[1]	B0[3]
Data[2]	R0[1]	G0[0]	B0[2]
Data[1]	R0[0]	B0[7]	B0[1]
Data[0]	G0[7]	B0[6]	B0[0]

RFBI_CONFIG.CYCLEFORMAT= 0x2
RFBI_DATA_CYCLE1 = 0x00000009
RFBI_DATA_CYCLE2 = 0x00000009
RFBI_DATA_CYCLE3 = 0x00000006

	18-bpp	
	1st cycle	2nd cycle
Data[8]	R0[5]	G0[2]
Data[7]	R0[4]	G0[1]
Data[6]	R0[3]	G0[0]
Data[5]	R0[2]	B0[5]
Data[4]	R0[1]	B0[4]
Data[3]	R0[0]	B0[3]
Data[2]	G0[5]	B0[2]
Data[1]	G0[4]	B0[1]
Data[0]	G0[3]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x0000000912
RFBI_DATA_CYCLE2 = 0x00000009

	16-bpp	
	1st cycle	2nd cycle
Data[8]	R0[4]	x
Data[7]	R0[3]	x
Data[6]	R0[2]	G0[1]
Data[5]	R0[1]	G0[0]
Data[4]	R0[0]	B0[4]
Data[3]	G0[5]	B0[3]
Data[2]	G0[4]	B0[2]
Data[1]	G0[3]	B0[1]
Data[0]	G0[2]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x00000009
RFBI_DATA_CYCLE2 = 0x00000007

	12-bpp	
	1st cycle	2nd cycle
Data[8]	R0[3]	x
Data[7]	R0[2]	x
Data[6]	R0[1]	x
Data[5]	R0[0]	x
Data[4]	G0[3]	x
Data[3]	G0[2]	x
Data[2]	G0[1]	B0[2]
Data[1]	G0[0]	B0[1]
Data[0]	B0[3]	B0[0]

RFBI_CONFIG.CYCLEFORMAT = 0x1
RFBI_DATA_CYCLE1 = 0x00000009
RFBI_DATA_CYCLE2 = 0x00000003

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Figure 10-171. 12-Bit Interface Settings

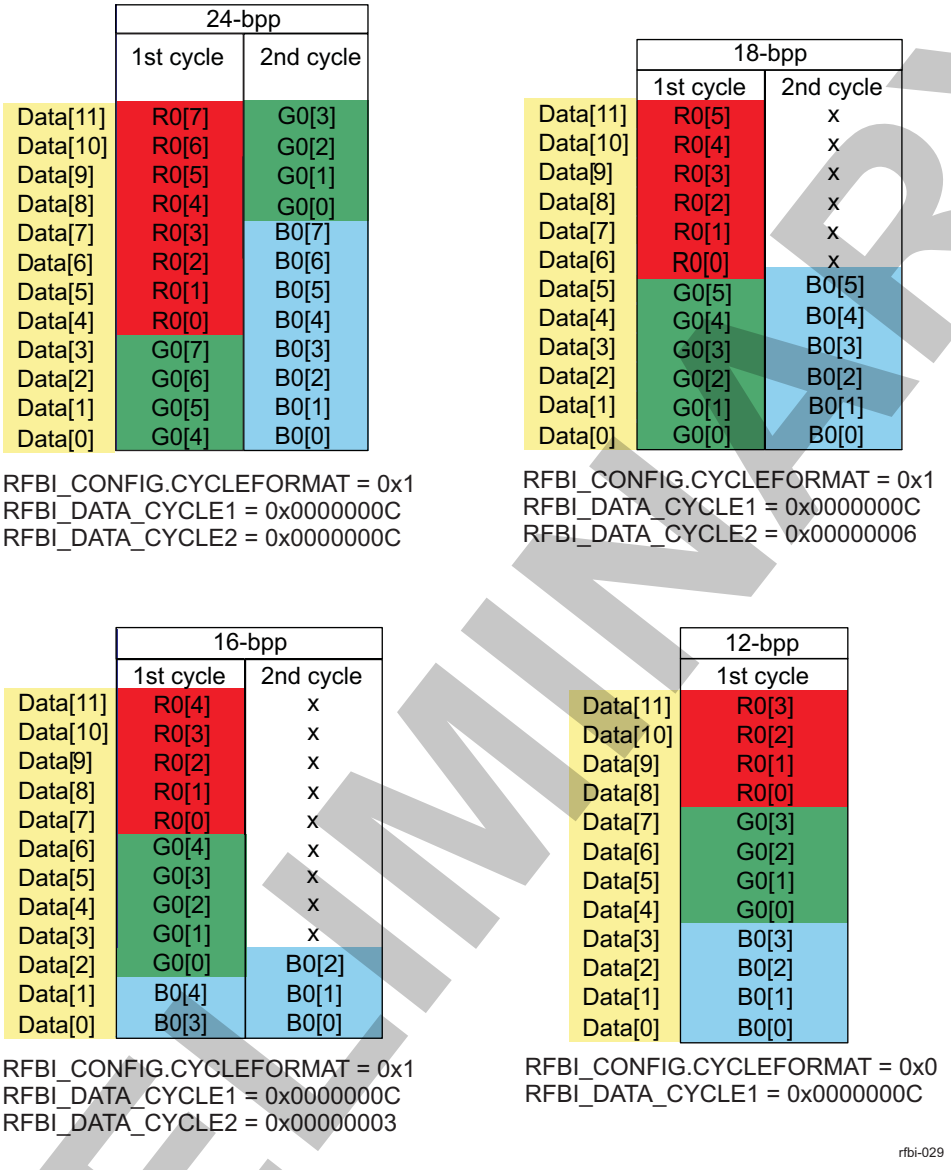

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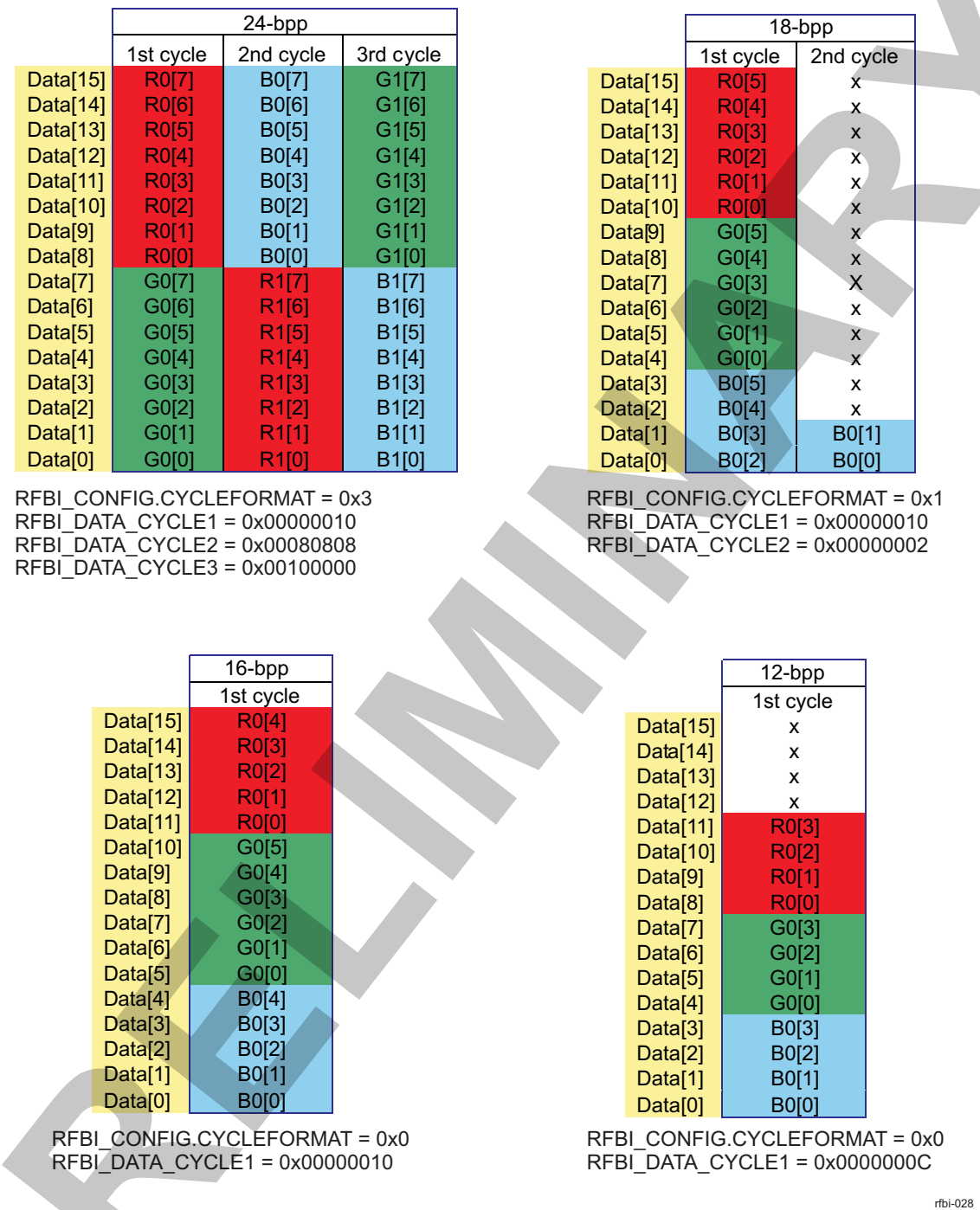
Figure 10-172. 16-Bit Interface Settings



10.5.4.9.2 RFBI Unmodified Bits

In a cycle, if every bit in the interface does not have a pixel value, the status of the unused bits can be programmed to be 0, 1, or the previous value (I/O power consumption optimization). Based on the configuration, the undefined bits for each cycle are defined with the previous values of the bits at the same position in the previous cycle, 0s, or 1s (the unused bits can be at any position). The RFBI_CONFIG[12:11] UNUSEDBITS bit field is used.

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10.5.4.9.3 RFBI Number of Pixels to Transfer

The RFBI_PIXEL_CNT[31:0] PIXELCNT bit field indicates the number of pixels to be transferred to the LCD panel. The value can be changed only when the RFBI_CONTROL[0] ENABLE bit is reset.

During the transfer, the hardware decrements the register when a pixel is sent to the RFB. When the RFBI_CONTROL[0] ENABLE bit is set and a new value is written in the RFBI_PIXEL_CNT register, and the current value in the register is a not 0 (the remaining number of pixels to transfer), the ongoing transfer is aborted.

10.5.4.10 RFBI Timing Generator

10.5.4.10.1 RFBI Configuration Selection

The RFBI_CONTROL[3:2] CONFIGSELECT bit field selects the chip-select.

10.5.4.10.2 RFBI Read/Write

Depending on the status of A0, WE, and RE, the commands and display/parameter data are written to the panel (handled by the state-machine for the commands/parameter data and stored in memory for the display data), or the display data/status values are read from the LCD panel (status and display data in the LCD panel memory). The polarity of A0 (RFBI_A0 signal), WE (RFBI_WE signal), RE (RFBI_RE signal), and CS0 (RFBI_CS0 signal) is programmable.

Table 10-689 describes the read/write function.

Table 10-689. RFBI Read/Write Function Description

A0 (RFBI_A0)	WE (RFBI_WE)	RE (RFBI_RE)	Function Description
1	0	1	Display data write, parameter data write
1	1	0	Display data read
0	1	0	Status read
0	0	1	Command data write

A minimum of RFBI_Cs cycle time, as defined in Table 10-690, is required to keep the RFBI_CS0 signal asserted between write transfers of multiple pixels.

Table 10-690 lists the minimum cycle time for RFBI_CS0, depending on the source of pixels (DISPC or slave port) and the cycle format (1pixel/cycle, 1 pixel/2 cycles, or 1 pixel/3 cycles).

Table 10-690. RFBI Minimum Cycle Time for CS0/WE Always Asserted

RFBI Performance	RFBI_CONFIG[10:9] CYCLEFORMAT	RFBI_CONFIG[8:7] PORTFORMAT	Minimum Cycle Time (in Number of RFBI_ICLK Clock Cycles)
Slave port interconnect	1 pixel/cycle	1 pixel	5
	1 pixel/2 cycles	1 pixel	4
	1 pixel/3 cycles	1 pixel	4
	1 pixel/cycle	2 pixels	4
	1 pixel/2 cycles	2 pixels	4
	1 pixel/3 cycles	2 pixels	4
DISPC	1 pixel/cycle	N/A	4
	1 pixel/2 cycles	N/A	3
	1 pixel/3 cycles	N/A	3
	2 pixel/3 cycles	N/A	6

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10.5.4.10.3 RFBI State-Machine

The RFBI_A0, RFBI_RE, and RFBI_WE signals are asserted and deasserted based on the register accessed (RFBI_CMD, RFBI_PARAM, RFBI_DATA, RFBI_READ, or RFBI_STATUS). (See Table 10-689.) When the RFBI_SYSSTATUS[8] BUSY bit is set by hardware, any access to the registers is stalled, except for the RFBI_DATA register.

The RFBI_SYSSTATUS[9] BUSYRFBIDATA bit indicates whether there are still pending data in the interconnect FIFO associated with the RFBI_DATA register only.

- Command register

  Write one command at a time by writing through the slave port interconnect into the RFBI_CMD register. If the previous command is not processed, the RFBI_SYSSTATUS[8] BUSY bit is set by hardware and access to writing a new command is stalled.

- Parameter register

  Write one parameter at a time by writing in the RFBI_PARAM register.

  If the previous parameter is not processed, the RFBI_SYSSTATUS[8] BUSY bit is set by hardware and access to writing a new parameter is stalled.

- Data register

  Write one or two pixels at a time by writing in the RFBI_DATA register.

  The pixels are formatted based on the specified cycle format. If two pixels are written into the 32-data register, the RFBI_CONFIG[8:7] PORTFORMAT bit field indicates the number of pixels for each slave port access to the register and the order of the pixels.

  If the previous data are not processed, the RFBI_SYSSTATUS[8] BUSY bit is set by hardware and any access for writing new data is stalled. When the RFBI_SYSSTATUS[8] BUSY bit is reset by hardware, access is not stalled.

- Read/status register

  Send through the command and parameter registers the correct information to receive data in the data or status register. The read data from the LCD panel is initiated by writing into the RFBI_READ or RFBI_STATUS registers. In this case, the RFBI_SYSSTATUS[8] BUSY bit is set until the data are available in the register.

  When the RFBI_SYSSTATUS[8] BUSY bit is set by hardware, the read or write access is stalled until the register is updated with a new value from the LCD panel. To avoid the stall, the software can poll the RFBI_SYSSTATUS[8] BUSY bit until it is reset by hardware. To receive the data, send the appropriate command/parameters.

10.5.4.10.4 RFBI Timings

The timing registers can be accessed only when there is no transaction in progress (based on the value of the RFBI_CONTROL[3:2] CONFIGSELECT bit field). Granularity is defined using the RFBI_CONFIG[4] TIMEGRANULARITY bit. This feature allows the extension of programmable ranges of timing parameters for the RFBI interface. See Table 10-691 for the configuration values of the timing bits.

- Chip-select assertion/deassertion time (CSOnTime/CSOffTime)

  RFBI_A0 setup time to chip-select assertion is assured by the programmable chip-select assertion time from the start access time:
  RFBI_ONOFF_TIME[3:0] CSONTIME bit field

  The chip-select deassertion time from the start access time is programmable:
  RFBI_ONOFF_TIME[9:4] CSOFFTIME bit field

CAUTION

Configuring RFBI_ONOFF_TIME[3:0] CSONTIME = RFBI_ONOFF_TIME[9:4] CSOFFTIME = 0 is not supported and must be avoided. This configuration creates contention on the bus and progressively damages the LCD panel.

- Chip-select pulse width (CSPulseWidth)

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The total chip-select pulse width is the time when write cycle time or read cycle time completes and is programmable:
RFBI_CYCLE_TIME[17:12] CSPULSEWIDTH bit field

It applies on the read-to-write, write-to-read, read-to-read, and write-to-write access based on:

– The RFBI_CYCLE_TIME[19] RRENABLE bit: Read-to-read access
– The RFBI_CYCLE_TIME[20] WWENABLE bit: Write-to-write access
– The RFBI_CYCLE_TIME[18] RWENABLE bit: Read-to-write access
– The RFBI_CYCLE_TIME[21] WRENABLE bit: Write-to-read access

By default, it applies to any access (read-to-read, read-to-write, write-to-read, write-to-write) when the chip-select CS0 is activated by setting the RFBI_CONTROL[3:2] CONFIGSELECT bit field to 0x1.

- Access time

  Access time is the time delay between A0 assertion to data sampling before RE signal deassertion; access time is programmable:
  RFBI_CYCLE_TIME[27:22] ACCESSTIME bit field

  When reading the data on the bus, the data are sampled at the end of the access time, which occurs before the end of the read off time (RFBI_ONOFF_TIME[29:24] REOFFTIME).

- Write-enable cycle time (WECycleTime)

  The total write-enable cycle time is the time when A0 becomes valid until write cycle completion; the write-enable cycle time is programmable:
  The RFBI_CYCLE_TIME[5:0] WECYCLETIME bit field

- Write-enable assertion/deassertion time (WEOnTime/WEOffTime)

  The WE assertion delay time from start access time is programmable:
  RFBI_ONOFF_TIME[13:10] WEONTIME bit field

  The WE deassertion delay time from the start access time is programmable:
  RFBI_ONOFF_TIME[19:14] WEOFFTIME bit field

- Read-enable cycle time (RECycleTime)

  The total read-enable cycle time is the time when A0 becomes valid until read cycle completion; the read-enable cycle time is programmable:
  The RFBI_CYCLE_TIME[11:6] RECYCLETIME bit field

- Read-enable assertion/deassertion time (REOnTime/REOffTime)

  The RE assertion delay time from the start access time is programmable:
  RFBI_ONOFF_TIME[23:20] REONTIME bit field

  The RE deassertion delay time from the start access time is programmable:
  RFBI_ONOFF_TIME[29:24] REOFFTIME bit field

At cycle time completion (read access or write access), all control signals (RFBI_CS0, RFBI_WE, and RFBI_RE) are deasserted regardless of their deassertion time parameter values, if they are not deasserted already.

However, an exception to this forced deassertion exists when a pipelined request to CS0 is pending. Also, a control signal with deassertion time parameters equal to the cycle time parameter is not necessarily deasserted when a pipelined request to the same chip-select or different chip-select is pending. This prevents any unnecessary glitch transitions.

If no inactive cycles are required between successive accesses to the same chip-select (the RFBI_CYCLE_TIME[17:12] CSPULSEWIDTH bit field = 0), and if assertion time parameters associated with the following access equal 0, the asserted control signals (RFBI_CS0, RFBI_WE, and RFBI_RE) stay asserted. This applies only to write-to-write access combination. In case of read-to-write, read-to-read, or write-to-read sequences, the RFBI_CS0, RFBI_WE, and RFBI_RE signals are always deasserted.

Table 10-691 lists the configuration values for each timing bit.

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Table 10-691. RFBI Timings Configuration

Timing Configuration Bits	Granularity[1]	
	One	Two
RFBI_ONOFF_TIME[3:0] CSONTIME	0 to 15	0 to 30
RFBI_ONOFF_TIME[9:4] CSOFFTIME	0 to 63	0 to 126
RFBI_CYCLE_TIME[17:12] CSPULSEWIDTH	0 to 63	0 to 126
RFBI_CYCLE_TIME[27:22] ACCESSTIME	0 to 63	0 to 126
RFBI_CYCLE_TIME[5:0] WECYCLETIME	0 to 63	0 to 126
RFBI_ONOFF_TIME[13:10] WEONTIME	0 to 15	0 to 30
RFBI_ONOFF_TIME[19:14] WEOFFTIME	0 to 63	0 to 126
RFBI_CYCLE_TIME[11:6] RECYCLETIME	0 to 63	0 to 126
RFBI_ONOFF_TIME[23:20] REONTIME	0 to 15	0 to 30
RFBI_ONOFF_TIME[29:24] REOFFTIME	0 to 63	0 to 126

(1) Number of RFBI_ICLK clock cycles. The granularity can be configured using the RFBI_CONFIG[4] TIMEGRANULARITY bit.

10.5.4.11 RFBI Trigger Detection Logic

10.5.4.11.1 RFBI Trigger Mode

Setting the RFBI_CONFIG[3:2] TRIGGERMODE bit field configures the different trigger modes:

- Internal trigger mode with the internal programmable RFBI_CONTROL[4] ITE bit
- External trigger mode with the external TE signal (RFBI_TE_VSYNC)
- External trigger mode with the external VSYNC/HSYNC signals

10.5.4.11.2 RFBI Internal Trigger Mode

10.5.4.11.2.1 RFBI ITE Bit

Set the RFBI_CONTROL[4] ITE bit to start capturing the data from the DISPC. The DISPC must be configured in the RFBI mode to account for the RFBI_DISPC_STALL signal. Setting the trigger mode to external (RFBI_CONFIG[3:2] TRIGGERMODE bit field set to 0x1 or 0x2) causes the RFBI_CONTROL[4] ITE bit to be ignored. The chip-select CS0 must be selected (RFBI_CONTROL[3:2] CONFIGSELECT set to 0x1) when this bit is set by users.

10.5.4.11.3 RFBI External Trigger Mode

There are two external trigger modes:

- TE only: VSYNC and HSYNC are merged by logical OR operation and are detected through VSYNC and HSYNC pulse widths.
- HSYNC/VSYNC: This mode uses the two external signals, which are detected through VSYNC and HSYNC pulse widths.

10.5.4.11.3.1 RFBI Programmable Line Number

When the trigger mode is set to external trigger mode with HSYNC and VSYNC or the TE, hardware resets the line counter when the VSYNC occurs and, after a programmable number of lines programmed by the user in the RFBI_LINE_NUMBER[10:0] LINENUMBER bit field (the HSYNC pulse occurs for every line), the transfer to the LCD panel begins. When the programmable line number is 0, only the VSYNC pulse indicates the beginning of the transfer in both modes: HSYNC/VSYNC and TE (logical OR operation between HSYNC and VSYNC).

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10.5.4.11.3.2 RFBI VSYNC Pulse Width (Minimum Value)

The RFBI_VSYNC_WIDTH[15:0] MINVSYNCPULSEWIDTH bit field defines the minimum number of RFBI_ICLK clock cycles of the VSYNC pulse for detection on VSYNC. It allows differentiation between VSYNC and HSYNC, which are ORed on the same signal, and is also used in HSYNC/VSYNC mode on the two separate input lines.

- The VSYNC pulse width must be equal to at least two RFBI_ICLK clock cycles when HSYNC is not present (TE trigger mode only).
- The VSYNC pulse width must be equal to at least four RFBI_ICLK clock cycles when HSYNC is present (TE trigger mode only).

10.5.4.11.3.3 RFBI HSYNC Pulse Width (Minimum Value)

The RFBI_HSYNC_WIDTH[15:0] MINHSYNCPULSEWIDTH bit field defines the minimum number of RFBI_ICLK clock cycles of the HSYNC pulse for detection on HSYNC. It allows differentiation between VSYNC and HSYNC, which are ORed on the same signal, and is also used in VSYNC/HSYNC mode on the separate two input lines. To be detected, the HSYNC/VSYNC pulse width must always be equal to at least two RFBI_ICLK clock cycles. See Table 10-692.

Table 10-692. RFBI Minimum Pulse Width (HSYNC/VSYNC)

Configuration Bits	TE Mode	HSYNC/VSYNC Mode
RFBI_HSYNC_WIDTH[15:0] MINHSYNCPULSEWIDTH field value	2	2
RFBI_VSYNC_WIDTH[15:0] MINVSYNCPULSEWIDTH field value	4	2

The pulse received by the RFBI must be at least two RFBI_ICLK clock cycles to be detected. For the TE mode, since the minimum value to differentiate VSYNC and HSYNC is two RFBI_ICLK clock cycles, the VSYNC pulse width must be at least four RFBI_ICLK clock cycles and the HSYNC pulse width must be at least two RFBI_ICLK clock cycles.

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10.5.5 RFBI Programming Guide

10.5.5.1 RFBI Low-Level Programming Models

This section covers the low-level hardware programming sequences for configuration and use of the RFBI.

10.5.5.1.1 RFBI Global Initialization

10.5.5.1.1.1 RFBI Surrounding Modules Global Initialization

This section identifies the requirements to initialize the surrounding modules when the RFBI is to be used for the first time after a device reset. This initialization of the surrounding modules is based on the integration and environment of the RFBI. For more information, see Section 10.5.2, *RFBI Environment*, and Section 10.5.3, *RFBI Integration*.

Table 10-693 describes the global initialization of surrounding modules.

Table 10-693. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	RFBI_ICLK interface clock must be enabled. For more information, see , *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
DISPC	RFBI_FCLK1 and RFBI_FCLK2 functional clocks must be enabled (see Section 10.2.1, DISPC Overview).
Control module	rfbi_re pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_we pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_cs0 pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_te_vsync0 pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_data[15:0] pads muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_hsync0 pad muxing must be set in the SYSCTRL_PADCONF_CORE module. rfbi_a0 pad muxing must be set in the SYSCTRL_PADCONF_CORE module. For more information, see , *Pad Functional Multiplexing and Configuration*, in *Chapter 18, Control Module*.
MPU INTC	MPU interrupt controller configuration must be done to enable the interrupts from the DISPC module. For more information, see , *Interrupt Controllers Overview*, in *Chapter 17, Interrupt Controllers*.
DMA_SYSTEM	DMA configuration must be done to enable the RFBI module DMA channel requests. For more information, see , *DMA_SYSTEM Module Overview*, in Chapter 16*System DMA*.
Interconnect	For more information about the interconnect configuration, see , *L3 Interconnect*, in *Chapter 14, Interconnects*.

NOTE: The MPU INTC and the DMA_SYSTEM configurations are necessary if the interrupt- and DMA-based communication modes are used.

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10.5.5.1.1.2 RFBI Global Initialization

10.5.5.1.1.2.1 RFBI Main Sequence RFBI Global Initialization

This procedure initializes the RFB and DISPC after a power on or software reset (see Table 10-694).

Table 10-694. RFBI Global Initialization

Step	Register/Bit Field Programming Model	Value
DISPC configuration in RFBI mode	See Section 10.5.5.1.1.2.2, *Subsequence: DISPC Configuration.*	
RFBI configuration	See Section 10.5.5.1.1.2.3, *Subsequence: RFBI Configuration.*	
LCD panel configuration	See Section 10.5.5.1.1.2.4, *Subsequence: LCD Panel Configuration*.	

10.5.5.1.1.2.2 RFBI Subsequence: DISPC Configuration

This procedure configures the DISPC registers in RFBI mode (see Table 10-695).

Table 10-695. RFBI DISPC Configuration in RFBI Mode

Step	Register/Bit Field Programming Model	Value
DISPC pipeline configuration	Configuration of the pipeline associated with the LCD output, such as the DMA engine and pipelines associated with the LCD output (see DISPC Overview, in *Display Controller*).	
Enable TFT mode.	DISPC_CONTROLo[3] STNTFT	0x1
Program the DISPC in RFBI mode.	DISPC_CONTROLo[11] STALLMODE	0x1
Reset the DISPC signal configuration to default value.	DISPC_POL_FREQo	0x00
Select the RFBI data path.	DISPC_CONTROL1[16:15] GPOUT	0x1
Enable the hardware handshake to avoid the DISPC FIFO underflow (applies to the pipeline connected to the LCD output).	DISPC_CONFIGo[16] BUFFERHANDCHECK	0x1

NOTE: In RFBI mode, the DISPC_CONTROLo[5] GOLCD bit must not be set to 1. It must be disabled before resetting the DISPC_CONTROLo[11] STALLMODE bit to 0.

The hardware handshake applies to the pipelines connected to the LCD output. It must be disabled before resetting the DISPC_CONTROLo[11] STALLMODE bit to 0.

10.5.5.1.1.2.3 RFBI Subsequence: RFBI Configuration

This procedure configures the RFBI registers. See Table 10-696.

CAUTION

The RFBI configuration registers for CS0 configuration can be accessed only when the configuration is not in use (that is, when the RFBI_CONTROL[3:2] CONFIGSELECT is set to 0x0).

Table 10-696. RFBI Configuration – Main Sequence

Step	Register/Bit Field Programming Model	Value
Enable the RFBI data path.	RFBI_CONTROL[1] RFBIMODE	0x0
DMA mode configuration	See Section 10.5.5.1.1.2.3.1, *Subsequence: DMA Mode Configuration.*	

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Table 10-696. RFBI Configuration – Main Sequence (continued)

Step	Register/Bit Field Programming Model	Value
Disable the chip-select and configuration (this step is necessary to configure the timing registers).	RFBI_CONTROL[3:2] CONFIGSELECT	0x0
Timing and polarity signals configuration	See Section 10.5.5.1.1.2.3.2, *Subsequence: Timing and Polarity Signals Configuration*.	
Configure the parallel input data width.	RFBI_CONFIG[6:5] DATATYPE	x(1)
Configure the number of cycles.	RFBI_CONFIG[10:9] CYCLEFORMAT	x(1)
Trigger mode settings	See Section 10.5.5.1.1.2.3.3, *Subsequence: Trigger Mode Settings*.	
Program the data format per cycle.	RFBI_DATA_CYCLE_1	xxx(1)
	RFBI_DATA_CYCLE_2	xxx(1)
	RFBI_DATA_CYCLE_3	xxx(1)
Select the configuration of CS0	RFBI_CONTROL[3:2] CONFIGSELECT	0x1

(1) Values depend on the application

10.5.5.1.1.2.3.1 RFBI Subsequence: DMA Mode Configuration

Figure 10-173 shows DMA mode configuration.

Figure 10-173. RFBI DMA Mode Configuration

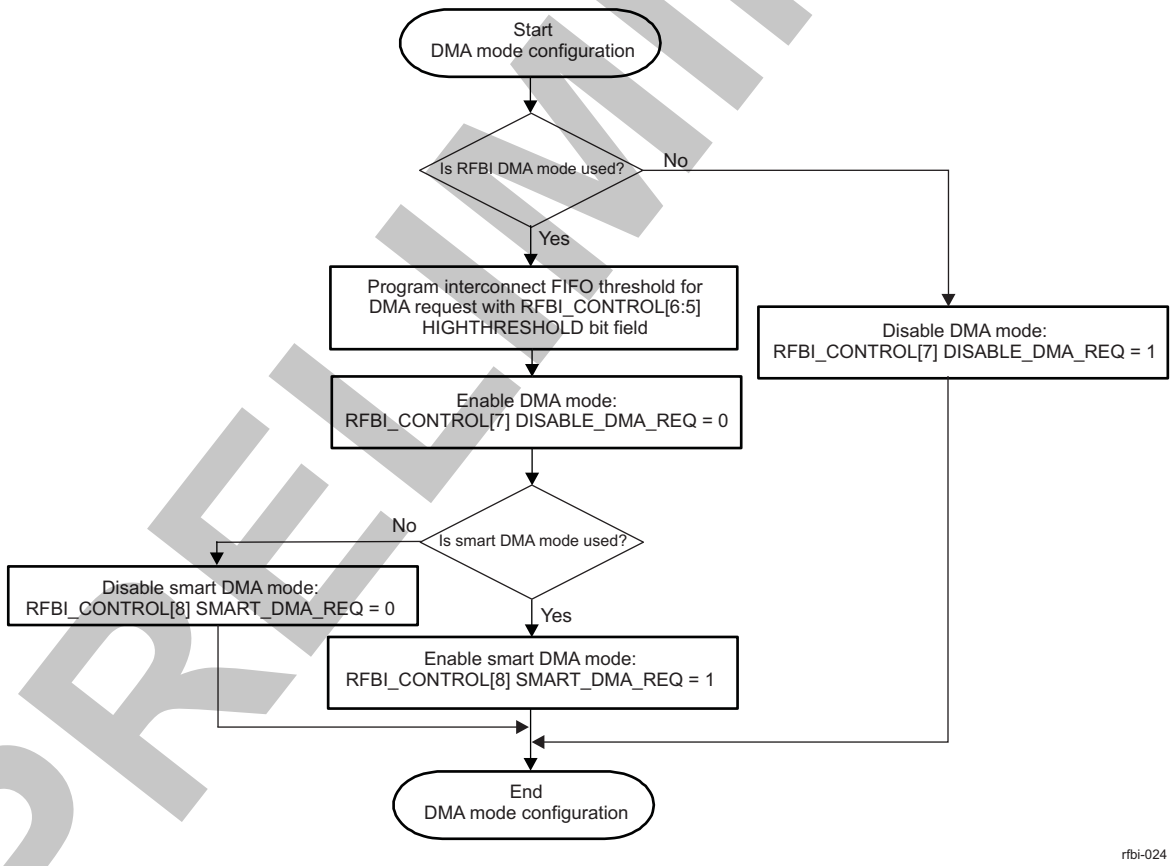

Table 10-697 describes the DMA mode configuration.

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Table 10-697. Register Call Summary for Subsequence: DMA Mode Configuration

Register Name
RFBI_CONTROL

10.5.5.1.1.2.3.2 RFBI Subsequence: Timing and Polarity Signals Configuration

Table 10-698 describes timing and polarity signals configuration.

Table 10-698. RFBI Timing and Polarity Signals Configuration

Step	Register/Bit Field Programming Model	Value
Program ON/OFF timings.	RFBI_ONOFF_TIME	xxx(1)
Program cycle timings.	RFBI_CYCLE_TIME	xxx(1)
Program CS polarity.	RFBI_CONFIG[19] CSPOLARITY	x(1)
Program WE polarity.	RFBI_CONFIG[18] WEPOLARITY	x(1)
Program RE polarity.	RFBI_CONFIG[17] REPOLARITY	x(1)
Program A0 polarity.	RFBI_CONFIG[16] A0POLARITY	x(1)
Program unused bits.	RFBI_CONFIG[12:11] UNUSEDBITS	x(1)
Program the factor x2 latency.	RFBI_CONFIG[4] TIMEGRANULARITY	x(1)

(1) Values depend on the application.

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10.5.5.1.1.2.3.3 RFBI Subsequence: Trigger Mode Settings

Figure 10-174 shows trigger mode settings.

Figure 10-174. RFBI Trigger Mode Settings

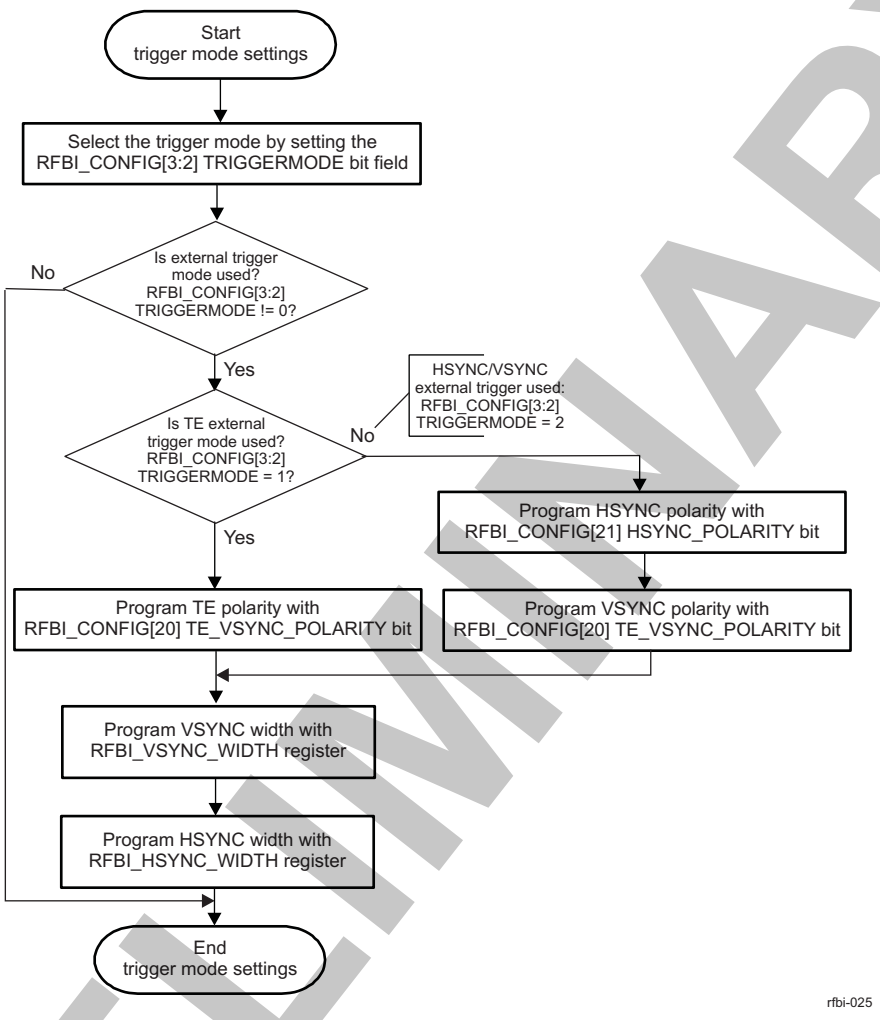

Table 10-699 describes the register call summary for subsequence: trigger mode settings

Table 10-699. Register Call Summary for Subsequence: Trigger Mode Settings

Register Name		
RFBI_CONFIG	RFBI_VSYNC_WIDTH	RFBI_HSYNC_WIDTH

10.5.5.1.1.2.4 RFBI Subsequence: LCD Panel Configuration

This procedure consists of sending and receiving commands. See Table 10-700 and Table 10-701.

Table 10-700. RFBI Command Interface: Writing Command to the LCD Panel

Step	Register/Bit Field Programming Model	Value
Write command to the LCD panel.	RFBI_CMD[8:0] CMD	0x(1)
Wait until BUSY != 1.	RFBI_SYSSTATUS[8] BUSY	

(1) Value depends on the command sent to the LCD panel.

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Table 10-701. RFBI Command Interface: Reading Command From the LCD Panel

Step	Register/Bit Field Programming Model	Value
Initialize reading command.	RFBI_STATUS[8:0] STATUS	0x
Initialize reading command.	RFBI_READ [8:0] READ	0x
Wait until BUSY != 1.	RFBI_SYSSTATUS[8] BUSY	
Read command from the LCD panel.	RFBI_STATUS[8:0] STATUS	0x(1)
	RFBI_READ [8:0] READ	0x(1)

(1) Value depends on the command read from the LCD panel.

10.5.5.1.2 RFBI Operational Modes Configuration

10.5.5.1.2.1 RFBI Start Transfer

10.5.5.1.2.1.1 RFBI Main Sequence: RFBI Start Transfer With Polling Method

Table 10-702 describes the RFBI start transfer polling method.

Table 10-702. RFBI Start Transfer With Polling Method

Step	Register/Bit Field Programming Model	Value
Enable DISPC module output.	See Section 10.5.5.1.2.1.4, *Subsequence: DISPC Output Enable.*	
Enable RFBI module output.	See Section 10.5.5.1.2.1.5, *Subsequence: RFBI Interrupts Enable.*	
Detect event.	See Table 10-708.	

10.5.5.1.2.1.2 RFBI Main Sequence: RFBI Start Transfer With Interrupts and DMA Method

Table 10-703 describes the RFBI start transfer interrupts method.

Table 10-703. RFBI Start Transfer With Interrupts Method

Step	Register/Bit Field Programming Model	Value
Enable DISPC interrupts.	See Table 10-704.	
Enable DISPC module output.	See Section 10.5.5.1.2.1.4, *Subsequence: DISPC Output Enable.*	
Enable RFBI module output.	See Section 10.5.5.1.2.1.5, *RFBI Interrupts Enable*.	
Detect Event.	See Table 10-708.	

10.5.5.1.2.1.3 RFBI Subsequence: DISPC Interrupts Enable

This procedure enables the DISPC interrupts used in RFBI mode (see Table 10-704).

Table 10-704. DISPC Interrupts Enable

Step	Register/Bit Field Programming Model	Value
Clear all interrupts.	DISPC_IRQSTATUS	0xFFFF
Enable the FRAMEDONEi IRQ.	DISPC_IRQENABLE FRAMEDONEi_EN	0x1
Enable the BUFFERUNDERFLOW IRQ.	DISPC_IRQENABLE BUFFERUNDERFLOW_EN	0x1
Enable the SYNCLOSTi IRQ.	DISPC_IRQENABLE SYNCLOSTi_EN	0x1

NOTE: The other DISPC interrupts requests can also be enabled, depending on the application.

10.5.5.1.2.1.4 RFBI Subsequence: DISPC Output Enable

This procedure enables the DISPC output. See Table 10-705.

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Table 10-705. DISPC Output Enable

Step	Register/Bit Field Programming Model	Value
Enable the video or GFX pipeline.	DISPC_VIDp_ATTRIBUTES[0] ENABLE	0x1
	DISPC_GFX_ATTRIBUTES[0] ENABLE	0x1
Enable the DISPC output.	DISPC_CONTROLo[0] LCDENABLE	0x1

10.5.5.1.2.1.5 RFBI Subsequence: RFBI Output Enable

This procedure enables the RFBI output. Figure 10-175 details the settings for this subsequence.

Figure 10-175. RFBI Output Enable Flow Chart

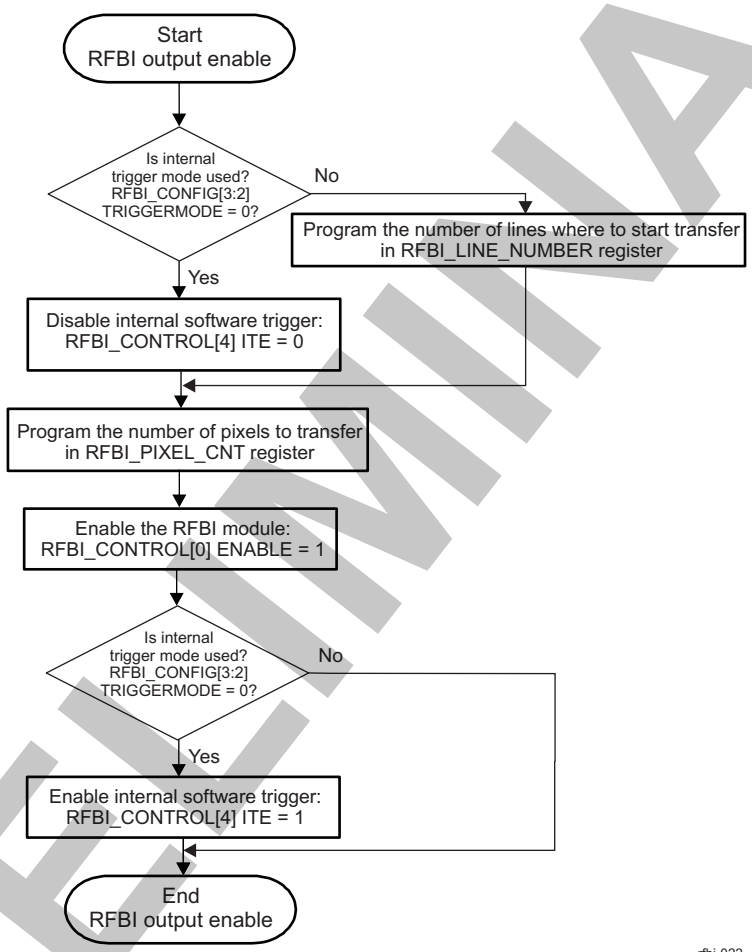

Table 10-706 describes the RFBI output enable.

Table 10-706. Register Call Summary for Subsequence: RFBI Output Enable

Register Name		
RFBI_CONFIG	RFBI_CONTROL	RFBI_LINE_NUMBER
RFBI_PIXEL_CNT		

Table 10-707 describes the RFBI behavior depending on the RFBI output enable.

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Table 10-707. RFBI Behavior

RFBI_CONTROL[0] ENABLE Bit Value	RFBI Behavior
0	Slave port interconnect can write command/parameter/data and read data/status from the RFB. Slave port interconnect access can only be done to the active CS0.
1	The DISPC sends pixels to the RFB.

NOTE: The LCD output is disabled at the end of the transfer of the frame. The software must reenable the LCD output to generate a new frame by setting the DISPC_CONTROLo[0] LCDENABLE bit to 1.

CAUTION

The following registers must not be modified when the module is enabled (the RFBI_CONTROL[0] ENABLE bit is set to 1):

- RFBI_CONTROL
- RFBI_PIXEL_CNT
- RFBI_LINE_NUMBER
- RFBI_STATUS
- RFBI_CONFIG
- RFBI_ONOFF_TIME
- RFBI_CYCLE_TIME
- RFBI_DATA_CYCLEi (i = 1 to 3)
- RFBI_VSYNC_WIDTH
- RFBI_HSYNC_WIDTH

NOTE: The RFBI_DISPC_STALL signal is asserted when the RFBI is disabled. Pixels can be sent to the LCD panel through the slave port only when the pixel count has reached 0x0.

10.5.5.1.2.1.6 RFBI Subsequence: Detect Event

Table 10-708 describes the detect event.

Table 10-708. RFBI Detect Event

Step	Register/Bit Field Programming Model	Value
Wait until DISPC_IRQSTATUS != 0.	DISPC_IRQSTATUS	
Service event	See Section 10.5.5.1.3, *RFBI Events Servicing*.	

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10.5.5.1.3 RFBI Events Servicing

10.5.5.1.3.1 RFBI FRAMEDONE Interrupt Servicing

The FRAMEDONE event occurs each time a frame is transferred to the LCD panel. Figure 10-176 details how to serve this event.

Figure 10-176. RFBI FRAMEDONE Event Servicing Flow Chart

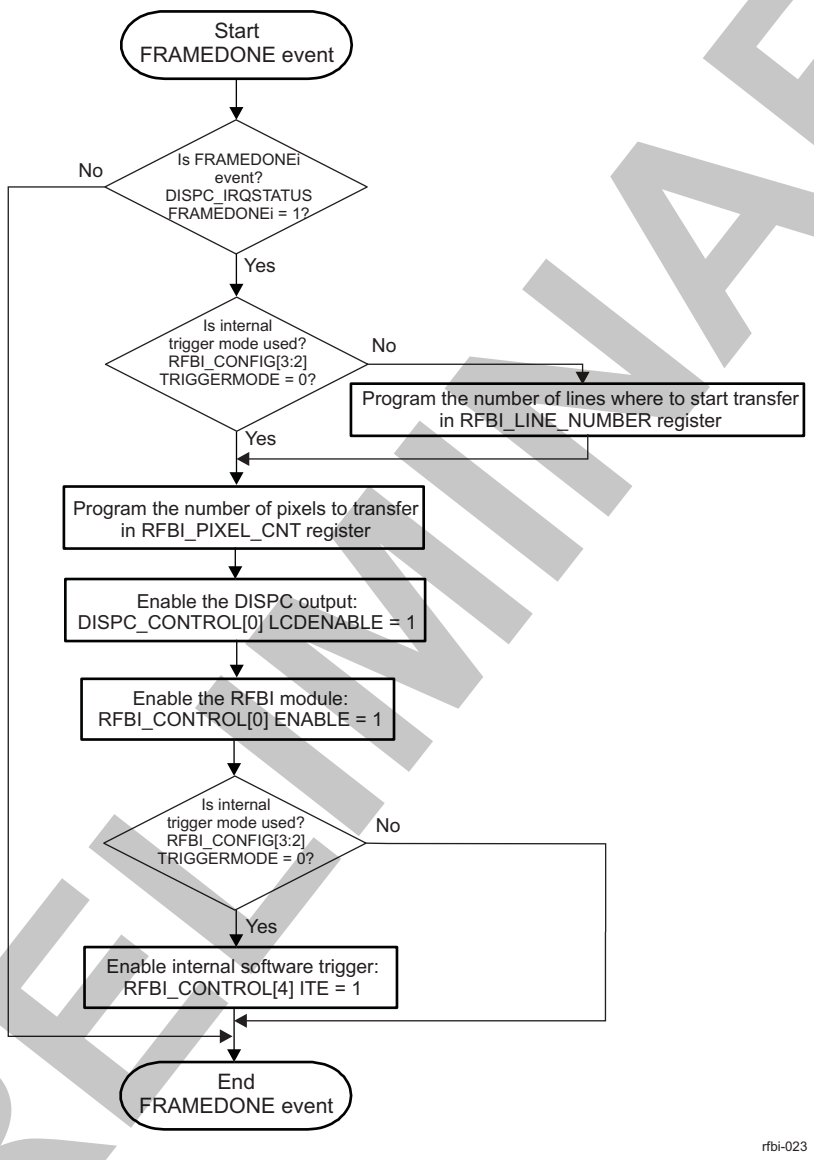

Table 10-709 describes FRAMEDONE interrupt servicing.

Table 10-709. Register Call Summary for RFBI Events Servicing: FRAMEDONE Interrupt Servicing

Register Name		
DISPC_IRQSTATUS	RFBI_CONFIG	RFBI_LINE_NUMBER
RFBI_PIXEL_CNT	DISPC_CONTROL	RFBI_CONTROL

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10.5.6 RFBI Hardware Status Features

Table 10-710 lists the RFBI hardware status features.

Table 10-710. RFBI Hardware Status Features

Feature	Type	Register/Bit Field/Observability Control	Description
Data pending	Status	RFBI_SYSTATUS[9] BUSYRFBIDATA	It is set to 1 when some data are pending to be processed from the interconnect FIFO.
Slave port bus busy	Status	RFBI_SYSTATUS[9] BUSY	It is set to 1 when the slave port bus is busy and access to some RFBI registers (RFBI_CMD, RFBI_STATUS, RFBI_PARAM, and RFBI_READ) is stalled.

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10.5.7 RFBI Register Manual

10.5.7.1 RFBI Instance Summary

Table 10-711. RFBI Instance Summary

Module Name	L3_MAIN Base Address	Size
RFBI	0x5800 2000	256 Bytes

10.5.7.2 RFBI Registers

10.5.7.2.1 RFBI Register Summary

Table 10-712. RFBI Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3_MAIN Physical Address
RFBI_REVISION	R	32	0x0000 0000	0x5800 2000
RFBI_SYSCONFIG	RW	32	0x0000 0010	0x5800 2010
RFBI_SYSSTATUS	R	32	0x0000 0014	0x5800 2014
RFBI_CONTROL	RW	32	0x0000 0040	0x5800 2040
RFBI_PIXEL_CNT	RW	32	0x0000 0044	0x5800 2044
RFBI_LINE_NUMBER	RW	32	0x0000 0048	0x5800 2048
RFBI_CMD	W	32	0x0000 004C	0x5800 204C
RFBI_PARAM	W	32	0x0000 0050	0x5800 2050
RFBI_DATA	W	32	0x0000 0054	0x5800 2054
RFBI_READ	RW	32	0x0000 0058	0x5800 2058
RFBI_STATUS	RW	32	0x0000 005C	0x5800 205C
RFBI_CONFIG	RW	32	0x0000 0060	0x5800 2060
RFBI_ONOFF_TIME	RW	32	0x0000 0064	0x5800 2064
RFBI_CYCLE_TIME	RW	32	0x0000 0068	0x5800 2068
RFBI_DATA_CYCLEi [(1)]	RW	32	0x0000 006C + (0x04 * i)[(1)]	0x5800 206C + (0x04 * i)[(1)]
RFBI_VSYNC_WIDTH	RW	32	0x0000 0090	0x5800 2090
RFBI_HSYNC_WIDTH	RW	32	0x0000 0094	0x5800 2094

(1) i = 0 to 2

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10.5.7.2.2 RFBI Register Description

Table 10-713. RFBI_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5800 2000	**Instance**	RFBI
Description	This register contains the IP revision.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1)

(1) Ti internal data

Table 10-714. Register Call Summary for Register RFBI_REVISION

Remote Frame Buffer Interface

- RFBI Register Summary: [0]

Table 10-715. RFBI_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5800 2010	**Instance**	RFBI
Description	This register controls various parameters of the slave port interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED	RESERVED	SIDLEMODE			RESERVED	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0000000
6	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0
5	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0
4:3	SIDLEMODE	Slave interface power management, idle req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged. 0x2: Smart-idle. Acknowledgment to an idle request is given based on the internal activity of the module.	RW	0x0
2	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0
1	SOFTRESET	Software reset Sets this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads, it always returns 0. 0x0: Normal mode 0x1: The module is reset.	RW	0

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Bits	Field Name	Description	Type	Reset
0	AUTOIDLE	Internal clock gating strategy (RFBI_ICLK clock and DISPC clock) 0x0: RFBI_ICLK clock and DISPC clock are free-running 0x1: Automatic clock gating strategy is applied for the RFBI_ICLK clock and DISPC clock, based on the slave port interface and internal activity.	RW	1

Table 10-716. Register Call Summary for Register RFBI_SYSCONFIG

Remote Frame Buffer Interface

- RFBI Software Reset: [0] [1]
- RFBI Power Management: [2] [3]
- RFBI Register Summary: [4]
- RFBI Register Description: [5]

Table 10-717. RFBI_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5800 2014	**Instance**	RFBI
Description	This register provides status information about the module, excluding interrupt status information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						BUSYRFBIDATA	BUSY	RESERVED							RESETDONE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved for module-specific status information. Reads return 0.	RO	0x000000
9	BUSYRFBIDATA	Data are pending to be processed from interconnect FIFO. Read 0x0: No data pending Read 0x1: Some data pending	R	0
8	BUSY	Slave port busy status bit Read 0x0: Access to the following register is not stalled: RFBI_CMD, RFBI_STATUS, RFBI_PARAM, RFBI_READ. Read 0x1: Access to any of the following registers is stalled: RFBI_CMD, RFBI_STATUS, RFBI_PARAM, RFBI_READ.	R	0
7:1	RESERVED	Reserved. Reads return 0.	RO	0x00
0	RESETDONE	Internal reset monitoring. It can be used to determine when a hardware reset is complete or when a software reset is complete (software has set RFBI_SYSCONFIG[0] SOFTRESET to 1). Read 0x0: Internal module reset ongoing Read 0x1: Reset completed	R	1

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Table 10-718. Register Call Summary for Register RFBI_SYSSTATUS

Remote Frame Buffer Interface

- RFBI Software Reset: [0]
- RFBI State-Machine: [1] [2] [3] [4] [5] [6] [7] [8] [9]
- RFBI Global Initialization: [10] [11]
- RFBI Register Summary: [12]

Table 10-719. RFBI_CONTROL

Address Offset	0x0000 0040		
Physical Address	0x5800 2040	**Instance**	RFBI
Description	The register configures the RFBI module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							SMART_DMA_REQ	DISABLE_DMA_REQ	HIGHTHRESHOLD		ITE	CONFIGSELECT		RFBIMODE	ENABLE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x000000
8	SMART_DMA_REQ	Smart DMA request 0x0: The dmareq is asserted and deasserted depending on FIFO space, even if MIdlereq is high in smart-idle/no-idle mode and the entire burst gets error responses from the module. 0x1: The dmareq is deasserted after 2 clock cycles, if it has been asserted for more than or equal to 2 clock cycles and MIdlereq is high in smart-idle or no-idle mode. No more burst requests are given, even if the space is available in the FIFO.	RW	0
7	DISABLE_DMA_REQ	Disable DMA request. 0x0: The dmareq is enabled and the signal is generated based on the space available and the request coming into the data register. 0x1: The dmareq is disabled and the signal is not generated at all based on space in FIFO. It stays high until the DISABLE DM AREQ is high even if there is space in FIFO to take requests.	RW	0
6:5	HIGHTHRESHOLD	Defines the FIFO high threshold used by hardware to assert DMA request. Used only if data written to RFBI_DATA are sent using sDMA. 0x0: Size of the transfer of 4 words of 32 bits wide 0x1: Size of the transfer of 8 words of 32 bits wide 0x2: Size of the transfer of 16 words of 32 bits wide	RW	0x0
4	ITE	Internal trigger 0x0: Hardware waits for the ITE bit to be set if in internal trigger mode for the configuration in use. 0x1: User sets the ITE bit to start the transfer. When hardware takes into account the bit, the hardware resets it.	RW	0

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Bits	Field Name	Description	Type	Reset
3:2	CONFIGSELECT	Select the CS and configuration. 0x0: No CS selected 0x1: CS0 selected 0x2: Reserved 0x3: Reserved	RW	0x0
1	RFBIMODE	RFBI mode 0x0: The RFBI mode is selected. 0x1: The RFBI mode is not selected.	RW	1
0	ENABLE	Enable/disable flag 0x0: Disable the RFBI module. 0x1: Enable the RFBI module.	RW	0

Table 10-720. Register Call Summary for Register RFBI_CONTROL

Remote Frame Buffer Interface

- RFBI Parallel Interface (MIPI DBI Protocol): [0]
- RFBI Description of the Tearing Effect Pulse Signal: [1]
- RFBI DMA Requests: [2]
- RFBI Video Port Description: [3]
- RFBI Stall Mechanism: [4] [5] [6]
- RFBI Using DMA Request With Interconnect FIFO: [7] [8] [9] [10] [11] [12]
- RFBI Number of Pixels to Transfer: [13] [14]
- RFBI Configuration Selection: [15]
- RFBI Timings: [16] [17]
- RFBI Trigger Mode: [18]
- RFBI Internal Trigger Mode: [19] [20] [21]
- RFBI Global Initialization: [22] [23] [24] [25] [26]
- RFBI Operational Modes Configuration: [27] [28] [29] [30]
- RFBI Events Servicing: [31]
- RFBI Register Summary: [32]

Table 10-721. RFBI_PIXEL_CNT

Address Offset	0x0000 0044		
Physical Address	0x5800 2044	**Instance**	RFBI
Description	The register configures the RFBI pixel count value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIXELCNT																															

Bits	Field Name	Description	Type	Reset
31:0	PIXELCNT	Pixel counter value The software indicates the number of pixels to transfer to the LCD panel frame buffer. The value is set when the module is disabled. During the transfer the hardware decrements the register when a pixel is sent to the RFB.	RW	0x0000 0000

Table 10-722. Register Call Summary for Register RFBI_PIXEL_CNT

Remote Frame Buffer Interface

- RFBI Number of Pixels to Transfer: [0] [1]
- RFBI Operational Modes Configuration: [2] [3]
- RFBI Events Servicing: [4]
- RFBI Register Summary: [5]

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Table 10-723. RFBI_LINE_NUMBER

Address Offset	0x0000 0048		
Physical Address	0x5800 2048	**Instance**	RFBI
Description	The register configures the number of lines to synchronize the beginning of the transfer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LINENUMBER							

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x000000
10:0	LINENUMBER	Programmable line number Line number from 0 to 2047. Number of HSYNC after the VSYNC occurs before the beginning of the transfer.	RW	0x000

Table 10-724. Register Call Summary for Register RFBI_LINE_NUMBER

Remote Frame Buffer Interface

- RFBI External Trigger Mode: [0]
- RFBI Operational Modes Configuration: [1] [2]
- RFBI Events Servicing: [3]
- RFBI Register Summary: [4]
- RFBI Register Description: [5] [6]

Table 10-725. RFBI_CMD

Address Offset	0x0000 004C		
Physical Address	0x5800 204C	**Instance**	RFBI
Description	The register configures the RFBI command.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CMD							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x000000
7:0	CMD	Command Value 8/9/12/16 bit value depending on the parallelMode [7:0] 8-bit DataType [8:0] 9-bit DataType [11:0] 12-bit DataType [15:0] 16-bit DataType	W	0x00

Table 10-726. Register Call Summary for Register RFBI_CMD

Remote Frame Buffer Interface

- RFBI State-Machine: [0] [1]
- RFBI Global Initialization: [2]
- RFBI Hardware Status Features: [3]
- RFBI Register Summary: [4]
- RFBI Register Description: [5] [6]

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Table 10-727. RFBI_PARAM

Address Offset	0x0000 0050		
Physical Address	0x5800 2050	**Instance**	RFBI
Description	The register configures the RFBI parameter.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PARAM							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x000000
7:0	PARAM	Parameter value 8/9/12/16 bit value depending on the parallelMode [7:0] 8-bit DataType [8:0] 9-bit DataType [11:0] 12-bit DataType [15:0] 16-bit DataType	W	0x00

Table 10-728. Register Call Summary for Register RFBI_PARAM

Remote Frame Buffer Interface

- RFBI State-Machine: [0] [1]
- RFBI Hardware Status Features: [2]
- RFBI Register Summary: [3]
- RFBI Register Description: [4] [5]

Table 10-729. RFBI_DATA

Address Offset	0x0000 0054		
Physical Address	0x5800 2054	**Instance**	RFBI
Description	The register configures the RFBI data.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	Data value 12/16/18/24/2x16 bit value depending on: DataType [11:0] 12-bit DataType [15:0] 16-bit DataType [17:0] 18-bit DataType [23:0] 24-bit DataType [31:0] 2x16-bit	W	0x0000 0000

Table 10-730. Register Call Summary for Register RFBI_DATA

Remote Frame Buffer Interface

- RFBI Overview: [0] [1]
- RFBI Description: [2] [3] [4]
- RFBI Using DMA Request With Interconnect FIFO: [5] [6] [7]
- RFBI State-Machine: [8] [9] [10] [11]
- RFBI Register Summary: [12]
- RFBI Register Description: [13]

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Table 10-731. RFBI_READ

Address Offset	0x0000 0058		
Physical Address	0x5800 2058	**Instance**	RFBI
Description	The register configures the RFBI read.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								READ							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x000000
7:0	READ	Read value 8/9/12/16 bit value depending on the parallelMode [7:0] 8-bit DataType [8:0] 9-bit DataType [11:0] 12-bit DataType [15:0] 16-bit DataType	RW	0x00

Table 10-732. Register Call Summary for Register RFBI_READ

Remote Frame Buffer Interface

- RFBI State-Machine: [0] [1]
- RFBI Global Initialization: [2] [3]
- RFBI Hardware Status Features: [4]
- RFBI Register Summary: [5]
- RFBI Register Description: [6] [7]

Table 10-733. RFBI_STATUS

Address Offset	0x0000 005C		
Physical Address	0x5800 205C	**Instance**	RFBI
Description	The register configures the RFBI status.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STATUS							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x000000
7:0	STATUS	Status value 8/9/12/16 bit value depending on the parallelMode [7:0] 8-bit DataType [8:0] 9-bit DataType [11:0] 12-bit DataType [15:0] 16-bit DataType	RW	0x00

Table 10-734. Register Call Summary for Register RFBI_STATUS

Remote Frame Buffer Interface

- RFBI State-Machine: [0] [1]
- RFBI Global Initialization: [2] [3]
- RFBI Operational Modes Configuration: [4]
- RFBI Hardware Status Features: [5]
- RFBI Register Summary: [6]
- RFBI Register Description: [7] [8]

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Table 10-735. RFBI_CONFIG

Address Offset	0x0000 0060		
Physical Address	0x5800 2060	**Instance**	RFBI
Description	The control register sets the configuration for the LCD 0, LCD 1, and LCD 2.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										HSYNCPOLARITY	TE_VSYNC_POLARITY	CSPOLARITY	WEPOLARITY	REPOLARITY	A0POLARITY	RESERVED			UNUSEDBITS		CYCLEFORMAT		PORTFORMAT	DATATYPE			TIMEGRANULARITY	TRIGGERMODE		PARALLELMODE	

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x000
21	HSYNCPOLARITY	HSYNC polarity 0x0: HSYNC active low 0x1: HSYNC active high	RW	1
20	TE_VSYNC_POLARITY	TE or VSYNC polarity 0x0: active low 0x1: active high	RW	1
19	CSPOLARITY	CS polarity 0x0: CS active low 0x1: CS active high	RW	0
18	WEPOLARITY	WE polarity 0x0: Active low 0x1: Active high	RW	0
17	REPOLARITY	RE polarity 0x0: Active low 0x1: Active high	RW	0
16	A0POLARITY	A0 polarity 0x0: A0 active low 0x1: A0 active high	RW	1
15:13	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0
12:11	UNUSEDBITS	State of unused bits 0x0: Low level (0) 0x1: High level (1) 0x2: Unchanged from previous state	RW	0x0
10:9	CYCLEFORMAT	Cycle format 0x0: 1 cycle for 1 pixel 0x1: 2 cycles for 1 pixel 0x2: 3 cycles for 1 pixel 0x3: 3 cycles for 2 pixels	RW	0x0

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Bits	Field Name	Description	Type	Reset
8:7	PORTFORMAT	Slave port write access format 0x0: 1 pixel per slave port access to the register data 0x2: 2 pixels per slave port access to the register data with first pixel at the position [15:0] 0x3: 2 pixels per slave port access to the register data with first pixel at the position [31:16]	RW	0x0
6:5	DATATYPE	Data type from the DISPC and slave port 0x0: 12-bit 0x1: 16-bit 0x2: 18-bit 0x3: 24-bit	RW	0x0
4	TIMEGRANULARITY	Multiplies signal timing latencies by 2 0x0: x2 latencies disabled 0x1: x2 latencies enabled	RW	0
3:2	TRIGGERMODE	Trigger mode 0x0: 00 Internal trigger mode (ITE bit mode) 0x1: External trigger mode (Tearing Effect Signal, rfbi_tevsync0 with programmable line counter defined in RFBI_LINE_NUMBER register) 0x2: External trigger mode (rfbi_tevsync0/rfbi_hsync0 with programmable line counter defined in RFBI_LINE_NUMBER register)	RW	0x0
1:0	PARALLELMODE	Parallel mode 0x0: 8-bit parallel output interface selected 0x1: 9-bit parallel output interface selected 0x2: 12-bit parallel output interface selected 0x3: 16-bit parallel output interface selected	RW	0x0

Table 10-736. Register Call Summary for Register RFBI_CONFIG

Remote Frame Buffer Interface

- RFBI Parallel Interface (MIPI DBI Protocol): [0] [1] [2]
- RFBI Description of the Tearing Effect Pulse Signal: [3] [4] [5] [6]
- RFBI Input Formats: [7]
- RFBI Stall Mechanism: [8]
- RFBI Cycle Mode Selection: [9] [10] [11] [12]
- RFBI Unmodified Bits: [13]
- RFBI Read/Write: [14] [15]
- RFBI State-Machine: [16]
- RFBI Timings: [17]
- RFBI Trigger Mode: [18]
- RFBI Internal Trigger Mode: [19]
- RFBI Global Initialization: [20] [21] [22] [23] [24] [25] [26] [27] [28]
- RFBI Operational Modes Configuration: [29] [30]
- RFBI Events Servicing: [31]
- RFBI Register Summary: [32]

Table 10-737. RFBI_ONOFF_TIME

Address Offset	0x0000 0064		
Physical Address	0x5800 2064	**Instance**	RFBI
Description	The control register configures the RFBI timings for the LCD 0, LCD 1, and LCD 2.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REOFFTIME								REONTIME								WEOFFTIME							
																								WEONTIME							
																								CSOFFTIME							
																												CSONTIME			

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0
29:24	REOFFTIME	Read enable deassertion time from start access time. Number of RFBI_ICLK cycles.	RW	0x00
23:20	REONTIME	Read enable assertion time from start access time. Number of RFBI_ICLK cycles.	RW	0x0
19:14	WEOFFTIME	Write enable deassertion time from start access time. Number of RFBI_ICLK cycles.	RW	0x00
13:10	WEONTIME	Write enable assertion time from start access time. Number of RFBI_ICLK cycles.	RW	0x0
9:4	CSOFFTIME	CS deassertion time from start access time Number of RFBI_ICLK cycles	RW	0x00
3:0	CSONTIME	CS assertion time from start access time Number of RFBI_ICLK cycles	RW	0x0

Table 10-738. Register Call Summary for Register RFBI_ONOFF_TIME

Remote Frame Buffer Interface

- RFBI Transaction Timing Diagrams: [0] [1] [2] [3] [4] [5]
- RFBI Timings: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
- RFBI Global Initialization: [21]
- RFBI Operational Modes Configuration: [22]
- RFBI Register Summary: [23]

Table 10-739. RFBI_CYCLE_TIME

Address Offset	0x0000 0068		
Physical Address	0x5800 2068	**Instance**	RFBI
Description	The control register configures the RFBI timings for the LCD 0, LCD 1, and LCD 2.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ACCESSTIME								WRENABLE	WWENABLE	RRENABLE	RWENABLE	CSPULSEWIDTH				RECYCLETIME				WECYCLETIME			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0
27:22	ACCESSTIME	Access time number of RFBI_ICLK cycles	RW	0x00
21	WRENABLE	Write-to-read pulse width enable (same CS)	RW	0
		0x0: CSPULSEWIDTH does not apply on write-to-read access.		
		0x1: CSPULSEWIDTH applies on write-to-read access.		
20	WWENABLE	Write-to-write pulse width enable (same CS)	RW	0
		0x0: CSPULSEWIDTH does not apply on write-to-write access.		
		0x1: CSPULSEWIDTH applies on write-to-write access.		

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Bits	Field Name	Description	Type	Reset
19	RRENABLE	Read-to-read pulse width enable (same CS) 0x0: CSPULSEWIDTH does not apply on read-to-read access. 0x1: CSPULSEWIDTH applies on read-to-read access.	RW	0
18	RWENABLE	Read-to-write pulse width enable (same CS): 0x0: CSPULSEWIDTH does not apply on read-to-write access. 0x1: CSPULSEWIDTH applies on read-to-write access.	RW	0
17:12	CSPULSEWIDTH	CS pulse width number of RFBI_ICLK cycles	RW	0x00
11:6	RECYCLETIME	RE cycle time number of RFBI_ICLK cycles	RW	0x00
5:0	WECYCLETIME	WE cycle time number of RFBI_ICLK cycles	RW	0x00

Table 10-740. Register Call Summary for Register RFBI_CYCLE_TIME

Remote Frame Buffer Interface

- RFBI Transaction Timing Diagrams: [0] [1] [2]
- RFBI Timings: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
- RFBI Global Initialization: [16]
- RFBI Operational Modes Configuration: [17]
- RFBI Register Summary: [18]

Table 10-741. RFBI_DATA_CYCLEi

Address Offset	0x0000 006C + (0x04 * i)	**Index**	i = 0 to 2
Physical Address	0x5800 206C + (0x04 * i)	**Instance**	RFBI
Description	The control register configures the RFBI data format for the i cycle (i = 1 for first cycle, i = 2 for second cycle, i = 3 for third cycle).		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
RESERVED	BITALIGNMENTPIXEL2	RESERVED	NBBITSPIXEL2	RESERVED	BITALIGNMENTPIXEL1	RESERVED	NBBITSPIXEL1

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0
27:24	BITALIGNMENTPIXEL2	Alignment of the bits from pixel 2 on the output interface	RW	0x0
23:21	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0
20:16	NBBITSPIXEL2	Number of bits from the pixel 2 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00
15:12	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0
11:8	BITALIGNMENTPIXEL1	Alignment of the bits from pixel 1 on the output interface	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0
4:0	NBBITSPIXEL1	Number of bits from the pixel 1 (value from 0 to 16 bits). The values from 17 to 31 are invalid.	RW	0x00

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Table 10-742. Register Call Summary for Register RFBI_DATA_CYCLEi

Remote Frame Buffer Interface

- RFBI Cycle Mode Selection: [0]
- RFBI Operational Modes Configuration: [1]
- RFBI Register Summary: [2]

Table 10-743. RFBI_VSYNC_WIDTH

Address Offset	0x0000 0090		
Physical Address	0x5800 2090	**Instance**	RFBI
Description	The register configures the RFBI VSYNC minimum pulse width.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MINVSYNCPULSEWIDTH															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0000
15:0	MINVSYNCPULSEWIDTH	Programmable minimum VSYNC pulse width. Minimum VSYNC pulse width from 0 to 65535. Number of RFBI_ICLK clock cycles to determine when VSYNC pulse occurs. The values 0 and 1 are invalid.	RW	0x0000

Table 10-744. Register Call Summary for Register RFBI_VSYNC_WIDTH

Remote Frame Buffer Interface

- RFBI Description of the Tearing Effect Pulse Signal: [0]
- RFBI External Trigger Mode: [1] [2]
- RFBI Global Initialization: [3]
- RFBI Operational Modes Configuration: [4]
- RFBI Register Summary: [5]

Table 10-745. RFBI_HSYNC_WIDTH

Address Offset	0x0000 0094		
Physical Address	0x5800 2094	**Instance**	RFBI
Description	The register configures the RFBI HSYNC minimum pulse width.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MINHSYNCPULSEWIDTH															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Reads return 0.	RO	0x0000
15:0	MINHSYNCPULSEWIDTH	Programmable minimum HSYNC pulse width. Minimum HSYNC pulse width from 0 to 65535. Number of RFBI_ICLK clock cycles to determine when HSYNC pulse occurs. The values 0 and 1 are invalid.	RW	0x0000

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Table 10-746. Register Call Summary for Register RFBI_HSYNC_WIDTH

Remote Frame Buffer Interface

- RFBI Description of the Tearing Effect Pulse Signal: [0]
- RFBI External Trigger Mode: [1] [2]
- RFBI Global Initialization: [3]
- RFBI Operational Modes Configuration: [4]
- RFBI Register Summary: [5]

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3D Accelerator GPU Subsystem

This chapter is a basic overview and describes the integration of the 3D graphics processing unit (GPU) subsystem in the device.

NOTE: The GPU subsystem is an instantiation by Texas Instruments of the POWERVR™ SGX544 core from Imagination Technologies Ltd.

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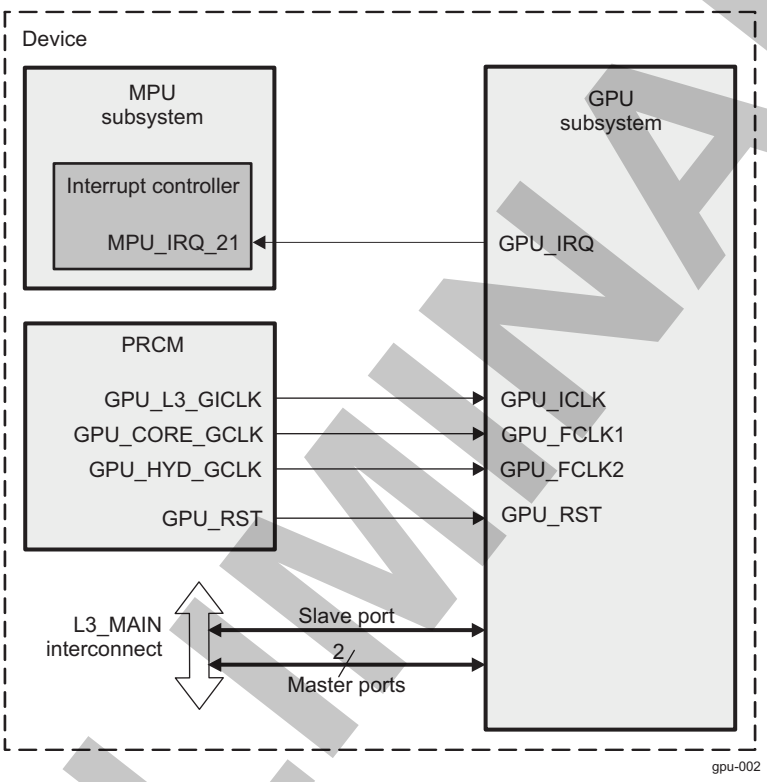
11.1 GPU Overview

The 3D graphics processing unit (GPU) accelerates 2-dimensional (2D) and 3-dimensional (3D) graphics and compute applications. It is based on the POWERVR® SGX544-MP2 core from Imagination Technologies. The SGX544-MP2 core is a multicore evolution of the POWERVR SGX544 GPU.

The multicore GPU splits geometry and pixel rendering among the cores to improve performance proportional to the number of cores.

Figure 11-1 shows the GPU subsystem.

Figure 11-1. GPU Overview



11.1.1 GPU Features Overview

- API support for industry standards:
  - OGL-ES 1.1 and 2.0
  - OpenVG™ 1.1
  - OpenCL™-EP 1.1
  - Direct3D™ Feature Level 9.3
- Multicore GPU architecture:
  - 2 × SGX544 core
  - Shared system level cache of 128 KiB
- Tile-based deferred rendering architecture:
  - Reduces external bandwidth to SDRAM
- Universal Scalable Shader Engine (USSE™):
  - Multithreaded engine incorporating vertex and pixel shader functionality
  - Automatic load balancing of vertex and pixel processing tasks
- Present and texture load accelerator (PTLA):
  - Enables to move, rotate, twiddle, and scale texture surfaces

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  - Supports RGB, ARGB, YUV4:2:2, and YUV4:2:0 surface formats
  - Supports bilinear upscale
  - Supports source color key
- Fully virtualized memory addressing for operating system (OS) in a unified memory architecture:
  - Memory management unit (MMU)
  - Up to 4-GiB virtual address space

11.1.2 Graphics Feature Overview

- Texture support:
  - Cube map
  - Projected textures
  - Non-square textures
- Texture formats:
  - RGBA 8888, 565, 1555, and 1565
  - Monochromatic 8, 16, 16f, 32f, and 32int
  - Dual channel, 8:8, 16:16, and 16f:16f
  - Compressed textures:
    - PVRTC-i 2 bpp
    - PVRTC-i 4 bpp
    - PVRTC-ii 2 bpp
    - PVRTC-ii 4 bpp
    - ETC1
    - DXT 1-5 and BC 4-5
  - Programmable support for YUV formats:
    - Programmable matrix in hardware, coefficients on 12 bits
    - YUV4:2;2, YUV4:2:0, two planes (NV12 or NV21); YUV4:2:0, three planes
- Resolution support:
  - Frame buffer maximum = 4096 × 4096
  - Texture maximum size = 4096 × 4096
- Texture filtering:
  - Bilinear, trilinear
  - Independent minimum and mag control
- Anti-aliasing:
  - 4× multisampling
  - Programmable sample positions

NOTE: TI provides the DXT1-5 and BC4-5 texture compression technology for use only with a Microsoft Windows operating system.

A separate license is required for the use of this technology (also referred to as S3 texture compression technology) with any other operating system.

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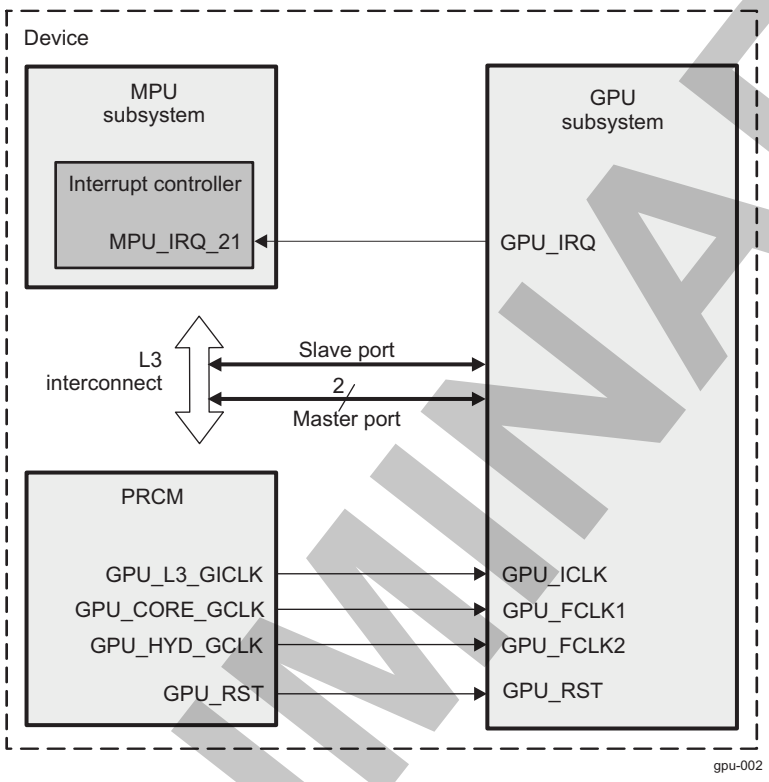
11.2 GPU Integration

This section describes the integration of the module in the device, including information about clocks, resets, and hardware requests.

Figure 11-2 shows the GPU integration.

Figure 11-2. GPU Integration



The GPU subsystem is connected to the level 3 (L3) interconnect by two 128-bit master and a 64-bit slave interfaces.

Table 11-1 through Table 11-3 summarize the integration of the module in the device.

Table 11-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
GPU	PD_GPU	L3_MAIN

Table 11-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
GPU	GPU_ICLK	GPU_L3_GICLK	PRCM	GPU interface clock
GPU	GPU_FCLK1	GPU_CORE_GCLK	PRCM	GPU functional clock
GPU	GPU_FCLK2	GPU_HYD_GCLK	PRCM	GPU functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
GPU	GPU_RST	GPU_RST	PRCM	GPU reset signal

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Table 11-3. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
GPU	GPU_IRQ	MPU_IRQ_21	Cortex™-A15 INTC	GPU interrupt request to the microprocessor unit (MPU) interrupt controller (INTC)

NOTE: For a description of the interrupt source, see Section 11.3.5, *GPU Interrupt Requests*.

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11.3 GPU Functional Description

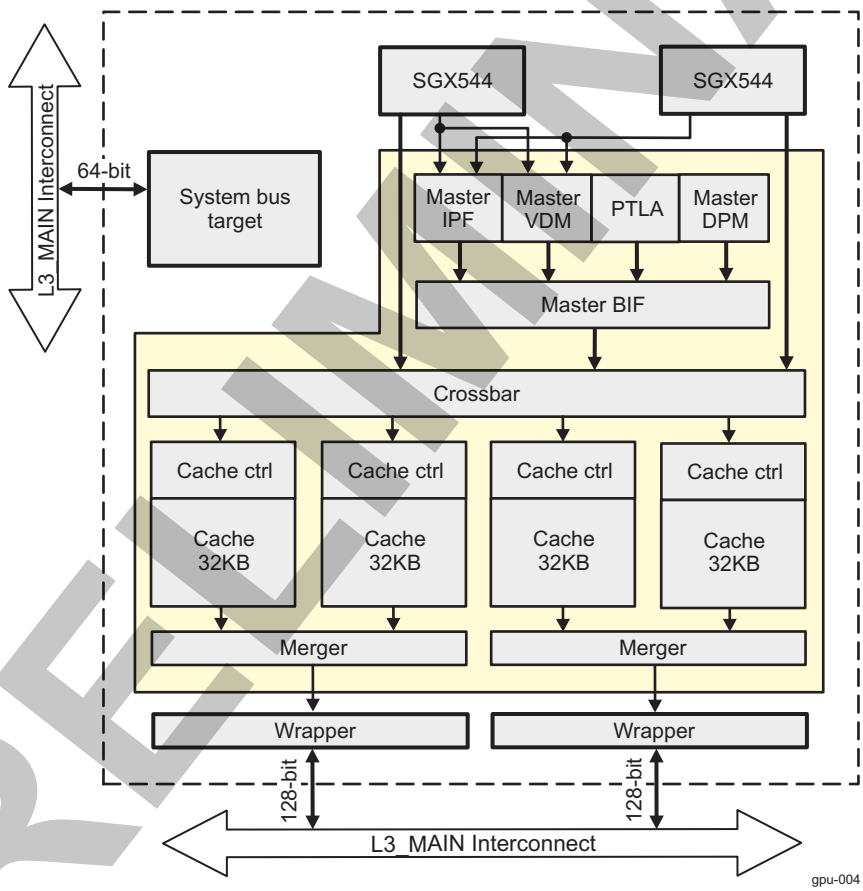
11.3.1 GPU Block Diagram

The GPU subsystem is based on the POWERVR SGX544-MP2 core. Multicore GPU can split geometry and pixel rendering among the cores to improve performance proportional to the number of cores. The graphics software engineer programming the OMAP5430 GPU does not have to deal with the multiple cores, this is done by the graphics drivers. The multiple cores are completely hidden behind the standard high-level graphics APIs that are supported by the graphics core. The GPU architecture comprises the following elements:

- SGX544 cores
- PTLA
- Cross bar
- System-level cache (SLC)

Figure 11-3 shows the GPU top-level block diagram.

Figure 11-3. GPU Block Diagram



The SGX544-MP2 has 2 × SGX544 cores. Graphics rendering is automatically load-balanced between the 2 × SGX544 cores. It is possible to disable one or two of the cores if required. The glue logic is used to enable the multicore architecture. The crossbar enables any SGX544 core to access the SLC. The SLC is a 128-KiB unified multibanked cache with four banks of 32 KiB. The cache line size is 64 bytes. The SGX544 core accesses are interleaved in the different banks.

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11.3.2 GPU Clock Configuration

The GPU subsystem operates from three clocks: an interface clock (GPU_ICLK) and two functional clocks (GPU_FCLK1 and GPU_FCLK2). The power, reset, and clock management (PRCM) module generates and distributes the clocks inside the device.

- The GPU_ICLK manages the data transfer on the L3 master and slave ports.

  The GPU_ICLK frequency is selected based on the L3 interconnect clock frequency of the whole device. For more information about the interface clock, see Section 3.6.12, *CD_GPU Clock Domains*.

  When no longer required by the GPU subsystem, GPU_ICLK can be disabled by software at the PRCM level. For more information, see PD_GPU Description, in *Power, Reset, and Clock Management*.

  NOTE: GPU_ICLK is cut only if the GPU is ready to go into IDLE state.

- GPU_FCLK1 and GPU_FCLK2 are the functional clocks and are used inside the GPU subsystem to generate clock signals to multiple GPU clock domains.

  Using the clock source selection and the digital phase-locked loop (DPLL) settings, GPU_FCLK1 and GPU_FCLK2 frequencies can be adjusted.

  The GPU_FCLK1 and GPU_FCLK2 clocks are provided by the peripheral DPLL and the core DPLL, as described in CD_GPU Clock Domain, in *Power, Reset, and Clock Management*. Selection is made at the PRCM level.

  When no longer needed by the GPU subsystem, GPU_FCLK1 and GPU_FCLK2 can be cut by software at the PRCM level if the module is ready to enter IDLE state. For more information, see PD_GPU Description, in *Power, Reset, and Clock Management*.

11.3.3 GPU Software Reset

The GPU subsystem has its own reset domain. Global reset of the GPU is performed by activating the GPU_RST signal in the GPU_RST domain.

NOTE: The APIs delivered with the GPU provide a software reset functionally equivalent to a hardware reset.

11.3.4 GPU Power Management

The GPU subsystem has its own power domain (GPU power domain). For additional information about the GPU power domain, see PD_GPU Description, in *Power, Reset, and Clock Management*.

NOTE: The GPU handles automatic clock gating performed on the multiple internal module clock domains.

In addition, software-controlled clock gating is managed inside the GPU and handled by the related API delivered with the module.

11.3.5 GPU Interrupt Requests

The GPU subsystem can generate one interrupt signal to the MPU INTC mapped to GPU_IRQ.

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11.4 GPU Register Manual

CAUTION

All GPU registers are limited to 32-bit data accesses; 8- and 16-bit accesses are not allowed because they can corrupt register content.

11.4.1 GPU Instance Summary

Table 11-4. GPU Instance Summary

Module Name	Base Address	Size
GPU_WRAPPER	0x5600 FE00	512 bytes

The GPU domain's base address is at 0x5600 0000. GPU address space is 32MiB wide.

11.4.2 GPU Registers

11.4.2.1 GPU_WRAPPER Register Summary

Table 11-5. GPU_WRAPPER Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
REVISION	R	32	0x0000 0000	0x5600 FE00
HWINFO	R	32	0x0000 0004	0x5600 FE04
SYSCONFIG	RW	32	0x0000 0010	0x5600 FE10
IRQSTATUS_RAW_0	RW	32	0x0000 0024	0x5600 FE24
IRQSTATUS_RAW_1	RW	32	0x0000 0028	0x5600 FE28
IRQSTATUS_RAW_2	RW	32	0x0000 002C	0x5600 FE2C
IRQSTATUS_0	RW	32	0x0000 0030	0x5600 FE30
IRQSTATUS_1	RW	32	0x0000 0034	0x5600 FE34
IRQSTATUS_2	RW	32	0x0000 0038	0x5600 FE38
IRQENABLE_SET_0	RW	32	0x0000 003C	0x5600 FE3C
IRQENABLE_SET_1	RW	32	0x0000 0040	0x5600 FE40
IRQENABLE_SET_2	RW	32	0x0000 0044	0x5600 FE44
IRQENABLE_CLR_0	RW	32	0x0000 0048	0x5600 FE48
IRQENABLE_CLR_1	RW	32	0x0000 004C	0x5600 FE4C
IRQENABLE_CLR_2	RW	32	0x0000 0050	0x5600 FE50
PAGE_CONFIG	RW	32	0x0000 0100	0x5600 FF00
INTERRUPT_EVENT	RW	32	0x0000 0104	0x5600 FF04
DEBUG_CONFIG	RW	32	0x0000 0108	0x5600 FF08
DEBUG_STATUS_0	R	32	0x0000 010C	0x5600 FF0C
DEBUG_STATUS_1	R	32	0x0000 0110	0x5600 FF10

11.4.2.2 GPU_WRAPPER Register Description

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Table 11-6. REVISION

Address Offset	0x0000 0000		
Physical Address	0x5600 FE00	**Instance**	GPU_WRAPPER
Description	Revision register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISIONID																															

Bits	Field Name	Description	Type	Reset
31:0	REVISIONID	Revision value	R	See (1)

(1) TI internal data

Table 11-7. Register Call Summary for Register REVISION

GPU Register Manual

- GPU Register Summary: [0]

Table 11-8. HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5600 FE04	**Instance**	GPU_WRAPPER
Description	Hardware implementation information		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MEM_BUS_WIDTH	SYS_BUS_WIDTH	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	MEM_BUS_WIDTH	Memory bus width Read 0x0: 64 bits Read 0x1: 128 bits	R	1
1:0	SYS_BUS_WIDTH	System bus width Read 0x0: 32 bits Read 0x1: 64 bits Read 0x2: 128 bits Read 0x3: Reserved	R	0x1

Table 11-9. Register Call Summary for Register HWINFO

GPU Register Manual

- GPU Register Summary: [0]

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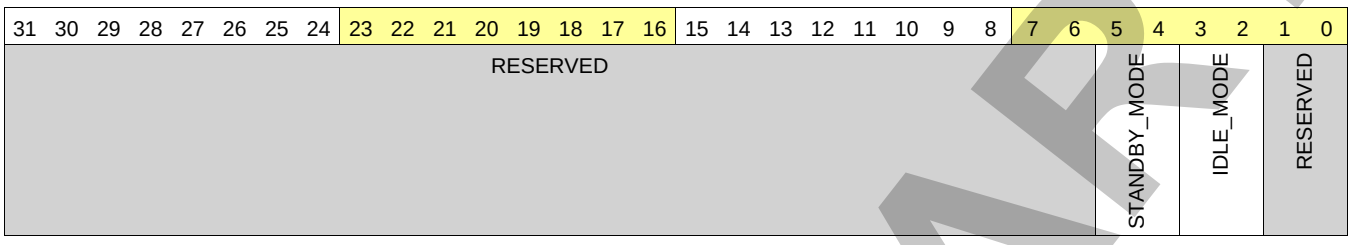
Table 11-10. SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5600 FE10	**Instance**	GPU_WRAPPER
Description	System configuration register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x000 0000
5:4	STANDBY_MODE	Clock standby mode: 0x0: Force-standby 0x1: No-standby 0x2: Smart-standby 0x3: Reserved	RW	0x2
3:2	IDLE_MODE	Clock idle mode: 0x0: Force-standby 0x1: No-standby 0x2: Smart-standby 0x3: Reserved	RW	0x2
1:0	RESERVED		R	0x0

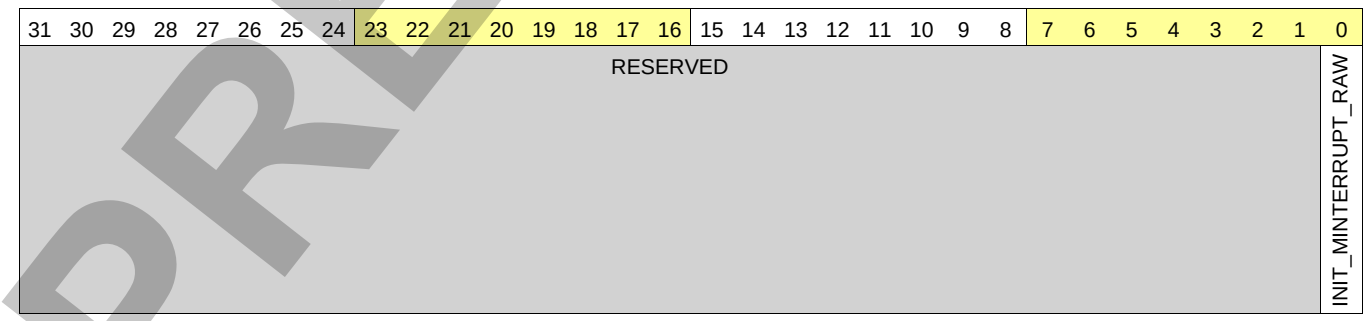
Table 11-11. Register Call Summary for Register SYSCONFIG

GPU Register Manual

- GPU Register Summary: [0]

Table 11-12. IRQSTATUS_RAW_0

Address Offset	0x0000 0024		
Physical Address	0x5600 FE24	**Instance**	GPU_WRAPPER
Description	Raw IRQ 0 status		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	INIT_MINTERRUPT_RAW	Interrupt 0 raw event: Write 0x0: No action Write 0x1: Set event (used for debug) Read 0x0: No event pending Read 0x1: Event pending	RW	0

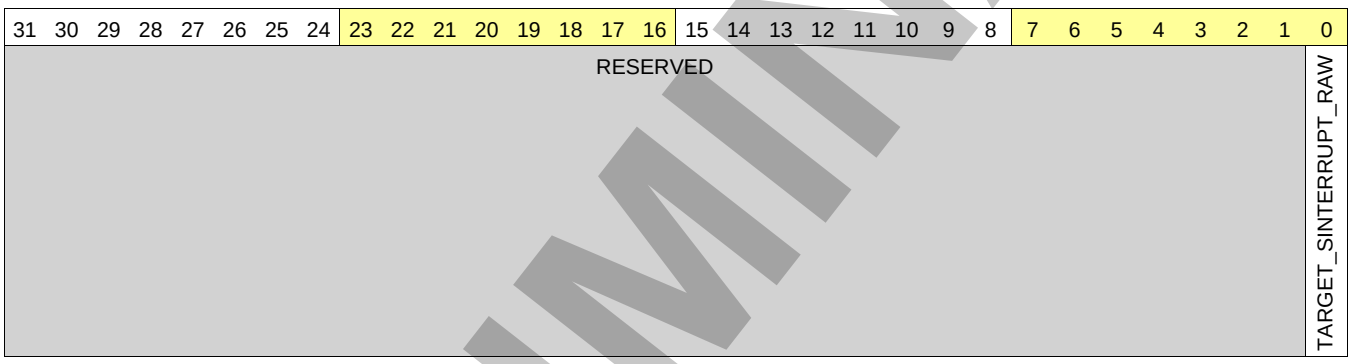
Table 11-13. Register Call Summary for Register IRQSTATUS_RAW_0

GPU Register Manual

- GPU Register Summary: [0]

Table 11-14. IRQSTATUS_RAW_1

Address Offset	0x0000 0028		
Physical Address	0x5600 FE28	**Instance**	GPU_WRAPPER
Description	Raw IRQ 1 status. Slave port interrupt.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	TARGET_SINTERRUPT_RAW	Interrupt 1 raw event: Write 0x0: No action Write 0x1: Set event (used for debug) Read 0x0: No event pending Read 0x1: Event pending	RW	0

Table 11-15. Register Call Summary for Register IRQSTATUS_RAW_1

GPU Register Manual

- GPU Register Summary: [0]

Table 11-16. IRQSTATUS_RAW_2

Address Offset	0x0000 002C		
Physical Address	0x5600 FE2C	**Instance**	GPU_WRAPPER
Description	Raw IRQ 2 status. Core interrupt.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															THALIA_IRQ_RAW

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	THALIA_IRQ_RAW	Interrupt 0 raw event: Write 0x0: No action Write 0x1: Set event (used for debug) Read 0x0: No event pending Read 0x1: Event pending	RW	0

Table 11-17. Register Call Summary for Register IRQSTATUS_RAW_2

GPU Register Manual
- GPU Register Summary: [0]

Table 11-18. IRQSTATUS_0

Address Offset	0x0000 0030		
Physical Address	0x5600 FE30	**Instance**	GPU_WRAPPER
Description	Interrupt 0 status event. Master port interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															INIT_MINTERRUPT_STATUS

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	INIT_MINTERRUPT_STATUS	Interrupt 0 raw event: Write 0x0: No action Write 0x1: Clear event Read 0x0: No event pending Read 0x1: Event pending and interrupt enabled	RW	0

Table 11-19. Register Call Summary for Register IRQSTATUS_0

GPU Register Manual
- GPU Register Summary: [0]

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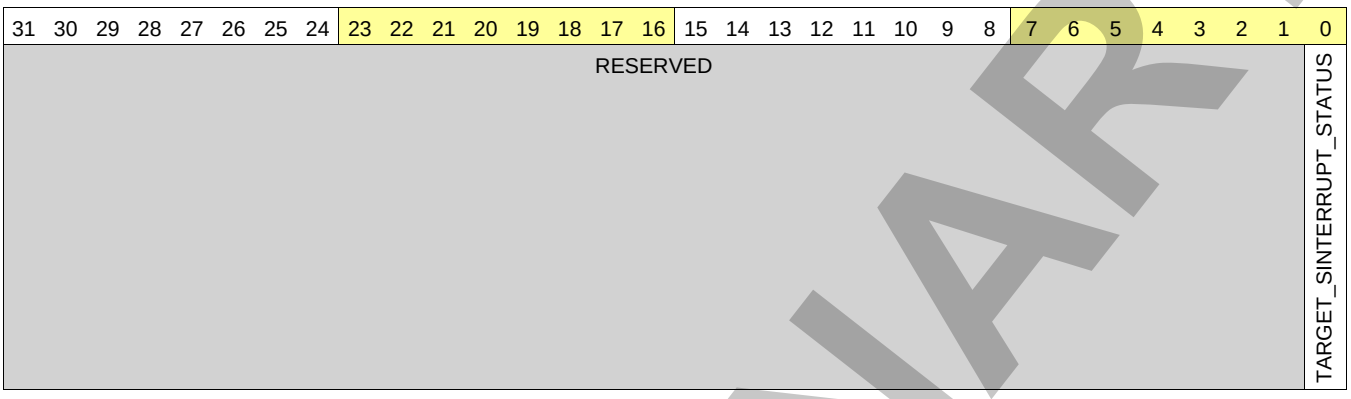
Table 11-20. IRQSTATUS_1

Address Offset	0x0000 0034		
Physical Address	0x5600 FE34	**Instance**	GPU_WRAPPER
Description	Interrupt 1 - slave port status event		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	TARGET_SINTERRUPT_STATUS	Interrupt 0 raw event: Write 0x0: No action Write 0x1: Clear event Read 0x0: No event pending Read 0x1: Event pending and interrupt enabled	RW	0

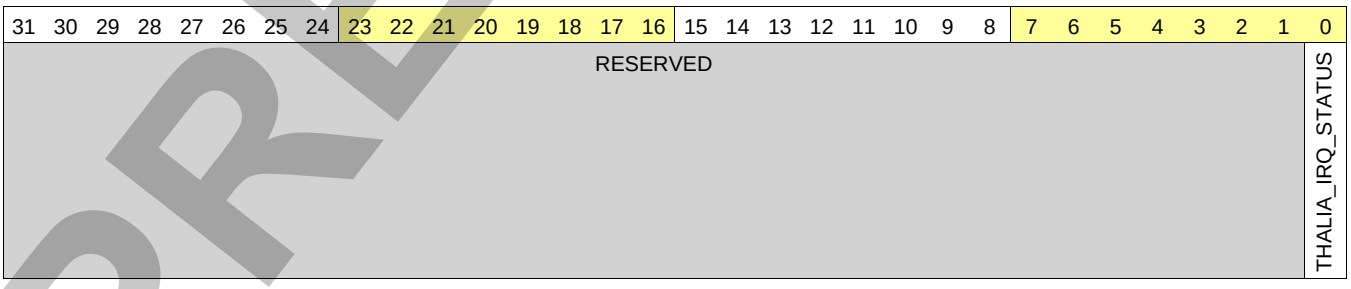
Table 11-21. Register Call Summary for Register IRQSTATUS_1

GPU Register Manual

- GPU Register Summary: [0]

Table 11-22. IRQSTATUS_2

Address Offset	0x0000 0038		
Physical Address	0x5600 FE38	**Instance**	GPU_WRAPPER
Description	Interrupt 2 - Core status event		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	THALIA_IRQ_STATUS	Interrupt 0 raw event: Write 0x0: No action Write 0x1: Clear event Read 0x0: No event pending Read 0x1: Event pending and interrupt enabled	RW	0

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Table 11-23. Register Call Summary for Register IRQSTATUS_2

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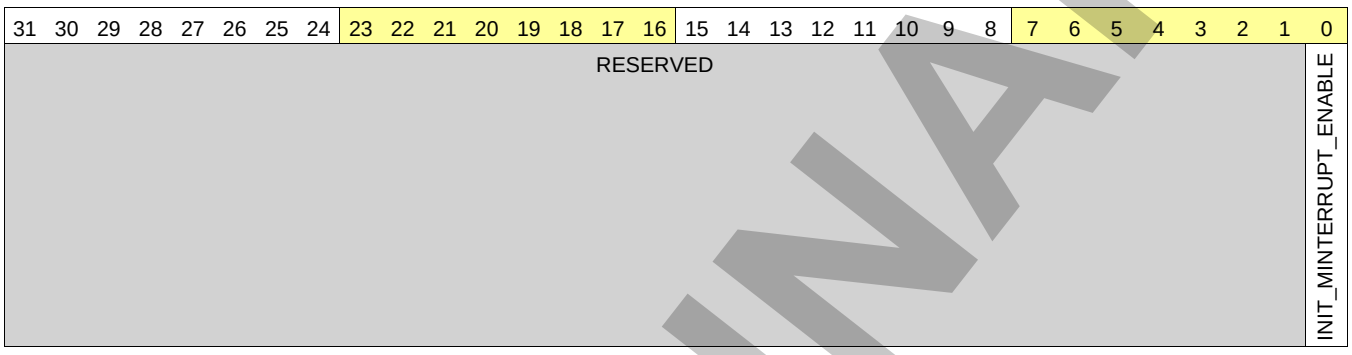
- GPU Register Summary: [0]

Table 11-24. IRQENABLE_SET_0

Address Offset	0x0000 003C		
Physical Address	0x5600 FE3C	**Instance**	GPU_WRAPPER
Description	Enable Interrupt 0 - Master port.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	INIT_MINTERRUPT_ENABLE	To enable interrupt: Write 0x0: No action Write 0x1: Enable interrupt Read 0x0: Interrupt is disabled Read 0x1: Interrupt is enabled	RW	0

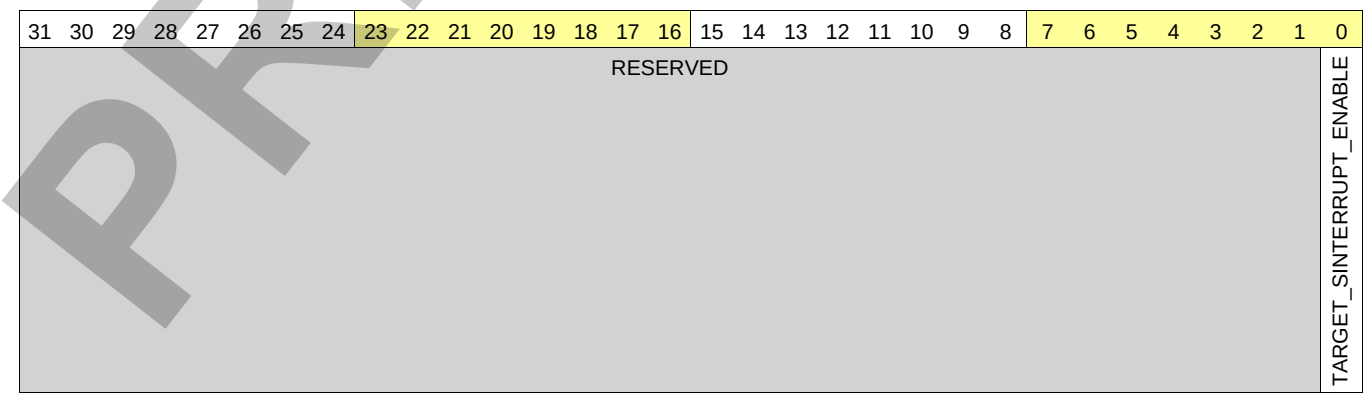
Table 11-25. Register Call Summary for Register IRQENABLE_SET_0

GPU Register Manual

- GPU Register Summary: [0]

Table 11-26. IRQENABLE_SET_1

Address Offset	0x0000 0040		
Physical Address	0x5600 FE40	**Instance**	GPU_WRAPPER
Description	Enable Interrupt 1. Core interrupt.		
Type	RW		



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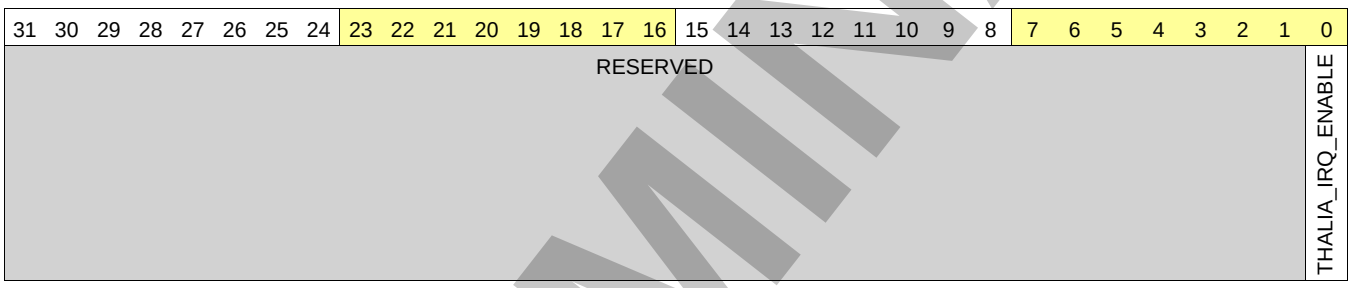
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	TARGET_SINTERRUPT_ENABLE	To enable interrupt: Write 0x0: No action Write 0x1: Enable interrupt Read 0x0: Interrupt is disabled Read 0x1: Interrupt is enabled	RW	0

Table 11-27. Register Call Summary for Register IRQENABLE_SET_1

GPU Register Manual
- GPU Register Summary: [0]

Table 11-28. IRQENABLE_SET_2

Address Offset	0x0000 0044		
Physical Address	0x5600 FE44	**Instance**	GPU_WRAPPER
Description	Enable Interrupt 2. Core interrupt.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	THALIA_IRQ_ENABLE	To enable interrupt: Write 0x0: No action Write 0x1: Enable interrupt Read 0x0: Interrupt is disabled Read 0x1: Interrupt is enabled	RW	0

Table 11-29. Register Call Summary for Register IRQENABLE_SET_2

GPU Register Manual
- GPU Register Summary: [0]

Table 11-30. IRQENABLE_CLR_0

Address Offset	0x0000 0048		
Physical Address	0x5600 FE48	**Instance**	GPU_WRAPPER
Description	Disable Interrupt 0 - Master port.		
Type	RW		

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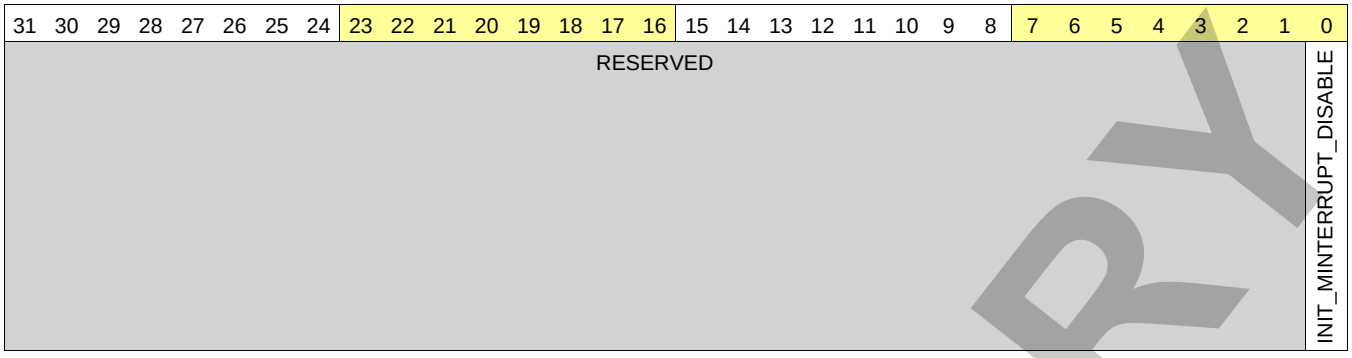


Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	INIT_MINTERRUPT_DISABLE	To disable interrupt: Write 0x0: No action Write 0x1: Disable interrupt Read 0x0: Interrupt is disabled Read 0x1: Interrupt is enabled	RW	0

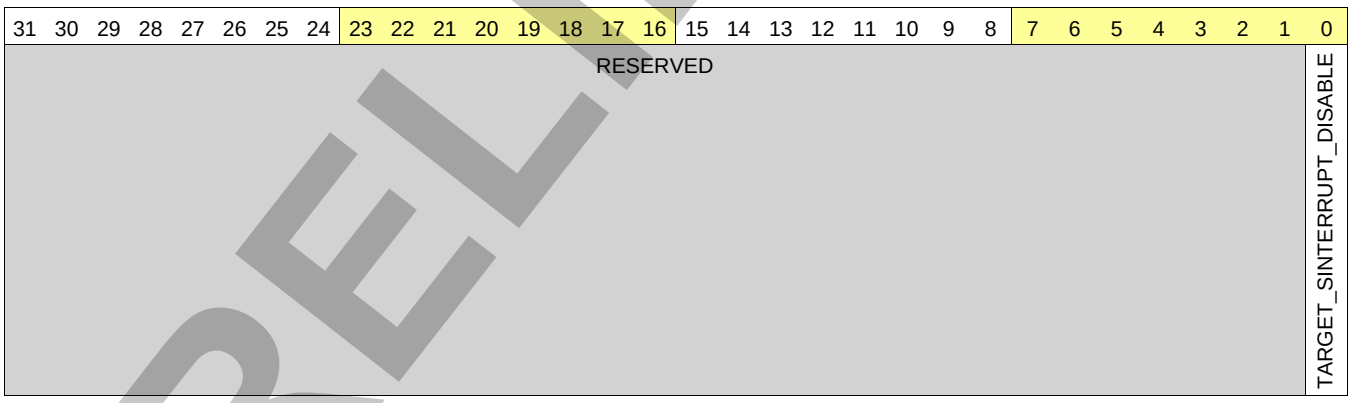
Table 11-31. Register Call Summary for Register IRQENABLE_CLR_0

GPU Register Manual

- GPU Register Summary: [0]

Table 11-32. IRQENABLE_CLR_1

Address Offset	0x0000 004C		
Physical Address	0x5600 FE4C	**Instance**	GPU_WRAPPER
Description	Disable Interrupt 2 - Core interrupt.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	TARGET_SINTERRUPT_DISABLE	To disable interrupt: Write 0x0: No action Write 0x1: Disable interrupt Read 0x0: Interrupt is disabled Read 0x1: Interrupt is enabled	RW	0

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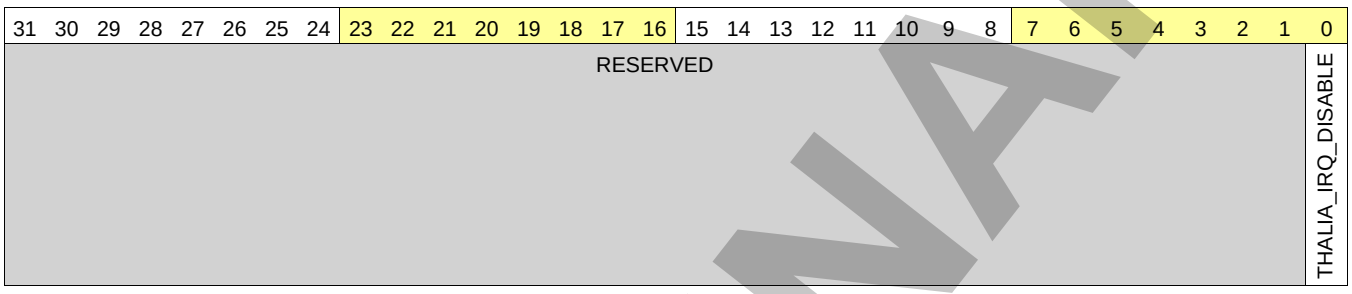
Table 11-33. Register Call Summary for Register IRQENABLE_CLR_1

GPU Register Manual

- GPU Register Summary: [0]

Table 11-34. IRQENABLE_CLR_2

Address Offset	0x0000 0050		
Physical Address	0x5600 FE50	**Instance**	GPU_WRAPPER
Description	Disable Interrupt 2 - Core interrupt.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	THALIA_IRQ_DISABLE	To disable interrupt: Write 0x0: No action Write 0x1: Disable interrupt Read 0x0: Interrupt is disabled Read 0x1: Interrupt is enabled	RW	0

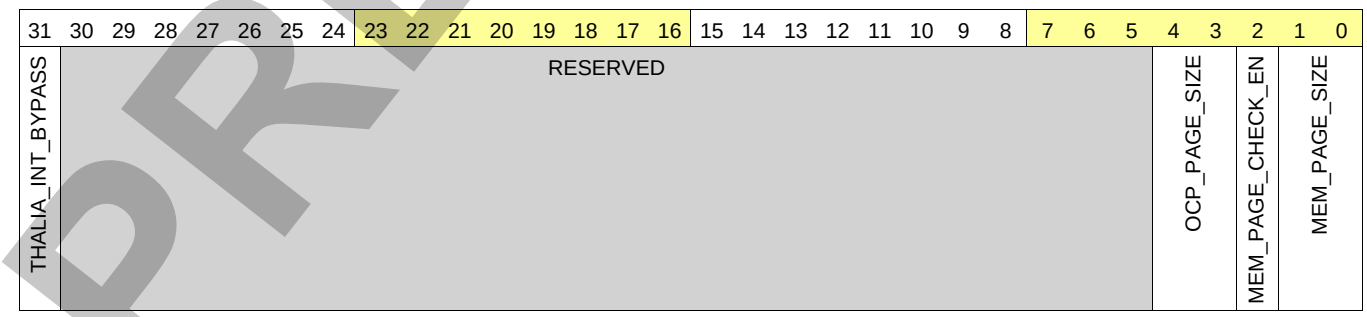
Table 11-35. Register Call Summary for Register IRQENABLE_CLR_2

GPU Register Manual

- GPU Register Summary: [0]

Table 11-36. PAGE_CONFIG

Address Offset	0x0000 0100		
Physical Address	0x5600 FF00	**Instance**	GPU_WRAPPER
Description	Configure memory pages.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31	THALIA_INT_BYPASS	Bypass OCP IPG interrupt logic 0x0: Do not bypass 0x1 Bypass core interrupt to I/O pin; that is, disregard the interrupt enable setting in the IPG register.	RW	0
30:5	RESERVED		R	0x000 0000
4:3	OCP_PAGE_SIZE	Defines the page size on OCP memory interface: 0x0: 4 KiB 0x1: 2 KiB 0x2: 1 KiB 0x3: 512B	RW	0x2
2	MEM_PAGE_CHECK_EN	To enable page boundary checking: 0x0: Disabled 0x1: Enabled	RW	1
1:0	MEM_PAGE_SIZE	Defines the page size on internal memory interface: 0x0: 4 KiB 0x1: 2 KiB 0x2: 1 KiB 0x3: 512B	RW	0x0

Table 11-37. Register Call Summary for Register PAGE_CONFIG

GPU Register Manual

- GPU Register Summary: [0]

Table 11-38. INTERRUPT_EVENT

Address Offset	0x0000 0104		
Physical Address	0x5600 FF04	**Instance**	GPU_WRAPPER
Description	Interrupt events		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													TARGET_INVALID_OCP_CMD	TARGET_CMD_FIFO_FULL	TARGET_RESP_FIFO_FULL	RESERVED		INT_MEM_REQ_FIFO_OVERRUN_1	INIT_READ_TAG_FIFO_OVERRUN_1	INIT_PAGE_CROSS_ERROR_1	INIT_RESP_ERROR_1	INIT_RESP_UNUSED_TAG_1	INIT_RESP_UNEXPECTED_1	RESERVED		INIT_MEM_REQ_FIFO_OVERRUN_0	INIT_READ_TAG_FIFO_OVERRUN_0	INIT_PAGE_CROSS_ERROR_0	INIT_RESP_ERROR_0	INIT_RESP_UNUSED_TAG_0	INIT_RESP_UNEXPECTED_0

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	TARGET_INVALID_OCP_CMD	Invalid command from OCP: Write 0x0: Clear the event Write 0x1: Set the event and interrupt if enabled (debug only) Read 0x0: No event pending Read 0x1: Event pending	RW	0

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Bits	Field Name	Description	Type	Reset
17	TARGET_CMD_FIFO_FULL	Command FIFO full: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
16	TARGET_RESP_FIFO_FULL	Response FIFO full: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
15:14	RESERVED		R	0x0
13	INT_MEM_REQ_FIFO_OVERRUN_1	Memory request FIFO overrun: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
12	INIT_READ_TAG_FIFO_OVERRUN_1	Read tag FIFO overrun: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
11	INIT_PAGE_CROSS_ERROR_1	Memory page had been crossed during a burst: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
10	INIT_RESP_ERROR_1	Receiving error response: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
9	INIT_RESP_UNUSED_TAG_1	Receiving response on an unused OCP TAG: Write 0x0: Clear the event Write 0x1: Set the event and interrupt if enabled (debug only) Read 0x0: No event pending Read 0x1: Event pending	RW	0
8	INIT_RESP_UNEXPECTED_1	Receiving response when not expected: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
7:6	RESERVED		R	0x0
5	INIT_MEM_REQ_FIFO_OVERRUN_0	Memory request FIFO overrun; Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
4	INIT_READ_TAG_FIFO_OVERRUN_0	Read tag FIFO overrun: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0

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Bits	Field Name	Description	Type	Reset
3	INIT_PAGE_CROSS_ERROR_0	Memory page had been crossed during a burst. Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
2	INIT_RESP_ERROR_0	Receiving error response: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
1	INIT_RESP_UNUSED_TAG_0	Receiving response on an unused OCP TAG: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0
0	INIT_RESP_UNEXPECTED_0	Receiving response when not expected: Write 0x0: Clear the event. Write 0x1: Set the event and interrupt if enabled (debug only). Read 0x0: No event pending Read 0x1: Event pending	RW	0

Table 11-39. Register Call Summary for Register INTERRUPT_EVENT

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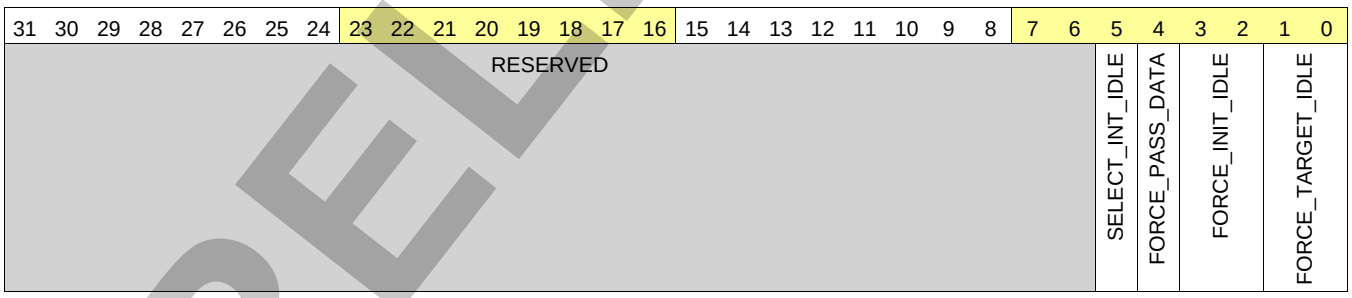
- GPU Register Summary: [0]

Table 11-40. DEBUG_CONFIG

Address Offset	0x0000 0108		
Physical Address	0x5600 FF08	**Instance**	GPU_WRAPPER
Description	Configuration of debug modes		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x000 0000
5	SELECT_INT_IDLE	To select which idle the disconnect protocol should act on: 0x0: Whole SGX idle 0x1: OCP initiator idle	RW	0
4	FORCE_PASS_DATA	Forces the initiator to pass data independent of disconnect protocol: 0x0: Do not force, normal operation 0x1: Never fence request to OCP	RW	0

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Bits	Field Name	Description	Type	Reset
3:2	FORCE_INIT_IDLE	Forces initiator idle: 0x0, 0x3: Do not force, normal operation 0x1: Always idle 0x2: Never idle	RW	0x0
1:0	FORCE_TARGET_IDLE	Forces target idle: 0x0, 0x3: Do not force, normal operation 0x1: Always idle 0x2: Never idle	RW	0x0

Table 11-41. Register Call Summary for Register DEBUG_CONFIG

GPU Register Manual

- GPU Register Summary: [0]

Table 11-42. DEBUG_STATUS_0

Address Offset	0x0000 010C		
Physical Address	0x5600 FF0C	**Instance**	GPU_WRAPPER
Description	Port0 debug status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_DEBUG_STATE		CMD_RESP_DEBUG_STATE		TARGET_IDLE		RESP_FIFO_FULL		CMD_FIFO_FULL		RESP_ERROR		WHICH_TARGET_REGISTER				TARGET_CMD_OUT				INIT_MSTANDBY		INIT_MWAIT		INIT_MDISCREQ		INIT_MDISCACK		INIT_SCONNECT_2		INIT_SCONNECT_1		INIT_SCONNECT_0		INIT_MCONNECT		TARGET_SIDLEACK		TARGET_SDISCACK		TARGET_SIDLEREQ		TARGET_SCONNECT		TARGET_MCONNECT	

Bits	Field Name	Description	Type	Reset
31	CMD_DEBUG_STATE	Target command state-machine: 0x0: IDLE 0x1: Accept command	R	0
30	CMD_RESP_DEBUG_STATE	Target response state-machine: 0x0: Send accept 0x1: Wait accept	R	0
29	TARGET_IDLE	Target idle	R	0
28	RESP_FIFO_FULL	Target response FIFO full	R	0
27	CMD_FIFO_FULL	Target command FIFO full	R	0
26	RESP_ERROR	Respond to OCP with error, which could be caused by either address misalignment or invalid byte enable.	R	0
25:21	WHICH_TARGET_REGISTER	Indicates which OCP target registers to read	R	0x00
20:18	TARGET_CMD_OUT	Command received from OCP: 0x0: CMD_WRSYS 0x1: CMD_RDSYS 0x2: CMD_WR_ERROR 0x3: CMD_RD_ERROR 0x4: CMD_CHK_WRADDR_PAGE (not used) 0x5: CMD_CHK_RDADDR_PAGE (not used) 0x6: CMD_TARGET_REG_WRITE 0x7: CMD_TARGET_REG_READ	R	0x0
17	INIT_MSTANDBY	Status of init_MStandby signal	R	0
16	INIT_MWAIT	Status of init_MWait signal	R	0

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Bits	Field Name	Description	Type	Reset
15	INIT_MDISCREQ	Request to disconnect from OCP interface	R	0
14:13	INIT_MDISCACK	Disconnect status of the OCP interface: 0x0: FUNCT 0x1: TRANS 0x2: Reserved 0x3: IDLE	R	0x0
12	INIT_SCONNECT_2	Defines whether to wait in M_WAIT state for MConnect FSM: 0x0: Skip M_WAIT state 0x1: Wait in M_WAIT state	R	0
11	INIT_SCONNECT_1	Defines the busy-ness state of the slave: 0x0: Slave is drained 0x1: Slave is loaded	R	0
10	INIT_SCONNECT_0	Disconnect from slave: 0x0: Disconnect request from slave 0x1: Connect request from slave	R	0
9:8	INIT_MCONNECT	Initiator MConnect state: 0x0: M_OFF 0x1: M_WAIT 0x2: M_DISC 0x3: M_CON	R	0x0
7:6	TARGET_SIDLEACK	Acknowledge the SIdleAck state-machine: 0x0: FUNCT 0x1: SLEEP TRANS 0x2: Reserved 0x3: IDLE	R	0x0
5:4	TARGET_SDISCACK	Acknowledge the SDiscAck state-machine: 0x0: FUNCT 0x1: TRANS 0x2: Reserved 0x3: IDLE	R	0x0
3	TARGET_SIDLEREQ	Request the target to go idle: 0 Do not go idle, or go active 1 Go idle	R	0
2	TARGET_SCONNECT	Target SConnect bit 0 state: 0x0: Disconnect interface 0x1: Connect OCP interface	R	0
1:0	TARGET_MCONNECT	Target MConnect state: 0x0: M_OFF 0x1: M_WAIT 0x2: M_DISC 0x3: M_CON	R	0x0

Table 11-43. Register Call Summary for Register DEBUG_STATUS_0

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- GPU Register Summary: [0]

Table 11-44. DEBUG_STATUS_1

Address Offset	0x0000 0110		
Physical Address	0x5600 FF10	**Instance**	GPU_WRAPPER
Description	Port1 debug status register		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_DEBUG_STATE	CMD_RESP_DEBUG_STATE	TARGET_IDLE	RESP_FIFO_FULL	CMD_FIFO_FULL	RESP_ERROR	WHICH_TARGET_REGISTER					TARGET_CMD_OUT			INIT_MSTANDBY	INIT_MWAIT	INIT_MDISCREQ	INIT_MDISCACK			INIT_SCONNECT_2	INIT_SCONNECT_1	INIT_SCONNECT_0	INIT_MCONNECT		TARGET_SIDLEACK		TARGET_SDISCACK		TARGET_SIDLEREQ	TARGET_SCONNECT	TARGET_MCONNECT	

Bits	Field Name	Description	Type	Reset
31	CMD_DEBUG_STATE	Target command state-machine: 0x0: IDLE 0x1: Accept command	R	0
30	CMD_RESP_DEBUG_STATE	Target response state-machine: 0x0: Send accept 0x1: Wait accept	R	0
29	TARGET_IDLE	Target idle	R	0
28	RESP_FIFO_FULL	Target response FIFO full	R	0
27	CMD_FIFO_FULL	Target command FIFO full	R	0
26	RESP_ERROR	Respond to OCP with error, which could be caused by either address misalignment or invalid byte enable.	R	0
25:21	WHICH_TARGET_REGISTER	Indicates which OCP target registers to read	R	0x00
20:18	TARGET_CMD_OUT	Command received from OCP: 0x0: CMD_WRSYS 0x1: CMD_RDSYS 0x2: CMD_WR_ERROR 0x3: CMD_RD_ERROR 0x4: CMD_CHK_WRADDR_PAGE (not used) 0x5: CMD_CHK_RDADDR_PAGE (not used) 0x6: CMD_TARGET_REG_WRITE 0x7: CMD_TARGET_REG_READ	R	0x0
17	INIT_MSTANDBY	Status of init_MStandby signal	R	0
16	INIT_MWAIT	Status of init_MWait signal	R	0
15	INIT_MDISCREQ	Request to disconnect from OCP interface	R	0
14:13	INIT_MDISCACK	Disconnect status of the OCP interface: 0x0: FUNCT 0x1: SLEEP TRANS 0x2: Reserved 0x3: IDLE	R	0x0
12	INIT_SCONNECT_2	Defines whether to wait in M_WAIT state for MConnect FSM: 0x0: Skip M_WAIT state. 0x1: Wait in M_WAIT state.	R	0
11	INIT_SCONNECT_1	Defines the busy-ness state of the slave: 0x0: Slave is drained. 0x1: Slave is loaded.	R	0
10	INIT_SCONNECT_0	Disconnect from slave: 0x0: Disconnect request from slave 0x1: Connect request from slave	R	0
9:8	INIT_MCONNECT	Initiator MConnect state: 0x0: M_OFF 0x1: M_WAIT 0x2: M_DISC 0x3: M_CON	R	0x0

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Bits	Field Name	Description	Type	Reset
7:6	TARGET_SIDLEACK	Acknowledge the SIdleAck state-machine: 0x0: FUNCT 0x1: SLEEP TRANS 0x2: Reserved 0x3: IDLE	R	0x0
5:4	TARGET_SDISCACK	Acknowledge the SDiscAck state-machine: 0x0: FUNCT 0x1: TRANS 0x2: Reserved 0x3: IDLE	R	0x0
3	TARGET_SIDLEREQ	Request the target to go idle: 0x0: Do not go idle, or go active 0x1: Go idle	R	0
2	TARGET_SCONNECT	Target SConnect bit 0 state: 0x0: Disconnect interface 0x1: Connect OCP interface	R	0
1:0	TARGET_MCONNECT	Target MConnect state: 0x0: M_OFF 0x1: M_WAIT 0x2: M_DISC 0x3: M_CON	R	0x0

Table 11-45. Register Call Summary for Register DEBUG_STATUS_1

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- GPU Register Summary: [0]

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2D Graphics Accelerator

This chapter describes the advanced bit blitter 2-dimensional (2D) graphics accelerator (BB2D) for the device.

NOTE: The BB2D subsystem is an instantiation by Texas Instruments of the GC320™ core from Vivante Corp.

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GC320 is a trademark or registered trademark of Vivante Corp.

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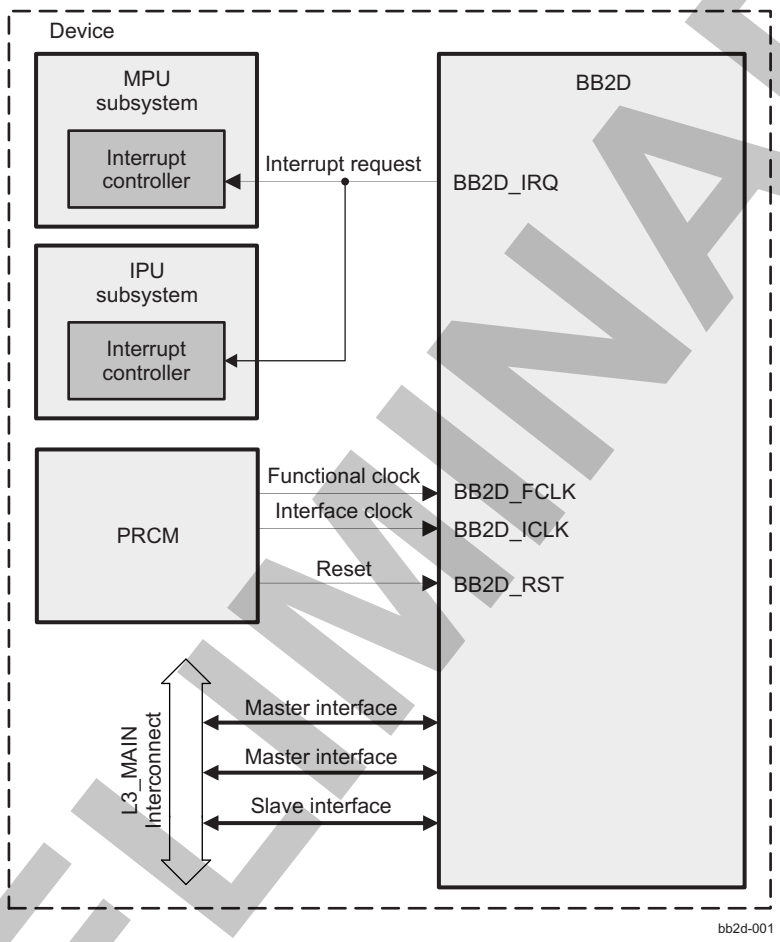
12.1 BB2D Overview

The 2D graphics accelerator subsystem accelerates 2D graphics applications. The 2D graphics accelerator subsystem is based on the GC320 2D GPU core from Vivante Corporation. The hardware acceleration is brought to numerous 2D applications, including on-screen display and touch screen user interfaces, graphical user interfaces (GUIs) and menu displays, flash animation, and gaming.

Figure 12-1 shows the BB2D subsystem.

Figure 12-1. BB2D Overview



12.1.1 BB2D Features Overview

- API support:
  - OpenWF™, DirectFB
  - GDI/DirectDraw™
  - Flash
- BB2D architecture:
  - BitBlt and StretchBlt
  - DirectFB hardware acceleration
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Clipping rectangle support
  - Alpha blending includes Java® 2 Porter-Duff compositing rules
  - 90-, 180-, 270-degree rotation on every primitive
  - YUV-to-RGB color space conversion

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  - Programmable display format conversion with 14 source and 7 destination formats
  - High-quality 9-tap, 32-phase filter for image and video scaling at 1080p
  - Monochrome expansion for text rendering
  - 32 K × 32 K coordinate system
- Hardware acceleration for DirectFB:
  - High-speed video scaler
  - ROP2/3/4
  - Rectangle filling and drawing
  - Line drawing
  - Simple blitting
  - Stretch blitting
  - Blending with alpha channel (per-pixel alpha)
  - Blending with alpha factor (alpha modulation)
  - Nine source and destination blending functions
  - Porter-Duff rules support
  - Premultiplied alpha support
  - Colorized blitting (color modulation)
  - Source color keying
  - Destination color keying

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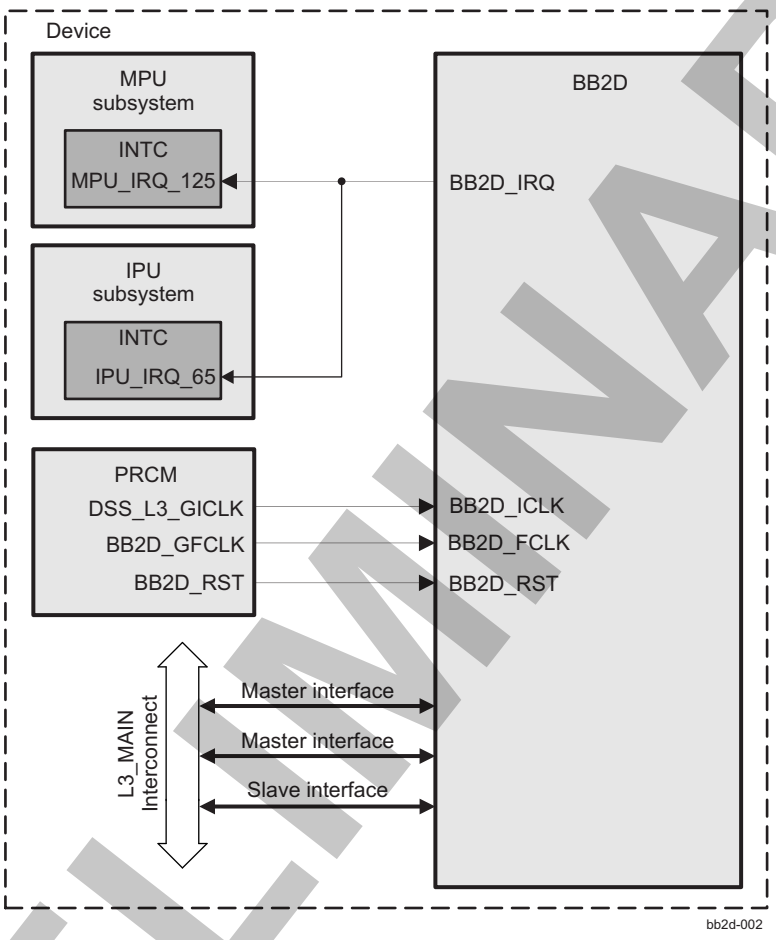
12.2 BB2D Integration

This section describes subsystem integration in the device, including information about clocks, resets, and hardware requests.

Figure 12-2 shows BB2D integration.

Figure 12-2. BB2D Integration



The BB2D subsystem is connected to the level 3 (L3_MAIN) interconnect by two 128-bit master interfaces and one 32-bit slave interface.

Table 12-1 through Table 12-3 summarize the integration of the subsystem in the device.

Table 12-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
BB2D	PD_DSS	L3_MAIN

Table 12-2. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
BB2D	BB2D_ICLK	DSS_L3_GICLK	PRCM	BB2D interfaces clock
	BB2D_FCLK	BB2D_GFCLK	PRCM	BB2D functional clock.
Resets				

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Table 12-2. Clocks and Resets (continued)

Module Instance	Destination Signal Name	Source Signal Name	Source	Description
BB2D	BB2D_RST	BB2D_RST	PRCM	BB2D reset signal

Table 12-3. Hardware Requests

	Interrupt Requests			
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
BB2D	BB2D_IRQ	MPU_IRQ_125	MPU INTC	BB2D interrupt request to the MPU interrupt controller (INTC)
	BB2D_IRQ	IPU_IRQ_65	IPU INTC	BB2D interrupt request to the IPU INTC

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12.3 BB2D Functional Description

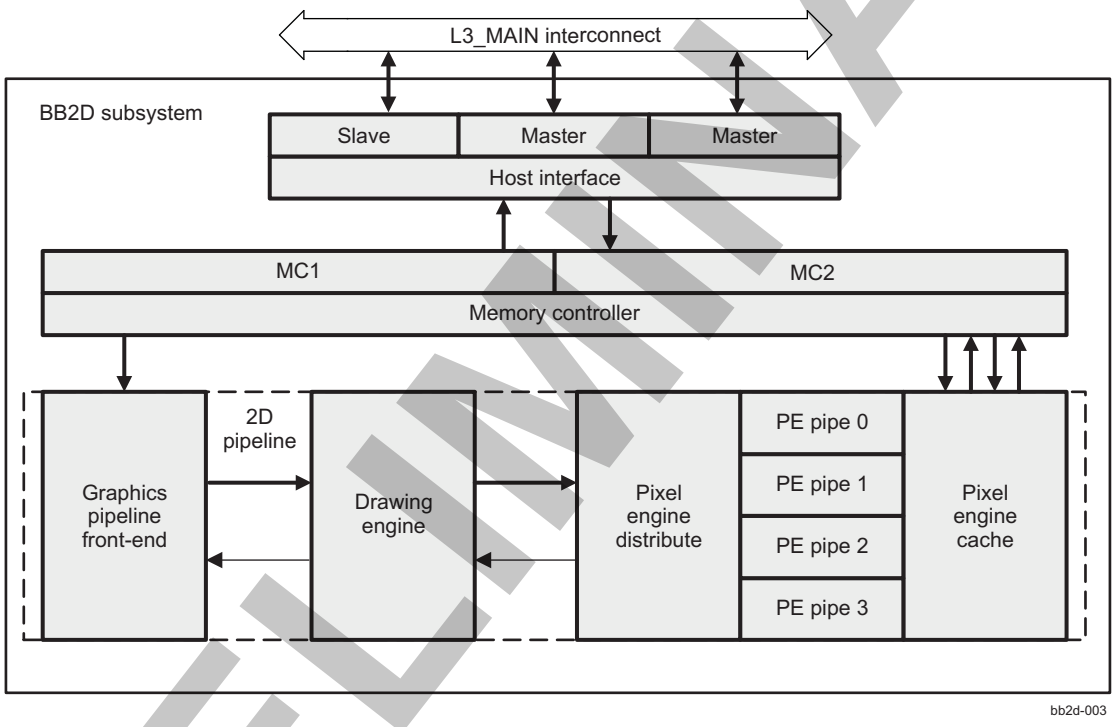
12.3.1 BB2D Block Diagram

The BB2D subsystem is based on the following main blocks:

- Host interface: Allows the BB2D core to communicate with external memory and the MPU through the L3_MAIN interconnect. In this block, data crosses clock domain boundaries.
- Memory controller: Internal memory unit that is the block-to-host interface for memory requests
- Graphics pipeline front-end: Inserts high-level primitives and commands into the graphics pipeline.
- 2D drawing and scaling engine: Draws 2D graphics primitives and rasterizes 2D images.
- Pixel engine: manipulates and filters pixels in rendered images. BB2D has four pixel pipes.

Figure 12-3 shows the BB2D top-level block diagram.

Figure 12-3. BB2D Block Diagram



12.3.2 BB2D Clock Configuration

The BB2D subsystem operates from two clocks: an interface clock (BB2D_ICLK) and functional clock (BB2D_FCLK). The power, reset, and clock management (PRCM) module generates and distributes the clocks inside the device.

- The BB2D_ICLK interface clock manages the data transfer on the L3_MAIN master and slave ports.

  The BB2D_ICLK frequency is selected based on the whole device L3 interconnect clock frequency. For more information on the interface clock, see *CD_DSS Clock Domain* in Section 3.6, *Clock Management Functional Description*.

  When BB2D_ICLK is no longer required by the BB2D subsystem, it can be disabled by software at the PRCM level.

  NOTE: BB2D_ICLK is cut only if the BB2D is ready to go into IDLE state.

- The BB2D_FCLK functional clock is used inside the BB2D subsystem to generate clock signals to multiple BB2D clock domains. The BB2D automatically gates clocks to domains, that are not currently in use.

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Using the clock source selection and the DPLL settings, the frequency of BB2D_FCLK can be adjusted.

When BB2D_FCLK is no longer needed by the BB2D subsystem, it can be cut by software at the PRCM level, if the module is ready to enter IDLE state.

12.3.3 BB2D Software Reset

The BB2D subsystem is part of the DSS reset domain. A global reset of the BB2D is performed by activating the BB2D_RST signal in the DSS_RST domain.

NOTE: The APIs delivered with the BB2D provide a software reset functionally equivalent to a hardware reset.

12.3.4 BB2D Power Management

The BB2D subsystem is part of the DSS power domain (PD_DSS). For additional information about PD_DSS, see *PD_DSS Description* in Section 3.1.2.3, *Power Management Functional Description*, in Chapter 3, *Power, Reset, and Clock Management*.

NOTE: The BB2D handles automatic clock gating performed on the multiple internal clock domains.

When 2D operations are complete, software may set the GCGPOUT0[0] GCHOLD bit to 1 to enter a low-power state. Setting GCHOLD to 1 moves the BB2D operational state into IDLE. Once in IDLE state, the system standby hardware signal (mstandby) is asserted.

12.3.5 BB2D Interrupt Requests

The BB2D subsystem can generate one interrupt signal to the MPU INTC and to the IPU INTC mapped to BB2D_IRQ.

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12.4 BB2D Register Manual

CAUTION

All BB2D registers are limited to 32-bit data accesses; 8- and 16-bit accesses are not allowed because they can corrupt register content.

12.4.1 BB2D Instance Summary

Table 12-4. BB2D Instance Summary

Module Name	Base Address	Size
BB2D	0x5900 0000	2 KB

12.4.2 BB2D Registers

12.4.2.1 BB2D Register Summary

Table 12-5. BB2D Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
AQHICLOCKCONTROL	RW	32	0x0000 0000	0x5900 0000
AQHIIDLE	R	32	0x0000 0004	0x5900 0004
AQAXICONFIG	RW	32	0x0000 0008	0x5900 0008
AQAXISTATUS	R	32	0x0000 000C	0x5900 000C
AQINTRACKNOWLEDGE	R	32	0x0000 0010	0x5900 0010
AQINTRENBL	RW	32	0x0000 0014	0x5900 0014
AQIDENT	R	32	0x0000 0018	0x5900 0018
GCFEATURES	R	32	0x0000 001C	0x5900 001C
GCCHIPID	R	32	0x0000 0020	0x5900 0020
GCCHIPREV	R	32	0x0000 0024	0x5900 0024
GCCHIPDATE	R	32	0x0000 0028	0x5900 0028
GCCHIPTIME	R	32	0x0000 002C	0x5900 002C
GCCHIPCUSTOMER	R	32	0x0000 0030	0x5900 0030
GCMINORFEATURES0	R	32	0x0000 0034	0x5900 0034
GCRESETMEMCOUNTERS	W	32	0x0000 003C	0x5900 003C
GCTOTALREADS	R	32	0x0000 0040	0x5900 0040
GCTOTALWRITES	R	32	0x0000 0044	0x5900 0044
GCCHIPSPECS	R	32	0x0000 0048	0x5900 0048
GCTOTALWRITEBURSTS	R	32	0x0000 004C	0x5900 004C
GCTOTALWRITEREQS	R	32	0x0000 0050	0x5900 0050
GCTOTALWRITELASTS	R	32	0x0000 0054	0x5900 0054
GCTOTALREADBURSTS	R	32	0x0000 0058	0x5900 0058
GCTOTALREADREQS	R	32	0x0000 005C	0x5900 005C
GCTOTALREADLASTS	R	32	0x0000 0060	0x5900 0060
GCGPOUT0	RW	32	0x0000 0064	0x5900 0064
RESERVED	RW	32	0x0000 0068	0x5900 0068
RESERVED	RW	32	0x0000 006C	0x5900 006C
GCAXICONTROL	RW	32	0x0000 0070	0x5900 0070
GCMINORFEATURES1	R	32	0x0000 0074	0x5900 0074

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Table 12-5. BB2D Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
GCTOTALCYCLES	RW	32	0x0000 0078	0x5900 0078
GCTOTALIDLECYCLES	RW	32	0x0000 007C	0x5900 007C
GCCHIPSPECS2	R	32	0x0000 0080	0x5900 0080
GCMINORFEATURES2	R	32	0x0000 0084	0x5900 0084
GCMODULEPOWERCONTROLS	RW	32	0x0000 0100	0x5900 0100
GCMODULEPOWERMODULECONTROL	RW	32	0x0000 0104	0x5900 0104
GCMODULEPOWERMODULESTATUS	R	32	0x0000 0108	0x5900 0108
GCREGMMUSTATUS	R	32	0x0000 0188	0x5900 0188
GCREGMMUCONTROL	W	32	0x0000 018C	0x5900 018C
GCREGMMUEXCEPTION0	RW	32	0x0000 0190	0x5900 0190
GCREGMMUEXCEPTION1	RW	32	0x0000 0194	0x5900 0194
GCREGMMUEXCEPTION2	RW	32	0x0000 0198	0x5900 0198
GCREGMMUEXCEPTION3	RW	32	0x0000 019C	0x5900 019C
AQMEMORYDEBUG	RW	32	0x0000 0414	0x5900 0414
AQREGISTERTIMINGCONTROL	RW	32	0x0000 042C	0x5900 042C
RESERVED	R	32	0x0000 0430	0x5900 0430
GCDISPLAYPRIORITY	RW	32	0x0000 0434	0x5900 0434
GCDBGCYCLECOUNTER	RW	32	0x0000 0438	0x5900 0438
GCOUTSTANDINGREADS0	R	32	0x0000 043C	0x5900 043C
GCOUTSTANDINGREADS1	R	32	0x0000 0440	0x5900 0440
GCOUTSTANDINGWRITES	R	32	0x0000 0444	0x5900 0444
GCDEBUGSIGNALSRA	R	32	0x0000 0448	0x5900 0448
GCDEBUGSIGNALSTX	R	32	0x0000 044C	0x5900 044C
GCDEBUGSIGNALSFE	R	32	0x0000 0450	0x5900 0450
GCDEBUGSIGNALSPE	R	32	0x0000 0454	0x5900 0454
GCDEBUGSIGNALSDE	R	32	0x0000 0458	0x5900 0458
GCDEBUGSIGNALSSH	R	32	0x0000 045C	0x5900 045C
GCDEBUGSIGNALSPA	R	32	0x0000 0460	0x5900 0460
GCDEBUGSIGNALSSE	R	32	0x0000 0464	0x5900 0464
GCDEBUGSIGNALSMC	R	32	0x0000 0468	0x5900 0468
GCDEBUGSIGNALSHI	R	32	0x0000 046C	0x5900 046C
GCDEBUGCONTROL0	RW	32	0x0000 0470	0x5900 0470
GCDEBUGCONTROL1	RW	32	0x0000 0474	0x5900 0474
GCDEBUGCONTROL2	RW	32	0x0000 0478	0x5900 0478
GCDEBUGCONTROL3	RW	32	0x0000 047C	0x5900 047C
GCBUSCONTROL	RW	32	0x0000 0480	0x5900 0480
GCREGENDIANNESS0	RW	32	0x0000 0484	0x5900 0484
GCREGENDIANNESS1	RW	32	0x0000 0488	0x5900 0488
GCREGENDIANNESS2	RW	32	0x0000 048C	0x5900 048C
GCREGDRAWPRIMITIVESTARTTIMESTAMP	R	32	0x0000 0490	0x5900 0490
GCREGDRAWPRIMITIVEENDTIMESTAMP	R	32	0x0000 0494	0x5900 0494
GCREGCONTROL0	RW	32	0x0000 0558	0x5900 0558
AQCMDBUFFERADDR	W	32	0x0000 0654	0x5900 0654
AQCMDBUFFERCTRL	W	32	0x0000 0658	0x5900 0658
AQFESTATUS	R	32	0x0000 065C	0x5900 065C
RESERVED	R	32	0x0000 0660	0x5900 0660

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Table 12-5. BB2D Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
AQFEDEBUGCURCMDADR	R	32	0x0000 0664	0x5900 0664
RESERVED	R	32	0x0000 0668	0x5900 0668
RESERVED	R	32	0x0000 066C	0x5900 066C

12.4.2.2 BB2D Register Description

Table 12-6. AQHICLOCKCONTROL

Address Offset	0x0000 0000		
Physical Address	0x5900 0000	**Instance**	BB2D
Description	Clock control register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MULTI_PIPE_USE_SINGLE_AXI				MULTI_PIPE_REG_SELECT				ISOLATE_GPU	IDLE_VG	IDLE2_D	IDLE3_D	RESERVED			SOFT_RESET	DISABLE_DEBUG_REGISTERS	DISABLE_RAM_CLOCK_GATING	FSCALE_CMD_LOAD	FSCALE_VAL							CLK2D_DIS	CLK3D_DIS

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	MULTI_PIPE_USE_SINGLE_AXI	Force all the transactions to go to one AXI	RW	0x0
23:20	MULTI_PIPE_REG_SELECT	Determines which HI/MC to use while reading registers	RW	0x0
19	ISOLATE_GPU	Isolate GPU bit	RW	0
18	IDLE_VG	VG pipe is idle	R	1
17	IDLE2_D	2D pipe is idle	R	1
16	IDLE3_D	3D pipe is idle	R	1
15:13	RESERVED		R	0x0
12	SOFT_RESET	Soft resets the subsystem	RW	0
11	DISABLE_DEBUG_REGISTERS	Disable debug registers. If this bit is 1, debug registers are clock gated	RW	0
10	DISABLE_RAM_CLOCK_GATING	Disables clock gating for RAMs	RW	0
9	FSCALE_CMD_LOAD		RW	0
8:2	FSCALE_VAL		RW	0x40
1	CLK2D_DIS	Disable 2D clock	RW	0
0	CLK3D_DIS	Disable 3D clock	RW	0

Table 12-7. Register Call Summary for Register AQHICLOCKCONTROL

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- BB2D Register Summary: [0]

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Table 12-8. AQHIIDLE

Address Offset	0x0000 0004		
Physical Address	0x5900 0004	**Instance**	BB2D
Description	Idle status register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AXI_LP	RESERVED																			IDLE_TS	IDLE_FP	IDLE_IM	IDLE_VG	IDLE_TX	IDLE_RA	IDLE_SE	IDLE_PA	IDLE_SH	IDLE_PE	IDLE_DE	IDLE_FE

Bits	Field Name	Description	Type	Reset
31	AXI_LP	AXI is in low power mode	R	0
30:12	RESERVED	Unused bits reserved for future expansion	R	0x7 FFFF
11	IDLE_TS	TS is idle	R	1
10	IDLE_FP	FP is idle	R	1
9	IDLE_IM	IM is idle	R	1
8	IDLE_VG	VG is idle	R	1
7	IDLE_TX	TX is idle	R	1
6	IDLE_RA	RA is idle	R	1
5	IDLE_SE	SE is idle	R	1
4	IDLE_PA	PA is idle	R	1
3	IDLE_SH	SH is idle	R	1
2	IDLE_PE	PE is idle	R	1
1	IDLE_DE	DE is idle	R	1
0	IDLE_FE	FE is idle	R	1

Table 12-9. Register Call Summary for Register AQHIIDLE

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- BB2D Register Summary: [0]

Table 12-10. AQAXICONFIG

Address Offset	0x0000 0008		
Physical Address	0x5900 0008	**Instance**	BB2D
Description	AXI config		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ARCACHE				AWCACHE				ARID				AWID			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	ARCACHE		RW	0x0
11:8	AWCACHE		RW	0x0
7:4	ARID		RW	0x0
3:0	AWID		RW	0x0

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Table 12-11. Register Call Summary for Register AQAXICONFIG

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- BB2D Register Summary: [0]

Table 12-12. AQAXISTATUS

Address Offset	0x0000 000C		
Physical Address	0x5900 000C	**Instance**	BB2D
Description	AXI status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						DET_RD_ERR	DET_WR_ERR	RD_ERR_ID				WR_ERR_ID			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x00 0000
9	DET_RD_ERR		R	0
8	DET_WR_ERR		R	0
7:4	RD_ERR_ID		R	0x0
3:0	WR_ERR_ID		R	0x0

Table 12-13. Register Call Summary for Register AQAXISTATUS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-14. AQINTRACKNOWLEDGE

Address Offset	0x0000 0010		
Physical Address	0x5900 0010	**Instance**	BB2D
Description	Interrupt acknowledge register. Each bit represents a corresponding event being triggered. Reading from this register clears the outstanding interrupt.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VEC																															

Bits	Field Name	Description	Type	Reset
31:0	INTR_VEC		R	0x0000 0000

Table 12-15. Register Call Summary for Register AQINTRACKNOWLEDGE

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- BB2D Register Summary: [0]

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Table 12-16. AQINTRENBL

Address Offset	0x0000 0014		
Physical Address	0x5900 0014	**Instance**	BB2D
Description	Interrupt enable register. Each bit enables a corresponding event.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_ENBL_VEC																															

Bits	Field Name	Description	Type	Reset
31:0	INTR_ENBL_VEC		RW	0x0000 0000

Table 12-17. Register Call Summary for Register AQINTRENBL

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- BB2D Register Summary: [0]

Table 12-18. AQIDENT

Address Offset	0x0000 0018		
Physical Address	0x5900 0018	**Instance**	BB2D
Description	Identification register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAMILY								PRODUCT								REVISION				TECHNOLOGY				CUSTOMER							

Bits	Field Name	Description	Type	Reset
31:24	FAMILY	Family value 0x1: GC500 0x2: GC520 0x3: GC530 0x4: GC400 0x5: GC450 0x8: GC600 0x9: GC700 0xA: GC350 0xB: GC380 0xC: GC800 0x10: GC1000 0x14: GC2000	R	0x14
23:16	PRODUCT	Product value	R	0x01
15:12	REVISION	Revision value	R	0x0
11:8	TECHNOLOGY	Technology value	R	0x0
7:0	CUSTOMER	Customer value	R	0x00

Table 12-19. Register Call Summary for Register AQIDENT

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- BB2D Register Summary: [0]

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Table 12-20. GCFEATURES

Address Offset	0x0000 001C		
Physical Address	0x5900 001C	**Instance**	BB2D
Description	Shows which features are enabled in current subsystem implementation. 0 : NONE 1 : AVAILABLE		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE20_BIT_INDEX	RS_YUV_TARGET	BYTE_WRITE_3D	FE20	VGTS	PIPE_VG	MEM32_BIT_SUPPORT	YUY2_RENDER_TARGET	HALF_TX_CACHE	HALF_PE_CACHE	YUY2_AVERAGING	NO_SCALER	BYTE_WRITE_2D	BUFFER_INTERLEAVING	NO422_TEXTURE	NO_EZ	MIN_AREA	MODULE_CG	YUV420_TILER	HIGH_DYNAMIC_RANGE	FAST_SCALER	ETC1_TEXTURE_COMPRESSION	PIPE_2D	DC	MSAA	YUV420_FILTER	ZCOMPRESSION	DEBUG_MODE	DXT_TEXTURE_COMPRESSION	PIPE_3D	SPECIAL_ANTI_ALIASING	FAST_CLEAR

Bits	Field Name	Description	Type	Reset
31	FE20_BIT_INDEX	Supports 20 bit index.	R	1
30	RS_YUV_TARGET	Supports resolveing into YUV target.	R	1
29	BYTE_WRITE_3D	3D PE has byte write capability.	R	1
28	FE20	FE 2.0 is present.	R	0
27	VGTS	VG tesselator is present.	R	0
26	PIPE_VG	VG pipe is present.	R	0
25	MEM32_BIT_SUPPORT	32 bit memory address support.	R	0
24	YUY2_RENDER_TARGET	YUY2 support in PE and YUY2 to RGB conversion in resolve.	R	0
23	HALF_TX_CACHE	TX cache is half.	R	0
22	HALF_PE_CACHE	PE cache is half.	R	0
21	YUY2_AVERAGING	YUY2 averaging support in resolve.	R	1
20	NO_SCALER	No 2D scaler.	R	0
19	BYTE_WRITE_2D	Supports byte write in 2D.	R	1
18	BUFFER_INTERLEAVING	Supports interleaving depth and color buffers.	R	1
17	NO422_TEXTURE	No 422 texture input format.	R	0
16	NO_EZ	No early-Z.	R	0
15	MIN_AREA	Configured to have minimum area.	R	1
14	MODULE_CG	Second level clock gating is available.	R	1
13	YUV420_TILER	YUV 4:2:0 tiler is available.	R	1
12	HIGH_DYNAMIC_RANGE	Shows if there is HDR support.	R	1
11	FAST_SCALER	Shows if there is HD scaler.	R	1
10	ETC1_TEXTURE_COMPRESSION	ETC1 texture compression.	R	1
9	PIPE_2D	Shows if there is 2D engine.	R	1
8	DC	Shows if there is a display controller.	R	0
7	MSAA	MSAA support.	R	1
6	YUV420_FILTER	YUV 4:2:0 support in filter blit.	R	1
5	ZCOMPRESSION	Depth and color compression.	R	0

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Bits	Field Name	Description	Type	Reset
4	DEBUG_MODE	Debug registers.	R	0
3	DXT_TEXTURE_COMPRESSION	DXT texture compression.	R	1
2	PIPE_3D	3D pipe.	R	0
1	SPECIAL_ANTI_ALIASING	Full-screen anti-aliasing.	R	1
0	FAST_CLEAR	Fast clear.	R	0

Table 12-21. Register Call Summary for Register GCFEATURES

BB2D Register Manual
- BB2D Register Summary: [0]

Table 12-22. GCCHIPID

Address Offset	0x0000 0020		
Physical Address	0x5900 0020	**Instance**	BB2D
Description	Shows the ID for the subsystem in BCD.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															

Bits	Field Name	Description	Type	Reset
31:0	ID	Subsystem ID in BCD	R	0x0000 0320

Table 12-23. Register Call Summary for Register GCCHIPID

BB2D Register Manual
- BB2D Register Summary: [0]

Table 12-24. GCCHIPREV

Address Offset	0x0000 0024		
Physical Address	0x5900 0024	**Instance**	BB2D
Description	Shows the revision for the subsystem in BCD.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	Revision in BCD	R	0x0000 5301

Table 12-25. Register Call Summary for Register GCCHIPREV

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- BB2D Register Summary: [0]

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Table 12-26. GCCHIPDATE

Address Offset	0x0000 0028		
Physical Address	0x5900 0028	**Instance**	BB2D
Description	Shows the release date for the subsystem.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATE																															

Bits	Field Name	Description	Type	Reset
31:0	DATE	Release date	R	0x2011 1103

Table 12-27. Register Call Summary for Register GCCHIPDATE

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- BB2D Register Summary: [0]

Table 12-28. GCCHIPTIME

Address Offset	0x0000 002C		
Physical Address	0x5900 002C	**Instance**	BB2D
Description	Shows the release time for the subsystem.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME																															

Bits	Field Name	Description	Type	Reset
31:0	TIME	Release time	R	0x0014 0300

Table 12-29. Register Call Summary for Register GCCHIPTIME

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- BB2D Register Summary: [0]

Table 12-30. GCCHIPCUSTOMER

Address Offset	0x0000 0030		
Physical Address	0x5900 0030	**Instance**	BB2D
Description	Shows the customer and group for the subsystem.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPANY																GROUP															

Bits	Field Name	Description	Type	Reset
31:16	COMPANY	Company	R	0x0000
15:0	GROUP	Group	R	0x0000

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Table 12-31. Register Call Summary for Register GCCHIPCUSTOMER

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- BB2D Register Summary: [0]

Table 12-32. GCMINORFEATURES0

Address Offset	0x0000 0034		
Physical Address	0x5900 0034	**Instance**	BB2D
Description	Shows which minor features are enabled in the subsytem. 0 : NONE 1 : AVAILABLE		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENHANCE_VR	CORRECT_STENCIL	A8_TARGET_SUPPORT	NEW_TEXTURE	HIERARCHICAL_Z	BYPASS_IN_MSAA	VAA	BUG_FIXES0	SHADER_MSAA_SIDEBAND	MC_20	DEFAULT_REG0	EXTRA_SHADER_INSTRUCTIONS1	SHADER_GETS_W	VG_21	VG_FILTER	EXTRA_SHADER_INSTRUCTIONS0	COMPRESSION_FIFO_FIXED	TS_EXTENDED_COMMANDS	VG_20	SUPER_TILED_32X32	SEPARATE_TILE_STATUS_WHEN_INTERLEAVED	TILE_STATUS_2BITS	RENDER_8K	CORRECT_AUTO_DISABLE	PE20_2D	FAST_CLEAR_FLUSH	SPECIAL_MSAA_LOD	CORRECT_TEXTURE_CONVERTER	TEXTURE8_K	ENDIANNESS_CONFIG	DUAL_RETURN_BUS	FLIP_Y

Bits	Field Name	Description	Type	Reset
31	ENHANCE_VR	Enhance VR and add a mode to walk 16 pixels in 16-bit mode in vertical pass to improve cache hit rate when rotating 90/270.	R	1
30	CORRECT_STENCIL	Correct stencil behavior in depth only.	R	1
29	A8_TARGET_SUPPORT	2D engine supports A8 target.	R	0
28	NEW_TEXTURE	New texture unit is available.	R	0
27	HIERARCHICAL_Z	Hierarchiccal Z is supported.	R	1
26	BYPASS_IN_MSAA	Shader supports bypass mode when MSAA is enabled.	R	0
25	VAA	VAA is available or not.	R	0
24	BUG_FIXES0		R	1
23	SHADER_MSAA_SIDEBAND	Put the MSAA data into sideband fifo.	R	0
22	MC_20	New style MC with separate paths for color and depth.	R	0
21	DEFAULT_REG0	Unavailable registers will return 0.	R	1
20	EXTRA_SHADER_INSTRUCTIONS1	Sqrt, sin, cos instructions are available.	R	1
19	SHADER_GETS_W	W is sent to SH from RA.	R	1
18	VG_21	Minor updates to VG pipe (Event generation from VG, TS, PE). Tiled image support.	R	0
17	VG_FILTER	VG filter is available.	R	0
16	EXTRA_SHADER_INSTRUCTIONS0	Floor, ceil, and sign instructions are available.	R	1

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Bits	Field Name	Description	Type	Reset
15	COMPRESSION_FIFO_FIXED	If this bit is not set, the FIFO counter should be set to 50. Else, the default should remain.	R	1
14	TS_EXTENDED_COMMANDS	New commands added to the tessellator.	R	0
13	VG_20	Major updates to VG pipe (TS buffer tiling. State masking.).	R	0
12	SUPER_TILED_32X32	32 × 32 super tile is available.	R	1
11	SEPARATE_TILE_STATUS_WHEN_INTERLEAVED	Use 2 separate tile status buffers in interleaved mode.	R	1
10	TILE_STATUS_2BITS	2 bits are used instead of 4 bits for tile status.	R	1
9	RENDER_8K	Supports 8K render target.	R	1
8	CORRECT_AUTO_DISABLE	Reserved.	R	0
7	PE20_2D	2D PE 2.0 is present.	R	1
6	FAST_CLEAR_FLUSH	Proper flush is done in fast clear cache.	R	1
5	SPECIAL_MSAA_LOD	Special LOD calculation when MSAA is on.	R	1
4	CORRECT_TEXTURE_CONVERTER	Driver hack is not needed.	R	1
3	TEXTURE8_K	Supports 8K × 8K textures.	R	1
2	ENDIANNESS_CONFIG	Configurable endianness support.	R	1
1	DUAL_RETURN_BUS	Dual Return Bus from HI to clients.	R	1
0	FLIP_Y	Y flipping capability is added to resolve.	R	1

Table 12-33. Register Call Summary for Register GCMINORFEATURES0

BB2D Register Manual
- BB2D Register Summary: [0]

Table 12-34. GCRESETMEMCOUNTERS

Address Offset	0x0000 003C		
Physical Address	0x5900 003C	**Instance**	BB2D
Description	Writing 1 will reset the counters and stop counting. Write 0 to start counting again.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESET

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		W	0x649C CF7F
0	RESET	1: reset the counters and stop counting 0: start counting	W	1

Table 12-35. Register Call Summary for Register GCRESETMEMCOUNTERS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 12-36. GCTOTALREADS

Address Offset	0x0000 0040		
Physical Address	0x5900 0040	**Instance**	BB2D
Description	Total reads in terms of 64 bits.		

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Table 12-36. GCTOTALREADS (continued)

Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total reads in terms of 64 bits	R	0x0000 0000

Table 12-37. Register Call Summary for Register GCTOTALREADS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-38. GCTOTALWRITES

Address Offset	0x0000 0044		
Physical Address	0x5900 0044	**Instance**	BB2D
Description	Total writes in terms of 64 bits.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total writes in terms of 64 bits	R	0x0000 0000

Table 12-39. Register Call Summary for Register GCTOTALWRITES

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- BB2D Register Summary: [0]

Table 12-40. GCCHIPSPECS

Address Offset	0x0000 0048		
Physical Address	0x5900 0048	**Instance**	BB2D
Description	Specs for the subsystem.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERTEX_OUTPUT_BUFFER_SIZE				NUM_PIXEL_PIPES				NUM_SHADER_CORES				RESERVED				VERTEX_CACHE_SIZE				THREAD_COUNT				TEMP_REGISTERS				STREAMS			

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Bits	Field Name	Description	Type	Reset
31:28	VERTEX_OUTPUT_BUFFER_SIZE		R	0x0
27:25	NUM_PIXEL_PIPES		R	0x0
24:20	NUM_SHADER_CORES		R	0x00
19:17	RESERVED		R	0x0
16:12	VERTEX_CACHE_SIZE		R	0x00
11:8	THREAD_COUNT		R	0x0
7:4	TEMP_REGISTERS		R	0x0
3:0	STREAMS		R	0x0

Table 12-41. Register Call Summary for Register GCCHIPSPECS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-42. GCTOTALWRITEBURSTS

Address Offset	0x0000 004C		
Physical Address	0x5900 004C	**Instance**	BB2D
Description	Total write data count in terms of 64 bits.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total write data count in terms of 64 bits	R	0x0000 0000

Table 12-43. Register Call Summary for Register GCTOTALWRITEBURSTS

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- BB2D Register Summary: [0]

Table 12-44. GCTOTALWRITEREQS

Address Offset	0x0000 0050		
Physical Address	0x5900 0050	**Instance**	BB2D
Description	Total write request count.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total write request count	R	0x0000 0000

Table 12-45. Register Call Summary for Register GCTOTALWRITEREQS

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1]

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Table 12-46. GCTOTALWRITELASTS

Address Offset	0x0000 0054		
Physical Address	0x5900 0054	**Instance**	BB2D
Description	Total WLAST count. This is used to match with GCTOTALWRITEREQS		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total WLAST count	R	0x0000 0000

Table 12-47. Register Call Summary for Register GCTOTALWRITELASTS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-48. GCTOTALREADBURSTS

Address Offset	0x0000 0058		
Physical Address	0x5900 0058	**Instance**	BB2D
Description	Total read data count in terms of 64 bits.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total read data count in terms of 64 bits	R	0x0000 0000

Table 12-49. Register Call Summary for Register GCTOTALREADBURSTS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-50. GCTOTALREADREQS

Address Offset	0x0000 005C		
Physical Address	0x5900 005C	**Instance**	BB2D
Description	Total read request count.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total read request count	R	0x0000 0000

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Table 12-51. Register Call Summary for Register GCTOTALREADREQS

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 12-52. GCTOTALREADLASTS

Address Offset	0x0000 0060		
Physical Address	0x5900 0060	**Instance**	BB2D
Description	Total RLAST count. This is used to match with GCTOTALREADREQS		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Total RLAST count	R	0x0000 0000

Table 12-53. Register Call Summary for Register GCTOTALREADLASTS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-54. GCGPOUT0

Address Offset	0x0000 0064		
Physical Address	0x5900 0064	**Instance**	BB2D
Description	General purpose output register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															GCHOLD

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	RW	0x0000 0000
0	GCHOLD	1 : Low power mode	RW	0

Table 12-55. Register Call Summary for Register GCGPOUT0

BB2D Functional Description

- BB2D Power Management: [0]

BB2D Register Manual

- BB2D Register Summary: [1]

Table 12-56. GCAXICONTROL

Address Offset	0x0000 0070		
Physical Address	0x5900 0070	**Instance**	BB2D
Description	Special handling on AXI Bus		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WR_FULL_BURST_MODE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	WR_FULL_BURST_MODE	0: NO_BURST_RESET_VALUE 1: BURST_RESET_VALUE	RW	0

Table 12-57. Register Call Summary for Register GCAXICONTROL

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-58. GCMINORFEATURES1

Address Offset	0x0000 0074		
Physical Address	0x5900 0074	**Instance**	BB2D
Description	Shows which features are enabled in the subsystem. 0 : NONE 1 : AVAILABLE		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FC_FLUSH_STALL	BUG_FIXES6	WIDE_LINE	MMU	OK_TO_GATE_AXI_CLOCK	RESOLVE_OFFSET	NEGATIVE_LOG_FIX	CORRECT_OVERFLOW_VG	HALTI0	LINEAR_TEXTURE_SUPPORT	NON_POWER_OF_TWO	TEXTURE_HORIZONTAL_ALIGNMENT_SELECT	NEW_FLOATING_POINT_ARITHMETIC	NEW_2D	BUG_FIXES5	DITHER_AND_FILTER_PLUS_ALPHA_2D	CORRECT_MIN_MAX_DEPTH	EXTENDED_PIXEL_FORMAT	TWO_STENCIL_REFERENCE	PIXEL_DITHER	HALF_FLOAT_PIPE	L2_WINDOWING	BUG_FIXES4	AUTO_RESTART_TS	CORRECT_AUTO_DISABLE	BUG_FIXES3	TEXTURE_STRIDE	BUG_FIXES2	BUG_FIXES1	VG_DOUBLE_BUFFER	V2_COMPRESSION	RSUV_SWIZZLE

Bits	Field Name	Description	Type	Reset
31	FC_FLUSH_STALL		R	1
30	BUG_FIXES6		R	1
29	WIDE_LINE		R	1
28	MMU		R	1
27	OK_TO_GATE_AXI_CLOCK		R	1
26	RESOLVE_OFFSET		R	1

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Bits	Field Name	Description	Type	Reset
25	NEGATIVE_LOG_FIX		R	1
24	CORRECT_OVERFLOW_VG		R	0
23	HALTI0		R	0
22	LINEAR_TEXTURE_SUPPORT		R	0
21	NON_POWER_OF_TWO		R	0
20	TEXTURE_HORIZONTAL_ALIGNMENT_SELECT		R	1
19	NEW_FLOATING_POINT_ARITHMETIC		R	1
18	NEW_2D		R	1
17	BUG_FIXES5		R	1
16	DITHER_AND_FILTER_PLUS_ALPHA_2D	Dither and filter+alpha available.	R	1
15	CORRECT_MIN_MAX_DEPTH	EEZ and HZ are correct.	R	1
14	EXTENDED_PIXEL_FORMAT		R	0
13	TWO_STENCIL_REFERENCE		R	1
12	PIXEL_DITHER		R	1
11	HALF_FLOAT_PIPE		R	0
10	L2_WINDOWING		R	0
9	BUG_FIXES4		R	1
8	AUTO_RESTART_TS		R	0
7	CORRECT_AUTO_DISABLE		R	1
6	BUG_FIXES3		R	1
5	TEXTURE_STRIDE	Texture has stride and memory addressing.	R	0
4	BUG_FIXES2		R	1
3	BUG_FIXES1		R	1
2	VG_DOUBLE_BUFFER	Double buffering support for VG (second TS-->VG semaphore is present).	R	0
1	V2_COMPRESSION	V2 compression.	R	1
0	RSUV_SWIZZLE	Resolve UV swizzle.	R	1

Table 12-59. Register Call Summary for Register GCMINORFEATURES1

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-60. GCTOTALCYCLES

Address Offset	0x0000 0078		
Physical Address	0x5900 0078	**Instance**	BB2D
Description	Total cycles. This register is a free running counter. It can be reset by writing 0 to it.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CYCLES																															

Bits	Field Name	Description	Type	Reset
31:0	CYCLES	Total cycles	RW	0x0000 1DE2

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Table 12-61. Register Call Summary for Register GCTOTALCYCLES

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 12-62. GCTOTALIDLECYCLES

Address Offset	0x0000 007C		
Physical Address	0x5900 007C	**Instance**	BB2D
Description	Total cycles where the GPU is idle. It is reset when GCTOTALCYCLES register is written to. It looks at all the blocks but FE when determining the subsystem is idle.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CYCLES																															

Bits	Field Name	Description	Type	Reset
31:0	CYCLES	Total cycles where the GPU is idle	RW	0x0000 1E08

Table 12-63. Register Call Summary for Register GCTOTALIDLECYCLES

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-64. GCCHIPSPECS2

Address Offset	0x0000 0080		
Physical Address	0x5900 0080	**Instance**	BB2D
Description	Specs for the subsystem		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUMBER_OF_CONSTANTS																INSTRUCTION_COUNT								BUFFER_SIZE							

Bits	Field Name	Description	Type	Reset
31:16	NUMBER_OF_CONSTANTS		R	0x0000
15:8	INSTRUCTION_COUNT		R	0x00
7:0	BUFFER_SIZE		R	0x00

Table 12-65. Register Call Summary for Register GCCHIPSPECS2

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-66. GCMINORFEATURES2

Address Offset	0x0000 0084		
Physical Address	0x5900 0084	**Instance**	BB2D
Description	Shows which features are enabled in the subsystem 0 : NONE 1 : AVAILABLE		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			NO_INDEX_PATTERN	RESERVED	NOT_USED	MIXED_STREAMS	INTERLEAVER	FLUSH_FIXED_2D	YUV_CONVERSION	MULTI_SOURCE_BLT	YUV_STANDARD	TILE_FILLER	THREAD_WALKER_IN_PS	ONE_PASS_2D_FILTER	FULL_DIRECT_FB	TX_FILTER	DYNAMIC_FREQUENCY_SCALING	TX_YUV_ASSEMBLER	RGB888	HALTI1	S1S8	END_EVENT	PE_SWIZZLE	CORRECT_AUTO_DISABLE_COUNT_WIDTH	COMPOSITION	RECT_PRIMITIVE	LINEAR_PE	SUPER_TILED_TEXTURE	SEAMLESS_CUBE_MAP	LOGIC_OP	LINE_LOOP

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28	NO_INDEX_PATTERN		R	1
27	RESERVED		R	1
26	NOT_USED		R	0
25	MIXED_STREAMS		R	1
24	INTERLEAVER		R	0
23	FLUSH_FIXED_2D		R	1
22	YUV_CONVERSION		R	1
21	MULTI_SOURCE_BLT		R	1
20	YUV_STANDARD		R	1
19	TILE_FILLER		R	1
18	THREAD_WALKER_IN_PS		R	1
17	ONE_PASS_2D_FILTER		R	1
16	FULL_DIRECT_FB		R	1
15	TX_FILTER		R	0
14	DYNAMIC_FREQUENCY_SCALING		R	1
13	TX_YUV_ASSEMBLER		R	0
12	RGB888		R	0
11	HALTI1		R	0
10	S1S8		R	0
9	END_EVENT		R	0
8	PE_SWIZZLE		R	0
7	CORRECT_AUTO_DISABLE_COUNT_WIDTH		R	1
6	COMPOSITION		R	0
5	RECT_PRIMITIVE		R	0
4	LINEAR_PE		R	0
3	SUPER_TILED_TEXTURE		R	0
2	SEAMLESS_CUBE_MAP		R	0
1	LOGIC_OP		R	0
0	LINE_LOOP		R	0

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Table 12-67. Register Call Summary for Register GCMINORFEATURES2

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- BB2D Register Summary: [0]

Table 12-68. GCMODULEPOWERCONTROLS

Address Offset	0x0000 0100		
Physical Address	0x5900 0100	**Instance**	BB2D
Description	Control register for module level power controls.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TURN_OFF_COUNTER																RESERVED								TURN_ON_COUNTER				RESERVED	DISABLE_STARVE_MODULE_CLOCK_GATING	DISABLE_STALL_MODULE_CLOCK_GATING	ENABLE_MODULE_CLOCK_GATING

Bits	Field Name	Description	Type	Reset
31:16	TURN_OFF_COUNTER	Counter value for clock gating the module if the module is idle for this amount of clock cycles	RW	0x0014
15:8	RESERVED		R	0x00
7:4	TURN_ON_COUNTER	Number of clock cycles to wait after turning on the clock	RW	0x2
3	RESERVED		R	0
2	DISABLE_STARVE_MODULE_CLOCK_GATING	Disables module level clock gating for starve/idle condition	RW	0
1	DISABLE_STALL_MODULE_CLOCK_GATING	Disables module level clock gating for stall condition	RW	0
0	ENABLE_MODULE_CLOCK_GATING	Enables module level clock gating	RW	0

Table 12-69. Register Call Summary for Register GCMODULEPOWERCONTROLS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-70. GCMODULEPOWERMODULECONTROL

Address Offset	0x0000 0104		
Physical Address	0x5900 0104	**Instance**	BB2D
Description	Module level control registers.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DISABLE_MODULE_CLOCK_GATING_TX	DISABLE_MODULE_CLOCK_GATING_RA	DISABLE_MODULE_CLOCK_GATING_SE	DISABLE_MODULE_CLOCK_GATING_PA	DISABLE_MODULE_CLOCK_GATING_SH	DISABLE_MODULE_CLOCK_GATING_PE	DISABLE_MODULE_CLOCK_GATING_DE	DISABLE_MODULE_CLOCK_GATING_FE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7	DISABLE_MODULE_CLOCK_GATING_TX	Disables module level clock gating for starve/idle condition	RW	0
6	DISABLE_MODULE_CLOCK_GATING_RA	Disables module level clock gating for stall condition	RW	0
5	DISABLE_MODULE_CLOCK_GATING_SE	Enables module level clock gating	RW	0
4	DISABLE_MODULE_CLOCK_GATING_PA	Counter value for clock gating the module if the module is idle for this amount of clock cycles	RW	0
3	DISABLE_MODULE_CLOCK_GATING_SH	Number of clock cycles to wait after turning on the clock	RW	0
2	DISABLE_MODULE_CLOCK_GATING_PE	Disables module level clock gating for starve/idle condition	RW	0
1	DISABLE_MODULE_CLOCK_GATING_DE	Disables module level clock gating for stall condition	RW	0
0	DISABLE_MODULE_CLOCK_GATING_FE	Enables module level clock gating	RW	0

Table 12-71. Register Call Summary for Register GCMODULEPOWERMODULECONTROL

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-72. GCMODULEPOWERMODULESTATUS

Address Offset	0x0000 0108		
Physical Address	0x5900 0108	**Instance**	BB2D
Description	Module level control status		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODULE_CLOCK_GATED_TX	MODULE_CLOCK_GATED_RA	MODULE_CLOCK_GATED_SE	MODULE_CLOCK_GATED_PA	MODULE_CLOCK_GATED_SH	MODULE_CLOCK_GATED_PE	MODULE_CLOCK_GATED_DE	MODULE_CLOCK_GATED_FE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7	MODULE_CLOCK_GATED_TX	Module level clock gating is ON for TX	R	0
6	MODULE_CLOCK_GATED_RA	Module level clock gating is ON for RA	R	0
5	MODULE_CLOCK_GATED_SE	Module level clock gating is ON for SE	R	0
4	MODULE_CLOCK_GATED_PA	Module level clock gating is ON for PA	R	0
3	MODULE_CLOCK_GATED_SH	Module level clock gating is ON for SH	R	0
2	MODULE_CLOCK_GATED_PE	Module level clock gating is ON for PE	R	0
1	MODULE_CLOCK_GATED_DE	Module level clock gating is ON for DE	R	0
0	MODULE_CLOCK_GATED_FE	Module level clock gating is ON for FE	R	0

Table 12-73. Register Call Summary for Register GCMODULEPOWERMODULESTATUS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-74. GCREGMMUSTATUS

Address Offset	0x0000 0188		
Physical Address	0x5900 0188	**Instance**	BB2D
Description	Status register that holds which MMU generated an exception		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		EXCEPTION3		RESERVED		EXCEPTION2		RESERVED		EXCEPTION1		RESERVED		EXCEPTION0	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	NOT USED	R	0x0 0000
13:12	EXCEPTION3	MMU 3 caused an exception and the GCREGMMUEXCEPTION3 register holds the offending address. 0x1: SLAVE_NOT_PRESENT 0x2: PAGE_NOT_PRESENT 0x3: WRITE_VIOLATION	R	0x0
11:10	RESERVED	NOT USED	R	0x0

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Bits	Field Name	Description	Type	Reset
9:8	EXCEPTION2	MMU 2 caused an exception and the GCREGMMUEXCEPTION2 register holds the offending address. 0x1: SLAVE_NOT_PRESENT 0x2: PAGE_NOT_PRESENT 0x3: WRITE_VIOLATION	R	0x0
7:6	RESERVED	NOT USED	R	0x0
5:4	EXCEPTION1	MMU 1 caused an exception and the GCREGMMUEXCEPTION1 register holds the offending address. 0x1: SLAVE_NOT_PRESENT 0x2: PAGE_NOT_PRESENT 0x3: WRITE_VIOLATION	R	0x0
3:2	RESERVED	NOT USED	R	0x0
1:0	EXCEPTION0	MMU 0 caused an exception and the GCREGMMUEXCEPTION0 holds the offending address: 0x1: SLAVE_NOT_PRESENT 0x2: PAGE_NOT_PRESENT 0x3: WRITE_VIOLATION	R	0x0

Table 12-75. Register Call Summary for Register GCREGMMUSTATUS

BB2D Register Manual
- BB2D Register Summary: [0]

Table 12-76. GCREGMMUCONTROL

Address Offset	0x0000 018C		
Physical Address	0x5900 018C	**Instance**	BB2D
Description	Control register that enables the MMU (one time shot).		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															ENABLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	NOT USED	W	0x0000 0000
0	ENABLE	Enable the MMU. For security reasons, once the MMU is enabled it cannot be disabled until reset.	W	0

Table 12-77. Register Call Summary for Register GCREGMMUCONTROL

BB2D Register Manual
- BB2D Register Summary: [0]

Table 12-78. GCREGMMUEXCEPTION0

Address Offset	0x0000 0190		
Physical Address	0x5900 0190	**Instance**	BB2D
Description	Holds the original address that generated an exception		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	ADDRESS	The original address that generated an exception	RW	0x0000 0000

Table 12-79. Register Call Summary for Register GCREGMMUEXCEPTION0

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 12-80. GCREGMMUEXCEPTION1

Address Offset	0x0000 0194		
Physical Address	0x5900 0194	**Instance**	BB2D
Description	Holds the original address that generated an exception		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	ADDRESS	The original address that generated an exception	RW	0x0000 0000

Table 12-81. Register Call Summary for Register GCREGMMUEXCEPTION1

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 12-82. GCREGMMUEXCEPTION2

Address Offset	0x0000 0198		
Physical Address	0x5900 0198	**Instance**	BB2D
Description	Holds the original address that generated an exception		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	ADDRESS	The original address that generated an exception	RW	0x0000 0000

Table 12-83. Register Call Summary for Register GCREGMMUEXCEPTION2

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1]

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Table 12-84. GCREGMMUEXCEPTION3

Address Offset	0x0000 019C		
Physical Address	0x5900 019C	**Instance**	BB2D
Description	Holds the original address that generated an exception		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	ADDRESS	The original address that generated an exception	RW	0x0000 0000

Table 12-85. Register Call Summary for Register GCREGMMUEXCEPTION3

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1]

Table 12-86. AQMEMORYDEBUG

Address Offset	0x0000 0414		
Physical Address	0x5900 0414	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DONT_STALL_WRITES_TO_SAME_ADDRESS	ZCOMP_LIMIT						DISABLE_WRITE_DATA_SPEEDUP	DISABLE_STALL_READS	RESERVED		LIMIT_CONTROL	RESERVED	INTERLEAVE_BUFFER_LOW_LATENCY_MODE	RESERVED	DISABLE_MINI_MMU_CACHE	RESERVED							MAX_OUTSTANDING_READS							

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30	DONT_STALL_WRITES_TO_SAME_ADDRESS		RW	0
29:24	ZCOMP_LIMIT		RW	0x3C
23	DISABLE_WRITE_DATA_SPEEDUP		RW	0
22	DISABLE_STALL_READS		RW	0
21:20	RESERVED	Reserved	RW	0

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Bits	Field Name	Description	Type	Reset
19	LIMIT_CONTROL	Limit control 0: REQUESTS 1: DATA	RW	0
18	RESERVED	Reserved	R	0
17	INTERLEAVE_BUFFER_LOW_LATENCY_MODE		RW	0
16:15	RESERVED	Reserved	R	0x0
14	DISABLE_MINI_MMU_CACHE		RW	0
13:8	RESERVED	Reserved	R	0x00
7:0	MAX_OUTSTANDING_READS	Limits the total number of outstanding read requests.	RW	0x00

Table 12-87. Register Call Summary for Register AQMEMORYDEBUG

BB2D Register Manual
- BB2D Register Summary: [0]
- BB2D Register Description: [1] [2]

Table 12-88. AQREGISTERTIMINGCONTROL

Address Offset	0x0000 042C		
Physical Address	0x5900 042C	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LIGHT_SLEEP	DEEP_SLEEP	POWER_DOWN	FAST_WTC			FAST_RTC		FOR_RF2P								FOR_RF1P							

Bits	Field Name	Description	Type	Reset
31:23	RESERVED	Reserved	RW	0x000
22	LIGHT_SLEEP	Light sleep	RW	0
21	DEEP_SLEEP	Deep sleep	RW	0
20	POWER_DOWN	Powerdown memory	RW	0
19:18	FAST_WTC	WTC for fast RAMs	RW	0x0
17:16	FAST_RTC	RTC for fast RAMs	RW	0x3
15:8	FOR_RF2P		RW	0x00
7:0	FOR_RF1P		RW	0x00

Table 12-89. Register Call Summary for Register AQREGISTERTIMINGCONTROL

BB2D Register Manual
- BB2D Register Summary: [0]

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Table 12-90. GCDISPLAYPRIORITY

Address Offset	0x0000 0434		
Physical Address	0x5900 0434	**Instance**	BB2D
Description	Controls the priority of the display controller requests. This works like a PWM. One register gives the period, and the other gives the ON time. When PWM is ON, display requests are accepted if both display and the other request is valid. If it is OFF, the other request will be accepted. If only one request is valid, it takes the bus regardless of the PWM bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HIGH								PERIOD							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	HIGH	'Duty cycle'	RW	0x01
7:0	PERIOD	Period	RW	0x02

Table 12-91. Register Call Summary for Register GCDISPLAYPRIORITY

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-92. GCDBGCYCLECOUNTER

Address Offset	0x0000 0438		
Physical Address	0x5900 0438	**Instance**	BB2D
Description	Increments every cycle.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	Increments every cycle	RW	0x0000 1C5E

Table 12-93. Register Call Summary for Register GCDBGCYCLECOUNTER

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-94. GCOUTSTANDINGREADS0

Address Offset	0x0000 043C		
Physical Address	0x5900 043C	**Instance**	BB2D
Description	Number of outstanding reads per client in multiples of 8 bytes.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MMU								FE								PEZ								PEC							

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Bits	Field Name	Description	Type	Reset
31:24	MMU	Number of outstanding MMU reads in multiples of 8 bytes	R	0x00
23:16	FE	Number of outstanding FE reads in multiples of 8 bytes	R	0x00
15:8	PEZ	Number of outstanding PEZ reads in multiples of 8 bytes	R	0x00
7:0	PEC	Number of outstanding PEC reads in multiples of 8 bytes	R	0x00

Table 12-95. Register Call Summary for Register GCOUTSTANDINGREADS0

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-96. GCOUTSTANDINGREADS1

Address Offset	0x0000 0440		
Physical Address	0x5900 0440	**Instance**	BB2D
Description	Number of outstanding reads per client in multiples of 8 bytes.		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
TOTAL	FC	TX	RA

Bits	Field Name	Description	Type	Reset
31:24	TOTAL	This field keeps the value of total read requests or total requested data (in 64 bits) depending on the value of AQMEMORYDEBUG[19] LIMIT_CONTROL register field.	R	0x00
23:16	FC	Number of outstanding FC reads in multiples of 8 bytes	R	0x00
15:8	TX	Number of outstanding TX reads in multiples of 8 bytes	R	0x00
7:0	RA	Number of outstanding RA reads in multiples of 8 bytes	R	0x00

Table 12-97. Register Call Summary for Register GCOUTSTANDINGREADS1

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-98. GCOUTSTANDINGWRITES

Address Offset	0x0000 0444		
Physical Address	0x5900 0444	**Instance**	BB2D
Description	Number of outstanding writes per client.		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
TOTAL	FC	PEZ	PEC

Bits	Field Name	Description	Type	Reset
31:24	TOTAL	This field keeps the value of total write requests or total requested data (in 64 bits) depending on the value of AQMEMORYDEBUG[19] LIMIT_CONTROL register field.	R	0x00
23:16	FC	Number of outstanding FC writes in multiples of 8 bytes	R	0x00
15:8	PEZ	Number of outstanding PEZ writes in multiples of 8 bytes	R	0x00
7:0	PEC	Number of outstanding PEC writes in multiples of 8 bytes	R	0x00

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Table 12-99. Register Call Summary for Register GCOUTSTANDINGWRITES

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-100. GCDEBUGSIGNALSRA

Address Offset	0x0000 0448		
Physical Address	0x5900 0448	**Instance**	BB2D
Description	32 bit debug signal from RA.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL1[19:16] RA: 0x0: Valid pixel count. 0x1: Total quad count (after EEZ). 0x2: Valid quad count (after EZ and EEZ). 0x3: Total primitive count. 0x4: Various signals from input stage. See GC320 spec for details. 0x5: Various signals from input stage. See GC320 spec for details. 0x6: Various signals from render pipe. See GC320 spec for details. 0x7: Various signals from render cache. See GC320 spec for details. 0x8: Various signals from raster engine. See GC320 spec for details. 0x9: Cache miss count (in the pipeline). 0xA: Cache miss count (in the prefetcher). 0xB: EEZ culled quads. 0xF: Signature = 0x12344321.	R	0x0000 0000

Table 12-101. Register Call Summary for Register GCDEBUGSIGNALSRA

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-102. GCDEBUGSIGNALSTX

Address Offset	0x0000 044C		
Physical Address	0x5900 044C	**Instance**	BB2D
Description	32 bit debug signal from TX.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

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Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL1[27:24] TX : 0x0: Total bilinear texture requests. 0x1: Total trilinear texture requests. 0x2: Total discarded texture requests. 0x3: Total texture requests. 0x4: Various signals from input stage. See GC320 spec for details. 0x5: Memory read count. 0x6: Memory read count in 8B. 0x7: Cache miss count (in the pipeline). 0x8: Total hitting texels (in pre-fetcher). 0x9: Total missing texels (in pre-fetcher). 0xF: Signature = 0x12211221.	R	0x0000 0000

Table 12-103. Register Call Summary for Register GCDEBUGSIGNALSTX

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-104. GCDEBUGSIGNALSFE

Address Offset	0x0000 0450		
Physical Address	0x5900 0450	**Instance**	BB2D
Description	32 bit debug signal from FE.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL		R	0x0000 0000

Table 12-105. Register Call Summary for Register GCDEBUGSIGNALSFE

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-106. GCDEBUGSIGNALSPE

Address Offset	0x0000 0454		
Physical Address	0x5900 0454	**Instance**	BB2D
Description	32 bit debug signal from PE.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

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Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL0[19:16] PE: 0x0: pixel count killed by color pipe 0x1: pixel count killed by depth pipe 0x2: pixel count drawn by color pipe 0x3: pixel count drawn by depth pipe 0x4: debug signals for 3d_io, 2d_filter, 2d_fsm 0x5: debug signals for cache2d_cntrl 0x6: debug signals for cache2d_tag_alloc 0x7: debug signals for cache3d_c_cntrl, cache3d_c_tag_alloc 0x8: debug signals for cache3d_z_cntrl, cache3d_z_tag_alloc 0x9: debug signals for pref_2d, pref_3d 0xA : debug signals for cmd_state 0xB: 2d pixel count drawn by 2d pipe 0xF: Signature = 0xBABEF00D.	R	0x0000 0000

Table 12-107. Register Call Summary for Register GCDEBUGSIGNALSPE

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-108. GCDEBUGSIGNALSDE

Address Offset	0x0000 0458		
Physical Address	0x5900 0458	**Instance**	BB2D
Description	32 bit debug signal from DE.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL		R	0x0000 0000

Table 12-109. Register Call Summary for Register GCDEBUGSIGNALSDE

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-110. GCDEBUGSIGNALSSH

Address Offset	0x0000 045C		
Physical Address	0x5900 045C	**Instance**	BB2D
Description	32 bit debug signal from SH.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

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Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL0[27:24] SH. Please refer to GC320 spec for bit position information for all the signals 0x0 : interface signals for debug 0x1 : Instruction Sequencing and vertex input state machine 0x2 : vertex input/output buffer full/empty. Context PC. Physical page valid 0x3 : vertex/pixel, output attribute counts. Some interface signals 0x4 : Shader cycle count, for determining the shader clock 0x5 : Current pixel XY value 0x6 : Last pixels XY value 0x7 : Total pixel instructions executed 0x8 : Total pixels shaded 0x9 : Total vertex instructions executed 0xA : Total vertices shaded 0xB : Total vertex branch instructions 0xC : Total vertex texture instructions 0xD : Total pixel branch instructions 0xE : Total pixel texture instructions 0xF : Reserved signature 0xDEADBEEF	R	0x0000 0000

Table 12-111. Register Call Summary for Register GCDEBUGSIGNALSSH

BB2D Register Manual
- BB2D Register Summary: [0]

Table 12-112. GCDEBUGSIGNALSPA

Address Offset	0x0000 0460		
Physical Address	0x5900 0460	**Instance**	BB2D
Description	32 bit debug signal from PA.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL1[3:0] PA: 0x0: Various signals from input stage. See GC320 spec for details. 0x1: Various signals from input stage. See GC320 spec for details. 0x2: Various signals from input stage. See GC320 spec for details. 0x3: total vertex count 0x4: input primitive count 0x5: output primitive count 0x6: depth clipped primitive count 0x7: trivial rejected primitive count 0x8: culled primitive count 0xF: Signature = 0x0000AAAA	R	0x0000 0000

Table 12-113. Register Call Summary for Register GCDEBUGSIGNALSPA

BB2D Register Manual
- BB2D Register Summary: [0]

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Table 12-114. GCDEBUGSIGNALSSE

Address Offset	0x0000 0464		
Physical Address	0x5900 0464	**Instance**	BB2D
Description	32 bit debug signal from SE.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL1[11:8] SE: 0x0: culled triangles count. 0x1: culled lines count. 0x2: [31:18] goto signals, [17:8] main state machine state, [7:0] output state machine state. See GC320 spec for details. 0x3: [31:22] unused, [21] early_isTriangle, [20] isTriangle, [19] increment_pc_e0, [18:14] jump_to_signals. See GC320 spec for details. [13:12] max_x_p_e2, [11:10] mid_x_p_e2, [9:8] min_x_p_e2, [7:6] max_y_p_e2, [5:4] mid_y_p_e2. See GC320 spec for details. [3:2] min_y_p_e2, [1:0] min_z_p_e2. See GC320 spec for details. 0x4: area_e2. See GC320 spec for details. 0x5: x0_e2. See GC320 spec for details. 0x6: x1_e2. See GC320 spec for details. 0x7: x2_e2. See GC320 spec for details. 0x8: y0_e2. See GC320 spec for details. 0x9: y1_e2. See GC320 spec for details. 0xA: y2_e2. See GC320 spec for details. 0xB: init_y_e2. See GC320 spec for details. 0xC: init_y_e2. See GC320 spec for details. 0xD: y2_e2. See GC320 spec for details. 0xE: y2_e2. See GC320 spec for details. 0xF: Signature = 0x5E5E5E5E.	R	0x0000 0000

Table 12-115. Register Call Summary for Register GCDEBUGSIGNALSSE

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-116. GCDEBUGSIGNALSMC

Address Offset	0x0000 0468		
Physical Address	0x5900 0468	**Instance**	BB2D
Description	32 bit debug signal from MC.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL2[3:0] MC: 0x0: Various signals from FC block. See GC320 spec for details. 0x1: Total read req in terms of 8B from pipeline. 0x2: Total read req in terms of 8B sent out from the subsystem. 0x3: Total write req in terms of 8B from pipeline. 0xF: Signature = 0x12345678.	R	0x0000 0000

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Table 12-117. Register Call Summary for Register GCDEBUGSIGNALSMC

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-118. GCDEBUGSIGNALSHI

Address Offset	0x0000 046C		
Physical Address	0x5900 046C	**Instance**	BB2D
Description	32 bit debug signal from HI.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGNAL																															

Bits	Field Name	Description	Type	Reset
31:0	SIGNAL	Signals according to GCDEBUGCONTROL2[11:8] HI: 0x0: Number of cycles AXI read request is stalled. 0x1: Number of cycles AXI write request is stalled. 0x2: Number of cycles AXI write data is stalled. 0xF: Signature = 0xAAAAAAAA	R	0x0000 0000

Table 12-119. Register Call Summary for Register GCDEBUGSIGNALSHI

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-120. GCDEBUGCONTROL0

Address Offset	0x0000 0470		
Physical Address	0x5900 0470	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SH				RESERVED				PE				RESERVED				DE				RESERVED				FE			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	SH	Selects which set of 32 bit data to get from SH. Resets the counters if set to 0xF	RW	0x0
23:20	RESERVED		R	0x0
19:16	PE	Selects which set of 32 bit data to get from PE. Resets the counters if set to 0xF	RW	0x0
15:12	RESERVED		R	0x0
11:8	DE	Selects which set of 32 bit data to get from DE. Resets the counters if set to 0xF	RW	0x0
7:4	RESERVED		R	0x0
3:0	FE	Selects which set of 32 bit data to get from FE. Resets the counters if set to 0xF	RW	0x0

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Table 12-121. Register Call Summary for Register GCDEBUGCONTROL0

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1] [2]

Table 12-122. GCDEBUGCONTROL1

Address Offset	0x0000 0474		
Physical Address	0x5900 0474	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TX				RESERVED				RA				RESERVED				SE				RESERVED				PA			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	TX	Selects which set of 32 bit data to get from TX. Resets the counters if set to 0xF	RW	0x0
23:20	RESERVED		R	0x0
19:16	RA	Selects which set of 32 bit data to get from RA. Resets the counters if set to 0xF	RW	0x0
15:12	RESERVED		R	0x0
11:8	SE	Selects which set of 32 bit data to get from SE. Resets the counters if set to 0xF	RW	0x0
7:4	RESERVED		R	0x0
3:0	PA	Selects which set of 32 bit data to get from PA. Resets the counters if set to 0xF	RW	0x0

Table 12-123. Register Call Summary for Register GCDEBUGCONTROL1

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1] [2] [3] [4]

Table 12-124. GCDEBUGCONTROL2

Address Offset	0x0000 0478		
Physical Address	0x5900 0478	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				HI				RESERVED				MC			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11:8	HI	Selects which set of 32 bit data to get from HI. Resets the counters if set to 0xF	RW	0x0
7:4	RESERVED		R	0x0
3:0	MC	Selects which set of 32 bit data to get from MC. Resets the counters if set to 0xF	RW	0x0

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Table 12-125. Register Call Summary for Register GCDEBUGCONTROL2

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1] [2]

Table 12-126. GCDEBUGCONTROL3

Address Offset	0x0000 047C		
Physical Address	0x5900 047C	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				PROBE1				RESERVED				PROBE0			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11:8	PROBE1	Selects which module's output will be put in the MSB 32 bits of 64 bit debug signal. 0x0: FE 0x1: DE 0x2: PE 0x3: SH 0x4: PA 0x5: SE 0x6: RA 0x7: TX 0x8: MC	RW	0x0
7:4	RESERVED		R	0x0
3:0	PROBE0	Selects which module's output will be put in the LSB 32 bits of 64 bit debug signal. 0x0: FE 0x1: DE 0x2: PE 0x3: SH 0x4: PA 0x5: SE 0x6: RA 0x7: TX 0x8: MC	RW	0x0

Table 12-127. Register Call Summary for Register GCDEBUGCONTROL3

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-128. GCBUSCONTROL

Address Offset	0x0000 0480		
Physical Address	0x5900 0480	**Instance**	BB2D
Description	Shows which features are enabled in the subsystem. 0 : NONE 1 : AVAILABLE		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FCC	TX	FC	MMU	RESERVED	FE	RESERVED	PEZ	PEC

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8	FCC	Select the return bus for FCC	RW	0
7	TX	Select the return bus for TX	RW	1
6	FC	Select the return bus for FC-Depth	RW	0
5	MMU	Select the return bus for MMU	RW	1
4	RESERVED		R	0
3	FE	Select the return bus for FE	RW	1
2	RESERVED		R	0
1	PEZ	Select the return bus for PEZ	RW	0
0	PEC	Select the return bus for PEC	RW	0

Table 12-129. Register Call Summary for Register GCBUSCONTROL

BB2D Register Manual
- BB2D Register Summary: [0]

Table 12-130. GCREGENDIANNESS0

Address Offset	0x0000 0484		
Physical Address	0x5900 0484	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WORD_SWAP																															

Bits	Field Name	Description	Type	Reset
31:0	WORD_SWAP	Flip the words of 32 bit data. 0x12345678 becomes 0x56781234	RW	0x0000 0000

Table 12-131. Register Call Summary for Register GCREGENDIANNESS0

BB2D Register Manual
- BB2D Register Summary: [0]

Table 12-132. GCREGENDIANNESS1

Address Offset	0x0000 0488		
Physical Address	0x5900 0488	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTE_SWAP																															

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Bits	Field Name	Description	Type	Reset
31:0	BYTE_SWAP	Flip the bytes of 16 bit data. 0x12345678 becomes 0x34127856	RW	0x0000 0000

Table 12-133. Register Call Summary for Register GCREGENDIANNESS1

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-134. GCREGENDIANNESS2

Address Offset	0x0000 048C		
Physical Address	0x5900 048C	**Instance**	BB2D
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT_SWAP																															

Bits	Field Name	Description	Type	Reset
31:0	BIT_SWAP	Flip the bits of 8 bit data. 0x12345678 becomes 0x84C2A6E1	RW	0x0000 0000

Table 12-135. Register Call Summary for Register GCREGENDIANNESS2

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-136. GCREGDRAWPRIMITIVESTARTTIMESTAMP

Address Offset	0x0000 0490		
Physical Address	0x5900 0490	**Instance**	BB2D
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_TIME																															

Bits	Field Name	Description	Type	Reset
31:0	START_TIME	32-bit timestamp when PE received draw_primitive_start command	R	0x0000 0000

Table 12-137. Register Call Summary for Register GCREGDRAWPRIMITIVESTARTTIMESTAMP

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-138. GCREGDRAWPRIMITIVEENDTIMESTAMP

Address Offset	0x0000 0494		
Physical Address	0x5900 0494	**Instance**	BB2D
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_TIME																															

Bits	Field Name	Description	Type	Reset
31:0	END_TIME	32-bit timestamp when PE received draw_primitive_end command	R	0x0000 0000

Table 12-139. Register Call Summary for Register GCREGDRAWPRIMITIVEENDTIMESTAMP

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-140. GCREGCONTROL0

Address Offset	0x0000 0558		
Physical Address	0x5900 0558	**Instance**	BB2D
Description	Composition trigger.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC1								OUTSTANDING_READS_PER_CHANNEL								MISC0												ENABLE_UNALIGNED_WRITE_MERGE	ENABLE_WRITE_MERGE	ENABLE_UNALIGNED_MERGE	ENABLE_READ_MERGE

Bits	Field Name	Description	Type	Reset
31:26	MISC1		RW	0x00
25:16	OUTSTANDING_READS_PER_CHANNEL		RW	0x080
15:4	MISC0		RW	0x000
3	ENABLE_UNALIGNED_WRITE_MERGE		RW	0
2	ENABLE_WRITE_MERGE		RW	1
1	ENABLE_UNALIGNED_MERGE		RW	0
0	ENABLE_READ_MERGE		RW	1

Table 12-141. Register Call Summary for Register GCREGCONTROL0

BB2D Register Manual

- BB2D Register Summary: [0]

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Table 12-142. AQCMDBUFFERADDR

Address Offset	0x0000 0654		
Physical Address	0x5900 0654	**Instance**	BB2D
Description	Base address for the command buffer. The address must be 64-bit aligned and it is always physical. To use addresses above 0x8000_0000, program AQMemoryFE with the appropriate offset. Also, this register cannot be read. To check the value of the current fetch address use AQFEDEBUGCURCMDADR.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE	ADDRESS																														

Bits	Field Name	Description	Type	Reset
31	TYPE	0: SYSTEM 1: VIRTUAL_SYSTEM	W	0
30:0	ADDRESS	ADDRESS	W	0x0000 0000

Table 12-143. Register Call Summary for Register AQCMDBUFFERADDR

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-144. AQCMDBUFFERCTRL

Address Offset	0x0000 0658		
Physical Address	0x5900 0658	**Instance**	BB2D
Description	Command buffer control		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										ENDIAN_CONTROL		RESERVED			ENABLE	PREFETCH															

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		W	0x000
21:20	ENDIAN_CONTROL	Endian control 0: NO_SWAP 1: SWAP_WORD 2: SWAP_DWORD	W	0x0
19:17	RESERVED		W	0x0
16	ENABLE	Command buffer 0: DISABLE 1: ENABLE	W	0
15:0	PREFETCH	Number of 64-bit words to fetch from the command buffer.	W	0x0000

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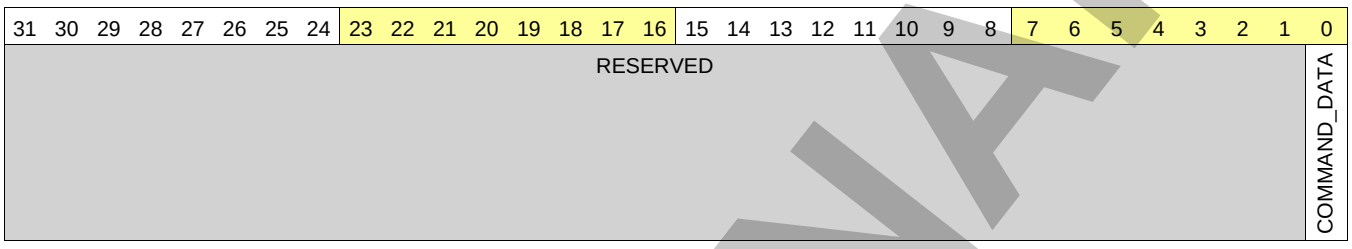
Table 12-145. Register Call Summary for Register AQCMDBUFFERCTRL

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-146. AQFESTATUS

Address Offset	0x0000 065C		
Physical Address	0x5900 065C	**Instance**	BB2D
Description	FE status		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	COMMAND_DATA	Status of the command parser. 0: Idle 1: Busy	R	0

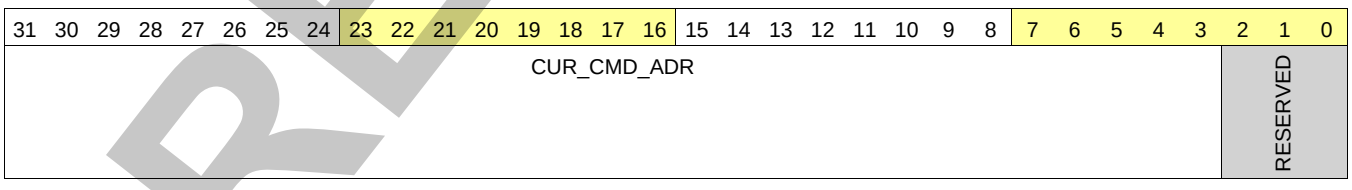
Table 12-147. Register Call Summary for Register AQFESTATUS

BB2D Register Manual

- BB2D Register Summary: [0]

Table 12-148. AQFEDEBUGCURCMDADR

Address Offset	0x0000 0664		
Physical Address	0x5900 0664	**Instance**	BB2D
Description	This is the command decoder address. The address is always physical so the MSB should always be 0.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:3	CUR_CMD_ADR		R	0x0000 0000
2:0	RESERVED		R	0x0

Table 12-149. Register Call Summary for Register AQFEDEBUGCURCMDADR

BB2D Register Manual

- BB2D Register Summary: [0]
- BB2D Register Description: [1]

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Audio Back End

This chapter describes the audio back end (ABE) module.

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13.1 ABE Overview **3118**

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13.1 ABE Overview

The audio back end (ABE) module is a subsystem that manages various audio and voice uplink and downlink streams between the initiator (the Cortex™-A15 microprocessor unit [MPU], digital signal processor [DSP], or direct memory access [DMA] controller) and the peripheral physical interfaces (multichannel buffered serial port [MCBSP], digital microcontroller [DMIC], multichannel pulse density modulation [MCPDM], and multichannel audio serial port [MCASP]).

The ABE module handles the audio processing for the applications. It receives voice or audio samples from the initiator or the external audio chip (TWL6041 or other) and sends them to the peripheral interfaces or memories after processing. The ABE can perform buffering of audio samples, mix audio with a voice downstream and/or a microphone upstream (sidetone), and can apply some post-processing.

The ABE integrates the following modules:

- Peripheral physical interfaces:
  - Three MCBSP modules
  - One MCASP module
  - One DMIC module to support up to six mono and three stereo digital microphones
  - One MCPDM module to support interconnect with an external audio chip
- Audio engine (AE):
  - Performs real-time signal processing, such as sample rate conversion, filtering, equalizing, and side-tone
  - Audio traffic controller (ATC):
    - Performs data move in the ABE
    - Generates interrupt requests to the DSP and Cortex-A15 interrupt controllers (INTCs)
  - On-chip memory:
    - 64KiB of RAM; 32-bit data memory (DMEM)
    - 6KiB for coefficient memory RAM (CMEM)
    - 18KiB for sample memory RAM (SMEM)
- Local level 4 (L4) interconnect (L4_ABE) to:
  - Level 3 (L3) interconnect
  - Cortex-A15 MPU
  - DSP

  The Cortex-A15 MPU and the DSP have private access to the L4_ABE interconnect. All other initiators (DMA_SYSTEM) can access the L4_ABE interconnect only through the L3 interconnect.
- Timers:
  - Four general-purpose (GP) timers
  - One watchdog timer
- Clock and reset management: Receives clock and reset signals from the device power, reset, and clock management (PRCM) module. The audio engine operates from the DPLL_ABE, which is in the PRCM module. Clock signals from the DPLL_ABE or the DPLL_PER can supply the ABE modules. The ABE has its own hardware reset domain (AUDIO_RST).
- Power management: The ABE module is power-independent. It has its own dedicated power domain (PD_ABE) and can execute audio processing with the rest of the device in retention or off mode.
- The initiator can directly access each peripheral in the ABE when the AE is bypassed (legacy mode, for old software compatability).

Figure 13-1 is a high-level overview of the ABE.

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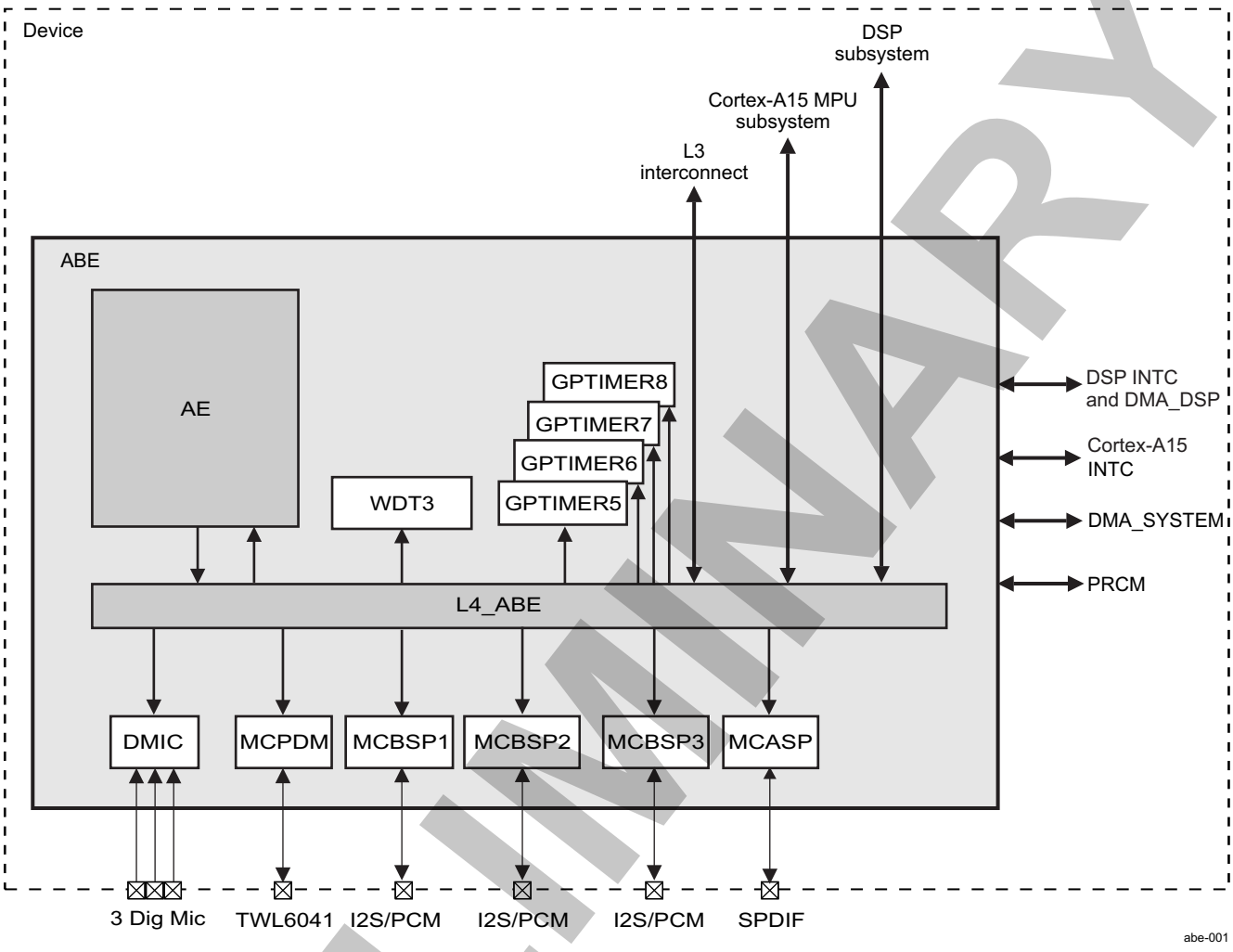
Figure 13-1. Audio Back End



13.1.1 AE Subsystem

The AE is the core of the ABE subsystem. It performs the real-time audio processing within the ABE:

- Mixing
- Muxing
- Volume control
- Smooth muting
- Sampling rate conversion
- Side-tone equalization

The AE subsystem also processes and executes all data transfers. To optimize the global processing, the ATC moves the data. An interrupt request (IRQ)/DMA controller controls system IRQs and DMA requests. Input DMA requests come from the ABE peripherals, and output DMA requests and IRQs are generated and sent to the system (Cortex-A15 MPU INTC, DSP INTC, system DMA [DMA_SYSTEM], and the DSP enhanced DMA controller [DMA_DSP]).

The AE subsystem contains:

- AE: Processes the sample in SMEM with the help of CMEM:
  - SMEM
  - CMEM

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- DMEM: Contains the audio buffer and communication circular buffer
- ATC: Transfers data between all modules in the ABE
- IRQ DMA controller

For more information about the audio engine, see the *Hardware Abstraction Layer (HAL) Addendum*.

13.1.2 Local Audio Interconnect

The ABE has its own audio local interconnect (L4_ABE), which interconnects and manages the data flow among all ABE modules.

The main features of the L4_ABE are:

- Initiator ports:
  - Cortex-A15 MPU
  - DSP
  - L3 interconnect
  - AE subsystem

  The sDMA operates with the L4_ABE interconnect through the L3 interconnect initiator port. The DMA_DSP operates with the L4_ABE interconnect through the DSP initiator port.
- Target ports:
  - AE subsystem
  - MCBSP1, MCBSP2, and MCBSP3
  - DMIC
  - MCPDM
  - MCASP
  - GPTIMER5 through GPTIMER8
  - WDT3
- 8-, 16-, or 32-bit data, single access
- 4-bit × 32-bit initiator ports for each interconnect instance
- Auto clock-gating feature
- Little-endian transaction assumed for all packing or unpacking operations
- Nonblocking architecture with fair arbitration between threads
- Target interconnect interfaces support fully synchronous and divided synchronous accesses.

For more information, see Chapter 14, *Interconnect*.

13.1.3 GP Timers

The ABE embeds four GP timers: GPTIMER5 through GPTIMER8. All GP timers have interrupts connected to the Cortex-A15 MPU, DSP, and AE subsystems.

GP timer controllers have the following functions:

- Interconnect slave interface (L4) supports:
  - 32-bit data bus width
  - 16- and 32-bit access
  - 10-bit address bus width
  - Write-Non-Posted (WNP)

  Burst is not supported.
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:

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  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- Programmable divider clock source
- Dedicated input trigger for capture mode and dedicated OUT trigger/pulse width modulation (PWM) signal
- On-the-fly read/write register
- The disconnect protocol

For more information, see Section 22.2, *General-Purpose Timers*.

13.1.4 Watchdog Timer

The ABE embeds one watchdog timer, WDT3, that generates an interrupt condition to the Cortex-A15 MPU on overflow. Application software can use an overflow to indirectly trigger a global warm reset through the PRCM module.

The main features of the WDT3 are:

- Interconnect slave interface (L4) supports:
  - 32-bit data bus width
  - 16- and 32-bit access
  - 11-bit address bus width
  - WNP

  Burst is not supported.
- Free-running 32-bit upward counter
- Programmable divider clock source
- Watchdog is reset on power up or after a warm reset and then starts counting.
- Reset or interrupt actions on a timer overflow condition and according to the watchdog timer source
- The disconnect protocol

For more information, see Section 22.3, *Watchdog Timers*.

13.1.5 Digital Microphone Controller

The DMIC allows support of up to three digital stereo microphones, which send it a pulse-density modulated stream of bits that are transferred on one period or one half-period of the clock (over-sampling clock) provided to the DMIC. Each microphone is connected directly to the TX filter decimator to extract the audio samples with a maximum of 96 db SNR with a frequency sampling set to 96 kHz.

The DMIC has the following features:

- Has six external pin connections (three data lines and three clock lines)
- Delivers one common clock (on the three clock lines) for all digital microphones
- Supports idle request and idle acknowledge protocol
- Supports stereo and mono digital microphones (up to three)
- Supoorts rising or falling edge configuration for the clock signal sampling
- Is DMIC-clock-programmable
- Has an interconnect slave interface (internal interconnect) that supports 32-bit data bus width.
- Has one DMA request capability on a programmable first in first out (FIFO) threshold
- Supports one RX FIFO (16-bit × 24-bit word depth) per microphone
- Complies with PRCM interrupts to the Cortex-A15 MPU and DSP subsystems
- Supports interconnect sample format: 32 bits (only 24 are significant)
- Supports idle request and idle acknowledge PRCM protocol

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For more information, see Section 23.7, *Digital Microphone Module*.

13.1.6 Multichannel Audio Serial Port

The MCASP is a GP audio serial port. It is useful for intercomponent (DIT) transmission. The MCASP is intended to be flexible enough so that it can connect gluelessly to audio A/D, D/A, CODEC, SPDIF transmit and recieve physical layer components and clocked frame-oriented protocols (inter-IC sound [I2S] and time division multiplexing [TDM]).

The MCASP has the following features:

- 2-interconnect slave interface supports:
  - One interconnect configuration slave interface
  - One interconnect DMA slave interface
  - 32-bit data bus width
  - 16- and 32-bit access
  - 10-bit address bus width
  - WNP

  Burst is not supported.
- Supports idle request/acknowledge protocol
- Buffers for transmit/receive operations
- DMA requests (one per direction) link with the 32-bit register
- Up to four transmit and receive channels
- Four serializers implemented
- Support of disconnect protocol

For more information, see Section 23.8, *MCASP*.

13.1.7 Multichannel Buffered Serial Port

There are three MCBSP instantiations: MCBSP1 through MCBSP3. They provide a full-duplex direct serial interface between the ABE and external devices, such as Bluetooth chips, or codecs. Because of its versatility, a MCBSP can accommodate a wide range of peripherals and clocked frame-oriented protocols (I2S, PCM, and TDM).

The recommended use per MCBSP is:

- MCBSP1: Bluetooth voice/audio data
- MCBSP2: Digital baseband (DBB) voice data
- MCBSP3: MIDI FM data

The MCBSP has the following features:

- Interconnect slave interface (internal interconnect) supports:
  - 32-bit data bus width
  - 8-, 16-, and 32- bit access
  - 10-bit address bus width
  - WNP

  Burst is not supported.
- Buffers for transmit/receive operations: 128/128 32-bit words (MCBSP1, 2, 3)
- Interrupts configurable in legacy mode (two requests) or PRCM module-compliant (one request)
- DMA requests (one per direction) triggered with programmable FIFO thresholds
- Multidrop support
- Serial interface description
- Four-pin configuration (MCBSP1, 2, 3)

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- Full-duplex communication
- Multichannel selection modes
- Support to enable or block transfers in each channel
- Up to 128 channels for transmission and for reception
- Supported protocols
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected A/D and D/A devices:
  - I2S-compliant devices
  - TDM bus devices
  - PCM devices
- A wide selection of data sizes: 8, 12, 16, 20, 24, and 32 bits
- Supports idle request/acknowledge protocol
- Clock generation support:
  - Independent clocking and framing for reception and transmission up to 48 MHz
  - Support for external generation of clock signals and frame-synchronization (frame-sync) signals
  - A programmable sample rate generator for internal generation and control of clock signals and frame-sync signals
- Support of disconnect protocol

For a complete description, see Section 23.5, *Multichannel Buffered Serial Port (MCBSP)*.

13.1.8 Multichannel Pulse Density Modulation Module

The MCPDM is a proprietary interface based on multichannel pulse density modulation. The module consists of five downlinks and three uplinks. Two other uplink channels are reserved for status communication.

The MCPDM has the following features:

- Interconnect slave interface (L4_ABE internal interconnect) supports:
  - 32-bit data bus width
  - 10-bit address bus width
  - WNP

  Burst is not supported.
- Full-duplex communication:
  - Five audio downstream channels
  - Three audio upstream channels
- RX/TX FIFO operations: 32-bit words per channel
- Complies with PRCM module interrupts:
  - One to the MPU subsystem
  - One to the DSP subsystem
- DMA requests (one per direction) triggered with programmable FIFO thresholds; depending on the FIFO implementation, one request per channel or one per direction
- Decimation filter for embedded uplink paths (five paths if two status paths)
- Oversampling for embedded uplinks (five paths)
- Sigma-delta for embedded downlinks (three paths)
- Deserializers for the two status upstream channels
- Support of disconnect protocol

For more information, see Section 23.6, *Multichannel PDM Controller*.

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Interconnect

This chapter describes the device interconnect.

NOTE: The level 3 (L3) interconnect is an instantiation of the NoC interconnect from Arteris, Inc. Arteris is a registered trademark of Arteris, Inc.

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NoC is an abbreviation for Network On Chip.

NOTE: The level 4 (L4) interconnects are instantiations of the Sonics3220™ interconnect from Sonics, Inc.

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SLX is an abbreviation for SonicsLX®.

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14.1 Interconnect Overview

14.1.1 Terminology

The following terminology is critical to understanding the interconnect:

- Initiator: Module able to initiate read and write requests to the chip interconnect (typically: processors, direct memory access (DMA), and so forth).
- Target: Unlike an initiator, a target module cannot generate read/write requests to the chip interconnect, but it can respond to these requests. However, it may generate interrupts or a DMA request to the system (typically: peripherals and memory controllers).

NOTE: A module can have several separate ports; therefore, a module can be an initiator and a target.

- Agent: Each connection of one module to one interconnect is done using an agent, which is an adaptation (sometimes configurable) between the module and the interconnect. A target module is connected by a target agent (TA), and an initiator module is connected by an initiator agent (IA).
- Interconnect: The decoding, routing, and arbitration logic that enables the connection between multiple initiator modules and multiple target modules connected on it
- Register target (RT): Special TA used to access the interconnect internal configuration registers
- Data-flow signal: Any signal that is part of a clearly identified transfer or data flow (typically: command, address, byte enables, and so forth). Signal behavior is defined by the protocol semantics.
- Sideband signal: Any signal whose behavior is not associated to a precise transaction or data flow
- Out-of-band error: Any signal whose behavior is associated to a device error-reporting scheme, as opposed to in-band errors

NOTE: Interrupt requests and DMA requests are not routed by the interconnect in the device.

- Firewall: A programmable feature integrated in a TA or level 4 (L4) interconnect to prevent unauthorized access to or from a module. A firewall can be configured using three criteria:
  - Initiator requesting access
  - Address space access
  - Type of access
- ConnID: Any transaction in the system interconnect is tagged by an in-band qualifier ConnID, which uniquely identifies the initiator at a given interconnect point. A ConnID is transmitted in band with the request and is used for firewall and error-logging mechanism.
- Firewall comparison mechanism: A comparison made in the firewall between access in-band qualifiers and access permissions that are programmed in the firewall configuration registers. If the comparison is successful, access is allowed; otherwise, access is denied.
- MCmd qualifier: Command bus that indicates the type of transfer requested. Table 14-1 lists the commands encoded. For information specific to L3_MAIN interconnect error logging, see Table 14-27.

Table 14-1. MCmd Qualifier Description

MCmd[2:0]	Transaction Type
0 0 0	Idle
0 0 1	Write
0 1 0	Read
0 1 1	ReadEx
1 0 0	Read link
1 0 1	Write nonposted
1 1 0	Write conditional
1 1 1	Write broadcast

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- MReqInfo qualifier: Four MReqInfo qualifiers describe the access during the use of the firewall comparison mechanism, as described in Table 14-2.

Table 14-2. MReqInfo Qualifier Description

Qualifiers	Description
MReqType	0: Data access
	1: Opcode fetch
MReqSupervisor	0: User mode
	1: Supervisor mode
MReqDebug	0: Functional access
	1: Debug access

- Register that configures the combination of the MReqInfo, allowing access permission to the target module (TM) based on the MReqInfo in-band qualifier values
- SError: Target that indicates an error condition to the initiator
- SResp qualifier: Response from the target to the initiator concerning the transaction, as described in Table 14-3

Table 14-3. SResp Qualifier Description

SResp[1:0]	Description
0 0	No response
0 1	Data valid/accept
1 0	Not used
1 1	Error

14.1.2 Architecture Overview

The device memory hierarchy includes four levels:

- Level 1 (L1) is internal to the CPUs. The L1 interconnect concerns data exchange with the internal L1 cache memory subsystem, and it is the closest memory to the microprocessor unit (MPU) core and the IVA core.
- Level 2 (L2) is included in the IPU subsystem and the MPU subsystem.
- The chip-level interconnect consists of one L3 interconnect and three L4 interconnects. The chip-level interconnect enables communication among the modules and subsystems in the device.

Figure 14-1 shows an overview of the L3 and L4 interconnect architecture.

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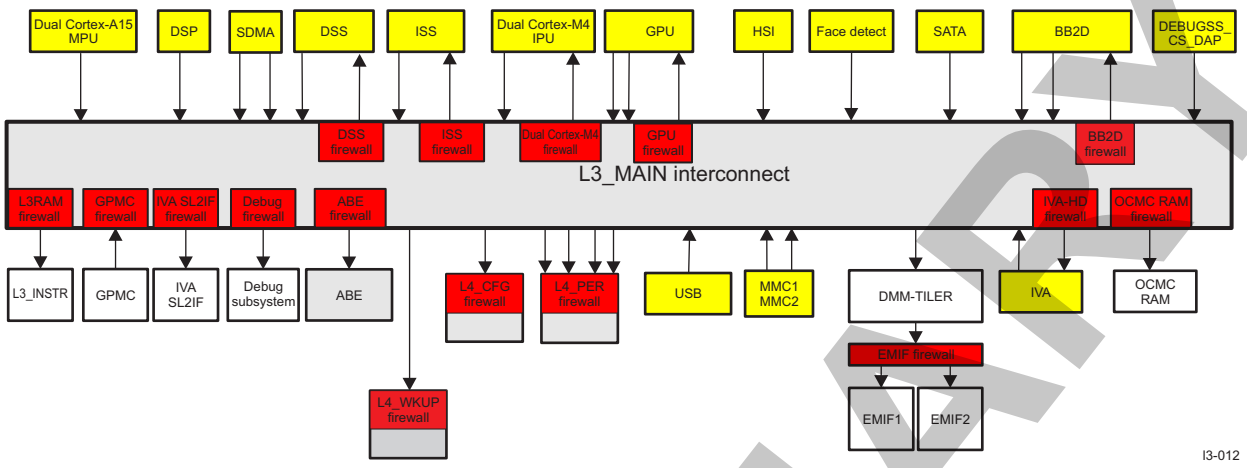
Figure 14-1. Interconnect Overview



- L3_MAIN handles many types of data transfers, especially exchanges with system-on-chip/external memories. L3 transfers data with a maximum width of 128 bits from the initiator to the target. The L3_MAIN interconnect is a little-endian platform
- The L4 is composed of the following:
  - L4_CFG: Includes the majority of the configuration interface for L3 system modules and peripheral interconnect
  - L4_PER: Includes the main peripherals that require system direct memory access (sDMA) access
  - L4_WKUP: Includes peripherals attached to the WKUP power domain

Modules are connected to the interconnect through an IA for the initiator module and a TA for target modules. Each module or subsystem connection is statically configured to tune the access, depending on the characteristics of the module.

To unauthorize a module or L4 interconnect access, some TAs include configurable firewalls (FWs). A firewall restricts or filters the accesses allowed to an initiator according to different access criteria. Software usually configures the firewalls.

The default settings of the L3_MAIN and L4 interconnect are fully functional; they enable all possible functional data paths and a minimal default protection setting. However, the interconnect parameters can be modified to fit user expectations. Interconnect parameters can also be modified by the ROM code for HS/EMU devices.

14.1.3 Module Distribution

IAs and TAs provide the interface to connect the different modules and the interconnect.

Table 14-4 through Table 14-11 list the device modules, subsystems, and associated agents. The agents are listed for each interconnect domain:

- L3_MAIN initiator (master network interface units (NIU) - MN) and target (slave NIUs - SN) agents
- L4_PER initiator and target agents
- L4_CFG initiator and target agents
- L4_WKUP initiator and target agents

14.1.3.1 L3_MAIN Interconnect Module Distribution

Table 14-4 and Table 14-5 list the IAs and TAs, respectively, of the L3_MAIN interconnect.

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Table 14-4. Master NIUs

Master NIU	Description
MPU_INIT	Cortex™ A15 MPU subsystem
DSP_INIT	DSP subsystem
IPU_INIT	IPU subsystem
IVA_INIT	Video accelerator subsystem
MMC1_INIT, MMC2_INIT	Multimedia controller
GPU_P1_INIT	3D graphics accelerator port 1
GPU_P2_INIT	3D graphics accelerator port 2
DSS_INIT	Display subsystem
ISS_INIT	Imaging accelerator subsystem
FDIF_INIT	Face detection module
DEBUG_CS_DAP_INIT	JTAG®/emulation access to system resources
SDMA_RD_INIT	System DMA read
SDMA_WR_INIT	System DMA write
HSI_INIT	HSI module
BB2D_P1_INIT	2D graphics accelerator port 1
BB2D_P2_INIT	2D graphics accelerator port 2
USB_HOST_HS_INIT	Multiport USB host controller
USB_OTG_SS_INIT	USB on-the-go controller
SATA_INIT	SATA initiator port

Table 14-5. Slave NIUs

Slave NIU	Description
OCMC_RAM_TARG	On-chip memory controller target port
GPMC_TARG	General-purpose memory controller target port
DMM_P1_TARG	Dynamic memory management target port 1
DMM_P2_TARG	Dynamic memory management target port 2
GPU_TARG	3D graphics accelerator target port
BB2D_TARG	2D graphics accelerator target port
ISS_TARG	Imaging accelerator target port
IVA_CONFIG_TARG	Video accelerator subsystem configuration
IVA_SL2IF_TARG	Video accelerator subsystem shared memory
IPU_TARG	Dual Cortex-M4 subsystem
DSS_TARG	Display subsystem
ABE_TARG	Audio back end (ABE) target port
L3_INSTR_TARG	L3 instrumentation target port
L4_CFG_TARG	L4 interconnect configuration
L4_PER0/1/2/3_TARG	L4 interconnect peripherals
L4_WKUP_TARG	L4 interconnec wakeup
DEBUGSS_CT_TBR_TARG	Debug subsystem target port

14.1.3.2 L4 Interconnect Module Distribution

IAs and TAs provide the interface to connect the different modules to their associated interconnect.

Table 14-6 through Table 14-11 list all modules and subsystems with their associated agents. The agents are listed for each L4 interconnect domain.

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14.1.3.2.1 L4_PER Interconnect Agents

The L4_PER interconnect handles transfers only to peripherals in the PER power domain. Table 14-6 lists the PER TAs.

Table 14-6. L4_PER TAs

Module Target Name	Description
UART1_TARG	UART port 1 module
UART2_TARG	UART port 2 module
UART3_TARG	UARTport 3 module
UART4_TARG	UART port 4 module
UART5_TARG	UART port 5 module
UART6_TARG	UART port 6 module
TIMER2_TARG	General-purpose TIMER2 module
TIMER3_TARG	General-purpose TIMER3 module
TIMER4_TARG	General-purpose TIMER4 module
TIMER9_TARG	Genera-purposel TIMER9 module
TIMER10_TARG	General-purpose TIMER10 module
TIMER11_TARG	General-purpose TIMER11 module
GPIO2_TARG	General-purpose input/output 2 (GPIO2) module
GPIO3_TARG	GPIO3 module
GPIO4_TARG	GPIO4 module
GPIO5_TARG	GPIO5 module
GPIO6_TARG	GPIO6 module
GPIO7_TARG	GPIO7 module
GPIO8_TARG	GPIO8 module
I2C1_TARG	Multimaster I2C1 module
I2C2_TARG	Multimaster I2C2 module
I2C3_TARG	Multimaster I2C3 module
I2C4_TARG	Multimaster I2C4 module
I2C5_TARG	Multimaster I2C5 module
MCSPI1_TARG	Multichannel serial port interface controller 1 module
MCSPI2_TARG	Multichannel serial port interface controller 2 module
MCSPI3_TARG	Multichannel serial port interface controller 3 module
MCSPI4_TARG	Multichannel serial port interface controller 4 module
MMC1_TARG	MMC1 module
MMC2_TARG	MMC2 module
MMC3_TARG	MMC3 module
MMC4_TARG	MMC4 module
MMC5_TARG	MMC5 module
ELM_TARG	Error location module
HDQ1W_TARG	HDQ 1-Wire® serial interface controller

Four ports communicate between the L3_MAIN interconnect and the L4_PER interconnect to allow the L3_MAIN initiators to access the L4_PER targets. Table 14-7 lists the L4_PER initiator TAs.

For the list of initiators authorized to access the L4_PER peripherals, see Section 14.2.3.2.2, *Connectivity Matrix*.

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Table 14-7. L4_PER IAs

Module Initiator Name	Description
L3_MAIN_P0_INIT	L3 sDMA RD interconnect port
L3_MAIN_P1_INIT	L3 sDMA WR interconnect port
L3_MAIN_P2_INIT	L3 MPU susbystem interconnect port
L3_MAIN_P3_INIT	L3 others interconnect port

14.1.3.2.2 L4_CFG Interconnect Agents

The L4 CFG interconnect handles only transfers to peripherals in the CORE power domain. Table 14-8 lists the TAs.

Table 14-8. L4_CFG TAs

Module Target Name	Description
CTRL_MODULE_CORE_TARG	Control module core
CM_CORE_AON_TARG	CORE_AON module
DMA_SYSTEM_TARG	System DMA module
HSI_TARG	High-speed synchronous serial interface module
USB_TLL_HS_TARG	High-speed USB_TLL module
USB_OTG_SS_TARG	USB_OTG module
USB_HOST_HS_TARG	High-Speed Multi-port USB host controller module
SMARTREFLEX_CORE_TARG	SmartReflex core module
SMARTREFLEX_MM_TARG	SmartReflex MM module
SMARTREFLEX_MPU_TARG	SmartReflex MPU module
OCP2SCP1_TARG	OCP to SCP1 module
CM_CORE_TARG	CM_CORE module
DSP_TARG	DSP module
MAILBOX_TARG	MAILBOX module
SPINLOCK_TARG	SPINLOCK module
IVA_FW_TARG	IVA firewall
MPU_NTTP_FW_TARG	MPU NTTP firewall
OCMC_RAM_FW_TARG	OCMC_RAM firewall
EMIF_OCP_FW_TARG	EMIF L3 firewall
GPMC_FW_TARG	GPMC firewall
ISS_FW_TARG	ISS firewall
GPU_FW_TARG	GPU firewall
IPU_FW_TARG	IPU firewall
IVA_SL2IF_FW_TARG	IVA SL2 interface firewall
DEBUGSS_CT_TBR_FW_TARG	Debug subsystem CT TBR firewall
L3_INSTR_FW_TARG	L3 instruction firewall
ABE_FW_TARG	ABE firewall
OCP_WP_NOC_TARG	OCP_WP firewall
DSS_FW_TARG	Display subsystem firewall
FDIF_TARG	Face detection interface module
SATA_TARG	SATA module
BB2D_TARG	2D graphics accelerator module
OCP2SCP3_TARG	OCP-to-SCP3 module

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L3_MAIN_INIT communicates between the L3_MAIN interconnect and the L4_CFG interconnect to allow the L3_MAIN initiators to access the L4_CFG targets (see Table 14-9).

For the list of initiators authorized to access the L4_CFG peripherals, see Section 14.2.3.2.2, *Connectivity Matrix*.

Table 14-9. L4_CFG IAs

Module Initiator Name	Description
L3_MAIN_INIT	L3_MAIN interconnect port

14.1.3.2.3 L4_WKUP Interconnect Agents

The L4_WKUP interconnect handles transfers only to peripherals in the WKUP power domain. Table 14-10 lists the TAs. Table 14-11 lists the L4_WKUP IAs.

Table 14-10. L4_WKUP TAs

Module Target Name	Description
GPIO1_TARG	GPIO1 module
32KTIMER_TARG	32-kHz timer module
SAR_RAM_TARG	Save-and-restore RAM
KEYBOARD_TARG	Keyboard module
CTRL_MODULE_WKUP_TARG	Control module WKUP module
PRM_TARG	Power reset management module
SCRM_TARG	System clock and reset management module
WD_TIMER2_TARG	Watchdog TIMER2 module
TIMER1_TARG	General-purpose TIMER1 module
SCRM_TARG	System clock and reset manager module

Table 14-11. L4_WKUP IAs

Module Initiator Name	Description
L3_MAIN_INIT	L4_CFG interconnect port

14.1.4 Connectivity Matrix

Figure 14-2 lists the functional paths between the L3_MAIN interconnect initiator modules and the L3_MAIN and L4 TAs. In this matrix:

- a cell is green when a functional path exists.
- a cell is red when a functional path does not exist.

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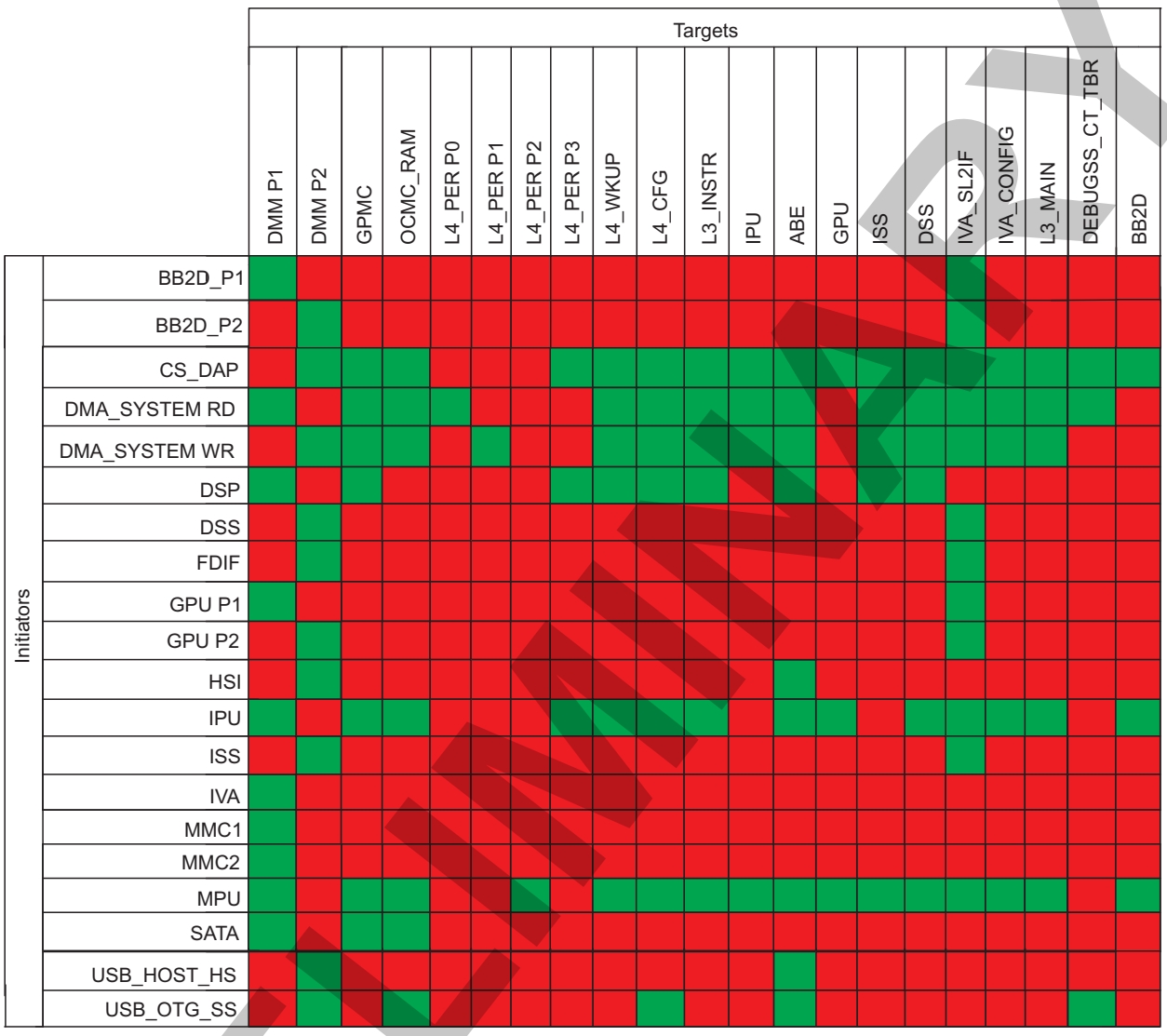
Figure 14-2. Connectivity Matrix



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14.2 L3 Interconnect

This section describes the L3 interconnect and its components. With the exception of register points, each component includes functions for the request and response networks.

14.2.1 L3_MAIN Interconnect Overview

The L3_MAIN interconnect links cores in a flexible topology that couples low power with high performance. Innovative physical structures and advanced protocols ensure bandwidth and latency to individual IP cores, providing dedicated connections between IP cores and logical connections over a shared interconnect.

The main features of the L3_MAIN interconnects are:

- NIUs: Master NIUs for the IAs and slave NIUs for the TAs
- A partially depleted cross-bar exchange network
- A special internal slave NIU for accessing L3_MAIN interconnect configuration registers
- QoS management for real-time hardware operators, while maintaining optimal memory latency for CPU access to memory resources
- True little-endian platform
- Transaction errors tracking and logging registers
- All signaling support for chip-level power-management infrastructure
- One interrupt line signaling transaction error
- One interrupt line for reporting satistical events on the L3_MAIN interconnect

Figure 14-3 shows an overview of the L3 interconnect and the peripherals attached to it.

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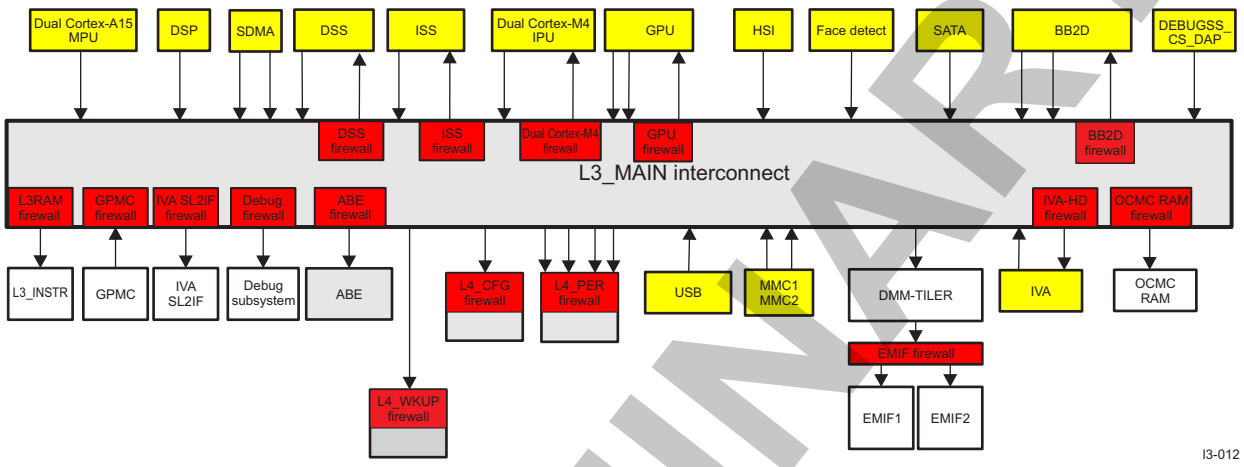
Figure 14-3. L3_MAIN Interconnect Overview



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14.2.2 L3_MAIN Interconnect Integration

Table 14-12 through Table 14-14 summarize the integration of the module in the device.

Table 14-12. Integration Attributes

Module Instance	Attributes
	Power Domain
L3_MAIN	PD_CORE

Table 14-13. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L3_MAIN	L3_CLK2	L3MAIN2_L3_GICLK	PRCM	Functional and interface clock
	L3_CLK1	L3MAIN1_L3_GICLK	PRCM	Functional and interface clock
	L3_CLK3	L3INSTR_L3_GICLK	PRCM	Functional and interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L3_MAIN	L3_CORE_RET_RST	CORE_PWRON_RET_RST	PRCM	Reset of L3_PER interconnect retention registers
	L3_CORE_RST	CORE_RST	PRCM	Reset of L3_PER interconnect

Table 14-14. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
L3_MAIN	L3_MAIN_IRQ_DBG_ERR	MPU_IRQ_9	Cortex-A15 INTC	Interrupt to the Cortex-A15
	L3_MAIN_IRQ_APP_ERR	DSP_IRQ_84	DSP INTC	Interrupt to the digital signal processor (DSP)
	L3_MAIN_IRQ_APP_ERR	MPU_IRQ_10	Cortex-A15 INTC	Interrupt to the Cortex-A15
	L3_MAIN_IRQ_START_ALARM	MPU_IRQ_16	Cortex-A15 INTC	Interrupt to the Cortex-A15
	L3_MAIN_IRQ_APP_ERR	IPU_IRQ_46	IPU INTC	Interrupt to the IPU

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14.2.3 L3_MAIN Interconnect Functional Description

14.2.3.1 Module Use in L3_MAIN Interconnect

The L3_MAIN interconnect network components have ConnID values for each master NIU or slave NIU. The ID uniquely identifies the master NIU or the slave NIU for an interconnect transfer. The interconnect uses ConnIDs for a number of purposes, including the following:

- Slave NIUs for error logging
- Power disconnect slave NIU for error logging
- FLAGMUX to mask interrupts: Three, one for each clock domain
- STATCOLL for configuring and monitoring: The STATCOLL components compute the traffic statistics within a user-defined window and periodically report to the user through the debug interface.
- Bandwidth regulator for configuration
- Some rate adapters for configuration of throughput ratio

14.2.3.2 Module Distribution

Master NIUs and slave NIUs provide the interface to connect the different modules to their associated interconnect.

Table 14-15 and Table 14-16 list all the modules and subsystems with their associated agents. The agents are listed for each L3_MAIN interconnect domain.

14.2.3.2.1 L3_MAIN Interconnect Agents

Any initiator or target core is connected to the L3_MAIN interconnect through an NIU. NIUs act as entry points to the L3_MAIN interconnect, and also include various programming registers. Table 14-15 lists the supported master NIU ports.

Table 14-15. Master NIUs

Master NIU	Description
MPU_INIT	Cortex-A15 microprocessor subsystem unit
DSP_INIT	DSP subsystem unit
IPU_INIT	IPU subsystem
IVA_INIT	Video accelerator subsystem
MMC1/2_INIT	Multimedia controller
GPU_P1_INIT	3D graphics accelerator port 1
GPU_P2_INIT	3D graphics accelerator port 2
DSS_INIT	Display subsystem
ISS_INIT	Imaging accelerator subsystem
FDIF_INIT	Face detection module
DEBUG_CS_DAP_INIT	JTAG or emulation access to system resources
SDMA_RD_INIT	System DMA read
SDMA_WR_INIT	System DMA write
HSI_INIT	HSI module
BB2D_P1_INIT	2D graphics accelerator port 1
BB2D_P2_INIT	2D graphics accelerator port 2
USB_HOST_HS_INIT	Multiport USB host controller
USB_OTG_SS_INIT	USB on-the-go controller
SATA_INIT	SATA initiator port

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Table 14-16 lists the supported slave NIU ports.

Table 14-16. Slave NIUs

Slave NIU	Description
OCMC_RAM_TARG	On-chip memory controller target port
GPMC_TARG	General-purpose memory controller target port
DMM_P1_TARG	Dynamic memory management target port 1
DMM_P2_TARG	Dynamic memory management target port 2
GPU_TARG	3D graphics accelerator target port
BB2D_TARG	2D graphics accelerator target port
ISS_TARG	Imaging accelerator target port
IVA_CONFIG_TARG	Video accelerator subsystem configuration
IVA_SL2IF_TARG	Video accelerator subsystem shared memory
IPU_TARG	Dual Cortex-M4 subsystem
DSS_TARG	Display subsystem
ABE_TARG	ABE target port
L3_INSTR_TARG	L3 instrumentation target port
L4_CFG_TARG	L4 interconnect configuration
L4_PER0/1/2/3_TARG	L4 interconnect peripherals
L4_WKUP_TARG	L4 interconnec wakeup
DEBUGSS_CT_TBR_TARG	Debug subsystem target port

14.2.3.2.2 L3_MAIN Connectivity Matrix

The L3 interconnect is divided into three clock domains:

- L3_CLK1: Low-power domain
- L3_CLK2: Peripherals and multimedia
- L3_CLK3: Instrumentation (debug)

Each clock element is implemented in a different clock domain.

14.2.3.2.2.1 Clock Domain Mapping of the L3_MAIN Interconnect Modules

Each clock domain (CLK1, CLK2, and CLK3) has it own host, flag mux, slave NIUs, and bandwidth regulators. Table 14-17 lists the relationships between these domains and these elements.

Table 14-17. L3_MAIN Clock Domains and Elements

Clock Domain	Elements
L3_CLK1	HOST_CLK1
	DMM1/2_TARG
	ABE_TARG
	L4_CFG_TARG
	FLAGMUX_CLK1
	FLAGMUX_CLK1_TIMEOUT
	CLK1_PWR_DISC_TARG_CLK2
	RATE_ADAPT_ABE
	L4_WKUP_TARG

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Table 14-17. L3_MAIN Clock Domains and Elements (continued)

Clock Domain	Elements
L3_CLK2	HOST_CLK2
	GPMC_TARG
	OCM_RAM_TARG
	DSS_TARG
	BB2D_TARG
	ISS_TARG
	IPU_TARG
	GPU_TARG
	IVA_CONFIG_TARG
	IVA_SL2IF_TARG
	L4_PER0/1/2/3_TARG
	FLAGMUX_CLK2
	FLAGMUX_CLK2_TIMEOUT
	CLK2_PWR_DISC_TARG_CLK1
	RATE_ADAPT_GPMC
	IVA_BW_REGULATOR
	GPU_P1_BW_REGULATOR
	GPU_P2_BW_REGULATOR
	BB2D_P1_BW_REGULATOR
	BB2D_P2_BW_REGULATOR
	BB2D_P1_BW_LIMITER
	BB2D_P2_BW_LIMITER
	HOST_CLK3
L3_INSTR_TARG	L3_CLK3
FLAGMUX_CLK3	
FLAGMUX_CLK3_TIMEOUT	
DEBUGSS_CT_TBR_TARG	
FLAGMUX_STATCOLL	
STATCOLL_SDRAM	
STATCOLL_LAT0	
STATCOLL_LAT1	

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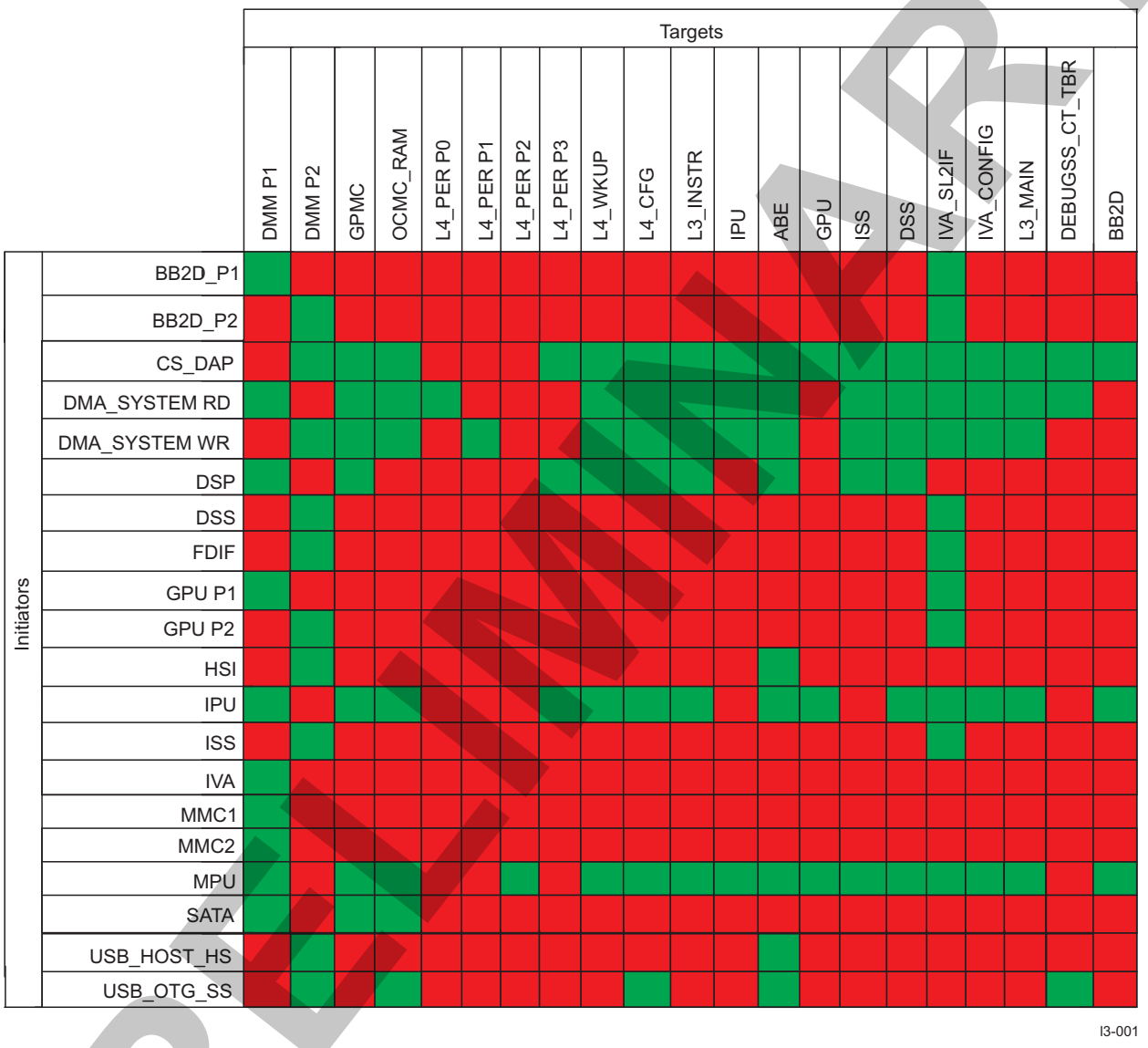
Figure 14-4 lists the functional paths between the L3_MAIN master NIUs and the L3_MAIN and L4 slave NIU agents. In this matrix:

- a cell is green when a functional path exists.
- a cell is red when a functional path does not exist.

Figure 14-4. L3_MAIN Connectivity Matrix



14.2.3.2.3 Master NIU Identification

A master NIU ID (ConnID) is assigned to every module in the device. The ID uniquely identifies the master NIU for an interconnect transfer (see Table 14-18). The interconnect uses ConnID values for a number of purposes, including:

- Master source identification for the protection mechanism
- Response route generation
- Firewall error logging
- L3_MAIN interconnect error logging

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Table 14-18. ConnID Values

ConnID	Master NIU
0x0	Cortex-A15 MPU
0x4	DAP
0x8	DSP
0xC	IVA
0x10	ISS
0x11	IPU subsytem
0x12	Face detect
0x14	sDMA_rd
0x15	sDMA_wr
0x18	GPU_P1
0x19	GPU_P2
0x1A	BB2D_P1
0x1B	BB2D_P2
0x1C	DSS
0x24	HSI
0x28	MMC1
0x29	MMC2
0x2A	SATA
0x2C	Reserved
0x30	HSUSBHOSTUSB_HOST_HS
0x33	HSUSBOTGUSB_OTG_SS
0x34	Reserved
0x38	PERF_PROBE

14.2.3.3 Bandwidth Regulators

The bandwidth regulators prevent master NIUs from consuming too much bandwidth of a link, or a slave NIU that is shared between several data flows: packets are then transported at a slower rate. The value of a bandwidth can be programmed in the bandwidth regulator. When the bandwidth is below the programmed value, the pressure bit is set to 1, giving priority to this master. When the bandwidth is above the programmed value, the pressure bit is set to 0 and the concerned master has the same weight as others.

A counter is used to store the sum of data lengths (in bytes) of each packet passing through the bandwidth regulator, and a value equal to the expected bandwidth is subtracted from the counter at each clock cycle. The value of the counter is compared to a programmable threshold (called Watermark), and this comparison determines whether the packet is processed with high pressure for minimum latency or low pressure for best effort processing.

The bandwidth regulator monitors the traffic using open connections between the initiators and the targets. If there is insufficient bandwidth allocated to the connection, the bandwidth regulator can increase the pressure on connections. Generally, the connection is a dataflow between master and slave NIUs. In some cases, the bandwidth regulator is attached to the master and monitors single dataflow to a target (single connection).

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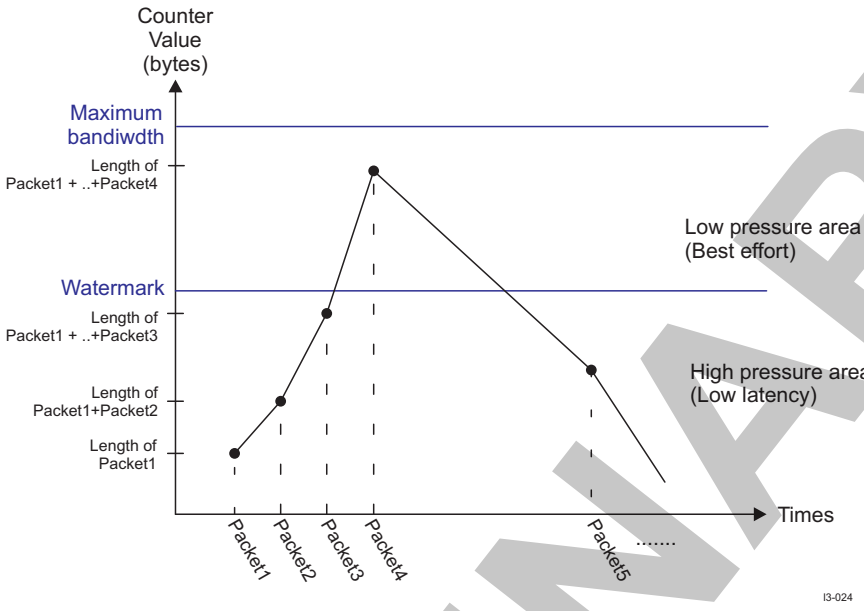
Figure 14-5. Bandwidth Regulator Pressure Settings



When Counter Value (bytes) falls below Watermark, the pressure bit is assigned to 1

The bandwidth regulator effective resolution is set to 16.6 MBps. The maximum average bandwidth (max watermark value) computed in a moving window is set to up to 4096 bytes of payload. These settings are implemented by hardware.

The following is an example of bandwidth regulator settings:

The bandwidth regulator is set to run at 200 MHz and the application requires an expected bandwidth of 165.888 MBps (±5 MBps), computed through a moving window of 5 µs (1000 cycles). To attribute high pressure on all packets requests, the watermark could be set to the maximum bandwidth needed in the 5-µs window.

Considering the example, the settings of the bandwidth regulator are:

- L3_BW_R_WATERMARK[11:0] WATERMARK = moving window × expected bandwidth = 829.44 bytes = 0x33D
- L3_BW_R_BANDWIDTH[15:0] BANDWIDTH = 165.888 MBps / effective resolution = 13,271 = 0xD

The bandwidth registers regulate the packet flow by applying flow control on the RX port, thus ensuring that the traffic does not exceed the allocated bandwidth. The next packet is sent only when an internal timer expires. The registers in this group are:

- L3_BW_REGULATOR_WATERMARK: Gives the amount of data allowed to exceed the average bandwidth during a short time period
- L3_BW_REGULATOR_PRESS: Describes the pressure applied to outgoing packets
- L3_BW_REGULATOR_CLEARHISTORY: Resets the traffic counter when set to 1. This register is used after an update in the L3_BW_REGULATOR_BANDWIDTH and L3_BW_REGULATOR_WATERMARK registers (see Section 14.2.5.1.6, *L3 BW Regulator Register Summary and Description*).

Bandwidth regulators are mainly used to give priority to the following masters: IVA, GPU_P1/P2 and BB2D_P1/P2.

As far as DSS and ISS real-time traffic is concerned, its priority is given by internal signal (outputted by the corresponding module). The L3_MAIN interconnect uses this signal to control its internal arbitration.

14.2.3.4 Bandwidth Limiters

The bandwidth limiter is added to control the bandwidth of the BB2D module. This prevents a large number of RD requests being processed together, thus avoiding a large number of RD responses.

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The bandwidth limiter regulates the packet flow in the L3_MAIN interconnect by applying flow control when a user-defined bandwidth limit is reached. The next packet is served only after an internal timer expires, thus ensuring that traffic does not exceed the allocated bandwidth.

The registers in this group are:

- L3_BW_LIMITER_WATERMARK_0: Gives the amount of data allowed to exceed the average bandwidth during a short time period. To set the actual watermark to n bytes, the register must be set to n + 1.
- L3_BW_LIMITER_CLEARHISTORY: Resets the traffic counter when set to 1.
- L3_BW_LIMITER_BANDWIDTH_FRACTIONAL and L3_BW_LIMITER_BANDWIDTH_INTEGER: These two registers are used to set the average payload bandwidth.

NOTE: The bandidth limiter is configured to be transparent at reset.

14.2.3.5 Flag Muxing

The flag mux generator collects information such as errors and interrupts from slave NIUs and the interconnect firewall. The result signals are then sent to the MPU interrupt controller (INTC) without interfering with the interconnect traffic. Using the L3_FLAGMUX_MASK registers can prevent the flag mux from seeing certain events.

The unit has a standard COREREG register for identification of the attached core type. The L3_FLAGMUX_STDHOSTHDR_VERSIONREG register identifies the characteristics of the attached core. Use unit-specific registers (MASK bit 0 or bit 1 of the flag inputs, and L3_FLAGMUX_REGERR bit 0 or bit 1) to read the input errors. Each register is dedicated to reporting the bit corresponding to the register number; for example, L3_FLAGMUX_REGERR0 reports on bit 0, and L3_FLAGMUX_REGERR1 reports on bit 1. Any given L3_FLAGMUX_REGERR register reports the same bit for all flag source inputs (see Table 14-164).

14.2.3.5.1 Flag Mux Time-out

If a target does not respond after a fixed number of clock cycles, an error time-out flag is generated, in case it is enabled. The value of the flag is always 3 if a time-out error is present.

To enable time-out for each target, set the L3_FLAGMUX_TIMEOUT_MASK0 register to 1. See Table 14-19.

Table 14-19. L3 Time-out Flag Mapping

	Flag Mux Input	Source
CLK1 Time-out FlagMux	0	L4_WKUP_TARG
	1	L4_CFG_TARG
	2	ABE_TARG
	3	DMM_P2_TARG
	4	DMM_P1_TARG

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Table 14-19. L3 Time-out Flag Mapping (continued)

	Flag Mux Input	Source
CLK2 Time-out FlagMux	0	IVA_SL2IF
	1	Reserved
	2	GPU
	3	OCMC_RAM
	5	L4_PER_P3
	6	Reserved
	7	Reserved
	8	L4_PER_P2
	9	L4_PER_P1
	10	L4_PER_P0
	11	IVA_CONFIG
	12	ISS
	13	GPMC
	14	Reserved
	15	Reserved
	16	IPU
	17	BB2D
	18	DSS
CLK3 Time-out FlagMux	0	03_INSTR
	1	DEBUGSS_CT_TBR

For example, to enable all targets in CLK1, write 0x1F in L3_FLAGMUX_TIMEOUT_MASK0. To enable only OCMC_RAM, write 0x8 in L3_FLAGMUX_TIMEOUT_MASK0 (for instance, CLK2_FLAGMUX_CLK2).

If an error time-out occurs, read the L3_FLAGMUX_TIMEOUT_REGERR0 register to check which target does not respond according to Table 14-19.

14.2.3.6 Rate Adapter Generators

The rate adapter generators give the option to configure the L3 interconnect to work in auto-adaptive mode or pipeline mode for sending the packets by using the CNF register. The rate adapter can be configured in store-and-forward mode when the throughput ratio is not well defined, or in auto-adaptive mode when the throughput ratio is predictable. Because the ratios are predictable in the L3_MAIN interconnect, the rate adapters are always used in auto-adaptive mode, except for the rate adapter on the L4_CFG and L4_ ABE responses path. L4_CFG and L4_ABE are configured in store-and-forward mode. The main rate adapt registers are:

- CLK1_RATE_ADAPT_RESP_32TO128_CLK1: Removes WAIT cycles on responses coming from ABE, L4_CFG, and power disconnect to host
- CLK2_RATE_ADAPT_RESP_32TO128_CLK2: Removes WAIT cycles on responses coming from CLK2 32-bit slaves (see Table 14-217)

14.2.3.7 Statistic Collectors Group

Statistic collectors are internal masters that share the same master address as the master NIUs. These components compute the traffic statistics within a defined window and periodically report through the DEBUG interface. The key features of the statistic collector are:

- Nonintrusive monitoring
- Programmable filters and counters
- Collects results at a programmable time interval

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Event detectors are programmed through the L3_STCOL_REQEVT and L3_STCOL_RSPEVT configuration registers for request and response ports, respectively. The following events can be identified:

- Word transfer
- WAIT cycles
- Flow control
- Payload transfers
- Latency measurements

Performance monitoring is enabled through the L3_STCOL_EN register. The L3_STCOL_SOFTEN register enables software to monitor the performance. Event muxes are programmed through the L3_STCOL_EVTMUX_SEL0 configuration register, which determines which port will be monitored by a filter configured by the filter registers (see Table 14-318).

Filters are programmed through the Table 14-318 configuration register, along with additional selection criteria programmed through the mask/match registers (see Table 14-227). A filter can be configured to accept or reject:

- Read operations
- Write operations
- Errors
- Addresses

Filter operation is programmed through the L3_STCOL_OP registers (see Table 14-227).

14.2.3.8 L3_MAIN Protection and Firewalls

Device protection relies on L3 firewalls and their configuration.

14.2.3.8.1 L3_MAIN Firewall Reset

The values of L3_MAIN firewall registers on reset are tied in hardware or exported from the control module registers.

Values exported from the control module are intended to give defined rights to the firewalls at reset and thus ensure the content after going out of reset. Because the control module consists of retention flip-flops (RFFs), which immunize it against register content loss during retention power state, the registers of the control module storing the exported values are not subject to a soft reset.

The L3_MAIN firewall registers are also retention-capable and are immune against content loss during CORE RETENTION power state. The control module registers are reset by a cold reset only, whereas the L3_MAIN firewall registers are reset by clearing the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit. When the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit comes back automatically to 1, the exported values are loaded.

CAUTION

Before reprogramming the firewall registers and/or before using the FW_LOAD_REQ mechanism, the request must be asserted by configuring the REGUPDATE_CONTROL[0] BUSY_REQ bit.

To load the exported values at run time:

1. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x1 to ensure that no transaction can reach the slave NIU (suspend).
2. Clear the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit by writing 0x1 to it.
3. Wait until the REGUPDATE_CONTROL[1] FW_LOAD_REQ bit is reset to 0x1 by hardware.
4. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x0 to allow transactions to reach the slave NIU (resume).

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To reprogram the firewall registers at run time:

1. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x1 to ensure that no transaction can reach the slave NIU (suspend).
2. Upload the new values to all firewall registers.
3. Set the REGUPDATE_CONTROL[0] BUSY_REQ bit to 0x0 to allow transactions to reach the slave NIU (resume).

NOTE: At reset, exported values from the control module can modify hardware reset values.

14.2.3.8.1.1 L3_MAIN Firewall – Exported Reset Values

Table 14-20 and Table 14-21 list the exported reset values and mapping, respectively.

Table 14-20. L3_MAIN Firewall Exported Reset Values

MRM_PERMISSION_REGION_LOW_j [15:12]	MRM_PERMISSION_REGION_LOW_j [11:0]
0x0	0xFFF
0xF	0xFFF
0x0	0x038
0x2	0x038

Table 14-21. L3_MAIN Firewall Exported Values Mapping

CONTROL_L3_HW_FW_EXPORTED_VALUES_CONF_FUNC and CONTROL_L3_HW_FW_EXPORTED_VALUES_CONF_DEBUG Bits	Slave NIU Firewall
[0]	GPMC
[3]	L3 RAM
[4]	DSS
[5]	ISS and IPU subsystem
[6]	GPU
[7]	IVA_SL2
[8]	IVA_CFG
[10]	ABE
[11]	EMIF
[12]	DEBUG Subsystem
[13]	L4_ABE
[16]	BB2D

For more information, see Chapter 18, *Control Module*.

14.2.3.8.2 Power Management

As part of the system-wide power-management scheme, the L3_MAIN interconnect goes into IDLE state after receiving a request from the power, reset, and clock management (PRCM) module after all commands are serviced. This function is handled by hardware.

To reduce power consumption, the L3_MAIN interconnect automatically performs internal clock autogating. This is managed by hardware; no software configurations or settings are required.

Retention is performed on all software-accessible registers:

- Statistic collectors
- Internal rate adapters
- Bandwidth regulators

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- Target agents
- Firewalls

This process prevents reconfiguration after a clock domain switches off.

14.2.3.8.3 L3_MAIN Firewall Functionality

The access to the slave NIUs is granted only to master NIUs according to in-band attributes sent in each transaction crossing the L3_MAIN interconnect, such as:

- MCMD: Specifies the type of access (read or write) required by the master NIU
- ConnID: Used to determine the permission of the master NIU
- MReqInfo: Transaction attribute adding information about the access type

Table 14-22 lists the MReqInfo values.

Table 14-22. MReqInfo Values

Qualifier	Access Definition	Access Description
MReqType	00: Processor data access 01: Processor instruction access 10: DMA access 11: Other	Indicates whether the request is for processor instruction fetch, processor data access or DMA access
MReqDebug	0: Functional 1: Debug	When set, indicates that the request has been issued by a master NIU in DEBUG state
MReqSupervisor	0: User 1: Privilege	When set, indicates that the request is qualified with the supervisor attribute. It can be provided by a processor running in supervisor mode or by a module that inherited this attribute from the processor (DMA channel with a supervisor attribute).

The firewall comparison mechanism enables access to a protected slave NIU only when a correct combination of three MReqInfo in-band parameters is transmitted.

MReqInfo is a combination of a fixed 3-bit pattern that corresponds to a combination of the parameters MReqDebug, MReqType, and MReqSupervisor. See Table 14-23.

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Table 14-23. L3_MAIN ReqInfo Mapping

ReqInfo Name		MReqDebug	MReqType	MReqSupervisor
Master NIUs	MPU_INIT	x	x	x
	IPU_INIT	x	x	x
	DSP_INIT	x	x	
	IVA_INIT			
	GPU_P1_INIT			
	GPU_P2_INIT			
	DSS_INIT			
	ISS_INIT			
	DEBUGSS_CS_DAP_INIT	x		x
	SDMA_RD_INIT		x	x
	SDMA_WR_INIT		x	x
	USB_HOST_HS_INIT			
	USB_OTG_SS_INIT			
	HSI_INIT			x
	FDIF_INIT			
	SATA_INIT			
	MMC1/2_INIT			
	BB2D_P1			
	BB2D_P2			
Slave NIUs	DMM_P1_TARG	x	x	x
	DMM2_P2_TARG	x	x	x
	GPMC_TARG			
	OCM_RAM_TARG			
	L4_PER_P1/2/3_TARG	x		x
	L4_CFG_TARG	x		x
	L4_WKUP_TARG	x		x
	ABE_TARG	x		
	IPU_TARG			
	GPU_TARG			
	L3_INSTR_TARG	x		
	ISS_TARG			
	OCMC_RAM			
	IVA_CONFIG_TARG	x		
	IVA_SL2IF_TARG			
	IVA_CONFIG_CT_TBR_TARG	x		
	DSS			
	ISS			
	IPU			
	GPU			
	BB2D			
	L3_INSTR			
	DEBUGSS_CT_TBR			

14.2.3.8.3.1 Protection Regions

Each slave NIU address space is subdivided into protection regions (maximum of 10). The regions are configurable with a size of 4-KiB granularity. The firewalls can also be multiport while using the description of the same regions for dual access memories or to support interleaving mechanisms on several memories.

Table 14-24 lists the number of protected regions and ports for each slave NIU.

Table 14-24. Slave NIU Firewall and Region Configuration

Domain	Slave NIU	Firewall	Number of Regions	Number of Ports
CLK1	ABE_TARG	ABE_FW	1	1
CLK2	OCMC_RAM	OCMC_RAM_FW	16	x 1
	GPMC	GPMC_FW	8	1
	IVA_SL2IF	IVA_SL2_IF_FW	4	1
	IVA_CONFIG	IVA_CONFIG_FW	1	1
	DSS	DSS_FW	8	1
	ISS	ISS_FW	1	1
	IPU	IPU_FW	4	1
	GPU	GPU_FW	1	1
	BB2D	BB2D_FW	1	1
CLK3	L3_INSTR	L3_INSTR_FW	2	1
	DEBUGSS_CT_TBR	DEBUGSS_CT_TBR_FW	1	1

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Two types of regions are distinguished in a slave NIU firewall:

- Default region: Available in all slave NIUs. The default region covers the entire slave NIU address range. Other firewall-configured regions must reset or overlay the default region, because it always has the lowest priority.
- Normal region: The number of normal regions varies in a slave NIU; they have identical capabilities (see Table 14-24).

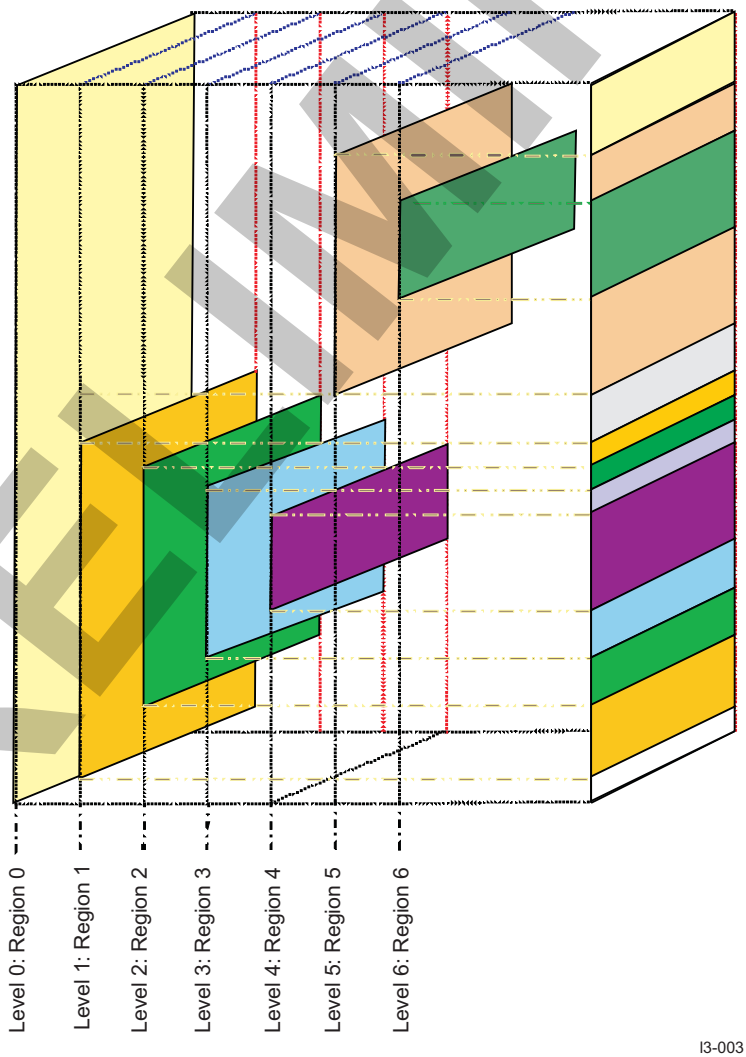
Each region has the following characteristics:

- Start address: Physical slave NIU start address
- End address: Physical slave NIU end address
- Specific access rights (see Section 14.2.3.8.3.3, *Protection Mechanism per Region Examples*)
- Priority level from 0 (lowest) to 10 (highest)

Depending on its priority level, a region can override the settings of another region; the access rights of the region with the highest priority apply. All regions have a fixed (not configurable) priority level that corresponds to their number: Region 1 has priority level 1, region 2 has priority level 2, and so on.

Figure 14-6 shows the priority level with associated regions. This priority level scheme allows multiplying the flexibility and capability of the firewall. Figure 14-6 shows a 7-region firewall setting that creates 13 regions (twice the number of regions created than originally available).

Figure 14-6. L3 Interconnect Region Overlay and Priority Level Overview



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The address range covered by the regions is defined in the START_REGION_i and END_REGION_i registers. The boundary checks are done on a minimum size of 4-KiB pages; thus, bits [11:0] of those 32-bit registers are not checked.

The address space size of the slave NIUs ([bits [31:12]) depends on the size of the slave NIU to protect (that is, if a memory is only 48KiB, then the size is defined through bits [16:12] of the slave NIU start and end address registers of the firewall region (START_REGION_i[16:12] and END_REGION_i[16:12]).

On multiport firewalls (EMIF), the checking of each REGION {0, n} can activate on one or several ports at the same time. However, if interleaving is not desired on some parts of the protected memory space, it is possible to apply or not apply region checking on selected ports using the region enable/disable on port instance capability of the END_REGION_i register.

Most slave NIUs support only one input port (port 0) except:

- The EMIF module protected by the EMIF firewall has three ports:
  - Port 0 for MPU accesses
  - Port 1 for the first L3_MAIN interconnect accesses
  - Port 2 for the second L3_MAIN interconnect accesses

A region can be applied or not to each port independently. To enable and disable the regions:

- For port 0: Set/clear the END_REGION_i[0] END_REGION_i_ENABLE_CORE0 bit (for all L3_MAIN firewalls).
- For port 1: Set/clear the END_REGION_i[1] END_REGION_i_ENABLE_CORE1 bit (EMIF firewalls).

14.2.3.8.3.2 L3_MAIN Firewall Registers Overview

Table 14-25 and Table 14-26 list the L3_MAIN firewall permission-setting registers.

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Table 14-25. L3_MAIN Firewall Read/Write Permission-Setting Register

Register Name	Bits	Field Name	Description (see Table 14-18)	Field Modifiability
MRM_PERMISSION_REGION_HIGH_j	31	W	ConnID = 15 write permission	RW
	30	R	ConnID = 15 read permission	RW
	29	W	ConnID = 14 write permission	RW
	28	R	ConnID = 14 read permission	RW
	27	W	ConnID = 13 write permission	RW
	26	R	ConnID = 13 read permission	RW
	25	W	ConnID = 12 write permission	RW
	24	R	ConnID = 12 read permission	RW
	23	W	ConnID = 11 write permission	RW
	22	R	ConnID = 11 read permission	RW
	21	W	ConnID = 10 write permission	RW
	20	R	ConnID = 10 read permission	RW
	19	W	ConnID = 9 write permission	RW
	18	R	ConnID = 9 read permission	RW
	17	W	ConnID = 8 write permission	RW
	16	R	ConnID = 8 read permission	RW
	15	W	ConnID = 7 write permission	RW
	14	R	ConnID = 7 read permission	RW
	13	W	ConnID = 6 write permission	RW
	12	R	ConnID = 6 read permission	RW
	11	W	ConnID = 5 write permission	RW
	10	R	ConnID = 5 read permission	RW
	9	W	ConnID = 4 write permission	RW
	8	R	ConnID = 4 read permission	RW
	7	W	ConnID = 3 write permission	RW
	6	R	ConnID = 3 read permission	RW
	5	W	ConnID = 2 write permission	RW
	4	R	ConnID = 2 read permission	RW
	3	W	ConnID = 1 write permission	RW
	2	R	ConnID = 1 read permission	RW
	1	W	ConnID = 0 write permission	RW
	0	R	ConnID = 0 read permission	RW

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Table 14-26. L3_MAIN Firewall Permission-Setting Register

Register name	Type of Permission	Bits	Field Name	Description	Field Modifiability
MRM_PERMISSION_REGION_LOW_j	Reserved	31:16		Reserved	
	Debug	15	DEBUG	PUBLIC PRIVILEGE DOMAIN DEBUG ALLOWED	RW
		14	DEBUG	PUBLIC USER DOMAIN DEBUG ALLOWED	RW
	Reserved	13:12		Reserved	
	Access	11	READ	PUBLIC PRIVILEGE READ ACCESS ALLOWED	RW
		10	WRITE	PUBLIC PRIVILEGE WRITE ACCESS ALLOWED	RW
		9	EXE	PUBLIC PRIVILEGE EXE ACCESS ALLOWED	RW
		8	READ	PUBLIC USER READ ACCESS ALLOWED	RW
		7	WRITE	PUBLIC USER WRITE ACCESS ALLOWED	RW
		6	EXE	PUBLIC USER ECXE ACCESS ALLOWED	RW

14.2.3.8.3.3 Protection Mechanism per Region Examples

The access permission of each region is configurable and defined through the MRM_PERMISSION_REGION_HIGH_j and MRM_PERMISSION_REGION_LOW_j registers (see Section 14.2.3.8.3.2, *L3_MAIN Firewall Registers Overview*).

Master NIU permissions:

1. To give read access to the master NIU with ConnID = n, set the MRM_PERMISSION_REGION_HIGH_j[n × 2] R bit.
2. To give write access to the master NIU with ConnID = n, set the MRM_PERMISSION_REGION_HIGH_j[n × 2 + 1] W bit.

Debug permissions:

1. To give privilege debug access, set the MRM_PERMISSION_REGION_LOW_j[15] DEBUG bit.
2. To give user debug access, set the MRM_PERMISSION_REGION_LOW_j[14] DEBUG bit.

User, read, write, and executable permissions:

1. To give privileged write access, set the MRM_PERMISSION_REGION_LOW_j[11] READ bit.
2. To give privileged read access, set the MRM_PERMISSION_REGION_LOW_j[10] WRITE bit.
3. To give privileged executable access, set the MRM_PERMISSION_REGION_LOW_j[9] EXE bit.
4. To give user write access, set the MRM_PERMISSION_REGION_LOW_j[8] READ bit.
5. To give user read access, set the MRM_PERMISSION_REGION_LOW_j[7] WRITE bit.
6. To give user executable access, set the MRM_PERMISSION_REGION_LOW_j[6] EXE bit.

Example: To provide debug write privilege access to the master NIU ConnID = 7, set the following bits:

- MRM_PERMISSION_REGION_HIGH_j[15] W
- MRM_PERMISSION_REGION_LOW_j[15] DEBUG

14.2.3.8.3.4 L3_MAIN Firewall Error Logging

If a protection violation error is detected, the following signals are generated:

- An in-band error is generated to the master NIU of the access.
- An interrupt is generated to the Cortex-A15 and DSP INTCs.

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The L3_MAIN interconnect does not differentiate errors generated by firewalls from all other supported types of errors.

An in-band error is generated by modules each time an access is not allowed. When an in-band error is sent back into the transaction it is seen as an external prefetch or data abort by the initiator, depending on whether the transaction was an instruction fetch or a data access.

Information about in-band errors is logged into two registers:

- ERROR_LOG_k: Logs the information about the start/end address of the hit region and the qualifiers of the transaction
- LOGICAL_PHYSICAL_ADDRESS_ERRLOG_k[31:12]: Logs the address of the failed access

NOTE: When a multiport firewall is implemented, these registers are duplicated for each port.

Table 14-27 lists the L3_MAIN firewall error-logging registers.

Table 14-27. L3 Firewall Error-Logging Registers

Register Name	Register Field Name	Field Modifiability	Parameter Comments
ERROR_LOG (When multiport firewall is implemented the error log register is duplicated for each port.)	RESERVED[31:24]	Read only	Reads return 0s.
	BLK_BURST_VIOLATION[23]	Read/write	Read 0x1: 2D burst not allowed or exceeds allowed size. Write to clear the ERROR_LOG and LOGICAL_PHYSICAL_ADDRESS_ERRLOG registers.
	SLVOFST_TRANSLATION_VIOLATION[22]	Read/write	START and END address of translated region cross two regions Marked as reserved when translation mechanism is not generated
	REGION_START_ERRLOG[21:17]	Read/write	Read: Wrong access hit this region number. Write to clear the ERROR_LOG and LOGICAL_PHYSICAL_ADDRESS_ERRLOG registers.
	REGION_END_ERRLOG[16:12]	Read/write	Read: Wrong access hit this region number. Write to clear the ERROR_LOG and LOGICAL_PHYSICAL_ADDRESS_ERRLOG registers.
	REQINFO_ERRLOG[11:0]	Read/write	Mapping of the error according to the reqinfo vector: ConnID [3:0] MCMD [0] [3] MReqDebug [1] MReqSupervisor [0] MReqType

L3 firewall errors can be cleared by writing to the ERROR_LOG_k register in the firewall that recorded the error. Clearing the ERROR_LOG_k register deasserts the corresponding error if it exists.

The L3 firewall register ERROR_LOG_k must be cleared before clearing the CONTROL_CORE_SEC_ERR_STATUS_FUNC and CONTROL_CORE_SEC_ERR_STATUS_DEBUG registers in the control module.

When a protection violation occurs, an interrupt is sent to the MPU and DSP INTC (if enabled). An in-band error is sent back, and an error is logged in the CONTROL_SEC_ERR_STATUS_FUNC and CONTROL_SEC_ERR_STATUS_DEBUG registers, depending on the functional mode:

- In application mode:
  - CONTROL_SEC_ERR_STATUS_FUNC[1] – L3 RAM protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[2] – GPMC protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[3] – EMIF protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[4] – IVA protection violation

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- CONTROL_SEC_ERR_STATUS_FUNC[5] – IPU protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[6] – IVA SL2 protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[8] – SYSTEM DMA protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[13] – GPU protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[14] – DSS protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[15] – ISS protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[16] – L4_PER protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[17] – L4_CFG protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[18] – DEBUG subsystem protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[19] – AUDIO slave NIU protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[22] – L4_WKUP protection violation
- CONTROL_SEC_ERR_STATUS_FUNC[23] – BB2D protection violation

• In debug mode:

- CONTROL_SEC_ERR_STATUS_DEBUG[1] – L3 RAM protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[2] – GPMC protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[3] – EMIF protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[4] – IVA protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[5] – IPU protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[6] – IVA SL2 protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[13] – GPU protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[14] – DSS protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[15] – ISS protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[16] – L4_PER protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[17] – L4_CFG protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[18] – DEBUG subsystem protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[19] – AUDIO slave NIU protection violation
- CONTROL_SEC_ERR_STATUS_DEBUG[22] – L4_WKUP protection violation
- CONTROL_SEC_ERR_STATUS_BEGUG[23] – BB2D protection violation

For more information, see Chapter 18, *Control Module*.

14.2.3.8.3.5 L3_MAIN Firewall Default Configuration

Table 14-28 summarizes the configuration of the L3_MAIN firewalls.

Table 14-28. L3_MAIN Firewalls Default Configurations

Device/Region: 0						
Permission Type	**Reset Value**	**Reset Value**	**Reset Type**	**Run Time**	**Firewall Register (where j = 0)**	**Control Module Register**
ACCESS_ PERMISSION	All	0xFFF	Exported	Configurable	MRM_PERMISSION_REGION_LOW_j[11:0]	CONTROL_CORE_L3_HW_FW_ EXPORTED_VALUES_LOCK[k]
DEBUG_ PERMISSION	All	0xF	Exported	Configurable	MRM_PERMISSION_REGION_LOW_j[15:12]	CONTROL_CORE_L3_HW_FW_ EXPORTED_VALUES_LOCK[k]
INITIATOR_ PERMISSION	All	0xFFF FFFFF	Tied	Configurable	MRM_PERMISSION_REGION_HIGH_j[31:0]	N/A

NOTE: For the values of k see Table 14-29.

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Table 14-29. Control Module Register – Factorization

Variable Value k	Module Name	Regions
3	L3 RAM firewall	Regions 1 to 7
0	GPMC firewall	Regions 1 to 7
7	IVA_SL2IF firewall	Regions 1 to 7
6	GPU firewall	Regions 1 to 7
5	ISS firewall	Regions 1 to 7
4	DSS firewall	Regions 1 to 7
8	IVA firewall	Regions 1 to 7
12	DEBUG firewall	Region 1
13	DEBUGSS_CT_TBR firewall	Region 1
11	EMIF firewall	Regions 1 to 7

14.2.3.9 L3_MAIN Interconnect Error Handling

Error logging is enabled in the L3_MAIN interconnect. The three major types of errors are:

- Slave NIU errors
- Firewall errors (see Section 14.2.3.8.3.4, *L3_MAIN Firewall Error Logging*)
- Flag mux errors

14.2.3.9.1 Global Error-Routing Scheme

Figure 14-7 shows the L3_MAIN global error-routing scheme.

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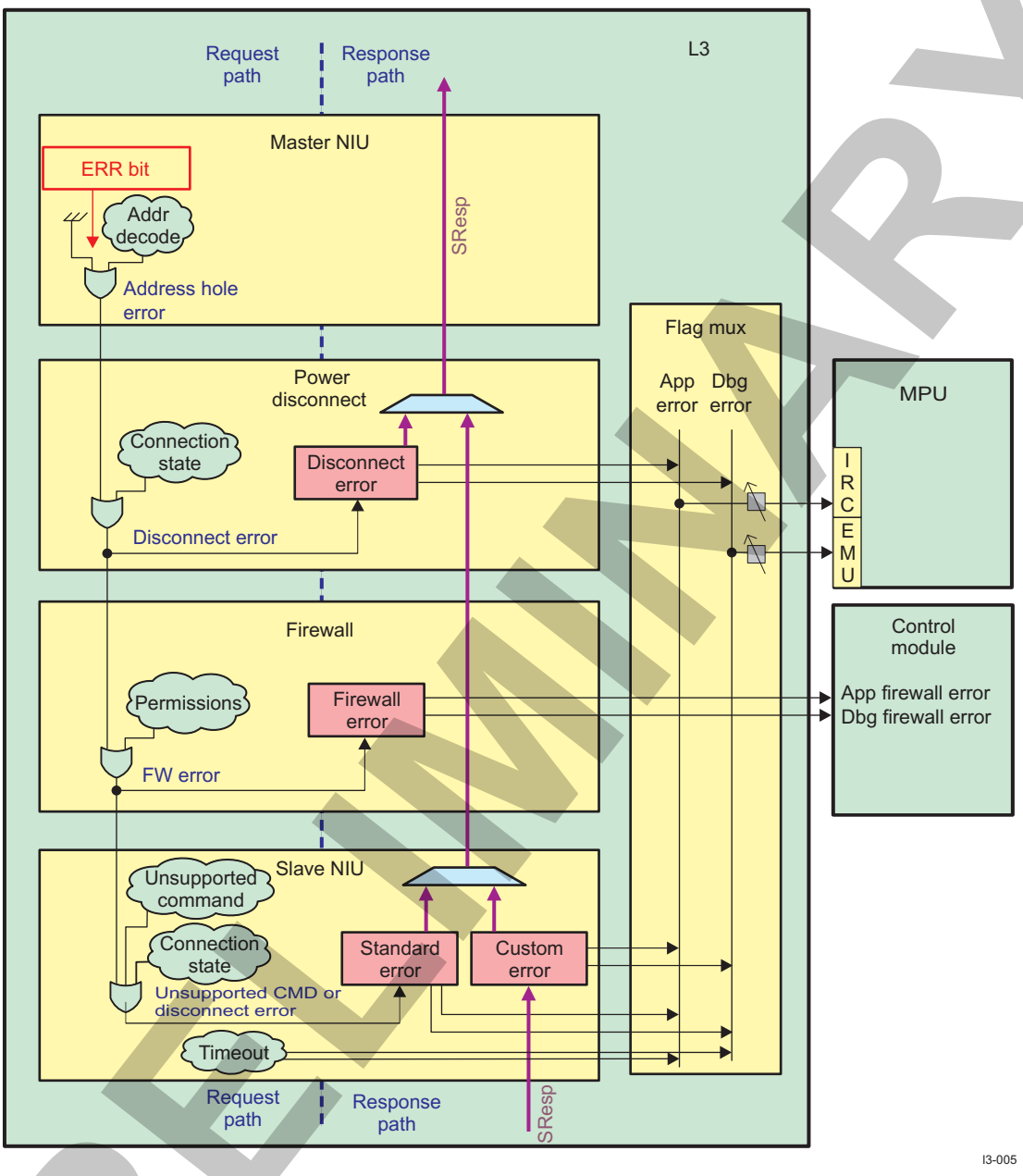
Figure 14-7. L3_MAIN Global Error-Routing Scheme



14.2.3.9.2 Slave NIU Error Logging

Error logging is implemented only at slave NIUs. Because the interconnect does not support master NIU error logging, an erroneous packet must be created and sent to one of the slave NIUs. The slave NIU that receives an erroneous packet is predictable but can change per master (see Table 14-30).

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Table 14-30. L3_MAIN Connectivity and Holes Error Routing

Master	Connectivity and Holes Errors Logged Into Slave NIUs
DEBUGSS_CS_DAP	GPMC
IPU	
MPU	
DMA_SYSTEM_RD	
DMA_SYSTEM_WR	
SATA	
DSP	
IVA	DMM1
MMC1	
MMC2	
BB2D_P1	
GPU_P1	
DSS	
	ISS
	FACDMM2ECT
	BB2D_P2
	GPU_P2
USB_OTG_SS	OCMC_RAM
HSI	ABE
USB_HOST_HS	

The slave NIU can be configured to report standard errors (errors generated within the interconnect):

- Firewall error: Protection violation; this error indicates that a request was rejected by a firewall and is reported to the control module. For more information, see Section 14.2.3.8.3.4, *L3_MAIN Firewall Error Logging*.
- Address hole: This error reports an unknown address for a request. The address map is local to each master NIU; therefore, an address hole error is reported each time a master NIU requests an access to a slave NIU to which it is not logically connected, even if this address exists in the global L3_MAIN address map. This error is detected only once per burst.
- Unsupported commands: This error reports that the master NIU sent a command that cannot be processed, because the slave NIU cannot accept it and no conversion to another command is possible. This error is detected only once per burst.
- Report custom errors: Basically, when the slave answer is SResp = ERR
- Report severity level, for standard error and custom errors:
  - None: Error logging for this type of error is disabled.
  - Error: Error is logged for this type of error.
  - Fault: Error is logged and interrupt is generated for this type of error.
- Generate interrupt on 2 bits depending on the MReqDebug qualifier:
  - Application error - FAULT[0]
  - Debug error - FAULT[1]

  By default, all slave NIUs are configured with standard and custom error levels set to FAULT. The errors are reported on the two flag muxes (see Figure 14-7), depending on the access type, application or debug. For more information, see Section 14.2.3.9.3, *Flag Mux Error Logging*.

  The slave NIU power-disconnect component also has error logging enabled, because in this case the slave NIU is in a clock domain that is switched off and therefore cannot catch the error. By nature, this component can generate only standard errors. By default, it is configured with the error level set to FAULT.

  Wake up on demand: If an error packet reaches a slave NIU that is set with MDiscBehave = 1 (wake up on demand), then the active signal is asserted and L3 processes the error generation when the

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slave is awake. Although this is inefficient, it simplifies NIU implementation and should not be a problem because errors are supposed to occur only during software debug.

14.2.3.9.3 Flag Mux Error Logging

All fault signals are sent to a flag mux component. There are four important FLAGMUX registers:

- L3_FLAGMUX_MASK0: Masks application error sources
- L3_FLAGMUX_MASK1: Masks debug error sources
- L3_FLAGMUX_REGERR0: Checks which application error sources are active
- L3_FLAGMUX_REGERR1: Checks which debug error sources are active

The two L3_FLAGMUX_MASK registers mask bit 0 or bit 1 of the flag inputs, and the L3_FLAGMUX_REGERR registers read input errors. Each register is dedicated to reporting the bit corresponding to the register number.

Table 14-31 describes the mapping of the flags to the corresponding sources.

Table 14-31. Interconnect Flag Mapping

	Flag Mux Input	Source
CLK1 Flag Mux	0	DMM_P1
	1	DMM_P2
	2	ABE
	3	L4_CFG
	4	CLK1_PWR_DISC_TARG_CLK2
	5	HOST_CLK1
	6	L4_WKUP
CLK2 Flag Mux	0	IPU
	1	DSS
	2	GPMC
	3	ISS
	4	IVA_CONFIG
	6	L4_PER_P0
	7	OCMC_RAM
	8	GPMC SERROR
	9	GPU
	10	IVA_SL2IF
	12	CLK2_PWR_DISC_TARG_CLK1
	15	L4_PER_P3
	16	L4_PER_P1
	17	L4_PER_P2
	18	HOST_CLK2
	22	BB2D
CLK3 Flag Mux	0	L3_INSTR
	1	DEBUGSS_CT_TBR
	2	HOST_CLK3

14.2.3.9.4 Severity Level of Standard and Custom Errors

The slave NIU registers are important for error logging.

- The L3_TARG_STDERRLOG_SVRTSTDLVL register shows the severity level for standard errors. According to the severity level, error logging is disabled, enabled with level ERROR, or enabled with level ERROR and flag FAULT.
- The L3_TARG_STDERRLOG_SVRTCUSTOMLVL register shows the severity level for custom errors

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(see Table 14-69).

- The L3_TARG_STDERRLOG_MAIN register (the main register for error-logging management) shows the validity of the logged information, standard or custom.
- The L3_TARG_STDERRLOG_HDR register stores packets in case of a standard error.
- The L3_TARG_STDERRLOG_MSTADDR register returns the MSTADDR field of the logged packet.
- The L3_TARG_STDERRLOG_SLVADDR register returns the SLVADDR field of the stored packet.
- The L3_TARG_STDERRLOG_INFO register saves the information field of the logged packet.

14.2.4 L3_MAIN Interconnect Programming Guide

14.2.4.1 L3 _MAIN Interconnect Low-Level Programming Models

This section describes the low-level hardware programming sequences for configuring and using the L3_MAIN interconnect module.

14.2.4.1.1 Global Initialization

14.2.4.1.1.1 Global Initialization of Surrounding Modules

This section identifies the requirements for initializing the surrounding modules when the L3_MAIN interconnect module is to be used for the first time after a device reset. The initialization of surrounding modules is based on the integration and environment of the L3_MAIN interconnect. For more information, see Section 14.2.2, *L3_MAIN Interconnect Integration* .

Table 14-32. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	For information about the configuration of the PRCM module, see Chapter 3, *Power, Reset, and Clock Management*.
Control module	For information about the configuration of the control module, see Chapter 18, *Control Module*.
MPU INTC	The MPU INTC must be configured to enable interrupts from the L3 interconnect module. See Chapter 17, *Interrupt Controllers*.
sDMA	For information about the configuration of the sDMA, see Chapter 16, *sDMA*.
L3 interconnect	For information about the configuration of the interconnect, see Chapter 14, *Interconnect*.

14.2.4.2 Operational Modes Configuration

14.2.4.2.1 L3_MAIN Interconnect Error Analysis Mode

14.2.4.2.1.1 Main Sequence: L3_MAIN Interconnect Error Analysis Mode

The information required to analyze an error source is logged in several registers. The number of registers to access depends on the error source.

Figure 14-8 shows the software sequence required in most cases.

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Figure 14-8. Typical Error Analysis Sequence

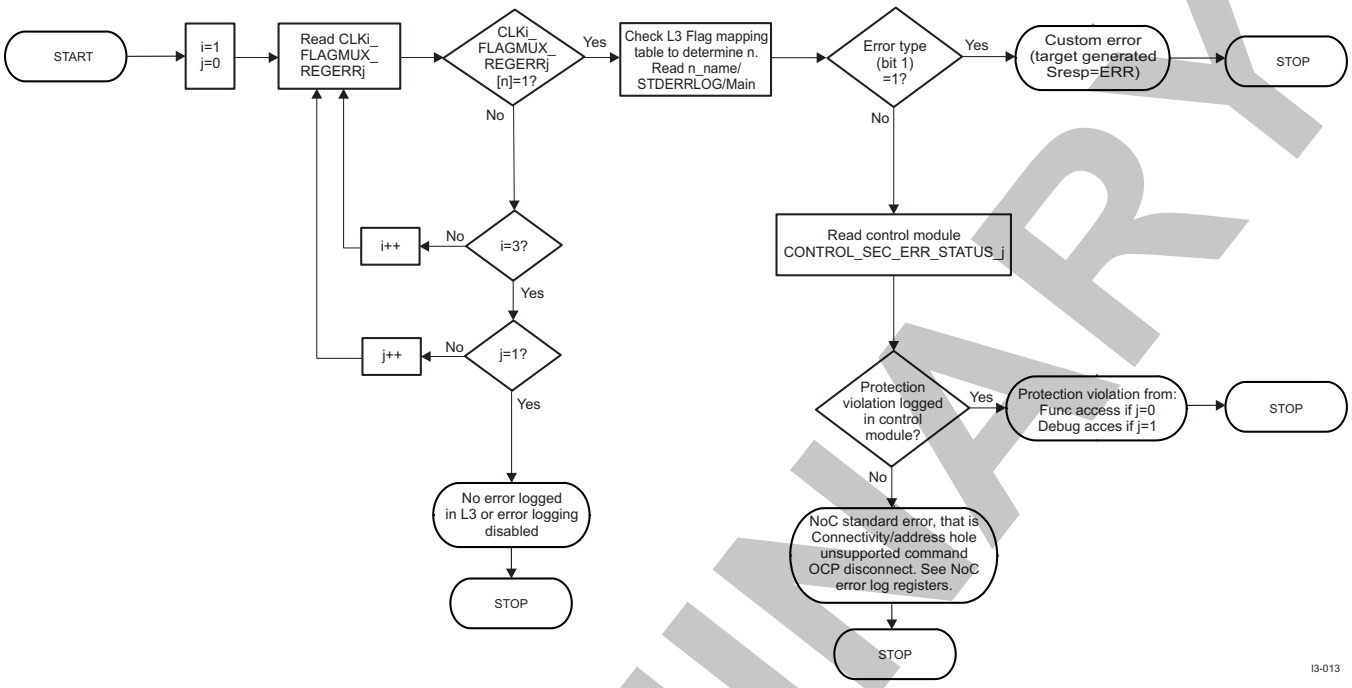

Table 14-33 lists the subprocess call summary for error analysis mode in the main sequence.

Table 14-33. Subprocess Call Summary for Main Sequence – Error Analysis Mode

Subprocess	Cross-Reference
L3 interconnect error analysis	See Section 14.2.4.2.1, *L3_MAIN Interconnect Error Analysis Mode.*
L3_MAIN interconnect protection violation error identification	See Section 14.2.4.2.1.1.2, *Subsequence: L3_MAIN Interconnect Protection Violation Error Identification.*
L3_MAIN interconnect unsupported command/address hole error identification	See Section 14.2.4.2.1.1.3, *Subsequence: L3_MAIN Interconnect Standard Error Identification.*
L3_MAIN interconnect reset FLAGMUX and module	See Section 14.2.4.2.1.1.4, *Subsequence: L3_MAIN Interconnect FLAGMUX Configuration.*

14.2.4.2.1.1.1 Subsequence: L3_MAIN Custom Error Identification

The procedure listed in Table 14-34 describes custom error identification.

Table 14-34. Custom Error Identification

Step	Register/Bit Field/Programming Model	Value
IF: Is custom error detected?	L3_TARG_STDERRLOG_MAIN[1] STDERRLOG_MAIN_ERRTYPE	=0x1
Read information field of the response packet.	L3_TARG_STDERRLOG_CUSTOMINFO_INFO[7:0] STDERRLOG_CUSTOMINFO_INFO	xxx
Read the address of the initiator that caused error.	L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR[10:0] STDERRLOG_CUSTOMINFO_MSTADDR	xxx
Read the type of operation (read/write).	L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE[1:0] STDERRLOG_CUSTOMINFO_OPCODE	xxx
ENDIF		

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14.2.4.2.1.1.2 Subsequence: L3_MAIN Interconnect Protection Violation Error Identification

The procedure listed in Table 14-35 describes protection violation error identification and where it is logged in the control module registers. Two types of errors are logged: application errors and debug errors.

Table 14-35. L3_MAIN Protection Violation Error Identification

Step	Register/Bit Field/Programming Model	Value
Read the burst violation.	ERROR_LOG_k[23] 2D_BURST_VIOLATION	xxx
Read the initiator ID.	ERROR_LOG_k[3:0] ConnID	xxx
Read the command that caused the error.	ERROR_LOG_k[7] MCMD	xxx
Read the address of the request that caused the error.	ERROR_LOG_k[31:12] SLVOFS_LOGICAL	xxx
IF: Is it an application error?	L3_FLAGMUX_REGERR0 [7:0] REGERROR0	0x0
Read the status bits to see which module firewall has worked.	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[20:0]	xxx
Clear the status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[20:0]	xxx
Clear the status bit.	L3_TARG_STDERRLOG_MAIN [31] STDERRLOG_MAIN_CLRLOG	0x0
ELSE IF	L3_FLAGMUX_REGERR1[7:0] REGERROR1	= 0x1
Read the status bits to see the module.	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[20:0]	xxx
Clear the status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[20:0]	xxx
Clear the status bit.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_MAIN_CLRLOG	0x0
ENDIF		
Clear the burst violation.	ERROR_LOG_k[23] 2D_BURST_VIOLATION	0x0
Clear the error status.	ERROR_LOG_k[21:17] REGION_START_ERRLOG	0x00

14.2.4.2.1.1.3 Subsequence: L3_MAIN Interconnect Standard Error Identification

The procedure listed in Table 14-36 describes the identification of standard errors inside the L3_MAIN interconnect. The standard errors are: unsupported command, address hole, and disconnect.

Table 14-36. L3_MAIN Standard Error Identification

Step	Register/Bit Field/Programming Model	Value
IF: Is an error detected?	L3_TARG_STDERRLOG_MAIN[18] STDERRLOG_MAIN_ERRCNT	= 0x1
Read the corresponding flag.	L3_FLAGMUX_REGERR0[7:0] REGERROR0	xxx
Read the corresponding flag.	L3_FLAGMUX_REGERR1[7:0] REGERROR1	xxx
Localize the slave NIU that generated the error.	See Table 14-31.	
ELSE		
Clear the error log.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_MAIN_CLRLOG	0x0
Clear the severity error status.	L3_TARG_STDERRLOG_SVRTSTDLVL[1:0] STDERRLOG_SVRTSTDLVL_0	0x2
ENDIF		

14.2.4.2.1.1.4 Subsequence: L3_MAIN Interconnect FLAGMUX Configuration

The procedures listed in Table 14-37 and Table 14-38 give information about the configuration of FLAGMUX masks.

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Table 14-37. FLAGMUX Configuration

Step	Register/Bit Field/Programming Model	Value
Set the FLAGMUX masks to mask an event.	L3_FLAGMUX_MASK0[7:0] MASK0 L3_FLAGMUX_MASK1[7:0] MASK1	xxx
Read the REGERR bits to see if an error is recorded.	L3_FLAGMUX_REGERR0[7:0] REGERR0 L3_FLAGMUX_REGERR1[7:0] REGERR1	xxx
Clear the slave NIU error log and the FLAGMUX error.	L3_TARG_STDERRLOG_MAIN[31] STDERRLOG_SVRTSTDLVL_0	0x1

Table 14-38. FLAGMUX Time-out Configuration

Step	Register/Bit Field/Programming Model	Value
Enable time-out for target.	L3_FLAGMUX_TIMEOUT_MASK0[4:0] MASK0 (1)	xxx
Read the REGERR bits to see if an error is recorded.	L3_FLAGMUX_TIMEOUT_REGERR0[4:0] REGERR0 (1)	xxx

(1) Bit fields are [4:0] for CLK1_FLAGMUX_CLK1, [18:0] for CLK2_FLAGMUX_CLK2, and [1:0] for CLK3_FLAGMUX_CLK3.

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14.2.5 L3_MAIN Interconnect Register Manual

14.2.5.1 L3_MAIN Register Group Summary

The registers in the L3 interconnect are divided into eight groups:

- Firewall registers (see Table 14-40)
- HOST registers (see Table 14-62)
- TARG registers (see Table 14-98)
- PWR_DISC registers (see Table 14-141)
- FLAGMUX registers (see Table 14-165)
- BW registers (see Table 14-188)
- RA registers (see Table 14-218)
- STATCOLL registers (see Table 14-227)

14.2.5.1.1 L3_MAIN Firewall Registers Summary and Description

Table 14-39. L3_MAIN Firewall Instance Summary

Module Name	Base Address	Size
EMIF Firewall	0x4A20 C000	256B
GPMC Firewall	0x4A21 0000	256B
OCMC_RAM Firewall	0x4A21 2000	384B
GPU Firewall	0x4A21 4000	144B
ISS Firewall	0x4A21 6000	144B
IPU Firewall	0x4A21 8000	192B
BB2D Firewall	0x4A21 A000	144B
DSS Firewall	0x4A21 C000	256B
IVA_SL2IF Firewall	0x4A21 E000	192B
IVA_CONFIG Firewall	0x4A22 0000	144B
DEBUGSS_CT_TBR Firewall	0x4A22 4000	144B
L3_INSTR Firewall	0x4A22 6000	160B
ABE Firewall	0x4A22 8000	144B

14.2.5.1.1.1 L3_MAIN Firewall Registers Summary

Table 14-40. L3_MAIN Firewall Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMIF Firewall L3_MAIN Physical Address	GPMC Firewall L3_MAIN Physical Address	OCMC_RAM Firewall L3_MAIN Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A20 C000+(0x10*k)	0x4A21 0000+(0x10*k)	0x4A21 2000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A20 C004+(0x10*k)	0x4A21 0004+(0x10*k)	0x4A21 2004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A20 C040	0x4A21 0040	0x4A21 2040
START_REGION_i [2]	RW	32	0x080+(0x10*i)	0x4A20 C080+(0x10*i)	0x4A21 0080+(0x10*i)	0x4A21 2080+(0x10*i)

(1) k = 0 to 1 for EMIF Firewall
k = 0 for GPMC Firewall
k = 0 for OCMC_RAM Firewall

(2) i = 1 to 7 for EMIF Firewall
i = 1 to 7 for GPMC Firewall
i = 1 to 15 for OCMC_RAM Firewall

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Table 14-40. L3_MAIN Firewall Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	EMIF Firewall L3_MAIN Physical Address	GPMC Firewall L3_MAIN Physical Address	OCMC_RAM Firewall L3_MAIN Physical Address
END_REGION_i [2]	RW	32	0x084+(0x10*i)	0x4A20 C084+(0x10*i)	0x4A21 0084+(0x10*i)	0x4A21 2084+(0x10*i)
MRM_PERMISSION_REGION_HIGH_j [3]	RW	32	0x08C+(0x10*j)	0x4A20 C08C+(0x10*j)	0x4A21 008C+(0x10*j)	0x4A21 208C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j [3]	RW	32	0x088+(0x10*j)	0x4A20 C088+(0x10*j)	0x4A21 0088+(0x10*j)	0x4A21 2088+(0x10*j)

[3] j = 0 to 7 for EMIF Firewall
j = 0 to 7 for GPMC Firewall
j = 0 to 15 for OCMC_RAM Firewall

Table 14-41. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPU Firewall L3_MAIN Physical Address	ISS Firewall L3_MAIN Physical Address	IPU Firewall L3_MAIN Physical Address	BB2D Firewall L3_MAIN Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A21 4000+(0x10*k)	0x4A21 6000+(0x10*k)	0x4A21 8000+(0x10*k)	0x4A21 A000 + (0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A21 4004+(0x10*k)	0x4A21 6004+(0x10*k)	0x4A21 8004+(0x10*k)	0x4A21 A004 + (0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A21 4040	0x4A21 6040	0x4A21 8040	0x4A21 A040
START_REGION_i [2]	RW	32	0x080+(0x10*i)	N/A	N/A	0x4A21 8080+(0x10*i)	N/A
END_REGION_i [2]	RW	32	0x084+(0x10*i)	N/A	N/A	0x4A21 8084+(0x10*i)	N/A
MRM_PERMISSION_REGION_HIGH_j [3]	RW	32	0x08C+(0x10*j)	0x4A21 408C+(0x10*j)	0x4A21 608C+(0x10*j)	0x4A21 808C+(0x10*j)	0x4A21 A08C + (0x10*j)
MRM_PERMISSION_REGION_LOW_j [3]	RW	32	0x088+(0x10*j)	0x4A21 4088+(0x10*j)	0x4A21 6088+(0x10*j)	0x4A21 8088+(0x10*j)	0x4A21 A088 + (0x10*j)

[1] k = 0 for GPU Firewall
k = 0 for ISS Firewall
k = 0 for IPU Firewall
k = 0 for BB2D Firewall

[2] i = 1 to 7 for GPU Firewall
i = 1 to 7 for ISS Firewall
i = 1 to 3 for IPU Firewall
i = 0 for BB2D Firewall

[3] j = 0 for GPU Firewall
j = 0 for ISS Firewall
j = 0 to 3 for IPU Firewall
j = 0 for BB2D Firewall

Table 14-42. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS Firewall L3_MAIN Physical Address	IVA_SL2IF Firewall L3_MAIN Physical Address	IVA_CONFIG Firewall L3_MAIN Physical Address
ERROR_LOG_k [1]	RW	32	0x000+(0x10*k)	0x4A21C000+(0x10*k)	0x4A21E000+(0x10*k)	0x4A22 0000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k [1]	RO	32	0x004+(0x10*k)	0x4A21C004+(0x10*k)	0x4A21E004+(0x10*k)	0x4A22 0004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A21 C040	0x4A21 E040	0x4A22 0040

[1] k = 0 for DSS Firewall
k = 0 for IVA_SL2IF Firewall
k = 0 for IVA_CONFIG Firewall

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Table 14-42. L3_MAIN Firewall Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DSS Firewall L3_MAIN Physical Address	IVA_SL2IF Firewall L3_MAIN Physical Address	IVA_CONFIG Firewall L3_MAIN Physical Address
START_REGION_i	RW	32	0x080+(0x10*i)	0x4A21 C080 + (0x10*i)	0x4A21 E080 + (0x10*i)	N/A
END_REGION_i	RW	32	0x084+(0x10*i)	0x4A21 C084 + (0x10*i)	0x4A21 E084 + (0x10*i)	N/A
MRM_PERMISSION_REGION_HIGH_j (2)	RW	32	0x08C+(0x10*j)	0x4A21 C08C+(0x10*j)	0x4A21 E08C+(0x10*j)	0x4A22 008C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j (2)	RW	32	0x088+(0x10*j)	0x4A21 C088+(0x10*j)	0x4A21 E088+(0x10*j)	0x4A22 0088+(0x10*j)

(2) j = 0 to 7 for DSS Firewall
j = 0 to 3 for IVA_SL2IF Firewall
j = 0 for IVA_CONFIG Firewall

Table 14-43. L3_MAIN Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3_INSTR Firewall L3_MAIN Physical Address	ABE Firewall L3_MAIN Physical Address	DEBUGSS_CT_TBR Firewall L3_MAIN Physical Address
ERROR_LOG_k (1)	RW	32	0x000+(0x10*k)	0x4A22 6000+(0x10*k)	0x4A22 8000+(0x10*k)	0x4A22 4000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k (1)	RO	32	0x004+(0x10*k)	0x4A22 6004+(0x10*k)	0x4A22 8004+(0x10*k)	0x4A22 4004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A22 6040	0x4A22 8040	0x4A22 4040
START_REGION_i (2)	RW	32	0x080+(0x10*i)	0x4A22 6080+(0x10*i)	N/A	N/A
END_REGION_i (2)	RW	32	0x084+(0x10*i)	0x4A22 6084+(0x10*i)	N/A	N/A
MRM_PERMISSION_REGION_HIGH_j (3)	RW	32	0x08C+(0x10*j)	0x4A22 608C+(0x10*j)	0x4A22 808C+(0x10*j)	0x4A22 408C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j (3)	RW	32	0x088+(0x10*j)	0x4A22 6088+(0x10*j)	0x4A22 8088+(0x10*j)	0x4A22 4088+(0x10*j)

(1) k = 0 for L3_INSTR Firewall
k = 0 for ABE Firewall
k = 0 for DEBUGSS_CT_TBR Firewall
(2) i = 1 for L3_INSTR Firewall
(3) j = 0 to 1 for L3_INSTR Firewall
j = 0 for ABE Firewall
j=0 for DEBUGSS_CT_TBR Firewall

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14.2.5.1.1.2 L3_MAIN Firewall Registers Description

NOTE: Hardware reset values can be modified by exported values from the control module at reset.

Table 14-44. ERROR_LOG_k

Address Offset	0x0000 0000+(0x10*k)	**Index**	See Table 14-40 to Table 14-43.
Physical Address	0x4A20 C000+(0x10*k) 0x4A21 0000+(0x10*k) 0x4A21 2000+(0x10*k) 0x4A21 4000+(0x10*k) 0x4A21 6000+(0x10*k) 0x4A21 8000+(0x10*k) 0x4A21 A000 + (0x10*k) 0x4A21C000+(0x10*k) 0x4A21E000+(0x10*k) 0x4A22 0000+(0x10*k) 0x4A22 6000+(0x10*k) 0x4A22 8000+(0x10*k) 0x4A22 4000+(0x10*k)	**Instance**	EMIF Firewall GPMC Firewall OCMC_RAM Firewall GPU Firewall ISS Firewall IPU Firewall BB2D Firewall DSS Firewall IVA_SL2IF Firewall IVA_CONFIG Firewall L3_INSTR Firewall ABE Firewall DEBUGSS_CT_TBR Firewall
Description	Error log register for port k		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BLK_BURST_VIOLATION	RESERVED	REGION_START_ERRLOG						REGION_END_ERRLOG				REQINFO_ERRLOG											

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reads return 0s.	R	0x00
23	BLK_BURST_VIOLATION	Read 0x1: 2D burst not allowed or exceeding allowed size Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0
22	RESERVED	Reads return 0s.	R	0
21:17	REGION_START_ERRLOG	Read: Wrong access hit this region number Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0x00
16:12	REGION_END_ERRLOG	Read: Wrong access hit this region number Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0x00
11:0	REQINFO_ERRLOG	Read: Error in reqinfo vector mapped as follows: [11: 8] ConnID [3:0] [7] MCMD [0] [6:4] Reserved [3] MReqDebug [2] Reserved [1] MReqSupervisor [0] MReqType Write to clear ERROR_LOG_k and LOGICAL_ADDR_ERRLOG_k registers	RW	0x000

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Table 14-45. Register Call Summary for Register ERROR_LOG_k

L3 Interconnect

- L3_MAIN Firewall Error Logging: [0] [1] [2] [3]
- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [4] [5] [6] [7] [8] [9]
- L3_MAIN Firewall Registers Summary: [10] [11] [12] [13]
- L3_MAIN Firewall Registers Description: [15] [16] [17] [18]

Table 14-46. LOGICAL_ADDR_ERRLOG_k

Address Offset	0x0000 0004+(0x10*k)	**Index**	See Table 14-40 to Table 14-43.
Physical Address	0x4A20 C004+(0x10*k) 0x4A21 0004+(0x10*k) 0x4A21 2004+(0x10*k) 0x4A21 4004+(0x10*k) 0x4A21 6004+(0x10*k) 0x4A21 8004+(0x10*k) 0x4A21 A004 + (0x10*k) 0x4A21C004+(0x10*k) 0x4A21E004+(0x10*k) 0x4A22 0004+(0x10*k) 0x4A22 6004+(0x10*k) 0x4A22 8004+(0x10*k) 0x4A22 4004+(0x10*k)	**Instance**	EMIF Firewall GPMC Firewall OCMC_RAM Firewall GPU Firewall ISS Firewall IPU Firewall BB2D Firewall DSS Firewall IVA_SL2IF Firewall IVA_CONFIG Firewall L3_INSTR Firewall ABE Firewall DEBUGSS_CT_TBR Firewall
Description	Logical Physical Address Error log register for port k		
Type	RO		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLVOFS_LOGICAL																															

Bits	Field Name	Description	Type	Reset
31[(1)]:0	SLVOFS_LOGICAL	Address generated by the Initiator before being translated	R	0x00000

(1) * = Size of the target

Table 14-47. Register Call Summary for Register LOGICAL_ADDR_ERRLOG_k

L3 Interconnect

- L3_MAIN Firewall Registers Summary: [0] [1] [2] [3]
- L3_MAIN Firewall Registers Description: [5] [6] [7] [8]

Table 14-48. REGUPDATE_CONTROL

Address Offset	0x0000 0040	**Index**	
Physical Address	0x4A20 C040 0x4A21 0040 0x4A21 2040 0x4A21 4040 0x4A21 6040 0x4A21 8040 0x4A21 A040 0x4A21 C040 0x4A21 E040 0x4A22 0040 0x4A22 6040 0x4A22 8040 0x4A22 4040	**Instance**	EMIF Firewall GPMC Firewall OCMC_RAM Firewall GPU Firewall ISS Firewall IPU Firewall BB2D Firewall DSS Firewall IVA_SL2IF Firewall IVA_CONFIG Firewall L3_INSTR Firewall ABE Firewall DEBUGSS_CT_TBR Firewall
Description	Register update control register		
Type	RW		

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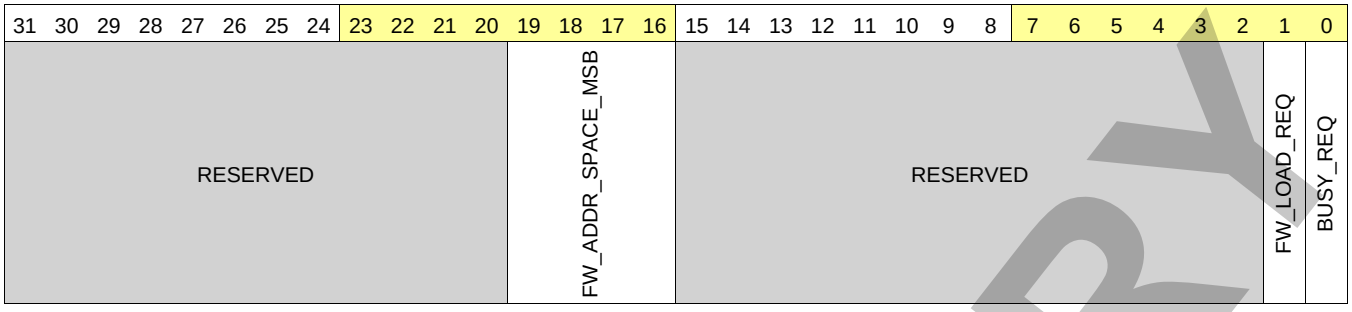


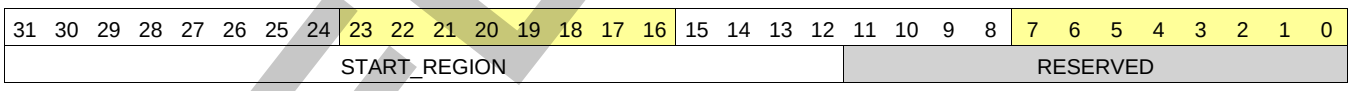
Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reads return 0s.	R	0x0000 0000
19:16	FW_ADDR_SPACE_MSB	Address space size	R	0x2
15:2	RESERVED	Reserved	R	0x0000 0000
1	FW_LOAD_REQ	Hadrdware set/Software clear	R	0x1
0	BUSY_REQ	Busy request	RW	0x0

Table 14-49. Register Call Summary for Register REGUPDATE_CONTROL

L3 Interconnect
- L3_MAIN Firewall Reset: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- L3_MAIN Firewall Registers Summary: [9] [10] [11] [12]

Table 14-50. START_REGION_i

Address Offset	0x0000 0080+(0x10*i)	**Index**	See Table 14-40 to Table 14-43.
Physical Address	0x4A20 C080+(0x10*i) 0x4A21 0080+(0x10*i) 0x4A21 2080+(0x10*i) 0x4A21 8080+(0x10*i) 0x4A21 C080 + (0x10*i) 0x4A21 E080 + (0x10*i) 0x4A22 6080+(0x10*i)	**Instance**	EMIF Firewall GPMC Firewall OCMC_RAM Firewall IPU Firewall DSS Firewall IVA_SL2IF Firewall L3_INSTR Firewall
Description	Start physical address of region i		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:12	START_REGION	Physical target start address of firewall region i. The size of this bit field depends on target addressable space, the maximum is [31:12]. See Table 14-52.	RW	0x00000
11:0	RESERVED	Reads return 0s.	R	0x0000

Table 14-51. Register Call Summary for Register START_REGION_i

L3 Interconnect
- Protection Regions: [0] [1]
- L3_MAIN Firewall Registers Summary: [2] [3] [4] [5]
- L3_MAIN Firewall Registers Description: [7] [8] [9] [10] [11] [12] [13]

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Table 14-52. Size of START_REGION_i[] START_REGION Bit Field

Firewall	Bit Field
EMIF Firewall	START_REGION_i[31:10] START_REGION
GPMCFirewall	START_REGION_i[30:12] START_REGION
OCMC_RAM Firewall	START_REGION_i[16:12] START_REGION
GPU Firewall	N/A
ISS Firewall	N/A
BB2D Firewall	N/A
IPU Firewall	START_REGION_i[23:12] START_REGION
DSS Firewall	START_REGION_i[22:12] START_REGION
IVA_SL2IF Firewall	START_REGION_i[17:12] START_REGION
IVA_CONFIG Firewall	N/A
DEBUGSS_CT_TBR	N/A
L3_INSTR Firewall	START_REGION_i[21:12] START_REGION
ABE Firewall	N/A

Table 14-53. END_REGION_i

Address Offset	0x0000 0084+(0x10*i)	**Index**	See Table 14-40 to Table 14-43.
Physical Address	0x4A20 C084+(0x10*i) 0x4A21 0084+(0x10*i) 0x4A21 2084+(0x10*i) 0x4A21 8084+(0x10*i) 0x4A21 C084 + (0x10*i) 0x4A21 E084 + (0x10*i) 0x4A22 6084+(0x10*i)	**Instance**	EMIF Firewall GPMC Firewall OCMC_RAM Firewall IPU Firewall DSS Firewall IVA_SL2IF Firewall L3_INSTR Firewall
Description	End physical address of region i		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_REGION																RESERVED														END_REGION_i_ENABLE_CORE1	END_REGION_i_ENABLE_CORE0

Bits	Field Name	Description	Type	Reset
31:12	END_REGION	Physical target end address of firewall region i. The size of this bit field depends on target addressable space, the maximum is [31:12]. See Table 14-55.	RW	0x00000
11:2	RESERVED	Reads return 0s.	R	0x0000
1	END_REGION_i_ENABLE_CORE1	Enable this region for port 1[(1)].	RW	0x0
0	END_REGION_i_ENABLE_CORE0	Enable this region for port 0.	RW	0x0

(1) Only for multiport firewalls with at least 1 port: EMIF Firewall

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Table 14-54. Register Call Summary for Register END_REGION_i

L3 Interconnect

- Protection Regions: [0] [1] [2] [3] [4] [5] [6]
- L3_MAIN Firewall Registers Summary: [7] [8] [9] [10]
- L3_MAIN Firewall Registers Description: [12] [13] [14] [15] [16] [17] [18]

Table 14-55. Size of END_REGION_i[] END_REGION Bit Field

Firewall	Bit Field
EMIFFirewall	END_REGION_i[31:10] END_REGION
GPMC Firewall	END_REGION_i[30:12] END_REGION
OCMC_RAM Firewall	END_REGION_i[16:12] END_REGION
GPU Firewall	N/A
ISS Firewall	N/A
BB2D Firewall	N/A
IPU Firewall	END_REGION_i[23:12] END_REGION
DSS Firewall	END_REGION_i[22:12] END_REGION
IVA_SL2IF Firewall	END_REGION_i[17:12] END_REGION
IVA_CONFIG Firewall	N/A
DEBUGSS_CT_TBR	N/A
L3_INSTR Firewall	END_REGION_i[21:12] END_REGION
ABE Firewall	N/A

Table 14-56. MRM_PERMISSION_REGION_HIGH_j

Address Offset	0x0000 008C+(0x10*i)	**Index**	See Table 14-40 to Table 14-43.
Physical Address	0x4A20 C08C+(0x10*j) 0x4A21 008C+(0x10*j) 0x4A21 208C+(0x10*j) 0x4A21 408C+(0x10*j) 0x4A21 608C+(0x10*j) 0x4A21 808C+(0x10*j) 0x4A21 A08C + (0x10*j) 0x4A21 C08C+(0x10*j) 0x4A21 E08C+(0x10*j) 0x4A22 008C+(0x10*j) 0x4A22 608C+(0x10*j) 0x4A22 808C+(0x10*j) 0x4A22 408C+(0x10*j)	**Instance**	EMIF Firewall GPMC Firewall OCMC_RAM Firewall GPU Firewall ISS Firewall IPU Firewall BB2D Firewall DSS Firewall IVA_SL2IF Firewall IVA_CONFIG Firewall L3_INSTR Firewall ABE Firewall DEBUGSS_CT_TBR Firewall
Description	Region j Permission High		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W15	R15	W14	R14	W13	R13	W12	R12	W11	R11	W10	R10	W9	R9	W8	R8	W7	R7	W6	R6	W5	R5	W4	R4	W3	R3	W2	R2	W1	R1	W0	R0

Bits	Field Name	Description	Type	Reset
31	W15	Master NIU ConnID = 115 write permission	RW	0x1
30	R15	Master NIU ConnID = 115 read permission	RW	0x1
29	W14	Master NIU ConnID = 14 write permission	RW	0x1
28	R14	Master NIU ConnID = 14 read permission	RW	0x1
27	W13	Master NIU ConnID = 13 write permission	RW	0x1
26	R13	Master NIU ConnID = 13 read permission	RW	0x1
25	W12	Master NIU ConnID = 12 write permission	RW	0x1
24	R12	Master NIU ConnID = 12 read permission	RW	0x1

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Bits	Field Name	Description	Type	Reset
23	W11	Master NIU ConnID = 11 write permission	RW	0x1
22	R11	Master NIU ConnID = 11 read permission	RW	0x1
21	W10	Master NIU ConnID = 10 write permission	RW	0x1
20	R10	Master NIU ConnID = 10 read permission	RW	0x1
19	W9	Master NIU ConnID = 9 write permission	RW	0x1
18	R9	Master NIU ConnID = 9 read permission	RW	0x1
17	W8	Master NIU ConnID = 8 write permission	RW	0x1
16	R8	Master NIU ConnID = 8 read permission	RW	0x1
15	W7	Master NIU ConnID = 7 write permission	RW	0x1
14	R7	Master NIU ConnID = 7 read permission	RW	0x1
13	W6	Master NIU ConnID = 6 write permission	RW	0x1
12	R6	Master NIU ConnID = 6 read permission	RW	0x1
11	W5	Master NIU ConnID = 5 write permission	RW	0x1
10	R5	Master NIU ConnID = 5 read permission	RW	0x1
9	W4	Master NIU ConnID = 4 write permission	RW	0x1
8	R4	Master NIU ConnID = 4 read permission	RW	0x1
7	W3	Master NIU ConnID = 3 write permission	RW	0x1
6	R3	Master NIU ConnID = 3 read permission	RW	0x1
5	W2	Master NIU ConnID = 2 write permission	RW	0x1
4	R2	Master NIU ConnID = 2 read permission	RW	0x1
3	W1	Master NIU ConnID = 1 write permission	RW	0x1
2	R1	Master NIU ConnID = 1 read permission	RW	0x1
1	W0	Master NIU ConnID = 0 write permission	RW	0x1
0	R0	Master NIU ConnID = 0 read permission	RW	0x1

Table 14-57. Register Call Summary for Register MRM_PERMISSION_REGION_HIGH_j

L3 Interconnect

- L3_MAIN Firewall Registers Overview: [0]
- Protection Mechanism per Region Examples: [1] [2] [3] [4]
- L3_MAIN Firewall Default Configuration: [5]
- L3_MAIN Firewall Registers Summary: [6] [7] [8] [9]

Table 14-58. MRM_PERMISSION_REGION_LOW_j

Address Offset	0x0000 0088+(0x10*i)	**Index**	See Table 14-40 to Table 14-43.
Physical Address	0x4A20 C088+(0x10*j)	**Instance**	EMIF Firewall
	0x4A21 0088+(0x10*j)		GPMC Firewall
	0x4A21 2088+(0x10*j)		OCMC_RAM Firewall
	0x4A21 4088+(0x10*j)		GPU Firewall
	0x4A21 6088+(0x10*j)		ISS Firewall
	0x4A21 8088+(0x10*j)		IPU Firewall
	0x4A21 A088 + (0x10*j)		BB2D Firewall
	0x4A21 C088+(0x10*j)		DSS Firewall
	0x4A21 E088+(0x10*j)		IVA_SL2IF Firewall
	0x4A22 0088+(0x10*j)		IVA_CONFIG Firewall
	0x4A22 6088+(0x10*j)		L3_INSTR Firewall
	0x4A22 8088+(0x10*j)		ABE Firewall
	0x4A22 4088+(0x10*j)		DEBUGSS_CT_TBR Firewall
Description	Region j Permission Low		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PUB_PRV_DEBUG	PUB_USR_DEBUG	RESERVED		PUB_PRV_WRITE	PUB_PRV_READ	PUB_PRV_EXE	PUB_USR_WRITE	PUB_USR_READ	PUB_USR_EXE	RESERVED					

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	RESERVED	R	See Table 14-60.
15	PUB_PRV_DEBUG	Public Privilege Debug Allowed	RW	See Table 14-60.
14	PUB_USR_DEBUG	Public User Debug Allowed	RW	See Table 14-60.
13:12	RESERVED	RESERVED	R	See Table 14-60.
11	PUB_PRV_WRITE	Public Privilege Write Allowed	RW	See Table 14-60.
10	PUB_PRV_READ	Public Privilege Read Allowed	RW	See Table 14-60.
9	PUB_PRV_EXE	Public Privilege Exe Allowed	RW	See Table 14-60.
8	PUB_USR_WRITE	Public User Write Access Allowed	RW	See Table 14-60.
7	PUB_USR_READ	Public User Read Access Allowed	RW	See Table 14-60.
6	PUB_USR_EXE	Public User Exe Access Allowed	RW	See Table 14-60.
5:0	RESERVED	RESERVED	R	See Table 14-60.

Table 14-59. Register Call Summary for Register MRM_PERMISSION_REGION_LOW_j

L3 Interconnect

- L3_MAIN Firewall – Exported Reset Values: [0] [1]
- L3_MAIN Firewall Registers Overview: [2]
- Protection Mechanism per Region Examples: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
- L3_MAIN Firewall Default Configuration: [13] [14]
- L3_MAIN Firewall Registers Summary: [15] [16] [17] [18]

Table 14-60. Reset Value for MRM_PERMISSION_REGION_LOW_j

Region	Reset Value
Region j = 0 (except EMIF firewall)	0xFFFF0000
Region j = 0 (for EMIF firewall)	0xFFFFFFFF
Region j 0 (for all firewalls)	0xFFFFFFFF

14.2.5.1.2 L3_MAIN Host Register Summary and Description

Table 14-61. HOST Instance Summary

Module Name	Base Address	Size
CLK1_HOST_CLK1	0x4400 0000	8MiB
CLK2_HOST_CLK2	0x4480 0000	8MiB
CLK3_HOST_CLK3	0x4500 0000	8MiB

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14.2.5.1.2.1 L3_MAIN HOST Register Summary

Table 14-62. HOST Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_HOST_CLK1	CLK1_HOST_CLK1 L3_MAIN Physical Address	Address Offset for CLK2_HOST_CLK2	CLK2_HOST_CLK2 L3_MAIN Physical Address	Address Offset for CLK3_HOST_CLK3	CLK3_HOST_CLK3 L3_MAIN Physical Address
L3_HOST_STDHOSTHDR_COREREG	R	32	0x0000 0000	0x4400 0000	0x0080 0000	0x4480 0000	0x0100 0000	0x4500 0000
L3_HOST_STDHOSTHDR_VERSIONREG	R	32	0x0000 0004	0x4400 0004	0x0080 0004	0x4480 0004	0x0100 0004	0x4500 0004
L3_HOST_STDHOSTHDR_MAINCTLREG	R	32	0x0000 0008	0x4400 0008	0x0080 0008	0x4480 0008	0x0100 0008	0x4500 0008
L3_HOST_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0040	0x4400 0040	0x0080 0040	0x4480 0040	0x0100 0040	0x4500 0040
L3_HOST_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0044	0x4400 0044	0x0080 0044	0x4480 0044	0x0100 0044	0x4500 0044
L3_HOST_STDERRLOG_MAIN	RW	32	0x0000 0048	0x4400 0048	0x0080 0048	0x4480 0048	0x0100 0048	0x4500 0048
L3_HOST_STDERRLOG_HDR	R	32	0x0000 004C	0x4400 004C	0x0080 004C	0x4480 004C	0x0100 004C	0x4500 004C
L3_HOST_STDERRLOG_MSTADDR	R	32	0x0000 0050	0x4400 0050	0x0080 0050	0x4480 0050	0x0100 0050	0x4500 0050
L3_HOST_STDERRLOG_SLVADDR	R	32	0x0000 0054	0x4400 0054	0x0080 0054	0x4480 0054	0x0100 0054	0x4500 0054
L3_HOST_STDERRLOG_INFO	R	32	0x0000 0058	0x4400 0058	0x0080 0058	0x4480 0058	0x0100 0058	0x4500 0058
L3_HOST_STDERRLOG_SLVOFSLSB	R	32	0x0000 005C	0x4400 005C	0x0080 005C	0x4480 005C	0x0100 005C	0x4500 005C
L3_HOST_STDERRLOG_SLVOFSMSB	R	32	0x0000 0060	0x4400 0060	0x0080 0060	0x4480 0060	0x0100 0060	0x4500 0060
L3_HOST_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0064	0x4400 0064	0x0080 0064	0x4480 0064	0x0100 0064	0x4500 0064
L3_HOST_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0068	0x4400 0068	0x0080 0068	0x4480 0068	0x0100 0068	0x4500 0068
L3_HOST_STDERRLOG_CUSTOMINFO_WR	R	32	0x0000 006C	0x4400 006C	0x0080 006C	0x4480 006C	0x0100 006C	0x4500 006C
L3_HOST_STDERRLOG_CUSTOMINFO_ADDR	R	32	0x0000 0070	0x4400 0070	0x0080 0070	0x4480 0070	0x0100 0070	0x4500 0070
L3_HOST_STDERRLOG_CUSTOMINFO_DECERR	R	32	0x0000 0074	0x4400 0074	0x0080 0074	0x4480 0074	0x0100 0074	0x4500 0074

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14.2.5.1.2.2 L3_MAIN HOST Register Description

Table 14-63. L3_HOST_STDHOSTHDR_COREREG

Address Offset	See Table 14-62.		
Physical Address	0x4400 0000 0x4480 0000 0x4500 0000	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x1A.	R	0x1A
15:1	RESERVED		R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-64. Register Call Summary for Register L3_HOST_STDHOSTHDR_COREREG

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-65. L3_HOST_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-62.		
Physical Address	0x4400 0004 0x4480 0004 0x4500 0004	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-66. Register Call Summary for Register L3_HOST_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-67. L3_HOST_STDHOSTHDR_MAINCTLREG

Address Offset	See Table 14-62.		
Physical Address	0x4400 0008 0x4480 0008 0x4500 0008	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													STDHOSTHDR_MAINCTLREG_FLT	RESERVED	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	STDHOSTHDR_MAINCTLREG_FLT	Asserted when a Fault condition is detected: if the unit includes Error Logging, Fault is asserted when the Fault Control register field indicates a Fault, and de-asserted when FltCnt is reset. If no Error Logging is implemented, this bit becomes unit-dependent. In all cases, Flt bit and Flt pin (service network) have the same logical level. Type: Status. Reset value: X.	R	0
1:0	RESERVED		R	0x0

Table 14-68. Register Call Summary for Register L3_HOST_STDHOSTHDR_MAINCTLREG

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-69. L3_HOST_STDERRLOG_SVRTSTDLVL

Address Offset	See Table 14-62.		
Physical Address	0x4400 0040 0x4480 0040 0x4500 0040	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SVRTSTDLVL_0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	STDERRLOG_SVRTSTDLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

Table 14-70. Register Call Summary for Register L3_HOST_STDERRLOG_SVRTSTDLVL

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

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Table 14-71. L3_HOST_STDERRLOG_SVRTCUSTOMLVL

Address Offset	See Table 14-62.		
Physical Address	0x4400 0044 0x4480 0044 0x4500 0044	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SVRTCUSTOMLVL_0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	STDERRLOG_SVRTCUSTOMLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

Table 14-72. Register Call Summary for Register L3_HOST_STDERRLOG_SVRTCUSTOMLVL

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-73. L3_HOST_STDERRLOG_MAIN

Address Offset	See Table 14-62.		
Physical Address	0x4400 0048 0x4480 0048 0x4500 0048	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	RW		

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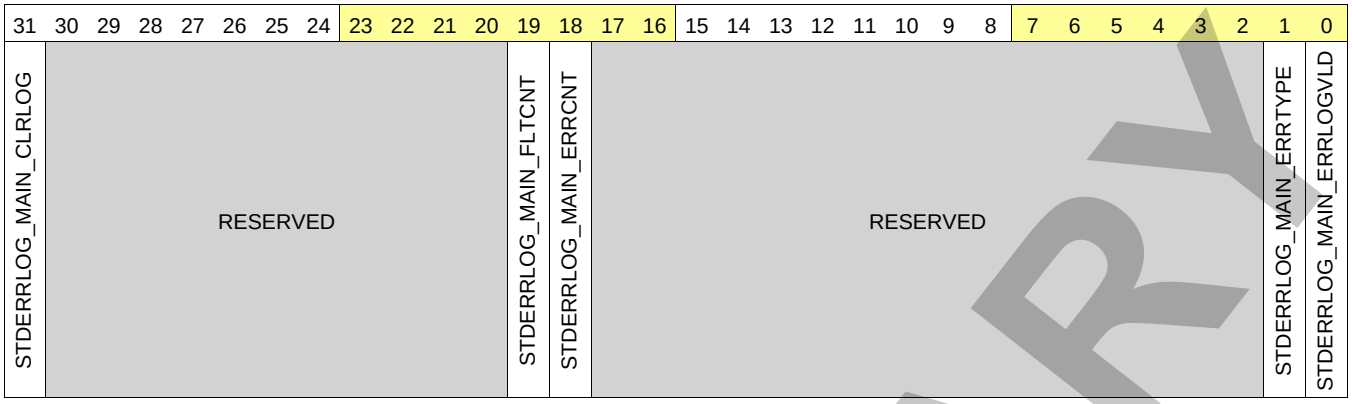

Bits	Field Name	Description	Type	Reset
31	STDERRLOG_MAIN_CLRLOG	Clears "Error Logging Valid" bit when written to 1. Type: Give_AutoCleared. Reset value: 0x0.	RW	0
30:20	RESERVED		R	0x000
19	STDERRLOG_MAIN_FLTCNT	Asserted when at least one error with severity level FAULT is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
18	STDERRLOG_MAIN_ERRCNT	Asserted when at least one error with severity level ERROR is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
17:2	RESERVED		R	0x0000
1	STDERRLOG_MAIN_ERRTYPE	Indicates logging type. Type: Status. Reset value: X. Read 0x0: Logged Error format is standard (header and necker recorded). Read 0x1: Logged Error format is module dependent. CustomInfo register(s) may be implemented to store additional information.	R	0
0	STDERRLOG_MAIN_ERRLOGVLD	Error Logging Valid. Asserted when logging information is valid(indicates that an error has been logged). Type: Status. Reset value: X.	R	0

Table 14-74. Register Call Summary for Register L3_HOST_STDERRLOG_MAIN

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-75. L3_HOST_STDERRLOG_HDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 004C 0x4480 004C 0x4500 004C	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDERRLOG_HDR_LEN1						RESERVED		STDERRLOG_HDR_STOPOFSWRPSZ				STDERRLOG_HDR_ERR	RESERVED			STDERRLOG_HDR_PRESSURE	RESERVED			STDERRLOG_HDR_OPCODE			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:18	STDERRLOG_HDR_LEN1	This field contains the number of payload cell(s) minus one of the logged packet. Type: Status. Reset value: X.	R	0x00
17:16	RESERVED		R	0x0
15:12	STDERRLOG_HDR_STOPOFSWRPSZ	StopOfs or WrapSize field of the logged packet (meaning depends on Wrp bit of logged opcode). Type: Status. Reset value: X.	R	0x0
11	STDERRLOG_HDR_ERR	Err bit of the logged packet. Type: Status. Reset value: X.	R	0
10:7	RESERVED		R	0x0
6	STDERRLOG_HDR_PRESSURE	Pressure field of the logged packet. Type: Status. Reset value: X.	R	0
5:4	RESERVED		R	0x0
3:0	STDERRLOG_HDR_OPCODE	Opcode of the logged packet. Type: Status. Reset value: X.	R	0x0

Table 14-76. Register Call Summary for Register L3_HOST_STDERRLOG_HDR

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-77. L3_HOST_STDERRLOG_MSTADDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0050 0x4480 0050 0x4500 0050	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:0	STDERRLOG_MSTADDR	Master Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

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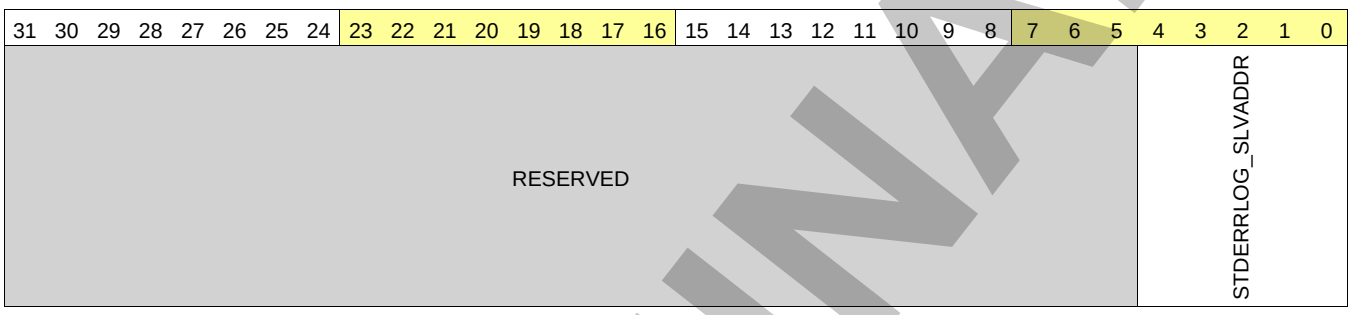
Table 14-78. Register Call Summary for Register L3_HOST_STDERRLOG_MSTADDR

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-79. L3_HOST_STDERRLOG_SLVADDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0054 0x4480 0054 0x4500 0054	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4:0	STDERRLOG_SLVADDR	Slave Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

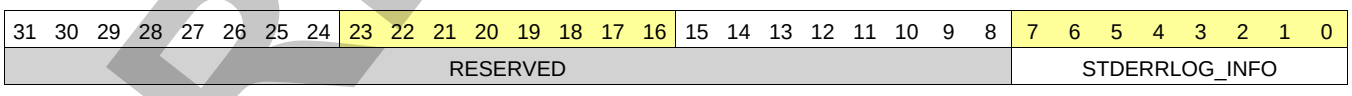
Table 14-80. Register Call Summary for Register L3_HOST_STDERRLOG_SLVADDR

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-81. L3_HOST_STDERRLOG_INFO

Address Offset	See Table 14-62.		
Physical Address	0x4400 0058 0x4480 0058 0x4500 0058	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_INFO	Info field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-82. Register Call Summary for Register L3_HOST_STDERRLOG_INFO

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

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Table 14-83. L3_HOST_STDERRLOG_SLVOFSLSB

Address Offset	See Table 14-62.		
Physical Address	0x4400 005C 0x4480 005C 0x4500 005C	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_SLVOFSLSB																															

Bits	Field Name	Description	Type	Reset
31:0	STDERRLOG_SLVOFSLSB	LSB of the "slave offset" field, concatenated with "start offset" field of the logged packet. Type: Status. Reset value: X.	R	0x0000 0000

Table 14-84. Register Call Summary for Register L3_HOST_STDERRLOG_SLVOFSLSB

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-85. L3_HOST_STDERRLOG_SLVOFSMSB

Address Offset	See Table 14-62.		
Physical Address	0x4400 0060 0x4480 0060 0x4500 0060	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_SLVOFSMSB

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STDERRLOG_SLVOFSMSB	MSB of the "slave offset" field of the logged packet (according to NTTP packet format, this register field may exceed the actual "slave offset" size. Unused bits are stuck at 0, if any). Type: Status. Reset value: X.	R	0

Table 14-86. Register Call Summary for Register L3_HOST_STDERRLOG_SLVOFSMSB

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

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Table 14-87. L3_HOST_STDERRLOG_CUSTOMINFO_MSTADDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0064 0x4480 0064 0x4500 0064	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					STDERRLOG_CUSTOMINFO_MSTADDR									

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10:0	STDERRLOG_CUSTOMINFO_MSTADDR	Type: Status. Reset value: X.	R	0x00

Table 14-88. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_MSTADDR

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-89. L3_HOST_STDERRLOG_CUSTOMINFO_INFO

Address Offset	See Table 14-62.		
Physical Address	0x4400 0068 0x4480 0068 0x4500 0068	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_CUSTOMINFO_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	STDERRLOG_CUSTOMINFO_INFO	Type: Status. Reset value: X.	R	0x00

Table 14-90. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_INFO

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

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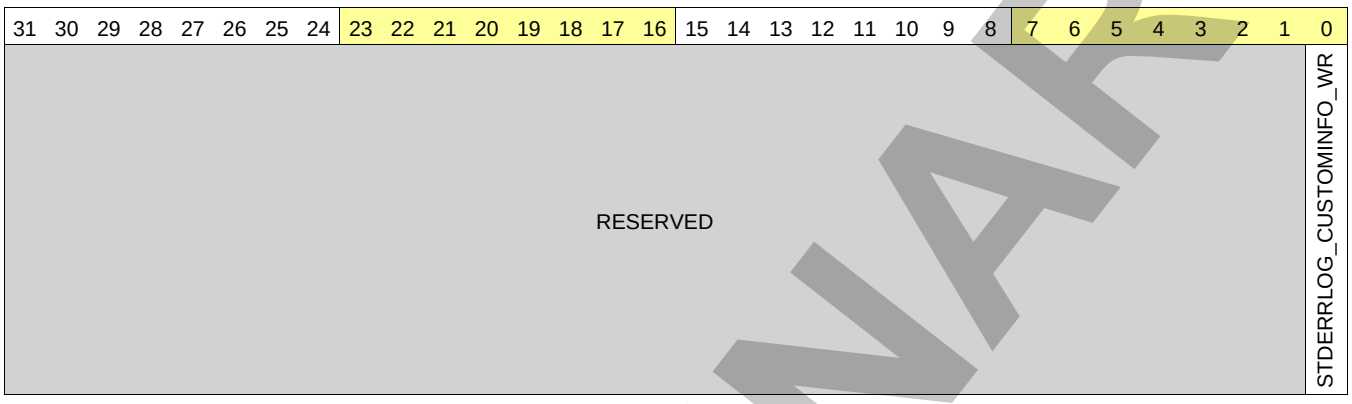
Table 14-91. L3_HOST_STDERRLOG_CUSTOMINFO_WR

Address Offset	See Table 14-62.		
Physical Address	0x4400 006C 0x4480 006C 0x4500 006C	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STDERRLOG_CUSTOMINFO_WR	Type: Status. Reset value: X.	R	0

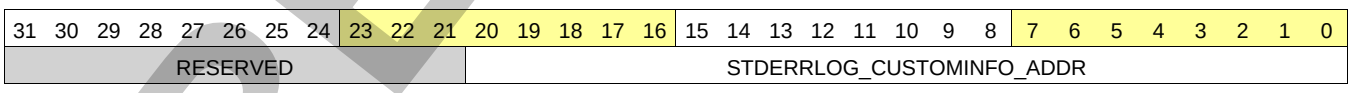
Table 14-92. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_WR

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

Table 14-93. L3_HOST_STDERRLOG_CUSTOMINFO_ADDR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0070 0x4480 0070 0x4500 0070	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20:0	STDERRLOG_CUSTOMINFO_ADDR	Type: Status. Reset value: X.	R	0x000000

Table 14-94. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_ADDR

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

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Table 14-95. L3_HOST_STDERRLOG_CUSTOMINFO_DECERR

Address Offset	See Table 14-62.		
Physical Address	0x4400 0074 0x4480 0074 0x4500 0074	**Instance**	CLK1_HOST_CLK1 CLK2_HOST_CLK2 CLK3_HOST_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_CUSTOMINFO_DECERR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	STDERRLOG_CUSTOMINFO_DECERR	Type: Status. Reset value: X.	R	0

Table 14-96. Register Call Summary for Register L3_HOST_STDERRLOG_CUSTOMINFO_DECERR

L3 Interconnect

- L3_MAIN HOST Register Summary: [0]

14.2.5.1.3 L3_MAIN TARG Register Summary and Description

Table 14-97. L3_MAIN TARG Instance Summary

Module Name	Base Address	Size
CLK1_DMM_P1_TARG	0x4400 0100	4KiB
CLK1_DMM_P2_TARG	0x4400 0200	4KiB
CLK1_ABE_TARG	0x4400 0300	4KiB
CLK1_L4_CFG_TARG	0x4400 0400	4KiB
CLK1_L4_WKUP_TARG	0x4400 0900	4KiB
CLK2_GPMC_TARG	0x4480 0100	4KiB
CLK2_OCMC_RAM_TARG	0x4480 0200	4KiB
CLK2_DSS_TARG	0x4480 0300	4KiB
CLK2_ISS_TARG	0x4480 0400	4KiB
CLK2_IPU_TARG	0x4480 0500	4KiB
CLK2_GPU_TARG	0x4480 0600	4KiB
CLK2_IVA_CONFIG_TARG	0x4480 0700	4KiB
CLK2_IVA_SL2IF_TARG	0x4480 0800	4KiB
CLK2_L4PER_P0_TARG	0x4480 0900	4KiB
CLK2_L4PER_P1_TARG	0x4480 0A00	4KiB

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Table 14-97. L3_MAIN TARG Instance Summary (continued)

Module Name	Base Address	Size
CLK2_L4PER_P2_TARG	0x4480 0B00	4KiB
CLK2_L4PER_P3_TARG	0x4480 0C00	4KiB
CLK2_BB2D_TARG	0x4480 2200	4KiB
CLK3_L3_INSTR_TARG	0x4500 0100	4KiB
CLK3_DEBUGSS_CT_TBR_TARG	0x4500 0300	4KiB

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14.2.5.1.3.1 L3_MAIN TARG Registers Summary

Table 14-98. L3_MAIN TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_DMM_P1	CLK1_DMM_P1_TARG L3_MAIN Physical Address	Address Offset for CLK1_DMM_P2	CLK1_DMM_P2_TARG L3_MAIN Physical Address	Address Offset for CLK1_ABE	CLK1_ABE_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0100	0x4400 0100	0x0000 0200	0x4400 0200	0x0000 0300	0x4400 0300
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0104	0x4400 0104	0x0000 0204	0x4400 0204	0x0000 0304	0x4400 0304
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0108	0x4400 0108	0x0000 0208	0x4400 0208	0x0000 0308	0x4400 0308
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0110	0x4400 0110	0x0000 0210	0x4400 0210	0x0000 0310	0x4400 0310
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0140	0x4400 0140	0x0000 0240	0x4400 0240	0x0000 0340	0x4400 0340
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0144	0x4400 0144	0x0000 0244	0x4400 0244	0x0000 0344	0x4400 0344
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0148	0x4400 0148	0x0000 0248	0x4400 0248	0x0000 0348	0x4400 0348
L3_TARG_STDERRLOG_HDR	R	32	0x0000 014C	0x4400 014C	0x0000 024C	0x4400 024C	0x0000 034C	0x4400 034C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0150	0x4400 0150	0x0000 0250	0x4400 0250	0x0000 0350	0x4400 0350
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0154	0x4400 0154	0x0000 0254	0x4400 0254	0x0000 0354	0x4400 0354
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0158	0x4400 0158	0x0000 0258	0x4400 0258	0x0000 0358	0x4400 0358
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 015C	0x4400 015C	0x0000 025C	0x4400 025C	0x0000 035C	0x4400 035C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0160	0x4400 0160	0x0000 0260	0x4400 0260	0x0000 0360	0x4400 0360
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0164	0x4400 0164	0x0000 0264	0x4400 0264	0x0000 0364	0x4400 0364
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0168	0x4400 0168	0x0000 0268	0x4400 0268	0x0000 0368	0x4400 0368
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 016C	0x4400 016C	0x0000 026C	0x4400 026C	0x0000 036C	0x4400 036C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0180	0x4400 0180	0x0000 0280	0x4400 0280	0x0000 0380	0x4400 0380

Table 14-99. L3_MAIN TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_L4_CFG	CLK1_L4_CFG_TARG L3_MAIN Physical Address	Address Offset for CLK2_GPMC	CLK2_GPMC_TARG L3_MAIN Physical Address	Address Offset for CLK2_OCMC_RAM	CLK2_OCMC_RAM_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0000 0400	0x4400 0400	0x0080 0100	0x4480 0100	0x0080 0200	0x4480 0200
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0000 0404	0x4400 0404	0x0080 0104	0x4480 0104	0x0080 0204	0x4480 0204
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0000 0408	0x4400 0408	0x0080 0108	0x4480 0108	0x0080 0208	0x4480 0208
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0000 0410	0x4400 0410	0x0080 0110	0x4480 0110	0x0080 0210	0x4480 0210
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0440	0x4400 0440	0x0080 0140	0x4480 0140	0x0080 0240	0x4480 0240

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Table 14-99. L3_MAIN TARG Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_L4_CFG	CLK1_L4_CFG_TARG L3_MAIN Physical Address	Address Offset for CLK2_GPMC	CLK2_GPMC_TARG L3_MAIN Physical Address	Address Offset for CLK2_OCMC_RAM	CLK2_OCMC_RAM_TARG L3_MAIN Physical Address
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0000 0444	0x4400 0444	0x0080 0144	0x4480 0144	0x0080 0244	0x4480 0244
L3_TARG_STDERRLOG_MAIN	RW	32	0x0000 0448	0x4400 0448	0x0080 0148	0x4480 0148	0x0080 0248	0x4480 0248
L3_TARG_STDERRLOG_HDR	R	32	0x0000 044C	0x4400 044C	0x0080 014C	0x4480 014C	0x0080 024C	0x4480 024C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0000 0450	0x4400 0450	0x0080 0150	0x4480 0150	0x0080 0250	0x4480 0250
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0000 0454	0x4400 0454	0x0080 0154	0x4480 0154	0x0080 0254	0x4480 0254
L3_TARG_STDERRLOG_INFO	R	32	0x0000 0458	0x4400 0458	0x0080 0158	0x4480 0158	0x0080 0258	0x4480 0258
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0000 045C	0x4400 045C	0x0080 015C	0x4480 015C	0x0080 025C	0x4480 025C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0000 0460	0x4400 0460	0x0080 0160	0x4480 0160	0x0080 0260	0x4480 0260
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0000 0464	0x4400 0464	0x0080 0164	0x4480 0164	0x0080 0264	0x4480 0264
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0000 0468	0x4400 0468	0x0080 0168	0x4480 0168	0x0080 0268	0x4480 0268
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0000 046C	0x4400 046C	0x0080 016C	0x4480 016C	0x0080 026C	0x4480 026C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0000 0480	0x4400 0480	0x0080 0180	0x4480 0180	0x0080 0280	0x4480 0280

Table 14-100. L3_MAIN TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_DSS	CLK2_DSS_TARG L3_MAIN Physical Address	Address Offset for CLK2_ISS	CLK2_ISS_TARG L3_MAIN Physical Address	Address Offset for CLK2_IPU	CLK2_IPU_TARG L3_MAIN Physical Address	CLK1_L4_WKUP_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 0300	0x4480 0300	0x0080 0400	0x4480 0400	0x0080 0500	0x4480 0500	0x4400 0900
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 0304	0x4480 0304	0x0080 0404	0x4480 0404	0x0080 0504	0x4480 0504	0x4400 0904
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 0308	0x4480 0308	0x0080 0408	0x4480 0408	0x0080 0508	0x4480 0508	0x4400 0908
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 0310	0x4480 0310	0x0080 0410	0x4480 0410	0x0080 0510	0x4480 0510	0x4400 0910
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 0340	0x4480 0340	0x0080 0440	0x4480 0440	0x0080 0540	0x4480 0540	0x4400 0940
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 0344	0x4480 0344	0x0080 0444	0x4480 0444	0x0080 0544	0x4480 0544	0x4400 0944
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 0348	0x4480 0348	0x0080 0448	0x4480 0448	0x0080 0548	0x4480 0548	0x4400 0948
L3_TARG_STDERRLOG_HDR	R	32	0x0080 034C	0x4480 034C	0x0080 044C	0x4480 044C	0x0080 054C	0x4480 054C	0x4400 094C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 0350	0x4480 0350	0x0080 0450	0x4480 0450	0x0080 0550	0x4480 0550	0x4400 0950
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 0354	0x4480 0354	0x0080 0454	0x4480 0454	0x0080 0554	0x4480 0554	0x4400 0954
L3_TARG_STDERRLOG_INFO	R	32	0x0080 0358	0x4480 0358	0x0080 0458	0x4480 0458	0x0080 0558	0x4480 0558	0x4400 0958

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Table 14-100. L3_MAIN TARG Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_DSS	CLK2_DSS_TARG L3_MAIN Physical Address	Address Offset for CLK2_ISS	CLK2_ISS_TARG L3_MAIN Physical Address	Address Offset for CLK2_IPU	CLK2_IPU_TARG L3_MAIN Physical Address	CLK1_L4_WKUP_TARG L3_MAIN Physical Address
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 035C	0x4480 035C	0x0080 045C	0x4480 045C	0x0080 055C	0x4480 055C	0x4400 095C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 0360	0x4480 0360	0x0080 0460	0x4480 0460	0x0080 0560	0x4480 0560	0x4400 0960
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 0364	0x4480 0364	0x0080 0464	0x4480 0464	0x0080 0564	0x4480 0564	0x4400 0964
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 0368	0x4480 0368	0x0080 0468	0x4480 0468	0x0080 0568	0x4480 0568	0x4400 0968
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 036C	0x4480 036C	0x0080 046C	0x4480 046C	0x0080 056C	0x4480 056C	0x4400 096C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 0380	0x4480 0380	0x0080 0480	0x4480 0480	0x0080 0580	0x4480 0580	0x4400 0980

Table 14-101. L3_MAIN TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_GPU	CLK2_GPU_TARG L3_MAIN Physical Address	Address Offset for CLK2_IVA_CONFIG	CLK2_IVA_CONFIG_TARG L3_MAIN Physical Address	Address Offset for CLK2_IVA_SL2IF	CLK2_IVA_SL2IF_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 0600	0x4480 0600	0x0080 0700	0x4480 0700	0x0080 0800	0x4480 0800
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 0604	0x4480 0604	0x0080 0704	0x4480 0704	0x0080 0804	0x4480 0804
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 0608	0x4480 0608	0x0080 0708	0x4480 0708	0x0080 0808	0x4480 0808
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 0610	0x4480 0610	0x0080 0710	0x4480 0710	0x0080 0810	0x4480 0810
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 0640	0x4480 0640	0x0080 0740	0x4480 0740	0x0080 0840	0x4480 0840
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 0644	0x4480 0644	0x0080 0744	0x4480 0744	0x0080 0844	0x4480 0844
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 0648	0x4480 0648	0x0080 0748	0x4480 0748	0x0080 0848	0x4480 0848
L3_TARG_STDERRLOG_HDR	R	32	0x0080 064C	0x4480 064C	0x0080 074C	0x4480 074C	0x0080 084C	0x4480 084C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 0650	0x4480 0650	0x0080 0750	0x4480 0750	0x0080 0850	0x4480 0850
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 0654	0x4480 0654	0x0080 0754	0x4480 0754	0x0080 0854	0x4480 0854
L3_TARG_STDERRLOG_INFO	R	32	0x0080 0658	0x4480 0658	0x0080 0758	0x4480 0758	0x0080 0858	0x4480 0858
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 065C	0x4480 065C	0x0080 075C	0x4480 075C	0x0080 085C	0x4480 085C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 0660	0x4480 0660	0x0080 0760	0x4480 0760	0x0080 0860	0x4480 0860
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 0664	0x4480 0664	0x0080 0764	0x4480 0764	0x0080 0864	0x4480 0864
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 0668	0x4480 0668	0x0080 0768	0x4480 0768	0x0080 0868	0x4480 0868

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Table 14-101. L3_MAIN TARG Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_GPU	CLK2_GPU_TARG L3_MAIN Physical Address	Address Offset for CLK2_IVA_CONFIG	CLK2_IVA_CONFIG_TARG L3_MAIN Physical Address	Address Offset for CLK2_IVA_SL2IF	CLK2_IVA_SL2IF_TARG L3_MAIN Physical Address
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 066C	0x4480 066C	0x0080 076C	0x4480 076C	0x0080 086C	0x4480 086C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 0680	0x4480 0680	0x0080 0780	0x4480 0780	0x0080 0880	0x4480 0880

Table 14-102. L3_MAIN TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_L4PER_P0	CLK2_L4PER_P0_TARG L3_MAIN Physical Address	Address Offset for CLK2_L4PER_P1	CLK2_L4PER_P1_TARG L3_MAIN Physical Address	Address Offset for CLK2_L4PER_P2	CLK2_L4PER_P2_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 0900	0x4480 0900	0x0080 0A00	0x4480 0A00	0x0080 0B00	0x4480 0B00
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 0904	0x4480 0904	0x0080 0A04	0x4480 0A04	0x0080 0B04	0x4480 0B04
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 0908	0x4480 0908	0x0080 0A08	0x4480 0A08	0x0080 0B08	0x4480 0B08
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 0910	0x4480 0910	0x0080 0A10	0x4480 0A10	0x0080 0B10	0x4480 0B10
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 0940	0x4480 0940	0x0080 0A40	0x4480 0A40	0x0080 0B40	0x4480 0B40
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 0944	0x4480 0944	0x0080 0A44	0x4480 0A44	0x0080 0B44	0x4480 0B44
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 0948	0x4480 0948	0x0080 0A48	0x4480 0A48	0x0080 0B48	0x4480 0B48
L3_TARG_STDERRLOG_HDR	R	32	0x0080 094C	0x4480 094C	0x0080 0A4C	0x4480 0A4C	0x0080 0B4C	0x4480 0B4C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 0950	0x4480 0950	0x0080 0A50	0x4480 0A50	0x0080 0B50	0x4480 0B50
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 0954	0x4480 0954	0x0080 0A54	0x4480 0A54	0x0080 0B54	0x4480 0B54
L3_TARG_STDERRLOG_INFO	R	32	0x0080 0958	0x4480 0958	0x0080 0A58	0x4480 0A58	0x0080 0B58	0x4480 0B58
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 095C	0x4480 095C	0x0080 0A5C	0x4480 0A5C	0x0080 0B5C	0x4480 0B5C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 0960	0x4480 0960	0x0080 0A60	0x4480 0A60	0x0080 0B60	0x4480 0B60
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 0964	0x4480 0964	0x0080 0A64	0x4480 0A64	0x0080 0B64	0x4480 0B64
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 0968	0x4480 0968	0x0080 0A68	0x4480 0A68	0x0080 0B68	0x4480 0B68
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 096C	0x4480 096C	0x0080 0A6C	0x4480 0A6C	0x0080 0B6C	0x4480 0B6C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 0980	0x4480 0980	0x0080 0A80	0x4480 0A80	0x0080 0B80	0x4480 0B80

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Table 14-103. L3_MAIN TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_L4PER_P3	CLK2_L4PER_P3_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 0C00	0x4480 0C00
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 0C04	0x4480 0C04
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 0C08	0x4480 0C08
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 0C10	0x4480 0C10
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 0C40	0x4480 0C40
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 0C44	0x4480 0C44
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 0C48	0x4480 0C48
L3_TARG_STDERRLOG_HDR	R	32	0x0080 0C4C	0x4480 0C4C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 0C50	0x4480 0C50
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 0C54	0x4480 0C54
L3_TARG_STDERRLOG_INFO	R	32	0x0080 0C58	0x4480 0C58
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 0C5C	0x4480 0C5C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 0C60	0x4480 0C60
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 0C64	0x4480 0C64
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 0C68	0x4480 0C68
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 0C6C	0x4480 0C6C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 0C80	0x4480 0C80

Table 14-104. L3_MAIN TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_BB2D_TARG	CLK2_BB2D_TARG L3_MAIN Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 2200	0x4480 2200
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 2204	0x4480 2204
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 2208	0x4480 2208
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 2210	0x4480 2210
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 2240	0x4480 2240
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 2244	0x4480 2244
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 2248	0x4480 2248
L3_TARG_STDERRLOG_HDR	R	32	0x0080 224C	0x4480 224C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 2250	0x4480 2250
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 2254	0x4480 2254
L3_TARG_STDERRLOG_INFO	R	32	0x0080 2258	0x4480 2258
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 225C	0x4480 225C

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Table 14-104. L3_MAIN TARG Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_BB2D_TARG	CLK2_BB2D_TARG L3_MAIN Physical Address
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 2260	0x4480 2260
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 2264	0x4480 2264
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 2268	0x4480 2268
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 226C	0x4480 226C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 2280	0x4480 2280

Table 14-105. L3_MAIN TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK3_L3_INSTR	CLK3_L3_INSTR_TARG L3_MAIN Physical Address	Address Offse for CLK3_DEBUGSS_CT_TBR_TARG	CLK3_DEBUGSS_CT_TBR_TARG L3_MAIN Physic al Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0100 0100	0x4500 0100	0x0100 0300	0x4500 0300
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0100 0104	0x4500 0104	0x0100 0304	0x4500 0304
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0100 0108	0x4500 0108	0x0100 0308	0x4500 0308
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0100 0110	0x4500 0110	0x0100 0310	0x4500 0310
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0100 0140	0x4500 0140	0x0100 0340	0x4500 0340
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0100 0144	0x4500 0144	0x0100 0344	0x4500 0344
L3_TARG_STDERRLOG_MAIN	RW	32	0x0100 0148	0x4500 0148	0x0100 0348	0x4500 0348
L3_TARG_STDERRLOG_HDR	R	32	0x0100 014C	0x4500 014C	0x0100 034C	0x4500 034C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0100 0150	0x4500 0150	0x0100 0350	0x4500 0350
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0100 0154	0x4500 0154	0x0100 0354	0x4500 0354
L3_TARG_STDERRLOG_INFO	R	32	0x0100 0158	0x4500 0158	0x0100 0358	0x4500 0358
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0100 015C	0x4500 015C	0x0100 035C	0x4500 035C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0100 0160	0x4500 0160	0x0100 0360	0x4500 0360
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0100 0164	0x4500 0164	0x0100 0364	0x4500 0364
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0100 0168	0x4500 0168	0x0100 0368	0x4500 0368
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0100 016C	0x4500 016C	0x0100 036C	0x4500 036C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0100 0180	0x4500 0180	0x0100 0380	0x4500 0380

14.2.5.1.3.2 L3_MAIN TARG Registers Description

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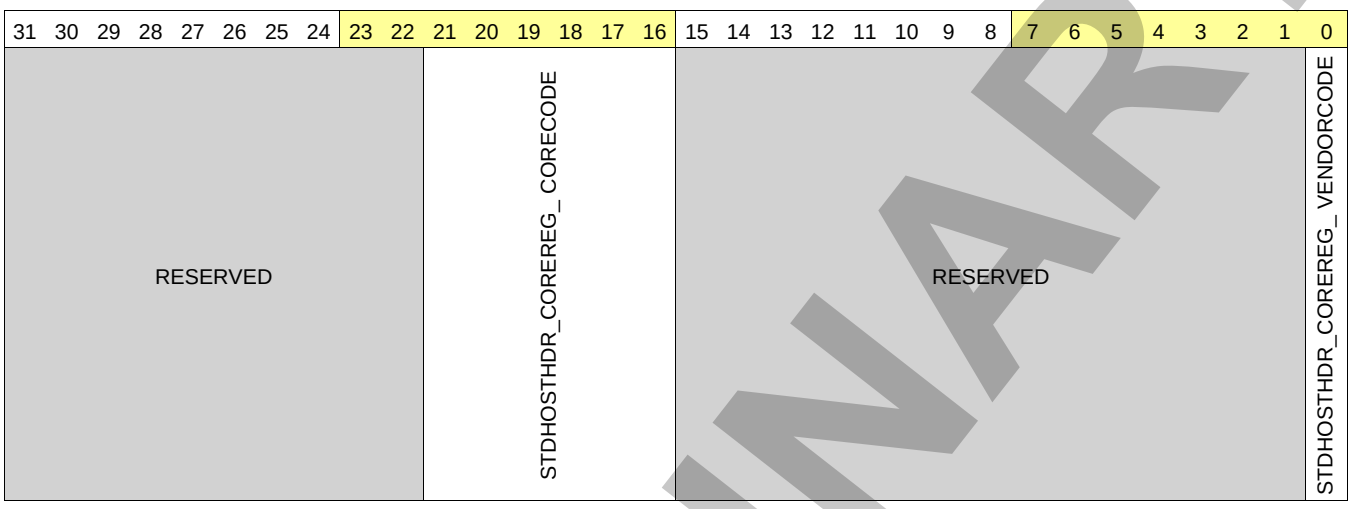
Table 14-106. L3_TARG_STDHOSTHDR_COREREG

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:16	STDHOSTHDR_COREREG_ CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x13.	R	0x13
15:1	RESERVED		R	0x0000
0	STDHOSTHDR_COREREG_ VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-107. Register Call Summary for Register L3_TARG_STDHOSTHDR_COREREG

L3 Interconnect

- L3_MAIN TARG Registers Summary: [0] [1] [2] [3] [4] [5] [7] [8]

Table 14-108. L3_TARG_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																									

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-109. Register Call Summary for Register L3_TARG_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3_MAIN TARG Registers Summary: [0] [1] [2] [3] [4] [5] [7] [8]

Table 14-110. L3_TARG_STDHOSTHDR_MAINCTLREG

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												STDHOSTHDR_MAINCTLREG_CM	STDHOSTHDR_MAINCTLREG_FLT	RESERVED	STDHOSTHDR_MAINCTLREG_EN

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	STDHOSTHDR_MAINCTLREG_CM	Reserved for internal testing. Must be set to 0. Type: Control. Reset value: 0x0.	R	0

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Bits	Field Name	Description	Type	Reset
2	STDHOSTHDR_MAINCTLREG_FLT	Asserted when a Fault condition is detected: if the unit includes Error Logging, Flt is asserted when the FltCnt register field indicates a Fault, and deasserted when FltCnt is reset. If no Error Logging is implemented, this bit becomes unit-dependent. In all cases, Flt bit and Flt pin (service network) have the same logical level. Type: Status. Reset value: X.	R	0
1	RESERVED	Reserved	R	0
0	STDHOSTHDR_MAINCTLREG_EN	Sets the global core enable. Note: A disabled master does not generate any NTTP requests, and a disabled slave replies with an error packet to any request it receives. Type: Control. Reset value: 0x1.	RW	1

Table 14-111. Register Call Summary for Register L3_TARG_STDHOSTHDR_MAINCTLREG

L3 Interconnect

- L3_MAIN TARG Registers Summary: [0] [1] [2] [3] [4] [5] [7] [8]

Table 14-112. L3_TARG_STDHOSTHDR_NTTPADDR_0

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDHOSTHDR_NTTPADDR_0							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	STDHOSTHDR_NTTPADDR_0	Sets the Rx port address. Type: Control. Reset value: 0x15.	R	0x01

Table 14-113. Register Call Summary for Register L3_TARG_STDHOSTHDR_NTTPADDR_0

L3 Interconnect

- L3_MAIN TARG Registers Summary: [0] [1] [2] [3] [4] [5] [7] [8]

Table 14-114. L3_TARG_STDERRLOG_SVRTSTDLVL

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	RW		

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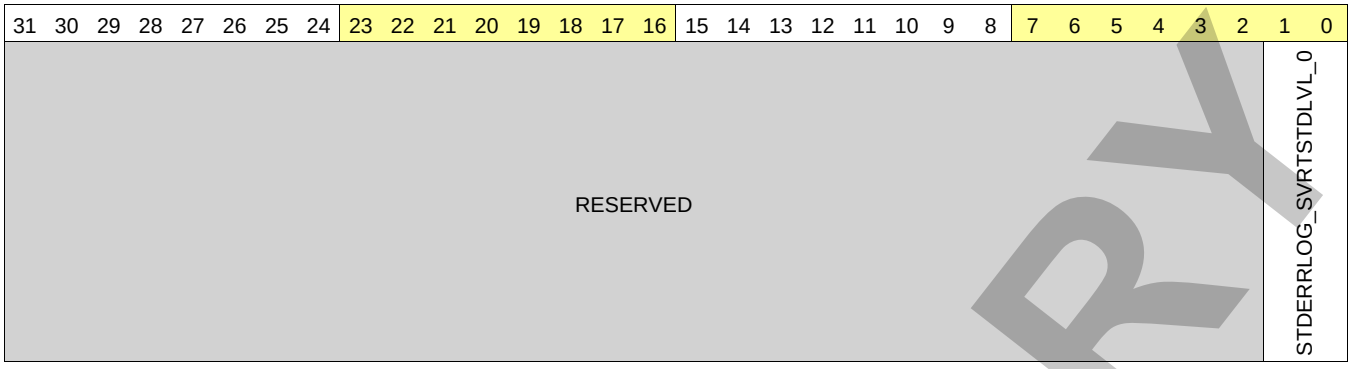


Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_SVRTSTDLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

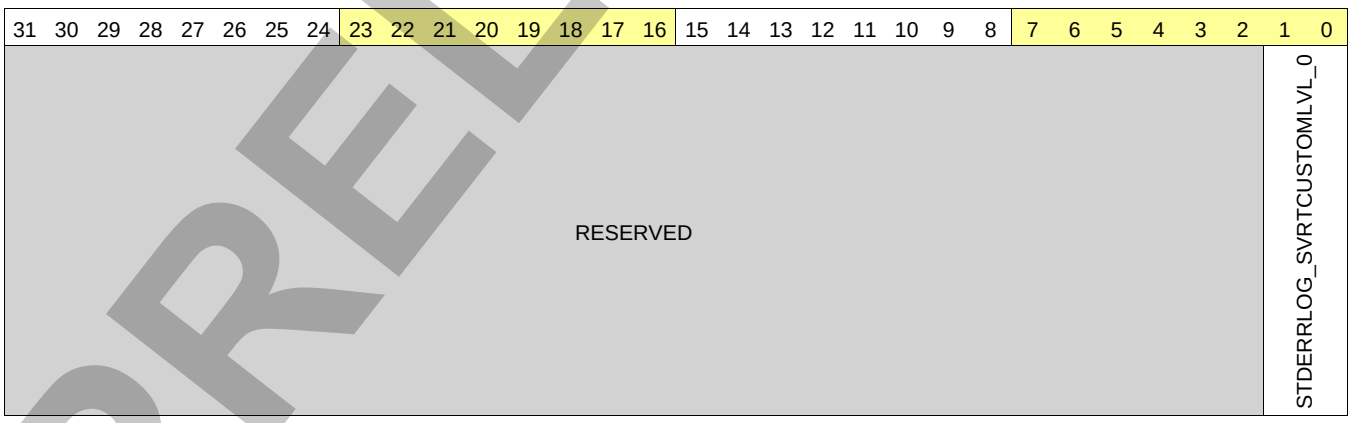
Table 14-115. Register Call Summary for Register L3_TARG_STDERRLOG_SVRTSTDLVL

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [1]
- L3_MAIN TARG Registers Summary: [2] [3] [4] [5] [6] [7] [9] [10]

Table 14-116. L3_TARG_STDERRLOG_SVRTCUSTOMLVL

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_SVRTCUSTOMLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

Table 14-117. Register Call Summary for Register L3_TARG_STDERRLOG_SVRTCUSTOMLVL

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Registers Summary: [1] [2] [3] [4] [5] [6] [8] [9]

Table 14-118. L3_TARG_STDERRLOG_MAIN

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_MAIN_CLRLOG	RESERVED											STDERRLOG_MAIN_FLTCNT	STDERRLOG_MAIN_ERRCNT	RESERVED																	STDERRLOG_MAIN_ERRTYPE	STDERRLOG_MAIN_ERRLOGVLD

Bits	Field Name	Description	Type	Reset
31	STDERRLOG_MAIN_CLRLOG	Clears "Error Logging Valid" bit when written to 1. Type: Give_AutoCleared. Reset value: 0x0.	RW	0
30:20	RESERVED	Reserved	R	0x000
19	STDERRLOG_MAIN_FLTCNT	Asserted when at least one error with severity level FAULT is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
18	STDERRLOG_MAIN_ERRCNT	Asserted when at least one error with severity level ERROR is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
17:2	RESERVED	Reserved	R	0x0000
1	STDERRLOG_MAIN_ERRTYPE	Indicates logging type. Type: Status. Reset value: X. Read 0x0: Logged Error format is standard (header and necker recorded). Read 0x1: Logged Error format is module dependent. CustomInfo register(s) may be implemented to store additional information.	R	0
0	STDERRLOG_MAIN_ERRLOGVLD	Error Logging Valid. Asserted when logging information is valid(indicates that an error has been logged). Type: Status. Reset value: X.	R	0

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Table 14-119. Register Call Summary for Register L3_TARG_STDERRLOG_MAIN

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [1] [2] [3] [4] [5] [6]
- L3_MAIN TARG Registers Summary: [7] [8] [9] [10] [11] [12] [14] [15]

Table 14-120. L3_TARG_STDERRLOG_HDR

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDERRLOG_HDR_LEN1						RESERVED		STDERRLOG_HDR_STOPOFSWRPSZ				STDERRLOG_HDR_ERR	RESERVED			STDERRLOG_HDR_PRESSURE	RESERVED			STDERRLOG_HDR_OPCODE			

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:18	STDERRLOG_HDR_LEN1	This field contains the number of payload cell(s) minus one of the logged packet. Type: Status. Reset value: X.	R	0x00
17:16	RESERVED	Reserved	R	0x0
15:12	STDERRLOG_HDR_STOPOFSWRPSZ	StopOfs or WrapSize field of the logged packet (meaning depends on Wrp bit of logged opcode). Type: Status. Reset value: X.	R	0x0
11	STDERRLOG_HDR_ERR	Err bit of the logged packet. Type: Status. Reset value: X.	R	0
10:7	RESERVED	Reserved	R	0x0
6	STDERRLOG_HDR_PRESSURE	Pressure field of the logged packet. Type: Status. Reset value: X.	R	0
5:4	RESERVED	Reserved	R	0x0
3:0	STDERRLOG_HDR_OPCODE	Opcode of the logged packet. Type: Status. Reset value: X.	R	0x0

Table 14-121. Register Call Summary for Register L3_TARG_STDERRLOG_HDR

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Registers Summary: [1] [2] [3] [4] [5] [6] [8] [9]

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Table 14-122. L3_TARG_STDERRLOG_MSTADDR

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					STDERRLOG_MSTADDR										

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10:0	STDERRLOG_MSTADDR	Master Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-123. Register Call Summary for Register L3_TARG_STDERRLOG_MSTADDR

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Registers Summary: [1] [2] [3] [4] [5] [6] [8] [9]

Table 14-124. L3_TARG_STDERRLOG_SLVADDR

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													STDERRLOG_SLVADDR		

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	STDERRLOG_SLVADDR	Slave Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-125. Register Call Summary for Register L3_TARG_STDERRLOG_SLVADDR

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Registers Summary: [1] [2] [3] [4] [5] [6] [8] [9]

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Table 14-126. L3_TARG_STDERRLOG_INFO

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_INFO	Info field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-127. Register Call Summary for Register L3_TARG_STDERRLOG_INFO

L3 Interconnect

- Severity Level of Standard and Custom Errors: [0]
- L3_MAIN TARG Registers Summary: [1] [2] [3] [4] [5] [6] [8] [9]

Table 14-128. L3_TARG_STDERRLOG_SLVOFSLSB

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_SLVOFSLSB																															

Bits	Field Name	Description	Type	Reset
31:0	STDERRLOG_SLVOFSLSB	LSB of the "slave offset" field, concatenated with "start offset" field of the logged packet. Type: Status. Reset value: X.	R	0x0000 0000

Table 14-129. Register Call Summary for Register L3_TARG_STDERRLOG_SLVOFSLSB

L3 Interconnect

- L3_MAIN TARG Registers Summary: [0] [1] [2] [3] [4] [5] [7] [8]

Table 14-130. L3_TARG_STDERRLOG_SLVOFSMSB

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_SLVOFSMSB

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	STDERRLOG_SLVOFSMSB	MSB of the "slave offset" field of the logged packet (according to NTTP packet format, this register field may exceed the actual "slave offset" size. Unused bits are stuck at 0, if any). Type: Status. Reset value: X.	R	0

Table 14-131. Register Call Summary for Register L3_TARG_STDERRLOG_SLVOFSMSB

L3 Interconnect

- L3_MAIN TARG Registers Summary: [0] [1] [2] [3] [4] [5] [7] [8]

Table 14-132. L3_TARG_STDERRLOG_CUSTOMINFO_INFO

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_CUSTOMINFO_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_CUSTOMINFO_INFO	Info field of the response packet. Type: Status. Reset value: X.	R	0x00

Table 14-133. Register Call Summary for Register L3_TARG_STDERRLOG_CUSTOMINFO_INFO

L3 Interconnect

- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [0]
- L3_MAIN TARG Registers Summary: [1] [2] [3] [4] [5] [6] [8] [9]

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Table 14-134. L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					STDERRLOG_CUSTOMINFO_MSTADDR									

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10:0	STDERRLOG_CUSTOMINFO_MSTADDR	MstAddr field of the response packet. Type: Status. Reset value: X.	R	0x00

Table 14-135. Register Call Summary for Register L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR

L3 Interconnect

- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [0]
- L3_MAIN TARG Registers Summary: [1] [2] [3] [4] [5] [6] [8] [9]

Table 14-136. L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_CUSTOMINFO_OPCODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_CUSTOMINFO_OPCODE	Opcode of the response packet. Type: Status. Reset value: X.	R	0x0

Table 14-137. Register Call Summary for Register L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE

L3 Interconnect

- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [0]
- L3_MAIN TARG Registers Summary: [1] [2] [3] [4] [5] [6] [8] [9]

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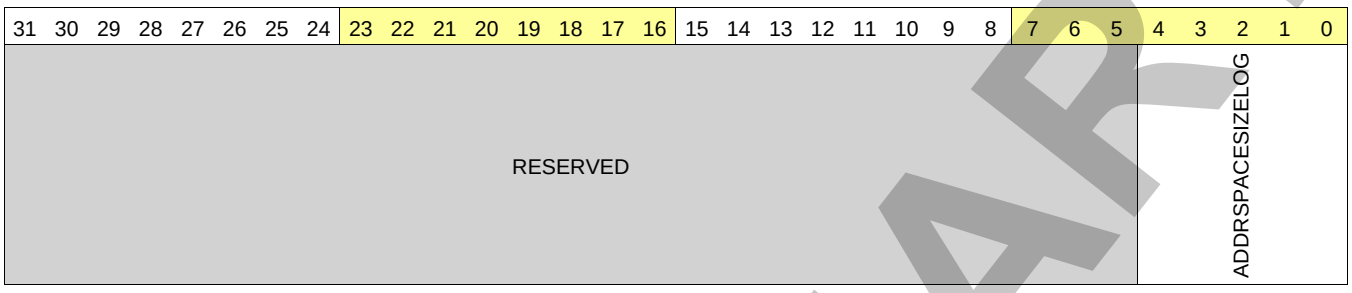
Table 14-138. L3_TARG_ADDRSPACESIZELOG

Address Offset	See Table 14-98.	**Index**	
Physical Address	See Table 14-98 to Table 14-105	**Instance**	See Table 14-98 to Table 14-105
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	ADDRSPACESIZELOG	The address space size is equal to 2**AddrSpaceSizeLog * 4K in bytes. Type: Control. Reset value: 0x1F.	RW	0x1F

Table 14-139. Register Call Summary for Register L3_TARG_ADDRSPACESIZELOG

L3 Interconnect

- L3_MAIN TARG Registers Summary: [0] [1] [2] [3] [4] [5] [7] [8]

14.2.5.1.4 L3_MAIN PWR_DISC Register Summary and Description

Table 14-140. PWR_DISC Instance Summary

Module Name	Base Address	Size
CLK1_CLK1_TARG_PWR_DISC_CLK2	0x4400 0600	4KiB
CLK2_CLK2_TARG_PWR_DISC_CLK1	0x4480 1100	4KiB

14.2.5.1.4.1 L3_MAIN PWR_DISC Register Summary

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Table 14-141. PWR_DISC Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_CLK1_TARG_PWR_DISC_CLK2	CLK1_CLK1_TARG_PWR_DISC_CLK2 L3_MAIN Physical Address	Address Offset for CLK2_CLK2_TARG_PWR_DISC_CLK`	CLK2_CLK2_TARG_PWR_DISC_CLK1 L3_MAIN Physical Address
L3_PWR_DISC_STDHOSTHDR_COREREG	R	32	0x0000 0600	0x4400 0600	0x0080 1100	0x4480 1100
L3_PWR_DISC_STDHOSTHDR_VERSIONREG	R	32	0x0000 0604	0x4400 0604	0x0080 1104	0x4480 1104
L3_PWR_DISC_STDHOSTHDR_MAINCTLREG	R	32	0x0000 0608	0x4400 0608	0x0080 1108	0x4480 1108
L3_PWR_DISC_STDERRLOG_SVRTSTDLVL	RW	32	0x0000 0640	0x4400 0640	0x0080 1140	0x4480 1140
L3_PWR_DISC_STDERRLOG_MAIN	RW	32	0x0000 0648	0x4400 0648	0x0080 1148	0x4480 1148
L3_PWR_DISC_STDERRLOG_HDR	R	32	0x0000 064C	0x4400 064C	0x0080 114C	0x4480 114C
L3_PWR_DISC_STDERRLOG_MSTADDR	R	32	0x0000 0650	0x4400 0650	0x0080 1150	0x4480 1150
L3_PWR_DISC_STDERRLOG_SLVADDR	R	32	0x0000 0654	0x4400 0654	0x0080 1154	0x4480 1154
L3_PWR_DISC_STDERRLOG_INFO	R	32	0x0000 0658	0x4400 0658	0x0080 1158	0x4480 1158
L3_PWR_DISC_STDERRLOG_SLVOFSLSB	R	32	0x0000 065C	0x4400 065C	0x0080 115C	0x4480 115C
L3_PWR_DISC_STDERRLOG_SLVOFSMSB	R	32	0x0000 0660	0x4400 0660	0x0080 1160	0x4480 1160

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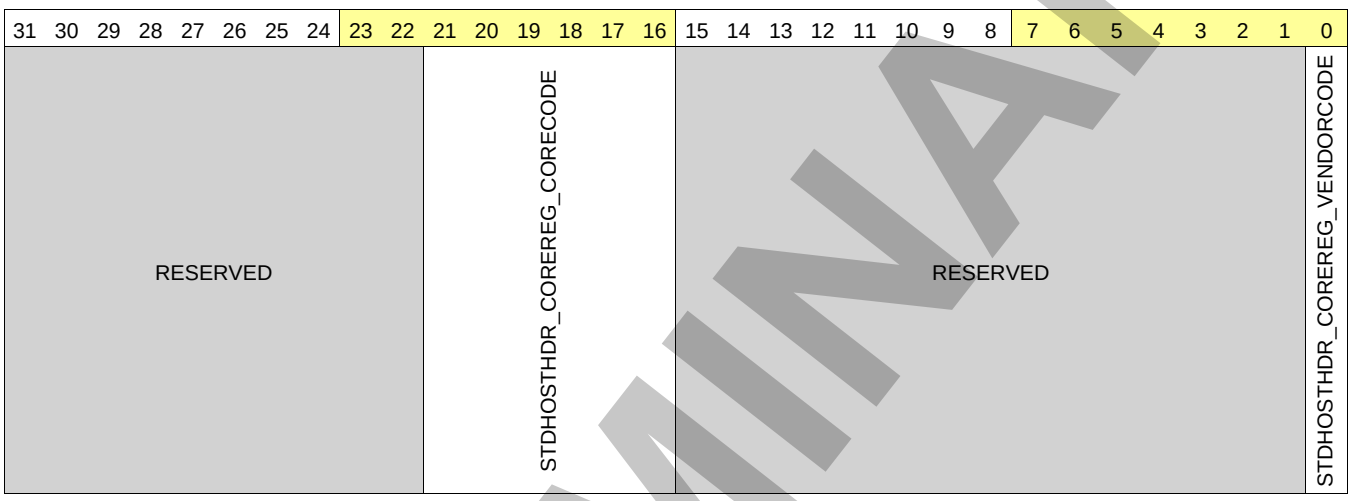
14.2.5.1.4.2 L3_MAIN PWR_DISC Register Description

Table 14-142. L3_PWR_DISC_STDHOSTHDR_COREREG

Address Offset	See Table 14-141.		
Physical Address	0x4400 0600 0x4480 1100	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:22	RESERVED	RESERVED	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x38.	R	0x38
15:1	RESERVED	RESERVED	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-143. Register Call Summary for Register L3_PWR_DISC_STDHOSTHDR_COREREG

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

Table 14-144. L3_PWR_DISC_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-141.		
Physical Address	0x4400 0604 0x4480 1104	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																									

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-145. Register Call Summary for Register L3_PWR_DISC_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

Table 14-146. L3_PWR_DISC_STDHOSTHDR_MAINCTLREG

Address Offset	See Table 14-141.		
Physical Address	0x4400 0608 0x4480 1108	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												STDHOSTHDR_MAINCTLREG_CM	STDHOSTHDR_MAINCTLREG_FLT	RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	STDHOSTHDR_MAINCTLREG_CM	Reserved for internal testing. Must be set to 0. Type: Control. Reset value: 0x0.	R	0

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Bits	Field Name	Description	Type	Reset
2	STDHOSTHDR_MAINCTLREG_FLT	Asserted when a Fault condition is detected: if the unit includes Error Logging, Flt is asserted when the FltCnt register field indicates a Fault, and deasserted when FltCnt is reset. If no Error Logging is implemented, this bit becomes unit-dependent. In all cases, Flt bit and Flt pin (service network) have the same logical level. Type: Status. Reset value: X.	R	0
1:0	RESERVED	Reserved	R	0x0

Table 14-147. Register Call Summary for Register L3_PWR_DISC_STDHOSTHDR_MAINCTLREG

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

Table 14-148. L3_PWR_DISC_STDERRLOG_SVRTSTDLVL

Address Offset	See Table 14-141.		
Physical Address	0x4400 0640 0x4480 1140	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														STDERRLOG_SVRTSTDLVL_0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	STDERRLOG_SVRTSTDLVL_0	Severity level parameters Type: Control. Reset value: 0x2. 0x0: Error logging is disabled. 0x1: Errors are logged with severity level Error. 0x2: Errors are logged with severity level Fault.	RW	0x2

Table 14-149. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_SVRTSTDLVL

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

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Table 14-150. L3_PWR_DISC_STDERRLOG_MAIN

Address Offset	See Table 14-141.		
Physical Address	0x4400 0648 0x4480 1148	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_MAIN_CLRLOG	RESERVED											STDERRLOG_MAIN_FLTCNT	STDERRLOG_MAIN_ERRCNT	RESERVED																	STDERRLOG_MAIN_ERRTYPE	STDERRLOG_MAIN_ERRLOGVLD

Bits	Field Name	Description	Type	Reset
31	STDERRLOG_MAIN_CLRLOG	Clears "Error Logging Valid" bit when written to 1. Type: Give_AutoCleared. Reset value: 0x0.	RW	0
30:20	RESERVED	Reserved	R	0x000
19	STDERRLOG_MAIN_FLTCNT	Asserted when at least one error with severity level FAULT is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
18	STDERRLOG_MAIN_ERRCNT	Asserted when at least one error with severity level ERROR is detected. Reset when written to 1. Type: Take. Reset value: 0x0.	RW	0
17:2	RESERVED	Reserved	R	0x0000
1	STDERRLOG_MAIN_ERRTYPE	Indicates logging type. Type: Status. Reset value: X. Read 0x0: Logged Error format is standard (header and necker recorded). Read 0x1: Logged Error format is module dependent. CustomInfo register(s) may be implemented to store additional information.	R	0
0	STDERRLOG_MAIN_ERRLOGVLD	Error Logging Valid. Asserted when logging information is valid(indicates that an error has been logged). Type: Status. Reset value: X.	R	0

Table 14-151. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_MAIN

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

Table 14-152. L3_PWR_DISC_STDERRLOG_HDR

Address Offset	See Table 14-141.		
Physical Address	0x4400 064C 0x4480 114C	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

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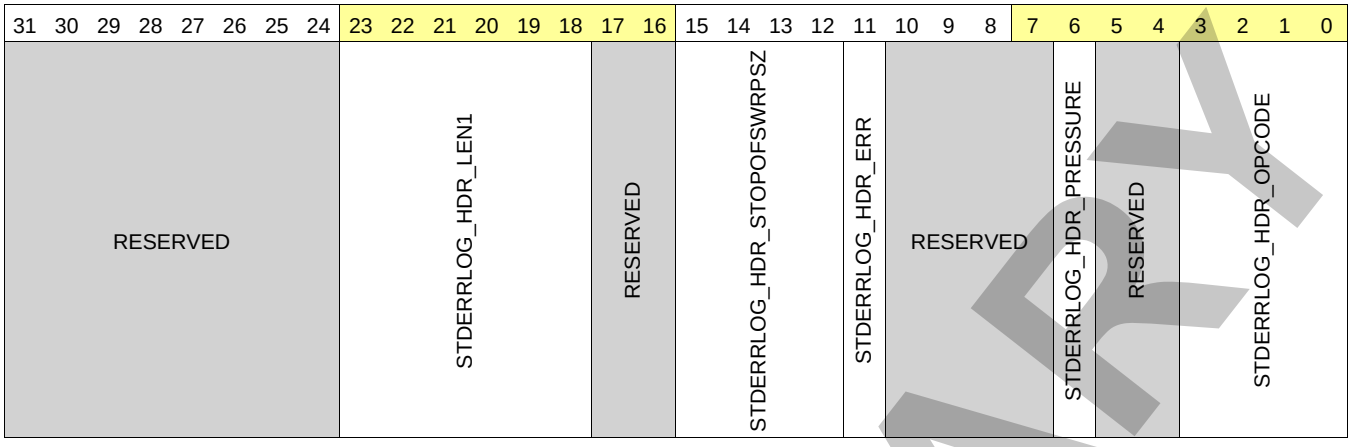


Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:18	STDERRLOG_HDR_LEN1	This field contains the number of payload cell(s) minus one of the logged packet. Type: Status. Reset value: X.	R	0x00
17:16	RESERVED	Reserved	R	0x0
15:12	STDERRLOG_HDR_STOPOFSWRPSZ	StopOfs or WrapSize field of the logged packet (meaning depends on Wrp bit of logged opcode). Type: Status. Reset value: X.	R	0x0
11	STDERRLOG_HDR_ERR	Err bit of the logged packet. Type: Status. Reset value: X.	R	0
10:7	RESERVED	Reserved	R	0x0
6	STDERRLOG_HDR_PRESSURE	Pressure field of the logged packet. Type: Status. Reset value: X.	R	0
5:4	RESERVED	Reserved	R	0x0
3:0	STDERRLOG_HDR_OPCODE	Opcode of the logged packet. Type: Status. Reset value: X.	R	0x0

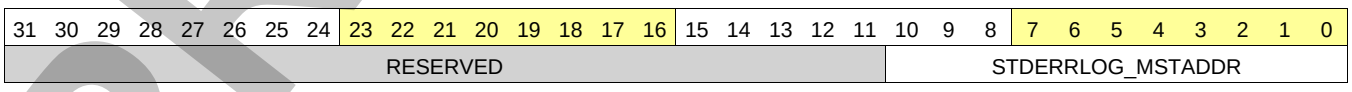
Table 14-153. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_HDR

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

Table 14-154. L3_PWR_DISC_STDERRLOG_MSTADDR

Address Offset	See Table 14-141.		
Physical Address	0x4400 0650 0x4480 1150	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10:0	STDERRLOG_MSTADDR	Master Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

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Table 14-155. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_MSTADDR

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

Table 14-156. L3_PWR_DISC_STDERRLOG_SLVADDR

Address Offset	See Table 14-141.		
Physical Address	0x4400 0654 0x4480 1154	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_SLVADDR							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	STDERRLOG_SLVADDR	Slave Address field of the logged packet. Type: Status. Reset value: X.	R	0x00

Table 14-157. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_SLVADDR

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

Table 14-158. L3_PWR_DISC_STDERRLOG_INFO

Address Offset	See Table 14-141.		
Physical Address	0x4400 0658 0x4480 1158	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STDERRLOG_INFO							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STDERRLOG_INFO	Info field of the logged packet. Type: Status. Reset value: X.	R	0x00

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Table 14-159. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_INFO

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

Table 14-160. L3_PWR_DISC_STDERRLOG_SLVOFSLSB

Address Offset	See Table 14-141.		
Physical Address	0x4400 065C 0x4480 115C	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDERRLOG_SLVOFSLSB																															

Bits	Field Name	Description	Type	Reset
31:0	STDERRLOG_SLVOFSLSB	LSB of the "slave offset" field, concatenated with "start offset" field of the logged packet. Type: Status. Reset value: X.	R	0x0000 0000

Table 14-161. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_SLVOFSLSB

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

Table 14-162. L3_PWR_DISC_STDERRLOG_SLVOFSMSB

Address Offset	See Table 14-141.		
Physical Address	0x4400 0660 0x4480 1160	**Instance**	CLK1_CLK1_TARG_PWR_DISC_CLK2 CLK2_CLK2_TARG_PWR_DISC_CLK1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															STDERRLOG_SLVOFSMSB

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	STDERRLOG_SLVOFSMSB	MSB of the "slave offset" field of the logged packet (according to NTTP packet format, this register field may exceed the actual "slave offset" size. Unused bits are stuck at 0, if any). Type: Status. Reset value: X.	R	0

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Table 14-163. Register Call Summary for Register L3_PWR_DISC_STDERRLOG_SLVOFSMSB

L3 Interconnect

- L3_MAIN PWR_DISC Register Summary: [0]

14.2.5.1.5 L3_MAIN FLAGMUX Register Summary and Description

Table 14-164. FLAGMUX Instance Summary

Module Name	Base Address	Size
CLK1_FLAGMUX_CLK1	0x4400 0500	4KiB
CLK2_FLAGMUX_CLK2	0x4480 1000	4KiB
CLK3_FLAGMUX_CLK3	0x4500 0200	4KiB

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14.2.5.1.5.1 L3_MAIN FLAGMUX Register Summary

Table 14-165. FLAGMUX Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1	CLK1_FLAGMUX_CLK1 L3_MAIN Physical Address
L3_FLAGMUX_STDHOSTHDR_COREREG	R	32	0x0000 0500	0x4400 0500
L3_FLAGMUX_STDHOSTHDR_VERSIONREG	R	32	0x0000 0504	0x4400 0504
L3_FLAGMUX_MASK0	RW	32	0x0000 0508	0x4400 0508
L3_FLAGMUX_REGERR0	R	32	0x0000 050C	0x4400 050C
L3_FLAGMUX_MASK1	RW	32	0x0000 0510	0x4400 0510
L3_FLAGMUX_REGERR1	RW	32	0x0000 0514	0x4400 0514
L3_FLAGMUX_TIMEOUT_STDHOSTHDR_COREREG	R	32	0x0000 1000	0x4400 1000
L3_FLAGMUX_TIMEOUT_STDHOSTHDR_VERSIONREG	R	32	0x0000 1004	0x4400 1004
L3_FLAGMUX_TIMEOUT_MASK0	RW	32	0x0000 1008	0x4400 1008
L3_FLAGMUX_TIMEOUT_REGERR0	R	32	0x0000 100C	0x4400 100C

Table 14-166. FLAGMUX Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2	CLK2_FLAGMUX_CLK2 L3_MAIN Physical Address	Address Offset for CLK3	CLK3_FLAGMUX_CLK3 L3_MAIN Physical Address
L3_FLAGMUX_STDHOSTHDR_COREREG	R	32	0x0080 1000	0x4480 1000	0x0100 0200	0x4500 0200
L3_FLAGMUX_STDHOSTHDR_VERSIONREG	R	32	0x0080 1004	0x4480 1004	0x0100 0204	0x4500 0204
L3_FLAGMUX_MASK0	RW	32	0x0080 1008	0x4480 1008	0x0100 0208	0x4500 0208
L3_FLAGMUX_REGERR0	R	32	0x0080 100C	0x4480 100C	0x0100 0210	0x4500 020C
L3_FLAGMUX_MASK1	RW	32	0x0080 1010	0x4480 1010	0x0100 0240	0x4500 0210
L3_FLAGMUX_REGERR1	RW	32	0x0080 1014	0x4480 1014	0x0100 0244	0x4500 0214
L3_FLAGMUX_TIMEOUT_STDHOSTHDR_COREREG	R	32	0x0080 2300	0x4480 2300	0x0100 0500	0x4500 0500
L3_FLAGMUX_TIMEOUT_STDHOSTHDR_VERSIONREG	R	32	0x0080 2304	0x4480 2304	0x0100 0504	0x4500 0504
L3_FLAGMUX_TIMEOUT_MASK0	RW	32	0x0080 2308	0x4480 2308	0x0100 0508	0x4500 0508
L3_FLAGMUX_TIMEOUT_REGERR0	R	32	0x0080 230C	0x4480 230C	0x0100 050C	0x4500 050C

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14.2.5.1.5.2 L3_MAIN FLAGMUX Register Description

Table 14-167. L3_FLAGMUX_STDHOSTHDR_COREREG

Address Offset	See Table 14-165.		
Physical Address	0x4400 0500 0x4480 1000 0x4500 0200	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x37.	R	0x37
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-168. Register Call Summary for Register L3_FLAGMUX_STDHOSTHDR_COREREG

L3 Interconnect

- L3_MAIN FLAGMUX Register Summary: [0] [1]

Table 14-169. L3_FLAGMUX_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-165.		
Physical Address	0x4400 0504 0x4480 1004 0x4500 0204	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																									

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-170. Register Call Summary for Register L3_FLAGMUX_STDHOSTHDR_VERSIONREG

L3 Interconnect

- Flag Muxing: [0]
- L3_MAIN FLAGMUX Register Summary: [1] [2]

Table 14-171. L3_FLAGMUX_MASK0

Address Offset	See Table 14-165.		
Physical Address	0x4400 0508 0x4480 1008 0x4500 0208	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MASK0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x0000
7:0	MASK0	Mask flag inputs 0 Type: Control. Reset value: 0x7F	RW	0x7F FFFF

Table 14-172. Register Call Summary for Register L3_FLAGMUX_MASK0

L3 Interconnect

- Flag Mux Error Logging: [0]
- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [1]
- L3_MAIN FLAGMUX Register Summary: [2] [3]

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Table 14-173. L3_FLAGMUX_REGERR0

Address Offset	See Table 14-165.		
Physical Address	0x4400 050C 0x4480 100C 0x4500 020C	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REGERR0							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x0000
7:0	REGERR0	Flag inputs 0 Type: Status. Reset value: X.	R	0x00000

Table 14-174. Register Call Summary for Register L3_FLAGMUX_REGERR0

L3 Interconnect

- Flag Muxing: [0]
- Flag Mux Error Logging: [1]
- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [2] [3] [4]
- L3_MAIN FLAGMUX Register Summary: [5] [6]

Table 14-175. L3_FLAGMUX_MASK1

Address Offset	See Table 14-165.		
Physical Address	0x4400 0510 0x4480 1010 0x4500 0210	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MASK1							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x0000
7:0	MASK1	Mask flag inputs 1 Type: Control. Reset value: 0x7FFFFF.	RW	0x7F FFFF

Table 14-176. Register Call Summary for Register L3_FLAGMUX_MASK1

L3 Interconnect

- Flag Mux Error Logging: [0]
- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [1]
- L3_MAIN FLAGMUX Register Summary: [2] [3]

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Table 14-177. L3_FLAGMUX_REGERR1

Address Offset	See Table 14-165.		
Physical Address	0x4400 0514 0x4480 1014 0x4500 0214	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REGERR1							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x0000
7:0	REGERR1	Flag inputs 1 Type: Status. Reset value: X.	R	0x00000

Table 14-178. Register Call Summary for Register L3_FLAGMUX_REGERR1

L3 Interconnect

- Flag Muxing: [0]
- Flag Mux Error Logging: [1]
- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [2] [3] [4]
- L3_MAIN FLAGMUX Register Summary: [5] [6]

Table 14-179. L3_FLAGMUX_TIMEOUT_STDHOSTHDR_COREREG

Address Offset	See Table 14-165.		
Physical Address	0x4400 1000 0x4480 2300 0x4500 0500	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0bxx xxxx xxxx
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constantreporting a vendor-specific core generator code. Type: Constant. Reset value: 0x37.	R	0x37
15:1	RESERVED		R	0bxxx xxxx xxxx xxxx

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Bits	Field Name	Description	Type	Reset
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constantreporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x1: Read 0x0: Third-party vendor.	R	1

Table 14-180. Register Call Summary for Register L3_FLAGMUX_TIMEOUT_STDHOSTHDR_COREREG

L3 Interconnect

- L3_MAIN FLAGMUX Register Summary: [0] [1]

Table 14-181. L3_FLAGMUX_TIMEOUT_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-165.		
Physical Address	0x4400 1004 0x4480 2304 0x4500 0504	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constantreporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x-- ----

Table 14-182. Register Call Summary for Register L3_FLAGMUX_TIMEOUT_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3_MAIN FLAGMUX Register Summary: [0] [1]

Table 14-183. L3_FLAGMUX_TIMEOUT_MASK0

Address Offset	See Table 14-165.		
Physical Address	0x4400 1008 0x4480 2308 0x4500 0508	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3

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Table 14-183. L3_FLAGMUX_TIMEOUT_MASK0 (continued)

Description	
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MASK0	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
4:0	MASK0	mask flag inputs 0 Type: Control. Reset value: 0x0.	RW	0x00

Table 14-184. Register Call Summary for Register L3_FLAGMUX_TIMEOUT_MASK0

L3 Interconnect

- Flag Mux Time-out: [0] [1] [2]
- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [3]
- L3_MAIN FLAGMUX Register Summary: [4] [5]

Table 14-185. L3_FLAGMUX_TIMEOUT_REGERR0

Address Offset	See Table 14-165.		
Physical Address	0x4400 100C 0x4480 230C 0x4500 050C	**Instance**	CLK1_FLAGMUX_CLK1 CLK2_FLAGMUX_CLK2 CLK3_FLAGMUX_CLK3
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														REGERR0	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
4:0	REGERR0	flag inputs 0 Type: Status. Reset value: X.	R	0bx xxxx

Table 14-186. Register Call Summary for Register L3_FLAGMUX_TIMEOUT_REGERR0

L3 Interconnect

- Flag Mux Time-out: [0]
- Main Sequence: L3_MAIN Interconnect Error Analysis Mode: [1]
- L3_MAIN FLAGMUX Register Summary: [2] [3]

14.2.5.1.6 L3_MAIN BW Regulator Register Summary and Description

Table 14-187. BW_REGULATOR Instance Summary

Module Name	Base Address	Size
CLK2_IVA_BW_REGULATOR	0x4480 1400	256 bytes
CLK2_GPU_P1_BW_REGULATOR	0x4480 1500	256B
CLK2_GPU_P2_BW_REGULATOR	0x4480 1900	256B
CLK2_BB2D_P1_BW_REGULATOR	0x4480 2000	256B

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Table 14-187. BW_REGULATOR Instance Summary (continued)

Module Name	Base Address	Size
CLK2_BB2D_P2_BW_REGULATOR	0x4480 2100	256B

14.2.5.1.6.1 L3_MAIN BW Regulator Register Summary

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Table 14-188. BW_REGULATOR Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_IVA_BW_REGULATOR	CLK2_IVA_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0080 1400	0x4480 1400
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0080 1404	0x4480 1404
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0080 1408	0x4480 1408
L3_BW_REGULATOR_WATERMARK	RW	32	0x0080 140C	0x4480 140C
L3_BW_REGULATOR_PRESS	R	32	0x0080 1410	0x4480 1410
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0080 1414	0x4480 1414

Table 14-189. BW_REGULATOR Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_GPU_P1_BW_REGULATOR	CLK2_GPU_P1_BW_REGULATOR L3_MAIN Physical Address	Address Offset for CLK2_GPU_P2_BW_REGULATOR	CLK2_GPU_P2_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0080 1500	0x4480 1500	0x0080 1900	0x4480 1900
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0080 1504	0x4480 1504	0x0080 1904	0x4480 1904
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0080 1508	0x4480 1508	0x0080 1908	0x4480 1908
L3_BW_REGULATOR_WATERMARK	RW	32	0x0080 150C	0x4480 150C	0x0080 190C	0x4480 190C
L3_BW_REGULATOR_PRESS	R	32	0x0080 1510	0x4480 1510	0x0080 1910	0x4480 1910
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0080 1514	0x4480 1514	0x0080 1914	0x4480 1914

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Table 14-190. BW_REGULATOR Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_BB2D_P1_BW_REGULATOR	CLK2_BB2D_P1_BW_REGULATOR L3_MAIN Physical Address	Address Offset for CLK2_BB2D_P2_BW_REGULATOR	CLK2_BB2D_P2_BW_REGULATOR L3_MAIN Physical Address
L3_BW_REGULATOR_STDHOSTHDR_COREREG	R	32	0x0080 2000	0x4480 2000	0x0080 2100	0x4480 2100
L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG	R	32	0x0080 2004	0x4480 2004	0x0080 2104	0x4480 2104
L3_BW_REGULATOR_BANDWIDTH	RW	32	0x0080 2008	0x4480 2008	0x0080 2108	0x4480 2108
L3_BW_REGULATOR_WATERMARK	RW	32	0x0080 200C	0x4480 200C	0x0080 210C	0x4480 210C
L3_BW_REGULATOR_PRESS	R	32	0x0080 2010	0x4480 2010	0x0080 2110	0x4480 2110
L3_BW_REGULATOR_CLEARHISTORY	RW	32	0x0080 2014	0x4480 2014	0x0080 2114	0x4480 2114

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14.2.5.1.6.2 L3_MAIN BW Regulator Register Description

Table 14-191. L3_BW_REGULATOR_STDHOSTHDR_COREREG

Address Offset	See Table 14-188.		
Physical Address	0x4480 1400 0x4480 1500 0x4480 1900 0x4480 2000 0x4480 2100	**Instance**	CLK2_IVA_BW_REGULATOR CLK2_GPU_P1_BW_REGULATOR CLK2_GPU_P2_BW_REGULATOR CLK2_BB2D_P1_BW_REGULATOR CLK2_BB2D_P2_BW_REGULATOR
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x31.	R	0x31
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-192. Register Call Summary for Register L3_BW_REGULATOR_STDHOSTHDR_COREREG

L3 Interconnect

- L3_MAIN BW Regulator Register Summary: [0] [1] [2]

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Table 14-193. L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-188.		
Physical Address	0x4480 1404 0x4480 1504 0x4480 1904 0x4480 2004 0x4480 2104	**Instance**	CLK2_IVA_BW_REGULATOR CLK2_GPU_P1_BW_REGULATOR CLK2_GPU_P2_BW_REGULATOR CLK2_BB2D_P1_BW_REGULATOR CLK2_BB2D_P2_BW_REGULATOR
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																									

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-194. Register Call Summary for Register L3_BW_REGULATOR_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3_MAIN BW Regulator Register Summary: [0] [1] [2]

Table 14-195. L3_BW_REGULATOR_BANDWIDTH

Address Offset	See Table 14-188.		
Physical Address	0x4480 1408 0x4480 1508 0x4480 1908 0x4480 2008 0x4480 2108	**Instance**	CLK2_IVA_BW_REGULATOR CLK2_GPU_P1_BW_REGULATOR CLK2_GPU_P2_BW_REGULATOR CLK2_BB2D_P1_BW_REGULATOR CLK2_BB2D_P2_BW_REGULATOR
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BANDWIDTH															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	BANDWIDTH	Bandwidth, in bytes per second. Type: Control. Reset value: 0x0.	RW	0x0000

Table 14-196. Register Call Summary for Register L3_BW_REGULATOR_BANDWIDTH

L3 Interconnect

- Bandwidth Regulators: [0]
- L3_MAIN BW Regulator Register Summary: [1] [2] [3]

Table 14-197. L3_BW_REGULATOR_WATERMARK

Address Offset See Table 14-188.

Physical Address 0x4480 140C
0x4480 150C
0x4480 190C
0x4480 200C
0x4480 210C

Instance CLK2_IVA_BW_REGULATOR
CLK2_GPU_P1_BW_REGULATOR
CLK2_GPU_P2_BW_REGULATOR
CLK2_BB2D_P1_BW_REGULATOR
CLK2_BB2D_P2_BW_REGULATOR

Description

Type RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				WATERMARK											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:0	WATERMARK	Peak permissible bandwidth, in bytes. Type: Control. Reset value: 0x1.	RW	0x001

Table 14-198. Register Call Summary for Register L3_BW_REGULATOR_WATERMARK

L3 Interconnect

- Bandwidth Regulators: [0] [1]
- L3_MAIN BW Regulator Register Summary: [2] [3] [4]

Table 14-199. L3_BW_REGULATOR_PRESS

Address Offset See Table 14-188.

Physical Address 0x4480 1410
0x4480 1510
0x4480 1910
0x4480 2010
0x4480 2110

Instance CLK2_IVA_BW_REGULATOR
CLK2_GPU_P1_BW_REGULATOR
CLK2_GPU_P2_BW_REGULATOR
CLK2_BB2D_P1_BW_REGULATOR
CLK2_BB2D_P2_BW_REGULATOR

Description

Type R

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														PRESS_LOW	PRESS_HIGH

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	PRESS_LOW	Pressure value inserted if the measured bandwidth is over the watermark. The pressure is bar graph encoded. Type: Control. Reset value: 0x0.	R	0
0	PRESS_HIGH	Pressure value inserted if the measured bandwidth is under the watermark. The pressure is bar graph encoded. Type: Control. Reset value: 0x1.	R	1

Table 14-200. Register Call Summary for Register L3_BW_REGULATOR_PRESS

L3 Interconnect

- Bandwidth Regulators: [0]
- L3_MAIN BW Regulator Register Summary: [1] [2] [3]

Table 14-201. L3_BW_REGULATOR_CLEARHISTORY

Address Offset See Table 14-188.

Physical Address 0x4480 1414
0x4480 1514
0x4480 1914
0x4480 2014
0x4480 2114

Instance CLK2_IVA_BW_REGULATOR
CLK2_GPU_P1_BW_REGULATOR
CLK2_GPU_P2_BW_REGULATOR
CLK2_BB2D_P1_BW_REGULATOR
CLK2_BB2D_P2_BW_REGULATOR

Description

Type RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLEARHISTORY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	CLEARHISTORY	Write a 1 clear the traffic counter Type: Give_AutoCleared. Reset value: 0x0.	RW	0

Table 14-202. Register Call Summary for Register L3_BW_REGULATOR_CLEARHISTORY

L3 Interconnect

- Bandwidth Regulators: [0]
- L3_MAIN BW Regulator Register Summary: [1] [2] [3]

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14.2.5.1.7 L3_MAIN Bandwidth Limiter Register Summary and Description

Table 14-203. BW_LIMITER Instance Summary

Module Name	Base Address	Size
CLK2_BB2D_P1_BW_LIMITER	0x4480 2400	256B
CLK2_BB2D_P2_BW_LIMITER	0x4480 2500	256B

14.2.5.1.7.1 L3_MAIN BW Limiter Register Summary

Table 14-204. BW_LIMITER Register Summary

Register Name	Type	Register Width (Bits)	Address offset for CLK2_BB2D_P1	CLK2_BB2D_P1_BW_LIMITER L3_MAIN Physical Address	Address offset for CLK2_BB2D_P2	CLK2_BB2D_P2_BW_LIMITER L3_MAIN Physical Address
L3_BW_LIMITER_STDHOSTHDR_COREREG	R	32	0x0080 2400	0x4480 2400	0x0080 2500	0x4480 2500
L3_BW_LIMITER_STDHOSTHDR_VERSIONREG	R	32	0x0080 2404	0x4480 2404	0x0080 2504	0x4480 2504
L3_BW_LIMITER_BANDWIDTH_FRACTIONAL	RW	32	0x0080 2408	0x4480 2408	0x0080 2508	0x4480 2508
L3_BW_LIMITER_BANDWIDTH_INTEGER	RW	32	0x0080 240C	0x4480 240C	0x0080 250C	0x4480 250C
L3_BW_LIMITER_WATERMARK_0	RW	32	0x0080 2410	0x4480 2410	0x0080 2510	0x4480 2510
L3_BW_LIMITER_CLEARHISTORY	RW	32	0x0080 2414	0x4480 2414	0x0080 2514	0x4480 2514

14.2.5.1.7.2 L3_MAIN BW Limiter Register Description

Table 14-205. L3_BW_LIMITER_STDHOSTHDR_COREREG

Address Offset	See Table 14-204		
Physical Address	0x4480 2400 0x4480 2500	**Instance**	CLK2_BB2D_P1_BW_LIMITER CLK2_BB2D_P2_BW_LIMITER
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

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Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x0
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constantreporting a vendor-specific core generator code. Type: Constant. Reset value: 0x2C.	R	0x2C
15:1	RESERVED		R	0x0
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constantreporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x1: Read 0x0: Third-party vendor.	R	1

Table 14-206. Register Call Summary for Register L3_BW_LIMITER_STDHOSTHDR_COREREG

L3 Interconnect

- L3_MAIN BW Limiter Register Summary: [0]

Table 14-207. L3_BW_LIMITER_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-204		
Physical Address	0x4480 2404 0x4480 2504	**Instance**	CLK2_BB2D_P1_BW_LIMITER CLK2_BB2D_P2_BW_LIMITER
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																							

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constantreporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x0

Table 14-208. Register Call Summary for Register L3_BW_LIMITER_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3_MAIN BW Limiter Register Summary: [0]

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Table 14-209. L3_BW_LIMITER_BANDWIDTH_FRACTIONAL

Address Offset	See Table 14-204		
Physical Address	0x4480 2408 0x4480 2508	**Instance**	CLK2_BB2D_P1_BW_LIMITER CLK2_BB2D_P2_BW_LIMITER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BANDWIDTH_FRACTIONAL							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0
4:0	BANDWIDTH_FRACTIONAL	Fractional part of bandwitdh in terms of bytes per second Type: Control. Reset value: 0x0.	RW	0x0

Table 14-210. Register Call Summary for Register L3_BW_LIMITER_BANDWIDTH_FRACTIONAL

L3 Interconnect

- Bandwidth Limiters: [0]
- L3_MAIN BW Limiter Register Summary: [3]

Table 14-211. L3_BW_LIMITER_BANDWIDTH_INTEGER

Address Offset	See Table 14-204		
Physical Address	0x4480 240C 0x4480 250C	**Instance**	CLK2_BB2D_P1_BW_LIMITER CLK2_BB2D_P2_BW_LIMITER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												BANDWIDTH_INTEGER			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0
3:0	BANDWIDTH_INTEGER	Integer part of bandwitdh in terms of bytes per second Type: Control. Reset value: 0x0.	RW	0x0

Table 14-212. Register Call Summary for Register L3_BW_LIMITER_BANDWIDTH_INTEGER

L3 Interconnect

- Bandwidth Limiters: [0]
- L3_MAIN BW Limiter Register Summary: [3]

Table 14-213. L3_BW_LIMITER_WATERMARK_0

Address Offset	See Table 14-204		
Physical Address	0x4480 2410 0x4480 2510	**Instance**	CLK2_BB2D_P1_BW_LIMITER CLK2_BB2D_P2_BW_LIMITER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								WATERMARK_0							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x0
9:0	WATERMARK_0	Peak bandwidth allowed Type: Control. Reset value: 0x3FF.	RW	0x3FF

Table 14-214. Register Call Summary for Register L3_BW_LIMITER_WATERMARK_0

L3 Interconnect

- Bandwidth Limiters: [0]
- L3_MAIN BW Limiter Register Summary: [2]

Table 14-215. L3_BW_LIMITER_CLEARHISTORY

Address Offset	See Table 14-204		
Physical Address	0x4480 2414 0x4480 2514	**Instance**	CLK2_BB2D_P1_BW_LIMITER CLK2_BB2D_P2_BW_LIMITER
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CLEARHISTORY

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0
0	CLEARHISTORY	Write a 1 clear the traffic counter Type: Give_AutoCleared. Reset value: 0x0.	RW	0

Table 14-216. Register Call Summary for Register L3_BW_LIMITER_CLEARHISTORY

L3 Interconnect

- Bandwidth Limiters: [0]
- L3_MAIN BW Limiter Register Summary: [2]

14.2.5.1.8 L3_MAIN Rate Adapt Register Summary and Description

Table 14-217. Rate Adapt Instance Summary

Module Name	Base Address	Size
CLK1_RATE_ADAPT_RESP_32TO128_CLK1	0x4400 0800	4KiB
CLK2_RATE_ADAPT_RESP_32TO128_CLK2	0x4480 1200	4KiB

14.2.5.1.8.1 L3_MAIN Rate Adapt Register Summary

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Table 14-218. Rate Adapt Register Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK1_RATE_ADAPT_RESP_32TO128_CLK1	CLK1_RATE_ADAPT_RESP_32TO128_CLK1 L3_MAIN Physical Address	Address Offset for CLK2_RATE_ADAPT_RESP_32TO128_CLK2	CLK2_RATE_ADAPT_RESP_32TO128_CLK2 L3_MAIN Physical Address
L3_RATE_ADAPT_STDHOSTHDR_COREREG	R	32	0x0000 0800	0x4400 0800	0x0080 1200	0x4480 1200
L3_RATE_ADAPT_STDHOSTHDR_VERSIONREG	R	32	0x0000 0804	0x4400 0804	0x0080 1204	0x4480 1204
L3_RATE_ADAPT_CNF	RW	32	0x0000 0808	0x4400 0808	0x0080 1208	0x4480 1208

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14.2.5.1.8.2 L3_MAIN Rate Adapt Register Description

Table 14-219. L3_RATE_ADAPT_STDHOSTHDR_COREREG

Address Offset	See Table 14-218.		
Physical Address	0x4400 0800 0x4480 1200	**Instance**	CLK1_RATE_ADAPT_RESP_32TO128_CLK1 CLK2_RATE_ADAPT_RESP_32TO128_CLK2
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STDHOSTHDR_COREREG_CORECODE								RESERVED								STDHOSTHDR_COREREG_VENDORCODE							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x2D.	R	0x2D
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R	1

Table 14-220. Register Call Summary for Register L3_RATE_ADAPT_STDHOSTHDR_COREREG

L3 Interconnect

- L3_MAIN Rate Adapt Register Summary: [0]

Table 14-221. L3_RATE_ADAPT_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-218.		
Physical Address	0x4400 0804 0x4480 1204	**Instance**	CLK1_RATE_ADAPT_RESP_32TO128_CLK1 CLK2_RATE_ADAPT_RESP_32TO128_CLK2
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																									

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x0.	R	0x00
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-222. Register Call Summary for Register L3_RATE_ADAPT_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3_MAIN Rate Adapt Register Summary: [0]

Table 14-223. L3_RATE_ADAPT_CNF

Address Offset	See Table 14-218.		
Physical Address	0x4400 0808 0x4480 1208	**Instance**	CLK1_RATE_ADAPT_RESP_32TO128_CLK1 CLK2_RATE_ADAPT_RESP_32TO128_CLK2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											CNF_RATE				CNF_STANDFWD

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:1	CNF_RATE	Indicates the throughput ratio between input and output (Rate = [16 x (Incoming_Throughput/Outgoing_Throuput)] - 1), when bit StAndFwd bit is reset. Ignored when StAndFwd bit is set. Type: Control. Reset value: 0x3.	RW	0x3
0	CNF_STANDFWD	When this bit is set, the Packet Transport Unit stores the entire NTTP packet, then forwards it on TX port. Type: Control. Reset value: 0x0.	RW	0

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Table 14-224. Register Call Summary for Register L3_RATE_ADAPT_CNF

L3 Interconnect
• L3_MAIN Rate Adapt Register Summary: [0]

14.2.5.1.9 L3_MAIN STATCOLL Register Summary and Description

Table 14-225. STATCOLL Instance Summary

Module Name	Base Address	Size
CLK3_FLAGMUX_STATCOLL	0x4500 0400	512 bytes
CLK3_STATCOLL_SDRAM	0x4500 1000	512 bytes
CLK3_STATCOLL_LAT0	0x4500 2000	512 bytes
CLK3_STATCOLL_LAT1	0x4500 3000	512 bytes

14.2.5.1.9.1 L3_MAIN STATCOLL Register Summary

Table 14-226. STATCOLL Register Summary

Register Name	Type	Register Width (bits)	Address offset for FlAGMUX	CLK3_FLAGMUX_STATCOLL L3_MAIN Physical Address
L3_STCOL_STDHOSTHDR_COREREG	R	32	0x0100 0400	0x4500 0400
L3_STCOL_STDHOSTHDR_VERSIONREG	R	32	0x0100 0404	0x4500 0404
L3_STCOL_MASK0	RW	32	0x0100 0408	0x4500 0408
L3_STCOL_REGERR0	R	32	0x0100 040C	0x4500 040C

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Table 14-227. STATCOLL Register Summary

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOLL_SDRAM L3_MAIN Physical Address	Address Offset for LAT0	CLK3_STATCOLL_LAT0 L3_MAIN Physical Address	Address Offset for LAT1	CLK3_STATCOLL_LAT1 L3_MAIN Physical Address
L3_STCOL_STDHOSTHDR_COREREG	R	32	0x0100 1000	0x4500 1 000	0x0100 2000	0x4500 2000	0x0100 3000	0x4500 3000
L3_STCOL_STDHOSTHDR_VERSIONREG	R	32	0x0100 1004	0x4500 1004	0x0100 2004	0x4500 2004	0x0100 3004	0x4500 3004
L3_STCOL_EN	RW	32	0x0100 1008	0x4500 1008	0x0100 2008	0x4500 2008	0x0100 3008	0x4500 3008
L3_STCOL_SOFTEN	RW	32	0x0100 100C	0x4500 100C	0x0100 200C	0x4500 200C	0x0100 300C	0x4500 300C
L3_STCOL_IGNORESUSPEND	RW	32	0x0100 1010	0x4500 1010	0x0100 2010	0x4500 2010	0x0100 3010	0x4500 3010
L3_STCOL_TRIGEN	RW	32	0x0100 1014	0x4500 1014	0x0100 2014	0x4500 2014	0x0100 3014	0x4500 3014
L3_STCOL_REQEVT	RW	32	0x0100 1018	0x4500 1018	0x0100 2018	0x4500 2018	0x0100 3018	0x4500 3018
L3_STCOL_RSPEVT	RW	32	0x0100 101C	0x4500 101C	0x0100 201C	0x4500 201C	0x0100 301C	0x4500 301C
L3_STCOL_EVTMUX_SEL0	RW	32	0x0100 1020	0x45001020	0x0100 2020	0x4500 2020	0x0100 3020	0x4500 3020
L3_STCOL_EVTMUX_SEL1	RW	32	0x0100 1024	0x4500 1024	0x0100 2024	0x4500 2024	0x0100 3024	0x4500 3024
L3_STCOL_EVTMUX_SEL2	RW	32	0x0100 1028	0x4500 1028	0x0100 2028	0x4500 2028	0x0100 3028	0x4500 3028
L3_STCOL_EVTMUX_SEL3	RW	32	0x0100 102C	0x4500 102C	0x0100 202C	0x4500 202C	0x0100 302C	0x4500 302C
L3_STCOL_EVTMUX_SEL4	RW	32	0x0100 1030	0x4500 1030	N/A	N/A	N/A	N/A
L3_STCOL_EVTMUX_SEL5	RW	32	0x0100 1034	0x4500 1034	N/A	N/A	N/A	N/A
L3_STCOL_EVTMUX_SEL6	RW	32	0x0100 1038	0x4500 1038	N/A	N/A	N/A	N/A
L3_STCOL_EVTMUX_SEL7	RW	32	0x0100 103C	0x4500 103C	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_IDENTIFIER	R	32	0x0100 1040	0x4500 1040	0x0100 2040	0x4500 2040	0x0100 3040	0x4500 3040
L3_STCOL_DUMP_COLLECTTIME	RW	32	0x010010444	0x4500 1044	0x0100 2044	0x4500 2044	0x0100 3044	0x4500 3044
L3_STCOL_DUMP_SLVADDR	R	32	0x0100 1048	0x4500 1048	0x0100 2048	0x4500 2048	0x0100 3048	0x4500 3048
L3_STCOL_DUMP_MSTADDR	R	32	0x0100 104C	0x4500 104C	0x0100 204C	0x4500 204C	0x0100 304C	0x4500 304C
L3_STCOL_DUMP_SLVOFS	RW	32	0x0100 1050	0x4500 1050	0x0100 2050	0x4500 2050	0x0100 3050	0x4500 3050
L3_STCOL_DUMP_MODE	RW	32	0x0100 1054	0x4500 1054	0x0100 2054	0x4500 2054	0x0100 3054	0x4500 3054
L3_STCOL_DUMP_SEND	RW	32	0x0100 1058	0x4500 1058	0x0100 2058	0x4500 2058	0x0100 3058	0x4500 3058
L3_STCOL_DUMP_DISABLE	RW	32	0x0100 105C	0x4500 105C	0x0100 205C	0x4500 205C	0x0100 305C	0x4500 305C
L3_STCOL_DUMP_ALARM_TRIG	RW	32	0x0100 1060	0x4500 1060	0x0100 2060	0x4500 2060	0x0100 3060	0x4500 3060
L3_STCOL_DUMP_ALARM_MINVAL	RW	32	0x0100 1064	0x4500 1064	0x0100 2064	0x4500 2064	0x0100 3064	0x4500 3064
L3_STCOL_DUMP_ALARM_MAXVAL	RW	32	0x0100 1068	0x4500 1068	0x0100 2068	0x4500 2068	0x0100 3068	0x4500 3068
L3_STCOL_DUMP_ALARM_MODE0	RW	32	0x0100 106C	0x4500 106C	0x0100 206C	0x4500 206C	0x0100 306C	0x4500 306C
L3_STCOL_DUMP_ALARM_MODE1	RW	32	0x0100 1070	0x4500 1070	0x0100 2070	0x4500 2070	0x0100 3070	0x4500 3070
L3_STCOL_DUMP_ALARM_MODE2	RW	32	0x0100 1074	0x4500 1074	0x0100 2074	0x4500 2074	0x0100 3074	0x4500 3074

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Table 14-227. STATCOLL Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOLL_SDRAM L3_MAIN Physical Address	Address Offset for LAT0	CLK3_STATCOLL_LAT0 L3_MAIN Physical Address	Address Offset for LAT1	CLK3_STATCOLL_LAT1 L3_MAIN Physical Address
L3_STCOL_DUMP_ALARM_MODE3	RW	32	0x0100 1078	0x4500 1078	0x0100 2078	0x4500 2078	0x0100 3078	0x4500 3078
L3_STCOL_DUMP_ALARM_MODE4	RW	32	0x0100 107C	0x4500 107C	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_ALARM_MODE5	RW	32	0x0100 1080	0x4500 1080	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_ALARM_MODE6	RW	32	0x0100 1084	0x4500 1084	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_ALARM_MODE7	RW	32	0x0100 1088	0x4500 1088	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT0	R	32	0x0100 108C	0x4500 108C	0x0100208C	0x4500 208C	0x0100 308C	0x4500 308C
L3_STCOL_DUMP_CNT1	R	32	0x0100 1090	0x4500 1090	0x0100 2090	0x4500 2090	0x0100 3090	0x4500 3090
L3_STCOL_DUMP_CNT2	R	32	0x0100 1094	0x4500 1094	0x0100 2094	0x4500 2094	0x0100 3094	0x4500 3094
L3_STCOL_DUMP_CNT3	R	32	0x0100 1098	0x4500 1098	0x0100 2098	0x4500 2098	0x0100 3098	0x4500 3098
L3_STCOL_DUMP_CNT4	R	32	0x0100 109C	0x4500 109C	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT5	R	32	0x0100 10A0	0x4500 10A0	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT6	R	32	0x0100 10A4	0x4500 10A4	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT7	R	32	0x0100 10A8	0x4500 10A8	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_GLOBALEN	RW	32	0x0100 10AC	0x4500 10AC	0x0100 20AC	0x4500 20AC	0x0100 30AC	0x4500 30AC
L3_STCOL_FILTER_i_ADDRMIN	RW	32	0x0100 10B0	0x4500 10B0	0x0100 20B0	0x4500 20B0	0x0100 30B0	0x4500 30B0
L3_STCOL_FILTER_i_ADDRMAX	RW	32	0x0100 10B4	0x4500 10B4	0x0100 20B4	0x4500 20B4	0x0100 30B4	0x4500 30B4
L3_STCOL_FILTER_i_ADDREN	RW	32	0x0100 10B8	0x4500 10B8	0x0100 20B8	0x4500 20B8	0x0100 30B8	0x4500 30B8
L3_STCOL_FILTER_i_EN_k	RW	32	0x010010BC	0x4500 10BC	0X0100 20BC	0x4500 20BC	0x0100 30BC	0x4500 30BC
L3_STCOL_FILTER_i_MASK_m_RD	RW	32	0x0100 10C0	0x4500 10C0	0x0100 20C0	0x4500 20C0	0x0100 30C0	0x4500 30C0
L3_STCOL_FILTER_i_MASK_m_WR	RW	32	0x0100 10C4	0x4500 10C4	0x0100 20C4	0x4500 20C4	0x0100 30C4	0x4500 30C4
L3_STCOL_FILTER_i_MASK_m_MSTADDR	RW	32	0x0100 10C8	0x4500 10C8	0x0100 20C8	0x4500 20C8	0x0100 30C8	0x4500 30C8
L3_STCOL_FILTER_i_MASK_m_SLVADDR	RW	32	N/A	N/A	0x0100 20CC	0x4500 20CC	0x0100 30CC	0x4500 30CC
L3_STCOL_FILTER_i_MASK_m_ERR	RW	32	0x0100 10D0	0x4500 10D0	0x0100 20D0	0x4500 20D0	0x0100 30D0	0x4500 30D0
L3_STCOL_FILTER_i_MASK_m_USERINFO	RW	32	0x0100 10D4	0x4500 10D4	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_MASK_m_REQUSERINFO	RW	32	N/A	N/A	0x0100 20D4	0x4500 20D4	0x0100 30D4	0x4500 30D4
L3_STCOL_FILTER_i_MASK_m_RSPUSERINFO	RW	32	N/A	N/A	0x0100 20D8	0x4500 20D8	0x0100 30D8	0x4500 30D8
L3_STCOL_FILTER_i_MATCH_m_RD	RW	32	0x0100 10E0	0x4500 10E0	0x0100 20E0	0x4500 20E0	0x0100 30E0	0x4500 30E0

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Table 14-227. STATCOLL Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOLL_SDRAM L3_MAIN Physical Address	Address Offset for LAT0	CLK3_STATCOLL_LAT0 L3_MAIN Physical Address	Address Offset for LAT1	CLK3_STATCOLL_LAT1 L3_MAIN Physical Address
L3_STCOL_FILTER_i_MATCH_m_WR	RW	32	0x0100 10E4	0x4500 10E4	0x0100 20E4	0x4500 20E4	0x0100 30E4	0x4500 30E4
L3_STCOL_FILTER_i_MATCH_m_MSTADDR	RW	32	0x0100 10E8	0x4500 10E8	0x0100 20E8	0x4500 20E8	0x0100 30E8	0x4500 30E8
L3_STCOL_FILTER_i_MATCH_m_SLVADDR	RW	32	N/A	N/A	0x0100 20EC	0x4500 20EC	0x0100 30EC	0x4500 30EC
L3_STCOL_FILTER_i_MATCH_m_ERR	RW	32	0x0100 10F0	0x4500 10F0	0x0100 20F0	0x4500 20F0	0x0100 30F0	0x4500 30F0
L3_STCOL_FILTER_i_MATCH_m_USERINFO	RW	32	0x0100 10F4	0x4500 10F4	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_MATCH_m_REQUSERINFO	RW	32	N/A	N/A	0x0100 20F4	0x4500 20F4	0x0100 30F4	0x4500 30F4
L3_STCOL_FILTER_i_MATCH_m_RSPUSERINFO	RW	32	N/A	N/A	0x0100 20F8	0x4500 20F8	0x0100 30F8	0x4500 30F8
L3_STCOL_OP_i_THRESHOLD_MINVAL	RW	32	0x0100 11F0	0x4500 11F0	0x0100 21F0	0x4500 21F0	0x0100 31F0	0x4500 31F0
L3_STCOL_OP_i_THRESHOLD_MAXVAL	RW	32	0x0100 11F4	0x4500 11F4	0x0100 21F4	0x4500 21F4	0x0100 31F4	0x4500 31F4
L3_STCOL_OP_i_EVTINFOSEL	RW	32	0x0100 11F8	0x4500 11F8	0x0100 21F8	0x4500 21F8	0x0100 31F8	0x4500 31F8
L3_STCOL_OP_i_SEL	RW	32	0x0100 11FC	0x4500 11FC	0x0100 21FC	0x4500 21FC	0x0100 31FC	0x4500 31FC

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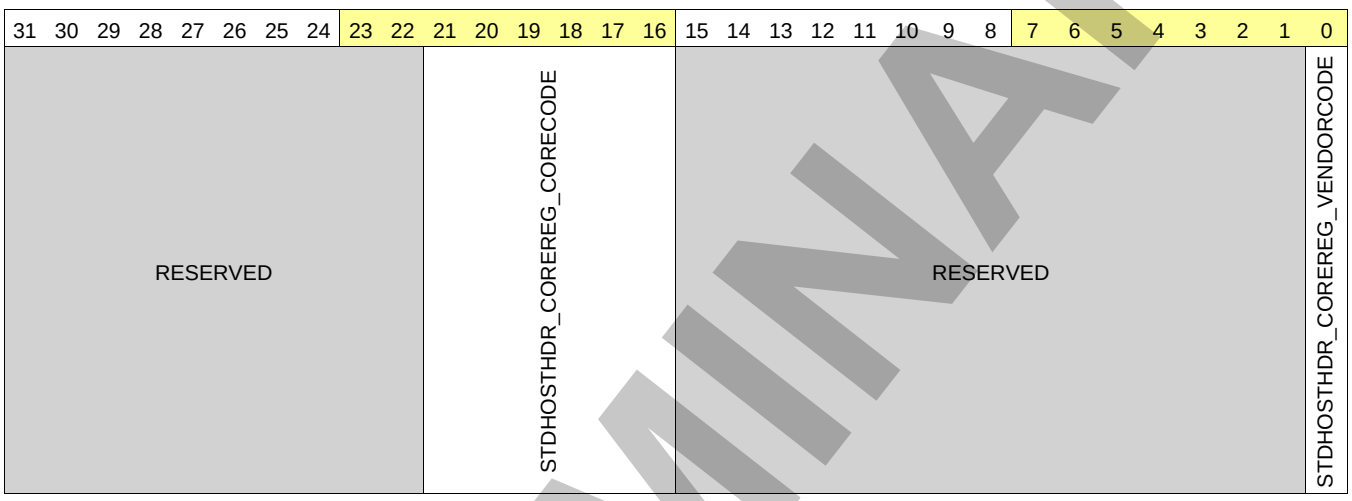
14.2.5.1.9.2 L3_MAIN STATCOLL Register Description

Table 14-228. L3_STCOL_STDHOSTHDR_COREREG

Address Offset	See Table 14-227.		
Physical Address	0x4500 0400 0x4500 1 000 0x4500 2000 0x4500 3000	**Instance**	CLK3_FLAGMUX_STATCOLL CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21:16	STDHOSTHDR_COREREG_CORECODE	The Core Code field is a constant reporting a vendor-specific core generator code. Type: Constant. Reset value: 0x3A. (When the instance is CLK3_FLAGMUX_STATCOLL reset value is 0x37)	R	0x3A
15:1	RESERVED	Reserved	R	0x0000
0	STDHOSTHDR_COREREG_VENDORCODE	The Vendor Code field is a constant reporting the core generator vendor code. Type: Constant. Reset value: 0x1. Read 0x0: Third-party vendor. Read 0x1:	R1	1

Table 14-229. Register Call Summary for Register L3_STCOL_STDHOSTHDR_COREREG

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0] [1]

Table 14-230. L3_STCOL_STDHOSTHDR_VERSIONREG

Address Offset	See Table 14-227.		
Physical Address	0x4500 0404 0x4500 1004 0x4500 2004 0x4500 3004	**Instance**	CLK3_FLAGMUX_STATCOLL CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STDHOSTHDR_VERSIONREG_REVISIONID								STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM																									

Bits	Field Name	Description	Type	Reset
31:24	STDHOSTHDR_VERSIONREG_REVISIONID	The Revision Identifier field is a constant reporting the core generator revision number. Type: Constant. Reset value: 0x1.	R	0x1
23:0	STDHOSTHDR_VERSIONREG_COREPARAMSCHECKSUM	Reserved. Type: Reserved. Reset value: Reserved.	R	0x000000

Table 14-231. Register Call Summary for Register L3_STCOL_STDHOSTHDR_VERSIONREG

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0] [1]

Table 14-232. L3_STCOL_MASK0

Address Offset	See Table 14-226.		
Physical Address	0x4500 0408	**Instance**	CLK3_FLAGMUX_STATCOLL
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MASK0	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MASK0	mask flag inputs 0 Type: Control. Reset value: 0x7.	RW	0x7

Table 14-233. Register Call Summary for Register L3_STCOL_MASK0

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-234. L3_STCOL_REGERR0

Address Offset	See Table 14-226.		
Physical Address	0x4500 040C	**Instance**	CLK3_FLAGMUX_STATCOLL
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														REGERR0	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	REGERR0	flag inputs 0 Type: Status. Reset value: X.	R	0x0000 0000

Table 14-235. Register Call Summary for Register L3_STCOL_REGERR0

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-236. L3_STCOL_EN

Address Offset See Table 14-227.

Physical Address 0x4500 1008 (CLK3_STATCOLL_SDRAM)
0x4500 2008 (CLK3_STATCOLL_LAT0)
0x4500 3008 (CLK3_STATCOLL_LAT1)

Instance

Description

Type RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	EN	Enable performance monitoring, this will also shut down the clock if En = 0 Type: Control. Reset value: 0x0.	RW	0

Table 14-237. Register Call Summary for Register L3_STCOL_EN

L3 Interconnect

- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary: [1]

Table 14-238. L3_STCOL_SOFTEN

Address Offset See Table 14-227.

Physical Address 0x4500 100C (CLK3_STATCOLL_SDRAM)
0x4500 200C (CLK3_STATCOLL_LAT0)
0x4500 300C (CLK3_STATCOLL_LAT1)

Instance

Description

Type RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SOFTEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SOFTEN	Software enable for performance monitoring Type: Control. Reset value: 0x0.	RW	0

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Table 14-239. Register Call Summary for Register L3_STCOL_SOFTEN

L3 Interconnect

- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary: [1]

Table 14-240. L3_STCOL_IGNORESUSPEND

Address Offset	See Table 14-227.		
Physical Address	0x4500 1010 0x4500 2010 0x4500 3010	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															IGNORESUSPEND

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	IGNORESUSPEND	Ignore suspend if set to one for suspend mechanism Type: Control. Reset value: 0x0.	RW	0

Table 14-241. Register Call Summary for Register L3_STCOL_IGNORESUSPEND

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-242. L3_STCOL_TRIGEN

Address Offset	See Table 14-227.		
Physical Address	0x4500 1014 0x4500 2014 0x4500 3014	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															TRIGEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	TRIGEN	TrigEn when set, it enable the external trigger start and stop Type: Control. Reset value: 0x0.	RW	0

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Table 14-243. Register Call Summary for Register L3_STCOL_TRIGEN

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-244. L3_STCOL_REQEVT

Address Offset	See Table 14-227.		
Physical Address	0x4500 1018 0x4500 2018 0x4500 3018	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												REQEVT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	REQEVT	Req event select Type: Control. Reset value: 0x0. 0x0: Collect is disabled default value 0x1: Collect all event: hit always (cycle) 0x2: Collect transfers: actually used cycle for transferring aN NTTP word 0x3: Collect wait cycle: transfer has been delayed by source 0x4: Collect busy: transfer has been delayed by destination 0x5: Collect packet: new packet start 0x6: Collect data: data cycle transfer, write for requests, read for responses 0x7: Collect idles: transfer is not initiated by source 0x8: Collect latency: hit when actually detecting debug bit on response links	RW	0x0

Table 14-245. Register Call Summary for Register L3_STCOL_REQEVT

L3 Interconnect

- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary: [1]

Table 14-246. L3_STCOL_RSPEVT

Address Offset	See Table 14-227.		
Physical Address	0x4500 101C 0x4500 201C 0x4500 301C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												RSPEVT			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	RSPEVT	Rsp event select Type: Control. Reset value: 0x0. 0x0: Collect is disabled default value 0x1: Collect all event: hit always (cycle) 0x2: Collect transfers: actually used cycle for transferring a NTTP word 0x3: Collect wait cycle: transfer has been delayed by source 0x4: Collect busy: transfer has been delayed by destination 0x5: Collect packet: new packet start 0x6: Collect data: data cycle transfer, write for requests, read for responses 0x7: Collect idles: transfer is not initiated by source 0x8: Collect latency: hit when actually detecting debug bit on response links	RW	0x0

Table 14-247. Register Call Summary for Register L3_STCOL_RSPEVT

L3 Interconnect
- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary: [1]

Table 14-248. L3_STCOL_EVTMUX_SEL0

Address Offset	See Table 14-227.		
Physical Address	0x45001020 0x4500 2020 0x4500 3020	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												EVTMUX_SEL0			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:0	EVTMUX_SEL0	The select of the mux 0 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-249. Register Call Summary for Register L3_STCOL_EVTMUX_SEL0

L3 Interconnect
- Statistic Collectors Group: [0]
- L3_MAIN STATCOLL Register Summary: [1]

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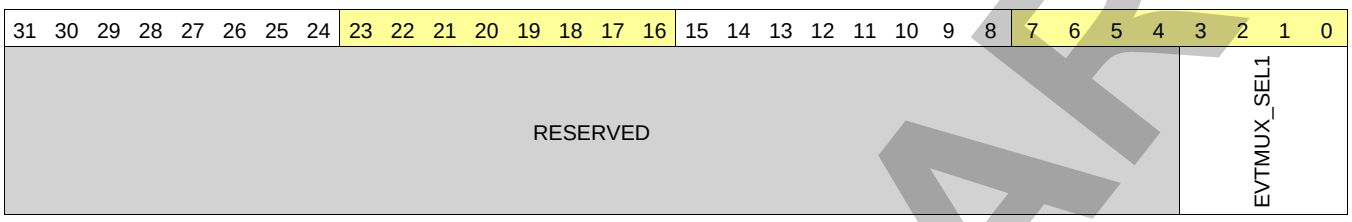
Table 14-250. L3_STCOL_EVTMUX_SEL1

Address Offset	See Table 14-227.		
Physical Address	0x4500 1024 0x4500 2024 0x4500 3024	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:0	EVTMUX_SEL1	The select of the mux 1 Type: Control. Reset value: 0x0.	RW	0x0

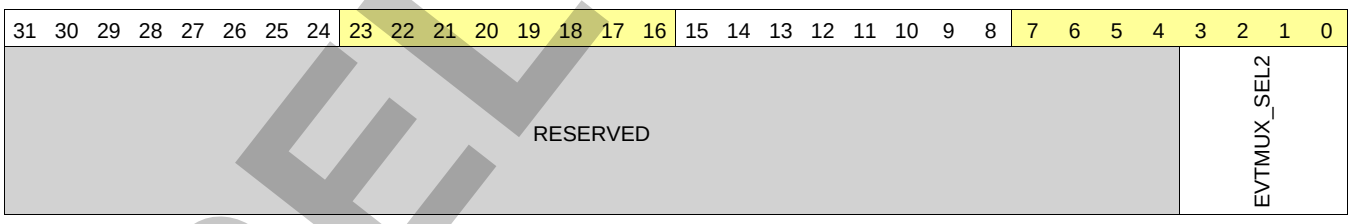
Table 14-251. Register Call Summary for Register L3_STCOL_EVTMUX_SEL1

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-252. L3_STCOL_EVTMUX_SEL2

Address Offset	See Table 14-227.		
Physical Address	0x4500 1028 0x4500 2028 0x4500 3028	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:0	EVTMUX_SEL2	The select of the mux 2 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-253. Register Call Summary for Register L3_STCOL_EVTMUX_SEL2

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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Table 14-254. L3_STCOL_EVTMUX_SEL3

Address Offset	See Table 14-227.		
Physical Address	0x4500 102C 0x4500 202C 0x4500 302C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL3	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:0	EVTMUX_SEL3	The select of the mux 3 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-255. Register Call Summary for Register L3_STCOL_EVTMUX_SEL3

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-256. L3_STCOL_EVTMUX_SEL4

Address Offset	See Table 14-227.		
Physical Address	0x4500 1030	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVTMUX_SEL4	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:0	EVTMUX_SEL4	The select of the mux 4 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-257. Register Call Summary for Register L3_STCOL_EVTMUX_SEL4

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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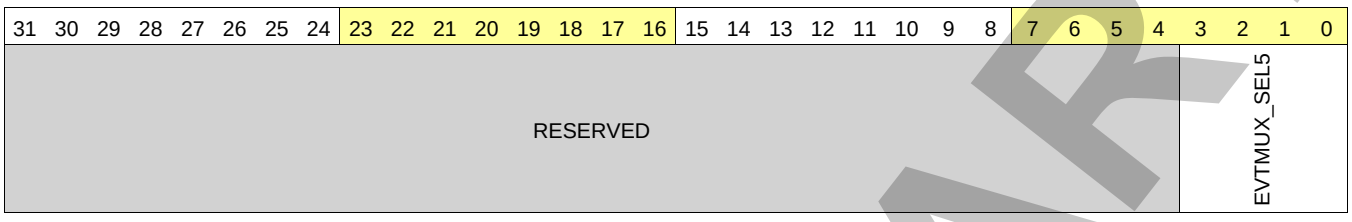
Table 14-258. L3_STCOL_EVTMUX_SEL5

Address Offset	See Table 14-227.		
Physical Address	0x4500 1034	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:0	EVTMUX_SEL5	The select of the mux 5 Type: Control. Reset value: 0x0.	RW	0x0

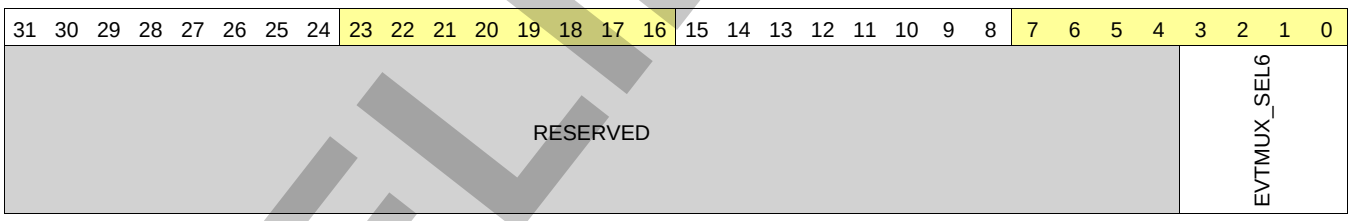
Table 14-259. Register Call Summary for Register L3_STCOL_EVTMUX_SEL5

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-260. L3_STCOL_EVTMUX_SEL6

Address Offset	See Table 14-227.		
Physical Address	0x4500 1038	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:0	EVTMUX_SEL6	The select of the mux 6 Type: Control. Reset value: 0x0.	RW	0x0

Table 14-261. Register Call Summary for Register L3_STCOL_EVTMUX_SEL6

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-262. L3_STCOL_EVTMUX_SEL7

Address Offset	See Table 14-227.		
Physical Address	0x4500 103C	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

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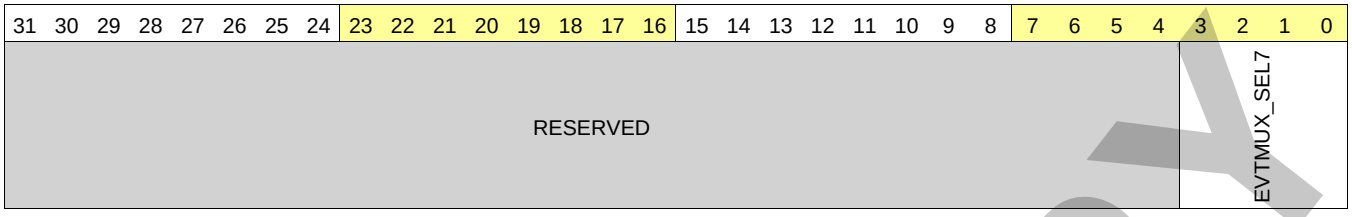


Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3:0	EVTMUX_SEL7	The select of the mux 7 Type: Control. Reset value: 0x0.	RW	0x0

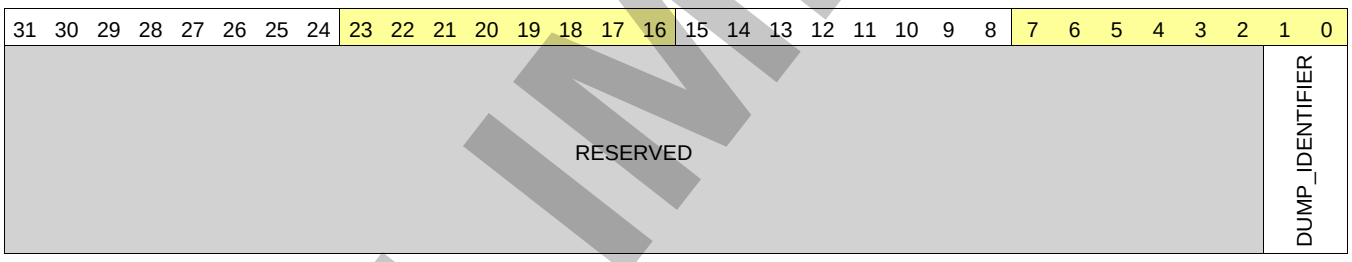
Table 14-263. Register Call Summary for Register L3_STCOL_EVTMUX_SEL7

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-264. L3_STCOL_DUMP_IDENTIFIER

Address Offset	See Table 14-227.		
Physical Address	0x4500 1040 0x4500 2040 0x4500 3040	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	DUMP_IDENTIFIER	Probe identifier Type: Control. Reset value: 0x0.	R	0x0

Table 14-265. Register Call Summary for Register L3_STCOL_DUMP_IDENTIFIER

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-266. L3_STCOL_DUMP_COLLECTTIME

Address Offset	See Table 14-227.		
Physical Address	0x4500 1044 0x4500 2044 0x4500 3044	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_COLLECTTIME																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_COLLECTTIME	Number of cycle to wait between two statistics frame Type: Control. Reset value: 0x0.	RW	0x0000

Table 14-267. Register Call Summary for Register L3_STCOL_DUMP_COLLECTTIME

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-268. L3_STCOL_DUMP_SLVADDR

Address Offset	See Table 14-227.		
Physical Address	0x4500 1048 0x4500 2048 0x4500 3048	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													DUMP_SLVADDR		

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	DUMP_SLVADDR	Dump slave address Type: Control. Reset value: 0x19.	R	0x19

Table 14-269. Register Call Summary for Register L3_STCOL_DUMP_SLVADDR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-270. L3_STCOL_DUMP_MSTADDR

Address Offset	See Table 14-227.		
Physical Address	0x4500 104C 0x4500 204C 0x4500 304C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					DUMP_MSTADDR										

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10:0	DUMP_MSTADDR	Dump master address Type: Control. Reset value: 0xE0.	R	0x380

Table 14-271. Register Call Summary for Register L3_STCOL_DUMP_MSTADDR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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Table 14-272. L3_STCOL_DUMP_SLVOFS

Address Offset	See Table 14-227.		
Physical Address	0x4500 1050 0x4500 2050 0x4500 3050	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_SLVOFS																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_SLVOFS	Dump slave offset Type: Control. Reset value: 0x800.	RW	0x0000 0800

Table 14-273. Register Call Summary for Register L3_STCOL_DUMP_SLVOFS

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-274. L3_STCOL_DUMP_MODE

Address Offset	See Table 14-227.		
Physical Address	0x4500 1054 0x4500 2054 0x4500 3054	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_MODE_CONDITIONAL	DUMP_MANUAL

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1	DUMP_MODE_CONDITIONAL	Define the stat conditional dump, if one a dump will be generated when alarm is trigged Type: Control. Reset value: 0x0.	RW	0
0	DUMP_MODE_MANUAL	Define the dump mode: if != 0 the dump is controlled by the Send register. Type: Control. Reset value: 0x0.	RW	0

Table 14-275. Register Call Summary for Register L3_STCOL_DUMP_MODE

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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Table 14-276. L3_STCOL_DUMP_SEND

Address Offset	See Table 14-227.		
Physical Address	0x4500 1058 0x4500 2058 0x4500 3058	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DUMP_SEND

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DUMP_SEND	In manual mode, is used to send the dump content and initialize the counters. Type: Give_AutoCleared. Reset value: 0x0. • Dumping can be performed only if monitoring is enabled • For “one shot metrics dump” the DUMP_SEND command has to be issued before disabling monitoring	RW	0

Table 14-277. Register Call Summary for Register L3_STCOL_DUMP_SEND

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-278. L3_STCOL_DUMP_DISABLE

Address Offset	See Table 14-227.		
Physical Address	0x4500 105C 0x4500 205C 0x4500 305C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DUMP_DISABLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	DUMP_DISABLE	If 1, the dump frame will be disabled, but counters still active.This is typically used when counters monitoring is enabled Type: Control. Reset value: 0x0.	RW	0

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Table 14-279. Register Call Summary for Register L3_STCOL_DUMP_DISABLE

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-280. L3_STCOL_DUMP_ALARM_TRIG

Address Offset	See Table 14-227.		
Physical Address	0x4500 1060 0x4500 2060 0x4500 3060	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DUMP_ALARM_TRIG

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
0	DUMP_ALARM_TRIG	In Alarm Mode, is used to reset Alarm Type: Take. Reset value: 0x0.	RW	0

Table 14-281. Register Call Summary for Register L3_STCOL_DUMP_ALARM_TRIG

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-282. L3_STCOL_DUMP_ALARM_MINVAL

Address Offset	See Table 14-227.		
Physical Address	0x4500 1064 0x4500 2064 0x4500 3064	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_ALARM_MINVAL																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_ALARM_MINVAL	In Alarm Mode, used to trig an alert if any of counter value is less than AlarmMinVal Type: Control. Reset value: 0x0.	RW	0x0000 0000

Table 14-283. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MINVAL

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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Table 14-284. L3_STCOL_DUMP_ALARM_MAXVAL

Address Offset	See Table 14-227.		
Physical Address	0x4500 1068 0x4500 2068 0x4500 3068	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_ALARM_MAXVAL																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_ALARM_MAXVAL	In Alarm Mode, used to trig an alert if any of counter value is larger or equal to AlarmMaxVal Type: Control. Reset value: 0x0.	RW	0x0000 0000

Table 14-285. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MAXVAL

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-286. L3_STCOL_DUMP_ALARM_MODE0

Address Offset	See Table 14-227.		
Physical Address	0x4500 106C 0x4500 206C 0x4500 306C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_ALARM_MODE0	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE0	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-287. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE0

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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Table 14-288. L3_STCOL_DUMP_ALARM_MODE1

Address Offset	See Table 14-227.		
Physical Address	0x4500 1070 0x4500 2070 0x4500 3070	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_ALARM_MODE1	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE1	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-289. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE1

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-290. L3_STCOL_DUMP_ALARM_MODE2

Address Offset	See Table 14-227.		
Physical Address	0x4500 1074 0x4500 2074 0x4500 3074	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_ALARM_MODE2	

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE2	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-291. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE2

L3 Interconnect
- L3_MAIN STATCOLL Register Summary: [0]

Table 14-292. L3_STCOL_DUMP_ALARM_MODE3

Address Offset	See Table 14-227.		
Physical Address	0x4500 1078 0x4500 2078 0x4500 3078	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_ALARM_MODE3	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE3	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-293. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE3

L3 Interconnect
- L3_MAIN STATCOLL Register Summary: [0]

Table 14-294. L3_STCOL_DUMP_ALARM_MODE4

Address Offset	See Table 14-227.		
Physical Address	0x4500 107C	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_ALARM_MODE4	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE4	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-295. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE4

L3 Interconnect
- L3_MAIN STATCOLL Register Summary: [0]

Table 14-296. L3_STCOL_DUMP_ALARM_MODE5

Address Offset	See Table 14-227.		
Physical Address	0x4500 1080	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DUMP_ALARM_MODE5	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE5	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

Table 14-297. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE5

L3 Interconnect
- L3_MAIN STATCOLL Register Summary: [0]

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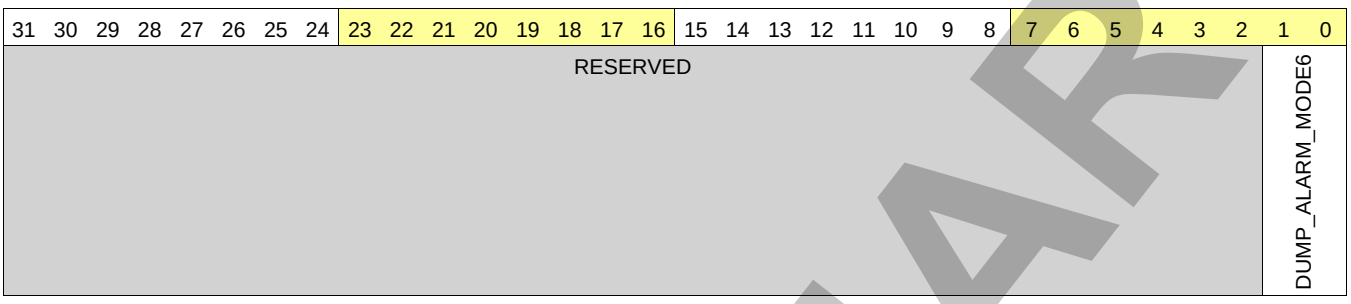
Table 14-298. L3_STCOL_DUMP_ALARM_MODE6

Address Offset	See Table 14-227.		
Physical Address	0x4500 1084	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE6	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: OFF 0x1: MIN 0x3: MAX 0x2: BOTH	RW	0x0

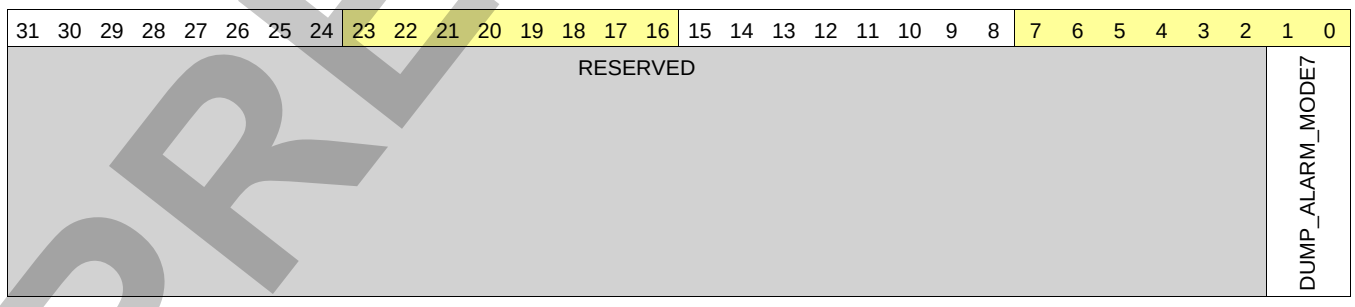
Table 14-299. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE6

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-300. L3_STCOL_DUMP_ALARM_MODE7

Address Offset	See Table 14-227.		
Physical Address	0x4500 1088	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	DUMP_ALARM_MODE7	Alarm Mode off/min/max/both Type: Control. Reset value: 0x0. 0x0: 0x1: 0x3: 0x2:	RW	0x0

Table 14-301. Register Call Summary for Register L3_STCOL_DUMP_ALARM_MODE7

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-302. L3_STCOL_DUMP_CNT0

Address Offset	See Table 14-227.		
Physical Address	0x4500 108C 0x4500 208C 0x4500 308C	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT0																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT0	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-303. Register Call Summary for Register L3_STCOL_DUMP_CNT0

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-304. L3_STCOL_DUMP_CNT1

Address Offset	See Table 14-227.		
Physical Address	0x4500 1090 0x4500 2090 0x4500 3090	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT1																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT1	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-305. Register Call Summary for Register L3_STCOL_DUMP_CNT1

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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Table 14-306. L3_STCOL_DUMP_CNT2

Address Offset	See Table 14-227.		
Physical Address	0x4500 1094 0x4500 2094 0x4500 3094	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT2																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT2	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-307. Register Call Summary for Register L3_STCOL_DUMP_CNT2

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-308. L3_STCOL_DUMP_CNT3

Address Offset	See Table 14-227.		
Physical Address	0x4500 1098 0x4500 2098 0x4500 3098	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT3																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT3	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-309. Register Call Summary for Register L3_STCOL_DUMP_CNT3

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-310. L3_STCOL_DUMP_CNT4

Address Offset	See Table 14-227.		
Physical Address	0x4500 109C	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT4																															

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Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT4	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-311. Register Call Summary for Register L3_STCOL_DUMP_CNT4

L3 Interconnect
- L3_MAIN STATCOLL Register Summary: [0]

Table 14-312. L3_STCOL_DUMP_CNT5

Address Offset	See Table 14-227.		
Physical Address	0x4500 10A0	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT5																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT5	Dump counter value Type: Status. Reset value: X.	R	0x0

Table 14-313. Register Call Summary for Register L3_STCOL_DUMP_CNT5

L3 Interconnect
- L3_MAIN STATCOLL Register Summary: [0]

Table 14-314. L3_STCOL_DUMP_CNT6

Address Offset	See Table 14-227.		
Physical Address	0x4500 10A4	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT6																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT6	Dump counter value Type: Status. Reset value: X.	R	0x---- ----

Table 14-315. Register Call Summary for Register L3_STCOL_DUMP_CNT6

L3 Interconnect
- L3_MAIN STATCOLL Register Summary: [0]

Table 14-316. L3_STCOL_DUMP_CNT7

Address Offset	See Table 14-227.		
Physical Address	0x4500 10A8	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMP_CNT7																															

Bits	Field Name	Description	Type	Reset
31:0	DUMP_CNT7	Dump counter value Type: Status. Reset value: X.	R	0x---- ----

Table 14-317. Register Call Summary for Register L3_STCOL_DUMP_CNT7

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-318. L3_STCOL_FILTER_i_GLOBALEN

Address Offset	See Table 14-227.		
Physical Address	0x4500 10AC 0x4500 20AC 0x4500 30AC	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_GLOBALEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_GLOBALEN	Filter global enable Type: Control. Reset value: 0x0.	RW	0

Table 14-319. Register Call Summary for Register L3_STCOL_FILTER_i_GLOBALEN

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-320. L3_STCOL_FILTER_i_ADDRMIN

Address Offset	See Table 14-227.		
Physical Address	0x4500 10B0 0x4500 20B0 0x4500 30B0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER0_ADDRMIN																							

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x0000 0000
22:0	FILTER0_ADDRMIN	Min addr range Type: Control. Reset value: 0x0.	RW	0x00 0000

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Table 14-321. Register Call Summary for Register L3_STCOL_FILTER_i_ADDRMIN

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-322. L3_STCOL_FILTER_i_ADDRMAX

Address Offset	See Table 14-227.		
Physical Address	0x4500 10B4 0x4500 20B4 0x4500 30B4	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER0_ADDRMAX																							

Bits	Field Name	Description	Type	Reset
31:23	RESERVED		R	0x0000 0000
22:0	FILTER0_ADDRMAX	Max addr range Type: Control. Reset value: 0x0.	RW	0x00 0000

Table 14-323. Register Call Summary for Register L3_STCOL_FILTER_i_ADDRMAX

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-324. L3_STCOL_FILTER_i_ADDREN

Address Offset	See Table 14-227.		
Physical Address	0x4500 10B8 0x4500 20B8 0x4500 30B8	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER0_ADDREN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0bxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
0	FILTER0_ADDREN	max filtering enable Type: Control. Reset value: 0x0.	RW	0

Table 14-325. Register Call Summary for Register L3_STCOL_FILTER_i_ADDREN

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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Table 14-326. L3_STCOL_FILTER_i_EN_k

Address Offset	See Table 14-227.		
Physical Address	0x4500 10BC 0x4500 20BC 0x4500 30BC	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_EN0

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_EN0	Enable filter stage 0 Type: Control. Reset value: 0x0.	RW	0

Table 14-327. Register Call Summary for Register L3_STCOL_FILTER_i_EN_k

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-328. L3_STCOL_FILTER_i_MASK_m_MSTADDR

Address Offset	See Table 14-227.		
Physical Address	0x4500 10C8 0x4500 20C8 0x4500 30C8	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FILTER_i_MASK_m_MSTADDR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	FILTER_i_MASK_m_MSTADDR	Mask/Match of MstAddr Type: Control. Reset value: 0x0.	RW	0x00

Table 14-329. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_MSTADDR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-330. L3_STCOL_FILTER_i_MASK_m_RD

Address Offset	See Table 14-227.		
Physical Address	0x4500 10C0 0x4500 20C0 0x4500 30C0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

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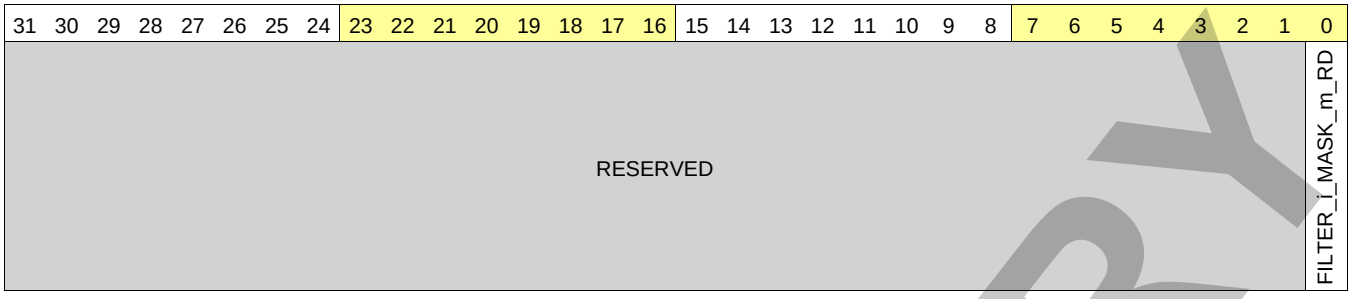


Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MASK_m_RD	Mask/Match of Rd Type: Control. Reset value: 0x0.	RW	0

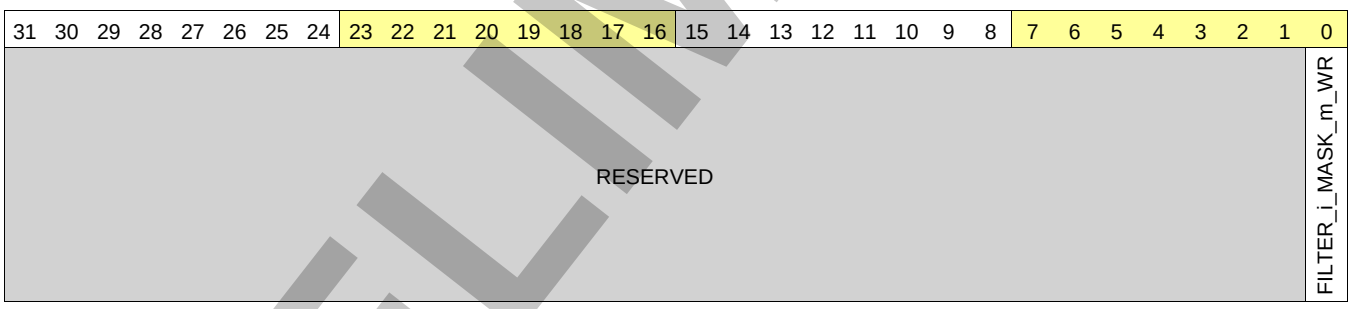
Table 14-331. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_RD

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-332. L3_STCOL_FILTER_i_MASK_m_WR

Address Offset	See Table 14-227.		
Physical Address	0x4500 10C4 0x4500 20C4 0x4500 30C4	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MASK_m_WR	Mask/Match of Wr Type: Control. Reset value: 0x0.	RW	0

Table 14-333. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_WR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-334. L3_STCOL_FILTER_i_MASK_m_ERR

Address Offset	See Table 14-227.		
Physical Address	0x4500 10D0 0x4500 20D0 0x4500 30D0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

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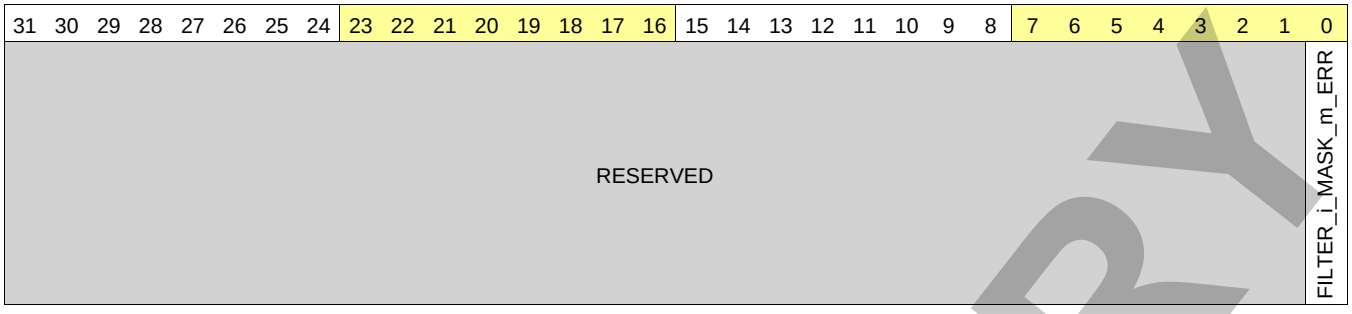


Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MASK_m_ERR	Mask/Match of Err Type: Control. Reset value: 0x0.	RW	0

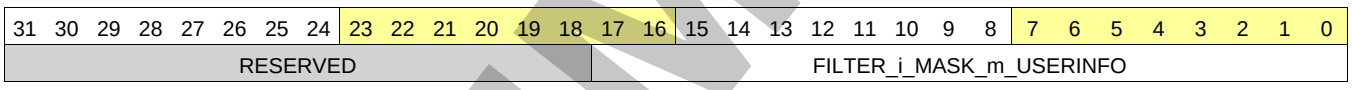
Table 14-335. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_ERR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-336. L3_STCOL_FILTER_i_MASK_m_USERINFO

Address Offset	See Table 14-227.		
Physical Address	0x4500 10D4	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	FILTER_i_MASK_m_USERINFO	Mask/Match of UserInfo Type: Control. Reset value: 0x0.	RW	0x00000

Table 14-337. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_USERINFO

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-338. L3_STCOL_FILTER_i_MASK_m_SLVADDR

Address Offset	See Table 14-227.		
Physical Address	0x4500 20CC 0x4500 30CC	**Instance**	CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

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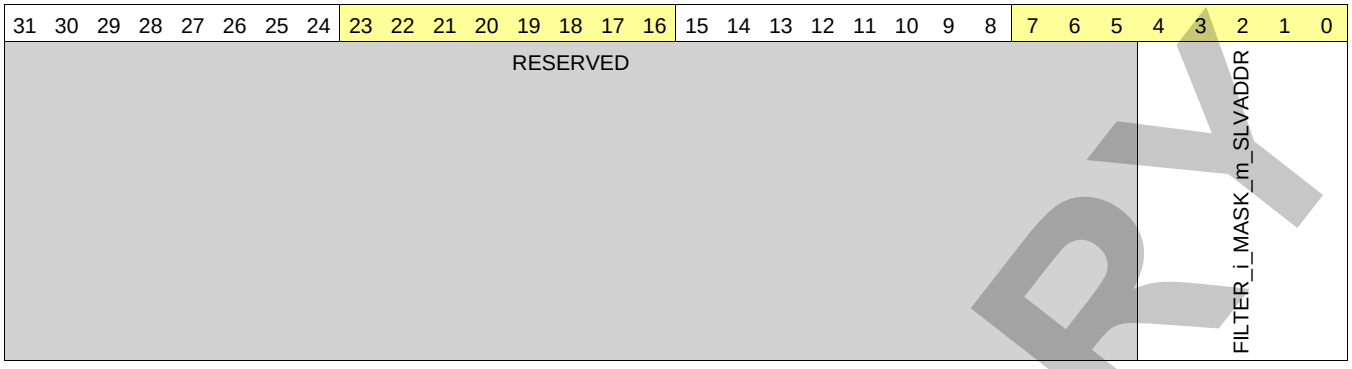


Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000 0000
4:0	FILTER_i_MASK_m_SLVADDR	Mask/Match of SlvAddr Type: Control. Reset value: 0x0.	RW	0x00

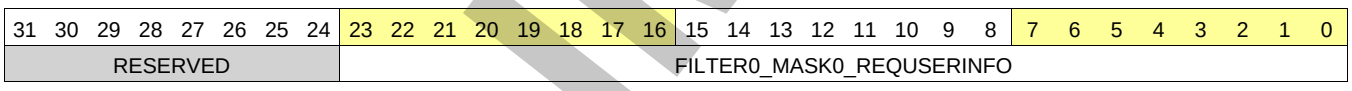
Table 14-339. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_SLVADDR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-340. L3_STCOL_FILTER_i_MASK_m_REQUSERINFO

Address Offset	See Table 14-227.		
Physical Address	0x4500 20D4 0x4500 30D4	**Instance**	CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x0000 0000
23:0	FILTER_i_MASK_m_REQUSERINFO	Mask/Match of ReqUserInfo Type: Control. Reset value: 0x0.	RW	0x00

Table 14-341. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_REQUSERINFO

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-342. L3_STCOL_FILTER_i_MASK_m_RSPUSERINFO

Address Offset	See Table 14-227.		
Physical Address	0x4500 20D8 0x4500 30D8	**Instance**	CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

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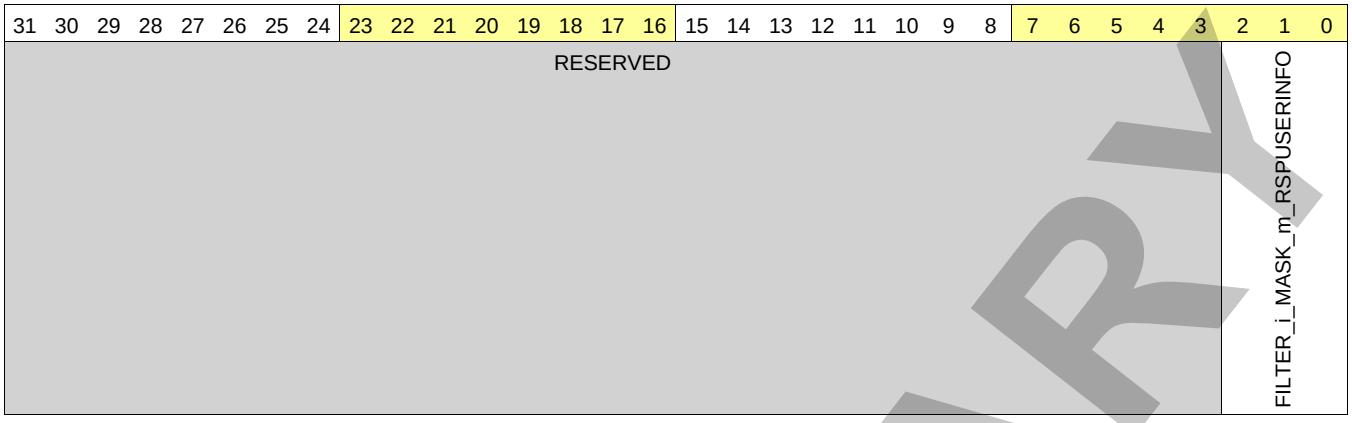


Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	FILTER_i_MASK_m_RSPUSERINFO	Mask/Match of RspUserInfo Type: Control. Reset value: 0x0.	RW	0x0

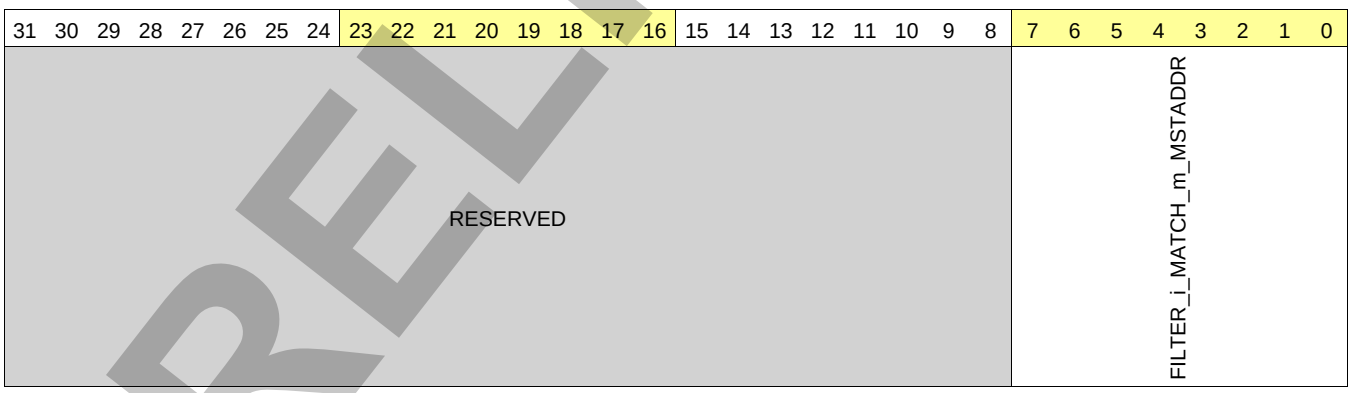
Table 14-343. Register Call Summary for Register L3_STCOL_FILTER_i_MASK_m_RSPUSERINFO

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-344. L3_STCOL_FILTER_i_MATCH_m_MSTADDR

Address Offset	See Table 14-227.		
Physical Address	0x4500 10E8 0x4500 20E8 0x4500 30E8	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	FILTER_i_MATCH_m_MSTADDR	Mask/Match of MstAddr Type: Control. Reset value: 0x0.	RW	0x00

Table 14-345. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_MSTADDR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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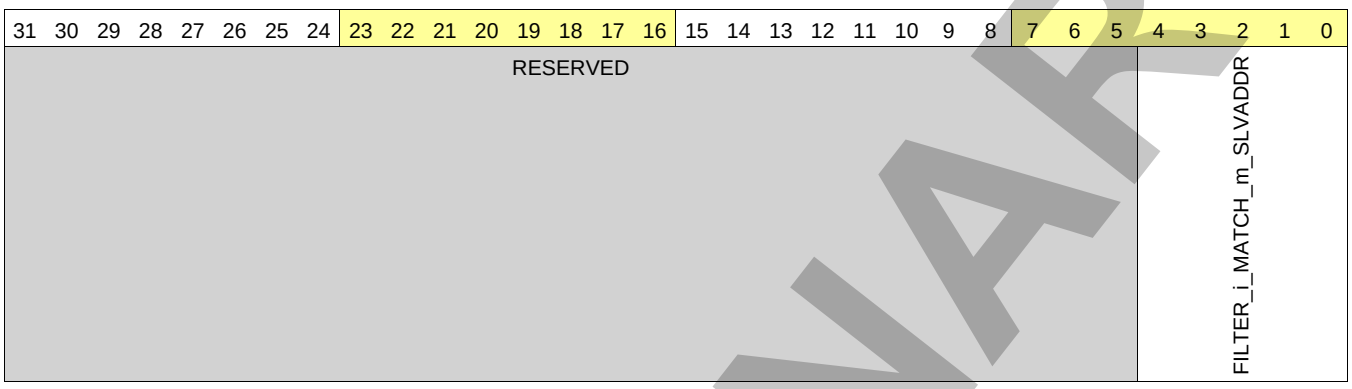
Table 14-346. L3_STCOL_FILTER_i_MATCH_m_SLVADDR

Address Offset	See Table 14-227.		
Physical Address	0x4500 20EC 0x4500 30EC	**Instance**	CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000 0000
4:0	FILTER0_MATCH0_SLVADDR	Mask/Match of SlvAddr Type: Control. Reset value: 0x0.	RW	0x00

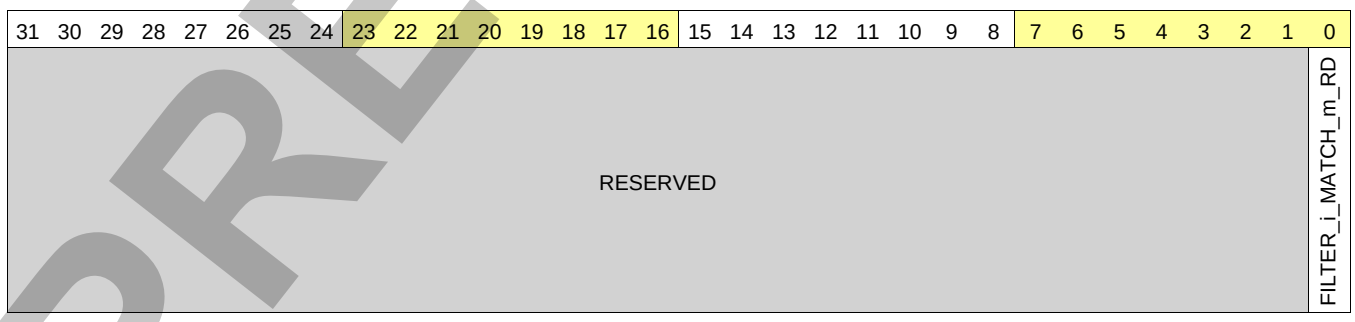
Table 14-347. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_SLVADDR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-348. L3_STCOL_FILTER_i_MATCH_m_RD

Address Offset	See Table 14-227.		
Physical Address	0x4500 10E0 0x4500 20E0 0x4500 30E0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MATCH_m_RD	Mask/Match of Rd Type: Control. Reset value: 0x0.	RW	0

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Table 14-349. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_RD

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-350. L3_STCOL_FILTER_i_MATCH_m_WR

Address Offset	See Table 14-227.		
Physical Address	0x4500 10E4 0x4500 20E4 0x4500 30E4	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MATCH_m_WR

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MATCH_m_WR	Mask/Match of Wr Type: Control. Reset value: 0x0.	RW	0

Table 14-351. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_WR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-352. L3_STCOL_FILTER_i_MATCH_m_ERR

Address Offset	See Table 14-227.		
Physical Address	0x4500 10F0 0x4500 20F0 0x4500 30F0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FILTER_i_MATCH_m_ERR

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	FILTER_i_MATCH_m_ERR	Mask/Match of Err Type: Control. Reset value: 0x0.	RW	0

Table 14-353. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_ERR

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-354. L3_STCOL_FILTER_i_MATCH_m_USERINFO

Address Offset	See Table 14-227.		
Physical Address	0x4500 10F4	**Instance**	CLK3_STATCOLL_SDRAM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER_i_MATCH_m_USERINFO																									

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:0	FILTER_i_MATCH_m_USERINFO	Mask/Match of UserInfo Type: Control. Reset value: 0x0.	RW	0x00000

Table 14-355. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_USERINFO

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-356. L3_STCOL_FILTER_i_MATCH_m_REQUSERINFO

Address Offset	See Table 14-227.		
Physical Address	0x4500 20F4 0x4500 30F4	**Instance**	CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FILTER0_MASK0_REQUSERINFO																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x0000 0000
23:0	FILTER_i_MASK_m_REQUSERINFO	Mask/Match of ReqUserInfo Type: Control. Reset value: 0x0.	RW	0x00

Table 14-357. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_REQUSERINFO

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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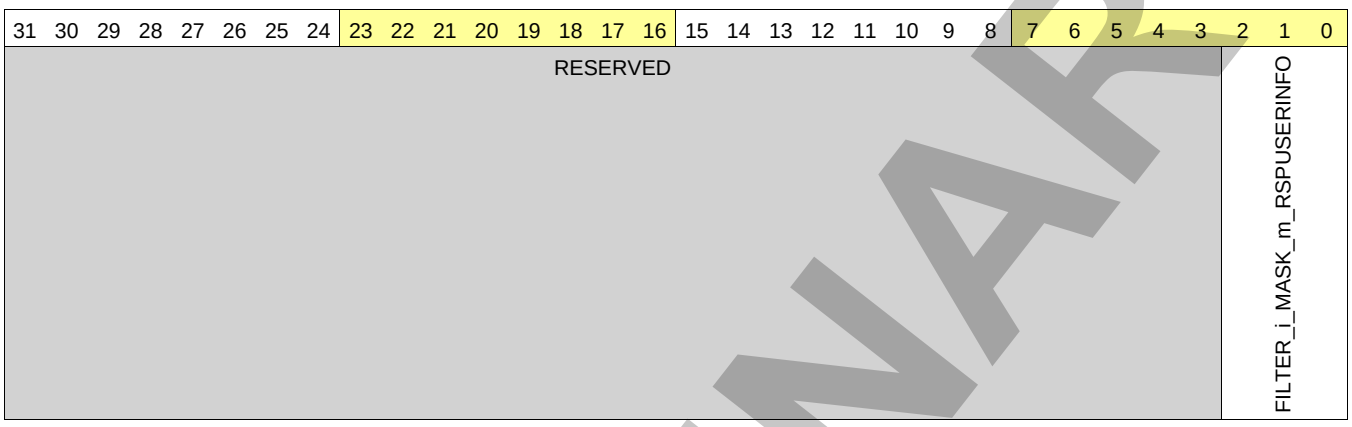
Table 14-358. L3_STCOL_FILTER_i_MATCH_m_RSPUSERINFO

Address Offset	See Table 14-227.		
Physical Address	0x4500 20F8 0x4500 30F8	**Instance**	CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	FILTER_i_MASK_m_RSPUSERINFO	Mask/Match of RspUserInfo Type: Control. Reset value: 0x0.	RW	0x0

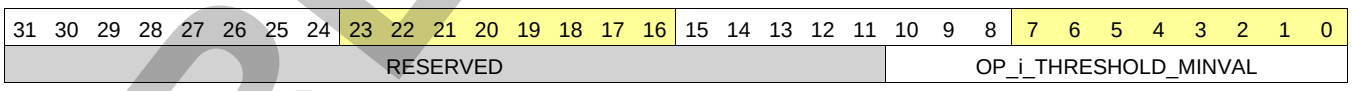
Table 14-359. Register Call Summary for Register L3_STCOL_FILTER_i_MATCH_m_RSPUSERINFO

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-360. L3_STCOL_OP_i_THRESHOLD_MINVAL

Address Offset	See Table 14-227.		
Physical Address	0x4500 11F0 0x4500 21F0 0x4500 31F0	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x00000
10:0	OP_i_THRESHOLD_MINVAL	Min value Type: Control. Reset value: 0x0.	RW	0x000

Table 14-361. Register Call Summary for Register L3_STCOL_OP_i_THRESHOLD_MINVAL

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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Table 14-362. L3_STCOL_OP_i_THRESHOLD_MAXVAL

Address Offset	See Table 14-227.		
Physical Address	0x4500 11F4 0x4500 21F4 0x4500 31F4	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					OP_i_THRESHOLD_MAXVAL										

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x00000
10:0	OP_i_THRESHOLD_MAXVAL	Max value Type: Control. Reset value: 0x0.	RW	0x000

Table 14-363. Register Call Summary for Register L3_STCOL_OP_i_THRESHOLD_MAXVAL

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

Table 14-364. L3_STCOL_OP_i_EVTINFOSEL

Address Offset	See Table 14-227.		
Physical Address	0x4500 11F8 0x4500 21F8 0x4500 31F8	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														OP_i_EVTINFOSEL	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000 0000
1:0	OP_i_EVTINFOSEL	Select event info data to add to counter (len/press or latency) Type: Control. Reset value: 0x0. 0x0: Select len from event info list 0x1: Select pressure if available from event info list 0x2: Select latency if available from event info list	RW	0x0

Table 14-365. Register Call Summary for Register L3_STCOL_OP_i_EVTINFOSEL

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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Table 14-366. L3_STCOL_OP_i_SEL

Address Offset	See Table 14-227.		
Physical Address	0x4500 11FC 0x4500 21FC 0x4500 31FC	**Instance**	CLK3_STATCOLL_SDRAM CLK3_STATCOLL_LAT0 CLK3_STATCOLL_LAT1
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OP_i_SEL			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	OP_i_SEL	Select logical operation Type: Control. Reset value: 0x0. 0x0: Increment counter on each mask/match filter hit 0x1: Increment counter on each min/max level hit 0x2: Add to counter the selected event info value (len/press or latency) 0x3: increment counter when all filter event hits (And(Fi)) 0x4: Increment counter if any of filter event hits (Or(Fi)) 0x5: Add to counter the number of current request event that hit 0x6: Add to counter the number of current response event that hit 0x7: Add to counter the number of all event that hit 0x8:Increment counter on each selected external event hit	RW	0x0

Table 14-367. Register Call Summary for Register L3_STCOL_OP_i_SEL

L3 Interconnect

- L3_MAIN STATCOLL Register Summary: [0]

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14.3 L4 Interconnects

This section details the device L4 interconnects.

14.3.1 L4 Interconnect Overview

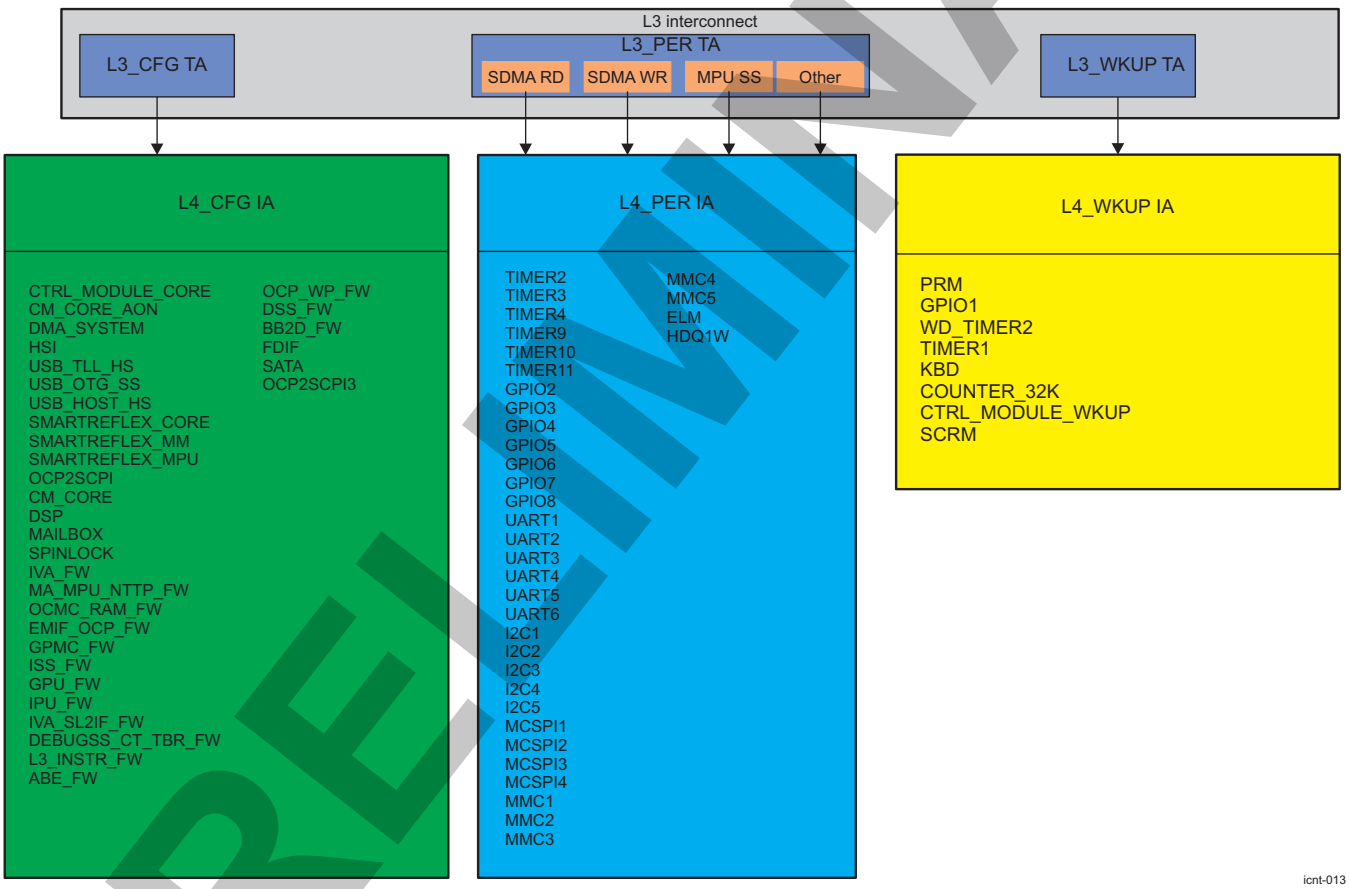
The device uses three separate L4 interconnect structures to connect peripheral modules. All L4s handle transfers with peripherals but are located in distinct power domains.

Figure 14-9 is an overview of the L4 interconnects and the peripherals attached to them.

The L4 interconnect is composed of the following interconnects:

- L4_CFG: Includes the majority of the configuration interface for L3_MAIN system modules and peripheral interconnect
- L4_PER: Includes the main peripherals that require sDMA access
- L4_WKUP: Includes peripherals attached to the WKUP power domain

Figure 14-9. L4 Interconnect Overview



The main features of the L4 interconnects are:

- Six ports from L3 interconnect onto three parallel L4 interconnects
- From one to four 32-bit initiator ports for each L4 interconnect instance
- 8-, 16-, or 32-bit data, single, or burst transactions
- Little-endian platform
- Nonblocking architecture with fair arbitration between threads
- Target interfaces: Fully synchronous or divided synchronous
- L4_CFG and L4_PER frequency equal half of L3 frequency
- Protection logic that provides user-configurable access control to targets by each initiator

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14.3.2 L4 Interconnect Integration

Table 14-368 and Table 14-369 summarize the integration of the module in the device.

Table 14-368. Integration Attributes

Module Instance	Attributes
	Power Domain
L4_PER	PD_L4_PER
L4_CFG	PD_CORE
L4_WKUP	PD_WKUPAON

Table 14-369. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L4_PER	L4_PER_CLK	L4PER_L4_GICLK	PRCM module	Functional and interface clock
L4_CFG	L4_CFG_CLK	L4CFG_L4_GICLK	PRCM module	Functional and interface clock
L4_WKUP	L4_WKUP_CLK	WKUPAON_GICLK	PRCM module	Functional and interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L4_PER	L4_PER_RST	L4_PER_RST	PRCM module	Reset of L4_PER interconnect
	L4_PER_RET_RST	L4_PER_PWRON_RET_RST	PRCM module	Reset of L4_PER interconnect retention registers. For information about retention reset, see Section 3.1.1, *Power, Reset, and Clock Management*.
L4_CFG	L4_CFG_RST	CORE_RST	PRCM module	Reset of L4_CFG interconnect
	L4_CFG_RET_RST	CORE_PWRON_RET_RST	PRCM module	Reset of L4_CFG interconnect retention registers. For information about retention reset, see Section 3.1.1, *Power, Reset, and Clock Management*.
L4_WKUP	L4_WKUP_RST	WKUPAON_RST	PRCM module	Reset of L4_WKUP interconnect

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14.3.3 L4 Interconnect Functional Description

14.3.3.1 Module Distribution

IAs and TAs provide the interface to connect the different modules to their associated interconnect.

Table 14-370 through Table 14-375 list all the modules and subsystems with their associated agents. The agents are listed for each L4 interconnect domain.

14.3.3.1.1 L4_PER Interconnect Agents

The L4_PER interconnect handles transfers only to peripherals in the PER power domain. Table 14-370 lists the L4_PER TAs.

Table 14-370. L4_PER TAs

Module Target Name	Description
UART1_TARG	UART port 1 module
UART2_TARG	UART port 2 module
UART3_TARG	UART port 3 module
UART4_TARG	UART port 4 module
UART5_TARG	UART port 5 module
UART6_TARG	UART port 6 module
TIMER2_TARG	General-purpose TIMER2 module
TIMER3_TARG	General-purpose TIMER3 module
TIMER4_TARG	General-purpose TIMER4 module
TIMER9_TARG	General-purpose TIMER9 module
TIMER10_TARG	General-purpose TIMER10 module
TIMER11_TARG	General-purpose TIMER11 module
GPIO2_TARG	General-purpose input/output 2 (GPIO2) module
GPIO3_TARG	GPIO3 module
GPIO4_TARG	GPIO4 module
GPIO5_TARG	GPIO5 module
GPIO6_TARG	GPIO6 module
GPIO7_TARG	GPIO7 module
GPIO8_TARG	GPIO8 module
I2C1_TARG	Multimaster I2C1 module
I2C2_TARG	Multimaster I2C2 module
I2C3_TARG	Multimaster I2C3 module
I2C4_TARG	Multimaster I2C4 module
I2C5_TARG	Multimaster I2C5 module
MCSPI1_TARG	Multichannel serial port interface controller 1 module
MCSPI2_TARG	Multichannel serial port interface controller 2 module
MCSPI3_TARG	Multichannel serial port interface controller 3 module
MCSPI4_TARG	Multichannel serial port interface controller 4 module
MMC1_TARG	MMC1 module
MMC2_TARG	MMC2 module
MMC3_TARG	MMC3 module
MMC4_TARG	MMC4 module
MMC5_TARG	MMC5 module
ELM_TARG	Error location module
HDQ1W_TARG	HDQ 1-Wire serial interface controller

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Four ports communicate between the L3 interconnect and the L4_PER interconnect to allow the L3_MAIN initiators to access the L4_PER targets. Table 14-371 lists the L4_PER initiator TAs.

For the list of initiators authorized to access the L4_PER peripherals, see Section 14.2.3.2.2, *Connectivity Matrix*.

Table 14-371. L4_PER IAs

Module Iniator Name	Description
L3_MAIN_P0_INIT	L3 sDMA RD interconnect port
L3_MAIN_P1_INIT	L3 sDMA WR interconnect port
L3_MAIN_P2_INIT	L3 MPU susbystem interconnect port
L3_MAIN_P3_INIT	L3 others interconnect port

14.3.3.1.2 L4_CFG Interconnect Agents

The L4_CFG interconnect handles only transfers to peripherals in the CORE power domain. Table 14-372 lists the TAs.

Table 14-372. L4_CFG TAs

Module Target Name	Description
CTRL_MODULE_CORE_TARG	Control module core
CM_CORE_AON_TARG	CORE_AON module
DMA_SYSTEM_TARG	System DMA module
HSI_TARG	High-speed synchronous serial interface module
USB_TLL_HS_TARG	High-speed USB_TLL module
USB_OTG_SS_TARG	USB_OTG module
USB_HOST_HS_TARG	High-speed multiport USB host controller module
SMARTREFLEX_CORE_TARG	SmartReflex core module
SMARTREFLEX_MM_TARG	SmartReflex MM module
SMARTREFLEX_MPU_TARG	SmartReflex MPU module
OCP2SCP1_TARG	OCP to SCP1 module
CM_CORE_TARG	CM_CORE module
DSP_TARG	DSP module
MAILBOX_TARG	MAILBOX module
SPINLOCK_TARG	SPINLOCK module
IVA_FW_TARG	IVA firewall
MPU_NTTP_FW_TARG	MPU NTTP firewall
OCMC_RAM_FW_TARG	OCMC_RAM firewall
EMIF_OCP_FW_TARG	EMIF L3 firewall
GPMC_FW_TARG	GPMC firewall
ISS_FW_TARG	ISS firewall
GPU_FW_TARG	GPU firewall
IPU_FW_TARG	IPU firewall
IVA_SL2IF_FW_TARG	IVA SL2 interface firewall
DEBUGSS_CT_TBR_FW_TARG	Debug subsystem CT TBR firewall
L3_INSTR_FW_TARG	L3 instruction firewall
ABE_FW_TARG	ABE firewall
OCP_WP_NOC_TARG	OCP_WP firewall
DSS_FW_TARG	Display subsystem firewall
FDIF_TARG	Face detection interface module
SATA_TARG	SATA module

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Table 14-372. L4_CFG TAs (continued)

Module Target Name	Description
BB2D_TARG	2D graphics accelerator module
OCP2SCP3_TARG	OCP-to-SCP3 module

A unique port, L3_MAIN_INIT, communicates between the L3 interconnect and the L4_CFG interconnect to allow the L3 initiators to access the L4_CFG targets (see Table 14-373).

For the list of initiators authorized to access the L4_CFG peripherals, see Section 14.2.3.2.2, *Connectivity Matrix*.

Table 14-373. L4_CFG IAs

Module Iniator Name	Description
L3_MAIN_INIT	L3 interconnect port

14.3.3.1.3 L4_WKUP Interconnect Agents

The L4-WKUP interconnect handles transfers only to peripherals in the WKUP power domain. Table 14-374 lists the TAs. Table 14-375 lists the L4 WKUP IAs.

Table 14-374. L4_WKUP TAs

Module Target Name	Description
GPIO1_TARG	GPIO1 module
32KTIMER_TARG	32-kHz timer module
SAR_RAM_TARG	Save-and-restore RAM
KEYBOARD_TARG	Keyboard module
CTRL_MODULE_WKUP_TARG	Control module WKUP module
PRM_TARG	Power reset management module
SCRM_TARG	System clock and reset management module
WD_TIMER2_TARG	Watchdog TIMER2 module
TIMER1_TARG	General-purpose TIMER1 module

Table 14-375. L4_WKUP IAs

Module Iniator Name	Description
L3_MAIN_INIT	L3 interconnect port

14.3.3.2 Power Management

As part of the system-wide power-management scheme, the L4 interconnects go into IDLE state after receiving a request from the PRCM module after all commands are serviced. This function is handled by hardware. For more information, see Section 3.1.1, *Power, Reset, and Clock Management*.

To reduce power consumption, each L4 interconnect automatically performs internal clock autogating. This is managed by hardware; no software configurations or settings are required.

Retention is performed on all software-accessible registers at IAs, TAs, and firewalls. This process prevents reconfiguration after a clock domain switches off. For more information, see Section 3.1.1.2, *Power Management*, in Section 3.1.1, *Power, Reset, and Clock Management*.

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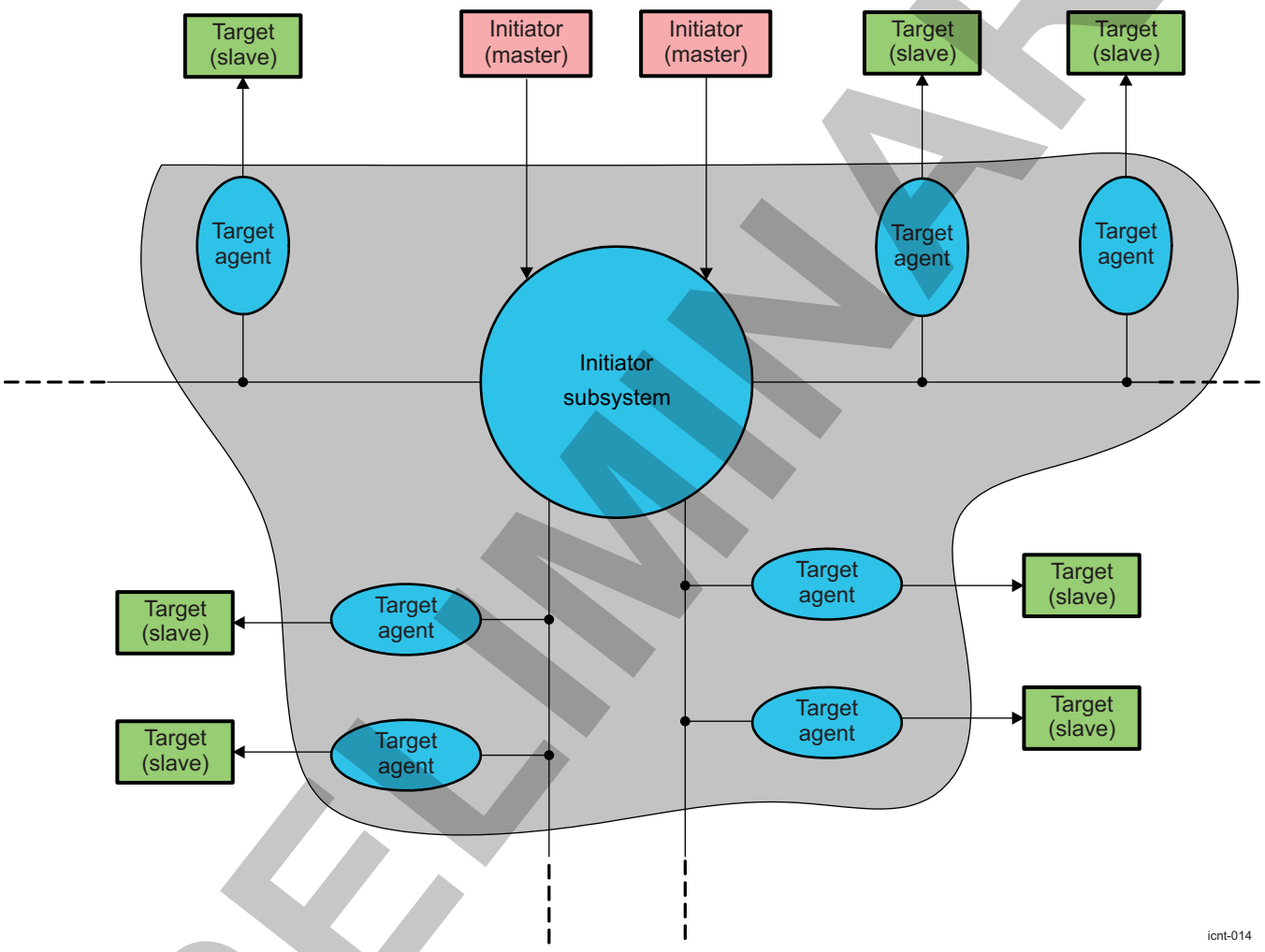
14.3.3.3 L4 Firewalls

Figure 14-10 is an internal view of the L4 interconnects in the overall interconnect. This architecture, with one initiator subsystem centralizing all initiator master requests and distributing them to all target modules (peripherals), enables the L4 interconnect firewall functions to be centralized at the L4 initiator subsystem level. The L4 firewall filters the accesses based on the configurable protection groups defined in the L4 address protection (AP) registers. Each module or TA is assigned to a protection group. The configuration is also defined in the L4 AP and is programmable on a module-per-module basis.

Figure 14-10. L4 Initiator-Target Connectivity



NOTE: As Figure 14-10 shows, targets are attached to branches. Branches do not impact the function of the L4 interconnect but are present to simplify timing closure and reduce active power consumption.

Because of the large address spaces and the number of peripherals connected to an L4 interconnect, two parameters are used to set up access permission:

- Programmable groups for initiators:
  - Eight protection groups for the L4 interconnect
- Segments divided into regions
  - 85 regions for the L4_PER interconnect
  - 112 regions for the L4_CFG interconnect
  - 30 regions for the L4_WKUP interconnect

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Protection group members are TAs with the same protection settings. A region is programmed to allow access to a unique selectable protection group. For better protection, different regions are grouped into protection group regions and associated with a protection group member.

14.3.3.3.1 Protection Group

A protection group is defined by its initiators (or members) and MReqInfo is allowed. Two registers define these two settings:

- The 64-bit CONNID_BIT_VECTOR field L4_AP_PROT_GROUP_MEMBERS_k_L and L4_AP_PROT_GROUP_MEMBERS_k_H registers define which initiator belongs to a group. A protection group is accessible by an initiator when the bit position corresponding to its ConnID is set to 1 in the CONNID_BIT_VECTOR field. Table 14-376 lists all the ConnIDs available at the L4 levels.
- The ENABLE field L4_AP_PROT_GROUP_ROLES_k_L register lists all possible MReqInfo combinations associated with the L4_AP_PROT_GROUP_MEMBERS register. Setting a Req bit in this register determines the initiators type of access. For more information, see Section 14.2.3.8, *L3 Firewall Functionality*. Two MReqInfos are used in L4 interconnects: MReqDebug and MReqSupervisor.

NOTE: Permissions are identical for read and write accesses in L4 interconnect.

k indicates the protection group number.

L indicates the region number.

Table 14-376. L4 ConnID Definition

ConnID	Initiator
0	Cortex-A15 MPU subsystem
1	Debug subsystem
2	DSP subsystem
3	IVAHD
4	ISS, IPU, Face Detect
5	sDMA
6	GPU, BB2D
7	Reserved
8	Reserved
9	HSI
A	MMC1, MMC2, SATA
B	Reserved
C	USB
D	Reserved
E	Reserved
F	Resered

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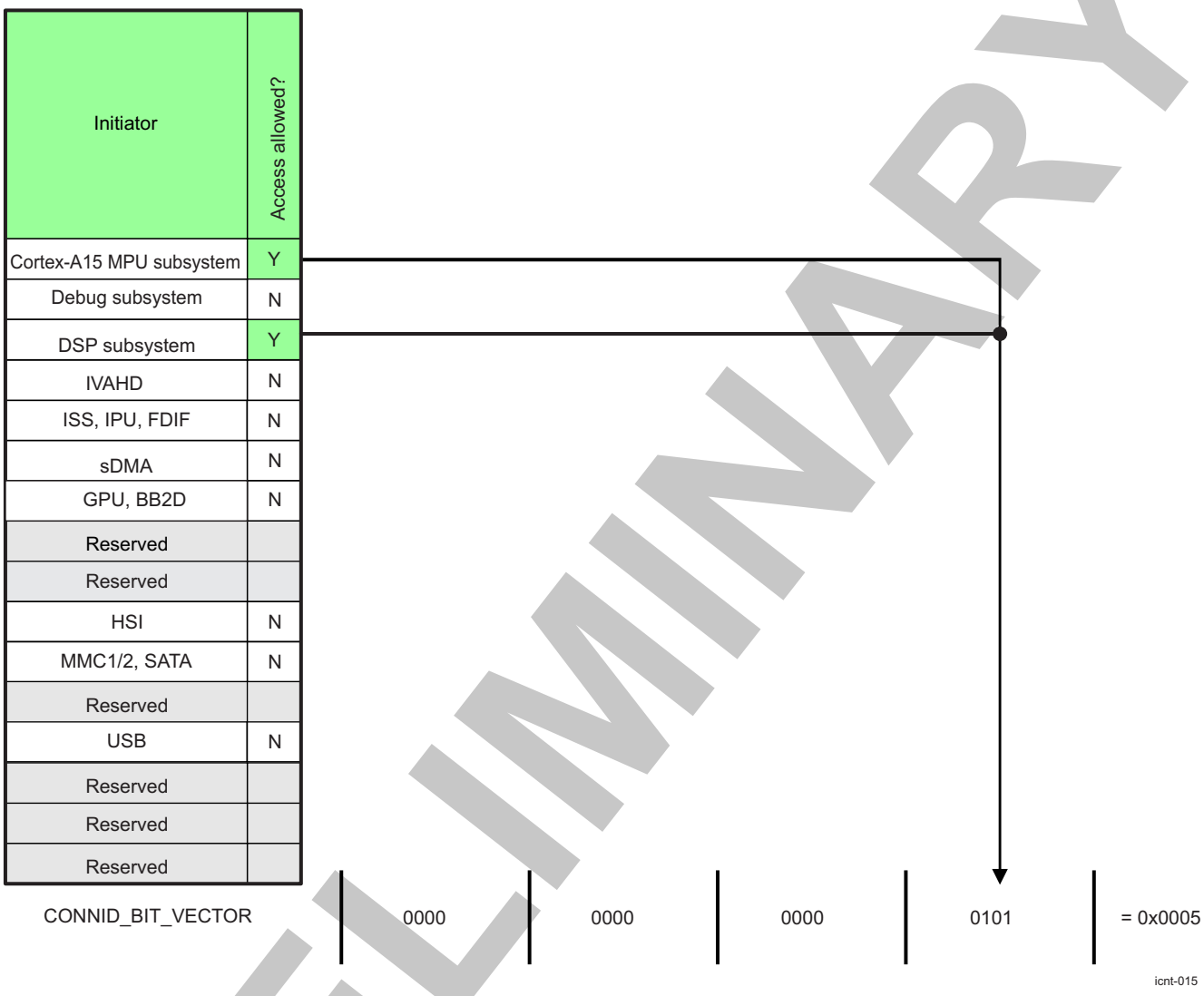
Figure 14-11 is an example of CONNID_BIT_VECTOR.

Figure 14-11. Example of CONNID_BIT_VECTOR L4_AP_PROT_GROUP_MEMBERS_k



Setting bits 0 and 2 in the PROT_GROUP_ID_1 register defines a group initiator that can access targets in protection group 1, and includes the following:

- Cortex-A15 MPU subsystem
- DSP subsystem

Protection group 1 can be applied to multiple protection regions with no limitation. Each protection region that is configured with protection group 1 enables permission access only to the two initiators.

The L4_AP_REGION_i_H PROT_GROUP_ID field determines the region to which the protection group member is attached.

The values of some CONNID_BIT_VECTOR and ENABLE fields are exported by the system control module (SCM) at reset or are user writable (see Figure 14-11 for more information).

Table 14-377 and Table 14-378 list the default configuration of the various groups for each L4 interconnect. For each group, some modules or regions are associated with it using default initiator members.

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Table 14-377. L4_PER Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	L4_PER_AP registers	L4_AP_PROT_GROUP_ROLES_0_L	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_ROLES_0_H	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_0_L	No	0xFFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_0_H	No	0xFFFF (all)
Group 1	Reserved	L4_AP_PROT_GROUP_ROLES_1_L	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_ROLES_1_H	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_1_L	No	0xFFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_1_H	No	0xFFFF (all)
Group 2–6 Free	No modules attached	L4_AP_PROT_GROUP_ROLES_k_L L4_AP_PROT_GROUP_ROLES_k_H where k = 2 to 6	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_k_L L4_AP_PROT_GROUP_MEMBERS_k_H where k = 2 to 6	Yes	0xFFFF (all)
Group 7 Other modules	Other L4_PER modules	L4_AP_PROT_GROUP_ROLES_7_L L4_AP_PROT_GROUP_ROLES_7_H	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_7_L L4_AP_PROT_GROUP_MEMBERS_7_H	Yes	0xFFFF (all)

Table 14-378. L4_CFG Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	AP registers	L4_AP_PROT_GROUP_ROLES_0_L L4_AP_PROT_GROUP_ROLES_0_H	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_0_L L4_AP_PROT_GROUP_MEMBERS_0_H	No	0xFFFF (all)
Group 1	L3 firewall registers	L4_AP_PROT_GROUP_ROLES_1_L L4_AP_PROT_GROUP_ROLES_1_H	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_1_L L4_AP_PROT_GROUP_MEMBERS_1_H	No	0xFFFF (all)

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Table 14-378. L4_CFG Firewall Default Configuration (continued)

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 5 Free	CPFROM	L4_AP_PROT_GROUP_ROLES_5_L L4_AP_PROT_GROUP_ROLES_5_H	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_5_L L4_AP_PROT_GROUP_MEMBERS_5_H	Yes	0xFFFF (all)
Group 2, 3, 4, and 6 Free	No modules attached	L4_AP_PROT_GROUP_ROLES_k_L L4_AP_PROT_GROUP_ROLES_k_L where k = 2, 3, 4 and 6	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_k_L L4_AP_PROT_GROUP_MEMBERS_k_H where k = 2, 3, 4, and 6	Yes	0xFFFF (all)
Group 7 Other modules	Other L4_CFG modules	L4_AP_PROT_GROUP_ROLES_7_L L4_AP_PROT_GROUP_ROLES_7_H	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_7_L L4_AP_PROT_GROUP_MEMBERS_7_H	Yes	0xFFFF (all)

Table 14-379. L4_WKUP Firewall Default Configuration

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 0 AP registers	AP registers	L4_AP_PROT_GROUP_ROLES_0_L L4_AP_PROT_GROUP_ROLES_0_H	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_0_L L4_AP_PROT_GROUP_MEMBERS_0_H	No	0xFFFF (all)
Group 1	Reserved	L4_AP_PROT_GROUP_ROLES_1_L L4_AP_PROT_GROUP_ROLES_1_H	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_1_L L4_AP_PROT_GROUP_MEMBERS_1_H	No	0xFFFF (all)
Group 2	No Modules Attached	L4_AP_PROT_GROUP_ROLES_5_L L4_AP_PROT_GROUP_ROLES_5_H	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_5_L L4_AP_PROT_GROUP_MEMBERS_5_H	Yes	0xFFFF (all)

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Table 14-379. L4_WKUP Firewall Default Configuration (continued)

Group	Default Modules Associated With Group	Register	Modifiability	Default Value
Group 3, 4 Free	Reserved	L4_AP_PROT_GROUP_ROLES_k_L L4_AP_PROT_GROUP_ROLES_k_L where k = 3, 4	No	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_k_L L4_AP_PROT_GROUP_MEMBERS_k_H where k = 3, 4	No	0xFFFF (all)
Group 5-7 Other modules	Other L4_WKUP modules	L4_AP_PROT_GROUP_ROLES_7_L L4_AP_PROT_GROUP_ROLES_7_H	Yes	0xFFFF FFFF FFFF FFFF (all)
		L4_AP_PROT_GROUP_MEMBERS_7_L L4_AP_PROT_GROUP_MEMBERS_7_H	Yes	0xFFFF (all)

14.3.3.3.2 Segments and Regions

The protection mechanism for L4 interconnects is based on a hierarchical segmentation, as shown in Figure 14-12. By default, some regions are attached to specific protection group members. This specificity lets users set up the permission access to certain types of modules requiring the same access protection without managing region allocation.

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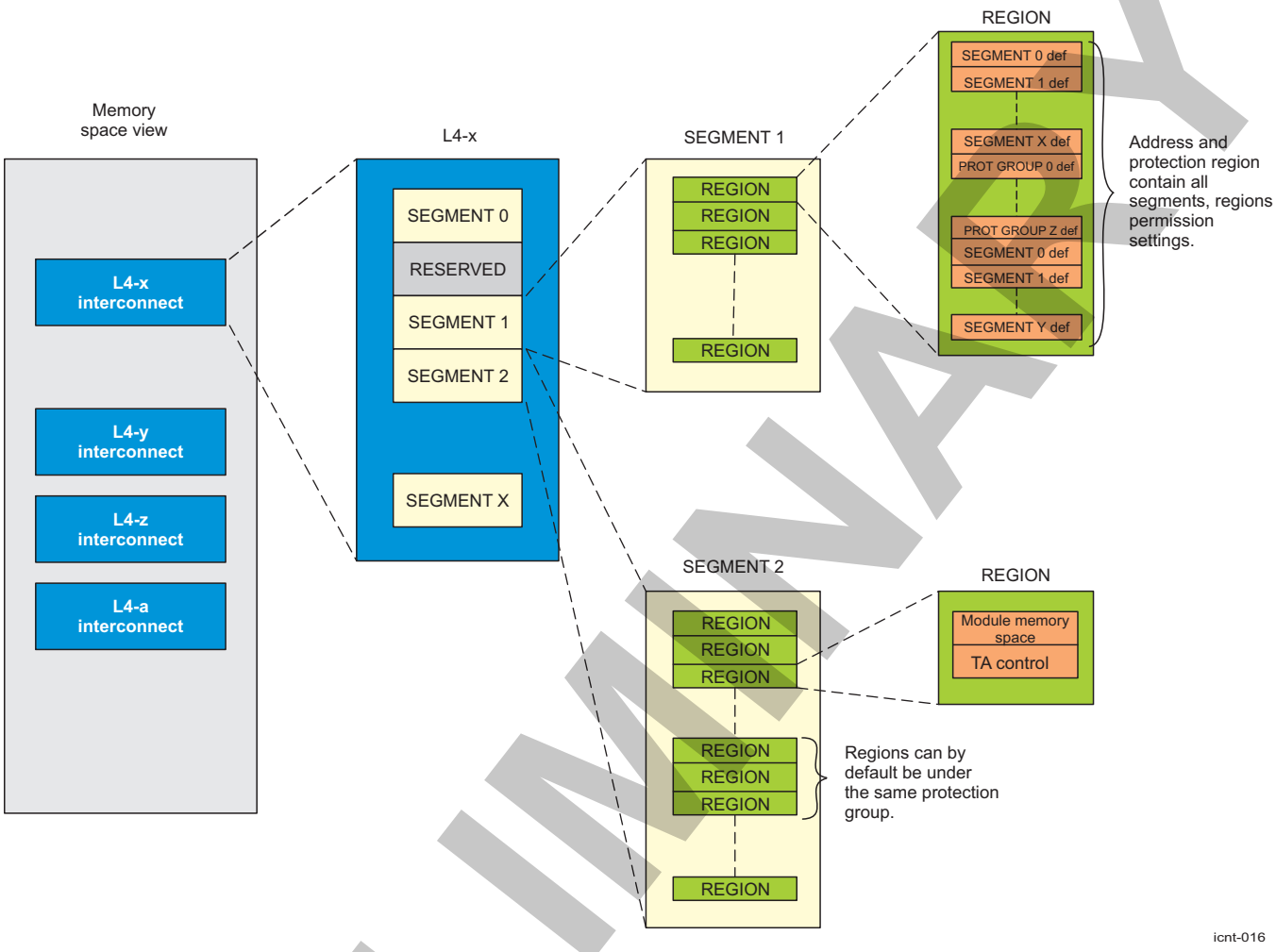
Figure 14-12. L4 Segmentation



All interconnect address spaces are covered by regions. Table 14-380 through Table 14-382 list the module mapping with their addresses, region numbers, and default protection group allocated to them.

NOTE: Module refers to the configuration registers of the module.

TA refers to the interconnect configuration registers of the TA associated with the module.

Table 14-380. Region Allocations for L4_PER Interconnect

Module	Region	Description
L4_PER CONFIG	0	Firewall
	1	PER_IA_0
	2	Link agent
UART3	3	TA
	4	Module
TIMER2	5	TA
	6	Module
TIMER3	7	TA
	8	Module

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Table 14-380. Region Allocations for L4_PER Interconnect (continued)

Module	Region	Description
TIMER4	9	TA
	10	Module
TIMER9	11	TA
	12	Module
GPIO2	13	TA
	14	Module
GPIO3	15	TA
	16	Module
GPIO4	17	TA
	18	Module
GPIO5	19	TA
	20	Module
GPIO6	21	TA
	22	Module
I2C3	23	TA
UART1	24	TA
	25	Module
UART2	26	TA
	27	Module
UART4	28	TA
	29	Module
I2C1	30	TA
	31	Module
I2C2	32	TA
	33	Module
I2C3	34	Module
GPIO8	35	TA
	36	Module
HDQ1W	37	TA
	38	Module
ELM	39	TA
	40	Module
TIMER10	41	TA
	42	Module
TIMER11	43	TA
	44	Module
GPIO7	45	TA
	46	Module
MSCPI1	47	TA
	48	Module
MSCPI2	49	TA
	50	Module
MMC1	51	TA
	52	Module
UART6	53	TA
	54	Module

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Table 14-380. Region Allocations for L4_PER Interconnect (continued)

Module	Region	Description
Reserved	55	TA
	56	Module
Reserved	57	TA address space 0
	58	Module
Reserved	59	TA
	60	Module
MMC3	61	TA
	62	Module
UART5	63	TA
	64	Module
MMC2	65	TA
	66	Module
MCSPI3	67	TA
	68	Module
MCSPI4	69	TA
	70	Module
MMC4	71	TA
	72	Module
MMC5	73	TA
	74	Module
Reserved	75	TA
	76	Module
L4_PER CONFIG	77	PER_IA_1
	78	PER_IA_2
	79	PER_IA_3
Reserved	80	TA address space 1
I2C4	81	TA
	82	Module
I2C5	83	TA
	84	Module

Table 14-381. Region Allocations for L4_CFG Interconnect

Module	Region	Description
L4_CFG CONFIG	0	Firewall
	1	CFG_IA_0
	2	Link agent
CTRL_MODULE_CORE	3	TA
	4	Module
CM_CORE_AON	5	TA
	6	Module
DMA_SYSTEM (sDMA)	7	TA
	8	Module
HSI	9	Module
	10	TA
USB_TLL_HS	11	TA
	12	Module

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Table 14-381. Region Allocations for L4_CFG Interconnect (continued)

Module	Region	Description
SMARTREFLEX_MPU	13	TA
	14	Module
SMARTREFLEX_MM	15	TA
	16	Module
SMARTREFLEX_CORE	17	TA
	18	Module
CM_CORE	21	TA
	22	Module
DSP subsystem	23	TA
	24	Module
Mailbox	25	TA
	26	Module
SPINLOCK	27	TA
	28	Module
IVA_SL2IF firewall	29	TA
	30	Module
MA firewall	31	TA
	32	Module
OCMC_RAM firewall	37	TA
	38	Module
EMIF firewall	39	TA
	40	Module
GPMC firewall	41	TA
	42	Module
ISS firewall	43	TA
	44	Module
GPU firewall	45	TaA
	46	Module
IPU firewall	47	TA
	48	Module
IVA_CFG firewall	49	TA
	50	Module
L3_INSTR firewall	51	TA
	52	Module
ABE firewall	53	TA
	54	Module
Reserved	55	TA
	56	Module
DSS firewall	57	TA
	58	Module
INTERCONN_WKUP	59	TA
	60	Module
P1500	61	TA
	62	Module
FACEDETECT	63	TA
	64	Module

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Table 14-381. Region Allocations for L4_CFG Interconnect (continued)

Module	Region	Description
USB_HOST_HS	71	TA
	72	Module
BB2D firewall	73	TA
	74	Module
DEBUGSS_CT_TBR firewall	75	TA
	76	Module
HSI	77	TA
	78	Module
INTERCONN_TO_SCP1 registers	83	TA
INTERCONN_TO_SCP1 SCP targets 0, 1, 2, 3	84	TA
INTERCONN_TO_SCP1 SCP targets 4, 5, 6, 7	85	TA
INTERCONN_TO_SCP1 SCP targets 8, 9, 10, 11	86	TA
INTERCONN_TO_SCP1 SCP targets 12, 13, 14, 15	87	TA
INTERCONN_TO_SCP1	88	Module
INTERCONN_TO_ SCP3 registers	89	TA
INTERCONN_TO_SCP3 targets 0, 1, 2, 3	90	TA
INTERCONN_TO_SCP3 targets 4, 5, 6, 7	91	TA
INTERCONN_TO_SCP3 targets 8, 9, 10, 11	92	TA
INTERCONN_TO_SCP3 targets 12, 13, 14, 15	93	TA
INTERCONN_TO_SCP3	94	Module
INTERCONN_TO_SCP2 registers	95	TA
INTERCONN_TO_SCP2 targets 0, 1, 2, 3	96	TA
INTERCONN_TO_SCP2 targets 4, 5, 6, 7	97	TA
INTERCONN_TO_SCP2 targets 8, 9, 10, 11	98	TA
INTERCONN_TO_SCP2 targets 12, 13, 14, 15	99	TA
INTERCONN_TO_SCP2	100	Module
SATA	101	TA
	102	Module
USB_OTG_SS	109	TA
	110	Module
HSI TARG	111	TA

Table 14-382. Region Allocations for L4_WKUP Interconnect

Module	Region	Description
L4 WKUP	0	AP
	1	WKUP_IA_0
	2	Link agent
PRM	3	TA
	4	Module
GPIO1	5	TA
	6	Module

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Table 14-382. Region Allocations for L4_WKUP Interconnect (continued)

Module	Region	Description
WD_TIMER2	7	TA
	8	Module
TIMER1	9	Module
	10	TA
KEYBOARD	11	TA
	12	Module
SAR_RAM1	13	TA
	14	Module
SCRM	15	TA
	16	Module
COUNTER_32K	17	TA
	18	Module
CTRL_MODULE_WKUP	19	TA
	20	Module
SAR_RAM2	25	TA

14.3.3.3.3 L4 Firewall Address and Protection Register Settings

Table 14-383 lists the settings of the AP registers relative to an L4 interconnect firewall. These values are computed based on the physical implementation of each L4 interconnect.

Table 14-383. L4 Firewall Register Description Overview

Register Type	Register Name	Bits	Field	Description
Segment	L4_AP_SEGMENT_i_L (1)	31:0	BASE	Segment base address
	L4_AP_SEGMENT_i_H (1)	5:0	SIZE	Segment size equals to 2^{SIZE}
Protection groups	L4_AP_PROT_GROUP_MEMBERS_k_L (2)	15:0	CONNID_BIT_VECTOR	For L4ConnID, see Table 14-376.
	L4_AP_PROT_GROUP_ROLES_k_L (2) L4_AP_PROT_GROUP_ROLES_k_H	31:0	ENABLE	See Section 14.2.3.8.3 for REQ_INFO description. (3)
Region setting	L4_AP_REGION_l_L (4)	20:0	BASE	Defines the base address of region with respect to its segment base address
	L4_AP_REGION_l_H (4)	31:28	MADDRSPACE	Target interconnect MAddrSpace
		26:24	SEGMENT_ID	Segment ID number of the region
		22:20	PROT_GROUP_ID	Protection group member attached to the region
		18:17	BYTE_DATA_WIDTH_EXP	Determines the number of bytes in an access
		14:8	PHY_TARGET_ID	Physical target ID
		6:1	SIZE	Size of the region equals to 2^{SIZE}
		0	ENABLE	Enables the region protection

(1) i = 0 to 1 for PER_AP
i = 0 to 6 for CFG_AP
i = 0 to 1 for WKUP_AP

(2) k = 0 to 7 for PER_AP
k = 0 to 7 for CFG_AP
k = 0 to 7 for WKUP_AP

(3) For L interconnects, only MReqDebug and MReqSupervisor are available.

(4) l = 0 to 84 for PER_AP
l = 0 to 111 for CFG_AP
l = 0 to 29 for WKUP_AP

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14.3.3.4 L4 Error Detection and Reporting

14.3.3.4.1 IA and TA Error Detection and Logging

The L4 interconnect provides mechanisms for handling internally detected errors or errors reported by modules attached to the L4 target ports.

NOTE: L4_IA denotes the IA for all L4 interconnects: L4_PER, L4_CFG, and L4_WKUP.

L4_TA denotes the TA for all L4 interconnects: L4_PER, L4_CFG, and L4_WKUP.

The L4 interconnects handle four types of errors:

- No target core found or address hole, detected and logged at IA
- Unsupported command, detected and logged at IA
- Protection violation, detected and logged at IA (see Section 14.3.3.3, *L4 Firewalls*)
- Target does not service a request before a time-out expires. The error is detected and logged at TA (see Section 14.3.3.4.2, *Time-Out*).

Table 14-384 lists the value of the L4_IA_ERROR_LOG_L[25:24] CODE bit field stored when an error occurs.

Table 14-384. L4 CODE Bit Field Definition

CODE (bits 1:0)	Error Type	REQ_INFO	Secondary	ConnID	CMD
0	No error				
1	Unsupported command	x	x	x	x
2	Address hole	x	x	x	x
3	Protection violation	x		x	x

- No target core found/address hole: This error indicates that a request was addressed to a hole in the L4 address map. When this error occurs, an in-band error response is returned to the L3 level. The error is also logged into the L4_IA_AGENT_STATUS_L[27] INBAND_ERROR bit. Additionally, an address hole error code is logged to the L4_IA_ERROR_LOG_L[25:24] CODE bit field.
- Unsupported command: This error indicates that the command type of the request is not supported by the accessed target register. The error is logged into the L4_IA_AGENT_STATUS_L[27] INBAND_ERROR bit. An unsupported command error code is written to the L4_IA_ERROR_LOG_L[25:24] CODE bit field for the initiator interface.
- Protection violation: This error indicates that a request is not issued from an allowed initiator member or is issued with the inappropriate ReqInfo qualifiers associated with the target region. This error is reported using an in-band error and is written to the L4_IA_AGENT_STATUS_L[27] INBAND_ERROR bit. A protection violation error code is saved into the L4_IA_ERROR_LOG_L[25:24] CODE bit field for the same initiator interface. A protection violation is also logged in the L4_IA_AGENT_STATUS_L[31] PROT_ERROR_SECONDARY or [30] PROT_ERROR_PRIMARY bit when in debug or applicative mode, respectively.

  The L4_IA_ERROR_LOG_L[30] SECONDARY bit indicates whether the error occurred in application or debug.

  The L4_IA_ERROR_LOG_H[15:0] REQ_INFO bit field returns the type of access (REQ_INFO qualifier) that caused the error.

  The L4_IA_ERROR_LOG_L[13:8] CONNID bit field returns the ID of the initiator that caused the error.

  The L4_IA_ERROR_LOG_ADDR_L[31:0] ADDR register logs the address for error conditions.

14.3.3.4.2 Time-Out

A time-out mechanism can be enabled at the interconnect level and on a per-target basis. If the mechanism is enabled for a TA and interconnect and commands are not accepted or responses are not returned within the expected delay, the L4 interconnect generates an error event.

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NOTE: The time-out mechanism is not available on the L4_WKUP interconnect, but L4_WKUP time-outs are detected in CFG_TA_L4WKUP of the L4_CFG interconnect.

The error is logged in the L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT bit. The affected TA enters an error state that causes it to send an error response to any new request targeted at it. To recover from this state, system software must reset the TA. The time-out is counted starting from the moment a command is presented to the target, regardless of the target response to this command.

The L4 interconnect implements a centralized time-base circuit that broadcasts a set of four periodic pulse signals to all connected TAs. The time-base circuit offers four possible sets of four time-base signals. The time-base signals are selected by programming the L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE bit field.

The selected time-base signals are available at any TA. Each TA can be programmed to refer to one of these four time-base signals, using the L4_TA_AGENT_CONTROL_L[10:8] REQ_TIMEOUT bit field. These four signals are referred to as 1X time-base, 4X time-base, 16X time-base, and 64X time-base.

Table 14-385 lists all values in number of L4 clock cycles.

Table 14-385. L4 Time-out Link and TA Programming

	L4_TA_AGENT_CONTROL_L [2:0] REQ_TIMEOUT				
L4_LA_NETWORK_CONTROL_L[2:0] TIMEOUT_BASE	**0**	**1**	**2**	**3**	**4**
0	All L4 time-out features are disabled.				
1	Locally disabled	64	256	1024	4096
2		256	1024	4096	16,384
3		1024	4096	16,384	65,536
4		4096	16,384	65,536	262,144

The default reset value is 0x2 for REQ_TIMEOUT and 0x4 for TIMEOUT_BASE, implying 16,384 clock cycles.

A time-out condition is detected when the command acceptance or the response is not received after a delay of from one to three time-base periods.

Example:

- L4 frequency = 65-MHz, 15.3-µs period
- TIMEOUT_BASE = 4 in the L4_LA_NETWORK_CONTROL_L register
- REQ_TIMEOUT = 2 in the L4_TA_AGENT_CONTROL_L for TA A
- REQ_TIMEOUT = 4 in the L4_TA_AGENT_CONTROL_L for TA B

At agent A, the time-base unit is 16,384 cycles. A time-out is issued when a request to the attached module is not accepted, or no response is sent after a delay of 252 µs to 756 µs.

At agent B, the time-base unit is 262,144 cycles. A time-out is issued when a request to the attached module is not accepted or no response is sent after a delay of 4 ms to 12 ms.

When a time-out condition is detected, the TA logs the error in the L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT bit, and it also reports the error to the IA, which forwards it to the L3 interconnects.

After the time-out is detected and logged, the behavior of the attached module is ignored. A new request targeting the module arriving at the timed-out TA receives an error response. If the request is addressed to the agent internal registers, it is processed normally.

To recover from a time-out error, software is assumed to first reset the faulty module and then the TA using the L4_TA_AGENT_CONTROL_L[0] OCP_RESET bit.

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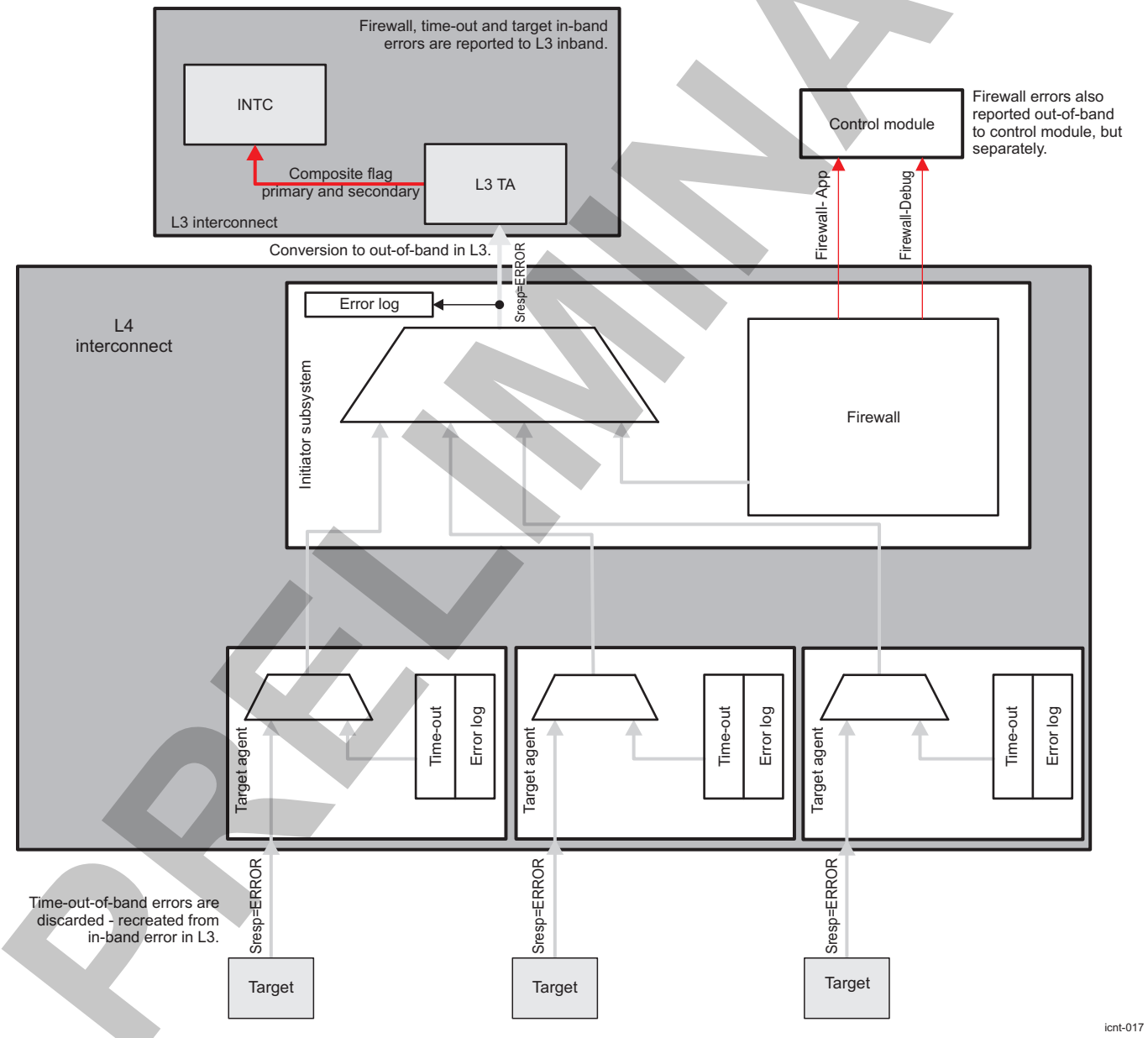
14.3.3.4.3 Error Reporting

Figure 14-13 shows the error-reporting scheme used in the L4 interconnects. All L4 in-band errors are reported to their respective L3 TA, where errors are converted in an out-of band error signal (the L3 applicative and debug composite flags) going to the L3 INTCs.

Two levels of mask are present to report the error at INTC level:

- At the applicative and debug composite flag, to enable interrupt reporting, the following bits must be set:
  - L4_CFG in L3_CLK1_FLAG_MASK_0[3] and L3_CLK1_FLAG_STATUS_1[3]
  - L4_PER in L3_CLK2_FLAG_MASK_0[17][16][15][6] and L3_CLK2_FLAG_STATUS_1[17][16][15][6]
- At the L3 TA level, see Section 14.2.1, *L3 Interconnect*.

Figure 14-13. L4 Error Reporting



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14.3.3.4.4 Error Recovery

Setting the L4_TA_AGENT_CONTROL_L[0] OCP_RESET bit to 1 initiates the software reset period. Software reset must be asserted for at least 16 cycles of the target module interface clock, which can be a divided clock with respect to the L4 clock.

During the software reset period:

- Requests sent to the target module receive error responses. Therefore, if the faulty request is part of a DMA transfer, it is necessary to stop the DMA to prevent unwanted errors.
- Requests sent to the TA register block are processed as usual.
- The L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT status bit is cleared.

Setting the L4_TA_AGENT_CONTROL_L[0] OCP_RESET bit to 0 terminates the software reset period.

Reset the attached module to complete the recovery.

14.3.3.4.5 Firewall Error Logging in the Control Module

When a protection violation occurs, an interrupt is send to the INTCs (if enabled). An in-band error is sent back to L3 IA and an out-of-band error can also be logged in the CONTROL.CONTROL_SEC_ERR_STATUS register in the SCM. These out-of-band errors are enabled and disabled at the L4 IA level by setting the L4_IA_AGENT_CONTROL_L[31][30] PROT_ERROR_SECONDARY_REP or PROT_ERROR_PRIMARY_REP bit to 1 for debug and application mode, respectively.

At the control module level, two logging registers are used, depending on the mode:

- In application mode or primary error reporting:
  - CONTROL_CORE_SEC_ERR_STATUS_FUNC[16] = L4_CFG protection violation
  - CONTROL_CORE_SEC_ERR_STATUS_FUNC[17] = L4_PER protection violation
  - CONTROL_CORE_SEC_ERR_STATUS_FUNC[22] = L4_WKUP protection violation
- In debug mode or secondary error reporting:
  - CONTROL_CORE_SEC_ERR_STATUS_DEBUG[16] = L4_CFG protection violation
  - CONTROL_CORE_SEC_ERR_STATUS_DEBUG[17] = L4_PER protection violation
  - CONTROL_CORE_SEC_ERR_STATUS_DEBUG[22] = L4_WKUP protection violation

NOTE: The CONTROL_CORE_SEC_ERR_STATUS_xxx registers are only readable.

Figure 14-14 shows the global protection error reporting to the control module.

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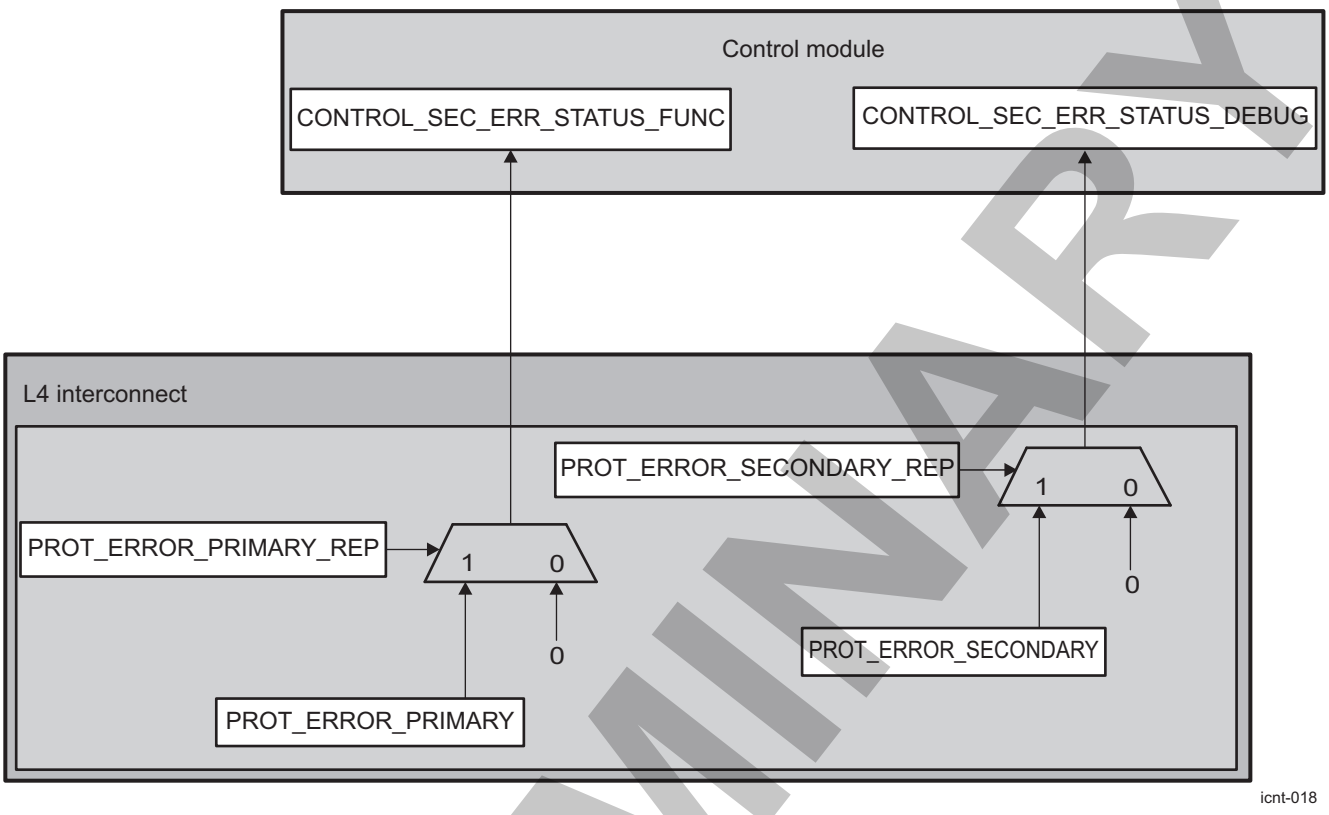
Figure 14-14. Protection Violation Out-of-Band Error Reporting



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14.3.4 L4 Interconnect Programming Guide

14.3.4.1 L4 Interconnect Low-level Programming Models

This section describes the low-level hardware programming sequences for configuring and using the L4 interconnect module.

14.3.4.1.1 Global Initialization

14.3.4.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the L4 interconnect module is used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the L4 interconnect. For more information, see Section 14.3.2, *L4 Interconnect Integration*.

Table 14-386 lists the surrounding modules.

Table 14-386. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	For more information about the configuration of the module, see Section 3.1.1, *Power, Reset, and Clock Management*.
Control module	For more information about the configuration of the module, see Figure 18-1, *Control Module*.
MPU INTC	Configure the MPU INTC to enable the interrupts from L4 interconnect module. SeeSection 17.1 *Interrupt Controllers*.
sDMA	For more information about the configuration of the sDMA, see Section 16.1, *sDMA*.
L3 interconnect	For more information about the interconnect configuration, see Section 14.2.1, *L3 Interconnect*.

14.3.4.1.2 Operational Modes Configuration

14.3.4.1.2.1 L4 Interconnect Error Analysis Mode

14.3.4.1.2.1.1 Main Sequence: L4 Interconnect Error Analysis Mode

The information required to analyze an error source is logged in several registers. The number of registers to access depends on the error source.

Figure 14-15 shows the software sequence required in most cases.

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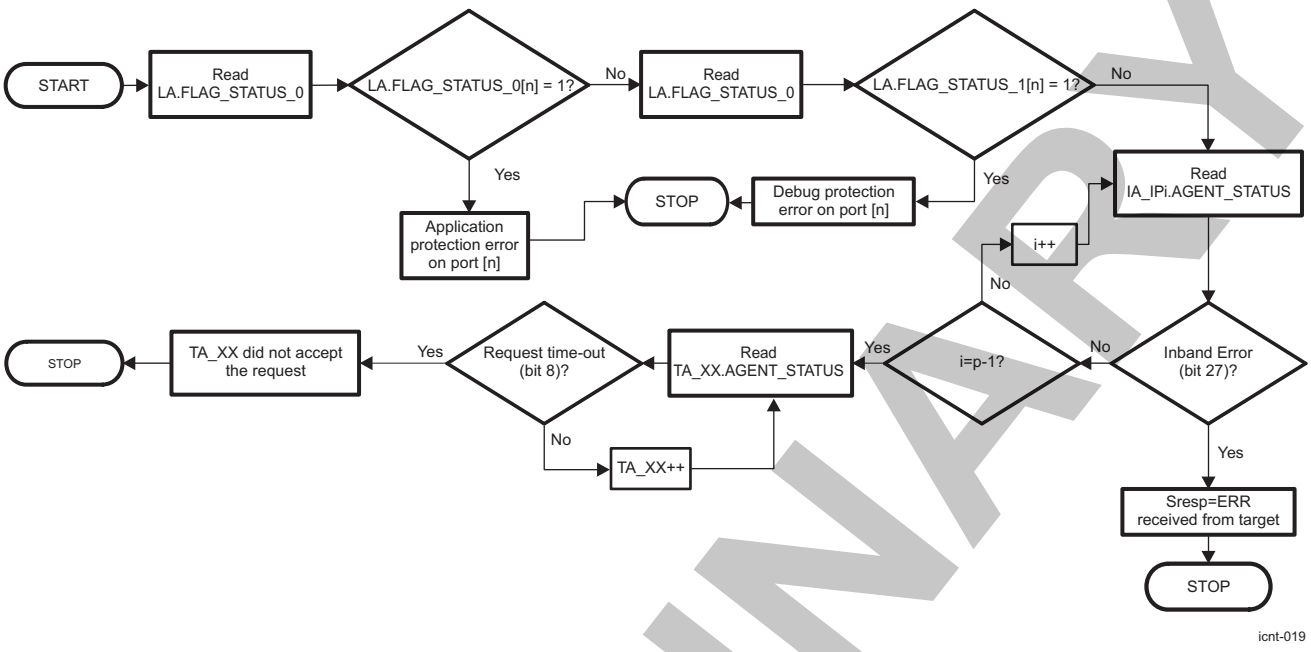
Figure 14-15. Typical Error Analysis Sequence



NOTE: L4 interconnects don't log any address or other specific information for a custom error returned from any target IP. They rather pass an error response ut to the master supposed to analyze it.

In case of posted writes, the master access completes before it actually completed at the end slave level, this way no error response is sent back to the master, making it impossible to have a direct way of uderstanding the origin of L4 error during posted writes. However, even though no address is logged, an error flag is generated and needs to be processed.

14.3.4.1.2.1.2 Subsequence: L4 Interconnect Protection Violation Error Identification

This procedure describes the protection violation error identification (see Table 14-387).

Table 14-387. Protection Violation Error Identification

Step	Register/Bit Field/Programming Model	Value
Read multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	
Read initiator ID.	L4_IA_ERROR_LOG_L[11:8] CONNID	
Read command that cause the error.	L4_IA_ERROR_LOG_L[2:0] CMD	
Read address of request that caused the error.	L4_IA_ERROR_LOG_ADDR_L[31:0] ADDR	
IF: Is it a primary error?	L4_IA_AGENT_STATUS_L[30] PROT_ERROR_PRIMARY	=0x1
Read status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[17:16]	
Write 1 to clear status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_FUNC[17:16]	0x3
Write 1 to clear IA status bit.	L4_IA_AGENT_STATUS_L[30] PROT_ERROR_PRIMARY	0x1
ELSE		
Read status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[17:16]	
Write 1 to clear status bits.	CONTROL.CONTROL_SEC_ERR_STATUS_DEBUG[17:16]	0x3

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Table 14-387. Protection Violation Error Identification (continued)

Step	Register/Bit Field/Programming Model	Value
Write 1 to clear IA status bit	L4_IA_AGENT_STATUS_L[31] PROT_ERROR_SECONDARY	0x1
ENDIF		
Write 1 to clear multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	0x1
Write 1 to clear in-band error status.	L4_IA_AGENT_STATUS_L[24] INBAND_ERROR	0x1

14.3.4.1.2.1.3 Subsequence: L4 Interconnect Unsupported Command/Address Hole Error Identification

This procedure describes the identification of unsupported command/address hole error (see Table 14-388).

Table 14-388. Unsupported Command/Address Hole Error Identification

Step	Register/Bit Field/Programming Model	Value
Read multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	
Read initiator ID.	L4_IA_ERROR_LOG_L[11:8] CONNID	
Read command that caused the error.	L4_IA_ERROR_LOG_L[2:0] CMD	
Read address of request that caused the error.	L4_IA_ERROR_LOG_ADDR_L[31:0] ADDR	
Read secondary status.	L4_IA_ERROR_LOG_L[30] SECONDARY	
Write 1 to clear secondary status.	L4_IA_ERROR_LOG_L[30] SECONDARY	0x1
Write 1 to clear multiple errors detection.	L4_IA_ERROR_LOG_L[31] MULTI	0x1
Write 1 to clear inband error status.	L4_IA_AGENT_STATUS_L[24] INBAND_ERROR	0x1

14.3.4.1.2.1.4 Subsequence: L4 Interconnect Reset TA and Module

This procedure describes the reset TA and module (see Table 14-389).

Table 14-389. Reset TA and Module

Step	Register/Bit Field/Programming Model	Value
Reset TA.	L4_TA_AGENT_CONTROL_L[0] OCP_RESET	0x1
Wait until target module clock = 16 cycles.		
Write 0 to clear TA time-out status.	L4_TA_AGENT_CONTROL_L[10:8] REQ_TIMEOUT	0x0
Write 0 to clear TA reset.	L4_TA_AGENT_CONTROL_L[0] OCP_RESET	0x0
Reset the attached module.(1)		

(1) For more information, see the respective module chapter.

14.3.4.1.2.2 L4 Interconnect Time-Out Configuration Mode

14.3.4.1.2.2.1 Main Sequence: L4 Interconnect Time-Out Configuration Mode

This procedure describes the time-out configuration sequence (see Table 14-390).

Table 14-390. Time-Out Configuration

Step	Register/Bit Field/Programming Model	Value
Disable time-out.	L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE	0x0
Clear TA time-out error status.(1)	L4_TA_AGENT_STATUS_L[8] REQ_TIMEOUT	0x1
Set time-out at TA level.(1)	L4_TA_AGENT_CONTROL_L[10:8] REQ_TIMEOUT	xxx

(1) Required for each TA.

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Table 14-390. Time-Out Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Set time-out base.	L4_LA_NETWORK_CONTROL_L[10:8] TIMEOUT_BASE	xxx

14.3.4.1.2.3 L4 Interconnect Firewall Configuration Mode

14.3.4.1.2.3.1 Main Sequence: L4 Interconnect Firewall Configuration Mode

This procedure describes the firewall configuration sequence (see Table 14-391).

Table 14-391. Firewall Configuration

Step	Register/Bit Field/Programming Model	Value
Define the members of protection group k.(1)	L4_AP_PROT_GROUP_MEMBERS_k_L[15:0] CONNID_BIT_VECTOR	xxx
Define the access type of a protection group k.(1)	L4_AP_PROT_GROUP_ROLES_k_L[15:0] ENABLE	xx
Set region affiliation to protection group.(2)	L4_AP_REGION_l_L[22:20] PROT_GROUP_ID	xxx

(1) Required for each protection group.
(2) Required for each region.

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14.3.5 L4 Interconnects Register Manual

Table 14-392 through Table 14-394 list all L4 register blocks for IA, TA, AP, and LA. Each module instance is shown with the module register mapping and bit and bit field definitions.

14.3.5.1 L4 Interconnects Instance Summary

Table 14-392. L4_PER Instance Summary

Module Name	L3_MAIN Base Address	Size
PER_AP	0x4800 0000	2KB
PER_LA	0x4800 0800	512B
PER_IA_IP0	0x4800 1000	128B
UART3_TARG	0x4802 1000	64B
TIMER2_TARG	0x4803 3000	64B
TIMER3_TARG	0x4803 5000	64B
TIMER4_TARG	0x4803 7000	64B
TIMER9_TARG	0x4803 F000	64B
GPIO7_TARG	0x4805 2000	64B
GPIO8_TARG	0x4805 4000	64B
GPIO2_TARG	0x4805 6000	64B
GPIO3_TARG	0x4805 8000	64B
GPIO4_TARG	0x4805 A000	64B
GPIO5_TARG	0x4805 C000	64B
GPIO6_TARG	0x4805 E000	64B
I2C3_TARG	0x4806 1000	64B
UART5_TARG	0x4806 7000	64B
UART6_TARG	0x4806 9000	64B
UART1_TARG	0x4806 B000	64B
UART2_TARG	0x4806 D000	64B
UART4_TARG	0x4806 F000	64B
I2C1_TARG	0x4807 1000	64B
I2C2_TARG	0x4807 3000	64B
ELM_TARG	0x4807 9000	64B
I2C4_TARG	0x4807 B000	64B
I2C5_TARG	0x4807 D000	64B
TIMER10_TARG	0x4808 7000	64B
TIMER11_TARG	0x4808 9000	64B
MCSPI1_TARG	0x4809 9000	64B
MCSPI2_TARG	0x4809 B000	64B
MMC1_TARG	0x4809 D000	64B
MMC3_TARG	0x480A E000	64B
HDQ1W_TARG	0x480B 3000	64B
MMC2_TARG	0x480B 5000	64B
MCSPI3_TARG	0x480B 9000	64B
MCSPI4_TARG	0x480B B000	64B
MMC4_TARG	0x480D 2000	64B
MMC5_TARG	0x480D 6000	64B

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Table 14-393. L4_CFG Instance Summary

Module Name	L3_MAIN Base Address	Size
CFG_AP	0x4A00 0000	2KiB
CFG_LA	0x4A00 0800	64B
CFG_IA_IP0	0x4A00 1000	128B
CTRL_MODULE_CORE_TARG	0x4A00 3000	64B
CM_CORE_AON_TARG	0x4A00 5000	64B
CM_CORE_TARG	0x4A00 A000	64B
USB_OTG_SS_TARG	0x4A04 0000	64B
DMA_SYSTEM_TARG	0x4A05 7000	64B
HSI_TARG	0x4A05 C000	64B
USB_TLL_HS_TARG	0x4A06 3000	64B
USB_HOST_HS_TARG	0x4A06 5000	64B
DSP_TARG	0x4A06 7000	64B
OCP2SCPI1_TARG	0x4A08 8000	64B
OCP2SCPI3_TARG	0x4A09 8000	64B
SMARTREFLEX_MPU_TARG	0x4A0D A000	64B
SMARTREFLEX_MM_TARG	0x4A0D C000	64B
SMARTREFLEX_CORE_TARG	0x4A0D E000	64B
MAILBOX_TARG	0x4A0F 5000	64B
SPINLOCK_TARG	0x4A0F 7000	64B
OCP_WP_NOC_TARG	0x4A10 3000	64B
FDIF_TARG	0x4A10 B000	64B
L4_CFG_TA_TARG	0x4A15 0000	64B
MA_MPU_NTTP_FW_CFG_TARG	0x4A20 B000	64B
EMIF_OCP_FW_CFG_TARG	0x4A20 D000	64B
GPMC_FW_CFG_TARG	0x4A21 1000	64B
OCMC_RAM_FW_CFG_TARG	0x4A21 3000	64B
GPU_FW_CFG_TARG	0x4A21 5000	64B
ISS_FW_CFG_TARG	0x4A21 7000	64B
IPU_FW_CFG_TARG	0x4A21 9000	64B
BB2D_FW_CFG_TARG	0x4A21 B000	64B
DSS_FW_CFG_TARG	0x4A21 D000	64B
IVA_SL2IF_FW_CFG_TARG	0x4A21 F000	64B
IVA_CONFIG_FW_CFG_TARG	0x4A22 1000	64B
DEBUGSS_CT_TBR_FW_CFG_TARG	0x4A22 5000	64B
L3_INSTR_FW_CFG_TARG	0x4A22 7000	64B
ABE_FW_CFG_TARG	0x4A22 9000	64B

Table 14-394. L4_WKUP Instance Summary

Module Name	L3_MAIN Base Address	Size
WKUP_AP	0x4AE0 0000	1KiB
WKUP_LA	0x4AE0 0800	64B
WKUP_IA_IP0	0x4AE0 1000	128B
TA_COUNTER32K_TARG	0x4AE0 5000	64B
TA_PRM_TARG	0x4AE0 8000	64B
TA_SCRM_TARG	0x4AE0 B000	64B
TA_CTRL_MODULE_WKUP_TARG	0x4AE0 D000	64B
TA_GPIO1_TARG	0x4AE1 1000	64B

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Table 14-394. L4_WKUP Instance Summary (continued)

Module Name	L3_MAIN Base Address	Size
TA_WD_TIMER2_TARG	0x4AE1 5000	64B
TA_TIMER1_TARG	0x4AE1 9000	64B
TA_KBD_TARG	0x4AE1 D000	64B
TA_SAR_RAM_TARG	0x4AE2 A000	64B

14.3.5.2 L4 Initiator Agent (L4 IA)

14.3.5.2.1 L4 Initiator Agent (L4 IA) Register Summary

Table 14-395 summarizes the L4 IA register mapping.

Table 14-395. IA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER_IA_IP0 L3 Physical Address	CFG_IA_IP0 L3 Physical Address	WKUP_IA_IP0 L3 Physical Address
L4_IA_COMPONENT_L	R	32	0x0000 0000	0x4800 1000	0x4A00 1000	0x4AE0 1000
L4_IA_COMPONENT_H	R	32	0x0000 0004	0x4800 1004	0x4A00 1004	0x4AE0 1004
L4_IA_CORE_L	R	32	0x0000 0018	0x4800 1018	0x4A00 1018	0x4AE0 1018
L4_IA_CORE_H	R	32	0x0000 001C	0x4800 101C	0x4A00 101C	0x4AE0 101C
L4_IA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4800 1020	0x4A00 1020	0x4AE0 1020
L4_IA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4800 1024	0x4A00 1024	0x4AE0 1024
L4_IA_AGENT_STATUS_L	RW	32	0x0000 0028	0x4800 1028	0x4A00 1028	0x4AE0 1028
L4_IA_AGENT_STATUS_H	R	32	0x0000 002C	0x4800 102C	0x4A00 102C	0x4AE0 102C
L4_IA_ERROR_LOG_L	RW	32	0x0000 0058	0x4800 1058	0x4A00 1058	0x4AE0 1058
L4_IA_ERROR_LOG_H	R	32	0x0000 005C	0x4800 105C	0x4A00 105C	0x4AE0 105C
L4_IA_ERROR_LOG_ADDR_L	R	32	0x0000 0060	0x4800 1060	0x4A00 1060	0x4AE0 1060
L4_IA_ERROR_LOG_ADDR_H	R	32	0x0000 0064	0x4800 1064	0x4A00 1064	0x4AE0 1064

14.3.5.2.2 L4 Initiator Agent (L4 IA) Register Description

Table 14-396 through Table 14-418 describe the L4 IA registers.

Table 14-396. L4_IA_COMPONENT_L

Address Offset	0x0000 0000		
Physical Address	0x4800 1000 0x4A00 1000 0x4AE0 1000	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	COMPONENT register identifies the component to which this register block belongs. The register contains a component code and revision, which are used to identify the hardware of the component. The COMPONENT register is read-only.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code	R	See (1).
15:0	REV	Component revision code	R	See(1).

(1) TI Internal Data

Table 14-397. Register Call Summary for Register L4_IA_COMPONENT_L

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

Table 14-398. L4_IA_COMPONENT_H

Address Offset	0x0000 0004		
Physical Address	0x4800 1004 0x4A00 1004 0x4AE0 1004	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	COMPONENT register identifies the component to which this register block belongs. The register contains a component code and revision, which are used to identify the hardware of the component. The COMPONENT register is read-only.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000

Table 14-399. Register Call Summary for Register L4_IA_COMPONENT_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

Table 14-400. L4_IA_CORE_L

Address Offset	0x0000 0018		
Physical Address	0x4800 1018 0x4A00 1018 0x4AE0 1018	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Provide information about the core initiator		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CODE																REV_CODE															

Bits	Field Name	Description	Type	Reset
31:16	CORE_CODE	Interconnect core code	R	See (1).
15:0	CORE_REV	Component revision code code	R	See(1).

(1) TI Internal Data

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Table 14-401. Register Call Summary for Register L4_IA_CORE_L

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

Table 14-402. L4_IA_CORE_H

Address Offset	0x0000 001C		
Physical Address	0x4800 101C 0x4A00 101C 0x4AE0 101C	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Provide information about the core initiator		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VENDOR_CODE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	VENDOR_CODE	Vendor revision core code	R	See (1).

(1) TI Internal Data

Table 14-403. Register Call Summary for Register L4_IA_CORE_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

Table 14-404. L4_IA_AGENT_CONTROL_L

Address Offset	0x0000 0020		
Physical Address	0x4800 1020 0x4A00 1020 0x4AE0 1020	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Enable error reporting on an initiator interface.The error reporting mechanism is enabled when the INBAND_ERROR_REP bit field is set to 1. The out-of-band OCP MError reporting mechanism is enabled when the MERROR_REP bit field is set to 1.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROT_ERROR_SECONDARY_REP	PROT_ERROR_PRIMARY_REP	RESERVED		INBAND_ERROR_REP	RESERVED		MERROR_REP	RESERVED																							

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Bits	Field Name	Description	Type	Reset
31	PROT_ERROR_SECONDARY_REP	Out-of-band reporting of protection mechanism secondary errors	RW	1
30	PROT_ERROR_PRIMARY_REP	Out-of-band reporting of protection mechanism primary errors	RW	1
29:28	RESERVED	Read returns 0.	R	0x0
27	INBAND_ERROR_REP	Setting this field to 1 reports on in-band errors using the INBAND_ERROR log bit of IA.AGENT_STATUS register.	RW	1
26:25	RESERVED	Read returns 0.	R	0x0
24	MERROR_REP	OCP MError reporting control	R	0
23:0	RESERVED		R	0x0

Table 14-405. Register Call Summary for Register L4_IA_AGENT_CONTROL_L

L4 Interconnects

- Firewall Error Logging in the Control Module: [0]
- L4 Initiator Agent (L4 IA) Register Summary: [1]

Table 14-406. L4_IA_AGENT_CONTROL_H

Address Offset	0x0000 0024		
Physical Address	0x4800 1024 0x4A00 1024 0x4AE0 1024	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Enable error reporting on an initiator interface.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 14-407. Register Call Summary for Register L4_IA_AGENT_CONTROL_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

Table 14-408. L4_IA_AGENT_STATUS_L

Address Offset	0x0000 0028		
Physical Address	0x4800 1028 0x4A00 1028 0x4AE0 1028	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Stores status information for an initiator. The INBAND_ERROR and MERROR fields are read/write and are implemented as log bits.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROT_ERROR_SECONDARY	PROT_ERROR_PRIMARY	RESERVED		INBAND_ERROR	RESERVED		MERROR	RESERVED																							

Bits	Field Name	Description	Type	Reset
31	PROT_ERROR_SECONDARY	0x0: Secondary Protection error not present.0x1: Secondary Protection error present	RW W1toClr	0
30	PROT_ERROR_PRIMARY	0x0: Primary Protection error not present.0x1: Primary Protection error present	RW W1toClr	0
29:28	RESERVED	Read returns 0.	R	0x0
27	INBAND_ERROR	0x0 No In-Band error present.0x1 In-Band error present.	RW W1toClr	0
26:25	RESERVED	Read returns 0.	R	0x0
24	MERROR	Value of the OCP MError signal	R	0
23:0	RESERVED	Read returns 0	R	0X0

Table 14-409. Register Call Summary for Register L4_IA_AGENT_STATUS_L

L4 Interconnects

- IA and TA Error Detection and Logging: [0] [1] [2] [3]
- Operational Modes Configuration: [4] [5] [6] [7] [8]
- L4 Initiator Agent (L4 IA) Register Summary: [9]

Table 14-410. L4_IA_AGENT_STATUS_H

Address Offset	0x0000 002C		
Physical Address	0x4800 102C 0x4A00 102C 0x4AE0 102C	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Stores status information for an initiator.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 14-411. Register Call Summary for Register L4_IA_AGENT_STATUS_H

L4 Interconnects

- L4 Initiator Agent (L4 IA) Register Summary: [0]

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Table 14-412. L4_IA_ERROR_LOG_L

Address Offset	0x0000 0058		
Physical Address	0x4800 1058 0x4A00 1058 0x4AE0 1058	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Log information about error conditions. The CODE field logs any protection violation or address hole errors detected by the initiator subsystem while decoding a request.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MULTI	SECONDARY	RESERVED				CODE		RESERVED								CONNID								RESERVED						CMD	

Bits	Field Name	Description	Type	Reset
31	MULTI	Multiple errors detected	RW W1toClr	0
30	SECONDARY	Indicates whether protection violation was a primary or secondary error	RW W1toClr	0
29:26	RESERVED	Read returns 0.	R	0x0
25:24	CODE	The error code of an initiator request. 0x00: No errors 0x01: Reserved 0x10: Address hole 0x11: Protection violation	RW W1toClr	0x0
23:14	RESERVED	Read returns 0.	R	0x000
13:8	CONNID	ConnID of request causing the error, refer to Table 14-376	R	0x00
7:3	RESERVED	Read returns 0.	R	0x00
2:0	CMD	Command that caused error	R	0x0

Table 14-413. Register Call Summary for Register L4_IA_ERROR_LOG_L

L4 Interconnects

- IA and TA Error Detection and Logging: [0] [1] [2] [3] [4] [5]
- Operational Modes Configuration: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
- L4 Initiator Agent (L4 IA) Register Summary: [16]

Table 14-414. L4_IA_ERROR_LOG_H

Address Offset	0x0000 005C		
Physical Address	0x4800 105C 0x4A00 105C 0x4AE0 105C	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Log information about error conditions.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																REQ_INFO															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Read returns 0.	R	0x0000
15:0	REQ_INFO	MReqInfo bits of request that caused the error REQ_INFO[0] = supervisor, REQ_INFO[1] = Debug	R	0x0000

Table 14-415. Register Call Summary for Register L4_IA_ERROR_LOG_H

L4 Interconnects
- IA and TA Error Detection and Logging: [0]
- L4 Initiator Agent (L4 IA) Register Summary: [1]

Table 14-416. L4_IA_ERROR_LOG_ADDR_L

Address Offset	0x0000 0060		
Physical Address	0x4800 1060 0x4A00 1060 0x4AE0 1060	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Extended error log (address information)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															

Bits	Field Name	Description	Type	Reset
31:0	ADDR	Address of request that caused the error. N is the number MAddr bits.	R	0x0000 0000

Table 14-417. Register Call Summary for Register L4_IA_ERROR_LOG_ADDR_L

L4 Interconnects
- IA and TA Error Detection and Logging: [0]
- Operational Modes Configuration: [1] [2]
- L4 Initiator Agent (L4 IA) Register Summary: [3]

Table 14-418. L4_IA_ERROR_LOG_ADDR_H

Address Offset	0x0000 0064		
Physical Address	0x4800 1064 0x4A00 1064 0x4AE0 1064	**Instance**	PER_IA_IP0 CFG_IA_IP0 WKUP_IA_IP0
Description	Extended error log (address information)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 14-419. Register Call Summary for Register L4_IA_ERROR_LOG_ADDR_H

L4 Interconnects
- L4 Initiator Agent (L4 IA) Register Summary: [0]

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14.3.5.3 L4 Target Agent (L4 TA)

14.3.5.3.1 L4 Target Agent (L4 TA) Register Summary

Table 14-420 through Table 14-449 summarizes the L4 TA mapping of the CFG_TA, PER_TA, and WKUP_TA registers.

Table 14-420. CFG_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_CTRL_MODULE_CORE_TARG L3 Physical Address	CFG_TA_CM_CORE_AON_TARG L3 Physical Address	CFG_TA_CM_CORE_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A00 3000	0x4A00 5000	0x4A00 A000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A00 3004	0x4A00 5004	0x4A00 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A00 3018	0x4A00 5018	0x4A00 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A00 301C	0x4A00 501C	0x4A00 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A00 3020	0x4A00 5020	0x4A00 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A00 3024	0x4A00 5024	0x4A00 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A00 3028	0x4A00 5028	0x4A00 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A00 302C	0x4A00 502C	0x4A00 A02C

Table 14-421. CFG_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_USB_OTG_SS_TARG L3 Physical Address	CFG_TA_DMA_SYSTEM_TARG L3 Physical Address	CFG_TA_HSI_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A04 0000	0x4A05 7000	0x4A05 C000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A04 0004	0x4A05 7004	0x4A05 C004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A04 0018	0x4A05 7018	0x4A05 C018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A04 001C	0x4A05 701C	0x4A05 C01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A04 0020	0x4A05 7020	0x4A05 C020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A04 0024	0x4A05 7024	0x4A05 C024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A04 0028	0x4A05 7028	0x4A05 C028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A04 002C	0x4A05 702C	0x4A05 C02C

Table 14-422. CFG_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_USB_TLL_HS_TARG L3 Physical Address	CFG_TA_USB_HOST_HS_TARG L3 Physical Address	CFG_TA_DSP_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A06 3000	0x4A06 5000	0x4A06 7000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A06 3004	0x4A06 5004	0x4A06 7004

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Table 14-422. CFG_TA Register Mapping Summary 3 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_USB_TLL_HS_TARG L3 Physical Address	CFG_TA_USB_HOST_HS_TARG L3 Physical Address	CFG_TA_DSP_TARG L3 Physical Address
L4_TA_CORE_L	R	32	0x0000 0018	0x4A06 3018	0x4A06 5018	0x4A06 7018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A06 301C	0x4A06 501C	0x4A06 701C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A06 3020	0x4A06 5020	0x4A06 7020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A06 3024	0x4A06 5024	0x4A06 7024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A06 3028	0x4A06 5028	0x4A06 7028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A06 302C	0x4A06 502C	0x4A06 702C

Table 14-423. CFG_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_OCP2SCPI1_TARG L3 Physical Address	CFG_TA_OCP2SCPI3_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A08 8000	0x4A09 8000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A08 8004	0x4A09 8004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A08 8018	0x4A09 8018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A08 801C	0x4A09 801C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A08 8020	0x4A09 8020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A08 8024	0x4A09 8024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A08 8028	0x4A09 8028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A08 802C	0x4A09 802C

Table 14-424. CFG_TA Register Mapping Summary 5

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_SMARTREFLEX_MPU_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A0D A000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A0D A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A0D A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A0D A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A0D A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A0D A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A0D A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A0D A02C

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Table 14-425. CFG_TA Register Mapping Summary 6

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_SMARTREFLEX_MM_TARG L3 Physical Address	CFG_TA_SMARTREFLEX_CORE_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A0D C000	0x4A0D E000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A0D C004	0x4A0D E004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A0D C018	0x4A0D E018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A0D C01C	0x4A0D E01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A0D C020	0x4A0D E020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A0D C024	0x4A0D E024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A0D C028	0x4A0D E028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A0D C02C	0x4A0D E02C

Table 14-426. CFG_TA Register Mapping Summary 7

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_MAILBOX_TARG L3 Physical Address	CFG_TA_SPINLOCK_TARG L3 Physical Address	CFG_TA_OCP_WP_NOC_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A0F 5000	0x4A0F 7000	0x4A10 3000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A0F 5004	0x4A0F 7004	0x4A10 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A0F 5018	0x4A0F 7018	0x4A10 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A0F 501C	0x4A0F 701C	0x4A10 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A0F 5020	0x4A0F 7020	0x4A10 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A0F 5024	0x4A0F 7024	0x4A10 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A0F 5028	0x4A0F 7028	0x4A10 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A0F 502C	0x4A0F 702C	0x4A10 302C

Table 14-427. CFG_TA Register Mapping Summary 8

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_FDIF_TARG L3 Physical Address	CFG_L4_CFG_TA_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A10 B000	0x4A15 0000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A10 B004	0x4A15 0004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A10 B018	0x4A15 0018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A10 B01C	0x4A15 001C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A10 B020	0x4A15 0020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A10 B024	0x4A15 0024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A10 B028	0x4A15 0028

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Table 14-427. CFG_TA Register Mapping Summary 8 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_FDIF_TARG L3 Physical Address	CFG_L4_CFG_TA_TARG L3 Physical Address
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A10 B02C	0x4A15 002C

Table 14-428. CFG_TA Register Mapping Summary 10

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_MA_MPU_NTTP_FW_CFG_TARG L3 Physical Address	CFG_TA_EMIF_OCP_FW_CFG_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A20 B000	0x4A20 D000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A20 B004	0x4A20 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A20 B018	0x4A20 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A20 B01C	0x4A20 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A20 B020	0x4A20 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A20 B024	0x4A20 D024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A20 B028	0x4A20 D028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A20 B02C	0x4A20 D02C

Table 14-429. CFG_TA Register Mapping Summary 11

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_BB2D_FW_CFG_TARG L3 Physical Address	CFG_TA_GPMC_FW_CFG_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A21 B000	0x4A21 1000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A21 B004	0x4A21 1004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A21 B018	0x4A21 1018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A21 B01C	0x4A21 101C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A21 B020	0x4A21 1020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A21 B024	0x4A21 1024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A21 B028	0x4A21 1028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A21 B02C	0x4A21 102C

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Table 14-430. CFG_TA Register Mapping Summary 12

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_OCMC_RAM_FW_CFG_TARG L3 Physical Address	CFG_TA_GPU_FW_CFG_TARG L3 Physical Address	CFG_TA_ISS_FW_CFG_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A21 3000	0x4A21 5000	0x4A21 7000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A21 3004	0x4A21 5004	0x4A21 7004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A21 3018	0x4A21 5018	0x4A21 7018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A21 301C	0x4A21 501C	0x4A21 701C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A21 3020	0x4A21 5020	0x4A21 7020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A21 3024	0x4A21 5024	0x4A21 7024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A21 3028	0x4A21 5028	0x4A21 7028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A21 302C	0x4A21 502C	0x4A21 702C

Table 14-431. CFG_TA Register Mapping Summary 13

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_IPU_FW_CFG_TARG L3 Physical Address	CFG_TA_DSS_FW_CFG_TARG L3 Physical Address	CFG_TA_IVA_SL2IF_FW_CFG_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A21 9000	0x4A21 D000	0x4A21 F000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A21 9004	0x4A21 D004	0x4A21 F004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A21 9018	0x4A21 D018	0x4A21 F018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A21 901C	0x4A21 D01C	0x4A21 F01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A21 9020	0x4A21 D020	0x4A21 F020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A21 9024	0x4A21 D024	0x4A21 F024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A21 9028	0x4A21 D028	0x4A21 F028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A21 902C	0x4A21 D02C	0x4A21 F02C

Table 14-432. CFG_TA Register Mapping Summary 14

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_IVA_CONFIG_FW_CFG_TARG L3 Physical Address	CFG_TA_DEBUGSS_CT_TBR_FW_CFG_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A22 1000	0x4A22 5000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A22 1004	0x4A22 5004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A22 1018	0x4A22 5018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A22 101C	0x4A22 501C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A22 1020	0x4A22 5020

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Table 14-432. CFG_TA Register Mapping Summary 14 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_IVA_CONFIG_FW_CFG_TARG L3 Physical Address	CFG_TA_DEBUGSS_CT_TBR_FW_CFG_TARG L3 Physical Address
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A22 1024	0x4A22 5024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A22 1028	0x4A22 5028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A22 102C	0x4A22 502C

Table 14-433. CFG_TA Register Mapping Summary 15

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_L3_INSTR_FW_CFG_TARG L3 Physical Address	CFG_TA_ABE_FW_CFG_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A22 7000	0x4A22 9000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A22 7004	0x4A22 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A22 7018	0x4A22 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A22 701C	0x4A22 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A22 7020	0x4A22 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A22 7024	0x4A22 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A22 7028	0x4A22 9028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A22 702C	0x4A22 902C

Table 14-434. PER_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_UART3_TARG L3 Physical Address	PER_TA_TIMER2_TARG L3 Physical Address	PER_TA_TIMER3_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4802 1000	0x4803 3000	0x4803 5000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4802 1004	0x4803 3004	0x4803 5004
L4_TA_CORE_L	R	32	0x0000 0018	0x4802 1018	0x4803 3018	0x4803 5018
L4_TA_CORE_H	R	32	0x0000 001C	0x4802 101C	0x4803 301C	0x4803 501C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4802 1020	0x4803 3020	0x4803 5020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4802 1024	0x4803 3024	0x4803 5024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4802 1028	0x4803 3028	0x4803 5028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4802 102C	0x4803 302C	0x4803 502C

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Table 14-435. PER_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_TIMER4_TARG L3 Physical Address	PER_TA_TIMER9_TARG L3 Physical Address	PER_TA_GPIO7_TARG L3 Physical Address	PER_TA_GPIO8_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4803 7000	0x4803 F000	0x4805 2000	0x4805 4000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4803 7004	0x4803 F004	0x4805 2004	0x4805 4004
L4_TA_CORE_L	R	32	0x0000 0018	0x4803 7018	0x4803 F018	0x4805 2018	0x4805 4018
L4_TA_CORE_H	R	32	0x0000 001C	0x4803 701C	0x4803 F01C	0x4805 201C	0x4805 401C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4803 7020	0x4803 F020	0x4805 2020	0x4805 4020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4803 7024	0x4803 F024	0x4805 2024	0x4805 4024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4803 7028	0x4803 F028	0x4805 2028	0x4805 4028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4803 702C	0x4803 F02C	0x4805 202C	0x4805 402C

Table 14-436. PER_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPIO2_TARG L3 Physical Address	PER_TA_GPIO3_TARG L3 Physical Address	PER_TA_GPIO4_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4805 6000	0x4805 8000	0x4805 A000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4805 6004	0x4805 8004	0x4805 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4805 6018	0x4805 8018	0x4805 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4805 601C	0x4805 801C	0x4805 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4805 6020	0x4805 8020	0x4805 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4805 6024	0x4805 8024	0x4805 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4805 6028	0x4805 8028	0x4805 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4805 602C	0x4805 802C	0x4805 A02C

Table 14-437. PER_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPIO5_TARG L3 Physical Address	PER_TA_GPIO6_TARG L3 Physical Address	PER_TA_I2C3_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4805 C000	0x4805 E000	0x4806 1000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4805 C004	0x4805 E004	0x4806 1004
L4_TA_CORE_L	R	32	0x0000 0018	0x4805 C018	0x4805 E018	0x4806 1018
L4_TA_CORE_H	R	32	0x0000 001C	0x4805 C01C	0x4805 E01C	0x4806 101C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4805 C020	0x4805 E020	0x4806 1020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4805 C024	0x4805 E024	0x4806 1024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4805 C028	0x4805 E028	0x4806 1028

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Table 14-437. PER_TA Register Mapping Summary 4 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPIO5_TARG L3 Physical Address	PER_TA_GPIO6_TARG L3 Physical Address	PER_TA_I2C3_TARG L3 Physical Address
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4805 C02C	0x4805 E02C	0x4806 102C

Table 14-438. PER_TA Register Mapping Summary 5

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_UART5_TARG L3 Physical Address	PER_TA_UART6_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4806 7000	0x4806 9000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4806 7004	0x4806 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x4806 7018	0x4806 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x4806 701C	0x4806 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4806 7020	0x4806 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4806 7024	0x4806 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4806 7028	0x4806 9028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4806 702C	0x4806 902C

Table 14-439. PER_TA Register Mapping Summary 6

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_UART1_TARG L3 Physical Address	PER_TA_UART2_TARG L3 Physical Address	PER_TA_UART4_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4806 B000	0x4806 D000	0x4806 F000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4806 B004	0x4806 D004	0x4806 F004
L4_TA_CORE_L	R	32	0x0000 0018	0x4806 B018	0x4806 D018	0x4806 F018
L4_TA_CORE_H	R	32	0x0000 001C	0x4806 B01C	0x4806 D01C	0x4806 F01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4806 B020	0x4806 D020	0x4806 F020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4806 B024	0x4806 D024	0x4806 F024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4806 B028	0x4806 D028	0x4806 F028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4806 B02C	0x4806 D02C	0x4806 F02C

Table 14-440. PER_TA Register Mapping Summary 7

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_I2C1_TARG L3 Physical Address	PER_TA_I2C2_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4807 1000	0x4807 3000

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Table 14-440. PER_TA Register Mapping Summary 7 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_I2C1_TARG L3 Physical Address	PER_TA_I2C2_TARG L3 Physical Address
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4807 1004	0x4807 3004
L4_TA_CORE_L	R	32	0x0000 0018	0x4807 1018	0x4807 3018
L4_TA_CORE_H	R	32	0x0000 001C	0x4807 101C	0x4807 301C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4807 1020	0x4807 3020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4807 1024	0x4807 3024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4807 1028	0x4807 3028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4807 102C	0x4807 302C

Table 14-441. PER_TA Register Mapping Summary 8

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_ELM_TARG L3 Physical Address	PER_TA_I2C4_TARG L3 Physical Address	PER_TA_I2C5_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4807 9000	0x4807 B000	0x4807 D000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4807 9004	0x4807 B004	0x4807 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4807 9018	0x4807 B018	0x4807 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4807 901C	0x4807 B01C	0x4807 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4807 9020	0x4807 B020	0x4807 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4807 9024	0x4807 B024	0x4807 D024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4807 9028	0x4807 B028	0x4807 D028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4807 902C	0x4807 B02C	0x4807 D02C

Table 14-442. PER_TA Register Mapping Summary 9

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPTIMER10_TARG L3 Physical Address	PER_TA_GPTIMER11_TARG L3 Physical Address	PER_TA_MCSPI1_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4808 7000	0x4808 9000	0x4809 9000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4808 7004	0x4808 9004	0x4809 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x4808 7018	0x4808 9018	0x4809 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x4808 701C	0x4808 901C	0x4809 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4808 7020	0x4808 9020	0x4809 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4808 7024	0x4808 9024	0x4809 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4808 7028	0x4808 9028	0x4809 9028

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Table 14-442. PER_TA Register Mapping Summary 9 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_GPTIMER10_TARG L3 Physical Address	PER_TA_GPTIMER11_TARG L3 Physical Address	PER_TA_MCSPI1_TARG L3 Physical Address
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4808 702C	0x4808 902C	0x4809 902C

Table 14-443. PER_TA Register Mapping Summary 10

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_MCSPI2_TARG L3 Physical Address	PER_TA_MMC1_TARG L3 Physical Address	PER_TA_MMC3_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4809 B000	0x4809 D000	0x480A E000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4809 B004	0x4809 D004	0x480A E004
L4_TA_CORE_L	R	32	0x0000 0018	0x4809 B018	0x4809 D018	0x480A E018
L4_TA_CORE_H	R	32	0x0000 001C	0x4809 B01C	0x4809 D01C	0x480A E01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4809 B020	0x4809 D020	0x480A E020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4809 B024	0x4809 D024	0x480A E024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4809 B028	0x4809 D028	0x480A E028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4809 B02C	0x4809 D02C	0x480A E02C

Table 14-444. PER_TA Register Mapping Summary 11

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_HDQ1W_TARG L3 Physical Address	PER_TA_MMC2_TARG L3 Physical Address	PER_TA_MCSPI3_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x480B 3000	0x480B 5000	0x480B 9000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x480B 3004	0x480B 5004	0x480B 9004
L4_TA_CORE_L	R	32	0x0000 0018	0x480B 3018	0x480B 5018	0x480B 9018
L4_TA_CORE_H	R	32	0x0000 001C	0x480B 301C	0x480B 501C	0x480B 901C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x480B 3020	0x480B 5020	0x480B 9020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x480B 3024	0x480B 5024	0x480B 9024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x480B 3028	0x480B 5028	0x480B 9028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x480B 302C	0x480B 502C	0x480B 902C

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Table 14-445. PER_TA Register Mapping Summary 12

Register Name	Type	Register Width (Bits)	Address Offset	PER_TA_MCSPI4_TARG L3 Physical Address	PER_TA_MMC4_TARG L3 Physical Address	PER_TA_MMC5_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x480B B000	0x480D 2000	0x480D 6000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x480B B004	0x480D 2004	0x480D 6004
L4_TA_CORE_L	R	32	0x0000 0018	0x480B B018	0x480D 2018	0x480D 6018
L4_TA_CORE_H	R	32	0x0000 001C	0x480B B01C	0x480D 201C	0x480D 601C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x480B B020	0x480D 2020	0x480D 6020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x480B B024	0x480D 2024	0x480D 6024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x480B B028	0x480D 2028	0x480D 6028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x480B B02C	0x480D 202C	0x480D 602C

Table 14-446. WKUP_TA Register Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_COUNTER32K_TARG L3 Physical Address	WKUP_TA_PRM_TARG L3 Physical Address	WKUP_TA_SCRM_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4AE0 5000	0x4AE0 8000	0x4AE0 B000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4AE0 5004	0x4AE0 8004	0x4AE0 B004
L4_TA_CORE_L	R	32	0x0000 0018	0x4AE0 5018	0x4AE0 8018	0x4AE0 B018
L4_TA_CORE_H	R	32	0x0000 001C	0x4AE0 501C	0x4AE0 801C	0x4AE0 B01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4AE0 5020	0x4AE0 8020	0x4AE0 B020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4AE0 5024	0x4AE0 8024	0x4AE0 B024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4AE0 5028	0x4AE0 8028	0x4AE0 B028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4AE0 502C	0x4AE0 802C	0x4AE0 B02C

Table 14-447. WKUP_TA Register Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_CTRL_MODULE_WKUP_TARG L3 Physical Address	WKUP_TA_GPIO1_TARG L3 Physical Address	WKUP_TA_WD_TIMER2_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4AE0 D000	0x4AE1 1000	0x4AE1 5000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4AE0 D004	0x4AE1 1004	0x4AE1 5004
L4_TA_CORE_L	R	32	0x0000 0018	0x4AE0 D018	0x4AE1 1018	0x4AE1 5018
L4_TA_CORE_H	R	32	0x0000 001C	0x4AE0 D01C	0x4AE1 101C	0x4AE1 501C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4AE0 D020	0x4AE1 1020	0x4AE1 5020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4AE0 D024	0x4AE1 1024	0x4AE1 5024

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Table 14-447. WKUP_TA Register Mapping Summary 2 (continued)

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_CTRL_MODULE_WKUP_TARG L3 Physical Address	WKUP_TA_GPIO1_TARG L3 Physical Address	WKUP_TA_WD_TIMER2_TARG L3 Physical Address
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4AE0 D028	0x4AE1 1028	0x4AE1 5028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4AE0 D02C	0x4AE1 102C	0x4AE1 502C

Table 14-448. WKUP_TA Register Mapping Summary 3

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_TIMER1_TARG L3 Physical Address	WKUP_TA_KBD_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4AE1 9000	0x4AE1 D000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4AE1 9004	0x4AE1 D004
L4_TA_CORE_L	R	32	0x0000 0018	0x4AE1 9018	0x4AE1 D018
L4_TA_CORE_H	R	32	0x0000 001C	0x4AE1 901C	0x4AE1 D01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4AE1 9020	0x4AE1 D020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4AE1 9024	0x4AE1 D024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4AE1 9028	0x4AE1 D028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4AE1 902C	0x4AE1 D02C

Table 14-449. WKUP_TA Register Mapping Summary 4

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_TA_SAR_RAM_TARG L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4AE2 A000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4AE2 A004
L4_TA_CORE_L	R	32	0x0000 0018	0x4AE2 A018
L4_TA_CORE_H	R	32	0x0000 001C	0x4AE2 A01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4AE2 A020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4AE2 A024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4AE2 A028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4AE2 A02C

14.3.5.3.2 L4 Target Agent (L4 TA) Register Description

Table 14-450 through Table 14-464 describe the L4 TA registers.

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Table 14-450. L4_TA_COMPONENT_H

Address Offset	0x0000 0000
Physical Address	See Table 14-420 to Table 14-433.
Description	Contains a component code and revision.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 000

Table 14-451. Register Call Summary for Register L4_TA_COMPONENT_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]

Table 14-452. L4_TA_COMPONENT_L

Address Offset	0x0000 0004
Physical Address	See Table 14-420 to Table 14-433.
Description	Contains a component code and revision.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code.	R	See (1).
15:0	REV	Component revision code.	R	See (1).

(1) TI Internal Data

Table 14-453. Register Call Summary for Register L4_TA_COMPONENT_L

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]

Table 14-454. L4_TA_CORE_L

Address Offset	0x0000 0018
Physical Address	See Table 14-420 to Table 14-433.
Description	Contains a component code and revision.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CODE																REV_CODE															

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Bits	Field Name	Description	Type	Reset
31:16	CORE_CODE	Interconnect core code	R	See (1).
15:0	CORE_REV	Component revision code code	R	See (1).

(1) TI Internal Data

Table 14-455. Register Call Summary for Register L4_TA_CORE_L

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]

Table 14-456. L4_TA_CORE_H

Address Offset	0x0000 001C
Physical Address	See Table 14-420 to Table 14-433.
Description	Contains a component code and revision.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VENDOR_CODE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	VENDOR_CODE	Vendor revision core code	R	See (1).

(1) TI Internal Data

Table 14-457. Register Call Summary for Register L4_TA_CORE_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]

Table 14-458. L4_TA_AGENT_CONTROL_L

Address Offset	0x0000 0020
Physical Address	See Table 14-420 to Table 14-433.
Description	Enable error reporting
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SERROR_REP	RESERVED													REQ_TIMEOUT			RESERVED							OCP_RESET

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24	SERROR_REP	Enable logging of error	R	0x0
23:11	RESERVED	Read returns 0.	UNDEFINED_TYPE_STRING	

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Bits	Field Name	Description	Type	Reset
10:8	REQ_TIMEOUT	Time-out Bound. Values are: 0 - No time-out 1 - 1x base cycles. 2 - 4x base cycles. 3 - 16x base cycles. 4 - 64x base cycles.	RW	0x2
7:1	RESERVED	Read returns 0.	R	0x00
0	OCP_RESET	The OCP_RESET field controls the OCP reset signal to the attached core. Setting this bit clears any pending transfers and resets the OCP interface. The bit must be cleared to deassert the OCP reset signal. When the software reset feature is available on a target agent, the target agent OCP must also have a reset signal directed to the target core.	RW	0

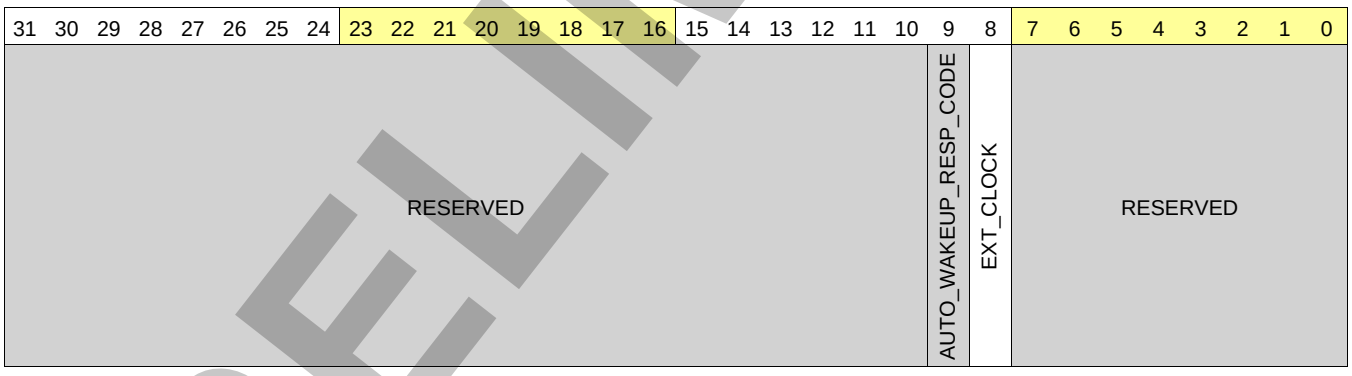
Table 14-459. Register Call Summary for Register L4_TA_AGENT_CONTROL_L

L4 Interconnects

- Time-Out: [0] [1] [2] [3] [4]
- Error Recovery: [5] [6]
- Operational Modes Configuration: [7] [8] [9] [10]
- L4 Target Agent (L4 TA) Register Summary: [11] [12] [13] [14] [15] [17] [18] [19] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42]

Table 14-460. L4_TA_AGENT_CONTROL_H

Address Offset	0x0000 0024
Physical Address	See Table 14-420 to Table 14-433.
Description	Enable clock power management
Type	R



Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Read returns 0.	R	0x000000
9	AUTO_WAKEUP_RESP_CODE		R	0
8	EXT_CLOCK	When set to 1, the ext_clk_off_i signal on a target agent indicates when the target agent should shut off.	R	0
7:0	RESERVED	Read returns 0.	R	0x00

Table 14-461. Register Call Summary for Register L4_TA_AGENT_CONTROL_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]

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Table 14-462. L4_TA_AGENT_STATUS_L

Address Offset	0x0000 0028
Physical Address	See Table 14-420 to Table 14-433.
Description	Error reporting
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SERROR	RESERVED															REQ_TIMEOUT	RESERVED							0CP_RESET

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24	SERROR	Value of OCP SError signal	R	0
23:9	RESERVED	Read returns 0.	R	0x0000
8	REQ_TIMEOUT	Time-out status: 0x0: No request time-out 0x1: A request time-out has occurred	R 1toCLR	0
7:1	RESERVED	Read returns 0.	R	0x00
0	OCP_RESET	L3 Reset	R	0

Table 14-463. Register Call Summary for Register L4_TA_AGENT_STATUS_L

L4 Interconnects

- Time-Out: [0] [1]
- Error Recovery: [2]
- Operational Modes Configuration: [3]
- L4 Target Agent (L4 TA) Register Summary: [4] [5] [6] [7] [8] [10] [11] [12] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35]

Table 14-464. L4_TA_AGENT_STATUS_H

Address Offset	0x0000 002C
Physical Address	See Table 14-420 to Table 14-433.
Description	Error reporting
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 000

Table 14-465. Register Call Summary for Register L4_TA_AGENT_STATUS_H

L4 Interconnects

- L4 Target Agent (L4 TA) Register Summary: [0] [1] [2] [3] [4] [6] [7] [8] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]

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14.3.5.4 L4 Link Agent (L4 LA)

14.3.5.4.1 L4 Link Agent (L4 LA) Register Summary

Table 14-466 summarizes the L4 LA register mapping.

Table 14-466. LA Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER_LA L3 Physical Address	CFG_LA L3 Physical Address	WKUP_LA L3 Physical Address
L4_LA_COMPONENT_L	R	32	0x0000 0000	0x4800 0800	0x4A00 0800	0x4AE0 0800
L4_LA_COMPONENT_H	R	32	0x0000 0004	0x4800 0804	0x4A00 0804	0x4AE0 0804
L4_LA_NETWORK_L	R	32	0x0000 0010	0x4800 0810	0x4A00 0810	0x4AE0 0810
L4_LA_NETWORK_H	R	32	0x0000 0014	0x4800 0814	0x4A00 0814	0x4AE0 0814
L4_LA_INITIATOR_INFO_L	R	32	0x0000 0018	0x4800 0818	0x4A00 0818	0x4AE0 0818
L4_LA_INITIATOR_INFO_H	R	32	0x0000 001C	0x4800 081C	0x4A00 081C	0x4AE0 081C
L4_LA_NETWORK_CONTROL_L	RW	32	0x0000 0020	0x4800 0820	0x4A00 0820	0x4AE0 0820
L4_LA_NETWORK_CONTROL_H	RW	32	0x0000 0024	0x4800 0824	0x4A00 0824	0x4AE0 0824
L4_LA_FLAG_MASK_j_L[(1)]	RW	32	0x0000 0100 + (0x20*j)	0x4800 0900 + (0x20*j)	N/A	N/A
L4_LA_FLAG_MASK_j_H[(1)]	RW	32	0x0000 0104 + (0x20*j)	0x4800 0904 + (0x20*j)	N/A	N/A
L4_LA_FLAG_STATUS_j_L[(1)]	R	32	0x0000 0110 + (0x20*j)	0x4800 0910 + (0x20*j)	N/A	N/A
L4_LA_FLAG_STATUS_j_H[(1)]	R	32	0x0000 0114 + (0x20*j)	0x4800 0914 + (0x20*j)	N/A	N/A

(1) j = 0 to 1

14.3.5.4.2 L4 Link Agent (L4 LA) Register Description

Table 14-467 through Table 14-483 describe the L4 LA registers.

Table 14-467. L4_LA_COMPONENT_L

Address Offset	0x0000 0000		
Physical Address	0x4800 0800 0x4A00 0800 0x4AE0 0800	**Instance**	PER_LA CFG_LA WKUP_LA
Description	Contain a component code and revision, which are used to identify the hardware of the component.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code.	R	See (1).
15:0	REV	Component revision code.	R	See (1).

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Table 14-468. Register Call Summary for Register L4_LA_COMPONENT_L

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-469. L4_LA_COMPONENT_H

Address Offset	0x0000 0004		
Physical Address	0x4800 0804 0x4A00 0804 0x4AE0 0804	**Instance**	PER_LA CFG_LA WKUP_LA
Description	Contain a component code and revision, which are used to identify the hardware of the component.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0.	R	0x0000 0000

Table 14-470. Register Call Summary for Register L4_LA_COMPONENT_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-471. L4_LA_NETWORK_L

Address Offset	0x0000 0010		
Physical Address	0x4800 0810 0x4A00 0810 0x4AE0 0810	**Instance**	PER_LA CFG_LA WKUP_LA
Description	Identify the interconnect		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 0000

Table 14-472. Register Call Summary for Register L4_LA_NETWORK_L

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-473. L4_LA_NETWORK_H

Address Offset	0x0000 0014		
Physical Address	0x4800 0814 0x4A00 0814 0x4AE0 0814	**Instance**	PER_LA CFG_LA WKUP_LA
Description	Identify the interconnect		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															

Bits	Field Name	Description	Type	Reset
31:0	ID	The ID field uniquely identifies this interconnect.	R	0x00000000

Table 14-474. Register Call Summary for Register L4_LA_NETWORK_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-475. L4_LA_INITIATOR_INFO_L

Address Offset	0x0000 0018		
Physical Address	0x4800 0818 0x4A00 0818 0x4AE0 0818	**Instance**	PER_LA CFG_LA WKUP_LA
Description	Contain initiator subsystem information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PROT_GROUPS				NUMBER_REGIONS								RESERVED												SEGMENTS			

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Read returns 0.	R	0x0
27:24	PROT_GROUPS	Number of protection group of in the current L4 0x0: No protection group 0x1: 1 protection group 0x2: 2 protection groups .... 0x8: 8 protection groups 0x9 to 0xF: Reserved	R	see Table 14-477
23:16	NUMBER_REGIONS	Number of regions in the current L4 0x0: Reserved 0x1: 1 region 0x2: 2 regions .... Max regions +1 to 0xFF: Reserved, maximum regions is listed in Table 14-477	R	see Table 14-477
15:4	RESERVED	Read returns 0.	R	0x000
3:0	SEGMENTS	Number of segments in the current L4 0x0: Reserved 0x1: 1 segment 0x2: 2 segments .... 0x8: 8 segments	R	see Table 14-477

Table 14-476. Register Call Summary for Register L4_LA_INITIATOR_INFO_L

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

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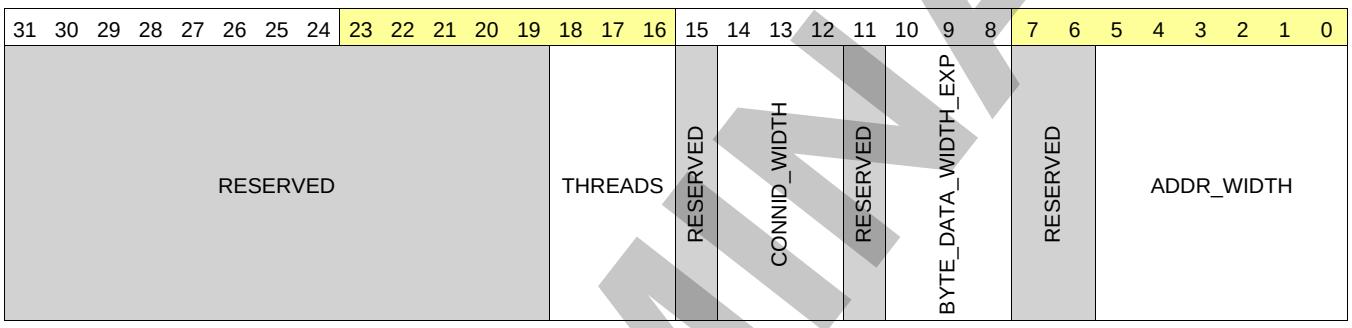
Table 14-477. Reset value for L4_LA_INITIATOR_INFO_L

Field Name	L4 PER	L4 CFG	L4 WKUP
PROT_GROUPS	0x8	0x8	0x8
NUMBER_REGIONS	0x66	0x72	0x1E
SEGMENTS	0x2	0x7	0x3

Table 14-478. L4_LA_INITIATOR_INFO_H

Address Offset	0x0000 001C		
Physical Address	0x4800 081C 0x4A00 081C 0x4AE0 081C	**Instance**	PER_LA CFG_LA WKUP_LA
Description	Contain initiator subsystem information.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:19	RESERVED	Read returns 0.	R	0x0000
18:16	THREADS	The THREADS field specifies the number of initiator threads connected to the interconnect. The field contains read-only configuration information for the initiator subsystem.	R	see Table 14-480
15	RESERVED	Read returns 0.	R	0
14:12	CONNID_WIDTH	The initiator subsystem ConnID width. The CONNID_WIDTH field contains read-only configuration information for the initiator subsystem.	R	see Table 14-480
11	RESERVED	Read returns 0.	R	0
10:8	BYTE_DATA_WIDTH_EXP	This field specifies the initiator subsystem data width.The BYTE_DATA_WIDTH_EXP field contains read-only configuration information for the initiator subsystem. 0x1: 16-bit data width is specified 0x2: 32-bit data width is specified	R	see Table 14-480
7:6	RESERVED	Read returns 0.	R	0x0
5:0	ADDR_WIDTH	This field specifies the initiator subsystem address width. The ADDR_WIDTH field contains read-only configuration information for the initiator subsystem.	R	see Table 14-480

Table 14-479. Register Call Summary for Register L4_LA_INITIATOR_INFO_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-480. Reset value for L4_LA_INITIATOR_INFO_H

Field Name	L4 PER	L4 CFG	L4 WKUP
THREADS	0x4	0x1	0x1
CONNID_WIDTH	0x4	0x4	0x4

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Table 14-480. Reset value for L4_LA_INITIATOR_INFO_H (continued)

Field Name	L4 PER	L4 CFG	L4 WKUP
BYTE_DATA_WIDTH_EXP	0x2	0x2	0x2
ADDR_WIDTH	0x18	0x18	0x15

Table 14-481. L4_LA_NETWORK_CONTROL_L

Address Offset	0x0000 0020		
Physical Address	0x4800 0820 0x4A00 0820 0x4AE0 0820	**Instance**	PER_LA CFG_LA WKUP_LA
Description	Control interconnect minimum timeout values.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						TIMEOUT_BASE		RESERVED							

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Read returns 0.	R	0x000000
10:8	TIMEOUT_BASE	The TIMEOUT_BASE field indicates the time-out period (that is, base cycles) for the highest frequency time-base signal sent from the L4 initiator subsystem to all target agents that have time-out enabled. Values for the field are: 0 - Time-out disabled 1 - L4 interconnect clock cycles divided by 64 2 - L4 interconnect clock cycles divided by 256 3 - L4 interconnect clock cycles divided by 1024 4 - L4 interconnect clock cycles divided by 4096	RW	0x4
7:0	RESERVED	Read returns 0.	R	0x00

Table 14-482. Register Call Summary for Register L4_LA_NETWORK_CONTROL_L

L4 Interconnects

- Time-Out: [0] [1] [2]
- Operational Modes Configuration: [3] [4]
- L4 Link Agent (L4 LA) Register Summary: [5]

Table 14-483. L4_LA_NETWORK_CONTROL_H

Address Offset	0x0000 0024		
Physical Address	0x4800 0824 0x4A00 0824 0x4AE0 0824	**Instance**	PER_LA CFG_LA WKUP_LA
Description	Control interconnect global power control		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLOCK_GATE_DISABLE	RESERVED			THREAD0_PRI	RESERVED											EXT_CLOCK	RESERVED							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Read returns 0.	R	0x00
24	CLOCK_GATE_DISABLE	When set to 1 this field disables all clock gating.	RW	0
23:21	RESERVED	Read returns 0.	R	0x0
20	THREAD0_PRI	Sets thread priority. If the field is set to 0, the default, all initiator threads are treated the same. Setting the THREAD0_PRI field to 1 assigns a higher arbitration priority to thread 0 of the first initiator OCP interface. To avoid starvation, arbitration is imposed by the initiator subsystem. When multiple requests from different initiator threads are dispatched to targets simultaneously, the oldest request is dispatched first. If thread 0 is assigned a higher priority, a request on thread 0 always wins arbitration. Assigning thread 0 of the first initiator OCP the highest priority on a request or response can result in the starvation of other threads.	R	1
19:9	RESERVED	Read returns 0.	R	0x000
8	EXT_CLOCK	When set to 1, the ext_clk_off_i signal on the initiator subsystem instructs the entire L4 to shut off.	R	1
7:0	RESERVED	Read returns 0.	R	0x00

Table 14-484. Register Call Summary for Register L4_LA_NETWORK_CONTROL_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-485. L4_LA_FLAG_MASK_j_L

Address Offset	0x0000 0100 + (0x20*j)		
Physical Address	0x4800 0900 + (0x20*j)	**Instance**	PER_LA
Description	Mask of composite sideband flag(0)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MASK			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Read returns 0	R	0x0000 0000
3:0	MASK	Number of input sideband signals	RW	0xF

Table 14-486. Register Call Summary for Register L4_LA_FLAG_MASK_j_L

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

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Table 14-487. L4_LA_FLAG_MASK_j_H

Address Offset	0x0000 0104 + (0x20*j)		
Physical Address	0x4800 0904 + (0x20*j)	**Instance**	PER_LA
Description	Status of composite sideband flag(0)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 0000

Table 14-488. Register Call Summary for Register L4_LA_FLAG_MASK_j_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-489. L4_LA_FLAG_STATUS_j_L

Address Offset	0x0000 0110 + (0x20*j)		
Physical Address	0x4800 0910 + (0x20*j)	**Instance**	PER_LA
Description	Mask of composite sideband flag(1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												STATUS			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Read returns 0	R	0x0000 0000
3:0	STATUS	Status of input sideband signals	RW	0x0

Table 14-490. Register Call Summary for Register L4_LA_FLAG_STATUS_j_L

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

Table 14-491. L4_LA_FLAG_STATUS_j_H

Address Offset	0x0000 0114 + (0x20*j)		
Physical Address	0x4800 0914 + (0x20*j)	**Instance**	PER_LA
Description	Status of composite sideband flag(1)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x000 0000 0000 0000

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Table 14-492. Register Call Summary for Register L4_LA_FLAG_STATUS_j_H

L4 Interconnects

- L4 Link Agent (L4 LA) Register Summary: [0]

14.3.5.5 L4 Address Protection (L4 AP)

14.3.5.5.1 L4 Address Protection (L4 AP) Register Summary

Table 14-493 summarizes the L4 AP register mapping.

Table 14-493. L4 AP Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	PER_AP Physical Address	CFG_AP Physical Address	WKUP_AP Physical Address
L4_AP_COMPONENT_L	R	32	0x0000 0000	0x4800 0 000	0x4A00 0 000	0x4AE0 0 000
L4_AP_COMPONENT_H	R	32	0x0000 0004	0x4800 0004	0x4A00 0004	0x4AE0 0004
L4_AP_SEGMENT_i_L (1)	RW	32	0x0000 0100 + (0x08*i)	0x4800 0100 + (0x08*i)	0x4A00 0100 + (0x08*i)	0x4AE0 0100 + (0x08*i)
L4_AP_SEGMENT_i_H (1)	RW	32	0x0000 0104 + (0x08*i)	0x4800 0104 + (0x08*i)	0x4A00 0104 + (0x08*i)	0x4AE0 0104 + (0x08*i)
L4_AP_PROT_GROUP_MEMBERS_k_L (2)	R	32	0x0000 0200 + (0x08*k)	0x4800 0200 + (0x08*k)	0x4A00 0200 + (0x08*k)	0x4AE0 0200 + (0x08*k)
L4_AP_PROT_GROUP_MEMBERS_k_H (2)	R	32	0x0000 0204 + (0x08*k)	0x4800 0204 + (0x08*k)	0x4A00 0204 + (0x08*k)	0x4AE0 0204 + (0x08*k)
L4_AP_PROT_GROUP_ROLES_k_L (2)	R	32	0x0000 0280 + (0x08*k)	0x4800 0280 + (0x08*k)	0x4A00 0280 + (0x08*k)	0x4AE0 0280 + (0x08*k)
L4_AP_PROT_GROUP_ROLES_k_H (2)	R	32	0x0000 0284 + (0x08*k)	0x4800 0284 + (0x08*k)	0x4A00 0284 + (0x08*k)	0x4AE0 0284 + (0x08*k)
L4_AP_REGION_l_L (3)	RW	32	0x0000 0300 + (0x08*l)	0x4800 0300 + (0x08*l)	0x4A00 0300 + (0x08*l)	0x4AE0 0300 + (0x08*l)
L4_AP_REGION_l_H (3)	RW	32	0x0000 0304 + (0x08*l)	0x4800 0304 + (0x08*l)	0x4A00 0304 + (0x08*l)	0x4AE0 0304 + (0x08*l)

(1) i = 0 to 1 for PER_AP
i = 0 to 6 for CFG_AP
i = 0 to 2 for WKUP_AP

(2) k = 0 to 7 for PER_AP
k = 0 to 7 for CFG_AP
k = 0 to 7 for WKUP_AP

(3) l = 0 to 85 for PER_AP
l = 0 to 111 for CFG_AP
l = 0 to 29 for WKUP_AP

14.3.5.5.2 L4 Address Protection (L4 AP) Register Description

Table 14-494 through Table 14-517 describe the L4 AP registers.

Table 14-494. L4_AP_COMPONENT_L

Address Offset	0x000		
Physical Address	0x4800 0 000 0x4A00 0 000 0x4AE0 0 000	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Contains a component code and revision, which are used to identify the hardware of the component.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE																REV															

Bits	Field Name	Description	Type	Reset
31:16	CODE	Interconnect code	R	See (1).
15:0	REV	Component revision code	R	See (1).

(1) TI Internal Data

Table 14-495. Register Call Summary for Register L4_AP_COMPONENT_L

L4 Interconnects

- L4 Address Protection (L4 AP) Register Summary: [0]

Table 14-496. L4_AP_COMPONENT_H

Address Offset	0x004		
Physical Address	0x4800 0004 0x4A00 0004 0x4AE0 0004	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Contains a component code and revision, which are used to identify the hardware of the component.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0	R	0x0000 0000

Table 14-497. Register Call Summary for Register L4_AP_COMPONENT_H

L4 Interconnects

- L4 Address Protection (L4 AP) Register Summary: [0]

Table 14-498. L4_AP_SEGMENT_i_L

Address Offset	0x100 + (0x08*i)	**Index**	i = 0 to 1 for PER_AP i = 0 to 6 for CFG_AP i= 0 to 2 for WKUP_AP
Physical Address	0x4800 0100 + (0x08*i) 0x4A00 0100 + (0x08*i) 0x4AE0 0100 + (0x08*i)	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Define the base address of each segments		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																															

Bits	Field Name	Description	Type	Reset
31:0	BASE	The base address of the segment (with 0s from bit 0 to bit SIZE-1).	R	see Table 14-502

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Table 14-499. Register Call Summary for Register L4_AP_SEGMENT_i_L

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- L4 Address Protection (L4 AP) Register Summary: [1]

Table 14-500. L4_AP_SEGMENT_i_H

Address Offset	0x104 + (0x08*i)	**Index**	i = 0 to 1 for PER_AP i = 0 to 6 for CFG_AP i = 0 to 2 for WKUP_AP
Physical Address	0x4800 0104 + (0x08*i) 0x4A00 0104 + (0x08*i) 0x4AE0 0104 + (0x08*i)	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Define the size of each segments		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								SIZE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Read returns 0.	R	0x0000000
4:0	SIZE	Segment size is a power of 2, where 2^{SIZE} is the byte size of a segment (all segment registers use the same size).	R	see Table 14-502

Table 14-501. Register Call Summary for Register L4_AP_SEGMENT_i_H

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- L4 Address Protection (L4 AP) Register Summary: [1]

Table 14-502. Reset Value for L4_AP_SEGMENT_i

i	L4 PER		L4 CFG		L4 WKUP	
	BASE	SIZE	BASE	SIZE	BASE	SIZE
0	0x0000 0000	0x15	0x0000 0000	0x13	0x0000 0000	0x10
1	0x0020 0000	0x15	0x0008 0000	0x13	0x0001 0000	0x10
2	-	-	0x0010 0000	0x13	0x0002 0000	0x10
3	-	-	0x0018 0000	0x13	-	-
4	-	-	0x0020 0000	0x13	-	-
5	-	-	0x0028 0000	0x13	-	-
6	-	-	0x0030 0000	0x13	-	-

Table 14-503. L4_AP_PROT_GROUP_MEMBERS_k_L

Address Offset	0x200 + (0x08*k)	**Index**	k = 0 to 7 for PER_AP k = 0 to 7 for CFG_AP k = 0 to 7 for WKUP_AP
Physical Address	0x4800 0200 + (0x08*k) 0x4A00 0200 + (0x08*k) 0x4AE0 0200 + (0x08*k)	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Define ConnID bit vectors for a protection group.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CONNID_BIT_VECTOR															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x000000000000
15:0	CONNID_BIT_VECTOR	Specifies protection group members N is 2**W, where W is the connID width	R	0xFFFF

Table 14-504. Register Call Summary for Register L4_AP_PROT_GROUP_MEMBERS_k_L

L4 Interconnects

- Protection Group: [0] [1] [2] [3]
- L4 Firewall Address and Protection Register Settings: [4]
- Operational Modes Configuration: [5]
- L4 Address Protection (L4 AP) Register Summary: [6]

Table 14-505. L4_AP_PROT_GROUP_MEMBERS_k_H

Address Offset	0x204 + (0x08*k)	**Index**	k = 0 to 7 for PER_AP k = 0 to 7 for CFG_AP k = 0 to 7 for WKUP_AP
Physical Address	0x4800 0204 + (0x08*k) 0x4A00 0204 + (0x08*k) 0x4AE0 0204 + (0x08*k)	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Define ConnID bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Read returns 0's	R	0x0000 0000

Table 14-506. Register Call Summary for Register L4_AP_PROT_GROUP_MEMBERS_k_H

L4 Interconnects

- Protection Group: [0] [1] [2] [3]
- L4 Address Protection (L4 AP) Register Summary: [4]

Table 14-507. L4_AP_PROT_GROUP_ROLES_k_L

Address Offset	0x200 + (0x08*k)	**Index**	k = 0 to 7 for PER_AP k = 0 to 7 for CFG_AP k = 0 to 7 for WKUP_AP
Physical Address	0x4800 0280 + (0x08*k) 0x4A00 0280 + (0x08*k) 0x4AE0 0280 + (0x08*k)	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Define MReqInfo bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE																															

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Bits	Field Name	Description	Type	Reset
15:0	ENABLE	Setting of type acces allowed for the group of initiators.	R	0xFFFF

Table 14-508. Register Call Summary for Register L4_AP_PROT_GROUP_ROLES_k_L

L4 Interconnects

- Protection Group: [0] [1] [2] [3] [4] [5]
- L4 Firewall Address and Protection Register Settings: [6]
- Operational Modes Configuration: [7]
- L4 Address Protection (L4 AP) Register Summary: [8]

Table 14-509. Reset Value for L4_AP_PROT_GROUP_ROLES_k

	L4_PER		L4_CFG		L4_WKUP	
k	Type	Reset Value	Type	Reset Value	Type	Reset value
0	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
1	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
2	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
3	RW	0xFFFF FFFF	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
4	RW	0xFFFF FFFF	R	0xFFFF FFFF(1)	R	0xFFFF FFFF(1)
5	RW	0xFFFF FFFF	RW	0xFFFF FFFF	RW	0xFFFF FFFF
6	RW	0xFFFF FFFF	RW	0xFFFF FFFF	RW	0xFFFF FFFF
7	RW	0xFFFF FFFF	RW	0xFFFF FFFF	RW	0xFFFF FFFF

(1) Value exported from SCM and valid for GP device only (see *Figure 18-1, System Control Module*). The values of the other protection registers can be modified during run time.

Table 14-510. L4_AP_PROT_GROUP_ROLES_k_H

Address Offset	0x204 + (0x08*k)	**Index**	k = 0 to 7 for PER_AP k = 0 to 7 for CFG_AP k = 0 to 7 for WKUP_AP
Physical Address	0x4800 0284 + (0x08*k) 0x4A00 0284 + (0x08*k) 0x4AE0 0284 + (0x08*k)	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Define ConnID bit vectors for a protection group.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE																															

Bits	Field Name	Description	Type	Reset
31:0	ENABLE	Read returns 0s.	R	0xFFFF

Table 14-511. Register Call Summary for Register L4_AP_PROT_GROUP_ROLES_k_H

L4 Interconnects

- Protection Group: [0]
- L4 Firewall Address and Protection Register Settings: [1]
- L4 Address Protection (L4 AP) Register Summary: [2]

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Table 14-512. L4_AP_REGION_I_L

Address Offset	0x300 + (0x08*I)	**Index**	I = 0 to 85 for PER_AP I = 0 to 111 for CFG_AP I = 0 to 29 for WKUP_AP
Physical Address	0x4800 0300 + (0x08*I) 0x4A00 0300 + (0x08*I) 0x4AE0 0300 + (0x08*I)	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Define the base address of the region in respect to the segment it belongs to.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BASE																							

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Read returns 0.	R	0x00
20:0	BASE	Sets the base address of the region relative to its segment base.	R	See Table 14-516 to Table 14-517

Table 14-513. Register Call Summary for Register L4_AP_REGION_I_L

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- Operational Modes Configuration: [1]
- L4 Address Protection (L4 AP) Register Summary: [2]

Table 14-514. L4_AP_REGION_I_H

Address Offset	0x304 + (0x08*I)	**Index**	I = 0 to 99 for CORE_AP
Physical Address	0x4800 0304 + (0x08*I) 0x4A00 0304 + (0x08*I) 0x4AE0 0304 + (0x08*I)	**Instance**	PER_AP CFG_AP WKUP_AP
Description	Define the size, protection group and segment ID of the region		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MADDRSPACE				RESERVED	SEGMENT_ID			RESERVED	PROT_GROUP_ID			RESERVED	BYTE_DATA_WIDTH_EXP		RESERVED	PHY_TARGET_ID								RESERVED	SIZE						ENABLE

Bits	Field Name	Description	Type	Reset
31:28	MADDRSPACE	Target interconnect MAddrSpace	R	See Table 14-516 through Table 14-518.
27	RESERVED	Read returns 0	R	0x0
26:24	SEGMENT_ID	Segment ID of the region	R	See Table 14-516 through Table 14-518.
23	RESERVED	Read returns 0	R	0x0
22:20	PROT_GROUP_ID	Protection group ID	RW	See Table 14-516 through Table 14-518.
19	RESERVED	Read returns 0	R	0x0

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Bits	Field Name	Description	Type	Reset
18:17	BYTE_DATA_WIDTH_EXP	Target data byte width	R	See Table 14-516 through Table 14-518.
16:15	RESERVED	Read returns 0	R	0x0
14:8	PHY_TARGET_ID	Physical target ID	R	See Table 14-516 throughTable 14-518.
7	RESERVED	Read returns 0.	R	0x0
6:1	SIZE	Define the size of the region in bytes. 2^{SIZE} equals the region.	R	See Table 14-516 through Table 14-518.
0	ENABLE	0x0: Disable the region, no access allows 0x1: Enable the region, with access as define in registers	R	0x1

Table 14-515. Register Call Summary for Register L4_AP_REGION_I_H

L4 Interconnects

- L4 Firewall Address and Protection Register Settings: [0]
- L4 Address Protection (L4 AP) Register Summary: [1]

Table 14-516. L4_AP_REGION_I Reset Value for L4 PER

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
0	0x0	0x0	0x0	0x2	0x00	0x0B	0x1	0x00 0000
1	0x1	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1000
2	0x5	0x0	0x0	0x2	0x01	0x0B	0x1	0x00 0800
3	0x0	0x0	0x7	0x2	0x04	0x0C	0x1	0x02 0000
4	0x0	0x0	0x7	0x2	0x05	0x0C	0x1	0x02 1000
5	0x0	0x0	0x7	0x2	0x3E	0x0C	0x1	0x03 2000
6	0x0	0x0	0x7	0x2	0x3F	0x0C	0x1	0x03 3000
7	0x0	0x0	0x7	0x2	0x46	0x0C	0x1	0x03 4000
8	0x0	0x0	0x7	0x2	0x47	0x0C	0x1	0x03 5000
9	0x0	0x0	0x7	0x2	0x4E	0x0C	0x1	0x03 6000
10	0x0	0x0	0x7	0x2	0x4F	0x0C	0x1	0x03 7000
11	0x0	0x0	0x7	0x2	0x56	0x0C	0x1	0x03 E000
12	0x0	0x0	0x7	0x2	0x57	0x0C	0x1	0x03 F000
13	0x0	0x0	0x7	0x2	0x0E	0x0C	0x1	0x05 5000
14	0x0	0x0	0x7	0x2	0x0F	0x0C	0x1	0x05 6000
15	0x0	0x0	0x7	0x2	0x06	0x0C	0x1	0x05 7000
16	0x0	0x0	0x7	0x2	0x07	0x0C	0x1	0x05 8000
17	0x0	0x0	0x7	0x2	0x16	0x0C	0x1	0x05 9000
18	0x0	0x0	0x7	0x2	0x17	0x0C	0x1	0x05 A000
19	0x0	0x0	0x7	0x2	0x1E	0x0C	0x1	0x05 B000
20	0x0	0x0	0x7	0x2	0x1F	0x0C	0x1	0x05 C000
21	0x0	0x0	0x7	0x2	0x26	0x0C	0x1	0x05 D000
22	0x0	0x0	0x7	0x2	0x27	0x0C	0x1	0x05 E000
23	0x0	0x0	0x7	0x2	0x24	0x0C	0x1	0x06 0000
24	0x0	0x0	0x7	0x2	0x0A	0x0C	0x1	0x06 A000
25	0x0	0x0	0x7	0x2	0x0B	0x0C	0x1	0x06 B000
26	0x0	0x0	0x7	0x2	0x22	0x0C	0x1	0x06 C000
27	0x0	0x0	0x7	0x2	0x23	0x0C	0x1	0x06 D000
28	0x1	0x0	0x7	0x2	0x44	0x0C	0x1	0x06 E000
29	0x0	0x0	0x7	0x2	0x45	0x0C	0x1	0x06 F000
30	0x0	0x0	0x7	0x2	0x14	0x0C	0x1	0x07 0000

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Table 14-516. L4_AP_REGION_I Reset Value for L4 PER (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
31	0x0	0x0	0x7	0x2	0x15	0x0C	0x1	0x07 1000
32	0x0	0x0	0x7	0x2	0x1C	0x0C	0x1	0x07 2000
33	0x0	0x0	0x7	0x2	0x1D	0x0C	0x1	0x07 3000
34	0x0	0x0	0x7	0x2	0x25	0x0C	0x1	0x06 1000
35	0x0	0x0	0x7	0x2	0x36	0x0C	0x1	0x05 3000
36	0x0	0x0	0x7	0x2	0x37	0x0C	0x1	0x05 4000
37	0x0	0x0	0x7	0x2	0x0C	0x0C	0x1	0x0B 2000
38	0x0	0x0	0x7	0x2	0x0D	0x0C	0x1	0x0B 3000
39	0x0	0x0	0x7	0x2	0x12	0x0C	0x1	0x07 8000
40	0x0	0x0	0x7	0x2	0x13	0x0C	0x1	0x07 9000
41	0x0	0x0	0x7	0x2	0x5E	0x0C	0x1	0x08 6000
42	0x0	0x0	0x7	0x2	0x5F	0x0C	0x1	0x08 7000
43	0x0	0x0	0x7	0x2	0x66	0x0C	0x1	0x08 8000
44	0x0	0x0	0x7	0x2	0x67	0x0C	0x1	0x08 9000
45	0x0	0x0	0x7	0x2	0x2E	0x0C	0x1	0x05 1000
46	0x0	0x0	0x7	0x2	0x2F	0x0C	0x1	0x05 2000
47	0x0	0x0	0x7	0x2	0x08	0x0C	0x1	0x09 8000
48	0x0	0x0	0x7	0x2	0x09	0x0C	0x1	0x09 9000
49	0x0	0x0	0x7	0x2	0x10	0x0C	0x1	0x09 A000
50	0x0	0x0	0x7	0x2	0x11	0x0C	0x1	0x09 B000
51	0x0	0x0	0x7	0x2	0x3A	0x0C	0x1	0x09 C000
52	0x0	0x0	0x7	0x2	0x3B	0x0C	0x1	0x09 D000
53	0x0	0x0	0x7	0x2	0x54	0x0C	0x1	0x06 8000
54	0x0	0x0	0x7	0x2	0x55	0x0C	0x1	0x06 9000
55	0x0	0x0	0x1	0x2	0x1A	0x0D	0x1	0x09 0000
56	0x0	0x0	0x7	0x2	0x1B	0x0C	0x1	0x09 2000
57	0x0	0x0	0x1	0x2	0x3C	0x0C	0x1	0x0A 4000
58	0x0	0x0	0x7	0x2	0x3D	0x0C	0x1	0x0A 6000
59	0x0	0x0	0x1	0x2	0x2A	0x0E	0x1	0x0A 8000
60	0x0	0x0	0x7	0x2	0x2B	0x0C	0x1	0x0A C000
61	0x0	0x0	0x7	0x2	0x20	0x0C	0x1	0x0A D000
62	0x0	0x0	0x7	0x2	0x21	0x0C	0x1	0x0A E000
63	0x0	0x0	0x7	0x2	0x4C	0x0C	0x1	0x06 6000
64	0x0	0x0	0x7	0x2	0x4D	0x0C	0x1	0x06 7000
65	0x0	0x0	0x7	0x2	0x42	0x0C	0x1	0x0B 4000
66	0x0	0x0	0x7	0x2	0x43	0x0C	0x1	0x0B 5000
67	0x0	0x0	0x7	0x2	0x32	0x0C	0x1	0x0B 8000
68	0x0	0x0	0x7	0x2	0x33	0x0C	0x1	0x0B 9000
69	0x0	0x0	0x7	0x2	0x18	0x0C	0x1	0x0B A000
70	0x0	0x0	0x7	0x2	0x19	0x0C	0x1	0x0B B000
71	0x0	0x0	0x7	0x2	0x28	0x0C	0x1	0x0D 1000
72	0x0	0x0	0x7	0x2	0x29	0x0C	0x1	0x0D 2000
73	0x0	0x0	0x7	0x2	0x30	0x0C	0x1	0x0D 5000
74	0x0	0x0	0x7	0x2	0x31	0x0C	0x1	0x0D 6000
75	0x0	0x0	0x7	0x2	0x02	0x0C	0x1	0x0A 2000
76	0x0	0x0	0x7	0x2	0x03	0x0C	0x1	0x0A 3000
77	0x2	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1400

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Table 14-516. L4_AP_REGION_l Reset Value for L4 PER (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
78	0x3	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1800
79	0x4	0x0	0x7	0x2	0x00	0x0A	0x1	0x00 1C00
80	0x1	0x0	0x1	0x2	0x3C	0x0C	0x1	0x0A 5000
81	0x0	0x0	0x7	0x2	0x2C	0x0C	0x1	0x07 A000
82	0x0	0x0	0x7	0x2	0x2D	0x0C	0x1	0x07 B000
83	0x0	0x0	0x7	0x2	0x34	0x0C	0x1	0x07 C000
84	0x0	0x0	0x7	0x2	0x35	0x0C	0x1	0x07 D000

Table 14-517. L4_AP_REGION_l Reset Value for L4 CFG

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
0	0x0	0x0	0x0	0x2	0x00	0x0B	0x1	0x0 0000
1	0x1	0x0	0x7	0x2	0x00	0x0C	0x1	0x0 1000
2	0x5	0x0	0x0	0x2	0x01	0x0B	0x1	0x0 0800
3	0x0	0x0	0x7	0x2	0x44	0x0C	0x1	0x0 2000
4	0x0	0x0	0x7	0x2	0x45	0x0C	0x1	0x0 3000
5	0x0	0x0	0x7	0x2	0x5C	0x0C	0x1	0x0 4000
6	0x0	0x0	0x7	0x2	0x5D	0x0C	0x1	0x0 5000
7	0x0	0x0	0x7	0x2	0x02	0x0C	0x1	0x5 6000
8	0x0	0x0	0x7	0x2	0x03	0x0C	0x1	0x5 7000
9	0x0	0x0	0x7	0x2	0x07	0x0C	0x1	0x5 C000
10	0x0	0x0	0x7	0x2	0x06	0x0C	0x1	0x5 8000
11	0x0	0x0	0x7	0x2	0x0E	0x0C	0x1	0x6 2000
12	0x0	0x0	0x7	0x2	0x0F	0x0C	0x1	0x6 3000
13	0x0	0x1	0x7	0x2	0x20	0x0C	0x1	0x5 9000
14	0x0	0x1	0x7	0x2	0x21	0x0C	0x1	0x5 A000
15	0x0	0x1	0x7	0x2	0x10	0x0C	0x1	0x5 B000
16	0x0	0x1	0x7	0x2	0x11	0x0C	0x1	0x5 C000
17	0x0	0x1	0x7	0x2	0x18	0x0C	0x1	0x5 D000
18	0x0	0x1	0x7	0x2	0x19	0x0C	0x1	0x5 E000
19	0x0	0x1	0x5	0x2	0x54	0x0C	0x1	0x6 0000
20	0x0	0x1	0x7	0x2	0x55	0x0C	0x1	0x6 1000
21	0x0	0x0	0x7	0x2	0x4C	0x0D	0x1	0x0 8000
22	0x0	0x0	0x7	0x2	0x4D	0x0C	0x1	0x0 A000
23	0x0	0x0	0x7	0x2	0x0A	0x0C	0x1	0x6 6000
24	0x0	0x0	0x7	0x2	0x0B	0x0C	0x1	0x6 7000
25	0x0	0x1	0x7	0x2	0x04	0x0C	0x1	0x7 4000
26	0x0	0x1	0x7	0x2	0x05	0x0C	0x1	0x7 5000
27	0x0	0x1	0x7	0x2	0x0C	0x0C	0x1	0x7 6000
28	0x0	0x1	0x7	0x2	0x0D	0x0C	0x1	0x7 7000
29	0x0	0x4	0x1	0x2	0x12	0x0C	0x1	0x1 E000
30	0x0	0x4	0x7	0x2	0x13	0x0C	0x1	0x1 F000
31	0x0	0x4	0x1	0x2	0x30	0x0C	0x1	0x0 A000
32	0x0	0x4	0x7	0x2	0x31	0x0C	0x1	0x0 B000
33	0x0	0x4	0x1	0x2	0x4E	0x0C	0x1	0x0 6000
34	0x0	0x4	0x7	0x2	0x4F	0x0C	0x1	0x0 7000

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Table 14-517. L4_AP_REGION_I Reset Value for L4 CFG (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
35	0x0	0x4	0x1	0x2	0x46	0x0C	0x1	0x0 4000
36	0x0	0x4	0x7	0x2	0x47	0x0C	0x1	0x0 5000
37	0x0	0x4	0x1	0x2	0x52	0x0C	0x1	0x1 2000
38	0x0	0x4	0x7	0x2	0x53	0x0C	0x1	0x1 3000
39	0x0	0x4	0x1	0x2	0x14	0x0C	0x1	0x0 C000
40	0x0	0x4	0x7	0x2	0x15	0x0C	0x1	0x0 D000
41	0x0	0x4	0x1	0x2	0x56	0x0C	0x1	0x1 0000
42	0x0	0x4	0x7	0x2	0x57	0x0C	0x1	0x1 1000
43	0x0	0x4	0x1	0x2	0x42	0x0C	0x1	0x1 6000
44	0x0	0x4	0x7	0x2	0x43	0x0C	0x1	0x1 7000
45	0x0	0x4	0x1	0x2	0x1C	0x0C	0x1	0x1 4000
46	0x0	0x4	0x7	0x2	0x1D	0x0C	0x1	0x1 5000
47	0x0	0x4	0x1	0x2	0x1A	0x0C	0X1	0x1 8000
48	0x0	0x4	0x7	0x2	0x1B	0x0C	0x1	0x1 9000
49	0x0	0x4	0x1	0x2	0x4A	0x0C	0x1	0x2 0000
50	0x0	0x4	0x7	0x2	0x4B	0x0C	0x1	0x2 1000
51	0x0	0x4	0x1	0x2	0x24	0x0C	0x1	0x2 6000
52	0x0	0x4	0x7	0x2	0x25	0x0C	0x01	0x2 7000
53	0x0	0x4	0x1	0x2	0x38	0x0C	0x01	0x2 8000
54	0x0	0x4	0x7	0x2	0x39	0x0C	0x01	0x2 9000
55	0x0	0x4	0x1	0x2	0x5A	0x0C	0X01	0x2 A000
56	0x0	0x4	0x7	0x2	0x5B	0x0C	0x01	0x2 B000
57	0x0	0x4	0x1	0x2	0x40	0x0C	0x01	0x1 C000
58	0x0	0x4	0x7	0x2	0x41	0x0C	0x01	0x1 D000
59	0x0	0x2	0x7	0x2	0x2C	0x0C	0x01	0x0 2000
60	0x0	0x2	0x7	0x2	0x2D	0x0C	0x01	0x0 3000
61	0x0	0x2	0x7	0x2	0x26	0x0C	0x01	0x0 8000
62	0x0	0x2	0x7	0x2	0x27	0x0C	0x01	0x0 9000
63	0x0	0x2	0x7	0x2	0x22	0x0C	0x01	0x0 A000
64	0x0	0x2	0x7	0x2	0x23	0x0C	0x01	0x0 B000
65	0x0	0x1	0x7	0x2	0x6C	0x0C	0x01	0x3 6000
66	0x0	0x1	0x7	0x2	0x6D	0x0C	0x01	0x3 7000
67	0x0	0x1	0x7	0x2	0x64	0x0C	0x01	0x4 D000
68	0x0	0x1	0x7	0x2	0x65	0x0C	0x01	0x4 E000
69	0x0	0x0	0x7	0x2	0x2A	0x0D	0x01	0x5 E000
70	0x0	0x0	0x7	0x2	0x2B	0x0C	0x01	0x6 0000
71	0x0	0x0	0x7	0x2	0x1E	0x0C	0x01	0x6 4000
72	0x0	0x0	0x7	0x2	0x1F	0x0C	0x01	0x6 5000
73	0x0	0x4	0x1	0x2	0x3E	0x0C	0x01	0x1 A000
74	0x0	0x4	0x7	0x2	0x3F	0x0C	0x01	0x1 B000
75	0x0	0x4	0x1	0x2	0x48	0x0C	0x01	0x2 4000
76	0x0	0x4	0x7	0x2	0x49	0x0C	0x01	0x2 5000
77	0x2	0x0	0x7	0x2	0x06	0x0C	0x01	0x5 A000
78	0x3	0x0	0x7	0x2	0x06	0x0C	0x01	0x5 B000
79	0x0	0x0	0x7	0x2	0x2E	0x0E	0x01	0x7 0000
80	0x0	0x0	0x7	0x2	0x2F	0x0C	0x01	0x7 4000
81	0x0	0x0	0x7	0x2	0x32	0x0C	0x01	0x7 5000

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Table 14-517. L4_AP_REGION_I Reset Value for L4 CFG (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
82	0x0	0x0	0x7	0x2	0x33	0x0C	0x01	0x7 6000
83	0x0	0x1	0x7	0x2	0x28	0x0E	0x01	0x0 0000
84	0x1	0x1	0x7	0x2	0x28	0x0C	0x01	0x0 4000
85	0x2	0x1	0x7	0x2	0x28	0x0C	0x01	0x0 5000
86	0x3	0x1	0x7	0x2	0x28	0x0C	0x01	0x0 6000
87	0x4	0x1	0x7	0x2	0x28	0x0C	0x01	0x0 7000
88	0x0	0x1	0x7	0x2	0x29	0x0C	0x01	0x0 8000
89	0x0	0x1	0x7	0x2	0x36	0x0E	0x01	0x1 0000
90	0x1	0x1	0x7	0x2	0x36	0x0C	0x01	0x1 4000
91	0x2	0x1	0x7	0x2	0x36	0x0C	0x01	0x1 5000
92	0x3	0x1	0x7	0x2	0x36	0x0C	0x01	0x1 6000
93	0x4	0x1	0x7	0x2	0x36	0x0C	0x01	0x1 7000
94	0x0	0x1	0x7	0x2	0x37	0x0C	0X01	0x1 8000
95	0x0	0x1	0x7	0x2	0x50	0x0E	0x01	0x2 0000
96	0x1	0x1	0x7	0x2	0x50	0x0C	0x01	0x2 4000
97	0x2	0x1	0x7	0x2	0x50	0x0C	0x01	0x2 5000
98	0x3	0x1	0x7	0x2	0x50	0x0C	0x01	0x2 6000
99	0x4	0x1	0x7	0x2	0x50	0x0C	0x01	0x2 7000
100	0x0	0x1	0x7	0x2	0x51	0x0C	0x01	0x2 8000
101	0x0	0x2	0x7	0x2	0x16	0x10	0x01	0x4 0000
102	0x0	0x2	0x7	0x2	0x17	0x0C	0x01	0x5 0000
103	0x0	0x4	0x1	0x2	0x3C	0x0C	0x01	0x0 2000
104	0x0	0x4	0x7	0x2	0x3D	0x0C	0x01	0x0 3000
105	0x0	0x4	0x1	0x2	0x34	0x0C	0x01	0x0 8000
106	0x0	0x4	0x7	0x2	0x35	0x0C	0x01	0x0 9000
107	0x0	0x4	0x1	0x2	0x3A	0x0C	0x01	0x2 2000
108	0x0	0x4	0x7	0x2	0x3B	0x0C	0x01	0x2 3000
109	0x0	0x0	0x7	0x2	0x08	0x11	0x01	0x2 0000
110	0x0	0x0	0x7	0x2	0x09	0x0C	0x01	0x4 0000
111	0x1	0x0	0x7	0x2	0x06	0x0C	0x01	0x5 9000

Table 14-518. L4_AP_REGION_I Reset values for L4 WKUP

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
0	0x0	0x0	0x0	0x2	0x0	0x0B	0x01	0x0000
1	0x1	0x0	0x7	0x2	0x0	0x0C	0x01	0x1000
2	0x5	0x0	0x0	0x2	0x01	0x0B	0x01	0x0800
3	0x0	0x0	0x7	0x2	0x08	0x0D	0x01	0x6000
4	0x0	0x0	0x7	0x2	0x09	0x0C	0x01	0x8000
5	0x0	0x1	0x7	0x2	0x10	0x0C	0x01	0x0000
6	0x0	0x1	0x7	0x2	0x11	0x0C	0x01	0x1000
7	0x0	0x1	0x7	0x2	0x14	0x0C	0x01	0x4000
8	0x0	0x1	0x7	0x2	0x15	0x0C	0x01	0x5000
9	0x0	0x1	0x7	0x2	0x18	0x0C	0x01	0x8000
10	0x0	0x1	0x7	0x2	0x19	0x0C	0x01	0x9000
11	0x0	0x1	0x7	0x2	0x1C	0x0C	0x01	0xC000

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Table 14-518. L4_AP_REGION_I Reset values for L4 WKUP (continued)

Region	MADDRSPACE	SEGMENT_ID	PROT_GROUP_ID	BYTE_DATA_WIDTH_EXP	PHY_TARGET_ID	SIZE	ENABLE	BASE
12	0x0	0x1	0x7	0x2	0x1D	0x0C	0x01	0xD000
13	0x0	0x2	0x7	0x2	0x24	0x0C	0x01	0x6000
14	0x0	0x2	0x7	0x2	0x25	0x0C	0x01	0xA000
15	0x0	0x0	0x7	0x2	0x2C	0x0C	0x01	0xA000
16	0x0	0x0	0x7	0x2	0x2D	0x0C	0x01	0xB000
17	0x0	0x0	0x7	0x2	0x20	0x0C	0x01	0x4000
18	0x0	0x0	0x7	0x2	0x21	0x0C	0x01	0x5000
19	0x0	0x0	0x7	0x2	0x28	0x0C	0x01	0xC000
20	0x0	0x0	0x7	0x2	0x29	0x0C	0x01	0xD000
21	0x0	0x2	0x1	0x2	0x04	0x0C	0x01	0x0000
22	0x0	0x2	0x7	0x2	0x05	0x0C	0x01	0x1000
23	0x0	0x2	0x1	0x2	0x0C	0x0C	0x01	0x2000
24	0x0	0x2	0x7	0x2	0x0D	0x0C	0x01	0x3000
25	0x1	0x2	0x3	0x2	0x24	0x0A	0x01	0x7000
26	0x2	0x2	0x1	0x2	0x24	0x0B	0x01	0x8000
27	0x3	0x2	0x4	0x2	0x24	0x08	0x01	0x9000
28	0x6	0x2	0x1	0x2	0x24	0x09	0x01	0x8800
29	0xE	0x2	0x1	0x2	0x24	0x08	0x01	0x8A00

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Memory Subsystem

This chapter introduces the memory subsystem of the device.

NOTE: Some of the memory subsystem features, primarily those concerning the device I/O pads, are not available in all OMAP54xx devices.

For details, see , *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

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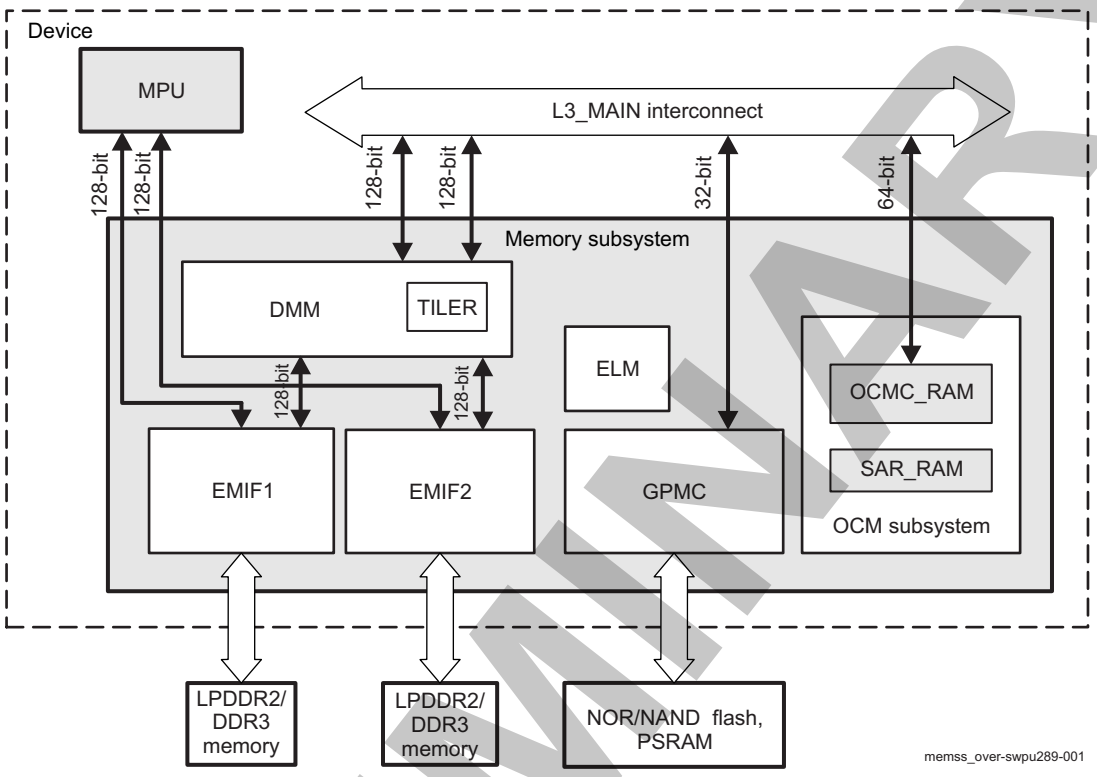
15.1 Memory Subsystem Overview

Figure 15-1 shows a functional diagram of all memory subsystems in the device.

Figure 15-1. Memory Subsystem Functional Diagram



15.1.1 DMM Overview

The dynamic memory manager (DMM) module is typically located immediately in front of the synchronous dynamic random access memory (SDRAM) controllers (EMIF), as shown in Figure 15-1, *Memory Subsystem Functional Diagram*.

In a broad sense, the DMM manages various aspects of memory accesses such as:

- Initiator-indexed priority generation
- Multizone SDRAM interleaving configuration
- Block object transfer optimization – tiling
- Centralized low-latency page translation – MMU-like feature

The dynamic qualifier for memory management highlights the software configurability, and hence the runtime nature, of the four aspects of memory management handled by the DMM.

15.1.1.1 DMM Features

From a functional perspective, the role of the DMM is to:

- Add initiator-based priority to any incoming requests
- Perform to/from tiling conversions of tiled requests
- Make on-the-fly basic transforms, such as quadrant rotations and mirroring
- Optionally, provide a low-latency page-based translation to handle memory fragmentation – MMU
- Distribute the traffic on all attached memory controllers according to the interleaving configuration

The main features of the DMM are:

- Programmable multizone DRAM mapping and interleaving configuration

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- Programmable initiator-based request priority extension
- Multichannel memory transfer optimization
- Single SDRAM page request generation
- Low-latency interconnect port
- Page-grained address translation to manage memory fragmentation
- Automatic synchronized reloading of the address translation table

15.1.2 TILER Overview

The tiling and isometric lightweight engine for rotation (TILER) is a submodule of the DMM (see Figure 15-1) and is therefore described in Section 15.2.1, *Dynamic Memory Manager*.

The TILER is intended to improve bidimensional (tiled) block transfer efficiency. It is, therefore, a module aimed at:

- Primarily, efficient handling of 2-dimension (2D) data mapped in tiles, such as video or graphics macroblocks
- Optionally, managing the memory fragmentation and zero-copy physical frame-buffer swapping through a page-grained translation
- Making isometric (distance preserving) transforms, such as 90-, 180-, or 270-degree rotations, with a horizontal or vertical reflection

The lightweight qualifier of this engine highlights its limited support of isometric transforms, as:

- Rotation performs only basic quadrant rotations by some multiple of 90 degrees.
- Reflection is limited to horizontal and vertical flip.
- Translation is restricted to a 4-KiB page granularity.

Written differently, the functionality of the TILER is to map a 2D virtually addressed interconnect request into one or more physically addressed interconnect requests by:

- Transforming the virtual address, data, and byte-enable to match the requested 0-, 90-, 180-, or 270-degree orientation in a tiled 2D addressing space
- Optionally, translating the oriented tiled address by a page-specific vector to manage memory fragmentation and physical object aliasing

15.1.2.1 TILER Features

The main features of the TILER are:

- Efficiency improvement of 2D block access on SDRAMs
- Optimized interlaced access on tiled frames
- 2D virtual-to-physical address translation of SDRAM bidimensional objects to handle rotation
- Page-grained address translation to manage memory fragmentation and physical buffer aliasing
- Unlimited number of 2D tiled objects supported in any (0, 90, 180, or 270 degrees) orientation
- Full bandwidth use by minimizing the size of raster-based initiator buffers
- Optimization of multichannel memory transfers
- Interconnect request granularity balance (in X and Y directions)

15.1.3 EMIF Overview

The two external memory interface (EMIF) modules are typically located near the DMM module, as shown in Figure 15-1 , *Memory Subsystem Functional Diagram*.

The EMIF module provides connectivity between the device and LPDDR2-type or DDR3-type of memories and manages data bus read/write accesses between external memories and device subsystems having master access to the L3_MAIN interconnect and DMA capability.

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15.1.3.1 Main Features

Each EMIF module has the following capabilities:

- Supports JEDEC standard-compliant DDR3-SDRAM, DDR3L-SDRAM, and LPDDR2-SDRAM (S2 and S4) devices
- 4-GiB SDRAM address range over two chip-selects (2 GiB per chip-select) (configurable with the dynamic memory manager (DMM) module; see Section 15.2.1, *Dynamic Memory Manager*, for more information)

NOTE: Even though the two EMIF modules work independently and can have connected different (LPDDR2 and DDR3) memories at a time, the device package restricts the physical connections to only one memory type (LPDDR2 or DDR3) per device. See more details about device family in , *Introduction*

- Supports SDRAM devices with one, two, four, or eight internal banks
- Data bus widths:
  - 128-bit L3_MAIN (system) interconnect data bus width
  - 128-bit port for direct connection with MPU subsystem
  - 32-bit SDRAM data bus width
- Supports CAS latencies:
  - DDR3: 5, 6, 7, 8, 9, 10, and 11
  - LPDDR2: 3, 4, 5, 6, 7, and 8
- Supports 256-, 512-, 1024-, and 2048-word page sizes
- Supported burst length: 8
- Supports sequential burst type
  - For LPDDR2, burst read can be interrupted by another read, burst write can be interrupted by another write.
  - DDR3 does not support the burst interrupt of a BL8 command
- SDRAM auto initialization from reset or configuration change for DDR3 (LPDDR2 needs to have initalization started via software)
- Supports bank interleaving across both chip-selects
- Supports self refresh and power-down modes for low power
- Supports deep power-down mode for LPDDR2 for low power
- Partial array self-refresh and temperature-controlled self-refresh modes for low power. Temperature-controlled self-refresh is supported only for mobile SDRAM having on-chip temperature sensor.
- Supports temperature monitoring for LPDDR2
- Output impedance (ZQ) calibration
- Supports on-die termination (ODT) on DDR3
- Supports prioritized refresh
- Programmable SDRAM refresh rate and backlog counter
- Programmable SDRAM timing parameters
- Write/read leveling/calibration and data eye training for DDR3.

The EMIF modules do not support:

- Burst chop for DDR3.
- Auto precharge
- Per-bank refreshes for LPDDR2-SDRAM

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15.1.4 GPMC Overview

The general-purpose memory controller (GPMC) is an unified memory controller dedicated to interfacing external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in nonmuxed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

15.1.4.1 GPMC Features

The GPMC is the external memory controller of the device. The GPMC data access engine provides a flexible programming model for communication with all standard memories. The GPMC supports various accesses:

- Asynchronous read/write access
- Asynchronous read page access (4, 8, and 16 Word16)
- Synchronous read/write access
- Synchronous read/write burst access without wrap capability (4, 8, and 16 Word16)
- Synchronous read/write burst access with wrap capability (4, 8, and 16 Word16)
- Address/data-multiplexed access
- Little- and big-endian access

The GPMC can communicate with a wide range of external devices:

- External asynchronous or synchronous 8-bit wide memory or device (nonburst device)
- External asynchronous or synchronous 16-bit wide memory or device
- External 16-bit nonmultiplexed device with limited address range (2 KiB)
- External 16-bit address/data-multiplexed NOR flash device
- External 8-bit and 16-bit NAND flash device
- External 16-bit pseudo-SRAM (pSRAM) device

The main features of the GPMC are:

- 8- or 16-bit-wide data path to external memory device
- Supports up to eight CS regions of programmable size and programmable base addresses in a total address space of 512 MiB
- Supports transactions controlled by a firewall
- On-the-fly error code detection using the Bose-ChaudhurI-Hocquenghem (BCH) (t = 4, 8, or 16) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)
- Fully pipelined operation for optimal memory bandwidth use
- External device clock provided from L3_MAIN clock (GPMC_FCLK) divided by 1, 2, 3, or 4
- Supports programmable autoclock gating when no access is detected
- Independent and programmable control signal timing parameters for setup and hold time on a per-chip basis. Parameters are set according to the memory device timing parameters, with a timing granularity of one GPMC_FCLK clock cycle.
- Flexible internal access time control (WAIT state) and flexible handshake mode using external WAIT pin monitoring
- Support bus keeping
- Support bus turnaround
- Prefetch and write posting engine associated with system DMA (sDMA) to achieve full performance from the AND device with minimum effect on NOR/SRAM concurrent access

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NOTE: Page mode is available only in nonmultiplexed mode.

15.1.5 ELM Overview

In the case of NAND modules with no internal correction capability, sometimes referred to as bare NAND, the correction process can be delegated to the error location module (ELM) used in conjunction with the GPMC.

15.1.5.1 ELM Features

The ELM features:

- 4, 8, and 16 bits per 512-byte block error location based on BCH algorithm
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation when error location process completes:
  - When the full page has been processed in page mode
  - For each syndrome polynomial in continuous mode

15.1.6 OCM Overview

The on-chip memory (OCM) subsystem consists of the following OCM controllers.

- One connected to an on-chip RAM (SAR RAM)
- One connected to an on-chip SRAM (L3 SRAM)

Each memory controller has its own dedicated interface to the L3_MAIN interconnect.

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15.2 Dynamic Memory Manager

15.2.1 DMM Overview

This section describes the dynamic memory manager (DMM) and its tiling and isometric lightweight engine for rotation (TILER) submodule.

The DMM is introduced in Section 15.1, *Memory Subsytem Overview*.

The function of the DMM is to:

- Add initiator-based priority to any incoming requests
- Perform to-and-from tiling conversions of tiled requests
- Make on-the-fly basic transforms, such as quadrant rotations and mirroring
- Optionally provide a low-latency page-based translation to handle memory fragmentation – memory management unit (MMU)
- Distribute the traffic on all attached memory controllers according to the interleaving configuration

The TILER is also introduced in Section 15.1, *Memory Subsystem Overview*.

The functions of the TILER are:

- Primary handling efficiently 2-dimensional (2D) data mapped in tiles, such as video or graphics macroblocks
- Optionally managing the memory fragmentation and zero-copy physical frame buffers swapping through a page-grained translation
- Allowing optimized interlaced accesses on tiled frames
- Making (distance preserving) transforms, such as 90-, 180-, or 270-degree rotations, with a horizontal or vertical reflection
- Interleaving the memory accesses among the two memory controllers (also called EMIF). For more information, see Section 15.3.1, *EMIF Controller*.

Figure 15-2 is an overview of the DMM and TILER in the device.

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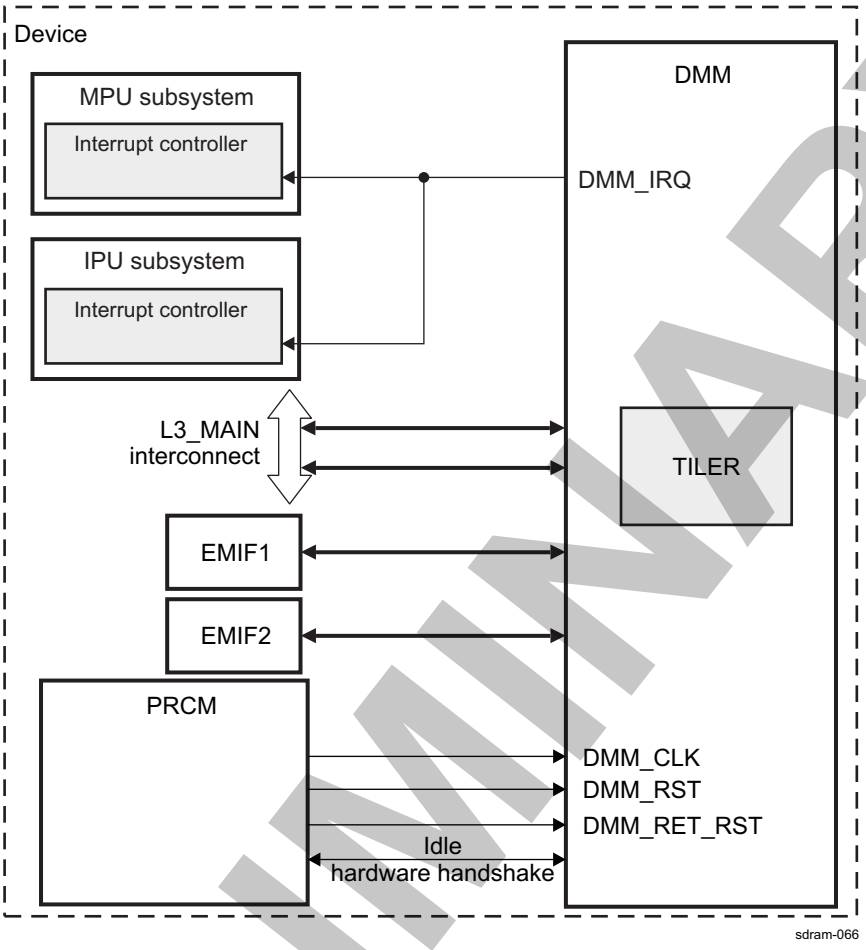
Figure 15-2. DMM and Tiler Overview



15.2.2 DMM Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

- IDLE hardware handshake (the DMM supports only smart-idle mode)
- No STANDBY hardware handshake
- No wake-up request
- No system direct memory access (sDMA) requests
- One interrupt line for interrupt request (IRQ)
- One functional clock

Figure 15-3 shows the integration of DMM in the device.

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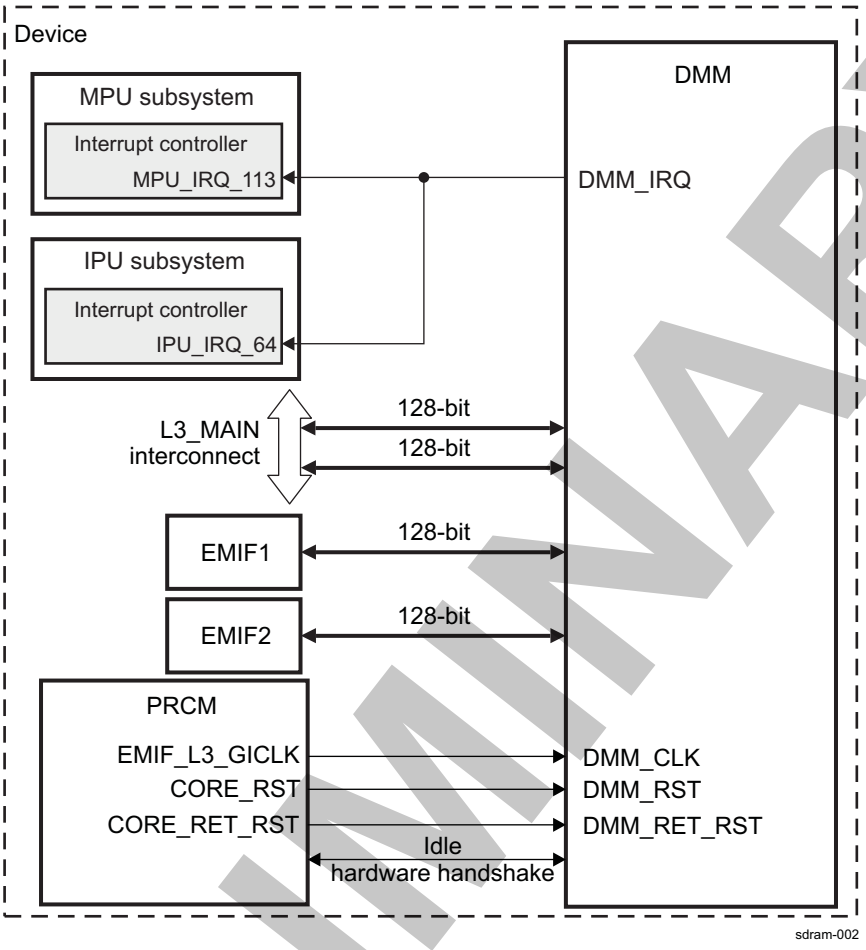
Figure 15-3. DMM Integration



NOTE: For more information about the IDLE hardware handshake, see Section 3.1.1, *Power, Reset, and Clock Management*.

Table 15-1 through Table 15-3 summarize the integration of DMM in the device.

Table 15-1. DMM Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
DMM	PD_CORE	No	L3_MAIN

Table 15-2. DMM Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMM	DMM_CLK	EMIF_L3_GICLK	PRCM	DMM interface and functional clock. For information about power, reset, and clock management (PRCM) module clock gating and management, see Section 3.1.1, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**

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Table 15-2. DMM Clocks and Resets (continued)

DMM	DMM_RST	CORE_RST	PRCM	Functional reset. For information about PRCM reset sources and distribution, see Section 3.1.1, *Power, Reset, and Clock Management*.
DMM	DMM_RET_RST	CORE_RET_RST	PRCM	Reset for retention flip-flop (RFF) registers, namely: DMM_SYSCONFIG DMM_LISA_LOCK DMM_LISA_MAP_i DMM_TILER_OR0 DMM_TILER_OR1 DMM_PAT_VIEW0 DMM_PAT_VIEW1 DMM_PAT_VIEW_MAP_i DMM_PAT_VIEW_MAP_BASE DMM_PAT_DESCR_i DMM_PAT_AREA_i DMM_PAT_CTRL_i DMM_PAT_DATA_i DMM_PEG_PRIO_k DMM_PEG_PRIO_PAT For information about PRCM reset sources and distribution, see Section 3.1.1, *Power, Reset, and Clock Management*.

Table 15-3. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DMM	DMM_IRQ	MPU_IRQ_113	MPU	DMM interrupt to the MPU subsystem
	DMM_IRQ	IPU_IRQ_64	IPU	DMM interrupt to the IPU subsystem
No DMA Requests				

15.2.2.1 DMM Configuration

Table 15-4 lists all configured parameters for the DMM. These parameters are read-only.

Table 15-4. DMM TILER Container Geometry

Scope	Bit field	Configuration Value	Description
LISA	DMM_HWINFO[3:0] TILER_CNT	0x2	Two TILER instances in the DMM
	DMM_HWINFO[19:16] ROBIN_CNT	0x2	Two ROBIN instances in the DMM
	DMM_LISA_HWINFO[4:0] SECTION_CNT	0x4	Four DMM sections
	DMM_LISA_HWINFO[11:8] SDRC_CNT	0x2	Two SDRAM controllers (EMIF) attached
TILER	DMM_TILER_HWINFO[6:0] OR_CNT	0x10	16 orientation entries
PAT	DMM_PAT_GEOMETRY[4:0] PAGE_SZ	0x1	4-KiB page granularity
	DMM_PAT_GEOMETRY[19:16] CONT_WDTH	0x8	Container width of 256 pages
	DMM_PAT_GEOMETRY[26:24] CONT_HGHT	0x8	Container height of 256 pages
	DMM_PAT_GEOMETRY[13:8] ADDR_RANGE	0x10	2-GiB PAT output physical address range
	DMM_PAT_HWINFO[6:0] VIEW_CNT	0x10	16 view entries
	DMM_PAT_HWINFO[11:8] VIEW_MAP_CNT	0x4	Four view maps
	DMM_PAT_HWINFO[20:16] LUT_CNT	0x1	One PAT LUT

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Table 15-4. DMM TILER Container Geometry (continued)

Scope	Bit field	Configuration Value	Description
	DMM_PAT_HWINFO[28:24] ENGINE_CNT	0x4	Four PAT refill engines
PEG	DMM_PEG_HWINFO[6:0] PRIO_CNT	0x40	64 priority entries

15.2.3 DMM Functional Description

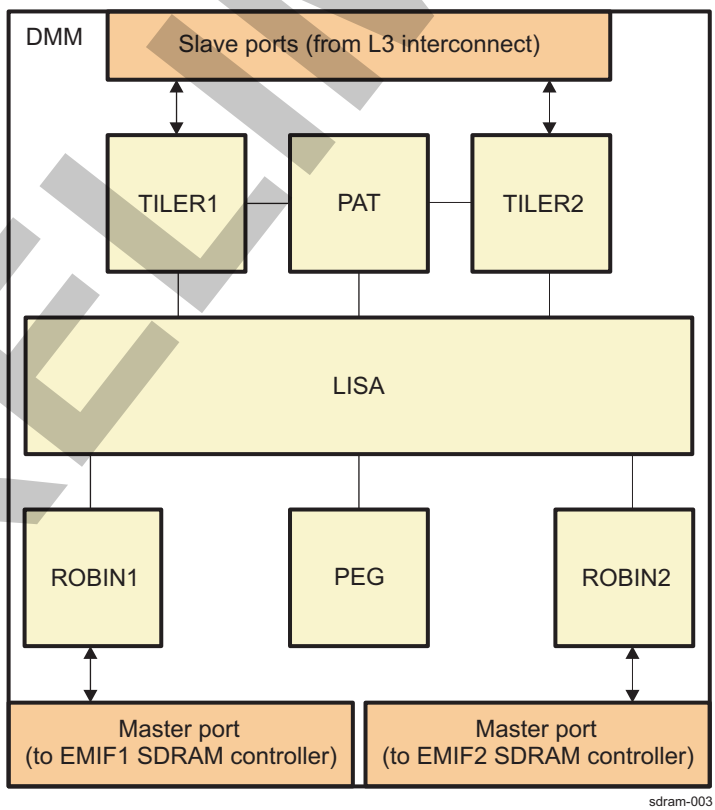
15.2.3.1 DMM Block Diagram

Figure 15-4 shows the DMM macro architecture. The DMM consists of six blocks:

- Two TILERs, each with its own interconnect slave port for converting requests back and forth between the input virtual addressing mode and the output physical tiledaddressing mode. The tiling conversions of requests, write data, and responses is performed entirely in the TILER blocks.
- Two reordering buffer and initiator nodes (ROBINs), each with its own interconnect master port to initiate requests to the SDRC and allow tiled data, tiled response, and split response reconstruction. The ROBIN block manages only the reordering buffer and performs data reordering due to the orientation.
- A physical address translator (PAT) for managing the memory fragmentation
- A priority extension generator (PEG) to generate priorities required by the SDRC; these priorities are not used in the DMM.
- A local interconnect and synchronization agent (LISA) to synchronize all DMM subsystems and provide access to their configuration registers

Figure 15-4 is a block diagram of the DMM.

Figure 15-4. DMM Block Diagram



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CAUTION

The interconnect must ensure that virtually addressed requests target only a TILER port.

15.2.3.2 DMM Clock Configuration

Table 15-5 describes the DMM clocks.

Table 15-5. DMM Clocks

Signal	I/O[1]	Description
DMM_CLK	I	Functional and interface clock

(1) I = Input; O = Output

The DMM is concerned with SDRC management and is in the MEMIF clock domain among the SDRCs. The DMM is a fully synchronous module, which uses the clock and clock-enable signals provided in the MEMIF clock domain to generate its interface and functional clocks.

To configure DMM_CLK control and settings, see Table 15-2.

15.2.3.3 DMM Power Management

DMM power is supplied by the CORE power domain, and DMM power management complies with system power-management guidelines.

Table 15-6 describes the power-management features available for the DMM module.

Table 15-6. DMM Local Power-Management Features

Feature	Registers	Description
Slave idle modes	DMM_SYSCONFIG[3:2] SIDLEMODE bit field	Only smart-idle wake-up mode is available.

15.2.3.4 DMM Interrupt Requests

Errors in PAT area refill registers are reported through the DMM_PAT_STATUS_i[15:10] ERROR bit field (see Table 15-7).

Table 15-7. DMM Hardware Status Features

Feature	Type	Register	Description
PAT error flags	Read-only	DMM_PAT_STATUS_i[15:10] ERROR (where i = 0 to 3)	Unexpected update of the PAT area refill registers

Table 15-8 lists the event flags, and their masks, that can cause module interrupts.

Table 15-8. Events

Interrupt	Event Flag	Event Mask
ERR_LUT_MISS3	DMM_PAT_IRQSTATUS[31] ERR_LUT_MISS3 DMM_PAT_IRQSTATUS_RAW[31] ERR_LUT_MISS3	DMM_PAT_IRQENABLE_SET[31] ERR_LUT_MISS3 DMM_PAT_IRQENABLE_CLR[31] ERR_LUT_MISS3
ERR_UPD_DATA3	DMM_PAT_IRQSTATUS[30] ERR_UPD_DATA3 DMM_PAT_IRQSTATUS_RAW[30] ERR_UPD_DATA3	DMM_PAT_IRQENABLE_SET[30] ERR_UPD_DATA3 DMM_PAT_IRQENABLE_CLR[30] ERR_UPD_DATA3

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Table 15-8. Events (continued)

Interrupt	Event Flag	Event Mask
ERR_UPD_CTRL3	DMM_PAT_IRQSTATUS[29] ERR_UPD_CTRL3 DMM_PAT_IRQSTATUS_RAW[29] ERR_UPD_CTRL3	DMM_PAT_IRQENABLE_SET[29] ERR_UPD_CTRL3 DMM_PAT_IRQENABLE_CLR[29] ERR_UPD_CTRL3
ERR_UPD_AREA3	DMM_PAT_IRQSTATUS[28] ERR_UPD_AREA3 DMM_PAT_IRQSTATUS_RAW[28] ERR_UPD_AREA3	DMM_PAT_IRQENABLE_SET[28] ERR_UPD_AREA3 DMM_PAT_IRQENABLE_CLR[28] ERR_UPD_AREA3
ERR_INV_DATA3	DMM_PAT_IRQSTATUS[27] ERR_INV_DATA3 DMM_PAT_IRQSTATUS_RAW[27] ERR_INV_DATA3	DMM_PAT_IRQENABLE_SET[27] ERR_INV_DATA3 DMM_PAT_IRQENABLE_CLR[27] ERR_INV_DATA3
ERR_INV_DSC3	DMM_PAT_IRQSTATUS[26] ERR_INV_DSC3 DMM_PAT_IRQSTATUS_RAW[26] ERR_INV_DSC3	DMM_PAT_IRQENABLE_SET[26] ERR_INV_DSC3 DMM_PAT_IRQENABLE_CLR[26] ERR_INV_DSC3
FILL_LST3	DMM_PAT_IRQSTATUS[25] FILL_LST3 DMM_PAT_IRQSTATUS_RAW[25] FILL_LST3	DMM_PAT_IRQENABLE_SET[25] FILL_LST3 DMM_PAT_IRQENABLE_CLR[25] FILL_LST3
FILL_DSC3	DMM_PAT_IRQSTATUS[24] FILL_DSC3 DMM_PAT_IRQSTATUS_RAW[24] FILL_DSC3	DMM_PAT_IRQENABLE_SET[24] FILL_DSC3 DMM_PAT_IRQENABLE_CLR[24] FILL_DSC3
ERR_LUT_MISS2	DMM_PAT_IRQSTATUS[23] ERR_LUT_MISS2 DMM_PAT_IRQSTATUS_RAW[23] ERR_LUT_MISS2	DMM_PAT_IRQENABLE_SET[23] ERR_LUT_MISS2 DMM_PAT_IRQENABLE_CLR[23] ERR_LUT_MISS2
ERR_UPD_DATA2	DMM_PAT_IRQSTATUS[22] ERR_UPD_DATA2 DMM_PAT_IRQSTATUS_RAW[22] ERR_UPD_DATA2	DMM_PAT_IRQENABLE_SET[22] ERR_UPD_DATA2 DMM_PAT_IRQENABLE_CLR[22] ERR_UPD_DATA2
ERR_UPD_CTRL2	DMM_PAT_IRQSTATUS[21] ERR_UPD_CTRL2 DMM_PAT_IRQSTATUS_RAW[21] ERR_UPD_CTRL2	DMM_PAT_IRQENABLE_SET[21] ERR_UPD_CTRL2 DMM_PAT_IRQENABLE_CLR[21] ERR_UPD_CTRL2
ERR_UPD_AREA2	DMM_PAT_IRQSTATUS[20] ERR_UPD_AREA2 DMM_PAT_IRQSTATUS_RAW[20] ERR_UPD_AREA2	DMM_PAT_IRQENABLE_SET[20] ERR_UPD_AREA2 DMM_PAT_IRQENABLE_CLR[20] ERR_UPD_AREA2
ERR_INV_DATA2	DMM_PAT_IRQSTATUS[19] ERR_INV_DATA2 DMM_PAT_IRQSTATUS_RAW[19] ERR_INV_DATA2	DMM_PAT_IRQENABLE_SET[19] ERR_INV_DATA2 DMM_PAT_IRQENABLE_CLR[19] ERR_INV_DATA2
ERR_INV_DSC2	DMM_PAT_IRQSTATUS[18] ERR_INV_DSC2 DMM_PAT_IRQSTATUS_RAW[18] ERR_INV_DSC2	DMM_PAT_IRQENABLE_SET[18] ERR_INV_DSC2 DMM_PAT_IRQENABLE_CLR[18] ERR_INV_DSC2
FILL_LST2	DMM_PAT_IRQSTATUS[17] FILL_LST2 DMM_PAT_IRQSTATUS_RAW[17] FILL_LST2	DMM_PAT_IRQENABLE_SET[17] FILL_LST2 DMM_PAT_IRQENABLE_CLR[17] FILL_LST2
FILL_DSC2	DMM_PAT_IRQSTATUS[16] FILL_DSC2 DMM_PAT_IRQSTATUS_RAW[16] FILL_DSC2	DMM_PAT_IRQENABLE_SET[16] FILL_DSC2 DMM_PAT_IRQENABLE_CLR[16] FILL_DSC2
ERR_LUT_MISS1	DMM_PAT_IRQSTATUS[15] ERR_LUT_MISS1 DMM_PAT_IRQSTATUS_RAW[15] ERR_LUT_MISS1	DMM_PAT_IRQENABLE_SET[15] ERR_LUT_MISS1 DMM_PAT_IRQENABLE_CLR[15] ERR_LUT_MISS1
ERR_UPD_DATA1	DMM_PAT_IRQSTATUS[14] ERR_UPD_DATA1 DMM_PAT_IRQSTATUS_RAW[14] ERR_UPD_DATA1	DMM_PAT_IRQENABLE_SET[14] ERR_UPD_DATA1 DMM_PAT_IRQENABLE_CLR[14] ERR_UPD_DATA1
ERR_UPD_CTRL1	DMM_PAT_IRQSTATUS[13] ERR_UPD_CTRL1 DMM_PAT_IRQSTATUS_RAW[13] ERR_UPD_CTRL1	DMM_PAT_IRQENABLE_SET[13] ERR_UPD_CTRL1 DMM_PAT_IRQENABLE_CLR[13] ERR_UPD_CTRL1

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Table 15-8. Events (continued)

Interrupt	Event Flag	Event Mask
ERR_UPD_AREA1	DMM_PAT_IRQSTATUS[12] ERR_UPD_AREA1 DMM_PAT_IRQSTATUS_RAW[12] ERR_UPD_AREA1	DMM_PAT_IRQENABLE_SET[12] ERR_UPD_AREA1 DMM_PAT_IRQENABLE_CLR[12] ERR_UPD_AREA1
ERR_INV_DATA1	DMM_PAT_IRQSTATUS[11] ERR_INV_DATA1 DMM_PAT_IRQSTATUS_RAW[11] ERR_INV_DATA1	DMM_PAT_IRQENABLE_SET[11] ERR_INV_DATA1 DMM_PAT_IRQENABLE_CLR[11] ERR_INV_DATA1
ERR_INV_DSC1	DMM_PAT_IRQSTATUS[10] ERR_INV_DSC1 DMM_PAT_IRQSTATUS_RAW[10] ERR_INV_DSC1	DMM_PAT_IRQENABLE_SET[10] ERR_INV_DSC1 DMM_PAT_IRQENABLE_CLR[10] ERR_INV_DSC1
FILL_LST1	DMM_PAT_IRQSTATUS[9] FILL_LST1 DMM_PAT_IRQSTATUS_RAW[9] FILL_LST1	DMM_PAT_IRQENABLE_SET[9] FILL_LST1 DMM_PAT_IRQENABLE_CLR[9] FILL_LST1
FILL_DSC1	DMM_PAT_IRQSTATUS[8] FILL_DSC1 DMM_PAT_IRQSTATUS_RAW[8] FILL_DSC1	DMM_PAT_IRQENABLE_SET[8] FILL_DSC1 DMM_PAT_IRQENABLE_CLR[8] FILL_DSC1
ERR_LUT_MISS0	DMM_PAT_IRQSTATUS[7] ERR_LUT_MISS0 DMM_PAT_IRQSTATUS_RAW[7] ERR_LUT_MISS0	DMM_PAT_IRQENABLE_SET[7] ERR_LUT_MISS0 DMM_PAT_IRQENABLE_CLR[7] ERR_LUT_MISS0
ERR_UPD_DATA0	DMM_PAT_IRQSTATUS[6] ERR_UPD_DATA0 DMM_PAT_IRQSTATUS_RAW[6] ERR_UPD_DATA0	DMM_PAT_IRQENABLE_SET[6] ERR_UPD_DATA0 DMM_PAT_IRQENABLE_CLR[6] ERR_UPD_DATA0
ERR_UPD_CTRL0	DMM_PAT_IRQSTATUS[5] ERR_UPD_CTRL0 DMM_PAT_IRQSTATUS_RAW[5] ERR_UPD_CTRL0	DMM_PAT_IRQENABLE_SET[5] ERR_UPD_CTRL0 DMM_PAT_IRQENABLE_CLR[5] ERR_UPD_CTRL0
ERR_UPD_AREA0	DMM_PAT_IRQSTATUS[4] ERR_UPD_AREA0 DMM_PAT_IRQSTATUS_RAW[4] ERR_UPD_AREA0	DMM_PAT_IRQENABLE_SET[4] ERR_UPD_AREA0 DMM_PAT_IRQENABLE_CLR[4] ERR_UPD_AREA0
ERR_INV_DATA0	DMM_PAT_IRQSTATUS[3] ERR_INV_DATA0 DMM_PAT_IRQSTATUS_RAW[3] ERR_INV_DATA0	DMM_PAT_IRQENABLE_SET[3] ERR_INV_DATA0 DMM_PAT_IRQENABLE_CLR[3] ERR_INV_DATA0
ERR_INV_DSC0	DMM_PAT_IRQSTATUS[2] ERR_INV_DSC0 DMM_PAT_IRQSTATUS_RAW[2] ERR_INV_DSC0	DMM_PAT_IRQENABLE_SET[2] ERR_INV_DSC0 DMM_PAT_IRQENABLE_CLR[2] ERR_INV_DSC0
FILL_LST0	DMM_PAT_IRQSTATUS[1] FILL_LST0 DMM_PAT_IRQSTATUS_RAW[1] FILL_LST0	DMM_PAT_IRQENABLE_SET[1] FILL_LST0 DMM_PAT_IRQENABLE_CLR[1] FILL_LST0
FILL_DSC0	DMM_PAT_IRQSTATUS[0] FILL_DSC0 DMM_PAT_IRQSTATUS_RAW[0] FILL_DSC0	DMM_PAT_IRQENABLE_SET[0] FILL_DSC0 DMM_PAT_IRQENABLE_CLR[0] FILL_DSC0

15.2.3.5 DMM

15.2.3.5.1 DMM Concepts

The DMM introduces the concepts of dynamic mapping and DMM atomic units.

15.2.3.5.1.1 Dynamic Mapping

The DMM manages its internal memory space as an ordered set of up to four sections. Figure 15-5 shows the DMM sections and memory mapping.

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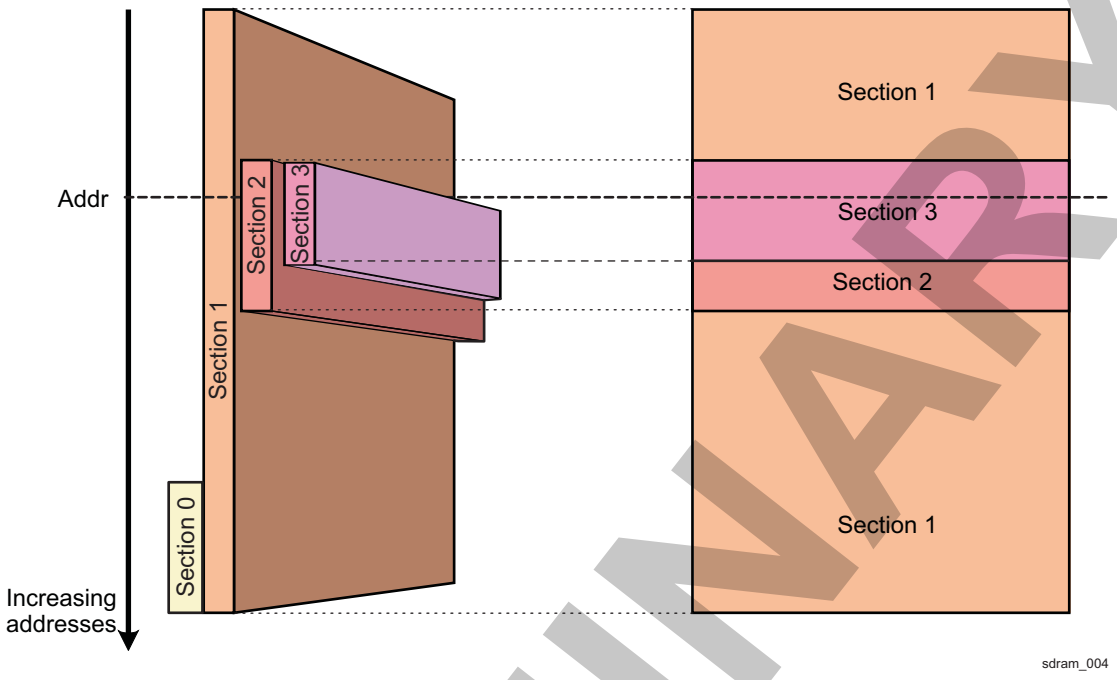
Figure 15-5. DMM Sections and Memory Mapping



In the DMM, a section is:

- A segment of 16MiB to 2GiB, which is power-of-two in size and aligned to that size in the system map
- An area with a constant interleaving scheme: constant interleaving granularity on a constant set of SDRC (EMIF) targets
- Given a priority equal to its index: the higher the index, the higher the priority

NOTE: Whenever a request hits more than one DMM section, it follows the interleaving scheme of the section having the highest index.

The interleaving configuration of the DMM, its section-based dynamic memory mapping, is shown on the right in Figure 15-5. In this example, a request at the system address Addr follows the interleaving scheme of section 3, although it hits sections 1, 2, and 3. Similarly, the DMM configuration given in this example prevents any request from using the interleaving scheme of section 0, because section 0 is fully masked by section 1, which has a higher priority.

Each of the four sections is configured through a DMM_LISA_MAP_i register, where i = 0 to 3.

NOTE: The DMM and SDRC registers (and EMIF registers; see Section 15.3.1, *EMIF Controller*) are declared in two extra static DMM sections of the highest priority so that they cannot be masked by any standard programmable DMM section.

NOTE: The DMM atomic size is:

- 1KiB in noninterleaved sections
- Equal to the interleaving granularity (128, 256, or 512 bytes) in interleaved sections

15.2.3.5.1.2 Address Mapping

The address mapping inside the DMM is configurable through up to four sections. A DMM section description fits in a single register (DMM_LISA_MAP_i). Each section is defined based on:

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- Its system address: The base address of the decoding range for the section
- Its size: The encoding is the number of bits used in the upper 8 bits of the incoming system address
- Its physical address: The base address of the memory range access in the external memory controller
- Its address space: The address space used on the external memory controller (for the DMM) when hitting this section. For details, see , *Local Interface*.
- The target memory controller. A section may hit a single or pair of controllers.
- Its interleaving definition

The address decoding is priority-based. In case of overlapping sections, only the highest-order one is hit. Register memory spaces have priority over regular memory sections. In case of four sections, the priority order is therefore:

1. Registers
2. DMM_LISA_MAP_3
3. DMM_LISA_MAP_2
4. DMM_LISA_MAP_1
5. DMM_LISA_MAP_0

All register-related addresses are reserved and fixed in the overall address mapping:

- DMM registers: 0x4E00_0000 to 0x4FFF_FFFF
- EMIF1 registers: 0x4C00_0000 to 0x4CFF_FFFF
- EMIF2 registers: 0x4D00_0000 to 0x4DFF_FFFF

There is no overlapping between register sections.

NOTE: Section decoding happens after PAT address translation in the case of TILER. In non-bypass mode, the system address considered for TILER accesses is the virtual address computed based on the PAT translation tables.

The DMM_LISA_LOCK register is used to lock the configuration once set. If written to 1, the LOCK bit prevents further writes to all DMM_LISA_MAP_i registers. The LOCK bit cannot be written back to 0. A reset is required to reprogram the sections.

15.2.3.5.1.3 Address Translation

The PAT engine of the DMM is composed of a 32-k entry physical address translation vector table and one or two refill engines. The refill engine is a specialized DMA for refilling the content of the PAT table.

The address translation mechanism is available only when the incoming request hits a page mode or tiled mode container; that is, when the incoming address targets the TILER or its aliased view in the system addressing space. Otherwise, the PAT logic is bypassed so that the resulting physical address corresponds to the input address.

The PAT engine supports multiple address translation schemes, called views, which can be bound to one or more initiators through a view mapping mechanism.

15.2.3.5.1.3.1 PAT View Mappings

The PAT engine can have up to 16 groups of initiators that share a set of four PAT views. The connection from an initiator to a PAT view is made through the DMM_PAT_VIEW register. Given that each PAT view index is coded on 4 bits, the DMM_PAT_VIEW register is a 64-bit register split into two 32-bit registers (DMM_PAT_VIEW0 for the first eight PAT view indexes and DMM_PAT_VIEW1 for the last eight PAT view indexes.

The PAT view index that corresponds to the initiator having the value i as the 4 most-significant bits (MSBs) of its L3 ConnID uses the view referenced in entry i of the DMM_PAT_VIEW. For example, the initiator 0xC7 uses the thirteenth view index of the DMM_PAT_VIEW register, the fifth view index in the DMM_PAT_VIEW1 register.

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The PAT view index of the initiator i is found in the Vi field. The Wi field is aimed at writing the corresponding Vi. When writing to the DMM_PAT_VIEW registers, the only Vi view indexes that are updated are those having their corresponding Wi bit, and byte enable, set. The Wi bits are always read as 0. For instance, to set the PAT view indexes V3 and V7 to 2 and 1, respectively, the DMM_PAT_VIEW0 register must be written with 5000 6000h.

15.2.3.5.1.3.2 PAT View Map Base Address

The PAT view map base address defines the base address of all PAT translated addresses.

Bit [31] of all PAT translated addresses is set to BASE_ADDR. For example, if the DMM_PAT_VIEW_MAP_BASE register is set to 8000 0000h, all PAT translated addresses will have bit [31] set to 1 so that the translated addresses range from 8000 0000h to FFFF FFFFh. All reserved bits of this DMM PAT base address register are read to 0.

15.2.3.5.1.3.3 PAT Views

A PAT view defines the kind of physical address translation to perform for each mode accesses (page, 8-bit, 16-bit and 32-bit). Each mode of each PAT view can be configured to use a container-grained translation or page-mode translation.

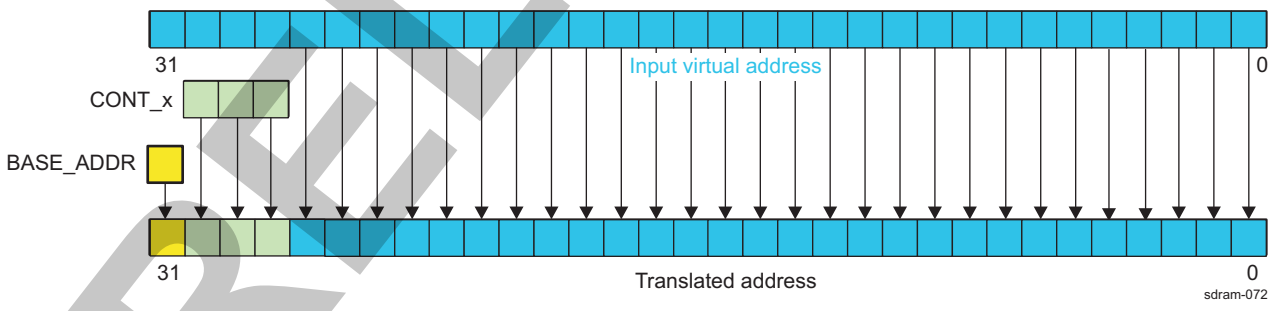
15.2.3.5.1.3.3.1 PAT Direct Access Translation

The container-grained translation is named the direct access. In this mode, the translation vector is given directly by the CONT_x bit field that corresponds to the accessed mode.

- A page mode access uses the vector contained in the DMM_PAT_VIEW_MAP_i[26:24] CONT_PAGE bit field concatenated with 1 (bit 27 of translated address).
- A 32-bit mode access uses the vector contained in the DMM_PAT_VIEW_MAP_i[18:16] CONT_32 bit field concatenated with 0 (bit 27 of translated address).
- A 16-bit mode access uses the vector contained in the DMM_PAT_VIEW_MAP_i[10:8] CONT_16 bit field concatenated with 0 (bit 27 of translated address).
- An 8-bit mode access uses the vector contained in the DMM_PAT_VIEW_MAP_i[2:0] CONT_8 bit field concatenated with 0 (bit 27 of translated address).

Figure 15-6, *PAT Direct Access Translation* describes PAT direct access translation .

Figure 15-6. PAT Direct Access Translation



15.2.3.5.1.3.3.2 PAT Indirect Access Translation

The page-grained translation is named the indirect access. In this mode the translation vector is found in the internal 32-k entry physical address translation vector table at the index given by bits [26:12] of the input virtual address, and the DMM_PAT_VIEW_MAP_i CONT_x bit field references the internal physical address translation table to use. Because the DMM uses only one such table, in this mode the CONT_x bit field must be written as 0. See Figure 15-7.

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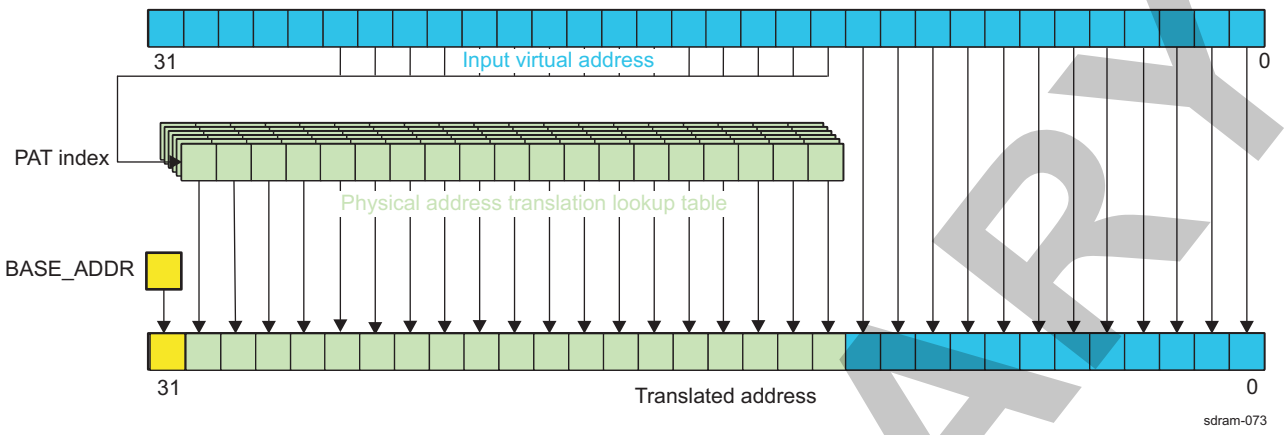
Figure 15-7. PAT Indirect Access Translation



Each entry of the PAT lookup table (LUT) is a 19-bit vector that replaces bits [30:12] of the input virtual address. The PAT index aimed at selecting the vector in the table consists of bits [26:12] of the input virtual address.

The mode associated to the transaction is used to define if the upper or lower half of the LUT is effectively used:

- If the mode is 8-, 16- or 32-bit, the lower part of the LUT (indexes 0x0000 to 0x7FFF; that is, lines 0 to 127) is used.
- If the mode is page, the upper part of the LUT (indexes 0x8000 to 0xFFFF; that is, ines 128 to 256) is used.

This means the PAT index used is the concatenation of 0 and address bits 12 to 26 in 8-, 16- or 32-bit mode, and the concatenation of 1 and address bits 12 to 26 in page mode.

Using different LUT indexes depending on the mode enables the user to define a larger tiled space, with the constraint that half of the space can be used only in 8-, 16- or 32-bit mode and the other half only in page mode. If the user wishes to preserve software compatibility with the case CONT_HGHT = 128, it is required to mirror the configuration for the lower half of the LUT on the upper half of the LUT. In that way, all views see the same address decoding through PAT.

15.2.3.5.1.3.3.3 PAT View Configuration

There are four different views in a DMM, each with its own DMM_PAT_VIEW_MAP_i register for defining the kind of address translation to perform.

The PAT view type of each mode is selected by the ACCESS_x bit field in the DMM_PAT_VIEW_MAP_i register, i being the index of the considered view. When this field is set to 1, the indirect access scheme is used; otherwise, the PAT performs the address translation in a direct way with the corresponding CONT_x vector.

When configuring a mode in a view to use the indirect access, the corresponding CONT_x bit field must be filled with 0.

15.2.3.5.1.3.3.4 PAT Address Translation LUT

The PAT LUT does not have the same geometry as the DMM container. The PAT LUT has 256 lines of 256 entries of 19 bits each. The geometry of the DMM container is 256 × 128 entries.

- The lower 128MiB are restricted for use with 8-, 16-, and 32-bit modes.
- The upper 128MiB are restricted for use with page mode.

See Figure 15-8.

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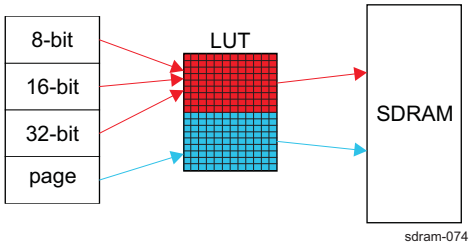
Figure 15-8. Physical Address Translation Table



15.2.3.5.1.3.3.5 Direct Access to the PAT Table Vectors

The PAT table is typically refilled with specialized DMA called refill engines. Some direct read and write access to the content of this table is granted when disabling the use of one or the other refill engine by writing 1 in the MODEi field of the DMM_PAT_CONFIG register that corresponds to the refill engine i to disable.

In this mode, often called the debug mode, the data read in or written to the DMM_PAT_DATA_i register corresponds to the vector in the PAT table, whose index is in the X0 and Y0 fields of the DMM_PAT_AREA_i register.

15.2.3.5.1.3.3.6 Automatic Refill Through the Refill Engines

See Section 15.2.4.1, *PAT Use Cases*.

15.2.3.5.2 DMM Transaction Flows

15.2.3.5.2.1 Nontiled Transaction Flow

Each nontiled interconnect transaction that reaches the DMM on a TILER port is subject to the same processing.

The TILER blocks consider separated request, data, and response paths. An overview of each path follows and more detailed information is in Section 15.2.3.5.3, *DMM Internal Macro-Architecture*.

On the request path, the flow consists of:

- Allocating a TILER response context for the timely generation of the appropriate responses
- Splitting 2D requests in a collection of 1D requests – TILER ports
- Splitting requests at DMM unit boundaries; the split granularity is provided by the LISA mapping registers
- Allocating an available buffer in the appropriate ROBIN, for both read and write requests
- In case of a write request, allocating and updating a TILER write context to direct the incoming write data into the relevant reordering buffer
- Generating the initiator-indexed priority extension by use of the PEG block

On the write data path, the flow consists of forwarding incoming data to the relevant reordering buffer in accordance with the corresponding TILER write context.

On the response path, responses are returned when:

- At least one response has entered each related buffer, in case of read requests.
- All related responses have returned from the SDRC, in case of write requests.
- No other previous pending response with the same tag exists.

15.2.3.5.2.2 Tiled Transaction Flow

Similarly, each tiled interconnect transaction that reaches the DMM is subject to the same processing.

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The TILER blocks consider separated request, data, and response paths. An overview of each path follows, and more detailed information is in Section 15.2.3.5.3, *DMM Internal Macro-Architecture*.

On the request path, the processing phase consists of:

- Decoding the address to qualify whether the request targets the TILER or the memory directly
- Transforming TILER-specific requests to their natural representation; the address, width, and height are modified accordingly

On the request path, the generation phase consists of:

- Allocating a TILER response context for the timely generation of the appropriate responses
- Splitting malformed: The request stride differs from the container stride and from the double of this container stride – tiled 2D requests in a collection of 1D requests
- Splitting tiled requests at tile boundaries
- Performing the page-based address translation by use of the PAT block
- Allocating an available buffer in the appropriate ROBIN, for read and write requests
- In case of a write request, allocating and updating a TILER write context to direct the incoming write data into the relevant reordering buffer
- Generating the initiator-indexed priority extension by use of the PEG block

On the data path, any incoming data is transformed in accordance with the corresponding TILER write context and sent to the appropriate reordering buffer.

On the response path, responses are returned when:

- A minimal number of responses have entered the corresponding buffers, in case of read requests.
- All related responses have returned from the SDRCs, in case of write requests.
- No other previous pending response with the same tag exists.

15.2.3.5.3 DMM Internal Macro-Architecture

This section describes the DMM internal macro-architecture, specifically:

- Input request decoding
- PAT and synchronized translation table reloading
- Output request and response generation
- Memory mapping in the system addressing space, including interleaving
- Tag management
- Priority handling
- Contexts
- Maximum allowed burst size
- Reconstruction buffer dimensioning

15.2.3.5.3.1 LISA Description

The LISA is a full crossbar aimed at setting priorities, managing tags, and mapping memory.

The interconnect routes are:

- TILER requests on the ROBIN initiator nodes
- TILER write data on the ROBIN write buffers
- ROBIN read data to the relevant TILER initiators

The LISA block registers are DMM_LISA_MAP_i (where i = 0 to 3) and DMM_LISA_LOCK.

When two ROBINs are in use, the two ports are interleaved at a programmable boundary from 128 bytes or more (configurable with the DMM_LISA_MAP_i[19:18] SDRC_INTL bit field).

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15.2.3.5.3.2 PAT Description

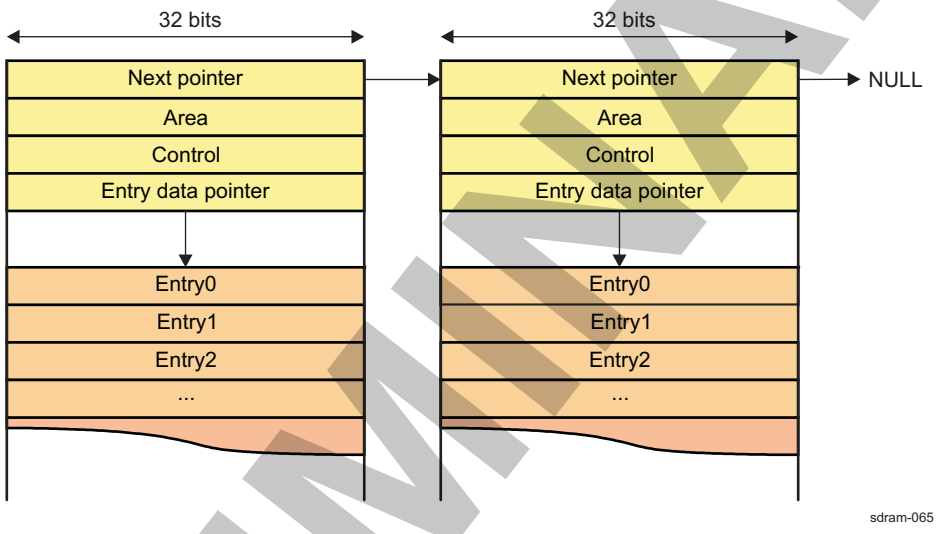
The PAT block maps physical pages to each TILER container page. The internal address translation memories used in the PAT block are designed with RFFs. It consists of:

- A memory-based LUT which has the same geometry as the container pages
- A refill engine for modifying entries in a given area of the internal LUT

A PAT descriptor is a singly-linked list node (see Figure 15-9) that contains:

- A description of the LUT area to reload
- A description of how to reload the defined LUT area
- A pointer to the location where the corresponding LUT entries are stored

Figure 15-9. PAT Descriptors



PAT descriptors are chained and processed until a NULL pointer is encountered. The PAT bank allocation scheme allows the updating of four consecutive entries of a line in a single cycle regardless of the refilling orientation.

The PAT descriptor structure directly maps the following registers (where i = 0 to 3):

- DMM_PAT_DESCR_i
- DMM_PAT_AREA_i
- DMM_PAT_CTRL_i
- DMM_PAT_DATA_i

The PAT refill engine can be started either of the following:

- Filling manually all the necessary registers:
  - DMM_PAT_AREA_i with the (x0, y0) (x1, y1) area definition
  - DMM_PAT_DATA_i with the physical address of the corresponding area entry table
  - DMM_PAT_CTRL_i[6:4] DIRECTION bit field with the relevant (S, Y, X) direction of the area refill
  - DMM_PAT_CTRL_i[0] START bit with 1
- Writing the physical address of a memory-mapped PAT descriptor in DMM_PAT_DESCR_i register, which updates:
  - DMM_PAT_AREA_i with the area value of the descriptor
  - DMM_PAT_DATA_i with the data value of the descriptor
  - DMM_PAT_CTRL_i with the control value of the descriptor
  - DMM_PAT_DESCR_i with the next value of the descriptor

The data part of the PAT refill starts only when the DMM_PAT_CTRL_i[0] START bit is asserted.

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The DMM_PAT_STATUS_i register can be used to determine whether the process has completed without errors.

15.2.3.5.3.3 PEG Description

The PEG is a dynamic software-programmable, initiator-indexed table of priorities. Its unique role is to bind a priority to an initiator on the fly. The mapping of each initiator to the table (split into eight registers) is based on its 6-MSB group ConnID (see Section 14.2.3.2.3, *Master NIU Identification*, in Chapter 14, *Interconnect*).

When an interconnect request enters the DMM, its priority is extracted from the PEG LUT.

The 64 priority entries are software-programmable with the DMM_PEG_PRIO_k register. A priority of 0 defines the highest priority and a priority of 7 defines the lowest priority. At reset, all priorities are set to 4.

These registers are each split into eight 4-bit fields, each field mapping an entry of the LUT with:

- The 3-bit priority coded on the 3 least-significant bits (LSBs): P field
- A $\overline{W}$ field-specific active-low local write enable bit, always read as 0, on the MSB. The role of the $\overline{W}$ bit is to allow the modification of a single entry without requiring a read-modify-write sequence. Because its $\overline{W}$ bits are always read as 0, writing back the modified register updates all priority fields of the register.

Table 15-9 lists the initiator ConnIDs that are mapped to PEG priority register fields (P/W).

Table 15-9. ConnIDs vs PEG Priority Register Fields

Registers	P0/W0	P1/W1	P2/W2	P3/W3	P4/W4	P5/W5	P6/W6	P7/W7
DMM_PEG_PRIO_0	0	1	2	3	4	5	6	7
DMM_PEG_PRIO_1	8	9	10(0xA)	11(0xB)	12(0xC)	13(0xD)	14(0xE)	15(0xF)
DMM_PEG_PRIO_2	16(0x10)	17(0x11)	18(0x12)	19(0x13)	20(0x14)	21(0x15)	22(0x16)	23(0x17)
DMM_PEG_PRIO_3	24(0x18)	25(0x19)	26(0x1A)	27(0x1B)	28(0x1C)	29(0x1D)	30(0x1E)	31(0x1F)
DMM_PEG_PRIO_4	32(0x20)	33(0x21)	34(0x22)	35(0x23)	36(0x24)	37(0x25)	38(0x26)	39(0x27)
DMM_PEG_PRIO_5	40(0x28)	41(0x29)	42(0x2A)	43(0x2B)	44(0x2C)	45(0x2D)	46(0x2E)	47(0x2F)
DMM_PEG_PRIO_6	48(0x30)	49(0x31)	50(0x32)	51(0x33)	52(0x34)	53(0x35)	54(0x36)	55(0x37)
DMM_PEG_PRIO_7	56(0x38)	57(0x39)	58(0x3A)	59(0x3B)	60(0x3C)	61(0x3D)	62(0x3E)	63(0x3F)

Although this priority information is generated before entering the LISA block, it is not used internally in the local interconnect arbitration but is forwarded to the EMIF as MReqInfo, where it indicates the command priority.

It is also possible to give a priority for the internal PAT engine through the DMM_PEG_PRIO_PAT register.

15.2.3.5.3.4 LISA Interconnect Arbitration

When Mflag[i][63:0] ≠ 0 is signaled at TILERi or both TILERs, the transactions of TILERi or both TILERs form an additional new group called the high priority group. Within this group, reads and writes are sorted and arbitrated the same way as in the normal priority group. Arbitration between transactions out of the high priority group and out of the normal priority group is based on a weighted round-robin algorithm. Weight is software selectable using the DMM_EMERGENCY[20:16] WEIGHT bit field. Weight selection is considered static (that is, behavior is undefined when software changes the weight, and DMM is not empty of transaction).

The counter that is implemented to support the weighted round-robin is enabled as long as emergency signaling is present. The counter increments by one each time a command (from the normal or the high priority group) is pushed to ROBIN. The counter wraps on DMM_EMERGENCY[20:16] WEIGHT value. One command from the normal priority group is serviced in any of the following scenarios:

- The counter is enabled and wraps.
- The counter is enabled, has not reached its wrap value, and no command is queued in the high priority group (a case where one device module is signaling emergency but its requests have not yet reached

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the TILERs).

- The counter is disabled.

Setting the DMM_EMERGENCY[0] ENABLE bit to 1 enables the emergency arbitration scheme.

NOTE: It is recommended to set the DMM_EMERGENCY[0] ENABLE bit to 1, and the DMM_EMERGENCY[20:16] WEIGHT bit to 0x8. This provides better and faster recovery behavior, and benefits system performance.

15.2.3.5.3.5 ROBIN Description

The ROBIN is a block that provides some working buffering for converting data and responses to-and-from between raster and tiled organizations, and a master port to connect to the EMIF.

The ROBIN block:

- Forwards requests
- Writes data and buffers responses
- Keeps write data ordering
- Performs intraword tiling and orientation transforms
- Handles tags

15.2.3.5.3.6 TILER Description

The main function of the TILER is request conversion caused by tiling.

The TILER block:

- Decodes the address to qualify whether the request targets the TILER or the memory directly
- Converts TILER-specific requests to their natural representation; address, width, and height are modified accordingly
- Allocates an internal response context for the timely generation of appropriate responses
- Splits tiled requests at tile boundaries and not-tiled requests at DMM atomic section boundaries
- Requests the page-based address translation
- Requests buffer allocation in the appropriate ROBIN
- In case of a write request, allocates and updates an internal write context to direct the incoming write data into the relevant reordering buffer

The interdependent tilingand isometric transform concepts introduced in the TILER are described in the following section.

15.2.3.6 TILER

15.2.3.6.1 TILER Concepts

This section describes the concepts behind the TILER transforms, through a top-down approach starting from the main object container.

15.2.3.6.1.1 TILER Rationale

This section is a synthesis of all TILER concepts, giving one rule per TILER structure level.

Figure 15-10 shows the TILER address space structure for tiled modes.

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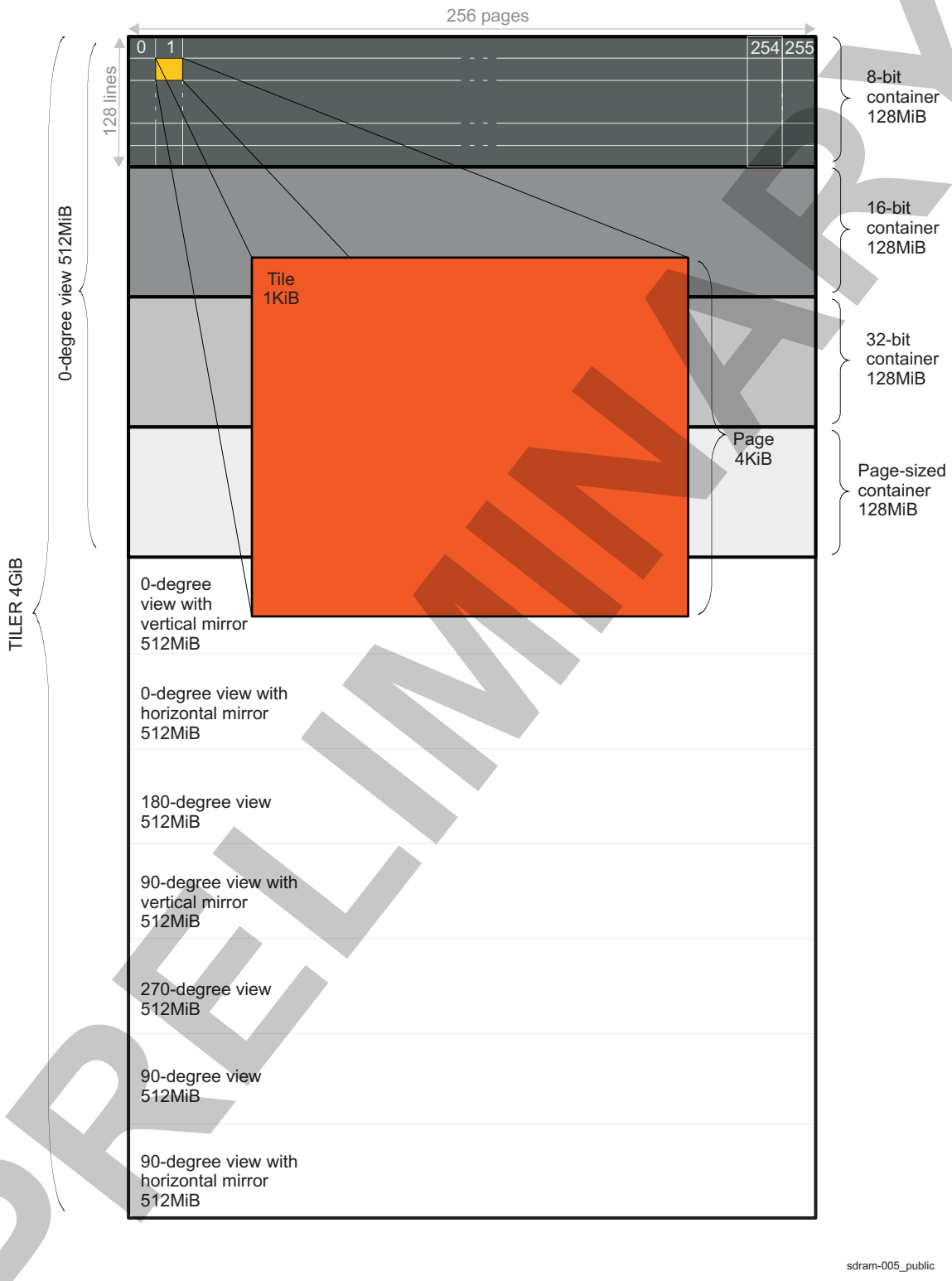
Figure 15-10. TILER Address Space Structure for Tiled Modes



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15.2.3.6.1.1.1 The TILER is a 4-GiB Virtual Address Space Composed of Eight Views

There is one view for each of the eight possible ways of scanning a frame-buffer:

- From left to right and then from top to bottom

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- From right to left and then from top to bottom
- From left to right and then from bottom to top
- From right to left and then from bottom to top
- From top to bottom and then from left to right
- From top to bottom and then from right to left
- From bottom to top and then from left to right
- From bottom to top and then from right to left

15.2.3.6.1.1.2 A View is a 512-MiB Virtual Address Space Composed of Four Containers

There is one container per element size to allow correct access patterns in any of the eight possible orientations. The container is the entity where all objects of a given element type are allocated.

The element is the entity of maximum size (8, 16, 32 bits, or page-sized), which is invariant in any orientation.

15.2.3.6.1.1.3 A Container is a 128-MiB Virtual Address Space

A container is composed of an array of 128 lines of 256 pages of 4kiB each.

The page defines the granularity of physical memory allocation through a PAT unit – MMU.

15.2.3.6.1.1.4 A Page is a 4-kiB Virtual Address Space

A page is composed of two lines. Each line consists of two tiles.

15.2.3.6.1.1.5 A Tile is a 1-kiB Address Space

The tile is designed to offer bidimensional data locality in a single SDRAM page. In this respect, it is sized to 1kiB; that is, to the size of the smallest SDRAM page.

15.2.3.6.1.2 TILER Modes

The TILER supports three major modes, bypass, page, and tiled. Each mode has a specific output request generation.

15.2.3.6.1.2.1 Bypass Mode

This mode is transparent from the TILER perspective. However, from the DMM perspective:

- 2D block bursts are broken down on a line basis in a set of incremental bursts.
- Incremental bursts, including those issued by a 2D block burst breakdown, are split at the DMM atomic unit of the section hit by the burst at:
  - The interleaving granularity of the section (128, 256, or 512 bytes) in interleaved sections
  - 1-kiB boundary in noninterleaved sections

15.2.3.6.1.2.2 Page Mode

This mode uses the DMM address translation mechanism for nontiled accesses. In this respect it is similar to bypass mode:

- 2D block bursts are broken down on a line basis in a set of incremental bursts.
- Incremental bursts, including those issued by a 2D block burst breakdown, are split at:
  - The interleaving granularity of the section (128, 256, or 512 bytes) in interleaved sections
  - 1-kiB boundary in noninterleaved sections

15.2.3.6.1.2.3 Tiled Mode

Tiled mode has two major breakdown algorithms:

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- One for well-formed 2D block requests that conform to the orientation, mode, and stride listed in Table 15-10
- One for 1D incremental requests and ill-formed 2D block requests

Table 15-10. Well-Formed Tiled Mode 2D Block Requests

Orientation			Mode		Stride	Description
S	$\overline{Y}$	$\overline{X}$	M1	M0	(bytes)	
0	x	x	0	0	16,384	Plain access to an 8-bit progressive frame in 0 or 180 degrees
					32,768	Field access to an 8-bit interlaced frame 0 or 180 degrees
			0	1	32,768	Plain access to a 16-bit progressive frame in 0 or 180 degrees
					65,536	Field access to a 16-bit interlaced frame 0 or 180 degrees
			1	0	32,768	Plain access to a 32-bit progressive frame in 0 or 180 degrees
					65,536	Field access to a 32-bit interlaced frame 0 or 180 degrees
1	x	x	0	0	8192	Plain access to an 8-bit progressive frame in 90 or 270 degrees
					16,384	Field access to an 8-bit interlaced frame 90 or 270 degrees
			0	1	8192	Plain access to a 16-bit progressive frame in 90 or 270 degrees
					16,384	Field access to a 16-bit interlaced frame 90 or 270 degrees
			1	0	16,384	Plain access to a 32-bit progressive frame in 90 or 270 degrees
					32,768	Field access to a 32-bit interlaced frame 90 or 270 degrees

Similar to the bypass and page modes, ill-formed 2D block requests are broken down on a line basis in a set of incremental bursts. In tiled mode, however, these incremental virtual bursts do not translate to 1D physical burst requests.

15.2.3.6.1.3 Object Container Definition

The object container is the unique addressable entry point of the TILER. It is a 128-MiB virtual address space, where all objects of a same kind and orientation are allocated.

Four main types of containers are present in the TILER, each referred by a mode:

- 8-bit element mode, for efficiently accessing bidimensional arrays of 8-bit data
- 16-bit element mode, for efficiently accessing bidimensional arrays of 16-bit data
- 32-bit element mode, for efficiently accessing bidimensional arrays of 32-bit data
- Page mode, for efficient 1D accesses

Figure 15-11 shows the TILER object containers and views.

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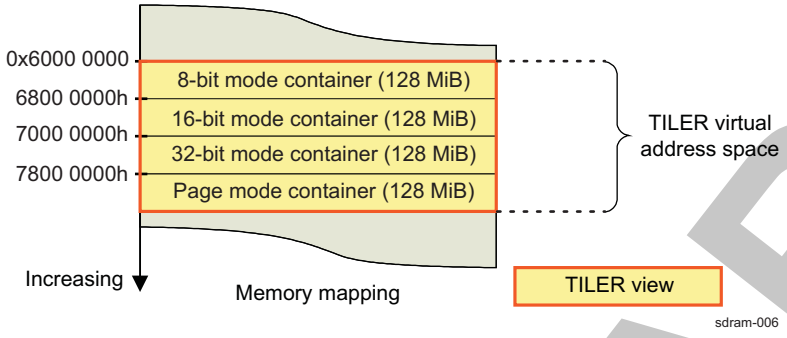
Figure 15-11. TILER Object Containers and Views

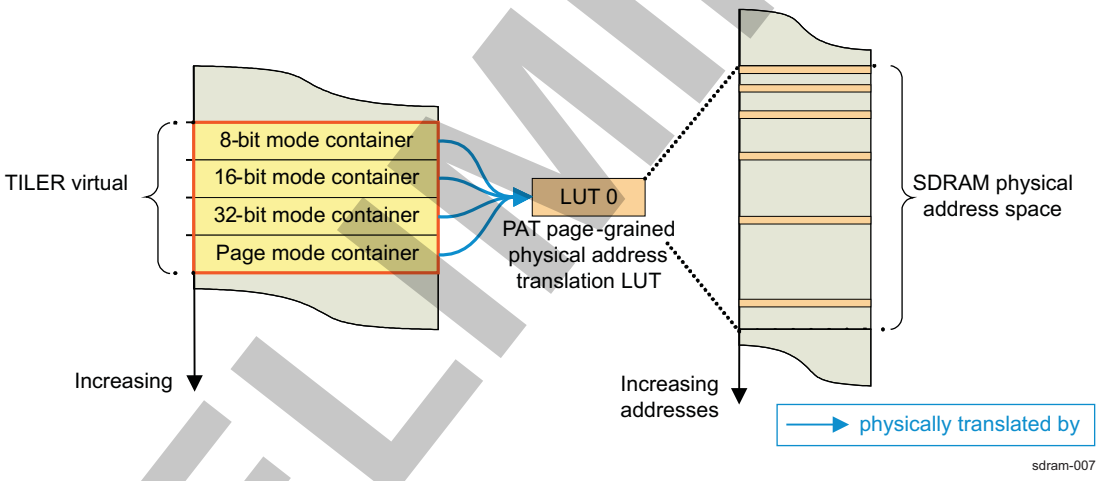


The 512-MiB virtual address space composed of four 128-MiB object containers of different modes is called a view. Because eight orientations are available per mode, the TILER actually manages 32 kinds of containers.

The physical memory footprint of a 512-MiB TILER view is directly subject to the nature of the PAT unit.

A unique PAT LUT is instantiated in the DMM. This table is shared by all TILER modes. Hence, each of the four modes cannot be given its own private page-grained PAT LUT. A maximum of 128MiB of objects among all TILER modes can be managed as shown in Figure 15-12.

Figure 15-12. TILER Memory Footprint With PAT and Shared Physical Address Translation LUT



Although each of the four modes has its own separate virtual 128-MiB object container, these containers are all mapped to the same piecewise 128-MiB physical address space, and are then not physically separated. Consequently, a memory-related system constraint is that no more than 128-MiB of objects can be available simultaneously in a TILER view.

NOTE: Software must ensure that any object allocated in a mode does not physically overlap with any other object, even in another mode.

15.2.3.6.1.4 Page Definition

A TILER page defines the granularity of object allocation in virtual TILER containers.

Because the subpage structure is mode-specific, the page is the smallest granularity common to all modes, making it the granularity to consider in the TILER resource manager for object allocation.

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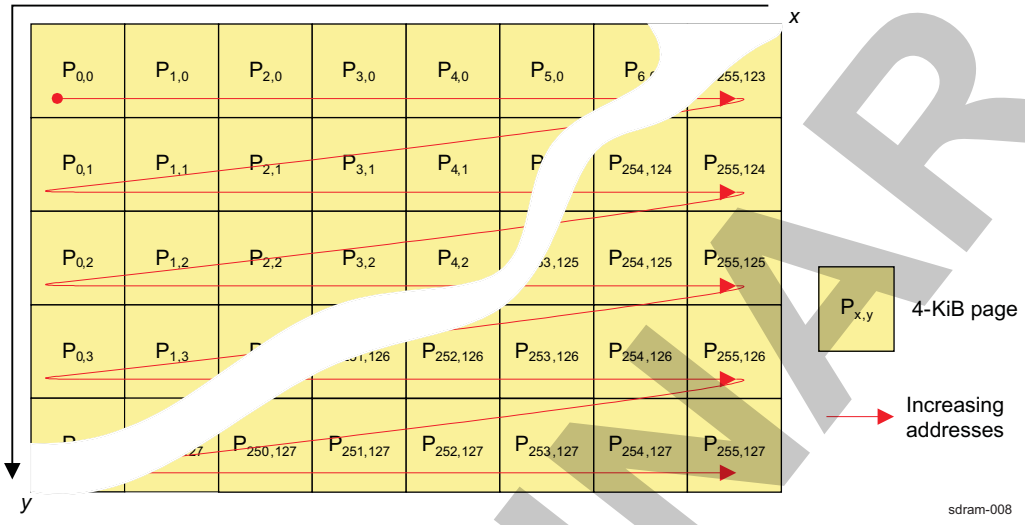
15.2.3.6.1.4.1 Container Geometry With 4-kiB Pages

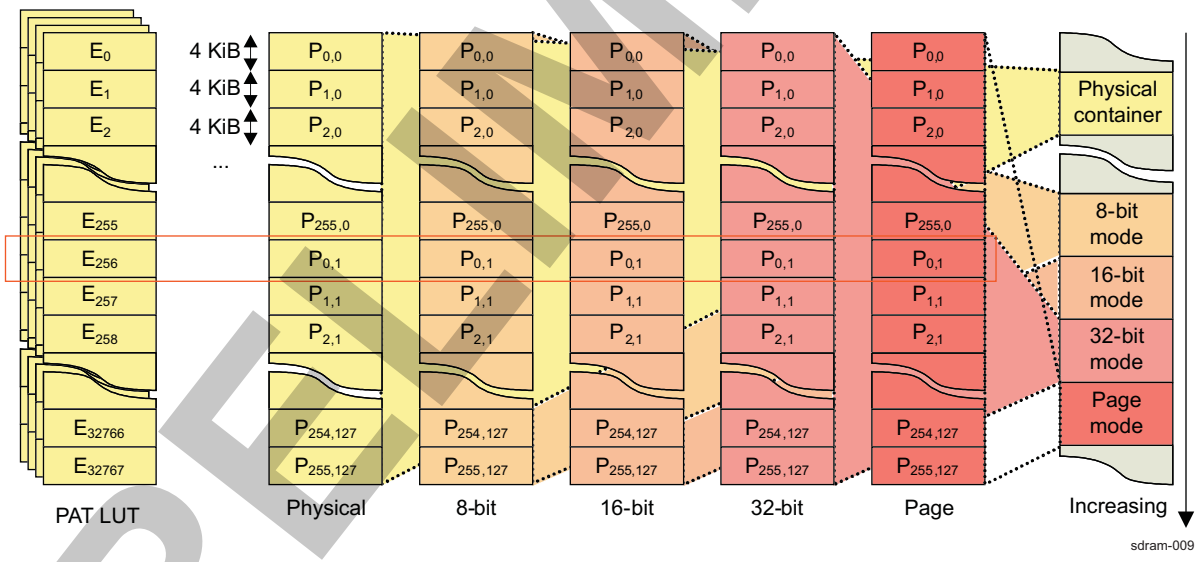
Because the size of the page is 4kiB, any 128-MiB object container is a set of 32,768 pages, organized in an array of 256 columns and 128 rows, as shown in Figure 15-13.

Figure 15-13. Object Container Geometry With 4-kiB Pages



This array of pages is mapped to the system address space, as shown in Figure 15-14.

Figure 15-14. TILER Page Mapping When Using 4-kiB Pages



In any 128-MiB object container, the 4-kiB page Px,y at column x (where 0 =< x < 256) and row y (where 0 =< y < 128), is found at an offset of 4096.(x+256.y) bytes from the base address of the related object container.

Similarly, the page Px,y at column x (where 0 =< x < 256) and row y (where 0 =< y < 128), is translated by the LUT entry Ex+256.y found at the index x+256.y.

15.2.3.6.1.4.2 Container Geometry and Page Mapping Summary

The TILER has a page size of 4096 bytes. The page $P_{x,y}$:

- Has max_x = 256 and max_y = 128
- Is found at an offset of 4096.(x + max_x.y) bytes from the base address of the related object container
- Is translated by the entry at the index (x + max_x.y) of the LUT

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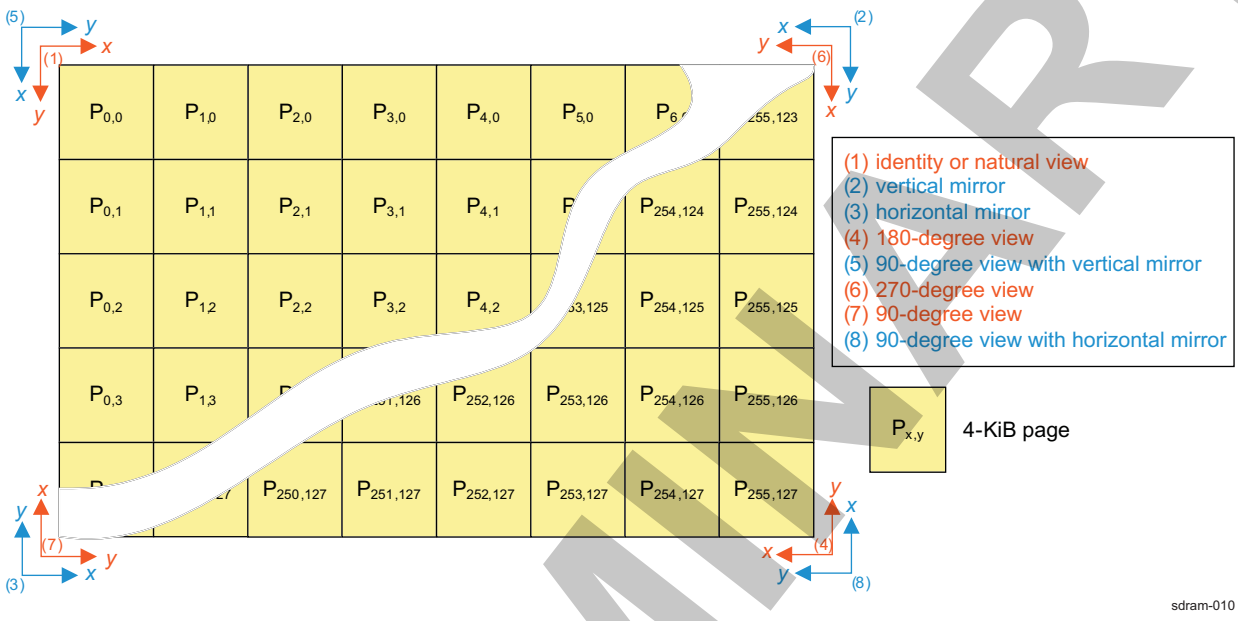
15.2.3.6.1.5 Orientation

This section describes the eight on-the-fly orientation-related isometric transforms, which correspond to all available changes of orthonormal basis in the bidimensional space of the TILER container.

Figure 15-15 shows isometric transforms in the TILER container

Figure 15-15. Isometric Transforms in the TILER Container



Mathematically speaking, all these transforms correspond to the composition of a 0-, 90-, 180-, or 270-degree rotation with an optional reflection. The nature of this orientation is based on the three following binary parameters:

- *X* to change the direction of the $_{x}$ axis of the TILER container
- *Y* to change the direction of the $_{y}$ axis of the TILER container
- *S* to swap the modified $_{x}$ and $_{y}$ axis

Hereafter in this document the term orientation refers to any composition of a "quadrant" rotation with an optional horizontal (flip-flop) or vertical mirroring.

15.2.3.6.1.6 Tile Definition

A tile is a subdivision of a page that is aimed at:

- Representing a 2D block to better balance accesses in both directions
- Ensuring that any tiled access that fits within a tile is made atomic in the SDRC and fits in a single SDRAM memory page
- Minimizing the number of SDRAM page openings per 2D block transfer

The tile is defined as a 1-kiB 2D block, and a 4-kiB page as an array of two lines of two tiles each.

When the considered page is in an interleaved DMM section, it is necessary that:

- The DMM memory interleaving size of tiled accesses is set to 1kiB (a tile size) so that any tiled request that fits within a tile, fits in a single SDRAM memory page.
- Any request that spans two or four tiles is distributed on a maximum number of SDRCs.

15.2.3.6.1.7 TILER Virtual Addressing

The TILER can be virtually accessed in four different modes: 8-, 16-, 32-bit, and page modes. Each mode defines the element granularity to apply isometric transforms, as summarized in Table 15-11.

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Table 15-11. Coding and Description of TILER Modes

Mode	Name	Granularity (Element Size)
0	8-bit tiled mode	8 bits
1	16-bit tiled mode	16 bits
2	32-bit tiled mode	32 bits
3	Page mode	4096 bytes

For instance, making a vertical mirror of a 16-byte horizontal line that contains the word 000102030405060708090A0B0C0D0E0Fh, leads to:

- 0F0E0D0C0B0A09080706050403020100h in 8-bit tiled mode
- 0E0F0C0D0A0B08090607040502030001h in 16-bit tiled mode
- 0C0D0E0F08090A0B0405060700010203h in 32-bit tiled mode
- 000102030405060708090A0B0C0D0E0Fh in page mode – unchanged because the element granularity is 4 KiB

Besides, because each of the eight orientations is available for any of the four modes, the TILER has 32 addressing possibilities (see Table 15-12).

Table 15-12. Coding and Description of TILER Orientations

S	$\overline{Y}$	$\overline{X}$	Description	Alternate description
0	0	0	0-degree view	Natural view
0	0	1	0-degree view with vertical mirror	180-degree view with horizontal mirror
0	1	0	0-degree view with horizontal mirror	180-degree view with vertical mirror
0	1	1	180-degree view	
1	0	0	90-degree view with vertical mirror	270-degree view with horizontal mirror
1	0	1	270-degree view	
1	1	0	90-degree view	
1	1	1	90-degree view with horizontal mirror	270-degree view with vertical mirror

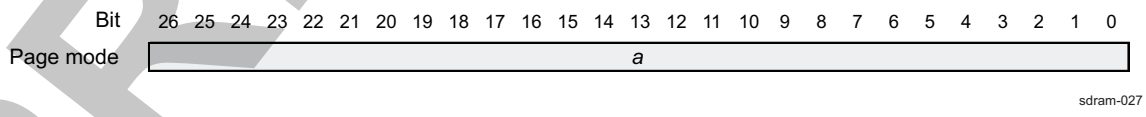
15.2.3.6.1.7.1 Page Mode Virtual Addressing and Characteristics

When used in page mode, the 128-MiB TILER space is seen as an orientation-specific sequence of 32,768 pages of 4kiB each. The access sequence inside a page is left unchanged.

Therefore, in page mode, the TILER is accessed similarly to any 128-MiB memory, with a 27-bit byte-based address.

NOTE: From here forward, the address is noted as *a* (see Figure 15-16).

Figure 15-16. Page Mode Virtual Addressing



15.2.3.6.1.7.2 Tiled Mode Virtual Addressing and Characteristics

When used in tiled mode, the 128-MiB TILER space is seen as a giant frame-buffer, the container. The addressing and characteristics of this giant frame-buffer depend on:

- The tiled mode, which defines the considered atomic element size
- The orientation, which potentially swaps its x and y axis, and hence the container geometry

Table 15-13 summarizes the container characteristics in tiled mode.

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Table 15-13. Tiled Mode Container Characteristics

Orientation			Element Size (Bits)	Width (Elements)	Height (Elements)	Stride (Bytes)	
S	$\bar{Y}$	$\bar{X}$				Progressive	Interlaced
0	x	x	8	16,384	8192	16,384	32,768
			16	16,384	4096	32,768	65,536
			32	8192	4096	32,768	65,536
1	x	x	8	8192	16,384	8192	16,384
			16	4096	16,384	8192	16,384
			32	4096	8192	16,384	32,768

As a result, the coordinate (x_0, y_0) of a pixel in an oriented view is translated in a virtual address, as shown in Figure 15-17 and Figure 15-18.

Figure 15-17. Tiled Mode Addressing in 0- or 180-Degree Orientation (S = 0)

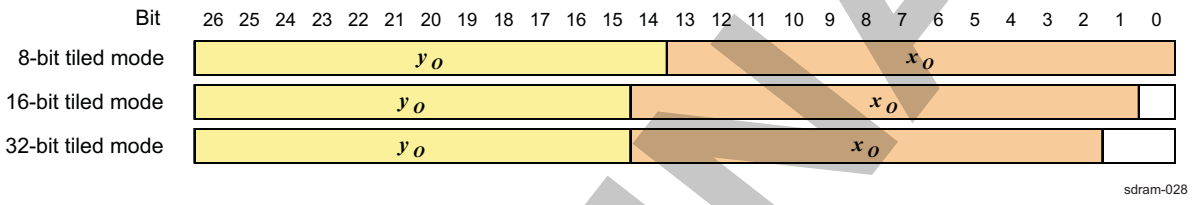
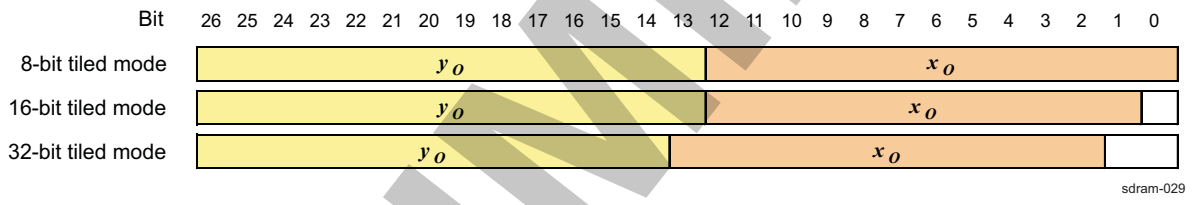


Figure 15-18. Tiled Mode Addressing in 90- or 270-Degree Orientation (S = 1)



15.2.3.6.1.7.3 Element Ordering in the TILER Container

This section describes how elements (8-, 16-, or 32-bit data or a 4-kiB page) are ordered in the container. In other words, this section describes how the path of incrementing virtual addresses is mapped in the container.

Regardless of the mode, and hence the element size, the sequence for ordering the elements in their related container is strictly similar and depends only on the related orientation. In other words:

- Mode is concerned with element granularity.
- Orientation is concerned with change of orthornormal basis for ordering the elements in the mode-specific container.

A corollary to the previous statements is that in a given mode the internal structure of an element is unchanged regardless of the orientation. In page mode for instance, the offset of a word inside a page is invariant by orientation; the content of a page is always accessed in the same manner.

In the following sections, the natural container orthonormal basis is referenced as:

$$(\vec{x}_N, \vec{y}_N)$$

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and the oriented orthonormal basis is referenced as:

$$(\vec{x}_O, \vec{y}_O)$$

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15.2.3.6.1.7.3.1 Natural View or 0-Degree View (Orientation 0)

This orientation defined by S = 0, $\overline{Y}$ = 0, and $\overline{X}$ = 0 means that the operated change of basis is:

$$\begin{cases} \vec{x}_O = \vec{x}_N \\ \vec{y}_O = \vec{y}_N \end{cases}$$

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In any TILER mode, the elements are ordered from left to right and then from top to bottom in their container, as shown in Figure 15-19 and Figure 15-20.

Figure 15-19. Tiled Mode Ordering of Elements in Natural View

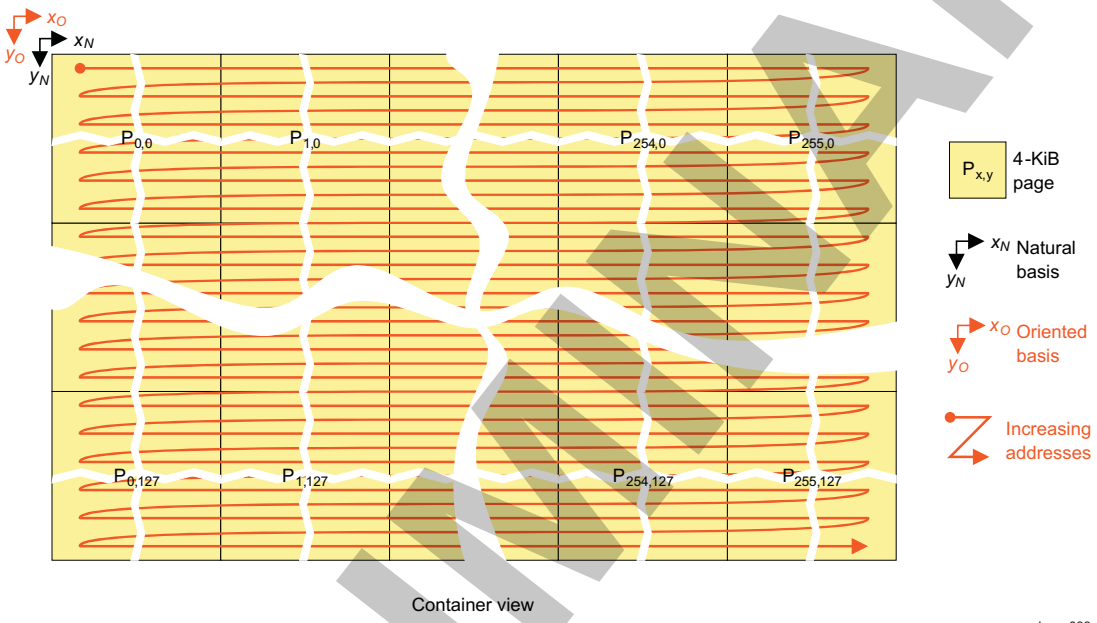
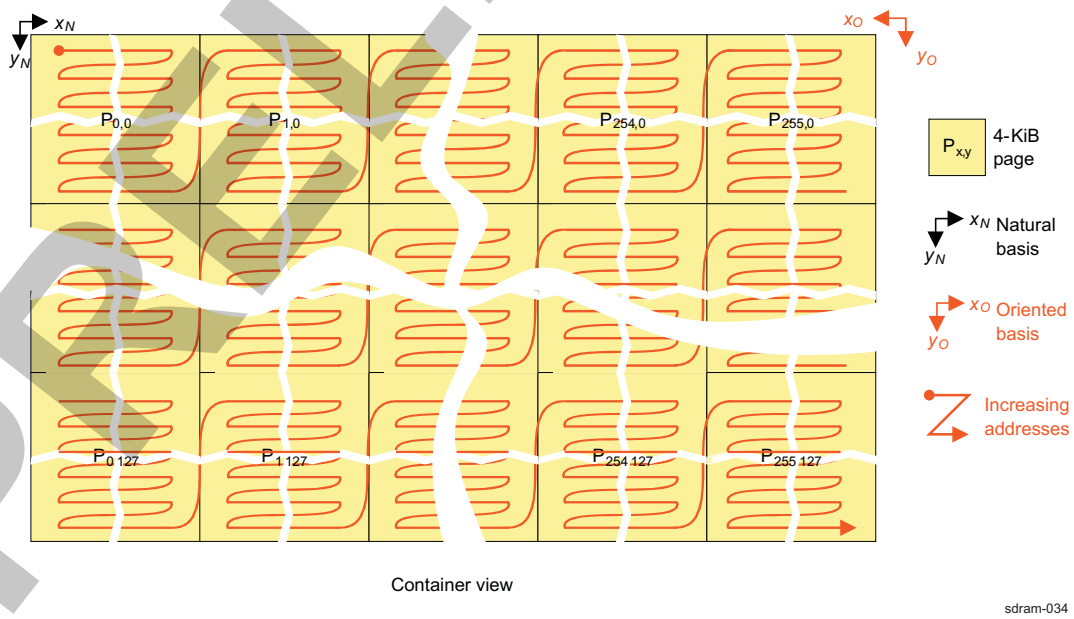


Figure 15-20. Page Mode Ordering of Elements in Natural View



15.2.3.6.1.7.3.2 0-Degree View With Vertical Mirror or 180-Degree View With Horizontal Mirror

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(Orientation 1)

This orientation defined by S = 0, $\overline{Y}$ = 0, and $\overline{X}$ = 1 and means that the operated change of basis is:

$$\begin{cases} \vec{x}_O = -\vec{x}_N \\ \vec{y}_O = \vec{y}_N \end{cases}$$

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In any TILER mode, the elements are then ordered from right to left and then from top to bottom in their container, as shown in Figure 15-21 and Figure 15-22.

Figure 15-21. Tiled Mode Ordering of Elements in 0-Degree View With Vertical Mirror

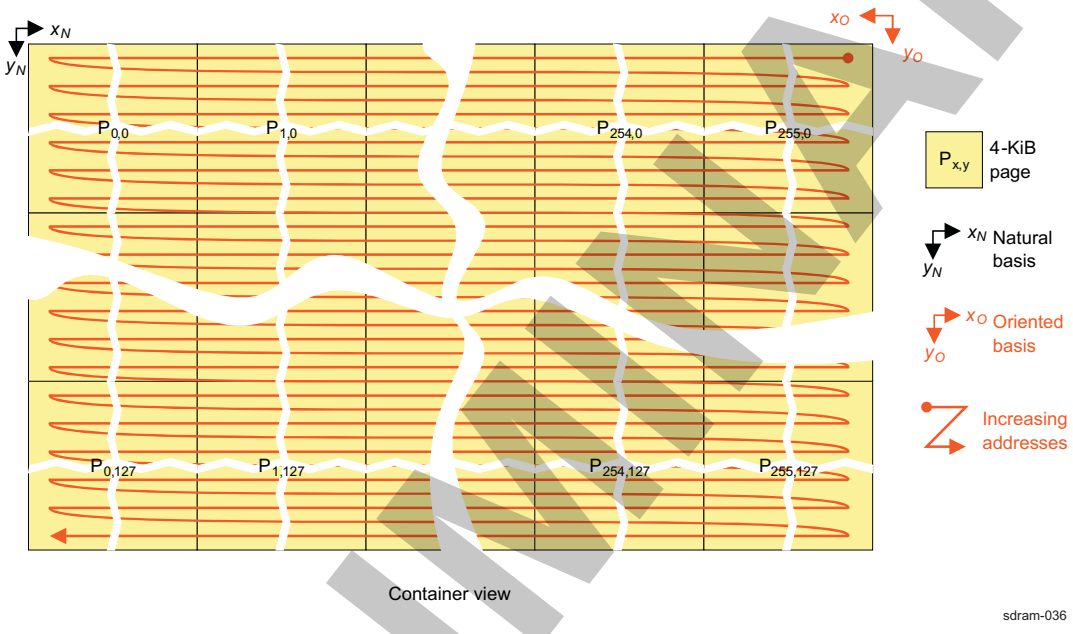
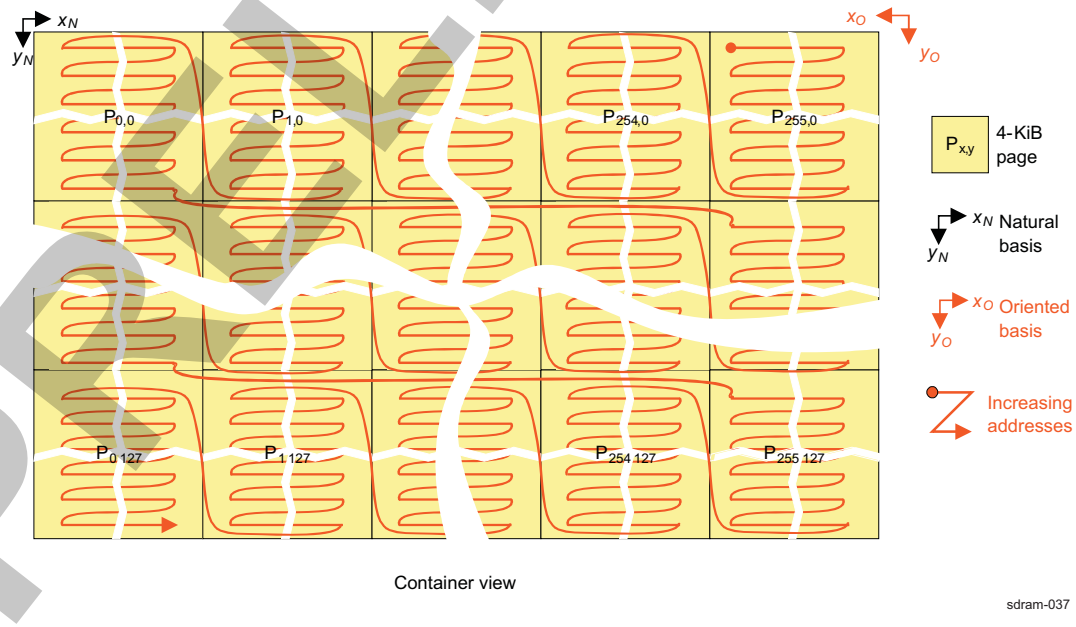


Figure 15-22. Page Mode Ordering of Elements in 0-Degree View With Vertical Mirror



15.2.3.6.1.7.3.3 0-Degree View With Horizontal Mirror or 180-Degree View With Vertical Mirror

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(Orientation 2)

This orientation defined by S = 0, $\overline{Y}$ = 1, and $\overline{X}$ = 0 and means that the operated change of basis is:

$$\begin{cases} \vec{x}_O = \vec{x}_N \\ \vec{y}_O = -\vec{y}_N \end{cases}$$

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In any TILER mode, the elements are ordered from left to right and then from bottom to top in their container, as shown in Figure 15-23 and Figure 15-24.

Figure 15-23. Tiled Mode Ordering of Elements in 0-Degree View With Horizontal Mirror

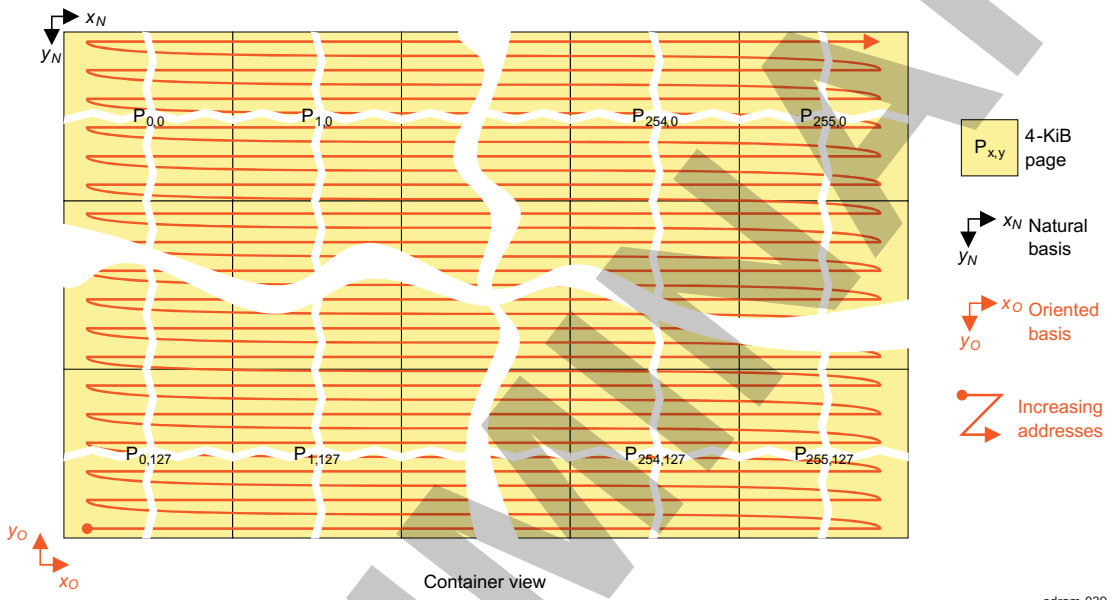
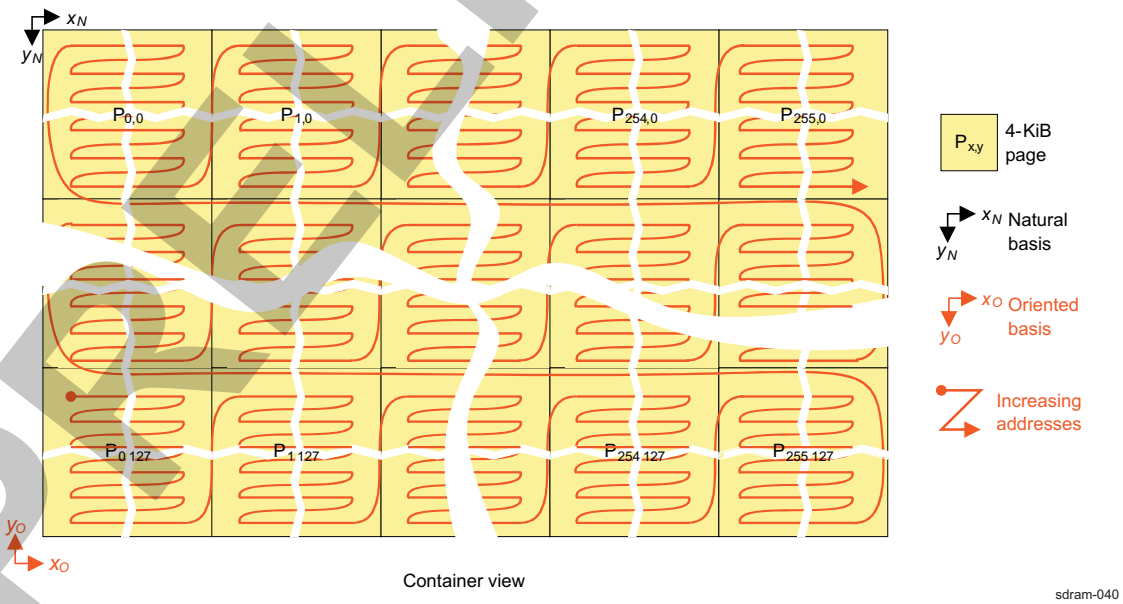


Figure 15-24. Page Mode Ordering of Elements in 0-Degree View With Horizontal Mirror



15.2.3.6.1.7.3.4 180-Degree View (Orientation 3)

This orientation defined by S = 0, $\overline{Y}$ = 1, and $\overline{X}$ = 1 and means that the operated change of basis is:

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$$\begin{cases} \vec{x}_O = -\vec{x}_N \\ \vec{y}_O = -\vec{y}_N \end{cases}$$

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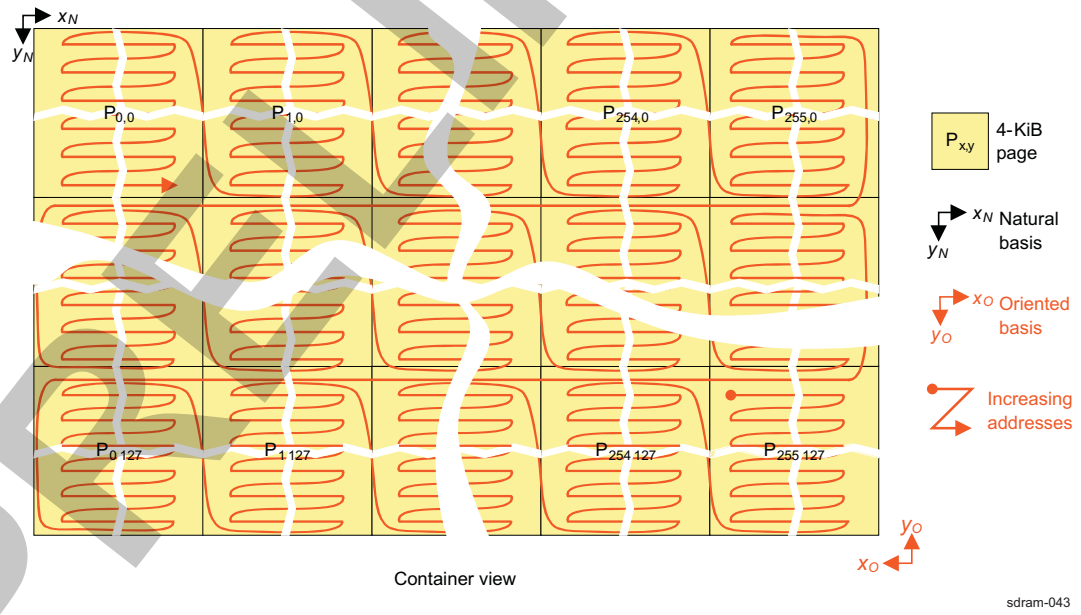
In any TILER mode, the elements are ordered from right to left and then from bottom to top in their container, as shown in Figure 15-25 and Figure 15-26.

Figure 15-25. Tiled Mode Ordering of Elements in 180-Degree View

Figure 15-26. Page Mode Ordering of Elements in 180-Degree View



15.2.3.6.1.7.3.5 90-Degree View With Vertical Mirror or 270-Degree View With Horizontal Mirror (Orientation 4)

This orientation defined by S = 1, $\overline{Y}$ = 0, and $\overline{X}$ = 0 and means that the operated change of basis is:

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$$\begin{cases} \vec{x}_O = \vec{y}_N \\ \vec{y}_O = \vec{x}_N \end{cases}$$

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In any TILER mode, the elements are ordered from top to bottom and then from left to right in their container, as shown in Figure 15-27 and Figure 15-28.

Figure 15-27. Tiled Mode Ordering of Elements in 90-Degree View With Vertical Mirror

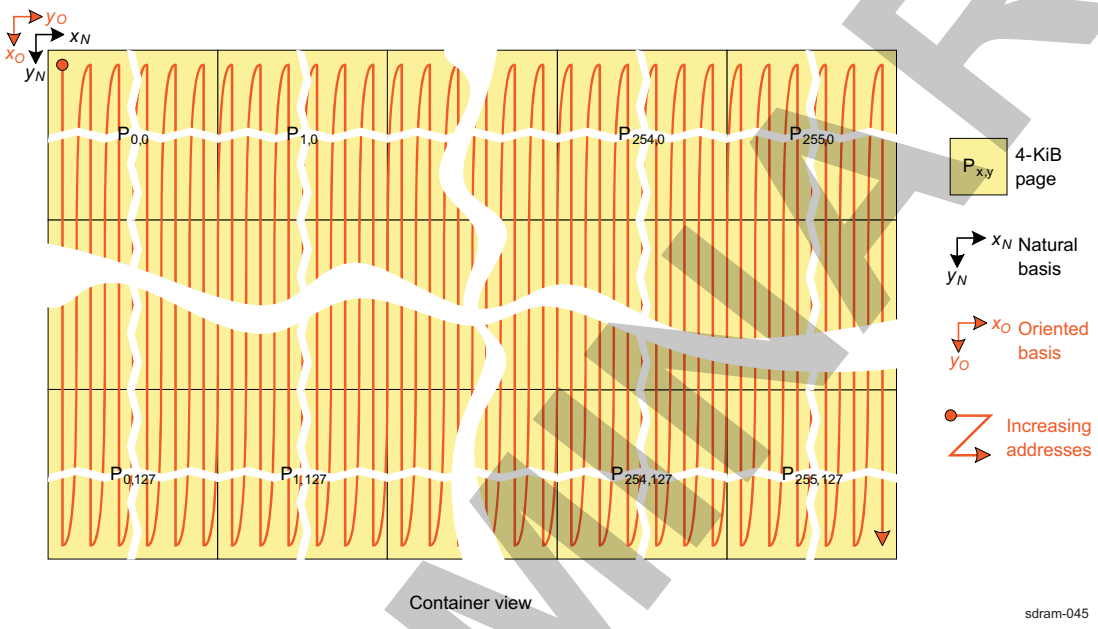

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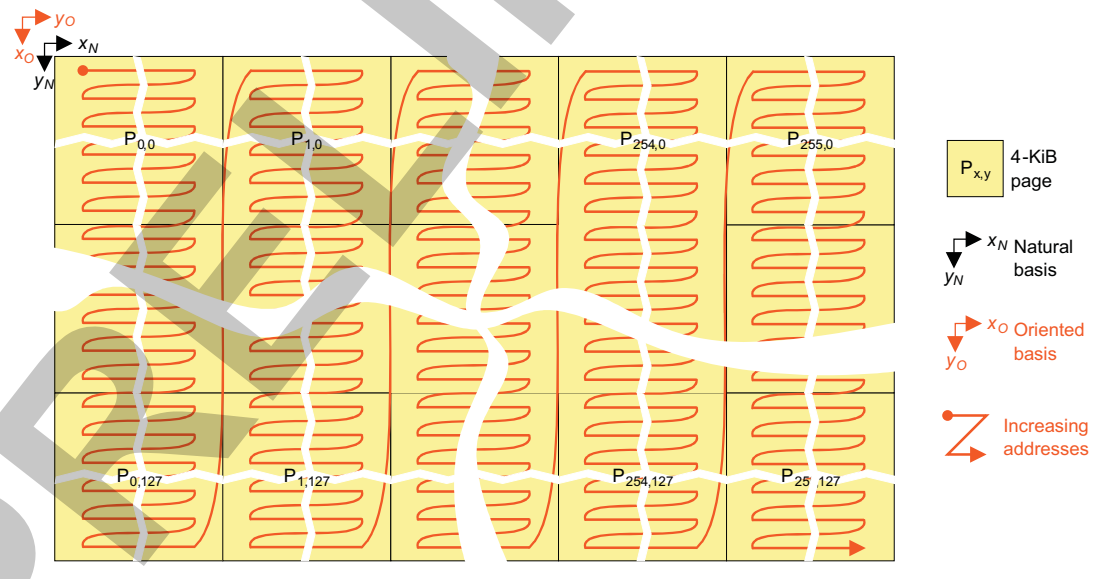
Figure 15-28. Page Mode Ordering of Elements in 90-Degree View With Vertical Mirror



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15.2.3.6.1.7.3.6 270-Degree View (Orientation 5)

This orientation defined by S = 1, $\overline{Y}$ = 0, and $\overline{X}$ = 1 and means that the operated change of basis is:

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$$\begin{cases} \vec{x}_O = \vec{y}_N \\ \vec{y}_O = -\vec{x}_N \end{cases}$$

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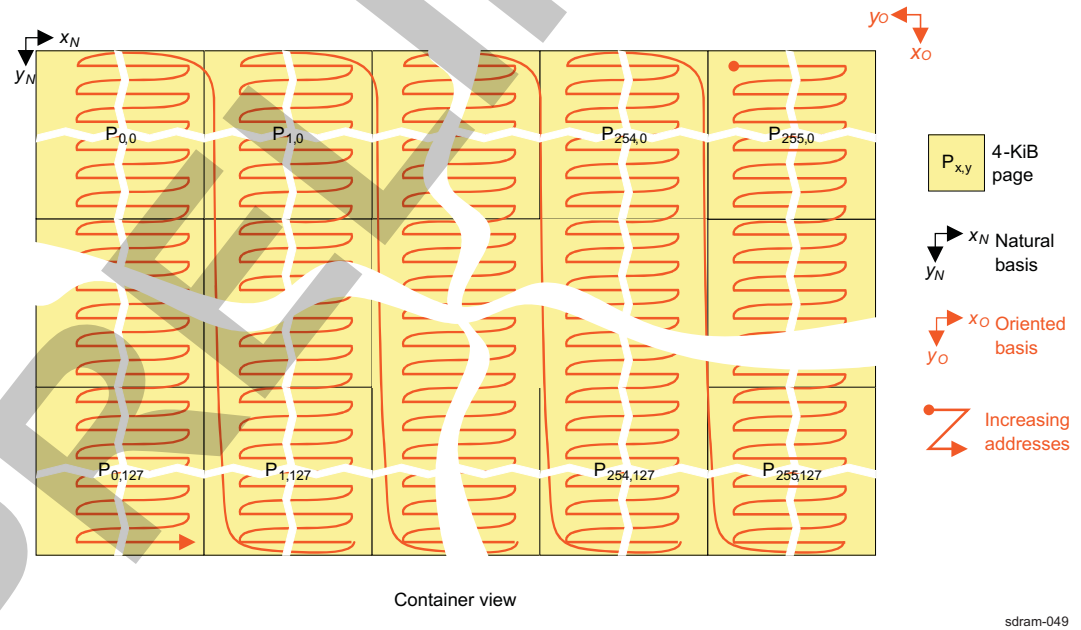
In any TILER mode, the elements are ordered from top to bottom and then from right to left in their container, as shown in Figure 15-29 and Figure 15-30.

Figure 15-29. Tiled Mode Ordering of Elements in 270-Degree View

Figure 15-30. Page Mode Ordering of Elements in 270-Degree View



15.2.3.6.1.7.3.7 90-Degree View (Orientation 6)

This orientation defined by S = 1, $\overline{Y}$ = 1, and $\overline{X}$ = 0 and means that the operated change of basis is:

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$$\begin{cases} \vec{x}_O = -\vec{y}_N \\ \vec{y}_O = \vec{x}_N \end{cases}$$

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In any TILER mode, the elements are ordered from bottom to top and then from left to right in their container, as shown in Figure 15-31 and Figure 15-32.

Figure 15-31. Tiled Mode Ordering of Elements in 90-Degree View

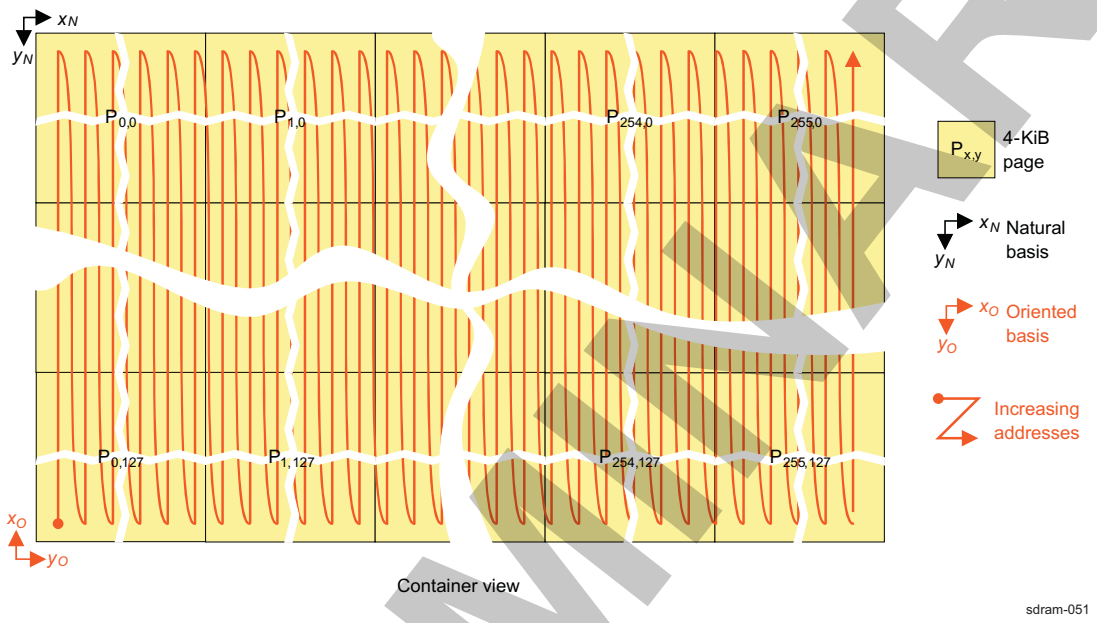
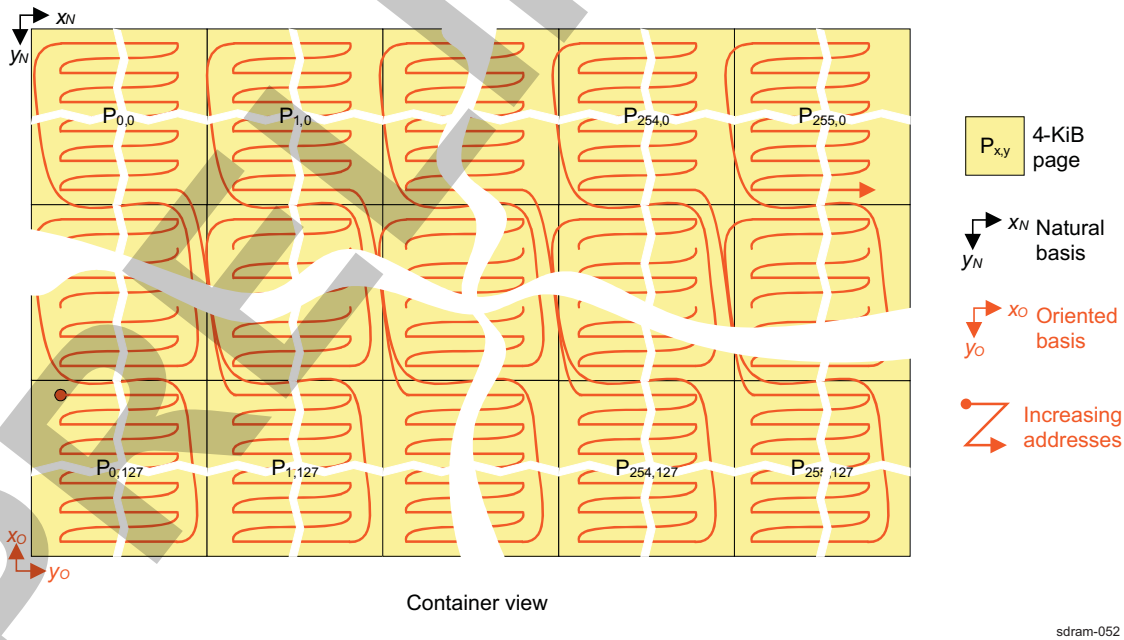


Figure 15-32. Page Mode Ordering of Elements in 90-Degree View



15.2.3.6.1.7.3.8 90-Degree View With Horizontal Mirror or 270-Degree View With Vertical Mirror (Orientation 7)

This orientation defined by S = 1, $\overline{Y}$ = 1, and $\overline{X}$ = 1 and means that the operated change of basis is:

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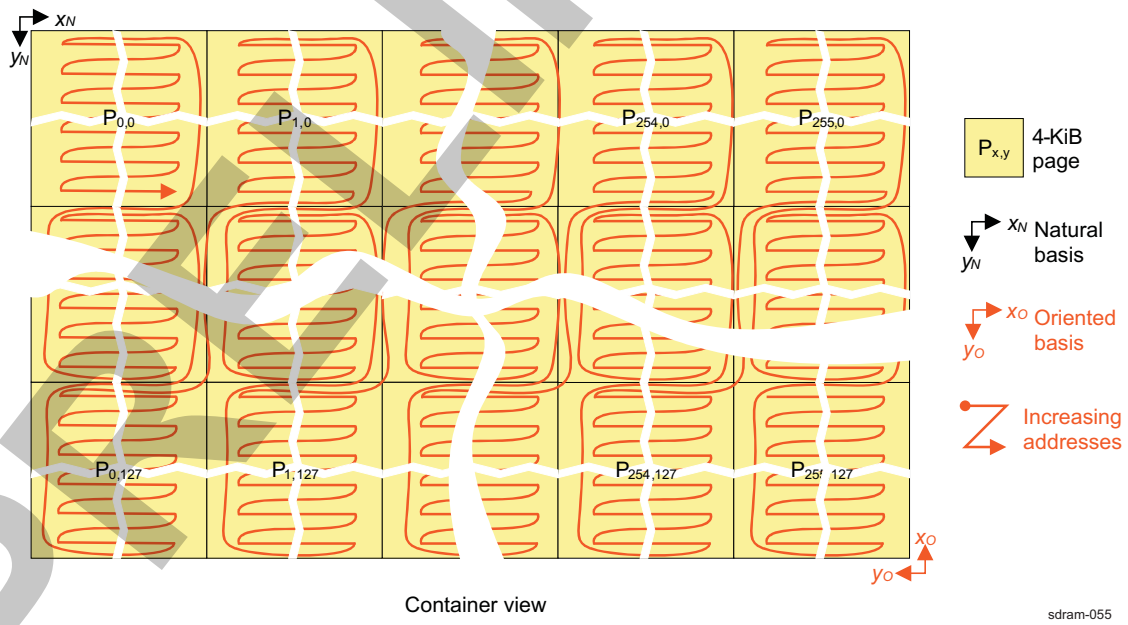
$$\begin{cases} \vec{x}_O = -\vec{y}_N \\ \vec{y}_O = -\vec{x}_N \end{cases}$$

sdram-053

In any TILER mode, the elements are ordered from bottom to top and then from right to left in their container, as shown in Figure 15-33 and Figure 15-34.

Figure 15-33. Tiled Mode Ordering of Elements in 90-Degree View With Horizontal Mirror

Figure 15-34. Page Mode Ordering of Elements in 90-Degree View With Horizontal Mirror



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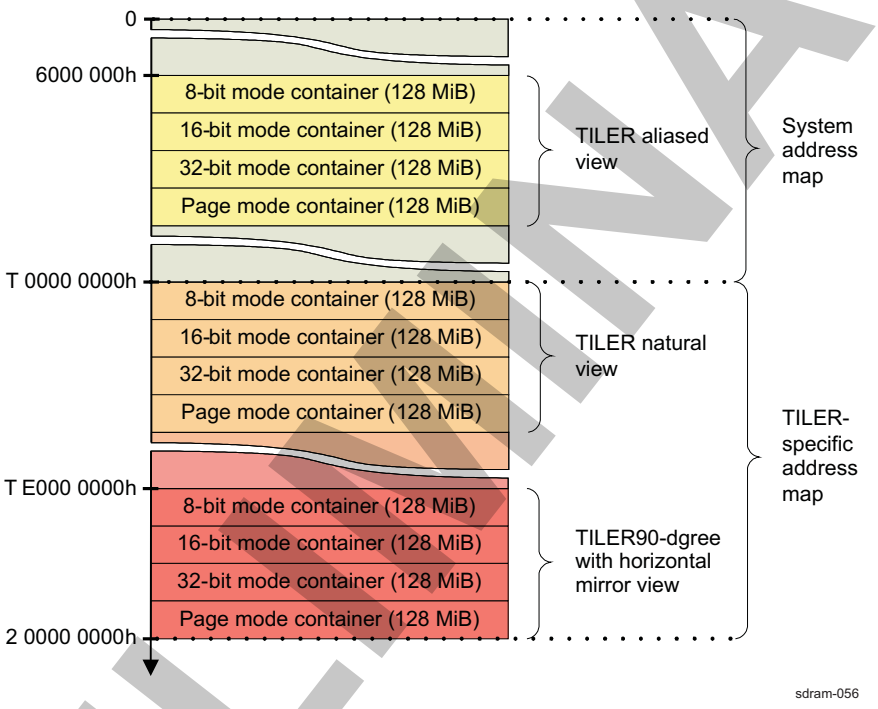
15.2.3.6.2 TILER Macro-Architecture

The TILER requires a 4-GiB addressing space to map its 128-MiB physical container in four modes and eight orientations. Because its addressing space alone fills the 4-GiB global system address map, the TILER addressing space cannot enter as-is into the system address map. Besides, putting in place a register-based mechanism per initiator to specify the orientation of the following accesses and then reducing the TILER addressing space to a single 512-MiB view is not an option; this is because most of the bandwidth-hungry initiators require simultaneous accesses to the TILER container in different views.

As a result, 32 bits are not enough to address all these requests, because the TILER port must convey not only virtually addressed requests to the "oriented" TILER containers but also physically addressed requests to the attached SDRCs. A thirty-third address bit is necessary to distinguish the two separated address maps, as shown in Figure 15-35.

Figure 15-35. TILER Port Address Map



Still, having separated systems and TILER-specific address maps is not sufficient. In a system many existing and external IP blocks still rely on a 32-bit address and would then be limited to one or the other 4-GiB addressing space. To overcome this limitation, one 512-MiB view is aliased in the system address map as (see Table 15-14 and Figure 15-36).

Table 15-14. TILER Aliased View in the L3 Interconnect Mapping

Start Address (hex)	End Address (hex)	Size
0x6000_0000	0x7FFF_FFFF	512 MiB

From all incoming requests, TILER requests are filtered as having an address that fits one of the following:

- The address format in the TILER-specific address map given in Table 15-15
- The address format of the aliased view in the system address map given in Table 15-16

Other requests are forwarded directly to the SDRC in TILER bypass mode.

Table 15-15. Address Format in the TILER-Specific Address Map

32	31	30	29	28	27	26 ... 4	3 ... 0
T	Orientation			Mode		Virtual address	
1	S	$\overline{Y}$	$\overline{X}$	M1	M0	A26 ... A4	0

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Table 15-16. Address Format of the TILER Aliased View in the System Address Map

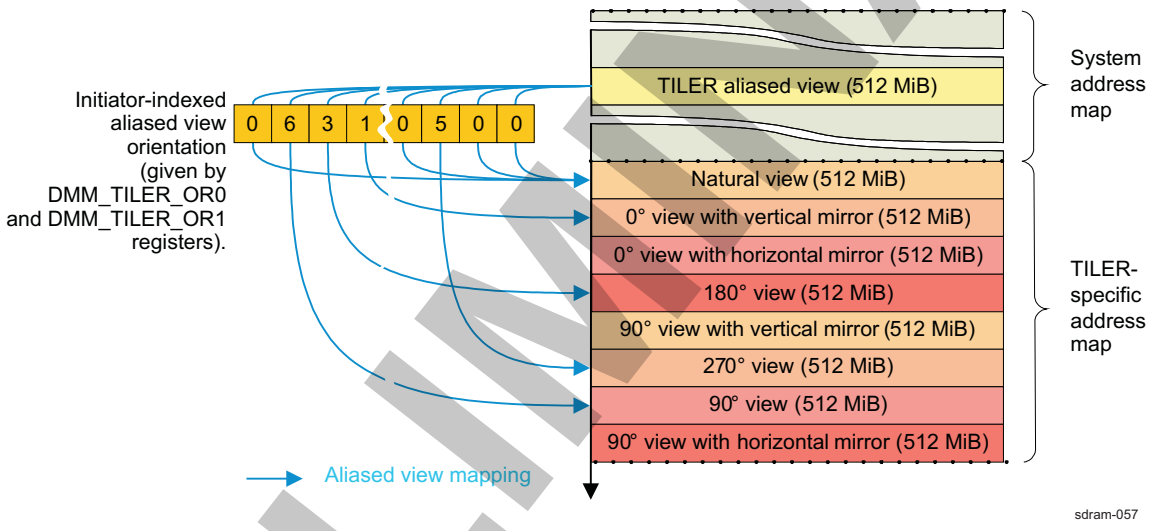
32	31	30	29	28	27	26 ... 4	3 ... 0
T	TILER aliasing			Mode		Virtual address	
0	0	1	1	M1	M0	A26 ... A4	0

In these address formats:

- The thirty-third bit, noted T, is aimed at distinguishing the standard 4-GiB system address map from the 4-GiB TILER-specific address map.
- The orientation bits, noted S, $\overline{Y}$, and $\overline{X}$, define the request orientation, as specified in Table 15-12.
- The mode bits, noted M1 and M0, define the request mode, as specified in Table 15-11.
- The remaining 27 bits, noted A0 to A26, define the mode and orientation specific virtual address, as defined in Figure 15-16, Figure 15-17, and Figure 15-18.

The orientation of the aliased TILER view is extracted from an initiator-indexed LUT, as shown in Figure 15-36.

Figure 15-36. TILER Aliased View Orientation



As shown in Figure 15-36, an internal initiator-indexed LUT stores the current orientation of the aliased view for each initiator.

When an interconnect request hits the TILER aliased view in the system address map, the request initiator orientation is extracted from the LUT and the request address is translated according to this orientation: the T bit is set and bits [31:29] are replaced with the orientation.

Regarding the dimensioning of this LUT, given that initiators simultaneously accessing multiple views use the TILER-specific address map, and many initiators do not need to access any view or can be restricted to accessing only the natural view, only a limited number of initiators are likely to dynamically modify the orientation of its aliased TILER view.

The orientation LUT is limited to 16 entries. These 16 orientation entries are mapped on the two 32-bit DMM_TILER_OR0 and DMM_TILER_OR1 registers.

The first eight entries of the LUT are mapped in the DMM_TILER_OR0 register, and the last eight entries are mapped in the DMM_TILER_OR1 register. Therefore, given an index x, the orientation related to this index is given in the ORx field.

Each of these registers is split into eight 4-bit fields, each field mapping an entry of the LUT with:

- An S, $\overline{Y}$, $\overline{X}$ orientation code on the 3 LSBs
- An $\overline{W}$ field-specific active-low local write-enable bit, always read as 0, on the MSB.

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The registers fields that correspond to initiators that do not need any dynamic configuration of their aliased view orientation must be specified as reserved fields, and only written with zeros.

The $\overline{W}$ bit allows the modification of a single entry without requiring a read-modify-write sequence. This approach is then more accommodating:

- In a system where multiple initiators can modify their own fields in the registers
- With initiators unable to make the read-modify-write sequence, such as DMA

Still, the $\overline{W}$ bit is active-low to keep the compatibility with the usual read-modify-write sequence. When reading an aliased view orientation register, because all its $\overline{W}$ bits are read as 0, if these bits are untouched by the modification—as they should be—writing back the modified register updates all orientation fields of the register.

15.2.3.6.3 TILER Guidelines for Initiators

15.2.3.6.3.1 Buffered Raster-Based Initiators

15.2.3.6.3.1.1 Buffer Size

The necessary minimum buffer size depends on the SDRAM prefetch size and on initiator support in terms of the following:

- Element size
- Orientation
- Maximum number of elements per line in all supported element sizes and orientations

Let N be the maximum number of elements per line for a given mode (element size) and orientation, P be the SDRAM memory prefetch size in bytes, and *max* be the function returning the maximum of the two parameters. The minimum necessary line buffer size to handle all resolutions in a given mode and orientation is listed in Table 15-17.

Table 15-17. Minimum Buffer Size to Efficiently Handle Lines of up to N Elements

	0- or 180- Degree Orientation (S = 0)	90- or 270-Degree Orientation (S = 1)
8-bit mode	4 × N bytes	*max* (4,P/4) × N bytes
16-bit mode	None	*max* (8,P/2) × N bytes
32-bit mode	None	*max* (8,P/2) × N bytes

This minimal buffer size can be reached only with an advanced FIFO management scheme. The standard ping-pong buffer requires twice this buffer size.

NOTE: Given their nature, field accesses to an interlaced frame-buffer require buffers twice as small as in the standard progressive case.

For instance, an initiator that must handle only a single progressive frame-buffer in any orientation of:

- Up to 1920 × 1080 in YUV4:2:0
- Up to 1600 × 1200 in 16-bit RGB565
- Up to 800 × 600 in 32-bit ARGB

requires a line buffer of at least 15,360 bytes because:

- 4 × 1920 + 4 × 2960 = 15,360 bytes required for a 3-plane YUV4:2:0 frame of 1920 × 1080
- 4 × 1920 + 8 × 960 = 15,360 bytes required for a 2-plane YUV4:2:0 frame of 1920 × 1080
- 8 × 1600 = 12,800 bytes required for a 16-bit RGB565 frame of 1600 × 1200
- 8 × 800 = 6400 bytes required for a 32-bit ARGB frame of 800 × 600

and a line buffer of at least 30,720 bytes when using a simple ping-pong buffer scheme.

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15.2.3.6.3.1.2 Performance

Table 15-18 gives the ratio of effective data to transferred data at the external memory interface for buffered raster-based initiators in each mode and orientation, when using an up-to-32-bit DDR, lpDDR, or lpDDR2 SDRAM, or an up-to-16-bit DDR2 memory.

Table 15-18. Memory Data Payload for Buffered Raster-Based Initiators on Up-to-32-Bit DDR, lpDDR, or lpDDR2

	0- or 180-Degree Orientation (S = 0)		90- or 270-Degree Orientation (S = 1)	
	Progressive	Interlaced	Progressive	Interlaced
8-bit mode	100%	100%	100%	50%
16-bit mode	100%	100%	100%	50%
32-bit mode	100%	100%	100%	50%
Page mode	100%	N/A	100%	100%

When using 32-bit DDR, lpDDR, or lpDDR2 SDRAMs, or 16-bit DDR, DDR2, lpDDR, or lpDDR2 memories, whenever all previous guidelines are fulfilled, there is no penalty for these initiators to access a tiled object in any orientation, except for accesses to an interlaced frame in 90- or 270-degree orientation where the memory bandwidth is twice the requested bandwidth.

When using up-to-32-bit DDR, lpDDR, lpDDR2, or up-to-16-bit DDR2 SDRAMs, all accesses, except interlaced accesses in a 90- or 270-degree orientation, are equally efficient and offer the full possible memory bandwidth.

Because of its progressive nature, page mode does not introduce any performance hit.

Table 15-19 lists the ratio of effective data-to-transferred data at the external memory interface for the buffered raster-based initiators in each mode and orientation when using a 32-bit DDR2 or DDR3 memory.

Table 15-19. Memory Data Payload for Buffered Raster-Based Initiators on 32-Bit DDR2 or DDR3

	0- or 180-Degree Orientation (S = 0)		90- or 270-Degree Orientation (S = 1)	
	Progressive	Interlaced	Progressive	Interlaced
8-bit mode	100%	50%	100%	50%
16-bit mode	100%	50%	100%	50%
32-bit mode	100%	50%	100%	50%
Page mode	100%	N/A	100%	100%

When using 32-bit DDR2 or DDR3 SDRAMs, whenever all previous guidelines are fulfilled, there is no penalty for these initiators to access a tiled object in any orientation, except for accesses to an interlaced frame in any orientation where the memory bandwidth is twice the requested bandwidth.

When using DDR2 or DDR3 SDRAMs, all accesses, except interlaced accesses, are equally efficient and offer the full possible memory bandwidth.

Similarly, page mode does not introduce any performance hit.

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15.2.4 DMM Use Cases and Tips

15.2.4.1 PAT Use Cases

Five ways to use PAT are:

- Simple manual area refill: Section 15.2.4.1.1
- Single auto-configured area refill: Section 15.2.4.1.2
- Chained auto-configured area refill: Section 15.2.4.1.3
- Synchronized auto-configured area refill: Section 15.2.4.1.4
- Cyclic synchronized auto-configured area refill: Section 15.2.4.1.5

NOTE: PAT refill area must be fully contained within either the LUT lower half or the LUT upper half. It must not span over both areas. That is, y0 MS

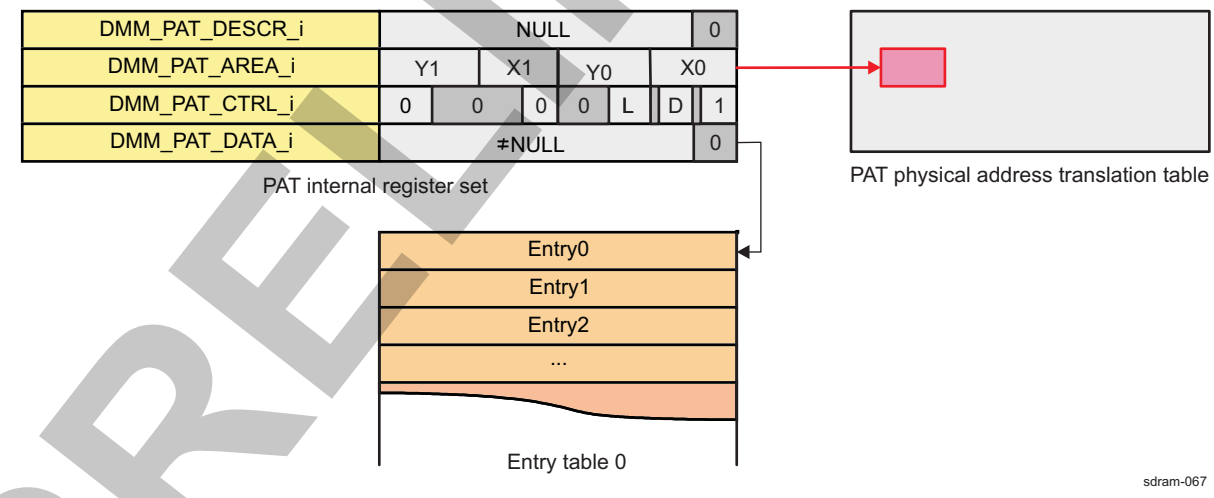
bit y0[7] must be equal to y1 MSbit y1[7] when defining the area descriptor.

15.2.4.1.1 Simple Manual Area Refill

The following must be performed to create a 16-byte aligned memory-mapped entry table containing all entries of the defined area (see Figure 15-37):

1. Write the DMM_PAT_AREA_i register with the relevant (x0, y0) (x1, y1) area definition.
2. Write the DMM_PAT_DATA_i register with the physical address of the created entry table.
3. Write the DMM_PAT_CTRL_i register with the requested refill direction and assert the DMM_PAT_CTRL_i[0] START bit with the requested refill direction D and with the LUT ID L if multiple LUTs are present in the system.
4. The refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.
5. A new refill can be initiated when the DMM_PAT_STATUS_i[0] READY bit is set.

Figure 15-37. Simple Manual Area Refill Scheme



15.2.4.1.2 Single Auto-Configured Area Refill

The following must be performed to create a 16-byte aligned memory-mapped entry table containing all entries of the defined area (see Figure 15-38):

1. Create a 16-byte aligned memory-mapped descriptor structure where:
   - The next field is set to NULL.
   - The area field is set with the relevant (x0, y0) (x1, y1) area definition.
   - The ctrl field is set with the requested direction D, with the requested LUT ID L if multiple LUTs are

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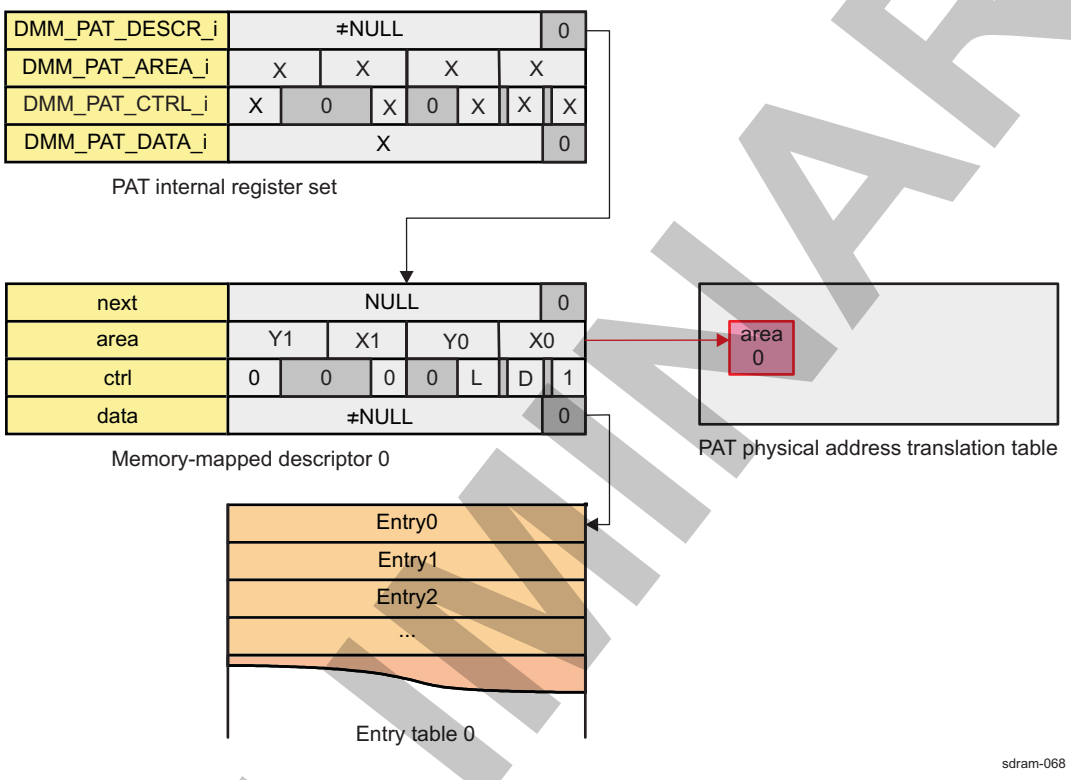
present in the system, and the START bit is asserted to start refilling as soon as this descriptor enters the PAT refill engine.

- The data field is set to the physical address of the created entry table.

2. Write the DMM_PAT_DESCR_i register with the physical address of the created descriptor.
3. The refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.
4. A new refill can be initiated when the DMM_PAT_STATUS_i[0] READY bit is set.

Figure 15-38. Single Auto-Configured Area Refill Scheme



15.2.4.1.3 Chained Auto-Configured Area Refill

The following must be performed to create one 16-byte aligned memory-mapped entry table per area containing the entries for the corresponding area (see Figure 15-39):

1. Create one 16-byte aligned memory-mapped descriptor structure per area where:
   - The next field is set to the physical address of the next descriptor or NULL for the last one.
   - The area field is set with the relevant (x0, y0) (x1, y1) area definition.
   - The ctrl field is set with the requested direction D, with the requested LUT ID L if multiple LUTs are present in the system, and the START bit is asserted to start refilling as soon as the previous area refill is done.
   - The data field is set to the physical address of the corresponding entry table.
2. Write the DMM_PAT_DESCR_i register with the physical address of the first created descriptor.
3. Each area refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.
4. All area refills are done when the DMM_PAT_STATUS_i[0] READY bit is set.
5. A new refill can be initiated when the DMM_PAT_STATUS_i[0] READY bit is set.

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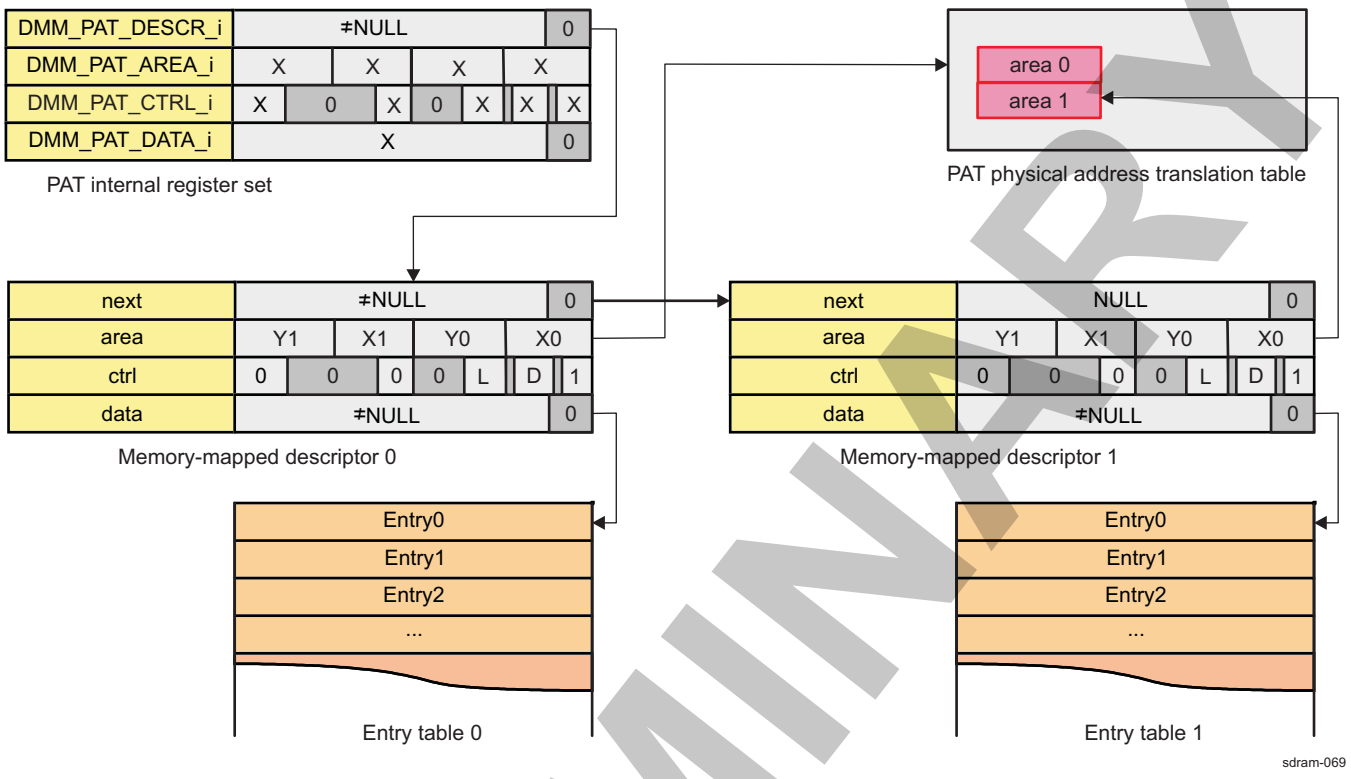
Figure 15-39. Chained Auto-Configured Area Refill Scheme



15.2.4.1.4 Synchronized Auto-Configured Area Refill

The following must be performed to create one 16-byte aligned memory-mapped entry table per area containing the entries for the corresponding area (see Figure 15-40):

1. Create one 16-byte aligned memory-mapped descriptor structure per area where:
   - The next field is set to the physical address of the next descriptor or NULL for the last one.
   - The area field is set with the relevant (x0, y0) (x1, y1) area definition.
   - The ctrl field is set with the synchronizing initiator identifier I, the SYNC bit is asserted, the requested direction D and the requested LUT ID L if multiple LUTs are present in the system, and the START bit is asserted to start refilling as soon as the previous area refill is done and initiator I has made one access in the previous area.
   - The data field is set to the physical address of the corresponding entry table.
2. Write the DMM_PAT_DESCR_i register with the physical address of the first created descriptor.
3. Each area refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.
4. All area refills are done when the DMM_PAT_STATUS_i[0] READY bit is set.
5. A new refill can be initiated when the DMM_PAT_STATUS_i[0] READY bit is set.

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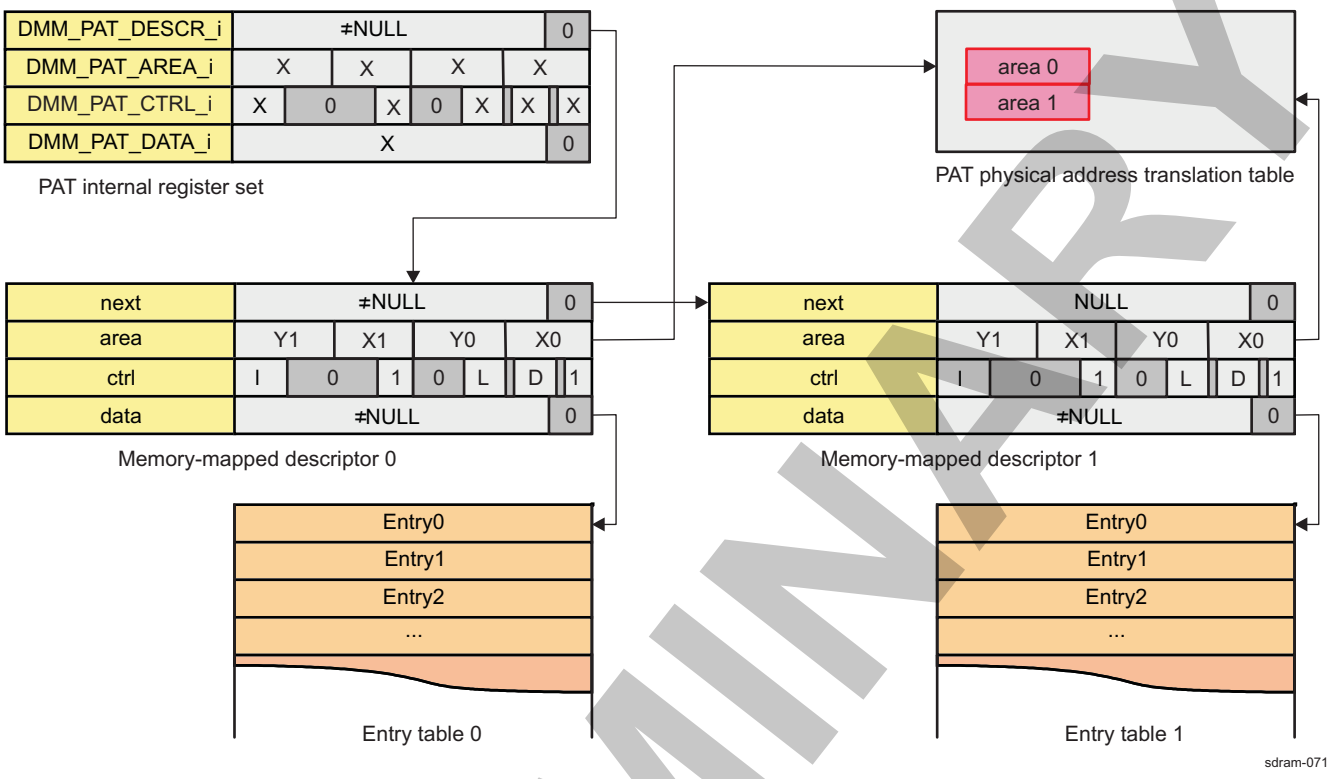
Figure 15-40. Synchronized Auto-Configured Area Refill Scheme



15.2.4.1.5 Cyclic Synchronized Auto-Configured Area Refill

The following must be performed to create one 16-byte aligned memory-mapped entry table per area containing the entries for the corresponding area (see Figure 15-41):

1. Create one 16-byte aligned memory-mapped descriptor structure per area where:
   - The next field is set to the physical address of the next descriptor in the circular list.
   - The area field is set with the relevant (x0, y0) (x1, y1) area definition.
   - The ctrl field is set with the synchronizing initiator identifier I, the SYNC bit asserted, the requested direction D and requested LUT ID L if multiple LUTs are present in the system, and the START bit is asserted to start refilling as soon as the previous area refill is done and initiator I has made one access in the previous area.
   - The data field is set to the physical address of the corresponding entry table.
2. Write the DMM_PAT_DESCR_i register with the physical address of the initial descriptor.
3. Each area refill is done when the DMM_PAT_STATUS_i[3] DONE bit is set.
4. A new refill can be initiated by writing any value to the DMM_PAT_DESCR_i register to abort the current one.

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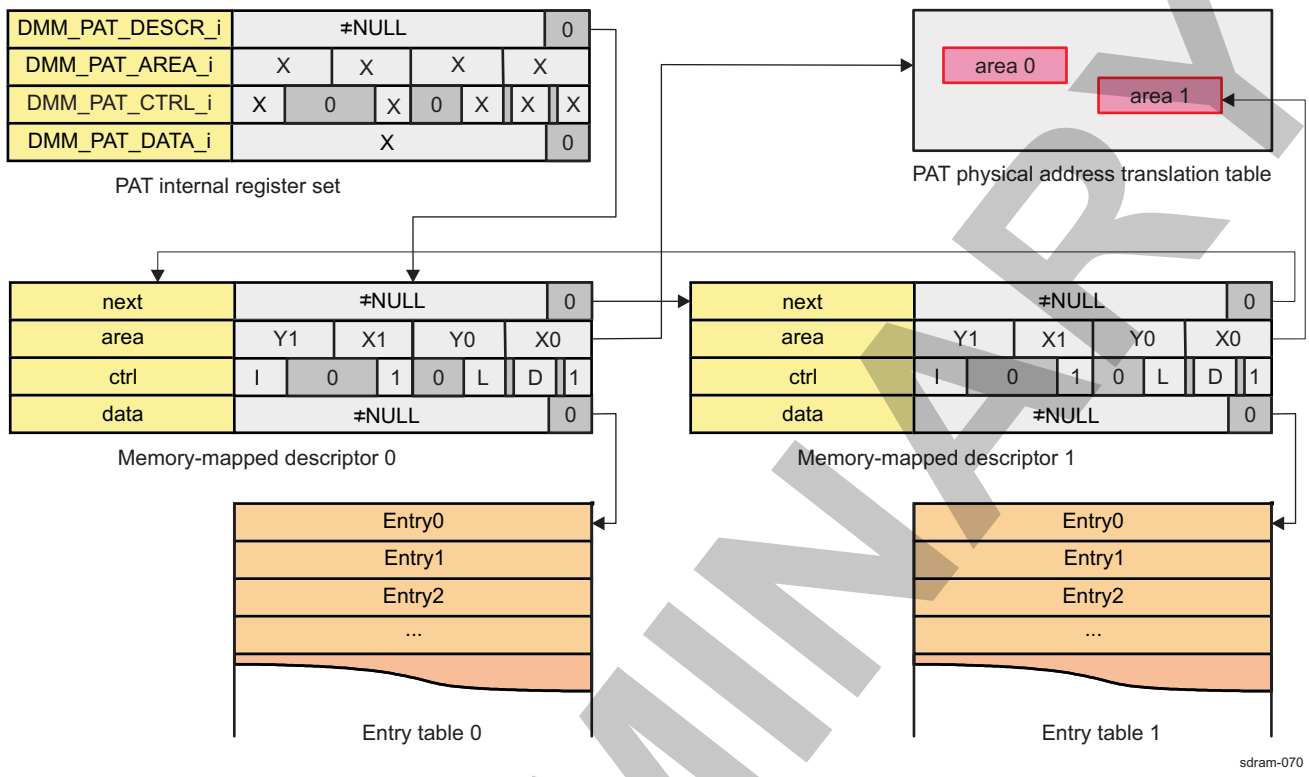
Figure 15-41. Cyclic Synchronized Auto-Configured Area Refill Scheme



NOTE: Never use circular lists of descriptors where all descriptors have the DMM_PAT_CTRL_i[0] START bit set and there is no synchronization. This leads to an endless continuous refill.

15.2.4.2 Addressing Management with LISA

15.2.4.2.1 Case 1: Use of One Memory Controller

In this example, assume there is 1 GiB of external memory evenly spread onto two address spaces. The address range for address space 0 must start at offset 0x2000_0000 (see Table 15-20).

Table 15-20. Address Definition

Address Range	Memory Controller	Memory Controller Address Space[(1)]	Memory Controller Address Range
0x8000_0000 to 0x9FFF_FFFF	EMIF1	0x1	0x0000_0000 to 0x1FFF_FFFF
0xA000_0000 to 0xBFFF_FFFF	EMIF1	0x0	0x2000_0000 to 0x3FFF_FFFF

(1) For memory controller address spaces, see , *Local Interface*.

This configuration requires two nonoverlapping sections to be set. They can be defined in any order because there is no concern with priority in this case (see Table 15-21):

Table 15-21. Configuration

Bit Field	Section 0 (DMM_LISA_MAP_0)	Section 1 (DMM_LISA_MAP_1)
[31:24] SYS_ADDR	0x80	0xA0
[22:20] SYS_SIZE	0x5	0x5
[19:18] SDRC_INTL	0x0 (not applicable)	0x0 (not applicable)

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Table 15-21. Configuration (continued)

Bit Field	Section 0 (DMM_LISA_MAP_0)	Section 1 (DMM_LISA_MAP_1)
[17:16] SDRC_ADDRSPC	0x1	0x0
[9:8] SDRC_MAP	0x1 (only EMIF1)	0x1 (only EMIF1)
[7:0] SDRC_ADDR	0x00	0x20

To check whether an address hits a section, use the 8 upper address bits of the address and mask them with the hit mask: 2^8–2^{SYS_SIZE}. If the result is equal to SYS_ADDR, the section is hit.

To define the physical address to be issued to the memory controller, use the 8 upper address bits of the system address, mask them with the address mask: 2^{SYS_SIZE}–1, and OR them with SDRC_ADDR. This gives the resulting 8 upper physical address bits. All lower address bits are forwarded unchanged.

Request to address 0x99AE_37F0:

- Upper address bits: 0x99
- Hit mask: 2^8–2^5 = 0xE0
- Masked upper address bits: 0x80, that is, hits section 0
- Address mask: 2^5–1 = 0x1F
- Masked upper address bits: 0x19
- OR with SDRC_ADDR: 0x19
- Physical address: 0x19AE_37F0

This request is forwarded to address 0x19AE_37F0, address space 1 of the memory controller.

Request to address 0xB7FF_0340:

- Upper address bits: 0xB7
- Hit mask: 2^8–2^5 = 0xE0
- Masked upper address bits: 0xA0, that is, hits section 1
- Address mask: 2^5–1 = 0x1F
- Masked upper address bits: 0x17
- OR with SDRC_ADDR: 0x37
- Physical address: 0x37FF_0340

This request is forwarded to address 0x37FF_0340, address space 0 of the memory controller.

15.2.4.2.2 Case 2: Use of Two Memory Controllers

In the case of 512 MiB interleaved at 128-byte boundaries and 256 MiB noninterleaved on the second memory controller, one address space per memory controller, we have the following results (see Table 15-22).

Table 15-22. Address Definition

Address Range	Memory Controller	Memory Controller Address Space[(1)]	Memory Controller Address Range
0x8000_0000 to 0x9FFF_FFFF	EMIF1 and EMIF2, interleaved at 128-byte boundaries	0x0 on both controllers	0x0000_0000 to 0x0FFF_FFFF on both controllers
0xA000_0000 to 0xAFFF_FFFF	EMIF2 only	0x0	0x1000_0000 to 0x1FFF_FFFF

(1) For memory controller address spaces, see , *Local Interface*.

Two sections are used to map such a configuration (see Table 15-23).

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Table 15-23. Configuration

Bit Field	Section 0 (DMM_LISA_MAP_0)	Section 1 (DMM_LISA_MAP_1)
[31:24] SYS_ADDR	0x80	0xA0
[22:20] SYS_SIZE	0x5	0x4
[19:18] SDRC_INTL	0x1	0x0 (not applicable)
[17:16] SDRC_ADDRSPC	0x0	0x0
[9:8] SDRC_MAP	0x3	0x2
[7:0] SDRC_ADDR	0x00	0x10

Detecting a section hit is the same for the interleaved case as for the single controller case: To check whether an address hits a section, use the 8 upper address bits of the address and mask them with the hit mask: 28–2^{SYS_SIZE}. If the result is equal to SYS_ADDR, the section is hit.

The physical address generation is modified for the interleaved case. In case of 256-byte interleaving, the first chunk of 256 bytes is mapped to the first controller, the second chunk to the second controller, and so on. This results in system address bit 8 to be decoded as the controller indicator, 0 for the first controller, and 1 for the second controller (system address bit 7 is used for interleaving at the 128-byte boundary, and bit 9 for 512 bytes). This bit is not included in the computed physical address, meaning the upper system address bits [31:9] are shifted to bits [30:8] when generating the physical address.

The rest of the address generation is handled the same as for the single controller case: to define the physical address to be issued to the memory controller, use the 8 upper address bits of the system address, mask them with the address mask: 2^{SYS_SIZE}–1, and OR them with SDRC_ADDR. This gives the resulting 8 upper physical address bits. All lower address bits are forwarded unchanged.

Request to address 0x99AE_37F0:

- Upper address bits: 0x99
- Hit mask: 2^8–2^5 = 0xE0
- Masked upper address bits: 0x80, that is, hits section 0
- Address mask: 2^5–1 = 0x1F
- Masked upper address bits: 0x19
- Full masked address: 0x19AE_37F0
- Bit 7 is 1, that is, targets the second memory controller
- Full masked shifted address (suppressing bit 7): 0x0CD7_1BF0 (see Section 15.2.4.2.2.1)
- OR upper physical address bits with SDRC_ADDR: 0x0CD7_1BF0
- Physical address: 0x0CD7_1BF0

This request is forwarded to address 0x0CD7_1BF0, address space 0, of the second memory controller.

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15.2.4.2.2.1 Address Upper Bits Shifting

Table 15-24 describes shifting the address upper bits.

Table 15-24. Address Upper Bits Shifting

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address Before Interleaving																															
0	0	0	1	1	0	0	1	1	0	1	0	1	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1	0	0	0	0
Address After Interleaving																															
0	0	0	0	1	1	0	0	1	1	0	1	0	1	1	1	0	0	0	1	1	0	1	1	1	1	1	1	0	0	0	0

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15.2.5 DMM Basic Programming Model

The programming model section:

- Describes how objects can be addressed in all TILER modes and orientations
- Explains how the physical containers and PAT LUT can be shared between different modes
- Does not give an exhaustive description of the TILER and DMM registers, because these are described in Section 15.2.3.5, *DMM*, and Section 15.2.3.6, *TILER*.

15.2.5.1 Global Initialization

This section identifies the requirements for initializing the surrounding modules when the DMM is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DMM (see Table 15-25).

Table 15-25. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface and functional clocks must be enabled. See Section 3.1.1, *Power, Reset, and Clock Management.*
Image processing unit (IPU)	IPU interrupt controller (INTC) configuration must be done to enable the interrupts from the DMM. See Section 17.1, *Interrupt Controllers.*
Main processing unit (MPU)	MPU INTC configuration must be done to enable interrupts from the DMM. See Section 17.1, *Interrupt Controllers.*
L3_MAIN interconnect	Data interface

15.2.5.2 DMM Module Global Initialization

Theprocedure in Table 15-26 initializes the DMM after a power-on reset (POR).

Table 15-26. DMM Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure the DMM for smart-idle power management mode.	DMM_SYSCONFIG[3:2] IDLE_MODE	0x2

15.2.5.3 DMM Operational Modes Configuration

15.2.5.3.1 Different Operational Modes

The TILER can be virtually accessed in four different modes: 8-, 16-, 32-bit, and page modes. Each mode defines the element granularity to apply isometric transforms (see Table 15-27).

Table 15-27. Coding and Description of TILER Modes

Mode	Name	Granularity (Element Size)
0	8-bit tiled mode	8 bits
1	16-bit tiled mode	16 bits
2	32-bit tiled mode	32 bits
3	Page mode	4096 bytes

15.2.5.3.2 Configuration Settings and LUT Refill

The procedure in Table 15-28 provides the configuration settings and LUT refill.

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Table 15-28. Configuration Settings and LUT Refill

Step	Register/Bit Field/Programming Model	Value
PAT configuration refill Engine 0	DMM_PAT_CONFIG[0] MODE0	xxx
PAT configuration refill Engine 1	DMM_PAT_CONFIG[1] MODE1	xxx
Set DMM PAT view register value for each initiator.	DMM_PAT_VIEW0 Vx DMM_PAT_VIEW1 Vx	xxx
Set DMM PAT write enable for the initiators.	DMM_PAT_VIEW0 Wx DMM_PAT_VIEW1 Wx	xxx
Choosing container type and access method	DMM_PAT_VIEW_MAP_i	xxx
Define the base address of all view mappings.	DMM_PAT_VIEW_MAP_BASE[31] BASE_ADDR	xxx
Set area definition for DMM physical address translator.	DMM_PAT_AREA_i	xxx
Set the physical address of the current table refill entry data or entry data when in manual mode.	DMM_PAT_DATA_i[31:4] ADDR	xxx
Define the direction of this PAT table refill (S Y X), different from 0x011.	DMM_PAT_CTRL_i[6:4] DIRECTION	xxx
Start a PAT table refill.	DMM_PAT_CTRL_i[0] START	0x1

15.2.5.3.3 Interleaving Settings

The procedure in Table 15-29 provides the interleaving settings.

Table 15-29. Interleaving Settings

Step	Register/Bit Field/Programming Model	Value
Set DMM system section address MSB.	DMM_LISA_MAP_i[31:24] SYS_ADDR	xxx
Set DMM system section size.	DMM_LISA_MAP_i[22:20] SYS_SIZE	xxx
Set SDRC interleaving mode.	DMM_LISA_MAP_i[19:18] SDRC_INTL	xxx
Set SDRC address space.	DMM_LISA_MAP_i[17:16] SDRC_ADDRSPC	xxx
Set SDRC mapping.	DMM_LISA_MAP_i[9:8] SDRC_MAP	xxx
Set SDRC address MSB.	DMM_LISA_MAP_i[7:0] SDRC_ADDR	xxx
Enable/disable DMM memory mapping lock.	DMM_LISA_LOCK[0] LOCK	xxx

15.2.5.3.4 Aliased Tiled View Orientation Settings and LUT Refill

The procedure in Table 15-30 provides the settings for aliased tiled view and LUT refill.

Table 15-30. Aliased Tiled View Orientation Settings and LUT Refill

Step	Register/Bit Field/Programming Model	Value
Set DMM TILER orientation for each initiator.	DMM_TILER_OR0 ORx DMM_TILER_OR1 ORx	xxx
Set DMM TILER write enable for the initiators.	DMM_TILER_OR0 Wx DMM_TILER_OR1 Wx	xxx
Define the base address of all view mappings.	DMM_PAT_VIEW_MAP_BASE[31] BASE_ADDR	xxx
DMM PAT initiator for synchronization	DMM_PAT_CTRL_i[31:28] INITIATOR	xxx
Set DMM PAT table reload synchronization.	DMM_PAT_CTRL_i[16] SYNC	xxx
Set DMM PAT LUT index (when more than one LUTs).	DMM_PAT_CTRL_i[9:8] LUT_ID	xxx
Define the direction of this PAT table refill (S Y X).	DMM_PAT_CTRL_i[6:4] DIRECTION	xxx
Start a PAT table refill.	DMM_PAT_CTRL_i[0] START	0x1

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15.2.5.3.5 Priority Settings

The procedure in Table 15-31 provides the sequence to set priorities.

Table 15-31. Priority Settings

Step	Register/Bit Field/Programming Model	Value
Set priority for each initiator.	DMM_PEG_PRIO_k Px	xxx
Set write enable for P_PAT field.	DMM_PEG_PRIO_PAT[4] W_PAT	xxx
Set priority for PAT engine.	DMM_PEG_PRIO_PAT[2:0] W_PAT	xxx

15.2.5.3.6 Error Handling

The procedure in Table 15-32 provides the sequence for error handling.

Table 15-32. Error Handling

Step	Register/Bit Field/Programming Model	Value
Enable interrupt for selected type of error.	DMM_PAT_IRQENABLE_SET[15:9] DMM_PAT_IRQENABLE_SET[7:0]	xxx
When interrupt occurs		
Disable type of error to handle.	DMM_PAT_IRQENABLE_CLR[15:9] DMM_PAT_IRQENABLE_CLR[7:0]	xxx
Check error status.	DMM_PAT_IRQSTATUS[15:9] DMM_PAT_IRQSTATUS[7:0]	xxx

15.2.5.3.7 PAT Programming Model

The PAT maps the tiled data anywhere in the 4-GiB physical address range, with a PAGE granularity. (The TILER page is the granularity of physical memory allocation in the TILER container. Each page is 4kiB).

A PAT view defines the kind of PAT to perform for each page, 8-, 16-, and 32-bit mode access. Each mode in each PAT view can be programmed in two different modes: direct translation and indirect translation.

15.2.5.3.7.1 PAT in Direct Translation Mode

In this mode, the PAT performs a translation of the 128-MiB virtual container as a whole in the physical address space (that is, in the SDRAM). This mode is used only for debug or in case of a DMM without a PAT.

15.2.5.3.7.2 PAT in Indirect Translation Mode

This is the most commonly used mode. In this mode, the PAT performs a translation of each 4-KiB page individually. In this way the 128-MiB virtual address space can be scattered in the whole 2 GiB of the physical address space. This is achieved by using a 32,678-word LUT that converts each page index (32,768 possible values) into 19 address bits that represent this page address in the physical memory. The main characteristic of this mode is there is no constraint on the use of the physical memory except that it is uses a multiple of 4-KiB areas located at 4-KiB boundaries in the physical memory. In this mode, the translation vector is in the internal 32-k entry PAT vector table at the index given by bits [26:12] of the input virtual address, and CONT_x = 0.

Programming sequence:

1. Set the DMM_PAT_VIEW0 register (or DMM_PAT_VIEW1, depending on the L3 CONN_ID of the initiator that is to perform the tiled accesses) with the appropriate value. For example, if the L3 CONN_ID equals 0, then the DMM_PAT_VIEW0 register must be programmed with the value 0x0000_0001 (PAT view 1 selected for initiator 0).
2. Set DMM_PAT_VIEW_MAP_BASE[31] = 0x8000_0000 (must always be programmed at 1 to select the upper 2 GiB of the physical address space that corresponds to the external memory).

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3. Set all 16-bit tiled accesses in indirect translation mode by setting at least the field ACCESS_16 to 1 (DMM_PAT_VIEW_MAP_1 = 0x0000_8000), program DMM_PAT_VIEW_MAP_1 at 0x8080_8080.

15.2.5.4 Addressing an Object in Tiled Mode

This section describes how a frame-buffer with a top-left pixel at (x0,y0) in the natural view container and a bottom right pixel at (x1,y1) in the natural view container is addressed in any tiled mode and orientation.

15.2.5.4.1 Frame-Buffer Addressing

NOTE: In this section, the (x,y) coordinates are given in pixel units.

Given an (S, $\overline{Y}$, $\overline{X}$) orientation, the (x,y) coordinates of the first pixel of the frame in the oriented view (where W = the width and H = the height in pixels of the container in the considered frame mode) is:

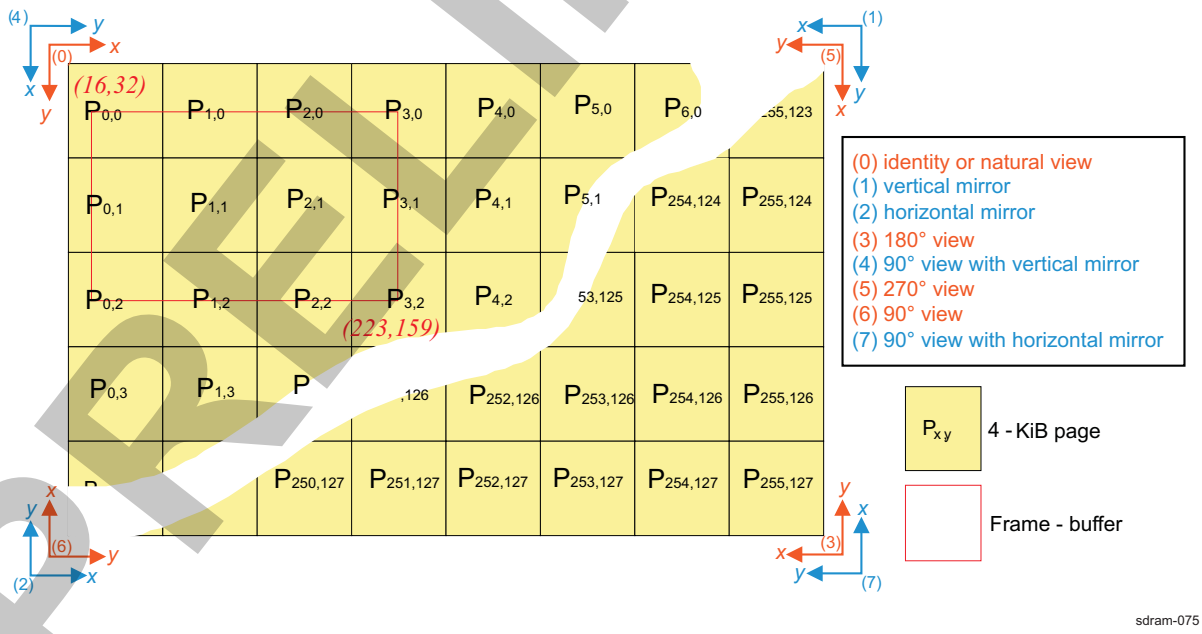
(x,y) = (x_{or}, y_{or}) when S, (y_{or}, x_{or}) otherwise
with:
x_{or} = x_0 when $\overline{X}$, W-1-x_1 otherwise
y_{or} = y_0 when $\overline{Y}$, H-1-y_1 otherwise

Given a (M_1, M_0) TILER mode where M_1 # 0 or M_0 # 0, the size in bytes of a pixel is 2^{2M1+M0}.

Therefore, given an (S, $\overline{Y}$, $\overline{X}$) orientation and a n(M_1, M_0) TILER mode where M_1 # 0 or M_0 # 0, the byte offset of the base address of the considered oriented frame in its container is:
base_address((x_0, y_0), (x_1, y_1), (S, $\overline{Y}$, $\overline{X}$), (M_1, M_0)) = (y_{or}W + x_{or}) P_5 when S, (x_{or}H + y_{or}) P_5 otherwise
with:
x_{or} = x_0 when $\overline{X}$, W-1-x_1 otherwise
y_{or} = y_0 when $\overline{Y}$, H-1-y_1 otherwise
P_5 = 2^{2M1+M0}

In its natural orientation, the TILER container consists of 8192 lines of 16,384 pixels of 8 bits, or 4096 lines of 16,384 pixels of 16 bits, or 4096 lines of 8192 pixels of 32 bits.

Figure 15-42. Example of 8-Bit Frame-Buffer Addressing in any Orientation



This frame-buffer address generation is independent from the page size. For instance, the 8-bit frame-buffer shown in Figure 15-42 that ranges from the top-left pixel at (16, 32) to the bottom-right pixel at (223, 159) in the natural orientation view, corresponds to the 29-bit view address offsets and full 33-bit TILER addresses given in Table 15-33.

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Table 15-33. 29-Bit View Address Offset and 33-Bit Full TILER Address for an 8-Bit Frame-Buffer

S	$\overline{Y}$	$\overline{X}$	x_{or}	y_{or}	29-Bit Address Offset in View	Full 33-Bit TILER Address
0	0	0	16	32	00080010h	100080010h
0	0	1	16,160	32	00083F20h	120083F20h
0	1	0	16	8032	07D80010h	147D80010h
0	1	1	16,160	8032	07D83F20h	167D83F20h
1	0	0	16	32	00020020h	180020020h
1	0	1	16,160	32	07E40020h	1A7E40020h
1	1	0	16	8032	00021F60h	1C0021F60h
1	1	1	16,160	8032	07E41F60h	1E7E41F60h

In this example the TILER is addressed in 8-bit mode, which translates to addresses with all mode bits (bits 27 and 28) cleared in the 29-bit address offset in view and in the full 33-bit TILER address.

15.2.5.4.2 TILER Page Mapping

Let:

- c (c = 0, 1, or 2) be the TILER page configuration (0 for 4-kiB pages, 1 for 16-kiB pages, and 2 for 64-kiB pages)
- (x_0, y_0) be the top-left pixel and (x_1, y_1) be the bottom-right pixel of a frame in its natural orientation
- W be the width and H the height in pixels of the container in the considered frame mode

The top-left page coordinates (P_{x0}, P_{y0}) and bottom-right page coordinates (P_{x1}, P_{y1}) that correspond to the frame are given by: $P_{x0} = (64.x_0.2^{2-c}) / W$, $P_{y0} = (32.y_0.2^{2-c}) / H$, $P_{x1} = (64.x_1.2^{2-c}) / W$ and $P_{y1} = (32.y_1.2^{2-c}) / H$.

In its natural orientation, the TILER container consists of 8192 lines of 16,384 pixels of 8 bits, or 4096 lines of 16,384 pixels of 16 bits, or 4096 lines of 8192 pixels of 32 bits.

NOTE: The page area type has the same structure as the DMM_PAT_AREA_i registers. For instance, the 8-bit frame-buffer described in Figure 15-42 and ranging from the top-left pixel at (16, 32) to the bottom-right pixel at (223, 159) in the natural orientation view, is mapped from the top-left page at P0,0 to the bottom-right page P3,2.

15.2.5.5 Addressing an Object in Page Mode

In page mode, the orientation modifies only the sequence of accessed pages, not their content. In this respect the orientation must be seen as a way to optimize the one-dimensional (1D) object allocation in a TILER container by allowing a 1D object spanning multiple pages to map a set of adjacent pages in any direction. For instance, a 1.25-MiB object, mapped on 320 pages of 4kiB can be allocated in a TILER container in any of the eight orientations (see Section 15.2.3.6.1.7.3, *Element Ordering in the TILER Container*).

The initial page can be chosen freely among all pages. In this respect, the address offset of a page in a TILER container is expressed as:

Let:

- c (c = 0, 1 or 2) be the TILER page configuration (0 for 4-kiB pages, 1 for 16-kiB pages, and 2 for 64-kiB pages)
- $(S, \overline{Y}, \overline{X})$ be the orientation of the considered 1D object in page mode
- (P_x, P_y) be the coordinate of the initial page in the natural orientation view

The byte offset of the base address of the considered initial page in its oriented container is:
$base\_address((P_x, P_y), (S, \overline{Y}, \overline{X})) = 4096.(64.y_{or}.2^{2-c} + x_{or}).2^{2.c}$ when S, $4096.(32.x_{or}.2^{2-c} + y_{or}).2^{2.c}$ otherwise with:
$x_{or} = P_x$ when $\overline{X}$, $64.2^{2-c}\text{-}1\text{-}P_x$ otherwise
$y_{or} = P_y$ when $\overline{Y}$, $32.2^{2-c}\text{-}1\text{-}P_y$ otherwise

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For instance, a 1D object starting from the page P32,63 in the natural orientation view on a DMM using 4-kiB pages, corresponds to the 29-bit view address offsets and full 33-bit TILER addresses given in Table 15-34.

Table 15-34. 29-Bit View Address Offset and 33-Bit Full TILER Address for a 1D Object

S	$\overline{Y}$	$\overline{X}$	x_{or}	y_{or}	29-Bit Address Offset in View	Full 33-Bit TILER Address
0	0	0	32	63	1BF20000h	11BF20000h
0	0	1	223	63	1BFDF000h	13BFDF000h
0	1	0	32	64	1C020000h	15C020000h
0	1	1	223	64	1C0DF000h	17C0DF000h
1	0	0	32	63	1903F000h	19903F000h
1	0	1	223	63	1EFBF000h	1BEFBF000h
1	1	0	32	64	19040000h	1D9040000h
1	1	1	223	64	1EFC0000h	1FEFC0000h

In this example the TILER is addressed in page mode, which translates to addresses with mode bits (bits 27 and 28) set in the 29-bit address offset in view and full 33-bit TILER address.

15.2.5.6 Sharing Containers Between Different Modes

When allocating objects in TILER containers, ensure that no two objects physically overlap.

In this respect, and to ease the object allocation and deallocation, it is strongly advised to share a TILER page only for different objects that do both of the following:

- Belong to the same mode
- Have the same lifetime (that is, are allocated and deallocated simultaneously)

Two objects of different modes can physically overlap if:

- One physical page is mapped twice in two different locations of the DMM LUT.
- The two objects share the DMM LUT and the intersection of their two page set is not empty.

  These two issues can be easily avoided by allocating a physical page only once in the DMM LUT.

  The second issue is a bit more difficult, especially if the allocation of objects in the various TILER containers must be dynamic. Managing the fragmentation within a flat memory model in a space-constrained system is not straightforward, and is the main reason for the existence of MMUs in most current processors, which adds yet another constraint to the problem (the y dimension, which makes it even more difficult).

Returning to the CPU-analogy, the memory fragmentation issue is mostly solved by using a virtual memory space larger than the actual physical memory space and a virtual-to-physical translation system. This allows contiguous virtual memory allocation when sufficient physical memory is available and the larger contiguous physical buffer is smaller than the requested memory allocation.

Similarly, the DMM answer to this object allocation in the TILER containers is two-fold:

- The DMM must have sufficient virtual address space in all modes to permit a static allocation of a pool of virtual buffers in all TILER modes for all TILER-aware initiators.
- Each TILER-aware initiator must dynamically manage its own pool of virtual buffers.

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15.2.6 DMM Register Manual

This section provides information about the DMM registers. Table 15-35 describes the DMM instance.

15.2.6.1 DMM Instance Summary

Table 15-35. DMM Instance Summary

Module Name	Base Address	Size
DMM	0x4E00 0000	32 MiB

15.2.6.2 DMM Registers

15.2.6.2.1 DMM Register Summary

Table 15-36 provides a summary of the DMM registers.

Table 15-36. DMM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address DMM
DMM_REVISION	R	32	0x0000 0000	0x4E00 0000
DMM_HWINFO	R	32	0x0000 0004	0x4E00 0004
DMM_LISA_HWINFO	R	32	0x0000 0008	0x4E00 0008
DMM_SYSCONFIG	RW	32	0x0000 0010	0x4E00 0010
DMM_LISA_LOCK	RW	32	0x0000 001C	0x4E00 001C
DMM_EMERGENCY	RW	32	0x0000 0020	0x4E00 0020
DMM_LISA_MAP_i (1)	RW	32	0x0000 0040 + (0x4 * i)	0x4E00 0040 + (0x4 * i)
DMM_TILER_HWINFO	R	32	0x0000 0208	0x4E00 0208
DMM_TILER_OR0	RW	32	0x0000 0220	0x4E00 0220
DMM_TILER_OR1	RW	32	0x0000 0224	0x4E00 0224
DMM_PAT_HWINFO	R	32	0x0000 0408	0x4E00 0408
DMM_PAT_GEOMETRY	R	32	0x0000 040C	0x4E00 040C
DMM_PAT_CONFIG	RW	32	0x0000 0410	0x4E00 0410
DMM_PAT_VIEW0	RW	32	0x0000 0420	0x4E00 0420
DMM_PAT_VIEW1	RW	32	0x0000 0424	0x4E00 0424
DMM_PAT_VIEW_MAP_i (1)	RW	32	0x0000 0440 + (0x4 * i)	0x4E00 0440 + (0x4 * i)
DMM_PAT_VIEW_MAP_BASE	RW	32	0x0000 0460	0x4E00 0460
DMM_PAT_IRQSTATUS_RAW	RW	32	0x0000 0480	0x4E00 0480
DMM_PAT_IRQSTATUS	RW	32	0x0000 0490	0x4E00 0490
DMM_PAT_IRQENABLE_SET	RW	32	0x0000 04A0	0x4E00 04A0
DMM_PAT_IRQENABLE_CLR	RW	32	0x0000 04B0	0x4E00 04B0
DMM_PAT_STATUS_i (1)	R	32	0x0000 04C0 + (0x4 * i)	0x4E00 04C0 + (0x4 * i)
DMM_PAT_DESCR_i (1)	RW	32	0x0000 0500 + (0x10 * i)	0x4E00 0500 + (0x10 * i)
DMM_PAT_AREA_i (1)	RW	32	0x0000 0504 + (0x10 * i)	0x4E00 0504 + (0x10 * i)
DMM_PAT_CTRL_i (1)	RW	32	0x0000 0508 + (0x10 * i)	0x4E00 0508 + (0x10 * i)
DMM_PAT_DATA_i (1)	RW	32	0x0000 050C + (0x10 * i)	0x4E00 050C + (0x10 * i)
DMM_PEG_HWINFO	R	32	0x0000 0608	0x4E00 0608
DMM_PEG_PRIO_k (2)	RW	32	0x0000 0620 + (0x4 * k)	0x4E00 0620 + (0x4 * k)

(1) i = 0 to 3 for DMM

(2) k = 0 to 7

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Table 15-36. DMM Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address DMM
DMM_PEG_PRIO_PAT	RW	32	0x0000 0640	0x4E00 0640

15.2.6.2.2 DMM Register Description

through describe the DMM registers.

Table 15-37. DMM_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4E00 0000	**Instance**	DMM
Description	DMM revision number		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	Revision number	R	0x-(1)

(1) TI internal data

Table 15-38. Register Call Summary for Register DMM_REVISION

Dynamic Memory Manager
- DMM Register Summary: [0]

Table 15-39. DMM_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4E00 0004	**Instance**	DMM
Description	DMM hardware configuration		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ROBIN_CNT				RESERVED				ELLA_CNT				RESERVED				TILER_CNT			

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:16	ROBIN_CNT	Number of ROBIN in the DMM	R	0x2
15:12	RESERVED	Reserved	R	0x0
11:8	ELLA_CNT	Number of ELLA in the DMM	R	0x0
7:4	RESERVED	Reserved	R	0x0
3:0	TILER_CNT	Number of TILER in the DMM	R	0x2

Table 15-40. Register Call Summary for Register DMM_HWINFO

Dynamic Memory Manager
- DMM Configuration: [0] [1]
- DMM Register Summary: [2]

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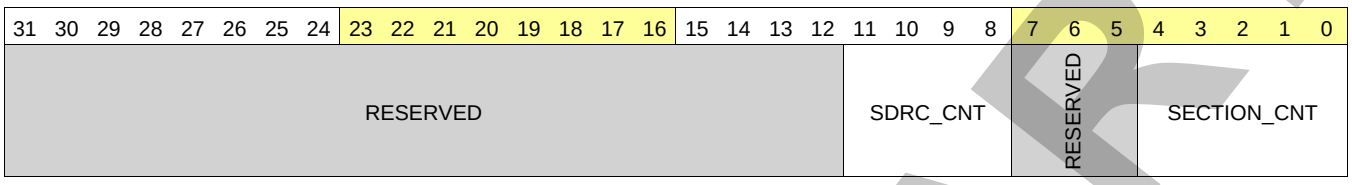
Table 15-41. DMM_LISA_HWINFO

Address Offset	0x0000 0008		
Physical Address	0x4E00 0008	**Instance**	DMM
Description	DMM hardware configuration for LISA		
Type	R		



Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:8	SDRC_CNT	Number of attached SDRAM controllers	R	0x2
7:5	RESERVED	Reserved	R	0x0
4:0	SECTION_CNT	Number of DMM sections	R	0x04

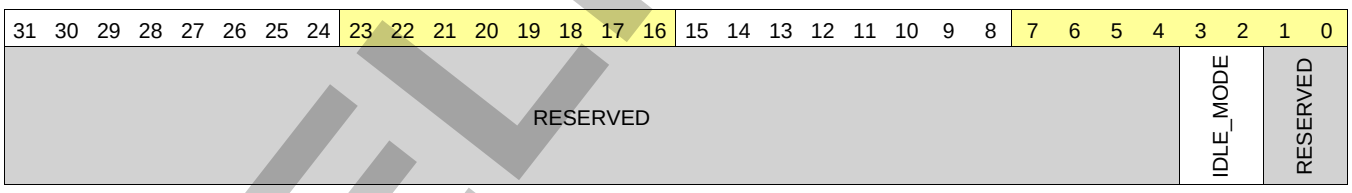
Table 15-42. Register Call Summary for Register DMM_LISA_HWINFO

Dynamic Memory Manager

- DMM Configuration: [0] [1]
- DMM Register Summary: [2]

Table 15-43. DMM_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4E00 0010	**Instance**	DMM
Description	DMM clock management configuration		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:2	IDLE_MODE	Configuration of the local target state management mode. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements. **Backup mode, for debug only.** 0x1: No-idle mode: local target never enters idle state. **Backup mode, for debug only.** 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Reserved	RW	0x2

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Bits	Field Name	Description	Type	Reset
1:0	RESERVED	Reserved	RW W0Only	0x0

Table 15-44. Register Call Summary for Register DMM_SYSCONFIG

Dynamic Memory Manager
- DMM Integration: [0]
- DMM Power Management: [1]
- DMM Module Global Initialization: [2]
- DMM Register Summary: [3]

Table 15-45. DMM_LISA_LOCK

Address Offset	0x0000 001C		
Physical Address	0x4E00 001C	**Instance**	DMM
Description	DMM memory mapping lock		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LOCK

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Should be written as 0	R	0x0000 0000
0	LOCK	DMM lock map Write 0x0: No effect (clear on reset only) Read 0x0: DMM_LISA_MAP_i unlocked Read 0x1: DMM_LISA_MAP_i locked Write 0x1: Locking DMM_LISA_MAP_i registers	RW	0

Table 15-46. Register Call Summary for Register DMM_LISA_LOCK

Dynamic Memory Manager
- DMM Integration: [0]
- Address Mapping: [1]
- LISA Description: [2]
- Interleaving Settings: [3]
- DMM Register Summary: [4]

Table 15-47. DMM_EMERGENCY

Address Offset	0x0000 0020		
Physical Address	0x4E00 0020	**Instance**	DMM
Description	DMM memory mapping register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WEIGHT								RESERVED															ENABLE

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Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved	R	0x000
20:16	WEIGHT	Weight for the LISA arbitration when any bit of the vector Mflag[63:0] is set. The recommendation is to set this field to 0x8 with ENABLE =1, after reset.	RW	0x04
15:1	Reserved	Reserved	R	0x0000
0	ENABLE	0: Emergency feature is disabled. 1: Enable the emergency feature. LISA arbitration priority is higher for the initiator that set Mflag input of this initiator. The recommendation is to enable the feature (=1) after reset.	RW	0

Table 15-48. Register Call Summary for Register DMM_EMERGENCY

Dynamic Memory Manager
- LISA Interconnect Arbitration: [0] [1] [2] [3] [4]
- DMM Register Summary: [5]

Table 15-49. DMM_LISA_MAP_i

Address Offset	0x0000 0040 + (0x4 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0040 + (0x4 * i)	**Instance**	DMM
Description	DMM memory mapping register		
Type	RW		

31 30 29 28 27 26 25 24	23	22 21 20	19 18	17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
SYS_ADDR	RESERVED	SYS_SIZE	SDRC_INTL	SDRC_ADDRSPC	RESERVED	SDRC_MAP	SDRC_ADDR

Bits	Field Name	Description	Type	Reset
31:24	SYS_ADDR	DMM system section address MSB for view mapping i	RW	0x00
23	RESERVED	Reserved	RW W0Only	0
22:20	SYS_SIZE	DMM system section size for view mapping i 0x0: 16-MiB section 0x1: 32-MiB section 0x2: 64-MiB section 0x3: 128-MiB section 0x4: 256-MiB section 0x5: 512-MiB section 0x6: 1-GiB section 0x7: 2-GiB section	RW	0x0

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Bits	Field Name	Description	Type	Reset
19:18	SDRC_INTL	SDRAM controller interleaving mode 0x0: No interleaving 0x1: 128-byte interleaving 0x2: 256-byte interleaving 0x3: 512-byte interleaving The 128-/256-/512-byte interleaving applies only to nontiled regions. If accesses are made to tiled regions, interleaving is forced to 1kiB. SDRC_INTL is don't care if SDRC_MAP is not 0x3 (no interleaving).	RW	0x0
17:16	SDRC_ADDRSPC	SDRAM controller address space for view mapping i	RW	0x0
15:10	RESERVED	Reserved	RW W0Only	0x00
9:8	SDRC_MAP	SDRAM controller mapping for view mapping i 0x0: Unmapped 0x1: Mapped on EMIF1 only (not interleaved) 0x2: Mapped on EMIF2 only (not interleaved) 0x3: Mapped on EMIF1 and EMIF2 (interleaved) To enable interleaving, SDRC_MAP must be 0x3 and SDRC_INTL must be a nonzero value.	RW	0
7:0	SDRC_ADDR	SDRAM controller address MSB for view mapping i	RW	0x00

Table 15-50. Register Call Summary for Register DMM_LISA_MAP_i

Dynamic Memory Manager

- DMM Integration: [0]
- Dynamic Mapping: [1]
- Address Mapping: [2] [3]
- LISA Description: [4] [5]
- Interleaving Settings: [6] [7] [8] [9] [10] [11]
- DMM Register Summary: [12]
- DMM Register Description: [13] [14] [15]

Table 15-51. DMM_TILER_HWINFO

Address Offset	0x0000 0208		
Physical Address	0x4E00 0208	**Instance**	DMM
Description	DMM hardware configuration for TILER		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								OR_CNT							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x000 0000
6:0	OR_CNT	Number of TILER orientation entries Read 0x4: Four orientation entries Read 0x20: Thirty-two orientation entries Read 0x40: Sixty-four orientation entries Read 0x2: Two orientation entries Read 0x1: One orientation entry Read 0x8: Eight orientation entries Read 0x10: Sixteen orientation entries	R	0x10

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Table 15-52. Register Call Summary for Register DMM_TILER_HWINFO

Dynamic Memory Manager

- DMM Configuration: [0]
- DMM Register Summary: [1]

Table 15-53. DMM_TILER_OR0

Address Offset	0x0000 02200	**Index**	0
Physical Address	0x4E00 0220	**Instance**	DMM
Description	DMM TILER orientation (initiators 0 to 7)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W7	OR7			W6	OR6			W5	OR5			W4	OR4			W3	OR3			W2	OR2			W1	OR1			W0	OR0		

Bits	Field Name	Description	Type	Reset
31	W7	Write-enable for OR7 bit field Write 0x0: OR7 field is unchanged. Write 0x1: OR7 field is updated.	RW	0
30:28	OR7	Orientation for initiator 7	RW	0x0
27	W6	Write-enable for OR6 bit field Write 0x0: OR6 field is unchanged. Write 0x1: OR6 field is updated.	RW	0
26:24	OR6	Orientation for initiator 6	RW	0x0
23	W5	Write-enable for OR5 bit field Write 0x0: OR5 field is unchanged. Write 0x1: OR5 field is updated.	RW	0
22:20	OR5	Orientation for initiator 5	RW	0x0
19	W4	Write-enable for OR4 bit field Write 0x0: OR4 field is unchanged. Write 0x1: OR4 field is updated.	RW	0
18:16	OR4	Orientation for initiator 4	RW	0x0
15	W3	Write-enable for OR3 bit field Write 0x0: OR3 field is unchanged. Write 0x1: OR3 field is updated.	RW	0
14:12	OR3	Orientation for initiator 3	RW	0x0
11	W2	Write-enable for OR2 bit field Write 0x0: OR2 field is unchanged. Write 0x1: OR2 field is updated.	RW	0
10:8	OR2	Orientation for initiator 2	RW	0x0
7	W1	Write-enable for OR1 bit field Write 0x0: OR1 field is unchanged. Write 0x1: OR1 field is updated.	RW	0
6:4	OR1	Orientation for initiator 1	RW	0x0
3	W0	Write-enable for OR0 bit field Write 0x0: OR0 field is unchanged. Write 0x1: OR0 field is updated.	RW	0
2:0	OR0	Orientation for initiator 0	RW	0x0

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Table 15-54. Register Call Summary for Register DMM_TILER_OR0

Dynamic Memory Manager

- DMM Integration: [0]
- TILER Macro-Architecture: [1] [2]
- Aliased Tiled View Orientation Settings and LUT Refill: [3] [4]
- DMM Register Summary: [5]

Table 15-55. DMM_TILER_OR1

Address Offset	0x0000 02204	**Index**	0
Physical Address	0x4E00 0224	**Instance**	DMM
Description	DMM TILER orientation (initiators 8 to 15)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W15	OR15			W14	OR14			W13	OR13			W12	OR12			W11	OR11			W10	OR10			W9	OR9			W8	OR8		

Bits	Field Name	Description	Type	Reset
31	W15	Write-enable for OR15 bit field Write 0x0: OR15 field is unchanged. Write 0x1: OR15 field is updated.	RW	0
30:28	OR15	Orientation for initiator 15	RW	0x0
27	W14	Write-enable for OR14 bit field Write 0x0: OR14 field is unchanged. Write 0x1: OR14 field is updated.	RW	0
26:24	OR14	Orientation for initiator 14	RW	0x0
23	W13	Write-enable for OR13 bit field Write 0x0: OR13 field is unchanged. Write 0x1: OR13 field is updated.	RW	0
22:20	OR13	Orientation for initiator 13	RW	0x0
19	W12	Write-enable for OR12 bit field Write 0x0: OR12 field is unchanged. Write 0x1: OR12 field is updated.	RW	0
18:16	OR12	Orientation for initiator 12	RW	0x0
15	W11	Write-enable for OR11 bit field Write 0x0: OR11 field is unchanged. Write 0x1: OR11 field is updated.	RW	0
14:12	OR11	Orientation for initiator 11	RW	0x0
11	W10	Write-enable for OR10 bit field Write 0x0: OR10 field is unchanged. Write 0x1: OR10 field is updated.	RW	0
10:8	OR10	Orientation for initiator 10	RW	0x0
7	W9	Write-enable for OR9 bit field Write 0x0: OR9 field is unchanged. Write 0x1: OR9 field is updated.	RW	0
6:4	OR9	Orientation for initiator 9	RW	0x0
3	W8	Write-enable for OR8 bit field Write 0x0: OR8 field is unchanged. Write 0x1: OR8 field is updated.	RW	0
2:0	OR8	Orientation for initiator 8	RW	0x0

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Table 15-56. Register Call Summary for Register DMM_TILER_OR1

Dynamic Memory Manager

- DMM Integration: [0]
- TILER Macro-Architecture: [1] [2]
- Aliased Tiled View Orientation Settings and LUT Refill: [3] [4]
- DMM Register Summary: [5]

Table 15-57. DMM_PAT_HWINFO

Address Offset	0x0000 0408		
Physical Address	0x4E00 0408	**Instance**	DMM
Description	DMM hardware configuration for PAT		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ENGINE_CNT					RESERVED			LUT_CNT					RESERVED				VIEW_MAP_CNT				RESERVED	VIEW_CNT						

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Reserved	R	0x0
28:24	ENGINE_CNT	Number of PAT refill engines	R	0x04
23:21	RESERVED	Reserved	R	0x0
20:16	LUT_CNT	Number of PAT LUT for page-grained physical address translation	R	0x01
15:12	RESERVED	Reserved	R	0x0
11:8	VIEW_MAP_CNT	Number of internal PAT view mappings. Read 0x1: One view map Read 0x2: Two view maps Read 0x4: Four view maps Read 0x8: Eight view maps	R	0x4
7	RESERVED	Reserved	R	0
6:0	VIEW_CNT	Number of PAT view entries Read 0x1: One view entry Read 0x2: Two view entries Read 0x4: Four view entries Read 0x8: Eight view entries Read 0x10: Sixteen view entries Read 0x20: Thirty-two view entries Read 0x40: Sixty-four view entries	R	0x10

Table 15-58. Register Call Summary for Register DMM_PAT_HWINFO

Dynamic Memory Manager

- DMM Configuration: [0] [1] [2] [3]
- DMM Register Summary: [4]

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Table 15-59. DMM_PAT_GEOMETRY

Address Offset	0x0000 040C		
Physical Address	0x4E00 040C	**Instance**	DMM
Description	PAT geometry-related settings		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					CONT_HGHT			RESERVED				CONT_WDTH				RESERVED		ADDR_RANGE						RESERVED			PAGE_SZ				

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26:24	CONT_HGHT	Container height in pages Read 0x1: Container height of 32 pages Read 0x2: Container height of 64 pages Read 0x4: Container height of 128 pages Read 0x8: Container height of 256 pages	R	0x8
23:20	RESERVED	Reserved	R	0x0
19:16	CONT_WDTH	Container width in pages Read 0x2: Container width of 64 pages Read 0x4: Container width of 128 pages Read 0x8: Container width of 256 pages	R	0x8
15:14	RESERVED	Reserved	R	0x0
13:8	ADDR_RANGE	PAT output physical address range Read 0x1: 128-MiB range Read 0x2: 256-MiB range Read 0x4: 512-MiB range Read 0x8: 1-GiB range Read 0x10: 2-GiB range Read 0x20: 4-GiB range	R	0x10
7:5	RESERVED	Reserved	R	0x0
4:0	PAGE_SZ	Page size in 4-kiB granularity Read 0x1: 4-kiB page Read 0x4: 16-kiB page Read 0x10: 64-kiB page	R	0x01

Table 15-60. Register Call Summary for Register DMM_PAT_GEOMETRY

Dynamic Memory Manager

- DMM Configuration: [0] [1] [2] [3]
- DMM Register Summary: [4]

Table 15-61. DMM_PAT_CONFIG

Address Offset	0x0000 0410		
Physical Address	0x4E00 0410	**Instance**	DMM
Description	This is the PAT configuration register aimed at defining the major PAT configuration of each refill engine.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE3	MODE2	MODE1	MODE0

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	MODE3	Mode of refill engine 3 0: Normal mode 1: Direct LUT access	RW	0
2	MODE2	Mode of refill engine 2 0: Normal mode 1: Direct LUT access	RW	0
1	MODE1	Mode of refill engine 1 0: Normal mode 1: Direct LUT access	RW	0
0	MODE0	Mode of refill engine 0 0: Normal mode 1: Direct LUT access	RW	0

Table 15-62. Register Call Summary for Register DMM_PAT_CONFIG

Dynamic Memory Manager

- Address Translation: [0]
- Configuration Settings and LUT Refill: [1] [2]
- DMM Register Summary: [3]

Table 15-63. DMM_PAT_VIEW0

Address Offset	0x0000 0420	**Index**	
Physical Address	0x4E00 0420	**Instance**	DMM
Description	DMM PAT View register (initiators 0 to 7)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W7	RESERVED	V7		W6	RESERVED	V6		W5	RESERVED	V5		W4	RESERVED	V4		W3	RESERVED	V3		W2	RESERVED	V2		W1	RESERVED	V1		W0	RESERVED	V0	

Bits	Field Name	Description	Type	Reset
31	W7	Write-enable for V7 bit field Write 0x0: V7 field is unchanged. Write 0x1: V7 field is updated.	RW	0
30	RESERVED	Reserved	RW W0Only	0
29:28	V7	PAT view for initiator 7	RW	0x0
27	W6	Write-enable for V6 bit field Write 0x0: V6 field is unchanged. Write 0x1: V6 field is updated.	RW	0
26	RESERVED	Reserved	RW W0Only	0

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Bits	Field Name	Description	Type	Reset
25:24	V6	PAT view for initiator 6	RW	0x0
23	W5	Write-enable for V5 bit field Write 0x0: V5 field is unchanged. Write 0x1: V5 field is updated.	RW	0
22	RESERVED	Reserved	RW W0Only	0
21:20	V5	PAT view for initiator 5	RW	0x0
19	W4	Write-enable for V4 bit field Write 0x0: V4 field is unchanged. Write 0x1: V4 field is updated.	RW	0
18	RESERVED	Reserved	RW W0Only	0
17:16	V4	PAT view for initiator 4	RW	0x0
15	W3	Write-enable for V3 bit field Write 0x0: V3 field is unchanged. Write 0x1: V3 field is updated.	RW	0
14	RESERVED	Reserved	RW W0Only	0
13:12	V3	PAT view for initiator 3	RW	0x0
11	W2	Write-enable for V2 bit field Write 0x0: V2 field is unchanged. Write 0x1: V2 field is updated.	RW	0
10	RESERVED	Reserved	RW W0Only	0
9:8	V2	PAT view for initiator 2	RW	0x0
7	W1	Write-enable for V1 bit field Write 0x0: V1 field is unchanged. Write 0x1: V1 field is updated.	RW	0
6	RESERVED	Reserved	RW W0Only	0
5:4	V1	PAT view for initiator 1	RW	0x0
3	W0	Write-enable for V0 bit field Write 0x0: V0 field is unchanged. Write 0x1: V0 field is updated.	RW	0
2	RESERVED	Reserved	RW W0Only	0
1:0	V0	PAT view for initiator 0	RW	0x0

Table 15-64. Register Call Summary for Register DMM_PAT_VIEW0

Dynamic Memory Manager

- DMM Integration: [0]
- Address Translation: [1] [2]
- Configuration Settings and LUT Refill: [3] [4]
- PAT in Indirect Translation Mode: [5] [6]
- DMM Register Summary: [7]

Table 15-65. DMM_PAT_VIEW1

Address Offset	0x0000 0424	**Index**	
Physical Address	0x4E00 0424	**Instance**	DMM
Description	DMM PAT view register (initiators 8 to 15)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W15	RESERVED	V15		W14	RESERVED	V14		W13	RESERVED	V13		W12	RESERVED	V12		W11	RESERVED	V11		W10	RESERVED	V10		W9	RESERVED	V9		W8	RESERVED	V8	

Bits	Field Name	Description	Type	Reset
31	W15	Write-enable for V15 bit field Write 0x0: V15 field is unchanged. Write 0x1: V15 field is updated.	RW	0
30	RESERVED	Reserved	RW W0Only	0
29:28	V15	PAT view for initiator 15	RW	0x0
27	W14	Write-enable for V14 bit field Write 0x0: V14 field is unchanged. Write 0x1: V14 field is updated.	RW	0
26	RESERVED	Reserved	RW W0Only	0
25:24	V14	PAT view for initiator 14	RW	0x0
23	W13	Write-enable for V13 bit field Write 0x0: V13 field is unchanged. Write 0x1: V13 field is updated.	RW	0
22	RESERVED	Reserved	RW W0Only	0
21:20	V13	PAT view for initiator 13	RW	0x0
19	W12	Write-enable for V12 bit field Write 0x0: V12 field is unchanged. Write 0x1: V12 field is updated.	RW	0
18	RESERVED	Reserved	RW W0Only	0
17:16	V12	PAT view for initiator 12	RW	0x0
15	W11	Write-enable for V11 bit field Write 0x0: V11 field is unchanged. Write 0x1: V11 field is updated.	RW	0
14	RESERVED	Reserved	RW W0Only	0
13:12	V11	PAT view for initiator 11	RW	0x0
11	W10	Write-enable for V10 bit field Write 0x0: V10 field is unchanged. Write 0x1: V10 field is updated.	RW	0
10	RESERVED	Reserved	RW W0Only	0
9:8	V10	PAT view for initiator 10	RW	0x0
7	W9	Write-enable for V9 bit field Write 0x0: V9 field is unchanged. Write 0x1: V9 field is updated.	RW	0
6	RESERVED	Reserved	RW W0Only	0
5:4	V9	PAT view for initiator 9	RW	0x0
3	W8	Write-enable for V8 bit field Write 0x0: V8 field is unchanged. Write 0x1: V8 field is updated.	RW	0

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Bits	Field Name	Description	Type	Reset
2	RESERVED	Reserved	RW W0Only	0
1:0	V8	PAT view for initiator 8	RW	0x0

Table 15-66. Register Call Summary for Register DMM_PAT_VIEW1

Dynamic Memory Manager

- DMM Integration: [0]
- Address Translation: [1] [2]
- Configuration Settings and LUT Refill: [3] [4]
- PAT in Indirect Translation Mode: [5]
- DMM Register Summary: [6]

Table 15-67. DMM_PAT_VIEW_MAP_i

Address Offset	0x0000 0440 + (0x4 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0440 + (0x4 * i)	**Instance**	DMM
Description	PAT view mapping register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCESS_PAGE	RESERVED							CONT_PAGE								ACCESS_32	RESERVED							CONT_32								ACCESS_16	RESERVED							CONT_16								ACCESS_8	RESERVED							CONT_8							

Bits	Field Name	Description	Type	Reset
31	ACCESS_PAGE	Kind of access for this page mode container in view mapping i 0x0: Direct access, container base address given in CONT_PAGE 0x1: indirect access through the LUT indexed by CONT_PAGE	RW	0
30:27	RESERVED	Reserved	RW W0Only	0x0
26:24	CONT_PAGE	Container for page mode in view mapping i	RW	0x0
23	ACCESS_32	Kind of access for this 32-bit mode container in view mapping i 0x0: Direct access, container base address given in CONT_32 0x1: indirect access through the LUT indexed by CONT_32	RW	0
22:19	RESERVED	Reserved	RW W0Only	0x0
18:16	CONT_32	Container for 32-bit mode in view mapping i	RW	0x0
15	ACCESS_16	Kind of access for this 16-bit mode container in view mapping i 0x0: Direct access, container base address given in CONT_16 0x1: indirect access through the LUT indexed by CONT_16	RW	0
14:11	RESERVED	Reserved	RW W0Only	0x0
10:8	CONT_16	Container for 16-bit mode in view mapping i	RW	0x0

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Bits	Field Name	Description	Type	Reset
7	ACCESS_8	Kind of access for this 8-bit mode container in view mapping i 0x0: Direct access, container base address given in CONT_8 0x1: indirect access through the LUT indexed by CONT_8	RW	0
6:3	RESERVED	Reserved	RW W0Only	0x0
2:0	CONT_8	Container for 8-bit mode in view mapping i	RW	0x0

Table 15-68. Register Call Summary for Register DMM_PAT_VIEW_MAP_i

Dynamic Memory Manager
- DMM Integration: [0]
- Address Translation: [1] [2] [3] [4] [5] [6] [7]
- Configuration Settings and LUT Refill: [8]
- DMM Register Summary: [9]

Table 15-69. DMM_PAT_VIEW_MAP_BASE

Address Offset	0x0000 0460		
Physical Address	0x4E00 0460	**Instance**	DMM
Description	Base address of all view mappings		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE_ADDR	RESERVED																														

Bits	Field Name	Description	Type	Reset
31	BASE_ADDR	MSB of the PAT view mapping base address	RW	0
30:0	RESERVED	Reserved	RW W0Only	0x0000 0000

Table 15-70. Register Call Summary for Register DMM_PAT_VIEW_MAP_BASE

Dynamic Memory Manager
- DMM Integration: [0]
- Address Translation: [1]
- Configuration Settings and LUT Refill: [2]
- Aliased Tiled View Orientation Settings and LUT Refill: [3]
- PAT in Indirect Translation Mode: [4]
- DMM Register Summary: [5]

Table 15-71. DMM_PAT_IRQSTATUS_RAW

Address Offset	0x0000 0480		
Physical Address	0x4E00 0480	**Instance**	DMM
Description	Per-event raw interrupt status vector. Raw status is set even if the related event is not enabled. Write 1 to set the (raw) status, mostly for debug. n = 0 for the first interrupt status raw register, n = 1 for the second interrupt status raw register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_LUT_MISS3	ERR_UPD_DATA3	ERR_UPD_CTRL3	ERR_UPD_AREA3	ERR_INV_DATA3	ERR_INV_DSC3	FILL_LST3	FILL_DSC3	ERR_LUT_MISS2	ERR_UPD_DATA2	ERR_UPD_CTRL2	ERR_UPD_AREA2	ERR_INV_DATA2	ERR_INV_DSC2	FILL_LST2	FILL_DSC2	ERR_LUT_MISS1	ERR_UPD_DATA1	ERR_UPD_CTRL1	ERR_UPD_AREA1	ERR_INV_DATA1	ERR_INV_DSC1	FILL_LST1	FILL_DSC1	ERR_LUT_MISS0	ERR_UPD_DATA0	ERR_UPD_CTRL0	ERR_UPD_AREA0	ERR_INV_DATA0	ERR_INV_DSC0	FILL_LST0	FILL_DSC0

Bits	Field Name	Description	Type	Reset
31	ERR_LUT_MISS3	Access to a yet-to-be-refilled area event in area 4.n+3 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
30	ERR_UPD_DATA3	Data register update whilst refilling error event in area 4.n+3 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
29	ERR_UPD_CTRL3	Control register update whilst refilling error event in area 4.n+3 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
28	ERR_UPD_AREA3	Area register update whilst refilling error event in area 4.n+3 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
27	ERR_INV_DATA3	Invalid entry-table pointer error event in area 4.n+3 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event.	RW W1toSet	0
26	ERR_INV_DSC3	Invalid descriptor pointer error event in area 4.n+3 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
25	FILL_LST3	End of refill event for the last descriptor in area 4.n+3 Write 0x0: Keep area 3 refill done event. Write 0x1: Set area 3 refill done event. Read 0x1: Area 3 is refilled. Read 0x0: Area 3 is yet-to-be refilled.	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
24	FILL_DSC3	End of refill event for any descriptor in area 4.n+3 Write 0x0: Keep area 3 refill done event. Write 0x1: Set area 3 refill done event. Read 0x1: Area 3 is refilled. Read 0x0: Area 3 is yet-to-be refilled.	RW W1toSet	0
23	ERR_LUT_MISS2	Access to a yet-to-be-refilled area event in area 4.n+2 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
22	ERR_UPD_DATA2	Data register update whilst refilling error event in area 4.n+2 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
21	ERR_UPD_CTRL2	Control register update whilst refilling error event in area 4.n+2 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
20	ERR_UPD_AREA2	Area register update whilst refilling error event in area 4.n+2 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
19	ERR_INV_DATA2	Invalid entry-table pointer error event in area 4.n+2 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
18	ERR_INV_DSC2	Invalid descriptor pointer error event in area 4.n+2 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
17	FILL_LST2	End of refill event for the last descriptor in area 4.n+2 Write 0x0: Keep area 2 refill done event. Write 0x1: Set area 2 refill done event. Read 0x1: Area 2 is refilled. Read 0x0: Area 2 is yet-to-be refilled.	RW W1toSet	0
16	FILL_DSC2	End of refill event for any descriptor in area 4.n+2 Write 0x0: Keep area 2 refill done event. Write 0x1: Set area 2 refill done event. Read 0x1: Area 2 is refilled. Read 0x0: Area 2 is yet-to-be refilled.	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
15	ERR_LUT_MISS1	Access to a yet-to-be-refilled area event in area 4.n+1 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
14	ERR_UPD_DATA1	Data register update whilst refilling error event in area 4.n+1 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
13	ERR_UPD_CTRL1	Control register update whilst refilling error event in area 4.n+1 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
12	ERR_UPD_AREA1	Area register update whilst refilling error event in area 4.n+1 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
11	ERR_INV_DATA1	Invalid entry-table pointer error event in area 4.n+1 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
10	ERR_INV_DSC1	Invalid descriptor pointer error event in area 4.n+1 Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
9	FILL_LST1	End of refill event for the last descriptor in area 4.n+1 Write 0x0: Keep area 1 refill done event. Write 0x1: Set area 1 refill done event. Read 0x1: Area 1 is refilled. Read 0x0: Area 1 is yet-to-be refilled.	RW W1toSet	0
8	FILL_DSC1	End of refill event for any descriptor in area 4.n+1 Write 0x0: Keep area 1 refill done event. Write 0x1: Set area 1 refill done event. Read 0x1: Area 1 is refilled. Read 0x0: Area 1 is yet-to-be refilled.	RW W1toSet	0
7	ERR_LUT_MISS0	Access to a yet-to-be-refilled area event in area 4.n Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
6	ERR_UPD_DATA0	Data register update whilst refilling error event in area 4.n Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
5	ERR_UPD_CTRL0	Control register update whilst refilling error event in area 4.n Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
4	ERR_UPD_AREA0	Area register update whilst refilling error event in area 4.n Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
3	ERR_INV_DATA0	Invalid entry-table pointer error event in area 4.n Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
2	ERR_INV_DSC0	Invalid descriptor pointer error event in area 4.n Write 0x0: Keep current error event. Write 0x1: Set error event. Read 0x1: Error event happened. Read 0x0: No such error event	RW W1toSet	0
1	FILL_LST0	End of refill event for the last descriptor in area 4.n Write 0x0: Keep area 0 refill done event. Write 0x1: Set area 0 refill done event. Read 0x1: Area 0 is refilled. Read 0x0: Area 0 is yet-to-be refilled.	RW W1toSet	0
0	FILL_DSC0	End of refill event for any descriptor in area 4.n Write 0x0: Keep area 0 refill done event. Write 0x1: Set area 0 refill done event. Read 0x1: Area 0 is refilled. Read 0x0: Area 0 is yet-to-be refilled.	RW W1toSet	0

Table 15-72. Register Call Summary for Register DMM_PAT_IRQSTATUS_RAW

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- DMM Register Summary: [32]

Table 15-73. DMM_PAT_IRQSTATUS

Address Offset	0x0000 0490		
Physical Address	0x4E00 0490	**Instance**	DMM
Description	Per-event "enabled" interrupt status vector. Enabled status is not set unless the event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). n = 0 for the first interrupt status register, n = 1 for the second interrupt status register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_LUT_MISS3	ERR_UPD_DATA3	ERR_UPD_CTRL3	ERR_UPD_AREA3	ERR_INV_DATA3	ERR_INV_DSC3	FILL_LST3	FILL_DSC3	ERR_LUT_MISS2	ERR_UPD_DATA2	ERR_UPD_CTRL2	ERR_UPD_AREA2	ERR_INV_DATA2	ERR_INV_DSC2	FILL_LST2	FILL_DSC2	ERR_LUT_MISS1	ERR_UPD_DATA1	ERR_UPD_CTRL1	ERR_UPD_AREA1	ERR_INV_DATA1	ERR_INV_DSC1	FILL_LST1	FILL_DSC1	ERR_LUT_MISS0	ERR_UPD_DATA0	ERR_UPD_CTRL0	ERR_UPD_AREA0	ERR_INV_DATA0	ERR_INV_DSC0	FILL_LST0	FILL_DSC0

Bits	Field Name	Description	Type	Reset
31	ERR_LUT_MISS3	Access to a yet-to-be-refilled area event in area 4.n+3 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
30	ERR_UPD_DATA3	Data register update whilst refilling error event in area 4.n+3 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
29	ERR_UPD_CTRL3	Control register update whilst refilling error event in area 4.n+3 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
28	ERR_UPD_AREA3	Area register update whilst refilling error event in area 4.n+3 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
27	ERR_INV_DATA3	Invalid entry-table pointer error event in area 4.n+3 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
26	ERR_INV_DSC3	Invalid descriptor pointer error event in area 4.n+3 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
25	FILL_LST3	End of refill event for the last descriptor in area 4.n+3 Write 0x0: Keep current area refill done maskable event. Write 0x1: Clear current area refill done maskable event. Read 0x1: Current area is refilled. Read 0x0: Current area is yet-to-be refilled or this event is masked.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
24	FILL_DSC3	End of refill event for any descriptor in area 4.n+3 Write 0x0: Keep current area refill done maskable event. Write 0x1: Clear current area refill done maskable event. Read 0x1: Current area is refilled. Read 0x0: Current area is yet-to-be refilled or this event is masked.	RW W1toClr	0
23	ERR_LUT_MISS2	Access to a yet-to-be-refilled area event in area 4.n+2 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
22	ERR_UPD_DATA2	Data register update whilst refilling error event in area 2 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
21	ERR_UPD_CTRL2	Control register update whilst refilling error event in area 4.n+2 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
20	ERR_UPD_AREA2	Area register update whilst refilling error event in area 4.n+2 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
19	ERR_INV_DATA2	Invalid entry-table pointer error event in area 4.n+2 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
18	ERR_INV_DSC2	Invalid descriptor pointer error event in area 4.n+2 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
17	FILL_LST2	End of refill event for the last descriptor in area 4.n+2 Write 0x0: Keep current area refill done maskable event. Write 0x1: Clear current area refill done maskable event. Read 0x1: Current area is refilled. Read 0x0: Current area is yet-to-be refilled or this event is masked.	RW W1toClr	0
16	FILL_DSC2	End of refill event for any descriptor in area 4.n+2 Write 0x0: Keep current area refill done maskable event. Write 0x1: Clear current area refill done maskable event. Read 0x1: Current area is refilled. Read 0x0: Current area is yet-to-be refilled or this event is masked.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
15	ERR_LUT_MISS1	Access to a yet-to-be-refilled area event in area 4.n+1 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
14	ERR_UPD_DATA1	Data register update whilst refilling error event in area 4.n+1 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
13	ERR_UPD_CTRL1	Control register update whilst refilling error event in area 4.n+1 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
12	ERR_UPD_AREA1	Area register update whilst refilling error event in area 4.n+1 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
11	ERR_INV_DATA1	Invalid entry-table pointer error event in area 4.n+1 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked	RW W1toClr	0
10	ERR_INV_DSC1	Invalid descriptor pointer error event in area 4.n+1 Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked	RW W1toClr	0
9	FILL_LST1	End of refill event for the last descriptor in area 4.n+1 Write 0x0: Keep current area refill done maskable event. Write 0x1: Clear current area refill done maskable event. Read 0x1: Current area is refilled. Read 0x0: Current area is yet-to-be refilled or this event is masked.	RW W1toClr	0
8	FILL_DSC1	End of refill event for any descriptor in area 4.n+1 Write 0x0: Keep current area refill done maskable event. Write 0x1: Clear current area refill done maskable event. Read 0x1: Current area is refilled. Read 0x0: Current area is yet-to-be refilled or this event is masked.	RW W1toClr	0
7	ERR_LUT_MISS0	Access to a yet-to-be-refilled area event in area 4.n Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
6	ERR_UPD_DATA0	Data register update whilst refilling error event in area 4.n Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
5	ERR_UPD_CTRL0	Control register update whilst refilling error event in area 4.n Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
4	ERR_UPD_AREA0	Area register update whilst refilling error event in area 4.n Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
3	ERR_INV_DATA0	Invalid entry-table pointer error event in area 4.n Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
2	ERR_INV_DSC0	Invalid descriptor pointer error event in area 4.n Write 0x0: Keep current maskable error event. Write 0x1: Clear this maskable error event. Read 0x1: Error event happened. Read 0x0: No such error event or this event is masked.	RW W1toClr	0
1	FILL_LST0	End of refill event for the last descriptor in area 4.n Write 0x0: Keep current area refill done maskable event. Write 0x1: Clear current area refill done maskable event. Read 0x1: Current area is refilled. Read 0x0: Current area is yet-to-be refilled or this event is masked.	RW W1toClr	0
0	FILL_DSC0	End of refill event for any descriptor in area 4.n Write 0x0: Keep current area refill done maskable event. Write 0x1: Clear current area refill done maskable event. Read 0x1: Current area is refilled. Read 0x0: Current area is yet-to-be refilled or this event is masked.	RW W1toClr	0

Table 15-74. Register Call Summary for Register DMM_PAT_IRQSTATUS

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- Error Handling: [32] [33]
- DMM Register Summary: [34]

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Table 15-75. DMM_PAT_IRQENABLE_SET

Address Offset	0x0000 04A0		
Physical Address	0x4E00 04A0	**Instance**	DMM
Description	Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register. n = 0 for the first interrupt enable set register, n = 1 for the second interrupt enable set register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_LUT_MISS3	ERR_UPD_DATA3	ERR_UPD_CTRL3	ERR_UPD_AREA3	ERR_INV_DATA3	ERR_INV_DSC3	FILL_LST3	FILL_DSC3	ERR_LUT_MISS2	ERR_UPD_DATA2	ERR_UPD_CTRL2	ERR_UPD_AREA2	ERR_INV_DATA2	ERR_INV_DSC2	FILL_LST2	FILL_DSC2	ERR_LUT_MISS1	ERR_UPD_DATA1	ERR_UPD_CTRL1	ERR_UPD_AREA1	ERR_INV_DATA1	ERR_INV_DSC1	FILL_LST1	FILL_DSC1	ERR_LUT_MISS0	ERR_UPD_DATA0	ERR_UPD_CTRL0	ERR_UPD_AREA0	ERR_INV_DATA0	ERR_INV_DSC0	FILL_LST0	FILL_DSC0

Bits	Field Name	Description	Type	Reset
31	ERR_LUT_MISS3	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
30	ERR_UPD_DATA3	Unexpected data register update whilst refilling interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
29	ERR_UPD_CTRL3	Unexpected control register update whilst refilling interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
28	ERR_UPD_AREA3	Unexpected area register update whilst refilling interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
27	ERR_INV_DATA3	Invalid entry-table pointer interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
26	ERR_INV_DSC3	Invalid descriptor pointer interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
25	FILL_LST3	End of refill interrupt source mask for the last descriptior in area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
24	FILL_DSC3	End of refill interrupt source mask for any descriptior in area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
23	ERR_LUT_MISS2	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
22	ERR_UPD_DATA2	Unexpected data register update whilst refilling interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
21	ERR_UPD_CTRL2	Unexpected control register update whilst refilling interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
20	ERR_UPD_AREA2	Unexpected area register update whilst refilling interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
19	ERR_INV_DATA2	Invalid entry-table pointer interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
18	ERR_INV_DSC2	Invalid descriptor pointer interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
17	FILL_LST2	End of refill interrupt source mask for the last descriptior in area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
16	FILL_DSC2	End of refill interrupt source mask for any descriptior in area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
15	ERR_LUT_MISS1	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
14	ERR_UPD_DATA1	Unexpected data register update whilst refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
13	ERR_UPD_CTRL1	Unexpected control register update whilst refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
12	ERR_UPD_AREA1	Unexpected area register update whilst refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
11	ERR_INV_DATA1	Invalid entry-table pointer interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
10	ERR_INV_DSC1	Invalid descriptor pointer interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
9	FILL_LST1	End of refill interrupt source mask for the last descriptior in area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
8	FILL_DSC1	End of refill interrupt source mask for any descriptior in area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
7	ERR_LUT_MISS0	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
6	ERR_UPD_DATA0	Unexpected data register update whilst refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
5	ERR_UPD_CTRL0	Unexpected control register update whilst refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
4	ERR_UPD_AREA0	Unexpected area register update whilst refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
3	ERR_INV_DATA0	Invalid entry-table pointer interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
2	ERR_INV_DSC0	Invalid descriptor pointer interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
1	FILL_LST0	End of refill interrupt source mask for the last descriptior in area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0
0	FILL_DSC0	End of refill interrupt source mask for any descriptior in area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Enable (unmask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toSet	0

Table 15-76. Register Call Summary for Register DMM_PAT_IRQENABLE_SET

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- Error Handling: [32] [33]
- DMM Register Summary: [34]

Table 15-77. DMM_PAT_IRQENABLE_CLR

Address Offset	0x0000 04B0		
Physical Address	0x4E00 04B0	**Instance**	DMM
Description	Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register. n = 0 for the first interrupt enable clear register, n = 1 for the second interrupt enable clear register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_LUT_MISS3	ERR_UPD_DATA3	ERR_UPD_CTRL3	ERR_UPD_AREA3	ERR_INV_DATA3	ERR_INV_DSC3	FILL_LST3	FILL_DSC3	ERR_LUT_MISS2	ERR_UPD_DATA2	ERR_UPD_CTRL2	ERR_UPD_AREA2	ERR_INV_DATA2	ERR_INV_DSC2	FILL_LST2	FILL_DSC2	ERR_LUT_MISS1	ERR_UPD_DATA1	ERR_UPD_CTRL1	ERR_UPD_AREA1	ERR_INV_DATA1	ERR_INV_DSC1	FILL_LST1	FILL_DSC1	ERR_LUT_MISS0	ERR_UPD_DATA0	ERR_UPD_CTRL0	ERR_UPD_AREA0	ERR_INV_DATA0	ERR_INV_DSC0	FILL_LST0	FILL_DSC0

Bits	Field Name	Description	Type	Reset
31	ERR_LUT_MISS3	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
30	ERR_UPD_DATA3	Unexpected data register update whilst refilling interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
29	ERR_UPD_CTRL3	Unexpected control register update whilst refilling interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
28	ERR_UPD_AREA3	Unexpected area register update whilst refilling interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
27	ERR_INV_DATA3	Invalid entry-table pointer interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
26	ERR_INV_DSC3	Invalid descriptor pointer interrupt source mask for area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
25	FILL_LST3	End of refill interrupt source mask for the last descriptior in area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked).. Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
24	FILL_DSC3	End of refill interrupt source mask for any descriptior in area 4.n+3 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
23	ERR_LUT_MISS2	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
22	ERR_UPD_DATA2	Unexpected data register update whilst refilling interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
21	ERR_UPD_CTRL2	Unexpected control register update whilst refilling interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
20	ERR_UPD_AREA2	Unexpected area register update whilst refilling interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
19	ERR_INV_DATA2	Invalid entry-table pointer interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
18	ERR_INV_DSC2	Invalid descriptor pointer interrupt source mask for area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
17	FILL_LST2	End of refill interrupt source mask for the last descriptior in area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
16	FILL_DSC2	End of refill interrupt source mask for any descriptior in area 4.n+2 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
15	ERR_LUT_MISS1	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
14	ERR_UPD_DATA1	Unexpected data register update whilst refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
13	ERR_UPD_CTRL1	Unexpected control register update whilst refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
12	ERR_UPD_AREA1	Unexpected area register update whilst refilling interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
11	ERR_INV_DATA1	Invalid entry-table pointer interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
10	ERR_INV_DSC1	Invalid descriptor pointer interrupt source mask for area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
9	FILL_LST1	End of refill interrupt source mask for the last descriptior in area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
8	FILL_DSC1	End of refill interrupt source mask for any descriptior in area 4.n+1 Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
7	ERR_LUT_MISS0	Unexpected access to a yet-to-be-refilled area interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
6	ERR_UPD_DATA0	Unexpected data register update whilst refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
5	ERR_UPD_CTRL0	Unexpected control register update whilst refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
4	ERR_UPD_AREA0	Unexpected area register update whilst refilling interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
3	ERR_INV_DATA0	Invalid entry-table pointer interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
2	ERR_INV_DSC0	Invalid descriptor pointer interrupt source mask for area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
1	FILL_LST0	End of refill interrupt source mask for the last descriptior in area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0
0	FILL_DSC0	End of refill interrupt source mask for any descriptior in area 4.n Write 0x0: Keep current mask of this interrupt source. Write 0x1: Disable (mask) this interrupt source. Read 0x1: This interrupt source is enabled (unmasked). Read 0x0: This interrupt source is disabled (masked).	RW W1toClr	0

Table 15-78. Register Call Summary for Register DMM_PAT_IRQENABLE_CLR

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- Error Handling: [32] [33]
- DMM Register Summary: [34]

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Table 15-79. DMM_PAT_STATUS_i

Address Offset	0x0000 04C0 + (0x4 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 04C0 + (0x4 * i)	**Instance**	DMM
Description	Status register for each refill engine n = 0 for the first engine status register, n = 1 for the second engine status register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CNT								ERROR						RESERVED		BYPASSED	RESERVED		LINKED	DONE	RUN	VALID	READY

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved	R	0x00
24:16	CNT	Counter of remaining lines to reload for engine n	R	0x000
15:10	ERROR	Error happened in engine n Read 0x0: No error Read 0x1: Invalid descriptor provided Read 0x2: Invalid data pointer provided Read 0x4: Unexpected area register update while refilling Read 0x8: Unexpected control register update while refilling Read 0x10: Unexpected data register update while refilling Read 0x20: Unexpected access to a yet-to-be-refilled location	R	0x00
9:8	RESERVED	Reserved	R	0x0
7	BYPASSED	Engine n is bypassed. Direct access to the LUT is provided.	R	0
6:5	RESERVED	Reserved	R	0x0
4	LINKED	Area reconfiguration link asserted for engine n	R	0
3	DONE	Area reloading finished for engine n	R	0
2	RUN	Area currently reloading for engine n	R	0
1	VALID	Valid area description for engine n	R	0
0	READY	Area registers ready for engine n	R	1

Table 15-80. Register Call Summary for Register DMM_PAT_STATUS_i

Dynamic Memory Manager

- DMM Interrupt Requests: [0] [1]
- PAT Description: [2]
- Simple Manual Area Refill: [3] [4]
- Single Auto-Configured Area Refill: [5] [6]
- Chained Auto-Configured Area Refill: [7] [8] [9]
- Synchronized Auto-Configured Area Refill: [10] [11] [12]
- Cyclic Synchronized Auto-Configured Area Refill: [13]
- DMM Register Summary: [14]

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Table 15-81. DMM_PAT_DESCR_i

Address Offset	0x0000 0500 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0500 + (0x10 * i)	**Instance**	DMM
Description	Physical address of the next table refill descriptor n = 0 for the descriptor register of the first engine, n = 1 for the descriptor register of the second engine. Writing to this register aborts the current ongoing area reload and resets the corresponding DMM_PAT_AREA_i, DMM_PAT_CTRL_i and DMM_PAT_DATA_i registers.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Physical address of the next table refill descriptor of engine n	RW WtoClr	0x0000000
3:0	RESERVED	Reserved	RW W0Only	0x0

Table 15-82. Register Call Summary for Register DMM_PAT_DESCR_i

Dynamic Memory Manager

- DMM Integration: [0]
- PAT Description: [1] [2] [3]
- Single Auto-Configured Area Refill: [4]
- Chained Auto-Configured Area Refill: [5]
- Synchronized Auto-Configured Area Refill: [6]
- Cyclic Synchronized Auto-Configured Area Refill: [7] [8]
- DMM Register Summary: [9]

Table 15-83. DMM_PAT_AREA_i

Address Offset	0x0000 0504 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0504 + (0x10 * i)	**Instance**	DMM
Description	Area definition for DMM physical address translator n = 0 for the area register of the first engine, n = 1 for the area register of the second engine.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y1								X1								Y0								X0							

Bits	Field Name	Description	Type	Reset
31:24	Y1	Y-coordinate of the bottom-right corner of the PAT area for engine n	RW	0x00
23:16	X1	X-coordinate of the bottom-right corner of the PAT area for engine n	RW	0x00
15:8	Y0	Y-coordinate of the top-left corner of the PAT area for engine n	RW	0x00
7:0	X0	X-coordinate of the top-left corner of the PAT area for engine n	RW	0x00

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Table 15-84. Register Call Summary for Register DMM_PAT_AREA_i

Dynamic Memory Manager

- DMM Integration: [0]
- Address Translation: [1]
- PAT Description: [2] [3] [4]
- Simple Manual Area Refill: [5]
- Configuration Settings and LUT Refill: [6]
- TILER Page Mapping: [7]
- DMM Register Summary: [8]
- DMM Register Description: [9]

Table 15-85. DMM_PAT_CTRL_i

Address Offset	0x0000 0508 + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 0508 + (0x10 * i)	**Instance**	DMM
Description	DMM physical address translator control register n = 0 for the control register of the first engine, n = 1 for the control register of the second engine.		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1	0
INITIATOR	RESERVED	SYNC	RESERVED	DIRECTION	RESERVED	START

Bits	Field Name	Description	Type	Reset
31:28	INITIATOR	DMM PAT initiator for synchronization in engine n	RW	0x0
27:17	RESERVED	Reserved	RW W0Only	0x000
16	SYNC	DMM PAT table reload synchronization for engine n 0x0: Not synchronized 0x1: Synchronized	RW	0
15:7	RESERVED	Reserved	RW W0Only	0x000
6:4	DIRECTION	Direction of this PAT table refill for engine n	RW	0x0
3:1	RESERVED	Reserved	RW W0Only	0x0
0	START	Starting a PAT table refill with engine n	RW	0

Table 15-86. Register Call Summary for Register DMM_PAT_CTRL_i

Dynamic Memory Manager

- DMM Integration: [0]
- PAT Description: [1] [2] [3] [4] [5]
- Simple Manual Area Refill: [6] [7]
- Cyclic Synchronized Auto-Configured Area Refill: [8]
- Configuration Settings and LUT Refill: [9] [10]
- Aliased Tiled View Orientation Settings and LUT Refill: [11] [12] [13] [14] [15]
- DMM Register Summary: [16]
- DMM Register Description: [17]

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Table 15-87. DMM_PAT_DATA_i

Address Offset	0x0000 050C + (0x10 * i)	**Index**	i = 0 to 3
Physical Address	0x4E00 050C + (0x10 * i)	**Instance**	DMM
Description	Physical address of the current table refill entry data n = 0 for the data register of the first engine, n = 1 for the data register of the second engine.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	ADDR	Physical address of the current table refill entry data or single actual entry data when in manual mode for engine n	RW	0x0000000
3:0	RESERVED	Reserved	RW W0Only	0x0

Table 15-88. Register Call Summary for Register DMM_PAT_DATA_i

Dynamic Memory Manager

- DMM Integration: [0]
- Address Translation: [1]
- PAT Description: [2] [3] [4]
- Simple Manual Area Refill: [5]
- Configuration Settings and LUT Refill: [6]
- DMM Register Summary: [7]
- DMM Register Description: [8]

Table 15-89. DMM_PEG_HWINFO

Address Offset	0x0000 0608		
Physical Address	0x4E00 0608	**Instance**	DMM
Description	DMM hardware configuration for PEG		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PRIO_CNT							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	PRIO_CNT	Number of PEG priority entries Read 0x1: One priority entry Read 0x2: Two priority entries Read 0x4: Four priority entries Read 0x8: Eight priority entries Read 0x10: Sixteen priority entries Read 0x20: Thirty-two priority entries Read 0x40: Sixty-four priority entries	R	0x40

Table 15-90. Register Call Summary for Register DMM_PEG_HWINFO

Dynamic Memory Manager

- DMM Configuration: [0]
- DMM Register Summary: [1]

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Table 15-91. DMM_PEG_PRIO_k

Address Offset	0x0000 0620 + (0x4 * k)	**Index**	k = 0 to 7
Physical Address	0x4E00 0620 + (0x4 * k)	**Instance**	DMM
Description	DMM PEG Priority register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W7	P7			W6	P6			W5	P5			W4	P4			W3	P3			W2	P2			W1	P1			W0	P0		

Bits	Field Name	Description	Type	Reset
31	W7	Write-enable for P7 bit field Write 0x0: P7 field is unchanged. Write 0x1: P7 field is updated.	RW	0
30:28	P7	Priority for initiator ConnID = 8 × k + 7	RW	0x4
27	W6	Write-enable for P6 bit field Write 0x0: P6 field is unchanged. Write 0x1: P6 field is updated.	RW	0
26:24	P6	Priority for initiator ConnID = 8 × k + 6	RW	0x4
23	W5	Write-enable for P5 bit field Write 0x0: P5 field is unchanged. Write 0x1: P5 field is updated.	RW	0
22:20	P5	Priority for initiator ConnID = 8 × k + 5	RW	0x4
19	W4	Write-enable for P4 bit field Write 0x0: P4 field is unchanged. Write 0x1: P4 field is updated.	RW	0
18:16	P4	Priority for initiator ConnID = 8 × k + 4	RW	0x4
15	W3	Write-enable for P3 bit field Write 0x0: P3 field is unchanged. Write 0x1: P3 field is updated.	RW	0
14:12	P3	Priority for initiator ConnID = 8 × k + 3	RW	0x4
11	W2	Write-enable for P2 bit field Write 0x0: P2 field is unchanged. Write 0x1: P2 field is updated.	RW	0
10:8	P2	Priority for initiator ConnID = 8 × k + 2	RW	0x4
7	W1	Write-enable for P1 bit field Write 0x0: P1 field is unchanged. Write 0x1: P1 field is updated.	RW	0
6:4	P1	Priority for initiator ConnID = 8 × k + 1	RW	0x4
3	W0	Write-enable for P0 bit field Write 0x0: P0 field is unchanged. Write 0x1: P0 field is updated.	RW	0
2:0	P0	Priority for initiator ConnID = 8 × k	RW	0x4

Table 15-92. Register Call Summary for Register DMM_PEG_PRIO_k

Dynamic Memory Manager

- DMM Integration: [0]
- PEG Description: [1]
- Priority Settings: [2]
- DMM Register Summary: [3]

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Table 15-93. DMM_PEG_PRIO_PAT

Address Offset	0x0000 0640		
Physical Address	0x4E00 0640	**Instance**	DMM
Description	DMM PEG priority register for the internal PAT engine.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												W_PAT	P_PAT		

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	RW W0Only	0x0000000
3	W_PAT	Write-enable for P_PAT bit field Write 0x0: P_PAT field is updated. Write 0x1: P_PAT field is unchanged.	RW	0
2:0	P_PAT	Priority for PAT engine	RW	0x4

Table 15-94. Register Call Summary for Register DMM_PEG_PRIO_PAT

Dynamic Memory Manager

- DMM Integration: [0]
- PEG Description: [1]
- Priority Settings: [2] [3]
- DMM Register Summary: [4]

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15.3 EMIF Controller

This section describes the features and functions of the external memory interface (EMIF) module of the device.

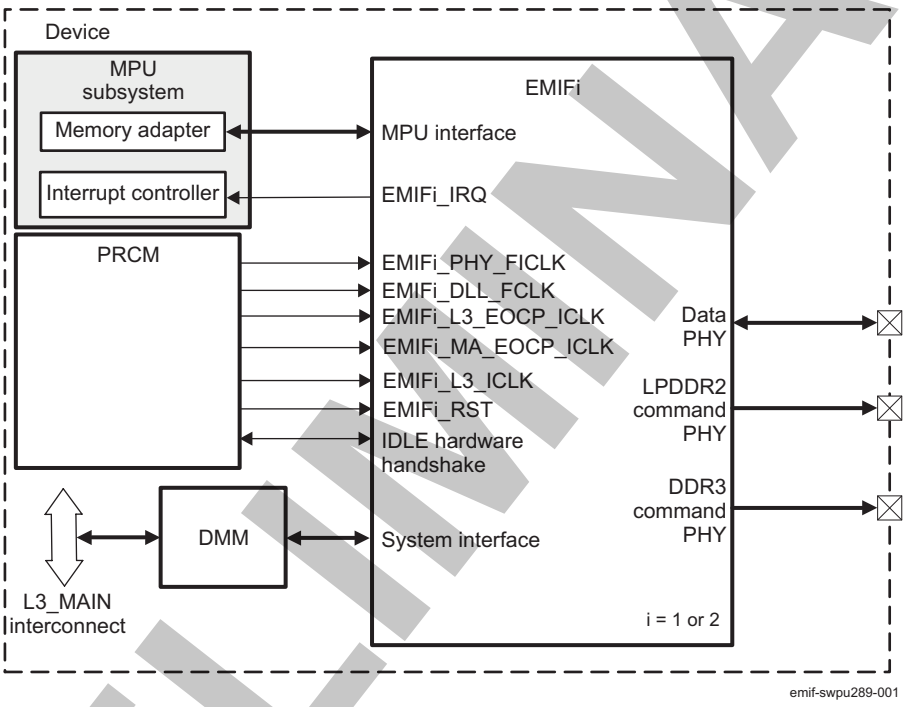
15.3.1 EMIF Module Overview

The EMIF module provides connectivity between the device and LPDDR2-type or DDR3-type of memories and manages data bus read/write accesses between external memories and the device subsystems having access to the L3_MAIN interconnect and DMA capability.

The EMIF is also introduced in Section 15.1, *Memory Subsystem Overview*.

The device includes two EMIF controllers. Figure 15-43 is an overview of the EMIF modules.

Figure 15-43. EMIF Module Overview



15.3.1.1 EMIF Overall Integration

Figure 15-44 shows the EMIF connection with the surrounding modules and SDRAM devices.

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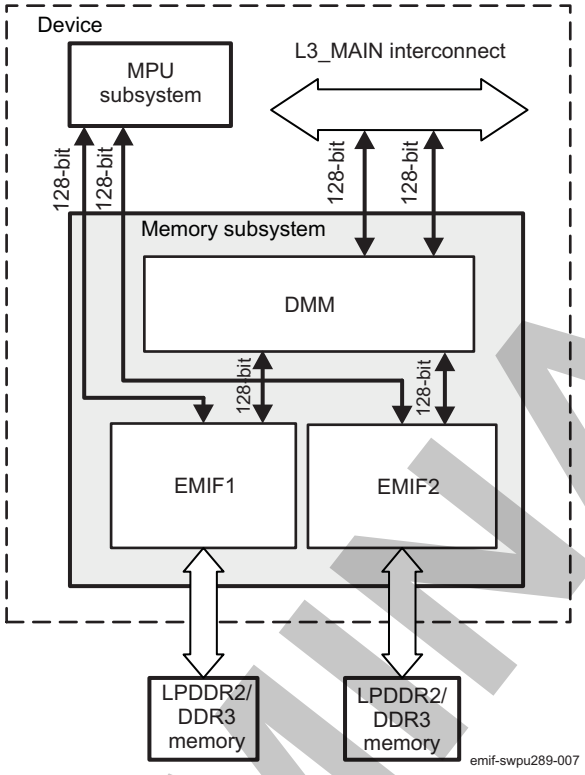
Figure 15-44. EMIF Overall Architecture



15.3.2 EMIF Environment

This section describes the EMIF application fields from an environment point of view (external connections).

NOTE: The device package restricts the physical connection to only one memory type: LPDDR2 or DDR3. See more details about device family and packaging in , *Introduction*.

Figure 15-45 shows the EMIF LPDDR2 generic configuration.

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Figure 15-45. EMIF LPDDR2 Generic Configuration

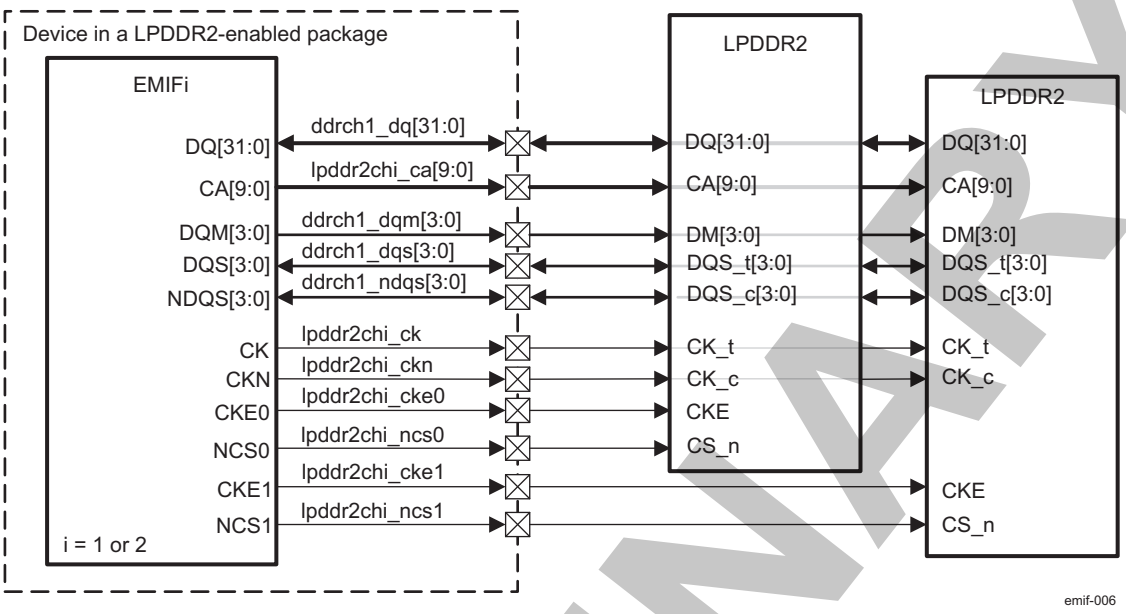

Figure 15-46 shows the EMIF DDR3 generic configuration.

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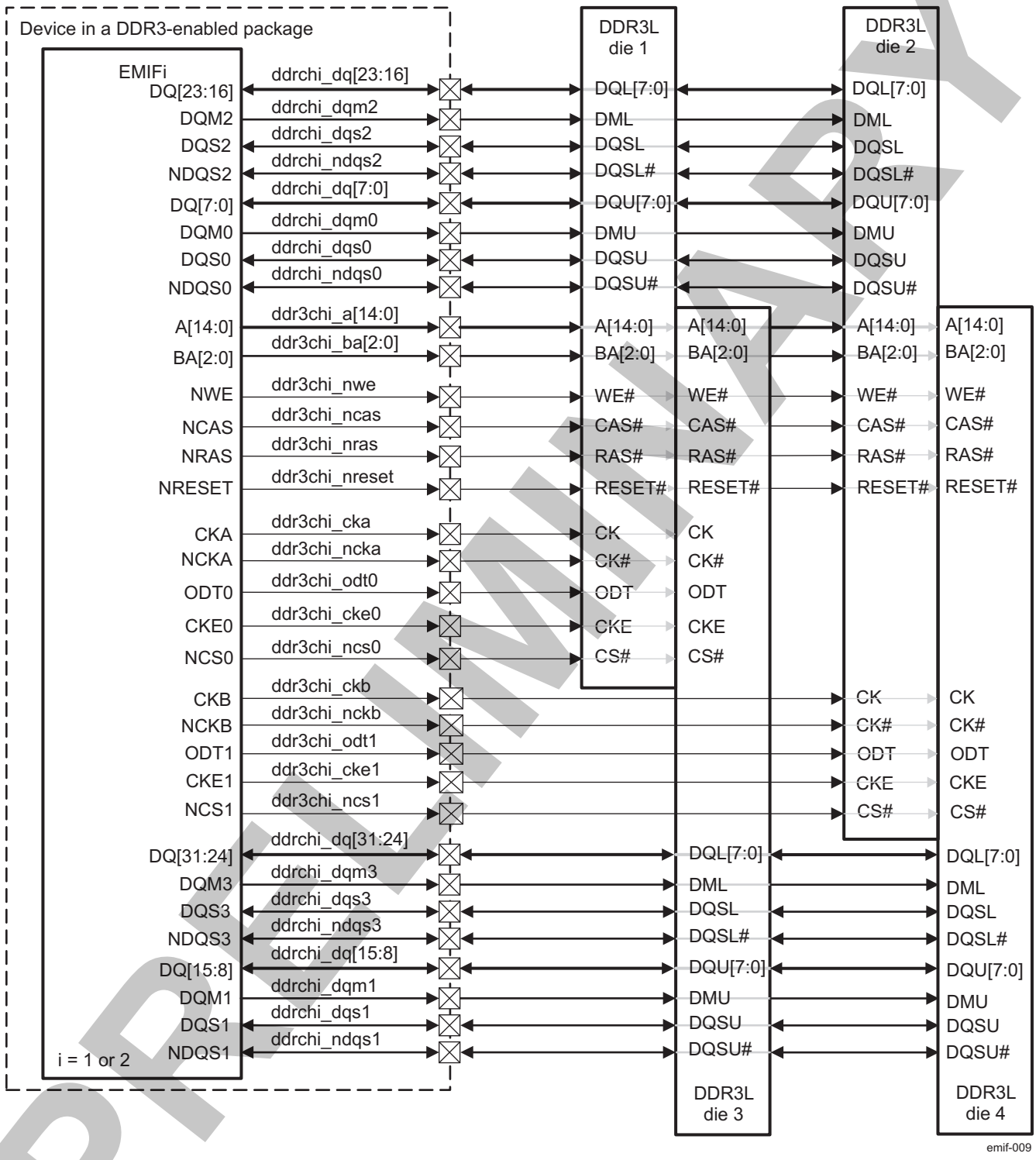
Figure 15-46. EMIF DDR3 Generic Configuration



15.3.2.1 EMIF Signals

Table 15-95 describes the module signals and specifies their links to functions used to connect LPDDR2 type of memories. LPDDR2 command PHY signals are available only on LPDDR2-enabled device packages. LPDDR2 data PHY signals are common with the DDR3 ones.

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Table 15-95. LPDDR2 I/O Signals

Module Pin	Device I/O Signal	I/O[1]	Description
EMIF1 Data PHYs			
DQ[31:0]	ddrch1_dq[31:0]	I/O	Data bus
DQM[3:0]	ddrch1_dqm[3:0]	I/O	Data mask
DQS[3:0]	ddrch1_dqs[3:0]	I/O	Data strobe
NDQS[3:0]	ddrch1_ndqs[3:0]	I/O	Data strobe invert
EMIF1 LPDDR2 Command PHY			
CA[9:0]	lpddr2ch1_ca[9:0]	O	Double-data rate (DDR) command/address
CK	lpddr2ch1_ck	O	Clock
NCK	lpddr2ch1_nck	O	Clock invert
NCS[1:0]	lpddr2ch1_ncs[1:0]	O	Chip-selects 1:0 (active low)
CKE[1:0]	lpddr2ch1_cke[1:0]	O	Clock-enables 1:0
EMIF2 Data PHYs			
DQ[31:0]	ddrch2_dq[31:0]	I/O	Data bus
DQM[3:0]	ddrch2_dqm[3:0]	I/O	Data mask
DQS[3:0]	ddrch2_dqs[3:0]	I/O	Data strobe
NDQS[3:0]	ddrch2_ndqs[3:0]	I/O	Data strobe invert
EMIF2 LPDDR2 Command PHY			
CA[9:0]	lpddr2ch2_ca[9:0]	O	Double-data rate (DDR) command/address
CK	lpddr2ch2_ck	O	Clock
NCK	lpddr2ch2_nck	O	Clock invert
NCS[1:0]	lpddr2ch2_ncs[1:0]	O	Chip-selects 1:0 (active low)
CKE[1:0]	lpddr2ch2_cke[1:0]	O	Clock-enables 1:0

(1) I = Input; O = Output

Table 15-96 describes the module signals and specifies their links to functions used to connect DDR3 type of memories. DDR3 command PHY signals are available only on DDR3-enabled device packages. DDR3 data PHY signals are common with the LPDDR2 ones.

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Table 15-96. DDR3 I/O Signals

Module Pin	Device I/O Signal	I/O[1]	Description
EMIF1 Data PHYs			
DQ[31:0]	ddrch1_dq[31:0]	I/O	Data bus
DQM[3:0]	ddrch1_dqm[3:0]	I/O	Data mask
DQS[3:0]	ddrch1_dqs[3:0]	I/O	Data strobe
NDQS[3:0]	ddrch1_ndqs[3:0]	I/O	Data strobe invert
EMIF1 DDR3 Command PHYs			
A[15:0]	ddr3ch1_a[15:0]	O	Row/column address bus
BA[2:0]	ddr3ch1_ba[2:0]	O	Bank select
CKA	ddr3ch1_cka	O	Differential clock, set a (DDR3 command PHY 0)
NCKA	ddr3ch1_ncka	O	Differential clock, set a (DDR3 command PHY 0)
CKB	ddr3ch1_ckb	O	Differential clock, set b (DDR3 command PHY 1)
NCKB	ddr3ch1_nckb	O	Differential clock, set b (DDR3 command PHY 1)
NCS[1:0]	ddr3ch1_ncs[1:0]	O	Rank select 1:0 (active low)
CKE[1:0]	ddr3ch1_cke[1:0]	O	Clock enable for rank 1:0
NCAS	ddr3ch1_ncas	O	Command
NRAS	ddr3ch1_nras	O	Command
NWE	ddr3ch1_nwe	O	Command
NRESET	ddr3ch1_nreset	O	Asynchronous reset (active low)
ODT[1:0]	ddr3ch1_odt[1:0]	O	On-die termination for rank 1:0
EMIF2 Data PHYs			
DQ[31:0]	ddrch2_dq[31:0]	I/O	Data bus
DQM[3:0]	ddrch2_dqm[3:0]	I/O	Data mask
DQS[3:0]	ddrch2_dqs[3:0]	I/O	Data strobe
NDQS[3:0]	ddrch2_ndqs[3:0]	I/O	Data strobe invert
EMIF2 DDR3 Command PHYs			
A[15:0]	ddr3ch2_a[15:0]	O	Row/column address bus
BA[2:0]	ddr3ch2_ba[2:0]	O	Bank select
CKA	ddr3ch2_cka	O	Differential clock, set a (DDR3 command PHY 0)
NCKA	ddr3ch2_ncka	O	Differential clock, set a (DDR3 command PHY 0)
CKB	ddr3ch2_ckb	O	Differential clock, set b (DDR3 command PHY 1)
NCKB	ddr3ch2_nckb	O	Differential clock, set b (DDR3 command PHY 1)
NCS[1:0]	ddr3ch2_ncs[1:0]	O	Rank select 1:0 (active low)
CKE[1:0]	ddr3ch2_cke[1:0]	O	Clock enable for rank 1:0
NCAS	ddr3ch2_ncas	O	Command
NRAS	ddr3ch2_nras	O	Command
NWE	ddr3ch2_nwe	O	Command
NRESET	ddr3ch2_nreset	O	Asynchronous reset (active low)
ODT[1:0]	ddr3ch2_odt[1:0]	O	On-die termination for rank 1:0

(1) I = Input; O = Output

Each SDRAM channel (that is, each EMIF controller) can be connected to two external SDRAM memories. For more information, see Section 15.2.1, *Dynamic Memory Manager*.

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15.3.3 EMIF Integration

This section describes the integration of the module in the device, and includes information about clocks, resets, and hardware requests.

Figure 15-47 shows the integration of the EMIF1 module in the device.

Figure 15-47. EMIF1 Integration

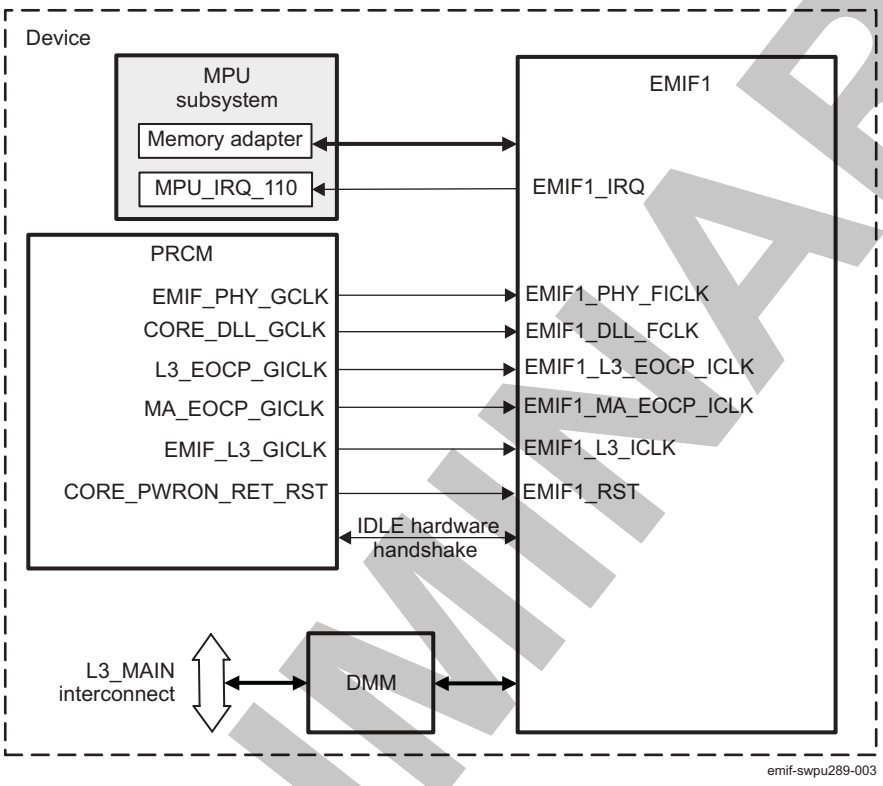

Figure 15-48 shows the integration of the EMIF2 module in the device.

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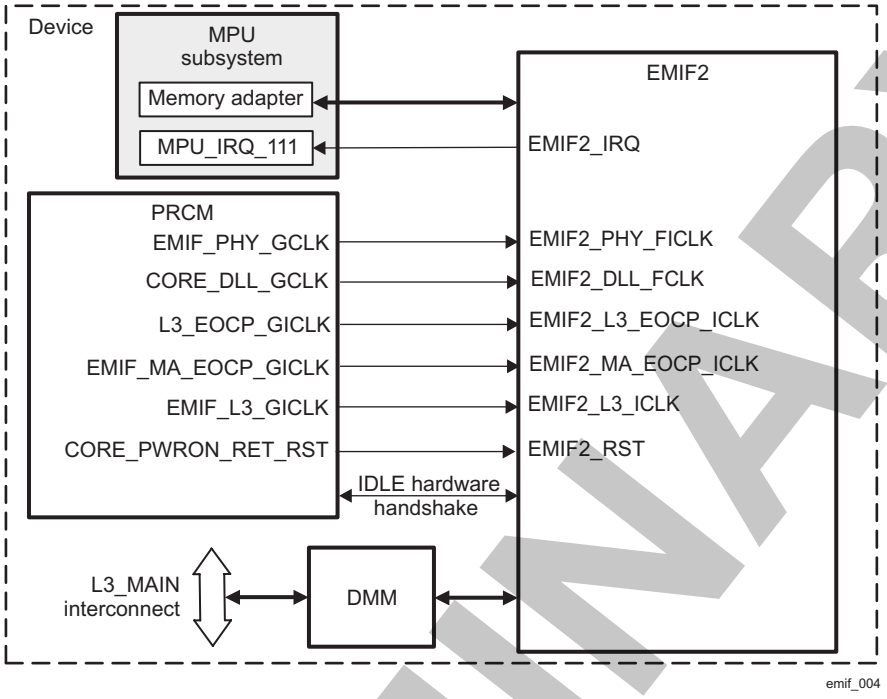
Figure 15-48. EMIF2 Integration



NOTE: For more information about the IDLE hardware handshake, see Section 3.1.1, *Power, Reset, and Clock Management*.

Table 15-97 through Table 15-99 summarize the integration of the module in the device.

Table 15-97. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
EMIF1	PD_CORE	No	L3_MAIN
EMIF2	PD_CORE	No	L3_MAIN

Table 15-98. Clocks and Resets

	Clocks			
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
EMIF1	EMIF1_L3_EOCP_ICLK	L3_EOCP _GICLK	PRCM	System interface clock
	EMIF1_L3_ICLK	EMIF_L3_GICLK	PRCM	L3_MAIN interface clock
	EMIF1_MA_EOCP_ICLK	MA_EOCP_GICLK	PRCM	MPU interface clock
	EMIF1_PHY_FICLK	EMIF_PHY_GCLK	PRCM	PHY functional clock (runs at DDR clock rate)
	EMIF1_DLL_FCLK	CORE_DLL_GCLK	PRCM	DLL functional clock
	EMIF_CORE1	EMIF1_PHY_FICLK/2	EMIF1 PHY	EMIF1 internal core functional clock (runs at half-speed DDR clock rate)
EMIF2	EMIF2_L3_EOCP_ICLK	L3_EOCP _GICLK	PRCM	System interface clock
	EMIF2_L3_ICLK	EMIF_L3_GICLK	PRCM	L3_MAIN interface clock
	EMIF2_MA_EOCP_ICLK	MA_EOCP_GICLK	PRCM	MPU interface clock

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Table 15-98. Clocks and Resets (continued)

	EMIF2_PHY_FICLK	EMIF_PHY_GCLK	PRCM	PHY functional clock (runs at DDR clock rate)
	EMIF2_DLL_FCLK	CORE_DLL_GCLK	PRCM	DLL functional clock
	EMIF_CORE2	EMIF2_PHY_FICLK/2	EMIF2 PHY	EMIF2 internal core functional clock (runs at half-speed DDR clock rate)
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
EMIF1	EMIF1_RST	CORE_POWERON_RET_RST	PRCM	Core/Power-on/Retention reset
EMIF2	EMIF2_RST	CORE_POWERON_RET_RST	PRCM	Core/Power-on/Retention reset

NOTE: The two clocks MA_EOCP_GICLK and L3_EOCP_GICLK are exclusive. EMIF modules are clocked by MA_EOCP_GICLK when MPU interface is active, otherwise L3_EOCP_GICLK clock is used.

NOTE: EMIF PHYs are clocked from EMIFi_PHY_FICLK which runs at the DDR clock rate. EMIF cores are clocked from EMIFi_PHY_FICLK divided by 2, that is, the so called EMIF clock rate.

Table 15-99. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
EMIF1	EMIF1_IRQ	MPU_IRQ_110	MPU interrupt controller (INTC)	Interrupt to the MPU subsystem
EMIF2	EMIF2_IRQ	MPU_IRQ_111	MPU INTC	Interrupt to the MPU subsystem

NOTE: For the description of the interrupt source, see Section 15.3.4.5, *Interrupt Requests*.

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15.3.4 EMIF Functional Description

15.3.4.1 Block Diagram

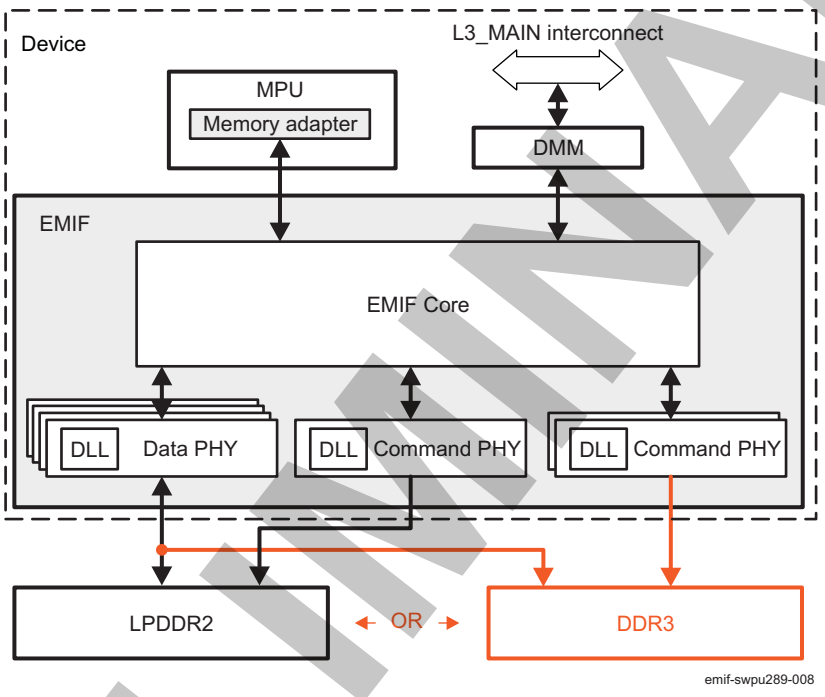
The EMIF is an L3 bus peripheral that provides an interface to SDRAM memories.

Figure 15-49 shows the interconnection between the EMIF module and the other modules.

Digital locked loops (DLLs) are used to delay the input DQS signals during reads so that these strobe signals can be used to latch incoming data on the DQ pins, as required by the DDR standard.

Physical layers (PHYs) convert single-data rate (SDR) signals to DDR signals.

Figure 15-49. EMIF Block Diagram



15.3.4.1.1 Local Interface

The EMIF supports three local (on-chip) interfaces:

- System interface (from L3_MAIN interconnect)
- MPU interface (from MPU subsystem)
- Low-latency interface This interface is not connected to any subsystem in this device.

System and Low-latency interfaces are used to request all external memory device accesses, to access the EMIF registers, and to transfer all data to and from the EMIF controller. MPU interface is used to process memory accesses. Each interface has its own clock.

Table 15-100 shows the MAddrSpace mapping to different CSs.

Table 15-100. MAddrSpace Mapping to Chip-Selects

MAddrSpace[1]	Chip-Select	Description	Exclusions
0x0	NCS[1:0]	SDRAM(s)	
0x1	NCS1	Reserved for LPDDR2-NVM	Not supported
0x2	N/A	Reserved. Any access to this area will generate an error on the L3 interface. This can be used by the software to track any unwanted access to the section defined in the DMM_LISA_MAP_i register.	Not visible to the MPU port

(1) See DMM_LISA_MAP_i [17:16] SDRC_ADDRSPC register bitfield in Section 15.2, *Dynamic Memory Manager*.

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Table 15-100. MAddrSpace Mapping to Chip-Selects (continued)

MAddrSpace[1]	Chip-Select	Description	Exclusions
0x3	N/A	Internal registers	Not visible to the MPU port

Table 15-101 lists the features of the EMIF interface port.

Table 15-101. Port Features

Feature	System	LL (not connected)	MPU
64-bit bus		√	
128-bit bus	√		√
Register access	√	√	
2D access	√	√	

15.3.4.1.2 FIFO Description

The EMIF module contains the following FIFOs:

- Command FIFO
- Write data FIFO
- Return command FIFO
- Two read data FIFOs

Figure 15-50 shows the overall architecture of the EMIF FIFOs.

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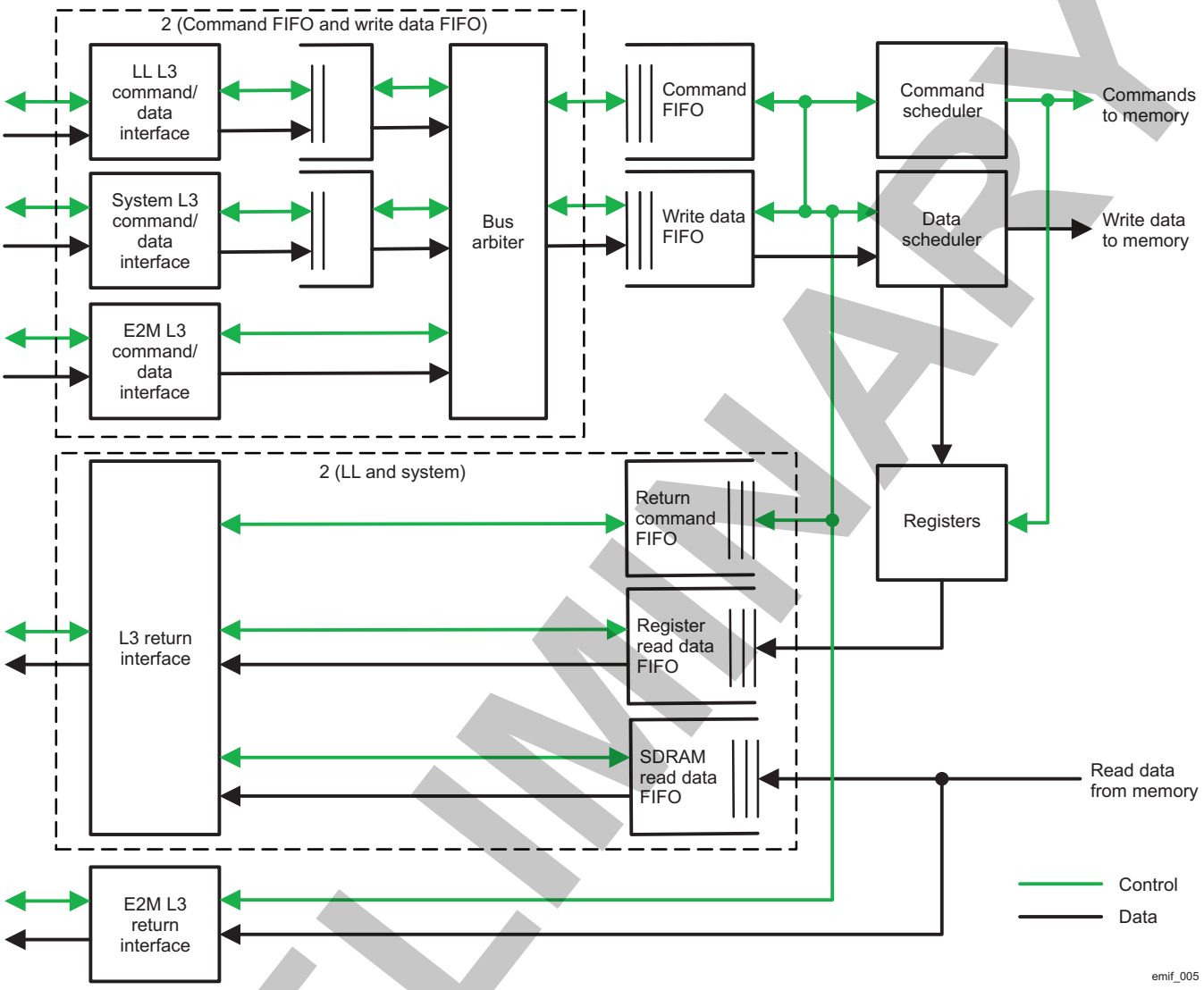
Figure 15-50. FIFO Block Diagram



Because the system (128-bit) local interface is the main interface, it has a higher allocation of FIFO slots than the low-latency (64-bit) local interface. Table 15-102 lists the allocation of the entries.

Table 15-102. FIFO Allocation

Parameter	System Local Interface Entries	Low-Latency Local Interface Entries	MPU Local Interface Entries
Pre Command FIFO	6	6	4
Command FIFO	Programmable (1)	Programmable (1)	Programmable (1)
Pre Write FIFO	6	6	8
Write Data FIFO (256-bit)	Up to (19 × 256 bits) + 6	Up to (19 × 256 bits) + 6	Up to 19 + 8
Return Command FIFO	22	17	24
SDRAM Read Data FIFO	22	17	24
Register Read Data FIFO	2	2	0

(1) The total number of entries in the command FIFO is 10.

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The command FIFO is shared between the three local interfaces, whereas there are three different FIFOs for every other type, one dedicated to each local interface.

The command FIFO stores all the commands coming in on the local command interface. The allocation of entries in the command FIFO is programmable per local interface using the following bit fields:

- EMIF_OCP_CONFIG[27:24] SYS_THRESH_MAX
- EMIF_OCP_CONFIG[19:16] LL_THRESH_MAX
- EMIF_OCP_CONFIG[23:20] MPU_TRESH_MAX

If the addition of the EMIF_OCP_CONFIG[27:24] SYS_THRESH_MAX and EMIF_OCP_CONFIG[19:16] LL_THRESH_MAX bit fields is greater than the number of entries in the command FIFO, the allocation depends on the traffic on the interfaces. For example, if both fields are programmed to 7, then either of the interfaces can use seven entries in the command FIFO if the other interface is idle. If both interfaces have traffic, then the EMIF starts to gradually allocate entries to both interfaces until it settles down to seven entries for the low-latency interface and three entries for the system interface, because the low-latency interface has higher priority. If the low-latency interface has no traffic, the system interface can use seven entries.

The allocation also depends on the traffic on the interfaces, if the EMIF_OCP_CONFIG[27:24] SYS_THRESH_MAX and EMIF_OCP_CONFIG[19:16] LL_THRESH_MAX bit fields are programmed to be equal to or greater than the number of entries in the command FIFO. For example, if both fields are programmed to 10, then the low-latency port can use all the entries if there is no traffic on the system interface. However, if there is no traffic on the low-latency interface, the system interface can use all but one entry. This is because the low-latency interface has higher priority than the system interface. The only way for the system interface to use all command FIFO entries is to set the EMIF_OCP_CONFIG[19:16] LL_THRESH_MAX bit field to 0. Writing 0 reserves no space for the associated interface. If the value is set to 0 and a request is seen for that interface, the command FIFO assumes a value of 1 for that interface.

The write data FIFO stores the write data for all the write transactions coming in on the local write data interface. The write FIFO is shared for all the ports. A similar token mechanism is used to allocate the write FIFO with the following exceptions. All ports are given a minimum of four tokens, which ensures that each has ensured access to three write FIFO locations. Any one port can only use up to 19 of the 25 write FIFO locations. Because there is a 6-word pre-FIFO, each port can have up to 25 backlogged writes. The LL interface can have up to twice the logged write data values, because the interface is 50 percent of the internal data storage.

The return command FIFO stores all the return transactions that are to be issued to the local return interface. These include the write status return and the read data return commands.

Two read data FIFOs store the read data to be sent to the local return interface. One read data FIFO stores read data from the memory mapped registers. The other read data FIFO stores read data from external memory.

A write command is executed only when four local words of the corresponding data is received in the write data FIFO, or when it is the last data, and if there is space in the return command FIFO. The EMIF schedules a read-only if the results can fit into the return command FIFO and the corresponding read data FIFOs.

15.3.4.1.3 MPU Port Restrictions

The EMIF MPU port is defined only to process memory requests. All register accesses are processed through the system or LL ports of the EMIF. The EMIF MPU port does not support 2D or register requests required or provided by the system and LL interfaces.

15.3.4.1.4 Port Priority

When Mflag = 0, or when the Mflag port override bit (EMIF_READ_WRITE_EXECUTION_THRESHOLD [31] MFLAG_OVERRIDE) is set:

1. LL port (highest priority)
2. System or MPU depending on the MPriority field of the MReqInfo bus

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When Mflag = 1:

- The system port is given highest priority: EMIF guarantees one System command will be executed, before switching back to legacy priority scheme (above). This ping-pong arbitration scheme continues until Mflag is returned to 0.
- If no system command is present, the legacy priority scheme is maintained.
- If refresh_must is asserted, then only one refresh is retried, to prevent refresh cycles taking away from bandwidth during this critical time.

15.3.4.1.5 Coherency

To maintain coherency, the following rules must be followed:

- Any command arriving on any interface (MPU, system, or LL) that matches an address in the command FIFO is executed after the command in the command FIFO
- The matching address is any address within a 2,000-address boundary
- On a 2-D transfer, the starting address is the compared address. The computed addresses of the 2-D transfer are not considered in address overlapping.
- Any command arriving within a 10-cycle window of another, from the different interfaces that do not match any address in the command FIFO, but may match command addresses arriving on a different interface, can be executed in any order.

15.3.4.1.6 Arbitration of Commands in the Command FIFO

The EMIF looks at all the commands stored in the command FIFO to schedule commands to the external memory. All commands with the same MConnID on a particular local interface complete in order. The EMIF does not ensure ordering between commands with different MConnIDs or between commands from two local interfaces. For more information about L3 interconnect terms (MConnID, MCMD, MADDR, etc.) see Section 14.2.1, *L3 Interconnect*.

However, the EMIF does maintain data coherency. Therefore, the EMIF blocks a command, regardless of priority or the local interface, if that command is to the same block address (2048 bytes) as an older command that is not complete. Thus, the EMIF may have one pending read or write for each MConnID. Among all pending reads, the EMIF selects all reads that have their corresponding SDRAM banks already open. Similarly, among all pending writes, the EMIF selects all writes that have their corresponding SDRAM banks already open. Accesses to memory mapped registers are treated as accesses that have open banks.

As a result of this reordering, the EMIF may now have several pending reads and writes that have their corresponding banks open. The EMIF then selects the highest priority read from pending reads, and the highest priority write from pending writes. Commands from the low-latency local interface have a higher priority over the commands from the system local interface. If two or more commands have the highest priority, the EMIF selects the oldest command. As a result, the EMIF may now have the next read and a write command. If the return command FIFO and the read data FIFO have space and the external bus conflict is resolved, the EMIF performs the final read command before the final write command. If the return command FIFO has space but the read data FIFO is full, the EMIF performs the final write command before the final read command. Resolution of external bus conflict means all the SDRAM command-to-command counters are satisfied and the read-to-write or write-to-read turnaround time is met.

The EMIF does not support tag interleaving. In other words, for an local interface, the EMIF completes executing an local command before it switches to another command. The EMIF can, however, interleave execution between commands from two local interfaces.

The data coherency inside the EMIF is ensured only in a single level of local infrastructure. For example, if a write from a secondary local bus segment is blocked by a bridge element, the read from a tertiary bus can still beat the write to the EMIF. In such a case, to confirm that a write from master A has landed before a read from master B is performed, master A must wait for the write status from the EMIF before indicating to master B that the data is ready to be read. If master A does not use the local wait status, it must do the following:

1. Perform the required write.
2. Perform a dummy write to the EMIF_REVISION register.

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3. Perform a dummy read to the EMIF_REVISION register.
4. Indicate to master B that the data is ready to be read after completion of read in Step 3. The completion of read in Step 3 ensures that the previous writes were done.

Apart from reads and writes, the EMIF must also open and close SDRAM banks and maintain the refresh counts for an SDRAM. The priority of SDRAM commands with respect to refresh levels are:

1. SDRAM refresh request when refresh-must level is reached (highest priority)
2. ZQ calibration
3. Leveling
4. local request for a read or write
5. local request for a write
6. SDRAM activate commands
7. SDRAM deactivate commands
8. SDRAM deep power-down request
9. SDRAM power-down request
10. SDRAM refresh request when refresh-may or release level is reached
11. SDRAM self-refresh request (lowest priority)

While performing the previous scheduling algorithm, the EMIF may encounter two conditions:

- A continuous stream of high-priority commands can block lower priority commands.
- A continuous stream of SDRAM commands to a row in an open bank can block commands to another row in the same bank.

In addition to this scheduling, the highest priority condition is a reset command. If this condition occurs, the EMIF abandons what it is doing and begins its start-up sequence. In this case, commands and data stored in the FIFOs are lost. The EMIF also starts its start-up sequence whenever the EMIF_SDRAM_CONFIG register is written and the EMIF_SDRAM_REFRESH_CONTROL[31] INITREF_DIS bit is set to 0. In this case, commands and data stored in the FIFOs are not lost. The EMIF ensures that in-flight read or write transactions to the SDRAM are complete before starting the initialization sequence.

All the accesses to an SDRAM are pipelined to maximize use of the external bus. All of these are done while fulfilling the access timing requirements of an SDRAM.

15.3.4.2 Clock Management

The EMIF can gate EMIF_COREi. There is an internal mechanism that can stop EMIF_COREi automatically. EMIF_COREi is stopped only after the SDRAM is put into self-refresh mode and the power-idle protocol on the local bus completes. The EMIF_COREi frequency can be changed only after putting the external SDRAM in self-refresh mode.

The EMIF waits for the DLL lock before performing any memory access.

EMIF_COREi frequency is equal to half of the EMIFi_PHY_FICLK frequency.

15.3.4.3 Reset

The EMIF does not support a software reset.

The EMIF supports a global warm reset mode, during which the EMIF keeps the SDRAM content. Upon a request from the PRCM module indicating a need to enter global warm reset mode, the EMIF does the following:

1. During a leveling operation, EMIF will immediately exit the operation, and a load mode register access (DDR3) will be used to exit leveling mode. Also, the incremental leveling prescaler and count register values will be reset to zero, preventing incremental leveling from firing later and causing an undesired exit from self-refresh during a warm reset state.
2. EMIF completes the ongoing access, and then puts the SDRAM in self-refresh mode. If the EMIF_SDRAM_REFRESH_CONTROL[31] INITREF_DIS field is set to 1, the EMIF does not put SDRAM in self-refresh mode. If EMIF is in LPDDR2 mode and the

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EMIF_LPDDR2_MODE_REG_CONFIG[30] REFRESH_EN is set to 0, the EMIF does not put LPDDR2 in self-refresh mode.

3. EMIF clears all its FIFO contents.
4. EMIF does not wait for all interrupts to be serviced.

To exit the global warm reset:

1. If the EMIF was in Self Refresh state, it will exit Self Refresh state.
2. If leveling was enabled at the time of a global warm reset, a PHY reset must occur to bring the PHY back into a known state, as it may have been left in a leveling state upon warm reset assertion. To guarantee the SDRAM memory clocks are off when issuing a PHY reset, the EMIF_POWER_MANAGEMENT_CONTROL register may be needed to enter self refresh before asserting PHY reset.
3. It is the responsibility of software to go through a full leveling and reinitialize any incremental leveling thereafter.

15.3.4.4 System Power Management

15.3.4.4.1 Power-Down Mode

The EMIF supports power-down mode for low power. The EMIF automatically puts the SDRAM into power-down mode after it is idle for EMIF_POWER_MANAGEMENT_CONTROL[15:12] PD_TIM number of DDR clock cycles and the EMIF_POWER_MANAGEMENT_CONTROL[10:8] LP_MODE bit field is set to 0x4. In power-down mode, the EMIF does not stop the clocks to the SDRAM. The EMIF maintains CKE pin low to maintain the power-down mode.

When the SDRAM is in power-down mode, the EMIF services register accesses normally.

If the SDRAM is in power-down mode and one of the following occurs, the EMIF brings SDRAM out of power-down mode:

- EMIF_POWER_MANAGEMENT_CONTROL[10:8] LP_MODE bit field is changed from 0x4 to some other value.
- An SDRAM access is requested.
- The refresh-must level is reached.

For DDR3, the EMIF also exits power-down mode to perform incremental leveling. If refresh-must brings EMIF out of Power-Down, it will reenter Power-Down when the refreshes are complete if there has not been a SDRAM request.

To exit power-down, the EMIF:

1. Drives CKE high after t_cke + 1 cycles have elapsed since the power-down command was issued. The value of t_cke is taken from EMIF_SDRAM_TIMING_2[2:0] T_CKE bit field.
2. Waits for EMIF_SDRAM_TIMING_2[30:28] T_XP + 1 cycles
3. Enters its idle state and can issue any commands

15.3.4.4.2 LPDDR2 Deep Power-Down Mode

For ultimate power savings, the EMIF supports deep power-down mode for LPDDR2.

The SDRAM can be forced into deep power-down mode through software by setting the EMIF_POWER_MANAGEMENT_CONTROL[11] DPD_EN bit to 0x1. In this case the EMIF continues normal operation until all SDRAM access requests are serviced. At this point the EMIF issues a deep power-down command. The EMIF then maintains CKE pin low to maintain deep power-down mode. In deep power-down mode, the EMIF automatically stops the clocks to the SDRAM.

Setting the EMIF_POWER_MANAGEMENT_CONTROL[11] DPD_EN bit to 1 overrides the setting of the EMIF_POWER_MANAGEMENT_CONTROL[10:8] LP_MODE bit field. Therefore, if the SDRAM is in any other power-saving mode, and the EMIF_POWER_MANAGEMENT_CONTROL[11] DPD_EN bit is set to 1, the EMIF exits those modes and goes into deep power-down mode.

When the SDRAM is in deep power-down mode, the EMIF services register accesses normally.

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If the EMIF_POWER_MANAGEMENT_CONTROL[11] DPD_EN bit is set to 0x0, the EMIF brings the SDRAM out of deep power-down mode.

For LPDDR2, the EMIF controller performs SDRAM initialization as specified in Section 15.3.4.7.1, *LPDDR2-SDRAM Initialization*. Note the initialization part that must be performed by the software.

15.3.4.4.3 Self-Refresh Mode

The EMIF supports self-refresh mode for low power. The EMIF automatically puts the SDRAM into self-refresh mode after the EMIF is idle for EMIF_POWER_MANAGEMENT_CONTROL[7:4] SR_TIMING number of DDR clock cycles and the EMIF_POWER_MANAGEMENT_CONTROL[10:8] LP_MODE bit field is set to 0x2. The EMIF will complete all pending refreshes before it puts the SDRAM into self-refresh. Therefore, after the expiration of SR_TIMING, the EMIF will start issuing refreshes to complete the refresh backlog, and then issue a self-refresh command to the SDRAM.

In self-refresh mode, the EMIF automatically stops the clocks to the SDRAM. The EMIF drives CKE pin low to maintain self-refresh mode.

When the SDRAM is in self-refresh mode, the EMIF services register accesses normally.

If the SDRAM is in self-refresh mode and one of the following occurs, the EMIF brings SDRAM out of self-refresh mode:

- The EMIF_POWER_MANAGEMENT_CONTROL[10:8] LP_MODE bit field is changed from 0x2 to some other value.
- SDRAM access is requested .

For DDR3, the EMIF also exits self-refresh to perform incremental leveling.

To exit self-refresh, for LPDDR2, the EMIF:

1. Waits for EMIF_SDRAM_TIMING_2[2:0] T_CKE + 1 cycles have elapsed since the self-refresh command was issued and enables clocks
2. Drives CKE pin high
3. Waits for EMIF_SDRAM_TIMING_2[24:16] T_XSNR + 1 cycles
4. Starts an auto-refresh cycle in the next cycle. It also services all refreshes down to the refresh-release level.
5. Enters its idle state and can issue any commands

To exit self-refresh, for DDR3, the EMIF:

1. Waits for EMIF_SDRAM_TIMING_2[2:0] T_CKE + 1 cycles have elapsed since the self-refresh command was issued and enables clocks
2. Drives CKE pin high
3. Waits for EMIF_SDRAM_TIMING_2[24:16] T_XSNR + 1 cycles
4. If EMIF_SDRAM_CONFIG[20] DDR_DISABLE_DLL is 1, issues a load mode register command to the extended mode register 1 (pins BA[2:0] = 0x1) with the A[15:0] pins set as inTable 15-103

Table 15-103. Extended Mode Register 1 Value

Bits	Value	Description
A[15:13]	0x0	Reserved
A[12]	0x0	Output buffer enabled
A[11]	0x0	TDQS disable
A[12]	0x0	Reserved
A[9]	DDR_TERM[2]	DDR3 termination resistor value from EMIF_SDRAM_CONFIG register, bit 26
A[8]	0x0	Reserved
A[7]	0x0	Write leveling disabled
A[6]	DDR_TERM[1]	DDR3 termination resistor value from EMIF_SDRAM_CONFIG register, bit 19

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Table 15-103. Extended Mode Register 1 Value (continued)

Bits	Value	Description
A[5]	SDRAM_DRIVE[1]	SDRAM drive strength from EMIF_SDRAM_CONFIG register, bit 25
A[4:3]	0x0	Additive latency = 0
A[2]	DDR_TERM[0]	DDR3 termination resistor value from EMIF_SDRAM_CONFIG register, bit 24
A[1]	SDRAM_DRIVE[0]	SDRAM drive strength from EMIF_SDRAM_CONFIG register, bit 18
A[0]	0x1	Disable DLL

5. Starts an auto-refresh cycle in the next cycle. It also services all refreshes down to the refresh-release level.
6. Enters its idle state and can issue any other commands except for a write or a read. A write or a read is issued only after EMIF_SDRAM_TIMING_2[15:6] T_XSRD + 1 cycles clock cycles have elapsed since pin CKE is driven high.

To use partial array self-refresh, the EMIF_SDRAM_REFRESH_CONTROL[26:24] PASR bits must be appropriately programmed. The EMIF performs bank interleaving when EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 0x0. Because the SDRAM is partially refreshed during partial array self-refresh, for software ease, it is recommended that IBANK_POS be set to 1, 2, or 3 depending on the scheme used. If IBANK_POS is set to 0, software must move critical data into the banks that are going to be refreshed during partial array self-refresh.

15.3.4.4.4 Retention Mode

EMIF supports full-retention mode.

NOTE: It is a responsibility of the software to:

- Disable incremental leveling on entry into retention to avoid possible collision with SDRAM self refresh entry
- Enable incremental leveling or perform a full leveling upon exit of retention

15.3.4.5 Interrupt Requests

The EMIF sources two interrupts: one for the system and MPU local interfaces, and the other for the low-latency local interface. The pulse and level interrupt signals for a particular interface are sourced from the same raw interrupt internal to the module.

The EMIF sets the EMIF_SYSTEM_OCP_INTERRUPT_RAW_STATUS[0] RAW_SYS/EMIF_LOW_LATENCY_OCP_INTERRUPT_RAW_STATUS[0] RAW_LL bit (depending on which interface sent the command having an error) to 1, if an access request to an unsupported MAddrSpace is received. If such an error occurs, it is due to bad programming of the DMM. For more information about addressing, see Section 15.2.1, *Dynamic Memory Manager*.

Table 15-104 lists the event flags and their mask that can cause module interrupts.

Table 15-104. Events

Event Flag	Event Mask	Description
EMIF_SYSTEM_OCP_INTERRUPT_RAW_STATUS[1] TA_SYS / EMIF_SYSTEM_OCP_INTERRUPT_STATUS[1] TA_SYS	EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_SET[1] EN_TA_SYS / EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_CLEAR[1] EN_TA_SYS	System interface interrupt for SDRAM temperature alert
EMIF_SYSTEM_OCP_INTERRUPT_RAW_STATUS[0] ERR_SYS / EMIF_SYSTEM_OCP_INTERRUPT_STATUS[0] ERR_SYS	EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_SET[0] EN_ERR_SYS / EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_CLEAR[0] EN_ERR_SYS	System interface interrupt for command or address error

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15.3.4.6 SDRAM Refresh Scheduling

The EMIF uses two counters to schedule AUTO REFRESH commands: a 13-bit decrementing refresh interval counter and a 4-bit refresh backlog counter. The interval counter is used to define the rate at which connected SDRAM devices are refreshed. It is loaded with the value of the EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE bit field at reset (only the 13 LSBs are taken). The interval counter decrements by 1 each cycle until it reaches 0, at which point it reloads from the EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE bit field and restarts decrementing. The counter also reloads and restarts decrementing whenever the EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE bit field is updated.

The refresh backlog counter records the number of outstanding AUTO REFRESH commands the EMIF has. The backlog counter increments by 1 each time the interval counter reloads (unless it has reached its maximum value of 8). The backlog counter decrements by 1 each time the EMIF issues an AUTO REFRESH command (unless it is already 0). For the range of values that the backlog counter can take, there are three levels of urgency with which the EMIF must perform an auto refresh cycle (in which it issues AUTO REFRESH commands):

1. Refresh-may level is reached when the backlog count is greater than 0, which indicates there is a refresh backlog; therefore, if the EMIF is not busy and none of the SDRAM banks are open, the EMIF must perform an auto refresh cycle.
2. Refresh-release level is reached when the backlog count is greater than 4, which indicates the refresh backlog is getting bigger; therefore, if the EMIF is not busy it must perform an auto refresh cycle even if any of the banks are open.
3. Refresh-must level is reached when the backlog count is greater than 7, which indicates the refresh backlog is becoming excessive and the EMIF must perform an auto refresh cycle before servicing any new memory access requests. The EMIF starts servicing new memory accesses after the refresh-release level is cleared.

The refresh counters do not operate when SDRAM is in self-refresh mode. Also, the refresh counters start tracking the missed refreshes only after initialization is complete in case of DDR3. For LPDDR2, the refresh counters will start tracking missed refreshes after the RESET command is issued.

The EMIF issues AUTO REFRESH commands within auto refresh cycles. An auto refresh cycle consists of issuing an AUTO REFRESH command and waiting T_RFC (see EMIF_SDRAM_TIMING_3) cycles before rechecking the refresh levels. If the refresh-release level is not reached, the EMIF starts another auto refresh cycle; otherwise, it returns to idle mode where it can issue any command. The EMIF ensures that no more than eight AUTO REFRESH commands are issued in any rolling t_{REFBW} (= 4 × 8 × t_{RFC}) window.

15.3.4.7 SDRAM Initialization

15.3.4.7.1 LPDDR2 SDRAM Initialization

When coming out of reset, if the EMIF_SDRAM_CONFIG[31:29] SDRAM_TYPE bit field is equal to 4, the EMIF performs an LPDDR2 initialization sequence as follows:

1. Drives the CKE pin high and starts to issue NOP commands continuously
2. After 17 SDRAM refresh rate intervals, issues a PRECHARGE-ALL command. The SDRAM refresh rate is defined in the EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE bit field.
3. Issues a RESET command
4. Software must initialize LPDDR2 using the EMIF_LPDDR2_MODE_REG_CONFIG and EMIF_LPDDR2_MODE_DATA registers. Software must enable refreshes by writing 1 in the EMIF_LPDDR2_MODE_REG_CONFIG[30] REFRESH_EN bit during the last MRW command.

The EMIF also performs the initialization sequence whenever the EMIF_SDRAM_CONFIG register is written and the LPDDR2 initialization was not performed previously because the EMIF_SDRAM_REFRESH_CONTROL[31] INITREF_DIS bit was set to 0. Once the EMIF performs initialization, rewriting the EMIF_SDRAM_CONFIG/EMIF_SDRAM_CONFIG_2 configuration registers does not cause reinitialization.

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NOTE: The values of the bit fields in the EMIF_SDRAM_CONFIG and EMIF_SDRAM_CONFIG_2 registers are loaded by the control module at reset. These values can be modified by the configuration header (CH) feature of the ROM code or by the initial boot image running from an external XIP booting memory or internal RAM (see Section 28.3.8, *Image Format*). They must not be modified during run time, because they reflect the used hardware SDRAM memory configurations.

The EMIF does not perform any transactions until the LPDDR2 initialization sequence completes.

When the EMIF comes out of reset, the delay time in Step 2 resulting from the 17 refresh rate intervals + 8 cycles is approximately 17 × EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE / input frequency.

15.3.4.7.2 DDR3 Initialization

On coming out of reset, if EMIF_SDRAM_CONFIG[31:29] SDRAM_TYPE is equal to 3 and EMIF_SDRAM_REFRESH_CONTROL[31] INITREF_DIS bit is set to 0, the EMIF performs a DDR3 SDRAM initialization sequence as follows:

1. Drives the CKE pin low
2. After 17 SDRAM refresh rate intervals, issues a NOP command with CKE pin held high. The SDRAM refresh rate is as defined in the EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE bit field.
3. After one SDRAM refresh rate interval, issues a LOAD MODE REGISTER command to the extended mode register 2 (pins BA[2:0] = 0x2) with pins A[15:0] set as in Table 15-105

Table 15-105. Extended Mode Register 2 Value

Bits	Value	Description
A[15:11]	0x0	Reserved
A[10:9]	DYN_ODT[1:0]	Dynamic ODT value from EMIF_SDRAM_CONFIG[22:21] DYN_ODT. Dynamic ODT is NOT supported. Set to 0x0 in the register bitfield.
A[8]	0x0	Reserved
A[7]	SRT	Self-refresh temperature range from EMIF_SDRAM_REFRESH_CONTROL[29] SRT
A[6]	ASR	Auto self-refresh enable from EMIF_SDRAM_REFRESH_CONTROL[28] ASR
A[5]	0x0	Reserved
A[4:3]	CWL[1:0]	CAS write latency from EMIF_SDRAM_CONFIG[17:16] CWL
A[2:0]	PASR[2:0]	Partial array self-refresh from EMIF_SDRAM_REFRESH_CONTROL[26:24] PASR

4. Issues a LOAD MODE REGISTER command to the extended mode register 3 (pins BA[2:0] = 0x3) with A[15:0] = 0x0
5. Issues a LOAD MODE REGISTER command to the extended mode register 1 (BA[2:0] = 0x1) with A[15:0] set as in Table 15-106

Table 15-106. Extended Mode Register 1 Value

Bits	Value	Description
A[15:13]	0x0	Reserved
A[12]	0x0	Output buffer enabled
A[11]	0x0	TDQS disable
A[10]	0x0	Reserved
A[9]	DDR_TERM[2]	DDR3 termination resistor value from EMIF_SDRAM_CONFIG[26] DDR_TERM
A[8]	0x0	Reserved
A[7]	0x0	Write leveling disabled

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Table 15-106. Extended Mode Register 1 Value (continued)

Bits	Value	Description
A[6]	DDR_TERM[1]	DDR3 termination resistor value from EMIF_SDRAM_CONFIG[25] DDR_TERM
A[5]	SDRAM_DRIVE[1]	SDRAM drive strength from EMIF_SDRAM_CONFIG[19] SDRAM_DRIVE
A[4:3]	0x0	Additive latency = 0
A[2]	DDR_TERM[0]	DDR3 termination resistor value from EMIF_SDRAM_CONFIG[24] DDR_TERM
A[1]	SDRAM_DRIVE[0]	SDRAM drive strength from EMIF_SDRAM_CONFIG[18] SDRAM_DRIVE
A[0]	0x0	Enable SDRAM DLL

6. Issues a LOAD MODE REGISTER command to the mode register 0 (BA[2:0] = 0x0) with A[15:0] set as in Table 15-107

Table 15-107. Mode Register 0 Value

Bits	Value	Description
A[15:13]	0x0	Reserved
A[12]	0x0	Fast exit active power-down exit time
A[11:9]	T_WR[4:0]	Write recovery for auto pre-charge from EMIF_SDRAM_TIMING_1[20:17] T_WR
A[8]	0x1	DLL reset
A[7]	0x0	Normal mode
A[6:4]	CL[3:1]	CAS latency from EMIF_SDRAM_CONFIG[13:11] CL
A[3]	0x0	Sequential burst type
A[2]	CL[0]	CAS latency from EMIF_SDRAM_CONFIG[10] CL
A[1:0]	0x0	Burst length of 8

7. Issues a ZQCL command to start long ZQ calibration
8. Waits for t_{DLLK} and t_{ZQinit} to complete
9. If the EMIF_SDRAM_CONFIG[20] DDR_DISABLE_DLL bit is 1, issues a LOAD MODE REGISTER command to the extended mode register 1 (BA[2:0] = 0x1) with A[15:1] set as in Table 15-106 (Step 5) and A[0] set to 0x1.
10. Issues an AUTO REFRESH command
11. The EMIF enters its IDLE state.

The EMIF also performs the initialization sequence whenever the EMIF_SDRAM_CONFIG register is written. But in this case, the EMIF starts from Step 3.

The EMIF does not perform any transactions until the DDR3 initialization sequence is complete.

NOTE: The LOAD MODE REGISTER command may be referred to as MODE REGISTER SET command in some DDR3 datasheets.

When the EMIF comes out of reset, the delay time in Step 2 resulting from the 16 refresh rate intervals + 8 cycles is approximately 17 × REFRESH_RATE / input frequency.

15.3.4.8 DDR3 Read-Write Leveling

The EMIF supports two types of write/read leveling:

- Full leveling
- Incremental leveling

Each leveling type has three parts:

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1. Write leveling
2. Read DQS gate training
3. Read data eye training

15.3.4.8.1 Full Leveling

The EMIF does not perform full leveling after initialization upon reset. Full leveling must be triggered by software after the EMIF registers are properly configured. The EMIF also supports triggering of full leveling through software through the use of the EMIF_READ_WRITE_LEVELING_CONTROL[31] RDWRLVLFULL_START bit.

Full leveling will be interrupted by auto refresh if a refresh-must state is reached. Upon completion of the auto refresh, full leveling will be reentered at the point it exited and continue until completion.

15.3.4.8.2 Incremental Leveling

The EMIF supports incremental leveling to better track voltage and temperature changes during normal operation. The incremental leveling can be enabled by writing a non-zero value to the following bit fields in the EMIF_READ_WRITE_LEVELING_CONTROL register:

- [7:0] WRLVLINC_INT
- [15:8] RDLVLGATEINC_INT
- [23:16] RDLVLINC_INT

The EMIF periodically triggers incremental write leveling every time WRLVLINC_INT expires. In other words, the WRLVLINC_INT defines the interval between successive incremental write leveling.

Similarly, the EMIF periodically triggers incremental read DQS gate training every time RDLVLGATEINC_INT expires, and triggers incremental read data eye training every time RDLVLINC_INT expires. To minimize impact on bandwidth, the software can program these intervals such that these three intervals do not expire at same time. The value of interval programmed is dependent on the slope of voltage and temperature changes.

The EMIF supports increasing the rate of incremental leveling automatically for a defined period of time. This can be achieved by programming the EMIF_READ_WRITE_LEVELING_RAMP_CONTROL register and by using a signal to increase the rate of incremental leveling from PHY. Whenever a signal is received, the EMIF uses the intervals programmed in the EMIF_READ_WRITE_LEVELING_RAMP_CONTROL register until the ramp window in the EMIF_READ_WRITE_LEVELING_RAMP_WINDOW[12:0] RDWRLVLINC_RMP_WIN bit field expires. After the expiration, the EMIF switches back to use the intervals programmed in the EMIF_READ_WRITE_LEVELING_CONTROL register. To ensure none of the incremental leveling events are missed, the EMIF_READ_WRITE_LEVELING_RAMP_WINDOW[12:0] RDWRLVLINC_RMP_WIN bit field must be programmed greater than the intervals in the EMIF_READ_WRITE_LEVELING_RAMP_CONTROL register.

If the EMIF is in self-refresh or power-down mode when any of the incremental leveling intervals expire, the EMIF exits self-refresh or power-down mode, perform the required leveling, and then re-enter the exited mode.

15.3.4.9 EMIF Access Cycles

By default, the EMIF keeps the SDRAM CSs high (CSs are active-low signals). To direct a command to only one of the SDRAMs, the EMIF asserts the CS to the SDRAM for the duration of the command. If the EMIF_SDRAM_CONFIG[3] EBANK bit in the SDRAM configuration register is set to 0, NCS1 is always driven high except during initialization and for the REFRESH, POWER-DOWN, SELF-REFRESH, and DEEP POWER-DOWN commands.

The EMIF always performs burst accesses to the SDRAM. Multiple SDRAM bursts may be needed to service a single local burst request. Table 15-108 through Table 15-112 show a few examples of how EMIF accesses SDRAM for a linear incrementing transaction type. T0, T1, etc. are clock cycles. R0 is read starting at column 0, R8 is read starting at column 8, and R16 is read starting at column 16. D0-1 is the data from column 0 and 1, D2-3 is the data from column 2 and 3, and so on.

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Table 15-108. 64-Byte Linear Read Starting at Address 0x0

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11
R0				R8							
				D0-1	D2-3	D4-5	D6-7	D8-9	D10-11	D12-13	D14-15

Table 15-109. 64-Byte Linear Read Starting at Address 0x8 (LPDDR2-S2)

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14
R2			R8				R16							
				D2-3	D4-5	D6-7	D8-9	D10-11	D12-13	D14-15	D16-17	Unused	Unused	Unused

Table 15-110. 64-Byte Linear Read Starting at Address 0x8 (LPDDR2-S4)

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15
R2				R8				R16							
				D2-3	D4-5	D6-7	Unused	D8-9	D10-11	D12-13	D14-15	D16-17	Unused	Unused	Unused

Table 15-111. 64-Byte Linear Read Starting at Address 0x10

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
R4		R8				R16							
				D4-5	D6-7	D8-9	D10-11	D12-13	D14-15	D16-17	D18-19	Unused	Unused

Table 15-112. 64-Byte Linear Read Starting at Address 0x18

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
R6		R8				R16							
				D6-7	Unused	D8-9	D10-11	D12-13	D14-15	D16-17	D18-19	D20-21	Unused

The EMIF uses the unused data phases in the preceding figures by issuing successive read commands if there are reads to open banks pending in the command FIFO.

The write data conversion from SDR to DDR is done outside the EMIF.

15.3.4.9.1 LPDDR2 Read

A read access to an LPDDR2 is initiated with a READ command. The EMIF provides the internal bank address and the column address on pins CA[9:0] with the READ command. The EMIF registers the first read data from DQ[31:0] after (EMIF_DDR_PHY_CONTROL_1[4:0] READ_LATENCY) DDR clock cycles.

15.3.4.9.2 LPDDR2 Write

A write access to an LPDDR2 is initiated with a WRITE command. The EMIF provides the internal bank address and the column address on pins CA[9:0] with the WRITE command.

The EMIF delays the write data by the appropriate write latency minus 1. Subsequent data words are provided on DQ[31:0] along with the appropriate data mask on DM[3:0] on each successive clock cycle. The DDR PHY then adds one more clock cycle delay to the write data to appropriately center the write data to the outgoing DQS.

15.3.4.10 Turnaround Time

Table 15-113 lists the turnaround time the EMIF introduces on the data bus for various back-to-back accesses. The EMIF takes advantage of the CAS latencies and packs the commands as close as possible on the control bus to introduce the following turnaround time on the data bus.

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Table 15-113. Turnaround Time

Current Access	Next Access	Turnaround Time (Number of DDR Clock Cycles)
SDRAM write	SDRAM write to the same CS	0
SDRAM write	SDRAM write to a different CS	EMIF_SDRAM_TIMING_3[27:24] T_CSTA + 1
SDRAM read	SDRAM read to the same CS	0
SDRAM read	SDRAM read to a different CS	EMIF_SDRAM_TIMING_3[27:24] T_CSTA + 1
SDRAM write	SDRAM read	EMIF_SDRAM_TIMING_1[2:0] T_WTR + 1 + CL
SDRAM read	SDRAM write	EMIF_SDRAM_TIMING_1[31:29] T_RTW + 1

15.3.4.11 PHY DLL Calibration

When running in normal locked mode, the PHY DLL gets a reference clock (EMIFi_DLL_FCLK) from the PRCM, which is used by the DLL master to lock to the right frequency and provide the control code for a full period phase shift to the slave. The slave uses this code as a control for its internal delay line to produce the required delay for the signal considered.

When working in locked mode, the delay lines only get an updated control value from the master DLLs when an explicit dll_calib command is issued by the EMIF controller. Failure to send such commands on a timely basis will result in inaccurate delay-line information if there is a significant voltage and temperature drift in the system. It is recommended to issue at least one command every 100 µs. EMIF automatically sends ctrl_update commands for:

- Refresh Exit
- Self Refresh Exit
- phy_ready asserted during initialization

The PHY also internally generates a control value update upon completion of a leveling operation. Control is also added for the when leveling is not used (that is, not using ramp reg_rdwrlvlinc_rmp_win, which generates increased level of incremental leveling and an internally generated phy calib signal), and there are gradual voltage changes during frequency change. The EMIF_DLL_CALIB_CTRL register can be programmed to generate a phy_dll_calib for a periodic interval based on EMIF_COREi cycles, so allow continued memory access as voltage is changing. A safe window of no activity will be guaranteed for this periodic generation of phy_dll_calib. In addition, a one shot generator for phy_pll_calib has also been added that will generate a single phy_dll_calib by setting the EMIF_MISC_REG[0] DLL_CALIB_OS bit to 1.

15.3.4.12 SDRAM Address Mapping

The EMIF interleaves the internal banks for SDRAM connected to both CSs (see Table 15-114 for the SDRAM addressing space), according to the DMM (for more information, see Section 15.2.1, *Dynamic Memory Manager*). From the system point of view, the external SDRAM is seen as one block of SDRAM. If two external 64-MiB devices are used, a 128-MiB memory block is observed. If two external 32-MiB devices are used, a 64-MiB block is observed.

Table 15-114. SDRAM Addressing Space

Module Name	Base Address	Size
EMIF1 | EMIF2-CS0-SDRAM[(1)]	0x8000 0000	0 to 1GiB, programmable in DMM (see Section 15.2.1, *Dynamic Memory Manager*)

(1) The addressing space is interleaved on two SDRAM memory controllers (EMIF1, EMIF2), each activating itsCS0 line. These CSs can address 64, 128, 256, 512, 1024, or 2048MiB. Interleaving occurs at 128-byte granularity. EMIF1-CS0 base address is always 0x8000 0000 at reset, and occupies a 1-GiB address space at reset (interleaving disabled at reset).

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Table 15-114. SDRAM Addressing Space (continued)

Module Name	Base Address	Size
EMIF1| EMIF2-CS1-SDRAM[2]	0xC000 0000	0 to 1GiB, programmable in DMM (see Section 15.2.1, *Dynamic Memory Manager*)

[2] The addressing space is interleaved on two SDRAM memory controllers (EMIF1, EMIF2), each activating its CS1 line. These CSs are programmable to 64, 128, 256, 512, or 1024MiB. Interleaving occurs at 128-byte granularity. EMIF1-CS1 and EMIF2-CS1 are disabled at reset. Their base address is programmable to achieve a continuous address space with the respective CS0, regardless of the programmed address range. EMIF1-CS1 is disabled if the EMIF1-CS0 memory density is set to 2048MiB (2GiB) when interleaving is disabled, or if the EMIF1-CS0 + EMIF2-CS0 memory density is set to 1024MiB (1GiB) when interleaving is enabled.

When addressing SDRAM, if the EMIF_SDRAM_CONFIG[28:27] IBANK_POS bit field is set to 0, the EMIF uses the following three bit fields to determine the mapping from the source address to the SDRAM row, column, bank, and CS:

- EMIF_SDRAM_CONFIG[6:4] IBANK
- EMIF_SDRAM_CONFIG[3] EBANK
- EMIF_SDRAM_CONFIG[2:0] PAGESIZE

If the EMIF_SDRAM_CONFIG[28:27] IBANK_POS bit field is set to 1, 2, or 3, the EMIF uses the following four bit fields to determine the mapping from the source address to the SDRAM row, column, bank, and CS:

- EMIF_SDRAM_CONFIG[6:4] IBANK
- EMIF_SDRAM_CONFIG[3] EBANK
- EMIF_SDRAM_CONFIG[2:0] PAGESIZE
- EMIF_SDRAM_CONFIG[9:7] ROWSIZE

In all cases the EMIF considers its SDRAM address space to be a single logical block, regardless of the number of physical devices or whether the devices are mapped across one or two EMIF CSs.

15.3.4.12.1 Address Mapping for IBANK_POS = 0 and EBANK_POS = 0

For EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 0 and EMIF_SDRAM_CONFIG_2[27] EBANK_POS = 0, Table 15-115 lists which source address bits (MAddr) map to the SDRAM row, column, bank, and CS bits for all combinations of IBANK, EBANK, and PAGESIZE.

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Table 15-115. Local Address to 32-bit SDRAM Address Mapping for IBANK_POS = 0 and EBANK_POS = 0

MiB	EBANK	IBANK	PAGESIZE	MAddr 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
64	0	0	0	-							row (16 bits DDR3 / 15 bits LPDDR2)															col (8 bits)								
128	1			-						row														cs	col								
	0	1		-						row														bnk	col								
256	1			-					row														cs	bnk	col								
	0	2		-					row														bank	col								
512	1			-				row														cs	bank	col								
	0	3		-				row														bank	col								
1G	1			-			row														cs	bank	col								
128	0	0	1	-						row														col (9 bits)								
256	1			-					row														cs	col								
	0	1		-					row														bnk	col								
512	1			-				row														cs	bnk	col								
	0	2		-				row														bank	col								
1G	1			-			row														cs	bank	col								
	0	3		-			row														bank	col								
2G	1			-		row														cs	bank	col								
256	0	0	2	-					row													col (10 bits)								
512	1			-				row														cs	col								
	0	1		-				row														bnk	col								
1G	1			-			row														cs	bnk	col								
	0	2		-			row														bank	col								
2G	1			-		row														cs	bank	col								
	0	3		-		row														bank	col								
4G	1			row															cs	bank	col								
512	0	0	3	-				row														col (11 bits)								
1G	1			-			row														cs	col								
	0	1		-			row														bnk	col								
2G	1			-		row														cs	bnk	col								
	0	2		-		row														bank	col								
4G	1			row															cs	bank	col								
	0	3		row															bank	col								
	1			row														cs	bank	col								

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NOTE: ROWSIZE is unused in case of IBANK_POS = 0 and EBANK_POS = 0.

For EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 0, the effect of the address-mapping scheme is that as the source address increments across SDRAM page boundaries, the EMIF moves onto the same page in the next bank in the current device (pin CS0). This movement along the banks of the current device continues until the page is accessed in all banks in the current device. The EMIF then proceeds to the same page in the next device (if EMIF_SDRAM_CONFIG[3] EBANK = 1, pin CS1) and proceeds through the same page in all its banks before moving to the next page in the first device (pin CS0). The EMIF exploits this movement across internal banks and CSs while remaining on the same page to maximize the number of open SDRAM banks within the overall SDRAM space.

Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, and can interleave among all of them.

15.3.4.12.2 Address Mapping for IBANK_POS = 1 and EBANK_POS = 0

Table 15-116 list the local address to SDRAM address mapping. There are x bits for bank[2], followed by y bits for row, followed by z bits for CS, followed by s bits for bank[1:0], and t bits for col in MAddr[31:2] (x, y, z, s, and t are given depending on the value of the EMIF_SDRAM_CONFIG bit fields).

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Table 15-116. Local Address to SDRAM Address Mapping for IBANK_POS = 1 and EBANK_POS = 0

MAddr[31:2]									
bank[2]		row		cs		bank[1:0]		col	
IBANK	bank[2] width (bits)	ROWSIZE	row width (bits)	EBANK	cs width (bits)	IBANK	bank[1:0] width (bits)	PAGESIZE	col width (bits)
0	0	0	9	0	0	0	0	0	8
1	0	1	10	1	1	1	1	1	9
2	0	2	11			2	2	2	10
3	1	3	12			3	2	3	11
		4	13						
		5	14						
		6	15						
		7	16						

For EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 1, the EMIF interleaves banks the same as for EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 0, but the interleaving of banks within a device (per CS) is limited to four banks. Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, but can interleave among only 8 of them.

15.3.4.12.3 Address Mapping for IBANK_POS = 2 and EBANK_POS = 0

Table 15-117 list the local address to SDRAM address mapping. There are x bits for bank[2:1], followed by y bits for row, followed by z bits for CS, followed by s bits for bank[0], and t bits for col in MAddr[31:2] (x, y, z, s, and t are given depending on the value of the EMIF_SDRAM_CONFIG bit fields).

Table 15-117. Local Address to SDRAM Address Mapping for IBANK_POS = 2 and EBANK_POS = 0

MAddr[31:2]									
bank[2:1]		row		cs		bank[0]		col	
IBANK	bank[2:1] width (bits)	ROWSIZE	row width (bits)	EBANK	cs width (bits)	IBANK	bank[0] width (bits)	PAGESIZE	col width (bits)
0	0	0	9	0	0	0	0	0	8
1	0	1	10	1	1	1	1	1	9
2	1	2	11			2	1	2	10
3	2	3	12			3	1	3	11
		4	13						
		5	14						
		6	15						
		7	16						

For EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 2, the EMIF interleaves banks the same as for EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 0, but the interleaving of banks within a device (per CS) is limited to two banks. Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, but can interleave among only 4 of them.

15.3.4.12.4 Address Mapping for IBANK_POS = 3 and EBANK_POS = 0

Table 15-118 list the local address to SDRAM address mapping. There are x bits for bank, followed by y bits for row, followed by z bits for CS, and t bits for col in MAddr[31:2] (x, y, z, s, and t are given depending on the value of the EMIF_SDRAM_CONFIG bit fields).

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Table 15-118. Local Address to SDRAM Address Mapping for IBANK_POS = 3 and EBANK_POS = 0

MAddr[31:2]							
bank		row		cs		col	
IBANK	bank width (bits)	ROWSIZE	row width (bits)	EBANK	cs width (bits)	PAGESIZE	col width (bits)
0	0	0	9	0	0	0	8
1	1	1	10	1	1	1	9
2	2	2	11			2	10
3	3	3	12			3	11
		4	13				
		5	14				
		6	15				
		7	16				

For EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 3, the EMIF cannot interleave banks within a device (per CS). However, it can interleave banks between the two CSs. Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, but can interleave among only two of them.

15.3.4.12.5 Address Mapping for IBANK_POS = 0 and EBANK_POS = 1

Table 15-119 list the local address to SDRAM address mapping. There are z bits for CS, followed by y bits for row, followed by x bits for bank, and t bits for col in MAddr[31:2] (x, y, z and t are given depending on the value of the EMIF_SDRAM_CONFIG bit fields).

Table 15-119. Local Address to SDRAM Address Mapping for IBANK_POS = 0 and EBANK_POS = 1

MAddr[31:2]							
cs		row		bank		col	
EBANK	cs width (bits)	ROWSIZE	row width (bits)	IBANK	bank width (bits)	PAGESIZE	col width (bits)
0	0	0	9	0	0	0	8
1	1	1	10	1	1	1	9
		2	11	2	2	2	10
		3	12	3	3	3	11
		4	13				
		5	14				
		6	15				
		7	16				

For EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 0, and EMIF_SDRAM_CONFIG_2[27] EBANK_POS = 1, the EMIF interleaves among all the banks within a device (per CS), but cannot interleave banks between the two CSs. Thus, the EMIF can keep a maximum of 16 banks (8 internal banks across two CSs) open at a time, but can interleave among only 8 of them.

15.3.4.12.6 Address Mapping for IBANK_POS = 1 and EBANK_POS = 1

Table 15-120 list the local address to SDRAM address mapping. There are z bits for CS, followed by x bits for bank[2], followed by y bits for row, followed by s bits for bank[1:0],and t bits for col in MAddr[31:2] (x, y, z, s, and t are given depending on the value of the EMIF_SDRAM_CONFIG bit fields).

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Table 15-120. Local Address to SDRAM Address Mapping for IBANK_POS = 1 and EBANK_POS = 1

MAddr[31:2]									
cs		bank[2]		row		bank[1:0]		col	
EBANK	cs width (bits)	IBANK	bank[2] width (bits)	ROWSIZE	row width (bits)	IBANK	bank[1:0] width (bits)	PAGESIZE	col width (bits)
0	0	0	0	0	9	0	0	0	8
1	1	1	0	1	10	1	1	1	9
		2	0	2	11	2	2	2	10
		3	1	3	12	3	2	3	11
				4	13				
				5	14				
				6	15				
				7	16				

For EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 1, and EMIF_SDRAM_CONFIG_2[27] EBANK_POS = 1, the EMIF interleaves banks the same as for EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 0, but the interleaving of banks within a device (per CS) is limited to four banks. Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, but can interleave among only 4 of them.

15.3.4.12.7 Address Mapping for IBANK_POS = 2 and EBANK_POS = 1

Table 15-121 list the local address to SDRAM address mapping. There are z bits for CS, followed by x bits for bank[2:1], followed by y bits for row, followed by s bits for bank[0],and t bits for col in MAddr[31:2] (x, y, z, s, and t are given depending on the value of the EMIF_SDRAM_CONFIG bit fields).

Table 15-121. Local Address to SDRAM Address Mapping for IBANK_POS = 2 and EBANK_POS = 1

MAddr[31:2]									
cs		bank[2:1]		row		bank[0]		col	
EBANK	cs width (bits)	IBANK	bank[2:1] width (bits)	ROWSIZE	row width (bits)	IBANK	bank[0] width (bits)	PAGESIZE	col width (bits)
0	0	0	0	0	9	0	0	0	8
1	1	1	0	1	10	1	1	1	9
		2	1	2	11	2	1	2	10
		3	2	3	12	3	1	3	11
				4	13				
				5	14				
				6	15				
				7	16				

For EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 2 and EMIF_SDRAM_CONFIG_2[27] EBANK_POS = 1, the EMIF interleaves banks the same as for EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 0, but the interleaving of banks within a device (per CS) is limited to two banks. Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, but can interleave among only two of them.

15.3.4.12.8 Address Mapping for IBANK_POS = 3 and EBANK_POS = 1

list the local address to SDRAM address mapping. There are z bits for CS, followed by x bits for bank, followed by y bits for row, and t bits for col in MAddr[31:2] (x, y, z and t are given depending on the value of the EMIF_SDRAM_CONFIG bit fields).

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Table 15-122. Local Address to SDRAM Address Mapping for IBANK_POS = 3 and EBANK_POS = 1

MAddr[31:2]							
cs		bank		row		col	
EBANK	cs width (bits)	IBANK	bank width (bits)	ROWSIZE	row width (bits)	PAGESIZE	col width (bits)
0	0	0	0	0	9	0	8
1	1	1	1	1	10	1	9
		2	2	2	11	2	10
		3	3	3	12	3	11
				4	13		
				5	14		
				6	15		
				7	16		

For EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 3 and EMIF_SDRAM_CONFIG_2[27] EBANK_POS = 1, the EMIF cannot interleave banks within a device (per CS). Thus, the EMIF can keep a maximum of 16 banks (eight internal banks across two CSs) open at a time, but cannot interleave among them.

NOTE: Because the EMIF interleaves among a fewer number of banks when EMIF_SDRAM_CONFIG[28:27] IBANK_POS ≠ 0 or EMIF_SDRAM_CONFIG_2[27] EBANK_POS = 1, these cases are lower in performance than the EMIF_SDRAM_CONFIG[28:27] IBANK_POS = 0 case. Thus, these cases are recommended to be used only with partial array self-refresh where performance can be traded off for power savings.

15.3.4.13 Output Impedance Calibration

The EMIF supports automatic output impedance calibration. The ZQ calibration can be enabled per CS by setting the EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[31] ZQ_CS1EN and EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[30] ZQ_CS0EN bits. The EMIF supports three types of ZQ calibration commands:

- ZQINIT: ZQ calibration command during initialization
- ZQCS: ZQ calibration short command
- ZQCL: ZQ calibration long command

For DDR3, the EMIF automatically issues a ZQINIT command during initialization. For LPDDR2, software must issue a ZQINIT command (MRW to mode register 10). EMIF waits and blocks any other command for (ZQ_ZQINIT_MULT + 1) × (ZQ_ZQCL_MULT + 1) × (ZQ_ZQCS + 1) number of DDR clock cycles every time a ZQINIT command is issued. The bit fields used are:

- EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[19:18] ZQ_ZQINIT_MULT
- EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[17:16] ZQ_ZQCL_MULT
- EMIF_SDRAM_TIMING_3[20:15] ZQ_ZQCS

The EMIF issues a ZQCS command each time the EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[15:0] ZQ_REFINTERVAL bit field expires. In other words, the ZQ_REFINTERVAL defines the interval between ZQCS commands. When a ZQCS command is issued, the EMIF waits and blocks any other command for (EMIF_SDRAM_TIMING_3[20:15] ZQ_ZQCS + 1) number of DDR clock cycles.

If the EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[28] ZQ_SFEXITEN bit field is set to 1, the EMIF issues a ZQCL command every time it exits self-refresh modes. When a ZQCL command is issued, the EMIF waits and blocks any other command for (EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[17:16] ZQ_ZQCL_MULT + 1) × (EMIF_SDRAM_TIMING_3[20:15] ZQ_ZQCS + 1) number of DDR clock cycles.

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If a separate calibration resistor is used per device, the ZQ calibration can be performed simultaneously over both CSs. To enable ZQ calibration to be performed simultaneously over both CSs, the EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[27] ZQ_DUALCALEN bit must be set to 1. If ZQ_DUALCALEN is set to 0, the EMIF performs ZQ calibration per CS serially.

15.3.4.14 LPDDR2 Temperature Monitoring

The EMIF supports automatic temperature monitoring to facilitate the software update of the refresh rate according to the temperature changes of the LPDDR2. Temperature monitoring can be enabled per CS by setting the EMIF_TEMPERATURE_ALERT_CONFIG[31] TA_CS1EN and EMIF_TEMPERATURE_ALERT_CONFIG[30] TA_CS0EN bits.

The EMIF polls the temperature of the LPDDR2 (issues an MRR command to mode register 4) every time the EMIF_TEMPERATURE_ALERT_CONFIG[21:0] TA_REFINTERVAL bit field expires. In other words, TA_REFINTERVAL defines the interval between temperature alert polls. If the EMIF sees a 1 on bit 7 of the read data value from the MRR, which indicates the temperature has changed, the EMIF_SYSTEM_OCP_INTERRUPT_STATUS[1] TA_SYS bit (for system interface) and EMIF_LOW_LATENCY_OCP_INTERRUPT_STATUS[1] TA_LL bit (for low-latency interface) are set and the module sends an interrupt on the system and low-latency interrupt lines, respectively. When the interrupt is received, software must update the EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE bit field to the required value as per the temperature change.

If the EMIF_TEMPERATURE_ALERT_CONFIG[28] TA_SFEXITEN bit is set to 1, the EMIF polls for temperature change every time it exits self-refresh, active power-down, and precharge power-down modes.

Because the EMIF is performing an MRR, it needs information about how the LPDDR2 is connected. The EMIF_TEMPERATURE_ALERT_CONFIG[27:26] TA_DEVWDT and EMIF_TEMPERATURE_ALERT_CONFIG[25:24] TA_DEVCNT bit fields provide the necessary information to the EMIF for MRR data compare. For example, if TA_DEVWDT is set to 0, which indicates 8-bit devices are used, and if TA_DEVCNT is set to 2, which indicates four devices are used to form a 32-bit bus, the mask used for checking is 4'b1111; that is, the EMIF expects data on each byte lane on a 32-bit bus.

15.3.4.15 Performance Counters

The EMIF_PERFORMANCE_COUNTER_1 and EMIF_PERFORMANCE_COUNTER_2 registers can be used to monitor or calculate the EMIF bandwidth and efficiency. These counters can count events such as total SDRAM accesses, SDRAM activates, reads, writes, etc. Each counter counts events independent of the other counters. In addition to the ability to count events, the counters can also filter the events from a particular master or address space. The events to be counted and the filter enabling can be configured using the EMIF_PERFORMANCE_COUNTER_CONFIG register. The filter value to be used can be configured using the EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT register. Each counter can be configured independently.

Table 15-123 lists all the events that can be counted and whether a filter can be applied to a particular event. A filter can be applied to an event if the following bits for Performance Counter 1 and Performance Counter 2 can be set equal to 0x1 for that event:

- Performance Counter 1: EMIF_PERFORMANCE_COUNTER_CONFIG[15] CNTR1_MCONNID_EN and EMIF_PERFORMANCE_COUNTER_CONFIG[14] CNTR1_REGION_EN
- Performance Counter 2: EMIF_PERFORMANCE_COUNTER_CONFIG[31] CNTR2_MCONNID_EN and EMIF_PERFORMANCE_COUNTER_CONFIG[30] CNTR2_REGION_EN

Table 15-123. Performance Counter Filter Configuration

CNTRn_CFG[1]	CNTRn_REGION_EN	CNTRn_MCONNID_EN	Description
0x0	0x0	0x0 or 0x1	Count total SDRAM accesses
0x1	0x0	0x0 or 0x1	Count total SDRAM activates
0x2	0x0 or 0x1	0x0 or 0x1	Count total reads
0x3	0x0 or 0x1	0x0 or 0x1	Count total writes

(1) n = 1 or 2

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Table 15-123. Performance Counter Filter Configuration (continued)

CNTRn_CFG[1]	CNTRn_REGION_EN	CNTRn_MCONNID_EN	Description
0x4	0x0	0x0	Count number of EMIF_COREi clock cycles local Command FIFO is full
0x5	0x0	0x0	Count number of EMIF_COREi clock cycles local Write Data FIFO is full
0x6	0x0	0x0	Count number of EMIF_COREi clock cycles local Read Data FIFO is full
0x7	0x0	0x0	Count number of EMIF_COREi clock cycles local Return Command FIFO is full
0x8	0x0 or 0x1	0x0 or 0x1	Count number of priority elevations
0x9	0x0	0x0	Count number of EMIF_COREi clock cycles that a command was pending
0xA	0x0	0x0	Count number of EMIF_COREi clock cycles for which the memory data bus was transferring data.
0xB - 0xF	0x0	0x0	Reserved for future use.

NOTE: When MReqDebug is set to 1 for a particular local command, the performance counters are not incremented for that particular command if the CNTRn_CONFIG values are equal to 0x0, 0x1, 0x2, 0x3, or 0xA.

Table 15-123 shows the possible filter configurations for the two performance counters. These filter configurations can be used in conjunction with a local master ID and/or an external chip-select to obtain performance statistics for a particular local master and/or an external chip-select.

The EMIF clock frequency is half the DDR speed.

15.3.4.15.1 Performance Counters General Examples

15.3.4.15.1.1 PERF_COUNTER_1 General Example for Counting Write Accesses

The Performance Counter 1 register must count all write accesses from the IPU subsystem:

- To enable counting writes, the EMIF_PERFORMANCE_COUNTER_CONFIG[3:0] CNTR1_CONFIG bit field must be set to 0x3.
- The EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT[15:8] MCONNID1 bit field must be set to 0x44. The values programmed into the MCONNIDx bit fields are those in *ConnID Mapping (Debug View)*, in , *On-Chip Debug Support*, left-shifted by 2 bits.
- To enable filtering, the EMIF_PERFORMANCE_COUNTER_CONFIG[15] CNTR1_MCONNID_EN bit must be set to 0x1.

With this configuration, Counter 1 counts every write made to the EMIF from master 0x44 to any address space. This does not include accesses from other masters and does not include commands other than writes.

15.3.4.15.1.2 PERF_COUNTER_2 General Example for Counting Total Access

The Performance Counter 2 register must count total accesses to SDRAM regardless of the masters or address space.

- To enable counting all SDRAM accesses, the EMIF_PERFORMANCE_COUNTER_CONFIG[19:16] CNTR2_CONFIG bit field must be set to 0x0.
- To disable filtering, the EMIF_PERFORMANCE_COUNTER_CONFIG[31] CNTR2_MCONNID_EN and EMIF_PERFORMANCE_COUNTER_CONFIG[30] CNTR2_REGION_EN bits must be set to 0x0.

With this configuration, Counter 2 counts every access made to the EMIF. This includes all accesses from all masters and to any address space.

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15.3.4.15.1.3 PERF_COUNTER_3 General Example for Counting all Read Accesses

The Performance Counter 1 register must count all read accesses from the IPU subsystem to address space 0x0.

- To enable counting reads, the EMIF_PERFORMANCE_COUNTER_CONFIG[3:0] CNTR1_CONFIG bit field must be set to 0x2.
- The EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT[15:8] MCONNID1 and EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT[1:0] REGION_SEL1 bit fields must be set to 0x44 and 0x0, respectively.
- To enable filtering, the EMIF_PERFORMANCE_COUNTER_CONFIG[15] CNTR1_MCONNID_EN and EMIF_PERFORMANCE_COUNTER_CONFIG[14] CNTR1_REGION_EN bits must be set to 0x1.

With this configuration, Counter 1 counts every read made to the EMIF from master 0x44 to address space 0x0. This does not include accesses from other masters or accesses to other address space and does not include commands other than reads.

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15.3.5 EMIF Programming Guide

15.3.5.1 EMIF Low-Level Programming Models

This section describers the low-level hardware programming sequences for the configuration and use of the EMIF module.

The following programming sequences are doubled, when the two EMIF modules (EMIF1 and EMIF2) are used.

15.3.5.1.1 Global Initialization

Table 15-124. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface and functional clocks must be enabled. See Section 3.1.1, *Power, Reset, and Clock Management*.
Interrupt submodule of the MPU	The interrupt requests from the EMIF must be enabled (unmasked). See Section 17.1, *Interrupt Controllers*.
DMM	The EMIF is a slave to the DMM. The DMM must be enabled and configured for communication with LPDDR2 memories. See Section 15.2.1, *Dynamic Memory Manager*.

15.3.5.1.1.1 EMIF Module Global Initialization

This procedure initializes the EMIF after a power-on reset. The unused bits in all registers should be written with zeros. The values of the shadow registers are loaded in their corresponding registers a frequency update sequence is performed.

Table 15-125. EMIF Global Initialization

Step	Register/ Bit Field / Programming Model	Value
Assign the external bank address bits from lower or higher L3 address as shown in Section 15.3.4.12, *SDRAM Address Mapping*.	EMIF_SDRAM_CONFIG_2[27] EBANK_POS	0x-
Select the SDRAM type (LPDDR2 S2 or S4, or DDR3)	EMIF_SDRAM_CONFIG[31:29] SDRAM_TYPE	0x-
Assign internal bank address bits from L3 address as shown in Section 15.3.4.12, *SDRAM Address Mapping*.	EMIF_SDRAM_CONFIG[28:27] IBANK_POS	0x-
Choose 32-bit SDRAM data bus.	EMIF_SDRAM_CONFIG[15:14] NARROW_MODE	0x0
Define CAS latency when accessing connected SDRAM devices.	EMIF_SDRAM_CONFIG[13:10] CL	0x-
Define the number of row address bits of connected SDRAM device.	EMIF_SDRAM_CONFIG[9:7] ROWSIZE	0x-
Define the number of banks inside connected SDRAM device.	EMIF_SDRAM_CONFIG[6:4] IBANK	0x-
Define whether SDRAM accesses use 1 or 2 chip-select lines.	EMIF_SDRAM_CONFIG[3] EBANK	0x-
Define the internal page size of connected SDRAM device.	EMIF_SDRAM_CONFIG[2:0] PAGESIZE	0x-
Configure the DDR PHY-specific settings. Refer to register descriptions of EMIF_DDR_PHY_CONTROL_1, and EMIF_EXT_PHY_CONTROL_1 through EMIF_EXT_PHY_CONTROL_24	EMIF_DDR_PHY_CONTROL_1, and EMIF_EXT_PHY_CONTROL_1 through EMIF_EXT_PHY_CONTROL_24	0x-
Initialize MR LPDDR2 registers	External LPDDR2 initialization, seeTable 15-128	
Define timings and clock parameters	EMIF Timing Initialization, see Table 15-126	

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Table 15-125. EMIF Global Initialization (continued)

Step	Register/ Bit Field / Programming Model	Value
Configure the SDRAM Output Impedance Calibration parameters	EMIF Output Impedance Calibration Mode, see Table 15-129	
Configure the Temperature Alert parameters	EMIF Temperature Monitoring Mode, see Table 15-138	
(Optional) Configure the Performance Counter Config Register	EMIF_PERFORMANCE_COUNTER_CONFIG	0x-
(Optional) Configure the Performance Counter Master Region Select Register	EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT	0x-
Configure the System, MPU and LL max number of transactions in the command FIFO	EMIF_OCP_CONFIG	0x-
Clear all eventual previous indications of treated interrupts.	EMIF_SYSTEM_OCP_INTERRUPT_STATUS, EMIF_LOW_LATENCY_OCP_INTERRUPT_STATUS	0x-
(Optional) Enable System L3 interrupt for Command or Address Error.	EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_SET[0] EN_ERR_SYS	0x1
DDR3-specific settings		
DDR3 write latency (WL)	EMIF_SDRAM_CONFIG[17:16] CWL	0x-
SDRAM drive strength	EMIF_SDRAM_CONFIG[19:18] SDRAM_DRIVE	0x-
Disable(=1)/enable DLL inside SDRAM	EMIF_SDRAM_CONFIG[20] DDR_DISABLE_DLL	0x-
DDR3 termination resistor value	EMIF_SDRAM_CONFIG[26:24] DDR_TERM	0x-
Partial array self refresh	EMIF_SDRAM_REFRESH_CONTROL[26:24] PASR	0x-
DDR3 auto self refresh enable(=1)/disable	EMIF_SDRAM_REFRESH_CONTROL[28] ASR	0x-
When the EMIF_SDRAM_REFRESH_CONTROL[28] ASR field is set to 0, set to 0 for normal operating temperature range and set to 1 for extended operating temperature range. Set to 0 if ASR field is set to 1.	EMIF_SDRAM_REFRESH_CONTROL[29] SRT	0x-

Table 15-126. Sub-process call summary for Main Sequence - EMIF Global Initialization

Sub-process Name	Crossreference
EMIF Timing Initialization	Table 15-127
EMIF Output Impedance Calibration Mode	Table 15-129
EMIF Temperature Monitoring Mode	Table 15-138
External LPDDR2 initialization	Table 15-128

15.3.5.1.1.2 Subsequence - EMIF Timing Initialization

Table 15-127. Subsequence - EMIF Timing Initialization

Step	Register/ Bit Field / Programming Model	Value
Determine the the required wait time after a phy_dll_calib is generated before another command can be sent	EMIF_DLL_CALIB_CTRL[19:16] ACK_WAIT	0x-
Determine the interval between phy_dll_calib generation	EMIF_DLL_CALIB_CTRL[8:0] DLL_CALIB_INTERVAL	0x-
Write the Shadow register of the EMIF_DLL_CALIB_CTRL with the same value.	EMIF_DLL_CALIB_CTRL_SHADOW	EMIF_DLL_CALIB_CTRL

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Table 15-127. Subsequence - EMIF Timing Initialization (continued)

Step	Register/ Bit Field / Programming Model	Value
Define the minimum number of DDR clock cycles from Precharge to Activate or Refresh, minus one.	EMIF_SDRAM_TIMING_1[28:25] T_RP	0x-
Define minimum number of DDR clock cycles from Activate to Read or Write, minus one.	EMIF_SDRAM_TIMING_1[24:21] T_RCD	0x-
Define minimum number of DDR clock cycles from last Write transfer to Precharge, minus one.	EMIF_SDRAM_TIMING_1[20:17] T_WR	0x-
Define minimum number of DDR clock cycles from Activate to Precharge, minus one.	EMIF_SDRAM_TIMING_1[16:12] T_RAS	0x-
Define Minimum number of DDR clock cycles from Activate to Activate, minus one.	EMIF_SDRAM_TIMING_1[11:6] T_RC	0x-
Define Minimum number of DDR clock cycles from Activate to Activate for a different bank, minus one.	EMIF_SDRAM_TIMING_1[5:3] T_RRD	0x-
Define Minimum number of DDR clock cycles from last Write to Read, minus one.	EMIF_SDRAM_TIMING_1[2:0] T_WTR	0x-
Write the Shadow register of the EMIF_SDRAM_TIMING_1 (1).	EMIF_SDRAM_TIMING_1_SHADOW (1)	0x-
Define minimum number of DDR clock cycles from Powerdown exit to any command other than a Read, minus one.	EMIF_SDRAM_TIMING_2[30:28] T_XP	0x-
Define minimum number of DDR clock cycles from Self-Refresh exit to any command other than a Read command, minus one.	EMIF_SDRAM_TIMING_2[24:16] T_XSNR	0x-
Define minimum number of DDR clock cycles from Self-Refresh exit to a Read command, minus one.	EMIF_SDRAM_TIMING_2[15:6] T_XSRD	0x-
Define minimum number of DDR clock cycles for the last read command to a Precharge command, minus one.	EMIF_SDRAM_TIMING_2[5:3] T_RTP	0x-
Write the Shadow register of the EMIF_SDRAM_TIMING_2 (2).	EMIF_SDRAM_TIMING_2_SHADOW (2)	0x-
Define minimum number of DDR clock cycles for which LPDDR2 must remain in Self Refresh, minus one.	EMIF_SDRAM_TIMING_3[23:21] T_CKESR	0x-
Define number of DDR clock cycles for a ZQCS command duration, minus one.	EMIF_SDRAM_TIMING_3[20:15] ZQ_ZQCS	0x-
Define number of DDR clock that satisfies tDQSCKmax for LPDDR2, minus one.	EMIF_SDRAM_TIMING_3[14:13] T_TDQSCKMAX	0x-
Define minimum number of DDR clock cycles from Refresh or Load Mode to Refresh or Activate, minus one.	EMIF_SDRAM_TIMING_3[12:4] T_RFC	0x-
Define maximum number of EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE intervals from Activate to Precharge command.	EMIF_SDRAM_TIMING_3[3:0] T_RAS_MAX	0x-
Write the Shadow register of the EMIF_SDRAM_TIMING_3 (2).	EMIF_SDRAM_TIMING_3_SHADOW (2)	0x-
Define the rate at which the connected SDRAM devices are refreshed.	EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE	0x-
Write the Shadow register of the EMIF_SDRAM_REFRESH_CONTROL with the same value.	EMIF_SDRAM_REFRESH_CONTROL_SHADOW	EMIF_SDRAM_REFRESH_CONTROL

(1) Values loaded in these registers depend on OPP.
(2) Values loaded in these registers depend on OPP.

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15.3.5.1.1.3 Subsequence - External LPDDR2 Initialization

Table 15-128. Subsequence - External LPDDR2 Initialization

Step	LPDDR2 mode registers (MR)	Value
Wait until MR0[0]=0 (MR0[0] = 0 indicates that memory auto – initialization is completed).	MR0[0]	=0
Issue ZQINIT calibration command.	MR10	0xFF
Configure BT, BL, WC.	MR1	0x-
Configure the memory latency settings (RL and WL).	MR2 (1)	0x-
Unmask memory banks.	MR16	0x-
Unmask memory segments.	MR17	0x-

(1) Memory latency settings (RL and WL) depend on OPP.

15.3.5.1.2 Operational Modes Configuration

15.3.5.1.2.1 EMIF Output Impedance Calibration Mode

Table 15-129. EMIF Output Impedance Calibration Mode

Step	Register/ Bit Field / Programming Model	Value
IF : Calibration per CS		
Determine on which chip select 1 or 0 the calibration is enabled.	EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[31:30] ZQ_CS1/0EN	0x-
ELSE : (Calibration on both the CS0 and CS1)		
Enable automatic output impedance calibration for both the chip selects simultaneously.	EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[29] ZQ_DUALCALEN	0x1
ENDIF		
Define the interval (number of refresh periods) between ZQCS commands.	EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[15:0] ZQ_REFINTERVAL	0x-
Define the number of ZQCL durations that build the ZQINIT duration.	EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[19:18] ZQ_ZQINIT_MULT	0x-
Define the number of ZQCS intervals that build the ZQCL duration.	EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[17:16] ZQ_ZQCL_MULT	0x-
Enable the issuing of ZQ-Long Command on Self-Refresh exit.	EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG[28] ZQ_SFEXITEN	0x1

15.3.5.1.2.2 EMIF MR Read

Table 15-130. EMIF MR Read

Step	Register/ Bit Field / Programming Model	Value
Choose chip-select 0 or 1 to issue mode register read command	EMIF_LPDDR2_MODE_REG_CONFIG[31] CS	0x-
Write the mode register (MR) address	EMIF_LPDDR2_MODE_REG_CONFIG[7:0] ADDRESS	0x-
Initiate Read command by reading the register	EMIF_LPDDR2_MODE_REG_DATA[7:0]	0x-

15.3.5.1.2.3 EMIF MR Write

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Table 15-131. EMIF MR Write

Step	Register/ Bit Field / Programming Model	Value
Choose chip-select 0 or 1 to issue mode register write command	EMIF_LPDDR2_MODE_REG_CONFIG[31] CS	0x-
Write the mode register (MR) address	EMIF_LPDDR2_MODE_REG_CONFIG[7:0] ADDRESS	0x-
Supply the Data Byte to be written and initiate Write command by writing the register	EMIF_LPDDR2_MODE_REG_DATA[7:0] VALUE_0	0x-

15.3.5.1.2.4 EMIF SDRAM Self-Refresh

Table 15-132. EMIF SDRAM Self-Refresh Entering

Step	Register/ Bit Field / Programming Model	Value
Define the number of DDR clock cycles after which the EMIF puts the external SDRAM in Self Refresh mode, when EMIF is idle.	EMIF_POWER_MANAGEMENT_CONTROL[7:4] SR_TIM	0x-
Enable the Self-Refresh mode	EMIF_POWER_MANAGEMENT_CONTROL[10:8] LP_MODE	0x2
Write the shadow register of EMIF_POWER_MANAGEMENT_CONTROL	EMIF_POWER_MANAGEMENT_CONTROL_SHADOW	0x-

Table 15-133. EMIF SDRAM Self-Refresh Exiting

Step	Register/ Bit Field / Programming Model	Value
Change LP_MODE bitfield from 0x2 to any value.	EMIF_POWER_MANAGEMENT_CONTROL[10:8] LP_MODE	0x-
Write the shadow register of EMIF_POWER_MANAGEMENT_CONTROL	EMIF_POWER_MANAGEMENT_CONTROL_SHADOW	0x-

15.3.5.1.2.5 EMIF LPDDR2 Power-Down Mode

Table 15-134. EMIF SDRAM Power-Down Mode Entering

Step	Register/ Bit Field / Programming Model	Value
Define the number of DDR clock cycles after which the EMIF puts the external SDRAM in Power Down mode, when EMIF is idle.	EMIF_POWER_MANAGEMENT_CONTROL[15:12] PD_TIM	0x-
Enable (enter) the Power-down mode	EMIF_POWER_MANAGEMENT_CONTROL[10:8] LP_MODE	0x4
Write the shadow register of EMIF_POWER_MANAGEMENT_CONTROL	EMIF_POWER_MANAGEMENT_CONTROL_SHADOW	0x-

Table 15-135. EMIF SDRAM Power-Down Mode Exiting

Step	Register/ Bit Field / Programming Model	Value
Change LP_MODE bitfield from 0x4 to any value.	EMIF_POWER_MANAGEMENT_CONTROL[10:8] LP_MODE	0x-
Write the shadow register of EMIF_POWER_MANAGEMENT_CONTROL	EMIF_POWER_MANAGEMENT_CONTROL_SHADOW	0x-

15.3.5.1.2.6 EMIF LPDDR2-SDRAM Deep Power-Down Mode

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Table 15-136. EMIF LPDDR2-SDRAM Deep Power-Down Mode Entering

Step	Register/ Bit Field / Programming Model	Value
Define the number of DDR clock cycles after which the EMIF puts the external SDRAM in Power saving mode, when EMIF is idle.	EMIF_POWER_MANAGEMENT_CONTROL[3:0] CS_TIM	0x-
Enable (enter) the Deep Power-Down mode	EMIF_POWER_MANAGEMENT_CONTROL[11] DPD_EN	0x1
Write the shadow register of EMIF_POWER_MANAGEMENT_CONTROL	EMIF_POWER_MANAGEMENT_CONTROL_SHADOW	0x-

Table 15-137. EMIF LPDDR2-SDRAM Deep Power-Down Mode Exiting

Step	Register/ Bit Field / Programming Model	Value
Clear DPD_EN bit.	EMIF_POWER_MANAGEMENT_CONTROL[11] DPD_EN	0
Write the shadow register of EMIF_POWER_MANAGEMENT_CONTROL	EMIF_POWER_MANAGEMENT_CONTROL_SHADOW	0x-

NOTE: After Deep Power-Down exit, software must perform initialization as specified in Table 15-128.

15.3.5.1.2.7 LPDDR2 Temperature Monitoring Mode

Table 15-138. LPDDR2 Temperature Monitoring Mode

Step	Register/ Bit Field / Programming Model	Value
Determine which chip-select 1 or 0 is used for Temperature Alert Polling	EMIF_TEMPERATURE_ALERT_CONFIG[31] TA_CS1EN EMIF_TEMPERATURE_ALERT_CONFIG[30] TA_CS0EN	0x-
Define the interval (number of refresh periods) between temperature alert polls.	EMIF_TEMPERATURE_ALERT_CONFIG[21:0] TA_REFINTERVAL	0x-
Define the width of the physical memory device	EMIF_TEMPERATURE_ALERT_CONFIG[27:26] TA_DEVWDT	0x-
Define which external byte lanes contain a device for temperature monitoring (which devices to be polled).	EMIF_TEMPERATURE_ALERT_CONFIG[25:24] TA_DEVCNT	0x-
(Optional) Enable the issuing of a temperature alert poll on Self-Refresh exit (poll for temperature change every time EMIF exits Self-Refresh, Active Power-Down, and Precharge Power-Down modes).	EMIF_TEMPERATURE_ALERT_CONFIG[28] TA_SFEXITEN	0x1
Enable System L3 interrupt for SDRAM temperature alert.	EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_SET[1] EN_TA_SYS	0x1

15.3.5.1.3 EMIF Events Servicing

15.3.5.1.3.1 Interrupt Servicing

This section covers the event servicing (interrupt treatment) of the EMIF module.

Please, have in mind that the following Interrupt mechanism is double as there are two EMIF modules with different register addresses and 2 Interrupt lines - EMIF1_IRQ and EMIF2_IRQ.

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Table 15-139. EMIF Event Servicing

Step	Register/ Bit Field / Programming Model	Value
Read the status registers:	EMIF_SYSTEM_OCP_INTERRUPT_STATUS	
IF :	EMIF_SYSTEM_OCP_INTERRUPT_STATUS[0]	=1
Read the Error Log register and determine the Addressing mode, Command type and the Connection ID of the first errored transaction.	EMIF_OCP_ERROR_LOG	
Clear corresponding status flag	EMIF_SYSTEM_OCP_INTERRUPT_STATUS[0] ERR_SYS	0x1
ELSE IF :	EMIF_SYSTEM_OCP_INTERRUPT_STATUS[1]	=1
Update the REFRESH_RATE to the required value as per the temperature change.	EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE	0x-
Clear corresponding status flag	EMIF_SYSTEM_OCP_INTERRUPT_STATUS[1] TA_SYS	0x1
ENDIF		
Disable interrupts if needed	EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_CLEAR[0] EN_ERR_SYS	0x1

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15.3.6 EMIF Register Manual

Table 15-140 lists the EMIF instance.

15.3.6.1 EMIF Instance Summary

Table 15-140. EMIF Instance Summary

Module Name	Base Address	Size
EMIF1	0x4C00 0000	16 MiB
EMIF2	0x4D00 0000	16 MiB

15.3.6.2 EMIF Registers

Many register values are programmed with full-speed DDR clock cycles, whereas EMIF always runs at half the speed of this clock. Because EMIF is only capable of decrementing these values at half speed (taking into account the minus 1 programming model) the following model applies for data issued on a lower bus:

- REG_VALUE = 0 → 2 DDR clocks
- REG_VALUE = 1 → 2 DDR clocks
- REG_VALUE = 2 → 4 DDR clocks
- REG_VALUE = 3 → 4 DDR clocks
- REG_VALUE = 4 → 6 DDR clocks
- REG_VALUE = 5 → 6 DDR clocks
- REG_VALUE = 6 → 8 DDR clocks
- REG_VALUE = 7 → 8 DDR clocks

Activate and deactivate commands use the upper bus. Register values associated with these operations follow the general rule:

- REG_VALUE = 0 → 1 DDR clocks
- REG_VALUE = 1 → 2 DDR clocks
- REG_VALUE = 2 → 2 DDR clocks
- REG_VALUE = 3 → 4 DDR clocks
- REG_VALUE = 4 → 4 DDR clocks
- REG_VALUE = 5 → 6 DDR clocks
- REG_VALUE = 6 → 6 DDR clocks

NOTE: Shadow registers are loaded on any frequency change or SidleReq/SidleAck transition at the point where the EMIF has put SDRAM into self-refresh mode.

CAUTION

All EMIF registers are limited to 32-bit data accesses; 8- and 16-bit accesses are not allowed because they can corrupt register content.

Table 15-141 summarizes the EMIF register mapping.

15.3.6.2.1 EMIF Register Summary

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Table 15-141. EMIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 Physical Address	EMIF2 Physical Address
EMIF_REVISION	R	32	0x0000 0000	0x4C00 0000	0x4D00 0000
EMIF_STATUS	R	32	0x0000 0004	0x4C00 0004	0x4D00 0004
EMIF_SDRAM_CONFIG	RW	32	0x0000 0008	0x4C00 0008	0x4D00 0008
EMIF_SDRAM_CONFIG_2	RW	32	0x0000 000C	0x4C00 000C	0x4D00 000C
EMIF_SDRAM_REFRESH_CONTROL	RW	32	0x0000 0010	0x4C00 0010	0x4D00 0010
EMIF_SDRAM_REFRESH_CONTROL_SHADOW	RW	32	0x0000 0014	0x4C00 0014	0x4D00 0014
EMIF_SDRAM_TIMING_1	RW	32	0x0000 0018	0x4C00 0018	0x4D00 0018
EMIF_SDRAM_TIMING_1_SHADOW	RW	32	0x0000 001C	0x4C00 001C	0x4D00 001C
EMIF_SDRAM_TIMING_2	RW	32	0x0000 0020	0x4C00 0020	0x4D00 0020
EMIF_SDRAM_TIMING_2_SHADOW	RW	32	0x0000 0024	0x4C00 0024	0x4D00 0024
EMIF_SDRAM_TIMING_3	RW	32	0x0000 0028	0x4C00 0028	0x4D00 0028
EMIF_SDRAM_TIMING_3_SHADOW	RW	32	0x0000 002C	0x4C00 002C	0x4D00 002C
RESERVED	RW	32	0x0000 0030	0x4C00 0030	0x4D00 0030
RESERVED	RW	32	0x0000 0034	0x4C00 0034	0x4D00 0034
EMIF_POWER_MANAGEMENT_CONTROL	RW	32	0x0000 0038	0x4C00 0038	0x4D00 0038
EMIF_POWER_MANAGEMENT_CONTROL_SHADOW	RW	32	0x0000 003C	0x4C00 003C	0x4D00 003C
EMIF_LPDDR2_MODE_REG_DATA	RW	32	0x0000 0040	0x4C00 0040	0x4D00 0040
EMIF_LPDDR2_MODE_REG_CONFIG	RW	32	0x0000 0050	0x4C00 0050	0x4D00 0050
EMIF_OCP_CONFIG	RW	32	0x0000 0054	0x4C00 0054	0x4D00 0054
EMIF_OCP_CONFIG_VALUE_1	R	32	0x0000 0058	0x4C00 0058	0x4D00 0058
EMIF_OCP_CONFIG_VALUE_2	R	32	0x0000 005C	0x4C00 005C	0x4D00 005C
EMIF_PERFORMANCE_COUNTER_1	R	32	0x0000 0080	0x4C00 0080	0x4D00 0080
EMIF_PERFORMANCE_COUNTER_2	R	32	0x0000 0084	0x4C00 0084	0x4D00 0084
EMIF_PERFORMANCE_COUNTER_CONFIG	RW	32	0x0000 0088	0x4C00 0088	0x4D00 0088
EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT	RW	32	0x0000 008C	0x4C00 008C	0x4D00 008C
EMIF_PERFORMANCE_COUNTER_TIME	R	32	0x0000 0090	0x4C00 0090	0x4D00 0090
EMIF_MISC_REG	RW	32	0x0000 0094	0x4C00 0094	0x4D00 0094
EMIF_DLL_CALIB_CTRL	RW	32	0x0000 0098	0x4C00 0098	0x4D00 0098
EMIF_DLL_CALIB_CTRL_SHADOW	RW	32	0x0000 009C	0x4C00 009C	0x4D00 009C
EMIF_SYSTEM_OCP_INTERRUPT_RAW_STATUS	RW	32	0x0000 00A4	0x4C00 00A4	0x4D00 00A4
EMIF_LOW_LATENCY_OCP_INTERRUPT_RAW_STATUS	RW	32	0x0000 00A8	0x4C00 00A8	0x4D00 00A8
EMIF_SYSTEM_OCP_INTERRUPT_STATUS	RW	32	0x0000 00AC	0x4C00 00AC	0x4D00 00AC
EMIF_LOW_LATENCY_OCP_INTERRUPT_STATUS	RW	32	0x0000 00B0	0x4C00 00B0	0x4D00 00B0
EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_SET	RW	32	0x0000 00B4	0x4C00 00B4	0x4D00 00B4
EMIF_LOW_LATENCY_OCP_INTERRUPT_ENABLE_SET	RW	32	0x0000 00B8	0x4C00 00B8	0x4D00 00B8

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Table 15-141. EMIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 Physical Address	EMIF2 Physical Address
EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_CLEAR	RW	32	0x0000 00BC	0x4C00 00BC	0x4D00 00BC
EMIF_LOW_LATENCY_OCP_INTERRUPT_ENABLE_CLEAR	RW	32	0x0000 00C0	0x4C00 00C0	0x4D00 00C0
EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG	RW	32	0x0000 00C8	0x4C00 00C8	0x4D00 00C8
EMIF_TEMPERATURE_ALERT_CONFIG	RW	32	0x0000 00CC	0x4C00 00CC	0x4D00 00CC
EMIF_OCP_ERROR_LOG	R	32	0x0000 00D0	0x4C00 00D0	0x4D00 00D0
EMIF_READ_WRITE_LEVELING_RAMP_WINDOW	RW	32	0x0000 00D4	0x4C00 00D4	0x4D00 00D4
EMIF_READ_WRITE_LEVELING_RAMP_CONTROL	RW	32	0x0000 00D8	0x4C00 00D8	0x4D00 00D8
EMIF_READ_WRITE_LEVELING_CONTROL	RW	32	0x0000 00DC	0x4C00 00DC	0x4D00 00DC
EMIF_DDR_PHY_CONTROL_1	RW	32	0x0000 00E4	0x4C00 00E4	0x4D00 00E4
EMIF_DDR_PHY_CONTROL_1_SHADOW	RW	32	0x0000 00E8	0x4C00 00E8	0x4D00 00E8
EMIF_READ_WRITE_EXECUTION_THRESHOLD	RW	32	0x0000 0120	0x4C00 0120	0x4D00 0120
EMIF_PHY_STATUS_1	R	32	0x0000 0140	0x4C00 0140	0x4D00 0140
EMIF_PHY_STATUS_20	R	32	0x0000 018C	0x4C00 018C	0x4D00 018C
EMIF_PHY_STATUS_21	R	32	0x0000 0190	0x4C00 0190	0x4D00 0190
EMIF_EXT_PHY_CONTROL_1	RW	32	0x0000 0200	0x4C00 0200	0x4D00 0200
EMIF_EXT_PHY_CONTROL_1_SHADOW	RW	32	0x0000 0204	0x4C00 0204	0x4D00 0204
EMIF_EXT_PHY_CONTROL_2	RW	32	0x0000 0208	0x4C00 0208	0x4D00 0208
EMIF_EXT_PHY_CONTROL_2_SHADOW	RW	32	0x0000 020C	0x4C00 020C	0x4D00 020C
EMIF_EXT_PHY_CONTROL_3	RW	32	0x0000 0210	0x4C00 0210	0x4D00 0210
EMIF_EXT_PHY_CONTROL_3_SHADOW	RW	32	0x0000 0214	0x4C00 0214	0x4D00 0214
EMIF_EXT_PHY_CONTROL_4	RW	32	0x0000 0218	0x4C00 0218	0x4D00 0218
EMIF_EXT_PHY_CONTROL_4_SHADOW	RW	32	0x0000 021C	0x4C00 021C	0x4D00 021C
EMIF_EXT_PHY_CONTROL_5	RW	32	0x0000 0220	0x4C00 0220	0x4D00 0220
EMIF_EXT_PHY_CONTROL_5_SHADOW	RW	32	0x0000 0224	0x4C00 0224	0x4D00 0224
EMIF_EXT_PHY_CONTROL_6	RW	32	0x0000 0228	0x4C00 0228	0x4D00 0228
EMIF_EXT_PHY_CONTROL_6_SHADOW	RW	32	0x0000 022C	0x4C00 022C	0x4D00 022C
EMIF_EXT_PHY_CONTROL_7	RW	32	0x0000 0230	0x4C00 0230	0x4D00 0230
EMIF_EXT_PHY_CONTROL_7_SHADOW	RW	32	0x0000 0234	0x4C00 0234	0x4D00 0234
EMIF_EXT_PHY_CONTROL_8	RW	32	0x0000 0238	0x4C00 0238	0x4D00 0238
EMIF_EXT_PHY_CONTROL_8_SHADOW	RW	32	0x0000 023C	0x4C00 023C	0x4D00 023C
EMIF_EXT_PHY_CONTROL_9	RW	32	0x0000 0240	0x4C00 0240	0x4D00 0240
EMIF_EXT_PHY_CONTROL_9_SHADOW	RW	32	0x0000 0244	0x4C00 0244	0x4D00 0244
EMIF_EXT_PHY_CONTROL_10	RW	32	0x0000 0248	0x4C00 0248	0x4D00 0248

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Table 15-141. EMIF Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 Physical Address	EMIF2 Physical Address
EMIF_EXT_PHY_CONTROL_10_SHADOW	RW	32	0x0000 024C	0x4C00 024C	0x4D00 024C
EMIF_EXT_PHY_CONTROL_11	RW	32	0x0000 0250	0x4C00 0250	0x4D00 0250
EMIF_EXT_PHY_CONTROL_11_SHADOW	RW	32	0x0000 0254	0x4C00 0254	0x4D00 0254
EMIF_EXT_PHY_CONTROL_12	RW	32	0x0000 0258	0x4C00 0258	0x4D00 0258
EMIF_EXT_PHY_CONTROL_12_SHADOW	RW	32	0x0000 025C	0x4C00 025C	0x4D00 025C
EMIF_EXT_PHY_CONTROL_13	RW	32	0x0000 0260	0x4C00 0260	0x4D00 0260
EMIF_EXT_PHY_CONTROL_13_SHADOW	RW	32	0x0000 0264	0x4C00 0264	0x4D00 0264
EMIF_EXT_PHY_CONTROL_14	RW	32	0x0000 0268	0x4C00 0268	0x4D00 0268
EMIF_EXT_PHY_CONTROL_14_SHADOW	RW	32	0x0000 026C	0x4C00 026C	0x4D00 026C
EMIF_EXT_PHY_CONTROL_15	RW	32	0x0000 0270	0x4C00 0270	0x4D00 0270
EMIF_EXT_PHY_CONTROL_15_SHADOW	RW	32	0x0000 0274	0x4C00 0274	0x4D00 0274
EMIF_EXT_PHY_CONTROL_16	RW	32	0x0000 0278	0x4C00 0278	0x4D00 0278
EMIF_EXT_PHY_CONTROL_16_SHADOW	RW	32	0x0000 027C	0x4C00 027C	0x4D00 027C
EMIF_EXT_PHY_CONTROL_17	RW	32	0x0000 0280	0x4C00 0280	0x4D00 0280
EMIF_EXT_PHY_CONTROL_17_SHADOW	RW	32	0x0000 0284	0x4C00 0284	0x4D00 0284
EMIF_EXT_PHY_CONTROL_18	RW	32	0x0000 0288	0x4C00 0288	0x4D00 0288
EMIF_EXT_PHY_CONTROL_18_SHADOW	RW	32	0x0000 028C	0x4C00 028C	0x4D00 028C
EMIF_EXT_PHY_CONTROL_19	RW	32	0x0000 0290	0x4C00 0290	0x4D00 0290
EMIF_EXT_PHY_CONTROL_19_SHADOW	RW	32	0x0000 0294	0x4C00 0294	0x4D00 0294
EMIF_EXT_PHY_CONTROL_20	RW	32	0x0000 0298	0x4C00 0298	0x4D00 0298
EMIF_EXT_PHY_CONTROL_20_SHADOW	RW	32	0x0000 029C	0x4C00 029C	0x4D00 029C
EMIF_EXT_PHY_CONTROL_21	RW	32	0x0000 02A0	0x4C00 02A0	0x4D00 02A0
EMIF_EXT_PHY_CONTROL_21_SHADOW	RW	32	0x0000 02A4	0x4C00 02A4	0x4D00 02A4
EMIF_EXT_PHY_CONTROL_22	RW	32	0x0000 02A8	0x4C00 02A8	0x4D00 02A8
EMIF_EXT_PHY_CONTROL_22_SHADOW	RW	32	0x0000 02AC	0x4C00 02AC	0x4D00 02AC
EMIF_EXT_PHY_CONTROL_23	RW	32	0x0000 02B0	0x4C00 02B0	0x4D00 02B0
EMIF_EXT_PHY_CONTROL_23_SHADOW	RW	32	0x0000 02B4	0x4C00 02B4	0x4D00 02B4
EMIF_EXT_PHY_CONTROL_24	RW	32	0x0000 02B8	0x4C00 02B8	0x4D00 02B8
EMIF_EXT_PHY_CONTROL_24_SHADOW	RW	32	0x0000 02BC	0x4C00 02BC	0x4D00 02BC

15.3.6.2.2 EMIF Register Description

through describe the individual EMIF registers.

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Table 15-142. EMIF_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4C00 0000 0x4D00 0000	**Instance**	EMIF1 EMIF2
Description	Revision number register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	Module revision	R	0x- [1]

[1] TI internal data

Table 15-143. Register Call Summary for Register EMIF_REVISION

EMIF Controller

- Arbitration of Commands in the Command FIFO: [0] [1]
- EMIF Register Summary: [2]

Table 15-144. EMIF_STATUS

Address Offset	0x0000 0004		
Physical Address	0x4C00 0004 0x4D00 0004	**Instance**	EMIF1 EMIF2
Description	SDRAM Status Register (STATUS)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BE	DUAL_CLK_MODE	FAST_INIT	RESERVED																					RDLVLGATETO	RDLVLTO	WRLVLTO	RESERVED	PHY_DLL_READY	RESERVED		

Bits	Field Name	Description	Type	Reset
31	BE	Big endian mode select for 8 and 16-bit devices, set to 1 for big endian or 0 for little endian operation. In current implementation, only 32-bit devices are supported - this bit is don't care.	R	0
30	DUAL_CLK_MODE	Dual Clock mode. Defines whether the EMIFi_L3_ICLK and EMIF_COREi clock are asynchronous. EMIFi_L3_ICLK and EMIF_COREi clock are asynchronous, if set to 1.	R	0
29	FAST_INIT	Fast Init. Defines whether the EMIF fast initialization mode has been enabled. Fast initialization is enabled if set to 1.	R	0
28:7	RESERVED	Reserved	R	0x00 0000
6	RDLVLGATETO	Read DQS Gate Training Timeout. Value of 1 indicates read DQS gate training has timed out because read DQS gate training done was not received from the PHY.	R	0
5	RDLVLTO	Read Data Eye Training Timeout. Value of 1 indicates read data eye training has timed out because read data eye training done was not received from the PHY.	R	0

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Bits	Field Name	Description	Type	Reset
4	WRLVLTO	Write Leveling Timeout. Value of 1 indicates write leveling has timed out because write leveling done was not received from the PHY.	R	0
3	RESERVED		R	0
2	PHY_DLL_READY	DDR PHY Ready. The DDR PHY is ready for normal operation, if set to 1.	R	0
1:0	RESERVED	Reserved	R	0x0

Table 15-145. Register Call Summary for Register EMIF_STATUS

EMIF Controller

- EMIF Register Summary: [0]

Table 15-146. EMIF_SDRAM_CONFIG

Address Offset 0x0000 0008

Physical Address 0x4C00 0008 (EMIF1), 0x4D00 0008 (EMIF2) **Instance** EMIF1, EMIF2

Description SDRAM Config Register.
A write to this register will cause the EMIF to start the SDRAM initialization sequence. For LPDDR2, initialization is only re-started if it was not performed previously because EMIF_SDRAM_REFRESH_CONTROL[31] INITREF_DIS was a zero.
CAUTION: This register is loaded with values by control module at device reset.

Type RW

31 30 29	28 27 26	25 24	23	22	21 20	19 18	17 16	15 14	13 12 11 10	9 8	7 6 5 4	3 2	1 0
SDRAM_TYPE	IBANK_POS	DDR_TERM	DDR2_DDQS	DYN_ODT	DDR_DISABLE_DLL	SDRAM_DRIVE	CWL	NARROW_MODE	CL	ROWSIZE	IBANK	EBANK	PAGESIZE

Bits	Field Name	Description	Type	Reset
31:29	SDRAM_TYPE	SDRAM Type selection. This field is loaded from e-fuse. Set to 3 for DDR3 Set to 4 for LPDDR2 All other values are reserved.	RW	0x0
28:27	IBANK_POS	Internal bank position. See section Section 15.3.4.12, *SDRAM Address Mapping*.	RW	0x0
26:24	DDR_TERM	DDR3 termination resistor value. Set to 0 to disable termination. For DDR3, set to 1 for RZQ/4, set to 2 for RZQ/2, set to 3 for RZQ/6, set to 4 for RZQ/12, and set to 5 for RZQ/8. All other values are reserved.	RW	0x0
23	DDR2_DDQS	DDR2 differential DDQS enable. NOT SUPPORTED. Set to 1 for compatibility.	RW	0
22:21	DYN_ODT	DDR3 Dynamic ODT. NOT SUPPORTED. Set to 0 to turn off dynamic ODT.	RW	0x0
20	DDR_DISABLE_DLL	Disable DLL select. Set to 1 to disable DLL inside SDRAM.	RW	0
19:18	SDRAM_DRIVE	SDRAM drive strength.For DDR3, set to 0 for RZQ/6 and set to 1 for RZQ/7. All other values are reserved.	RW	0x0

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Bits	Field Name	Description	Type	Reset
17:16	CWL	DDR3 CAS Write latency. Value of 0, 1, 2, and 3 (CAS write latency of 5, 6, 7, and 8) are supported. Use the lowest value supported for best performance. All other values are reserved.	RW	0x0
15:14	NARROW_MODE	SDRAM data bus width. Set to 0 for 32-bit and set to 1 for 16-bit. All other values are reserved. In the current implementation, only 32-bit devices are supported. Two DDR3 devices are used in parallel to make one 32-bit device.	RW	0x0
13:10	CL	CAS Latency (referred to as read latency (RL) in some SDRAM specs). The value of this field defines the CAS latency to be used when accessing connected SDRAM devices. Values of 3, 4, 5, 6, 7, and 8 (CAS latency of 3, 4, 5, 6, 7, and 8) are supported for LPDDR2-SDRAM. Values of 2, 4, 6, 8, 10, 12, and 14 (CAS latency of 5, 6, 7, 8, 9, 10, and 11) are supported for DDR3. All other values are reserved. The write latency (WL) is tied to the RL for the LPDDR2. See the LPDDR2 SDRAM standard. Also program the EMIF_DDR_PHY_CONTROL_1[4:0] READ_LATENCY	RW	0x0
9:7	ROWSIZE	Row Size. Defines the number of row address bits of connected SDRAM devices. Set to 0 for 9 row bits, Set to 1 for 10 row bits, Set to 2 for 11 row bits, Set to 3 for 12 row bits, Set to 4 for 13 row bits, Set to 5 for 14 row bits, Set to 6 for 15 row bits, Set to 7 for 16 row bits. This field is only used when EMIF_SDRAM_CONFIG[28:27] IBANK_POS field is set to 1, 2, or 3 or EBANK_POS field in EMIF_SDRAM_CONFIG_2 register is set to 1.	RW	0x0
6:4	IBANK	Internal Bank setup. Defines number of banks inside connected SDRAM devices. Set to 0 for 1 bank, Set to 1 for 2 banks, Set to 2 for 4 banks, Set to 3 for 8 banks. All other values are reserved.	RW	0x0
3	EBANK	External chip select setup. Defines whether SDRAM accesses will use 1 or 2 chip select lines. Set to 0 to use NCS0 only. Set to 1 to use NCS[1:0]. This bit will automatically be set to 0 if EMIF_SDRAM_CONFIG_2[30] CS1NVMEN field is set to 1.	RW	0
2:0	PAGESIZE	Page Size. Defines the internal page size of connected SDRAM devices. Set to 0 for 256-word page (8 column bits), Set to 1 for 512-word page (9 column bits), Set to 2 for 1024-word page (10 column bits), Set to 3 for 2048-word page (11 column bits). All other values are reserved.	RW	0x0

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Table 15-147. Register Call Summary for Register EMIF_SDRAM_CONFIG

EMIF Controller

- Arbitration of Commands in the Command FIFO: [0]
- Self-Refresh Mode: [1] [2] [3] [4] [5] [6] [7]
- LPDDR2 SDRAM Initialization: [8] [9] [10] [11]
- DDR3 Initialization: [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]
- EMIF Access Cycles: [24]
- SDRAM Address Mapping: [25] [26] [27] [28] [29] [30] [31] [32] [33]
- Address Mapping for IBANK_POS = 0 and EBANK_POS = 0: [34] [35] [36]
- Address Mapping for IBANK_POS = 1 and EBANK_POS = 0: [37] [38] [39]
- Address Mapping for IBANK_POS = 2 and EBANK_POS = 0: [40] [41] [42]
- Address Mapping for IBANK_POS = 3 and EBANK_POS = 0: [43] [44]
- Address Mapping for IBANK_POS = 0 and EBANK_POS = 1: [45] [46]
- Address Mapping for IBANK_POS = 1 and EBANK_POS = 1: [47] [48] [49]
- Address Mapping for IBANK_POS = 2 and EBANK_POS = 1: [50] [51] [52]
- Address Mapping for IBANK_POS = 3 and EBANK_POS = 1: [53] [54] [55] [56]
- EMIF Module Global Initialization: [57] [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68]
- EMIF Register Summary: [69]
- EMIF Register Description: [70]

Table 15-148. EMIF_SDRAM_CONFIG_2

Address Offset	0x0000 000C		
Physical Address	0x4C00 000C 0x4D00 000C	**Instance**	EMIF1 EMIF2
Description	SDRAM Config Register 2 **CAUTION:** This register is loaded with values by control module at device reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		CS1NVMEN		RESERVED				EBANK_POS							RESERVED											RDBNUM		RESERVED		RDBSIZE		

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30	CS1NVMEN	CS1 LPDDR2-NVM enable. NVMs are not supported at device level.	RW	0
29:28	RESERVED		R	0x0
27	EBANK_POS	External bank position. Set to 0 to assign external bank address bits from lower OCP address. Set to 1 to assign external bank address bits from higher OCP address bits. See section Section 15.3.4.12, *SDRAM Address Mapping*.	RW	0
26:6	RESERVED		R	0x00 0000
5:4	RDBNUM	Row Buffer setup. Defines number of row buffers inside connected LPDDR2-NVM devices. NVM devices are not supported at the device level. Set to 0 for 1 row buffer, set to 1 for 2 row buffers, set to 2 for 4 row buffers, and set to 3 for 8 row buffers. All other values are reserved.	RW	0x0
3	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
2:0	RDBSIZE	Row Data Buffer Size. Defines the row data buffer size of connected LPDDR2-NVM devices. NVM devices are not supported at the device level. Set to 0 for 32 bytes, set to 1 for 64 bytes, set to 2 for 128 bytes, set to 3 for 256 bytes, set to 4 for 512 bytes, set to 5 for 1024 bytes, set to 6 for 2048 bytes, and set to 7 for 4096 bytes.	RW	0x0

Table 15-149. Register Call Summary for Register EMIF_SDRAM_CONFIG_2

EMIF Controller

- LPDDR2 SDRAM Initialization: [0] [1]
- Address Mapping for IBANK_POS = 0 and EBANK_POS = 0: [2]
- Address Mapping for IBANK_POS = 0 and EBANK_POS = 1: [3]
- Address Mapping for IBANK_POS = 1 and EBANK_POS = 1: [4]
- Address Mapping for IBANK_POS = 2 and EBANK_POS = 1: [5]
- Address Mapping for IBANK_POS = 3 and EBANK_POS = 1: [6] [7]
- EMIF Module Global Initialization: [8]
- EMIF Register Summary: [9]
- EMIF Register Description: [10] [11]

Table 15-150. EMIF_SDRAM_REFRESH_CONTROL

Address Offset	0x0000 0010		
Physical Address	0x4C00 0010 0x4D00 0010	**Instance**	EMIF1 EMIF2
Description	SDRAM Refresh Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INITREF_DIS	RESERVED	SRT	ASR	RESERVED	PASR			RESERVED								REFRESH_RATE															

Bits	Field Name	Description	Type	Reset
31	INITREF_DIS	Initialization and Refresh disable. When set to 1, EMIF will disable SDRAM initialization and refreshes, but will carry out SDRAM write/read transactions.	RW	0
30	RESERVED		R	0
29	SRT	DDR3 Self Refresh temperature range. Set to 0 for normal operating temperature range and set to 1 for extended operating temperature range when the ASR field is set to 0. This bit must be set to 0 if the ASR field is set to 1. A write to this field will cause the EMIF to start the SDRAM initialization sequence.	RW	0
28	ASR	DDR3 Auto Self Refresh enable. Set to 1 for auto Self Refresh enable. Set to 0 for manual Self Refresh reference indicated by the SRT field. A write to this field will cause the EMIF to start the SDRAM initialization sequence.	RW	0
27	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
26:24	PASR	Partial Array Self Refresh. These bits get loaded into the Extended Mode Register of DDR3 during initialization. For DDR3, set to 0 for full array, set to 1 or 5 for 1/2 array, set to 2 or 6 for 1/4 array, set to 3 or 7 for 1/8 array, and set to 4 for 3/4 array to be refreshed. All other values are reserved. A write to this field will cause the EMIF to start the SDRAM initialization sequence.	RW	0x0
23:16	RESERVED		R	0x00
15:0	REFRESH_RATE	Refresh Rate. Value in this field is used to define the rate at which connected SDRAM devices will be refreshed. SDRAM refresh rate = REFRESH_RATE / EMIFi_PHY_FICLK. A 533-MHz DDR clock rate system that requires a 7.8 µs refresh rate would need 7.8 × 533 = 4157 or 0x103D value to be written. To avoid lock-up situations, the programmer must not program REFRESH_RATE < (6 × EMIF_SDRAM_TIMING_3[12:4] T_RFC).	RW	0x0000

Table 15-151. Register Call Summary for Register EMIF_SDRAM_REFRESH_CONTROL

EMIF Controller

- Arbitration of Commands in the Command FIFO: [0]
- Reset: [1]
- Self-Refresh Mode: [2]
- SDRAM Refresh Scheduling: [3] [4] [5]
- LPDDR2 SDRAM Initialization: [6] [7] [8]
- DDR3 Initialization: [9] [10] [11] [12] [13]
- LPDDR2 Temperature Monitoring: [14]
- EMIF Module Global Initialization: [15] [16] [17] [18]
- Subsequence - EMIF Timing Initialization: [19] [20] [21] [22]
- Interrupt Servicing: [23]
- EMIF Register Summary: [25]
- EMIF Register Description: [26] [27] [28] [29] [30] [31] [32]

Table 15-152. EMIF_SDRAM_REFRESH_CONTROL_SHADOW

Address Offset	0x0000 0014		
Physical Address	0x4C00 0014 0x4D00 0014	**Instance**	EMIF1 EMIF2
Description	SDRAM Refresh Control Shadow Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																REFRESH_RATE_SHDW															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	REFRESH_RATE_SHDW	Shadow field for REFRESH_RATE. This field is loaded into EMIF_SDRAM_REFRESH_CONTROL[15:0] REFRESH_RATE field when SIdleAck is asserted.	RW	0x0000

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Table 15-153. Register Call Summary for Register EMIF_SDRAM_REFRESH_CONTROL_SHADOW

EMIF Controller

- Subsequence - EMIF Timing Initialization: [0]
- EMIF Register Summary: [1]

Table 15-154. EMIF_SDRAM_TIMING_1

Address Offset	0x0000 0018		
Physical Address	0x4C00 0018 0x4D00 0018	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 1 Register. If this register is byte written, care must be taken that all the fields are written before performing any accesses to the SDRAM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_RTW			T_RP					T_RCD				T_WR				T_RAS					T_RC							T_RRD			T_WTR	

Bits	Field Name	Description	Type	Reset
31:29	T_RTW	Minimum number of DDR clock cycles between Read to Write data phases, minus one.	RW	0x0
28:25	T_RP	Minimum number of DDR clock cycles from Precharge to Activate or Refresh, minus one.	RW	0x0
24:21	T_RCD	Minimum number of DDR clock cycles from Activate to Read or Write, minus one.	RW	0x0
20:17	T_WR	Minimum number of DDR clock cycles from last Write transfer to Precharge, minus one.	RW	0x0
16:12	T_RAS	Minimum number of DDR clock cycles from Activate to Precharge, minus one. T_RAS value needs to be bigger than or equal to T_RDC value.	RW	0x00
11:6	T_RC	Minimum number of DDR clock cycles from Activate to Activate, minus one.	RW	0x00
5:3	T_RRD	Minimum number of DDR clock cycles from Activate to Activate for a different bank, minus one. For an 8-bank, this field must be equal to ((tFAW / (4 × tCK)) - 1).	RW	0x0
2:0	T_WTR	Minimum number of DDR clock cycles from last Write to Read, minus one.	RW	0x0

Table 15-155. Register Call Summary for Register EMIF_SDRAM_TIMING_1

EMIF Controller

- DDR3 Initialization: [0]
- Turnaround Time: [1] [2]
- Subsequence - EMIF Timing Initialization: [3] [4] [5] [6] [7] [8] [9] [10]
- EMIF Register Summary: [11]
- EMIF Register Description: [12] [13] [14] [15] [16] [17] [18] [19]

Table 15-156. EMIF_SDRAM_TIMING_1_SHADOW

Address Offset	0x0000 001C		
Physical Address	0x4C00 001C 0x4D00 001C	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 1 Shadow Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_RTW_SHDW			T_RP_SHDW					T_RCD_SHDW			T_WR_SHDW					T_RAS_SHDW								T_RC_SHDW								T_RRD_SHDW			T_WTR_SHDW		

Bits	Field Name	Description	Type	Reset
31:29	T_RTW_SHDW	Shadow field for T_RTW. This field is loaded into EMIF_SDRAM_TIMING_1[31:29] T_RTW field when SIdleAck is asserted.	RW	0x0
28:25	T_RP_SHDW	Shadow field for T_RP. This field is loaded into EMIF_SDRAM_TIMING_1[28:25] T_RP field when SIdleAck is asserted.	RW	0x0
24:21	T_RCD_SHDW	Shadow field for T_RCD. This field is loaded into EMIF_SDRAM_TIMING_1[24:21] T_RCD field when SIdleAck is asserted.	RW	0x0
20:17	T_WR_SHDW	Shadow field for T_WR. This field is loaded into EMIF_SDRAM_TIMING_1[20:17] T_WR field when SIdleAck is asserted.	RW	0x0
16:12	T_RAS_SHDW	Shadow field for T_RAS. This field is loaded into EMIF_SDRAM_TIMING_1[16:12] T_RAS field when SIdleAck is asserted.	RW	0x00
11:6	T_RC_SHDW	Shadow field for T_RC. This field is loaded into EMIF_SDRAM_TIMING_1[11:6] T_RC field when SIdleAck is asserted.	RW	0x00
5:3	T_RRD_SHDW	Shadow field for T_RRD. This field is loaded into EMIF_SDRAM_TIMING_1[5:3] T_RRD field when SIdleAck is asserted.	RW	0x0
2:0	T_WTR_SHDW	Shadow field for T_WTR. This field is loaded into EMIF_SDRAM_TIMING_1[2:0] T_WTR field when SIdleAck is asserted.	RW	0x0

Table 15-157. Register Call Summary for Register EMIF_SDRAM_TIMING_1_SHADOW

EMIF Controller

- Subsequence - EMIF Timing Initialization: [0]
- EMIF Register Summary: [1]

Table 15-158. EMIF_SDRAM_TIMING_2

Address Offset	0x0000 0020		
Physical Address	0x4C00 0020 0x4D00 0020	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 2 Register. If this register is byte written, care must be taken that all the fields are written before performing any accesses to the SDRAM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			T_XP					T_ODT								T_XSNR																T_XSRD												T_RTP					T_CKE			

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30:28	T_XP	Minimum number of DDR clock cycles from power-down exit to any command other than a read command, minus one.	RW	0x0
27:25	T_ODT	Minimum number of DDR clock cycles from ODT enable to write data driven for DDR3. Must be equal to tAOND.	RW	0x0
24:16	T_XSNR	Minimum number of DDR clock cycles from Self-Refresh exit to any command other than a Read command, minus one. For LPDDR2, T_XSNR and T_XSRD must be programmed with the same value (tXSR). For DDR3, the value of tXS must be programmed.	RW	0x000
15:6	T_XSRD	Minimum number of DDR clock cycles from Self-Refresh exit to a Read command, minus one. For LPDDR2, T_XSNR and T_XSRD must be programmed with the same value (tXSR). For DDR3, the value of tXSDLL must be programmed.	RW	0x000
5:3	T_RTP	Minimum number of DDR clock cycles for the last read command to a Precharge command, minus one.	RW	0x0
2:0	T_CKE	Minimum number of DDR clock cycles between CKE pin changes, minus one.	RW	0x0

Table 15-159. Register Call Summary for Register EMIF_SDRAM_TIMING_2

EMIF Controller

- Power-Down Mode: [0] [1]
- Self-Refresh Mode: [2] [3] [4] [5] [6]
- Subsequence - EMIF Timing Initialization: [7] [8] [9] [10] [11]
- EMIF Register Summary: [12]
- EMIF Register Description: [13] [14] [15] [16] [17]

Table 15-160. EMIF_SDRAM_TIMING_2_SHADOW

Address Offset	0x0000 0024		
Physical Address	0x4C00 0024 0x4D00 0024	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 2 Shadow Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		T_XP_SHDW			T_ODT_SHDW			T_XSNR_SHDW								T_XSRD_SHDW								T_RTP_SHDW				T_CKE_SHDW			

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30:28	T_XP_SHDW	Shadow field for T_XP. This field is loaded into EMIF_SDRAM_TIMING_2[30:28] T_XP field when SIdleAck is asserted.	RW	0x0
27:25	T_ODT_SHDW	Shadow field for T_ODT. This field is loaded into T_ODT field in SDRAM Timing 2 register when SIdleAck is asserted.	RW	0x0
24:16	T_XSNR_SHDW	Shadow field for T_XSNR. This field is loaded into EMIF_SDRAM_TIMING_2[24:16] T_XSNR field when SIdleAck is asserted.	RW	0x000

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Bits	Field Name	Description	Type	Reset
15:6	T_XSRD_SHDW	Shadow field for T_XSRD. This field is loaded into EMIF_SDRAM_TIMING_2[15:6] T_XSRD field when SIdleAck is asserted.	RW	0x000
5:3	T_RTP_SHDW	Shadow field for T_RTP. This field is loaded into EMIF_SDRAM_TIMING_2[5:3] T_RTP field when SIdleAck is asserted.	RW	0x0
2:0	T_CKE_SHDW	Shadow field for T_CKE. This field is loaded into EMIF_SDRAM_TIMING_2[2:0] T_CKE field when SIdleAck is asserted.	RW	0x0

Table 15-161. Register Call Summary for Register EMIF_SDRAM_TIMING_2_SHADOW

EMIF Controller

- Subsequence - EMIF Timing Initialization: [0]
- EMIF Register Summary: [1]

Table 15-162. EMIF_SDRAM_TIMING_3

Address Offset	0x0000 0028		
Physical Address	0x4C00 0028 0x4D00 0028	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 3 Register. If this register is byte written, care must be taken that all the fields are written before performing any accesses to the SDRAM.		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
T_PDLL_UL	T_CSTA	T_CKESR	ZQ_ZQCS	T_TDQSCKMAX	T_RFC		T_RAS_MAX

Bits	Field Name	Description	Type	Reset
31:28	T_PDLL_UL	Minimum number of DDR clock cycles for PHY DLL to unlock. A value of N will be equal to N x 128 clocks.	RW	0x0
27:24	T_CSTA	Minimum number of DDR clock cycles between write-to-write or read-to-read data phases to different chip selects, minus one.	RW	0x0
23:21	T_CKESR	Minimum number of DDR clock cycles for which SDRAM must remain in Self Refresh, minus one.	RW	0x0
20:15	ZQ_ZQCS	Number of DDR clock cycles for a ZQCS command, minus one.	RW	0x00
14:13	T_TDQSCKMAX	Number of DDR clock that satisfies tDQSCKmax for LPDDR2, minus one.	RW	0x0
12:4	T_RFC	Minimum number of DDR clock cycles from Refresh or Load Mode to Refresh or Activate, minus one.	RW	0x000
3:0	T_RAS_MAX	Maximum number of REFRESH_RATE intervals from Activate to Precharge command. This field must be equal to ((tRASmax / tREFI)-1) rounded down to the next lower integer. Value for T_RAS_MAX can be calculated as follows: If tRASmax = 120 us and tREFI = 15.7 us, then T_RAS_MAX = ((120/15.7)-1) = 6.64. Round down to the next lower integer. Therefore, the programmed value must be 6.	RW	0x0

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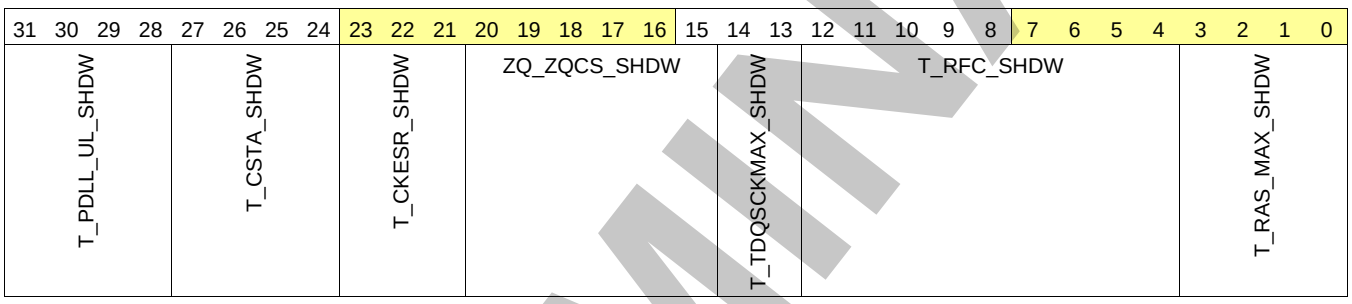
Table 15-163. Register Call Summary for Register EMIF_SDRAM_TIMING_3

EMIF Controller

- SDRAM Refresh Scheduling: [0]
- Turnaround Time: [1] [2]
- Output Impedance Calibration: [3] [4] [5]
- Subsequence - EMIF Timing Initialization: [6] [7] [8] [9] [10] [11]
- EMIF Register Summary: [12]
- EMIF Register Description: [13] [14] [15] [16] [17] [18] [19] [20] [21]

Table 15-164. EMIF_SDRAM_TIMING_3_SHADOW

Address Offset	0x0000 002C		
Physical Address	0x4C00 002C 0x4D00 002C	**Instance**	EMIF1 EMIF2
Description	SDRAM Timing 3 Shadow Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:28	T_PDLL_UL_SHDW	Shadow field for T_PDLL_UL. This field is loaded into T_PDLL_UL field in EMIF_SDRAM_TIMING_3 register when SIdleAck is asserted.	RW	0x0
27:24	T_CSTA_SHDW	Shadow field for T_CSTA. This field is loaded into T_CSTA field in EMIF_SDRAM_TIMING_3 register when SIdleAck is asserted.	RW	0x0
23:21	T_CKESR_SHDW	Shadow field for T_CKESR. This field is loaded into T_CKESR field in EMIF_SDRAM_TIMING_3 register when SIdleAck is asserted.	RW	0x0
20:15	ZQ_ZQCS_SHDW	Shadow field for ZQ_ZQCS. This field is loaded into ZQ_ZQCS field in EMIF_SDRAM_TIMING_3 register when SIdleAck is asserted.	RW	0x00
14:13	T_TDQSCKMAX_SHDW	Shadow field for T_TDQSCKMAX. This field is loaded into EMIF_SDRAM_TIMING_3[14:13] T_TDQSCKMAX field when SIdleAck is asserted.	RW	0x0
12:4	T_RFC_SHDW	Shadow field for T_RFC. This field is loaded into EMIF_SDRAM_TIMING_3[12:4] T_RFC when SIdleAck is asserted.	RW	0x000
3:0	T_RAS_MAX_SHDW	Shadow field for T_RAS_MAX. This field is loaded into EMIF_SDRAM_TIMING_3[3:0] T_RAS_MAX field when SIdleAck is asserted.	RW	0x0

Table 15-165. Register Call Summary for Register EMIF_SDRAM_TIMING_3_SHADOW

EMIF Controller

- Subsequence - EMIF Timing Initialization: [0]
- EMIF Register Summary: [1]

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Table 15-166. EMIF_POWER_MANAGEMENT_CONTROL

Address Offset	0x0000 0038		
Physical Address	0x4C00 0038 0x4D00 0038	**Instance**	EMIF1 EMIF2
Description	Power Management Control Register. Updating the *_TIM fields must be followed by at least one access to SDRAM for the new value to take an effect.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PD_TIM				DPD_EN	LP_MODE			SR_TIM				RESERVED			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PD_TIM	Power Management timer for Power-Down. The EMIF will put the external SDRAM in Power-Down mode after the EMIF is idle for these number of DDR clock cycles and if LP_MODE field is set to 4. Set to 0 to immediately enter Power-Down mode. Set to 1 for 16 clocks, set to 2 for 32 clocks, set to 3 for 64 clocks, set to 4 for 128 clocks, set to 5 for 256 clocks, set to 6 for 512 clocks, set to 7 for 1024 clocks, set to 8 for 2048 clocks, set to 9 for 4096 clocks, set to 10 for 8192 clocks, set to 11 for 16384 clocks, set to 12 for 32768 clocks, set to 13 for 65536 clocks, set to 14 for 131072 clocks, and set to 15 for 262144 clocks.	RW	0x0
11	DPD_EN	Deep Power Down enable. Set to 0 for normal operation. Set to 1 to enter deep power-down mode. This mode will override the LP_MODE field setting.	RW	0
10:8	LP_MODE	Automatic Power Management enable. Set to 1 for Clock Stop (reserved for the not supported LPDDR1 memories), set to 2 for Self Refresh mode, and set to 4 for Power-Down mode. All other values will disable automatic power management.	RW	0x0
7:4	SR_TIM	Power Management timer for Self Refresh. The EMIF will put the external SDRAM in Self Refresh mode after the EMIF is idle for these number of DDR clock cycles and if LP_MODE field is set to 2. Set to 0 to immediately enter Self Refresh mode. Set to 1 for 16 clocks, set to 2 for 32 clocks, set to 3 for 64 clocks, set to 4 for 128 clocks, set to 5 for 256 clocks, set to 6 for 512 clocks, set to 7 for 1024 clocks, set to 8 for 2048 clocks, set to 9 for 4096 clocks, set to 10 for 8192 clocks, set to 11 for 16384 clocks, set to 12 for 32768 clocks, set to 13 for 65536 clocks, set to 14 for 131072 clocks, and set to 15 for 262144 clocks.	RW	0x0
3:0	RESERVED		RW	0x0

Table 15-167. Register Call Summary for Register EMIF_POWER_MANAGEMENT_CONTROL

EMIF Controller

- Reset: [0]
- Power-Down Mode: [1] [2] [3]
- LPDDR2 Deep Power-Down Mode: [4] [5] [6] [7] [8]
- Self-Refresh Mode: [9] [10] [11]
- EMIF SDRAM Self-Refresh: [12] [13] [14] [15] [16]
- EMIF LPDDR2 Power-Down Mode: [17] [18] [19] [20] [21]
- EMIF LPDDR2-SDRAM Deep Power-Down Mode: [22] [23] [24] [25] [26]
- EMIF Register Summary: [27]
- EMIF Register Description: [28] [29]

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Table 15-168. EMIF_POWER_MANAGEMENT_CONTROL_SHADOW

Address Offset	0x0000 003C		
Physical Address	0x4C00 003C 0x4D00 003C	**Instance**	EMIF1 EMIF2
Description	Power Management Control Shadow Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PD_TIM_SHDW				RESERVED				SR_TIM_SHDW				RESERVED			

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:12	PD_TIM_SHDW	Shadow field for PD_TIM. This field is loaded into PD_TIM field in EMIF_POWER_MANAGEMENT_CONTROL register when SIdleAck is asserted.	RW	0x0
11:8	RESERVED		R	0x0
7:4	SR_TIM_SHDW	Shadow field for SR_TIM. This field is loaded into SR_TIM field in EMIF_POWER_MANAGEMENT_CONTROL register when SIdleAck is asserted.	RW	0x0
3:0	RESERVED		RW	0x0

Table 15-169. Register Call Summary for Register EMIF_POWER_MANAGEMENT_CONTROL_SHADOW

EMIF Controller

- EMIF SDRAM Self-Refresh: [0] [1]
- EMIF LPDDR2 Power-Down Mode: [2] [3]
- EMIF LPDDR2-SDRAM Deep Power-Down Mode: [4] [5]
- EMIF Register Summary: [6]

Table 15-170. EMIF_LPDDR2_MODE_REG_DATA

Address Offset	0x0000 0040		
Physical Address	0x4C00 0040 0x4D00 0040	**Instance**	EMIF1 EMIF2
Description	LPDDR2 Mode Reg Data Register A write to this register will cause a Mode Register write command to be sent to the LPDDR2 device with write data as specified in the VALUE_0 field. The address and chip select are taken from the EMIF_LPDDR2_MODE_REG_CONFIG register. A read to this register will cause a Mode Register read command to be sent to the LPDDR2 device. The address and chip select are taken from the EMIF_LPDDR2_MODE_REG_CONFIG register. The read data will appear in VALUE_0 field.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VALUE_0							

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000
6:0	VALUE_0	Mode register value.	RW	0x00

Table 15-171. Register Call Summary for Register EMIF_LPDDR2_MODE_REG_DATA

EMIF Controller

- EMIF MR Read: [0]
- EMIF MR Write: [1]
- EMIF Register Summary: [2]
- EMIF Register Description: [3]

Table 15-172. EMIF_LPDDR2_MODE_REG_CONFIG

Address Offset	0x0000 0050		
Physical Address	0x4C00 0050 0x4D00 0050	**Instance**	EMIF1 EMIF2
Description	LPDDR2 Mode Reg Config Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS	REFRESH_EN	RESERVED																						ADDRESS							

Bits	Field Name	Description	Type	Reset
31	CS	Chip select to issue mode register command. Set to 0 for CS0 and set to 1 for CS1.	RW	0
30	REFRESH_EN	Refresh Enable after MRW write. If a EMIF_LPDDR2_MODE_REG_DATA register write occurs with this bit set to 1, the refresh operations will commence.	RW	0
29:8	RESERVED	Reserved	R	0x00 0000
7:0	ADDRESS	Mode register address.	RW	0x00

Table 15-173. Register Call Summary for Register EMIF_LPDDR2_MODE_REG_CONFIG

EMIF Controller

- Reset: [0]
- LPDDR2 SDRAM Initialization: [1] [2]
- EMIF MR Read: [3] [4]
- EMIF MR Write: [5] [6]
- EMIF Register Summary: [7]
- EMIF Register Description: [8] [9]

Table 15-174. EMIF_OCP_CONFIG

Address Offset	0x0000 0054		
Physical Address	0x4C00 0054 0x4D00 0054	**Instance**	EMIF1 EMIF2
Description	OCP Config Register		
Type	RW		

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31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	SYS_THRESH_MAX	MPU_THRESH_MAX	LL_THRESH_MAX	RESERVED	

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	SYS_THRESH_MAX	System OCP Threshold Maximum. The number of commands the system interface can consume in the command FIFO. The value is used to determine when to stop future request, writing a zero will reserve no space for the associated interface. In the event the value is set to zero and a request is seen for that interface, the command FIFO will assume a value of 1. Since the low-latency interface has effectively a higher priority, the only way for the system interface to use all command FIFO entries is to set the LL_THRESH_MAX to zero.	RW	0x7
23:20	MPU_THRESH_MAX	MPU Threshold Maximum. The number of commands the MPU interface can consume in the command FIFO. The value is used to determine when to stop future request, writing a zero will reserve no space for the associated interface. In the event the value is set to zero and a request is seen for that interface, the command FIFO will assume a value of 1. Since the low-latency interface has effectively a higher priority, the only way for the MPU interface to use all command FIFO entries is to set the LL_THRESH_MAX to zero.	RW	0x7
19:16	LL_THRESH_MAX	Low-latency OCP Threshold Maximum. The number of commands the low latency interface can consume in the command FIFO. The value is used to determine when to stop future request, writing a zero will reserve no space for the associated interface. In the event the value is set to zero and a request is seen for that interface, the command FIFO will assume a value of 1.	RW	0x7
15:0	RESERVED		R	0x0000

Table 15-175. Register Call Summary for Register EMIF_OCP_CONFIG

EMIF Controller

- FIFO Description: [0] [1] [2] [3] [4] [5] [6] [7]
- EMIF Module Global Initialization: [8]
- EMIF Register Summary: [9]

Table 15-176. EMIF_OCP_CONFIG_VALUE_1

Address Offset	0x0000 0058		
Physical Address	0x4C00 0058 0x4D00 0058	**Instance**	EMIF1 EMIF2
Description	OCP Config Value 1 Register		
Type	R		

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31 30	29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
SYS_BUS_WIDTH	LL_BUS_WIDTH	RESERVED		WR_FIFO_DEPTH	CMD_FIFO_DEPTH

Bits	Field Name	Description	Type	Reset
31:30	SYS_BUS_WIDTH	System OCP data bus width 0 = 32-bit wide, 1 = 64-bit wide, 2 = 128-bit wide, 3 = Reserved	R	0x2
29:28	LL_BUS_WIDTH	Low-latency OCP data bus width 0 = 32-bit wide, 1 = 64-bit wide, 2 = 128-bit wide, 3 = Reserved	R	0x1
27:16	RESERVED	Reserved for future use.	R	0x000
15:8	WR_FIFO_DEPTH	Write Data FIFO depth	R	0x19
7:0	CMD_FIFO_DEPTH	Command FIFO depth	R	0x0A

Table 15-177. Register Call Summary for Register EMIF_OCP_CONFIG_VALUE_1

EMIF Controller

- EMIF Register Summary: [0]

Table 15-178. EMIF_OCP_CONFIG_VALUE_2

Address Offset	0x0000 005C		
Physical Address	0x4C00 005C 0x4D00 005C	**Instance**	EMIF1 EMIF2
Description	OCP Config Value 2 Register		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	RREG_FIFO_DEPTH	RSD_FIFO_DEPTH	RCMD_FIFO_DEPTH

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:16	RREG_FIFO_DEPTH	Register Read Data FIFO depth	R	0x04
15:8	RSD_FIFO_DEPTH	SDRAM Read Data FIFO depth	R	0x27
7:0	RCMD_FIFO_DEPTH	Read Command FIFO depth	R	0x27

Table 15-179. Register Call Summary for Register EMIF_OCP_CONFIG_VALUE_2

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-180. EMIF_PERFORMANCE_COUNTER_1

Address Offset	0x0000 0080		
Physical Address	0x4C00 0080 0x4D00 0080	**Instance**	EMIF1 EMIF2
Description	Performance Counter 1 Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER1																															

Bits	Field Name	Description	Type	Reset
31:0	COUNTER1	32-bit counter that can be configured as specified in the EMIF_PERFORMANCE_COUNTER_CONFIG register and EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT register.	R	0x0000 0000

Table 15-181. Register Call Summary for Register EMIF_PERFORMANCE_COUNTER_1

EMIF Controller

- Performance Counters: [0]
- EMIF Register Summary: [1]
- EMIF Register Description: [2] [3] [4] [5] [6]

Table 15-182. EMIF_PERFORMANCE_COUNTER_2

Address Offset	0x0000 0084		
Physical Address	0x4C00 0084 0x4D00 0084	**Instance**	EMIF1 EMIF2
Description	Performance Counter 2 Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER2																															

Bits	Field Name	Description	Type	Reset
31:0	COUNTER2	32-bit counter that can be configured as specified in the EMIF_PERFORMANCE_COUNTER_CONFIG register and EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT register.	R	0x0000 0000

Table 15-183. Register Call Summary for Register EMIF_PERFORMANCE_COUNTER_2

EMIF Controller

- Performance Counters: [0]
- EMIF Register Summary: [1]
- EMIF Register Description: [2] [3] [4] [5] [6]

Table 15-184. EMIF_PERFORMANCE_COUNTER_CONFIG

Address Offset	0x0000 0088		
Physical Address	0x4C00 0088 0x4D00 0088	**Instance**	EMIF1 EMIF2
Description	Performance Counter Config Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTR2_MCONNID_EN	CNTR2_REGION_EN	RESERVED										CNTR2_CFG				CNTR1_MCONNID_EN	CNTR1_REGION_EN	RESERVED										CNTR1_CFG			

Bits	Field Name	Description	Type	Reset
31	CNTR2_MCONNID_EN	MConnID filter enable for EMIF_PERFORMANCE_COUNTER_2 register.	RW	0
30	CNTR2_REGION_EN	Chip Select filter enable for EMIF_PERFORMANCE_COUNTER_2 register.	RW	0
29:20	RESERVED	Reserved for future use	R	0x000
19:16	CNTR2_CFG	Filter configuration for EMIF_PERFORMANCE_COUNTER_2. Refer to Table 15-123 for details.	RW	0x1
15	CNTR1_MCONNID_EN	MConnID filter enable for EMIF_PERFORMANCE_COUNTER_1 register.	RW	0
14	CNTR1_REGION_EN	Chip Select filter enable for EMIF_PERFORMANCE_COUNTER_1 register.	RW	0
13:4	RESERVED	Reserved for future use	R	0x000
3:0	CNTR1_CFG	Filter configuration for EMIF_PERFORMANCE_COUNTER_1. Refer to Table 15-123 for details.	RW	0x0

Table 15-185. Register Call Summary for Register EMIF_PERFORMANCE_COUNTER_CONFIG

EMIF Controller

- Performance Counters: [0] [1] [2] [3] [4]
- PERF_COUNTER_1 General Example for Counting Write Accesses: [5] [6]
- PERF_COUNTER_2 General Example for Counting Total Access: [7] [8] [9]
- PERF_COUNTER_3 General Example for Counting all Read Accesses: [10] [11] [12]
- EMIF Module Global Initialization: [13]
- EMIF Register Summary: [14]
- EMIF Register Description: [15] [16]

Table 15-186. EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT

Address Offset	0x0000 008C		
Physical Address	0x4C00 008C 0x4D00 008C	**Instance**	EMIF1 EMIF2
Description	Performance Counter Master Region Select Register The values programmed into the MCONNIDx fields are those in Table *ConnID Mapping (Debug View)*, in , *On-Chip Debug Support*, left-shifted by 2 bits. For example, to monitor accesses from the IPU subsystem (ConnID = 0x11), the value 0x44 is programmed into the MCONNIDx field.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCONNID2								RESERVED						REGION_SEL2		MCONNID1								RESERVED						REGION_SEL1	

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Bits	Field Name	Description	Type	Reset
31:24	MCONNID2	MConnID for EMIF_PERFORMANCE_COUNTER_2 register.	RW	0x00
23:18	RESERVED	Reserved	R	0x00
17:16	REGION_SEL2	MAddrSpace for EMIF_PERFORMANCE_COUNTER_2 register.	RW	0x0
15:8	MCONNID1	MConnID for EMIF_PERFORMANCE_COUNTER_1 register.	RW	0x00
7:2	RESERVED	Reserved	R	0x00
1:0	REGION_SEL1	MAddrSpace for EMIF_PERFORMANCE_COUNTER_1 register.	RW	0x0

Table 15-187. Register Call Summary for Register EMIF_PERFORMANCE_COUNTER_MASTER_REGION_SELECT

EMIF Controller

- Performance Counters: [0]
- PERF_COUNTER_1 General Example for Counting Write Accesses: [1]
- PERF_COUNTER_3 General Example for Counting all Read Accesses: [2] [3]
- EMIF Module Global Initialization: [4]
- EMIF Register Summary: [5]
- EMIF Register Description: [6] [7]

Table 15-188. EMIF_PERFORMANCE_COUNTER_TIME

Address Offset	0x0000 0090		
Physical Address	0x4C00 0090 0x4D00 0090	**Instance**	EMIF1 EMIF2
Description	Performance Counter Time Register. This is a free running counter.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOTAL_TIME																															

Bits	Field Name	Description	Type	Reset
31:0	TOTAL_TIME	32-bit counter that continuously counts number for EMIF_COREi clock cycles elapsed after EMIF is brought out of reset.	R	0x0000 0000

Table 15-189. Register Call Summary for Register EMIF_PERFORMANCE_COUNTER_TIME

EMIF Controller

- EMIF Register Summary: [0]

Table 15-190. EMIF_MISC_REG

Address Offset	0x0000 0094		
Physical Address	0x4C00 0094 0x4D00 0094	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DLL_CALIB_OS

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0
0	DLL_CALIB_OS	Phy_dll_calib one shot : Setting bit to 1 generates a phy_pll_calib pulse. Bit is self cleared when pll_calib gets generated and ack_wait has been satisfied. Software can poll to confirm completion. Uses the EMIF_DLL_CALIB_CTRL[19:16] ACK_WAIT bit field for time to wait after firing off the phy_dll_calib.	RW	0x0

Table 15-191. Register Call Summary for Register EMIF_MISC_REG

EMIF Controller

- PHY DLL Calibration: [0]
- EMIF Register Summary: [1]
- EMIF Register Description: [2]

Table 15-192. EMIF_DLL_CALIB_CTRL

Address Offset	0x0000 0098		
Physical Address	0x4C00 0098 0x4D00 0098	**Instance**	EMIF1 EMIF2
Description	Control register to force idle window time to generate a phy_dll_calib that can be used for updating PHY DLLs during voltage ramps. NOTE: Should always be loaded via the shadow register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ACK_WAIT				RESERVED								DLL_CALIB_INTERVAL							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:16	ACK_WAIT	The ack_wait determines the required wait time after a phy_dll_calib is generated before another command can be sent. Value program is in terms of EMIF_COREi cycle count. **CAUTION:** 5 must be the minimum value ever programmed.	RW	0x9
15:9	RESERVED		R	0x00
8:0	DLL_CALIB_INTERVAL	This field determines the interval between phy_dll_calib generation. This value is multiplied by a precounter of 16 EMIF_COREi cycles. Program this field one less the value you are targeting; program 1 to achieve interval of 2 (minimum interval supported). Programming zero turns off function. Note the final intervals between dll_calib generation is also a function of ACK_WAIT. Final periodic interval is calculated by: ((DLL_CALIB_INTERVAL + 1) × 16) + ACK_WAIT	RW	0x000

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Table 15-193. Register Call Summary for Register EMIF_DLL_CALIB_CTRL

EMIF Controller

- PHY DLL Calibration: [0]
- Subsequence - EMIF Timing Initialization: [1] [2] [3] [4]
- EMIF Register Summary: [5]
- EMIF Register Description: [6] [7] [8]

Table 15-194. EMIF_DLL_CALIB_CTRL_SHADOW

Address Offset	0x0000 009C		
Physical Address	0x4C00 009C 0x4D00 009C	**Instance**	EMIF1 EMIF2
Description	Read Idle Control Shadow Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ACK_WAIT_SHDW				RESERVED								DLL_CALIB_INTERVAL_SHDW							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:16	ACK_WAIT_SHDW	Shadow field for ACK_WAIT. This field is loaded into ACK_WAIT field in EMIF_DLL_CALIB_CTRL register when SIdleAck is asserted	RW	0x9
15:9	RESERVED		R	0x00
8:0	DLL_CALIB_INTERVAL_SHDW	Shadow field for DLL_CALIB_INTERVAL. This field is loaded into DLL_CALIB_INTERVAL field in the EMIF_DLL_CALIB_CTRL register when SIdleAck is asserted	RW	0x000

Table 15-195. Register Call Summary for Register EMIF_DLL_CALIB_CTRL_SHADOW

EMIF Controller

- Subsequence - EMIF Timing Initialization: [0]
- EMIF Register Summary: [1]

Table 15-196. EMIF_SYSTEM_OCP_INTERRUPT_RAW_STATUS

Address Offset	0x0000 00A4		
Physical Address	0x4C00 00A4 0x4D00 00A4	**Instance**	EMIF1 EMIF2
Description	System OCP Interrupt Raw Status Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													DNV_SYS	TA_SYS	ERR_SYS

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	DNV_SYS	Raw status of system OCP interrupt for LPDDR2 NVM data not valid. Write 1 to set the (raw) status, typically for debug. Writing 0 has no effect.	RW	0
1	TA_SYS	Raw status of system OCP interrupt for SDRAM temperature alert. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.	RW	0
0	ERR_SYS	Raw status of system OCP interrupt for command or address error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.	RW	0

Table 15-197. Register Call Summary for Register EMIF_SYSTEM_OCP_INTERRUPT_RAW_STATUS

EMIF Controller

- Interrupt Requests: [0] [2] [3]
- EMIF Register Summary: [4]

Table 15-198. EMIF_LOW_LATENCY_OCP_INTERRUPT_RAW_STATUS

Address Offset	0x0000 00A8		
Physical Address	0x4C00 00A8 0x4D00 00A8	**Instance**	EMIF1 EMIF2
Description	Low-Latency OCP Interrupt Raw Status Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													DNV_LL	TA_LL	ERR_LL

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	DNV_LL	Raw status of low-latency OCP interrupt for LPDDR2 NVM data not valid. Write 1 to set the (raw) status, typically for debug. Writing 0 has no effect.	RW	0
1	TA_LL	Raw status of low-latency OCP interrupt or SDRAM temperature alert. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.	RW	0
0	ERR_LL	Raw status of low-latency OCP interrupt for command or address error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.	RW	0

Table 15-199. Register Call Summary for Register EMIF_LOW_LATENCY_OCP_INTERRUPT_RAW_STATUS

EMIF Controller

- Interrupt Requests: [0]
- EMIF Register Summary: [4]

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Table 15-200. EMIF_SYSTEM_OCP_INTERRUPT_STATUS

Address Offset	0x0000 00AC		
Physical Address	0x4C00 00AC 0x4D00 00AC	**Instance**	EMIF1 EMIF2
Description	System OCP Interrupt Status Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													DNV_SYS	TA_SYS	ERR_SYS

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	DNV_SYS	Enabled status of system OCP interrupt for LPDDR2 NVM data not valid. Write 1 to clear the status after interrupt is serviced (raw status is cleared; that is, even if not enabled). Writing 0 has no effect.	RW	0
1	TA_SYS	Enabled status of system OCP interrupt for SDRAM temperature alert. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Writing a 0 has no effect.	RW	0
0	ERR_SYS	Enabled status of system OCP interrupt interrupt for command or address error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Writing a 0 has no effect.	RW	0

Table 15-201. Register Call Summary for Register EMIF_SYSTEM_OCP_INTERRUPT_STATUS

EMIF Controller

- Interrupt Requests: [1] [2]
- LPDDR2 Temperature Monitoring: [3]
- EMIF Module Global Initialization: [4]
- Interrupt Servicing: [5] [6] [7] [8] [9]
- EMIF Register Summary: [10]

Table 15-202. EMIF_LOW_LATENCY_OCP_INTERRUPT_STATUS

Address Offset	0x0000 00B0		
Physical Address	0x4C00 00B0 0x4D00 00B0	**Instance**	EMIF1 EMIF2
Description	Low-Latency OCP Interrupt Status Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													DNV_LL	TA_LL	ERR_LL

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	DNV_LL	Enabled status of low-latency OCP interrupt for LPDDR2 NVM data not valid. Write 1 to clear the status after interrupt is serviced (raw status is cleared; that is, even if not enabled). Writing 0 has no effect.	RW	0
1	TA_LL	Enabled status of low-latency OCP interrupt for SDRAM temperature alert. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Writing a 0 has no effect.	RW	0
0	ERR_LL	Enabled status of low-latency OCP interrupt for command or address error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled). Writing a 0 has no effect.	RW	0

Table 15-203. Register Call Summary for Register EMIF_LOW_LATENCY_OCP_INTERRUPT_STATUS

EMIF Controller

- Interrupt Requests:
- LPDDR2 Temperature Monitoring: [3]
- EMIF Module Global Initialization: [4]
- Interrupt Servicing:
- EMIF Register Summary: [10]

Table 15-204. EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_SET

Address Offset	0x0000 00B4		
Physical Address	0x4C00 00B4 0x4D00 00B4	**Instance**	EMIF1 EMIF2
Description	System OCP Interrupt Enable Set Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													EN_DNV_SYS	EN_TA_SYS	EN_ERR_SYS

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	EN_DNV_SYS	Enable set for system OCP interrupt for LPDDR2 NVM data not valid. Writing 1 enables the interrupt and sets this bit and the corresponding Interrupt-enable clear register. Writing 0 has no effect.	RW W1toSet	0
1	EN_TA_SYS	Enable set for system OCP interrupt for SDRAM temperature alert. . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
0	EN_ERR_SYS	Enable set for system OCP interrupt for command or address error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.	RW W1toSet	0

Table 15-205. Register Call Summary for Register EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_SET

EMIF Controller

- Interrupt Requests: [0] [1]
- EMIF Module Global Initialization: [2]
- LPDDR2 Temperature Monitoring Mode: [3]
- EMIF Register Summary: [4]

Table 15-206. EMIF_LOW_LATENCY_OCP_INTERRUPT_ENABLE_SET

Address Offset	0x0000 00B8		
Physical Address	0x4C00 00B8 0x4D00 00B8	**Instance**	EMIF1 EMIF2
Description	Low-Latency OCP Interrupt Enable Set Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													EN_DNV_LL	EN_TA_LL	EN_ERR_LL

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	EN_DNV_LL	Enable set for low-latency OCP interrupt for LPDDR2 NVM data not valid. Writing 1 enables the interrupt and sets this bit and the corresponding Interrupt-enable clear register. Writing a 0 has no effect.	RW W1toSet	0
1	EN_TA_LL	Enable set for low-latency OCP interrupt for SDRAM temperature alert. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.	RW W1toSet	0
0	EN_ERR_LL	Enable set for low-latency OCP interrupt for command or address error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.	RW W1toSet	0

Table 15-207. Register Call Summary for Register EMIF_LOW_LATENCY_OCP_INTERRUPT_ENABLE_SET

EMIF Controller

- Interrupt Requests:
- EMIF Module Global Initialization:
- LPDDR2 Temperature Monitoring Mode:
- EMIF Register Summary: [4]

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Table 15-208. EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_CLEAR

Address Offset	0x0000 00BC		
Physical Address	0x4C00 00BC 0x4D00 00BC	**Instance**	EMIF1 EMIF2
Description	System OCP Interrupt Enable Clear Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													EN_DNV_SYS	EN_TA_SYS	EN_ERR_SYS

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use	R	0x0000 0000
2	EN_DNV_SYS	Enable clear for system OCP interrupt for LPDDR2 NVM data not valid. Writing 1 disables the interrupt and clears this bit and the corresponding interrupt-enable set register. Writing 0 has no effect.	RW W1toClr	0
1	EN_TA_SYS	Enable clear for system OCP interrupt for SDRAM temperature alert. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.	RW W1toClr	0
0	EN_ERR_SYS	Enable clear for system OCP interrupt for command or address error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.	RW W1toClr	0

Table 15-209. Register Call Summary for Register EMIF_SYSTEM_OCP_INTERRUPT_ENABLE_CLEAR

EMIF Controller

- Interrupt Requests: [0] [1]
- Interrupt Servicing: [2]
- EMIF Register Summary: [3]

Table 15-210. EMIF_LOW_LATENCY_OCP_INTERRUPT_ENABLE_CLEAR

Address Offset	0x0000 00C0		
Physical Address	0x4C00 00C0 0x4D00 00C0	**Instance**	EMIF1 EMIF2
Description	Low-Latency OCP Interrupt Enable Clear Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													EN_DNV_LL	EN_TA_LL	EN_ERR_LL

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved for future use.	R	0x0000 0000
2	EN_DNV_LL	Enable clear for low-latency OCP interrupt for LPDDR2 NVM data not valid. Writing 1 disables the interrupt and clears this bit and the corresponding interrupt enable set register. Writing 0 has no effect.	RW W1toClr	0
1	EN_TA_LL	Enable clear for low-latency OCP interrupt for SDRAM temperature alert. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.	RW W1toClr	0
0	EN_ERR_LL	Enable clear for low-latency OCP interrupt for command or address error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.	RW W1toClr	0

Table 15-211. Register Call Summary for Register EMIF_LOW_LATENCY_OCP_INTERRUPT_ENABLE_CLEAR

EMIF Controller

- Interrupt Requests:
- Interrupt Servicing:
- EMIF Register Summary: [3]

Table 15-212. EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG

Address Offset	0x0000 00C8		
Physical Address	0x4C00 00C8 0x4D00 00C8	**Instance**	EMIF1 EMIF2
Description	SDRAM Output Impedance Calibration Config Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CS1EN	ZQ_CS0EN	ZQ_DUALCALEN	ZQ_SFEXITEN	ZQ_PDEXITEN	RESERVED							ZQ_ZQINIT_MULT		ZQ_ZQCL_MULT		ZQ_REFINTERVAL															

Bits	Field Name	Description	Type	Reset
31	ZQ_CS1EN	Writing a 1 enables ZQ calibration for CS1.	RW	0x0
30	ZQ_CS0EN	Writing a 1 enables ZQ calibration for CS0.	RW	0x0
29	ZQ_DUALCALEN	ZQ Dual Calibration enable. Allows both ranks to be ZQ calibrated simultaneously. Setting this bit requires both chip selects to have a separate calibration resistor per device.	RW	0x0
28	ZQ_SFEXITEN	Writing a 1 enables the issuing of ZQCL on Self-Refresh exit.	RW	0x0
27	ZQ_PDEXITEN	Writing a 1 enables the issuing of ZQCL on Active Power-Down, and Precharge Power-Down exit.	RW	0
26:20	RESERVED	Reserved	R	0x00
19:18	ZQ_ZQINIT_MULT	Indicates the number of ZQCL durations that make up a ZQINIT duration, minus one..	RW	0x0
17:16	ZQ_ZQCL_MULT	Indicates the number of ZQCS intervals that make up a ZQCL duration, minus one. ZQCS interval is defined by ZQ_ZQCS in EMIF_SDRAM_TIMING_3.	RW	0x0

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Bits	Field Name	Description	Type	Reset
15:0	ZQ_REFINTERVAL	Number of refresh periods between ZQCS commands. This field supports between one refresh period to 256 ms between ZQCS calibration commands. Refresh period is defined by refresh_rate in EMIF_SDRAM_REFRESH_CONTROL register.	RW	0x0000

Table 15-213. Register Call Summary for Register EMIF_SDRAM_OUTPUT_IMPEDANCE_CALIBRATION_CONFIG

EMIF Controller

- Output Impedance Calibration: [0] [1] [2] [3] [4] [5] [6] [7]
- EMIF Output Impedance Calibration Mode: [8] [9] [10] [11] [12] [13]
- EMIF Register Summary: [14]

Table 15-214. EMIF_TEMPERATURE_ALERT_CONFIG

Address Offset	0x0000 00CC		
Physical Address	0x4C00 00CC 0x4D00 00CC	**Instance**	EMIF1 EMIF2
Description	Temperature Alert Config Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TA_CS1EN		TA_CS0EN		RESERVED		TA_SFEXITEN		TA_DEVWDT			TA_DEVCNT			RESERVED																	
TA_REFINTERVAL																															

Bits	Field Name	Description	Type	Reset
31	TA_CS1EN	Writing a 1 enables temperature alert polling for CS1.	RW	0x0
30	TA_CS0EN	Writing a 1 enables temperature alert polling for CS0.	RW	0x0
29	RESERVED	Reserved	R	0x0
28	TA_SFEXITEN	Temperature Alert Poll on Self-Refresh, Active Power-Down, and Precharge Power-Down exit enable. Writing a 1 enables the issuing of a temperature alert poll on Self-Refresh exit.	RW	0x0
27:26	TA_DEVWDT	This field indicates how wide a physical device is. It is used in conjunction with the TA_DEVCNT field to determine which byte lanes contain the temperature alert info. A value of 0: 8-bit wide, 1: 16- bit wide, 2: 32-bit wide. All others are reserved. If this field is set to 1 and the TA_DEVCNT field is set to 1 the byte mask for checking will be 4'b0101.	RW	0x0
25:24	TA_DEVCNT	This field indicates which external byte lanes contain a device for temperature monitoring. A value of 0 = one device, 1 = two devices, 2 = four devices. All other reserved.	RW	0x0
23:22	RESERVED	Reserved	R	0x0
21:0	TA_REFINTERVAL	Number of refresh periods between temperature alert polls. This field supports between one refresh period to 10 seconds between temperature alert polls. Refresh period is defined by REFRESH_RATE in EMIF_SDRAM_REFRESH_CONTROL register.	RW	0x000000

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Table 15-215. Register Call Summary for Register EMIF_TEMPERATURE_ALERT_CONFIG

EMIF Controller

- LPDDR2 Temperature Monitoring: [0] [1] [2] [3] [4] [5]
- LPDDR2 Temperature Monitoring Mode: [6] [7] [8] [9] [10] [11]
- EMIF Register Summary: [12]

Table 15-216. EMIF_OCP_ERROR_LOG

Address Offset	0x0000 00D0		
Physical Address	0x4C00 00D0 0x4D00 00D0	**Instance**	EMIF1 EMIF2
Description	OCP Error Log Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MADDRSPACE		MBURSTSEQ			MCMD			MCONNID							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved for future use.	R	0x0000
15:14	MADDRSPACE	Address space of the first errored transaction. 0x0: SDRAM 0x1: Reserved for LPDDR2-NVM 0x2: Reserved 0x3: Internal registers	R	0x0
13:11	MBURSTSEQ	Addressing mode of the first errored transaction. (see Section 14.2.1, *L3_MAIN Interconnect* for more information)	R	0x0
10:8	MCMD	Command type of the first errored transaction. (see Section 14.2.1, *L3_MAIN Interconnect* for more information)	R	0x0
7:0	MCONNID	Connection ID of the first errored transaction.	R	0x00

Table 15-217. Register Call Summary for Register EMIF_OCP_ERROR_LOG

EMIF Controller

- Interrupt Servicing: [0]
- EMIF Register Summary: [2]

Table 15-218. EMIF_READ_WRITE_LEVELING_RAMP_WINDOW

Address Offset	0x0000 00D4		
Physical Address	0x4C00 00D4 0x4D00 00D4	**Instance**	EMIF1 EMIF2
Description	Read/write leveling ramp window register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RDWRLVLINC_RMP_WIN							

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x0 0000
12:0	RDWRLVLINC_RMP_WIN	Incremental leveling ramp window in number of refresh periods. The value programmed is minus one the required value. Refresh period is defined by REFRESH_RATE in EMIF_SDRAM_REFRESH_CONTROL register.	RW	0x0000

Table 15-219. Register Call Summary for Register EMIF_READ_WRITE_LEVELING_RAMP_WINDOW

EMIF Controller

- Incremental Leveling: [0] [1]
- EMIF Register Summary: [2]

Table 15-220. EMIF_READ_WRITE_LEVELING_RAMP_CONTROL

Address Offset	0x0000 00D8		
Physical Address	0x4C00 00D8 0x4D00 00D8	**Instance**	EMIF1 EMIF2
Description	Read/write leveling ramp control register		
Type	RW		

31	30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RDWRLVL_EN	RDWRLVLINC_RMP_PRE	RDLVLINC_RMP_INT	RDLVLGATEINC_RMP_INT	WRLVLINC_RMP_INT

Bits	Field Name	Description	Type	Reset
31	RDWRLVL_EN	Read-Write Leveling enable. Set 1 to enable leveling. Set 0 to disable leveling.	RW	0
30:24	RDWRLVLINC_RMP_PRE	Incremental leveling pre-scalar in number of refresh periods during ramp window. The value programmed is minus one the required value. Refresh period is defined by REFRESH_RATE in EMIF_SDRAM_REFRESH_CONTROL register.	RW	0x00
23:16	RDLVLINC_RMP_INT	Incremental read data eye training interval during ramp window. Number of RDWRLVLINC_RMP_PRE intervals between incremental read data eye training during ramp window. A value of 0 will disable incremental read data eye training.	RW	0x00
15:8	RDLVLGATEINC_RMP_INT	Incremental read DQS gate training interval during ramp window. Number of RDWRLVLINC_RMP_PRE intervals between incremental read DQS gate training during ramp window. A value of 0 will disable incremental read DQS gate training.	RW	0x00
7:0	WRLVLINC_RMP_INT	Incremental write leveling interval during ramp window. Number of RDWRLVLINC_RMP_PRE intervals between incremental write leveling during ramp window. A value of 0 will disable incremental write leveling.	RW	0x00

Table 15-221. Register Call Summary for Register EMIF_READ_WRITE_LEVELING_RAMP_CONTROL

EMIF Controller

- Incremental Leveling: [0] [1] [2]
- EMIF Register Summary: [3]

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Table 15-222. EMIF_READ_WRITE_LEVELING_CONTROL

Address Offset	0x0000 00DC		
Physical Address	0x4C00 00DC 0x4D00 00DC	**Instance**	EMIF1 EMIF2
Description	Read/write leveling control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDWRLVLFULL_START	RDWRLVLINC_PRE							RDLVLINC_INT								RDLVLGATEINC_INT								WRLVLINC_INT							

Bits	Field Name	Description	Type	Reset
31	RDWRLVLFULL_START	Full leveling trigger. Writing a 1 to this field triggers full read and write leveling. This bit will self clear to 0.	RW	0
30:24	RDWRLVLINC_PRE	Incremental leveling pre-scalar in number of refresh periods. The value programmed is minus one the required value. Refresh period is defined by REFRESH_RATE in EMIF_SDRAM_REFRESH_CONTROL register.	RW	0x00
23:16	RDLVLINC_INT	Incremental read data eye training interval. Number of RDWRLVLINC_PRE intervals between incremental read data eye training. A value of 0 will disable incremental read data eye training.	RW	0x00
15:8	RDLVLGATEINC_INT	Incremental read DQS gate training interval. Number of RDWRLVLINC_PRE intervals between incremental read DQS gate training. A value of 0 will disable incremental read DQS gate training.	RW	0x00
7:0	WRLVLINC_INT	Incremental write leveling interval. Number of RDWRLVLINC_PRE intervals between incremental write leveling. A value of 0 will disable incremental write leveling.	RW	0x00

Table 15-223. Register Call Summary for Register EMIF_READ_WRITE_LEVELING_CONTROL

EMIF Controller

- Full Leveling: [0]
- Incremental Leveling: [1] [2]
- EMIF Register Summary: [3]

Table 15-224. EMIF_DDR_PHY_CONTROL_1

Address Offset	0x0000 00E4		
Physical Address	0x4C00 00E4 0x4D00 00E4	**Instance**	EMIF1 EMIF2
Description	PHY control register 1		
Type	RW		

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31 30 29 28	27	26	25	24	23 22	21	20	19	18	17 16	15 14 13 12 11 10	9	8	7 6 5	4 3 2 1 0
RESERVED	RDLVL_MASK	RDLVLGATE_MASK	WRLVL_MASK	RESERVED		PHY_HALF_DELAYS	PHY_CLK_STALL_LEVEL	PHY_DIS_CALIB_RST	PHY_INVERT_CLKOUT	PHY_DLL_LOCK_DIFF		PHY_FAST_DLL_LOCK	RESERVED		READ_LATENCY

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	RW	0x0
27	RDLVL_MASK	Writing a 1 to this field will mask read data eye training during full leveling command, plus drives reg_phy_use_rd_data_eye_level control low to allow user to use programmed ratio values. Incremental training needs to be disabled using incremental training registers.	RW	0
26	RDLVLGATE_MASK	Writing a 1 to this field will mask dqs gate training during full leveling command, plus drives reg_phy_use_rd_dqs_level control low to allow user to use programmed ratio values. Incremental training needs to be disabled using incremental training registers.	RW	0
25	WRLVL_MASK	Writing a 1 to this field will mask write leveling training during full leveling command, plus drives reg_phy_use_wr_level control low to allow user to use programmed ratio values. Incremental training needs to be disabled using incremental training registers.	RW	0
24:22	RESERVED	Reserved	RW	0x0
21	PHY_HALF_DELAYS	Adjust slave delay line delays to support 2× mode 1: 2× mode (MDLL clock is half the rate of PHY) - OPP_NOM 0: 1× mode (MDLL clock rate is same as PHY) - OPP_BOOT	RW	0
20	PHY_CLK_STALL_LEVEL	Enable variable idle value for delay lines. Enable during normal operations to avoid differential aging in the delay lines.	RW	0
19	PHY_DIS_CALIB_RST	Disable the dll_calib (internally generated) signal from resetting the Read Capture FIFO pointers and portions of data PHYs. Debug only. Note: dll_calib is generated by 1. EMIF_MISC_REG[0] DLL_CALIB_OS set to 1,or 2. by the PHY when it detects that the clock frequency variation has exceeded the bounds set by PHY_DLL_LOCK_DIFF or 3. periodically throughout the leveling process.	RW	0
18	PHY_INVERT_CLKOUT	Inverts the polarity of DRAM clock. This bit must be set to 0 when in LDDDR2 mode. 0: core clock is passed on to DRAM 1: inverted core clock is passed on to DRAM	RW	0
17:10	PHY_DLL_LOCK_DIFF	The maximum number of delay line taps variation while maintaining the master DLL lock. When the PHY is in locked state and the variation on the clock exceeds the variation indicated by this field, the lock signal is de-asserted and a dll_calib signal is generated. To prevent the dll_calib signal from being asserted in the middle of traffic when the clock jitter exceeds the variation, this register needs to be set to a value which will ensure that the lock will not be lost. Recommended value is 16.	RW	0x02

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Bits	Field Name	Description	Type	Reset
9	PHY_FAST_DLL_LOCK	Controls master DLL to lock fast or average logic must be part of locking process. Set to 1 before OPP transition commences, and set back to 0 after OPP transition completes. 1: MDLL lock is asserted based on single sample 0: MDLL lock is asserted based on average of 16 samples.	RW	0
8:5	RESERVED	Reserved	RW	0x00
4:0	READ_LATENCY	This field defines the read latency for the read data from SDRAM in number of DDR clock cycles. This field is used by the EMIF as well as the PHY. READ_LATENCY = RL + reg_phy_rdc_we_to_re -1. EMIF uses above equation to calculate reg_phy_rdc_we_to_re and forward it to the PHY. For DDR3, the true RL is used, not the decoded value. See JEDEC spec. The write latency (WL) is tied to the RL for the LPDDR2. See the LPDDR2 SDRAM standard.	RW	0x01E

Table 15-225. Register Call Summary for Register EMIF_DDR_PHY_CONTROL_1

EMIF Controller

- LPDDR2 Read: [0]
- EMIF Module Global Initialization: [1] [2]
- EMIF Register Summary: [3]
- EMIF Register Description: [4] [5] [6]

Table 15-226. EMIF_DDR_PHY_CONTROL_1_SHADOW

Address Offset	0x0000 00E8		
Physical Address	0x4C00 00E8 0x4D00 00E8	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RDLVL_MASK_SHDW	RDLVLGATE_MASK_SHDW	WRLVL_MASK_SHDW	RESERVED			PHY_HALF_DELAYS_SHDW	PHY_CLK_STALL_LEVEL_SHDW	PHY_DIS_CALIB_RST_SHDW	PHY_INVERT_CLKOUT_SHDW	PHY_DLL_LOCK_DIFF_SHDW								PHY_FAST_DLL_SHDW	RESERVED					READ_LATENCY_SHDW					

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	RW	0x0
27	RDLVL_MASK_SHDW	Shadow field for RDLVL_MASK	RW	0
26	RDLVLGATE_MASK_SHDW	Shadow field for RDLVLGATE_MASK	RW	0
25	WRLVL_MASK_SHDW	Shadow field for WRLVL_MASK	RW	0
24:22	RESERVED	Reserved	RW	0x0
21	PHY_HALF_DELAYS_SHDW	Shadow field for PHY_HALF_DELAYS	RW	0
20	PHY_CLK_STALL_LEVEL_SHDW	Shadow field for PHY_CLK_STALL_LEVEL	RW	0

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Bits	Field Name	Description	Type	Reset
19	PHY_DIS_CALIB_RST_SHDW	Shadow field for PHY_DIS_CALIB_RST	RW	0
18	PHY_INVERT_CLKOUT_SHDW	Shadow field for PHY_INVERT_CLKOUT	RW	0
17:10	PHY_DLL_LOCK_DIFF_SHDW	Shadow field for PHY_DLL_LOCK_DIFF	RW	0x00
9	PHY_FAST_DLL_SHDW	Shadow field for PHY_FAST_DLL	RW	0
8:5	RESERVED	Reserved	RW	0x00
4:0	READ_LATENCY_SHDW	Shadow field for READ_LATENCY	RW	0x000

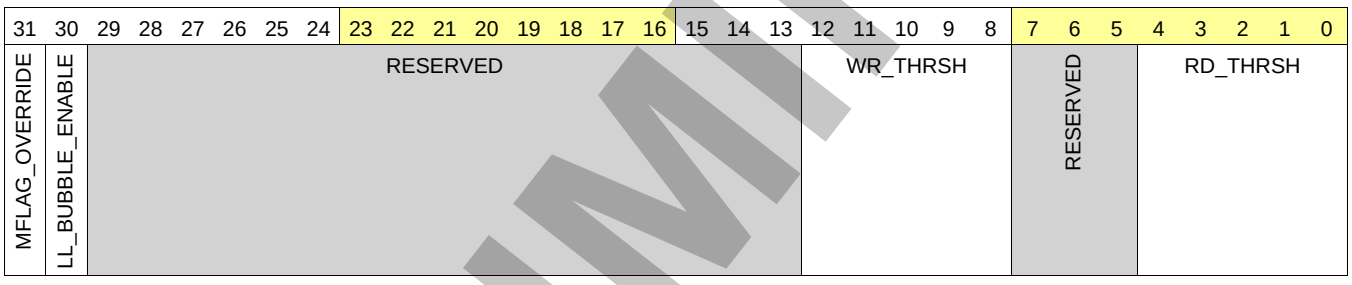
Table 15-227. Register Call Summary for Register EMIF_DDR_PHY_CONTROL_1_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-228. EMIF_READ_WRITE_EXECUTION_THRESHOLD

Address Offset	0x0000 0120		
Physical Address	0x4C00 0120 0x4D00 0120	**Instance**	EMIF1 EMIF2
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31	MFLAG_OVERRIDE	Mflag override. When set to 1, forces Mflag internally to be zero (compatibility mode). **NOTE**: MFLAG_OVERRIDE must be considered a static control.	RW	0
30	LL_BUBBLE_ENABLE	LL bubble enable. When set to 1, enables LL bubble function. Allows one access (one beat of burst), for any bank that is open. This gives performance improvement and avoids bank thrashing (in other words, have gone thru activation stage and should allow one access, even if higher priority LL port command comes thru)	RW	0
29:13	RESERVED	Reserved	R	0x0000
12:8	WR_THRSH	Write Threshold. Number of SDRAM write bursts after which the EMIF arbitration will switch to executing read commands. The value programmed is always minus one the required number	RW	0x03
7:5	RESERVED	Reserved	R	0x0
4:0	RD_THRSH	Read threshold. Number of SDRAM read bursts after which the EMIF arbitration will switch to executing write commands. The value that is programmed is always minus one the required number	R	0x05

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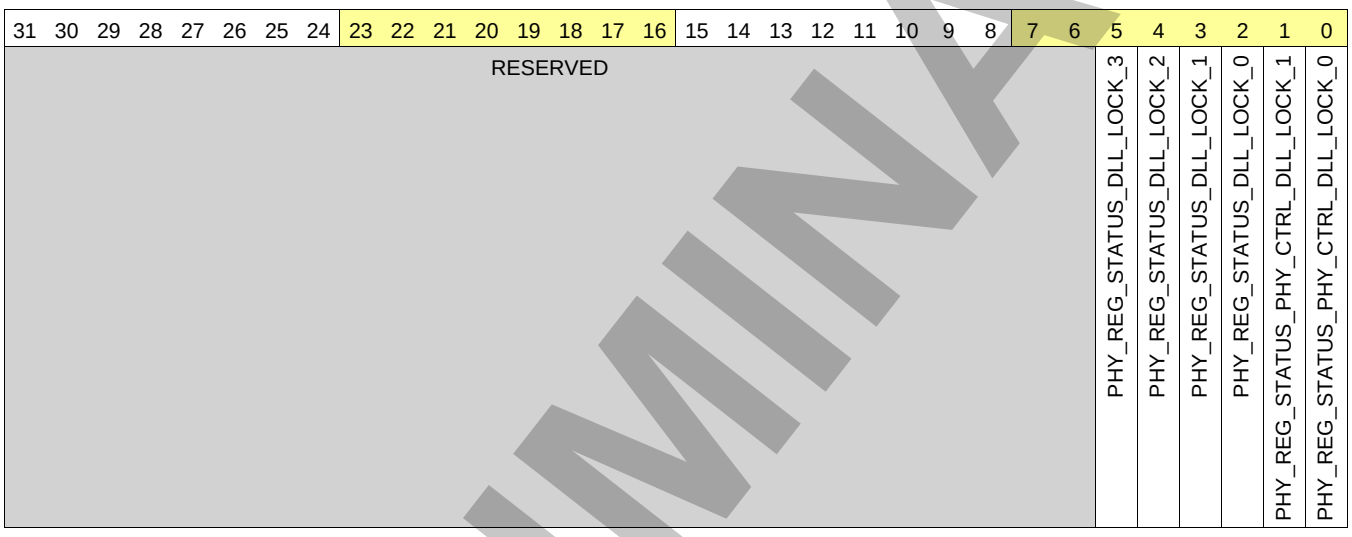
Table 15-229. Register Call Summary for Register EMIF_READ_WRITE_EXECUTION_THRESHOLD

EMIF Controller

- Port Priority: [0]
- EMIF Register Summary: [2]

Table 15-230. EMIF_PHY_STATUS_1

Address Offset	0x0000 0140		
Physical Address	0x4C00 0140 0x4D00 0140	**Instance**	EMIF1 EMIF2
Description			
Type	R		



Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x000 0000
5	PHY_REG_STATUS_DLL_LOCK_3	Reflects lock status of DLL of data PHY 3 1: Master DLL is locked 0: Master DLL is not locked	R	0
4	PHY_REG_STATUS_DLL_LOCK_2	Reflects lock status of DLL of data PHY 2 1: Master DLL is locked 0: Master DLL is not locked	R	0
3	PHY_REG_STATUS_DLL_LOCK_1	Reflects lock status of DLL of data PHY 1 1: Master DLL is locked 0: Master DLL is not locked	R	0
2	PHY_REG_STATUS_DLL_LOCK_0	Reflects lock status of DLL of data PHY 0 1: Master DLL is locked 0: Master DLL is not locked	R	0
1	PHY_REG_STATUS_PHY_CTRL_DLL_LOCK_1	Reflects lock status of DLL 1 (command PHY 2) 1: Master DLL is locked 0: Master DLL is not locked	R	0
0	PHY_REG_STATUS_PHY_CTRL_DLL_LOCK_0	Reflects lock status of DLL 0 (command PHY 0 and 1) 1: Master DLL is locked 0: Master DLL is not locked	R	0

Table 15-231. Register Call Summary for Register EMIF_PHY_STATUS_1

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-232. EMIF_PHY_STATUS_20

Address Offset	0x0000 018C		
Physical Address	0x4C00 018C 0x4D00 018C	**Instance**	EMIF1 EMIF2
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_REG_WRLVL_INC_FAIL_1	PHY_REG_WRLVL_INC_FAIL_0	PHY_REG_RDLVL_INC_FAIL_3	PHY_REG_RDLVL_INC_FAIL_2	PHY_REG_RDLVL_INC_FAIL_1	PHY_REG_RDLVL_INC_FAIL_0	PHY_REG_FIFO_WE_IN_MISALIGNED_STICKY_3	PHY_REG_FIFO_WE_IN_MISALIGNED_STICKY_2	PHY_REG_FIFO_WE_IN_MISALIGNED_STICKY_1	PHY_REG_FIFO_WE_IN_MISALIGNED_STICKY_0	PHY_REG_STATUS_PHY_CTRL_MDLL_UNLOCK_STICKY_1	PHY_REG_STATUS_PHY_CTRL_MDLL_UNLOCK_STICKY_0	PHY_REG_STATUS_MDLL_UNLOCK_STICKY_3	PHY_REG_STATUS_MDLL_UNLOCK_STICKY_2	PHY_REG_STATUS_MDLL_UNLOCK_STICKY_1	PHY_REG_STATUS_MDLL_UNLOCK_STICKY_0	PHY_REG_RDC_FIFO_RST_ERR_CNT_3				PHY_REG_RDC_FIFO_RST_ERR_CNT_2				PHY_REG_RDC_FIFO_RST_ERR_CNT_1				PHY_REG_RDC_FIFO_RST_ERR_CNT_0			

Bits	Field Name	Description	Type	Reset
31	PHY_REG_WRLVL_INC_FAIL_1	Incremental Write Leveling Fail Status Flag. Data PHY 1 1: Incremental read leveling test has failed. 0: Incremental read leveling test has passed.	R	0
30	PHY_REG_WRLVL_INC_FAIL_0	Incremental Write Leveling Fail Status Flag. Data PHY 0 1: Incremental read leveling test has failed. 0: Incremental read leveling test has passed.	R	0
29	PHY_REG_RDLVL_INC_FAIL_3	Incremental Read Leveling Fail Status Flag. Data PHY 3 1: Incremental read leveling test has failed. 0: Incremental read leveling test has passed.	R	0
28	PHY_REG_RDLVL_INC_FAIL_2	Incremental Read Leveling Fail Status Flag. Data PHY 2 1: Incremental read leveling test has failed. 0: Incremental read leveling test has passed.	R	0
27	PHY_REG_RDLVL_INC_FAIL_1	Incremental Read Leveling Fail Status Flag. Data PHY 1 1: Incremental read leveling test has failed. 0: Incremental read leveling test has passed.	R	0
26	PHY_REG_RDLVL_INC_FAIL_0	Incremental Read Leveling Fail Status Flag. Data PHY 0 1: Incremental read leveling test has failed. 0: Incremental read leveling test has passed.	R	0
25	PHY_REG_FIFO_WE_IN_MISALIGNED_STICKY_3	Data PHY 3 1: fifo_we_in rising edge doesn't fall in pre-amble phase of dqs_in. Error case. 0: fifo_we_in rising edge falls in pre-amble phase of dqs_in. No error.	R	0
24	PHY_REG_FIFO_WE_IN_MISALIGNED_STICKY_2	Data PHY 2 1: fifo_we_in rising edge doesn't fall in pre-amble phase of dqs_in. Error case. 0: fifo_we_in rising edge falls in pre-amble phase of dqs_in. No error.	R	0

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Bits	Field Name	Description	Type	Reset
23	PHY_REG_FIFO_WE_IN_MISALIGNED_STICKY_1	Data PHY 1 1: fifo_we_in rising edge doesn't fall in pre-amble phase of dqs_in. Error case. 0: fifo_we_in rising edge falls in pre-amble phase of dqs_in. No error.	R	0
22	PHY_REG_FIFO_WE_IN_MISALIGNED_STICKY_0	Data PHY 0 1: fifo_we_in rising edge doesn't fall in pre-amble phase of dqs_in. Error case. 0: fifo_we_in rising edge falls in pre-amble phase of dqs_in. No error.	R	0
21	PHY_REG_STATUS_PHY_CTRL_MDLL_UNLOCK_STICKY_1	Command DLL 1 (command PHY 2) 1: Master DLL has lost the lock 0: Master DLL never lost the lock	R	0
20	PHY_REG_STATUS_PHY_CTRL_MDLL_UNLOCK_STICKY_0	Command DLL 0 (command PHYs 0 and 1) 1: Master DLL has lost the lock 0: Master DLL never lost the lock	R	0
19	PHY_REG_STATUS_MDLL_UNLOCK_STICKY_3	Data PHY 3 1: Master DLL has lost the lock 0: Master DLL never lost the lock	R	0
18	PHY_REG_STATUS_MDLL_UNLOCK_STICKY_2	Data PHY 2 1: Master DLL has lost the lock 0: Master DLL never lost the lock	R	0
17	PHY_REG_STATUS_MDLL_UNLOCK_STICKY_1	Data PHY 1 1: Master DLL has lost the lock 0: Master DLL never lost the lock	R	0
16	PHY_REG_STATUS_MDLL_UNLOCK_STICKY_0	Data PHY 0 1: Master DLL has lost the lock 0: Master DLL never lost the lock	R	0
15:12	PHY_REG_RDC_FIFO_RST_ERR_CNT_3	Counter for counting the number of times the pointers of read capture FIFO differ when they are reset by dll_calib. Data PHY 3	R	0x0
11:8	PHY_REG_RDC_FIFO_RST_ERR_CNT_2	Counter for counting the number of times the pointers of read capture FIFO differ when they are reset by dll_calib. Data PHY 2	R	0x0
7:4	PHY_REG_RDC_FIFO_RST_ERR_CNT_1	Counter for counting the number of times the pointers of read capture FIFO differ when they are reset by dll_calib. Data PHY 1	R	0x0
3:0	PHY_REG_RDC_FIFO_RST_ERR_CNT_0	Counter for counting the number of times the pointers of read capture FIFO differ when they are reset by dll_calib. Data PHY 0	R	0x0

Table 15-233. Register Call Summary for Register EMIF_PHY_STATUS_20

EMIF Controller

- EMIF Register Summary: [0]
- EMIF Register Description: [1] [2] [3]

Table 15-234. EMIF_PHY_STATUS_21

Address Offset	0x0000 0190		
Physical Address	0x4C00 0190 0x4D00 0190	**Instance**	EMIF1 EMIF2
Description			
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PHY_REG_GATELVL_INC_FAIL_3	PHY_REG_GATELVL_INC_FAIL_2	PHY_REG_GATELVL_INC_FAIL_1	PHY_REG_GATELVL_INC_FAIL_0	PHY_REG_WRLVL_INC_FAIL_3	PHY_REG_WRLVL_INC_FAIL_2				

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x000 0000
5	PHY_REG_GATELVL_INC_FAIL_3	Incremental Gate Leveling Fail Status Flag. Data PHY 3 1: Incremental gate leveling test has failed. 0: Incremental gate leveling test has passed.	R	0
4	PHY_REG_GATELVL_INC_FAIL_2	Incremental Gate Leveling Fail Status Flag. Data PHY 2 1: Incremental gate leveling test has failed. 0: Incremental gate leveling test has passed.	R	0
3	PHY_REG_GATELVL_INC_FAIL_1	Incremental Gate Leveling Fail Status Flag. Data PHY 1 1: Incremental gate leveling test has failed. 0: Incremental gate leveling test has passed.	R	0
2	PHY_REG_GATELVL_INC_FAIL_0	Incremental Gate Leveling Fail Status Flag. Data PHY 0 1: Incremental gate leveling test has failed. 0: Incremental gate leveling test has passed.	R	0
1	PHY_REG_WRLVL_INC_FAIL_3	Incremental Write Leveling Fail Status Flag. Data PHY 3 1: Incremental read leveling test has failed. 0: Incremental read leveling test has passed.	R	0
0	PHY_REG_WRLVL_INC_FAIL_2	Incremental Write Leveling Fail Status Flag. Data PHY 2 1: Incremental read leveling test has failed. 0: Incremental read leveling test has passed.	R	0

Table 15-235. Register Call Summary for Register EMIF_PHY_STATUS_21

EMIF Controller

- EMIF Register Summary: [0]

Table 15-236. EMIF_EXT_PHY_CONTROL_1

Address Offset	0x0000 0200		
Physical Address	0x4C00 0200 0x4D00 0200	**Instance**	EMIF1 EMIF2
Description	Programs command PHY slave DLL ratio. Ratio value for address/command launch timing in command PHYs. 0x80: 50% (180°), 0x40: 25% (90°)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_CTRL_SLAVE_RATIO_2								PHY_CTRL_SLAVE_RATIO_1								PHY_CTRL_SLAVE_RATIO_0							

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Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Reserved	RW	0x0
29:20	PHY_CTRL_SLAVE_RATIO_2	Slave DLL ratio for command PHY 2	RW	0x040
19:10	PHY_CTRL_SLAVE_RATIO_1	Slave DLL ratio for command PHY 1. In DDR3 mode, set to 0x100 (100%) if inverted clock is used (EMIF_DDR_PHY_CONTROL_1[18] PHY_INVERT_CLKOUT = 1).	RW	0x080
9:0	PHY_CTRL_SLAVE_RATIO_0	Slave DLL ratio for command PHY 0. In DDR3 mode, set to 0x100 (100%) if inverted clock is used (EMIF_DDR_PHY_CONTROL_1[18] PHY_INVERT_CLKOUT = 1).	RW	0x080

Table 15-237. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_1

EMIF Controller

- EMIF Module Global Initialization: [0] [1]
- EMIF Register Summary: [2]

Table 15-238. EMIF_EXT_PHY_CONTROL_1_SHADOW

Address Offset	0x0000 0204		
Physical Address	0x4C00 0204 0x4D00 0204	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_CTRL_SLAVE_RATIO_2_SHDW								PHY_CTRL_SLAVE_RATIO_1_SHDW								PHY_CTRL_SLAVE_RATIO_0_SHDW							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Reserved	RW	0x0
29:20	PHY_CTRL_SLAVE_RATIO_2_SHDW	Shadow field for PHY_CTRL_SLAVE_RATIO_2	RW	0x000
19:10	PHY_CTRL_SLAVE_RATIO_1_SHDW	Shadow field for PHY_CTRL_SLAVE_RATIO_1	RW	0x000
9:0	PHY_CTRL_SLAVE_RATIO_0_SHDW	Shadow field for PHY_CTRL_SLAVE_RATIO_0	RW	0x000

Table 15-239. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_1_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-240. EMIF_EXT_PHY_CONTROL_2

Address Offset	0x0000 0208		
Physical Address	0x4C00 0208 0x4D00 0208	**Instance**	EMIF1 EMIF2
Description	DQS gate opening delay. Set to 0x0B7 for each PHY/Rank.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_FIFO_WE_SLAVE_RATIO_1_0								PHY_FIFO_WE_SLAVE_RATIO_0_1								PHY_FIFO_WE_SLAVE_RATIO_0_0															

Bits	Field Name	Description	Type	Reset
31:22	PHY_FIFO_WE_SLAVE_RATIO_1_0	DQS gate opening delay[9:0] for Data PHY 1, Rank 0	RW	0x000
21:11	PHY_FIFO_WE_SLAVE_RATIO_0_1	DQS gate opening delay[10:0] for Data PHY 0, Rank 1	RW	0x000
10:0	PHY_FIFO_WE_SLAVE_RATIO_0_0	DQS gate opening delay[10:0] for Data PHY 0, Rank 0	RW	0x000

Table 15-241. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_2

EMIF Controller

- EMIF Register Summary: [0]

Table 15-242. EMIF_EXT_PHY_CONTROL_2_SHADOW

Address Offset	0x0000 020C		
Physical Address	0x4C00 020C 0x4D00 020C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_FIFO_WE_SLAVE_RATIO_1_0_SHDW																PHY_FIFO_WE_SLAVE_RATIO_0_1_SHDW								PHY_FIFO_WE_SLAVE_RATIO_0_0_SHDW							

Bits	Field Name	Description	Type	Reset
31:22	PHY_FIFO_WE_SLAVE_RATIO_1_0_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_1_0	RW	0x000
21:11	PHY_FIFO_WE_SLAVE_RATIO_0_1_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_0_1	RW	0x000
10:0	PHY_FIFO_WE_SLAVE_RATIO_0_0_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_0_0	RW	0x000

Table 15-243. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_2_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-244. EMIF_EXT_PHY_CONTROL_3

Address Offset	0x0000 0210		
Physical Address	0x4C00 0210 0x4D00 0210	**Instance**	EMIF1 EMIF2
Description	DQS gate opening delay. Set to 0x0B7 for each PHY/Rank.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_FIFO_WE_SLAVE_RATIO_2_1								PHY_FIFO_WE_SLAVE_RATIO_2_0								PHY_FIFO_WE_SLAVE_RATIO_1_1								PHY_FIFO_WE_SLAVE_RATIO_1_0							

Bits	Field Name	Description	Type	Reset
31:23	PHY_FIFO_WE_SLAVE_RATIO_2_1	DQS gate opening delay[8:0] for Data PHY 2, Rank 1	RW	0x000
22:12	PHY_FIFO_WE_SLAVE_RATIO_2_0	DQS gate opening delay[10:0] for Data PHY 2, Rank 0	RW	0x000
11:1	PHY_FIFO_WE_SLAVE_RATIO_1_1	DQS gate opening delay[10:0] for Data PHY 1, Rank 1	RW	0x000
0	PHY_FIFO_WE_SLAVE_RATIO_1_0	DQS gate opening delay[10] for Data PHY 1, Rank 0	RW	0

Table 15-245. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_3

EMIF Controller

- EMIF Register Summary: [0]

Table 15-246. EMIF_EXT_PHY_CONTROL_3_SHADOW

Address Offset	0x0000 0214		
Physical Address	0x4C00 0214 0x4D00 0214	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
PHY_FIFO_WE_SLAVE_RATIO_2_1_SHDW	PHY_FIFO_WE_SLAVE_RATIO_2_0_SHDW	PHY_FIFO_WE_SLAVE_RATIO_1_1_SHDW	PHY_FIFO_WE_SLAVE_RATIO_1_0_SHDW

Bits	Field Name	Description	Type	Reset
31:23	PHY_FIFO_WE_SLAVE_RATIO_2_1_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_2_1	RW	0x000
22:12	PHY_FIFO_WE_SLAVE_RATIO_2_0_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_2_0	RW	0x000
11:1	PHY_FIFO_WE_SLAVE_RATIO_1_1_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_1_1	RW	0x000
0	PHY_FIFO_WE_SLAVE_RATIO_1_0_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_1_0	RW	0

Table 15-247. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_3_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-248. EMIF_EXT_PHY_CONTROL_4

Address Offset	0x0000 0218		
Physical Address	0x4C00 0218 0x4D00 0218	**Instance**	EMIF1 EMIF2
Description	DQS gate opening delay. Set to 0x0B7 for each PHY/Rank.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	PHY_FIFO_WE_SLAVE_RATIO_3_1	PHY_FIFO_WE_SLAVE_RATIO_3_0	PHY_FIFO_WE_SLAVE_RATIO_2_1

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	RW	0x00
23:13	PHY_FIFO_WE_SLAVE_RATIO_3_1	DQS gate opening delay[10:0] for Data PHY 3, Rank 1	RW	0x000
12:2	PHY_FIFO_WE_SLAVE_RATIO_3_0	DQS gate opening delay[10:0] for Data PHY 3, Rank 0	RW	0x000
1:0	PHY_FIFO_WE_SLAVE_RATIO_2_1	DQS gate opening delay[10:9] for Data PHY 2, Rank 1	RW	0x0

Table 15-249. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_4

EMIF Controller

- EMIF Register Summary: [0]

Table 15-250. EMIF_EXT_PHY_CONTROL_4_SHADOW

Address Offset	0x0000 021C		
Physical Address	0x4C00 021C 0x4D00 021C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_FIFO_WE_SLAVE_RATIO_3_1_SHDW								PHY_FIFO_WE_SLAVE_RATIO_3_0_SHDW										PHY_FIFO_WE_SLAVE_RATIO_2_1_SHDW							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	RW	0x00
23:13	PHY_FIFO_WE_SLAVE_RATIO_3_1_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_3_1	RW	0x000
12:2	PHY_FIFO_WE_SLAVE_RATIO_3_0_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_3_0	RW	0x000
1:0	PHY_FIFO_WE_SLAVE_RATIO_2_1_SHDW	Shadow field for PHY_FIFO_WE_SLAVE_RATIO_2_1	RW	0x0

Table 15-251. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_4_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-252. EMIF_EXT_PHY_CONTROL_5

Address Offset	0x0000 0220		
Physical Address	0x4C00 0220 0x4D00 0220	**Instance**	EMIF1 EMIF2
Description	Ratio value for read DQS slave DLL. Do not change. This is a fixed value in LPDDR2 mode, and a don't care in DDR3 mode due to the training.		
Type	RW		

31 30	29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
PHY_RD_DQS_SLAVE_RATIO_1_1	PHY_RD_DQS_SLAVE_RATIO_1_0	PHY_RD_DQS_SLAVE_RATIO_0_1		PHY_RD_DQS_SLAVE_RATIO_0_0

Bits	Field Name	Description	Type	Reset
31:30	PHY_RD_DQS_SLAVE_RATIO_1_1	Ratio value for read DQS slave DLL.[1:0] for Data PHY 1, Rank 1	RW	0x0
29:20	PHY_RD_DQS_SLAVE_RATIO_1_0	Ratio value for read DQS slave DLL.[9:0] for Data PHY 1, Rank 0	RW	0x040
19:10	PHY_RD_DQS_SLAVE_RATIO_0_1	Ratio value for read DQS slave DLL.[9:0] for Data PHY 0, Rank 1	RW	0x040
9:0	PHY_RD_DQS_SLAVE_RATIO_0_0	Ratio value for read DQS slave DLL.[9:0] for Data PHY 0, Rank 0	RW	0x040

Table 15-253. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_5

EMIF Controller

- EMIF Register Summary: [0]

Table 15-254. EMIF_EXT_PHY_CONTROL_5_SHADOW

Address Offset	0x0000 0224		
Physical Address	0x4C00 0224 0x4D00 0224	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

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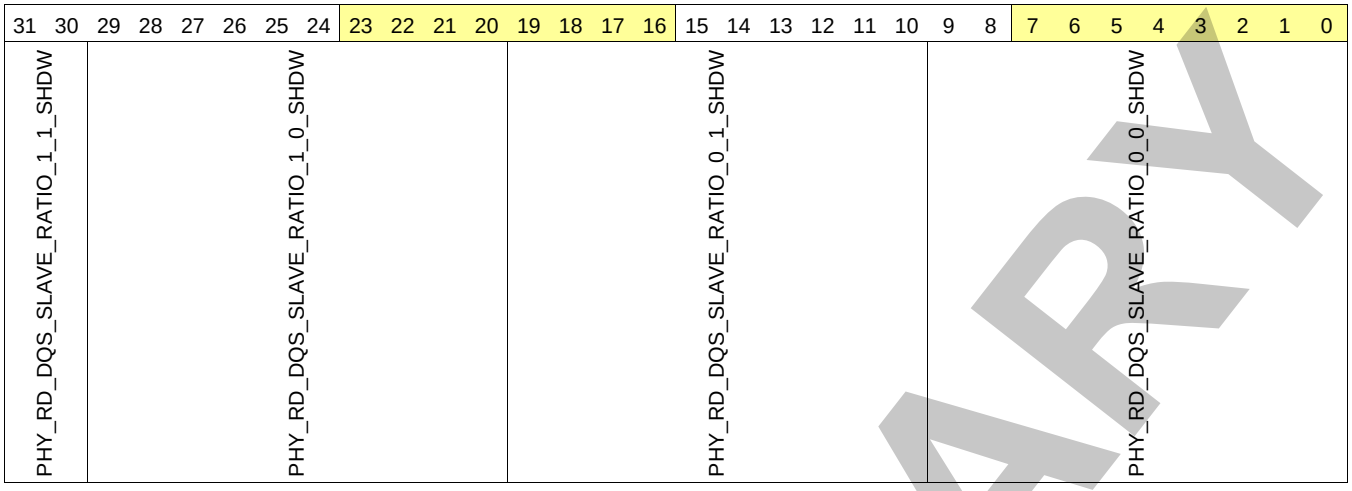


Bits	Field Name	Description	Type	Reset
31:30	PHY_RD_DQS_SLAVE_RATIO_1_1_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_1_1	RW	0x0
29:20	PHY_RD_DQS_SLAVE_RATIO_1_0_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_1_0	RW	0x000
19:10	PHY_RD_DQS_SLAVE_RATIO_0_1_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_0_1	RW	0x000
9:0	PHY_RD_DQS_SLAVE_RATIO_0_0_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_0_0	RW	0x000

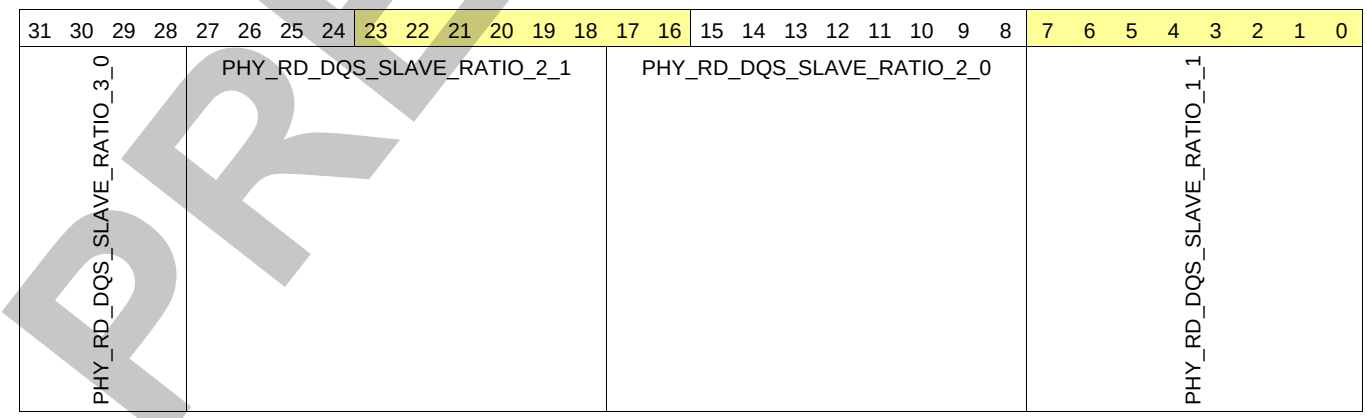
Table 15-255. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_5_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-256. EMIF_EXT_PHY_CONTROL_6

Address Offset	0x0000 0228		
Physical Address	0x4C00 0228 0x4D00 0228	**Instance**	EMIF1 EMIF2
Description	Ratio value for read DQS slave DLL. Do not change. This is a fixed value in LPDDR2 mode, and a don't care in DDR3 mode due to the training.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:28	PHY_RD_DQS_SLAVE_RATIO_3_0	Ratio value for read DQS slave DLL.[3:0] for Data PHY 3, Rank 0	RW	0x0
27:18	PHY_RD_DQS_SLAVE_RATIO_2_1	Ratio value for read DQS slave DLL.[9:0] for Data PHY 2, Rank 1	RW	0x040
17:8	PHY_RD_DQS_SLAVE_RATIO_2_0	Ratio value for read DQS slave DLL.[9:0] for Data PHY 2, Rank 0	RW	0x040
7:0	PHY_RD_DQS_SLAVE_RATIO_1_1	Ratio value for read DQS slave DLL.[9:2] for Data PHY 1, Rank 1	RW	0x10

Table 15-257. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_6

EMIF Controller

- EMIF Register Summary: [0]

Table 15-258. EMIF_EXT_PHY_CONTROL_6_SHADOW

Address Offset	0x0000 022C		
Physical Address	0x4C00 022C 0x4D00 022C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
PHY_RD_DQS_SLAVE_RATIO_3_0_SHDW	PHY_RD_DQS_SLAVE_RATIO_2_1_SHDW		PHY_RD_DQS_SLAVE_RATIO_2_0_SHDW	PHY_RD_DQS_SLAVE_RATIO_1_1_SHDW

Bits	Field Name	Description	Type	Reset
31:28	PHY_RD_DQS_SLAVE_RATIO_3_0_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_3_0	RW	0x0
27:18	PHY_RD_DQS_SLAVE_RATIO_2_1_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_2_1	RW	0x000
17:8	PHY_RD_DQS_SLAVE_RATIO_2_0_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_2_0	RW	0x000
7:0	PHY_RD_DQS_SLAVE_RATIO_1_1_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_1_1	RW	0x00

Table 15-259. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_6_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

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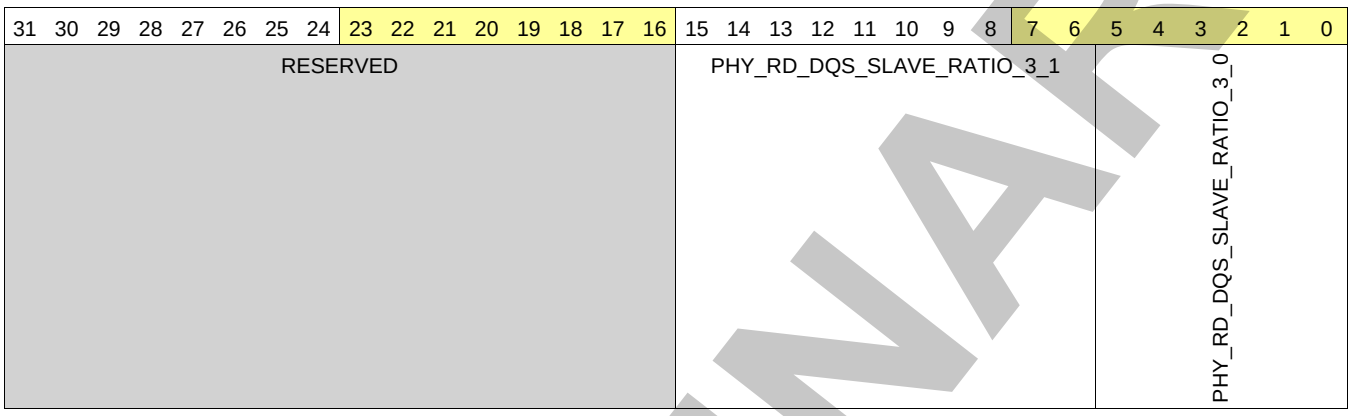
Table 15-260. EMIF_EXT_PHY_CONTROL_7

Address Offset	0x0000 0230		
Physical Address	0x4C00 0230 0x4D00 0230	**Instance**	EMIF1 EMIF2
Description	Ratio value for read DQS slave DLL. Do not change. This is a fixed value in LPDDR2 mode, and a don't care in DDR3 mode due to the training.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x0000
15:6	PHY_RD_DQS_SLAVE_RATIO_3_1	Ratio value for read DQS slave DLL.[9:0] for Data PHY 3, Rank 1	RW	0x040
5:0	PHY_RD_DQS_SLAVE_RATIO_3_0	Ratio value for read DQS slave DLL.[9:4] for Data PHY 3, Rank 0	RW	0x04

Table 15-261. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_7

EMIF Controller

- EMIF Register Summary: [0]

Table 15-262. EMIF_EXT_PHY_CONTROL_7_SHADOW

Address Offset	0x0000 0234		
Physical Address	0x4C00 0234 0x4D00 0234	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

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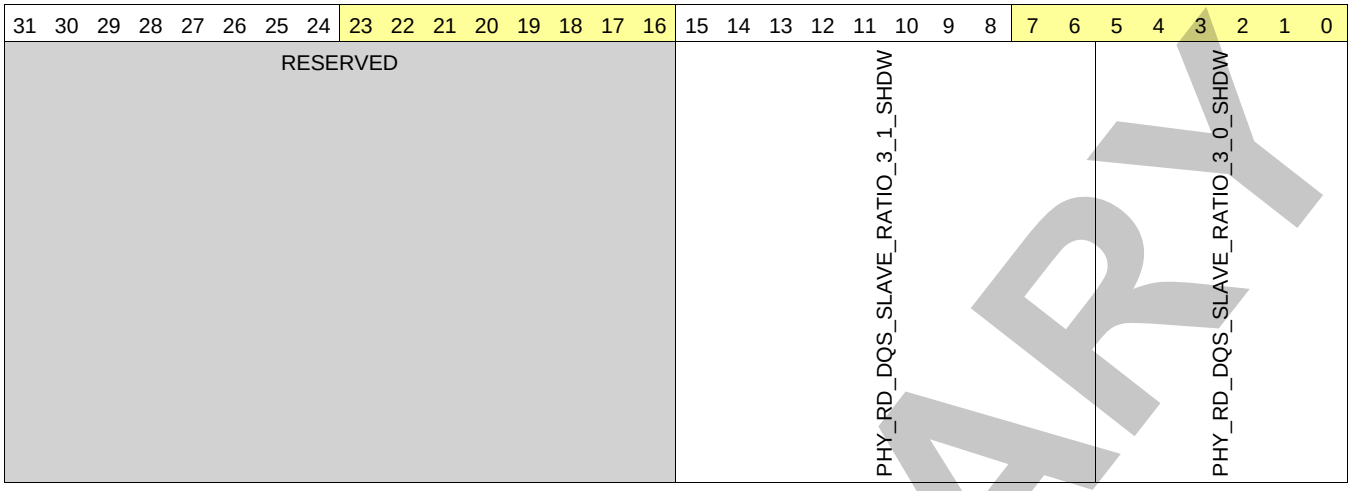


Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x0000
15:6	PHY_RD_DQS_SLAVE_RATIO_3_1_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_3_1	RW	0x000
5:0	PHY_RD_DQS_SLAVE_RATIO_3_0_SHDW	Shadow field for PHY_RD_DQS_SLAVE_RATIO_3_0	RW	0x00

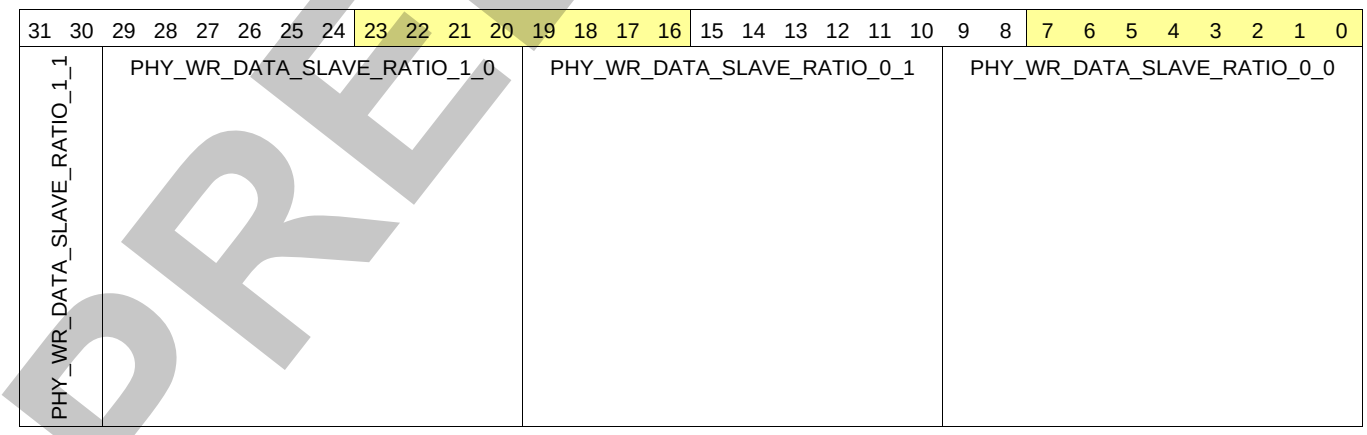
Table 15-263. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_7_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-264. EMIF_EXT_PHY_CONTROL_8

Address Offset	0x0000 0238		
Physical Address	0x4C00 0238 0x4D00 0238	**Instance**	EMIF1 EMIF2
Description	Ratio value for write data slave DLL. Do not change. This is a fixed value in LPDDR2 mode, and a don't care in DDR3 mode due to the training.		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31:30	PHY_WR_DATA_SLAVE_RATIO_1_1	Ratio value for write data slave DLL.[1:0] for Data PHY 1, Rank 1	RW	0x0
29:20	PHY_WR_DATA_SLAVE_RATIO_1_0	Ratio value for write data slave DLL.[9:0] for Data PHY 1, Rank 0	RW	0x040
19:10	PHY_WR_DATA_SLAVE_RATIO_0_1	Ratio value for write data slave DLL.[9:0] for Data PHY 0, Rank 1	RW	0x040
9:0	PHY_WR_DATA_SLAVE_RATIO_0_0	Ratio value for write data slave DLL.[9:0] for Data PHY 0, Rank 0	RW	0x040

Table 15-265. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_8

EMIF Controller

- EMIF Register Summary: [0]

Table 15-266. EMIF_EXT_PHY_CONTROL_8_SHADOW

Address Offset	0x0000 023C		
Physical Address	0x4C00 023C 0x4D00 023C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31 30	29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
PHY_WR_DATA_SLAVE_RATIO_1_1_SHDW	PHY_WR_DATA_SLAVE_RATIO_1_0_SHDW		PHY_WR_DATA_SLAVE_RATIO_0_1_SHDW		PHY_WR_DATA_SLAVE_RATIO_0_0_SHDW

Bits	Field Name	Description	Type	Reset
31:30	PHY_WR_DATA_SLAVE_RATIO_1_1_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_1_1	RW	0x0
29:20	PHY_WR_DATA_SLAVE_RATIO_1_0_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_1_0	RW	0x000
19:10	PHY_WR_DATA_SLAVE_RATIO_0_1_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_0_1	RW	0x000
9:0	PHY_WR_DATA_SLAVE_RATIO_0_0_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_0_0	RW	0x000

Table 15-267. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_8_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-268. EMIF_EXT_PHY_CONTROL_9

Address Offset	0x0000 0240		
Physical Address	0x4C00 0240 0x4D00 0240	**Instance**	EMIF1 EMIF2
Description	Ratio value for write data slave DLL. Do not change. This is a fixed value in LPDDR2 mode, and a don't care in DDR3 mode due to the training.		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
PHY_WR_DATA_SLAVE_RATIO_3_0	PHY_WR_DATA_SLAVE_RATIO_2_1		PHY_WR_DATA_SLAVE_RATIO_2_0	PHY_WR_DATA_SLAVE_RATIO_1_1

Bits	Field Name	Description	Type	Reset
31:28	PHY_WR_DATA_SLAVE_RATIO_3_0	Ratio value for write data slave DLL.[3:0] for Data PHY 3, Rank 0	RW	0x0
27:18	PHY_WR_DATA_SLAVE_RATIO_2_1	Ratio value for write data slave DLL.[9:0] for Data PHY 2, Rank 1	RW	0x040
17:8	PHY_WR_DATA_SLAVE_RATIO_2_0	Ratio value for write data slave DLL.[9:0] for Data PHY 2, Rank 0	RW	0x040
7:0	PHY_WR_DATA_SLAVE_RATIO_1_1	Ratio value for write data slave DLL.[9:2] for Data PHY 1, Rank 1	RW	0x10

Table 15-269. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_9

EMIF Controller

- EMIF Register Summary: [0]

Table 15-270. EMIF_EXT_PHY_CONTROL_9_SHADOW

Address Offset	0x0000 0244		
Physical Address	0x4C00 0244 0x4D00 0244	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

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31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
PHY_WR_DATA_SLAVE_RATIO_3_0_SHDW		PHY_WR_DATA_SLAVE_RATIO_2_1_SHDW		PHY_WR_DATA_SLAVE_RATIO_2_0_SHDW		PHY_WR_DATA_SLAVE_RATIO_1_1_SHDW	

Bits	Field Name	Description	Type	Reset
31:28	PHY_WR_DATA_SLAVE_RATIO_3_0_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_3_0	RW	0x0
27:18	PHY_WR_DATA_SLAVE_RATIO_2_1_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_2_1	RW	0x000
17:8	PHY_WR_DATA_SLAVE_RATIO_2_0_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_2_0	RW	0x000
7:0	PHY_WR_DATA_SLAVE_RATIO_1_1_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_1_1	RW	0x00

Table 15-271. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_9_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-272. EMIF_EXT_PHY_CONTROL_10

Address Offset	0x0000 0248		
Physical Address	0x4C00 0248 0x4D00 0248	**Instance**	EMIF1 EMIF2
Description	Ratio value for write data slave DLL. Do not change. This is a fixed value in LPDDR2 mode, and a don't care in DDR3 mode due to the training.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED		PHY_WR_DATA_SLAVE_RATIO_3_1	PHY_WR_DATA_SLAVE_RATIO_3_0

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x0000
15:6	PHY_WR_DATA_SLAVE_RATIO_3_1	Ratio value for write data slave DLL.[9:0] for Data PHY 3, Rank 1	RW	0x040
5:0	PHY_WR_DATA_SLAVE_RATIO_3_0	Ratio value for write data slave DLL.[9:4] for Data PHY 3, Rank 0	RW	0x04

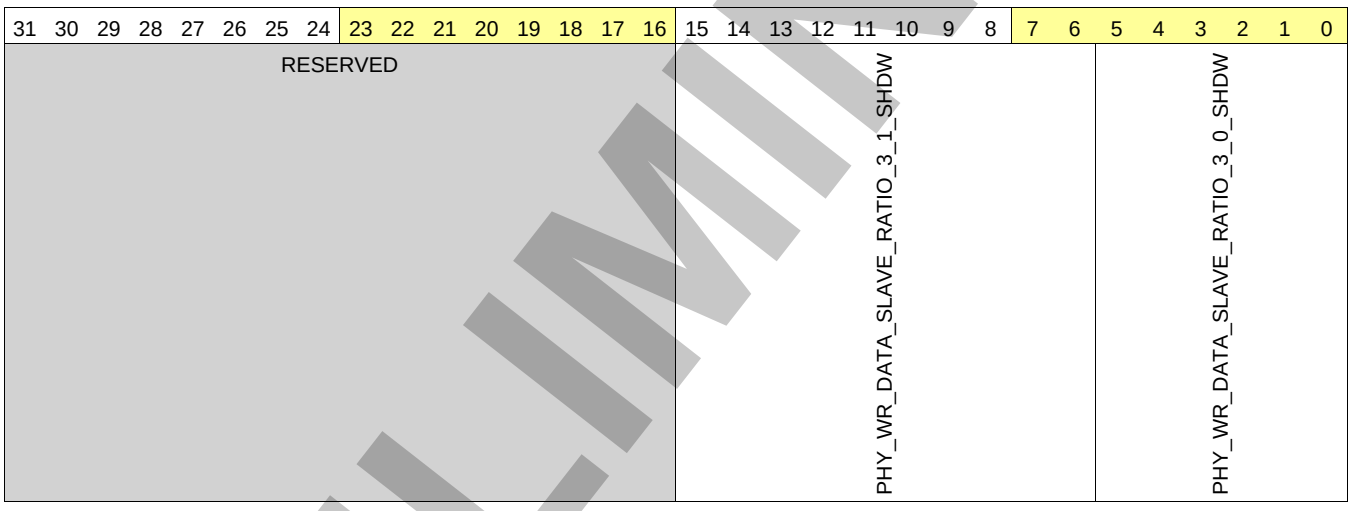
Table 15-273. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_10

EMIF Controller

- EMIF Register Summary: [0]

Table 15-274. EMIF_EXT_PHY_CONTROL_10_SHADOW

Address Offset	0x0000 024C		
Physical Address	0x4C00 024C 0x4D00 024C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x0000
15:6	PHY_WR_DATA_SLAVE_RATIO_3_1_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_3_1	RW	0x000
5:0	PHY_WR_DATA_SLAVE_RATIO_3_0_SHDW	Shadow field for PHY_WR_DATA_SLAVE_RATIO_3_0	RW	0x00

Table 15-275. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_10_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-276. EMIF_EXT_PHY_CONTROL_11

Address Offset	0x0000 0250		
Physical Address	0x4C00 0250 0x4D00 0250	**Instance**	EMIF1 EMIF2
Description	Ratio value for write DQS slave DLL. Do not change. This is a fixed value in LPDDR2 mode, and a don't care in DDR3 mode due to the training.		

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Table 15-276. EMIF_EXT_PHY_CONTROL_11 (continued)

Type	RW

31 30	29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
PHY_WR_DQS_SLAVE_RATIO_1_1	PHY_WR_DQS_SLAVE_RATIO_1_0	PHY_WR_DQS_SLAVE_RATIO_0_1		PHY_WR_DQS_SLAVE_RATIO_0_0	

Bits	Field Name	Description	Type	Reset
31:30	PHY_WR_DQS_SLAVE_RATIO_1_1	Ratio value for write DQS slave DLL.[1:0] for Data PHY 1, Rank 1	RW	0x0
29:20	PHY_WR_DQS_SLAVE_RATIO_1_0	Ratio value for write DQS slave DLL.[9:0] for Data PHY 1, Rank 0	RW	0x000
19:10	PHY_WR_DQS_SLAVE_RATIO_0_1	Ratio value for write DQS slave DLL.[9:0] for Data PHY 0, Rank 1	RW	0x000
9:0	PHY_WR_DQS_SLAVE_RATIO_0_0	Ratio value for write DQS slave DLL.[9:0] for Data PHY 0, Rank 0	RW	0x000

Table 15-277. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_11

EMIF Controller

- EMIF Register Summary: [0]

Table 15-278. EMIF_EXT_PHY_CONTROL_11_SHADOW

Address Offset	0x0000 0254		
Physical Address	0x4C00 0254 0x4D00 0254	Instance	EMIF1 EMIF2
Description			
Type	RW		

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31 30	29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7 6 5 4 3 2 1 0
PHY_WR_DQS_SLAVE_RATIO_1_1_SHDW	PHY_WR_DQS_SLAVE_RATIO_1_0_SHDW		PHY_WR_DQS_SLAVE_RATIO_0_1_SHDW		PHY_WR_DQS_SLAVE_RATIO_0_0_SHDW

Bits	Field Name	Description	Type	Reset
31:30	PHY_WR_DQS_SLAVE_RATIO_1_1_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_1_1	RW	0x0
29:20	PHY_WR_DQS_SLAVE_RATIO_1_0_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_1_0	RW	0x000
19:10	PHY_WR_DQS_SLAVE_RATIO_0_1_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_0_1	RW	0x000
9:0	PHY_WR_DQS_SLAVE_RATIO_0_0_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_0_0	RW	0x000

Table 15-279. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_11_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-280. EMIF_EXT_PHY_CONTROL_12

Address Offset	0x0000 0258		
Physical Address	0x4C00 0258 0x4D00 0258	**Instance**	EMIF1 EMIF2
Description	Ratio value for write DQS slave DLL. Do not change. This is a fixed value in LPDDR2 mode, and a don't care in DDR3 mode due to the training.		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
PHY_WR_DQS_SLAVE_RATIO_3_0	PHY_WR_DQS_SLAVE_RATIO_2_1		PHY_WR_DQS_SLAVE_RATIO_2_0	PHY_WR_DQS_SLAVE_RATIO_1_1

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Bits	Field Name	Description	Type	Reset
31:28	PHY_WR_DQS_SLAVE_RATIO_3_0	Ratio value for write DQS slave DLL.[3:0] for Data PHY 3, Rank 0	RW	0x0
27:18	PHY_WR_DQS_SLAVE_RATIO_2_1	Ratio value for write DQS slave DLL.[9:0] for Data PHY 2, Rank 1	RW	0x000
17:8	PHY_WR_DQS_SLAVE_RATIO_2_0	Ratio value for write DQS slave DLL.[9:0] for Data PHY 2, Rank 0	RW	0x000
7:0	PHY_WR_DQS_SLAVE_RATIO_1_1	Ratio value for write DQS slave DLL.[9:2] for Data PHY 1, Rank 1	RW	0x00

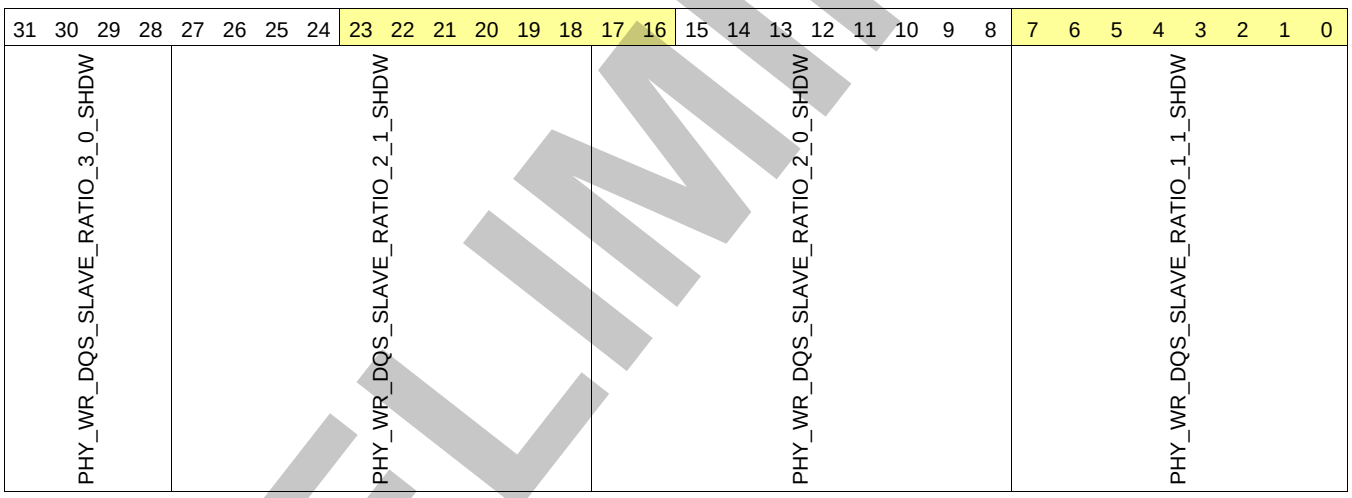
Table 15-281. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_12

EMIF Controller

- EMIF Register Summary: [0]

Table 15-282. EMIF_EXT_PHY_CONTROL_12_SHADOW

Address Offset	0x0000 025C		
Physical Address	0x4C00 025C 0x4D00 025C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:28	PHY_WR_DQS_SLAVE_RATIO_3_0_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_3_0	RW	0x0
27:18	PHY_WR_DQS_SLAVE_RATIO_2_1_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_2_1	RW	0x000
17:8	PHY_WR_DQS_SLAVE_RATIO_2_0_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_2_0	RW	0x000
7:0	PHY_WR_DQS_SLAVE_RATIO_1_1_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_1_1	RW	0x00

Table 15-283. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_12_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

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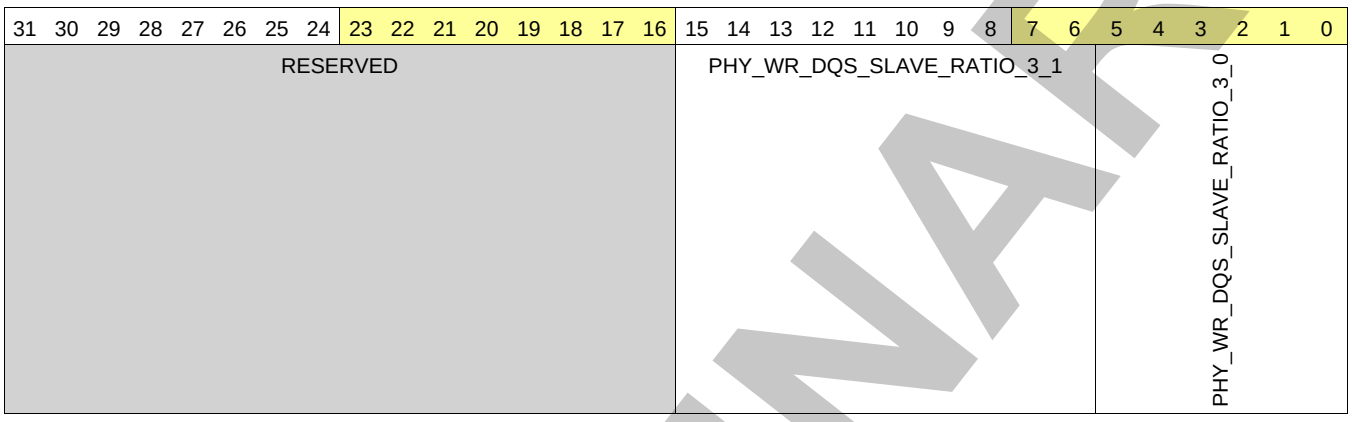
Table 15-284. EMIF_EXT_PHY_CONTROL_13

Address Offset	0x0000 0260		
Physical Address	0x4C00 0260 0x4D00 0260	**Instance**	EMIF1 EMIF2
Description	Ratio value for write DQS slave DLL. Do not change. This is a fixed value in LPDDR2 mode, and a don't care in DDR3 mode due to the training.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x0000
15:6	PHY_WR_DQS_SLAVE_RATIO_3_1	Ratio value for write DQS slave DLL.[9:0] for Data PHY 3, Rank 1	RW	0x000
5:0	PHY_WR_DQS_SLAVE_RATIO_3_0	Ratio value for write DQS slave DLL.[9:4] for Data PHY 3, Rank 0	RW	0x00

Table 15-285. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_13

EMIF Controller

- EMIF Register Summary: [0]

Table 15-286. EMIF_EXT_PHY_CONTROL_13_SHADOW

Address Offset	0x0000 0264		
Physical Address	0x4C00 0264 0x4D00 0264	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

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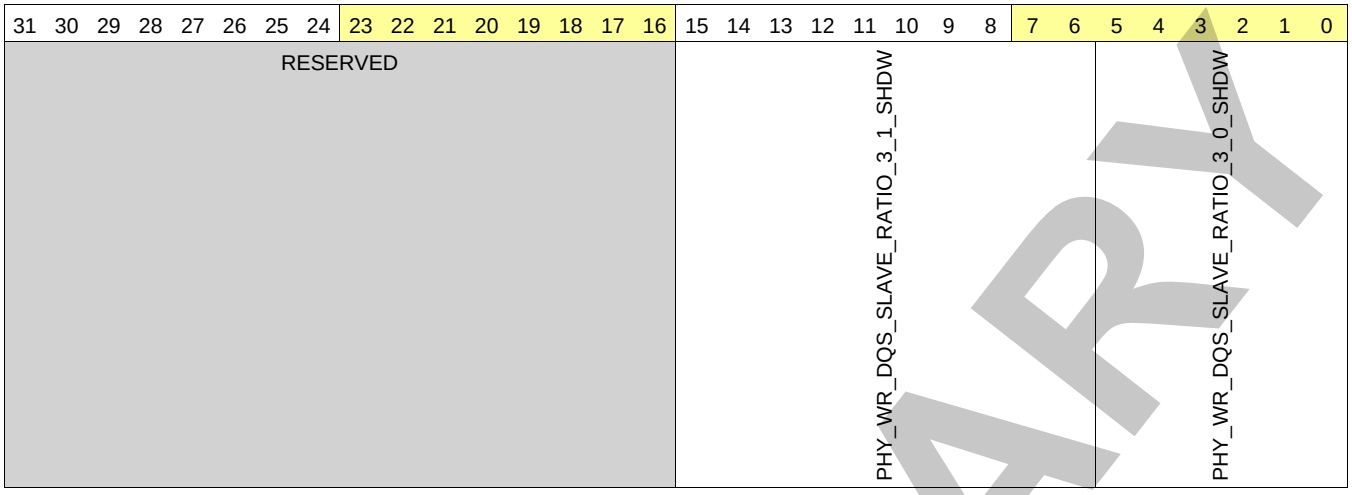


Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x0000
15:6	PHY_WR_DQS_SLAVE_RATIO_3_1_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_3_1	RW	0x000
5:0	PHY_WR_DQS_SLAVE_RATIO_3_0_SHDW	Shadow field for PHY_WR_DQS_SLAVE_RATIO_3_0	RW	0x00

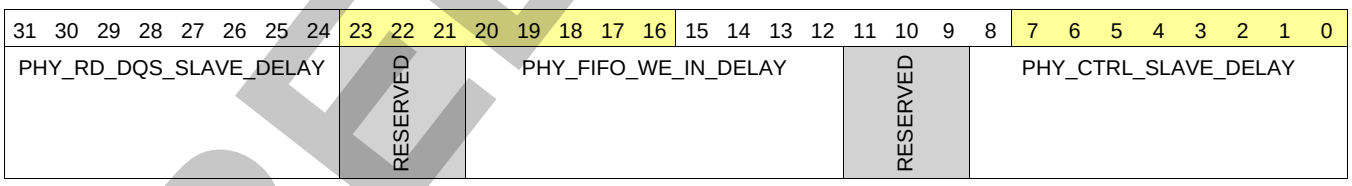
Table 15-287. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_13_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-288. EMIF_EXT_PHY_CONTROL_14

Address Offset	0x0000 0268		
Physical Address	0x4C00 0268 0x4D00 0268	**Instance**	EMIF1 EMIF2
Description	Only relevant when using the DLL in unlocked mode.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:24	PHY_RD_DQS_SLAVE_DELAY	Replace delay/tap value for read DQS slave DLL with this value. Broadcast to all Ranks, all data PHYs, bits [7:0]	RW	0x80
23:21	RESERVED	Reserved	RW	0x0
20:12	PHY_FIFO_WE_IN_DELAY	Replace delay/tap value for slave DLL with this value. Broadcast to all Ranks, all data PHYs	RW	0x080
11:9	RESERVED	Reserved	RW	0x0
8:0	PHY_CTRL_SLAVE_DELAY	Replace delay/tap value for address/command timing slave DLL with this value. Broadcast to Command PHYs 2,1, and 0.	RW	0x080

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Table 15-289. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_14

EMIF Controller

- EMIF Register Summary: [0]

Table 15-290. EMIF_EXT_PHY_CONTROL_14_SHADOW

Address Offset	0x0000 026C		
Physical Address	0x4C00 026C 0x4D00 026C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RD_DQS_SLAVE_DELAY_SHDW								RESERVED			PHY_FIFO_WE_IN_DELAY_SHDW									RESERVED				PHY_CTRL_SLAVE_DELAY_SHDW							

Bits	Field Name	Description	Type	Reset
31:24	PHY_RD_DQS_SLAVE_DELAY_SHDW	Shadow field for PHY_RD_DQS_SLAVE_DELAY	RW	0x00
23:21	RESERVED	Reserved	RW	0x0
20:12	PHY_FIFO_WE_IN_DELAY_SHDW	Shadow field for PHY_FIFO_WE_IN_DELAY	RW	0x000
11:9	RESERVED	Reserved	RW	0x0
8:0	PHY_CTRL_SLAVE_DELAY_SHDW	Shadow field for PHY_CTRL_SLAVE_DELAY	RW	0x000

Table 15-291. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_14_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-292. EMIF_EXT_PHY_CONTROL_15

Address Offset	0x0000 0270		
Physical Address	0x4C00 0270 0x4D00 0270	**Instance**	EMIF1 EMIF2
Description	Only relevant when using the DLL in unlocked mode.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_WR_DATA_SLAVE_DELAY								RESERVED			PHY_WR_DQS_SLAVE_DELAY									RESERVED			PHY_RD_DQS_SLAVE_DELA

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved	RW	0x00
24:16	PHY_WR_DATA_SLAVE_DELAY	Replace delay/tap value for write data slave DLL with this value. Broadcast to all Ranks, all data PHYs	RW	0x080
15:13	RESERVED	Reserved	RW	0x0
12:4	PHY_WR_DQS_SLAVE_DELAY	Replace delay/tap value for write DQS slave DLL with this value. Broadcast to all Ranks, all data PHYs	RW	0x080
3:1	RESERVED	Reserved	RW	0x0
0	PHY_RD_DQS_SLAVE_DELAY	Replace delay/tap value for read DQS slave DLL with this value. Broadcast to all Ranks, all data PHYs, bit 8	RW	0

Table 15-293. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_15

EMIF Controller

- EMIF Register Summary: [0]

Table 15-294. EMIF_EXT_PHY_CONTROL_15_SHADOW

Address Offset	0x0000 0274		
Physical Address	0x4C00 0274 0x4D00 0274	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_WR_DATA_SLAVE_DELAY_SHDW								RESERVED			PHY_WR_DQS_SLAVE_DELAY_SHDW									RESERVED			PHY_RD_DQS_SLAVE_DELA_SHDW

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Reserved	RW	0x00
24:16	PHY_WR_DATA_SLAVE_DELAY_SHDW	Shadow field for PHY_WR_DATA_SLAVE_DELAY	RW	0x000

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Bits	Field Name	Description	Type	Reset
15:13	RESERVED	Reserved	RW	0x0
12:4	PHY_WR_DQS_SLAVE_DELAY_SHDW	Shadow field for PHY_WR_DQS_SLAVE_DELAY	RW	0x000
3:1	RESERVED	Reserved	RW	0x0
0	PHY_RD_DQS_SLAVE_DELAY_SHDW	Shadow field for PHY_RD_DQS_SLAVE_DELAY	RW	0

Table 15-295. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_15_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-296. EMIF_EXT_PHY_CONTROL_16

Address Offset	0x0000 0278		
Physical Address	0x4C00 0278 0x4D00 0278	**Instance**	EMIF1 EMIF2
Description	Offset value from write dqs to write dq during write leveling. Set to 0x40 in LPDDR2 mode. Don't care in DDR3 mode due to the leveling.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PHY_DQ_OFFSET_3				PHY_DQ_OFFSET_2								PHY_DQ_OFFSET_1								PHY_DQ_OFFSET_0							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	RW	0x0
27:21	PHY_DQ_OFFSET_3	Offset value from write dqs to write dq during write leveling. Data PHY 3	RW	0x00
20:14	PHY_DQ_OFFSET_2	Offset value from write dqs to write dq during write leveling. Data PHY 2	RW	0x00
13:7	PHY_DQ_OFFSET_1	Offset value from write dqs to write dq during write leveling. Data PHY 1	RW	0x00
6:0	PHY_DQ_OFFSET_0	Offset value from write dqs to write dq during write leveling. Data PHY 0	RW	0x00

Table 15-297. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_16

EMIF Controller

- EMIF Register Summary: [0]

Table 15-298. EMIF_EXT_PHY_CONTROL_16_SHADOW

Address Offset	0x0000 027C		
Physical Address	0x4C00 027C 0x4D00 027C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

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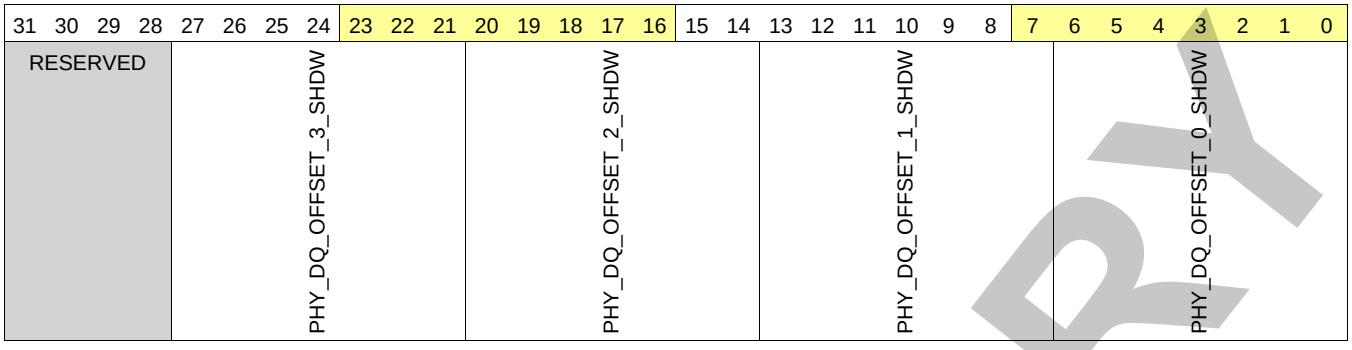


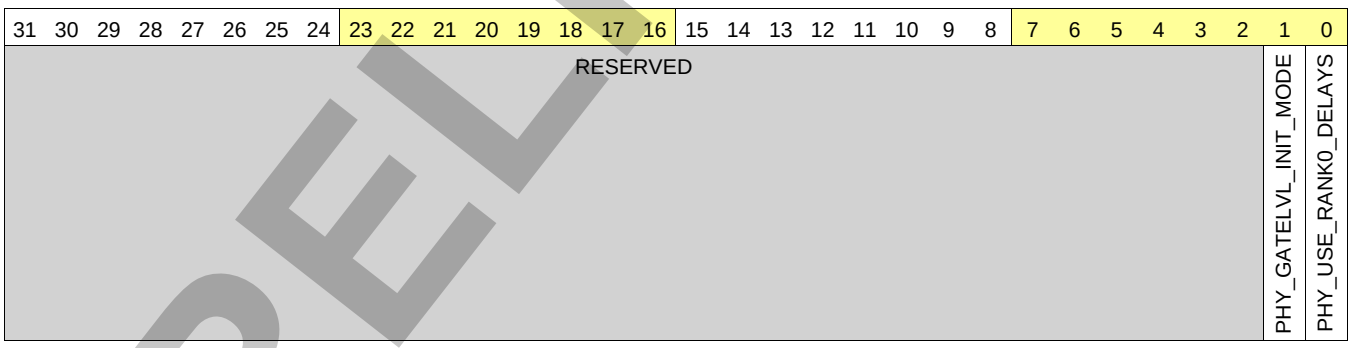
Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	RW	0x0
27:21	PHY_DQ_OFFSET_3_SHDW	Shadow field for PHY_DQ_OFFSET_3	RW	0x00
20:14	PHY_DQ_OFFSET_2_SHDW	Shadow field for PHY_DQ_OFFSET_2	RW	0x00
13:7	PHY_DQ_OFFSET_1_SHDW	Shadow field for PHY_DQ_OFFSET_1	RW	0x00
6:0	PHY_DQ_OFFSET_0_SHDW	Shadow field for PHY_DQ_OFFSET_0	RW	0x00

Table 15-299. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_16_SHADOW

EMIF Controller
- EMIF Register Summary: [0]

Table 15-300. EMIF_EXT_PHY_CONTROL_17

Address Offset	0x0000 0280		
Physical Address	0x4C00 0280 0x4D00 0280	**Instance**	EMIF1 EMIF2
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	RW	0x0000 0000
1	PHY_GATELVL_INIT_MODE	The user programmable init ratio selection mode. This bit must be 1 when in LPDDR2 mode. 1: selects a starting ratio value based on PHY_GATELVL_INIT_RATIO fields. 0: selects a starting ratio value based on Write Leveling of the same data PHY. This mode is only supported when write leveling has been run before gate leveling.	RW	1

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Bits	Field Name	Description	Type	Reset
0	PHY_USE_RANK0_DELAYS	Delay selection. Must be set to 1 for LPDDR2, not recommended in DDR3 mode. 1: Rank 0 delays are used for both ranks during read/write. 0: Each Rank uses its own delay.	RW	0

Table 15-301. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_17

EMIF Controller

- EMIF Register Summary: [0]

Table 15-302. EMIF_EXT_PHY_CONTROL_17_SHADOW

Address Offset	0x0000 0284		
Physical Address	0x4C00 0284 0x4D00 0284	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	RW	0x0000 0000

Table 15-303. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_17_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-304. EMIF_EXT_PHY_CONTROL_18

Address Offset	0x0000 0288		
Physical Address	0x4C00 0288 0x4D00 0288	**Instance**	EMIF1 EMIF2
Description	DQS gate training starting ratio. The recommended setting of PHY_GATELVL_INIT_RATIO is half cycle less than total delay required on fifo_we_in to align to DQS at PHY.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GATELVL_INIT_RATIO_1_0										PHY_GATELVL_INIT_RATIO_0_1										PHY_GATELVL_INIT_RATIO_0_0											

Bits	Field Name	Description	Type	Reset
31:22	PHY_GATELVL_INIT_RATIO_1_0	DQS gate training starting ratio[9:0] for Data PHY 1, Rank 0	RW	0x150
21:11	PHY_GATELVL_INIT_RATIO_0_1	DQS gate training starting ratio[10:0] for Data PHY 0, Rank 1	RW	0x150
10:0	PHY_GATELVL_INIT_RATIO_0_0	DQS gate training starting ratio[10:0] for Data PHY 0, Rank 0	RW	0x150

Table 15-305. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_18

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-306. EMIF_EXT_PHY_CONTROL_18_SHADOW

Address Offset	0x0000 028C		
Physical Address	0x4C00 028C 0x4D00 028C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	RW	0x0000 0000

Table 15-307. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_18_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-308. EMIF_EXT_PHY_CONTROL_19

Address Offset	0x0000 0290		
Physical Address	0x4C00 0290 0x4D00 0290	**Instance**	EMIF1 EMIF2
Description	DQS gate training starting ratio. The recommended setting of PHY_GATELVL_INIT_RATIO is half cycle less than total delay required on fifo_we_in to align to DQS at PHY.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GATELVL_INIT_RATIO_2_1								PHY_GATELVL_INIT_RATIO_2_0								PHY_GATELVL_INIT_RATIO_1_1								PHY_GATELVL_INIT_RATIO_1_0							

Bits	Field Name	Description	Type	Reset
31:23	PHY_GATELVL_INIT_RATIO_2_1	DQS gate training starting ratio[8:0] for Data PHY 2, Rank 1	RW	0x150
22:12	PHY_GATELVL_INIT_RATIO_2_0	DQS gate training starting ratio[10:0] for Data PHY 2, Rank 0	RW	0x150
11:1	PHY_GATELVL_INIT_RATIO_1_1	DQS gate training starting ratio[10:0] for Data PHY 1, Rank 1	RW	0x150
0	PHY_GATELVL_INIT_RATIO_1_0	DQS gate training starting ratio[10] for Data PHY 1, Rank 0	RW	0

Table 15-309. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_19

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-310. EMIF_EXT_PHY_CONTROL_19_SHADOW

Address Offset	0x0000 0294		
Physical Address	0x4C00 0294 0x4D00 0294	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	RW	0x0000 0000

Table 15-311. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_19_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-312. EMIF_EXT_PHY_CONTROL_20

Address Offset	0x0000 0298		
Physical Address	0x4C00 0298 0x4D00 0298	**Instance**	EMIF1 EMIF2
Description	DQS gate training starting ratio. The recommended setting of PHY_GATELVL_INIT_RATIO is half cycle less than total delay required on fifo_we_in to align to DQS at PHY.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_GATELVL_INIT_RATIO_3_1								PHY_GATELVL_INIT_RATIO_3_0														PHY_GATELVL_INIT_RATIO_2_1		

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	RW	0x00
23:13	PHY_GATELVL_INIT_RATIO_3_1	DQS gate training starting ratio[10:0] for Data PHY 3, Rank 1	RW	0x150
12:2	PHY_GATELVL_INIT_RATIO_3_0	DQS gate training starting ratio[10:0] for Data PHY 3, Rank 0	RW	0x150
1:0	PHY_GATELVL_INIT_RATIO_2_1	DQS gate training starting ratio[10:9] for Data PHY 2, Rank 1	RW	0x0

Table 15-313. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_20

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-314. EMIF_EXT_PHY_CONTROL_20_SHADOW

Address Offset	0x0000 029C		
Physical Address	0x4C00 029C 0x4D00 029C	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	RW	0x0000 0000

Table 15-315. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_20_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-316. EMIF_EXT_PHY_CONTROL_21

Address Offset	0x0000 02A0		
Physical Address	0x4C00 02A0 0x4D00 02A0	**Instance**	EMIF1 EMIF2
Description	Write leveling starting ratio. The recommended setting of PHY_WRLVL_INIT_RATIO is half cycle less than total skew between CLK and DQS at the DDR.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_INIT_RATIO_1_1								PHY_WRLVL_INIT_RATIO_1_0								PHY_WRLVL_INIT_RATIO_0_1								PHY_WRLVL_INIT_RATIO_0_0							

Bits	Field Name	Description	Type	Reset
31:30	PHY_WRLVL_INIT_RATIO_1_1	Write leveling starting ratio[1:0] for Data PHY 1, Rank 1	RW	0x0
29:20	PHY_WRLVL_INIT_RATIO_1_0	Write leveling starting ratio[9:0] for Data PHY 1, Rank 0	RW	0x000
19:10	PHY_WRLVL_INIT_RATIO_0_1	Write leveling starting ratio[9:0] for Data PHY 0, Rank 1	RW	0x000
9:0	PHY_WRLVL_INIT_RATIO_0_0	Write leveling starting ratio[9:0] for Data PHY 0, Rank 0	RW	0x000

Table 15-317. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_21

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-318. EMIF_EXT_PHY_CONTROL_21_SHADOW

Address Offset	0x0000 02A4		
Physical Address	0x4C00 02A4 0x4D00 02A4	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	RW	0x0000 0000

Table 15-319. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_21_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-320. EMIF_EXT_PHY_CONTROL_22

Address Offset	0x0000 02A8		
Physical Address	0x4C00 02A8 0x4D00 02A8	**Instance**	EMIF1 EMIF2
Description	Write leveling starting ratio. The recommended setting of PHY_WRLVL_INIT_RATIO is half cycle less than total skew between CLK and DQS at the DDR.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_INIT_RATIO_3_0				PHY_WRLVL_INIT_RATIO_2_1												PHY_WRLVL_INIT_RATIO_2_0								PHY_WRLVL_INIT_RATIO_1_1							

Bits	Field Name	Description	Type	Reset
31:28	PHY_WRLVL_INIT_RATIO_3_0	Write leveling starting ratio[3:0] for Data PHY 3, Rank 0	RW	0x0
27:18	PHY_WRLVL_INIT_RATIO_2_1	Write leveling starting ratio[9:0] for Data PHY 2, Rank 1	RW	0x000
17:8	PHY_WRLVL_INIT_RATIO_2_0	Write leveling starting ratio[9:0] for Data PHY 2, Rank 0	RW	0x000
7:0	PHY_WRLVL_INIT_RATIO_1_1	Write leveling starting ratio[9:2] for Data PHY 1, Rank 1	RW	0x00

Table 15-321. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_22

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-322. EMIF_EXT_PHY_CONTROL_22_SHADOW

Address Offset	0x0000 02AC		
Physical Address	0x4C00 02AC 0x4D00 02AC	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	RW	0x0000 0000

Table 15-323. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_22_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-324. EMIF_EXT_PHY_CONTROL_23

Address Offset	0x0000 02B0		
Physical Address	0x4C00 02B0 0x4D00 02B0	**Instance**	EMIF1 EMIF2
Description	Write leveling starting ratio. The recommended setting of PHY_WRLVL_INIT_RATIO is half cycle less than total skew between CLK and DQS at the DDR.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PHY_WRLVL_INIT_RATIO_3_1								PHY_WRLVL_INIT_RATIO_3_0							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x0000
15:6	PHY_WRLVL_INIT_RATIO_3_1	Write leveling starting ratio[9:0] for Data PHY 3, Rank 1	RW	0x000
5:0	PHY_WRLVL_INIT_RATIO_3_0	Write leveling starting ratio[9:4] for Data PHY 3, Rank 0	RW	0x00

Table 15-325. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_23

EMIF Controller

- EMIF Register Summary: [0]

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Table 15-326. EMIF_EXT_PHY_CONTROL_23_SHADOW

Address Offset	0x0000 02B4		
Physical Address	0x4C00 02B4 0x4D00 02B4	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED	Reserved	RW	0x0000 0000

Table 15-327. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_23_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

Table 15-328. EMIF_EXT_PHY_CONTROL_24

Address Offset	0x0000 02B8		
Physical Address	0x4C00 02B8 0x4D00 02B8	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					PHY_RDC_FIFO_RST_ERR_CNT_CLR	PHY_MDLL_UNLOCK_CLEAR	PHY_FIFO_WE_IN_MISALIGNED_CLR	PHY_WRLVL_NUM_OF_DQ0				PHY_GATELVL_NUM_OF_DQ0								

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	RW	0x00 0000
10	PHY_RDC_FIFO_RST_ERR_CNT_CLR	Clear/reset the EMIF_PHY_STATUS_20[15:0] PHY_REG_RDC_FIFO_RST_ERR_CNT_0, EMIF_PHY_STATUS_5[11:0] PHY_REG_RDFIFO_RDPTR_*, and EMIF_PHY_STATUS_5[27:16] PHY_REG_RDFIFO_WRPTR_* status fields and flags. 0: no effect 1: clear	RW	0
9	PHY_MDLL_UNLOCK_CLEAR	Clears the EMIF_PHY_STATUS_20[19:16] PHY_REG_STATUS_MDLL_UNLOCK_STICKY_* status flags. 0: no effect 1: clear	RW	0

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Bits	Field Name	Description	Type	Reset
8	PHY_FIFO_WE_IN_MISALIGNED_CLR	Clears the for EMIF_PHY_STATUS_20[25:20] PHY_REG_FIFO_WE_IN_MISALIGNED_STICKY_* status flags. 0: no effect 1: clear	RW	0
7:4	PHY_WRLVL_NUM_OF_DQ0	This bit field determines the number of samples for dq0_in for each ratio increment by the write leveling FSM. Num_of_iteration = PHY_WRLVL_NUM_OF_DQ0 + 1. The minimum value supported is 3. Default setting of 7 is recommended.	RW	0x7
3:0	PHY_GATELVL_NUM_OF_DQ0	This bit field determines the number of samples for dq0_in for each ratio increment by the Gate Training FSM. Num_of_iteration = PHY_GATELVL_NUM_OF_DQ0 + 1. In LPDDR2 mode, the minimum value supported is 7. The overall minimum value supported is 3. Default setting of 7 is recommended.	RW	0x7

Table 15-329. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_24

EMIF Controller

- EMIF Module Global Initialization: [0] [1]
- EMIF Register Summary: [2]

Table 15-330. EMIF_EXT_PHY_CONTROL_24_SHADOW

Address Offset	0x0000 02BC		
Physical Address	0x4C00 02BC 0x4D00 02BC	**Instance**	EMIF1 EMIF2
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PHY_GATELVL_NUM_OF_DQ0_SHDW							

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	RW	0x00 0000
3:0	PHY_GATELVL_NUM_OF_DQ0_SHDW	Shadow field for PHY_GATELVL_NUM_OF_DQ0	RW	0x0

Table 15-331. Register Call Summary for Register EMIF_EXT_PHY_CONTROL_24_SHADOW

EMIF Controller

- EMIF Register Summary: [0]

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15.4 General-Purpose Memory Controller

15.4.1 GPMC Overview

The general-purpose memory controller (GPMC) is a unified memory controller dedicated to interfacing external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in nonmultiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

The GPMC is also introduced in Section 15.1, *Memory Subsystem Overview*.

15.4.2 GPMC Environment

This section describes the GPMC application fields from an environment point of view (external connections). It describes GPMC connectivity options, and gives three possible interfaces.

15.4.2.1 GPMC Modes

This section shows three GPMC external connections options:

- Figure 15-51 shows a connection between the GPMC and a 16-bit synchronous address/data-multiplexed (or AAD-multiplexed, but this protocol uses fewer address pins) external memory device.
- Figure 15-52 shows a connection between the GPMC and a 16-bit synchronous nonmultiplexed external memory device .
- Figure 15-53 shows a connection between the GPMC and a 8-bit NAND device.

NOTE: The device does not provide the A0 byte address line required for random-byte addressable 8-bit-wide device interfacing (for multiplexed and nonmultiplexed protocol). Hence, an 8-bit device must be connected to the D[7:0]/gpmc_ad[7:0] data bus (rather than D[15:8]/gpmc_ad[15:8]) of the GPMC controller. This limits the use of 8-bit-wide device interfacing to byte-alias access.

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Figure 15-51. GPMC to 16-Bit Address/Data-Multiplexed Memory

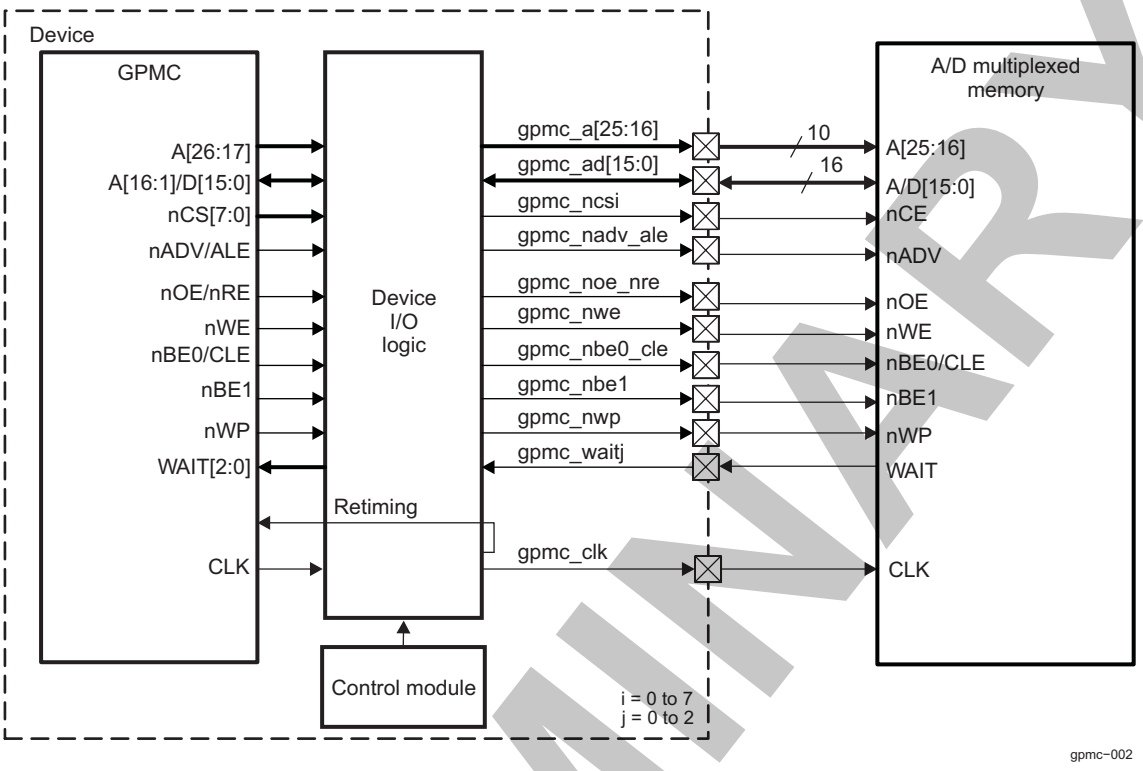

Figure 15-52. GPMC to 16-Bit Nonmultiplexed Memory

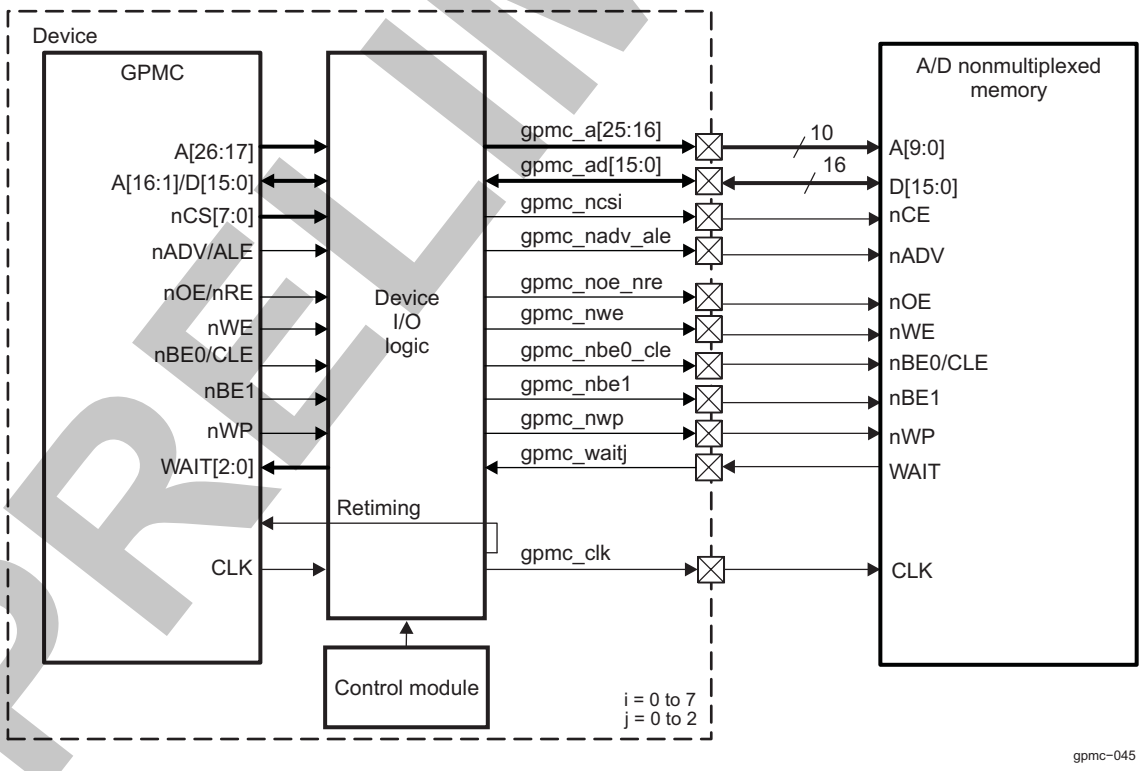

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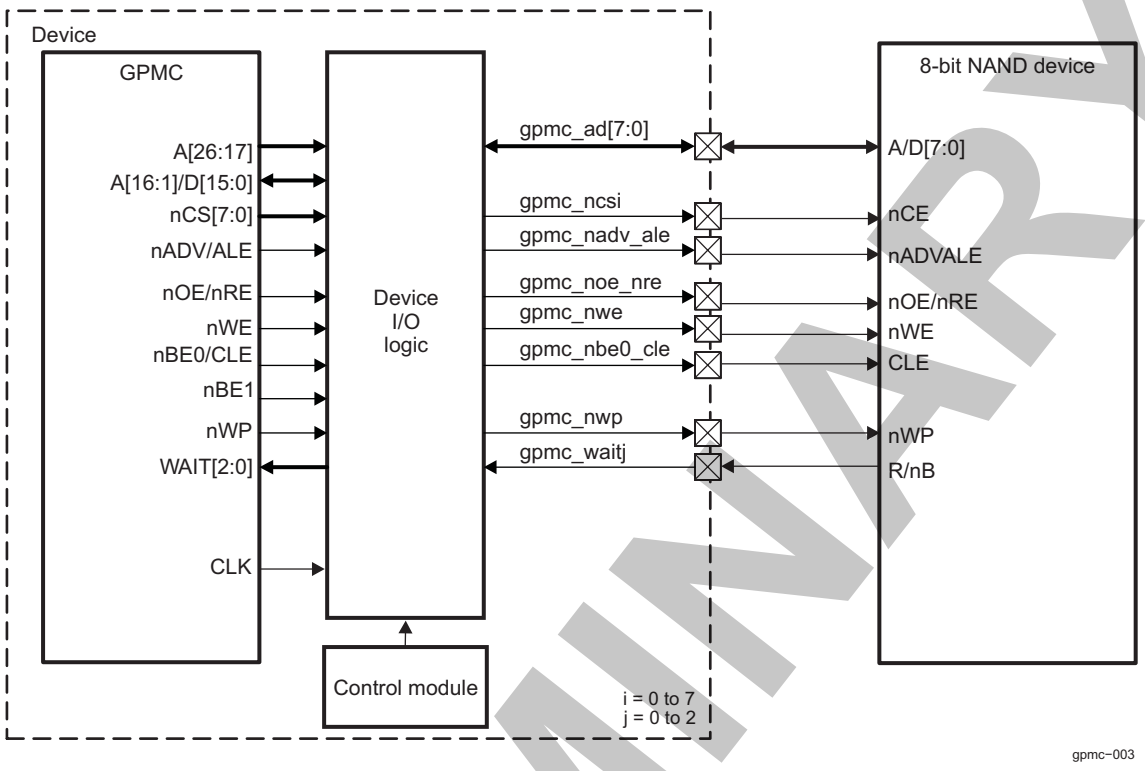
Figure 15-53. GPMC to 8-Bit NAND Device



15.4.2.2 GPMC Signals

Table 15-332 lists the GPMC subsystem input/output (I/O) pins.

Table 15-332. GPMC I/O Description

Pin Name	Device Signal	I/O[1]	Description
A[26:17]	gpmc_a[25:16]	O	Address
A[16:1]/D[15:0]	gpmc_ad[15:0]	I/O	Multiplexed address/data
nCS[7:0]	gpmc_ncs[7:0]	O	Chip-selects (active low)
CLK	gpmc_clk	O[2]	Clock generated for the external memory or device
nADV/ALE	gpmc_nadv_ale	O	Address valid (active low). Also used as address latch enable (active high) for NAND protocol memories.
nOE/nRE	gpmc_noe_nre	O	Output enable (active low). Also used as read enable (active low) for NAND protocol memories.
nWE	gpmc_nwe	O	Write enable (active low)
nBE0/CLE	gpmc_nbe0_cle	O	Lower-byte enable (active low). Also used as command latch enable for NAND protocol memories.
nBE1	gpmc_nbe1	O	Upper-byte enable (active low).
nWP	gpmc_nwp	O	Write protect (active low)
WAIT[2:0]	gpmc_wait[2:0]	I	External wait signal for NOR and NAND protocol memories. The wait signals can be mapped on any of the chip-select.

(1) I = Input; O = Output

(2) This output signal is also used as retiming input. During synchronous operation, the INPUTENABLE bit of the CONTROL_CORE_PAD0_GPMC_NWP_PAD1_GPMC_CLK register must be set to 1.

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NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The control module registers assign the specific function to the device pads. For more information on control module settings, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*.

Table 15-333 shows the use of address and data GPMC controller pins based on the type of external device.

Table 15-333. GPMC Pin Multiplexing Options

GPMC Pin	Multiplexed Address Data 16-Bit Device	Nonmultiplexed Address Data 16-Bit Device With LIMITED-ADDRESS Bit Enabled	16-Bit NAND Device	8-Bit NAND Device
gpmc_a[25]	A26	A10	Not used	Not used
gpmc_a[24]	A25	A9	Not used	Not used
gpmc_a[23]	A24	A8	Not used	Not used
gpmc_a[22]	A23	A7	Not used	Not used
gpmc_a[21]	A22	A6	Not used	Not used
gpmc_a[20]	A21	A5	Not used	Not used
gpmc_a[19]	A20	A4	Not used	Not used
gpmc_a[18]	A19	A3	Not used	Not used
gpmc_a[17]	A18	A2	Not used	Not used
gpmc_a[16]	A17	A1	Not used	Not used
gpmc_ad[15]	A16/D15	D15	D15	Not used
gpmc_ad[14]	A15/D14	D14	D14	Not used
gpmc_ad[13]	A14/D13	D13	D13	Not used
gpmc_ad[12]	A13/D12	D12	D12	Not used
gpmc_ad[11]	A12/D11	D11	D11	Not used
gpmc_ad[10]	A11/D10	D10	D10	Not used
gpmc_ad[9]	A10/D9	D9	D9	Not used
gpmc_ad[8]	A9/D8	D8	D8	Not used
gpmc_ad[7]	A8/D7	D7	D7	D7
gpmc_ad[6]	A7/D6	D6	D6	D6
gpmc_ad[5]	A6/D5	D5	D5	D5
gpmc_ad[4]	A5/D4	D4	D4	D4
gpmc_ad[3]	A4/D3	D3	D3	D3
gpmc_ad[2]	A3/D2	D2	D2	D2
gpmc_ad[1]	A2/D1	D1	D1	D1
gpmc_ad[0]	A1/D0	D0	D0	D0

When using nonmultiplexed memories, it is recommended to enable the GPMC_CONFIG[1] LIMITEDADDRESS bit. This bit forces A[26:11] to 1 on the GPMC I/O side. Thus, only 2 KiB of memory address space is accessible, regardless of the memory size.

With all device types, the GPMC does not drive unnecessary address lines. They stay at their reset value of 0x00.

Address mapping supports address/data-multiplexed 16-bit-wide devices:

- The NOR flash memory controller still supports nonmultiplexed address and data memory devices.
- Multiplexing mode can be selected through the GPMC_CONFIG1_i[9:8] MUXADDDATA bit field (where i = 0 to 7).
- Asynchronous page mode is not supported for multiplexed address and data devices.

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NOTE: The numbering for A (address) starts from 1 instead of 0, such as D (data), because the A0 signal is handled within the GPMC but is not driven to any pad. The signal is relevant only to 8-bit accesses and this configuration is not recommended. If such a memory or device is connected, only every second word in the memory is accessible; that is, each 16-bit-aligned 8-bit word is mapped, but not the non-16-bit aligned ones. Any access to a nonaligned word results in accessing the associated aligned word, at address A1 instead of address A.

15.4.3 GPMC Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

- No STANDBY hardware handshake
- No wake-up request
- One system direct memory access (sDMA) request
- One interrupt request to the microprocessor unit (MPU) interrupt controller (INTC) and to the DSP subsystem
- One clock for functional and interface domains

Figure 15-54 shows GPMC integration.

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Figure 15-54. GPMC Integration

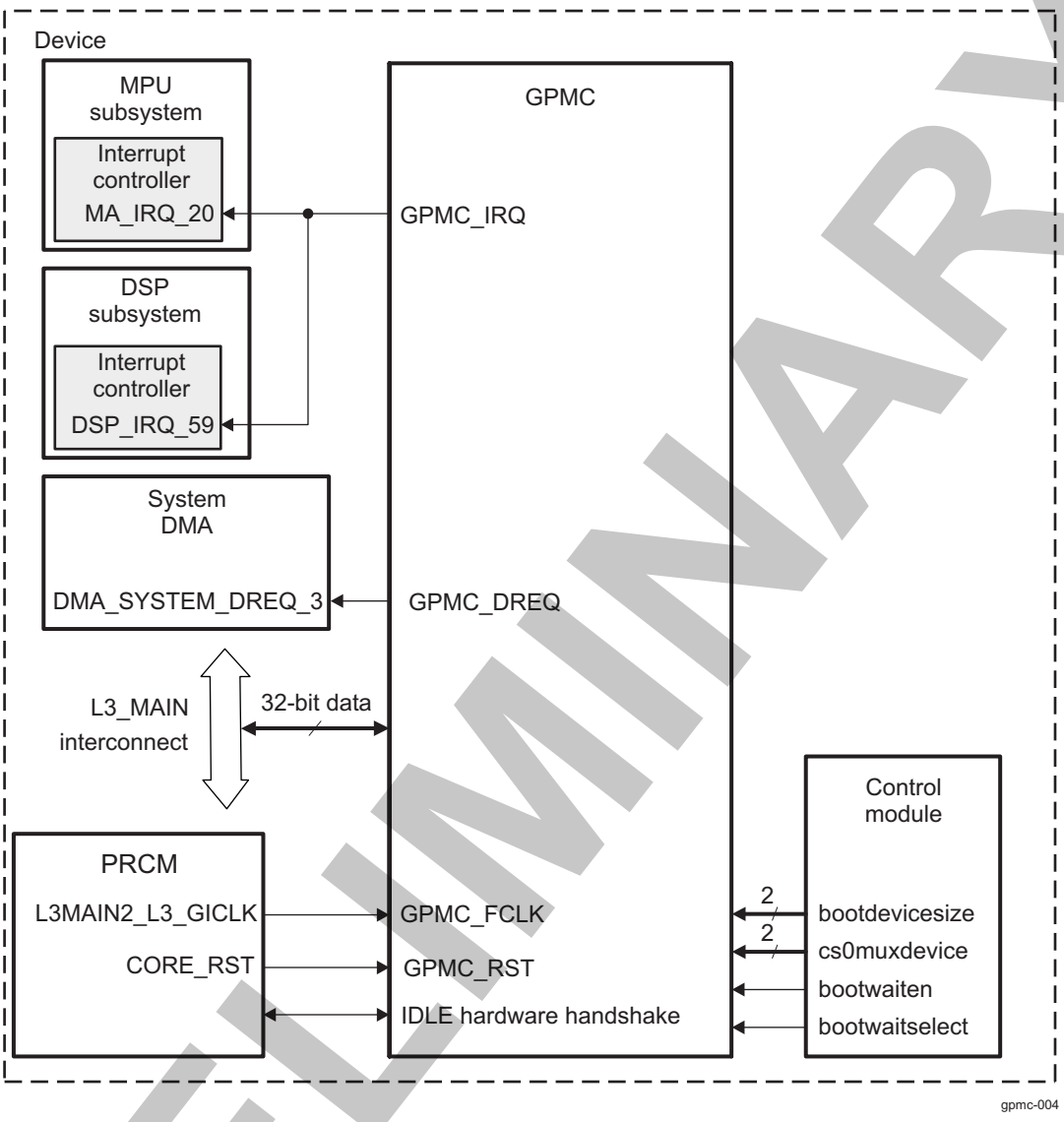

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Table 15-334 through Table 15-336 summarize the integration of the module in the device.

Table 15-334. GPMC Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
GPMC	PD_CORE	No	L3_MAIN

NOTE:

- For the description of the operation performance point (OPP) configuration, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 15-335. GPMC Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
GPMC	GPMC_FCLK	L3MAIN2_L3_GICLK	PRCM	Functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
GPMC	GPMC_RST	CORE_RET_RST	PRCM	GPMC reset

NOTE: For the clock description, see Section 15.4.4.2, *GPMC Clock Configuration*.

Table 15-336. GPMC Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
GPMC	GPMC_IRQ	DSP_IRQ_59	DSP	GPMC interrupt to DSP subsystem
	GPMC_IRQ	MPU_IRQ_20	MPU	GPMC interrupt to MPU subsystem
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
GPMC	GPMC_DREQ	DMA_SYSTEM_DREQ_3	sDMA	GPMC request from prefetch engine to sDMA

NOTE:

- For the description of the interrupt source, see Section 15.4.4.5, *GPMC Interrupt Requests*.
- For the description of the DMA source, see Section 15.4.4.6, *GPMC DMA Requests*.

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15.4.4 GPMC Functional Description

The GPMC basic programming model offers maximum flexibility to support various access protocols for each of the eight configurable chip-selects. Use optimal chip-select settings, based on the characteristics of the external device:

- Different protocols can be selected to support generic asynchronous or synchronous random-access devices (NOR flash, SRAM) or to support specific NAND devices.
- The address and data bus can be multiplexed on the same external bus.
- Read and write access can be independently defined as asynchronous or synchronous.
- System requests (byte, 16-bit word, burst) are performed through single or multiple accesses. External access profiles (single, multiple with optimized burst length, native- or emulated-wrap) are based on external device characteristics (supported protocol, bus width, data buffer size, native-wrap support).
- System burst read or write requests are synchronous-burst (multiple-read or multiple-write). When neither burst nor page mode is supported by external memory or ASIC devices, system burst read or write requests are translated to successive single synchronous or asynchronous accesses (single reads or single writes). 8-bit wide devices are supported only in single synchronous or single asynchronous read or write mode.
- To simulate a programmable internal-wait-state, an external wait pin can be monitored to dynamically control external access at the beginning (initial access time) of and during a burst access.

Each control signal is controlled independently for each chip-select. The internal functional clock of the GPMC (GPMC_FCLK) is used as a time reference to specify the following:

- Read- and write-access duration
- Most GPMC external interface control-signal assertion and deassertion times
- Data-capture time during read access
- External wait-pin monitoring time
- Duration of idle time between accesses, when required

15.4.4.1 GPMC Block Diagram

Figure 15-55 shows the GPMC functional block diagram. The GPMC consists of six blocks:

- L3 interconnect port interface
- Address decoder, GPMC configuration, and chip-select configuration register file
- Access engine
- Prefetch and write-posting engine
- Error correction code engine (ECC)
- External device/memory port interface

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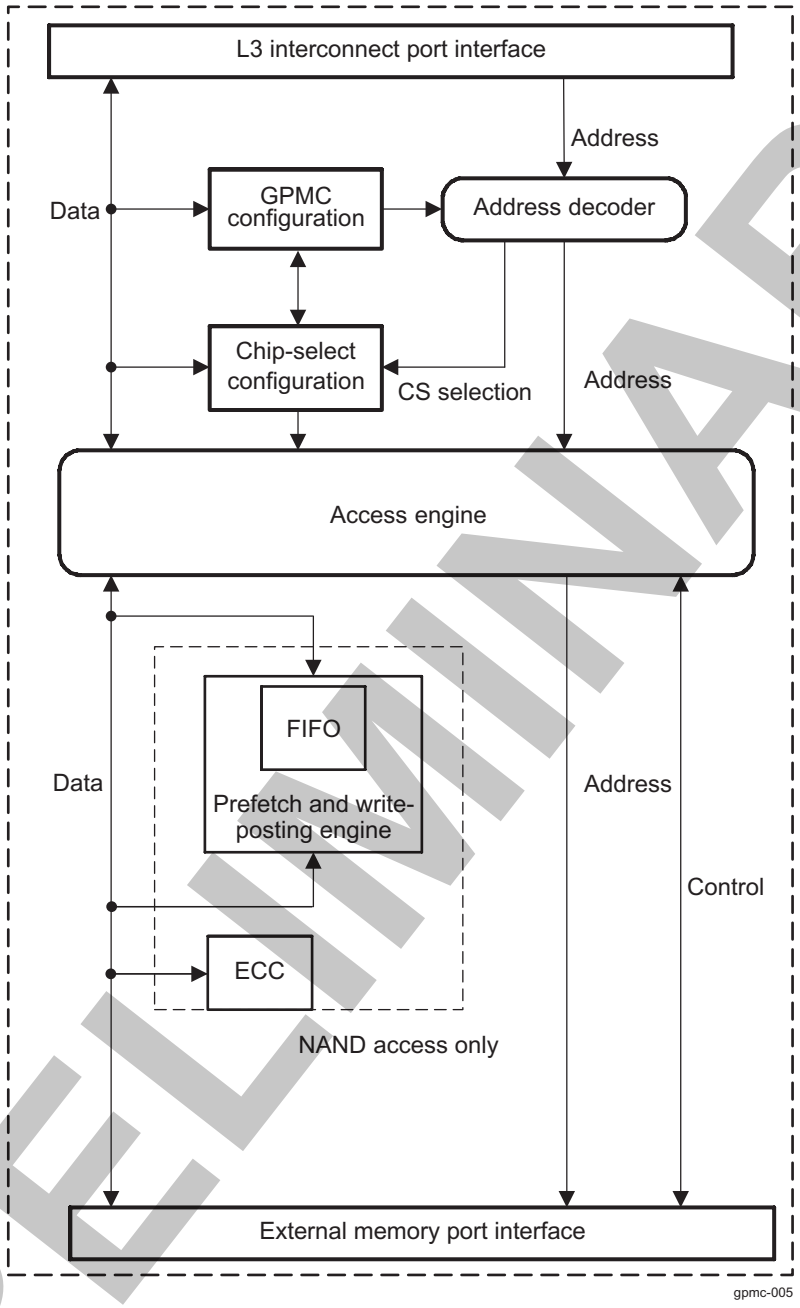
Figure 15-55. GPMC Block Diagram



The GPMC can access various external devices through the L3_MAIN Interconnect. The flexible programming model allows a wide range of attached device types and access schemes.

Based on the programmed configuration bit fields stored in the GPMC registers, the GPMC can generate the timing of all control signals depending on the attached device and access type.

Given the chip-select decoding and its associated configuration registers, the GPMC selects the appropriate control signal timing for the device type.

15.4.4.2 GPMC Clock Configuration

Table 15-337 describes the GPMC clocks.

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Table 15-337. GPMC Clocks

Signal	I/O[1]	Description
GPMC_FCLK	I	Functional and interface clock
gpmc_clk	O	External clock provided to synchronous external memory devices

(1) I = Input; O = Output

The gpmc_clk is generated by the GPMC from the internal GPMC_FCLK clock. The source of the GPMC_FCLK is described in Table 15-335. The gpmc_clk is configured using the GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER bit field (where i = 0 to 7), as shown in Table 15-338.

Table 15-338. gpmc_clk Configuration

Source Clock	GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER	gpmc_clk Generated Clock Provided to External Memory Device
GPMC_FCLK	00	GPMC_FCLK
	01	GPMC_FCLK/2
	10	GPMC_FCLK/3
	11	GPMC_FCLK/4

15.4.4.3 GPMC Software Reset

The GPMC can be reset by software through the GPMC_SYSCONFIG[1] SOFTRESET bit. Setting the bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. Hardware and software resets initialize all GPMC registers and the finite state-machine (FSM) immediately and unconditionally. The GPMC_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. Software must ensure that the software reset completes before performing GPMC operations.

15.4.4.4 GPMC Power Management

GPMC power is supplied by the CORE power domain, and GPMC power management complies with system power-management guidelines.

Table 15-339 describes the power-management features available for the GPMC module.

NOTE:

- For information about source clock gating and sleep/wake-up transitions, see Section 3.1.1.1, *Clock Management*, in Section 3.1.1, *Power, Reset, and Clock Management*.
- For descriptions of the EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.6, *Clock Management Functional Description*, in Section 3.1.1, *Power, Reset, and Clock Management*.

Table 15-339. GPMC Local Power-Management Features

Feature	Registers	Description
Clock autogating	GPMC_SYSCONFIG[0] AUTOIDLE	This bit allows a local power optimization inside the module, by gating the GPMC_FCLK clock upon the internal activity.
Slave idle modes	GPMC_SYSCONFIG[4:3] SIDLEMODE	Force-idle, no-idle and smart-idle wake-up modes are available.
Clock activity	N/A	Feature not available
Master standby modes	N/A	Feature not available
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	N/A	Feature not available

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15.4.4.5 GPMC Interrupt Requests

The GPMC generates one interrupt request (see Figure 15-54).

Table 15-340 lists the event flags, and their mask, that can cause module interrupts.

Table 15-340. GPMC Interrupt Events

Event Flag	Event Mask	Sensitivity	Description
GPMC_IRQSTATUS[10] WAIT2EDGE DETECTIONSTATUS	GPMC_IRQENABLE[10] WAIT2EDGE DETECTIONENABLE	Edge	Wait2 edge detection interrupt: Triggered if a rising or falling edge is detected on the gpmc_wait2 signal. The rising or falling edge detection of Wait2 is selected through the GPMC_CONFIG[10] WAIT2PINPOLARITY bit.
GPMC_IRQSTATUS[9] WAIT1EDGE DETECTIONSTATUS	GPMC_IRQENABLE[9] WAIT1EDGE DETECTIONENABLE	Edge	Wait1 edge detection interrupt: Triggered if a rising or falling edge is detected on the gpmc_wait1 signal. The rising or falling edge detection of Wait1 is selected through the GPMC_CONFIG[9] WAIT1PINPOLARITY bit.
GPMC_IRQSTATUS[8] WAIT0EDGE DETECTIONSTATUS	GPMC_IRQENABLE[8] WAIT0EDGE DETECTIONENABLE	Edge	Wait0 edge detection interrupt: Triggered if a rising or falling edge is detected on the gpmc_wait0 signal. The rising or falling edge detection of Wait0 is selected through the GPMC_CONFIG[8] WAIT0PINPOLARITY bit.
GPMC_IRQSTATUS[1] TERMINAL COUNTSTATUS	GPMC_IRQENABLE[1] TERMINAL COUNTENABLE	Level	Terminal count event: Triggered on prefetch process completion; that is, when the number of currently remaining data to be requested reaches 0
GPMC_IRQSTATUS[0] FIFOEVENTSTATUS	GPMC_IRQENABLE[0] FIFOEVENTENABLE	Level	FIFO event interrupt: Indicates available FIFO levels for write-posting mode and prefetch mode. GPMC_PREFETCH_CONFIG1[2] DMAMODE must be set to 0.

15.4.4.6 GPMC DMA Requests

The GPMC generates one DMA event (see Figure 15-54).

15.4.4.7 L3 Interconnect Interface

The GPMC L3 interconnect interface is a pipelined interface including a 16 × 32-bit word write buffer.

Any system host can issue external access requests through the GPMC.

The device system can issue the following requests through this interface:

- One 8-, 16-, or 32-bit interconnect access (read/write)
- Two incrementing 32-bit interconnect accesses (read/write)
- Two wrapped 32-bit interconnect accesses (read/write)
- Four incrementing 32-bit interconnect accesses (read/write)
- Four wrapped 32-bit interconnect accesses (read/write)
- Eight incrementing 32-bit interconnect accesses (read/write)
- Eight wrapped 32-bit interconnect accesses (read/write)

Only linear burst transactions are supported; interleaved burst transactions are not supported. Only power-of-two-length precise bursts 2 × 32, 4 × 32, 8 × 32, and 16 × 32, with the burst base address aligned on the total burst size, are supported (this limitation applies to incrementing bursts only).

This interface also provides one interrupt and one DMA request line for specific event control.

It is recommended to program the GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH bit field according to the page length of the effective attached device and to enable the GPMC_CONFIG1_i[31] WRAPBURST bit if the attached device supports wrapping burst.

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It is possible, however, to emulate wrapping burst on a nonwrapping memory by providing relevant addresses within the page or by splitting transactions. Bursts larger than the memory page length are chopped into multiple burst transactions. Because of the alignment requirements, a page boundary is never crossed.

15.4.4.8 GPMC Address and Data Bus

The current application supports GPMC connection to NAND devices and to address/data-multiplexed memories or devices. Connection to address/data-nonmultiplexed memories or devices is supported with a limited address range of 2KiB.

Depending on the GPMC configuration of each chip-select, address and data bus lines that are not required for a particular access protocol are not updated (changed from current value) and are not sampled when input (input data bus).

- When the GPMC_CONFIG[1] LIMITEDADDRESS bit is set to 1, A26–A11 are not modified during an external memory access. This limits the memory address space to 2KiB, regardless of the memory size.
- For address/data-multiplexed and AAD-multiplexed NOR devices, the address is multiplexed on the data bus.
- 8-bit-wide NOR devices do not use GPMC I/O: gpmc_ad[15:8] for data (they are used for address if needed).
- 16-bit-wide NAND devices do not use GPMC I/O: gpmc_a[25:16].
- 8-bit-wide NAND devices do not use GPMC I/O: gpmc_a[25:16] and GPMC I/O: gpmc_ad[15:8].

CAUTION

Before accessing a chip-select configured with a nonmultiplexed protocol, set the LIMITEDADDRESS bit control.

15.4.4.8.1 GPMC I/O Configuration Setting

NOTE: In this section and the following sections, the i in GPMC_CONFIGx_i stands for the GPMC chip-select i, where i = 0 to 7.

To select a NAND device, program the following register fields:

- GPMC_CONFIG1_i[11:10] DEVICETYPE = 0b10
- GPMC_CONFIG1_i[9:8] MUXADDDATA = 0b00

To select an address/data-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11:10] DEVICETYPE = 0b00
- GPMC_CONFIG1_i[9:8] MUXADDDATA = 0b10

To select an address/address/data-multiplexed device, program the following register fields:

- GPMC_CONFIG1_i[11:10] DEVICETYPE = 0b00
- GPMC_CONFIG1_i[9:8] MUXADDDATA = 0b01

To select an address/data-nonmultiplexed device (limited to a 2-KiB address range), program the following register fields:

- GPMC_CONFIG1_i[11:10] DEVICETYPE = 0b00
- GPMC_CONFIG1_i[9:8] MUXADDDATA = 0b00
- GPMC_CONFIG[1] LIMITEDADDRESS = 1

NOTE: The GPMC_CONFIG[1] LIMITEDADDRESS bit applies only to address/data-nonmultiplexed devices; it has no effect on other device types (NAND, address/data-multiplexed).

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15.4.4.8.2 GPMC CS0 Default Configuration at Device Reset

To ensure a correct, fast external boot (see Section 28.3.6, *Fast External Booting*, in Section 28.1, *Initialization*) with a GPMC access on device reset, several pins are sampled:

- The sys_boot[3:0] pins (device boundary) define the sequence of interfaces and devices to use for booting. They are sampled by the control module at reset and used later by the device ROM code. For more information, see Section 28.2.4, *Boot Configuration*, in Section 28.1, *Initialization,* .
- Additional pins are used to configure reset values in the GPMC_CONFIG1_i register (where i = 0) as explained in the following and in Table 15-341:
  - The *bootdevicesize* input pin (at the GPMC boundary) defines the size of the attached device on chip-select 0 (CS0) and is used to configure the GPMC_CONFIG1_i[13:12] DEVICESIZE bit field (where i = 0). The BOOT_DEVICE_TYPE signal is propagated from the device control module. Its value is fixed for the device at 0x1 at device reset, which means that only 16-bit memories are supported for booting.
  - The *cs0muxdevice* input pin (at the GPMC boundary) selects whether or not the device attached to CS0 is an address/data-multiplexed device. The input pin is used to configure the GPMC_CONFIG1_i[9:8] MUXADDDATA bit field (where i = 0). The CS0_MUX_DEVICE signal is propagated from the SCM. Its value is fixed for the device at 0x2 at device reset, which means only address/data-multiplexed memories are supported for booting (that is, in a standalone way from memories connected to CS0).
  - The *bootwaiten* input pin (at the GPMC boundary) enables the monitoring on CS0 of the wait pin at device reset release time for read accesses. The input pin is used to configure the GPMC_CONFIG1_i[22] WAITREADMONITORING bit (where i = 0). The BOOT_WAIT_ENABLE signal is propagated from the system control module (SCM). When sys_boot[5:0] = 0b11 1111, the BOOT_WAIT_ENABLE signal is activated, which causes the wait pin to be monitored for read accesses.
  - The *bootwaitselect* input pin selects the WAIT signal at device reset release time between the WAIT0, WAIT1, and WAIT2 input pins. At device reset release time, these three pins have different polarity.

Table 15-341. Boot Control Interface Input Signals Description

Signal Name	Width	Description
bootdevicesize	2	Size of the device attached on CS0 0b00: 8-bit 0b01: 16-bit 0b10: Reserved 0b11: Reserved
cs0muxdevice	2	Multiplexing mode of the device on CS0 0b00: Nonmultiplexed device on CS0 0b01: AAD-multiplexed device on CS0 (address-address-data) 0b10: Address/data-multiplexed device on CS0 0b11: Reserved
bootwaiten	1	Wait monitoring on CS0 at device reset release time for read accesses 0: Wait pin is not monitored 1: Wait pin is monitored
bootwaitselect	1	Selection of the wait pin 0: WAIT0 input pin 1: WAIT1 input pin 2: WAIT2 input pin

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CAUTION

Using the internal boot code, the entire CS0 configuration can be modified before the first CS0 access. For more information, see Section 28.3.7, *Memory Booting*, and Section 28.3.8 , *Image Format*, in Section 28.1, *Initialization*. This modification of internal boot code is necessary for two external devices:

- NAND device attached to CS0
- Nonmultiplexed 2-KiB address range device attached to CS0

At reset time, the device can boot from the internal ROM.

The reset values of the timing control parameters are defined to cope with direct boot on address and data-multiplexed NOR flash devices, nonmultiplexed NOR flash devices, or any asynchronous device with large timing margins, assuming a low GPMC_FCLK frequency (for example, 19.2 MHz) at boot time.

For a multiplexed access, the address 16 low-order bits are presented onto gpmc_ad[15:0], while the high-order bits are presented onto gpmc_a[26:16]. If the external chip interface to the memories uses a 16-bit data bus, the high-order address bits are sampled on the address bus.

The reset values of timing parameters used at boot time are:

- CSONTIME = 1
- CSRDOFFTIME = 16
- ADVONTIME = 4
- ADVRDOFFTIME = 5
- OEONTIME = 6
- OEOFFTIME = 16
- RDACCESSTIME = 15
- RDCYCLETIME = 17

For an AAD-multiplexed access, all address bits are passed onto the data bus using two nADV rising edges. The first rising edge latches the address most-significant bit (MSB) down to bit 17, while the second rising edge latches address bits 16 down to 1. This configuration is only used for 16-bit memories.

The reset values of these timing parameters used at boot time are:

- ADVAADMUXONTIME = 1
- ADVAADMUXRDOFFTIME = 2
- OEAADMUXONTIME = 1
- OEAADMUXRDOFFTIME = 3

15.4.4.9 Address Decoder and Chip-Select Configuration

Addresses are decoded accordingly with the address request of the chip-select and the content of the chip-select base address register file, which includes a set of global GPMC configuration registers and eight sets of chip-select configuration registers.

The GPMC configuration register file is memory-mapped and can be read or written with byte, 16-bit word, or 32-bit word accesses. The register file must be configured as a noncacheable, nonbufferable region to prevent any desynchronization between host execution (write request) and the completion of register configuration (write completed with register updated). Section 15.4.7,*GPMC Register Manual*, provides the GPMC register locations. For the map of GPMC memory locations, see Section 2.2 , *Memory Mapping*.

After the chip-select is configured, the access engine accesses the external device, drives the external interface control signals, and applies the interface protocol based on user-defined timing parameters and settings.

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15.4.4.9.1 Chip-Select Base Address and Region Size

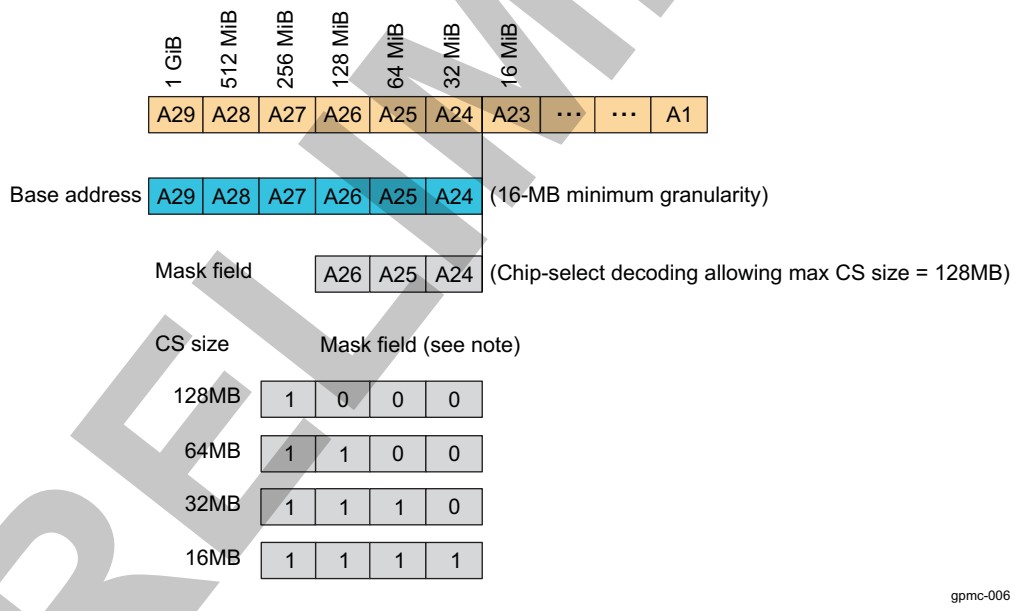
Any external memory or ASIC device attached to the GPMC external interface can be accessed by any device system host within the GPMC 512-MiB contiguous address space. For more information, see Section 2.2, *Memory Mapping*.

The GPMC 512-MiB address space can be divided into a maximum of eight chip-select regions with programmable base address and programmable chip-select size. The chip-select size is programmable from 16MiB to 128MiB (must be a power-of-two) and is defined by the mask field. Attached memory smaller than the programmed chip-select region size is accessed through the entire chip-select region (aliasing).

Each chip-select has a 6-bit base address encoding and 4-bit decoding mask, which must be programmed according to the following rules:

- The programmed chip-select region base address must be aligned on the chip-select region size address boundary and is limited to a power-of-two address value. During access decoding, the value of the register base address is used to compare the address with the address bit line mapping, as shown in Figure 15-56 (with A0 as the device system byte-address line). The base address is programmed through the GPMC_CONFIG7_i[5:0] BASEADDRESS bit field.
- The register mask is used to exclude some address lines from the decoding. A register mask bit field set to 0 suppresses the associated address line from the address comparison (incoming address bit line is don't care). The value of the register mask must be limited to the subsequent value, based on the desired chip-select region size. Any other value has an undefined result. When multiple chip-select regions with overlapping addresses are enabled concurrently, access to these chip-select regions is cancelled and a GPMC access error is posted. The mask field is programmed through the GPMC_CONFIG7_i[11:8] MASKADDRESS bit field.

Figure 15-56. Chip-Select Address Mapping and Decoding Mask



Chip-select configuration (base and mask address or any protocol and timing settings) must be performed while the associated chip-select is disabled through the GPMC_CONFIG7_i[6] CSVALID bit (where i stands for the GPMC chip-select value, 0 to 7). In addition, a chip-select configuration can be disabled only if there is no ongoing access to that chip-select. This requires monitoring the activity of the prefetch or write-posting engine if the engine is active on the chip-select. Also, the write buffer state must be monitored to wait for any posted write completion to the chip-select.

Any access attempted to a nonvalid GPMC address region (CSVALID disabled or address decoding outside a valid chip-select region) is not propagated to the external interface and a GPMC access error is posted. In case of overlapping chip-selects, an error is generated and no access occurs on either chip-select.

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CS0 is the only chip-select region enabled after a power up or GPMC reset.

CAUTION

Although the GPMC interface can drive up to four chip-selects, the frequency specified for this interface is for a specific load. If this load is exceeded, the maximum frequency cannot be reached. One solution is to implement a board with buffers to allow the slowest device to maintain the total load on the lines.

15.4.4.9.2 Access Protocol

15.4.4.9.2.1 Supported Devices

The access protocol of each chip-select can be independently specified through the GPMC_CONFIG1_i[11:10] DEVICETYPE parameter (where i = 0 to 7) for:

- Random-access synchronous or asynchronous memory, such as NOR flash and SRAM
- NAND flash asynchronous devices

NOTE: For more information about the NAND flash GPMC basic programming model and NAND support, see Section 15.4.4.13, *NAND Device Basic Programming Model*, and Section 15.4.4.13.1, *NAND Memory Device in Byte or Word16 Stream Mode*.

15.4.4.9.2.2 Access Size Adaptation and Device Width

Each chip-select can be independently configured through the GPMC_CONFIG1_i[13:12] DEVICESIZE bit field (where i = 0 to 7) to interface with a 16- or 8-bit-wide device. System requests with data width greater than the external device data bus width are split into successive accesses according to the external device data-bus width and little-endian data organization.

NOTE: The device does not provide the A0 byte address line required for random-byte addressable 8-bit-wide device interfacing (for multiplexed and nonmultiplexed protocols). It limits the use of 8-bit-wide device interfacing to byte-alias accesses. This limitation is not applicable to NAND device interfacing (8- or 16-bit-wide devices).

15.4.4.9.2.3 Address/Data-Multiplexing Interface

For random synchronous or asynchronous memory interfacing (DEVICETYPE = 0b00), an address- and data-multiplexing protocol can be selected through the GPMC_CONFIG1_i[9:8] MUXADDDATA bit field (where i = 0 to 7). The nADV signal must be used as the external device address latch control signal. For the associated chip-select configuration, nADV assertion and deassertion time and nOE assertion time must be set to the appropriate value to meet the address latch setup/hold time requirements of the external device. See Section 15.4.3, *GPMC Integration*.

NOTE: This address/data-multiplexing interface is not applicable to NAND device interfacing. NAND devices require a specific address, command, and data-multiplexing protocol. See Section 15.4.4.13, *NAND Device Basic Programming Model*.

15.4.4.9.3 External Signals

15.4.4.9.3.1 Wait Pin Monitoring Control

GPMC access time can be dynamically controlled using an external gpmc_wait pin when the external device access time is not deterministic and cannot be defined and controlled using only the GPMC internal RDACCESSTIME, WRACCESSTIME, and PAGEBURSTACCESSTIME wait-state generator.

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The GPMC features three input wait pins: gpmc_wait2, gpmc_wait1, and gpmc_wait0. These pins allow control of external devices with different wait pin polarity. They also allow the overlap of wait pin assertion from different devices without affecting access to devices for which the wait pin is not asserted.

- The GPMC_CONFIG1_i[17:16] WAITPINSELECT bit field (where i = 0 to 7) selects which input gpmc_wait pin is used for the device attached to the corresponding chip-select.
- The polarity of the wait pin is defined through the WAITxPINPOLARITY bit of the GPMC_CONFIG register. A wait pin configured to be active low means that low level on the WAIT signal indicates that the data is not ready and that the data bus is invalid. When a wait pin is inactive, data is valid.

The GPMC access engine can be configured per chip-select to monitor or not the wait pin of the external memory device, based on the access type: read or write.

- The GPMC_CONFIG1_i[22] WAITREADMONITORING bit defines whether or not the wait pin must be monitored during read accesses.
- The GPMC_CONFIG1_i[21] WAITWRITEMONITORING bit defines whether or not the wait pin must be monitored during write accesses.

The GPMC access engine can be configured to monitor the wait pin of the external memory device asynchronously or synchronously with the GPMC_CLK clock, depending on the access type: synchronous or asynchronous (the GPMC_CONFIG1_i[29] READTYPE and GPMC_CONFIG1_i[27] WRITETYPE bits).

15.4.4.9.3.1.1 Wait Monitoring During Asynchronous Read Access

When wait pin monitoring is enabled for read accesses (WAITREADMONITORING), the effective access time is a logical AND combination of the RDACCESSTIME timing completion and the wait-deasserted state.

During asynchronous read accesses with wait pin monitoring enabled, the wait pin must be at a valid level (asserted or deasserted) for at least two GPMC clock cycles before RDACCESSTIME completes, to ensure correct dynamic access-time control through wait pin monitoring. The advance pipelining of the two GPMC clock cycles is the result of the internal synchronization requirements for the WAIT signal.

In this context, RDACCESSTIME is used as a wait invalid timing window and is set to such a value that the wait pin is at a valid state two GPMC clock cycles before RDACCESSTIME completes.

Similarly, during a multiple-access cycle (for example, asynchronous read page mode), the effective access time is a logical AND combination of PAGEBURSTACCESSTIME timing completion and the wait-deasserted state. Wait monitoring pipelining is also applicable to multiple accesses (access within a page).

- Wait monitored as active freezes the CYCLETIME counter. For an access within a page, when the CYCLETIME counter is by definition in a lock state, wait monitored as asserted extends the current access time in the page. Control signals are kept in their current state. The data bus is considered invalid, and no data are captured during this clock cycle.
- Wait monitored as inactive unfreezes the CYCLETIME counter. For an access within a page, when the CYCLETIME counter is by definition in a lock state, wait monitored as inactive completes the current access time and starts the next access phase in the page. The data bus is considered valid, and data are captured during this clock cycle. In case of a single access or if this was the last access in a multiple-access cycle, all signals are controlled according to their related control timing value and according to the CYCLETIME counter status.

When a delay larger than two GPMC clocks must be observed between wait-pin deactivation time and data valid time (including the required GPMC and the device data setup time), an extra delay can be added between wait-pin deassertion time detection and effective data-capture time and the effective unlock of the CYCLETIME counter. This extra delay can be programmed in the GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME bit field (where i = 0 to 7).

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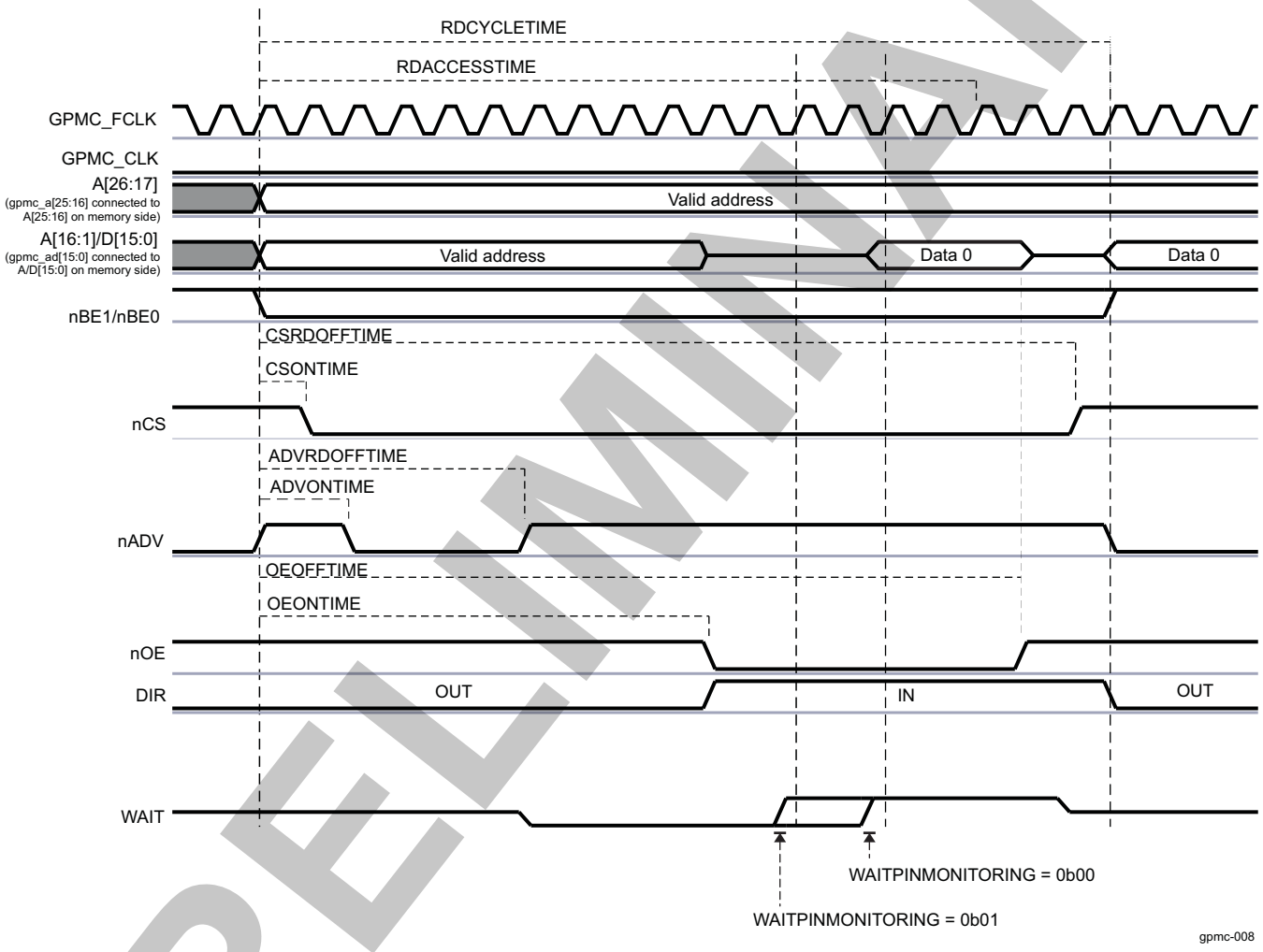
NOTE:

- The WAITMONITORINGTIME parameter does not delay the wait pin active or inactive detection, nor does it modify the two GPMC clocks pipelined detection delay.
- This extra delay is expressed as a number of GPMC_CLK clock cycles, even though the access is defined as asynchronous, and no GPMC_CLK clock is provided to the external device. Still, because GPMCFCLKDIVIDER is used as a divider for the GPMC clock, it must be programmed to define the correct WAITMONITORINGTIME delay.

Figure 15-57 shows wait behavior during an asynchronous single read access.

Figure 15-57. Wait Behavior During an Asynchronous Single Read Access (GPMCFCLKDivider = 1)



NOTE: The WAIT signal is active low. GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME = 0b00, or 0b01.

15.4.4.9.3.1.2 Wait Monitoring During Asynchronous Write Access

When wait pin monitoring is enabled for write accesses (GPMC_CONFIG1_i[21] WAITWRITEMONITORING bit = 0x1), the wait invalid timing window is defined by the WRACCESSTIME field. WRACCESSTIME must be set so that the wait pin is at a valid state two GPMC clock cycles before WRACCESSTIME completes. The advance pipelining of the two GPMC clock cycles is the result of the internal synchronization requirements for the WAIT signal.

- Wait monitored as active freezes the CYCLETIME counter. This informs the GPMC that the data bus is

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not captured by the external device. The control signals are kept in their current state. The data bus still drives the data.

- Wait monitored as inactive unfreezes the CYCLETIME counter. This informs that the data bus is correctly captured by the external device. All signals, including the data bus, are controlled according to their related control timing value and to the CYCLETIME counter status.

When a delay larger than two GPMC clock cycles must be observed between wait-pin deassertion time and the effective data write into the external device (including the required GPMC data setup time and the device data setup time), an extra delay can be added between wait-pin deassertion time detection and effective data write time into the external device and the effective unfreezing of the CYCLETIME counter. This extra delay can be programmed in the GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME bit field (where i = 0 to 7).

NOTE:

- The WAITMONITORINGTIME parameter does not delay the wait pin assertion or deassertion detection, nor does it modify the two GPMC clock cycles pipelined detection delay.
- This extra delay is expressed as a number of GPMC_CLK clock cycles, even though the access is defined as asynchronous, and even though no clock is provided to the external device. Still, because the GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER bit field is used as a divider for the GPMC clock, it must be programmed to define the correct WAITMONITORINGTIME delay.

15.4.4.9.3.1.3 Wait Monitoring During Synchronous Read Access

During synchronous accesses with wait pin monitoring enabled, the wait pin is captured synchronously with GPMC_CLK, using the rising edge of this clock.

The WAIT signal can be programmed to apply to the same clock cycle in which it is captured. Alternatively, it can be sampled one or two GPMC_CLK cycles ahead of the clock cycle to which it applies. This pipelining is applicable to the entire burst access and to all data phases in the burst access. This wait pipelining depth is programmed in the GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME bit field (where i = 0 to 7), and is expressed as a number of GPMC_CLK clock cycles.

In synchronous mode, when wait pin monitoring is enabled (the GPMC_CONFIG1_i[22] WAITREADMONITORING bit), the effective access time is a logical AND combination of the RDACCESSTIME timing completion and the wait-deasserted state detection.

Depending on the programmed value of WAITMONITORINGTIME, the wait pin must be at a valid level, either asserted or deasserted:

- In the same clock cycle the data is valid if WAITMONITORINGTIME = 0 (at RDACCESSTIME completion)
- In the WAITMONITORINGTIME x (GPMCFCLKDIVIDER + 1) GPMC_FCLK clock cycles before RDACCESSTIME completion if WAITMONITORINGTIME is not equal to 0

Similarly, during a multiple-access cycle (burst mode), the effective access time is a logical AND combination of PAGEBURSTACCESSTIME timing completion and the WAIT-INACTIVE state. The wait pipelining-depth programming applies to the whole burst access.

- Wait monitored as active freezes the CYCLETIME counter. For an access within a burst (when the CYCLETIME counter is by definition in a lock state), wait monitored as active extends the current access time in the burst. Control signals are kept in their current state. The data bus is considered invalid, and no data are captured during this clock cycle.
- Wait monitored as inactive unfreezes the CYCLETIME counter. For an access within a burst (when the CYCLETIME counter is by definition in lock state), wait monitored as inactive completes the current access time and starts the next access phase in the burst. The data bus is considered valid, and data are captured during this clock cycle. In a single access or if this was the last access in a multiple-access cycle, all signals are controlled according to their relative control timing value and the CYCLETIME counter status.

Figure 15-58 shows wait behavior during a synchronous read burst access.

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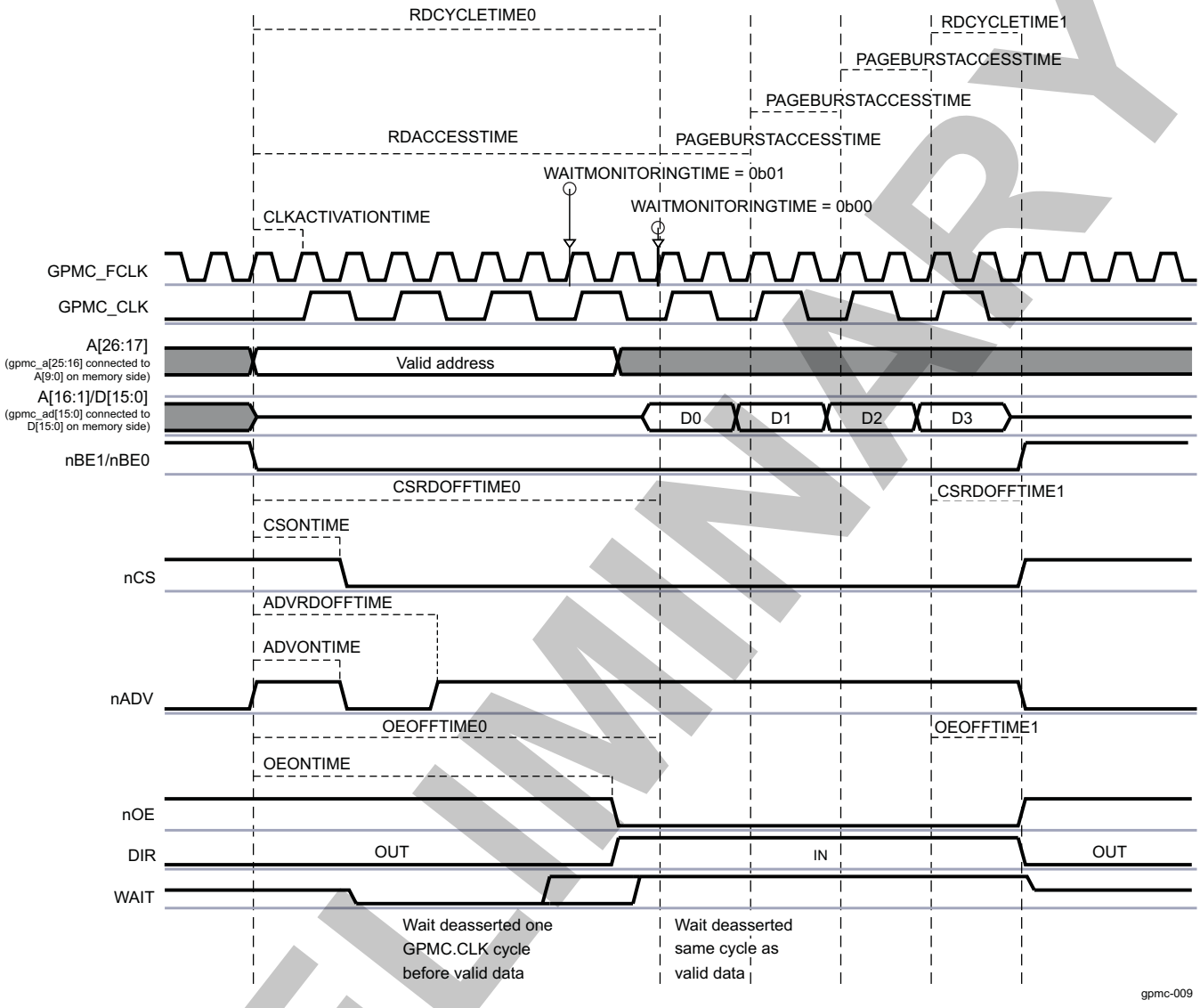
Figure 15-58. Wait Behavior During a Synchronous Read Burst Access



NOTE: The WAIT signal is active low. WAITMONITORINGTIME = 00, 01.

15.4.4.9.3.1.4 Wait Monitoring During Synchronous Write Access

During synchronous accesses with wait pin monitoring enabled (the WAITWRITEMONITORING bit), the wait pin is captured synchronously with GPMC_CLK, using the rising edge of this clock.

If enabled, external wait pin monitoring can be used in combination with WRACCESSTIME to delay the GPMC_CLK capture edge of the effective memory device.

Wait-monitoring pipelining depth is similar to synchronous read access:

- At WRACCESSTIME completion if WAITMONITORINGTIME = 0
- In the WAITMONITORINGTIME x (GPMCFCLKDIVIDER + 1) GPMC_FCLK cycles before WRACCESSTIME completion if WAITMONITORINGTIME is not equal to 0

Wait-monitoring pipelining definition applies to whole burst accesses:

- Wait monitored as active freezes the CYCLETIME counter. For accesses within a burst, when the CYCLETIME counter is by definition in a lock state, wait monitored as active indicates that the data

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bus is not being captured by the external device. Control signals are kept in their current state. The data bus is kept in its current state.

- Wait monitored as inactive unfreezes the CYCLETIME counter. For accesses within a burst, when the CYCLETIME counter is by definition in a lock state, wait monitored as inactive indicates the effective data capture of the bus by the external device and starts the next access of the burst. In case of a single access or if this was the last access in a multiple access cycle, all signals, including the data bus, are controlled according to their related control timing value and the CYCLETIME counter status.

NOTE: Wait monitoring is supported for all configurations except GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME = 0x0 (where i = 0 to 7) for write bursts with a clock divider of 1 or 2 (the GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER bit field is equal to 0x0 or 0x1, respectively).

15.4.4.9.3.1.5 Wait With NAND Device

For information about the use of the wait pin for communication with a NAND flash external device, see Section 15.4.4.13.2, *NAND Device-Ready Pin*.

15.4.4.9.3.1.6 Idle Cycle Control Between Successive Accesses

15.4.4.9.3.1.6.1 Bus Turnaround (BUSTURNAROUND)

To prevent data-bus contention, an access that follows a read access to a slow memory/device must be delayed (in other words, control the nCS/nOE deassertion to data bus in high-impedance delay).

The bus turnaround is a time-out counter starting after nCS or nOE deassertion time, whichever occurs first, and delays the next access start-cycle time. The counter is programmed through the GPMC_CONFIG6_i[3:0] BUSTURNAROUND bit field (where i = 0 to 7).

After a read access to a chip-select with a nonzero BUSTURNAROUND, the next access is delayed until the BUSTURNAROUND delay completes, if the next access is one of the following:

- A write access to any chip-select (the same or different chip-select from which the data was read)
- A read access to a different chip-select than the chip-select from which the data was read access
- A read or write access to a chip-select associated with an address/data-multiplexed device

NOTE: Bus keeping starts after bus turnaround completion so that DIR changes from IN to OUT after bus turnaround. The bus does not have enough time to go into high-impedance even though it can be driven with the same value before bus turnaround timing.

BUSTURNAROUND delay runs in parallel with GPMC_CONFIG6_i[3:0] CYCLE2CYCLEDELAY bi field delays. BUSTURNAROUND is a timing parameter for the ending chip-select access, while CYCLE2CYCLEDELAY is a timing parameter for the following chip-select access. The effective minimum delay between successive accesses is driven by these delay timing parameters and by the access type of the following access (see Figure 15-59 through Figure 15-61).

Another way to prevent bus contention is to define an earlier nCS or nOE deassertion time for slow devices or to extend the value of RDCYCLETIME. Doing this prevents bus contention, but it also affects all accesses of this specific chip-select.

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Figure 15-59. Read-to-Read for an Address-Data Multiplexed Device, on Different Chip-Select, Without Bus Turnaround (nCS Attached to a Fast Device)

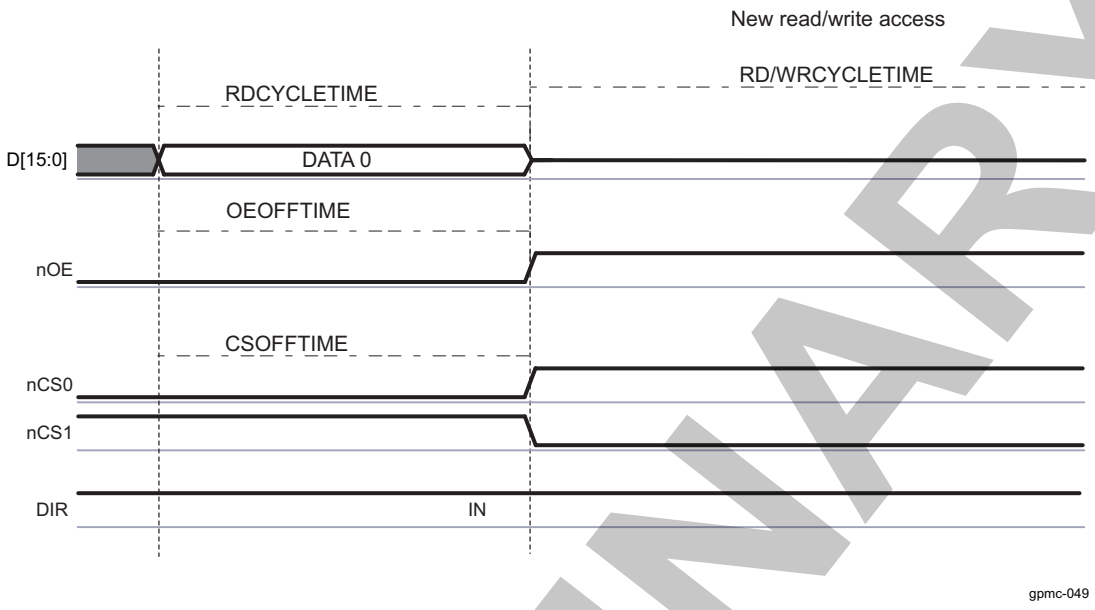

Figure 15-60. Read- to-Read/Write for an Address-Data Multiplexed Device, on Different Chip-Select, With Bus Turnaround

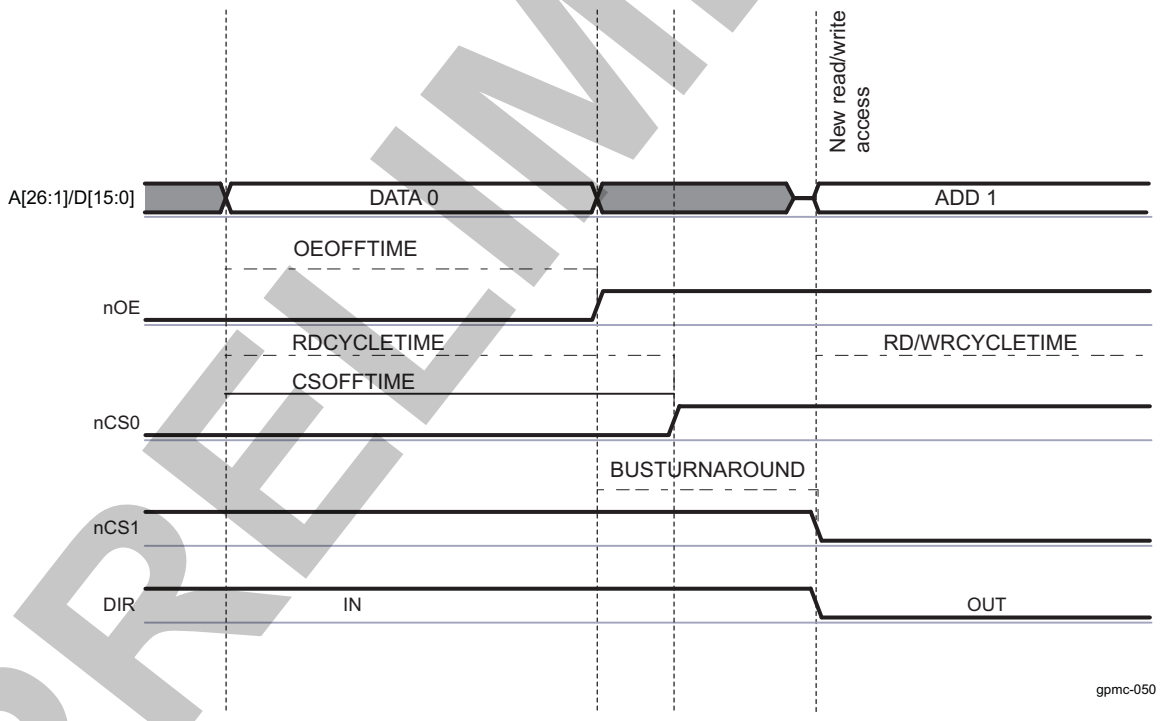

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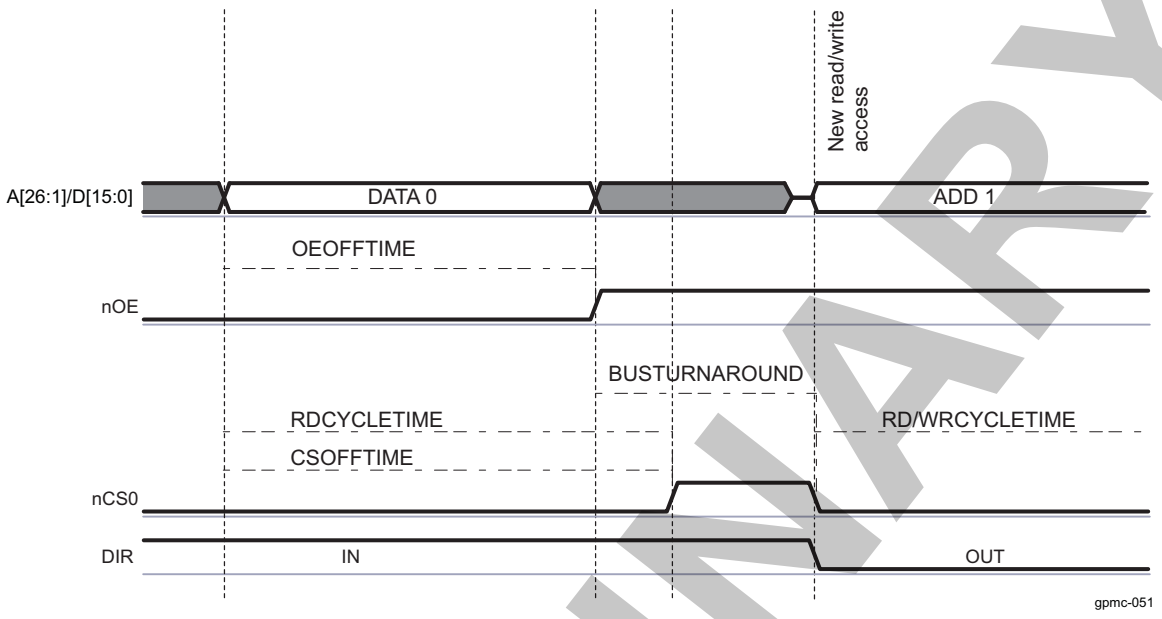
Figure 15-61. Read-to-Read/Write for a Address-Data or AAD-Multiplexed Device, on Same Chip-Select, With Bus Turnaround



15.4.4.9.3.1.6.2 Idle Cycles Between Accesses to Same Chip-Select (CYCLE2CYCLESAMECSEN, CYCLE2CYCLEDELAY)

Some devices require a minimum chip-select signal inactive time between accesses. The GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN bit (where i = 0 to 7) enables insertion of a minimum number of GPMC_FCLK cycles, defined by the GPMC_CONFIG6_i[11:8] CYCLE2CYCLEDELAY bit field, between successive accesses of any type (read or write) to the same chip-select.

If CYCLE2CYCLESAMECSEN is enabled, any subsequent access to the same chip-select is delayed until its CYCLE2CYCLEDELAY completes. The CYCLE2CYCLEDELAY counter starts when CSRDOFFTIME/CSWROFFTIME completes.

The same applies to successive accesses occurring during 32-bit word or burst accesses split into successive single accesses when the single-access mode is used (GPMC_CONFIG1_i[30] READMULTIPLE = 0 or GPMC_CONFIG1_i[28] WRITEMULTIPLE = 0).

All control signals (CS, ADV#/ALE, BE0#/CLE, WE#, and GPMC.CLK) are kept inactive (ADV#/ALE, BE0#/CLE, and GPMC.CLK at low level; and CS, OE#/RE, and WE at high level) during the idle GPMC.FCLK cycles. This prevents back-to-back accesses to the same chip-select without idle cycles between accesses.

15.4.4.9.3.1.6.3 Idle Cycles Between Accesses to Different Chip-Select (CYCLE2CYCLEDIFFCSEN, CYCLE2CYCLEDELAY)

Because of the pipelined behavior of the system, successive accesses to different chip-selects can occur back-to-back with no idle cycles between accesses. Depending on the control signals (nCS, nADV/ALE, nBE0/CLE, nOE/RE, nWE) assertion and deassertion timing parameters and on the device timing parameters, the assertion times of some control signals may overlap between the successive accesses to a different chip-select. Similarly, some control signals (WE, OE/RE) may not respect required transition times.

To work around overlapping and to observe the required control-signal transitions, a minimum of CYCLE2CYCLEDELAY inactive cycles is inserted between the access being initiated to this chip-select and the previous access ending for a different chip-select. This applies to any type of access (read or write).

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If the GPMC_CONFIG6_i[6] CYCLE2CYCLEDIFFCSEN bit is enabled, the chip-select access is delayed until CYCLE2CYCLEDELAY cycles have expired since the end of a previous access to a different chip-select. CYCLE2CYCLEDELAY count starts at CSRDOFFTIME/CSWROFFTIME completion. All control signals are kept inactive during the idle GPMC_FCLK cycles.

NOTE: CYCLE2CYCLESAMECSEN and CYCLE2CYCLEDIFFCSEN must be set in the GPMC_CONFIG6_i registers to get idle cycles inserted between accesses on this chip-select and after accesses to a different chip-select, respectively.

The CYCLE2CYCLEDELAY delay runs in parallel with the BUSTURNAROUND delay. The BUSTURNAROUND is a timing parameter defined for the ending chip-select access, whereas CYCLE2CYCLEDELAY is a timing parameter defined for the starting chip-select access. The effective minimum delay between successive accesses is based on the larger delay timing parameter and on access type combination, because bus turnaround does not apply to all access types. For more information about bus turnaround, see Section 15.4.4.9.3.1.6.1, *Bus Turnaround (BUSTURNAROUND)*.

Table 15-342 describes the configuration required for idle cycle insertion.

Table 15-342. Idle Cycle Insertion Configuration

1st Access Type	BUSTURNAROUND Timing Parameter	Second Access Type	Chip-Select	Add/Data Multiplexed	CYCLE2CYCLESAMECSEN Parameter	CYCLE2CYCLEDIFFCSEN Parameter	Idle Cycle Insertion Between the Two Accesses
R/W	= 0	R/W	Any	Any	0	x	No idle cycles are inserted if the two accesses are well pipelined.
R	> 0	R	Same	Nonmuxed	x	0	No idle cycles are inserted if the two accesses are well pipelined.
R	> 0	R	Different	Nonmuxed	0	0	BUSTURNAROUND cycles are inserted.
R	> 0	R/W	Any	Muxed	0	0	BUSTURNAROUND cycles are inserted.
R	> 0	W	Any	Any	0	0	BUSTURNAROUND cycles are inserted.
W	> 0	R/W	Any	Any	0	0	No idle cycles are inserted if the two accesses are well pipelined.
R/W	= 0	R/W	Same	Any	1	x	CYCLE2CYCLEDELAY cycles are inserted.
R/W	= 0	R/W	Different	Any	x	1	CYCLE2CYCLEDELAY cycles are inserted.
R/W	> 0	R/W	Same	Any	1	x	CYCLE2CYCLEDELAY cycles are inserted. If BTA idle cycles already apply on these two back-to-back accesses, the effective delay is max (BUSTURNAROUND, CYCLE2CYCLEDELAY).
R/W	> 0	R/W	Different	Any	x	1	CYCLE2CYCLEDELAY cycles are inserted. If BTA idle cycles already apply on these two back-to-back accesses, the effective delay is maximum (BUSTURNAROUND, CYCLE2CYCLEDELAY).

15.4.4.9.3.1.7 Slow Device Support (TIMEPARAGRANULARITY Parameter)

All access-timing parameters can be multiplied by 2 by setting the GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit (where i stands for the GPMC chip-select value, 0 to 7). Increasing all access timing parameters allows support of slow devices.

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15.4.4.9.3.2 gpmc_io_dir Pin

The gpmc_io_dir pin is used to control I/O direction on the GPMC data bus gpmc_ad[15:0]. Depending on top-level pad multiplexing, this signal can be output and used externally to the device, if required.

The gpmc_io_dir pin is low during transmit (OUT) and high during receive (IN).

For write accesses, the gpmc_io_dir pin stays OUT from start-cycle time to end-cycle time.

For read accesses, the gpmc_io_dir pin goes from OUT-to-IN at nOE assertion time and stays IN until:

- BUSTURNAROUND is enabled:
  - The gpmc_io_dir pin goes from IN-to-OUT at end-cycle time plus programmable bus turnaround time.
- BUSTURNAROUND is disabled:
  - After an asynchronous read access, the gpmc_io_dir pin goes from IN-to-OUT at RDACCESSTIME + 1 GPMC_FCLK cycle or when RDCYCLETIME completes, whichever occurs last.
  - After a synchronous read access, the gpmc_io_dir pin goes from IN-to-OUT at RDACCESSTIME + 2 GPMC_FCLK cycles or when RDCYCLETIME completes, whichever occurs last.

Because of the bus-keeping feature of the GPMC, after a read or write access and with no other accesses pending, the default value of the gpmc_io_dir pin is OUT (see Section 15.4.4.10.10, *Bus Keeping Support*).

In nonmultiplexed devices, the gpmc_io_dir pin stays IN between two successive read accesses to prevent unnecessary toggling (nonmultiplexed 16-bit-wide device support is limited to 2KiB).

15.4.4.9.3.3 Reset

No reset signal is sent to the external memory device by the GPMC. For more information about external-device reset, see Section 3.1.1, *Power, Reset, and Clock Management*.

The PRCM module provides an input pin, global_rst_n, to the GPMC:

- The global_rst_n pin is activated during device warm reset and cold reset.
- The global_rst_n pin initializes the internal state-machine and the internal configuration registers.

15.4.4.9.3.4 Write Protect Signal (nWP)

When connected to the attached memory device, the write protect signal can enable or disable the lockdown function of the attached memory.

The gpmc_nwp output pin value is controlled through the GPMC_CONFIG[4] WRITEPROTECT bit, which is common to all chip-selects.

15.4.4.9.3.5 Byte Enable (nBE1/nBE0)

Byte enable signals (nBE1/nBE0) are:

- Valid (asserted or nonasserted according to the incoming system request) from access start to access completion for asynchronous and synchronous single accesses
- Asserted low from access start to access completion for asynchronous and synchronous multiple read accesses
- Valid (asserted or nonasserted, according to the incoming system request) synchronously to each written data for synchronous multiple write accesses

15.4.4.9.4 Error Handling

When an error occurs in the GPMC, the error information is stored in the GPMC_ERR_TYPE register and the address of the illegal access is stored in the GPMC_ERR_ADDRESS register. The GPMC keeps only the first error abort information until the GPMC_ERR_TYPE register is reset. Subsequent accesses that cause errors are not logged until the error is cleared by hardware with the GPMC_ERR_TYPE[0] ERRORVALID bit.

- ERRORNOTSUPPADD occurs when an incoming system request address decoding does not match

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any valid chip-select region, or if two chip-select regions are defined as overlapped, or if a register file access is tried outside the valid address range of 1KiB.

- ERRORNOTSUPPMCMD occurs when an unsupported command request is decoded at the L3 interconnect interface.
- ERRORTIMEOUT: A time-out mechanism prevents the system from hanging. The start value of the 9-bit time-out counter is defined in the GPMC_TIMEOUT_CONTROL register and enabled with the GPMC_TIMEOUT_CONTROL[0] TIMEOUTENABLE bit. When enabled, the counter starts at start-cycle time until it reaches 0 and data is not responded to from memory, and then a time-out error occurs. When data are sent from memory, this counter is reset to its start value. With multiple accesses (asynchronous page mode or synchronous burst mode), the counter is reset to its start value for each data access within the burst.

The GPMC does not generate interrupts on these errors. True abort to the MPU or interrupt generation is handled at interconnect level.

15.4.4.10 Timing Setting

The GPMC offers maximum flexibility to support various access protocols. Most of the timing parameters of the protocol access used by the GPMC to communicate with attached memories or devices are programmable on a chip-select basis. Assertion and deassertion times of control signals are defined to match the attached memory or device timing specifications and to get maximum performance during accesses. For more information about GPMC_CLK and GPMC_FCLK see Section 15.4.4.10.6, *GPMC_CLK*.

NOTE: In the following sections, the start access time refers to the time at which the access begins.

15.4.4.10.1 Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME)

The GPMC_CONFIG5_i[4:0] RDCYCLETIME and GPMC_CONFIG5_i[12:8] WRCYCLETIME bit fields (where i = 0 to 7) define the address bus and byte-enable valid times for read and write accesses. To ensure a correct duty cycle of GPMC_CLK between accesses, RDCYCLETIME and WRCYCLETIME are expressed in GPMC_FCLK cycles and must be multiples of the GPMC_CLK cycle. The RDCYCLETIME and WRCYCLETIME bit fields can be set with a granularity of 1 or 2 through the GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit.

When RDCYCLETIME or WRCYCLETIME completes, if they are not already deasserted, all control signals (nCS, nADV/ALE, nOE/RE, nWE, and BE0/CLE) are deasserted to their reset values, regardless of their deassertion time parameters.

An exception to this forced deassertion occurs when a pipelined request to the same chip-select or to a different chip-select is pending. In such a case, it is not necessary to deassert a control signal with deassertion time parameters equal to the cycle-time parameter. This exception to forced deassertion prevents any unnecessary glitches. This requirement also applies to BE signals, thus avoiding an unnecessary BE glitch transition when pipelining requests.

NOTE: All control signals (CS, ADV#/ALE, BE0#/CLE, WE#, and GPMC.CLK) are kept inactive (ADV#/ALE, BE0#/CLE, and GPMC.CLK at low level; and CS, OE#/RE, and WE at high level) during the idle GPMC.FCLK cycles.

If no inactive cycles are required between successive accesses to the same chip-select or a different chip-select (GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN = 0 or GPMC_CONFIG6_i[6] CYCLE2CYCLEDIFFCSEN = 0, where i = 0 to 7), and if assertion-time parameters associated with the pipelined access are equal to 0, asserted control signals (nCS, nADV/ALE, nBE0/CLE, nWE, and nOE/RE) are kept asserted. This applies to any read/write to read/write access combination.

If inactive cycles are inserted between successive accesses (that is, CYCLE2CYCLESAMECSEN = 1 or CYCLE2CYCLEDIFFCSEN = 1), the control signals are forced to their respective default reset values for the number of GPMC_FCLK cycles defined in CYCLE2CYCLEDELAY.

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15.4.4.10.2 nCS: Chip-Select Signal Control Assertion/Deassertion Time (CSONTIME / CSRDOFFTIME / CSWROFFTIME / CSEXTRADELAY)

The GPMC_CONFIG2_i[3:0] CSONTIME bit field (where i = 0 to 7) defines the nCS signal-assertion time relative to the start access time. It is common for read and write accesses.

The GPMC_CONFIG2_i[12:8] CSRDOFFTIME (read access) and GPMC_CONFIG2_i[20:16] CSWROFFTIME (write access) bit fields define the nCS signal deassertion time relative to start access time.

The CSONTIME, CSRDOFFTIME, and CSWROFFTIME parameters apply to synchronous and asynchronous modes. CSONTIME can be used to control an address and byte-enable setup time before chip-select assertion. CSRDOFFTIME and CSWROFFTIME can be used to control an address and byte-enable hold time after chip-select deassertion.

nCS signal transitions, as controlled through CSONTIME, CSRDOFFTIME, and CSWROFFTIME, can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG2_i[7] CSEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on the nCS assertion and deassertion time to ensure proper setup and hold time relative to GPMC_CLK. CSEXTRADELAY is especially useful in configurations where GPMC_CLK and GPMC_FCLK have the same frequency, but it can also be used for all GPMC configurations. If enabled, CSEXTRADELAY applies to all parameters that control nCS transitions.

The CSEXTRADELAY bit must be used carefully to avoid control signal overlap between successive accesses to different chip-selects. This implies the need to program the RDCYCLETIME and WRCYCLETIME bit fields to be greater than the nCS signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

15.4.4.10.3 nADV/ALE: Address Valid/Address Latch Enable Signal Control Assertion/Deassertion Time (ADVONTIME / ADVRDOFFTIME / ADVWROFFTIME / ADVEXTRADELAY/ADVAADMUXONTIME/ADVAADMUXRDOFFTIME/ADVAADMUXWROFFTIME)

The GPMC_CONFIG3_i[3:0] ADVONTIME field (where i = 0 to 7) defines the nADV/ALE signal-assertion time relative to start access time. It is common to read and write accesses.

The GPMC_CONFIG3_i[12:8] ADVRDOFFTIME (read access) and GPMC_CONFIG3_i[20:16] ADVWROFFTIME (write access) bit fields define the nADV/ALE signal-deassertion time relative to start access time.

ADVONTIME can be used to control an address and byte-enable valid setup time control before nADV/ALE assertion. ADVRDOFFTIME and ADVWROFFTIME can be used to control an address and byte-enable valid hold time control after nADV/ALE deassertion. ADVRDOFFTIME and ADVWROFFTIME apply to synchronous and asynchronous modes.

The nADV/ALE signal transitions as controlled through ADVONTIME, ADVRDOFFTIME, and ADVWROFFTIME can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG3_i[7] ADVEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on nADV/ALE assertion and deassertion time to ensure proper setup and hold time relative to GPMC_CLK. The ADVEXTRADELAY configuration parameter is especially useful in configurations where GPMC_CLK and GPMC_FCLK have the same frequency, but can be used for all GPMC configurations. If enabled, ADVEXTRADELAY applies to all parameters controlling nADV/ALE transitions.

ADVEXTRADELAY must be used carefully to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program the RDCYCLETIME and WRCYCLETIME bit fields to be greater than nADV/ALE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME, GPMC_CONFIG3_i[26:24] ADVAADMUXRDOFFTIME, and GPMC_CONFIG3_i[30:28] ADVAADMUXWROFFTIME parameters have the same functions as ADVONTIME, ADVRDOFFTIME, and ADVWROFFTIME, but apply to the first address phase in the AAD-multiplexed protocol. The user must ensure that ADVAADMUXxxOFFTIME is programmed to a value less than or equal to ADVxxOFFTIME. Functionality in AAD-multiplexed mode is undefined if the settings do not comply with this requirement. ADVAADMUXxxOFFTIME can be programmed to the same value as ADVONTIME if no high nADV pulse is needed between the two AAD-multiplexed address phases, which is the typical case in synchronous mode. In this configuration, nADV is kept low until it reaches the correct ADVxxOFFTIME.

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For more information about the use of ADVONTIME, ADVRDOFFTIME, ADVWROFFTIME, and ADVAADMUXRDOFFTIME and ADVAADMUXWROFFTIME for command latch enable (CLE) and address latch enable (ALE) use for a NAND flash interface, see Section 15.4.4.13, *NAND Access Description*.

15.4.4.10.4 nOE/nRE: Output Enable/Read Enable Signal Control Assertion/Deassertion Time (OEONTIME / OEOFFTIME / OEEXTRADELAY / OEAADMUXONTIME / OEAADMUXOFFTIME)

The GPMC_CONFIG4_i[3:0] OEONTIME bit field (where i = 0 to 7) defines the nOE/nRE signal assertion time relative to start access time. It applies only to read accesses.

The GPMC_CONFIG4_i[12:8] OEOFFTIME bit field defines the nOE/nRE signal deassertion time relative to start access time. It applies only to read accesses. nOE/nRE is not asserted during a write cycle.

The OEONTIME, OEOFFTIME, OEAADMUXONTIME, and OEAADMUXOFFTIME parameters apply to synchronous and asynchronous modes. OEONTIME can be used to control an address and byte enable valid setup time control before nOE/nRE assertion. OEOFFTIME can be used to control an address and byte-enable valid hold time control after nOE/nRE assertion.

The OEAADMUXONTIME and OEAADMUXOFFTIME parameters have the same functions as OEONTIME and OEOFFTIME, but apply to the first OE assertion in the AAD-multiplexed protocol for a read phase, or to the only OE assertion for a write phase. The user mut ensure that OEAADMUXOFFTIME is programmed to a value less than OEONTIME. Functionality in AAD-multiplexed mode is undefined if the settings do not comply with this requirement. OEAADMUXOFFTIME must never be equal to OEONTIME because the AAD-multiplexed protocol requires a second address phase with the nOE signal deasserted before nOE can be asserted again to define a read command.

The nOE/RE signal transitions as controlled through OEONTIME, OEOFFTIME, OEAADMUXONTIME, and OEAADMUXOFFTIME can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG4_i[7] OEEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on the nOE/RE assertion and deassertion time to ensure proper setup and hold time relative to GPMC_CLK. If enabled, OEEXTRADELAY applies to all parameters controlling nOE/nRE transitions.

OEEXTRADELAY must be used carefully, to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program RDCYCLETIME and WRCYCLETIME to be greater than the nOE/RE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

NOTE: When the GPMC generates a read access to an address-/data-multiplexed device, it drives the address bus until nOE assertion time.

15.4.4.10.5 nWE: Write Enable Signal Control Assertion/Deassertion Time (WEONTIME / WEOFFTIME / WEEXTRADELAY)

The GPMC_CONFIG4_i[19:16] WEONTIME bit field (where i = 0 to 7) defines the nWE signal-assertion time relative to start access time. The GPMC_CONFIG4_i[28:24] WEOFFTIME bit field defines the nWE signal-deassertion time relative to start access time. These bit fields apply only to write accesses. nWE is not asserted during a read cycle.

WEONTIME can be used to control an address and byte-enable valid setup time control before nWE assertion. WEOFFTIME can be used to control an address and byte-enable valid hold time control after nWE assertion.

nWE signal transitions as controlled through WEONTIME, and WEOFFTIME can be delayed by a half-GPMC_FCLK period by enabling the GPMC_CONFIG4_i[23] WEEXTRADELAY bit. This half-GPMC_FCLK period provides more granularity on nWE assertion and deassertion time to ensure proper setup and hold time relative to GPMC_CLK. If enabled, WEEXTRADELAY applies to all parameters controlling nWE transitions.

The WEEXTRADELAY bit must be used carefully to avoid control-signal overlap between successive accesses to different chip-selects. This implies the need to program the WRCYCLETIME bit field to be greater than the nWE signal-deassertion time, including the extra half-GPMC_FCLK-period delay.

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15.4.4.10.6 GPMC_CLK

GPMC_CLK is the external clock provided to the attached synchronous memory or device.

- The GPMC_CLK clock frequency is the GPMC_FCLK functional clock frequency divided by 1, 2, 3, or 4, depending on the GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER bit field (where i = 0 to 7), with a guaranteed 50-percent duty cycle.
- The GPMC_CLK clock is activated only when the access in progress is defined as synchronous (read or write access).
- The GPMC_CONFIG1_i[26:25] CLKACTIVATIONTIME bit field (where i = 0 to 7) defines the number of GPMC_FCLK cycles from start access time to GPMC_CLK activation.
- The GPMC_CLK clock is stopped when cycle time completes and is asserted low between accesses.
- The GPMC_CLK clock is kept low when access is defined as asynchronous.

CAUTION

When the cycle time completes, the GPMC_CLK may be high because of the GPMCFCLKDIVIDER bit field. To ensure correct stoppage of the GPMC_CLK clock within the required 50-percent duty cycle, the user must extend the RDCYCLETIME or WRCYCLETIME value.

NOTE: To ensure a correct external clock cycle, the following rules must be applied:

- (RDCYCLETIME CLKACTIVATIONTIME) must be a multiple of (GPMCFCLKDIVIDER + 1).
- The PAGEBURSTACCESSTIME value must be a multiple of (GPMCFCLKDIVIDER + 1).

15.4.4.10.7 GPMC_CLK and Control Signals Setup and Hold

Control-signal transition (assertion and deassertion) setup and hold values with respect to the GPMC_CLK edge can be controlled in the following ways:

- For the GPMC_CLK signal, the GPMC_CONFIG1_i[26:25] CLKACTIVATIONTIME bit field (where i = 0 to 7) allows setup and hold control of control-signal assertion time.
- The use of a divided GPMC_CLK allows setup and hold control of the control-signal assertion and deassertion times.
- When GPMC_CLK runs at the GPMC_FCLK frequency so that GPMC_CLK edge and control-signal transitions refer to the same GPMC_FCLK edge, the control-signal transitions can be delayed by a half-GPMC_FCLK period to provide minimum setup and hold times. This half-GPMC_FCLK delay is enabled with the CSEXTRADELAY, ADVEXTRADELAY, OEEXTRADELAY, or WEEXTRADELAY parameter. This delay must be used carefully to prevent control-signal overlap between successive accesses to different chip-selects. This implies that the RDCYCLETIME and WRCYCLETIME are greater than the last control-signal deassertion time, including the extra half-GPMC_FCLK cycle.

15.4.4.10.8 Access Time (RDACCESSTIME / WRACCESSTIME)

The read/write access time durations can be programmed independently through the GPMC_CONFIG5_i[20:16] RDACCESSTIME and GPMC_CONFIG6_i[28:24] WRACCESSTIME bit fields (where i = 0 to 7). This allows nOE and GPMC data-capture timing parameters to be independent of nWE and memory device data capture timing parameters. The RDACCESSTIME and WRACCESSTIME bit fields can be set with a granularity of 1 or 2 through the GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit.

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15.4.4.10.8.1 Access Time on Read Access

In asynchronous read mode, for single and paged accesses, the GPMC_CONFIG5_i[20:16] RDACCESSTIME bit field (where i = 0 to 7) defines the number of GPMC_FCLK cycles from start access time to the GPMC_FCLK rising edge used for the first data capture. RDACCESSTIME must be programmed to the rounded greater value (in GPMC_FCLK cycles) of the read access time of the attached memory device.

In synchronous read mode, for single or burst accesses, RDACCESSTIME defines the number of GPMC_FCLK cycles from the start access time to the GPMC_FCLK rising edge corresponding to the GPMC_CLK rising edge used for the first data capture.

GPMC_CLK, which is sent to the memory device for synchronization with the GPMC controller, is internally retimed to correctly latch the returned data. The GPMC_CONFIG5_i[4:0] RDCYCLETIME bit field must be greater than RDACCESSTIME to let the GPMC latch the last return data using the internally retimed GPMC_CLK.

The external WAIT signal can be used in conjunction with RDACCESSTIME to control the effective GPMC data-capture GPMC_FCLK edge on read access in asynchronous and synchronous modes. For more information about wait monitoring, see Section 15.4.4.9.3.1, *Wait Pin Monitoring Control*.

15.4.4.10.8.2 Access Time on Write Access

In asynchronous write mode, the GPMC_CONFIG6_i[28:24] WRACCESSTIME timing parameter is not used to define the effective write access time. Instead, it is used as a wait invalid timing window and must be set to a correct value so that the gpmc_wait pin is at a valid state two GPMC_CLK cycles before WRACCESSTIME completes. For more information about wait monitoring, see Section 15.4.4.9.3.1, *Wait Pin Monitoring Control*.

In synchronous write mode , for single or burst accesses, WRACCESSTIME defines the number of GPMC_FCLK cycles from the start access time to the GPMC_CLK rising edge used by the memory device for the first data capture.

The external WAIT signal can be used in conjunction with WRACCESSTIME to control the effective memory device data-capture GPMC_CLK edge for a synchronous write access. For more information about wait monitoring, see Section 15.4.4.9.3.1, *Wait Pin Monitoring Control*.

15.4.4.10.9 Page Burst Access Time (PAGEBURSTACCESSTIME)

The GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME bit field (where i = 0 to 7) can be set with a granularity of 1 or 2 through theGPMC_CONFIG1_i[4] TIMEPARAGRANULARITY bit.

15.4.4.10.9.1 Page Burst Access Time on Read Access

In asynchronous page read mode, the delay between successive word captures in a page is controlled through the PAGEBURSTACCESSTIME bit field. The PAGEBURSTACCESSTIME parameter must be programmed to the rounded greater value (in GPMC_FCLK cycles) of the read access time of the attached device.

In synchronous burst read mode, the delay between successive word captures in a burst is controlled through the PAGEBURSTACCESSTIME bit field.

The external WAIT signal can be used in conjunction with PAGEBURSTACCESSTIME to control the effective GPMC data-capture GPMC_FCLK edge on read access. For more information about wait monitoring, see Section 15.4.4.9.3.1, *Wait Pin Monitoring Control*.

15.4.4.10.9.2 Page Burst Access Time on Write Access

Asynchronous page write mode is not supported. PAGEBURSTACCESSTIME is irrelevant in this case.

In synchronous burst write mode, PAGEBURSTACCESSTIME controls the delay between successive memory device word captures in a burst.

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The external WAIT signal can be used in conjunction with PAGEBURSTACCESSTIME to control the effective memory device data capture GPMC_CLK edge in synchronous write mode. For more information about wait monitoring, see Section 15.4.4.9.3.1, *Wait Pin Monitoring Control*.

15.4.4.10.10 Bus Keeping Support

At the end cycle time of a read access, if no other access is pending, the GPMC drives the bus with the last data read after RDCYCLETIME completes to prevent bus floating and reduce power consumption.

After a write access, if no other access is pending, the GPMC keeps driving the data bus after WRCYCLETIME completes with the same data to prevent bus floating and power consumption.

15.4.4.11 NOR Access Description

For each chip-select configuration, the read access can be specified as asynchronous or synchronous access through the GPMC_CONFIG1_i[29] READTYPE bit (where i = 0 to 7). For each chip-select configuration, the write access can be specified as synchronous or asynchronous access through the GPMC_CONFIG1_i[27] WRITETYPE bit where (i = 0 to 7).

Asynchronous and synchronous read and write access time and related control signals are controlled through timing parameters that refer to GPMC_FCLK. The primary difference of synchronous mode is the availability of a configurable clock interface (GPMC_CLK) to control the external device. Synchronous mode also affects data-capture and wait-pin monitoring schemes in read access.

For more information about asynchronous and synchronous access, see the descriptions of GPMC_CLK, RdAccessTime, WrAccessTime, and wait pin monitoring.

For more information about timing-parameter settings, see the sample timing diagrams in this chapter.

NOTE: The address bus and nBE[1:0] are fixed for the duration of a synchronous burst read access, but they are updated for each beat of an asynchronous page-read access.

15.4.4.11.1 Asynchronous Access Description

This section describes:

- Asynchronous single-read operation on an address/data multiplexed device
- Asynchronous single write operation on an address/data-multiplexed device
- Asynchronous single read operation on an AAD-multiplexed device
- Asynchronous single write operation on an AAD-multiplexed device
- Asynchronous multiple (page) read operation on a non-multiplexed device

In asynchronous operations GPMC_CLK is not provided outside the GPMC and is kept low.

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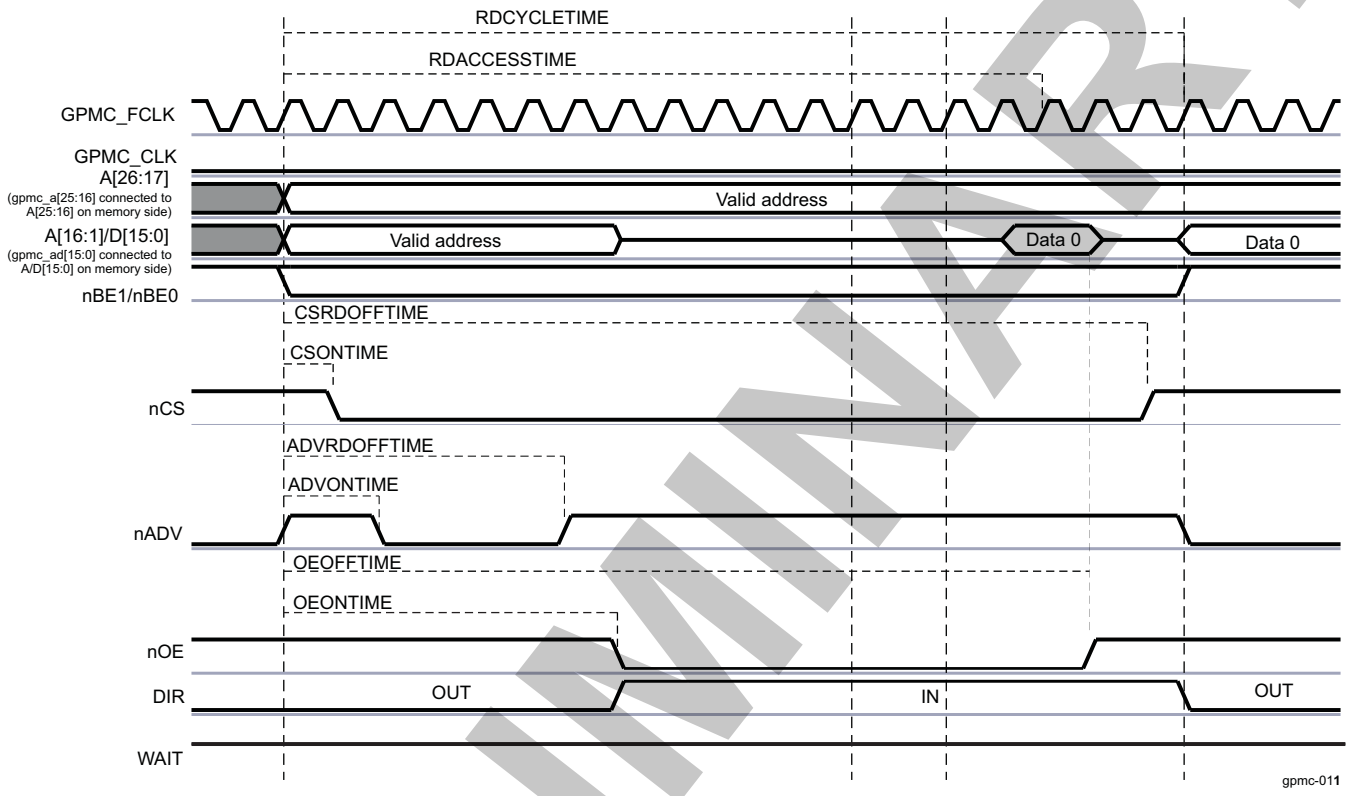
15.4.4.11.1.1 Access on Address/Data Multiplexed Devices

15.4.4.11.1.1.1 Asynchronous Single-Read Operation on an Address/Data Multiplexed Device

Figure 15-62 shows an asynchronous single read operation on an address/data-multiplexed device.

Figure 15-62. Asynchronous Single Read on an Address/Data-Multiplexed Device



For formulas to calculate timing parameters, see Section 15.4.5.6.1, *GPMC Timing Parameters Formulas*.

Table 15-374 lists the timing bit fields to set up to configure the GPMC in asynchronous single-read mode.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For more information, see Section 15.4.4.9.2.3, *Address/Data-Multiplexing Interface*.

Address bits (A[16:1] from a GPMC perspective, A[15:0] from an external device perspective) are placed on the address/data bus, and the remaining address bits gpmc_a[25:16] are placed on the address bus. The address phase ends at nOE assertion, when the DIR signal goes from OUT to IN.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3:0] CSONTIME bit field. It controls the address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC_CONFIG2_i[12:8] CSRDOFFTIME bit field. It controls the address hold time from nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME bit field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME bit field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME bit field.
  - nOE deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME bit field.

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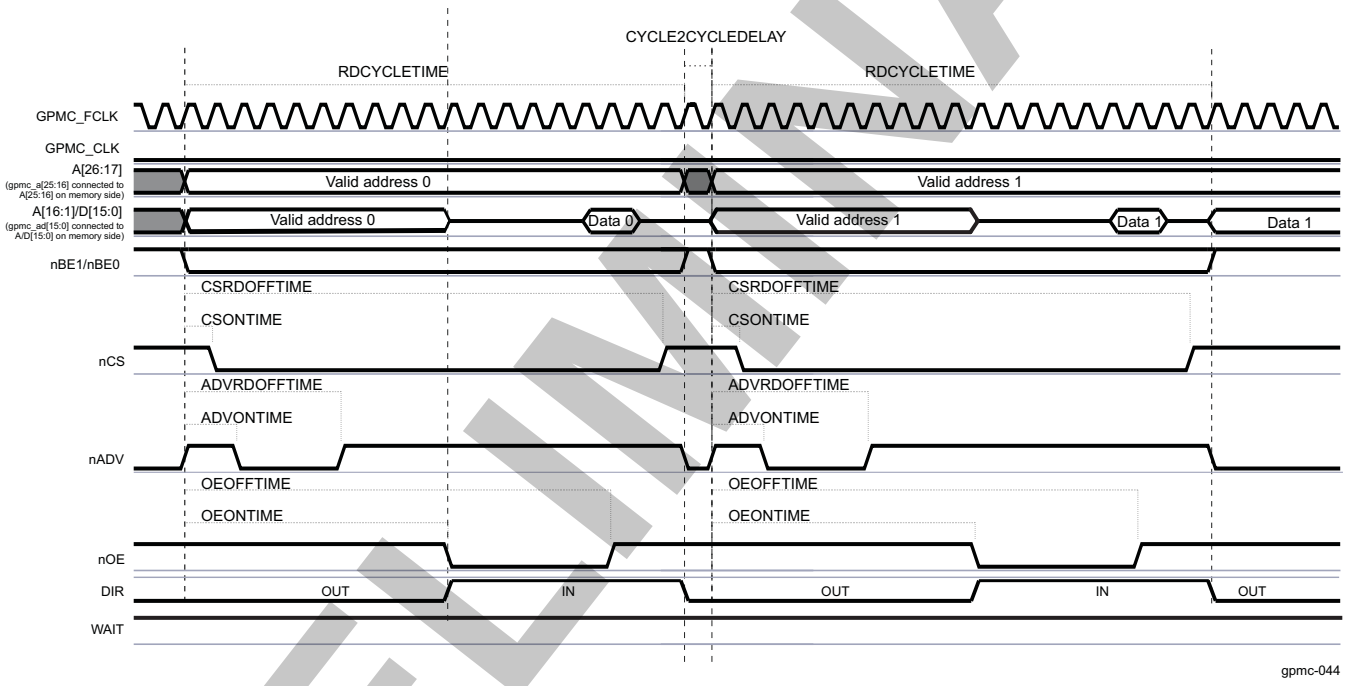
- Read data is latched when RDACCESSTIME completes. Access time is defined in the GPMC_CONFIG5_i[20:16] RDACCESSTIME bit field.
- Direction signal DIR: DIR goes from OUT to IN at the same time that nOE is asserted.
- The end of the access is defined by the GPMC_CONFIG5_i[4:0] RDCYCLETIME parameter.

In the GPMC, when a 16-bit wide device is attached to the controller, a 32-bit word write access is split into two 16-bit word write accesses. For more information about GPMC access size and type adaptation, see Section 15.4.4.11.5, *System Burst Versus External Device Burst Support*.

Between two successive accesses, if an nCS pulse is needed:

- The GPMC_CONFIG6_i[11:8] CYCLE2CYCLEDELAY bit field can be programmed with the GPMC_CONFIG6_i[7] CYCLE2CYCLESAMECSEN bit enabled.
- The CSWROFFTIME and CSONTIME parameters also allow a chip-select pulse, but this affects all other types of access.

Figure 15-63. Two Asynchronous Single-Read Accesses on an Address/Data-Multiplexed Device (32-Bit Read Split Into 2 x 16-Bit Read)



15.4.4.11.1.2 Asynchronous Single-Write Operation on an Address/Data-Multiplexed Device

Figure 15-64 shows an asynchronous single-write operation on an address/data-multiplexed device.

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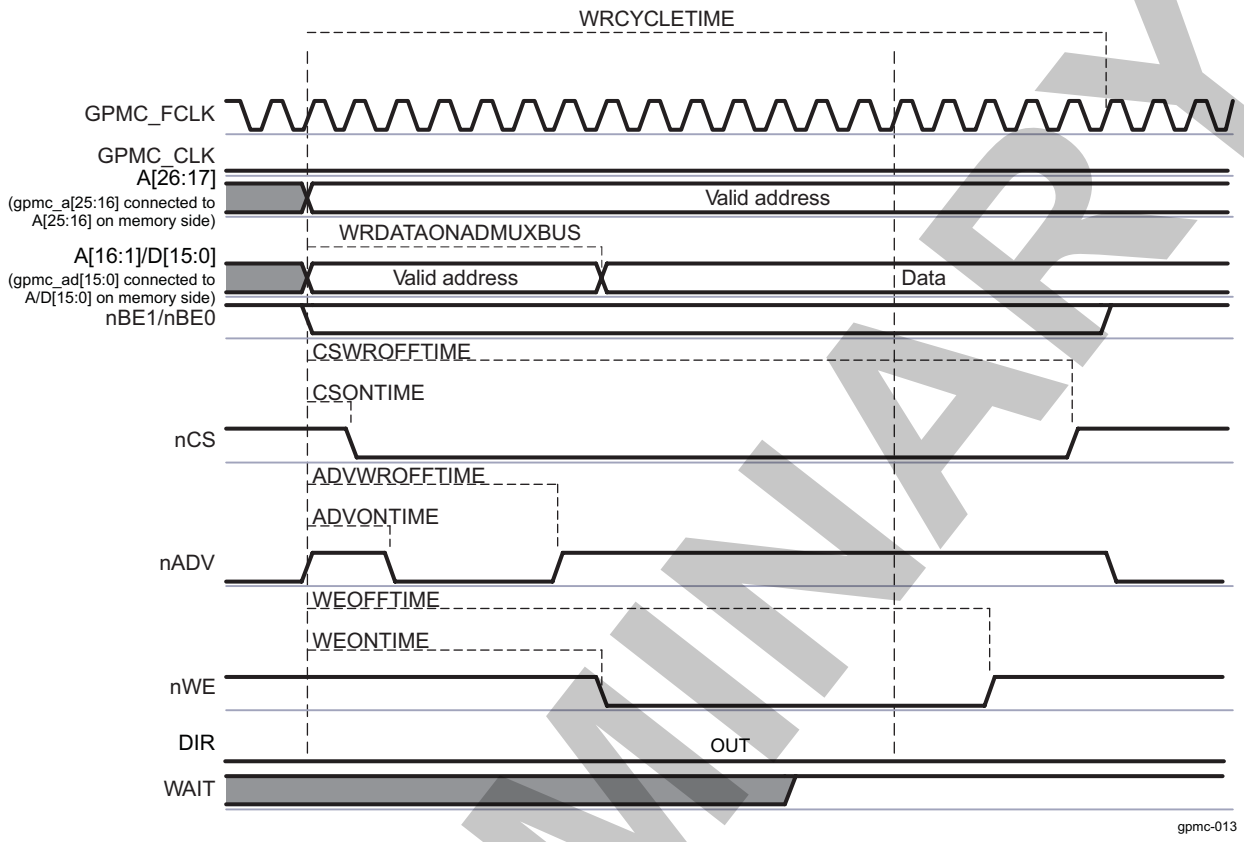
Figure 15-64. Asynchronous Single-Write on an Address/Data-Multiplexed Device



For formulas to calculate timing parameters, see Section 15.4.5.6.1, *GPMC Timing Parameters Formulas*.

Table 15-374 lists the timing bit fields to set up to configure the GPMC in asynchronous single-write mode.

When the GPMC generates a write access to an address/data-multiplexed device, it drives the address bus until nWE assertion time. For more information, see Section 15.4.4.9.2.3, *Address/Data-Multiplexing Interface*.

The nCS and nADV signals are controlled in the same way as for a asynchronous single-read operation on an address/data-multiplexed device.

- Write enable signal nWE:
  - nWE assertion indicates a write cycle.
  - nWE assertion time is controlled by the GPMC_CONFIG4_i[19:16] WEONTIME bit field.
  - nWE deassertion time is controlled by the GPMC_CONFIG4_i[28:24] WEOFFTIME bit field.
- Direction signal DIR: DIR signal is OUT during the entire access.
- The end of the access is defined by the GPMC_CONFIG5_i[12:8] WRCYCLETIME parameter.

Address bits A[16:1] (GPMC point of view) are placed on the address/data bus at the start of cycle time, and the remaining address bits A[26:17] are placed on the address bus.

Data is driven on the address/data bus at a GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS time.

NOTE: Write multiple access in asynchronous mode is not supported. If WRITEMULTIPLE is enabled with WRITETYPE as asynchronous, the GPMC processes single asynchronous accesses.

After a write operation, if no other access (read or write) is pending, the data bus keeps its previous value. See Section 15.4.4.10.10, *Bus Keeping Support*.

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15.4.4.11.1.1.3 Asynchronous Multiple (Page) Write Operation on an Address/Data-Multiplexed Device

Write multiple (page) access in asynchronous mode is not supported for address/data-multiplexed devices.

If the GPMC_CONFIG1_i[28] WRITEMULTIPLE bit is enabled (0x1) with the GPMC_CONFIG1_i[27] WRITETYPE bit as asynchronous (0x0), the GPMC processes single asynchronous accesses.

For accesses on nonmultiplexed devices, see Section 15.4.4.11.3, *Asynchronous and Synchronous Accesses in Nonmultiplexed Mode*.

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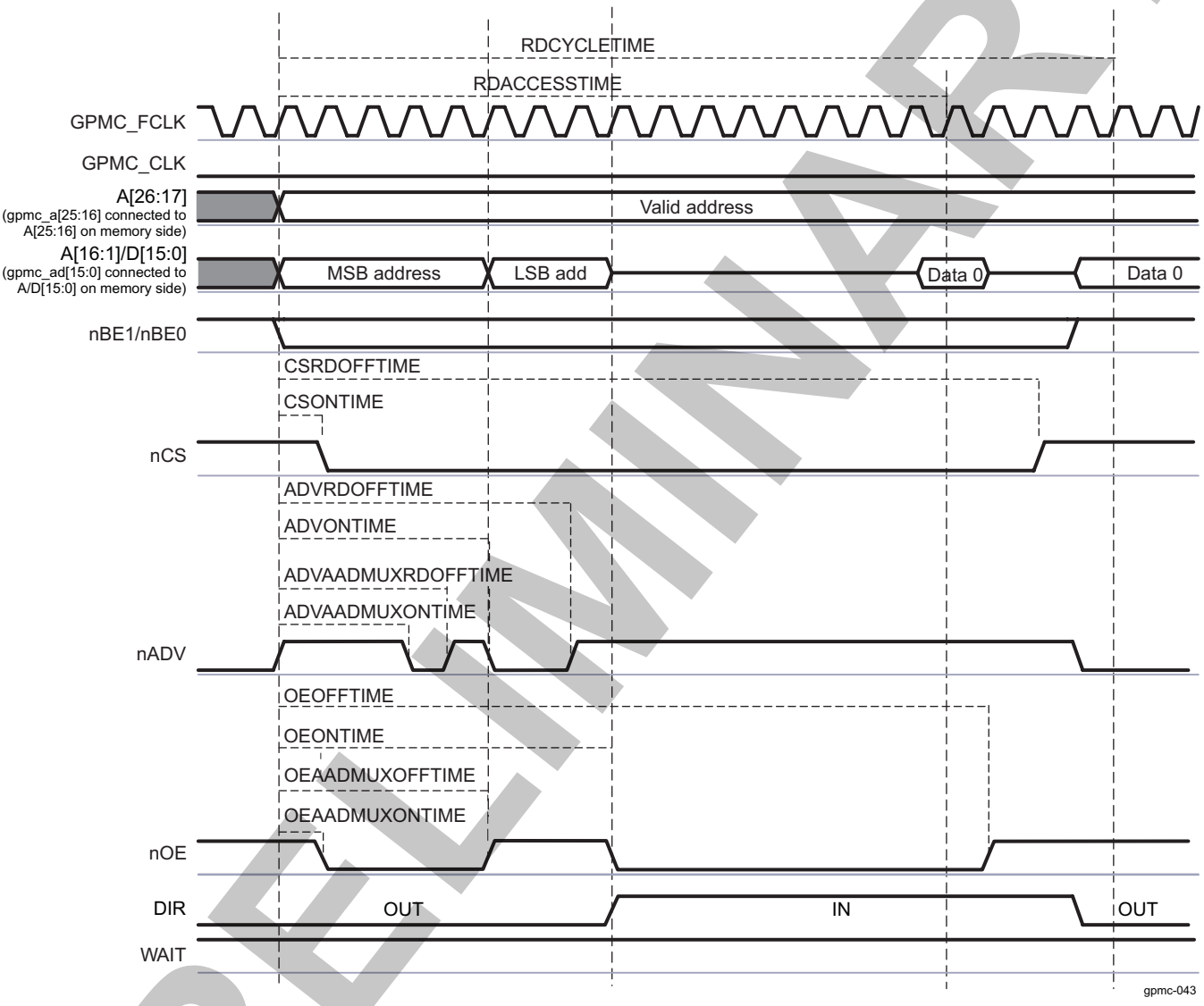
15.4.4.11.1.2 Access on Address/Address/Data-Multiplexed Devices

15.4.4.11.1.2.1 Asynchronous Single Read Operation on an AAD-Multiplexed Device

Figure 15-65 shows an asynchronous single-read operation on an AAD-multiplexed device.

Figure 15-65. Asynchronous Single Read on an AAD-Multiplexed Device



For formulas to calculate timing parameters, see Section 15.4.5.6.1, *GPMC Timing Parameters Formulas*.

Table 15-374 lists the timing bit fields to set up to configure the GPMC in asynchronous single write mode.

When the GPMC generates a read access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The first address phase ends at the first nOE deassertion time. The second phase for LSB address is qualified with nOE driven high. The second address phase ends at the second nOE assertion time, when the DIR signal goes from OUT to IN.

The nCS and DIR signals are controlled in the same way as for an asynchronous single-read operation on an address/data-multiplexed device.

- Address valid signal nADV. nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME bit field.

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- nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26:24] ADVAADMUXRDOFFTIME bit field.
- nADV second assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME bit field.
- nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME bit field.

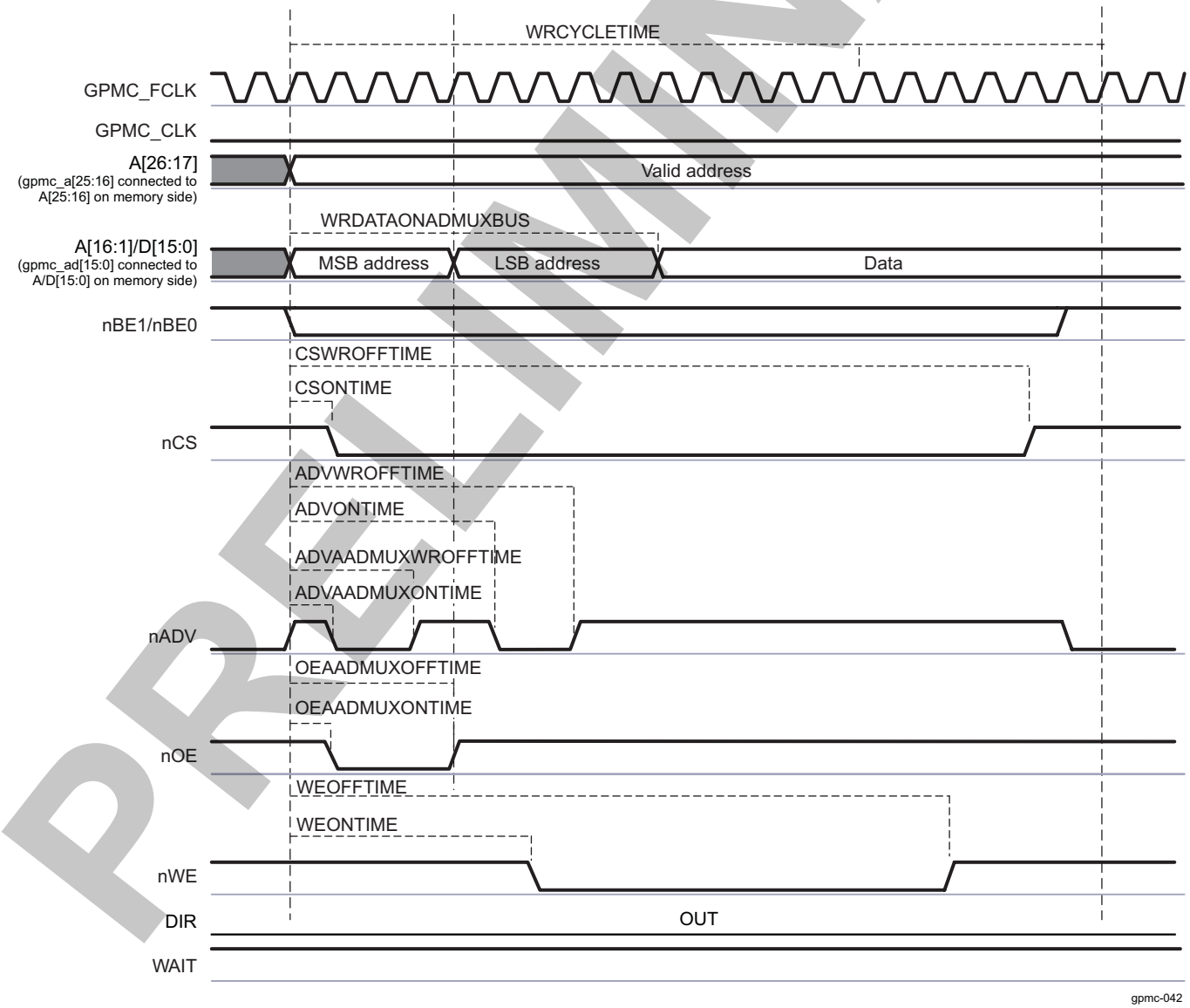
• Output Enable signal nOE. nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):

- nOE first assertion time is controlled by the GPMC_CONFIG4_i[6:4] OEAADMUXONTIME bit field.
- nOE first deassertion time is controlled by the GPMC_CONFIG3_i[15:13] OEAADMUXOFFTIME bit field.
- nOE second assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME bit field.
- nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME bit field.

15.4.4.11.1.2.2 Asynchronous Single-Write Operation on an AAD-Multiplexed Device

Figure 15-66 shows an asynchronous single-write operation on an AAD-multiplexed device.

Figure 15-66. Asynchronous Single Write on an AAD-Multiplexed Device



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For formulas to calculate timing parameters, see Section 15.4.5.6.1, *GPMC Timing Parameters Formulas*.

Table 15-374 lists the timing bit fields to set up to configure the GPMC in asynchronous single-write mode.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS, nWE, and DIR signals are controlled in the same way as for an asynchronous single-write operation on an address/data-multiplexed device. See Table 15-365.

- Address valid signal nADV is asserted and deasserted twice during a write transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[30:28] ADVAADMUXWROFFTIME bit field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[20:16] ADVWROFFTIME bit field.
- Output enable signal nOE is asserted during the address phase of a write transaction:
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[6:4] OEAADMUXONTIME bit field.
  - nOE deassertion time is controlled by the GPMC_CONFIG3_i[15:13] OEAADMUXOFFTIME bit field.

The address bits for the first address phase are driven onto the data bus until nOE deassertion. Data is driven onto the address/data bus at the clock edge defined by the GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS parameter.

15.4.4.11.1.2.3 Asynchronous Multiple (Page) Read Operation on an AAD-Multiplexed Device

Write multiple (page) access in asynchronous mode is not supported for AAD-multiplexed devices.

If the GPMC_CONFIG1_i[28] WRITEMULTIPLE bit is enabled (0x1) with the GPMC_CONFIG1_i[27] WRITETYPE bit as asynchronous (0x0), the GPMC processes single asynchronous accesses.

For accesses on nonmultiplexed devices, see Section 15.4.4.11.3, *Asynchronous and Synchronous Accessed in Nonmultiplexed Mode*.

15.4.4.11.2 Synchronous Access Description

This section describes read and write synchronous accesses on address/data-multiplexed devices. All information in this section can be applied to any type of memory (nonmultiplexed, address and data-multiplexed, or AAD-multiplexed) with the difference limited to the address phase. For accesses on nonmultiplexed devices, see Section 15.4.4.11.3, *Asynchronous and Synchronous Accessed in Nonmultiplexed Mode*.

In synchronous operations:

- The GPMC_CLK clock is provided outside the GPMC when accessing the memory device.
- The GPMC_CLK clock is derived from the GPMC_FCLK clock using the GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER bit field. In the following section i stands for the chip-select number, i = 0 to 7.
- The GPMC_CONFIG1_i[26:25] CLKACTIVATIONTIME bit field specifies that the GPMC_CLK is provided outside the GPMC for 0 to 2 GPMC_FCLK cycles after start access time until RDCYCLETIME or WRCYCLETIME completes.

15.4.4.11.2.1 Synchronous Single Read

Figure 15-67 and Figure 15-68 show a synchronous single-read operation with GPMCFCLKDIVIDER equal to 0 and 1, respectively.

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Figure 15-67. Synchronous Single Read (GPMCFCLKDIVIDER = 0)

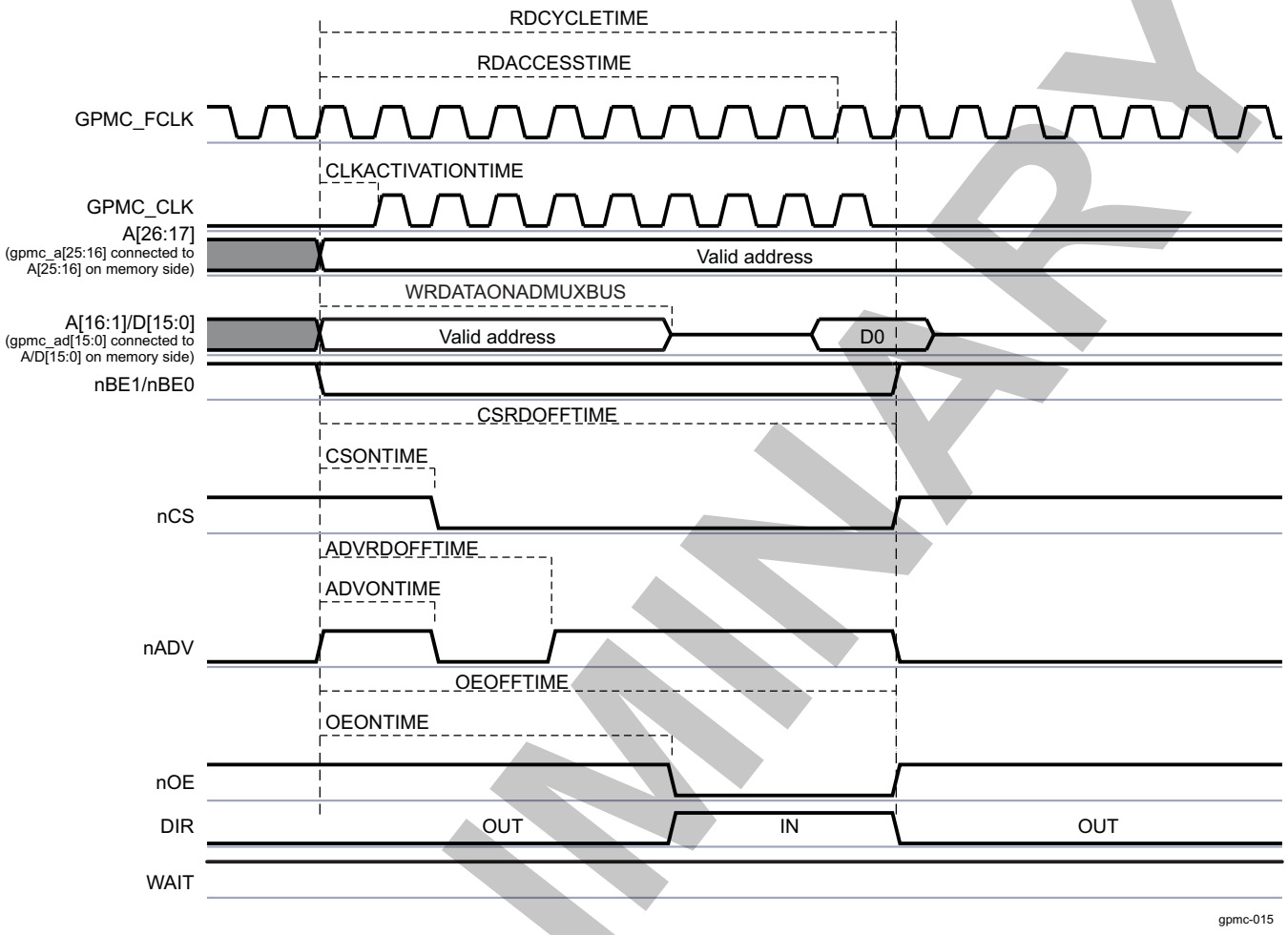

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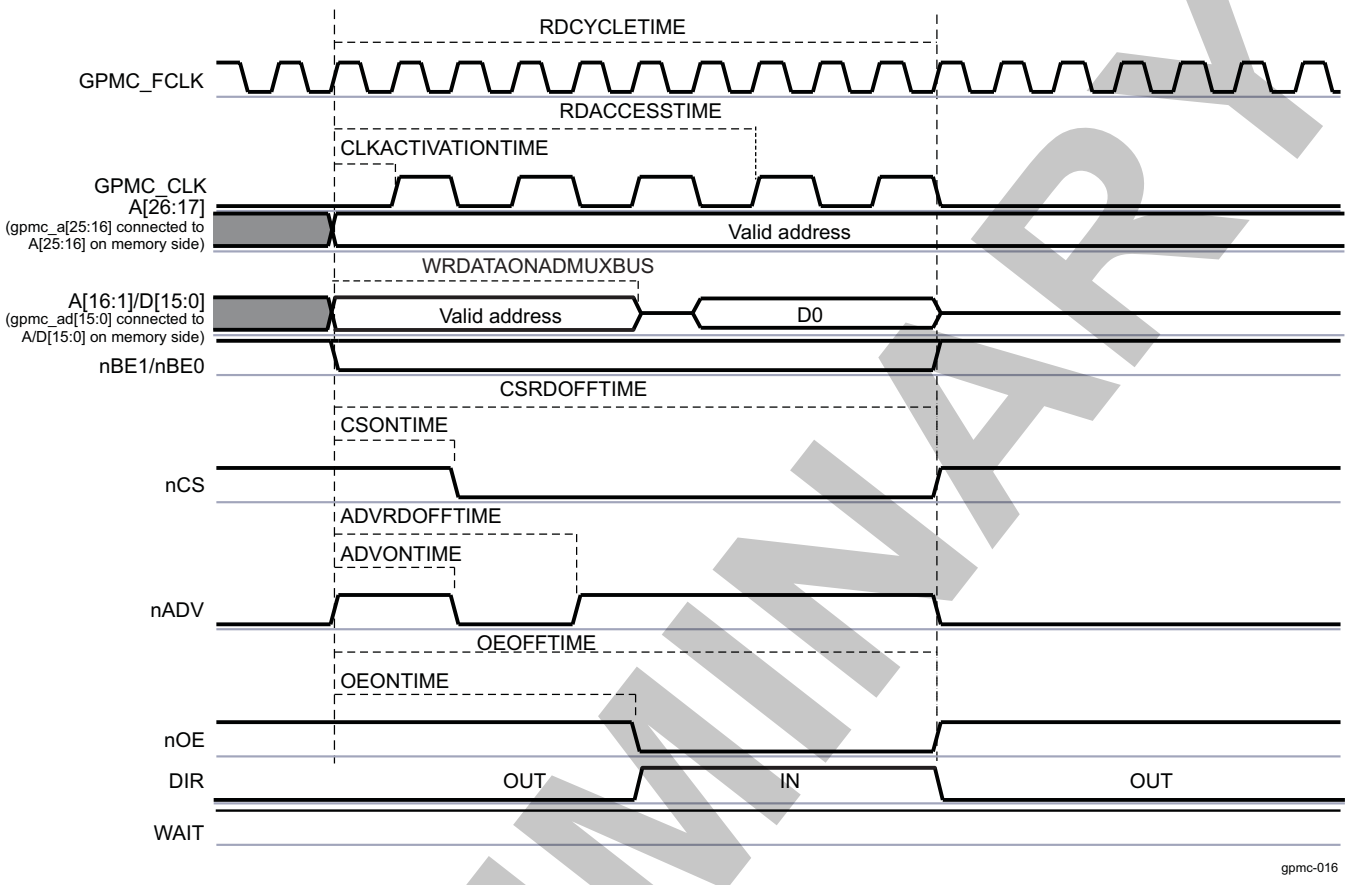
Figure 15-68. Synchronous Single Read (GPMCFCLKDIVIDER = 1)



For formulas to calculate timing parameters, see Section 15.4.5.6.1, *GPMC Timing Parameters Formulas*.

Table 15-374 lists the timing bit fields to set up to configure the GPMC in asynchronous single-read mode.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For more information, see Section 15.4.4.9.2.3, *Address/Data-Multiplexing Interface*.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3:0] CSONTIME bit field and ensures address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC_CONFIG2_i[12:8] CSRDOFFTIME bit field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME bit field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME bit field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME bit field.
  - nOE deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME bit field.
- Initial latency for the first read data is controlled by GPMC_CONFIG5_i[20:16] RDACCESSTIME bit field or by monitoring the WAIT signal.
- Total access time (the GPMC_CONFIG5_i[4:0] RDCYCLETIME bit field) corresponds to RDACCESSTIME plus the address hold time from nCS deassertion, plus time from RDACCESSTIME to CSRDOFFTIME.

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- Direction signal DIR: DIR goes from OUT to IN at the same time as nOE assertion.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS and DIR signals are controlled in the same way as for a synchronous single-read operation on an address/data-multiplexed device.

- Address valid signal nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26:24] ADVAADMUXRDOFFTIME bit field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME bit field.
- Output Enable signal nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6:4] OEAADMUXONTIME bit field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG3_i[15:13] OEAADMUXOFFTIME bit field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME bit field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME bit field.

After a read operation, if no other access (read or write) is pending, the data bus is driven with the previous read value. See Section 15.4.4.10.10, *Bus Keeping Support*.

15.4.4.11.2.2 Synchronous Multiple (Burst) Read (4-, 8-, 16-Word16 Burst With Wraparound Capability)

Figure 15-69 and Figure 15-70 show a synchronous multiple-read operation with GPMCFCLKDivider equal to 0 and 1, respectively.

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Figure 15-69. Synchronous Multiple (Burst) Read (GPMCFCLKDIVIDER = 0)

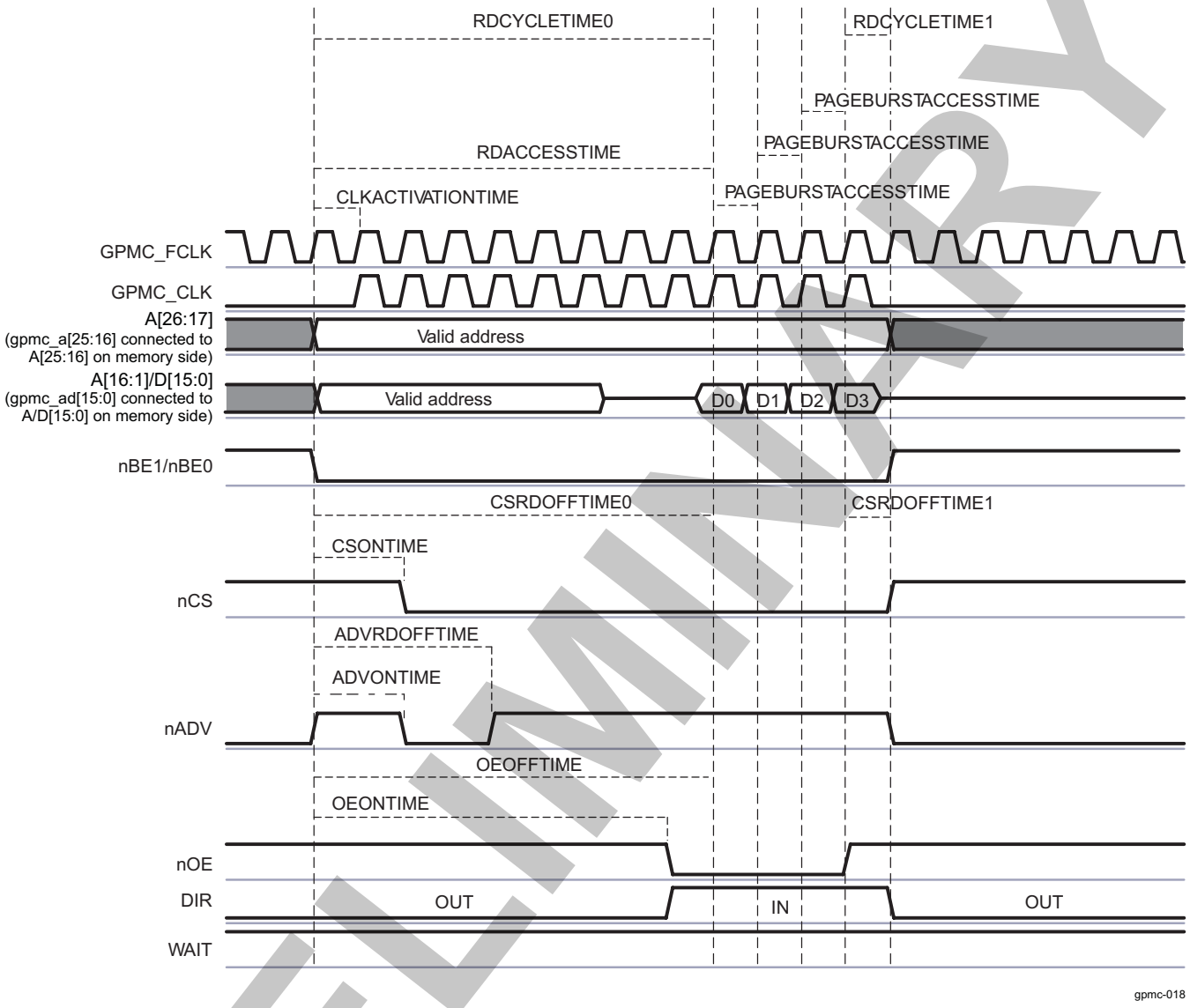

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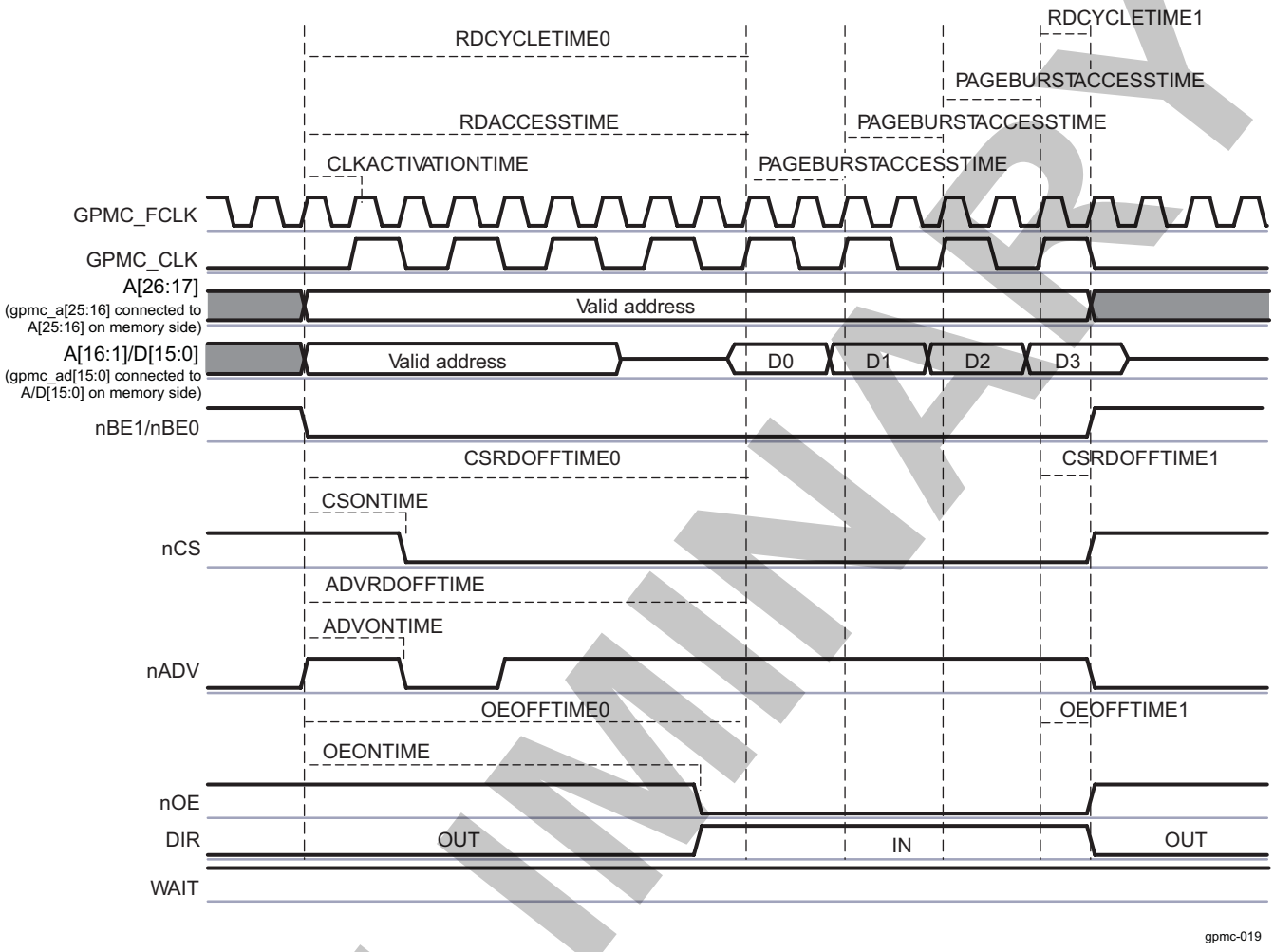
Figure 15-70. Synchronous Multiple (Burst) Read (GPMCFCLKDIVIDER = 1)



When the GPMC_CONFIG5_i[20:16] RDACCESSTIME bit field completes, control-signal timings are frozen during the multiple data transactions, corresponding to the GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME bit field multiplied by the number of remaining data transactions.

The nCS, nADV, nOE, and DIR signals are controlled in the same way as for a synchronous single-read operation. See Table 15-360.

Initial latency for the first read data is controlled by RDACCESSTIME or by monitoring the WAIT signal. Successive read data are provided by the memory device every one or two GPMC_CLK cycles. The PAGEBURSTACCESSTIME parameter must be set accordingly with the GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER bit field and the memory-device internal configuration. Depending on the device page length, the GPMC checks the device page crossing during a new burst request and purposely inserts initial latency (of RDACCESSTIME) when required.

Total access time GPMC_CONFIG5_i[4:0] RDCYCLETIME corresponds to RDACCESSTIME plus the address hold time from nCS deassertion. In Figure 15-70, the programmed value of RDCYCLETIME equals RDCYCLETIME0 + RDCYCLETIME1.

After a read operation, if no other access (read or write) is pending, the data bus is driven with the previous read value. See Section 15.4.4.10.10, *Bus Keeping Support*.

Burst wraparound is enabled through the GPMC_CONFIG1_i[31] WRAPBURST bit and allows a 4-, 8-, or 16-Word16 linear burst access to wrap within its burst-length boundary through the GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH bit field.

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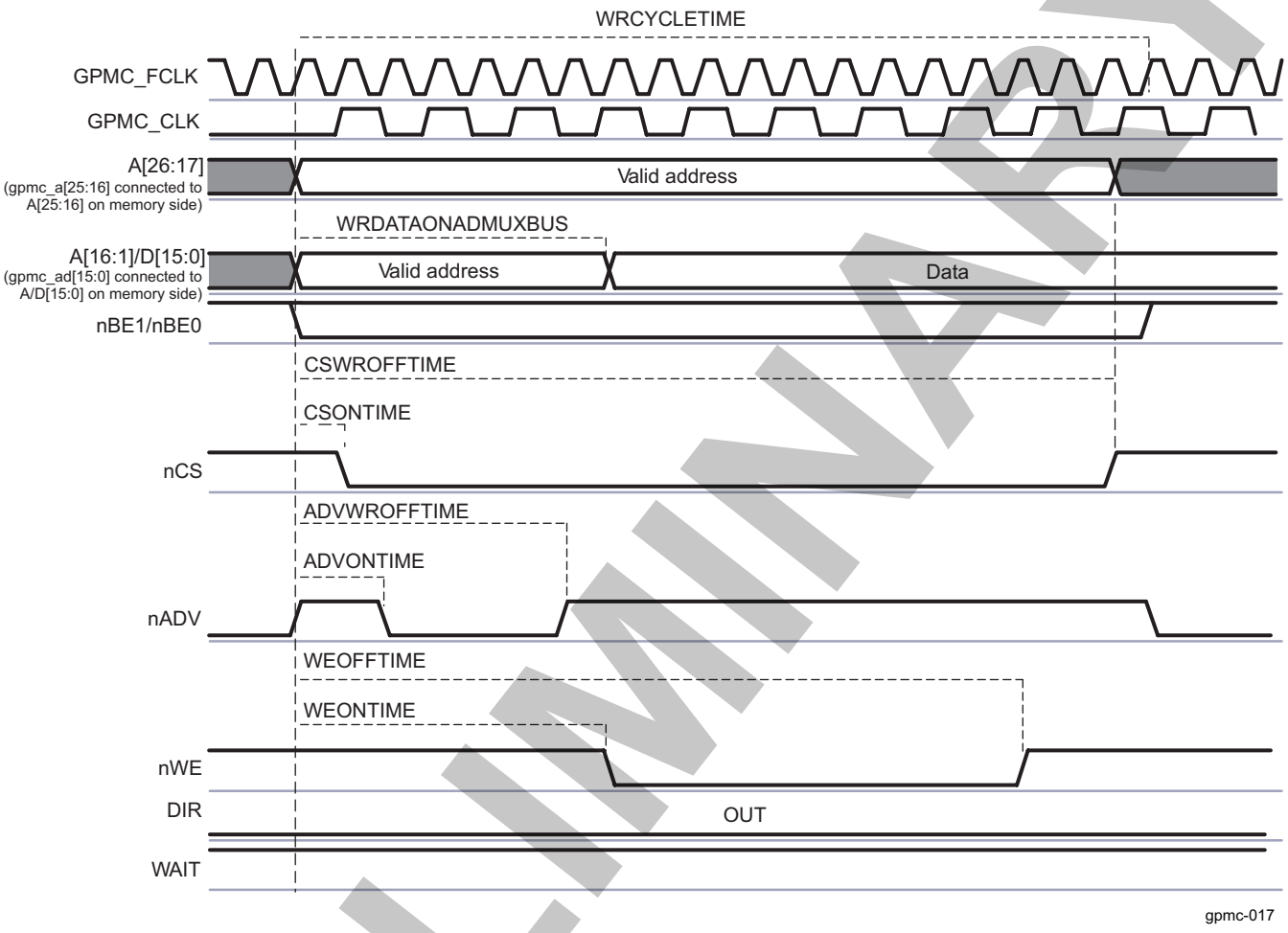
15.4.4.11.2.3 Synchronous Single Write

Burst write mode is used for synchronous single or burst accesses.

Figure 15-71. Synchronous Single Write on an Address/Data-Multiplexed Device



When the GPMC generates a write access to an address/data-multiplexed device, it drives the data bus (with address bits A[16:1]) until the GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS bit field time. The first data of the burst is driven on the address/data bus at WRDATAONADMUXBUS time.

15.4.4.11.2.4 Synchronous Multiple (Burst) Write

Synchronous burst write mode provides synchronous single or consecutive accesses.

Figure 15-72 shows a synchronous burst write access when the chip-select is configured in address/data-multiplexed mode.

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Figure 15-72. Synchronous Multiple Write (Burst Write) in Address/Data-Multiplexed Mode

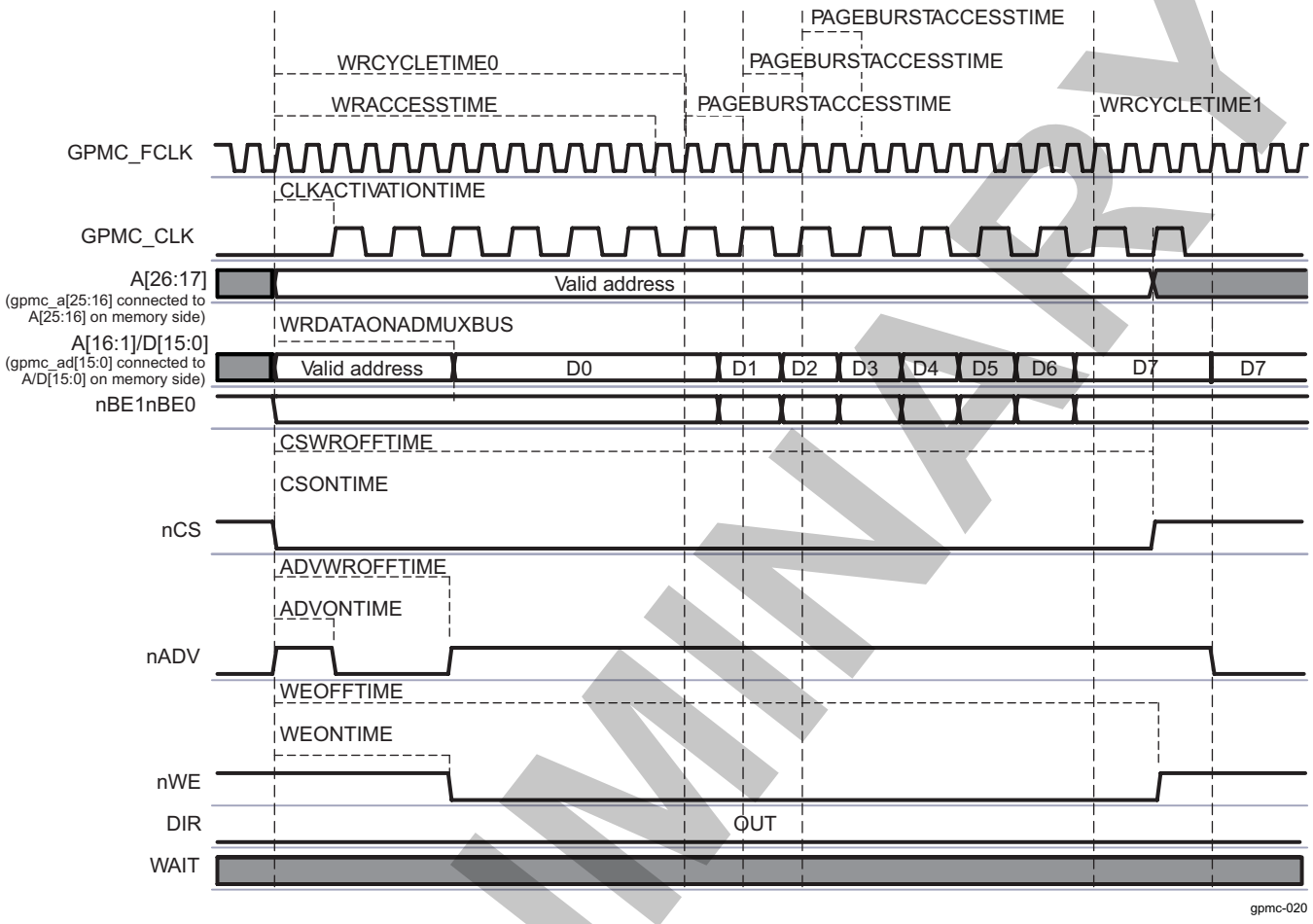

Figure 15-73 shows the same synchronous burst write access when the chip-select is configured in address/address/data-multiplexed (AAD-multiplexed) mode.

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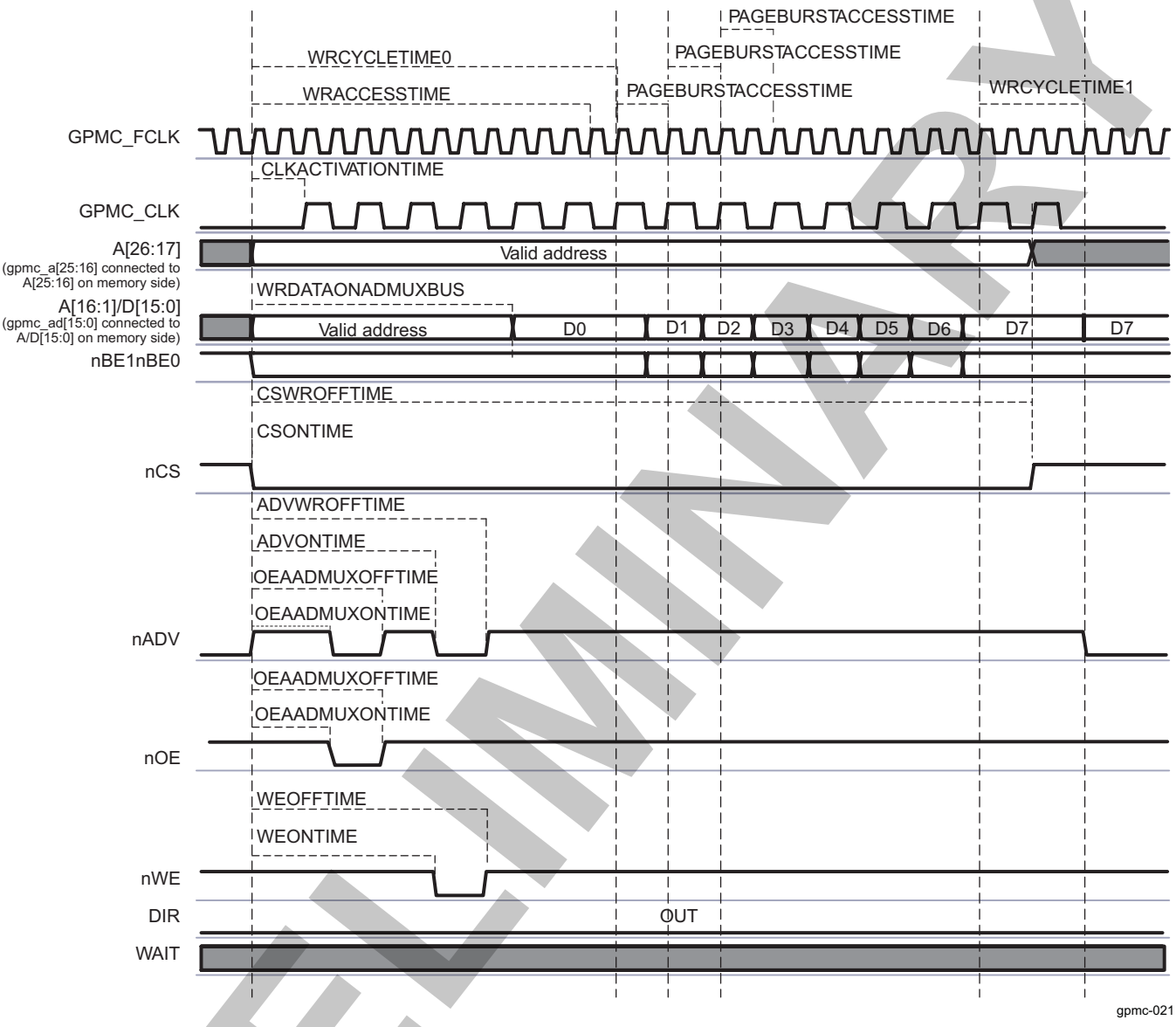
Figure 15-73. Synchronous Multiple Write (Burst Write) in Address/Address/Data-Multiplexed Mode



The first data of the burst is driven on the A/D bus at the GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS bit field.

When WRACCESSTIME completes, control-signal timings are frozen during the multiple data transactions, corresponding to the GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME bit field multiplied by the number of remaining data transactions.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time. For more information, see Section 15.4.4.9.2.3, *Address/Data-Multiplexing Interface*.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3:0] CSONTIME bit field (where i = 0 to 7) and ensures address setup time to nCS assertion.
  - nCS deassertion time controlled by the GPMC_CONFIG2_i[20:16] CSWROFFTIME bit field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME bit field.

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  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[20:16] ADVWROFFTIME bit field.
- Write enable signal nWE:
  - nWE assertion indicates a read cycle.
  - nWE assertion time is controlled by the GPMC_CONFIG4_i[19:16] WEONTIME bit field.
  - nWE deassertion time is controlled by the GPMC_CONFIG4_i[28:24] WEOFFTIME bit field.

NOTE: The nWE falling edge must not be used to control the time when the burst first data is driven in the address/data bus, because some new devices require the nWE signal to be low during the address phase.

- Direction signal DIR is OUT during the entire access.

When the GPMC generates a write access to an AAD-multiplexed device, all address bits are driven onto the address/data bus in two separate phases. The first phase is used for the MSB address and is qualified with nOE driven low. The second phase for LSB address is qualified with nOE driven high. The address phase ends at nWE assertion time.

The nCS, and DIR signals are controlled as previously described..

- Address valid signal nADV is asserted and deasserted twice during a read transaction:
  - nADV first assertion time is controlled by the GPMC_CONFIG3_i[6:4] ADVAADMUXONTIME bit field.
  - nADV first deassertion time is controlled by the GPMC_CONFIG3_i[26:24] ADVAADMUXRDOFFTIME bit field.
  - nADV second assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVONTIME bit field.
  - nADV second deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRDOFFTIME bit field.
- Output Enable signal nOE is asserted and deasserted twice during a read transaction (nOE second assertion indicates a read cycle):
  - nOE first assertion time is controlled by the GPMC_CONFIG4_i[6:4] OEAADMUXONTIME bit field.
  - nOE first deassertion time is controlled by the GPMC_CONFIG4_i[15:13] OEAADMUXOFFTIME bit field.
  - nOE second assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEONTIME bit field.
  - nOE second deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOFFTIME bit field.

First write data is driven by the GPMC at GPMC_CONFIG6_i[19:16] WRDATAONADMUXBUS, when in address/data-multiplexed configuration. The next write data of the burst is driven on the bus at WRACCESSTIME + 1 during GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME GPMC_FCLK cycles. The last data of the synchronous burst write is driven until GPMC_CONFIG5_i[12:8] WRCYCLETIME completes.

- WRACCESSTIME is defined in the GPMC_CONFIG6_i[28:24] bit field.
- The PAGEBURSTACCESSTIME parameter must be set accordingly with GPMCFCLKDIVIDER and the memory-device internal configuration.

Total access time GPMC_CONFIG5_i[12:8] WRCYCLETIME corresponds to WRACCESSTIME plus the address hold time from nCS deassertion. In Figure 15-72, the programmed value of WRCYCLETIME equals WRCYCLETIME0 + WRCYCLETIME1. WRCYCLETIME0 and WRCYCLETIME1 delays are not actual parameters and are only a graphical representation of the full WRCYCLETIME value.

After a write operation, if no other access (read or write) is pending, the data bus keeps the previous value. See Section 15.4.4.10.10, *Bus Keeping Support*.

15.4.4.11.3 Asynchronous and Synchronous Accesses in Nonmultiplexed Mode

Page mode is available only in nonmultiplexed mode. Nonmultiplexed mode is described in this section even though its use is limited (address space limited to 2KiB).

- Asynchronous single-read operation on a nonmultiplexed device
- Asynchronous single-write operation on a nonmultiplexed device

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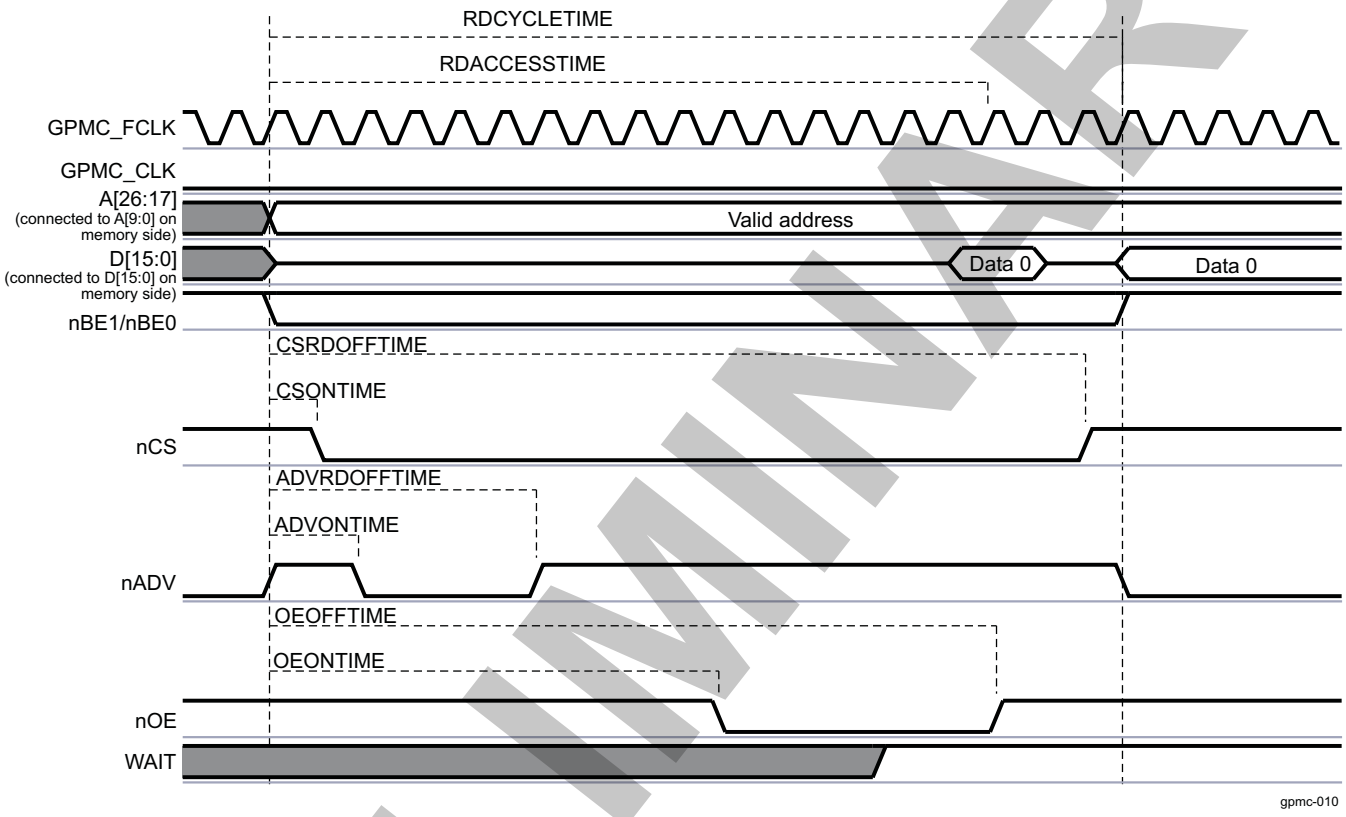
- Asynchronous multiple- (page mode) read operation on a nonmultiplexed device
- Synchronous operations on a nonmultiplexed device

15.4.4.11.3.1 Asynchronous Single-Read Operation on Nonmultiplexed Device

Figure 15-74 shows an asynchronous single-read operation on a nonmultiplexed device.

Figure 15-74. Asynchronous Single Read on an Address/Data-Nonmultiplexed Device



The 10-bit address is driven onto the address bus A[10:1] and the 16-bit data is driven onto the data bus D[15:0].

Read data is latched at GPMC_CONFIG1_5[20:16] RDACCESSTIME completion time. The end of the access is defined by the GPMC_CONFIG1_5[4:0] RDCYCLETIME parameter.

Set GPMC_CONFIG[1] LIMITEDADDRESS to 0x1 (A26-A11 are not modified during an external memory access).

The nCS, nADV, nOE, and DIR signals are controlled in the same way as address/data-multiplexed accesses (see Table 15-365).

15.4.4.11.3.2 Asynchronous Single-Write Operation on Nonmultiplexed Device

Figure 15-75 shows an asynchronous single-write operation on a nonmultiplexed device.

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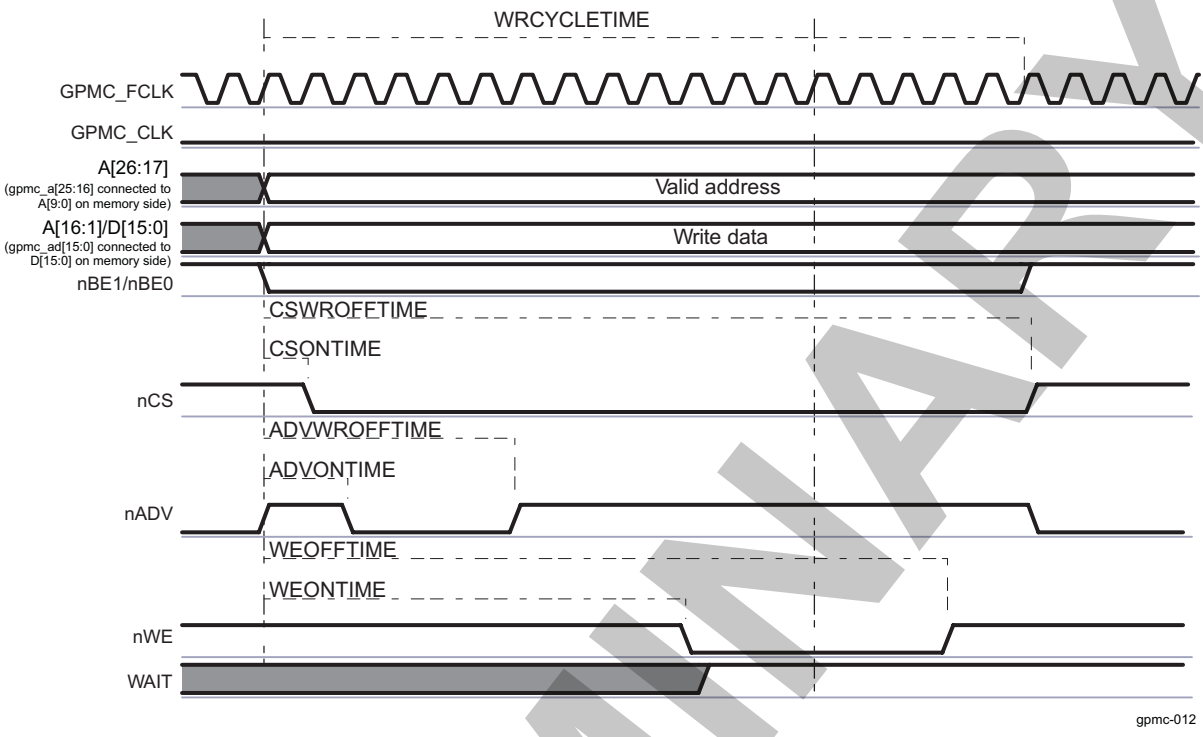
Figure 15-75. Asynchronous Single Write on an Address/Data-Nonmultiplexed Device



The 10-bit address is driven onto the address bus A[10:1] and the 16-bit data is driven onto the data bus D[15:0].

Set GPMC_CONFIG[1] LIMITEDADDRESS to 0x1 (A26-A11 are not modified during an external memory access).

The nCS, nADV, nWE, and DIR signals are controlled in the same way as address/data-multiplexed accesses (see Table 15-365).

15.4.4.11.3.3 Asynchronous Multiple (Page Mode) Read Operation on Nonmultiplexed Device

Figure 15-76 shows an asynchronous multiple-read operation on a nonmultiplexed device in which two word32 host read accesses to the GPMC are split into one multiple- (page mode of 4 word16) read access to the attached device.

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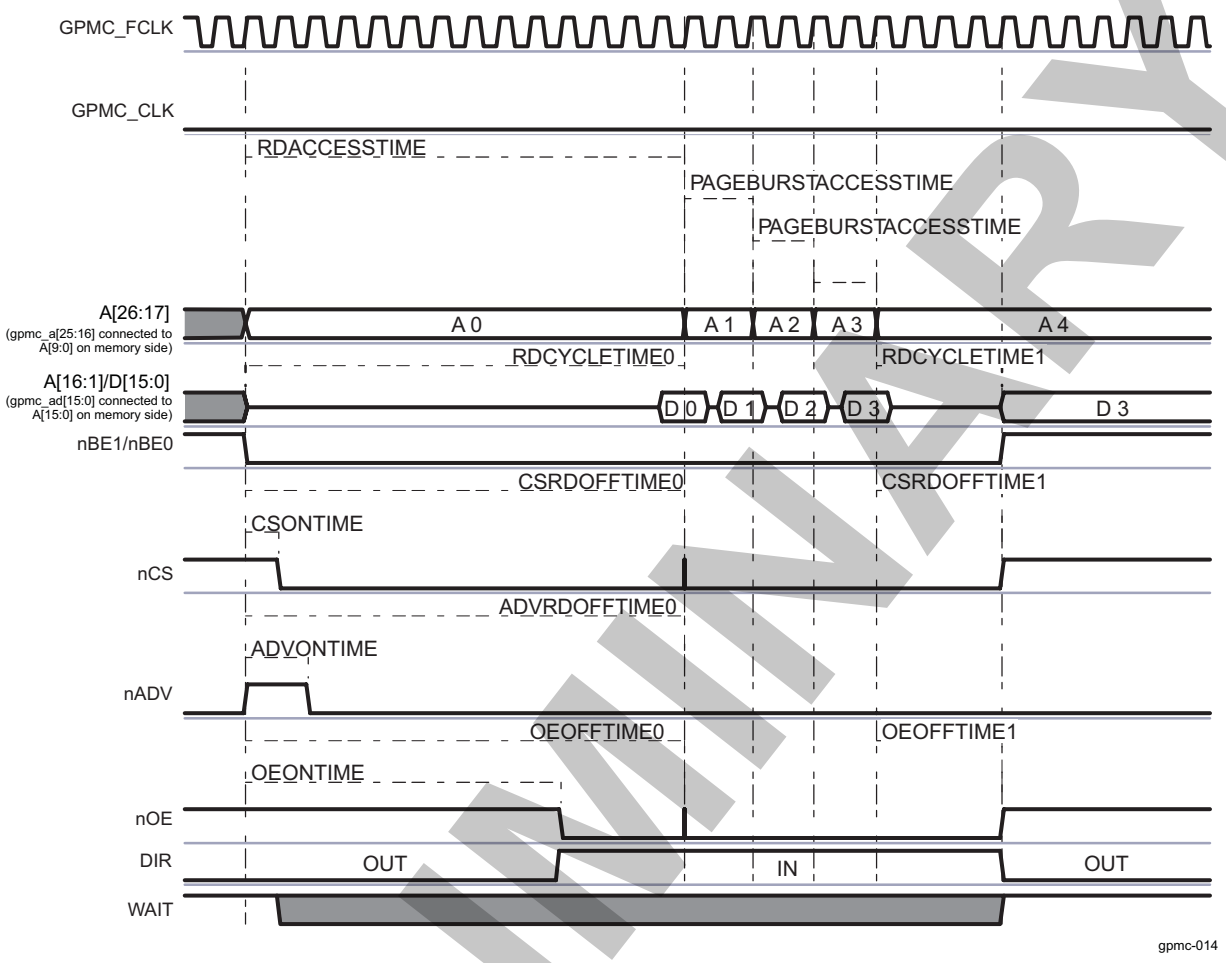
Figure 15-76. Asynchronous Multiple (Page Mode) Read



NOTE: The WAIT signal is active low.

The nCS, nADV, nOE, and DIR signals are controlled in the same way as address/data-multiplexed accesses (see Table 15-365).

When RDACCESSTIME completes, control signal timings are frozen during the multiple data transactions, corresponding to PAGEBURSTACCESSTIME multiplied by the number of remaining data transactions.

Read data is latched at GPMC_CONFIG5_i[20:16] RDACCESSTIME completion time (where i = 0 to 7). The end of the access is defined by the GPMC_CONFIG5_i[4:0] RDCYCLETIME parameter.

Set GPMC_CONFIG[1] LIMITEDADDRESS to 0x1 (A26-A11 are not modified during an external memory access).

During consecutive accesses, the GPMC increments the address after each data read completes.

Delay between successive read data in the page is controlled by the GPMC_CONFIG5_i[27:24] PAGEBURSTACCESSTIME parameter. Depending on the device page length, the GPMC can control device page crossing during a burst request and insert initial RDACCESSTIME latency. Page crossing is possible only with a new burst access, meaning a new initial access phase is initiated.

Total access time RDCYCLETIME corresponds to RDACCESSTIME, plus the address hold time, starting from the nCS deassertion.

- The read cycle time is defined in the GPMC_CONFIG5_i[4:0] RDCYCLETIME bit field.
- In Figure 15-76, the programmed value of RDCYCLETIME equals RDCYCLETIME0 (before paged accesses) + RDCYCLETIME1 (after paged accesses).

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15.4.4.11.3.4 Synchronous Operations on a Nonmultiplexed Device

All information for this section is equivalent to similar operations for address/data-multiplexed or AAD-multiplexed accesses. The only difference resides in the address phase. See Section 15.4.5.3, *GPMC Configuration in NOR Mode*.

15.4.4.11.4 Page and Burst Support

Each chip-select can be configured to process system single or burst requests into successive single accesses or asynchronous page/synchronous burst accesses, with appropriate access size adaptation.

Depending on the external device page or burst capability, read and write accesses can be independently configured through the GPMC. The GPMC_CONFIG1_i[30] READMULTIPLE and GPMC_CONFIG1_i[28] WRITMULTIPLE bits (where i = 0 to 7) are associated with the READTYPE and WRITETYPE parameters.

NOTE:

- Asynchronous write page mode is not supported.
- 8-bit-wide device support is limited to nonburstable devices (READMULTIPLE and WRITEMULTIPLE are ignored).
- Not applicable to NAND device interfacing

15.4.4.11.5 System Burst vs External Device Burst Support

The device system can issue the following requests to the GPMC:

- Byte, 16-bit word, 32-bit word requests (byte-enable-controlled). This is always a single request from the interconnect point of view.
- Incrementing fixed-length bursts of two, four, and eight words
- Wrapped (critical word access first) fixed-length burst of two, four, or eight words

To process a system request with the optimal protocol, the READMULTIPLE (and READTYPE) and WRITEMULTIPLE (and WRITETYPE) parameters must be set according to the burstable capability (synchronous or asynchronous) of the attached device.

The GPMC access engine issues only fixed-length bursts. The maximum length that can be issued is defined per chip-select by the GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH bit field (where i = 0 to 7). When the value of ATTACHEDDEVICEPAGELENGTH is less than the length of the system burst request (including the appropriate access size adaptation according to the device width), the GPMC splits the system burst request into multiple bursts. Within the specified 4-, 8-, or 16-word value, the value of the ATTACHEDDEVICEPAGELENGTH bit field must correspond to the maximum length burst supported by the memory device configured in fixed-length burst mode (as opposed to continuous burst mode).

To get optimal performance from memory devices that natively support 16 Word16-length-wrapping burst capability (critical word access first), the ATTACHEDDEVICEPAGELENGTH parameter must be set to 16 words and the GPMC_CONFIG1_i[31] WRAPBURST bit (where i = 0 to 7) must be set to 1. Similarly DEVICEPAGELENGTH is set to 4 and 8 for memories supporting 4 and 8 Word16-length-wrapping burst, respectively.

When the memory device does not offer (or is not configured to offer) native 16 Word16-length-wrapping burst, the WRAPBURST parameter must be cleared, and the GPMC access engine emulates the wrapping burst by issuing the appropriate burst sequences according to the value of ATTACHEDDEVICEPAGELENGTH.

When the memory device does not support native-wrapping burst, there is usually no difference in behavior between a fixed-burst length mode and a continuous-burst mode configuration (except for a potential power increase from a memory-speculative data prefetch in a continuous burst read). However, even though continuous burst mode is compatible with GPMC behavior, because the GPMC access engine issues only fixed-length burst and does not benefit from continuous burst mode, it is best to configure the memory device in fixed-length burst mode.

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The memory device maximum-length burst (configured in fixed-length burst wrap or nonwrap mode) usually corresponds to the memory device data buffer size. Memory devices with a minimum of 16 half-word buffers are the most appropriate (especially with wrap support), but memory devices with smaller buffer size (4 or 8) are also supported, assuming that the GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH bit field is set accordingly to 4 or 8 words.

The device system issues only requests with addresses or starting addresses for nonwrapping burst requests; that is, the request size boundary is aligned. In case of an eight-word-wrapping burst, the wrapping address always occurs on the eight-word boundary. As a consequence, all words requested must be available from the memory data buffer when the buffer size is equal to or greater than the value of ATTACHEDDEVICEPAGELENGTH. This usually means that data can be read from or written to the buffer at a constant rate (number of cycles between data) without wait-states between data accesses. If the memory does not behave this way (nonzero wait-state burstable memory), wait pin monitoring must be enabled to dynamically control data access completion within the burst.

NOTE: When the system burst request length is less than the value of ATTACHEDDEVICEPAGELENGTH, the GPMC proceeds with the required accesses.

15.4.4.12 pSRAM Access Specificities

pSRAM devices are SRAM-pin-compatible low-power memories that contain a self-refreshed DRAM memory array. The GPMC_CONFIG1_i[11:10] DEVICETYPE bit field (where i = 0 to 7) must be set to 0b00.

The pSRAM device uses the NOR protocol. It supports the following operations:

- Asynchronous single read
- Asynchronous page read
- Asynchronous single write
- Synchronous single read and write
- Synchronous burst read
- Synchronous burst write (not supported by NOR flash memory)

pSRAM devices must be powered up and initialized in a predefined manner according to the specifications of the attached device.

pSRAM devices can be programmed to use either mode: fixed or variable latency. pSRAM devices can automatically schedule autorefresh operations, which force the GPMC to use its WAIT signal capability when read or write operations occur during an internal self-refresh operation, or they can automatically include the autorefresh operation in the access time. These devices do not require additional WAIT signal capability or a minimum nCS high pulse width between consecutive accesses to ensure that the correct internal refresh operation is scheduled.

15.4.4.13 NAND Access Description

NAND (8-bit and 16-bit) memory devices using a standard NAND asynchronous address/data-multiplexing scheme can be supported on any chip-select with the appropriate asynchronous configuration settings.

As for any other type of memory compatible with the GPMC interface, accesses to a chip-select allocated to a NAND device can be interleaved with accesses to chip-selects allocated to other external devices. This interleaved capability limits the system to *chip enable don't care* NAND devices, because the chip-select allocated to the NAND device must be deasserted if accesses to other chip-selects are requested.

15.4.4.13.1 NAND Memory Device in Byte or 16-bit Word Stream Mode

NAND devices require correct command and address programming before data array read or write accesses. The GPMC does not include specific hardware to translate a random address system request into a NAND-specific multiphase access. In that sense, GPMC NAND support, as opposed to random memory-map device support, is data stream-oriented (byte or 16-bit word).

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The GPMC NAND programming model relies on a software driver for address and command formatting with the correct data address pointer value according to the block and page structure. Because of NAND structure and protocol interface diversity, the GPMC does not support automatic command and address phase programming, and software drivers must access the NAND device ID to ensure that correct command and address formatting are used for the identified device.

NAND device data read and write accesses are achieved through an asynchronous read or write access. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Any chip-select region can be qualified as a NAND region to constrain the nADV/ALE signal as ALE (ALE active high, default state value at low) during address program access, and the nBE0/CLE signal as CLE (CLE active high, default state value at low) during command program access. GPMC address lines are not used (the previous value is not changed) during NAND access.

15.4.4.13.1.1 Chip-Select Configuration for NAND Interfacing in Byte or Word Stream Mode

The GPMC_CONFIG7_i register (where i = 0 to 7) associated with a NAND device region interfaced in byte or word stream mode can be initialized with a minimum size of 16MiB, because any address location in the chip-select memory region can be used to access a NAND data array. The NAND flash protocol specifies an address sequence where address bits are passed through the data bus in a series of write accesses with the ALE pin asserted. After this address phase, all operations are streamed and the system requests address is irrelevant.

CAUTION

To allow correct command, address, and data-access controls, the GPMC_CONFIG1_i register associated with a NAND device region must be initialized in asynchronous read and write modes with the parameters listed in Table 15-343. Failure to comply with these settings corrupts the NAND interface protocol.

Table 15-343. Chip-Select Configuration for NAND Interfacing

Bit Field	Register	Value	Comments
WRAPBURST	GPMC_CONFIG1_i[31] (1)	0	No wrap
READMULTIPLE	GPMC_CONFIG1_i[30]	0	Single access
READTYPE	GPMC_CONFIG1_i[29]	0	Asynchronous mode
WRITEMULTIPLE	GPMC_CONFIG1_i[28]	0	Single access
WRITETYPE	GPMC_CONFIG1_i[27]	0	Asynchronous mode
CLKACTIVATIONTIME	GPMC_CONFIG1_i[26:25]	0b00	
ATTACHEDDEVICEPAGELENGTH	GPMC_CONFIG1_i[24:23]	Don't care	Single-access mode
WAITREADMONITORING	GPMC_CONFIG1_i[22]	0	Wait not monitored by GPMC access engine
WAITWRITEMONITORING	GPMC_CONFIG1_i[21]	0	Wait not monitored by GPMC access engine
WAITMONITORINGTIME	GPMC_CONFIG1_i[19:18]	Don't care	Wait not monitored by GPMC access engine
WAITPINSELECT	GPMC_CONFIG1_i[17:16]		Select which wait is monitored by edge detectors
DEVICESIZE	GPMC_CONFIG1_i[13:12]	0b00 or 0b01	8- or 16-bit interface
DEVICETYPE	GPMC_CONFIG1_i[11:10]	0b10	NAND device in stream mode
MUXADDDATA	GPMC_CONFIG1_i[9:8]	0b00	Nonmultiplexed mode

(1) i = 0 to 7

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Table 15-343. Chip-Select Configuration for NAND Interfacing (continued)

Bit Field	Register	Value	Comments
TIMEPARAGRANULARITY	GPMC_CONFIG1_i[4]	0	Timing achieved with best GPMC clock granularity
GPMCFCLKDIVIDER	GPMC_CONFIG1_i[1:0]	Don't care	Asynchronous mode

The GPMC_CONFIG1_i to GPMC_CONFIG4_i registers (where i = 0 to 7) associated with a NAND device region must be initialized with the correct control-signal timing value according to the NAND device timing parameters.

15.4.4.13.1.2 NAND Device Command and Address Phase Control

NAND devices require multiple address programming phases. The MPU software driver must issue the correct number of command and address program accesses, according to the device command set and the device address-mapping scheme.

NAND device-command and address-phase programming is achieved through write requests to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i register locations (where i = 0 to 7) with the correct command and address values. These locations are mapped in the associated chip-select register region. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Command and address values are not latched during the access and cannot be read back at the register location.

- Only write accesses must be issued to these locations, but the GPMC does not discard any read access. Accessing a NAND device with nOE and CLE or ALE asserted (read access) can produce undefined results.
- Write accesses to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i register locations must be posted for faster operations (where i = 0 to 7). The GPMC_CONFIG[0] NANDFORCEPOSTEDWRITE bit enables write accesses to these locations as posted, even if they are defined as nonposted.

A write buffer is used to store write transaction information before the external device is accessed:

- Up to eight consecutive posted write accesses can be accepted and stored in the write buffer.
- For nonposted write, the pipeline is one deep.
- An GPMC_STATUS[0] EMPTYWRITEBUFFERSTATUS bit stores the empty status of the write buffer.

The GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i registers (where i = 0 to 7) are 32-bit word locations, which means any 32-or 16-bit word access is split into 4- or 2-byte accesses if an 8-bit-wide NAND device is attached. For multiple-command phase or multiple-address phase, the software driver can use 32- or 16-bit word access to these registers, but it must consider the splitting and little-endian ordering scheme. When only one byte command or address phase is required, only byte write access to the GPMC_NAND_COMMAND_i and GPMC_NAND_ADDRESS_i registers can be used, and any of the four byte locations of the registers is valid.

The same applies to a GPMC_NAND_COMMAND_i and a GPMC_NAND_ADDRESS_i (where i = 0 to 7) 32-bit word write access to a 16-bit-wide NAND device (split into two 16-bit word accesses). In the case of a 16-bit word write access, the MSByte of the 16-bit word value must be set according to the NAND device requirement (usually 0). Either 16-bit word location or any one of the four byte locations of the registers is valid.

15.4.4.13.1.3 Command Latch Cycle

Writing data at the GPMC_NAND_COMMAND_i location (where i = 0 to 7) places the data as the NAND command value on the bus, using a regular asynchronous write access.

- nCE is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- CLE is controlled by the ADVONTIME and ADVWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.

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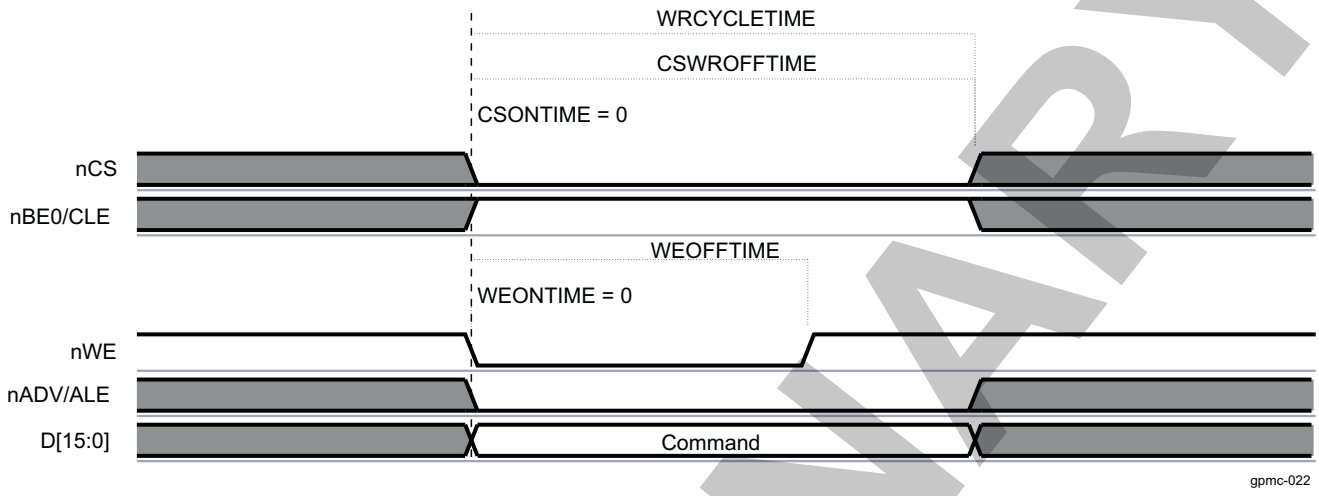
- ALE and nRE (nOE) are maintained inactive.

Figure 15-77 shows the NAND command latch cycle.

Figure 15-77. NAND Command Latch Cycle



NOTE: CLE is shared with the nBE0 output signal and has an inverted polarity from BE0. The NAND qualifier deals with this. During the asynchronous NAND data access cycle, nBE0 (also nBE1) must not toggle, because it is shared with CLE.

NAND flash memories do not use byte-enable signals.

15.4.4.13.1.4 Address Latch Cycle

Writing data at the GPMC_NAND_ADDRESS_i location (where i = 0 to 7) places the data as the NAND partial address value on the bus, using a regular asynchronous write access.

- nCS is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- ALE is controlled by the ADVONTIME and ADVWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- CLE and nRE (nOE) are maintained inactive.

Figure 15-78 shows the NAND address latch cycle.

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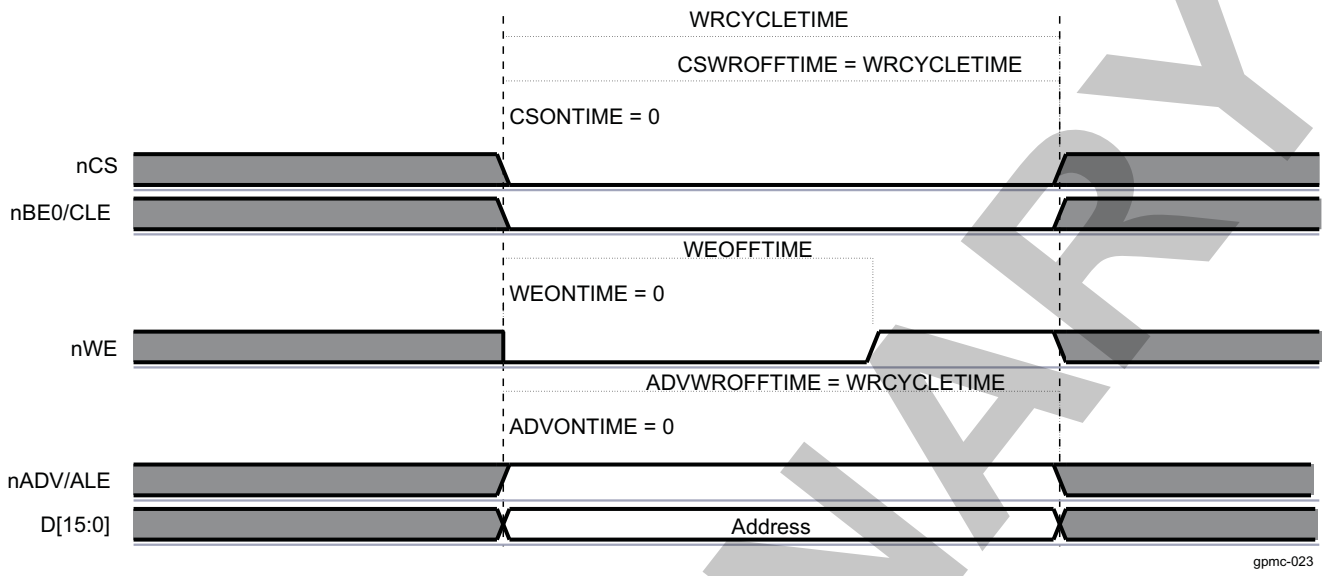
Figure 15-78. NAND Address Latch Cycle



NOTE: ALE is shared with the nADV output signal and has an inverted polarity from ADV. The NAND qualifier deals with this. During the asynchronous NAND data access cycle, ALE is kept stable.

15.4.4.13.1.5 NAND Device Data Read and Write Phase Control in Stream Mode

NAND device data read and write accesses are achieved through a read or write request to the chip-select-associated memory region at any address location in the region or through a read or write request to the GPMC_NAND_DATA_i location (where i = 0 to 7) mapped in the chip-select-associated control register region. GPMC_NAND_DATA_i is not a true register, but an address location to enable nRE or nWE signal control. The associated chip-select signal timing control must be programmed according to the NAND device timing specification.

Reading data from the GPMC_NAND_DATA_i location or from any location in the associated chip-select memory region activates an asynchronous read access.

- nCS is controlled by the CSONTIME and CSRDOFFTIME timing parameters.
- nRE is controlled by the OEONTIME and OEOFFTIME timing parameters.
- To take advantage of nRE high-to-data invalid minimum timing value, RDACCESSTIME can be set so that data are effectively captured after nRE deassertion. This allows optimization of NAND read access cycle time completion. For optimal timing parameter settings, see the NAND device and the device timing parameters.

ALE, CLE, and nWE are maintained inactive.

Figure 15-79 shows the NAND data read cycle.

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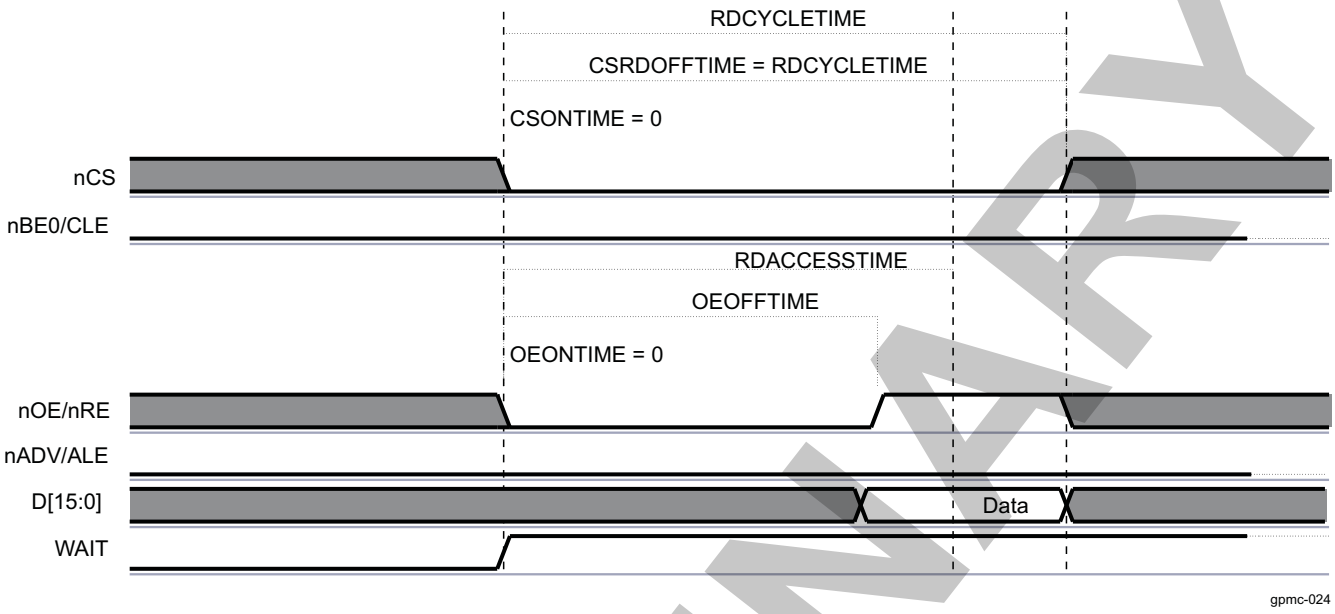
Figure 15-79. NAND Data Read Cycle

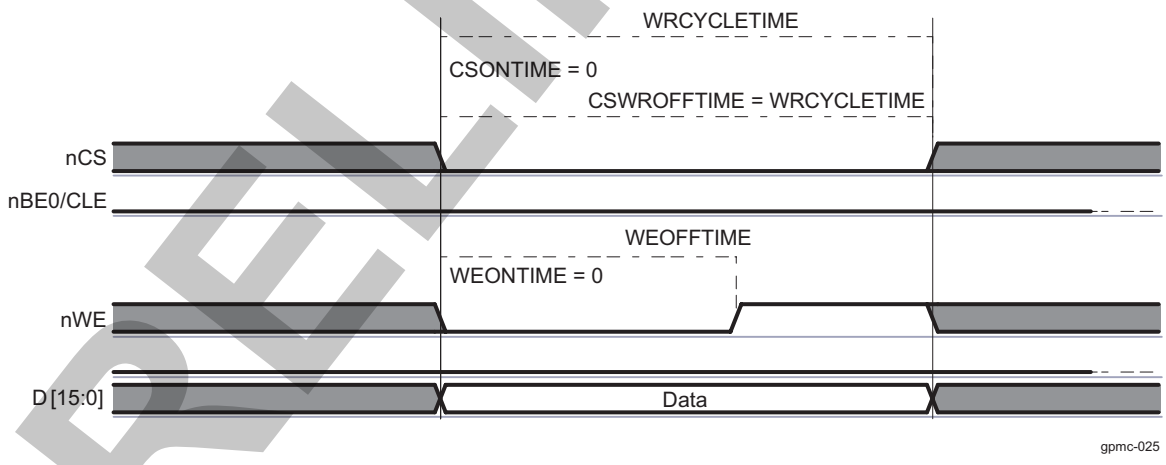


Writing data to the GPMC_NAND_DATA_i location or to any location in the associated chip-select memory region activates an asynchronous write access.

- nCS is controlled by the CSONTIME and CSWROFFTIME timing parameters.
- nWE is controlled by the WEONTIME and WEOFFTIME timing parameters.
- ALE, CLE, and nRE (nOE) are maintained inactive.

Figure 15-80 shows the NAND data write cycle.

Figure 15-80. NAND Data Write Cycle



15.4.4.13.1.6 NAND Device General Chip-Select Timing Control Requirement

For most NAND devices, read data access time is dominated by nCS-to-data-valid timing and has faster nRE-to-data-valid timing. Successive accesses with nCS deassertions between accesses are affected by this timing constraint. Because accesses to a NAND device can be interleaved with other chip-select accesses, there is no certainty that nCS always stays low between two accesses to the same chip-select. Moreover, an nCS deassertion time between the same chip-select NAND accesses is likely to be required as follows: the nCS deassertion requires programming CYCLETIME and RDACCESSTIME according to the nCS-to-data-valid critical timing.

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To get full performance from NAND read and write accesses, the prefetch engine can dynamically reduce the following on back-to-back NAND accesses (to the same memory) and suppress the minimum nCS high pulse width between accesses:

- RDCYCLETIME
- WRCYCLETIME
- RDACCESSTIME
- WRACCESSTIME
- CSRDOFFTIME
- CSWROFFTIME
- ADVRDOFFTIME
- ADVWROFFTIME
- OEOFFTIME
- WEOFFTIME

For more information about optimal prefetch engine access, see Section 15.4.4.13.4, *Prefetch and Write-Posting Engine*.

Some NAND devices require minimum write-to-read idle time, especially for device-status read accesses following status-read command programming (write access). If such write-to-read transactions are used, a minimum nCS high pulse width must be set. For this, CYCLE2CYCLESAMECSEN and CYCLE2CYCLEDELAY must be set according to the appropriate timing requirement to prevent any timing violation.

NAND devices usually have an important nRE high-to-data bus in three-state mode. This requires a bus turnaround setting (BUSTURNAROUND = 1) so that the next access to a different chip-select is delayed until the BUSTURNAROUND delay completes. Back-to-back NAND read accesses to the same NAND flash are not affected by the programmed bus turnaround delay.

15.4.4.13.1.7 Read and Write Access Size Adaptation

15.4.4.13.1.7.1 8-Bit-Wide NAND Device

Host 16- and 32-bit word read and write access requests to a chip-select associated with an 8-bit-wide NAND device are split into successive read and write byte accesses to the NAND memory device. Byte access is ordered according to little-endian organization. A NAND 8-bit-wide device must be interfaced on the D0D7 interface bus lane. GPMC data accesses are justified on this bus lane when the cs is associated with an 8-bit-wide NAND device.

15.4.4.13.1.7.2 16-Bit-Wide NAND Device

Host 32-bit word read and write access requests to a chip-select associated with a 16-bit-wide NAND device are split into successive read and write 16-bit word accesses to the NAND memory device. 16-bit word access is ordered according to little-endian organization.

Host byte read and write access requests to a 16-bit-wide NAND device are completed as 16-bit accesses on the device itself, because there is no byte-addressing capability on 16-bit-wide NAND devices. This means that the NAND device address pointer is incremented on a 16-bit word basis and not on a byte basis. For a read access, only the requested byte is given back to the host, but the remaining byte is not stored or saved by the GPMC, and the next byte or 16-bit word read access gets the next 16-bit word NAND location. For a write access, the invalid byte part of the 16-bit word is driven to FF, and the next byte or 16-bit word write access programs the next 16-bit word NAND location.

Generally, byte access to a 16-bit-wide NAND device must be avoided, especially when ECC calculation is enabled. 8- or 16-bit ECC-based computations are corrupted by a byte read to a 16-bit-wide NAND device, because the nonrequested byte is considered invalid on a read access (not captured on the external data bus; FF is fed to the ECC engine) and is set to FF on a write access.

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Host requests (read/write) issued in the chip-select memory region are translated in successive single or split accesses (read/write) to the attached device. Therefore, incrementing 32-bit burst requests are translated in multiple 32-bit sequential accesses following the access adaptation of the 32-bit to 8- or 16-bit device.

15.4.4.13.2 NAND Device-Ready Pin

The NAND memory device provides a ready pin to indicate data availability after a block/page opening and to indicate that data programming is complete. The ready pin can be connected to one of the wait GPMC input pins; data read accesses must not be tried when the ready pin is sampled inactive (device is not ready) even if the associated chip-select WAITREADMONITORING bit field is set. The duration of the NAND device busy state after the block/page opening is so long (up to 50 micro second) that accesses occurring when the ready pin is sampled inactive can stall GPMC access and eventually cause a system time-out.

NOTE: If a read access to a NAND flash is done using wait monitoring mode, the device is blocked during a page opening, and so is the GPMC. If the correct settings are used, other chip-selects can be used while the memory processes the page opening command.

To avoid a time-out caused by a block/page opening delay in NAND flash, disable the wait pin monitoring for read and write accesses (that is, set the GPMC_CONFIG1_i[21] WAITWRITEMONITORING and GPMC_CONFIG1_i[22] WAITREADMONITORING bits to 0, where i = 0 to 7), and use one of the following methods instead:

- Use software to poll the WAITxSTATUS bit (where x = 0 to 2) of the GPMC_STATUS .
- Configure an interrupt that is generated on the WAIT signal change (through the GPMC_IRQENABLE register bits[11:8]).

Even if the READWAITMONITORING bit is not set, the external memory nR/B pin status is captured in the programmed wait bit in the GPMC_STATUS register.

The READWAITMONITORING bit method must be used for other memories than NAND flash, if they require the use of a WAIT signal.

15.4.4.13.2.1 Ready Pin Monitored by Software Polling

The ready signal state can be monitored through the GPMC_STATUS WAITxSTATUS bit (where x = 0 to 2). Software must monitor the ready pin only when the signal is declared valid. Refer to the NAND device timing parameters to set the correct software temporization to monitor ready only after the invalid window is complete from the last read command written to the NAND device.

15.4.4.13.2.2 Ready Pin Monitored by Hardware Interrupt

Each gpmc_wait input pin can generate an interrupt when a wait-to-no-wait transition is detected. Depending on whether the GPMC_CONFIG WAITxPINPOLARITY bits (where x = 0 to 2) is active low or active high, the wait-to-no-wait transition is a low-to-high external WAIT signal transition or a high-to-low external WAIT signal transition, respectively.

The wait transition pin detector must be cleared before any transition detection. This is done by writing 1 to the WAITxEDGEDETECTIONSTATUS bit (where x = 0 to 2) of the GPMC_IRQSTATUS register according to the gpmc_wait pin used for the NAND device-ready signal monitoring. To detect a wait-to-no-wait transition, the transition detector requires a wait active time detection of a minimum of two GPMC_FCLK cycles. Software must incorporate precautions to clear the wait transition pin detector before wait (busy) time completes.

A wait-to-no-wait transition detection can issue a GPMC interrupt if the WAITxEDGEDETECTIONENABLE bit in the GPMC_IRQENABLE register is set and if the WAITxEDGEDETECTIONSTATUS bit field in the GPMC_IRQSTATUS register is set.

The WAITMONITORINGTIME bit field does not affect wait-to-no-wait transition time detection.

It is also possible to poll the WAITxEDGEDETECTIONSTATUS bit field in the GPMC_IRQSTATUS register according to the gpmc_wait pin used for NAND device ready signal monitoring.

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15.4.4.13.3 ECC Calculator

The GPMC includes an error code correction (ECC) calculator circuitry that enables ECC calculation on the fly during data read or data program (that is, write) operations. The page size supported by the ECC calculator in one calculation/context is 512 bytes.

The user can choose from two different algorithms with different error correction capabilities through the GPMC_ECC_CONFIG[16] ECCALGORITHM bit:

1. Hamming code for 1-bit error code correction on 8- or 16-bit NAND flash organized with page size greater than 512 bytes
2. Bose-Chaudhurl-Hocquenghem (BCH) code for 4- to 16-bit error correction

The GPMC does not handle the error code correction directly. During writes, the GPMC computes parity bits. During reads, the GPMC provides enough information for the processor to correct errors without reading the data buffer all over again.

The Hamming code ECC is based on a 2-dimensional (2D) (row and column) bit parity accumulation. This parity accumulation is accomplished on the programmed number of bytes or 16-bit words read from the memory device, or is written to the memory device in stream mode.

Because the ECC engine includes only one accumulation context, it can be allocated to only one chip-select at a time through the GPMC_ECC_CONFIG[3:1] ECCCS bit field. Even if two chip-selects use different ECC algorithms, one the Hamming code and the other a BCH code, they must define separate ECC contexts because some of the ECC registers are common to all types of algorithms.

15.4.4.13.3.1 Hamming Code

All references to ECC in this subsection refer to the 1-bit error correction Hamming code.

The ECC is based on a 2D (row and column) bit parity accumulation known as the Hamming code. The parity accumulation is done for a programmed number of bytes or 16-bit word read from the memory device or written to the memory device in stream mode.

There is no automatic error detection or correction, and the software NAND driver must read the multiple ECC calculation results, compare them to the expected code value, and take the appropriate corrective actions according to the error handling strategy (ECC storage in spare byte, error correction on read, block invalidation).

The ECC engine includes a single accumulation context. It can be allocated to a single designated chip-select at a time, and parallel computations on different chip-selects are not possible. Because it is allocated to a single chip-select, the ECC computation is not affected by interleaved GPMC accesses to other chip-selects and devices. The ECC accumulation is sequentially processed in the order of data read from or written to the memory on the designated chip-select. The ECC engine does not differentiate read accesses from write accesses and does not differentiate data from command or status information. Software must ensure that only relevant data are passed to the NAND flash memory while the ECC computation engine is active.

The starting NAND page location must be programmed first, followed by an ECC accumulation context reset with an ECC enabling, if required. The NAND device accesses discussed in the following sections must be limited to data read or write until the specified number of ECC calculations is complete.

15.4.4.13.3.1.1 ECC Result Register and ECC Computation Accumulation Size

The GPMC includes up to nine ECC result registers (GPMC_ECCj_RESULT, where j = 1 to 9) to store ECC computation results when the specified number of bytes or 16-bit words has been computed.

The ECC result registers are used sequentially: one ECC result is stored in one ECC result register on the list, the next ECC result is stored in the next ECC result register on the list, and so forth, until the last ECC computation. The value of the GPMC_ECCj_RESULT register is valid only when the programmed number of bytes or 16-bit words has been accumulated, which means that the same number of bytes or 16-bit words has been read from or written to the NAND device in sequence.

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The GPMC_ECC_CONTROL[3:0] ECCPOINTER bit field must be set to the correct value to select the ECC result register to be used first in the list for the incoming ECC computation process. The ECCPointer can be read to determine which ECC register is used in the next ECC result storage for the ongoing ECC computation. The value of the GPMC_ECCj_RESULT register (where j = 1 to 9) can be considered valid when ECCPOINTER equals j + 1. When the GPMC_ECCj_RESULT register (where j = 9) is updated, ECCPOINTER is frozen at 10, and ECC computing is stopped (ECCENABLE = 0).

The ECC accumulator must be reset before any ECC computation accumulation process. The GPMC_ECC_CONTROL[8] ECCCLEAR bit must be set to 1 (nonpersistent bit) to clear the accumulator and all ECC result registers.

For each ECC result (each GPMC_ECCj_RESULT register, where j = 1 to 9), the number of bytes or 16-bit words used for ECC computing accumulation can be selected from between two programmable values.

The ECCjRESULTSIZE bits (where j = 1 to 9) in the GPMC_ECC_SIZE_CONFIG register select which programmable size value (ECCSIZE0 or ECCSIZE1) must be used for this ECC result (stored in the GPMC_ECCj_RESULT register).

The ECCSIZE0 and ECCSIZE1 bit fields allow selection of the number of bytes or 16-bit words used for ECC computation accumulation. Any even values from 2 to 512 are allowed.

Flexibility in the number of ECCs computed and the number of bytes or 16-bit words used in the successive ECC computations enables different NAND page error-correction strategies. Usually based on 256 or 512 bytes and on 128 or 256 16-bit word, the number of ECC results required is a function of the NAND device page size. Specific ECC accumulation size can be used when computing the ECC on the NAND spare byte.

For example, with a 2-KiB data page, 8-bit-wide NAND device, eight ECCs accumulated on 256 bytes can be computed and added to one extra ECC computed on the 24 spare bytes area where the eight ECC results used for comparison and correction with the computed data page ECC are stored. The GPMC then provides nine GPMC_ECCj_RESULT registers (j = 1 to 9) to store the results. In this case, ECCSIZE0 is set to 256, and ECCSIZE1 is set to 24; the ECC[1:8] RESULTSIZE bits are set to 0, and the ECC9RESULTSIZE bit is set to 1.

15.4.4.13.3.1.2 ECC Enabling

The GPMC_ECC_CONFIG[3:1] ECCCS bit field selects the allocated chip-select. The GPMC_ECC_CONFIG[0] ECCENABLE bit enables ECC computation on the next detected read or write access to the selected chip-select.

The following fields must not be changed or cleared while an ECC computation is in progress:

- CCPOINTER
- ECCCLEAR
- ECCSIZE
- ECCjRESULTSIZE (where j = 1 to 9)
- ECC16B
- ECCCS

The ECC accumulator and ECC result register must not be changed or cleared while an ECC computation is in progress.

Table 15-344 describes the ECC enable settings.

Table 15-344. ECC Enable Settings

Bit Field	Register	Value	Comments
ECCCS	GPMC_ECC_CONFIG	0–3	Selects the chip-select where ECC is computed
ECC16B	GPMC_ECC_CONFIG	0/1	Selects column number for ECC calculation
ECCCLEAR	GPMC_ECC_CONTROL	0–7	Clears all ECC result registers
ECCPOINTER	GPMC_ECC_CONTROL	0–7	A write to this bit field selects the ECC result register where the first ECC computation is stored. Set to 1 by default.

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Table 15-344. ECC Enable Settings (continued)

Bit Field	Register	Value	Comments
ECCSIZE1	GPMC_ECC_SIZE_CONFIG	0x00–0xFF	Defines ECCSIZE1
ECCSIZE0	GPMC_ECC_SIZE_CONFIG	0x00–0xFF	Defines ECCSIZE0
ECCjRESULTSIZE (j from 1 to 9)	GPMC_ECC_SIZE_CONFIG	0/1	Selects the size of ECCn result register
ECCENABLE	GPMC_ECC_CONFIG	1	Enables the ECC computation

15.4.4.13.3.1.3 ECC Computation

The ECC algorithm is a multiple parity bit accumulation computed on the odd and even bit streams extracted from the byte or Word16 streams. The parity accumulation is split into row and column accumulations, as shown in Figure 15-81 and Figure 15-82. The intermediate row and column parities are used to compute the upper level row and column parities. Only the final computation of each parity bit is used for ECC comparison and correction.

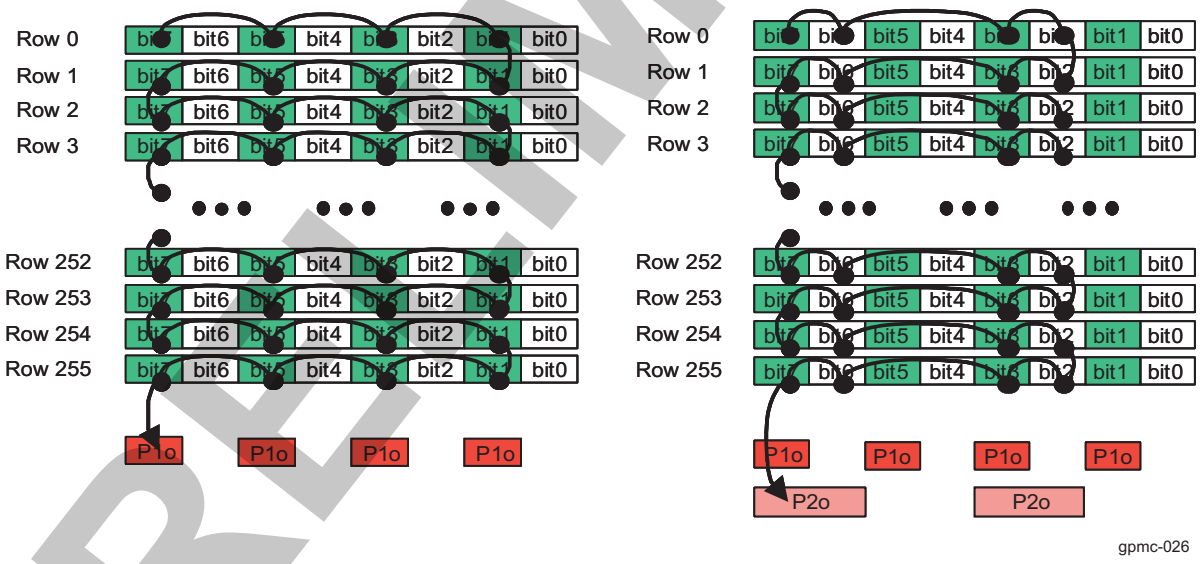
P1o = bit7 XOR bit5 XOR bit3 XOR bit1 on each byte of the data stream
P1e = bit6 XOR bit4 XOR bit2 XOR bit0 on each byte of the data stream

P2o = bit7 XOR bit6 XOR bit3 XOR bit2 on each byte of the data stream
P2e = bit5 XOR bit4 XOR bit1 XOR bit0 on each byte of the data stream

P4o = bit7 XOR bit6 XOR bit5 XOR bit4 on each byte of the data stream
P4e = bit3 XOR bit2 XOR bit1 XOR bit0 on each byte of the data stream

Each column parity bit is XORed with the previous accumulated value.

Figure 15-81. Hamming Code Accumulation Algorithm (1/2)



For line parities, the bits of each new data are XORed together, and line parity bits are computed as described below:

P8e = row0 XOR row2 XOR row4 XOR ... XOR row254
P8o = row1 XOR row3 XOR row5 XOR ... XOR row255

P16e = row0 XOR row1 XOR row4 XOR row5 XOR ... XOR row252 XOR row 253
P16o = row2 XOR row3 XOR row6 XOR row7 XOR ... XOR row254 XOR row 255

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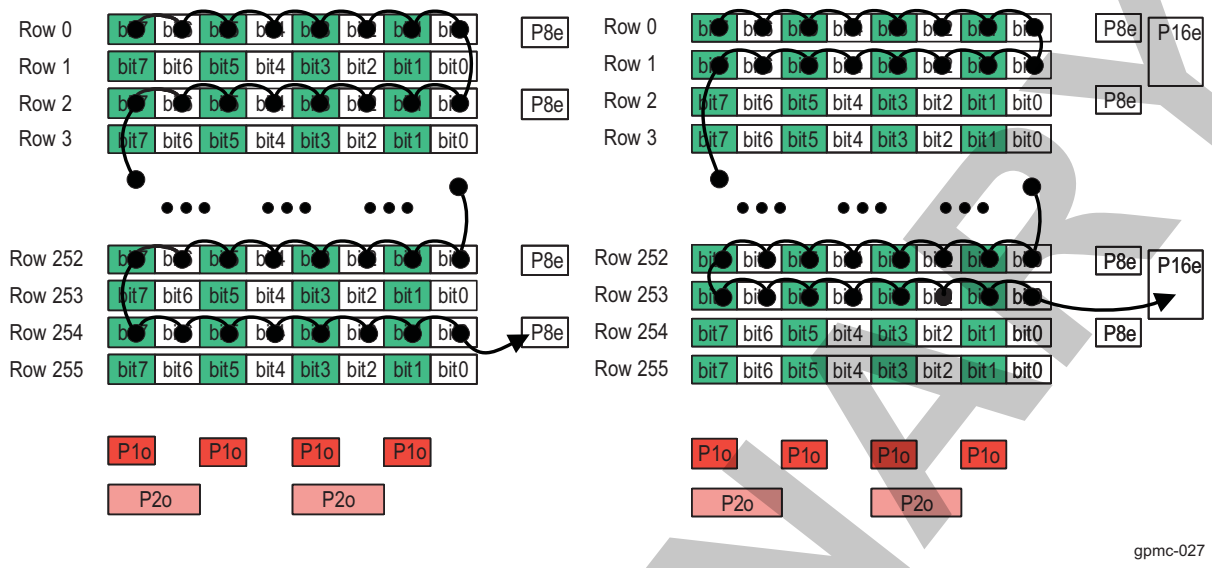
Figure 15-82. Hamming Code Accumulation Algorithm (2/2)



Unused parity bits in the result registers are set to 0.

Figure 15-83 shows ECC computation for a 256-byte data stream (read or write). The result includes six column parity bits (P1o-P2o-P4o for odd parities, and P1e-P2e-P4e for even parities) and sixteen row parity bits (P8o-P16o-P32o--P1024o for odd parities, and P8e-P16e-P32e--P1024e for even parities).

Figure 15-83. ECC Computation for a 256-Byte Data Stream (Read or Write)

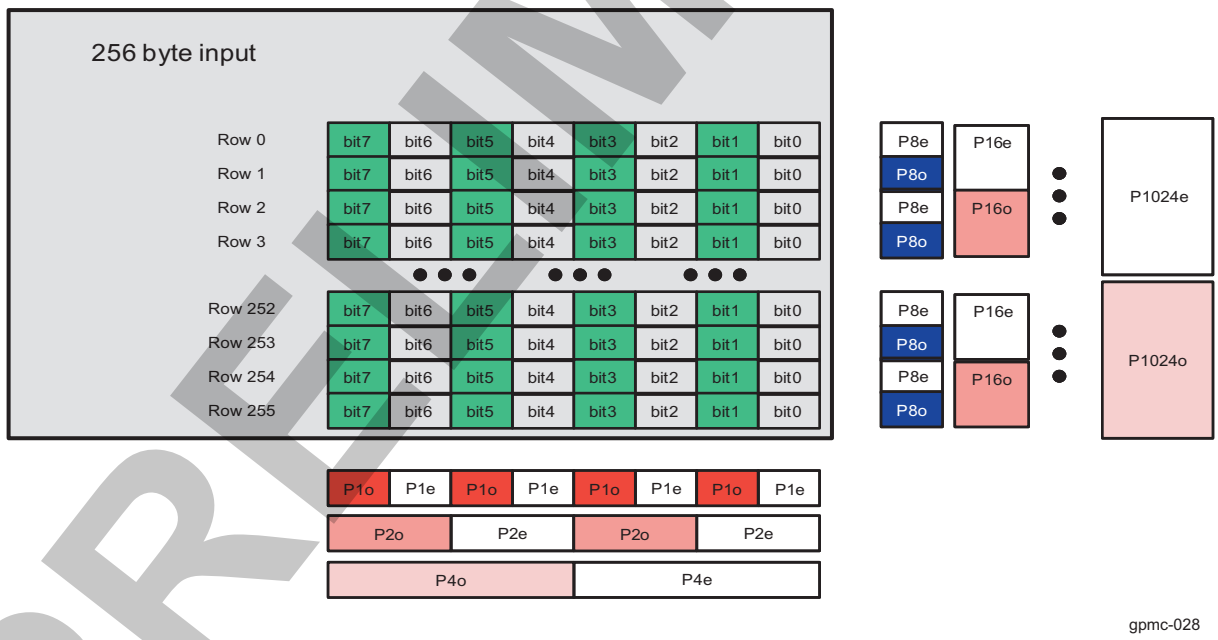


Figure 15-84 shows ECC computation for a 512-byte data stream (read or write). The result includes six column parity bits (P1o-P2o-P4o for odd parities, and P1e-P2e-P4e for even parities) and eighteen row parity bits (P8o-P16o-P32o--P1024o- - P2048o for odd parities, and P8e-P16e-P32e--P1024e- P2048e for even parities).

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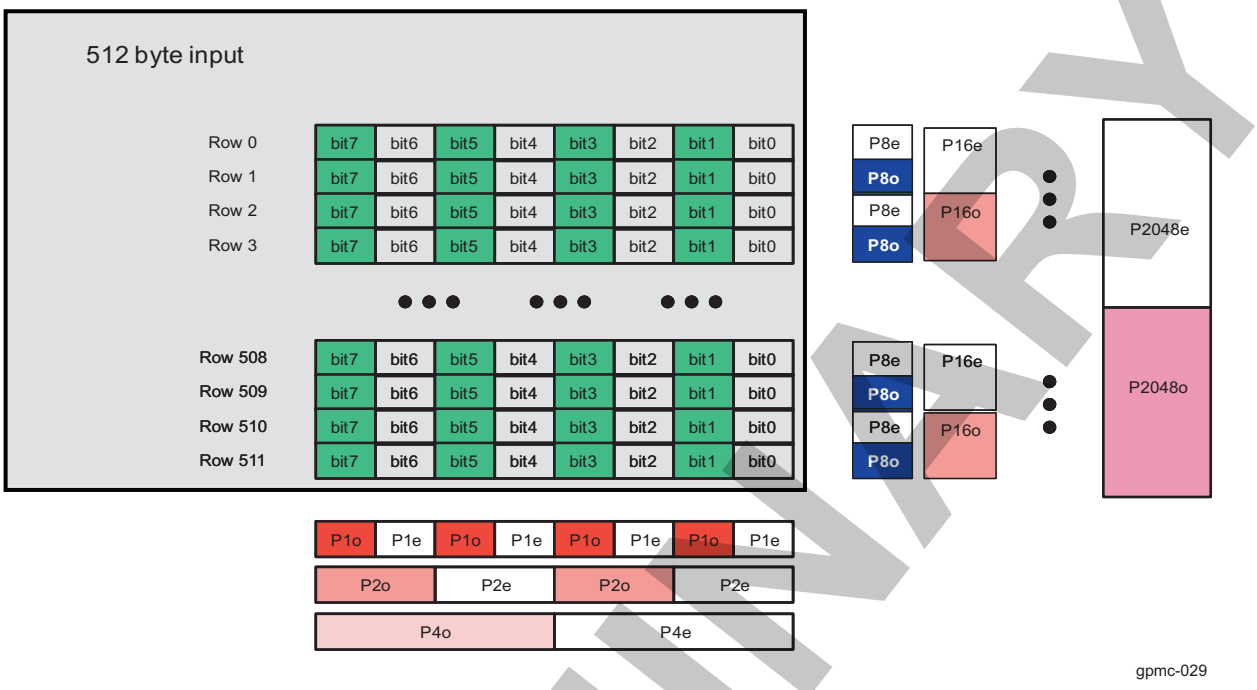
Figure 15-84. ECC Computation for a 512-Byte Data Stream (Read or Write)



For a 2-KiB page, four 512 bytes ECC calculations plus 1 for the spare area are required. Results are stored in the GPMC_ECCj_RESULT registers (where j = 1 to 9).

15.4.4.13.3.1.4 ECC Comparison and Correction

To detect an error, the computed ECC result must be XORed with the parity value stored in the spare area of the accessed page.

- If the result of this logical XOR is all 0s, no error is detected and the read data is correct.
- If every second bit in the parity result is a 1, 1 bit is corrupted and is located at bit address (P2048o, P1024o, P512o, P256o, P128o, P64o, P32o, P16o, P8o, P4o, P2o, P1o). Software must correct the corresponding bit.
- If only 1 bit in the parity result is 1, it is an ECC error and the read data is correct.

15.4.4.13.3.1.5 ECC Calculation Based on 8-Bit Word

The 8-bit-based ECC computation is used for 8-bit-wide NAND device interfacing.

The 8-bit-based ECC computation can be used for 16-bit-wide NAND device interfacing to get backward compatibility on the error-handling strategy used with 8-bit-wide NAND devices. In this case, the 16-bit-wide data read from or written to the NAND device is fragmented into 2 bytes. According to little-endian access, the LSB of the 16-bit-wide data is ordered first in the byte stream used for 8-bit-based ECC computation.

15.4.4.13.3.1.6 ECC Calculation Based on 16-Bit Word

ECC computation based on an 16-bit word is used for 16-bit-wide NAND device interfacing. This ECC computation is not supported when interfacing an 8-bit-wide NAND device, and the GPMC_ECC_CONFIG[7] ECC16B bit must be set to 0 when interfacing an 8-bit-wide NAND device.

The parity computation based on 16-bit words affects the row and column parity mapping. The main difference is that the odd and even parity bits P8o and P8e are computed on rows for an 8-bit-based ECC and on columns for a 16-bit based ECC. Figure 15-85 and Figure 15-86 show a 128 Word16 ECC computation scheme and a 256 16-bit word ECC computation scheme.

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Figure 15-85. 128 Word16 ECC Computation

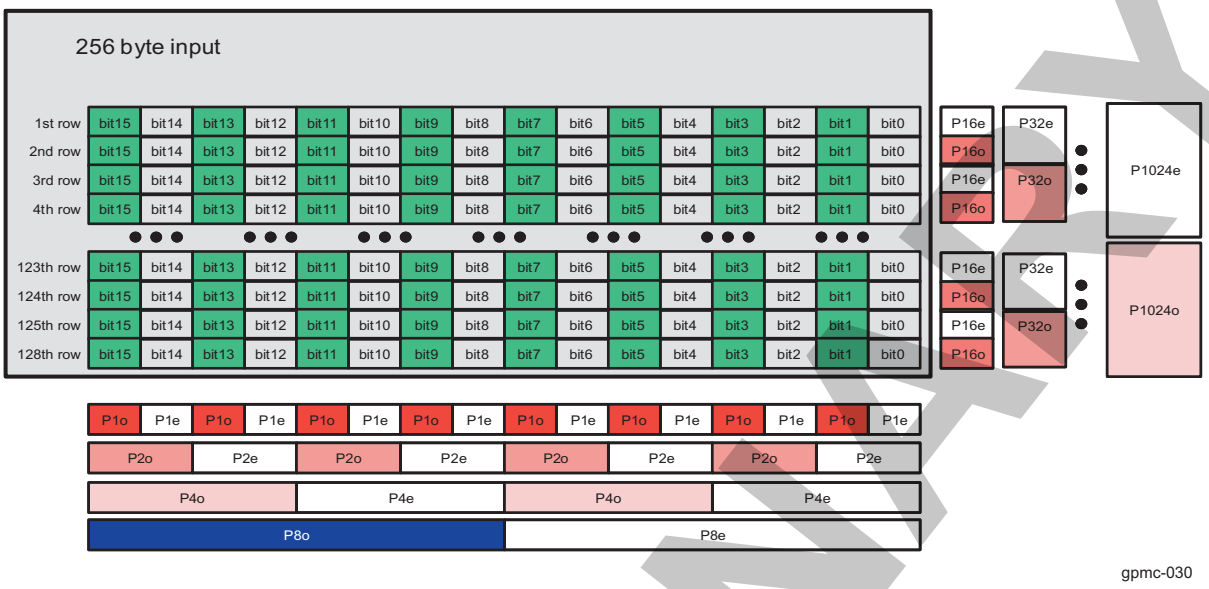
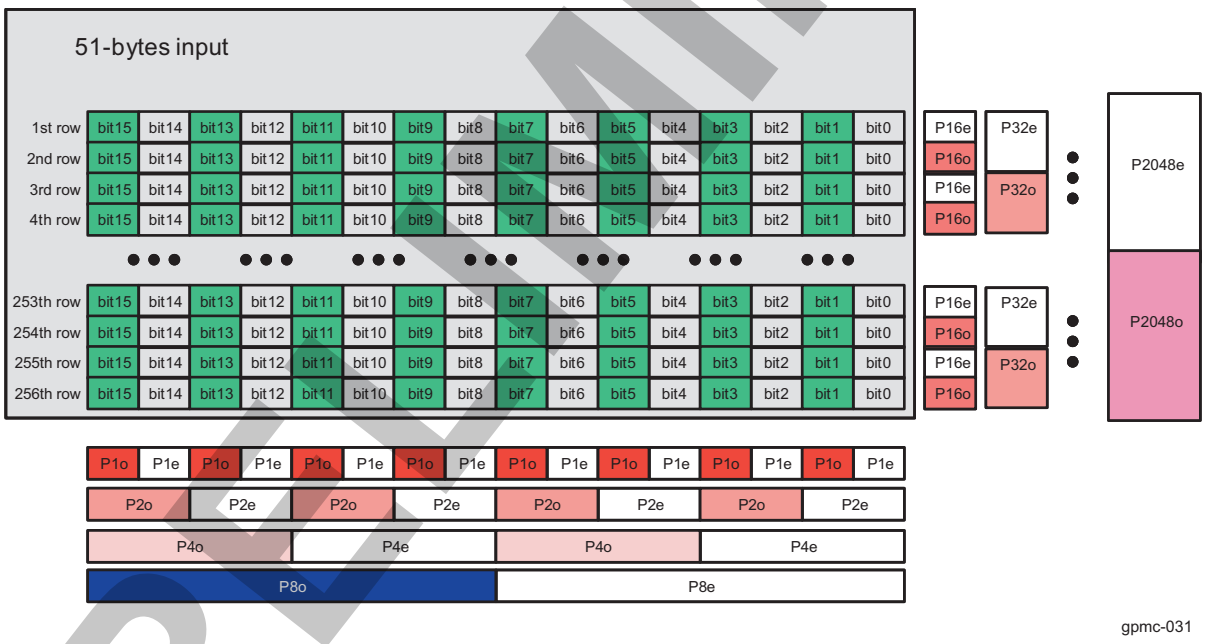


Figure 15-86. 256 Word16 ECC Computation



15.4.4.13.3.2 BCH Code

All references to ECC in this subsection refer to the 4- to 16-bit error correction BCH code.

15.4.4.13.3.2.1 Requirements

1. Read and write accesses to a NAND flash take place by whole pages, in a predetermined sequence: first the data byte page itself, and then some spare bytes, including the BCH ECC (and other information). The NAND device can cache a full page, including spares, for read and write accesses.
   - Typical page write sequence:
     - Sequential write to NAND cache of main data plus spare data, for a page. ECC is calculated on the fly. Calculated ECC can be inserted on the fly in the spares or replaced by dummy

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accesses.
  - When the calculated ECC is replaced by dummy accesses, it must be written to the cache in a second, separate phase. The ECC module is disabled during that time.
  - NAND writes its cache line (page) to the array.
- Typical page read sequence:
  - Sequential read of a page. ECC is calculated on the fly.
  - The status of the ECC module buffers determines the presence of errors.

2. Accesses to several memories can be interleaved by the GPMC, but only one of those memories at a time can be a NAND using the BCH engine; in other words, only one BCH calculation (for example, for a single page) can be ongoing at any time. The sequential nature of NAND accesses ensures that the data is always written or read out in the same order. BCH-relevant accesses are selected by the chip-selects of the GPMC.
3. Each page can hold up to 4KiB of data, spare bytes not included. This means up to 8 × 512-byte BCH messages. Because all the data is written or read out first, followed by the BCH ECC, the BCH engine must be able to hold eight 104-bit remainders or syndromes (or smaller, 52-bit ones) at the same time.

   The BCH module can store all remainders internally. After the page start, an internal counter is used to detect the 512-byte sector boundaries. On those boundaries, the current remainder is stored and the divider reset for the next calculation. At the end of the page, the BCH module contains all remainders.
4. NAND access cycles hold 8 or 16 bits of data each (1 or 2 bytes); Each NAND cycle takes at least four cycles of the GPMC internal clock. This means the NAND flash timing parameters must define a RDCYCLETIME and a WRCYCLETIME of at least four clock cycles after optimization when using the BCH calculator.
5. The spare area is assumed to be large enough to hold the BCH ECC; that is, to have a message of at least 13 bytes available per 512-byte sector of data. The zone of unused spare area by the ECC may or may not be protected by the same ECC scheme, by extending the BCH message beyond 512 bytes (the maximum codeword is 1023 bytes long, ECC included, which leaves much space to cover spare bytes).

15.4.4.13.3.2.2 Memory Mapping of BCH Codeword

BCH encoding considers a block of data to protect as a polynomial message M(x). In a standard case, 512 bytes of data (that is, 2^{12} bits = 4096 bits) are seen as a polynomial of degree $2^{12} – 1 = 4095$, with parameters ranging from M0 to M4095. For 512 bytes of data, 52 bits are required for 4-bit error correction, 104 bits are required for 8-bit error correction, and 207 bits are required for 16-bit error correction. The ECC is a remainder polynomial R(x) of degree 103 (or 51, depending on the selected mode). The complete codeword C(x) is the concatenation of M(x) and R(x), as described in Table 15-345.

Table 15-345. Flattened BCH Codeword Mapping (512 Bytes + 104 Bits)

	Message M(x)			ECC R(x)		
Bit Number	M4095	...	M0	R103	...	R0

If the message is extended by the addition of spare bytes to be protected by the same ECC, the principle is still valid. For example, a 3-byte extension of the message gives a polynomial message M(x) of degree ((512 + 3) × 8) – 1 = 4119, for a total of 3 + 13 = 16 spare bytes of spare, all protected as part of the same codeword.

The message and the ECC bits are manipulated and mapped in the GPMC byte-oriented system. The ECC bits are stored in the following registers (where i = 0 to 7):

- GPMC_BCH_RESULT0_i
- GPMC_BCH_RESULT1_i
- GPMC_BCH_RESULT2_i
- GPMC_BCH_RESULT3_i

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15.4.4.13.3.2.2.1 Memory Mapping of Data Message

The data message mapping must follow the following rules:

- Bit endianness within a byte is little-endian; that is, the bytes LSB is also the lowest-degree polynomial parameter: a byte b7-b0 (with b0 the LSB) represents a segment of polynomial b7 * $x^{(7+i)}$ + b6 * $x^{(6+i)}$ + ... + b0 * x^{i}
- The message is mapped in the NAND starting with the highest-order parameters, that is, in the lowest addresses of a NAND page.
- Byte endianness within the 16-bit words in the NAND is big-endian (that is, the same message mapped in 8- and 16-bit memories has the same content at the same byte address).

NOTE: The BCH module has no visibility over actual addresses. The most important point is the sequence of data words the BCH sees. However, the NAND page is always scanned incrementally in read and write accesses, which produces the mapping patterns described in the following.

Table 15-346 and Table 15-347 describe the mapping of the same 512-byte vector (typically, a BCH message) in the NAND memory space. The byte address is only an offset modulo 512 (0x200), because the same page may contain several contiguous 512-byte sectors (BCH blocks). The LSB and MSB are, respectively, the bits M0 and M(2^{12}–1) of the codeword mapping discussed previously. In both cases the data vectors are aligned; that is, their boundaries coincide with the RAM data word boundaries.

Table 15-346. Aligned Message Byte Mapping in 8-Bit NAND

Byte Offset	8-Bit Word
0x000	(MSB) Byte 511 (0x1FF)
0x001	Byte 510 (0x1FE)
...	...
0x1FF	Byte 0 (0x0) (LSB)

Table 15-347. Aligned Message Byte Mapping in 16-Bit NAND

Byte Offset	16-Bit Word MSB	16-Bit Word LSB
0x000	Byte 510 (0x1FE)	(MSB) Byte 511 (0x1FF)
0x002	Byte 508 (0x1FC)	Byte 509 (0x1FD)
...	...	...
0x1FE	Byte 0 (0x0)	(LSB) Byte 1 (0x1)

Table 15-348 through Table 15-353 list the mapping in memory of arbitrarily-sized messages, starting on access (byte or 16-bit word) boundaries for more clarity. Note that message may actually start and stop on arbitrary nibbles. A nibble is a 4-bit entity. The unused nibbles are not discarded, and they can still be used by the BCH module, but as part of the next message section (for example, on the ECC of another sector).

Table 15-348. Aligned Nibble Mapping of Message in 8-Bit NAND

Byte Offset	8-Bit Word	
	4-Bit Most Significant Nibble	4-Bit Least Significant Nibble
1	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-3	Nibble S-4
...	...	...
S/2 – 2	Nibble 3	Nibble 2
S/2 – 1	Nibble 1	Nibble 0 (LSB)

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Table 15-349. Misaligned Nibble Mapping of Message in 8-Bit NAND

Byte Offset	8-Bit Word	
	4-Bit Most Significant Nibble	4-Bit Least Significant Nibble
1	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-3	Nibble S-4
...	...	...
(S + 1) / 2 – 2	Nibble 2	Nibble 1
(S + 1) / 2 – 1	Nibble 0 (LSB)	

Table 15-350. Aligned Nibble Mapping of Message in 16-Bit NAND

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		4-Bit Least Significant Nibble	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
S/2 – 4	Nibble 5	Nibble 4	Nibble 7	Nibble 6
S/2 – 2	Nibble 1	Nibble 0 (LSB)	Nibble 3	Nibble 2

Table 15-351. Misaligned Nibble Mapping of Message in 16-Bit NAND (1 Unused Nibble)

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		4-Bit Least Significant Nibble	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S + 1) / 2 – 4	Nibble 4	Nibble 3	Nibble 6	Nibble 5
(S + 1) / 2 – 2	Nibble 0 (LSB)		Nibble 2	Nibble 1

Table 15-352. Misaligned Nibble Mapping of Message in 16-Bit NAND (2 Unused Nibbles)

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		4-Bit Least Significant Nibble	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S + 2) / 2 – 4	Nibble 3	Nibble 2	Nibble 5	Nibble 4
(S + 2) / 2 – 2			Nibble 1	Nibble 0 (LSB)

Table 15-353. Misaligned Nibble Mapping of Message in 16-Bit NAND (3 Unused Nibbles)

Byte Offset	16-Bit Word			
	4-Bit Most Significant Nibble		4-Bit Least Significant Nibble	
0	Nibble S-3	Nibble S-4	(MSB) Nibble S-1	Nibble S-2
2	Nibble S-7	Nibble S-8	Nibble S-5	Nibble S-6
...	...		...	
(S + 3) / 2 – 4	Nibble 2	Nibble 1	Nibble 4	Nibble 3
(S + 3) / 2 – 2			Nibble 0 (LSB)	

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Many other cases exist than those given in the previous tables; for example, where the message does not start on a word boundary.

15.4.4.13.3.2.2.2 Memory-Mapping of the ECC

The ECC (or remainder) is presented by the BCH module as a single 104-bit (or 52-bit), little-endian vector. Software must fetch those 13 bytes (or 6 bytes) from the module interface and then store them to the spare area (page write) in the NAND or to an intermediate buffer for comparison with the stored ECC (page read). There are no constraints on the ECC mapping inside the spare area: it is software-controlled.

It is advised, however, to maintain a coherence in the respective formats of the message or the ECC remainder once they have been read out of the NAND. The error correction algorithm works from the complete codeword (concatenated message and remainder) once an error is detected. The creation of this codeword must be made as straightforward as possible.

There are cases in which the same NAND access contains both data and the ECC protecting that data. This is the case when the data/ECC boundary (which can be on any nibble) does not coincide with an access boundary. The ECC is calculated on the fly following the write. In that case, the write must also contain part of the ECC because it is impossible to insert the ECC on the fly. Instead:

- During the initial page write (BCH encoding), the ECC is replaced by dummy bits. The BCH encoder is by definition turned OFF during the ECC section, so the BCH result is unmodified.
- During a second phase, the ECC is written to the correct location, next to the actual data.
- The completed line buffer is then written to the NAND array.

15.4.4.13.3.2.2.3 Wrapping Modes

For a given wrapping mode, the module automatically goes through a specific number of sections as data is being fed into the module. For each section, the BCH core can be enabled (in which case the data is fed to the BCH divider) or not (in which case the BCH simply counts to the end of the section). When enabled, the data is added to the ongoing calculation for a given sector number (for example, number 0).

Wrapping modes are described as follows. To better understand and see the real-life read and write sequences implemented with each mode, see Section 15.4.4.13.3.2.3, *Supported NAND Page Mappings and ECC Schemes*.

For each mode:

- A sequence describes the mode in pseudo language, with, for each section, the size and the buffer used for ECC processing (if ON). The programmable lengths are size, size0, and size1.
- A checksum condition is given. If the checksum condition is not respected for a given mode, the module behavior is unpredictable. S is the number of sectors in the page; size0 and size1 are the section sizes programmed for the mode, in nibbles.

Wrapping modes 8 through 11 insert a 1-nibble padding where the BCH processing is OFF. This is intended for t = 4 ECC, where ECC is 6 bytes long and the ECC area is expected to include (at least) 1 unused nibble to remain byte-aligned.

15.4.4.13.3.2.2.4 Manual Mode (0x0)

This mode is intended for short sequences, added manually to a given buffer through the software data port input. A complete page may be built out of several such sequences.

To process an arbitrary sequence of 4-bit nibbles, accesses to the software data port, containing the appropriate data, must be made. If the sequence end does not coincide with an access boundary (for example, to process 5 nibbles = 20 bits in 16-bit access mode) and those nibbles must be skipped, a number of unused nibbles must be programmed in GPMC_ECC_SIZE_CONFIG[29:22] ECCSIZE1 In the same example, 5 nibbles to process + 3 to discard = 8 nibbles = 2 × 16-bit accesses. Software must set:

- GPMC_ECC_SIZE_CONFIG[19:12] ECCSIZE0 = 0x5
- GPMC_ECC_SIZE_CONFIG[29:22] ECCSIZE1 = 0x3

NOTE: In the following figures, size and size0 are the same parameter.

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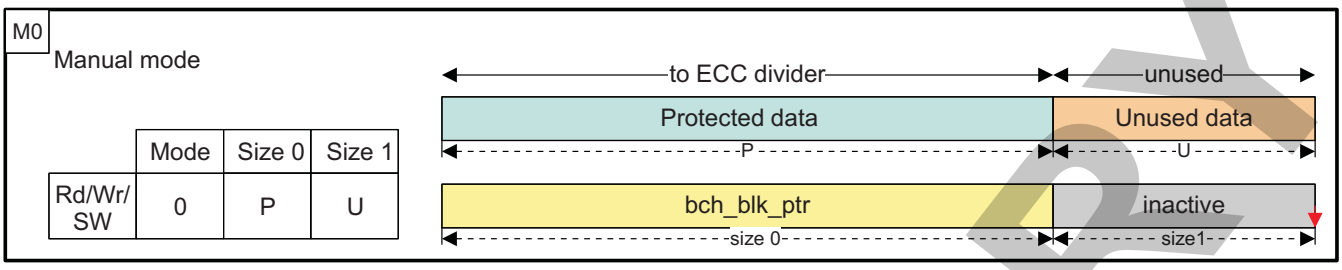
Figure 15-87. Manual Mode Sequence and Mapping



Section processing sequence:

- One time with buffer
  - size0 nibbles of data, processing ON
  - size1 nibbles of unused data, processing OFF

Checksum: size0 + size1 nibbles must fit in a whole number of accesses.

In the following sections, S is the number of sectors in the page.

15.4.4.13.3.2.2.5 Mode 0x1

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S – (size0 + size1)

15.4.4.13.3.2.2.6 Mode 0xA (10)

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
  - 1 nibble pad spare, processing OFF
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S – (size0 + 1 + size1)

15.4.4.13.3.2.2.7 Mode 0x2

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S – (size0 + size1)

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15.4.4.13.3.2.2.8 Mode 0x3

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – size1)

15.4.4.13.3.2.2.9 Mode 0x7

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat S times (no buffer used)
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = size0 + (S – size1)

15.4.4.13.3.2.2.10 Mode 0x8

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time with buffer 0
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – (1 + size1))

15.4.4.13.3.2.2.11 Mode 0x4

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- One time (no buffer used)
  - size0 nibbles spare, processing OFF
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – size1)

15.4.4.13.3.2.2.12 Mode 0x9

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON

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- One time (no buffer used)
  - size0 nibbles spare, processing OFF
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = size0 + (S – (1 + size1))

15.4.4.13.3.2.2.13 Mode 0x5

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S – (size0 + size1)

15.4.4.13.3.2.2.14 Mode 0xB (11)

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat with buffer 0 to S-1
  - 1 nibble padding spare, processing OFF
  - size1 nibbles spare, processing ON

Checksum: Spare area size (nibbles) = S – (size0 + 1 + size1)

15.4.4.13.3.2.2.15 Mode 0x6

Page processing sequence:

- Repeat with buffer 0 to S-1
  - 512-byte data, processing ON
- Repeat with buffer 0 to S-1
  - size0 nibbles spare, processing ON
- Repeat S times (no buffer used)
  - size1 nibbles spare, processing OFF

Checksum: Spare area size (nibbles) = S – (size0 + size1)

15.4.4.13.3.2.3 Supported NAND Page Mappings and ECC Schemes

The following rules apply to the entire mapping description:

- Main data area (sectors) size is hardcoded to 512 bytes.
- Spare area size is programmable.
- All page sections (of main area data bytes, protected spare bytes, unprotected spare bytes, and ECC) are defined as explained in Section 15.4.4.13.3.2.2.1, *Memory Mapping of Data Message*.

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Each of the following sections gives a NAND page mapping example (per-sector spare mappings, pooled spare mapping, per-sector spare mapping, with ECC separated at the end of the page).

In the mapping diagrams, sections that belong to the same BCH codeword have the same color (blue or green); unprotected sections are not covered (orange) by the BCH scheme.

Below each mapping diagram, a write (encoding) and read (decoding: syndrome generation) sequence is given, with the number of the active buffers at each point in time (yellow). In the inactive zones (grey), no computing is taking place but the data counter is still active.

In Figure 15-88 through Figure 15-90, the tables on the left summarize the mode, size0, and size1 parameters to program for, respectively, write and read processing of a page, with the given mapping, where:

- P is the size of spare byte section Protected by the ECC (in nibbles)
- U is the size of spare byte section Unprotected by the ECC (in nibbles)
- E is the size of the ECC (in nibbles)
- S is the number of Sectors per page (two in the current diagrams)

Each time the processing of a BCH block is complete (ECC calculation for write/encoding, syndrome generation for read/decoding, indicated by red arrows), the update pointer is pulsed. The processing for block 0 can be the first or the last to complete, depending on the NAND page mapping and operation (read or write). All examples show a page size of 1 KiB + spares; that is, S = 2 sectors of 512 bytes. The same principles can be extended to larger pages by adding more sectors.

The actual BCH codeword size is used during the error location work to restrict the search range: by definition, errors can happen only in the codeword that was actually written to the NAND, not in the mathematical codeword of $n = 2^{13} - 1 = 8191$ bits; that codeword (higher-order bits) is all-zero and implicit during computations.

The actual BCH codeword size depends on the mode, the programmed sizes, and the sector number (all sizes in nibbles):

- Spares mapped and protected per sector (below: see M1-M2-M3-M9-M10):
  - All sectors: (512) + P + E
- Spares pooled and protected by sector 0 (below: see M5-M6):
  - Sector 0 codeword: (512) + P + E
  - Other sectors: (512) + E
- Unprotected spares (below: see M4-M7-M8-M11-M12):
  - All codewords (512) + E

15.4.4.13.3.2.3.1 Per-Sector Spare Mappings

In these schemes, each 512-byte sector of the main area has its own dedicated section of the spare area. The spare area of each sector is composed of:

- ECC, which must be located after the data it protects
- Other data, which may or may not be protected by the ECC for its sector.

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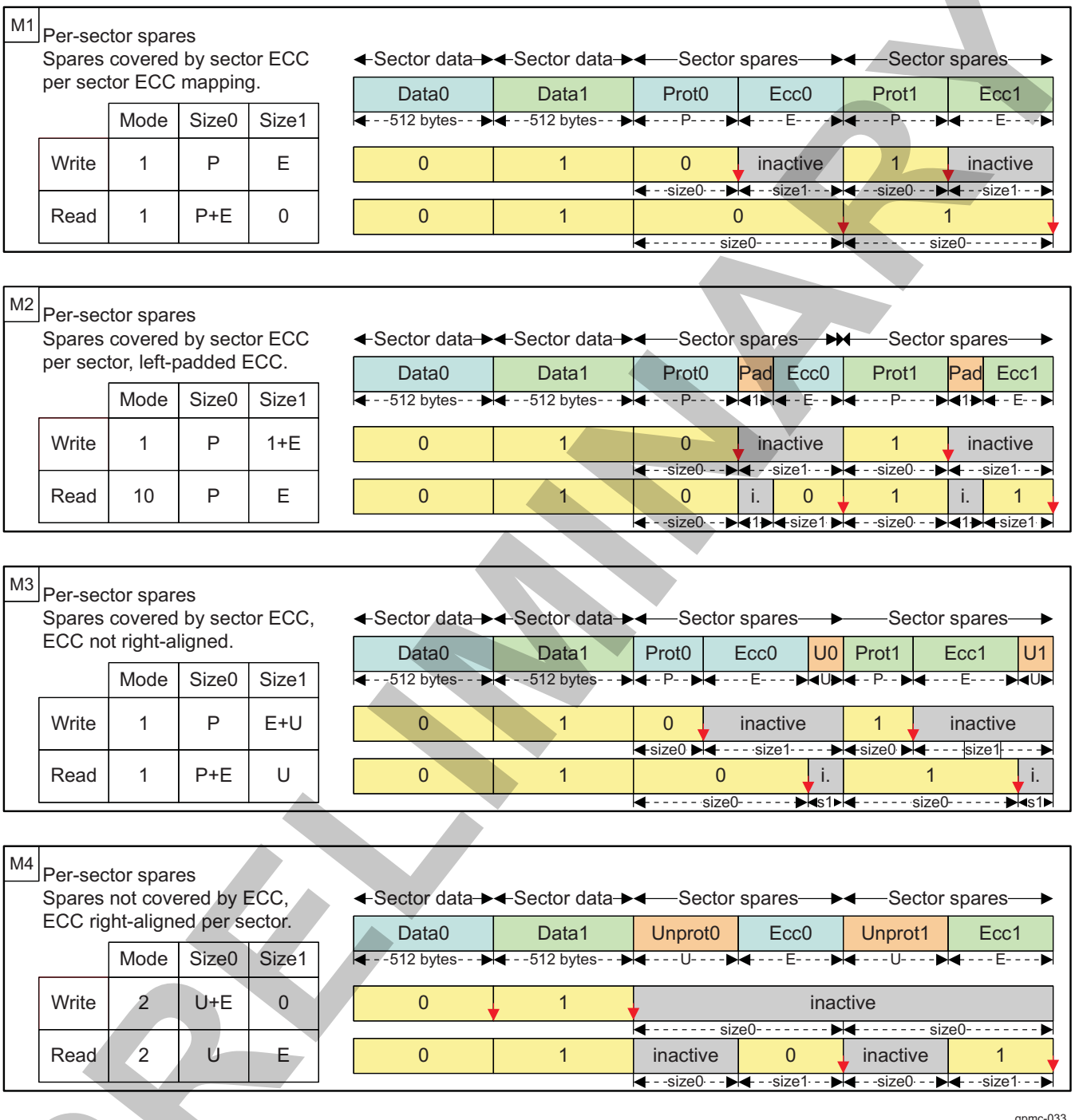
Figure 15-88. NAND Page Mapping and ECC: Per-Sector Schemes



gpmc-033

15.4.4.13.3.2.3.2 Pooled Spare Mapping

In the following schemes, the spare area is pooled for the page.

- The ECC of each sector is aligned at the end of the spare area.
- The non-ECC spare data may or may not be covered by the ECC of sector 0.

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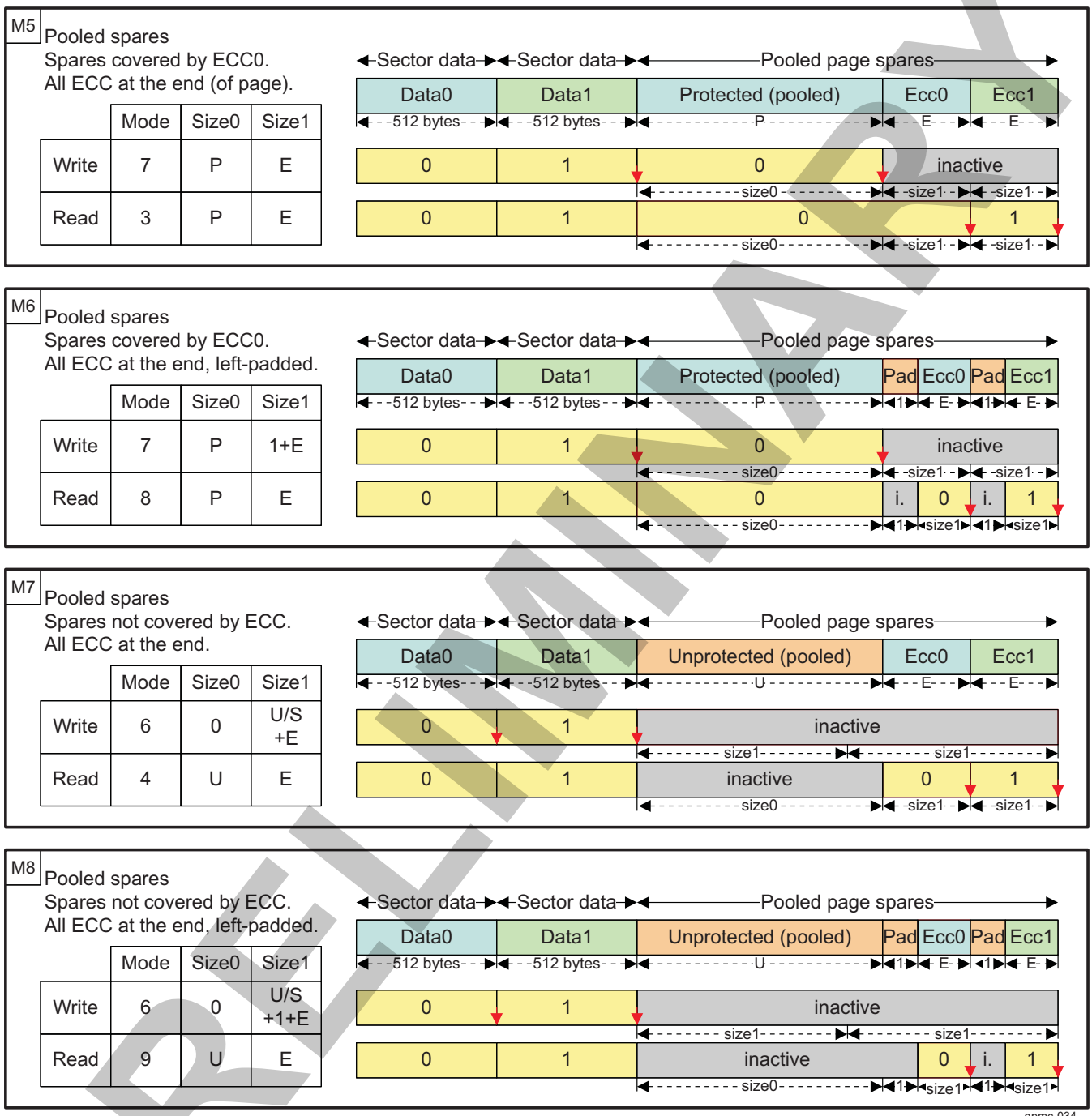
Figure 15-89. NAND Page Mapping and ECC: Pooled Spare Schemes



15.4.4.13.3.2.3.3 Per-Sector Spare Mapping, with ECC Separated at the End of the Page

In these schemes, each 512-byte sector of the main area is associated with two sections of the spare area.

- ECC section, all aligned at the end of the page
- Other data section, aligned before the ECCs, each of which may or may not be protected by the ECC for its sector.

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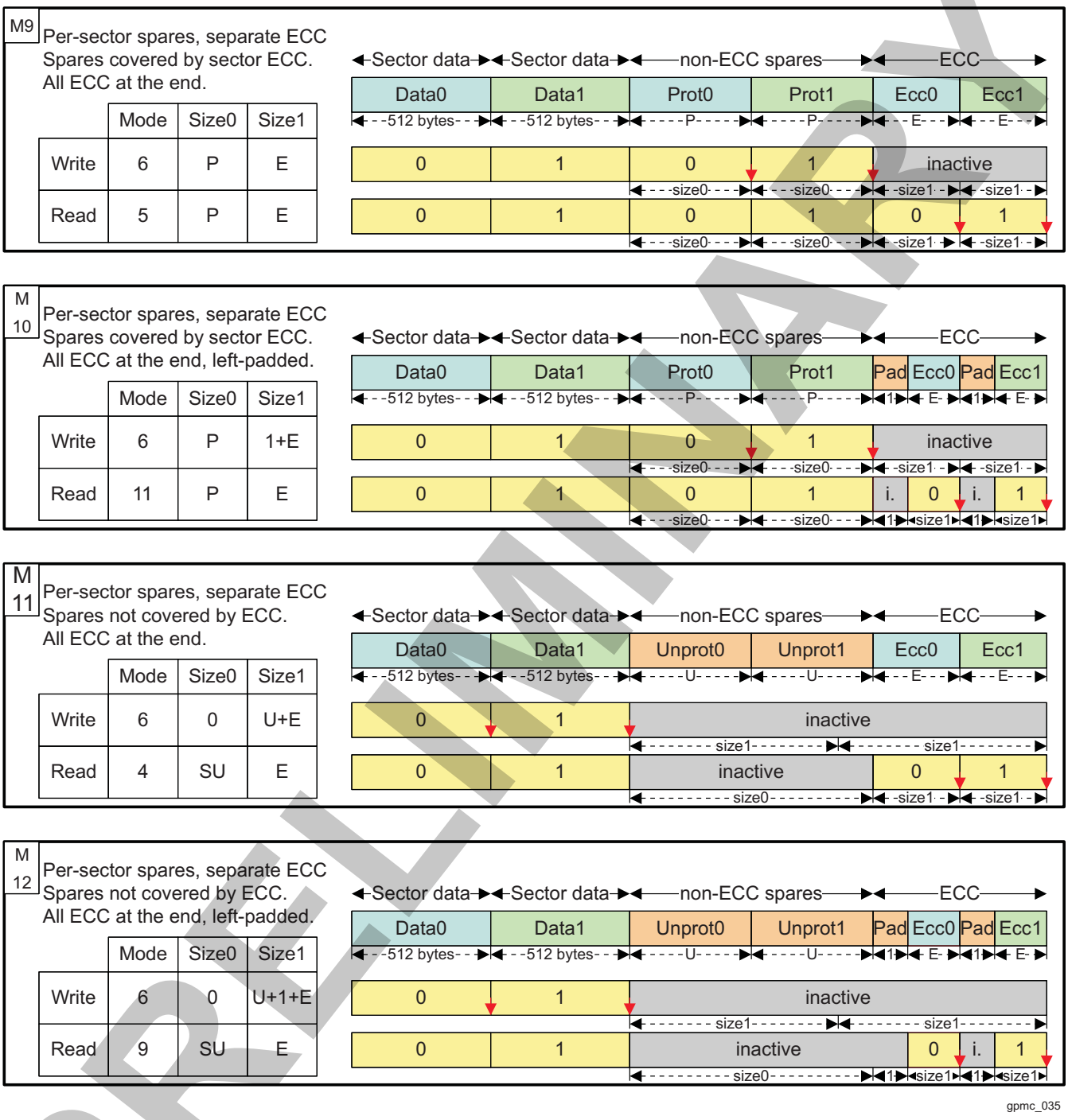
Figure 15-90. NAND Page Mapping and ECC: Per-Sector Schemes, With Separate ECC



15.4.4.13.4 Prefetch and Write-Posting Engine

NAND device data access cycles are usually much slower than the MPU system frequency; such NAND read or write accesses issued by the processor affect the overall system performance, especially considering long read or write sequences required for NAND page loading or programming. To minimize this effect on system performance, the GPMC includes a prefetch and write-posting engine, which can be used to read from or write to any chip-select location in a buffered manner.

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The prefetch and write-posting engine is a simplified embedded-access requester that presents requests to the access engine on a user-defined chip-select target. The access engine interleaves these requests with any request coming from the L3 interface; as a default, the prefetch and write-posting engine has the lowest priority.

The prefetch and write-posting engine is dedicated to data-stream access (as opposed to random data access); thus, it is primarily dedicated to NAND support. The engine does not include an address generator; the request is limited to chip-select target identification. It includes a 64-byte FIFO associated with a DMA request synchronization line, for optimal DMA-based use.

The prefetch and write-posting engine uses an embedded 64-byte (32 16-bit word) FIFO to prefetch data from the NAND device in read mode (prefetch mode) or to store host data to be programmed into the NAND device in write mode (write-posting mode). The FIFO draining and filling (read and write) can be controlled by the MPU through interrupt synchronization (an interrupt is triggered whenever a programmable threshold is reached) or by the sDMA through DMA request synchronization, with a programmable request byte size in prefetch or posting mode.

The prefetch and write-posting engine includes a single memory pool. Therefore, only one mode, read or write, can be used at any given time. In other words, the prefetch and write-posting engine is a single-context engine that can be allocated to only one chip-select at a time for a read prefetch or a write-posting process.

The engine does not support atomic command and address phase programming and is limited to linear memory read or write access. As a consequence, it is limited to NAND data-stream access. The engine relies on the MPU NAND software driver to control block and page opening with the correct data address pointer initialization, before the engine can read from or write to the NAND memory device.

Once started, engine data read and write sequencing is based solely on FIFO location availability and until the total programmed number of bytes is read or written.

Any host-concurrent accesses to a different chip-select are correctly interleaved with ongoing engine accesses. The engine has the lowest priority access so that host accesses to a different chip-select do not suffer a large latency.

A round-robin arbitration scheme can be enabled to ensure minimum bandwidth to the prefetch and write-posting engine in the case of back-to-back direct memory requests to a different chip-select. If the GPMC_PREFETCH_CONFIG1[23] PFPWENROUNDROBIN bit is enabled, the arbitration grants the prefetch and write posting engine access to the GPMC bus for a number of requests programmed in the GPMC_PREFETCH_CONFIG1[19:16] PFPWWEIGHTEDPRIO bit field.

The prefetch/write-posting engine read or write request is routed to the access engine with the chip-select destination ID. After the required arbitration phase, the access engine processes the request as a single access with the data access size equal to the device size specified in the corresponding chip-select configuration.

NOTE: The destination chip-select configuration must be set to the NAND protocol-compatible configuration for which address lines are not used (the address bus is not changed from its current value). Selecting a different chip-select configuration can produce undefined behavior.

15.4.4.13.4.1 General Facts About the Engine Configuration

The engine can be configured only if the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit is deasserted.

The engine must be correctly configured in prefetch or write-posting mode and must be linked to a NAND chip-select before it can be started. The chip-select is linked using the GPMC_PREFETCH_CONFIG1[26:24] ENGINECSSELECTOR bit field.

In prefetch and write-posting modes, the engine uses byte or 16-bit word access requests, respectively, for an 8- or 16-bit-wide NAND device attached to the linked chip-select. The FIFOTHRESHOLD and TRANSFERCOUNT bit fields must be programmed accordingly as a number of bytes.

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When the GPMC_PREFETCH_CONFIG1[7] ENABLEENGINE bit is set, the FIFO entry on the L3 interconnect port side is accessible at any address in the associated chip-select memory region. When the ENABLEENGINE bit is set, any host access to this chip-select is rerouted to the FIFO input. Directly accessing the NAND device linked to this chip-select from the host is still possible through the following registers (where i = 0 to 7):

- GPMC_NAND_COMMAND_i
- GPMC_NAND_ADDRESS_i
- GPMC_NAND_DATA_i

The FIFO entry on the L3 interconnect port can be accessed with byte, 16-bit word, or 32-bit word access size, according to little-endian format, even though the FIFO input is 32 bits wide.

The FIFO control is made easier through the use of interrupts or DMA requests associated with the FIFOTHRESHOLD bit field. The GPMC_PREFETCH_STATUS[30:24] FIFOPOINTER bit field monitors the number of available bytes to be read in prefetch mode or the number of free empty slots that can be written in write-posting mode. The GPMC_PREFETCH_STATUS[13:0] COUNTVALUE bit field monitors the number of remaining bytes to be read or written by the engine according to the value of the TRANSFERCOUNT bit field. The FIFOPOINTER and COUNTVALUE bit fields are always expressed as a number of bytes even if a 16-bit-wide NAND device is attached to the linked chip-select.

In prefetch mode, when the FIFOPOINTER equals 0 (that is, the FIFO is empty), a host read access receives the byte last read from the FIFO as its response. In case of 32-bit word or 16-bit word read accesses, the last byte read from the FIFO is copied the required number of times to fit the requested word size. In write-posting mode, when the FIFOPOINTER equals 0 (that is, the FIFO is full), a host write overwrites the last FIFO byte location. There is no underflow or overflow error reporting in the GPMC.

15.4.4.13.4.2 Prefetch Mode

The prefetch mode is selected when the GPMC_PREFETCH_CONFIG1[0] ACCESSMODE bit is cleared.

The MPU NAND software driver must issue the block and page opening (READ) command with the correct data address pointer initialization before the engine can be started to read from the NAND memory device. The engine is started by asserting the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit. The STARTENGINE bit automatically clears when the prefetch process completes.

If required, the ECC calculator engine must be initialized (that is, reset, configured, and enabled) before the prefetch engine is started so that the ECC is computed correctly on all data read by the prefetch engine.

When the GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE bit is cleared, the prefetch engine starts requesting data as soon as the STARTENGINE bit is set. If using this configuration, the host must monitor the NAND device-ready pin so that it sets the STARTENGINE bit only when the NAND device is in a ready state (that is, data is valid for prefetching).

When the SYNCHROMODE bit is set, the prefetch engine starts requesting data when an active-to-inactive WAIT signal transition is detected. The transition detector must be cleared before any transition detection (see Section 15.4.4.13.2.2, *Ready Pin Monitored by Hardware Interrupt*). The GPMC_PREFETCH_CONFIG1[5:4] WAITPINSELECTOR bit field selects which gpmc_wait pin edge detector triggers the prefetch engine in this synchronized mode.

If the STARTENGINE bit is set after the NAND address phase (page opening command), the engine is effectively started only after the actual NAND address phase completion. To prevent GPMC stall during this NAND address phase, set the STARTENGINE bit before NAND address phase completion when in synchronized mode. The prefetch engine starts when an active-to-inactive WAIT signal transition is detected. The STARTENGINE bit is automatically cleared on prefetch process completion.

The prefetch engine issues a read request to fill the FIFO with the amount of data specified by the GPMC_PREFETCH_CONFIG2[13:0] TRANSFERCOUNT bit field.

Table 15-354 describes the prefetch mode configuration.

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Table 15-354. Prefetch Mode Configuration

Bit Field	Register	Value	Comments
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	0	Prefetch engine can be configured only if STARTENGINE is set to 0.
ENGINECSSELECTOR	GPMC_PREFETCH_CONFIG1[26:24]	0 to 3	Selects the chip-select associated with a NAND device where the prefetch engine is active.
ACCESSMODE	GPMC_PREFETCH_CONFIG1[0]	0	Selects prefetch mode
FIFOTHRESHOLD	GPMC_PREFETCH_CONFIG1[14:8]		Selects the maximum number of bytes read or written by the host on DMA or interrupt request
TRANSFERCOUNT	GPMC_PREFETCH_CONFIG2[13:0]		Selects the number of bytes to be read or written by the engine to the selected chip-select
SYNCHROMODE	GPMC_PREFETCH_CONFIG1[3]	0/1	Selects when the engine starts the access to the chip-select
WAITPINSELECT	GPMC_PREFETCH_CONFIG1[17:16]	0 to 1	Selects wait pin edge detector (if GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE = 0x1)
ENABLEOPTIMIZEDACCESS	GPMC_PREFETCH_CONFIG1[27]	0/1	See Section 15.4.4.13.4.6, *Optimizing NAND Access Using the Prefetch and Write-Posting Engine*.
CYCLEOPTIMIZATION	GPMC_PREFETCH_CONFIG1[30:28]		Number of clock cycle removed to timing parameters
ENABLEENGINE	GPMC_PREFETCH_CONFIG1[7]	1	Engine enabled
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	1	Starts the prefetch engine

15.4.4.13.4.3 FIFO Control in Prefetch Mode

The FIFO can be drained directly by the MPU or by an sDMA channel.

In MPU draining mode, the FIFO status can be monitored through the GPMC_PREFETCH_STATUS[30:24] FIFOPOINTER bit field or through the GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bit. The FIFOPOINTER indicates the current number of available data to be read; FIFOTHRESHOLDSTATUS set to 1 indicates that at least FIFOTHRESHOLD bytes are available from the FIFO.

An interrupt can be triggered by the GPMC if the GPMC_IRQENABLE[0] FIFOEVENTENABLE bit is set. The FIFO interrupt event is logged, and the GPMC_IRQSTATUS[0] FIFOEVENTSTATUS bit is set. To clear the interrupt, the MPU must read all the available bytes, or at least enough bytes to get below the programmed FIFO threshold, and the FIFOEVENTSTATUS bit must be cleared to enable further interrupt events. The FIFOEVENTSTATUS bit must always be reset before asserting the FIFOEVENTENABLE bit to clear any out-of-date logged interrupt event. This interrupt generation must be enabled after enabling the STARTENGINE bit.

Prefetch completion can be monitored through the GPMC_PREFETCH_STATUS[13:0] COUNTVALUE bit field. COUNTVALUE indicates the number of currently remaining data to be requested according to the TRANSFERCOUNT value. An interrupt can be triggered by the GPMC when the prefetch process is complete (that is, COUNTVALUE equals 0) if the GPMC_IRQENABLE[1] TERMINALCOUNTEVENTENABLE bit is set. At prefetch completion, the TERMINALCOUNT interrupt event is also logged, and the GPMC_IRQSTATUS[1] TERMINALCOUNTSTATUS bit is set. To clear the interrupt, the MPU must clear the TERMINALCOUNTSTATUS bit. The TERMINALCOUNTSTATUS bit must always be cleared prior to asserting the TERMINALCOUNTEVENTENABLE bit to clear any out-of-date logged interrupt event.

NOTE: The COUNTVALUE value is valid only when the prefetch engine is active (started), and an interrupt is only triggered when COUNTVALUE reaches 0, that is, when the prefetch engine automatically goes from an active to an inactive state.

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The number of bytes to be prefetched (programmed in TRANSFERCOUNT) must be a multiple of the programmed FIFOTHRESHOLD to trigger the correct number of interrupts allowing a deterministic and transparent FIFO control. If this guideline is respected, the number of ISR accesses is always required and the FIFO is always empty after the last interrupt is triggered. In other cases, the TERMINALCOUNT interrupt must be used to read the remaining bytes in the FIFO (the number of remaining bytes being lower than the FIFOTHRESHOLD value).

In DMA draining mode, the GPMC_PREFETCH_CONFIG1[2] DMAMODE bit must be set so that the GPMC issues a DMA hardware request when at least FIFOTHRESHOLD bytes are ready to be read from the FIFO. The DMA channel that owns this DMA request must be programmed so that the number of bytes programmed in FIFOTHRESHOLD is read from the FIFO during the DMA request process. The DMA request is kept active until this number of bytes has effectively been read from the FIFO, and no other DMA request can be issued until the ongoing active request is complete.

In prefetch mode, the TERMINALCOUNT event is also a source of DMA requests if the number of bytes to be prefetched is not a multiple of FIFOTHRESHOLD, the remaining bytes in the FIFO can be read by the DMA channel using the last DMA request. This assumes that the number of remaining bytes to be read is known and controlled through the DMA channel programming model.

Any potentially active DMA request is cleared when the prefetch engine goes from inactive-to-active prefetch (the STARTENGINE bit is set to 1). The associated DMA channel must always be enabled by the MPU after setting the STARTENGINE bit so that the out-of-date active DMA request does not trigger spurious DMA transfers.

15.4.4.13.4.4 Write-Posting Mode

The write-posting mode is selected when the GPMC_PREFETCH_CONFIG1[0] ACCESSMODE bit is set.

The MPU NAND software driver must issue the correct address pointer initialization command (page program) before the engine can start writing data into the NAND memory device. The engine starts when the GPMC_PREFETCH_CONTROL[0] STARTENGINE bit is set to 1. The STARTENGINE bit clears automatically when posting completes. When all data have been written to the NAND memory device, the MPU NAND software driver must issue the second cycle program command and monitor the status for programming process completion (adding ECC handling, if required).

If used, the ECC calculator engine must be started (configured, reset, and enabled) before the posting engine is started so that the ECC parities are calculated properly on all data written by the prefetch engine to the associated chip-select.

In write-posting mode, the GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE bit must be cleared so that posting starts as soon as the STARTENGINE bit is set and the FIFO is not empty.

If the STARTENGINE bit is set after the NAND address phase (page program command), the STARTENGINE setting is effective only after the actual NAND command completion. To prevent GPMC stall during this NAND command phase, set the STARTENGINE bit field before the NAND address completion and ensure that the associated DMA channel is enabled after the NAND address phase.

The posting engine issues a write request when valid data are available from the FIFO and until the programmed GPMC_PREFETCH_CONFIG2[13:0] TRANSFERCOUNT accesses are complete.

The STARTENGINE bit clears automatically when posting completes. When all data have been written to the NAND memory device, the MPU NAND software driver must issue the second cycle program command and monitor the status for programming process completion. The closing program command phase must be issued only when the full NAND page has been written into the NAND flash write buffer, including the spare area data and the ECC parities, if used.

Table 15-355 describes the write-posting configuration.

Table 15-355. Write-Posting Mode Configuration

Bit Field	Register	Value	Comments
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	0	Write-posting engine can be configured only if STARTENGINE is set to 0.

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Table 15-355. Write-Posting Mode Configuration (continued)

Bit Field	Register	Value	Comments
ENGINECSSELECTOR	GPMC_PREFETCH_CONFIG1[26:24]	0 to 3	Selects the chip-select associated with a NAND device where the prefetch engine is active
ACCESSMODE	GPMC_PREFETCH_CONFIG1[0]	1	Selects write-posting mode
FIFOTHRESHOLD	GPMC_PREFETCH_CONFIG1[14:8]		Selects the maximum number of bytes read or written by the host on DMA or interrupt request
TRANSFERCOUNT	GPMC_PREFETCH_CONFIG2[13:0]		Selects the number of bytes to be read or written by the engine from/to the selected chip-select
SYNCHROMODE	GPMC_PREFETCH_CONFIG1[3]	0	Engine starts the access to chip-select as soon as STARTENGINE is set.
ENABLEOPTIMIZEDACCESS	GPMC_PREFETCH_CONFIG1[27]	0/1	See Section 15.4.4.13.4.6, *Optimizing NAND Access Using the Prefetch and Write-Posting Engine*.
CYCLEOPTIMIZATION	GPMC_PREFETCH_CONFIG1[30:28]		
ENABLEENGINE	GPMC_PREFETCH_CONFIG1[7]	1	Engine enabled
STARTENGINE	GPMC_PREFETCH_CONTROL[0]	1	Starts the prefetch engine

15.4.4.13.4.5 FIFO Control in Write-Posting Mode

The FIFO can be filled directly by the MPU or by an sDMA channel.

In MPU filling mode, the FIFO status can be monitored through the FIFOPOINTER or through the GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bit. FIFOPOINTER indicates the current number of available free byte places in the FIFO, and the FIFOTHRESHOLDSTATUS bit, when set, indicates that at least FIFOTHRESHOLD free byte places are available in the FIFO.

An interrupt can be issued by the GPMC if the GPMC_IRQENABLE[0] FIFOEVENTENABLE bit is set. When the interrupt is fired, the GPMC_IRQSTATUS[0] FIFOEVENTSTATUS bit is set. To clear the interrupt, the MPU must write enough bytes to fill the FIFO or to get below the programmed threshold, and the FIFOEVENTSTATUS bit must be cleared to get further interrupt events. The FIFOEVENTSTATUS bit must always be cleared before asserting the FIFOEVENTENABLE bit to clear any out-of-date logged interrupt event. This interrupt must be enabled after enabling the STARTENGINE bit.

The posting completion can be monitored through the GPMC_PREFETCH_STATUS[13:0] COUNTVALUE bit field. COUNTVALUE indicates the current number of remaining data to be written based on the value of the TRANSFERCOUNT bit field. An interrupt is issued by the GPMC when the write-posting process completes (that is, COUNTVALUE equal to 0) if the GPMC_IRQENABLE[1] TERMINALCOUNTEVENTENABLE bit is set. When the interrupt is fired, the GPMC_IRQSTATUS[1] TERMINALCOUNTSTATUS bit is set. To clear the interrupt, the MPU must clear the TERMINALCOUNTSTATUS bit. The TERMINALCOUNTSTATUS bit must always be cleared before asserting the TERMINALCOUNTEVENTENABLE bit to clear any out-of-date logged interrupt event.

NOTE: The value of the COUNTVALUE bit field is valid only if the write-posting engine is active and started, and an interrupt is issued only when COUNTVALUE reaches 0; that is, when the posting engine automatically goes from active to inactive.

In DMA filling mode, the DMAMode bit field in the GPMC_PREFETCH_CONFIG1[2] DMAMODE bit must be set so that the GPMC issues a DMA hardware request when at least FIFOTHRESHOLD bytes-free places are available in the FIFO. The DMA channel that owns this DMA request must be programmed so that a number of bytes equal to the value programmed in the FIFOTHRESHOLD bit field are written into the FIFO during the DMA access. The DMA request remains active until the associated number of bytes has effectively been written into the FIFO, and no other DMA request can be issued until the ongoing active request completes.

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Any potentially active DMA request is cleared when the prefetch engine goes from inactive-to-active prefetch (STARTENGINE set to 1). The associated DMA channel must always be enabled by the MPU after setting the STARTENGINE bit so that an out-of-date active DMA request does not trigger spurious DMA transfers.

In write-posting mode, the DMA or MPU fills the FIFO with no consideration for the associated byte enables. Any byte stored in the FIFO is written into the memory device.

15.4.4.13.4.6 Optimizing NAND Access Using the Prefetch and Write-Posting Engine

Access time to a NAND memory device can be optimized for back-to-back accesses if the associated nCS signal is not deasserted between accesses. The GPMC access engine can track prefetch engine accesses to optimize the access timing parameter programmed for the allocated chip-select, if no accesses to other chip-selects (that is, interleaved accesses) occur. Similarly, the access engine also eliminates CYCLE2CYCLEDELAY even if CYCLE2CYCLESAMECSEN is set. This capability is limited to the prefetch and write-posting engine accesses, and MPU accesses to a NAND memory device (through the defined chip-select memory region or through the GPMC_NAND_DATA_i location, where i = 0 to 7) are never optimized.

The GPMC_PREFETCH_CONFIG1[27] ENABLEOPTIMIZEDACCESS bit must be set to enable optimized accesses. To optimize access time, the GPMC_PREFETCH_CONFIG1[30:28] CYCLEOPTIMIZATION bit field defines the number of GPMC_FCLK cycles to be suppressed from the following timing parameters:

- RDCYCLETIME
- WRCYCLETIME
- RDACCESSTIME
- WRACCESSTIME
- CSOFFTIME
- ADVOFFTIME
- OEOFFTIME
- WEOFFTIME

Figure 15-91 shows that in the case of back-to-back accesses to the NAND flash through the prefetch engine, CYCLE2CYCLESAMECSEN is forced to 0 when using optimized accesses. The first access uses the regular timing settings for this chip-select. All accesses after this one use settings reduced by x clock cycles, x being defined by the GPMC_PREFETCH_CONFIG1[30:28] CYCLEOPTIMIZATION bit field.

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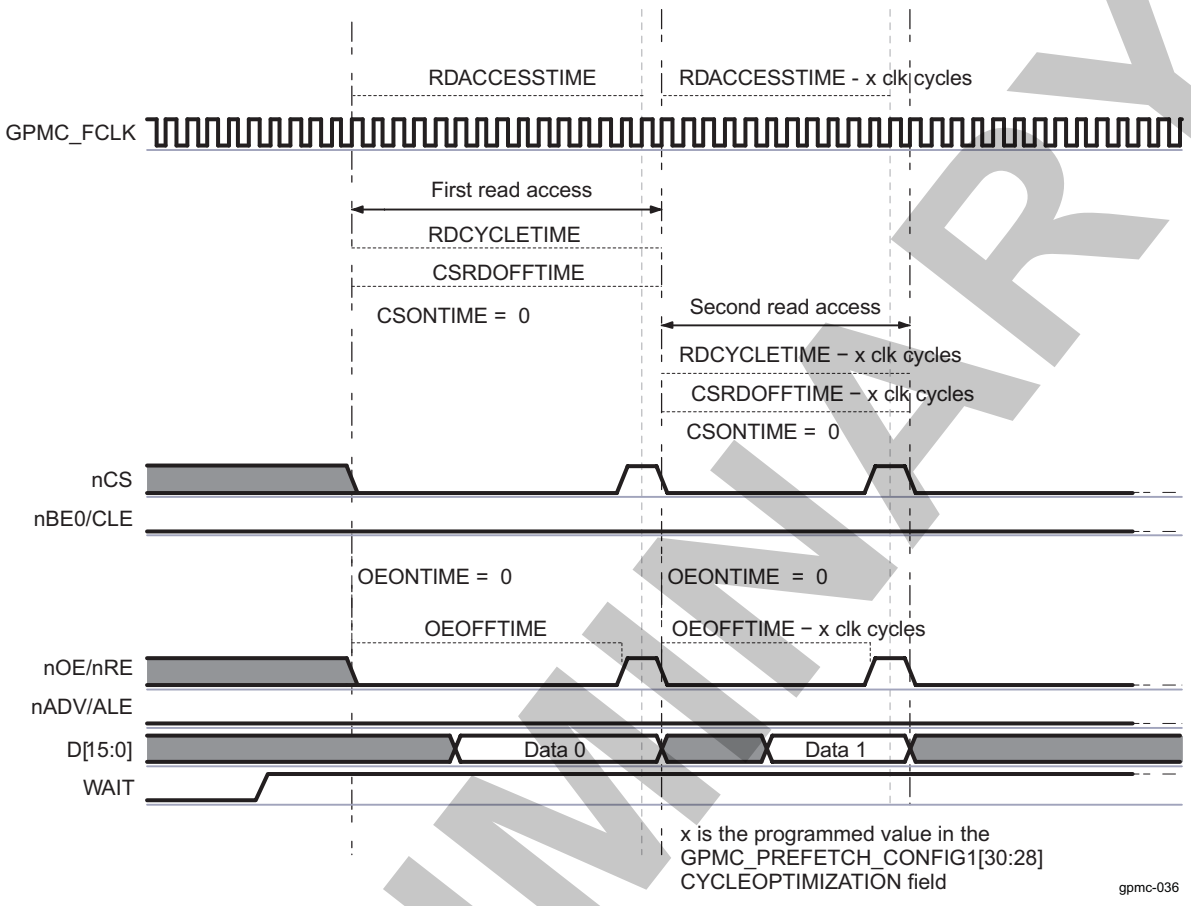
Figure 15-91. NAND Read Cycle Optimization Timing Description



15.4.4.13.4.7 Interleaved Accesses Between Prefetch and Write-Posting Engine and Other Chip-Selects

Any on-going read or write access from the prefetch and write-posting engine is completed before an access to any other chip-select can be initiated. As a default, the arbiter uses a fixed-priority algorithm, and the prefetch and write-posting engine has the lowest priority. The maximum latency added to access starting time in this case equals the RDCYCLETIME or WRCYCLETIME (optimized or not) plus the requested BUSTURNAROUND delay for bus turnaround completion programmed for the chip-select to which the NAND device is connected.

Alternatively, a round-robin arbitration can be used to prioritize accesses to the external bus. This arbitration scheme is enabled by setting the GPMC_PREFETCH_CONFIG1[23] PFPWENROUNDROBIN bit. When a request to another chip-select is received while the prefetch and write-posting engine is active, priority is given to the new request. The request processed thereafter is the prefetch and write-posting engine request, even if another interconnect request is passed in the mean time. The engine keeps control of the bus for an additional number of requests programmed in the GPMC_PREFETCH_CONFIG1[19:16] PFPWWEIGHTEDPRIO bit field. Control is then passed to the direct interconnect request.

As an example, the round-robin arbitration scheme is selected with PFPWWEIGHTEDPRIO set to 0x2. Considering that the prefetch and write-posting engine and the interconnect interface are always requesting access to the external interface, the GPMC grants priority to the direct interconnect access for one request. The GPMC then grants priority to the engine for three requests, and finally back to the direct interconnect access, until the arbiter is reset when one of the two initiators stops initiating requests.

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15.4.5 GPMC Basic Programming Model

15.4.5.1 GPMC High-Level Programming Model Overview

The goal of the basic high-level programming model is to introduce a top-down approach to users that need to configure the GPMC module.

Figure 15-92 and Table 15-356 through Table 15-358 show a programming model top-level diagram for the GPMC, and a description of each step. Each block of the diagram is described in one of the following sections through a set of registers to configure.

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Figure 15-92. Programming Model Top-Level Diagram

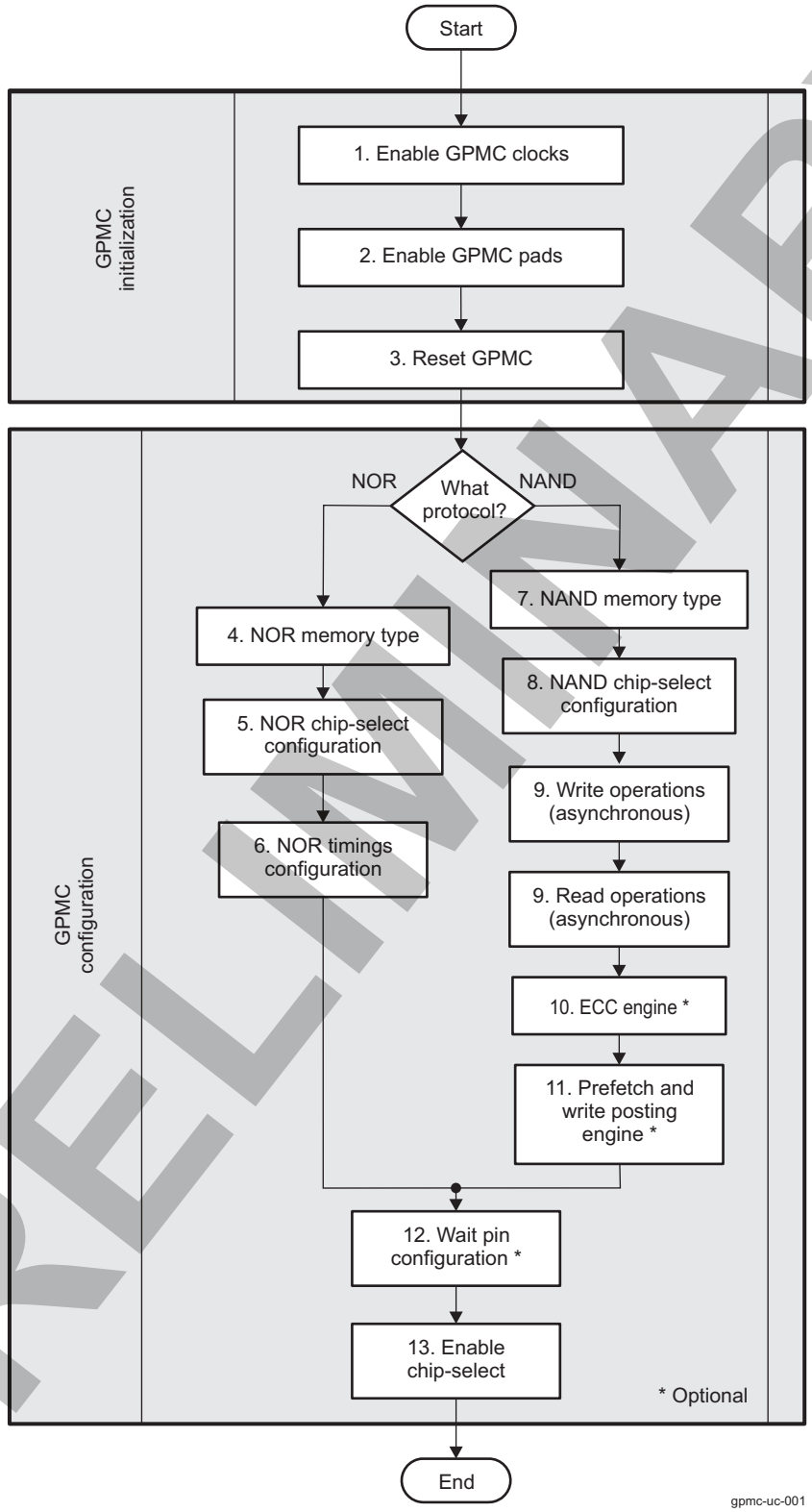

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Table 15-356. GPMC Initialization

Step	Description
Enable GPMC clocks.	Module interface and functional clocks must be enabled. See Section 3.1.1, *Power, Reset, and Clock Management*.
Enable GPMC pads.	Module-specific pad multiplexing and configuration must be set in the control module. See Figure 18-1, *Control Module*.
Reset GPMC.	See Table 15-359.

Table 15-357. GPMC Configuration in NOR Mode

Step	Description
NOR Memory Type	See Table 15-360.
NOR Chip-Select Configuration	See Table 15-361.
NOR Timings Configuration	See Table 15-362.
Wait Pin Configuration	See Table 15-370.
Enable Chip-Select	See Table 15-371.

Table 15-358. GPMC Configuration in NAND Mode

Step	Description
NAND Memory Type	See Table 15-365.
NAND Chip-Select Configuration	See Table 15-366.
Write Operations (Asynchronous)	See Table 15-367.
Read Operations (Asynchronous)	See Table 15-367.
ECC Engine	See Table 15-368.
Prefetch and Write-Posting Engine	See Table 15-369.
Wait Pin Configuration	See Table 15-370.
Enable Chip-Select	See Table 15-371.

15.4.5.2 GPMC Initialization

Table 15-387 describes the settings required to prepare the GPMC; that is enabling its clock and pads, and proceeding to a GPMC reset.

Table 15-359. Reset GPMC

Subprocess Name	Register/Bit Field	Value
Start a software reset.	GPMC_SYSCONFIG[1] SOFTRESET	0x1
Wait until	GPMC_SYSSTATUS[0] RESETDONE =	0x1

15.4.5.3 GPMC Configuration in NOR Mode

This section gives a generic configuration for parameters related to the NOR memory connected to the GPMC.

Table 15-360. NOR Memory Type

Subprocess Name	Register / Bit Field	Value
Set the NOR protocol.	GPMC_CONFIG1_i[11:10] DEVICETYPE	0x0
Set a device size.	GPMC_CONFIG1_i[13:12] DEVICESIZE	x
Select an address and data multiplexing protocol.	GPMC_CONFIG1_i[9] MUXADDDATA	x
Set the attached device page length.	GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH	x
Set the wrapping burst capabilities.	GPMC_CONFIG1_i[31] WRAPBURST	x

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Table 15-360. NOR Memory Type (continued)

Subprocess Name	Register / Bit Field	Value
Select a timing signals latencies factor.	GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY	x
Select an output clock frequency (1).	GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER	x
Choose an output clock activation time (1).	GPMC_CONFIG1_i[26:25] CLKACTIVATIONTIME	x
Set a single or multiple access for read operations (1).	GPMC_CONFIG1_i[30] READMULTIPLE	x
Set a synchronous or asynchronous mode for read operations.	GPMC_CONFIG1_i[29] READTYPE	x
Set a single or multiple access for write operations.	GPMC_CONFIG1_i[28] WRITEMULTIPLE	x
Set a synchronous or asynchronous mode for write operations.	GPMC_CONFIG1_i[27] WRITETYPE	x

(1) Applies only to synchronous configurations (or nonmultiplexed asynchronous for multiple access one)

Table 15-361. NOR Chip-Select Configuration

Subprocess Name	Register/Bit Field	Value
Select the chip-select base address.	GPMC_CONFIG7_i[5:0] BASEADDRESS	x
Select the chip-select mask address.	GPMC_CONFIG7_i[11:8] MASKADDRESS	x

Table 15-362. NOR Timings Configuration

Subprocess Name	Register/Bit Field	Value
Configure adequate timing parameters in various memory modes.	See Section 15.4.5.6, *GPMC Timing Parameters*	

Table 15-363. Wait Pin Configuration

Subprocess Name	Register/Bit Field	Value
Enable or disable wait pin monitoring for read operations.	GPMC_CONFIG1_i[22] WAITREADMONITORING	x
Enable or disable wait pin monitoring for write operations.	GPMC_CONFIG1_i[21] WAITWRITEMONITORING	x
Select a wait pin monitoring time.	GPMC_CONFIG1_i[19:18] WAITMONITORINGTIME	x
Choose the input wait pin for the chip-select.	GPMC_CONFIG1_i[17:16] WAITPINSELECT	x

Table 15-364. Enable Chip-Select

Subprocess Name	Register/Bit Field	Value
When all parameters are configured, enable the chip-select.	GPMC_CONFIG7_i[6] CSVALID	x

15.4.5.4 GPMC Configuration in NAND Mode

This section gives a generic configuration for parameters related to the NAND memory connected to the GPMC.

Table 15-365. NAND Memory Type

Subprocess Name	Register/Bit Field	Value
Set the NAND protocol.	GPMC_CONFIG1_i[11:10] DEVICETYPE	0x2
Set a device size.	GPMC_CONFIG1_i[13:12] DEVICESIZE	x
Set the address and data multiplexing protocol to non-multiplexed attached device.	GPMC_CONFIG1_i[9] MUXADDDATA	0x0
Select a timing signals latencies factor.	GPMC_CONFIG1_i[4] TIMEPARAGRANULARITY	x
Set a synchronous or asynchronous mode and a single or multiple access for read and write operations.	See Section 15.4.5.5, *Set Memory Access*.	x

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Table 15-366. NAND Chip-Select Configuration

Subprocess Name	Register/Bit Field	Value
Select the chip-select base address.	GPMC_CONFIG7_i[5:0] BASEADDRESS	x
Select the chip-select minimum granularity (16MiB).	GPMC_CONFIG7_i[11:8] MASKADDRESS	x

Table 15-367. Asynchronous Read and Write Operations

Subprocess Name	Register/Bit Field	Value
Configure adequate timing parameters in asynchronous modes	See Section 15.4.5.6, *GPMC Timing Parameters*.	

Table 15-368. ECC Engine

Subprocess Name	Register/Bit Field	Value
Select the ECC result register where the first ECC computation is stored (applies only to Hamming).	GPMC_ECC_CONTROL[3:0] ECCPOINTER	x (1)
Clear all ECC result registers.	GPMC_ECC_CONTROL[8] ECCCLEAR	Write 1 to clear.
Define ECCSIZE0 and ECCSIZE1.	GPMC_ECC_SIZE_CONFIG[19:12] ECCSIZE0 and [29:22] ECCSIZE1	x (2)
Select the size of each of the 9 result registers (size specified by ECCSIZE0 or ECCSIZE1).	GPMC_ECC_SIZE_CONFIG[j-1] ECCjRESULTSIZE where j = 1 to 9	x
Select the chip-select where ECC is computed.	GPMC_ECC_CONFIG[3:1] ECCCS	x
Select the Hamming code or BCH code ECC algorithm in use.	GPMC_ECC_CONFIG[16] ECCALGORITHM	x
Select word size for ECC calculation.	GPMC_ECC_CONFIG[7] ECC16B	x
If the BCH code is used, Set an error correction capability and Select a number of sectors to process.	GPMC_ECC_CONFIG[13:12] ECCBCHTSEL and GPMC_ECC_CONFIG[6:4] ECCTOPSECTOR	x
Enable the ECC computation.	GPMC_ECC_CONFIG[0] ECCENABLE	0x1

(1) This parameter depends on the numbers of sectors in a page.
(2) Depends on the size of each sector in the NAND page

Table 15-369. Prefetch and Write-Posting Engine

Subprocess Name	Register/Bit Field	Value
Disable the engine before configuration.	GPMC_PREFETCH_CONTROL[0] STARTENGINE	0x0
Select the chip-select associated with a NAND device where the prefetch engine is active.	GPMC_PREFETCH_CONFIG1[26:24] ENGINECSSELECTOR	x
Select access direction through prefetch engine, read or write.	GPMC_PREFETCH_CONFIG1[0] ACCESSMODE	x
Select the threshold used to issue a DMA request.	GPMC_PREFETCH_CONFIG1[14:8] FIFOTHRESHOLD	x
Select DMA synchronized mode or software manual mode.	GPMC_PREFETCH_CONFIG1[2] DMAMODE	x
Select if the engine immediately starts accessing the memory upon STARTENGINE assertion or if hardware synchronization based on a WAIT signal is used.	GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE	x
Select which wait pin edge detector should start the engine in synchronized mode.	GPMC_PREFETCH_CONFIG1[5:4] WAITPINSELECTOR	x
Enter a number of clock cycles removed to timing parameters (for all back-to-back accesses to the NAND flash except the first one).	GPMC_PREFETCH_CONFIG1[30:28] CYCLEOPTIMIZATION	x
Enable the prefetch postwrite engine.	GPMC_PREFETCH_CONFIG1[7] ENABLEENGINE	0x1
Select the number of bytes to be read or written by the engine to the selected chip-select.	GPMC_PREFETCH_CONFIG2[13:0] TRANSFERCOUNT	x
Start the prefetch engine.	GPMC_PREFETCH_CONTROL[0] STARTENGINE	0x1

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Table 15-370. Wait Pin Configuration

Subprocess Name	Register/Bit Field	Value
Selects when the engine starts the access to chip-select.	GPMC_PREFETCH_CONFIG1[3] SYNCHROMODE	x
Select which wait pin edge detector should start the engine in synchronized mode.	GPMC_PREFETCH_CONFIG1[5:4] WAITPINSELECTOR	x

Table 15-371. Enable Chip-Select

Subprocess Name	Register/Bit Field	Value
When all parameters are configured, enable the chip-select.	GPMC_CONFIG7_i[6] CSVALID	x

15.4.5.5 Set Memory Access

This section describes the bit field to configure to set the GPMC in various memory modes. Table 15-372 and Table 15-373 provide check lists for mode parameters and access type parameters, respectively.

Table 15-372. Mode Parameters Check List

Register	Bit	Name	Asynchronous				Synchronous			
			Single Read Access	Single Write Access	Multiple Read (Page) Access	Multiple Write (Page) Access	Single Read Access	Single Write Access	Multiple Read (Burst) Access	Multiple Write (Burst) Access
GPMC_CONFIG1_i	30	READMULTIPLE	0x0	–	0x1 (1)	N/S	0x0	–	0x1	–
GPMC_CONFIG1_i	29	READTYPE	0x0	–	0x0 (1)	N/S	0x1	–	0x1	–
GPMC_CONFIG1_i	28	WRITEMULTIPLE	–	0x0	- (1)	N/S	–	0x0	–	0x1
GPMC_CONFIG1_i	27	WRITETYPE	–	0x0	- (1)	N/S	–	0x1	–	0x1

(1) Multiple read is not supported in address/data-multiplexed and AAD-multiplexed modes. Multiple read is supported in nonmultiplexed mode.

Table 15-373. Access Type Parameters Check List

Register	Bit	Name	Access Type		
			Nonmultiplexed	Address/ Data-Multiplexed	AAD-Multiplexed
GPMC_CONFIG1_i	9:8	MUXADDDATA	0x0	0x2	0x1
GPMC_CONFIG	1	LIMITEDADDRESS (1)	0x1	0x0	0x0

(1) This parameter applies to all chip-selects. There is no per-chip-select configuration for this parameter.

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15.4.5.6 GPMC Timing Parameters

Figure 15-93 shows a programming model diagram for the NOR interfacing timing parameters.

Figure 15-93. NOR Interfacing Timing Parameters Diagram

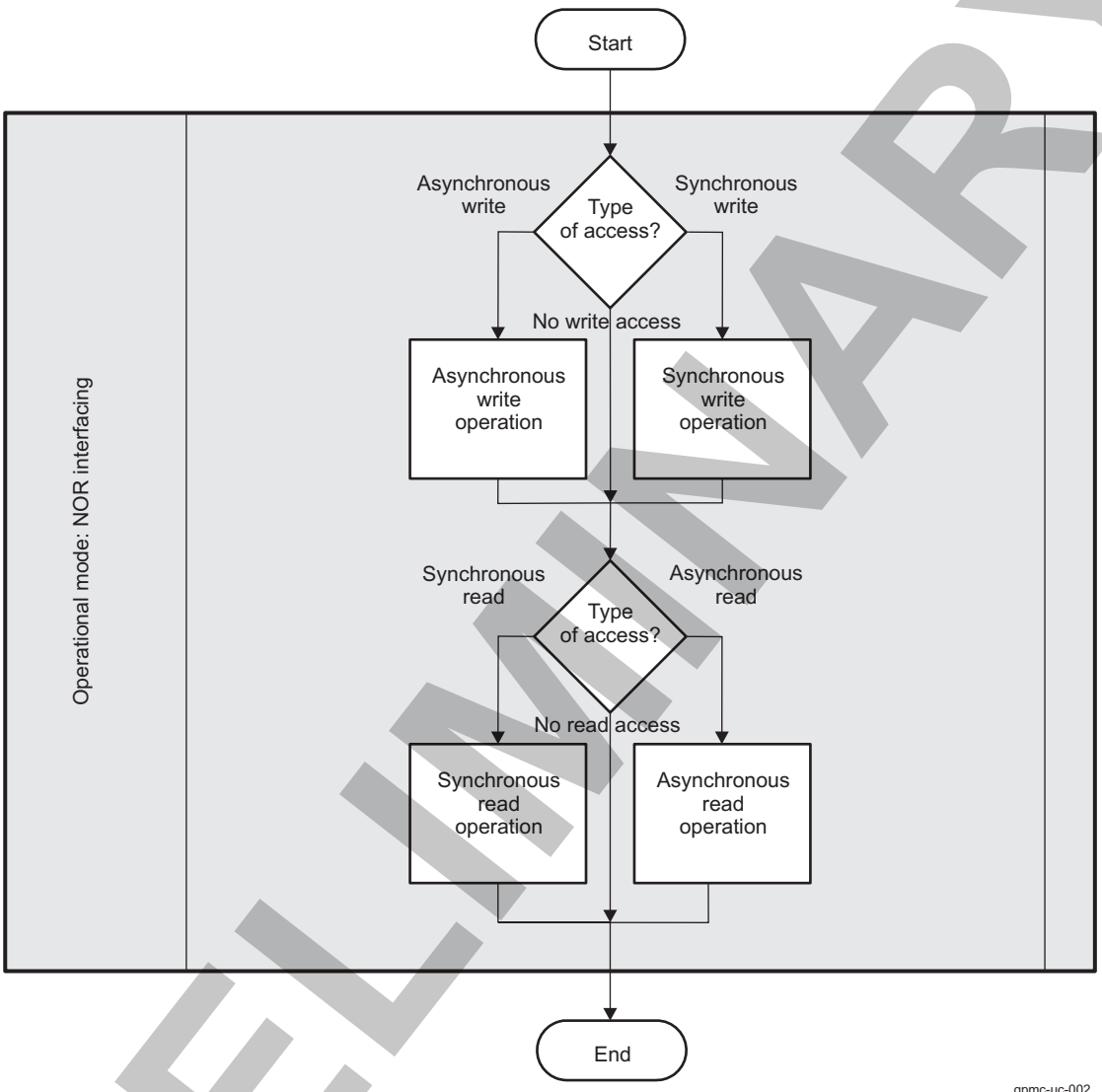

Table 15-374 lists the bit fields to configure adequate timing parameters in various memory modes.

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Table 15-374. Timing Parameters

			Asynchronous			Synchronous				Access Type		
Register	Bit	Name	Single Read Access	Single Write Access	Multiple Read (Page) access	Single Read Access	Single Write Access	Multiple Read (Burst) Access	Multiple Write (Burst) Access	Non-multiplexed	Address / Data-Multiplexed	AAD Multiplexed
GPMC_CONFIG1_i	9	MUXADDDATA	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG1_i	29	READTYPE	y		y	y		y		y	y	y
GPMC_CONFIG1_i	30	READMULTIPLE	y		y	y		y		y	y	y
GPMC_CONFIG1_i	27	WRITETYPE		y			y		y	y	y	y
GPMC_CONFIG1_i	28	WRITEMULTIPLE		y			y		y	y	y	y
GPMC_CONFIG1_i	31	WRAPBURST						y	y	y	y	y
GPMC_CONFIG1_i	26:25	CLKACTIVATIONTIME				y	y	y	y	y	y	y
GPMC_CONFIG1_i	19:18	WAITMONITORINGTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG1_i	4	TIMEPARAGRANULARITY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG2_i	20:16	CSWROFFTIME		y			y		y	y	y	y
GPMC_CONFIG2_i	12:8	CSRDOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG2_i	7	CSEXTRADELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG2_i	3:0	CSONTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG3_i	30:28	ADVAADMUXWROFFTIME		y			y		y			y
GPMC_CONFIG3_i	30:29	ADVAADMUXRDOFFTIME	y		y	y		y				y
GPMC_CONFIG3_i	6:4	ADVAADMUXONTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG3_i	20:16	ADVWROFFTIME		y			y		y	y	y	y
GPMC_CONFIG3_i	12:8	ADVRDOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG3_i	7	ADVEXTRADELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG3_i	3:0	ADVONTIME	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG4_i	15:13	OEAADMUXOFFTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG4_i	6:4	OEAADMUXONTIME	y	y	y	y	y	y	y			y
GPMC_CONFIG4_i	28:24	WEOFFTIME		y			y		y	y	y	y
GPMC_CONFIG4_i	23	WEEXTRADELAY		y			y		y	y	y	y
GPMC_CONFIG4_i	19:16	WEONTIME		y			y		y	y	y	y
GPMC_CONFIG4_i	12:8	OEOFFTIME	y		y	y		y		y	y	y
GPMC_CONFIG4_i	7	OEEXTRADELAY	y		y	y		y		y	y	y
GPMC_CONFIG4_i	3:0	OEONTIME	y		y	y		y		y	y	y
GPMC_CONFIG5_i	27:24	PAGEBURSTACCESSTIME			y			y	y	y	y	y
GPMC_CONFIG5_i	20:16	RDACCESSTIME	y		y	y		y		y	y	y

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Table 15-374. Timing Parameters (continued)

			Asynchronous			Synchronous			Access Type		
GPMC_CONFIG5_i	12:8	WRCYCLETIME		y			y	y	y	y	y
GPMC_CONFIG5_i	4:0	RDCYCLETIME	y		y	y			y	y	y
GPMC_CONFIG6_i	28:24	WRACCESSTIME		y			y	y	y	y	y
GPMC_CONFIG6_i	19:16	WRDATAONADMUXBUS		y			y	y		y	y
GPMC_CONFIG6_i	11:8	CYCLE2CYCLEDELAY	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	7	CYCLE2CYCLESAMECSEN	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	6	CYCLE2CYCLEDIFFCSEN	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG6_i	3:0	BUSTURNAROUND	y	y	y	y	y	y	y	y	y	y
GPMC_CONFIG7_i	6	CSVALID	y	y	y	y	y	y	y	y	y	y

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15.4.5.6.1 GPMC Timing Parameters Formulas

This section is intended to help the user calculate the GPMC timing bit field values. Formulas are not listed exhaustively.

The section describes:

- NAND flash interface timing parameters formulas
- Synchronous NOR flash timing parameters formulas
- Asynchronous NOR flash timing parameters formulas

15.4.5.6.1.1 NAND Flash Interface Timing Parameters Formulas

This section lists formulas to calculate NAND timing parameters. This is the case when GPMC_CONFIG1_i[11:10] DEVICETYPE = 0x2. Table 15-375 describes the NAND timing parameters.

Table 15-375. NAND Formulas Description

Configuration Parameter	Unit	Description
A	ns	Pulse duration – gpmc_nwe valid time
B	ns	Delay time – gpmc_ncs valid to gpmc_nwe valid
C	ns	Delay time – gpmc_nbe0_cle/gpmc_nadv_ale high to gpmc_nwe valid
D	ns	Delay time – gpmc_ad[15:0] valid to gpmc_nwe valid
E	ns	Delay time – gpmc_nwe invalid to gpmc_ad[15:0] invalid
F	ns	Delay time – gpmc_nwe invalid to gpmc_nbe0_cle/gpmc_nadv_ale invalid
G	ns	Delay time – gpmc_nwe invalid to gpmc_ncs invalid
H	ns	Cycle time – Write cycle time
I	ns	Delay time – gpmc_ncs valid to gpmc_noe valid
J	ns	Setup time – gpmc_ad[15:0] valid to gpmc_noe invalid
K	ns	Pulse duration – gpmc_noe valid time
L	ns	Cycle time – Read cycle time
M	ns	Delay time – gpmc_noe invalid to gpmc_ncs invalid

The configuration parameters are calculated through the following formulas.

A = (WEOffTime – WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period

B = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK period

C = ((WEOnTime – ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - ADVExtraDelay)) * GPMC_FCLK period

D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK period

E = (WrCycleTime – WEOffTime * (TimeParaGranularity + 1) – 0.5 * WEExtraDelay) * GPMC_FCLK period

F = (ADVWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – WEExtraDelay) * GPMC_FCLK period

G = (CSWrOffTime – WEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – WEExtraDelay) * GPMC_FCLK period

H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK period

I = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK period

J = ((AccessTime – OEOffTime) * (TimeParaGranularity + 1) – 0.5 * OEExtraDelay)) * GPMC_FCLK period

K = (OEOffTime – OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK period

L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK period

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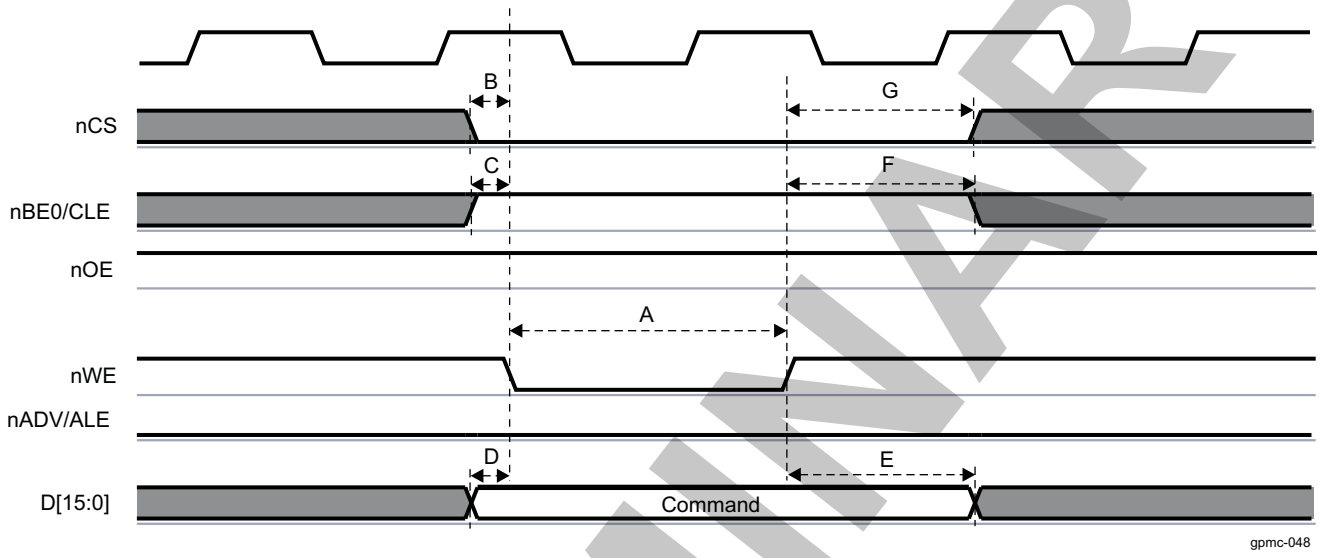
M = (CSRdOffTime – OEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - OEExtraDelay) * GPMC_FCLK period

Figure 15-94 shows a simplified example of command latch cycle timing where formulas are associated with signal waves.

Figure 15-94. NAND Command Latch Cycle Timing Simplified Example



15.4.5.6.1.2 Synchronous NOR Flash Timing Parameters Formulas

This section lists all formulas to calculate synchronous NOR timing parameters. This is the case when GPMC_CONFIG1_i[11:10] DEVICETYPE = 0x0 and when READTYPE or WRITETYPE are set to synchronous mode. Table 15-376 describes the synchronous NOR formulas.

Table 15-376. Synchronous NOR Formulas Description

Configuration Parameter	Unit	Description
A	ns	Pulse duration – gpmc_ncs low
B	ns	Delay time – address bus valid to gpmc_clk first edge
		Delay time – gpmc_nbe0_cle/gpmc_nbe1 valid to gpmc_clk first edge
C	ns	Pulse duration – gpmc_nbe0_cle/gpmc_nbe1 low
D	ns	Delay time – gpmc_clk rising edge to gpmc_nbe0_cle/gpmc_nbe1 invalid
		Delay time – gpmc_clk rising edge to gpmc_nadv_ale invalid
E	ns	Delay time – gpmc_clk rising edge to gpmc_ncs invalid
		Delay time – gpmc_clk rising edge to gpmc_noe invalid
F	ns	Delay time – gpmc_clk rising edge to gpmc_ncs transition
G	ns	Delay time – gpmc_clk rising edge to gpmc_nadv_ale transition
H	ns	Delay time – gpmc_clk rising edge to gpmc_noe transition
I	ns	Delay time – gpmc_clk rising edge to gpmc_nwe transition
J	ns	Delay time – gpmc_clk rising edge to gpmc_ad data bus transition
		Delay time – gpmc_clk rising edge to gpmc_nbe0_cle/gpmc_nbe1 transition
K	ns	Pulse duration – gpmc_nadv_ale low
L	ns	Delay time – gpmc_wait invalid to first data latching gpmc_clk edge

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The configuration parameters are calculated through the following formulas.

1. For single read accesses:
   A = (CSRDOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = RDCYCLETIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (RDCYCLETIME – ACCESSTIME) * GPMC_FCLK period
   E = (CSRDOFFTIME – ACCESSTIME) * GPMC_FCLK period
2. For burst read accesses (where n is the page burst access number):
   A = (CSRDOFFTIME – CSONTIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = (RDCYCLETIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (RDCYCLETIME – (ACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME) * GPMC_FCLK period
   E = (CSRDOFFTIME – (ACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME) * GPMC_FCLK period
3. For burst write accesses (where n is the page burst access number):
   A = (CSWROFFTIME – CSONTIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   C = (WRCYCLETIME + (n – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
   D = (WRCYCLETIME – (ACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME) * GPMC_FCLK period
   E = (CSWROFFTIME – (ACCESSTIME + (n – 1) * PAGEBURSTACCESSTIME) * GPMC_FCLK period
4. For all accesses:
   For nCS falling edge (chip-select activated):
   - Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSONTIME are odd) or (CLKACTIVATIONTIME and CSONTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSONTIME – CLKACTIVATIONTIME) is a multiple of 3
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
     F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

   For nCS rising edge (chip-select deactivated) in reading mode:
   - Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and CSRDOFFTIME are odd) or (CLKACTIVATIONTIME and CSRDOFFTIME are even)
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.
   - Case where GPMCFCLKDIVIDER = 0x2:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSRDOFFTIME – CLKACTIVATIONTIME) is a multiple of 3
     F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSRDOFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
     F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSRDOFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

   For nCS rising edge (chip-select deactivated) in writing mode:
   - Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period
   - Case where GPMCFCLKDIVIDER = 0x1:
     F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and

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CSWROFFTIME are odd) or (CLKACTIVATIONTIME and CSWROFFTIME are even)
F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period otherwise.

- Case where GPMCFCLKDIVIDER = 0x2:
  F = 0.5 * CSEXTRADELAY * GPMC_FCLK period, when (CSWROFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  F = (1 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSWROFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  F = (2 + 0.5 * CSEXTRADELAY) * GPMC_FCLK period, when (CSWROFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nADV falling edge (nADV activated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVONTIME are odd) or (CLKACTIVATIONTIME and ADVONTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVONTIME – CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nADV rising edge (nADV deactivated) in reading mode:

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVRDOFFTIME are odd) or (CLKACTIVATIONTIME and ADVRDOFFTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME - 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVRDOFFTIME - CLKACTIVATIONTIME - 2) is a multiple of 3

For nADV rising edge (nADV deactivated) in writing mode:

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and ADVWROFFTIME are odd) or (CLKACTIVATIONTIME and ADVWROFFTIME are even)
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  G = 0.5 * ADVEXTRADELAY * GPMC_FCLK period, when (ADVWROFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  G = (1 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVWROFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  G = (2 + 0.5 * ADVEXTRADELAY) * GPMC_FCLK period, when (ADVWROFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nOE falling edge (nOE activated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and OEONTIME

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are odd) or (CLKACTIVATIONTIME and OEONTIME are even)
H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period otherwise.

- Case where GPMCFCLKDIVIDER = 0x2:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (OEONTIME – CLKACTIVATIONTIME) is a multiple of 3
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  H = (2 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nOE rising edge (nOE deactivated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and OEOFFTIME are odd) or (CLKACTIVATIONTIME and OEOFFTIME are even)
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  H = 0.5 * OEEXTRADELAY * GPMC_FCLK period, when (OEOFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  H = (1 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEOFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  H = (2 + 0.5 * OEEXTRADELAY) * GPMC_FCLK period, when (OEOFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nWE falling edge (nWE activated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and WEONTIME are odd) or (CLKACTIVATIONTIME and WEONTIME are even)
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (WEONTIME – CLKACTIVATIONTIME) is a multiple of 3
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEONTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  I = (2 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEONTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For nWE rising edge (nWE deactivated):

- Case where GPMC_CONFIG1_i[1:0] GPMCFCLKDIVIDER = 0x0:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period
- Case where GPMCFCLKDIVIDER = 0x1:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (CLKACTIVATIONTIME and WEOFFTIME are odd) or (CLKACTIVATIONTIME and WEOFFTIME are even)
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period otherwise.
- Case where GPMCFCLKDIVIDER = 0x2:
  I = 0.5 * WEEXTRADELAY * GPMC_FCLK period, when (WEOFFTIME – CLKACTIVATIONTIME) is a multiple of 3
  I = (1 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEOFFTIME – CLKACTIVATIONTIME – 1) is a multiple of 3
  I = (2 + 0.5 * WEEXTRADELAY) * GPMC_FCLK period, when (WEOFFTIME – CLKACTIVATIONTIME – 2) is a multiple of 3

For gpmc_nadv low pulse duration:

- Read operation:
  K = (ADVRDOFFTIME – ADVONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
- Write operation:
  K = (ADVWROFFTIME – ADVONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period

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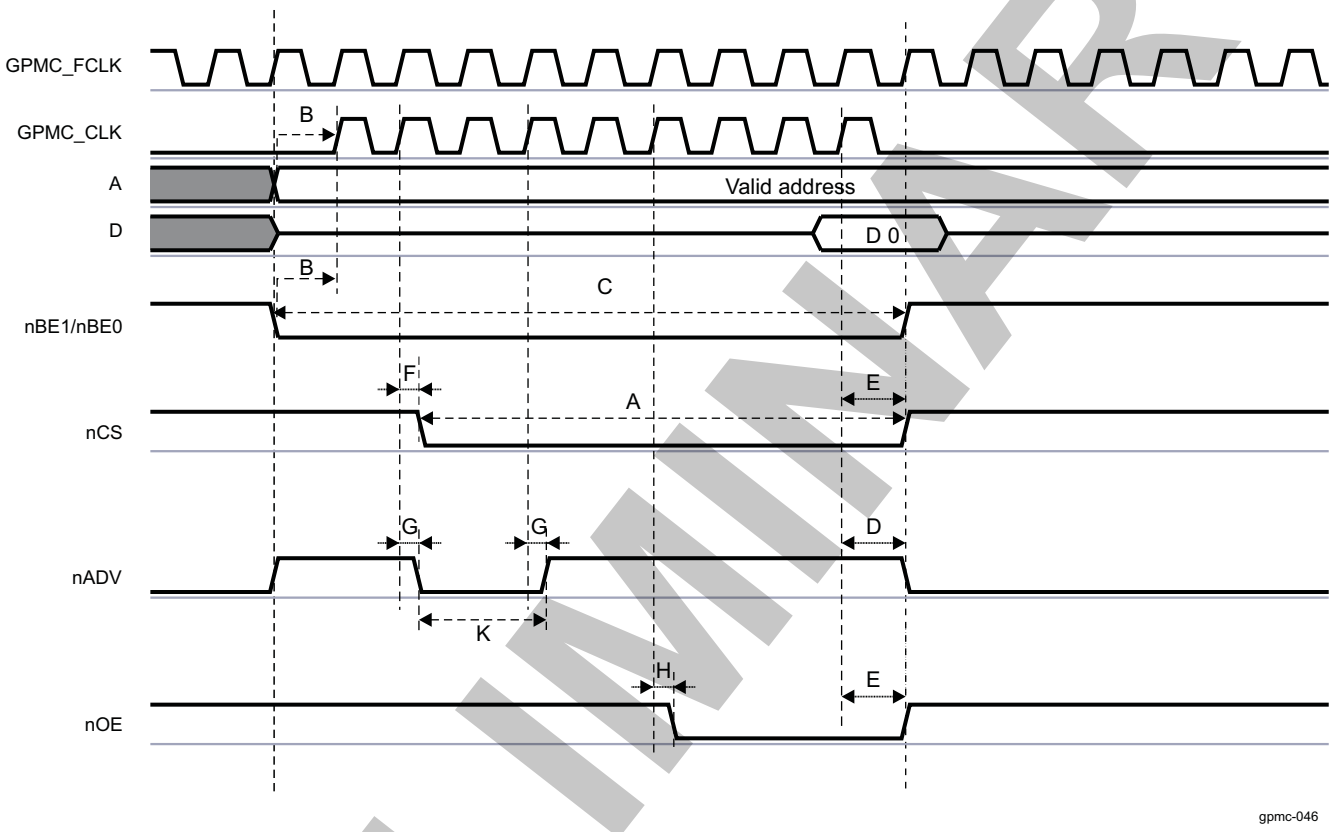
For gpmc_wait invalid to first data latching gpmc_clk edge:

- L = WAITMONITORINGTIME * (GPMCFCLKDIVIDER + 1) * GPMC_FCLK period + GPMC_CLK period

Figure 15-95 shows a simplified example of a synchronous NOR single read where formulas are associated with signal waves.

Figure 15-95. Synchronous NOR Single Read Simplified Example



15.4.5.6.1.3 Asynchronous NOR Flash Timing Parameters Formulas

This section lists all the formulas to calculate asynchronous NOR timing parameters. This is the case when GPMC_CONFIG1_i[11:10] DEVICETYPE = 0x0 and when READTYPE or WRITETYPE are set to asynchronous mode. Table 15-377 describes the asynchronous NOR formulas.

Table 15-377. Asynchronous NOR Formulas Description

Configuration Parameter	Unit	Description
A	ns	Pulse duration – gpmc_ncs low
B	ns	Delay time – gpmc_ncs valid to gpmc_nadv_ale invalid
C	ns	Delay time – gpmc_ncs valid to gpmc_noe invalid (single read)
D	ns	Pulse duration – address bus valid - 2nd, 3rd and 4th accesses
E	ns	Delay time – gpmc_ncs valid to gpmc_nwe valid
F	ns	Delay time – gpmc_ncs valid to gpmc_nwe invalid
G	ns	Address invalid duration between two successive R/W accesses
H	ns	Setup time – read data valid before gpmc_noe high
I	ns	Delay time – gpmc_ncs valid to gpmc_noe invalid (burst read)

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Table 15-377. Asynchronous NOR Formulas Description (continued)

Configuration Parameter	Unit	Description
J	ns	Delay time – address bus valid to gpmc_ncs valid
		Delay time – data bus valid to gpmc_ncs valid
		Delay time – gpmc_nbe0_cle/gpmc_nbe1 valid to gpmc_ncs valid
K	ns	Delay time – gpmc_ncs valid to gpmc_nadv_ale valid
L	ns	Delay time – gpmc_ncs valid to gpmc_noe valid
M	ns	Delay time – gpmc_ncs valid to first data latching edge
N	ns	Pulse duration – gpmc_nbe0_cle/gpmc_nbe1 valid time
O	ns	Delay time – gpmc_ncs valid to gpmc_nadv_ale valid

The configuration parameters are calculated through the following formulas. These formulas are not exhaustive.

- gpmc_ncs low pulse:
  For single read: A = (CSRDOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst read: A = (CSRDOFFTIME – CSONTIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
  For single write: A = (CSWROFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst write: A = (CSWROFFTIME – CSONTIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
- gpmc_ncs valid to gpmc_nadv_ale invalid delay:
  For reading: B = ((ADVRDOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
  For writing: B = ((ADVWROFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- C = ((OEOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- D = PAGEBURSTACCESSTIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
- E = ((WEONTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (WEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- F = ((WEOFFTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (WEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- G = CYCLE2CYCLEDELAY * GPMC_FCLK period
- H = ((OEOFFTIME – ACCESSTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * OEEXTRADELAY) * GPMC_FCLK period
- I = ((OEOFFTIME + (N – 1) * PAGEBURSTACCESSTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period, where N = page burst access number
- J = (CSONTIME * (TIMEPARAGRANULARITY + 1) + 0.5 * CSEXTRADELAY) * GPMC_FCLK period
- K = ((ADVONTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- L = ((OEONTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (OEEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period
- M = ((ACCESSTIME - CSONTIME) * (TIMEPARAGRANULARITY + 1) – 0.5 * CSEXTRADELAY) * GPMC_FCLK period
- gpmc_nbe0_cle/gpmc_nbe1 pulse:
  For single read: N = RDCYCLETIME * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period
  For burst read: N = (RDCYCLETIME + (N – 1) * PAGEBURSTACCESSTIME) * (TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number
  For burst write: N = (WRCYCLETIME + (N – 1) * PAGEBURSTACCESSTIME) *

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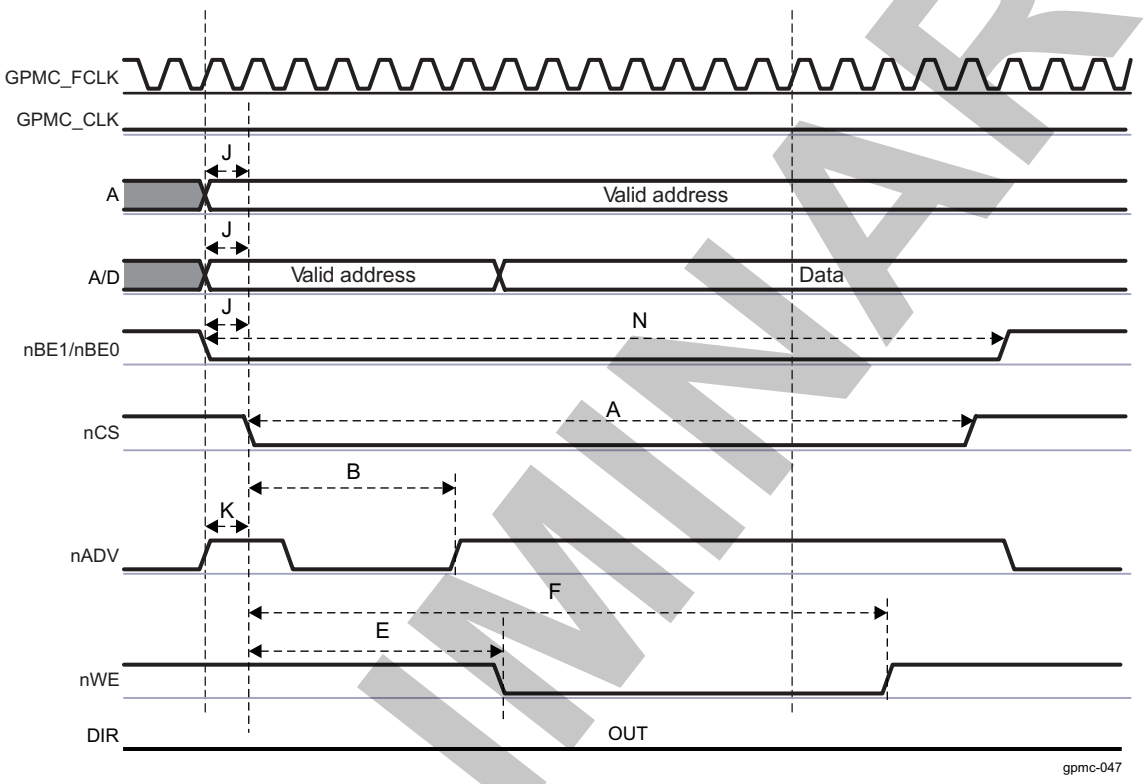
(TIMEPARAGRANULARITY + 1) * GPMC_FCLK period, where N = page burst access number

- O = ((WRCYCLETIME + (N – 1) * PAGEBURSTACCESSTIME – CSONTIME) * (TIMEPARAGRANULARITY + 1) + 0.5 * (ADVEXTRADELAY – CSEXTRADELAY)) * GPMC_FCLK period

Figure 15-96 shows a simplified example of an asynchronous NOR single write where formulas are associated with signal waves.

Figure 15-96. Asynchronous NOR Single Write Simplified Example



NOTE: Write multiple access is not supported in asynchronous mode. If WRITEMULTIPLE is enabled with WRITETYPE as asynchronous, the GPMC processes single asynchronous accesses.

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15.4.6 GPMC Use Cases and Tips

15.4.6.1 How to Set GPMC Timing Parameters for Typical Accesses

15.4.6.1.1 External Memory Attached to the GPMC Module

As discussed in the introduction to this chapter, the GPMC module supports the following external memory types:

- Asynchronous or synchronous, 8- or 16-bit-wide memory or device
- 16-bit address/data-multiplexed or not multiplexed NOR flash device
- 8- or 16-bit NAND flash device

The following examples describe how to calculate GPMC timing parameters by showing a typical parameter setup for the access to be performed.

The example is based on a 512-Mb multiplexed NOR flash memory with the following characteristics:

- Type: NOR flash (address/data-multiplexed mode)
- Size: 512M bits
- Data Bus: 16 bits wide
- Speed: 104-MHz clock frequency
- Read access time: 80 ns

15.4.6.1.2 Typical GPMC Setup

Table 15-378 lists some of the I/Os of the GPMC module.

Table 15-378. GPMC Signals

Signal Name	I/0	Description
GPMC_FCLK	Internal	Functional and interface clock. Acts as the time reference.
gpmc_clk(1)	O	External clock provided to the external device for synchronous operations
gpmc_a[25:16]	O	Address
gpmc_ad[15: 0]	I/O	Data-multiplexed with addresses A[16:1] on memory side
gpmc_ncsx	O	Chip-select (where x = 0, or 1)
gpmc_nadv_ale	O	Address valid enable
gpmc_noe_nre	O	Output enable (read access only)
gpmc_nwe	O	Write enable (write access only)
gpmc_wait[2:0]	I	Ready signal from memory device. Indicates when valid burst data is ready to be read

(1) This output signal is also used as a retiming input. During synchronous operation, the INPUTENABLE bit of the CONTROL_CORE_PAD0_GPMC_NWP_PAD1_GPMC_CLK register must be set to 1.

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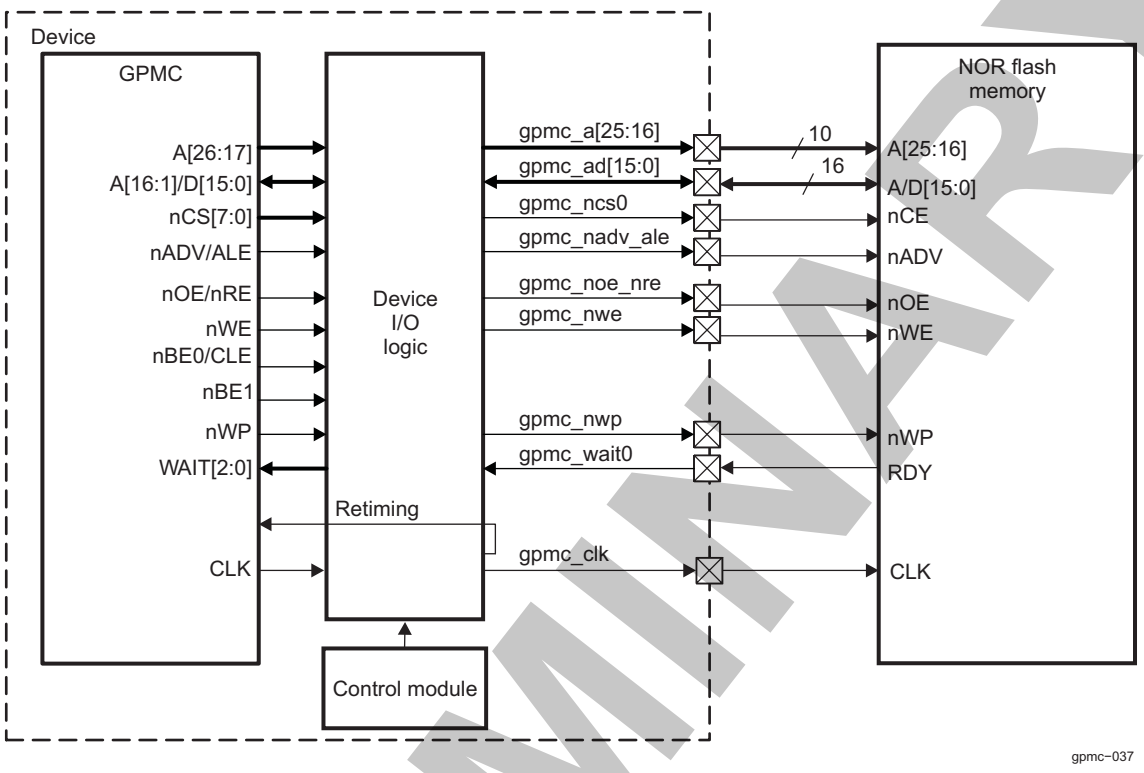
Figure 15-97 shows the typical connection between the GPMC module and an attached NOR Flash memory.

Figure 15-97. GPMC Connection to an External NOR Flash Memory



The following sections demonstrate how to calculate GPMC parameters for three access types:

- Synchronous burst read
- Asynchronous read
- Asynchronous single write

15.4.6.1.2.1 GPMC Configuration for Synchronous Burst Read Access

The clock runs at 104 MHz (f = 104 MHz; T = 9, 615 ns).

Table 15-379 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Table 15-380 shows how to calculate timings for the GPMC using the memory parameters.

Figure 15-98 shows the synchronous burst read access.

Table 15-379. Useful Timing Parameters on the Memory Side

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tCES	nCS setup time to clock	0
tACS	Address setup time to clock	3
tIACC	Synchronous access time	80
tBACC	Burst access time valid clock to output delay	5,2
tCEZ	Chip-select to High-Z	7
tOEZ	Output enable to High-Z	7
tAVC	nADV setup time	6

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Table 15-379. Useful Timing Parameters on the Memory Side (continued)

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tAVD	nAVD pulse	6
tACH	Address hold time from clock	3

The following terms, which describe the timing interface between the controller and its attached device, are used to calculate the timing parameters on the GPMC side:

- Read access time (GPMC side): Time required to activate the clock + read access time requested on the memory side + data setup time required for optimal capture of a burst of data
- Data setup time (GPMC side): Ensures a good capture of a burst of data (as opposed to taking a burst of data out). One word of data is processed in one clock cycle (T = 9,615 ns). The read access time between two bursts of data is tBACC = 5.2 ns. Therefore, data setup time is a clock period – tBACC = 4,415 ns of data setup.
- Access completion (GPMC side): (Different from page burst access time) Time required between the last burst access and access completion: nCS/nOE hold time (nCS and nOE must be released at the end of an access. These signals are held to allow the access to complete).
- Read cycle time (GPMC side): Read access time + access completion
- Write cycle time for burst access: Not supported for NOR flash memory

Table 15-380. Calculating GPMC Timing Parameters

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Register Configurations
GPMC FCLK Divider	–	–	–	GPMCFCLKDIVIDER = 0x0
ClkActivation Time	min (tCES, tACS)	3	1	CLKACTIVATIONTIME = 0x1
RdAccessTime	roundmax (ClkActivationTime + tIACC + DataSetupTime)	94.03: (9,615 + 80 + 4,415)	10: roundmax (94.03 / 9,615)	ACCESSTIME = 0x0A
PageBurst AccessTime	roundmax (tBACC)	roundmax (5.2)	1	PAGEBURSTACCESSTIME = 0x1
RdCycleTime	Access time + max (tCEZ, tOEZ)	101.03: (94.03 + 7)	11	RDCYCLETIME = 0x0B
CsOnTime	tCES	0	0	CSONTIME = 0x0
CsReadOffTime	RdCycleTime	-	11	CSRDOFFTIME = 0x0B
AdvOnTime	tAVC (1)	0	0	ADVONTIME = 0x0
AdvRdOffTime	tAVD + tAVC (2)	12	2	ADVRDOFFTIME = 0x02
OeOnTime (3)	(ClkActivationTime + tACH) < OeOnTime (ClkActivationTime + tIACC)	–	3, for instance	OEONTIME = 0x3
OeOffTime	RdCycleTime	–	11	OEOFFTIME = 0x0B

(1) The external clock provided to the NOR flash is not yet available.
(2) AdvRdOffTime – AdvOnTime = tAVD; thus, AdvRdOffTime = tAVD + AdvOnTime = tAVD + tAVC.
(3) OeOnTime must ensure that addresses are available. It must not exceed the availability of the first burst of data.

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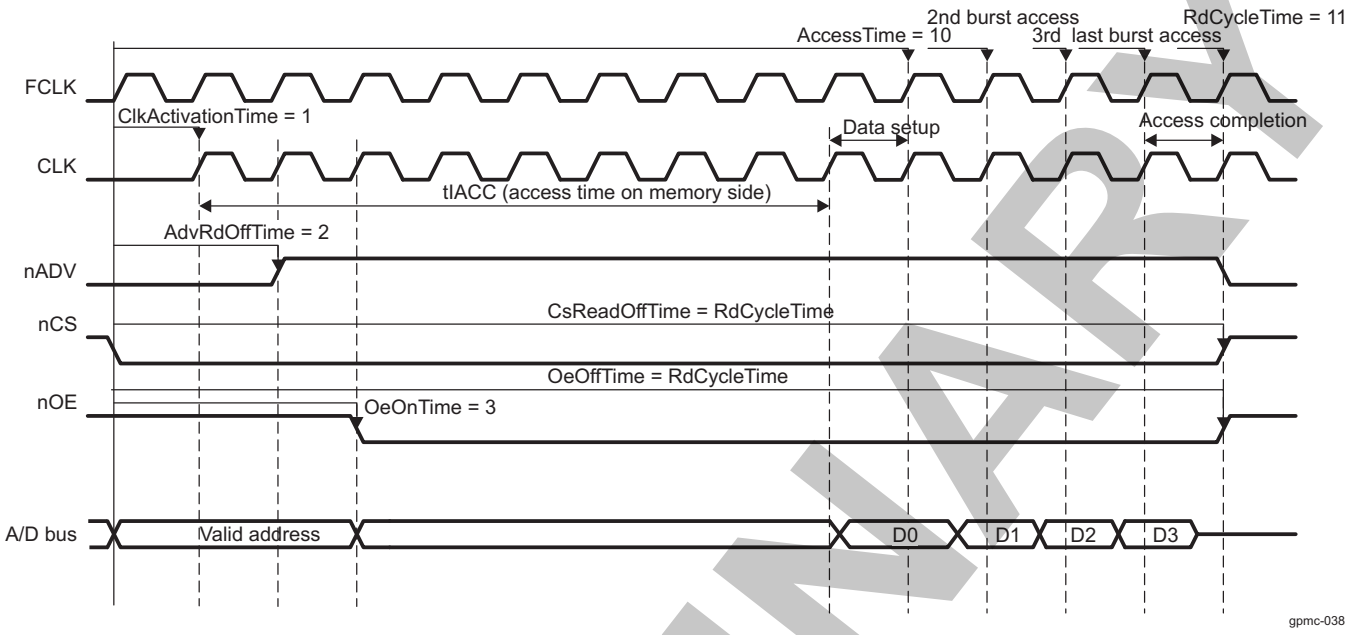
Figure 15-98. Synchronous Burst Read Access (Timing Parameters in Clock Cycles)



15.4.6.1.2.2 GPMC Configuration for Asynchronous Read Access

The clock runs at 104 MHz (f = 104 MHz; T = 9, 615 ns).

Table 15-381 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Table 15-382 shows how to calculate timings for the GPMC using the memory parameters.

Figure 15-99 shows the asynchronous read access.

Table 15-381. AC Characteristics for Asynchronous Read Access

AC Read Characteristics on the Memory Side	Description	Duration (ns)
tCE	Read Access time from nCS low	80
tAAVDS	Address setup time to rising edge of nADV	3
tAVDP	nADV low time	6
tCAS	nCS setup time to nADV	0
tOE	Output enable to output valid	6
tOEZ	Output enable to High-Z	7

Use the following formula to calculate the RdCycleTime parameter for this typical access:

RdCycleTime = RdAccessTime + AccessCompletion = RdAccessTime + 1 clock cycle + tOEZ:

1. On the memory side, the external memory makes the data available to the output bus. This is the memory-side read access time defined in Table 15-381: the number of clock cycles between the address capture (nADV rising edge) and the data valid on the output bus.

   The GPMC requires some hold time to allow the data to be captured correctly and the access to be finished.
2. To read the data correctly, the GPMC must be configured to meet the data setup time requirement of the memory; the GPMC module captures the data on the next rising edge. This is access time on the GPMC side.
3. There must also be a data hold time for correctly reading the data (checking that there is no nOE/nCS deassertion while reading the data). This data hold time is one clock cycle (that is, AccessTime + 1).

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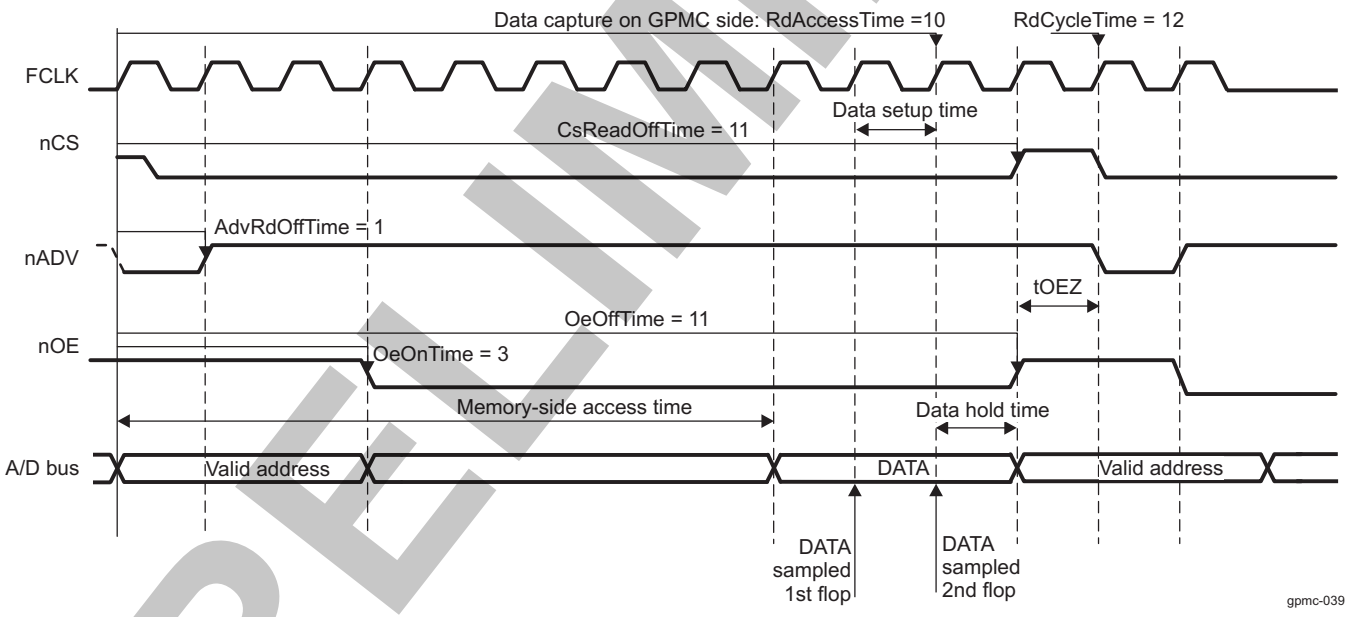
4. To complete the access, nOE/nCS signals are driven to High-Z. AccessTime + 1 + tOEZ is the read cycle time.
5. Addresses can now be relatched and a new read cycle begun.

Table 15-382. GPMC Timing Parameters for Asynchronous Read Access

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Register Configurations
ClkActivationTime	n/a (asynchronous mode)			
AccessTime	round max (tCE)	80	10	ACCESSTIME = 0x0A
PageBurstAccess Time	N/A (single access)			
RdCycleTime	AccessTime + 1cycle + tOEZ	96, 615	12	RDCYCLETIME = 0x0C
CsOnTime	tCAS	0	0	CSONTIME = 0x0
CsReadOffTime	AccessTime + 1 cycle	89, 615	11	CSRDOFFTIME = 0x0B
AdvOnTime	tAAVDS	3	1	ADVONTIME = 0X1
AdvRdOffTime	tAAVDS + tAVDP	9	1	ADVRDOFFTIME = 0x01
OeOnTime	OeOnTime >= AdvRdOffTime (multiplexed mode)	-	3, for instance	OEONTIME = 0x3
OeOffTime	AccessTime + 1cycle	89, 615	11	OEOFFTIME = 0x0B

Figure 15-99. Asynchronous Single Read Access (Timing Parameters in Clock Cycles)



15.4.6.1.2.3 GPMC Configuration for Asynchronous Single Write Access

The clock runs at 104 MHz: (f = 104 MHz; T = 9, 615 ns).

Table 15-384 shows how to calculate timings for the GPMC using the memory parameters.

Table 15-383 shows the timing parameters (on the memory side) that determine the parameters on the GPMC side.

Figure 15-100 shows the synchronous burst write access.

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Table 15-383. AC Characteristics for Asynchronous Single Write (Memory Side)

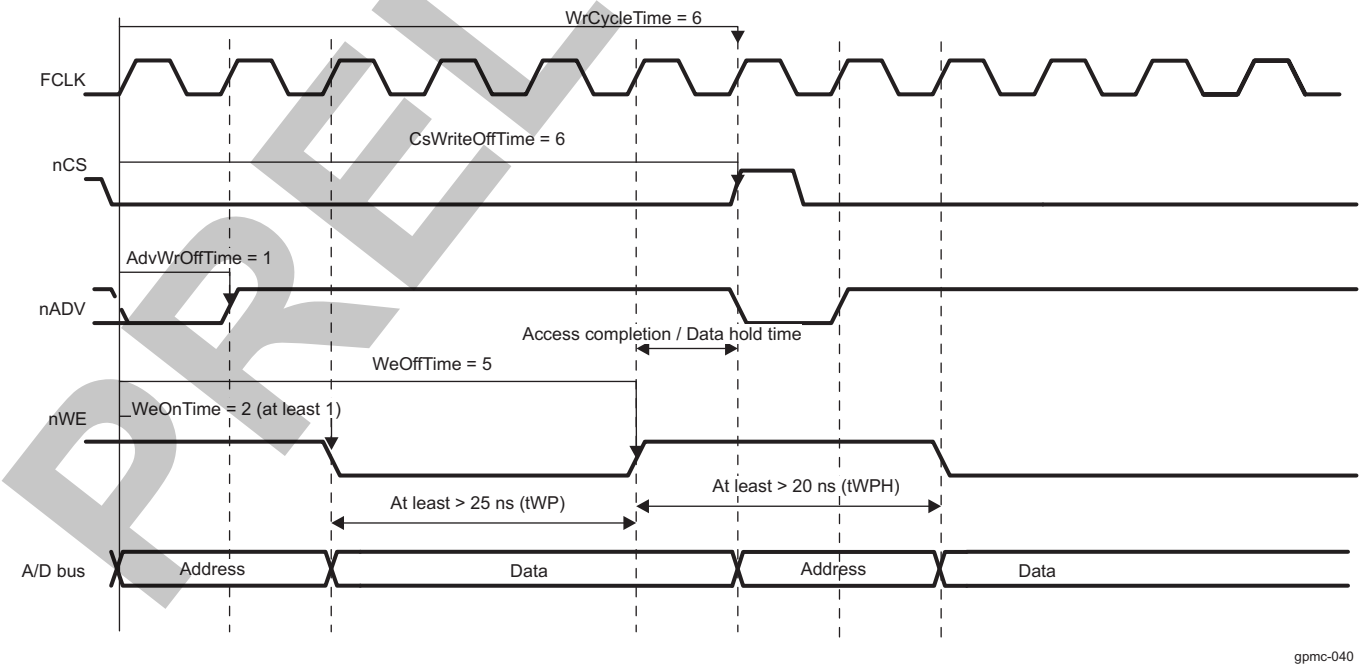
AC Characteristics on the Memory Side	Description	Duration (ns)
tWC	Write cycle time	60
tAVDP	nADV low time	6
tWP	Write pulse width	25
tWPH	Write pulse width high	20
tCS	nCS setup time to nWE	3
tCAS	nCS setup time to nADV	0
tAVSC	nADV setup time	3

For asynchronous single write access, write cycle time is WrCycleTime = WeOffTime + AccessCompletion = WeOffTime + 1. For the AccesCompletion, the GPMC requires one cycle of data hold time (nCS deassertion).

Table 15-384. GPMC Timing Parameters for Asynchronous Single Write

Parameter Name on GPMC Side	Formula	Duration (ns)	Number of Clock Cycles (F = 104 MHz)	GPMC Registers Configuration
ClkActivationTime	N/A (asynchronous mode)			
AccessTime	Applicable only to WAITMONITORING (the value is the same as for read access)			
PageBurstAccessTime	N/A (single access)			
WrCycleTime	WeOffTime + AccessCompletion	57, 615	6	WRCYCLETIME = 0x06
CsOnTime	tCAS	0	0	CSONTIME = 0x0
CsWrOffTime	WeOffTime + 1	57, 615	6	CSWROFFTIME = 0x06
AdvOnTime	tAVSC	3	1	ADVONTIME = 0x1
AdvWrOffTime	tAVSC + tAVDP	9	1	ADVWROFFTIME = 0x01
WeOnTime	tCS	3	1	WEONTIME = 0x1
WeOffTime	tCS + tWP + tWPH	48	5	WEOFFTIME = 0x05

Figure 15-100. Asynchronous Single Write Access (Timing Parameters in Clock Cycles)



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15.4.6.2 How to Choose a Suitable Memory to Use With the GPMC

This section is intended to help the user select a suitable memory device to interface with the GPMC controller.

15.4.6.2.1 Supported Memories or Devices

NAND flash and NOR flash architectures are the two flash technologies. The GPMC supports various types of external memory or devices, basically any one that supports NAND or NOR protocols:

- 8- and 16-bit-wide asynchronous or synchronous memory or device (only 8-bit: nonburst device)
- 16-bit address and data-multiplexed NOR flash devices (pSRAM, OneNAND™, etc.)
- 8- and 16-bit NAND flash devices

NOTE: Nonmultiplexed NOR flash devices are supported by the GPMC, but their use is highly limited. Because only 10 address pins are available on the GPMC interface, the maximum device size supported is 2KiB.

15.4.6.2.1.1 Memory Pin Multiplexing

This section describes the interfacing differences of the GPMC supported memories.

Table 15-385. Supported Memories Interfaces

Function	16-Bit Address/ Data-Multiplexed pSRAM or NOR Flash [1]	OneNAND	16-Bit NAND	8-Bit NAND
gpmc_a[25]	A26			
gpmc_a[24]	A25			
gpmc_a[23]	A24			
gpmc_a[22]	A23			
gpmc_a[21]	A22			
gpmc_a[20]	A21			
gpmc_a[19]	A20			
gpmc_a[18]	A19			
gpmc_a[17]	A18			
gpmc_a[16]	A17			
gpmc_ad[15]	D15 or A16		IO15	
gpmc_ad[14]	D14 or A15		IO14	
gpmc_ad[13]	D13 or A14		IO13	
gpmc_ad[12]	D12 or A13		IO12	
gpmc_ad[11]	D11 or A12		IO11	
gpmc_ad[10]	D10 or A11		IO10	
gpmc_ad[9]	D9 or A10		IO9	
gpmc_ad[8]	D8 or A9		IO8	
gpmc_ad[7]	D7 or A8		IO7	
gpmc_ad[6]	D6 or A7		IO6	
gpmc_ad[5]	D5 or A6		IO5	
gpmc_ad[4]	D4 or A5		IO4	
gpmc_ad[3]	D3 or A4		IO3	
gpmc_ad[2]	D2 or A3		IO2	
gpmc_ad[1]	D1 or A2		IO1	
gpmc_ad[0]	D0 or A1		IO0	

(1) Addresses seen from the device side. When interfacing to the external device, A1 is connected to the memory A0, A2 to the memory A1, and so on.

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Table 15-385. Supported Memories Interfaces (continued)

Function	16-Bit Address/ Data-Multiplexed pSRAM or NOR Flash [1]	OneNAND	16-Bit NAND	8-Bit NAND
gpmc_clk	CLK			
gpmc_ncs0	nCS0 (chip-select)		nCE0 (chip-enable)	
gpmc_ncs1	nCS1		nCE1	
gpmc_ncs2	nCS2		nCE2	
gpmc_ncs3	nCS3		nCE3	
gpmc_ncs4	nCS4		nCE4	
gpmc_ncs5	nCS5		nCE5	
gpmc_ncs6	nCS6		nCE6	
gpmc_ncs7	nCS7		nCE7	
gpmc_nadv_ale	nADV (address valid)		ALE (address latch enable)	
gpmc_noe	nOE (output enable)		nRE (read enable)	
gpmc_nwe	nWE (Write enable)		nWE (write enable)	
gpmc_nbe0_cle	nBE0 (byte enable)		CLE (command latch enable)	
gpmc_nbe1	nBE1			
gpmc_nwp	nWP (write protect)		nWP (write protect)	
gpmc_wait0	WAIT0		R/nB0 (ready/busy)	
gpmc_wait1	WAIT1		R/nB1	
gpmc_wait2	WAIT2		R/nB2	

15.4.6.2.1.2 NAND Interface Protocol

NAND flash architecture, introduced in 1989, is a flash technology. NAND is a page-oriented memory device; that is, read and write accesses are done by pages. NAND achieves great density by sharing common areas of the storage transistor, which creates strings of serially connected transistors (in NOR devices, each transistor stands alone). Because of its high density NAND is best suited to devices that require high capacity data storage, such as pictures, music, and data files. NAND nonvolatility makes of it a good storage solution for many applications where mobility, low power, and speed are key factors. Low pin count and simple interface are other advantages of NAND.

Table 15-386 summarizes the NAND interface signals level applied to external device or memories.

Table 15-386. NAND Interface Bus Operations Summary

Bus Operation	CLE	ALE	nCE	nWE [1]	nRE [1]	nWP
Read (cmd input)	H	L	L	RE	H	x
Read (add input)	L	H	L	RE	H	x
Write (cmd input)	H	L	L	RE	H	H
Write (add input)	L	H	L	RE	H	H
Data input	L	L	L	RE	H	H
Data output	L	L	L	H	FE	x
Busy (during read)	x	x	H [2]	H [2]	H [2]	x
Busy (during program)	x	x	x	x	x	H
Busy (during erase)	x	x	x	x	x	H
Write protect	x	x	x	x	x	L
Standby	x	x	H	x	x	H/L [3]

(1) RE stands for rising edge; FE stands for falling edge
(2) Can be nCE high, or WE and nRE high.
(3) nWP must be biased to CMOS high or CMOS low for standby

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15.4.6.2.1.3 NOR Interface Protocol

NOR flash architecture, introduced in 1988, is a flash technology. Unlike NAND, which is a sequential access device, NOR is directly addressable; that is, it is designed to be a random access device. NOR is best suited to devices used to store and run code or firmware, usually in small capacities. While NOR has fast read capabilities, it also has slow write and erase functions when compared to the NAND architecture.

Table 15-387 summarizes the level of the NOR interface signals applied to external devices or memories.

Table 15-387. NOR Interface Bus Operations Summary

Bus Operation	CLK	nADV	nCS	nOE	nWE	WAIT	DQ[15:0]
Read (asynchronous)	x	L	L	L	H	Asserted	Output
Read (synchronous)	Running	L	L	L	H	Driven	Output
Read (burst suspend)	Halted	x	L	H	H	Active	Output
Write	x	L	L	H	L	Asserted	Input
Output disable	x	x	L	H	H	Asserted	High-Z
Standby	x	x	H	x	x	High-Z	High-Z

15.4.6.2.1.4 Other Technologies

Other supported device types interact with the GPMC through the NOR interface protocol.

OneNAND is a high-density, low-power memory device. OneNAND is based on single- or multilevel-cell NAND core with SRAM and logic. It interfaces as a synchronous NOR flash and has synchronous write capability. It reads faster than conventional NAND and writes faster than conventional NOR flash. Hence, it is appropriate for mass storage and code storage.

pSRAM (pseudo-static random access memory) is a low-power memory device for mobile applications. pSRAM is based on the DRAM cell with internal refresh and address control features, and interfaces as a synchronous NOR flash. It also has synchronous write capability.

15.4.6.2.1.5 Supported Protocols

The GPMC supports the following interface protocols when communicating with external memory or external devices:

- Asynchronous read/write access
- Asynchronous read page access (4, 8, 16 Word16)
- Synchronous read/write access
- Synchronous read burst access without wrap capability (4, 8, 16 Word16)
- Synchronous read burst access with wrap capability (4, 8, 16 Word16)

15.4.6.2.2 GPMC Features and Settings

The features and settings of the GPMC are:

- Supported device type: Up to four NAND or NOR protocol external memories or devices
- Operating voltage: 1.8 V
- Maximum GPMC addressing capability: 512MiB divided into eight chip-selects
- Maximum supported memory size: 256MiB (must be a power-of-two)
- Minimum supported memory size: 16MiB (must be a power-of-two). Aliasing occurs when addressing smaller memories.
- Data path to external memory or device: 8, 16 bits wide
- Burst and page access: burst of 4, 8, 16 Word16
- Supports bus keeping
- Supports bus turnaround

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15.4.7 GPMC Register Manual

This section provides information about the GPMC instance in this product. Table 15-389 provides a summary of the GPMC registers. The remaining parts of this section describe the registers within the module instance.

15.4.7.1 GPMC Register Summary

Table 15-388. GPMC Instance Summary

Module Name	Base Address	Size
GPMC	0x5000 0000	32 MiB

Table 15-389. GPMC Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address GPMC
GPMC_REVISION	R	32	0x0000 0000	0x5000 0000
GPMC_SYSCONFIG	RW	32	0x0000 0010	0x5000 0010
GPMC_SYSSTATUS	R	32	0x0000 0014	0x5000 0014
GPMC_IRQSTATUS	RW	32	0x0000 0018	0x5000 0018
GPMC_IRQENABLE	RW	32	0x0000 001C	0x5000 001C
GPMC_TIMEOUT_CONTROL	RW	32	0x0000 0040	0x5000 0040
GPMC_ERR_ADDRESS	RW	32	0x0000 0044	0x5000 0044
GPMC_ERR_TYPE	RW	32	0x0000 0048	0x5000 0048
GPMC_CONFIG	RW	32	0x0000 0050	0x5000 0050
GPMC_STATUS	RW	32	0x0000 0054	0x5000 0054
GPMC_CONFIG1_i (1)	RW	32	0x0000 0060 + (0x0000 0030 * i)	0x5000 0060 + (0x0000 0030 * i)
GPMC_CONFIG2_i (1)	RW	32	0x0000 0064 + (0x0000 0030 * i)	0x5000 0064 + (0x0000 0030 * i)
GPMC_CONFIG3_i (1)	RW	32	0x0000 0068 + (0x0000 0030 * i)	0x5000 0068 + (0x0000 0030 * i)
GPMC_CONFIG4_i (1)	RW	32	0x0000 006C + (0x0000 0030 * i)	0x5000 006C + (0x0000 0030 * i)
GPMC_CONFIG5_i (1)	RW	32	0x0000 0070 + (0x0000 0030 * i)	0x5000 0070 + (0x0000 0030 * i)
GPMC_CONFIG6_i (1)	RW	32	0x0000 0074 + (0x0000 0030 * i)	0x5000 0074 + (0x0000 0030 * i)
GPMC_CONFIG7_i (1)	RW	32	0x0000 0078 + (0x0000 0030 * i)	0x5000 0078 + (0x0000 0030 * i)
GPMC_NAND_COMMAND_i (1)	W	32	0x0000 007C + (0x0000 0030 * i)	0x5000 007C + (0x0000 0030 * i)
GPMC_NAND_ADDRESS_i (1)	W	32	0x0000 0080 + (0x0000 0030 * i)	0x5000 0080 + (0x0000 0030 * i)
GPMC_NAND_DATA_i (1)	RW	32	0x0000 0084 + (0x0000 0030 * i)	0x5000 0084 + (0x0000 0030 * i)
GPMC_PREFETCH_CONFIG1	RW	32	0x0000 01E0	0x5000 01E0
GPMC_PREFETCH_CONFIG2	RW	32	0x0000 01E4	0x5000 01E4
GPMC_PREFETCH_CONTROL	RW	32	0x0000 01EC	0x5000 01EC
GPMC_PREFETCH_STATUS	RW	32	0x0000 01F0	0x5000 01F0
GPMC_ECC_CONFIG	RW	32	0x0000 01F4	0x5000 01F4
GPMC_ECC_CONTROL	RW	32	0x0000 01F8	0x5000 01F8
GPMC_ECC_SIZE_CONFIG	RW	32	0x0000 01FC	0x5000 01FC
GPMC_ECCj_RESULT (2)	RW	32	0x0000 0200 + (0x0000 0004 * j)	0x5000 0200 + (0x0000 0004 * j)
GPMC_BCH_RESULT0_i (1)	RW	32	0x0000 0240 + (0x0000 0010 * i)	0x5000 0240 + (0x0000 0010 * i)
GPMC_BCH_RESULT1_i (1)	RW	32	0x0000 0244 + (0x0000 0010 * i)	0x5000 0244 + (0x0000 0010 * i)
GPMC_BCH_RESULT2_i (1)	RW	32	0x0000 0248 + (0x0000 0010 * i)	0x5000 0248 + (0x0000 0010 * i)
GPMC_BCH_RESULT3_i (1)	RW	32	0x0000 024C + (0x0000 0010 * i)	0x5000 024C + (0x0000 0010 * i)
GPMC_BCH_RESULT4_i (1)	RW	32	0x0000 0300 + (0x0000 0010 * i)	0x5000 0300 + (0x0000 0010 * i)
GPMC_BCH_RESULT5_i (1)	RW	32	0x0000 0304 + (0x0000 0010 * i)	0x5000 0304 + (0x0000 0010 * i)
GPMC_BCH_RESULT6_i (1)	RW	32	0x0000 0308 + (0x0000 0010 * i)	0x5000 0308 + (0x0000 0010 * i)
GPMC_BCH_SWDATA	RW	32	0x0000 02D0	0x5000 02D0

(1) i = 0 to 7 for GPMC
(2) j = 0 to 8 for GPMC

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15.4.7.2 GPMC Register Descriptions

NOTE: All GPMC registers are aligned to 32-bit address boundaries. All register file accesses, except to GPMC_NAND_DATA_i register, are little-endian. If the GPMC_NAND_DATA_i register location is accessed, the endianness is access-dependent.

In this section i corresponds to the chip-select number, where i = 0 to 7.

Table 15-390. GPMC_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5000 0000	**Instance**	GPMC
Description	This register contains the IP revision code.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 15-391. Register Call Summary for Register GPMC_REVISION

General-Purpose Memory Controller
- GPMC Register Summary: [0]

Table 15-392. GPMC_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5000 0010	**Instance**	GPMC
Description	This register controls the various parameters of the interconnect.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IDLEMODE		RESERVED	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0000000
4:3	IDLEMODE	0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged. 0x2: Smart-idle. Acknowledgment to an idle request is given based on the internal activity of the module. 0x3: Do not use.	RW	0x0
2	RESERVED	Write 0 for future compatibility Read returns 0.	RW	0x0
1	SOFTRESET	Software reset. Set this bit to 1 triggers a module reset. This bit is automatically reset by hardware. During reads, it always returns 0. 0x0: Normal mode 0x1: The module is reset.	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	AUTOIDLE	Internal interface clock-gating strategy 0x0: Interface clock is free-running. 0x1: Automatic Interface clock gating strategy is applied, based on the interconnect activity.	RW	0x0

Table 15-393. Register Call Summary for Register GPMC_SYSCONFIG

General-Purpose Memory Controller
- GPMC Software Reset: [0]
- GPMC Power Management: [1] [2]
- GPMC Initialization: [3]
- GPMC Register Summary: [4]

Table 15-394. GPMC_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5000 0014	**Instance**	GPMC
Description	This register provides status information about the module, excluding the interrupt status information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED							RESETDONE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:1	RESERVED	Read returns 0 (reserved for interconnect-socket status information).	R	0x00
0	RESETDONE	Internal reset monitoring 0x0: Internal module reset is ongoing. 0x1: Reset is complete.	R	0x-

Table 15-395. Register Call Summary for Register GPMC_SYSSTATUS

General-Purpose Memory Controller
- GPMC Software Reset: [0]
- GPMC Initialization: [1]
- GPMC Register Summary: [2]

Table 15-396. GPMC_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5000 0018	**Instance**	GPMC
Description	This interrupt status register regroups all the status of the module internal events that can generate an interrupt.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					WAIT2EDGEDETECTIONSTATUS	WAIT1EDGEDETECTIONSTATUS	WAIT0EDGEDETECTIONSTATUS	RESERVED						TERMINALCOUNTSTATUS	FIFOEVENTSTATUS

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
10	WAIT2EDGEDETECTIONSTATUS	Status of the Wait2 Edge Detection interrupt Read 0x0: A transition on WAIT2 input pin has not been detected. Write 0x0: WAIT2EDGEDETECTIONSTATUS bit is unchanged. Read 0x1: A transition on WAIT2 input pin has been detected. Write 0x1: WAIT2EDGEDETECTIONSTATUS bit is reset.	RW	0x0
9	WAIT1EDGEDETECTIONSTATUS	Status of the Wait1 Edge Detection interrupt Read 0x0: A transition on WAIT1 input pin has not been detected. Write 0x0: WAIT1EDGEDETECTIONSTATUS bit is unchanged. Read 0x1: A transition on WAIT1 input pin has been detected. Write 0x1: WAIT1EDGEDETECTIONSTATUS bit is reset.	RW	0x0
8	WAIT0EDGEDETECTIONSTATUS	Status of the Wait0 Edge Detection interrupt Read 0x0: A transition on WAIT0 input pin has not been detected. Write 0x0: WAIT0EDGEDETECTIONSTATUS bit is unchanged. Read 0x1: A transition on WAIT0 input pin has been detected. Write 0x1: WAIT0EDGEDETECTIONSTATUS bit is reset.	RW	0x0
7:2	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00
1	TERMINALCOUNTSTATUS	Status of the TerminalCountEvent interrupt Read 0x0: Indicates that CountValue is greater than 0 Write 0x0: TERMINALCOUNTSTATUS bit is unchanged. Read 0x1: Indicates that CountValue is equal to 0 Write 0x1: TERMINALCOUNTSTATUS bit is reset.	RW	0x0
0	FIFOEVENTSTATUS	Status of the FIFOEvent interrupt Read 0x0: Indicates that less than GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bytes are available in prefetch mode and less than FIFOTHRESHOLD bytes free places are available in write-posting mode Write 0x0: FIFOEVENTSTATUS bit is unchanged. Read 0x1: Indicates that at least GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bytes are available in prefetch mode and at least FIFOTHRESHOLD bytes free places are available in write-posting mode Write 0x1: FIFOEVENTSTATUS bit is reset.	RW	0x0

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Table 15-397. Register Call Summary for Register GPMC_IRQSTATUS

General-Purpose Memory Controller

- GPMC Interrupt Requests: [0] [1] [2] [3] [4]
- NAND Device-Ready Pin: [5] [6] [7]
- Prefetch and Write-Posting Engine: [8] [9] [10] [11]
- GPMC Register Summary: [12]

Table 15-398. GPMC_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x5000 001C	**Instance**	GPMC
Description	The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on a event-by-event basis.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					WAIT2EDGEDETECTIONENABLE	WAIT1EDGEDETECTIONENABLE	WAIT0EDGEDETECTIONENABLE	RESERVED						TERMINALCOUNTEVENTENABLE	FIFOEVENTENABLE

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
10	WAIT2EDGEDETECTIONENABLE	Enables the Wait2 Edge Detection interrupt 0x0: Wait2EdgeDetection interrupt is masked. 0x1: Wait2EdgeDetection event generates an interrupt if occurs.	RW	0
9	WAIT1EDGEDETECTIONENABLE	Enables the Wait1 Edge Detection interrupt 0x0: Wait1EdgeDetection interrupt is masked. 0x1: Wait1EdgeDetection event generates an interrupt if occurs.	RW	0x0
8	WAIT0EDGEDETECTIONENABLE	Enables the Wait0 Edge Detection interrupt 0x0: Wait0EdgeDetection interrupt is masked. 0x1: Wait0EdgeDetection event generates an interrupt if occurs.	RW	0x0
7:2	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00
1	TERMINALCOUNTEVENTENABLE	Enables TerminalCountEvent interrupt issuing in prefetch or write-posting mode 0x0: TerminalCountEvent interrupt is masked. 0x1: TerminalCountEvent interrupt is not masked.	RW	0x0
0	FIFOEVENTENABLE	Enables the FIFOEvent interrupt 0x0: FIFOEvent interrupt is masked. 0x1: FIFOEvent interrupt is not masked.	RW	0x0

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Table 15-399. Register Call Summary for Register GPMC_IRQENABLE

General-Purpose Memory Controller

- GPMC Interrupt Requests: [0] [1] [2] [3] [4]
- NAND Device-Ready Pin: [5] [6]
- Prefetch and Write-Posting Engine: [7] [8] [9] [10]
- GPMC Register Summary: [11]

Table 15-400. GPMC_TIMEOUT_CONTROL

Address Offset	0x0000 0040		
Physical Address	0x5000 0040	**Instance**	GPMC
Description	The GPMC_TIMEOUT_CONTROL register allows the user to set the start value of the timeout counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TIMEOUTSTARTVALUE								RESERVED							TIMEOUTENABLE

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00000
12:4	TIMEOUTSTARTVALUE	Start value of the time-out counter 0x000: Zero GPMC_FCLK cycle 0x001: One GPMC_FCLK cycle ... 0x1FF: 511 GPMC_FCLK cycles	RW	0x1FF
3:1	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
0	TIMEOUTENABLE	Enable bit of the TimeOut feature 0x0: TimeOut feature is disabled. 0x1: TimeOut feature is enabled.	RW	0x0

Table 15-401. Register Call Summary for Register GPMC_TIMEOUT_CONTROL

General-Purpose Memory Controller

- Error Handling: [0] [1]
- GPMC Register Summary: [2]
- GPMC Register Descriptions: [3]

Table 15-402. GPMC_ERR_ADDRESS

Address Offset	0x0000 0044		
Physical Address	0x5000 0044	**Instance**	GPMC
Description	The GPMC_ERR_ADDRESS register stores the address of the illegal access when an error occurs.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	ILLEGALADD																														

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
30:0	ILLEGALADD	Address of illegal access A30: 0 for memory region, 1 for GPMC register region A29-A0: 1 GiB maximum	R	0x00000000

Table 15-403. Register Call Summary for Register GPMC_ERR_ADDRESS

General-Purpose Memory Controller

- Error Handling: [0]
- GPMC Register Summary: [1]
- GPMC Register Descriptions: [2]

Table 15-404. GPMC_ERR_TYPE

Address Offset	0x0000 0048		
Physical Address	0x5000 0048	**Instance**	GPMC
Description	The GPMC_ERR_TYPE register stores the type of error when an error occurs.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					ILLEGALMCMD			RESERVED			ERRORNOTSUPPADD	ERRORNOTSUPPMCMD	ERRORTIMEOUT	RESERVED	ERRORVALID

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
10:8	ILLEGALMCMD	System command of the transaction that caused the error	R	0x0
7:5	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
4	ERRORNOTSUPPADD	Not supported address error 0x0: No error occurs. 0x1: The error is due to a nonsupported address.	R	0x0
3	ERRORNOTSUPPMCMD	Not supported command error 0x0: No error occurs. 0x1: The error is due to a nonsupported command	R	0x0
2	ERRORTIMEOUT	Time-out error 0x0: No error occurs. 0x1: The error is due to a timeout.	R	0x0
1	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
0	ERRORVALID	Error validity status - Must be explicitly cleared with a write 1 transaction 0x0: All error fields no longer valid 0x1: Error detected and logged in the other error fields	RW	0x0

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Table 15-405. Register Call Summary for Register GPMC_ERR_TYPE

General-Purpose Memory Controller

- Error Handling: [0] [1] [2]
- GPMC Register Summary: [3]
- GPMC Register Descriptions: [4]

Table 15-406. GPMC_CONFIG

Address Offset	0x0000 0050		
Physical Address	0x5000 0050	**Instance**	GPMC
Description	The configuration register allows global configuration of the GPMC.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					WAIT2PINPOLARITY	WAIT1PINPOLARITY	WAIT0PINPOLARITY	RESERVED			WRITEPROTECT	RESERVED		LIMITEDADDRESS	NANDFORCEPOSTEDWRITE

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
10	WAIT2PINPOLARITY	Selects the polarity of input pin WAIT2 0x0: WAIT2 active low 0x1: WAIT2 active high	RW	0x0
9	WAIT1PINPOLARITY	Selects the polarity of input pin WAIT1 0x0: WAIT1 active low 0x1: WAIT1 active high	RW	0x1
8	WAIT0PINPOLARITY	Selects the polarity of input pin WAIT0 0x0: WAIT0 active low 0x1: WAIT0 active high	RW	0x0
7:5	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
4	WRITEPROTECT	Controls the WP output pin level 0x0: WP output pin is low. 0x1: WP output pin is high.	RW	0x0
3:2	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
1	LIMITEDADDRESS	Limited Address device support 0x0: No effect 0x1: A26-A11 are not modified during an external memory access.	RW	0x0
0	NANDFORCEPOSTEDWRITE	Enables the Force Posted Write feature to NAND Cmd/Add/Data location 0x0: Disables Force Posted Write 0x1: Enables Force Posted Write	RW	0x0

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Table 15-407. Register Call Summary for Register GPMC_CONFIG

General-Purpose Memory Controller

- GPMC Signals: [0]
- GPMC Interrupt Requests: [1] [2] [3]
- GPMC Address and Data Bus: [4]
- GPMC I/O Configuration Setting: [5] [6]
- External Signals: [7] [8]
- Asynchronous and Synchronous Accesses in Nonmultiplexed Mode: [9] [10] [11] [12] [13]
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [14]
- NAND Device-Ready Pin: [15]
- Set Memory Access: [16]
- GPMC Register Summary: [17]

Table 15-408. GPMC_STATUS

Address Offset	0x0000 0054		
Physical Address	0x5000 0054	**Instance**	GPMC
Description	The status register provides global status bits of the GPMC.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					WAIT2STATUS	WAIT1STATUS	WAIT0STATUS	RESERVED							EMPTYWRITEBUFFERSTATUS

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
10	WAIT2STATUS	Is a copy of input pin WAIT2. (Reset value is WAIT2 input pin sampled at device reset.) 0x0: WAIT2 asserted (inactive state) 0x1: WAIT2 deasserted	R	0x-
9	WAIT1STATUS	Is a copy of input pin WAIT1. (Reset value is WAIT1 input pin sampled at device reset.) 0x0: WAIT1 asserted (inactive state) 0x1: WAIT1 deasserted	R	0x-
8	WAIT0STATUS	Is a copy of input pin WAIT0. (Reset value is WAIT0 input pin sampled at device reset.) 0x0: WAIT0 asserted (inactive state) 0x1: WAIT0 deasserted	R	0x-
7:1	RESERVED	Write 0s for future compatibility. Reads returns 0	RW	0x00
0	EMPTYWRITEBUFFERSTATUS	Stores the empty status of the write buffer 0x0: Write buffer is not empty. 0x1: Write buffer is empty.	R	0x1

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Table 15-409. Register Call Summary for Register GPMC_STATUS

General-Purpose Memory Controller

- NAND Memory Device in Byte or 16-bit Word Stream Mode: [0]
- NAND Device-Ready Pin: [1] [2] [3]
- GPMC Register Summary: [4]

Table 15-410. GPMC_CONFIG1_i

Address Offset	0x0000 0060 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0060 + (0x0000 0030 * i)	**Instance**	GPMC
Description	The configuration register 1 sets signal control parameters per chip-select.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRAPBURST	READMULTIPLE	READTYPE	WRITEMULTIPLE	WRITETYPE	CLKACTIVATIONTIME			ATTACHEDDEVICEPAGELENGTH		WAITREADMONITORING	WAITWRITEMONITORING	RESERVED		WAITMONITORINGTIME		WAITPINSELECT		RESERVED		DEVICESIZE		DEVICETYPE		MUXADDDATA		RESERVED			TIMEPARAGRANULARITY	RESERVED		GPMCFCLKDIVIDER	

Bits	Field Name	Description	Type	Reset
31	WRAPBURST	Enables the wrapping burst capability. Must be set if the attached device is configured in wrapping burst 0x0: Synchronous wrapping burst not supported 0x1: Synchronous wrapping burst supported	RW	0x0
30	READMULTIPLE	Selects the read single or multiple access 0x0: Single access 0x1: Multiple access (burst if synchronous, page if asynchronous)	RW	0x0
29	READTYPE	Selects the read mode operation 0x0: Read asynchronous 0x1: Read synchronous	RW	0x0
28	WRITEMULTIPLE	Selects the write single or multiple access 0x0: Single access 0x1: Multiple access (burst if synchronous, considered as single if asynchronous)	RW	0x0
27	WRITETYPE	Selects the write mode operation 0x0: Write asynchronous 0x1: Write synchronous	RW	0x0
26:25	CLKACTIVATIONTIME	Output GPMC_CLK activation time 0x0: First rising edge of GPMC_CLK at start access time 0x1: First rising edge of GPMC_CLK one GPMC_FCLK cycle after start access time 0x2: First rising edge of GPMC_CLK two GPMC_FCLK cycles after start access time 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
24:23	ATTACHEDDEVICEPAGELENGTH	Specifies the attached device page (burst) length 0x0: 4 words 0x1: 8 words 0x2: 16 words 0x3: Reserved (1 word = interface size)	RW	0x0
22	WAITREADMONITORING	Selects the Wait monitoring configuration for Read accesses (Reset value is *bootwaiten* input pin sampled at device reset) 0x0: Wait pin is not monitored for read accesses. 0x1: Wait pin is monitored for read accesses.	RW	0x-
21	WAITWRITEMONITORING	Selects the Wait monitoring configuration for Write accesses 0x0: Wait pin is not monitored for write accesses. 0x1: Wait pin is monitored for write accesses.	RW	0x0
20	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
19:18	WAITMONITORINGTIME	Selects input pin Wait monitoring time 0x0: Wait pin is monitored with valid data. 0x1: Wait pin is monitored one GPMC_CLK cycle before valid data. 0x2: Wait pin is monitored two GPMC_CLK cycle before valid data. 0x3: Reserved	RW	0x0
17:16	WAITPINSELECT	Selects the input wait pin for this chip-select (Reset value is *bootwaitselect* input pin sampled at device reset for CS0 and 0 for CS1-7) 0x0: Wait input pin is WAIT0. 0x1: Wait input pin is WAIT1. 0x2: Wait input pin is WAIT2. 0x3: Reserved	RW	0x-
15:14	RESERVED	Write 0s for future compatibility. Reads returns 0	RW	0x0
13:12	DEVICESIZE	Selects the device size attached (Reset value is *bootdevicesize* input pin sampled at device reset for CS0 and 0x1 for CS1 to CS7) 0x0: 8 bit 0x1: 16 bit 0x2: Reserved 0x3: Reserved	RW	0x-
11:10	DEVICETYPE	Selects the attached device type 0x0: NOR flash-like, asynchronous and synchronous devices 0x1: Reserved 0x2: NAND flash-like devices, stream mode 0x3: Reserved	RW	0x0
9:8	MUXADDDATA	Enables the address and data multiplexed protocol (Reset value is *cs0muxdevice* input pin sampled at device reset for CS0 and 0 for CS1-CS7) 0x0: Nonmultiplexed attached device 0x1: AAD-multiplexed protocol device 0x2: Address and data multiplexed attached device 0x3: Reserved	RW	0x-
7:5	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0

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Bits	Field Name	Description	Type	Reset
4	TIMEPARAGRANULARITY	Signals timing latencies scalar factor (RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS) 0x0: x1 latencies 0x1: x2 latencies	RW	0x0
3:2	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
1:0	GPMCFCLKDIVIDER	Divides the GPMC_FCLK clock 0x0: GPMC_CLK frequency = GPMC_FCLK frequency 0x1: GPMC_CLK frequency = GPMC_FCLK frequency / 2 0x2: GPMC_CLK frequency = GPMC_FCLK frequency / 3 0x3: GPMC_CLK frequency = GPMC_FCLK frequency /4	RW	0x0

Table 15-411. Register Call Summary for Register GPMC_CONFIG1_i

General-Purpose Memory Controller

- GPMC Signals: [0]
- GPMC Clock Configuration: [1] [2]
- L3 Interconnect Interface: [3] [4]
- GPMC I/O Configuration Setting: [5] [6] [7] [8] [9] [10] [11] [12]
- GPMC CS0 Default Configuration at Device Reset: [13] [14] [15] [16]
- Access Protocol: [17] [18] [19]
- External Signals: [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36]
- Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME): [37]
- GPMC_CLK: [38] [39]
- GPMC_CLK and Control Signals Setup and Hold: [40]
- Access Time (RDACCESSTIME / WRACCESSTIME): [41]
- Page Burst Access Time (PAGEBURSTACCESSTIME): [42]
- NOR Access Description: [43] [44]
- Asynchronous Access Description: [45] [46] [47] [48]
- Synchronous Access Description: [49] [50] [51] [52] [53]
- Page and Burst Support: [54] [55]
- System Burst vs External Device Burst Support: [56] [57] [58]
- pSRAM Access Specificities: [59]
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74] [75] [76] [77]
- NAND Device-Ready Pin: [78] [79]
- GPMC Configuration in NOR Mode: [80] [81] [82] [83] [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95]
- GPMC Configuration in NAND Mode: [96] [97] [98] [99]
- Set Memory Access: [100] [101] [102] [103] [104]
- GPMC Timing Parameters: [105] [106] [107] [108] [109] [110] [111] [112] [113]
- GPMC Timing Parameters Formulas: [114] [115] [116] [117] [118] [119] [120] [121] [122] [123] [124] [125] [126]
- GPMC Register Summary: [127]

Table 15-412. GPMC_CONFIG2_i

Address Offset	0x0000 0064 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0064 + (0x0000 0030 * i)	**Instance**	GPMC
Description	CS signal timing parameter configuration		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											CSWROFFTIME					RESERVED			CSRDOFFTIME					CSEXTRADELAY	RESERVED			CSONTIME			

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000
20:16	CSWROFFTIME	CS i deassertion time from start cycle time for write accesses 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x10
15:13	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
12:8	CSRDOFFTIME	CS i de-assertion time from start cycle time for read accesses 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x10
7	CSEXTRADELAY	CS i Add extra half-GPMC_FCLK cycle 0x0: CS i Timing control signal is not delayed 0x1: CS i Timing control signal is delayed of half GPMC_FCLK clock cycle	RW	0x0
6:4	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
3:0	CSONTIME	CS i assertion time from start cycle time 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x1

Table 15-413. Register Call Summary for Register GPMC_CONFIG2_i

General-Purpose Memory Controller

- nCS: Chip-Select Signal Control Assertion/Deassertion Time (CSONTIME / CSRDOFFTIME / CSWROFFTIME / CSEXTRADELAY): [0] [1] [2] [3]
- Asynchronous Access Description: [4] [5]
- Synchronous Access Description: [6] [7] [8] [9]
- GPMC Timing Parameters: [10] [11] [12] [13]
- GPMC Register Summary: [14]

Table 15-414. GPMC_CONFIG3_i

Address Offset	0x0000 0068 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0068 + (0x0000 0030 * i)	**Instance**	GPMC
Description	nADV signal timing parameter configuration		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	ADVAADMUXWROFFTIME			RESERVED	ADVAADMUXRDOFFTIME			RESERVED	ADVWROFFTIME							RESERVED	ADVRDOFFTIME							ADVEXTRADELAY	ADVAADMUXONTIME			ADVONTIME			

Bits	Field Name	Description	Type	Reset
31	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0
30:28	ADVAADMUXWROFFTIME	nADV deassertion for first address phase when using the AAD-multiplexed protocol 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x2
27	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0
26:24	ADVAADMUXRDOFFTIME	nADV assertion for first address phase when using the AAD-multiplexed protocol 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x2
23:21	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
20:16	ADVWROFFTIME	nADV deassertion time from start cycle time for write accesses 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x06
15:13	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
12:8	ADVRDOFFTIME	nADV deassertion time from start cycle time for read accesses 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x05
7	ADVEXTRADELAY	nADV add extra half-GPMC_FCLK cycle 0x0: nADV timing control signal is not delayed 0x1: nADV timing control signal is delayed of half GPMC_FCLK clock cycle	RW	0
6:4	ADVAADMUXONTIME	nADV assertion for first address phase when using the AAD-multiplexed protocol 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x1
3:0	ADVONTIME	nADV assertion time from start cycle time 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x4

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Table 15-415. Register Call Summary for Register GPMC_CONFIG3_i

General-Purpose Memory Controller

- nADV/ALE: Address Valid/Address Latch Enable Signal Control Assertion/Deassertion Time (ADVONTIME / ADVRDOFFTIME / ADVWROFFTIME / ADVEXTRADELAY/ADVAADMUXONTIME/ADVAADMUXRDOFFTIME/ADVAADMUXWROFFTIME): [0] [1] [2] [3] [4] [5] [6]
- Asynchronous Access Description: [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
- Synchronous Access Description: [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31]
- GPMC Timing Parameters: [32] [33] [34] [35] [36] [37] [38]
- GPMC Register Summary: [39]

Table 15-416. GPMC_CONFIG4_i

Address Offset	0x0000 006C + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 006C + (0x0000 0030 * i)	**Instance**	GPMC
Description	nWE and nOE signals timing parameter configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			WEOFFTIME					WEEXTRADELAY	RESERVED			WEONTIME				OEAADMUXOFFTIME			OEOFFTIME					OEEXTRADELAY	OEAADMUXONTIME			OEONTIME			

Bits	Field Name	Description	Type	Reset
31:29	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
28:24	WEOFFTIME	nWE deassertion time from start cycle time 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x10
23	WEEXTRADELAY	nWE add extra half-GPMC_FCLK cycle 0x0: nWE timing control signal is not delayed 0x1: nWE timing control signal is delayed of half-GPMC_FCLK clock cycle	RW	0
22:20	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
19:16	WEONTIME	nWE assertion time from start cycle time 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x5
15:13	OEAADMUX OFFTIME	nOE deassertion time for the first address phase in an AAD-multiplexed access 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x3
12:8	OEOFFTIME	nOE deassertion time from start cycle time 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x10
7	OEEXTRADELAY	nOE add extra half-GPMC_FCLK cycle 0x0: nOE timing control signal is not delayed 0x1: nOE timing control signal is delayed of half-GPMC_FCLK clock cycle	RW	0x0

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Bits	Field Name	Description	Type	Reset
6:4	OEAADMUX ONTIME	nOE assertion time for the first address phase in an AAD-mux access 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x1
3:0	OEONTIME	nOE assertion time from start cycle time 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x6

Table 15-417. Register Call Summary for Register GPMC_CONFIG4_i

General-Purpose Memory Controller

- nOE/nRE: Output Enable/Read Enable Signal Control Assertion/Deassertion Time (OEONTIME / OEOFFTIME / OEEXTRADELAY / OEAADMUXONTIME / OEAADMUXOFFTIME): [0] [1] [2]
- nWE: Write Enable Signal Control Assertion/Deassertion Time (WEONTIME / WEOFFTIME / WEEXTRADELAY): [3] [4] [5]
- Asynchronous Access Description: [6] [7] [8] [9] [10] [11] [12] [13]
- Synchronous Access Description: [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24]
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [25]
- GPMC Timing Parameters: [26] [27] [28] [29] [30] [31] [32] [33]
- GPMC Register Summary: [34]

Table 15-418. GPMC_CONFIG5_i

Address Offset	0x0000 0070 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0070 + (0x0000 0030 * i)	**Instance**	GPMC
Description	RdAccessTime and CycleTime timing parameters configuration		
Type	RW		

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
RESERVED	PAGEBURSTACCESSTIME	RESERVED	RDACCESSTIME	RESERVED	WRCYCLETIME	RESERVED	RDCYCLETIME

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
27:24	PAGEBURSTACCESSTIME	Delay between successive words in a multiple access 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x1
23:21	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
20:16	RDACCESSTIME	Delay between start cycle time and first data valid 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x0F
15:13	RESERVED	Write 0s for future compatibility. Reads returns 0	RW	0x0

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Bits	Field Name	Description	Type	Reset
12:8	WRCYCLETIME	Total write cycle time 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x11
7:5	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
4:0	RDCYCLETIME	Total read cycle time 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x11

Table 15-419. Register Call Summary for Register GPMC_CONFIG5_i

General-Purpose Memory Controller

- Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME): [0] [1]
- Access Time (RDACCESSTIME / WRACCESSTIME): [2] [3] [4]
- Page Burst Access Time (PAGEBURSTACCESSTIME): [5]
- Asynchronous Access Description: [6] [7] [8]
- Synchronous Access Description: [9] [10] [11] [12] [13] [14] [15] [16] [17]
- Asynchronous and Synchronous Accesses in Nonmultiplexed Mode: [18] [19] [20] [21]
- GPMC Timing Parameters: [22] [23] [24] [25]
- GPMC Register Summary: [26]

Table 15-420. GPMC_CONFIG6_i

Address Offset	0x0000 0074 + (0x0000 0030 * i)	**Index**	i = 0 to7
Physical Address	0x5000 0074 + (0x0000 0030 * i)	**Instance**	GPMC
Description	WrAccessTime, WrDataOnADmuxBus, Cycle2Cycle and BusTurnAround parameters configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			RESERVED					WRACCESSTIME					RESERVED			WRDATAONADMUXBUS				RESERVED				CYCLE2CYCLEDELAY								CYCLE2CYCLESAMECSEN	CYCLE2CYCLEDIFFCSEN	RESERVED				BUSTURNAROUND			

Bits	Field Name	Description	Type	Reset
31	RESERVED	TI Internal use - Do not modify.	RW	1
30:29	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
28:24	WRACCESSTIME	Delay from start access time to the GPMC_FCLK rising edge corresponding the GPMC_CLK rising edge used by the attached memory for the first data capture 0x00: 0 GPMC_FCLK cycle 0x01: 1 GPMC_FCLK cycle ... 0x1F: 31 GPMC_FCLK cycles	RW	0x0F
23:20	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
19:16	WRDATAONADMUXBUS	Specifies on which GPMC_FCLK rising edge the first data of the synchronous burst write is driven in the add/data mux bus	RW	0x7
15:12	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0

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Bits	Field Name	Description	Type	Reset
11:8	CYCLE2CYCLEDELAY	Chip-select high pulse delay between successive accesses 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x0
7	CYCLE2CYCLESAMECSEN	Add CYCLE2CYCLEDELAY between successive accesses to the same chip-select (any access type) 0x0: No delay between the two accesses 0x1: Add CYCLE2CYCLEDELAY	RW	0
6	CYCLE2CYCLEDIFFCSEN	Add CYCLE2CYCLEDELAY between successive accesses to a different chip-select (any access type) 0x0: No delay between the two accesses 0x1: Add CYCLE2CYCLEDELAY	RW	0x0
5:4	RESERVED	Write 0s for future compatibility. Reads return 0.	RW	0x0
3:0	BUSTURNAROUND	Bus turnaround latency between successive accesses to the same chip-select (read to write) or to a different chip-select (read to read and read to write) 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0xF: 15 GPMC_FCLK cycles	RW	0x0

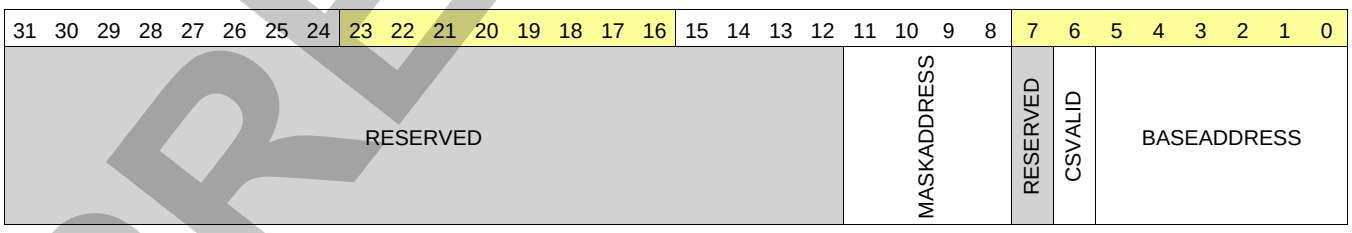
Table 15-421. Register Call Summary for Register GPMC_CONFIG6_i

General-Purpose Memory Controller

- External Signals: [0] [1] [2] [3] [4] [5]
- Read Cycle Time and Write Cycle Time (RDCYCLETIME / WRCYCLETIME): [6] [7]
- Access Time (RDACCESSTIME / WRACCESSTIME): [8] [9]
- Asynchronous Access Description: [10] [11] [12] [13]
- Synchronous Access Description: [14] [15] [16] [17]
- GPMC Timing Parameters: [18] [19] [20] [21] [22] [23]
- GPMC Register Summary: [24]

Table 15-422. GPMC_CONFIG7_i

Address Offset	0x0000 0078 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0078 + (0x0000 0030 * i)	**Instance**	GPMC
Description	CS address mapping configuration		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00000
11:8	MASKADDRESS	CS mask address. 0x1000: Chip-select size of 128 MiB 0x1100: Chip-select size of 64 MiB 0x1110: Chip-select size of 32 MiB 0x1111: Chip-select size of 16 MiB Other values must be avoided as they create holes in the chip-select address space.	RW	0xF

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Bits	Field Name	Description	Type	Reset
7	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
6	CSVALID	CS enable 0x0: CS disabled 0x1: CS enabled	RW	See (1)
5:0	BASEADDRESS	CSi base address where i = 0 to 7 (16-MiB minimum granularity) bits [5:0] corresponds to A29, A28, A27, A26, A25, and A24. See Figure 15-56	RW	0x00

(1) Reset value is 0x1 for CS0 and 0x0 for CS1 to CS7

Table 15-423. Register Call Summary for Register GPMC_CONFIG7_i

General-Purpose Memory Controller
- Chip-Select Base Address and Region Size: [0] [1] [2]
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [3]
- GPMC Configuration in NOR Mode: [4] [5] [6]
- GPMC Configuration in NAND Mode: [7] [8] [9]
- GPMC Timing Parameters: [10]
- GPMC Register Summary: [11]

Table 15-424. GPMC_NAND_COMMAND_i

Address Offset	0x0000 007C + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 007C + (0x0000 0030 * i)	**Instance**	GPMC
Description	This register is not a true register, only an address location.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_COMMAND																															

Bits	Field Name	Description	Type	Reset
31:0	GPMC_NAND_COMMAND	This register is not a true register, only an address location. Writing data at the GPMC_NAND_COMMAND_i location places the data as the NAND command value on the bus, using a regular asynchronous write access.	W	0x-

Table 15-425. Register Call Summary for Register GPMC_NAND_COMMAND_i

General-Purpose Memory Controller
- NAND Memory Device in Byte or 16-bit Word Stream Mode: [0] [1] [2] [3] [4] [5]
- Prefetch and Write-Posting Engine: [6]
- GPMC Register Summary: [7]
- GPMC Register Descriptions: [8]

Table 15-426. GPMC_NAND_ADDRESS_i

Address Offset	0x0000 0080 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0080 + (0x0000 0030 * i)	**Instance**	GPMC
Description	This register is not a true register, only an address location.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_ADDRESS																															

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Bits	Field Name	Description	Type	Reset
31:0	GPMC_NAND_ADDRESS	This register is not a true register, only an address location. Writing data at the GPMC_NAND_ADDRESS_i location places the data as the NAND partial address value on the bus, using a regular asynchronous write access.	W	0x-

Table 15-427. Register Call Summary for Register GPMC_NAND_ADDRESS_i

General-Purpose Memory Controller

- NAND Memory Device in Byte or 16-bit Word Stream Mode: [0] [1] [2] [3] [4] [5]
- Prefetch and Write-Posting Engine: [6]
- GPMC Register Summary: [7]
- GPMC Register Descriptions: [8]

Table 15-428. GPMC_NAND_DATA_i

Address Offset	0x0000 0084 + (0x0000 0030 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0084 + (0x0000 0030 * i)	**Instance**	GPMC
Description	This register is not a true register,only an address location.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_DATA																															

Bits	Field Name	Description	Type	Reset
31:0	GPMC_NAND_DATA	This register is not a true register, only an address location. Reading data from the GPMC_NAND_DATA_i location or from any location in the associated chip-select memory region activates an asynchronous read access.	W	0x-

Table 15-429. Register Call Summary for Register GPMC_NAND_DATA_i

General-Purpose Memory Controller

- NAND Memory Device in Byte or 16-bit Word Stream Mode: [0] [1] [2] [3]
- Prefetch and Write-Posting Engine: [4] [5]
- GPMC Register Summary: [6]
- GPMC Register Descriptions: [7] [8] [9]

Table 15-430. GPMC_PREFETCH_CONFIG1

Address Offset	0x0000 01E0		
Physical Address	0x5000 01E0	**Instance**	GPMC
Description	Prefetch engine configuration 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	CYCLEOPTIMIZATION			ENABLEOPTIMIZEDACCESS	ENGINECSSELECTOR			PFPWENROUNDROBIN	RESERVED			PFPWWEIGHTEDPRIO				RESERVED	FIFOTHRESHOLD							ENABLEENGINE	RESERVED	WAITPINSELECTOR		SYNCHROMODE	DMAMODE	RESERVED	ACCESSMODE

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Bits	Field Name	Description	Type	Reset
31	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
30:28	CYCLEOPTIMIZATION	Define the number of GPMC_FCLK cycles to be subtracted from RDCYCLETIME, WRCYCLETIME, ACCESSTIME, CSRDOFFTIME, CSWROFFTIME, ADVRDOFFTIME, ADVWROFFTIME, OEOFFTIME, WEOFFTIME 0x0: 0 GPMC_FCLK cycle 0x1: 1 GPMC_FCLK cycle ... 0x7: 7 GPMC_FCLK cycles	RW	0x0
27	ENABLEOPTIMIZEDACCESS	Enables access cycle optimization 0x0: Access cycle optimization is disabled. 0x1: Access cycle optimization is enabled.	RW	0x0
26:24	ENGINECSSELECTOR	Selects the chip-select where Prefetch Postwrite engine is active 0x0: CS0 0x1: CS1 0x2: CS2 0x3: CS3 0x4: CS4 0x5: CS5 0x6: CS6 0x7: CS7	RW	0x0
23	PFPWENROUNDROBIN	Enables the PFPW RoundRobin arbitration 0x0: Prefetch Postwrite engine round robin arbitration is disabled. 0x1: Prefetch Postwrite engine round robin arbitration is enabled.	RW	0x0
22:20	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
19:16	PFPWWEIGHTEDPRIO	When an arbitration occurs between a DMA and a PFPW engine access, the DMA is always serviced. If the PFPWEnRoundRobin is enabled, 0x0: The next access is granted to the PFPW engine. 0x1: The next two accesses are granted to the PFPW engine. ..., 0xF: The next 16 accesses are granted to the PFPW engine.	RW	0x0
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
14:8	FIFOTHRESHOLD	Selects the maximum number of bytes read from the FIFO or written to the FIFO by the host on a DMA or interrupt request 0x00: 0 byte 0x01: 1 byte ... 0x40: 64 bytes	RW	0x40
7	ENABLEENGINE	Enables the Prefetch Postwite engine 0x0: Prefetch Postwrite engine is disabled. 0x1: Prefetch Postwrite engine is enabled.	RW	0x0
6	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
5:4	WAITPINSELECTOR	Select which wait pin edge detector should start the engine in synchronized mode 0x0: Selects Wait0 EdgeDetection 0x1: Selects Wait1 EdgeDetection 0x2: Selects Wait2 EdgeDetection 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
3	SYNCHROMODE	Selects when the engine starts the access to chip-select 0x0: Engine starts the access to chip-select as soon as STARTENGINE is set 0x1: Engine starts the access to chip-select as soon as STARTENGINE is set AND wait to nonwait edge detection on the selected wait pin	RW	0x0
2	DMAMODE	Selects interrupt synchronization or DMA request synchronization 0x0: Interrupt synchronization is enabled. Only interrupt line is activated on FIFO threshold crossing. 0x1: DMA request synchronization is enabled. A DMA request protocol is used.	RW	0x0
1	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
0	ACCESSMODE	Selects prefetch read or write-posting accesses 0x0: Prefetch read mode 0x1: Write-posting mode	RW	0x0

Table 15-431. Register Call Summary for Register GPMC_PREFETCH_CONFIG1

General-Purpose Memory Controller

- GPMC Interrupt Requests: [0]
- Prefetch and Write-Posting Engine: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32]
- GPMC Configuration in NAND Mode: [33] [34] [35] [36] [37] [38] [39] [40] [41] [42]
- GPMC Register Summary: [43]

Table 15-432. GPMC_PREFETCH_CONFIG2

Address Offset	0x0000 01E4		
Physical Address	0x5000 01E4	**Instance**	GPMC
Description	Prefetch engine configuration 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TRANSFERCOUNT															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00000
13:0	TRANSFERCOUNT	Selects the number of bytes to be read or written by the engine to the selected chip-select 0x0000: 0 byte 0x0001: 1 byte ... 0x2000: 8 Kbytes	RW	0x0000

Table 15-433. Register Call Summary for Register GPMC_PREFETCH_CONFIG2

General-Purpose Memory Controller

- Prefetch and Write-Posting Engine: [0] [1] [2] [3]
- GPMC Configuration in NAND Mode: [4]
- GPMC Register Summary: [5]

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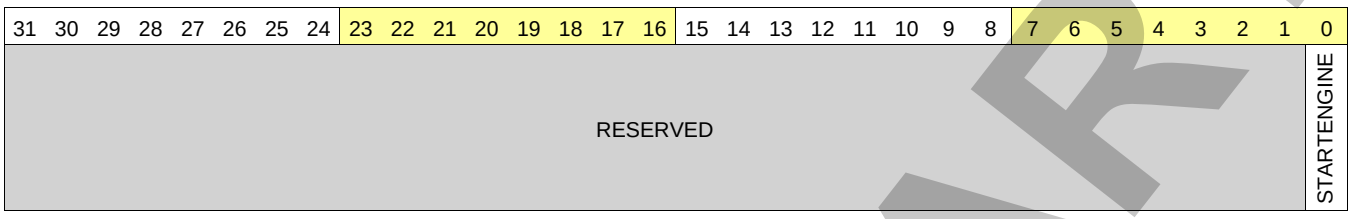
Table 15-434. GPMC_PREFETCH_CONTROL

Address Offset	0x0000 01EC		
Physical Address	0x5000 01EC	**Instance**	GPMC
Description	Prefetch engine control		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00000000
0	STARTENGINE	Resets the FIFO pointer and starts the engine Read 0x0: Engine is stopped. Write 0x0: Stops the engine Read 0x1: Engine is running. Write 0x1: Resets the FIFO pointer to 0x0 in prefetch mode and 0x40 in postwrite mode and starts the engine	RW	0x0

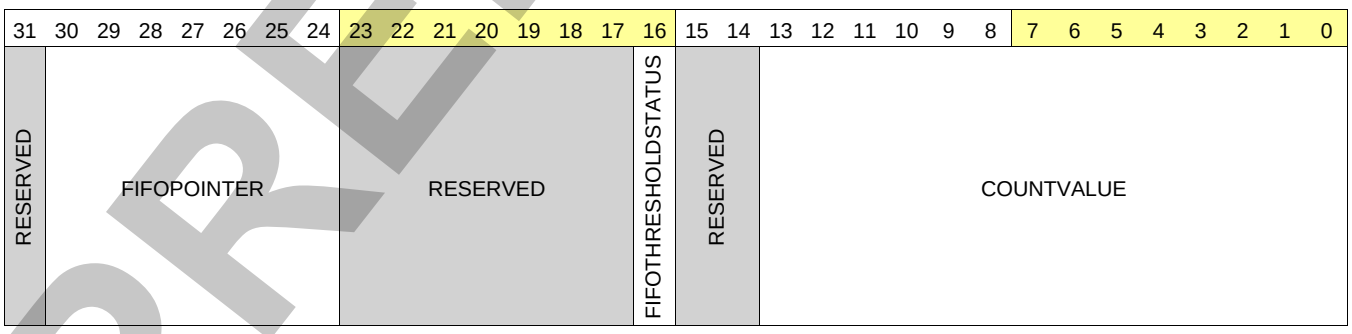
Table 15-435. Register Call Summary for Register GPMC_PREFETCH_CONTROL

General-Purpose Memory Controller

- Prefetch and Write-Posting Engine: [0] [1] [2] [3] [4] [5] [6]
- GPMC Configuration in NAND Mode: [7] [8]
- GPMC Register Summary: [9]

Table 15-436. GPMC_PREFETCH_STATUS

Address Offset	0x0000 01F0		
Physical Address	0x5000 01F0	**Instance**	GPMC
Description	Prefetch engine status		
Type	RW		



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Bits	Field Name	Description	Type	Reset
31	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0x0
30:24	FIFOPOINTER	Number of available bytes to be read or number of free empty byte places to be written 0x00: 0 byte available to be read or 0 free empty place to be written ... 0x40: 64 bytes available to be read or 64 empty places to be written	R	0x00
23:17	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x00
16	FIFOTHRESHOLDSTATUS	Set when FIFOPointer exceeds FIFOThreshold value 0x0: FIFOPointer smaller or equal to FIFOThreshold. Writing to this bit has no effect. 0x1: FIFOPointer greater than FIFOThreshold. Writing to this bit has no effect.	R	0x0
15:14	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
13:0	COUNTVALUE	Number of remaining bytes to be read or to be written by the engine according to the TransferCount value 0x0000: 0 byte remaining to be read or to be written 0x0001: 1 byte remaining to be read or to be written ... 0x2000: 8 KiB remaining to be read or to be written	R	0x0000

Table 15-437. Register Call Summary for Register GPMC_PREFETCH_STATUS

General-Purpose Memory Controller

- Prefetch and Write-Posting Engine: [0] [1] [2] [3] [4] [5] [6]
- GPMC Register Summary: [7]
- GPMC Register Descriptions: [8] [9]

Table 15-438. GPMC_ECC_CONFIG

Address Offset	0x0000 01F4		
Physical Address	0x5000 01F4	**Instance**	GPMC
Description	ECC configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ECCALGORITHM	RESERVED		ECCBCHTSEL		ECCWRAPMODE				ECC16B	ECCTOPSECTOR			ECCCS			ECCENABLE

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0000
16	ECCALGORITHM	ECC algorithm used 0x0: Hamming code 0x1: BCH code	RW	0x0
15:14	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
13:12	ECCBCHTSEL	Error correction capability used for BCH 0x0: Up to 4 bits error correction (t = 4) 0x1: Up to 8 bits error correction (t = 8) 0x2: Up to 16 bits error correction (t = 16) 0x3: Reserved	RW	0x1

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Bits	Field Name	Description	Type	Reset
11:8	ECCWRAPMODE	Spare area organization definition for the BCH algorithm. See the BCH syndrome/parity calculator module functional specification for more details	RW	0x0
7	ECC16B	Selects an ECC calculated on 16 columns 0x0: ECC calculated on 8 columns 0x1: ECC calculated on 16 columns	RW	0x0
6:4	ECCTOPSECTOR	Number of sectors to process with the BCH algorithm 0x0: 1 sector (512-kB page) 0x1: 2 sectors ... 0x3: 4 sectors (2-kB page) ... 0x7: 8 sectors (4-kB page)	RW	0x3
3:1	ECCCS	Selects the CS where ECC is computed 0x0: CS0 0x1: CS1 0x2: CS2 0x3: CS3 Other: Reserved	RW	0x0
0	ECCENABLE	Enables the ECC feature 0x0: ECC disabled 0x1: ECC enabled	RW	0x0

Table 15-439. Register Call Summary for Register GPMC_ECC_CONFIG

General-Purpose Memory Controller

- ECC Calculator: [0] [1] [2] [3] [4] [5] [6] [7]
- GPMC Configuration in NAND Mode: [8] [9] [10] [11] [12] [13]
- GPMC Register Summary: [14]
- GPMC Register Descriptions: [15] [16] [17]

Table 15-440. GPMC_ECC_CONTROL

Address Offset	0x0000 01F8		
Physical Address	0x5000 01F8	**Instance**	GPMC
Description	ECC control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							ECCCLEAR	RESERVED				ECCPOINTER			

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x000000
8	ECCCLEAR	Clear all ECC result registers Reads return 0. Write 0x1 to this field clears all ECC result registers. Write 0x0 is ignored.	RW	0x0
7:4	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0

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Bits	Field Name	Description	Type	Reset
3:0	ECCPOINTER	Selects ECC result register (Reads to this field give the dynamic position of the ECC pointer - Writes to this field select the ECC result register where the first ECC computation will be stored.); Other enums: writing other values disables the ECC engine (ECCENABLE bit of GPMC_ECC_CONFIG set to 0) 0x0: Writing 0x0 disables the ECC engine (ECCENABLE bit of GPMC_ECC_CONFIG set to 0) 0x1: ECC result register 1 selected 0x2: ECC result register 2 selected 0x3: ECC result register 3 selected 0x4: ECC result register 4 selected 0x5: ECC result register 5 selected 0x6: ECC result register 6 selected 0x7: ECC result register 7 selected 0x8: ECC result register 8 selected 0x9: ECC result register 9 selected	RW	0x0

Table 15-441. Register Call Summary for Register GPMC_ECC_CONTROL

General-Purpose Memory Controller

- ECC Calculator: [0] [1] [2] [3]
- GPMC Configuration in NAND Mode: [4] [5]
- GPMC Register Summary: [6]

Table 15-442. GPMC_ECC_SIZE_CONFIG

Address Offset	0x0000 01FC		
Physical Address	0x5000 01FC	**Instance**	GPMC
Description	ECC size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ECCSIZE1								RESERVED				ECCSIZE0				RESERVED				ECC9RESULTSIZE	ECC8RESULTSIZE	ECC7RESULTSIZE	ECC6RESULTSIZE	ECC5RESULTSIZE	ECC4RESULTSIZE	ECC3RESULTSIZE	ECC2RESULTSIZE	ECC1RESULTSIZE

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Write 0s for future compatibility. Read returns 3.	RW	0x3
29:22	ECCSIZE1	Defines Hamming code ECC size 1 in bytes 0x00: 2 bytes 0x01: 4 bytes 0x02: 6 bytes 0x03: 8 bytes ... 0xFF: 512 bytes For BCH code ECC, the size 1 is programmed directly with the number of nibbles. For details, see Section 15.4.4.13.3.2.2.3, *Wrapping Modes*.	RW	0xFF
21:20	RESERVED	Write 0s for future compatibility. Read returns 3.	RW	0x3

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Bits	Field Name	Description	Type	Reset
19:12	ECCSIZE0	Defines Hamming code ECC size 0 in bytes 0x00: 2 bytes 0x01: 4 bytes 0x02: 6 bytes 0x03: 8 bytes ... 0xFF: 512 bytes For BCH code ECC, the size 0 is programmed directly with the number of nibbles. For details, see Section 15.4.4.13.3.2.2.3, *Wrapping Modes*.	RW	0xFF
11:9	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
8	ECC9RESULTSIZE	Selects ECC size for ECC 9 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
7	ECC8RESULTSIZE	Selects ECC size for ECC 8 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
6	ECC7RESULTSIZE	Selects ECC size for ECC 7 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
5	ECC6RESULTSIZE	Selects ECC size for ECC 6 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
4	ECC5RESULTSIZE	Selects ECC size for ECC 5 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
3	ECC4RESULTSIZE	Selects ECC size for ECC 4 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
2	ECC3RESULTSIZE	Selects ECC size for ECC 3 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
1	ECC2RESULTSIZE	Selects ECC size for ECC 2 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0
0	ECC1RESULTSIZE	Selects ECC size for ECC 1 result register 0x0: ECCSIZE0 selected 0x1: ECCSIZE1 selected	RW	0x0

Table 15-443. Register Call Summary for Register GPMC_ECC_SIZE_CONFIG

General-Purpose Memory Controller

- ECC Calculator: [0] [1] [2] [3] [4] [5] [6]
- GPMC Configuration in NAND Mode: [7] [8]
- GPMC Register Summary: [9]

Table 15-444. GPMC_ECCj_RESULT

Address Offset	0x0000 0200 + (0x0000 0004 * (j - 1))	**Index**	j = 1 to 9
Physical Address	0x5000 0200 + (0x0000 0004 * j)	**Instance**	GPMC
Description	ECC result register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				P2048O	P1024O	P512O	P256O	P128O	P64O	P32O	P16O	P8O	P4O	P2O	P1O	RESERVED				P2048E	P1024E	P512E	P256E	P128E	P64E	P32E	P16E	P8E	P4E	P2E	P1E

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
27	P2048O	Odd row parity bit 2048, only used for ECC computed on 512 bytes	R	0x0
26	P1024O	Odd row parity bit 1024	R	0x0
25	P512O	Odd row parity bit 512	R	0x0
24	P256O	Odd row parity bit 256	R	0x0
23	P128O	Odd row parity bit 128	R	0x0
22	P64O	Odd row parity bit 64	R	0x0
21	P32O	Odd row parity bit 32	R	0x0
20	P16O	Odd row parity bit 16	R	0x0
19	P8O	Odd row parity bit 8	R	0x0
18	P4O	Odd Column Parity bit 4	R	0x0
17	P2O	Odd Column Parity bit 2	R	0x0
16	P1O	Odd Column Parity bit 1	R	0x0
15:12	RESERVED	Write 0s for future compatibility. Read returns 0s.	RW	0x0
11	P2048E	Even row parity bit 2048, only used for ECC computed on 512 bytes	R	0x0
10	P1024E	Even row parity bit 1024	R	0x0
9	P512E	Even row parity bit 512	R	0x0
8	P256E	Even row parity bit 256	R	0x0
7	P128E	Even row parity bit 128	R	0x0
6	P64E	Even row parity bit 64	R	0x0
5	P32E	Even row parity bit 32	R	0x0
4	P16E	Even row parity bit 16	R	0x0
3	P8E	Even row parity bit 8	R	0x0
2	P4E	Even column parity bit 4	R	0x0
1	P2E	Even column parity bit 2	R	0x0
0	P1E	Even column parity bit 1	R	0x0

Table 15-445. Register Call Summary for Register GPMC_ECCj_RESULT

General-Purpose Memory Controller

- ECC Calculator: [0] [1] [2] [3] [4] [5] [6] [7]
- GPMC Register Summary: [8]

Table 15-446. GPMC_BCH_RESULT0_i

Address Offset	0x0000 0240 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0240 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 0 to 31)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_0																															

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Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_0	BCH ECC result (bits 0 to 31)	RW	0x00000000

Table 15-447. Register Call Summary for Register GPMC_BCH_RESULT0_i

General-Purpose Memory Controller
- ECC Calculator: [0]
- GPMC Register Summary: [1]

Table 15-448. GPMC_BCH_RESULT1_i

Address Offset	0x0000 0244 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0244 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 32 to 63)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_1																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_1	BCH ECC result (bits 32 to 63)	RW	0x00000000

Table 15-449. Register Call Summary for Register GPMC_BCH_RESULT1_i

General-Purpose Memory Controller
- ECC Calculator: [0]
- GPMC Register Summary: [1]

Table 15-450. GPMC_BCH_RESULT2_i

Address Offset	0x0000 0248 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0248 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 64 to 95)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_2																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_2	BCH ECC result (bits 64 to 95)	RW	0x00000000

Table 15-451. Register Call Summary for Register GPMC_BCH_RESULT2_i

General-Purpose Memory Controller
- ECC Calculator: [0]
- GPMC Register Summary: [1]

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Table 15-452. GPMC_BCH_RESULT3_i

Address Offset	0x0000 024C + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 024C + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 96 to 127)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_3																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_3	BCH ECC result (bits 96 to 127)	RW	0x00000000

Table 15-453. Register Call Summary for Register GPMC_BCH_RESULT3_i

General-Purpose Memory Controller

- ECC Calculator: [0]
- GPMC Register Summary: [1]

Table 15-454. GPMC_BCH_RESULT4_i

Address Offset	0x0000 0300 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0300 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 128 to 159)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_4																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_4	BCH ECC result (bits 128 to 159)	RW	0x00000000

Table 15-455. Register Call Summary for Register GPMC_BCH_RESULT4_i

General-Purpose Memory Controller

- GPMC Register Summary: [0]

Table 15-456. GPMC_BCH_RESULT5_i

Address Offset	0x0000 0304 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0304 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 160 to 191)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_5																															

Bits	Field Name	Description	Type	Reset
31:0	BCH_RESULT_5	BCH ECC result (bits 160 to 191)	RW	0x00000000

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Table 15-457. Register Call Summary for Register GPMC_BCH_RESULT5_i

General-Purpose Memory Controller

- GPMC Register Summary: [0]

Table 15-458. GPMC_BCH_RESULT6_i

Address Offset	0x0000 0308 + (0x0000 0010 * i)	**Index**	i = 0 to 7
Physical Address	0x5000 0308 + (0x0000 0010 * i)	**Instance**	GPMC
Description	BCH ECC result (bits 192 to 207)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BCH_RESULT_6															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Read returns 0s.	R	0x0000
15:0	BCH_RESULT_6	BCH ECC result (bits 192 to 207)	RW	0x0000

Table 15-459. Register Call Summary for Register GPMC_BCH_RESULT6_i

General-Purpose Memory Controller

- GPMC Register Summary: [0]

Table 15-460. GPMC_BCH_SWDATA

Address Offset	0x0000 02D0		
Physical Address	0x5000 02D0	**Instance**	GPMC
Description	This register is used to directly pass data to the BCH ECC calculator without accessing the actual NAND flash interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BCH_DATA															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0s for future compatibility. Read returns 0s.	R	0x0000
15:0	BCH_DATA	Data to be included in the BCH calculation Only bits 0 to 7 are considered if the calculator is configured to use 8-bit data (GPMC_ECC_CONFIG[7] ECC16B = 0)	RW	0x0000

Table 15-461. Register Call Summary for Register GPMC_BCH_SWDATA

General-Purpose Memory Controller

- GPMC Register Summary: [0]

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15.5 Error Location Module

15.5.1 Error Location Module Overview

Nonmanaged NAND flash memories can be dense and nonvolatile in their own nature, but error-prone. When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller.

The general-purpose memory controller (GPMC) probes data read from an external NAND flash and uses this to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare-area data field, with a maximum block size of 1023 bytes. Computation is based on a Bose-Chaudhuri-Hocquenghem (BCH) algorithm. The error-location module (ELM) extracts error addresses from these syndrome polynomials.

Based on the syndrome polynomial value, the ELM can detect errors, compute the number of errors, and give the location of each error bit. The actual data is not required to complete the error-correction algorithm. Errors can be reported anywhere in the NAND flash block, including in the parity bits.

The maximum acceptable number of errors that can be corrected depends on a programmable configuration parameter. 4-, 8-, and 16-bit error-correction levels are supported. The ELM relies on a static and fixed definition of the generator polynomial for each error-correction level that corresponds to the generator polynomials defined in the GPMC (there are three fixed polynomial for the three correction error levels). A larger number of errors than the programmed error-correction level may be detected, but the ELM cannot correct them all. The offending block is then tagged as *uncorrectable* in the associated computation exit status register. If the computation is successful, that is, if the number of errors detected does not exceed the maximum value authorized for the chosen correction capability, the exit status register contains the information on the number of detected errors.

When the error-location process completes, an interrupt is triggered to inform the software that its status can be checked. The number of detected errors and their locations in the NAND block can be retrieved from the module through register accesses.

15.5.1.1 ELM Features

The ELM has the following features:

- 4, 8, and 16 bits per 512-byte block error-location based on BCH algorithms
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation on error-location process completion:
  - When the full page has been processed in page mode
  - For each syndrome polynomial in continuous mode

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15.5.2 ELM Integration

The ELM extracts error addresses from generated syndrome polynomials.

The ELM is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. The microprocessor unit (MPU) can then correct the data block by flipping the bits to which the ELM error-location outputs point.

Figure 15-101 shows the integration of the ELM subsystem in the device.

Figure 15-101. ELM Integration

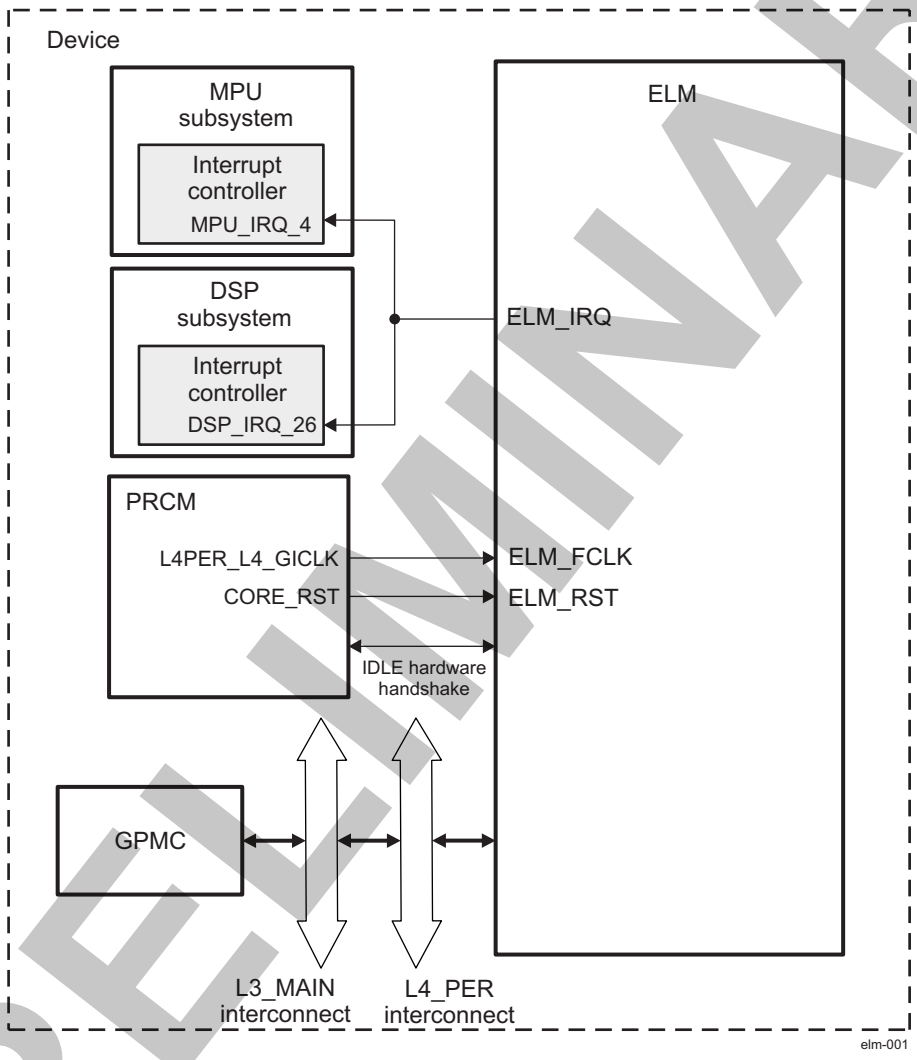

Table 15-462 through Table 15-464 summarize the integration of the module in the device.

Table 15-462. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
ELM	PD_L4_PER	No	L4_PER

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Table 15-463. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
ELM	ELM_FCLK	L4PER_L4_GICLK	PRCM	Functional clock For information about PRCM clock gating and management, see Section 3.6.8, *CD_L4_PER Clock Domain*, in Section 3.1.1, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
ELM	ELM_RST	L4_PER_RST	PRCM	Module hardware reset For information about PRCM reset sources and distribution, see Section 3.5.4, *Reset Domains*, inSection 3.1.1, *Power, Reset, and Clock Management*.

Table 15-464. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
ELM	ELM_IRQ	MPU_IRQ_4	MPU	BCH error-location module interrupt For information about MPU interrupt control, see Section 17.3.2, *Interrupt Requests to INTC_MPU*.
		DSP_IRQ_26	DSP	BCH error-location module interrupt For information about DSP interrupt control, see Section 5.3.2.6, *DSP INTC*.

15.5.3 ELM Functional Description

The ELM is designed around the error-location engine, which handles the computation based on the input syndrome polynomials.

The ELM maps the error-location engine to a standard interconnect interface by using a set of registers to control inputs and outputs.

15.5.3.1 ELM Software Reset

To perform a software reset, set the ELM_SYSCONFIG[1] SOFTRESET bit to 1. The ELM_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. When the software reset completes, the ELM_SYSCONFIG[1] SOFTRESET bit is automatically reset.

15.5.3.2 ELM Power Management

Table 15-465 describes the power-management features available to the ELM.

NOTE:

- For information about source clock gating and a description of the sleep/wake-up transitions, see the Section 3.6.8, *CD_L4_PER Clock Domain*, in Section 3.1.1, *Power, Reset, and Clock Management*.
- For a general description of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.6, *Clock Management Functional Description*, in Section 3.1.1, *Power, Reset, and Clock Management*

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Table 15-465. Local Power-Management Features

Feature	Registers	Description
Clock autogating	ELM_SYSCONFIG[0] AUTOGATING	This bit allows a local power optimization inside the module by gating the ELM_FCLK clock upon the interface activity.
Slave idle modes	ELM_SYSCONFIG[4:3] SIDLEMODE	Force-idle, no-idle, and smart-idle modes are available.
Clock activity	ELM_SYSCONFIG[8] CLOCKACTIVITY	The clock can be switched off or maintained during the wake-up period.
Master standby modes	N/A	
Global wake-up enable	N/A	
Wake-up sources enable	N/A	

CAUTION

The PRCM module has no hardware means of reading CLOCKACTIVITY settings. Thus, software must ensure consistent programming between the ELM CLOCKACTIVITY and ELM clock PRCM control bits. For a description of the ClockActivity feature, see Section 3.1.1, *Power, Reset, and Clock Management*.

15.5.3.3 ELM Interrupt Requests

Table 15-466 lists the event flags, and their masks, that can cause module interrupts.

Table 15-466. Events

Event Flag	Event Mask	Description
ELM_IRQSTATUS[8] PAGE_VALID	ELM_IRQENABLE[8] PAGE_MASK	Page interrupt
ELM_IRQSTATUS[7] LOC_VALID_7	ELM_IRQENABLE[7] LOCATION_MASK_7	Error-location interrupt for syndrome polynomial 7
ELM_IRQSTATUS[6] LOC_VALID_6	ELM_IRQENABLE[6] LOCATION_MASK_6	Error-location interrupt for syndrome polynomial 6
ELM_IRQSTATUS[5] LOC_VALID_5	ELM_IRQENABLE[5] LOCATION_MASK_5	Error-location interrupt for syndrome polynomial 5
ELM_IRQSTATUS[4] LOC_VALID_4	ELM_IRQENABLE[4] LOCATION_MASK_4	Error-location interrupt for syndrome polynomial 4
ELM_IRQSTATUS[3] LOC_VALID_3	ELM_IRQENABLE[3] LOCATION_MASK_3	Error-location interrupt for syndrome polynomial 3
ELM_IRQSTATUS[2] LOC_VALID_2	ELM_IRQENABLE[2] LOCATION_MASK_2	Error-location interrupt for syndrome polynomial 2
ELM_IRQSTATUS[1] LOC_VALID_1	ELM_IRQENABLE[1] LOCATION_MASK_1	Error-location interrupt for syndrome polynomial 1
ELM_IRQSTATUS[0] LOC_VALID_0	ELM_IRQENABLE[0] LOCATION_MASK_0	Error-location interrupt for syndrome polynomial 0

15.5.3.4 Processing Initialization

ELM_LOCATION_CONFIG global setting parameters must be set before using the error-location engine. The ELM_LOCATION_CONFIG[1:0] ECC_BCH_LEVEL bit field defines the error-correction level used (4-,8-, or 16-bit error correction). The ELM_LOCATION_CONFIG[26:16] ECC_SIZE bit field defines the maximum buffer length beyond which the engine processing no longer looks for errors.

Software can choose to use the ELM in continuous mode or page mode. If all ELM_PAGE_CTRL[i] SECTOR_i bits (i is the syndrome polynomial number, where i = 0 to 7) are reset, continuous mode is used. In any other case, page mode is implicitly selected.

- Continuous mode: Each syndrome polynomial is processed independently. Results for a syndrome can be retrieved and acknowledged at any time, regardless of the status of the other seven processing

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contexts.

- Page mode: Syndrome polynomials are grouped into atomic entities: only one page can be processed at any given time, even if all eight contexts are not used for this page. Unused contexts are lost and cannot be affected to any other processing. The full page must be acknowledged and cleared before moving to the next page.

For completion interrupts to be generated correctly, all ELM_IRQENABLE[i] LOCATION_MASK_i bits (where i = 0 to 7) must be forced to 0 when in page mode, and set to 1 in continuous mode. Additionally, the ELM_IRQENABLE[8] PAGE_MASK bit must be set to 1 when in page mode.

Software initiates error-location processing by writing a syndrome polynomial into one of the eight possible register sets. Each of these register sets includes seven registers: ELM_SYNDROME_FRAGMENT_0_i to ELM_SYNDROME_FRAGMENT_6_i. The first six registers can be written in any order, but ELM_SYNDROME_FRAGMENT_6_i must be written last because it includes the validity bit, which instructs the ELM that this syndrome polynomial must be processed (the ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit).

As soon as one validity bit is asserted (ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID = 0x1, where i = 0 to 7), error-location processing can start for the corresponding syndrome polynomial. The associated ELM_LOCATION_STATUS_i and ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i registers (where i = 0 to 7) are not reset. Software must not consider them until the corresponding ELM_IRQSTATUS[i] LOC_VALID_i bit is set.

15.5.3.5 Processing Sequence

While the error-location engine is busy processing one syndrome polynomial, further syndrome polynomials can be written. They are processed when the current processing completes.

The engine completes early when:

- No error is detected; that is, when the ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE bit is set to 1 and the ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS bit field is set to 0x0.
- Too many errors are detected; that is, when the ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE bit is set to 0 while the ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS bit field is set with the value output by the error-location engine. The reported number of errors is not ensured if ECC_CORRECTABLE is 0.

If the engine completes early, the associated error-location registers ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i (where i = 0 to 7) are not updated.

In all other cases, the engine goes through the entire error-location process. Each time an error location is found, it is logged in the associated ECC_ERROR_LOCATION bit field. The first error detected is logged in the ELM_ERROR_LOCATION_0_i[12:0] ECC_ERROR_LOCATION bit field; the second is logged in the ELM_ERROR_LOCATION_1_i[12:0] ECC_ERROR_LOCATION bit field, and so on.

Table 15-467 describes the ELM_LOCATION_STATUS_i value decoding.

Table 15-467. ELM_LOCATION_STATUS_i Value Decoding

ECC_CORRECTABLE Value	ECC_NB_ERRORS Value	Status	Number of Errors Detected	Action Required
1	0	OK	0	None
1	≠ 0	OK	ECC_NB_ERRORS	Correct the data buffer read based on the ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i results.
0	Any	Failed	Unknown	Software-dependent

15.5.3.6 Processing Completion

When the processing for a given syndrome polynomial completes, its ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit is reset. It must not be set again until the exit status registers, ELM_LOCATION_STATUS_i (where i = 0 to 7) for this processing are checked. Failure to comply with this rule leads to potential loss of the first polynomial process data output.

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The error-location engine signals the process completion to the ELM. When this event is detected, the corresponding ELM_IRQSTATUS[i] LOC_VALID_i bit (where i = 0 to 7) is set. The processing exit status is available from the associated ELM_LOCATION_STATUS_i register, and error locations are stored in order in the ECC_ERROR_LOCATION bit fields. Software must read only valid error-location registers based on the number of errors detected and located.

Immediately after the error-location engine completes, a new syndrome polynomial can be processed, if any is available, as reported by the ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID bit, depending on the configured error-correction level. If several syndrome polynomials are available, a round-robin arbitration is used to select one for processing.

In continuous mode (that is, all bits in ELM_PAGE_CTRL are reset), an interrupt is triggered whenever a ELM_IRQSTATUS[i] LOC_VALID_i bit is asserted. Software must read the ELM_IRQSTATUS register to determine which polynomial is processed and retrieve the exit status and error locations (ELM_LOCATION_STATUS_i and ELM_ERROR_LOCATION_0_i to ELM_ERROR_LOCATION_15_i). When done, software must clear the corresponding ELM_IRQSTATUS[i] LOC_VALID_i bit by setting it to 1. Other status bits must be set to 0 so that other interrupts are not unintentionally cleared. When using this mode, the ELM_IRQSTATUS[8] PAGE_VALID interrupt is never triggered.

In page mode, the module does not trigger interrupts for the processing completion of each polynomial because the ELM_IRQENABLE[i] LOCATION_MASK_i bits are cleared. A page is defined using the ELM_PAGE_CTRL register. Each SECTOR_i bit set means the corresponding polynomial i is part of the page processing. A page is fully processed when all tagged polynomials have been processed, as logged in the ELM_IRQSTATUS[i] LOC_VALID_i bits. The module triggers an ELM_IRQSTATUS[8] PAGE_VALID interrupt whenever it detects that the full page has been processed. To make sure the next page can be correctly processed, all status bits in the ELM_IRQSTATUS register must be cleared by using a single atomic-write access.

NOTE: Do not modify page setting parameters in the ELM_PAGE_CTRL register unless the engine is idle, no polynomial input is valid, and all interrupts have been cleared.

Because no polynomial-level interrupt is triggered in page mode, polynomials cleared in the ELM_PAGE_CTRL[i] SECTOR_i bits (where i = 0 to 7) are processed as usual, but are essentially ignored. Software must manually poll the ELM_IRQSTATUS bits to check for their status.

15.5.4 ELM Basic Programming Model

15.5.4.1 ELM Low-Level Programming Model

15.5.4.1.1 Processing Initialization

Table 15-468. ELM Processing Initialization

Step	Register/Bit Field/Programming Model	Value
Resets the module	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTATUS[0] RESETDONE	0x1
Configure the slave interface power management.	ELM_SYSCONFIG[4:3] SIDLEMODE	Set value.
Defines the error-correction level used	ELM_LOCATION_CONFIG[1:0] ECC_BCH_LEVEL	Set value.
Defines the maximum buffer length	ELM_LOCATION_CONFIG[26:16] ECC_SIZE	Set value.
Sets the ELM in continuous mode or page mode	ELM_PAGE_CTRL	Set value.
If continuous mode is used	All ELM_PAGE_CTRL[i] SECTOR_i (where i = 0 to 7)	0x0
Enables interrupt for syndrome polynomial i	ELM_IRQENABLE[i] LOCATION_MASK_i	0x1
else (page mode is used)	One syndrome polynomial i is set ELM_PAGE_CTRL[i] SECTOR_i (where i = 0 to 7)	0x1
Disable all interrupts for syndrome polynomial and enable PAGE_MASK interrupt.	All ELM_IRQENABLE[i] LOCATION_MASK_i = 0x0 and ELM_IRQENABLE[8] PAGE_MASK = 0x1	Set value.
endif		Set value.

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Table 15-468. ELM Processing Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Set the input syndrome polynomial i.	ELM_SYNDROME_FRAGMENT_0_i	Set value.
	ELM_SYNDROME_FRAGMENT_1_i	Set value.
	ELM_SYNDROME_FRAGMENT_5_i	Set value.
	ELM_SYNDROME_FRAGMENT_6_i	Set value.
Initiates the computation process	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID	0x1

15.5.4.1.2 Read Results

The engine goes through the entire error-location process and results can be read. Table 15-469 and Table 15-470 describe the processing completion for continuous and page modes, respectively.

Table 15-469. ELM Processing Completion for Continuous Mode

Step	Register/Bit Field/Programming Model	Value
Wait until process is complete for syndrome polynomial i: Wait until the ELM_IRQ interrupt is generated, or poll the status register.		
Read for which i the error-location process is complete.	ELM_IRQSTATUS[i] LOC_VALID_i	0x1
if the process fails (too many errors)	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x0
It is software dependant.		
else (process successful, the engine completes)	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x1
Read the number of errors.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS	
Read the error-location bit addresses for syndrome polynomial i of the ECC_NB_ERRORS first registers. Software must correct errors in the data buffer.	ELM_ERROR_LOCATION_0_i[12:0] ECC_ERROR_LOCATION	
	ELM_ERROR_LOCATION_1_i[12:0] ECC_ERROR_LOCATION	
	...	
	ELM_ERROR_LOCATION_15_i[12:0] ECC_ERROR_LOCATION	
endif		
Clear the corresponding i interrupt.	ELM_IRQSTATUS[i] LOC_VALID_i	0x1

A new syndrome polynomial can be processed after the end of processing (ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID = 0x0) and after the exit status register check (ELM_LOCATION_STATUS_i).

Table 15-470. ELM Processing Completion for Page Mode

Step	Register/Bit Field/Programming Model	Value
Wait until process is complete for syndrome polynomial i: Wait until the ELM_IRQ interrupt is generated, or poll the status register.		
Wait for page completed interrupt: All error locations are valid.	ELM_IRQSTATUS[8] PAGE_VALID	0x1
Repeat the following actions the necessary number of times. That is, once for each valid defined block in the page.		
Read the process exit status.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	
if the process fails (too many errors)	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x0
It is software dependent.		
else (process successful, the engine completes)	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE	0x1
Read the number of errors.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS	

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Table 15-470. ELM Processing Completion for Page Mode (continued)

Step	Register/Bit Field/Programming Model	Value
Read the error-location bit addresses for syndrome polynomial i of the ECC_NB_ERRORS first registers.	ELM_ERROR_LOCATION_0_i[12:0] ECC_ERROR_LOCATION	
	ELM_ERROR_LOCATION_1_i[12:0] ECC_ERROR_LOCATION	
	...	
	ELM_ERROR_LOCATION_15_i[12:0] ECC_ERROR_LOCATION	
endif		
End Repeat		
Clear the ELM_IRQSTATUS register.	ELM_IRQSTATUS	0x1FF

Next page can be correctly processed after a page is fully processed, when all tagged polynomials have been processed (ELM_IRQSTATUS[i] LOC_VALID_i = 0x1 for all syndrome polynomials i used in the page).

15.5.4.2 Use Case: ELM Used in Continuous Mode

In this example, the ELM is programmed for an 8-bit error-correction capability in continuous mode (see Table 15-471). After reading a 528-byte NAND flash sector (512B data plus 16B spare area) with a 16-bit interface, a nonzero polynomial syndrome is reported from the GPMC (polynomial syndrome 0 is used in the ELM):

- P = 0x0A16ABE115E44F767BFB0D0980

Table 15-471. Use Case: Continuous Mode

Step	Register/Bit Field/Programming Model	Value
Resets the module	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTATUS[0] RESETDONE	0x1
Configure the slave interface power management: Smart idle is used.	ELM_SYSCONFIG[4:3] SIDLEMODE	0x2
Defines the error-correction level used: 8 bits	ELM_LOCATION_CONFIG[1:0] ECC_BCH_LEVEL	0x1
Defines the maximum buffer length: 528 bytes (2 × 528 = 1056)	ELM_LOCATION_CONFIG[26:16] ECC_SIZE	0x420
Sets the ELM in continuous mode	ELM_PAGE_CTRL	0
Enables interrupt for syndrome polynomial 0	ELM_IRQENABLE[0] LOCATION_MASK_0	0x1
Set the input syndrome polynomial 0.	ELM_SYNDROME_FRAGMENT_0_i (where i = 0)	0xFB0D0980
	ELM_SYNDROME_FRAGMENT_1_i (where i = 0)	0xE44F767B
	ELM_SYNDROME_FRAGMENT_2_i (where i = 0)	0x16ABE115
	ELM_SYNDROME_FRAGMENT_3_i (where i = 0)	0x0000000A
Initiates the computation process	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 0)	0x1
Wait until process is complete for syndrome polynomial 0: IRQ_ELM is generated or poll the status register.		
Read that error-location process is complete for syndrome polynomial 0.	ELM_IRQSTATUS[0] LOC_VALID_0	0x1
Read the process exit status: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 0)	0x1
Read the number of errors: Four errors detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (where i = 0)	0x4

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Table 15-471. Use Case: Continuous Mode (continued)

Step	Register/Bit Field/Programming Model	Value
Read the error-location bit addresses for syndrome polynomial 0 of the first four registers: Errors are located in the data buffer at decimal addresses 431, 1062, 1909, 3452.	ELM_ERROR_LOCATION_0_i (where i = 0)	0x1AF
	ELM_ERROR_LOCATION_1_i (where i = 0)	0x426
	ELM_ERROR_LOCATION_2_i (where i = 0)	0x775
	ELM_ERROR_LOCATION_3_i (where i = 0)	0xD7C
Clear the corresponding interrupt for polynomial 0.	ELM_IRQSTATUS[0] LOC_VALID_0	0x1

The NAND flash data in the sector are seen as a polynomial of degree 4223 (number of bits in a 528 byte buffer minus 1), with each data bit being a coefficient in the polynomial. When reading from a NAND flash using the GPMC module, computation of the polynomial syndrome assumes that the first NAND word read at address 0x0 contains the highest-order coefficient in the message. Furthermore, in the 16-bit NAND word, bits are ordered from bit 7 to bit 0, and then from bit 15 to bit 8. Based on this convention, an address table of the data buffer can be built. NAND memory addresses in Table 15-472 are given in decimal format.

Table 15-472. 16-Bit NAND Sector Buffer Address Map

NAND Memory Address	Message Bit Addresses in Memory Word															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	4215	4214	4213	4212	4211	4210	4209	4208	4223	4222	4221	4220	4219	4218	4217	4216
1	4175	4174	4173	4172	4171	4170	4169	4168	4183	4182	4181	4180	4179	4178	4177	4176
...																
47	3463	3462	3461	3460	3459	3458	3457	3456	3471	3470	3469	3468	3467	3466	3465	3464
48	3447	3446	3445	3444	3443	3442	3441	3440	3455	3454	3453	3452	3451	3450	3449	3448
49	3431	3430	3429	3428	3427	3426	3425	3424	3439	3438	3437	3436	3435	3434	3433	3432
50	3415	3414	3413	3412	3411	3410	3409	3408	3423	3422	3421	3420	3419	3418	3417	3416
...																
255	135	134	133	132	131	130	129	128	143	142	141	140	139	138	137	136
256	119	118	117	116	115	114	113	112	127	126	125	124	123	122	121	120
257	103	102	101	100	99	98	97	96	111	110	109	108	107	106	105	104
258	87	86	85	84	83	82	81	80	95	94	93	92	91	90	89	88
259	71	70	69	68	67	66	65	64	79	78	77	76	75	74	73	72
260	55	54	53	52	51	50	49	48	63	62	61	60	59	58	57	56
261	39	38	37	36	35	34	33	32	47	46	45	44	43	42	41	40
262	23	22	21	20	19	18	17	16	31	30	29	28	27	26	25	24
263	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

The table can now be used to determine which bits in the buffer were incorrect and must be flipped. In this example, the first bit to be flipped is bit 4 from the 49th byte read from memory. It is up to the processor to correctly map this word to the copied buffer and flip this bit. The same process must be repeated for all detected errors.

15.5.4.3 Use Case: ELM Used in Page Mode

In this example, the ELM module is programmed for an 16-bit error-correction capability in page mode (see Table 15-473). After reading a 528-byte NAND flash sector (512B data plus 16B spare area) with a 16-bit interface, four non-zero polynomial syndromes are reported from the GPMC (polynomial syndrome 0, 1, 2, and 3 are used in the ELM):

- P0 = 0xE8B0 12ADDB5A318E05BE B0693DB28330B5CC A329AA05E0B718EF
- P1 = 0xBAD0 49A0D932C22E6669 0948DF08BE093336 79C6BA10E5F935EB
- P2 = 0x69D9 B86ABCD5EC3697FA A6498FEE54556EA0 1579EF7D60BA3189

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- P3 = 0x0

Table 15-473. Use Case: Page Mode

Step	Register/Bit Field/Programming Model	Value
Resets the module	ELM_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is done.	ELM_SYSSTATUS[0] RESETDONE	0x1
Configure the slave interface power management: Smart idle is used.	ELM_SYSCONFIG[4:3] SIDLEMODE	0x2
Defines the error-correction level used: 16 bits	ELM_LOCATION_CONFIG[1:0] ECC_BCH_LEVEL	0x2
Defines the maximum buffer length: 528 bytes	ELM_LOCATION_CONFIG[26:16] ECC_SIZE	0x420
Sets the ELM in page mode (four blocks in a page)	ELM_PAGE_CTRL[0] SECTOR_0	0x1
	ELM_PAGE_CTRL[1] SECTOR_1	0x1
	ELM_PAGE_CTRL[2] SECTOR_2	0x1
	ELM_PAGE_CTRL[3] SECTOR_3	0x1
Disable all interrupts for syndrome polynomial and enable PAGE_MASK interrupt.	ELM_IRQENABLE	0x100
Set the input syndrome polynomial 0.	ELM_SYNDROME_FRAGMENT_0_i (where i = 0)	0xE0B718EF
	ELM_SYNDROME_FRAGMENT_1_i (where i = 0)	0xA329AA05
	ELM_SYNDROME_FRAGMENT_2_i (where i = 0)	0x8330B5CC
	ELM_SYNDROME_FRAGMENT_3_i (where i = 0)	0xB0693DB2
	ELM_SYNDROME_FRAGMENT_4_i (where i = 0)	0x318E05BE
	ELM_SYNDROME_FRAGMENT_5_i (where i = 0)	0x12ADDB5A
	ELM_SYNDROME_FRAGMENT_6_i (where i = 0)	0xE8B0
Set the input syndrome polynomial 1.	ELM_SYNDROME_FRAGMENT_0_i (where i = 1)	0xE5F935EB
	ELM_SYNDROME_FRAGMENT_1_i (where i = 1)	0x79C6BA10
	ELM_SYNDROME_FRAGMENT_2_i ((where i = 1)	0xBE093336
	ELM_SYNDROME_FRAGMENT_3_i (where i = 1)	0x0948DF08
	ELM_SYNDROME_FRAGMENT_4_i (where i = 1)	0xC22E6669
	ELM_SYNDROME_FRAGMENT_5_i (where i = 1)	0x49A0D932
	ELM_SYNDROME_FRAGMENT_6_i (where i = 1)	0xBAD0
Set the input syndrome polynomial 2.	ELM_SYNDROME_FRAGMENT_0_i (where i = 2)	0x60BA3189
	ELM_SYNDROME_FRAGMENT_1_i (where i = 2)	0x1579EF7D
	ELM_SYNDROME_FRAGMENT_2_i (where i = 2)	0x54556EA0
	ELM_SYNDROME_FRAGMENT_3_i (where i = 2)	0xA6498FEE
	ELM_SYNDROME_FRAGMENT_4_i (where i = 2)	0xEC3697FA
	ELM_SYNDROME_FRAGMENT_5_i (where i = 2)	0xB86ABCD5
	ELM_SYNDROME_FRAGMENT_6_i (where i = 2)	0x69D9
Set the input syndrome polynomial 3.	ELM_SYNDROME_FRAGMENT_0_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_1_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_2_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_3_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_4_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_5_i (where i = 3)	0x0
	ELM_SYNDROME_FRAGMENT_6_i (where i = 3)	0x0
Initiates the computation process for syndrome polynomial 0	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 0)	0x1
Initiates the computation process for syndrome polynomial 1	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 1)	0x1
Initiates the computation process for syndrome polynomial 2	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 2)	0x1
Initiates the computation process for syndrome polynomial 3	ELM_SYNDROME_FRAGMENT_6_i[16] SYNDROME_VALID (where i = 3)	0x1

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Table 15-473. Use Case: Page Mode (continued)

Step	Register/Bit Field/Programming Model	Value
Wait until process is complete for syndrome polynomial 0, 1, 2, and 3: Wait until the ELM_IRQ interrupt is generated or poll the status register.		
Wait for page completed interrupt: All error locations are valid.	ELM_IRQSTATUS[8] PAGE_VALID	0x1
Read the process exit status for syndrome polynomial 0: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 0)	0x1
Read the process exit status for syndrome polynomial 1: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 1)	0x1
Read the process exit status for syndrome polynomial 2: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 2)	0x1
Read the process exit status for syndrome polynomial 3: All errors were successfully located.	ELM_LOCATION_STATUS_i[8] ECC_CORRECTABLE (where i = 3)	0x1
Read the number of errors for syndrome polynomial 0: four errors detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (where i = 0)	0x4
Read the number of errors for syndrome polynomial 1: two errors detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (where i = 1)	0x2
Read the number of errors for syndrome polynomial 2: one error detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (where i = 2)	0x1
Read the number of errors for syndrome polynomial 3: no errors detected.	ELM_LOCATION_STATUS_i[4:0] ECC_NB_ERRORS (where i = 3)	0x0
Read the error-location bit addresses for syndrome polynomial 0 of the first four registers:	ELM_ERROR_LOCATION_0_i (where i = 0)	0x1FE
	ELM_ERROR_LOCATION_1_i (where i = 0)	0x617
	ELM_ERROR_LOCATION_2_i (where i = 0)	0x650
	ELM_ERROR_LOCATION_3_i (where i = 0)	0xA83
Read the error-location bit addresses for syndrome polynomial 1 of the first two registers:	ELM_ERROR_LOCATION_0_i (where i = 1)	0x4
	ELM_ERROR_LOCATION_1_i (where i = 1)	0x1036
Read the errors location bit addresses for syndrome polynomial 2 of the first registers:	ELM_ERROR_LOCATION_0_i (where i = 1)	0x3E8
Clear the ELM_IRQSTATUS register.	ELM_IRQSTATUS	0x1FF

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15.5.5 ELM Register Manual

15.5.5.1 ELM Instance Summary

Table 15-474summarizes the ELM instance.

Table 15-474. ELM Instance Summary

Module Name	Base Address	Size
ELM	0x4807 8000	4 KiB

15.5.5.2 ELM Registers

15.5.5.2.1 ELM Register Summary

Table 15-475 summarizes the ELM register mapping.

Table 15-475. ELM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address ELM
ELM_REVISION	R	32	0x0000 0000	0x4807 8000
ELM_SYSCONFIG	RW	32	0x0000 0010	0x4807 8010
ELM_SYSSTATUS	R	32	0x0000 0014	0x4807 8014
ELM_IRQSTATUS	RW	32	0x0000 0018	0x4807 8018
ELM_IRQENABLE	RW	32	0x0000 001C	0x4807 801C
ELM_LOCATION_CONFIG	RW	32	0x0000 0020	0x4807 8020
ELM_PAGE_CTRL	RW	32	0x0000 0080	0x4807 8080
ELM_SYNDROME_FRAGMENT_0_i (1)	RW	32	0x0000 0400 + (0x40 * i)	0x4807 8400 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_1_i (1)	RW	32	0x0000 0404 + (0x40 * i)	0x4807 8404 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_2_i (1)	RW	32	0x0000 0408 + (0x40 * i)	0x4807 8408 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_3_i (1)	RW	32	0x0000 040C + (0x40 * i)	0x4807 840C + (0x40 * i)
ELM_SYNDROME_FRAGMENT_4_i (1)	RW	32	0x0000 0410 + (0x40 * i)	0x4807 8410 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_5_i (1)	RW	32	0x0000 0414 + (0x40 * i)	0x4807 8414 + (0x40 * i)
ELM_SYNDROME_FRAGMENT_6_i (1)	RW	32	0x0000 0418 + (0x40 * i)	0x4807 8418 + (0x40 * i)
ELM_LOCATION_STATUS_i (1)	R	32	0x0000 0800 + (0x100 * i)	0x4807 8800 + (0x100 * i)
ELM_ERROR_LOCATION_0_i (1)	R	32	0x0000 0880 + (0x100 * i)	0x4807 8880 + (0x100 * i)
ELM_ERROR_LOCATION_1_i (1)	R	32	0x0000 0884 + (0x100 * i)	0x4807 8884 + (0x100 * i)
ELM_ERROR_LOCATION_2_i (1)	R	32	0x0000 0888 + (0x100 * i)	0x4807 8888 + (0x100 * i)
ELM_ERROR_LOCATION_3_i (1)	R	32	0x0000 088C + (0x100 * i)	0x4807 888C + (0x100 * i)
ELM_ERROR_LOCATION_4_i (1)	R	32	0x0000 0890 + (0x100 * i)	0x4807 8890 + (0x100 * i)
ELM_ERROR_LOCATION_5_i (1)	R	32	0x0000 0894 + (0x100 * i)	0x4807 8894 + (0x100 * i)
ELM_ERROR_LOCATION_6_i (1)	R	32	0x0000 0898 + (0x100 * i)	0x4807 8898 + (0x100 * i)
ELM_ERROR_LOCATION_7_i (1)	R	32	0x0000 089C + (0x100 * i)	0x4807 889C + (0x100 * i)
ELM_ERROR_LOCATION_8_i (1)	R	32	0x0000 08A0 + (0x100 * i)	0x4807 88A0 + (0x100 * i)
ELM_ERROR_LOCATION_9_i (1)	R	32	0x0000 08A4 + (0x100 * i)	0x4807 88A4 + (0x100 * i)
ELM_ERROR_LOCATION_10_i (1)	R	32	0x0000 08A8 + (0x100 * i)	0x4807 88A8 + (0x100 * i)
ELM_ERROR_LOCATION_11_i (1)	R	32	0x0000 08AC + (0x100 * i)	0x4807 88AC + (0x100 * i)
ELM_ERROR_LOCATION_12_i (1)	R	32	0x0000 08B0 + (0x100 * i)	0x4807 88B0 + (0x100 * i)
ELM_ERROR_LOCATION_13_i (1)	R	32	0x0000 08B4 + (0x100 * i)	0x4807 88B4 + (0x100 * i)
ELM_ERROR_LOCATION_14_i (1)	R	32	0x0000 08B8 + (0x100 * i)	0x4807 88B8 + (0x100 * i)
ELM_ERROR_LOCATION_15_i (1)	R	32	0x0000 08BC + (0x100 * i)	0x4807 88BC + (0x100 * i)

(1) i = 0 to 7 for ELM

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15.5.5.2.2 ELM Register Description

through describe the individual ELM registers.

Table 15-476. ELM_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4807 8000	**Instance**	ELM
Description	This register contains the IP revision code. (A write or reset of to this register has no effect.)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision (TI internal data)	R	0x-

Table 15-477. Register Call Summary for Register ELM_REVISION

Error Location Module

- ELM Register Summary: [0]

Table 15-478. ELM_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4807 8010	**Instance**	ELM
Description	This register allows controlling various parameters of the OCP interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CLOCKACTIVITYOCP	RESERVED			SIDLEMODE		RESERVED	SOFTRESET	AUTOGATING

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	CLOCKACTIVITYOCP	OCP clock activity when module is in IDLE mode (during wake-up mode period) 0x0: OCP clock can be switched off. 0x1: OCP clock is maintained during wake-up period.	RW	0
7:5	RESERVED	Reserved	R	0x0
4:3	SIDLEMODE	Slave interface power management (IDLE req/ack control) 0x0: Force-idle. IDLE request is acknowledged unconditionally and immediately (Default *Dumb* mode for safety) 0x1: No-idle. IDLE request is never acknowledged. 0x2: Smart-idle. The acknowledgment to an IDLE request is given based on the internal activity. 0x3: Reserved - do not use	RW	0x2

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Bits	Field Name	Description	Type	Reset
2	RESERVED	Reserved	R	0
1	SOFTRESET	Module software reset This bit is automatically reset by hardware (during reads, it always returns 0). It has same effect as the OCP hardware reset. 0x0: Normal mode 0x1: Start soft reset sequence.	RW	0
0	AUTOGATING	Internal OCP clock gating strategy (no module visible effect other than saving power) 0x0: OCP clock is free-running. 0x1: Automatic internal OCP clock gating strategy is applied based on the OCP interface activity.	RW	1

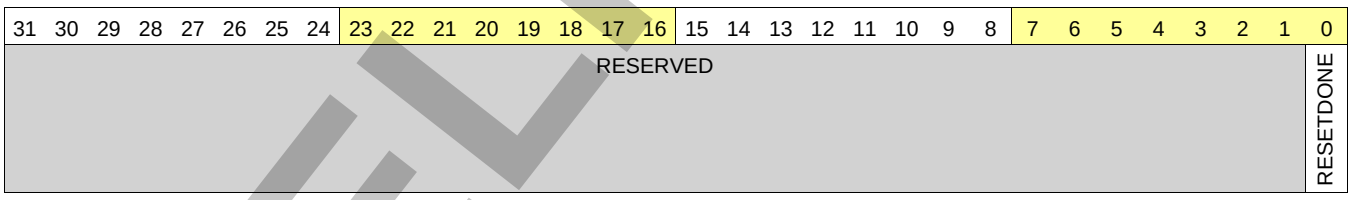
Table 15-479. Register Call Summary for Register ELM_SYSCONFIG

Error Location Module

- ELM Software Reset: [0] [1]
- ELM Power Management: [2] [3] [4]
- Processing Initialization: [5] [6]
- Use Case: ELM Used in Continuous Mode: [7] [8]
- Use Case: ELM Used in Page Mode: [9] [10]
- ELM Register Summary: [11]

Table 15-480. ELM_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4807 8014	**Instance**	ELM
Description	Internal reset monitoring (OCP domain) Undefined since: From hardware perspective, the reset state is 0. From software user perspective, when the accessible module is 1.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	Internal reset monitoring (OCP domain) Undefined since: From hardware perspective, the reset state is 0. From software user perspective, when the accessible module is 1. Read 0x0: Reset is ongoing. Read 0x1: Reset is done (completed).	R	1

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Table 15-481. Register Call Summary for Register ELM_SYSSTATUS

Error Location Module

- ELM Software Reset: [0]
- Processing Initialization: [1]
- Use Case: ELM Used in Continuous Mode: [2]
- Use Case: ELM Used in Page Mode: [3]
- ELM Register Summary: [4]

Table 15-482. ELM_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x4807 8018	**Instance**	ELM
Description	Interrupt status. This register doubles as a status register for the error-location processes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							PAGE_VALID	LOC_VALID_7	LOC_VALID_6	LOC_VALID_5	LOC_VALID_4	LOC_VALID_3	LOC_VALID_2	LOC_VALID_1	LOC_VALID_0

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	PAGE_VALID	Error-location status for a full page, based on the mask definition Read 0x0: Error locations invalid for all polynomials enabled in the ECC_INTERRUPT_MASK register Read 0x1: All error locations valid Write 0x0: No effect Write 0x1: Clear interrupt	RW	0
7	LOC_VALID_7	Error-location status for syndrome polynomial 7 Read 0x0: No syndrome processed or process in progress Read 0x1: Error-location process completed Write 0x0: No effect Write 0x1: Clear interrupt	RW W1toClr	0
6	LOC_VALID_6	Error-location status for syndrome polynomial 6	RW W1toClr	0
5	LOC_VALID_5	Error-location status for syndrome polynomial 5	RW W1toClr	0
4	LOC_VALID_4	Error-location status for syndrome polynomial 4	RW W1toClr	0
3	LOC_VALID_3	Error-location status for syndrome polynomial 3	RW W1toClr	0
2	LOC_VALID_2	Error-location status for syndrome polynomial 2	RW W1toClr	0
1	LOC_VALID_1	Error-location status for syndrome polynomial 1	RW W1toClr	0
0	LOC_VALID_0	Error-location status for syndrome polynomial 0	RW W1toClr	0

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Table 15-483. Register Call Summary for Register ELM_IRQSTATUS

Error Location Module

- ELM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- Processing Initialization: [9]
- Processing Completion: [10] [11] [12] [13] [14] [15] [16] [17] [18]
- Read Results: [19] [20] [21] [22] [23] [24]
- Use Case: ELM Used in Continuous Mode: [25] [26]
- Use Case: ELM Used in Page Mode: [27] [28] [29]
- ELM Register Summary: [30]

Table 15-484. ELM_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x4807 801C	**Instance**	ELM
Description	Interrupt enable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							PAGE_MASK	LOCATION_MASK_7	LOCATION_MASK_6	LOCATION_MASK_5	LOCATION_MASK_4	LOCATION_MASK_3	LOCATION_MASK_2	LOCATION_MASK_1	LOCATION_MASK_0

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	PAGE_MASK	Page interrupt mask bit 0: Disable interrupt 1: Enable interrupt	RW	0
7	LOCATION_MASK_7	Error-location interrupt mask bit for syndrome polynomial 7	RW	0
6	LOCATION_MASK_6	Error-location interrupt mask bit for syndrome polynomial 6	RW	0
5	LOCATION_MASK_5	Error-location interrupt mask bit for syndrome polynomial 5	RW	0
4	LOCATION_MASK_4	Error-location interrupt mask bit for syndrome polynomial 4	RW	0
3	LOCATION_MASK_3	Error-location interrupt mask bit for syndrome polynomial 3	RW	0
2	LOCATION_MASK_2	Error-location interrupt mask bit for syndrome polynomial 2	RW	0
1	LOCATION_MASK_1	Error-location interrupt mask bit for syndrome polynomial 1	RW	0
0	LOCATION_MASK_0	Error-location interrupt mask bit for syndrome polynomial 0 0: Disable interrupt 1: Enable interrupt	RW	0

Table 15-485. Register Call Summary for Register ELM_IRQENABLE

Error Location Module

- ELM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- Processing Initialization: [9] [10]
- Processing Completion: [11]
- Processing Initialization: [12] [13] [14]
- Use Case: ELM Used in Continuous Mode: [15]
- Use Case: ELM Used in Page Mode: [16]
- ELM Register Summary: [17]

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Table 15-486. ELM_LOCATION_CONFIG

Address Offset	0x0000 0020		
Physical Address	0x4807 8020	**Instance**	ELM
Description	ECC algorithm parameters		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ECC_SIZE								RESERVED														ECC_BCH_LEVEL	

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Reserved	R	0x00
26:16	ECC_SIZE	Maximum size of the buffers for which the error-location engine is used, in number of nibbles (4-bit entities)	RW	0x000
15:2	RESERVED	Reserved	R	0x0000
1:0	ECC_BCH_LEVEL	Error correction level 0x0: 4 bits 0x1: 8 bits 0x2: 16 bits 0x3: Reserved	RW	0x0

Table 15-487. Register Call Summary for Register ELM_LOCATION_CONFIG

Error Location Module

- Processing Initialization: [0] [1] [2]
- Processing Initialization: [3] [4]
- Use Case: ELM Used in Continuous Mode: [5] [6]
- Use Case: ELM Used in Page Mode: [7] [8]
- ELM Register Summary: [9]

Table 15-488. ELM_PAGE_CTRL

Address Offset	0x0000 0080		
Physical Address	0x4807 8080	**Instance**	ELM
Description	Page definition		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SECTOR_7	SECTOR_6	SECTOR_5	SECTOR_4	SECTOR_3	SECTOR_2	SECTOR_1	SECTOR_0

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7	SECTOR_7	Set to 1 if syndrome polynomial 7 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
6	SECTOR_6	Set to 1 if syndrome polynomial 6 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
5	SECTOR_5	Set to 1 if syndrome polynomial 5 is part of the page in page mode. Must be 0 in continuous mode.	RW	0

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Bits	Field Name	Description	Type	Reset
4	SECTOR_4	Set to 1 if syndrome polynomial 4 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
3	SECTOR_3	Set to 1 if syndrome polynomial 3 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
2	SECTOR_2	Set to 1 if syndrome polynomial 2 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
1	SECTOR_1	Set to 1 if syndrome polynomial 1 is part of the page in page mode. Must be 0 in continuous mode.	RW	0
0	SECTOR_0	Set to 1 if syndrome polynomial 0 is part of the page in page mode. Must be 0 in continuous mode.	RW	0

Table 15-489. Register Call Summary for Register ELM_PAGE_CTRL

Error Location Module

- Processing Initialization: [0]
- Processing Completion: [1] [2] [3] [4]
- Processing Initialization: [5] [6] [7]
- Use Case: ELM Used in Continuous Mode: [8]
- Use Case: ELM Used in Page Mode: [9] [10] [11] [12]
- ELM Register Summary: [13]

Table 15-490. ELM_SYNDROME_FRAGMENT_0_i

Address Offset	0x0000 0400 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8400 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 0 to 31.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_0																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_0	Syndrome bits 0 to 31	RW	0x0000 0000

Table 15-491. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_0_i

Error Location Module

- Processing Initialization: [0]
- Processing Initialization: [1]
- Use Case: ELM Used in Continuous Mode: [2]
- Use Case: ELM Used in Page Mode: [3] [4] [5] [6]
- ELM Register Summary: [7]

Table 15-492. ELM_SYNDROME_FRAGMENT_1_i

Address Offset	0x0000 0404 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8404 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 32 to 63.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_1																															

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Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_1	Syndrome bits 32 to 63	RW	0x0000 0000

Table 15-493. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_1_i

Error Location Module
- Processing Initialization: [0]
- Use Case: ELM Used in Continuous Mode: [1]
- Use Case: ELM Used in Page Mode: [2] [3] [4] [5]
- ELM Register Summary: [6]

Table 15-494. ELM_SYNDROME_FRAGMENT_2_i

Address Offset	0x0000 0408 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8408 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 64 to 95.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_2																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_2	Syndrome bits 64 to 95	RW	0x0000 0000

Table 15-495. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_2_i

Error Location Module
- Use Case: ELM Used in Continuous Mode: [0]
- Use Case: ELM Used in Page Mode: [1] [2] [3] [4]
- ELM Register Summary: [5]

Table 15-496. ELM_SYNDROME_FRAGMENT_3_i

Address Offset	0x0000 040C + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 840C + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 96 to 127		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_3																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_3	Syndrome bits 96 to 127	RW	0x0000 0000

Table 15-497. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_3_i

Error Location Module
- Use Case: ELM Used in Continuous Mode: [0]
- Use Case: ELM Used in Page Mode: [1] [2] [3] [4]
- ELM Register Summary: [5]

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Table 15-498. ELM_SYNDROME_FRAGMENT_4_i

Address Offset	0x0000 0410 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8410 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 128 to 159.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_4																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_4	Syndrome bits 128 to 159	RW	0x0000 0000

Table 15-499. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_4_i

Error Location Module

- Use Case: ELM Used in Page Mode: [0] [1] [2] [3]
- ELM Register Summary: [4]

Table 15-500. ELM_SYNDROME_FRAGMENT_5_i

Address Offset	0x0000 0414 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8414 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 160 to 191.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_5																															

Bits	Field Name	Description	Type	Reset
31:0	SYNDROME_5	Syndrome bits 160 to 191	RW	0x0000 0000

Table 15-501. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_5_i

Error Location Module

- Processing Initialization: [0]
- Use Case: ELM Used in Page Mode: [1] [2] [3] [4]
- ELM Register Summary: [5]

Table 15-502. ELM_SYNDROME_FRAGMENT_6_i

Address Offset	0x0000 0418 + (0x40 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8418 + (0x40 * i)	**Instance**	ELM
Description	Input syndrome polynomial bits 192 to 207.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SYNDROME_VALID	SYNDROME_6															

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Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Reserved	R	0x0000
16	SYNDROME_VALID	Syndrome valid bit 0x0: This syndrome polynomial must not be processed. 0x1: This syndrome polynomial must be processed.	RW	0
15:0	SYNDROME_6	Syndrome bits 192 to 207	RW	0x0000

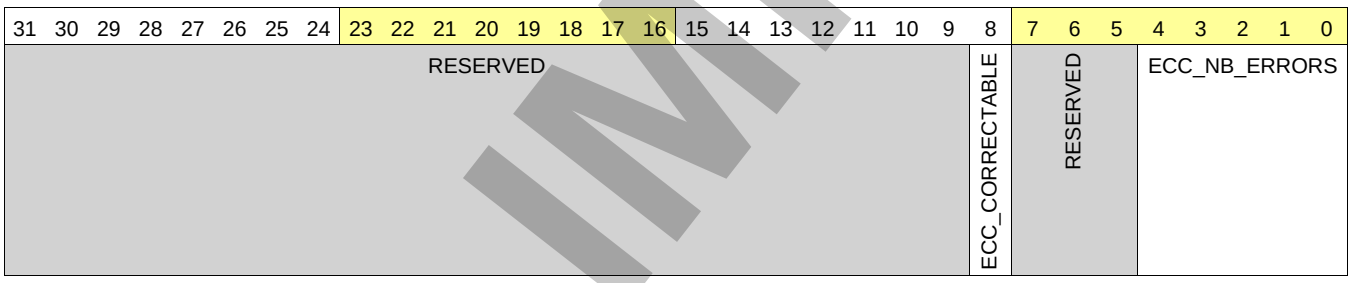
Table 15-503. Register Call Summary for Register ELM_SYNDROME_FRAGMENT_6_i

Error Location Module

- Processing Initialization: [0] [1] [2] [3]
- Processing Completion: [4] [5]
- Processing Initialization: [6] [7]
- Read Results: [8]
- Use Case: ELM Used in Continuous Mode: [9]
- Use Case: ELM Used in Page Mode: [10] [11] [12] [13] [14] [15] [16] [17]
- ELM Register Summary: [18]

Table 15-504. ELM_LOCATION_STATUS_i

Address Offset	0x0000 0800 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8800 + (0x100 * i)	**Instance**	ELM
Description	Exit status for the syndrome polynomial processing		
Type	R		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	ECC_CORRECTABLE	Error-location process exit status 0x0: ECC error-location process failed. Number of errors and error locations are invalid. 0x1: All errors were successfully located. Number of errors and error locations are valid.	R	0
7:5	RESERVED	Reserved	R	0x0
4:0	ECC_NB_ERRORS	Number of errors detected and located	R	0x00

Table 15-505. Register Call Summary for Register ELM_LOCATION_STATUS_i

Error Location Module

- Processing Initialization: [0]
- Processing Sequence: [1] [2] [3] [4] [5]
- Processing Completion: [6] [7] [8]
- Read Results: [9] [10] [11] [12] [13] [14] [15] [16]
- Use Case: ELM Used in Continuous Mode: [17] [18]
- Use Case: ELM Used in Page Mode: [19] [20] [21] [22] [23] [24] [25] [26]
- ELM Register Summary: [27]

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Table 15-506. ELM_ERROR_LOCATION_0_i

Address Offset	0x0000 0880 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8880 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_ERROR_LOCATION															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-507. Register Call Summary for Register ELM_ERROR_LOCATION_0_i

Error Location Module

- Processing Initialization: [0]
- Processing Sequence: [1] [2] [3]
- Processing Completion: [4]
- Read Results: [5] [6]
- Use Case: ELM Used in Continuous Mode: [7]
- Use Case: ELM Used in Page Mode: [8] [9] [10]
- ELM Register Summary: [11]

Table 15-508. ELM_ERROR_LOCATION_1_i

Address Offset	0x0000 0884 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8884 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_ERROR_LOCATION															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-509. Register Call Summary for Register ELM_ERROR_LOCATION_1_i

Error Location Module

- Processing Sequence: [0]
- Read Results: [1] [2]
- Use Case: ELM Used in Continuous Mode: [3]
- Use Case: ELM Used in Page Mode: [4] [5]
- ELM Register Summary: [6]

Table 15-510. ELM_ERROR_LOCATION_2_i

Address Offset	0x0000 0888 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8888 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			ECC_ERROR_LOCATION												

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-511. Register Call Summary for Register ELM_ERROR_LOCATION_2_i

Error Location Module

- Use Case: ELM Used in Continuous Mode: [0]
- Use Case: ELM Used in Page Mode: [1]
- ELM Register Summary: [2]

Table 15-512. ELM_ERROR_LOCATION_3_i

Address Offset	0x0000 088C + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 888C + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			ECC_ERROR_LOCATION												

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-513. Register Call Summary for Register ELM_ERROR_LOCATION_3_i

Error Location Module

- Use Case: ELM Used in Continuous Mode: [0]
- Use Case: ELM Used in Page Mode: [1]
- ELM Register Summary: [2]

Table 15-514. ELM_ERROR_LOCATION_4_i

Address Offset	0x0000 0890 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8890 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			ECC_ERROR_LOCATION												

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-515. Register Call Summary for Register ELM_ERROR_LOCATION_4_i

Error Location Module

- ELM Register Summary: [0]

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Table 15-516. ELM_ERROR_LOCATION_5_i

Address Offset	0x0000 0894 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8894 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-517. Register Call Summary for Register ELM_ERROR_LOCATION_5_i

Error Location Module

- ELM Register Summary: [0]

Table 15-518. ELM_ERROR_LOCATION_6_i

Address Offset	0x0000 0898 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 8898 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-519. Register Call Summary for Register ELM_ERROR_LOCATION_6_i

Error Location Module

- ELM Register Summary: [0]

Table 15-520. ELM_ERROR_LOCATION_7_i

Address Offset	0x0000 089C + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 889C + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

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Table 15-521. Register Call Summary for Register ELM_ERROR_LOCATION_7_i

Error Location Module

- ELM Register Summary: [0]

Table 15-522. ELM_ERROR_LOCATION_8_i

Address Offset	0x0000 08A0 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88A0 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_ERROR_LOCATION															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-523. Register Call Summary for Register ELM_ERROR_LOCATION_8_i

Error Location Module

- ELM Register Summary: [0]

Table 15-524. ELM_ERROR_LOCATION_9_i

Address Offset	0x0000 08A4 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88A4 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_ERROR_LOCATION															

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-525. Register Call Summary for Register ELM_ERROR_LOCATION_9_i

Error Location Module

- ELM Register Summary: [0]

Table 15-526. ELM_ERROR_LOCATION_10_i

Address Offset	0x0000 08A8 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88A8 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_ERROR_LOCATION															

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-527. Register Call Summary for Register ELM_ERROR_LOCATION_10_i

Error Location Module
- ELM Register Summary: [0]

Table 15-528. ELM_ERROR_LOCATION_11_i

Address Offset	0x0000 08AC + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88AC + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-529. Register Call Summary for Register ELM_ERROR_LOCATION_11_i

Error Location Module
- ELM Register Summary: [0]

Table 15-530. ELM_ERROR_LOCATION_12_i

Address Offset	0x0000 08B0 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88B0 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-531. Register Call Summary for Register ELM_ERROR_LOCATION_12_i

Error Location Module
- ELM Register Summary: [0]

Table 15-532. ELM_ERROR_LOCATION_13_i

Address Offset	0x0000 08B4 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88B4 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-533. Register Call Summary for Register ELM_ERROR_LOCATION_13_i

Error Location Module
- ELM Register Summary: [0]

Table 15-534. ELM_ERROR_LOCATION_14_i

Address Offset	0x0000 08B8 + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88B8 + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-535. Register Call Summary for Register ELM_ERROR_LOCATION_14_i

Error Location Module
- ELM Register Summary: [0]

Table 15-536. ELM_ERROR_LOCATION_15_i

Address Offset	0x0000 08BC + (0x100 * i)	**Index**	i = 0 to 7
Physical Address	0x4807 88BC + (0x100 * i)	**Instance**	ELM
Description	Error-location register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ECC_ERROR_LOCATION							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	R	0x00000
12:0	ECC_ERROR_LOCATION	Error-location bit address	R	0x0000

Table 15-537. Register Call Summary for Register ELM_ERROR_LOCATION_15_i

Error Location Module
- Processing Initialization: [0]
- Processing Sequence: [1] [2]
- Processing Completion: [3]
- Read Results: [4] [5]
- ELM Register Summary: [6]

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15.6 On-Chip Memory (OCM) Subsystem

15.6.1 OCM Subsystem Overview

There are two on-chip memories in the device.

- 5-KiB SAR random-access memory (RAM)
- 128-KiB level 3 (L3) static random-access memory (L3 OCM_RAM)

There are other on-chip memories inside other subsystems (MPU, DSP, IVA-HD, ABE, IPU) that are not described in the following sections. For more information about these memories, see each subsystem chapter.

15.6.2 OCM Subsystem Integration

Figure 15-102 shows the integration of the OCM subsystem to the device.

Figure 15-102. OCM Subsystem Integration to the Device

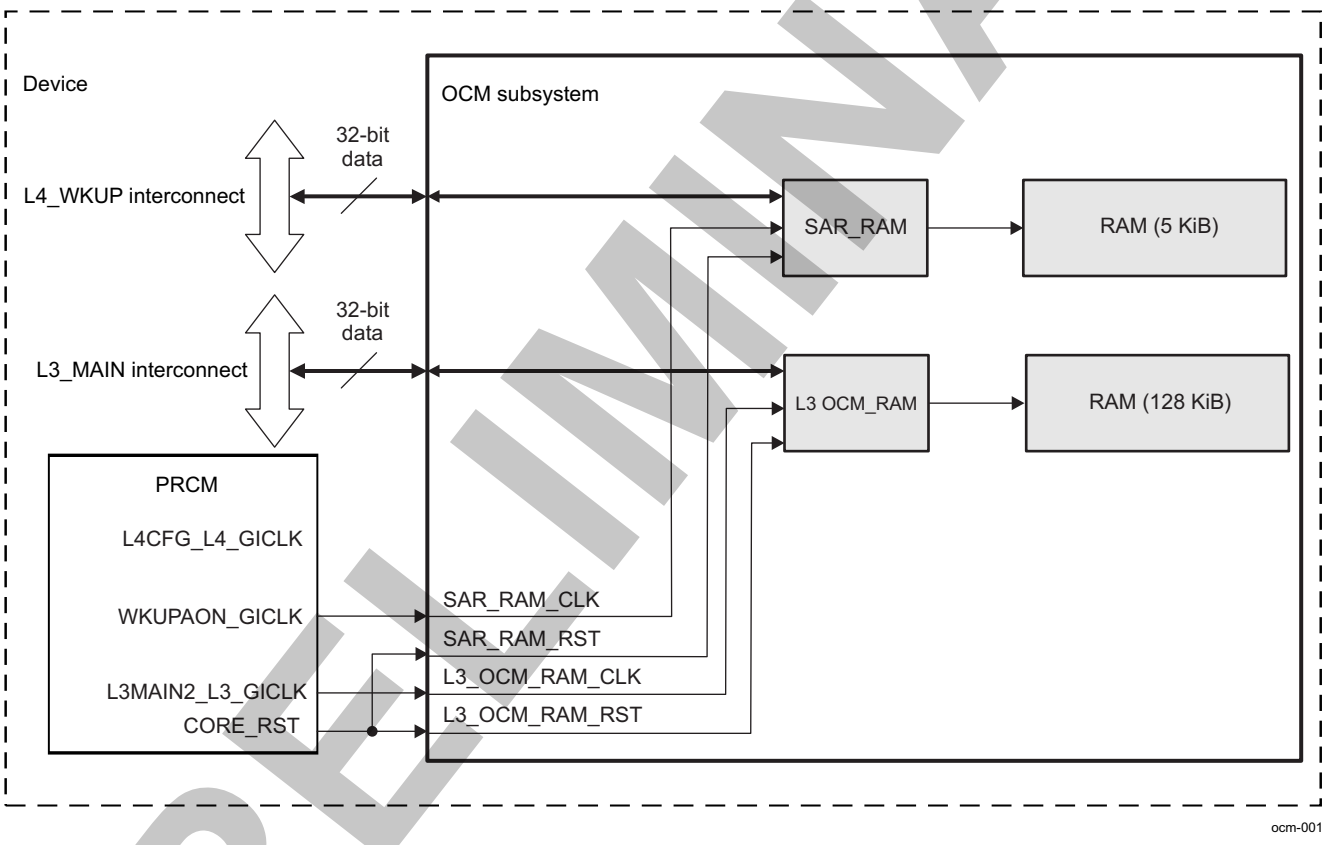

Table 15-538 and Table 15-539 summarize the integration of the module in the device.

Table 15-538. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
L3 OCM_RAM	PD_CORE	No	L3_MAIN
SAR_RAM	PD_WKUPAON	No	L4_WKUP

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Table 15-539. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L3 OCM_RAM	L3_OCM_RAM_CLK	L3MAIN_L3_GICLK	PRCM	L3 OCM_RAM Clock For information about power, reset, and clock management (PRCM) clock gating and management, see the Section 3.6.17, *CD_L3_MAIN2 Clock Domain* section in Section 3.1.1, *Power, Reset, and Clock Management*.
SAR_RAM	SAR_RAM_CLK	WKUPAON_GICLK	PRCM	SAR RAM clock For information about PRCM clock gating and management, see the Section 3.6.4.3, *CD_WKUPAON Clock Domain* section in Section 3.1.1, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
L3 OCM_RAM	L3_OCM_RAM_RST	CORE_RST	PRCM	L3 OCM_RAM reset signal For information about PRCM reset sources and distribution, see Section 3.5.4, *Reset Domains* section in Section 3.1.1, *Power, Reset, and Clock Management*.
SAR_RAM	SAR_RAM_RST	WKUPAON_RST	PRCM	SAR RAM reset signal

15.6.3 OCM Subsystem Functional Description

15.6.3.1 SAR RAM

The on-chip SAR RAM contains 5 KiB and is mapped as two blocks. The SAR RAM is used by device ROM code to store the software booting configuration: a logical structure that allows the redefinition of the ROM code default settings when booting after a warm reset. The SAR RAM is mapped on the wake-up voltage domain.

The device-embedded SAR RAM has the following characteristics:

- Support for single-access transactions
  - Operates at full L4_PER interconnect clock frequency
  - 32-bit access per cycle

The SAR RAM space is at the following location:

- SAR space 1 (4 KiB): Starts at 0x4AE2 6000 and ends at 0x4AE2 6FFF
- SAR space 2 (1 KiB): Starts at 0x4AE2 7000 and ends at 0x4AE2 73FF

15.6.3.2 L3 OCM_RAM

The on-chip L3 OCM_RAM contains 128 KiB of RAM, partitioning is defined by the L3 firewall logic.

The device-embedded L3 OCM_RAM has the following characteristics:

- Support for single and burst access transactions:
  - Operates at full L3 interconnect clock frequency
  - Fully pipelined, one 32-bit access per cycle
- Restricted access support based on:
  - A region-based partitioning (see the L3 firewall description)
  - The module owner of the access, with respect to its read and write permissions to that region
  - The transaction attributes of the access, with respect to the region permission properties. For more information, see Section 14.2.1, *L3 _MAIN Interconnect*.

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The memory space of the embedded RAM starts at 0x4030 0000 and ends at 0x4031 FFFF.

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System DMA

This chapter describes the system direct memory access (DMA_SYSTEM) module.

NOTE: Some of the system DMA features, primarily those concerning the device I/O pads and the system DMA integration, are not available in all OMAP54xx devices.

For details, see , *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

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16.1 DMA_SYSTEM Module Overview

The system direct memory access (DMA_SYSTEM) module, also called DMA4, performs high-performance data transfers between memories and peripheral devices without microprocessor unit (MPU) or digital signal processor (DSP) support during transfer. A DMA transfer is programmed through a logical DMA channel, which allows the transfer to be optimally tailored to the requirements of the application.

The DMA controller includes the following main features:

- Data transfer support in either direction between:
  - Memory and memory
  - Memory and peripheral device
- 32 logical DMA channels supporting:
  - Multiple concurrent transfers
  - Independent transfer profile for each channel
  - 8-bit, 16-bit, or 32-bit data element transfer size
  - Software-triggered or hardware-synchronized transfers
  - Flexible source and destination address generation
  - Burst read and write - max burst size is 16
  - Chained multiple-channel transfers
  - Endianism conversion
  - Draining
  - Linked-list support for descriptor types 1, 2, and 3
- First-come, first-serve DMA scheduling with fixed priority
- Up to 127 DMA requests
- Constant fill
- Transparent copy
- Four programmable interrupt request output lines
- FIFO depth: 256 × 64-bit
- Data buffering
- FIFO budget allocation
- Power-management support
- Auto-idle power-saving support
- Implementation of retention flip-flops (RFFs) to support dynamic power switching (DPS) between system power modes without MPU involvement. For more information about DPS, see Section 3.1.2.3, *Dynamic Power Switching*, in Chapter 3, *Power, Reset and Clock Management*.

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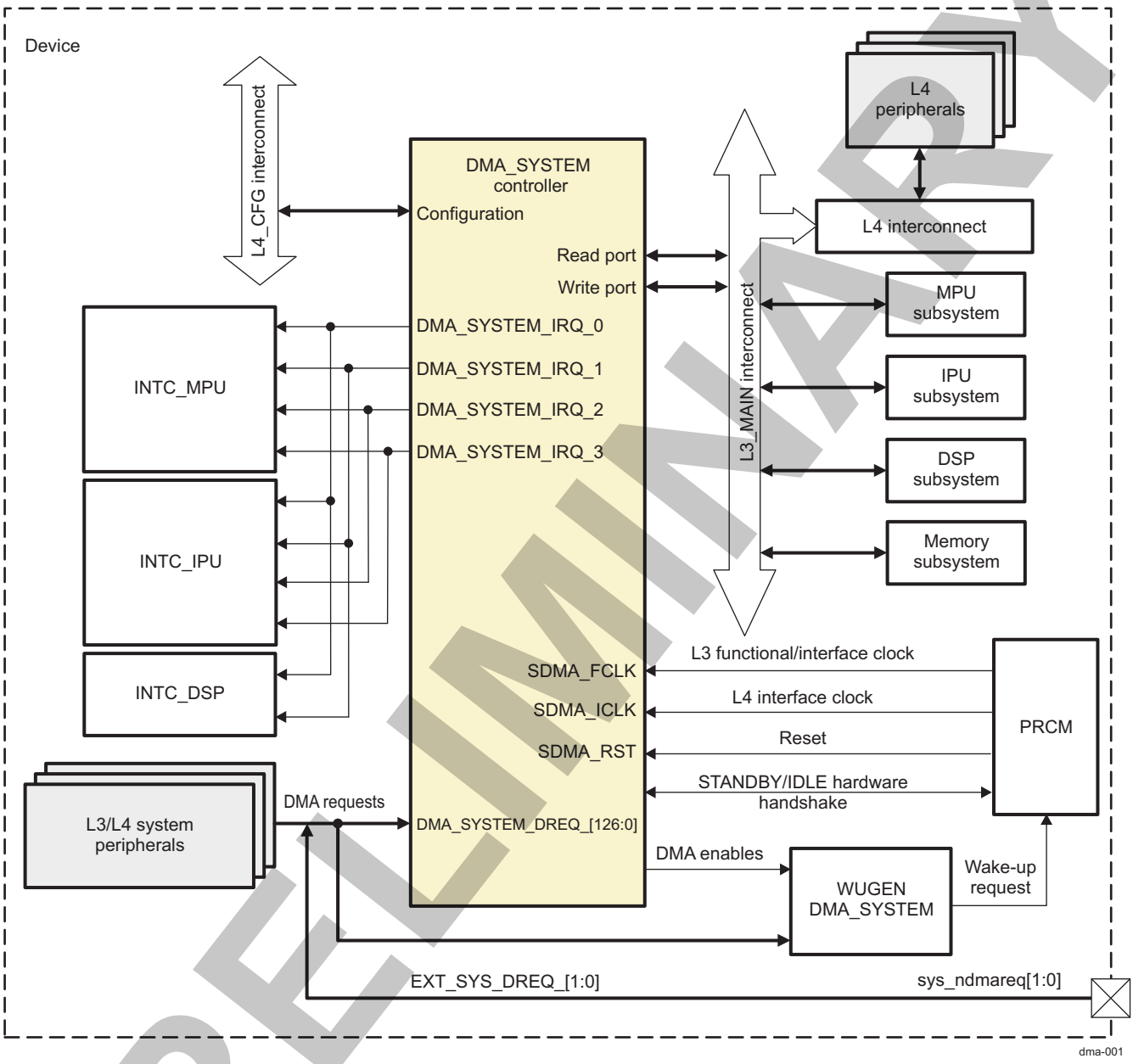
Figure 16-1 shows an overview of the DMA_SYSTEM module.

Figure 16-1. DMA_SYSTEM Overview



The DMA_SYSTEM module has three ports: one read, one write, and one configuration port, and provides multiple logical channel support. A dynamically allocated FIFO queue memory pool provides buffering between the read and write ports, which are multithreaded (two threads for the write port and four threads for the read port); this means that each transaction is flagged by a thread ID (0, 1, 2, or 3) in the request direction and in the response direction. This allows the read port to have four outstanding requests at a time. The write port has two threads budget available.

The MPU (or DSP) configures the DMA_SYSTEM through the L4_CFG interconnect.

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16.2 DMA_SYSTEM Controller Environment

The DMA_SYSTEM controller supports external DMA requests through the sys_ndmareq[1:0] pins (see Table 16-1). A logical channel can be configured to respond to an external synchronization request.

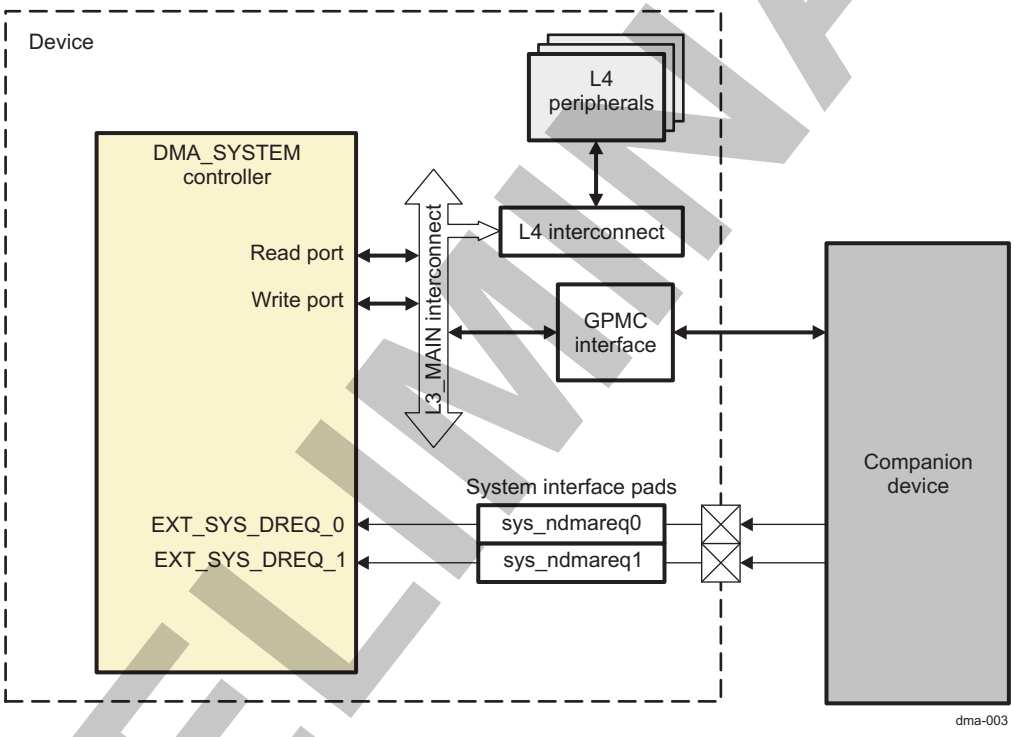
Table 16-1. External DMA_SYSTEM Request Signals

Pin Name	Signal Name	I/O[1]	Description	Module Reset Value
sys_ndmareq0	EXT_SYS_DREQ_0	I	External DMA request 0 (system expansion)	Z
sys_ndmareq1	EXT_SYS_DREQ_1	I	External DMA request 1 (system expansion)	Z

(1) I = Input, O = Output

Figure 16-2 shows an example of how to use the external hardware DMA request pins in the DMA_SYSTEM environment.

Figure 16-2. Example of External DMA Requests Use



An external device can use the external DMA request pins to start a logical channel transfer over the general-purpose memory controller (GPMC) interface. The transfer can be a memory-to-memory transfer in which the source memory is in the external device.

By default, the external DMA request signals are not available on external pins after a cold reset. For more information about multiplexing out the two signal lines to pins, see Chapter 18, *Control Module*.

All 127 DMA request lines are transition sensitive.

For a transition-sensitive DMA request (see Figure 16-3), the line must be maintained low (asserted) until the first DMA access is complete, after which the line must be maintained high (deasserted) for greater than one clock cycle (DMA_L3_GICLK):

- When the deassertion time is less than one clock cycle, the DMA_SYSTEM may not detect the deassertion.
- When the channel is enabled one cycle after a DMA request is disabled, the channel detects the DMA request and starts the corresponding transfer.
- When the channel is enabled two cycles after the DMA request is disabled, the channel does not detect the DMA request.

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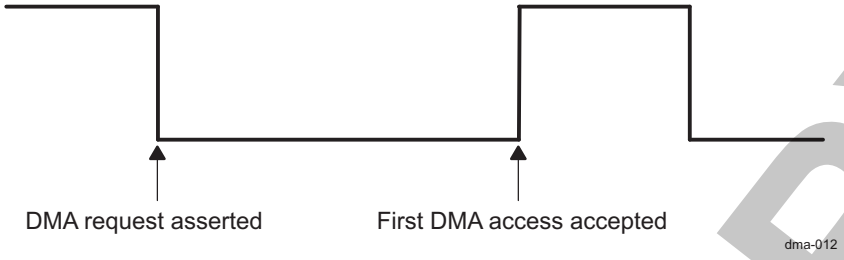
Figure 16-3. Transition-Sensitive DMA Request Scheme



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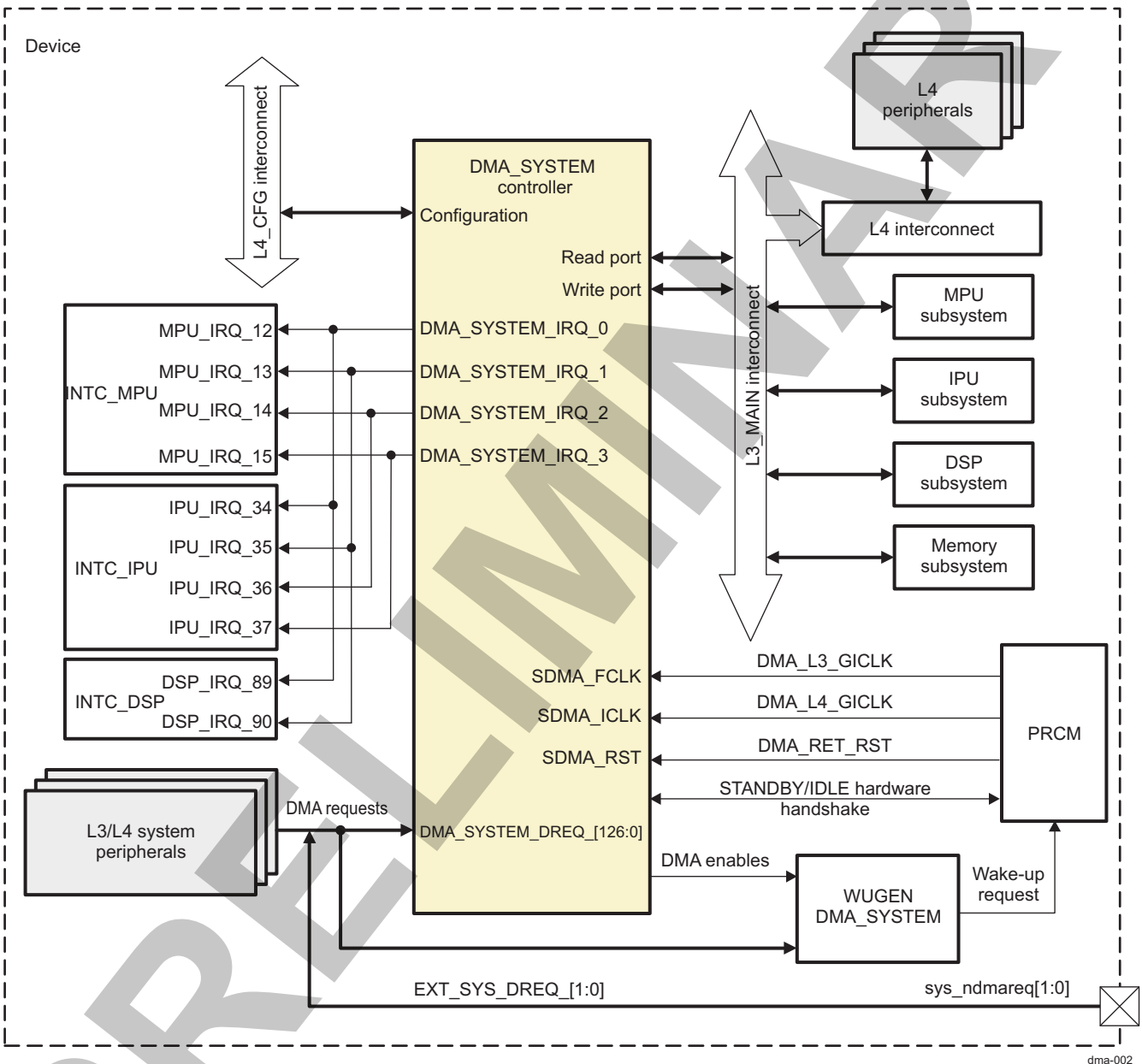
16.3 DMA_SYSTEM Module Integration

This section describes the integration of the module in the device, including information about clocks, resets, and hardware requests.

Figure 16-4 shows the DMA_SYSTEM controller integration.

Figure 16-4. DMA_SYSTEM Controller Integration



NOTE: For more information about the system DMA wake-up generator (WUGEN_DMA_SYSTEM), the STANDBY/IDLE hardware handshake, and the wake-up request, see Section 3.1.1.1.2, *Clock Management* , in Chapter 3, *Power, Reset, and Clock Management*.

Table 16-2 through Table 16-4 summarize the integration of the module in the device.

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Table 16-2. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
DMA_SYSTEM	PD_CORE	L3_MAIN and L4_CFG

Table 16-3. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMA_SYSTEM	SDMA_FCLK	DMA_L3_GICLK	PRCM	Functional clock for all internal logic and for the two master read and write ports. For information about the power, reset, and clock management (PRCM) clock gating and management, see Chapter 3, *Power, Reset, and Clock Management*.
	SDMA_ICLK	DMA_L4_GICLK		Interface clock. It supports the configuration port. For information about PRCM clock gating and management, see Chapter 3, *Power, Reset, and Clock Management*.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMA_SYSTEM	SDMA_RST	DMA_RET_RST	PRCM	Hardware retention reset. It initializes all internal logic of the DMA_SYSTEM module, all global registers, and some of the per-channel registers, implemented in flip-flops. However, all remaining per-channel registers are memory-based, and, therefore, are not reset (have undefined values). Thus, when programming a channel for the first time, all bits that have undefined reset values must be configured before enabling the channel. For information about PRCM reset sources and distribution, see Chapter 3, *Power, Reset, and Clock Management*.

Table 16-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DMA_SYSTEM	DMA_SYSTEM_IRQ_0	MPU_IRQ_12	INTC_MPU	DMA_SYSTEM interrupt request 0. For information about the INTC_MPU, see INTC_MPU Functional Description.
	DMA_SYSTEM_IRQ_1	MPU_IRQ_13	INTC_MPU	DMA_SYSTEM interrupt request 1
	DMA_SYSTEM_IRQ_2	MPU_IRQ_14	INTC_MPU	DMA_SYSTEM interrupt request 2
	DMA_SYSTEM_IRQ_3	MPU_IRQ_15	INTC_MPU	DMA_SYSTEM interrupt request 3
	DMA_SYSTEM_IRQ_0	IPU_IRQ_34	INTC_IPU	DMA_SYSTEM interrupt request 0. For information about the INTC_IPU, see INTC_IPU Functional Description.
	DMA_SYSTEM_IRQ_1	IPU_IRQ_35	INTC_IPU	DMA_SYSTEM interrupt request 1
	DMA_SYSTEM_IRQ_2	IPU_IRQ_36	INTC_IPU	DMA_SYSTEM interrupt request 2
	DMA_SYSTEM_IRQ_3	IPU_IRQ_37	INTC_IPU	DMA_SYSTEM interrupt request 3
	DMA_SYSTEM_IRQ_0	DSP_IRQ_89	INTC_DSP	DMA_SYSTEM interrupt request 0. For information about the INTC_DSP, see Interrupt Controllers Overview.

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Table 16-4. Hardware Requests (continued)

DMA_SYSTEM_IRQ_1	DSP_IRQ_90	INTC_DSP	DMA_SYSTEM interrupt request 1

NOTE: For a description of the interrupt source, see Section 16.4.2, *DMA_SYSTEM Controller Interrupt Requests*.

16.3.1 DMA Requests to the DMA_SYSTEM Controller

Table 16-5 lists the DMA_SYSTEM controller request mapping.

Table 16-5. DMA_SYSTEM Controller Request Mapping

DMA Request Line	Source	Description
DMA_SYSTEM_DREQ_0	Reserved	Reserved
DMA_SYSTEM_DREQ_1	EXT_SYS_DREQ_0	External DMA request 0 (system expansion)
DMA_SYSTEM_DREQ_2	EXT_SYS_DREQ_1	External DMA request 1 (system expansion)
DMA_SYSTEM_DREQ_3	GPMC_DREQ	GPMC data transmit request from prefetch engine
DMA_SYSTEM_DREQ_4	Reserved	Reserved
DMA_SYSTEM_DREQ_5	DISPC_DREQ	Frame update request
DMA_SYSTEM_DREQ_6	CT_TBR_DREQ	DEBUG subsystem CT_TBR request
DMA_SYSTEM_DREQ_7	MCASP_DREQ_AXEVT	MCASP transmit request
DMA_SYSTEM_DREQ_8	ISS_DREQ_1	Imaging subsystem request 1
DMA_SYSTEM_DREQ_9	ISS_DREQ_2	Imaging subsystem request 2
DMA_SYSTEM_DREQ_10	Reserved	Reserved
DMA_SYSTEM_DREQ_11	ISS_DREQ_3	Imaging subsystem request 3
DMA_SYSTEM_DREQ_12	ISS_DREQ_4	Imaging subsystem request 4
DMA_SYSTEM_DREQ_13	RFBI_DREQ	Display subsystem RFBI request
DMA_SYSTEM_DREQ_14	MCSPI3_DREQ_TX0	MCSPI3 transmit request channel 0
DMA_SYSTEM_DREQ_15	MCSPI3_DREQ_RX0	MCSPI3 receive request channel 0
DMA_SYSTEM_DREQ_16	MCBSP2_DREQ_TX	MCBSP2 transmit request
DMA_SYSTEM_DREQ_17	MCBSP2_DREQ_RX	MCBSP2 receive request
DMA_SYSTEM_DREQ_18	MCBSP3_DREQ_TX	MCBSP3 transmit request
DMA_SYSTEM_DREQ_19	MCBSP3_DREQ_RX	MCBSP3 receive request
DMA_SYSTEM_DREQ_20	Reserved	Reserved
DMA_SYSTEM_DREQ_21	Reserved	Reserved
DMA_SYSTEM_DREQ_22	Reserved	Reserved
DMA_SYSTEM_DREQ_23	Reserved	Reserved
DMA_SYSTEM_DREQ_24	I2C3_DREQ_TX	I2C3 transmit request
DMA_SYSTEM_DREQ_25	I2C3_DREQ_RX	I2C3 receive request
DMA_SYSTEM_DREQ_26	I2C1_DREQ_TX	I2C1 transmit request
DMA_SYSTEM_DREQ_27	I2C1_DREQ_RX	I2C1 receive request
DMA_SYSTEM_DREQ_28	I2C2_DREQ_TX	I2C2 transmit request
DMA_SYSTEM_DREQ_29	I2C2_DREQ_RX	I2C2 receive request
DMA_SYSTEM_DREQ_30	ISS_DREQ_5	Imaging subsystem request 5
DMA_SYSTEM_DREQ_31	ISS_DREQ_6	Imaging subsystem request 6
DMA_SYSTEM_DREQ_32	MCBSP1_DREQ_TX	MCBSP1 transmit request
DMA_SYSTEM_DREQ_33	MCBSP1_DREQ_RX	MCBSP1 receive request
DMA_SYSTEM_DREQ_34	MCSPI1_DREQ_TX0	MCSPI1 transmit request channel 0
DMA_SYSTEM_DREQ_35	MCSPI1_DREQ_RX0	MCSPI1 receive request channel 0

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Table 16-5. DMA_SYSTEM Controller Request Mapping (continued)

DMA Request Line	Source	Description
DMA_SYSTEM_DREQ_36	MCSPI1_DREQ_TX1	MCSPI1 transmit request channel 1
DMA_SYSTEM_DREQ_37	MCSPI1_DREQ_RX1	MCSPI1 receive request channel 1
DMA_SYSTEM_DREQ_38	MCSPI1_DREQ_TX2	MCSPI1 transmit request channel 2
DMA_SYSTEM_DREQ_39	MCSPI1_DREQ_RX2	MCSPI1 receive request channel 2
DMA_SYSTEM_DREQ_40	MCSPI1_DREQ_TX3	MCSPI1 transmit request channel 3
DMA_SYSTEM_DREQ_41	MCSPI1_DREQ_RX3	MCSPI1 receive request channel 3
DMA_SYSTEM_DREQ_42	MCSPI2_DREQ_TX0	MCSPI2 transmit request channel 0
DMA_SYSTEM_DREQ_43	MCSPI2_DREQ_RX0	MCSPI2 receive request channel 0
DMA_SYSTEM_DREQ_44	MCSPI2_DREQ_TX1	MCSPI2 transmit request channel 1
DMA_SYSTEM_DREQ_45	MCSPI2_DREQ_RX1	MCSPI2 receive request channel 1
DMA_SYSTEM_DREQ_46	MMC2_DREQ_TX	MMC2 transmit request
DMA_SYSTEM_DREQ_47	MMC2_DREQ_RX	MMC2 receive request
DMA_SYSTEM_DREQ_48	UART1_DREQ_TX	UART1 transmit request
DMA_SYSTEM_DREQ_49	UART1_DREQ_RX	UART1 receive request
DMA_SYSTEM_DREQ_50	UART2_DREQ_TX	UART2 transmit request
DMA_SYSTEM_DREQ_51	UART2_DREQ_RX	UART2 receive request
DMA_SYSTEM_DREQ_52	UART3_DREQ_TX	UART3 transmit request
DMA_SYSTEM_DREQ_53	UART3_DREQ_RX	UART3 receive request
DMA_SYSTEM_DREQ_54	UART4_DREQ_TX	UART4 transmit request
DMA_SYSTEM_DREQ_55	UART4_DREQ_RX	UART4 receive request
DMA_SYSTEM_DREQ_56	MMC4_DREQ_TX	MMC4 transmit request
DMA_SYSTEM_DREQ_57	MMC4_DREQ_RX	MMC4 receive request
DMA_SYSTEM_DREQ_58	MMC5_DREQ_TX	MMC5 transmit request
DMA_SYSTEM_DREQ_59	MMC5_DREQ_RX	MMC5 receive request
DMA_SYSTEM_DREQ_60	MMC1_DREQ_TX	MMC1 transmit request
DMA_SYSTEM_DREQ_61	MMC1_DREQ_RX	MMC1 receive request
DMA_SYSTEM_DREQ_62	UART5_DREQ_TX	UART5 transmit request
DMA_SYSTEM_DREQ_63	UART5_DREQ_RX	UART5 receive request
DMA_SYSTEM_DREQ_64	MCPDM_DREQ_UP_LINK	MCPDM uplink request
DMA_SYSTEM_DREQ_65	MCPDM_DREQ_DN_LINK	MCPDM downlink request
DMA_SYSTEM_DREQ_66	DMIC_DREQ	DMIC DMA request
DMA_SYSTEM_DREQ_67	Reserved	Reserved
DMA_SYSTEM_DREQ_68	Reserved	Reserved
DMA_SYSTEM_DREQ_69	MCSPI4_DREQ_TX0	MCSPI4 transmit request channel 0
DMA_SYSTEM_DREQ_70	MCSPI4_DREQ_RX0	MCSPI4 receive request channel 0
DMA_SYSTEM_DREQ_71	DSI1_A_DREQ_0	Display subsystem DSI1_A request 0
DMA_SYSTEM_DREQ_72	DSI1_A_DREQ_1	Display subsystem DSI1_A request 1
DMA_SYSTEM_DREQ_73	DSI1_A_DREQ_2	Display subsystem DSI1_A request 2
DMA_SYSTEM_DREQ_74	DSI1_A_DREQ_3	Display subsystem DSI1_A request 3
DMA_SYSTEM_DREQ_75	HDMI_DREQ	Display subsystem HDMI audio request
DMA_SYSTEM_DREQ_76	MMC3_DREQ_TX	MMC3 transmit request
DMA_SYSTEM_DREQ_77	MMC3_DREQ_RX	MMC3 receive request
DMA_SYSTEM_DREQ_78	UART6_DREQ_TX	UART6 transmit request
DMA_SYSTEM_DREQ_79	UART6_DREQ_RX	UART6 receive request
DMA_SYSTEM_DREQ_80	DSI1_C_DREQ_0	Display subsystem DSI1_C request 0
DMA_SYSTEM_DREQ_81	DSI1_C_DREQ_1	Display subsystem DSI1_C request 1
DMA_SYSTEM_DREQ_82	DSI1_C_DREQ_2	Display subsystem DSI1_C request 2

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Table 16-5. DMA_SYSTEM Controller Request Mapping (continued)

DMA Request Line	Source	Description
DMA_SYSTEM_DREQ_83	DSI1_C_DREQ_3	Display subsystem DSI1_C request 3
DMA_SYSTEM_DREQ_84	Reserved	Reserved
DMA_SYSTEM_DREQ_85	Reserved	Reserved
DMA_SYSTEM_DREQ_86	Reserved	Reserved
DMA_SYSTEM_DREQ_87	Reserved	Reserved
DMA_SYSTEM_DREQ_88	Reserved	Reserved
DMA_SYSTEM_DREQ_89	Reserved	Reserved
DMA_SYSTEM_DREQ_90	Reserved	Reserved
DMA_SYSTEM_DREQ_91	Reserved	Reserved
DMA_SYSTEM_DREQ_92	Reserved	Reserved
DMA_SYSTEM_DREQ_93	Reserved	Reserved
DMA_SYSTEM_DREQ_94	Reserved	Reserved
DMA_SYSTEM_DREQ_95	Reserved	Reserved
DMA_SYSTEM_DREQ_96	Reserved	Reserved
DMA_SYSTEM_DREQ_97	Reserved	Reserved
DMA_SYSTEM_DREQ_98	Reserved	Reserved
DMA_SYSTEM_DREQ_99	Reserved	Reserved
DMA_SYSTEM_DREQ_100	AESS_DREQ_FIFO0	Audio back-end (Audio engine) – request FIFO 0
DMA_SYSTEM_DREQ_101	AESS_DREQ_FIFO1	Audio back-end (Audio engine) – request FIFO 1
DMA_SYSTEM_DREQ_102	AESS_DREQ_FIFO2	Audio back-end (Audio engine) – request FIFO 2
DMA_SYSTEM_DREQ_103	AESS_DREQ_FIFO3	Audio back-end (Audio engine) – request FIFO 3
DMA_SYSTEM_DREQ_104	AESS_DREQ_FIFO4	Audio back-end (Audio engine) – request FIFO 4
DMA_SYSTEM_DREQ_105	AESS_DREQ_FIFO5	Audio back-end (Audio engine) – request FIFO 5
DMA_SYSTEM_DREQ_106	AESS_DREQ_FIFO6	Audio back-end (Audio engine) – request FIFO 6
DMA_SYSTEM_DREQ_107	AESS_DREQ_FIFO7	Audio back-end (Audio engine) – request FIFO 7
DMA_SYSTEM_DREQ_108	Reserved	Reserved
DMA_SYSTEM_DREQ_109	Reserved	Reserved
DMA_SYSTEM_DREQ_110	Reserved	Reserved
DMA_SYSTEM_DREQ_111	Reserved	Reserved
DMA_SYSTEM_DREQ_112	Reserved	Reserved
DMA_SYSTEM_DREQ_113	Reserved	Reserved
DMA_SYSTEM_DREQ_114	Reserved	Reserved
DMA_SYSTEM_DREQ_115	Reserved	Reserved
DMA_SYSTEM_DREQ_116	Reserved	Reserved
DMA_SYSTEM_DREQ_117	Reserved	Reserved
DMA_SYSTEM_DREQ_118	Reserved	Reserved
DMA_SYSTEM_DREQ_119	Reserved	Reserved
DMA_SYSTEM_DREQ_120	Reserved	Reserved
DMA_SYSTEM_DREQ_121	Reserved	Reserved
DMA_SYSTEM_DREQ_122	Reserved	Reserved
DMA_SYSTEM_DREQ_123	I2C4_DREQ_TX	I2C4 transmit request
DMA_SYSTEM_DREQ_124	I2C4_DREQ_RX	I2C4 receive request
DMA_SYSTEM_DREQ_125	ISS_DREQ_7	Imaging subsystem request 7
DMA_SYSTEM_DREQ_126	ISS_DREQ_8	Imaging subsystem request 8

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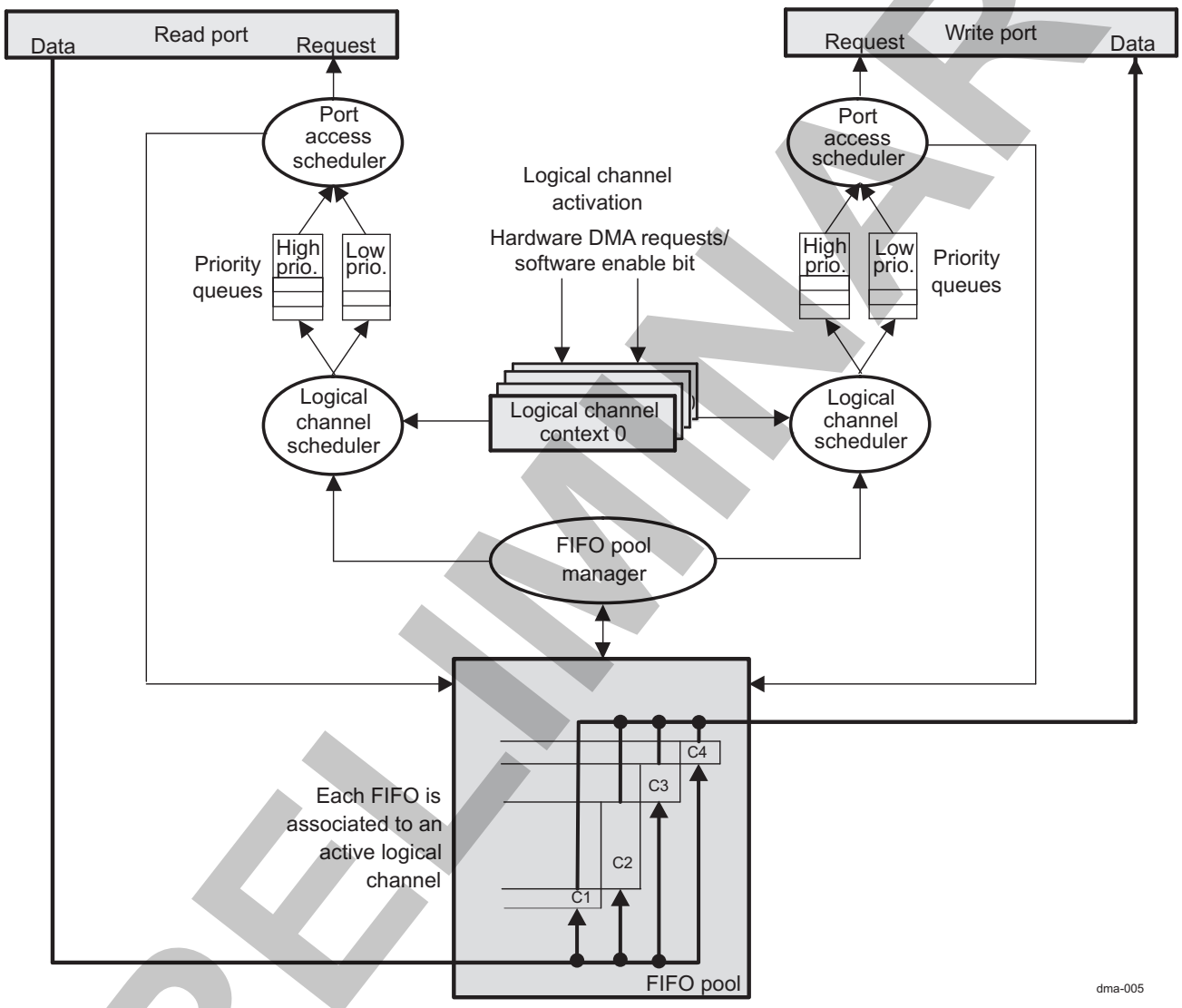
16.4 DMA_SYSTEM Functional Description

The DMA_SYSTEM module provides high-performance data transfers between memories and peripheral devices with low processor use. A DMA transfer is programmed through a logical DMA channel, which allows the transfer to be optimally tailored to the requirements of the application.

Figure 16-5 shows the DMA_SYSTEM controller top-level block diagram.

Figure 16-5. DMA_SYSTEM Controller Top-Level Block Diagram



16.4.1 DMA_SYSTEM Controller Power Management

Table 16-6 describes power-management features available for the DMA_SYSTEM controller.

NOTE:

- For information about source clock gating and sleep/wake-up transitions, see Section 3.1.1.1.2, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
- For a description of the EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

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Table 16-6. Local Power-Management Features

Feature	Registers	Description
Clock auto gating	DMA4_OCP_SYSCONFIG[0] AUTOIDLE bit	This bit allows local power optimization inside the module by gating the SDMA_ICLK clock upon the interface activity.
Slave idle modes	DMA4_OCP_SYSCONFIG[4:3] SIDLEMODE bit field	Force-idle, no-idle, and smart-idle modes are available.
Clock activity	DMA4_OCP_SYSCONFIG[9:8] CLOCKACTIVITY bit field	For configuration details, see Table 16-7.
Master standby modes	DMA4_OCP_SYSCONFIG[13:12] MIDLEMODE bit field	Force-standby, no-standby, and smart-standby modes are available.
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	N/A	Feature not available

Table 16-7. Clock Activity Settings

SDMA_CLOCKACTIVITY Values	Clock State When Module is in IDLE State	
	SDMA_ICLK	SDMA_FCLK
00	Off	Off
10	Off	On
01	On	Off
11	On	On

CAUTION

Because the PRCM module cannot read CLOCKACTIVITY settings through hardware, software must ensure consistent programming between the SDMA_CLOCKACTIVITY and DMA_SYSTEM clock PRCM control bits. For a description of the ClockActivity feature, see Section 3.1.1.1.2, *Module Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

16.4.2 DMA_SYSTEM Controller Interrupt Requests

DMA4 has four interrupt lines (Lj, where j = 0, 1, 2, 3). Each logical channel can request an interrupt over any line. The attachment of a channel interrupt event to one of these four external lines is programmable. Software determines whether it attaches a channel interrupt to a single IRQ line or to multiple IRQ lines.

There are two different registers per interrupt line:

- The DMA4_IRQSTATUS_Lj CH_31_0_Lj field shows the status of the different sources of interrupt. If the DMA4_IRQENABLE_Lj bit is 1, channel *i* is the source of interrupt in line *j*. In contrast to the DMA4_CSRi registers, the DMA4_IRQSTATUS_Lj registers are updated regardless of the corresponding bits in the DMA4_IRQENABLE_Lj registers.
- The DMA4_IRQENABLE_Lj CH_31_0_Lj_EN field masks/unmasks the channel interrupt. If the DMA4_IRQENABLE_Lj bit is set to 0, channel interrupt *i* of the line *j* is masked.

Each logical channel can generate a number of different interrupt events when enabled (that is, set to 1) in the DMA4_CICRi register. Each status bit is updated in the DMA4_CSRi register only when the corresponding enable bit is enabled in the DMA4_CICRi register.

To determine an interrupt source when an interrupt rises on an interrupt line L*j*:

- Identify the channel (LCH*i*) generating the interrupt.

  Read DMA4_IRQSTATUS_Lj.LCH*i* (LCH0 to LCH31). If LCH*i* = 1, channel *i* is the originator of the interrupt.
- Identify the interrupt event.

  Read the LCH*i* DMA4_CSRi. For example, if the drop event (the DMA4_CSRi[1] DROP bit) is 1, a

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request collision will occur.

The interrupt event status bit in the DMA4_CSRi register is immediately reset after it is written to 1.

The interrupt status bit in the DMA4_IRQSTATUS_Lj register is cleared after it is written to 1.

16.4.2.1 Interrupt Generation

The DMA_SYSTEM module has four interrupt request output lines, DMA_SYSTEM_IRQ_0 to DMA_SYSTEM_IRQ_3. One or more logical channels can be programmed to generate an interrupt request on any of these lines when any one of the maskable DMA events listed in Table 16-8 occurs.

Table 16-8. Logical DMA Channel Events

Event	Description
End of packet	A packet transfer completed.
End of block	A block transfer completed.
End of frame	A frame transfer completed.
End of super block	A super block transfer completed.
Half of frame	Half of the current frame transferred.
Start of last frame	The first element of the last frame transferred.
Transaction error	A transaction error is returned by the interconnect in either the read or write port.
Address error	An attempt was made to perform a DMA access to an address not aligned on an ES boundary. Condition to occur: if DMA4_CEN[23:0] CHANNEL_ELMNT_NBR = 0x000000 or DMA4_CFN[15:0] CHANNEL_FRAME_NBR = 0x0000 or DMA4_CSDP[1:0] DATA_TYPE = 0x3.
Supervisor transaction error	An error occurred, for example, when an unauthorized initiator (that is not a supervisor) tries to use a supervisor transfer.
Drain end	Drain is completed (DMA4_CCRi[10] WR_ACTIVE becomes 0).
Drop error	A drop event interrupt is generated when a DMA request is being serviced while a second one is asserted and a third one arrives before the second DMA request is serviced.

The logical DMA channels that generate an interrupt on a particular IRQ output are specified through the DMA4_IRQENABLE_Lj register (where *j* is the IRQ number: 0, 1, 2, or 3). The events that generate an interrupt for a particular channel can be configured through the channel DMA4_CICRi register.

When an interrupt is detected, the logical DMA channel generating the event can first be identified by reading the DMA4_IRQSTATUS_Lj register. The event causing the interrupt then can be identified by reading the interrupt status via the relevant DMA channel DMA4_CSRi register.

16.4.3 Logical Channel Transfer Overview

As Figure 16-5 shows, the DMA_SYSTEM module has one read port and one write port operating independently of one another. Buffering is provided between the read and write ports through a FIFO queue memory pool that is shared dynamically between the active logical channels.

- Logical channel synchronization

  A logical channel is described as hardware-synchronized when the DMA transfers are triggered by DMA requests from a hardware device. Alternatively, a logical channel is described as nonsynchronized when the DMA transfer is triggered by software.
- Logical channel activation

  A logical channel becomes active as follows:
  - For hardware-synchronized transfers, when the logical channel is enabled and the hardware DMA request line is asserted
  - For software-triggered (nonsynchronized) transfers, as soon as software enables the logical channel
- Logical channel transfer composition

  A DMA transfer is divided automatically into a number of transactions. Depending on the logical channel context configured, the transfer size, start address alignment, addressing mode, and

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configured maximum burst size, each transaction can be a single access or a burst of accesses.

- Logical channel scheduling

  When several logical channels are active at the same time, schedulers manage the read and write ports. The scheduling of logical channel transfers is similar for both read and write ports. When a logical channel becomes active, it is added to the tail of a scheduling queue. If more than one logical channel becomes active at the same time, the one with the lower number is queued first. This mechanism provides a first-come, first-serve scheduling scheme between the concurrently active logical channels.

  In addition, each read and write port has a high-priority queue and a low-priority queue. The priority bits (WRITE_PRIORITY and READ_ PRIORITY) in the logical channel DMA4_CCRi register determine whether a logical channel is queued as high or low priority. A software-configurable 8-bit priority counter gives weighting to the priority write queue. For every N (1 to 255) schedules from the priority write queue, one is scheduled from the regular write queue. A channel that is scheduled goes to the end of the queue after it completes its turn on the port. The relative weighting of the scheduling of the high-priority queue to the low priority queue is programmable from 1:1 to 1:256 through the DMA global channel register using the DMA4_GCR[23:16] ARBITRATION_RATE bit field.

  NOTE: The DMA4_GCR[23:16] ARBITRATION_RATE bit field does not depend on the DMA4_GCR[13:12] HI_THREAD_RESERVED bit field. The ARBITRATION_ RATE bit field depends on the DMA4_CCRi[26] WRITE_PRIORITY bit and the DMA4_CCRi[6] READ_PRIORITY bit.

- Read/write port access scheduling policy

  When either the read or write port becomes available, the port access scheduler selects the next logical channel for which to perform a DMA transaction from either the high- or low-priority queue.

  When the current DMA transaction (single or burst access) is complete and the full DMA transfer is not finished, the logical channel returns to the tail of the queue. Because the port access scheduling is on a per-transaction basis, a logical channel can be queued repeatedly this way several times during its block transfer.

The DMA_SYSTEM module can have up to four outstanding read transactions and two outstanding write transactions in the system interconnect; four read and two write thread IDs exist. For an arbitration cycle to occur, these two conditions must be met:

- At least one channel is requesting
- At least one free thread ID is available

On an arbitration cycle, the scheduler grants the highest priority channel that has an active request, allocates the thread ID, and tags this thread as busy. At a given time, a channel cannot be allocated for more than one thread ID.

NOTE: If more than one channel is active, each channel is given a thread ID for the current service only, not for the whole channel transfer.

When only one channel is enabled, only one thread is allocated for the channel. In such a situation the channel can have maximum of four outstanding commands (without getting the responses) without rescheduling the channel at the end of each transaction. Each command can be either single access (8-bit, 16-bit or 32-bit) or burst access (2 × M, 4 × M, 8 × M or 16 × M, where M can be 8, 16, or 32 bits).

When nonburst alignment is at the beginning of the transfer, the channel is rescheduled for each smaller access until burst-aligned. When the end of the transfer is not burst-aligned, the channel is rescheduled for each of the remaining smaller accesses.

For a logical channel transfer completion, when the last access is written to the destination, the logical channel becomes inactive. If enabled, an interrupt request is generated (see Section 16.4.2.1, *Interrupt Generation*).

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16.4.4 FIFO Queue Memory Pool

A FIFO queue memory pool provides buffering between the read and write ports. The hardware allocates the space dynamically to a number of FIFO queues, and each queue is associated with an active logical channel.

To avoid a memory pool overflow, if there are fewer entries in the FIFO queue memory pool than are required for the maximum configured source burst size of the next logical channel to be scheduled, the logical channel is returned to the tail of the queue, and the port access scheduler continues to search the queue until it finds a logical channel that can be scheduled.

The maximum FIFO depth that can be allocated to each individual logical channel can be limited globally through the DMA4_GCR[7:0] MAX_CHANNEL_FIFO_DEPTH bit field. This value should be configured to allow a fair allocation of the memory pool between the active channels.

A logical channel is scheduled if it has not yet reached its allocation limit, even if the access to be performed will exceed this limit. This means that the effective number of entries used by a particular logical channel is limited to the configured maximum entries per channel + channel maximum configured burst size (in words) 1.

16.4.5 Addressing Modes

A DMA transfer block consists of a number of frames (FN). Each frame consists of a number of elements (EN), and each element can have a size of 8, 16, or 32 bits (ES), as follows:

transfer block size = FN × EN × ES

The FN, EN, and ES are common for the source and destination. However, the way in which the data is represented (addressing profile/mode) is independently programmable for the source and destination devices, using one of these four addressing modes:

- Constant: The address remains the same for consecutive element accesses.
- Post-increment: The address increases by the ES, even across consecutive frames.
- Single-index: The address increases by the ES plus the element index (EI) value minus 1 (even across consecutive frames).
- Double-index: The address increases by the ES plus the EI value minus 1 within a frame. When a full frame is transferred, the address increases by the ES plus the frame index (FI) value minus 1.

The ES, EI, and FI values are expressed in bytes. The EI and FI values can be positive or negative.

When calculating the EI and FI values, it is critical to note that, after an element is accessed, the logical channel address pointer equals the address of the last byte (highest address) of the accessed element. The correct value for the EI or FI must be such that, when added to the logical channel address pointer, it results in the address of the first byte (lowest address) of the next element to be accessed.

The EI and FI values must be configured so that the address of each element in the transfer is aligned on an ES boundary.

Consequently, the single-index addressing mode with EI = 1 or double-index addressing mode with EI = 1 and FI = 1 is equivalent to post-increment addressing.

NOTE: The source and destination start addresses must also be aligned on an ES boundary.

When the address of an element to be accessed is not aligned on an ES boundary, the transfer is stopped and a misaligned address error interrupt occurs, if enabled (see Section 16.4.2.1, *Interrupt Generation*).

The DMA4_CFNi register configures the FN in a block.

The DMA4_CENi register configures the EN.

The DMA4_CSDPi register configures the ES.

The DMA4_CSSAi and DMA4_CDSAi registers configure the source and destination start addresses.

The DMA4_CCRi register configures the source and destination addressing modes.

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The DMA4_CSEIi, DMA4_CSFIi, DMA4_CDEIi, and DMA4_CDFIi registers configure the source EI, source FI, destination EI, and destination FI, respectively.

The addressing profiles are expressed as equations as follows:

Equation 1. Constant addressing:

$$A(n + 1) = A(n)$$

NOTE: Constant addressing mode with DMA4 to/from DDR memory is not supported on the device. To fill the DDR memory with a single value, the constant fill feature of the DMA4 must be used, instead of a constant-addressing mode transfer.

Equation 2. Post-increment addressing:

$$A(n + 1) = A(n) + ES$$

Equation 3. Single-indexed addressing:

$$A(n + 1) = A(n) + ES + (EI\ 1)$$

Equation 4. Double-indexed addressing:

When not at the end of a frame or transfer (that is, when the element counter ≠ 0):

$$A(n + 1) = A(n) + ES + (EI\ 1)$$

When at the end of a frame but not at the end of the transfer (that is, when the element counter = 0 and the frame counter ≠ 0):

$$A(n + 1) = A(n) + ES + (FI\ 1)$$

Calculate the element and frame index as follows:

Equation 5. EIement index

$$EI = [(Stride\ EI\ 1) * ES] + 1$$

Equation 6. Frame index

$$FI = [(Stride\ FI\ 1) * ES] + 1$$

where:

A(n): Byte address of the element *n* within the transfer.

ES is in bytes, ES{1, 2, 4}.

EI is in bytes, specified in a configuration register, 32768 EI 32767.

Stride EI: The difference in the number of elements between the start of the current element *n* to the start of next element, *n+1*.

Element counter: A counter that is (re)initiated with the number of elements per frame or per transfer. Decreased by 1 for each element transferred. The initial value is configured in the register DMA channel element number, DMA4_CENi.

FI is in bytes, specified in a configuration register, 2147483648 FI 2147483647.

Stride FI: The difference in the number of elements between the start of the last element of the current frame and the beginning of the first element of the next frame.

Frame counter: A counter that is (re)initiated with the FN per transfer. Decreased by 1 for each frame transferred. The initial value is configured in the register DMA channel frame number, DMA4_CFNi.

Figure 16-6 shows how a stride EI and FI are defined. When handling complex configurations, using strides can make it easier to calculate EI and FI because you can calculate in elements instead of bytes. (This approach is used in the 90-degree clockwise image rotation example shown in Figure 16-10.) The double-index addressing example shown in Figure 16-6 uses ES = 4, EN = 2, EI = 5, FI = 5, and FN = 2.

Figure 16-6 through Figure 16-9 show examples of addressing mode configurations. Table 16-9 lists parameter values for the examples.

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Figure 16-6. Example Showing Double-Index Addressing, Elements, Frames, and Strides

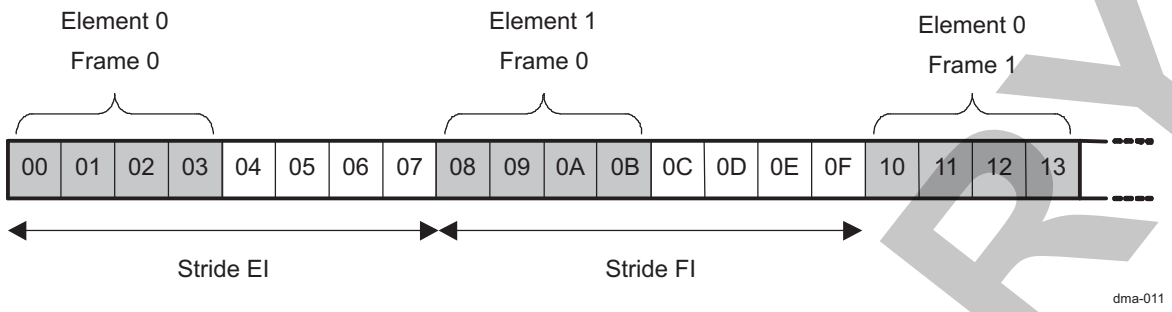

Figure 16-7. Addressing Mode Example (a)

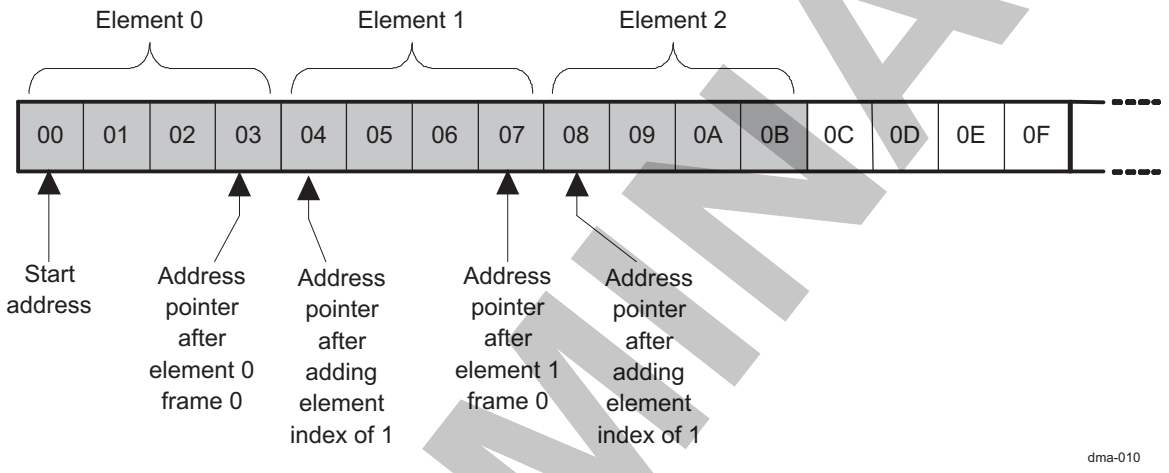

Figure 16-8. Addressing Mode Example (b)

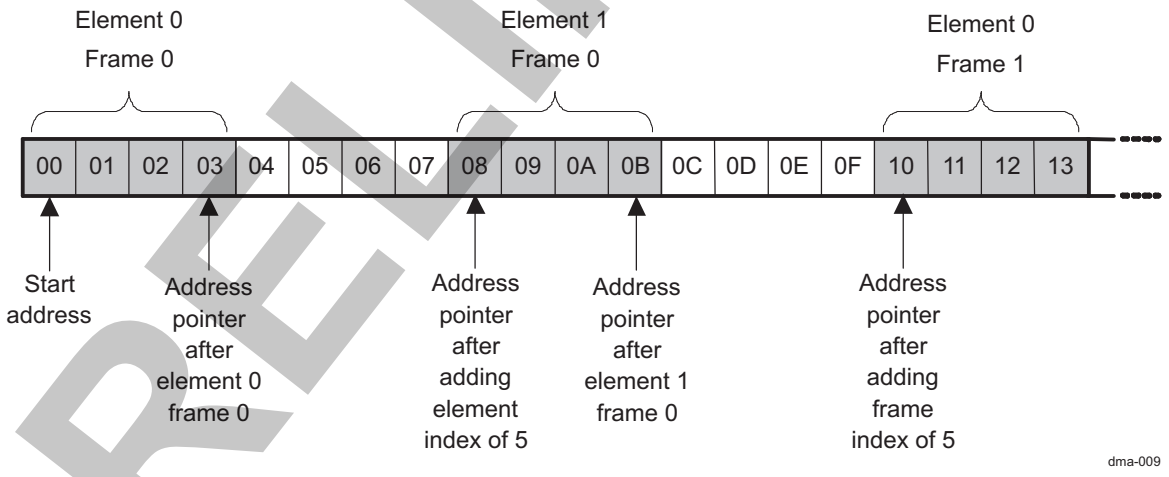

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Figure 16-9. Addressing Mode Example (c)

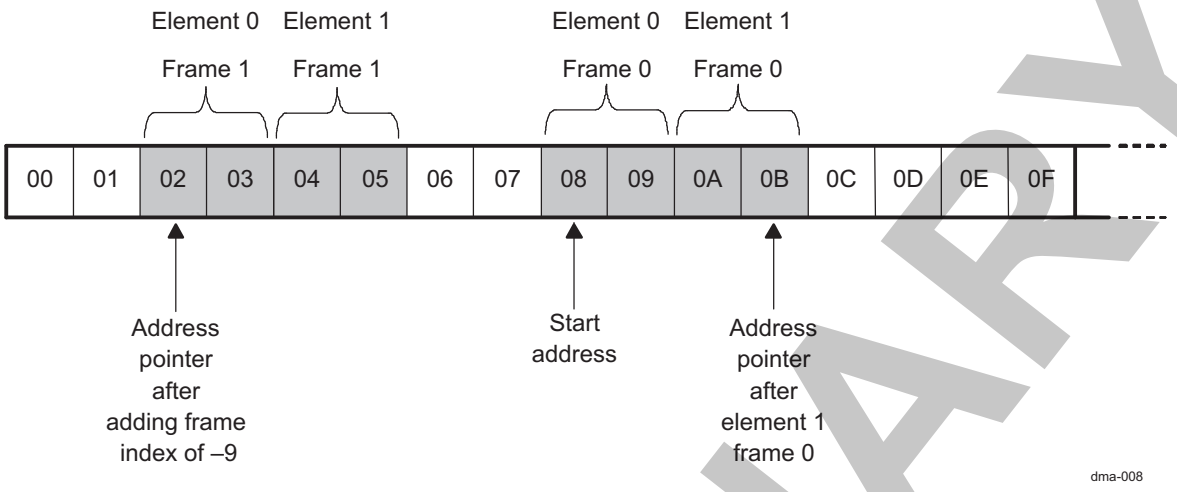

Table 16-9. Parameter Values for Addressing Mode Examples (a), (b), and (c)

Parameter	Example (a)	Example (b)	Example (c)
Addressing mode	Single index (or post-increment)	Double index	Double index
Start address	0	0	8
ES	4 (32-bit)	4 (32-bit)	2 (16-bit)
EN	3	2	2
EI	1	5	1
FN	1	2	2
Frame index	N/A	5	-9

Double indexing can occur on source (read) or destination (write). Equations for rotation of xx degrees on destination are obtained by taking equations for rotation of (360 – xx) degrees on source, and swapping the width (x) and height (y) of the image in them. The opposite is also true. Table 16-10 lists the equations for 90-, 180-, and 270-degree rotations.

Table 16-10. Equations for Rotation

		90° Rotation	180° Rotation	270° Rotation
Double indexing on destination (write)	Base address	ES*(y–1)	ES*(x*y–1)	ES*y*(x–1)
	EI	ES*(y–1) + 1	1–2*ES	1–ES*(y + 1)
	FI	1 ES*[(x–1)*y + 2]	1–2*ES	1+ES*(x–1)*y
Double indexing on source (read)	Base address	ES*x*(y–1)	ES*(x*y–1)	ES*(x–1)
	EI	1–ES*(x + 1)	1–2*ES	ES*(x–1) + 1
	FI	1+ES*(y–1)*x	1–2*ES	1 ES*[(y–1)*x + 2]

Table 16-11 and Figure 16-10 show the configuration required to perform a 90-degree clockwise rotation of a 240 × 160 pixel, 32-bit image. The EI, frame size, and FI values are configured so that the image is rotated line-by-line starting at the left end of the top line.

NOTE: The FI value for the destination is negative so that the first pixel of each subsequent line of the source image is written to the correct location at the destination.

Equation 5 and Equation 6 calculate the destination, FI and EI. The example assumes that the image lines are stored at consecutive addresses in memory, meaning that both EI and FI on the source side are 1.

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Rotations:

Section 16.5.7, *90-Degree Clockwise Image Rotation*, describes how to program an example of a 90-degree clockwise image rotation.

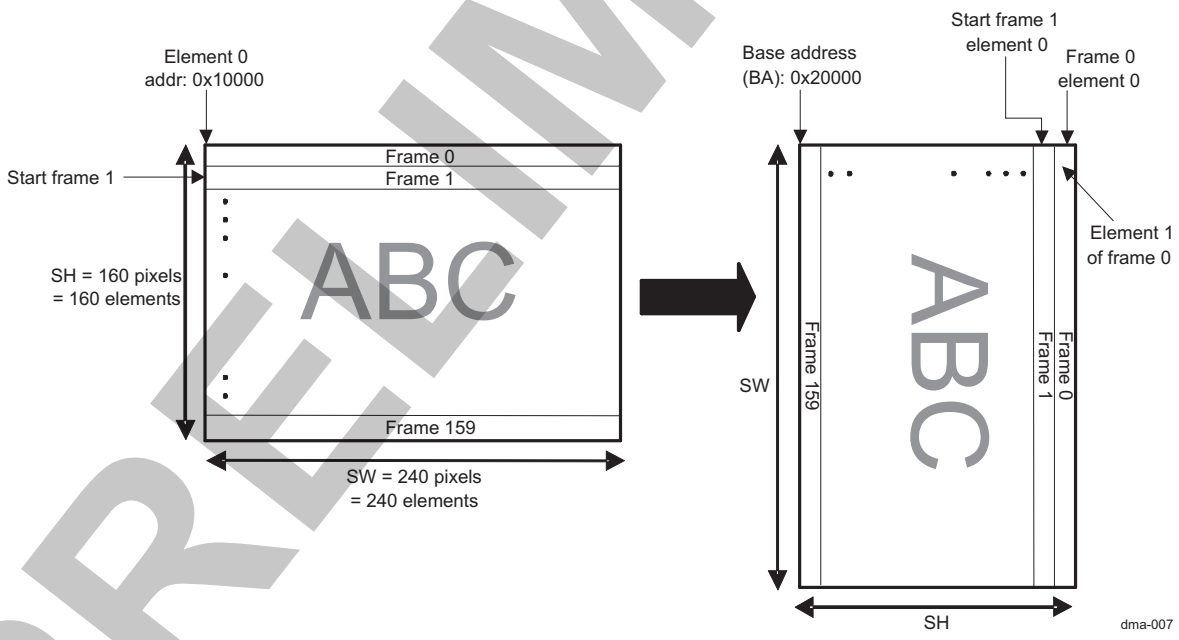
Observe that:

- One pixel = one element
- One line = one DMA frame
- Pixel size = element size = ES

Table 16-11. Example Parameter Values for a 90-Degree Clockwise Image Rotation

Parameter	Source Value	Destination Value
Bits per pixel	32	32
ES	4	4
Image width	SW	SH
Image height	SH	SW
Stride elements (stride EI)	1 element	SH
Stride frames (stride FI)	1 element	–[(SW-1)*SH + 1] = 38,241 elements
Start address	0x100000	0x200000 + (SH 1) x ES = 0x20027C
EN	SW	SW
EI	[(Stride EI 1) * ES] + 1 = 1	[(Stride EI 1) * ES] + 1 = 637
FN	SH	SH
FI	[(Stride FI 1) * ES] + 1= 1	[(Stride FI 1) * ES] + 1 = 152,967

Figure 16-10. Example of a 90-Degree Clockwise Image Rotation



16.4.6 Packed Accesses

To pack data means to group data to match the bus size, thus optimizing a transfer. When the logical channel ES is less than the DMA module read/write port size, and the addressing profile supports it (post-increment mode or single- or double-index mode with EI = 1), the number of elements to transfer in each read/write port access can be maximized by specifying that the source or destination is packed through the channel DMA4_CSDPi register. Thus:

- For a read/write port size of 32 bits, the source or destination can be configured as packed for transfer ESs of 8 bits (four elements per access) and 16 bits (two elements per access).

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- For a read/write port size of 64 bits, the source or destination can be configured as packed for transfer ESs of 8 bits (eight elements per access), 16 bits (four elements per access), and 32 bits (two elements per access).

Depending on the start address and transfer length, the first or last packed access can be only partially filled. This is indicated to the source or destination using the byte-enable signals.

16.4.7 Burst Transactions

Transfer performance can be improved so that the source or destination and addressing profile supports it. This can be achieved by configuring the logical channel to perform burst transactions consisting of multiple instead of single accesses. The channel can be programmed to use burst sizes equal to 16, 32, or 64 bytes through the DMA4_CSDPi register, with the read burst size programmable independently of the write burst size. Typically, the optimal burst size is 64 bytes (16 accesses for a 32-bit read/write port size or 8 accesses for a 64-bit read/write port size).

To obtain the maximum benefit from burst transactions, the source and destination start addresses must be aligned with the burst size. If this is not the case, the start of the transfer can consist of a number of smaller (single or burst) transactions until the first burst size boundary is reached.

Similarly, if the end of the transfer is not aligned on a burst size boundary, the final part of the transfer can consist of a number of smaller transactions.

NOTE: If post-incrementing is used, data must be packed to DMA data-port width, to use burst.

16.4.8 Endianism Conversion

The source and destination are each specified as little-endian or big-endian through the DMA4_CSDPi register for the particular logical channel. If the endianism of the source and destination differ, and if the logical channel ES is less than the DMA_SYSTEM module read/write port size, an endianism conversion is applied to the data before it is written to the destination.

When transferring data between a source and a destination with different endianism, it is important to specify an ES that equals the type of data being transferred to preserve the correct data image at the destination.

In the system, endianism conversion can be performed in more than one place. It is possible to instruct the source and/or destination to lock the endianism (that is, to not perform a conversion) through the logical DMA channel DMA4_CSDPi register.

NOTE: Because the device is little-endian by construction, the DMA_SYSTEM endianism registers must never be set to big-endian.

If DMA_SYSTEM is used to execute endian conversion by setting the source and destination to different endianism values, it is important to consider that the L3_MAIN interconnect also executes endian conversion if the DMA_SYSTEM and the source or destination have a different data bus width.

16.4.9 Transfer Synchronization

A logical channel can be programmed for software-triggered or hardware synchronized transfers.

16.4.9.1 Software Synchronization

A transfer is software-triggered when the logical channel is set up and started by software. To specify a software-triggered transfer, set the channel DMA DMA4_CCRi[4:0] and DMA4_CCRi[20:19] bit fields to 0. The transfer starts as soon as the DMA DMA4_CCRi[7] bit is set (when it enters the scheduling process).

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16.4.9.2 Hardware Synchronization

A transfer is hardware-synchronized if the logical channel activation is driven by hardware requests from the source or destination target. A hardware-synchronized transfer is specified by configuring the DMA request line number in the channel DMA4_CCRi register to a value that corresponds to the DMA request line from the source or destination that generates the DMA requests. The DMA request numbers to be configured are specified in the DMA request mapping (see Table 16-8).

Specify the DMA request number in the DMA4_CCRi[4:0] SYNCHRO_CONTROL and DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER bit fields. After the DMA4_CCRi[7] ENABLE bit is set, the logical channel becomes enabled but not activated (it does not enter the scheduling process), which means that channel registers are not updated until the first DMA request is received.

NOTE: The channel synchronization control registers are 1-based. For example, to enable the S_DMA_1 request, the DMA4_CCRi[4:0] SYNCHRO_CONTROL bit field must be set to 0x2 (DMA request number + 1).

NOTE: A DMA request line must not be shared between concurrently enabled DMA channels. However, a DMA request line can be shared among several chained logical channels.

For hardware synchronization, the amount of data to be transferred for each assertion of the DMA request line is configured through the frame synchronization (FS) and block synchronization (BS) bits in the logical channel DMA4_CCRi register and the DMA4_CCRi[5] FS and DMA4_CCRi[18] BS bits, respectively.

The amount of data can be any of the following:

- A single element transfer: A complete element defined by data type. For example, 8/16/32 bits are transferred in response to a DMA request.
- A full frame: A complete frame of several elements is transferred in response to a DMA request.
- A full block (a full channel transfer): A complete block of several frames is transferred in response to a DMA request.
- A full packet (a full channel transfer): A complete packet of several elements is transferred in response to a DMA request.

Packets allow the size of each part of the full DMA transfer to be configured independently of the organization of the data to be transferred (typically a number of elements). This can be useful when the source or destination has a buffer (such as a FIFO queue) with a size unrelated to the frame size of the transfer. The packet size then can be set to the size of the buffer.

Packet transfer must be used only where the source or destination is addressed in constant addressing mode, because FI registers are reused to specify the packet size.

To support the burst mode, the logical channel must also be configured in target-port packed access mode.

The packet size is configured based on the DMA4_CCRi[24] SEL_SRC_DST_SYNC bit through either the channel DMA4_CDFIi register (source synchronized) or the DMA4_CSFIi register (destination synchronized).

When the logical channel transfer block is not an exact multiple of the packet size, the final packet consists of the remaining elements in the transfer, using burst or single accesses to complete the block transfer.

The maximum transfer size, regardless of the packet size, is always as follows:

Block_size = Number_of_Frame_in_Block * Number_of_Element_in_Frame * Element_Size

- Synchronized at the source

  The DMA module optimizes the transfer with respect to the number and size of burst transactions for the given source and destination addressing profiles and configured maximum burst sizes. When writing to the destination is slower than reading from the source, data is buffered in the channel FIFO queue. If the transfer is packet-synchronized at the source, the end-of-packet interrupt is disabled (see Section 16.4.13, *Reprogramming an Active Channel*).

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For a source synchronized transfer, buffering can be enabled or disabled by setting the DMA4_CCRi[25] BUFFERING_DISABLE bit. For a packet source synchronization with buffering disabled and the packed/burst across the packet boundary, the last packed/burst write transaction is split in optimized smaller accesses to complete the packet transfer size. However, for a packet source synchronized transfer with buffering enabled and with the packed/burst across the packet boundary, the DMA module waits for the next DMA request(s) to read enough data to issue an atomic packed/burst write transaction (assuming that the address is packed/burst aligned).

NOTE: Buffering is not performed between frames, even if it is enabled. If the packed/burst is across the frame boundary, the last packed/burst write transaction is split in optimized smaller accesses to complete the frame transfer size.

- Synchronized at the destination

  The performance of a hardware-synchronized transfer can be improved by using the prefetch mode, enabled through the channel DMA4_CCRi[23] PREFETCH bit. Data is prefetched on the read port side before the DMA request received and buffered in the FIFO queue. Up to a full transfer block can be prefetched, although this can be limited by the specified maximum channel FIFO queue depth (see Section 16.4.4, *FIFO Queue Memory Pool*).

  Buffering disable is not allowed for a destination-synchronized transfer.

NOTE: Behavior is undefined when prefetch is enabled and a transfer is synchronized to the source.

Regardless of whether buffering is enabled, the last transaction in the frame or in the block is write nonposted (WNP) even if the write mode is specified as write last nonposted (WLNP; the DMA4_CSDPi[17:16] WRITE_MODE bit field = 0x2). However, in a packet synchronization mode, the last transaction of each packet in the transfer is WNP only if the buffering disable is on (even if the write mode is specified as WLNP).

Regardless of whether buffering is enabled, the packet interrupt is not generated in the packet source synchronized mode.

CAUTION

The DMA4_CCRi[25] BUFFERING_DISABLE bit must be filled with an allowed value, as specified in Table 16-12.

Table 16-12. Buffering Disable

	BUFFERING_DISABLE (0: Buffering enable, 1: Buffering disable)	
Destination synchronized	0	Allowed
	1	Not allowed
Source synchronized	0	Allowed
	1	Allowed

- Synchronized transfer monitoring using CDAC (DMA4_CDACi):

  Context is restored only when the channel becomes active on a DMA request (not at software enable). The channel is software-enabled first, and then a DMA request is asserted followed by the first context restore.

  The CDAC register is writable; thus, the CDAC can be initialized to monitor the transfer and determine whether the transfer is started (for more information, see Section 16.5.4, *Synchronized Transfer Monitoring Using CDAC*).

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NOTE: For 16-bit transactions, start reading from or writing to the LSByte first to enable the register update. This is not an issue for 32-bit read-write transactions.

16.4.10 Thread Budget Allocation

When several concurrent channels are latency critical and hardware synchronized, a specific latency cannot be ensured until the target is served. This situation occurs when the number of concurrent channels is greater than the number of available threads.

NOTE: Four threads are available on the read port, and two threads are available on the write port.

For a hardware-synchronized transfer (memory to peripheral), a minimum bandwidth for a latency-critical transfer must be ensured to avoid collisions between two hardware requests.

Because it is latency critical, the software user is responsible for the following:

- Programming the synchronized channel as a high-priority channel
- Reserving one or several threads for high-priority channels

The proposed implementation is as follows (see Section 16.5.5, *Concurrent Software and Hardware Synchronization*):

Prevent the regular channel queue from exceeding more than a programmable (3, 2, or 1) number of threads on the read port and no more than one thread on the write port. This number can be set in the global register DMA4_GCR[13:12] .

The thread reservation is programmable for maximum use of thread resources for concurrent, low-priority channel transfer. Programmability can also allow a partial throughput control by limiting in software the number of concurrent outstanding requests that break the pipelining.

Depending on the DMA4_GCR [13:12] value, the following threadID on the read/write ports are allocated for a high-priority channel:

Read port priority thread reservation:

- DMA4_GCR[13:12] = 0x0 => No ThreadID is reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x1 => Read ThreadID 0 is reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x2 => Read ThreadID 0 and Read ThreadID 1 are reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x3 => Read ThreadID 0, Read ThreadID 1, and Read ThreadID 2 are reserved for high-priority channels.

Write port priority thread reservation:

- DMA4_GCR[13:12] = 0x0 => No ThreadID is reserved for high-priority channels
- DMA4_GCR[13:12] = 0x1 => Write ThreadID 0 is reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x2 => Write ThreadID 0 is reserved for high-priority channels.
- DMA4_GCR[13:12] = 0x3 => Write ThreadID 0 is reserved for high-priority channels.

Regardless of whether the enabled channels are high priority, only the setting of the DMA4_GCR[13:12] value forces the thread reservation to these values. Set the appropriate value to avoid losing threads using only regular channels.

To have an independent read and write priority context, a per-channel bit (DMA4_CCRi[26]) is added for write priority, and the previous priority bit becomes read priority bit (DMA4_CCRi[6]).

NOTE: The device has one priority bit per logical channel, not one priority bit per port.

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16.4.11 FIFO Budget Allocation

To avoid fully occupying the FIFO with a high-priority transfer while low-priority channels wait in the arbitration queue, two separate FIFO budgets are specified: one for high-priority channels and one for low-priority channels. This is defined in the DMA4_GCR register, allowing the user to share the FIFO budget between the low- and high-priority channels. The amount of the FIFO allocated by the low- and high-priority channels is fixed by the value set in the DMA4_GCR[15:14] HI_LO_FIFO_BUDGET field. The maximum channel FIFO depth is limited by the HI_LO_FIFO_BUDGET field as follows:

If the channel is low priority:

- When HI_LO_FIFO_BUDGET = 0x1, then low priority cannot exceed 75 percent of the total FIFO.
- When HI_LO_FIFO_BUDGET = 0x2, then low priority cannot exceed 25 percent of the total FIFO.
- When HI_LO_FIFO_BUDGET = 0x3, then low priority cannot exceed 50 percent of the total FIFO.

If channel is high priority

- When HI_LO_FIFO_BUDGET = 0x1, then high priority cannot exceed 25 percent of the total FIFO.
- When HI_LO_FIFO_BUDGET = 0x2, then high priority cannot exceed 75 percent of the total FIFO.
- When HI_LO_FIFO_BUDGET = 0x3, then high priority cannot exceed 50 percent of the total FIFO.

The user must perform the following equation:

- For a high-priority channel: (Per_Channel_Maximum FIFO Depth + 1) x Number of High Channel =< High Budget FIFO
- For a low-priority channel: (Per_Channel_Maximum FIFO Depth + 1) x Number of Low Channel =< Low Budget FIFO

NOTE: Ensure that *Number of High Channel* means *Number of Active High-Priority Channel* and that *Number of Low Channel* means *Number of Active Low-Priority Channel*.

16.4.12 Chained Logical Channel Transfers

Chaining multiple logical channels permits transfers consisting of multiple parts to be executed without repeated software intervention. This results in better performance than the alternative of software setting up and starting each transfer separately. Each part of a chained transfer can have the data addressed in a different manner that permits the programming of a variety of complex transfers. For example:

- Interlaced video data with one logical channel configured to transfer the even lines and another logical channel configured to transfer the odd lines
- Protocol headers with a separate DMA4 channel configured to transfer each field in the header

Channels can be chained through each channel DMA4_CLNK_CTRLi register. When the transfer for the first channel completes, the next channel in the chain is enabled. The number of channels in the chain that are configured for hardware-synchronized transfers is flexible (although typically it may be all, none, or simply the first one). The DMA request line number must be set to 0 to specify that any or all of the channels in a chain are software-triggered or nonsynchronized.

The last channel in a chain can be chained to the first channel to create a continuously looping chain. The continuously looping transfer can be stopped on the fly at a specific channel by disabling the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit. The looping transfer stops after the specified channel transfer is complete.

NOTE: A DMA request line must not be shared between concurrently enabled DMA channels. However, a DMA request line can be shared between several chained logical channels.

For more information about the programming model, see Section 16.5, *DMA_SYSTEM Basic Programming Model*.

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16.4.13 Reprogramming an Active Channel

A currently active logical DMA channel can be disabled through the DMA4_CCRi[7] ENABLE bit. When an ongoing transaction is complete and the read-active and write-active bits in the DMA4_CCRi register (DMA4_CCRi[9] RD_ACTIVE and DMA4_CCRi[10] WR_ACTIVE) are reset, the channel can be reprogrammed for a new transfer.

16.4.14 Packet Synchronization

A packet transfer notion is related to the behavior of some peripherals, which have certain buffering capability and requires to transfer the buffer content once an element number threshold is reached (a hardware DMA request is generated). To associate a frame synchronization to each DMA request is possible, but this limits the maximum transfer size. Indeed the maximum transfer size is proportional to the FIFO depth of the peripheral:

maximum_transfer_size =peripheral_FIFO_depth x number_of_frame_in_block

The packet synchronization allows to dissociate the transfer size from the FIFO depth of the peripheral. Only Constant addressing mode is allowed on a read port or a write port if source target or destination target is packet synchronized respectively.

Example:

Consider a camera interface with a FIFO_depth of 128 words and a FIFO_element_number_threshold of 128, and a picture to transfer with a size 320 lines by 240 columns. If frame synchronization is associated with each DMA request then the maximum transfer size that can be performed is $128x2^{16}$ words. In this case, a frame is 128-word long, which does not fit the size of a line, and it is not possible to generate an interrupt at the end of line. However, by introducing the packet transfer notion, which is related to the peripheral FIFO behavior/structure, the maximum transfer size (maximum_transfer_size = 2^{24} x 2^{16} words) is independent of both peripheral_FIFO_depth and FIFO_element_number_threshold. This allows a long-enough transfer within one channel context and rotation operation on a large image format.

The main features of DMA Packet transfer are as follows:

- DMA Packet_Data_Size for each DMA Request: The Peripheral_element_number_threshold (the number of elements in a packet) shares the DMA4_CSFIi and DMA4_CDFIi configuration registers. If the peripheral is the source target, the addressing mode is constant, and the DMA4_CSFIi[15:0] bit field is used to specify the packet data size in the DMA4_CSFIi register. The user must set the DMA.SDMA4_CCRi[24] SEL_SRC_DST_SYNC bit to 1. If the peripheral is the destination target, the addressing mode is constant, the DMA4_CDFIi[15:0], is used to specify the packet data size (PKT_ELNT_NBR), and the bit field [31:16] is unused. To specify the packet data size in the DMA4_CDFIi register, the user must set the DMA4_CCRi[24] SEL_SRC_DST_SYNC bit to 0.

  NOTE: The packet size can be a submultiple or non-submultiple of a frame size. If DMA Packet_Data_Size is aligned on the DMA channel block data size boundary, then DMA transfers the last data in the channel block boundary and stops at the block boundary for the last packet DMA Request. If the Packet_Data_size is not aligned on the block boundary, the remaining data smaller than a packet size are transferred using burst or single accesses to complete the block.

- DMA Packet_Data_Transfer does not affect DMA channel capabilities in term of packing and bursting.

  The packet synchronization mode is active when DMA4_CCRi[5] FS = DMA4_CCRi[18] BS = 1. Then:

  – If DMA4_CCRi[24] SEL_SRC_DST_SYNC = 0, the DMA4_CDFIi[15:0] bit field gives the number of elements in the packet and the DMA4_CDFIi[31:16] bit field is unused for the packet size.

  – If DMA4_CCRi[24] SEL_SRC_DST_SYNC = 1, the DMA4_CSFIi[15:0] bit field gives the number of element in the packet and the DMA4_CSFIi[31:16] bit field is unused for the packet size.

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NOTE: The maximum transfer size, regardless of the packet size, is always:

Block_size = Number_of_Frame_in_Block x Number_of_Element_in_Frame x Element_Size.

If DMA channel packet/burst access is across the packet boundary, the DMA hardware automatically splits this packing/burst access into multiple smaller accesses that are aligned on the packet boundary. Otherwise, the DMA transfers data as a usual packing/burst access.

16.4.15 Graphics Acceleration Support

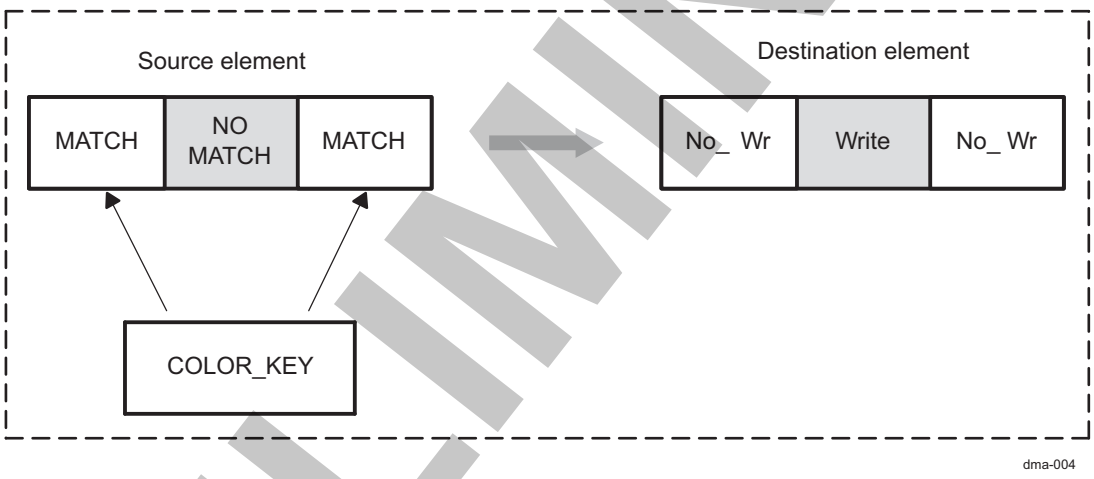
The DMA_SYSTEM supports two graphic acceleration features: transparent copy and constant fill.

Only one of these features can be enabled at a time through the DMA4_CCRi register for the particular logical DMA channel.

The transparent copy feature enables specification of a particular color through the DMA4_COLORi register so that when it is recognized in the data from the source, it is not copied to the corresponding location in the destination but instead leaves the data in the corresponding location in the destination as it is.

Figure 16-11 shows the 2-D graphic transparent color block diagram.

Figure 16-11. 2-D Graphic Transparent Color Block Diagram



The constant fill feature provides the ability to specify a particular color through the DMA4_COLORi register for every specified location in the destination. In this case, the transfer consists only of writing to the destination without reading from a source.

Both features support 8, 16, and 24 bpp, depending on what is specified as the DMA transfer ES through the DMA4_CSDPi register. An ES of 32 bits corresponds to 24 bpp. During a 32-bit (24 bpp) transfer, the 8 most-significant bits (MSBs) ([31:24]) are 0. Both features are compatible with packed and burst transactions.

16.4.16 Supervisor Modes

A logical DMA channel can be configured to operate in supervisor mode through the DMA4_CCRi[22] SUPERVISOR bit. This must be done using supervisor access. Once a channel is configured in supervisor mode, the channel configuration is protected from nonsupervisor accesses. All DMA transactions on a supervisor channel are supervisor transactions.

16.4.17 Posted and Nonposted Writes

A logical channel can be configured in its DMA4_CSDPi[17:16] bits to use one of three write access handshake modes for the destination:

- Nonposted write: Each write must complete before transfer can continue or complete.

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- Posted write: Transfer continues without waiting for each write to complete (may improve performance with slow devices).
- Posted with final write nonposted: Transfer continues without waiting for each write to complete, but final write completes before transfer can complete.

16.4.18 Disabling a Channel During Transfer

When a channel is disabled during a transfer, the channel undergoes an abort, unless it is hardware-source-synchronized with buffering enabled (DMA4_CCRi[25] BUFFERING_DISABLE = 0). If this is the case, the FIFO is drained to prevent the loss of data. For more information about this feature, see Section 16.4.19, *FIFO Draining Mechanism*.

16.4.19 FIFO Draining Mechanism

When a source-synchronized channel is disabled during a transfer, the current hardware request (element/packet/frame/block) service completes and the channel DMA4_CCRi[9] RD_ACTIVE bit is set to 0, which means the channel is not active on the read port. The remaining data in the corresponding disabled channel FIFO is drained onto the write port and transferred to the programmed destination as in normal transfer.

At the end of the draining the DMA4_CCRi[10] WR_ACTIVE bit is set to 0 (channel is no longer active on the write port) and if the DMA4_CICRi[12] DRAIN_END_IE is set to 1, the DMA4_CSRi[12] DRAIN_END status bit is updated and an interrupt is generated.

Once a channel is disabled during a transfer, it must wait for the DMA4_CCRi[9] RD_ACTIVE and DMA4_CCRi[10] WR_ACTIVE bits to become 0 before being reenabled for a new transfer. The FIFO drain for a channel occurs only in the following cases:

- If the channel is a source synchronized channel and DMA4_CCRi[25] BUFFERING_DISABLE = 0 and
- If the channel is not a solid fill channel and
- If the channel is not a transparent and copy channel and
- If the channel is a hardware, synchronized channel

NOTE: For a self-linked or chain-linked channel, the user must disable the DMA4_CLNK_CTRLi[15] ENABLE_LINK bit before disabling the channel.

In all other cases, the channel undergoes an abort.

16.4.20 Linked List

16.4.20.1 Overview

The DMA_SYSTEM supports the logical transfer-descriptor loader feature. A transfer descriptor represents a set of values that maps to a set of logical channel configuration registers.

A logical channel transfer descriptor can be loaded by DMA from memories, and then successive transfer descriptors can be autonomously loaded based on a linked-list scheme. This enables DMA4 scatter-gather transfers with minimum MPU support by removing successive channel configuration processing and associated interrupt handling overheads. It also optimizes DMA4 channel resources by enabling efficient transfer serialization on a single logical channel versus concurrent (multiple) logical channel use.

Different types of transfer descriptors are supported (full or partial logical channel configuration registers are set). This optimizes the memory size required for storing a long linked list, because parameter changes are limited to only a few logical channel configuration registers.

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16.4.20.2 Link-List Transfer Profile

A linked-list transfer can be seen as a super-block transfer (where the block is composed of FN frames and each frame includes EN elements). The block size (FN x EN x ES) can be changed in the linked list by loading an updated transfer descriptor.

The end of the super block is signaled in the last descriptor associated with the last block. Generally, for a given link-list transfer, the logical channel is set at the beginning of the transfer and the logical channel configurations for the subsequent blocks are slightly changed. Thus, the descriptor can be limited to an update of only few parameters, such as FN or EN. This assumes that the content of unmodified registers is preserved when a new descriptor is loaded.

A transfer descriptor is composed of a set of channel configuration register values with the addition of the next-descriptor pointer register (DMA4_CNDPi) and a channel-descriptor parameter register (DMA4_CDPi) . The next-descriptor pointer is the 32-bit address pointer from where the next transfer descriptor is to be loaded. The next-descriptor pointer is mapped depending on the descriptor type (1, 2, or 3).

16.4.20.3 Descriptors

A transfer descriptor is a set of values that maps to a set of logical channel configuration registers. The descriptor contains the parameters associated with a transfer profile (transfer size, source or destination addresses, etc). Four different types of transfer descriptors are supported to optimize the memory size required to store a long linked list and to minimize MPU use to create and maintain the descriptor list.

A transfer descriptor is a list of 32-bit values. A descriptor must be 32-bit aligned in memory. Only the 30 least-significant bits (LSBs) of the next-descriptor address pointer are updated from the descriptor, and the DMA4 forces the 2 LSBs to 0 on generation of the pointer address. The descriptor size is variable, depending on the descriptor type and the Nxt_Dv and Nxt_Sv bit fields.

Transfer descriptor bit mapping is the same as DMA4 logical-channel configuration register bit mapping, with the following exceptions:

- Src_Element_index and Dst_Element_index are concatenated in the same 32-bit location.
- DMA4_CICRi (interrupt event mask)
- CFN (frame number)
- Bit fields:
  - P: Corresponds to the PAUSE_LINK_LIST bit:
    - When set to 1 in the descriptor, the channel is suspended when the descriptor load completes.
    - The user must not set the PAUSE_LINK_LIST bit through the configuration port. Otherwise, behavior is undefined.
    - When set to 0 (through the configuration port) after pause, the linked-list channel resumes its transfer (descriptor load or data load).
  - B: Corresponds to the end-of-block enable bit (BLOCK_IE) of the DMA4_CICRi register; valid only for type 3. This value is don't care for descriptor types 1 and 2, where DMA4_CICRi is fully specified.
  - Nxt_Dv, Nxt_Sv: Mapped in the DMA4_CDPi register. They indicate one of the following possibilities:
    - Next descriptor contains an updated destination or source address.
    - Next descriptor does not update the source or destination address, but increments the last source or destination address (from the end of the last transfer).
    - The next source address and/or destination address are the last valid ones in the configuration memory. This means that the corresponding location in the configuration memory is not updated (assuming that they were initialized at least once in the past). This is also called wrapping addressing.
  - Next_Descriptor_Type: Specifies the next descriptor type that corresponds to the NEXT_DESCRIPTOR_TYPE bit field in the DMA4_CDPi register

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16.4.20.3.1 Type 1

A type 1 descriptor includes the overall channel configuration register value to be loaded (global registers are not part of the type 1 descriptor). This descriptor is used primarily when major changes are required:

- Channel read or write access profiles must be modified; for example, bursting and packing (included in the DMA4_CSDPi register)
- Attach a new DMA request to the same channel or change the priority or access privilege (included in the DMA4_CCRi register)
- Enable solid or transparent color fill (included in the DMA4_CCRi and DMA4_COLORi registers)
- Enable a channel link (included in the DMA4_CLNK_CTRLi register)

Table 16-13 shows a type 1 descriptor.

Table 16-13. Type 1

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0x2C	CCR																															
Ptr+ 0x28	CLNK_CTRL																															
Ptr+ 0x24	CSDP																															
Ptr+ 0x20	COLOR																															
Ptr+ 0x1C	Src_Frame_index/Src_Packet_size																															
Ptr+ 0x18	Dst_Frame_index/Dst_Packet_size																															
Ptr+ 0x14	Src_Element_index																Dst_Element_index															
Ptr+ 0x10	CICR (interrupt events mask)																CFN frame number															
Ptr+ 0xC	Destination_Start_Address																															
Ptr+ 0x8	Source_Start_Address																															
Ptr+ 0x4	N_type				B		Dv			Sv			Element_number																			
Ptr	Next_descriptor_address_pointer																														Rsv	P

16.4.20.3.2 Type 2

A type 2 descriptor includes the overall logical channel transfer address register and transfer format register to be loaded. This descriptor enables 2D addressing linked-list transfer (for example, a multimedia application where 2D objects are moved in a link). Table 16-14 shows a type 2 descriptor with source and destination address updates. Table 16-15 shows a type 2 descriptor with one source or destination address update.

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Table 16-14. Type 2 With Source and Destination Address Updates

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0x1C	Src_Frame_index/Src_Packet_size																															
Ptr+ 0x18	Dst_Frame_index/Dst_Packet_size																															
Ptr+ 0x14	Src_Element_index																Dst_Element_index															
Ptr+ 0x10	CICR (interrupt events Mask)																CFN frame number															
Ptr+ 0xC	Destination_Start_Address																															
Ptr+ 0x8	Source_Start_Address																															
Ptr+ 0x4	N_type				B		Dv		Sv		Element_number																					
Ptr	Next_descriptor_address_pointer																													Rsv		P

Table 16-15. Type 2 With Source or Destination Address Update

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0x18	Src_Frame_index/Src_Packet_size																															
Ptr+ 0x14	Dst_Frame_index/Dst_Packet_size																															
Ptr+ 0x10	Src_Element_index																Dst_Element_index															
Ptr+ 0xC	CICR (interrupt events Mask)																CFN frame number															
Ptr+ 0x8	Source_Start_Address or Destination_Start_Address																															
Ptr+ 0x4	N_type				B		Dv		Sv		Element_number																					
Ptr	Next_descriptor_address_pointer																													Rsv		P

16.4.20.3.3 Type 3

A type 3 descriptor is limited to a few logical channel transfer address registers and transfer format registers to be loaded. This descriptor enables simple 1D addressing link transfer (for example, scatter-gather or ping-pong memory movement using a linked list). Table 16-16 shows a type 3 descriptor with source and destination address updates. Table 16-17 shows a type 3 descriptor with one source or address destination update.

Table 16-16. Type 3 With Source and Destination Address Updates

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0xC	Destination_Start_Address																															
Ptr+ 0x8	Source_Start_Address																															
Ptr+ 0x4	N_type				B		Dv		Sv		Element_number																					
Ptr	Next_descriptor_address_pointer																													Rsv		P

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Table 16-17. Type 3 With Source or Destination Address Update

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ptr+ 0x8	Source_Start_Address or Destination_Start_Address																															
Ptr+ 0x4	N_type			B	Dv			Sv	Element_number																							
Ptr	Next_descriptor_address_pointer																														Rsv	P

16.4.20.4 Linked-List Control and Monitoring

16.4.20.4.1 Transfer Mode Setting

Four descriptor types are available in DMA4_CDPi[9:8] TRANSFER_MODE to distinguish the different transfer modes:

- DMA4_CDPi[9:8] TRANSFER_MODE = 00: The current channel is using normal mode.
- DMA4_CDPi[9:8] TRANSFER_MODE = 01: The current channel is using link-list channel mode for a type 1, 2, or 3 descriptor.

The reset value is normal mode (DMA4_CDPi[9:8] TRANSFER_MODE = 0).

16.4.20.4.2 Starting a Linked List

Like a nonlinked-list transfer, a link transfer starts under host control by enabling the associated logical channel (set the DMA4_CCRi[7] ENABLE bit to 1). The DMA4_CDPi[10] FAST bit sets the start mode of the link-list transfer:

In nonfast-start mode, the logical channel configuration is fully initialized so that the transfer can start without descriptor loading.

In fast-start mode, the descriptor pointer and other inputs are given. The channel starts by loading the descriptor and then starts the data transfer phase.

16.4.20.4.3 Monitoring a Linked-List Progression

In addition to the DMA4_CCENi (remaining elements) and DMA4_CCFNi (remaining frames) registers that are used to monitor the transfer progress, a per-channel register, DMA4_CCDNi (channel current active descriptor number), monitors which descriptor in the list is active. The user must initialize the DMA4_CCDNi register to 0 during the initial configuration. When the DMA4_CCDNi register is updated, the DMA4_CCFNi and the DMA4_CCENi registers are updated. The user must also initialize the DMA4_CCFNi and DMA4_CCENi registers to 0xFFFF and to 0xFFFFFF, respectively, to track the effective transfer start of synchronized transfer.

16.4.20.4.4 Interrupt During Linked-List Execution

Any logical channel source of interrupt can be triggered during a linked-list execution, if the interrupt source is enabled during the initial configuration in CICR. The DMA4_CICRi register can also be updated during the linked-list execution if descriptor types 1 and 2 are used.

The use of an interrupt event in a link execution can be difficult, because the link can progress in parallel with interrupt service routine (ISR) execution. This makes it difficult to synchronize them unless system assumptions are used. The most appropriate synchronization model is to get an interrupt-only on linked-list completion, when the last transfer block is complete. This prevents the interrupt from occurring during the link execution. An end-of-super-block interrupt event available in the DMA4_CICRi and DMA4_CSRi registers can be enabled at initial configuration or when using descriptor types 1 and 2. To prevent the use of descriptor type 1 or 2 to update BLOCK_IE (full DMA4_CICRi update), a dedicated BLOCK_IE bit field is also available in a type 3 descriptor.

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16.4.20.4.5 Pause a Linked List

When the channel is suspended, it remains enabled.

The pause behaves differently, depending on the transfer mode:

- Normal transfer mode: If the user sets the DMA4_CDPi[7] PAUSE_LINK_LIST bit to 1, the channel completes the current read and write transactions and then suspends the channel. The channel can be resumed by setting the channel DMA4_CDPi[7] PAUSE_LINK_LIST bit to 0.
- Linked-list type 1, 2, or 3 mode: The user must not set the DMA4_CDPi[7] PAUSE_LINK_LIST bit through the configuration port; otherwise, transfer behavior is undefined.

  A PAUSE_LINK_LIST bit (P) is set to 1 in the descriptor.

  – The channel is suspended after the descriptor load, translation, and configuration memory update are complete.
  – The linked list can be resumed by resetting the DMA4_CDPi[7] PAUSE_LINK_LIST bit (through the configuration port).

16.4.20.4.6 Stop a Linked List (Abort or Drain)

The channel can be stopped for a drain or an abort. These cases are exclusive.

16.4.20.4.6.1 Drain

- Drain conditions:

  A channel is a drain candidate if it is a hardware-source-synchronized transfer with DMA4_CCRi[25] BUFFERING_DISABLE = 0 and should not be doing any of the graphics operation (transparent copy or solid-color fill).
- Drain trigger:

  A drain candidate channel is drained if it is disabled (DMA4_CCRi[7] ENABLE = 0) or if it receives a transaction error on the read port.
- Drain behavior with a type 1, 2, or 3 descriptor. Drain trigger can occur in two situations:
  – During descriptor loading: Any ongoing current transaction is complete and the channel is aborted.
  – During data loading: The read is completed at the boundary of the request (element/frame/packet/block boundary), the FIFO is drained to the destination, and then a DRAIN_END interrupt can be asserted.

16.4.20.4.6.2 Abort

- Abort condition:

  A channel is an abort candidate if it is software-synchronized, hardware-destination-synchronized, solid color-fill, transparent-color fill, or hardware-source-synchronized with DMA4_CCRi[25] BUFFERING_DISABLE = 1.
- Abort trigger:

  A channel is an abort candidate if it is disabled (DMA4_CCRi[7] ENABLE = 0), if it receives a transaction error on the read or write port, or if there is a MISALIGNMENT_ERROR.
- Abort behavior with a type 1, 2, or 3 descriptor:

  If an abort trigger occurs, the channel aborts immediately after completion of current read/write transactions and then the FIFO is cleaned up.

  In type 1, 2, or 3, if an abort trigger or drain trigger occurs during the descriptor load phase, the channel aborts.

16.4.20.4.7 Status Bit Behavior

This section describes the behavior of the DMA4_CSRi[6] SYNC, DMA4_CCRi[9] RD_ACTIVE and DMA4_CCRi[10] WR_ACTIVE status bits:

- For a hardware-synchronized channel in linked-list mode, the DMA4_CSRi[6] SYNC bit becomes active (DMA4_CSRi[6] SYNC = 1) when the first data load transaction is scheduled and remains active

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until the last data load transaction in the block (not super block) is descheduled (DMA4_CSRi[6] SYNC = 0). The SYNC bit is not active during the descriptor load phase.

- The DMA4_CCRi[9] RD_ACTIVE bit is active during the data load phase and the descriptor load phase. It becomes active when the first read transaction is scheduled. It becomes inactive:
  - When (during the descriptor load phase) the last descriptor write request is descheduled
  - When (during the data load phase) the last read transaction in the block (not super block) is descheduled for software-synchronized transfer or destination-synchronized transfer with prefetch enabled
  - When (during the data load phase) the last read transaction in the request (element/frame/packet/block sync) is descheduled for hardware-source-synchronized transfer or hardware-destination-synchronized transfer without prefetch
- The DMA4_CCRi[10] WR_ACTIVE bit is active only during the data load phase. It becomes active when the first write transaction is scheduled and becomes inactive:
  - Until the last write transaction in the block (not super block) is descheduled and the FIFO is cleaned up for software-synchronized transfer
  - Until the last write transaction in the request (element/frame/packet/block sync) is descheduled and the FIFO is cleaned up for hardware-source-synchronized transfer (with DMA4_CCRi[25] BUFFERING_DISABLE = 0) or hardware-destination-synchronized transfer.

16.4.20.4.8 Linked-List Channel Linking

Channel linking for inter- and intra-super blocks is supported for type 1, 2, and 3 descriptors.

Assume that CHx and CHz are linked-list channels using generic descriptors. If CHx is composed of N descriptors and CHz is composed of M descriptors, then in nonfast mode:

CHx: CHx[Data1]-> CHx[DES1] -> . -> CHx[DESN]->CHx[DataN + 1]

CHz: CHz[Data1]-> CHz[DES1] -> . -> CHz[DESM]->CHz[DataM + 1]

It is possible to link CHx to CHz or CHx to itself after the completion of the CHx transfer (end of super block). To do this, the user must set the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit to 1 and the DMA4_CLNK_CTRLi[4:0] NEXTLCH_ID bit to z (or to x for self linking) through the last descriptor using a type 1 descriptor. The sequence is:

CHx: CHx[Data1]-> CHx[DES1] -> . -> CHx[DESN]-CHx[DataN+1] -> CHz: CHz[Data1]-> CHz[DES1] -> . -> CHz[DESM]->CHz[DataM+1]

It is also possible to link CHx to CHz during the CHx transfer and before the end of super block. The user must set the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit to 1 and the DMA4_CLNK_CTRLi[4:0] NEXTLCH_ID bit to z through descriptor p (CHx[DESp]) using a type 1 descriptor. The sequence is:

CHx: CHx[Data1]-> CHx[DES1] ->.-> CHx[DESp]->CHx[Data(p + 1)] -> CHz[Data1]-> CHz[DES1] -> .

The user must continue the linking until channels CHx and CHz complete their super-block transfers; otherwise, the channels remain enabled.

NOTE: In channel linking, the head of a chain can be in fast mode or nonfast mode. All channels that are not in the head of the chain can be in nonfast mode only. In self-linking, the channel cannot be in fast mode.

NOTE: If channel CHx links to CHz in the middle of the superblock transfer (remember link bit can be set through Type-1 descriptor load), CHx is disabled after the corresponding data load and enables the channel CHz.

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16.5 DMA_SYSTEM Basic Programming Model

16.5.1 Setup Configuration

After a hardware reset, program all fields in the logical channel registers to default values for any channels used, because most fields are undefined following reset.

Before programming any DMA transfers, the priority arbitration rate and the maximum FIFO depth must be configured through the DMA4_GCR register, and any required interrupts must be enabled through the DMA4_IRQENABLE_Lj registers and the logical channel DMA4_CICRi registers.

Software clears the DMA4_CSRi register and the IRQSTATUS bit for the different interrupt lines before enabling the channel.

16.5.2 Software-Triggered (Nonsynchronized) Transfer

To program a software-triggered DMA transfer:

1. Configure the transfer parameters in the logical DMA channel registers:
   - DMA4_CSDPi:
     - Transfer ES (8, 16, or 32 bits) in the DMA DMA4_CSDPi[1:0] bit field.
     - Read and write port access types (single/burst), DMA DMA4_CSDPi[8:7] and DMA4_CSDPi[15:14] bit fields
     - Source and destination endianism, DMA DMA4_CSDPi[21] and DMA4_CSDPi[19] bits
     - Write mode (posted or nonposted) and DMA DMA4_CSDPi[17:16] bit field
     - Source or destination packed or nonpacked (if the ES is less than the read/write port size), DMA DMA4_CSDPi[6] and DMA4_CSDPi[13] bits
   - DMA4_CENi: EN
   - DMA4_CFNi: FN per transfer block
   - DMA4_CSSAi and DMA4_CDSAi: Source and destination start address (aligned with transfer ES)
   - DMA4_CCRi:
     - Read and write port addressing modes, DMA DMA4_CCRi[13:12] and DMA4_CCRi[15:14] bit field
     - Priority bit for both read and write ports, DMA DMA4_CCRi[6] and DMA4_CCRi[26] bits
     - DMA request number (set to 0 for a software-triggered transfer) and DMA register bit fields DMA4_CCRi[4:0] = 0 and DMA4_CCRi[20:19] = 0
   - DMA4_CSEIi, DMA4_CSFIi, DMA4_CDEIi, and DMA4_CDFIi: Source and destination element and frame indexes (depending on addressing mode)
2. Start the transfer through the enable bit in the channel DMA4_CCRi register and DMA DMA4_CCRi[7] bit

The following example performs a DMA transfer on channel 10 of a 240*160 picture from RAM to RAM (0x80C00000 to 0x80F00000):

```
UWORD32 RegVal = 0;
DMA4_t *DMA4;
DMA4 = (DMA4_t
      *)malloc(sizeof(DMA4_t));

/* Init. parameters
      */
DMA4->DataType = 0x2; //
      DMA4_CSDPi[1:0]
DMA4->ReadPortAccessType = 0; //
      DMA4_CSDPi[8:7]
DMA4->WritePortAccessType = 0; //
      DMA4_CSDPi[15:14]
DMA4->SourceEndiansim = 0; //
      DMA4_CSDPi[21]
```

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```
DMA4->DestinationEndianism = 0; //
      DMA4_CSDPi[19]
DMA4->WriteMode = 0; //
      DMA4_CSDPi[17:16]
DMA4->SourcePacked = 0; //
      DMA4_CSDPi[6]
DMA4->DestinationPacked = 0; //
      DMA4_CSDPi[13]
DMA4->NumberOfElementPerFrame = 240; //
      DMA4_CENi
DMA4->NumberOfFramePerTransferBlock = 160; //
      DMA4_CFNi
DMA4->SourceStartAddress = 0x80C00000; //
      DMA4_CSSAi
DMA4->DestinationStartAddress = 0x80F00000; //
      DMA4_CDSAi
DMA4->SourceElementIndex = 1; //
      DMA4_CSEIi
DMA4->SourceFrameIndex = 1; //
      DMA4_CSFIi
DMA4->DestinationElementIndex = 1; //
      DMA4_CDEIi
DMA4->DestinationFrameIndex = 1; //
      DMA4_CDFIi
DMA4->ReadPortAccessMode = 1; //
      DMA4_CCRi[13:12]
DMA4->WritePortAccessMode = 1; //
      DMA4_CCRi[15:14]
DMA4->ReadPriority = 0; //
      DMA4_CCRi[6]
DMA4->WritePriority = 0; //
      DMA4_CCRi[23]
DMA4->ReadRequestNumber = 0; //
      DMA4_CCRi[4:0]
DMA4->WriteRequestNumber = 0; //
      DMA4_CCRi[20:19]


/* 1) Configure the transfer
      parameters in the logical DMA registers
      */
/*-------------------------------------------------------------------*/

/*
      a) Set the data type CSDP[1:0], the Read/Write Port access type
      CSDP[8:7]/[15:14], the Source/dest endianism CSDP[21]/CSDP[19], write
      mode CSDP[17:16], source/dest packed or non-packed
      CSDP[6]/CSDP[13]*/

// Read CSDP
RegVal =
      DMA4_CSDP_CH10;

// Build reg
RegVal = ((RegVal &~ 0x3)
      | DMA4->DataType );
RegVal = ((RegVal &~(0x3 << 7)) |
      (DMA4->ReadPortAccessType << 7));
RegVal = ((RegVal &~(0x3 << 14)) |
      (DMA4->WritePortAccessType << 14));
RegVal = ((RegVal &~(0x1 << 21)) |
      (DMA4->SourceEndiansim << 21));
RegVal = ((RegVal &~(0x1 << 19)) |
      (DMA4->DestinationEndianism << 19));
RegVal = ((RegVal &~(0x3 << 16)) |
      (DMA4->WriteMode << 16));
```

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```
RegVal = ((RegVal &~(0x1 << 6)) |
      (DMA4->SourcePacked << 6));
RegVal = ((RegVal &~(0x1 << 13)) |
      (DMA4->DestinationPacked << 13));

// Write CSDP

DMA4_CSDP_CH10 = RegVal;

/* b) Set the number of
      element per frame CEN[23:0]*/

DMA4_CEN_CH10 =
      DMA4->NumberOfElementPerFrame;

/* c) Set the number of frame
      per block CFN[15:0]*/

DMA4_CFN_CH10 =
      DMA4->NumberOfFramePerTransferBlock;

/* d) Set the
      Source/dest start address index CSSA[31:0]/CDSA[31:0]*/


DMA4_CSSA_CH10 = DMA4->SourceStartAddress; // address start

DMA4_CDSA_CH10 = DMA4->DestinationStartAddress; // address dest


/* e) Set the Read Port addressing mode CCR[13:12], the
      Write Port addressing mode CCR[15:14], read/write priority
      CCR[6]/CCR[26], the current LCH CCR[20:19]=00 and CCR[4:0]=00000*/


// Read CCR
RegVal = DMA4_CCR_CH10;

//
      Build reg
RegVal = ((RegVal &~(0x3 << 12)) | (DMA4->ReadPortAccessMode      << 12));
RegVal = ((RegVal &~(0x3 << 14)) | (DMA4->WritePortAccessMode
      << 14));
RegVal = ((RegVal &~(0x1 << 6)) | (DMA4->ReadPriority << 6));

RegVal = ((RegVal &~(0x1 << 26)) | (DMA4->WritePriority << 26));

RegVal &= 0xFFCFFFE0 ;

// Write CCR
DMA4_CCR_CH10
      = RegVal;

/* f)- Set the source element index CSEI[15:0]*/


DMA4_CSEI_CH10 = DMA4->SourceElementIndex;

/* g)-
      Set the source frame index CSFI[15:0]*/

DMA4_CSFI_CH10 =
      DMA4->SourceFrameIndex ;

/* h)- Set the destination element
      index CDEI[15:0]*/
```

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```
DMA4_CDEI_CH10 =
      DMA4->DestinationElementIndex;

/* i)- Set the destination
      frame index CDFI[31:0]*/

DMA4_CDFI_CH10 =
      DMA4->DestinationFrameIndex;

/* 2) Start the DMA transfer by
      Setting the enable bit CCR[7]=1 */

/*----------------------------------------------------------------*/


//write enable bit
DMA4_CCR_CH10 |= 1 << 7; /* start */
```

16.5.3 Hardware-Synchronized Transfer

To monitor a hardware synchronized DMA transfer, initialize the DMA4_CDACi register before the software enable.

To configure an LCh to synchronize by element, packet, frame, or block, the frame synchronization DMA4_CCRi[5] FS bit and the block synchronization DMA4_CCRi[18] BS bit must be programmed. For all the following synchronized transfers (element, packet, and frame or block-synchronized transfers), the user must first set the DMA4_CCRi[24] SEL_SRC_DST_SYNC bit to 1 when the source triggers on the DMA request and set it the DMA4_CCRi[24] SEL_SRC_DST_SYNC bit to 0 when the destination triggers on the DMA request.

NOTE: The user must take care when setting the DMA4_CCRi[23] PREFETCH bit it is in conjunction with DMA4_CCRi[24] SEL_SRC_DST_SYNC bit.

- To configure an LCh to transfer one element per DMA request:
  1. Set the number of DMA request associated with the current LCH in the DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER and DMA4_CCRi[4:0] SYNCHRO bit field.
  2. Set the data type, also referenced as element size (ES), in the DMA4_CSDPi[1:0] DATA_TYPE bit field.
  3. Set the Read Port access type (single or burst access) in the DMA4_CSDPi[8:7] SRC_BURST_EN bit field.
  4. Set the Write Port access type (single or burst access) in the DMA4_CSDPi[15:14] DST_BURST_EN bit field.
  5. Set the Read Port addressing mode in the DMA4_CCRi[13:12] SRC_AMODE bit field.
  6. Set the Write Port addressing mode in the DMA4_CCRi[15:14] DST_AMODE bit field.
  7. Set the Read start address in the DMA4_CSSAi[31:0] SRC_START_ADRS bit field.
  8. Set the Write start address in the DMA4_CDSAi[31:0] DST_START_ADRS bit field.
  9. Set both FS and BS to 0 in DMA4_CCRi[5] FS and DMA4_CCRi[18] BS.
  10. Set to 1 the channel enable bit DMA4_CCRi[7] EN.
- To configure an LCh to transfer one frame per DMA request:
  1. Set the number of DMA request associated to the current LCH in the DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER and DMA4_CCRi[4:0] SYNCHRO bit field.
  2. Set the data type, also referenced as element size (ES), in the DMA4_CSDPi[1:0] DATA_TYPE bit field.
  3. Set the number of element per frame in the DMA4_CENi[23:0] CHANNEL_ELMNT_NBR bit field.
  4. Set the Read Port access type (single or burst access) in the DMA4_CSDPi[8:7] SRC_BURST_EN

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bit field.

5. Set the Write Port access type (single or burst access) in the DMA4_CSDPi[15:14] DST_BURST_EN bit field.
6. Set the Read Port addressing mode in the DMA4_CCRi[13:12] SRC_AMODE bit field.
7. Set the Write Port addressing mode in the DMA4_CCRi[15:14] DST_AMODE bit field.
8. Set the Read start address in the DMA4_CSSAi[31:0] SRC_START_ADRS bit field.
9. Set the Write start address in the DMA4_CDSAi[31:0] DST_START_ADRS bit field.
10. Set FS to 1 and BS to 0, respectively, in DMA4_CCRi[5] FS and DMA4_CCRi[18] BS.
11. Set to 1 the channel enable bit DMA4_CCRi[7] EN.

- To configure an LCh to transfer one block per DMA request:
  1. Set the number of DMA request associated to the current LCH in the DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER and DMA4_CCRi[4:0] SYNCHRO bit field.
  2. Set the data type, also referenced as element size (ES), in the DMA4_CSDPi[1:0] DATA_TYPE bit field.
  3. Set the number of element per frame in the DMA4_CENi[23:0] CHANNEL_ELMNT_NBR bit field.
  4. Set in the DMA4_CFNi[15:0] CHANNEL_FRAME_NBR bit field the number of frame (transfers), to take place before the LCH gets disabled.
  5. Set the Read Port access type (single or burst access) in the DMA4_CSDPi[8:7] SRC_BURST_EN bit field.
  6. Set the Write Port access type (single or burst access) in the DMA4_CSDPi[15:14] DST_BURST_EN bit field.
  7. Set the Read Port addressing mode in the DMA4_CCRi[13:12] SRC_AMODE bit field.
  8. Set the Write Port addressing mode in the DMA4_CCRi[15:14] DST_AMODE bit field.
  9. Set the Read start address in the DMA4_CSSAi[31:0] SRC_START_ADRS bit field.
  10. Set the Write start address in the DMA4_CDSAi[31:0] DST_START_ADRS bit field.
  11. Set FS to 0 and BS to 1, respectively, in DMA4_CCRi[5] FS and DMA4_CCRi[18] BS.
  12. Set to 1 the channel enable bit DMA4_CCRi[7] EN.
- To configure an LCh to transfer one packet per DMA request:
  1. Set the number of DMA request associated to the current LCH in the DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER and DMA4_CCRi[4:0] SYNCHRO bit field.
  2. Set the data type, also referenced as element size (ES), in the DMA4_CSDPi[1:0] DATA_TYPE bit field.
  3. Set the number of elements per packet to transfer: If the packet requestor is in the source, set DMA4_CCRi [24] SEL_SRC_DST_SYNC to 1 and set the packet element number in the DMA4_CSFIi register and set the addressing mode of source to constant addressing in DMA4_CCRi[13:12] SRC_AMODE bit field; else, if the packet requestor is in the destination, set the DMA4_CCRi[24] SEL_SRC_DST_SYNC to 0 and set the packet element number in the DMA4_CDFIi register and set the addressing mode of destination to constant addressing in DMA4_CCRi[15:14] DST_AMODE bit field.
  4. Set the number of elements per frame in the DMA4_CENi[23:0] CHANNEL_ELMNT_NBR bit field.
  5. Set in the DMA4_CFNi[15:0] CHANNEL_FRAME_NBR bit field the number of frames (transfers), to take place before the LCH gets disabled.
  6. Set the element number in the packet in the DMA4_CSFIi[15:0] PKT_ELNT_NBR, if constant addressing or post-incremented addressing modes are used in the source side. However, the number of element in the packet is set in the DMA4_CDFIi[15:0] PKT_ELNT_NBR if constant addressing mode is used in the destination side.
  7. Set the Read Port access type (single or burst access) in the DMA4_CSDPi[8:7] SRC_BURST_EN bit field.
  8. Set the Write Port access type (single or burst access) in the DMA4_CSDPi[15:14] DST_BURST_EN bit field.

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9. Set the Read Port addressing mode in the DMA4_CCRi[13:12] SRC_AMODE bit field.
10. Set the Write Port addressing mode in the DMA4_CCRi[15:14] DST_AMODE bit field.
11. Set the Read start address in the DMA4_CSSAi[31:0] SRC_START_ADRS bit field.
12. Set the Write start address in the DMA4_CDSAi[31:0] DST_START_ADRS bit field.
13. Set FS to 1 and BS to 1, respectively, in DMA4_CCRi[5] FS and DMA4_CCRi[18] BS.
14. Set to 1 the channel enable bit DMA4_CCRi[7] EN.

NOTE: It is possible to stop a transfer by disabling the channel by resetting the DMA4_CCRi[7] ENABLE bit.

16.5.4 Synchronized Transfer Monitoring Using CDAC

The DMA4_CDACi register is writable and non-initialized (value undefined). It can be initialized to monitor a transfer by applying the following programming model:

1. Write 0 in the DMA4_CDACi register.
2. Enable the channel.
3. If a time-out occurs, read DMA4_CDACi register.
4. If DMA4_CDACi != 0 (it is the value configured in DMA4_CDACi):

   This indicates that the corresponding transfer has started. The user can then rely on DMA4_CCENi and DMA4_CCFNi element and frame counters.

   Otherwise, if DMA4_CDACi = 0 (it is the value configured in the DMA4_CDACi):

   This indicates that the corresponding transfer did not start.

16.5.5 Concurrent Software and Hardware Synchronization

This section describes thread allocation only; it does not describe the entire transfer. Because synchronized transfers are latency critical, you must allocate a thread at least on the synchronized target side.

Even for multiple concurrent channels, thread reservation ensures that when a hardware DMA request arrives, the read/write scheduler finds available thread(s) to initiate a channel schedule and issue a read/write transaction.

Consider six concurrent channels:

- Channels 0, 1, 2, and 3 are dedicated to memory-memory transfer; they are software triggered and not synchronized.
- Channel 4 is dedicated to memory-peripheral transfer, hardware triggered, and synchronized on the write side.
- Channel 5 is dedicated to peripheral-memory transfer, hardware triggered, and synchronized on the read side.

To perform thread reservation:

1. Allow thread reservation for priority channel 4 and channel 5:

   Reserve one thread (Read ThreadID 0) on the read port and one thread (Write ThreadID 0) on the write port: set the DMA4_GCR[13:12] HI_THREAD_RESERVED bit field to 0x1.
2. Specify channel priority:

   Channel 4 is a write high priority channel: set DMA4_CCRi[26] WRITE_PRIORITY = 1.

   Channel 5 is a read high priority channel: set DMA4_CCRi[6] READ_PRIORITY = 1.

16.5.6 Chained Transfer

A chained DMA transfer can be programmed as follows:

1. Configure the transfer parameters for each logical DMA channel in the chain as in step 1 for either the synchronized or non-synchronized transfers describe in Section 16.5.5, *Concurrent Software and*

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Hardware Synchronization.

2. For each channel in the chain, configure the DMA4_CLNK_CTRLi register as follows:
   - Next logical DMA channel number (for a looping chained transfer link last channel to first channel number), in the DMA4_CLNK_CTRLi[4:0] NEXTLCH_ID bit field.
   - Include the logical channel to the chain and enable link by setting the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit.
   - For a non-looping chain, the last logical channel in the chain must have the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit set to 0 to indicate the end of the chain.
3. Enable the transfer through the enable bit in the first logical channel DMA4_CCRi[7] ENABLE bit. All other channels in the chain must be disabled. Each channel is enabled automatically in turn when the previous logical channel transfer completes. A non-synchronized transfer starts immediately; a hardware-synchronized transfer starts when the DMA request line corresponding to the first DMA channel in the chain is asserted.

To stop a looping chained transfer, disable the DMA4_CLNK_CTRLi[15] ENABLE_LNK bit (by setting it to 0x0), of the final channel transfer.

In the RAM-to-RAM copy example, to copy in loop, it is possible to link channel 10 on itself. The following line can be added in the channel configuration:

```
/* g) Set link for loop */
DMA4_CLINK_CTRL_CH10 =
      0x0000800A;
```

16.5.7 90-Degree Clockwise Image Rotation

The 90-degree clockwise image rotation example described in Section 16.4.5, *Addressing Modes*, can be programmed as follows:

1. Configure the transfer parameters in the logical DMA channel registers:
   - DMA4_CSDPi:
     - Transfer ES = 32-bit (32 bpp), DMA4_CSDPi[1:0] DATA_TYPE bit field
     - Read and write port access types = maximum burst size supported by memory device, DMA4_CSDPi[8:7] SRC_BURST_EN and DMA4_CSDPi[15:14] DST_BURST_EN bit fields
     - Source and destination endianism, DMA4_CSDPi[21] SRC_ENDIAN and DMA4_CSDPi[19] DST_ENDIAN bits
     - Write mode = posted with last element nonposted, DMA4_CSDPi[17:16] WRITE_MODE bit field
     - Source and destination packed = Yes (although destination writes do not benefit because EI1), DMA4_CSDPi[6] SRC_PACKED and DMA4_CSDPi[13] DST_PACKED bits
   - DMA4_CENi: EN = 240
   - DMA4_CFNi: FN per transfer block = 160
   - DMA4_CSSAi: Source start address = 0x100000
   - DMA4_CDSAi: destination start address = 0x20013E
   - DMA4_CCRi:
     - Read and write port addressing modes = double-index addressing mode for both or post-increment addressing on source and double-index addressing on destination, DMA4_CCRi[13:12] SRC_AMODE and DMA4_CCRi[15:14] DST_AMODE bit fields
     - Low or high priority, DMA4_CCRi[6] READ_PRIORITY bit
     - DMA request number = 0 (for software-triggered transfer), DMA4_CCRi[4:0] SYNCHRO_CONTROL and DMA4_CCRi[20:19] SYNCHRO_CONTROL_UPPER bit fields
   - DMA4_CSEIi: Source EI = 1
   - DMA4_CSFIi: Source frame index = 1
   - DMA4_CDEIi: destination EI = 637
   - DMA4_CDFIi: destination frame index = 152967

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2. Start the transfer through the enable bit in the channel DMA4_CCRi register.

The following parameters are used to perform this rotation from 0x80C00000 RAM address to 0x80F00000, with the same code used in Section 16.5.2, *Software-Triggered (Nonsynchronized) Transfer*:

```
/* Init. parameters */
DMA4->DataType = 0x2; //
      DMA4_CSDPi[1:0]
DMA4->ReadPortAccessType = 0x3; // DMA4_CSDPi[8:7]

DMA4->WritePortAccessType = 0x3; // DMA4_CSDPi[15:14]

DMA4->SourceEndiansim = 0; // DMA4_CSDPi[21]

DMA4->DestinationEndianism = 0; // DMA4_CSDPi[19]

DMA4->WriteMode = 0x2; // DMA4_CSDPi[17:16]
DMA4->SourcePacked
      = 0x1; // DMA4_CSDPi[6]
DMA4->DestinationPacked = 0x1; //
      DMA4_CSDPi[13]
DMA4->NumberOfElementPerFrame = 240; // DMA4_CENi

DMA4->NumberOfFramePerTransferBlock = 160; // DMA4_CFNi

DMA4->SourceStartAddress = 0x80C00000; // DMA4_CSSAi

DMA4->DestinationStartAddress = 0x80F00000; // DMA4_CDSAi

DMA4->SourceElementIndex = 1; // DMA4_CSEIi

DMA4->SourceFrameIndex = 1; // DMA4_CSFIi

DMA4->DestinationElementIndex = 637; // DMA4_CDEIi

DMA4->DestinationFrameIndex = -152967; // DMA4_CDFIi

DMA4->ReadPortAccessMode = 0x3; // DMA4_CCRi[13:12]

DMA4->WritePortAccessMode = 0x3; // DMA4_CCRi[15:14]

DMA4->ReadPriority = 0; // DMA4_CCRi[6]
DMA4->WritePriority =
      0; // DMA4_CCRi[23]
DMA4->ReadRequestNumber = 0; // DMA4_CCRi[4:0]

DMA4->WriteRequestNumber = 0; // DMA4_CCRi[20:19]
```

16.5.8 Graphic Operations

- Transparent copy:
  1. Set the DMA4_CCRi[17] TRANSPARENT_COPY_ENABLE bit to 1
  2. Set the DMA4_CCRi[16] CONST_FILL_ENABLE bit to 0
  3. Set the value of the key color in the DMA4_COLORi[15:0] COLOR_KEY bit field

  To perform this graphic operation, the following lines can be added to the example of Section 16.5.2, *Software-Triggered (Nonsynchronized) Transfer*.

```
DMA4_CCR_CH10 &= ~(0x1 << 16);
DMA4_CCR_CH10 |= 0x1 << 17;

DMA4_COLOR_CH10 = 0x00000003;
```

- Solid Color fill:
  1. Set the DMA4_CCRi[16] CONST_FILL_ENABLE bit to 1
  2. Set the DMA4_CCRi[17] TRANSPARENT_COPY_ENABLE bit to 0

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3. Set the value of key the color in the DMA4_COLORi[15:0] SOLID_COLOR bit field

To perform this graphic operation, the following lines can be added to the example of Section 16.5.2, *Software-Triggered (Nonsynchronized) Transfer*.

```
DMA4_CCR_CH10 &= ~(0x1 << 17);
DMA4_CCR_CH10 |= 0x1 << 16;

DMA4_COLOR_CH10 = 0x00000003;
```

16.5.9 Linked-List Programming Guidelines

- With the exception of the DMA4_CCRi[7] ENABLE bit and the DMA4_CDPi[7] PAUSE_LINK_LIST bit during a linked-list transfer (descriptor load phase or data load phase), avoid programming any register through the configuration port.
- Before enabling any linked-list transfer, ensure that all global registers and all registers in the descriptor are initialized. Some static channel registers (registers that are not updated by the descriptor to be loaded) must also be initialized correctly:
  - For type 2, the following registers must be initialized with consistent values:
    - All global registers
    - DMA4_CCRi
    - DMA4_CSDPi
    - DMA4_CLNK_CTRLi
  - For type 3, the following registers must be initialized with consistent values:
    - All global registers
    - DMA4_CCRi
    - DMA4_CSDPi
    - DMA4_CLNK_CTRLi
    - DMA4_CICRi
    - DMA4_CFNi
- In case of a linked list with descriptor types 2 and 3, the content of the DMA4_CCRi register must not change during super-block life.
- The PAUSE_LINK_LIST bit must not be set in the initialization phase.

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16.6 DMA_SYSTEM Register Manual

16.6.1 DMA_SYSTEM Instance Summary

Table 16-18. DMA_SYSTEM Instance Summary

Module Name	Base Address	Size
DMA_SYSTEM	0x4A05 6000	4 KiB

16.6.2 DMA_SYSTEM Registers

16.6.2.1 DMA_SYSTEM Register Summary

Index *i* represents the logical channel number (where i = 0 to 31). The offset address for some registers is calculated from the channel *c* number. For example, the DMA4_CCR10 (channel 10) register has an offset address of 10 × 0x60 = 0x3C0, and thus a physical address of 0x4A05 6080 + 0x3C0 = 0x4A05 6440.

Index *j* represents the interrupt line number (where j = 0 to 3) The offset address for some registers is calculated from the channel *c* number. For example, the DMA4_IRQSTATUS_L3 (line 3) register has an offset address of 3 × 0x4 = 0xC, and thus a physical address of 0x4A05 6008 + 0xC = 0x4A05 6014.

Table 16-19. DMA_SYSTEM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DMA_SYSTEM Base Address
DMA4_REVISION	R	32	0x0000 0000	0x4A05 6000
DMA4_IRQSTATUS_Lj (1)	RW	32	0x0000 0008 + (0x4 * j)	0x4A05 6008 + (0x4 * j)
DMA4_IRQENABLE_Lj (1)	RW	32	0x0000 0018 + (0x4 * j)	0x4A05 6018 + (0x4 * j)
DMA4_SYSSTATUS	R	32	0x0000 0028	0x4A05 6028
DMA4_OCP_SYSCONFIG	RW	32	0x0000 002C	0x4A05 602C
DMA4_CAPS_0	RW	32	0x0000 0064	0x4A05 6064
DMA4_CAPS_2	R	32	0x0000 006C	0x4A05 606C
DMA4_CAPS_3	R	32	0x0000 0070	0x4A05 6070
DMA4_CAPS_4	RW	32	0x0000 0074	0x4A05 6074
DMA4_GCR	RW	32	0x0000 0078	0x4A05 6078
DMA4_CCRi (2)	RW	32	0x0000 0080 + (0x60 * i)	0x4A05 6080 + (0x60 * i)
DMA4_CLNK_CTRLi (2)	RW	32	0x0000 0084 + (0x60 * i)	0x4A05 6084 + (0x60 * i)
DMA4_CICRi (2)	RW	32	0x0000 0088 + (0x60 * i)	0x4A05 6088 + (0x60 * i)
DMA4_CSRi (2)	RW	32	0x0000 008C + (0x60 * i)	0x4A05 608C + (0x60 * i)
DMA4_CSDPi (2)	RW	32	0x0000 0090 + (0x60 * i)	0x4A05 6090 + (0x60 * i)
DMA4_CENi (2)	RW	32	0x0000 0094 + (0x60 * i)	0x4A05 6094 + (0x60 * i)
DMA4_CFNi (2)	RW	32	0x0000 0098 + (0x60 * i)	0x4A05 6098 + (0x60 * i)
DMA4_CSSAi (2)	RW	32	0x0000 009C + (0x60 * i)	0x4A05 609C + (0x60 * i)

(1) j = 0 to 3
(2) i = 0 to 31

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Table 16-19. DMA_SYSTEM Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	DMA_SYSTEM Base Address
DMA4_CDSAi [2]	RW	32	0x0000 00A0 + (0x60 * i)	0x4A05 60A0 + (0x60 * i)
DMA4_CSEIi [2]	RW	32	0x0000 00A4 + (0x60 * i)	0x4A05 60A4 + (0x60 * i)
DMA4_CSFIi [2]	RW	32	0x0000 00A8 + (0x60 * i)	0x4A05 60A8 + (0x60 * i)
DMA4_CDEIi [2]	RW	32	0x0000 00AC + (0x60 * i)	0x4A05 60AC + (0x60 * i)
DMA4_CDFIi [2]	RW	32	0x0000 00B0 + (0x60 * i)	0x4A05 60B0 + (0x60 * i)
DMA4_CSACi [2]	R	32	0x0000 00B4 + (0x60 * i)	0x4A05 60B4 + (0x60 * i)
DMA4_CDACi [2]	RW	32	0x0000 00B8 + (0x60 * i)	0x4A05 60B8 + (0x60 * i)
DMA4_CCENi [2]	RW	32	0x0000 00BC + (0x60 * i)	0x4A05 60BC + (0x60 * i)
DMA4_CCFNi [2]	RW	32	0x0000 00C0 + (0x60 * i)	0x4A05 60C0 + (0x60 * i)
DMA4_COLORi [3]	RW	32	0x0000 00C4 + (0x60 * i)	0x4A05 60C4 + (0x60 * i)
DMA4_CDPi [3]	RW	32	0x0000 00D0 + (0x60 * i)	0x4A05 60D0 + (0x60 * i)
DMA4_CNDPi [3]	RW	32	0x0000 00D4 + (0x60 * i)	0x4A05 60D4 + (0x60 * i)
DMA4_CCDNi [3]	RW	32	0x0000 00D8 + (0x60 * i)	0x4A05 60D8 + (0x60 * i)

[3] i = 0 to 31

16.6.2.2 DMA_SYSTEM Register Description

NOTE: Some registers have no reset value (marked with -) because of hardware implementation in memory. Software must ensure the correct programming of these registers, if needed.

Shadow registers are used to read run-time registers such as CCEN, CCFN, CDAC, and CSAC. Typically, when accessed in 8-bit or 16-bit access for two consecutive accesses, the value of the previous registers can change. A shadow register holds the entire value to let the next access recover the remaining 24 or 16 bits.

For non-32-bit transactions, start reading or writing from the LSByte first to enable the register update. There is no issue for 32-bit read-write transactions.

Table 16-20. DMA4_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A05 6000	**Instance**	DMA_SYSTEM
Description	This register contains the DMA revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

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Bits	Field Name	Description	Type	Reset
31:0	REVISION	Reserved, Write 0's for future compatibility. Read returns 0	R	See(1)

(1) TI internal Data

Table 16-21. Register Call Summary for Register DMA4_REVISION

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [0]

Table 16-22. DMA4_IRQSTATUS_Lj

Address Offset	0x0000 0008 + (0x4 * j)	**Index**	j = 0 to 3
Physical Address	0x4A05 6008 + (0x4 * j)	**Instance**	DMA_SYSTEM
Description	The interrupt status register regroups all the status of the DMA_SYSTEM channels that can generate an interrupt over line Lj.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH_31_0_Lj																															

Bits	Field Name	Description	Type	Reset
31:0	CH_31_0_Lj	Channel 31 Interrupt on Lj: When an interrupt is seen on the line Lj the status of a interrupting channel i is read in the bit field i. Read 0x0: Channel Interrupt Lj false Write 0x0: Channel Interrupt Lj status bit unchanged Write 0x1: Channel Interrupt Lj status bit is reset Read 0x1: Channel Interrupt Lj true (pending)	RW W1toClr	0x0000 0000

Table 16-23. Register Call Summary for Register DMA4_IRQSTATUS_Lj

DMA_SYSTEM Functional Description
- DMA_SYSTEM Controller Interrupt Requests: [0] [1] [2] [3]
- Interrupt Generation: [4]

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [5]

Table 16-24. DMA4_IRQENABLE_Lj

Address Offset	0x0000 0018 + (0x4 * j)	**Index**	j = 0 to 3
Physical Address	0x4A05 6018 + (0x4 * j)	**Instance**	DMA_SYSTEM
Description	The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on line Lj		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH_31_0_Lj_EN																															

Bits	Field Name	Description	Type	Reset
31:0	CH_31_0_Lj_EN	Channel Interrupt on Lj mask/unmask : to Mask/Unmask a channel i interrupt on Lj the user writes 0/1 on the bit field i. 0x0: Channel Interrupt Lj is masked 0x1: Channel Interrupt Lj generates an interrupt when it occurs	RW	0x0000 0000

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Table 16-25. Register Call Summary for Register DMA4_IRQENABLE_Lj

DMA_SYSTEM Functional Description • DMA_SYSTEM Controller Interrupt Requests: [0] [1] [2] [3] • Interrupt Generation: [4]
DMA_SYSTEM Basic Programming Model • Setup Configuration: [5]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [6]

Table 16-26. DMA4_SYSSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4A05 6028	**Instance**	DMA_SYSTEM
Description	The register provides status information about the module excluding the interrupt status information (see interrupt status register)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved for module-specific status information	R	0x0000 0000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is on-going Read 0x1: Reset completed	R	1

Table 16-27. Register Call Summary for Register DMA4_SYSSTATUS

DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [0]

Table 16-28. DMA4_OCP_SYSCONFIG

Address Offset	0x0000 002C		
Physical Address	0x4A05 602C	**Instance**	DMA_SYSTEM
Description	DMA system configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MIDLEMODE		RESERVED		CLOCKACTIVITY		RESERVED		EMUFREE		SIDLEMODE		RESERVED	RESERVED	AUTOIDLE

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Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0x00000
13:12	MIDLEMODE	Read write power management, standby/wait control 0x0: Force-standby: MStandby is asserted only when all the DMA channels are disabled 0x1: No-Standby: MStandby is never asserted 0x2: Smart-Standby: MStandby is asserted if at least one of the following two conditions is satisfied: 1. All the channels are disabled, OR 2. There is no non-synchronized channel enabled AND [if hardware synchronized channel is enabled, then no DMA request input is asserted and no requests are pending to be serviced]. 0x3: Reserved	RW	0x0
11:10	RESERVED	Reserved for clocks activities extension	RW	0x0
9:8	CLOCKACTIVITY	Clocks activities during wake-up Bit 8: Interface clock 0x0: Interface clock can be switched-off Bit 9: Functional clock 0x0: Functional clock can be switched-off	R	0x0
7:6	RESERVED	Write 0's for future compatibility. Read returns 0	RW	0x0
5	EMUFREE	Enable sensitivity to MSuspend 0x0: DMA4 freezes its internal logic upon MSuspend assertion 0x1: DMA4 ignores the MSuspend input	RW	0
4:3	SIDLEMODE	Configuration port power management, Idle req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Idle acknowledge is given by DMA4 if all of the conditions are true: 1. All the channels are disabled. 2. If hardware synchronized channel is enabled, then no DMA request input is asserted and no requests are pending to be serviced. 3. All transactions are completed on all the DMA ports. 4.No interrupts are pending to be serviced. 0x3: Reserved. Do not use	RW	0x0
2	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0
1	RESERVED	Reserved for non-GP devices	RW	0
0	AUTOIDLE	Internal interface clock gating strategy 0x0: Interface clock is free running 0x1: Automatic interface clock gating strategy is applied, based on the interface activity.	RW	0

Table 16-29. Register Call Summary for Register DMA4_OCP_SYSCONFIG

DMA_SYSTEM Functional Description

- DMA_SYSTEM Controller Power Management: [0] [1] [2] [3]

DMA_SYSTEM Register Manual

- DMA_SYSTEM Register Summary: [4]

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Table 16-30. DMA4_CAPS_0

Address Offset	0x0000 0064		
Physical Address	0x4A05 6064	**Instance**	DMA_SYSTEM
Description	DMA Capabilities Register 0 LSW		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										LINK_LIST_CPBLTY_TYPE4	LINK_LIST_CPBLTY_TYPE123	CONST_FILL_CPBLTY	TRANSPARENT_BLT_CPBLTY	RESERVED																	

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Write 0's for future compatibility. Read returns 0	RW	0x000
21	LINK_LIST_CPBLTY_TYPE4	Link List capability for type4 descriptor capability	R	0
20	LINK_LIST_CPBLTY_TYPE123	Link List capability for type123 descriptor capability	R	1
19	CONST_FILL_CPBLTY	Constant_Fill_Capability Read 0x0: No LCH supports constant fill copy Read 0x1: any LCH supports constant fill copy	R	1
18	TRANSPARENT_BLT_CPBLTY	Transparent_BLT_Capability Read 0x0: No LCH supports transparent BLT copy Read 0x1: any LCH supports transparent BLT copy	R	1
17:0	RESERVED	Write 0's for future compatibility. Read returns 0	RW	0x00000

Table 16-31. Register Call Summary for Register DMA4_CAPS_0

DMA_SYSTEM Register Manual

- DMA_SYSTEM Register Summary: [0]

Table 16-32. DMA4_CAPS_2

Address Offset	0x0000 006C		
Physical Address	0x4A05 606C	**Instance**	DMA_SYSTEM
Description	DMA Capabilities Register 2		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							SEPARATE_SRC_AND_DST_INDEX_CPBLTY	DST_DOUBLE_INDEX_ADRS_CPBLTY	DST_SINGLE_INDEX_ADRS_CPBLTY	DST_POST_INCRMNT_ADRS_CPBLTY	DST_CONST_ADRS_CPBLTY	SRC_DOUBLE_INDEX_ADRS_CPBLTY	SRC_SINGLE_INDEX_ADRS_CPBLTY	SRC_POST_INCREMENT_ADRS_CPBLTY	SRC_CONST_ADRS_CPBLTY

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Write 0's for future compatibility. Read returns 0	R	0x000000
8	SEPARATE_SRC_AND_DST_INDEX_CPBLTY	Separate_source/destination_index_capability Read 0x0: Does not support separate src/dst index for 2D addressing Read 0x1: Supports separate src/dest index for 2D addressing	R	1
7	DST_DOUBLE_INDEX_ADRS_CPBLTY	Destination_double_index_address_capability Read 0x0: Does not support double index address mode on the destination port Read 0x1: Supports double index address mode on the destination port	R	1
6	DST_SINGLE_INDEX_ADRS_CPBLTY	Destination_single_index_address_capability Read 0x0: Does not support single index address mode on the destination port Read 0x1: Supports single index address mode on the destination port	R	1
5	DST_POST_INCRMNT_ADRS_CPBLTY	Destination_post_increment_address_capability Read 0x0: Does not supports post-increment address mode in the destination port Read 0x1: Supports post-increment address mode in the destination port	R	1
4	DST_CONST_ADRS_CPBLTY	Destination_constant_address_capability Read 0x0: Does not supports constant address mode in the destination port Read 0x1: Supports constant address mode in the destination port	R	1
3	SRC_DOUBLE_INDEX_ADRS_CPBLTY	Source_double_index_address_capability Read 0x0: Does not support double index address mode on the source port Read 0x1: Supports double index address mode on the source port	R	1
2	SRC_SINGLE_INDEX_ADRS_CPBLTY	Source_single_index_address_capability Read 0x0: Does not support single index address mode on the source port Read 0x1: Supports single index address mode in the source port	R	1

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Bits	Field Name	Description	Type	Reset
1	SRC_POST_INCREMENT_ADRS_CPBLTY	Source_post_increment_address_capability Read 0x0: Does not supports post-increment address mode in the source port Read 0x1: Supports post-increment address mode in the source port	R	1
0	SRC_CONST_ADRS_CPBLTY	Source_constant_address_capability Read 0x0: Does not supports constant address mode in the source port Read 0x1: Supports constant address mode in the source port	R	1

Table 16-33. Register Call Summary for Register DMA4_CAPS_2

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [0]

Table 16-34. DMA4_CAPS_3

Address Offset	0x0000 0070		
Physical Address	0x4A05 6070	**Instance**	DMA_SYSTEM
Description	DMA Capabilities Register 3		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BLOCK_SYNCHR_CPBLTY	PKT_SYNCHR_CPBLTY	CHANNEL_CHANINIG_CPBLTY	CHANNEL_INTERLEAVE_CPBLTY	RESERVED		FRAME_SYNCHR_CPBLTY	ELMNT_SYNCHR_CPBLTY

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write 0's for future compatibility. Read returns 0	R	0x000000
7	BLOCK_SYNCHR_CPBLTY	Block_synchronization_capability Read 0x0: Does not support synchronization transfer on block boundary Read 0x1: Supports synchronization transfer on block boundary	R	1
6	PKT_SYNCHR_CPBLTY	Packet_synchronization_capability Read 0x0: Does not support synchronization transfer on packet boundary Read 0x1: Supports synchronization transfer on packet boundary	R	1
5	CHANNEL_CHANINIG_CPBLTY	Channel_Chaninig_capability Read 0x0: Does not support Channel Chaninig capability Read 0x1: Supports Channel Chaninig capability	R	1

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Bits	Field Name	Description	Type	Reset
4	CHANNEL_INTERLEAVE_CPBLTY	Channel_interleave_capability Read 0x0: Does not support Channel interleave capability Read 0x1: Supports Channel_interleave capability	R	1
3:2	RESERVED		R	0x0
1	FRAME_SYNCHR_CPBLTY	Frame_synchronization_capability Read 0x0: Does not support synchronization transfer on Frame boundary Read 0x1: Supports synchronization transfer on Frame boundary	R	1
0	ELMNT_SYNCHR_CPBLTY	Element_synchronization_capability Read 0x0: Does not support synchronization transfer on Element boundary Read 0x1: Supports synchronization transfer on Element boundary	R	1

Table 16-35. Register Call Summary for Register DMA4_CAPS_3

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [0]

Table 16-36. DMA4_CAPS_4

Address Offset	0x0000 0074		
Physical Address	0x4A05 6074	**Instance**	DMA_SYSTEM
Description	DMA Capabilities Register 4		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	EOSB_INTERRUPT_CPBLTY	RESERVED	DRAIN_END_INTERRUPT_CPBLTY	MISALIGNED_ADRS_ERR_INTERRUPT_CPBLTY	SUPERVISOR_ERR_INTERRUPT_CPBLTY	RESERVED	TRANS_ERR_INTERRUPT_CPBLTY	PKT_INTERRUPT_CPBLTY	SYNC_STATUS_CPBLTY	BLOCK_INTERRUPT_CPBLTY	LAST_FRAME_INTERRUPT_CPBLTY	FRAME_INTERRUPT_CPBLTY	HALF_FRAME_INTERRUPT_CPBLTY	EVENT_DROP_INTERRUPT_CPBLTY	RESERVED

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00000
14	EOSB_INTERRUPT_CPBLTY	End of Super Block detection capability.	R	1
13	RESERVED	Reserved for non-GP devices	R	1
12	DRAIN_END_INTERRUPT_CPBLTY	Drain End detection capability.	R	1
11	MISALIGNED_ADRS_ERR_INTERRUPT_CPBLTY	Misaligned error detection capability.	R	1

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Bits	Field Name	Description	Type	Reset
10	SUPERVISOR_ERR_INTERRUPT_CPBLTY	Supervisor error detection capability.	R	1
9	RESERVED	Reserved for non-GP devices	R	1
8	TRANS_ERR_INTERRUPT_CPBLTY	Transaction error detection capability.	R	1
7	PKT_INTERRUPT_CPBLTY	End of Packet detection capability. Read 0x0: Does not support end of packet interrupt generation capability Read 0x1: Supports end of packet interrupt generation capability	R	1
6	SYNC_STATUS_CPBLTY	Sync_status_capability Read 0x0: Does not support synchronized transfer status bit generation Read 0x1: Supports synchronized transfer status bit generation	R	1
5	BLOCK_INTERRUPT_CPBLTY	End of block detection capability. Read 0x0: Does not support end of block interrupt generation capability Read 0x1: Supports end of block interrupt generation capability	R	1
4	LAST_FRAME_INTERRUPT_CPBLTY	Start of last frame detection capability. Read 0x0: Does not support last frame interrupt generation capability Read 0x1: Supports last frame interrupt generation capability	R	1
3	FRAME_INTERRUPT_CPBLTY	End of frame detection capability. Read 0x0: Does not support end of frame interrupt generation capability Read 0x1: Supports end of frame interrupt generation capability	R	1
2	HALF_FRAME_INTERRUPT_CPBLTY	Detection capability of the half of frame end. Read 0x0: Does not support half of frame interrupt generation capability Read 0x1: Supports half of frame interrupt generation capability	R	1
1	EVENT_DROP_INTERRUPT_CPBLTY	Request collision detection capability. Read 0x0: Does not support event drop interrupt generation capability Read 0x1: Supports event drop interrupt generation capability	R	1
0	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0

Table 16-37. Register Call Summary for Register DMA4_CAPS_4

DMA_SYSTEM Register Manual

- DMA_SYSTEM Register Summary: [0]

Table 16-38. DMA4_GCR

Address Offset	0x0000 0078		
Physical Address	0x4A05 6078	**Instance**	DMA_SYSTEM
Description	FIFO sharing between high and low priority channel. The Maximum per channel FIFO depth is bounded by the low and high channel FIFO budget. The high respectively low priority channels maximum burst size must be less than the min (high respectively low priority channel FIFO budget , per channel maximum FIFO depth)		
Type	RW		

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	CHANNEL_ID_GATE	ARBITRATION_RATE	HI_LO_FIFO_BUDGET	HI_THREAD_RESERVED	RESERVED	MAX_CHANNEL_FIFO_DEPTH

Bits	Field Name	Description	Type	Reset
31:25	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00
24	CHANNEL_ID_GATE	Gates the Channel ID bus monitoring on both Read and Write ports 0x0: Gates the Channel ID qualifiers on both Read and Write Ports 0x1: Does not gate the Channel ID qualifiers on both Read and Write Ports	RW	0x0
23:16	ARBITRATION_RATE	Arbitration switching rate between prioritized and regular channel queues	RW	0x01
15:14	HI_LO_FIFO_BUDGET	Allow to have a separate Global FIFO budget for high and low priority channels. For Hi priority Channel: (Per_channel_Maximum FIFO depth + 1) x Number of active High priority Channel =< High Budget FIFO For Low priority channel: (Per_channel_Maximum FIFO depth + 1) x Number of active Low priority Channel =< Low Budget FIFO 0x0: no fixed budget for neither higher nor lower priority channel 0x1: 75% of FIFO for low priority and 25% for high priority channels 0x2: 25% of FIFO for low priority and 75% for high priority channels 0x3: 50% of FIFO for low priority and 50% for high priority channels	RW	0x0
13:12	HI_THREAD_RESERVED	Allow thread reservation for high priority channel on both read and write ports. 0x0: No ThreadID is reserved on the Read Port for high priority channels. No ThreadID is reserved on the Write Port for high priority channels. 0x1: Read Port ThreadID 0 is reserved for high priority channels. Write Port ThreadID 0 is reserved for high priority channels. 0x2: Read port ThreadID 0 and ThreadID 1 are reserved for high priority channels. Write Port ThreadID 0 is reserved for high priority channels. 0x3: Read PortThreadID 0, ThreadID 1 and ThreadID 2 are reserved for high priority channels. Write Port ThreadID 0 is reserved for high priority channels.	RW	0x0
11:8	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0
7:0	MAX_CHANNEL_FIFO_DEPTH	Maximum FIFO depth allocated to one logical channel. Maximum FIFO depth can not be 0x0. It should be at least 0x1 or greater. Note that If channel limit is less than destination burst size enough data will not be accumulated in the data FIFO and it will never be sent out on the WR port. The burst size should be less than the FIFO limit specified in this bit field.	RW	0x10

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Table 16-39. Register Call Summary for Register DMA4_GCR

DMA_SYSTEM Functional Description

- Logical Channel Transfer Overview: [0] [1] [2]
- FIFO Queue Memory Pool: [3]
- Thread Budget Allocation: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- FIFO Budget Allocation: [15] [16]

DMA_SYSTEM Basic Programming Model

- Setup Configuration: [17]
- Concurrent Software and Hardware Synchronization: [18]

DMA_SYSTEM Register Manual

- DMA_SYSTEM Register Summary: [19]

Table 16-40. DMA4_CCRi

Address Offset	0x0000 0080 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6080 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RESERVED			WRITE_PRIORITY	BUFFERING_DISABLE	SEL_SRC_DST_SYNC	PREFETCH	SUPERVISOR	RESERVED	SYNCHRO_CONTROL_UPPER		BS	TRANSPARENT_COPY_ENABLE	CONST_FILL_ENABLE	DST_AMODE		SRC_AMODE		RESERVED	WR_ACTIVE	RD_ACTIVE	SUSPEND_SENSITIVE	ENABLE	READ_PRIORITY	FS	SYNCHRO_CONTROL				

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0
29:27	RESERVED	Reserved for non-GP devices	RW	0x0
26	WRITE_PRIORITY	Channel priority on the Write side 0x0: Channel has low priority on the write side during the arbitration process. 0x1: Channel has high priority on write sided during the arbitration process.	RW	0
25	BUFFERING_DISABLE	This bit allows to disable the default buffering functionality when transfer is source synchronized. 0x0: Buffering is enabled across element/packet when source is synchronized to element, packet, frame or blocks. 0x1: Buffering is disabled across element/packet when source is synchronized to element, packet, frame or blocks.	RW	-

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Bits	Field Name	Description	Type	Reset
24	SEL_SRC_DST_SYNC	Specifies that element, packet, frame or block transfer (depending on CCR.bs and CCR.fs) is triggered by the source or the destination on the DMA request 0x0: Transfer is triggered by the destination. If synch on packet the packet element number is specified in the CDFI register. 0x1: Transfer is triggered by the source. If synchronized on packet the packet element number is specified in the CSFI register.	RW	-
23	PREFETCH	Enables the prefetch mode 0x0: Prefetch mode is disabled. When Sel_Src_Dst_Sync=1 transfers are buffered and pipelined between DMA requests. 0x1: Prefetch mode is enabled. Prefetch mode is active only when destination is synchronized. It is software user responsibility not to have at the same time Prefetch=1 when Sel_Src_Dst_Sync=1. This mode is not supported.	RW	0
22	SUPERVISOR	Enables the supervisor mode 0x0: Supervisor mode is disabled. 0x1: Supervisor mode is enabled.	RW	0
21	RESERVED	Reserved for non-GP devices	RW	0
20:19	SYNCHRO_CONTROL_UPPER	Channel Synchronization control upper (used in conjunction with the 5 bits of synchro channel DMA4_CCRi[4:0]) Used in conjunction, as 2 MSB, with the 5 bits of the synchro channel bit field.	RW	0b00
18	BS	Block synchronization This bit used in conjunction with the fs to see how the DMA request is serviced in a synchronized transfer.	RW	-
17	TRANSPARENT_COPY_ENABLE	Transparent copy enable 0x0: Transparent copy mode is disabled. 0x1: Transparent copy mode is enabled.	RW	-
16	CONST_FILL_ENABLE	Constant fill enable 0x0: Constant fill mode is disabled. 0x1: Constant fill mode is enabled.	RW	0
15:14	DST_AMODE	Selects the addressing mode on the Write Port of a channel. 0x0: Constant address mode 0x1: Post-incremented address mode 0x2: Single index address mode 0x3: Double index address mode	RW	0bxx
13:12	SRC_AMODE	Selects the addressing mode on the Read Port of a channel. 0x0: Constant address mode 0x1: Post-incremented address mode 0x2: Single index address mode 0x3: Double index address mode	RW	0bxx
11	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
10	WR_ACTIVE	Indicates if the channel write context is active or not Read 0x0: Channel is not active on the write port. Read 0x1: Channel is currently active on the write port.	R	0
9	RD_ACTIVE	Indicates if the channel read context is active or not Read 0x0: Channel is not active on the read port. Read 0x1: Channel is currently active on the read port.	R	0

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Bits	Field Name	Description	Type	Reset
8	SUSPEND_SENSITIVE	Logical channel suspend enable bit 0x0: The channel ignores the MSuspend even if EMUFree is set to 0. 0x1: If EMUFree is set to 0 and MSuspend comes in then all current OCP services (single transaction or burst transaction as specified in the corresponding CSDP register) have to be completed before stopping processing any more transactions.	RW	0
7	ENABLE	Logical channel enable. It is SW responsibility to clear the CSR register and the IRQSTATUS bit for the different interrupt lines before enabling the channel. 0x0: The logical channel is disabled. 0x1: The logical channel is enabled.	RW	0
6	READ_PRIORITY	Channel priority on the read side 0x0: Channel has low priority on the read side during the arbitration process. 0x1: Channel has high priority on read sided during the arbitration process.	RW	0
5	FS	Frame synchronization This bit used in conjunction with the BS to see how the DMA request is serviced in a synchronized transfer FS = 0 and BS = 0: An element is transferred once a DMA request is made. FS = 0 and BS = 1: An entire block is transferred once a DMA request is made. FS = 1 and BS = 0: An entire frame is transferred once a DMA request is made. FS = 1 and BS = 1: A packet is transferred once a DMA request is made. All these different transfers can be interleaved on the port with other DMA requests.	RW	-
4:0	SYNCHRO_CONTROL	Channel synchronization control This bit field used in conjunction with the second_level_ synchro_control_upper (as 2 MSB) 0000000 : Is reserved for non synchronized LCH transfer xxxxxxx (from 1 to 127)There are 127 possible DMA request to assign to any LCH. **Note:** The channel synchronization control registers are 1-based. For example, to enable the S_DMA_1 request, DMA4_CCR[4:0] SYNCHRO_CONTROL must be set to 0x2 (DMA request number + 1).	RW	0b00000

Table 16-41. Register Call Summary for Register DMA4_CCRi

DMA_SYSTEM Functional Description

- Interrupt Generation: [0]
- Logical Channel Transfer Overview: [1] [2] [3]
- Addressing Modes: [4]
- Software Synchronization: [5] [6] [7]
- Hardware Synchronization: [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19]
- Thread Budget Allocation: [20] [21]
- Reprogramming an Active Channel: [22] [23] [24] [25]
- Packet Synchronization: [26] [27] [28] [29] [30]
- Graphics Acceleration Support: [31]
- Supervisor Modes: [32]
- Disabling a Channel During Transfer: [33]
- FIFO Draining Mechanism: [34] [35] [36] [37] [38]
- Descriptors: [39] [40]
- Linked-List Control and Monitoring: [41] [42] [43] [44] [45] [46] [47] [48] [49] [50]

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Table 16-41. Register Call Summary for Register DMA4_CCRi (continued)

DMA_SYSTEM Basic Programming Model

- Software-Triggered (Nonsynchronized) Transfer: [51] [52] [53] [54] [55] [56] [57] [58] [59]
- Hardware-Synchronized Transfer: [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74] [75] [76] [77] [78] [79] [80] [81] [82] [83] [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95] [96] [97] [98]
- Concurrent Software and Hardware Synchronization: [99] [100]
- Chained Transfer: [101]
- 90-Degree Clockwise Image Rotation: [102] [103] [104] [105] [106] [107] [108]
- Graphic Operations: [109] [110] [111] [112]
- Linked-List Programming Guidelines: [113] [114] [115] [116]

DMA_SYSTEM Register Manual

- DMA_SYSTEM Register Summary: [117]
- DMA_SYSTEM Register Description: [118]

Table 16-42. DMA4_CLNK_CTRLi

Address Offset	0x0000 0084 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6084 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Link Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ENABLE_LNK	RESERVED							NEXTLCH_ID							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15	ENABLE_LNK	Enables or disable the channel linking. 0x0: Channel linking mode is disabled When set on the fly to 0 the current channel will complete the transfer and stops the chain linking 0x1: Channel linking mode is enabled. The logical channel defined in the NextLCH_ID is enabled at the end of the current transfer	RW	0
14:5	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x000
4:0	NEXTLCH_ID	Defines the NextLCh_ID, which is used to build logical channel chaining queue.	RW	0bxxxxx

Table 16-43. Register Call Summary for Register DMA4_CLNK_CTRLi

DMA_SYSTEM Functional Description

- Chained Logical Channel Transfers: [0] [1]
- FIFO Draining Mechanism: [2]
- Descriptors: [3]
- Linked-List Control and Monitoring: [4] [5] [6] [7]

DMA_SYSTEM Basic Programming Model

- Chained Transfer: [8] [9] [10] [11] [12]
- Linked-List Programming Guidelines: [13] [14]

DMA_SYSTEM Register Manual

- DMA_SYSTEM Register Summary: [15]

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Table 16-44. DMA4_CICRi

Address Offset	0x0000 0088 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6088 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Interrupt Control Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	SUPER_BLOCK_IE	RESERVED	DRAIN_IE	MISALIGNED_ERR_IE	SUPERVISOR_ERR_IE	RESERVED	TRANS_ERR_IE	PKT_IE	RESERVED	BLOCK_IE	LAST_IE	FRAME_IE	HALF_IE	DROP_IE	RESERVED

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00000
14	SUPER_BLOCK_IE	Enables the end of super block interrupt	RW	-
13	RESERVED	Reserved for non-GP devices	RW	1
12	DRAIN_IE	Enables the end of draining interrupt	RW	0
11	MISALIGNED_ERR_IE	Enables the address misaligned error event interrupt 0x0: Disables the misaligned address error event interrupt 0x1: Enables the misaligned address error event interrupt	RW	-
10	SUPERVISOR_ERR_IE	Enables the supervisor transaction error event interrupt 0x0: Disables the supervisor transaction error event interrupt 0x1: Enables the supervisor transaction error event interrupt	RW	1
9	RESERVED	Reserved for non-GP devices	RW	1
8	TRANS_ERR_IE	Enables the transaction error event interrupt 0x0: Disables the transaction error event interrupt 0x1: Enables the transaction error event interrupt	RW	-
7	PKT_IE	Enables the end of Packet interrupt 0x0: Disables the end of Packet transfer interrupt 0x1: Enables the end of Packet transfer interrupt	RW	-
6	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
5	BLOCK_IE	Enables the end of block interrupt 0x0: Disables the end of block interrupt 0x1: Disables the end of block interrupt	RW	-
4	LAST_IE	Last frame interrupt enable (start of last frame) 0x0: Disables the last frame interrupt 0x1: Enables the last frame interrupt	RW	-
3	FRAME_IE	Frame interrupt enable (end of frame) 0x0: Disables the end of frame interrupt 0x1: Enables the end of frame interrupt	RW	-
2	HALF_IE	Enables or disables the half frame interrupt. 0x0: Disables the half frame interrupt 0x1: Enables the half frame interrupt	RW	-

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Bits	Field Name	Description	Type	Reset
1	DROP_IE	Synchronization event drop interrupt enable (request collision) 0x0: Disables the event drop interrupt 0x1: Enables the event drop interrupt	RW	0
0	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0

Table 16-45. Register Call Summary for Register DMA4_CICRi

DMA_SYSTEM Functional Description
- DMA_SYSTEM Controller Interrupt Requests: [0] [1]
- Interrupt Generation: [2]
- FIFO Draining Mechanism: [3]
- Descriptors: [4] [5] [6]
- Linked-List Control and Monitoring: [7] [8] [9]

DMA_SYSTEM Basic Programming Model
- Setup Configuration: [10]
- Linked-List Programming Guidelines: [11]

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [12]

Table 16-46. DMA4_CSRi

Address Offset	0x0000 008C + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 608C + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Status Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED	SUPER_BLOCK	RESERVED	DRAIN_END	MISALIGNED_ADRS_ERR	SUPERVISOR_ERR	RESERVED	TRANS_ERR	PKT	SYNC	BLOCK	LAST	FRAME	HALF	DROP	RESERVED

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
16:15	RESERVED	Reserved for debug (Monitor descriptor/data load phase), Write 0's for future compatibility, Read returns 0	RW	0x0
14	SUPER_BLOCK	End of Super block event Read 0x0: The current Super block transfer has not been finished Write 0x0: Status bit unchanged Read 0x1: The current Super block has been transferred Write 0x1: Status bit is reset	RW W1toClr	0
13	RESERVED	Reserved for non-GP devices	RW	0

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Bits	Field Name	Description	Type	Reset
12	DRAIN_END	End of channel draining Read 0x0: No drain end in the current transfer Write 0x0: Status bit unchanged Read 0x1: The current channel draining is completed Write 0x1: Status bit is reset	RW W1toClr	0
11	MISALIGNED_ADRS_ERR	Misaligned address error event Read 0x0: No address error Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: An address error has been occurred	RW W1toClr	0
10	SUPERVISOR_ERR	Supervisor transaction error event Read 0x0: No supervisor transaction error Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: A supervisor transaction error has been occurred	RW W1toClr	0
9	RESERVED	Reserved for non-GP devices	RW	0
8	TRANS_ERR	Transaction error event Read 0x0: No transaction error Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: A transaction error has been occurred	RW W1toClr	0
7	PKT	End of Packet transfer Read 0x0: The current packet transfer has not been finished Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The current packet has been transferred	RW W1toClr	0
6	SYNC	Synchronization status of a channel. Read 0x0: Logical channel is not scheduled or servicing a non synchronized DMA request. Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: Logical channel is servicing a synchronized DMA request	RW W1toClr	0
5	BLOCK	End of block event Read 0x0: The current block transfer has not been finished Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The current block has been transferred	RW W1toClr	0
4	LAST	Last frame (start of last frame) Read 0x0: The start of the last frame to transfer is not reached Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The start of the last frame to transfer is reached	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
3	FRAME	End of frame event Read 0x0: The end of current transferred frame is not reached Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The end of current transferred frame is reached	RW W1toClr	0
2	HALF	Half of frame event. Read 0x0: The half of current transferred frame is not reached Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: The half of current transferred frame is reached	RW W1toClr	0
1	DROP	Synchronization event drop occured during the transfer Read 0x0: No synchronization collision Write 0x0: Status bit unchanged Write 0x1: Status bit is reset Read 0x1: A synchronization collision has been occurred	RW W1toClr	0
0	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0

Table 16-47. Register Call Summary for Register DMA4_CSRi

DMA_SYSTEM Functional Description • DMA_SYSTEM Controller Interrupt Requests: [0] [1] [2] [3] [4] • Interrupt Generation: [5] • FIFO Draining Mechanism: [6] • Linked-List Control and Monitoring: [7] [8] [9] [10] [11]
DMA_SYSTEM Basic Programming Model • Setup Configuration: [12]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [13]

Table 16-48. DMA4_CSDPi

Address Offset	0x0000 0090 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6090 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Source Destination Parameters		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SRC_ENDIAN	SRC_ENDIAN_LOCK	DST_ENDIAN	DST_ENDIAN_LOCK	WRITE_MODE		DST_BURST_EN		DST_PACKED	RESERVED					SRC_BURST_EN		SRC_PACKED	RESERVED				DATA_TYPE		

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Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x000
21	SRC_ENDIAN	Channel source endianness control 0x0: Source has Little Endian type 0x1: Source has Big Endian type	RW	-
20	SRC_ENDIAN_LOCK	Endianness Lock 0x0: Endianness adapt 0x1: Endianness lock	RW	-
19	DST_ENDIAN	Channel Destination endianness control 0x0: Destination has Little Endian type 0x1: Destination has Big Endian type	RW	-
18	DST_ENDIAN_LOCK	Endianness Lock 0x0: Endianness adapt 0x1: Endianness lock	RW	-
17:16	WRITE_MODE	Used to enable writing mode without posting or with posting 0x0: Write None Posted (WRNP) 0x1: Write (Posted) 0x2: All transaction are mapped on the Write command as posted except for the last transaction in the transfer mapped on a Write None Posted 0x3: Undefined	RW	0bxx
15:14	DST_BURST_EN	Used to enable bursting on the Write Port. Smaller burst size than the programmed burst size is also allowed 0x0: single access 0x1: 16 bytes or 4x32-bit / 2x64-bit burst access 0x2: 32 bytes or 8x32-bit / 4x64-bit burst access 0x3: 64 bytes or 16x32-bit / 8x64-bit burst access	RW	0b00
13	DST_PACKED	Destination receives packed data. 0x0: The destination target is non packed 0x1: The destination target is packed	RW	-
12:9	RESERVED	Write the reset value. Read returns reset value	RW	0x-
8:7	SRC_BURST_EN	Used to enable bursting on the Read Port. Smaller burst size than the programmed burst size is also allowed 0x0: single access 0x1: 16 bytes or 4x32-bit / 2x64-bit burst access 0x2: 32 bytes or 8x32-bit / 4x64-bit burst access 0x3: 64 bytes or 16x32-bit / 8x64-bit burst access	RW	0bxx
6	SRC_PACKED	Source provides packed data. 0x0: The source target is non packed 0x1: The source target is packed	RW	-
5:2	RESERVED	Write the reset value. Read returns reset value	RW	0x-
1:0	DATA_TYPE	Defines the type of the data moved in the channel. 0x0: 8 bits scalar 0x1: 16 bits scalar 0x2: 32 bits scalar 0x3: Reserved	RW	0bxx

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Table 16-49. Register Call Summary for Register DMA4_CSDPi

DMA_SYSTEM Functional Description • Addressing Modes: [0] • Packed Accesses: [1] • Burst Transactions: [2] • Endianism Conversion: [3] [4] • Hardware Synchronization: [5] • Graphics Acceleration Support: [6] • Posted and Nonposted Writes: [7] • Descriptors: [8]
DMA_SYSTEM Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [9] [10] [11] [12] [13] [14] [15] [16] [17] • Hardware-Synchronized Transfer: [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] • 90-Degree Clockwise Image Rotation: [30] [31] [32] [33] [34] [35] [36] [37] [38] • Linked-List Programming Guidelines: [39] [40]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [41]

Table 16-50. DMA4_CENi

Address Offset	0x0000 0094 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6094 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Element Number		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CHANNEL_ELMNT_NBR																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00
23:0	CHANNEL_ELMNT_NBR	Number of elements within a frame (unsigned) to transfer	RW	0x------

Table 16-51. Register Call Summary for Register DMA4_CENi

DMA_SYSTEM Functional Description • Addressing Modes: [0] [1]
DMA_SYSTEM Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [2] • Hardware-Synchronized Transfer: [3] [4] [5] • 90-Degree Clockwise Image Rotation: [6]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [7]

Table 16-52. DMA4_CFNi

Address Offset	0x0000 0098 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 6098 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Frame Number		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CHANNEL_FRAME_NBR															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15:0	CHANNEL_FRAME_NBR	Number of frames within the block to be transferred (unsigned)	RW	0x----

Table 16-53. Register Call Summary for Register DMA4_CFNi

DMA_SYSTEM Functional Description • Addressing Modes: [0] [1]
DMA_SYSTEM Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [2] • Hardware-Synchronized Transfer: [3] [4] • 90-Degree Clockwise Image Rotation: [5] • Linked-List Programming Guidelines: [6]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [7]

Table 16-54. DMA4_CSSAi

Address Offset	0x0000 009C + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 609C + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Source Start Address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_START_ADRS																															

Bits	Field Name	Description	Type	Reset
31:0	SRC_START_ADRS	32 bits of the source start address	RW	0x--------

Table 16-55. Register Call Summary for Register DMA4_CSSAi

DMA_SYSTEM Functional Description • Addressing Modes: [0]
DMA_SYSTEM Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [1] • Hardware-Synchronized Transfer: [2] [3] [4] [5] • 90-Degree Clockwise Image Rotation: [6]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [7]

Table 16-56. DMA4_CDSAi

Address Offset	0x0000 00A0 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60A0 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Destination Start Address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST_START_ADRS																															

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Bits	Field Name	Description	Type	Reset
31:0	DST_START_ADRS	32 bits of the destination start address	RW	0x--------

Table 16-57. Register Call Summary for Register DMA4_CDSAi

DMA_SYSTEM Functional Description • Addressing Modes: [0]
DMA_SYSTEM Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [1] • Hardware-Synchronized Transfer: [2] [3] [4] [5] • 90-Degree Clockwise Image Rotation: [6]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [7]

Table 16-58. DMA4_CSEIi

Address Offset	0x0000 00A4 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60A4 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Source Element Index (Signed)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CHANNEL_SRC_ELMNT_INDEX															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15:0	CHANNEL_SRC_ELMNT_INDEX	Channel source element index	RW	0x----

Table 16-59. Register Call Summary for Register DMA4_CSEIi

DMA_SYSTEM Functional Description • Addressing Modes: [0]
DMA_SYSTEM Basic Programming Model • Software-Triggered (Nonsynchronized) Transfer: [1] • 90-Degree Clockwise Image Rotation: [2]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [3]

Table 16-60. DMA4_CSFIi

Address Offset	0x0000 00A8 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60A8 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Source Frame Index (Signed) or 16-bit Packet size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH_SRC_FRM_INDEX_OR_16BIT_PKT_ELNT_NBR																															

Bits	Field Name	Description	Type	Reset
31:0	CH_SRC_FRM_INDEX_OR_16BIT_PKT_ELNT_NBR	Channel source frame index value if source address is in double index mode. Or if fs=bs=1 and DMA_CCR[SEL_SRC_DST_SYNC] = 1; the bit field [15:0] gives the number of element in packet. The field [31:16] is unused for the packet size.	RW	0x--------

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Table 16-61. Register Call Summary for Register DMA4_CSFIi

DMA_SYSTEM Functional Description
- Addressing Modes: [0]
- Hardware Synchronization: [1]
- Packet Synchronization: [2] [3] [4] [5] [6]

DMA_SYSTEM Basic Programming Model
- Software-Triggered (Nonsynchronized) Transfer: [7]
- Hardware-Synchronized Transfer: [8] [9]
- 90-Degree Clockwise Image Rotation: [10]

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [11]

Table 16-62. DMA4_CDEIi

Address Offset	0x0000 00AC + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60AC + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Destination Element Index (Signed)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CHANNEL_DST_ELMNT_INDEX															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15:0	CHANNEL_DST_ELMNT_INDEX	Channel destination element index	RW	0x----

Table 16-63. Register Call Summary for Register DMA4_CDEIi

DMA_SYSTEM Functional Description
- Addressing Modes: [0]

DMA_SYSTEM Basic Programming Model
- Software-Triggered (Nonsynchronized) Transfer: [1]
- 90-Degree Clockwise Image Rotation: [2]

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [3]

Table 16-64. DMA4_CDFIi

Address Offset	0x0000 00B0 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60B0 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Destination Frame Index (Signed) or 16-bit Packet size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH_DST_FRM_IDX_OR_16BIT_PKT_ELNT_NBR																															

Bits	Field Name	Description	Type	Reset
31:0	CH_DST_FRM_IDX_OR_16BIT_PKT_ELNT_NBR	Channel destination frame index value if destination address is in double index mode. Or if fs=bs=1 and DMA_CCR[SEL_SRC_DST_SYNC]=0; the bit field [15:0] gives the number of element in packet. The field [31:16] is unused for the packet size..	RW	0x--------

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Table 16-65. Register Call Summary for Register DMA4_CDFIi

DMA_SYSTEM Functional Description
- Addressing Modes: [0]
- Hardware Synchronization: [1]
- Packet Synchronization: [2] [3] [4] [5] [6]

DMA_SYSTEM Basic Programming Model
- Software-Triggered (Nonsynchronized) Transfer: [7]
- Hardware-Synchronized Transfer: [8] [9]
- 90-Degree Clockwise Image Rotation: [10]

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [11]

Table 16-66. DMA4_CSACi

Address Offset	0x0000 00B4 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60B4 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Source Address Value. User has to access this register only in 32-bit access. If accessed in 8-bit or 16bit data may be corrupted.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_ELMNT_ADRS																															

Bits	Field Name	Description	Type	Reset
31:0	SRC_ELMNT_ADRS	Current source address counter value	R	0x--------

Table 16-67. Register Call Summary for Register DMA4_CSACi

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [0]

Table 16-68. DMA4_CDACi

Address Offset	0x0000 00B8 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60B8 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Destination Address Value. User has to access this register only in 32-bit access. If accessed in 8-bit or 16bit data may be corrupted.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DST_ELMNT_ADRS																															

Bits	Field Name	Description	Type	Reset
31:0	DST_ELMNT_ADRS	Current destination address counter value	RW	0x--------

Table 16-69. Register Call Summary for Register DMA4_CDACi

DMA_SYSTEM Functional Description
- Hardware Synchronization: [0]

DMA_SYSTEM Basic Programming Model
- Hardware-Synchronized Transfer: [1]
- Synchronized Transfer Monitoring Using CDAC: [2] [3] [4] [5] [6] [7] [8]

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [9]

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Table 16-70. DMA4_CCENi

Address Offset	0x0000 00BC + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60BC + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Current Transferred Element Number in the current frame. User has to access this register only in 32-bit access. If accessed in 8-bit or 16bit data may be corrupted.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CURRENT_ELMNT_NBR																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x00
23:0	CURRENT_ELMNT_NBR	Channel current transferred element number in the current frame	RW	0x------

Table 16-71. Register Call Summary for Register DMA4_CCENi

DMA_SYSTEM Functional Description • Linked-List Control and Monitoring: [0] [1] [2]
DMA_SYSTEM Basic Programming Model • Synchronized Transfer Monitoring Using CDAC: [3]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [4]

Table 16-72. DMA4_CCFNi

Address Offset	0x0000 00C0 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60C0 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel Current Transferred Frame Number in the current transfer. User has to access this register only in 32-bit access. If accessed in 8-bit or 16bit data may be corrupted.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CURRENT_FRAME_NBR															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x0000
15:0	CURRENT_FRAME_NBR	Channel current transferred frame number in the current transfer	RW	0x----

Table 16-73. Register Call Summary for Register DMA4_CCFNi

DMA_SYSTEM Functional Description • Linked-List Control and Monitoring: [0] [1] [2]
DMA_SYSTEM Basic Programming Model • Synchronized Transfer Monitoring Using CDAC: [3]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [4]

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Table 16-74. DMA4_COLORi

Address Offset	0x0000 00C4 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60C4 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	Channel DMA COLOR KEY /SOLID COLOR		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CH_BLT_FRGRND_COLOR_OR_SOLID_COLOR_PTRN																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0x–
23:0	CH_BLT_FRGRND_COLOR_OR_SOLID_COLOR_PTRN	Color key or solid color pattern: The pattern is replicated according to the data type. If the data-type is 8-bit the pattern is replicated 4 times to fill the register in order to enhance processing when data is packed at the graphic module input. The same reasoning for 16-bit data-type.	RW	0x------

Table 16-75. Register Call Summary for Register DMA4_COLORi

DMA_SYSTEM Functional Description
- Graphics Acceleration Support: [0] [1]
- Descriptors: [2]

DMA_SYSTEM Basic Programming Model
- Graphic Operations: [3] [4]

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [5]

Table 16-76. DMA4_CDPi

Address Offset	0x0000 00D0 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60D0 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	This register controls the various parameters of the link list mechanism		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					FAST	TRANSFER_MODE		PAUSE_LINK_LIST	NEXT_DESCRIPTOR_TYPE				SRC_VALID		DEST_VALID

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0x00000
10	FAST	Sets the fast-start mode for linked list descriptor types 1, 2 and 3 0x0: No fast-start mode 0x1: Fast-start mode is enabled.	RW	0x0

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Bits	Field Name	Description	Type	Reset
9:8	TRANSFER_MODE	Enable linked-list transfer mode 0x0: Normal transfer mode is used. 0x1: Linked-list channel mode for type 1, 2, or 3 descriptor is used. 0x2: Undefined 0x3: Undefined	RW	0x0
7	PAUSE_LINK_LIST	Suspend the linked-list transfer at completion of the current block transfer. 0x0: Linked list is active. 0x1: Linked list is suspended at the boundary of next descriptor loading.	RW	0x0
6:4	NEXT_DESCRIPTOR_TYPE	Next Descriptor Type 0x0: Undefined 0x1: Next descriptor is of type 1. 0x2: Next descriptor is of type 2. 0x3: Next descriptor is of type 3. 0x4: Undefined 0x5: Undefined 0x6: Undefined 0x7: Undefined	RW	0x-
3:2	SRC_VALID	Source address valid 0x0: The source address is not present in the next descriptor and continuous incrementing is enabled. 0x1: The source address must be reloaded in the next descriptor transfer. 0x2: The source start address is not present in the next descriptor. But will reload the one from configuration memory which belongs to the previous descriptor. 0x3: Undefined addressing mode	RW	0x-
1:0	DEST_VALID	Destination address valid 0x0: The destination address is not present in the next descriptor and continuous incrementing is enabled. 0x1: The destination address must be reloaded in the next descriptor transfer. 0x2: The destination start address is not present in the next descriptor. But will reload the one from configuration memory which belongs to the previous descriptor. 0x3: Undefined addressing mode	RW	0x-

Table 16-77. Register Call Summary for Register DMA4_CDPi

DMA_SYSTEM Functional Description • Link-List Transfer Profile: [0] • Descriptors: [1] [2] • Linked-List Control and Monitoring: [3] [4] [5] [6] [7] [8] [9] [10] [11]
DMA_SYSTEM Basic Programming Model • Linked-List Programming Guidelines: [12]
DMA_SYSTEM Register Manual • DMA_SYSTEM Register Summary: [13]

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Table 16-78. DMA4_CNDPi

Address Offset	0x0000 00D4 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60D4 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description	This register contains the Next descriptor Address Pointer for the link list Mechanism		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_DESCRIPTOR_POINTER																														RESERVED	

Bits	Field Name	Description	Type	Reset
31:2	NEXT_DESCRIPTOR_POINTER	This register contains the Next descriptor Address Pointer for the link list Mechanism	RW	0bxxxxxxxxxxxxxxxx xxxxxxxxxxxx
1:0	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0x0

Table 16-79. Register Call Summary for Register DMA4_CNDPi

DMA_SYSTEM Functional Description
- Link-List Transfer Profile: [0]

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [1]

Table 16-80. DMA4_CCDNi

Address Offset	0x0000 00D8 + (0x60 * i)	**index:**	i = 0 to 31
Physical Address	0x4A05 60D8 + (0x60 * i)	**Instance**	DMA_SYSTEM
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CURRENT_DESCRIPTOR_NBR															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility, Reads return 0	RW	0x0000
15:0	CURRENT_DESCRIPTOR_NBR	This register when read contains the current active descriptor number in the link list. This register is Read/write to allow user initialization.	RW	0x----

Table 16-81. Register Call Summary for Register DMA4_CCDNi

DMA_SYSTEM Functional Description
- Linked-List Control and Monitoring: [0] [1] [2]

DMA_SYSTEM Register Manual
- DMA_SYSTEM Register Summary: [3]

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Interrupt Controllers

This chapter describes the interrupt controllers (INTCs) in the device.

NOTE: Some of the interrupt controllers features, primarily those concerning the device I/O pads and the interrupt controllers integration, are not available in all OMAP54xx devices.

For details, see , *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

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17.1 Interrupt Controllers Overview

The device provides three INTC modules, which handle interrupts at the device level:

- Microprocessor unit (MPU) subsystem (dual Cortex™-A15) interrupt controller (INTC_MPU): This INTC module is a single functional unit that is integrated in the Cortex-A15 multiprocessor core alongside Cortex-A15 processors. It provides:
  - 160 hardware interrupt inputs
  - Generation of interrupts by software
  - Prioritization of interrupts
  - Masking of any interrupts
  - Distribution of the interrupts to the target Cortex-A15 processor(s)
  - Tracking the status of interrupts
  - Support for virtualization extensions
  - Wake-up generator (WUGEN_MPU) module on external and local interrupts
- Digital signal processor (DSP) subsystem interrupt controller (INTC_DSP): This module is a specific combination of wake-up generator (WUGEN_DSP) and the C64x+ INTC_DSP. The INTC_DSP is used in the device but not described in detail in this chapter. For detailed information about this module, see DSP Subsystem.
- Interrupt processor unit (IPU) subsystem (dual Cortex-M4) interrupt controller (INTC_IPU): This module is also called nested vectored interrupt controller (NVIC) and is integrated within each Cortex-M4 core so the different interrupt lines are directly connected to each core. The interrupt mapping is the same for the two cores to facilitate parallel processing. INTC_IPU supports:
  - 64 external interrupts (in addition to 16 Cortex-M4 internal interrupts), which are dynamically prioritized with 16 levels of priority defined for each core
  - Low-latency exception and interrupt handling
  - Prioritization and handling of exceptions
  - Control of the local power management
  - Debug accesses to the processor core
  - Wake-up generator (WUGEN_IPU) module on external interrupts, coming from device peripherals

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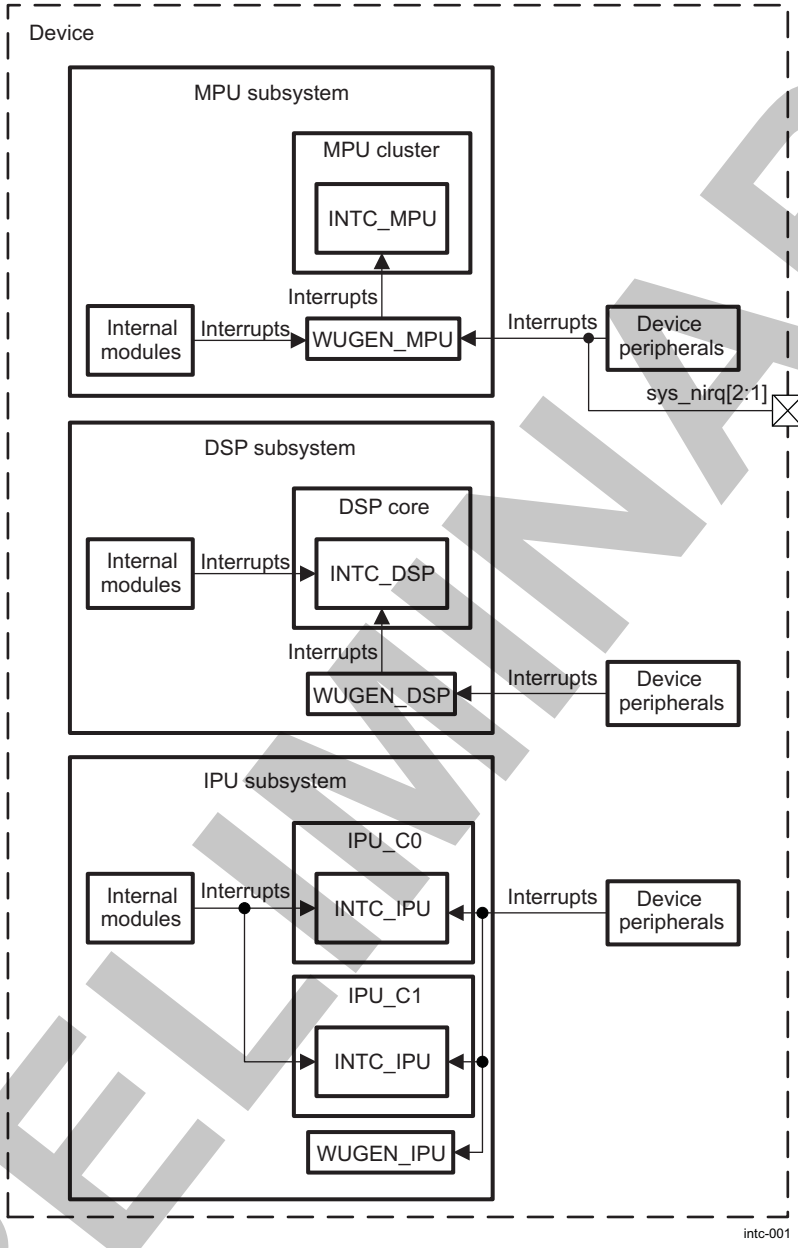
Figure 17-1 shows an overview of the device interrupt controllers.

Figure 17-1. Interrupt Controllers Overview



NOTE: For more information about the WUGEN_MPU module (including integration, functional and register description), see Dual Cortex-A15 MPU Subsystem.

For more information about the WUGEN_IPU module (including integration, functional and register description), see Dual Cortex-M4 IPU Subsystem.

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17.2 Interrupt Controllers Environment

This section describes the environment of the INTC application fields (in other words, external connections).

Figure 17-2 shows the relationship between the module and external interrupts.

Figure 17-2. Interrupts From External Devices

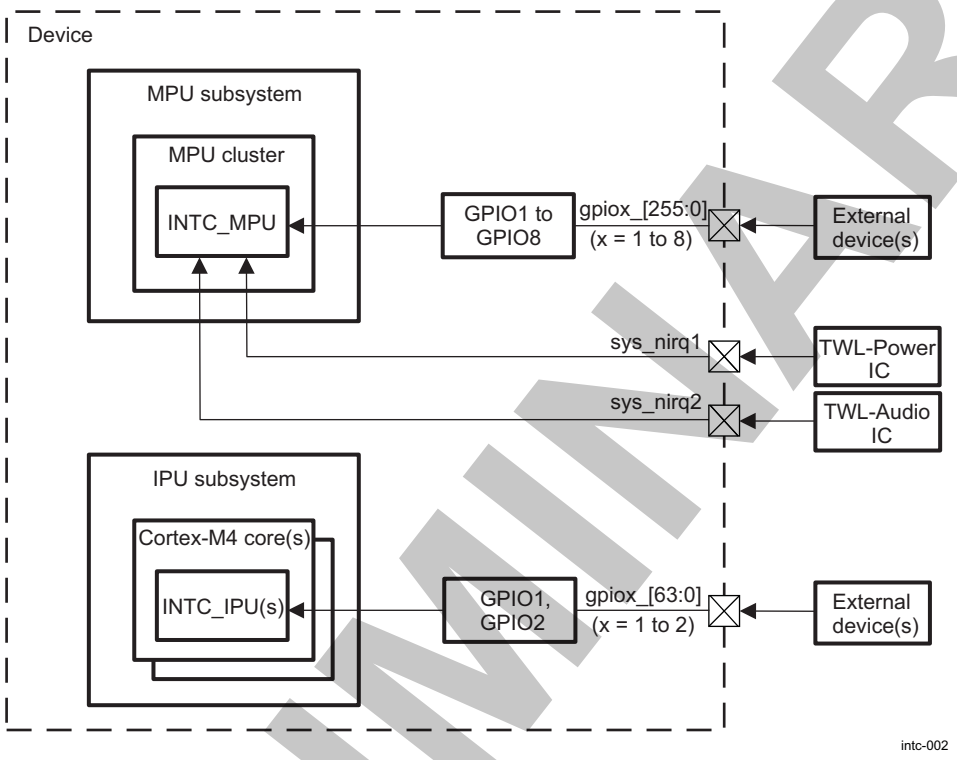

Table 17-1 describes the I/O signals that can be used by external devices to generate interrupts to the INTC_MPU or INTC_IPU.

Table 17-1. Interrupt Controllers I/O Signals

Signal Name	I/O[1]	Reset Value	Description	INTC_MPU	INTC_IPU
sys_nirq1	I	1	TWL-Power IC can use this pin to generate a system wake-up event to INTC_MPU.	✓	–
sys_nirq2	I	1	TWL-Audio IC can use this pin to generate a system wake-up event to INTC_MPU.	✓	–

(1) I = Input, O = Output

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Table 17-1. Interrupt Controllers I/O Signals (continued)

Signal Name	I/O[1]	Reset Value	Description	INTC_MPU	INTC_IPU
gpio1_[31:0]	I/O	–	External devices can use GPIO modules to generate interrupts to INTC_MPU or INTC_IPU. There are eight dedicated interrupt lines (for GPIO1 to GPIO8) to the INTC_MPU and two dedicated interrupt lines (for GPIO1 and GPIO2) to the INTC_IPU. Each GPIO module can generate a single interrupt whenever there is at least one event in any one of the configured 32 GPIO inputs. For more information about GPIO interrupt generation, see General-Purpose Interface.	✓	✓
gpio2_[63:32]	I/O	–		✓	✓
gpio3_[95:64]	I/O	–		✓	–
gpio4_[127:96]	I/O	–		✓	–
gpio5_[159:128]	I/O	–		✓	–
gpio6_[191:160]	I/O	–		✓	–
gpio7_[223:192]	I/O	–		✓	–
gpio8_[255:224]	I/O	–		✓	–

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17.3 Interrupt Controllers Integration

The INTC_MPU is integrated inside the Cortex-A15 MPCore (MPU cluster). For more information about INTC_MPU integration, see Section 4.2, *Dual Cortex-A15 MPU Subsystem Integration*, in Chapter 4, *Dual Cortex-A15 MPU Subsystem*.

The INTC_IPU is integrated inside each Cortex-M4 core. For more information about INTC_IPU integration, see Section 7.2, *Dual Cortex-M4 IPU Subsystem Integration*, in Chapter 7, *Dual Cortex-M4 IPU Subsystem*.

17.3.1 Interrupts Mapping

NOTE: All device peripherals interrupts (external to the MPU, DSP, and IPU subsystems) are active-high, level sensitive.

CAUTION

A single interrupt source can be physically mapped to multiple INTCs (MPU, DSP, and IPU subsystems). With multiple-mapped interrupts, TI strongly recommendeds unmasking each interrupt source in only one INTC at a time.

17.3.2 Interrupt Requests to INTC_MPU

Table 17-2 shows the INTC_MPU interrupt mapping.

Table 17-2. INTC_MPU Interrupt Mapping

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
MPU_IRQ_0	MPU_CLUSTER_IRQ_INTERR	MPU_CLUSTER	Illegal writes to interrupt controller memory map region[1]
MPU_IRQ_1	CS_CTI_MPU_C0_IRQ	CS_CTI_MPU_C0	TRIGOUT[6] of Cross Trigger Interface 0 (CTI0)[1]
MPU_IRQ_2	CS_CTI_MPU_C1_IRQ	CS_CTI_MPU_C1	TRIGOUT[6] of Cross Trigger Interface 1 (CTI1)[1]
MPU_IRQ_3	MPU_CLUSTER_IRQ_AXIERR	MPU_CLUSTER	Error indication for AXI write transactions with a BRESP error condition[1]
MPU_IRQ_4	ELM_IRQ	ELM	Error location process completion[2]
MPU_IRQ_5	WD_TIMER_MPU_C0_IRQ_WARN	WD_TIMER_MPU_C0	WD_TIMER_MPU_C0 warning interrupt
MPU_IRQ_6	WD_TIMER_MPU_C1_IRQ_WARN	WD_TIMER_MPU_C1	WD_TIMER_MPU_C1 warning interrupt
MPU_IRQ_7	EXT_SYS_IRQ_1	EXT_SYS	External interrupt (active low)
MPU_IRQ_8	Reserved	Reserved	Reserved
MPU_IRQ_9	L3_MAIN_IRQ_DBG_ERR	L3_MAIN	Reports debug errors on L3
MPU_IRQ_10	L3_MAIN_IRQ_APP_ERR	L3_MAIN	Reports application or nonattributable errors on L3
MPU_IRQ_11	PRM_IRQ_MPU	PRM	PRCM module
MPU_IRQ_12	DMA_SYSTEM_IRQ_0	DMA_SYSTEM	System DMA interrupt request 0[4]
MPU_IRQ_13	DMA_SYSTEM_IRQ_1	DMA_SYSTEM	System DMA interrupt request 1[4]
MPU_IRQ_14	DMA_SYSTEM_IRQ_2	DMA_SYSTEM	System DMA interrupt request 2[3]
MPU_IRQ_15	DMA_SYSTEM_IRQ_3	DMA_SYSTEM	System DMA interrupt request 3[3]
MPU_IRQ_16	L3_MAIN_IRQ_STAT_ALARM	L3_MAIN	L3 NoC statistic collector alarm
MPU_IRQ_17	MCBSP1_IRQ	MCBSP1	McBSP 1 / PORCOMMONIRQ: common synchronous interrupt Request line[2]
MPU_IRQ_18	SMARTREFLEX_MPU_IRQ	SMARTREFLEX_MPU	SmartReflex MCU interrupt request

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Table 17-2. INTC_MPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
MPU_IRQ_19	SMARTREFLEX_CORE_IRQ	SMARTREFLEX_CORE	SmartReflex Core interrupt request
MPU_IRQ_20	GPMC_IRQ	GPMC	General-purpose memory controller module(2)
MPU_IRQ_21	GPU_IRQ	GPU	3D graphics module interrupt
MPU_IRQ_22	MCBSP2_IRQ	MCBSP2	McBSP 2 / PORCOMMONIRQ: common synchronous interrupt Request line(2)
MPU_IRQ_23	MCBSP3_IRQ	MCBSP3	McBSP 3 / PORCOMMONIRQ: common synchronous interrupt Request line(2)
MPU_IRQ_24	ISS_IRQ_5	ISS	Imaging subsystem interrupt request(3)
MPU_IRQ_25	DISPC_IRQ	DISPC	Display controller interrupt request(4)
MPU_IRQ_26	MAILBOX_IRQ_USER0	MAILBOX	Mailbox user 0 interrupt request
MPU_IRQ_27	Reserved	Reserved	Reserved
MPU_IRQ_28	DSP_IRQ_MMU	DSP	DSP MMU interrupt
MPU_IRQ_29	GPIO1_IRQ_1	GPIO1	GPIO module 1– interrupt 1(3)
MPU_IRQ_30	GPIO2_IRQ_1	GPIO2	GPIO module 2 – interrupt 1(3)
MPU_IRQ_31	GPIO3_IRQ_1	GPIO3	GPIO module 3 – interrupt 1
MPU_IRQ_32	GPIO4_IRQ_1	GPIO4	GPIO module 4 – interrupt 1
MPU_IRQ_33	GPIO5_IRQ_1	GPIO5	GPIO module 5 – interrupt 1
MPU_IRQ_34	GPIO6_IRQ_1	GPIO6	GPIO module 6 – interrupt 1
MPU_IRQ_35	GPIO7_IRQ_1	GPIO7	GPIO module 7 – interrupt 1
MPU_IRQ_36	WD_TIMER3_IRQ	WD_TIMER3	Watchdog timer module 3 overflow (WDT controlled by Mini64)
MPU_IRQ_37	TIMER1_IRQ	TIMER1	General-purpose timer module 1 (Timer 1ms / Wakeup domain)
MPU_IRQ_38	TIMER2_IRQ	TIMER2	General-purpose timer module 2 (Timer 1ms / Core domain)
MPU_IRQ_39	TIMER3_IRQ	TIMER3	General-purpose timer module 3(3)
MPU_IRQ_40	TIMER4_IRQ	TIMER4	General-purpose timer module 4(3)
MPU_IRQ_41	TIMER5_IRQ	TIMER5	General-purpose timer module 5 (Audio BE)(2)
MPU_IRQ_42	TIMER6_IRQ	TIMER6	General-purpose timer module 6 (Audio BE)(2)
MPU_IRQ_43	TIMER7_IRQ	TIMER7	General-purpose timer module 7 (Audio BE)(2)
MPU_IRQ_44	TIMER8_IRQ	TIMER8	General-purpose timer module 8 (Audio BE)(2)
MPU_IRQ_45	TIMER9_IRQ	TIMER9	General-purpose timer module 9(3)
MPU_IRQ_46	TIMER10_IRQ	TIMER10	General-purpose timer module 10 (Timer 1ms / Core domain)
MPU_IRQ_47	TIMER11_IRQ	TIMER11	General-purpose timer module 11(3)
MPU_IRQ_48	MCSPI4_IRQ	MCSPI4	McSPI module 4
MPU_IRQ_49	Reserved	Reserved	Reserved
MPU_IRQ_50	Reserved	Reserved	Reserved
MPU_IRQ_51	Reserved	Reserved	Reserved
MPU_IRQ_52	Reserved	Reserved	Reserved
MPU_IRQ_53	DSI1_A_IRQ	DSI1_A	Display DSI1_A interrupt request(4)
MPU_IRQ_54	SATA_IRQ	SATA	SATA interrupt request
MPU_IRQ_55	DSI1_C_IRQ	DSI1_C	Display DSI1_C interrupt request(4)
MPU_IRQ_56	I2C1_IRQ	I2C1	I2C module 1(3)
MPU_IRQ_57	I2C2_IRQ	I2C2	I2C module 2(3)
MPU_IRQ_58	HDQ1W_IRQ	HDQ1W	HDQ1W module interrupt
MPU_IRQ_59	MMC5_IRQ	MMC5	MMC5 interrupt request(3)
MPU_IRQ_60	I2C5_IRQ	I2C5	I2C module 5
MPU_IRQ_61	I2C3_IRQ	I2C3	I2C module 3(3)
MPU_IRQ_62	I2C4_IRQ	I2C4	I2C module 4(3)
MPU_IRQ_63	Reserved	Reserved	Reserved

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Table 17-2. INTC_MPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
MPU_IRQ_64	Reserved	Reserved	Reserved
MPU_IRQ_65	MCSPI1_IRQ	MCSPI1	McSPI module 1[4]
MPU_IRQ_66	MCSPI2_IRQ	MCSPI2	McSPI module 2[3]
MPU_IRQ_67	HSI_IRQ_MPU_P1	HSI	HSI interrupt request– Port 1 combined interrupt[3]
MPU_IRQ_68	HSI_IRQ_MPU_P2	HSI	HSI interrupt request– Port 2 combined interrupt[3]
MPU_IRQ_69	FDIF_IRQ_3	FDIF	Face detect Interrupt 3
MPU_IRQ_70	UART4_IRQ	UART4	UART module 4
MPU_IRQ_71	HSI_IRQ_MPU_DMA	HSI	HSI DMA engine[3]
MPU_IRQ_72	UART1_IRQ	UART1	UART module 1
MPU_IRQ_73	UART2_IRQ	UART2	UART module 2
MPU_IRQ_74	UART3_IRQ	UART3	UART module 3 (also infrared– IRDA)[4]
MPU_IRQ_75	PBIAS_IRQ	PBIAS	SDCARD_PBIAS interrupt
MPU_IRQ_76	USB_HOST_HS_IRQ_OHCI	USB_HOST_HS	USB_HOST_HS– OHCI controller interrupt
MPU_IRQ_77	USB_HOST_HS_IRQ_EHCI	USB_HOST_HS	USB_HOST_HS– EHCI controller interrupt[3]
MPU_IRQ_78	USB_TLL_HS_IRQ	USB_TLL_HS	USB_TLL_HS Interrupt[3]
MPU_IRQ_79	Reserved	Reserved	Reserved
MPU_IRQ_80	WD_TIMER2_IRQ	WD_TIMER2	WDT2 interrupt
MPU_IRQ_81	Reserved	Reserved	Reserved
MPU_IRQ_82	Reserved	Reserved	Reserved
MPU_IRQ_83	MMC1_IRQ	MMC1	MMC1_IRQ[4]
MPU_IRQ_84	Reserved	Reserved	Reserved
MPU_IRQ_85	Reserved	Reserved	Reserved
MPU_IRQ_86	MMC2_IRQ	MMC2	MMC/SDIO module 2[4]
MPU_IRQ_87	Reserved	Reserved	Reserved
MPU_IRQ_88	Reserved	Reserved	Reserved
MPU_IRQ_89	Reserved	Reserved	Reserved
MPU_IRQ_90	DEBUGSS_IRQ_CT_UART	DEBUGSS	CT_UART interrupt generated when data ready on RX or when TX empty
MPU_IRQ_91	MCSPI3_IRQ	MCSPI3	McSPI module 3
MPU_IRQ_92	USB_OTG_SS_IRQ_CORE	USB_OTG_SS	USB_OTG_SS– interrupt CORE (main source of interrupts)[3]
MPU_IRQ_93	USB_OTG_SS_IRQ_WRP	USB_OTG_SS	USB_OTG_SS - Interrupt Wrapper[3]
MPU_IRQ_94	MMC3_IRQ	MMC3	MMC/SDIO module 3[3]
MPU_IRQ_95	Reserved	Reserved	Reserved
MPU_IRQ_96	MMC4_IRQ	MMC4	MMC/SDIO module 4[3]
MPU_IRQ_97	Reserved	Reserved	Reserved
MPU_IRQ_98	Reserved	Reserved	Reserved
MPU_IRQ_99	AESS_IRQ_MPU	AESS	Audo engine subsystem interrupt (in ABE)
MPU_IRQ_100	IPU_IRQ_MPU	IPU	IPU MMU interrupt
MPU_IRQ_101	HDMI_IRQ	HDMI	Display HDMI interrupt request[4]
MPU_IRQ_102	SMARTREFLEX_MM_IRQ	SMARTREFLEX_MM	SmartReflex IVA interrupt request
MPU_IRQ_103	IVA_IRQ_SYNC_1	IVA	Sync interrupt from ICONT2 (vDMA)[4]
MPU_IRQ_104	IVA_IRQ_SYNC_0	IVA	Sync interrupt from ICONT1[4]
MPU_IRQ_105	UART5_IRQ	UART5	UART module 5

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Table 17-2. INTC_MPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
MPU_IRQ_106	UART6_IRQ	UART6	UART module 6
MPU_IRQ_107	IVA_IRQ_MAILBOX_0	IVA	IVA-HD subsystem interrupt request (Mailbox interrupt 0)
MPU_IRQ_108	Reserved	Reserved	Reserved
MPU_IRQ_109	MCASP_IRQ_AXEVT	MCASP	McASP Transmit interrupt (Audio BE)(2)
MPU_IRQ_110	EMIF1_IRQ	EMIF1	EMIF1 interrupt request
MPU_IRQ_111	EMIF2_IRQ	EMIF2	EMIF2 interrupt request
MPU_IRQ_112	MCPDM_IRQ	MCPDM	McPDM interrupt (Audio BE)(2)
MPU_IRQ_113	DMM_IRQ	DMM	DMM interrupt(3)
MPU_IRQ_114	DMIC_IRQ	DMIC	DMIC interrupt (Audio BE)(2)
MPU_IRQ_115	Reserved	Reserved	Reserved
MPU_IRQ_116	Reserved	Reserved	Reserved
MPU_IRQ_117	Reserved	Reserved	Reserved
MPU_IRQ_118	Reserved	Reserved	Reserved
MPU_IRQ_119	EXT_SYS_IRQ_2	EXT_SYS	External interrupt 2 (active low)
MPU_IRQ_120	KBD_IRQ	KBD	Keyboard controller interrupt
MPU_IRQ_121	GPIO8_IRQ_1	GPIO8	GPIO module 8 - interrupt 1
MPU_IRQ_122	Reserved	Reserved	Reserved
MPU_IRQ_123	Reserved	Reserved	Reserved
MPU_IRQ_124	Reserved	Reserved	Reserved
MPU_IRQ_125	BB2D_IRQ	BB2D	BB2D interrupt request(3)
MPU_IRQ_126	CTRL_MODULE_CORE_IRQ_THERMAL_ALERT	CTRL_MODULE_CORE	Thermal alert is generated by the CTRL_MODULE when one of the three thermal sensors go over a defined threshold value
MPU_IRQ_127	Reserved	Reserved	Reserved
MPU_IRQ_128	Reserved	Reserved	Reserved
MPU_IRQ_129	Reserved	Reserved	Reserved
MPU_IRQ_130	Reserved	Reserved	Reserved
MPU_IRQ_131	MPU_CLUSTER_IRQ_PMU_C0	MPU_CLUSTER	PMU Interrupt signal from MPU core 0
MPU_IRQ_132	MPU_CLUSTER_IRQ_PMU_C1	MPU_CLUSTER	PMU Interrupt signal from MPU core 1
MPU_IRQ_133	Reserved	Reserved	Reserved
MPU_IRQ_134	Reserved	Reserved	Reserved
MPU_IRQ_135	Reserved	Reserved	Reserved
MPU_IRQ_136	Reserved	Reserved	Reserved
MPU_IRQ_137	Reserved	Reserved	Reserved
MPU_IRQ_138	Reserved	Reserved	Reserved
MPU_IRQ_139	WD_TIMER_MPU_C0_IRQ	WD_TIMER_MPU_C0	WD_TIMER_MPU_C0 time-out interrupt
MPU_IRQ_140	WD_TIMER_MPU_C1_IRQ	WD_TIMER_MPU_C1	WD_TIMER_MPU_C1 time-out interrupt
MPU_IRQ_141	Reserved	Reserved	Reserved
MPU_IRQ_142	Reserved	Reserved	Reserved
MPU_IRQ_143	Reserved	Reserved	Reserved
MPU_IRQ_144	Reserved	Reserved	Reserved
MPU_IRQ_145	Reserved	Reserved	Reserved
MPU_IRQ_146	Reserved	Reserved	Reserved
MPU_IRQ_147	Reserved	Reserved	Reserved
MPU_IRQ_148	Reserved	Reserved	Reserved

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Table 17-2. INTC_MPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
MPU_IRQ_149	Reserved	Reserved	Reserved
MPU_IRQ_150	Reserved	Reserved	Reserved
MPU_IRQ_151	Reserved	Reserved	Reserved
MPU_IRQ_152	Reserved	Reserved	Reserved
MPU_IRQ_153	Reserved	Reserved	Reserved
MPU_IRQ_154	Reserved	Reserved	Reserved
MPU_IRQ_155	Reserved	Reserved	Reserved
MPU_IRQ_156	Reserved	Reserved	Reserved
MPU_IRQ_157	Reserved	Reserved	Reserved
MPU_IRQ_158	Reserved	Reserved	Reserved
MPU_IRQ_159	Reserved	Reserved	Reserved

(1) Internally generated within the MPU subsystem
(2) Shared with INTC_DSP
(3) Shared with INTC_IPU
(4) Shared with INTC_DSP and INTC_IPU

NOTE: All MPU subsystem internal interrupts are active-high, level-sensitive.

17.3.3 Interrupt Requests to INTC_IPU

Table 17-3 shows the INTC_IPU interrupt mapping.

Table 17-3. INTC_IPU Interrupt Mapping

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
IPU_IRQ_0	–	–	MSP initial value in exception vector table
IPU_IRQ_1	RESET_IRQ	RESET	Reset
IPU_IRQ_2	NMI_IRQ	NMI	External NMI inputs(1)
IPU_IRQ_3	HARD_FAULT_IRQ	HARD_FAULT	All fault conditions, if the fault handle is not enabled(1)
IPU_IRQ_4	MEM_MANAGE_FAULT_IRQ	MEM_MANAGE_FAULT	Memory management fault; access to illegal locations(1)
IPU_IRQ_5	BUS_FAULT_IRQ	BUS_FAULT	Bus error (on AHB interface)(1)
IPU_IRQ_6	USAGE_FAULT_IRQ	USAGE_FAULT	Program error(1)
IPU_IRQ_7	Reserved	Reserved	Reserved
IPU_IRQ_8	Reserved	Reserved	Reserved
IPU_IRQ_9	Reserved	Reserved	Reserved
IPU_IRQ_10	Reserved	Reserved	Reserved
IPU_IRQ_11	SV_CALL_IRQ	SV_CALL	Service system call(1)
IPU_IRQ_12	DEBUG_MON_IRQ	DEBUG_MON	BP, WP, or external debug request(1)
IPU_IRQ_13	Reserved	Reserved	Reserved
IPU_IRQ_14	PEND_SV_IRQ	PEND_SV	Pendable request for system device(1)
IPU_IRQ_15	SYS_TICK_TIMER_IRQ	SYS_TICK_TIMER	System tick timer has fired(1)
IPU_IRQ_16	XLATE_MMU_FAULT_IRQ	XLATE_MMU_FAULT	xlate_mmu_fault (from L2_MMU)(2)
IPU_IRQ_17	SCACHE_MMU_IRQ	SCACHE_MMU	Shared cache or MMU maintenance complete(2)
IPU_IRQ_18	CTM_TIM_EVENT1_IRQ	CTM_TIM_EVENT1	CTM timer event (timer 1)(2)

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Table 17-3. INTC_IPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
IPU_IRQ_19	SPINLOCK_IRQ	SPINLOCK	Semaphore interrupt (1 to each core)(2)
IPU_IRQ_20	ICE_NEMU_IRQ	ICE_NEMU	ICECrusher (1 to each core)(2)
IPU_IRQ_21	IPU_IMP_FAULT_IRQ	IPU_IMP_FAULT	Ducati imprecise fault (from interconnect)(2)
IPU_IRQ_22	CTM_TIM_EVENT2_IRQ	CTM_TIM_EVENT2	CTM timer event (timer 2)(2)
IPU_IRQ_23	DISPC_IRQ	DISPC	Display Controller interrupt request(5)
IPU_IRQ_24	DSI1_A_IRQ	DSI1_A	Display DSI1_A interrupt request(5)
IPU_IRQ_25	Reserved	Reserved	Reserved
IPU_IRQ_26	HDMI_IRQ	HDMI	Display HDMI interrupt request(5)
IPU_IRQ_27	ISS_IRQ_0	ISS	Interrupt from ISS
IPU_IRQ_28	ISS_IRQ_1	ISS	Interrupt from ISS
IPU_IRQ_29	ISS_IRQ_2	ISS	Interrupt from ISS
IPU_IRQ_30	ISS_IRQ_3	ISS	Interrupt from ISS
IPU_IRQ_31	ISS_IRQ_4	ISS	Interrupt from ISS(3)
IPU_IRQ_32	ISS_IRQ_5	ISS	Interrupt from ISS(4)
IPU_IRQ_33	FDIF_IRQ_1	FDIF	Face detect Interrupt 1
IPU_IRQ_34	DMA_SYSTEM_IRQ_0	DMA_SYSTEM	System DMA interrupt request 0(5)
IPU_IRQ_35	DMA_SYSTEM_IRQ_1	DMA_SYSTEM	System DMA interrupt request 1(5)
IPU_IRQ_36	DMA_SYSTEM_IRQ_2	DMA_SYSTEM	System DMA interrupt request 2(4)
IPU_IRQ_37	DMA_SYSTEM_IRQ_3	DMA_SYSTEM	System DMA interrupt request 3(4)
IPU_IRQ_38	IVA_IRQ_MAILBOX_2	IVA	IVA-HD subsystem interrupt request (Mailbox interrupt 2)
IPU_IRQ_39	IVA_IRQ_SYNC_1	IVA	Sync interrupt from ICONT2 (vDMA)(5)
IPU_IRQ_40	IVA_IRQ_SYNC_0	IVA	Sync interrupt from ICONT1(5)
IPU_IRQ_41	I2C1_IRQ	I2C1	I2C module 1(4)
IPU_IRQ_42	I2C2_IRQ	I2C2	I2C module 2(4)
IPU_IRQ_43	I2C3_IRQ	I2C3	I2C module 3(4)
IPU_IRQ_44	I2C4_IRQ	I2C4	I2C module 4(4)
IPU_IRQ_45	UART3_IRQ	UART3	UART module 3 (also infrared - IRDA)(5)
IPU_IRQ_46	L3_MAIN_IRQ_APP_ERR	L3_MAIN	Reports application or non-attributable errors on L3
IPU_IRQ_47	PRM_IRQ_IPU	PRM	PRCM module
IPU_IRQ_48	SMARTREFLEX_CORE_IRQ	SMARTREFLEX_CORE	SmartReflex Core OR SmartReflex MM
IPU_IRQ_49	HSI_IRQ_MPU_DMA	HSI	HSI - MPU DMA interrupt request(4)
IPU_IRQ_50	MAILBOX_IRQ_USER2	MAILBOX	Mailbox user 2 interrupt request
IPU_IRQ_51	GPIO1_IRQ_1	GPIO1	GPIO module 1 - interrupt 1(4)
IPU_IRQ_52	GPIO2_IRQ_1	GPIO2	GPIO module 2 - interrupt 1(4)
IPU_IRQ_53	TIMER3_IRQ	TIMER3	General-purpose timer module 3(4)
IPU_IRQ_54	TIMER4_IRQ	TIMER4	General-purpose timer module 4(4)
IPU_IRQ_55	TIMER9_IRQ	TIMER9	General-purpose timer module 9(4)
IPU_IRQ_56	TIMER11_IRQ	TIMER11	General-purpose timer module 11(4)
IPU_IRQ_57	MCSPI1_IRQ	MCSPI1	McSPI module 1(5)
IPU_IRQ_58	MCSPI2_IRQ	MCSPI2	McSPI module 2(4)
IPU_IRQ_59	DSI1_C_IRQ	DSI1_C	Display DSI1_C interrupt request(5)
IPU_IRQ_60	Reserved	Reserved	Reserved
IPU_IRQ_61	Reserved	Reserved	Reserved
IPU_IRQ_62	Reserved	Reserved	Reserved
IPU_IRQ_63	Reserved	Reserved	Reserved

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Table 17-3. INTC_IPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
IPU_IRQ_64	DMM_IRQ	DMM	DMM interrupt(4)
IPU_IRQ_65	BB2D_IRQ	BB2D	BB2D interrupt request(4)
IPU_IRQ_66	MMC1_IRQ	MMC1	MMC/SDIO module 1(5)
IPU_IRQ_67	MMC2_IRQ	MMC2	MMC/SDIO module 2(5)
IPU_IRQ_68	MMC3_IRQ	MMC3	MMC/SDIO module 3(4)
IPU_IRQ_69	Reserved	Reserved	Reserved
IPU_IRQ_70	Reserved	Reserved	Reserved
IPU_IRQ_71	Reserved	Reserved	Reserved
IPU_IRQ_72	Reserved	Reserved	Reserved
IPU_IRQ_73	USB_HOST_HS_IRQ_EHCI	USB_HOST_HS	USB_HOST_HS - Interrupt EHCI controller(4)
IPU_IRQ_74	USB_TLL_HS_IRQ	USB_TLL_HS	USB_TLL_HS Interrupt(4)
IPU_IRQ_75	Reserved	Reserved	Reserved
IPU_IRQ_76	USB_OTG_SS_IRQ_CORE	USB_OTG_SS	USB_OTG_SS controller - interrupt CORE (main interrupt source)(4)
IPU_IRQ_77	USB_OTG_SS_IRQ_WRP	USB_OTG_SS	USB_OTG_SS - Interrupt Wrapper(4)
IPU_IRQ_78	HSI_IRQ_MPU_P1	HSI	HSI interrupt request - Port 1 combined interrupt(4)
IPU_IRQ_79	HSI_IRQ_MPU_P2	HSI	HSI interrupt request - Port 2 combined interrupt(4)

(1) Internally generated within IPU_Cx (where x = 0 or 1)
(2) Internally generated within IPU subsystem
(3) Shared with INTC_DSP
(4) Shared with INTC_MPU
(5) Shared with INTC_DSP and INTC_MPU

NOTE: All IPU subsystem internal interrupts are edge interrupts, except the one generated from the MMU (XLATE_MMU_FAULT_IRQ), which is level interrupt.

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17.4 Interrupt Controllers Functional Description

17.4.1 INTC_MPU Functional Description

INTC_MPU is configured to have the following interrupt sources:

- 16 software-generated interrupts (SGIs): ID[15:0]
- 7 private peripheral interrupts (PPIs): ID[31:25]
- 160 shared peripheral interrupts (SPIs): ID[191:32] (rising-edge or high-level sensitive). The interrupt mapping of these interrupts is presented in Table 17-2.

CAUTION

Although the hardware interrupts can be configured to be rising-edge or high-level sensitive in the INTC, the device supports only active-high, level-sensitive configuration.

For more information about the functionality of the INTC_MPU, see ARM *Cortex-A15 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

17.4.2 INTC_IPU Functional Description

The INTC_IPU has the following configuration in the device:

- 64 hardware interrupts/16 levels of priority for each Cortex-M4 core. The interrupt mapping of these interrupts (IPU_IRQ_[79:16]) is presented in Table 17-3.
- The calibration register, which is used to reload the SYSTICK timer to generate a fixed interval, is not supported in the Cortex-M4 core within the IPU subsystem. The TENMS field is not available due to the different frequencies during voltage scaling.
- The SYSRESETREQ reset feature is not supported at the Cortex-M4 processor level. Writing to this bit has no effect.

For more information about the functionality of the INTC_IPU, see *ARM Cortex-M4 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

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17.5 Interrupt Controllers Register Manual

17.5.1 Interrupt Controllers Instance Summary

For information about the INTC_MPU and INTC_IPU instances, see Dual Cortex-A15 MPU Subsystem and Dual Cortex-M4 IPU Subsystem, respectively.

17.5.2 INTC_MPU Registers

For information about the INTC_MPU registers and their description, see *ARM Cortex-A15 MP Core Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

17.5.3 INTC_IPU Registers

For information about the INTC_IPU (NVIC) registers and their description, see *ARM Cortex-M4 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

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Control Module

This chapter describes the system control module for the device.

NOTE: Some of the control module features, primarily those concerning the device I/O pads, are not available in all OMAP54xx devices.

For details, see Section 1.5, *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

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18.1 Control Module Overview

The control module allows software control of the various static modes supported by the device. It is composed of two control submodules: general control module and device (pad configuration) control module.

The general control module has the following features:

- General status and control
- Hardware observability input/output (I/O) multiplexing
- Standard eFuse logic

The device control module provides the following features:

- Pad functional I/O multiplexing
- Pad pullup and pulldown configuration
- Pad groups associated signal integrity controls
- Complex I/O configuration
- Analog function control
- Device-specific eFuse registers

Both control submodules are split into two instances: the control core instance within the CORE power domain, and the control wake-up instance within the WKUP power domain. For more information about the four control module instances, see Section 18.3, *Control Module Integration*.

Figure 18-1 is an overview of the control module.

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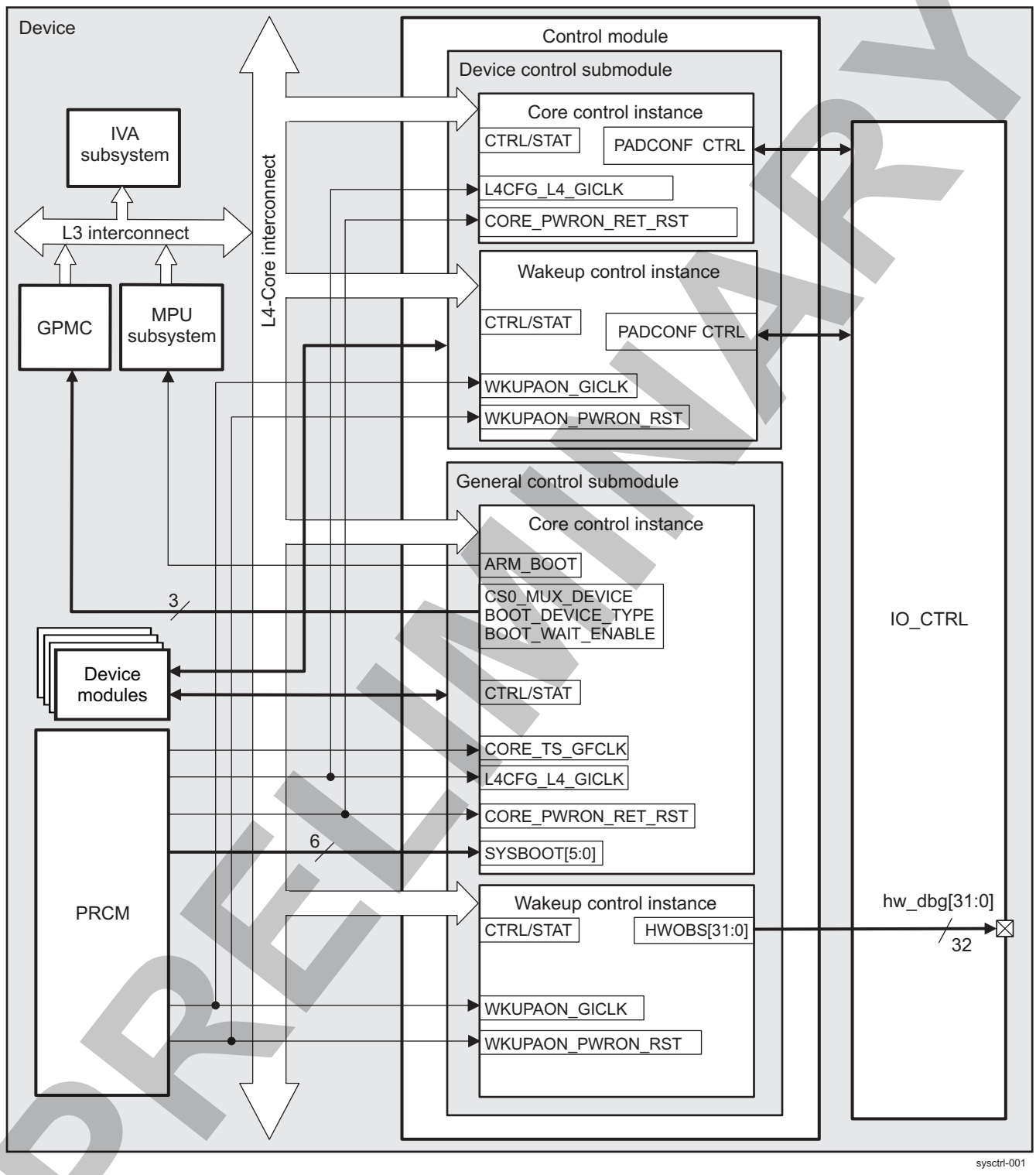
Figure 18-1. Control Module Overview



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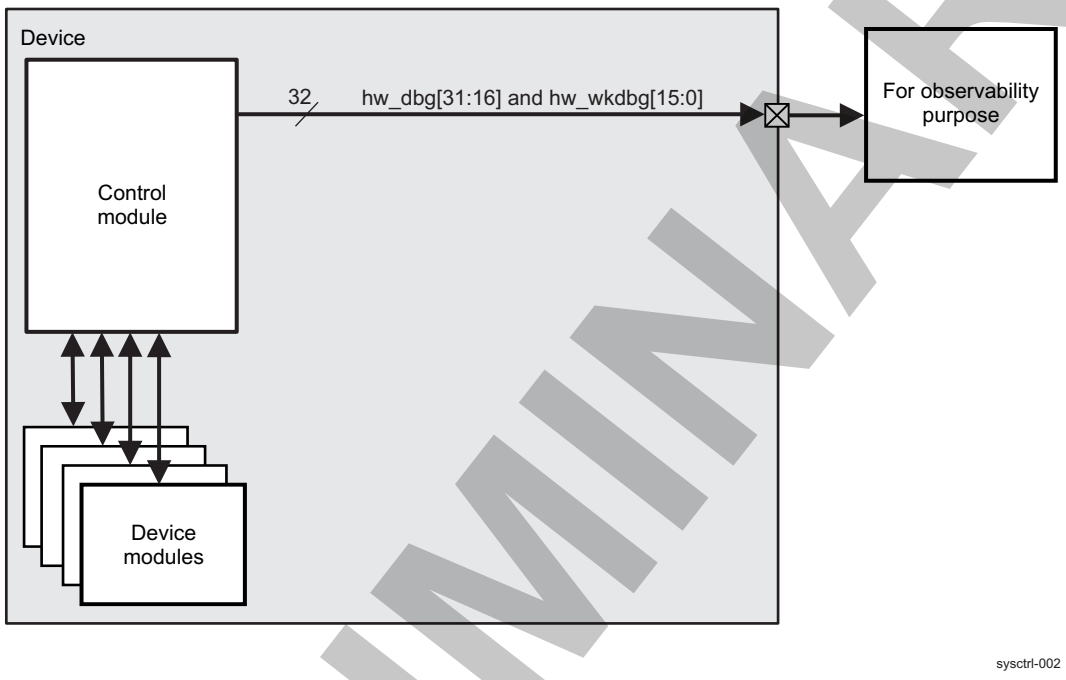
18.2 Control Module Environment

The control module controls the multiplexing of device internal module signals routed to the external pins (hw_dbg[31:0]) for hardware debug purposes. For more information, see Section 18.4.11, *Hardware Observability*, and Section 18.4.8, *PAD Functional Multiplexing and Configuration*. Using the correct pad configuration, the control module maps these pins at the device boundary to observe the internal signals from the power, reset, and clock management (PRCM) module, direct memory access (DMA) requests, and interrupts. Figure 18-2 is an overview of the control module environment.

Figure 18-2. Control Module Environment



18.2.1 Control Module Signals

Table 18-1 lists the control module hardware observability outputs configured to observe the debug signals of the device module. It describes the module signals and specifies their links to functions.

Table 18-1. Control Module I/O Description

Signal	I/O[1]	Description	Reset Value[2]
hw_dbg[31:16] and hw_wkdbg[15:0]	O	32 internal hardware observability signals. hw_dbg[31:16] are mapped to pads in the CORE power domain and hw_wkdbg[15:0] are mapped to pads in the WKUP power domain.	Hi-Z

(1) I = Input; O = Output; I/O = Bidirectional
(2) Hi-Z = High impedance

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18.3 Control Module Integration

The control module of the device is on the L4_CORE interconnect. It consists of four module instances:

- General core control module (CTRL_MODULE_CORE)
- General wakeup control module (CTRL_MODULE_WKUP)
- Device core control module (CTRL_MODULE_CORE_PAD)
- Device wakeup control module (CTRL_MODULE_WKUP_PAD)

For more information about the different control module instances, see Table 18-4.

Each of these four module instances has an associated register set and shares one functional clock and one reset signal with the PRCM module. The exception is the general core control module (CTRL_MODULE_CORE), which also receives a secondary functional clock, L3INSTR_TS_GCLK. Table 18-2 describes the signals.

Table 18-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
CTRL_MODULE_WKUP	WKUPAON_GICLK	WKUPAON_GICLK	PRCM	L4_WKUP interface/functional clock propagated to the general wkup control module
CTRL_MODULE_WKUP_PAD	WKUPAON_GICLK	WKUPAON_GICLK	PRCM	L4_WKUP interface/functional clock propagated to the device wkup control module
CTRL_MODULE_CORE	L4CFG_L4_GICLK	L4CFG_L4_GICLK	PRCM	L4_CFG interface/functional clock propagated to the general core control module
	L3INSTR_TS_GCLK	L3INSTR_TS_GCLK	PRCM	Functional clock for the three bandgap state-machines instantiated in the general core control module
CTRL_MODULE_CORE_PAD	L4CFG_L4_GICLK	L4CFG_L4_GICLK	PRCM	L4_CFG interface/functional clock propagated to the device core control module
Resets				
CTRL_MODULE_WKUP	WKUPAON_PWRON_RST	WKUPAON_PWRON_RST	PRCM	Internal power-on reset (POR) affecting the general wakeup control module
CTRL_MODULE_CORE	CORE_PWRON_RET_RST	CORE_PWRON_RET_RST	PRCM	Internal POR affecting the general core control module
CTRL_MODULE_WKUP_PAD	WKUPAON_PWRON_RST	WKUPAON_PWRON_RST	PRCM	Internal POR affecting the device wakeup control module
CTRL_MODULE_CORE_PAD	CORE_PWRON_RET_RST	CORE_PWRON_RET_RST	PRCM	Internal POR affecting the device core control module

Table 18-3. Hardware Requests

Interrupt Requests				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Destination**	**Description**
CTRL_MODULE_CORE	MPU_IRQ_126	THERMAL_ALERT	MPU	Interrupt generated by general core control module to the MPU
CTRL_MODULE_CORE	MPU_IRQ_75	PBIAS_IRQ	MPU	Interrupt generated by the PBIAS cell to the MPU

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NOTE: For a description of the interrupt sources, see Section 17.3.2, *Interrupt Requests to INTC_MPU*, in Chapter 17, *Interrupt Controllers*.

The control module is reset by the internal POR, which is active low. The PRCM module provides a retention POR signal (CORE_PWRON_RET_RST) duplicated to both of the core control module instances, and a nonretention POR signal (WKUPAON_PWRON_RST) duplicated to each of the two wake-up control module instances in the control module. For more information, see Section 3.5.4, *Reset Domains*, in Chapter 3, *Power, Reset, and Clock Management*. The control module does not respond to a warm reset or to an L4_CORE reset.

The main sequential logic within the system control module is accessible in a register file through the L4_CORE interconnect. The PRCM module provides the L4CFG_L4_GICLK functional clock signal (CD_L4_CFG clock domain) separately to each of the two core control submodules. In addition, the bandgap state-machine, instantiated inside the CTRL_MODULE_CORE receives its functional clock (L3INSTR_TS_GCLK) from the PRCM module. For more information about this signal, see Section 3.6.3.1 , *PRM Clock Source*, in Chapter 3, *Power, Reset, and Clock Management*.

The PRCM module also supplies the WKUPAON_GICLK functional clock signal (CD_WKUPAON clock domain) to each of the two wake-up control module instances. For more information about this signal, see Section 3.6.3.1 , *PRM Clock Source*, in Chapter 3, *Power, Reset, and Clock Management*.

The PRCM module latches the sys_boot[5:0] pad signals at POR and exports them as vector to the SYS_BOOT[5:0] input of the CTRL_MODULE_CORE. It is scanned in the CONTROL_STATUS[5:0] SYS_BOOT bit field.

The thermal management subsystem inside the general core control module delivers one interrupt request (THERMAL_ALERT) to line MPU_IRQ_126 of the MPU subsystem interrupt controller (INTC), and delivers three thermal protection output signals (TSHUT) to the PRCM module, used as warm resets. For more information about the functional outputs of the thermal management control module, see Section 18.4.10.

The PBIAS cell delivers an interrupt request (PBIAS_IRQ) to the MPU_IRQ_75 line of the MPU subsystem INTC. This line is activated when a PBIAS error occurs.

The signal integration of the control module features:

- No IDLE hardware handshake
- No STANDBY hardware handshake
- No wake-up request generation
- No DMA request generation
- Two interrupt requests to the MPU subsystem - THERMAL_ALERT and PBIAS_IRQ
- Three TSHUT used as PRCM warm-reset sources
- Three functional clocks: two clocks in the CFG and one in the WKUP clock domains
- One retention and one nonretention internal power-on-based resets

Figure 18-3 shows the integration of the module in the device.

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Figure 18-3. Control Module Integration

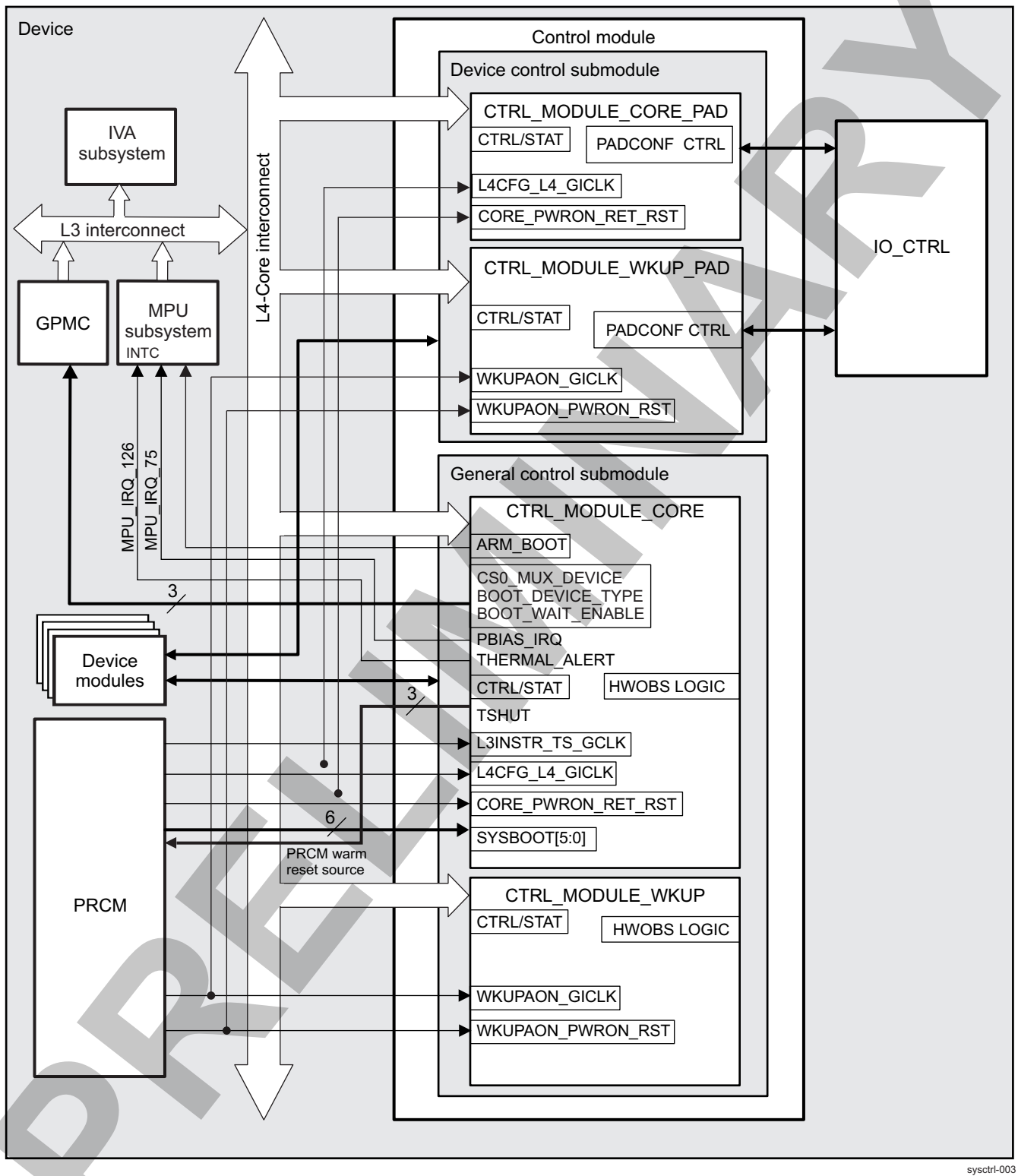

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Table 18-4 lists the integration attributes.

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Table 18-4. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
CTRL_MODULE_WKUP	PD_WKUPAON	L4_WKUP
CTRL_MODULE_CORE	PD_CORE	L4_CFG
CTRL_MODULE_WKUP_PAD	PD_WKUPAON	L4_WKUP
CTRL_MODULE_CORE_PAD	PD_CORE	L4_CFG

Software sets the configuration registers to the desired values depending on the configuration of the requested device. Software can set static device configuration registers any time, and the settings are effective immediately.

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18.4 Control Module Functional Description

18.4.1 Control Module Block Diagram

The control module controls the settings of various device modules through the register configuration and internal signals. It also controls the pad configuration, pin functional multiplexing, and the routing of internal signals (such as PRCM signals or DMA requests) to output pads configured for hardware observability.

Figure 18-4 is the control module block diagram.

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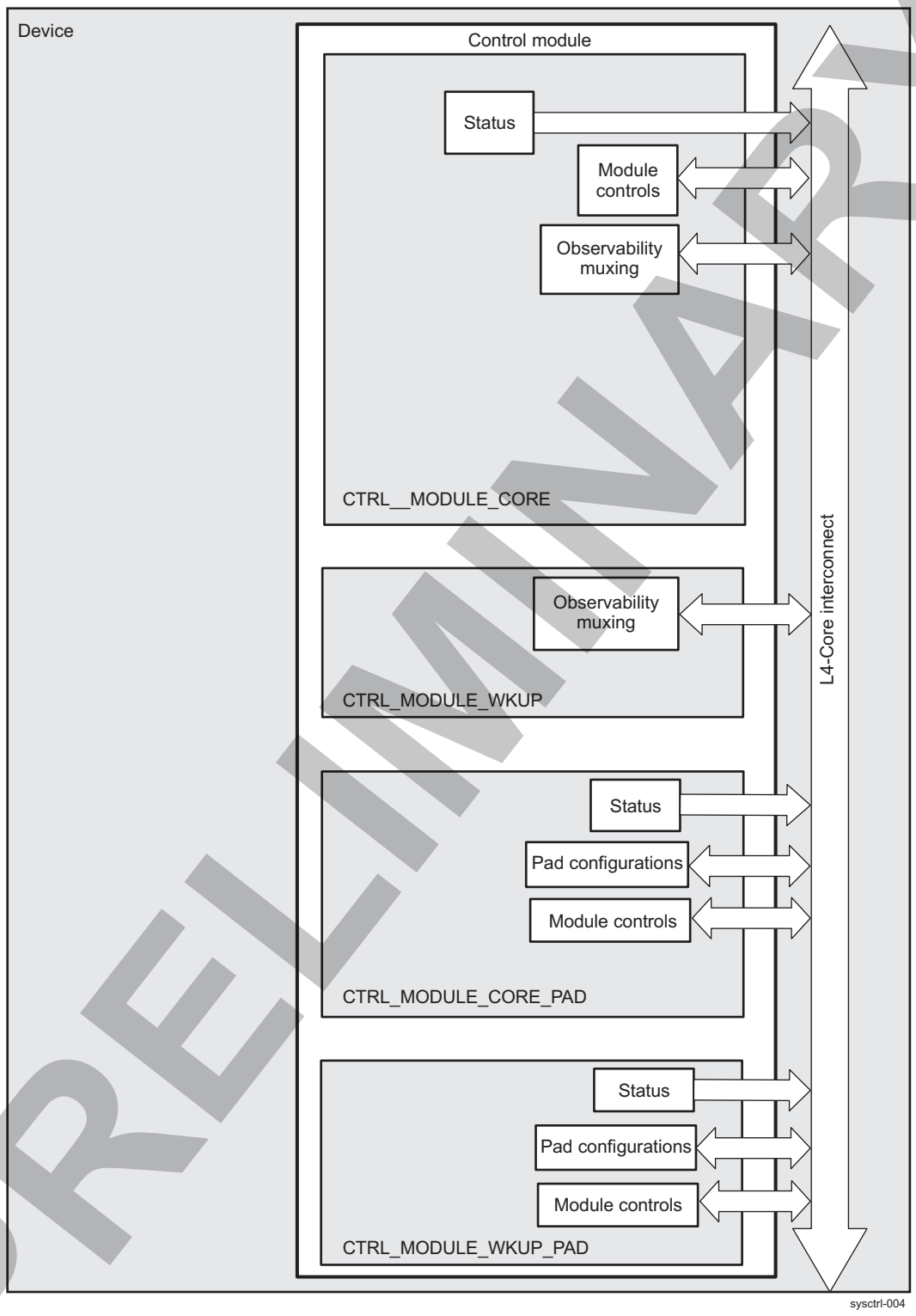
Figure 18-4. Control Module Block Diagram



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The control submodules primarily implement a bank of registers accessible (read and write) by software and some read-only registers that provide status information.

The 32-bit read and write registers in the general control module (CTRL_MODULE_CORE and CTRL_MODULE_WKUP) can be divided into the following classes:

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- Hardware observability registers
- Status and configuration registers
- Boot registers
- eFuse ROM registers
- Miscellaneous functional registers

The 32-bit read/write registers in the device control module (CTRL_MODULE_CORE_PAD and CTRL_MODULE_WKUP_PAD) can be divided into the following classes:

- Pad configuration registers
- Pad groups (not individual per pad) associated registers for signal integrity parameters control (32-bit read/write registers)
- I/O cells associated specific control registers
- Device-specific status and configuration registers
- Miscellaneous functional registers

18.4.2 Control Module Clock Configuration

The L4CFG_L4_GICLK and WKUPAON_GICLK source clocks are internally distributed into two clock paths: the first path directly mirrors the source clock and is an always-running clock. It is used to synchronize and resample some of the module inputs. The other clock path is automatically gated when there is no access to the control module through the L4 interconnect.

There are no PRCM software controls for the L4CFG_L4_GICLK and WKUPAON_GICLK clocks in the control module. There are, however, clock activity status bits in the PRCM module.

The L3INSTR_TS_GCLK has the following software controls located in the PRCM module:

- Status: see in Chapter 3, *Power, Reset, and Clock Management*
- Divider ratio: see in Chapter 3, *Power, Reset, and Clock Management*

18.4.3 Control Module Software Reset

The control module is not sensitive to software reset.

18.4.4 Control Module Power Management

18.4.4.1 Retention

The control module CORE instances are fully built with retention flip-flops (RFFs) and are powered in the CORE power domain; thus, they can be in active or retention mode. In contrast to the core control instances, the control wake-up instances are always powered and active. For more information about the device low-power states, see Section 3.1.1, *Device Power-Management Architecture Building Blocks*, in Chapter 3*, Power, Reset, and Clock Management*.

18.4.4.2 Power Management Protocols

The control module, which is slave on the L4 interconnect, does not support standby or idle mode protocols.

18.4.5 Hardware Requests

The control module does not generate DMA or wake-up requests. The general core control module generates one IRQ (THERMAL_ALERT) to the MPU (MPU_IRQ_126 line). For more information, see Section 17.3.2, *Interrupt Requests to INTC_MPU*.

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18.4.6 Control Module Initialization

The control module responds only to the internal POR and device type. At power on, reset values for the registers define the safe state for the device. In the initialization mode, only modules to be used at boot time are associated with the pads. Other module inputs are internally tied and outputs pads are turned off. After POR, software must set the pad functional multiplexing and configuration registers to the desired values according to the requested device configuration. For more information, see Section 28.1, *Initialization overview*.

The CONTROL_STATUS[5:0] SYS_BOOT bit field reflects the state of the sys_boot pads captured at POR in the PRCM module.

18.4.7 Control Module Instances

18.4.7.1 General Core Control Module Instance

The CTRL_MODULE_CORE instance contains most of the control logic that provides the hardware observability features for different digital phase-locked loop (DPLL) clockout and DPLL-specific signals, DMA requests, IRQs, and other internal hardware signals. The general core control provides the system boot decoding logic and has control over the standard eFuse settings. The system configuration registers, specific function controls, and some peripheral control and status registers are also mapped there.

The following register sets are available within the CTRL_MODULE_CORE:

- Observability control registers:
  - CONTROL_HWOBS_CONTROL
  - CONTROL_DEBOBS_FINAL_MUX_SEL
  - CONTROL_CONF_SDMA_REQ_SELx
  - CONTROL_CONF_CLK_SELx (where x = 0 to 2)
  - CONTROL_CONF_DPLL_X_SEL (where X = FREQLOCK, TINITZ, PHASELOCK, TENABLE, TENABLEDIV, BYPASSACK, IDLE)
  - CONTROL_CONF_DPLLCTRL_X_SEL (where X = PLLLOCK, PLLRECAL, STOPCLOCK, STOPCLOCKACKZ)
  - CONTROL_CONF_MMCX_X_SEL (where X = ADPIDLE, OCPL4IDLEREQ, OCPL3MWAIT, PIRFFRET, OCPL4SIDLEACKO1, OCPL4SIDLEACKO0, OCPL3MSTANDBYO, SWAKEUP)
- Part of the debug view channel selection registers: CONTROL_CORE_CONF_DEBUG_SEL_TST_X
- MMU address translation-related registers: CONTROL_CORTEX_M4_MMUADDRTRANSLTR and CONTROL_CORTEX_M4_MMUADDRLOGICTR
- Standard fuse registers: CONTROL_STD_FUSE_X
- Control status register: CONTROL_STATUS
- Different peripheral control registers.

18.4.7.2 General Wake-Up Control Module Instance

The following registers are associated with the CTRL_MODULE_WKUP instance:

- Register with spare bits: CONTROL_OCPREG_SPARE
- Part of the debug view channel selection registers: CONTROL_CONF_DEBUG_SEL_TST_X

18.4.7.3 Device Core Control Module Instance

The CTRL_MODULE_CORE_PAD instance provides the device-specific pad control features, such as pullup and pulldown I/O configuration and pad functional multiplexing. Wake-up control and status features are also subjects of the device core control.

The following registers are associated with this module:

- Different peripheral pad mode configuration and wake-up status and configuration registers, such as:
  - CONTROL_CORE_PAD0_X_PAD1_Y

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  - CONTROL_PADCONF_WAKEUPEVENTx
  - CONTROL_SMARTxIO
- Peripheral pad voltage-level control register: CONTROL_PADCONF_MODE
- Miscellaneous controls for different device interface modules: CONTROL_X registers, such as the CONTROL_EMIF register (including the CONTROL_EFUSE registers)

18.4.7.4 Device Wake-Up Control Module Instance

Configuration registers for all pads linked to the wake-up voltage domain are in the CTRL_MODULE_WKUP instance. The registers instantiated are:

- CONTROL_WKUP_PAD0_X_PAD1_Y registers for configuring FREF clock oscillator pads, reset signals, and power mode pad configurations
- Peripheral pad voltage-level control register: CONTROL_WKUP_PADCONF_MODE

Section 18.6.1, *Control Module Instance Summary*, shows the memory size and base addresses assigned to the different control module instances.

18.4.8 Pad Functional Multiplexing and Configuration

After POR, software must set the pad functional multiplexing and configuration registers to the desired values according to the requested device configuration. The configuration is controlled by pads or a group of pads. Each configurable pad has its own configuration register for pullup and pulldown control and for assignment to a given module.

Two sets of 32-bit registers provide the pad functional multiplexing and configuration feature of the control module. The first set of registers (CONTROL_CORE_PAD0_X_PAD1_Y) configures the pads in the CORE power domain. The second set of registers (CONTROL_WKUP_PAD0_X_PAD1_Y) configures the pads in the WKUP power domain.

The pad configuration as defined in this module is used in the IO_CTRL logic along with the gating and protection features. The gating feature is implemented for the output pads. The protection feature is implemented for input lines. These features implement additional control and multiplexing capabilities hard-wired in the IO_CTRL logic and driven by the state and/or logic of the internal device.

The gating feature allows forcing an output pad to a fixed value (Z, pullup, pulldown, 1, 0) or to a given internal signal. Each gating command is defined with a logic equation and the output state or value to be set on the pad when the logic equation is True.

The protection feature provides control on each input line of the control module when no pad is assigned to this input (protected value). When POR is released, the value on the pad is driven by the default configuration of the control module. This configuration is usually aligned with the default value selected on the I/O cell. The protected value can be logical level (0 or 1) or a signal from a pad; it is selected when none of the pad_x.MuxMod selects a device input.

Each 32-bit pad configuration register controls two pads: the first pad is controlled by the 16 least-significant bits (LSBs), and the second pad is controlled by the 16 most-significant bits (MSBs); thus, one pad configuration register provides control for two different pins. After POR, software sets the pad functional multiplexing and configuration registers to the requested device pad configurations. Data written in these registers directly commands the multiplexing of the pad configuration logic. Figure 18-5 shows the 16-bit-wide pad configuration register field associated with each pin.

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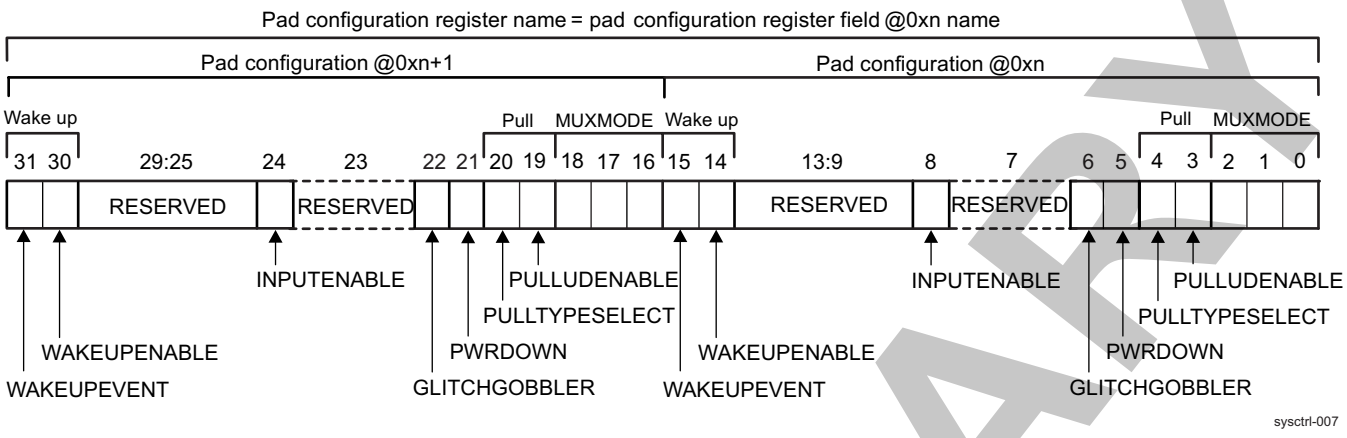
Figure 18-5. Pad Configuration Register Functionality



NOTE: These registers can be accessed using 8-, 16-, and 32-bit operations.

The functional bits of a pad configuration register field are divided into the following seven fields:

- MUXMODE (3 bits) defines the multiplexing mode applied to the pad. A mode corresponds to the selection of the function mapped on the pad with seven (0 to 6) possible functional modes for each pad.
- PULL (2 bits) for combinational pullup and pulldown configuration:
  - PULLTYPESELECT: Pullup and pulldown type selection for the pad
  - PULLUDENABLE: Enables pullup and pulldown feature for the pad
- INPUTENABLE (1 bit) drives an input enable signal to the I/O CTRL.
  - INPUTENABLE = 0: Input disable. Pad is configured only in output mode.
  - INPUTENABLE = 1: Input enable. Pad is configured in bidirectional mode.
- Wake-up bits (2 bits):
  - WAKEUPENABLE: Enable wake-up detection on input.
  - WAKEUPEVENT: Wake-up event status for the pad
- PWRDOWN (1 bit): The Power Down setting for the corresponding pad
  - PWRDOWN = 0: The I/O cell is powered.
  - PWRDOWN = 1: The I/O cell is not powered.
- GLITCHGOBBLER (1 bit): Enables/Disables glitch filtering
  - GLITCHGOBBLER = 0: The I/O cell does not filter outside glitches.
  - GLITCHGOBBLER = 1: The I/O cell filters outside glitches.

NOTE: The GLITCHGOBBLER bit is available only in several pad configuration registers at bit positions [22] or [6].

Figure 18-6 shows the pad configuration functionality.

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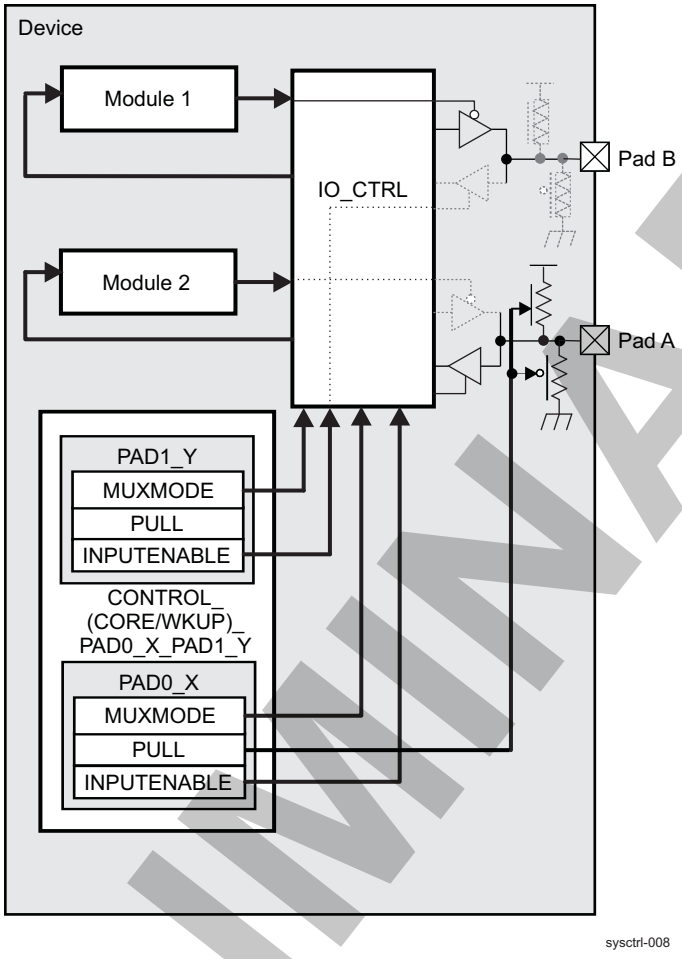
Figure 18-6. Pad Configuration Diagram



The I/O pads are controlled by software by:

- Writing to the CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y registers in the device control module for I/O and pullup and pulldown configuration
- Writing to the GPIOi.GPIO_OE registers in the GPIO module for I/O configuration

For more information about the GPIO module, see Section 25.4.8, *General-Purpose Interface Data Input/Output Capabilities*.

NOTE: For the proper functioning of the following modules, the INPUTENABLE bit in the corresponding pad configuration register must be set to 1 for pads configured to drive output clocks:

- GPMC
- I2Ci
- MMCi
- USB_HOST_HS
- MCPDM

The output clock is driven back and used for retiming of the modules.

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NOTE: For a correct configuration of each pad direction (input, output, bidirectional), the CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y and GPIOi.GPIO_OE registers must be written.

Table 18-5 lists the bit directions of the CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y registers.

Table 18-5. Bit Meanings for CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y Registers

Pad Configuration Bit	Bit Meaning	
	0	1
PULLUDENABLE	Not activated	Activated
PULLTYPESELECT	Pulldown	Pullup
INPUTENABLE	Input enable signal is inactive.	Input enable signal is active.
WAKEUPENABLE	Disable I/O wake-up function.	Enable I/O wake-up function.
WAKEUPEVENT	Wake-up event is not detected.	Wake-up event is detected.
MUXMODE bits	See Table 18-6	See Table 18-6
PWRDOWN	The I/O cell is powered.	The I/O cell is not powered.
GLITCHGOBBLER	Glitch filter disable	Glitch filter enable

18.4.8.1 Mode Selection

Table 18-6 lists the multiplexing modes and settings.

Table 18-6. Mode Selection

MUXMODE	Selected Mode
0b000	Primary mode = Mode 0
0b001	Mode 1
0b010	Mode 2
0b011	Mode 3
0b100	Mode 4
0b101	Mode 5
0b110	Mode 6
0b111	Safe mode = Mode 7

The MUXMODE field in the CONTROL_CORE_PAD0_X_PAD1_Y and CONTROL_WKUP_PAD0_X_PAD1_Y registers defines the multiplexing mode applied to the pad. Modes are referred to by their decimal (from 0 to 7) or binary (from 0b000 to 0b111) representation. Functional modes are defined from 0b000 to 0b110; mode 0b111 is referred to as the safe mode.

For most pads, the reset value for the MUXMODE field in the CONTROL_CORE_PAD0_X_PAD1_Y and CONTROL_WKUP_PAD0_X_PAD1_Y registers is 0b111. The exceptions are pads to be used at boot time to transfer data from selected peripherals to the external flash memory.

Mode 0 is the primary mode. When mode 0 is set, the function mapped to the pad corresponds to the name of the pad.

Modes 1–6 are possible modes for alternate functions. On each pad, some modes are used effectively for alternate functions, while other modes are unused and correspond to no functional configuration.

Safe mode (mode 7) avoids any risk of electrical contention by configuring the pad as an input with no functional interface mapped to it. Safe mode is used mainly as the default mode for all pads containing no mandatory interface at the release of POR.

NOTE: When a pad is set into a mux mode that is not defined by pad multiplexing, the pad is actually set undriven (Hi-Z) with potential pullup or pulldown.

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For more information about the configurable mode on each pad, see Table 18-8 and Table 18-9.

NOTE: Pad names are signal names available in mode 0.

18.4.8.2 Pull Selection

There is no automatic gating control to ensure that internal weak pulldown or pullup resistors on a pad are disconnected whenever pad is configured as output. If a pad is always configured in output mode, it is recommended for user software to disable any internal pull resistor tied to it, to avoid unnecessary consumption.

Table 18-7 describes the software controls available for pad internal pullup and pulldown resistors in the control module padconfiguration registers.

Table 18-7. Pull Selection

PULL		Pin Behavior
PULLTYPESELECT	PULLUDENABLE	
0b0	0b0	Pulldown selected but not activated
0b0	0b1	Pulldown selected and activated
0b1	0b0	Pullup selected but not activated
0b1	0b1	Pullup selected and activated

For more information about the pull available on each pad, see Table 18-8 and Table 18-9.

NOTE: Software controls for internal active mode pullups and pulldowns on the lpddr21_x and lpddr22_x pads are available in the CONTROL_LPDDR2CH1_0 and CONTROL_LPDDR2CH1_1 registers, respectively.

Software controls for internal active mode pullups and pulldowns on the usbb1_hsic_x, usbb2_hsic_x, and usbb3_hsic_x pads are available in the CONTROL_SMART3IO_PADCONF_1 register.

18.4.8.3 Pad Multiplexing Register Fields

Table 18-8 and Table 18-9 provide for each pad configuration register field the address offset and associated signal name for each multiplexing mode (as set by the MUXMODE bit field). Mode 0 is always defined. Modes with no signal name are undefined for the given pad. For more information about default pad configuration settings (POR values) for pads in the CORE power domain, see Section 18.6.3, *CTRL_MODULE_CORE_PAD Registers.* For pads in the WKUP power domain, see Section 18.6.5, *CTRL_MODULE_WKUP_PAD Registers*.

NOTE:

- Table 18-8 lists the pad configuration registers instantiated in the WKUP power domain that drive the pads in the WKUP power domain. Table 18-9 lists the pad configuration registers instantiated in the CORE power domain that drive the pads in the CORE power domain.
- In Table 18-8 and Table 18-9, an empty cell indicates that the mode or pull is not available for this pad.

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Table 18-8. Device Wake-Up Control Module Pad Configuration Register Fields

CTRL_MODULE_WKUP_PAD [Register name]	Address Offset	Mode 0[1]	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_LLIA_WAKEREQIN_PAD1_LLIB_WAKEREQIN[15:0]	0x040	llia_wakereqin	Reserved				hw_wkdbg14	gpio1_wk14	safe_mode_wakeup1
CONTROL_WKUP_PAD0_LLIA_WAKEREQIN_PAD1_LLIB_WAKEREQIN[31:16]	0x040	llib_wakereqin	Reserved				hw_wkdbg13	gpio1_wk15	safe_mode_wakeup0
CONTROL_WKUP_PAD0_DRM_EMU0_PAD1_DRM_EMU1[15:0]	0x044	drm_emu0					hw_wkdbg6	gpio1_wk6	safe_mode_wakeup2
CONTROL_WKUP_PAD0_DRM_EMU0_PAD1_DRM_EMU1[31:16]	0x044	drm_emu1					hw_wkdbg7	gpio1_wk7	safe_mode_wakeup3
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK[15:0]	0x048	jtag_ntrst							safe_mode_wakeup4
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK[31:16]	0x048	jtag_tck							safe_mode_wakeup5
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMSC[15:0]	0x04C	jtag_rtck							safe_mode_wakeup6
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMSC[31:16]	0x04C	jtag_tmsc							safe_mode_wakeup7
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO[15:0]	0x050	jtag_tdi							safe_mode_wakeup8
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO[31:16]	0x050	jtag_tdo							safe_mode_wakeup9
CONTROL_WKUP_PAD0_SYS_32K_PAD1_FREF_CLK_IOREQ[15:0]	0x054	sys_32k							
CONTROL_WKUP_PAD0_SYS_32K_PAD1_FREF_CLK_IOREQ[31:16]	0x054	fref_clk_ioreq						gpio1_wk13	safe_mode_wakeup10
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK1_OUT[15:0]	0x058	fref_clk0_out					hw_wkdbg9	gpio1_wk12	safe_mode_wakeup11

(1) For the pad-configuration registers in which multiplexing has only one signal set (available in muxmode 0), the MUXMODE bit is not implemented, and described as RESERVED. Software must keep this bit field at its default (POR) value.

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Table 18-8. Device Wake-Up Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_WKUP_PAD [Register name]	Address Offset	Mode 0[(1)]	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK1_OUT[31:16]	0x058	fref_clk1_out					hw_wkdbg5	gpio1_wk11	safe_mode_wakeup12
CONTROL_WKUP_PAD0_FREF_CLK2_OUT_PAD1_FREF_CLK2_REQ[15:0]	0x05C	fref_clk2_out					hw_wkdbg10	gpio1_wk10	safe_mode_wakeup13
CONTROL_WKUP_PAD0_FREF_CLK2_OUT_PAD1_FREF_CLK2_REQ[31:16]	0x05C	fref_clk2_req	fref_clk3_out		sys_ndmareq0		hw_wkdbg11	gpio1_wk9	safe_mode_wakeup14
CONTROL_WKUP_PAD0_FREF_CLK1_REQ_PAD1_SYS_NRESPWRON[15:0]	0x060	fref_clk1_req			sys_ndmareq1		hw_wkdbg12	gpio1_wk8	safe_mode_wakeup15
CONTROL_WKUP_PAD0_FREF_CLK1_REQ_PAD1_SYS_NRESPWRON[31:16]	0x060	sys_nrespwron							
CONTROL_WKUP_PAD0_SYS_NRESWARM_PAD1_SYS_PWR_REQ[15:0]	0x064	sys_nreswarm							
CONTROL_WKUP_PAD0_SYS_NRESWARM_PAD1_SYS_PWR_REQ[31:16]	0x064	sys_pwr_req					hw_wkdbg15		safe_mode_wakeup16
CONTROL_WKUP_PAD0_SYS_NIRQ1_PAD1_SYS_NIRQ2[15:0]	0x068	sys_nirq1						gpio1_wk16	
CONTROL_WKUP_PAD0_SYS_NIRQ1_PAD1_SYS_NIRQ2[31:16]	0x068	sys_nirq2						gpio1_wk17	
CONTROL_WKUP_PAD0_SR_PMIC_SCL_PAD1_SR_PMIC_SDA[15:0]	0x06C	sr_pmic_scl							
CONTROL_WKUP_PAD0_SR_PMIC_SCL_PAD1_SR_PMIC_SDA[31:16]	0x06C	sr_pmic_sda							
CONTROL_WKUP_PAD0_SYS_BOOT0_PAD1_SYS_BOOT1[15:0]	0x070	sys_boot0			drm_emu2	drm_emu15	hw_wkdbg0	gpio1_wkout0	safe_mode_wakeup17
CONTROL_WKUP_PAD0_SYS_BOOT0_PAD1_SYS_BOOT1[31:16]	0x070	sys_boot1			drm_emu3	drm_emu16	hw_wkdbg1	gpio1_wkout1	safe_mode_wakeup18
CONTROL_WKUP_PAD0_SYS_BOOT2_PAD1_SYS_BOOT3[15:0]	0x074	sys_boot2			drm_emu4	drm_emu17	hw_wkdbg2	gpio1_wkout2	safe_mode_wakeup19

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Table 18-8. Device Wake-Up Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_WKUP_PAD [Register name]	Address Offset	Mode 0[(1)]	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_SYS_BOOT2_PAD1_SYS_BOOT3[31:16]	0x074	sys_boot3			drm_emu5	drm_emu18	hw_wkdbg3	gpio1_wkout3	safe_mode_wakeup20
CONTROL_WKUP_PAD0_SYS_BOOT4_PAD1_SYS_BOOT5[15:0]	0x078	sys_boot4			drm_emu6	drm_emu19	hw_wkdbg4	gpio1_wkout4	safe_mode_wakeup21
CONTROL_WKUP_PAD0_SYS_BOOT4_PAD1_SYS_BOOT5[31:16]	0x078	sys_boot5	Reserved				hw_wkdbg8	gpio1_wkout5	safe_mode_wakeup22

Table 18-9. Device Core Control Module Pad Configuration Register Fields

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_EMMC_CLK_PAD1_EMMC_CMD[15:0]	0x040	emmc_clk						gpio2_46	safe_mode_core0
CONTROL_CORE_PAD0_EMMC_CLK_PAD1_EMMC_CMD[31:16]	0x040	emmc_cmd						gpio2_47	safe_mode_core1
CONTROL_CORE_PAD0_EMMC_DATA0_PAD1_EMMC_DATA1[15:0]	0x044	emmc_data0						gpio2_48	safe_mode_core2
CONTROL_CORE_PAD0_EMMC_DATA0_PAD1_EMMC_DATA1[31:16]	0x044	emmc_data1						gpio2_49	safe_mode_core3
CONTROL_CORE_PAD0_EMMC_DATA2_PAD1_EMMC_DATA3[15:0]	0x048	emmc_data2						gpio2_50	safe_mode_core4
CONTROL_CORE_PAD0_EMMC_DATA2_PAD1_EMMC_DATA3[31:16]	0x048	emmc_data3						gpio2_51	safe_mode_core5
CONTROL_CORE_PAD0_EMMC_DATA4_PAD1_EMMC_DATA5[15:0]	0x04C	emmc_data4						gpio2_52	safe_mode_core6
CONTROL_CORE_PAD0_EMMC_DATA4_PAD1_EMMC_DATA5[31:16]	0x04C	emmc_data5						gpio2_53	safe_mode_core7
CONTROL_CORE_PAD0_EMMC_DATA6_PAD1_EMMC_DATA7[15:0]	0x050	emmc_data6						gpio2_54	safe_mode_core8

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_EMMC_DATA6_PAD1_EMMC_DATA7[31:16]	0x050	emmc_data7						gpio2_55	safe_mode_core9
CONTROL_CORE_PAD0_C2C_CLKOUT0_PAD1_C2C_CLKOUT1[15:0]	0x054	Reserved				gpmc_nadv_ale		gpio2_33	safe_mode_core20
CONTROL_CORE_PAD0_C2C_CLKOUT0_PAD1_C2C_CLKOUT1[31:16]	0x054	Reserved			kbd_col8	gpmc_nbe0_cle		gpio2_34	safe_mode_core21
CONTROL_CORE_PAD0_C2C_CLKIN0_PAD1_C2C_CLKIN1[15:0]	0x058	Reserved				gpmc_nwp	gpmc_nbe1	gpio2_35	safe_mode_core19
CONTROL_CORE_PAD0_C2C_CLKIN0_PAD1_C2C_CLKIN1[31:16]	0x058	Reserved			kbd_row8	gpmc_clk		gpio2_36	safe_mode_core18
CONTROL_CORE_PAD0_C2C_DATAIN0_PAD1_C2C_DATAIN1[15:0]	0x05C	Reserved			kbd_row0	gpmc_ad0		gpio2_37	safe_mode_core10
CONTROL_CORE_PAD0_C2C_DATAIN0_PAD1_C2C_DATAIN1[31:16]	0x05C	Reserved			kbd_row1	gpmc_ad1		gpio2_38	safe_mode_core11
CONTROL_CORE_PAD0_C2C_DATAIN2_PAD1_C2C_DATAIN3[15:0]	0x060	Reserved			kbd_row2	gpmc_ad2		gpio2_39	safe_mode_core12
CONTROL_CORE_PAD0_C2C_DATAIN2_PAD1_C2C_DATAIN3[31:16]	0x060	Reserved			kbd_row3	gpmc_ad3		gpio2_40	safe_mode_core13
CONTROL_CORE_PAD0_C2C_DATAIN4_PAD1_C2C_DATAIN5[15:0]	0x064	Reserved			kbd_row4	gpmc_ad4		gpio2_41	safe_mode_core14
CONTROL_CORE_PAD0_C2C_DATAIN4_PAD1_C2C_DATAIN5[31:16]	0x064	Reserved			kbd_row5	gpmc_ad5		gpio2_42	safe_mode_core15
CONTROL_CORE_PAD0_C2C_DATAIN6_PAD1_C2C_DATAIN7[15:0]	0x068	Reserved			kbd_row6	gpmc_ad6		gpio2_43	safe_mode_core16
CONTROL_CORE_PAD0_C2C_DATAIN6_PAD1_C2C_DATAIN7[31:16]	0x068	Reserved			kbd_row7	gpmc_ad7		gpio2_44	safe_mode_core17
CONTROL_CORE_PAD0_C2C_DATAOUT0_PAD1_C2C_DATAOUT1[15:0]	0x06C	Reserved			kbd_col0	gpmc_ad8	hw_dbg16	gpio2_56	safe_mode_core22

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_C2C_DATAOUT0_PAD1_C2C_DATAOUT1[31:16]	0x06C	Reserved			kbd_col1	gpmc_ad9	hw_dbg17	gpio2_57	safe_mode_core23
CONTROL_CORE_PAD0_C2C_DATAOUT2_PAD1_C2C_DATAOUT3[15:0]	0x070	Reserved			kbd_col2	gpmc_ad10	hw_dbg18	gpio2_58	safe_mode_core24
CONTROL_CORE_PAD0_C2C_DATAOUT2_PAD1_C2C_DATAOUT3[31:16]	0x070	Reserved			kbd_col3	gpmc_ad11	hw_dbg19	gpio2_59	safe_mode_core25
CONTROL_CORE_PAD0_C2C_DATAOUT4_PAD1_C2C_DATAOUT5 [15:0]	0x074	Reserved			kbd_col4	gpmc_ad12	hw_dbg20	gpio2_60	safe_mode_core26
CONTROL_CORE_PAD0_C2C_DATAOUT4_PAD1_C2C_DATAOUT5[31:16]	0x074	Reserved			kbd_col5	gpmc_ad13	hw_dbg21	gpio2_61	safe_mode_core27
CONTROL_CORE_PAD0_C2C_DATAOUT6_PAD1_C2C_DATAOUT7[15:0]	0x078	Reserved			kbd_col6	gpmc_ad14	hw_dbg22	gpio2_62	safe_mode_core28
CONTROL_CORE_PAD0_C2C_DATAOUT6_PAD1_C2C_DATAOUT7[31:16]	0x078	Reserved			kbd_col7	gpmc_ad15	hw_dbg23	gpio2_63	safe_mode_core29
CONTROL_CORE_PAD0_C2C_DATA8_PAD1_C2C_DATA9[15:0]	0x07C	Reserved				gpmc_a16	hw_dbg24	gpio4_113	safe_mode_core30
CONTROL_CORE_PAD0_C2C_DATA8_PAD1_C2C_DATA9[31:16]	0x07C	Reserved				gpmc_a17	hw_dbg25	gpio4_114	safe_mode_core31
CONTROL_CORE_PAD0_C2C_DATA10_PAD1_C2C_DATA11[15:0]	0x080	Reserved				gpmc_a18	hw_dbg26	gpio4_115	safe_mode_core32
CONTROL_CORE_PAD0_C2C_DATA10_PAD1_C2C_DATA11[31:16]	0x080	Reserved				gpmc_a19	hw_dbg27	gpio4_116	safe_mode_core33
CONTROL_CORE_PAD0_C2C_DATA12_PAD1_C2C_DATA13[15:0]	0x084	Reserved				gpmc_a20	hw_dbg28	gpio4_117	safe_mode_core34
CONTROL_CORE_PAD0_C2C_DATA12_PAD1_C2C_DATA13[31:16]	0x084	Reserved				gpmc_a21	hw_dbg29	gpio4_118	safe_mode_core35
CONTROL_CORE_PAD0_C2C_DATA14_PAD1_C2C_DATA15[15:0]	0x088	Reserved				gpmc_a22	hw_dbg30	gpio4_119	safe_mode_core36

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_C2C_DATA14_PAD1_C2C_DATA15[31:16]	0x088	Reserved				gpmc_a23	hw_dbg31	gpio4_120	safe_mode_core37
CONTROL_CORE_PAD0_LLIA_WAKEREQOUT_PAD1_LLIB_WAKEREQOUT[15:0]	0x08C	llia_wakereqout	Reserved			gpmc_wait0		gpio2_45	safe_mode_core39
CONTROL_CORE_PAD0_LLIA_WAKEREQOUT_PAD1_LLIB_WAKEREQOUT[31:16]	0x08C	llib_wakereqout				gpmc_ncs0		gpio2_32	safe_mode_core38
CONTROL_CORE_PAD0_HSI1_ACREADY_PAD1_HSI1_CAREADY[15:0]	0x090	hsi1_acready	cam_strobe		usbb2_ulpitll_clk			gpio3_64	safe_mode_core40
CONTROL_CORE_PAD0_HSI1_ACREADY_PAD1_HSI1_CAREADY[31:16]	0x090	hsi1_caready			usbb2_ulpitll_nxt			gpio3_65	safe_mode_core41
CONTROL_CORE_PAD0_HSI1_ACWAKE_PAD1_HSI1_CAWAKE[15:0]	0x094	hsi1_acwake			usbb2_ulpitll_dir			gpio3_66	safe_mode_core42
CONTROL_CORE_PAD0_HSI1_ACWAKE_PAD1_HSI1_CAWAKE[31:16]	0x094	hsi1_cawake			usbb2_ulpitll_stp			gpio3_67	safe_mode_core43
CONTROL_CORE_PAD0_HSI1_ACFLAG_PAD1_HSI1_ACDATA[15:0]	0x098	hsi1_acflag			usbb2_ulpitll_data0			gpio3_68	safe_mode_core44
CONTROL_CORE_PAD0_HSI1_ACFLAG_PAD1_HSI1_ACDATA[31:16]	0x098	hsi1_acdata			usbb2_ulpitll_data1			gpio3_69	safe_mode_core45
CONTROL_CORE_PAD0_HSI1_CAFLAG_PAD1_HSI1_CADATA[15:0]	0x09C	hsi1_caflag			usbb2_ulpitll_data2			gpio3_70	safe_mode_core46
CONTROL_CORE_PAD0_HSI1_CAFLAG_PAD1_HSI1_CADATA[31:16]	0x09C	hsi1_cadata			usbb2_ulpitll_data3			gpio3_71	safe_mode_core47
CONTROL_CORE_PAD0_UART1_TX_PAD1_UART1_CTS[15:0]	0x0A0	uart1_tx			usbb2_ulpitll_data4			gpio3_72	safe_mode_core48
CONTROL_CORE_PAD0_UART1_TX_PAD1_UART1_CTS[31:16]	0x0A0	uart1_cts			usbb2_ulpitll_data5	gpmc_wait3		gpio3_73	safe_mode_core49
CONTROL_CORE_PAD0_UART1_RX_PAD1_UART1_RTS[15:0]	0x0A4	uart1_rx			usbb2_ulpitll_data6			gpio3_74	safe_mode_core50

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_UART1_RX_PAD1_UART1_RTS[31:16]	0x0A4	uart1_rts			usbb2_ulpitll_data7	gpmc_ncs7		gpio3_75	safe_mode_core51
CONTROL_CORE_PAD0_HSI2_CAREADY_PAD1_HSI2_ACREADY[15:0]	0x0A8	hsi2_caready			usbb1_ulpiphy_clk	gpmc_wait1		gpio3_76	safe_mode_core52
CONTROL_CORE_PAD0_HSI2_CAREADY_PAD1_HSI2_ACREADY[31:16]	0x0A8	hsi2_acready			usbb1_ulpiphy_nxt	gpmc_ncs1		gpio3_77	safe_mode_core53
CONTROL_CORE_PAD0_HSI2_CAWAKE_PAD1_HSI2_ACWAKE[15:0]	0x0AC	hsi2_cawake			usbb1_ulpiphy_dir	gpmc_a24		gpio3_78	safe_mode_core54
CONTROL_CORE_PAD0_HSI2_CAWAKE_PAD1_HSI2_ACWAKE[31:16]	0x0AC	hsi2_acwake			usbb1_ulpiphy_stp	gpmc_a25		gpio3_79	safe_mode_core55
CONTROL_CORE_PAD0_HSI2_CAFLAG_PAD1_HSI2_CADATA[15:0]	0x0B0	hsi2_caflag			usbb1_ulpiphy_data0	gpmc_wait2		gpio3_80	safe_mode_core56
CONTROL_CORE_PAD0_HSI2_CAFLAG_PAD1_HSI2_CADATA[31:16]	0x0B0	hsi2_cadata			usbb1_ulpiphy_data1	gpmc_ncs2		gpio3_81	safe_mode_core57
CONTROL_CORE_PAD0_HSI2_ACFLAG_PAD1_HSI2_ACDATA[15:0]	0x0B4	hsi2_acflag			usbb1_ulpiphy_data2	gpmc_ncs3		gpio3_82	safe_mode_core58
CONTROL_CORE_PAD0_HSI2_ACFLAG_PAD1_HSI2_ACDATA[31:16]	0x0B4	hsi2_acdata			usbb1_ulpiphy_data3	gpmc_ncs4		gpio3_83	safe_mode_core59
CONTROL_CORE_PAD0_UART2_RTS_PAD1_UART2_CTS[15:0]	0x0B8	uart2_rts	mcspi3_somi		usbb1_ulpiphy_data4	gpmc_nwe	hw_dbg16	gpio3_84	safe_mode_core60
CONTROL_CORE_PAD0_UART2_RTS_PAD1_UART2_CTS[31:16]	0x0B8	uart2_cts	mcspi3_cs0		usbb1_ulpiphy_data5	gpmc_noe_nre	hw_dbg17	gpio3_85	safe_mode_core61
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[15:0]	0x0BC	uart2_rx	mcspi3_simo		usbb1_ulpiphy_data6	gpmc_ncs5	hw_dbg18	gpio3_86	safe_mode_core62
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[31:16]	0x0BC	uart2_tx	mcspi3_clk		usbb1_ulpiphy_data7	gpmc_ncs6	hw_dbg19	gpio3_87	safe_mode_core63
CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBB1_HSIC_DATA[15:0]	0x0C0	usbb1_hsic_strobe						gpio3_92	safe_mode_core64

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBB1_HSIC_DATA[31:16]	0x0C0	usbb1_hsic_data						gpio3_93	safe_mode_core65
CONTROL_CORE_PAD0_USBB2_HSIC_STROBE_PAD1_USBB2_HSIC_DATA[15:0]	0x0C4	usbb2_hsic_strobe						gpio3_94	safe_mode_core66
CONTROL_CORE_PAD0_USBB2_HSIC_STROBE_PAD1_USBB2_HSIC_DATA[31:16]	0x0C4	usbb2_hsic_data						gpio3_95	safe_mode_core67
CONTROL_CORE_PAD0_TIMER10_PWM_EVT_PAD1_DSIPORTA_TE0[15:0]	0x0C8	timer10_pwm_evt						gpio6_188	safe_mode_core68
CONTROL_CORE_PAD0_TIMER10_PWM_EVT_PAD1_DSIPORTA_TE0[31:16]	0x0C8	dsiporta_te0						gpio6_189	safe_mode_core69
CONTROL_CORE_PAD0_DSIPORTA_LANE0X_PAD1_DSIPORTA_LANE0Y[15:0]	0x0CC	dsiporta_lane0x							
CONTROL_CORE_PAD0_DSIPORTA_LANE0X_PAD1_DSIPORTA_LANE0Y[31:16]	0x0CC	dsiporta_lane0y							
CONTROL_CORE_PAD0_DSIPORTA_LANE1X_PAD1_DSIPORTA_LANE1Y[15:0]	0x0D0	dsiporta_lane1x							
CONTROL_CORE_PAD0_DSIPORTA_LANE1X_PAD1_DSIPORTA_LANE1Y[31:16]	0x0D0	dsiporta_lane1y							
CONTROL_CORE_PAD0_DSIPORTA_LANE2X_PAD1_DSIPORTA_LANE2Y[15:0]	0x0D4	dsiporta_lane2x							
CONTROL_CORE_PAD0_DSIPORTA_LANE2X_PAD1_DSIPORTA_LANE2Y[31:16]	0x0D4	dsiporta_lane2y							
CONTROL_CORE_PAD0_DSIPORTA_LANE3X_PAD1_DSIPORTA_LANE3Y[15:0]	0x0D8	dsiporta_lane3x							
CONTROL_CORE_PAD0_DSIPORTA_LANE3X_PAD1_DSIPORTA_LANE3Y[31:16]	0x0D8	dsiporta_lane3y							
CONTROL_CORE_PAD0_DSIPORTA_LANE4X_PAD1_DSIPORTA_LANE4Y[15:0]	0x0DC	dsiporta_lane4x							

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_DSIPORTA_LANE4X_PAD1_DSIPORTA_LANE4Y[31:16]	0x0DC	dsiporta_lane4y							
CONTROL_CORE_PAD0_DSIPORTC_LANE0X_PAD1_DSIPORTC_LANE0Y[15:0]	0x0E0	dsiportc_lane0x							
CONTROL_CORE_PAD0_DSIPORTC_LANE0X_PAD1_DSIPORTC_LANE0Y[31:16]	0x0E0	dsiportc_lane0y							
CONTROL_CORE_PAD0_DSIPORTC_LANE1X_PAD1_DSIPORTC_LANE1Y[15:0]	0x0E4	dsiportc_lane1x							
CONTROL_CORE_PAD0_DSIPORTC_LANE1X_PAD1_DSIPORTC_LANE1Y[31:16]	0x0E4	dsiportc_lane1y							
CONTROL_CORE_PAD0_DSIPORTC_LANE2X_PAD1_DSIPORTC_LANE2Y[15:0]	0x0E8	dsiportc_lane2x							
CONTROL_CORE_PAD0_DSIPORTC_LANE2X_PAD1_DSIPORTC_LANE2Y[31:16]	0x0E8	dsiportc_lane2y							
CONTROL_CORE_PAD0_DSIPORTC_LANE3X_PAD1_DSIPORTC_LANE3Y[15:0]	0x0EC	dsiportc_lane3x							
CONTROL_CORE_PAD0_DSIPORTC_LANE3X_PAD1_DSIPORTC_LANE3Y[31:16]	0x0EC	dsiportc_lane3y							
CONTROL_CORE_PAD0_DSIPORTC_LANE4X_PAD1_DSIPORTC_LANE4Y[15:0]	0x0F0	dsiportc_lane4x							
CONTROL_CORE_PAD0_DSIPORTC_LANE4X_PAD1_DSIPORTC_LANE4Y[31:16]	0x0F0	dsiportc_lane4y							
CONTROL_CORE_PAD0_DSIPORTC_TE0_PAD1_TIMER9_PWM_EVT[15:0]	0x0F4	dsiportc_te0						gpio6_191	safe_mode_core71
CONTROL_CORE_PAD0_DSIPORTC_TE0_PAD1_TIMER9_PWM_EVT[31:16]	0x0F4	timer9_pwm_evt	sync_sof_clk	sync_usof_itp_clk				gpio6_190	safe_mode_core70
CONTROL_CORE_PAD0_I2C4_SCL_PAD1_I2C4_SDA[15:0]	0x0F8	i2c4_scl	jtagtapext_tdi					gpio7_200	safe_mode_core104

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_I2C4_SCL_PAD1_I2C4_SDA[31:16]	0x0F8	i2c4_sda	jtagtapext_rtck					gpio7_201	safe_mode_core105
CONTROL_CORE_PAD0_MCSPI2_CLK_PAD1_MCSPI2_SIMO[15:0]	0x0FC	mcspi2_clk	jtagtapext_tck					gpio7_197	safe_mode_core101
CONTROL_CORE_PAD0_MCSPI2_CLK_PAD1_MCSPI2_SIMO[31:16]	0x0FC	mcspi2_simo	jtagtapext_tmsc				hw_dbg20	gpio7_198	safe_mode_core102
CONTROL_CORE_PAD0_MCSPI2_SOMI_PAD1_MCSPI2_CS0[15:0]	0x100	mcspi2_somi	jtagtapext_tdo				hw_dbg21	gpio7_199	safe_mode_core103
CONTROL_CORE_PAD0_MCSPI2_SOMI_PAD1_MCSPI2_CS0[31:16]	0x100	mcspi2_cs0	jtagtapext_ntrst		dispc_fid			gpio7_196	safe_mode_core100
CONTROL_CORE_PAD0_RFBI_DATA15_PAD1_RFBI_DATA14[15:0]	0x104	rfbi_data15	mcspi2_cs1		dispc_data15	kbd_col6	drm_emu19	gpio6_181	safe_mode_core83
CONTROL_CORE_PAD0_RFBI_DATA15_PAD1_RFBI_DATA14[31:16]	0x104	rfbi_data14			dispc_data14	kbd_col7	drm_emu18	gpio6_180	safe_mode_core82
CONTROL_CORE_PAD0_RFBI_DATA13_PAD1_RFBI_DATA12[15:0]	0x108	rfbi_data13			dispc_data13	kbd_col8	drm_emu17	gpio6_179	safe_mode_core81
CONTROL_CORE_PAD0_RFBI_DATA13_PAD1_RFBI_DATA12[31:16]	0x108	rfbi_data12			dispc_data12	kbd_row6	drm_emu16	gpio6_178	safe_mode_core80
CONTROL_CORE_PAD0_RFBI_DATA11_PAD1_RFBI_DATA10[15:0]	0x10C	rfbi_data11			dispc_data11	kbd_row7	drm_emu15	gpio6_177	safe_mode_core79
CONTROL_CORE_PAD0_RFBI_DATA11_PAD1_RFBI_DATA10[31:16]	0x10C	rfbi_data10			dispc_data10	kbd_row8	drm_emu14	gpio6_176	safe_mode_core78
CONTROL_CORE_PAD0_RFBI_DATA9_PAD1_RFBI_DATA8[15:0]	0x110	rfbi_data9			dispc_data9	kbd_row3	drm_emu13	gpio6_175	safe_mode_core77
CONTROL_CORE_PAD0_RFBI_DATA9_PAD1_RFBI_DATA8[31:16]	0x110	rfbi_data8			dispc_data8	kbd_col3	drm_emu12	gpio6_174	safe_mode_core76
CONTROL_CORE_PAD0_RFBI_DATA7_PAD1_RFBI_DATA6[15:0]	0x114	rfbi_data7			dispc_data7	jtagtapext_tdi	drm_emu11	gpio6_173	safe_mode_core97

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_RFBI_DATA7_PAD1_RFBI_DATA6[31:16]	0x114	rfbi_data6			dispc_data6	jtagtapext_tdo	drm_emu10	gpio6_172	safe_mode_core96
CONTROL_CORE_PAD0_RFBI_DATA5_PAD1_RFBI_DATA4[15:0]	0x118	rfbi_data5			dispc_data5	jtagtapext_tmsc	drm_emu9	gpio6_171	safe_mode_core95
CONTROL_CORE_PAD0_RFBI_DATA5_PAD1_RFBI_DATA4[31:16]	0x118	rfbi_data4			dispc_data4	jtagtapext_tck	drm_emu8	gpio6_170	safe_mode_core94
CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2[15:0]	0x11C	rfbi_data3			dispc_data3	jtagtapext_ntrst	drm_emu7	gpio6_169	safe_mode_core93
CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2[31:16]	0x11C	rfbi_data2			dispc_data2	uart3_tx_irtx	drm_emu6	gpio6_168	safe_mode_core92
CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[15:0]	0x120	rfbi_data1			dispc_data1	uart3_rx_irrx	drm_emu5	gpio6_167	safe_mode_core91
CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[31:16]	0x120	rfbi_data0			dispc_data0	jtagtapext_rtck	drm_emu4	gpio6_166	safe_mode_core90
CONTROL_CORE_PAD0_RFBI_WE_PAD1_RFBI_CS0[15:0]	0x124	rfbi_we			dispc_vsync		drm_emu2	gpio6_162	safe_mode_core99
CONTROL_CORE_PAD0_RFBI_WE_PAD1_RFBI_CS0[31:16]	0x124	rfbi_cs0			dispc_hsync		drm_emu3	gpio6_163	safe_mode_core98
CONTROL_CORE_PAD0_RFBI_A0_PAD1_RFBI_RE[15:0]	0x128	rfbi_a0			dispc_de	kbd_row4		gpio6_165	safe_mode_core75
CONTROL_CORE_PAD0_RFBI_A0_PAD1_RFBI_RE[31:16]	0x128	rfbi_re			dispc_pclk	kbd_col4		gpio6_164	safe_mode_core74
CONTROL_CORE_PAD0_RFBI_HSYNC0_PAD1_RFBI_TE_VSYNC0[15:0]	0x12C	rfbi_hsync0			dispc_data17	kbd_col5		gpio6_160	safe_mode_core72
CONTROL_CORE_PAD0_RFBI_HSYNC0_PAD1_RFBI_TE_VSYNC0[31:16]	0x12C	rfbi_te_vsync0			dispc_data16	kbd_row5	jtag_sel	gpio6_161	safe_mode_core73
CONTROL_CORE_PAD0_GPIO6_182_PAD1_GPIO6_183[15:0]	0x130	gpio6_182			dispc_data18	kbd_col0		gpio6_182	safe_mode_core84
CONTROL_CORE_PAD0_GPIO6_182_PAD1_GPIO6_183[31:16]	0x130	gpio6_183			dispc_data19	kbd_col1		gpio6_183	safe_mode_core85

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_GPIO6_184_PAD1_GPIO6_185[15:0]	0x134	gpio6_184			dispc_data20	kbd_col2	hw_dbg22	gpio6_184	safe_mode_core86
CONTROL_CORE_PAD0_GPIO6_184_PAD1_GPIO6_185[31:16]	0x134	gpio6_185			dispc_data21	kbd_row0	hw_dbg23	gpio6_185	safe_mode_core87
CONTROL_CORE_PAD0_GPIO6_186_PAD1_GPIO6_187[15:0]	0x138	gpio6_186			dispc_data22	kbd_row1	hw_dbg24	gpio6_186	safe_mode_core88
CONTROL_CORE_PAD0_GPIO6_186_PAD1_GPIO6_187[31:16]	0x138	gpio6_187			dispc_data23	kbd_row2	hw_dbg25	gpio6_187	safe_mode_core89
CONTROL_CORE_PAD0_HDMI_CEC_PAD1_HDMI_HPD[15:0]	0x13C	hdmi_cec						gpio7_192	safe_mode_core106
CONTROL_CORE_PAD0_HDMI_CEC_PAD1_HDMI_HPD[31:16]	0x13C	hdmi_hpd						gpio7_193	safe_mode_core107
CONTROL_CORE_PAD0_HDMI_DDC_SCL_PAD1_HDMI_DDC_SDA[15:0]	0x140	hdmi_ddc_scl						gpio7_194	safe_mode_core108
CONTROL_CORE_PAD0_HDMI_DDC_SCL_PAD1_HDMI_DDC_SDA[31:16]	0x140	hdmi_ddc_sda						gpio7_195	safe_mode_core109
CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[15:0]	0x144	csiportc_lane0x			cpi_data9			gpio8_in253	safe_mode_core127
CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[31:16]	0x144	csiportc_lane0y			cpi_data8			gpio8_in252	safe_mode_core126
CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[15:0]	0x148	csiportc_lane1x			cpi_data11			gpio8_in255	safe_mode_core129
CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[31:16]	0x148	csiportc_lane1y			cpi_data10			gpio8_in254	safe_mode_core128
CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[15:0]	0x14C	csiportb_lane0x				cpi_data12		gpio8_in246	safe_mode_core120
CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[31:16]	0x14C	csiportb_lane0y				cpi_data13		gpio8_in247	safe_mode_core121

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[15:0]	0x150	csiportb_lane1x				cpi_data15		gpio8_in249	safe_mode_core123
CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[31:16]	0x150	csiportb_lane1y				cpi_data14		gpio8_in248	safe_mode_core122
CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[15:0]	0x154	csiportb_lane2x				cpi_vsyncin		gpio8_in251	safe_mode_core125
CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[31:16]	0x154	csiportb_lane2y				cpi_hsyncin		gpio8_in250	safe_mode_core124
CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[15:0]	0x158	csiporta_lane0x			cpi_pclk			gpio8_in236	safe_mode_core110
CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[31:16]	0x158	csiporta_lane0y			cpi_wen			gpio8_in237	safe_mode_core111
CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[15:0]	0x15C	csiporta_lane1x			cpi_data1			gpio8_in239	safe_mode_core113
CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[31:16]	0x15C	csiporta_lane1y			cpi_data0			gpio8_in238	safe_mode_core112
CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[15:0]	0x160	csiporta_lane2x			cpi_data3			gpio8_in241	safe_mode_core115
CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[31:16]	0x160	csiporta_lane2y			cpi_data2			gpio8_in240	safe_mode_core114
CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[15:0]	0x164	csiporta_lane3x			cpi_data4			gpio8_in242	safe_mode_core116
CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[31:16]	0x164	csiporta_lane3y			cpi_data5			gpio8_in243	safe_mode_core117
CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[15:0]	0x168	csiporta_lane4x			cpi_data6			gpio8_in244	safe_mode_core118
CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[31:16]	0x168	csiporta_lane4y			cpi_data7			gpio8_in245	safe_mode_core119

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE[15:0]	0x16C	cam_shutter					sys_nodeid0	gpio8_224	safe_mode_core130
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE[31:16]	0x16C	cam_strobe					sys_nodeid1	gpio8_225	safe_mode_core131
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_TIMER11_PWM_EVT[15:0]	0x170	cam_globalreset	cam_shutter		cpi_fid			gpio8_226	safe_mode_core132
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_TIMER11_PWM_EVT[31:16]	0x170	timer11_pwm_evt		uart1_tx	cpi_data12		hw_dbg26	gpio8_227	safe_mode_core133
CONTROL_CORE_PAD0_TIMER5_PWM_EVT_PAD1_TIMER6_PWM_EVT[15:0]	0x174	timer5_pwm_evt	sdcard_cd	uart1_cts	cpi_data13			gpio8_228	safe_mode_core134
CONTROL_CORE_PAD0_TIMER5_PWM_EVT_PAD1_TIMER6_PWM_EVT[31:16]	0x174	timer6_pwm_evt	sdcard_wp	uart1_rx	cpi_data14			gpio8_229	safe_mode_core135
CONTROL_CORE_PAD0_TIMER8_PWM_EVT_PAD1_I2C3_SCL[15:0]	0x178	timer8_pwm_evt	sdcard_wp	uart1_rts	cpi_data15		hw_dbg27	gpio8_230	safe_mode_core136
CONTROL_CORE_PAD0_TIMER8_PWM_EVT_PAD1_I2C3_SCL[31:16]	0x178	i2c3_scl						gpio8_231	safe_mode_core137
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_GPIO8_233[15:0]	0x17C	i2c3_sda						gpio8_232	safe_mode_core138
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_GPIO8_233[31:16]	0x17C	gpio8_233	Reserved	timer8_pwm_evt	cpi_hsync			gpio8_233	safe_mode_core139
CONTROL_CORE_PAD0_GPIO8_234_PAD1_ABE_CLKS[15:0]	0x180	gpio8_234	Reserved		cpi_vsync			gpio8_234	safe_mode_core140
CONTROL_CORE_PAD0_GPIO8_234_PAD1_ABE_CLKS[31:16]	0x180	abe_clks			abemcasp_axr			gpio4_96	safe_mode_core141
CONTROL_CORE_PAD0_ABEDMIC_DIN1_PAD1_ABEDMIC_DIN2[15:0]	0x184	abedmic_din1			abemcasp_ahclkr	abemcbsp3_fsx		gpio4_97	safe_mode_core142
CONTROL_CORE_PAD0_ABEDMIC_DIN1_PAD1_ABEDMIC_DIN2[31:16]	0x184	abedmic_din2			abemcasp_axr	abemcbsp3_dx		gpio4_98	safe_mode_core143

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_ABEDMIC_DIN3_PAD1_ABEDMIC_CLK1[15:0]	0x188	abedmic_din3				abemcbsp3_dr		gpio4_99	safe_mode_core144
CONTROL_CORE_PAD0_ABEDMIC_DIN3_PAD1_ABEDMIC_CLK1[31:16]	0x188	abedmic_clk1				abemcbsp3_clkx		gpio4_100	safe_mode_core145
CONTROL_CORE_PAD0_ABEDMIC_CLK2_PAD1_ABEDMIC_CLK3[15:0]	0x18C	abedmic_clk2	abemcbsp1_fsx		abemcasp_amutein			gpio4_101	safe_mode_core146
CONTROL_CORE_PAD0_ABEDMIC_CLK2_PAD1_ABEDMIC_CLK3[31:16]	0x18C	abedmic_clk3	abemcbsp1_dx		abemcasp_aclkx			gpio4_102	safe_mode_core147
CONTROL_CORE_PAD0_ABESLIMBUS1_CLOCK_PAD1_ABESLIMBUS1_DATA[15:0]	0x190	abeslimbus1_clock	abemcbsp1_clkx		abemcasp_afsr			gpio4_103	safe_mode_core148
CONTROL_CORE_PAD0_ABESLIMBUS1_CLOCK_PAD1_ABESLIMBUS1_DATA[31:16]	0x190	abeslimbus1_data	abemcbsp1_dr		abemcasp_aclkr			gpio4_104	safe_mode_core149
CONTROL_CORE_PAD0_ABEMCBSP2_DR_PAD1_ABEMCBSP2_DX[15:0]	0x194	abemcbsp2_dr			abemcasp_axr			gpio4_105	safe_mode_core150
CONTROL_CORE_PAD0_ABEMCBSP2_DR_PAD1_ABEMCBSP2_DX[31:16]	0x194	abemcbsp2_dx			abemcasp_amuteout			gpio4_106	safe_mode_core151
CONTROL_CORE_PAD0_ABEMCBSP2_FSX_PAD1_ABEMCBSP2_CLKX[15:0]	0x198	abemcbsp2_fsx			abemcasp_afsx			gpio4_107	safe_mode_core152
CONTROL_CORE_PAD0_ABEMCBSP2_FSX_PAD1_ABEMCBSP2_CLKX[31:16]	0x198	abemcbsp2_clkx			abemcasp_ahclkx			gpio4_108	safe_mode_core153
CONTROL_CORE_PAD0_ABEMCPDM_UL_DATA_PAD1_ABEMCPDM_DL_DATA[15:0]	0x19C	abemcpdm_ul_data	abemcbsp3_dr		abemcasp_axr3			gpio4_109	safe_mode_core154
CONTROL_CORE_PAD0_ABEMCPDM_UL_DATA_PAD1_ABEMCPDM_DL_DATA[31:16]	0x19C	abemcpdm_dl_data	abemcbsp3_dx		abemcasp_axr2			gpio4_110	safe_mode_core155
CONTROL_CORE_PAD0_ABEMCPDM_FRAME_PAD1_ABEMCPDM_LB_CLK[15:0]	0x1A0	abemcpdm_frame	abemcbsp3_clkx		abemcasp_axr1			gpio4_111	safe_mode_core156
CONTROL_CORE_PAD0_ABEMCPDM_FRAME_PAD1_ABEMCPDM_LB_CLK[31:16]	0x1A0	abemcpdm_lb_clk	abemcbsp3_fsx					gpio4_112	safe_mode_core157

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_WLSDIO_CLK_PAD1_WLSDIO_CMD[15:0]	0x1A4	wlsdio_clk	mcspi4_clk					gpio5_128(1)	safe_mode_core158
CONTROL_CORE_PAD0_WLSDIO_CLK_PAD1_WLSDIO_CMD[31:16]	0x1A4	wlsdio_cmd						gpio5_129	safe_mode_core159
CONTROL_CORE_PAD0_WLSDIO_DATA0_PAD1_WLSDIO_DATA1[15:0]	0x1A8	wlsdio_data0	mcspi4_simo					gpio5_130	safe_mode_core160
CONTROL_CORE_PAD0_WLSDIO_DATA0_PAD1_WLSDIO_DATA1[31:16]	0x1A8	wlsdio_data1	mcspi4_somi					gpio5_131	safe_mode_core161
CONTROL_CORE_PAD0_WLSDIO_DATA2_PAD1_WLSDIO_DATA3[15:0]	0x1AC	wlsdio_data2	mcspi4_cs0					gpio5_132	safe_mode_core162
CONTROL_CORE_PAD0_WLSDIO_DATA2_PAD1_WLSDIO_DATA3[31:16]	0x1AC	wlsdio_data3						gpio5_133	safe_mode_core163
CONTROL_CORE_PAD0_UART5_RX_PAD1_UART5_TX[15:0]	0x1B0	uart5_rx				sdio4_data1	hw_dbg28	gpio5_134	safe_mode_core164
CONTROL_CORE_PAD0_UART5_RX_PAD1_UART5_TX[31:16]	0x1B0	uart5_tx				sdio4_data2	hw_dbg29	gpio5_135	safe_mode_core165
CONTROL_CORE_PAD0_UART5_CTS_PAD1_UART5_RTS[15:0]	0x1B4	uart5_cts				sdio4_data0	hw_dbg30	gpio5_136	safe_mode_core166
CONTROL_CORE_PAD0_UART5_CTS_PAD1_UART5_RTS[31:16]	0x1B4	uart5_rts				sdio4_data3	hw_dbg31	gpio5_137	safe_mode_core167
CONTROL_CORE_PAD0_I2C2_SCL_PAD1_I2C2_SDA[15:0]	0x1B8	i2c2_scl						gpio5_138	safe_mode_core168
CONTROL_CORE_PAD0_I2C2_SCL_PAD1_I2C2_SDA[31:16]	0x1B8	i2c2_sda						gpio5_139	safe_mode_core169
CONTROL_CORE_PAD0_MCSPI1_CLK_PAD1_MCSPI1_SOMI[15:0]	0x1BC	mcspi1_clk					usbd0_ulpiphy_clk	gpio5_140	safe_mode_core170
CONTROL_CORE_PAD0_MCSPI1_CLK_PAD1_MCSPI1_SOMI[31:16]	0x1BC	mcspi1_somi					usbd0_ulpiphy_nxt	gpio5_141	safe_mode_core171

(1) (1) The wlsdio_clk pad does not have wake – up functionality when configured as gpio5_128.

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_MCSPI1_SIMO_PAD1_MCSPI1_CS0[15:0]	0x1C0	mcspi1_simo					usbd0_ulpiphy_dir	gpio5_142	safe_mode_core172
CONTROL_CORE_PAD0_MCSPI1_SIMO_PAD1_MCSPI1_CS0[31:16]	0x1C0	mcspi1_cs0					usbd0_ulpiphy_data0	gpio5_143	safe_mode_core173
CONTROL_CORE_PAD0_MCSPI1_CS1_PAD1_I2C5_SCL[15:0]	0x1C4	mcspi1_cs1					usbd0_ulpiphy_data1	gpio5_144	safe_mode_core174
CONTROL_CORE_PAD0_MCSPI1_CS1_PAD1_I2C5_SCL[31:16]	0x1C4	i2c5_scl		uart4_rx				gpio5_147	safe_mode_core175
CONTROL_CORE_PAD0_I2C5_SDA_PAD1_GPIO5_145[15:0]	0x1C8	i2c5_sda		uart4_tx				gpio5_148	safe_mode_core176
CONTROL_CORE_PAD0_I2C5_SDA_PAD1_GPIO5_145[31:16]	0x1C8	gpio5_145	mcspi1_cs2	uart4_cts	sdio5_clk		usbd0_ulpiphy_data2	gpio5_145	safe_mode_core177
CONTROL_CORE_PAD0_GPIO5_146_PAD1_UART6_TX[15:0]	0x1CC	gpio5_146	mcspi1_cs3	uart4_rts	sdio5_cmd		usbd0_ulpiphy_data3	gpio5_146	safe_mode_core178
CONTROL_CORE_PAD0_GPIO5_146_PAD1_UART6_TX[31:16]	0x1CC	uart6_tx			sdio5_data3	usbb2_mm_rxdp		gpio5_149	safe_mode_core179
CONTROL_CORE_PAD0_UART6_RX_PAD1_UART6_CTS[15:0]	0x1D0	uart6_rx			sdio5_data2	usbb2_mm_rxdm		gpio5_150	safe_mode_core180
CONTROL_CORE_PAD0_UART6_RX_PAD1_UART6_CTS[31:16]	0x1D0	uart6_cts	sys_ndmareq1		sdio5_data1	usbb2_mm_rxrcv		gpio5_151	safe_mode_core181
CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[15:0]	0x1D4	uart6_rts	sys_ndmareq0		sdio5_data0	usbb2_mm_txse0	usbd0_ulpiphy_stp	gpio5_152	safe_mode_core182
CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[31:16]	0x1D4	uart3_cts_rctx	sata_actled		sdio5_data7	usbb2_mm_txen	usbd0_ulpiphy_data4	gpio5_153	safe_mode_core183
CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[15:0]	0x1D8	uart3_rts_irsd	hdq_sio		sdio5_data6	usbb2_mm_txdat	usbd0_ulpiphy_data5	gpio5_154	safe_mode_core184
CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[31:16]	0x1D8	uart3_tx_irtx			sdio5_data5	sdio4_clk	usbd0_ulpiphy_data6	gpio5_155	safe_mode_core185

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Table 18-9. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[15:0]	0x1DC	uart3_rx_irrx			sdio5_data4	sdio4_cmd	usbd0_ulpiphy_data7	gpio5_156	safe_mode_core186
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[31:16]	0x1DC	usbb3_hsic_strobe						gpio5_158	safe_mode_core187
CONTROL_CORE_PAD0_USBB3_HSIC_DATA_PAD1_SDCARD_CLK[15:0]	0x1E0	usbb3_hsic_data						gpio5_159	safe_mode_core188
CONTROL_CORE_PAD0_USBB3_HSIC_DATA_PAD1_SDCARD_CLK[31:16]	0x1E0	sdcard_clk			jtag_rtck		n_clk		safe_mode_core189
CONTROL_CORE_PAD0_SDCARD_CMD_PAD1_SDCARD_DATA2[15:0]	0x1E4	sdcard_cmd			jtag_tdo	uart6_rx		n_d2	safe_mode_core190
CONTROL_CORE_PAD0_SDCARD_CMD_PAD1_SDCARD_DATA2[31:16]	0x1E4	sdcard_data2			jtag_tmsc		n_d2		safe_mode_core193
CONTROL_CORE_PAD0_SDCARD_DATA3_PAD1_SDCARD_DATA0[15:0]	0x1E8	sdcard_data3			jtag_tck		n_d3		safe_mode_core194
CONTROL_CORE_PAD0_SDCARD_DATA3_PAD1_SDCARD_DATA0[31:16]	0x1E8	sdcard_data0			jtag_tdi		n_d0		safe_mode_core191
CONTROL_CORE_PAD0_SDCARD_DATA1_PAD1_USBD0_HS_DP[15:0]	0x1EC	sdcard_data1			jtag_ntrst		n_d1		safe_mode_core192
CONTROL_CORE_PAD0_SDCARD_DATA1_PAD1_USBD0_HS_DP[31:16]	0x1EC	usbd0_hs_dp				uart3_rx_irrx			safe_mode_core195
CONTROL_CORE_PAD0_USBD0_HS_DM_PAD1_I2C1_PMIC_SCL[15:0]	0x1F0	usbd0_hs_dm				uart3_tx_irtx			safe_mode_core196
CONTROL_CORE_PAD0_USBD0_HS_DM_PAD1_I2C1_PMIC_SCL[31:16]	0x1F0	i2c1_pmic_scl							
CONTROL_CORE_PAD0_I2C1_PMIC_SDA_PAD1_USBD0_SS_RX[15:0]	0x1F4	i2c1_pmic_sda							
CONTROL_CORE_PAD0_I2C1_PMIC_SDA_PAD1_USBD0_SS_RX[31:16]	0x1F4	usbd0_ss_rx							

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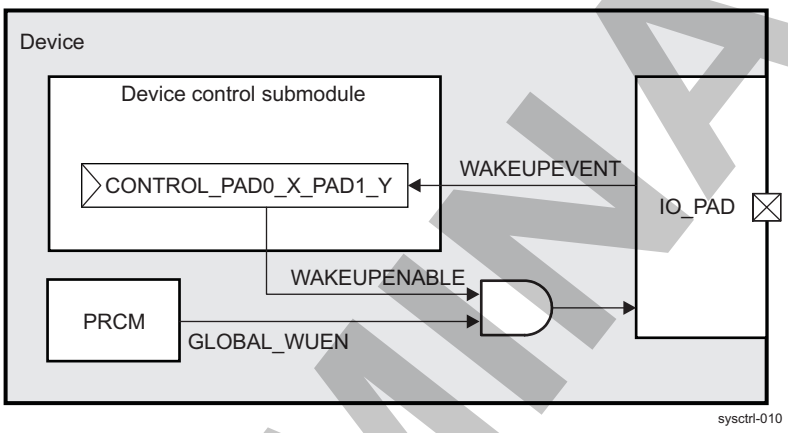
18.4.8.4 Wake-Up Event Detection

In low power mode, wake-up event detection can also be enabled on an input pad. The pad wake-up event is latched in the CONTROL_CORE_PAD0_X_PAD1_Y[31,15] and CONTROL_WKUP_PAD0_X_PAD1_Y[31,15] WAKEUPEVENT bits.

The wake-up scheme is enabled by setting the PRM_IO_PMCTRL[16] GLOBAL_WUEN bit from the PRCM module. The status of the wake-up scheme is transmitted by the WKUP_ENABLE signal. The capability of each I/O pad to detect wake-up events in the device is individually enabled or disabled by writing the CONTROL_CORE_PAD0_X_PAD1_Y[30,14] and CONTROL_WKUP_PAD0_X_PAD1_Y[30,14] WAKEUPENABLE bits.

Figure 18-7 is an overview of wake-up event detection in the device.

Figure 18-7. Wake-Up Event Detection Overview



NOTE: When wake-up detection is enabled for a pad, the pad must be configured as input to avoid contention between the device output buffer and an external driver.

NOTE: Regardless of whether the INPUTENABLE bit is set high or low during active mode, to enable wake-up detection for a pad, user software must set the WAKEUPENABLE bit to 0x1. It is recommended to apply pullup and pulldown resistors at the pad to avoid spurious wake-up detection.

The CONTROL_PADCONF_WAKEUPEVENT_0 through CONTROL_PADCONF_WAKEUPEVENT_6 registers are dedicated 32-bit registers for a separate capture of the WAKEUPEVENT from different pads. Duplication of the CONTROL_CORE_PAD0_X_PAD1_Y[31,15] and CONTROL_WKUP_PAD0_X_PAD1_Y[31,15] wake-up event bits inside these additional registers helps to reduce the software latency when identifying which pad has triggered a wake-up event.

For unconnected device pads, safe_mode pad configuration is recommended if available. Table 18-10 summarizes recommendations for the configuration of unconnected pads (in terms of mux mode, input, and output buffer states) for all cases, including those where safe_mode configuration is not available.

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Table 18-10. Recommended Configuration For Unconnected Device Pads

Pad MuxMode Set Features	Power-on reset default configuration		Recommended Unconnected Device Pad Configuration				
Safe Mode Available?	Multiplexed Signal Direction at Pad	Pad State[1]	Multiplexed Signal Direction at Pad	Pad State	Input Buffer Disabled? [2]	Output Buffer Disabled? [3]	MUX Function Selected [4]
Yes	Input	PU	Safe mode	PU	Yes	N/A	Safe mode
Yes	Input	PD	Safe mode	PD	Yes	N/A	Safe mode
Yes	Output	1	Safe mode	PD	Yes	N/A	Safe mode
Yes	Output	0	Safe mode	PD	Yes	N/A	Safe mode
Yes	–	Hi-Z	Safe mode	PD	Yes	N/A	Safe mode
No	Input	PU	Input	PU	Yes	N/A	N/A (default)
No	Input	PD	Input	PD	Yes	N/A	N/A (default)
No	Output	1	Output	1	Yes	N/A	N/A (default)
No	Output	0	Output	0	Yes	N/A	N/A (default)
No	–	Hi-Z	Input	PD	Yes	N/A	N/A (default)

(1) PU = Pullup; PD = Pulldown; Hi-Z = High impedance

(2) Yes: If a certain device pad is left unconnected, its associated pad configuration register INPUTENABLE bit must be explicitly disabled in software (set to 0b0), regardless of pad MUXMODE bit field value.

(3) N/A: There is no software control over the pad associated output buffer in the control module.

(4) SAFE MODE: If a certain pad has a defined safe_mode and is left unconnected in an application, it is recommended to keep its padconfiguration MUXMODE value at 0x7 (that is, safe_mode).
N/A (default): The pad does not have a defined safe_mode. Keeping the default value is recommended.

18.4.9 Extended-Drain I/O and PBIAS Cell

The device primarily supports 1.8-V I/O voltage on its interfaces, with the exception of the MMC/SD/SDIO1 interface, which supports 1.8-V and 3.0-V voltages. The need for embedded extended-drain I/Os on the MMC/SD/SDIO1 interface imposes the use of embedded PBIAS cell SDCARD_PBIAS to provide a 1.8-V or 3.0-V reference.

The SDCARD_PBIAS cell and its associated extended-drain I/O cell are software-controlled by bits in the CONTROL_PBIAS and CONTROL_HYST_1 registers of the device core control module.

Figure 18-8 shows the functional block diagram with the connections between the PBIAS cell and the extended-drain I/O cell.

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Figure 18-8. Functional Block Diagram

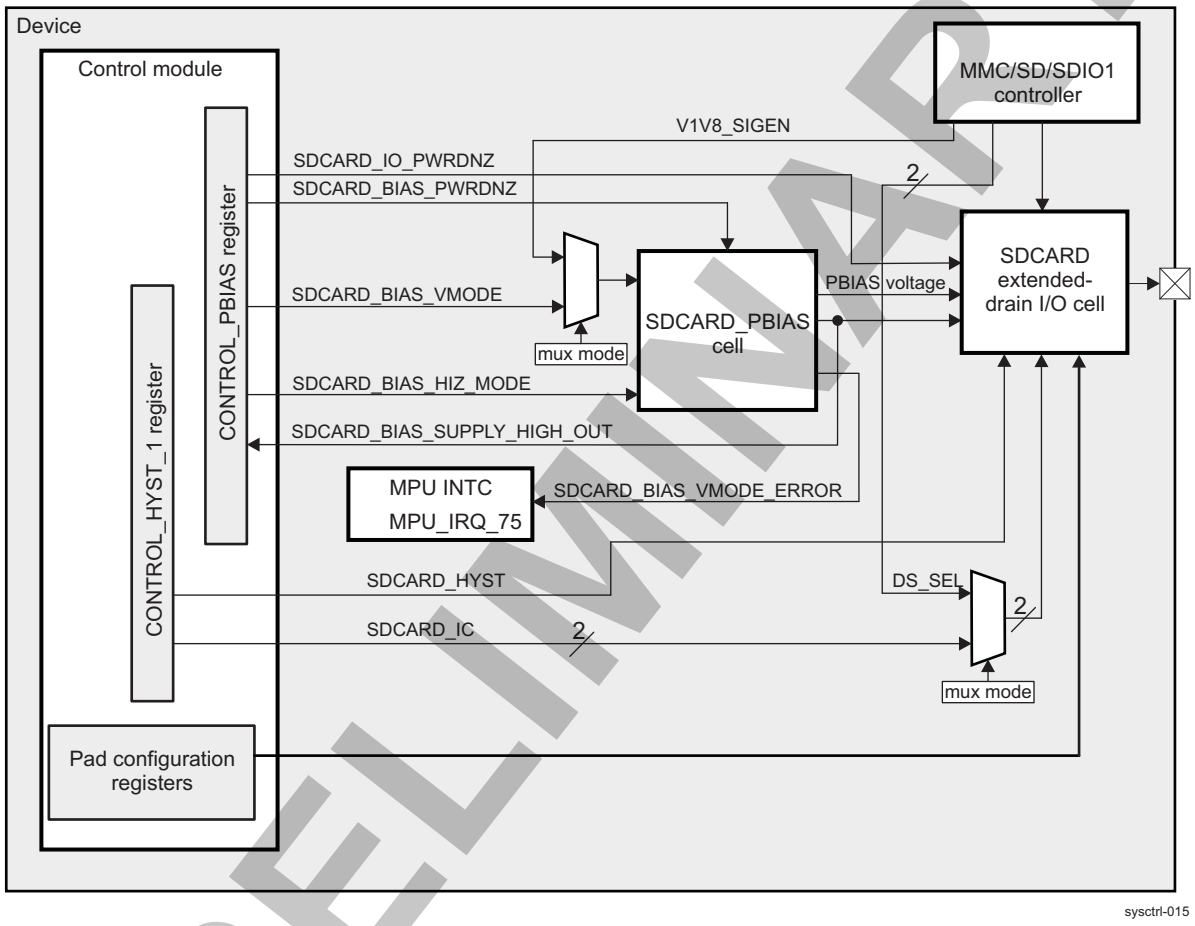

Table 18-11 describes PBIAS cell and extended-drain I/O cell control signals.

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Table 18-11. PBIAS Cell and Extended-Drain I/O Pin CONTROL_PBIAS Bit Control

Control Signals for PBIAS Cell and Extended-Drain I/O Cell	Description
SDCARD_BIAS_PWRDNZ	Protects the SDCARD_PBIAS cell when the SDCARD_VDDS supply voltage is not stable. Software must keep this signal to 0b0 whenever this voltage ramps up/down or changes. When this bit is set to 0, the PBIAS output voltage is equal to the SDCARD_VDDS voltage and the PBIAS supply detector is disabled.
SDCARD_IO_PWRDNZ	Protects the SDCARD extended-drain I/O cell when the SDCARD_VDDS voltage is not stable. Software must keep this signal to 0b0 whenever the SDCARD_VDDS supply voltage ramps up/down or changes. When this bit is set to 0, the pad is floating.
SDCARD_BIAS_VMODE	Controls the SDCARD_VDDS voltage level. The default state of this bit is HIGH, indicating that the voltage level SDCARD_VDDS is 3.0 V.
SDCARD_BIAS_HIZ_MODE	When SDCARD_BIAS_HIZ_MODE is set to 1, the PBIAS output is in high impedance. SDCARD_BIAS_ERROR is automatically set to 1 when SDCARD_BIAS_HIZ_MODE is set to 1. When SDCARD_BIAS_HIZ_MODE is set to 0, SDCARD_PBIAS cell is in normal operation mode.
SDCARD_BIAS_SUPPLY_HI_OUT	Output from the internal SDCARD_PBIAS voltage supply detector, which indicates whether the SDCARD_VDDS supply is 3.0 V or 1.8 V
SDCARD_BIAS_VMODE_ERROR	Indicates whether the software-programmed voltage level of the SDCARD_PBIAS cell matches the SDCARD_BIAS_SUPPLY_HI_OUT output signal during normal operation
SDCARD_HYST	Hysteresis enabling/disabling for the extended-drain I/O cell input buffer.
SDCARD_IC	Impedance control for the extended-drain I/O cell output buffer.
V1V8_SIGEN	Controls the SDCARD_VDDS voltage level. The default state of this bit is LOW, indicating that the voltage level SDCARD_VDDS is 3.0 V.
DS_SEL	Drive strength (impedance) control for extended-drain I/O cell output buffer

NOTE: When MUXMODE is set to 0 (sdcard_i signals are selected), then the CONTROL_PBIAS[21] SDCARD_BIAS_VMODE and CONTROL_HYST_1[30:29] SDCARD_IC bits do not apply. In this case the voltage level and drive strength are controlled through the MMC1.MMCHS_AC12[19] V1V8_SIGEN and MMC1.MMCHS_AC12[21:20] DS_SEL bits, respectively.

Table 18-12 lists the power supplies for PBIAS and the extended-drain I/O cells.

Table 18-12. Power Supplies

Power Supply Name	Description
VDD2	Core voltage supply
SDCARD_VDDS	SDCARD I/O cell supply voltage nominal 1.8 V/3.0 V
VDDS	1.8-V supply for the input buffer

18.4.9.1 PBIAS Cell

The SDCARD_PBIAS cell provides a bias for the MMC/SD/SDIO1 extended-drain I/O cell used with high voltage for the MMC/SD/SDIO1 interface. This PBIAS cell provides a voltage reference (PBIAS voltage) for biasing extended drain in the MMC/SD/SDIO1 cell. In addition to generate the bias voltage, the cell can detect the supply voltage (SDCARD_VDDS) value (1.8 V or 3.0 V) and update, with its status, the CONTROL_PBIAS[24] SDCARD_BIAS_SUPPLY_HI_OUT bit. However, this is possible when the voltage reaches its steady state (the internal PBIAS voltage detector is enabled only when the SDCARD_BIAS_PWRDNZ signal is set to 0b1).

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CAUTION

A PBIAS cell lets the peripheral associated with its corresponding extended-drain I/O cells support 1.8-V and 3.0-V voltages. A PBIAS cell is not part of a peripheral, but part of the device I/Os to which this peripheral is internally connected. These device I/Os are not exclusive to one peripheral; through I/O multiplexing they can be connected to other internal signals. It is necessary to configure the PBIAS to enable the I/Os, regardless of how I/O multiplexing is configured for these device I/Os.

18.4.9.2 Extended-Drain I/O

The following MMC1 interface signals (selected when MuxMode = 0) use the device I/Os associated with the SDCARD extended-drain I/O cell:

- sdcard_clk
- sdcard_cmd
- sdcard_datai (where i = 0 to 3)

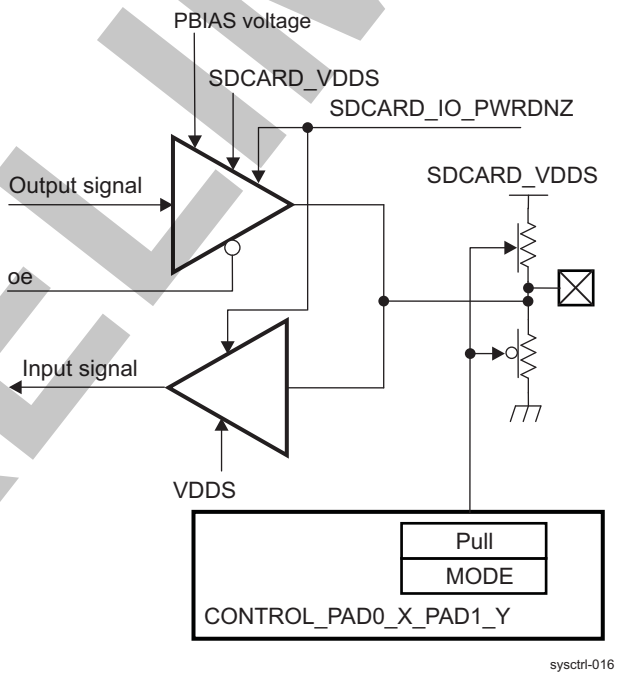
The SDCARD I/O cell is powered externally through the vdds_sdcard pad.

NOTE: The device pads associated with SDCARD I/O cells are also shared with other signals. jtag_tdo, jtag_tdi, uart6_rx, and so forth. are available when MuxMode is different than 0x0. If signals other than sdcard_x are selected, the SDCARD I/O cell must also be configured.

For more information about signal multiplexing, see Table 18-9.

Figure 18-9 shows the extended-drain I/O cells.

Figure 18-9. Extended-Drain I/O



The extended-drain I/O cells have the following I/O signals:

- The output signal, input signal, and oe, which comes from the selected I/O module with the correctly configured MUXMODE field within the corresponding CONTROL_CORE_PAD0_X_PAD1_Y or CONTROL_WKUP_PAD0_X_PAD1_Y register

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NOTE: Extended-drain I/Os are muxed I/Os with mode and pullup and pulldown configurations programmable in the control module.

- The PBIAS voltage is a voltage reference for biasing the extended-drain in the SDCARD cell.
- The SDCARD_IO_PWRDNZ signal is used to protect the extended-drain I/O cell when the SDCARD_VDDS voltage is not stable.

NOTE: Software must keep the SDCARD_IO_PWRDNZ signal set to 0b0 whenever the SDCARD_VDDS signal ramps up/down or changes. When SDCARD_IO_PWRDNZ is set to 0, the pad is floating (the pad may not reflect the state of the output signal, and the input signal may not reflect the state of the pad).

- CONTROL_PBIAS[24] SDCARD_BIAS_SUPPLY_HI_OUT is a status bit for the SDCARD_VDDS value and is used to inform the SDCARD I/O cell about the value of the SDCARD_VDDS signal.

For more information about the software configurations of the extended drain I/Os and PBIAS cells, see Section 18.5.1.2.1, *Extended-Drain I/Os and PBIAS Cells Programming Guide.*

NOTE: The device can be supplied by an external power IC. TI provides such a global solution to its customers with the TWL60xx power IC.

If the device is associated with the TWL60xx power IC, before using an extended-drain I/O interface, software must program the TWL60xx to enable SDCARD_VDDS (for the MMC/SD/SDIO1 or muxed I/O modules) and the LDO to provide 1.8-V/3.0-V voltage. This is done by software through the inter-integrated circuit (I^2C™) interface that links the device and the TWL60xx IC.

CAUTION

The power supply voltage, generated from the companion power IC and applied on the vdds_sdcard device pad, must be programmed according to the recommendations for the currently selected I/O module power supply range.

If the application does not want the I/O interface to run at 3.0 V, for 1.8-V activity software must either assert the SDCARD_BIAS_VMODE signal to low or the V1V8_SIGEN signal to high depending on the selected muxmode: in this case, the PBIAS is connected to ground.

Table 18-13 lists the control signals with the corresponding control bits from the CONTROL_PBIAS, CONTROL_HYST_1, and MMC1.MMCHS_AC12 registers to configure the PBIAS and the extended-drain I/O cells. Software can control these signals.

Table 18-13. PBIAS and Extended-Drain I/O Cells Control Signals

Control Signals for PBIAS Cell and Extended-Drain I/O Cell	Bits Used for PBIAS Cell and I/O Cell Configurations for Different I/O Modules	Reset Value
SDCARD_BIAS_PWRDNZ	CONTROL_PBIAS[27] SDCARD_BIAS_PWRDNZ	0
SDCARD_IO_PWRDNZ	CONTROL_PBIAS[26] SDCARD_IO_PWRDNZ	0
SDCARD_BIAS_VMODE	CONTROL_PBIAS[21] SDCARD_BIAS_VMODE	1
SDCARD_BIAS_HIZ_MODE	CONTROL_PBIAS[25] SDCARD_BIAS_HIZ_MODE	0
SDCARD_BIAS_SUPPLY_HI_OUT	CONTROL_PBIAS[24] SDCARD_BIAS_SUPPLY_HI_OUT	0
SDCARD_BIAS_VMODE_ERROR	CONTROL_PBIAS[23] SDCARD_BIAS_VMODE_ERROR	0
SDCARD_HYST	CONTROL_HYST_1[31] SDCARD_HYST	1
SDCARD_IC	CONTROL_HYST_1[30:29] SDCARD_IC	0x0
DS_SEL	MMC1. MMCHS_AC12[21:20] DS_SEL	0x0
V1V8_SIGEN	MMC1. MMCHS_AC12[19] V1V8_SIGEN	0

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The PBIAS cell supports two ranges of SDCARD_VDDS: 1.8 V, typical for low-voltage applications, and 3.0 V, typical for high-voltage applications. For each supply voltage range, the PBIAS cell generates suitable bias voltage (PBIAS) for the extended-drain I/O cell.

CAUTION

The PBIAS cell must be programmed according to peripheral power supply voltage. See Table 18-14.

Table 18-14. Voltage Configuration(1)

PBIASVMODE Configuration	SDCARD_VDDS Voltage	Type of Operation
1.8 V	1.8 V	Normal 1.8-V operation
1.8 V	3.0 V	Damaging configuration(2)
3.0 V	1.8 V	Degraded functionality(2)
3.0 V	3.0 V	Normal 3.0-V operation

(1) For damaging configuration, hardware system protection is provided to prevent deterioration of the associated extended-drain I/Os.

(2) These modes must not be used.

Once the SDCARD_VDDS supply is stable, software can release SDCARD_BIAS_PWRNDZ and SDCARD_IO_PWRDNZ bits setting them high. Setting SDCARD_BIAS_PWRNDZ to 0b1 powers-up the PBIAS cell and it starts to generate the bias voltage. During the completion process the corresponding I/Os cannot be used to transmit data. If the voltage level is set correctly (compared with supply detector output and found to be the same), then bias voltage is generated based on this value.

NOTE: In the case of a damaging configuration, hardware system protection prevents deterioration of the associated extended-drain I/Os.

CAUTION

The following requirements are critical for an extended-drain I/O cell:

- The SDCARD_BIAS_VMODE or V1V8_SIGEN bit must be defined before the SDCARD_IO_PWRNDZ bit is made high (cell is brought out of power-down mode).
- The default state of SDCARD_BIAS_VMODE bit is high (indicates 3.0-V operation).
- The default state of the MMC1.MMCHS_AC12[19] V1V8_SIGEN bit is low (indicates 3.0-V operation).
- The SDCARD_IO_PWRNDZ bit must be kept low whenever the SDCARD_VDDS supply ramps up/down or changes. This can be damaging.

18.4.9.3 PBIAS Error Generation

If the programmed PBIAS voltage and supply detector output are unequal, it takes 4 µs for the comparator to process the inputs and generate the SDCARD_BIAS_VMODE_ERROR flag.

Table 18-15 summarizes the generation of the PBIAS error signal (SDCARD_BIAS_VMODE_ERROR of the SDCARD_PBIAS cell), which depends on the various CONTROL_PBIAS bit combinations. The shaded row in the table indicates a condition that could cause a reliability issue if not detected. To prevent this reliability issue, the PBIAS voltage is tied to SDCARD_VDDS when the PBIAS error signal is high. This condition disables the I/Os.

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NOTE: Although asserting SDCARD_BIAS_VMODE_ERROR to 1 ensures that PBIAS voltage is equal to SDCARD_VDDS, this does not completely protect the I/O cells. It is recommended that all the I/Os are powered down, thus setting the CONTROL_PBIAS[26] SDCARD_IO_PWRDNZ bit to 0b0 by software as soon as CONTROL_PBIAS[23] SDCARD_BIAS_VMODE_ERROR = 0b1.

Table 18-15. PBIAS Error Signal Truth Table

Programmed voltage level		PWRDNZ Bits	SDCARD_BIAS_HIZ_MODE	SDCARD_BIAS_SUPPLY_HI_OUT	SDCARD_BIAS_VMODE_ERROR
SDCARD_BIAS_VMODE (MUXMODE ≠ 0)	V1V8_SIGEN (MUXMODE = 0)				
0	1	0	X	0	0
0	1	1	0	0	0
0	1	1	0	1	1
X	X	1	1	X	1
1	0	0	X	0	0
1	0	1	0	0	1
1	0	1	0	1	0

NOTE: SDCARD_BIAS_VMODE_ERROR = 0b1: The programmed voltage level is not the same as SDCARD_BIAS_SUPPLY_HI_OUT, or Hi-Z mode is selected.

SDCARD_BIAS_VMODE_ERROR = 0b0: The programmed voltage level is the same as SDCARD_BIAS_SUPPLY_HI_OUT, or it is not considered (SDCARD_PWRDNZ = 0b0).

The SDCARD_BIAS_VMODE_ERROR signal output is mapped to the MPU subsystem INTC. The interrupt line MPU_IRQ_75 is activated when an error occurs. For more information about the MPU INTC registers and their description, see the *ARM Cortex-A15 MPCore Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

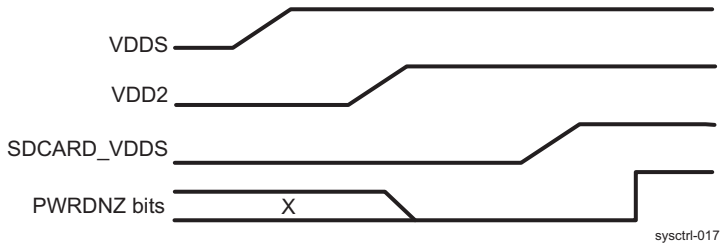
The CONTROL_PBIAS[23] SDCARD_BIAS_VMODE_ERROR bit also indicates whether this kind of error occurs.

18.4.9.4 Critical Timing Requirements

It is critical that SDCARD_BIAS_PWRDNZ and SDCARD_IO_PWRDNZ bits are deasserted (changed from 0 to 1) only after SDCARD_VDDS power supply voltage is stable in the device. The cells support only the case where the 1.8-V input buffer supply voltage VDDS ramps up before VDD2 (core voltage). This power-up sequence is automatically provided upon POR by hardware in the device. Take care to ensure that the externally provided SDCARD_VDDS voltage (1.8 V/ 3 V) is powered up only after VDD2 and VDDS reach their steady state.

Figure 18-10 shows the only possible power-up sequence, as well as the expected behavior of PWRNDZ mode-related bit with regard to supplying voltage ramp up.

Figure 18-10. VDDS Ramps Up Before VDD2



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18.4.10 Bandgap Voltage and Temperature Sensor

The device supplies a voltage reference and a temperature sensor feature that are gathered in the bandgap voltage and temperature sensor (VBGAPTS) module. The bandgap provides current and voltage reference for its internal circuits and other analog IP blocks. The analog-to-digital converter (ADC) produces an output value that is proportional to the silicon temperature. There are three bandgaps: one for MPU, one for GPU and one for device die center.

The main features of the VBGAPTS modules are:

- A constant voltage reference output
- Five constant current reference outputs
- Nominal analog supply
- Small ADC with 10-bit digital output

Three small finite state-machines (FSMs) (bandgap FSMs) are instantiated inside the general core control module to help the three VBGAPTS cells accomplish different measurement modes (see Section 18.4.10.2, *Temperature Sensor*). In addition, three sets of two programmable comparator blocks inside the general core control module post-process the converted data and provide the following outputs:

- Thermal alert programmable comparator outputs
- Thermal shutdown nonprogrammable comparator outputs

Figure 18-11 shows the functional block diagram of the bandgap and the temperature sensor module.

Figure 18-11. Functional Block Diagram

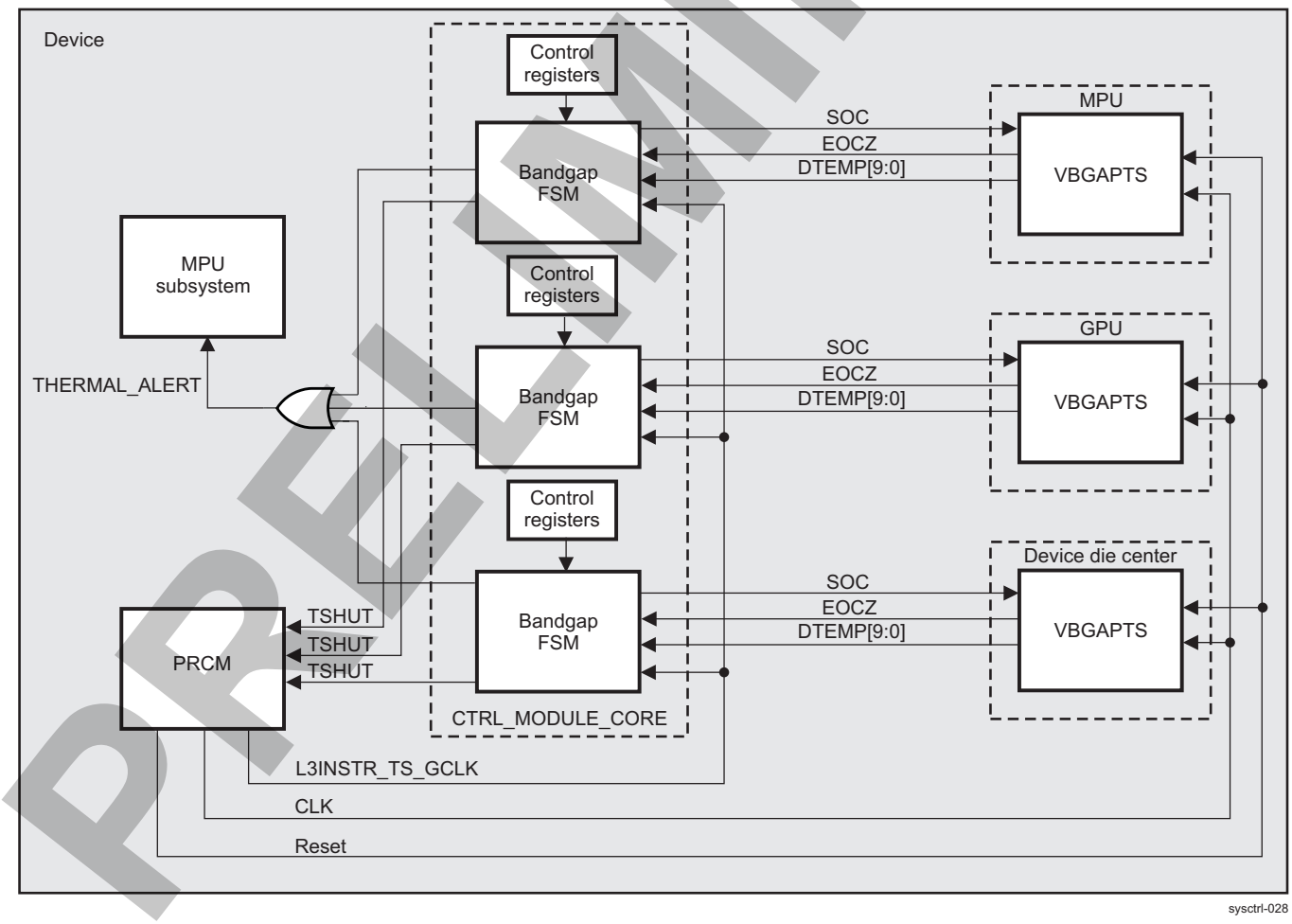

Table 18-16 describes the I/O signals, some of which (SOC, EOCZ, DTEMP[9:0]) build the interface between the VBGAPTS modules and the bandgap state-machines of the general core control module.

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Table 18-16. Bandgap Voltage and Temperature Sensor Signal Description

Pin	I/O[1]	Description
SOC	I	Start of Conversion signal. A transition to high starts a new ADC conversion cycle. This signal is automatically generated by the bandgap FSM.
EOCZ	O	End of Conversion signal. When low, the signal indicates that the value of DTEMP[9:0] is valid.
DTEMP[9:0]	O	Temperature data from the temperature sensor. This value is valid when EOCZ is low.
CLK	I	Functional clock in the range (500 kHz - 5 MHz) from the WKUP power domain used by the temperature sensor during temperature conversion

(1) I = Input; O = Output; I/O = Bidirectional

All the configuration signals of the VBGAPTS temperature conversion logic are available through the CONTROL_TEMP_SENSOR_MPU, CONTROL_TEMP_SENSOR_MM, and CONTROL_TEMP_SENSOR_CORE registers.

NOTE: For more information about all of the configuration registers related to temperature sensor control, see Table 18-63.

The bandgap state-machines of the general core control module are driven by a dedicated clock (L3INSTR_TS_GCLK) that shares a common PRCM clock source with the VBGAPTS CLK. For more information about the thermal management clocks, see Section 3.1.1, *Device Power-Management Architecture Building Blocks*.

Table 18-17 describes the functional outputs of the two post-processing comparator blocks integrated in the general core control module.

Table 18-17. General Core Control Thermal Logic Outputs Description

Functional Output	Description
THERMAL_ALERT	The three thermal alert outputs from each bandgap FSM are ORed and then mapped as an interrupt in the MPU subsystem. Software uses this interrupt to implement a thermal management policy of the device.
TSHUT	Each of the three general core control module thermal shutdown comparator outputs is mapped as a source of PRCM warm reset signals. These overheat protection signals are high during normal operation and go low during a thermal shutdown event.

The configuration bits of the thermal post-processing logic are in several registers of the general core control module. For more information, see Section 18.4.10.2.2, *Thermal Data Post-Processing Logic*.

18.4.10.1 Bandgap Voltage Reference

The bandgap voltage reference feature provides several constant voltage and current references for its internal circuits and for other analog modules.

The voltage reference signal is a 0.5-V output. This output is used internally by the module and is exported for external modules or tests.

The current reference signals consist of five lines, each of which generates a 1-µA current with a 1.8-V voltage. These lines can be used to bias other modules.

18.4.10.2 Temperature Sensor

The temperature sensor feature is used to convert the temperature of the device into a decimal value coded on 10 bits. An internal ADC, which is part of the device embedded bandgap cell, is used for conversion.

For more information on the thermal sensor operating parameters–temperature range, accuracy, and so on, see the *Temperature Sensor* section of the device data manual.

For more details on the device operating junction temperature ranges under different conditions, see the *Recommended Operating Conditions* section of the device data manual.

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NOTE: The temperature measured at the three temperature sensor locations is lower than the temperature of the hottest spot on the device die. This difference, defined also as the temperature offset between the on-die hottest spot temperature and the temperature registered by the on-die thermal sensors, depends on a number of factors, such as the current system power dissipation, device cooling conditions, etc. For more information regarding the temperature sensor offset values under different conditions, contact your TI representative.

CAUTION

User software must always take care to program thermal alert thresholds at levels which do not exceed the device hottest spot maximum-allowed temperature minus the device temperature sensor offset estimated at current conditions.

The TSHUT signals are connected internally to PRCM pins. The three bandgap state-machines operate in continuous conversion mode.

18.4.10.2.1 Continuous Conversion Mode

The continuous conversion mode follows this sequence:

After reset, each FSM produces a programmable delay which is also used as a main delay between two temperature measurements. After this delay the three FSMs automatically generate SOC pulses which start a temperature conversion. Software can control the main delay between two measurements through the dedicated bit field CONTROL_BANDGAP_MASK[29:28] COUNTER_DELAY. The conversion is complete when the CONTROL_TEMP_SENSOR_MPU[10] BGAP_EOCZ_MPU, CONTROL_TEMP_SENSOR_MM[10] BGAP_EOCZ_MM, and CONTROL_TEMP_SENSOR_CORE[10] BGAP_EOCZ_CORE status bits are set to 0b0. After this stage the valid temperature is written automatically by each FSM in the CONTROL_TEMP_SENSOR_MPU[9:0] BGAP_DTEMP_MPU, CONTROL_TEMP_SENSOR_MM[9:0] BGAP_DTEMP_MM, and CONTROL_TEMP_SENSOR_CORE[9:0] BGAP_DTEMP_CORE bit fields, and then software is able to read the valid temperature value from each register. After writing the valid temperature values the three FSMs wait one clock cycle and start another conversion cycle.

NOTE: The main delay between two measurements is controlled by the CONTROL_BANDGAP_MASK[29:28] COUNTER_DELAY bit field. After this delay there is an additional 5µs delay before a new temperature conversion starts. This is managed automatically by each FSM.

Figure 18-12 shows the timing sequence for a programmable-delay continuous conversion mode. The continuous temperature measurement is performed as a sequence of single ADC conversions automatically initiated at regular time intervals. As show in Figure 18-12, the duration of a single temperature conversion is 17 bandgap clock cycles regardless of the CLK frequency.

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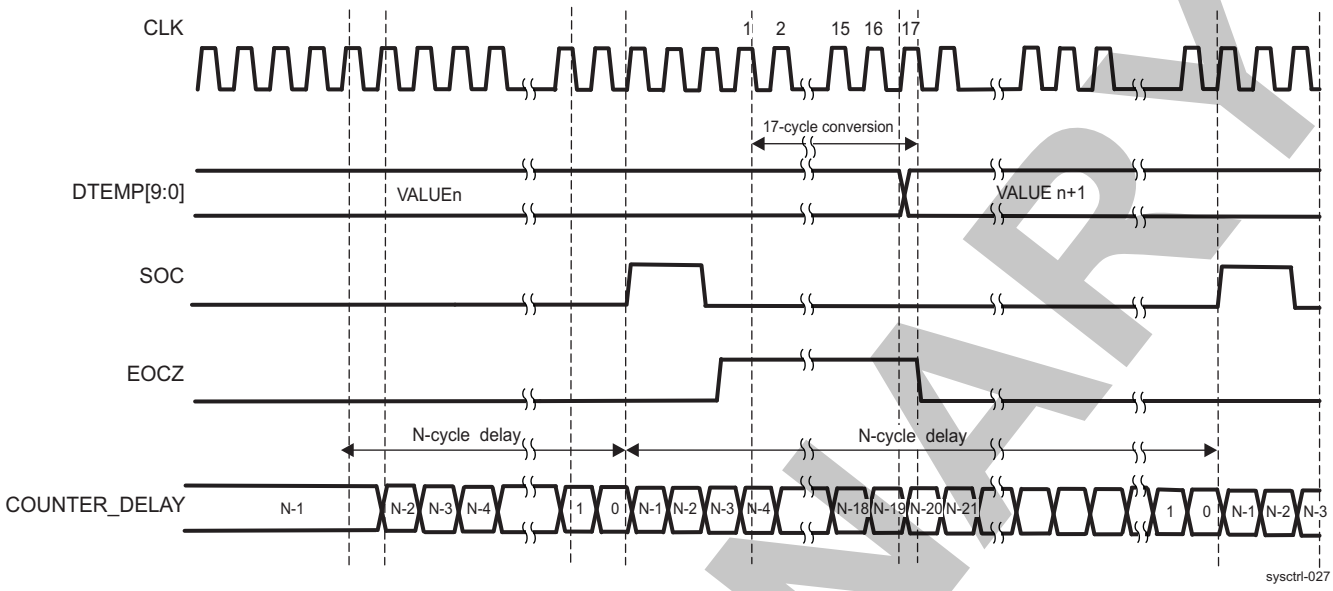
Figure 18-12. Programmable-Delay Continuous Conversion Mode



18.4.10.2.2 Thermal Data Post-Processing Logic

A thermal data post-processing logic with dedicated registers is implemented in the general core control module. The registered ADC value from each of the three temperature sensors is passed in parallel to the inputs of four comparators (two blocks of two comparators). In each block, the temperature data is compared to high- and low-temperature thresholds, to handle the hysteresis effect when temperature decreases. Three sets of two comparator blocks provide different thermal management functions.

Figure 18-13 shows the thermal management schema in the device.

There are three register sets

- CONTROL_TEMP_SENSOR_MPU, CONTROL_BANDGAP_TSHUT_MPU, CONTROL_BANDGAP_THRESHOLD_MPU, CONTROL_BANDGAP_CUMUL_DTEMP_MPU, and CONTROL_DTEMP_MPU_x (where x = 0 to 4) for the MPU thermal sensor
- CONTROL_TEMP_SENSOR_MM, CONTROL_BANDGAP_TSHUT_MM, CONTROL_BANDGAP_THRESHOLD_MM, CONTROL_BANDGAP_CUMUL_DTEMP_MM, and CONTROL_DTEMP_MM_x (where x = 0 to 4) for the GPU thermal sensor
- CONTROL_TEMP_SENSOR_CORE, CONTROL_BANDGAP_TSHUT_CORE, CONTROL_BANDGAP_THRESHOLD_CORE, CONTROL_BANDGAP_CUMUL_DTEMP_CORE, and CONTROL_DTEMP_CORE_x (where x = 0 to 4) for the device die center thermal sensor.

For more information, see Table 18-63 *Temperature Sensor Registers*.

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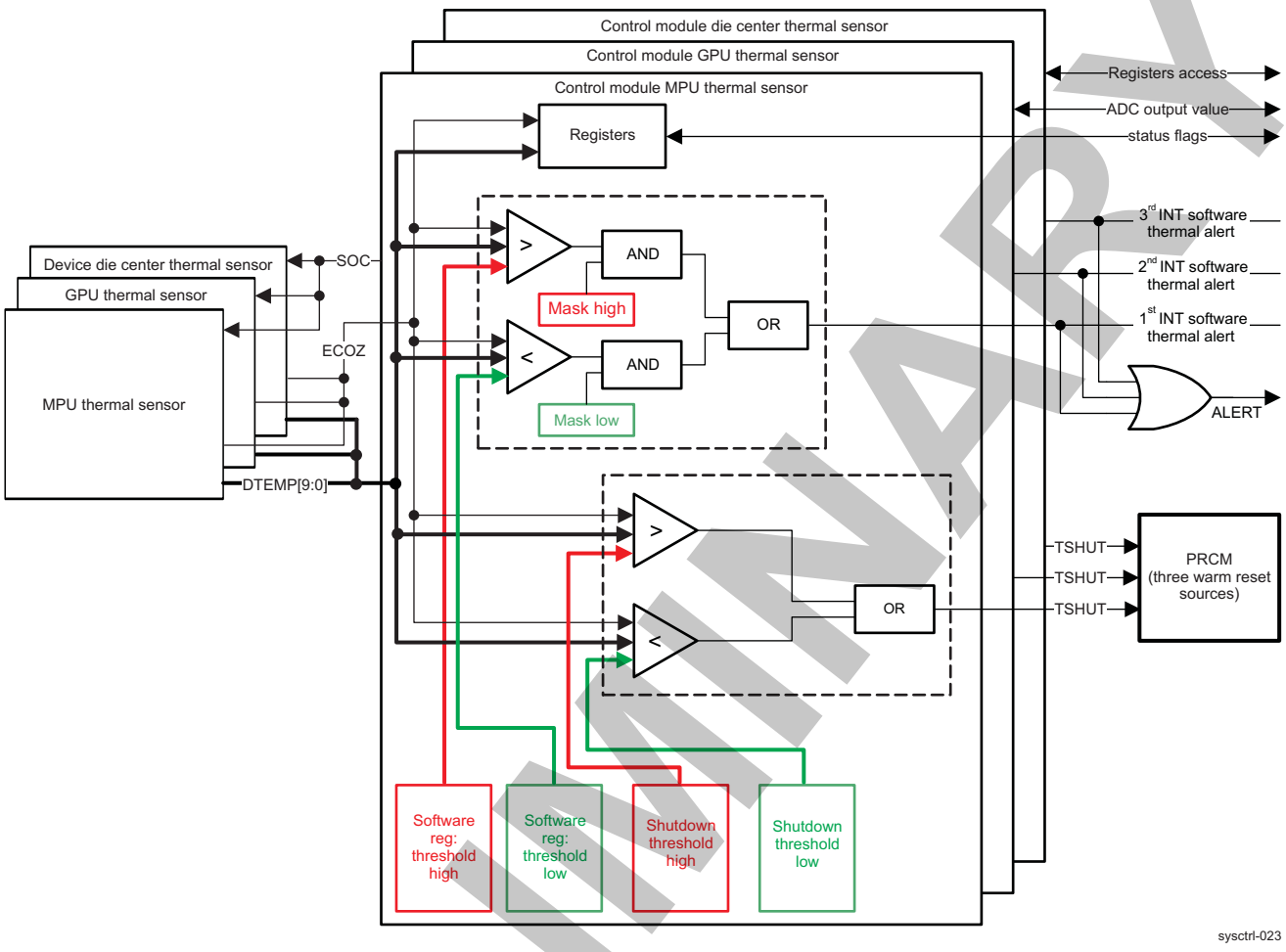
Figure 18-13. Thermal Management Schema



18.4.10.2.3 Thermal Alert Functionality Comparators

There are three sets (for MPU, for GPU, and for the device die center) of two comparator blocks inside the general core control module. The first three comparator blocks are programmable and provide a thermal alert function output. The high-temperature threshold for this function is configurable through the follwoing 10-bit fields:

- CONTROL_BANDGAP_THRESHOLD_MPU[25:16] THOLD_HOT_MPU for the MPU temperature sensor
- CONTROL_BANDGAP_THRESHOLD_MM[25:16] THOLD_HOT_MM for the GPU temperature sensor
- CONTROL_BANDGAP_THRESHOLD_CORE[25:16] THOLD_HOT_CORE for the device die center temperature sensor

The low-temperature threshold for this function is configurable through the following 10-bit fields:

- CONTROL_BANDGAP_THRESHOLD_MPU[9:0] THOLD_COLD_MPU for the MPU temperature sensor
- CONTROL_BANDGAP_THRESHOLD_MM[9:0] THOLD_COLD_MM for the GPU temperature sensor
- CONTROL_BANDGAP_THRESHOLD_CORE[9:0] THOLD_COLD_CORE for the device die center temperature sensor

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Thermal alert logic in the general core control module provides the capability to mask (active low) comparator outputs for hot events through the CONTROL_BANDGAP_MASK[1] MASK_HOT_MPU, CONTROL_BANDGAP_MASK[3] MASK_HOT_MM and CONTROL_BANDGAP_MASK[5] MASK_HOT_CORE bits, and for cold events through the CONTROL_BANDGAP_MASK[0] MASK_COLD_MPU, CONTROL_BANDGAP_MASK[2] MASK_COLD_MM, and CONTROL_BANDGAP_MASK[4] MASK_COLD_CORE bits. The masked HOT and COLD point-monitoring signals from each of the three comparator blocks are ORed in three thermal alert signals (first, second, third INT software thermal alert) (for details, see Figure 18-13). These three signals are then ORed in the THERMAL_ALERT signal, which delivers an interrupt to the MPU subsystem on the MPU_IRQ_126 input (see Section 18.3, *Control Module Integration*). Software can use this interrupt to implement the thermal management policy of the device. For more information about this interrupt, see Section 17.3.2, *Interrupt Requests to INTC_MPU*, in Chapter 17, *Interrupt Controllers*.

The nonmasked outputs of the thermal alert logic comparators are individually registered in the following read-only (RO) bits:

- CONTROL_BANDGAP_STATUS[1] HOT_MPU
- CONTROL_BANDGAP_STATUS[3] HOT_MM
- CONTROL_BANDGAP_STATUS[5] HOT_CORE
- CONTROL_BANDGAP_STATUS[0] COLD_MPU
- CONTROL_BANDGAP_STATUS[2] COLD_MM
- CONTROL_BANDGAP_STATUS[4] COLD_CORE

The THERMAL_ALERT signal is mapped to the CONTROL_BANDGAP_STATUS[31] ALERT RO bit.

Figure 18-14 shows the behavior of the thermal alert logic.

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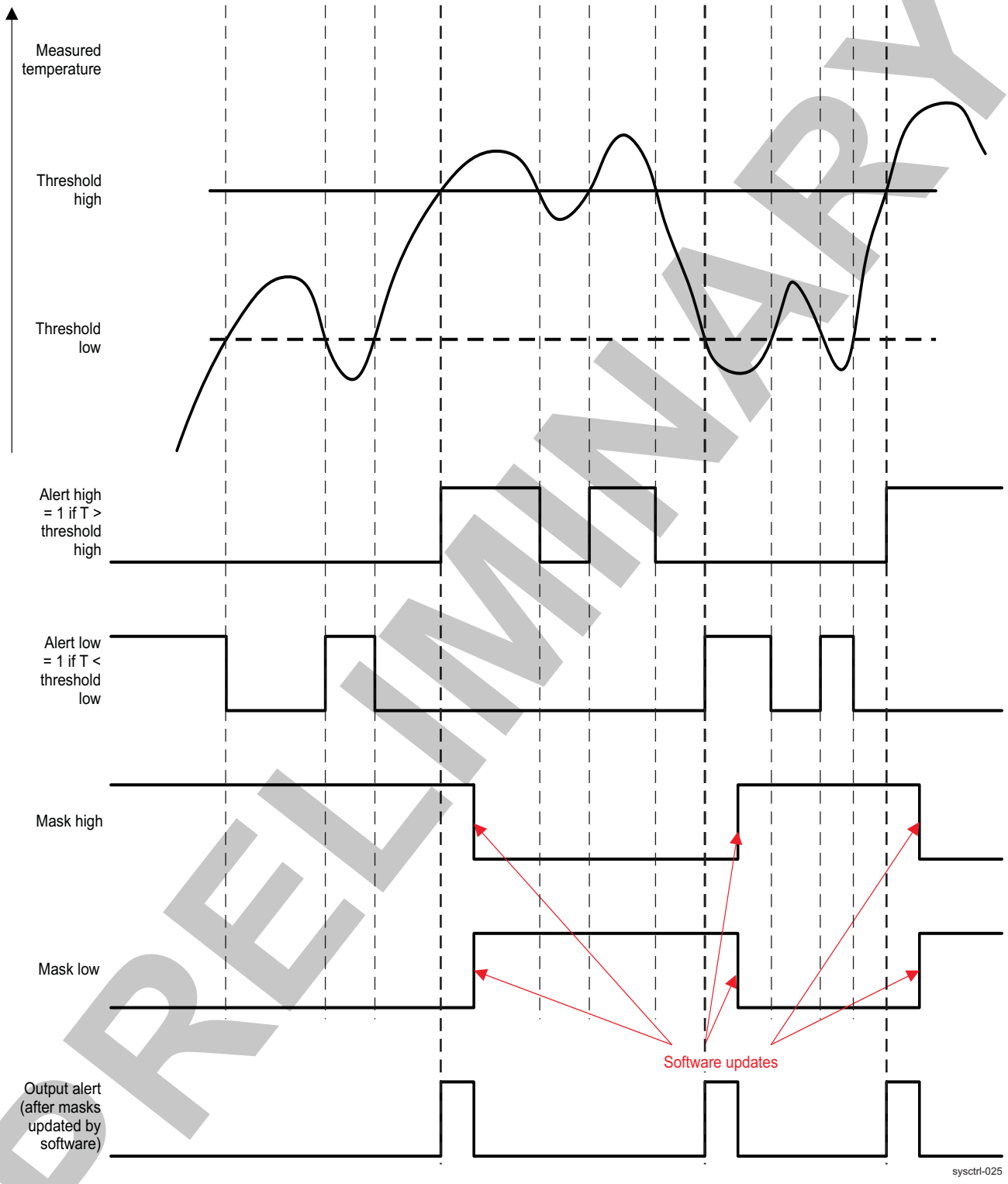
Figure 18-14. Thermal Alert Generation Signals



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18.4.10.2.4 Thermal Shutdown Functionality Comparators

There are three sets (for MPU, for GPU, and for the device die center) of two comparator blocks inside the general core control module. The second set of three comparator blocks cannot be programmed and are responsible for the thermal shutdown protection of the device. The values of the three high and low TSHUT thresholds are set by default and connot be overriden by software.

High thresholds can be read through the following bit fields:

- CONTROL_BANDGAP_TSHUT_MPU[25:16] TSHUT_HOT_MPU
- CONTROL_BANDGAP_TSHUT_MM[25:16] TSHUT_HOT_MM
- CONTROL_BANDGAP_TSHUT_CORE[25:16] TSHUT_HOT_CORE

Low thresholds can be read through the following bit fields:

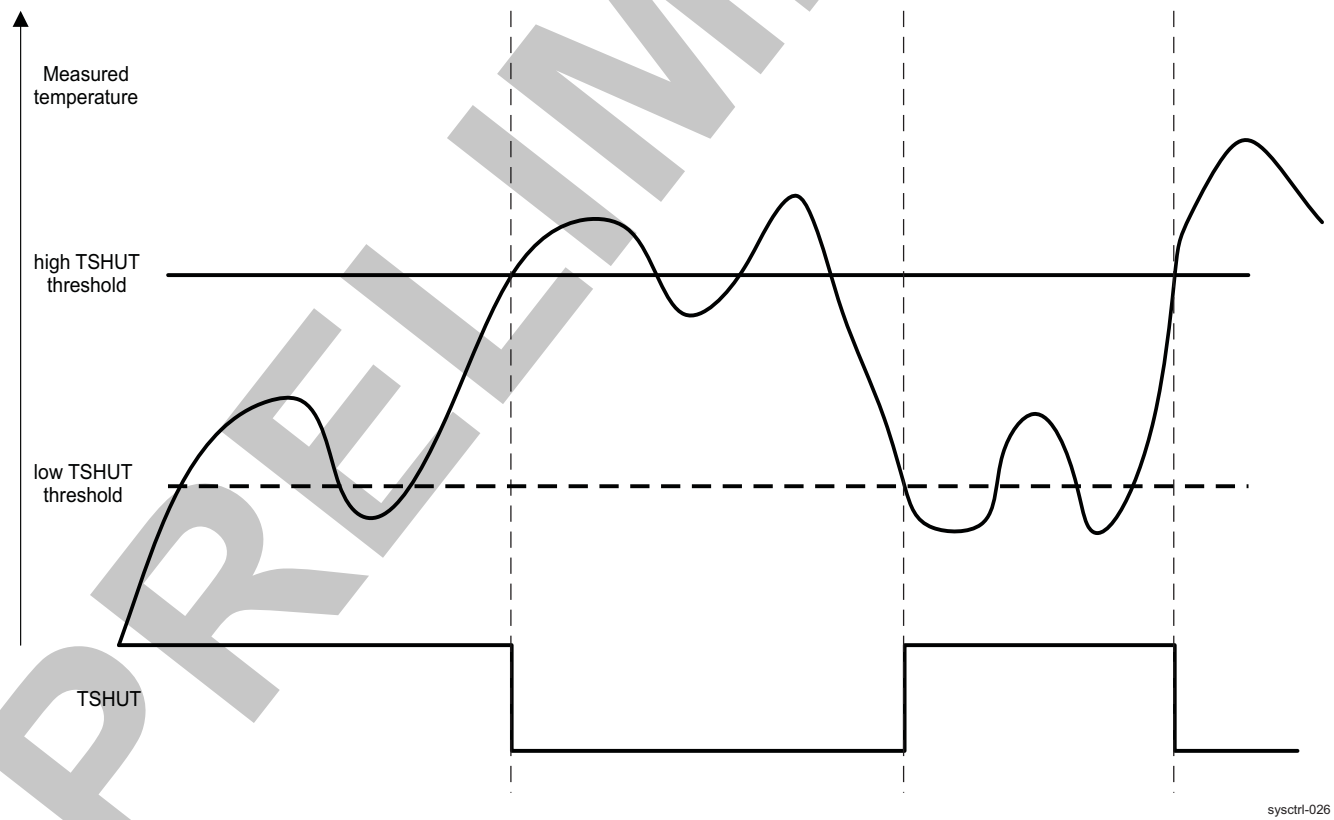
- CONTROL_BANDGAP_TSHUT_MPU[9:0] TSHUT_COLD_MPU
- CONTROL_BANDGAP_TSHUT_MM[9:0] TSHUT_COLD_MM
- CONTROL_BANDGAP_TSHUT_CORE[9:0] TSHUT_COLD_CORE

When the maximum allowed MPU, GPU, or device die center temperature is reached, one of the three TSHUT outputs is activated, respectively (see Figure 18-13). Each of these TSHUT outputs is tied internally to the PRCM module, and is used as a warm reset signal. It flags that the maximum MPU, GPU, or device die center junction temperature is reached.

To deactivate each TSHUT output, the temperature must go below the value of each low TSHUT threshold.

Figure 18-15 shows the behavior of the TSHUT logic.

Figure 18-15. Thermal Shutdown Generation Signals



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18.4.10.2.5 Temperature Timestamping

Each time one of the three bit fields (CONTROL_TEMP_SENSOR_MPU[9:0] BGAP_DTEMP_MPU, CONTROL_TEMP_SENSOR_MM[9:0] BGAP_DTEMP_MM, and CONTROL_TEMP_SENSOR_CORE[9:0] BGAP_DTEMP_CORE) is updated with new temperature value, this value is also automatically stored into a 5-level deep FIFO and a timestamp is also registered. The FIFO registers are in CTRL_MODULE_CORE.

There are three (one for MPU, one for GPU, and one for the device die center) 5-level FIFOs which store a brief history for the last few temperature measurements and are also dedicated to temperature timestamping feature.

The MPU FIFO consists of the following registers:

- CONTROL_DTEMP_MPU_0
- CONTROL_DTEMP_MPU_1
- CONTROL_DTEMP_MPU_2
- CONTROL_DTEMP_MPU_3
- CONTROL_DTEMP_MPU_4

The GPU FIFO consists of the following registers:

- CONTROL_DTEMP_MM_0
- CONTROL_DTEMP_MM_1
- CONTROL_DTEMP_MM_2
- CONTROL_DTEMP_MM_3
- CONTROL_DTEMP_MM_4

The device die center FIFO consists of the following registers:

- CONTROL_DTEMP_CORE_0
- CONTROL_DTEMP_CORE_1
- CONTROL_DTEMP_CORE_2
- CONTROL_DTEMP_CORE_3
- CONTROL_DTEMP_CORE_4

Table 18-18 shows a generic description of FIFOs.

Each FIFO has two fields. The first one is 10 bits wide, 5 levels deep, and is intended to store the temperature values for the last five measurements. The second field is 22 bits wide, 5 levels deep, and acts like a counter for the number of temperature measurements.

Table 18-18. FIFOs Generic Description

FIFO Levels	Second FIFO Field (22 Bits) – Timestamp Bits [31:10] (x=MPU,MM and CORE)	Description	First FIFO field (10 Bits) – Temperature Bits [9:0] (x=MPU,MM and CORE)	Description
Level 1	DTEMP_TAG_x_0	Indicates the number of temperature measurements	DTEMP_TEMPERATURE_x_0	Indicates the last measured temperature value (the most recent sample)
Level 2	DTEMP_TAG_x_1	Indicates the number of temperature measurements minus one (DTEMP_TEMPERATURE_x_0 – 1)	DTEMP_TEMPERATURE_x_1	Indicates the penultimate measured temperature value
Level 3	DTEMP_TAG_x_2	Indicates the number of temperature measurements minus two (DTEMP_TEMPERATURE_x_0 – 2)	DTEMP_TEMPERATURE_x_2	Indicates temperature value measured before DTEMP_TEMPERATURE_x_1

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Table 18-18. FIFOs Generic Description (continued)

FIFO Levels	Second FIFO Field (22 Bits) – Timestamp Bits [31:10] (x=MPU,MM and CORE)	Description	First FIFO field (10 Bits) – Temperature Bits [9:0] (x=MPU,MM and CORE)	Description
Level 4	DTEMP_TAG_x_3	Indicates the number of temperature measurements minus three (DTEMP_TEMPERATURE_x_0 – 3)	DTEMP_TEMPERATURE_x_3	Indicates temperature value measured before DTEMP_TEMPERATURE_x_2
Level 5	DTEMP_TAG_x_4	Indicates the number of temperature measurements minus four (DTEMP_TEMPERATURE_x_0 – 4)	DTEMP_TEMPERATURE_x_4	Indicates temperature value measured before DTEMP_TEMPERATURE_x_3 (the oldest sample)

NOTE: DTEMP_TAG_x_4 (where x=MPU,MM and CORE) increments its value with one after each fifth temperature measurement.

DTEMP_TAG_x_3 (where x=MPU,MM and CORE) increments its value with one after each forth temperature measurement.

DTEMP_TAG_x_2 (where x=MPU,MM and CORE) increments its value with one after each third temperature measurement.

DTEMP_TAG_x_1 (where x=MPU,MM and CORE) increments its value with one after each second temperature measurement.

DTEMP_TAG_x_0 (where x=MPU,MM and CORE) increments its value with one after each temperature measurement.

Software can stop a certain FIFO to update with new temperature and timestamp values when setting one of the following bits to 0x1:

- CONTROL_BANDGAP_MASK[21] FREEZE_MPU for the MPU FIFO.
- CONTROL_BANDGAP_MASK[22] FREEZE_MM for the GPU FIFO.
- CONTROL_BANDGAP_MASK[23] FREEZE_CORE for the device die center FIFO.

These 3 bits are automatically cleared by hardware after FIFOs are reset.

Each FIFO can also be cleared setting the following bits to 0x1:

- CONTROL_BANDGAP_MASK[18] CLEAR_MPU for the MPU FIFO.
- CONTROL_BANDGAP_MASK[19] CLEAR_MM for the GPU FIFO.
- CONTROL_BANDGAP_MASK[20] CLEAR_CORE for the device die center FIFO.

These 3 bits are automatically cleared by hardware after FIFOs are reset.

18.4.10.2.6 Temperature Accumulators

Three registers are intended to accumulate the temperature after each measurement. The value of every next temperature measurement is added to the previous value and then stored in the following bit fields:

- CONTROL_BANDGAP_CUMUL_DTEMP_MPU[31:0] CUMUL_DTEMP_MPU
- CONTROL_BANDGAP_CUMUL_DTEMP_MM[31:0] CUMUL_DTEMP_MM
- CONTROL_BANDGAP_CUMUL_DTEMP_CORE[31:0] CUMUL_DTEMP_CORE

Software can divide the accumulated in each register value to the number of measurements and thus get the average temperature. For example, the MPU average temperature for a given time period is:

MPU Average Temperature = CONTROL_BANDGAP_CUMUL_DTEMP_MPU[31:0] CUMUL_DTEMP_MPU / CONTROL_DTEMP_MPU_0[31:10] DTEMP_TAG_MPU_0

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Software can reset CONTROL_BANDGAP_CUMUL_DTEMP_MPU[31:0] CUMUL_DTEMP_MPU, CONTROL_BANDGAP_CUMUL_DTEMP_MM[31:0] CUMUL_DTEMP_MM, and CONTROL_BANDGAP_CUMUL_DTEMP_CORE[31:0] CUMUL_DTEMP_CORE temperature accumulators through bits CONTROL_BANDGAP_MASK[15] CLEAR_ACCUM_MPU, CONTROL_BANDGAP_MASK[16] CLEAR_ACCUM_MM, and CONTROL_BANDGAP_MASK[17] CLEAR_ACCUM_CORE, respectively, setting each one of them to 0x1. These bits also reset the three FIFOs and are automatically cleared by hardware when the reset procedure completes.

18.4.10.2.7 Bandgap FSMs Power Management

Each one of the three bandgap FSMs comply with the PRCM power-management protocol. They share common functional clock (L3INSTR_TS_GCLK), which is automatically gated by PRCM depending on the value of the CONTROL_BANDGAP_MASK[31:30] SIDLEMODE bit field. L3INSTR_TS_GCLK clock is also enabled automatically by the PRCM module.

18.4.10.2.8 ADC Codes Versus Temperature

Table 18-19 gives the temperature range that corresponds to each value of the following bit fields:

- CONTROL_TEMP_SENSOR_MPU[9:0] BGAP_DTEMP_MPU
- CONTROL_TEMP_SENSOR_MM[9:0] BGAP_DTEMP_MM
- CONTROL_TEMP_SENSOR_CORE[9:0] BGAP_DTEMP_CORE

Table 18-19. ADC Code Versus Temperature

ADC Code	Temperature		ADC Code	Temperature		ADC Code	Temperature		ADC Code	Temperature	
	From	To		From	To		From	To		From	To
0-539	Outside region of operation										
540	-40	-40	586	-22.4	-22	632	-2.8	-2.4	678	16.4	16.8
541	-40	-40	587	-22	-21.6	633	-2.4	-2	679	16.8	17.2
542	-40	-40	588	-21.6	-21.2	634	-2	-1.6	680	17.2	17.6
543	-40	-40	589	-21.2	-20.8	635	-1.6	-1.2	681	17.6	18
544	-40	-39.6	590	-20.8	-20.2	636	-1.2	-0.8	682	18	18.4
545	-39.6	-39.2	591	-20.2	-19.6	637	-0.8	-0.4	683	18.4	18.8
546	-39.2	-38.8	592	-19.6	-19.2	638	-0.4	0	684	18.8	19.2
547	-38.8	-38.4	593	-19.2	-18.8	639	0	0.4	685	19.2	19.6
548	-38.4	-38	594	-18.8	-18.4	640	0.4	0.8	686	19.6	20
549	-38	-37.6	595	-18.4	-18	641	0.8	1.2	687	20	20.4
550	-37.6	-37.2	596	-18	-17.6	642	1.2	1.6	688	20.4	20.8
551	-37.2	-36.8	597	-17.6	-17.2	643	1.6	2	689	20.8	21.2
552	-36.8	-36.4	598	-17.2	-16.8	644	2	2.4	690	21.2	21.6
553	-36.4	-36	599	-16.8	-16.4	645	2.4	2.8	691	21.6	22.2
554	-36	-35.6	600	-16.4	-16	646	2.8	3.2	692	22.2	22.8
555	-35.6	-35	601	-16	-15.6	647	3.2	3.6	693	22.8	23.2
556	-35	-34.4	602	-15.6	-15.2	648	3.6	4.2	694	23.2	23.6
557	-34.4	-34	603	-15.2	-14.8	649	4.2	4.8	695	23.6	24
558	-34	-33.6	604	-14.8	-14.4	650	4.8	5.2	696	24	24.4
559	-33.6	-33.2	605	-14.4	-14	651	5.2	5.6	697	24.4	24.8
560	-33.2	-32.8	606	-14	-13.6	652	5.6	6	698	24.8	25.2
561	-32.8	-32.4	607	-13.6	-13.2	653	6	6.4	699	25.2	25.6
562	-32.4	-32	608	-13.2	-12.8	654	6.4	6.8	700	25.6	26
563	-32	-31.6	609	-12.8	-12.2	655	6.8	7.2	701	26	26.4
564	-31.6	-31.2	610	-12.2	-11.6	656	7.2	7.6	702	26.4	26.8

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Table 18-19. ADC Code Versus Temperature (continued)

ADC Code	Temperature		ADC Code	Temperature		ADC Code	Temperature		ADC Code	Temperature	
565	-31.2	-30.8	611	-11.6	-11.2	657	7.6	8	703	26.8	27.2
566	-30.8	-30.4	612	-11.2	-10.8	658	8	8.4	704	27.2	27.6
567	-30.4	-30	613	-10.8	-10.4	659	8.4	8.8	705	27.6	28
568	-30	-29.6	614	-10.4	-10	660	8.8	9.2	706	28	28.4
569	-29.6	-29.2	615	-10	-9.6	661	9.2	9.6	707	28.4	28.8
570	-29.2	-28.8	616	-9.6	-9.2	662	9.6	10	708	28.8	29.2
571	-28.8	-28.4	617	-9.2	-8.8	663	10	10.4	709	29.2	29.6
572	-28.4	-28	618	-8.8	-8.4	664	10.4	10.8	710	29.6	30
573	-28	-27.4	619	-8.4	-8	665	10.8	11.2	711	30	30.4
574	-27.4	-26.8	620	-8	-7.6	666	11.2	11.6	712	30.4	30.8
575	-26.8	-26.4	621	-7.6	-7.2	667	11.6	12	713	30.8	31.2
576	-26.4	-26	622	-7.2	-6.8	668	12	12.4	714	31.2	31.6
577	-26	-25.6	623	-6.8	-6.4	669	12.4	13	715	31.6	32.2
578	-25.6	-25.2	624	-6.4	-6	670	13	13.6	716	32.2	32.8
579	-25.2	-24.8	625	-6	-5.6	671	13.6	14	717	32.8	33.2
580	-24.8	-24.4	626	-5.6	-5.2	672	14	14.4	718	33.2	33.6
581	-24.4	-24	627	-5.2	-4.8	673	14.4	14.8	719	33.6	34
582	-24	-23.6	628	-4.8	-4.2	674	14.8	15.2	720	34	34.4
583	-23.6	-23.2	629	-4.2	-3.6	675	15.2	15.6	721	34.4	34.8
584	-23.2	-22.8	630	-3.6	-3.2	676	15.6	16	722	34.8	35.2
585	-22.8	-22.4	631	-3.2	-2.8	677	16	16.4	723	35.2	35.6
724	35.6	36	770	54.4	54.8	816	73.6	74	862	92	92.4
725	36	36.4	771	54.8	55.2	817	74	74.4	863	92.4	92.8
726	36.4	36.8	772	55.2	55.6	818	74.4	74.8	864	92.8	93.2
727	36.8	37.2	773	55.6	56.2	819	74.8	75.2	865	93.2	93.6
728	37.2	37.6	774	56.2	56.8	820	75.2	75.6	866	93.6	94
729	37.6	38	775	56.8	57.2	821	75.6	76	867	94	94.4
730	38	38.4	776	57.2	57.6	822	76	76.4	868	94.4	94.8
731	38.4	38.8	777	57.6	58	823	76.4	76.8	869	94.8	95.2
732	38.8	39.2	778	58	58.4	824	76.8	77.2	870	95.2	95.6
733	39.2	39.6	779	58.4	58.8	825	77.2	77.6	871	95.6	96
734	39.6	40	780	58.8	59.2	826	77.6	78	872	96	96.4
735	40	40.4	781	59.2	59.6	827	78	78.4	873	96.4	96.8
736	40.4	40.8	782	59.6	60	828	78.4	78.8	874	96.8	97.2
737	40.8	41.2	783	60	60.4	829	78.8	79.2	875	97.2	97.8
738	41.2	41.6	784	60.4	60.8	830	79.2	79.6	876	97.8	98.4
739	41.6	42	785	60.8	61.2	831	79.6	80	877	98.4	98.8
740	42	42.4	786	61.2	61.6	832	80	80.4	878	98.8	99.2
741	42.4	42.8	787	61.6	62	833	80.4	80.8	879	99.2	99.6
742	42.8	43.4	788	62	62.4	834	80.8	81.2	880	99.6	100
743	43.4	44	789	62.4	62.8	835	81.2	81.6	881	100	100.4
744	44	44.4	790	62.8	63.2	836	81.6	82	882	100.4	100.8
745	44.4	44.8	791	63.2	63.6	837	82	82.4	883	100.8	101.2
746	44.8	45.2	792	63.6	64	838	82.4	82.8	884	101.2	101.6
747	45.2	45.6	793	64	64.4	839	82.8	83.2	885	101.6	102
748	45.6	46	794	64.4	64.8	840	83.2	83.6	886	102	102.4

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Table 18-19. ADC Code Versus Temperature (continued)

ADC Code	Temperature		ADC Code	Temperature		ADC Code	Temperature		ADC Code	Temperature	
749	46	46.4	795	64.8	65.2	841	83.6	84	887	102.4	102.8
750	46.4	46.8	796	65.2	65.6	842	84	84.4	888	102.8	103.2
751	46.8	47.2	797	65.6	66	843	84.4	84.8	889	103.2	103.6
752	47.2	47.6	798	66	66.4	844	84.8	85.2	890	103.6	104
753	47.6	48	799	66.4	66.8	845	85.2	85.6	891	104	104.4
754	48	48.4	800	66.8	67.2	846	85.6	86	892	104.4	104.8
755	48.4	48.8	801	67.2	67.6	847	86	86.4	893	104.8	105.2
756	48.8	49.2	802	67.6	68	848	86.4	86.8	894	105.2	105.6
757	49.2	49.6	803	68	68.4	849	86.8	87.2	895	105.6	106
758	49.6	50	804	68.4	68.8	850	87.2	87.6	896	106	106.4
759	50	50.4	805	68.8	69.2	851	87.6	88	897	106.4	106.8
760	50.4	50.8	806	69.2	69.6	852	88	88.4	898	106.8	107.2
761	50.8	51.2	807	69.6	70	853	88.4	88.8	899	107.2	107.6
762	51.2	51.6	808	70	70.4	854	88.8	89.2	900	107.6	108
763	51.6	52	809	70.4	70.8	855	89.2	89.6	901	108	108.4
764	52	52.4	810	70.8	71.2	856	89.6	90	902	108.4	108.8
765	52.4	52.8	811	71.2	71.8	857	90	90.4	903	108.8	109.2
766	52.8	53.2	812	71.8	72.4	858	90.4	90.8	904	109.2	109.6
767	53.2	53.6	813	72.4	72.8	859	90.8	91.2	905	109.6	110
768	53.6	54	814	72.8	73.2	860	91.2	91.6	906	110	110.4
769	54	54.4	815	73.2	73.6	861	91.6	92	907	110.4	110.8
908	110.8	111.2	922	116.4	116.8	936	122	122.4			
909	111.2	111.6	923	116.8	117.2	937	122.4	122.8			
910	111.6	112	924	117.2	117.6	938	122.8	123.2			
911	112	112.4	925	117.6	118	939	123.2	123.6			
912	112.4	112.8	926	118	118.4	940	123.6	124			
913	112.8	113.2	927	118.4	118.8	941	124	124.4			
914	113.2	113.6	928	118.8	119.2	942	124.4	124.8			
915	113.6	114	929	119.2	119.6	943	124.8	125			
916	114	114.4	930	119.6	120	945	125	125			
917	114.4	114.8	931	120	120.4	945	125	125			
918	114.8	115.2	932	120.4	120.8	945	125	125			
919	115.2	115.6	933	120.8	121.2	945	125	125			
920	115.6	116	934	121.2	121.6	946-1023					
921	116	116.4	935	121.6	122						

NOTE: ADC code values in the subranges 0–539 and 946–1023 are reserved for future use.

18.4.11 Hardware Observability

18.4.11.1 Device Internal Signals Observability Overview

The general control module provides observability features covering different module internal signals related to:

- Power and reset management protocol inside different power domains
- Power domain states and transition indication

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- IRQs by different modules
- DMA requests by different modules
- Clocks and clock management

The associated signal multiplexing function is controlled through the hardware observability I/O multiplexing registers (32-bit read/write registers). The selected observable signals reside in the CORE or WKUP power domain and are mapped on the po_hw_dbg[31:0] observability bus, which is in the WKUP power domain. The po_hw_dbg[31:16] and po_hw_dbg[15:0] observability outputs are then further multiplexed as their corresponding hw_dbg[31:16] and hw_wkdbg[15:0] signals on the different pads of the CORE and WKUP power domain, respectively.

Figure 18-16 is an overview of observability multiplexing, which minimizes the number of signals exchanged at the device boundary.

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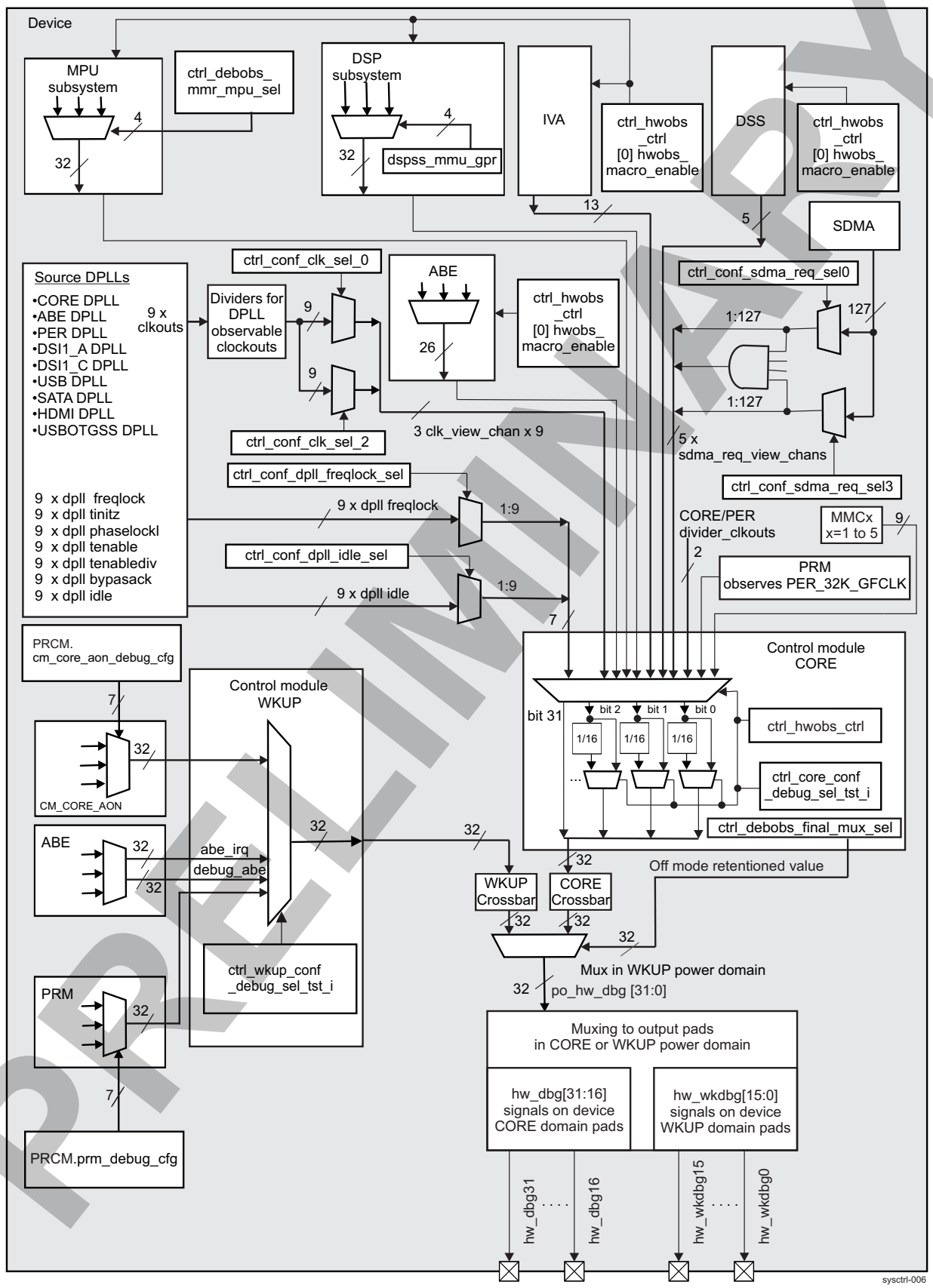
Figure 18-16. Overview of the Hardware Observability Functionality



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18.4.11.2 Observability Gating Capabilities

The programmer has the option to gate all 32 signals of the observability bus simultaneously at the observability paths of the CORE and WKUP power domains, keeping them tied to 1 (CONTROL_HWOBS_CONTROL[1] HWOBS_ALL_ONE_MODE = 0b1) or keeping them tied to 0 (CONTROL_HWOBS_CONTROL[2] HWOBS_ALL_ZERO_MODE = 0b1). This can be useful to check the path from hardware observability to external pads. These 2 bits must be set to 0 to enable the observability feature for all observability pads.

Additionally, the CONTROL_HWOBS_CONTROL[0] HWOBS_MACRO_ENABLE bit provides the gating feature only to observability signals muxed in the CORE power domain that come from the following modules (identified in the so-called MACRO group):

- MPU subsystem
- DSP subsystem
- IVA
- Display subsystem
- CM_CORE
- ABE

When the CONTROL_HWOBS_CONTROL[0] HWOBS_MACRO_ENABLE bit is set to 0b0, the observability outputs associated with the MACRO group are gated and forced to 0b0.

NOTE: Do not set the observability gating bits CONTROL_HWOBS_CONTROL[1] HWOBS_ALL_ONE_MODE and CONTROL_HWOBS_CONTROL[2] HWOBS_ALL_ZERO_MODE simultaneously to 1 to avoid undefined states of the observability bus.

In the CORE power domain, the frequency of the signals which are mapped on po_hw_dbg[2:0] lines can be optionally divided by 1, 2, 4, 8, or 16 through programming dedicated bit fields in the CONTROL_HWOBS_CONTROL register.

Assignment of the dividers is as follows:

- CONTROL_HWOBS_CONTROL[7:3] HWOBS_CLKDIV_SEL for po_hw_dbg0
- CONTROL_HWOBS_CONTROL[13:9] HWOBS_CLKDIV_SEL_1 for po_hw_dbg1
- CONTROL_HWOBS_CONTROL[18:14] HWOBS_CLKDIV_SEL_2 for po_hw_dbg2

NOTE: To enable observability over the po_hw_dbg0, po_hw_dbg1, and po_hw_dbg2 bus lines, the respective bit fields in the CONTROL_HWOBS_CONTROL register (HWOBS_CLKDIV_SEL, HWOBS_CLKDIV_SEL_1, and HWOBS_CLKDIV_SEL_2) must be set different than 0. The default value (0) is not sufficient to see an observability value.

NOTE: The frequency division and ability to gate the MACRO group observability signals (configurable in the CONTROL_HWOBS_CONTROL register) are limited only to hardware observability signals multiplexed and propagated in the CORE power domain (CONTROL_DEBOBS_FINAL_MUX_SEL[i] SELECT = 0b1).

These options do not apply to hardware observability signals muxed and propagated in the WKUP power domain (CONTROL_DEBOBS_FINAL_MUX_SEL[i] SELECT = 0b0).

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18.4.11.3 Observability Signals Multiplexing at General Core/Wake-Up Control Level

Most of the observability multiplexers (MACRO group modules/DPLLs/sDMA associated) are configurable in CTRL_MODULE_CORE, which is part of the switchable CORE power domain. Signal multiplexers are also instantiated in CTRL_MODULE_WKUP (CM1/PRM/ABE dedicated), which is part of the WKUP power domain. The CONTROL_DEBOBS_FINAL_MUX_SEL[31:0] SELECT bit field, instantiated in the CORE power domain, selects a signal to be observed between the outputs at the CORE and WKUP multiplexing levels. A bit from this register set to 1 selects to route a signal from the CORE power domain to a certain po_hw_dbgn (where n = 0 to 31) line; when the bit is set to 0, selects to route a signal from the WKUP power domain to the same line. The output of this top-level multiplexing is further passed to the pad configuration muxing I/O level within device control module boundaries.

The module and view-channel selection/reduction layer in the CORE domain is configured through the 5-bit field MODE in the 32 × 32-bit registers CONTROL_CORE_CONF_DEBUG_SEL_TST_0 through CONTROL_CORE_CONF_DEBUG_SEL_TST_31. The following modules can be selected as source of observability signals: Cortex-A15 MPU subsystem, DSP subsystem, IVA, display subsystem, CM2, and ABE (MACRO signal sources).

Some of the CONTROL_CONF_DEBUG_SEL_TST registers are responsible for selection of sDMA view channels, different DPLL clock view channels, and other signal view channels.

- 3 x DPLL clkout signal view channels
- 7 x DPLL (other than clkout signal) view channels
- 5 x sDMA signal view channels
- 3 x additional clkout view channels monitoring the hwobs_coredivider_clkout3, hwobs_perdivider_clkout4, and hwobs_pd_l4_per_per32k_gfclk signals

Table 18-20 summarizes the internal signals multiplexing schema for each of the 32 CONTROL_CORE_CONF_DEBUG_SEL_TST registers.

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Table 18-20. CORE Power Domain Observability Signals Multiplexing Modes 0 to 17

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12	INPUT13	INPUT14	INPUT15	INPUT16	INPUT17
Reg Name	Reg	Reg	Mode value upon POR	Mode 0x0	Mode 0x1	Mode 0x2	Mode 0x3	Mode 0x4	Mode 0x5	Mode 0x6	Mode 0x7	Mode 0x8	Mode 0x9	Mode 0xA	Mode 0xB	Mode 0xC	Mode 0xD	Mode 0xE	Mode 0xF	Mode 0x10	Mode 0x11
CONTROL_CORE_CONF_DEBUG_SEL_TST_0	0	0x04D0	0x0	hwobs_debug_mpu_0	clk_view_0	Reserved	Reserved	hwobs_debug_dsp_1	Reserved	hwobs_debug_ivahd_0	Reserved	hwobs_debug_abe_0	hwobs_debug_dsp_0	Reserved	Reserved	hwobs_debug_dsp_2	Reserved	Reserved	Reserved	Reserved	dpllctrl_plllock
CONTROL_CORE_CONF_DEBUG_SEL_TST_1	1	0x04D4	0x0	hwobs_debug_mpu_1	clk_view_1	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_1	Reserved	hwobs_debug_abe_1	hwobs_debug_dsp_1	Reserved	Reserved	Reserved	Reserved	hwobs_emif1_pwr_sidlereq	Reserved	Reserved	dpllctrl_pllrecal
CONTROL_CORE_CONF_DEBUG_SEL_TST_2	2	0x04D8	0x0	hwobs_debug_mpu_2	clk_view_2	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_2	Reserved	hwobs_debug_abe_2	hwobs_debug_dsp_2	Reserved	hwobs_dsshdmiphypwrcmdtxon	Reserved	Reserved	hwobs_emif1_pwr_sidleack(1)	Reserved	Reserved	dpllctrl_stopclock
CONTROL_CORE_CONF_DEBUG_SEL_TST_3	3	0x04DC	0x0	hwobs_debug_mpu_3	dpll_freqlock	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_3	Reserved	hwobs_debug_abe_3	hwobs_debug_dsp_3	Reserved	hwobs_dsshdmiphypwrcmdoff	Reserved	Reserved	hwobs_emif1_pwr_sidleack(0)	Reserved	Reserved	dpllctrl_stopclockackz
CONTROL_CORE_CONF_DEBUG_SEL_TST_4	4	0x04E0	0x0	hwobs_debug_mpu_4	dpll_tinitz	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_4	Reserved	hwobs_debug_abe_4	hwobs_debug_dsp_4	Reserved	hwobs_dsshdmiphypwrack	Reserved	Reserved	hwobs_emif1_pwr_fclken	Reserved	Reserved	dpllctrl_dispcupdatesync
CONTROL_CORE_CONF_DEBUG_SEL_TST_5	5	0x04E4	0x0	hwobs_debug_mpu_5	dpll_phaselock	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_5	Reserved	hwobs_debug_abe_5	hwobs_debug_dsp_5	Reserved	hwobs_dsshdmihpd	Reserved	Reserved	hwobs_emif1_sys_err_intr_req	Reserved	Reserved	Reserved
CONTROL_CORE_CONF_DEBUG_SEL_TST_6	6	0x04E8	0x0	hwobs_debug_mpu_6	dpll_tenable	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_6	Reserved	hwobs_debug_abe_6	hwobs_debug_dsp_6	Reserved	Reserved	Reserved	Reserved	hwobs_emif1_sys_err_intr_pend	Reserved	Reserved	Reserved

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Table 18-20. CORE Power Domain Observability Signals Multiplexing Modes 0 to 17 (continued)

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12	INPUT13	INPUT14	INPUT15	INPUT16	INPUT17
CONTROL_CORE_CONF_DEBUG_SEL_TST_7	7	0x04EC	0x0	hwobs_debug_mpu_7	dpll_tenablediv	sdma_req_view(0)	Reserved	Reserved	Reserved	hwobs_debug_ivahd_7	Reserved	hwobs_debug_abe_7	hwobs_debug_dsp_7	Reserved	Reserved	Reserved	Reserved	hwobs_emif1_ll_err_intr_req	Reserved	Reserved	Reserved
CONTROL_CORE_CONF_DEBUG_SEL_TST_8	8	0x04F0	0x0	hwobs_debug_mpu_8	dpll_bypassack	sdma_req_view_1	Reserved	Reserved	Reserved	hwobs_debug_ivahd_8	Reserved	hwobs_debug_abe_8	hwobs_debug_dsp_8	Reserved	Reserved	Reserved	Reserved	hwobs_emif1_ll_err_intr_pend	Reserved	Reserved	Reserved
CONTROL_CORE_CONF_DEBUG_SEL_TST_9	9	0x04F4	0x0	hwobs_debug_mpu_9	dpll_idle	sdma_req_view_2	Reserved	Reserved	Reserved	hwobs_debug_ivahd_9	Reserved	hwobs_debug_abe_9	hwobs_debug_dsp_9	Reserved	Reserved	Reserved	Reserved	hwobs_emif1_ret_powerRet	Reserved	Reserved	Reserved
CONTROL_CORE_CONF_DEBUG_SEL_TST_10	10	0x04F8	0x0	hwobs_debug_mpu_10	Reserved	sdma_req_view_3	Reserved	Reserved	Reserved	hwobs_debug_ivahd_10	Reserved	hwobs_debug_abe_10	hwobs_debug_dsp_10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CONTROL_CORE_CONF_DEBUG_SEL_TST_11	11	0x04FC	0x0	hwobs_debug_mpu_11	hwobs_emif1_pwr_sidlereq	sdma_req_view_all	Reserved	Reserved	Reserved	hwobs_debug_ivahd_11	Reserved	hwobs_debug_abe_11	hwobs_debug_dsp_11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CONTROL_CORE_CONF_DEBUG_SEL_TST_12	12	0x0500	0x0	hwobs_debug_mpu_12	hwobs_emif1_pwr_sidleack_(1)	hwobs_corediv ider_clkout3	Reserved	Reserved	Reserved	hwobs_debug_ivahd_12	Reserved	hwobs_debug_abe_12	hwobs_debug_dsp_12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CONTROL_CORE_CONF_DEBUG_SEL_TST_13	13	0x0504	0x0	hwobs_debug_mpu_13	hwobs_emif1_pwr_sidleack_(0)	hwobs_perdivider_clkout4	Reserved	Reserved	Reserved	hwobs_debug_ivahd_13	Reserved	hwobs_debug_abe_13	hwobs_debug_dsp_13	Reserved	Reserved	Reserved	Reserved	hwobs_emif2_pwr_sidlereq	Reserved	Reserved	Reserved

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Table 18-20. CORE Power Domain Observability Signals Multiplexing Modes 0 to 17 (continued)

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12	INPUT13	INPUT14	INPUT15	INPUT16	INPUT17
CONTROL_CORE_CONF_DEBUG_SEL_TST_14	14	0x0508	0x0	hwobs_debug_mpu_14	hwobs_emif1_pwr_fclken	hwobs_pd_l4_per_per32k_gfclk	Reserved	Reserved	Reserved	hwobs_debug_ivahd_14	Reserved	hwobs_debug_abe_14	hwobs_debug_dsp_14	Reserved	Reserved	Reserved	Reserved	hwobs_emif2_pwr_sidleack_(1)	Reserved	Reserved	Reserved
CONTROL_CORE_CONF_DEBUG_SEL_TST_15	15	0x050C	0x0	hwobs_debug_mpu_15	hwobs_emif1_sys_err_intr_req	0	Reserved	Reserved	Reserved	hwobs_debug_ivahd_15	Reserved	hwobs_debug_abe_15	hwobs_debug_dsp_15	Reserved	Reserved	Reserved	Reserved	hwobs_emif2_pwr_sidleack_(0)	Reserved	Reserved	dpll_freqlock
CONTROL_CORE_CONF_DEBUG_SEL_TST_16	16	0x0510	0x0	hwobs_debug_mpu_16	hwobs_emif1_sys_err_intr_pend	geni	Reserved	Reserved	Reserved	hwobs_debug_ivahd_16	Reserved	hwobs_debug_abe_16	hwobs_debug_dsp_16	Reserved	Reserved	Reserved	Reserved	hwobs_emif2_pwr_fclken	Reserved	Reserved	dpll_tinitz
CONTROL_CORE_CONF_DEBUG_SEL_TST_17	17	0x0514	0x0	hwobs_debug_mpu_17	hwobs_emif1_ll_err_intr_req	geno	Reserved	Reserved	Reserved	hwobs_debug_ivahd_17	Reserved	hwobs_debug_abe_17	hwobs_debug_dsp_17	Reserved	Reserved	Reserved	Reserved	hwobs_emif2_sys_err_intr_req	Reserved	Reserved	dpll_phaselock
CONTROL_CORE_CONF_DEBUG_SEL_TST_18	18	0x0518	0x0	hwobs_debug_mpu_18	hwobs_emif1_ll_err_intr_pend	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_18	Reserved	hwobs_debug_abe_18	hwobs_debug_dsp_18	Reserved	Reserved	Reserved	Reserved	hwobs_emif2_sys_err_intr_pend	Reserved	Reserved	dpll_tenable
CONTROL_CORE_CONF_DEBUG_SEL_TST_19	19	0x051C	0x0	hwobs_debug_mpu_19	hwobs_emif1_ret_powerRet	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_19	Reserved	hwobs_debug_abe_19	hwobs_debug_dsp_19	Reserved	Reserved	Reserved	Reserved	hwobs_emif2_ll_err_intr_req	Reserved	Reserved	dpll_tenablediv

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Table 18-20. CORE Power Domain Observability Signals Multiplexing Modes 0 to 17 (continued)

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12	INPUT13	INPUT14	INPUT15	INPUT16	INPUT17
CONTROL_CORE_CONF_DEBUG_SEL_TST_20	20	0x0520	0x0	hwobs_debug_mpu_20	Reserved	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_20	Reserved	hwobs_debug_abe_20	hwobs_debug_dsp_20	Reserved	Reserved	Reserved	Reserved	hwobs_emif2_ll_err_intr_pend	Reserved	Reserved	dpll_bypassack
CONTROL_CORE_CONF_DEBUG_SEL_TST_21	21	0x0524	0x0	hwobs_debug_mpu_21	Reserved	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_21	Reserved	hwobs_debug_abe_21	hwobs_debug_dsp_21	Reserved	Reserved	Reserved	hwobs_hsi_sidlereq	hwobs_emif2_ret_powerret	Reserved	Reserved	dpll_idle
CONTROL_CORE_CONF_DEBUG_SEL_TST_22	22	0x0528	0x0	hwobs_debug_mpu_22	hwobs_emif2_pwr_sidlereq	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_22	Reserved	hwobs_debug_abe_22	hwobs_debug_dsp_22	Reserved	Reserved	Reserved	hwobs_hsi_fclken	Reserved	Reserved	Reserved	mmcx_adpidle
CONTROL_CORE_CONF_DEBUG_SEL_TST_23	23	0x052C	0x0	hwobs_debug_mpu_23	hwobs_emif2_pwr_sidleack(1)	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_23	Reserved	hwobs_debug_abe_23	hwobs_debug_dsp_23	Reserved	Reserved	Reserved	hwobs_hsi_swakeup (1)	Reserved	Reserved	Reserved	mmcx_adpdat1paden
CONTROL_CORE_CONF_DEBUG_SEL_TST_24	24	0x0530	0x0	hwobs_debug_mpu_24	hwobs_emif2_pwr_sidleack(0)	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_24	Reserved	hwobs_debug_abe_24	hwobs_debug_dsp_24	Reserved	Reserved	Reserved	hwobs_hsi_swakeup (0)	0	Reserved	Reserved	mmcx_ocpl4idlereq
CONTROL_CORE_CONF_DEBUG_SEL_TST_25	25	0x0534	0x0	hwobs_debug_mpu_25	hwobs_emif2_pwr_fclken	Reserved	Reserved	Reserved	Reserved	hwobs_debug_ivahd_25	Reserved	hwobs_debug_abe_25	hwobs_debug_dsp_25	Reserved	Reserved	0	hwobs_hsi_sidleack(1)	0	Reserved	Reserved	mmcx_ocpl3mwait
CONTROL_CORE_CONF_DEBUG_SEL_TST_26	26	0x0538	0x0	hwobs_debug_mpu_26	hwobs_emif2_sys_err_intr_req	Reserved	Reserved	hwobs_dmm_ocpclken	Reserved	hwobs_debug_ivahd_26	Reserved	hwobs_debug_abe_26	hwobs_debug_dsp_26	Reserved	0	0	hwobs_hsi_sidleack(0)	0	Reserved	Reserved	mmcx_pirffret

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Table 18-20. CORE Power Domain Observability Signals Multiplexing Modes 0 to 17 (continued)

REG_NAME	REG_ID	REG_OFFSET	REG_RESET	INPUT0	INPUT1	INPUT2	INPUT3	INPUT4	INPUT5	INPUT6	INPUT7	INPUT8	INPUT9	INPUT10	INPUT11	INPUT12	INPUT13	INPUT14	INPUT15	INPUT16	INPUT17
CONTROL_CORE_CONF_DEBUG_SEL_TST_27	27	0x053C	0x0	hwobs_debug_mpu_27	hwobs_emif2_sys_err_intr_pend	Reserved	Reserved	hwobs_dmm_rstna	Reserved	hwobs_debug_ivahd_27	Reserved	hwobs_debug_abe_27	hwobs_debug_dsp_27	Reserved	0	sdma_req_view_0	hwobs_hsi_mwakeup	0	Reserved	Reserved	mmcx_ocpl4sidleacko1
CONTROL_CORE_CONF_DEBUG_SEL_TST_28	28	0x0540	0x0	hwobs_debug_mpu_28	hwobs_emif2_ll_err_intr_req	Reserved	Reserved	hwobs_dmm_rstretna	Reserved	hwobs_debug_ivahd_28	Reserved	hwobs_debug_abe_28	hwobs_debug_dsp_28	Reserved	0	sdma_req_view_1	hwobs_hsi_mwait	0	Reserved	Reserved	mmcx_ocpl4sidleacko0
CONTROL_CORE_CONF_DEBUG_SEL_TST_29	29	0x0544	0x0	hwobs_debug_mpu_29	hwobs_emif2_ll_err_intr_pend	0	Reserved	hwobs_dmm_idlereq	Reserved	hwobs_debug_ivahd_29	Reserved	hwobs_debug_abe_29	hwobs_debug_dsp_29	Reserved	0	sdma_req_view_2	hwobs_hsi_mstandby	0	Reserved	Reserved	mmcx_ocpl3mstandbyo
CONTROL_CORE_CONF_DEBUG_SEL_TST_30	30	0x0548	0x0	hwobs_debug_mpu_30	hwobs_emif2_ret_powerret	Reserved	Reserved	hwobs_dmm_idleack(1)	Reserved	hwobs_debug_ivahd_30	Reserved	hwobs_debug_abe_30	hwobs_debug_dsp_30	Reserved	0	sdma_req_view_3	hwobs_hsi_retff	0	Reserved	Reserved	mmcx_swakeup
CONTROL_CORE_CONF_DEBUG_SEL_TST_31	31	0x054C	0x0	hwobs_debug_mpu_31	Reserved	Reserved	Reserved	hwobs_dmm_idleack(0)	Reserved	hwobs_debug_ivahd_31	Reserved	hwobs_debug_abe_31	hwobs_debug_dsp_31	Reserved	0	sdma_req_view_all	0	Reserved	Reserved	Reserved	0

A third 1:N selection layer is applied over several signals to route them one-at-a-time to a certain view channel output:

- The CONTROL_CONF_CLK_SEL0[3:0] MULT through CONTROL_CONF_CLK_SEL2[3:0] MULT bit fields control the multiplexing of DPLL CLKOUT signals over three parallel DPLL clockout view channels. The signal source of a certain view channel can be selected to be one of the following DPLLs in the device:
  - CORE DPLL
  - ABE DPLL
  - PER DPLL

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  - DSI1_A DPLL
  - DSI1_C DPLL
  - USB DPLL
  - HDMI DPLL
  - SATA DPLL
  - USBOTGSS DPLL
- The register bit fields associated with the seven different DPLL signal view channels are summarized in Table 18-21. Again, the 4-bit MULT bit field in each of the seven registers makes it possible to choose the source of the DPLL signal to be one of the following DPLLs in the device:
  - CORE DPLL
  - ABE DPLL
  - PER DPLL
  - DSI1_A DPLL
  - DSI1_C DPLL
  - USB DPLL
  - HDMI DPLL
  - SATA DPLL
  - USBOTGSS DPLL
- Nine registers are associated with the power-management observable signals of MMCx (where x = 1 to 5) modules. These registers are summarized in Table 18-22.
- There are four independent sDMA request view channels, each of which has a dedicated register (CONTROL_CONF_SDMA_REQ_SEL0 through CONTROL_CONF_SDMA_REQ_SEL3) with a 7-bit MULT bit field to select 1 from 127 possible DMA_SYSTEM request signals for observation purposes. For more information, see Section 16.1, *DMA_SYSTEM Module Overview*. The fifth channel, sdma_req_view_all, is acquired by applying logical AND reduction over the four currently selected sDMA view channel output signals.
- The General Core observability logic input (hwobs_pd_l4_per_per32k_gfclk) is tied to a PRM output observability signal. This PRM signal corresponds to the hardware gated in the CD_L4_PER clock domain clock (PER_32K_GFCLK), which is directly sourced by the SCRM clock (SYS_32K).
- The General Core observability logic input, hwobs_coredivider_clkout3, is tied to the Core DPLL observability output, CLK_FUNC_1_0_3, which is a direct (nongated, nondivided) version of the CORE DPLL clock output, CLKOUTX2_M3.
- The General Core observability logic input, hwobs_perdivider_clkout4, is tied to the Core DPLL observability output, CLK_FUNC_1_0_4, which is a direct (nongated, nondivided) version of the PER DPLL clock output, CLKOUTX2_M4. For more information, see Section 3.6.3.4, *DPLL_PER Description*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 18-21 lists the DPLL signal observability controls.

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Table 18-21. DPLL Signal Observability Controls

Feature	Type	Register/Bit Field/Observability Control	Description
Different domain DPLL freqlock observability	Control	CONTROL_CONF_DPLL_FREQLOCK_SEL[3:0] MULT	Selects DPLL freqlock view channel
Different domain DPLL phaselock observability	Control	CONTROL_CONF_DPLL_PHASELOCK_SEL[3:0] MULT	Selects DPLL phaselock view channel
Different domain DPLL tinitz observability	Control	CONTROL_CONF_DPLL_TINITZ_SEL[3:0] MULT	Selects to observe DPLL tinitzview channel
Different domain DPLL tenable observability	Control	CONTROL_CONF_DPLL_TENABLE_SEL[3:0] MULT	Selects to observe DPLL tenableview channel
Different domain DPLL tenablediv observability	Control	CONTROL_CONF_DPLL_TENABLEDIV_SEL[3:0] MULT	Selects to observe DPLL tenabledivview channel
Different domain DPLL bypassack observability	Control	CONTROL_CONF_DPLL_BYPASSACK_SEL[3:0] MULT	Selects to observe DPLL bypassackview channel
Different domain DPLL idle observability	Control	CONTROL_CONF_DPLL_IDLE_SEL[3:0] MULT	Selects to observe DPLL idleview channel

Table 18-22. MMCx Signal Observability Controls

Register/Bit Field/Observability Control	Description
CONTROL_CONF_MMCX_ADPIDLE_SEL[2:0] MULT	Selects to observe hwobs_mmcx_adpidle (where x = 1 to 5)
CONTROL_CONF_MMCX_ADPDAT1PADEN_SEL[2:0] MULT	Selects to observe hwobs_mmcx_adpdat1paden (where x = 1 to 5)
CONTROL_CONF_MMCX_OCPL4IDLEREQ_SEL[2:0] MULT	Selects to observe hwobs_mmcx_ocpl4idlereq (where x = 1 to 5)
CONTROL_CONF_MMCX_OCPL3MWAIT_SEL[2:0] MULT	Selects to observe hwobs_mmcx_ocpl3mwait (where x = 1 to 5)
CONTROL_CONF_MMCX_PIRFFRET_SEL[2:0] MULT	Selects to observe hwobs_mmcx_pirffret (where x = 1 to 5)
CONTROL_CONF_MMCX_OCPL4SIDLEACKO1_SEL[2:0] MULT	Selects to observe hwobs_mmcx_ocpl4sidleacko_1 (where x = 1 to 5)
CONTROL_CONF_MMCX_OCPL4SIDLEACKO0_SEL[2:0] MULT	Selects to observe hwobs_mmcx_ocpl4sidleacko_0 (where x = 1 to 5)
CONTROL_CONF_MMCX_OCPL3MSTANDBYO_SEL[2:0] MULT	Selects to observe hwobs_mmcx_ocpl3mstandbyo (where x = 1 to 5)
CONTROL_CONF_MMCX_SWAKEUP_SEL[2:0] MULT	Selects to observe hwobs_mmcx_swakeup (where x = 1 to 5)

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NOTE: Features configured in the following registers are limited to hardware observability signals multiplexed and propagated in the CORE power domain (CONTROL_DEBOBS_FINAL_MUX_SEL[i] SELECT = 0b1):

- CONTROL_CORE_CONF_DEBUG_SEL_TST_0 through CONTROL_CORE_CONF_DEBUG_SEL_TST_31
- CONTROL_CONF_CLK_SEL0[3:0] MULT through CONTROL_CONF_CLK_SEL2[3:0] MULT
- CONTROL_CONF_SDMA_REQ_SEL0 through CONTROL_CONF_SDMA_REQ_SEL3
- CONTROL_CONF_MMCX_ADPIDLE_SEL through CONTROL_CONF_MMCX_SWAKEUP_SEL
- CONTROL_CONF_DPLL_FREQLOCK_SEL
- CONTROL_CONF_DPLL_TINITZ_SEL
- CONTROL_CONF_DPLL_PHASELOCK_SEL
- CONTROL_CONF_DPLL_TENABLE_SEL
- CONTROL_CONF_DPLL_TENABLEDIV_SEL
- CONTROL_CONF_DPLL_BYPASSACK_SEL
- CONTROL_CONF_DPLL_IDLE_SEL

These options do not apply to hardware observability signals muxed and propagated in the WKUP power domain (CONTROL_DEBOBS_FINAL_MUX_SEL[i] SELECT = 0b0).

The CONTROL_WKUP_CONF_DEBUG_SEL_TST_i[1:0] MODE bit (where i = 0 to 31) provides the option to choose between observation of power and reset manager signals in the device or observation of signals related to CM1. If CONTROL_WKUP_CONF_DEBUG_SEL_TST_i[1:0] = 0b1, the hwobs_int_prm_i signal is selected. Otherwise, the hwobs_int_cm1_i signal is output.

NOTE: The CM1 and PRM observable signals are multiplexed in the WKUP power domain.

18.4.11.4 Observability Signals Multiplexing at Device Control Module Level

The pads used for the hardware debug must be properly configured by selecting the hardware debug function (hw_dbgn/hw_wkdbgn) of the pad.

18.4.11.4.1 Observability Signals Muxed on Pads in the CORE Power Domain

To map the hw_dbg16 through hw_dbg31 signals to their associated external device pads in the CORE power domain, set the related MUXMODE bit fields within the CONTROL_CORE_PAD0_C2C_DATAOUT0_PAD1_C2C_DATAOUT1 through CONTROL_CORE_PAD0_C2C_DATA14_PAD1_C2C_DATA15 pad configuration registers to 0b101 (mode 5). These signals can also be mapped on the external device pads in the CORE power domain through the following registers (MUXMODE = 0x5):

- CONTROL_CORE_PAD0_UART2_RTS_PAD1_UART2_CTS through CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX to map hw_dbg16 through hw_dbg19 signals on the uart2_rts – uart2_tx pads, respectively
- CONTROL_CORE_PAD0_MCSPI2_CLK_PAD1_MCSPI2_SIMO[31:16] to map the hw_dbg20 signal on the mcspi2_simo pad
- CONTROL_CORE_PAD0_MCSPI2_SOMI_PAD1_MCSPI2_CS0[15:0] to map the hw_dbg21 signal on the mcspi2_somi pad
- CONTROL_CORE_PAD0_GPIO6_184_PAD1_GPIO6_185 through CONTROL_CORE_PAD0_GPIO6_186_PAD1_GPIO6_187 to map hw_dbg22 through hw_dbg25 signals on the gpio6_184 – gpio6_187 pads, respectively
- CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_TIMER11_PWM_EVT[31:16] to map the hw_dbg26 signal on the timer11_pwm_evt pad
- CONTROL_CORE_PAD0_TIMER8_PWM_EVT_PAD1_I2C3_SCL to map the hw_dbg27signal on the timer8_pwm_evt pad

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- CONTROL_CORE_PAD0_UART5_RX_PAD1_UART5_TX through CONTROL_CORE_PAD0_UART5_CTS_PAD1_UART5_RTS to map hw_dbg28 through hw_dbg31 signals on the uart5_rx – uart5_rts pads, respectively

For more information, see Table 18-9.

18.4.11.4.2 Observability Signals Muxed on Pads in the WKUP Power Domain

To map the hw_wkdbg0 through hw_wkdbg15 signals to their associated external device pads in the WKUP power domain, set the MUXMODE bit field to 0x5 in the following CTRL_MODULE_WKUP_PAD registers:

- CONTROL_WKUP_PAD0_LLIA_WAKEREQIN_PAD1_LLIB_WAKEREQIN to map the hw_wkdbg14 and hw_wkdbg13 signals on the llia_wakereqin and llib_wakereqin pads, respectively.
- CONTROL_WKUP_PAD0_DRM_EMU0_PAD1_DRM_EMU1 to map the hw_wkdbg6 and hw_wkdbg7 signals on the drm_emu0 and drm_emu1 pads, respectively.
- CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK1_OUT to map the hw_wkdbg9 and hw_wkdbg5 signals on the fref_clk0_out and fref_clk1_out pads, respectively.
- CONTROL_WKUP_PAD0_FREF_CLK2_OUT_PAD1_FREF_CLK2_REQ to map the hw_wkdbg10 and hw_wkdbg11 signals on the fref_clk2_out and fref_clk2_req pads, respectively.
- CONTROL_WKUP_PAD0_FREF_CLK1_REQ_PAD1_SYS_NRESPWRON[15:0] to map the hw_wkdbg12 signal on the fref_clk1_req pad.
- CONTROL_WKUP_PAD0_SYS_NRESWARM_PAD1_SYS_PWR_REQ[31:16] to map the hw_wkdbg15 signal on the sys_pwr_req pad.
- CONTROL_WKUP_PAD0_SYS_BOOT0_PAD1_SYS_BOOT1 through CONTROL_WKUP_PAD0_SYS_BOOT4_PAD1_SYS_BOOT5 to map the hw_wkdbg0 – hw_wkdbg4 and hw_wkdbg8 signals on the sys_boot0 – sys_boot5 pads, respectively.

For more information, see Table 18-8.

18.4.11.5 Observability Signals Sourced at Module Level

Observable signals coming from within different device subsystems are mapped to general core control and general wakeup control observability inputs. Additional multiplexing is also implemented inside some of the observable modules (see Figure 18-16).

18.4.11.5.1 MPU Subsystem Observable Signals

Table 18-23 through Table 18-38 list the MPU subsystem observable signals available in 16 functional multiplexing modes. The mode is selected at the general core control module level by programming the CONTROL_DEBOBS_MMR_MPU[3:0] SELECT bit field.

Table 18-23. Observability Signals Multiplexing at MPU Subsystem Level – Mode 0

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0000			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:27]	IRQ[159:155]	hwobs_debug_mpu_31 down to hwobs_debug_mpu_27 correspond to MPU subsystem interrupt requests on lines MPU_IRQ_159 down to MPU_IRQ_155.	–
hwobs_debug_mpu_[26:9]	Reserved	–	–
hwobs_debug_mpu_8	mpussresetreq	WD_TIMER_MPU reset request to PRCM.	–
hwobs_debug_mpu_7	Reserved	–	–
hwobs_debug_mpu_6	PIDPLLTENABLEDIV	–	–

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Table 18-23. Observability Signals Multiplexing at MPU Subsystem Level – Mode 0 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0000			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_5	DPLLPhaseLock	Module in phase lock condition	–
hwobs_debug_mpu_4	DPLLInitZ	–	–
hwobs_debug_mpu_3	DPLLFreqLock	Module in freqlock condition	–
hwobs_debug_mpu_2	PIDPLLIDLE	Observes PLL to Idle mode setting. Sets CLKOUT to the bypass mode clock as selected by ULOWCLKEN.	–
hwobs_debug_mpu_1	PIDPLLTENABLE		–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

Table 18-24. Observability Signals Multiplexing at MPU Subsystem Level – Mode 1

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0001			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	Reserved	–	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

Table 18-25. Observability Signals Multiplexing at MPU Subsystem Level – Mode 2

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0010			
CTRL_MODULE_CORE Observability Inputs tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_20	EDBGRQ[1]	–	–
hwobs_debug_mpu_19	EDBGRQ[0]	–	–
hwobs_debug_mpu_18	DBGACK[1]	Asserted when either CPU0 or CPU1 enters debug state	–
hwobs_debug_mpu_17	DBGACK[0]	Asserted when either CPU0 or CPU1 enters debug state	–
hwobs_debug_mpu_[16:1]	Reserved	–	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

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Table 18-26. Observability Signals Multiplexing at MPU Subsystem Level – Mode 3

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0011			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	IRQ[30:0]	hwobs_debug_mpu_31 down to hwobs_debug_mpu_1 correspond to MPU subsystem interrupt requests on line :MPU_IRQ_30 down to MPU_IRQ_0.	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

Table 18-27. Observability Signals Multiplexing at MPU Subsystem Level – Mode 4

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0100			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	IRQ[61:31]	hwobs_debug_mpu_31 down to hwobs_debug_mpu_1 correspond to MPU subsystem interrupt requests on line :MPU_IRQ_61 down to MPU_IRQ_31.	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

Table 18-28. Observability Signals Multiplexing at MPU Subsystem Level – Mode 5

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0101			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	IRQ[92:62]	hwobs_debug_mpu_31 down to hwobs_debug_mpu_1 correspond to MPU subsystem interrupt requests on line :MPU_IRQ_92 down to MPU_IRQ_62.	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

Table 18-29. Observability Signals Multiplexing at MPU Subsystem Level – Mode 6

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0110			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	IRQ[123:93]	hwobs_debug_mpu_31 down to hwobs_debug_mpu_1 correspond to MPU subsystem interrupt requests on line :MPU_IRQ_123 down to MPU_IRQ_93.	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

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Table 18-30. Observability Signals Multiplexing at MPU Subsystem Level – Mode 7

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b0111			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	IRQ[154:124]	hwobs_debug_mpu_31 down to hwobs_debug_mpu_1 correspond to MPU subsystem interrupt requests on line :MPU_IRQ_154 down to MPU_IRQ_124.	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

Table 18-31. Observability Signals Multiplexing at MPU Subsystem Level – Mode 8

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1000			
CTRL_MODULE_CORE observability inputs tied to signals inside MPU subsystem	**MPU subsystem observable signals mapped to CTRL_MODULE_CORE observability inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	ma_hwdbgout[30:0]	–	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

Table 18-32. Observability Signals Multiplexing at MPU Subsystem Level – Mode 9

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1001			
CTRL_MODULE_CORE observability inputs tied to signals inside MPU subsystem	**MPU subsystem observable signals mapped to CTRL_MODULE_CORE observability inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	ma_hwdbgout[61:31]	–	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

Table 18-33. Observability Signals Multiplexing at MPU Subsystem Level – Mode 10

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1010			
CTRL_MODULE_CORE observability inputs tied to signals inside MPU subsystem	**MPU subsystem observable signals mapped to CTRL_MODULE_CORE observability inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	ma_hwdbgout[92:62]	–	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

Table 18-34. Observability Signals Multiplexing at MPU Subsystem Level – Mode 11

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1011			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:1]	Reserved	–	–
hwobs_debug_mpu_0	clk_mpu	MPU system clock	–

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Table 18-35. Observability Signals Multiplexing at MPU Subsystem Level – Mode 12

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1100			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_31	cpu0_emupwr_fsm_state[0]	Bit 0 of cpu0_emupwr_fsm_state signal. For more details, see the bits cpu0_emupwr_fsm_state[4:1] bits in Table 18-36.	–
hwobs_debug_mpu_[30:29]	cpu0_emupwr_ackfsm_state[1:0]	–	0x00 = INHIBACK 0x01 = ACKOFF 0x10 = BOTHACK 0x11 = FORCEACKSTATE
hwobs_debug_mpu_28	cpu0_emu_pwrst	–	'1' when PD is ON.
hwobs_debug_mpu_27	cpu0_emu_clken	–	'1' when clock is requested.
hwobs_debug_mpu_26	cpu0_inhibitsleep	–	'1' when a cpu1_inhibitsleep command is applied.
hwobs_debug_mpu_25	cpu0_forceactive	–	'1' when a cpu1_forceactive command is applied.
hwobs_debug_mpu_[24:23]	cpu0_l1_membankst[1:0]	–	0x00 = MEM_OFF 0x01 = MEM_RET 0x11 = MEM_ON
hwobs_debug_mpu_[22:21]	cpu0_powrst[1:0]	–	0x00 = PD_OFF 0x01 = PD_RET 0x10 = PD_ON-INACTIVE 0x11 = PD_ON-ACTIVE
hwobs_debug_mpu_20	cpu0_rst_n	–	'0' when reset is active.
hwobs_debug_mpu_19	cpu0_pwron_rst_n	–	'0' when reset is active.
hwobs_debug_mpu_18	cpu0_ifsm_init_wait	–	'1' when initiator is stalled.
hwobs_debug_mpu_17	cpu0_ifsm_module_mwakeup	–	'1' when Mwakeup is active.
hwobs_debug_mpu_16	cpu0_ifsm_mstandby	–	'1' when Inititator is in Standby.
hwobs_debug_mpu_[15:13]	cpu0_cmfsm_state[2:0]	–	0x000 = INACTIVE 0x001 = INACT2ACT 0x011 = ACTIVE 0x101 = ACT2INACT2 0x111 = ACT2INACT1
hwobs_debug_mpu_12	cpu0_cmfsm_domain_is_on	–	'1' when PD is ON.
hwobs_debug_mpu_11	cpu0_domain_wakeup_ack	–	'1' when domain_wakeup is acknowledged.
hwobs_debug_mpu_10	cpu0_domain_wakeup	–	'1' when domain wakeup event is pending.
hwobs_debug_mpu_9	cpu0_pwr_ret	–	'1' when RFF are retained.
hwobs_debug_mpu_8	cpu0_pgoodout_hg	–	'1' when Mercury pscon chain is ON.
hwobs_debug_mpu_7	cpu0_pgoodout_or	–	'1' when 50x pscon chain is ON.
hwobs_debug_mpu_6	cpu0_pmfsm_done	–	'1' when pscon update is done.

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Table 18-35. Observability Signals Multiplexing at MPU Subsystem Level – Mode 12 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1100			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[5:1]	cpu0_pmfsm_state[4:0]	–	0x00000 = RESET 0x00001 = CHANGEMEM 0x00010 = ONSTATE 0x00011 = STATEUPDATE 0x00100 = INACTIVE 0x00101 = ON2INACT 0x00110 = INACT2ON 0x00111 = ON2OFF 0x01000 = ON2RETL 0x01001 = ON2RETH 0x01010 = OFFSTATE 0x01011 = RETL, 0x01100 = RETH 0x01101 = OFF2ON 0x01110 = RETL2ON 0x01111 = RETH2ON 0x10000 = OFF2ONISO 0x10001 = RETL2ONISO 0x10010 = RETH2ONISO 0x10011 = OFF2ONNOISO 0x10100 = RETL2ONNOISO 0x10101 = RETH2ONNOISO 0x10110 = OFF2ONRST 0x10111 = RETL2ONRST 0x11000 = RETH2ONRST 0x11001 = INACTIVE2ON 0x11010 = INACTIVE2ONISO 0x11011 = INACTIVE2ONNOISO 0x11100 = INACTIVE2ONRST 0x11101 = UPDATE2OFF 0x11110 = UPDATE2RETL 0x11111 = UPDATE2RETH
hwobs_debug_mpu_0	prcmmpuclk	–	Ungated PRCM_MPU clock to drive PSCON.

Table 18-36. Observability Signals Multiplexing at MPU Subsystem Level – Mode 13

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1101			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_31	cpu1_ifsm_mstandby	–	'1' when Inititator is in Standby.
hwobs_debug_mpu_[30:28]	cpu1_cmfsm_state[2:0]	–	0x000 = INACTIVE 0x001 = INACT2ACT 0x011 = ACTIVE 0x101 = ACT2INACT2 0x111 = ACT2INACT1
hwobs_debug_mpu_27	cpu1_cmfsm_domain_is_on	–	'1' when PD is ON.
hwobs_debug_mpu_26	cpu1_domain_wakeup_ack	–	'1' when domain_wakeup is acknowledged.
hwobs_debug_mpu_25	cpu1_domain_wakeup	–	'1' when domain wakeup event is pending.
hwobs_debug_mpu_24	cpu1_pwr_ret	–	'1' when RFF are retained.
hwobs_debug_mpu_23	cpu1_pgoodout_hg	–	'1' when Mercury pscon chain is ON.

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Table 18-36. Observability Signals Multiplexing at MPU Subsystem Level – Mode 13 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1101			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_22	cpu1_pgoodout_or	–	'1' when 50x pscon chain is ON.
hwobs_debug_mpu_21	cpu1_pmfsm_done	–	'1' when pscon update is done.
hwobs_debug_mpu_[20:16]	cpu1_pmfsm_state[4:0]	–	0x00000 = RESET 0x00001 = CHANGEMEM 0x00010 = ONSTATE 0x00011 = STATEUPDATE 0x00100 = INACTIVE 0x00101 = ON2INACT 0x00110 = INACT2ON 0x00111 = ON2OFF 0x01000 = ON2RETL 0x01001 = ON2RETH 0x01010 = OFFSTATE 0x01011 = RETL 0x01100 = RETH 0x01101 = OFF2ON 0x01110 = RETL2ON 0x01111 = RETH2ON 0x10000 = OFF2ONISO 0x10001 = RETL2ONISO 0x10010 = RETH2ONISO 0x10011 = OFF2ONNOISO 0x10100 = RETL2ONNOISO 0x10101 = RETH2ONNOISO 0x10110 = OFF2ONRST 0x10111 = RETL2ONRST 0x11000 = RETH2ONRST 0x11001 = INACTIVE2ON 0x11010 = INACTIVE2ONISO 0x11011 = INACTIVE2ONNOISO 0x11100 = INACTIVE2ONRST 0x11101 = UPDATE2OFF 0x11110 = UPDATE2RETL 0x11111 = UPDATE2RETH
hwobs_debug_mpu_15	mpu_power_ok	–	'1' when MPU PD is ON.
hwobs_debug_mpu_14	vdd_mpu_m_ok	–	'1' when MPU logic voltage is ON.
hwobs_debug_mpu_13	vdd_mpu_l_ok	–	'1' when MPU memory voltage is ON.
hwobs_debug_mpu_12	prm_idle	–	'1' when LPRM is in Idle.
hwobs_debug_mpu_[11:10]	mpu_lp_allowed[1:0]	–	0x00 = PD_OFF 0x01 = PD_RET 0x10 = PD_ON-INACTIVE 0x11 = PD_ON-ACTIVE
hwobs_debug_mpu_[9:7]	cpu0_emuclk_fsm_state[2:0]	–	0x000 = NORMAL 0x001 = TOSLEEPD 0x010 = FORCEON 0x101 = SLEEP2NORMAL 0x111 = SLEEPDESIREDSTATE
hwobs_debug_mpu_[6:5]	cpu0_emuclk_ackfsm_state[1:0]	–	0x00 = INHIBACK 0x01 = ACKOFF 0x10 = BOTHACK 0x11 = FORCEACKSTATE

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Table 18-36. Observability Signals Multiplexing at MPU Subsystem Level – Mode 13 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1101			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[4:1]	cpu0_emupwr_fsm_state[4:1]	–	0x00000 = NORMAL 0x00001 = SLEEPDESIREDSTATE 0x00010 = FORCEON 0x00011 = OFF2EMUON 0x00100 = RETL2EMUON 0x00101 = RETH2EMUON 0x00110 = OFF2EMUONISO 0x00111 = RETL2EMUONISO 0x01000 = RETH2EMUONISO 0x01001 = EMUON2OFF 0x01010 = EMUON2RETL 0x01011 = EMUON2RETH 0x01100 = OFF2EMUONNOISO 0x01101 = RETL2EMUONNOISO 0x01110 = RETH2EMUONNOISO 0x01111 = OFF2EMUONRST 0x10000 = RETL2EMUONRST 0x10001 = RETH2EMUONRST 0x10010 = EMUON2ONINACT
hwobs_debug_mpu_0	prcmmpuclk	–	Ungated PRCM_MPU clock to drive PSCON.

Table 18-37. Observability Signals Multiplexing at MPU Subsystem Level – Mode 14

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1110			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:25]	Reserved	–	–
hwobs_debug_mpu_[24:22]	cpu1_emuclk_fsm_state[2:0]		0x000 = NORMAL 0x001 = TOSLEEPD 0x010 = FORCEON 0x101 = SLEEP2NORMAL 0x111 = SLEEPDESIREDSTATE
hwobs_debug_mpu_[21:20]	cpu1_emuclk_ackfsm_state[1:0]	–	0x00 = INHIBACK 0x01 = ACKOFF 0x10 = BOTHACK 0x11 = FORCEACKSTATE

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Table 18-37. Observability Signals Multiplexing at MPU Subsystem Level – Mode 14 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1110			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[19:15]	cpu1_emupwr_fsm_state[4:0]	–	0x00000 = NORMAL 0x00001 = SLEEPDESIREDSTATE 0x00010 = FORCEON 0x00011 = OFF2EMUON 0x00100 = RETL2EMUON 0x00101 = RETH2EMUON 0x00110 = OFF2EMUONISO 0x00111 = RETL2EMUONISO 0x01000 = RETH2EMUONISO 0x01001 = EMUON2OFF 0x01010 = EMUON2RETL 0x01011 = EMUON2RETH 0x01100 = OFF2EMUONNOISO 0x01101 = RETL2EMUONNOISO 0x01110 = RETH2EMUONNOISO 0x01111 = OFF2EMUONRST 0x10000 = RETL2EMUONRST 0x10001 = RETH2EMUONRST 0x10010 = EMUON2ONINACT
hwobs_debug_mpu_[14:13]	cpu1_emupwr_ackfsm_state[1:0]	–	0x00 = INHIBACK 0x01 = ACKOFF 0x10 = BOTHACK 0x11 = FORCEACKSTATE
hwobs_debug_mpu_12	cpu1_emu_pwrst	–	'1' when PD is ON.
hwobs_debug_mpu_11	cpu1_emu_clken	–	'1' when clock is requested.
hwobs_debug_mpu_10	cpu1_inhibitsleep	–	'1' when a cpu1_inhibitsleep command is applied.
hwobs_debug_mpu_9	cpu1_forceactive	–	'1' when a cpu1_forceactive command is applied.
hwobs_debug_mpu_[8:7]	cpu1_l1_membankst[1:0]	–	0x00 = MEM_OFF 0x01 = MEM_RET 0x11 = MEM_ON.
hwobs_debug_mpu_[6:5]	cpu1_powrst (1 downto 0)	–	0x00 = PD_OFF 0x01 = PD_RET 0x10 = PD_ON-INACTIVE 0x11 = PD_ON-ACTIVE.
hwobs_debug_mpu_4	cpu1_rst_n	–	'0' when reset is active.
hwobs_debug_mpu_3	cpu1_pwron_rst_n	–	'0' when reset is active.
hwobs_debug_mpu_2	cpu1_ifsm_init_wait	–	'1' when initiator is stalled.
hwobs_debug_mpu_1	cpu1_ifsm_module_mwakeup	–	'1' when Mwakeup is active.
hwobs_debug_mpu_0	prcmmpuclk	–	Ungated PRCM_MPU clock to drive PSCON.

Table 18-38. Observability Signals Multiplexing at MPU Subsystem Level – Mode 15

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1111			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[31:29]	Reserved	–	–

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Table 18-38. Observability Signals Multiplexing at MPU Subsystem Level – Mode 15 (continued)

CONTROL_DEBOBS_MMR_MPU[3:0] SELECT = 0b1111			
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside MPU Subsystem	**MPU Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_mpu_[28:27]	POEMUBLOCKRESET[1:0]	Block local (CPU0 and/or CPU1) reset from taking place	–
hwobs_debug_mpu_[26:25]	POEMURELEASEFROMWIR[1:0]	Release from Reset	–
hwobs_debug_mpu_[24:23]	POEMUWAITINRESET[1:0]	Wait in Reset	–
hwobs_debug_mpu_[22:21]	POEMUASSERTNRESET[1:0]	Assert Reset: This command causes the reset manager to force a local reset to a CPU. Since the rest of the system is not getting reset, the debugger must ensure there is no outstanding transaction from the CPU that is getting a reset.	–
hwobs_debug_mpu_[20:19]	Reserved	–	–
hwobs_debug_mpu_18	PIPRESETN	Debug Reset	–
hwobs_debug_mpu_17	PIATRESETN	Debug Reset	–
hwobs_debug_mpu_16	PIDBGOCPCLK	Debug Clock	–
hwobs_debug_mpu_15	Reserved	–	–
hwobs_debug_mpu_[14:13]	PIEMUCOREPOWERED[1:0]	Power–Down–Desired	–
hwobs_debug_mpu_[12:11]	PIEMUDOMAINCLOCKED[1:0]	Local CPU clock and power status.	–
hwobs_debug_mpu_[10:9]	PIEMUCLKDOWNDESIRED[1:0]	Local CPU clock and power status.	–
hwobs_debug_mpu_[8:7]	PIEMUDOMAINPOWERED[1:0]	Indicates that the domain would power down if it was not for DAP_PC keeping the domain powered	–
hwobs_debug_mpu_[6:5]	PIEMUPRWDWNDESIRED[1:0]	Power-Down-Desired	–
hwobs_debug_mpu_[4:3]	PIEMUFORCEACTIVEACK[1:0]	Force CPU power domain on and CPU clock to be running. If CPU power domain was already on and running, prevent it from power down. If it was off, initiates a wakeup sequence to power it up.	–
hwobs_debug_mpu_[2:1]	PIEMUINHIBITSLEEPACK[1:0]	Inhibit CPU from power down.	–
hwobs_debug_mpu_0	prcmmpuclk	–	–

18.4.11.5.2 IVA Subsystem Observable Signals

Table 18-39 lists the full set of 13 IVA observable signals from inside the IVA subsystem. No observability signal multiplexing is implemented at the IVA level. POHWDBGOUT[31:0] outputs are internal signals exported at IVA boundary to provide support during platform debug. They are enabled when PIHWDBGEN is high. They are always low when PIHWDBGEN is low

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Table 18-39. Observability Signals at IVA Subsystem Level

CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside IVA Subsystem	IVA Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_debug_ivahd_[31:13]	unused	General control module IVA inputs tied to low	Tied to low
hwobs_debug_ivahd_12	MAILBOX_poidleack[1]	Mailbox idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_11	IVAHD_INTC_poidleack[1]	IVA local interconnect idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_10	SMSET_poidleack[1]	SMSET idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_9	MSGIF_poidleack[1]	MSGIF idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_8	ECD3_poidleack[1]	ECD3 idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_7	MC3_poidleack[1]	MC3 idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_6	IPE3_poidleack[1]	iPE3 idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_5	CALC3_poidleack[1]	CALC3 idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_4	ILF3_poidleack[1]	iLF3 idle acknowledge s (idle domain 0)	–
hwobs_debug_ivahd_3	IME3_poidleack[1]	iME3 idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_2	VDMA_poidleack[1]	vDMA idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_1	ICONT2_poidleack[1]	ICONT2 idle acknowledge (idle domain 0)	–
hwobs_debug_ivahd_0	ICONT1_poidleack[1]	ICONT1 idle acknowledge (idle domain 0)	–

18.4.11.5.3 Display Subsystem Observable Signals

The display subsystem observable signals described in Table 18-40 are directly mapped to the display subsystem observability inputs of the CTRL_MODULE_CORE module, and no additional multiplexing is performed inside the display subsystem wrapper.

Table 18-40. Observability Signals at Display Subsystem Level

CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside Display Subsystem	Display Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_dsshdmiphypwrcmdtxon	HDMI_PHYPWRCMD_TXON	Command for TX ON	–
hwobs_dsshdmiphypwrcmdoff	HDMI_PHYPWRCMD_OFF	Command to go off state	
hwobs_dsshdmiphypwrack	HDMI_PHYPWRACK	Acknowledge	
hwobs_dsshdmihpd	HDMI_HPD	Hot plug detect	

18.4.11.5.4 DSP Subsystem Observable Signals

Table 18-41 through Table 18-47 show DSP subsystem observable signals available in sixteen multiplexing modes. The mode is selected at the general control module level through writing in the bit field DSPSS_MMU_GPR[3:0] HWDEBUG_MUX.

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The DSPSS.DSPSS_MMU_GPR register provides mux control for hardware observability signals exported at the DSPSS boundary to the general control module. Interrupts, DMA requests, and other events can be seen on the PO_HW_DBG_OUT bus. The DSPSS.DSPSS_MMU_GPR register provides mux controls for selecting the appropriate 32-bit value to be output on the PO_HW_DBG_OUT signal bus. The mux values and associated signals that can be observed on the PO_HW_DBG_OUT bus are described in Chapter 20, *Memory Management Units*. Setting the DSPSS.DSPSS_MMU_GPR[15] FORCE_IDLE_REQ bit initiates IDLE request/acknowledgment protocol with various blocks; the acknowledge information can be observed when HWDEBUG_MUX = 4'b1110.

All interrupts into DSPSS can be observed by setting the DSPSS.DSPSS_MMU_GPR[3:0] HWDEBUG_MUX bit field to 0x6, 0x7, 0x8, and 0x9. All interrupts to the INTC, which includes external and internal interrupts, can be seen by setting the HWDEBUG_MUX values to 0x2, 0x3, 0x4, and 0x5. DMA requests can be seen when the HWDEBUG_MUX values are set to 0xA and 0xB.

DPLL_IVA and the associated HSDIVIDER values can be seen by values of 0x0, the default reset value. DSPSS raw CD0 clock is sent out without any division. Other clocks are divided by 32.

The DSPSS.DSPSS_MMU_GPR[15] FORCE_IDLE_REQ bit must be used only for observability purposes, not in functional mode. When set, the FORCE_IDLE_REQ bit causes IDLE requests to be sent to various components inside the DSPSS, and idle acknowledgment is displayed when the value of the HWDEBUG_MUX[3:0] bit field is 4'b1110; the signals listed can then be checked to determine which component is not idle.

NOTE: Once this feature is used, FORCE_IDLE_REQ must be set to 0 before continuing the observability process.

Table 18-41. Observability Signals Multiplexing at DSP Subsystem Level – Mode 0

DSPSS_MMU_GPR[3:0] HWDEBUG_MUX = 0x0				
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside DSP Subsystem	**DSP Subsystem Module/Group**	**DSP Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_dsp_[31:24]		Reserved		
hwobs_debug_dsp_23		sysctrl_reset_reset_wait_tr	Release reset signal from SYSC to clock_reset module	
hwobs_debug_dsp_22		dspss_lreset_req	Emulation reset request from ECM	
hwobs_debug_dsp_21		PI_GL_RET_RESET_NA	Resets retention logic inside DSP subsystem	Active low from PRCM
hwobs_debug_dsp_20		PI_GL_DSPS_RESET_NA	Software reset to DSP core	Active low from PRCM
hwobs_debug_dsp_19		PI_GL_WGN_RESET_NA	Reset of the always-on domain of WUGEN	Active low from PRCM
hwobs_debug_dsp_18		PI_GL_SYS_RESET_NA	Reset at DSP system level	Active low from PRCM
hwobs_debug_dsp_17		PI_GL_PWR_RESEST_NA	Global DSP subsystem POR	Active low from PRCM
hwobs_debug_dsp_16	RESET	gl_lrst_n	DSP RESET from clock_reset to CORE	–
hwobs_debug_dsp_15		Reserved	–	–
hwobs_debug_dsp_14		DPLL_CLKOUT		
hwobs_debug_dsp_13		DPLL_BYPASSACK		
hwobs_debug_dsp_12		DPLL_IDLE		
hwobs_debug_dsp_11		DPLL_TENABLEDIV		
hwobs_debug_dsp_10		DPLL_TENABLE		
hwobs_debug_dsp_9		PHASELOCK	PLL in phase lock condition	–
hwobs_debug_dsp_8		TINITZ	Lock initialization	–
hwobs_debug_dsp_7	DPLL	FREQLOCK	Signal indicating that DPLL has locked	Active high to PRCM

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Table 18-41. Observability Signals Multiplexing at DSP Subsystem Level – Mode 0 (continued)

DSPSS_MMU_GPR[3:0] HWDEBUG_MUX = 0x0				
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside DSP Subsystem	**DSP Subsystem Module/Group**	**DSP Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_dsp_6		Reserved	–	–
hwobs_debug_dsp_5		redge_to_core_div32	L3 Redge signal divided by 32	–
hwobs_debug_dsp_4		cd1_clk_div32	CD1 free clock divided by 32	(Not active when POR is active)
hwobs_debug_dsp_3		cd0_mod_clk_free_div32	CD0 pure free clock divided by 32	–
hwobs_debug_dsp_2	clock_reset	cd0_mod_clk_free	CD0 raw clock	–
hwobs_debug_dsp_1		HSD_CLKOUT5	Raw clock for IVA	–
hwobs_debug_dsp_0	HSDIVIDER	HSD_CLKOUT4	Raw CD0 clock from HSDIVIDER	–

Table 18-42. Observability Signals Multiplexing at DSP Subsystem Level – Mode 1

DSPSS_MMU_GPR[3:0] HWDEBUG_MUX = 0x1				
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside DSP Subsystem	**DSP Subsystem Module/Group**	**DSP Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_dsp_[31:11]		Reserved	–	
hwobs_debug_dsp_[10:8]		po_l2_unicache_master_mcmd_tr	L3 Master CMD from SmartMSS L2	–
hwobs_debug_dsp_[7:6]		po_l1_unicache_sllave_n_rd_miss_tr[1] po_l1_unicache_slave_n_wr_accept_tr[1]	L1 cache miss signals for DMC port ([0]:Rd, [1]:Write)	–
hwobs_debug_dsp_5	SmartMSS	po_l1_unicache_sllave_n_rd_miss_tr[0]	L1 cache read miss for PMC port	–
hwobs_debug_dsp_4		cpu_to_dmc_stall	EXE pipe stall signal from CPU	–
hwobs_debug_dsp_3	CPU	cpu_to_pmc_dispatch_stall	PF pipe stall signal from CPU	–
hwobs_debug_dsp_2		dmc_to_cpu_stall	CPU stall signal from DMC	–
hwobs_debug_dsp_1		dmc_to_cache_req_tr	DMC request signal to Unicache	–
hwobs_debug_dsp_0	dsp_intf	pmc_to_cache_req_tr	PMC request signal to Unicache	–

Table 18-43. Observability Signals Multiplexing at DSP Subsystem Level – Mode 2 through Mode 11

DSPSS_MMU_GPR[3:0] HWDEBUG_MUX Value	**CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside DSP Subsystem**	**DSP Subsystem Module/Group**	**DSP Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
0x2	hwobs_debug_dsp_[31:0]	–	Reserved	–	–
0x3	hwobs_debug_dsp_[31:0]	–	Reserved	–	–
0x4	hwobs_debug_dsp_[31:0]	–	Reserved	–	–
0x5	hwobs_debug_dsp_[31:0]	–	Reserved	–	–
0x6	hwobs_debug_dsp_[31:0]	PI	PI_GL_IRQ_NA[31:0]	Level interrupt input signal/ asynchronous to WUGEN clk	Active low.

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Table 18-43. Observability Signals Multiplexing at DSP Subsystem Level – Mode 2 through Mode 11 (continued)

DSPSS_MMU_GPR[3:0] HWDEBUG_MUX Value	CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside DSP Subsystem	DSP Subsystem Module/Group	DSP Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	Logical Value Meaning
0x7	hwobs_debug_dsp_[31:0]	PI	PI_GL_IRQ_NA[63:32]	Level interrupt input signal/ asynchronous to WUGEN clk	Active low.
0x8	hwobs_debug_dsp_[31:0]	PI	PI_GL_IRQ_NA[95:64]	Level interrupt input signal	Avtive low.
0x9	hwobs_debug_dsp_[31:0]	PI	PI_GL_IRQ_NA[127:96]	Level interrupt input signal	–
0xA	hwobs_debug_dsp_[31:0]	DMA	PI_GL_DMARQ_NA[31:0]	DMA request event input signal	–
0xB	hwobs_debug_dsp_[31:0]	DMA	PI_GL_DMARQ_NA[63:32]	DMA request event input signal	–

Table 18-44. Observability Signals Multiplexing at DSP Subsystem Level – Mode 12

DSPSS_MMU_GPR[3:0] HWDEBUG_MUX = 0xC				
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside DSP subsystem	**DSP Subsystem Module/Group**	**DSP Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_dsp_[31:6]	–	Reserved	–	–
hwobs_debug_dsp_[5:4]	PRCM	PO_WGN_SIDLEACK_TR	Idle handshake acknowledge by WKGEN	Active high signal to PRCM for L4 port
hwobs_debug_dsp_3		PI_GL_WGN_SIDLEREQ_TA	Idle handshake request with the WKGEN	Active high signal from PRCM for L4 port
hwobs_debug_dsp_2		PI_GL_DSP_MWAIT_TA	PRCM is indicating wait response to MWakeup	Active high signal from PRCM
hwobs_debug_dsp_1		PO_WGN_MWAKEUP_TA	DSP subsystem is waking up.	Active high signal to PRCM
hwobs_debug_dsp_0	PRCM	PO_DSP_MSTANDBY_TR	DSP subsystem is going into standby.	Active high signal to PRCM

Table 18-45. Observability Signals Multiplexing at DSP Subsystem Level – Mode 13

DSPSS_MMU_GPR[3:0] HWDEBUG_MUX = 0xD				
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside DSP subsystem	**DSP Subsystem Module/Group**	**DSP Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_dsp_[31:16]		Reserved		
hwobs_debug_dsp_[15:7]		sysctrl_cd1clken_tr	CD1 clock enable for each modules	–
hwobs_debug_dsp_[6:5]		sysctrl_cd0clken_tr	CD0 clock enable for each modules	–
hwobs_debug_dsp_[4:2]		edma_mstandby_tr	EDMA Mstandby	–
hwobs_debug_dsp_[1:0]	PRCM	dspss_pdstat_tr	CPU power-down state to SYSC	–

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Table 18-46. Observability Signals Multiplexing at DSP Subsystem Level – Mode 14

DSPSS_MMU_GPR[3:0] HWDEBUG_MUX = 0xE				
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside DSP Subsystem	**DSP Subsystem Module/Group**	**DSP Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_dsp_[31:22]		Reserved		
hwobs_debug_dsp_[21:12]		sisg_sys_idleack_tr	Idle ack from each module	
hwobs_debug_dsp_[11:2]		sysctrl_sys_idlereq_tr	Idle req to each module	
hwobs_debug_dsp_1		sig_wkgen_clkoffack_tr	WKGEN acknowledges clock-off request from SYS control	
hwobs_debug_dsp_0	IDLE	sysctrl_wkgenclkoffreq_tr	Clock-off request to WKGEN	

Table 18-47. Observability Signals Multiplexing at DSP Subsystem Level – Mode 15

DSPSS_MMU_GPR[3:0] HWDEBUG_MUX = 0xF				
CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside DSP Subsystem	**DSP Subsystem Module/Group**	**DSP Subsystem Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_dsp_[31:0]	–	Reserved	–	–

18.4.11.5.5 ABE Subsystem Observable Signals

The audio backend (ABE) observable signals described in Table 18-48 are directly mapped to the ABE dedicated observability inputs, hwobs_debug_abe_[31:0] of the CTRL_MODULE_CORE module, and no additional multiplexing is performed inside the ABE.

Table 18-48. Observability Signals at ABE Subsystem Level

CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside ABE Subsystem	**CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside ABE Subsystem**	**Signal Description**	**Logical Value Meaning**
hwobs_debug_abe_[31:26]	–	–	–
hwobs_debug_abe_[25:24]	OPP_DIV	OPP DIVIDER bits [1:0]	–
hwobs_debug_abe_23	AESS_to_MPU_IRQ	IRQ sent from AESS to MCU. See Chapter 13, *ABE.*	–
hwobs_debug_abe_22	AESS_to_DSPSS_IRQ	IRQ sent from AESS to DSP. See Section 5.3.7, *Interrupt Requests,* and Chapter 13, *ABE.*	–
hwobs_debug_abe_21	Reserved	–	–
hwobs_debug_abe_20	GPT_WDT_PWM_INP	PWM received from the GPTIMER or watchdog (OR)	–
hwobs_debug_abe_19	AESS_DMAREQ_ALL	(Logical OR with all DMA requests out)	High while outcoming DMA requests from audio engine have not been acknowledged by the host
hwobs_debug_abe_18	AESS_DMAREQ_PER	(Logical OR with all DMA requests coming from the peripheral)	High when incoming DMA requests from audio engine are still to be served
hwobs_debug_abe_17	AESS_IDLEPO	PO_IDLE AESS output	High when the audio engine executes a wait until an activation of the PI_WAKEUP pin is done

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Table 18-48. Observability Signals at ABE Subsystem Level (continued)

CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside ABE Subsystem	CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside ABE Subsystem	Signal Description	Logical Value Meaning
hwobs_debug_abe_[16:0]	Reserved	–	–

18.4.11.5.6 DPLL Clockview Channel Observable Signals Multiplexing

Table 18-49 describes the multiplexing of the different DPLL clock outputs for each of the three available channels, clk_view_0, clk_view_1, and clk_view_2.

The CONTROL_HWOBSDIVIDER1 and CONTROL_HWOBSDIVIDER2 registers allow the division of the frequency of these observable DPLL clock outputs.

Table 18-49. Different DPLL Observable Clock Output Signals

CTRL_MODULE_CORE Observability Inputs Tied to Signals Inside Different Module DPLLs	Different DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	DPLL CLKOUT Selection Per clk_view channel i CONTROL_CONF_CLK_SELi [3:0] MULT Value (where i = 0 to 2]
hwobs_coredpll_clkout	DPLL_TESTCLKOUT	CORE DPLL	0x0
hwobs_abedpll_clkout	PODPLLTESTCLKOUT	ABE DPLL	0x1
hwobs_perdpll_clkout	DPLL_TESTCLKOUT	PERIPH DPLL	0x2
hwobs_dsi1adpll_clkout	PODPLLTESTCLKOUT	DSI1_A DPLL	0x3
hwobs_dsi1cdpll_clkout	DPLL_TESTCLKOUT	DSI1_C DPLL	0x4
hwobs_hdmidpll_clkout	DPLL_TESTCLKOUT	HDMI DPLL	0x5
hwobs_satadpll_clkout	DPLL_TESTCLKOUT	SATA DPLL	0x6
hwobs_usbotgssdpll_clkout	DPLL_TESTCLKOUT	USBOTGSS DPLL	0x7
hwobs_usbdpll_clkout	PODPLLTESTCLKOUT	USB DPLL	0x8

18.4.11.5.7 Other CORE DPLL Observable Signals

Table 18-50 describes the mapping of CORE DPLL observability signals (other than CLKOUT) to the CTRL_MODULE_CORE DPLL observability inputs. The selection of CORE DPLL as the source of the additional DPLL signals is done at the CTRL_MODULE_CORE level by setting the MULT bit field to 0x0 inside each of the seven registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-50. Other CORE DPLL Observability Signals

CTRL_MODULE_CORE Observability Inputs Tied to CORE DPLL Observable Signals	Other CORE DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_coredpll_freqlock	COREdpll_freqlock	CORE DPLL frequency lock check	–
hwobs_coredpll_tinitz	COREdpll_tinitz	Check CORE DPLL status, lock/relock time	–
hwobs_coredpll_phaselock	COREdpll_phaselock	CORE DPLL phase lock check	–
hwobs_coredpll_tenable	COREdpll_tenable	CORE DPLL core RegM/N load enable input	–
hwobs_coredpll_tenablediv	COREdpll_tenablediv	CORE DPLL core RegM2/N2 load enable input	–
hwobs_coredpll_bypassack	COREdpll_bypassack	CORE DPLL bypass status signal	–

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Table 18-50. Other CORE DPLL Observability Signals (continued)

CTRL_MODULE_CORE Observability Inputs Tied to CORE DPLL Observable Signals	Other CORE DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_coredpll_idle	COREdpll_idle	CORE DPLL idle mode input	–

18.4.11.5.8 Other ABE DPLL Observable Signals

Table 18-51 describes the mapping of ABE DPLL observability signals (other than CLKOUT) to the CTRL_MODULE_CORE DPLL observability inputs. The selection of ABE DPLL as the source of the additional DPLL signals is done at the CTRL_MODULE_CORE level by setting the MULT bit field to 0x1 inside each of the seven registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-51. Other ABE DPLL Observability Signals

CTRL_MODULE_CORE Observability Inputs Tied to ABE DPLL Observable Signals	Other ABE DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_abedpll_freqlock	dspdpll_freqlock	ABE DPLL frequency lock check	–
hwobs_abedpll_tinitz	dspdpll_tinitz	Check ABE DPLL status, lock/relock time.	–
hwobs_abedpll_phaselock	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_abedpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_abedpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_abedpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_abedpll_idle	dspDpllPhaseLock	dspDPLL phase lock check	–

18.4.11.5.9 Other PERIPH DPLL Observable Signals

Table 18-52 describes the mapping of PERIPH DPLL observability signals (other than CLKOUT) to the CTRL_MODULE_CORE DPLL observability inputs. The selection of PERIPH DPLL as the source of the additional DPLL signals is done at the CTRL_MODULE_CORE level by setting the MULT bit field to 0x2 inside each of the seven registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-52. Other PERIPH DPLL Observability Signals

CTRL_MODULE_CORE Observability Inputs Tied to PERIPH DPLL Observable Signals	Other PERIPH DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_perdpll_freqlock	PERIPHdpll_freqlock	PERIPH DPLL frequency lock check	–
hwobs_perdpll_tinitz	PERIPHdpll_tinitz	Check PERIPH DPLL status, lock/relock time.	–
hwobs_perdpll_phaselock	PERIPHDpllPhaseLock	PERIPH DPLL phase lock check	–
hwobs_perdpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_perdpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_perdpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_perdpll_idle	PERIPHDpllPhaseLock	PERIPH DPLL phase lock check	–

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18.4.11.5.10 Other DSI1_A DPLL Observable Signals

Table 18-53 describes the mapping of DSI1_A DPLL observability signals (other than CLKOUT) to the CTRL_MODULE_CORE DPLL observability inputs. The selection of DSI1_A DPLL as the source of the additional DPLL signals is done at the CTRL_MODULE_CORE level by setting the MULT bit field to 0x3 inside each of the seven registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-53. Other DSI1_A DPLL Observability Signals

CTRL_MODULE_CORE Observability Inputs Tied to DSI1_A DPLL Observable Signals	Other DSI1_A DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_dsi1adpll_freqlock	dspdpll_freqlock	dspDPLL frequency lock check	–
hwobs_dsi1adpll_tinitz	dspdpll_tinitz	Check dspDPLL status, lock/relock time.	–
hwobs_dsi1adpll_phaselock	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1adpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1adpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1adpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1adpll_idle	dspDpllPhaseLock	dspDPLL phase lock check	–

18.4.11.5.11 Other DSI1_C DPLL Observable Signals

Table 18-54 describes the mapping of DSI1_C DPLL observability signals (other than CLKOUT) to the CTRL_MODULE_CORE DPLL observability inputs. The selection of DSI1_C DPLL as the source of the additional DPLL signals is done at the CTRL_MODULE_CORE level by setting the MULT bit field to 0x4 inside each of the seven registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-54. Other DSI1_C DPLL Observability Signals

CTRL_MODULE_CORE Observability Inputs Tied to DSI1_C DPLL Observable Signals	Other DSI1_C DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability Inputs	Signal Description	Logical Value Meaning
hwobs_dsi1cdpll_freqlock	PERIPHdpll_freqlock	PERIPH DPLL frequency lock check	–
hwobs_dsi1cdpll_tinitz	PERIPHdpll_tinitz	Check PERIPH DPLL status, lock/relock time.	–
hwobs_dsi1cdpll_phaselock	PERIPHDpllPhaseLock	PERIPH DPLL phase lock check	–
hwobs_dsi1cdpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1cdpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1cdpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_dsi1cdpll_idle	PERIPHDpllPhaseLock	PERIPH DPLL phase lock check	–

18.4.11.5.12 Other HDMI DPLL Observable Signals

Table 18-55 describes the mapping of HDMI DPLL observability signals (other than CLKOUT) to the CTRL_MODULE_CORE DPLL observability inputs. The selection of HDMI DPLL as the source of the additional DPLL signals is done at the CTRL_MODULE_CORE level by setting the MULT bit field to 0x5 inside each of the seven registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

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Table 18-55. Other HDMI DPLL Observability Signals

CTRL_MODULE_CORE Observability Inputs Tied to HDMI DPLL Observable Signals	Other HDMI DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability inputs	Signal Description	Logical Value Meaning
hwobs_hdmidpll_freqlock	PERIPHdpll_freqlock	HDMI DPLL frequency lock check	–
hwobs_hdmidpll_tinitz	PERIPHdpll_tinitz	Check HDMI DPLL status, lock / relock time	–
hwobs_hdmidpll_phaselock	PERIPHDpllPhaseLock	HDMI DPLL phase lock check	–
hwobs_hdmidpll_tenable	dspDpllPhaseLock	HDMI DPLL Core RegM/N load enable input	–
hwobs_hdmidpll_tenablediv	dspDpllPhaseLock	HDMI DPLL Core RegM/N load enable input	–
hwobs_hdmidpll_bypassack	dspDpllPhaseLock	HDMI DPLL Core RegM/N load enable input	–
hwobs_hdmidpll_idle	PERIPHDpllPhaseLock	HDMI DPLL Idle mode input	–

18.4.11.5.13 Other USBOTGSS DPLL Observable Signals

Table 18-56 describes the mapping of USBOTGSS DPLL observability signals (other than CLKOUT) to the CTRL_MODULE_CORE DPLL observability inputs. The selection of USBOTGSS DPLL as the source of the additional DPLL signals is done at the CTRL_MODULE_CORE level by setting the MULT bit field to 0x7 inside each of the seven registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-56. Other USBOTGSS DPLL Observability Signals

CTRL_MODULE_CORE Observability Inputs Tied to USBOTGSS DPLL Observable Signals	Other USBOTGSS DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability inputs	Signal Description	Logical Value Meaning
hwobs_usbotgssdpll_freqlock	PERIPHdpll_freqlock	USBOTGSS DPLL frequency lock check	–
hwobs_usbotgssdpll_tinitz	PERIPHdpll_tinitz	Check USBOTGSS DPLL status, lock / relock time	–
hwobs_usbotgssdpll_phaselock	PERIPHDpllPhaseLock	USBOTGSS DPLL phase lock check	–
hwobs_usbotgssdpll_tenable	dspDpllPhaseLock	USBOTGSS DPLL Core RegM/N load enable input	–
hwobs_usbotgssdpll_tenablediv	dspDpllPhaseLock	USBOTGSS DPLL Core RegM/N load enable input	–
hwobs_usbotgssdpll_bypassack	dspDpllPhaseLock	USBOTGSS DPLL Core RegM/N load enable input	–
hwobs_usbotgssdpll_idle	PERIPHDpllPhaseLock	USBOTGSS DPLL Idle mode input	–

18.4.11.5.14 Other USB DPLL Observable Signals

Table 18-57 describes the mapping of USB DPLL observability signals (other than CLKOUT) to the CTRL_MODULE_CORE DPLL observability inputs. The selection of USB DPLL as the source of the additional DPLL signals is done at CTRL_MODULE_CORE level by setting the MULTbit field to 0x8 inside each of the seven registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

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Table 18-57. Other USB DPLL Observability Signals

CTRL_MODULE_CORE Observability Inputs Tied to USB DPLL Observable Signals	Other USB DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability inputs	Signal Description	Logical Value Meaning
hwobs_usbdpll_freqlock	dspdpll_freqlock	dspDPLL frequency lock check	–
hwobs_usbdpll_tinitz	dspdpll_tinitz	check dspDPLL status, lock/relock time.	–
hwobs_usbdpll_phaselock	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_usbdpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_usbdpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_usbdpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_usbdpll_idle	dspDpllPhaseLock	dspDPLL phase lock check	–

18.4.11.5.15 Other SATA DPLL Observable Signals

Table 18-58 describes the mapping of SATA DPLL observability signals (other than CLKOUT) to the CTRL_MODULE_CORE dpll observability inputs. The selection of SATA DPLL as the source of the additional DPLL signals is done at CTRL_MODULE_CORE level by setting the MULT bit field to 0x6 inside each of the seven registers (CONTROL_CONF_DPLL_FREQLOCK_SEL through CONTROL_CONF_DPLL_IDLE_SEL).

Table 18-58. Other SATA DPLL Observability Signals

CTRL_MODULE_CORE Observability Inputs Tied to SATA DPLL Observable Signals	Other SATA DPLL Observable Signals Mapped to CTRL_MODULE_CORE Observability inputs	Signal Description	Logical Value Meaning
hwobs_satadpll_freqlock	PERIPHdpll_freqlock	SATA DPLL frequency lock check	–
hwobs_satadpll_tinitz	PERIPHdpll_tinitz	Check SATA DPLL status, lock / relock time	–
hwobs_satadpll_phaselock	PERIPHDpllPhaseLock	SATA DPLL phase lock check	–
hwobs_satadpll_tenable	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_satadpll_tenablediv	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_satadpll_bypassack	dspDpllPhaseLock	dspDPLL phase lock check	–
hwobs_satadpll_idle	PERIPHDpllPhaseLock	SATA DPLL Idle mode input	–

18.4.11.6 Cross-bar

The cross-bar is part of the device observability logic. The purpose of the cross-bar is to shuffle any input observable signal to any output observable signal. There are two identical cross-bars, one for CORE observability signals and one for WKUP observability signals. Each cross-bar has 32 inputs and 32 outputs and can be seen as a 32-to-32 multiplexer. The cross-bar resides between the CORE/WKUP multiplexing level and the gate layer before the top-level multiplexer, which selects an observable signal between the CORE and WKUP power domains.

Figure 18-17 shows the location of the cross-bar in device observability logic.

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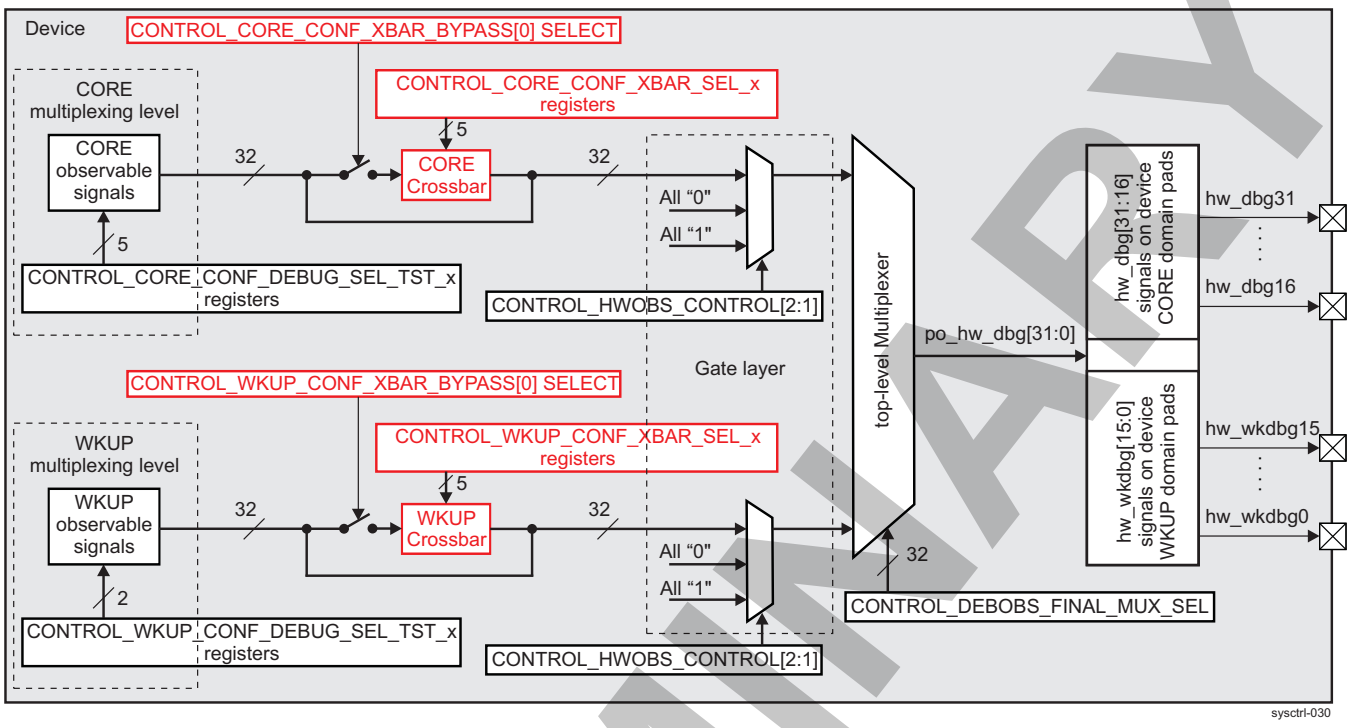
Figure 18-17. Cross-bar Location



The cross-bars in the CORE and in WKUP power domains can be bypassed by setting the CONTROL_CORE_CONF_XBAR_BYPASS[0] SELECT and CONTROL_WKUP_CONF_XBAR_BYPASS[0] SELECT bits to 0x1, respectively. By default both the cross-bars are bypassed.

Figure 18-18 represents the way in which the cross-bar works. The selection of an input signal to remap is made through the CONTROL_CORE_CONF_XBAR_SEL_x and CONTROL_WKUP_CONF_XBAR_SEL_x registers. Each of these registers has a structure described in Table 18-59. Each of the 5-bit fields (CONF_XBAR_SEL) selects one of the 32 observable input signals to be mapped on a certain cross-bar output. The number of each cross-bar output corresponds to the suffix number of each one of these 5-bit fields. For example:

- The CONTROL_CORE_CONF_XBAR_SEL_0[4:0] CONF_XBAR_SEL_0 bit field selects one of 32 observable signals to be mapped on cross-bar output 0.
- The CONTROL_CORE_CONF_XBAR_SEL_0[12:8] CONF_XBAR_SEL_1 bit field selects one of 32 observable signals to be mapped on cross-bar output 1.
- The CONTROL_CORE_CONF_XBAR_SEL_28[28:24] CONF_XBAR_SEL_31 bit field selects one of 32 observable signals to be mapped on cross-bar output 31.

The same logic is applied for cross-bar control registers in the WKUP power domain.

Table 18-60 shows all the cross-bar control registers.

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Figure 18-18. CORE/WKUP Cross-bar Functional Diagram

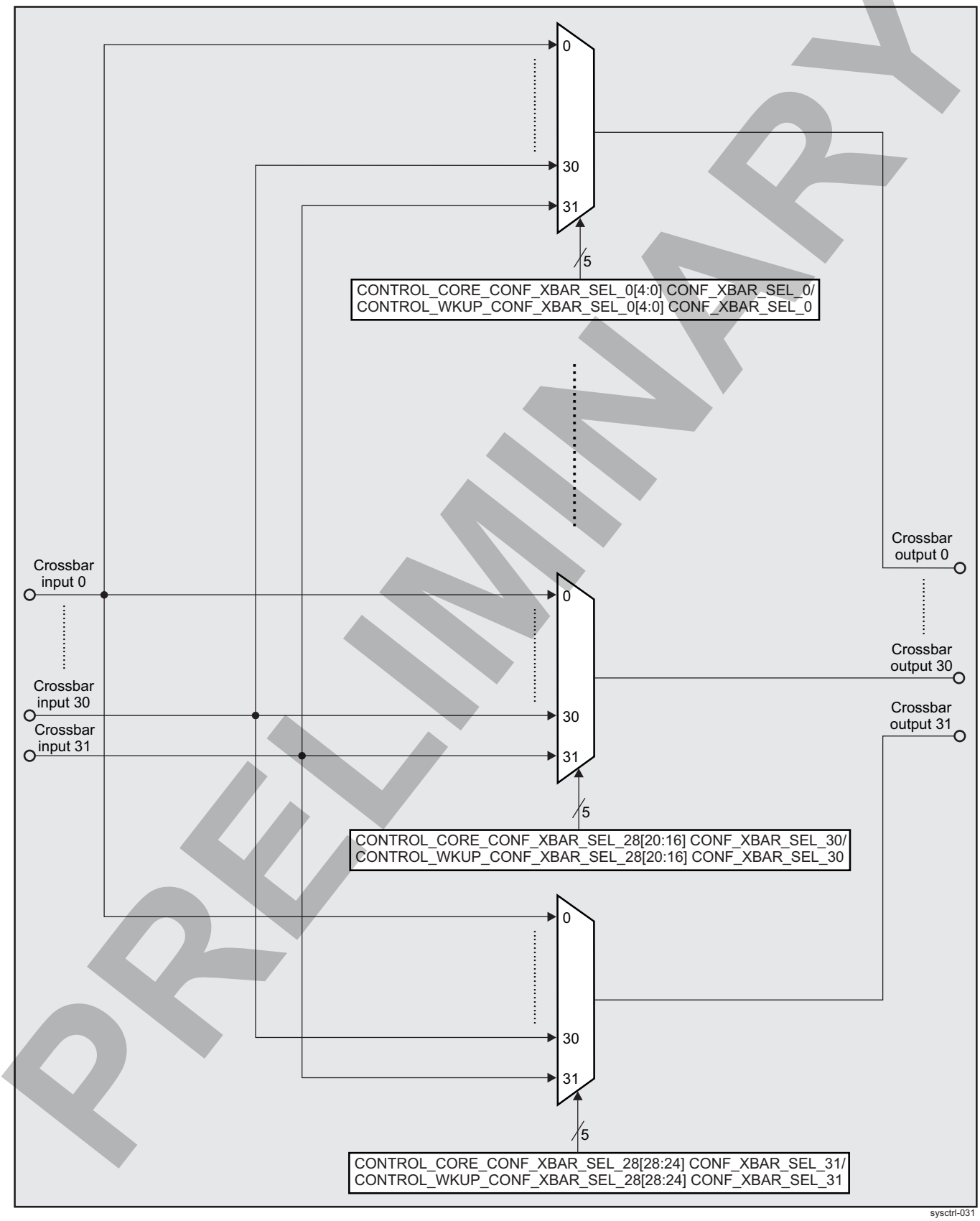

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Table 18-59. Generic Description of CONTROL_CORE_CONF_XBAR_SEL_x and CONTROL_WKUP_CONF_XBAR_SEL_x Registers (where x = 0, 4, 8, 12, 16, 20, 24, and 28)

Bits	Field Name	Description	Type	Note
31:29	RESERVED		R	
28:24	CONF_XBAR_SEL_D	Selects 1 of 32 cross-bar input signals to be mapped on cross-bar output D 0x0: Maps cross-bar input signal 0 on cross-bar output D 0x1: Maps cross-bar input signal 1 on cross-bar output D 0x-: ..... 0x1E: Maps cross-bar input signal 30 on cross-bar output D 0x1F: Maps cross-bar input signal 31 on cross-bar output D	RW	D is summarization. Its value is equal to 3, 7, 11, 15, 19, 23, 27 and 31 for the different CONTROL_CORE_CONF_XBAR_SEL_x and CONTROL_WKUP_CONF_XBAR_SEL_x registers
23:21	RESERVED		R	
20:16	CONF_XBAR_SEL_C	Selects 1 of 32 cross-bar input signals to be mapped on cross-bar output C 0x0: Maps cross-bar input signal 0 on cross-bar output C 0x1: Maps cross-bar input signal 1 on cross-bar output C 0x-: ..... 0x1E: Maps cross-bar input signal 30 on cross-bar output C 0x1F: Maps cross-bar input signal 31 on cross-bar output C	RW	C is summarization. Its value is equal to 2, 6, 10, 14, 18, 22, 26 and 30 for the different CONTROL_CORE_CONF_XBAR_SEL_x and CONTROL_WKUP_CONF_XBAR_SEL_x registers
15:13	RESERVED		R	
12:8	CONF_XBAR_SEL_B	Selects 1 of 32 cross-bar input signals to be mapped on cross-bar output B 0x0: Maps cross-bar input signal 0 on cross-bar output B 0x1: Maps cross-bar input signal 1 on cross-bar output B 0x-: ..... 0x1E: Maps cross-bar input signal 30 on cross-bar output B 0x1F: Maps cross-bar input signal 31 on cross-bar output B	RW	B is summarization. Its value is equal to 1, 5, 9, 13, 17, 21, 25 and 29 for the different CONTROL_CORE_CONF_XBAR_SEL_x and CONTROL_WKUP_CONF_XBAR_SEL_x registers
7:5	RESERVED		R	
4:0	CONF_XBAR_SEL_A	Selects 1 of 32 cross-bar input signals to be mapped on cross-bar output A 0x0: Maps cross-bar input signal 0 on cross-bar output A 0x1: Maps cross-bar input signal 1 on cross-bar output A 0x-: ..... 0x1E: Maps cross-bar input signal 30 on cross-bar output A 0x1F: Maps cross-bar input signal 31 on cross-bar output A	RW	A is summarization. Its value is equal to 0, 4, 8, 12, 16, 20, 24 and 28 for the different CONTROL_CORE_CONF_XBAR_SEL_x and CONTROL_WKUP_CONF_XBAR_SEL_x registers

Table 18-60. Cross-bar Control Registers

CORE Cross-bar	WKUP Cross-bar
CONTROL_CORE_CONF_XBAR_BYPASS	CONTROL_WKUP_CONF_XBAR_BYPASS
CONTROL_CORE_CONF_XBAR_SEL_0	CONTROL_WKUP_CONF_XBAR_SEL_0

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Table 18-60. Cross-bar Control Registers (continued)

CORE Cross-bar	WKUP Cross-bar
CONTROL_CORE_CONF_XBAR_SEL_4	CONTROL_WKUP_CONF_XBAR_SEL_4
CONTROL_CORE_CONF_XBAR_SEL_8	CONTROL_WKUP_CONF_XBAR_SEL_8
CONTROL_CORE_CONF_XBAR_SEL_12	CONTROL_WKUP_CONF_XBAR_SEL_12
CONTROL_CORE_CONF_XBAR_SEL_16	CONTROL_WKUP_CONF_XBAR_SEL_16
CONTROL_CORE_CONF_XBAR_SEL_20	CONTROL_WKUP_CONF_XBAR_SEL_20
CONTROL_CORE_CONF_XBAR_SEL_24	CONTROL_WKUP_CONF_XBAR_SEL_24
CONTROL_CORE_CONF_XBAR_SEL_28	CONTROL_WKUP_CONF_XBAR_SEL_28

18.4.12 Functional Register Description

18.4.12.1 DSP Boot Register

Table 18-61 describes the DSP boot address register.

Table 18-61. DSP Boot Address Register

Physical Address	Register Name	Description	Access
0x4A00 2304	CONTROL_DSP_BOOTADDR	DSP boot loader address register	R/W

The CONTROL_DSP_BOOTADDR register defines the physical address for the DSP boot loader and drives the DSP_BOOTADDR[31:10] signals from the control block to the DSP subsystem.

18.4.12.1.1 PBIAS Control Register

Table 18-62 describes the CONTROL_PBIAS register, which controls some settings of PBIASLITE cells for the SDCARD I/O interface.

Table 18-62. PBIAS Control Register

Physical Address	Register Name	Description	Access
0x4A00 2E00	CONTROL_PBIAS	Control settings for PBIAS cell	RW

18.4.12.2 Temperature Sensor Control Registers

Table 18-63 describes the thermal management registers of the general core control module, which control the temperature sensor, bandgap state-machine, thermal post-processing logic, temperature accumulation, and temperature time stamping features.

Table 18-63. Temperature Sensor Registers

Physical Address	Register Name	Description	Access
0x4A00 232C	CONTROL_TEMP_SENSOR_MPU	Temperature sensor control registers	R/W
0x4A00 2330	CONTROL_TEMP_SENSOR_MM		
0x4A00 2334	CONTROL_TEMP_SENSOR_CORE		
0x4A00 239C	CONTROL_BANDGAP_CUMUL_DTEMP_MPU	Temperature accumulator registers	RO
0x4A00 23A0	CONTROL_BANDGAP_CUMUL_DTEMP_MM		
0x4A00 23A4	CONTROL_BANDGAP_CUMUL_DTEMP_CORE		
0x4A00 2390	CONTROL_BANDGAP_TSHUT_MPU	Bandgap thermal shutdown threshold registers	RO
0x4A00 2394	CONTROL_BANDGAP_TSHUT_MM		
0x4A00 2398	CONTROL_BANDGAP_TSHUT_CORE		

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Table 18-63. Temperature Sensor Registers (continued)

Physical Address	Register Name	Description	Access
0x4A00 2384	CONTROL_BANDGAP_THRESHOLD_MPU	Bandgap thermal alert threshold registers	R/W
0x4A00 2388	CONTROL_BANDGAP_THRESHOLD_MM		
0x4A00 238C	CONTROL_BANDGAP_THRESHOLD_CORE		
0x4A00 23A8	CONTROL_BANDGAP_STATUS	Thermal alert and bandgap idle events status register	RO
0x4A00 2380	CONTROL_BANDGAP_MASK	Hot and cold bandgap events mask register. This register is also used to control the FIFOs and temperature accumulators.	R/W
0x4A00 23C0	CONTROL_DTEMP_MPU_0	Temperature timestamping registers	RO
0x4A00 23C4	CONTROL_DTEMP_MPU_1		
0x4A00 23C8	CONTROL_DTEMP_MPU_2		
0x4A00 23CC	CONTROL_DTEMP_MPU_3		
0x4A00 23D0	CONTROL_DTEMP_MPU_4		
0x4A00 23D4	CONTROL_DTEMP_MM_0		
0x4A00 23D8	CONTROL_DTEMP_MM_1		
0x4A00 23DC	CONTROL_DTEMP_MM_2		
0x4A00 23E0	CONTROL_DTEMP_MM_3		
0x4A00 23E4	CONTROL_DTEMP_MM_4		
0x4A00 23E8	CONTROL_DTEMP_CORE_0		
0x4A00 23EC	CONTROL_DTEMP_CORE_1		
0x4A00 23F0	CONTROL_DTEMP_CORE_2		
0x4A00 23F4	CONTROL_DTEMP_CORE_3		
0x4A00 23F8	CONTROL_DTEMP_CORE_4		

18.4.12.2.1 CSI Receiver Control Register

To enable the physical layer of the camera receiver, the programmer manipulates the bits within the CONTROL_CAMERA_RX register as described in Table 18-64.

Table 18-64. CSI Receiver Control Register

Physical Address	Register Name	Description	Access
0x4A00 2E08	CONTROL_CAMERA_RX	Module dedicated configurations	RW

18.4.12.3 Protection Status Registers

Table 18-65 lists the protection status registers.

Table 18-65. Protection Status Registers

Physical Address	Register Name	Description	Access
0x4A00 2148	CONTROL_SEC_ERR_STATUS_FUNC	Protection firewall error status register	Public (R)
0x4A00 2150	CONTROL_SEC_ERR_STATUS_DEBUG	Protection firewall error status register debug	Public (RW)

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These registers do not depend on the device type.

The CONTROL_SEC_ERR_STATUS_FUNC can be read in public mode, but cannot be written.

The CONTROL_SEC_ERR_STATUS_DEBUG register is both read and write accessible in GP devices.

These bits are cleared when the L3 and L4 firewall embedded-error log registers are cleared. All bits in these registers reflect internal events in the device related to the device protection.

On a specific event (signal rising edge), the corresponding bit is set. On a rising edge, the input signal must stay high for at least two interface clock periods to be recognized. Software must clear each bit after reviewing the events.

When a protection violation occurs, the following bits are set:

- In application mode:
  - CONTROL_SEC_ERR_STATUS_FUNC[1] = L3RAM protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[2] = GPMC protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[3] = EMIF protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[4] = IVA-HD protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[5] = Dual Cortex-M4 protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[6] = IVAHD SL2 protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[8] = SYSTEMDMA protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[10] = DISPDMA protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[13] = GPU protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[14] = DSS protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[15] = ISS protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[16] = L4_PER protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[17] = L4_CFG protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[18] = DebugSS protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[19] = AUDIOSS protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[22] = L4 wakeup protection violation
  - CONTROL_SEC_ERR_STATUS_FUNC[23] = BB2D protection violation
- In debug mode:
  - CONTROL_SEC_ERR_STATUS_DEBUG[1] = L3RAM protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[2] = GPMC protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[3] = EMIF protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[4] = IVA-HD protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[5] = Dual Cortex-M4 protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[6] = IVAHD SL2 protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[13] = GPU protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[14] = DSS protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[15] = ISS protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[16] = L4_PER protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[17] = L4_CFG protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[18] = DebugSS protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[19] = AUDIOSS protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[22] = L4 wakeup protection violation
  - CONTROL_SEC_ERR_STATUS_DEBUG[23] = BB2D protection violation

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18.4.12.4 Protection SDRAM Configuration Registers

Table 18-66 lists the protection SDRAM configuration registers for EMIF1 and EMIF2 that are part of the general wakeup control module (CTRL_MODULE_WKUP). Upon POR, their values are exported as reset values of the EMIF1 and EMIF2 registers (EMIF_SDRAM_CONFIG and EMIF_SDRAM_CONFIG_2, respectively).

Table 18-66. Protection SDRAM Configuration Registers for EMIF1 and EMIF2

Physical Address	Register Name	Description	Access
0x4AE0 C110	CONTROL_PROT_EMIF1_SDRAM_CONFIG	Protection SDRAM configuration register 1. This register defines the bit field reset values of the EMIF1.EMIF_SDRAM_CONFIG register	RW
0x4AE0 C114	CONTROL_PROT_EMIF1_LPDDR2_NVM_CONFIG	Protection SDRAM configuration register 2. This register defines the bit field reset values of the EMIF1.EMIF_SDRAM_CONFIG_2 register	RW
0x4AE0 C118	CONTROL_PROT_EMIF2_SDRAM_CONFIG	Protection SDRAM configuration register 1. This register defines the bit field reset values of the EMIF2.EMIF_SDRAM_CONFIG register	RW
0x4AE0 C11C	CONTROL_PROT_EMIF2_LPDDR2_NVM_CONFIG2	Protection SDRAM configuration register 2. This register defines the bit field reset values of the EMIF2.EMIF_SDRAM_CONFIG_2 register	RW

18.4.12.5 Reference Voltage for Device LPDDR2/DDR3 I/O Buffers and LPDDR2/DDR3 Memory

The device LPDDR2/DDR3 I/O buffers work in so-called Vref-based receiver mode. In this mode, the buffers act like differential comparators with positive terminal connected to a device pad which receives signals from LPDDR2/DDR3 memory and negative terminal connected to a source of reference voltage. To work properly, a reference voltage must be provided to the device LPDDR2/DDR3 I/O buffers. Several Vref-generation cells are integrated in the device to supply this internal reference voltage. They are referred to as internal Vref-generation cells. There are also external Vref-generation cells which provide reference voltage to the externally connected LPDDR2/DDR3 memory.

Figure 18-19 shows the internal and external Vref-generation cells for the device.

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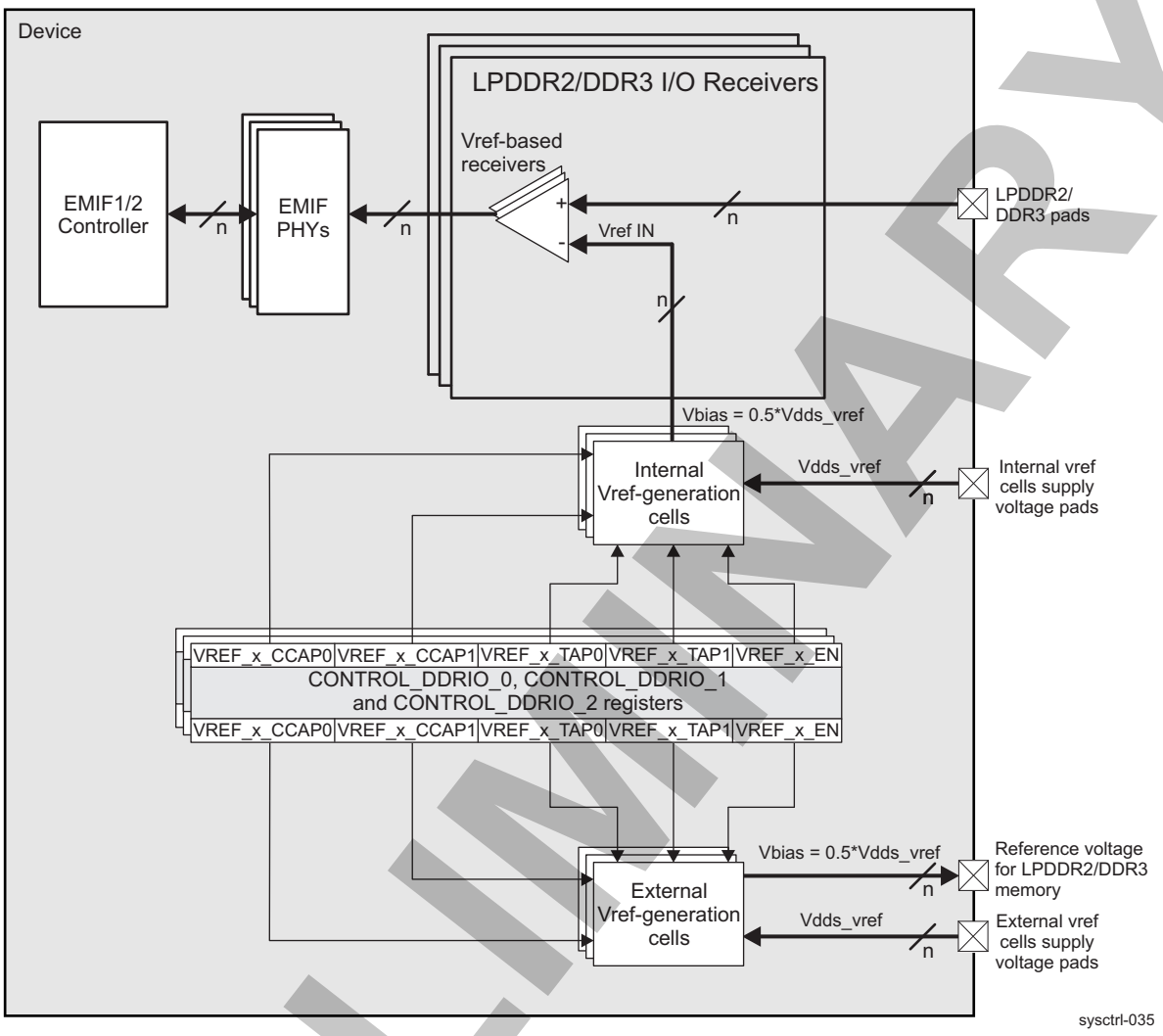
Figure 18-19. Internal and External Vref-Generation Cells and Their Controls



The Vref-generation cells reference voltage (Vbias) is equal to 0.5 × Vdds_vref, where Vdds_vref is the power supply voltage of the Vref cell. The Vref-based receiver allows improvement of speed performance when the LPDDR2/DDR3 I/Os are supplied by 1.2 V. A reference voltage is also provided to externally attached LPDDR2/DDR3 memory. The same type of Vref-generation cells are used for these external reference voltages.

The control bits for these internal and external Vref-generation cells reside in the CONTROL_DDRIO_0, CONTROL_DDRIO_1 and CONTROL_DDRIO_2 registers. Individual VREF_x_TAP[1:0] control bits set the output drive capability of the Vref cells. Table 18-67 lists the possible options for selection of load current sourced from the output of the Vref-generation cell.

Table 18-67. Vref Cell Load Current Selection

VREF_x_TAP1	VREF_x_TAP0	Description
0	0	2-µA load current
0	1	4-µA load current
1	0	8-µA load current
1	1	32-µA load current

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According to the noise environment, the user can choose to filter the supplied reference voltage. Two coupling capacitors internal to the Vref-generation cell are available and configurable through the individual VREF_x_CCAP[1:0] control bits in the CONTROL_DDRIO_0, CONTROL_DDRIO_1 and CONTROL_DDRIO_2 registers, as specified in Table 18-68.

Table 18-68. Vref Cell Coupling Capacitor Selection

VREF_x_CCAP1	VREF_x_CCAP0	Capacitor
0	0	No capacitor connected.
0	1	One capacitor connected between Vbias and ground.(1)
1	0	One capacitor connected between Vbias and Vdds_vref.(2)
1	1	One capacitor connected between Vbias and ground and one capacitor connected between Vbias and Vdds_vref.

(1) Vbias is the output of the Vref-generation cell which provides the reference voltage.
(2) Vdds_vref is the power supply voltage of the Vref-generation cell.

The Vref-gereration cells can be enabled by setting the VREF_x_EN bits in the CONTROL_DDRIO_0, CONTROL_DDRIO_1, and CONTROL_DDRIO_2 registers to 0x1; these cells can be disabled (for leakage improvement and when not in use) by clearing the same VREF_x_EN bits.

There are the following internal and external Vref-generation cells per memory channel:

- Four internal Vref-generation cells providing reference voltage for the device LPDDR2/DDR3 DQ line I/Os (one Vref cell per data byte);
- One external Vref-generation cell that is intended to provide reference voltage to CA line receivers of the LPDDR2 memory;
- One external Vref-generation cell that provides reference voltage simultaneously to the four DQ lines of the LPDDR2/DDR3 memory;
- Two external Vref-generation cells intended to provide reference voltage to the command and address line receivers of the DDR3 memory.

NOTE: For leakage improvement software must set the CONTROL_DDRIO_2[27] LPDDR2CH1_VREF_CA_INT_EN and CONTROL_DDRIO_2[17] LPDDR2CH2_VREF_CA_INT_EN bits to 0x0.

Table 18-69 shows the internal Vref-generation cells control bits and the LPDDR2/DDR3 IOs pads used as receivers to which the corresponding Vref cell supplies reference voltage.

Table 18-69. Internal Vref-Generation Cells Controls Versus LPDDR2/DDR3 Receiver Pads

Internal Vref-generation Cell Control Bits for Memory Channel 1	Vref Cell Associated LPDDR2/DDR3 Pads Used as Receivers (pads for memory channel 1)
CONTROL_DDRIO_0[19] DDRCH1_VREF_DQ0_INT_CCAP0	ddrch1_fifo_we0, ddrch1_dq[7:0], ddrch1_dm0
CONTROL_DDRIO_0[18] DDRCH1_VREF_DQ0_INT_CCAP1	
CONTROL_DDRIO_0[17] DDRCH1_VREF_DQ0_INT_TAP0	
CONTROL_DDRIO_0[16] DDRCH1_VREF_DQ0_INT_TAP1	
CONTROL_DDRIO_0[15] DDRCH1_VREF_DQ0_INT_EN	
CONTROL_DDRIO_0[14] DDRCH1_VREF_DQ1_INT_CCAP0	ddrch1_fifo_we1, ddrch1_dq[15:8], ddrch1_dm1
CONTROL_DDRIO_0[13] DDRCH1_VREF_DQ1_INT_CCAP1	
CONTROL_DDRIO_0[12] DDRCH1_VREF_DQ1_INT_TAP0	
CONTROL_DDRIO_0[11] DDRCH1_VREF_DQ1_INT_TAP1	
CONTROL_DDRIO_0[10] DDRCH1_VREF_DQ1_INT_EN	

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Table 18-69. Internal Vref-Generation Cells Controls Versus LPDDR2/DDR3 Receiver Pads (continued)

CONTROL_DDRIO_0[9] DDRCH1_VREF_DQ2_INT_CCAP0	ddrch1_fifo_we2, ddrch1_dq[23:16], ddrch1_dm2
CONTROL_DDRIO_0[8] DDRCH1_VREF_DQ2_INT_CCAP1	
CONTROL_DDRIO_0[7] DDRCH1_VREF_DQ2_INT_TAP0	
CONTROL_DDRIO_0[6] DDRCH1_VREF_DQ2_INT_TAP1	
CONTROL_DDRIO_0[5] DDRCH1_VREF_DQ2_INT_EN	
CONTROL_DDRIO_0[4] DDRCH1_VREF_DQ3_INT_CCAP0	ddrch1_fifo_we3, ddrch1_dq[31:24], ddrch1_dm3
CONTROL_DDRIO_0[3] DDRCH1_VREF_DQ3_INT_CCAP1	
CONTROL_DDRIO_0[2] DDRCH1_VREF_DQ3_INT_TAP0	
CONTROL_DDRIO_0[1] DDRCH1_VREF_DQ3_INT_TAP1	
CONTROL_DDRIO_0[0] DDRCH1_VREF_DQ3_INT_EN	
Internal Vref-generation Cell Control Bits for Memory Channel 2	**Vref Cell Associated LPDDR2/DDR3 Pads Used as Receivers (pads for memory channel 2)**
CONTROL_DDRIO_1[26] DDRCH2_VREF_DQ0_INT_CCAP0	ddrch2_fifo_we0, ddrch2_dq[7:0], ddrch2_dm0
CONTROL_DDRIO_1[25] DDRCH2_VREF_DQ0_INT_CCAP1	
CONTROL_DDRIO_1[24] DDRCH2_VREF_DQ0_INT_TAP0	
CONTROL_DDRIO_1[23] DDRCH2_VREF_DQ0_INT_TAP1	
CONTROL_DDRIO_1[22] DDRCH2_VREF_DQ0_INT_EN	
CONTROL_DDRIO_1[21] DDRCH2_VREF_DQ1_INT_CCAP0	ddrch2_fifo_we1, ddrch2_dq[15:8], ddrch2_dm1
CONTROL_DDRIO_1[20] DDRCH2_VREF_DQ1_INT_CCAP1	
CONTROL_DDRIO_1[19] DDRCH2_VREF_DQ1_INT_TAP0	
CONTROL_DDRIO_1[18] DDRCH2_VREF_DQ1_INT_TAP1	
CONTROL_DDRIO_1[17] DDRCH2_VREF_DQ1_INT_EN	
CONTROL_DDRIO_1[16] DDRCH2_VREF_DQ2_INT_CCAP0	ddrch2_fifo_we2, ddrch2_dq[23:16], ddrch2_dm2
CONTROL_DDRIO_1[15] DDRCH2_VREF_DQ2_INT_CCAP1	
CONTROL_DDRIO_1[14] DDRCH2_VREF_DQ2_INT_TAP0	
CONTROL_DDRIO_1[13] DDRCH2_VREF_DQ2_INT_TAP1	
CONTROL_DDRIO_1[12] DDRCH2_VREF_DQ2_INT_EN	
CONTROL_DDRIO_1[11] DDRCH2_VREF_DQ3_INT_CCAP0	ddrch2_fifo_we3, ddrch2_dq[31:24], ddrch2_dm3
CONTROL_DDRIO_1[10] DDRCH2_VREF_DQ3_INT_CCAP1	
CONTROL_DDRIO_1[9] DDRCH2_VREF_DQ3_INT_TAP0	
CONTROL_DDRIO_1[8] DDRCH2_VREF_DQ3_INT_TAP1	
CONTROL_DDRIO_1[7] DDRCH2_VREF_DQ3_INT_EN	

Table 18-70 shows the external Vref-generation cells control bits and the pads to which the corresponding Vref cell supplies reference voltage.

Table 18-70. External Vref-Generation Cells Controls Versus Pads Supplying Reference Voltage to LPDDR2/DDR3 Memory

Pads Supplying Reference Voltage Out of the Device (used with memory channel 1)	External Vref-generation Cell Control Bits for Memory Channel 1
lpddr2ch1_vref_ca_out	CONTROL_DDRIO_2[26] LPDDR2CH1_VREF_CA_OUT_CCAP0
	CONTROL_DDRIO_2[25] LPDDR2CH1_VREF_CA_OUT_CCAP1
	CONTROL_DDRIO_2[24] LPDDR2CH1_VREF_CA_OUT_TAP0
	CONTROL_DDRIO_2[23] LPDDR2CH1_VREF_CA_OUT_TAP1
	CONTROL_DDRIO_2[22] LPDDR2CH1_VREF_CA_OUT_EN

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Table 18-70. External Vref-Generation Cells Controls Versus Pads Supplying Reference Voltage to LPDDR2/DDR3 Memory (continued)

ddrch1_vref_dq	CONTROL_DDRIO_1[31] DDRCH1_VREF_DQ_OUT_CCAP0
	CONTROL_DDRIO_1[30] DDRCH1_VREF_DQ_OUT_CCAP1
	CONTROL_DDRIO_1[29] DDRCH1_VREF_DQ_OUT_TAP0
	CONTROL_DDRIO_1[28] DDRCH1_VREF_DQ_OUT_TAP1
	CONTROL_DDRIO_1[27] DDRCH1_VREF_DQ_OUT_EN
ddr3ch1_vref_ca0	CONTROL_DDRIO_0[31] DDR3CH1_VREF_CA_CCAP0
	CONTROL_DDRIO_0[30] DDR3CH1_VREF_CA_CCAP1
	CONTROL_DDRIO_0[29] DDR3CH1_VREF_CA_TAP0
	CONTROL_DDRIO_0[28] DDR3CH1_VREF_CA_TAP1
	CONTROL_DDRIO_0[27] DDR3CH1_VREF_CA_EN
ddr3ch1_vref_ca1	CONTROL_DDRIO_EXT_[31] DDR3CH1_VREF_CA1_CCAP0
	CONTROL_DDRIO_EXT_[30] DDR3CH1_VREF_CA1_CCAP1
	CONTROL_DDRIO_EXT_[29] DDR3CH1_VREF_CA1_TAP0
	CONTROL_DDRIO_EXT_[28] DDR3CH1_VREF_CA1_TAP1
	CONTROL_DDRIO_EXT_[27] DDR3CH1_VREF_CA1_EN
Pads Supplying Reference Voltage Out of the Device (used with memory channel 2)	**External Vref-generation Cell Control Bits for Memory Channel 2**
lpddr2ch2_vref_ca_out	CONTROL_DDRIO_2[16] LPDDR2CH2_VREF_CA_OUT_CCAP0
	CONTROL_DDRIO_2[15] LPDDR2CH2_VREF_CA_OUT_CCAP1
	CONTROL_DDRIO_2[14] LPDDR2CH2_VREF_CA_OUT_TAP0
	CONTROL_DDRIO_2[13] LPDDR2CH2_VREF_CA_OUT_TAP1
	CONTROL_DDRIO_2[12] LPDDR2CH2_VREF_CA_OUT_EN
ddrch2_vref_dq	CONTROL_DDRIO_1[6] DDRCH2_VREF_DQ_OUT_CCAP0
	CONTROL_DDRIO_1[5] DDRCH2_VREF_DQ_OUT_CCAP1
	CONTROL_DDRIO_1[4] DDRCH2_VREF_DQ_OUT_TAP0
	CONTROL_DDRIO_1[3] DDRCH2_VREF_DQ_OUT_TAP1
	CONTROL_DDRIO_1[2] DDRCH2_VREF_DQ_OUT_EN
ddr3ch2_vref_ca0	CONTROL_DDRIO_0[25] DDR3CH2_VREF_CA_CCAP0
	CONTROL_DDRIO_0[24] DDR3CH2_VREF_CA_CCAP1
	CONTROL_DDRIO_0[23] DDR3CH2_VREF_CA_TAP0
	CONTROL_DDRIO_0[22] DDR3CH2_VREF_CA_TAP1
	CONTROL_DDRIO_0[21] DDR3CH2_VREF_CA_EN
ddr3ch2_vref_ca1	CONTROL_DDRIO_EXT_[25] DDR3CH2_VREF_CA1_CCAP0
	CONTROL_DDRIO_EXT_[24] DDR3CH2_VREF_CA1_CCAP1
	CONTROL_DDRIO_EXT_[23] DDR3CH2_VREF_CA1_TAP0
	CONTROL_DDRIO_EXT_[22] DDR3CH2_VREF_CA1_TAP1
	CONTROL_DDRIO_EXT_[21] DDR3CH2_VREF_CA1_EN

18.4.12.6 Force MPU Write Nonposted Transactions Control Register

At the top level, software can force all writes from the MPU subsystem to the L3 interconnect to be nonposted, regardless of the attributes of the transactions coming from the MPU. When active-high bit FORCEWRNP = 1, only nonposted write commands are sent to the L3 interconnect. This bit must remain stable for the entire transfer and must not change during the transfer.

Table 18-71 describes the general core control module register with FORCEWRNP control.

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Table 18-71. Force MPU Write Nonposted Transactions Control Register

Physical Address	Register Name	Description	Access
0x4A00 215C	CONTROL_FORCEWRNP	Forces only nonposted write commands from the MPU subsystem to the L3 interconnect	R/W

18.4.12.7 Signal Integrity Parameter Control Registers With Pad Group Assignment

18.4.12.7.1 Signal Integrity Parameter Controls Overview

Most of the I/O cells associated with the device pads can be configured to deliver their carried signals to the targeted input with maximum signal integrity. Configuration of these I/Os is done by pad group assignment, and not individually per pad.

The different I/O-specific requirements determine the use of different types of I/O cells for the device I/Os. Software controls associated with the signal integrity parameters are implemented at the CTRL_MODULE_CORE_PAD and CTRL_MODULE_WKUP_PAD level.

The following types of I/O cells associated with pad groups can be identified:

- LPDDR2/DDR3 high-speed I/O cells with impedance (I), slew rate (SR), and weak driver (WD) settings
- SMART I/O cells for most of the pads with slew rate control (SC) and drive strength (DS) control settings
- I2Cx I/O cells with pullup resistance versus capacitance load (LB), glitch free operation (GLFENB) and PULLUPRESX settings
- Extended drain I/O cells for sdcard pads. For more information, see Section 18.4.9, *Extended-Drain I/O and PBIAS Cell*
- Glitch Free I/O cells only for pads sys_nrespwron and sys_nreswarm

NOTE: Unlike most of the I/O cells, the glitch free I/O cell does not have signal integrity or dual voltage group control settings.

NOTE: C_{LOAD} is the total capacitance seen at the far end of the transmission line.

NOTE: I/Os are non-failsafe, meaning one must never apply voltage at a pad before the internal I/O supply voltage VDDS is powered.

The pad group-assigned signal integrity controls are provided through the registers described in Table 18-72.

Table 18-72. Signal Integrity Parameter Control Registers

Physical Address	Register Name	Description	Access
0x4A00 2DA8	CONTROL_SMART1IO_PADCONF_0	Signal integrity pad group assignment control register	R/W
0x4A00 2DAC	CONTROL_SMART1IO_PADCONF_1	Signal integrity pad group assignment control register	R/W
0x4A00 2DB0	CONTROL_SMART1IO_PADCONF_2	Signal integrity pad group assignment control register	R/W
0x4A00 2DB4	CONTROL_SMART2IO_PADCONF_0	Signal integrity pad group assignment control register	R/W
0x4A00 2DB8	CONTROL_SMART2IO_PADCONF_1	Signal integrity pad group assignment control register	R/W
0x4A00 2DBC	CONTROL_SMART2IO_PADCONF_2	Signal integrity pad group assignment control register	R/W
0x4A00 2DC0	CONTROL_SMART3IO_PADCONF_0	Signal integrity pad group assignment control register	R/W

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Table 18-72. Signal Integrity Parameter Control Registers (continued)

Physical Address	Register Name	Description	Access
0x4A00 2DC4	CONTROL_SMART3IO_PADCONF_1	Signal integrity pad group assignment control register	R/W
0x4A00 2E04	CONTROL_I2C_0	Signal integrity pad group assignment control register	R/W
0x4A00 2E30	CONTROL_DDR3CH1_0	Signal integrity pad group assignment control register	R/W
0x4A00 2E34	CONTROL_DDR3CH2_0	Signal integrity pad group assignment control register	R/W
0x4A00 2E38	CONTROL_DDRCH1_0	Signal integrity pad group assignment control register	R/W
0x4A00 2E3C	CONTROL_DDRCH1_1	Signal integrity pad group assignment control register	R/W
0x4A00 2E40	CONTROL_DDRCH2_0	Signal integrity pad group assignment control register	R/W
0x4A00 2E44	CONTROL_DDRCH2_1	Signal integrity pad group assignment control register	R/W
0x4A00 2E48	CONTROL_LPDDR2CH1_0	Signal integrity pad group assignment control register	R/W
0x4A00 2E4C	CONTROL_LPDDR2CH1_1	Signal integrity pad group assignment control register	R/W
0x4AE0 CDA0	CONTROL_SMART1NOPMIO_PADCONF_0	Signal integrity pad group assignment control register	R/W
0x4AE0 CDA4	CONTROL_SMART1NOPMIO_PADCONF_1	Signal integrity pad group assignment control register	R/W
0x4AE0 CDB0	CONTROL_I2C_2	Signal integrity pad group assignment control register	R/W

18.4.12.7.2 High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings

The LPDDR2/DDR3 buffers are based on 1.2-V high-speed unterminated logic and require excellent driver impedance control to achieve optimal timing-EMI trade-offs. A specific type of device I/O cells with programmable features are used to meet this requirement. These I/O cells support 1.2-V operation. These cells are also provided with additional features to support the high-speed inter-chip (HSIC) interface.

Two types of software-configurable I/O cells are integrated to support high-speed unterminated logic:

- Single-ended I/O cells
- Two-pad differential I/O cells

Two-pad differential I/O cells are provided with a differential receiver and complementary transmitter. They are used to support the LPDDR2/DDR3 clock pads and LPDDR2/DDR3 strobe pads.

The LPDDR2/DDR3 I/O cells are integrated with the following controls in the CTRL_MODULE_CORE_PAD module:

- Driver output impedance (I) controls
- SR controls
- WD controls to support LPDDR2/DDR3/HSIC interface and avoid floating pad
- Process-only impedance compensation using 5-bit binary coded schema separately for pullup p<1:5> and pulldown n<1:5> impedance

Programmable bits for impedance and SR control are provided when the I/Os are set to operate in driver mode (outputs).

The bits I[2:0] are used to program the desired impedance value of the driver. Table 18-73 describes the driver impedance settings.

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Table 18-73. Driver Impedance Output Settings

I[2]	I[1]	I[0]	Drive Setting Name
0	0	0	Drv5
0	0	1	Drv6
0	1	0	Drv7
0	1	1	Drv8
1	0	0	Drv9
1	0	1	Drv10
1	1	0	Drv11
1	1	1	Drv12

NOTE:

- Table 18-73 is valid for pullup and pulldown outputs.
- For all electrical characteristics please see the Electrical Characteristics / DC Electrical Characteristics section of the device Data Manual.

To achieve optimal noise/speed trade off, the slew rate of the output signal can also be programmed using the slew rate (turn-on time) control bits SR[2:0]. The SR settings in Table 18-74 do not affect the driver DC drive strength. They control only the driver turn-on time.

Table 18-74. Driver Slew Rate Settings

SR[2]	SR[1]	SR[0]	Turn-On Time Level	Note
0	0	0	fastest	All 8 values are valid.
...	...	...		
...	...	...		
1	1	1	slowest	

Weak pullup or pulldown or a keeper on pad is enabled through the WD[0] and WD[1] bits. The weak pullup or pulldown option is used to define the pad state (high or low) when no signal is driving the pad. The weak keeper option is used to maintain the previous output value when nothing is driving the pad. Table 18-75 describes the WD controls.

NOTE: The WD[1:0] bit field controls play the role of the PULLTYPESELECT and PULLUDENABLE bits within the standard pad configuration registers, and provides the keeper function to the I/Os with the state WD = 0b11.

Similar to the ddr1_x, ddr2_x and ddr3_x pads, the usbb1_hsic_data/strobe, usbb2_hsic_data/strobe, and usbb3_hsic_data/strobe pads also have weak driver software controls. They are in the CONTROL_SMART3IO_PADCONF_1 register.

Table 18-75. Weak Driver PUPD/Latch Mode

WD[1]	WD[0]	Operation
0	0	Pull logic disabled
0	1	Weak pullup enabled
1	0	Weak pulldown enabled
1	1	Weak keeper enabled

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NOTE: To avoid unnecessary power consumption, software must overwrite the Weak Driver (WD) reset values by setting them to 0x0.

NOTE: There is no software control (INPUTENABLE) for the input buffer of the high-speed unterminated logic I/Os associated with the ddr, usbb_hsic_data/strobe pads. If the CMOS buffer is enabled, it is always bidirectional (that is, the input buffer is always enabled).

18.4.12.7.3 SMART I/O Buffers with Slew Rate and Drive Strength Control Settings

Most of the device pads are associated with SMART I/O cells. The SMART I/O cell includes an output buffer which has programmable slew rate and drive strength controls (SC and DS bits, respectively).

There are three programmable slew rate levels for these I/Os. Based on the required AC performance, the slew rate selection is done for a given group of I/Os through the CONTROL_SMART2IO_PADCONF_0, CONTROL_SMART2IO_PADCONF_1 and CONTROL_SMART2IO_PADCONF_2 registers in the CORE power domain and the CONTROL_SMART1NOPMIO_PADCONF_1 registers located in the WKUP power domain. For the different groups of pads and corresponding signal integrity control registers, see Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*.

Table 18-76 provides the slew rate control settings that are selectable through the SC[1:0] bit field.

Table 18-76. Slew Rate Control Settings

SC1 Bit	SC0 Bit	Slew Rate Control Mode
0	0	slow
0	1	medium
1	0	high
1	1	Not applicable

The SMART I/O output buffer has four programmable drive strength levels. The drive strength selection is done for a given group of I/Os through the CONTROL_SMART1IO_PADCONF_0, CONTROL_SMART1IO_PADCONF_1, and CONTROL_SMART1IO_PADCONF_2 registers in the CORE power domain, and the CONTROL_SMART1NOPMIO_PADCONF_0 registers in the WKUP power domain. For the different groups of pads and corresponding signal integrity control registers, see Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*.

Table 18-77 provides the drive strength control settings selectable through the DS[1:0] bit fields.

Table 18-77. Drive Strength Control Settings

DS1	DS0	Drive Strength Control Mode
0	0	Maximum output buffer resistance
0	1	
1	0	
1	1	Minimum output buffer resistance

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NOTE: For all electrical characteristics please see the device Data Manual.

18.4.12.7.4 I2Cx I/Os Group PULLUPRESX Controls and Load Range Settings

The I2Cx buffer contains internal pullup resistors for FS and HS modes. The I2Cx_LB (where x = 1 to 5) bit fields in the CONTROL_SMART3IO_PADCONF_0 register are used to select an appropriate pullup resistor for a given load range. These pullup resistors can be enabled or disabled through the I2Cx_SDA_PULLUPRESx and I2Cx_SCL_PULLUPRESx (where x = 1 to 5) bits, which reside in the CONTROL_I2C_0 register. In the same register, the active high I2Cx_SDA_GLFENB and I2Cx_SCL_GLFENB bits are implemented for I^2C receivers to enable glitch-free operation.

The CONTROL_SMART1NOPMIO_PADCONF_0[7:6] SR_LB bit field is used to select an appropriate pullup resistor value for SR PMIC I2C. The SR PMIC associated internal pullup resistors can be enabled and disabled through the CONTROL_I2C_2[30] SR_PMIC_SDA_PULLUPRESX and CONTROL_I2C_2[28] SR_PMIC_SCL_PULLUPRESX bits. Setting the CONTROL_I2C_2[31] SR_PMIC_SDA_GLFENB and CONTROL_I2C_2[29] SR_PMIC_SCL_GLFENB bits enables glitch-free operation.

NOTE: The pullup-versus-load settings applicable to I2Cx FS mode also apply to I2Cx standard speed mode.

NOTE: PULLUDENABLE must be set to 0b0 in the I2Cx pad configuration registers (disable internal weak pullup resistors on I2Cx pads) to ensure the full I/O cell performance capabilities of the I^2C.

NOTE: For all electrical characteristics and different modes settings, see the device Data Manual.

18.4.12.7.5 Device Interfaces Signal Group Controls Mapping

Table 18-78 through Table 18-96 describe the mapping of the signal integrity control bit fields in the different signal integrity control registers described in Table 18-72.

NOTE: The same I/O cell and I/O cell controls assigned to a pad signal available when MUXMODE = 0 are shared between signals available on the same pad when MUXMODE is selected different than 0. For more information, see Section 18.4.8.3, *Pad Multiplexing Register Fields*.

Table 18-78. EMIF LPDDR2/DDR3 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

EMIF (LPDDR2/LPDDR3) Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_LPDDR2CH1_0[31:29] LPDDR2CH1_PART0_I CONTROL_LPDDR2CH1_0[28:26] LPDDR2CH1_PART0_SR CONTROL_LPDDR2CH1_0[25:24] LPDDR2CH1_PART0_WD	lpddr2ch1_ncs0; lpddr2ch1_ncs1; lpddr2ch1_cke0; lpddr2ch1_cke1
CONTROL_LPDDR2CH1_0[23:21] LPDDR2CH1_PART5_I CONTROL_LPDDR2CH1_0[20:18] LPDDR2CH1_PART5_SR CONTROL_LPDDR2CH1_0[17:16] LPDDR2CH1_PART5_WD	lpddr2ch1_ca0, lpddr2ch1_ca1, lpddr2ch1_ca2, lpddr2ch1_ca3, lpddr2ch1_ca4, lpddr2ch1_ca5, lpddr2ch1_ca6, lpddr2ch1_ca7, lpddr2ch1_ca8, lpddr2ch1_ca9
CONTROL_LPDDR2CH1_0[15:13] LPDDR2CH1_PART6_I CONTROL_LPDDR2CH1_0[12:10] LPDDR2CH1_PART6_SR CONTROL_LPDDR2CH1_0[9:8] LPDDR2CH1_PART6_WD	lpddr2ch1_ck; lpddr2ch1_nck
CONTROL_LPDDR2CH1_1[31:29] LPDDR2CH2_PART0_I	lpddr2ch2_ncs0, lpddr2ch2_ncs1, lpddr2ch2_cke0, lpddr2ch2_cke1

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Table 18-78. EMIF LPDDR2/DDR3 Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

EMIF (LPDDR2/LPDDR3) Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_LPDDR2CH1_1[28:26] LPDDR2CH2_PART0_SR CONTROL_LPDDR2CH1_1[25:24] LPDDR2CH2_PART0_WD	
CONTROL_LPDDR2CH1_1[23:21] LPDDR2CH2_PART5_I CONTROL_LPDDR2CH1_1[20:18] LPDDR2CH2_PART5_SR CONTROL_LPDDR2CH1_1[17:16] LPDDR2CH2_PART5_WD	lpddr2ch2_ca0, lpddr2ch2_ca1, lpddr2ch2_ca2, lpddr2ch2_ca3, lpddr2ch2_ca4, lpddr2ch2_ca5, lpddr2ch2_ca6, lpddr2ch2_ca7, lpddr2ch2_ca8, lpddr2ch2_ca9
CONTROL_LPDDR2CH1_1[15:13] LPDDR2CH2_PART6_I CONTROL_LPDDR2CH1_1[12:10] LPDDR2CH2_PART6_SR CONTROL_LPDDR2CH1_1[9:8] LPDDR2CH2_PART6_WD	lpddr2ch2_ck, lpddr2ch2_nck
CONTROL_DDR3CH1_0[31:29] DDR3CH1_PART0_I CONTROL_DDR3CH1_0[28:26] DDR3CH1_PART0_SR CONTROL_DDR3CH1_0[25:24] DDR3CH1_PART0_WD	ddr3ch1_ncas, ddr3ch1_nras, ddr3ch1_nreset, ddr3ch1_nwe, ddr3ch1_ncs0, ddr3ch1_ncs1, ddr3ch1_cke0, ddr3ch1_cke1, ddr3ch1_odt0, ddr3ch1_odt1
CONTROL_DDR3CH1_0[23:21] DDR3CH1_PART5A_I CONTROL_DDR3CH1_0[20:18] DDR3CH1_PART5A_SR CONTROL_DDR3CH1_0[17:16] DDR3CH1_PART5A_WD	ddr3ch1_a0, ddr3ch1_a1, ddr3ch1_a10_ap, ddr3ch1_a11, ddr3ch1_a12_nbc, ddr3ch1_a13, ddr3ch1_a14, ddr3ch1_a15, ddr3ch1_a2, ddr3ch1_a3, ddr3ch1_a4, ddr3ch1_a5, ddr3ch1_a6, ddr3ch1_a7, ddr3ch1_a8, ddr3ch1_a9
CONTROL_DDR3CH1_0[15:13] DDR3CH1_PART5B_I CONTROL_DDR3CH1_0[12:10] DDR3CH1_PART5B_SR CONTROL_DDR3CH1_0[9:8] DDR3CH1_PART5B_WD	ddr3ch1_ba0, ddr3ch1_ba1, ddr3ch1_ba2
CONTROL_DDR3CH1_0[7:5] DDR3CH1_PART6_I CONTROL_DDR3CH1_0[4:2] DDR3CH1_PART6_SR CONTROL_DDR3CH1_0[1:0] DDR3CH1_PART6_WD	ddr3ch1_cka, ddr3ch1_ncka, ddr3ch1_ckb, ddr3ch1_nckb
CONTROL_DDR3CH2_0[31:29] DDR3CH2_PART0_I CONTROL_DDR3CH2_0[28:26] DDR3CH2_PART0_SR CONTROL_DDR3CH2_0[25:24] DDR3CH2_PART0_WD	ddr3ch2_ncas, ddr3ch2_nras, ddr3ch2_nreset, ddr3ch2_nwe, ddr3ch2_ncs0, ddr3ch2_ncs1, ddr3ch2_cke0, ddr3ch2_cke1, ddr3ch2_odt0, ddr3ch2_odt1
CONTROL_DDR3CH2_0[23:21] DDR3CH2_PART5A_I CONTROL_DDR3CH2_0[20:18] DDR3CH2_PART5A_SR CONTROL_DDR3CH2_0[17:16] DDR3CH2_PART5A_WD	ddr3ch2_a0, ddr3ch2_a1, ddr3ch2_a10_ap, ddr3ch2_a11, ddr3ch2_a12_nbc, ddr3ch2_a13, ddr3ch2_a14, ddr3ch2_a15, ddr3ch2_a2, ddr3ch2_a3, ddr3ch2_a4, ddr3ch2_a5, ddr3ch2_a6, ddr3ch2_a7, ddr3ch2_a8, ddr3ch2_a9
CONTROL_DDR3CH2_0[15:13] DDR3CH2_PART5B_I CONTROL_DDR3CH2_0[12:10] DDR3CH2_PART5B_SR CONTROL_DDR3CH2_0[9:8] DDR3CH2_PART5B_WD	ddr3ch2_ba0, ddr3ch2_ba1, ddr3ch2_ba2
CONTROL_DDR3CH2_0[7:5] DDR3CH2_PART6_I CONTROL_DDR3CH2_0[4:2] DDR3CH2_PART6_SR CONTROL_DDR3CH2_0[1:0] DDR3CH2_PART6_WD	ddr3ch2_cka, ddr3ch2_ncka, ddr3ch2_ckb, ddr3ch2_nckb
CONTROL_DDRCH1_0[31:29] DDRCH1_PART1A_I CONTROL_DDRCH1_0[28:26] DDRCH1_PART1A_SR CONTROL_DDRCH1_0[25:24] DDRCH1_PART1A_WD	ddrch1_dq0, ddrch1_dq1, ddrch1_dq2, ddrch1_dq3, ddrch1_dq4, ddrch1_dq5, ddrch1_dq6, ddrch1_dq7, ddrch1_dm0
CONTROL_DDRCH1_0[23:21] DDRCH1_PART1B_I CONTROL_DDRCH1_0[20:18] DDRCH1_PART1B_SR CONTROL_DDRCH1_0[17:16] DDRCH1_PART1B_WD	ddrch1_dqs0, ddrch1_ndqs0, ddrch1_fifo_we0

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Table 18-78. EMIF LPDDR2/DDR3 Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

EMIF (LPDDR2/LPDDR3) Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_DDRCH1_0[15:13] DDRCH1_PART2A_I CONTROL_DDRCH1_0[12:10] DDRCH1_PART2A_SR CONTROL_DDRCH1_0[9:8] DDRCH1_PART2A_WD	ddrch1_dq8, ddrch1_dq9, ddrch1_dq10, ddrch1_dq11, ddrch1_dq12, ddrch1_dq13, ddrch1_dq14, ddrch1_dq15, ddrch1_dm1
CONTROL_DDRCH1_0[7:5] DDRCH1_PART2B_I CONTROL_DDRCH1_0[4:2] DDRCH1_PART2B_SR CONTROL_DDRCH1_0[1:0] DDRCH1_PART2B_WD	ddrch1_dqs1, ddrch1_ndqs1, ddrch1_fifo_we1
CONTROL_DDRCH1_1[31:29] DDRCH1_PART3A_I CONTROL_DDRCH1_1[28:26] DDRCH1_PART3A_SR CONTROL_DDRCH1_1[25:24] DDRCH1_PART3A_WD	ddrch1_dq16, ddrch1_dq17, ddrch1_dq18, ddrch1_dq19, ddrch1_dq20, ddrch1_dq21, ddrch1_dq22, ddrch1_dq23, ddrch1_dm2
CONTROL_DDRCH1_1[23:21] DDRCH1_PART3B_I CONTROL_DDRCH1_1[20:18] DDRCH1_PART3B_SR CONTROL_DDRCH1_1[17:16] DDRCH1_PART3B_WD	ddrch1_dqs2, ddrch1_ndqs2, ddrch1_fifo_we2
CONTROL_DDRCH1_1[15:13] DDRCH1_PART4A_I CONTROL_DDRCH1_1[12:10] DDRCH1_PART4A_SR CONTROL_DDRCH1_1[9:8] DDRCH1_PART4A_WD	ddrch1_dq24, ddrch1_dq25, ddrch1_dq26, ddrch1_dq27, ddrch1_dq28, ddrch1_dq28, ddrch1_dq30, ddrch1_dq31, ddrch1_dm3
CONTROL_DDRCH1_1[7:5] DDRCH1_PART4B_I CONTROL_DDRCH1_1[4:2] DDRCH1_PART4B_SR CONTROL_DDRCH1_1[1:0] DDRCH1_PART4B_WD	ddrch1_dqs3, ddrch1_ndqs3, ddrch1_fifo_we3
CONTROL_DDRCH2_0[31:29] DDRCH2_PART1A_I CONTROL_DDRCH2_0[28:26] DDRCH2_PART1A_SR CONTROL_DDRCH2_0[25:24] DDRCH2_PART1A_WD	ddrch2_dq0, ddrch2_dq1, ddrch2_dq2, ddrch2_dq3, ddrch2_dq4, ddrch2_dq5, ddrch2_dq6, ddrch2_dq7, ddrch2_dm0
CONTROL_DDRCH2_0[23:21] DDRCH2_PART1B_I CONTROL_DDRCH2_0[20:18] DDRCH2_PART1B_SR CONTROL_DDRCH2_0[17:16] DDRCH2_PART1B_WD	ddrch2_dqs0, ddrch2_ndqs0, ddrch2_fifo_we0
CONTROL_DDRCH2_0[15:13] DDRCH2_PART2A_I CONTROL_DDRCH2_0[12:10] DDRCH2_PART2A_SR CONTROL_DDRCH2_0[9:8] DDRCH2_PART2A_WD	ddrch2_dq8, ddrch2_dq9, ddrch2_dq10, ddrch2_dq11, ddrch2_dq12, ddrch2_dq13, ddrch2_dq14, ddrch2_dq15, ddrch2_dm1
CONTROL_DDRCH2_0[7:5] DDRCH2_PART2B_I CONTROL_DDRCH2_0[4:2] DDRCH2_PART2B_SR CONTROL_DDRCH2_0[1:0] DDRCH2_PART2B_WD	ddrch2_dqs1, ddrch2_ndqs1, ddrch2_fifo_we1
CONTROL_DDRCH2_1[31:29] DDRCH2_PART3A_I CONTROL_DDRCH2_1[28:26] DDRCH2_PART3A_SR CONTROL_DDRCH2_1[25:24] DDRCH2_PART3A_WD	ddrch2_dq16, ddrch2_dq17, ddrch2_dq18, ddrch2_dq19, ddrch2_dq20, ddrch2_dq21, ddrch2_dq22, ddrch2_dq23, ddrch2_dm2
CONTROL_DDRCH2_1[23:21] DDRCH2_PART3B_I CONTROL_DDRCH2_1[20:18] DDRCH2_PART3B_SR CONTROL_DDRCH2_1[17:16] DDRCH2_PART3B_WD	ddrch2_dqs2, ddrch2_ndqs2, ddrch2_fifo_we2
CONTROL_DDRCH2_1[15:13] DDRCH2_PART4A_I	

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Table 18-78. EMIF LPDDR2/DDR3 Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

EMIF (LPDDR2/LPDDR3) Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_DDRCH2_1[12:10] DDRCH2_PART4A_SR CONTROL_DDRCH2_1[9:8] DDRCH2_PART4A_WD	ddrch2_dq24, ddrch2_dq25, ddrch2_dq26, ddrch2_dq27, ddrch2_dq28, ddrch2_dq29, ddrch2_dq30, ddrch2_dq31, ddrch2_dm3
CONTROL_DDRCH2_1[7:5] DDRCH2_PART4B_I CONTROL_DDRCH2_1[4:2] DDRCH2_PART4B_SR CONTROL_DDRCH2_1[1:0] DDRCH2_PART4B_WD	ddrch2_dqs3, ddrch2_ndqs3, ddrch2_fifo_we3

Table 18-79. C2C Pad Group Parameter Controls

Bit Fields for Pad Group Controls	Pads in Group
CONTROL_SMART1IO_PADCONF_0[19:18] C2C_PART1_DS	c2c_datain0, c2c_datain1, c2c_datain2, c2c_datain3, c2c_datain4, c2c_datain5, c2c_datain6, c2c_datain7
CONTROL_SMART2IO_PADCONF_0[19:18] C2C_PART1_SC	
CONTROL_SMART1IO_PADCONF_0[17:16] C2C_PART2_DS	c2c_clkin1, c2c_clkin0, c2c_clkout0, c2c_clkout1
CONTROL_SMART2IO_PADCONF_0[17:16] C2C_PART2_SC	
CONTROL_SMART1IO_PADCONF_2[17:16] C2C_PART3_DS	c2c_dataout0, c2c_dataout1, c2c_dataout2, c2c_dataout3, c2c_dataout4, c2c_dataout5, c2c_dataout6, c2c_dataout7
CONTROL_SMART2IO_PADCONF_2[19:18] C2C_PART3_SC	
CONTROL_SMART1IO_PADCONF_2[15:14] C2C_PART4_DS	From c2c_data8 to c2c_data15
CONTROL_SMART2IO_PADCONF_2[17:16] C2C_PART4_SC	

Table 18-80. CAMERA I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

CAMERA Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_0[15:14] CAM_DS CONTROL_SMART2IO_PADCONF_0[15:14] CAM_SC	cam_shutter; cam_strobe; cam_globalreset

Table 18-81. USBB1, USBB2, and USBB3 I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

USBBx Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART3IO_PADCONF_1[31:29] USBB1_I	usbb1_hsic_strobe, usbb1_hsic_data
CONTROL_SMART3IO_PADCONF_1[22:20] USBB1_SR	
CONTROL_SMART3IO_PADCONF_1[28:26] USBB2_I	usbb2_hsic_strobe, usbb2_hsic_data
CONTROL_SMART3IO_PADCONF_1[19:17] USBB2_SR	
CONTROL_SMART3IO_PADCONF_1[25:23] USBB3_I	usbb3_hsic_strobe, usbb3_hsic_data
CONTROL_SMART3IO_PADCONF_1[16:14] USBB3_SR	

Table 18-82. EMMC I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

EMMC Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_0[9:8] EMMC_DS	emmc_clk, emmc_cmd, from emmc_data0 to emmc_data7
CONTROL_SMART2IO_PADCONF_0[9:8] EMMC_SC	

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Table 18-83. LLI Wakeup Signal Group Parameter Controls to Different Interface I/O Pads Mapping

LLI Wakeup Signal I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_2[11:10] LLIA_WKUP1_DS CONTROL_SMART2IO_PADCONF_2[13:12] LLIA_WKUP1_SC	llib_wakereqout, llia_wakereqout
CONTROL_SMART1NOPMIO_PADCONF_0[11:10] LLIA_WKUP0_DS CONTROL_SMART1NOPMIO_PADCONF_1[11:10] LLIA_WKUP0_SC	llib_wakereqin, llia_wakereqin

Table 18-84. ABE Signal Group Parameter Controls to Different Interface I/O Pads Mapping

McBSP1 Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_0[31:30] ABE_PART0_DS CONTROL_SMART2IO_PADCONF_0[31:30] ABE_PART0_SC	abe_clks
CONTROL_SMART1IO_PADCONF_0[29:28] ABE_PART1_DS CONTROL_SMART2IO_PADCONF_0[29:28] ABE_PART1_SC	abedmic_din1, abedmic_din2, abedmic_din3, abedmic_clk1
CONTROL_SMART1IO_PADCONF_0[27:26] ABE_PART2_DS CONTROL_SMART2IO_PADCONF_0[27:26] ABE_PART2_SC	abedmic_clk2, abedmic_clk3
CONTROL_SMART1IO_PADCONF_0[25:24] ABE_PART3C_DS CONTROL_SMART2IO_PADCONF_0[25:24] ABE_PART3C_SC	abeslimbus1_clock, abeslimbus1_data
CONTROL_SMART1IO_PADCONF_0[22:22] ABE_PART4_DS CONTROL_SMART2IO_PADCONF_0[22:22] ABE_PART4_SC	abemcbsp2_dr, abemcbsp2_dx, abemcbsp2_fsx, abemcbsp2_clkx
CONTROL_SMART1IO_PADCONF_0[21:20] ABE_PART5_DS CONTROL_SMART2IO_PADCONF_0[21:20] ABE_PART5_SC	abemcpdm_ul_data, abemcpdm_dl_data, abemcpdm_frame, abemcpdm_lb_clk

Table 18-85. UARTx Signal Group Parameter Controls to Different Interface I/O Pads Mapping

UART2 Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_1[9:8] UART2_PART1_DS CONTROL_SMART2IO_PADCONF_1[7:6] UART2_PART1_SC	uart2_rts, uart2_cts
CONTROL_SMART1IO_PADCONF_2[13:12] UART2_PART2_DS	uart2_rx, uart2_tx
CONTROL_SMART1IO_PADCONF_2[31:30] UART5_PART1_DS CONTROL_SMART2IO_PADCONF_2[29:28] UART5_PART1_SC	uart5_rx, uart5_tx
CONTROL_SMART1IO_PADCONF_1[7:6] UART3_PART1_DS CONTROL_SMART2IO_PADCONF_1[5:4] UART3_PART1_SC	uart3_cts_rctx, uart3_rts_irsd
CONTROL_SMART1IO_PADCONF_1[5:4] UART3_PART2_DS CONTROL_SMART2IO_PADCONF_2[31:30] UART3_PART2_SC	uart3_tx_irtx, uart3_rx_irrx
CONTROL_SMART1IO_PADCONF_2[31:30] UART5_PART2_DS CONTROL_SMART2IO_PADCONF_2[27:26] UART5_PART2_SC	uart5_cts, uart5_rts
CONTROL_SMART1IO_PADCONF_2[27:26] UART6_PART1_DS CONTROL_SMART2IO_PADCONF_2[25:24] UART6_PART1_SC	uart6_tx, uart6_rx
CONTROL_SMART1IO_PADCONF_2[25:24] UART6_PART2_DS CONTROL_SMART2IO_PADCONF_2[23:22] UART6_PART2_SC	uart6_cts, uart6_rts
CONTROL_SMART1IO_PADCONF_1[11:10] UART1_DS CONTROL_SMART2IO_PADCONF_1[9:8] UART1_SC	uart1_tx, uart1_cts, uart1_rx, uart1_rts

Table 18-86. MCSPI1 and MCSPI2 Signal Group Parameter Controls to Different Interface I/O Pads Mapping

McSPI1 Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_0[1:0] MCSPI1_DS	mcspi1_clk, mcspi1_somi, mcspi1_simo, mcspi1_cs0, mcspi1_cs1
CONTROL_SMART2IO_PADCONF_1[27:26] MCSPI1_SC	

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Table 18-86. MCSPI1 and MCSPI2 Signal Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

McSPI1 Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART2IO_PADCONF_1[25:24] MCSPI2_SC	mcspi2_cs0, mcspi2_clk, mcspi2_simo, mcspi2_somi
CONTROL_SMART1IO_PADCONF_1[31:30] MCSPI2_DS	

Table 18-87. I2Cx Signal Group Parameter Controls to Different Interface I/O Pads Mapping

I2Cx Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART3IO_PADCONF_0[23:22] I2C1_LB	i2c1_scl, i2c1_sda
CONTROL_I2C_0[25] I2C1_PMIC_SDA_GLFENB	
CONTROL_I2C_0[24] I2C1_PMIC_SDA_PULLUPRESX	
CONTROL_I2C_0[17] I2C1_PMIC_SCL_GLFENB	
CONTROL_I2C_0[16] I2C1_PMIC_SCL_PULLUPRESX	
CONTROL_SMART3IO_PADCONF_0[21:20] I2C2_LB	i2c2_scl, i2c2_sda
CONTROL_I2C_0[27] I2C2_SDA_GLFENB	
CONTROL_I2C_0[26] I2C2_SDA_PULLUPRESX	
CONTROL_I2C_0[19] I2C2_SCL_GLFENB	
CONTROL_I2C_0[18] I2C2_SCL_PULLUPRESX	
CONTROL_SMART3IO_PADCONF_0[19:18] I2C3_LB	i2c3_scl, i2c3_sda
CONTROL_I2C_0[29] I2C3_SDA_GLFENB	
CONTROL_I2C_0[28] I2C3_SDA_PULLUPRESX	
CONTROL_I2C_0[21] I2C3_SCL_GLFENB	
CONTROL_I2C_0[20] I2C3_SCL_PULLUPRESX	
CONTROL_SMART3IO_PADCONF_0[17:16] I2C4_LB	i2c4_scl, i2c4_sda
CONTROL_I2C_0[31] I2C4_SDA_GLFENB	
CONTROL_I2C_0[30] I2C4_SDA_PULLUPRESX	
CONTROL_I2C_0[23] I2C4_SCL_GLFENB	
CONTROL_I2C_0[22] I2C4_SCL_PULLUPRESX	
CONTROL_SMART3IO_PADCONF_0[15:14] I2C5_LB	i2c5_scl, i2c5_sda
CONTROL_I2C_0[15] 2C5_SDA_GLFENB	
CONTROL_I2C_0[14] I2C5_SDA_PULLUPRESX	
CONTROL_I2C_0[13] I2C5_SCL_GLFENB	
CONTROL_I2C_0[12] I2C5_SCL_PULLUPRESX	

Table 18-88. System Signals Group Parameter Controls to Different Interface I/O Pads Mapping

System Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1NOPMIO_PADCONF_0[27:26] FREF_IOREQ_DS CONTROL_SMART1NOPMIO_PADCONF_1[27:26] FREF_IOREQ_SC	fref_clk_ioreq
CONTROL_SMART1NOPMIO_PADCONF_0[25:24] FREF_OUT0_DS CONTROL_SMART1NOPMIO_PADCONF_1[25:24] FREF_OUT0_SC	fref_clk0_out

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Table 18-88. System Signals Group Parameter Controls to Different Interface I/O Pads Mapping (continued)

System Interface I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1NOPMIO_PADCONF_0[23:22] FREF_OUT1_DS CONTROL_SMART1NOPMIO_PADCONF_1[23:22] FREF_OUT1_SC	fref_clk1_out
CONTROL_SMART1NOPMIO_PADCONF_0[21:20] FREF_OUT2_DS CONTROL_SMART1NOPMIO_PADCONF_1[21:20] FREF_OUT2_SC	fref_clk2_out
CONTROL_SMART1NOPMIO_PADCONF_0[17:16] FREF_REQ2_DS CONTROL_SMART1NOPMIO_PADCONF_1[17:16] FREF_REQ2_SC	fref_clk2_req
CONTROL_SMART1NOPMIO_PADCONF_0[19:18] FREF_REQ1_DS CONTROL_SMART1NOPMIO_PADCONF_1[19:18] FREF_REQ1_SC	fref_clk1_req
CONTROL_SMART1NOPMIO_PADCONF_0[9:8] SYS_DS CONTROL_SMART1NOPMIO_PADCONF_1[9:8] SYS_SC	sys_pwr_req, sys_nirq1, sys_nirq2
CONTROL_SMART1NOPMIO_PADCONF_0[31:30] BOOT_GPO_DS CONTROL_SMART1NOPMIO_PADCONF_1[31:30] BOOT_GPO_SC	sys_boot0, sys_boot1, sys_boot2, sys_boot3, sys_boot4, sys_boot5

Table 18-89. HSI Signal Group Parameter Controls to Different Interface I/O Pads Mapping

HSI I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_0[5:4] HSI1_DS CONTROL_SMART2IO_PADCONF_1[31:30] HSI1_SC	hsi1_aready, hsi1_caready, hsi1_acwake, hsi1_cawake, hsi1_acflag, hsi1_acdata, hsi1_caflag, hsi1_cadata
CONTROL_SMART1IO_PADCONF_0[3:2] HSI2_DS CONTROL_SMART2IO_PADCONF_1[29:28] HSI2_SC	hsi2_caready, hsi2_aready, hsi2_cawake, hsi2_acwake, hsi2_caflag, hsi2_cadata, hsi2_acflag, hsi2_acdata

Table 18-90. GP Timers I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

GP Timers I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_1[25:24] TIMER10_DS CONTROL_SMART2IO_PADCONF_1[19:18] TIMER10_SC	timer10_pwm_evt
CONTROL_SMART1IO_PADCONF_1[15:14] TIMER9_DS CONTROL_SMART1IO_PADCONF_1[13:12] TIMER9_SC	timer9_pwm_evt
CONTROL_SMART1IO_PADCONF_1[23:22] TIMER11_DS CONTROL_SMART2IO_PADCONF_1[17:16] TIMER11_SC	timer11_pwm_evt
CONTROL_SMART1IO_PADCONF_1[21:20] TIMER5_DS CONTROL_SMART2IO_PADCONF_1[15:14] TIMER5_SC	timer5_pwm_evt
CONTROL_SMART1IO_PADCONF_1[19:18] TIMER6_DS CONTROL_SMART2IO_PADCONF_1[13:12] TIMER6_SC	timer6_pwm_evt
CONTROL_SMART1IO_PADCONF_1[17:16] TIMER8_DS CONTROL_SMART2IO_PADCONF_1[11:10]TIMER8_SC	timer8_pwm_evt

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Table 18-91. DSS RFBI/DPI I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

DSS RFBI/DPI I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_2[21:20] DSS_PART1_DS CONTROL_SMART2IO_PADCONF_0[5:4] DSS_PART1_SC	rfbi_hsync0, rfbi_te_vsync0, rfbi_re, rfbi_a0, rfbi_data8, rfbi_data9, rfbi_data10, rfbi_data11, rfbi_data12, rfbi_data13, rfbi_data14, rfbi_data15, gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187
CONTROL_SMART1IO_PADCONF_2[19:18] DSS_PART2_DS CONTROL_SMART2IO_PADCONF_0[3:2] DSS_PART2_SC	rfbi_data0, rfbi_data1, rfbi_data2, rfbi_data3, rfbi_data4 rfbi_data5, rfbi_data6, rfbi_data7, rfbi_cs0, rfbi_we

Table 18-92. WLSDIO Signal Group Parameter Controls to Different Interface I/O Pads Mapping

WLSDIO I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_2[23:22] WLSDIO_DS CONTROL_SMART2IO_PADCONF_2[21:20] WLSDIO_SC	wlsdio_clk, wlsdio_cmd, wlsdio_data0, wlsdio_data1, wlsdio_data2, wlsdio_data3

Table 18-93. GPIO Signal Group Parameter Controls to Different Interface I/O Pads Mapping

GPIO I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_1[29:28] GPIO_DS CONTROL_SMART2IO_PADCONF_1[23:22] GPIO_SC	gpio5_145, gpio5_146

Table 18-94. JTAG I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

JTAG I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1NOPMIO_PADCONF_0[15:14] JTAG_PART0_DS CONTROL_SMART1NOPMIO_PADCONF_1[15:14] JTAG_PART0_SC	drm_emu0, drm_emu1
CONTROL_SMART1NOPMIO_PADCONF_0[13:12] JTAG_PART1_DS CONTROL_SMART1NOPMIO_PADCONF_1[13:12] JTAG_PART1_SC	jtag_ntrst, jtag_tck, jtag_rtck, jtag_tmsc, jtag_tdi, jtag_tdo

Table 18-95. DSI TE I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

DSI TE I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_0[13:12] DSIPORTA_DS CONTROL_SMART2IO_PADCONF_0[13:12] DSIPORTA_SC	dsiporta_te0
CONTROL_SMART1IO_PADCONF_0[11:10] DSIPORTC_DS CONTROL_SMART2IO_PADCONF_0[11:10] DSIPORTC_SC	dsiportc_te0

Table 18-96. HDMI I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping

HDMI I/O Controls	
Bit Fields for Pad Group Controls	**Pads (MUXMODE = 0) in Group**
CONTROL_SMART1IO_PADCONF_0[7:6] HDMI_PART1_DS CONTROL_SMART2IO_PADCONF_0[7:6] HDMI_PART1_SC	hdmi_cec, hdmi_hpd
CONTROL_SMART3IO_PADCONF_0[25:24] HDMI_PART2_LB	hdmi_ddc_scl, hdmi_ddc_sda

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18.4.12.8 Dual Voltage-Supplied Peripheral Controls

Some of the peripheral I/Os have the option to be supplied with a 1.2-V or 1.8-V power supply (VDDS through device external pads). The power supply level to the dual-voltage I/Os of different peripherals is configurable through bit fields in the CONTROL_PADCONF_MODE register in the CORE domain (Camera TCTRL i/f, GPIO, I2C2, I2C3, I2C4, I2C5, Timers, ABE modules i/f, SDIO/MMC2, SDIO/MMC3, MCSPI1, MCSPI2, DSI, UART1, UART2, UART3, UART5, UART6, HSI1, HSI2, HDMI) and the CONTROL_WKUP_PADCONF_MODE register in the WKUP domain (I2C1 i/f, Power management IC i/f, system i/f). One control bit in these registers is dedicated to set dual-voltage per group of pads.

Table 18-97 describes dual-voltage controls versus the mapping of different pads.

Table 18-97. Dual-Voltage Peripheral Control Bits vs Pad Mapping

Dual-Voltage VDDS = 1.2-V/1.8-V Control Bits	Pads With Dual-Voltage Settings
CONTROL_PADCONF_MODE[31] VDDS_10_MODE	cam_shutter, cam_strobe, cam_globalreset, timer11_pwm_evt, timer5_pwm_evt, timer6_pwm_evt, timer8_pwm_evt, i2c3_scl, i2c3_sda, gpio8_233, gpio8_234
CONTROL_PADCONF_MODE[30] VDDS_11_MODE	abemcbsp2_dr, abemcbsp2_dx, abemcbsp2_fsx, abemcbsp2_clkx, abemcpdm_ul_data abemcpdm_dl_data, abemcpdm_frame, abemcpdm_lb_clk, abe_clks
CONTROL_PADCONF_MODE[29] VDDS_12_MODE	abedmic_din1, abedmic_din2, abedmic_din3, abedmic_clk1, abedmic_clk2, abedmic_clk3
CONTROL_PADCONF_MODE[28] VDDS_14_MODE	abeslimbus1_clock, abeslimbus1_data,
CONTROL_PADCONF_MODE[27] VDDS_15_MODE	wlsdio_clk, wlsdio_cmd, wlsdio_data0, wlsdio_data1, wlsdio_data2, wlsdio_data3
CONTROL_PADCONF_MODE[26] VDDS_16_MODE	uart5_rx, uart5_tx, uart5_cts, uart5_rts, i2c2_scl, i2c2_sda
CONTROL_PADCONF_MODE[25] VDDS_18_MODE	mcspi1_clk, mcspi1_somi, mcspi1_simo, mcspi1_cs0, mcspi1_cs1, i2c5_scl, i2c5_sda
CONTROL_PADCONF_MODE[24] VDDS_19_MODE	gpio5_145, gpio5_146
CONTROL_PADCONF_MODE[23] VDDS_21_MODE	uart6_tx, uart6_rx, uart6_cts, uart6_rts, uart3_cts_rctx, uart3_rts_irsd, uart3_tx_irtx, uart3_rx_irrx
CONTROL_PADCONF_MODE[22] VDDS_5_MODE	timer9_pwm_evt, dsiportc_te0
CONTROL_PADCONF_MODE[21] VDDS_8_MODE	mcspi2_cs0, mcspi2_clk, mcspi2_simo, mcspi2_somi, i2c4_scl, i2c4_sda
CONTROL_PADCONF_MODE[20] VDDS_2_MODE	hsi1_acready, hsi1_caready, hsi1_acwake, hsi1_cawake, hsi1_acflag, hsi1_acdata, hsi1_caflag hsi1_cadata, uart1_tx, uart1_cts, uart1_rx, uart1_rts
CONTROL_PADCONF_MODE[19] VDDS_4_MODE	hsi2_caready, hsi2_acready, hsi2_cawake, hsi2_acwake, hsi2_caflag, hsi2_cadata, hsi2_acflag, hsi2_acdata, uart2_rts, uart2_cts, uart2_rx, uart2_tx
CONTROL_PADCONF_MODE[18] VDDS_9_MODE	rfbi_hsync0, rfbi_te_vsync0, rfbi_re, rfbi_a0, rfbi_data8, rfbi_data9, rfbi_data10, rfbi_data11, rfbi_data12, rfbi_data13, rfbi_data14, rfbi_data15 gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187 rfbi_data0, rfbi_data1, rfbi_data2, rfbi_data3, rfbi_data4, rfbi_data5, rfbi_data6, rfbi_data7, rfbi_cs0, rfbi_we
CONTROL_PADCONF_MODE[17] VDDS_EMMC_MODE	emmc_clk, emmc_cmd, emmc_data0, emmc_data1, emmc_data2, emmc_data3, emmc_data4, emmc_data5, emmc_data6, emmc_data7
CONTROL_PADCONF_MODE[16] VDDS_HDMI_MODE	hdmi_cec, hdmi_hpd, hdmi_ddc_scl, hdmi_ddc_sda, vdda_hdmi, hdmi_clkx, hdmi_clky, hdmi_data0x, hdmi_data0y, hdmi_data1x, hdmi_data1y, hdmi_data2x, hdmi_data2y
CONTROL_PADCONF_MODE[15] VDDA_DSIPORTA_MODE	dsiporta_lane0x, dsiporta_lane0y, dsiporta_lane1x, dsiporta_lane1y, dsiporta_lane2x, dsiporta_lane2y, dsiporta_lane3x, dsiporta_lane3y, dsiporta_lane4x, dsiporta_lane4y

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Table 18-97. Dual-Voltage Peripheral Control Bits vs Pad Mapping (continued)

Dual-Voltage VDDS = 1.2-V/1.8-V Control Bits	Pads With Dual-Voltage Settings
CONTROL_PADCONF_MODE[14] VDDA_DSIPORTC_MODE	dsiportc_lane0x, dsiportc_lane0y, dsiportc_lane1x, dsiportc_lane1y, dsiportc_lane2x, dsiportc_lane2y, dsiportc_lane3x, dsiportc_lane3y, dsiportc_lane4x, dsiportc_lane4y
CONTROL_PADCONF_MODE[13] VDDS_C2C_MODE	from c2c_datain0 to c2c_datain7 c2c_clkin1, c2c_clkin0, c2c_clkout0, c2c_clkout1 from c2c_dataout0 to c2c_dataout7 from c2c_data8 to c2c_data15
CONTROL_WKUP_PADCONF_MODE[31] VDDS_25_MODE	fref_clk1_out, fref_clk2_out, fref_clk2_req, fref_clk1_req, llib_wakereqout, llia_wakereqout, llib_wakereqin, llia_wakereqin
CONTROL_WKUP_PADCONF_MODE[30] VDDS_26_MODE	sys_pwr_req, sr_pmic_scl, sr_pmic_sda, sys_nirq1, sys_nirq2, i2c1_pmic_scl, i2c1_pmic_sda, sys_boot0, sys_boot1, sys_boot2, sys_boot3, sys_boot4, sys_boot5

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18.5 Control Module Programming Guide

18.5.1 Control Module Low-Level Programming Models

This section describes the low-level programming sequences for the configuration and use of the control module.

18.5.1.1 Global Initialization

18.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the control module is used for the first time after a device reset. This initialization of surrounding modules is based on the environment and integration of the control module. For more information, see *Section 18.2, Control Module Environment*, and Section 18.3, *Control Module Integration*.

Table 18-98. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The three clocks coming from the PRCM module (L4CFG_L4_GICLK, WKUPAON_GICLK, and L3INSTR_TS_GCLK) are not software-controlled by PRCM. For more information about the three clocks, see Section 3.6, *Clock Management Functional Description*, in Chapter 3, *Power, Reset, and Clock Management*.
L4 interconnect	For information about the L4_CFG interconnect configuration, see Section 14.3, *L4 Interconnects*.

18.5.1.1.2 Control Module Global Initialization

18.5.1.1.2.1 Software Reset

The control module is not sensitive to a software reset.

18.5.1.2 Operational Modes Configuration

18.5.1.2.1 Extended-Drain I/Os and PBIAS Cells Programming Guide

This section describes the programming flow from 3.0 V to 1.8 V, and vice versa, when operating with the extended-drain I/Os and PBIAS cells. Figure 18-20 shows the interrup-method configuration of the PBIAS cell for operation in different modes. Table 18-99 lists the registration settings for configuring the SDCARD_PBIAS cell and SDCARD extended-drain I/O cell.

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Figure 18-20. Configuring PBIAS Cell to Operate in Different Modes, Interrupt Method

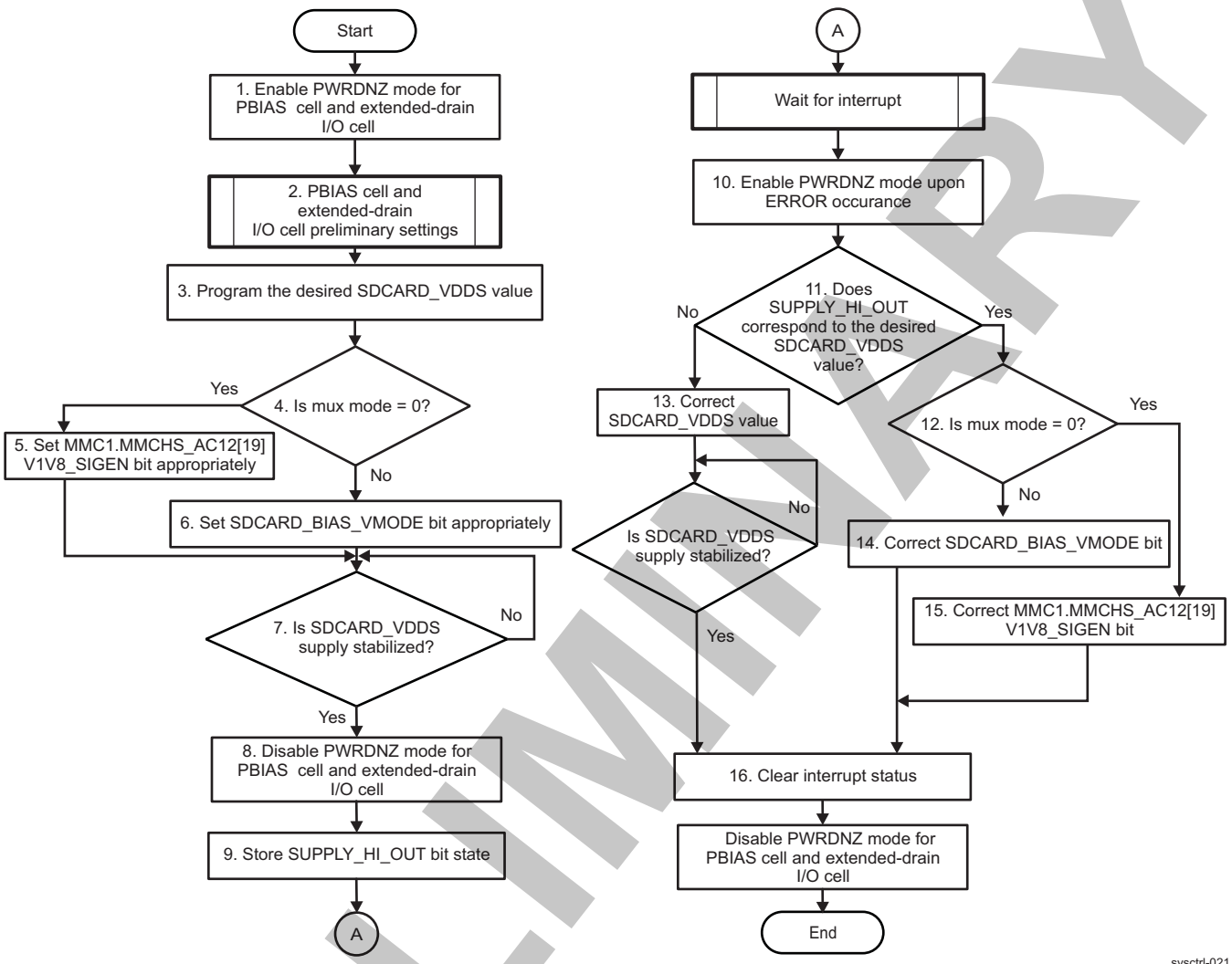

Table 18-99. Register Settings for Configuring the SDCARD_PBIAS Cell and SDCARD Extended-Drain I/O Cell

Procedure Name	Description	Register Settings
1. Enable PWRDNZ mode for PBIAS cell and extended-drain I/O cell.	Software must keep SDCARD_PBIAS cell and SDCARD extended-drain I/O cell PWRDNZ signals low whenever SDCARD_VDDS ramps up/down or changes. This is for cell protection purposes.	1. Set CONTROL_PBIAS[26] SDCARD_IO_PWRDNZ = 0b0. 2. Set CONTROL_PBIAS[27] SDCARD_BIAS_PWRDNZ = 0b0.
2. Preliminary SDCARD_PBIAS cell and SDCARD extended-drain I/O cell settings.	Enable SDCARD_PBIAS cell output and SDCARD_PBIAS error associated interrupt. Select desired I/Os within the SDCARD I/O cell and set the corresponding pad configuration fields appropriately.	1. Set CONTROL_PBIAS[25]SDCARD_BIAS_HIZ_MODE = 0b0. 2. For more information about setting MPU_IRQ_75 line-associated interrupt request PBIAS_IRQ, see Chapter 17, *Interrupt Controllers*. 3. For I/O multiplexing and pad configuration settings, see Section 18.5.1.2.3, *Pad Configuration Programming Points*.
3. Program the desired SDCARD_VDDS voltage for MMC/SD/SDIO1 I/Os.	Program external power supply IC to generate appropriate SDCARD_VDDS voltage (3.0 V or 1.8 V).	For more information about I^2C interface operation, see Section 23.1.1, *HS I2C Overview*.

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Table 18-99. Register Settings for Configuring the SDCARD_PBIAS Cell and SDCARD Extended-Drain I/O Cell (continued)

Procedure Name	Description	Register Settings
4. Check whether MUXMODE is set to 0 or not.	When mux mode is set to 0 sdcard_i signals are muxed on the pads and SDCARD_BIAS_VMODE does not apply. In this case MMC1.MMCHS_AC12[19] V1V8_SIGEN applies.	CONTROL_CORE_PAD0_X_PAD1_Y.MUXMODE = 0x-
5. Set V1V8_SIGEN bit appropriately.	PBIAS voltage generation is based on the value of V1V8_SIGEN, set according to externally applied SDCARD_VDDS voltage.	MMC1.MMCHS_AC12[19] V1V8_SIGEN = 0b- (1)
6. Set SDCARD_BIAS_VMODE bit appropriately.	PBIAS voltage generation is based on the value of SDCARD_BIAS_VMODE, set according to externally applied SDCARD_VDDS voltage.	Set CONTROL_PBIAS[21] SDCARD_BIAS_VMODE = 0b- (2).
7. Check whether the SDCARD_VDDS supply is stabilized.	Check the state of the externally generated SDCARD_VDDS voltage, which is provided through communication between the device and external power supply device over the I^2C interface.	For more information about I^2C interface settings, see Section 23.1.1, *HS I2C Overview*.
8. Disable PWRDNZ mode for SDCARD_PBIAS cell and extended-drain I/O cell	This starts the SDCARD_PBIAS cell work to generate the PBIAS voltage.	1. Set CONTROL_PBIAS[26] SDCARD_IO_PWRDNZ = 0b1. 2. Set CONTROL_PBIAS[27] SDCARD_BIAS_PWRDNZ = 0b1.
9. Store the state of the SUPPLY_HI_OUT bit.	Done as a preliminary step for error-handling analysis. (Whenever PWRDNZ = 0b0, SUPPLY_HI_OUT is unconditionally set to 0b0.)	Store the CONTROL_PBIAS[24] SDCARD_BIAS_SUPPLY_HI_OUT bit in memory.
10.Enable PWRDNZ mode upon error occurrence.	It is recommended that all the I/Os are powered down (PWRDNZ = 0) as soon as VMODE_ERROR is high.	1. Set CONTROL_PBIAS[26] SDCARD_IO_PWRDNZ = 0b0 2. Set CONTROL_PBIAS[27] SDCARD_BIAS_PWRDNZ = 0b0.
11. Does SUPPLY_HI_OUT correspond to the desired SDCARD_VDDS?	Test whether the error comes from incorrectly set value of SDCARD_VDDS or incorrectly set VMODE bit.	Check the SUPPLY_HI_OUT bit stored in memory.
12. Check whether MUXMODE is set to 0 or not.	When muxmode is set to 0, sdcard_i signals are muxed on the pads and SDCARD_BIAS_VMODE does not apply. In this case MMC1.MMCHS_AC12[19] V1V8_SIGEN applies.	CONTROL_CORE_PAD0_X_PAD1_Y.MUXMODE = 0x-
13. Correct SDCARD_VDDS value.	If SUPPLY_HI_OUT is different from expected, correct and set SDCARD_VDDS value over I^2C again.	For more information about I^2C interface settings, see Section 23.1.1, *HS I2C Overview*.
14. Correct SDCARD_BIAS_VMODE bit.	If the level of SUPPLY_HI_OUT corresponds to the desired value of SDCARD_VDDS, correct the value of the SDCARD_BIAS_VMODE bit.	Modify the value of the CONTROL_PBIAS[21] SDCARD_BIAS_VMODE bit.
15. Correct V1V8_SIGEN bit.	If the level of SUPPLY_HI_OUT corresponds to the desired value of SDCARD_VDDS, correct the value of the V1V8_SIGEN bit.	Modify the value of the MMC1.MMCHS_AC12[19] V1V8_SIGEN bit.
16. Clear interrupt status.	Clear the MPU_IRQ_75 interrupt status flag.	For more information about setting the MPU_IRQ_75 line associated interrupt request PBIAS_IRQ, see Section 17.1, *Interrupt Controllers Overview*.

(1) Must be set low when the external SDCARD_VDDS source is programmed to be 3.0 V, or set to high when the external SDCARD_VDDS source is programmed to be 1.8 V. The reset default value corresponds to 3.0 V.

(2) Must be set high when external SDCARD_VDDS source is programmed to be 3.0 V, or low when the external SDCARD_VDDS source is programmed to be 1.8 V. The reset default value corresponds to 3.0 V.

18.5.1.2.2 Hardware Observability Settings

This section describes the procedures to control the hardware observability features of the device. To configure these features, the programmer must perform the steps listed in Table 18-100.

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Table 18-100. Configure Hardware Observability Features

	Step	Register/Bit Field/Programming Model	Value
1.	Select the hwobs(0)/hwobs(1)/hwobs(2) signal frequency divider value (applies only to po_hw_dbg0, po_hw_dbg1, and po_hw_dbg2 bus signals propagated in the CORE power domain).	CONTROL_HWOBS_CONTROL[7:3] HWOBS_CLKDIV_SEL CONTROL_HWOBS_CONTROL[13:9] HWOBS_CLKDIV_SEL_1 CONTROL_HWOBS_CONTROL[18:14] HWOBS_CLKDIV_SEL_2	0x- (1)
2.	Enable/disable gating of hwobs and alternatively set all hwobs ports to 0 or 1.	.CONTROL_HWOBS_CONTROL[2] HWOBS_ALL_ZERO_MODE CONTROL_HWOBS_CONTROL[1] HWOBS_ALL_ONE_MODE	0x- (2)
3.	Enable/disable hwobs port gating only for signals coming from IPs identified in the MACRO group (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_HWOBS_CONTROL[0] HWOBS_MACRO_ENABLE	0x- (3)
4.	Associate a certain hwobs channel to the CORE or WKUP power domain.	Configure each bit from the CONTROL_DEBOBS_FINAL_MUX_SEL[31:0] SELECT bit field appropriately for its corresponding hw_dbg channel.	0x-
5.	Choose the source of a signal or signal view channel in the CORE power domain.	Configure each CONTROL_CORE_CONF_DEBUG_SEL_TST_0[3:0] MODE through CONTROL_CORE_CONF_DEBUG_SEL_TST_31[3:0] MODE bit field appropriately for its corresponding hw_dbg channel.	0x-
6.	Choose the source of a signal within the WKUP power domain.	Configure each CONTROL_WKUP_CONF_DEBUG_SEL_TST_i[1:0] MODE bit field, (where i = 0 to 31) appropriately for its corresponding hw_dbg channel i (where i = 0 to 31).	0x-
7.	Choose to associate a certain DPLL signal to a given DPLL signal view channel (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_CONF_DPLL_FREQLOCK_SEL[3:0] MULT CONTROL_CONF_DPLL_TINITZ_SEL[3:0] MULT CONTROL_CONF_DPLL_PHASELOCK_SEL[3:0] MULT CONTROL_CONF_DPLL_TENABLE_SEL[3:0] MULT CONTROL_CONF_DPLL_TENABLEDIV_SEL[3:0] MULT CONTROL_CONF_DPLL_BYPASSACK_SEL[3:0] MULT CONTROL_CONF_DPLL_IDLE_SEL[3:0] MULT	0x-
8.	Choose to associate a certain DPLL controller signal to a given DPLL controller signal view channel (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_CONF_DPLLCTRL_PLLLOCK_SEL[2:0] MULT CONTROL_CONF_DPLLCTRL_PLLRECAL_SEL[2:0] MULT CONTROL_CONF_DPLLCTRL_STOPCLOCK_SEL[2:0] MULT CONTROL_CONF_DPLLCTRL_STOPCLOCKACKZ_SEL[2:0] MULT	0x-
9.	Choose to associate a certain MMCx power-management signal to a given MMCx power-management signal view channel (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_CONF_MMCX_ADPIDLE_SEL[2:0] MULT CONTROL_CONF_MMCX_ADPDAT1PADEN_SEL[2:0] MULT CONTROL_CONF_MMCX_OCPL4IDLEREQ_SEL[2:0] MULT CONTROL_CONF_MMCX_OCPL3MWAIT_SEL[2:0] MULT CONTROL_CONF_MMCX_PIRFFRET_SEL[2:0] MULT CONTROL_CONF_MMCX_OCPL4SIDLEACKO1_SEL[2:0] MULT CONTROL_CONF_MMCX_OCPL4SIDLEACKO0_SEL[2:0] MULT CONTROL_CONF_MMCX_OCPL3MSTANDBYO_SEL[2:0] MULT CONTROL_CONF_MMCX_SWAKEUP_SEL[2:0] MULT	0x-
10.	Choose to associate a certain clockout signal to a given clockview channel (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_CONF_CLK_SEL0[3:0] MULT through CONTROL_CONF_CLK_SEL2[3:0] MULT	0x-
11.	Choose to associate an sDMA signal to a given sDMA view channel (applies only to po_hw_dbg bus signals propagated in the CORE power domain).	CONTROL_CONF_SDMA_REQ_SEL0[6:0] MULT through CONTROL_CONF_SDMA_REQ_SEL3[6:0] MULT	0x-

(1) To configure the hwobs(0) channel to operate normally, the value of the HWOBS_CLKDIV_SEL, HWOBS_CLKDIV_SEL_1, or HWOBS_CLKDIV_SEL_2 bit must be set different than 0.

(2) Set both bits to 0 to enable hardware observability. Set only one bit to 1 to gate hwobs ports according to the output state required.

(3) The following subsystems belong to this group: MPU subsystem, IVA and ABE.

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Table 18-100. Configure Hardware Observability Features (continued)

	Step	Register/Bit Field/Programming Model	Value
12.	Set the appropriate pad configuration bit fields to associate the hw_dbgn pad function to output pins and configure additional output pad features.	For more information, see Section 18.4.11, *Hardware Observability*, and Section 18.4.8, *Pad Functional Multiplexing and Configuration*.	For more information, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*.

For more information about the different functions and registers associated with the hardware observability features, see Section 18.4.11, *Hardware Observability*.

18.5.1.2.3 Pad Configuration Programming Points

This section uses an example to describe the configurations of pads necessary for working in active mode.

Perform the follwing steps to configure the pad:

1. Identify interface signals required from the target application.

   Example: Configure the UART3 interface with the required signals: uart3_rx_irrx, uart3_tx_irtx, uart3_cts_rctx, and uart3_rts_irsd.

2. Choose the pads used for those signals. Some signals may be available on several pads and/or may be multiplexed with other signals needed for another application. See Section 18.4.8.3, *Pad Multiplexing Register Fields*.

   Example: Unlike the uart3_rx_irrx and uart3_tx_irtx signals, each of which is available on three pads, the uart3_cts_rctx and uart3_rts_irsd signals are available only on one pad each (MUXMODE = 0x0).

   However, on pad uart3_rx_irrx, the uart3_rx_irrx signal is multiplexed with the sdio4_cmd signal (MUXMODE = 0x4), and on pad uart3_tx_irtx, the uart3_tx_irtx signal is multiplexed with the sdio4_clk signal. The uart3_rx_irrx and uart3_tx_irtx pads are the only pads on which the sdio4_cmd and sdio4_clk signals are available in the device, respectively. Assuming that the SDIO4 interface is required in the system along with UART3 interface, the only way is to choose to multiplex uart3_tx_irtx and uart3_rx_irrx on other pads.

   To preserve SDIO4 capability, the uart3_rx_irrx and uart3_tx_irtx signals can be remapped on alternative pads of the device (for example, the rfbi_data1 and rfbi_data2 pads [with MUXMODE set to 0x4 in the corresponding padconfiguration registers]).

3. Identify the signal integrity parameter settings (drive strength, impedance, slew rate, pullup and pulldown strength, and so forth) necessary for the pads associated with I/O cells, listed in Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*).

   For the register settings of the signal integrity parameters for the uart3_cts_rctx and uart3_rts_irsd pads, see Table 18-85. According to the table, the assigned to uart3_cts_rctx and uart3_rts_irsd pads, software signal parameter controls are:

- CONTROL_SMART1IO_PADCONF_1[7:6] UART3_PART1_DS
- CONTROL_SMART2IO_PADCONF_1[5:4] UART3_PART1_SC

   According to Table 18-85, for the sdio4_clk and sdio4_cmd (available on pads uart3_tx_irtx and uart3_rx_irrx when corresponding padconfiguration MUXMODE bit field is set to 0x4), the following bit fields should be set to tune signal performance:

  - CONTROL_SMART1IO_PADCONF_1[5:4] UART3_PART2_DS
  - CONTROL_SMART2IO_PADCONF_2[31:30] UART3_PART2_SC

   Assuming the uart3_rx_irrx and uart3_tx_irtx signals are mapped on the rfbi_data1 and rfbi_data2 pads (MUXMODE set to 0x4), the following signal integrity parameter control bit fields must be set appropriately:

- CONTROL_SMART1IO_PADCONF_2[19:18] DSS_PART2_DS

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- CONTROL_SMART2IO_PADCONF_0[3:2] DSS_PART2_SC.

NOTE: To identify the signal-associated I/O cell signal parameter settings in Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, the user must search for the device pad name on which the desired signal is muxed, because the I/O cell settings are designated and listed on a per-pad basis. This means that a signal name does not appear (unless MUXMODE = 0x0) in Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, but only the name of the pad on which the signal is muxed. Pads that do not have software I/O cell signal integrity parameter controls are not listed in Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*.

Assume the user application configures the kpd_row6 and kpd_row7 signals on the c2c_datain6 and c2c_datain7 pads (MUXMODE = 0x3). The I/O cell signal parameter control bit fields CONTROL_SMART1IO_PADCONF_0[19:18] C2C_PART1_DS and CONTROL_SMART2IO_PADCONF_0[19:18] C2C_PART1_SC listed in Table 18-79 also apply to the kpd_row6 and kpd_row7 signals.

For recommendations about the mentioned pad group signal integrity parameter settings, see the device data manual.

4. Identify and program the peripheral dual-voltage settings, if they apply to the chosen pads. Table 18-97 lists the corresponding control bits of the pads in the CTRL_MODULE_CORE_PAD.CONTROL_PADCONF_MODE and CTRL_MODULE_WKUP_PAD.CONTROL_WKUP_PADCONF_MODE registers.

The identification of the I/O dual-voltage domains control bits for a signal must be made on a per-pad basis.

The I/O supply voltage (1.2 V/1.8 V) for pads uart3_cts_rctx, uart3_rts_irsd, uart3_rx_irrx (signal sdio4_cmd), and uart3_tx_irtx (signal sdio4_clk) is configured by setting the CTRL_MODULE_CORE_PAD.CONTROL_PADCONF_MODE[23] VDDS_21_MODE bit. Because the uart3_rx_irrx and uart3_tx_irtx signals are multiplexed on the rfbi_data1 and rfbi_data2 pads in MUXMODE = 0x4, the dual-voltage control for these uart3 signals is the dual-voltage control corresponding to the pads – CTRL_MODULE_CORE_PAD.CONTROL_PADCONF_MODE[18] VDDS_9_MODE.

For more information about pad performance dependencies from I/O dual-voltage supply settings, see the device data manual.

5. Identify the pad configuration registers associated with the pads to be used in the application. See Section 18.4.8.3, *Pad Multiplexing Register Fields*.

Example: Under the previous hypothesis, the pad configuration registers to program are:

- uart3_cts_rctx (MUXMODE = 0x0): CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[31:16]
- uart3_rts_irsd (MUXMODE = 0x0): CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[15:0]
- uart3_rx_irrx (MUXMODE = 0x4): CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[15:0]
- uart3_tx_irtx (MUXMODE = 0x4): CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2 [31:16]
- sdio4_clk (MUXMODE = 0x4): CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[31:16]
- sdio4_cmd (MUXMODE = 0x4): CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[15:0]

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Table 18-101. Active Pads Configuration Points

Step	Register/Bit Field/Programming Model	Value
1. Identify the interface signals and map them to the appropriate pads according to the application requirements and the device-specific pad I/O muxing capabilities. See Section 18.4.8.3, *Pad Multiplexing Register Fields*.	Define the list of I/O signal names: uart3_cts_rctx, uart3_rts_irsd, uart3_rx_irrx, uart3_tx_irtx, sdio4_clk and sdio4_cmd. Define the list of corresponding pads used by application: uart3_cts_rctx, uart3_rts_irsd, rfbi_data1, rfbi_data2, uart3_tx_irtx, and uart3_rx_irrx, respectively	–
2. Identify the corresponding I/O cell signal integrity parameter controls for the pad (on a per-pad basis). See Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*.	(uart3_cts_rctx, uart3_rts_irsd pads) CONTROL_SMART1IO_PADCONF_1[7:6] UART3_PART1_DS CONTROL_SMART2IO_PADCONF_1[5:4] UART3_PART1_SC (uart3_rx_irrx, uart3_tx_irtx pads) CONTROL_SMART1IO_PADCONF_1[5:4] UART3_PART2_DS CONTROL_SMART2IO_PADCONF_2[31:30] UART3_PART2_SC (rfbi_data1, rfbi_data2 pads) CONTROL_SMART1IO_PADCONF_2[19:18] DSS_PART2_DS CONTROL_SMART2IO_PADCONF_0[3:2] DSS_PART2_SC	For more information about the recommended I/O settings, see the device data manual
3. Determine whether the pad is associated with a peripheral dual-voltage domain (see the device data manual). Identify its corresponding 1.2-V/1.8-V dual-voltage control bit in the CTRL_MODULE_CORE_PAD.CONTROL_PADCONF_MODE or CTRL_MODULE_WKUP_PAD.CONTROL_PADCONF_MODE registers. For more information, see Table 18-97.	(uart3_cts_rctx, uart3_rts_irsd, uart3_rx_irrx, uart3_tx_irtx) CTRL_MODULE_CORE_PAD.CONTROL_PADCONF_MODE[23] VDDS_21_MODE (rfbi_data1, rfbi_data2) CTRL_MODULE_CORE_PAD.CONTROL_PADCONF_MODE[18] VDDS_9_MODE	For more information about the I/O performance dependency on dual-voltage settings, see the device data manual.
4. Configure MUXMODE field in pad configuration registers associated with the pads used.	(signal uart3_cts_rctx) CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[18:16] UART3_CTS_RCTX_MUXMODE	0x0
	(signal uart3_rts_irsd) CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[2:0] UART3_RTS_IRSD_MUXMODE	0x0
	(signal sdio4_clk) CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[18:16] UART3_TX_IRTX_MUXMODE	0x4
	(signal sdio4_cmd) CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[2:0] UART3_RX_IRRX_MUXMODE	0x4
	(signal uart3_rx_irrx) CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[2:0] RFBI_DATA1_MUXMODE	0x4
	(signal uart3_tx_irtx) CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2[18:16] RFBI_DATA2_MUXMODE	0x4

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Table 18-101. Active Pads Configuration Points (continued)

Step	Register/Bit Field/Programming Model	Value
5. Select the type of the internal pullup/down resistor.(1)	CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[20] UART3_CTS_RCTX_PULLTYPESELECT	0x-
	CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[4] UART3_RTS_IRSD_ PULLTYPESELECT	0x-
	CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[20] UART3_TX_IRTX_ PULLTYPESELECT	0x-
	CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[4] UART3_RX_IRRX_ PULLTYPESELECT	0x-
	CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[4] RFBI_DATA1_PULLTYPESELECT	0x-
	CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2[20] RFBI_DATA2_PULLTYPESELECT	0x-
6. Enable/disable pullup/down feature of the pad. (2)	CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[19] UART3_CTS_RCTX_PULLUDENABLE	0x-
	CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[3] UART3_RTS_IRSD_PULLUDENABLE	0x-
	CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[19] UART3_TX_IRTX_PULLUDENABLE	0x-
	CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[3] UART3_RX_IRRX_PULLUDENABLE	0x-
	CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[3] RFBI_DATA1_PULLUDENABLE	0x-
	CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2[19] RFBI_DATA2_PULLUDENABLE	0x-
7. Set the direction of the pin signal.(2)	CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[24] UART3_CTS_RCTX_INPUTENABLE	0x-
	CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[8] UART3_RTS_IRSD_INPUTENABLE	0x-
	CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[24] UART3_TX_IRTX_INPUTENABLE	0x-
	CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[8] UART3_RX_IRRX_INPUTENABLE	0x-
	CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[8] RFBI_DATA1_INPUTENABLE	0x-
	CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2[24] RFBI_DATA2_INPUTENABLE	0x-
8. Glitch filter enable/disable	The GLITCHGOBBLER bit setting applies to several device pads only (bit is available in several padconfiguration registers, at positions [22] or [6]). It enables/disables I/O cell to filter glitches from outside. The example pads listed in this table do NOT have such setting.	0x-
9. Enable/disable the I/O cell power	CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[21] UART3_CTS_RCTX_PWRDOWN	0x-(3)
	CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[5] UART3_RTS_IRSD_PWRDOWN	0x-(3)
	CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[21] UART3_TX_IRTX_PWRDOWN	0x-(3)
	CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[5] UART3_RX_IRRX_PWRDOWN	0x-(3)
	CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[5] RFBI_DATA1_PWRDOWN	0x-(3)
	CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2[21] RFBI_DATA2_PWRDOWN	0x-(3)

(1) It is recommended to use internal pullup/down resistor if pad is used as input and external pullup/down is not used.
(2) If the pad is configured in output mode, the hardware automatically disables the internal weak pullup/down resistors.
(3) Default (power-on reset) value is 0, which corresponds to I/O cell powered on.

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NOTE: The order for setting the previous pad configuration bits is not important.

NOTE: If a device pad is left unconnected but power is supplied to the I/O cell, it is recommended to keep the corresponding pad configuration bit, CONTROL_CORE/WKUP_PAD0_X_PAD1_Y.INPUTENABLE, set to 0b0. This keeps the input buffer disabled and reduces static current consumption.

NOTE: I/Os are non-failsafe, which means that voltage must never be applied at a pad before the internal I/O supply voltage VDDS is powered.

18.6 Control Module Register Manual

18.6.1 Control Module Instance Summary

Table 18-102. CONTROL MODULE Instance Summary

Module Name	Module Base Address	Size
CTRL_MODULE_CORE	0x4A00 2000	2 KiB
CTRL_MODULE_CORE_PAD	0x4A00 2800	2 KiB
CTRL_MODULE_WKUP	0x4AE0 C000	2 KiB
CTRL_MODULE_WKUP_PAD	0x4AE0 C800	2 KiB

18.6.2 CTRL_MODULE_CORE registers

18.6.2.1 CTRL_MODULE_CORE Register Summary

Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_CORE_REVISION	R	32	0x0000 0000	0x4A00 2000
CONTROL_CORE_HWINFO	R	32	0x0000 0004	0x4A00 2004
CONTROL_CORE_SYSCONFIG	RW	32	0x0000 0010	0x4A00 2010
RESERVED	R	32	0x0000 0100	0x4A00 2100
RESERVED	R	32	0x0000 0104	0x4A00 2104
RESERVED	R	32	0x0000 0108	0x4A00 2108
RESERVED	R	32	0x0000 010C	0x4A00 210C
RESERVED	R	32	0x0000 0110	0x4A00 2110
RESERVED	R	32	0x0000 0114	0x4A00 2114
RESERVED	R	32	0x0000 0118	0x4A00 2118
RESERVED	R	32	0x0000 011C	0x4A00 211C
RESERVED	R	32	0x0000 0120	0x4A00 2120
RESERVED	R	32	0x0000 0124	0x4A00 2124
RESERVED	R	32	0x0000 0128	0x4A00 2128
RESERVED	R	32	0x0000 012C	0x4A00 212C
RESERVED	R	32	0x0000 0130	0x4A00 2130
CONTROL_STATUS	R	32	0x0000 0134	0x4A00 2134

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
RESERVED	R	32	0x0000 0138	0x4A00 2138
RESERVED	R	32	0x0000 013C	0x4A00 213C
RESERVED	R	32	0x0000 0140	0x4A00 2140
RESERVED	R	32	0x0000 0144	0x4A00 2144
CONTROL_SEC_ERR_STATUS_FUNC	R	32	0x0000 0148	0x4A00 2148
RESERVED	R	32	0x0000 014C	0x4A00 214C
CONTROL_SEC_ERR_STATUS_DEBUG	RW	32	0x0000 0150	0x4A00 2150
RESERVED	R	32	0x0000 0154	0x4A00 2154
RESERVED	R	32	0x0000 0158	0x4A00 2158
CONTROL_FORCEWRNP	RW	32	0x0000 015C	0x4A00 215C
RESERVED	R	32	0x0000 0160	0x4A00 2160
RESERVED	R	32	0x0000 0164	0x4A00 2164
RESERVED	R	32	0x0000 0168	0x4A00 2168
RESERVED	R	32	0x0000 016C	0x4A00 216C
RESERVED	R	32	0x0000 0170	0x4A00 2170
RESERVED	R	32	0x0000 0174	0x4A00 2174
RESERVED	R	32	0x0000 0178	0x4A00 2178
RESERVED	R	32	0x0000 017C	0x4A00 217C
RESERVED	R	32	0x0000 0180	0x4A00 2180
RESERVED	R	32	0x0000 0184	0x4A00 2184
RESERVED	R	32	0x0000 0188	0x4A00 2188
RESERVED	R	32	0x0000 018C	0x4A00 218C
RESERVED	R	32	0x0000 0190	0x4A00 2190
CONTROL_STD_FUSE_OPP_VDD_MM_0	R	32	0x0000 0194	0x4A00 2194
CONTROL_STD_FUSE_OPP_VDD_MM_1	R	32	0x0000 0198	0x4A00 2198
CONTROL_STD_FUSE_OPP_VDD_MM_2	R	32	0x0000 019C	0x4A00 219C
CONTROL_STD_FUSE_OPP_VDD_MM_3	R	32	0x0000 01A0	0x4A00 21A0
CONTROL_STD_FUSE_OPP_VDD_MM_4	R	32	0x0000 01A4	0x4A00 21A4
CONTROL_STD_FUSE_OPP_VDD_MM_5	R	32	0x0000 01A8	0x4A00 21A8
CONTROL_STD_FUSE_OPP_VDD_MPU_0	R	32	0x0000 01AC	0x4A00 21AC
CONTROL_STD_FUSE_OPP_VDD_MPU_1	R	32	0x0000 01B0	0x4A00 21B0
CONTROL_STD_FUSE_OPP_VDD_MPU_2	R	32	0x0000 01B4	0x4A00 21B4
CONTROL_STD_FUSE_OPP_VDD_MPU_3	R	32	0x0000 01B8	0x4A00 21B8
CONTROL_STD_FUSE_OPP_VDD_MPU_4	R	32	0x0000 01BC	0x4A00 21BC
CONTROL_STD_FUSE_OPP_VDD_MPU_5	R	32	0x0000 01C0	0x4A00 21C0
CONTROL_STD_FUSE_OPP_VDD_MPU_6	R	32	0x0000 01C4	0x4A00 21C4

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_STD_FUSE_OPP_VDD_MPU_7	R	32	0x0000 01C8	0x4A00 21C8
CONTROL_STD_FUSE_OPP_VDD_CORE_0	R	32	0x0000 01CC	0x4A00 21CC
CONTROL_STD_FUSE_OPP_VDD_CORE_1	R	32	0x0000 01D0	0x4A00 21D0
CONTROL_STD_FUSE_OPP_VDD_CORE_2	R	32	0x0000 01D4	0x4A00 21D4
CONTROL_STD_FUSE_OPP_VDD_CORE_3	R	32	0x0000 01D8	0x4A00 21D8
CONTROL_STD_FUSE_OPP_VDD_CORE_4	R	32	0x0000 01DC	0x4A00 21DC
CONTROL_STD_FUSE_OPP_BGAP_MM	R	32	0x0000 01E0	0x4A00 21E0
CONTROL_STD_FUSE_OPP_BGAP_MPU	R	32	0x0000 01E4	0x4A00 21E4
CONTROL_STD_FUSE_OPP_BGAP_CORE	R	32	0x0000 01E8	0x4A00 21E8
CONTROL_STD_FUSE_OPP_BGAP_MPU23	R	32	0x0000 01EC	0x4A00 21EC
CONTROL_STD_FUSE_DIE_ID_0	R	32	0x0000 0200	0x4A00 2200
RESERVED	R	32	0x0000 0204	0x4A00 2204
CONTROL_STD_FUSE_DIE_ID_1	R	32	0x0000 0208	0x4A00 2208
CONTROL_STD_FUSE_DIE_ID_2	R	32	0x0000 020C	0x4A00 220C
CONTROL_STD_FUSE_DIE_ID_3	R	32	0x0000 0210	0x4A00 2210
CONTROL_STD_FUSE_PROD_ID	R	32	0x0000 0214	0x4A00 2214
CONTROL_STD_FUSE_CONF_ID_0	R	32	0x0000 0218	0x4A00 2218
CONTROL_STD_FUSE_CONF_ID_1	R	32	0x0000 021C	0x4A00 221C
CONTROL_STD_FUSE_MPK_0	R	32	0x0000 0220	0x4A00 2220
CONTROL_STD_FUSE_MPK_1	R	32	0x0000 0224	0x4A00 2224
CONTROL_STD_FUSE_MPK_2	R	32	0x0000 0228	0x4A00 2228
CONTROL_STD_FUSE_MPK_3	R	32	0x0000 022C	0x4A00 222C
CONTROL_STD_FUSE_MPK_4	R	32	0x0000 0230	0x4A00 2230
CONTROL_STD_FUSE_MPK_5	R	32	0x0000 0234	0x4A00 2234
CONTROL_STD_FUSE_MPK_6	R	32	0x0000 0238	0x4A00 2238
CONTROL_STD_FUSE_MPK_7	R	32	0x0000 023C	0x4A00 223C
CONTROL_STD_FUSE_OPP_VDD_MM_LVT_0	R	32	0x0000 0240	0x4A00 2240
CONTROL_STD_FUSE_OPP_VDD_MM_LVT_1	R	32	0x0000 0244	0x4A00 2244

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_STD_FUSE_OPP_VDD_MM_LVT_2	R	32	0x0000 0248	0x4A00 2248
CONTROL_STD_FUSE_OPP_VDD_MM_LVT_3	R	32	0x0000 024C	0x4A00 224C
CONTROL_STD_FUSE_OPP_VDD_MM_LVT_4	R	32	0x0000 0250	0x4A00 2250
CONTROL_STD_FUSE_OPP_VDD_MM_LVT_5	R	32	0x0000 0254	0x4A00 2254
CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_0	R	32	0x0000 0258	0x4A00 2258
CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_1	R	32	0x0000 025C	0x4A00 225C
CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_2	R	32	0x0000 0260	0x4A00 2260
CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_3	R	32	0x0000 0264	0x4A00 2264
CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_4	R	32	0x0000 0268	0x4A00 2268
CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_5	R	32	0x0000 026C	0x4A00 226C
CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_6	R	32	0x0000 0270	0x4A00 2270
CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_7	R	32	0x0000 0274	0x4A00 2274
RESERVED	R	32	0x0000 028C	0x4A00 228C
RESERVED	R	32	0x0000 0290	0x4A00 2290
RESERVED	R	32	0x0000 0294	0x4A00 2294
RESERVED	R	32	0x0000 0298	0x4A00 2298
RESERVED	R	32	0x0000 029C	0x4A00 229C
RESERVED	R	32	0x0000 02A0	0x4A00 22A0
RESERVED	R	32	0x0000 02A4	0x4A00 22A4
RESERVED	R	32	0x0000 02A8	0x4A00 22A8
RESERVED	R	32	0x0000 02AC	0x4A00 22AC
RESERVED	R	32	0x0000 02B0	0x4A00 22B0
RESERVED	R	32	0x0000 02B4	0x4A00 22B4
RESERVED	R	32	0x0000 02B8	0x4A00 22B8
CONTROL_CUST_FUSE_SWRV_0	R	32	0x0000 02BC	0x4A00 22BC
CONTROL_CUST_FUSE_SWRV_1	R	32	0x0000 02C0	0x4A00 22C0
CONTROL_CUST_FUSE_SWRV_2	R	32	0x0000 02C4	0x4A00 22C4
CONTROL_CUST_FUSE_SWRV_3	R	32	0x0000 02C8	0x4A00 22C8
CONTROL_CUST_FUSE_SWRV_4	R	32	0x0000 02CC	0x4A00 22CC

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_CUST_FUSE_SWRV_5	R	32	0x0000 02D0	0x4A00 22D0
CONTROL_CUST_FUSE_SWRV_6	R	32	0x0000 02D4	0x4A00 22D4
CONTROL_HWOBSDIVIDER1	RW	32	0x0000 02D8	0x4A00 22D8
CONTROL_HWOBSDIVIDER2	RW	32	0x0000 02DC	0x4A00 22DC
RESERVED	R	32	0x0000 02E0	0x4A00 22E0
RESERVED	R	32	0x0000 02E4	0x4A00 22E4
RESERVED	R	32	0x0000 02E8	0x4A00 22E8
RESERVED	R	32	0x0000 02EC	0x4A00 22EC
CONTROL_DEV_CONF	RW	32	0x0000 0300	0x4A00 2300
CONTROL_DSP_BOOTADDR	RW	32	0x0000 0304	0x4A00 2304
RESERVED	R	32	0x0000 0314	0x4A00 2314
RESERVED	R	32	0x0000 0318	0x4A00 2318
RESERVED	R	32	0x0000 031C	0x4A00 231C
RESERVED	R	32	0x0000 0324	0x4A00 2324
RESERVED	R	32	0x0000 0328	0x4A00 2328
CONTROL_TEMP_SENSOR_MPU	RW	32	0x0000 032C	0x4A00 232C
CONTROL_TEMP_SENSOR_MM	RW	32	0x0000 0330	0x4A00 2330
CONTROL_TEMP_SENSOR_CORE	RW	32	0x0000 0334	0x4A00 2334
CONTROL_LDOSRAM_MPU_LVT_VOLTAGE_CTRL	RW	32	0x0000 0338	0x4A00 2338
RESERVED	R	32	0x0000 033C	0x4A00 233C
RESERVED	R	32	0x0000 0340	0x4A00 2340
RESERVED	R	32	0x0000 0344	0x4A00 2344
RESERVED	RW	32	0x0000 0348	0x4A00 2348
RESERVED	RW	32	0x0000 034C	0x4A00 234C
RESERVED	RW	32	0x0000 0350	0x4A00 2350
CONTROL_CORTEX_M4_MMUADDRTRANSLTR	RW	32	0x0000 0358	0x4A00 2358
CONTROL_CORTEX_M4_MMUADDRLOGICTR	RW	32	0x0000 035C	0x4A00 235C
CONTROL_HWOBS_CONTROL	RW	32	0x0000 0360	0x4A00 2360
RESERVED	R	32	0x0000 0364	0x4A00 2364
RESERVED	R	32	0x0000 0368	0x4A00 2368
RESERVED	R	32	0x0000 036C	0x4A00 236C
CONTROL_PHY_POWER_USB	RW	32	0x0000 0370	0x4A00 2370
CONTROL_PHY_POWER_SATA	RW	32	0x0000 0374	0x4A00 2374
RESERVED	R	32	0x0000 0378	0x4A00 2378
RESERVED	R	32	0x0000 037C	0x4A00 237C

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_BANDGAP_MASK	RW	32	0x0000 0380	0x4A00 2380
CONTROL_BANDGAP_THRESHOLD_MPU	RW	32	0x0000 0384	0x4A00 2384
CONTROL_BANDGAP_THRESHOLD_MM	RW	32	0x0000 0388	0x4A00 2388
CONTROL_BANDGAP_THRESHOLD_CORE	RW	32	0x0000 038C	0x4A00 238C
CONTROL_BANDGAP_TSHUT_MPU	RW	32	0x0000 0390	0x4A00 2390
CONTROL_BANDGAP_TSHUT_MM	RW	32	0x0000 0394	0x4A00 2394
CONTROL_BANDGAP_TSHUT_CORE	RW	32	0x0000 0398	0x4A00 2398
CONTROL_BANDGAP_CUMUL_DTEMP_MPU	R	32	0x0000 039C	0x4A00 239C
CONTROL_BANDGAP_CUMUL_DTEMP_MM	R	32	0x0000 03A0	0x4A00 23A0
CONTROL_BANDGAP_CUMUL_DTEMP_CORE	R	32	0x0000 03A4	0x4A00 23A4
CONTROL_BANDGAP_STATUS	R	32	0x0000 03A8	0x4A00 23A8
CONTROL_SATA_EXT_MODE	RW	32	0x0000 03AC	0x4A00 23AC
RESERVED	R	32	0x0000 03B0	0x4A00 23B0
RESERVED	R	32	0x0000 03B4	0x4A00 23B4
RESERVED	R	32	0x0000 03B8	0x4A00 23B8
RESERVED	R	32	0x0000 03BC	0x4A00 23BC
CONTROL_DTEMP_MPU_0	R	32	0x0000 03C0	0x4A00 23C0
CONTROL_DTEMP_MPU_1	R	32	0x0000 03C4	0x4A00 23C4
CONTROL_DTEMP_MPU_2	R	32	0x0000 03C8	0x4A00 23C8
CONTROL_DTEMP_MPU_3	R	32	0x0000 03CC	0x4A00 23CC
CONTROL_DTEMP_MPU_4	R	32	0x0000 03D0	0x4A00 23D0
CONTROL_DTEMP_MM_0	R	32	0x0000 03D4	0x4A00 23D4
CONTROL_DTEMP_MM_1	R	32	0x0000 03D8	0x4A00 23D8
CONTROL_DTEMP_MM_2	R	32	0x0000 03DC	0x4A00 23DC
CONTROL_DTEMP_MM_3	R	32	0x0000 03E0	0x4A00 23E0
CONTROL_DTEMP_MM_4	R	32	0x0000 03E4	0x4A00 23E4
CONTROL_DTEMP_CORE_0	R	32	0x0000 03E8	0x4A00 23E8
CONTROL_DTEMP_CORE_1	R	32	0x0000 03EC	0x4A00 23EC
CONTROL_DTEMP_CORE_2	R	32	0x0000 03F0	0x4A00 23F0

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_DTEMP_CORE_3	R	32	0x0000 03F4	0x4A00 23F4
CONTROL_DTEMP_CORE_4	R	32	0x0000 03F8	0x4A00 23F8
CONTROL_OCPREG_SPARE	RW	32	0x0000 03FC	0x4A00 23FC
CONTROL_DEBOBS_FINAL_MUX_SEL	RW	32	0x0000 0400	0x4A00 2400
CONTROL_DEBOBS_OCPWP_SYS_EVENT_SEL	RW	32	0x0000 0404	0x4A00 2404
CONTROL_DEBOBS_MMR_MPU	RW	32	0x0000 0408	0x4A00 2408
RESERVED	RW	32	0x0000 0410	0x4A00 2410
RESERVED	RW	32	0x0000 0414	0x4A00 2414
RESERVED	RW	32	0x0000 0418	0x4A00 2418
RESERVED	RW	32	0x0000 041C	0x4A00 241C
RESERVED	RW	32	0x0000 0420	0x4A00 2420
RESERVED	RW	32	0x0000 0424	0x4A00 2424
CONTROL_CONF_SDMA_REQ_SEL0	RW	32	0x0000 042C	0x4A00 242C
CONTROL_CONF_SDMA_REQ_SEL1	RW	32	0x0000 0430	0x4A00 2430
CONTROL_CONF_SDMA_REQ_SEL2	RW	32	0x0000 0434	0x4A00 2434
CONTROL_CONF_SDMA_REQ_SEL3	RW	32	0x0000 0438	0x4A00 2438
CONTROL_CONF_CLK_SEL0	RW	32	0x0000 0440	0x4A00 2440
CONTROL_CONF_CLK_SEL1	RW	32	0x0000 0444	0x4A00 2444
CONTROL_CONF_CLK_SEL2	RW	32	0x0000 0448	0x4A00 2448
CONTROL_CONF_DPLL_FREQLOCK_SEL	RW	32	0x0000 044C	0x4A00 244C
CONTROL_CONF_DPLL_TINITZ_SEL	RW	32	0x0000 0450	0x4A00 2450
CONTROL_CONF_DPLL_PHASELOCK_SEL	RW	32	0x0000 0454	0x4A00 2454
CONTROL_CONF_DPLL_TENABLE_SEL	RW	32	0x0000 0458	0x4A00 2458
CONTROL_CONF_DPLL_TENABLEDIV_SEL	RW	32	0x0000 045C	0x4A00 245C
CONTROL_CONF_DPLL_BYPASSACK_SEL	RW	32	0x0000 0460	0x4A00 2460
CONTROL_CONF_DPLL_IDLE_SEL	RW	32	0x0000 0464	0x4A00 2464
CONTROL_CONF_DPLCTRL_PLLLOCK_SEL	RW	32	0x0000 0468	0x4A00 2468
CONTROL_CONF_DPLCTRL_PLLRECAL_SEL	RW	32	0x0000 046C	0x4A00 246C
CONTROL_CONF_DPLCTRL_STOPCLOCK_SEL	RW	32	0x0000 0470	0x4A00 2470

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_CONF_DPLLCTRL_STOPCLOCKACKZ_SEL	RW	32	0x0000 0474	0x4A00 2474
CONTROL_CONF_DPLLCTRL_DISPCUPDATESYNC_SEL	RW	32	0x0000 0478	0x4A00 2478
RESERVED	RW	32	0x0000 047C	0x4A00 247C
RESERVED	RW	32	0x0000 0480	0x4A00 2480
RESERVED	RW	32	0x0000 0484	0x4A00 2484
RESERVED	RW	32	0x0000 0488	0x4A00 2488
RESERVED	RW	32	0x0000 048C	0x4A00 248C
RESERVED	RW	32	0x0000 0490	0x4A00 2490
RESERVED	RW	32	0x0000 0494	0x4A00 2494
RESERVED	RW	32	0x0000 0498	0x4A00 2498
RESERVED	RW	32	0x0000 049C	0x4A00 249C
RESERVED	RW	32	0x0000 04A0	0x4A00 24A0
CONTROL_CONF_MMCX_ADPIDLE_SEL	RW	32	0x0000 04AC	0x4A00 24AC
CONTROL_CONF_MMCX_ADPDAT1PADEN_SEL	RW	32	0x0000 04B0	0x4A00 24B0
CONTROL_CONF_MMCX_OCPL4IDLEREQ_SEL	RW	32	0x0000 04B4	0x4A00 24B4
CONTROL_CONF_MMCX_OCPL3MWAIT_SEL	RW	32	0x0000 04B8	0x4A00 24B8
CONTROL_CONF_MMCX_PIRFFRET_SEL	RW	32	0x0000 04BC	0x4A00 24BC
CONTROL_CONF_MMCX_OCPL4SIDLEACKO1_SEL	RW	32	0x0000 04C0	0x4A00 24C0
CONTROL_CONF_MMCX_OCPL4SIDLEACKO0_SEL	RW	32	0x0000 04C4	0x4A00 24C4
CONTROL_CONF_MMCX_OCPL3MSTANDBYO_SEL	RW	32	0x0000 04C8	0x4A00 24C8
CONTROL_CONF_MMCX_SWAKEUP_SEL	RW	32	0x0000 04CC	0x4A00 24CC
CONTROL_CORE_CONF_DEBUG_SEL_TST_0	RW	32	0x0000 04D0	0x4A00 24D0
CONTROL_CORE_CONF_DEBUG_SEL_TST_1	RW	32	0x0000 04D4	0x4A00 24D4
CONTROL_CORE_CONF_DEBUG_SEL_TST_2	RW	32	0x0000 04D8	0x4A00 24D8
CONTROL_CORE_CONF_DEBUG_SEL_TST_3	RW	32	0x0000 04DC	0x4A00 24DC
CONTROL_CORE_CONF_DEBUG_SEL_TST_4	RW	32	0x0000 04E0	0x4A00 24E0

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_CORE_CONF_DEBUG_SEL_TST_5	RW	32	0x0000 04E4	0x4A00 24E4
CONTROL_CORE_CONF_DEBUG_SEL_TST_6	RW	32	0x0000 04E8	0x4A00 24E8
CONTROL_CORE_CONF_DEBUG_SEL_TST_7	RW	32	0x0000 04EC	0x4A00 24EC
CONTROL_CORE_CONF_DEBUG_SEL_TST_8	RW	32	0x0000 04F0	0x4A00 24F0
CONTROL_CORE_CONF_DEBUG_SEL_TST_9	RW	32	0x0000 04F4	0x4A00 24F4
CONTROL_CORE_CONF_DEBUG_SEL_TST_10	RW	32	0x0000 04F8	0x4A00 24F8
CONTROL_CORE_CONF_DEBUG_SEL_TST_11	RW	32	0x0000 04FC	0x4A00 24FC
CONTROL_CORE_CONF_DEBUG_SEL_TST_12	RW	32	0x0000 0500	0x4A00 2500
CONTROL_CORE_CONF_DEBUG_SEL_TST_13	RW	32	0x0000 0504	0x4A00 2504
CONTROL_CORE_CONF_DEBUG_SEL_TST_14	RW	32	0x0000 0508	0x4A00 2508
CONTROL_CORE_CONF_DEBUG_SEL_TST_15	RW	32	0x0000 050C	0x4A00 250C
CONTROL_CORE_CONF_DEBUG_SEL_TST_16	RW	32	0x0000 0510	0x4A00 2510
CONTROL_CORE_CONF_DEBUG_SEL_TST_17	RW	32	0x0000 0514	0x4A00 2514
CONTROL_CORE_CONF_DEBUG_SEL_TST_18	RW	32	0x0000 0518	0x4A00 2518
CONTROL_CORE_CONF_DEBUG_SEL_TST_19	RW	32	0x0000 051C	0x4A00 251C
CONTROL_CORE_CONF_DEBUG_SEL_TST_20	RW	32	0x0000 0520	0x4A00 2520
CONTROL_CORE_CONF_DEBUG_SEL_TST_21	RW	32	0x0000 0524	0x4A00 2524
CONTROL_CORE_CONF_DEBUG_SEL_TST_22	RW	32	0x0000 0528	0x4A00 2528
CONTROL_CORE_CONF_DEBUG_SEL_TST_23	RW	32	0x0000 052C	0x4A00 252C

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_CORE_CONF_DEBUG_SEL_TST_24	RW	32	0x0000 0530	0x4A00 2530
CONTROL_CORE_CONF_DEBUG_SEL_TST_25	RW	32	0x0000 0534	0x4A00 2534
CONTROL_CORE_CONF_DEBUG_SEL_TST_26	RW	32	0x0000 0538	0x4A00 2538
CONTROL_CORE_CONF_DEBUG_SEL_TST_27	RW	32	0x0000 053C	0x4A00 253C
CONTROL_CORE_CONF_DEBUG_SEL_TST_28	RW	32	0x0000 0540	0x4A00 2540
CONTROL_CORE_CONF_DEBUG_SEL_TST_29	RW	32	0x0000 0544	0x4A00 2544
CONTROL_CORE_CONF_DEBUG_SEL_TST_30	RW	32	0x0000 0548	0x4A00 2548
CONTROL_CORE_CONF_DEBUG_SEL_TST_31	RW	32	0x0000 054C	0x4A00 254C
RESERVED	R	32	0x0000 0550	0x4A00 2550
RESERVED	R	32	0x0000 0554	0x4A00 2554
RESERVED	R	32	0x0000 0558	0x4A00 2558
RESERVED	R	32	0x0000 055C	0x4A00 255C
RESERVED	R	32	0x0000 0560	0x4A00 2560
RESERVED	R	32	0x0000 0564	0x4A00 2564
RESERVED	R	32	0x0000 0568	0x4A00 2568
RESERVED	R	32	0x0000 056C	0x4A00 256C
RESERVED	R	32	0x0000 0570	0x4A00 2570
RESERVED	R	32	0x0000 0574	0x4A00 2574
RESERVED	R	32	0x0000 0578	0x4A00 2578
RESERVED	R	32	0x0000 057C	0x4A00 257C
RESERVED	R	32	0x0000 0580	0x4A00 2580
RESERVED	R	32	0x0000 0584	0x4A00 2584
RESERVED	R	32	0x0000 0588	0x4A00 2588
RESERVED	R	32	0x0000 058C	0x4A00 258C
CONTROL_CORE_CONF_XBAR_SEL_0	RW	32	0x0000 05DC	0x4A00 25DC
CONTROL_CORE_CONF_XBAR_SEL_4	RW	32	0x0000 05E0	0x4A00 25E0
CONTROL_CORE_CONF_XBAR_SEL_8	RW	32	0x0000 05E4	0x4A00 25E4
CONTROL_CORE_CONF_XBAR_SEL_12	RW	32	0x0000 05E8	0x4A00 25E8
CONTROL_CORE_CONF_XBAR_SEL_16	RW	32	0x0000 05EC	0x4A00 25EC
CONTROL_CORE_CONF_XBAR_SEL_20	RW	32	0x0000 05F0	0x4A00 25F0
CONTROL_CORE_CONF_XBAR_SEL_24	RW	32	0x0000 05F4	0x4A00 25F4

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Table 18-103. CTRL_MODULE_CORE Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE Base Address
CONTROL_CORE_CONF_XBAR_SEL_28	RW	32	0x0000 05F8	0x4A00 25F8
CONTROL_CORE_CONF_XBAR_BYPASS	RW	32	0x0000 05FC	0x4A00 25FC

18.6.2.2 CTRL_MODULE_CORE Register Description

Table 18-104. CONTROL_CORE_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A00 2000	**Instance**	CTRL_MODULE_CORE
Description	Control module revision identifier Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISON																															

Bits	Field Name	Description	Type	Reset
31:0	REVISON	IP Revision	R	TI Internal data

Table 18-105. Register Call Summary for Register CONTROL_CORE_REVISION

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-106. CONTROL_CORE_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A00 2004	**Instance**	CTRL_MODULE_CORE
Description	Information about the IP module hardware configuration i.e. typically the module HDL generics (if any). Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	IP_HWINFO	IP-module dependent	R	0x0000 0000

Table 18-107. Register Call Summary for Register CONTROL_CORE_HWINFO

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

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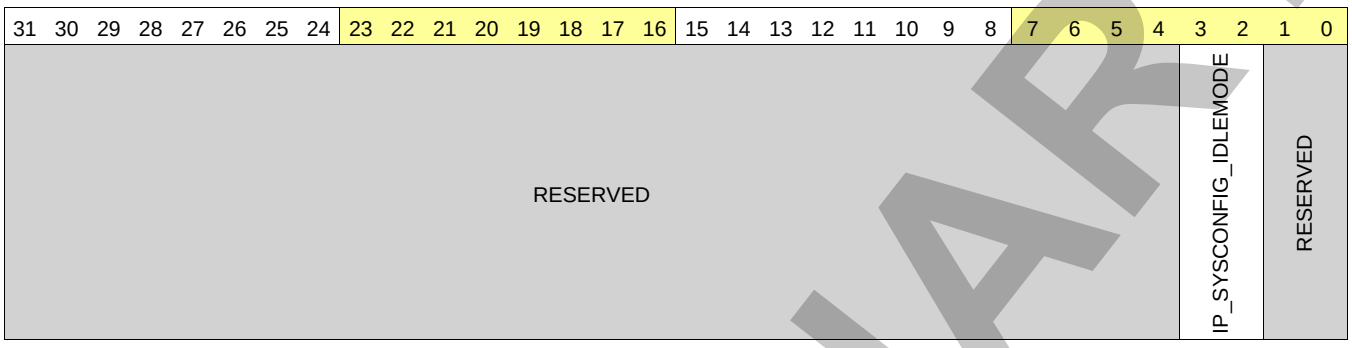
Table 18-108. CONTROL_CORE_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A00 2010	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:2	IP_SYSCONFIG_IDLEMODE	RESERVED (not used).	RW	0x2
1:0	RESERVED		R	0x0

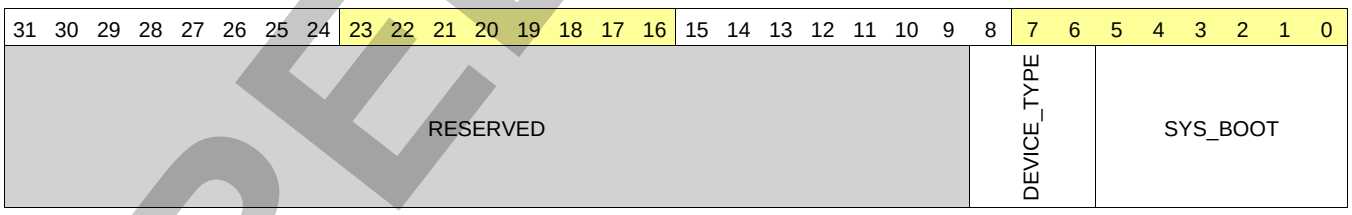
Table 18-109. Register Call Summary for Register CONTROL_CORE_SYSCONFIG

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-110. CONTROL_STATUS

Address Offset	0x0000 0134		
Physical Address	0x4A00 2134	**Instance**	CTRL_MODULE_CORE
Description	Control Module Status Register Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		



Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8:6	DEVICE_TYPE	Device type captured at reset time Device type value sampled at power-on reset. Read 0x3: General Purpose (GP)	R	0x0
5:0	SYS_BOOT	Sys.Boot pins state captured at reset time Sys.Boot pin values sampled at power-on reset	R	0x00

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Table 18-111. Register Call Summary for Register CONTROL_STATUS

Control Module Integration • Control Module Integration: [0]
Control Module Functional Description • Control Module Initialization: [1] • General Core Control Module Instance: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-112. CONTROL_SEC_ERR_STATUS_FUNC

Address Offset	0x0000 0148		
Physical Address	0x4A00 2148	**Instance**	CTRL_MODULE_CORE
Description	Firewall Error Status functional Register Access conditions. Read Only		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BB2D_FW_ERROR	L4_WAKEUP_FW_ERROR	RESERVED		AUDIOSS_FW_ERROR	DEBUGSS_FW_ERROR	L4_CONFIG_FW_ERROR	L4_PERIPH_FW_ERROR	ISS_FW_ERROR	DSS_FW_ERROR	GPU_FW_ERROR	RESERVED		DISPDMA_ACC_ERROR	RESERVED	SYSTEMDMA_ACC_ERROR	RESERVED	IVAHD_SL2_FW_ERROR	DUAL_CORTEX_M4_FW_ERROR	IVAHD_FW_ERROR	EMIF_FW_ERROR	GPMC_FW_ERROR	L3RAM_FW_ERROR	RESERVED

Table 18-113. Register Call Summary for Register CONTROL_SEC_ERR_STATUS_FUNC

Control Module Functional Description • Protection Status Registers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [11] [12] [13] [14] [15] [16] [17] [19] [20]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [21]

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	BB2D_FW_ERROR	BB2D firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
22	L4_WAKEUP_FW_ERROR	L4 wakeup firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
21:20	RESERVED		R	0
19	AUDIOSS_FW_ERROR	AUDIOSS firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
18	DEBUGSS_FW_ERROR	DebugSS firewall 0x0: No error from firewall 0x1: Error from firewall	R	0

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Bits	Field Name	Description	Type	Reset
17	L4_CONFIG_FW_ERROR	L4 config firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
16	L4_PERIPH_FW_ERROR	L4 periph firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
15	ISS_FW_ERROR	ISS firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
14	DSS_FW_ERROR	DSS firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
13	GPU_FW_ERROR	GPU firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
12:11	RESERVED		R	0
10	DISPDMA_ACC_ERROR	DISPDMA target firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
9	RESERVED		R	0
8	SYSTEMDMA_ACC_ERROR	SYSTEMDMA target firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
7	RESERVED		R	0
6	IVAHD_SL2_FW_ERROR	IVAHD SL2 firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
5	DUAL_CORTEX_M4_FW_ERRO R	Dual Cortex M4 firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
4	IVAHD_FW_ERROR	IVAHD firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
3	EMIF_FW_ERROR	EMIF firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
2	GPMC_FW_ERROR	GPMC firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
1	L3RAM_FW_ERROR	L3RAM firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
0	RESERVED		R	0

Table 18-114. CONTROL_SEC_ERR_STATUS_DEBUG

Address Offset	0x0000 0150		
Physical Address	0x4A00 2150	**Instance**	CTRL_MODULE_CORE
Description	Firewall Error Status debug Register. Access conditions. Read: unrestricted, Write: unrestricted		

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Table 18-114. CONTROL_SEC_ERR_STATUS_DEBUG (continued)

Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BB2D_DBGFW_ERROR	L4_WAKEUP_DBGFW_ERROR	RESERVED		AUDIOSS_DBGFW_ERROR	DEBUGSS_DBGFW_ERROR	L4_CONFIG_DBGFW_ERROR	L4_PERIPH_DBGFW_ERROR	ISS_DBGFW_ERROR	DSS_DBGFW_ERROR	GPU_DBGFW_ERROR	RESERVED					IVAHD_SL2_DBGFW_ERROR	DUAL_CORTEX_M4_DBGFW_ERROR	IVAHD_DBGFW_ERROR	EMIF_DBGFW_ERROR	GPMC_DBGFW_ERROR	L3RAM_DBGFW_ERROR	RESERVED	

Table 18-115. Register Call Summary for Register CONTROL_SEC_ERR_STATUS_DEBUG

Control Module Functional Description

- Protection Status Registers: [0] [1] [2] [3] [4] [5] [6] [7] [9] [10] [11] [12] [13] [14] [15] [17] [18]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [19]

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23	BB2D_DBGFW_ERROR	BB2D debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
22	L4_WAKEUP_DBGFW_ERROR	L4 wakeup debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
21:20	RESERVED		R	0
19	AUDIOSS_DBGFW_ERROR	AUDIOSS debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
18	DEBUGSS_DBGFW_ERROR	DebugSS debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
17	L4_CONFIG_DBGFW_ERROR	L4 config debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
16	L4_PERIPH_DBGFW_ERROR	L4 periph debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
15	ISS_DBGFW_ERROR	ISS debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
14	DSS_DBGFW_ERROR	DSS debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
13	GPU_DBGFW_ERROR	GPU debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
12:7	RESERVED		R	0x0
6	IVAHD_SL2_DBGFW_ERROR	IVAHD SL2 debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
5	DUAL_CORTEX_M4_DBGFW_ERROR	Dual Cortex M4 debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
4	IVAHD_DBGFW_ERROR	IVAHD debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
3	EMIF_DBGFW_ERROR	EMIF debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
2	GPMC_DBGFW_ERROR	GPMC debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
1	L3RAM_DBGFW_ERROR	L3RAM debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW W1toClr	0
0	RESERVED		R	0

Table 18-116. CONTROL_FORCEWRNP

Address Offset	0x0000 015C		
Physical Address	0x4A00 215C	**Instance**	CTRL_MODULE_CORE
Description	FORCE WRITE NON POSTED Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															MPU_FORCEWRNP

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MPU_FORCEWRNP	Force mpu write non posted 0x0: disable force wrnp 0x1: force wrnp	RW	0

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Table 18-117. Register Call Summary for Register CONTROL_FORCEWRNP

Control Module Functional Description
• Force MPU Write Nonposted Transactions Control Register: [0]
Control Module Register Manual
• CTRL_MODULE_CORE Register Summary: [1]

Table 18-118. CONTROL_STD_FUSE_OPP_VDD_MM_0

Address Offset	0x0000 0194		
Physical Address	0x4A00 2194	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MM [31:0]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_0																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_0		R	0x0000 0000

Table 18-119. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_0

Control Module Register Manual
• CTRL_MODULE_CORE Register Summary: [0]

Table 18-120. CONTROL_STD_FUSE_OPP_VDD_MM_1

Address Offset	0x0000 0198		
Physical Address	0x4A00 2198	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MM [63:32]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_1		R	0x0000 0000

Table 18-121. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_1

Control Module Register Manual
• CTRL_MODULE_CORE Register Summary: [0]

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Table 18-122. CONTROL_STD_FUSE_OPP_VDD_MM_2

Address Offset	0x0000 019C		
Physical Address	0x4A00 219C	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MM [95:64]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_2																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_2		R	0x0000 0000

Table 18-123. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_2

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-124. CONTROL_STD_FUSE_OPP_VDD_MM_3

Address Offset	0x0000 01A0		
Physical Address	0x4A00 21A0	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MM [127:96]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_3																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_3		R	0x0000 0000

Table 18-125. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_3

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-126. CONTROL_STD_FUSE_OPP_VDD_MM_4

Address Offset	0x0000 01A4		
Physical Address	0x4A00 21A4	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MM [159:128]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_4																															

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Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_4		R	0x0000 0000

Table 18-127. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_4

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-128. CONTROL_STD_FUSE_OPP_VDD_MM_5

Address Offset	0x0000 01A8		
Physical Address	0x4A00 21A8	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MM [191:160]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_5																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_5		R	0x0000 0000

Table 18-129. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_5

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-130. CONTROL_STD_FUSE_OPP_VDD_MPU_0

Address Offset	0x0000 01AC		
Physical Address	0x4A00 21AC	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MPU [31:0]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_0																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_0		R	0x0000 0000

Table 18-131. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_0

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- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-132. CONTROL_STD_FUSE_OPP_VDD_MPU_1

Address Offset	0x0000 01B0		
Physical Address	0x4A00 21B0	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MPU [63:32]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_1		R	0x0000 0000

Table 18-133. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_1

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-134. CONTROL_STD_FUSE_OPP_VDD_MPU_2

Address Offset	0x0000 01B4		
Physical Address	0x4A00 21B4	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MPU [95:64]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_2																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_2		R	0x0000 0000

Table 18-135. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_2

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-136. CONTROL_STD_FUSE_OPP_VDD_MPU_3

Address Offset	0x0000 01B8		
Physical Address	0x4A00 21B8	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MPU [127:96]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_3																															

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Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_3		R	0x0000 0000

Table 18-137. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_3

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-138. CONTROL_STD_FUSE_OPP_VDD_MPU_4

Address Offset	0x0000 01BC		
Physical Address	0x4A00 21BC	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MPU [159:128]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_4																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_4		R	0x0000 0000

Table 18-139. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_4

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-140. CONTROL_STD_FUSE_OPP_VDD_MPU_5

Address Offset	0x0000 01C0		
Physical Address	0x4A00 21C0	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MPU [191:160]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_5																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_5		R	0x0000 0000

Table 18-141. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_5

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-142. CONTROL_STD_FUSE_OPP_VDD_MPU_6

Address Offset	0x0000 01C4		
Physical Address	0x4A00 21C4	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MPU [223:192]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_6																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_6		R	0x0000 0000

Table 18-143. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_6

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-144. CONTROL_STD_FUSE_OPP_VDD_MPU_7

Address Offset	0x0000 01C8		
Physical Address	0x4A00 21C8	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_MPU [255:224]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_7																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_7		R	0x0000 0000

Table 18-145. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_7

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-146. CONTROL_STD_FUSE_OPP_VDD_CORE_0

Address Offset	0x0000 01CC		
Physical Address	0x4A00 21CC	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_CORE [31:0]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_CORE_0																															

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Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_CORE_0		R	0x0000 0000

Table 18-147. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_0

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-148. CONTROL_STD_FUSE_OPP_VDD_CORE_1

Address Offset	0x0000 01D0		
Physical Address	0x4A00 21D0	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_CORE [63:32]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_CORE_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_CORE_1		R	0x0000 0000

Table 18-149. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_1

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-150. CONTROL_STD_FUSE_OPP_VDD_CORE_2

Address Offset	0x0000 01D4		
Physical Address	0x4A00 21D4	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_CORE [95:64]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_CORE_2																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_CORE_2		R	0x0000 0000

Table 18-151. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_2

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-152. CONTROL_STD_FUSE_OPP_VDD_CORE_3

Address Offset	0x0000 01D8		
Physical Address	0x4A00 21D8	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_CORE [127:96]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_CORE_3																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_CORE_3		R	0x0000 0000

Table 18-153. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_3

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-154. CONTROL_STD_FUSE_OPP_VDD_CORE_4

Address Offset	0x0000 01DC		
Physical Address	0x4A00 21DC	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP VDD_CORE [159:128]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_CORE_4																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_CORE_4		R	0x0000 0000

Table 18-155. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_4

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-156. CONTROL_STD_FUSE_OPP_BGAP_MM

Address Offset	0x0000 01E0		
Physical Address	0x4A00 21E0	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP BGAP MM. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_BGAP_MM																															

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Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_BGAP_MM		R	0x0000 0000

Table 18-157. Register Call Summary for Register CONTROL_STD_FUSE_OPP_BGAP_MM

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-158. CONTROL_STD_FUSE_OPP_BGAP_MPU

Address Offset	0x0000 01E4		
Physical Address	0x4A00 21E4	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP BGAP BGAP. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_BGAP_MPU																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_BGAP_MPU		R	0x0000 0000

Table 18-159. Register Call Summary for Register CONTROL_STD_FUSE_OPP_BGAP_MPU

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-160. CONTROL_STD_FUSE_OPP_BGAP_CORE

Address Offset	0x0000 01E8		
Physical Address	0x4A00 21E8	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP BGAP CORE. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_BGAP_CORE																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_BGAP_CORE		R	0x0000 0000

Table 18-161. Register Call Summary for Register CONTROL_STD_FUSE_OPP_BGAP_CORE

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-162. CONTROL_STD_FUSE_OPP_BGAP_MPU23

Address Offset	0x0000 01EC		
Physical Address	0x4A00 21EC	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse OPP BGAP MPU3. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		

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Table 18-162. CONTROL_STD_FUSE_OPP_BGAP_MPU23 (continued)

Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_BGAP_MPU3																STD_FUSE_OPP_BGAP_MPU2															

Bits	Field Name	Description	Type	Reset
31:16	STD_FUSE_OPP_BGAP_MPU3		R	0x0000
15:0	STD_FUSE_OPP_BGAP_MPU2		R	0x0000

Table 18-163. Register Call Summary for Register CONTROL_STD_FUSE_OPP_BGAP_MPU23

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-164. CONTROL_STD_FUSE_DIE_ID_0

Address Offset	0x0000 0200		
Physical Address	0x4A00 2200	Instance	CTRL_MODULE_CORE
Description	Die ID Register - Part 0. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_DIE_ID_0																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_DIE_ID_0		R	0x0000 0000

Table 18-165. Register Call Summary for Register CONTROL_STD_FUSE_DIE_ID_0

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-166. ID_CODE

Address Offset	0x0000 0204		
Physical Address	Please refer to Table 18-103	Instance	CTRL_MODULE_CORE
Description	ID_CODE Key Register. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Field Name	Description	Type	Reset
31:0	ID_CODE		R	0x0000 0000

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Table 18-167. Register Call Summary for Register ID_CODE

Control Module Register Manual

- CTRL_MODULE_CORE Register Description: [0] [1]
- CTRL_MODULE_WKUP Register Description: [2]

Table 18-168. CONTROL_STD_FUSE_DIE_ID_1

Address Offset	0x0000 0208		
Physical Address	0x4A00 2208	**Instance**	CTRL_MODULE_CORE
Description	Die ID Register - Part 1. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. For more information, see Section 1.5 *OMAP543x Family and Device Identification* Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_DIE_ID_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_DIE_ID_1		R	0x0000 0000

Table 18-169. Register Call Summary for Register CONTROL_STD_FUSE_DIE_ID_1

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-170. CONTROL_STD_FUSE_DIE_ID_2

Address Offset	0x0000 020C		
Physical Address	0x4A00 220C	**Instance**	CTRL_MODULE_CORE
Description	Die ID Register - Part 2. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. For more information, see Section 1.5 *OMAP543x Family and Device Identification* Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_DIE_ID_2																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_DIE_ID_2		R	0x0000 0000

Table 18-171. Register Call Summary for Register CONTROL_STD_FUSE_DIE_ID_2

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- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-172. CONTROL_STD_FUSE_DIE_ID_3

Address Offset	0x0000 0210		
Physical Address	0x4A00 2210	**Instance**	CTRL_MODULE_CORE
Description	Die ID Register - Part 3. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. For more information, see Section 1.5 *OMAP543x Family and Device Identification* Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_DIE_ID_3																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_DIE_ID_3		R	0x0000 0000

Table 18-173. Register Call Summary for Register CONTROL_STD_FUSE_DIE_ID_3

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-174. CONTROL_STD_FUSE_PROD_ID

Address Offset	0x0000 0214		
Physical Address	0x4A00 2214	**Instance**	CTRL_MODULE_CORE
Description	Prod ID Register - Part 0. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_PROD_ID																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_PROD_ID		R	0x0000 0000

Table 18-175. Register Call Summary for Register CONTROL_STD_FUSE_PROD_ID

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-176. CONTROL_STD_FUSE_CONF_ID_0

Address Offset	0x0000 0218		
Physical Address	0x4A00 2218	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse conf [31:0]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_CONF_ID_0																															

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Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_CONF_ID_0		R	0x0000 0000

Table 18-177. Register Call Summary for Register CONTROL_STD_FUSE_CONF_ID_0

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-178. CONTROL_STD_FUSE_CONF_ID_1

Address Offset	0x0000 021C		
Physical Address	0x4A00 221C	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse conf [63:32]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_CONF_ID_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_CONF_ID_1		R	0x0000 0000

Table 18-179. Register Call Summary for Register CONTROL_STD_FUSE_CONF_ID_1

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-180. CONTROL_STD_FUSE_MPK_0

Address Offset	0x0000 0220		
Physical Address	0x4A00 2220	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse keys. Root_public_key_hash [31:0]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_MPK_0																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_MPK_0		R	0x0000 0000

Table 18-181. Register Call Summary for Register CONTROL_STD_FUSE_MPK_0

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-182. CONTROL_STD_FUSE_MPK_1

Address Offset	0x0000 0224		
Physical Address	0x4A00 2224	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse keys. Root_public_key_hash [63:32]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_MPK_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_MPK_1		R	0x0000 0000

Table 18-183. Register Call Summary for Register CONTROL_STD_FUSE_MPK_1

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-184. CONTROL_STD_FUSE_MPK_2

Address Offset	0x0000 0228		
Physical Address	0x4A00 2228	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse keys. Root_public_key_hash [95:64]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_MPK_2																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_MPK_2		R	0x0000 0000

Table 18-185. Register Call Summary for Register CONTROL_STD_FUSE_MPK_2

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-186. CONTROL_STD_FUSE_MPK_3

Address Offset	0x0000 022C		
Physical Address	0x4A00 222C	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse keys. Root_public_key_hash [127:96]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_MPK_3																															

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Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_MPK_3		R	0x0000 0000

Table 18-187. Register Call Summary for Register CONTROL_STD_FUSE_MPK_3

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-188. CONTROL_STD_FUSE_MPK_4

Address Offset	0x0000 0230		
Physical Address	0x4A00 2230	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse keys. Root_public_key_hash [159:128]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_MPK_4																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_MPK_4		R	0x0000 0000

Table 18-189. Register Call Summary for Register CONTROL_STD_FUSE_MPK_4

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-190. CONTROL_STD_FUSE_MPK_5

Address Offset	0x0000 0234		
Physical Address	0x4A00 2234	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse keys. Root_public_key_hash [191:160]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_MPK_5																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_MPK_5		R	0x0000 0000

Table 18-191. Register Call Summary for Register CONTROL_STD_FUSE_MPK_5

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- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-192. CONTROL_STD_FUSE_MPK_6

Address Offset	0x0000 0238		
Physical Address	0x4A00 2238	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse keys. Root_public_key_hash [223:192]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_MPK_6																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_MPK_6		R	0x0000 0000

Table 18-193. Register Call Summary for Register CONTROL_STD_FUSE_MPK_6

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-194. CONTROL_STD_FUSE_MPK_7

Address Offset	0x0000 023C		
Physical Address	0x4A00 223C	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse keys. Root_public_key_hash [255:224]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_MPK_7																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_MPK_7		R	0x0000 0000

Table 18-195. Register Call Summary for Register CONTROL_STD_FUSE_MPK_7

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-196. CONTROL_STD_FUSE_OPP_VDD_MM_LVT_0

Address Offset	0x0000 0240		
Physical Address	0x4A00 2240	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MM [31:0]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_LVT_0																															

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Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_LVT_0		R	0x0000 0000

Table 18-197. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_LVT_0

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-198. CONTROL_STD_FUSE_OPP_VDD_MM_LVT_1

Address Offset	0x0000 0244		
Physical Address	0x4A00 2244	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MM [63:32]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_LVT_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_LVT_1		R	0x0000 0000

Table 18-199. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_LVT_1

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-200. CONTROL_STD_FUSE_OPP_VDD_MM_LVT_2

Address Offset	0x0000 0248		
Physical Address	0x4A00 2248	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MM [95:64]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_LVT_2																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_LVT_2		R	0x0000 0000

Table 18-201. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_LVT_2

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-202. CONTROL_STD_FUSE_OPP_VDD_MM_LVT_3

Address Offset	0x0000 024C
Physical Address	0x4A00 224C **Instance** CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MM [127:96]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_LVT_3																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_LVT_3		R	0x0000 0000

Table 18-203. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_LVT_3

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-204. CONTROL_STD_FUSE_OPP_VDD_MM_LVT_4

Address Offset	0x0000 0250
Physical Address	0x4A00 2250 **Instance** CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MM [159:128]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_LVT_4																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_LVT_4		R	0x0000 0000

Table 18-205. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_LVT_4

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-206. CONTROL_STD_FUSE_OPP_VDD_MM_LVT_5

Address Offset	0x0000 0254
Physical Address	0x4A00 2254 **Instance** CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MM [191:160]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MM_LVT_5																															

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Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MM_LVT_5		R	0x0000 0000

Table 18-207. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MM_LVT_5

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-208. CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_0

Address Offset	0x0000 0258		
Physical Address	0x4A00 2258	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MPU [31:0]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_LVT_0																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_LVT_0		R	0x0000 0000

Table 18-209. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_0

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-210. CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_1

Address Offset	0x0000 025C		
Physical Address	0x4A00 225C	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MPU [63:32]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_LVT_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_LVT_1		R	0x0000 0000

Table 18-211. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_1

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-212. CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_2

Address Offset	0x0000 0260
Physical Address	0x4A00 2260 **Instance** CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MPU [95:64]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_LVT_2																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_LVT_2		R	0x0000 0000

Table 18-213. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_2

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-214. CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_3

Address Offset	0x0000 0264
Physical Address	0x4A00 2264 **Instance** CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MPU [127:96]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_LVT_3																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_LVT_3		R	0x0000 0000

Table 18-215. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_3

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-216. CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_4

Address Offset	0x0000 0268
Physical Address	0x4A00 2268 **Instance** CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MPU [159:128]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_LVT_4																															

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Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_LVT_4		R	0x0000 0000

Table 18-217. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_4

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-218. CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_5

Address Offset	0x0000 026C		
Physical Address	0x4A00 226C	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MPU [191:160]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_LVT_5																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_LVT_5		R	0x0000 0000

Table 18-219. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_5

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-220. CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_6

Address Offset	0x0000 0270		
Physical Address	0x4A00 2270	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MPU [223:192]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_LVT_6																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_LVT_6		R	0x0000 0000

Table 18-221. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_6

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-222. CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_7

Address Offset	0x0000 0274		
Physical Address	0x4A00 2274	**Instance**	CTRL_MODULE_CORE
Description	Standard Fuse LVT OPP VDD_MPU [255:224]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_OPP_VDD_MPU_LVT_7																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_OPP_VDD_MPU_LVT_7		R	0x0000 0000

Table 18-223. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_LVT_7

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-224. CONTROL_CUST_FUSE_SWRV_0

Address Offset	0x0000 02BC		
Physical Address	0x4A00 22BC	**Instance**	CTRL_MODULE_CORE
Description	Customer Fuse keys. Software Version Control [031:000] (16 bits upper Redundant field) [FIELD OVERFLOW]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST_FUSE_SWRV_0																															

Bits	Field Name	Description	Type	Reset
31:0	CUST_FUSE_SWRV_0		R	0x0000 0000

Table 18-225. Register Call Summary for Register CONTROL_CUST_FUSE_SWRV_0

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-226. CONTROL_CUST_FUSE_SWRV_1

Address Offset	0x0000 02C0		
Physical Address	0x4A00 22C0	**Instance**	CTRL_MODULE_CORE
Description	Customer Fuse keys. Software Version Control [063:032] (16 bits upper Redundant field) [FIELD F]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST_FUSE_SWRV_1																															

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Bits	Field Name	Description	Type	Reset
31:0	CUST_FUSE_SWRV_1		R	0x0000 0000

Table 18-227. Register Call Summary for Register CONTROL_CUST_FUSE_SWRV_1

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-228. CONTROL_CUST_FUSE_SWRV_2

Address Offset	0x0000 02C4		
Physical Address	0x4A00 22C4	**Instance**	CTRL_MODULE_CORE
Description	Customer Fuse keys. Software Version Control [095:064] (16 bits upper Redundant field) [FIELD E]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST_FUSE_SWRV_2																															

Bits	Field Name	Description	Type	Reset
31:0	CUST_FUSE_SWRV_2		R	0x0000 0000

Table 18-229. Register Call Summary for Register CONTROL_CUST_FUSE_SWRV_2

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-230. CONTROL_CUST_FUSE_SWRV_3

Address Offset	0x0000 02C8		
Physical Address	0x4A00 22C8	**Instance**	CTRL_MODULE_CORE
Description	Customer Fuse keys. Software Version Control [127:096] (16 bits upper Redundant field) [FIELD D]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST_FUSE_SWRV_3																															

Bits	Field Name	Description	Type	Reset
31:0	CUST_FUSE_SWRV_3		R	0x0000 0000

Table 18-231. Register Call Summary for Register CONTROL_CUST_FUSE_SWRV_3

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

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Table 18-232. CONTROL_CUST_FUSE_SWRV_4

Address Offset	0x0000 02CC		
Physical Address	0x4A00 22CC	**Instance**	CTRL_MODULE_CORE
Description	Customer Fuse keys. Software Version Control [159:127] (16 bits upper Redundant field) [FIELD C]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST_FUSE_SWRV_4																															

Bits	Field Name	Description	Type	Reset
31:0	CUST_FUSE_SWRV_4		R	0x0000 0000

Table 18-233. Register Call Summary for Register CONTROL_CUST_FUSE_SWRV_4

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-234. CONTROL_CUST_FUSE_SWRV_5

Address Offset	0x0000 02D0		
Physical Address	0x4A00 22D0	**Instance**	CTRL_MODULE_CORE
Description	Customer Fuse keys. Software Version Control [191:160] (16 bits upper Redundant field) [FIELD B]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST_FUSE_SWRV_5																															

Bits	Field Name	Description	Type	Reset
31:0	CUST_FUSE_SWRV_5		R	0x0000 0000

Table 18-235. Register Call Summary for Register CONTROL_CUST_FUSE_SWRV_5

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-236. CONTROL_CUST_FUSE_SWRV_6

Address Offset	0x0000 02D4		
Physical Address	0x4A00 22D4	**Instance**	CTRL_MODULE_CORE
Description	Customer Fuse keys. Software Version Control [223:192] (16 bits upper Redundant field) [FIELD A]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST_FUSE_SWRV_6																															

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Bits	Field Name	Description	Type	Reset
31:0	CUST_FUSE_SWRV_6		R	0x0000 0000

Table 18-237. Register Call Summary for Register CONTROL_CUST_FUSE_SWRV_6

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-238. CONTROL_HWOBSDIVIDER1

Address Offset	0x0000 02D8		
Physical Address	0x4A00 22D8	**Instance**	CTRL_MODULE_CORE
Description	Divider selection register1. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		HWOBSDIV_USB			RESERVED						HWOBSDIV_SATA			HWOBSDIV_PER		HWOBSDIV_HDMI		HWOBSDIV_DSI1C		HWOBSDIV_DSI1A		HWOBSDIV_CORE		HWOBSDIV_ABE							

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:27	HWOBSDIV_USB	Control USB DPLL divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0
26:21	RESERVED		R	0x0
20:18	HWOBSDIV_SATA	Control SATA DPLL divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0

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Bits	Field Name	Description	Type	Reset
17:15	HWOBSDIV_PER	Control PER DPLL divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0
14:12	HWOBSDIV_HDMI	Control HDMI DPLL divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0
11:9	HWOBSDIV_DSI1C	Control DSI1C DPLL divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0
8:6	HWOBSDIV_DSI1A	Control DSI1A DPLL divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0
5:3	HWOBSDIV_CORE	Control CORE DPLL divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0

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Bits	Field Name	Description	Type	Reset
2:0	HWOBSDIV_ABE	Control ABE DPLL divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0

Table 18-239. Register Call Summary for Register CONTROL_HWOBSDIVIDER1

Control Module Functional Description • DPLL Clockview Channel Observable Signals Multiplexing: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-240. CONTROL_HWOBSDIVIDER2

Address Offset	0x0000 02DC		
Physical Address	0x4A00 22DC	**Instance**	CTRL_MODULE_CORE
Description	Divider selection register2. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWOBSDIV_SPARE																								HWOBSDIV_CORE13			HWOBSDIV_PER4			HWOBSDIV_USBOTGSS	

Bits	Field Name	Description	Type	Reset
31:9	HWOBSDIV_SPARE	Spare, can be used to control resources	RW	0x00 0000
8:6	HWOBSDIV_CORE13	Control CORE13 divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0

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Bits	Field Name	Description	Type	Reset
5:3	HWOBSDIV_PER4	Control PER4 divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0
2:0	HWOBSDIV_USBOTGSS	Control USBOTGSS DPLL divider 0x6: input is divided by 32 0x1: input is divided by 1 0x7: input is divided by 64 0x0: output is 0 0x2: input is divided by 2 0x4: input is divided by 8 0x5: input is divided by 16 0x3: input is divided by 4	RW	0x0

Table 18-241. Register Call Summary for Register CONTROL_HWOBSDIVIDER2

Control Module Functional Description • DPLL Clockview Channel Observable Signals Multiplexing: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-242. CONTROL_DEV_CONF

Address Offset	0x0000 0300		
Physical Address	0x4A00 2300	**Instance**	CTRL_MODULE_CORE
Description	Device configuration register. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_CONF																															USBPHY_PD

Bits	Field Name	Description	Type	Reset
31:1	DEV_CONF	Spare bits for device configuration.	RW	0x0000 0000
0	USBPHY_PD	Power down entire USB phy (data, common module and UTMI). Controls USB2PHYCORE.PD pin. 0x0: Normal operation 0x1: Power down the USB PHY	RW	0

Table 18-243. Register Call Summary for Register CONTROL_DEV_CONF

Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [0]

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Table 18-244. CONTROL_DSP_BOOTADDR

Address Offset	0x0000 0304		
Physical Address	0x4A00 2304	**Instance**	CTRL_MODULE_CORE
Description	DSP boot loader physical address Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSP_BOOT_LOAD_ADDR																						Reserved									

Bits	Field Name	Description	Type	Reset
31:10	DSP_BOOT_LOAD_ADDR	DSP boot loader physical address This index addresses a 4kbytes page	RW	0x08 0000
9:0	Reserved	Reserved	RW	0x000

Table 18-245. Register Call Summary for Register CONTROL_DSP_BOOTADDR

Control Module Functional Description

- DSP Boot Register: [0] [1]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [2]

Table 18-246. CONTROL_TEMP_SENSOR_MPU

Address Offset	0x0000 032C		
Physical Address	0x4A00 232C	**Instance**	CTRL_MODULE_CORE
Description	Control VBGAPTS temperature sensor and thermal comparator shutdown register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				BGAP_TMPSOFF_MPU	BGAP_EOCZ_MPU	BGAP_DTEMP_MPU									

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11	BGAP_TMPSOFF_MPU	Temperature sensor and thermal shutdown mode.	R	1
10	BGAP_EOCZ_MPU	ADC End of Conversion. Active low, when CTRL_TEMP(9:0) is valid.	R	0
9:0	BGAP_DTEMP_MPU	Temperature data from the ADC. Valid if EOCZ is low.	R	0x000

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Table 18-247. Register Call Summary for Register CONTROL_TEMP_SENSOR_MPU

Control Module Functional Description

- Bandgap Voltage and Temperature Sensor: [0]
- Continuous Conversion Mode: [1] [2]
- Thermal Data Post-Processing Logic: [3]
- Temperature Timestamping: [4]
- ADC Codes Versus Temperature: [5]
- Temperature Sensor Control Registers: [6]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [7]

Table 18-248. CONTROL_TEMP_SENSOR_MM

Address Offset	0x0000 0330		
Physical Address	0x4A00 2330	**Instance**	CTRL_MODULE_CORE
Description	Control VBGAPTS temperature sensor and thermal comparator shutdown register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				BGAP_TMPSOFF_MM	BGAP_EOCZ_MM	BGAP_DTEMP_MM									

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11	BGAP_TMPSOFF_MM	Temperature sensor and thermal shutdown mode.	R	1
10	BGAP_EOCZ_MM	ADC End of Conversion. Active low, when CTRL_TEMP(9:0) is valid.	R	0
9:0	BGAP_DTEMP_MM	Temperature data from the ADC. Valid if EOCZ is low.	R	0x000

Table 18-249. Register Call Summary for Register CONTROL_TEMP_SENSOR_MM

Control Module Functional Description

- Bandgap Voltage and Temperature Sensor: [0]
- Continuous Conversion Mode: [1] [2]
- Thermal Data Post-Processing Logic: [3]
- Temperature Timestamping: [4]
- ADC Codes Versus Temperature: [5]
- Temperature Sensor Control Registers: [6]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [7]

Table 18-250. CONTROL_TEMP_SENSOR_CORE

Address Offset	0x0000 0334		
Physical Address	0x4A00 2334	**Instance**	CTRL_MODULE_CORE
Description	Control VBGAPTS temperature sensor and thermal comparator shutdown register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				BGAP_TMPSOFF_CORE	BGAP_EOCZ_CORE	BGAP_DTEMP_CORE									

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11	BGAP_TMPSOFF_CORE	Temperature sensor and thermal shutdown mode.	R	1
10	BGAP_EOCZ_CORE	ADC End of Conversion. Active low, when CTRL_TEMP(9:0) is valid.	R	0
9:0	BGAP_DTEMP_CORE	Temperature data from the ADC. Valid if EOCZ is low.	R	0x000

Table 18-251. Register Call Summary for Register CONTROL_TEMP_SENSOR_CORE

Control Module Functional Description

- Bandgap Voltage and Temperature Sensor: [0]
- Continuous Conversion Mode: [1] [2]
- Thermal Data Post-Processing Logic: [3]
- Temperature Timestamping: [4]
- ADC Codes Versus Temperature: [5]
- Temperature Sensor Control Registers: [6]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [7]

Table 18-252. CONTROL_LDOSRAM_MPU_LVT_VOLTAGE_CTRL

Address Offset	0x0000 0338		
Physical Address	0x4A00 2338	**Instance**	CTRL_MODULE_CORE
Description	MPU LVT SRAM LDO Control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					LDOSRAMMPU_LVT_RETMODE_MUX_CTRL			LDOSRAMMPU_LVT_RETMODE_VSET_IN				LDOSRAMMPU_LVT_RETMODE_VSET_OUT				RESERVED					LDOSRAMMPU_LVT_ACTMODE_MUX_CTRL			LDOSRAMMPU_LVT_ACTMODE_VSET_IN				LDOSRAMMPU_LVT_ACTMODE_VSET_OUT			

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	LDOSRAMMPU_LVT_RETMODE_MUX_CTRL	Override control of EFUSE Retention Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
25:21	LDOSRAMMPU_LVT_RETMODE_VSET_IN	EFUSE Retention Mode Voltage value (vset[9:5])	R	0x00
20:16	LDOSRAMMPU_LVT_RETMODE_VSET_OUT	Override value for Retention Mode Voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOSRAMMPU_LVT_ACTMODE_MUX_CTRL	Override control of EFUSE Active Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOSRAMMPU_LVT_ACTMODE_VSET_IN	EFUSE Active Mode Voltage value (vset[4:0])	R	0x00
4:0	LDOSRAMMPU_LVT_ACTMODE_VSET_OUT	Override value for Active Mode Voltage value	RW	0x00

Table 18-253. Register Call Summary for Register CONTROL_LDOSRAM_MPU_LVT_VOLTAGE_CTRL

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-254. CONTROL_CORTEX_M4_MMUADDRTRANSLTR

Address Offset	0x0000 0358		
Physical Address	0x4A00 2358	**Instance**	CTRL_MODULE_CORE
Description	CORTEX_M4 reg Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CORTEX_M4_MMUADDRTRANSLTR																									

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	CORTEX_M4_MMUADDRTRANSLTR	Used to save the mmu address boot	RW	0x0 0000

Table 18-255. Register Call Summary for Register CONTROL_CORTEX_M4_MMUADDRTRANSLTR

Control Module Functional Description
- General Core Control Module Instance: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-256. CONTROL_CORTEX_M4_MMUADDRLOGICTR

Address Offset	0x0000 035C		
Physical Address	0x4A00 235C	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CORTEX_M4_MMUADDRLOGICTR															

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	CORTEX_M4_MMUADDRLOGICTR		RW	0x0 0000

Table 18-257. Register Call Summary for Register CONTROL_CORTEX_M4_MMUADDRLOGICTR

Control Module Functional Description • General Core Control Module Instance: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-258. CONTROL_HWOBS_CONTROL

Address Offset	0x0000 0360		
Physical Address	0x4A00 2360	**Instance**	CTRL_MODULE_CORE
Description	HW observability control. This register enables or disables HW observability outputs (to save power primarily) Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HWOBS_CLKDIV_SEL_2				HWOBS_CLKDIV_SEL_1				HWOBS_CLKOBS_GATE_ENABLE		HWOBS_CLKDIV_SEL					HWOBS_ALL_ZERO_MODE	HWOBS_ALL_ONE_MODE	HWOBS_MACRO_ENABLE

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18:14	HWOBS_CLKDIV_SEL_2	Clock divider selection on po_hwobs(2). 0x8: output is divided by 8 0x1: output is not divided 0x4: output is divided by 4 0x10: output is divided by 16 0x2: output is divided by 2	RW	0x00
13:9	HWOBS_CLKDIV_SEL_1	Clock divider selection on po_hwobs(1). 0x8: output is divided by 8 0x1: output is not divided 0x4: output is divided by 4 0x10: output is divided by 16 0x2: output is divided by 2	RW	0x00
8	HWOBS_CLKOBS_GATE_ENABLE	Used to gate clk observable signals at the output of the DPLLs in order to save power	RW	0

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Bits	Field Name	Description	Type	Reset
7:3	HWOBS_CLKDIV_SEL	Clock divider selection on po_hwobs(0). 0x8: output is divided by 8 0x1: output is not divided 0x4: output is divided by 4 0x10: output is divided by 16 0x2: output is divided by 2	RW	0x00
2	HWOBS_ALL_ZERO_MODE	Used to gate observable signals. When set all outputs are set to zero (can be used to check the path from HW observability to external pads). 0x0: hw observability ports are not gated 0x1: hw observability ports are all set to 0	RW	0
1	HWOBS_ALL_ONE_MODE	Used to gate observable signals. When set all outputs are set to one (can be used to check the path from HW observability to external pads). 0x0: hw observability ports are not gated 0x1: hw observability ports are all set to 1	RW	0
0	HWOBS_MACRO_ENABLE	Used to gate observable signals coming from macros using the 32-bit HWOBS bus definition. When deasserted all outputs of the HWOBS busdef are set to zero. 0x0: hw observability ports from macros are gated and set to zero 0x1: hw observability ports from macros are not gated	RW	0

Table 18-259. Register Call Summary for Register CONTROL_HWOBS_CONTROL

Control Module Functional Description • General Core Control Module Instance: [0] • Observability Gating Capabilities: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
Control Module Programming Guide • Hardware Observability Settings: [13] [14] [15] [16] [17] [18]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [19]

Table 18-260. CONTROL_PHY_POWER_USB

Address Offset	0x0000 0370		
Physical Address	0x4A00 2370	**Instance**	CTRL_MODULE_CORE
Description	phy_power_usb Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USB_PWRCTL_CLK_FREQ								USB_PWRCTL_CLK_CMD								RESERVED															

Bits	Field Name	Description	Type	Reset
31:22	USB_PWRCTL_CLK_FREQ	Indicates the frequency of REF_CLK 0x26: If SYSCLK = 38.4 MHz 0x1A: If SYSCLK = 26.0 MHz 0x13: If SYSCLK = 19.2 MHz 0x10: If SYSCLK = 16.8 MHz 0x0C: If SYSCLK = 12.0 MHz	RW	0x000

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Bits	Field Name	Description	Type	Reset
21:14	USB_PWRCTL_CLK_CMD	Powers up/down the USB3_PHY_TX and USB3_PHY_RX modules. 0x0: powers down USB3_PHY_TX and USB3_PHY_RX 0x1: powers up the USB3_PHY_RX only. 0x2: powers up the USB3_PHY_TX only. 0x3: simultaneously powers up the USB3_PHY_RX and the USB3_PHY_TX	RW	0x00
13:0	RESERVED	Reserved	R	0x0000

Table 18-261. Register Call Summary for Register CONTROL_PHY_POWER_USB

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-262. CONTROL_PHY_POWER_SATA

Address Offset	0x0000 0374		
Physical Address	0x4A00 2374	**Instance**	CTRL_MODULE_CORE
Description	phy_power_sata Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SATA_PWRCTL_CLK_FREQ										SATA_PWRCTL_CLK_CMD														RESERVED							

Bits	Field Name	Description	Type	Reset
31:22	SATA_PWRCTL_CLK_FREQ	Indicate the frequency of REF_CLK 0x26: If SYSCLK = 38.4 MHz 0x1A: If SYSCLK = 26.0 MHz 0x13: If SYSCLK = 19.2 MHz 0x10: If SYSCLK = 16.8 MHz 0x0C: If SYSCLK = 12.0 MHz	RW	0x000
21:14	SATA_PWRCTL_CLK_CMD	Powers up/down the SATA_PHY_TX and SATA_PHY_RX modules 0x0: powers down SATA_PHY_TX and SATA_PHY_RX 0x1: powers up the SATA_PHY_RX only. 0x2: powers up the SATA_PHY_TX only. 0x3: simultaneously powers up the SATA_PHY_RX and the SATA_PHY_TX	RW	0x00
13:0	RESERVED	Reserved	R	0x0000

Table 18-263. Register Call Summary for Register CONTROL_PHY_POWER_SATA

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-264. CONTROL_BANDGAP_MASK

Address Offset	0x0000 0380		
Physical Address	0x4A00 2380	**Instance**	CTRL_MODULE_CORE
Description	bgap_mask Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31 30	29 28 27	26 25 24	23	22	21	20	19	18	17	16	15 14 13 12 11 10 9 8	7 6	5	4	3	2	1	0
SIDLEMODE	COUNTER_DELAY	RESERVED	FREEZE_CORE	FREEZE_MM	FREEZE_MPU	CLEAR_CORE	CLEAR_MM	CLEAR_MPU	CLEAR_ACCUM_CORE	CLEAR_ACCUM_MM	CLEAR_ACCUM_MPU	RESERVED	MASK_HOT_CORE	MASK_COLD_CORE	MASK_HOT_MM	MASK_COLD_MM	MASK_HOT_MPU	MASK_COLD_MPU

Bits	Field Name	Description	Type	Reset
31:30	SIDLEMODE	sidlemode for bandgap 0x0: No Idle 0x1: Force Idle 0x3: Reserved 0x2: Smart Idle	RW	0x2
29:27	COUNTER_DELAY	Counter delay 0x1: Delay of 1ms 0x0: Immediate 0x2: Delay of 10ms 0x4: Delay of 250ms 0x5: Delay of 500ms 0x3: Delay of 100ms	RW	0x2
26:24	RESERVED		R	0x0
23	FREEZE_CORE	Freeze the FIFO CORE 0x0: No operation 0x1: Freeze the FIFO	RW	0
22	FREEZE_MM	Freeze the FIFO MM 0x0: No operation 0x1: Freeze the FIFO	RW	0
21	FREEZE_MPU	Freeze the FIFO MPU 0x0: No operation 0x1: Freeze the FIFO	RW	0
20	CLEAR_CORE	Reset the FIFO CORE 0x0: No operation 0x1: Reset the FIFO	RW	0
19	CLEAR_MM	Reset the FIFO MM 0x0: No operation 0x1: Reset the FIFO	RW	0
18	CLEAR_MPU	Reset the FIFO MPU 0x0: No operation 0x1: Reset the FIFO	RW	0
17	CLEAR_ACCUM_CORE	Reset the accumulator CORE. Reset also the FIFO CORE 0x0: No operation 0x1: Reset the accumulator	RW	0
16	CLEAR_ACCUM_MM	Reset the accumulator MM. Reset also the FIFO MM 0x0: No operation 0x1: Reset the accumulator	RW	0

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Bits	Field Name	Description	Type	Reset
15	CLEAR_ACCUM_MPU	Reset the accumulator MPU. Reset also the FIFO MPU 0x0: No operation 0x1: Reset the accumulator	RW	0
14:6	RESERVED		R	0x000
5	MASK_HOT_CORE	Mask for hot event CORE 0x0: hot event is masked 0x1: hot event is unmasked	RW	0
4	MASK_COLD_CORE	Mask for cold event CORE 0x0: cold event is masked 0x1: cold event is unmasked	RW	0
3	MASK_HOT_MM	Mask for hot event MM 0x0: hot event is masked 0x1: hot event is unmasked	RW	0
2	MASK_COLD_MM	Mask for cold event MM 0x0: cold event is masked 0x1: cold event is unmasked	RW	0
1	MASK_HOT_MPU	Mask for hot event MPU 0x0: hot event is masked 0x1: hot event is unmasked	RW	0
0	MASK_COLD_MPU	Mask for cold event MPU 0x0: cold event is masked 0x1: cold event is unmasked	RW	0

Table 18-265. Register Call Summary for Register CONTROL_BANDGAP_MASK

Control Module Functional Description

- Continuous Conversion Mode: [0] [1]
- Thermal Alert Functionality Comparators: [2] [3] [4] [5] [6] [7]
- Temperature Timestamping: [8] [9] [10] [11] [12] [13]
- Temperature Accumulators: [14] [15] [16]
- Bandgap FSMs Power Management: [17]
- Temperature Sensor Control Registers: [18]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [19]

Table 18-266. CONTROL_BANDGAP_THRESHOLD_MPU

Address Offset	0x0000 0384		
Physical Address	0x4A00 2384	**Instance**	CTRL_MODULE_CORE
Description	BGAP THRESHOLD MPU Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THOLD_HOT_MPU								RESERVED								THOLD_COLD_MPU							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	THOLD_HOT_MPU	alert value hot	RW	0x000
15:10	RESERVED		R	0x00
9:0	THOLD_COLD_MPU	alert value cold	RW	0x000

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Table 18-267. Register Call Summary for Register CONTROL_BANDGAP_THRESHOLD_MPU

Control Module Functional Description
- Thermal Data Post-Processing Logic: [0]
- Thermal Alert Functionality Comparators: [1] [2]
- Temperature Sensor Control Registers: [3]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [4]

Table 18-268. CONTROL_BANDGAP_THRESHOLD_MM

Address Offset	0x0000 0388		
Physical Address	0x4A00 2388	**Instance**	CTRL_MODULE_CORE
Description	BGAP THRESHOLD MM Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THOLD_HOT_MM								RESERVED								THOLD_COLD_MM							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	THOLD_HOT_MM	alert value hot	RW	0x000
15:10	RESERVED		R	0x00
9:0	THOLD_COLD_MM	alert value cold	RW	0x000

Table 18-269. Register Call Summary for Register CONTROL_BANDGAP_THRESHOLD_MM

Control Module Functional Description
- Thermal Data Post-Processing Logic: [0]
- Thermal Alert Functionality Comparators: [1] [2]
- Temperature Sensor Control Registers: [3]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [4]

Table 18-270. CONTROL_BANDGAP_THRESHOLD_CORE

Address Offset	0x0000 038C		
Physical Address	0x4A00 238C	**Instance**	CTRL_MODULE_CORE
Description	BGAP THRESHOLD CORE Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THOLD_HOT_CORE								RESERVED								THOLD_COLD_CORE							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	THOLD_HOT_CORE	alert value hot	RW	0x000
15:10	RESERVED		R	0x00
9:0	THOLD_COLD_CORE	alert value cold	RW	0x000

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Table 18-271. Register Call Summary for Register CONTROL_BANDGAP_THRESHOLD_CORE

Control Module Functional Description
- Thermal Data Post-Processing Logic: [0]
- Thermal Alert Functionality Comparators: [1] [2]
- Temperature Sensor Control Registers: [3]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [4]

Table 18-272. CONTROL_BANDGAP_TSHUT_MPU

Address Offset	0x0000 0390		
Physical Address	0x4A00 2390	**Instance**	CTRL_MODULE_CORE
Description	BGAP TSHUT THRESHOLD MPU Access conditions. Read Only		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSHUT_HOT_MPU								RESERVED								TSHUT_COLD_MPU							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved	R	0x00
25:16	TSHUT_HOT_MPU	tshut value hot	R	0x000
15:10	RESERVED	Reserved	R	0x00
9:0	TSHUT_COLD_MPU	tshut value cold	R	0x000

Table 18-273. Register Call Summary for Register CONTROL_BANDGAP_TSHUT_MPU

Control Module Functional Description
- Thermal Data Post-Processing Logic: [0]
- Thermal Shutdown Functionality Comparators: [1] [2]
- Temperature Sensor Control Registers: [3]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [4]

Table 18-274. CONTROL_BANDGAP_TSHUT_MM

Address Offset	0x0000 0394		
Physical Address	0x4A00 2394	**Instance**	CTRL_MODULE_CORE
Description	BGAP TSHUT THRESHOLD MM Access conditions. Read Only		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSHUT_HOT_MM								RESERVED								TSHUT_COLD_MM							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved	R	0x00
25:16	TSHUT_HOT_MM	tshut value hot	R	0x000
15:10	RESERVED	Reserved	R	0x00
9:0	TSHUT_COLD_MM	tshut value cold	R	0x000

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Table 18-275. Register Call Summary for Register CONTROL_BANDGAP_TSHUT_MM

Control Module Functional Description
- Thermal Data Post-Processing Logic: [0]
- Thermal Shutdown Functionality Comparators: [1] [2]
- Temperature Sensor Control Registers: [3]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [4]

Table 18-276. CONTROL_BANDGAP_TSHUT_CORE

Address Offset	0x0000 0398		
Physical Address	0x4A00 2398	**Instance**	CTRL_MODULE_CORE
Description	BGAP TSHUT THRESHOLD CORE Access conditions. Read Only		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TSHUT_HOT_CORE								RESERVED								TSHUT_COLD_CORE							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved	R	0x00
25:16	TSHUT_HOT_CORE	tshut value hot	R	0x000
15:10	RESERVED	Reserved	R	0x00
9:0	TSHUT_COLD_CORE	tshut value cold	R	0x000

Table 18-277. Register Call Summary for Register CONTROL_BANDGAP_TSHUT_CORE

Control Module Functional Description
- Thermal Data Post-Processing Logic: [0]
- Thermal Shutdown Functionality Comparators: [1] [2]
- Temperature Sensor Control Registers: [3]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [4]

Table 18-278. CONTROL_BANDGAP_CUMUL_DTEMP_MPU

Address Offset	0x0000 039C		
Physical Address	0x4A00 239C	**Instance**	CTRL_MODULE_CORE
Description	BGAP TEMPERATURE ACCUMULATOR MPU Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUMUL_DTEMP_MPU																															

Bits	Field Name	Description	Type	Reset
31:0	CUMUL_DTEMP_MPU	temperature accumulator	R	0x0000 0000

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Table 18-279. Register Call Summary for Register CONTROL_BANDGAP_CUMUL_DTEMP_MPU

Control Module Functional Description
- Thermal Data Post-Processing Logic: [0]
- Temperature Accumulators: [1] [2] [3]
- Temperature Sensor Control Registers: [4]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [5]

Table 18-280. CONTROL_BANDGAP_CUMUL_DTEMP_MM

Address Offset	0x0000 03A0		
Physical Address	0x4A00 23A0	**Instance**	CTRL_MODULE_CORE
Description	BGAP TEMPERATURE ACCUMULATOR MM Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUMUL_DTEMP_MM																															

Bits	Field Name	Description	Type	Reset
31:0	CUMUL_DTEMP_MM	temperature accumulator	R	0x0000 0000

Table 18-281. Register Call Summary for Register CONTROL_BANDGAP_CUMUL_DTEMP_MM

Control Module Functional Description
- Thermal Data Post-Processing Logic: [0]
- Temperature Accumulators: [1] [2]
- Temperature Sensor Control Registers: [3]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [4]

Table 18-282. CONTROL_BANDGAP_CUMUL_DTEMP_CORE

Address Offset	0x0000 03A4		
Physical Address	0x4A00 23A4	**Instance**	CTRL_MODULE_CORE
Description	BGAP TEMPERATURE ACCUMULATOR CORE Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUMUL_DTEMP_CORE																															

Bits	Field Name	Description	Type	Reset
31:0	CUMUL_DTEMP_CORE	temperature accumulator	R	0x0000 0000

Table 18-283. Register Call Summary for Register CONTROL_BANDGAP_CUMUL_DTEMP_CORE

Control Module Functional Description
- Thermal Data Post-Processing Logic: [0]
- Temperature Accumulators: [1] [2]
- Temperature Sensor Control Registers: [3]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [4]

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Table 18-284. CONTROL_BANDGAP_STATUS

Address Offset	0x0000 03A8		
Physical Address	0x4A00 23A8	**Instance**	CTRL_MODULE_CORE
Description	BGAP STATUS Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALERT	RESERVED																									HOT_CORE	COLD_CORE	HOT_MM	COLD_MM	HOT_MPU	COLD_MPU

Bits	Field Name	Description	Type	Reset
31	ALERT	Alert temperature when '1'	R	0
30:6	RESERVED		R	0x000 0000
5	HOT_CORE	Event for hot temperature mpu bandgap when '1' Read 0x1: event detected Read 0x0: event not detected	R	0
4	COLD_CORE	Event for cold temperature mpu bandgap when '1' Read 0x1: event detected Read 0x0: event not detected	R	0
3	HOT_MM	Event for hot temperature mm bandgap when '1' Read 0x1: event detected Read 0x0: event not detected	R	0
2	COLD_MM	Event for cold temperature mm bandgap when '1' Read 0x1: event detected Read 0x0: event not detected	R	0
1	HOT_MPU	Event for hot temperature core bandgap when '1' Read 0x1: event detected Read 0x0: event not detected	R	0
0	COLD_MPU	Event for cold temperature core bandgap when '1' Read 0x1: event detected Read 0x0: event not detected	R	0

Table 18-285. Register Call Summary for Register CONTROL_BANDGAP_STATUS

Control Module Functional Description
- Thermal Alert Functionality Comparators: [0] [1] [2] [3] [4] [5] [6]
- Temperature Sensor Control Registers: [7]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [8]

Table 18-286. CONTROL_SATA_EXT_MODE

Address Offset	0x0000 03AC		
Physical Address	0x4A00 23AC	**Instance**	CTRL_MODULE_CORE
Description	SATA EXTENDED MODE Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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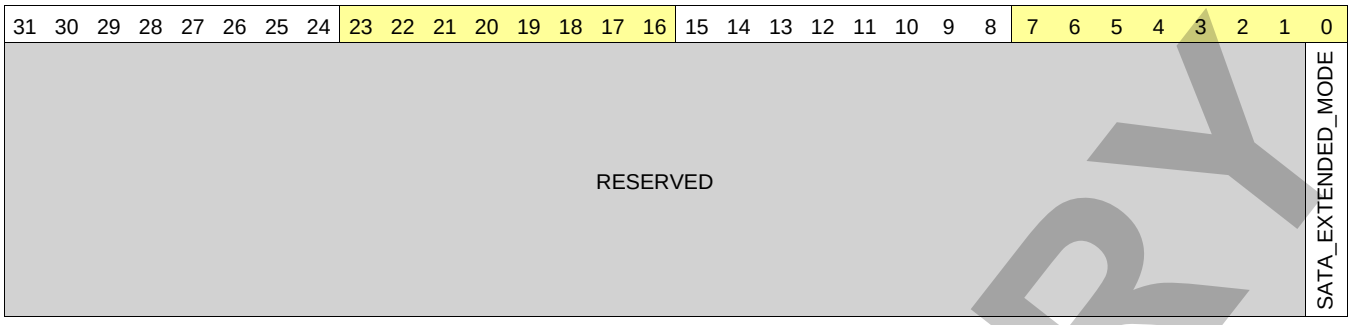


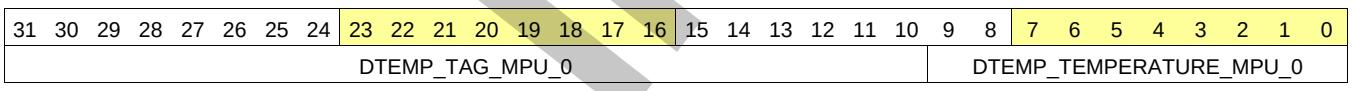
Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	SATA_EXTENDED_MODE	sata extended mode 0x0: no extended mode 0x1: extended mode	RW	0

Table 18-287. Register Call Summary for Register CONTROL_SATA_EXT_MODE

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [0]

Table 18-288. CONTROL_DTEMP_MPU_0

Address Offset	0x0000 03C0		
Physical Address	0x4A00 23C0	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MPU DOMAIN. Most recent sample Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		



Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MPU_0	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MPU_0	temperature	R	0x000

Table 18-289. Register Call Summary for Register CONTROL_DTEMP_MPU_0

Control Module Functional Description
- Temperature Timestamping: [0]
- Temperature Accumulators: [1]
- Temperature Sensor Control Registers: [2]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [3]

Table 18-290. CONTROL_DTEMP_MPU_1

Address Offset	0x0000 03C4		
Physical Address	0x4A00 23C4	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MPU DOMAIN Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_MPU_1																DTEMP_TEMPERATURE_MPU_1															

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MPU_1	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MPU_1	temperature	R	0x000

Table 18-291. Register Call Summary for Register CONTROL_DTEMP_MPU_1

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-292. CONTROL_DTEMP_MPU_2

Address Offset	0x0000 03C8		
Physical Address	0x4A00 23C8	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MPU DOMAIN Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_MPU_2																DTEMP_TEMPERATURE_MPU_2															

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MPU_2	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MPU_2	temperature	R	0x000

Table 18-293. Register Call Summary for Register CONTROL_DTEMP_MPU_2

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-294. CONTROL_DTEMP_MPU_3

Address Offset	0x0000 03CC		
Physical Address	0x4A00 23CC	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MPU DOMAIN Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_MPU_3																DTEMP_TEMPERATURE_MPU_3															

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Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MPU_3	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MPU_3	temperature	R	0x000

Table 18-295. Register Call Summary for Register CONTROL_DTEMP_MPU_3

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-296. CONTROL_DTEMP_MPU_4

Address Offset	0x0000 03D0		
Physical Address	0x4A00 23D0	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MPU DOMAIN. Oldest sample Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_MPU_4																DTEMP_TEMPERATURE_MPU_4															

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MPU_4	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MPU_4	temperature	R	0x000

Table 18-297. Register Call Summary for Register CONTROL_DTEMP_MPU_4

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-298. CONTROL_DTEMP_MM_0

Address Offset	0x0000 03D4		
Physical Address	0x4A00 23D4	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MM DOMAIN. Most recent sample. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_MM_0																DTEMP_TEMPERATURE_MM_0															

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MM_0	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MM_0	temperature	R	0x000

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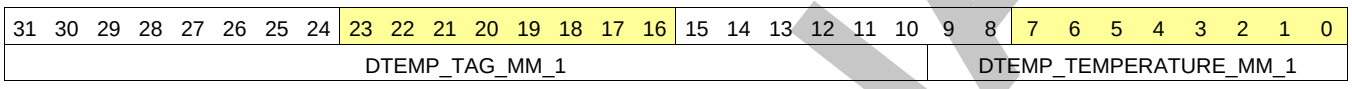
Table 18-299. Register Call Summary for Register CONTROL_DTEMP_MM_0

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-300. CONTROL_DTEMP_MM_1

Address Offset	0x0000 03D8		
Physical Address	0x4A00 23D8	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MM DOMAIN Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		



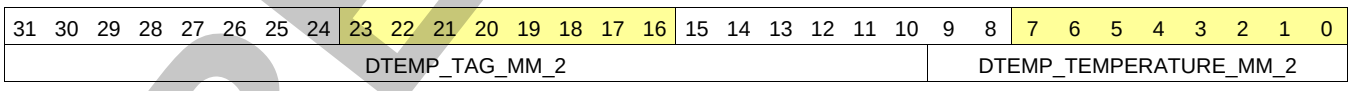
Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MM_1	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MM_1	temperature	R	0x000

Table 18-301. Register Call Summary for Register CONTROL_DTEMP_MM_1

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-302. CONTROL_DTEMP_MM_2

Address Offset	0x0000 03DC		
Physical Address	0x4A00 23DC	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MM DOMAIN Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		



Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MM_2	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MM_2	temperature	R	0x000

Table 18-303. Register Call Summary for Register CONTROL_DTEMP_MM_2

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

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Table 18-304. CONTROL_DTEMP_MM_3

Address Offset	0x0000 03E0		
Physical Address	0x4A00 23E0	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MM DOMAIN Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_MM_3																								DTEMP_TEMPERATURE_MM_3							

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MM_3	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MM_3	temperature	R	0x000

Table 18-305. Register Call Summary for Register CONTROL_DTEMP_MM_3

Control Module Functional Description
- Temperature Timestamping: [0]
- Temperature Sensor Control Registers: [1]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [2]

Table 18-306. CONTROL_DTEMP_MM_4

Address Offset	0x0000 03E4		
Physical Address	0x4A00 23E4	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE MM DOMAIN. Oldest sample. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_MM_4																								DTEMP_TEMPERATURE_MM_4							

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_MM_4	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_MM_4	temperature	R	0x000

Table 18-307. Register Call Summary for Register CONTROL_DTEMP_MM_4

Control Module Functional Description
- Temperature Timestamping: [0]
- Temperature Sensor Control Registers: [1]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [2]

Table 18-308. CONTROL_DTEMP_CORE_0

Address Offset	0x0000 03E8		
Physical Address	0x4A00 23E8	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE CORE DOMAIN. Most recent sample. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_CORE_0																DTEMP_TEMPERATURE_CORE_0															

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_CORE_0	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_CORE_0	temperature	R	0x000

Table 18-309. Register Call Summary for Register CONTROL_DTEMP_CORE_0

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-310. CONTROL_DTEMP_CORE_1

Address Offset	0x0000 03EC		
Physical Address	0x4A00 23EC	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE CORE DOMAIN Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_CORE_1																DTEMP_TEMPERATURE_CORE_1															

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_CORE_1	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_CORE_1	temperature	R	0x000

Table 18-311. Register Call Summary for Register CONTROL_DTEMP_CORE_1

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-312. CONTROL_DTEMP_CORE_2

Address Offset	0x0000 03F0		
Physical Address	0x4A00 23F0	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE CORE DOMAIN Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_CORE_2																DTEMP_TEMPERATURE_CORE_2															

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Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_CORE_2	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_CORE_2	temperature	R	0x000

Table 18-313. Register Call Summary for Register CONTROL_DTEMP_CORE_2

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-314. CONTROL_DTEMP_CORE_3

Address Offset	0x0000 03F4		
Physical Address	0x4A00 23F4	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE CORE DOMAIN Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_CORE_3																DTEMP_TEMPERATURE_CORE_3															

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_CORE_3	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_CORE_3	temperature	R	0x000

Table 18-315. Register Call Summary for Register CONTROL_DTEMP_CORE_3

Control Module Functional Description • Temperature Timestamping: [0] • Temperature Sensor Control Registers: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-316. CONTROL_DTEMP_CORE_4

Address Offset	0x0000 03F8		
Physical Address	0x4A00 23F8	**Instance**	CTRL_MODULE_CORE
Description	TAGGED TEMPERATURE CORE DOMAIN. Oldest sample. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEMP_TAG_CORE_4																DTEMP_TEMPERATURE_CORE_4															

Bits	Field Name	Description	Type	Reset
31:10	DTEMP_TAG_CORE_4	tag. Indicate number of times in the bgap state machine.	R	0x00 0000
9:0	DTEMP_TEMPERATURE_CORE_4	temperature	R	0x000

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Table 18-317. Register Call Summary for Register CONTROL_DTEMP_CORE_4

Control Module Functional Description
- Temperature Timestamping: [0]
- Temperature Sensor Control Registers: [1]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [2]

Table 18-318. CONTROL_OCPREG_SPARE

Address Offset	0x0000 03FC		
Physical Address	0x4A00 23FC	**Instance**	CTRL_MODULE_CORE
Description	Spare Register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCPREG_SPARE																															

Bits	Field Name	Description	Type	Reset
31:0	OCPREG_SPARE	Spare register	RW	0x0000 0000

Table 18-319. Register Call Summary for Register CONTROL_OCPREG_SPARE

Control Module Functional Description
- General Wake-Up Control Module Instance: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-320. CONTROL_DEBOBS_FINAL_MUX_SEL

Address Offset	0x0000 0400		
Physical Address	0x4A00 2400	**Instance**	CTRL_MODULE_CORE
Description	Final mux select signal. It selects between core and wkup signal (controls external observability logic). Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SELECT																															

Bits	Field Name	Description	Type	Reset
31:0	SELECT	(Control external observability logic)	RW	0x0000 0000

Table 18-321. Register Call Summary for Register CONTROL_DEBOBS_FINAL_MUX_SEL

Control Module Functional Description
- General Core Control Module Instance: [0]
- Observability Gating Capabilities: [1] [2]
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [3] [4] [5]

Control Module Programming Guide
- Hardware Observability Settings: [6]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [7]

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Table 18-322. CONTROL_DEBOBS_OCPWP_SYS_EVENT_SEL

Address Offset	0x0000 0404		
Physical Address	0x4A00 2404	**Instance**	CTRL_MODULE_CORE
Description	Selection between debug module (0) or PRM (1) outputs for OCP WP (controls external observability logic). Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SELECT															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	SELECT	(Control external observability logic)	RW	0x0000

Table 18-323. Register Call Summary for Register CONTROL_DEBOBS_OCPWP_SYS_EVENT_SEL

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-324. CONTROL_DEBOBS_MMR_MPU

Address Offset	0x0000 0408		
Physical Address	0x4A00 2408	**Instance**	CTRL_MODULE_CORE
Description	MPU MMR register to control HW observability muxing inside mpu (controls external observability logic). Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SELECT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	SELECT	(Control external observability logic)	RW	0x0

Table 18-325. Register Call Summary for Register CONTROL_DEBOBS_MMR_MPU

Control Module Functional Description

- MPU Subsystem Observable Signals: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [17]

Table 18-326. CONTROL_CONF_SDMA_REQ_SEL0

Address Offset	0x0000 042C		
Physical Address	0x4A00 242C	**Instance**	CTRL_MODULE_CORE
Description	System DMA requests view channel 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000

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Bits	Field Name	Description	Type	Reset
6:0	MULT	Select one of the following signals : 0x72: hwobs_sdma_dma_req_114 0x6B: hwobs_sdma_dma_req_107 0x77: hwobs_sdma_dma_req_119 0x2E: hwobs_sdma_dma_req_46 0x48: hwobs_sdma_dma_req_72 0x60: hwobs_sdma_dma_req_96 0x36: hwobs_sdma_dma_req_54 0x7E: hwobs_sdma_dma_req_126 0x9: hwobs_sdma_dma_req_9 0x1D: hwobs_sdma_dma_req_29 0x14: hwobs_sdma_dma_req_20 0x25: hwobs_sdma_dma_req_37 0x64: hwobs_sdma_dma_req_100 0x20: hwobs_sdma_dma_req_32 0x17: hwobs_sdma_dma_req_23 0x5B: hwobs_sdma_dma_req_91 0x35: hwobs_sdma_dma_req_53 0x31: hwobs_sdma_dma_req_49 0x7B: hwobs_sdma_dma_req_123 0x12: hwobs_sdma_dma_req_18 0x4D: hwobs_sdma_dma_req_77 0x46: hwobs_sdma_dma_req_70 0x2B: hwobs_sdma_dma_req_43 0x37: hwobs_sdma_dma_req_55 0x38: hwobs_sdma_dma_req_56 0x30: hwobs_sdma_dma_req_48 0x51: hwobs_sdma_dma_req_81 0x49: hwobs_sdma_dma_req_73 0x55: hwobs_sdma_dma_req_85 0x73: hwobs_sdma_dma_req_115 0x4E: hwobs_sdma_dma_req_78 0x22: hwobs_sdma_dma_req_34 0x68: hwobs_sdma_dma_req_104 0x43: hwobs_sdma_dma_req_67 0x63: hwobs_sdma_dma_req_99 0x52: hwobs_sdma_dma_req_82 0x61: hwobs_sdma_dma_req_97 0x2: hwobs_sdma_dma_req_2 0x6D: hwobs_sdma_dma_req_109 0x7C: hwobs_sdma_dma_req_124 0x42: hwobs_sdma_dma_req_66 0x1: hwobs_sdma_dma_req_1 0x3F: hwobs_sdma_dma_req_63 0x71: hwobs_sdma_dma_req_113 0x0: hwobs_sdma_dma_req_0 0x7A: hwobs_sdma_dma_req_122 0x3E: hwobs_sdma_dma_req_62 0x6F: hwobs_sdma_dma_req_111	RW	0x00

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Bits	Field Name	Description	Type	Reset
		0x41: hwobs_sdma_dma_req_65		
		0x7D: hwobs_sdma_dma_req_125		
		0x4B: hwobs_sdma_dma_req_75		
		0x3: hwobs_sdma_dma_req_3		
		0x11: hwobs_sdma_dma_req_17		
		0xA: hwobs_sdma_dma_req_10		
		0x10: hwobs_sdma_dma_req_16		
		0x21: hwobs_sdma_dma_req_33		
		0x65: hwobs_sdma_dma_req_101		
		0xE: hwobs_sdma_dma_req_14		
		0x2A: hwobs_sdma_dma_req_42		
		0x7: hwobs_sdma_dma_req_7		
		0x6E: hwobs_sdma_dma_req_110		
		0x1A: hwobs_sdma_dma_req_26		
		0x53: hwobs_sdma_dma_req_83		
		0x3B: hwobs_sdma_dma_req_59		
		0x1E: hwobs_sdma_dma_req_30		
		0x8: hwobs_sdma_dma_req_8		
		0x78: hwobs_sdma_dma_req_120		
		0x6C: hwobs_sdma_dma_req_108		
		0x59: hwobs_sdma_dma_req_89		
		0x57: hwobs_sdma_dma_req_87		
		0x4: hwobs_sdma_dma_req_4		
		0x28: hwobs_sdma_dma_req_40		
		0x6A: hwobs_sdma_dma_req_106		
		0x45: hwobs_sdma_dma_req_69		
		0x3C: hwobs_sdma_dma_req_60		
		0xB: hwobs_sdma_dma_req_11		
		0x40: hwobs_sdma_dma_req_64		
		0x5A: hwobs_sdma_dma_req_90		
		0x19: hwobs_sdma_dma_req_25		
		0x56: hwobs_sdma_dma_req_86		
		0x32: hwobs_sdma_dma_req_50		
		0x58: hwobs_sdma_dma_req_88		
		0x54: hwobs_sdma_dma_req_84		
		0x5E: hwobs_sdma_dma_req_94		
		0x69: hwobs_sdma_dma_req_105		
		0x4F: hwobs_sdma_dma_req_79		
		0x66: hwobs_sdma_dma_req_102		
		0x16: hwobs_sdma_dma_req_22		
		0x50: hwobs_sdma_dma_req_80		
		0x1C: hwobs_sdma_dma_req_28		
		0x5C: hwobs_sdma_dma_req_92		
		0x47: hwobs_sdma_dma_req_71		
		0x74: hwobs_sdma_dma_req_116		
		0x76: hwobs_sdma_dma_req_118		
		0x2F: hwobs_sdma_dma_req_47		
		0x3A: hwobs_sdma_dma_req_58		
		0x39: hwobs_sdma_dma_req_57		

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Bits	Field Name	Description	Type	Reset
		0x27: hwobs_sdma_dma_req_39		
		0xD: hwobs_sdma_dma_req_13		
		0x33: hwobs_sdma_dma_req_51		
		0x15: hwobs_sdma_dma_req_21		
		0x62: hwobs_sdma_dma_req_98		
		0x1B: hwobs_sdma_dma_req_27		
		0x2C: hwobs_sdma_dma_req_44		
		0x79: hwobs_sdma_dma_req_121		
		0x5: hwobs_sdma_dma_req_5		
		0x6: hwobs_sdma_dma_req_6		
		0x24: hwobs_sdma_dma_req_36		
		0x2D: hwobs_sdma_dma_req_45		
		0x3D: hwobs_sdma_dma_req_61		
		0x75: hwobs_sdma_dma_req_117		
		0x23: hwobs_sdma_dma_req_35		
		0x44: hwobs_sdma_dma_req_68		
		0x26: hwobs_sdma_dma_req_38		
		0x5F: hwobs_sdma_dma_req_95		
		0x4C: hwobs_sdma_dma_req_76		
		0x34: hwobs_sdma_dma_req_52		
		0x13: hwobs_sdma_dma_req_19		
		0x18: hwobs_sdma_dma_req_24		
		0x5D: hwobs_sdma_dma_req_93		
		0x4A: hwobs_sdma_dma_req_74		
		0x70: hwobs_sdma_dma_req_112		
		0x67: hwobs_sdma_dma_req_103		
		0x1F: hwobs_sdma_dma_req_31		
		0x29: hwobs_sdma_dma_req_41		
		0xF: hwobs_sdma_dma_req_15		
		0xC: hwobs_sdma_dma_req_12		

Table 18-327. Register Call Summary for Register CONTROL_CONF_SDMA_REQ_SEL0

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-328. CONTROL_CONF_SDMA_REQ_SEL1

Address Offset	0x0000 0430		
Physical Address	0x4A00 2430	**Instance**	CTRL_MODULE_CORE
Description	System DMA requests view channel 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MULT							

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000

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Bits	Field Name	Description	Type	Reset
6:0	MULT	Select one of the following signals : 0x72: hwobs_sdma_dma_req_114 0x6B: hwobs_sdma_dma_req_107 0x77: hwobs_sdma_dma_req_119 0x2E: hwobs_sdma_dma_req_46 0x48: hwobs_sdma_dma_req_72 0x60: hwobs_sdma_dma_req_96 0x36: hwobs_sdma_dma_req_54 0x7E: hwobs_sdma_dma_req_126 0x9: hwobs_sdma_dma_req_9 0x1D: hwobs_sdma_dma_req_29 0x14: hwobs_sdma_dma_req_20 0x25: hwobs_sdma_dma_req_37 0x64: hwobs_sdma_dma_req_100 0x20: hwobs_sdma_dma_req_32 0x17: hwobs_sdma_dma_req_23 0x5B: hwobs_sdma_dma_req_91 0x35: hwobs_sdma_dma_req_53 0x31: hwobs_sdma_dma_req_49 0x7B: hwobs_sdma_dma_req_123 0x12: hwobs_sdma_dma_req_18 0x4D: hwobs_sdma_dma_req_77 0x46: hwobs_sdma_dma_req_70 0x2B: hwobs_sdma_dma_req_43 0x37: hwobs_sdma_dma_req_55 0x38: hwobs_sdma_dma_req_56 0x30: hwobs_sdma_dma_req_48 0x51: hwobs_sdma_dma_req_81 0x49: hwobs_sdma_dma_req_73 0x55: hwobs_sdma_dma_req_85 0x73: hwobs_sdma_dma_req_115 0x4E: hwobs_sdma_dma_req_78 0x22: hwobs_sdma_dma_req_34 0x68: hwobs_sdma_dma_req_104 0x43: hwobs_sdma_dma_req_67 0x63: hwobs_sdma_dma_req_99 0x52: hwobs_sdma_dma_req_82 0x61: hwobs_sdma_dma_req_97 0x2: hwobs_sdma_dma_req_2 0x6D: hwobs_sdma_dma_req_109 0x7C: hwobs_sdma_dma_req_124 0x42: hwobs_sdma_dma_req_66 0x1: hwobs_sdma_dma_req_1 0x3F: hwobs_sdma_dma_req_63 0x71: hwobs_sdma_dma_req_113 0x0: hwobs_sdma_dma_req_0 0x7A: hwobs_sdma_dma_req_122 0x3E: hwobs_sdma_dma_req_62 0x6F: hwobs_sdma_dma_req_111	RW	0x01

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Bits	Field Name	Description	Type	Reset
		0x41: hwobs_sdma_dma_req_65		
		0x7D: hwobs_sdma_dma_req_125		
		0x4B: hwobs_sdma_dma_req_75		
		0x3: hwobs_sdma_dma_req_3		
		0x11: hwobs_sdma_dma_req_17		
		0xA: hwobs_sdma_dma_req_10		
		0x10: hwobs_sdma_dma_req_16		
		0x21: hwobs_sdma_dma_req_33		
		0x65: hwobs_sdma_dma_req_101		
		0xE: hwobs_sdma_dma_req_14		
		0x2A: hwobs_sdma_dma_req_42		
		0x7: hwobs_sdma_dma_req_7		
		0x6E: hwobs_sdma_dma_req_110		
		0x1A: hwobs_sdma_dma_req_26		
		0x53: hwobs_sdma_dma_req_83		
		0x3B: hwobs_sdma_dma_req_59		
		0x1E: hwobs_sdma_dma_req_30		
		0x8: hwobs_sdma_dma_req_8		
		0x78: hwobs_sdma_dma_req_120		
		0x6C: hwobs_sdma_dma_req_108		
		0x59: hwobs_sdma_dma_req_89		
		0x57: hwobs_sdma_dma_req_87		
		0x4: hwobs_sdma_dma_req_4		
		0x28: hwobs_sdma_dma_req_40		
		0x6A: hwobs_sdma_dma_req_106		
		0x45: hwobs_sdma_dma_req_69		
		0x3C: hwobs_sdma_dma_req_60		
		0xB: hwobs_sdma_dma_req_11		
		0x40: hwobs_sdma_dma_req_64		
		0x5A: hwobs_sdma_dma_req_90		
		0x19: hwobs_sdma_dma_req_25		
		0x56: hwobs_sdma_dma_req_86		
		0x32: hwobs_sdma_dma_req_50		
		0x58: hwobs_sdma_dma_req_88		
		0x54: hwobs_sdma_dma_req_84		
		0x5E: hwobs_sdma_dma_req_94		
		0x69: hwobs_sdma_dma_req_105		
		0x4F: hwobs_sdma_dma_req_79		
		0x66: hwobs_sdma_dma_req_102		
		0x16: hwobs_sdma_dma_req_22		
		0x50: hwobs_sdma_dma_req_80		
		0x1C: hwobs_sdma_dma_req_28		
		0x5C: hwobs_sdma_dma_req_92		
		0x47: hwobs_sdma_dma_req_71		
		0x74: hwobs_sdma_dma_req_116		
		0x76: hwobs_sdma_dma_req_118		
		0x2F: hwobs_sdma_dma_req_47		
		0x3A: hwobs_sdma_dma_req_58		
		0x39: hwobs_sdma_dma_req_57		

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Bits	Field Name	Description	Type	Reset
		0x27: hwobs_sdma_dma_req_39 0xD: hwobs_sdma_dma_req_13 0x33: hwobs_sdma_dma_req_51 0x15: hwobs_sdma_dma_req_21 0x62: hwobs_sdma_dma_req_98 0x1B: hwobs_sdma_dma_req_27 0x2C: hwobs_sdma_dma_req_44 0x79: hwobs_sdma_dma_req_121 0x5: hwobs_sdma_dma_req_5 0x6: hwobs_sdma_dma_req_6 0x24: hwobs_sdma_dma_req_36 0x2D: hwobs_sdma_dma_req_45 0x3D: hwobs_sdma_dma_req_61 0x75: hwobs_sdma_dma_req_117 0x23: hwobs_sdma_dma_req_35 0x44: hwobs_sdma_dma_req_68 0x26: hwobs_sdma_dma_req_38 0x5F: hwobs_sdma_dma_req_95 0x4C: hwobs_sdma_dma_req_76 0x34: hwobs_sdma_dma_req_52 0x13: hwobs_sdma_dma_req_19 0x18: hwobs_sdma_dma_req_24 0x5D: hwobs_sdma_dma_req_93 0x4A: hwobs_sdma_dma_req_74 0x70: hwobs_sdma_dma_req_112 0x67: hwobs_sdma_dma_req_103 0x1F: hwobs_sdma_dma_req_31 0x29: hwobs_sdma_dma_req_41 0xF: hwobs_sdma_dma_req_15 0xC: hwobs_sdma_dma_req_12		

Table 18-329. Register Call Summary for Register CONTROL_CONF_SDMA_REQ_SEL1

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-330. CONTROL_CONF_SDMA_REQ_SEL2

Address Offset	0x0000 0434		
Physical Address	0x4A00 2434	**Instance**	CTRL_MODULE_CORE
Description	System DMA requests view channel 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MULT							

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000

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Bits	Field Name	Description	Type	Reset
6:0	MULT	Select one of the following signals : 0x72: hwobs_sdma_dma_req_114 0x6B: hwobs_sdma_dma_req_107 0x77: hwobs_sdma_dma_req_119 0x2E: hwobs_sdma_dma_req_46 0x48: hwobs_sdma_dma_req_72 0x60: hwobs_sdma_dma_req_96 0x36: hwobs_sdma_dma_req_54 0x7E: hwobs_sdma_dma_req_126 0x9: hwobs_sdma_dma_req_9 0x1D: hwobs_sdma_dma_req_29 0x14: hwobs_sdma_dma_req_20 0x25: hwobs_sdma_dma_req_37 0x64: hwobs_sdma_dma_req_100 0x20: hwobs_sdma_dma_req_32 0x17: hwobs_sdma_dma_req_23 0x5B: hwobs_sdma_dma_req_91 0x35: hwobs_sdma_dma_req_53 0x31: hwobs_sdma_dma_req_49 0x7B: hwobs_sdma_dma_req_123 0x12: hwobs_sdma_dma_req_18 0x4D: hwobs_sdma_dma_req_77 0x46: hwobs_sdma_dma_req_70 0x2B: hwobs_sdma_dma_req_43 0x37: hwobs_sdma_dma_req_55 0x38: hwobs_sdma_dma_req_56 0x30: hwobs_sdma_dma_req_48 0x51: hwobs_sdma_dma_req_81 0x49: hwobs_sdma_dma_req_73 0x55: hwobs_sdma_dma_req_85 0x73: hwobs_sdma_dma_req_115 0x4E: hwobs_sdma_dma_req_78 0x22: hwobs_sdma_dma_req_34 0x68: hwobs_sdma_dma_req_104 0x43: hwobs_sdma_dma_req_67 0x63: hwobs_sdma_dma_req_99 0x52: hwobs_sdma_dma_req_82 0x61: hwobs_sdma_dma_req_97 0x2: hwobs_sdma_dma_req_2 0x6D: hwobs_sdma_dma_req_109 0x7C: hwobs_sdma_dma_req_124 0x42: hwobs_sdma_dma_req_66 0x1: hwobs_sdma_dma_req_1 0x3F: hwobs_sdma_dma_req_63 0x71: hwobs_sdma_dma_req_113 0x0: hwobs_sdma_dma_req_0 0x7A: hwobs_sdma_dma_req_122 0x3E: hwobs_sdma_dma_req_62 0x6F: hwobs_sdma_dma_req_111	RW	0x02

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Bits	Field Name	Description	Type	Reset
		0x41: hwobs_sdma_dma_req_65		
		0x7D: hwobs_sdma_dma_req_125		
		0x4B: hwobs_sdma_dma_req_75		
		0x3: hwobs_sdma_dma_req_3		
		0x11: hwobs_sdma_dma_req_17		
		0xA: hwobs_sdma_dma_req_10		
		0x10: hwobs_sdma_dma_req_16		
		0x21: hwobs_sdma_dma_req_33		
		0x65: hwobs_sdma_dma_req_101		
		0xE: hwobs_sdma_dma_req_14		
		0x2A: hwobs_sdma_dma_req_42		
		0x7: hwobs_sdma_dma_req_7		
		0x6E: hwobs_sdma_dma_req_110		
		0x1A: hwobs_sdma_dma_req_26		
		0x53: hwobs_sdma_dma_req_83		
		0x3B: hwobs_sdma_dma_req_59		
		0x1E: hwobs_sdma_dma_req_30		
		0x8: hwobs_sdma_dma_req_8		
		0x78: hwobs_sdma_dma_req_120		
		0x6C: hwobs_sdma_dma_req_108		
		0x59: hwobs_sdma_dma_req_89		
		0x57: hwobs_sdma_dma_req_87		
		0x4: hwobs_sdma_dma_req_4		
		0x28: hwobs_sdma_dma_req_40		
		0x6A: hwobs_sdma_dma_req_106		
		0x45: hwobs_sdma_dma_req_69		
		0x3C: hwobs_sdma_dma_req_60		
		0xB: hwobs_sdma_dma_req_11		
		0x40: hwobs_sdma_dma_req_64		
		0x5A: hwobs_sdma_dma_req_90		
		0x19: hwobs_sdma_dma_req_25		
		0x56: hwobs_sdma_dma_req_86		
		0x32: hwobs_sdma_dma_req_50		
		0x58: hwobs_sdma_dma_req_88		
		0x54: hwobs_sdma_dma_req_84		
		0x5E: hwobs_sdma_dma_req_94		
		0x69: hwobs_sdma_dma_req_105		
		0x4F: hwobs_sdma_dma_req_79		
		0x66: hwobs_sdma_dma_req_102		
		0x16: hwobs_sdma_dma_req_22		
		0x50: hwobs_sdma_dma_req_80		
		0x1C: hwobs_sdma_dma_req_28		
		0x5C: hwobs_sdma_dma_req_92		
		0x47: hwobs_sdma_dma_req_71		
		0x74: hwobs_sdma_dma_req_116		
		0x76: hwobs_sdma_dma_req_118		
		0x2F: hwobs_sdma_dma_req_47		
		0x3A: hwobs_sdma_dma_req_58		
		0x39: hwobs_sdma_dma_req_57		

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Bits	Field Name	Description	Type	Reset
		0x27: hwobs_sdma_dma_req_39		
		0xD: hwobs_sdma_dma_req_13		
		0x33: hwobs_sdma_dma_req_51		
		0x15: hwobs_sdma_dma_req_21		
		0x62: hwobs_sdma_dma_req_98		
		0x1B: hwobs_sdma_dma_req_27		
		0x2C: hwobs_sdma_dma_req_44		
		0x79: hwobs_sdma_dma_req_121		
		0x5: hwobs_sdma_dma_req_5		
		0x6: hwobs_sdma_dma_req_6		
		0x24: hwobs_sdma_dma_req_36		
		0x2D: hwobs_sdma_dma_req_45		
		0x3D: hwobs_sdma_dma_req_61		
		0x75: hwobs_sdma_dma_req_117		
		0x23: hwobs_sdma_dma_req_35		
		0x44: hwobs_sdma_dma_req_68		
		0x26: hwobs_sdma_dma_req_38		
		0x5F: hwobs_sdma_dma_req_95		
		0x4C: hwobs_sdma_dma_req_76		
		0x34: hwobs_sdma_dma_req_52		
		0x13: hwobs_sdma_dma_req_19		
		0x18: hwobs_sdma_dma_req_24		
		0x5D: hwobs_sdma_dma_req_93		
		0x4A: hwobs_sdma_dma_req_74		
		0x70: hwobs_sdma_dma_req_112		
		0x67: hwobs_sdma_dma_req_103		
		0x1F: hwobs_sdma_dma_req_31		
		0x29: hwobs_sdma_dma_req_41		
		0xF: hwobs_sdma_dma_req_15		
		0xC: hwobs_sdma_dma_req_12		

Table 18-331. Register Call Summary for Register CONTROL_CONF_SDMA_REQ_SEL2

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [0]

Table 18-332. CONTROL_CONF_SDMA_REQ_SEL3

Address Offset	0x0000 0438		
Physical Address	0x4A00 2438	**Instance**	CTRL_MODULE_CORE
Description	System DMA requests view channel 3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MULT							

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Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000

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Bits	Field Name	Description	Type	Reset
6:0	MULT	Select one of the following signals : 0x72: hwobs_sdma_dma_req_114 0x6B: hwobs_sdma_dma_req_107 0x77: hwobs_sdma_dma_req_119 0x2E: hwobs_sdma_dma_req_46 0x48: hwobs_sdma_dma_req_72 0x60: hwobs_sdma_dma_req_96 0x36: hwobs_sdma_dma_req_54 0x7E: hwobs_sdma_dma_req_126 0x9: hwobs_sdma_dma_req_9 0x1D: hwobs_sdma_dma_req_29 0x14: hwobs_sdma_dma_req_20 0x25: hwobs_sdma_dma_req_37 0x64: hwobs_sdma_dma_req_100 0x20: hwobs_sdma_dma_req_32 0x17: hwobs_sdma_dma_req_23 0x5B: hwobs_sdma_dma_req_91 0x35: hwobs_sdma_dma_req_53 0x31: hwobs_sdma_dma_req_49 0x7B: hwobs_sdma_dma_req_123 0x12: hwobs_sdma_dma_req_18 0x4D: hwobs_sdma_dma_req_77 0x46: hwobs_sdma_dma_req_70 0x2B: hwobs_sdma_dma_req_43 0x37: hwobs_sdma_dma_req_55 0x38: hwobs_sdma_dma_req_56 0x30: hwobs_sdma_dma_req_48 0x51: hwobs_sdma_dma_req_81 0x49: hwobs_sdma_dma_req_73 0x55: hwobs_sdma_dma_req_85 0x73: hwobs_sdma_dma_req_115 0x4E: hwobs_sdma_dma_req_78 0x22: hwobs_sdma_dma_req_34 0x68: hwobs_sdma_dma_req_104 0x43: hwobs_sdma_dma_req_67 0x63: hwobs_sdma_dma_req_99 0x52: hwobs_sdma_dma_req_82 0x61: hwobs_sdma_dma_req_97 0x2: hwobs_sdma_dma_req_2 0x6D: hwobs_sdma_dma_req_109 0x7C: hwobs_sdma_dma_req_124 0x42: hwobs_sdma_dma_req_66 0x1: hwobs_sdma_dma_req_1 0x3F: hwobs_sdma_dma_req_63 0x71: hwobs_sdma_dma_req_113 0x0: hwobs_sdma_dma_req_0 0x7A: hwobs_sdma_dma_req_122 0x3E: hwobs_sdma_dma_req_62 0x6F: hwobs_sdma_dma_req_111	RW	0x03

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Bits	Field Name	Description	Type	Reset
		0x41: hwobs_sdma_dma_req_65		
		0x7D: hwobs_sdma_dma_req_125		
		0x4B: hwobs_sdma_dma_req_75		
		0x3: hwobs_sdma_dma_req_3		
		0x11: hwobs_sdma_dma_req_17		
		0xA: hwobs_sdma_dma_req_10		
		0x10: hwobs_sdma_dma_req_16		
		0x21: hwobs_sdma_dma_req_33		
		0x65: hwobs_sdma_dma_req_101		
		0xE: hwobs_sdma_dma_req_14		
		0x2A: hwobs_sdma_dma_req_42		
		0x7: hwobs_sdma_dma_req_7		
		0x6E: hwobs_sdma_dma_req_110		
		0x1A: hwobs_sdma_dma_req_26		
		0x53: hwobs_sdma_dma_req_83		
		0x3B: hwobs_sdma_dma_req_59		
		0x1E: hwobs_sdma_dma_req_30		
		0x8: hwobs_sdma_dma_req_8		
		0x78: hwobs_sdma_dma_req_120		
		0x6C: hwobs_sdma_dma_req_108		
		0x59: hwobs_sdma_dma_req_89		
		0x57: hwobs_sdma_dma_req_87		
		0x4: hwobs_sdma_dma_req_4		
		0x28: hwobs_sdma_dma_req_40		
		0x6A: hwobs_sdma_dma_req_106		
		0x45: hwobs_sdma_dma_req_69		
		0x3C: hwobs_sdma_dma_req_60		
		0xB: hwobs_sdma_dma_req_11		
		0x40: hwobs_sdma_dma_req_64		
		0x5A: hwobs_sdma_dma_req_90		
		0x19: hwobs_sdma_dma_req_25		
		0x56: hwobs_sdma_dma_req_86		
		0x32: hwobs_sdma_dma_req_50		
		0x58: hwobs_sdma_dma_req_88		
		0x54: hwobs_sdma_dma_req_84		
		0x5E: hwobs_sdma_dma_req_94		
		0x69: hwobs_sdma_dma_req_105		
		0x4F: hwobs_sdma_dma_req_79		
		0x66: hwobs_sdma_dma_req_102		
		0x16: hwobs_sdma_dma_req_22		
		0x50: hwobs_sdma_dma_req_80		
		0x1C: hwobs_sdma_dma_req_28		
		0x5C: hwobs_sdma_dma_req_92		
		0x47: hwobs_sdma_dma_req_71		
		0x74: hwobs_sdma_dma_req_116		
		0x76: hwobs_sdma_dma_req_118		
		0x2F: hwobs_sdma_dma_req_47		
		0x3A: hwobs_sdma_dma_req_58		
		0x39: hwobs_sdma_dma_req_57		

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Bits	Field Name	Description	Type	Reset
		0x27: hwobs_sdma_dma_req_39		
		0xD: hwobs_sdma_dma_req_13		
		0x33: hwobs_sdma_dma_req_51		
		0x15: hwobs_sdma_dma_req_21		
		0x62: hwobs_sdma_dma_req_98		
		0x1B: hwobs_sdma_dma_req_27		
		0x2C: hwobs_sdma_dma_req_44		
		0x79: hwobs_sdma_dma_req_121		
		0x5: hwobs_sdma_dma_req_5		
		0x6: hwobs_sdma_dma_req_6		
		0x24: hwobs_sdma_dma_req_36		
		0x2D: hwobs_sdma_dma_req_45		
		0x3D: hwobs_sdma_dma_req_61		
		0x75: hwobs_sdma_dma_req_117		
		0x23: hwobs_sdma_dma_req_35		
		0x44: hwobs_sdma_dma_req_68		
		0x26: hwobs_sdma_dma_req_38		
		0x5F: hwobs_sdma_dma_req_95		
		0x4C: hwobs_sdma_dma_req_76		
		0x34: hwobs_sdma_dma_req_52		
		0x13: hwobs_sdma_dma_req_19		
		0x18: hwobs_sdma_dma_req_24		
		0x5D: hwobs_sdma_dma_req_93		
		0x4A: hwobs_sdma_dma_req_74		
		0x70: hwobs_sdma_dma_req_112		
		0x67: hwobs_sdma_dma_req_103		
		0x1F: hwobs_sdma_dma_req_31		
		0x29: hwobs_sdma_dma_req_41		
		0xF: hwobs_sdma_dma_req_15		
		0xC: hwobs_sdma_dma_req_12		

Table 18-333. Register Call Summary for Register CONTROL_CONF_SDMA_REQ_SEL3

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-334. CONTROL_CONF_CLK_SEL0

Address Offset	0x0000 0440		
Physical Address	0x4A00 2440	**Instance**	CTRL_MODULE_CORE
Description	clk view channel 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x6: hwobs_satadpll_clkout 0x1: hwobs_abedpll_clkout 0xA: Reserved 0x7: hwobs_usbotgssdpll_clkout 0x0: hwobs_coredpll_clkout 0x2: hwobs_perdpll_clkout 0x8: hwobs_usbdpll_clkout 0x9: Reserved 0x4: hwobs_dsi1cdpll_clkout 0x5: hwobs_hdmidpll_clkout 0x3: hwobs_dsi1adpll_clkout	RW	0x0

Table 18-335. Register Call Summary for Register CONTROL_CONF_CLK_SEL0

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-336. CONTROL_CONF_CLK_SEL1

Address Offset	0x0000 0444		
Physical Address	0x4A00 2444	**Instance**	CTRL_MODULE_CORE
Description	clk view channel 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x6: hwobs_satadpll_clkout 0x1: hwobs_abedpll_clkout 0xA: Reserved 0x7: hwobs_usbotgssdpll_clkout 0x0: hwobs_coredpll_clkout 0x2: hwobs_perdpll_clkout 0x8: hwobs_usbdpll_clkout 0x9: Reserved 0x4: hwobs_dsi1cdpll_clkout 0x5: hwobs_hdmidpll_clkout 0x3: hwobs_dsi1adpll_clkout	RW	0x1

Table 18-337. Register Call Summary for Register CONTROL_CONF_CLK_SEL1

Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [0]

Table 18-338. CONTROL_CONF_CLK_SEL2

Address Offset	0x0000 0448		
Physical Address	0x4A00 2448	**Instance**	CTRL_MODULE_CORE
Description	clk view channel 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x6: hwobs_satadpll_clkout 0x1: hwobs_abedpll_clkout 0xA: Reserved 0x7: hwobs_usbotgssdpll_clkout 0x0: hwobs_coredpll_clkout 0x2: hwobs_perdpll_clkout 0x8: hwobs_usbdpll_clkout 0x9: Reserved 0x4: hwobs_dsi1cdpll_clkout 0x5: hwobs_hdmidpll_clkout 0x3: hwobs_dsi1adpll_clkout	RW	0x2

Table 18-339. Register Call Summary for Register CONTROL_CONF_CLK_SEL2

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]

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Table 18-339. Register Call Summary for Register CONTROL_CONF_CLK_SEL2 (continued)

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [3]

Table 18-340. CONTROL_CONF_DPLL_FREQLOCK_SEL

Address Offset	0x0000 044C		
Physical Address	0x4A00 244C	**Instance**	CTRL_MODULE_CORE
Description	dpll_freqlock view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x6: hwobs_satadpll_freqlock 0x1: hwobs_abedpll_freqlock 0xA: Reserved 0x7: hwobs_usbotgssdpll_freqlock 0x0: hwobs_coredpll_freqlock 0x2: hwobs_perdpll_freqlock 0x8: hwobs_usbdpll_freqlock 0x9: Reserved 0x4: hwobs_dsi1cdpll_freqlock 0x5: hwobs_hdmidpll_freqlock 0x3: hwobs_dsi1adpll_freqlock	RW	0x0

Table 18-341. Register Call Summary for Register CONTROL_CONF_DPLL_FREQLOCK_SEL

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
- Other CORE DPLL Observable Signals: [2]
- Other ABE DPLL Observable Signals: [3]
- Other PERIPH DPLL Observable Signals: [4]
- Other DSI1_A DPLL Observable Signals: [5]
- Other DSI1_C DPLL Observable Signals: [6]
- Other HDMI DPLL Observable Signals: [7]
- Other USBOTGSS DPLL Observable Signals: [8]
- Other USB DPLL Observable Signals: [9]
- Other SATA DPLL Observable Signals: [10]

Control Module Programming Guide
- Hardware Observability Settings: [11]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [12]

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Table 18-342. CONTROL_CONF_DPLL_TINITZ_SEL

Address Offset	0x0000 0450		
Physical Address	0x4A00 2450	**Instance**	CTRL_MODULE_CORE
Description	dpll_tinitz view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x0: hwobs_coredpll_tinitz	RW	0x0

Table 18-343. Register Call Summary for Register CONTROL_CONF_DPLL_TINITZ_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-344. CONTROL_CONF_DPLL_PHASELOCK_SEL

Address Offset	0x0000 0454		
Physical Address	0x4A00 2454	**Instance**	CTRL_MODULE_CORE
Description	dpll_phaselock view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x6: hwobs_satadpll_phaselock 0x1: hwobs_abedpll_phaselock 0xA: Reserved 0x7: hwobs_usbotgssdpll_phaselock 0x0: hwobs_coredpll_phaselock 0x2: hwobs_perdpll_phaselock 0x8: hwobs_usbdpll_phaselock 0x9: Reserved 0x4: hwobs_dsi1cdpll_phaselock 0x5: hwobs_hdmidpll_phaselock 0x3: hwobs_dsi1adpll_phaselock	RW	0x0

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Table 18-345. Register Call Summary for Register CONTROL_CONF_DPLL_PHASELOCK_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-346. CONTROL_CONF_DPLL_TENABLE_SEL

Address Offset	0x0000 0458		
Physical Address	0x4A00 2458	**Instance**	CTRL_MODULE_CORE
Description	dpll_tenable view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x6: hwobs_satadpll_tenable 0x1: hwobs_abedpll_tenable 0xA: Reserved 0x7: hwobs_usbotgssdpll_tenable 0x0: hwobs_coredpll_tenable 0x2: hwobs_perdpll_tenable 0x8: hwobs_usbdpll_tenable 0x9: Reserved 0x4: hwobs_dsi1cdpll_tenable 0x5: hwobs_hdmidpll_tenable 0x3: hwobs_dsi1adpll_tenable	RW	0x0

Table 18-347. Register Call Summary for Register CONTROL_CONF_DPLL_TENABLE_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-348. CONTROL_CONF_DPLL_TENABLEDIV_SEL

Address Offset	0x0000 045C		
Physical Address	0x4A00 245C	**Instance**	CTRL_MODULE_CORE
Description	dpll_tenablediv view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x6: hwobs_satadpll_tenablediv 0x1: hwobs_abedpll_tenablediv 0xA: Reserved 0x7: hwobs_usbotgssdpll_tenablediv 0x0: hwobs_coredpll_tenablediv 0x2: hwobs_perdpll_tenablediv 0x8: hwobs_usbdpll_tenablediv 0x9: Reserved 0x4: hwobs_dsi1cdpll_tenablediv 0x5: hwobs_hdmidpll_tenablediv 0x3: hwobs_dsi1adpll_tenablediv	RW	0x0

Table 18-349. Register Call Summary for Register CONTROL_CONF_DPLL_TENABLEDIV_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-350. CONTROL_CONF_DPLL_BYPASSACK_SEL

Address Offset	0x0000 0460		
Physical Address	0x4A00 2460	**Instance**	CTRL_MODULE_CORE
Description	dpll_bypassack view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x6: hwobs_satadpll_bypassack 0x1: hwobs_abedpll_bypassack 0xA: Reserved 0x7: hwobs_usbotgssdpll_bypassack 0x0: hwobs_coredpll_bypassack 0x2: hwobs_perdpll_bypassack 0x8: hwobs_usbdpll_bypassack 0x9: Reserved 0x4: hwobs_dsi1cdpll_bypassack 0x5: hwobs_hdmidpll_bypassack 0x3: hwobs_dsi1adpll_bypassack	RW	0x0

Table 18-351. Register Call Summary for Register CONTROL_CONF_DPLL_BYPASSACK_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-352. CONTROL_CONF_DPLL_IDLE_SEL

Address Offset	0x0000 0464		
Physical Address	0x4A00 2464	**Instance**	CTRL_MODULE_CORE
Description	dpll_idle view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MULT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	MULT	Select one of the following signals : 0x6: hwobs_satadpll_idle 0x1: hwobs_abedpll_idle 0xA: Reserved 0x7: hwobs_usbotgssdpll_idle 0x0: hwobs_coredpll_idle 0x2: hwobs_perdpll_idle 0x8: hwobs_usbdpll_idle 0x9: Reserved 0x4: hwobs_dsi1cdpll_idle 0x5: hwobs_hdmidpll_idle 0x3: hwobs_dsi1adpll_idle	RW	0x0

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Table 18-353. Register Call Summary for Register CONTROL_CONF_DPLL_IDLE_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1] • Other CORE DPLL Observable Signals: [2] • Other ABE DPLL Observable Signals: [3] • Other PERIPH DPLL Observable Signals: [4] • Other DSI1_A DPLL Observable Signals: [5] • Other DSI1_C DPLL Observable Signals: [6] • Other HDMI DPLL Observable Signals: [7] • Other USBOTGSS DPLL Observable Signals: [8] • Other USB DPLL Observable Signals: [9] • Other SATA DPLL Observable Signals: [10]
Control Module Programming Guide • Hardware Observability Settings: [11]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [12]

Table 18-354. CONTROL_CONF_DPLLCTRL_PLLLOCK_SEL

Address Offset	0x0000 0468		
Physical Address	0x4A00 2468	**Instance**	CTRL_MODULE_CORE
Description	dpllctrl_plllock view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MULT		

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_dsi1a_plllock 0x1: hwobs_dsi1c_plllock 0x3: hwobs_sata_plllock 0x4: hwobs_usbotgss_plllock 0x2: hwobs_hdmi_plllock	RW	0x0

Table 18-355. Register Call Summary for Register CONTROL_CONF_DPLLCTRL_PLLLOCK_SEL

Control Module Programming Guide • Hardware Observability Settings: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-356. CONTROL_CONF_DPLLCTRL_PLLRECAL_SEL

Address Offset	0x0000 046C		
Physical Address	0x4A00 246C	**Instance**	CTRL_MODULE_CORE
Description	dpllctrl_pllrecal view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MULT		

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_dsi1a_pllrecal 0x1: hwobs_dsi1c_pllrecal 0x3: hwobs_sata_pllrecal 0x4: hwobs_usbotgss_pllrecal 0x2: hwobs_hdmi_pllrecal	RW	0x0

Table 18-357. Register Call Summary for Register CONTROL_CONF_DPLLCTRL_PLLRECAL_SEL

Control Module Programming Guide • Hardware Observability Settings: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-358. CONTROL_CONF_DPLLCTRL_STOPCLOCK_SEL

Address Offset	0x0000 0470		
Physical Address	0x4A00 2470	**Instance**	CTRL_MODULE_CORE
Description	dpllctrl_stopclock view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MULT		

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_dsi1a_stopclock 0x1: hwobs_dsi1c_stopclock 0x3: hwobs_sata_stopclock 0x4: hwobs_usbotgss_stopclock 0x2: hwobs_hdmi_stopclock	RW	0x0

Table 18-359. Register Call Summary for Register CONTROL_CONF_DPLLCTRL_STOPCLOCK_SEL

Control Module Programming Guide • Hardware Observability Settings: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-360. CONTROL_CONF_DPLLCTRL_STOPCLOCKACKZ_SEL

Address Offset	0x0000 0474		
Physical Address	0x4A00 2474	**Instance**	CTRL_MODULE_CORE
Description	dpllctrl_stopclockackz view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MULT		

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_dsi1a_stopclockackz 0x1: hwobs_dsi1c_stopclockackz 0x3: hwobs_sata_stopclockackz 0x4: hwobs_usbotgss_stopclockackz 0x2: hwobs_hdmi_stopclockackz	RW	0x0

Table 18-361. Register Call Summary for Register CONTROL_CONF_DPLLCTRL_STOPCLOCKACKZ_SEL

Control Module Programming Guide • Hardware Observability Settings: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-362. CONTROL_CONF_DPLLCTRL_DISPCUPDATESYNC_SEL

Address Offset	0x0000 0478		
Physical Address	0x4A00 2478	**Instance**	CTRL_MODULE_CORE
Description	dpllctrl_dispcupdatesync view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													MULT		

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_dsi1a_dispcupdatesync 0x1: hwobs_dsi1c_dispcupdatesync 0x3: hwobs_sata_dispcupdatesync 0x4: hwobs_usbotgss_dispcupdatesync 0x2: hwobs_hdmi_dispcupdatesync	RW	0x0

Table 18-363. Register Call Summary for Register CONTROL_CONF_DPLLCTRL_DISPCUPDATESYNC_SEL

Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [0]

Table 18-364. CONTROL_CONF_DPLLCTRL_SCPCMD0_SEL

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Table 18-365. CONTROL_CONF_MMCX_ADPIDLE_SEL

Address Offset	0x0000 04AC		
Physical Address	0x4A00 24AC	**Instance**	CTRL_MODULE_CORE
Description	conf_mmcx_adpidle_view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_mmc1_adpidle 0x1: hwobs_mmc2_adpidle 0x3: hwobs_mmc4_adpidle 0x4: hwobs_mmc5_adpidle 0x2: hwobs_mmc3_adpidle	RW	0x0

Table 18-366. Register Call Summary for Register CONTROL_CONF_MMCX_ADPIDLE_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-367. CONTROL_CONF_MMCX_ADPDAT1PADEN_SEL

Address Offset	0x0000 04B0		
Physical Address	0x4A00 24B0	**Instance**	CTRL_MODULE_CORE
Description	conf_mmcx_adpdat1paden_view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_mmc1_adpdat1paden 0x1: hwobs_mmc2_adpdat1paden 0x3: hwobs_mmc4_adpdat1paden 0x4: hwobs_mmc5_adpdat1paden 0x2: hwobs_mmc3_adpdat1paden	RW	0x0

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Table 18-368. Register Call Summary for Register CONTROL_CONF_MMCX_ADPDAT1PADEN_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Programming Guide • Hardware Observability Settings: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-369. CONTROL_CONF_MMCX_OCPL4IDLEREQ_SEL

Address Offset	0x0000 04B4		
Physical Address	0x4A00 24B4	**Instance**	CTRL_MODULE_CORE
Description	conf_mmcx_ocpl4idlereq_view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_mmc1_ocpl4idlereq 0x1: hwobs_mmc2_ocpl4idlereq 0x3: hwobs_mmc4_ocpl4idlereq 0x4: hwobs_mmc5_ocpl4idlereq 0x2: hwobs_mmc3_ocpl4idlereq	RW	0x0

Table 18-370. Register Call Summary for Register CONTROL_CONF_MMCX_OCPL4IDLEREQ_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Programming Guide • Hardware Observability Settings: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-371. CONTROL_CONF_MMCX_OCPL3MWAIT_SEL

Address Offset	0x0000 04B8		
Physical Address	0x4A00 24B8	**Instance**	CTRL_MODULE_CORE
Description	conf_mmcx_ocpl3mwait_view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_mmc1_ocpl3mwait 0x1: hwobs_mmc2_ocpl3mwait 0x3: hwobs_mmc4_ocpl3mwait 0x4: hwobs_mmc5_ocpl3mwait 0x2: hwobs_mmc3_ocpl3mwait	RW	0x0

Table 18-372. Register Call Summary for Register CONTROL_CONF_MMCX_OCPL3MWAIT_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Programming Guide • Hardware Observability Settings: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-373. CONTROL_CONF_MMCX_PIRFFRET_SEL

Address Offset	0x0000 04BC		
Physical Address	0x4A00 24BC	**Instance**	CTRL_MODULE_CORE
Description	conf_mmcx_pirffret_view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_mmc1_pirffret 0x1: hwobs_mmc2_pirffret 0x3: hwobs_mmc4_pirffret 0x4: hwobs_mmc5_pirffret 0x2: hwobs_mmc3_pirffret	RW	0x0

Table 18-374. Register Call Summary for Register CONTROL_CONF_MMCX_PIRFFRET_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Programming Guide • Hardware Observability Settings: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

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Table 18-375. CONTROL_CONF_MMCX_OCPL4SIDLEACKO1_SEL

Address Offset	0x0000 04C0		
Physical Address	0x4A00 24C0	**Instance**	CTRL_MODULE_CORE
Description	conf_mmcx_ocpl4sidleacko1_view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_mmc1_ocpl4sidleacko_1 0x1: hwobs_mmc2_ocpl4sidleacko_1 0x3: hwobs_mmc4_ocpl4sidleacko_1 0x4: hwobs_mmc5_ocpl4sidleacko_1 0x2: hwobs_mmc3_ocpl4sidleacko_1	RW	0x0

Table 18-376. Register Call Summary for Register CONTROL_CONF_MMCX_OCPL4SIDLEACKO1_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Programming Guide • Hardware Observability Settings: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-377. CONTROL_CONF_MMCX_OCPL4SIDLEACKO0_SEL

Address Offset	0x0000 04C4		
Physical Address	0x4A00 24C4	**Instance**	CTRL_MODULE_CORE
Description	conf_mmcx_ocpl4sidleacko0_view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_mmc1_ocpl4sidleacko_0 0x1: hwobs_mmc2_ocpl4sidleacko_0 0x3: hwobs_mmc4_ocpl4sidleacko_0 0x4: hwobs_mmc5_ocpl4sidleacko_0 0x2: hwobs_mmc3_ocpl4sidleacko_0	RW	0x0

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Table 18-378. Register Call Summary for Register CONTROL_CONF_MMCX_OCPL4SIDLEACKO0_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Programming Guide • Hardware Observability Settings: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-379. CONTROL_CONF_MMCX_OCPL3MSTANDBYO_SEL

Address Offset	0x0000 04C8		
Physical Address	0x4A00 24C8	**Instance**	CTRL_MODULE_CORE
Description	conf_mmcx_ocpl3mstandbyo_view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_mmc1_ocpl3mstandbyo 0x1: hwobs_mmc2_ocpl3mstandbyo 0x3: hwobs_mmc4_ocpl3mstandbyo 0x4: hwobs_mmc5_ocpl3mstandbyo 0x2: hwobs_mmc3_ocpl3mstandbyo	RW	0x0

Table 18-380. Register Call Summary for Register CONTROL_CONF_MMCX_OCPL3MSTANDBYO_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Programming Guide • Hardware Observability Settings: [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-381. CONTROL_CONF_MMCX_SWAKEUP_SEL

Address Offset	0x0000 04CC		
Physical Address	0x4A00 24CC	**Instance**	CTRL_MODULE_CORE
Description	conf_mmcx_swakeup_view Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MULT	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	MULT	Select one of the following signals : 0x0: hwobs_mmc1_swakeup 0x1: hwobs_mmc2_swakeup 0x3: hwobs_mmc4_swakeup 0x4: hwobs_mmc5_swakeup 0x2: hwobs_mmc3_swakeup	RW	0x0

Table 18-382. Register Call Summary for Register CONTROL_CONF_MMCX_SWAKEUP_SEL

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1]
Control Module Programming Guide • Hardware Observability Settings: [2]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [3]

Table 18-383. CONTROL_CORE_CONF_DEBUG_SEL_TST_0

Address Offset	0x0000 04D0		
Physical Address	0x4A00 24D0	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

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Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_0 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: hwobs_debug_dsp_1 0x6: hwobs_debug_ivahd_0 0x1: clk_view_0 0x1D: hwobs_bb2d_sys_interrupt_reqz 0x0: hwobs_debug_mpu_0 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: dpllctrl_plllock 0xA: Reserved 0x9: hwobs_debug_dsp_0 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: Reserved 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: hwobs_debug_dsp_2	RW	0x00

Table 18-384. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_0

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1] [2]
Control Module Programming Guide • Hardware Observability Settings: [3]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [4]

Table 18-385. CONTROL_CORE_CONF_DEBUG_SEL_TST_1

Address Offset	0x0000 04D4		
Physical Address	0x4A00 24D4	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_1 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_1 0x1: clk_view_1 0x0: hwobs_debug_mpu_1 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: dpllctrl_pllrecal 0xA: Reserved 0x9: hwobs_debug_dsp_1 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif1_pwr_sidlereq 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-386. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_1

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-387. CONTROL_CORE_CONF_DEBUG_SEL_TST_2

Address Offset	0x0000 04D8		
Physical Address	0x4A00 24D8	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_2 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_2 0x1: clk_view_2 0x0: hwobs_debug_mpu_2 0xB: hwobs_dsshdmiphypwrcmdtxon 0x3: Reserved 0x17: Reserved 0x11: dpllctrl_stopclock 0xA: Reserved 0x9: hwobs_debug_dsp_2 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif1_pwr_sidleack_1 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-388. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_2

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-389. CONTROL_CORE_CONF_DEBUG_SEL_TST_3

Address Offset	0x0000 04DC		
Physical Address	0x4A00 24DC	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_3 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_3 0x1: dpll_freqlock 0x0: hwobs_debug_mpu_3 0xB: hwobs_dsshdmiphypwrcmdoff 0x3: Reserved 0x17: Reserved 0x11: dpllctrl_stopclockackz 0xA: Reserved 0x9: hwobs_debug_dsp_3 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif1_pwr_sidleack_0 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-390. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_3

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-391. CONTROL_CORE_CONF_DEBUG_SEL_TST_4

Address Offset	0x0000 04E0		
Physical Address	0x4A00 24E0	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_4 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_4 0x1: dpll_tinitz 0x0: hwobs_debug_mpu_4 0xB: hwobs_dsshdmiphypwrack 0x3: Reserved 0x17: Reserved 0x11: dpllctrl_dispcupdatesync 0xA: Reserved 0x9: hwobs_debug_dsp_4 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif1_pwr_fclken 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-392. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_4

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-393. CONTROL_CORE_CONF_DEBUG_SEL_TST_5

Address Offset	0x0000 04E4		
Physical Address	0x4A00 24E4	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_5 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_5 0x1: dpll_phaselock 0x0: hwobs_debug_mpu_5 0xB: hwobs_dsshdmihpd 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA:Reserved 0x9: hwobs_debug_dsp_5 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif1_sys_err_intr_req 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-394. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_5

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-395. CONTROL_CORE_CONF_DEBUG_SEL_TST_6

Address Offset	0x0000 04E8		
Physical Address	0x4A00 24E8	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_6 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_6 0x1: dpll_tenable 0x0: hwobs_debug_mpu_6 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA:Reserved 0x9: hwobs_debug_dsp_6 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif1_sys_err_intr_pend 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-396. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_6

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-397. CONTROL_CORE_CONF_DEBUG_SEL_TST_7

Address Offset	0x0000 04EC		
Physical Address	0x4A00 24EC	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_7 0x5: Reserved 0x1B: Reserved 0x2: sdma_req_view_0 0x4: Reserved 0x6: hwobs_debug_ivahd_7 0x1: dpll_tenablediv 0x0: hwobs_debug_mpu_7 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA: Reserved 0x9: hwobs_debug_dsp_7 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif1_ll_err_intr_req 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-398. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_7

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-399. CONTROL_CORE_CONF_DEBUG_SEL_TST_8

Address Offset	0x0000 04F0		
Physical Address	0x4A00 24F0	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_8 0x5: Reserved 0x1B: Reserved 0x2: sdma_req_view_1 0x4: Reserved 0x6: hwobs_debug_ivahd_8 0x1: dpll_bypassack 0x0: hwobs_debug_mpu_8 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA: Reserved 0x9: hwobs_debug_dsp_8 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif1_ll_err_intr_pend 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-400. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_8

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-401. CONTROL_CORE_CONF_DEBUG_SEL_TST_9

Address Offset	0x0000 04F4		
Physical Address	0x4A00 24F4	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_9 0x5: Reserved 0x1B: Reserved 0x2: sdma_req_view_2 0x4: Reserved 0x6: hwobs_debug_ivahd_9 0x1: dpll_idle 0x0: hwobs_debug_mpu_9 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA: Reserved 0x9: hwobs_debug_dsp_9 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif1_ret_powerRet 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-402. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_9

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-403. CONTROL_CORE_CONF_DEBUG_SEL_TST_10

Address Offset	0x0000 04F8		
Physical Address	0x4A00 24F8	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_10 0x5: Reserved 0x1B: Reserved 0x2: sdma_req_view_3 0x4: Reserved 0x6: hwobs_debug_ivahd_10 0x1: Reserved 0x1D: Reserved 0x0: hwobs_debug_mpu_10 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA: Reserved 0x9: hwobs_debug_dsp_10 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: Reserved 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-404. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_10

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [1]

Table 18-405. CONTROL_CORE_CONF_DEBUG_SEL_TST_11

Address Offset	0x0000 04FC		
Physical Address	0x4A00 24FC	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_11 0x5: Reserved 0x1B: Reserved 0x2: sdma_req_view_all 0x4: Reserved 0x6: hwobs_debug_ivahd_11 0x1: hwobs_emif1_pwr_sidlereq 0x0: hwobs_debug_mpu_11 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA: Reserved 0x9: hwobs_debug_dsp_11 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: Reserved 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-406. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_11

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-407. CONTROL_CORE_CONF_DEBUG_SEL_TST_12

Address Offset	0x0000 0500		
Physical Address	0x4A00 2500	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_12 0x5: Reserved 0x1B: Reserved 0x2: hwobs_coredivider_clkout3 0x4: Reserved 0x6: hwobs_debug_ivahd_12 0x1: hwobs_emif1_pwr_sidleack_1 0x0: hwobs_debug_mpu_12 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA: Reserved 0x9: hwobs_debug_dsp_12 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: Reserved 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-408. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_12

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-409. CONTROL_CORE_CONF_DEBUG_SEL_TST_13

Address Offset	0x0000 0504		
Physical Address	0x4A00 2504	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_13 0x5: Reserved 0x1B: Reserved 0x2: hwobs_perdivider_clkout4 0x4: Reserved 0x6: hwobs_debug_ivahd_13 0x1: hwobs_emif1_pwr_sidleack_0 0x0: hwobs_debug_mpu_13 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA: Reserved 0x9: hwobs_debug_dsp_13 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif2_pwr_sidlereq 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-410. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_13

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-411. CONTROL_CORE_CONF_DEBUG_SEL_TST_14

Address Offset	0x0000 0508		
Physical Address	0x4A00 2508	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_14 0x5: Reserved 0x1B: Reserved 0x2: hwobs_pd_l4_per_per32k_gfclk 0x4: Reserved 0x6: hwobs_debug_ivahd_14 0x1: hwobs_emif1_pwr_fclken 0x0: hwobs_debug_mpu_14 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: Reserved 0xA: Reserved 0x9: hwobs_debug_dsp_14 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: Reserved 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-412. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_14

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-413. CONTROL_CORE_CONF_DEBUG_SEL_TST_15

Address Offset	0x0000 050C		
Physical Address	0x4A00 250C	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_15 0x5: Reserved 0x1B: Reserved 0x2: '0' 0x4: Reserved 0x6: hwobs_debug_ivahd_15 0x1: hwobs_emif1_sys_err_intr_req 0x0: hwobs_debug_mpu_15 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: dpll_freqlock 0xA: Reserved 0x9: hwobs_debug_dsp_15 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif2_pwr_sidleack_0 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-414. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_15

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-415. CONTROL_CORE_CONF_DEBUG_SEL_TST_16

Address Offset	0x0000 0510		
Physical Address	0x4A00 2510	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_16 0x5: Reserved 0x1B: Reserved 0x2: geni 0x4: Reserved 0x6: hwobs_debug_ivahd_16 0x1: hwobs_emif1_sys_err_intr_pend 0x0: hwobs_debug_mpu_16 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: dpll_tinitz 0xA: Reserved 0x9: hwobs_debug_dsp_16 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif2_pwr_fclken 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-416. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_16

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-417. CONTROL_CORE_CONF_DEBUG_SEL_TST_17

Address Offset	0x0000 0514		
Physical Address	0x4A00 2514	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_17 0x5: Reserved 0x1B: Reserved 0x2: geno 0x4: Reserved 0x6: hwobs_debug_ivahd_17 0x1: hwobs_emif1_ll_err_intr_req 0x0: hwobs_debug_mpu_17 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: dpll_phaselock 0xA: Reserved 0x9: hwobs_debug_dsp_17 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif2_sys_err_intr_req 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-418. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_17

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-419. CONTROL_CORE_CONF_DEBUG_SEL_TST_18

Address Offset	0x0000 0518		
Physical Address	0x4A00 2518	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_18 0x5: Reserved 0x1B: Reserved 0x2:Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_18 0x1: hwobs_emif1_ll_err_intr_pend 0x0: hwobs_debug_mpu_18 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: dpll_tenable 0xA: Reserved 0x9: hwobs_debug_dsp_18 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif2_sys_err_intr_pend 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-420. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_18

Control Module Functional Description • Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-421. CONTROL_CORE_CONF_DEBUG_SEL_TST_19

Address Offset	0x0000 051C		
Physical Address	0x4A00 251C	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_19 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_19 0x1: hwobs_emif1_ret_powerRet 0x0: hwobs_debug_mpu_19 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: dpll_tenablediv 0xA: Reserved 0x9: hwobs_debug_dsp_19 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif2_ll_err_intr_req 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-422. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_19

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-423. CONTROL_CORE_CONF_DEBUG_SEL_TST_20

Address Offset	0x0000 0520		
Physical Address	0x4A00 2520	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: Reserved 0x15: Reserved 0x8: hwobs_debug_abe_20 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_20 0x1: Reserved 0x0: hwobs_debug_mpu_20 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: dpll_bypassack 0xA: Reserved 0x9: hwobs_debug_dsp_20 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif2_ll_err_intr_pend 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-424. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_20

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-425. CONTROL_CORE_CONF_DEBUG_SEL_TST_21

Address Offset	0x0000 0524		
Physical Address	0x4A00 2524	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_sidlereq 0x15: Reserved 0x8: hwobs_debug_abe_21 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_21 0x1: Reserved 0x0: hwobs_debug_mpu_21 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: dpll_idle 0xA: Reserved 0x9: hwobs_debug_dsp_21 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: hwobs_emif2_ret_powerret 0x16: Reserved 0x1C: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-426. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_21

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-427. CONTROL_CORE_CONF_DEBUG_SEL_TST_22

Address Offset	0x0000 0528		
Physical Address	0x4A00 2528	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_fclken 0x15: Reserved 0x8: hwobs_debug_abe_22 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_22 0x1: hwobs_emif2_pwr_sidlereq 0x0: hwobs_debug_mpu_22 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: mmcx_adpidle 0xA: Reserved 0x9: hwobs_debug_dsp_22 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: Reserved 0x16: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-428. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_22

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-429. CONTROL_CORE_CONF_DEBUG_SEL_TST_23

Address Offset	0x0000 052C		
Physical Address	0x4A00 252C	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_swakeup_1 0x15: Reserved 0x8: hwobs_debug_abe_23 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4:Reserved 0x6: hwobs_debug_ivahd_23 0x1: hwobs_emif2_pwr_sidleack_1 0x0: hwobs_debug_mpu_23 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: mmcx_adpdat1paden 0xA: Reserved 0x9: hwobs_debug_dsp_23 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: Reserved 0x16: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-430. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_23

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [1]

Table 18-431. CONTROL_CORE_CONF_DEBUG_SEL_TST_24

Address Offset	0x0000 0530		
Physical Address	0x4A00 2530	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_swakeup_0 0x15: Reserved 0x8: hwobs_debug_abe_24 0x5:Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_24 0x1: hwobs_emif2_pwr_sidleack_0 0x0: hwobs_debug_mpu_24 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: mmcx_ocpl4idlereq 0xA: Reserved 0x9: hwobs_debug_dsp_24 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: '0' 0x16: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: Reserved	RW	0x00

Table 18-432. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_24

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-433. CONTROL_CORE_CONF_DEBUG_SEL_TST_25

Address Offset	0x0000 0534		
Physical Address	0x4A00 2534	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_sidleack_1 0x15: Reserved 0x8: hwobs_debug_abe_25 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: Reserved 0x6: hwobs_debug_ivahd_25 0x1: hwobs_emif2_pwr_fclken 0x0: hwobs_debug_mpu_25 0xB: Reserved 0x3: Reserved 0x17: Reserved 0x11: mmcx_ocpl3mwait 0xA:Reserved 0x9: hwobs_debug_dsp_25 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: '0' 0x16: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: '0'	RW	0x00

Table 18-434. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_25

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [1]

Table 18-435. CONTROL_CORE_CONF_DEBUG_SEL_TST_26

Address Offset	0x0000 0538		
Physical Address	0x4A00 2538	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_sidleack_0 0x15: Reserved 0x8: hwobs_debug_abe_26 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: hwobs_dmm_ocpclken 0x6: hwobs_debug_ivahd_26 0x1: hwobs_emif2_sys_err_intr_req 0x0: hwobs_debug_mpu_26 0xB: '0' 0x3: Reserved 0x17: Reserved 0x11: mmcx_pirffret 0xA: Reserved 0x9: hwobs_debug_dsp_26 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: '0' 0x16: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: '0'	RW	0x00

Table 18-436. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_26

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [1]

Table 18-437. CONTROL_CORE_CONF_DEBUG_SEL_TST_27

Address Offset	0x0000 053C		
Physical Address	0x4A00 253C	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_mwakeup 0x15: Reserved 0x8: hwobs_debug_abe_27 0x5:Reserved 0x1B: Reserved 0x2: Reserved 0x4: hwobs_dmm_rstna 0x6: hwobs_debug_ivahd_27 0x1: hwobs_emif2_sys_err_intr_pend 0x0: hwobs_debug_mpu_27 0xB: '0' 0x3: Reserved 0x17: Reserved 0x11: mmcx_ocpl4sidleacko1 0xA: Reserved 0x9: hwobs_debug_dsp_27 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: '0' 0x16: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: sdma_req_view_0	RW	0x00

Table 18-438. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_27

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [1]

Table 18-439. CONTROL_CORE_CONF_DEBUG_SEL_TST_28

Address Offset	0x0000 0540		
Physical Address	0x4A00 2540	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_mwait 0x15: Reserved 0x8: hwobs_debug_abe_28 0x5:Reserved 0x1B: Reserved 0x2: Reserved 0x4: hwobs_dmm_rstretna 0x6: hwobs_debug_ivahd_28 0x1: hwobs_emif2_ll_err_intr_req 0x0: hwobs_debug_mpu_28 0xB: '0' 0x3: Reserved 0x17: Reserved 0x11: mmcx_ocpl4sidleacko0 0xA: Reserved 0x9: hwobs_debug_dsp_28 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: '0' 0x16: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: sdma_req_view_1	RW	0x00

Table 18-440. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_28

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [1]

Table 18-441. CONTROL_CORE_CONF_DEBUG_SEL_TST_29

Address Offset	0x0000 0544		
Physical Address	0x4A00 2544	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_mstandby 0x15: Reserved 0x8: hwobs_debug_abe_29 0x5: Reserved 0x1B: Reserved 0x2: '0' 0x4: hwobs_dmm_idlereq 0x6: hwobs_debug_ivahd_29 0x1: hwobs_emif2_ll_err_intr_pend 0x0: hwobs_debug_mpu_29 0xB: '0' 0x3: Reserved 0x17: Reserved 0x11: mmcx_ocpl3mstandbyo 0xA: Reserved 0x9: hwobs_debug_dsp_29 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: '0' 0x16: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: sdma_req_view_2	RW	0x00

Table 18-442. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_29

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [1]

Table 18-443. CONTROL_CORE_CONF_DEBUG_SEL_TST_30

Address Offset	0x0000 0548		
Physical Address	0x4A00 2548	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0xD: hwobs_hsi_retff 0x15: Reserved 0x8: hwobs_debug_abe_30 0x5: Reserved 0x1B: Reserved 0x2: Reserved 0x4: hwobs_dmm_idleack_1 0x6: hwobs_debug_ivahd_30 0x1: hwobs_emif2_ret_powerret 0x0: hwobs_debug_mpu_30 0xB: '0' 0x3: Reserved 0x17: Reserved 0x11: mmcx_swakeup 0xA: Reserved 0x9: hwobs_debug_dsp_30 0x10: Reserved 0x12: Reserved 0x13: Reserved 0x18: Reserved 0x14: Reserved 0xE: '0' 0x16: Reserved 0x7: Reserved 0x19: Reserved 0x1A: Reserved 0xF: Reserved 0xC: sdma_req_view_3	RW	0x00

Table 18-444. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_30

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0]

Control Module Register Manual

- CTRL_MODULE_CORE Register Summary: [1]

Table 18-445. CONTROL_CORE_CONF_DEBUG_SEL_TST_31

Address Offset	0x0000 054C		
Physical Address	0x4A00 254C	**Instance**	CTRL_MODULE_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MODE							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	MODE	Select one of the following signals : 0x6: hwobs_debug_ivahd_31 0x1: Reserved 0xA: Reserved 0x11: '0' 0x7: Reserved 0xD: '0' 0x0: hwobs_debug_mpu_31 0x2: Reserved 0x8: hwobs_debug_abe_31 0x9: hwobs_debug_dsp_31 0x10: Reserved 0x12: Reserved 0xB: '0' 0x13: Reserved 0x4: hwobs_dmm_idleack_0 0x5: Reserved 0xF: Reserved 0xC: sdma_req_view_all 0x3: Reserved 0x14: Reserved 0xE: Reserved	RW	0x00

Table 18-446. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_31

Control Module Functional Description
- Observability Signals Multiplexing at General Core/Wake-Up Control Level: [0] [1] [2]

Control Module Programming Guide
- Hardware Observability Settings: [3]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [4]

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_debug_mpu_10 0x1: hwobs_debug_mpu_26 0x3: hwobs_debug_cm2_26 0x2: hwobs_debug_cm2_10	RW	0x0

Table 18-447. CONTROL_CORE_CONF_XBAR_SEL_0

Address Offset	0x0000 05DC		
Physical Address	0x4A00 25DC	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_3					RESERVED			CONF_XBAR_SEL_2					RESERVED			CONF_XBAR_SEL_1					RESERVED			CONF_XBAR_SEL_0				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_3	Select for xbar test_port_3	RW	0x03
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_2	Select for xbar test_port_2	RW	0x02
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_1	Select for xbar test_port_1	RW	0x01
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_0	Select for xbar test_port_0	RW	0x00

Table 18-448. Register Call Summary for Register CONTROL_CORE_CONF_XBAR_SEL_0

Control Module Functional Description
- Cross-bar: [0] [1] [2]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [3]

Table 18-449. CONTROL_CORE_CONF_XBAR_SEL_4

Address Offset	0x0000 05E0		
Physical Address	0x4A00 25E0	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_7					RESERVED			CONF_XBAR_SEL_6					RESERVED			CONF_XBAR_SEL_5					RESERVED			CONF_XBAR_SEL_4				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_7	Select for xbar test_port_7	RW	0x07
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_6	Select for xbar test_port_6	RW	0x06
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_5	Select for xbar test_port_5	RW	0x05
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_4	Select for xbar test_port_4	RW	0x04

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Table 18-450. Register Call Summary for Register CONTROL_CORE_CONF_XBAR_SEL_4

Control Module Functional Description • Cross-bar: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-451. CONTROL_CORE_CONF_XBAR_SEL_8

Address Offset	0x0000 05E4		
Physical Address	0x4A00 25E4	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_11					RESERVED			CONF_XBAR_SEL_10					RESERVED			CONF_XBAR_SEL_9					RESERVED			CONF_XBAR_SEL_8				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_11	Select for xbar test_port_11	RW	0x0B
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_10	Select for xbar test_port_10	RW	0x0A
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_9	Select for xbar test_port_9	RW	0x09
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_8	Select for xbar test_port_8	RW	0x08

Table 18-452. Register Call Summary for Register CONTROL_CORE_CONF_XBAR_SEL_8

Control Module Functional Description • Cross-bar: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-453. CONTROL_CORE_CONF_XBAR_SEL_12

Address Offset	0x0000 05E8		
Physical Address	0x4A00 25E8	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_15					RESERVED			CONF_XBAR_SEL_14					RESERVED			CONF_XBAR_SEL_13					RESERVED			CONF_XBAR_SEL_12				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_15	Select for xbar test_port_15	RW	0x0F
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_14	Select for xbar test_port_14	RW	0x0E
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_13	Select for xbar test_port_13	RW	0x0D
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_12	Select for xbar test_port_12	RW	0x0C

Table 18-454. Register Call Summary for Register CONTROL_CORE_CONF_XBAR_SEL_12

Control Module Functional Description
- Cross-bar: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-455. CONTROL_CORE_CONF_XBAR_SEL_16

Address Offset	0x0000 05EC		
Physical Address	0x4A00 25EC	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_19					RESERVED			CONF_XBAR_SEL_18					RESERVED			CONF_XBAR_SEL_17					RESERVED			CONF_XBAR_SEL_16				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_19	Select for xbar test_port_19	RW	0x13
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_18	Select for xbar test_port_18	RW	0x12
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_17	Select for xbar test_port_17	RW	0x11
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_16	Select for xbar test_port_16	RW	0x10

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Table 18-456. Register Call Summary for Register CONTROL_CORE_CONF_XBAR_SEL_16

Control Module Functional Description • Cross-bar: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-457. CONTROL_CORE_CONF_XBAR_SEL_20

Address Offset	0x0000 05F0		
Physical Address	0x4A00 25F0	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_23					RESERVED			CONF_XBAR_SEL_22					RESERVED			CONF_XBAR_SEL_21					RESERVED			CONF_XBAR_SEL_20				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_23	Select for xbar test_port_23	RW	0x17
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_22	Select for xbar test_port_22	RW	0x16
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_21	Select for xbar test_port_21	RW	0x15
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_20	Select for xbar test_port_20	RW	0x14

Table 18-458. Register Call Summary for Register CONTROL_CORE_CONF_XBAR_SEL_20

Control Module Functional Description • Cross-bar: [0]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [1]

Table 18-459. CONTROL_CORE_CONF_XBAR_SEL_24

Address Offset	0x0000 05F4		
Physical Address	0x4A00 25F4	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_27					RESERVED			CONF_XBAR_SEL_26					RESERVED			CONF_XBAR_SEL_25					RESERVED			CONF_XBAR_SEL_24				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_27	Select for xbar test_port_27	RW	0x1B
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_26	Select for xbar test_port_26	RW	0x1A
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_25	Select for xbar test_port_25	RW	0x19
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_24	Select for xbar test_port_24	RW	0x18

Table 18-460. Register Call Summary for Register CONTROL_CORE_CONF_XBAR_SEL_24

Control Module Functional Description
- Cross-bar: [0]

Control Module Register Manual
- CTRL_MODULE_CORE Register Summary: [1]

Table 18-461. CONTROL_CORE_CONF_XBAR_SEL_28

Address Offset	0x0000 05F8		
Physical Address	0x4A00 25F8	**Instance**	CTRL_MODULE_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_31					RESERVED			CONF_XBAR_SEL_30					RESERVED			CONF_XBAR_SEL_29					RESERVED			CONF_XBAR_SEL_28				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_31	Select for xbar test_port_31	RW	0x1F
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_30	Select for xbar test_port_30	RW	0x1E
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_29	Select for xbar test_port_29	RW	0x1D
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_28	Select for xbar test_port_28	RW	0x1C

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Table 18-462. Register Call Summary for Register CONTROL_CORE_CONF_XBAR_SEL_28

Control Module Functional Description • Cross-bar: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

Table 18-463. CONTROL_CORE_CONF_XBAR_BYPASS

Address Offset	0x0000 05FC		
Physical Address	0x4A00 25FC	**Instance**	CTRL_MODULE_CORE
Description	Crossbar bypass control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SELECT

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	SELECT	Crossbar enable/disable 0x0: Crossbar is enabled 0x1: Crossbar is disabled (baypassed)	RW	1

Table 18-464. Register Call Summary for Register CONTROL_CORE_CONF_XBAR_BYPASS

Control Module Functional Description • Cross-bar: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE Register Summary: [2]

18.6.3 CTRL_MODULE_CORE_PAD Registers

18.6.3.1 CTRL_MODULE_CORE_PAD Register Summary

Table 18-465. CTRL_MODULE_CORE_PAD Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE _PAD Base Address
CONTROL_CORE_PAD _REVISION	R	32	0x0000 0000	0x4A00 2800
CONTROL_CORE_PAD _HWINFO	R	32	0x0000 0004	0x4A00 2804
CONTROL_CORE_PAD _SYSCONFIG	RW	32	0x0000 0010	0x4A00 2810
CONTROL_CORE_PAD 0_EMMC_CLK_PAD1_E MMC_CMD	RW	32	0x0000 0040	0x4A00 2840
CONTROL_CORE_PAD 0_EMMC_DATA0_PAD 1_EMMC_DATA1	RW	32	0x0000 0044	0x4A00 2844
CONTROL_CORE_PAD 0_EMMC_DATA2_PAD 1_EMMC_DATA3	RW	32	0x0000 0048	0x4A00 2848

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Table 18-465. CTRL_MODULE_CORE_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE_PAD Base Address
CONTROL_CORE_PAD0_EMMC_DATA4_PAD1_EMMC_DATA5	RW	32	0x0000 004C	0x4A00 284C
CONTROL_CORE_PAD0_EMMC_DATA6_PAD1_EMMC_DATA7	RW	32	0x0000 0050	0x4A00 2850
CONTROL_CORE_PAD0_C2C_CLKOUT0_PAD1_C2C_CLKOUT1	RW	32	0x0000 0054	0x4A00 2854
CONTROL_CORE_PAD0_C2C_CLKIN0_PAD1_C2C_CLKIN1	RW	32	0x0000 0058	0x4A00 2858
CONTROL_CORE_PAD0_C2C_DATAIN0_PAD1_C2C_DATAIN1	RW	32	0x0000 005C	0x4A00 285C
CONTROL_CORE_PAD0_C2C_DATAIN2_PAD1_C2C_DATAIN3	RW	32	0x0000 0060	0x4A00 2860
CONTROL_CORE_PAD0_C2C_DATAIN4_PAD1_C2C_DATAIN5	RW	32	0x0000 0064	0x4A00 2864
CONTROL_CORE_PAD0_C2C_DATAIN6_PAD1_C2C_DATAIN7	RW	32	0x0000 0068	0x4A00 2868
CONTROL_CORE_PAD0_C2C_DATAOUT0_PAD1_C2C_DATAOUT1	RW	32	0x0000 006C	0x4A00 286C
CONTROL_CORE_PAD0_C2C_DATAOUT2_PAD1_C2C_DATAOUT3	RW	32	0x0000 0070	0x4A00 2870
CONTROL_CORE_PAD0_C2C_DATAOUT4_PAD1_C2C_DATAOUT5	RW	32	0x0000 0074	0x4A00 2874
CONTROL_CORE_PAD0_C2C_DATAOUT6_PAD1_C2C_DATAOUT7	RW	32	0x0000 0078	0x4A00 2878
CONTROL_CORE_PAD0_C2C_DATA8_PAD1_C2C_DATA9	RW	32	0x0000 007C	0x4A00 287C
CONTROL_CORE_PAD0_C2C_DATA10_PAD1_C2C_DATA11	RW	32	0x0000 0080	0x4A00 2880
CONTROL_CORE_PAD0_C2C_DATA12_PAD1_C2C_DATA13	RW	32	0x0000 0084	0x4A00 2884
CONTROL_CORE_PAD0_C2C_DATA14_PAD1_C2C_DATA15	RW	32	0x0000 0088	0x4A00 2888
CONTROL_CORE_PAD0_LLIA_WAKEREQOUT_PAD1_LLIB_WAKEREQOUT	RW	32	0x0000 008C	0x4A00 288C
CONTROL_CORE_PAD0_HSI1_ACREADY_PAD1_HSI1_CAREADY	RW	32	0x0000 0090	0x4A00 2890
CONTROL_CORE_PAD0_HSI1_ACWAKE_PAD1_HSI1_CAWAKE	RW	32	0x0000 0094	0x4A00 2894

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Table 18-465. CTRL_MODULE_CORE_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE_PAD Base Address
CONTROL_CORE_PAD0_HSI1_ACFLAG_PAD1_HSI1_ACDATA	RW	32	0x0000 0098	0x4A00 2898
CONTROL_CORE_PAD0_HSI1_CAFLAG_PAD1_HSI1_CADATA	RW	32	0x0000 009C	0x4A00 289C
CONTROL_CORE_PAD0_UART1_TX_PAD1_UART1_CTS	RW	32	0x0000 00A0	0x4A00 28A0
CONTROL_CORE_PAD0_UART1_RX_PAD1_UART1_RTS	RW	32	0x0000 00A4	0x4A00 28A4
CONTROL_CORE_PAD0_HSI2_CAREADY_PAD1_HSI2_ACREADY	RW	32	0x0000 00A8	0x4A00 28A8
CONTROL_CORE_PAD0_HSI2_CAWAKE_PAD1_HSI2_ACWAKE	RW	32	0x0000 00AC	0x4A00 28AC
CONTROL_CORE_PAD0_HSI2_CAFLAG_PAD1_HSI2_CADATA	RW	32	0x0000 00B0	0x4A00 28B0
CONTROL_CORE_PAD0_HSI2_ACFLAG_PAD1_HSI2_ACDATA	RW	32	0x0000 00B4	0x4A00 28B4
CONTROL_CORE_PAD0_UART2_RTS_PAD1_UART2_CTS	RW	32	0x0000 00B8	0x4A00 28B8
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX	RW	32	0x0000 00BC	0x4A00 28BC
CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBB1_HSIC_DATA	RW	32	0x0000 00C0	0x4A00 28C0
CONTROL_CORE_PAD0_USBB2_HSIC_STROBE_PAD1_USBB2_HSIC_DATA	RW	32	0x0000 00C4	0x4A00 28C4
CONTROL_CORE_PAD0_TIMER10_PWM_EVT_PAD1_DSIPORTA_TE0	RW	32	0x0000 00C8	0x4A00 28C8
CONTROL_CORE_PAD0_DSIPORTA_LANE0X_PAD1_DSIPORTA_LANE0Y	RW	32	0x0000 00CC	0x4A00 28CC
CONTROL_CORE_PAD0_DSIPORTA_LANE1X_PAD1_DSIPORTA_LANE1Y	RW	32	0x0000 00D0	0x4A00 28D0
CONTROL_CORE_PAD0_DSIPORTA_LANE2X_PAD1_DSIPORTA_LANE2Y	RW	32	0x0000 00D4	0x4A00 28D4
CONTROL_CORE_PAD0_DSIPORTA_LANE3X_PAD1_DSIPORTA_LANE3Y	RW	32	0x0000 00D8	0x4A00 28D8

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Table 18-465. CTRL_MODULE_CORE_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE_PAD Base Address
CONTROL_CORE_PAD0_DSIPORTA_LANE4X_PAD1_DSIPORTA_LANE4Y	RW	32	0x0000 00DC	0x4A00 28DC
CONTROL_CORE_PAD0_DSIPORTC_LANE0X_PAD1_DSIPORTC_LANE0Y	RW	32	0x0000 00E0	0x4A00 28E0
CONTROL_CORE_PAD0_DSIPORTC_LANE1X_PAD1_DSIPORTC_LANE1Y	RW	32	0x0000 00E4	0x4A00 28E4
CONTROL_CORE_PAD0_DSIPORTC_LANE2X_PAD1_DSIPORTC_LANE2Y	RW	32	0x0000 00E8	0x4A00 28E8
CONTROL_CORE_PAD0_DSIPORTC_LANE3X_PAD1_DSIPORTC_LANE3Y	RW	32	0x0000 00EC	0x4A00 28EC
CONTROL_CORE_PAD0_DSIPORTC_LANE4X_PAD1_DSIPORTC_LANE4Y	RW	32	0x0000 00F0	0x4A00 28F0
CONTROL_CORE_PAD0_DSIPORTC_TE0_PAD1_TIMER9_PWM_EVT	RW	32	0x0000 00F4	0x4A00 28F4
CONTROL_CORE_PAD0_I2C4_SCL_PAD1_I2C4_SDA	RW	32	0x0000 00F8	0x4A00 28F8
CONTROL_CORE_PAD0_MCSPI2_CLK_PAD1_MCSPI2_SIMO	RW	32	0x0000 00FC	0x4A00 28FC
CONTROL_CORE_PAD0_MCSPI2_SOMI_PAD1_MCSPI2_CS0	RW	32	0x0000 0100	0x4A00 2900
CONTROL_CORE_PAD0_RFBI_DATA15_PAD1_RFBI_DATA14	RW	32	0x0000 0104	0x4A00 2904
CONTROL_CORE_PAD0_RFBI_DATA13_PAD1_RFBI_DATA12	RW	32	0x0000 0108	0x4A00 2908
CONTROL_CORE_PAD0_RFBI_DATA11_PAD1_RFBI_DATA10	RW	32	0x0000 010C	0x4A00 290C
CONTROL_CORE_PAD0_RFBI_DATA9_PAD1_RFBI_DATA8	RW	32	0x0000 0110	0x4A00 2910
CONTROL_CORE_PAD0_RFBI_DATA7_PAD1_RFBI_DATA6	RW	32	0x0000 0114	0x4A00 2914
CONTROL_CORE_PAD0_RFBI_DATA5_PAD1_RFBI_DATA4	RW	32	0x0000 0118	0x4A00 2918
CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2	RW	32	0x0000 011C	0x4A00 291C
CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0	RW	32	0x0000 0120	0x4A00 2920

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Table 18-465. CTRL_MODULE_CORE_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE_PAD Base Address
CONTROL_CORE_PAD0_RFBI_WE_PAD1_RFBI_CS0	RW	32	0x0000 0124	0x4A00 2924
CONTROL_CORE_PAD0_RFBI_A0_PAD1_RFBI_RE	RW	32	0x0000 0128	0x4A00 2928
CONTROL_CORE_PAD0_RFBI_HSYNC0_PAD1_RFBI_TE_VSYNC0	RW	32	0x0000 012C	0x4A00 292C
CONTROL_CORE_PAD0_GPIO6_182_PAD1_GPIO6_183	RW	32	0x0000 0130	0x4A00 2930
CONTROL_CORE_PAD0_GPIO6_184_PAD1_GPIO6_185	RW	32	0x0000 0134	0x4A00 2934
CONTROL_CORE_PAD0_GPIO6_186_PAD1_GPIO6_187	RW	32	0x0000 0138	0x4A00 2938
CONTROL_CORE_PAD0_HDMI_CEC_PAD1_HDMI_HPD	RW	32	0x0000 013C	0x4A00 293C
CONTROL_CORE_PAD0_HDMI_DDC_SCL_PAD1_HDMI_DDC_SDA	RW	32	0x0000 0140	0x4A00 2940
CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y	RW	32	0x0000 0144	0x4A00 2944
CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y	RW	32	0x0000 0148	0x4A00 2948
CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y	RW	32	0x0000 014C	0x4A00 294C
CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y	RW	32	0x0000 0150	0x4A00 2950
CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y	RW	32	0x0000 0154	0x4A00 2954
CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y	RW	32	0x0000 0158	0x4A00 2958
CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y	RW	32	0x0000 015C	0x4A00 295C
CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y	RW	32	0x0000 0160	0x4A00 2960
CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y	RW	32	0x0000 0164	0x4A00 2964

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Table 18-465. CTRL_MODULE_CORE_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE_PAD Base Address
CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y	RW	32	0x0000 0168	0x4A00 2968
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE	RW	32	0x0000 016C	0x4A00 296C
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_TIMER11_PWM_EVT	RW	32	0x0000 0170	0x4A00 2970
CONTROL_CORE_PAD0_TIMER5_PWM_EVT_PAD1_TIMER6_PWM_EVT	RW	32	0x0000 0174	0x4A00 2974
CONTROL_CORE_PAD0_TIMER8_PWM_EVT_PAD1_I2C3_SCL	RW	32	0x0000 0178	0x4A00 2978
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_GPIO8_233	RW	32	0x0000 017C	0x4A00 297C
CONTROL_CORE_PAD0_GPIO8_234_PAD1_ABE_CLKS	RW	32	0x0000 0180	0x4A00 2980
CONTROL_CORE_PAD0_ABEDMIC_DIN1_PAD1_ABEDMIC_DIN2	RW	32	0x0000 0184	0x4A00 2984
CONTROL_CORE_PAD0_ABEDMIC_DIN3_PAD1_ABEDMIC_CLK1	RW	32	0x0000 0188	0x4A00 2988
CONTROL_CORE_PAD0_ABEDMIC_CLK2_PAD1_ABEDMIC_CLK3	RW	32	0x0000 018C	0x4A00 298C
CONTROL_CORE_PAD0_ABESLIMBUS1_CLOCK_PAD1_ABESLIMBUS1_DATA	RW	32	0x0000 0190	0x4A00 2990
CONTROL_CORE_PAD0_ABEMCBSP2_DR_PAD1_ABEMCBSP2_DX	RW	32	0x0000 0194	0x4A00 2994
CONTROL_CORE_PAD0_ABEMCBSP2_FSX_PAD1_ABEMCBSP2_CLKX	RW	32	0x0000 0198	0x4A00 2998
CONTROL_CORE_PAD0_ABEMCPDM_UL_DATA_PAD1_ABEMCPDM_DL_DATA	RW	32	0x0000 019C	0x4A00 299C
CONTROL_CORE_PAD0_ABEMCPDM_FRAME_PAD1_ABEMCPDM_LB_CLK	RW	32	0x0000 01A0	0x4A00 29A0
CONTROL_CORE_PAD0_WLSDIO_CLK_PAD1_WLSDIO_CMD	RW	32	0x0000 01A4	0x4A00 29A4
CONTROL_CORE_PAD0_WLSDIO_DATA0_PAD1_WLSDIO_DATA1	RW	32	0x0000 01A8	0x4A00 29A8

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Table 18-465. CTRL_MODULE_CORE_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE_PAD Base Address
CONTROL_CORE_PAD0_WLSDIO_DATA2_PAD1_WLSDIO_DATA3	RW	32	0x0000 01AC	0x4A00 29AC
CONTROL_CORE_PAD0_UART5_RX_PAD1_UART5_TX	RW	32	0x0000 01B0	0x4A00 29B0
CONTROL_CORE_PAD0_UART5_CTS_PAD1_UART5_RTS	RW	32	0x0000 01B4	0x4A00 29B4
CONTROL_CORE_PAD0_I2C2_SCL_PAD1_I2C2_SDA	RW	32	0x0000 01B8	0x4A00 29B8
CONTROL_CORE_PAD0_MCSPI1_CLK_PAD1_MCSPI1_SOMI	RW	32	0x0000 01BC	0x4A00 29BC
CONTROL_CORE_PAD0_MCSPI1_SIMO_PAD1_MCSPI1_CS0	RW	32	0x0000 01C0	0x4A00 29C0
CONTROL_CORE_PAD0_MCSPI1_CS1_PAD1_I2C5_SCL	RW	32	0x0000 01C4	0x4A00 29C4
CONTROL_CORE_PAD0_I2C5_SDA_PAD1_GPIO5_145	RW	32	0x0000 01C8	0x4A00 29C8
CONTROL_CORE_PAD0_GPIO5_146_PAD1_UART6_TX	RW	32	0x0000 01CC	0x4A00 29CC
CONTROL_CORE_PAD0_UART6_RX_PAD1_UART6_CTS	RW	32	0x0000 01D0	0x4A00 29D0
CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX	RW	32	0x0000 01D4	0x4A00 29D4
CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX	RW	32	0x0000 01D8	0x4A00 29D8
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE	RW	32	0x0000 01DC	0x4A00 29DC
CONTROL_CORE_PAD0_USBB3_HSIC_DATA_PAD1_SDCARD_CLK	RW	32	0x0000 01E0	0x4A00 29E0
CONTROL_CORE_PAD0_SDCARD_CMD_PAD1_SDCARD_DATA2	RW	32	0x0000 01E4	0x4A00 29E4
CONTROL_CORE_PAD0_SDCARD_DATA3_PAD1_SDCARD_DATA0	RW	32	0x0000 01E8	0x4A00 29E8
CONTROL_CORE_PAD0_SDCARD_DATA1_PAD1_USBD0_HS_DP	RW	32	0x0000 01EC	0x4A00 29EC
CONTROL_CORE_PAD0_USBD0_HS_DM_PAD1_I2C1_PMIC_SCL	RW	32	0x0000 01F0	0x4A00 29F0
CONTROL_CORE_PAD0_I2C1_PMIC_SDA_PAD1_USBD0_SS_RX	RW	32	0x0000 01F4	0x4A00 29F4

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Table 18-465. CTRL_MODULE_CORE_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE_PAD Base Address
CONTROL_PADCONF_WAKEUPEVENT_0	R	32	0x0000 01FC	0x4A00 29FC
CONTROL_PADCONF_WAKEUPEVENT_1	R	32	0x0000 0200	0x4A00 2A00
CONTROL_PADCONF_WAKEUPEVENT_2	R	32	0x0000 0204	0x4A00 2A04
CONTROL_PADCONF_WAKEUPEVENT_3	R	32	0x0000 0208	0x4A00 2A08
CONTROL_PADCONF_WAKEUPEVENT_4	R	32	0x0000 020C	0x4A00 2A0C
CONTROL_PADCONF_WAKEUPEVENT_5	R	32	0x0000 0210	0x4A00 2A10
CONTROL_PADCONF_WAKEUPEVENT_6	R	32	0x0000 0214	0x4A00 2A14
RESERVED	R	32	0x0000 05A0	0x4A00 2DA0
CONTROL_PADCONF_MODE	RW	32	0x0000 05A4	0x4A00 2DA4
CONTROL_SMART1IO_PADCONF_0	RW	32	0x0000 05A8	0x4A00 2DA8
CONTROL_SMART1IO_PADCONF_1	RW	32	0x0000 05AC	0x4A00 2DAC
CONTROL_SMART1IO_PADCONF_2	RW	32	0x0000 05B0	0x4A00 2DB0
CONTROL_SMART2IO_PADCONF_0	RW	32	0x0000 05B4	0x4A00 2DB4
CONTROL_SMART2IO_PADCONF_1	RW	32	0x0000 05B8	0x4A00 2DB8
CONTROL_SMART2IO_PADCONF_2	RW	32	0x0000 05BC	0x4A00 2DBC
CONTROL_SMART3IO_PADCONF_0	RW	32	0x0000 05C0	0x4A00 2DC0
CONTROL_SMART3IO_PADCONF_1	RW	32	0x0000 05C4	0x4A00 2DC4
CONTROL_PBIAS	RW	32	0x0000 0600	0x4A00 2E00
CONTROL_I2C_0	RW	32	0x0000 0604	0x4A00 2E04
CONTROL_CAMERA_RX	RW	32	0x0000 0608	0x4A00 2E08
CONTROL_HDMI_TX_PHY	RW	32	0x0000 060C	0x4A00 2E0C
RESERVED	R	32	0x0000 0610	0x4A00 2E10
CONTROL_DSIPHY	RW	32	0x0000 0614	0x4A00 2E14
CONTROL_MCBSPLP	RW	32	0x0000 0618	0x4A00 2E18
CONTROL_USB2PHYCORE	RW	32	0x0000 061C	0x4A00 2E1C
CONTROL_HDMI_1	RW	32	0x0000 0620	0x4A00 2E20
RESERVED	R	32	0x0000 0624	0x4A00 2E24
CONTROL_DDR3CH1_0	RW	32	0x0000 0630	0x4A00 2E30
CONTROL_DDR3CH2_0	RW	32	0x0000 0634	0x4A00 2E34
CONTROL_DDRCH1_0	RW	32	0x0000 0638	0x4A00 2E38
CONTROL_DDRCH1_1	RW	32	0x0000 063C	0x4A00 2E3C
CONTROL_DDRCH2_0	RW	32	0x0000 0640	0x4A00 2E40

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Table 18-465. CTRL_MODULE_CORE_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_CORE_PAD Base Address
CONTROL_DDRCH2_1	RW	32	0x0000 0644	0x4A00 2E44
CONTROL_LPDDR2CH1_0	RW	32	0x0000 0648	0x4A00 2E48
CONTROL_LPDDR2CH1_1	RW	32	0x0000 064C	0x4A00 2E4C
CONTROL_DDRIO_0	RW	32	0x0000 0650	0x4A00 2E50
CONTROL_DDRIO_1	RW	32	0x0000 0654	0x4A00 2E54
CONTROL_DDRIO_2	RW	32	0x0000 0658	0x4A00 2E58
CONTROL_HYST_1	RW	32	0x0000 065C	0x4A00 2E5C
RESERVED	R	32	0x0000 0660	0x4A00 2E60
RESERVED	R	32	0x0000 0664	0x4A00 2E64
CONTROL_CORE_CONTROL_SPARE_RW	RW	32	0x0000 0668	0x4A00 2E68
CONTROL_CORE_CONTROL_SPARE_R	R	32	0x0000 066C	0x4A00 2E6C
CONTROL_CORE_CONTROL_SPARE_R_C0	RW	32	0x0000 0670	0x4A00 2E70
RESERVED	R	32	0x0000 0674	0x4A00 2E74
RESERVED	R	32	0x0000 0678	0x4A00 2E78
RESERVED	R	32	0x0000 067C	0x4A00 2E7C
RESERVED	R	32	0x0000 0680	0x4A00 2E80
RESERVED	R	32	0x0000 0684	0x4A00 2E84
CONTROL_DDRIO_EXT_0	RW	32	0x0000 0688	0x4A00 2E88

18.6.3.2 CTRL_MODULE_CORE_PAD Register Description

Table 18-466. CONTROL_CORE_PAD_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A00 2800 0x4A00 2800	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Control module revision identifier Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISON																															

Bits	Field Name	Description	Type	Reset
31:0	REVISON	IP Revision	R	TI Internal data

Table 18-467. Register Call Summary for Register CONTROL_CORE_PAD_REVISION

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [0]

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Table 18-468. CONTROL_CORE_PAD_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A00 2804 0x4A00 2804	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Information about the IP module hardware configuration i.e. typically the module HDL generics (if any). Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	IP_HWINFO	IP-module dependent	R	0x0000 0000

Table 18-469. Register Call Summary for Register CONTROL_CORE_PAD_HWINFO

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [0]

Table 18-470. CONTROL_CORE_PAD_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A00 2810 0x4A00 2810	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IP_SYSCONFIG_IDLEMODE		RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:2	IP_SYSCONFIG_IDLEMODE	RESERVED (not used).	RW	0x2
1:0	RESERVED		R	0x0

Table 18-471. Register Call Summary for Register CONTROL_CORE_PAD_SYSCONFIG

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [0]

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Table 18-472. CONTROL_CORE_PAD0_EMMC_CLK_PAD1_EMMC_CMD

Address Offset	0x0000 0040		
Physical Address	0x4A00 2840 0x4A00 2840	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads emmc_clk and emmc_cmd Access conditions. Read: unrestricted, Write: unrestricted)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMMC_CMD_WAKEUPEVENT	EMMC_CMD_WAKEUPENABLE	RESERVED					EMMC_CMD_INPUTENABLE	RESERVED		EMMC_CMD_PWRDOWN	EMMC_CMD_PULLTYPESELECT	EMMC_CMD_PULLUDENABLE	EMMC_CMD_MUXMODE			EMMC_CLK_WAKEUPEVENT	EMMC_CLK_WAKEUPENABLE	RESERVED					EMMC_CLK_INPUTENABLE	RESERVED	EMMC_CLK_GLITCHGOBBLER	EMMC_CLK_PWRDOWN	EMMC_CLK_PULLTYPESELECT	EMMC_CLK_PULLUDENABLE	EMMC_CLK_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	EMMC_CMD_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	EMMC_CMD_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	EMMC_CMD_INPUTENABLE	Input enable value for pad emmc_cmd 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	EMMC_CMD_PWRDOWN	Power Down setting for pad emmc_cmd 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	EMMC_CMD_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_cmd 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	EMMC_CMD_PULLUDENABLE	Pull-Up/Down enable for pad emmc_cmd 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	EMMC_CMD_MUXMODE	Functional multiplexing selection for pad emmc_cmd 0x0: Select emmc_cmd 0x7: Select safe_mode_core1 0x6: Select gpio2_47	RW	0x0
15	EMMC_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	EMMC_CLK_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	EMMC_CLK_INPUTENABLE	Input enable value for pad emmc_clk 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7	RESERVED		R	0
6	EMMC_CLK_GLITCHGOBBLER	Glitch Gobbler setting for pad emmc_clk 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
5	EMMC_CLK_PWRDOWN	Power Down setting for pad emmc_clk 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	EMMC_CLK_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_clk 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	EMMC_CLK_PULLUDENABLE	Pull-Up/Down enable for pad emmc_clk 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	EMMC_CLK_MUXMODE	Functional multiplexing selection for pad emmc_clk 0x0: Select emmc_clk 0x7: Select safe_mode_core0 0x6: Select gpio2_46	RW	0x0

Table 18-473. Register Call Summary for Register CONTROL_CORE_PAD0_EMMC_CLK_PAD1_EMMC_CMD

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-474. CONTROL_CORE_PAD0_EMMC_DATA0_PAD1_EMMC_DATA1

Address Offset	0x0000 0044		
Physical Address	0x4A00 2844 0x4A00 2844	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads emmc_data0 and emmc_data1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMMC_DATA1_WAKEUPEVENT	EMMC_DATA1_WAKEUPENABLE	RESERVED					EMMC_DATA1_INPUTENABLE	RESERVED		EMMC_DATA1_PWRDOWN	EMMC_DATA1_PULLTYPESELECT	EMMC_DATA1_PULLUDENABLE	EMMC_DATA1_MUXMODE			EMMC_DATA0_WAKEUPEVENT	EMMC_DATA0_WAKEUPENABLE	RESERVED					EMMC_DATA0_INPUTENABLE	RESERVED		EMMC_DATA0_PWRDOWN	EMMC_DATA0_PULLTYPESELECT	EMMC_DATA0_PULLUDENABLE	EMMC_DATA0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	EMMC_DATA1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	EMMC_DATA1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	EMMC_DATA1_INPUTENABLE	Input enable value for pad emmc_data1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	EMMC_DATA1_PWRDOWN	Power Down setting for pad emmc_data1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	EMMC_DATA1_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_data1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	EMMC_DATA1_PULLUDENABLE	Pull-Up/Down enable for pad emmc_data1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	EMMC_DATA1_MUXMODE	Functional multiplexing selection for pad emmc_data1 0x0: Select emmc_data1 0x7: Select safe_mode_core3 0x6: Select gpio2_49	RW	0x0
15	EMMC_DATA0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	EMMC_DATA0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	EMMC_DATA0_INPUTENABLE	Input enable value for pad emmc_data0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	EMMC_DATA0_PWRDOWN	Power Down setting for pad emmc_data0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	EMMC_DATA0_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_data0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	EMMC_DATA0_PULLUDENABLE	Pull-Up/Down enable for pad emmc_data0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	EMMC_DATA0_MUXMODE	Functional multiplexing selection for pad emmc_data0 0x0: Select emmc_data0 0x7: Select safe_mode_core2 0x6: Select gpio2_48	RW	0x0

Table 18-475. Register Call Summary for Register CONTROL_CORE_PAD0_EMMC_DATA0_PAD1_EMMC_DATA1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-476. CONTROL_CORE_PAD0_EMMC_DATA2_PAD1_EMMC_DATA3

Address Offset	0x0000 0048		
Physical Address	0x4A00 2848 0x4A00 2848	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads emmc_data2 and emmc_data3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMMC_DATA3_WAKEUPEVENT	EMMC_DATA3_WAKEUPENABLE	RESERVED					EMMC_DATA3_INPUTENABLE	RESERVED		EMMC_DATA3_PWRDOWN	EMMC_DATA3_PULLTYPESELECT	EMMC_DATA3_PULLUDENABLE	EMMC_DATA3_MUXMODE			EMMC_DATA2_WAKEUPEVENT	EMMC_DATA2_WAKEUPENABLE	RESERVED					EMMC_DATA2_INPUTENABLE	RESERVED		EMMC_DATA2_PWRDOWN	EMMC_DATA2_PULLTYPESELECT	EMMC_DATA2_PULLUDENABLE	EMMC_DATA2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	EMMC_DATA3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	EMMC_DATA3_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
24	EMMC_DATA3_INPUTENABLE	Input enable value for pad emmc_data3 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	EMMC_DATA3_PWRDOWN	Power Down setting for pad emmc_data3 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	EMMC_DATA3_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_data3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	EMMC_DATA3_PULLUDENABLE	Pull-Up/Down enable for pad emmc_data3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	EMMC_DATA3_MUXMODE	Functional multiplexing selection for pad emmc_data3 0x0: Select emmc_data3 0x7: Select safe_mode_core5 0x6: Select gpio2_51	RW	0x0
15	EMMC_DATA2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	EMMC_DATA2_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	EMMC_DATA2_INPUTENABLE	Input enable value for pad emmc_data2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	EMMC_DATA2_PWRDOWN	Power Down setting for pad emmc_data2 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	EMMC_DATA2_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_data2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	EMMC_DATA2_PULLUDENABLE	Pull-Up/Down enable for pad emmc_data2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	EMMC_DATA2_MUXMODE	Functional multiplexing selection for pad emmc_data2 0x0: Select emmc_data2 0x7: Select safe_mode_core4 0x6: Select gpio2_50	RW	0x0

Table 18-477. Register Call Summary for Register CONTROL_CORE_PAD0_EMMC_DATA2_PAD1_EMMC_DATA3

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-478. CONTROL_CORE_PAD0_EMMC_DATA4_PAD1_EMMC_DATA5

Address Offset	0x0000 004C		
Physical Address	0x4A00 284C 0x4A00 284C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads emmc_data4 and emmc_data5 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMMC_DATA5_WAKEUPEVENT	EMMC_DATA5_WAKEUPENABLE	RESERVED					EMMC_DATA5_INPUTENABLE	RESERVED		EMMC_DATA5_PWRDOWN	EMMC_DATA5_PULLTYPESELECT	EMMC_DATA5_PULLUDENABLE	EMMC_DATA5_MUXMODE			EMMC_DATA4_WAKEUPEVENT	EMMC_DATA4_WAKEUPENABLE	RESERVED					EMMC_DATA4_INPUTENABLE	RESERVED		EMMC_DATA4_PWRDOWN	EMMC_DATA4_PULLTYPESELECT	EMMC_DATA4_PULLUDENABLE	EMMC_DATA4_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	EMMC_DATA5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	EMMC_DATA5_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	EMMC_DATA5_INPUTENABLE	Input enable value for pad emmc_data5 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	EMMC_DATA5_PWRDOWN	Power Down setting for pad emmc_data5 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	EMMC_DATA5_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_data5 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	EMMC_DATA5_PULLUDENABLE	Pull-Up/Down enable for pad emmc_data5 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	EMMC_DATA5_MUXMODE	Functional multiplexing selection for pad emmc_data5 0x0: Select emmc_data5 0x7: Select safe_mode_core7 0x6: Select gpio2_53	RW	0x0
15	EMMC_DATA4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	EMMC_DATA4_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	EMMC_DATA4_INPUTENABLE	Input enable value for pad emmc_data4 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	EMMC_DATA4_PWRDOWN	Power Down setting for pad emmc_data4 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	EMMC_DATA4_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_data4 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	EMMC_DATA4_PULLUDENABLE	Pull-Up/Down enable for pad emmc_data4 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	EMMC_DATA4_MUXMODE	Functional multiplexing selection for pad emmc_data4 0x0: Select emmc_data4 0x7: Select safe_mode_core6 0x6: Select gpio2_52	RW	0x0

Table 18-479. Register Call Summary for Register CONTROL_CORE_PAD0_EMMC_DATA4_PAD1_EMMC_DATA5

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-480. CONTROL_CORE_PAD0_EMMC_DATA6_PAD1_EMMC_DATA7

Address Offset	0x0000 0050		
Physical Address	0x4A00 2850 0x4A00 2850	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads emmc_data6 and emmc_data7 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMMC_DATA7_WAKEUPEVENT	EMMC_DATA7_WAKEUPENABLE	RESERVED					EMMC_DATA7_INPUTENABLE	RESERVED		EMMC_DATA7_PWRDOWN	EMMC_DATA7_PULLTYPESELECT	EMMC_DATA7_PULLUDENABLE	EMMC_DATA7_MUXMODE			EMMC_DATA6_WAKEUPEVENT	EMMC_DATA6_WAKEUPENABLE	RESERVED					EMMC_DATA6_INPUTENABLE	RESERVED		EMMC_DATA6_PWRDOWN	EMMC_DATA6_PULLTYPESELECT	EMMC_DATA6_PULLUDENABLE	EMMC_DATA6_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	EMMC_DATA7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	EMMC_DATA7_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	EMMC_DATA7_INPUTENABLE	Input enable value for pad emmc_data7 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	EMMC_DATA7_PWRDOWN	Power Down setting for pad emmc_data7 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	EMMC_DATA7_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_data7 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	EMMC_DATA7_PULLUDENABLE	Pull-Up/Down enable for pad emmc_data7 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	EMMC_DATA7_MUXMODE	Functional multiplexing selection for pad emmc_data7 0x0: Select emmc_data7 0x7: Select safe_mode_core9 0x6: Select gpio2_55	RW	0x0
15	EMMC_DATA6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	EMMC_DATA6_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	EMMC_DATA6_INPUTENABLE	Input enable value for pad emmc_data6 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	EMMC_DATA6_PWRDOWN	Power Down setting for pad emmc_data6 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	EMMC_DATA6_PULLTYPESELECT	Pull-Up/Down selection for pad emmc_data6 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	EMMC_DATA6_PULLUDENABLE	Pull-Up/Down enable for pad emmc_data6 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	EMMC_DATA6_MUXMODE	Functional multiplexing selection for pad emmc_data6 0x0: Select emmc_data6 0x7: Select safe_mode_core8 0x6: Select gpio2_54	RW	0x0

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Table 18-481. Register Call Summary for Register CONTROL_CORE_PAD0_EMMC_DATA6_PAD1_EMMC_DATA7

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-482. CONTROL_CORE_PAD0_C2C_CLKOUT0_PAD1_C2C_CLKOUT1

Address Offset	0x0000 0054		
Physical Address	0x4A00 2854 0x4A00 2854	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_clkout0 and c2c_clkout1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_CLKOUT1_WAKEUPEVENT	C2C_CLKOUT1_WAKEUPENABLE	RESERVED					C2C_CLKOUT1_INPUTENABLE	RESERVED		C2C_CLKOUT1_PWRDOWN	C2C_CLKOUT1_PULLTYPESELECT	C2C_CLKOUT1_PULLUDENABLE	C2C_CLKOUT1_MUXMODE			C2C_CLKOUT0_WAKEUPEVENT	C2C_CLKOUT0_WAKEUPENABLE	RESERVED					C2C_CLKOUT0_INPUTENABLE	RESERVED		C2C_CLKOUT0_PWRDOWN	C2C_CLKOUT0_PULLTYPESELECT	C2C_CLKOUT0_PULLUDENABLE	C2C_CLKOUT0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_CLKOUT1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_CLKOUT1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_CLKOUT1_INPUTENABLE	Input enable value for pad c2c_clkout1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_CLKOUT1_PWRDOWN	Power Down setting for pad c2c_clkout1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_CLKOUT1_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_clkout1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_CLKOUT1_PULLUDENABLE	Pull-Up/Down enable for pad c2c_clkout1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	C2C_CLKOUT1_MUXMODE	Functional multiplexing selection for pad c2c_clkout1 0x0: Reserved 0x3: Select kbd_col8 0x7: Select safe_mode_core21 0x4: Select gpmc_nbe0_cle 0x6: Select gpio2_34	RW	0x4
15	C2C_CLKOUT0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_CLKOUT0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_CLKOUT0_INPUTENABLE	Input enable value for pad c2c_clkout0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_CLKOUT0_PWRDOWN	Power Down setting for pad c2c_clkout0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_CLKOUT0_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_clkout0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_CLKOUT0_PULLUDENABLE	Pull-Up/Down enable for pad c2c_clkout0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_CLKOUT0_MUXMODE	Functional multiplexing selection for pad c2c_clkout0 0x0: Reserved 0x4: Select gpmc_nadv_ale 0x7: Select safe_mode_core20 0x6: Select gpio2_33	RW	0x4

Table 18-483. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_CLKOUT0_PAD1_C2C_CLKOUT1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-484. CONTROL_CORE_PAD0_C2C_CLKIN0_PAD1_C2C_CLKIN1

Address Offset	0x0000 0058		
Physical Address	0x4A00 2858 0x4A00 2858	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_clkin0 and c2c_clkin1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_CLKIN1_WAKEUPEVENT	C2C_CLKIN1_WAKEUPENABLE	RESERVED					C2C_CLKIN1_INPUTENABLE	RESERVED	C2C_CLKIN1_GLITCHGOBBLER	C2C_CLKIN1_PWRDOWN	C2C_CLKIN1_PULLTYPESELECT	C2C_CLKIN1_PULLUDENABLE	C2C_CLKIN1_MUXMODE			C2C_CLKIN0_WAKEUPEVENT	C2C_CLKIN0_WAKEUPENABLE	RESERVED					C2C_CLKIN0_INPUTENABLE	RESERVED		C2C_CLKIN0_PWRDOWN	C2C_CLKIN0_PULLTYPESELECT	C2C_CLKIN0_PULLUDENABLE	C2C_CLKIN0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_CLKIN1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_CLKIN1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_CLKIN1_INPUTENABLE	Input enable value for pad c2c_clkin1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23	RESERVED		R	0
22	C2C_CLKIN1_GLITCHGOBBLER	Glitch Gobbler setting for pad c2c_clkin1 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
21	C2C_CLKIN1_PWRDOWN	Power Down setting for pad c2c_clkin1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_CLKIN1_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_clkin1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_CLKIN1_PULLUDENABLE	Pull-Up/Down enable for pad c2c_clkin1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_CLKIN1_MUXMODE	Functional multiplexing selection for pad c2c_clkin1 0x0: Reserved 0x3: Select kbd_row8 0x7: Select safe_mode_core18 0x4: Select gpmc_clk 0x6: Select gpio2_36	RW	0x4
15	C2C_CLKIN0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_CLKIN0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
8	C2C_CLKIN0_INPUTENABLE	Input enable value for pad c2c_clkin0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_CLKIN0_PWRDOWN	Power Down setting for pad c2c_clkin0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_CLKIN0_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_clkin0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_CLKIN0_PULLUDENABLE	Pull-Up/Down enable for pad c2c_clkin0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_CLKIN0_MUXMODE	Functional multiplexing selection for pad c2c_clkin0 0x0: Reserved 0x6: Select gpio2_35 0x4: Select gpmc_nwp 0x7: Select safe_mode_core19 0x5: Select gpmc_nbe1	RW	0x4

Table 18-485. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_CLKIN0_PAD1_C2C_CLKIN1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-486. CONTROL_CORE_PAD0_C2C_DATAIN0_PAD1_C2C_DATAIN1

Address Offset	0x0000 005C		
Physical Address	0x4A00 285C 0x4A00 285C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_datain0 and c2c_datain1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATAIN1_WAKEUPEVENT	C2C_DATAIN1_WAKEUPENABLE	RESERVED					C2C_DATAIN1_INPUTENABLE	RESERVED		C2C_DATAIN1_PWRDOWN	C2C_DATAIN1_PULLTYPESELECT	C2C_DATAIN1_PULLUDENABLE	C2C_DATAIN1_MUXMODE			C2C_DATAIN0_WAKEUPEVENT	C2C_DATAIN0_WAKEUPENABLE	RESERVED					C2C_DATAIN0_INPUTENABLE	RESERVED		C2C_DATAIN0_PWRDOWN	C2C_DATAIN0_PULLTYPESELECT	C2C_DATAIN0_PULLUDENABLE	C2C_DATAIN0_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	C2C_DATAIN1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATAIN1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATAIN1_INPUTENABLE	Input enable value for pad c2c_datain1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATAIN1_PWRDOWN	Power Down setting for pad c2c_datain1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATAIN1_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_datain1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATAIN1_PULLUDENABLE	Pull-Up/Down enable for pad c2c_datain1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATAIN1_MUXMODE	Functional multiplexing selection for pad c2c_datain1 0x0: Reserved 0x3: Select kbd_row1 0x7: Select safe_mode_core11 0x4: Select gpmc_ad1 0x6: Select gpio2_38	RW	0x4
15	C2C_DATAIN0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATAIN0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATAIN0_INPUTENABLE	Input enable value for pad c2c_datain0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATAIN0_PWRDOWN	Power Down setting for pad c2c_datain0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATAIN0_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_datain0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATAIN0_PULLUDENABLE	Pull-Up/Down enable for pad c2c_datain0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	C2C_DATAIN0_MUXMODE	Functional multiplexing selection for pad c2c_datain0 0x0: Reserved 0x3: Select kbd_row0 0x7: Select safe_mode_core10 0x4: Select gpmc_ad0 0x6: Select gpio2_37	RW	0x4

Table 18-487. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATAIN0_PAD1_C2C_DATAIN1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-488. CONTROL_CORE_PAD0_C2C_DATAIN2_PAD1_C2C_DATAIN3

Address Offset	0x0000 0060		
Physical Address	0x4A00 2860 0x4A00 2860	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_datain2 and c2c_datain3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATAIN3_WAKEUPEVENT	C2C_DATAIN3_WAKEUPENABLE	RESERVED					C2C_DATAIN3_INPUTENABLE	RESERVED		C2C_DATAIN3_PWRDOWN	C2C_DATAIN3_PULLTYPESELECT	C2C_DATAIN3_PULLUDENABLE	C2C_DATAIN3_MUXMODE			C2C_DATAIN2_WAKEUPEVENT	C2C_DATAIN2_WAKEUPENABLE	RESERVED					C2C_DATAIN2_INPUTENABLE	RESERVED		C2C_DATAIN2_PWRDOWN	C2C_DATAIN2_PULLTYPESELECT	C2C_DATAIN2_PULLUDENABLE	C2C_DATAIN2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATAIN3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATAIN3_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATAIN3_INPUTENABLE	Input enable value for pad c2c_datain3 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATAIN3_PWRDOWN	Power Down setting for pad c2c_datain3 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0

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Bits	Field Name	Description	Type	Reset
20	C2C_DATAIN3_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_datain3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATAIN3_PULLUDENABLE	Pull-Up/Down enable for pad c2c_datain3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATAIN3_MUXMODE	Functional multiplexing selection for pad c2c_datain3 0x0: Reserved 0x3: Select kbd_row3 0x7: Select safe_mode_core13 0x4: Select gpmc_ad3 0x6: Select gpio2_40	RW	0x4
15	C2C_DATAIN2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATAIN2_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATAIN2_INPUTENABLE	Input enable value for pad c2c_datain2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATAIN2_PWRDOWN	Power Down setting for pad c2c_datain2 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATAIN2_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_datain2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATAIN2_PULLUDENABLE	Pull-Up/Down enable for pad c2c_datain2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_DATAIN2_MUXMODE	Functional multiplexing selection for pad c2c_datain2 0x0: Reserved 0x3: Select kbd_row2 0x7: Select safe_mode_core12 0x4: Select gpmc_ad2 0x6: Select gpio2_39	RW	0x4

Table 18-489. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATAIN2_PAD1_C2C_DATAIN3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-490. CONTROL_CORE_PAD0_C2C_DATAIN4_PAD1_C2C_DATAIN5

Address Offset	0x0000 0064		
Physical Address	0x4A00 2864 0x4A00 2864	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_datain4 and c2c_datain5 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATAIN5_WAKEUPEVENT	C2C_DATAIN5_WAKEUPENABLE	RESERVED					C2C_DATAIN5_INPUTENABLE	RESERVED		C2C_DATAIN5_PWRDOWN	C2C_DATAIN5_PULLTYPESELECT	C2C_DATAIN5_PULLUDENABLE	C2C_DATAIN5_MUXMODE			C2C_DATAIN4_WAKEUPEVENT	C2C_DATAIN4_WAKEUPENABLE	RESERVED					C2C_DATAIN4_INPUTENABLE	RESERVED		C2C_DATAIN4_PWRDOWN	C2C_DATAIN4_PULLTYPESELECT	C2C_DATAIN4_PULLUDENABLE	C2C_DATAIN4_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATAIN5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATAIN5_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATAIN5_INPUTENABLE	Input enable value for pad c2c_datain5 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATAIN5_PWRDOWN	Power Down setting for pad c2c_datain5 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATAIN5_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_datain5 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATAIN5_PULLUDENABLE	Pull-Up/Down enable for pad c2c_datain5 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATAIN5_MUXMODE	Functional multiplexing selection for pad c2c_datain5 0x0: Reserved 0x3: Select kbd_row5 0x7: Select safe_mode_core15 0x4: Select gpmc_ad5 0x6: Select gpio2_42	RW	0x4
15	C2C_DATAIN4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	C2C_DATAIN4_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATAIN4_INPUTENABLE	Input enable value for pad c2c_datain4 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATAIN4_PWRDOWN	Power Down setting for pad c2c_datain4 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATAIN4_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_datain4 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATAIN4_PULLUDENABLE	Pull-Up/Down enable for pad c2c_datain4 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_DATAIN4_MUXMODE	Functional multiplexing selection for pad c2c_datain4 0x0: Reserved 0x3: Select kbd_row4 0x7: Select safe_mode_core14 0x4: Select gpmc_ad4 0x6: Select gpio2_41	RW	0x4

Table 18-491. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATAIN4_PAD1_C2C_DATAIN5

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-492. CONTROL_CORE_PAD0_C2C_DATAIN6_PAD1_C2C_DATAIN7

Address Offset	0x0000 0068		
Physical Address	0x4A00 2868 0x4A00 2868	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_datain6 and c2c_datain7 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATAIN7_WAKEUPEVENT	C2C_DATAIN7_WAKEUPENABLE	RESERVED					C2C_DATAIN7_INPUTENABLE	RESERVED		C2C_DATAIN7_PWRDOWN	C2C_DATAIN7_PULLTYPESELECT	C2C_DATAIN7_PULLUDENABLE	C2C_DATAIN7_MUXMODE			C2C_DATAIN6_WAKEUPEVENT	C2C_DATAIN6_WAKEUPENABLE	RESERVED					C2C_DATAIN6_INPUTENABLE	RESERVED		C2C_DATAIN6_PWRDOWN	C2C_DATAIN6_PULLTYPESELECT	C2C_DATAIN6_PULLUDENABLE	C2C_DATAIN6_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATAIN7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATAIN7_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATAIN7_INPUTENABLE	Input enable value for pad c2c_datain7 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATAIN7_PWRDOWN	Power Down setting for pad c2c_datain7 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATAIN7_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_datain7 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATAIN7_PULLUDENABLE	Pull-Up/Down enable for pad c2c_datain7 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATAIN7_MUXMODE	Functional multiplexing selection for pad c2c_datain7 0x0: Reserved 0x3: Select kbd_row7 0x7: Select safe_mode_core17 0x4: Select gpmc_ad7 0x6: Select gpio2_44	RW	0x4
15	C2C_DATAIN6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATAIN6_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATAIN6_INPUTENABLE	Input enable value for pad c2c_datain6 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
7:6	RESERVED		R	0x0
5	C2C_DATAIN6_PWRDOWN	Power Down setting for pad c2c_datain6 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATAIN6_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_datain6 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATAIN6_PULLUDENABLE	Pull-Up/Down enable for pad c2c_datain6 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_DATAIN6_MUXMODE	Functional multiplexing selection for pad c2c_datain6 0x0: Reserved 0x3: Select kbd_row6 0x7: Select safe_mode_core16 0x4: Select gpmc_ad6 0x6: Select gpio2_43	RW	0x4

Table 18-493. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATAIN6_PAD1_C2C_DATAIN7

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-494. CONTROL_CORE_PAD0_C2C_DATAOUT0_PAD1_C2C_DATAOUT1

Address Offset	0x0000 006C		
Physical Address	0x4A00 286C 0x4A00 286C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_dataout0 and c2c_dataout1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATAOUT1_WAKEUPEVENT	C2C_DATAOUT1_WAKEUPENABLE	RESERVED					C2C_DATAOUT1_INPUTENABLE	RESERVED		C2C_DATAOUT1_PWRDOWN	C2C_DATAOUT1_PULLTYPESELECT	C2C_DATAOUT1_PULLUDENABLE	C2C_DATAOUT1_MUXMODE			C2C_DATAOUT0_WAKEUPEVENT	C2C_DATAOUT0_WAKEUPENABLE	RESERVED					C2C_DATAOUT0_INPUTENABLE	RESERVED		C2C_DATAOUT0_PWRDOWN	C2C_DATAOUT0_PULLTYPESELECT	C2C_DATAOUT0_PULLUDENABLE	C2C_DATAOUT0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATAOUT1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	C2C_DATAOUT1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATAOUT1_INPUTENABLE	Input enable value for pad c2c_dataout1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATAOUT1_PWRDOWN	Power Down setting for pad c2c_dataout1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATAOUT1_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_dataout1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATAOUT1_PULLUDENABLE	Pull-Up/Down enable for pad c2c_dataout1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATAOUT1_MUXMODE	Functional multiplexing selection for pad c2c_dataout1 0x6: Select gpio2_57 0x7: Select safe_mode_core23 0x0: Reserved 0x4: Select gpmc_ad9 0x5: Select hw_dbg17 0x3: Select kbd_col1	RW	0x4
15	C2C_DATAOUT0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATAOUT0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATAOUT0_INPUTENABLE	Input enable value for pad c2c_dataout0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATAOUT0_PWRDOWN	Power Down setting for pad c2c_dataout0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATAOUT0_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_dataout0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATAOUT0_PULLUDENABLE	Pull-Up/Down enable for pad c2c_dataout0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	C2C_DATAOUT0_MUXMODE	Functional multiplexing selection for pad c2c_dataout0 0x6: Select gpio2_56 0x7: Select safe_mode_core22 0x0: Reserved 0x4: Select gpmc_ad8 0x5: Select hw_dbg16 0x3: Select kbd_col0	RW	0x4

Table 18-495. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATAOUT0_PAD1_C2C_DATAOUT1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [3]

Table 18-496. CONTROL_CORE_PAD0_C2C_DATAOUT2_PAD1_C2C_DATAOUT3

Address Offset	0x0000 0070		
Physical Address	0x4A00 2870 0x4A00 2870	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_dataout2 and c2c_dataout3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATAOUT3_WAKEUPEVENT	C2C_DATAOUT3_WAKEUPENABLE	RESERVED					C2C_DATAOUT3_INPUTENABLE	RESERVED		C2C_DATAOUT3_PWRDOWN	C2C_DATAOUT3_PULLTYPESELECT	C2C_DATAOUT3_PULLUDENABLE	C2C_DATAOUT3_MUXMODE			C2C_DATAOUT2_WAKEUPEVENT	C2C_DATAOUT2_WAKEUPENABLE	RESERVED					C2C_DATAOUT2_INPUTENABLE	RESERVED		C2C_DATAOUT2_PWRDOWN	C2C_DATAOUT2_PULLTYPESELECT	C2C_DATAOUT2_PULLUDENABLE	C2C_DATAOUT2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATAOUT3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATAOUT3_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATAOUT3_INPUTENABLE	Input enable value for pad c2c_dataout3 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	C2C_DATAOUT3_PWRDOWN	Power Down setting for pad c2c_dataout3 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATAOUT3_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_dataout3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATAOUT3_PULLUDENABLE	Pull-Up/Down enable for pad c2c_dataout3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATAOUT3_MUXMODE	Functional multiplexing selection for pad c2c_dataout3 0x6: Select gpio2_59 0x7: Select safe_mode_core25 0x0: Reserved 0x4: Select gpmc_ad11 0x5: Select hw_dbg19 0x3: Select kbd_col3	RW	0x4
15	C2C_DATAOUT2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATAOUT2_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATAOUT2_INPUTENABLE	Input enable value for pad c2c_dataout2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATAOUT2_PWRDOWN	Power Down setting for pad c2c_dataout2 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATAOUT2_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_dataout2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATAOUT2_PULLUDENABLE	Pull-Up/Down enable for pad c2c_dataout2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_DATAOUT2_MUXMODE	Functional multiplexing selection for pad c2c_dataout2 0x6: Select gpio2_58 0x7: Select safe_mode_core24 0x0: Reserved 0x4: Select gpmc_ad10 0x5: Select hw_dbg18 0x3: Select kbd_col2	RW	0x4

Table 18-497. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATAOUT2_PAD1_C2C_DATAOUT3

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-497. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATAOUT2_PAD1_C2C_DATAOUT3 (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-498. CONTROL_CORE_PAD0_C2C_DATAOUT4_PAD1_C2C_DATAOUT5

Address Offset	0x0000 0074		
Physical Address	0x4A00 2874 0x4A00 2874	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_dataout4 and c2c_dataout5 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATAOUT5_WAKEUPEVENT	C2C_DATAOUT5_WAKEUPENABLE	RESERVED					C2C_DATAOUT5_INPUTENABLE	RESERVED		C2C_DATAOUT5_PWRDOWN	C2C_DATAOUT5_PULLTYPESELECT	C2C_DATAOUT5_PULLUDENABLE	C2C_DATAOUT5_MUXMODE			C2C_DATAOUT4_WAKEUPEVENT	C2C_DATAOUT4_WAKEUPENABLE	RESERVED					C2C_DATAOUT4_INPUTENABLE	RESERVED		C2C_DATAOUT4_PWRDOWN	C2C_DATAOUT4_PULLTYPESELECT	C2C_DATAOUT4_PULLUDENABLE	C2C_DATAOUT4_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATAOUT5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATAOUT5_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATAOUT5_INPUTENABLE	Input enable value for pad c2c_dataout5 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATAOUT5_PWRDOWN	Power Down setting for pad c2c_dataout5 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATAOUT5_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_dataout5 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATAOUT5_PULLUDENABLE	Pull-Up/Down enable for pad c2c_dataout5 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	C2C_DATAOUT5_MUXMODE	Functional multiplexing selection for pad c2c_dataout5 0x6: Select gpio2_61 0x7: Select safe_mode_core27 0x0: Reserved 0x4: Select gpmc_ad13 0x5: Select hw_dbg21 0x3: Select kbd_col5	RW	0x4
15	C2C_DATAOUT4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATAOUT4_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATAOUT4_INPUTENABLE	Input enable value for pad c2c_dataout4 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATAOUT4_PWRDOWN	Power Down setting for pad c2c_dataout4 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATAOUT4_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_dataout4 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATAOUT4_PULLUDENABLE	Pull-Up/Down enable for pad c2c_dataout4 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_DATAOUT4_MUXMODE	Functional multiplexing selection for pad c2c_dataout4 0x6: Select gpio2_60 0x7: Select safe_mode_core26 0x0: Reserved 0x4: Select gpmc_ad12 0x5: Select hw_dbg20 0x3: Select kbd_col4	RW	0x4

Table 18-499. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATAOUT4_PAD1_C2C_DATAOUT5

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-500. CONTROL_CORE_PAD0_C2C_DATAOUT6_PAD1_C2C_DATAOUT7

Address Offset	0x0000 0078		
Physical Address	0x4A00 2878 0x4A00 2878	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_dataout6 and c2c_dataout7 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATAOUT7_WAKEUPEVENT	C2C_DATAOUT7_WAKEUPENABLE	RESERVED					C2C_DATAOUT7_INPUTENABLE	RESERVED		C2C_DATAOUT7_PWRDOWN	C2C_DATAOUT7_PULLTYPESELECT	C2C_DATAOUT7_PULLUDENABLE	C2C_DATAOUT7_MUXMODE			C2C_DATAOUT6_WAKEUPEVENT	C2C_DATAOUT6_WAKEUPENABLE	RESERVED					C2C_DATAOUT6_INPUTENABLE	RESERVED		C2C_DATAOUT6_PWRDOWN	C2C_DATAOUT6_PULLTYPESELECT	C2C_DATAOUT6_PULLUDENABLE	C2C_DATAOUT6_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATAOUT7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATAOUT7_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATAOUT7_INPUTENABLE	Input enable value for pad c2c_dataout7 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATAOUT7_PWRDOWN	Power Down setting for pad c2c_dataout7 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATAOUT7_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_dataout7 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATAOUT7_PULLUDENABLE	Pull-Up/Down enable for pad c2c_dataout7 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATAOUT7_MUXMODE	Functional multiplexing selection for pad c2c_dataout7 0x6: Select gpio2_63 0x7: Select safe_mode_core29 0x0: Reserved 0x4: Select gpmc_ad15 0x5: Select hw_dbg23 0x3: Select kbd_col7	RW	0x4
15	C2C_DATAOUT6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATAOUT6_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
8	C2C_DATAOUT6_INPUTENABLE	Input enable value for pad c2c_dataout6 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATAOUT6_PWRDOWN	Power Down setting for pad c2c_dataout6 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATAOUT6_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_dataout6 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATAOUT6_PULLUDENABLE	Pull-Up/Down enable for pad c2c_dataout6 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_DATAOUT6_MUXMODE	Functional multiplexing selection for pad c2c_dataout6 0x6: Select gpio2_62 0x7: Select safe_mode_core28 0x0: Reserved 0x4: Select gpmc_ad14 0x5: Select hw_dbg22 0x3: Select kbd_col6	RW	0x4

Table 18-501. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATAOUT6_PAD1_C2C_DATAOUT7

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-502. CONTROL_CORE_PAD0_C2C_DATA8_PAD1_C2C_DATA9

Address Offset	0x0000 007C		
Physical Address	0x4A00 287C 0x4A00 287C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_data8 and c2c_data9 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATA9_WAKEUPEVENT	C2C_DATA9_WAKEUPENABLE	RESERVED					C2C_DATA9_INPUTENABLE	RESERVED		C2C_DATA9_PWRDOWN	C2C_DATA9_PULLTYPESELECT	C2C_DATA9_PULLUDENABLE	C2C_DATA9_MUXMODE			C2C_DATA8_WAKEUPEVENT	C2C_DATA8_WAKEUPENABLE	RESERVED					C2C_DATA8_INPUTENABLE	RESERVED		C2C_DATA8_PWRDOWN	C2C_DATA8_PULLTYPESELECT	C2C_DATA8_PULLUDENABLE	C2C_DATA8_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	C2C_DATA9_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATA9_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATA9_INPUTENABLE	Input enable value for pad c2c_data9 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATA9_PWRDOWN	Power Down setting for pad c2c_data9 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATA9_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_data9 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATA9_PULLUDENABLE	Pull-Up/Down enable for pad c2c_data9 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATA9_MUXMODE	Functional multiplexing selection for pad c2c_data9 0x0: Reserved 0x6: Select gpio4_114 0x4: Select gpmc_a17 0x7: Select safe_mode_core31 0x5: Select hw_dbg25	RW	0x7
15	C2C_DATA8_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATA8_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATA8_INPUTENABLE	Input enable value for pad c2c_data8 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATA8_PWRDOWN	Power Down setting for pad c2c_data8 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATA8_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_data8 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATA8_PULLUDENABLE	Pull-Up/Down enable for pad c2c_data8 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	C2C_DATA8_MUXMODE	Functional multiplexing selection for pad c2c_data8 0x0: Reserved 0x6: Select gpio4_113 0x4: Select gpmc_a16 0x7: Select safe_mode_core30 0x5: Select hw_dbg24	RW	0x7

Table 18-503. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATA8_PAD1_C2C_DATA9

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-504. CONTROL_CORE_PAD0_C2C_DATA10_PAD1_C2C_DATA11

Address Offset	0x0000 0080		
Physical Address	0x4A00 2880 0x4A00 2880	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_data10 and c2c_data11 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATA11_WAKEUPEVENT	C2C_DATA11_WAKEUPENABLE	RESERVED					C2C_DATA11_INPUTENABLE	RESERVED		C2C_DATA11_PWRDOWN	C2C_DATA11_PULLTYPESELECT	C2C_DATA11_PULLUDENABLE	C2C_DATA11_MUXMODE			C2C_DATA10_WAKEUPEVENT	C2C_DATA10_WAKEUPENABLE	RESERVED					C2C_DATA10_INPUTENABLE	RESERVED		C2C_DATA10_PWRDOWN	C2C_DATA10_PULLTYPESELECT	C2C_DATA10_PULLUDENABLE	C2C_DATA10_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATA11_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATA11_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATA11_INPUTENABLE	Input enable value for pad c2c_data11 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATA11_PWRDOWN	Power Down setting for pad c2c_data11 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0

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Bits	Field Name	Description	Type	Reset
20	C2C_DATA11_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_data11 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATA11_PULLUDENABLE	Pull-Up/Down enable for pad c2c_data11 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATA11_MUXMODE	Functional multiplexing selection for pad c2c_data11 0x0: Reserved 0x6: Select gpio4_116 0x4: Select gpmc_a19 0x7: Select safe_mode_core33 0x5: Select hw_dbg27	RW	0x7
15	C2C_DATA10_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATA10_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATA10_INPUTENABLE	Input enable value for pad c2c_data10 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATA10_PWRDOWN	Power Down setting for pad c2c_data10 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATA10_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_data10 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATA10_PULLUDENABLE	Pull-Up/Down enable for pad c2c_data10 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_DATA10_MUXMODE	Functional multiplexing selection for pad c2c_data10 0x0: Reserved 0x6: Select gpio4_115 0x4: Select gpmc_a18 0x7: Select safe_mode_core32 0x5: Select hw_dbg26	RW	0x7

Table 18-505. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATA10_PAD1_C2C_DATA11

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-506. CONTROL_CORE_PAD0_C2C_DATA12_PAD1_C2C_DATA13

Address Offset	0x0000 0084		
Physical Address	0x4A00 2884 0x4A00 2884	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_data12 and c2c_data13 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATA13_WAKEUPEVENT	C2C_DATA13_WAKEUPENABLE	RESERVED					C2C_DATA13_INPUTENABLE	RESERVED		C2C_DATA13_PWRDOWN	C2C_DATA13_PULLTYPESELECT	C2C_DATA13_PULLUDENABLE	C2C_DATA13_MUXMODE			C2C_DATA12_WAKEUPEVENT	C2C_DATA12_WAKEUPENABLE	RESERVED					C2C_DATA12_INPUTENABLE	RESERVED		C2C_DATA12_PWRDOWN	C2C_DATA12_PULLTYPESELECT	C2C_DATA12_PULLUDENABLE	C2C_DATA12_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATA13_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATA13_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATA13_INPUTENABLE	Input enable value for pad c2c_data13 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATA13_PWRDOWN	Power Down setting for pad c2c_data13 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATA13_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_data13 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATA13_PULLUDENABLE	Pull-Up/Down enable for pad c2c_data13 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATA13_MUXMODE	Functional multiplexing selection for pad c2c_data13 0x0: Reserved 0x6: Select gpio4_118 0x4: Select gpmc_a21 0x7: Select safe_mode_core35 0x5: Select hw_dbg29	RW	0x7
15	C2C_DATA12_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	C2C_DATA12_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATA12_INPUTENABLE	Input enable value for pad c2c_data12 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	C2C_DATA12_PWRDOWN	Power Down setting for pad c2c_data12 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATA12_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_data12 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATA12_PULLUDENABLE	Pull-Up/Down enable for pad c2c_data12 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_DATA12_MUXMODE	Functional multiplexing selection for pad c2c_data12 0x0: Reserved 0x6: Select gpio4_117 0x4: Select gpmc_a20 0x7: Select safe_mode_core34 0x5: Select hw_dbg28	RW	0x7

Table 18-507. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATA12_PAD1_C2C_DATA13

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-508. CONTROL_CORE_PAD0_C2C_DATA14_PAD1_C2C_DATA15

Address Offset	0x0000 0088		
Physical Address	0x4A00 2888 0x4A00 2888	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads c2c_data14 and c2c_data15 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATA15_WAKEUPEVENT	C2C_DATA15_WAKEUPENABLE	RESERVED					C2C_DATA15_INPUTENABLE	RESERVED		C2C_DATA15_PWRDOWN	C2C_DATA15_PULLTYPESELECT	C2C_DATA15_PULLUDENABLE	C2C_DATA15_MUXMODE			C2C_DATA14_WAKEUPEVENT	C2C_DATA14_WAKEUPENABLE	RESERVED					C2C_DATA14_INPUTENABLE	RESERVED		C2C_DATA14_PWRDOWN	C2C_DATA14_PULLTYPESELECT	C2C_DATA14_PULLUDENABLE	C2C_DATA14_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	C2C_DATA15_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	C2C_DATA15_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	C2C_DATA15_INPUTENABLE	Input enable value for pad c2c_data15 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	C2C_DATA15_PWRDOWN	Power Down setting for pad c2c_data15 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	C2C_DATA15_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_data15 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	C2C_DATA15_PULLUDENABLE	Pull-Up/Down enable for pad c2c_data15 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	C2C_DATA15_MUXMODE	Functional multiplexing selection for pad c2c_data15 0x0: Reserved 0x6: Select gpio4_120 0x4: Select gpmc_a23 0x7: Select safe_mode_core37 0x5: Select hw_dbg31	RW	0x7
15	C2C_DATA14_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	C2C_DATA14_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	C2C_DATA14_INPUTENABLE	Input enable value for pad c2c_data14 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	C2C_DATA14_PWRDOWN	Power Down setting for pad c2c_data14 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	C2C_DATA14_PULLTYPESELECT	Pull-Up/Down selection for pad c2c_data14 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	C2C_DATA14_PULLUDENABLE	Pull-Up/Down enable for pad c2c_data14 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	C2C_DATA14_MUXMODE	Functional multiplexing selection for pad c2c_data14 0x0: Reserved 0x6: Select gpio4_119 0x4: Select gpmc_a22 0x7: Select safe_mode_core36 0x5: Select hw_dbg30	RW	0x7

Table 18-509. Register Call Summary for Register CONTROL_CORE_PAD0_C2C_DATA14_PAD1_C2C_DATA15

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [3]

Table 18-510. CONTROL_CORE_PAD0_LLIA_WAKEREQOUT_PAD1_LLIB_WAKEREQOUT

Address Offset	0x0000 008C		
Physical Address	0x4A00 288C 0x4A00 288C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads llia_wakereqout and llib_wakereqout Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LLIB_WAKEREQOUT_WAKEUPEVENT	LLIB_WAKEREQOUT_WAKEUPENABLE	RESERVED					LLIB_WAKEREQOUT_INPUTENABLE	RESERVED		LLIB_WAKEREQOUT_PWRDOWN	LLIB_WAKEREQOUT_PULLTYPESELECT	LLIB_WAKEREQOUT_PULLUDENABLE	LLIB_WAKEREQOUT_MUXMODE			LLIA_WAKEREQOUT_WAKEUPEVENT	LLIA_WAKEREQOUT_WAKEUPENABLE	RESERVED					LLIA_WAKEREQOUT_INPUTENABLE	RESERVED		LLIA_WAKEREQOUT_PWRDOWN	LLIA_WAKEREQOUT_PULLTYPESELECT	LLIA_WAKEREQOUT_PULLUDENABLE	LLIA_WAKEREQOUT_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	LLIB_WAKEREQOUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	LLIB_WAKEREQOUT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	LLIB_WAKEREQOUT_INPUTENABLE	Input enable value for pad llib_wakereqout 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	LLIB_WAKEREQOUT_PWRDOWN	Power Down setting for pad llib_wakereqout 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	LLIB_WAKEREQOUT_PULLTYPESELECT	Pull-Up/Down selection for pad llib_wakereqout 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	LLIB_WAKEREQOUT_PULLUDENABLE	Pull-Up/Down enable for pad llib_wakereqout 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	LLIB_WAKEREQOUT_MUXMODE	Functional multiplexing selection for pad llib_wakereqout 0x0: Select llib_wakereqout 0x4: Select gpmc_ncs0 0x7: Select safe_mode_core38 0x6: Select gpio2_32	RW	0x4
15	LLIA_WAKEREQOUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	LLIA_WAKEREQOUT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	LLIA_WAKEREQOUT_INPUTENABLE	Input enable value for pad llia_wakereqout 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	LLIA_WAKEREQOUT_PWRDOWN	Power Down setting for pad llia_wakereqout 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	LLIA_WAKEREQOUT_PULLTYPESELECT	Pull-Up/Down selection for pad llia_wakereqout 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	LLIA_WAKEREQOUT_PULLUDENABLE	Pull-Up/Down enable for pad llia_wakereqout 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	LLIA_WAKEREQOUT_MUXMODE	Functional multiplexing selection for pad llia_wakereqout 0x0: Select llia_wakereqout 0x1: Select c2c_wakereqout 0x4: Select gpmc_wait0 0x7: Select safe_mode_core39 0x6: Select gpio2_45	RW	0x4

Table 18-511. Register Call Summary for Register CONTROL_CORE_PAD0_LLIA_WAKEREQOUT_PAD1_LLIB_WAKEREQOUT

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-512. CONTROL_CORE_PAD0_HSI1_ACREADY_PAD1_HSI1_CAREADY

Address Offset	0x0000 0090		
Physical Address	0x4A00 2890 0x4A00 2890	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hsi1_acready and hsi1_caready Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSI1_CAREADY_WAKEUPEVENT	HSI1_CAREADY_WAKEUPENABLE	RESERVED					HSI1_CAREADY_INPUTENABLE	RESERVED		HSI1_CAREADY_PWRDOWN	HSI1_CAREADY_PULLTYPESELECT	HSI1_CAREADY_PULLUDENABLE	HSI1_CAREADY_MUXMODE			HSI1_ACREADY_WAKEUPEVENT	HSI1_ACREADY_WAKEUPENABLE	RESERVED					HSI1_ACREADY_INPUTENABLE	RESERVED	HSI1_ACREADY_GLITCHGOBBLER	HSI1_ACREADY_PWRDOWN	HSI1_ACREADY_PULLTYPESELECT	HSI1_ACREADY_PULLUDENABLE	HSI1_ACREADY_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HSI1_CAREADY_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	HSI1_CAREADY_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	HSI1_CAREADY_INPUTENABLE	Input enable value for pad hsi1_caready 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	HSI1_CAREADY_PWRDOWN	Power Down setting for pad hsi1_caready 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HSI1_CAREADY_PULLTYPESELECT	Pull-Up/Down selection for pad hsi1_caready 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	HSI1_CAREADY_PULLUDENABLE	Pull-Up/Down enable for pad hsi1_caready 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	HSI1_CAREADY_MUXMODE	Functional multiplexing selection for pad hsi1_caready 0x0: Select hsi1_caready 0x3: Select usbb2_ulpitll_nxt 0x7: Select safe_mode_core41 0x6: Select gpio3_65	RW	0x7
15	HSI1_ACREADY_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HSI1_ACREADY_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HSI1_ACREADY_INPUTENABLE	Input enable value for pad hsi1_acready 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7	RESERVED		R	0
6	HSI1_ACREADY_GLITCHGOBBLER	Glitch Gobbler setting for pad hsi1_acready 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
5	HSI1_ACREADY_PWRDOWN	Power Down setting for pad hsi1_acready 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HSI1_ACREADY_PULLTYPESELECT	Pull-Up/Down selection for pad hsi1_acready 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	HSI1_ACREADY_PULLUDENABLE	Pull-Up/Down enable for pad hsi1_acready 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HSI1_ACREADY_MUXMODE	Functional multiplexing selection for pad hsi1_acready 0x0: Select hsi1_acready 0x1: Select cam_strobe 0x3: Select usbb2_ulpitll_clk 0x7: Select safe_mode_core40 0x6: Select gpio3_64	RW	0x7

Table 18-513. Register Call Summary for Register CONTROL_CORE_PAD0_HSI1_ACREADY_PAD1_HSI1_CAREADY

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-513. Register Call Summary for Register CONTROL_CORE_PAD0_HSI1_ACREADY_PAD1_HSI1_CAREADY (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-514. CONTROL_CORE_PAD0_HSI1_ACWAKE_PAD1_HSI1_CAWAKE

Address Offset	0x0000 0094		
Physical Address	0x4A00 2894 0x4A00 2894	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hsi1_acwake and hsi1_cawake Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSI1_CAWAKE_WAKEUPEVENT	HSI1_CAWAKE_WAKEUPENABLE	RESERVED					HSI1_CAWAKE_INPUTENABLE	RESERVED		HSI1_CAWAKE_PWRDOWN	HSI1_CAWAKE_PULLTYPESELECT	HSI1_CAWAKE_PULLUDENABLE	HSI1_CAWAKE_MUXMODE			HSI1_ACWAKE_WAKEUPEVENT	HSI1_ACWAKE_WAKEUPENABLE	RESERVED					HSI1_ACWAKE_INPUTENABLE	RESERVED		HSI1_ACWAKE_PWRDOWN	HSI1_ACWAKE_PULLTYPESELECT	HSI1_ACWAKE_PULLUDENABLE	HSI1_ACWAKE_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HSI1_CAWAKE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	HSI1_CAWAKE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	HSI1_CAWAKE_INPUTENABLE	Input enable value for pad hsi1_cawake 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	HSI1_CAWAKE_PWRDOWN	Power Down setting for pad hsi1_cawake 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HSI1_CAWAKE_PULLTYPESELECT	Pull-Up/Down selection for pad hsi1_cawake 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	HSI1_CAWAKE_PULLUDENABLE	Pull-Up/Down enable for pad hsi1_cawake 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	HSI1_CAWAKE_MUXMODE	Functional multiplexing selection for pad hsi1_cawake 0x0: Select hsi1_cawake 0x3: Select usbb2_ulpitll_stp 0x7: Select safe_mode_core43 0x6: Select gpio3_67	RW	0x7
15	HSI1_ACWAKE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HSI1_ACWAKE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HSI1_ACWAKE_INPUTENABLE	Input enable value for pad hsi1_acwake 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	HSI1_ACWAKE_PWRDOWN	Power Down setting for pad hsi1_acwake 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HSI1_ACWAKE_PULLTYPESELECT	Pull-Up/Down selection for pad hsi1_acwake 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	HSI1_ACWAKE_PULLUDENABLE	Pull-Up/Down enable for pad hsi1_acwake 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HSI1_ACWAKE_MUXMODE	Functional multiplexing selection for pad hsi1_acwake 0x0: Select hsi1_acwake 0x3: Select usbb2_ulpitll_dir 0x7: Select safe_mode_core42 0x6: Select gpio3_66	RW	0x7

Table 18-515. Register Call Summary for Register CONTROL_CORE_PAD0_HSI1_ACWAKE_PAD1_HSI1_CAWAKE

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-516. CONTROL_CORE_PAD0_HSI1_ACFLAG_PAD1_HSI1_ACDATA

Address Offset	0x0000 0098		
Physical Address	0x4A00 2898 0x4A00 2898	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hsi1_acflag and hsi1_acdata Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSI1_ACDATA_WAKEUPEVENT	HSI1_ACDATA_WAKEUPENABLE	RESERVED					HSI1_ACDATA_INPUTENABLE	RESERVED		HSI1_ACDATA_PWRDOWN	HSI1_ACDATA_PULLTYPESELECT	HSI1_ACDATA_PULLUDENABLE	HSI1_ACDATA_MUXMODE			HSI1_ACFLAG_WAKEUPEVENT	HSI1_ACFLAG_WAKEUPENABLE	RESERVED					HSI1_ACFLAG_INPUTENABLE	RESERVED		HSI1_ACFLAG_PWRDOWN	HSI1_ACFLAG_PULLTYPESELECT	HSI1_ACFLAG_PULLUDENABLE	HSI1_ACFLAG_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HSI1_ACDATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	HSI1_ACDATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	HSI1_ACDATA_INPUTENABLE	Input enable value for pad hsi1_acdata 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	HSI1_ACDATA_PWRDOWN	Power Down setting for pad hsi1_acdata 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HSI1_ACDATA_PULLTYPESELECT	Pull-Up/Down selection for pad hsi1_acdata 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	HSI1_ACDATA_PULLUDENABLE	Pull-Up/Down enable for pad hsi1_acdata 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	HSI1_ACDATA_MUXMODE	Functional multiplexing selection for pad hsi1_acdata 0x0: Select hsi1_acdata 0x3: Select usbb2_ulpitll_data1 0x7: Select safe_mode_core45 0x6: Select gpio3_69	RW	0x7
15	HSI1_ACFLAG_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HSI1_ACFLAG_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HSI1_ACFLAG_INPUTENABLE	Input enable value for pad hsi1_acflag 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	HSI1_ACFLAG_PWRDOWN	Power Down setting for pad hsi1_acflag 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HSI1_ACFLAG_PULLTYPESELECT	Pull-Up/Down selection for pad hsi1_acflag 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	HSI1_ACFLAG_PULLUDENABLE	Pull-Up/Down enable for pad hsi1_acflag 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HSI1_ACFLAG_MUXMODE	Functional multiplexing selection for pad hsi1_acflag 0x0: Select hsi1_acflag 0x3: Select usbb2_ulpitll_data0 0x7: Select safe_mode_core44 0x6: Select gpio3_68	RW	0x7

Table 18-517. Register Call Summary for Register CONTROL_CORE_PAD0_HSI1_ACFLAG_PAD1_HSI1_ACDATA

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-518. CONTROL_CORE_PAD0_HSI1_CAFLAG_PAD1_HSI1_CADATA

Address Offset	0x0000 009C		
Physical Address	0x4A00 289C 0x4A00 289C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hsi1_caflag and hsi1_cadata Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSI1_CADATA_WAKEUPEVENT	HSI1_CADATA_WAKEUPENABLE	RESERVED					HSI1_CADATA_INPUTENABLE	RESERVED		HSI1_CADATA_PWRDOWN	HSI1_CADATA_PULLTYPESELECT	HSI1_CADATA_PULLUDENABLE	HSI1_CADATA_MUXMODE			HSI1_CAFLAG_WAKEUPEVENT	HSI1_CAFLAG_WAKEUPENABLE	RESERVED					HSI1_CAFLAG_INPUTENABLE	RESERVED		HSI1_CAFLAG_PWRDOWN	HSI1_CAFLAG_PULLTYPESELECT	HSI1_CAFLAG_PULLUDENABLE	HSI1_CAFLAG_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HSI1_CADATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	HSI1_CADATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29:25	RESERVED		R	0x0
24	HSI1_CADATA_INPUTENABLE	Input enable value for pad hsi1_cadata 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	HSI1_CADATA_PWRDOWN	Power Down setting for pad hsi1_cadata 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HSI1_CADATA_PULLTYPESELECT	Pull-Up/Down selection for pad hsi1_cadata 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	HSI1_CADATA_PULLUDENABLE	Pull-Up/Down enable for pad hsi1_cadata 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	HSI1_CADATA_MUXMODE	Functional multiplexing selection for pad hsi1_cadata 0x0: Select hsi1_cadata 0x3: Select usbb2_ulpitll_data3 0x7: Select safe_mode_core47 0x6: Select gpio3_71	RW	0x7
15	HSI1_CAFLAG_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HSI1_CAFLAG_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HSI1_CAFLAG_INPUTENABLE	Input enable value for pad hsi1_caflag 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	HSI1_CAFLAG_PWRDOWN	Power Down setting for pad hsi1_caflag 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HSI1_CAFLAG_PULLTYPESELECT	Pull-Up/Down selection for pad hsi1_caflag 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	HSI1_CAFLAG_PULLUDENABLE	Pull-Up/Down enable for pad hsi1_caflag 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HSI1_CAFLAG_MUXMODE	Functional multiplexing selection for pad hsi1_caflag 0x0: Select hsi1_caflag 0x3: Select usbb2_ulpitll_data2 0x7: Select safe_mode_core46 0x6: Select gpio3_70	RW	0x7

Table 18-519. Register Call Summary for Register CONTROL_CORE_PAD0_HSI1_CAFLAG_PAD1_HSI1_CADATA

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-519. Register Call Summary for Register CONTROL_CORE_PAD0_HSI1_CAFLAG_PAD1_HSI1_CADATA (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-520. CONTROL_CORE_PAD0_UART1_TX_PAD1_UART1_CTS

Address Offset	0x0000 00A0		
Physical Address	0x4A00 28A0 0x4A00 28A0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart1_tx and uart1_cts Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART1_CTS_WAKEUPEVENT	UART1_CTS_WAKEUPENABLE	RESERVED					UART1_CTS_INPUTENABLE	RESERVED		UART1_CTS_PWRDOWN	UART1_CTS_PULLTYPESELECT	UART1_CTS_PULLUDENABLE	UART1_CTS_MUXMODE			UART1_TX_WAKEUPEVENT	UART1_TX_WAKEUPENABLE	RESERVED					UART1_TX_INPUTENABLE	RESERVED		UART1_TX_PWRDOWN	UART1_TX_PULLTYPESELECT	UART1_TX_PULLUDENABLE	UART1_TX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART1_CTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART1_CTS_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	UART1_CTS_INPUTENABLE	Input enable value for pad uart1_cts 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	UART1_CTS_PWRDOWN	Power Down setting for pad uart1_cts 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	UART1_CTS_PULLTYPESELECT	Pull-Up/Down selection for pad uart1_cts 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART1_CTS_PULLUDENABLE	Pull-Up/Down enable for pad uart1_cts 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	UART1_CTS_MUXMODE	Functional multiplexing selection for pad uart1_cts 0x0: Select uart1_cts 0x3: Select usbb2_ulpitll_data5 0x7: Select safe_mode_core49 0x4: Select gpmc_wait3 0x6: Select gpio3_73	RW	0x7
15	UART1_TX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART1_TX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	UART1_TX_INPUTENABLE	Input enable value for pad uart1_tx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	UART1_TX_PWRDOWN	Power Down setting for pad uart1_tx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART1_TX_PULLTYPESELECT	Pull-Up/Down selection for pad uart1_tx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	UART1_TX_PULLUDENABLE	Pull-Up/Down enable for pad uart1_tx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART1_TX_MUXMODE	Functional multiplexing selection for pad uart1_tx 0x0: Select uart1_tx 0x3: Select usbb2_ulpitll_data4 0x7: Select safe_mode_core48 0x6: Select gpio3_72	RW	0x7

Table 18-521. Register Call Summary for Register CONTROL_CORE_PAD0_UART1_TX_PAD1_UART1_CTS

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-522. CONTROL_CORE_PAD0_UART1_RX_PAD1_UART1_RTS

Address Offset	0x0000 00A4		
Physical Address	0x4A00 28A4 0x4A00 28A4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart1_rx and uart1_rts Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART1_RTS_WAKEUPEVENT	UART1_RTS_WAKEUPENABLE	RESERVED					UART1_RTS_INPUTENABLE	RESERVED		UART1_RTS_PWRDOWN	UART1_RTS_PULLTYPESELECT	UART1_RTS_PULLUDENABLE	UART1_RTS_MUXMODE			UART1_RX_WAKEUPEVENT	UART1_RX_WAKEUPENABLE	RESERVED					UART1_RX_INPUTENABLE	RESERVED		UART1_RX_PWRDOWN	UART1_RX_PULLTYPESELECT	UART1_RX_PULLUDENABLE	UART1_RX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART1_RTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART1_RTS_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	UART1_RTS_INPUTENABLE	Input enable value for pad uart1_rts 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	UART1_RTS_PWRDOWN	Power Down setting for pad uart1_rts 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	UART1_RTS_PULLTYPESELECT	Pull-Up/Down selection for pad uart1_rts 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART1_RTS_PULLUDENABLE	Pull-Up/Down enable for pad uart1_rts 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	UART1_RTS_MUXMODE	Functional multiplexing selection for pad uart1_rts 0x0: Select uart1_rts 0x3: Select usbb2_ulpitll_data7 0x7: Select safe_mode_core51 0x4: Select gpmc_ncs7 0x6: Select gpio3_75	RW	0x7
15	UART1_RX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART1_RX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	UART1_RX_INPUTENABLE	Input enable value for pad uart1_rx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	UART1_RX_PWRDOWN	Power Down setting for pad uart1_rx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART1_RX_PULLTYPESELECT	Pull-Up/Down selection for pad uart1_rx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	UART1_RX_PULLUDENABLE	Pull-Up/Down enable for pad uart1_rx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART1_RX_MUXMODE	Functional multiplexing selection for pad uart1_rx 0x0: Select uart1_rx 0x3: Select usbb2_ulpitll_data6 0x7: Select safe_mode_core50 0x6: Select gpio3_74	RW	0x7

Table 18-523. Register Call Summary for Register CONTROL_CORE_PAD0_UART1_RX_PAD1_UART1_RTS

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-524. CONTROL_CORE_PAD0_HSI2_CAREADY_PAD1_HSI2_ACREADY

Address Offset	0x0000 00A8		
Physical Address	0x4A00 28A8 0x4A00 28A8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hsi2_caready and hsi2_acready Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSI2_ACREADY_WAKEUPEVENT	HSI2_ACREADY_WAKEUPENABLE	RESERVED					HSI2_ACREADY_INPUTENABLE	RESERVED		HSI2_ACREADY_PWRDOWN	HSI2_ACREADY_PULLTYPESELECT	HSI2_ACREADY_PULLUDENABLE	HSI2_ACREADY_MUXMODE			HSI2_CAREADY_WAKEUPEVENT	HSI2_CAREADY_WAKEUPENABLE	RESERVED					HSI2_CAREADY_INPUTENABLE	RESERVED		HSI2_CAREADY_PWRDOWN	HSI2_CAREADY_PULLTYPESELECT	HSI2_CAREADY_PULLUDENABLE	HSI2_CAREADY_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HSI2_ACREADY_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	HSI2_ACREADY_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	HSI2_ACREADY_INPUTENABLE	Input enable value for pad hsi2_acready 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	HSI2_ACREADY_PWRDOWN	Power Down setting for pad hsi2_acready 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HSI2_ACREADY_PULLTYPESELECT	Pull-Up/Down selection for pad hsi2_acready 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	HSI2_ACREADY_PULLUDENABLE	Pull-Up/Down enable for pad hsi2_acready 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	HSI2_ACREADY_MUXMODE	Functional multiplexing selection for pad hsi2_acready 0x0: Select hsi2_acready 0x3: Select usbb1_ulpiphy_nxt 0x7: Select safe_mode_core53 0x4: Select gpmc_ncs1 0x6: Select gpio3_77	RW	0x7
15	HSI2_CAREADY_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HSI2_CAREADY_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HSI2_CAREADY_INPUTENABLE	Input enable value for pad hsi2_caready 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	HSI2_CAREADY_PWRDOWN	Power Down setting for pad hsi2_caready 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HSI2_CAREADY_PULLTYPESELECT	Pull-Up/Down selection for pad hsi2_caready 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	HSI2_CAREADY_PULLUDENABLE	Pull-Up/Down enable for pad hsi2_caready 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HSI2_CAREADY_MUXMODE	Functional multiplexing selection for pad hsi2_caready 0x0: Select hsi2_caready 0x3: Select usbb1_ulpiphy_clk 0x7: Select safe_mode_core52 0x4: Select gpmc_wait1 0x6: Select gpio3_76	RW	0x7

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Table 18-525. Register Call Summary for Register CONTROL_CORE_PAD0_HSI2_CAREADY_PAD1_HSI2_ACREADY

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-526. CONTROL_CORE_PAD0_HSI2_CAWAKE_PAD1_HSI2_ACWAKE

Address Offset	0x0000 00AC		
Physical Address	0x4A00 28AC 0x4A00 28AC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hsi2_cawake and hsi2_acwake Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSI2_ACWAKE_WAKEUPEVENT	HSI2_ACWAKE_WAKEUPENABLE	RESERVED					HSI2_ACWAKE_INPUTENABLE	RESERVED		HSI2_ACWAKE_PWRDOWN	HSI2_ACWAKE_PULLTYPESELECT	HSI2_ACWAKE_PULLUDENABLE	HSI2_ACWAKE_MUXMODE			HSI2_CAWAKE_WAKEUPEVENT	HSI2_CAWAKE_WAKEUPENABLE	RESERVED					HSI2_CAWAKE_INPUTENABLE	RESERVED		HSI2_CAWAKE_PWRDOWN	HSI2_CAWAKE_PULLTYPESELECT	HSI2_CAWAKE_PULLUDENABLE	HSI2_CAWAKE_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HSI2_ACWAKE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	HSI2_ACWAKE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	HSI2_ACWAKE_INPUTENABLE	Input enable value for pad hsi2_acwake 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	HSI2_ACWAKE_PWRDOWN	Power Down setting for pad hsi2_acwake 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HSI2_ACWAKE_PULLTYPESELECT	Pull-Up/Down selection for pad hsi2_acwake 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	HSI2_ACWAKE_PULLUDENABLE	Pull-Up/Down enable for pad hsi2_acwake 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	HSI2_ACWAKE_MUXMODE	Functional multiplexing selection for pad hsi2_acwake 0x0: Select hsi2_acwake 0x3: Select usbb1_ulpiphy_stp 0x7: Select safe_mode_core55 0x4: Select gpmc_a25 0x6: Select gpio3_79	RW	0x7
15	HSI2_CAWAKE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HSI2_CAWAKE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HSI2_CAWAKE_INPUTENABLE	Input enable value for pad hsi2_cawake 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	HSI2_CAWAKE_PWRDOWN	Power Down setting for pad hsi2_cawake 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HSI2_CAWAKE_PULLTYPESELECT	Pull-Up/Down selection for pad hsi2_cawake 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	HSI2_CAWAKE_PULLUDENABLE	Pull-Up/Down enable for pad hsi2_cawake 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HSI2_CAWAKE_MUXMODE	Functional multiplexing selection for pad hsi2_cawake 0x0: Select hsi2_cawake 0x3: Select usbb1_ulpiphy_dir 0x7: Select safe_mode_core54 0x4: Select gpmc_a24 0x6: Select gpio3_78	RW	0x7

Table 18-527. Register Call Summary for Register CONTROL_CORE_PAD0_HSI2_CAWAKE_PAD1_HSI2_ACWAKE

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-528. CONTROL_CORE_PAD0_HSI2_CAFLAG_PAD1_HSI2_CADATA

Address Offset	0x0000 00B0		
Physical Address	0x4A00 28B0 0x4A00 28B0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hsi2_caflag and hsi2_cadata Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSI2_CADATA_WAKEUPEVENT	HSI2_CADATA_WAKEUPENABLE	RESERVED					HSI2_CADATA_INPUTENABLE	RESERVED		HSI2_CADATA_PWRDOWN	HSI2_CADATA_PULLTYPESELECT	HSI2_CADATA_PULLUDENABLE	HSI2_CADATA_MUXMODE			HSI2_CAFLAG_WAKEUPEVENT	HSI2_CAFLAG_WAKEUPENABLE	RESERVED					HSI2_CAFLAG_INPUTENABLE	RESERVED		HSI2_CAFLAG_PWRDOWN	HSI2_CAFLAG_PULLTYPESELECT	HSI2_CAFLAG_PULLUDENABLE	HSI2_CAFLAG_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HSI2_CADATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	HSI2_CADATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	HSI2_CADATA_INPUTENABLE	Input enable value for pad hsi2_cadata 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	HSI2_CADATA_PWRDOWN	Power Down setting for pad hsi2_cadata 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HSI2_CADATA_PULLTYPESELECT	Pull-Up/Down selection for pad hsi2_cadata 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	HSI2_CADATA_PULLUDENABLE	Pull-Up/Down enable for pad hsi2_cadata 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	HSI2_CADATA_MUXMODE	Functional multiplexing selection for pad hsi2_cadata 0x0: Select hsi2_cadata 0x3: Select usbb1_ulpiphy_data1 0x7: Select safe_mode_core57 0x4: Select gpmc_ncs2 0x6: Select gpio3_81	RW	0x7
15	HSI2_CAFLAG_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HSI2_CAFLAG_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HSI2_CAFLAG_INPUTENABLE	Input enable value for pad hsi2_caflag 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
7:6	RESERVED		R	0x0
5	HSI2_CAFLAG_PWRDOWN	Power Down setting for pad hsi2_caflag 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HSI2_CAFLAG_PULLTYPESELECT	Pull-Up/Down selection for pad hsi2_caflag 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	HSI2_CAFLAG_PULLUDENABLE	Pull-Up/Down enable for pad hsi2_caflag 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HSI2_CAFLAG_MUXMODE	Functional multiplexing selection for pad hsi2_caflag 0x0: Select hsi2_caflag 0x3: Select usbb1_ulpiphy_data0 0x7: Select safe_mode_core56 0x4: Select gpmc_wait2 0x6: Select gpio3_80	RW	0x7

Table 18-529. Register Call Summary for Register CONTROL_CORE_PAD0_HSI2_CAFLAG_PAD1_HSI2_CADATA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-530. CONTROL_CORE_PAD0_HSI2_ACFLAG_PAD1_HSI2_ACDATA

Address Offset	0x0000 00B4		
Physical Address	0x4A00 28B4 0x4A00 28B4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hsi2_acflag and hsi2_acdata Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSI2_ACDATA_WAKEUPEVENT	HSI2_ACDATA_WAKEUPENABLE	RESERVED					HSI2_ACDATA_INPUTENABLE	RESERVED		HSI2_ACDATA_PWRDOWN	HSI2_ACDATA_PULLTYPESELECT	HSI2_ACDATA_PULLUDENABLE	HSI2_ACDATA_MUXMODE			HSI2_ACFLAG_WAKEUPEVENT	HSI2_ACFLAG_WAKEUPENABLE	RESERVED					HSI2_ACFLAG_INPUTENABLE	RESERVED		HSI2_ACFLAG_PWRDOWN	HSI2_ACFLAG_PULLTYPESELECT	HSI2_ACFLAG_PULLUDENABLE	HSI2_ACFLAG_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HSI2_ACDATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	HSI2_ACDATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	HSI2_ACDATA_INPUTENABLE	Input enable value for pad hsi2_acdata 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	HSI2_ACDATA_PWRDOWN	Power Down setting for pad hsi2_acdata 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HSI2_ACDATA_PULLTYPESELECT	Pull-Up/Down selection for pad hsi2_acdata 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	HSI2_ACDATA_PULLUDENABLE	Pull-Up/Down enable for pad hsi2_acdata 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	HSI2_ACDATA_MUXMODE	Functional multiplexing selection for pad hsi2_acdata 0x0: Select hsi2_acdata 0x3: Select usbb1_ulpiphy_data3 0x7: Select safe_mode_core59 0x4: Select gpmc_ncs4 0x6: Select gpio3_83	RW	0x7
15	HSI2_ACFLAG_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HSI2_ACFLAG_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HSI2_ACFLAG_INPUTENABLE	Input enable value for pad hsi2_acflag 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	HSI2_ACFLAG_PWRDOWN	Power Down setting for pad hsi2_acflag 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HSI2_ACFLAG_PULLTYPESELECT	Pull-Up/Down selection for pad hsi2_acflag 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	HSI2_ACFLAG_PULLUDENABLE	Pull-Up/Down enable for pad hsi2_acflag 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HSI2_ACFLAG_MUXMODE	Functional multiplexing selection for pad hsi2_acflag 0x0: Select hsi2_acflag 0x3: Select usbb1_ulpiphy_data2 0x7: Select safe_mode_core58 0x4: Select gpmc_ncs3 0x6: Select gpio3_82	RW	0x7

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Table 18-531. Register Call Summary for Register CONTROL_CORE_PAD0_HSI2_ACFLAG_PAD1_HSI2_ACDATA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-532. CONTROL_CORE_PAD0_UART2_RTS_PAD1_UART2_CTS

Address Offset	0x0000 00B8		
Physical Address	0x4A00 28B8 0x4A00 28B8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart2_rts and uart2_cts Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART2_CTS_WAKEUPEVENT	UART2_CTS_WAKEUPENABLE	RESERVED					UART2_CTS_INPUTENABLE	RESERVED		UART2_CTS_PWRDOWN	UART2_CTS_PULLTYPESELECT	UART2_CTS_PULLUDENABLE	UART2_CTS_MUXMODE			UART2_RTS_WAKEUPEVENT	UART2_RTS_WAKEUPENABLE	RESERVED					UART2_RTS_INPUTENABLE	RESERVED		UART2_RTS_PWRDOWN	UART2_RTS_PULLTYPESELECT	UART2_RTS_PULLUDENABLE	UART2_RTS_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART2_CTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART2_CTS_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	UART2_CTS_INPUTENABLE	Input enable value for pad uart2_cts 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	UART2_CTS_PWRDOWN	Power Down setting for pad uart2_cts 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	UART2_CTS_PULLTYPESELECT	Pull-Up/Down selection for pad uart2_cts 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART2_CTS_PULLUDENABLE	Pull-Up/Down enable for pad uart2_cts 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	UART2_CTS_MUXMODE	Functional multiplexing selection for pad uart2_cts 0x6: Select gpio3_85 0x1: Select mcspi3_cs0 0x7: Select safe_mode_core61 0x0: Select uart2_cts 0x4: Select gpmc_noe_nre 0x5: Select hw_dbg17 0x3: Select usbb1_ulpiphy_data5	RW	0x4
15	UART2_RTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART2_RTS_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	UART2_RTS_INPUTENABLE	Input enable value for pad uart2_rts 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	UART2_RTS_PWRDOWN	Power Down setting for pad uart2_rts 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART2_RTS_PULLTYPESELECT	Pull-Up/Down selection for pad uart2_rts 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	UART2_RTS_PULLUDENABLE	Pull-Up/Down enable for pad uart2_rts 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART2_RTS_MUXMODE	Functional multiplexing selection for pad uart2_rts 0x6: Select gpio3_84 0x1: Select mcspi3_somi 0x7: Select safe_mode_core60 0x0: Select uart2_rts 0x4: Select gpmc_nwe 0x5: Select hw_dbg16 0x3: Select usbb1_ulpiphy_data4	RW	0x4

Table 18-533. Register Call Summary for Register CONTROL_CORE_PAD0_UART2_RTS_PAD1_UART2_CTS

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [3]

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Table 18-534. CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX

Address Offset	0x0000 00BC		
Physical Address	0x4A00 28BC 0x4A00 28BC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart2_rx and uart2_tx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART2_TX_WAKEUPEVENT	UART2_TX_WAKEUPENABLE	RESERVED					UART2_TX_INPUTENABLE	RESERVED	UART2_TX_GLITCHGOBBLER	UART2_TX_PWRDOWN	UART2_TX_PULLTYPESELECT	UART2_TX_PULLUDENABLE	UART2_TX_MUXMODE			UART2_RX_WAKEUPEVENT	UART2_RX_WAKEUPENABLE	RESERVED					UART2_RX_INPUTENABLE	RESERVED			UART2_RX_PWRDOWN	UART2_RX_PULLTYPESELECT	UART2_RX_PULLUDENABLE	UART2_RX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART2_TX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART2_TX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	UART2_TX_INPUTENABLE	Input enable value for pad uart2_tx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23	RESERVED		R	0
22	UART2_TX_GLITCHGOBBLER	Glitch Gobbler setting for pad uart2_tx 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
21	UART2_TX_PWRDOWN	Power Down setting for pad uart2_tx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	UART2_TX_PULLTYPESELECT	Pull-Up/Down selection for pad uart2_tx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART2_TX_PULLUDENABLE	Pull-Up/Down enable for pad uart2_tx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	UART2_TX_MUXMODE	Functional multiplexing selection for pad uart2_tx 0x6: Select gpio3_87 0x1: Select mcspi3_clk 0x7: Select safe_mode_core63 0x0: Select uart2_tx 0x4: Select gpmc_ncs6 0x5: Select hw_dbg19 0x3: Select usbb1_ulpiphy_data7	RW	0x7
15	UART2_RX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART2_RX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	UART2_RX_INPUTENABLE	Input enable value for pad uart2_rx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	UART2_RX_PWRDOWN	Power Down setting for pad uart2_rx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART2_RX_PULLTYPESELECT	Pull-Up/Down selection for pad uart2_rx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	UART2_RX_PULLUDENABLE	Pull-Up/Down enable for pad uart2_rx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART2_RX_MUXMODE	Functional multiplexing selection for pad uart2_rx 0x6: Select gpio3_86 0x1: Select mcspi3_simo 0x7: Select safe_mode_core62 0x0: Select uart2_rx 0x4: Select gpmc_ncs5 0x5: Select hw_dbg18 0x3: Select usbb1_ulpiphy_data6	RW	0x7

Table 18-535. Register Call Summary for Register CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [3]

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Table 18-536. CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBB1_HSIC_DATA

Address Offset	0x0000 00C0		
Physical Address	0x4A00 28C0 0x4A00 28C0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads usbb1_hsic_strobe and usbb1_hsic_data Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB1_HSIC_DATA_WAKEUPEVENT	USBB1_HSIC_DATA_WAKEUPENABLE	RESERVED					USBB1_HSIC_DATA_INPUTENABLE	RESERVED					USBB1_HSIC_DATA_MUXMODE			USBB1_HSIC_STROBE_WAKEUPEVENT	USBB1_HSIC_STROBE_WAKEUPENABLE	RESERVED					USBB1_HSIC_STROBE_INPUTENABLE	RESERVED					USBB1_HSIC_STROBE_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	USBB1_HSIC_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	USBB1_HSIC_DATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	USBB1_HSIC_DATA_INPUTENABLE	Input enable value for pad usbb1_hsic_data 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:19	RESERVED		R	0x00
18:16	USBB1_HSIC_DATA_MUXMODE	Functional multiplexing selection for pad usbb1_hsic_data 0x0: Select usbb1_hsic_data 0x7: Select safe_mode_core65 0x6: Select gpio3_93	RW	0x7
15	USBB1_HSIC_STROBE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	USBB1_HSIC_STROBE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	USBB1_HSIC_STROBE_INPUTENABLE	Input enable value for pad usbb1_hsic_strobe 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:3	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
2:0	USBB1_HSIC_STROBE_MUXMODE	Functional multiplexing selection for pad usbb1_hsic_strobe 0x0: Select usbb1_hsic_strobe 0x7: Select safe_mode_core64 0x6: Select gpio3_92	RW	0x7

Table 18-537. Register Call Summary for Register CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBB1_HSIC_DATA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-538. CONTROL_CORE_PAD0_USBB2_HSIC_STROBE_PAD1_USBB2_HSIC_DATA

Address Offset	0x0000 00C4		
Physical Address	0x4A00 28C4 0x4A00 28C4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads usbb2_hsic_strobe and usbb2_hsic_data Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB2_HSIC_DATA_WAKEUPEVENT	USBB2_HSIC_DATA_WAKEUPENABLE	RESERVED					USBB2_HSIC_DATA_INPUTENABLE	RESERVED					USBB2_HSIC_DATA_MUXMODE			USBB2_HSIC_STROBE_WAKEUPEVENT	USBB2_HSIC_STROBE_WAKEUPENABLE	RESERVED					USBB2_HSIC_STROBE_INPUTENABLE	RESERVED					USBB2_HSIC_STROBE_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	USBB2_HSIC_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	USBB2_HSIC_DATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	USBB2_HSIC_DATA_INPUTENABLE	Input enable value for pad usbb2_hsic_data 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:19	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
18:16	USBB2_HSIC_DATA_MUXMODE	Functional multiplexing selection for pad usbb2_hsic_data 0x0: Select usbb2_hsic_data 0x7: Select safe_mode_core67 0x6: Select gpio3_95	RW	0x7
15	USBB2_HSIC_STROBE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	USBB2_HSIC_STROBE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	USBB2_HSIC_STROBE_INPUTENABLE	Input enable value for pad usbb2_hsic_strobe 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:3	RESERVED		R	0x00
2:0	USBB2_HSIC_STROBE_MUXMODE	Functional multiplexing selection for pad usbb2_hsic_strobe 0x0: Select usbb2_hsic_strobe 0x7: Select safe_mode_core66 0x6: Select gpio3_94	RW	0x7

Table 18-539. Register Call Summary for Register CONTROL_CORE_PAD0_USBB2_HSIC_STROBE_PAD1_USBB2_HSIC_DATA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-540. CONTROL_CORE_PAD0_TIMER10_PWM_EVT_PAD1_DSIPORTA_TE0

Address Offset	0x0000 00C8		
Physical Address	0x4A00 28C8 0x4A00 28C8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads timer10_pwm_evt and dsiporta_te0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSIPORTA_TE0_WAKEUPEVENT	DSIPORTA_TE0_WAKEUPENABLE	RESERVED					DSIPORTA_TE0_INPUTENABLE	RESERVED		DSIPORTA_TE0_PWRDOWN	DSIPORTA_TE0_PULLTYPESELECT	DSIPORTA_TE0_PULLUDENABLE	DSIPORTA_TE0_MUXMODE			TIMER10_PWM_EVT_WAKEUPEVENT	TIMER10_PWM_EVT_WAKEUPENABLE	RESERVED					TIMER10_PWM_EVT_INPUTENABLE	RESERVED		TIMER10_PWM_EVT_PWRDOWN	TIMER10_PWM_EVT_PULLTYPESELECT	TIMER10_PWM_EVT_PULLUDENABLE	TIMER10_PWM_EVT_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	DSIPORTA_TE0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	DSIPORTA_TE0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	DSIPORTA_TE0_INPUTENABLE	Input enable value for pad dsiporta_te0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTA_TE0_PWRDOWN	Power Down setting for pad dsiporta_te0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	DSIPORTA_TE0_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_te0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTA_TE0_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_te0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	DSIPORTA_TE0_MUXMODE	Functional multiplexing selection for pad dsiporta_te0 0x0: Select dsiporta_te0 0x7: Select safe_mode_core69 0x6: Select gpio6_189	RW	0x7
15	TIMER10_PWM_EVT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	TIMER10_PWM_EVT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	TIMER10_PWM_EVT_INPUTENABLE	Input enable value for pad timer10_pwm_evt 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	TIMER10_PWM_EVT_PWRDOWN	Power Down setting for pad timer10_pwm_evt 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	TIMER10_PWM_EVT_PULLTYPESELECT	Pull-Up/Down selection for pad timer10_pwm_evt 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	TIMER10_PWM_EVT_PULLUDENABLE	Pull-Up/Down enable for pad timer10_pwm_evt 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	TIMER10_PWM_EVT_MUXMODE	Functional multiplexing selection for pad timer10_pwm_evt 0x0: Select timer10_pwm_evt 0x7: Select safe_mode_core68 0x6: Select gpio6_188	RW	0x7

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Table 18-541. Register Call Summary for Register CONTROL_CORE_PAD0_TIMER10_PWM_EVT_PAD1_DSIPORTA_TE0

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-542. CONTROL_CORE_PAD0_DSIPORTA_LANE0X_PAD1_DSIPORTA_LANE0Y

Address Offset	0x0000 00CC		
Physical Address	0x4A00 28CC 0x4A00 28CC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiporta_lane0x and dsiporta_lane0y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSIPORTA_LANE0Y_INPUTENABLE	RESERVED		DSIPORTA_LANE0Y_PWRDOWN	DSIPORTA_LANE0Y_PULLTYPESELECT	DSIPORTA_LANE0Y_PULLUDENABLE	RESERVED											DSIPORTA_LANE0X_INPUTENABLE	RESERVED			DSIPORTA_LANE0X_PWRDOWN	DSIPORTA_LANE0X_PULLTYPESELECT	DSIPORTA_LANE0X_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTA_LANE0Y_INPUTENABLE	Input enable value for pad dsiporta_lane0y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTA_LANE0Y_PWRDOWN	Power Down setting for pad dsiporta_lane0y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	DSIPORTA_LANE0Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane0y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTA_LANE0Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane0y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTA_LANE0X_INPUTENABLE	Input enable value for pad dsiporta_lane0x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	DSIPORTA_LANE0X_PWRDOWN	Power Down setting for pad dsiporta_lane0x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTA_LANE0X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane0x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTA_LANE0X_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane0x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-543. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTA_LANE0X_PAD1_DSIPORTA_LANE0Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-544. CONTROL_CORE_PAD0_DSIPORTA_LANE1X_PAD1_DSIPORTA_LANE1Y

Address Offset	0x0000 00D0		
Physical Address	0x4A00 28D0 0x4A00 28D0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiporta_lane1x and dsiporta_lane1y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSIPORTA_LANE1Y_INPUTENABLE	RESERVED		DSIPORTA_LANE1Y_PWRDOWN	DSIPORTA_LANE1Y_PULLTYPESELECT	DSIPORTA_LANE1Y_PULLUDENABLE	RESERVED										DSIPORTA_LANE1X_INPUTENABLE	RESERVED			DSIPORTA_LANE1X_PWRDOWN	DSIPORTA_LANE1X_PULLTYPESELECT	DSIPORTA_LANE1X_PULLUDENABLE	RESERVED			

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTA_LANE1Y_INPUTENABLE	Input enable value for pad dsiporta_lane1y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTA_LANE1Y_PWRDOWN	Power Down setting for pad dsiporta_lane1y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0

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Bits	Field Name	Description	Type	Reset
20	DSIPORTA_LANE1Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane1y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTA_LANE1Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane1y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTA_LANE1X_INPUTENABLE	Input enable value for pad dsiporta_lane1x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	DSIPORTA_LANE1X_PWRDOWN	Power Down setting for pad dsiporta_lane1x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTA_LANE1X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane1x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTA_LANE1X_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane1x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-545. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTA_LANE1X_PAD1_DSIPORTA_LANE1Y

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-546. CONTROL_CORE_PAD0_DSIPORTA_LANE2X_PAD1_DSIPORTA_LANE2Y

Address Offset	0x0000 00D4		
Physical Address	0x4A00 28D4 0x4A00 28D4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiporta_lane2x and dsiporta_lane2y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSIPORTA_LANE2Y_INPUTENABLE	RESERVED		DSIPORTA_LANE2Y_PWRDOWN	DSIPORTA_LANE2Y_PULLTYPESELECT	DSIPORTA_LANE2Y_PULLUDENABLE	RESERVED			DSIPORTA_LANE2X_INPUTENABLE	RESERVED							RESERVED		DSIPORTA_LANE2X_PWRDOWN	DSIPORTA_LANE2X_PULLTYPESELECT	DSIPORTA_LANE2X_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTA_LANE2Y_INPUTENABLE	Input enable value for pad dsiporta_lane2y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTA_LANE2Y_PWRDOWN	Power Down setting for pad dsiporta_lane2y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	DSIPORTA_LANE2Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane2y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTA_LANE2Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane2y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTA_LANE2X_INPUTENABLE	Input enable value for pad dsiporta_lane2x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	DSIPORTA_LANE2X_PWRDOWN	Power Down setting for pad dsiporta_lane2x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTA_LANE2X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane2x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTA_LANE2X_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane2x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-547. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTA_LANE2X_PAD1_DSIPORTA_LANE2Y

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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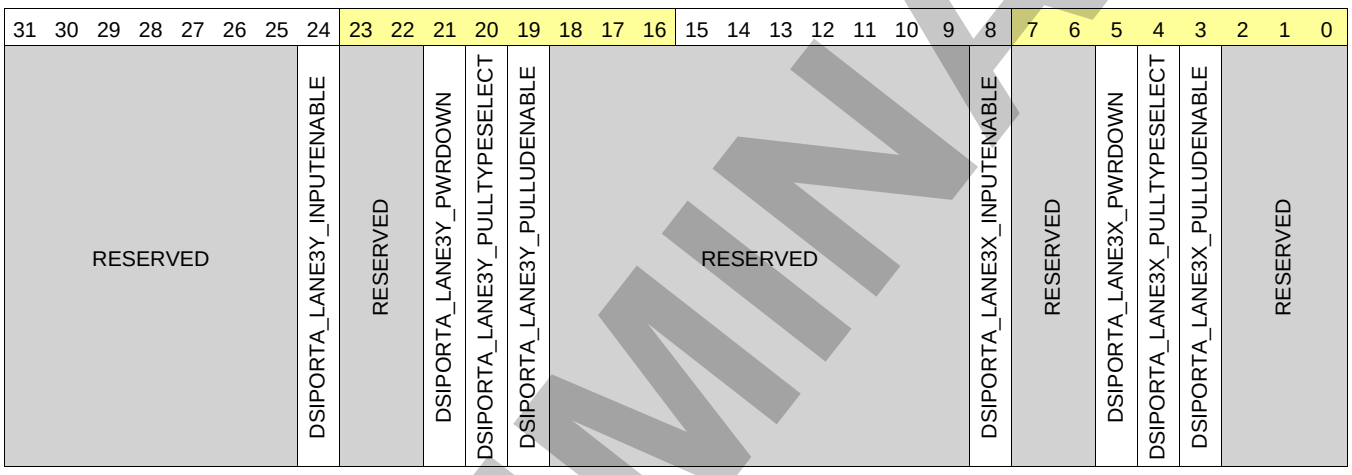
Table 18-547. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTA_LANE2X_PAD1_DSIPORTA_LANE2Y (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-548. CONTROL_CORE_PAD0_DSIPORTA_LANE3X_PAD1_DSIPORTA_LANE3Y

Address Offset	0x0000 00D8		
Physical Address	0x4A00 28D8 0x4A00 28D8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiporta_lane3x and dsiporta_lane3y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTA_LANE3Y_INPUTENABLE	Input enable value for pad dsiporta_lane3y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTA_LANE3Y_PWRDOWN	Power Down setting for pad dsiporta_lane3y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	DSIPORTA_LANE3Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane3y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTA_LANE3Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane3y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTA_LANE3X_INPUTENABLE	Input enable value for pad dsiporta_lane3x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	DSIPORTA_LANE3X_PWRDOWN	Power Down setting for pad dsiporta_lane3x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTA_LANE3X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane3x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTA_LANE3X_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane3x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-549. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTA_LANE3X_PAD1_DSIPORTA_LANE3Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-550. CONTROL_CORE_PAD0_DSIPORTA_LANE4X_PAD1_DSIPORTA_LANE4Y

Address Offset	0x0000 00DC		
Physical Address	0x4A00 28DC 0x4A00 28DC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiporta_lane4x and dsiporta_lane4y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSIPORTA_LANE4Y_INPUTENABLE	RESERVED		DSIPORTA_LANE4Y_PWRDOWN	DSIPORTA_LANE4Y_PULLTYPESELECT	DSIPORTA_LANE4Y_PULLUDENABLE	RESERVED										DSIPORTA_LANE4X_INPUTENABLE	RESERVED			DSIPORTA_LANE4X_PWRDOWN	DSIPORTA_LANE4X_PULLTYPESELECT	DSIPORTA_LANE4X_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTA_LANE4Y_INPUTENABLE	Input enable value for pad dsiporta_lane4y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTA_LANE4Y_PWRDOWN	Power Down setting for pad dsiporta_lane4y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0

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Bits	Field Name	Description	Type	Reset
20	DSIPORTA_LANE4Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane4y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTA_LANE4Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane4y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTA_LANE4X_INPUTENABLE	Input enable value for pad dsiporta_lane4x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	DSIPORTA_LANE4X_PWRDOWN	Power Down setting for pad dsiporta_lane4x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTA_LANE4X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiporta_lane4x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTA_LANE4X_PULLUDENABLE	Pull-Up/Down enable for pad dsiporta_lane4x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-551. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTA_LANE4X_PAD1_DSIPORTA_LANE4Y

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-552. CONTROL_CORE_PAD0_DSIPORTC_LANE0X_PAD1_DSIPORTC_LANE0Y

Address Offset	0x0000 00E0		
Physical Address	0x4A00 28E0 0x4A00 28E0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiportc_lane0x and dsiportc_lane0y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSIPORTC_LANE0Y_INPUTENABLE	RESERVED		DSIPORTC_LANE0Y_PWRDOWN	DSIPORTC_LANE0Y_PULLTYPESELECT	DSIPORTC_LANE0Y_PULLUDENABLE	RESERVED										DSIPORTC_LANE0X_INPUTENABLE	RESERVED			DSIPORTC_LANE0X_PWRDOWN	DSIPORTC_LANE0X_PULLTYPESELECT	DSIPORTC_LANE0X_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTC_LANE0Y_INPUTENABLE	Input enable value for pad dsiportc_lane0y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTC_LANE0Y_PWRDOWN	Power Down setting for pad dsiportc_lane0y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	DSIPORTC_LANE0Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane0y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTC_LANE0Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane0y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTC_LANE0X_INPUTENABLE	Input enable value for pad dsiportc_lane0x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	DSIPORTC_LANE0X_PWRDOWN	Power Down setting for pad dsiportc_lane0x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTC_LANE0X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane0x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTC_LANE0X_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane0x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-553. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTC_LANE0X_PAD1_DSIPORTC_LANE0Y

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-553. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTC_LANE0X_PAD1_DSIPORTC_LANE0Y (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-554. CONTROL_CORE_PAD0_DSIPORTC_LANE1X_PAD1_DSIPORTC_LANE1Y

Address Offset	0x0000 00E4		
Physical Address	0x4A00 28E4 0x4A00 28E4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiportc_lane1x and dsiportc_lane1y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSIPORTC_LANE1Y_INPUTENABLE	RESERVED		DSIPORTC_LANE1Y_PWRDOWN	DSIPORTC_LANE1Y_PULLTYPESELECT	DSIPORTC_LANE1Y_PULLUDENABLE	RESERVED										DSIPORTC_LANE1X_INPUTENABLE	RESERVED				DSIPORTC_LANE1X_PWRDOWN	DSIPORTC_LANE1X_PULLTYPESELECT	DSIPORTC_LANE1X_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTC_LANE1Y_INPUTENABLE	Input enable value for pad dsiportc_lane1y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTC_LANE1Y_PWRDOWN	Power Down setting for pad dsiportc_lane1y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	DSIPORTC_LANE1Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane1y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTC_LANE1Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane1y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTC_LANE1X_INPUTENABLE	Input enable value for pad dsiportc_lane1x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	DSIPORTC_LANE1X_PWRDOWN	Power Down setting for pad dsiportc_lane1x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTC_LANE1X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane1x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTC_LANE1X_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane1x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-555. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTC_LANE1X_PAD1_DSIPORTC_LANE1Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-556. CONTROL_CORE_PAD0_DSIPORTC_LANE2X_PAD1_DSIPORTC_LANE2Y

Address Offset	0x0000 00E8		
Physical Address	0x4A00 28E8 0x4A00 28E8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiportc_lane2x and dsiportc_lane2y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSIPORTC_LANE2Y_INPUTENABLE	RESERVED		DSIPORTC_LANE2Y_PWRDOWN	DSIPORTC_LANE2Y_PULLTYPESELECT	DSIPORTC_LANE2Y_PULLUDENABLE	RESERVED										DSIPORTC_LANE2X_INPUTENABLE	RESERVED		DSIPORTC_LANE2X_PWRDOWN	DSIPORTC_LANE2X_PULLTYPESELECT	DSIPORTC_LANE2X_PULLUDENABLE	RESERVED			

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTC_LANE2Y_INPUTENABLE	Input enable value for pad dsiportc_lane2y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTC_LANE2Y_PWRDOWN	Power Down setting for pad dsiportc_lane2y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0

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Bits	Field Name	Description	Type	Reset
20	DSIPORTC_LANE2Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane2y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTC_LANE2Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane2y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTC_LANE2X_INPUTENABLE	Input enable value for pad dsiportc_lane2x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	DSIPORTC_LANE2X_PWRDOWN	Power Down setting for pad dsiportc_lane2x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTC_LANE2X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane2x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTC_LANE2X_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane2x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-557. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTC_LANE2X_PAD1_DSIPORTC_LANE2Y

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-558. CONTROL_CORE_PAD0_DSIPORTC_LANE3X_PAD1_DSIPORTC_LANE3Y

Address Offset	0x0000 00EC		
Physical Address	0x4A00 28EC 0x4A00 28EC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiportc_lane3x and dsiportc_lane3y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSIPORTC_LANE3Y_INPUTENABLE	RESERVED		DSIPORTC_LANE3Y_PWRDOWN	DSIPORTC_LANE3Y_PULLTYPESELECT	DSIPORTC_LANE3Y_PULLUDENABLE	RESERVED										DSIPORTC_LANE3X_INPUTENABLE	RESERVED			DSIPORTC_LANE3X_PWRDOWN	DSIPORTC_LANE3X_PULLTYPESELECT	DSIPORTC_LANE3X_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTC_LANE3Y_INPUTENABLE	Input enable value for pad dsiportc_lane3y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTC_LANE3Y_PWRDOWN	Power Down setting for pad dsiportc_lane3y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	DSIPORTC_LANE3Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane3y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTC_LANE3Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane3y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTC_LANE3X_INPUTENABLE	Input enable value for pad dsiportc_lane3x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	DSIPORTC_LANE3X_PWRDOWN	Power Down setting for pad dsiportc_lane3x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTC_LANE3X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane3x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTC_LANE3X_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane3x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-559. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTC_LANE3X_PAD1_DSIPORTC_LANE3Y

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-559. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTC_LANE3X_PAD1_DSIPORTC_LANE3Y (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-560. CONTROL_CORE_PAD0_DSIPORTC_LANE4X_PAD1_DSIPORTC_LANE4Y

Address Offset	0x0000 00F0		
Physical Address	0x4A00 28F0 0x4A00 28F0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiportc_lane4x and dsiportc_lane4y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							DSIPORTC_LANE4Y_INPUTENABLE	RESERVED		DSIPORTC_LANE4Y_PWRDOWN	DSIPORTC_LANE4Y_PULLTYPESELECT	DSIPORTC_LANE4Y_PULLUDENABLE	RESERVED			DSIPORTC_LANE4X_INPUTENABLE	RESERVED							DSIPORTC_LANE4X_PWRDOWN	DSIPORTC_LANE4X_PULLTYPESELECT	DSIPORTC_LANE4X_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	DSIPORTC_LANE4Y_INPUTENABLE	Input enable value for pad dsiportc_lane4y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DSIPORTC_LANE4Y_PWRDOWN	Power Down setting for pad dsiportc_lane4y 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	DSIPORTC_LANE4Y_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane4y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	DSIPORTC_LANE4Y_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane4y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:9	RESERVED		R	0x0
8	DSIPORTC_LANE4X_INPUTENABLE	Input enable value for pad dsiportc_lane4x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	DSIPORTC_LANE4X_PWRDOWN	Power Down setting for pad dsiportc_lane4x 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTC_LANE4X_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_lane4x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTC_LANE4X_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_lane4x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-561. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTC_LANE4X_PAD1_DSIPORTC_LANE4Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-562. CONTROL_CORE_PAD0_DSIPORTC_TE0_PAD1_TIMER9_PWM_EVT

Address Offset	0x0000 00F4		
Physical Address	0x4A00 28F4 0x4A00 28F4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads dsiportc_te0 and timer9_pwm_evt Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER9_PWM_EVT_WAKEUPEVENT	TIMER9_PWM_EVT_WAKEUPENABLE	RESERVED					TIMER9_PWM_EVT_INPUTENABLE	RESERVED		TIMER9_PWM_EVT_PWRDOWN	TIMER9_PWM_EVT_PULLTYPESELECT	TIMER9_PWM_EVT_PULLUDENABLE	TIMER9_PWM_EVT_MUXMODE			DSIPORTC_TE0_WAKEUPEVENT	DSIPORTC_TE0_WAKEUPENABLE	RESERVED					DSIPORTC_TE0_INPUTENABLE	RESERVED		DSIPORTC_TE0_PWRDOWN	DSIPORTC_TE0_PULLTYPESELECT	DSIPORTC_TE0_PULLUDENABLE	DSIPORTC_TE0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	TIMER9_PWM_EVT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	TIMER9_PWM_EVT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
24	TIMER9_PWM_EVT_INPUTENABLE	Input enable value for pad timer9_pwm_evt 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	TIMER9_PWM_EVT_PWRDOWN	Power Down setting for pad timer9_pwm_evt 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	TIMER9_PWM_EVT_PULLTYPESELECT	Pull-Up/Down selection for pad timer9_pwm_evt 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	TIMER9_PWM_EVT_PULLUDENABLE	Pull-Up/Down enable for pad timer9_pwm_evt 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	TIMER9_PWM_EVT_MUXMODE	Functional multiplexing selection for pad timer9_pwm_evt 0x0: Select timer9_pwm_evt 0x1: Select sync_sof_clk 0x2: Select sync_usof_itp_clk 0x7: Select safe_mode_core70 0x6: Select gpio6_190	RW	0x7
15	DSIPORTC_TE0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	DSIPORTC_TE0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	DSIPORTC_TE0_INPUTENABLE	Input enable value for pad dsiportc_te0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	DSIPORTC_TE0_PWRDOWN	Power Down setting for pad dsiportc_te0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DSIPORTC_TE0_PULLTYPESELECT	Pull-Up/Down selection for pad dsiportc_te0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	DSIPORTC_TE0_PULLUDENABLE	Pull-Up/Down enable for pad dsiportc_te0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	DSIPORTC_TE0_MUXMODE	Functional multiplexing selection for pad dsiportc_te0 0x0: Select dsiportc_te0 0x7: Select safe_mode_core71 0x6: Select gpio6_191	RW	0x7

Table 18-563. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTC_TE0_PAD1_TIMER9_PWM_EVT

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-563. Register Call Summary for Register CONTROL_CORE_PAD0_DSIPORTC_TE0_PAD1_TIMER9_PWM_EVT (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-564. CONTROL_CORE_PAD0_I2C4_SCL_PAD1_I2C4_SDA

Address Offset	0x0000 00F8		
Physical Address	0x4A00 28F8 0x4A00 28F8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads i2c4_scl and i2c4_sda Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C4_SDA_WAKEUPEVENT	I2C4_SDA_WAKEUPENABLE	RESERVED					I2C4_SDA_INPUTENABLE	RESERVED		I2C4_SDA_PWRDOWN	I2C4_SDA_PULLTYPESELECT	I2C4_SDA_PULLUDENABLE	I2C4_SDA_MUXMODE			I2C4_SCL_WAKEUPEVENT	I2C4_SCL_WAKEUPENABLE	RESERVED					I2C4_SCL_INPUTENABLE	RESERVED		I2C4_SCL_PWRDOWN	I2C4_SCL_PULLTYPESELECT	I2C4_SCL_PULLUDENABLE	I2C4_SCL_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	I2C4_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	I2C4_SDA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	I2C4_SDA_INPUTENABLE	Input enable value for pad i2c4_sda 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	I2C4_SDA_PWRDOWN	Power Down setting for pad i2c4_sda 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	I2C4_SDA_PULLTYPESELECT	Pull-Up/Down selection for pad i2c4_sda 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	I2C4_SDA_PULLUDENABLE	Pull-Up/Down enable for pad i2c4_sda 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	I2C4_SDA_MUXMODE	Functional multiplexing selection for pad i2c4_sda 0x0: Select i2c4_sda 0x1: Select jtagtapext_rtck 0x7: Select safe_mode_core105 0x6: Select gpio7_201	RW	0x7
15	I2C4_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	I2C4_SCL_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	I2C4_SCL_INPUTENABLE	Input enable value for pad i2c4_scl 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	I2C4_SCL_PWRDOWN	Power Down setting for pad i2c4_scl 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	I2C4_SCL_PULLTYPESELECT	Pull-Up/Down selection for pad i2c4_scl 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	I2C4_SCL_PULLUDENABLE	Pull-Up/Down enable for pad i2c4_scl 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	I2C4_SCL_MUXMODE	Functional multiplexing selection for pad i2c4_scl 0x0: Select i2c4_scl 0x1: Select jtagtapext_tdi 0x7: Select safe_mode_core104 0x6: Select gpio7_200	RW	0x7

Table 18-565. Register Call Summary for Register CONTROL_CORE_PAD0_I2C4_SCL_PAD1_I2C4_SDA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-566. CONTROL_CORE_PAD0_MCSPI2_CLK_PAD1_MCSPI2_SIMO

Address Offset	0x0000 00FC		
Physical Address	0x4A00 28FC 0x4A00 28FC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads mcspi2_clk and mcspi2_simo Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI2_SIMO_WAKEUPEVENT	MCSPI2_SIMO_WAKEUPENABLE	RESERVED					MCSPI2_SIMO_INPUTENABLE	RESERVED		MCSPI2_SIMO_PWRDOWN	MCSPI2_SIMO_PULLTYPESELECT	MCSPI2_SIMO_PULLUDENABLE	MCSPI2_SIMO_MUXMODE			MCSPI2_CLK_WAKEUPEVENT	MCSPI2_CLK_WAKEUPENABLE	RESERVED					MCSPI2_CLK_INPUTENABLE	RESERVED	MCSPI2_CLK_GLITCHGOBBLER	MCSPI2_CLK_PWRDOWN	MCSPI2_CLK_PULLTYPESELECT	MCSPI2_CLK_PULLUDENABLE	MCSPI2_CLK_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	MCSPI2_SIMO_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	MCSPI2_SIMO_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	MCSPI2_SIMO_INPUTENABLE	Input enable value for pad mcspi2_simo 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	MCSPI2_SIMO_PWRDOWN	Power Down setting for pad mcspi2_simo 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	MCSPI2_SIMO_PULLTYPESELECT	Pull-Up/Down selection for pad mcspi2_simo 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	MCSPI2_SIMO_PULLUDENABLE	Pull-Up/Down enable for pad mcspi2_simo 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	MCSPI2_SIMO_MUXMODE	Functional multiplexing selection for pad mcspi2_simo 0x0: Select mcspi2_simo 0X1: Select jtagtapext_tmsc 0x6: Select gpio7_198 0x7: Select safe_mode_core102 0x5: Select hw_dbg20	RW	0x7
15	MCSPI2_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	MCSPI2_CLK_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	MCSPI2_CLK_INPUTENABLE	Input enable value for pad mcspi2_clk 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
7	RESERVED		R	0
6	MCSPI2_CLK_GLITCHGOBBLER	Glitch Gobbler setting for pad mcspi2_clk 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
5	MCSPI2_CLK_PWRDOWN	Power Down setting for pad mcspi2_clk 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	MCSPI2_CLK_PULLTYPESELECT	Pull-Up/Down selection for pad mcspi2_clk 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	MCSPI2_CLK_PULLUDENABLE	Pull-Up/Down enable for pad mcspi2_clk 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	MCSPI2_CLK_MUXMODE	Functional multiplexing selection for pad mcspi2_clk 0x0: Select mcspi2_clk 0x1: Select jtagtapext_tck 0x7: Select safe_mode_core101 0x6: Select gpio7_197	RW	0x7

Table 18-567. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI2_CLK_PAD1_MCSPI2_SIMO

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [3]

Table 18-568. CONTROL_CORE_PAD0_MCSPI2_SOMI_PAD1_MCSPI2_CS0

Address Offset	0x0000 0100		
Physical Address	0x4A00 2900 0x4A00 2900	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads mcspi2_somi and mcspi2_cs0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI2_CS0_WAKEUPEVENT	MCSPI2_CS0_WAKEUPENABLE	RESERVED					MCSPI2_CS0_INPUTENABLE	RESERVED		MCSPI2_CS0_PWRDOWN	MCSPI2_CS0_PULLTYPESELECT	MCSPI2_CS0_PULLUDENABLE	MCSPI2_CS0_MUXMODE			MCSPI2_SOMI_WAKEUPEVENT	MCSPI2_SOMI_WAKEUPENABLE	RESERVED					MCSPI2_SOMI_INPUTENABLE	RESERVED		MCSPI2_SOMI_PWRDOWN	MCSPI2_SOMI_PULLTYPESELECT	MCSPI2_SOMI_PULLUDENABLE	MCSPI2_SOMI_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	MCSPI2_CS0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	MCSPI2_CS0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	MCSPI2_CS0_INPUTENABLE	Input enable value for pad mcspi2_cs0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	MCSPI2_CS0_PWRDOWN	Power Down setting for pad mcspi2_cs0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	MCSPI2_CS0_PULLTYPESELECT	Pull-Up/Down selection for pad mcspi2_cs0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	MCSPI2_CS0_PULLUDENABLE	Pull-Up/Down enable for pad mcspi2_cs0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	MCSPI2_CS0_MUXMODE	Functional multiplexing selection for pad mcspi2_cs0 0x0: Select mcspi2_cs0 0x1: Select jtagtapext_ntrst 0x3: Select dispc_fid 0x7: Select safe_mode_core100 0x6: Select gpio7_196	RW	0x7
15	MCSPI2_SOMI_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	MCSPI2_SOMI_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	MCSPI2_SOMI_INPUTENABLE	Input enable value for pad mcspi2_somi 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	MCSPI2_SOMI_PWRDOWN	Power Down setting for pad mcspi2_somi 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	MCSPI2_SOMI_PULLTYPESELECT	Pull-Up/Down selection for pad mcspi2_somi 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	MCSPI2_SOMI_PULLUDENABLE	Pull-Up/Down enable for pad mcspi2_somi 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	MCSPI2_SOMI_MUXMODE	Functional multiplexing selection for pad mcspi2_somi 0x0: Select mcspi2_somi 0x1: Select jtagtapext_tdo 0x6: Select gpio7_199 0x7: Select safe_mode_core103 0x5: Select hw_dbg21	RW	0x7

Table 18-569. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI2_SOMI_PAD1_MCSPI2_CS0

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1] • Observability Signals Muxed on Pads in the CORE Power Domain: [2]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [3]

Table 18-570. CONTROL_CORE_PAD0_RFBI_DATA15_PAD1_RFBI_DATA14

Address Offset	0x0000 0104		
Physical Address	0x4A00 2904 0x4A00 2904	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_data15 and rfbi_data14 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_DATA14_WAKEUPEVENT	RFBI_DATA14_WAKEUPENABLE	RESERVED					RFBI_DATA14_INPUTENABLE	RESERVED		RFBI_DATA14_PWRDOWN	RFBI_DATA14_PULLTYPESELECT	RFBI_DATA14_PULLUDENABLE	RFBI_DATA14_MUXMODE			RFBI_DATA15_WAKEUPEVENT	RFBI_DATA15_WAKEUPENABLE	RESERVED					RFBI_DATA15_INPUTENABLE	RESERVED		RFBI_DATA15_PWRDOWN	RFBI_DATA15_PULLTYPESELECT	RFBI_DATA15_PULLUDENABLE	RFBI_DATA15_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_DATA14_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_DATA14_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_DATA14_INPUTENABLE	Input enable value for pad rfbi_data14 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	RFBI_DATA14_PWRDOWN	Power Down setting for pad rfbi_data14 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_DATA14_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data14 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_DATA14_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data14 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	RFBI_DATA14_MUXMODE	Functional multiplexing selection for pad rfbi_data14 0x6: Select gpio6_180 0x7: Select safe_mode_core82 0x0: Select rfbi_data14 0x4: Select kbd_col7 0x5: Select drm_emu18 0x3: Select dispc_data14	RW	0x7
15	RFBI_DATA15_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_DATA15_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_DATA15_INPUTENABLE	Input enable value for pad rfbi_data15 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	RFBI_DATA15_PWRDOWN	Power Down setting for pad rfbi_data15 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_DATA15_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data15 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_DATA15_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data15 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RFBI_DATA15_MUXMODE	Functional multiplexing selection for pad rfbi_data15 0x6: Select gpio6_181 0x1: Select mcspi2_cs1 0x7: Select safe_mode_core83 0x0: Select rfbi_data15 0x4: Select kbd_col6 0x5: Select drm_emu19 0x3: Select dispc_data15	RW	0x7

Table 18-571. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA15_PAD1_RFBI_DATA14

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-571. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA15_PAD1_RFBI_DATA14 (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-572. CONTROL_CORE_PAD0_RFBI_DATA13_PAD1_RFBI_DATA12

Address Offset	0x0000 0108		
Physical Address	0x4A00 2908 0x4A00 2908	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_data13 and rfbi_data12 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_DATA12_WAKEUPEVENT	RFBI_DATA12_WAKEUPENABLE	RESERVED					RFBI_DATA12_INPUTENABLE	RESERVED		RFBI_DATA12_PWRDOWN	RFBI_DATA12_PULLTYPESELECT	RFBI_DATA12_PULLUDENABLE	RFBI_DATA12_MUXMODE			RFBI_DATA13_WAKEUPEVENT	RFBI_DATA13_WAKEUPENABLE	RESERVED					RFBI_DATA13_INPUTENABLE	RESERVED		RFBI_DATA13_PWRDOWN	RFBI_DATA13_PULLTYPESELECT	RFBI_DATA13_PULLUDENABLE	RFBI_DATA13_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_DATA12_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_DATA12_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_DATA12_INPUTENABLE	Input enable value for pad rfbi_data12 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	RFBI_DATA12_PWRDOWN	Power Down setting for pad rfbi_data12 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_DATA12_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data12 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_DATA12_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data12 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	RFBI_DATA12_MUXMODE	Functional multiplexing selection for pad rfbi_data12 0x6: Select gpio6_178 0x7: Select safe_mode_core80 0x0: Select rfbi_data12 0x4: Select kbd_row6 0x5: Select drm_emu16 0x3: Select dispc_data12	RW	0x7
15	RFBI_DATA13_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_DATA13_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_DATA13_INPUTENABLE	Input enable value for pad rfbi_data13 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	RFBI_DATA13_PWRDOWN	Power Down setting for pad rfbi_data13 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_DATA13_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data13 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_DATA13_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data13 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RFBI_DATA13_MUXMODE	Functional multiplexing selection for pad rfbi_data13 0x6: Select gpio6_179 0x7: Select safe_mode_core81 0x0: Select rfbi_data13 0x4: Select kbd_col8 0x5: Select drm_emu17 0x3: Select dispc_data13	RW	0x7

Table 18-573. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA13_PAD1_RFBI_DATA12

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-574. CONTROL_CORE_PAD0_RFBI_DATA11_PAD1_RFBI_DATA10

Address Offset	0x0000 010C		
Physical Address	0x4A00 290C 0x4A00 290C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_data11 and rfbi_data10 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_DATA10_WAKEUPEVENT	RFBI_DATA10_WAKEUPENABLE	RESERVED					RFBI_DATA10_INPUTENABLE	RESERVED		RFBI_DATA10_PWRDOWN	RFBI_DATA10_PULLTYPESELECT	RFBI_DATA10_PULLUDENABLE	RFBI_DATA10_MUXMODE			RFBI_DATA11_WAKEUPEVENT	RFBI_DATA11_WAKEUPENABLE	RESERVED					RFBI_DATA11_INPUTENABLE	RESERVED		RFBI_DATA11_PWRDOWN	RFBI_DATA11_PULLTYPESELECT	RFBI_DATA11_PULLUDENABLE	RFBI_DATA11_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_DATA10_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_DATA10_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_DATA10_INPUTENABLE	Input enable value for pad rfbi_data10 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	RFBI_DATA10_PWRDOWN	Power Down setting for pad rfbi_data10 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_DATA10_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data10 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_DATA10_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data10 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	RFBI_DATA10_MUXMODE	Functional multiplexing selection for pad rfbi_data10 0x6: Select gpio6_176 0x7: Select safe_mode_core78 0x0: Select rfbi_data10 0x4: Select kbd_row8 0x5: Select drm_emu14 0x3: Select dispc_data10	RW	0x7
15	RFBI_DATA11_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_DATA11_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_DATA11_INPUTENABLE	Input enable value for pad rfbi_data11 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
7:6	RESERVED		R	0x0
5	RFBI_DATA11_PWRDOWN	Power Down setting for pad rfbi_data11 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_DATA11_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data11 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_DATA11_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data11 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RFBI_DATA11_MUXMODE	Functional multiplexing selection for pad rfbi_data11 0x6: Select gpio6_177 0x7: Select safe_mode_core79 0x0: Select rfbi_data11 0x4: Select kbd_row7 0x5: Select drm_emu15 0x3: Select dispc_data11	RW	0x7

Table 18-575. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA11_PAD1_RFBI_DATA10

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-576. CONTROL_CORE_PAD0_RFBI_DATA9_PAD1_RFBI_DATA8

Address Offset	0x0000 0110		
Physical Address	0x4A00 2910 0x4A00 2910	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_data9 and rfbi_data8 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_DATA8_WAKEUPEVENT	RFBI_DATA8_WAKEUPENABLE	RESERVED					RFBI_DATA8_INPUTENABLE	RESERVED		RFBI_DATA8_PWRDOWN	RFBI_DATA8_PULLTYPESELECT	RFBI_DATA8_PULLUDENABLE	RFBI_DATA8_MUXMODE			RFBI_DATA9_WAKEUPEVENT	RFBI_DATA9_WAKEUPENABLE	RESERVED					RFBI_DATA9_INPUTENABLE	RESERVED		RFBI_DATA9_PWRDOWN	RFBI_DATA9_PULLTYPESELECT	RFBI_DATA9_PULLUDENABLE	RFBI_DATA9_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_DATA8_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
30	RFBI_DATA8_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_DATA8_INPUTENABLE	Input enable value for pad rfbi_data8 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	RFBI_DATA8_PWRDOWN	Power Down setting for pad rfbi_data8 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_DATA8_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data8 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_DATA8_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data8 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	RFBI_DATA8_MUXMODE	Functional multiplexing selection for pad rfbi_data8 0x6: Select gpio6_174 0x7: Select safe_mode_core76 0x0: Select rfbi_data8 0x4: Select kbd_col3 0x5: Select drm_emu12 0x3: Select dispc_data8	RW	0x7
15	RFBI_DATA9_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_DATA9_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_DATA9_INPUTENABLE	Input enable value for pad rfbi_data9 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	RFBI_DATA9_PWRDOWN	Power Down setting for pad rfbi_data9 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_DATA9_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data9 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_DATA9_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data9 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	RFBI_DATA9_MUXMODE	Functional multiplexing selection for pad rfbi_data9 0x6: Select gpio6_175 0x7: Select safe_mode_core77 0x0: Select rfbi_data9 0x4: Select kbd_row3 0x5: Select drm_emu13 0x3: Select dispc_data9	RW	0x7

Table 18-577. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA9_PAD1_RFBI_DATA8

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-578. CONTROL_CORE_PAD0_RFBI_DATA7_PAD1_RFBI_DATA6

Address Offset	0x0000 0114		
Physical Address	0x4A00 2914 0x4A00 2914	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_data7 and rfbi_data6 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_DATA6_WAKEUPEVENT	RFBI_DATA6_WAKEUPENABLE	RESERVED					RFBI_DATA6_INPUTENABLE	RESERVED		RFBI_DATA6_PWRDOWN	RFBI_DATA6_PULLTYPESELECT	RFBI_DATA6_PULLUDENABLE	RFBI_DATA6_MUXMODE			RFBI_DATA7_WAKEUPEVENT	RFBI_DATA7_WAKEUPENABLE	RESERVED					RFBI_DATA7_INPUTENABLE	RESERVED		RFBI_DATA7_PWRDOWN	RFBI_DATA7_PULLTYPESELECT	RFBI_DATA7_PULLUDENABLE	RFBI_DATA7_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_DATA6_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_DATA6_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_DATA6_INPUTENABLE	Input enable value for pad rfbi_data6 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	RFBI_DATA6_PWRDOWN	Power Down setting for pad rfbi_data6 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_DATA6_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data6 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_DATA6_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data6 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	RFBI_DATA6_MUXMODE	Functional multiplexing selection for pad rfbi_data6 0x0: Select rfbi_data6 0x6: Select gpio6_172 0x3: Select dispc_data6 0x4: Select jtagtapext_tdo 0x7: Select safe_mode_core96 0x5: Select drm_emu10	RW	0x7
15	RFBI_DATA7_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_DATA7_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_DATA7_INPUTENABLE	Input enable value for pad rfbi_data7 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	RFBI_DATA7_PWRDOWN	Power Down setting for pad rfbi_data7 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_DATA7_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data7 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_DATA7_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data7 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RFBI_DATA7_MUXMODE	Functional multiplexing selection for pad rfbi_data7 0x0: Select rfbi_data7 0x6: Select gpio6_173 0x3: Select dispc_data7 0x4: Select jtagtapext_tdi 0x7: Select safe_mode_core97 0x5: Select drm_emu11	RW	0x7

Table 18-579. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA7_PAD1_RFBI_DATA6

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-579. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA7_PAD1_RFBI_DATA6 (continued)

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- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-580. CONTROL_CORE_PAD0_RFBI_DATA5_PAD1_RFBI_DATA4

Address Offset	0x0000 0118		
Physical Address	0x4A00 2918 0x4A00 2918	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_data5 and rfbi_data4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_DATA4_WAKEUPEVENT	RFBI_DATA4_WAKEUPENABLE	RESERVED					RFBI_DATA4_INPUTENABLE	RESERVED		RFBI_DATA4_PWRDOWN	RFBI_DATA4_PULLTYPESELECT	RFBI_DATA4_PULLUDENABLE	RFBI_DATA4_MUXMODE			RFBI_DATA5_WAKEUPEVENT	RFBI_DATA5_WAKEUPENABLE	RESERVED					RFBI_DATA5_INPUTENABLE	RESERVED		RFBI_DATA5_PWRDOWN	RFBI_DATA5_PULLTYPESELECT	RFBI_DATA5_PULLUDENABLE	RFBI_DATA5_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_DATA4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_DATA4_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_DATA4_INPUTENABLE	Input enable value for pad rfbi_data4 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	RFBI_DATA4_PWRDOWN	Power Down setting for pad rfbi_data4 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_DATA4_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data4 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_DATA4_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data4 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	RFBI_DATA4_MUXMODE	Functional multiplexing selection for pad rfbi_data4 0x0: Select rfbi_data4 0x6: Select gpio6_170 0x3: Select dispc_data4 0x4: Select jtagtapext_tck 0x7: Select safe_mode_core94 0x5: Select drm_emu8	RW	0x7
15	RFBI_DATA5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_DATA5_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_DATA5_INPUTENABLE	Input enable value for pad rfbi_data5 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	RFBI_DATA5_PWRDOWN	Power Down setting for pad rfbi_data5 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_DATA5_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data5 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_DATA5_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data5 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RFBI_DATA5_MUXMODE	Functional multiplexing selection for pad rfbi_data5 0x0: Select rfbi_data5 0x6: Select gpio6_171 0x3: Select dispc_data5 0x4: Select jtagtapext_tmsc 0x7: Select safe_mode_core95 0x5: Select drm_emu9	RW	0x7

Table 18-581. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA5_PAD1_RFBI_DATA4

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-582. CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2

Address Offset	0x0000 011C		
Physical Address	0x4A00 291C 0x4A00 291C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_data3 and rfbi_data2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_DATA2_WAKEUPEVENT	RFBI_DATA2_WAKEUPENABLE	RESERVED					RFBI_DATA2_INPUTENABLE	RESERVED		RFBI_DATA2_PWRDOWN	RFBI_DATA2_PULLTYPESELECT	RFBI_DATA2_PULLUDENABLE	RFBI_DATA2_MUXMODE			RFBI_DATA3_WAKEUPEVENT	RFBI_DATA3_WAKEUPENABLE	RESERVED					RFBI_DATA3_INPUTENABLE	RESERVED		RFBI_DATA3_PWRDOWN	RFBI_DATA3_PULLTYPESELECT	RFBI_DATA3_PULLUDENABLE	RFBI_DATA3_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_DATA2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_DATA2_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_DATA2_INPUTENABLE	Input enable value for pad rfbi_data2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	RFBI_DATA2_PWRDOWN	Power Down setting for pad rfbi_data2 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_DATA2_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_DATA2_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	RFBI_DATA2_MUXMODE	Functional multiplexing selection for pad rfbi_data2 0x6: Select gpio6_168 0x7: Select safe_mode_core92 0x0: Select rfbi_data2 0x4: Select uart3_tx_irtx 0x5: Select drm_emu6 0x3: Select dispc_data2	RW	0x7
15	RFBI_DATA3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_DATA3_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_DATA3_INPUTENABLE	Input enable value for pad rfbi_data3 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
7:6	RESERVED		R	0x0
5	RFBI_DATA3_PWRDOWN	Power Down setting for pad rfbi_data3 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_DATA3_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_DATA3_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RFBI_DATA3_MUXMODE	Functional multiplexing selection for pad rfbi_data3 0x0: Select rfbi_data3 0x6: Select gpio6_169 0x3: Select dispc_data3 0x4: Select jtagtapext_ntrst 0x7: Select safe_mode_core93 0x5: Select drm_emu7	RW	0x7

Table 18-583. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Programming Guide • Pad Configuration Programming Points: [2] [3] [4] [5] [6] [7]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [8]

Table 18-584. CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0

Address Offset	0x0000 0120		
Physical Address	0x4A00 2920 0x4A00 2920	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_data1 and rfbi_data0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_DATA0_WAKEUPEVENT	RFBI_DATA0_WAKEUPENABLE	RESERVED					RFBI_DATA0_INPUTENABLE	RESERVED		RFBI_DATA0_PWRDOWN	RFBI_DATA0_PULLTYPESELECT	RFBI_DATA0_PULLUDENABLE	RFBI_DATA0_MUXMODE			RFBI_DATA1_WAKEUPEVENT	RFBI_DATA1_WAKEUPENABLE	RESERVED					RFBI_DATA1_INPUTENABLE	RESERVED		RFBI_DATA1_PWRDOWN	RFBI_DATA1_PULLTYPESELECT	RFBI_DATA1_PULLUDENABLE	RFBI_DATA1_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	RFBI_DATA0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_DATA0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_DATA0_INPUTENABLE	Input enable value for pad rfbi_data0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	RFBI_DATA0_PWRDOWN	Power Down setting for pad rfbi_data0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_DATA0_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_DATA0_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	RFBI_DATA0_MUXMODE	Functional multiplexing selection for pad rfbi_data0 0x0: Select rfbi_data0 0x6: Select gpio6_166 0x3: Select dispc_data0 0x4: Select jtagtapext_rtck 0x7: Select safe_mode_core90 0x5: Select drm_emu4	RW	0x7
15	RFBI_DATA1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_DATA1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_DATA1_INPUTENABLE	Input enable value for pad rfbi_data1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	RFBI_DATA1_PWRDOWN	Power Down setting for pad rfbi_data1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_DATA1_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_data1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_DATA1_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_data1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	RFBI_DATA1_MUXMODE	Functional multiplexing selection for pad rfbi_data1 0x6: Select gpio6_167 0x7: Select safe_mode_core91 0x0: Select rfbi_data1 0x4: Select uart3_rx_irrx 0x5: Select drm_emu5 0x3: Select dispc_data1	RW	0x7

Table 18-585. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Programming Guide • Pad Configuration Programming Points: [2] [3] [4] [5] [6] [7]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [8]

Table 18-586. CONTROL_CORE_PAD0_RFBI_WE_PAD1_RFBI_CS0

Address Offset	0x0000 0124		
Physical Address	0x4A00 2924 0x4A00 2924	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_we and rfbi_cs0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_CS0_WAKEUPEVENT	RFBI_CS0_WAKEUPENABLE	RESERVED					RFBI_CS0_INPUTENABLE	RESERVED		RFBI_CS0_PWRDOWN	RFBI_CS0_PULLTYPESELECT	RFBI_CS0_PULLUDENABLE	RFBI_CS0_MUXMODE			RFBI_WE_WAKEUPEVENT	RFBI_WE_WAKEUPENABLE	RESERVED					RFBI_WE_INPUTENABLE	RESERVED		RFBI_WE_PWRDOWN	RFBI_WE_PULLTYPESELECT	RFBI_WE_PULLUDENABLE	RFBI_WE_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_CS0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_CS0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_CS0_INPUTENABLE	Input enable value for pad rfbi_cs0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	RFBI_CS0_PWRDOWN	Power Down setting for pad rfbi_cs0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_CS0_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_cs0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_CS0_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_cs0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	RFBI_CS0_MUXMODE	Functional multiplexing selection for pad rfbi_cs0 0x0: Select rfbi_cs0 0x6: Select gpio6_163 0x3: Select dispc_hsync 0x7: Select safe_mode_core98 0x5: Select drm_emu3	RW	0x7
15	RFBI_WE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_WE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_WE_INPUTENABLE	Input enable value for pad rfbi_we 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	RFBI_WE_PWRDOWN	Power Down setting for pad rfbi_we 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_WE_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_we 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_WE_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_we 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RFBI_WE_MUXMODE	Functional multiplexing selection for pad rfbi_we 0x0: Select rfbi_we 0x6: Select gpio6_162 0x3: Select dispc_vsync 0x7: Select safe_mode_core99 0x5: Select drm_emu2	RW	0x7

Table 18-587. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_WE_PAD1_RFBI_CS0

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-588. CONTROL_CORE_PAD0_RFBI_A0_PAD1_RFBI_RE

Address Offset	0x0000 0128		
Physical Address	0x4A00 2928 0x4A00 2928	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_a0 and rfbi_re Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_RE_WAKEUPEVENT	RFBI_RE_WAKEUPENABLE	RESERVED					RFBI_RE_INPUTENABLE	RESERVED		RFBI_RE_PWRDOWN	RFBI_RE_PULLTYPESELECT	RFBI_RE_PULLUDENABLE	RFBI_RE_MUXMODE			RFBI_A0_WAKEUPEVENT	RFBI_A0_WAKEUPENABLE	RESERVED					RFBI_A0_INPUTENABLE	RESERVED		RFBI_A0_PWRDOWN	RFBI_A0_PULLTYPESELECT	RFBI_A0_PULLUDENABLE	RFBI_A0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_RE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_RE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_RE_INPUTENABLE	Input enable value for pad rfbi_re 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	RFBI_RE_PWRDOWN	Power Down setting for pad rfbi_re 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_RE_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_re 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_RE_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_re 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	RFBI_RE_MUXMODE	Functional multiplexing selection for pad rfbi_re 0x0: Select rfbi_re 0x3: Select dispc_pclk 0x7: Select safe_mode_core74 0x4: Select kbd_col4 0x6: Select gpio6_164	RW	0x7
15	RFBI_A0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	RFBI_A0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	RFBI_A0_INPUTENABLE	Input enable value for pad rfbi_a0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	RFBI_A0_PWRDOWN	Power Down setting for pad rfbi_a0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_A0_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_a0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_A0_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_a0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RFBI_A0_MUXMODE	Functional multiplexing selection for pad rfbi_a0 0x0: Select rfbi_a0 0x3: Select dispc_de 0x7: Select safe_mode_core75 0x4: Select kbd_row4 0x6: Select gpio6_165	RW	0x7

Table 18-589. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_A0_PAD1_RFBI_RE

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-590. CONTROL_CORE_PAD0_RFBI_HSYNC0_PAD1_RFBI_TE_VSYNC0

Address Offset	0x0000 012C		
Physical Address	0x4A00 292C 0x4A00 292C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads rfbi_hsync0 and rfbi_te_vsync0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_TE_VSYNC0_WAKEUPEVENT	RFBI_TE_VSYNC0_WAKEUPENABLE	RESERVED					RFBI_TE_VSYNC0_INPUTENABLE	RESERVED		RFBI_TE_VSYNC0_PWRDOWN	RFBI_TE_VSYNC0_PULLTYPESELECT	RFBI_TE_VSYNC0_PULLUDENABLE	RFBI_TE_VSYNC0_MUXMODE			RFBI_HSYNC0_WAKEUPEVENT	RFBI_HSYNC0_WAKEUPENABLE	RESERVED					RFBI_HSYNC0_INPUTENABLE	RESERVED		RFBI_HSYNC0_PWRDOWN	RFBI_HSYNC0_PULLTYPESELECT	RFBI_HSYNC0_PULLUDENABLE	RFBI_HSYNC0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	RFBI_TE_VSYNC0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	RFBI_TE_VSYNC0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	RFBI_TE_VSYNC0_INPUTENABLE	Input enable value for pad rfbi_te_vsync0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	RFBI_TE_VSYNC0_PWRDOWN	Power Down setting for pad rfbi_te_vsync0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	RFBI_TE_VSYNC0_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_te_vsync0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	RFBI_TE_VSYNC0_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_te_vsync0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	RFBI_TE_VSYNC0_MUXMODE	Functional multiplexing selection for pad rfbi_te_vsync0 0x6: Select gpio6_161 0x7: Select safe_mode_core73 0x0: Select rfbi_te_vsync0 0x4: Select kbd_row5 0x5: Select jtag_sel 0x3: Select dispc_data16	RW	0x7
15	RFBI_HSYNC0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	RFBI_HSYNC0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
8	RFBI_HSYNC0_INPUTENABLE	Input enable value for pad rfbi_hsync0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	RFBI_HSYNC0_PWRDOWN	Power Down setting for pad rfbi_hsync0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	RFBI_HSYNC0_PULLTYPESELECT	Pull-Up/Down selection for pad rfbi_hsync0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	RFBI_HSYNC0_PULLUDENABLE	Pull-Up/Down enable for pad rfbi_hsync0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RFBI_HSYNC0_MUXMODE	Functional multiplexing selection for pad rfbi_hsync0 0x0: Select rfbi_hsync0 0x3: Select dispc_data17 0x7: Select safe_mode_core72 0x4: Select kbd_col5 0x6: Select gpio6_160	RW	0x7

Table 18-591. Register Call Summary for Register CONTROL_CORE_PAD0_RFBI_HSYNC0_PAD1_RFBI_TE_VSYNC0

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-592. CONTROL_CORE_PAD0_GPIO6_182_PAD1_GPIO6_183

Address Offset	0x0000 0130		
Physical Address	0x4A00 2930 0x4A00 2930	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads gpio6_182 and gpio6_183 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO6_183_WAKEUPEVENT	GPIO6_183_WAKEUPENABLE	RESERVED					GPIO6_183_INPUTENABLE	RESERVED		GPIO6_183_PWRDOWN	GPIO6_183_PULLTYPESELECT	GPIO6_183_PULLUDENABLE	GPIO6_183_MUXMODE			GPIO6_182_WAKEUPEVENT	GPIO6_182_WAKEUPENABLE	RESERVED					GPIO6_182_INPUTENABLE	RESERVED		GPIO6_182_PWRDOWN	GPIO6_182_PULLTYPESELECT	GPIO6_182_PULLUDENABLE	GPIO6_182_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	GPIO6_183_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPIO6_183_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	GPIO6_183_INPUTENABLE	Input enable value for pad gpio6_183 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	GPIO6_183_PWRDOWN	Power Down setting for pad gpio6_183 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	GPIO6_183_PULLTYPESELECT	Pull-Up/Down selection for pad gpio6_183 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	GPIO6_183_PULLUDENABLE	Pull-Up/Down enable for pad gpio6_183 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPIO6_183_MUXMODE	Functional multiplexing selection for pad gpio6_183 0x0: Select gpio6_183 0x3: Select dispc_data19 0x7: Select safe_mode_core85 0x4: Select kbd_col1 0x6: Select gpio6_183	RW	0x7
15	GPIO6_182_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPIO6_182_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	GPIO6_182_INPUTENABLE	Input enable value for pad gpio6_182 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	GPIO6_182_PWRDOWN	Power Down setting for pad gpio6_182 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	GPIO6_182_PULLTYPESELECT	Pull-Up/Down selection for pad gpio6_182 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPIO6_182_PULLUDENABLE	Pull-Up/Down enable for pad gpio6_182 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	GPIO6_182_MUXMODE	Functional multiplexing selection for pad gpio6_182 0x0: Select gpio6_182 0x3: Select dispc_data18 0x7: Select safe_mode_core84 0x4: Select kbd_col0 0x6: Select gpio6_182	RW	0x7

Table 18-593. Register Call Summary for Register CONTROL_CORE_PAD0_GPIO6_182_PAD1_GPIO6_183

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-594. CONTROL_CORE_PAD0_GPIO6_184_PAD1_GPIO6_185

Address Offset	0x0000 0134		
Physical Address	0x4A00 2934 0x4A00 2934	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads gpio6_184 and gpio6_185 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO6_185_WAKEUPEVENT	GPIO6_185_WAKEUPENABLE	RESERVED					GPIO6_185_INPUTENABLE	RESERVED		GPIO6_185_PWRDOWN	GPIO6_185_PULLTYPESELECT	GPIO6_185_PULLUDENABLE	GPIO6_185_MUXMODE			GPIO6_184_WAKEUPEVENT	GPIO6_184_WAKEUPENABLE	RESERVED					GPIO6_184_INPUTENABLE	RESERVED		GPIO6_184_PWRDOWN	GPIO6_184_PULLTYPESELECT	GPIO6_184_PULLUDENABLE	GPIO6_184_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPIO6_185_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPIO6_185_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	GPIO6_185_INPUTENABLE	Input enable value for pad gpio6_185 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	GPIO6_185_PWRDOWN	Power Down setting for pad gpio6_185 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0

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Bits	Field Name	Description	Type	Reset
20	GPIO6_185_PULLTYPESELECT	Pull-Up/Down selection for pad gpio6_185 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	GPIO6_185_PULLUDENABLE	Pull-Up/Down enable for pad gpio6_185 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPIO6_185_MUXMODE	Functional multiplexing selection for pad gpio6_185 0x6: Select gpio6_185 0x7: Select safe_mode_core87 0x0: Select gpio6_185 0x4: Select kbd_row0 0x5: Select hw_dbg23 0x3: Select dispc_data21	RW	0x7
15	GPIO6_184_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPIO6_184_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	GPIO6_184_INPUTENABLE	Input enable value for pad gpio6_184 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	GPIO6_184_PWRDOWN	Power Down setting for pad gpio6_184 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	GPIO6_184_PULLTYPESELECT	Pull-Up/Down selection for pad gpio6_184 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPIO6_184_PULLUDENABLE	Pull-Up/Down enable for pad gpio6_184 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPIO6_184_MUXMODE	Functional multiplexing selection for pad gpio6_184 0x6: Select gpio6_184 0x7: Select safe_mode_core86 0x0: Select gpio6_184 0x4: Select kbd_col2 0x5: Select hw_dbg22 0x3: Select dispc_data20	RW	0x7

Table 18-595. Register Call Summary for Register CONTROL_CORE_PAD0_GPIO6_184_PAD1_GPIO6_185

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [3]

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Table 18-596. CONTROL_CORE_PAD0_GPIO6_186_PAD1_GPIO6_187

Address Offset	0x0000 0138		
Physical Address	0x4A00 2938 0x4A00 2938	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads gpio6_186 and gpio6_187 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO6_187_WAKEUPEVENT	GPIO6_187_WAKEUPENABLE	RESERVED					GPIO6_187_INPUTENABLE	RESERVED		GPIO6_187_PWRDOWN	GPIO6_187_PULLTYPESELECT	GPIO6_187_PULLUDENABLE	GPIO6_187_MUXMODE			GPIO6_186_WAKEUPEVENT	GPIO6_186_WAKEUPENABLE	RESERVED					GPIO6_186_INPUTENABLE	RESERVED		GPIO6_186_PWRDOWN	GPIO6_186_PULLTYPESELECT	GPIO6_186_PULLUDENABLE	GPIO6_186_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPIO6_187_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPIO6_187_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	GPIO6_187_INPUTENABLE	Input enable value for pad gpio6_187 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	GPIO6_187_PWRDOWN	Power Down setting for pad gpio6_187 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	GPIO6_187_PULLTYPESELECT	Pull-Up/Down selection for pad gpio6_187 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	GPIO6_187_PULLUDENABLE	Pull-Up/Down enable for pad gpio6_187 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPIO6_187_MUXMODE	Functional multiplexing selection for pad gpio6_187 0x6: Select gpio6_187 0x7: Select safe_mode_core89 0x0: Select gpio6_187 0x4: Select kbd_row2 0x5: Select hw_dbg25 0x3: Select dispc_data23	RW	0x7
15	GPIO6_186_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	GPIO6_186_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	GPIO6_186_INPUTENABLE	Input enable value for pad gpio6_186 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	GPIO6_186_PWRDOWN	Power Down setting for pad gpio6_186 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	GPIO6_186_PULLTYPESELECT	Pull-Up/Down selection for pad gpio6_186 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPIO6_186_PULLUDENABLE	Pull-Up/Down enable for pad gpio6_186 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPIO6_186_MUXMODE	Functional multiplexing selection for pad gpio6_186 0x6: Select gpio6_186 0x7: Select safe_mode_core88 0x0: Select gpio6_186 0x4: Select kbd_row1 0x5: Select hw_dbg24 0x3: Select dispc_data22	RW	0x7

Table 18-597. Register Call Summary for Register CONTROL_CORE_PAD0_GPIO6_186_PAD1_GPIO6_187

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [3]

Table 18-598. CONTROL_CORE_PAD0_HDMI_CEC_PAD1_HDMI_HPD

Address Offset	0x0000 013C		
Physical Address	0x4A00 293C 0x4A00 293C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hdmi_cec and hdmi_hpd Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HDMI_HPD_WAKEUPEVENT	HDMI_HPD_WAKEUPENABLE	RESERVED					HDMI_HPD_INPUTENABLE	RESERVED		HDMI_HPD_PWRDOWN	HDMI_HPD_PULLTYPESELECT	HDMI_HPD_PULLUDENABLE	HDMI_HPD_MUXMODE			HDMI_CEC_WAKEUPEVENT	HDMI_CEC_WAKEUPENABLE	RESERVED					HDMI_CEC_INPUTENABLE	RESERVED		HDMI_CEC_PWRDOWN	HDMI_CEC_PULLTYPESELECT	HDMI_CEC_PULLUDENABLE	HDMI_CEC_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HDMI_HPD_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	HDMI_HPD_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	HDMI_HPD_INPUTENABLE	Input enable value for pad hdmi_hpd 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	HDMI_HPD_PWRDOWN	Power Down setting for pad hdmi_hpd 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HDMI_HPD_PULLTYPESELECT	Pull-Up/Down selection for pad hdmi_hpd 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	HDMI_HPD_PULLUDENABLE	Pull-Up/Down enable for pad hdmi_hpd 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	HDMI_HPD_MUXMODE	Functional multiplexing selection for pad hdmi_hpd 0x0: Select hdmi_hpd 0x7: Select safe_mode_core107 0x6: Select gpio7_193	RW	0x7
15	HDMI_CEC_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HDMI_CEC_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HDMI_CEC_INPUTENABLE	Input enable value for pad hdmi_cec 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	HDMI_CEC_PWRDOWN	Power Down setting for pad hdmi_cec 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HDMI_CEC_PULLTYPESELECT	Pull-Up/Down selection for pad hdmi_cec 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	HDMI_CEC_PULLUDENABLE	Pull-Up/Down enable for pad hdmi_cec 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HDMI_CEC_MUXMODE	Functional multiplexing selection for pad hdmi_cec 0x0: Select hdmi_cec 0x7: Select safe_mode_core106 0x6: Select gpio7_192	RW	0x7

Table 18-599. Register Call Summary for Register CONTROL_CORE_PAD0_HDMI_CEC_PAD1_HDMI_HPD

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-600. CONTROL_CORE_PAD0_HDMI_DDC_SCL_PAD1_HDMI_DDC_SDA

Address Offset	0x0000 0140		
Physical Address	0x4A00 2940 0x4A00 2940	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads hdmi_ddc_scl and hdmi_ddc_sda Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HDMI_DDC_SDA_WAKEUPEVENT	HDMI_DDC_SDA_WAKEUPENABLE	RESERVED					HDMI_DDC_SDA_INPUTENABLE	RESERVED		HDMI_DDC_SDA_PWRDOWN	HDMI_DDC_SDA_PULLTYPESELECT	HDMI_DDC_SDA_PULLUDENABLE	HDMI_DDC_SDA_MUXMODE			HDMI_DDC_SCL_WAKEUPEVENT	HDMI_DDC_SCL_WAKEUPENABLE	RESERVED					HDMI_DDC_SCL_INPUTENABLE	RESERVED		HDMI_DDC_SCL_PWRDOWN	HDMI_DDC_SCL_PULLTYPESELECT	HDMI_DDC_SCL_PULLUDENABLE	HDMI_DDC_SCL_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	HDMI_DDC_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	HDMI_DDC_SDA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29:25	RESERVED		R	0x0
24	HDMI_DDC_SDA_INPUTENABLE	Input enable value for pad hdmi_ddc_sda 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	HDMI_DDC_SDA_PWRDOWN	Power Down setting for pad hdmi_ddc_sda 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	HDMI_DDC_SDA_PULLTYPESELECT	Pull-Up/Down selection for pad hdmi_ddc_sda 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	HDMI_DDC_SDA_PULLUDENABLE	Pull-Up/Down enable for pad hdmi_ddc_sda 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	HDMI_DDC_SDA_MUXMODE	Functional multiplexing selection for pad hdmi_ddc_sda 0x0: Select hdmi_ddc_sda 0x7: Select safe_mode_core109 0x6: Select gpio7_195	RW	0x7
15	HDMI_DDC_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	HDMI_DDC_SCL_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	HDMI_DDC_SCL_INPUTENABLE	Input enable value for pad hdmi_ddc_scl 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	HDMI_DDC_SCL_PWRDOWN	Power Down setting for pad hdmi_ddc_scl 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	HDMI_DDC_SCL_PULLTYPESELECT	Pull-Up/Down selection for pad hdmi_ddc_scl 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	HDMI_DDC_SCL_PULLUDENABLE	Pull-Up/Down enable for pad hdmi_ddc_scl 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	HDMI_DDC_SCL_MUXMODE	Functional multiplexing selection for pad hdmi_ddc_scl 0x0: Select hdmi_ddc_scl 0x7: Select safe_mode_core108 0x6: Select gpio7_194	RW	0x7

Table 18-601. Register Call Summary for Register CONTROL_CORE_PAD0_HDMI_DDC_SCL_PAD1_HDMI_DDC_SDA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-602. CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y

Address Offset	0x0000 0144		
Physical Address	0x4A00 2944 0x4A00 2944	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiportc_lane0x and csiportc_lane0y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTC_LANE0Y_WAKEUPEVENT	CSIPORTC_LANE0Y_WAKEUPENABLE	RESERVED					CSIPORTC_LANE0Y_INPUTENABLE	RESERVED			CSIPORTC_LANE0Y_PULLTYPESELECT	CSIPORTC_LANE0Y_PULLUDENABLE	CSIPORTC_LANE0Y_MUXMODE			CSIPORTC_LANE0X_WAKEUPEVENT	CSIPORTC_LANE0X_WAKEUPENABLE	RESERVED					CSIPORTC_LANE0X_INPUTENABLE	RESERVED			CSIPORTC_LANE0X_PULLTYPESELECT	CSIPORTC_LANE0X_PULLUDENABLE	CSIPORTC_LANE0X_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSIPORTC_LANE0Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTC_LANE0Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	CSIPORTC_LANE0Y_INPUTENABLE	Input enable value for pad csiportc_lane0y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTC_LANE0Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiportc_lane0y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTC_LANE0Y_PULLUDENABLE	Pull-Up/Down enable for pad csiportc_lane0y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	CSIPORTC_LANE0Y_MUXMODE	Functional multiplexing selection for pad csiportc_lane0y 0x0: Select csiportc_lane0y 0x3: Select cpi_data8 0x7: Select safe_mode_core126 0x6: Select gpio8_in252	RW	0x7
15	CSIPORTC_LANE0X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	CSIPORTC_LANE0X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTC_LANE0X_INPUTENABLE	Input enable value for pad csiportc_lane0x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSIPORTC_LANE0X_PULLTYPESELECT	Pull-Up/Down selection for pad csiportc_lane0x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTC_LANE0X_PULLUDENABLE	Pull-Up/Down enable for pad csiportc_lane0x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTC_LANE0X_MUXMODE	Functional multiplexing selection for pad csiportc_lane0x 0x0: Select csiportc_lane0x 0x3: Select cpi_data9 0x7: Select safe_mode_core127 0x6: Select gpio8_in253	RW	0x7

Table 18-603. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-604. CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y

Address Offset	0x0000 0148		
Physical Address	0x4A00 2948 0x4A00 2948	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiportc_lane1x and csiportc_lane1y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTC_LANE1Y_WAKEUPEVENT	CSIPORTC_LANE1Y_WAKEUPENABLE	RESERVED					CSIPORTC_LANE1Y_INPUTENABLE	RESERVED			CSIPORTC_LANE1Y_PULLTYPESELECT	CSIPORTC_LANE1Y_PULLUDENABLE	CSIPORTC_LANE1Y_MUXMODE			CSIPORTC_LANE1X_WAKEUPEVENT	CSIPORTC_LANE1X_WAKEUPENABLE	RESERVED					CSIPORTC_LANE1X_INPUTENABLE	RESERVED				CSIPORTC_LANE1X_PULLTYPESELECT	CSIPORTC_LANE1X_PULLUDENABLE	CSIPORTC_LANE1X_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	CSIPORTC_LANE1Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTC_LANE1Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	CSIPORTC_LANE1Y_INPUTENABLE	Input enable value for pad csiportc_lane1y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTC_LANE1Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiportc_lane1y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTC_LANE1Y_PULLUDENABLE	Pull-Up/Down enable for pad csiportc_lane1y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	CSIPORTC_LANE1Y_MUXMODE	Functional multiplexing selection for pad csiportc_lane1y 0x0: Select csiportc_lane1y 0x3: Select cpi_data10 0x7: Select safe_mode_core128 0x6: Select gpio8_in254	RW	0x7
15	CSIPORTC_LANE1X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSIPORTC_LANE1X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTC_LANE1X_INPUTENABLE	Input enable value for pad csiportc_lane1x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSIPORTC_LANE1X_PULLTYPESELECT	Pull-Up/Down selection for pad csiportc_lane1x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTC_LANE1X_PULLUDENABLE	Pull-Up/Down enable for pad csiportc_lane1x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTC_LANE1X_MUXMODE	Functional multiplexing selection for pad csiportc_lane1x 0x0: Select csiportc_lane1x 0x3: Select cpi_data11 0x7: Select safe_mode_core129 0x6: Select gpio8_in255	RW	0x7

Table 18-605. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-605. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-606. CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y

Address Offset	0x0000 014C		
Physical Address	0x4A00 294C 0x4A00 294C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiportb_lane0x and csiportb_lane0y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTB_LANE0Y_WAKEUPEVENT	CSIPORTB_LANE0Y_WAKEUPENABLE	RESERVED					CSIPORTB_LANE0Y_INPUTENABLE	RESERVED			CSIPORTB_LANE0Y_PULLTYPESELECT	CSIPORTB_LANE0Y_PULLUDENABLE	CSIPORTB_LANE0Y_MUXMODE			CSIPORTB_LANE0X_WAKEUPEVENT	CSIPORTB_LANE0X_WAKEUPENABLE	RESERVED					CSIPORTB_LANE0X_INPUTENABLE	RESERVED			CSIPORTB_LANE0X_PULLTYPESELECT	CSIPORTB_LANE0X_PULLUDENABLE	CSIPORTB_LANE0X_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSIPORTB_LANE0Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTB_LANE0Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	CSIPORTB_LANE0Y_INPUTENABLE	Input enable value for pad csiportb_lane0y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTB_LANE0Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiportb_lane0y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTB_LANE0Y_PULLUDENABLE	Pull-Up/Down enable for pad csiportb_lane0y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	CSIPORTB_LANE0Y_MUXMODE	Functional multiplexing selection for pad csiportb_lane0y 0x0: Select csiportb_lane0y 0x4: Select cpi_data13 0x7: Select safe_mode_core121 0x6: Select gpio8_in247	RW	0x7
15	CSIPORTB_LANE0X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSIPORTB_LANE0X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTB_LANE0X_INPUTENABLE	Input enable value for pad csiportb_lane0x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSIPORTB_LANE0X_PULLTYPESELECT	Pull-Up/Down selection for pad csiportb_lane0x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTB_LANE0X_PULLUDENABLE	Pull-Up/Down enable for pad csiportb_lane0x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTB_LANE0X_MUXMODE	Functional multiplexing selection for pad csiportb_lane0x 0x0: Select csiportb_lane0x 0x4: Select cpi_data12 0x7: Select safe_mode_core120 0x6: Select gpio8_in246	RW	0x7

Table 18-607. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-608. CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y

Address Offset	0x0000 0150		
Physical Address	0x4A00 2950 0x4A00 2950	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiportb_lane1x and csiportb_lane1y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTB_LANE1Y_WAKEUPEVENT	CSIPORTB_LANE1Y_WAKEUPENABLE	RESERVED					CSIPORTB_LANE1Y_INPUTENABLE	RESERVED			CSIPORTB_LANE1Y_PULLTYPESELECT	CSIPORTB_LANE1Y_PULLUDENABLE	CSIPORTB_LANE1Y_MUXMODE			CSIPORTB_LANE1X_WAKEUPEVENT	CSIPORTB_LANE1X_WAKEUPENABLE	RESERVED					CSIPORTB_LANE1X_INPUTENABLE	RESERVED			CSIPORTB_LANE1X_PULLTYPESELECT	CSIPORTB_LANE1X_PULLUDENABLE	CSIPORTB_LANE1X_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSIPORTB_LANE1Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTB_LANE1Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	CSIPORTB_LANE1Y_INPUTENABLE	Input enable value for pad csiportb_lane1y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTB_LANE1Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiportb_lane1y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTB_LANE1Y_PULLUDENABLE	Pull-Up/Down enable for pad csiportb_lane1y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	CSIPORTB_LANE1Y_MUXMODE	Functional multiplexing selection for pad csiportb_lane1y 0x0: Select csiportb_lane1y 0x4: Select cpi_data14 0x7: Select safe_mode_core122 0x6: Select gpio8_in248	RW	0x7
15	CSIPORTB_LANE1X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSIPORTB_LANE1X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTB_LANE1X_INPUTENABLE	Input enable value for pad csiportb_lane1x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	CSIPORTB_LANE1X_PULLTYPESELECT	Pull-Up/Down selection for pad csiportb_lane1x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTB_LANE1X_PULLUDENABLE	Pull-Up/Down enable for pad csiportb_lane1x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTB_LANE1X_MUXMODE	Functional multiplexing selection for pad csiportb_lane1x 0x0: Select csiportb_lane1x 0x4: Select cpi_data15 0x7: Select safe_mode_core123 0x6: Select gpio8_in249	RW	0x7

Table 18-609. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-610. CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y

Address Offset	0x0000 0154		
Physical Address	0x4A00 2954 0x4A00 2954	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiportb_lane2x and csiportb_lane2y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTB_LANE2Y_WAKEUPEVENT	CSIPORTB_LANE2Y_WAKEUPENABLE	RESERVED					CSIPORTB_LANE2Y_INPUTENABLE	RESERVED			CSIPORTB_LANE2Y_PULLTYPESELECT	CSIPORTB_LANE2Y_PULLUDENABLE	CSIPORTB_LANE2Y_MUXMODE			CSIPORTB_LANE2X_WAKEUPEVENT	CSIPORTB_LANE2X_WAKEUPENABLE	RESERVED					CSIPORTB_LANE2X_INPUTENABLE	RESERVED				CSIPORTB_LANE2X_PULLTYPESELECT	CSIPORTB_LANE2X_PULLUDENABLE	CSIPORTB_LANE2X_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSIPORTB_LANE2Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTB_LANE2Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
24	CSIPORTB_LANE2Y_INPUTENABLE	Input enable value for pad csiportb_lane2y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTB_LANE2Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiportb_lane2y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTB_LANE2Y_PULLUDENABLE	Pull-Up/Down enable for pad csiportb_lane2y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	CSIPORTB_LANE2Y_MUXMODE	Functional multiplexing selection for pad csiportb_lane2y 0x0: Select csiportb_lane2y 0x4: Select cpi_hsyncin 0x7: Select safe_mode_core124 0x6: Select gpio8_in250	RW	0x7
15	CSIPORTB_LANE2X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSIPORTB_LANE2X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTB_LANE2X_INPUTENABLE	Input enable value for pad csiportb_lane2x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSIPORTB_LANE2X_PULLTYPESELECT	Pull-Up/Down selection for pad csiportb_lane2x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTB_LANE2X_PULLUDENABLE	Pull-Up/Down enable for pad csiportb_lane2x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTB_LANE2X_MUXMODE	Functional multiplexing selection for pad csiportb_lane2x 0x0: Select csiportb_lane2x 0x4: Select cpi_vsyncin 0x7: Select safe_mode_core125 0x6: Select gpio8_in251	RW	0x7

Table 18-611. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-612. CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y

Address Offset	0x0000 0158		
Physical Address	0x4A00 2958 0x4A00 2958	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiporta_lane0x and csiporta_lane0y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTA_LANE0Y_WAKEUPEVENT	CSIPORTA_LANE0Y_WAKEUPENABLE	RESERVED					CSIPORTA_LANE0Y_INPUTENABLE	RESERVED			CSIPORTA_LANE0Y_PULLTYPESELECT	CSIPORTA_LANE0Y_PULLUDENABLE	CSIPORTA_LANE0Y_MUXMODE			CSIPORTA_LANE0X_WAKEUPEVENT	CSIPORTA_LANE0X_WAKEUPENABLE	RESERVED					CSIPORTA_LANE0X_INPUTENABLE	RESERVED			CSIPORTA_LANE0X_PULLTYPESELECT	CSIPORTA_LANE0X_PULLUDENABLE	CSIPORTA_LANE0X_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSIPORTA_LANE0Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTA_LANE0Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	CSIPORTA_LANE0Y_INPUTENABLE	Input enable value for pad csiporta_lane0y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTA_LANE0Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane0y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTA_LANE0Y_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane0y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	CSIPORTA_LANE0Y_MUXMODE	Functional multiplexing selection for pad csiporta_lane0y 0x0: Select csiporta_lane0y 0x3: Select cpi_wen 0x7: Select safe_mode_core111 0x6: Select gpio8_in237	RW	0x7
15	CSIPORTA_LANE0X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	CSIPORTA_LANE0X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTA_LANE0X_INPUTENABLE	Input enable value for pad csiporta_lane0x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSIPORTA_LANE0X_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane0x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTA_LANE0X_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane0x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTA_LANE0X_MUXMODE	Functional multiplexing selection for pad csiporta_lane0x 0x0: Select csiporta_lane0x 0x3: Select cpi_pclk 0x7: Select safe_mode_core110 0x6: Select gpio8_in236	RW	0x7

Table 18-613. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-614. CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y

Address Offset	0x0000 015C		
Physical Address	0x4A00 295C 0x4A00 295C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiporta_lane1x and csiporta_lane1y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTA_LANE1Y_WAKEUPEVENT	CSIPORTA_LANE1Y_WAKEUPENABLE	RESERVED					CSIPORTA_LANE1Y_INPUTENABLE	RESERVED			CSIPORTA_LANE1Y_PULLTYPESELECT	CSIPORTA_LANE1Y_PULLUDENABLE	CSIPORTA_LANE1Y_MUXMODE			CSIPORTA_LANE1X_WAKEUPEVENT	CSIPORTA_LANE1X_WAKEUPENABLE	RESERVED					CSIPORTA_LANE1X_INPUTENABLE	RESERVED			CSIPORTA_LANE1X_PULLTYPESELECT	CSIPORTA_LANE1X_PULLUDENABLE	CSIPORTA_LANE1X_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	CSIPORTA_LANE1Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTA_LANE1Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	CSIPORTA_LANE1Y_INPUTENABLE	Input enable value for pad csiporta_lane1y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTA_LANE1Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane1y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTA_LANE1Y_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane1y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	CSIPORTA_LANE1Y_MUXMODE	Functional multiplexing selection for pad csiporta_lane1y 0x0: Select csiporta_lane1y 0x3: Select cpi_data0 0x7: Select safe_mode_core112 0x6: Select gpio8_in238	RW	0x7
15	CSIPORTA_LANE1X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSIPORTA_LANE1X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTA_LANE1X_INPUTENABLE	Input enable value for pad csiporta_lane1x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSIPORTA_LANE1X_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane1x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTA_LANE1X_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane1x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTA_LANE1X_MUXMODE	Functional multiplexing selection for pad csiporta_lane1x 0x0: Select csiporta_lane1x 0x3: Select cpi_data1 0x7: Select safe_mode_core113 0x6: Select gpio8_in239	RW	0x7

Table 18-615. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-615. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-616. CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y

Address Offset	0x0000 0160		
Physical Address	0x4A00 2960 0x4A00 2960	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiporta_lane2x and csiporta_lane2y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTA_LANE2Y_WAKEUPEVENT	CSIPORTA_LANE2Y_WAKEUPENABLE	RESERVED					CSIPORTA_LANE2Y_INPUTENABLE	RESERVED			CSIPORTA_LANE2Y_PULLTYPESELECT	CSIPORTA_LANE2Y_PULLUDENABLE	CSIPORTA_LANE2Y_MUXMODE			CSIPORTA_LANE2X_WAKEUPEVENT	CSIPORTA_LANE2X_WAKEUPENABLE	RESERVED					CSIPORTA_LANE2X_INPUTENABLE	RESERVED			CSIPORTA_LANE2X_PULLTYPESELECT	CSIPORTA_LANE2X_PULLUDENABLE	CSIPORTA_LANE2X_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSIPORTA_LANE2Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTA_LANE2Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	CSIPORTA_LANE2Y_INPUTENABLE	Input enable value for pad csiporta_lane2y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTA_LANE2Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane2y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTA_LANE2Y_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane2y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	CSIPORTA_LANE2Y_MUXMODE	Functional multiplexing selection for pad csiporta_lane2y 0x0: Select csiporta_lane2y 0x3: Select cpi_data2 0x7: Select safe_mode_core114 0x6: Select gpio8_in240	RW	0x7
15	CSIPORTA_LANE2X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSIPORTA_LANE2X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTA_LANE2X_INPUTENABLE	Input enable value for pad csiporta_lane2x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSIPORTA_LANE2X_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane2x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTA_LANE2X_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane2x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTA_LANE2X_MUXMODE	Functional multiplexing selection for pad csiporta_lane2x 0x0: Select csiporta_lane2x 0x3: Select cpi_data3 0x7: Select safe_mode_core115 0x6: Select gpio8_in241	RW	0x7

Table 18-617. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-618. CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y

Address Offset	0x0000 0164		
Physical Address	0x4A00 2964 0x4A00 2964	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiporta_lane3x and csiporta_lane3y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTA_LANE3Y_WAKEUPEVENT	CSIPORTA_LANE3Y_WAKEUPENABLE	RESERVED					CSIPORTA_LANE3Y_INPUTENABLE	RESERVED			CSIPORTA_LANE3Y_PULLTYPESELECT	CSIPORTA_LANE3Y_PULLUDENABLE	CSIPORTA_LANE3Y_MUXMODE			CSIPORTA_LANE3X_WAKEUPEVENT	CSIPORTA_LANE3X_WAKEUPENABLE	RESERVED					CSIPORTA_LANE3X_INPUTENABLE	RESERVED				CSIPORTA_LANE3X_PULLTYPESELECT	CSIPORTA_LANE3X_PULLUDENABLE	CSIPORTA_LANE3X_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSIPORTA_LANE3Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTA_LANE3Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	CSIPORTA_LANE3Y_INPUTENABLE	Input enable value for pad csiporta_lane3y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTA_LANE3Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane3y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTA_LANE3Y_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane3y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	CSIPORTA_LANE3Y_MUXMODE	Functional multiplexing selection for pad csiporta_lane3y 0x0: Select csiporta_lane3y 0x3: Select cpi_data5 0x7: Select safe_mode_core117 0x6: Select gpio8_in243	RW	0x7
15	CSIPORTA_LANE3X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSIPORTA_LANE3X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTA_LANE3X_INPUTENABLE	Input enable value for pad csiporta_lane3x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	CSIPORTA_LANE3X_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane3x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTA_LANE3X_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane3x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTA_LANE3X_MUXMODE	Functional multiplexing selection for pad csiporta_lane3x 0x0: Select csiporta_lane3x 0x3: Select cpi_data4 0x7: Select safe_mode_core116 0x6: Select gpio8_in242	RW	0x7

Table 18-619. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-620. CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y

Address Offset	0x0000 0168		
Physical Address	0x4A00 2968 0x4A00 2968	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads csiporta_lane4x and csiporta_lane4y Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTA_LANE4Y_WAKEUPEVENT	CSIPORTA_LANE4Y_WAKEUPENABLE	RESERVED					CSIPORTA_LANE4Y_INPUTENABLE	RESERVED			CSIPORTA_LANE4Y_PULLTYPESELECT	CSIPORTA_LANE4Y_PULLUDENABLE	CSIPORTA_LANE4Y_MUXMODE			CSIPORTA_LANE4X_WAKEUPEVENT	CSIPORTA_LANE4X_WAKEUPENABLE	RESERVED					CSIPORTA_LANE4X_INPUTENABLE	RESERVED				CSIPORTA_LANE4X_PULLTYPESELECT	CSIPORTA_LANE4X_PULLUDENABLE	CSIPORTA_LANE4X_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSIPORTA_LANE4Y_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSIPORTA_LANE4Y_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
24	CSIPORTA_LANE4Y_INPUTENABLE	Input enable value for pad csiporta_lane4y 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSIPORTA_LANE4Y_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane4y 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSIPORTA_LANE4Y_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane4y 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	CSIPORTA_LANE4Y_MUXMODE	Functional multiplexing selection for pad csiporta_lane4y 0x0: Select csiporta_lane4y 0x3: Select cpi_data7 0x7: Select safe_mode_core119 0x6: Select gpio8_in245	RW	0x7
15	CSIPORTA_LANE4X_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSIPORTA_LANE4X_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CSIPORTA_LANE4X_INPUTENABLE	Input enable value for pad csiporta_lane4x 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSIPORTA_LANE4X_PULLTYPESELECT	Pull-Up/Down selection for pad csiporta_lane4x 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSIPORTA_LANE4X_PULLUDENABLE	Pull-Up/Down enable for pad csiporta_lane4x 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSIPORTA_LANE4X_MUXMODE	Functional multiplexing selection for pad csiporta_lane4x 0x0: Select csiporta_lane4x 0x3: Select cpi_data6 0x7: Select safe_mode_core118 0x6: Select gpio8_in244	RW	0x7

Table 18-621. Register Call Summary for Register CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-622. CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE

Address Offset	0x0000 016C		
Physical Address	0x4A00 296C 0x4A00 296C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads cam_shutter and cam_strobe Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAM_STROBE_WAKEUPEVENT	CAM_STROBE_WAKEUPENABLE	RESERVED					CAM_STROBE_INPUTENABLE	RESERVED		CAM_STROBE_PWRDOWN	CAM_STROBE_PULLTYPESELECT	CAM_STROBE_PULLUDENABLE	CAM_STROBE_MUXMODE			CAM_SHUTTER_WAKEUPEVENT	CAM_SHUTTER_WAKEUPENABLE	RESERVED					CAM_SHUTTER_INPUTENABLE	RESERVED		CAM_SHUTTER_PWRDOWN	CAM_SHUTTER_PULLTYPESELECT	CAM_SHUTTER_PULLUDENABLE	CAM_SHUTTER_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CAM_STROBE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CAM_STROBE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	CAM_STROBE_INPUTENABLE	Input enable value for pad cam_strobe 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	CAM_STROBE_PWRDOWN	Power Down setting for pad cam_strobe 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	CAM_STROBE_PULLTYPESELECT	Pull-Up/Down selection for pad cam_strobe 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CAM_STROBE_PULLUDENABLE	Pull-Up/Down enable for pad cam_strobe 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
18:16	CAM_STROBE_MUXMODE	Functional multiplexing selection for pad cam_strobe 0x0: Select cam_strobe 0x6: Select gpio8_225 0x7: Select safe_mode_core131 0x5: Select sys_nodeid1	RW	0x5
15	CAM_SHUTTER_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	CAM_SHUTTER_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	CAM_SHUTTER_INPUTENABLE	Input enable value for pad cam_shutter 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	CAM_SHUTTER_PWRDOWN	Power Down setting for pad cam_shutter 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	CAM_SHUTTER_PULLTYPESELECT	Pull-Up/Down selection for pad cam_shutter 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CAM_SHUTTER_PULLUDENABLE	Pull-Up/Down enable for pad cam_shutter 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
2:0	CAM_SHUTTER_MUXMODE	Functional multiplexing selection for pad cam_shutter 0x0: Select cam_shutter 0x6: Select gpio8_224 0x7: Select safe_mode_core130 0x5: Select sys_nodeid0	RW	0x5

Table 18-623. Register Call Summary for Register CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-624. CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_TIMER11_PWM_EVT

Address Offset	0x0000 0170		
Physical Address	0x4A00 2970 0x4A00 2970	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads cam_globalreset and timer11_pwm_evt Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER11_PWM_EVT_WAKEUPEVENT	TIMER11_PWM_EVT_WAKEUPENABLE	RESERVED					TIMER11_PWM_EVT_INPUTENABLE	RESERVED		TIMER11_PWM_EVT_PWRDOWN	TIMER11_PWM_EVT_PULLTYPESELECT	TIMER11_PWM_EVT_PULLUDENABLE	TIMER11_PWM_EVT_MUXMODE			CAM_GLOBALRESET_WAKEUPEVENT	CAM_GLOBALRESET_WAKEUPENABLE	RESERVED					CAM_GLOBALRESET_INPUTENABLE	RESERVED		CAM_GLOBALRESET_PWRDOWN	CAM_GLOBALRESET_PULLTYPESELECT	CAM_GLOBALRESET_PULLUDENABLE	CAM_GLOBALRESET_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	TIMER11_PWM_EVT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	TIMER11_PWM_EVT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	TIMER11_PWM_EVT_INPUTENABLE	Input enable value for pad timer11_pwm_evt 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	TIMER11_PWM_EVT_PWRDOWN	Power Down setting for pad timer11_pwm_evt 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	TIMER11_PWM_EVT_PULLTYPESELECT	Pull-Up/Down selection for pad timer11_pwm_evt 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	TIMER11_PWM_EVT_PULLUDENABLE	Pull-Up/Down enable for pad timer11_pwm_evt 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	TIMER11_PWM_EVT_MUXMODE	Functional multiplexing selection for pad timer11_pwm_evt 0x0: Select timer11_pwm_evt 0x2: Select uart1_tx 0x6: Select gpio8_227 0x3: Select cpi_data12 0x7: Select safe_mode_core133 0x5: Select hw_dbg26	RW	0x7
15	CAM_GLOBALRESET_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CAM_GLOBALRESET_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
8	CAM_GLOBALRESET_INPUTENABLE	Input enable value for pad cam_globalreset 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	CAM_GLOBALRESET_PWRDOWN	Power Down setting for pad cam_globalreset 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	CAM_GLOBALRESET_PULLTYPESELECT	Pull-Up/Down selection for pad cam_globalreset 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CAM_GLOBALRESET_PULLUDENABLE	Pull-Up/Down enable for pad cam_globalreset 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CAM_GLOBALRESET_MUXMODE	Functional multiplexing selection for pad cam_globalreset 0x0: Select cam_globalreset 0x1: Select cam_shutter 0x3: Select cpi_fid 0x7: Select safe_mode_core132 0x6: Select gpio8_226	RW	0x7

Table 18-625. Register Call Summary for Register CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_TIMER11_PWM_EVT

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [3]

Table 18-626. CONTROL_CORE_PAD0_TIMER5_PWM_EVT_PAD1_TIMER6_PWM_EVT

Address Offset	0x0000 0174		
Physical Address	0x4A00 2974 0x4A00 2974	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads timer5_pwm_evt and timer6_pwm_evt Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER6_PWM_EVT_WAKEUPEVENT	TIMER6_PWM_EVT_WAKEUPENABLE	RESERVED					TIMER6_PWM_EVT_INPUTENABLE	RESERVED		TIMER6_PWM_EVT_PWRDOWN	TIMER6_PWM_EVT_PULLTYPESELECT	TIMER6_PWM_EVT_PULLUDENABLE	TIMER6_PWM_EVT_MUXMODE			TIMER5_PWM_EVT_WAKEUPEVENT	TIMER5_PWM_EVT_WAKEUPENABLE	RESERVED					TIMER5_PWM_EVT_INPUTENABLE	RESERVED		TIMER5_PWM_EVT_PWRDOWN	TIMER5_PWM_EVT_PULLTYPESELECT	TIMER5_PWM_EVT_PULLUDENABLE	TIMER5_PWM_EVT_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	TIMER6_PWM_EVT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	TIMER6_PWM_EVT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	TIMER6_PWM_EVT_INPUTENABLE	Input enable value for pad timer6_pwm_evt 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	TIMER6_PWM_EVT_PWRDOWN	Power Down setting for pad timer6_pwm_evt 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	TIMER6_PWM_EVT_PULLTYPESELECT	Pull-Up/Down selection for pad timer6_pwm_evt 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	TIMER6_PWM_EVT_PULLUDENABLE	Pull-Up/Down enable for pad timer6_pwm_evt 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	TIMER6_PWM_EVT_MUXMODE	Functional multiplexing selection for pad timer6_pwm_evt 0x0: Select timer6_pwm_evt 0x1: Select sdcard_wp 0x2: Select uart1_rx 0x3: Select cpi_data14 0x7: Select safe_mode_core135 0x6: Select gpio8_229	RW	0x7
15	TIMER5_PWM_EVT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	TIMER5_PWM_EVT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	TIMER5_PWM_EVT_INPUTENABLE	Input enable value for pad timer5_pwm_evt 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	TIMER5_PWM_EVT_PWRDOWN	Power Down setting for pad timer5_pwm_evt 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	TIMER5_PWM_EVT_PULLTYPESELECT	Pull-Up/Down selection for pad timer5_pwm_evt 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	TIMER5_PWM_EVT_PULLUDENABLE	Pull-Up/Down enable for pad timer5_pwm_evt 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	TIMER5_PWM_EVT_MUXMODE	Functional multiplexing selection for pad timer5_pwm_evt 0x0: Select timer5_pwm_evt 0x1: Select sdcard_cd 0x2: Select uart1_cts 0x3: Select cpi_data13 0x7: Select safe_mode_core134 0x6: Select gpio8_228	RW	0x7

Table 18-627. Register Call Summary for Register CONTROL_CORE_PAD0_TIMER5_PWM_EVT_PAD1_TIMER6_PWM_EVT

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-628. CONTROL_CORE_PAD0_TIMER8_PWM_EVT_PAD1_I2C3_SCL

Address Offset	0x0000 0178		
Physical Address	0x4A00 2978 0x4A00 2978	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads timer8_pwm_evt and i2c3_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C3_SCL_WAKEUPEVENT	I2C3_SCL_WAKEUPENABLE	RESERVED					I2C3_SCL_INPUTENABLE	RESERVED		I2C3_SCL_PWRDOWN	I2C3_SCL_PULLTYPESELECT	I2C3_SCL_PULLUDENABLE	I2C3_SCL_MUXMODE			TIMER8_PWM_EVT_WAKEUPEVENT	TIMER8_PWM_EVT_WAKEUPENABLE	RESERVED					TIMER8_PWM_EVT_INPUTENABLE	RESERVED		TIMER8_PWM_EVT_PWRDOWN	TIMER8_PWM_EVT_PULLTYPESELECT	TIMER8_PWM_EVT_PULLUDENABLE	TIMER8_PWM_EVT_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	I2C3_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	I2C3_SCL_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	I2C3_SCL_INPUTENABLE	Input enable value for pad i2c3_scl 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	I2C3_SCL_PWRDOWN	Power Down setting for pad i2c3_scl 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	I2C3_SCL_PULLTYPESELECT	Pull-Up/Down selection for pad i2c3_scl 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	I2C3_SCL_PULLUDENABLE	Pull-Up/Down enable for pad i2c3_scl 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	I2C3_SCL_MUXMODE	Functional multiplexing selection for pad i2c3_scl 0x0: Select i2c3_scl 0x7: Select safe_mode_core137 0x6: Select gpio8_231	RW	0x7
15	TIMER8_PWM_EVT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	TIMER8_PWM_EVT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	TIMER8_PWM_EVT_INPUTENABLE	Input enable value for pad timer8_pwm_evt 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	TIMER8_PWM_EVT_PWRDOWN	Power Down setting for pad timer8_pwm_evt 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	TIMER8_PWM_EVT_PULLTYPESELECT	Pull-Up/Down selection for pad timer8_pwm_evt 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	TIMER8_PWM_EVT_PULLUDENABLE	Pull-Up/Down enable for pad timer8_pwm_evt 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	TIMER8_PWM_EVT_MUXMODE	Functional multiplexing selection for pad timer8_pwm_evt 0x0: Select timer8_pwm_evt 0x1: Select sdcard_wp 0x2: Select uart1_rts 0x6: Select gpio8_230 0x3: Select cpi_data15 0x7: Select safe_mode_core136 0x5: Select hw_dbg27	RW	0x7

Table 18-629. Register Call Summary for Register CONTROL_CORE_PAD0_TIMER8_PWM_EVT_PAD1_I2C3_SCL

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [3]

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Table 18-630. CONTROL_CORE_PAD0_I2C3_SDA_PAD1_GPIO8_233

Address Offset	0x0000 017C		
Physical Address	0x4A00 297C 0x4A00 297C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads i2c3_sda and gpio8_233 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO8_233_WAKEUPEVENT	GPIO8_233_WAKEUPENABLE	RESERVED					GPIO8_233_INPUTENABLE	RESERVED		GPIO8_233_PWRDOWN	GPIO8_233_PULLTYPESELECT	GPIO8_233_PULLUDENABLE	GPIO8_233_MUXMODE			I2C3_SDA_WAKEUPEVENT	I2C3_SDA_WAKEUPENABLE	RESERVED					I2C3_SDA_INPUTENABLE	RESERVED		I2C3_SDA_PWRDOWN	I2C3_SDA_PULLTYPESELECT	I2C3_SDA_PULLUDENABLE	I2C3_SDA_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPIO8_233_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPIO8_233_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	GPIO8_233_INPUTENABLE	Input enable value for pad gpio8_233 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	GPIO8_233_PWRDOWN	Power Down setting for pad gpio8_233 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	GPIO8_233_PULLTYPESELECT	Pull-Up/Down selection for pad gpio8_233 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	GPIO8_233_PULLUDENABLE	Pull-Up/Down enable for pad gpio8_233 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPIO8_233_MUXMODE	Functional multiplexing selection for pad gpio8_233 0x6: Select gpio8_233 0x1: Reserved 0x7: Select safe_mode_core139 0x0: Select gpio8_233 0x2: Select timer8_pwm_evt 0x3: Select cpi_hsync	RW	0x7
15	I2C3_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	I2C3_SDA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	I2C3_SDA_INPUTENABLE	Input enable value for pad i2c3_sda 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	I2C3_SDA_PWRDOWN	Power Down setting for pad i2c3_sda 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	I2C3_SDA_PULLTYPESELECT	Pull-Up/Down selection for pad i2c3_sda 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	I2C3_SDA_PULLUDENABLE	Pull-Up/Down enable for pad i2c3_sda 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	I2C3_SDA_MUXMODE	Functional multiplexing selection for pad i2c3_sda 0x0: Select i2c3_sda 0x7: Select safe_mode_core138 0x6: Select gpio8_232	RW	0x7

Table 18-631. Register Call Summary for Register CONTROL_CORE_PAD0_I2C3_SDA_PAD1_GPIO8_233

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-632. CONTROL_CORE_PAD0_GPIO8_234_PAD1_ABE_CLKS

Address Offset	0x0000 0180		
Physical Address	0x4A00 2980 0x4A00 2980	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads gpio8_234 and abe_clks Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABE_CLKS_WAKEUPEVENT	ABE_CLKS_WAKEUPENABLE	RESERVED					ABE_CLKS_INPUTENABLE	RESERVED		ABE_CLKS_PWRDOWN	ABE_CLKS_PULLTYPESELECT	ABE_CLKS_PULLUDENABLE	ABE_CLKS_MUXMODE			GPIO8_234_WAKEUPEVENT	GPIO8_234_WAKEUPENABLE	RESERVED					GPIO8_234_INPUTENABLE	RESERVED		GPIO8_234_PWRDOWN	GPIO8_234_PULLTYPESELECT	GPIO8_234_PULLUDENABLE	GPIO8_234_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	ABE_CLKS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	ABE_CLKS_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	ABE_CLKS_INPUTENABLE	Input enable value for pad abe_clks 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	ABE_CLKS_PWRDOWN	Power Down setting for pad abe_clks 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	ABE_CLKS_PULLTYPESELECT	Pull-Up/Down selection for pad abe_clks 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	ABE_CLKS_PULLUDENABLE	Pull-Up/Down enable for pad abe_clks 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	ABE_CLKS_MUXMODE	Functional multiplexing selection for pad abe_clks 0x0: Select abe_clks 0x3: Select abemcasp_axr 0x7: Select safe_mode_core141 0x6: Select gpio4_96	RW	0x7
15	GPIO8_234_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPIO8_234_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	GPIO8_234_INPUTENABLE	Input enable value for pad gpio8_234 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	GPIO8_234_PWRDOWN	Power Down setting for pad gpio8_234 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	GPIO8_234_PULLTYPESELECT	Pull-Up/Down selection for pad gpio8_234 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPIO8_234_PULLUDENABLE	Pull-Up/Down enable for pad gpio8_234 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	GPIO8_234_MUXMODE	Functional multiplexing selection for pad gpio8_234 0x0: Select gpio8_234 0x1: Reserved 0x3: Select cpi_vsync 0x7: Select safe_mode_core140 0x6: Select gpio8_234	RW	0x7

Table 18-633. Register Call Summary for Register CONTROL_CORE_PAD0_GPIO8_234_PAD1_ABE_CLKS

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-634. CONTROL_CORE_PAD0_ABEDMIC_DIN1_PAD1_ABEDMIC_DIN2

Address Offset	0x0000 0184		
Physical Address	0x4A00 2984 0x4A00 2984	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads abedmic_din1 and abedmic_din2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABEDMIC_DIN2_WAKEUPEVENT	ABEDMIC_DIN2_WAKEUPENABLE	RESERVED					ABEDMIC_DIN2_INPUTENABLE	RESERVED		ABEDMIC_DIN2_PWRDOWN	ABEDMIC_DIN2_PULLTYPESELECT	ABEDMIC_DIN2_PULLUDENABLE	ABEDMIC_DIN2_MUXMODE			ABEDMIC_DIN1_WAKEUPEVENT	ABEDMIC_DIN1_WAKEUPENABLE	RESERVED					ABEDMIC_DIN1_INPUTENABLE	RESERVED		ABEDMIC_DIN1_PWRDOWN	ABEDMIC_DIN1_PULLTYPESELECT	ABEDMIC_DIN1_PULLUDENABLE	ABEDMIC_DIN1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABEDMIC_DIN2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	ABEDMIC_DIN2_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	ABEDMIC_DIN2_INPUTENABLE	Input enable value for pad abedmic_din2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	ABEDMIC_DIN2_PWRDOWN	Power Down setting for pad abedmic_din2 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	ABEDMIC_DIN2_PULLTYPESELECT	Pull-Up/Down selection for pad abedmic_din2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	ABEDMIC_DIN2_PULLUDENABLE	Pull-Up/Down enable for pad abedmic_din2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	ABEDMIC_DIN2_MUXMODE	Functional multiplexing selection for pad abedmic_din2 0x0: Select abedmic_din2 0x3: Select abemcasp_axr 0x4: Select abemcbsp3_dx 0x7: Select safe_mode_core143 0x6: Select gpio4_98	RW	0x7
15	ABEDMIC_DIN1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	ABEDMIC_DIN1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	ABEDMIC_DIN1_INPUTENABLE	Input enable value for pad abedmic_din1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	ABEDMIC_DIN1_PWRDOWN	Power Down setting for pad abedmic_din1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	ABEDMIC_DIN1_PULLTYPESELECT	Pull-Up/Down selection for pad abedmic_din1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	ABEDMIC_DIN1_PULLUDENABLE	Pull-Up/Down enable for pad abedmic_din1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	ABEDMIC_DIN1_MUXMODE	Functional multiplexing selection for pad abedmic_din1 0x0: Select abedmic_din1 0x3: Select abemcasp_ahclkr 0x4: Select abemcbsp3_fsx 0x7: Select safe_mode_core142 0x6: Select gpio4_97	RW	0x7

Table 18-635. Register Call Summary for Register CONTROL_CORE_PAD0_ABEDMIC_DIN1_PAD1_ABEDMIC_DIN2

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-636. CONTROL_CORE_PAD0_ABEDMIC_DIN3_PAD1_ABEDMIC_CLK1

Address Offset	0x0000 0188		
Physical Address	0x4A00 2988 0x4A00 2988	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads abedmic_din3 and abedmic_clk1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABEDMIC_CLK1_WAKEUPEVENT	ABEDMIC_CLK1_WAKEUPENABLE	RESERVED					ABEDMIC_CLK1_INPUTENABLE	RESERVED	ABEDMIC_CLK1_GLITCHGOBBLER	ABEDMIC_CLK1_PWRDOWN	ABEDMIC_CLK1_PULLTYPESELECT	ABEDMIC_CLK1_PULLUDENABLE	ABEDMIC_CLK1_MUXMODE			ABEDMIC_DIN3_WAKEUPEVENT	ABEDMIC_DIN3_WAKEUPENABLE	RESERVED					ABEDMIC_DIN3_INPUTENABLE	RESERVED			ABEDMIC_DIN3_PWRDOWN	ABEDMIC_DIN3_PULLTYPESELECT	ABEDMIC_DIN3_PULLUDENABLE	ABEDMIC_DIN3_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABEDMIC_CLK1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	ABEDMIC_CLK1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	ABEDMIC_CLK1_INPUTENABLE	Input enable value for pad abedmic_clk1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23	RESERVED		R	0
22	ABEDMIC_CLK1_GLITCHGOBBLER	Glitch Gobbler setting for pad abedmic_clk1 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
21	ABEDMIC_CLK1_PWRDOWN	Power Down setting for pad abedmic_clk1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	ABEDMIC_CLK1_PULLTYPESELECT	Pull-Up/Down selection for pad abedmic_clk1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	ABEDMIC_CLK1_PULLUDENABLE	Pull-Up/Down enable for pad abedmic_clk1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	ABEDMIC_CLK1_MUXMODE	Functional multiplexing selection for pad abedmic_clk1 0x0: Select abedmic_clk1 0x4: Select abemcbsp3_clkx 0x7: Select safe_mode_core145 0x6: Select gpio4_100	RW	0x7

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Bits	Field Name	Description	Type	Reset
15	ABEDMIC_DIN3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	ABEDMIC_DIN3_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	ABEDMIC_DIN3_INPUTENABLE	Input enable value for pad abedmic_din3 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	ABEDMIC_DIN3_PWRDOWN	Power Down setting for pad abedmic_din3 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	ABEDMIC_DIN3_PULLTYPESELECT	Pull-Up/Down selection for pad abedmic_din3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	ABEDMIC_DIN3_PULLUDENABLE	Pull-Up/Down enable for pad abedmic_din3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	ABEDMIC_DIN3_MUXMODE	Functional multiplexing selection for pad abedmic_din3 0x0: Select abedmic_din3 0x4: Select abemcbsp3_dr 0x7: Select safe_mode_core144 0x6: Select gpio4_99	RW	0x7

Table 18-637. Register Call Summary for Register CONTROL_CORE_PAD0_ABEDMIC_DIN3_PAD1_ABEDMIC_CLK1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-638. CONTROL_CORE_PAD0_ABEDMIC_CLK2_PAD1_ABEDMIC_CLK3

Address Offset	0x0000 018C		
Physical Address	0x4A00 298C 0x4A00 298C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads abedmic_clk2 and abedmic_clk3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABEDMIC_CLK3_WAKEUPEVENT	ABEDMIC_CLK3_WAKEUPENABLE	RESERVED					ABEDMIC_CLK3_INPUTENABLE	RESERVED		ABEDMIC_CLK3_PWRDOWN	ABEDMIC_CLK3_PULLTYPESELECT	ABEDMIC_CLK3_PULLUDENABLE	ABEDMIC_CLK3_MUXMODE			ABEDMIC_CLK2_WAKEUPEVENT	ABEDMIC_CLK2_WAKEUPENABLE	RESERVED					ABEDMIC_CLK2_INPUTENABLE	RESERVED		ABEDMIC_CLK2_PWRDOWN	ABEDMIC_CLK2_PULLTYPESELECT	ABEDMIC_CLK2_PULLUDENABLE	ABEDMIC_CLK2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABEDMIC_CLK3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	ABEDMIC_CLK3_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	ABEDMIC_CLK3_INPUTENABLE	Input enable value for pad abedmic_clk3 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	ABEDMIC_CLK3_PWRDOWN	Power Down setting for pad abedmic_clk3 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	ABEDMIC_CLK3_PULLTYPESELECT	Pull-Up/Down selection for pad abedmic_clk3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	ABEDMIC_CLK3_PULLUDENABLE	Pull-Up/Down enable for pad abedmic_clk3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	ABEDMIC_CLK3_MUXMODE	Functional multiplexing selection for pad abedmic_clk3 0x0: Select abedmic_clk3 0x1: Select abemcbsp1_dx 0x3: Select abemcasp_aclkx 0x7: Select safe_mode_core147 0x6: Select gpio4_102	RW	0x7
15	ABEDMIC_CLK2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	ABEDMIC_CLK2_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	ABEDMIC_CLK2_INPUTENABLE	Input enable value for pad abedmic_clk2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1

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Bits	Field Name	Description	Type	Reset
7:6	RESERVED		R	0x0
5	ABEDMIC_CLK2_PWRDOWN	Power Down setting for pad abedmic_clk2 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	ABEDMIC_CLK2_PULLTYPESELECT	Pull-Up/Down selection for pad abedmic_clk2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	ABEDMIC_CLK2_PULLUDENABLE	Pull-Up/Down enable for pad abedmic_clk2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	ABEDMIC_CLK2_MUXMODE	Functional multiplexing selection for pad abedmic_clk2 0x0: Select abedmic_clk2 0x1: Select abemcbsp1_fsx 0x3: Select abemcasp_amutein 0x7: Select safe_mode_core146 0x6: Select gpio4_101	RW	0x7

Table 18-639. Register Call Summary for Register CONTROL_CORE_PAD0_ABEDMIC_CLK2_PAD1_ABEDMIC_CLK3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-640. CONTROL_CORE_PAD0_ABESLIMBUS1_CLOCK_PAD1_ABESLIMBUS1_DATA

Address Offset	0x0000 0190		
Physical Address	0x4A00 2990 0x4A00 2990	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads abeslimbus1_clock and abeslimbus1_data Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABESLIMBUS1_DATA_WAKEUPEVENT	ABESLIMBUS1_DATA_WAKEUPENABLE	RESERVED					ABESLIMBUS1_DATA_INPUTENABLE	RESERVED		ABESLIMBUS1_DATA_PWRDOWN	ABESLIMBUS1_DATA_PULLTYPESELECT	ABESLIMBUS1_DATA_PULLUDENABLE	ABESLIMBUS1_DATA_MUXMODE			ABESLIMBUS1_CLOCK_WAKEUPEVENT	ABESLIMBUS1_CLOCK_WAKEUPENABLE	RESERVED					ABESLIMBUS1_CLOCK_INPUTENABLE	RESERVED	ABESLIMBUS1_CLOCK_GLITCHGOBBLER	ABESLIMBUS1_CLOCK_PWRDOWN	ABESLIMBUS1_CLOCK_PULLTYPESELECT	ABESLIMBUS1_CLOCK_PULLUDENABLE	ABESLIMBUS1_CLOCK_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	ABESLIMBUS1_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	ABESLIMBUS1_DATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	ABESLIMBUS1_DATA_INPUTENABLE	Input enable value for pad abeslimbus1_data 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	ABESLIMBUS1_DATA_PWRDOWN	Power Down setting for pad abeslimbus1_data 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	ABESLIMBUS1_DATA_PULLTYPESELECT	Pull-Up/Down selection for pad abeslimbus1_data 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	ABESLIMBUS1_DATA_PULLUDENABLE	Pull-Up/Down enable for pad abeslimbus1_data 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	ABESLIMBUS1_DATA_MUXMODE	Functional multiplexing selection for pad abeslimbus1_data 0x0: Select abeslimbus1_data 0x1: Select abemcbsp1_dr 0x3: Select abemcasp_aclkr 0x7: Select safe_mode_core149 0x6: Select gpio4_104	RW	0x7
15	ABESLIMBUS1_CLOCK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	ABESLIMBUS1_CLOCK_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	ABESLIMBUS1_CLOCK_INPUTENABLE	Input enable value for pad abeslimbus1_clock 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7	RESERVED		R	0
6	ABESLIMBUS1_CLOCK_GLITCHGOBBLER	Glitch Gobbler setting for pad abeslimbus1_clock 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
5	ABESLIMBUS1_CLOCK_PWRDOWN	Power Down setting for pad abeslimbus1_clock 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	ABESLIMBUS1_CLOCK_PULLTYPESELECT	Pull-Up/Down selection for pad abeslimbus1_clock 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0

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Bits	Field Name	Description	Type	Reset
3	ABESLIMBUS1_CLOCK_PULLUDENABLE	Pull-Up/Down enable for pad abeslimbus1_clock 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	ABESLIMBUS1_CLOCK_MUXMODE	Functional multiplexing selection for pad abeslimbus1_clock 0x0: Select abeslimbus1_clock 0x1: Select abemcbsp1_clkx 0x3: Select abemcasp_afsr 0x7: Select safe_mode_core148 0x6: Select gpio4_103	RW	0x7

Table 18-641. Register Call Summary for Register CONTROL_CORE_PAD0_ABESLIMBUS1_CLOCK_PAD1_ABESLIMBUS1_DATA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-642. CONTROL_CORE_PAD0_ABEMCBSP2_DR_PAD1_ABEMCBSP2_DX

Address Offset	0x0000 0194		
Physical Address	0x4A00 2994 0x4A00 2994	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads abemcbsp2_dr and abemcbsp2_dx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABEMCBSP2_DX_WAKEUPEVENT	ABEMCBSP2_DX_WAKEUPENABLE	RESERVED					ABEMCBSP2_DX_INPUTENABLE	RESERVED		ABEMCBSP2_DX_PWRDOWN	ABEMCBSP2_DX_PULLTYPESELECT	ABEMCBSP2_DX_PULLUDENABLE	ABEMCBSP2_DX_MUXMODE			ABEMCBSP2_DR_WAKEUPEVENT	ABEMCBSP2_DR_WAKEUPENABLE	RESERVED					ABEMCBSP2_DR_INPUTENABLE	RESERVED		ABEMCBSP2_DR_PWRDOWN	ABEMCBSP2_DR_PULLTYPESELECT	ABEMCBSP2_DR_PULLUDENABLE	ABEMCBSP2_DR_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABEMCBSP2_DX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	ABEMCBSP2_DX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
24	ABEMCBSP2_DX_INPUTENABLE	Input enable value for pad abemcbsp2_dx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	ABEMCBSP2_DX_PWRDOWN	Power Down setting for pad abemcbsp2_dx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	ABEMCBSP2_DX_PULLTYPESELECT	Pull-Up/Down selection for pad abemcbsp2_dx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	ABEMCBSP2_DX_PULLUDENABLE	Pull-Up/Down enable for pad abemcbsp2_dx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	ABEMCBSP2_DX_MUXMODE	Functional multiplexing selection for pad abemcbsp2_dx 0x0: Select abemcbsp2_dx 0x3: Select abemcasp_amuteout 0x7: Select safe_mode_core151 0x6: Select gpio4_106	RW	0x7
15	ABEMCBSP2_DR_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	ABEMCBSP2_DR_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	ABEMCBSP2_DR_INPUTENABLE	Input enable value for pad abemcbsp2_dr 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	ABEMCBSP2_DR_PWRDOWN	Power Down setting for pad abemcbsp2_dr 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	ABEMCBSP2_DR_PULLTYPESELECT	Pull-Up/Down selection for pad abemcbsp2_dr 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	ABEMCBSP2_DR_PULLUDENABLE	Pull-Up/Down enable for pad abemcbsp2_dr 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	ABEMCBSP2_DR_MUXMODE	Functional multiplexing selection for pad abemcbsp2_dr 0x0: Select abemcbsp2_dr 0x3: Select abemcasp_axr 0x7: Select safe_mode_core150 0x6: Select gpio4_105	RW	0x7

Table 18-643. Register Call Summary for Register CONTROL_CORE_PAD0_ABEMCBSP2_DR_PAD1_ABEMCBSP2_DX

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-643. Register Call Summary for Register CONTROL_CORE_PAD0_ABEMCBSP2_DR_PAD1_ABEMCBSP2_DX (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-644. CONTROL_CORE_PAD0_ABEMCBSP2_FSX_PAD1_ABEMCBSP2_CLKX

Address Offset	0x0000 0198		
Physical Address	0x4A00 2998 0x4A00 2998	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads abemcbsp2_fsx and abemcbsp2_clkx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABEMCBSP2_CLKX_WAKEUPEVENT	ABEMCBSP2_CLKX_WAKEUPENABLE	RESERVED					ABEMCBSP2_CLKX_INPUTENABLE	RESERVED	ABEMCBSP2_CLKX_GLITCHGOBBLER	ABEMCBSP2_CLKX_PWRDOWN	ABEMCBSP2_CLKX_PULLTYPESELECT	ABEMCBSP2_CLKX_PULLUDENABLE	ABEMCBSP2_CLKX_MUXMODE			ABEMCBSP2_FSX_WAKEUPEVENT	ABEMCBSP2_FSX_WAKEUPENABLE	RESERVED					ABEMCBSP2_FSX_INPUTENABLE	RESERVED	ABEMCBSP2_FSX_PWRDOWN	ABEMCBSP2_FSX_PULLTYPESELECT	ABEMCBSP2_FSX_PULLUDENABLE	ABEMCBSP2_FSX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABEMCBSP2_CLKX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	ABEMCBSP2_CLKX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	ABEMCBSP2_CLKX_INPUTENABLE	Input enable value for pad abemcbsp2_clkx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23	RESERVED		R	0
22	ABEMCBSP2_CLKX_GLITCHGOBBLER	Glitch Gobbler setting for pad abemcbsp2_clkx 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
21	ABEMCBSP2_CLKX_PWRDOWN	Power Down setting for pad abemcbsp2_clkx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	ABEMCBSP2_CLKX_PULLTYPESELECT	Pull-Up/Down selection for pad abemcbsp2_clkx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0

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Bits	Field Name	Description	Type	Reset
19	ABEMCBSP2_CLKX_PULLUDENABLE	Pull-Up/Down enable for pad abemcbsp2_clkx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	ABEMCBSP2_CLKX_MUXMODE	Functional multiplexing selection for pad abemcbsp2_clkx 0x0: Select abemcbsp2_clkx 0x3: Select abemcasp_ahclkx 0x7: Select safe_mode_core153 0x6: Select gpio4_108	RW	0x7
15	ABEMCBSP2_FSX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	ABEMCBSP2_FSX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	ABEMCBSP2_FSX_INPUTENABLE	Input enable value for pad abemcbsp2_fsx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	ABEMCBSP2_FSX_PWRDOWN	Power Down setting for pad abemcbsp2_fsx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	ABEMCBSP2_FSX_PULLTYPESELECT	Pull-Up/Down selection for pad abemcbsp2_fsx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	ABEMCBSP2_FSX_PULLUDENABLE	Pull-Up/Down enable for pad abemcbsp2_fsx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	ABEMCBSP2_FSX_MUXMODE	Functional multiplexing selection for pad abemcbsp2_fsx 0x0: Select abemcbsp2_fsx 0x3: Select abemcasp_afsx 0x7: Select safe_mode_core152 0x6: Select gpio4_107	RW	0x7

Table 18-645. Register Call Summary for Register CONTROL_CORE_PAD0_ABEMCBSP2_FSX_PAD1_ABEMCBSP2_CLKX

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-646. CONTROL_CORE_PAD0_ABEMCPDM_UL_DATA_PAD1_ABEMCPDM_DL_DATA

Address Offset	0x0000 019C		
Physical Address	0x4A00 299C 0x4A00 299C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads abemcpdm_ul_data and abemcpdm_dl_data Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABEMCPDM_DL_DATA_WAKEUPEVENT	ABEMCPDM_DL_DATA_WAKEUPENABLE	RESERVED					ABEMCPDM_DL_DATA_INPUTENABLE	RESERVED		ABEMCPDM_DL_DATA_PWRDOWN	ABEMCPDM_DL_DATA_PULLTYPESELECT	ABEMCPDM_DL_DATA_PULLUDENABLE	ABEMCPDM_DL_DATA_MUXMODE			ABEMCPDM_UL_DATA_WAKEUPEVENT	ABEMCPDM_UL_DATA_WAKEUPENABLE	RESERVED					ABEMCPDM_UL_DATA_INPUTENABLE	RESERVED		ABEMCPDM_UL_DATA_PWRDOWN	ABEMCPDM_UL_DATA_PULLTYPESELECT	ABEMCPDM_UL_DATA_PULLUDENABLE	ABEMCPDM_UL_DATA_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	ABEMCPDM_DL_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	ABEMCPDM_DL_DATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	ABEMCPDM_DL_DATA_INPUTENABLE	Input enable value for pad abemcpdm_dl_data 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	ABEMCPDM_DL_DATA_PWRDOWN	Power Down setting for pad abemcpdm_dl_data 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	ABEMCPDM_DL_DATA_PULLTYPESELECT	Pull-Up/Down selection for pad abemcpdm_dl_data 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	ABEMCPDM_DL_DATA_PULLUDENABLE	Pull-Up/Down enable for pad abemcpdm_dl_data 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	ABEMCPDM_DL_DATA_MUXMODE	Functional multiplexing selection for pad abemcpdm_dl_data 0x0: Select abemcpdm_dl_data 0x1: Select abemcbsp3_dx 0x3: Select abemcasp_axr2 0x7: Select safe_mode_core155 0x6: Select gpio4_110	RW	0x7
15	ABEMCPDM_UL_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	ABEMCPDM_UL_DATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
8	ABEMCPDM_UL_DATA_INPUTENABLE	Input enable value for pad abemcpdm_ul_data 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	ABEMCPDM_UL_DATA_PWRDOWN	Power Down setting for pad abemcpdm_ul_data 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	ABEMCPDM_UL_DATA_PULLTYPESELECT	Pull-Up/Down selection for pad abemcpdm_ul_data 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	ABEMCPDM_UL_DATA_PULLUDENABLE	Pull-Up/Down enable for pad abemcpdm_ul_data 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	ABEMCPDM_UL_DATA_MUXMODE	Functional multiplexing selection for pad abemcpdm_ul_data 0x0: Select abemcpdm_ul_data 0x1: Select abemcbsp3_dr 0x3: Select abemcasp_axr3 0x7: Select safe_mode_core154 0x6: Select gpio4_109	RW	0x7

Table 18-647. Register Call Summary for Register CONTROL_CORE_PAD0_ABEMCPDM_UL_DATA_PAD1_ABEMCPDM_DL_DATA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-648. CONTROL_CORE_PAD0_ABEMCPDM_FRAME_PAD1_ABEMCPDM_LB_CLK

Address Offset	0x0000 01A0		
Physical Address	0x4A00 29A0 0x4A00 29A0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads abemcpdm_frame and abemcpdm_lb_clk Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABEMCPDM_LB_CLK_WAKEUPEVENT	ABEMCPDM_LB_CLK_WAKEUPENABLE	RESERVED					ABEMCPDM_LB_CLK_INPUTENABLE	RESERVED		ABEMCPDM_LB_CLK_PWRDOWN	ABEMCPDM_LB_CLK_PULLTYPESELECT	ABEMCPDM_LB_CLK_PULLUDENABLE	ABEMCPDM_LB_CLK_MUXMODE			ABEMCPDM_FRAME_WAKEUPEVENT	ABEMCPDM_FRAME_WAKEUPENABLE	RESERVED					ABEMCPDM_FRAME_INPUTENABLE	RESERVED	ABEMCPDM_FRAME_GLITCHGOBBLER	ABEMCPDM_FRAME_PWRDOWN	ABEMCPDM_FRAME_PULLTYPESELECT	ABEMCPDM_FRAME_PULLUDENABLE	ABEMCPDM_FRAME_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	ABEMCPDM_LB_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	ABEMCPDM_LB_CLK_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	ABEMCPDM_LB_CLK_INPUTENABLE	Input enable value for pad abemcpdm_lb_clk 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	ABEMCPDM_LB_CLK_PWRDOWN	Power Down setting for pad abemcpdm_lb_clk 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	ABEMCPDM_LB_CLK_PULLTYPESELECT	Pull-Up/Down selection for pad abemcpdm_lb_clk 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	ABEMCPDM_LB_CLK_PULLUDENABLE	Pull-Up/Down enable for pad abemcpdm_lb_clk 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	ABEMCPDM_LB_CLK_MUXMODE	Functional multiplexing selection for pad abemcpdm_lb_clk 0x0: Select abemcpdm_lb_clk 0x1: Select abemcbsp3_fsx 0x7: Select safe_mode_core157 0x6: Select gpio4_112	RW	0x7
15	ABEMCPDM_FRAME_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	ABEMCPDM_FRAME_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	ABEMCPDM_FRAME_INPUTENABLE	Input enable value for pad abemcpdm_frame 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7	RESERVED		R	0
6	ABEMCPDM_FRAME_GLITCHGOBBLER	Glitch Gobbler setting for pad abemcpdm_frame 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
5	ABEMCPDM_FRAME_PWRDOWN	Power Down setting for pad abemcpdm_frame 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	ABEMCPDM_FRAME_PULLTYPESELECT	Pull-Up/Down selection for pad abemcpdm_frame 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	ABEMCPDM_FRAME_PULLUDENABLE	Pull-Up/Down enable for pad abemcpdm_frame 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	ABEMCPDM_FRAME_MUXMODE	Functional multiplexing selection for pad abemcpdm_frame 0x0: Select abemcpdm_frame 0x1: Select abemcbsp3_clkx 0x3: Select abemcasp_axr1 0x7: Select safe_mode_core156 0x6: Select gpio4_111	RW	0x7

Table 18-649. Register Call Summary for Register CONTROL_CORE_PAD0_ABEMCPDM_FRAME_PAD1_ABEMCPDM_LB_CLK

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-650. CONTROL_CORE_PAD0_WLSDIO_CLK_PAD1_WLSDIO_CMD

Address Offset	0x0000 01A4		
Physical Address	0x4A00 29A4 0x4A00 29A4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads wlsdio_clk and wlsdio_cmd Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WLSDIO_CMD_WAKEUPEVENT	WLSDIO_CMD_WAKEUPENABLE	RESERVED					WLSDIO_CMD_INPUTENABLE	RESERVED		WLSDIO_CMD_PWRDOWN	WLSDIO_CMD_PULLTYPESELECT	WLSDIO_CMD_PULLUDENABLE	WLSDIO_CMD_MUXMODE			RESERVED							WLSDIO_CLK_INPUTENABLE	RESERVED	WLSDIO_CLK_GLITCHGOBBLER	WLSDIO_CLK_PWRDOWN	WLSDIO_CLK_PULLTYPESELECT	WLSDIO_CLK_PULLUDENABLE	WLSDIO_CLK_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	WLSDIO_CMD_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	WLSDIO_CMD_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	WLSDIO_CMD_INPUTENABLE	Input enable value for pad wlsdio_cmd 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	WLSDIO_CMD_PWRDOWN	Power Down setting for pad wlsdio_cmd 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	WLSDIO_CMD_PULLTYPESELECT	Pull-Up/Down selection for pad wlsdio_cmd 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	WLSDIO_CMD_PULLUDENABLE	Pull-Up/Down enable for pad wlsdio_cmd 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	WLSDIO_CMD_MUXMODE	Functional multiplexing selection for pad wlsdio_cmd 0x0: Select wlsdio_cmd 0x7: Select safe_mode_core159 0x6: Select gpio5_129	RW	0x7
15:9	RESERVED		R	0x0
8	WLSDIO_CLK_INPUTENABLE	Input enable value for pad wlsdio_clk 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7	RESERVED		R	0
6	WLSDIO_CLK_GLITCHGOBBLER	Glitch Gobbler setting for pad wlsdio_clk 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
5	WLSDIO_CLK_PWRDOWN	Power Down setting for pad wlsdio_clk 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	WLSDIO_CLK_PULLTYPESELECT	Pull-Up/Down selection for pad wlsdio_clk 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	WLSDIO_CLK_PULLUDENABLE	Pull-Up/Down enable for pad wlsdio_clk 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	WLSDIO_CLK_MUXMODE	Functional multiplexing selection for pad wlsdio_clk 0x0: Select wlsdio_clk 0x1: Select mcspi4_clk 0x7: Select safe_mode_core158 0x6: Select gpio5_128[1]	RW	0x7

[1] (1) The wlsdio_clk pad cannot wake – up the device when configured as gpio5_128.

Table 18-651. Register Call Summary for Register CONTROL_CORE_PAD0_WLSDIO_CLK_PAD1_WLSDIO_CMD

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-652. CONTROL_CORE_PAD0_WLSDIO_DATA0_PAD1_WLSDIO_DATA1

Address Offset	0x0000 01A8		
Physical Address	0x4A00 29A8 0x4A00 29A8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads wlsdio_data0 and wlsdio_data1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WLSDIO_DATA1_WAKEUPEVENT	WLSDIO_DATA1_WAKEUPENABLE	RESERVED					WLSDIO_DATA1_INPUTENABLE	RESERVED		WLSDIO_DATA1_PWRDOWN	WLSDIO_DATA1_PULLTYPESELECT	WLSDIO_DATA1_PULLUDENABLE	WLSDIO_DATA1_MUXMODE			WLSDIO_DATA0_WAKEUPEVENT	WLSDIO_DATA0_WAKEUPENABLE	RESERVED					WLSDIO_DATA0_INPUTENABLE	RESERVED		WLSDIO_DATA0_PWRDOWN	WLSDIO_DATA0_PULLTYPESELECT	WLSDIO_DATA0_PULLUDENABLE	WLSDIO_DATA0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	WLSDIO_DATA1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	WLSDIO_DATA1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	WLSDIO_DATA1_INPUTENABLE	Input enable value for pad wlsdio_data1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	WLSDIO_DATA1_PWRDOWN	Power Down setting for pad wlsdio_data1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	WLSDIO_DATA1_PULLTYPESELECT	Pull-Up/Down selection for pad wlsdio_data1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	WLSDIO_DATA1_PULLUDENABLE	Pull-Up/Down enable for pad wlsdio_data1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	WLSDIO_DATA1_MUXMODE	Functional multiplexing selection for pad wlsdio_data1 0x0: Select wlsdio_data1 0x1: Select mcspi4_somi 0x7: Select safe_mode_core161 0x6: Select gpio5_131	RW	0x7
15	WLSDIO_DATA0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	WLSDIO_DATA0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	WLSDIO_DATA0_INPUTENABLE	Input enable value for pad wlsdio_data0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	WLSDIO_DATA0_PWRDOWN	Power Down setting for pad wlsdio_data0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	WLSDIO_DATA0_PULLTYPESELECT	Pull-Up/Down selection for pad wlsdio_data0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	WLSDIO_DATA0_PULLUDENABLE	Pull-Up/Down enable for pad wlsdio_data0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	WLSDIO_DATA0_MUXMODE	Functional multiplexing selection for pad wlsdio_data0 0x0: Select wlsdio_data0 0x1: Select mcspi4_simo 0x7: Select safe_mode_core160 0x6: Select gpio5_130	RW	0x7

Table 18-653. Register Call Summary for Register CONTROL_CORE_PAD0_WLSDIO_DATA0_PAD1_WLSDIO_DATA1

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-654. CONTROL_CORE_PAD0_WLSDIO_DATA2_PAD1_WLSDIO_DATA3

Address Offset	0x0000 01AC		
Physical Address	0x4A00 29AC 0x4A00 29AC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads wlsdio_data2 and wlsdio_data3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WLSDIO_DATA3_WAKEUPEVENT	WLSDIO_DATA3_WAKEUPENABLE	RESERVED					WLSDIO_DATA3_INPUTENABLE	RESERVED		WLSDIO_DATA3_PWRDOWN	WLSDIO_DATA3_PULLTYPESELECT	WLSDIO_DATA3_PULLUDENABLE	WLSDIO_DATA3_MUXMODE			WLSDIO_DATA2_WAKEUPEVENT	WLSDIO_DATA2_WAKEUPENABLE	RESERVED					WLSDIO_DATA2_INPUTENABLE	RESERVED		WLSDIO_DATA2_PWRDOWN	WLSDIO_DATA2_PULLTYPESELECT	WLSDIO_DATA2_PULLUDENABLE	WLSDIO_DATA2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	WLSDIO_DATA3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	WLSDIO_DATA3_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	WLSDIO_DATA3_INPUTENABLE	Input enable value for pad wlsdio_data3 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	WLSDIO_DATA3_PWRDOWN	Power Down setting for pad wlsdio_data3 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	WLSDIO_DATA3_PULLTYPESELECT	Pull-Up/Down selection for pad wlsdio_data3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	WLSDIO_DATA3_PULLUDENABLE	Pull-Up/Down enable for pad wlsdio_data3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	WLSDIO_DATA3_MUXMODE	Functional multiplexing selection for pad wlsdio_data3 0x0: Select wlsdio_data3 0x7: Select safe_mode_core163 0x6: Select gpio5_133	RW	0x7
15	WLSDIO_DATA2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	WLSDIO_DATA2_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	WLSDIO_DATA2_INPUTENABLE	Input enable value for pad wlsdio_data2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	WLSDIO_DATA2_PWRDOWN	Power Down setting for pad wlsdio_data2 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	WLSDIO_DATA2_PULLTYPESELECT	Pull-Up/Down selection for pad wlsdio_data2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	WLSDIO_DATA2_PULLUDENABLE	Pull-Up/Down enable for pad wlsdio_data2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	WLSDIO_DATA2_MUXMODE	Functional multiplexing selection for pad wlsdio_data2 0x0: Select wlsdio_data2 0x1: Select mcspi4_cs0 0x7: Select safe_mode_core162 0x6: Select gpio5_132	RW	0x7

Table 18-655. Register Call Summary for Register CONTROL_CORE_PAD0_WLSDIO_DATA2_PAD1_WLSDIO_DATA3

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-656. CONTROL_CORE_PAD0_UART5_RX_PAD1_UART5_TX

Address Offset	0x0000 01B0		
Physical Address	0x4A00 29B0 0x4A00 29B0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart5_rx and uart5_tx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART5_TX_WAKEUPEVENT	UART5_TX_WAKEUPENABLE	RESERVED					UART5_TX_INPUTENABLE	RESERVED		UART5_TX_PWRDOWN	UART5_TX_PULLTYPESELECT	UART5_TX_PULLUDENABLE	UART5_TX_MUXMODE			UART5_RX_WAKEUPEVENT	UART5_RX_WAKEUPENABLE	RESERVED					UART5_RX_INPUTENABLE	RESERVED		UART5_RX_PWRDOWN	UART5_RX_PULLTYPESELECT	UART5_RX_PULLUDENABLE	UART5_RX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART5_TX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART5_TX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
24	UART5_TX_INPUTENABLE	Input enable value for pad uart5_tx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	UART5_TX_PWRDOWN	Power Down setting for pad uart5_tx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	UART5_TX_PULLTYPESELECT	Pull-Up/Down selection for pad uart5_tx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART5_TX_PULLUDENABLE	Pull-Up/Down enable for pad uart5_tx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	UART5_TX_MUXMODE	Functional multiplexing selection for pad uart5_tx 0x0: Select uart5_tx 0x6: Select gpio5_135 0x4: Select sdio4_data2 0x7: Select safe_mode_core165 0x5: Select hw_dbg29	RW	0x7
15	UART5_RX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART5_RX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	UART5_RX_INPUTENABLE	Input enable value for pad uart5_rx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	UART5_RX_PWRDOWN	Power Down setting for pad uart5_rx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART5_RX_PULLTYPESELECT	Pull-Up/Down selection for pad uart5_rx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	UART5_RX_PULLUDENABLE	Pull-Up/Down enable for pad uart5_rx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART5_RX_MUXMODE	Functional multiplexing selection for pad uart5_rx 0x0: Select uart5_rx 0x6: Select gpio5_134 0x4: Select sdio4_data1 0x7: Select safe_mode_core164 0x5: Select hw_dbg28	RW	0x7

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Table 18-657. Register Call Summary for Register CONTROL_CORE_PAD0_UART5_RX_PAD1_UART5_TX

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [3]

Table 18-658. CONTROL_CORE_PAD0_UART5_CTS_PAD1_UART5_RTS

Address Offset	0x0000 01B4		
Physical Address	0x4A00 29B4 0x4A00 29B4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart5_cts and uart5_rts Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART5_RTS_WAKEUPEVENT	UART5_RTS_WAKEUPENABLE	RESERVED					UART5_RTS_INPUTENABLE	RESERVED		UART5_RTS_PWRDOWN	UART5_RTS_PULLTYPESELECT	UART5_RTS_PULLUDENABLE	UART5_RTS_MUXMODE			UART5_CTS_WAKEUPEVENT	UART5_CTS_WAKEUPENABLE	RESERVED					UART5_CTS_INPUTENABLE	RESERVED		UART5_CTS_PWRDOWN	UART5_CTS_PULLTYPESELECT	UART5_CTS_PULLUDENABLE	UART5_CTS_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART5_RTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART5_RTS_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	UART5_RTS_INPUTENABLE	Input enable value for pad uart5_rts 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	UART5_RTS_PWRDOWN	Power Down setting for pad uart5_rts 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	UART5_RTS_PULLTYPESELECT	Pull-Up/Down selection for pad uart5_rts 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART5_RTS_PULLUDENABLE	Pull-Up/Down enable for pad uart5_rts 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	UART5_RTS_MUXMODE	Functional multiplexing selection for pad uart5_rts 0x0: Select uart5_rts 0x6: Select gpio5_137 0x4: Select sdio4_data3 0x7: Select safe_mode_core167 0x5: Select hw_dbg31	RW	0x7
15	UART5_CTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART5_CTS_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	UART5_CTS_INPUTENABLE	Input enable value for pad uart5_cts 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	UART5_CTS_PWRDOWN	Power Down setting for pad uart5_cts 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART5_CTS_PULLTYPESELECT	Pull-Up/Down selection for pad uart5_cts 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	UART5_CTS_PULLUDENABLE	Pull-Up/Down enable for pad uart5_cts 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART5_CTS_MUXMODE	Functional multiplexing selection for pad uart5_cts 0x0: Select uart5_cts 0x6: Select gpio5_136 0x4: Select sdio4_data0 0x7: Select safe_mode_core166 0x5: Select hw_dbg30	RW	0x7

Table 18-659. Register Call Summary for Register CONTROL_CORE_PAD0_UART5_CTS_PAD1_UART5_RTS

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the CORE Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [3]

Table 18-660. CONTROL_CORE_PAD0_I2C2_SCL_PAD1_I2C2_SDA

Address Offset	0x0000 01B8		
Physical Address	0x4A00 29B8 0x4A00 29B8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads i2c2_scl and i2c2_sda Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C2_SDA_WAKEUPEVENT	I2C2_SDA_WAKEUPENABLE	RESERVED					I2C2_SDA_INPUTENABLE	RESERVED		I2C2_SDA_PWRDOWN	I2C2_SDA_PULLTYPESELECT	I2C2_SDA_PULLUDENABLE	I2C2_SDA_MUXMODE			I2C2_SCL_WAKEUPEVENT	I2C2_SCL_WAKEUPENABLE	RESERVED					I2C2_SCL_INPUTENABLE	RESERVED	I2C2_SCL_GLITCHGOBBLER	I2C2_SCL_PWRDOWN	I2C2_SCL_PULLTYPESELECT	I2C2_SCL_PULLUDENABLE	I2C2_SCL_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	I2C2_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	I2C2_SDA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	I2C2_SDA_INPUTENABLE	Input enable value for pad i2c2_sda 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	I2C2_SDA_PWRDOWN	Power Down setting for pad i2c2_sda 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	I2C2_SDA_PULLTYPESELECT	Pull-Up/Down selection for pad i2c2_sda 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	I2C2_SDA_PULLUDENABLE	Pull-Up/Down enable for pad i2c2_sda 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	I2C2_SDA_MUXMODE	Functional multiplexing selection for pad i2c2_sda 0x0: Select i2c2_sda 0x7: Select safe_mode_core169 0x6: Select gpio5_139	RW	0x7
15	I2C2_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	I2C2_SCL_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	I2C2_SCL_INPUTENABLE	Input enable value for pad i2c2_scl 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7	RESERVED		R	0
6	I2C2_SCL_GLITCHGOBBLER	Glitch Gobbler setting for pad i2c2_scl 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0

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Bits	Field Name	Description	Type	Reset
5	I2C2_SCL_PWRDOWN	Power Down setting for pad i2c2_scl 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	I2C2_SCL_PULLTYPESELECT	Pull-Up/Down selection for pad i2c2_scl 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	I2C2_SCL_PULLUDENABLE	Pull-Up/Down enable for pad i2c2_scl 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	I2C2_SCL_MUXMODE	Functional multiplexing selection for pad i2c2_scl 0x0: Select i2c2_scl 0x7: Select safe_mode_core168 0x6: Select gpio5_138	RW	0x7

Table 18-661. Register Call Summary for Register CONTROL_CORE_PAD0_I2C2_SCL_PAD1_I2C2_SDA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-662. CONTROL_CORE_PAD0_MCSPI1_CLK_PAD1_MCSPI1_SOMI

Address Offset	0x0000 01BC		
Physical Address	0x4A00 29BC 0x4A00 29BC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads mcspi1_clk and mcspi1_somi Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI1_SOMI_WAKEUPEVENT	MCSPI1_SOMI_WAKEUPENABLE	RESERVED					MCSPI1_SOMI_INPUTENABLE	RESERVED		MCSPI1_SOMI_PWRDOWN	MCSPI1_SOMI_PULLTYPESELECT	MCSPI1_SOMI_PULLUDENABLE	MCSPI1_SOMI_MUXMODE			MCSPI1_CLK_WAKEUPEVENT	MCSPI1_CLK_WAKEUPENABLE	RESERVED					MCSPI1_CLK_INPUTENABLE	RESERVED	MCSPI1_CLK_GLITCHGOBBLER	MCSPI1_CLK_PWRDOWN	MCSPI1_CLK_PULLTYPESELECT	MCSPI1_CLK_PULLUDENABLE	MCSPI1_CLK_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	MCSPI1_SOMI_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	MCSPI1_SOMI_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
24	MCSPI1_SOMI_INPUTENABLE	Input enable value for pad mcspi1_somi 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	MCSPI1_SOMI_PWRDOWN	Power Down setting for pad mcspi1_somi 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	MCSPI1_SOMI_PULLTYPESELECT	Pull-Up/Down selection for pad mcspi1_somi 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	MCSPI1_SOMI_PULLUDENABLE	Pull-Up/Down enable for pad mcspi1_somi 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	MCSPI1_SOMI_MUXMODE	Functional multiplexing selection for pad mcspi1_somi 0x0: Select mcspi1_somi 0x6: Select gpio5_141 0x7: Select safe_mode_core171 0x5: Select usbd0_ulpiphy_nxt	RW	0x7
15	MCSPI1_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	MCSPI1_CLK_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	MCSPI1_CLK_INPUTENABLE	Input enable value for pad mcspi1_clk 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7	RESERVED		R	0
6	MCSPI1_CLK_GLITCHGOBBLER	Glitch Gobbler setting for pad mcspi1_clk 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
5	MCSPI1_CLK_PWRDOWN	Power Down setting for pad mcspi1_clk 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	MCSPI1_CLK_PULLTYPESELECT	Pull-Up/Down selection for pad mcspi1_clk 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	MCSPI1_CLK_PULLUDENABLE	Pull-Up/Down enable for pad mcspi1_clk 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	MCSPI1_CLK_MUXMODE	Functional multiplexing selection for pad mcspi1_clk 0x0: Select mcspi1_clk 0x6: Select gpio5_140 0x7: Select safe_mode_core170 0x5: Select usbd0_ulpiphy_clk	RW	0x7

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Table 18-663. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI1_CLK_PAD1_MCSPI1_SOMI

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-664. CONTROL_CORE_PAD0_MCSPI1_SIMO_PAD1_MCSPI1_CS0

Address Offset	0x0000 01C0		
Physical Address	0x4A00 29C0 0x4A00 29C0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads mcspi1_simo and mcspi1_cs0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCSPI1_CS0_WAKEUPEVENT	MCSPI1_CS0_WAKEUPENABLE	RESERVED					MCSPI1_CS0_INPUTENABLE	RESERVED		MCSPI1_CS0_PWRDOWN	MCSPI1_CS0_PULLTYPESELECT	MCSPI1_CS0_PULLUDENABLE	MCSPI1_CS0_MUXMODE			MCSPI1_SIMO_WAKEUPEVENT	MCSPI1_SIMO_WAKEUPENABLE	RESERVED					MCSPI1_SIMO_INPUTENABLE	RESERVED		MCSPI1_SIMO_PWRDOWN	MCSPI1_SIMO_PULLTYPESELECT	MCSPI1_SIMO_PULLUDENABLE	MCSPI1_SIMO_MUXMODE				

Bits	Field Name	Description	Type	Reset
31	MCSPI1_CS0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	MCSPI1_CS0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	MCSPI1_CS0_INPUTENABLE	Input enable value for pad mcspi1_cs0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	MCSPI1_CS0_PWRDOWN	Power Down setting for pad mcspi1_cs0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	MCSPI1_CS0_PULLTYPESELECT	Pull-Up/Down selection for pad mcspi1_cs0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	MCSPI1_CS0_PULLUDENABLE	Pull-Up/Down enable for pad mcspi1_cs0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	MCSPI1_CS0_MUXMODE	Functional multiplexing selection for pad mcspi1_cs0 0x0: Select mcspi1_cs0 0x6: Select gpio5_143 0x7: Select safe_mode_core173 0x5: Select usbd0_ulpiphy_data0	RW	0x7
15	MCSPI1_SIMO_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	MCSPI1_SIMO_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	MCSPI1_SIMO_INPUTENABLE	Input enable value for pad mcspi1_simo 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	MCSPI1_SIMO_PWRDOWN	Power Down setting for pad mcspi1_simo 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	MCSPI1_SIMO_PULLTYPESELECT	Pull-Up/Down selection for pad mcspi1_simo 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	MCSPI1_SIMO_PULLUDENABLE	Pull-Up/Down enable for pad mcspi1_simo 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	MCSPI1_SIMO_MUXMODE	Functional multiplexing selection for pad mcspi1_simo 0x0: Select mcspi1_simo 0x6: Select gpio5_142 0x7: Select safe_mode_core172 0x5: Select usbd0_ulpiphy_dir	RW	0x7

Table 18-665. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI1_SIMO_PAD1_MCSPI1_CS0

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-666. CONTROL_CORE_PAD0_MCSPI1_CS1_PAD1_I2C5_SCL

Address Offset	0x0000 01C4		
Physical Address	0x4A00 29C4 0x4A00 29C4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads mcspi1_cs1 and i2c5_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C5_SCL_WAKEUPEVENT	I2C5_SCL_WAKEUPENABLE	RESERVED					I2C5_SCL_INPUTENABLE	RESERVED		I2C5_SCL_PWRDOWN	I2C5_SCL_PULLTYPESELECT	I2C5_SCL_PULLUDENABLE	I2C5_SCL_MUXMODE			MCSPI1_CS1_WAKEUPEVENT	MCSPI1_CS1_WAKEUPENABLE	RESERVED					MCSPI1_CS1_INPUTENABLE	RESERVED		MCSPI1_CS1_PWRDOWN	MCSPI1_CS1_PULLTYPESELECT	MCSPI1_CS1_PULLUDENABLE	MCSPI1_CS1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	I2C5_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	I2C5_SCL_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	I2C5_SCL_INPUTENABLE	Input enable value for pad i2c5_scl 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	I2C5_SCL_PWRDOWN	Power Down setting for pad i2c5_scl 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	I2C5_SCL_PULLTYPESELECT	Pull-Up/Down selection for pad i2c5_scl 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	I2C5_SCL_PULLUDENABLE	Pull-Up/Down enable for pad i2c5_scl 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	I2C5_SCL_MUXMODE	Functional multiplexing selection for pad i2c5_scl 0x0: Select i2c5_scl 0x6: Select gpio5_147 0x7: Select safe_mode_core175 0x2: Select uart4_rx	RW	0x7
15	MCSPI1_CS1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	MCSPI1_CS1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	MCSPI1_CS1_INPUTENABLE	Input enable value for pad mcspi1_cs1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
5	MCSPI1_CS1_PWRDOWN	Power Down setting for pad mcspi1_cs1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	MCSPI1_CS1_PULLTYPESELECT	Pull-Up/Down selection for pad mcspi1_cs1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	MCSPI1_CS1_PULLUDENABLE	Pull-Up/Down enable for pad mcspi1_cs1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	MCSPI1_CS1_MUXMODE	Functional multiplexing selection for pad mcspi1_cs1 0x0: Select mcspi1_cs1 0x6: Select gpio5_144 0x7: Select safe_mode_core174 0x5: Select usbd0_ulpiphy_data1	RW	0x7

Table 18-667. Register Call Summary for Register CONTROL_CORE_PAD0_MCSPI1_CS1_PAD1_I2C5_SCL

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-668. CONTROL_CORE_PAD0_I2C5_SDA_PAD1_GPIO5_145

Address Offset	0x0000 01C8		
Physical Address	0x4A00 29C8 0x4A00 29C8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads i2c5_sda and gpio5_145 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO5_145_WAKEUPEVENT	GPIO5_145_WAKEUPENABLE	RESERVED					GPIO5_145_INPUTENABLE	RESERVED	GPIO5_145_GLITCHGOBBLER	GPIO5_145_PWRDOWN	GPIO5_145_PULLTYPESELECT	GPIO5_145_PULLUDENABLE	GPIO5_145_MUXMODE			I2C5_SDA_WAKEUPEVENT	I2C5_SDA_WAKEUPENABLE	RESERVED					I2C5_SDA_INPUTENABLE	RESERVED			I2C5_SDA_PWRDOWN	I2C5_SDA_PULLTYPESELECT	I2C5_SDA_PULLUDENABLE	I2C5_SDA_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPIO5_145_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPIO5_145_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29:25	RESERVED		R	0x0
24	GPIO5_145_INPUTENABLE	Input enable value for pad gpio5_145 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23	RESERVED		R	0
22	GPIO5_145_GLITCHGOBBLER	Glitch Gobbler setting for pad gpio5_145 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
21	GPIO5_145_PWRDOWN	Power Down setting for pad gpio5_145 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	GPIO5_145_PULLTYPESELECT	Pull-Up/Down selection for pad gpio5_145 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	GPIO5_145_PULLUDENABLE	Pull-Up/Down enable for pad gpio5_145 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPIO5_145_MUXMODE	Functional multiplexing selection for pad gpio5_145 0x6: Select gpio5_145 0x1: Select mcspi1_cs2 0x7: Select safe_mode_core177 0x0: Select gpio5_145 0x2: Select uart4_cts 0x5: Select usbd0_ulpiphy_data2 0x3: Select sdio5_clk	RW	0x7
15	I2C5_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	I2C5_SDA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	I2C5_SDA_INPUTENABLE	Input enable value for pad i2c5_sda 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	I2C5_SDA_PWRDOWN	Power Down setting for pad i2c5_sda 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	I2C5_SDA_PULLTYPESELECT	Pull-Up/Down selection for pad i2c5_sda 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	I2C5_SDA_PULLUDENABLE	Pull-Up/Down enable for pad i2c5_sda 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	I2C5_SDA_MUXMODE	Functional multiplexing selection for pad i2c5_sda 0x0: Select i2c5_sda 0x6: Select gpio5_148 0x7: Select safe_mode_core176 0x2: Select uart4_tx	RW	0x7

Table 18-669. Register Call Summary for Register CONTROL_CORE_PAD0_I2C5_SDA_PAD1_GPIO5_145

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-670. CONTROL_CORE_PAD0_GPIO5_146_PAD1_UART6_TX

Address Offset	0x0000 01CC		
Physical Address	0x4A00 29CC 0x4A00 29CC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads gpio5_146 and uart6_tx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART6_TX_WAKEUPEVENT	UART6_TX_WAKEUPENABLE	RESERVED					UART6_TX_INPUTENABLE	RESERVED		UART6_TX_PWRDOWN	UART6_TX_PULLTYPESELECT	UART6_TX_PULLUDENABLE	UART6_TX_MUXMODE			GPIO5_146_WAKEUPEVENT	GPIO5_146_WAKEUPENABLE	RESERVED					GPIO5_146_INPUTENABLE	RESERVED		GPIO5_146_PWRDOWN	GPIO5_146_PULLTYPESELECT	GPIO5_146_PULLUDENABLE	GPIO5_146_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART6_TX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART6_TX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	UART6_TX_INPUTENABLE	Input enable value for pad uart6_tx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	UART6_TX_PWRDOWN	Power Down setting for pad uart6_tx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0

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Bits	Field Name	Description	Type	Reset
20	UART6_TX_PULLTYPESELECT	Pull-Up/Down selection for pad uart6_tx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART6_TX_PULLUDENABLE	Pull-Up/Down enable for pad uart6_tx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	UART6_TX_MUXMODE	Functional multiplexing selection for pad uart6_tx 0x0: Select uart6_tx 0x3: Select sdio5_data3 0x7: Select safe_mode_core179 0x4: Select usbb2_mm_rxdp 0x6: Select gpio5_149	RW	0x7
15	GPIO5_146_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPIO5_146_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	GPIO5_146_INPUTENABLE	Input enable value for pad gpio5_146 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	GPIO5_146_PWRDOWN	Power Down setting for pad gpio5_146 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	GPIO5_146_PULLTYPESELECT	Pull-Up/Down selection for pad gpio5_146 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPIO5_146_PULLUDENABLE	Pull-Up/Down enable for pad gpio5_146 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPIO5_146_MUXMODE	Functional multiplexing selection for pad gpio5_146 0x6: Select gpio5_146 0x1: Select mcspi1_cs3 0x7: Select safe_mode_core178 0x0: Select gpio5_146 0x2: Select uart4_rts 0x5: Select usbd0_ulpiphy_data3 0x3: Select sdio5_cmd	RW	0x7

Table 18-671. Register Call Summary for Register CONTROL_CORE_PAD0_GPIO5_146_PAD1_UART6_TX

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-672. CONTROL_CORE_PAD0_UART6_RX_PAD1_UART6_CTS

Address Offset	0x0000 01D0		
Physical Address	0x4A00 29D0 0x4A00 29D0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart6_rx and uart6_cts Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART6_CTS_WAKEUPEVENT	UART6_CTS_WAKEUPENABLE	RESERVED					UART6_CTS_INPUTENABLE	RESERVED		UART6_CTS_PWRDOWN	UART6_CTS_PULLTYPESELECT	UART6_CTS_PULLUDENABLE	UART6_CTS_MUXMODE			UART6_RX_WAKEUPEVENT	UART6_RX_WAKEUPENABLE	RESERVED					UART6_RX_INPUTENABLE	RESERVED		UART6_RX_PWRDOWN	UART6_RX_PULLTYPESELECT	UART6_RX_PULLUDENABLE	UART6_RX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART6_CTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART6_CTS_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	UART6_CTS_INPUTENABLE	Input enable value for pad uart6_cts 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	UART6_CTS_PWRDOWN	Power Down setting for pad uart6_cts 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	UART6_CTS_PULLTYPESELECT	Pull-Up/Down selection for pad uart6_cts 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART6_CTS_PULLUDENABLE	Pull-Up/Down enable for pad uart6_cts 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	UART6_CTS_MUXMODE	Functional multiplexing selection for pad uart6_cts 0x0: Select uart6_cts 0x1: Select sys_ndmareq1 0x3: Select sdio5_data1 0x7: Select safe_mode_core181 0x4: Select usbb2_mm_rxrcv 0x6: Select gpio5_151	RW	0x7

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Bits	Field Name	Description	Type	Reset
15	UART6_RX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART6_RX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	UART6_RX_INPUTENABLE	Input enable value for pad uart6_rx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	UART6_RX_PWRDOWN	Power Down setting for pad uart6_rx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART6_RX_PULLTYPESELECT	Pull-Up/Down selection for pad uart6_rx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	UART6_RX_PULLUDENABLE	Pull-Up/Down enable for pad uart6_rx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART6_RX_MUXMODE	Functional multiplexing selection for pad uart6_rx 0x0: Select uart6_rx 0x3: Select sdio5_data2 0x7: Select safe_mode_core180 0x4: Select usbb2_mm_rxdm 0x6: Select gpio5_150	RW	0x7

Table 18-673. Register Call Summary for Register CONTROL_CORE_PAD0_UART6_RX_PAD1_UART6_CTS

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-674. CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX

Address Offset	0x0000 01D4		
Physical Address	0x4A00 29D4 0x4A00 29D4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart6_rts and uart3_cts_rctx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART3_CTS_RCTX_WAKEUPEVENT	UART3_CTS_RCTX_WAKEUPENABLE	RESERVED					UART3_CTS_RCTX_INPUTENABLE	RESERVED		UART3_CTS_RCTX_PWRDOWN	UART3_CTS_RCTX_PULLTYPESELECT	UART3_CTS_RCTX_PULLUDENABLE	UART3_CTS_RCTX_MUXMODE			UART6_RTS_WAKEUPEVENT	UART6_RTS_WAKEUPENABLE	RESERVED					UART6_RTS_INPUTENABLE	RESERVED		UART6_RTS_PWRDOWN	UART6_RTS_PULLTYPESELECT	UART6_RTS_PULLUDENABLE	UART6_RTS_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART3_CTS_RCTX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART3_CTS_RCTX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	UART3_CTS_RCTX_INPUTENABLE	Input enable value for pad uart3_cts_rctx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	UART3_CTS_RCTX_PWRDOWN	Power Down setting for pad uart3_cts_rctx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	UART3_CTS_RCTX_PULLTYPESELECT	Pull-Up/Down selection for pad uart3_cts_rctx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART3_CTS_RCTX_PULLUDENABLE	Pull-Up/Down enable for pad uart3_cts_rctx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	UART3_CTS_RCTX_MUXMODE	Functional multiplexing selection for pad uart3_cts_rctx 0x6: Select gpio5_153 0x1: Select sata_actled 0x7: Select safe_mode_core183 0x0: Select uart3_cts_rctx 0x4: Select usbb2_mm_txen 0x5: Select usbd0_ulpiphy_data4 0x3: Select sdio5_data7	RW	0x7
15	UART6_RTS_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART6_RTS_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
8	UART6_RTS_INPUTENABLE	Input enable value for pad uart6_rts 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	UART6_RTS_PWRDOWN	Power Down setting for pad uart6_rts 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART6_RTS_PULLTYPESELECT	Pull-Up/Down selection for pad uart6_rts 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	UART6_RTS_PULLUDENABLE	Pull-Up/Down enable for pad uart6_rts 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART6_RTS_MUXMODE	Functional multiplexing selection for pad uart6_rts 0x6: Select gpio5_152 0x1: Select sys_ndmareq0 0x7: Select safe_mode_core182 0x0: Select uart6_rts 0x4: Select usbb2_mm_txse0 0x5: Select usbd0_ulpiphy_stp 0x3: Select sdio5_data0	RW	0x7

Table 18-675. Register Call Summary for Register CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Programming Guide • Pad Configuration Programming Points: [2] [3] [4] [5] [6] [7]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [8]

Table 18-676. CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX

Address Offset	0x0000 01D8		
Physical Address	0x4A00 29D8 0x4A00 29D8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart3_rts_irsd and uart3_tx_irtx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART3_TX_IRTX_WAKEUPEVENT	UART3_TX_IRTX_WAKEUPENABLE	RESERVED					UART3_TX_IRTX_INPUTENABLE	RESERVED		UART3_TX_IRTX_PWRDOWN	UART3_TX_IRTX_PULLTYPESELECT	UART3_TX_IRTX_PULLUDENABLE	UART3_TX_IRTX_MUXMODE			UART3_RTS_IRSD_WAKEUPEVENT	UART3_RTS_IRSD_WAKEUPENABLE	RESERVED					UART3_RTS_IRSD_INPUTENABLE	RESERVED		UART3_RTS_IRSD_PWRDOWN	UART3_RTS_IRSD_PULLTYPESELECT	UART3_RTS_IRSD_PULLUDENABLE	UART3_RTS_IRSD_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART3_TX_IRTX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	UART3_TX_IRTX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	UART3_TX_IRTX_INPUTENABLE	Input enable value for pad uart3_tx_irtx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	UART3_TX_IRTX_PWRDOWN	Power Down setting for pad uart3_tx_irtx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	UART3_TX_IRTX_PULLTYPESELECT	Pull-Up/Down selection for pad uart3_tx_irtx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	UART3_TX_IRTX_PULLUDENABLE	Pull-Up/Down enable for pad uart3_tx_irtx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	UART3_TX_IRTX_MUXMODE	Functional multiplexing selection for pad uart3_tx_irtx 0x6: Select gpio5_155 0x7: Select safe_mode_core185 0x0: Select uart3_tx_irtx 0x4: Select sdio4_clk 0x5: Select usbd0_ulpiphy_data6 0x3: Select sdio5_data5	RW	0x0
15	UART3_RTS_IRSD_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART3_RTS_IRSD_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
8	UART3_RTS_IRSD_INPUTENABLE	Input enable value for pad uart3_rts_irsd 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	UART3_RTS_IRSD_PWRDOWN	Power Down setting for pad uart3_rts_irsd 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART3_RTS_IRSD_PULLTYPESELECT	Pull-Up/Down selection for pad uart3_rts_irsd 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	UART3_RTS_IRSD_PULLUDENABLE	Pull-Up/Down enable for pad uart3_rts_irsd 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART3_RTS_IRSD_MUXMODE	Functional multiplexing selection for pad uart3_rts_irsd 0x6: Select gpio5_154 0x1: Select hdq_sio 0x7: Select safe_mode_core184 0x0: Select uart3_rts_irsd 0x4: Select usbb2_mm_txdat 0x5: Select usbd0_ulpiphy_data5 0x3: Select sdio5_data6	RW	0x7

Table 18-677. Register Call Summary for Register CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Programming Guide • Pad Configuration Programming Points: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [14]

Table 18-678. CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE

Address Offset	0x0000 01DC		
Physical Address	0x4A00 29DC 0x4A00 29DC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads uart3_rx_irrx and usbb3_hsic_strobe Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB3_HSIC_STROBE_WAKEUPEVENT	USBB3_HSIC_STROBE_WAKEUPENABLE	RESERVED					USBB3_HSIC_STROBE_INPUTENABLE	RESERVED					USBB3_HSIC_STROBE_MUXMODE			UART3_RX_IRRX_WAKEUPEVENT	UART3_RX_IRRX_WAKEUPENABLE	RESERVED					UART3_RX_IRRX_INPUTENABLE	RESERVED		UART3_RX_IRRX_PWRDOWN	UART3_RX_IRRX_PULLTYPESELECT	UART3_RX_IRRX_PULLUDENABLE	UART3_RX_IRRX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	USBB3_HSIC_STROBE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	USBB3_HSIC_STROBE_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	USBB3_HSIC_STROBE_INPUTENABLE	Input enable value for pad usbb3_hsic_strobe 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:19	RESERVED		R	0x00
18:16	USBB3_HSIC_STROBE_MUXMODE	Functional multiplexing selection for pad usbb3_hsic_strobe 0x0: Select usbb3_hsic_strobe 0x7: Select safe_mode_core187 0x6: Select gpio5_158	RW	0x7
15	UART3_RX_IRRX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	UART3_RX_IRRX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	UART3_RX_IRRX_INPUTENABLE	Input enable value for pad uart3_rx_irrx 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	UART3_RX_IRRX_PWRDOWN	Power Down setting for pad uart3_rx_irrx 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	UART3_RX_IRRX_PULLTYPESELECT	Pull-Up/Down selection for pad uart3_rx_irrx 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1

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Bits	Field Name	Description	Type	Reset
3	UART3_RX_IRRX_PULLUDENABLE	Pull-Up/Down enable for pad uart3_rx_irrx 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	UART3_RX_IRRX_MUXMODE	Functional multiplexing selection for pad uart3_rx_irrx 0x6: Select gpio5_156 0x7: Select safe_mode_core186 0x0: Select uart3_rx_irrx 0x4: Select sdio4_cmd 0x5: Select usbd0_ulpiphy_data7 0x3: Select sdio5_data4	RW	0x0

Table 18-679. Register Call Summary for Register CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Programming Guide • Pad Configuration Programming Points: [2] [3] [4] [5] [6] [7]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [8]

Table 18-680. CONTROL_CORE_PAD0_USBB3_HSIC_DATA_PAD1_SDCARD_CLK

Address Offset	0x0000 01E0		
Physical Address	0x4A00 29E0 0x4A00 29E0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads usbb3_hsic_data and sdcard_clk Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDCARD_CLK_WAKEUPEVENT	SDCARD_CLK_WAKEUPENABLE	RESERVED					SDCARD_CLK_INPUTENABLE	RESERVED	SDCARD_CLK_GLITCHGOBBLER	RESERVED	SDCARD_CLK_PULLTYPESELECT	SDCARD_CLK_PULLUDENABLE	SDCARD_CLK_MUXMODE			USBB3_HSIC_DATA_WAKEUPEVENT	USBB3_HSIC_DATA_WAKEUPENABLE	RESERVED					USBB3_HSIC_DATA_INPUTENABLE	RESERVED						USBB3_HSIC_DATA_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SDCARD_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO[1] Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	SDCARD_CLK_WAKEUPENABLE	Input pad wake-up enable [1] 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

(1) Wakeup feature is not supported on this pad because it is output only.

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Bits	Field Name	Description	Type	Reset
29:25	RESERVED		R	0x0
24	SDCARD_CLK_INPUTENABLE	Input enable value for pad sdcard_clk 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23	RESERVED		R	0
22	SDCARD_CLK_GLITCHGOBBLER	Glitch Gobbler setting for pad sdcard_clk 0x0: IO do not Filter glitch from outside 0x1: IO Filter glitch from outside	RW	0
21	RESERVED		R	0
20	SDCARD_CLK_PULLTYPESELECT	Pull-Up/Down selection for pad sdcard_clk 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	SDCARD_CLK_PULLUDENABLE	Pull-Up/Down enable for pad sdcard_clk 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	SDCARD_CLK_MUXMODE	Functional multiplexing selection for pad sdcard_clk 0x0: Select sdcard_clk 0x3: Select jtag_rtck 0x7: Select safe_mode_core189 0x5: Select n_clk	RW	0x0
15	USBB3_HSIC_DATA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	USBB3_HSIC_DATA_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	USBB3_HSIC_DATA_INPUTENABLE	Input enable value for pad usbb3_hsic_data 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:3	RESERVED		R	0x00
2:0	USBB3_HSIC_DATA_MUXMODE	Functional multiplexing selection for pad usbb3_hsic_data 0x0: Select usbb3_hsic_data 0x7: Select safe_mode_core188 0x6: Select gpio5_159	RW	0x7

Table 18-681. Register Call Summary for Register CONTROL_CORE_PAD0_USBB3_HSIC_DATA_PAD1_SDCARD_CLK

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

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Table 18-682. CONTROL_CORE_PAD0_SDCARD_CMD_PAD1_SDCARD_DATA2

Address Offset	0x0000 01E4		
Physical Address	0x4A00 29E4 0x4A00 29E4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads sdcard_cmd and sdcard_data2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDCARD_DATA2_WAKEUPEVENT	SDCARD_DATA2_WAKEUPENABLE	RESERVED					SDCARD_DATA2_INPUTENABLE	RESERVED			SDCARD_DATA2_PULLTYPESELECT	SDCARD_DATA2_PULLUDENABLE	SDCARD_DATA2_MUXMODE			SDCARD_CMD_WAKEUPEVENT	SDCARD_CMD_WAKEUPENABLE	RESERVED					SDCARD_CMD_INPUTENABLE	RESERVED			SDCARD_CMD_PULLTYPESELECT	SDCARD_CMD_PULLUDENABLE	SDCARD_CMD_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SDCARD_DATA2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	SDCARD_DATA2_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	SDCARD_DATA2_INPUTENABLE	Input enable value for pad sdcard_data2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDCARD_DATA2_PULLTYPESELECT	Pull-Up/Down selection for pad sdcard_data2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	SDCARD_DATA2_PULLUDENABLE	Pull-Up/Down enable for pad sdcard_data2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	SDCARD_DATA2_MUXMODE	Functional multiplexing selection for pad sdcard_data2 0x0: Select sdcard_data2 0x3: Select jtag_tmsc 0x7: Select safe_mode_core193 0x5: Select n_d2	RW	0x0
15	SDCARD_CMD_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	SDCARD_CMD_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13:9	RESERVED		R	0x0
8	SDCARD_CMD_INPUTENABLE	Input enable value for pad sdcard_cmd 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDCARD_CMD_PULLTYPESELECT	Pull-Up/Down selection for pad sdcard_cmd 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	SDCARD_CMD_PULLUDENABLE	Pull-Up/Down enable for pad sdcard_cmd 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	SDCARD_CMD_MUXMODE	Functional multiplexing selection for pad sdcard_cmd 0x0: Select sdcard_cmd 0x3: Select jtag_tdo 0x7: Select safe_mode_core190 0x4: Select uart6_rx 0x6: Select n_d2	RW	0x0

Table 18-683. Register Call Summary for Register CONTROL_CORE_PAD0_SDCARD_CMD_PAD1_SDCARD_DATA2

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-684. CONTROL_CORE_PAD0_SDCARD_DATA3_PAD1_SDCARD_DATA0

Address Offset	0x0000 01E8		
Physical Address	0x4A00 29E8 0x4A00 29E8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads sdcard_data3 and sdcard_data0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDCARD_DATA0_WAKEUPEVENT	SDCARD_DATA0_WAKEUPENABLE	RESERVED					SDCARD_DATA0_INPUTENABLE	RESERVED			SDCARD_DATA0_PULLTYPESELECT	SDCARD_DATA0_PULLUDENABLE	SDCARD_DATA0_MUXMODE			SDCARD_DATA3_WAKEUPEVENT	SDCARD_DATA3_WAKEUPENABLE	RESERVED					SDCARD_DATA3_INPUTENABLE	RESERVED			SDCARD_DATA3_PULLTYPESELECT	SDCARD_DATA3_PULLUDENABLE	SDCARD_DATA3_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	SDCARD_DATA0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	SDCARD_DATA0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x0
24	SDCARD_DATA0_INPUTENABLE	Input enable value for pad sdcard_data0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDCARD_DATA0_PULLTYPESELECT	Pull-Up/Down selection for pad sdcard_data0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	SDCARD_DATA0_PULLUDENABLE	Pull-Up/Down enable for pad sdcard_data0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	SDCARD_DATA0_MUXMODE	Functional multiplexing selection for pad sdcard_data0 0x0: Select sdcard_data0 0x3: Select jtag_tdi 0x7: Select safe_mode_core191 0x5: Select n_d0	RW	0x0
15	SDCARD_DATA3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	SDCARD_DATA3_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	SDCARD_DATA3_INPUTENABLE	Input enable value for pad sdcard_data3 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDCARD_DATA3_PULLTYPESELECT	Pull-Up/Down selection for pad sdcard_data3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	SDCARD_DATA3_PULLUDENABLE	Pull-Up/Down enable for pad sdcard_data3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	SDCARD_DATA3_MUXMODE	Functional multiplexing selection for pad sdcard_data3 0x0: Select sdcard_data3 0x3: Select jtag_tck 0x7: Select safe_mode_core194 0x5: Select n_d3	RW	0x0

Table 18-685. Register Call Summary for Register CONTROL_CORE_PAD0_SDCARD_DATA3_PAD1_SDCARD_DATA0

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]

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Table 18-685. Register Call Summary for Register CONTROL_CORE_PAD0_SDCARD_DATA3_PAD1_SDCARD_DATA0 (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-686. CONTROL_CORE_PAD0_SDCARD_DATA1_PAD1_USBD0_HS_DP

Address Offset	0x0000 01EC		
Physical Address	0x4A00 29EC 0x4A00 29EC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads sdcard_data1 and usbd0_hs_dp Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBD0_HS_DP_WAKEUPEVENT	USBD0_HS_DP_WAKEUPENABLE	RESERVED									USBD0_HS_DP_PULLTYPESELECT	USBD0_HS_DP_PULLUDENABLE	USBD0_HS_DP_MUXMODE			SDCARD_DATA1_WAKEUPEVENT	SDCARD_DATA1_WAKEUPENABLE	RESERVED						SDCARD_DATA1_INPUTENABLE	RESERVED				SDCARD_DATA1_PULLTYPESELECT	SDCARD_DATA1_PULLUDENABLE	SDCARD_DATA1_MUXMODE			

Bits	Field Name	Description	Type	Reset
31	USBD0_HS_DP_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	USBD0_HS_DP_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:21	RESERVED		R	0x0
20	USBD0_HS_DP_PULLTYPESELECT	Pull-Up/Down selection for pad usbd0_hs_dp 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	USBD0_HS_DP_PULLUDENABLE	Pull-Up/Down enable for pad usbd0_hs_dp 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
18:16	USBD0_HS_DP_MUXMODE	Functional multiplexing selection for pad usbd0_hs_dp 0x0: Select usbd0_hs_dp 0x4: Select uart3_rx_irrx 0x7: Select safe_mode_core195	RW	0x0
15	SDCARD_DATA1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0

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Bits	Field Name	Description	Type	Reset
14	SDCARD_DATA1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x0
8	SDCARD_DATA1_INPUTENABLE	Input enable value for pad sdcard_data1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDCARD_DATA1_PULLTYPESELECT	Pull-Up/Down selection for pad sdcard_data1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	SDCARD_DATA1_PULLUDENABLE	Pull-Up/Down enable for pad sdcard_data1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	SDCARD_DATA1_MUXMODE	Functional multiplexing selection for pad sdcard_data1 0x0: Select sdcard_data1 0x3: Select jtag_ntrst 0x7: Select safe_mode_core192 0x5: Select n_d1	RW	0x0

Table 18-687. Register Call Summary for Register CONTROL_CORE_PAD0_SDCARD_DATA1_PAD1_USBD0_HS_DP

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-688. CONTROL_CORE_PAD0_USBD0_HS_DM_PAD1_I2C1_PMIC_SCL

Address Offset	0x0000 01F0		
Physical Address	0x4A00 29F0 0x4A00 29F0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads usbd0_hs_dm and i2c1_pmic_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								I2C1_PMIC_SCL_INPUTENABLE	RESERVED							I2C1_PMIC_SCL_PWRDOWN	I2C1_PMIC_SCL_PULLTYPESELECT	I2C1_PMIC_SCL_PULLUDENABLE	RESERVED									USBD0_HS_DM_PULLTYPESELECT	USBD0_HS_DM_PULLUDENABLE	USBD0_HS_DM_MUXMODE			

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Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x0
24	I2C1_PMIC_SCL_INPUTENABLE	Input enable value for pad i2c1_pmic_scl 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	I2C1_PMIC_SCL_PWRDOWN	Power Down setting for pad i2c1_pmic_scl 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	I2C1_PMIC_SCL_PULLTYPESELECT	Pull-Up/Down selection for pad i2c1_pmic_scl 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	I2C1_PMIC_SCL_PULLUDENABLE	Pull-Up/Down enable for pad i2c1_pmic_scl 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
18:5	RESERVED		R	0x0
4	USBD0_HS_DM_PULLTYPESELECT	Pull-Up/Down selection for pad usbd0_hs_dm 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	USBD0_HS_DM_PULLUDENABLE	Pull-Up/Down enable for pad usbd0_hs_dm 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
2:0	USBD0_HS_DM_MUXMODE	Functional multiplexing selection for pad usbd0_hs_dm 0x0: Select usbd0_hs_dm 0x4: Select uart3_tx_irtx 0x7: Select safe_mode_core196	RW	0x0

Table 18-689. Register Call Summary for Register CONTROL_CORE_PAD0_USBD0_HS_DM_PAD1_I2C1_PMIC_SCL

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-690. CONTROL_CORE_PAD0_I2C1_PMIC_SDA_PAD1_USBD0_SS_RX

Address Offset	0x0000 01F4		
Physical Address	0x4A00 29F4 0x4A00 29F4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Register control for Pads i2c1_pmic_sda and usbd0_ss_rx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBD0_SS_RX_WAKEUPEVENT	USBD0_SS_RX_WAKEUPENABLE	RESERVED																					I2C1_PMIC_SDA_INPUTENABLE	RESERVED			I2C1_PMIC_SDA_PWRDOWN	I2C1_PMIC_SDA_PULLTYPESELECT	I2C1_PMIC_SDA_PULLUDENABLE	RESERVED			

Bits	Field Name	Description	Type	Reset
31	USBD0_SS_RX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	USBD0_SS_RX_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:9	RESERVED		R	0x0
8	I2C1_PMIC_SDA_INPUTENABLE	Input enable value for pad i2c1_pmic_sda 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	I2C1_PMIC_SDA_PWRDOWN	Power Down setting for pad i2c1_pmic_sda 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	I2C1_PMIC_SDA_PULLTYPESELECT	Pull-Up/Down selection for pad i2c1_pmic_sda 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	I2C1_PMIC_SDA_PULLUDENABLE	Pull-Up/Down enable for pad i2c1_pmic_sda 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
2:0	RESERVED		R	0x0

Table 18-691. Register Call Summary for Register CONTROL_CORE_PAD0_I2C1_PMIC_SDA_PAD1_USBD0_SS_RX

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-692. CONTROL_PADCONF_WAKEUPEVENT_0

Address Offset	0x0000 01FC		
Physical Address	0x4A00 29FC 0x4A00 29FC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2C_DATA9_DUPLICATEWAKEUPEVENT	C2C_DATA8_DUPLICATEWAKEUPEVENT	C2C_DATAOUT7_DUPLICATEWAKEUPEVENT	C2C_DATAOUT6_DUPLICATEWAKEUPEVENT	C2C_DATAOUT5_DUPLICATEWAKEUPEVENT	C2C_DATAOUT4_DUPLICATEWAKEUPEVENT	C2C_DATAOUT3_DUPLICATEWAKEUPEVENT	C2C_DATAOUT2_DUPLICATEWAKEUPEVENT	C2C_DATAOUT1_DUPLICATEWAKEUPEVENT	C2C_DATAOUT0_DUPLICATEWAKEUPEVENT	C2C_DATAIN7_DUPLICATEWAKEUPEVENT	C2C_DATAIN6_DUPLICATEWAKEUPEVENT	C2C_DATAIN5_DUPLICATEWAKEUPEVENT	C2C_DATAIN4_DUPLICATEWAKEUPEVENT	C2C_DATAIN3_DUPLICATEWAKEUPEVENT	C2C_DATAIN2_DUPLICATEWAKEUPEVENT	C2C_DATAIN1_DUPLICATEWAKEUPEVENT	C2C_DATAIN0_DUPLICATEWAKEUPEVENT	C2C_CLKIN1_DUPLICATEWAKEUPEVENT	C2C_CLKIN0_DUPLICATEWAKEUPEVENT	C2C_CLKOUT1_DUPLICATEWAKEUPEVENT	C2C_CLKOUT0_DUPLICATEWAKEUPEVENT	EMMC_DATA7_DUPLICATEWAKEUPEVENT	EMMC_DATA6_DUPLICATEWAKEUPEVENT	EMMC_DATA5_DUPLICATEWAKEUPEVENT	EMMC_DATA4_DUPLICATEWAKEUPEVENT	EMMC_DATA3_DUPLICATEWAKEUPEVENT	EMMC_DATA2_DUPLICATEWAKEUPEVENT	EMMC_DATA1_DUPLICATEWAKEUPEVENT	EMMC_DATA0_DUPLICATEWAKEUPEVENT	EMMC_CMD_DUPLICATEWAKEUPEVENT	EMMC_CLK_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	C2C_DATA9_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_data9 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
30	C2C_DATA8_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_data8 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
29	C2C_DATAOUT7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_dataout7 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
28	C2C_DATAOUT6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_dataout6 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
27	C2C_DATAOUT5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_dataout5 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
26	C2C_DATAOUT4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_dataout4 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
25	C2C_DATAOUT3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_dataout3 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
24	C2C_DATAOUT2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_dataout2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
23	C2C_DATAOUT1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_dataout1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
22	C2C_DATAOUT0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_dataout0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
21	C2C_DATAIN7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_datain7 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
20	C2C_DATAIN6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_datain6 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
19	C2C_DATAIN5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_datain5 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
18	C2C_DATAIN4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_datain4 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
17	C2C_DATAIN3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_datain3 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
16	C2C_DATAIN2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_datain2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
15	C2C_DATAIN1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_datain1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
14	C2C_DATAIN0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_datain0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
13	C2C_CLKIN1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_clkin1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
12	C2C_CLKIN0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_clkin0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
11	C2C_CLKOUT1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_clkout1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
10	C2C_CLKOUT0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_clkout0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
9	EMMC_DATA7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_data7 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
8	EMMC_DATA6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_data6 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
7	EMMC_DATA5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_data5 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
6	EMMC_DATA4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_data4 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
5	EMMC_DATA3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_data3 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
4	EMMC_DATA2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_data2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
3	EMMC_DATA1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_data1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
2	EMMC_DATA0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_data0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
1	EMMC_CMD_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_cmd Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
0	EMMC_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad emmc_clk Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

Table 18-693. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_0

Control Module Functional Description
- Wake-Up Event Detection: [0]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [1]
- CTRL_MODULE_WKUP_PAD Register Summary: [2]

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Table 18-694. CONTROL_PADCONF_WAKEUPEVENT_1

Address Offset	0x0000 0200		
Physical Address	0x4A00 2A00 0x4A00 2A00	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART2_TX_DUPLICATEWAKEUPEVENT	UART2_RX_DUPLICATEWAKEUPEVENT	UART2_CTS_DUPLICATEWAKEUPEVENT	UART2_RTS_DUPLICATEWAKEUPEVENT	HSI2_ACDATA_DUPLICATEWAKEUPEVENT	HSI2_ACFLAG_DUPLICATEWAKEUPEVENT	HSI2_CADATA_DUPLICATEWAKEUPEVENT	HSI2_CAFLAG_DUPLICATEWAKEUPEVENT	HSI2_ACWAKE_DUPLICATEWAKEUPEVENT	HSI2_CAWAKE_DUPLICATEWAKEUPEVENT	HSI2_ACREADY_DUPLICATEWAKEUPEVENT	HSI2_CAREADY_DUPLICATEWAKEUPEVENT	UART1_RTS_DUPLICATEWAKEUPEVENT	UART1_RX_DUPLICATEWAKEUPEVENT	UART1_CTS_DUPLICATEWAKEUPEVENT	UART1_TX_DUPLICATEWAKEUPEVENT	HSI1_CADATA_DUPLICATEWAKEUPEVENT	HSI1_CAFLAG_DUPLICATEWAKEUPEVENT	HSI1_ACDATA_DUPLICATEWAKEUPEVENT	HSI1_ACFLAG_DUPLICATEWAKEUPEVENT	HSI1_CAWAKE_DUPLICATEWAKEUPEVENT	HSI1_ACWAKE_DUPLICATEWAKEUPEVENT	HSI1_CAREADY_DUPLICATEWAKEUPEVENT	HSI1_ACREADY_DUPLICATEWAKEUPEVENT	LLIB_WAKEREQOUT_DUPLICATEWAKEUPEVENT	LLIA_WAKEREQOUT_DUPLICATEWAKEUPEVENT	C2C_DATA15_DUPLICATEWAKEUPEVENT	C2C_DATA14_DUPLICATEWAKEUPEVENT	C2C_DATA13_DUPLICATEWAKEUPEVENT	C2C_DATA12_DUPLICATEWAKEUPEVENT	C2C_DATA11_DUPLICATEWAKEUPEVENT	C2C_DATA10_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	UART2_TX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart2_tx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
30	UART2_RX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart2_rx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
29	UART2_CTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart2_cts Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
28	UART2_RTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart2_rts Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
27	HSI2_ACDATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi2_acdata Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
26	HSI2_ACFLAG_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi2_acflag Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
25	HSI2_CADATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi2_cadata Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
24	HSI2_CAFLAG_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi2_caflag Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
23	HSI2_ACWAKE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi2_acwake Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
22	HSI2_CAWAKE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi2_cawake Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
21	HSI2_ACREADY_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi2_acready Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
20	HSI2_CAREADY_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi2_caready Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
19	UART1_RTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart1_rts Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
18	UART1_RX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart1_rx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
17	UART1_CTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart1_cts Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
16	UART1_TX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart1_tx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
15	HSI1_CADATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi1_cadata Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
14	HSI1_CAFLAG_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi1_caflag Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
13	HSI1_ACDATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi1_acdata Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
12	HSI1_ACFLAG_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi1_acflag Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
11	HSI1_CAWAKE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi1_cawake Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
10	HSI1_ACWAKE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi1_acwake Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
9	HSI1_CAREADY_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi1_caready Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
8	HSI1_ACREADY_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hsi1_acready Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
7	LLIB_WAKEREQOUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad llib_wakereqout Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
6	LLIA_WAKEREQOUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad llia_wakereqout Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
5	C2C_DATA15_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_data15 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
4	C2C_DATA14_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_data14 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
3	C2C_DATA13_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_data13 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
2	C2C_DATA12_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_data12 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
1	C2C_DATA11_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_data11 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
0	C2C_DATA10_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad c2c_data10 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

Table 18-695. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_1

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [0]

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Table 18-696. CONTROL_PADCONF_WAKEUPEVENT_2

Address Offset	0x0000 0204		
Physical Address	0x4A00 2A04 0x4A00 2A04	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFBI_CS0_DUPLICATEWAKEUPEVENT	RFBI_WE_DUPLICATEWAKEUPEVENT	RFBI_DATA0_DUPLICATEWAKEUPEVENT	RFBI_DATA1_DUPLICATEWAKEUPEVENT	RFBI_DATA2_DUPLICATEWAKEUPEVENT	RFBI_DATA3_DUPLICATEWAKEUPEVENT	RFBI_DATA4_DUPLICATEWAKEUPEVENT	RFBI_DATA5_DUPLICATEWAKEUPEVENT	RFBI_DATA6_DUPLICATEWAKEUPEVENT	RFBI_DATA7_DUPLICATEWAKEUPEVENT	RFBI_DATA8_DUPLICATEWAKEUPEVENT	RFBI_DATA9_DUPLICATEWAKEUPEVENT	RFBI_DATA10_DUPLICATEWAKEUPEVENT	RFBI_DATA11_DUPLICATEWAKEUPEVENT	RFBI_DATA12_DUPLICATEWAKEUPEVENT	RFBI_DATA13_DUPLICATEWAKEUPEVENT	RFBI_DATA14_DUPLICATEWAKEUPEVENT	RFBI_DATA15_DUPLICATEWAKEUPEVENT	MCSPI2_CS0_DUPLICATEWAKEUPEVENT	MCSPI2_SOMI_DUPLICATEWAKEUPEVENT	MCSPI2_SIMO_DUPLICATEWAKEUPEVENT	MCSPI2_CLK_DUPLICATEWAKEUPEVENT	I2C4_SDA_DUPLICATEWAKEUPEVENT	I2C4_SCL_DUPLICATEWAKEUPEVENT	TIMER9_PWM_EVT_DUPLICATEWAKEUPEVENT	DSIPORTC_TE0_DUPLICATEWAKEUPEVENT	DSIPORTA_TE0_DUPLICATEWAKEUPEVENT	TIMER10_PWM_EVT_DUPLICATEWAKEUPEVENT	USBB2_HSIC_DATA_DUPLICATEWAKEUPEVENT	USBB2_HSIC_STROBE_DUPLICATEWAKEUPEVENT	USBB1_HSIC_DATA_DUPLICATEWAKEUPEVENT	USBB1_HSIC_STROBE_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	RFBI_CS0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_cs0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
30	RFBI_WE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_we Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
29	RFBI_DATA0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
28	RFBI_DATA1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
27	RFBI_DATA2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
26	RFBI_DATA3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data3 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
25	RFBI_DATA4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data4 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
24	RFBI_DATA5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data5 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
23	RFBI_DATA6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data6 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
22	RFBI_DATA7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data7 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
21	RFBI_DATA8_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data8 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
20	RFBI_DATA9_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data9 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
19	RFBI_DATA10_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data10 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
18	RFBI_DATA11_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data11 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
17	RFBI_DATA12_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data12 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
16	RFBI_DATA13_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data13 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
15	RFBI_DATA14_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data14 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
14	RFBI_DATA15_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_data15 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
13	MCSPI2_CS0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad mcspi2_cs0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
12	MCSPI2_SOMI_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad mcspi2_somi Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
11	MCSPI2_SIMO_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad mcspi2_simo Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
10	MCSPI2_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad mcspi2_clk Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
9	I2C4_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad i2c4_sda Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
8	I2C4_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad i2c4_scl Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
7	TIMER9_PWM_EVT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad timer9_pwm_evt Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
6	DSIPORTC_TE0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad dsiportc_te0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
5	DSIPORTA_TE0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad dsiporta_te0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
4	TIMER10_PWM_EVT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad timer10_pwm_evt Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
3	USBB2_HSIC_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad usbb2_hsic_data Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
2	USBB2_HSIC_STROBE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad usbb2_hsic_strobe Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
1	USBB1_HSIC_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad usbb1_hsic_data Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
0	USBB1_HSIC_STROBE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad usbb1_hsic_strobe Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

Table 18-697. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_2

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [0]

Table 18-698. CONTROL_PADCONF_WAKEUPEVENT_3

Address Offset	0x0000 0208		
Physical Address	0x4A00 2A08 0x4A00 2A08	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIPORTA_LANE3Y_DUPLICATEWAKEUPEVENT	CSIPORTA_LANE3X_DUPLICATEWAKEUPEVENT	CSIPORTA_LANE2Y_DUPLICATEWAKEUPEVENT	CSIPORTA_LANE2X_DUPLICATEWAKEUPEVENT	CSIPORTA_LANE1Y_DUPLICATEWAKEUPEVENT	CSIPORTA_LANE1X_DUPLICATEWAKEUPEVENT	CSIPORTA_LANE0Y_DUPLICATEWAKEUPEVENT	CSIPORTA_LANE0X_DUPLICATEWAKEUPEVENT	CSIPORTB_LANE2Y_DUPLICATEWAKEUPEVENT	CSIPORTB_LANE2X_DUPLICATEWAKEUPEVENT	CSIPORTB_LANE1Y_DUPLICATEWAKEUPEVENT	CSIPORTB_LANE1X_DUPLICATEWAKEUPEVENT	CSIPORTB_LANE0Y_DUPLICATEWAKEUPEVENT	CSIPORTB_LANE0X_DUPLICATEWAKEUPEVENT	CSIPORTC_LANE1Y_DUPLICATEWAKEUPEVENT	CSIPORTC_LANE1X_DUPLICATEWAKEUPEVENT	CSIPORTC_LANE0Y_DUPLICATEWAKEUPEVENT	CSIPORTC_LANE0X_DUPLICATEWAKEUPEVENT	HDMI_DDC_SDA_DUPLICATEWAKEUPEVENT	HDMI_DDC_SCL_DUPLICATEWAKEUPEVENT	HDMI_HPD_DUPLICATEWAKEUPEVENT	HDMI_CEC_DUPLICATEWAKEUPEVENT	GPIO6_187_DUPLICATEWAKEUPEVENT	GPIO6_186_DUPLICATEWAKEUPEVENT	GPIO6_185_DUPLICATEWAKEUPEVENT	GPIO6_184_DUPLICATEWAKEUPEVENT	GPIO6_183_DUPLICATEWAKEUPEVENT	GPIO6_182_DUPLICATEWAKEUPEVENT	RFBI_TE_VSYNC0_DUPLICATEWAKEUPEVENT	RFBI_HSYNC0_DUPLICATEWAKEUPEVENT	RFBI_RE_DUPLICATEWAKEUPEVENT	RFBI_A0_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	CSIPORTA_LANE3Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane3y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
30	CSIPORTA_LANE3X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane3x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
29	CSIPORTA_LANE2Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane2y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
28	CSIPORTA_LANE2X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane2x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
27	CSIPORTA_LANE1Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane1y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
26	CSIPORTA_LANE1X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane1x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
25	CSIPORTA_LANE0Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane0y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
24	CSIPORTA_LANE0X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane0x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
23	CSIPORTB_LANE2Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportb_lane2y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
22	CSIPORTB_LANE2X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportb_lane2x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
21	CSIPORTB_LANE1Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportb_lane1y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
20	CSIPORTB_LANE1X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportb_lane1x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
19	CSIPORTB_LANE0Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportb_lane0y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
18	CSIPORTB_LANE0X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportb_lane0x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
17	CSIPORTC_LANE1Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportc_lane1y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
16	CSIPORTC_LANE1X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportc_lane1x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
15	CSIPORTC_LANE0Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportc_lane0y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
14	CSIPORTC_LANE0X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiportc_lane0x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
13	HDMI_DDC_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hdmi_ddc_sda Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
12	HDMI_DDC_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hdmi_ddc_scl Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
11	HDMI_HPD_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hdmi_hpd Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
10	HDMI_CEC_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad hdmi_cec Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
9	GPIO6_187_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio6_187 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
8	GPIO6_186_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio6_186 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
7	GPIO6_185_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio6_185 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
6	GPIO6_184_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio6_184 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
5	GPIO6_183_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio6_183 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
4	GPIO6_182_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio6_182 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
3	RFBI_TE_VSYNC0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_te_vsync0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
2	RFBI_HSYNC0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_hsync0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
1	RFBI_RE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_re Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
0	RFBI_A0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad rfbi_a0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

Table 18-699. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_3

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [0]

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Table 18-700. CONTROL_PADCONF_WAKEUPEVENT_4

Address Offset	0x0000 020C		
Physical Address	0x4A00 2A0C 0x4A00 2A0C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WLSDIO_DATA0_DUPLICATEWAKEUPEVENT	WLSDIO_CMD_DUPLICATEWAKEUPEVENT	ABEMCPDM_LB_CLK_DUPLICATEWAKEUPEVENT	ABEMCPDM_FRAME_DUPLICATEWAKEUPEVENT	ABEMCPDM_DL_DATA_DUPLICATEWAKEUPEVENT	ABEMCPDM_UL_DATA_DUPLICATEWAKEUPEVENT	ABEMCBSP2_CLKX_DUPLICATEWAKEUPEVENT	ABEMCBSP2_FSX_DUPLICATEWAKEUPEVENT	ABEMCBSP2_DX_DUPLICATEWAKEUPEVENT	ABEMCBSP2_DR_DUPLICATEWAKEUPEVENT	ABESLIMBUS1_DATA_DUPLICATEWAKEUPEVENT	ABESLIMBUS1_CLOCK_DUPLICATEWAKEUPEVENT	ABEDMIC_CLK3_DUPLICATEWAKEUPEVENT	ABEDMIC_CLK2_DUPLICATEWAKEUPEVENT	ABEDMIC_CLK1_DUPLICATEWAKEUPEVENT	ABEDMIC_DIN3_DUPLICATEWAKEUPEVENT	ABEDMIC_DIN2_DUPLICATEWAKEUPEVENT	ABEDMIC_DIN1_DUPLICATEWAKEUPEVENT	ABE_CLKS_DUPLICATEWAKEUPEVENT	GPIO8_234_DUPLICATEWAKEUPEVENT	GPIO8_233_DUPLICATEWAKEUPEVENT	I2C3_SDA_DUPLICATEWAKEUPEVENT	I2C3_SCL_DUPLICATEWAKEUPEVENT	TIMER8_PWM_EVT_DUPLICATEWAKEUPEVENT	TIMER6_PWM_EVT_DUPLICATEWAKEUPEVENT	TIMER5_PWM_EVT_DUPLICATEWAKEUPEVENT	TIMER11_PWM_EVT_DUPLICATEWAKEUPEVENT	CAM_GLOBALRESET_DUPLICATEWAKEUPEVENT	CAM_STROBE_DUPLICATEWAKEUPEVENT	CAM_SHUTTER_DUPLICATEWAKEUPEVENT	CSIPORTA_LANE4Y_DUPLICATEWAKEUPEVENT	CSIPORTA_LANE4X_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	WLSDIO_DATA0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad wlsdio_data0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
30	WLSDIO_CMD_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad wlsdio_cmd Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
29	ABEMCPDM_LB_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abemcpdm_lb_clk Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
28	ABEMCPDM_FRAME_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abemcpdm_frame Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
27	ABEMCPDM_DL_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abemcpdm_dl_data Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
26	ABEMCPDM_UL_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abemcpdm_ul_data Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
25	ABEMCBSP2_CLKX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abemcbsp2_clkx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
24	ABEMCBSP2_FSX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abemcbsp2_fsx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
23	ABEMCBSP2_DX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abemcbsp2_dx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
22	ABEMCBSP2_DR_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abemcbsp2_dr Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
21	ABESLIMBUS1_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abeslimbus1_data Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
20	ABESLIMBUS1_CLOCK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abeslimbus1_clock Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
19	ABEDMIC_CLK3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abedmic_clk3 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
18	ABEDMIC_CLK2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abedmic_clk2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
17	ABEDMIC_CLK1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abedmic_clk1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
16	ABEDMIC_DIN3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abedmic_din3 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
15	ABEDMIC_DIN2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abedmic_din2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
14	ABEDMIC_DIN1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abedmic_din1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
13	ABE_CLKS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad abe_clks Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
12	GPIO8_234_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio8_234 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
11	GPIO8_233_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio8_233 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
10	I2C3_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad i2c3_sda Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
9	I2C3_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad i2c3_scl Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
8	TIMER8_PWM_EVT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad timer8_pwm_evt Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
7	TIMER6_PWM_EVT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad timer6_pwm_evt Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
6	TIMER5_PWM_EVT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad timer5_pwm_evt Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
5	TIMER11_PWM_EVT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad timer11_pwm_evt Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
4	CAM_GLOBALRESET_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad cam_globalreset Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
3	CAM_STROBE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad cam_strobe Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
2	CAM_SHUTTER_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad cam_shutter Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
1	CSIPORTA_LANE4Y_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane4y Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
0	CSIPORTA_LANE4X_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csiporta_lane4x Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Table 18-701. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_4

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [0]

Table 18-702. CONTROL_PADCONF_WAKEUPEVENT_5

Address Offset	0x0000 0210		
Physical Address	0x4A00 2A10 0x4A00 2A10	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDCARD_DATA3_DUPLICATEWAKEUPEVENT	SDCARD_DATA2_DUPLICATEWAKEUPEVENT	SDCARD_CMD_DUPLICATEWAKEUPEVENT	SDCARD_CLK_DUPLICATEWAKEUPEVENT	USBB3_HSIC_DATA_DUPLICATEWAKEUPEVENT	USBB3_HSIC_STROBE_DUPLICATEWAKEUPEVENT	UART3_RX_IRRX_DUPLICATEWAKEUPEVENT	UART3_TX_IRTX_DUPLICATEWAKEUPEVENT	UART3_RTS_IRSD_DUPLICATEWAKEUPEVENT	UART3_CTS_RCTX_DUPLICATEWAKEUPEVENT	UART6_RTS_DUPLICATEWAKEUPEVENT	UART6_CTS_DUPLICATEWAKEUPEVENT	UART6_RX_DUPLICATEWAKEUPEVENT	UART6_TX_DUPLICATEWAKEUPEVENT	GPIO5_146_DUPLICATEWAKEUPEVENT	GPIO5_145_DUPLICATEWAKEUPEVENT	I2C5_SDA_DUPLICATEWAKEUPEVENT	I2C5_SCL_DUPLICATEWAKEUPEVENT	MCSPI1_CS1_DUPLICATEWAKEUPEVENT	MCSPI1_CS0_DUPLICATEWAKEUPEVENT	MCSPI1_SIMO_DUPLICATEWAKEUPEVENT	MCSPI1_SOMI_DUPLICATEWAKEUPEVENT	MCSPI1_CLK_DUPLICATEWAKEUPEVENT	I2C2_SDA_DUPLICATEWAKEUPEVENT	I2C2_SCL_DUPLICATEWAKEUPEVENT	UART5_RTS_DUPLICATEWAKEUPEVENT	UART5_CTS_DUPLICATEWAKEUPEVENT	UART5_TX_DUPLICATEWAKEUPEVENT	UART5_RX_DUPLICATEWAKEUPEVENT	WLSDIO_DATA3_DUPLICATEWAKEUPEVENT	WLSDIO_DATA2_DUPLICATEWAKEUPEVENT	WLSDIO_DATA1_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	SDCARD_DATA3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad sdcard_data3 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
30	SDCARD_DATA2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad sdcard_data2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
29	SDCARD_CMD_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad sdcard_cmd Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
28	SDCARD_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad sdcard_clk Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
27	USBB3_HSIC_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad usbb3_hsic_data Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
26	USBB3_HSIC_STROBE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad usbb3_hsic_strobe Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
25	UART3_RX_IRRX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart3_rx_irrx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
24	UART3_TX_IRTX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart3_tx_irtx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
23	UART3_RTS_IRSD_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart3_rts_irsd Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
22	UART3_CTS_RCTX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart3_cts_rctx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
21	UART6_RTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart6_rts Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
20	UART6_CTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart6_cts Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
19	UART6_RX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart6_rx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
18	UART6_TX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart6_tx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
17	GPIO5_146_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio5_146 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
16	GPIO5_145_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad gpio5_145 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
15	I2C5_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad i2c5_sda Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
14	I2C5_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad i2c5_scl Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
13	MCSPI1_CS1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad mcspi1_cs1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
12	MCSPI1_CS0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad mcspi1_cs0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
11	MCSPI1_SIMO_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad mcspi1_simo Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
10	MCSPI1_SOMI_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad mcspi1_somi Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
9	MCSPI1_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad mcspi1_clk Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
8	I2C2_SDA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad i2c2_sda Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
7	I2C2_SCL_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad i2c2_scl Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
6	UART5_RTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart5_rts Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
5	UART5_CTS_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart5_cts Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
4	UART5_TX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart5_tx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
3	UART5_RX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad uart5_rx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
2	WLSDIO_DATA3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad wlsdio_data3 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
1	WLSDIO_DATA2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad wlsdio_data2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
0	WLSDIO_DATA1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad wlsdio_data1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

Table 18-703. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_5

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [0]

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Table 18-704. CONTROL_PADCONF_WAKEUPEVENT_6

Address Offset	0x0000 0214		
Physical Address	0x4A00 2A14 0x4A00 2A14	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												USBD0_SS_RX_DUPLICATEWAKEUPEVENT	USBD0_HS_DP_DUPLICATEWAKEUPEVENT	SDCARD_DATA1_DUPLICATEWAKEUPEVENT	SDCARD_DATA0_DUPLICATEWAKEUPEVENT				

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	USBD0_SS_RX_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad usbd0_ss_rx Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
2	USBD0_HS_DP_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad usbd0_hs_dp Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
1	SDCARD_DATA1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad sdcard_data1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
0	SDCARD_DATA0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad sdcard_data0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

Table 18-705. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_6

Control Module Functional Description
- Wake-Up Event Detection: [0]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [1]

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Table 18-706. CONTROL_PADCONF_MODE

Address Offset	0x0000 05A4		
Physical Address	0x4A00 2DA4 0x4A00 2DA4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	PAD Voltage Mode control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDS_10_MODE	VDDS_11_MODE	VDDS_12_MODE	VDDS_14_MODE	VDDS_15_MODE	VDDS_16_MODE	VDDS_18_MODE	VDDS_19_MODE	VDDS_21_MODE	VDDS_5_MODE	VDDS_8_MODE	VDDS_2_MODE	VDDS_4_MODE	VDDS_9_MODE	VDDS_EMMC_MODE	VDDS_HDMI_MODE	VDDA_DSIPORTA_MODE	VDDA_DSIPORTC_MODE	VDDS_C2C_MODE	RESERVED												

Bits	Field Name	Description	Type	Reset
31	VDDS_10_MODE	PAD Voltage level control for vdds_10_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
30	VDDS_11_MODE	PAD Voltage level control for vdds_11_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
29	VDDS_12_MODE	PAD Voltage level control for vdds_12_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
28	VDDS_14_MODE	PAD Voltage level control for vdds_14_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
27	VDDS_15_MODE	PAD Voltage level control for vdds_15_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
26	VDDS_16_MODE	PAD Voltage level control for vdds_16_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
25	VDDS_18_MODE	PAD Voltage level control for vdds_18_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
24	VDDS_19_MODE	PAD Voltage level control for vdds_19_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
23	VDDS_21_MODE	PAD Voltage level control for vdds_21_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
22	VDDS_5_MODE	PAD Voltage level control for vdds_5_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0

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Bits	Field Name	Description	Type	Reset
21	VDDS_8_MODE	PAD Voltage level control for vdds_8_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
20	VDDS_2_MODE	PAD Voltage level control for vdds_8_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
19	VDDS_4_MODE	PAD Voltage level control for vdds_4_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
18	VDDS_9_MODE	PAD Voltage level control for vdds_9_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
17	VDDS_EMMC_MODE	PAD Voltage level control for vdds_emmc_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
16	VDDS_HDMI_MODE	PAD Voltage level control for vdds_hdmi_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
15	VDDA_DSIPORTA_MODE	PAD Voltage level control for vdda_dsiporta_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
14	VDDA_DSIPORTC_MODE	PAD Voltage level control for vdda_dsiporta_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
13	VDDS_C2C_MODE	PAD Voltage level control for vdds_c2c_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
12:0	RESERVED		R	0x0000

Table 18-707. Register Call Summary for Register CONTROL_PADCONF_MODE

Control Module Functional Description • Device Core Control Module Instance: [0] • Dual Voltage-Supplied Peripheral Controls: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
Control Module Programming Guide • Pad Configuration Programming Points: [21] [22] [23] [24] [25] [26] [27]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [28]

Table 18-708. CONTROL_SMART1IO_PADCONF_0

Address Offset	0x0000 05A8		
Physical Address	0x4A00 2DA8 0x4A00 2DA8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	SMART1 IO control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
ABE_PART0_DS	ABE_PART1_DS	ABE_PART2_DS	ABE_PART3C_DS	ABE_PART4_DS	ABE_PART5_DS	C2C_PART1_DS	C2C_PART2_DS	CAM_DS	DSIPORTA_DS	DSIPORTC_DS	EMMC_DS	HDMI_PART1_DS	HSI1_DS	HSI2_DS	MCSPI1_DS

Bits	Field Name	Description	Type	Reset
31:30	ABE_PART0_DS	DS control for abe part0 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
29:28	ABE_PART1_DS	DS control for abe part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
27:26	ABE_PART2_DS	DS control for abe part2 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
25:24	ABE_PART3C_DS	DS control for abe part3 clock 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
23:22	ABE_PART4_DS	DS control for abe part4 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
21:20	ABE_PART5_DS	DS control for abe part5 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
19:18	C2C_PART1_DS	DS control for c2c part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
17:16	C2C_PART2_DS	DS control for c2c part2 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2

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Bits	Field Name	Description	Type	Reset
15:14	CAM_DS	DS control for cam 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
13:12	DSIPORTA_DS	DS control for iporta 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
11:10	DSIPORTC_DS	DS control for iportc 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
9:8	EMMC_DS	DS control for emmc 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
7:6	HDMI_PART1_DS	DS control for hdmi part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
5:4	HSI1_DS	DS control for hsi1 part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
3:2	HSI2_DS	DS control for hsi2 part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
1:0	MCSPI1_DS	DS control for mcspi1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2

Table 18-709. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_0

Control Module Functional Description

- Signal Integrity Parameter Controls Overview: [0]
- SMART I/O Buffers with Slew Rate and Drive Strength Control Settings: [1]
- Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17]

Control Module Programming Guide

- Pad Configuration Programming Points: [18]

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Table 18-709. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_0 (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [19]

Table 18-710. CONTROL_SMART1IO_PADCONF_1

Address Offset	0x0000 05AC		
Physical Address	0x4A00 2DAC 0x4A00 2DAC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	SMART1 IO control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
MCSPI2_DS	GPIO_DS	prot_DS	TIMER10_DS	TIMER11_DS	TIMER5_DS	TIMER6_DS	TIMER8_DS	TIMER9_DS	TIMER9_SC	UART1_DS	UART2_PART1_DS	UART3_PART1_DS	UART3_PART2_DS	ABE_PART3D_DS	RESERVED

Bits	Field Name	Description	Type	Reset
31:30	MCSPI2_DS	DS control for mcspi2 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
29:28	GPIO_DS	DS control for gpio 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
27:26	prot_DS	DS control for prot 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
25:24	TIMER10_DS	DS control for timer10 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
23:22	TIMER11_DS	DS control for timer11 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2

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Bits	Field Name	Description	Type	Reset
21:20	TIMER5_DS	DS control for timer5 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
19:18	TIMER6_DS	DS control for timer6 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
17:16	TIMER8_DS	DS control for timer8 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
15:14	TIMER9_DS	DS control for timer9 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
13:12	TIMER9_SC	DS control for timer9 sc 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x0
11:10	UART1_DS	DS control for uart1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
9:8	UART2_PART1_DS	DS control for uart2 part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
7:6	UART3_PART1_DS	DS control for uart3 part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
5:4	UART3_PART2_DS	DS control for uart3 part2 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2

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Bits	Field Name	Description	Type	Reset
3:2	ABE_PART3D_DS	DS control for abe part3 clock 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
1:0	RESERVED		R	0x0

Table 18-711. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_1

Control Module Functional Description
- Signal Integrity Parameter Controls Overview: [0]
- SMART I/O Buffers with Slew Rate and Drive Strength Control Settings: [1]
- Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Control Module Programming Guide
- Pad Configuration Programming Points: [15] [16] [17] [18]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [19]

Table 18-712. CONTROL_SMART1IO_PADCONF_2

Address Offset	0x0000 05B0		
Physical Address	0x4A00 2DB0 0x4A00 2DB0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	SMART1 IO control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6 5 4 3 2 1 0
UART5_PART1_DS	UART5_PART2_DS	UART6_PART1_DS	UART6_PART2_DS	WLSDIO_DS	DSS_PART1_DS	DSS_PART2_DS	C2C_PART3_DS	C2C_PART4_DS	UART2_PART2_DS	LLIA_WKUP1_DS	RESERVED	

Bits	Field Name	Description	Type	Reset
31:30	UART5_PART1_DS	DS control for uart5 part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
29:28	UART5_PART2_DS	DS control for uart5 part2 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
27:26	UART6_PART1_DS	DS control for uart6 part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2

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Bits	Field Name	Description	Type	Reset
25:24	UART6_PART2_DS	DS control for uart6 part2 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
23:22	WLSDIO_DS	DS control for wlsdio 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
21:20	DSS_PART1_DS	DS control for dss part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
19:18	DSS_PART2_DS	DS control for dss part1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
17:16	C2C_PART3_DS	DS control for c2c part3 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
15:14	C2C_PART4_DS	DS control for c2c part4 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
13:12	UART2_PART2_DS	DS control for uart2 part2 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
11:10	LLIA_WKUP1_DS	DS control for llia wakeup1 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
9:0	RESERVED		R	0x000

Table 18-713. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_2

Control Module Functional Description

- Signal Integrity Parameter Controls Overview: [0]
- SMART I/O Buffers with Slew Rate and Drive Strength Control Settings: [1]
- Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

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- Pad Configuration Programming Points: [13] [14]

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Table 18-713. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_2 (continued)

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- CTRL_MODULE_CORE_PAD Register Summary: [15]

Table 18-714. CONTROL_SMART2IO_PADCONF_0

Address Offset	0x0000 05B4		
Physical Address	0x4A00 2DB4 0x4A00 2DB4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	SMART2 IO control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
ABE_PART0_SC	ABE_PART1_SC	ABE_PART2_SC	ABE_PART3C_SC	ABE_PART4_SC	ABE_PART5_SC	C2C_PART1_SC	C2C_PART2_SC	CAM_SC	DSIPORTA_SC	DSIPORTC_SC	EMMC_SC	HDMI_PART1_SC	DSS_PART1_SC	DSS_PART2_SC	ABE_PART3D_SC

Bits	Field Name	Description	Type	Reset
31:30	ABE_PART0_SC	slew rate control for abe part0 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
29:28	ABE_PART1_SC	slew rate control for abe part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
27:26	ABE_PART2_SC	slew rate control for abe part2 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
25:24	ABE_PART3C_SC	slew rate control for abe part3 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
23:22	ABE_PART4_SC	slew rate control for abe part4 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0

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Bits	Field Name	Description	Type	Reset
21:20	ABE_PART5_SC	slew rate control for abe part5 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
19:18	C2C_PART1_SC	slew rate control for c2c part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
17:16	C2C_PART2_SC	slew rate control for c2c part2 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
15:14	CAM_SC	slew rate control for cam 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
13:12	DSIPORTA_SC	slew rate control for dsiporta 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
11:10	DSIPORTC_SC	slew rate control for dsiportc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
9:8	EMMC_SC	slew rate control for emmc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
7:6	HDMI_PART1_SC	slew rate control for hdmi part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
5:4	DSS_PART1_SC	slew rate control for dss part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0

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Bits	Field Name	Description	Type	Reset
3:2	DSS_PART2_SC	slew rate control for dss part2 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
1:0	ABE_PART3D_SC		RW	0x0

Table 18-715. Register Call Summary for Register CONTROL_SMART2IO_PADCONF_0

Control Module Functional Description • Signal Integrity Parameter Controls Overview: [0] • SMART I/O Buffers with Slew Rate and Drive Strength Control Settings: [1] • Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]
Control Module Programming Guide • Pad Configuration Programming Points: [17] [18] [19]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [20]

Table 18-716. CONTROL_SMART2IO_PADCONF_1

Address Offset	0x0000 05B8		
Physical Address	0x4A00 2DB8 0x4A00 2DB8	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	SMART2 IO control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2 1 0
HSI1_SC	HSI2_SC	MCSPI1_SC	MCSPI2_SC	GPIO_SC	SECURE_SC	TIMER10_SC	TIMER11_SC	TIMER5_SC	TIMER6_SC	TIMER8_SC	UART1_SC	UART2_PART1_SC	UART3_PART1_SC	RESERVED

Bits	Field Name	Description	Type	Reset
31:30	HSI1_SC	slew rate control for hsi1 part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
29:28	HSI2_SC	slew rate control for hsi2 part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
27:26	MCSPI1_SC	slew rate control for mcspi1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0

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Bits	Field Name	Description	Type	Reset
25:24	MCSPI2_SC	slew rate control for mcspi2 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
23:22	GPIO_SC	slew rate control for gpio 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
21:20	SECURE_SC	slew rate control for secure 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
19:18	TIMER10_SC	slew rate control for timer10 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
17:16	TIMER11_SC	slew rate control for timer11 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
15:14	TIMER5_SC	slew rate control for timer5 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
13:12	TIMER6_SC	slew rate control for timer6 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
11:10	TIMER8_SC	slew rate control for timer8 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
9:8	UART1_SC	slew rate control for uart1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0

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Bits	Field Name	Description	Type	Reset
7:6	UART2_PART1_SC	slew rate control for uart2 part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
5:4	UART3_PART1_SC	slew rate control for uart3 part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
3:0	RESERVED		R	0x0

Table 18-717. Register Call Summary for Register CONTROL_SMART2IO_PADCONF_1

Control Module Functional Description
- Signal Integrity Parameter Controls Overview: [0]
- SMART I/O Buffers with Slew Rate and Drive Strength Control Settings: [1]
- Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Control Module Programming Guide
- Pad Configuration Programming Points: [15] [16]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [17]

Table 18-718. CONTROL_SMART2IO_PADCONF_2

Address Offset	0x0000 05BC		
Physical Address	0x4A00 2DBC 0x4A00 2DBC	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	SMART2 IO control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10 9 8	7 6 5 4 3 2 1 0
UART3_PART2_SC	UART5_PART1_SC	UART5_PART2_SC	UART6_PART1_SC	UART6_PART2_SC	WLSDIO_SC	C2C_PART3_SC	C2C_PART4_SC	UART2_PART2_SC	LLIA_WKUP1_SC	RESERVED	

Bits	Field Name	Description	Type	Reset
31:30	UART3_PART2_SC	slew rate control for uart3 part2 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
29:28	UART5_PART1_SC	slew rate control for uart5 part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0

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Bits	Field Name	Description	Type	Reset
27:26	UART5_PART2_SC	slew rate control for uart5 part2 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
25:24	UART6_PART1_SC	slew rate control for uart6 part1 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
23:22	UART6_PART2_SC	slew rate control for uart6 part2 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
21:20	WLSDIO_SC	slew rate control for wlsdio 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
19:18	C2C_PART3_SC	slew rate control for c2c part3 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
17:16	C2C_PART4_SC	slew rate control for c2c part4 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
15:14	UART2_PART2_SC	slew rate control for uart2 part2 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
13:12	LLIA_WKUP1_SC	slew rate control for llia wakeup 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
11:0	RESERVED		R	0x000

Table 18-719. Register Call Summary for Register CONTROL_SMART2IO_PADCONF_2

Control Module Functional Description

- Signal Integrity Parameter Controls Overview: [0]
- SMART I/O Buffers with Slew Rate and Drive Strength Control Settings: [1]
- Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10]

Control Module Programming Guide

- Pad Configuration Programming Points: [11] [12]

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Table 18-719. Register Call Summary for Register CONTROL_SMART2IO_PADCONF_2 (continued)

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [13]

Table 18-720. CONTROL_SMART3IO_PADCONF_0

Address Offset	0x0000 05C0		
Physical Address	0x4A00 2DC0 0x4A00 2DC0	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	SMART3 IO control 0. samrt reflex Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						HDMI_PART2_LB		I2C1_LB		I2C2_LB		I2C3_LB		I2C4_LB		I2C5_LB		RESERVED													

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	HDMI_PART2_LB	lb (internal pull-up resistors for both Fast and High-Speed modes) for control for hdmi_part2 0x0: Fast mode(5-15pf),High-Speed mode(5-12pf) 0x1: Fast mode(15-50pf),High-Speed mode(12-25pf) 0x3: Fast mode(N/A),High-Speed mode(50-80pf) 0x2: Fast mode(50-150pf),High-Speed mode(25-50pf)	RW	0x0
23:22	I2C1_LB	lb (internal pull-up resistors for both Fast and High-Speed modes) for control for i2c1 0x0: Fast mode(5-15pf),High-Speed mode(5-12pf) 0x1: Fast mode(15-50pf),High-Speed mode(12-25pf) 0x3: Fast mode(N/A),High-Speed mode(50-80pf) 0x2: Fast mode(50-150pf),High-Speed mode(25-50pf)	RW	0x1
21:20	I2C2_LB	lb (internal pull-up resistors for both Fast and High-Speed modes) for control for i2c2 0x0: Fast mode(5-15pf),High-Speed mode(5-12pf) 0x1: Fast mode(15-50pf),High-Speed mode(12-25pf) 0x3: Fast mode(N/A),High-Speed mode(50-80pf) 0x2: Fast mode(50-150pf),High-Speed mode(25-50pf)	RW	0x0
19:18	I2C3_LB	lb (internal pull-up resistors for both Fast and High-Speed modes) for control for i2c3 0x0: Fast mode(5-15pf),High-Speed mode(5-12pf) 0x1: Fast mode(15-50pf),High-Speed mode(12-25pf) 0x3: Fast mode(N/A),High-Speed mode(50-80pf) 0x2: Fast mode(50-150pf),High-Speed mode(25-50pf)	RW	0x0

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Bits	Field Name	Description	Type	Reset
17:16	I2C4_LB	lb (internal pull-up resistors for both Fast and High-Speed modes) for control for i2c4 0x0: Fast mode(5-15pf),High-Speed mode(5-12pf) 0x1: Fast mode(15-50pf),High-Speed mode(12-25pf) 0x3: Fast mode(N/A),High-Speed mode(50-80pf) 0x2: Fast mode(50-150pf),High-Speed mode(25-50pf)	RW	0x0
15:14	I2C5_LB	lb (internal pull-up resistors for both Fast and High-Speed modes) for control for i2c5 0x0: Fast mode(5-15pf),High-Speed mode(5-12pf) 0x1: Fast mode(15-50pf),High-Speed mode(12-25pf) 0x3: Fast mode(N/A),High-Speed mode(50-80pf) 0x2: Fast mode(50-150pf),High-Speed mode(25-50pf)	RW	0x0
13:0	RESERVED		R	0x0000

Table 18-721. Register Call Summary for Register CONTROL_SMART3IO_PADCONF_0

Control Module Functional Description
- Signal Integrity Parameter Controls Overview: [0]
- I2Cx I/Os Group PULLUPRESX Controls and Load Range Settings: [1]
- Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [8]

Table 18-722. CONTROL_SMART3IO_PADCONF_1

Address Offset	0x0000 05C4		
Physical Address	0x4A00 2DC4 0x4A00 2DC4	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	SMART3 IO control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30 29	28 27 26	25 24	23 22 21	20 19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
USBB1_I	USBB2_I	USBB3_I	USBB1_SR	USBB2_SR	USBB3_SR	USBB1_HSIC_DATA_WD	USBB1_HSIC_STROBE_WD	USBB2_HSIC_DATA_WD	USBB2_HSIC_STROBE_WD	USBB3_HSIC_DATA_WD	USBB3_HSIC_STROBE_WD	RESERVED	

Bits	Field Name	Description	Type	Reset
31:29	USBB1_I	usbb1 HSIC Impedence control i3:i2:i0 0x0: i0	RW	0x2
28:26	USBB2_I	usbb2 HSIC Impedence control i3:i2:i0 0x0: i0	RW	0x2
25:23	USBB3_I	usbb3 HSIC Impedence control i3:i2:i0 0x0: i0	RW	0x2
22:20	USBB1_SR	usbb1 HSIC Slew Rate control sr2:sr1:sr0 0x0: sr0	RW	0x0

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Bits	Field Name	Description	Type	Reset
19:17	USBB2_SR	usbb2 HSIC Slew Rate control sr2:sr1:sr0 0x0: sr0	RW	0x0
16:14	USBB3_SR	usbb3 HSIC Slew Rate control sr2:sr1:sr0 0x0: sr0	RW	0x0
13:12	USBB1_HSIC_DATA_WD	usbb1 HSIC DATA Weak Driver control i2:i0 0x0:	RW	0x2
11:10	USBB1_HSIC_STROBE_WD	usbb1 HSIC STROBE Weak Driver control i2:i0 0x0:	RW	0x2
9:8	USBB2_HSIC_DATA_WD	usbb2 HSIC DATA Weak Driver control i2:i0 0x0:	RW	0x2
7:6	USBB2_HSIC_STROBE_WD	usbb2 HSIC STROBE Weak Driver control i2:i0 0x0:	RW	0x2
5:4	USBB3_HSIC_DATA_WD	usbb3 HSIC DATA Weak Driver control i2:i0 0x0:	RW	0x2
3:2	USBB3_HSIC_STROBE_WD	usbb3 HSIC STROBE Weak Driver control i2:i0 0x0:	RW	0x2
1:0	RESERVED		R	0x0

Table 18-723. Register Call Summary for Register CONTROL_SMART3IO_PADCONF_1

Control Module Functional Description
- Pull Selection: [0]
- Signal Integrity Parameter Controls Overview: [1]
- High-Speed I/O Buffers With Impedance, Slew Rate, and Weak Driver Settings: [2]
- Device Interfaces Signal Group Controls Mapping: [3] [4] [5] [6] [7] [8]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [9]

Table 18-724. CONTROL_PBIAS

Address Offset	0x0000 0600		
Physical Address	0x4A00 2E00 0x4A00 2E00	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	PBIAS control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDCARD_BIAS_PWRDNZ	SDCARD_IO_PWRDNZ	SDCARD_BIAS_HIZ_MODE	SDCARD_BIAS_SUPPLY_HI_OUT	SDCARD_BIAS_VMODE_ERROR	RESERVED	SDCARD_BIAS_VMODE	RESERVED																						

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27	SDCARD_BIAS_PWRDNZ	PWRDNZ control for SDCARD PBIAS cell 0x0: This signal is used to protect SDCARD PBIAS cell when SDCARD_VDDS is not stable 0x1: SW keep this bit to 1'b1 after SDCARD_VDDS stabilizing	RW	0
26	SDCARD_IO_PWRDNZ	PWRDNZ control for SDCARD I/O cell 0x0: This signal is used to protect SDCARD IOs when SDCARD_VDDS is not stable 0x1: SW keep this bit to 1'b1 after SDCARD_VDDS stabilizing	RW	0
25	SDCARD_BIAS_HIZ_MODE	HIZ_MODE from SDCARD PBIAS 0x0: PBIAS in normal operation mode 0x1: PBIAS output is in high impedence state	RW	0
24	SDCARD_BIAS_SUPPLY_HI_OUT	SUPPLY_HI_OUT from SDCARD PBIAS Read 0x1: SDCARD_VDDS = 3V Read 0x0: SDCARD_VDDS = 1.8V	R	0
23	SDCARD_BIAS_VMODE_ERROR	VMODE ERROR from SDCARD PBIAS Read 0x1: VMODE level is not same as SUPPLY_HI_OUT Read 0x0: VMODE level is same as SUPPLY_HI_OUT	R	0
22	RESERVED		R	0
21	SDCARD_BIAS_VMODE	VMODE control to SDCARD PBIAS. Not applicable when the pad muxing selects SDCARD. When SDCARD is selected by the pad muxing, PBIAS VMODE is directly controlled by the MMCHS IP via bit MMCHS.MMCHS_AC12[19] V1V8_SIGEN 0x0: SDCARD_VDDS = 1.8V 0x1: SDCARD_VDDS = 3V	RW	1
20:0	RESERVED		R	0x00 0000

Table 18-725. Register Call Summary for Register CONTROL_PBIAS

Control Module Functional Description
- Extended-Drain I/O and PBIAS Cell: [0] [1]
- PBIAS Cell: [2]
- Extended-Drain I/O: [3] [4] [5] [6] [7] [8] [9] [10]
- PBIAS Error Generation: [11] [12] [13] [14]
- PBIAS Control Register: [15] [16]

Control Module Programming Guide
- Extended-Drain I/Os and PBIAS Cells Programming Guide: [17] [18] [19] [20] [21] [22] [23] [24] [25] [26]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [27]

Table 18-726. CONTROL_I2C_0

Address Offset	0x0000 0604		
Physical Address	0x4A00 2E04 0x4A00 2E04	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	I2C pads control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C4_SDA_GLFENB	I2C4_SDA_PULLUPRESX	I2C3_SDA_GLFENB	I2C3_SDA_PULLUPRESX	I2C2_SDA_GLFENB	I2C2_SDA_PULLUPRESX	I2C1_PMIC_SDA_GLFENB	I2C1_PMIC_SDA_PULLUPRESX	I2C4_SCL_GLFENB	I2C4_SCL_PULLUPRESX	I2C3_SCL_GLFENB	I2C3_SCL_PULLUPRESX	I2C2_SCL_GLFENB	I2C2_SCL_PULLUPRESX	I2C1_PMIC_SCL_GLFENB	I2C1_PMIC_SCL_PULLUPRESX	I2C5_SDA_GLFENB	I2C5_SDA_PULLUPRESX	I2C5_SCL_GLFENB	I2C5_SCL_PULLUPRESX	RESERVED											

Bits	Field Name	Description	Type	Reset
31	I2C4_SDA_GLFENB	Active_high glitch free operation enable pin for i2c4 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
30	I2C4_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c4 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	1
29	I2C3_SDA_GLFENB	Active_high glitch free operation enable pin for i2c3 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
28	I2C3_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c3 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	1
27	I2C2_SDA_GLFENB	Active_high glitch free operation enable pin for i2c2 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
26	I2C2_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c2 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	1
25	I2C1_PMIC_SDA_GLFENB	Active_high glitch free operation enable pin for i2c1_pmic receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
24	I2C1_PMIC_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c1_pmic 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
23	I2C4_SCL_GLFENB	Active_high glitch free operation enable pin for i2c4 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
22	I2C4_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c4 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	1
21	I2C3_SCL_GLFENB	Active_high glitch free operation enable pin for i2c3 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0

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Bits	Field Name	Description	Type	Reset
20	I2C3_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c3 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	1
19	I2C2_SCL_GLFENB	Active_high glitch free operation enable pin for i2c2 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
18	I2C2_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c2 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	1
17	I2C1_PMIC_SCL_GLFENB	Active_high glitch free operation enable pin for i2c1_pmic receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
16	I2C1_PMIC_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c1_pmic 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
15	I2C5_SDA_GLFENB	Active_high glitch free operation enable pin for i2c5 receiver 0x0: Disable i2c5 glitch free operation 0x1: Enable i2c5 glitch free operation	RW	0
14	I2C5_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c5 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	1
13	I2C5_SCL_GLFENB	Active_high glitch free operation enable pin for i2c5 receiver 0x0: Disable i2c5 glitch free operation 0x1: Enable i2c5 glitch free operation	RW	0
12	I2C5_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c5 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	1
11:0	RESERVED		R	0x000

Table 18-727. Register Call Summary for Register CONTROL_I2C_0

Control Module Functional Description

- Signal Integrity Parameter Controls Overview: [0]
- I2Cx I/Os Group PULLUPRESX Controls and Load Range Settings: [1]
- Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [22]

Table 18-728. CONTROL_CAMERA_RX

Address Offset	0x0000 0608		
Physical Address	0x4A00 2E08 0x4A00 2E08	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	CAMERA RX control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31 30 29 28 27	26	25 24	23 22	21	20	19 18 17 16	15 14 13	12 11	10	9	8	7 6 5 4 3	2 1	0
RESERVED	CSIPORTC_MODE	CSIPORTC_LANEENABLE	CSIPORTC_CAMMODE	CSIPORTC_CTRLCLKEN	CSIPORTC_SEL_N	RESERVED	CSIPORTB_MODE	CSIPORTB_LANEENABLE	CSIPORTB_CAMMODE	CSIPORTB_CTRLCLKEN	RESERVED	CSIPORTA_MODE	CSIPORTA_LANEENABLE	CSIPORTA_CAMMODE	CSIPORTA_CTRLCLKEN

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	CSIPORTC_MODE	portc camera MODE	RW	0
25:24	CSIPORTC_LANEENABLE	portc camera Lane Enable 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x0
23:22	CSIPORTC_CAMMODE	portc camera CAMMODE control 0x0: DPHY mode 0x1: Data/Strobe Transmission for mat 0x3: GPI mode 0x2: Data/Clock Transmission for mat	RW	0x3
21	CSIPORTC_CTRLCLKEN	portc cameraclock enable control. This is the internal PHY CTRLCLK driven from CSI_PHY_CTRL_FCLK. 0x0: Disable for CTRLCLK 0x1: Active high enable for CTRLCLK	RW	0
20	CSIPORTC_SEL_N	select port 0x0: select portc 0x1: select portb	RW	0
19:17	RESERVED		R	0x0
16	CSIPORTB_MODE	portb camera MODE	RW	0
15:13	CSIPORTB_LANEENABLE	portb camera Lane Enable 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x0
12:11	CSIPORTB_CAMMODE	portb camera CAMMODE control 0x0: DPHY mode 0x1: Data/Strobe Transmission for mat 0x3: GPI mode 0x2: Data/Clock Transmission for mat	RW	0x3
10	CSIPORTB_CTRLCLKEN	portb camera clock enable control. This is the internal PHY CTRLCLK driven from CSI_PHY_CTRL_FCLK. 0x0: Disable for CTRLCLK 0x1: Active high enable for CTRLCLK	RW	0
9	RESERVED		R	0
8	CSIPORTA_MODE	porta camera MODE	RW	0
7:3	CSIPORTA_LANEENABLE	porta camera Lane Enable 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x00

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Bits	Field Name	Description	Type	Reset
2:1	CSIPORTA_CAMMODE	porta camera CAMMODE control 0x0: DPHY mode 0x1: Data/Strobe Transmission for mat 0x3: GPI mode 0x2: Data/Clock Transmission for mat	RW	0x3
0	CSIPORTA_CTRLCLKEN	porta cameraclock enable control. This is the internal PHY CTRLCLK driven from CSI_PHY_CTRL_FCLK. 0x0: Disable for CTRLCLK 0x1: Active high enable for CTRLCLK	RW	0

Table 18-729. Register Call Summary for Register CONTROL_CAMERA_RX

Control Module Functional Description • CSI Receiver Control Register: [0] [1]
Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [2]

Table 18-730. CONTROL_HDMI_TX_PHY

Address Offset	0x0000 060C		
Physical Address	0x4A00 2E0C 0x4A00 2E0C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	HDMI TX PHY control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	HDMITXPHY_TXVALID	HDMITXPHY_ENBYPASSCLK	HDMITXPHY_PD_PULLUPDET	RESERVED																											

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	RW	0
30	HDMITXPHY_TXVALID		RW	0
29	HDMITXPHY_ENBYPASSCLK		RW	0
28	HDMITXPHY_PD_PULLUPDET		RW	1
27:0	RESERVED	Reserved	R	0x000 0000

Table 18-731. Register Call Summary for Register CONTROL_HDMI_TX_PHY

Control Module Register Manual • CTRL_MODULE_CORE_PAD Register Summary: [0]

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Table 18-732. CONTROL_DSIPHY

Address Offset	0x0000 0614		
Physical Address	0x4A00 2E14 0x4A00 2E14	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DSIPHY control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			DSIPORTA_LANEENABLE					DSIPORTC_LANEENABLE								RESERVED															

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	DSIPORTA_LANEENABLE	DSI porta Lane Enable 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x00
23:19	DSIPORTC_LANEENABLE	DSI portc Lane Enable 0x0: Pull down enabled 0x1: Pull down disabled	RW	0x00
18:0	RESERVED		R	0x0 0000

Table 18-733. Register Call Summary for Register CONTROL_DSIPHY

Control Module Register Manual

- CTRL_MODULE_CORE_PAD Register Summary: [0]

Table 18-734. CONTROL_MCBSPLP

Address Offset	0x0000 0618		
Physical Address	0x4A00 2E18 0x4A00 2E18	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	McBSPLP control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALBCTRLRX_FSX	ALBCTRLRX_CLKX							RESERVED																							

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Bits	Field Name	Description	Type	Reset
31	ALBCTRLRX_FSX	Analog loop_back control for FSX 0x0: PIFSR is used 0x1: PIFSX is used instead of PIFSR 4pin mode	RW	0
30	ALBCTRLRX_CLKX	Analog loop_back control for CLKX 0x0: PICLKR is used 0x1: PICLKX is used instead of PICLKR 4pin mode	RW	0
29:0	RESERVED		R	0x0000 0000

Table 18-735. Register Call Summary for Register CONTROL_MCBSPLP

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [0]

Table 18-736. CONTROL_USB2PHYCORE

Address Offset	0x0000 061C		
Physical Address	0x4A00 2E1C 0x4A00 2E1C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	USB2PHYCORE control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USB2PHY_AUTORESUME_EN	USB2PHY_DISCHGDET	USB2PHY_GPIOMODE	USB2PHY_CHG_DET_EXT_CTL	USB2PHY_RDM_PD_CHGDET_EN	USB2PHY_RDP_PU_CHGDET_EN	USB2PHY_CHG_VSRC_EN	USB2PHY_CHG_ISINK_EN	USB2PHY_CHG_DET_STATUS			USB2PHY_CHG_DET_DM_COMP	USB2PHY_CHG_DET_DP_COMP	USB2PHY_DATADET	USB2PHY_SINKONDP	USB2PHY_SRCONDM	USB2PHY_RESTARTCHGDET	USB2PHY_CHGDETDONE	USB2PHY_CHGDETECTED	USB2PHY_MCPCPUEN	USB2PHY_MCPCMODEEN	USB2PHY_RESETDONEMCLK	USB2PHY_UTMIRESETDONE	RESERVED	USB2PHY_DATAPOLARITYN	USBDPLL_FREQLOCK	USB2PHY_RESETDONETCLK	RESERVED			

Bits	Field Name	Description	Type	Reset
31	USB2PHY_AUTORESUME_EN	Auto resume enable 0x0: disable autoresume 0x1: enable autoresume	RW	0
30	USB2PHY_DISCHGDET	Disable charger detect 0x0: charger detect function enabled 0x1: charger detect function disabled	RW	0
29	USB2PHY_GPIOMODE	GPIO mode 0x0: USB mode enabled 0x1: GPIO mode enabled	RW	0
28	USB2PHY_CHG_DET_EXT_CTL	Charge detect external control 0x0: charger detect internal state machine used 0x1: charge detect statemachine is bypassed	RW	0
27	USB2PHY_RDM_PD_CHGDET_EN	DM Pull down control 0x0: PD disabled 0x1: PD enabled	RW	0

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Bits	Field Name	Description	Type	Reset
26	USB2PHY_RDP_PU_CHGDET_EN	DP Pull up control 0x0: PU disabled 0x1: PU enabled	RW	0
25	USB2PHY_CHG_VSRC_EN	VSRC enable on DP line-Host charger case 0x0: disable VSRC drive on DP 0x1: drives VSRC 600mV on DP line	RW	0
24	USB2PHY_CHG_ISINK_EN	ISINK enable on DM line-Host charger case 0x0: disable the isink on DM 0x1: enables the ISINK (100uA) on DM line	RW	0
23:21	USB2PHY_CHG_DET_STATUS	Status of charger detection Read 0x3: Unknown error Read 0x4: Dedicated charger Read 0x2: PS/2 Read 0x0: Wait state Read 0x6: PC Read 0x1: No contact Read 0x7: Interrupt Read 0x5: HOST charger	R	0x0
20	USB2PHY_CHG_DET_DM_COMP	Output of the comparator on DM during the resistor host detect protocol Read 0x1: DM line is above 0.75V to 0.95V Read 0x0: DM line is below 0.75V to 0.95V	R	0
19	USB2PHY_CHG_DET_DP_COMP	Output of the comparator on DP during the resistor host detect protocol Read 0x1: DP line is above 0.75V to 0.95V Read 0x0: DP line is below 0.75V to 0.95V	R	1
18	USB2PHY_DATADET	Output of the charger detect comparator Read 0x1: DM line is above 0.25V to 0.4V Read 0x0: DM line is below 0.25V to 0.4V	R	0
17	USB2PHY_SINKONDP	When '1' current sink is connected to DP instead of DM 0x0: Default value 0x1: enables the ISINK on DP instead of DM	RW	0
16	USB2PHY_SRCONDM	When '1' voltage source is connected to DP instead of DM 0x0: Default value 0x1: enable the VSRC on DM instead of DP	RW	0
15	USB2PHY_RESTARTCHGDET	restartchgdet = '1' for 1 msec cause the CD_START to reset 0x0: Default value 0x1: a high pulse of 1 msec causes the charger detect to restart on negative edge of restartchgdet	RW	0
14	USB2PHY_CHGDETDONE	Status indicates that charger detection protocol is over Read 0x1: charger detection protocol is over Read 0x0: charger detection protocol is not over	R	0
13	USB2PHY_CHGDETECTED	Output of the charger detection protocol Read 0x1: charger detected Read 0x0: charger not detected	R	0
12	USB2PHY_MCPCPUEN	MCPC Pull up enable 0x0: disable the MCPC pull up 0x1: enable the 4.7K to10K pull up on receive line DP when datapolarityn is 0 and DM when datapolarityn is 1	RW	0

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Bits	Field Name	Description	Type	Reset
11	USB2PHY_MCPCMODEEN	MCPC Mode enable 0x0: disable MCPC mode 0x1: enable MCPC mode	RW	0
10	USB2PHY_RESETDONEMCLK	OCP reset status Read 0x1: OCP domain is out of reset Read 0x0: OCP domain is in reset	R	0
9	USB2PHY_UTMIRESETDONE	UTMI FSM reset status Read 0x1: UTMI FSMs are out of reset Read 0x0: UTMI FSMs are in reset	R	0
8	RESERVED		R	0
7	USB2PHY_DATAPOLARITYN	Data polarity 0x0: DP functionality is on DP and DM funcationality is on DM 0x1: DP functionality is on DM and DM functionality is on DP	RW	0
6	USBDPLL_FREQLOCK	Status from USB DPLL	R	0
5	USB2PHY_RESETDONETCLK	resetdonetclk status from USB2PHY	R	0
4:0	RESERVED		R	0x00

Table 18-737. Register Call Summary for Register CONTROL_USB2PHYCORE

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [0]

Table 18-738. CONTROL_HDMI_1

Address Offset	0x0000 0620		
Physical Address	0x4A00 2E20 0x4A00 2E20	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	HDMI pads control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HDMI_DDC_SDA_GLFENB	HDMI_DDC_SDA_PULLUPRESX	HDMI_DDC_SCL_GLFENB	HDMI_DDC_SCL_PULLUPRESX	HDMI_DDC_SDA_HSMODE	HDMI_DDC_SCL_HSMODE	RESERVED																									

Bits	Field Name	Description	Type	Reset
31	HDMI_DDC_SDA_GLFENB	Active_high glitch free operation enable pin for hdmi_ddc_sda receiver 0x0: Disable hdmi_ddc_sda glitch free operation 0x1: Enable hdmi_ddc_sda glitch free operation	RW	0

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Bits	Field Name	Description	Type	Reset
30	HDMI_DDC_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for hdmi_ddc_sda 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
29	HDMI_DDC_SCL_GLFENB	Active_high glitch free operation enable pin for hdmi_ddc_scl receiver 0x0: Disable hdmi_ddc_sc glitch free operation 0x1: Enable hdmi_ddc_sc glitch free operation	RW	0
28	HDMI_DDC_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for hdmi_ddc_scl 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
27	HDMI_DDC_SDA_HSMODE	Active-high selection for I2C High-Speed mode 0x0: I2C Standard/Fast mode 0x1: Enable I2C High speed mode	RW	0
26	HDMI_DDC_SCL_HSMODE	Active-high selection for I2C High-Speed mode 0x0: I2C Standard/Fast mode 0x1: Enable I2C High speed mode	RW	0
25:0	RESERVED		R	0x000 0000

Table 18-739. Register Call Summary for Register CONTROL_HDMI_1

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [0]

Table 18-740. CONTROL_DDR3CH1_0

Address Offset	0x0000 0630		
Physical Address	0x4A00 2E30 0x4A00 2E30	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDR3CH1 control For more information about pad group assignment and signal group parameter controls, see Section 18.4.12.7.1, *Signal Integrity Parameter Controls Overview,* and Table 18-78. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDR3CH1_PART0_I			DDR3CH1_PART0_SR			DDR3CH1_PART0_WD		DDR3CH1_PART5A_I			DDR3CH1_PART5A_SR			DDR3CH1_PART5A_WD		DDR3CH1_PART5B_I			DDR3CH1_PART5B_SR			DDR3CH1_PART5B_WD		DDR3CH1_PART6_I			DDR3CH1_PART6_SR			DDR3CH1_PART6_WD	

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Bits	Field Name	Description	Type	Reset
31:29	DDR3CH1_PART0_I	Group 0 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
28:26	DDR3CH1_PART0_SR	Group 0 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
25:24	DDR3CH1_PART0_WD	Group 0 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
23:21	DDR3CH1_PART5A_I	Group 5 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
20:18	DDR3CH1_PART5A_SR	Group 5 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
17:16	DDR3CH1_PART5A_WD	Group 5 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
15:13	DDR3CH1_PART5B_I	Group 6 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2

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Bits	Field Name	Description	Type	Reset
12:10	DDR3CH1_PART5B_SR	Group 6 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
9:8	DDR3CH1_PART5B_WD	Group 6 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
7:5	DDR3CH1_PART6_I	Group 6 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
4:2	DDR3CH1_PART6_SR	Group 6 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
1:0	DDR3CH1_PART6_WD	Group 6 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

Table 18-741. Register Call Summary for Register CONTROL_DDR3CH1_0

Control Module Functional Description
- Signal Integrity Parameter Controls Overview: [0]
- Device Interfaces Signal Group Controls Mapping: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [13]

Table 18-742. CONTROL_DDR3CH2_0

Address Offset	0x0000 0634		
Physical Address	0x4A00 2E34 0x4A00 2E34	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDR3CH2 control For more information about pad group assignment and signal group parameter controls, see Section 18.4.12.7.1, *Signal Integrity Parameter Controls Overview,* and Table 18-78. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31 30 29	28 27 26	25 24	23 22 21	20 19 18	17 16	15 14 13	12 11 10	9 8	7 6 5	4 3	2 1 0
DDR3CH2_PART0_I	DDR3CH2_PART0_SR	DDR3CH2_PART0_WD	DDR3CH2_PART5A_I	DDR3CH2_PART5A_SR	DDR3CH2_PART5A_WD	DDR3CH2_PART5B_I	DDR3CH2_PART5B_SR	DDR3CH2_PART5B_WD	DDR3CH2_PART6_I	DDR3CH2_PART6_SR	DDR3CH2_PART6_WD

Bits	Field Name	Description	Type	Reset
31:29	DDR3CH2_PART0_I	Group 0 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
28:26	DDR3CH2_PART0_SR	Group 0 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
25:24	DDR3CH2_PART0_WD	Group 0 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
23:21	DDR3CH2_PART5A_I	Group 5 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
20:18	DDR3CH2_PART5A_SR	Group 5 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
17:16	DDR3CH2_PART5A_WD	Group 5 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

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Bits	Field Name	Description	Type	Reset
15:13	DDR3CH2_PART5B_I	Group 6 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
12:10	DDR3CH2_PART5B_SR	Group 6 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
9:8	DDR3CH2_PART5B_WD	Group 6 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
7:5	DDR3CH2_PART6_I	Group 6 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
4:2	DDR3CH2_PART6_SR	Group 6 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
1:0	DDR3CH2_PART6_WD	Group 6 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

Table 18-743. Register Call Summary for Register CONTROL_DDR3CH2_0

Control Module Functional Description

- Signal Integrity Parameter Controls Overview: [0]
- Device Interfaces Signal Group Controls Mapping: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

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- CTRL_MODULE_CORE_PAD Register Summary: [13]

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Table 18-744. CONTROL_DDRCH1_0

Address Offset	0x0000 0638		
Physical Address	0x4A00 2E38 0x4A00 2E38	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDRCH1 control 0 For more information about pad group assignment and signal group parameter controls, see Section 18.4.12.7.1, *Signal Integrity Parameter Controls Overview,* and Table 18-78. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDRCH1_PART1A_I			DDRCH1_PART1A_SR			DDRCH1_PART1A_WD		DDRCH1_PART1B_I			DDRCH1_PART1B_SR			DDRCH1_PART1B_WD		DDRCH1_PART2A_I			DDRCH1_PART2A_SR			DDRCH1_PART2A_WD		DDRCH1_PART2B_I			DDRCH1_PART2B_SR			DDRCH1_PART2B_WD	

Bits	Field Name	Description	Type	Reset
31:29	DDRCH1_PART1A_I	Group 1a Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
28:26	DDRCH1_PART1A_SR	Group 1a Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
25:24	DDRCH1_PART1A_WD	Group 1a Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
23:21	DDRCH1_PART1B_I	Group 1b Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2

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Bits	Field Name	Description	Type	Reset
20:18	DDRCH1_PART1B_SR	Group 1b Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
17:16	DDRCH1_PART1B_WD	Group 1b Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
15:13	DDRCH1_PART2A_I	Group 2a Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
12:10	DDRCH1_PART2A_SR	Group 2a Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
9:8	DDRCH1_PART2A_WD	Group 2a Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
7:5	DDRCH1_PART2B_I	Group 2b Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
4:2	DDRCH1_PART2B_SR	Group 2b Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
1:0	DDRCH1_PART2B_WD	Group 2b Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

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Table 18-745. Register Call Summary for Register CONTROL_DDRCH1_0

Control Module Functional Description

- Signal Integrity Parameter Controls Overview: [0]
- Device Interfaces Signal Group Controls Mapping: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

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- CTRL_MODULE_CORE_PAD Register Summary: [13]

Table 18-746. CONTROL_DDRCH1_1

Address Offset	0x0000 063C		
Physical Address	0x4A00 2E3C 0x4A00 2E3C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDRCH1 control 1 For more information about pad group assignment and signal group parameter controls, see Section 18.4.12.7.1, *Signal Integrity Parameter Controls Overview,* and Table 18-78. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30 29	28 27 26	25 24	23 22 21	20 19 18	17 16	15 14 13	12 11 10	9 8	7 6 5	4 3 2	1 0
DDRCH1_PART3A_I	DDRCH1_PART3A_SR	DDRCH1_PART3A_WD	DDRCH1_PART3B_I	DDRCH1_PART3B_SR	DDRCH1_PART3B_WD	DDRCH1_PART4A_I	DDRCH1_PART4A_SR	DDRCH1_PART4A_WD	DDRCH1_PART4B_I	DDRCH1_PART4B_SR	DDRCH1_PART4B_WD

Bits	Field Name	Description	Type	Reset
31:29	DDRCH1_PART3A_I	Group 3a Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
28:26	DDRCH1_PART3A_SR	Group 3a Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
25:24	DDRCH1_PART3A_WD	Group 3a Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

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Bits	Field Name	Description	Type	Reset
23:21	DDRCH1_PART3B_I	Group 3b Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
20:18	DDRCH1_PART3B_SR	Group 3b Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
17:16	DDRCH1_PART3B_WD	Group 3b Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
15:13	DDRCH1_PART4A_I	Group 4a Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
12:10	DDRCH1_PART4A_SR	Group 4a Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
9:8	DDRCH1_PART4A_WD	Group 4a Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
7:5	DDRCH1_PART4B_I	Group 4b Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2

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Bits	Field Name	Description	Type	Reset
4:2	DDRCH1_PART4B_SR	Group 4b Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
1:0	DDRCH1_PART4B_WD	Group 4b Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

Table 18-747. Register Call Summary for Register CONTROL_DDRCH1_1

Control Module Functional Description
- Signal Integrity Parameter Controls Overview: [0]
- Device Interfaces Signal Group Controls Mapping: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [13]

Table 18-748. CONTROL_DDRCH2_0

Address Offset	0x0000 0640		
Physical Address	0x4A00 2E40 0x4A00 2E40	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDRCH2 control 0 For more information about pad group assignment and signal group parameter controls, see Section 18.4.12.7.1, *Signal Integrity Parameter Controls Overview,* and Table 18-78. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDRCH2_PART1A_I			DDRCH2_PART1A_SR			DDRCH2_PART1A_WD		DDRCH2_PART1B_I			DDRCH2_PART1B_SR			DDRCH2_PART1B_WD		DDRCH2_PART2A_I			DDRCH2_PART2A_SR			DDRCH2_PART2A_WD		DDRCH2_PART2B_I			DDRCH2_PART2B_SR			DDRCH2_PART2B_WD	

Bits	Field Name	Description	Type	Reset
31:29	DDRCH2_PART1A_I	Group 1a Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2

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Bits	Field Name	Description	Type	Reset
28:26	DDRCH2_PART1A_SR	Group 1a Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
25:24	DDRCH2_PART1A_WD	Group 1a Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
23:21	DDRCH2_PART1B_I	Group 1b Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
20:18	DDRCH2_PART1B_SR	Group 1b Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
17:16	DDRCH2_PART1B_WD	Group 1b Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
15:13	DDRCH2_PART2A_I	Group 2a Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
12:10	DDRCH2_PART2A_SR	Group 2a Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
9:8	DDRCH2_PART2A_WD	Group 2a Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

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Bits	Field Name	Description	Type	Reset
7:5	DDRCH2_PART2B_I	Group 2b Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
4:2	DDRCH2_PART2B_SR	Group 2b Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
1:0	DDRCH2_PART2B_WD	Group 2b Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

Table 18-749. Register Call Summary for Register CONTROL_DDRCH2_0

Control Module Functional Description
- Signal Integrity Parameter Controls Overview: [0]
- Device Interfaces Signal Group Controls Mapping: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [13]

Table 18-750. CONTROL_DDRCH2_1

Address Offset	0x0000 0644		
Physical Address	0x4A00 2E44 0x4A00 2E44	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDRCH2 control 1 For more information about pad group assignment and signal group parameter controls, see Section 18.4.12.7.1, *Signal Integrity Parameter Controls Overview,* and Table 18-78. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDRCH2_PART3A_I			DDRCH2_PART3A_SR			DDRCH2_PART3A_WD		DDRCH2_PART3B_I			DDRCH2_PART3B_SR			DDRCH2_PART3B_WD		DDRCH2_PART4A_I			DDRCH2_PART4A_SR			DDRCH2_PART4A_WD		DDRCH2_PART4B_I			DDRCH2_PART4B_SR			DDRCH2_PART4B_WD	

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Bits	Field Name	Description	Type	Reset
31:29	DDRCH2_PART3A_I	Group 3a Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
28:26	DDRCH2_PART3A_SR	Group 3a Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
25:24	DDRCH2_PART3A_WD	Group 3a Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
23:21	DDRCH2_PART3B_I	Group 3b Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
20:18	DDRCH2_PART3B_SR	Group 3b Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
17:16	DDRCH2_PART3B_WD	Group 3b Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
15:13	DDRCH2_PART4A_I	Group 4a Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2

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Bits	Field Name	Description	Type	Reset
12:10	DDRCH2_PART4A_SR	Group 4a Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
9:8	DDRCH2_PART4A_WD	Group 4a Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
7:5	DDRCH2_PART4B_I	Group 4b Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
4:2	DDRCH2_PART4B_SR	Group 4b Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
1:0	DDRCH2_PART4B_WD	Group 4b Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

Table 18-751. Register Call Summary for Register CONTROL_DDRCH2_1

Control Module Functional Description

- Signal Integrity Parameter Controls Overview: [0]
- Device Interfaces Signal Group Controls Mapping: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]

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- CTRL_MODULE_CORE_PAD Register Summary: [13]

Table 18-752. CONTROL_LPDDR2CH1_0

Address Offset	0x0000 0648		
Physical Address	0x4A00 2E48 0x4A00 2E48	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	LPDDR2 1 IO control 0 For more information about pad group assignment and signal group parameter controls, see Section 18.4.12.7.1, *Signal Integrity Parameter Controls Overview,* and Table 18-78. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31 30 29	28 27 26	25 24	23 22 21	20 19 18	17 16	15 14 13	12 11 10	9 8	7 6 5 4 3 2 1 0
LPDDR2CH1_PART0_I	LPDDR2CH1_PART0_SR	LPDDR2CH1_PART0_WD	LPDDR2CH1_PART5_I	LPDDR2CH1_PART5_SR	LPDDR2CH1_PART5_WD	LPDDR2CH1_PART6_I	LPDDR2CH1_PART6_SR	LPDDR2CH1_PART6_WD	RESERVED

Bits	Field Name	Description	Type	Reset
31:29	LPDDR2CH1_PART0_I	Group 0 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
28:26	LPDDR2CH1_PART0_SR	Group 0 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
25:24	LPDDR2CH1_PART0_WD	Group 0 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
23:21	LPDDR2CH1_PART5_I	Group 5 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
20:18	LPDDR2CH1_PART5_SR	Group 5 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
17:16	LPDDR2CH1_PART5_WD	Group 5 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2

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Bits	Field Name	Description	Type	Reset
15:13	LPDDR2CH1_PART6_I	Group 6 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
12:10	LPDDR2CH1_PART6_SR	Group 6 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
9:8	LPDDR2CH1_PART6_WD	Group 6 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
7:0	RESERVED		R	0x00

Table 18-753. Register Call Summary for Register CONTROL_LPDDR2CH1_0

Control Module Functional Description
- Pull Selection: [0]
- Signal Integrity Parameter Controls Overview: [1]
- Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [11]

Table 18-754. CONTROL_LPDDR2CH1_1

Address Offset	0x0000 064C		
Physical Address	0x4A00 2E4C 0x4A00 2E4C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	LPDDR2 1 IO control 1 For more information about pad group assignment and signal group parameter controls, see Section 18.4.12.7.1, *Signal Integrity Parameter Controls Overview,* and Table 18-78. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPDDR2CH2_PART0_I			LPDDR2CH2_PART0_SR			LPDDR2CH2_PART0_WD		LPDDR2CH2_PART5_I			LPDDR2CH2_PART5_SR			LPDDR2CH2_PART5_WD		LPDDR2CH2_PART6_I			LPDDR2CH2_PART6_SR			LPDDR2CH2_PART6_WD		RESERVED							

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Bits	Field Name	Description	Type	Reset
31:29	LPDDR2CH2_PART0_I	Group 0 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
28:26	LPDDR2CH2_PART0_SR	Group 0 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
25:24	LPDDR2CH2_PART0_WD	Group 0 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
23:21	LPDDR2CH2_PART5_I	Group 5 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2
20:18	LPDDR2CH2_PART5_SR	Group 5 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
17:16	LPDDR2CH2_PART5_WD	Group 5 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
15:13	LPDDR2CH2_PART6_I	Group 6 Impedence control i3:i2:i0 0x6: for Drv11 0x1: for Drv6 0x7: Drv12 0x0: for Drv5 0x2: for Drv7 0x4: for Drv9 0x5: for Drv10 0x3: for Drv8	RW	0x2

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Bits	Field Name	Description	Type	Reset
12:10	LPDDR2CH2_PART6_SR	Group 6 Slew Rate control sr2:sr1:sr0 0x0: Turn_on time 125ps for Drv8 0x1: Turn_on time 500ps for Drv8 0x3: Turn_on time 750ps for Drv8 0x2: Turn_on time 325ps for Drv8	RW	0x2
9:8	LPDDR2CH2_PART6_WD	Group 6 Weak driver control wd1:wd0 0x0: Pull logic disabled 0x1: pull up 0x3: Maintain the previous output value 0x2: pull down	RW	0x2
7:0	RESERVED		R	0x00

Table 18-755. Register Call Summary for Register CONTROL_LPDDR2CH1_1

Control Module Functional Description
- Pull Selection: [0]
- Signal Integrity Parameter Controls Overview: [1]
- Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [11]

Table 18-756. CONTROL_DDRIO_0

Address Offset	0x0000 0650		
Physical Address	0x4A00 2E50 0x4A00 2E50	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDR CONTROL 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDR3CH1_VREF_CA0_CCAP0	DDR3CH1_VREF_CA0_CCAP1	DDR3CH1_VREF_CA0_TAP0	DDR3CH1_VREF_CA0_TAP1	DDR3CH1_VREF_CA0_EN	RESERVED	DDR3CH2_VREF_CA0_CCAP0	DDR3CH2_VREF_CA0_CCAP1	DDR3CH2_VREF_CA0_TAP0	DDR3CH2_VREF_CA0_TAP1	DDR3CH2_VREF_CA0_EN	RESERVED	DDRCH1_VREF_DQ0_INT_CCAP0	DDRCH1_VREF_DQ0_INT_CCAP1	DDRCH1_VREF_DQ0_INT_TAP0	DDRCH1_VREF_DQ0_INT_TAP1	DDRCH1_VREF_DQ0_INT_EN	DDRCH1_VREF_DQ1_INT_CCAP0	DDRCH1_VREF_DQ1_INT_CCAP1	DDRCH1_VREF_DQ1_INT_TAP0	DDRCH1_VREF_DQ1_INT_TAP1	DDRCH1_VREF_DQ1_INT_EN	DDRCH1_VREF_DQ2_INT_CCAP0	DDRCH1_VREF_DQ2_INT_CCAP1	DDRCH1_VREF_DQ2_INT_TAP0	DDRCH1_VREF_DQ2_INT_TAP1	DDRCH1_VREF_DQ2_INT_EN	DDRCH1_VREF_DQ3_INT_CCAP0	DDRCH1_VREF_DQ3_INT_CCAP1	DDRCH1_VREF_DQ3_INT_TAP0	DDRCH1_VREF_DQ3_INT_TAP1	DDRCH1_VREF_DQ3_INT_EN

Bits	Field Name	Description	Type	Reset
31	DDR3CH1_VREF_CA0_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
30	DDR3CH1_VREF_CA0_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
29	DDR3CH1_VREF_CA0_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
28	DDR3CH1_VREF_CA0_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
27	DDR3CH1_VREF_CA0_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
26	RESERVED		R	0
25	DDR3CH2_VREF_CA0_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
24	DDR3CH2_VREF_CA0_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
23	DDR3CH2_VREF_CA0_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
22	DDR3CH2_VREF_CA0_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
21	DDR3CH2_VREF_CA0_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
20	RESERVED		R	0
19	DDRCH1_VREF_DQ0_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
18	DDRCH1_VREF_DQ0_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
17	DDRCH1_VREF_DQ0_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
16	DDRCH1_VREF_DQ0_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
15	DDRCH1_VREF_DQ0_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
14	DDRCH1_VREF_DQ1_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
13	DDRCH1_VREF_DQ1_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
12	DDRCH1_VREF_DQ1_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
11	DDRCH1_VREF_DQ1_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
10	DDRCH1_VREF_DQ1_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
9	DDRCH1_VREF_DQ2_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
8	DDRCH1_VREF_DQ2_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
7	DDRCH1_VREF_DQ2_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
6	DDRCH1_VREF_DQ2_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
5	DDRCH1_VREF_DQ2_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
4	DDRCH1_VREF_DQ3_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
3	DDRCH1_VREF_DQ3_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
2	DDRCH1_VREF_DQ3_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
1	DDRCH1_VREF_DQ3_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
0	DDRCH1_VREF_DQ3_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1

Table 18-757. Register Call Summary for Register CONTROL_DDRIO_0

Control Module Functional Description

- Reference Voltage for Device LPDDR2/DDR3 I/O Buffers and LPDDR2/DDR3 Memory: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32]

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- CTRL_MODULE_CORE_PAD Register Summary: [33]

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Table 18-758. CONTROL_DDRIO_1

Address Offset	0x0000 0654		
Physical Address	0x4A00 2E54 0x4A00 2E54	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDR CONTROL 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDRCH1_VREF_DQ_OUT_CCAP0	DDRCH1_VREF_DQ_OUT_CCAP1	DDRCH1_VREF_DQ_OUT_TAP0	DDRCH1_VREF_DQ_OUT_TAP1	DDRCH1_VREF_DQ_OUT_EN	DDRCH2_VREF_DQ0_INT_CCAP0	DDRCH2_VREF_DQ0_INT_CCAP1	DDRCH2_VREF_DQ0_INT_TAP0	DDRCH2_VREF_DQ0_INT_TAP1	DDRCH2_VREF_DQ0_INT_EN	DDRCH2_VREF_DQ1_INT_CCAP0	DDRCH2_VREF_DQ1_INT_CCAP1	DDRCH2_VREF_DQ1_INT_TAP0	DDRCH2_VREF_DQ1_INT_TAP1	DDRCH2_VREF_DQ1_INT_EN	DDRCH2_VREF_DQ2_INT_CCAP0	DDRCH2_VREF_DQ2_INT_CCAP1	DDRCH2_VREF_DQ2_INT_TAP0	DDRCH2_VREF_DQ2_INT_TAP1	DDRCH2_VREF_DQ2_INT_EN	DDRCH2_VREF_DQ3_INT_CCAP0	DDRCH2_VREF_DQ3_INT_CCAP1	DDRCH2_VREF_DQ3_INT_TAP0	DDRCH2_VREF_DQ3_INT_TAP1	DDRCH2_VREF_DQ3_INT_EN	DDRCH2_VREF_DQ_OUT_CCAP0	DDRCH2_VREF_DQ_OUT_CCAP1	DDRCH2_VREF_DQ_OUT_TAP0	DDRCH2_VREF_DQ_OUT_TAP1	DDRCH2_VREF_DQ_OUT_EN	RESERVED

Bits	Field Name	Description	Type	Reset
31	DDRCH1_VREF_DQ_OUT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
30	DDRCH1_VREF_DQ_OUT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
29	DDRCH1_VREF_DQ_OUT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
28	DDRCH1_VREF_DQ_OUT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
27	DDRCH1_VREF_DQ_OUT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
26	DDRCH2_VREF_DQ0_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
25	DDRCH2_VREF_DQ0_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
24	DDRCH2_VREF_DQ0_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
23	DDRCH2_VREF_DQ0_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
22	DDRCH2_VREF_DQ0_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
21	DDRCH2_VREF_DQ1_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
20	DDRCH2_VREF_DQ1_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
19	DDRCH2_VREF_DQ1_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
18	DDRCH2_VREF_DQ1_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
17	DDRCH2_VREF_DQ1_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
16	DDRCH2_VREF_DQ2_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
15	DDRCH2_VREF_DQ2_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
14	DDRCH2_VREF_DQ2_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
13	DDRCH2_VREF_DQ2_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
12	DDRCH2_VREF_DQ2_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
11	DDRCH2_VREF_DQ3_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
10	DDRCH2_VREF_DQ3_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
9	DDRCH2_VREF_DQ3_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
8	DDRCH2_VREF_DQ3_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
7	DDRCH2_VREF_DQ3_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
6	DDRCH2_VREF_DQ_OUT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
5	DDRCH2_VREF_DQ_OUT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
4	DDRCH2_VREF_DQ_OUT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
3	DDRCH2_VREF_DQ_OUT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
2	DDRCH2_VREF_DQ_OUT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
1:0	RESERVED		R	0x0

Table 18-759. Register Call Summary for Register CONTROL_DDRIO_1

Control Module Functional Description
- Reference Voltage for Device LPDDR2/DDR3 I/O Buffers and LPDDR2/DDR3 Memory: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [33]

Table 18-760. CONTROL_DDRIO_2

Address Offset	0x0000 0658		
Physical Address	0x4A00 2E58 0x4A00 2E58	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDR CONTROL 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPDDR2CH1_VREF_CA_INT_CCAP0	LPDDR2CH1_VREF_CA_INT_CCAP1	LPDDR2CH1_VREF_CA_INT_TAP0	LPDDR2CH1_VREF_CA_INT_TAP1	LPDDR2CH1_VREF_CA_INT_EN	LPDDR2CH1_VREF_CA_OUT_CCAP0	LPDDR2CH1_VREF_CA_OUT_CCAP1	LPDDR2CH1_VREF_CA_OUT_TAP0	LPDDR2CH1_VREF_CA_OUT_TAP1	LPDDR2CH1_VREF_CA_OUT_EN	LPDDR2CH2_VREF_CA_INT_CCAP0	LPDDR2CH2_VREF_CA_INT_CCAP1	LPDDR2CH2_VREF_CA_INT_TAP0	LPDDR2CH2_VREF_CA_INT_TAP1	LPDDR2CH2_VREF_CA_INT_EN	LPDDR2CH2_VREF_CA_OUT_CCAP0	LPDDR2CH2_VREF_CA_OUT_CCAP1	LPDDR2CH2_VREF_CA_OUT_TAP0	LPDDR2CH2_VREF_CA_OUT_TAP1	LPDDR2CH2_VREF_CA_OUT_EN	RESERVED									

Bits	Field Name	Description	Type	Reset
31	LPDDR2CH1_VREF_CA_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
30	LPDDR2CH1_VREF_CA_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
29	LPDDR2CH1_VREF_CA_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
28	LPDDR2CH1_VREF_CA_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
27	LPDDR2CH1_VREF_CA_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
26	LPDDR2CH1_VREF_CA_OUT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
25	LPDDR2CH1_VREF_CA_OUT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
24	LPDDR2CH1_VREF_CA_OUT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
23	LPDDR2CH1_VREF_CA_OUT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
22	LPDDR2CH1_VREF_CA_OUT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
21	LPDDR2CH2_VREF_CA_INT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
20	LPDDR2CH2_VREF_CA_INT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
19	LPDDR2CH2_VREF_CA_INT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
18	LPDDR2CH2_VREF_CA_INT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
17	LPDDR2CH2_VREF_CA_INT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
16	LPDDR2CH2_VREF_CA_OUT_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
15	LPDDR2CH2_VREF_CA_OUT_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
14	LPDDR2CH2_VREF_CA_OUT_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
13	LPDDR2CH2_VREF_CA_OUT_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
12	LPDDR2CH2_VREF_CA_OUT_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
11:0	RESERVED		R	0x000

Table 18-761. Register Call Summary for Register CONTROL_DDRIO_2

Control Module Functional Description

- Reference Voltage for Device LPDDR2/DDR3 I/O Buffers and LPDDR2/DDR3 Memory: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

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- CTRL_MODULE_CORE_PAD Register Summary: [15]

Table 18-762. CONTROL_HYST_1

Address Offset	0x0000 065C		
Physical Address	0x4A00 2E5C 0x4A00 2E5C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	HYSTERESIS CONTROL 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDCARD_HYST	SDCARD_IC	RESERVED																													

Bits	Field Name	Description	Type	Reset
31	SDCARD_HYST	hysteresis control for sdcard 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
30:29	SDCARD_IC	The ic control for sdcard. Not applicable when the pad muxing selects SDCARD. When SDCARD is selected by the pad muxing, IO PAD drive strength is controlled by the MMCHS IP. In 3V signaling mode: 0x0: Reserved 0x1: 33 Ohms Drive Strength (HS mode, 50MHz, 40pF) 0x2: 66 Ohms Drive Strength (DS mode, 25MHz, 40pF) 0x3: Reserved In 1.8V signaling mode: 0x0: 44 Ohms Drive Strength (UHS - Type B, 15pF) 0x1: 33 Ohms Drive Strength (UHS - Type A, 21pF) 0x2: 58 Ohms Drive Strength (UHS - Type C, 11pF) 0x3: 100 Ohms Drive Strength (UHS - Type D)	RW	0x0
28:0	RESERVED		R	0x0000 0000

Table 18-763. Register Call Summary for Register CONTROL_HYST_1

Control Module Functional Description
- Extended-Drain I/O and PBIAS Cell: [0] [1]
- Extended-Drain I/O: [2] [3] [4]

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [5]

Table 18-764. CONTROL_CORE_CONTROL_SPARE_RW

Address Offset	0x0000 0668		
Physical Address	0x4A00 2E68 0x4A00 2E68	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	CORE control spare RW Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_RW																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_RW	Core control spare register bits RW	RW	0x0000 0000

Table 18-765. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_RW

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [0]

Table 18-766. CONTROL_CORE_CONTROL_SPARE_R

Address Offset	0x0000 066C		
Physical Address	0x4A00 2E6C 0x4A00 2E6C	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	CORE control spare R Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_R																															

Bits	Field Name	Description	Type	Reset
31:0	CORE_CONTROL_SPARE_R	Core control spare register bits R	R	0x0000 0000

Table 18-767. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_R

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [0]

Table 18-768. CONTROL_CORE_CONTROL_SPARE_R_C0

Address Offset	0x0000 0670		
Physical Address	0x4A00 2E70 0x4A00 2E70	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	CORE control spare RC Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_CONTROL_SPARE_R_C0	CORE_CONTROL_SPARE_R_C1	CORE_CONTROL_SPARE_R_C2	CORE_CONTROL_SPARE_R_C3	CORE_CONTROL_SPARE_R_C4	CORE_CONTROL_SPARE_R_C5	CORE_CONTROL_SPARE_R_C6	CORE_CONTROL_SPARE_R_C7	RESERVED																							

Bits	Field Name	Description	Type	Reset
31	CORE_CONTROL_SPARE_R_C0	Core control spare register bits RC	RW W1toClr	0
30	CORE_CONTROL_SPARE_R_C1	Core control spare register bits RC	RW W1toClr	0
29	CORE_CONTROL_SPARE_R_C2	Core control spare register bits RC	RW W1toClr	0
28	CORE_CONTROL_SPARE_R_C3	Core control spare register bits RC	RW W1toClr	0
27	CORE_CONTROL_SPARE_R_C4	Core control spare register bits RC	RW W1toClr	0
26	CORE_CONTROL_SPARE_R_C5	Core control spare register bits RC	RW W1toClr	0
25	CORE_CONTROL_SPARE_R_C6	Core control spare register bits RC	RW W1toClr	0
24	CORE_CONTROL_SPARE_R_C7	Core control spare register bits RC	RW W1toClr	0
23:0	RESERVED		R	0x00 0000

Table 18-769. Register Call Summary for Register CONTROL_CORE_CONTROL_SPARE_R_C0

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [0]

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Table 18-770. CONTROL_DDRIO_EXT_0

Address Offset	0x0000 0688		
Physical Address	0x4A00 2E88 0x4A00 2E88	**Instance**	CTRL_MODULE_CORE CTRL_MODULE_CORE_PAD
Description	DDR CONTROL EXT 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDR3CH1_VREF_CA1_CCAP0	DDR3CH1_VREF_CA1_CCAP1	DDR3CH1_VREF_CA1_TAP0	DDR3CH1_VREF_CA1_TAP1	DDR3CH1_VREF_CA1_EN	RESERVED	DDR3CH2_VREF_CA1_CCAP0	DDR3CH2_VREF_CA1_CCAP1	DDR3CH2_VREF_CA1_TAP0	DDR3CH2_VREF_CA1_TAP1	DDR3CH2_VREF_CA1_EN	RESERVED																				

Bits	Field Name	Description	Type	Reset
31	DDR3CH1_VREF_CA1_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
30	DDR3CH1_VREF_CA1_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
29	DDR3CH1_VREF_CA1_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
28	DDR3CH1_VREF_CA1_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1
27	DDR3CH1_VREF_CA1_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
26	RESERVED		R	0
25	DDR3CH2_VREF_CA1_CCAP0	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	1
24	DDR3CH2_VREF_CA1_CCAP1	Selection for coupling cap connection 0x0: Disabled 0x1: Enabled	RW	0
23	DDR3CH2_VREF_CA1_TAP0	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	0
22	DDR3CH2_VREF_CA1_TAP1	Selection for internal reference voltage drive 0x0: Disabled 0x1: Enabled	RW	1

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Bits	Field Name	Description	Type	Reset
21	DDR3CH2_VREF_CA1_EN	Enable 0x0: Disabled 0x1: Enabled	RW	1
20:0	RESERVED		R	0x00 0000

Table 18-771. Register Call Summary for Register CONTROL_DDRIO_EXT_0

Control Module Register Manual
- CTRL_MODULE_CORE_PAD Register Summary: [0]

18.6.4 CTRL_MODULE_WKUP Registers

18.6.4.1 CTRL_MODULE_WKUP Register Summary

Table 18-772. CTRL_MODULE_WKUP Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_WKUP Base Address
CONTROL_WKUP_REVISION	R	32	0x0000 0000	0x4AE0 C000
CONTROL_WKUP_HWINFO	R	32	0x0000 0004	0x4AE0 C004
CONTROL_WKUP_SYSCONFIG	RW	32	0x0000 0010	0x4AE0 C010
CONTROL_WKUP_PROT_CTRL	RW	32	0x0000 0100	0x4AE0 C100
RESERVED	R	32	0x0000 0104	0x4AE0 C104
RESERVED	R	32	0x0000 0108	0x4AE0 C108
CONTROL_WKUP_OCPREG_SPARE	RW	32	0x0000 010C	0x4AE0 C10C
CONTROL_PROT_EMIF1_SDRAM_CONFIG	RW	32	0x0000 0110	0x4AE0 C110
CONTROL_PROT_EMIF1_LPDDR2_NVM_CONFIG	RW	32	0x0000 0114	0x4AE0 C114
CONTROL_PROT_EMIF2_SDRAM_CONFIG	RW	32	0x0000 0118	0x4AE0 C118
CONTROL_PROT_EMIF2_LPDDR2_NVM_CONFIG2	RW	32	0x0000 011C	0x4AE0 C11C
CONTROL_STD_FUSE_USB_CONF	R	32	0x0000 0138	0x4AE0 C138
CONTROL_STD_FUSE_CONF	R	32	0x0000 013C	0x4AE0 C13C
RESERVED	W	32	0x0000 0140	0x4AE0 C140
CONTROL_EMIF1_SDRAM_CONFIG_EXT	RW	32	0x0000 0144	0x4AE0 C144
CONTROL_EMIF2_SDRAM_CONFIG_EXT	RW	32	0x0000 0148	0x4AE0 C148
CONTROL_EMIF1_SDRAM_CONFIG_EXT_1	R	32	0x0000 014C	0x4AE0 C14C
CONTROL_EMIF2_SDRAM_CONFIG_EXT_2	R	32	0x0000 0150	0x4AE0 C150
CONTROL_WKUP_STD_FUSE_DIE_ID_0	R	32	0x0000 0200	0x4AE0 C200

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Table 18-772. CTRL_MODULE_WKUP Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_WKUP Base Address
CONTROL_WKUP_ID_CODE	R	32	0x0000 0204	0x4AE0 C204
CONTROL_WKUP_STD_FUSE_DIE_ID_1	R	32	0x0000 0208	0x4AE0 C208
CONTROL_WKUP_STD_FUSE_DIE_ID_2	R	32	0x0000 020C	0x4AE0 C20C
CONTROL_WKUP_STD_FUSE_DIE_ID_3	R	32	0x0000 0210	0x4AE0 C210
CONTROL_WKUP_STD_FUSE_PROD_ID_0	R	32	0x0000 0214	0x4AE0 C214
CONTROL_WKUP_LDOVBB_MM_VOLTAGE_CTRL	RW	32	0x0000 0314	0x4AE0 C314
CONTROL_WKUP_LDOVBB_MPU_VOLTAGE_CTRL	RW	32	0x0000 0318	0x4AE0 C318
CONTROL_WKUP_LDOSRAM_MM_VOLTAGE_CTRL	RW	32	0x0000 031C	0x4AE0 C31C
CONTROL_WKUP_LDOSRAM_MPU_VOLTAGE_CTRL	RW	32	0x0000 0324	0x4AE0 C324
CONTROL_WKUP_LDOSRAM_CORE_VOLTAGE_CTRL	RW	32	0x0000 0328	0x4AE0 C328
CONTROL_WKUP_LDOSRAM_MPU_LVT_VOLTAGE_CTRL	RW	32	0x0000 0338	0x4AE0 C338
CONTROL_WKUP_CONF_DEBUG_SEL_TST_0	RW	32	0x0000 0460	0x4AE0 C460
CONTROL_WKUP_CONF_DEBUG_SEL_TST_1	RW	32	0x0000 0464	0x4AE0 C464
CONTROL_WKUP_CONF_DEBUG_SEL_TST_2	RW	32	0x0000 0468	0x4AE0 C468
CONTROL_WKUP_CONF_DEBUG_SEL_TST_3	RW	32	0x0000 046C	0x4AE0 C46C
CONTROL_WKUP_CONF_DEBUG_SEL_TST_4	RW	32	0x0000 0470	0x4AE0 C470
CONTROL_WKUP_CONF_DEBUG_SEL_TST_5	RW	32	0x0000 0474	0x4AE0 C474
CONTROL_WKUP_CONF_DEBUG_SEL_TST_6	RW	32	0x0000 0478	0x4AE0 C478
CONTROL_WKUP_CONF_DEBUG_SEL_TST_7	RW	32	0x0000 047C	0x4AE0 C47C
CONTROL_WKUP_CONF_DEBUG_SEL_TST_8	RW	32	0x0000 0480	0x4AE0 C480
CONTROL_WKUP_CONF_DEBUG_SEL_TST_9	RW	32	0x0000 0484	0x4AE0 C484

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Table 18-772. CTRL_MODULE_WKUP Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_WKUP Base Address
CONTROL_WKUP_CONF_DEBUG_SEL_TST_10	RW	32	0x0000 0488	0x4AE0 C488
CONTROL_WKUP_CONF_DEBUG_SEL_TST_11	RW	32	0x0000 048C	0x4AE0 C48C
CONTROL_WKUP_CONF_DEBUG_SEL_TST_12	RW	32	0x0000 0490	0x4AE0 C490
CONTROL_WKUP_CONF_DEBUG_SEL_TST_13	RW	32	0x0000 0494	0x4AE0 C494
CONTROL_WKUP_CONF_DEBUG_SEL_TST_14	RW	32	0x0000 0498	0x4AE0 C498
CONTROL_WKUP_CONF_DEBUG_SEL_TST_15	RW	32	0x0000 049C	0x4AE0 C49C
CONTROL_WKUP_CONF_DEBUG_SEL_TST_16	RW	32	0x0000 04A0	0x4AE0 C4A0
CONTROL_WKUP_CONF_DEBUG_SEL_TST_17	RW	32	0x0000 04A4	0x4AE0 C4A4
CONTROL_WKUP_CONF_DEBUG_SEL_TST_18	RW	32	0x0000 04A8	0x4AE0 C4A8
CONTROL_WKUP_CONF_DEBUG_SEL_TST_19	RW	32	0x0000 04AC	0x4AE0 C4AC
CONTROL_WKUP_CONF_DEBUG_SEL_TST_20	RW	32	0x0000 04B0	0x4AE0 C4B0
CONTROL_WKUP_CONF_DEBUG_SEL_TST_21	RW	32	0x0000 04B4	0x4AE0 C4B4
CONTROL_WKUP_CONF_DEBUG_SEL_TST_22	RW	32	0x0000 04B8	0x4AE0 C4B8
CONTROL_WKUP_CONF_DEBUG_SEL_TST_23	RW	32	0x0000 04BC	0x4AE0 C4BC
CONTROL_WKUP_CONF_DEBUG_SEL_TST_24	RW	32	0x0000 04C0	0x4AE0 C4C0
CONTROL_WKUP_CONF_DEBUG_SEL_TST_25	RW	32	0x0000 04C4	0x4AE0 C4C4
CONTROL_WKUP_CONF_DEBUG_SEL_TST_26	RW	32	0x0000 04C8	0x4AE0 C4C8
CONTROL_WKUP_CONF_DEBUG_SEL_TST_27	RW	32	0x0000 04CC	0x4AE0 C4CC
CONTROL_WKUP_CONF_DEBUG_SEL_TST_28	RW	32	0x0000 04D0	0x4AE0 C4D0

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Table 18-772. CTRL_MODULE_WKUP Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_WKUP Base Address
CONTROL_WKUP_CONF_DEBUG_SEL_TST_29	RW	32	0x0000 04D4	0x4AE0 C4D4
CONTROL_WKUP_CONF_DEBUG_SEL_TST_30	RW	32	0x0000 04D8	0x4AE0 C4D8
CONTROL_WKUP_CONF_DEBUG_SEL_TST_31	RW	32	0x0000 04DC	0x4AE0 C4DC
CONTROL_WKUP_CONF_XBAR_SEL_0	RW	32	0x0000 05DC	0x4AE0 C5DC
CONTROL_WKUP_CONF_XBAR_SEL_4	RW	32	0x0000 05E0	0x4AE0 C5E0
CONTROL_WKUP_CONF_XBAR_SEL_8	RW	32	0x0000 05E4	0x4AE0 C5E4
CONTROL_WKUP_CONF_XBAR_SEL_12	RW	32	0x0000 05E8	0x4AE0 C5E8
CONTROL_WKUP_CONF_XBAR_SEL_16	RW	32	0x0000 05EC	0x4AE0 C5EC
CONTROL_WKUP_CONF_XBAR_SEL_20	RW	32	0x0000 05F0	0x4AE0 C5F0
CONTROL_WKUP_CONF_XBAR_SEL_24	RW	32	0x0000 05F4	0x4AE0 C5F4
CONTROL_WKUP_CONF_XBAR_SEL_28	RW	32	0x0000 05F8	0x4AE0 C5F8
CONTROL_WKUP_CONF_XBAR_BYPASS	RW	32	0x0000 05FC	0x4AE0 C5FC

18.6.4.2 CTRL_MODULE_WKUP Register Description

Table 18-773. CONTROL_WKUP_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4AE0 C000	**Instance**	CTRL_MODULE_WKUP
Description	Control module revision identifier Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISON																															

Bits	Field Name	Description	Type	Reset
31:0	REVISON	IP Revision	R	TI Internal data

Table 18-774. Register Call Summary for Register CONTROL_WKUP_REVISION

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- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-775. CONTROL_WKUP_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4AE0 C004	**Instance**	CTRL_MODULE_WKUP
Description	Information about the IP module hardware configuration i.e. typically the module HDL generics (if any). Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	IP_HWINFO	IP-module dependent	R	0x0000 0000

Table 18-776. Register Call Summary for Register CONTROL_WKUP_HWINFO

Control Module Register Manual
- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-777. CONTROL_WKUP_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4AE0 C010	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IP_SYSCONFIG_IDLEMODE		RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:2	IP_SYSCONFIG_IDLEMODE	RESERVED (not used).	RW	0x2
1:0	RESERVED		R	0x0

Table 18-778. Register Call Summary for Register CONTROL_WKUP_SYSCONFIG

Control Module Register Manual
- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-779. CONTROL_WKUP_PROT_CTRL

Address Offset	0x0000 0100		
Physical Address	0x4AE0 C100	**Instance**	CTRL_MODULE_WKUP
Description	Control Register. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRLWRDISABLE	RESERVED															MODEMDISABLE	RESERVED									OBSERVABILITYDISABLE	EMIF_CONFIG_RO_EN	RESERVED			

Table 18-780. Register Call Summary for Register CONTROL_WKUP_PROT_CTRL

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Bits	Field Name	Description	Type	Reset
31	CTRLWRDISABLE	Control Register write disable control. 0x0: Write in the Control Register is allowed 0x1: Write in the Control Register is forbidden	RW Woco	0
30:16	RESERVED		R	0x0
15	MODEMDISABLE	Modem enable/disable. When modem functionality has been disabled it is not possible to enable it again without a power-on-reset. 0x0: Modem is enabled 0x1: Modem is disabled (forced under reset)	RW Woco	0
14:6	RESERVED		R	0x00E
5	OBSERVABILITYDISABLE	Control the Observability feature 0x0: Observability is enabled. 0x1: Observability is disabled. If pads are configured for the hardware debug, outputs are tied to low	RW Woco	0
4	EMIF_CONFIG_RO_EN	Access mode for registers: CONTROL_PROT_EMIF1_SDRAM_CONFIG, CONTROL_PROT_EMIF2_SDRAM_CONFIG, CONTROL_PROT_EMIF1_LPDDR2_NVM_CONFIG, CONTROL_PROT_EMIF2_LPDDR2_NVM_CONFIG2 0x0: These registers are R/W 0x1: These registers are RO	RW Woco	0
3:0	RESERVED		R	0x0

Table 18-781. CONTROL_WKUP_OCPREG_SPARE

Address Offset	0x0000 010C		
Physical Address	0x4AE0 C10C	**Instance**	CTRL_MODULE_WKUP
Description	OCP Spare Register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCPREG_SPARE31	OCPREG_SPARE30	OCPREG_SPARE29	OCPREG_SPARE28	OCPREG_SPARE27	OCPREG_SPARE26	OCPREG_SPARE25	OCPREG_SPARE24	OCPREG_SPARE23	OCPREG_SPARE22	OCPREG_SPARE21	OCPREG_SPARE20	OCPREG_SPARE19	OCPREG_SPARE18	OCPREG_SPARE17	OCPREG_SPARE16	OCPREG_SPARE15	OCPREG_SPARE14	OCPREG_SPARE13	OCPREG_SPARE12	OCPREG_SPARE11	OCPREG_SPARE10	OCPREG_SPARE9	OCPREG_SPARE8	OCPREG_SPARE7	OCPREG_SPARE6	OCPREG_SPARE5	OCPREG_SPARE4	OCPREG_SPARE3	OCPREG_SPARE2	OCPREG_SPARE1	RESERVED

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Bits	Field Name	Description	Type	Reset
31	OCPREG_SPARE31	OCP spare register 31	RW	0
30	OCPREG_SPARE30	OCP spare register 30	RW	0
29	OCPREG_SPARE29	OCP spare register 29	RW	0
28	OCPREG_SPARE28	OCP spare register 28	RW	0
27	OCPREG_SPARE27	OCP spare register 27	RW	0
26	OCPREG_SPARE26	OCP spare register 26	RW	0
25	OCPREG_SPARE25	OCP spare register 25	RW	0
24	OCPREG_SPARE24	OCP spare register 24	RW	0
23	OCPREG_SPARE23	OCP spare register 23	RW	0
22	OCPREG_SPARE22	OCP spare register 22	RW	0
21	OCPREG_SPARE21	OCP spare register 21	RW	0
20	OCPREG_SPARE20	OCP spare register 20	RW	0
19	OCPREG_SPARE19	OCP spare register 19	RW	0
18	OCPREG_SPARE18	OCP spare register 18	RW	0
17	OCPREG_SPARE17	OCP spare register 17	RW	0
16	OCPREG_SPARE16	OCP spare register 16	RW	0
15	OCPREG_SPARE15	OCP spare register 15	RW	0
14	OCPREG_SPARE14	OCP spare register 14	RW	0
13	OCPREG_SPARE13	OCP spare register 13	RW	0
12	OCPREG_SPARE12	OCP spare register 12	RW	0
11	OCPREG_SPARE11	OCP spare register 11	RW	0
10	OCPREG_SPARE10	OCP spare register 10	RW	0
9	OCPREG_SPARE9	OCP spare register 9	RW	0
8	OCPREG_SPARE8	OCP spare register 8	RW	0
7	OCPREG_SPARE7	OCP spare register 7	RW	0
6	OCPREG_SPARE6	OCP spare register 6	RW	0
5	OCPREG_SPARE5	OCP spare register 5	RW	0
4	OCPREG_SPARE4	OCP spare register 4	RW	0
3	OCPREG_SPARE3	OCP spare register 3	RW	0
2	OCPREG_SPARE2	OCP spare register 2	RW	0
1	OCPREG_SPARE1	OCP spare register 1	RW	0
0	RESERVED		R	0

Table 18-782. Register Call Summary for Register CONTROL_WKUP_OCPREG_SPARE

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-783. CONTROL_PROT_EMIF1_SDRAM_CONFIG

Address Offset	0x0000 0110		
Physical Address	0x4AE0 C110	**Instance**	CTRL_MODULE_WKUP
Description	EMIF1 SDRAM configuration protection register. Values are exported to EMIF_SDRAM_CONFIG register at POR. For bit field descriptions see EMIF_SDRAM_CONFIG register in Section 15.3, *EMIF Controller*, in Chapter 15, *Memory Subsystem*.. Access conditions. Read: unrestricted, Write: If EMIF_CONFIG_RO_EN = 0 (default)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			EMIF1_SDRAM_IBANK_POS		EMIF1_SDRAM_DDR_TERM			EMIF1_SDRAM_DDR2_DDQS	EMIF1_SDRAM_DYN_ODT		EMIF1_SDRAM_DDR_DISABLE_DLL	EMIF1_SDRAM_DRIVE		EMIF1_SDRAM_CWL		RESERVED		EMIF1_SDRAM_CL			EMIF1_SDRAM_ROWSIZE			EMIF1_SDRAM_IBANK			EMIF1_SDRAM_EBANK	EMIF1_SDRAM_PAGESIZE		

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:27	EMIF1_SDRAM_IBANK_POS	Internal bank position.	RW	0x0
26:24	EMIF1_SDRAM_DDR_TERM	DDR3 termination resistor value.	RW	0x0
23	EMIF1_SDRAM_DDR2_DDQS	Not used.	RW	1
22:21	EMIF1_SDRAM_DYN_ODT	DDR3 Dynamic ODT.	RW	0x0
20	EMIF1_SDRAM_DDR_DISABLE_DLL	Disable DLL select.	RW	0
19:18	EMIF1_SDRAM_DRIVE	SDRAM drive strength.	RW	0x0
17:16	EMIF1_SDRAM_CWL	DDR3 CAS Write latency.	RW	0x1
15:14	RESERVED		R	0x0
13:10	EMIF1_SDRAM_CL	CAS Latency.	RW	0x3
9:7	EMIF1_SDRAM_ROWSIZE	Row Size.	RW	0x0
6:4	EMIF1_SDRAM_IBANK	Internal Bank setup.	RW	0x3
3	EMIF1_SDRAM_EBANK	External chip select setup.	RW	0
2:0	EMIF1_SDRAM_PAGESIZE	Page Size.	RW	0x1

Table 18-784. Register Call Summary for Register CONTROL_PROT_EMIF1_SDRAM_CONFIG

Control Module Functional Description

- Protection SDRAM Configuration Registers: [0]

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [1]
- CTRL_MODULE_WKUP Register Description: [3]

Table 18-785. CONTROL_PROT_EMIF1_LPDDR2_NVM_CONFIG

Address Offset	0x0000 0114		
Physical Address	0x4AE0 C114	**Instance**	CTRL_MODULE_WKUP
Description	EMIF1 configuration protection register. Values are exported to EMIF_SDRAM_CONFIG_2 register at POR. For bit field descriptions see EMIF_SDRAM_CONFIG_2 register in Section 15.3, *EMIF Controller*, in Chapter 15, *Memory Subsystem*. Access conditions. Read: unrestricted, Write: If EMIF_CONFIG_RO_EN = 0 (default)		
Type	RW		

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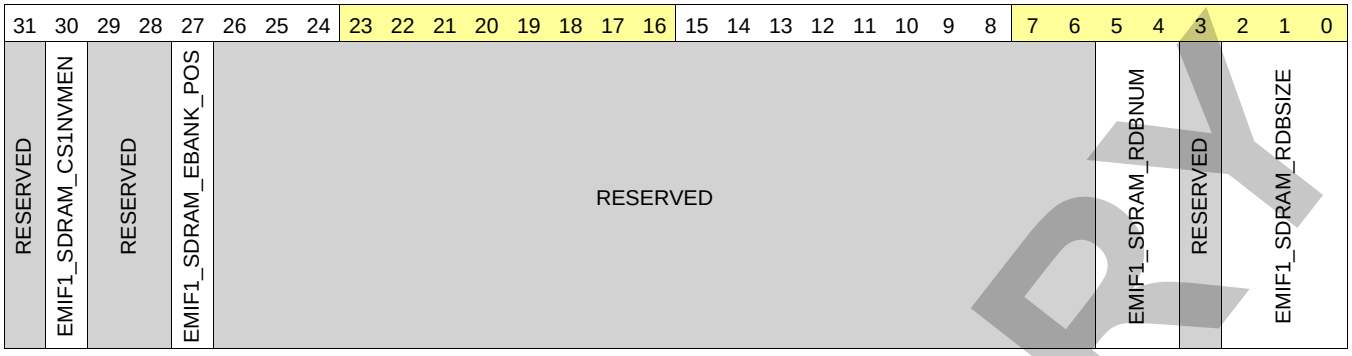

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30	EMIF1_SDRAM_CS1NVMEN	CS1 LPDDR2-NVM enable.	RW	0
29:28	RESERVED		R	0x0
27	EMIF1_SDRAM_EBANK_POS	External bank position. Set to 0 to assign external bank address bits from OCP address. Set to 1 to assign external bank address bits to the most significant bit of the OCP address. This field is not implemented in the design and is resertved fiel for the future use.	R	0
26:6	RESERVED		R	0x00 0000
5:4	EMIF1_SDRAM_RDBNUM	Row Buffer setup.	RW	0x1
3	RESERVED		R	0
2:0	EMIF1_SDRAM_RDBSIZE	Row Data Buffer Size.	RW	0x0

Table 18-786. Register Call Summary for Register CONTROL_PROT_EMIF1_LPDDR2_NVM_CONFIG

Control Module Functional Description
- Protection SDRAM Configuration Registers: [0]

Control Module Register Manual
- CTRL_MODULE_WKUP Register Summary: [1]
- CTRL_MODULE_WKUP Register Description: [3]

Table 18-787. CONTROL_PROT_EMIF2_SDRAM_CONFIG

Address Offset	0x0000 0118		
Physical Address	0x4AE0 C118	**Instance**	CTRL_MODULE_WKUP
Description	EMIF2 SDRAM configuration protection register. Values are exported to EMIF_SDRAM_CONFIG register at POR. For bit field descriptions see EMIF_SDRAM_CONFIG register in Section 15.3, *EMIF Controller*, in Chapter 15, *Memory Subsystem*. Access conditions. Read: unrestricted, Write: EMIF_CONFIG_RO_EN = 0 (default)		
Type	RW		

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31 30 29	28 27	26 25 24	23 22 21	20	19 18	17 16	15 14	13 12 11 10	9 8	7 6 5 4	3	2 1 0
RESERVED	EMIF2_SDRAM_IBANK_POS	EMIF2_SDRAM_DDR_TERM	EMIF2_SDRAM_DDR2_DDQS	EMIF2_SDRAM_DYN_ODT	EMIF2_SDRAM_DDR_DISABLE_DLL	EMIF2_SDRAM_DRIVE	EMIF2_SDRAM_CWL	RESERVED	EMIF2_SDRAM_CL	EMIF2_SDRAM_ROWSIZE	EMIF2_SDRAM_IBANK	EMIF2_SDRAM_EBANK	EMIF2_SDRAM_PAGESIZE

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:27	EMIF2_SDRAM_IBANK_POS	Internal bank position.	RW	0x0
26:24	EMIF2_SDRAM_DDR_TERM	DDR3 termination resistor value.	RW	0x0
23	EMIF2_SDRAM_DDR2_DDQS	Not used.	RW	1
22:21	EMIF2_SDRAM_DYN_ODT	DDR3 Dynamic ODT.	RW	0x0
20	EMIF2_SDRAM_DDR_DISABLE_DLL	Disable DLL select.	RW	0
19:18	EMIF2_SDRAM_DRIVE	SDRAM drive strength.	RW	0x0
17:16	EMIF2_SDRAM_CWL	DDR3 CAS Write latency.	RW	0x1
15:14	RESERVED		R	0x0
13:10	EMIF2_SDRAM_CL	CAS Latency.	RW	0x3
9:7	EMIF2_SDRAM_ROWSIZE	Row Size.	RW	0x0
6:4	EMIF2_SDRAM_IBANK	Internal Bank setup.	RW	0x3
3	EMIF2_SDRAM_EBANK	External chip select setup.	RW	0
2:0	EMIF2_SDRAM_PAGESIZE	Page Size.	RW	0x1

Table 18-788. Register Call Summary for Register CONTROL_PROT_EMIF2_SDRAM_CONFIG

Control Module Functional Description
- Protection SDRAM Configuration Registers: [0]

Control Module Register Manual
- CTRL_MODULE_WKUP Register Summary: [1]
- CTRL_MODULE_WKUP Register Description: [3]

Table 18-789. CONTROL_PROT_EMIF2_LPDDR2_NVM_CONFIG2

Address Offset	0x0000 011C		
Physical Address	0x4AE0 C11C	**Instance**	CTRL_MODULE_WKUP
Description	EMIF2 configuration protection register. Values are exported to EMIF_SDRAM_CONFIG_2 register at POR. For bit field descriptions see EMIF_SDRAM_CONFIG_2 register in Section 15.3, *EMIF Controller*, in Chapter 15, *Memory Subsystem*. Access conditions. Read: unrestricted, Write: EMIF_CONFIG_RO_EN = 0 (default)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	EMIF2_SDRAM_CS1NVMEN	RESERVED		EMIF2_SDRAM_EBANK_POS	RESERVED																			EMIF2_SDRAM_RDBNUM			RESERVED	EMIF2_SDRAM_RDBSIZE				

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30	EMIF2_SDRAM_CS1NVMEN	CS1 LPDDR2-NVM enable.	RW	0
29:28	RESERVED		R	0x0
27	EMIF2_SDRAM_EBANK_POS	External bank position. Set to 0 to assign external bank address bits from OCP address. Set to 1 to assign external bank address bits to the most significant bit of the OCP address. This field is not implemented in the design and is resertved fiel for the future use.	R	0
26:6	RESERVED		R	0x00 0000
5:4	EMIF2_SDRAM_RDBNUM	Row Buffer setup.	RW	0x1
3	RESERVED		R	0
2:0	EMIF2_SDRAM_RDBSIZE	Row Data Buffer Size.	RW	0x0

Table 18-790. Register Call Summary for Register CONTROL_PROT_EMIF2_LPDDR2_NVM_CONFIG2

Control Module Functional Description
- Protection SDRAM Configuration Registers: [0]

Control Module Register Manual
- CTRL_MODULE_WKUP Register Summary: [1]
- CTRL_MODULE_WKUP Register Description: [3]

Table 18-791. CONTROL_STD_FUSE_USB_CONF

Address Offset	0x0000 0138		
Physical Address	0x4AE0 C138	**Instance**	CTRL_MODULE_WKUP
Description	Standard Fuse conf [31:0]. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USB_PROD_ID																USB_VENDOR_ID															

Bits	Field Name	Description	Type	Reset
31:16	USB_PROD_ID	USB Product Identification	R	0x0000
15:0	USB_VENDOR_ID	USB Vendor Identification	R	0x0000

Table 18-792. Register Call Summary for Register CONTROL_STD_FUSE_USB_CONF

Control Module Register Manual
- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-793. CONTROL_STD_FUSE_CONF

Address Offset	0x0000 013C		
Physical Address	0x4AE0 C13C	**Instance**	CTRL_MODULE_WKUP
Description	Standard Fuse conf [63:32]. Register shows part of the chip eFuse configuration. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read Only.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										STD_FUSE_EMIF2_INITREF_DEF_DIS	STD_FUSE_EMIF2_DDR3_LPDDR2N	STD_FUSE_EMIF1_INITREF_DEF_DIS	STD_FUSE_EMIF1_DDR3_LPDDR2N	RESERVED	STD_FUSE_HDCP_ENABLE	STD_TEXTURE_COMPRESSION_ENABLE	STD_FUSE_FACE_DETECT_DISABLE	RESERVED	STD_FUSE_CH_SPEEDUP_DISABLE	RESERVED		STD_FUSE_ISS_EFUSE1_EN	STD_FUSE_ISS_EFUSE2_EN	STD_FUSE_ISS_EFUSE3_EN	STD_FUSE_ISS_EFUSE4_EN	STD_FUSE_SGX540_3D_CLOCK_SOURCE	STD_FUSE_SGX540_3D_DISABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x-
21	STD_FUSE_EMIF2_INITREF_DEF_DIS	EMIF2 disable EMIF DDR refresh and init sequence Read 0x1: refresh and init sequence are disabled Read 0x0: refresh and init sequence are enabled	R	0x-
20	STD_FUSE_EMIF2_DDR3_LPDDR2N	EMIF2 DDR3 or LPDDR2 Read 0x1: DDR3 configured Read 0x0: LPDDR2 configured	R	0x-
19	STD_FUSE_EMIF1_INITREF_DEF_DIS	EMIF1 disable EMIF DDR refresh and init sequence Read 0x1: refresh and init sequence are disabled Read 0x0: refresh and init sequence are enabled	R	0x-
18	STD_FUSE_EMIF1_DDR3_LPDDR2N	EMIF1 DDR3 or LPDDR2 Read 0x1: DDR3 configured Read 0x0: LPDDR2 configured	R	0x-
17	RESERVED	Reserved	R	0x-
16	STD_FUSE_HDCP_ENABLE	Enable HDCP Read 0x1: HDCP is disabled Read 0x0: HDCP is enabled	R	0x-
15	STD_TEXTURE_COMPRESSION_ENABLE	Disable texture compression(note: this bit is inverted compared to its eFuse) Read 0x1: texture compression is enabled Read 0x0: texture compression is disabled	R	0x-
14	STD_FUSE_FACE_DETECT_DISABLE	Disable face detect Read 0x1: face detect is disabled Read 0x0: face detect is enabled	R	0x-
13	RESERVED	Reserved	R	0x-

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Bits	Field Name	Description	Type	Reset
12	STD_FUSE_CH_SPEEDUP_DISABLE	ROM code settings for configuration header block. Only SW access. Read 0x1: CH is disabled Read 0x0: CH is enabled	R	0x-
11:9	RESERVED	Reserved	R	0x-
8	STD_FUSE_ISS_EFUSE1_EN	Enable implementation specific features. Read 0x1: specific features are enabled Read 0x0: specific features are disabled	R	0x-
7	STD_FUSE_ISS_EFUSE2_EN	Enable implementation specific features. Read 0x1: specific features are enabled Read 0x0: specific features are disabled	R	0x-
6	STD_FUSE_ISS_EFUSE3_EN	Enable implementation specific features. Read 0x1: specific features are enabled Read 0x0: specific features are disabled	R	0x-
5	STD_FUSE_ISS_EFUSE4_EN	Enable implementation specific features. Read 0x1: specific features are enabled Read 0x0: specific features are disabled	R	0x-
4	STD_FUSE_SGX540_3D_CLOCK_SOURCE	Functional clock selection for the 3D accelerator engine Read 0x0: GPU is fully enabled (DPLL_CORE/PER) Read 0x1: GPU is partially enabled (DPLL_PER/8 max)	R	0x-
3	STD_FUSE_SGX540_3D_DISABLE	Disable the 3D accelerator engine Read 0x1: SGX is disabled Read 0x0: SGX is enabled	R	0x-
2:0	RESERVED	Reserved	R	0x-

Table 18-794. Register Call Summary for Register CONTROL_STD_FUSE_CONF

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-795. CONTROL_EMIF1_SDRAM_CONFIG_EXT

Address Offset	0x0000 0144		
Physical Address	0x4AE0 C144	**Instance**	CTRL_MODULE_WKUP
Description	PHY register for EMIF1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EMIF1_REG_PHY_NUM_OF_SAMPLES		EMIF1_REG_PHY_SEL_LOGIC	EMIF1_REG_PHY_ALL_DQ_MPR_RD_RESP	EMIF1_REG_PHY_OUTPUT_STATUS_SELECT			RESERVED	EMIF1_SDRAM_DISABLE_RESET	EMIF1_PHY_RD_LOCAL_ODT		RESERVED	EMIF1_DFI_CLOCK_PHASE_CTRL	EMIF1_EN_SLICE_2	EMIF1_EN_SLICE_1	EMIF1_EN_SLICE_0	

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:14	EMIF1_REG_PHY_NUM_OF_SAMPLES	Controls the number of DQ samples required for read leveling. The recommended setting for full leveling is 0x3 (128 samples) and for incremental leveling is 0x0 (4 samples). 0x0: 4 samples. 0x1: 8 samples. 0x2: 16 samples. 0x3: 128 samples.	RW	0x2
13	EMIF1_REG_PHY_SEL_LOGIC	Selects an algorithm for read leveling. The use of algorithm 1 (set by default) is recommended. 0x0: Algorithm 1 is used. 0x1: Algorithm 2 is used.	RW	0
12	EMIF1_REG_PHY_ALL_DQ_MPR_RD_RESP	Analysis method of DQ bits during read leveling. 0x0: if the DRAM provides a read response on only one DQ bit. This is the default setting and works with all memory types (memories send responses on all DQ bits or on a single DQ bit). 0x1: if the DRAM provides a read response on all DQ bits.	RW	0
11:9	EMIF1_REG_PHY_OUTPUT_STATUS_SELECT	Selects the status to be observed on the outputs of the DDR PHYs through CONTROL_EMIF1_SDRAM_CONFIG_EXT_1 register. 0x0: selects phy_reg_rdlvl_start_ratio[7:0] 0x1: selects phy_reg_rdlvl_start_ratio[15:8] 0x2: selects phy_reg_rdlvl_end_ratio[7:0] 0x3: selects phy_reg_rdlvl_end_ratio[15:8]	RW	0x0
8	RESERVED	Reserved	R	1
7	EMIF1_SDRAM_DISABLE_RESET	ddr3ch1_nreset signal disable. Keep this bit set to 0x1 during normal operations and to 0x0 at boot time and when a memory reset is necessary. 0x0: ddr3ch1_nreset is enabled. It can be asserted by EMIF. 0x1: ddr3ch1_nreset is disabled. It is forbidden to EMIF to assert it.	RW	0

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Bits	Field Name	Description	Type	Reset
6:5	EMIF1_PHY_RD_LOCAL_ODT	Control of ODT (on – die termination) settings for the device DDR I/Os. ODT is enabled only during read operations when termination is required. 0x0: ODT disabled. 0x1: 60 Ohms. 0x2: 80 Ohms. 0x3: 120 Ohms.	RW	0x0
4	RESERVED	Reserved	R	0
3	EMIF1_DFI_CLOCK_PHASE_CTRL	EMIF_CORE1 clock phase control (shifting by 180°). For normal operation this bit must always be set to 0x0 (disabled).	RW	0
2	EMIF1_EN_SLICE_2	Enable command PHY 2. 0x1 is the mandatory setting if LPDDR2 is used. When using DDR3 this bit can be set to 0x0 or 0x1. For lower power consumption 0x0 is used.	RW	1
1	EMIF1_EN_SLICE_1	Enable command PHY 1. 0x1 is the mandatory setting if DDR3 is used. When using LPDDR2 this bit can be set to 0x0 or 0x1. For lower power consumption 0x0 is used. EMIF1_EN_SLICE_0 and EMIF1_EN_SLICE_1 have to be programmed with the same value.	RW	1
0	EMIF1_EN_SLICE_0	Enable command PHY 0. 0x1 is the mandatory setting if DDR3 is used. When using LPDDR2 this bit can be set to 0x0 or 0x1. For lower power consumption 0x0 is used. EMIF1_EN_SLICE_0 and EMIF1_EN_SLICE_1 have to be programmed with the same value.	RW	1

Table 18-796. Register Call Summary for Register CONTROL_EMIF1_SDRAM_CONFIG_EXT

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-797. CONTROL_EMIF2_SDRAM_CONFIG_EXT

Address Offset	0x0000 0148		
Physical Address	0x4AE0 C148	**Instance**	CTRL_MODULE_WKUP
Description	PHY register for EMIF2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EMIF2_REG_PHY_NUM_OF_SAMPLES		EMIF2_REG_PHY_SEL_LOGIC	EMIF2_REG_PHY_ALL_DQ_MPR_RD_RESP	EMIF2_REG_PHY_OUTPUT_STATUS_SELECT		RESERVED		EMIF2_SDRAM_DISABLE_RESET	EMIF2_PHY_RD_LOCAL_ODT		RESERVED	EMIF2_DFI_CLOCK_PHASE_CTRL	EMIF2_EN_SLICE_2	EMIF2_EN_SLICE_1	EMIF2_EN_SLICE_0

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:14	EMIF2_REG_PHY_NUM_OF_SAMPLES	Controls the number of DQ samples required for read leveling. The recommended setting for full leveling is 0x3 (128 samples) and for incremental leveling is 0x0 (4 samples). 0x0: 4 samples. 0x1: 8 samples. 0x2: 16 samples. 0x3: 128 samples.	RW	0x2
13	EMIF2_REG_PHY_SEL_LOGIC	Selects an algorithm for read leveling. The use of algorithm 1 (set by default) is recommended. 0x0: Algorithm 1 is used. 0x1: Algorithm 2 is used.	RW	0
12	EMIF2_REG_PHY_ALL_DQ_MPR_RD_RESP	Analysis method of DQ bits during read leveling. 0x0: if the DRAM provides a read response on only one DQ bit. This is the default setting and works with all memory types (memories send responses on all DQ bits or on a single DQ bit). 0x1: if the DRAM provides a read response on all DQ bits.	RW	0
11:9	EMIF2_REG_PHY_OUTPUT_STATUS_SELECT	Selects the status to be observed on the outputs of the DDR PHYs through CONTROL_EMIF2_SDRAM_CONFIG_EXT_2 register. 0x0: selects phy_reg_rdlvl_start_ratio[7:0] 0x1: selects phy_reg_rdlvl_start_ratio[15:8] 0x2: selects phy_reg_rdlvl_end_ratio[7:0] 0x3: selects phy_reg_rdlvl_end_ratio[15:8]	RW	0x0
8	RESERVED	Reserved	R	1
7	EMIF2_SDRAM_DISABLE_RESET	ddr3ch2_nreset signal disable. Keep this bit set to 0x1 during normal operations and to 0x0 at boot time and when a memory reset is necessary. 0x0: ddr3ch2_nreset is enabled. It can be asserted by EMIF. 0x1: ddr3ch2_nreset is disabled. It is forbidden to EMIF to assert it.	RW	0
6:5	EMIF2_PHY_RD_LOCAL_ODT	Control of ODT (on – die termination) settings for the device DDR I/Os. ODT is enabled only during read operations when termination is required. 0x0: ODT disabled. 0x1: 60 Ohms. 0x2: 80 Ohms. 0x3: 120 Ohms.	RW	0x0
4	RESERVED	Reserved	R	0
3	EMIF2_DFI_CLOCK_PHASE_CTRL	EMIF_CORE2 clock phase control (shifting by 180°). For normal operation this bit must always be set to 0x0 (disabled).	RW	0
2	EMIF2_EN_SLICE_2	Enable command PHY 2. 0x1 is the mandatory setting if LPDDR2 is used. When using DDR3 this bit can be set to 0x0 or 0x1. For lower power consumption 0x0 is used.	RW	1
1	EMIF2_EN_SLICE_1	Enable command PHY 1. 0x1 is the mandatory setting if DDR3 is used. When using LPDDR2 this bit can be set to 0x0 or 0x1. For lower power consumption 0x0 is used. EMIF2_EN_SLICE_0 and EMIF2_EN_SLICE_1 have to be programmed with the same value.	RW	1

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Bits	Field Name	Description	Type	Reset
0	EMIF2_EN_SLICE_0	Enable command PHY 0. 0x1 is the mandatory setting if DDR3 is used. When using LPDDR2 this bit can be set to 0x0 or 0x1. For lower power consumption 0x0 is used. EMIF2_EN_SLICE_0 and EMIF2_EN_SLICE_1 have to be programmed with the same value.	RW	1

Table 18-798. Register Call Summary for Register CONTROL_EMIF2_SDRAM_CONFIG_EXT

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-799. CONTROL_EMIF1_SDRAM_CONFIG_EXT_1

Address Offset	0x0000 014C		
Physical Address	0x4AE0 C14C	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMIF1_PHY_REG_READ_DATA_EYE_LVL																															

Bits	Field Name	Description	Type	Reset
31:0	EMIF1_PHY_REG_READ_DATA_EYE_LVL		R	0x0000 0000

Table 18-800. Register Call Summary for Register CONTROL_EMIF1_SDRAM_CONFIG_EXT_1

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]
- CTRL_MODULE_WKUP Register Description: [1]

Table 18-801. CONTROL_EMIF2_SDRAM_CONFIG_EXT_2

Address Offset	0x0000 0150		
Physical Address	0x4AE0 C150	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMIF2_PHY_REG_READ_DATA_EYE_LVL																															

Bits	Field Name	Description	Type	Reset
31:0	EMIF2_PHY_REG_READ_DATA_EYE_LVL		R	0x0000 0000

Table 18-802. Register Call Summary for Register CONTROL_EMIF2_SDRAM_CONFIG_EXT_2

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]
- CTRL_MODULE_WKUP Register Description: [1]

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Table 18-803. CONTROL_WKUP_STD_FUSE_DIE_ID_0

Address Offset	0x0000 0200
Physical Address	0x4AE0 C200 **Instance** CTRL_MODULE_WKUP
Description	Die ID Register - Part 0. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_DIE_ID_0																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_DIE_ID_0		R	0x0000 0000

Table 18-804. Register Call Summary for Register CONTROL_WKUP_STD_FUSE_DIE_ID_0

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-805. CONTROL_WKUP_ID_CODE

Address Offset	0x0000 0204
Physical Address	0x4AE0 C204 **Instance** CTRL_MODULE_WKUP
Description	ID_CODE Key Register Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_IDCODE																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_IDCODE		R	0x0000 0000

Table 18-806. Register Call Summary for Register CONTROL_WKUP_ID_CODE

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-807. CONTROL_WKUP_STD_FUSE_DIE_ID_1

Address Offset	0x0000 0208
Physical Address	0x4AE0 C208 **Instance** CTRL_MODULE_WKUP
Description	Die ID Register - Part 1. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_DIE_ID_1																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_DIE_ID_1		R	0x0000 0000

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Table 18-808. Register Call Summary for Register CONTROL_WKUP_STD_FUSE_DIE_ID_1

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-809. CONTROL_WKUP_STD_FUSE_DIE_ID_2

Address Offset	0x0000 020C		
Physical Address	0x4AE0 C20C	**Instance**	CTRL_MODULE_WKUP
Description	Die ID Register - Part 2. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_DIE_ID_2																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_DIE_ID_2		R	0x0000 0000

Table 18-810. Register Call Summary for Register CONTROL_WKUP_STD_FUSE_DIE_ID_2

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-811. CONTROL_WKUP_STD_FUSE_DIE_ID_3

Address Offset	0x0000 0210		
Physical Address	0x4AE0 C210	**Instance**	CTRL_MODULE_WKUP
Description	Die ID Register - Part 3. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_DIE_ID_3																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_DIE_ID_3		R	0x0000 0000

Table 18-812. Register Call Summary for Register CONTROL_WKUP_STD_FUSE_DIE_ID_3

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-813. CONTROL_WKUP_STD_FUSE_PROD_ID_0

Address Offset	0x0000 0214		
Physical Address	0x4AE0 C214	**Instance**	CTRL_MODULE_WKUP
Description	Prod ID Register - Part 0. Register shows part of the chip eFuse configuration on the OCP interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STD_FUSE_PROD_ID																															

Bits	Field Name	Description	Type	Reset
31:0	STD_FUSE_PROD_ID		R	0x0000 0000

Table 18-814. Register Call Summary for Register CONTROL_WKUP_STD_FUSE_PROD_ID_0

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-815. CONTROL_WKUP_LDOVBB_MM_VOLTAGE_CTRL

Address Offset	0x0000 0314		
Physical Address	0x4AE0 C314	**Instance**	CTRL_MODULE_WKUP
Description	MM Voltage Body Bias LDO Control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					LDOVBBMM_FBB_MUX_CTRL			LDOVBBMM_FBB_VSET_IN						LDOVBBMM_FBB_VSET_OUT					

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x00 0000
10	LDOVBBMM_FBB_MUX_CTRL	Override control of EFUSE Forward Body Bias voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOVBBMM_FBB_VSET_IN	EFUSE Forward Body Bias voltage value	R	0x00
4:0	LDOVBBMM_FBB_VSET_OUT	Override value for Forward Body Bias voltage	RW	0x00

Table 18-816. Register Call Summary for Register CONTROL_WKUP_LDOVBB_MM_VOLTAGE_CTRL

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-817. CONTROL_WKUP_LDOVBB_MPU_VOLTAGE_CTRL

Address Offset	0x0000 0318		
Physical Address	0x4AE0 C318	**Instance**	CTRL_MODULE_WKUP
Description	MPU Voltage Body Bias LDO Control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31:11	10	9:5	4:0
RESERVED	LDOVBBMPU_FBB_MUX_CTRL	LDOVBBMPU_FBB_VSET_IN	LDOVBBMPU_FBB_VSET_OUT

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x00 0000
10	LDOVBBMPU_FBB_MUX_CTRL	Override control of EFUSE Forward Body Bias voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOVBBMPU_FBB_VSET_IN	EFUSE Forward Body Bias voltage value	R	0x00
4:0	LDOVBBMPU_FBB_VSET_OUT	Override value for Forward Body Bias voltage	RW	0x00

Table 18-818. Register Call Summary for Register CONTROL_WKUP_LDOVBB_MPU_VOLTAGE_CTRL

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-819. CONTROL_WKUP_LDOSRAM_MM_VOLTAGE_CTRL

Address Offset	0x0000 031C		
Physical Address	0x4AE0 C31C	**Instance**	CTRL_MODULE_WKUP
Description	IVA SRAM LDO Control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31:26	25:24	23:19	18:16	15:10	9:5	4:0
RESERVED	LDOSRAMMM_RETMODE_MUX_CTRL	LDOSRAMMM_RETMODE_VSET_IN	LDOSRAMMM_RETMODE_VSET_OUT	RESERVED	LDOSRAMMM_ACTMODE_MUX_CTRL	LDOSRAMMM_ACTMODE_VSET_IN	LDOSRAMMM_ACTMODE_VSET_OUT

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Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	LDOSRAMMM_RETMODE_MUX_CTRL	Override control of EFUSE Retention Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
25:21	LDOSRAMMM_RETMODE_VSET_IN	EFUSE Retention Mode Voltage value (vset[9:5])	R	0x00
20:16	LDOSRAMMM_RETMODE_VSET_OUT	Override value for Retention Mode Voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOSRAMMM_ACTMODE_MUX_CTRL	Override control of EFUSE Active Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOSRAMMM_ACTMODE_VSET_IN	EFUSE Active Mode Voltage value (vset[4:0])	R	0x00
4:0	LDOSRAMMM_ACTMODE_VSET_OUT	Override value for Active Mode Voltage value	RW	0x00

Table 18-820. Register Call Summary for Register CONTROL_WKUP_LDOSRAM_MM_VOLTAGE_CTRL

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-821. CONTROL_WKUP_LDOSRAM_MPU_VOLTAGE_CTRL

Address Offset	0x0000 0324		
Physical Address	0x4AE0 C324	**Instance**	CTRL_MODULE_WKUP
Description	MPU SRAM LDO Control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					LDOSRAMMPU_RETMODE_MUX_CTRL	LDOSRAMMPU_RETMODE_VSET_IN								LDOSRAMMPU_RETMODE_VSET_OUT		RESERVED					LDOSRAMMPU_ACTMODE_MUX_CTRL	LDOSRAMMPU_ACTMODE_VSET_IN						LDOSRAMMPU_ACTMODE_VSET_OUT				

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	LDOSRAMMPU_RETMODE_MUX_CTRL	Override control of EFUSE Retention Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
25:21	LDOSRAMMPU_RETMODE_VSET_IN	EFUSE Retention Mode Voltage value (vset[9:5])	R	0x00

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Bits	Field Name	Description	Type	Reset
20:16	LDOSRAMMPU_RETMODE_VSET_OUT	Override value for Retention Mode Voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOSRAMMPU_ACTMODE_MUX_CTRL	Override control of EFUSE Active Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOSRAMMPU_ACTMODE_VSET_IN	EFUSE Active Mode Voltage value (vset[4:0])	R	0x00
4:0	LDOSRAMMPU_ACTMODE_VSET_OUT	Override value for Active Mode Voltage value	RW	0x00

Table 18-822. Register Call Summary for Register CONTROL_WKUP_LDOSRAM_MPU_VOLTAGE_CTRL

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-823. CONTROL_WKUP_LDOSRAM_CORE_VOLTAGE_CTRL

Address Offset	0x0000 0328		
Physical Address	0x4AE0 C328	**Instance**	CTRL_MODULE_WKUP
Description	Core SRAM LDO Control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					LDOSRAMCORE_RETMODE_MUX_CTRL	LDOSRAMCORE_RETMODE_VSET_IN					LDOSRAMCORE_RETMODE_VSET_OUT					RESERVED					LDOSRAMCORE_ACTMODE_MUX_CTRL	LDOSRAMCORE_ACTMODE_VSET_IN						LDOSRAMCORE_ACTMODE_VSET_OUT				

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	LDOSRAMCORE_RETMODE_MUX_CTRL	Override control of EFUSE Retention Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
25:21	LDOSRAMCORE_RETMODE_VSET_IN	EFUSE Retention Mode Voltage value (vset[9:5])	R	0x00
20:16	LDOSRAMCORE_RETMODE_VSET_OUT	Override value for Retention Mode Voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOSRAMCORE_ACTMODE_MUX_CTRL	Override control of EFUSE Active Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0

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Bits	Field Name	Description	Type	Reset
9:5	LDOSRAMCORE_ACTMODE_VSET_IN	EFUSE Active Mode Voltage value (vset[4:0])	R	0x00
4:0	LDOSRAMCORE_ACTMODE_VSET_OUT	Override value for Active Mode Voltage value	RW	0x00

Table 18-824. Register Call Summary for Register CONTROL_WKUP_LDOSRAM_CORE_VOLTAGE_CTRL

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-825. CONTROL_WKUP_LDOSRAM_MPU_LVT_VOLTAGE_CTRL

Address Offset	0x0000 0338		
Physical Address	0x4AE0 C338	**Instance**	CTRL_MODULE_WKUP
Description	MPU LVT SRAM LDO Control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30 29 28 27	26	25 24 23 22 21	20 19 18 17 16	15 14 13 12 11	10	9 8 7 6 5	4 3 2 1 0
RESERVED	LDOSRAMMPU_LVT_RETMODE_MUX_CTRL	LDOSRAMMPU_LVT_RETMODE_VSET_IN	LDOSRAMMPU_LVT_RETMODE_VSET_OUT	RESERVED	LDOSRAMMPU_LVT_ACTMODE_MUX_CTRL	LDOSRAMMPU_LVT_ACTMODE_VSET_IN	LDOSRAMMPU_LVT_ACTMODE_VSET_OUT

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	LDOSRAMMPU_LVT_RETMODE_MUX_CTRL	Override control of EFUSE Retention Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
25:21	LDOSRAMMPU_LVT_RETMODE_VSET_IN	EFUSE Retention Mode Voltage value (vset[9:5])	R	0x00
20:16	LDOSRAMMPU_LVT_RETMODE_VSET_OUT	Override value for Retention Mode Voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOSRAMMPU_LVT_ACTMODE_MUX_CTRL	Override control of EFUSE Active Mode Voltage value 0x0: efuse value is used 0x1: override value is used	RW	0
9:5	LDOSRAMMPU_LVT_ACTMODE_VSET_IN	EFUSE Active Mode Voltage value (vset[4:0])	R	0x00
4:0	LDOSRAMMPU_LVT_ACTMODE_VSET_OUT	Override value for Active Mode Voltage value	RW	0x00

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Table 18-826. Register Call Summary for Register CONTROL_WKUP_LDOSRAM_MPU_LVT_VOLTAGE_CTRL

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- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-827. CONTROL_WKUP_CONF_DEBUG_SEL_TST_0

Address Offset	0x0000 0460		
Physical Address	0x4AE0 C460	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_0 0x1: hwobs_int_cm1_0 0x3: hwobs_debug_abe_0 0x2: hwobs_abe_irq	RW	0x0

Table 18-828. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_0

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-829. CONTROL_WKUP_CONF_DEBUG_SEL_TST_1

Address Offset	0x0000 0464		
Physical Address	0x4AE0 C464	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_1 0x1: hwobs_int_cm1_1 0x3: hwobs_debug_abe_1 0x2: '0'	RW	0x0

Table 18-830. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_1

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-831. CONTROL_WKUP_CONF_DEBUG_SEL_TST_2

Address Offset	0x0000 0468		
Physical Address	0x4AE0 C468	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_2 0x1: hwobs_int_cm1_2 0x3: hwobs_debug_abe_2 0x2: '0'	RW	0x0

Table 18-832. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_2

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-833. CONTROL_WKUP_CONF_DEBUG_SEL_TST_3

Address Offset	0x0000 046C		
Physical Address	0x4AE0 C46C	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_3 0x1: hwobs_int_cm1_3 0x3: hwobs_debug_abe_3 0x2: '0'	RW	0x0

Table 18-834. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_3

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-835. CONTROL_WKUP_CONF_DEBUG_SEL_TST_4

Address Offset	0x0000 0470		
Physical Address	0x4AE0 C470	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_4 0x1: hwobs_int_cm1_4 0x3: hwobs_debug_abe_4 0x2: '0'	RW	0x0

Table 18-836. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_4

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-837. CONTROL_WKUP_CONF_DEBUG_SEL_TST_5

Address Offset	0x0000 0474		
Physical Address	0x4AE0 C474	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_5 0x1: hwobs_int_cm1_5 0x3: hwobs_debug_abe_5 0x2: '0'	RW	0x0

Table 18-838. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_5

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-839. CONTROL_WKUP_CONF_DEBUG_SEL_TST_6

Address Offset	0x0000 0478		
Physical Address	0x4AE0 C478	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_6 0x1: hwobs_int_cm1_6 0x3: hwobs_debug_abe_6 0x2: '0'	RW	0x0

Table 18-840. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_6

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-841. CONTROL_WKUP_CONF_DEBUG_SEL_TST_7

Address Offset	0x0000 047C		
Physical Address	0x4AE0 C47C	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_7 0x1: hwobs_int_cm1_7 0x3: hwobs_debug_abe_7 0x2: '0'	RW	0x0

Table 18-842. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_7

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-843. CONTROL_WKUP_CONF_DEBUG_SEL_TST_8

Address Offset	0x0000 0480		
Physical Address	0x4AE0 C480	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_8 0x1: hwobs_int_cm1_8 0x3: hwobs_debug_abe_8 0x2: '0'	RW	0x0

Table 18-844. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_8

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-845. CONTROL_WKUP_CONF_DEBUG_SEL_TST_9

Address Offset	0x0000 0484		
Physical Address	0x4AE0 C484	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_9 0x1: hwobs_int_cm1_9 0x3: hwobs_debug_abe_9 0x2: '0'	RW	0x0

Table 18-846. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_9

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-847. CONTROL_WKUP_CONF_DEBUG_SEL_TST_10

Address Offset	0x0000 0488		
Physical Address	0x4AE0 C488	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_10 0x1: hwobs_int_cm1_10 0x3: hwobs_debug_abe_10 0x2: '0'	RW	0x0

Table 18-848. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_10

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-849. CONTROL_WKUP_CONF_DEBUG_SEL_TST_11

Address Offset	0x0000 048C		
Physical Address	0x4AE0 C48C	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_11 0x1: hwobs_int_cm1_11 0x3: hwobs_debug_abe_11 0x2: '0'	RW	0x0

Table 18-850. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_11

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-851. CONTROL_WKUP_CONF_DEBUG_SEL_TST_12

Address Offset	0x0000 0490		
Physical Address	0x4AE0 C490	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_12 0x1: hwobs_int_cm1_12 0x3: hwobs_debug_abe_12 0x2: '0'	RW	0x0

Table 18-852. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_12

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-853. CONTROL_WKUP_CONF_DEBUG_SEL_TST_13

Address Offset	0x0000 0494		
Physical Address	0x4AE0 C494	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_13 0x1: hwobs_int_cm1_13 0x3: hwobs_debug_abe_13 0x2: '0'	RW	0x0

Table 18-854. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_13

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-855. CONTROL_WKUP_CONF_DEBUG_SEL_TST_14

Address Offset	0x0000 0498		
Physical Address	0x4AE0 C498	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_14 0x1: hwobs_int_cm1_14 0x3: hwobs_debug_abe_14 0x2: '0'	RW	0x0

Table 18-856. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_14

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-857. CONTROL_WKUP_CONF_DEBUG_SEL_TST_15

Address Offset	0x0000 049C		
Physical Address	0x4AE0 C49C	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_15 0x1: hwobs_int_cm1_15 0x3: hwobs_debug_abe_15 0x2: '0'	RW	0x0

Table 18-858. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_15

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- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-859. CONTROL_WKUP_CONF_DEBUG_SEL_TST_16

Address Offset	0x0000 04A0		
Physical Address	0x4AE0 C4A0	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_16 0x1: hwobs_int_cm1_16 0x3: hwobs_debug_abe_16 0x2: '0'	RW	0x0

Table 18-860. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_16

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-861. CONTROL_WKUP_CONF_DEBUG_SEL_TST_17

Address Offset	0x0000 04A4		
Physical Address	0x4AE0 C4A4	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_17 0x1: hwobs_int_cm1_17 0x3: hwobs_debug_abe_17 0x2: '0'	RW	0x0

Table 18-862. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_17

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-863. CONTROL_WKUP_CONF_DEBUG_SEL_TST_18

Address Offset	0x0000 04A8		
Physical Address	0x4AE0 C4A8	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_18 0x1: hwobs_int_cm1_18 0x3: hwobs_debug_abe_18 0x2: '0'	RW	0x0

Table 18-864. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_18

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-865. CONTROL_WKUP_CONF_DEBUG_SEL_TST_19

Address Offset	0x0000 04AC		
Physical Address	0x4AE0 C4AC	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_19 0x1: hwobs_int_cm1_19 0x3: hwobs_debug_abe_19 0x2: '0'	RW	0x0

Table 18-866. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_19

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-867. CONTROL_WKUP_CONF_DEBUG_SEL_TST_20

Address Offset	0x0000 04B0		
Physical Address	0x4AE0 C4B0	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_20 0x1: hwobs_int_cm1_20 0x3: hwobs_debug_abe_20 0x2: '0'	RW	0x0

Table 18-868. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_20

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-869. CONTROL_WKUP_CONF_DEBUG_SEL_TST_21

Address Offset	0x0000 04B4		
Physical Address	0x4AE0 C4B4	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_21 0x1: hwobs_int_cm1_21 0x3: hwobs_debug_abe_21 0x2: '0'	RW	0x0

Table 18-870. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_21

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-871. CONTROL_WKUP_CONF_DEBUG_SEL_TST_22

Address Offset	0x0000 04B8		
Physical Address	0x4AE0 C4B8	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_22 0x1: hwobs_int_cm1_22 0x3: hwobs_debug_abe_22 0x2: '0'	RW	0x0

Table 18-872. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_22

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-873. CONTROL_WKUP_CONF_DEBUG_SEL_TST_23

Address Offset	0x0000 04BC		
Physical Address	0x4AE0 C4BC	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_23 0x1: hwobs_int_cm1_23 0x3: hwobs_debug_abe_23 0x2: '0'	RW	0x0

Table 18-874. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_23

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-875. CONTROL_WKUP_CONF_DEBUG_SEL_TST_24

Address Offset	0x0000 04C0		
Physical Address	0x4AE0 C4C0	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_24 0x1: hwobs_int_cm1_24 0x3: hwobs_debug_abe_24 0x2: '0'	RW	0x0

Table 18-876. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_24

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-877. CONTROL_WKUP_CONF_DEBUG_SEL_TST_25

Address Offset	0x0000 04C4		
Physical Address	0x4AE0 C4C4	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_25 0x1: hwobs_int_cm1_25 0x3: hwobs_debug_abe_25 0x2: '0'	RW	0x0

Table 18-878. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_25

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-879. CONTROL_WKUP_CONF_DEBUG_SEL_TST_26

Address Offset	0x0000 04C8		
Physical Address	0x4AE0 C4C8	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_26 0x1: hwobs_int_cm1_26 0x3: hwobs_debug_abe_26 0x2: '0'	RW	0x0

Table 18-880. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_26

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-881. CONTROL_WKUP_CONF_DEBUG_SEL_TST_27

Address Offset	0x0000 04CC		
Physical Address	0x4AE0 C4CC	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_27 0x1: hwobs_int_cm1_27 0x3: hwobs_debug_abe_27 0x2: '0'	RW	0x0

Table 18-882. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_27

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-883. CONTROL_WKUP_CONF_DEBUG_SEL_TST_28

Address Offset	0x0000 04D0		
Physical Address	0x4AE0 C4D0	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_28 0x1: hwobs_int_cm1_28 0x3: hwobs_debug_abe_28 0x2: '0'	RW	0x0

Table 18-884. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_28

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-885. CONTROL_WKUP_CONF_DEBUG_SEL_TST_29

Address Offset	0x0000 04D4		
Physical Address	0x4AE0 C4D4	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_29 0x1: hwobs_int_cm1_29 0x3: hwobs_debug_abe_29 0x2: '0'	RW	0x0

Table 18-886. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_29

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

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Table 18-887. CONTROL_WKUP_CONF_DEBUG_SEL_TST_30

Address Offset	0x0000 04D8		
Physical Address	0x4AE0 C4D8	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_30 0x1: hwobs_int_cm1_30 0x3: hwobs_debug_abe_30 0x2: '0'	RW	0x0

Table 18-888. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_30

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-889. CONTROL_WKUP_CONF_DEBUG_SEL_TST_31

Address Offset	0x0000 04DC		
Physical Address	0x4AE0 C4DC	**Instance**	CTRL_MODULE_WKUP
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														MODE	

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1:0	MODE	Select one of the following signals : 0x0: hwobs_int_prm_31 0x1: hwobs_int_cm1_31 0x3: hwobs_debug_abe_31 0x2: '0'	RW	0x0

Table 18-890. Register Call Summary for Register CONTROL_WKUP_CONF_DEBUG_SEL_TST_31

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-891. CONTROL_WKUP_CONF_XBAR_SEL_0

Address Offset	0x0000 05DC		
Physical Address	0x4AE0 C5DC	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_3					RESERVED			CONF_XBAR_SEL_2					RESERVED			CONF_XBAR_SEL_1					RESERVED			CONF_XBAR_SEL_0				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_3	Select for xbar test_port_3	RW	0x03
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_2	Select for xbar test_port_2	RW	0x02
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_1	Select for xbar test_port_1	RW	0x01
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_0	Select for xbar test_port_0	RW	0x00

Table 18-892. Register Call Summary for Register CONTROL_WKUP_CONF_XBAR_SEL_0

Control Module Functional Description
- Cross-bar: [0]

Control Module Register Manual
- CTRL_MODULE_WKUP Register Summary: [1]

Table 18-893. CONTROL_WKUP_CONF_XBAR_SEL_4

Address Offset	0x0000 05E0		
Physical Address	0x4AE0 C5E0	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_7					RESERVED			CONF_XBAR_SEL_6					RESERVED			CONF_XBAR_SEL_5					RESERVED			CONF_XBAR_SEL_4				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_7	Select for xbar test_port_7	RW	0x07
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_6	Select for xbar test_port_6	RW	0x06
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_5	Select for xbar test_port_5	RW	0x05
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_4	Select for xbar test_port_4	RW	0x04

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Table 18-894. Register Call Summary for Register CONTROL_WKUP_CONF_XBAR_SEL_4

Control Module Functional Description • Cross-bar: [0]
Control Module Register Manual • CTRL_MODULE_WKUP Register Summary: [1]

Table 18-895. CONTROL_WKUP_CONF_XBAR_SEL_8

Address Offset	0x0000 05E4		
Physical Address	0x4AE0 C5E4	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_11					RESERVED			CONF_XBAR_SEL_10					RESERVED			CONF_XBAR_SEL_9					RESERVED			CONF_XBAR_SEL_8				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_11	Select for xbar test_port_11	RW	0x0B
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_10	Select for xbar test_port_10	RW	0x0A
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_9	Select for xbar test_port_9	RW	0x09
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_8	Select for xbar test_port_8	RW	0x08

Table 18-896. Register Call Summary for Register CONTROL_WKUP_CONF_XBAR_SEL_8

Control Module Functional Description • Cross-bar: [0]
Control Module Register Manual • CTRL_MODULE_WKUP Register Summary: [1]

Table 18-897. CONTROL_WKUP_CONF_XBAR_SEL_12

Address Offset	0x0000 05E8		
Physical Address	0x4AE0 C5E8	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_15					RESERVED			CONF_XBAR_SEL_14					RESERVED			CONF_XBAR_SEL_13					RESERVED				CONF_XBAR_SEL_12			

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_15	Select for xbar test_port_15	RW	0x0F
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_14	Select for xbar test_port_14	RW	0x0E
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_13	Select for xbar test_port_13	RW	0x0D
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_12	Select for xbar test_port_12	RW	0x0C

Table 18-898. Register Call Summary for Register CONTROL_WKUP_CONF_XBAR_SEL_12

Control Module Functional Description
- Cross-bar: [0]

Control Module Register Manual
- CTRL_MODULE_WKUP Register Summary: [1]

Table 18-899. CONTROL_WKUP_CONF_XBAR_SEL_16

Address Offset	0x0000 05EC		
Physical Address	0x4AE0 C5EC	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_19					RESERVED			CONF_XBAR_SEL_18					RESERVED			CONF_XBAR_SEL_17					RESERVED				CONF_XBAR_SEL_16			

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_19	Select for xbar test_port_19	RW	0x13
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_18	Select for xbar test_port_18	RW	0x12
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_17	Select for xbar test_port_17	RW	0x11
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_16	Select for xbar test_port_16	RW	0x10

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Table 18-900. Register Call Summary for Register CONTROL_WKUP_CONF_XBAR_SEL_16

Control Module Functional Description • Cross-bar: [0]
Control Module Register Manual • CTRL_MODULE_WKUP Register Summary: [1]

Table 18-901. CONTROL_WKUP_CONF_XBAR_SEL_20

Address Offset	0x0000 05F0		
Physical Address	0x4AE0 C5F0	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_23					RESERVED			CONF_XBAR_SEL_22					RESERVED			CONF_XBAR_SEL_21					RESERVED			CONF_XBAR_SEL_20				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_23	Select for xbar test_port_23	RW	0x17
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_22	Select for xbar test_port_22	RW	0x16
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_21	Select for xbar test_port_21	RW	0x15
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_20	Select for xbar test_port_20	RW	0x14

Table 18-902. Register Call Summary for Register CONTROL_WKUP_CONF_XBAR_SEL_20

Control Module Functional Description • Cross-bar: [0]
Control Module Register Manual • CTRL_MODULE_WKUP Register Summary: [1]

Table 18-903. CONTROL_WKUP_CONF_XBAR_SEL_24

Address Offset	0x0000 05F4		
Physical Address	0x4AE0 C5F4	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_27					RESERVED			CONF_XBAR_SEL_26					RESERVED			CONF_XBAR_SEL_25					RESERVED			CONF_XBAR_SEL_24				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_27	Select for xbar test_port_27	RW	0x1B
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_26	Select for xbar test_port_26	RW	0x1A
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_25	Select for xbar test_port_25	RW	0x19
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_24	Select for xbar test_port_24	RW	0x18

Table 18-904. Register Call Summary for Register CONTROL_WKUP_CONF_XBAR_SEL_24

Control Module Functional Description
- Cross-bar: [0]

Control Module Register Manual
- CTRL_MODULE_WKUP Register Summary: [1]

Table 18-905. CONTROL_WKUP_CONF_XBAR_SEL_28

Address Offset	0x0000 05F8		
Physical Address	0x4AE0 C5F8	**Instance**	CTRL_MODULE_WKUP
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CONF_XBAR_SEL_31					RESERVED			CONF_XBAR_SEL_30					RESERVED			CONF_XBAR_SEL_29					RESERVED			CONF_XBAR_SEL_28				

Bits	Field Name	Description	Type	Reset
31:29	RESERVED		R	0x0
28:24	CONF_XBAR_SEL_31	Select for xbar test_port_31	RW	0x1F
23:21	RESERVED		R	0x0
20:16	CONF_XBAR_SEL_30	Select for xbar test_port_30	RW	0x1E
15:13	RESERVED		R	0x0
12:8	CONF_XBAR_SEL_29	Select for xbar test_port_29	RW	0x1D
7:5	RESERVED		R	0x0
4:0	CONF_XBAR_SEL_28	Select for xbar test_port_28	RW	0x1C

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Table 18-906. Register Call Summary for Register CONTROL_WKUP_CONF_XBAR_SEL_28

Control Module Functional Description • Cross-bar: [0]
Control Module Register Manual • CTRL_MODULE_WKUP Register Summary: [1]

Table 18-907. CONTROL_WKUP_CONF_XBAR_BYPASS

Address Offset	0x0000 05FC		
Physical Address	0x4AE0 C5FC	**Instance**	CTRL_MODULE_WKUP
Description	Crossbar bypass control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SELECT

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	SELECT	Crossbar enable/disable 0x0: Crossbar is enabled 0x1: Crossbar is disabled (bypassed)	RW	1

Table 18-908. Register Call Summary for Register CONTROL_WKUP_CONF_XBAR_BYPASS

Control Module Functional Description • Cross-bar: [0] [1]
Control Module Register Manual • CTRL_MODULE_WKUP Register Summary: [2]

18.6.5 CTRL_MODULE_WKUP_PAD Registers

18.6.5.1 CTRL_MODULE_WKUP_PAD Register Summary

Table 18-909. CTRL_MODULE_WKUP_PAD Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_WKUP_PAD Base Address
CONTROL_WKUP_PAD_REVISION	R	32	0x0000 0000	0x4AE0 C800
CONTROL_WKUP_PAD_HWINFO	R	32	0x0000 0004	0x4AE0 C804
CONTROL_WKUP_PAD_SYSCONFIG	RW	32	0x0000 0010	0x4AE0 C810
CONTROL_WKUP_PAD0_LLIA_WAKEREQIN_PAD1_LLIB_WAKEREQIN	RW	32	0x0000 0040	0x4AE0 C840
CONTROL_WKUP_PAD0_DRM_EMU0_PAD1_DRM_EMU1	RW	32	0x0000 0044	0x4AE0 C844

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Table 18-909. CTRL_MODULE_WKUP_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_WKUP_PAD Base Address
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK	RW	32	0x0000 0048	0x4AE0 C848
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMSC	RW	32	0x0000 004C	0x4AE0 C84C
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO	RW	32	0x0000 0050	0x4AE0 C850
CONTROL_WKUP_PAD0_SYS_32K_PAD1_FREF_CLK_IOREQ	RW	32	0x0000 0054	0x4AE0 C854
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK1_OUT	RW	32	0x0000 0058	0x4AE0 C858
CONTROL_WKUP_PAD0_FREF_CLK2_OUT_PAD1_FREF_CLK2_REQ	RW	32	0x0000 005C	0x4AE0 C85C
CONTROL_WKUP_PAD0_FREF_CLK1_REQ_PAD1_SYS_NRESPWRON	RW	32	0x0000 0060	0x4AE0 C860
CONTROL_WKUP_PAD0_SYS_NRESWARM_PAD1_SYS_PWR_REQ	RW	32	0x0000 0064	0x4AE0 C864
CONTROL_WKUP_PAD0_SYS_NIRQ1_PAD1_SYS_NIRQ2	RW	32	0x0000 0068	0x4AE0 C868
CONTROL_WKUP_PAD0_SR_PMIC_SCL_PAD1_SR_PMIC_SDA	RW	32	0x0000 006C	0x4AE0 C86C
CONTROL_WKUP_PAD0_SYS_BOOT0_PAD1_SYS_BOOT1	RW	32	0x0000 0070	0x4AE0 C870
CONTROL_WKUP_PAD0_SYS_BOOT2_PAD1_SYS_BOOT3	RW	32	0x0000 0074	0x4AE0 C874
CONTROL_WKUP_PAD0_SYS_BOOT4_PAD1_SYS_BOOT5	RW	32	0x0000 0078	0x4AE0 C878
CONTROL_PADCONF_WAKEUPEVENT_0	R	32	0x0000 0080	0x4AE0 C880
CONTROL_SMART1NOPMIO_PADCONF_0	RW	32	0x0000 05A0	0x4AE0 CDA0
CONTROL_SMART1NOPMIO_PADCONF_1	RW	32	0x0000 05A4	0x4AE0 CDA4
CONTROL_WKUP_PADCONF_MODE	RW	32	0x0000 05A8	0x4AE0 CDA8
CONTROL_XTAL_OSCILLATOR	RW	32	0x0000 05AC	0x4AE0 CDAC
CONTROL_I2C_2	RW	32	0x0000 05B0	0x4AE0 CDB0
CONTROL_CKOBUFFER	RW	32	0x0000 05B4	0x4AE0 CDB4
CONTROL_WKUP_CONTROL_SPARE_RW	RW	32	0x0000 05B8	0x4AE0 CDB8
CONTROL_WKUP_CONTROL_SPARE_R	R	32	0x0000 05BC	0x4AE0 CDBC

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Table 18-909. CTRL_MODULE_WKUP_PAD Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	CTRL_MODULE_WKUP_PAD Base Address
CONTROL_WKUP_CONTROL_SPARE_R_C0	RW	32	0x0000 05C0	0x4AE0 CDC0
RESERVED	R	32	0x0000 05C4	0x4AE0 CDC4
CONTROL_EFUSE_1	RW	32	0x0000 05C8	0x4AE0 CDC8
CONTROL_EFUSE_2	RW	32	0x0000 05CC	0x4AE0 CDCC
CONTROL_EFUSE_3	RW	32	0x0000 05D0	0x4AE0 CDD0
CONTROL_EFUSE_4	RW	32	0x0000 05D4	0x4AE0 CDD4
CONTROL_EFUSE_5	RW	32	0x0000 05D8	0x4AE0 CDD8
CONTROL_EFUSE_6	RW	32	0x0000 05DC	0x4AE0 CDDC
CONTROL_EFUSE_7	RW	32	0x0000 05E0	0x4AE0 CDE0
CONTROL_EFUSE_8	RW	32	0x0000 05E4	0x4AE0 CDE4
CONTROL_EFUSE_9	RW	32	0x0000 05E8	0x4AE0 CDE8
CONTROL_EFUSE_10	RW	32	0x0000 05EC	0x4AE0 CDEC
CONTROL_EFUSE_11	RW	32	0x0000 05F0	0x4AE0 CDF0
CONTROL_EFUSE_12	RW	32	0x0000 05F4	0x4AE0 CDF4
CONTROL_EFUSE_13	RW	32	0x0000 05F8	0x4AE0 CDF8

18.6.5.2 CTRL_MODULE_WKUP_PAD Register Description

Table 18-910. CONTROL_WKUP_PAD_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4AE0 C800 0x4AE0 C800	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Control module revision identifier Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISON																															

Bits	Field Name	Description	Type	Reset
31:0	REVISON	IP Revision	R	TI Internal data

Table 18-911. Register Call Summary for Register CONTROL_WKUP_PAD_REVISION

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-912. CONTROL_WKUP_PAD_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4AE0 C804 0x4AE0 C804	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Information about the IP module hardware configuration i.e. typically the module HDL generics (if any). Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	IP_HWINFO	IP-module dependent	R	0x0000 0000

Table 18-913. Register Call Summary for Register CONTROL_WKUP_PAD_HWINFO

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-914. CONTROL_WKUP_PAD_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4AE0 C810 0x4AE0 C810	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IP_SYSCONFIG_IDLEMODE		RESERVED	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:2	IP_SYSCONFIG_IDLEMODE	RESERVED (not used).	RW	0x2
1:0	RESERVED		R	0x0

Table 18-915. Register Call Summary for Register CONTROL_WKUP_PAD_SYSCONFIG

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-916. CONTROL_WKUP_PAD0_LLIA_WAKEREQIN_PAD1_LLIB_WAKEREQIN

Address Offset	0x0000 0040		
Physical Address	0x4AE0 C840 0x4AE0 C840	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads llia_wakereqin and llib_wakereqin Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LLIB_WAKEREQIN_WAKEUPEVENT	LLIB_WAKEREQIN_WAKEUPENABLE	RESERVED					LLIB_WAKEREQIN_INPUTENABLE	RESERVED		LLIB_WAKEREQIN_PWRDOWN	LLIB_WAKEREQIN_PULLTYPESELECT	LLIB_WAKEREQIN_PULLUDENABLE	LLIB_WAKEREQIN_MUXMODE			LLIA_WAKEREQIN_WAKEUPEVENT	LLIA_WAKEREQIN_WAKEUPENABLE	RESERVED					LLIA_WAKEREQIN_INPUTENABLE	RESERVED		LLIA_WAKEREQIN_PWRDOWN	LLIA_WAKEREQIN_PULLTYPESELECT	LLIA_WAKEREQIN_PULLUDENABLE	LLIA_WAKEREQIN_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	LLIB_WAKEREQIN_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	LLIB_WAKEREQIN_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	LLIB_WAKEREQIN_INPUTENABLE	Input enable value for pad llib_wakereqin 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	LLIB_WAKEREQIN_PWRDOWN	Power Down setting for pad llib_wakereqin 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	LLIB_WAKEREQIN_PULLTYPESELECT	Pull-Up/Down selection for pad llib_wakereqin 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	LLIB_WAKEREQIN_PULLUDENABLE	Pull-Up/Down enable for pad llib_wakereqin 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	LLIB_WAKEREQIN_MUXMODE	Functional multiplexing selection for pad llib_wakereqin 0x0: Select llib_wakereqin 0x1: Reserved 0x6: Select gpio1_wk15 0x7: Select safe_mode_wakeup0 0x5: Select hw_wkdbg13	RW	0x7
15	LLIA_WAKEREQIN_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	LLIA_WAKEREQIN_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
8	LLIA_WAKEREQIN_INPUTENABLE	Input enable value for pad llia_wakereqin 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	LLIA_WAKEREQIN_PWRDOWN	Power Down setting for pad llia_wakereqin 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	LLIA_WAKEREQIN_PULLTYPESELECT	Pull-Up/Down selection for pad llia_wakereqin 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	LLIA_WAKEREQIN_PULLUDENABLE	Pull-Up/Down enable for pad llia_wakereqin 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	LLIA_WAKEREQIN_MUXMODE	Functional multiplexing selection for pad llia_wakereqin 0x0: Select llia_wakereqin 0x1: Reserved 0x6: Select gpio1_wk14 0x7: Select safe_mode_wakeup1 0x5: Select hw_wkdbg14	RW	0x7

Table 18-917. Register Call Summary for Register CONTROL_WKUP_PAD0_LLIA_WAKEREQIN_PAD1_LLIB_WAKEREQIN

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the WKUP Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [3]

Table 18-918. CONTROL_WKUP_PAD0_DRM_EMU0_PAD1_DRM_EMU1

Address Offset	0x0000 0044		
Physical Address	0x4AE0 C844 0x4AE0 C844	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads drm_emu0 and drm_emu1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRM_EMU1_WAKEUPEVENT	DRM_EMU1_WAKEUPENABLE	RESERVED					DRM_EMU1_INPUTENABLE	RESERVED		DRM_EMU1_PWRDOWN	DRM_EMU1_PULLTYPESELECT	DRM_EMU1_PULLUDENABLE	DRM_EMU1_MUXMODE			DRM_EMU0_WAKEUPEVENT	DRM_EMU0_WAKEUPENABLE	RESERVED					DRM_EMU0_INPUTENABLE	RESERVED		DRM_EMU0_PWRDOWN	DRM_EMU0_PULLTYPESELECT	DRM_EMU0_PULLUDENABLE	DRM_EMU0_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	DRM_EMU1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	DRM_EMU1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	DRM_EMU1_INPUTENABLE	Input enable value for pad drm_emu1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	DRM_EMU1_PWRDOWN	Power Down setting for pad drm_emu1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	DRM_EMU1_PULLTYPESELECT	Pull-Up/Down selection for pad drm_emu1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	DRM_EMU1_PULLUDENABLE	Pull-Up/Down enable for pad drm_emu1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	DRM_EMU1_MUXMODE	Functional multiplexing selection for pad drm_emu1 0x0: Select drm_emu1 0x6: Select gpio1_wk7 0x7: Select safe_mode_wakeup3 0x5: Select hw_wkdbg7	RW	0x0
15	DRM_EMU0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	DRM_EMU0_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	DRM_EMU0_INPUTENABLE	Input enable value for pad drm_emu0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	DRM_EMU0_PWRDOWN	Power Down setting for pad drm_emu0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	DRM_EMU0_PULLTYPESELECT	Pull-Up/Down selection for pad drm_emu0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	DRM_EMU0_PULLUDENABLE	Pull-Up/Down enable for pad drm_emu0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	DRM_EMU0_MUXMODE	Functional multiplexing selection for pad drm_emu0 0x0: Select drm_emu0 0x6: Select gpio1_wk6 0x7: Select safe_mode_wakeup2 0x5: Select hw_wkdbg6	RW	0x0

Table 18-919. Register Call Summary for Register CONTROL_WKUP_PAD0_DRM_EMU0_PAD1_DRM_EMU1

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the WKUP Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [3]

Table 18-920. CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK

Address Offset	0x0000 0048		
Physical Address	0x4AE0 C848 0x4AE0 C848	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads jtag_ntrst and jtag_tck Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							JTAG_TCK_INPUTENABLE	RESERVED		JTAG_TCK_PWRDOWN	JTAG_TCK_PULLTYPESELECT	JTAG_TCK_PULLUDENABLE	JTAG_TCK_MUXMODE			RESERVED							JTAG_NTRST_INPUTENABLE	RESERVED		JTAG_NTRST_PWRDOWN	JTAG_NTRST_PULLTYPESELECT	JTAG_NTRST_PULLUDENABLE	JTAG_NTRST_MUXMODE	

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	JTAG_TCK_INPUTENABLE	Input enable value for pad jtag_tck 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	JTAG_TCK_PWRDOWN	Power Down setting for pad jtag_tck 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	JTAG_TCK_PULLTYPESELECT	Pull-Up/Down selection for pad jtag_tck 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	JTAG_TCK_PULLUDENABLE	Pull-Up/Down enable for pad jtag_tck 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	JTAG_TCK_MUXMODE	Functional multiplexing selection for pad jtag_tck 0x0: Select jtag_tck 0x7: Select safe_mode_wakeup5	RW	0x0
15:9	RESERVED		R	0x00
8	JTAG_NTRST_INPUTENABLE	Input enable value for pad jtag_ntrst 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	JTAG_NTRST_PWRDOWN	Power Down setting for pad jtag_ntrst 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	JTAG_NTRST_PULLTYPESELECT	Pull-Up/Down selection for pad jtag_ntrst 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	JTAG_NTRST_PULLUDENABLE	Pull-Up/Down enable for pad jtag_ntrst 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	JTAG_NTRST_MUXMODE	Functional multiplexing selection for pad jtag_ntrst 0x0: Select jtag_ntrst 0x7: Select safe_mode_wakeup4	RW	0x0

Table 18-921. Register Call Summary for Register CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_WKUP_PAD Register Summary: [2]

Table 18-922. CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMSC

Address Offset	0x0000 004C		
Physical Address	0x4AE0 C84C 0x4AE0 C84C	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads jtag_rtck and jtag_tmsc Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							JTAG_TMSC_INPUTENABLE	RESERVED		JTAG_TMSC_PWRDOWN	JTAG_TMSC_PULLTYPESELECT	JTAG_TMSC_PULLUDENABLE	JTAG_TMSC_MUXMODE			RESERVED							JTAG_RTCK_INPUTENABLE	RESERVED		JTAG_RTCK_PWRDOWN	JTAG_RTCK_PULLTYPESELECT	JTAG_RTCK_PULLUDENABLE	JTAG_RTCK_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	JTAG_TMSC_INPUTENABLE	Input enable value for pad jtag_tmsc 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	JTAG_TMSC_PWRDOWN	Power Down setting for pad jtag_tmsc 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	JTAG_TMSC_PULLTYPESELECT	Pull-Up/Down selection for pad jtag_tmsc 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	JTAG_TMSC_PULLUDENABLE	Pull-Up/Down enable for pad jtag_tmsc 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	JTAG_TMSC_MUXMODE	Functional multiplexing selection for pad jtag_tmsc 0x0: Select jtag_tmsc 0x7: Select safe_mode_wakeup7	RW	0x0
15:9	RESERVED		R	0x00
8	JTAG_RTCK_INPUTENABLE	Input enable value for pad jtag_rtck 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	JTAG_RTCK_PWRDOWN	Power Down setting for pad jtag_rtck 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	JTAG_RTCK_PULLTYPESELECT	Pull-Up/Down selection for pad jtag_rtck 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	JTAG_RTCK_PULLUDENABLE	Pull-Up/Down enable for pad jtag_rtck 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	JTAG_RTCK_MUXMODE	Functional multiplexing selection for pad jtag_rtck 0x0: Select jtag_rtck 0x7: Select safe_mode_wakeup6	RW	0x0

Table 18-923. Register Call Summary for Register CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMSC

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [2]

Table 18-924. CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO

Address Offset	0x0000 0050		
Physical Address	0x4AE0 C850 0x4AE0 C850	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads jtag_tdi and jtag_tdo Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							JTAG_TDO_INPUTENABLE	RESERVED		JTAG_TDO_PWRDOWN	JTAG_TDO_PULLTYPESELECT	JTAG_TDO_PULLUDENABLE	JTAG_TDO_MUXMODE			RESERVED							JTAG_TDI_INPUTENABLE	RESERVED		JTAG_TDI_PWRDOWN	JTAG_TDI_PULLTYPESELECT	JTAG_TDI_PULLUDENABLE	JTAG_TDI_MUXMODE		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	JTAG_TDO_INPUTENABLE	Input enable value for pad jtag_tdo 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	JTAG_TDO_PWRDOWN	Power Down setting for pad jtag_tdo 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	JTAG_TDO_PULLTYPESELECT	Pull-Up/Down selection for pad jtag_tdo 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	JTAG_TDO_PULLUDENABLE	Pull-Up/Down enable for pad jtag_tdo 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	JTAG_TDO_MUXMODE	Functional multiplexing selection for pad jtag_tdo 0x0: Select jtag_tdo 0x7: Select safe_mode_wakeup9	RW	0x0
15:9	RESERVED		R	0x00
8	JTAG_TDI_INPUTENABLE	Input enable value for pad jtag_tdi 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	JTAG_TDI_PWRDOWN	Power Down setting for pad jtag_tdi 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	JTAG_TDI_PULLTYPESELECT	Pull-Up/Down selection for pad jtag_tdi 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	JTAG_TDI_PULLUDENABLE	Pull-Up/Down enable for pad jtag_tdi 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	JTAG_TDI_MUXMODE	Functional multiplexing selection for pad jtag_tdi 0x0: Select jtag_tdi 0x7: Select safe_mode_wakeup8	RW	0x0

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Table 18-925. Register Call Summary for Register CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [2]

Table 18-926. CONTROL_WKUP_PAD0_SYS_32K_PAD1_FREF_CLK_IOREQ

Address Offset	0x0000 0054		
Physical Address	0x4AE0 C854 0x4AE0 C854	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads sys_32k and fref_clk_ioreq Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_CLK_IOREQ_WAKEUPEVENT	FREF_CLK_IOREQ_WAKEUPENABLE	RESERVED					FREF_CLK_IOREQ_INPUTENABLE	RESERVED		FREF_CLK_IOREQ_PWRDOWN	FREF_CLK_IOREQ_PULLTYPESELECT	FREF_CLK_IOREQ_PULLUDENABLE	FREF_CLK_IOREQ_MUXMODE			RESERVED							SYS_32K_INPUTENABLE	RESERVED		SYS_32K_PWRDOWN	SYS_32K_PULLTYPESELECT	SYS_32K_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31	FREF_CLK_IOREQ_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	FREF_CLK_IOREQ_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	FREF_CLK_IOREQ_INPUTENABLE	Input enable value for pad fref_clk_ioreq 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	FREF_CLK_IOREQ_PWRDOWN	Power Down setting for pad fref_clk_ioreq 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	FREF_CLK_IOREQ_PULLTYPESELECT	Pull-Up/Down selection for pad fref_clk_ioreq 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	FREF_CLK_IOREQ_PULLUDENABLE	Pull-Up/Down enable for pad fref_clk_ioreq 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
18:16	FREF_CLK_IOREQ_MUXMODE	Functional multiplexing selection for pad fref_clk_ioreq 0x0: Select fref_clk_ioreq 0x7: Select safe_mode_wakeup10 0x6: Select gpio1_wk13	RW	0x0
15:9	RESERVED		R	0x00
8	SYS_32K_INPUTENABLE	Input enable value for pad sys_32k 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	SYS_32K_PWRDOWN	Power Down setting for pad sys_32k 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	SYS_32K_PULLTYPESELECT	Pull-Up/Down selection for pad sys_32k 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	SYS_32K_PULLUDENABLE	Pull-Up/Down enable for pad sys_32k 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
2:0	RESERVED		R	0x0

Table 18-927. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_32K_PAD1_FREF_CLK_IOREQ

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_WKUP_PAD Register Summary: [2]

Table 18-928. CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK1_OUT

Address Offset	0x0000 0058		
Physical Address	0x4AE0 C858 0x4AE0 C858	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads fref_clk0_out and fref_clk1_out Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_CLK1_OUT_WAKEUPEVENT	FREF_CLK1_OUT_WAKEUPENABLE	RESERVED					FREF_CLK1_OUT_INPUTENABLE	RESERVED		FREF_CLK1_OUT_PWRDOWN	FREF_CLK1_OUT_PULLTYPESELECT	FREF_CLK1_OUT_PULLUDENABLE	FREF_CLK1_OUT_MUXMODE			FREF_CLK0_OUT_WAKEUPEVENT	FREF_CLK0_OUT_WAKEUPENABLE	RESERVED					FREF_CLK0_OUT_INPUTENABLE	RESERVED		FREF_CLK0_OUT_PWRDOWN	FREF_CLK0_OUT_PULLTYPESELECT	FREF_CLK0_OUT_PULLUDENABLE	FREF_CLK0_OUT_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31	FREF_CLK1_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	FREF_CLK1_OUT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	FREF_CLK1_OUT_INPUTENABLE	Input enable value for pad fref_clk1_out 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	FREF_CLK1_OUT_PWRDOWN	Power Down setting for pad fref_clk1_out 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	FREF_CLK1_OUT_PULLTYPESELECT	Pull-Up/Down selection for pad fref_clk1_out 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	FREF_CLK1_OUT_PULLUDENABLE	Pull-Up/Down enable for pad fref_clk1_out 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	FREF_CLK1_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk1_out 0x0: Select fref_clk1_out 0x6: Select gpio1_wk11 0x7: Select safe_mode_wakeup12 0x5: Select hw_wkdbg5	RW	0x7
15	FREF_CLK0_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	FREF_CLK0_OUT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	FREF_CLK0_OUT_INPUTENABLE	Input enable value for pad fref_clk0_out 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	FREF_CLK0_OUT_PWRDOWN	Power Down setting for pad fref_clk0_out 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	FREF_CLK0_OUT_PULLTYPESELECT	Pull-Up/Down selection for pad fref_clk0_out 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	FREF_CLK0_OUT_PULLUDENABLE	Pull-Up/Down enable for pad fref_clk0_out 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1

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Bits	Field Name	Description	Type	Reset
2:0	FREF_CLK0_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk0_out 0x0: Select fref_clk0_out 0x6: Select gpio1_wk12 0x7: Select safe_mode_wakeup11 0x5: Select hw_wkdbg9	RW	0x0

Table 18-929. Register Call Summary for Register CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK1_OUT

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the WKUP Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [3]

Table 18-930. CONTROL_WKUP_PAD0_FREF_CLK2_OUT_PAD1_FREF_CLK2_REQ

Address Offset	0x0000 005C		
Physical Address	0x4AE0 C85C 0x4AE0 C85C	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads fref_clk2_out and fref_clk2_req Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREF_CLK2_REQ_WAKEUPEVENT	FREF_CLK2_REQ_WAKEUPENABLE	RESERVED					FREF_CLK2_REQ_INPUTENABLE	RESERVED		FREF_CLK2_REQ_PWRDOWN	FREF_CLK2_REQ_PULLTYPESELECT	FREF_CLK2_REQ_PULLUDENABLE	FREF_CLK2_REQ_MUXMODE			FREF_CLK2_OUT_WAKEUPEVENT	FREF_CLK2_OUT_WAKEUPENABLE	RESERVED					FREF_CLK2_OUT_INPUTENABLE	RESERVED		FREF_CLK2_OUT_PWRDOWN	FREF_CLK2_OUT_PULLTYPESELECT	FREF_CLK2_OUT_PULLUDENABLE	FREF_CLK2_OUT_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	FREF_CLK2_REQ_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	FREF_CLK2_REQ_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	FREF_CLK2_REQ_INPUTENABLE	Input enable value for pad fref_clk2_req 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	FREF_CLK2_REQ_PWRDOWN	Power Down setting for pad fref_clk2_req 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	FREF_CLK2_REQ_PULLTYPESELECT	Pull-Up/Down selection for pad fref_clk2_req 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	FREF_CLK2_REQ_PULLUDENABLE	Pull-Up/Down enable for pad fref_clk2_req 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	FREF_CLK2_REQ_MUXMODE	Functional multiplexing selection for pad fref_clk2_req 0x6: Select gpio1_wk9 0x1: Select fref_clk3_out 0x7: Select safe_mode_wakeup14 0x0: Select fref_clk2_req 0x5: Select hw_wkdbg11 0x3: Select sys_ndmareq0	RW	0x7
15	FREF_CLK2_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	FREF_CLK2_OUT_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	FREF_CLK2_OUT_INPUTENABLE	Input enable value for pad fref_clk2_out 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	FREF_CLK2_OUT_PWRDOWN	Power Down setting for pad fref_clk2_out 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	FREF_CLK2_OUT_PULLTYPESELECT	Pull-Up/Down selection for pad fref_clk2_out 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	FREF_CLK2_OUT_PULLUDENABLE	Pull-Up/Down enable for pad fref_clk2_out 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	FREF_CLK2_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk2_out 0x0: Select fref_clk2_out 0x6: Select gpio1_wk10 0x7: Select safe_mode_wakeup13 0x5: Select hw_wkdbg10	RW	0x7

Table 18-931. Register Call Summary for Register CONTROL_WKUP_PAD0_FREF_CLK2_OUT_PAD1_FREF_CLK2_REQ

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the WKUP Power Domain: [2]

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [3]

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Table 18-932. CONTROL_WKUP_PAD0_FREF_CLK1_REQ_PAD1_SYS_NRESPWRON

Address Offset	0x0000 0060		
Physical Address	0x4AE0 C860 0x4AE0 C860	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads fref_clk1_req and sys_nrespwron Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SYS_NRESPWRON_PWRDOWN	SYS_NRESPWRON_PULLTYPESELECT	SYS_NRESPWRON_PULLUDENABLE	RESERVED			FREF_CLK1_REQ_WAKEUPEVENT	FREF_CLK1_REQ_WAKEUPENABLE	RESERVED					FREF_CLK1_REQ_INPUTENABLE	RESERVED		FREF_CLK1_REQ_PWRDOWN	FREF_CLK1_REQ_PULLTYPESELECT	FREF_CLK1_REQ_PULLUDENABLE	FREF_CLK1_REQ_MUXMODE				

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21	SYS_NRESPWRON_PWRDOWN	Power Down setting for pad sys_nrespwron 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	SYS_NRESPWRON_PULLTYPESELECT	Pull-Up/Down selection for pad sys_nrespwron 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	SYS_NRESPWRON_PULLUDENABLE	Pull-Up/Down enable for pad sys_nrespwron 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
18:16	RESERVED		R	0x0
15	FREF_CLK1_REQ_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	FREF_CLK1_REQ_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	FREF_CLK1_REQ_INPUTENABLE	Input enable value for pad fref_clk1_req 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	FREF_CLK1_REQ_PWRDOWN	Power Down setting for pad fref_clk1_req 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0

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Bits	Field Name	Description	Type	Reset
4	FREF_CLK1_REQ_PULLTYPESELECT	Pull-Up/Down selection for pad fref_clk1_req 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	FREF_CLK1_REQ_PULLUDENABLE	Pull-Up/Down enable for pad fref_clk1_req 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	FREF_CLK1_REQ_MUXMODE	Functional multiplexing selection for pad fref_clk1_req 0x0: Select fref_clk1_req 0x6: Select gpio1_wk8 0x3: Select sys_ndmareq1 0x7: Select safe_mode_wakeup15 0x5: Select hw_wkdbg12	RW	0x7

Table 18-933. Register Call Summary for Register CONTROL_WKUP_PAD0_FREF_CLK1_REQ_PAD1_SYS_NRESPWRON

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the WKUP Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [3]

Table 18-934. CONTROL_WKUP_PAD0_SYS_NRESWARM_PAD1_SYS_PWR_REQ

Address Offset	0x0000 0064		
Physical Address	0x4AE0 C864 0x4AE0 C864	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads sys_nreswarm and sys_pwr_req Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SYS_PWR_REQ_INPUTENABLE	RESERVED		SYS_PWR_REQ_PWRDOWN	SYS_PWR_REQ_PULLTYPESELECT	SYS_PWR_REQ_PULLUDENABLE	SYS_PWR_REQ_MUXMODE			RESERVED								SYS_NRESWARM_PWRDOWN	SYS_NRESWARM_PULLTYPESELECT	SYS_NRESWARM_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	SYS_PWR_REQ_INPUTENABLE	Input enable value for pad sys_pwr_req 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
21	SYS_PWR_REQ_PWRDOWN	Power Down setting for pad sys_pwr_req 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	SYS_PWR_REQ_PULLTYPESELECT	Pull-Up/Down selection for pad sys_pwr_req 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	SYS_PWR_REQ_PULLUDENABLE	Pull-Up/Down enable for pad sys_pwr_req 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	SYS_PWR_REQ_MUXMODE	Functional multiplexing selection for pad sys_pwr_req 0x0: Select sys_pwr_req 0x7: Select safe_mode_wakeup16 0x5: Select hw_wkdbg15	RW	0x0
15:6	RESERVED		R	0x000
5	SYS_NRESWARM_PWRDOWN	Power Down setting for pad sys_nreswarm 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	SYS_NRESWARM_PULLTYPESELECT	Pull-Up/Down selection for pad sys_nreswarm 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	SYS_NRESWARM_PULLUDENABLE	Pull-Up/Down enable for pad sys_nreswarm 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18-935. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_NRESWARM_PAD1_SYS_PWR_REQ

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the WKUP Power Domain: [2]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [3]

Table 18-936. CONTROL_WKUP_PAD0_SYS_NIRQ1_PAD1_SYS_NIRQ2

Address Offset	0x0000 0068		
Physical Address	0x4AE0 C868 0x4AE0 C868	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads sys_nirq1 and sys_nirq2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_NIRQ2_WAKEUPEVENT	SYS_NIRQ2_WAKEUPENABLE	RESERVED					SYS_NIRQ2_INPUTENABLE	RESERVED		SYS_NIRQ2_PWRDOWN	SYS_NIRQ2_PULLTYPESELECT	SYS_NIRQ2_PULLUDENABLE	SYS_NIRQ2_MUXMODE			SYS_NIRQ1_WAKEUPEVENT	SYS_NIRQ1_WAKEUPENABLE	RESERVED					SYS_NIRQ1_INPUTENABLE	RESERVED		SYS_NIRQ1_PWRDOWN	SYS_NIRQ1_PULLTYPESELECT	SYS_NIRQ1_PULLUDENABLE	SYS_NIRQ1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SYS_NIRQ2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	SYS_NIRQ2_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	SYS_NIRQ2_INPUTENABLE	Input enable value for pad sys_nirq2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	SYS_NIRQ2_PWRDOWN	Power Down setting for pad sys_nirq2 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	SYS_NIRQ2_PULLTYPESELECT	Pull-Up/Down selection for pad sys_nirq2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	SYS_NIRQ2_PULLUDENABLE	Pull-Up/Down enable for pad sys_nirq2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	SYS_NIRQ2_MUXMODE	Functional multiplexing selection for pad sys_nirq2 0x0: Select sys_nirq2 0x6: Select gpio1_wk17	RW	0x0
15	SYS_NIRQ1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	SYS_NIRQ1_WAKEUPENABLE	Input pad wake-up enable 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	SYS_NIRQ1_INPUTENABLE	Input enable value for pad sys_nirq1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	SYS_NIRQ1_PWRDOWN	Power Down setting for pad sys_nirq1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0

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Bits	Field Name	Description	Type	Reset
4	SYS_NIRQ1_PULLTYPESELECT	Pull-Up/Down selection for pad sys_nirq1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	SYS_NIRQ1_PULLUDENABLE	Pull-Up/Down enable for pad sys_nirq1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	SYS_NIRQ1_MUXMODE	Functional multiplexing selection for pad sys_nirq1 0x0: Select sys_nirq1 0x6: Select gpio1_wk16	RW	0x0

Table 18-937. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_NIRQ1_PAD1_SYS_NIRQ2

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [2]

Table 18-938. CONTROL_WKUP_PAD0_SR_PMIC_SCL_PAD1_SR_PMIC_SDA

Address Offset	0x0000 006C		
Physical Address	0x4AE0 C86C 0x4AE0 C86C	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads sr_pmic_scl and sr_pmic_sda Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SR_PMIC_SDA_INPUTENABLE	RESERVED		SR_PMIC_SDA_PWRDOWN	SR_PMIC_SDA_PULLTYPESELECT	SR_PMIC_SDA_PULLUDENABLE	RESERVED										SR_PMIC_SCL_INPUTENABLE	RESERVED		SR_PMIC_SCL_PWRDOWN	SR_PMIC_SCL_PULLTYPESELECT	SR_PMIC_SCL_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	SR_PMIC_SDA_INPUTENABLE	Input enable value for pad sr_pmic_sda 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	SR_PMIC_SDA_PWRDOWN	Power Down setting for pad sr_pmic_sda 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	SR_PMIC_SDA_PULLTYPESELECT	Pull-Up/Down selection for pad sr_pmic_sda 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0

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Bits	Field Name	Description	Type	Reset
19	SR_PMIC_SDA_PULLUDENABLE	Pull-Up/Down enable for pad sr_pmic_sda 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
18:9	RESERVED		R	0x000
8	SR_PMIC_SCL_INPUTENABLE	Input enable value for pad sr_pmic_scl 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	SR_PMIC_SCL_PWRDOWN	Power Down setting for pad sr_pmic_scl 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	SR_PMIC_SCL_PULLTYPESELECT	Pull-Up/Down selection for pad sr_pmic_scl 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	SR_PMIC_SCL_PULLUDENABLE	Pull-Up/Down enable for pad sr_pmic_scl 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
2:0	RESERVED		R	0x0

Table 18-939. Register Call Summary for Register CONTROL_WKUP_PAD0_SR_PMIC_SCL_PAD1_SR_PMIC_SDA

Control Module Functional Description
- Pad Multiplexing Register Fields: [0] [1]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [2]

Table 18-940. CONTROL_WKUP_PAD0_SYS_BOOT0_PAD1_SYS_BOOT1

Address Offset	0x0000 0070		
Physical Address	0x4AE0 C870 0x4AE0 C870	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads sys_boot0 and sys_boot1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SYS_BOOT1_INPUTENABLE	RESERVED		SYS_BOOT1_PWRDOWN	SYS_BOOT1_PULLTYPESELECT	SYS_BOOT1_PULLUDENABLE	SYS_BOOT1_MUXMODE			RESERVED							SYS_BOOT0_INPUTENABLE	RESERVED		SYS_BOOT0_PWRDOWN	SYS_BOOT0_PULLTYPESELECT	SYS_BOOT0_PULLUDENABLE	SYS_BOOT0_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	SYS_BOOT1_INPUTENABLE	Input enable value for pad sys_boot1 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	SYS_BOOT1_PWRDOWN	Power Down setting for pad sys_boot1 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	SYS_BOOT1_PULLTYPESELECT	Pull-Up/Down selection for pad sys_boot1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	SYS_BOOT1_PULLUDENABLE	Pull-Up/Down enable for pad sys_boot1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
18:16	SYS_BOOT1_MUXMODE	Functional multiplexing selection for pad sys_boot1 0x6: Select gpio1_wkout1 0x7: Select safe_mode_wakeup18 0x0: Select sys_boot1 0x4: Select drm_emu16 0x5: Select hw_wkdbg1 0x3: Select drm_emu3	RW	0x0
15:9	RESERVED		R	0x00
8	SYS_BOOT0_INPUTENABLE	Input enable value for pad sys_boot0 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	SYS_BOOT0_PWRDOWN	Power Down setting for pad sys_boot0 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	SYS_BOOT0_PULLTYPESELECT	Pull-Up/Down selection for pad sys_boot0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	SYS_BOOT0_PULLUDENABLE	Pull-Up/Down enable for pad sys_boot0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
2:0	SYS_BOOT0_MUXMODE	Functional multiplexing selection for pad sys_boot0 0x6: Select gpio1_wkout0 0x7: Select safe_mode_wakeup17 0x0: Select sys_boot0 0x4: Select drm_emu15 0x5: Select hw_wkdbg0 0x3: Select drm_emu2	RW	0x0

Table 18-941. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_BOOT0_PAD1_SYS_BOOT1

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the WKUP Power Domain: [2]

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Table 18-941. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_BOOT0_PAD1_SYS_BOOT1 (continued)

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [3]

Table 18-942. CONTROL_WKUP_PAD0_SYS_BOOT2_PAD1_SYS_BOOT3

Address Offset	0x0000 0074		
Physical Address	0x4AE0 C874 0x4AE0 C874	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads sys_boot2 and sys_boot3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SYS_BOOT3_INPUTENABLE	RESERVED		SYS_BOOT3_PWRDOWN	SYS_BOOT3_PULLTYPESELECT	SYS_BOOT3_PULLUDENABLE	SYS_BOOT3_MUXMODE			RESERVED							SYS_BOOT2_INPUTENABLE	RESERVED		SYS_BOOT2_PWRDOWN	SYS_BOOT2_PULLTYPESELECT	SYS_BOOT2_PULLUDENABLE	SYS_BOOT2_MUXMODE		

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	SYS_BOOT3_INPUTENABLE	Input enable value for pad sys_boot3 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	SYS_BOOT3_PWRDOWN	Power Down setting for pad sys_boot3 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	SYS_BOOT3_PULLTYPESELECT	Pull-Up/Down selection for pad sys_boot3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	SYS_BOOT3_PULLUDENABLE	Pull-Up/Down enable for pad sys_boot3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
18:16	SYS_BOOT3_MUXMODE	Functional multiplexing selection for pad sys_boot3 0x0: Select sys_boot3 0x6: Select gpio1_wkout3 0x4: Select drm_emu18 0x7: Select safe_mode_wakeup20 0x5: Select hw_wkdbg3 0x3: Select drm_emu5	RW	0x0
15:9	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
8	SYS_BOOT2_INPUTENABLE	Input enable value for pad sys_boot2 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	SYS_BOOT2_PWRDOWN	Power Down setting for pad sys_boot2 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	SYS_BOOT2_PULLTYPESELECT	Pull-Up/Down selection for pad sys_boot2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	SYS_BOOT2_PULLUDENABLE	Pull-Up/Down enable for pad sys_boot2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
2:0	SYS_BOOT2_MUXMODE	Functional multiplexing selection for pad sys_boot2 0x0: Select sys_boot2 0x6: Select gpio1_wkout2 0x4: Select drm_emu17 0x7: Select safe_mode_wakeup19 0x5: Select hw_wkdbg2 0x3: Select drm_emu4	RW	0x0

Table 18-943. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_BOOT2_PAD1_SYS_BOOT3

Control Module Functional Description • Pad Multiplexing Register Fields: [0] [1]
Control Module Register Manual • CTRL_MODULE_WKUP_PAD Register Summary: [2]

Table 18-944. CONTROL_WKUP_PAD0_SYS_BOOT4_PAD1_SYS_BOOT5

Address Offset	0x0000 0078		
Physical Address	0x4AE0 C878 0x4AE0 C878	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	Register control for Pads sys_boot4 and sys_boot5 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							SYS_BOOT5_INPUTENABLE	RESERVED		SYS_BOOT5_PWRDOWN	SYS_BOOT5_PULLTYPESELECT	SYS_BOOT5_PULLUDENABLE	SYS_BOOT5_MUXMODE			RESERVED							SYS_BOOT4_INPUTENABLE	RESERVED		SYS_BOOT4_PWRDOWN	SYS_BOOT4_PULLTYPESELECT	SYS_BOOT4_PULLUDENABLE	SYS_BOOT4_MUXMODE		

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Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	SYS_BOOT5_INPUTENABLE	Input enable value for pad sys_boot5 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:22	RESERVED		R	0x0
21	SYS_BOOT5_PWRDOWN	Power Down setting for pad sys_boot5 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
20	SYS_BOOT5_PULLTYPESELECT	Pull-Up/Down selection for pad sys_boot5 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	SYS_BOOT5_PULLUDENABLE	Pull-Up/Down enable for pad sys_boot5 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
18:16	SYS_BOOT5_MUXMODE	Functional multiplexing selection for pad sys_boot5 0x0: Select sys_boot5 0x1: Reserved 0x6: Select gpio1_wkout5 0x7: Select safe_mode_wakeup22 0x5: Select hw_wkdbg8	RW	0x0
15:9	RESERVED		R	0x00
8	SYS_BOOT4_INPUTENABLE	Input enable value for pad sys_boot4 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:6	RESERVED		R	0x0
5	SYS_BOOT4_PWRDOWN	Power Down setting for pad sys_boot4 0x0: IO cell power is ON 0x1: IO cell power is OFF	RW	0
4	SYS_BOOT4_PULLTYPESELECT	Pull-Up/Down selection for pad sys_boot4 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	SYS_BOOT4_PULLUDENABLE	Pull-Up/Down enable for pad sys_boot4 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
2:0	SYS_BOOT4_MUXMODE	Functional multiplexing selection for pad sys_boot4 0x0: Select sys_boot4 0x6: Select gpio1_wkout4 0x4: Select drm_emu19 0x7: Select safe_mode_wakeup21 0x5: Select hw_wkdbg4 0x3: Select drm_emu6	RW	0x0

Table 18-945. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_BOOT4_PAD1_SYS_BOOT5

Control Module Functional Description

- Pad Multiplexing Register Fields: [0] [1]
- Observability Signals Muxed on Pads in the WKUP Power Domain: [2]

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [3]

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Table 18-946. PADCONF_WAKEUPEVENT_0

Address Offset	0x0000 0080		
Physical Address	Please refer to Table 18-909	**Instance**	CTRL_MODULE_WKUP_PAD
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				SYS_NIRQ2_DUPLICATEWAKEUPEVENT	SYS_NIRQ1_DUPLICATEWAKEUPEVENT	FREF_CLK1_REQ_DUPLICATEWAKEUPEVENT	FREF_CLK2_REQ_DUPLICATEWAKEUPEVENT	FREF_CLK2_OUT_DUPLICATEWAKEUPEVENT	FREF_CLK1_OUT_DUPLICATEWAKEUPEVENT	FREF_CLK0_OUT_DUPLICATEWAKEUPEVENT	FREF_CLK_IOREQ_DUPLICATEWAKEUPEVENT	DRM_EMU1_DUPLICATEWAKEUPEVENT	DRM_EMU0_DUPLICATEWAKEUPEVENT	LLIB_WAKEREQIN_DUPLICATEWAKEUPEVENT	LLIA_WAKEREQIN_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11	SYS_NIRQ2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad sys_nirq2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
10	SYS_NIRQ1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad sys_nirq1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
9	FREF_CLK1_REQ_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad fref_clk1_req Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
8	FREF_CLK2_REQ_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad fref_clk2_req Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
7	FREF_CLK2_OUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad fref_clk2_out Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
6	FREF_CLK1_OUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad fref_clk1_out Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
5	FREF_CLK0_OUT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad fref_clk0_out Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

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Bits	Field Name	Description	Type	Reset
4	FREF_CLK_IOREQ_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad fref_clk_ioreq Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
3	DRM_EMU1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad drm_emu1 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
2	DRM_EMU0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad drm_emu0 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
1	LLIB_WAKEREQIN_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad llib_wakereqin Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
0	LLIA_WAKEREQIN_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad llia_wakereqin Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0

Table 18-947. CONTROL_SMART1NOPMIO_PADCONF_0

Address Offset	0x0000 05A0		
Physical Address	0x4AE0 CDA0 0x4AE0 CDA0	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	SMART1 NOPM IO control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4 3 2 1 0
BOOT_GPO_DS	RESERVED	FREF_IOREQ_DS	FREF_OUT0_DS	FREF_OUT1_DS	FREF_OUT2_DS	FREF_REQ1_DS	FREF_REQ2_DS	JTAG_PART0_DS	JTAG_PART1_DS	LLIA_WKUP0_DS	SYS_DS	SR_LB	RESERVED

Bits	Field Name	Description	Type	Reset
31:30	BOOT_GPO_DS	drive stength for boot gpo ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
29:28	RESERVED		R	0x0
27:26	FREF_IOREQ_DS	drive stength for fref ioreq ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2

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Bits	Field Name	Description	Type	Reset
25:24	FREF_OUT0_DS	drive stength for fref out0 ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
23:22	FREF_OUT1_DS	drive stength for fref out1 ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
21:20	FREF_OUT2_DS	drive stength for fref out2 ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
19:18	FREF_REQ1_DS	drive stength for fref req1 ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
17:16	FREF_REQ2_DS	drive stength for fref req2 ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
15:14	JTAG_PART0_DS	drive stength for jtag part0 ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
13:12	JTAG_PART1_DS	drive stength for jtag part1 ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
11:10	LLIA_WKUP0_DS	drive stength for llia wakeup0 ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2
9:8	SYS_DS	drive stength for sys ds 0x0: 120 ohm 0x1: 60 ohm 0x3: 30 ohm 0x2: 45 ohm	RW	0x2

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Bits	Field Name	Description	Type	Reset
7:6	SR_LB	Control for internal pull-up resistors in both Fast and High-Speed modes for sr group of pads: In Fast-Speed mode: 0x0: 5-15pf 0x1: 15-50pf 0x3: N/A 0x2: 50-150pf In High-Speed mode: 0x0: 5-12pf 0x1: 12-25pf 0x3: 50-80pf 0x2: 25-50pf	RW	0x0
5:0	RESERVED		R	0x00

Table 18-948. Register Call Summary for Register CONTROL_SMART1NOPMIO_PADCONF_0

Control Module Functional Description

- Signal Integrity Parameter Controls Overview: [0]
- SMART I/O Buffers with Slew Rate and Drive Strength Control Settings: [1]
- I2Cx I/Os Group PULLUPRESX Controls and Load Range Settings: [2]
- Device Interfaces Signal Group Controls Mapping: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [14]

Table 18-949. CONTROL_SMART1NOPMIO_PADCONF_1

Address Offset	0x0000 05A4		
Physical Address	0x4AE0 CDA4 0x4AE0 CDA4	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	SMART1 NOPM IO control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6 5 4 3 2 1 0
BOOT_GPO_SC	RESERVED	FREF_IOREQ_SC	FREF_OUT0_SC	FREF_OUT1_SC	FREF_OUT2_SC	FREF_REQ1_SC	FREF_REQ2_SC	JTAG_PART0_SC	JTAG_PART1_SC	LLIA_WKUP0_SC	SYS_SC	RESERVED

Bits	Field Name	Description	Type	Reset
31:30	BOOT_GPO_SC	slew rate control for boot gpo sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
29:28	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
27:26	FREF_IOREQ_SC	slew rate control for fref ioreq sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
25:24	FREF_OUT0_SC	slew rate control for fref out0 sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
23:22	FREF_OUT1_SC	slew rate control for fref out1 sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
21:20	FREF_OUT2_SC	slew rate control for fref out2 sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
19:18	FREF_REQ1_SC	slew rate control for fref req1 sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
17:16	FREF_REQ2_SC	slew rate control for fref req2 sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
15:14	JTAG_PART0_SC	slew rate control for jtag part0 sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
13:12	JTAG_PART1_SC	slew rate control for jtag part1 sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x2
11:10	LLIA_WKUP0_SC	slew rate control for llia wakeup0 sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0

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Bits	Field Name	Description	Type	Reset
9:8	SYS_SC	slew rate control for sys sc 0x0: slow 0x1: medium 0x3: not_applicable 0x2: fast	RW	0x0
7:0	RESERVED		R	0x00

Table 18-950. Register Call Summary for Register CONTROL_SMART1NOPMIO_PADCONF_1

Control Module Functional Description • Signal Integrity Parameter Controls Overview: [0] • SMART I/O Buffers with Slew Rate and Drive Strength Control Settings: [1] • Device Interfaces Signal Group Controls Mapping: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
Control Module Register Manual • CTRL_MODULE_WKUP_PAD Register Summary: [13]

Table 18-951. CONTROL_WKUP_PADCONF_MODE

Address Offset	0x0000 05A8		
Physical Address	0x4AE0 CDA8 0x4AE0 CDA8	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	PAD Conf Mode Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDDS_25_MODE	VDDS_26_MODE	RESERVED																													

Bits	Field Name	Description	Type	Reset
31	VDDS_25_MODE	PAD Voltage level control for vdds_25_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
30	VDDS_26_MODE	PAD Voltage level control for vdds_26_mode 0x0: VDDS = 1.8V 0x1: VDDS = 1.2V	RW	0
29:0	RESERVED		R	0x0000 0000

Table 18-952. Register Call Summary for Register CONTROL_WKUP_PADCONF_MODE

Control Module Functional Description • Device Wake-Up Control Module Instance: [0] • Dual Voltage-Supplied Peripheral Controls: [1] [2] [3]
Control Module Programming Guide • Pad Configuration Programming Points: [4]
Control Module Register Manual • CTRL_MODULE_WKUP_PAD Register Summary: [5]

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Table 18-953. CONTROL_XTAL_OSCILLATOR

Address Offset	0x0000 05AC		
Physical Address	0x4AE0 CDAC 0x4AE0 CDAC	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	XTAL OSCILLATOR control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSCILLATOR_BOOST	OSCILLATOR_OS_OUT	RESERVED																													

Bits	Field Name	Description	Type	Reset
31	OSCILLATOR_BOOST	Fast startup control 0x0: Fast startup is disabled 0x1: Fast startup is enabled	RW	1
30	OSCILLATOR_OS_OUT	Oscillator output Read 0x1: BOOST is disabled Read 0x0: low to high transition in BOOST mode	R	0
29:0	RESERVED		R	0x0000 0000

Table 18-954. Register Call Summary for Register CONTROL_XTAL_OSCILLATOR

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-955. CONTROL_I2C_2

Address Offset	0x0000 05B0		
Physical Address	0x4AE0 CDB0 0x4AE0 CDB0	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	I2C pads control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR_PMIC_SDA_GLFENB	SR_PMIC_SDA_PULLUPRESX	SR_PMIC_SCL_GLFENB	SR_PMIC_SCL_PULLUPRESX	RESERVED																											

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Bits	Field Name	Description	Type	Reset
31	SR_PMIC_SDA_GLFENB	Active_high glitch free operation enable pin for pmic_sda receiver 0x0: Disable pmic_sda glitch free operation 0x1: Enable pmic_sda glitch free operation	RW	0
30	SR_PMIC_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for pmic_sda 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
29	SR_PMIC_SCL_GLFENB	Active_high glitch free operation enable pin for pmic_scl receiver 0x0: Disable pmic_scl glitch free operation 0x1: Enable pmic_scl glitch free operation	RW	0
28	SR_PMIC_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for pmic_scl 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
27:0	RESERVED		R	0x000 0000

Table 18-956. Register Call Summary for Register CONTROL_I2C_2

Control Module Functional Description
- Signal Integrity Parameter Controls Overview: [0]
- I2Cx I/Os Group PULLUPRESX Controls and Load Range Settings: [1] [2] [3] [4]

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [5]

Table 18-957. CONTROL_CKOBUFFER

Address Offset	0x0000 05B4		
Physical Address	0x4AE0 CDB4 0x4AE0 CDB4	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	CKO buffer control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKOBUFFER_OUT_EN	CKOBUFFER_ALTSEL	CKOBUFFER_POLARITY	CKOBUFFER_CLK_EN	RESERVED																											

Bits	Field Name	Description	Type	Reset
31	CKOBUFFER_OUT_EN	Output buffer enable. 0x0: The output buffer is driving a clock signal 0x1: The output buffer (fref_xtal_clk pad) does not drive a clock signal. Its output value depends on the value of the CKOBUFFER_POLARITY bit.	RW	0
30	CKOBUFFER_ALTSEL	Selects an alternative clock source. 0x0: The output buffer drives the same signal present on the fref_xtal_in pad 0x1: The output buffer drives an alternative clock. In this case 0 is present on the pad. There is no alternative clock.	RW	0

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Bits	Field Name	Description	Type	Reset
29	CKOBUFFER_POLARITY	Defines the polarity of the clock-out buffer when the CKOBUFFER_OUT_EN bit is set to 0x0. 0x0: The output buffer is 0. 0x1: The output buffer is 1.	RW	0
28	CKOBUFFER_CLK_EN	Output clock enable control. 0x0: The output clock is disabled. 0x1: The output clock is enabled.	RW	0
27:0	RESERVED	Reserved	R	0x000 0000

Table 18-958. Register Call Summary for Register CONTROL_CKOBUFFER

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-959. CONTROL_WKUP_CONTROL_SPARE_RW

Address Offset	0x0000 05B8		
Physical Address	0x4AE0 CDB8 0x4AE0 CDB8	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	WKUP control spare RW Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_RW																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_RW	wkup control spare register bits RW	RW	0x0000 0000

Table 18-960. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_RW

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-961. CONTROL_WKUP_CONTROL_SPARE_R

Address Offset	0x0000 05BC		
Physical Address	0x4AE0 CDBC 0x4AE0 CDBC	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	WKUP control spare R Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_R																															

Bits	Field Name	Description	Type	Reset
31:0	WKUP_CONTROL_SPARE_R	wkup control spare register bits R	R	0x0000 0000

Table 18-962. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_R

Control Module Register Manual
- CTRL_MODULE_WKUP_PAD Register Summary: [0]

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Table 18-963. CONTROL_WKUP_CONTROL_SPARE_R_C0

Address Offset	0x0000 05C0		
Physical Address	0x4AE0 CDC0 0x4AE0 CDC0	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	WKUP control spare RC Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKUP_CONTROL_SPARE_R_C0	WKUP_CONTROL_SPARE_R_C1	WKUP_CONTROL_SPARE_R_C2	WKUP_CONTROL_SPARE_R_C3	WKUP_CONTROL_SPARE_R_C4	WKUP_CONTROL_SPARE_R_C5	WKUP_CONTROL_SPARE_R_C6	WKUP_CONTROL_SPARE_R_C7	RESERVED																									

Bits	Field Name	Description	Type	Reset
31	WKUP_CONTROL_SPARE_R_C0	wkup control spare register bits RC	RW W1toClr	0
30	WKUP_CONTROL_SPARE_R_C1	wkup control spare register bits RC	RW W1toClr	0
29	WKUP_CONTROL_SPARE_R_C2	wkup control spare register bits RC	RW W1toClr	0
28	WKUP_CONTROL_SPARE_R_C3	wkup control spare register bits RC	RW W1toClr	0
27	WKUP_CONTROL_SPARE_R_C4	wkup control spare register bits RC	RW W1toClr	0
26	WKUP_CONTROL_SPARE_R_C5	wkup control spare register bits RC	RW W1toClr	0
25	WKUP_CONTROL_SPARE_R_C6	wkup control spare register bits RC	RW W1toClr	0
24	WKUP_CONTROL_SPARE_R_C7	wkup control spare register bits RC	RW W1toClr	0
23:0	RESERVED		R	0x00 0000

Table 18-964. Register Call Summary for Register CONTROL_WKUP_CONTROL_SPARE_R_C0

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-965. CONTROL_EFUSE_1

Address Offset	0x0000 05C8		
Physical Address	0x4AE0 CDC8 0x4AE0 CDC8	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 1. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDRDIFF_PTV_NORTH_SIDE_N5	DDRDIFF_PTV_NORTH_SIDE_N4	DDRDIFF_PTV_NORTH_SIDE_N3	DDRDIFF_PTV_NORTH_SIDE_N2	DDRDIFF_PTV_NORTH_SIDE_N1	DDRDIFF_PTV_NORTH_SIDE_N0	DDRDIFF_PTV_NORTH_SIDE_P5	DDRDIFF_PTV_NORTH_SIDE_P4	DDRDIFF_PTV_NORTH_SIDE_P3	DDRDIFF_PTV_NORTH_SIDE_P2	DDRDIFF_PTV_NORTH_SIDE_P1	DDRDIFF_PTV_NORTH_SIDE_P0	DDRDIFF_PTV_EAST_SIDE_N5	DDRDIFF_PTV_EAST_SIDE_N4	DDRDIFF_PTV_EAST_SIDE_N3	DDRDIFF_PTV_EAST_SIDE_N2	DDRDIFF_PTV_EAST_SIDE_N1	DDRDIFF_PTV_EAST_SIDE_N0	DDRDIFF_PTV_EAST_SIDE_P5	DDRDIFF_PTV_EAST_SIDE_P4	DDRDIFF_PTV_EAST_SIDE_P3	DDRDIFF_PTV_EAST_SIDE_P2	DDRDIFF_PTV_EAST_SIDE_P1	DDRDIFF_PTV_EAST_SIDE_P0	RESERVED							

Bits	Field Name	Description	Type	Reset
31	DDRDIFF_PTV_NORTH_SIDE_N5	control_ddrdiff_ptv_north_side_n5 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_n5	RW	0
30	DDRDIFF_PTV_NORTH_SIDE_N4	control_ddrdiff_ptv_north_side_n4 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_n4	RW	0
29	DDRDIFF_PTV_NORTH_SIDE_N3	control_ddrdiff_ptv_north_side_n3 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_n3	RW	0
28	DDRDIFF_PTV_NORTH_SIDE_N2	control_ddrdiff_ptv_north_side_n2 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_n2	RW	0
27	DDRDIFF_PTV_NORTH_SIDE_N1	control_ddrdiff_ptv_north_side_n1 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_n1	RW	0
26	DDRDIFF_PTV_NORTH_SIDE_N0	control_ddrdiff_ptv_north_side_n0 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_n0	RW	0
25	DDRDIFF_PTV_NORTH_SIDE_P5	control_ddrdiff_ptv_north_side_p5 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_p5	RW	0
24	DDRDIFF_PTV_NORTH_SIDE_P4	control_ddrdiff_ptv_north_side_p4 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_p4	RW	0
23	DDRDIFF_PTV_NORTH_SIDE_P3	control_ddrdiff_ptv_north_side_p3 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_p3	RW	0
22	DDRDIFF_PTV_NORTH_SIDE_P2	control_ddrdiff_ptv_north_side_p2 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_p2	RW	0
21	DDRDIFF_PTV_NORTH_SIDE_P1	control_ddrdiff_ptv_north_side_p1 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_p1	RW	0
20	DDRDIFF_PTV_NORTH_SIDE_P0	control_ddrdiff_ptv_north_side_p0 Note that reset is exported. Its value is = pi_ddrdiff_ptv_north_side_p0	RW	0
19	DDRDIFF_PTV_EAST_SIDE_N5	control_ddrdiff_ptv_east_side_n5 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_n5	RW	0
18	DDRDIFF_PTV_EAST_SIDE_N4	control_ddrdiff_ptv_east_side_n4 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_n4	RW	0
17	DDRDIFF_PTV_EAST_SIDE_N3	control_ddrdiff_ptv_east_side_n3 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_n3	RW	0

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Bits	Field Name	Description	Type	Reset
16	DDRDIFF_PTV_EAST_SIDE_N2	control_ddrdiff_ptv_east_side_n2 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_n2	RW	0
15	DDRDIFF_PTV_EAST_SIDE_N1	control_ddrdiff_ptv_east_side_n1 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_n1	RW	0
14	DDRDIFF_PTV_EAST_SIDE_N0	control_ddrdiff_ptv_east_side_n0 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_n0	RW	0
13	DDRDIFF_PTV_EAST_SIDE_P5	control_ddrdiff_ptv_east_side_p5 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_p5	RW	0
12	DDRDIFF_PTV_EAST_SIDE_P4	control_ddrdiff_ptv_east_side_p4 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_p4	RW	0
11	DDRDIFF_PTV_EAST_SIDE_P3	control_ddrdiff_ptv_east_side_p3 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_p3	RW	0
10	DDRDIFF_PTV_EAST_SIDE_P2	control_ddrdiff_ptv_east_side_p2 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_p2	RW	0
9	DDRDIFF_PTV_EAST_SIDE_P1	control_ddrdiff_ptv_east_side_p1 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_p1	RW	0
8	DDRDIFF_PTV_EAST_SIDE_P0	control_ddrdiff_ptv_east_side_p0 Note that reset is exported. Its value is = pi_ddrdiff_ptv_east_side_p0	RW	0
7:0	RESERVED		R	0x00

Table 18-966. Register Call Summary for Register CONTROL_EFUSE_1

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0] [1]

Table 18-967. CONTROL_EFUSE_2

Address Offset	0x0000 05CC		
Physical Address	0x4AE0 CDCC 0x4AE0 CDCC	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 2. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDRDIFF_PTV_SOUTH_SIDE_N5	DDRDIFF_PTV_SOUTH_SIDE_N4	DDRDIFF_PTV_SOUTH_SIDE_N3	DDRDIFF_PTV_SOUTH_SIDE_N2	DDRDIFF_PTV_SOUTH_SIDE_N1	DDRDIFF_PTV_SOUTH_SIDE_N0	DDRDIFF_PTV_SOUTH_SIDE_P5	DDRDIFF_PTV_SOUTH_SIDE_P4	DDRDIFF_PTV_SOUTH_SIDE_P3	DDRDIFF_PTV_SOUTH_SIDE_P2	DDRDIFF_PTV_SOUTH_SIDE_P1	DDRDIFF_PTV_SOUTH_SIDE_P0	DDRDIFF_PTV_WEST_SIDE_N5	DDRDIFF_PTV_WEST_SIDE_N4	DDRDIFF_PTV_WEST_SIDE_N3	DDRDIFF_PTV_WEST_SIDE_N2	DDRDIFF_PTV_WEST_SIDE_N1	DDRDIFF_PTV_WEST_SIDE_N0	DDRDIFF_PTV_WEST_SIDE_P5	DDRDIFF_PTV_WEST_SIDE_P4	DDRDIFF_PTV_WEST_SIDE_P3	DDRDIFF_PTV_WEST_SIDE_P2	DDRDIFF_PTV_WEST_SIDE_P1	DDRDIFF_PTV_WEST_SIDE_P0	RESERVED							

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Bits	Field Name	Description	Type	Reset
31	DDRDIFF_PTV_SOUTH_SIDE_N5	control_ddrdiff_ptv_south_side_n5 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_n5	RW	0
30	DDRDIFF_PTV_SOUTH_SIDE_N4	control_ddrdiff_ptv_south_side_n4 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_n4	RW	0
29	DDRDIFF_PTV_SOUTH_SIDE_N3	control_ddrdiff_ptv_south_side_n3 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_n3	RW	0
28	DDRDIFF_PTV_SOUTH_SIDE_N2	control_ddrdiff_ptv_south_side_n2 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_n2	RW	0
27	DDRDIFF_PTV_SOUTH_SIDE_N1	control_ddrdiff_ptv_south_side_n1 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_n1	RW	0
26	DDRDIFF_PTV_SOUTH_SIDE_N0	control_ddrdiff_ptv_south_side_n0 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_n0	RW	0
25	DDRDIFF_PTV_SOUTH_SIDE_P5	control_ddrdiff_ptv_south_side_p5 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_p5	RW	0
24	DDRDIFF_PTV_SOUTH_SIDE_P4	control_ddrdiff_ptv_south_side_p4 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_p4	RW	0
23	DDRDIFF_PTV_SOUTH_SIDE_P3	control_ddrdiff_ptv_south_side_p3 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_p3	RW	0
22	DDRDIFF_PTV_SOUTH_SIDE_P2	control_ddrdiff_ptv_south_side_p2 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_p2	RW	0
21	DDRDIFF_PTV_SOUTH_SIDE_P1	control_ddrdiff_ptv_south_side_p1 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_p1	RW	0
20	DDRDIFF_PTV_SOUTH_SIDE_P0	control_ddrdiff_ptv_south_side_p0 Note that reset is exported. Its value is = pi_ddrdiff_ptv_south_side_p0	RW	0
19	DDRDIFF_PTV_WEST_SIDE_N5	control_ddrdiff_ptv_west_side_n5 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_n5	RW	0
18	DDRDIFF_PTV_WEST_SIDE_N4	control_ddrdiff_ptv_west_side_n4 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_n4	RW	0
17	DDRDIFF_PTV_WEST_SIDE_N3	control_ddrdiff_ptv_west_side_n3 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_n3	RW	0
16	DDRDIFF_PTV_WEST_SIDE_N2	control_ddrdiff_ptv_west_side_n2 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_n2	RW	0
15	DDRDIFF_PTV_WEST_SIDE_N1	control_ddrdiff_ptv_west_side_n1 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_n1	RW	0
14	DDRDIFF_PTV_WEST_SIDE_N0	control_ddrdiff_ptv_west_side_n0 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_n0	RW	0
13	DDRDIFF_PTV_WEST_SIDE_P5	control_ddrdiff_ptv_west_side_p5 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_p5	RW	0
12	DDRDIFF_PTV_WEST_SIDE_P4	control_ddrdiff_ptv_west_side_p4 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_p4	RW	0

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Bits	Field Name	Description	Type	Reset
11	DDRDIFF_PTV_WEST_SIDE_P3	control_ddrdiff_ptv_west_side_p3 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_p3	RW	0
10	DDRDIFF_PTV_WEST_SIDE_P2	control_ddrdiff_ptv_west_side_p2 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_p2	RW	0
9	DDRDIFF_PTV_WEST_SIDE_P1	control_ddrdiff_ptv_west_side_p1 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_p1	RW	0
8	DDRDIFF_PTV_WEST_SIDE_P0	control_ddrdiff_ptv_west_side_p0 Note that reset is exported. Its value is = pi_ddrdiff_ptv_west_side_p0	RW	0
7:0	RESERVED		R	0x00

Table 18-968. Register Call Summary for Register CONTROL_EFUSE_2

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-969. CONTROL_EFUSE_3

Address Offset	0x0000 05D0		
Physical Address	0x4AE0 CDD0 0x4AE0 CDD0	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 3. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDRSE_PTV_NORTH_SIDE_N5	DDRSE_PTV_NORTH_SIDE_N4	DDRSE_PTV_NORTH_SIDE_N3	DDRSE_PTV_NORTH_SIDE_N2	DDRSE_PTV_NORTH_SIDE_N1	DDRSE_PTV_NORTH_SIDE_N0	DDRSE_PTV_NORTH_SIDE_P5	DDRSE_PTV_NORTH_SIDE_P4	DDRSE_PTV_NORTH_SIDE_P3	DDRSE_PTV_NORTH_SIDE_P2	DDRSE_PTV_NORTH_SIDE_P1	DDRSE_PTV_NORTH_SIDE_P0	DDRSE_PTV_EAST_SIDE_N5	DDRSE_PTV_EAST_SIDE_N4	DDRSE_PTV_EAST_SIDE_N3	DDRSE_PTV_EAST_SIDE_N2	DDRSE_PTV_EAST_SIDE_N1	DDRSE_PTV_EAST_SIDE_N0	DDRSE_PTV_EAST_SIDE_P5	DDRSE_PTV_EAST_SIDE_P4	DDRSE_PTV_EAST_SIDE_P3	DDRSE_PTV_EAST_SIDE_P2	DDRSE_PTV_EAST_SIDE_P1	DDRSE_PTV_EAST_SIDE_P0	RESERVED							

Bits	Field Name	Description	Type	Reset
31	DDRSE_PTV_NORTH_SIDE_N5	control_ddrse_ptv_north_side_n5 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_n5	RW	0
30	DDRSE_PTV_NORTH_SIDE_N4	control_ddrse_ptv_north_side_n4 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_n4	RW	0
29	DDRSE_PTV_NORTH_SIDE_N3	control_ddrse_ptv_north_side_n3 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_n3	RW	0
28	DDRSE_PTV_NORTH_SIDE_N2	control_ddrse_ptv_north_side_n2 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_n2	RW	0
27	DDRSE_PTV_NORTH_SIDE_N1	control_ddrse_ptv_north_side_n1 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_n1	RW	0

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Bits	Field Name	Description	Type	Reset
26	DDRSE_PTV_NORTH_SIDE_N0	control_ddrse_ptv_north_side_n0 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_n0	RW	0
25	DDRSE_PTV_NORTH_SIDE_P5	control_ddrse_ptv_north_side_p5 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_p5	RW	0
24	DDRSE_PTV_NORTH_SIDE_P4	control_ddrse_ptv_north_side_p4 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_p4	RW	0
23	DDRSE_PTV_NORTH_SIDE_P3	control_ddrse_ptv_north_side_p3 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_p3	RW	0
22	DDRSE_PTV_NORTH_SIDE_P2	control_ddrse_ptv_north_side_p2 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_p2	RW	0
21	DDRSE_PTV_NORTH_SIDE_P1	control_ddrse_ptv_north_side_p1 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_p1	RW	0
20	DDRSE_PTV_NORTH_SIDE_P0	control_ddrse_ptv_north_side_p0 Note that reset is exported. Its value is = pi_ddrse_ptv_north_side_p0	RW	0
19	DDRSE_PTV_EAST_SIDE_N5	control_ddrse_ptv_east_side_n5 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_n5	RW	0
18	DDRSE_PTV_EAST_SIDE_N4	control_ddrse_ptv_east_side_n4 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_n4	RW	0
17	DDRSE_PTV_EAST_SIDE_N3	control_ddrse_ptv_east_side_n3 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_n3	RW	0
16	DDRSE_PTV_EAST_SIDE_N2	control_ddrse_ptv_east_side_n2 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_n2	RW	0
15	DDRSE_PTV_EAST_SIDE_N1	control_ddrse_ptv_east_side_n1 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_n1	RW	0
14	DDRSE_PTV_EAST_SIDE_N0	control_ddrse_ptv_east_side_n0 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_n0	RW	0
13	DDRSE_PTV_EAST_SIDE_P5	control_ddrse_ptv_east_side_p5 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_p5	RW	0
12	DDRSE_PTV_EAST_SIDE_P4	control_ddrse_ptv_east_side_p4 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_p4	RW	0
11	DDRSE_PTV_EAST_SIDE_P3	control_ddrse_ptv_east_side_p3 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_p3	RW	0
10	DDRSE_PTV_EAST_SIDE_P2	control_ddrse_ptv_east_side_p2 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_p2	RW	0
9	DDRSE_PTV_EAST_SIDE_P1	control_ddrse_ptv_east_side_p1 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_p1	RW	0
8	DDRSE_PTV_EAST_SIDE_P0	control_ddrse_ptv_east_side_p0 Note that reset is exported. Its value is = pi_ddrse_ptv_east_side_p0	RW	0
7:0	RESERVED		R	0x00

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Table 18-970. Register Call Summary for Register CONTROL_EFUSE_3

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-971. CONTROL_EFUSE_4

Address Offset	0x0000 05D4		
Physical Address	0x4AE0 CDD4 0x4AE0 CDD4	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 4. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDRSE_PTV_SOUTH_SIDE_N5	DDRSE_PTV_SOUTH_SIDE_N4	DDRSE_PTV_SOUTH_SIDE_N3	DDRSE_PTV_SOUTH_SIDE_N2	DDRSE_PTV_SOUTH_SIDE_N1	DDRSE_PTV_SOUTH_SIDE_N0	DDRSE_PTV_SOUTH_SIDE_P5	DDRSE_PTV_SOUTH_SIDE_P4	DDRSE_PTV_SOUTH_SIDE_P3	DDRSE_PTV_SOUTH_SIDE_P2	DDRSE_PTV_SOUTH_SIDE_P1	DDRSE_PTV_SOUTH_SIDE_P0	DDRSE_PTV_WEST_SIDE_N5	DDRSE_PTV_WEST_SIDE_N4	DDRSE_PTV_WEST_SIDE_N3	DDRSE_PTV_WEST_SIDE_N2	DDRSE_PTV_WEST_SIDE_N1	DDRSE_PTV_WEST_SIDE_N0	DDRSE_PTV_WEST_SIDE_P5	DDRSE_PTV_WEST_SIDE_P4	DDRSE_PTV_WEST_SIDE_P3	DDRSE_PTV_WEST_SIDE_P2	DDRSE_PTV_WEST_SIDE_P1	DDRSE_PTV_WEST_SIDE_P0	RESERVED							

Bits	Field Name	Description	Type	Reset
31	DDRSE_PTV_SOUTH_SIDE_N5	control_ddrse_ptv_south_side_n5 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_n5	RW	0
30	DDRSE_PTV_SOUTH_SIDE_N4	control_ddrse_ptv_south_side_n4 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_n4	RW	0
29	DDRSE_PTV_SOUTH_SIDE_N3	control_ddrse_ptv_south_side_n3 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_n3	RW	0
28	DDRSE_PTV_SOUTH_SIDE_N2	control_ddrse_ptv_south_side_n2 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_n2	RW	0
27	DDRSE_PTV_SOUTH_SIDE_N1	control_ddrse_ptv_south_side_n1 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_n1	RW	0
26	DDRSE_PTV_SOUTH_SIDE_N0	control_ddrse_ptv_south_side_n0 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_n0	RW	0
25	DDRSE_PTV_SOUTH_SIDE_P5	control_ddrse_ptv_south_side_p5 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_p5	RW	0
24	DDRSE_PTV_SOUTH_SIDE_P4	control_ddrse_ptv_south_side_p4 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_p4	RW	0
23	DDRSE_PTV_SOUTH_SIDE_P3	control_ddrse_ptv_south_side_p3 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_p3	RW	0
22	DDRSE_PTV_SOUTH_SIDE_P2	control_ddrse_ptv_south_side_p2 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_p2	RW	0

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Bits	Field Name	Description	Type	Reset
21	DDRSE_PTV_SOUTH_SIDE_P1	control_ddrse_ptv_south_side_p1 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_p1	RW	0
20	DDRSE_PTV_SOUTH_SIDE_P0	control_ddrse_ptv_south_side_p0 Note that reset is exported. Its value is = pi_ddrse_ptv_south_side_p0	RW	0
19	DDRSE_PTV_WEST_SIDE_N5	control_ddrse_ptv_west_side_n5 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_n5	RW	0
18	DDRSE_PTV_WEST_SIDE_N4	control_ddrse_ptv_west_side_n4 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_n4	RW	0
17	DDRSE_PTV_WEST_SIDE_N3	control_ddrse_ptv_west_side_n3 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_n3	RW	0
16	DDRSE_PTV_WEST_SIDE_N2	control_ddrse_ptv_west_side_n2 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_n2	RW	0
15	DDRSE_PTV_WEST_SIDE_N1	control_ddrse_ptv_west_side_n1 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_n1	RW	0
14	DDRSE_PTV_WEST_SIDE_N0	control_ddrse_ptv_west_side_n0 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_n0	RW	0
13	DDRSE_PTV_WEST_SIDE_P5	control_ddrse_ptv_west_side_p5 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_p5	RW	0
12	DDRSE_PTV_WEST_SIDE_P4	control_ddrse_ptv_west_side_p4 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_p4	RW	0
11	DDRSE_PTV_WEST_SIDE_P3	control_ddrse_ptv_west_side_p3 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_p3	RW	0
10	DDRSE_PTV_WEST_SIDE_P2	control_ddrse_ptv_west_side_p2 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_p2	RW	0
9	DDRSE_PTV_WEST_SIDE_P1	control_ddrse_ptv_west_side_p1 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_p1	RW	0
8	DDRSE_PTV_WEST_SIDE_P0	control_ddrse_ptv_west_side_p0 Note that reset is exported. Its value is = pi_ddrse_ptv_west_side_p0	RW	0
7:0	RESERVED		R	0x00

Table 18-972. Register Call Summary for Register CONTROL_EFUSE_4

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-973. CONTROL_EFUSE_5

Address Offset	0x0000 05D8		
Physical Address	0x4AE0 CDD8 0x4AE0 CDD8	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 5. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMARTIO_PTV_NORTH_SIDE_1V2_N9	SMARTIO_PTV_NORTH_SIDE_1V2_N8	SMARTIO_PTV_NORTH_SIDE_1V2_N7	SMARTIO_PTV_NORTH_SIDE_1V2_N6	SMARTIO_PTV_NORTH_SIDE_1V2_N5	SMARTIO_PTV_NORTH_SIDE_1V2_N4	SMARTIO_PTV_NORTH_SIDE_1V2_N3	SMARTIO_PTV_NORTH_SIDE_1V2_N2	SMARTIO_PTV_NORTH_SIDE_1V2_N1	SMARTIO_PTV_NORTH_SIDE_1V2_N0	SMARTIO_PTV_NORTH_SIDE_1V2_P9	SMARTIO_PTV_NORTH_SIDE_1V2_P8	SMARTIO_PTV_NORTH_SIDE_1V2_P7	SMARTIO_PTV_NORTH_SIDE_1V2_P6	SMARTIO_PTV_NORTH_SIDE_1V2_P5	SMARTIO_PTV_NORTH_SIDE_1V2_P4	SMARTIO_PTV_NORTH_SIDE_1V2_P3	SMARTIO_PTV_NORTH_SIDE_1V2_P2	SMARTIO_PTV_NORTH_SIDE_1V2_P1	SMARTIO_PTV_NORTH_SIDE_1V2_P0	RESERVED									

Bits	Field Name	Description	Type	Reset
31	SMARTIO_PTV_NORTH_SIDE_1V2_N9	control_smartio_ptv_north_side_1v2_n9 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n9	RW	0
30	SMARTIO_PTV_NORTH_SIDE_1V2_N8	control_smartio_ptv_north_side_1v2_n8 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n8	RW	0
29	SMARTIO_PTV_NORTH_SIDE_1V2_N7	control_smartio_ptv_north_side_1v2_n7 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n7	RW	0
28	SMARTIO_PTV_NORTH_SIDE_1V2_N6	control_smartio_ptv_north_side_1v2_n6 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n6	RW	0
27	SMARTIO_PTV_NORTH_SIDE_1V2_N5	control_smartio_ptv_north_side_1v2_n5 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n5	RW	0
26	SMARTIO_PTV_NORTH_SIDE_1V2_N4	control_smartio_ptv_north_side_1v2_n4 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n4	RW	0
25	SMARTIO_PTV_NORTH_SIDE_1V2_N3	control_smartio_ptv_north_side_1v2_n3 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n3	RW	0
24	SMARTIO_PTV_NORTH_SIDE_1V2_N2	control_smartio_ptv_north_side_1v2_n2 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n2	RW	0
23	SMARTIO_PTV_NORTH_SIDE_1V2_N1	control_smartio_ptv_north_side_1v2_n1 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n1	RW	0
22	SMARTIO_PTV_NORTH_SIDE_1V2_N0	control_smartio_ptv_north_side_1v2_n0 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_n0	RW	0
21	SMARTIO_PTV_NORTH_SIDE_1V2_P9	control_smartio_ptv_north_side_1v2_p9 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p9	RW	0
20	SMARTIO_PTV_NORTH_SIDE_1V2_P8	control_smartio_ptv_north_side_1v2_p8 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p8	RW	0
19	SMARTIO_PTV_NORTH_SIDE_1V2_P7	control_smartio_ptv_north_side_1v2_p7 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p7	RW	0
18	SMARTIO_PTV_NORTH_SIDE_1V2_P6	control_smartio_ptv_north_side_1v2_p6 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p6	RW	0
17	SMARTIO_PTV_NORTH_SIDE_1V2_P5	control_smartio_ptv_north_side_1v2_p5 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p5	RW	0

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Bits	Field Name	Description	Type	Reset
16	SMARTIO_PTV_NORTH_SIDE_1V2_P4	control_smartio_ptv_north_side_1v2_p4 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p4	RW	0
15	SMARTIO_PTV_NORTH_SIDE_1V2_P3	control_smartio_ptv_north_side_1v2_p3 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p3	RW	0
14	SMARTIO_PTV_NORTH_SIDE_1V2_P2	control_smartio_ptv_north_side_1v2_p2 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p2	RW	0
13	SMARTIO_PTV_NORTH_SIDE_1V2_P1	control_smartio_ptv_north_side_1v2_p1 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p1	RW	0
12	SMARTIO_PTV_NORTH_SIDE_1V2_P0	control_smartio_ptv_north_side_1v2_p0 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v2_p0	RW	0
11:0	RESERVED		R	0x000

Table 18-974. Register Call Summary for Register CONTROL_EFUSE_5

Control Module Register Manual

- CTRL_MODULE_WKUP Register Summary: [0]

Table 18-975. CONTROL_EFUSE_6

Address Offset	0x0000 05DC		
Physical Address	0x4AE0 CDDC 0x4AE0 CDDC	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 6. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMARTIO_PTV_EAST_SIDE_1V2_N9	SMARTIO_PTV_EAST_SIDE_1V2_N8	SMARTIO_PTV_EAST_SIDE_1V2_N7	SMARTIO_PTV_EAST_SIDE_1V2_N6	SMARTIO_PTV_EAST_SIDE_1V2_N5	SMARTIO_PTV_EAST_SIDE_1V2_N4	SMARTIO_PTV_EAST_SIDE_1V2_N3	SMARTIO_PTV_EAST_SIDE_1V2_N2	SMARTIO_PTV_EAST_SIDE_1V2_N1	SMARTIO_PTV_EAST_SIDE_1V2_N0	SMARTIO_PTV_EAST_SIDE_1V2_P9	SMARTIO_PTV_EAST_SIDE_1V2_P8	SMARTIO_PTV_EAST_SIDE_1V2_P7	SMARTIO_PTV_EAST_SIDE_1V2_P6	SMARTIO_PTV_EAST_SIDE_1V2_P5	SMARTIO_PTV_EAST_SIDE_1V2_P4	SMARTIO_PTV_EAST_SIDE_1V2_P3	SMARTIO_PTV_EAST_SIDE_1V2_P2	SMARTIO_PTV_EAST_SIDE_1V2_P1	SMARTIO_PTV_EAST_SIDE_1V2_P0	RESERVED									

Bits	Field Name	Description	Type	Reset
31	SMARTIO_PTV_EAST_SIDE_1V2_N9	control_smartio_ptv_east_side_1v2_n9 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n9	RW	0
30	SMARTIO_PTV_EAST_SIDE_1V2_N8	control_smartio_ptv_east_side_1v2_n8 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n8	RW	0
29	SMARTIO_PTV_EAST_SIDE_1V2_N7	control_smartio_ptv_east_side_1v2_n7 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n7	RW	0

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Bits	Field Name	Description	Type	Reset
28	SMARTIO_PTV_EAST_SIDE_1V2_N6	control_smartio_ptv_east_side_1v2_n6 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n6	RW	0
27	SMARTIO_PTV_EAST_SIDE_1V2_N5	control_smartio_ptv_east_side_1v2_n5 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n5	RW	0
26	SMARTIO_PTV_EAST_SIDE_1V2_N4	control_smartio_ptv_east_side_1v2_n4 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n4	RW	0
25	SMARTIO_PTV_EAST_SIDE_1V2_N3	control_smartio_ptv_east_side_1v2_n3 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n3	RW	0
24	SMARTIO_PTV_EAST_SIDE_1V2_N2	control_smartio_ptv_east_side_1v2_n2 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n2	RW	0
23	SMARTIO_PTV_EAST_SIDE_1V2_N1	control_smartio_ptv_east_side_1v2_n1 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n1	RW	0
22	SMARTIO_PTV_EAST_SIDE_1V2_N0	control_smartio_ptv_east_side_1v2_n0 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_n0	RW	0
21	SMARTIO_PTV_EAST_SIDE_1V2_P9	control_smartio_ptv_east_side_1v2_p9 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p9	RW	0
20	SMARTIO_PTV_EAST_SIDE_1V2_P8	control_smartio_ptv_east_side_1v2_p8 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p8	RW	0
19	SMARTIO_PTV_EAST_SIDE_1V2_P7	control_smartio_ptv_east_side_1v2_p7 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p7	RW	0
18	SMARTIO_PTV_EAST_SIDE_1V2_P6	control_smartio_ptv_east_side_1v2_p6 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p6	RW	0
17	SMARTIO_PTV_EAST_SIDE_1V2_P5	control_smartio_ptv_east_side_1v2_p5 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p5	RW	0
16	SMARTIO_PTV_EAST_SIDE_1V2_P4	control_smartio_ptv_east_side_1v2_p4 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p4	RW	0
15	SMARTIO_PTV_EAST_SIDE_1V2_P3	control_smartio_ptv_east_side_1v2_p3 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p3	RW	0
14	SMARTIO_PTV_EAST_SIDE_1V2_P2	control_smartio_ptv_east_side_1v2_p2 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p2	RW	0
13	SMARTIO_PTV_EAST_SIDE_1V2_P1	control_smartio_ptv_east_side_1v2_p1 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p1	RW	0
12	SMARTIO_PTV_EAST_SIDE_1V2_P0	control_smartio_ptv_east_side_1v2_p0 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v2_p0	RW	0
11:0	RESERVED		R	0x000

Table 18-976. Register Call Summary for Register CONTROL_EFUSE_6

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

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Table 18-977. CONTROL_EFUSE_7

Address Offset	0x0000 05E0
Physical Address	0x4AE0 CDE0 **Instance** CTRL_MODULE_WKUP 0x4AE0 CDE0 CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 7. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMARTIO_PTV_SOUTH_SIDE_1V2_N9	SMARTIO_PTV_SOUTH_SIDE_1V2_N8	SMARTIO_PTV_SOUTH_SIDE_1V2_N7	SMARTIO_PTV_SOUTH_SIDE_1V2_N6	SMARTIO_PTV_SOUTH_SIDE_1V2_N5	SMARTIO_PTV_SOUTH_SIDE_1V2_N4	SMARTIO_PTV_SOUTH_SIDE_1V2_N3	SMARTIO_PTV_SOUTH_SIDE_1V2_N2	SMARTIO_PTV_SOUTH_SIDE_1V2_N1	SMARTIO_PTV_SOUTH_SIDE_1V2_N0	SMARTIO_PTV_SOUTH_SIDE_1V2_P9	SMARTIO_PTV_SOUTH_SIDE_1V2_P8	SMARTIO_PTV_SOUTH_SIDE_1V2_P7	SMARTIO_PTV_SOUTH_SIDE_1V2_P6	SMARTIO_PTV_SOUTH_SIDE_1V2_P5	SMARTIO_PTV_SOUTH_SIDE_1V2_P4	SMARTIO_PTV_SOUTH_SIDE_1V2_P3	SMARTIO_PTV_SOUTH_SIDE_1V2_P2	SMARTIO_PTV_SOUTH_SIDE_1V2_P1	SMARTIO_PTV_SOUTH_SIDE_1V2_P0	RESERVED									

Bits	Field Name	Description	Type	Reset
31	SMARTIO_PTV_SOUTH_SIDE_1V2_N9	control_smartio_ptv_south_side_1v2_n9 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n9	RW	0
30	SMARTIO_PTV_SOUTH_SIDE_1V2_N8	control_smartio_ptv_south_side_1v2_n8 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n8	RW	0
29	SMARTIO_PTV_SOUTH_SIDE_1V2_N7	control_smartio_ptv_south_side_1v2_n7 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n7	RW	0
28	SMARTIO_PTV_SOUTH_SIDE_1V2_N6	control_smartio_ptv_south_side_1v2_n6 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n6	RW	0
27	SMARTIO_PTV_SOUTH_SIDE_1V2_N5	control_smartio_ptv_south_side_1v2_n5 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n5	RW	0
26	SMARTIO_PTV_SOUTH_SIDE_1V2_N4	control_smartio_ptv_south_side_1v2_n4 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n4	RW	0
25	SMARTIO_PTV_SOUTH_SIDE_1V2_N3	control_smartio_ptv_south_side_1v2_n3 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n3	RW	0
24	SMARTIO_PTV_SOUTH_SIDE_1V2_N2	control_smartio_ptv_south_side_1v2_n2 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n2	RW	0
23	SMARTIO_PTV_SOUTH_SIDE_1V2_N1	control_smartio_ptv_south_side_1v2_n1 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n1	RW	0
22	SMARTIO_PTV_SOUTH_SIDE_1V2_N0	control_smartio_ptv_south_side_1v2_n0 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_n0	RW	0
21	SMARTIO_PTV_SOUTH_SIDE_1V2_P9	control_smartio_ptv_south_side_1v2_p9 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p9	RW	0

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Bits	Field Name	Description	Type	Reset
20	SMARTIO_PTV_SOUTH_SIDE_1V2_P8	control_smartio_ptv_south_side_1v2_p8 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p8	RW	0
19	SMARTIO_PTV_SOUTH_SIDE_1V2_P7	control_smartio_ptv_south_side_1v2_p7 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p7	RW	0
18	SMARTIO_PTV_SOUTH_SIDE_1V2_P6	control_smartio_ptv_south_side_1v2_p6 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p6	RW	0
17	SMARTIO_PTV_SOUTH_SIDE_1V2_P5	control_smartio_ptv_south_side_1v2_p5 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p5	RW	0
16	SMARTIO_PTV_SOUTH_SIDE_1V2_P4	control_smartio_ptv_south_side_1v2_p4 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p4	RW	0
15	SMARTIO_PTV_SOUTH_SIDE_1V2_P3	control_smartio_ptv_south_side_1v2_p3 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p3	RW	0
14	SMARTIO_PTV_SOUTH_SIDE_1V2_P2	control_smartio_ptv_south_side_1v2_p2 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p2	RW	0
13	SMARTIO_PTV_SOUTH_SIDE_1V2_P1	control_smartio_ptv_south_side_1v2_p1 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p1	RW	0
12	SMARTIO_PTV_SOUTH_SIDE_1V2_P0	control_smartio_ptv_south_side_1v2_p0 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v2_p0	RW	0
11:0	RESERVED		R	0x000

Table 18-978. Register Call Summary for Register CONTROL_EFUSE_7

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-979. CONTROL_EFUSE_8

Address Offset	0x0000 05E4		
Physical Address	0x4AE0 CDE4 0x4AE0 CDE4	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 8. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMARTIO_PTV_WEST_SIDE_1V2_N9	SMARTIO_PTV_WEST_SIDE_1V2_N8	SMARTIO_PTV_WEST_SIDE_1V2_N7	SMARTIO_PTV_WEST_SIDE_1V2_N6	SMARTIO_PTV_WEST_SIDE_1V2_N5	SMARTIO_PTV_WEST_SIDE_1V2_N4	SMARTIO_PTV_WEST_SIDE_1V2_N3	SMARTIO_PTV_WEST_SIDE_1V2_N2	SMARTIO_PTV_WEST_SIDE_1V2_N1	SMARTIO_PTV_WEST_SIDE_1V2_N0	SMARTIO_PTV_WEST_SIDE_1V2_P9	SMARTIO_PTV_WEST_SIDE_1V2_P8	SMARTIO_PTV_WEST_SIDE_1V2_P7	SMARTIO_PTV_WEST_SIDE_1V2_P6	SMARTIO_PTV_WEST_SIDE_1V2_P5	SMARTIO_PTV_WEST_SIDE_1V2_P4	SMARTIO_PTV_WEST_SIDE_1V2_P3	SMARTIO_PTV_WEST_SIDE_1V2_P2	SMARTIO_PTV_WEST_SIDE_1V2_P1	SMARTIO_PTV_WEST_SIDE_1V2_P0	RESERVED										

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Bits	Field Name	Description	Type	Reset
31	SMARTIO_PTV_WEST_SIDE_1V2_N9	control_smartio_ptv_west_side_1v2_n9 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n9	RW	0
30	SMARTIO_PTV_WEST_SIDE_1V2_N8	control_smartio_ptv_west_side_1v2_n8 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n8	RW	0
29	SMARTIO_PTV_WEST_SIDE_1V2_N7	control_smartio_ptv_west_side_1v2_n7 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n7	RW	0
28	SMARTIO_PTV_WEST_SIDE_1V2_N6	control_smartio_ptv_west_side_1v2_n6 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n6	RW	0
27	SMARTIO_PTV_WEST_SIDE_1V2_N5	control_smartio_ptv_west_side_1v2_n5 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n5	RW	0
26	SMARTIO_PTV_WEST_SIDE_1V2_N4	control_smartio_ptv_west_side_1v2_n4 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n4	RW	0
25	SMARTIO_PTV_WEST_SIDE_1V2_N3	control_smartio_ptv_west_side_1v2_n3 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n3	RW	0
24	SMARTIO_PTV_WEST_SIDE_1V2_N2	control_smartio_ptv_west_side_1v2_n2 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n2	RW	0
23	SMARTIO_PTV_WEST_SIDE_1V2_N1	control_smartio_ptv_west_side_1v2_n1 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n1	RW	0
22	SMARTIO_PTV_WEST_SIDE_1V2_N0	control_smartio_ptv_west_side_1v2_n0 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_n0	RW	0
21	SMARTIO_PTV_WEST_SIDE_1V2_P9	control_smartio_ptv_west_side_1v2_p9 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p9	RW	0
20	SMARTIO_PTV_WEST_SIDE_1V2_P8	control_smartio_ptv_west_side_1v2_p8 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p8	RW	0
19	SMARTIO_PTV_WEST_SIDE_1V2_P7	control_smartio_ptv_west_side_1v2_p7 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p7	RW	0
18	SMARTIO_PTV_WEST_SIDE_1V2_P6	control_smartio_ptv_west_side_1v2_p6 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p6	RW	0
17	SMARTIO_PTV_WEST_SIDE_1V2_P5	control_smartio_ptv_west_side_1v2_p5 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p5	RW	0
16	SMARTIO_PTV_WEST_SIDE_1V2_P4	control_smartio_ptv_west_side_1v2_p4 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p4	RW	0
15	SMARTIO_PTV_WEST_SIDE_1V2_P3	control_smartio_ptv_west_side_1v2_p3 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p3	RW	0
14	SMARTIO_PTV_WEST_SIDE_1V2_P2	control_smartio_ptv_west_side_1v2_p2 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p2	RW	0
13	SMARTIO_PTV_WEST_SIDE_1V2_P1	control_smartio_ptv_west_side_1v2_p1 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p1	RW	0
12	SMARTIO_PTV_WEST_SIDE_1V2_P0	control_smartio_ptv_west_side_1v2_p0 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v2_p0	RW	0
11:0	RESERVED		R	0x000

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Table 18-980. Register Call Summary for Register CONTROL_EFUSE_8

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-981. CONTROL_EFUSE_9

Address Offset	0x0000 05E8		
Physical Address	0x4AE0 CDE8 0x4AE0 CDE8	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 9. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMARTIO_PTV_NORTH_SIDE_1V8_N9	SMARTIO_PTV_NORTH_SIDE_1V8_N8	SMARTIO_PTV_NORTH_SIDE_1V8_N7	SMARTIO_PTV_NORTH_SIDE_1V8_N6	SMARTIO_PTV_NORTH_SIDE_1V8_N5	SMARTIO_PTV_NORTH_SIDE_1V8_N4	SMARTIO_PTV_NORTH_SIDE_1V8_N3	SMARTIO_PTV_NORTH_SIDE_1V8_N2	SMARTIO_PTV_NORTH_SIDE_1V8_N1	SMARTIO_PTV_NORTH_SIDE_1V8_N0	SMARTIO_PTV_NORTH_SIDE_1V8_P9	SMARTIO_PTV_NORTH_SIDE_1V8_P8	SMARTIO_PTV_NORTH_SIDE_1V8_P7	SMARTIO_PTV_NORTH_SIDE_1V8_P6	SMARTIO_PTV_NORTH_SIDE_1V8_P5	SMARTIO_PTV_NORTH_SIDE_1V8_P4	SMARTIO_PTV_NORTH_SIDE_1V8_P3	SMARTIO_PTV_NORTH_SIDE_1V8_P2	SMARTIO_PTV_NORTH_SIDE_1V8_P1	SMARTIO_PTV_NORTH_SIDE_1V8_P0	RESERVED									

Bits	Field Name	Description	Type	Reset
31	SMARTIO_PTV_NORTH_SIDE_1V8_N9	control_smartio_ptv_north_side_1v8_n9 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n9	RW	0
30	SMARTIO_PTV_NORTH_SIDE_1V8_N8	control_smartio_ptv_north_side_1v8_n8 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n8	RW	0
29	SMARTIO_PTV_NORTH_SIDE_1V8_N7	control_smartio_ptv_north_side_1v8_n7 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n7	RW	0
28	SMARTIO_PTV_NORTH_SIDE_1V8_N6	control_smartio_ptv_north_side_1v8_n6 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n6	RW	0
27	SMARTIO_PTV_NORTH_SIDE_1V8_N5	control_smartio_ptv_north_side_1v8_n5 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n5	RW	0
26	SMARTIO_PTV_NORTH_SIDE_1V8_N4	control_smartio_ptv_north_side_1v8_n4 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n4	RW	0
25	SMARTIO_PTV_NORTH_SIDE_1V8_N3	control_smartio_ptv_north_side_1v8_n3 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n3	RW	0
24	SMARTIO_PTV_NORTH_SIDE_1V8_N2	control_smartio_ptv_north_side_1v8_n2 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n2	RW	0
23	SMARTIO_PTV_NORTH_SIDE_1V8_N1	control_smartio_ptv_north_side_1v8_n1 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n1	RW	0

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Bits	Field Name	Description	Type	Reset
22	SMARTIO_PTV_NORTH_SIDE_1V8_N0	control_smartio_ptv_north_side_1v8_n0 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_n0	RW	0
21	SMARTIO_PTV_NORTH_SIDE_1V8_P9	control_smartio_ptv_north_side_1v8_p9 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p9	RW	0
20	SMARTIO_PTV_NORTH_SIDE_1V8_P8	control_smartio_ptv_north_side_1v8_p8 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p8	RW	0
19	SMARTIO_PTV_NORTH_SIDE_1V8_P7	control_smartio_ptv_north_side_1v8_p7 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p7	RW	0
18	SMARTIO_PTV_NORTH_SIDE_1V8_P6	control_smartio_ptv_north_side_1v8_p6 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p6	RW	0
17	SMARTIO_PTV_NORTH_SIDE_1V8_P5	control_smartio_ptv_north_side_1v8_p5 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p5	RW	0
16	SMARTIO_PTV_NORTH_SIDE_1V8_P4	control_smartio_ptv_north_side_1v8_p4 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p4	RW	0
15	SMARTIO_PTV_NORTH_SIDE_1V8_P3	control_smartio_ptv_north_side_1v8_p3 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p3	RW	0
14	SMARTIO_PTV_NORTH_SIDE_1V8_P2	control_smartio_ptv_north_side_1v8_p2 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p2	RW	0
13	SMARTIO_PTV_NORTH_SIDE_1V8_P1	control_smartio_ptv_north_side_1v8_p1 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p1	RW	0
12	SMARTIO_PTV_NORTH_SIDE_1V8_P0	control_smartio_ptv_north_side_1v8_p0 Note that reset is exported. Its value is = pi_smartio_ptv_north_side_1v8_p0	RW	0
11:0	RESERVED		R	0x000

Table 18-982. Register Call Summary for Register CONTROL_EFUSE_9

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-983. CONTROL_EFUSE_10

Address Offset	0x0000 05EC		
Physical Address	0x4AE0 CDEC 0x4AE0 CDEC	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 10. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMARTIO_PTV_EAST_SIDE_1V8_N9	SMARTIO_PTV_EAST_SIDE_1V8_N8	SMARTIO_PTV_EAST_SIDE_1V8_N7	SMARTIO_PTV_EAST_SIDE_1V8_N6	SMARTIO_PTV_EAST_SIDE_1V8_N5	SMARTIO_PTV_EAST_SIDE_1V8_N4	SMARTIO_PTV_EAST_SIDE_1V8_N3	SMARTIO_PTV_EAST_SIDE_1V8_N2	SMARTIO_PTV_EAST_SIDE_1V8_N1	SMARTIO_PTV_EAST_SIDE_1V8_N0	SMARTIO_PTV_EAST_SIDE_1V8_P9	SMARTIO_PTV_EAST_SIDE_1V8_P8	SMARTIO_PTV_EAST_SIDE_1V8_P7	SMARTIO_PTV_EAST_SIDE_1V8_P6	SMARTIO_PTV_EAST_SIDE_1V8_P5	SMARTIO_PTV_EAST_SIDE_1V8_P4	SMARTIO_PTV_EAST_SIDE_1V8_P3	SMARTIO_PTV_EAST_SIDE_1V8_P2	SMARTIO_PTV_EAST_SIDE_1V8_P1	SMARTIO_PTV_EAST_SIDE_1V8_P0	RESERVED										

Bits	Field Name	Description	Type	Reset
31	SMARTIO_PTV_EAST_SIDE_1V8_N9	control_smartio_ptv_east_side_1v8_n9 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n9	RW	0
30	SMARTIO_PTV_EAST_SIDE_1V8_N8	control_smartio_ptv_east_side_1v8_n8 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n8	RW	0
29	SMARTIO_PTV_EAST_SIDE_1V8_N7	control_smartio_ptv_east_side_1v8_n7 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n7	RW	0
28	SMARTIO_PTV_EAST_SIDE_1V8_N6	control_smartio_ptv_east_side_1v8_n6 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n6	RW	0
27	SMARTIO_PTV_EAST_SIDE_1V8_N5	control_smartio_ptv_east_side_1v8_n5 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n5	RW	0
26	SMARTIO_PTV_EAST_SIDE_1V8_N4	control_smartio_ptv_east_side_1v8_n4 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n4	RW	0
25	SMARTIO_PTV_EAST_SIDE_1V8_N3	control_smartio_ptv_east_side_1v8_n3 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n3	RW	0
24	SMARTIO_PTV_EAST_SIDE_1V8_N2	control_smartio_ptv_east_side_1v8_n2 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n2	RW	0
23	SMARTIO_PTV_EAST_SIDE_1V8_N1	control_smartio_ptv_east_side_1v8_n1 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n1	RW	0
22	SMARTIO_PTV_EAST_SIDE_1V8_N0	control_smartio_ptv_east_side_1v8_n0 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_n0	RW	0
21	SMARTIO_PTV_EAST_SIDE_1V8_P9	control_smartio_ptv_east_side_1v8_p9 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p9	RW	0
20	SMARTIO_PTV_EAST_SIDE_1V8_P8	control_smartio_ptv_east_side_1v8_p8 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p8	RW	0
19	SMARTIO_PTV_EAST_SIDE_1V8_P7	control_smartio_ptv_east_side_1v8_p7 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p7	RW	0
18	SMARTIO_PTV_EAST_SIDE_1V8_P6	control_smartio_ptv_east_side_1v8_p6 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p6	RW	0
17	SMARTIO_PTV_EAST_SIDE_1V8_P5	control_smartio_ptv_east_side_1v8_p5 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p5	RW	0

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Bits	Field Name	Description	Type	Reset
16	SMARTIO_PTV_EAST_SIDE_1V8_P4	control_smartio_ptv_east_side_1v8_p4 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p4	RW	0
15	SMARTIO_PTV_EAST_SIDE_1V8_P3	control_smartio_ptv_east_side_1v8_p3 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p3	RW	0
14	SMARTIO_PTV_EAST_SIDE_1V8_P2	control_smartio_ptv_east_side_1v8_p2 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p2	RW	0
13	SMARTIO_PTV_EAST_SIDE_1V8_P1	control_smartio_ptv_east_side_1v8_p1 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p1	RW	0
12	SMARTIO_PTV_EAST_SIDE_1V8_P0	control_smartio_ptv_east_side_1v8_p0 Note that reset is exported. Its value is = pi_smartio_ptv_east_side_1v8_p0	RW	0
11:0	RESERVED		R	0x000

Table 18-984. Register Call Summary for Register CONTROL_EFUSE_10

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- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-985. EFUSE_11

Address Offset	0x0000 05F0
Physical Address	Please refer to Table 18-909 **Instance** CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 11. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMARTIO_PTV_SOUTH_SIDE_1V8_N9	SMARTIO_PTV_SOUTH_SIDE_1V8_N8	SMARTIO_PTV_SOUTH_SIDE_1V8_N7	SMARTIO_PTV_SOUTH_SIDE_1V8_N6	SMARTIO_PTV_SOUTH_SIDE_1V8_N5	SMARTIO_PTV_SOUTH_SIDE_1V8_N4	SMARTIO_PTV_SOUTH_SIDE_1V8_N3	SMARTIO_PTV_SOUTH_SIDE_1V8_N2	SMARTIO_PTV_SOUTH_SIDE_1V8_N1	SMARTIO_PTV_SOUTH_SIDE_1V8_N0	SMARTIO_PTV_SOUTH_SIDE_1V8_P9	SMARTIO_PTV_SOUTH_SIDE_1V8_P8	SMARTIO_PTV_SOUTH_SIDE_1V8_P7	SMARTIO_PTV_SOUTH_SIDE_1V8_P6	SMARTIO_PTV_SOUTH_SIDE_1V8_P5	SMARTIO_PTV_SOUTH_SIDE_1V8_P4	SMARTIO_PTV_SOUTH_SIDE_1V8_P3	SMARTIO_PTV_SOUTH_SIDE_1V8_P2	SMARTIO_PTV_SOUTH_SIDE_1V8_P1	SMARTIO_PTV_SOUTH_SIDE_1V8_P0	RESERVED								

Bits	Field Name	Description	Type	Reset
31	SMARTIO_PTV_SOUTH_SIDE_1V8_N9	control_smartio_ptv_south_side_1v8_n9 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n9	RW	0
30	SMARTIO_PTV_SOUTH_SIDE_1V8_N8	control_smartio_ptv_south_side_1v8_n8 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n8	RW	0
29	SMARTIO_PTV_SOUTH_SIDE_1V8_N7	control_smartio_ptv_south_side_1v8_n7 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n7	RW	0

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Bits	Field Name	Description	Type	Reset
28	SMARTIO_PTV_SOUTH_SIDE_1V8_N6	control_smartio_ptv_south_side_1v8_n6 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n6	RW	0
27	SMARTIO_PTV_SOUTH_SIDE_1V8_N5	control_smartio_ptv_south_side_1v8_n5 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n5	RW	0
26	SMARTIO_PTV_SOUTH_SIDE_1V8_N4	control_smartio_ptv_south_side_1v8_n4 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n4	RW	0
25	SMARTIO_PTV_SOUTH_SIDE_1V8_N3	control_smartio_ptv_south_side_1v8_n3 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n3	RW	0
24	SMARTIO_PTV_SOUTH_SIDE_1V8_N2	control_smartio_ptv_south_side_1v8_n2 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n2	RW	0
23	SMARTIO_PTV_SOUTH_SIDE_1V8_N1	control_smartio_ptv_south_side_1v8_n1 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n1	RW	0
22	SMARTIO_PTV_SOUTH_SIDE_1V8_N0	control_smartio_ptv_south_side_1v8_n0 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_n0	RW	0
21	SMARTIO_PTV_SOUTH_SIDE_1V8_P9	control_smartio_ptv_south_side_1v8_p9 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p9	RW	0
20	SMARTIO_PTV_SOUTH_SIDE_1V8_P8	control_smartio_ptv_south_side_1v8_p8 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p8	RW	0
19	SMARTIO_PTV_SOUTH_SIDE_1V8_P7	control_smartio_ptv_south_side_1v8_p7 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p7	RW	0
18	SMARTIO_PTV_SOUTH_SIDE_1V8_P6	control_smartio_ptv_south_side_1v8_p6 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p6	RW	0
17	SMARTIO_PTV_SOUTH_SIDE_1V8_P5	control_smartio_ptv_south_side_1v8_p5 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p5	RW	0
16	SMARTIO_PTV_SOUTH_SIDE_1V8_P4	control_smartio_ptv_south_side_1v8_p4 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p4	RW	0
15	SMARTIO_PTV_SOUTH_SIDE_1V8_P3	control_smartio_ptv_south_side_1v8_p3 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p3	RW	0
14	SMARTIO_PTV_SOUTH_SIDE_1V8_P2	control_smartio_ptv_south_side_1v8_p2 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p2	RW	0
13	SMARTIO_PTV_SOUTH_SIDE_1V8_P1	control_smartio_ptv_south_side_1v8_p1 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p1	RW	0
12	SMARTIO_PTV_SOUTH_SIDE_1V8_P0	control_smartio_ptv_south_side_1v8_p0 Note that reset is exported. Its value is = pi_smartio_ptv_south_side_1v8_p0	RW	0
11:0	RESERVED		R	0x000

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Table 18-986. CONTROL_EFUSE_12

Address Offset	0x0000 05F4		
Physical Address	0x4AE0 CDF4 0x4AE0 CDF4	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 12. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMARTIO_PTV_WEST_SIDE_1V8_N9	SMARTIO_PTV_WEST_SIDE_1V8_N8	SMARTIO_PTV_WEST_SIDE_1V8_N7	SMARTIO_PTV_WEST_SIDE_1V8_N6	SMARTIO_PTV_WEST_SIDE_1V8_N5	SMARTIO_PTV_WEST_SIDE_1V8_N4	SMARTIO_PTV_WEST_SIDE_1V8_N3	SMARTIO_PTV_WEST_SIDE_1V8_N2	SMARTIO_PTV_WEST_SIDE_1V8_N1	SMARTIO_PTV_WEST_SIDE_1V8_N0	SMARTIO_PTV_WEST_SIDE_1V8_P9	SMARTIO_PTV_WEST_SIDE_1V8_P8	SMARTIO_PTV_WEST_SIDE_1V8_P7	SMARTIO_PTV_WEST_SIDE_1V8_P6	SMARTIO_PTV_WEST_SIDE_1V8_P5	SMARTIO_PTV_WEST_SIDE_1V8_P4	SMARTIO_PTV_WEST_SIDE_1V8_P3	SMARTIO_PTV_WEST_SIDE_1V8_P2	SMARTIO_PTV_WEST_SIDE_1V8_P1	SMARTIO_PTV_WEST_SIDE_1V8_P0	RESERVED										

Bits	Field Name	Description	Type	Reset
31	SMARTIO_PTV_WEST_SIDE_1V8_N9	control_smartio_ptv_west_side_1v8_n9 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n9	RW	0
30	SMARTIO_PTV_WEST_SIDE_1V8_N8	control_smartio_ptv_west_side_1v8_n8 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n8	RW	0
29	SMARTIO_PTV_WEST_SIDE_1V8_N7	control_smartio_ptv_west_side_1v8_n7 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n7	RW	0
28	SMARTIO_PTV_WEST_SIDE_1V8_N6	control_smartio_ptv_west_side_1v8_n6 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n6	RW	0
27	SMARTIO_PTV_WEST_SIDE_1V8_N5	control_smartio_ptv_west_side_1v8_n5 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n5	RW	0
26	SMARTIO_PTV_WEST_SIDE_1V8_N4	control_smartio_ptv_west_side_1v8_n4 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n4	RW	0
25	SMARTIO_PTV_WEST_SIDE_1V8_N3	control_smartio_ptv_west_side_1v8_n3 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n3	RW	0
24	SMARTIO_PTV_WEST_SIDE_1V8_N2	control_smartio_ptv_west_side_1v8_n2 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n2	RW	0
23	SMARTIO_PTV_WEST_SIDE_1V8_N1	control_smartio_ptv_west_side_1v8_n1 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n1	RW	0
22	SMARTIO_PTV_WEST_SIDE_1V8_N0	control_smartio_ptv_west_side_1v8_n0 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_n0	RW	0
21	SMARTIO_PTV_WEST_SIDE_1V8_P9	control_smartio_ptv_west_side_1v8_p9 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p9	RW	0

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Bits	Field Name	Description	Type	Reset
20	SMARTIO_PTV_WEST_SIDE_1V8_P8	control_smartio_ptv_west_side_1v8_p8 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p8	RW	0
19	SMARTIO_PTV_WEST_SIDE_1V8_P7	control_smartio_ptv_west_side_1v8_p7 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p7	RW	0
18	SMARTIO_PTV_WEST_SIDE_1V8_P6	control_smartio_ptv_west_side_1v8_p6 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p6	RW	0
17	SMARTIO_PTV_WEST_SIDE_1V8_P5	control_smartio_ptv_west_side_1v8_p5 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p5	RW	0
16	SMARTIO_PTV_WEST_SIDE_1V8_P4	control_smartio_ptv_west_side_1v8_p4 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p4	RW	0
15	SMARTIO_PTV_WEST_SIDE_1V8_P3	control_smartio_ptv_west_side_1v8_p3 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p3	RW	0
14	SMARTIO_PTV_WEST_SIDE_1V8_P2	control_smartio_ptv_west_side_1v8_p2 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p2	RW	0
13	SMARTIO_PTV_WEST_SIDE_1V8_P1	control_smartio_ptv_west_side_1v8_p1 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p1	RW	0
12	SMARTIO_PTV_WEST_SIDE_1V8_P0	control_smartio_ptv_west_side_1v8_p0 Note that reset is exported. Its value is = pi_smartio_ptv_west_side_1v8_p0	RW	0
11:0	RESERVED		R	0x000

Table 18-987. Register Call Summary for Register CONTROL_EFUSE_12

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

Table 18-988. CONTROL_EFUSE_13

Address Offset	0x0000 05F8		
Physical Address	0x4AE0 CDF8 0x4AE0 CDF8	**Instance**	CTRL_MODULE_WKUP CTRL_MODULE_WKUP_PAD
Description	EFUSE compensation 13. Since reset value is exported, at the time of control module generation, reset value is not known. Using 0 as default Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDIO1833_PTV_N5	SDIO1833_PTV_N4	SDIO1833_PTV_N3	SDIO1833_PTV_N2	SDIO1833_PTV_N1	SDIO1833_PTV_N0	SDIO1833_PTV_P5	SDIO1833_PTV_P4	SDIO1833_PTV_P3	SDIO1833_PTV_P2	SDIO1833_PTV_P1	SDIO1833_PTV_P0	RESERVED																			

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Bits	Field Name	Description	Type	Reset
31	SDIO1833_PTV_N5	control_sdio1833_ptv_n5 Note that reset is exported. Its value is = pi_sdio1833_ptv_n5	RW	0
30	SDIO1833_PTV_N4	control_sdio1833_ptv_n4 Note that reset is exported. Its value is = pi_sdio1833_ptv_n4	RW	0
29	SDIO1833_PTV_N3	control_sdio1833_ptv_n3 Note that reset is exported. Its value is = pi_sdio1833_ptv_n3	RW	0
28	SDIO1833_PTV_N2	control_sdio1833_ptv_n2 Note that reset is exported. Its value is = pi_sdio1833_ptv_n2	RW	0
27	SDIO1833_PTV_N1	control_sdio1833_ptv_n1 Note that reset is exported. Its value is = pi_sdio1833_ptv_n1	RW	0
26	SDIO1833_PTV_N0	control_sdio1833_ptv_n0 Note that reset is exported. Its value is = pi_sdio1833_ptv_n0	RW	0
25	SDIO1833_PTV_P5	control_sdio1833_ptv_p5 Note that reset is exported. Its value is = pi_sdio1833_ptv_p5	RW	0
24	SDIO1833_PTV_P4	control_sdio1833_ptv_p4 Note that reset is exported. Its value is = pi_sdio1833_ptv_p4	RW	0
23	SDIO1833_PTV_P3	control_sdio1833_ptv_p3 Note that reset is exported. Its value is = pi_sdio1833_ptv_p3	RW	0
22	SDIO1833_PTV_P2	control_sdio1833_ptv_p2 Note that reset is exported. Its value is = pi_sdio1833_ptv_p2	RW	0
21	SDIO1833_PTV_P1	control_sdio1833_ptv_p1 Note that reset is exported. Its value is = pi_sdio1833_ptv_p1	RW	0
20	SDIO1833_PTV_P0	control_sdio1833_ptv_p0 Note that reset is exported. Its value is = pi_sdio1833_ptv_p0	RW	0
19:0	RESERVED		R	0x0 0000

Table 18-989. Register Call Summary for Register CONTROL_EFUSE_13

Control Module Register Manual

- CTRL_MODULE_WKUP_PAD Register Summary: [0]

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Mailbox

This chapter describes the mailbox module in the device.

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19.2 Mailbox Integration 4434
19.3 Mailbox Functional Description 4438
19.4 Mailbox Programming Guide 4444
19.5 Mailbox Register Manual 4447

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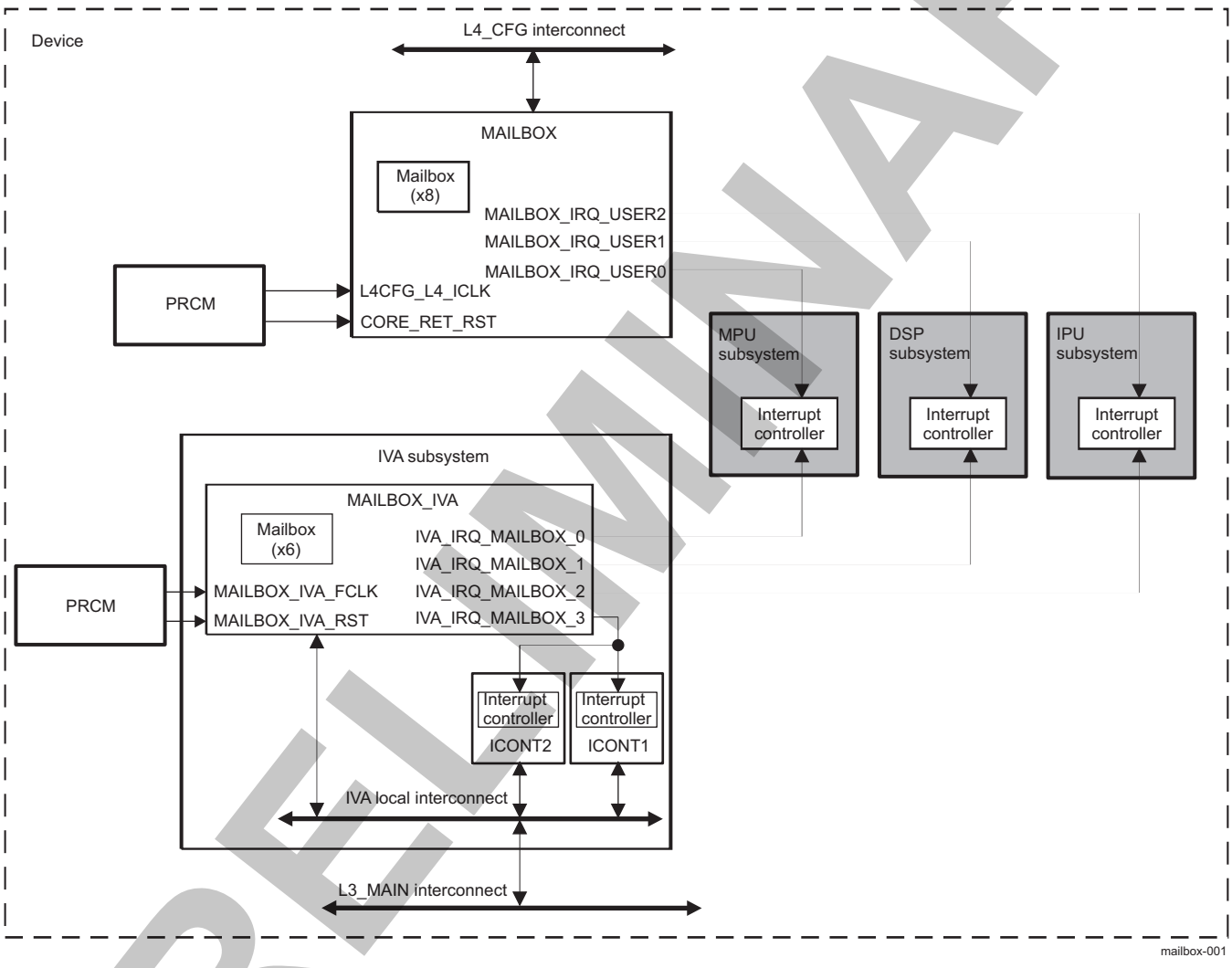
19.1 Mailbox Overview

Communication between the on-chip processors of the device uses a queued mailbox-interrupt mechanism.

The queued mailbox-interrupt mechanism allows the software to establish a communication channel between two processors through a set of registers and associated interrupt signals by sending and receiving messages (mailboxes).

Figure 19-1 shows an overview of the mailbox module.

Figure 19-1. Mailbox Overview



There are two mailbox module instances in the device:

- "System" mailbox (MAILBOX) - used for communication between microprocessor unit (MPU), digital signal processor (DSP), and image processing unit (IPU).
- IVA mailbox (MAILBOX_IVA) - used for communication between one internal to the IVA subsystem user (ICONT1, or ICONT2) and three external to the IVA subsystem users (MPU, DSP and IPU). This communication is insured through three pairs of mailboxes.

The mailbox module includes the following features:

- Three users for the MAILBOX instance (MPU, DSP, and IPU); four users for the MAILBOX_IVA instance (ICONT1/ICONT2, MPU, DSP and IPU)
- Eight mailbox message queues for the MAILBOX instance; six mailbox message queues for the MAILBOX_IVA instance

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- Flexible assignment of receiver and sender for each mailbox through interrupt configuration
- Four interrupts (one per user) for the MAILBOX instance; four interrupts (one per user) for the MAILBOX_IVA instance
- 32-bit message width
- Four-message FIFO depth for each message queue
- Message reception and queue-not-full notification using interrupts
- Support of 16-/32-bit addressing scheme
- Power management support

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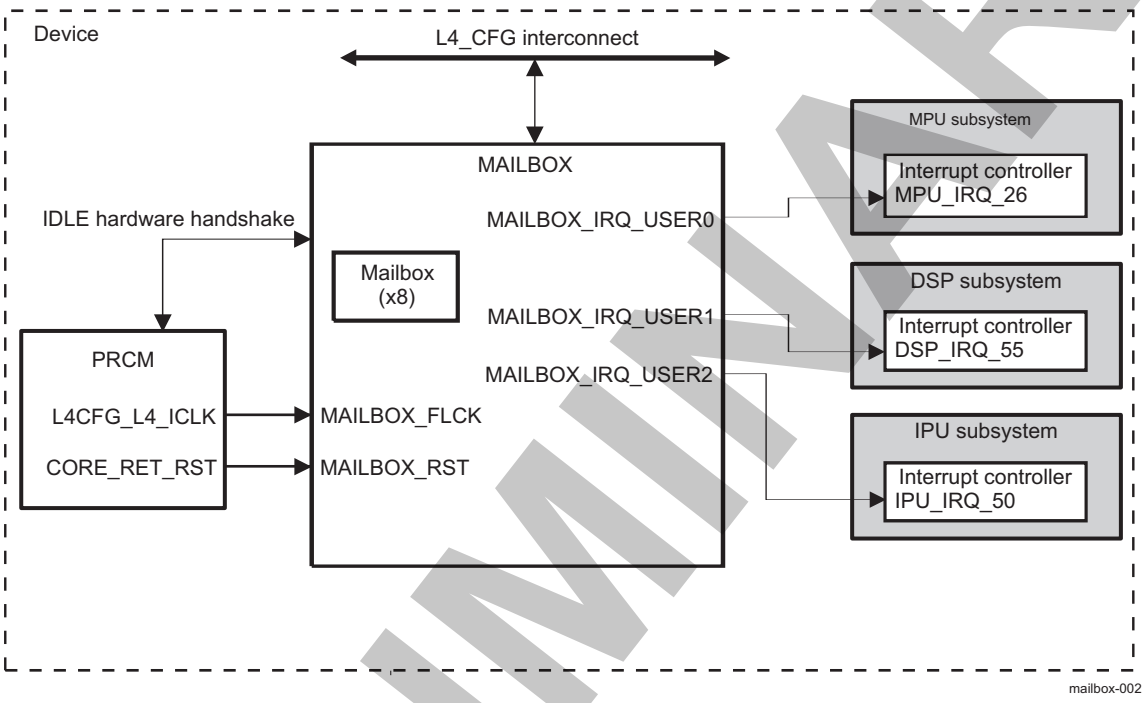
19.2 Mailbox Integration

This section describes the mailbox integration in the device, including information about clocks, resets, and hardware requests.

19.2.1 MAILBOX Integration

Figure 19-2 shows the MAILBOX integration.

Figure 19-2. MAILBOX Integration



NOTE: For more information about the IDLE hardware handshake, see Module-Level Clock Management, in Chapter 3, *Power, Reset, and Clock Management* chapter.

Table 19-1 through Table 19-3 summarize the MAILBOX integration in the device.

Table 19-1. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
MAILBOX	PD_CORE	NA	L4_CFG

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Table 19-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MAILBOX	MAILBOX_FCLK	L4CFG_L4_ICLK	PRCM	MAILBOX functional/interface clock. For information about PRCM clock gating and management, see CD_L4_CFG Clock Domain, in *Power, Reset, and Clock Management* chapter.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MAILBOX	MAILBOX_RST	CORE_RET_RST	PRCM	MAILBOX hardware reset. For information about PRCM reset sources and distribution, see Reset Domains, in *Power, Reset, and Clock Management* chapter.

Table 19-3. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MAILBOX	MAILBOX_IRQ_USER0	MPU_IRQ_26	MPU	MAILBOX user 0 interrupt request. For information about MPU interrupt mapping, see Interrupt Requests to INTC_MPU, in *Interrupt Controllers* chapter.
	MAILBOX_IRQ_USER1	DSP_IRQ_55	DSP	MAILBOX user 1 interrupt request. For information about DSP interrupt mapping, see Interrupt Requests, in *DSP Subsystem* chapter.
	MAILBOX_IRQ_USER2	IPU_IRQ_50	IPU	MAILBOX user 2 interrupt request. For information about IPU interrupt mapping, see Interrupt Requests to INTC_IPU, in *Interrupt Controllers* chapter.
No DMA Requests				

NOTE: For information about interrupt source description, see Section 19.3.4, *Interrupt Requests*.

19.2.2 MAILBOX_IVA Integration

Figure 19-3 shows the MAILBOX_IVA integration.

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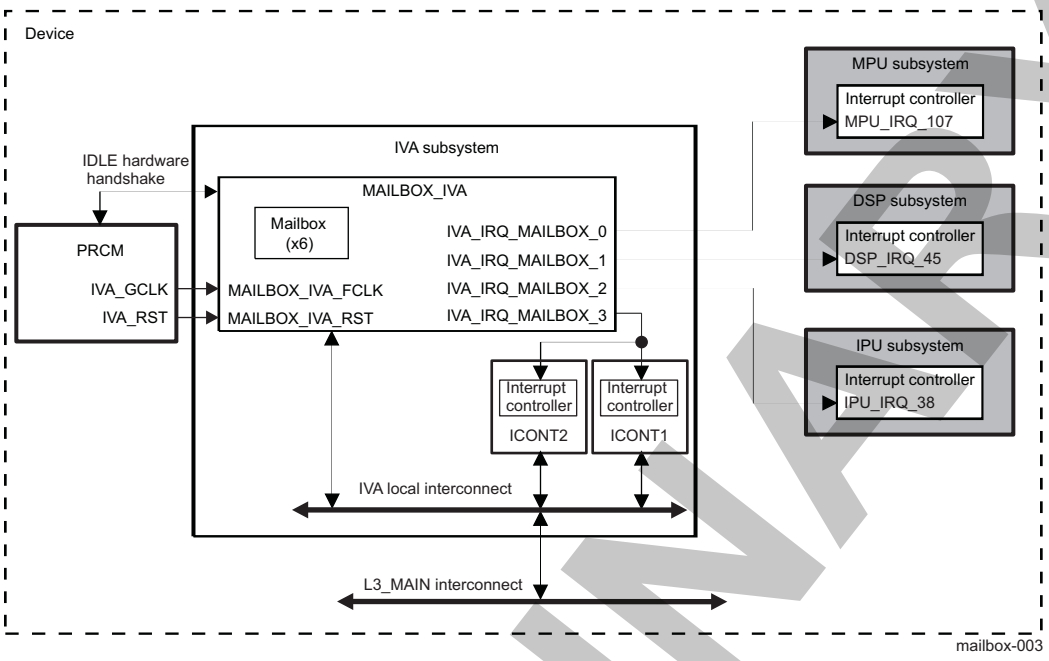
Figure 19-3. MAILBOX_IVA Integration



NOTE: For more information about the IDLE hardware handshake, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

NOTE: The two imaging controllers - ICONT1 and ICONT2, are mapped on a shared interrupt line. The choice between them is done by masking mailbox interrupt on ICONT1 or ICONT2.

Table 19-4 through Table 19-6 summarize the MAILBOX_IVA integration in the device.

Table 19-4. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
MAILBOX_IVA	PD_IVA	NA	IVA local interconnect

Table 19-5. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MAILBOX_IVA	MAILBOX_IVA_FCLK	IVA_GCLK	PRCM	MAILBOX_IVA functional/interface clock.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MAILBOX_IVA	MAILBOX_IVA_RST	IVA_RST	PRCM	MAILBOX_IVA hardware reset.

Table 19-6. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MAILBOX_IVA	IVA_IRQ_MAILBOX_0	MPU_IRQ_107	MPU	MAILBOX_IVA user 0 interrupt request

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Table 19-6. Hardware Requests (continued)

	IVA_IRQ_MAILBOX_1	DSP_IRQ_45	DSP	MAILBOX_IVA user 1 interrupt request
	IVA_IRQ_MAILBOX_2	IPU_IRQ_38	IPU	MAILBOX_IVA user 2 interrupt request
	IVA_IRQ_MAILBOX_3	IRQ#11	ICONT1/ICONT2	MAILBOX_IVA user 3 interrupt request.
	No DMA Requests			

NOTE: For information about interrupt source description, see Section 19.3.4, *Interrupt Requests*.

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19.3 Mailbox Functional Description

NOTE: In the mailbox functional description, *u* is the user number and *m* is the mailbox number as follows:

- for the MAILBOX module instance, *u*=0 to 2 and *m*=0 to 7
- for the MAILBOX_IVA module instance, *u*=0 to 3 and *m*=0 to 5

The mailbox module provides a means of communication through message queues among the users (depending on the mailbox module instance). The individual mailbox modules (8 for the MAILBOX instance, 6 for the MAILBOX_IVA instance), or FIFOs, can associate (or de-associate) with any of the processors using the MAILBOX_IRQENABLE_SET_u (or MAILBOX_IRQENABLE_CLR_u) register.

CAUTION

For the MAILBOX_IVA instance, communication is possible only if one of the users is ICONT1 or ICONT2.

The mailbox module includes the following user subsystems:

- User 0: MPU subsystem (u = 0)
- User 1: DSP subsystem (u = 1)
- User 2: IPU subsystem (u = 2)
- User 3:
  - For the MAILBOX_IVA instance - IVA subsystem (ICONT1 or ICONT2)

Each user has a dedicated interrupt signal from the corresponding mailbox module instance and dedicated interrupt enabling and status registers.
Each MAILBOX_IRQSTATUS_RAW_u/MAILBOX_IRQSTATUS_CLR_u interrupt status register corresponds to a particular user.

For the MAILBOX instance, a user can query its interrupt status register through the L4_CFG interconnect.

For the MAILBOX_IVA instance, a user can query its interrupt status register as follows:

- MPU and IPU - through the L3_MAIN interconnect
- ICONT1/ICONT2 and DSP - private access (directly through the IVA local interconnect)

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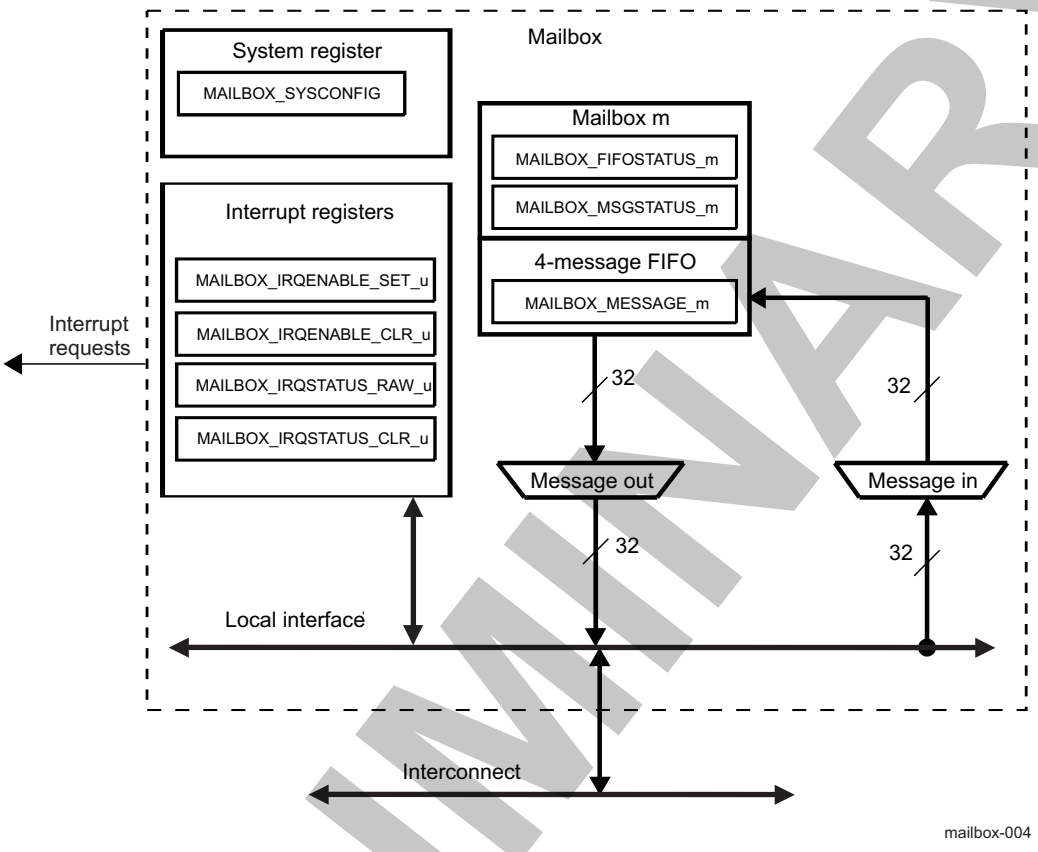
19.3.1 Mailbox Block Diagram

Figure 19-4 shows the mailbox block diagram.

Figure 19-4. Mailbox Block Diagram



NOTE: The interrupt requests and the interconnect depend on the mailbox module instance. For more information, see Section 19.2, *Mailbox Integration*.

19.3.2 Mailbox Software Reset

The mailbox module supports a software reset through the MAILBOX_SYSCONFIG[0] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. Reading the MAILBOX_SYSCONFIG[0] SOFTRESET bit gives the status of the software reset:

- Read 1: the software reset is on-going.
- Read 0: the software reset is complete.

The software must ensure that the software reset completes before doing mailbox operations.

19.3.3 Mailbox Power Management

Table 19-7 describes power-management features available for the mailbox module.

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NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see Clock Domain-Level Clock Management, in *Power, Reset, and Clock Management* chapter.
- For descriptions of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Module-Level Clock Management, in *Power, Reset, and Clock Management* chapter.

Table 19-7. Local Power Management Features

Feature	Registers	Description
Clock autogating	NA	Feature not available
Slave idle modes	MAILBOX_SYSCONFIG[3:2] SIDLEMODE bit field	Force-idle, no-idle and smart-idle modes are available
Clock activity	NA	Feature not available
Master standby modes	NA	Feature not available
Global wake-up enable	NA	Feature not available
Wake-up sources enable	NA	Feature not available

The mailbox module can be configured using the MAILBOX_SYSCONFIG[3:2] SIDLEMODE bit field to one of the following acknowledgment modes:

- Force-idle mode (SIDLEMODE = 0x0): The mailbox module immediately enters the idle state on receiving a low-power-mode request from the PRCM module. In this mode, the software must ensure that there are no asserted output interrupts before requesting this mode to go into the idle state.
- No-idle mode (SIDLEMODE = 0x1): The mailbox module never enters the idle state.
- Smart-idle mode (SIDLEMODE = 0x2): After receiving a low-power-mode request from the PRCM module, the mailbox module enters the idle state only after all asserted output interrupts are acknowledged.

19.3.4 Mailbox Interrupt Requests

An interrupt request allows the user of the mailbox to be notified when a message is received or when the message queue is not full. There is one interrupt per user.

NOTE: For more information about interrupt requests, see Section 19.2, *Mailbox Integration*.

Table 19-8 lists the event flags, and their mask, that can cause module interrupts.

Table 19-8. Interrupt Events

Non-Maskable Event Flag[1]	Maskable Event Flag	Event Mask Bit	Event Unmask Bit	Description
MAILBOX_IRQSTATUS_RAW_u[0+m*2] NEWMSGSTATUSUUMBm	MAILBOX_IRQSTATUS_CLR_u[0+m*2] NEWMSGSTATUSUUMBm	MAILBOX_IRQENABLE_CLR_u[0+m*2] NEWMSGSTATUSUUMBm	MAILBOX_IRQENABLE_SET_u[0+m*2] NEWMSGSTATUSUUMBm	Mailbox *m* receives a new message.
MAILBOX_IRQSTATUS_RAW_u[1+m*2] NOTFULLSTATUSUUMBm	MAILBOX_IRQSTATUS_CLR_u[1+m*2] NOTFULLSTATUSUUMBm	MAILBOX_IRQENABLE_CLR_u[1+m*2] NOTFULLSTATUSUUMBm	MAILBOX_IRQENABLE_SET_u[1+m*2] NOTFULLSTATUSUUMBm	Mailbox *m* message queue is not full.

(1) MAILBOX.MAILBOX_IRQSTATUS_RAW_u register is mostly used for debug purposes.

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CAUTION

Once an event generating the interrupt request has been processed by the software, it must be cleared by writing a logical 1 in the corresponding bit of the MAILBOX_IRQSTATUS_CLR_u register.

Writing a logical 1 in a bit of the MAILBOX_IRQSTATUS_CLR_u register will also clear to 0 the corresponding bit in the appropriate MAILBOX_IRQSTATUS_RAW_u register.

An event can generate an interrupt request when a logical 1 is written to the corresponding unmask bit in the MAILBOX_IRQENABLE_SET_u register. Events are reported in the appropriate MAILBOX_IRQSTATUS_CLR_u and MAILBOX_IRQSTATUS_RAW_u registers.

An event stops generating interrupt requests when a logical 1 is written to the corresponding mask bit in the MAILBOX_IRQENABLE_CLR_u register. Events are only reported in the appropriate MAILBOX_IRQSTATUS_RAW_u register.

In case of the MAILBOX_IRQSTATUS_RAW_u register, the event is reported in the corresponding bit even if the interrupt request generation is disabled for this event.

19.3.5 Mailbox Assignment

19.3.5.1 Description

To assign a receiver to a mailbox, set the new message interrupt enable bit corresponding to the desired mailbox in the MAILBOX_IRQENABLE_SET_u register. The receiver reads the MAILBOX_MESSAGE_m register to retrieve a message from the mailbox.

An alternate method for the receiver that does not use the interrupts is to poll the MAILBOX_FIFOSTATUS_m and/or MAILBOX_MSGSTATUS_m registers to know when to send or retrieve a message to or from the mailbox. This method does not require assigning a receiver to a mailbox. Because this method does not include the explicit assignment of the mailbox, the software must avoid having multiple receivers use the same mailbox, which can result in incoherency.

To assign a sender to a mailbox, set the queue-not-full interrupt enable bit of the desired mailbox in the MAILBOX_IRQENABLE_SET_u register, where *u* is the number of the sending user. However, direct allocation of a mailbox to a sender is not recommended because it can cause the sending processor to be constantly interrupted.

It is recommended that register polling be used to:

- Check the status of either the MAILBOX_FIFOSTATUS_m or MAILBOX_MSGSTATUS_m registers
- Write the message to the corresponding MAILBOX_MESSAGE_m register, if space is available.

The sender might use the queue-not-full interrupt when the initial mailbox status check indicates the mailbox is full. In this case, the sender can enable the queue-not-full interrupt for its mailbox in the appropriate MAILBOX_IRQENABLE_SET_u register. This allows the sender to be notified by interrupt only when a FIFO queue has at least one available entry.

Reading the MAILBOX_IRQSTATUS_CLR_u register determines the status of the new message and the queue-not-full interrupts for a particular user. Writing 1 to the corresponding bit in the MAILBOX_IRQSTATUS_CLR_u register acknowledges, and subsequently clears, an interrupt.

CAUTION

Assigning multiple senders or multiple receivers to the same mailbox is not recommended.

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19.3.6 Sending and Receiving Messages

19.3.6.1 Description

When a 32-bit message is written to the MAILBOX_MESSAGE_m register, the message is appended into the FIFO queue. This queue holds four messages. If the queue is full, the message is discarded.

Queue overflow can be avoided by first reading the MAILBOX_FIFOSTATUS_m register to check that the mailbox message queue is not full before writing a new message to it.

Reading the MAILBOX_MESSAGE_m register returns the message at the beginning of the FIFO queue and removes it from the queue. If the FIFO queue is empty when the MAILBOX_MESSAGE_m register is read, the value 0 is returned.

The new message interrupt is asserted when at least one message is in the mailbox message FIFO queue. To determine the number of messages in the mailbox message FIFO queue, read the MAILBOX_MSGSTATUS_m register.

19.3.7 16-Bit Register Access

19.3.7.1 Description

So that 16-bit processors can access the mailbox module, the module allows 16-bit register read and write access, with restrictions for the MAILBOX_MESSAGE_m registers. The 16-bit half-words are organized in little endian fashion; that is, the least-significant 16 bits are at the low address and the most-significant 16 bits are at the high address (low address + 0x02).

All mailbox module registers can be read or written to directly using individual 16-bit accesses with no restriction on interleaving, except the MAILBOX_MESSAGE_m registers, which must always be accessed by either single 32-bit accesses or two consecutive 16-bit accesses.

CAUTION

When using 16-bit accesses, it is critical to ensure that the mailbox used has only one assigned receiver and only one assigned sender.

When using 16-bit accesses to the MAILBOX_MESSAGE_m registers, the order of access must be the least-significant half-word first (low address) and the most-significant half-word last (high address). This requirement is because of the update operation by the message FIFO of the MAILBOX_MSGSTATUS_m registers. The update of the FIFO queue contents and the associated status registers and possible interrupt generation occurs only when the most-significant 16 bits of a MAILBOX_MESSAGE_m are accessed.

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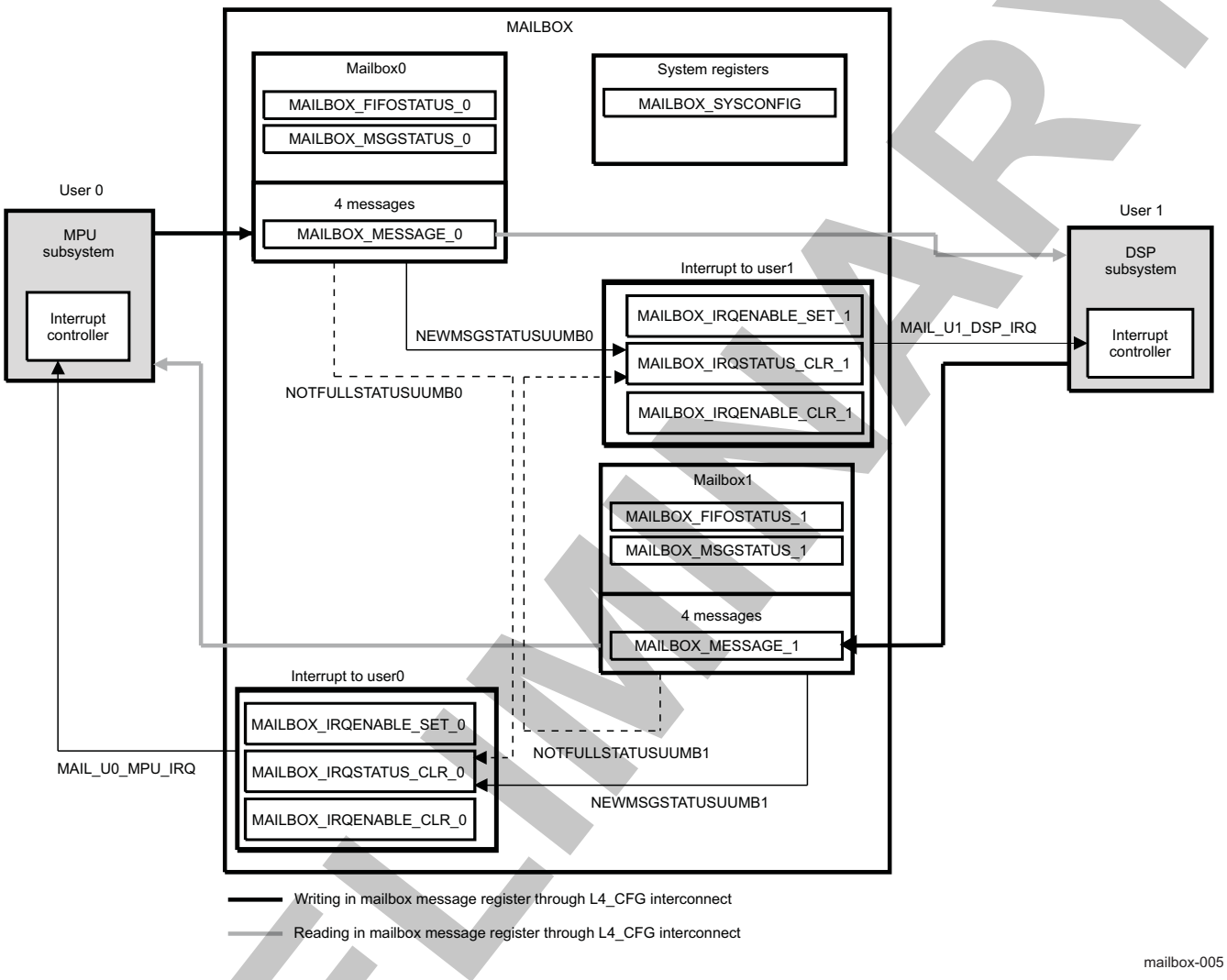
19.3.8 Example of Communication

Figure 19-5 shows an example of communication between MPU and DSP subsystems.

Figure 19-5. Example of Communication



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19.4 Mailbox Programming Guide

19.4.1 Mailbox Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the mailbox module.

19.4.1.1 Global Initialization

19.4.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the mailbox module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the mailbox.

See Section 19.2, *Mailbox Integration*, for further information.

Table 19-9. Global Initialization of Surrounding Modules for MAILBOX

Surrounding Modules	Comments
PRCM	Mailbox functional/interface clock must be enabled. For more information, see CD_L4_CFG Clock Domain , in *Power, Reset, and Clock Management* chapter.
Interrupt Controllers	MPU, or IPU, or DSP interrupt controller must be configured to enable the interrupt request generation to the MPU, or IPU, or DSP subsystem. For information about enabling interrupts in INTC_MPU, see the *ARM Cortex™-A15 MPCore Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp). For information about enabling interrupts in INTC_IPU, see the *ARM Cortex™-M4 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp). For information about enabling interrupts in INTC_DSP, see DSP Subsystem chapter.
Interconnect	For information about L4_CFG interconnect configuration, see L4 Interconnects, in *Interconnect* chapter.

Table 19-10. Global Initialization of Surrounding Modules for MAILBOX_IVA

Surrounding Modules	Comments
PRCM	Mailbox functional/interface clock must be enabled. For more information, see Power, Reset, and Clock Management chapter.
Interrupt Controllers	MPU, or IPU, or DSP, or ICONT1/ICONT2 interrupt controller must be configured to enable the interrupt request generation to the MPU, or IPU, or DSP, or IVA subsystem. For information about enabling interrupts in INTC_MPU, or INTC_IPU, or INTC_DSP, see Table 19-9, *Global Initialization of Surrounding Modules for MAILBOX*.
Interconnect	For information about L3_MAIN interconnect configuration, see L3 Interconnect, in *Interconnect* chapter.

19.4.1.1.2 Mailbox Global Initialization

19.4.1.1.2.1 Main Sequence - Mailbox Global Initialization

This procedure initializes the mailbox module after a power-on or software reset.

Table 19-11. Mailbox Global Initialization

Step	Register/ Bit Field / Programming Model	Value
Perform a software reset	MAILBOX_SYSCONFIG[0] SOFTRESET	0x1
Wait until reset is complete	MAILBOX_SYSCONFIG[0] SOFTRESET	= 0x0
Set idle mode configuration	MAILBOX_SYSCONFIG[3:2] SIDLEMODE	0x-

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19.4.1.2 Mailbox Operational Modes Configuration

19.4.1.2.1 Mailbox Processing modes

19.4.1.2.1.1 Main Sequence - Sending a Message (Polling Method)

Table 19-12. Sending a Message (Polling Method)

Step	Register/ Bit Field / Programming Model	Value
IF : Is FIFO full ?	MAILBOX_FIFOSTATUS_m[0] FIFOFULLMB	= 0x1
Wait until at least one message slot is available	MAILBOX_FIFOSTATUS_m[0] FIFOFULLMB	= 0x0
ELSE		
Write message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
ENDIF		

19.4.1.2.1.2 Main Sequence - Sending a Message (Interupt Method)

Table 19-13. Sending a Message (Interupt Method)

Step	Register/ Bit Field / Programming Model	Value
IF : Is FIFO full ?	MAILBOX_FIFOSTATUS_m[0] FIFOFULLMB	= 0x1
Enable interrupt event	MAILBOX_IRQENABLE_SET_u[1+ m*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 19.4.1.3.1 for interrupt handling in sending mode		
ELSE		
Write message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
ENDIF		

19.4.1.2.1.3 Main Sequence - Receiving a Message (Polling Method)

Table 19-14. Receiving a Message (Polling Method)

Step	Register/ Bit Field / Programming Model	Value
IF : Number of messages is not equal to 0	MAILBOX_MSGSTATUS_m[2:0] NBOFMSGMB	!= 0x0
Read message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
ENDIF		

19.4.1.2.1.4 Main Sequence - Receiving a Message (Interupt Method)

Table 19-15. Receiving a Message (Interupt Method)

Step	Register/ Bit Field / Programming Model	Value
Enable interrupt event	MAILBOX_IRQENABLE_SET_u[0 + m*2]	0x1
User (processor) can perform another task until interrupt occurs See Section 19.4.1.3.2 for interrupt handling in receiving mode		

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19.4.1.3 Mailbox Events Servicing

19.4.1.3.1 Events Servicing in Sending Mode

Table 19-16 describes the events servicing in sending mode.

Table 19-16. Events Servicing in Sending Mode

Step	Register/ Bit Field / Programming Model	Value
Read interrupt status bit	MAILBOX_IRQSTATUS_CLR_u[1 + m*2]	0x1
Write message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
Write 1 to acknowledge interrupt	MAILBOX_IRQSTATUS_CLR_u[1 + m*2]	0x1

19.4.1.3.2 Events Servicing in Receiving Mode

Table 19-17 describes the events servicing in receiving mode.

Table 19-17. Events Servicing in Receiving Mode

Step	Register/ Bit Field / Programming Model	Value
Read interrupt status bit	MAILBOX_IRQSTATUS_CLR_u[0 + m*2]	0x1
IF : Number of messages is not equal to 0 ?	MAILBOX_MSGSTATUS_m[2:0] NBOFMSGMB	!= 0x0
Read message	MAILBOX_MESSAGE_m[31:0] MESSAGEVALUEMBM	0x----
ELSE		
Write 1 to acknowledge interrupt	MAILBOX_IRQSTATUS_CLR_u[0 + m*2]	0x1
ENDIF		

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19.5 Mailbox Register Manual

19.5.1 Mailbox Instance Summary

Table 19-18. MAILBOX Instance Summary

Module Name	Base Address L4_CFG Interconnect	Size
MAILBOX	0x4A0F 4000	4 KiB

Table 19-19. MAILBOX_IVA Instance Summary

Module Name	Base Address L3_MAIN Interconnect	Base Address DSP Subsystem Private Access	Base Address Private Access	Size
MAILBOX_IVA	0x5A05 A800	0x01E5 A800	0x008D A800	4 KiB

NOTE: Private access is an access that does not use the L3_MAIN/L4 interconnects.

19.5.2 Mailbox Registers

19.5.2.1 Mailbox Register Summary

Table 19-20. MAILBOX Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L4_CFG Interconnect
MAILBOX_REVISION	R	32	0x0000 0000	0x4A0F 4000
MAILBOX_SYSCONFIG	RW	32	0x0000 0010	0x4A0F 4010
MAILBOX_MESSAGE_m (1)	RW	32	0x0000 0040 + (0x4 * m)	0x4A0F 4040 + (0x4 * m)
MAILBOX_FIFOSTATUS_m (1)	R	32	0x0000 0080 + (0x4 * m)	0x4A0F 4080 + (0x4 * m)
MAILBOX_MSGSTATUS_m (1)	R	32	0x0000 00C0 + (0x4 * m)	0x4A0F 40C0 + (0x4 * m)
MAILBOX_IRQSTATUS_RAW_u (2)	RW	32	0x0000 0100 + (0x10 * u)	0x4A0F 4100 + (0x10 * u)
MAILBOX_IRQSTATUS_CLR_u (2)	RW	32	0x0000 0104 + (0x10 * u)	0x4A0F 4104 + (0x10 * u)
MAILBOX_IRQENABLE_SET_u (2)	RW	32	0x0000 0108 + (0x10 * u)	0x4A0F 4108 + (0x10 * u)
MAILBOX_IRQENABLE_CLR_u (2)	RW	32	0x0000 010C + (0x10 * u)	0x4A0F 410C + (0x10 * u)
RESERVED			0x0000 0140	0x4A0F 4140

(1) m = 0 to 7
(2) u = 0 to 2

Table 19-21. MAILBOX_IVA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3_MAIN Interconnect	Physical Address DSP Private Access	Physical Address ICONT Private Access
MAILBOX_REVISION	R	32	0x0000 0000	0x5A05 A800	0x01E5 A800	0x008D A800
MAILBOX_SYSCONFIG	RW	32	0x0000 0010	0x5A05 A810	0x01E5 A810	0x008D A810
MAILBOX_MESSAGE_m (1)	RW	32	0x0000 0040 + (0x4 * m)	0x5A05 A840 + (0x4 * m)	0x01E5 A840 + (0x4 * m)	0x008D A840 + (0x4 * m)
MAILBOX_FIFOSTATUS_m (1)	R	32	0x0000 0080 + (0x4 * m)	0x5A05 A880 + (0x4 * m)	0x01E5 A880 + (0x4 * m)	0x008D A880 + (0x4 * m)

(1) m = 0 to 5

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Table 19-21. MAILBOX_IVA Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3_MAIN Interconnect	Physical Address DSP Private Access	Physical Address ICONT Private Access
MAILBOX_MSGSTATUS_m [1]	R	32	0x0000 00C0 + (0x4 * m)	0x5A05 A8C0 + (0x4 * m)	0x01E5 A8C0 + (0x4 * m)	0x008D A8C0 + (0x4 * m)
MAILBOX_IRQSTATUS_RAW_u [2]	RW	32	0x0000 0100 + (0x10 * u)	0x5A05 A900 + (0x10 * u)	0x01E5 A900 + (0x10 * u)	0x008D A900 + (0x10 * u)
MAILBOX_IRQSTATUS_CLR_u [2]	RW	32	0x0000 0104 + (0x10 * u)	0x5A05 A904 + (0x10 * u)	0x01E5 A904 + (0x10 * u)	0x008D A904 + (0x10 * u)
MAILBOX_IRQENABLE_SET_u [2]	RW	32	0x0000 0108 + (0x10 * u)	0x5A05 A908 + (0x10 * u)	0x01E5 A908 + (0x10 * u)	0x008D A908 + (0x10 * u)
MAILBOX_IRQENABLE_CLR_u [2]	RW	32	0x0000 010C + (0x10 * u)	0x5A05 A90C + (0x10 * u)	0x01E5 A90C + (0x10 * u)	0x008D A90C + (0x10 * u)
RESERVED			0x0000 0140	0x5A05 A940	0x01E5 A940	0x008D A940

[2] u = 0 to 3

19.5.2.2 Mailbox Register Description

Table 19-22. MAILBOX_REVISION

Address Offset	0x0000 0000		
Physical Address	0x0000 0000 0x4A0F 4000 0x0000 0000 0x5A05 A800 0x5A05 A800 0x5A05 A800 0x01E5 A800 0x01E5 A800 0x008D A800 0x008D A800 See Table 19-21	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
		Instance	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 19-23. Register Call Summary for Register MAILBOX_REVISION

Mailbox Register Manual
- Mailbox Register Summary: [0] [1]

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Table 19-24. MAILBOX_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x0000 0010 0x4A0F 4010 0x0000 0010 0x5A05 A810 0x5A05 A810 0x5A05 A810 0x01E5 A810 0x01E5 A810 0x008D A810 0x008D A810	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
	See Table 19-21	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
Description	This register controls the various parameters of the communication interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SIDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	RW	0x0000000
3:2	SIDLEMODE	Idle Mode 0x0: Force-idle. An idle request is acknowledged unconditionally 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module based on the internal activity of the module 0x3: reserved do not use	RW	0x2
1	RESERVED	Reserved	RW	0
0	SOFTRESET	Softreset Read 0x0: Soft/Hard reset done Write 0x0: No action Read 0x1: Reset is ongoing Write 0x1: Start the soft reset sequence	RW	0

Table 19-25. Register Call Summary for Register MAILBOX_SYSCONFIG

Mailbox Functional Description
- Mailbox Software Reset: [0] [1]
- Mailbox Power Management: [2] [3]

Mailbox Programming Guide
- Mailbox Global Initialization: [4] [5] [6]

Mailbox Register Manual
- Mailbox Register Summary: [7] [8]

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Table 19-26. MAILBOX_MESSAGE_m

Address Offset	0x0000 0040 + (0x4 * m)	**index:**	m = 0 to 7 (MAILBOX) or m = 0 to 5 (MAILBOX_IVA)
Physical Address	0x0000 0040 + (0x4 * m) 0x4A0F 4040 + (0x4 * m) 0x0000 0040 + (0x4 * m) 0x5A05 A840 + (0x4 * m) 0x5A05 A840 + (0x4 * m) 0x5A05 A840 + (0x4 * m) 0x01E5 A840 + (0x4 * m) 0x01E5 A840 + (0x4 * m) 0x008D A840 + (0x4 * m) 0x008D A840 + (0x4 * m)	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
	See Table 19-21	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
Description	The message register stores the next to be read message of the mailbox. Reads remove the message from the FIFO queue.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MESSAGEVALUEMBM																															

Bits	Field Name	Description	Type	Reset
31:0	MESSAGEVALUEMBM	Message in Mailbox	RW	0x0000 0000

Table 19-27. Register Call Summary for Register MAILBOX_MESSAGE_m

Mailbox Functional Description
- Description: [0] [1]
- Description: [2] [3] [4]
- Description: [5] [6] [7] [8]

Mailbox Programming Guide
- Mailbox Processing modes: [9] [10] [11]
- Events Servicing in Sending Mode: [12]
- Events Servicing in Receiving Mode: [13]

Mailbox Register Manual
- Mailbox Register Summary: [14] [15]

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Table 19-28. MAILBOX_FIFOSTATUS_m

Address Offset	0x0000 0080 + (0x4 * m)	**index:**	m = 0 to 7 (MAILBOX) or m = 0 to 5 (MAILBOX_IVA)
Physical Address	0x0000 0080 + (0x4 * m) 0x4A0F 4080 + (0x4 * m) 0x0000 0080 + (0x4 * m) 0x5A05 A880 + (0x4 * m) 0x5A05 A880 + (0x4 * m) 0x5A05 A880 + (0x4 * m) 0x01E5 A880 + (0x4 * m) 0x01E5 A880 + (0x4 * m) 0x008D A880 + (0x4 * m) 0x008D A880 + (0x4 * m)	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
	See Table 19-21	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
Description	The FIFO status register has the status related to the mailbox internal FIFO		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FIFOFULLMBM

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0	R	0x0000 0000
0	FIFOFULLMBM	Full flag for Mailbox Read 0x0: Mailbox FIFO is not full Read 0x1: Mailbox FIFO is full	R	0

Table 19-29. Register Call Summary for Register MAILBOX_FIFOSTATUS_m

Mailbox Functional Description • Description: [0] [1] • Description: [2]
Mailbox Programming Guide • Mailbox Processing modes: [3] [4] [5]
Mailbox Register Manual • Mailbox Register Summary: [6] [7]

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Table 19-30. MAILBOX_MSGSTATUS_m

Address Offset	0x0000 00C0 + (0x4 * m)	**index:**	m = 0 to 7 (MAILBOX) or m = 0 to 5 (MAILBOX_IVA)
Physical Address	0x0000 00C0 + (0x4 * m) 0x4A0F 40C0 + (0x4 * m) 0x0000 00C0 + (0x4 * m) 0x5A05 A8C0 + (0x4 * m) 0x5A05 A8C0 + (0x4 * m) 0x5A05 A8C0 + (0x4 * m) 0x01E5 A8C0 + (0x4 * m) 0x01E5 A8C0 + (0x4 * m) 0x008D A8C0 + (0x4 * m) 0x008D A8C0 + (0x4 * m)	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
	See Table 19-21	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
Description	The message status register has the status of the messages in the mailbox.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														NBOFMSGMBM	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved. Read returns 0	R	0x0000 0000
2:0	NBOFMSGMBM	Number of unread messages in Mailbox Note: Limited to four messages per mailbox.	R	0x00

Table 19-31. Register Call Summary for Register MAILBOX_MSGSTATUS_m

Mailbox Functional Description
- Description: [0] [1]
- Description: [2]
- Description: [3]

Mailbox Programming Guide
- Mailbox Processing modes: [4]
- Events Servicing in Receiving Mode: [5]

Mailbox Register Manual
- Mailbox Register Summary: [6] [7]

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Table 19-32. MAILBOX_IRQSTATUS_RAW_u

Address Offset	0x0000 0100 + (0x10 * u)	**index:**	u = 0 to 2 (MAILBOX) or u = 0 to 3 (MAILBOX_IVA)
Physical Address	0x0000 0100 + (0x10 * u) 0x4A0F 4100 + (0x10 * u) 0x0000 0100 + (0x10 * u) 0x5A05 A900 + (0x10 * u) 0x5A05 A900 + (0x10 * u) 0x5A05 A900 + (0x10 * u) 0x01E5 A900 + (0x10 * u) 0x01E5 A900 + (0x10 * u) 0x008D A900 + (0x10 * u) 0x008D A900 + (0x10 * u)	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
	See Table 19-21	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
Description	The interrupt status register has the raw status for each event that may be responsible for the generation of an interrupt to the corresponding user - write 1 to a given bit sets this bit. This register is mainly used for debug purpose.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NOTFULLSTATUSENUUMB7	NEWMSGSTATUSUUMB7	NOTFULLSTATUSUUMB6	NEWMSGSTATUSUUMB6	NOTFULLSTATUSUUMB5	NEWMSGSTATUSUUMB5	NOTFULLSTATUSUUMB4	NEWMSGSTATUSUUMB4	NOTFULLSTATUSUUMB3	NEWMSGSTATUSUUMB3	NOTFULLSTATUSUUMB2	NEWMSGSTATUSUUMB2	NOTFULLSTATUSUUMB1	NEWMSGSTATUSUUMB1	NOTFULLSTATUSUUMB0	NEWMSGSTATUSUUMB0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
15	NOTFULLSTATUSENUUMB7	NotFull Status bit for User u, Mailbox 7 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
14	NEWMSGSTATUSUUMB7	NewMessage Status bit for User u, Mailbox 7 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
13	NOTFULLSTATUSUUMB6	NotFull Status bit for User u, Mailbox 6 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1

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Bits	Field Name	Description	Type	Reset
12	NEWMSGSTATUSUUMB6	NewMessage Status bit for User u, Mailbox 6 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
11	NOTFULLSTATUSUUMB5	NotFull Status bit for User u, Mailbox 5 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
10	NEWMSGSTATUSUUMB5	NewMessage Status bit for User u, Mailbox 5 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
9	NOTFULLSTATUSUUMB4	NotFull Status bit for User u, Mailbox 4 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
8	NEWMSGSTATUSUUMB4	NewMessage Status bit for User u, Mailbox 4 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
7	NOTFULLSTATUSUUMB3	NotFull Status bit for User u, Mailbox 3 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
6	NEWMSGSTATUSUUMB3	NewMessage Status bit for User u, Mailbox 3 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
5	NOTFULLSTATUSUUMB2	NotFull Status bit for User u, Mailbox 2 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
4	NEWMSGSTATUSUUMB2	NewMessage Status bit for User u, Mailbox 2 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0

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Bits	Field Name	Description	Type	Reset
3	NOTFULLSTATUSUUMB1	NotFull Status bit for User u, Mailbox 1 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
2	NEWMSGSTATUSUUMB1	NewMessage Status bit for User u, Mailbox 1 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0
1	NOTFULLSTATUSUUMB0	NotFull Status bit for User u, Mailbox 0 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Set the event (for debug)	RW	1
0	NEWMSGSTATUSUUMB0	NewMessage Status bit for User u, Mailbox 0 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Set the event (for debug)	RW	0

Table 19-33. Register Call Summary for Register MAILBOX_IRQSTATUS_RAW_u

Mailbox Functional Description • Mailbox Functional Description: [0] • Mailbox Interrupt Requests: [1] [2] [3] [4] [5] [6]
Mailbox Register Manual • Mailbox Register Summary: [7] [8] • Mailbox Register Description: [9]

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Table 19-34. MAILBOX_IRQSTATUS_CLR_u

Address Offset	0x0000 0104 + (0x10 * u)	**index:**	u = 0 to 2 (MAILBOX) or u = 0 to 3 (MAILBOX_IVA)
Physical Address	0x0000 0104 + (0x10 * u) 0x4A0F 4104 + (0x10 * u) 0x0000 0104 + (0x10 * u) 0x5A05 A904 + (0x10 * u) 0x5A05 A904 + (0x10 * u) 0x5A05 A904 + (0x10 * u) 0x01E5 A904 + (0x10 * u) 0x01E5 A904 + (0x10 * u) 0x008D A904 + (0x10 * u) 0x008D A904 + (0x10 * u) See Table 19-21	**Instance** **Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
Description	The interrupt status register has the status combined with irq-enable for each event that may be responsible for the generation of an interrupt to the corresponding user - write 1 to a given bit resets this bit		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NOTFULLSTATUSENUUMB7	NEWMSGSTATUSENUUMB7	NOTFULLSTATUSENUUMB6	NEWMSGSTATUSENUUMB6	NOTFULLSTATUSENUUMB5	NEWMSGSTATUSENUUMB5	NOTFULLSTATUSENUUMB4	NEWMSGSTATUSENUUMB4	NOTFULLSTATUSENUUMB3	NEWMSGSTATUSENUUMB3	NOTFULLSTATUSENUUMB2	NEWMSGSTATUSENUUMB2	NOTFULLSTATUSENUUMB1	NEWMSGSTATUSENUUMB1	NOTFULLSTATUSENUUMB0	NEWMSGSTATUSENUUMB0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
15	NOTFULLSTATUSENUUMB7	NotFull Status bit for User u, Mailbox 7 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
14	NEWMSGSTATUSENUUMB7	NewMessage Status bit for User u, Mailbox 7 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
13	NOTFULLSTATUSENUUMB6	NotFull Status bit for User u, Mailbox 6 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0

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Bits	Field Name	Description	Type	Reset
12	NEWMSGSTATUSENUUMB6	NewMessage Status bit for User u, Mailbox 6 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
11	NOTFULLSTATUSENUUMB5	NotFull Status bit for User u, Mailbox 5 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
10	NEWMSGSTATUSENUUMB5	NewMessage Status bit for User u, Mailbox 5 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
9	NOTFULLSTATUSENUUMB4	NotFull Status bit for User u, Mailbox 4 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
8	NEWMSGSTATUSENUUMB4	NewMessage Status bit for User u, Mailbox 4 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
7	NOTFULLSTATUSENUUMB3	NotFull Status bit for User u, Mailbox 3 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
6	NEWMSGSTATUSENUUMB3	NewMessage Status bit for User u, Mailbox 3 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
5	NOTFULLSTATUSENUUMB2	NotFull Status bit for User u, Mailbox 2 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
4	NEWMSGSTATUSENUUMB2	NewMessage Status bit for User u, Mailbox 2 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0

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Bits	Field Name	Description	Type	Reset
3	NOTFULLSTATUSENUUMB1	NotFull Status bit for User u, Mailbox 1 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
2	NEWMSGSTATUSENUUMB1	NewMessage Status bit for User u, Mailbox 1 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0
1	NOTFULLSTATUSENUUMB0	NotFull Status bit for User u, Mailbox 0 Read 0x0: No event pending (message queue full) Write 0x0: No action Read 0x1: Event pending (message queue not full) Write 0x1: Clear pending event, if any	RW	0
0	NEWMSGSTATUSENUUMB0	NewMessage Status bit for User u, Mailbox 0 Read 0x0: No event (message) pending Write 0x0: No action Read 0x1: Event (message) pending Write 0x1: Clear pending event, if any	RW	0

Table 19-35. Register Call Summary for Register MAILBOX_IRQSTATUS_CLR_u

Mailbox Functional Description • Mailbox Functional Description: [0] • Mailbox Interrupt Requests: [1] [2] [3] [4] [5] • Description: [6] [7]
Mailbox Programming Guide • Events Servicing in Sending Mode: [8] [9] • Events Servicing in Receiving Mode: [10] [11]
Mailbox Register Manual • Mailbox Register Summary: [12] [13] • Mailbox Register Description: [14]

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Table 19-36. MAILBOX_IRQENABLE_SET_u

Address Offset	0x0000 0108 + (0x10 * u)	**index:**	u = 0 to 2 (MAILBOX) or u = 0 to 3 (MAILBOX_IVA)
Physical Address	0x0000 0108 + (0x10 * u) 0x4A0F 4108 + (0x10 * u) 0x0000 0108 + (0x10 * u) 0x5A05 A908 + (0x10 * u) 0x5A05 A908 + (0x10 * u) 0x5A05 A908 + (0x10 * u) 0x01E5 A908 + (0x10 * u) 0x01E5 A908 + (0x10 * u) 0x008D A908 + (0x10 * u) 0x008D A908 + (0x10 * u)	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
	See Table 19-21	**Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
Description	The interrupt enable register enables to unmask the module internal source of interrupt to the corresponding user. This register is write 1 to set.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NOTFULLENABLEUUMB7	NEWMSGENABLEUUMB7	NOTFULLENABLEUUMB6	NEWMSGENABLEUUMB6	NOTFULLENABLEUUMB5	NEWMSGENABLEUUMB5	NOTFULLENABLEUUMB4	NEWMSGENABLEUUMB4	NOTFULLENABLEUUMB3	NEWMSGENABLEUUMB3	NOTFULLENABLEUUMB2	NEWMSGENABLEUUMB2	NOTFULLENABLEUUMB1	NEWMSGENABLEUUMB1	NOTFULLENABLEUUMB0	NEWMSGENABLEUUMB0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
15	NOTFULLENABLEUUMB7	NotFull Enable bit for User u, Mailbox 7 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
14	NEWMSGENABLEUUMB7	NewMessage Enable bit for User u, Mailbox 7 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
13	NOTFULLENABLEUUMB6	NotFull Enable bit for User u, Mailbox 6 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0

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Bits	Field Name	Description	Type	Reset
12	NEWMSGENABLEUUMB6	NewMessage Enable bit for User u, Mailbox 6 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
11	NOTFULLENABLEUUMB5	NotFull Enable bit for User u, Mailbox 5 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
10	NEWMSGENABLEUUMB5	NewMessage Enable bit for User u, Mailbox 5 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
9	NOTFULLENABLEUUMB4	NotFull Enable bit for User u, Mailbox 4 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
8	NEWMSGENABLEUUMB4	NewMessage Enable bit for User u, Mailbox 4 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
7	NOTFULLENABLEUUMB3	NotFull Enable bit for User u, Mailbox 3 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
6	NEWMSGENABLEUUMB3	NewMessage Enable bit for User u, Mailbox 3 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
5	NOTFULLENABLEUUMB2	NotFull Enable bit for User u, Mailbox 2 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
4	NEWMSGENABLEUUMB2	NewMessage Enable bit for User u, Mailbox 2 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0

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Bits	Field Name	Description	Type	Reset
3	NOTFULLENABLEUUMB1	NotFull Enable bit for User u, Mailbox 1 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
2	NEWMSGENABLEUUMB1	NewMessage Enable bit for User u, Mailbox 1 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
1	NOTFULLENABLEUUMB0	NotFull Enable bit for User u, Mailbox 0 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0
0	NEWMSGENABLEUUMB0	NewMessage Enable bit for User u, Mailbox 0 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW	0

Table 19-37. Register Call Summary for Register MAILBOX_IRQENABLE_SET_u

Mailbox Functional Description • Mailbox Functional Description: [0] • Mailbox Interrupt Requests: [1] [2] [3] • Description: [4] [5] [6]
Mailbox Programming Guide • Mailbox Processing modes: [7] [8]
Mailbox Register Manual • Mailbox Register Summary: [9] [10] • Mailbox Register Description: [11]

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Table 19-38. MAILBOX_IRQENABLE_CLR_u

Address Offset	0x0000 010C + (0x10 * u)	**index:**	u = 0 to 2 (MAILBOX) or u = 0 to 3 (MAILBOX_IVA)
Physical Address	0x0000 010C + (0x10 * u) 0x4A0F 410C + (0x10 * u) 0x0000 010C + (0x10 * u) 0x5A05 A90C + (0x10 * u) 0x5A05 A90C + (0x10 * u) 0x5A05 A90C + (0x10 * u) 0x01E5 A90C + (0x10 * u) 0x01E5 A90C + (0x10 * u) 0x008D A90C + (0x10 * u) 0x008D A90C + (0x10 * u) See Table 19-21	**Instance** **Instance**	MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX MAILBOX MAILBOX MAILBOX_IVA_MAIN_L3 MAILBOX_IVA_ MAILBOX MAILBOX_IVA_ MAILBOX MAILBOX_IVA_
Description	The interrupt enable register enables to mask the module internal source of interrupt to the corresponding user. This register is write 1 to clear.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NOTFULLENABLEUUMB7	NEWMSGENABLEUUMB7	NOTFULLENABLEUUMB6	NEWMSGENABLEUUMB6	NOTFULLENABLEUUMB5	NEWMSGENABLEUUMB5	NOTFULLENABLEUUMB4	NEWMSGENABLEUUMB4	NOTFULLENABLEUUMB3	NEWMSGENABLEUUMB3	NOTFULLENABLEUUMB2	NEWMSGENABLEUUMB2	NOTFULLENABLEUUMB1	NEWMSGENABLEUUMB1	NOTFULLENABLEUUMB0	NEWMSGENABLEUUMB0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Write 0's for future compatibility. Read returns 0.	RW	0
15	NOTFULLENABLEUUMB7	NotFull Enable bit for User u, Mailbox 7 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
14	NEWMSGENABLEUUMB7	NewMessage Enable bit for User u, Mailbox 7 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
13	NOTFULLENABLEUUMB6	NotFull Enable bit for User u, Mailbox 6 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0

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Bits	Field Name	Description	Type	Reset
12	NEWMSGENABLEUUMB6	NewMessage Enable bit for User u, Mailbox 6 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
11	NOTFULLENABLEUUMB5	NotFull Enable bit for User u, Mailbox 5 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
10	NEWMSGENABLEUUMB5	NewMessage Enable bit for User u, Mailbox 5 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
9	NOTFULLENABLEUUMB4	NotFull Enable bit for User u, Mailbox 4 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
8	NEWMSGENABLEUUMB4	NewMessage Enable bit for User u, Mailbox 4 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
7	NOTFULLENABLEUUMB3	NotFull Enable bit for User u, Mailbox 3 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
6	NEWMSGENABLEUUMB3	NewMessage Enable bit for User u, Mailbox 3 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
5	NOTFULLENABLEUUMB2	NotFull Enable bit for User u, Mailbox 2 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
4	NEWMSGENABLEUUMB2	NewMessage Enable bit for User u, Mailbox 2 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0

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Bits	Field Name	Description	Type	Reset
3	NOTFULLENABLEUUMB1	NotFull Enable bit for User u, Mailbox 1 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
2	NEWMSGENABLEUUMB1	NewMessage Enable bit for User u, Mailbox 1 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
1	NOTFULLENABLEUUMB0	NotFull Enable bit for User u, Mailbox 0 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0
0	NEWMSGENABLEUUMB0	NewMessage Enable bit for User u, Mailbox 0 Read 0x0: Interupt disabled Write 0x0: No action Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW	0

Table 19-39. Register Call Summary for Register MAILBOX_IRQENABLE_CLR_u

Mailbox Functional Description • Mailbox Functional Description: [0] • Mailbox Interrupt Requests: [1] [2] [3]
Mailbox Register Manual • Mailbox Register Summary: [4] [5] • Mailbox Register Description: [6]

NOTE: For each interrupt status and enable register (MAILBOX_IRQSTATUS_RAW_u, MAILBOX_IRQSTATUS_CLR_u, MAILBOX_IRQENABLE_SET_u and MAILBOX_IRQENABLE_CLR_u), bits [15:12] have the given meaning only for the MAILBOX instance. For the MAILBOX_IVA instance, these bits are considered as Reserved.

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Memory Management Units

This chapter describes the memory management units (MMUs).

Topic **Page**

20.1 MMU Overview **4466**
20.2 MMU Integration **4467**
20.3 MMU Functional Description **4470**
20.4 MMU Low-level Programming Models **4483**
20.5 MMU Register Manual **4487**

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20.1 MMU Overview

A memory management unit (MMU) is a hardware component responsible for handling accesses to memory requested by a processing unit. MMU functions include translation of virtual addresses to physical addresses (that is, virtual memory management) and cache control.

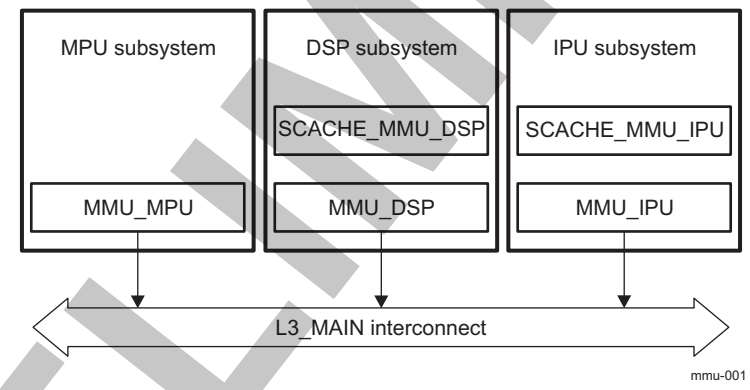
The device contains the following MMUs:

- One MMU inside the MPU (dual Cortex™-A15) subsystem – MMU_MPU. This MMU is integrated in the Cortex-A15 processor. For more information about this MMU, see the ARM® *Cortex™-A15 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).
- Two MMUs inside each of the DSP and IPU (dual Cortex-M4) subsystems:
  - One that manages the memory attribute and mapping at the L1/L2 shared cache level – SCACHE_MMU_DSP and SCACHE_MMU_IPU, respectively. For more information about these MMUs, see DSP Subsystem, and Dual Cortex-M4 IPU Subsystem.
  - One that manages all external accesses to the L3_MAIN interconnect (shared device memory space) – MMU_DSP and MMU_IPU, respectively. The functionality of these MMUs is described in this chapter.

NOTE: There is Physical Address Translator (PAT) module in the Dynamic Memory Manager (DMM), which has similar to the MMU functionality. For more information about this module, see Dynamic Memory Manager.

Figure 20-1 shows the MMU instances in the device.

Figure 20-1. Device MMU Instances



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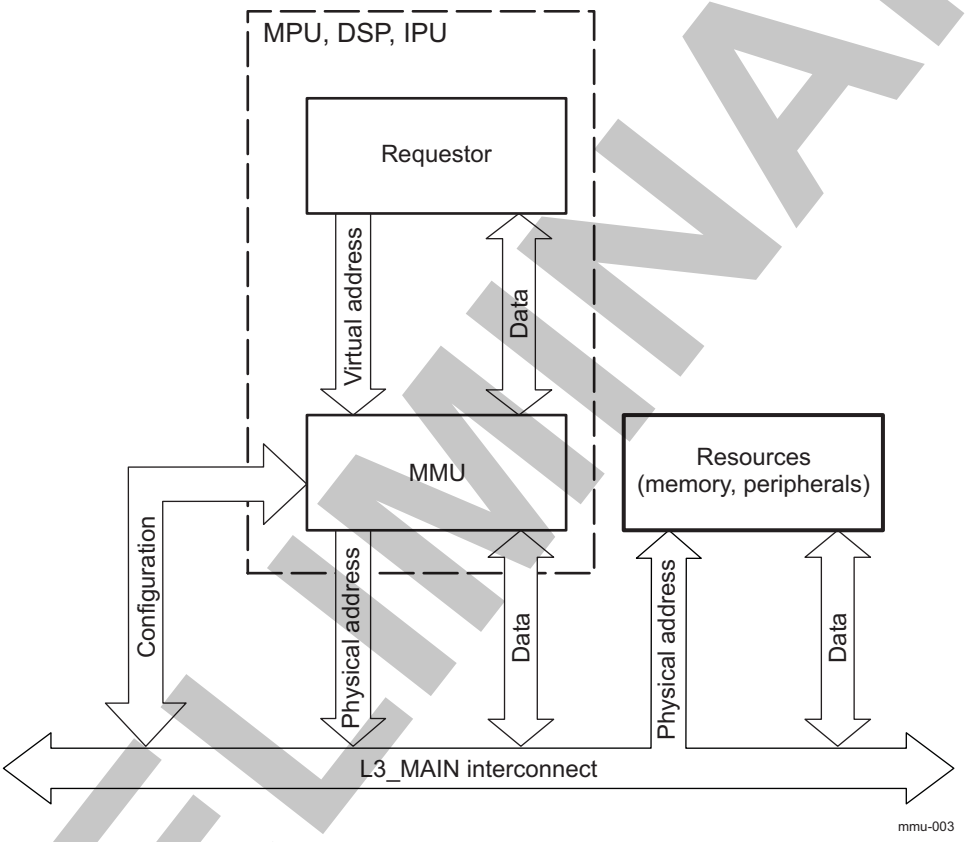
20.2 MMU Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

The MMU communicates accesses from the requestor (MPU, DSP, or IPU) to the L3_MAIN interconnect, performing virtual to physical address translation. Although all MMUs are programmed (configured) through the L3_MAIN interconnect, the MMU_DSP can be programmed both through the L3_MAIN interconnect or through the DSP local interconnect. MMU_DSP and MMU_IPU error conditions are signaled as interrupts to the system main processor Cortex-A15 MPU.

Figure 20-2 shows typical MMU integration.

Figure 20-2. MMU Integration



NOTE: All MMUs are programmed through the L3_MAIN interconnect.

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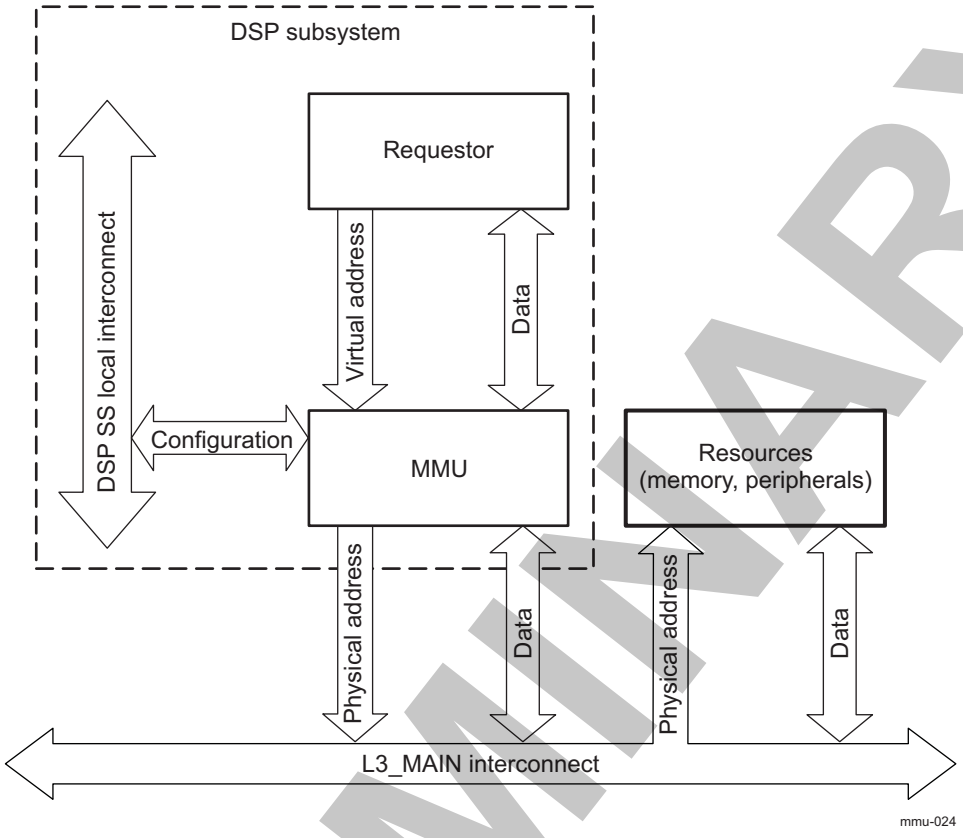
Figure 20-3. MMU_DSP Integration



NOTE: The MMU_DSP can be programmed from both the DSP local interconnect and from the L3_MAIN interconnect.

Table 20-1 through Table 20-3 summarize the MMU integration in the various modules of the device.

Table 20-1. Integration Attributes

Module Instance	Power Domain
MMU_IPU and SCACHE_MMU_IPU	PD_CORE
MMU_MPU	PD_MPU

Table 20-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MMU_MPU	MPU_CORE_CLK	MPU_DPLL_CLK	DPLL_MPU	Internal clock in the MPU subsystem; supplies the MMU in Cortex-A15.
MMU_IPU and SCACHE_MMU_IPU	IPU_GCLK	IPU_GCLK	PRCM	External clock from the power, reset, and clock management (PRCM) module; supplies the SCACHE_MMU_IPU and MMU_IPU.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MMU_IPU	IPU_PWRON_RST	IPU_PWRON_RST	PRCM	Power-on reset signal for the IPU subsystem
	IPU_MMU_SCACHE_RST	IPU_MMU_SCACHE_RST	PRCM	Reset signal to the MMU_IPU

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Table 20-2. Clocks and Resets (continued)

SCACHE_MMU_IPU	IPU_MMU_SCACHE_RST	IPU_MMU_SCACHE_RST	PRCM	Reset signal for the SCACHE_MMU_IPU
	IPU_RET_RST	IPU_RET_RST	PRCM	Retention reset signal for the IPU subsystem
MMU_MPU	MPU_PWRON_RST	MPU_PWRON_RST	PRCM	Power-on reset signal to the MMU_MPU and the rest of the MPU subsystem
	MPU_RST	MPU_RST	PRCM	Reset signal to the MMU_MPU and the rest of the MPU subsystem

Table 20-3. Hardware Requests

		Interrupt Requests		
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MMU_IPU	IPU_IRQ_MPU	MPU_IRQ_100	INTC_MPU	MMU_IPU interrupt to the MPU interrupt controller (INTC_MPU)
	XLATE_MMU_FAULT_IRQ	IPU_IRQ_16	INTC_IPU	Internal interrupt from the MMU_IPU to the IPU interrupt controller (INTC_IPU)
SCACHE_MMU_IPU	SCACHE_MMU_IRQ	IPU_IRQ_17	INTC_IPU	Internal interrupt from the SCACHE_MMU_IPU to the INTC_IPU

NOTE:

- For a description of the interrupt source, see Section 20.3.5, *Interrupt Requests*.

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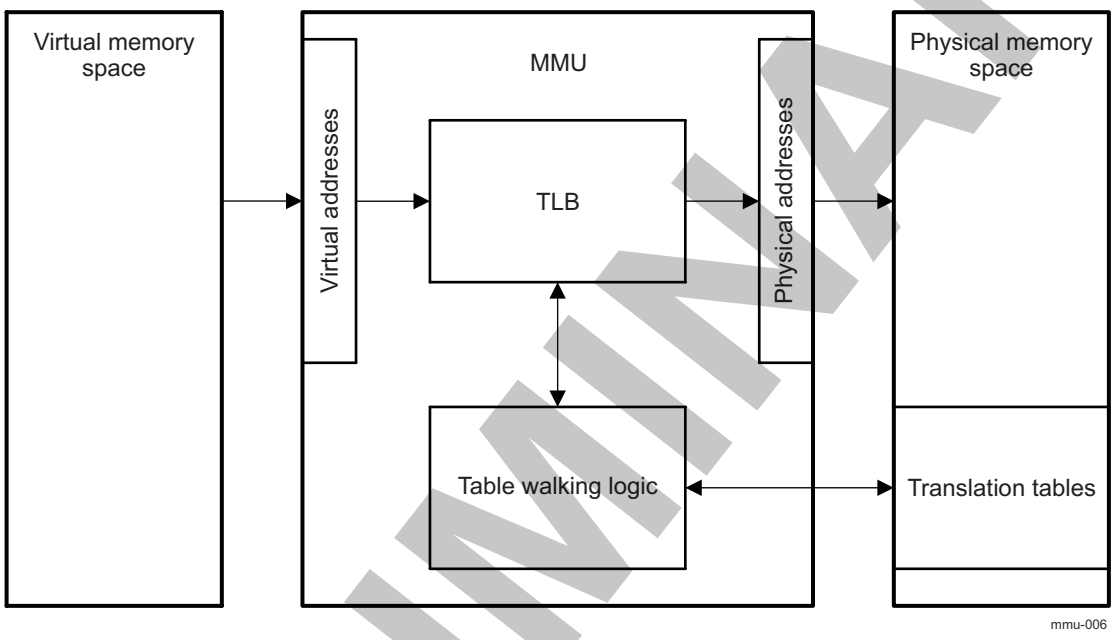
20.3 MMU Functional Description

20.3.1 MMU Block Diagram

The MMU manages the virtual to physical address translation for external addresses, as well as endianness conversion. The MMU can be programmed through the L3_MAIN interconnect. MMU programming is expected to be accomplished by the Cortex-A15 MPU, except for the MMU_DSP, of which the configuration can be accomplished through the DSP local interconnect.

Figure 20-4 is the MMU block diagram.

Figure 20-4. MMU Block Diagram



Each table entry describes the translation of one contiguous memory region. For a description of the structure of these tables, see Section 20.3.1.2, *Translation Tables*.

Two major functional units exist in the MMU to provide address translation automatically based on the table entries:

- The table walker automatically retrieves the correct translation table entry for a requested translation. If two-level translation is used (for the translation of small memory pages), the table walker also automatically reads the required second-level translation table entry. The two-level translation is described later in the chapter.
- The translation look-aside buffer (TLB) stores recently used translation entries, acting like a cache of the translation table.

20.3.1.1 MMU Address Translation Process

Whenever an address translation is requested (that is, for every access with the MMU enabled), the MMU first checks whether the translation is contained in the TLB, which acts like a cache storing recent translations. The TLB can also be programmed manually to ensure that time-critical data can be translated without delay.

If the requested translation is not in the TLB, the table-walking logic retrieves this translation from the translation table(s), and then updates the TLB. The address translation is then performed. Figure 20-5 summarizes the process.

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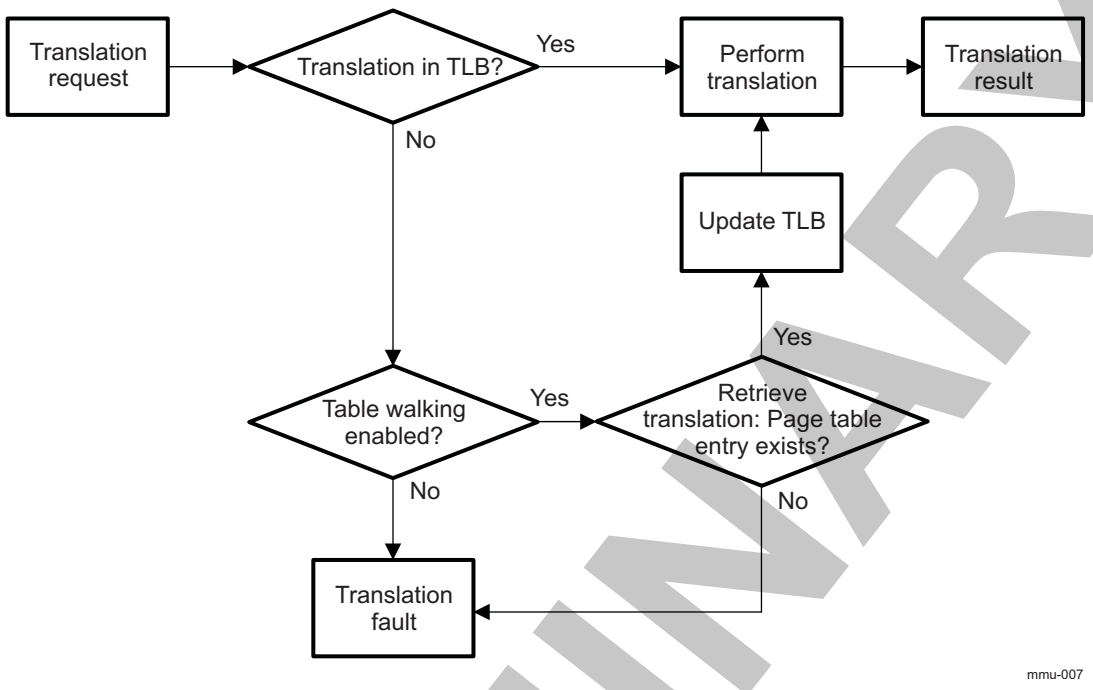
Figure 20-5. Translation Process



20.3.1.2 Translation Tables

The translation of virtual to physical addresses is based on entries in translation tables that define the following properties:

- Address translation, that is, the correspondence between virtual and physical addresses
- Size of the memory region the entry translates
- Endianness, data access size, and the mixed property of this memory region

The virtual addresses index the translation tables. Each virtual address corresponds to exactly one entry in the translation table.

20.3.1.2.1 Translation Table Hierarchy

When developing a table-based address translation scheme, one of the most important design parameters is the memory page size described by each translation table entry. MMU instances support 4-KiB and 64-KiB pages, a 1-MiB section, and a 16-MiB supersection. Using bigger page sizes means a smaller translation table.

Using a smaller page size greatly increases the efficiency of dynamic memory allocation and defragmentation. That is why many operating systems (OSs) can operate on memory blocks as small as 4 KiB; however, the smaller size implies a more complex table structure.

A quick calculation shows that using 4 KiB memory pages with one translation table would require one million entries to span the entire 4-GiB address range. The table itself would be 32 MiB, a size that is not feasible.

However, using bigger pages greatly reduces the functionality of the OS memory management. Implementing a two-level hierarchy reconciles these two requirements. Within this hierarchy, one first-level translation table describes the translation properties based on 1 MiB memory regions.

Each of the entries in this first-level translation table can specify the following:

- The translation properties for a big memory section. This memory section can be either 1 MiB (section) or 16 MiB (supersection). In this case, all translation parameters are specified in the first-level translation table entry.

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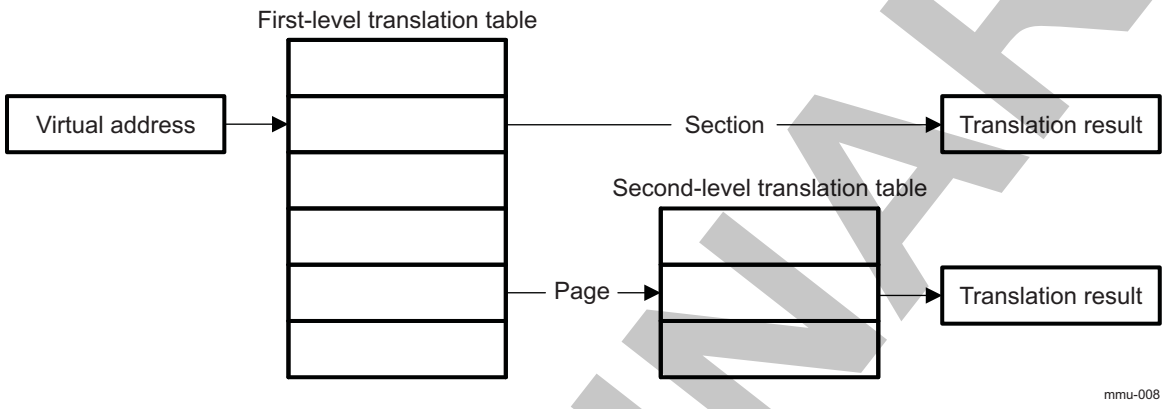
- A pointer to a second-level translation table that specifies individual translation properties based on smaller pages within the 1-MiB page of memory. These pages can be either 64 KiB (large page) or 4 KiB (small page). In this case, the actual translation parameters are specified in the second-level translation table entry. The first-level translation table entry specifies only the base address of the second-level translation table.

This hierarchical approach means that additional translation information for smaller pages must be provided only when the pages are actually used. Figure 20-6 shows the hierarchy.

Figure 20-6. Translation Hierarchy



The structure of the first and second-level translation tables and their entries are described in more detail in Section 20.3.1.2.2, *First-Level Translation Table*, and Section 20.3.1.2.3, *Two-Level Translation*.

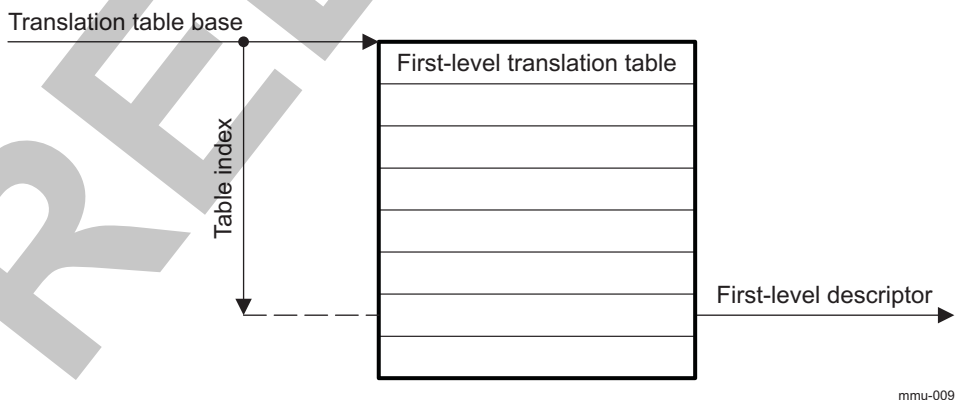
20.3.1.2.2 First-Level Translation Table

The first-level translation table describes the translation properties for 1-MiB sections. To describe a 4-GiB address range requires 4096 32-bit entries (so-called first-level descriptors).

The first-level translation table start address must be aligned on a multiple of the table size with a 128-byte minimum. Consequently, an alignment of at least 16K bytes is required for a complete 4096-entry table; that is, at least the last fourteen address bits must be zero.

The start address of the first-level translation table is specified by the so-called translation table base. The table is indexed by the upper 12-bits of the virtual address. Figure 20-7 shows this mechanism.

Figure 20-7. First-level Descriptor Address Calculation



To summarize, the translation table base and the translation table index together define the first-level descriptor address. Figure 20-8 outlines the precise mechanism used to calculate this address.

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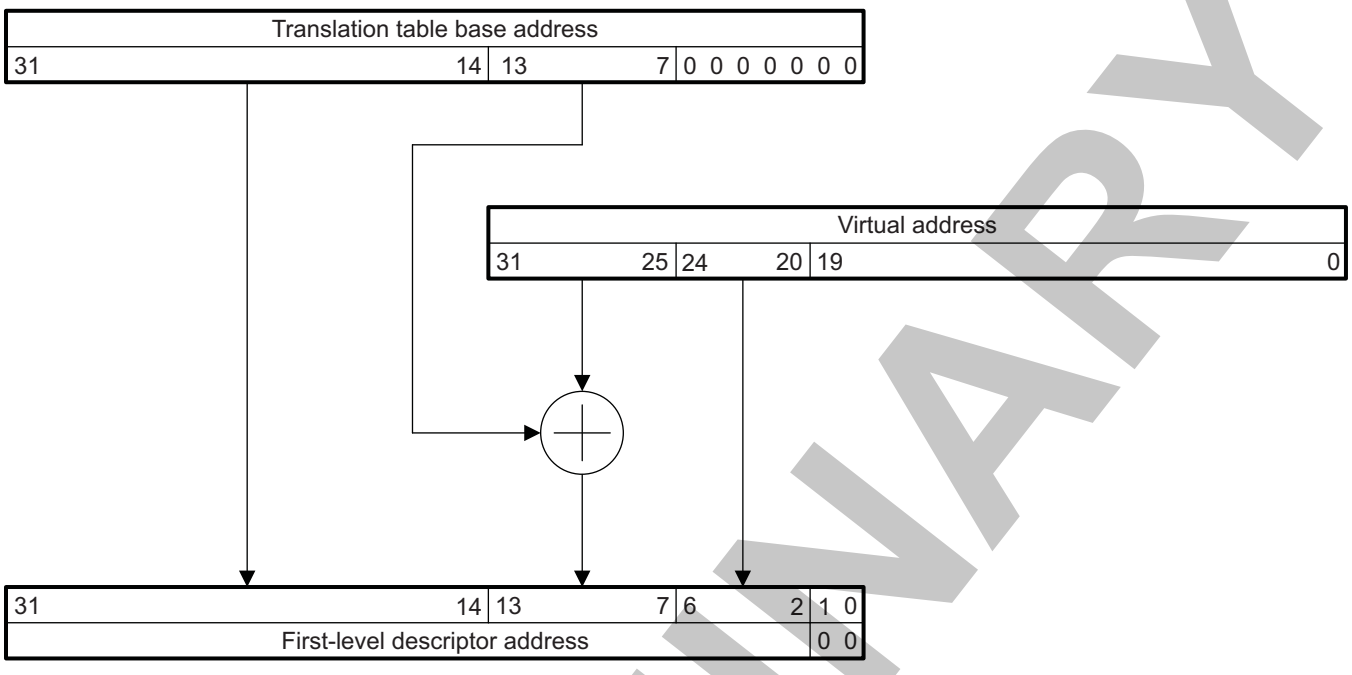
Figure 20-8. Detailed First-Level Descriptor Address Calculation



As an example of this mechanism, consider a translation table base address of 0x8000:0000 and a virtual address of 0x1234:5678. In this case, the first-level descriptor address is 0x8000:0000 + (0x123 << 2) = 0x8000:048C.

20.3.1.2.2.1 First-Level Descriptor Format

Each first-level descriptor provides either the complete address translation for 1-MiB or 16-MiB sections or provides a pointer to a second-level translation table for 4 KiB or 64 KiB pages. Table 20-4 shows the first-level descriptor format.

Table 20-4. First-Level Descriptor Format

First-Level Descriptor Format												
31:24	23:20	19	18	17	16	15	14:12	11:10	9:2	1	0	
X										0	0	Fault
Second-Level Translation Table Base Address									X	0	1	Page
Section Base Address		X	0	M	X	E (1)	X	ES	X	1	0	Section
Supersection Base Address	X		1	M	X	E	X	ES	X	1	0	Supersection
X										1	1	Fault

(1) See for endianness limitations.

M = Mixed region: 0 = Page-based endianness, 1 = Access-based endianness

E = Endianness: 0 = Little endian, 1 = Big endian (endianness is locked on little endian)

ES = Element Size: 00 = 8-bit, 01= 16-bit, 10 = 32-bit, 11 = No endianness conversion

X = Don't care

20.3.1.2.2.2 First-Level Page Descriptor Format

If a translation granularity smaller than 1 MiB is required, a two-level translation process is used. In this case, the first-level block descriptor specifies only the start address of a second-level translation table. The second-level translation table entries specify the actual translation properties.

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20.3.1.2.2.3 First-Level Section Descriptor Format

Each section descriptor in the first-level translation table specifies the complete translation properties for a 1-MiB section or a 16-MiB supersection.

NOTE: Supersection descriptors must be repeated 16 times, because each descriptor in the first-level translation table describes 1 MiB of memory. If an access points to a descriptor that is not initialized, the MMU will behave in an unpredictable way.

In addition to the address translation itself, three parameters are specified in the section descriptors:

- Endianness

  The *endianness* parameter specifies whether the memory section uses a big- or little-endian data format. This parameter is locked to little endian. See Table 20-42 for more information.

- Element size

  The *element size* parameter can optionally specify the data access size (8, 16, or 32 bits) for all data items in the defined section.

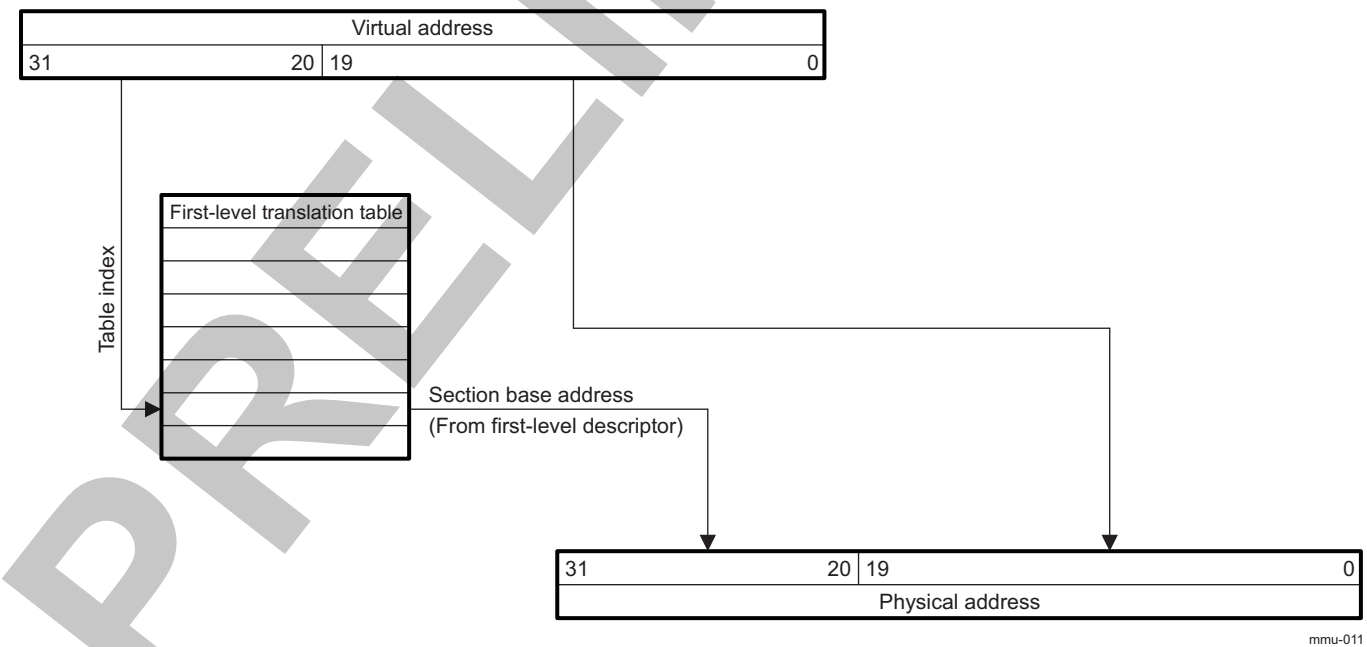
- Mixed region

  The *mixed region* parameter specifies whether the information about the data access size is detected from the access itself (access-based detection) or if the specified element size parameter is used (page-based detection). For example, the specified element size parameter can be used when several smaller sized accesses are packed into a bigger sized access, such as two 16-bit accesses packed into one 32-bit access. In this case, with no specified data access size, 32 bits would be the access size detected, leading to an incorrect result. To avoid this problem, specify the data access size for the memory section.

20.3.1.2.2.4 Section Translation Summary

Sections and supersections can be translated based solely on the information in the first-level translation table. Figure 20-9 summarizes the address translation process for a section.

Figure 20-9. Section Translation Summary



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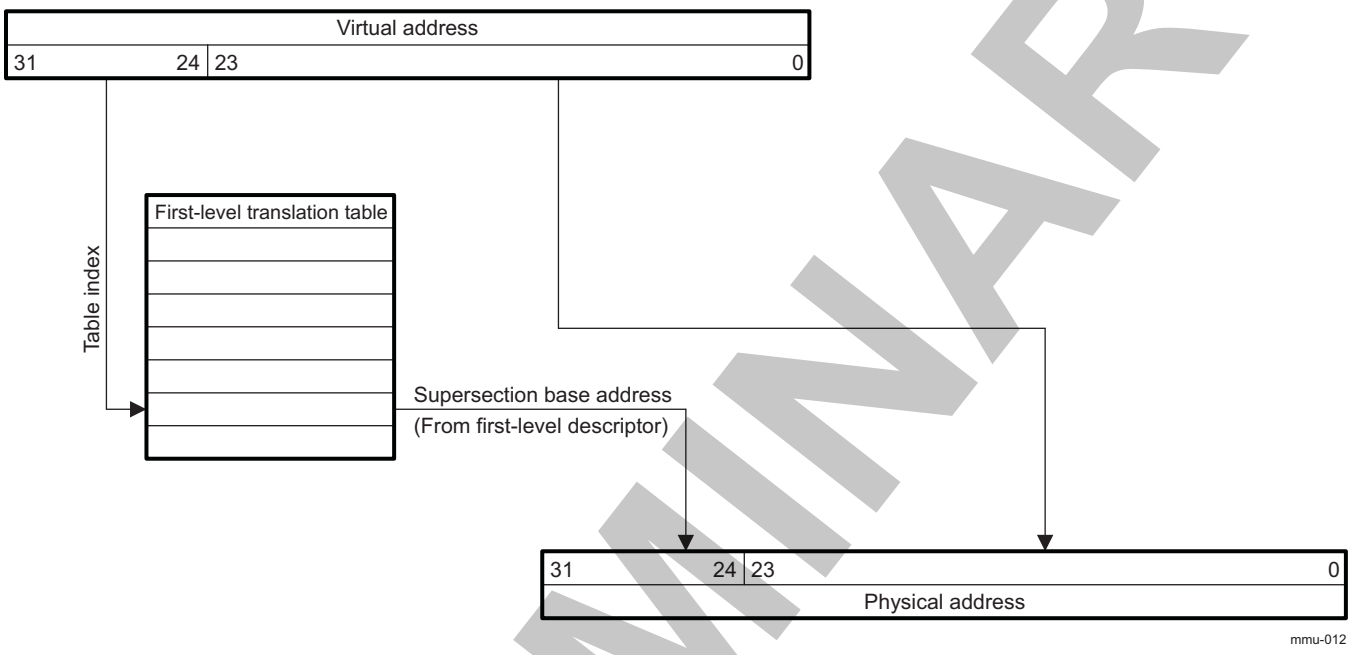
20.3.1.2.2.5 Supersection Translation Summary

The translation of a supersection is similar to the translation of a section. The difference is that for a supersection only bits 31 to 24 index into the first-level translation table. The last four bits of the table index are implicitly assumed to be zero as there are 16 identical consecutive entries for a supersection.

Figure 20-10 shows the translation mechanism for a supersection.

Figure 20-10. Supersection Translation Summary



20.3.1.2.3 Two-Level Translation

Two-level translation is used when fine-grain granularity is required, that is, when memory sections smaller than 1 MiB are needed. In this case, the first-level descriptor provides a pointer to the base address of a second-level translation table. This second-level table is indexed by bits 19 to 12 of the virtual address. Figure 20-11 shows this indexing mechanism.

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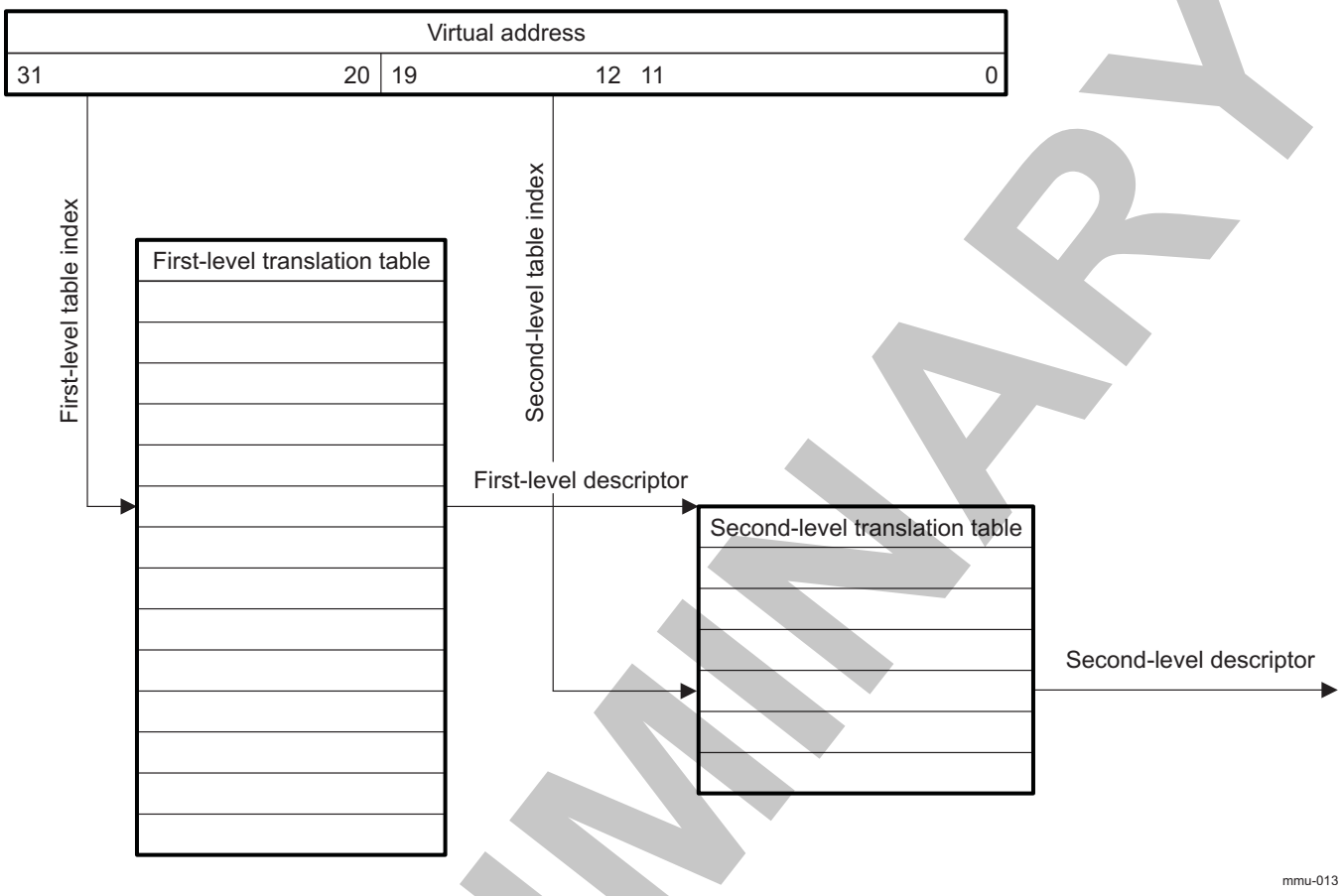
Figure 20-11. Two-Level Translation



Each second-level translation table describes the translation of 1 MiB of address space in pages of 64 KiB (large page) or 4 KiB (small page). It consists of 256 second-level descriptors describing 4 KiB each.

NOTE: In the case of a large page, the same descriptor must be repeated 16 times. If an access points to a descriptor that is not initialized, the MMU will behave in an unpredictable way.

20.3.1.2.3.1 Second-Level Descriptor Format

Similar to first-level section descriptors, second-level descriptors provide all of the necessary information for the translation of a large or small page. Table 20-5 shows the format of second-level descriptors. The translation parameters (endianness, element size, and mixed region) have the same meaning as those for sections.

Table 20-5. Second-Level Descriptor Format

Second-Level Descriptor Format										
31:16	15:12	11	10	9	8:6	5:4	3:2	1	0	
X								0	0	Fault
Large Page Base Address	X	M	X	E (1)	X	ES	X	0	1	Large Page
Small Page Base Address		M	X	E	X	ES	X	1	X	Small Page

(1) See for endianness limitations.

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M = Mixed region: 0 = Page-based endianness, 1 = Access-based endianness

E = Endianness: 0 = Little-endian, 1 = Big-endian (endianness is locked on little endian)

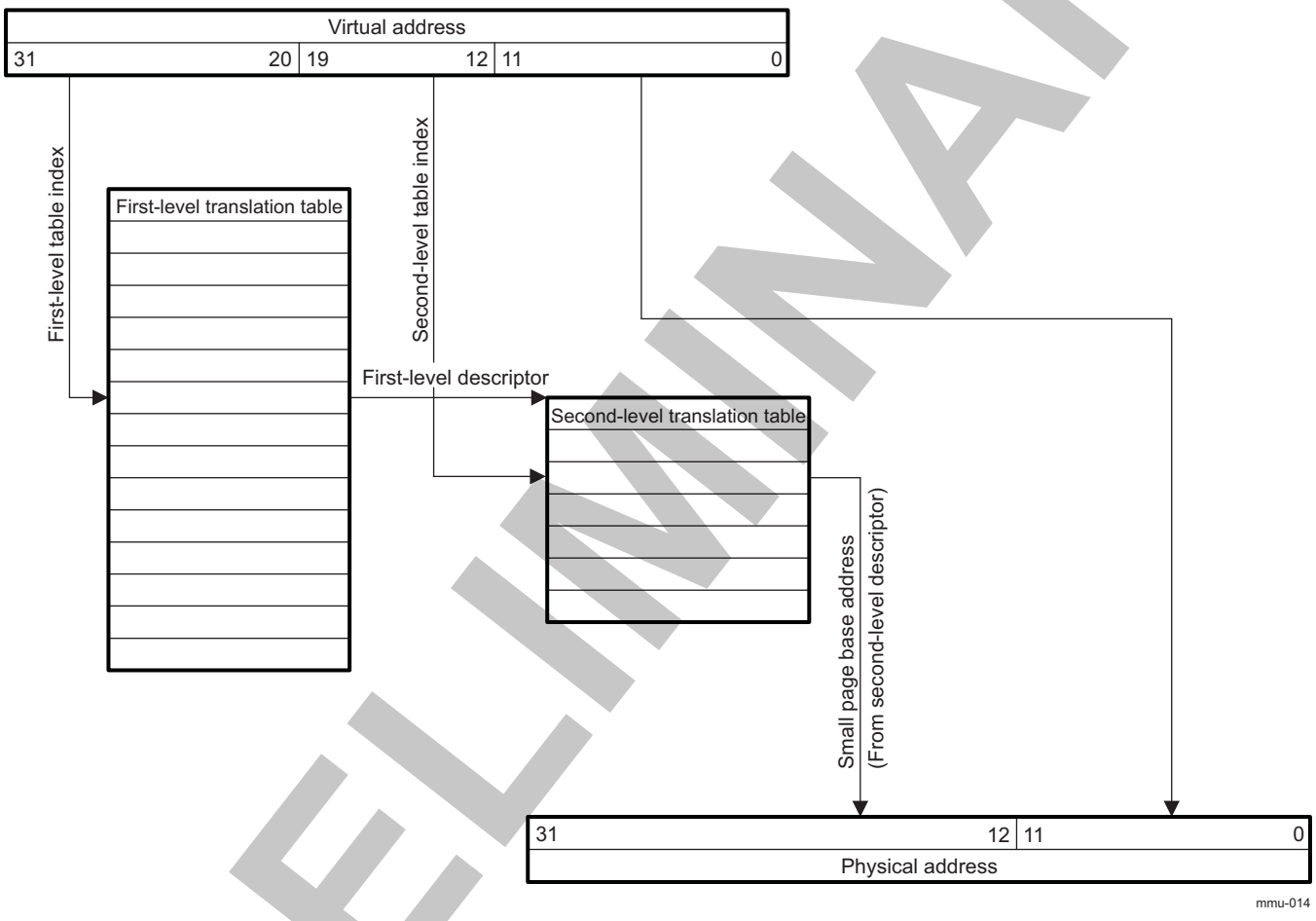
ES = Element Size: 00 = 8-bit, 01= 16-bit, 10 = 32-bit, 11 = No endianness conversion

X = Don't care

20.3.1.2.3.2 Small Page Translation Summary

Figure 20-12 summarizes the translation process for small pages.

Figure 20-12. Small Page Translation Summary



20.3.1.2.3.3 Large Page Translation Summary

The translation of a large page is similar to the translation of a small page. The difference is that, for a large page, only bits 19 to 16 index into the second-level translation table. The last four bits of the table index are implicitly assumed to be zero as there are 16 identical consecutive entries for a large page. This is shown in Figure 20-13.

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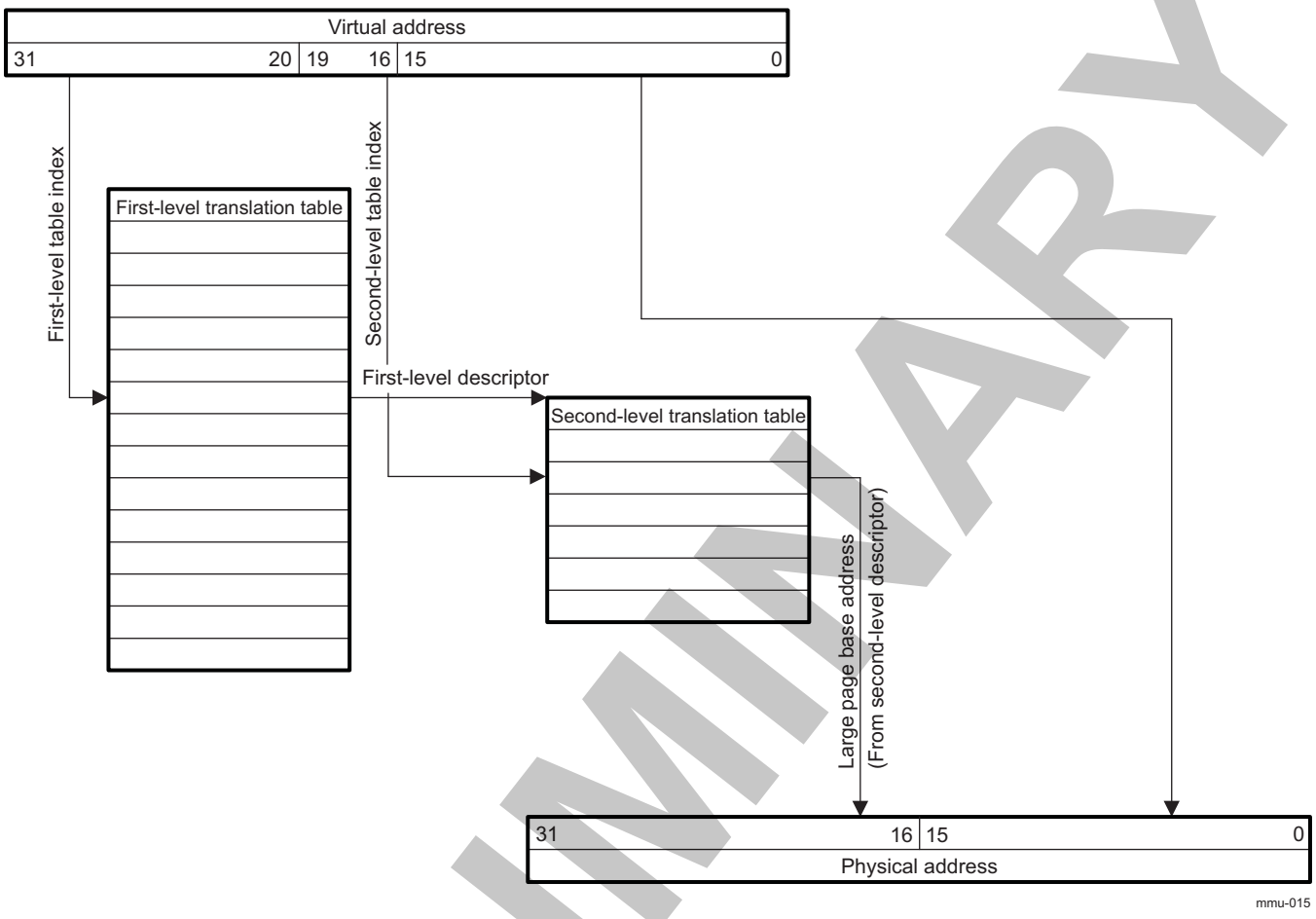
Figure 20-13. Large Page Translation Summary



20.3.1.3 Translation Lookaside Buffer

Translating virtual addresses to physical addresses is required for each memory access in systems using an MMU. To accelerate this translation process, a cache, or TLB, holds the result of recent translations.

For every translation, the MMU internal logic first checks whether the requested translation is already cached in the TLB. If the translation is cached, this translation is used; otherwise the translation is retrieved from the translation tables and the TLB is updated. If the TLB is full, one of its entries must be replaced. This entry is selected on a random basis.

The first *n* TLB entries, where *n* < *Total Number N of TLB Entries*, can be protected (locked) against being overwritten by setting the TLB base pointer to *n*. When this mechanism is used, only unprotected entries can be overwritten. The victim pointer indicates the next TLB entry to be written. Figure 20-14 shows an example of the TLB with N TLB entries (ranging from 0 to N-1). The base pointer contains the value "3" protecting Entry 0, Entry 1, and Entry 2 and the victim pointer points to the next TLB entry to be updated.

NOTE: The last TLB entry (Entry N-1) always remains unprotected.

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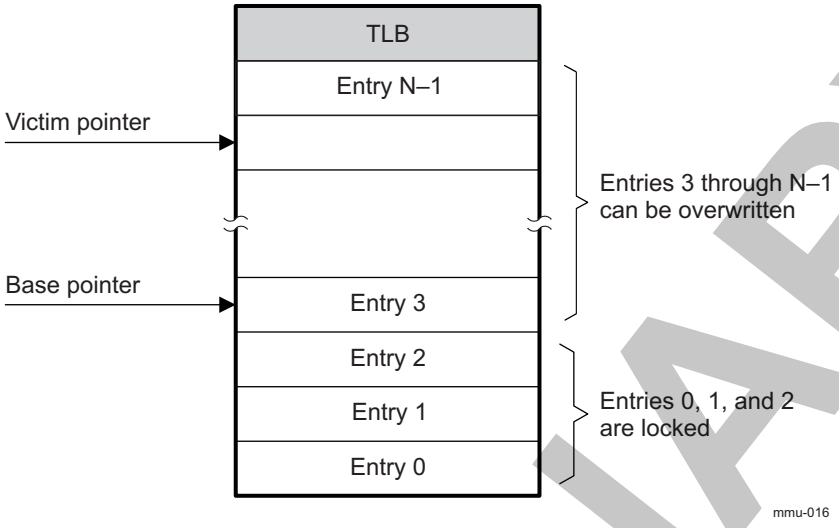
Figure 20-14. TLB Entry Lock Mechanism



The table walking logic automatically writes the TLB entries. The entries can also be manually written, which is done typically to ensure that the translation of time-critical data accesses is already present in the TLB so that they execute as fast as possible. The entries must be locked to prevent them from being overwritten.

20.3.1.3.1 TLB Entry Format

TLB entries consist of two parts:

- The CAM part contains the virtual address tag used to determine if a virtual address translation is in the TLB. The TLB acts like a fully associative cache addressed by the virtual address tag. The CAM part also contains the section/page size, as well as the preserved and the valid parameters. See the MMU_CAM register table for more details.
- The RAM part contains the address translation that belongs to the virtual address tag as well as the endianness, element size, and mixed parameters described in Section 20.3.1.2.2, *First-Level Translation Table*. See the MMU_RAM register table for more details.

The valid parameter specifies whether an entry is valid or not. The preserved parameter determines the behavior of an entry in the event of a TLB flush. If an entry is set as preserved, it is not deleted when a TLB is flushed, that is, when MMU_GFLUSH[0] GLOBALFLUSH is set to 1. Preserved entries must be deleted manually. Section 20.3.1.2.2 describes the procedure to delete TLB entries.

Figure 20-16 shows the TLB entry structure.

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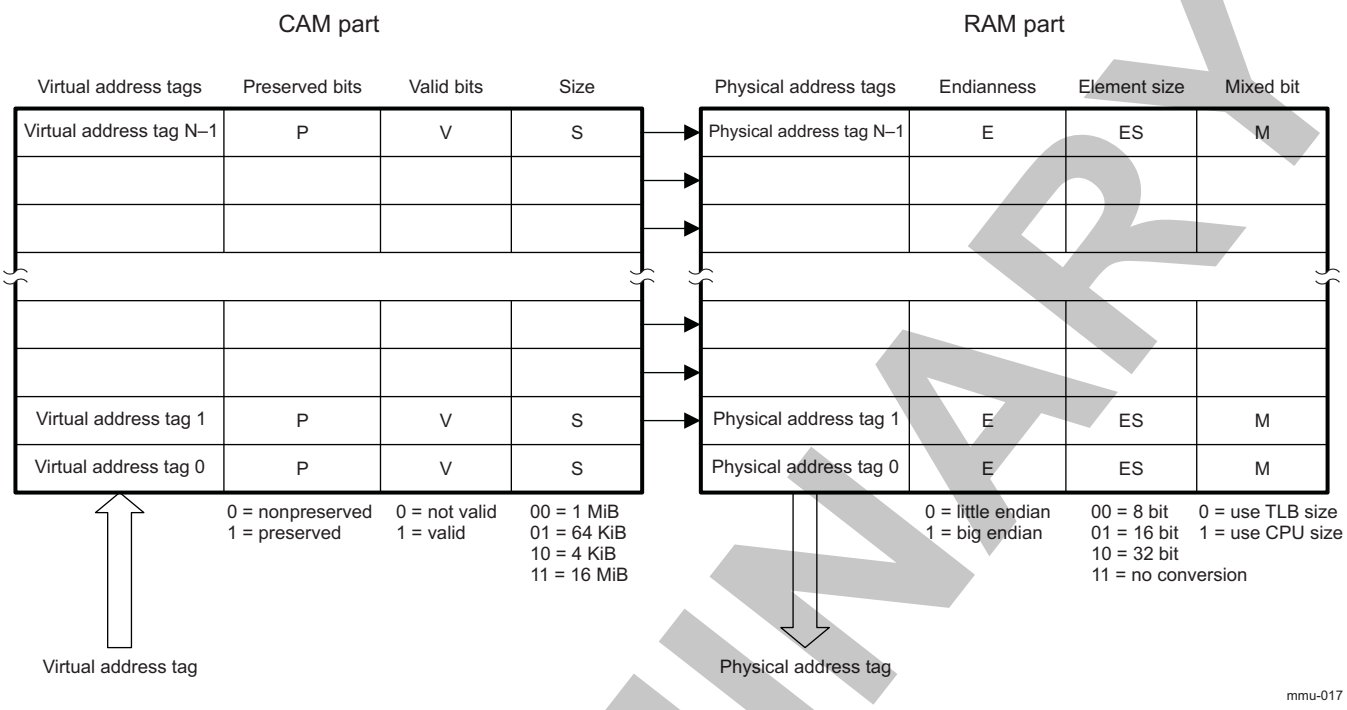
Figure 20-15. TLB Entry Structure



20.3.2 MMU Clock Configuration

There are two clock domains: The functional clock domain for the MMU, which is synchronous to the clock for the interconnect slave and master access ports; and the clock domain for the interconnect slave configuration port. As these clocks are matched, there is a single input clock with enables for each of the clock domains. If a clock domain should run at the same frequency as the input clock, that enable can be tied high.

Two clock enable signals exist, one to enable the interconnect data master and slave ports, and the other to enable the clock on the configuration L3_MAIN interconnect port. The clock signals are configured through the MMU_SYSCONFIG register. This is a system configuration register that controls the various parameters of the L3_MAIN interface.

20.3.3 MMU Software Reset

This section describes the software reset feature of the module. The MMU instances are reset together with their respective reset domains. See Table 20-2 for information about the reset domains of the different MMU instances.

To perform a software reset, write 1 in the MMU_SYSCONFIG[1] SOFTRESET bit. The MMU_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is 1. When the software reset completes, the MMU_SYSCONFIG[1] SOFTRESET bit is automatically reset. The software must ensure that the software reset completes before doing MMU operations. When an MMU instance is released from reset, its TLB is empty and the MMU is disabled.

20.3.4 MMU Power Management

As part of the device system-wide power management scheme, each MMU instance supports a communication protocol with the PRCM module that allows the PRCM module to request an MMU instance to enter a low-power state. When the MMU instance acknowledges a low-power mode request from the PRCM module, the clock to the instance is gated off at the PRCM clock generator. Because the clock is disabled at the source, the low-power mode offers lower power consumption than the internal clock gating method in the local power management.

Table 20-6 describes the power-management features available for the MMU modules.

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NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see Clock Management, in *Power, Reset, and Clock Management* chapter.
- For descriptions of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Module-Level Clock Management, in *Power, Reset, and Clock Management* chapter.

Table 20-6. MMU Local Power Management Features

Feature	Register
Idle modes	MMU_SYSCONFIG[4:3] IDLEMODE
Clock activity	MMU_SYSCONFIG[9:8] CLOCKACTIVITY
Clock autogating	MMU_SYSCONFIG[0] AUTOIDLE

NOTE: The MMU_SYSCONFIG[9:8] CLOCKACTIVITY bits are read only.

20.3.5 MMU Interrupt Requests

Table 20-7 lists the event flags and their masks that can cause module interrupts.

Table 20-7. Events

Event Flag	Event Mask	Synchronous	Sensitivity	Map to	Description
MMU_IRQSTATUS[4] MULTIHITFAULT	MMU_IRQENABLE[4] MULTIHITFAULT	Yes	Level	IPU_IRQ_16	Error in the L2 MMU due to multiple matches in the TLB
MMU_IRQSTATUS[3] TABLEWALKFAULT	MMU_IRQENABLE[3] TABLEWALKFAULT	Yes	Level	IPU_IRQ_16	Error in the L2 MMU due to error response received during a Table Walk
MMU_IRQSTATUS[2] EMUMISS	MMU_IRQENABLE[2] EMUMISS				For more information about emulation and debug features, see Chapter 29, *On-Chip Debug Support*.
MMU_IRQSTATUS[1] TRANSLATIONFAULT	MMU_IRQENABLE[1] TRANSLATIONFAULT	Yes	Level	IPU_IRQ_16	Error in the L2 MMU due to invalid descriptor in the translation tables (translation fault)
MMU_IRQSTATUS[0] TLBMISS	MMU_IRQENABLE[0] TLBMISS	Yes	Level	IPU_IRQ_16	Error in L2 MMU due to unrecoverable TLB miss (hardware TWL disabled)

20.3.6 MMU Error Handling

Table 20-8 summarizes the intended operation for real and potential error conditions.

Table 20-8. Error Handling

Item	Condition	Action
1	Table-walk read has an error response.	Treat generally the same as a translation fault, but set the TableWalkFault interrupt status bit to aid in diagnosis
2	MMU is disabled during table-walk.	Not permitted; can result in loss of the current transaction but must not deadlock the MMU.
		Avoid this condition by first disabling the table-walk logic and then polling the TWLRunning bit to ensure that no table walk is pending
3	MMU is disabled during an address translation.	Not permitted; can result in access to an unintended location, but must not deadlock MMU.
		This condition should be avoided by ensuring that no accesses are pending.
4	TLB is accessed during an address translation or a table walk.	Reading permitted; write should be done with care to ensure that the TLB is self-consistent at all times that a translation can occur.

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Table 20-8. Error Handling (continued)

Item	Condition	Action
5	TLB is flushed during address translation or a table walk.	Permitted; the flush is processed first, followed by the TWL update.
6	MMU is disabled while an interrupt is pending.	Not permitted; all pending interrupts should be processed before disabling the MMU.

L3_MAIN Interconnect configuration port: Accesses to undecoded register addresses must not give an error response.

To protect against changes to the address translation between a READEX and the corresponding write or during a burst the following configuration operations are protected against writes during these processes:

- TLB update
- Global flush
- Flush entry
- MMU disable

The protection is implemented by stalling the configuration interconnect transaction until the write can proceed safely.

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20.4 MMU Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the module.

20.4.1 Global Initialization

20.4.1.1 Surrounding Modules Global Initialization

This section identifies the requirements of initializing the surrounding modules when the MMU module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MMU. For more information, see Section Section 20.2, *MMU Module Integration* .

Table 20-9. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. For more information, see Power, Reset, and Clock Management chapter.
(optional) INTC_MPU or INTC_DSP or INTC_IPU	MPU, DSP, and IPU interrupt controller configuration must be done to enable the interrupts from module.
Interconnect	For more information about the L3_MAIN interconnect configuration, see L3 Interconnect.

NOTE: If the interrupt-based communication mode is used, the MPU, DSP, and IPU interrupt controllers configurations are required.

20.4.1.2 MMU Global Initialization

20.4.1.2.1 Main Sequence - MMU Global Initialization

Figure 20-16 shows the procedure to initialize the MMU after a power-on or software reset.

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Figure 20-16. MMU Global Initialization

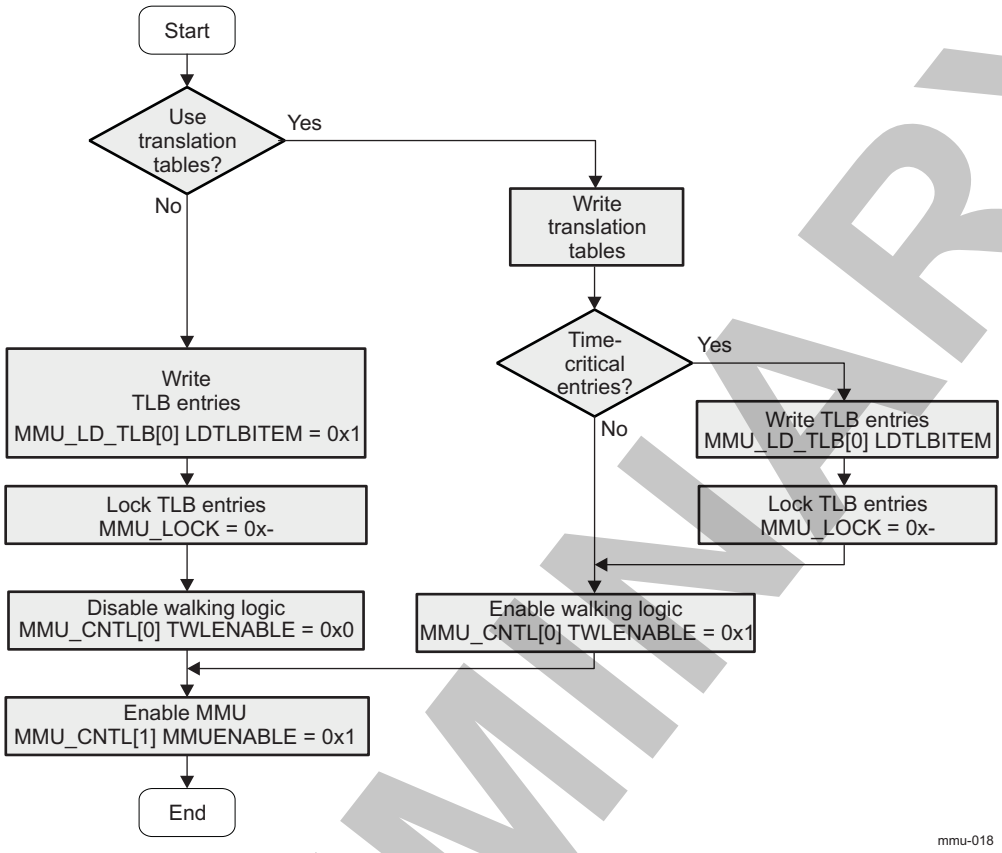

Table 20-10. Register Call Summary for Main Sequence - MMU Global Initialization

Register Name	Register Name	Register Name
MMU_LD_TLB	MMU_LOCK	MMU_CNTL

20.4.1.2.2 Subsequence - Configure a TLB entry

Table 20-11. Configure a TLB Entry

Step	Register / Bit Field / Programming Model	Value
Load the Virtual Address Tag	MMU_CAM[31:12] VATAG	0x-
Protect the TLB entry against flush	MMU_CAM[3] P	0x1
Validate the TLB entry	MMU_CAM[2] V	0x1
Define the page size	MMU_CAM[1:0] PAGESIZE	0x-

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20.4.1.3 Operational Modes Configuration

20.4.1.3.1 Main Sequence - Writing TLB Entries Statically

Writing TLB entries statically avoids the need to write translation tables in memory and is commonly used for relatively small address spaces. This method ensures that the translation of time-critical data accesses execute as fast as possible with entries already present in the TLB. These entries must be locked to prevent them from being overwritten.

Table 20-12. MMU Writing TLB Entries Statically

Step	Register/ Bit Field / Programming Model	Value
Execute software reset	MMU_SYSCONFIG[1] SOFTRESET	0x1
Wait for reset to complete	MMU_SYSSTATUS[0] RESETDONE	=0x1
Enable power saving via automatic interface clock gating	MMU_SYSCONFIG[0] AUTOIDLE	0x1
Configure TLB entries	See Table 20-11	
Load the physical Address of the page	MMU_RAM[31:12] PHYSICALADDRESS	0x-
Define the endianness of the page (little endian or big endian)	MMU_RAM[9] ENDIANNESS	0x-
Select the element size	MMU_RAM[8:7] ELEMENTSIZE	0x-
Define mixed page attribute	MMU_RAM[6] MIXED	0x-
Specify the TLB entry you want to write	MMU_LOCK[8:4] CURRENTVICTIM	0x-
Load the specified entry in the TLB	MMU_LD_TLB[0] LDTLBITEM	0x1
Enable multihit fault and TLB miss	MMU_IRQENABLE[4] MULTIHITFAULT	0x1
	MMU_IRQENABLE[0] TLBMISS	0x1
Enable memory translations	MMU_CNTL[1] MMUENABLE	0x1

20.4.1.3.2 Main Sequence - Protecting TLB Entries

The first *n* TLB entries (with *n* < total number of TLB entries) can be protected from being overwritten with new translations. This is useful to ensure that certain commonly used or time-critical translations are always in the TLB and do not require retrieval using the table walking process.

Table 20-13. Protecting TLB Entries

Step	Registe/Bit Field/Programming Model	Value
Locks the TLB entries	MMU_LOCK[14:10] BASEVALUE	0x-

20.4.1.3.3 Main Sequence - Deleting TLB Entries

Two mechanisms exist to delete TLB entries. All unpreserved TLB entries, that is, TLB entries written with the preserved bit set to zero, can be deleted by invoking a TLB flush. The preserved bit should only be used on protected TLB entries, as it does not prevent replacement by the table walking logic.

Table 20-14. Deleting TLB Entries

Step	Registet / Bit Field / Programming Model	Value
Flush all nonprotected TLB entries	MMU_GFLUSH[0] GLOBALFLUSH	0x1
Flush all TLB entries specified by the CAM register	MMU_FLUSH_ENTRY[0] FLUSHENTRY	0x1

20.4.1.3.4 Main Sequence - Read TLB Entries

TLB entries can be read by the programmer to determine the TLB content at runtime.

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Table 20-15. Read TLB Entries

Step	Register / Bit Field / Programming Model	Value
Set the current victim pointer	MMU_LOCK[8:4] CURRENTVICTIM	0x-
Read RAM parts of the TLB entry	MMU_READ_RAM	
Read CAM parts of the TLB entry	MMU_READ_CAM	

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20.5 MMU Register Manual

20.5.1 MMU Instance Summary

Table 20-16. MMU Instance Summary

Module Name	Base Address	Size
MMU_IPU	0x5508 2000	4 KiB
MMU_DSP	0x4A06 6000	4 KiB

20.5.2 MMU Registers

20.5.2.1 MMU Register Summary

Table 20-17. MMU Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MMU_IPU Physical Address	MMU_DSP Physical Address
MMU_REVISION	R	32	0x0000 0000	0x5508 2000	0x4A06 6000
MMU_SYSCONFIG	RW	32	0x0000 0010	0x5508 2010	0x4A06 6010
MMU_SYSSTATUS	R	32	0x0000 0014	0x5508 2014	0x4A06 6014
MMU_IRQSTATUS	RW	32	0x0000 0018	0x5508 2018	0x4A06 6018
MMU_IRQENABLE	RW	32	0x0000 001C	0x5508 201C	0x4A06 601C
MMU_WALKING_ST	R	32	0x0000 0040	0x5508 2040	0x4A06 6040
MMU_CNTL	RW	32	0x0000 0044	0x5508 2044	0x4A06 6044
MMU_FAULT_AD	R	32	0x0000 0048	0x5508 2048	0x4A06 6048
MMU_TTB	RW	32	0x0000 004C	0x5508 204C	0x4A06 604C
MMU_LOCK	RW	32	0x0000 0050	0x5508 2050	0x4A06 6050
MMU_LD_TLB	RW	32	0x0000 0054	0x5508 2054	0x4A06 6054
MMU_CAM	RW	32	0x0000 0058	0x5508 2058	0x4A06 6058
MMU_RAM	RW	32	0x0000 005C	0x5508 205C	0x4A06 605C
MMU_GFLUSH	RW	32	0x0000 0060	0x5508 2060	0x4A06 6060
MMU_FLUSH_ENTRY	RW	32	0x0000 0064	0x5508 2064	0x4A06 6064
MMU_READ_CAM	R	32	0x0000 0068	0x5508 2068	0x4A06 6068
MMU_READ_RAM	R	32	0x0000 006C	0x5508 206C	0x4A06 606C
MMU_EMU_FAULT_AD	R	32	0x0000 0070	0x5508 2070	0x4A06 6070
MMU_FAULT_PC	R	32	0x0000 0080	0x5508 2080	0x4A06 6080
MMU_FAULT_STATUS	RW	32	0x0000 0084	0x5508 2084	0x4A06 6084
MMU_GP_REG	RW	32	0x0000 0088	0x5508 2088	N/A
DSPSS_MMU_GPR	RW	32	0x0000 0088	N/A	0x4A06 6088

NOTE: MMU_IRQENABLE, MMU_CNTL and MMU_TTB registers have retention capabilities. For more information about the device retention state management, see Chapter 3, *Power, Reset, and Clock Management*.

20.5.2.2 MMU Register Description

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Table 20-18. MMU_REVISION

Address Offset	0x0000 0000		
Physical Address	0x5508 2000 0x4A06 6000	**Instance**	MMU_IPU MMU_DSP
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See (1)

(1) TI internal data

Table 20-19. Register Call Summary for Register MMU_REVISION

MMU Register Manual

- MMU Register Summary: [0]

Table 20-20. MMU_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x5508 2010 0x4A06 6010	**Instance**	MMU_IPU MMU_DSP
Description	This register controls the various parameters of the OCP interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED			IDLEMODE		RESERVED	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Write 0's for future compatibility Reads returns 0	R	0x000000
9:8	CLOCKACTIVITY	Clock activity during wake-up mode 00 Functional and Interconnect clocks can be switched off	R	0x0
7:5	RESERVED	Write 0's for future compatibility Reads returns 0	R	0x0
4:3	IDLEMODE	IdleMode 0x0: Force-idle. An idle request is acknowledged unconditionally 0x1: No-idle. An idle request is never acknowledged 0x2: Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module 0x3: reserved do not use	RW	0x0
2	RESERVED	Write 0's for future compatibility Reads returns 0	R	0

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Bits	Field Name	Description	Type	Reset
1	SOFTRESET	Software reset. This bit is automatically reset by the hardware. During reads, it always return 0 Read 0x0: always return 0 Write 0x0: no functional effect Write 0x1: The module is reset Read 0x1: never happens	RW	0
0	AUTOIDLE	Internal interconnect clock gating strategy 0x0: Interconnect clock is free-running 0x1: Automatic interconnect clock gating strategy is applied, based on the interconnect interface activity	RW	0

Table 20-21. Register Call Summary for Register MMU_SYSCONFIG

MMU Functional Description • MMU Clock Configuration: [0] • MMU Software Reset: [1] [2] • MMU Power Management: [3] [4] [5] [6]
MMU Low-level Programming Models • Main Sequence - Writing TLB Entries Statically: [7] [8]
MMU Register Manual • MMU Register Summary: [9]

Table 20-22. MMU_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x5508 2014 0x4A06 6014	**Instance**	MMU_IPU MMU_DSP
Description	This register provides status information about the module, excluding the interrupt status information		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0	R	0x000000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset in on-going Read 0x1: Reset completed	R	-

Table 20-23. Register Call Summary for Register MMU_SYSSTATUS

MMU Functional Description • MMU Software Reset: [0]
MMU Low-level Programming Models • Main Sequence - Writing TLB Entries Statically: [1]
MMU Register Manual • MMU Register Summary: [2]

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Table 20-24. MMU_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x5508 2018 0x4A06 6018	**Instance**	MMU_IPU MMU_DSP
Description	This interrupt status register regroups all the status of the module internal events that can generate an interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MULTIHITFAULT	TABLEWALKFAULT	EMUMISS	TRANSLATIONFAULT	TLBMISS

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Write 0's for future compatibility read returns 0	R	0x0000000
4	MULTIHITFAULT	Error due to multiple matches in the TLB Read 0x0: MultiHitFault false Write 0x0: MultiHitFault status bit unchanged Write 0x1: MultiHitFault status bit is reset Read 0x1: MultiHitFault is true ('pending')	RW W1toClr	0
3	TABLEWALKFAULT	Error response received during a Table Walk Read 0x0: TableWalkFault false Write 0x0: TableWalkFault status bit unchanged Write 0x1: TableWalkFault status bit is reset Read 0x1: TableWalkFault is true ('pending')	RW W1toClr	0
2	EMUMISS	Unrecoverable TLB miss during debug (hardware TWL disabled) Read 0x0: EMUMiss false Write 0x0: EMUMiss status bit unchanged Write 0x1: EMUMiss status bit is reset Read 0x1: EMUMiss is true ('pending')	RW W1toClr	0
1	TRANSLATIONFAULT	Invalid descriptor in translation tables (translation fault) Read 0x0: TranslationFault false Write 0x0: TranslationFault status bit unchanged Write 0x1: TranslationFault status bit is reset Read 0x1: TranslationFault is true ('pending')	RW W1toClr	0
0	TLBMISS	Unrecoverable TLB miss (hardware TWL disabled) Read 0x0: TLBMiss false Write 0x0: TLBMiss status bit unchanged Write 0x1: TLBMiss status bit is reset Read 0x1: TLBMiss is true ('pending')	RW W1toClr	0

Table 20-25. Register Call Summary for Register MMU_IRQSTATUS

MMU Functional Description
- MMU Interrupt Requests: [0] [1] [2] [3] [4]

MMU Register Manual
- MMU Register Summary: [5]

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Table 20-26. MMU_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x5508 201C 0x4A06 601C	**Instance**	MMU_IPU MMU_DSP
Description	The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on a event-by-event basis.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											MULTIHITFAULT	TABLEWALKFAULT	EMUMISS	TRANSLATIONFAULT	TLBMISS

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Write 0's for future compatibility Read returns 0	R	0x0000000
4	MULTIHITFAULT	Error due to multiple matches in the TLB 0x0: MultiHitFault is masked 0x1: MultiHitFault event generates an interrupt if occurs	RW	0
3	TABLEWALKFAULT	Error response received during a Table Walk 0x0: TableWalkFault is masked 0x1: TableWalkFault event generates an interrupt if occurs	RW	0
2	EMUMISS	Unrecoverable TLB miss during debug (hardware TWL disabled) 0x0: EMUMiss interrupt is masked 0x1: EMUMiss event generates an interrupt when it occurs	RW	0
1	TRANSLATIONFAULT	Invalid descriptor in translation tables (translation fault) 0x0: TranslationFault is masked 0x1: TranslationFault event generates an interrupt if occurs	RW	0
0	TLBMISS	Unrecoverable TLB miss (hardware TWL disabled) 0x0: TLBMiss interrupt is masked 0x1: TLBMiss event generates an interrupt when if occurs	RW	0

Table 20-27. Register Call Summary for Register MMU_IRQENABLE

MMU Functional Description
- MMU Interrupt Requests: [0] [1] [2] [3] [4]

MMU Low-level Programming Models
- Main Sequence - Writing TLB Entries Statically: [5] [6]

MMU Register Manual
- MMU Register Summary: [7] [8]

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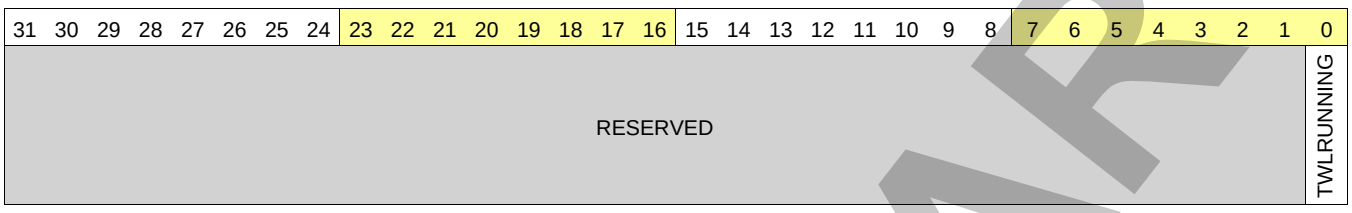
Table 20-28. MMU_WALKING_ST

Address Offset	0x0000 0040		
Physical Address	0x5508 2040 0x4A06 6040	**Instance**	MMU_IPU MMU_DSP
Description	This register provides status information about the table walking logic		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return 0	R	0x0000 0000
0	TWLRUNNING	Table Walking Logic is running Read 0x0: TWL Completed Read 0x1: TWL Running	R	0

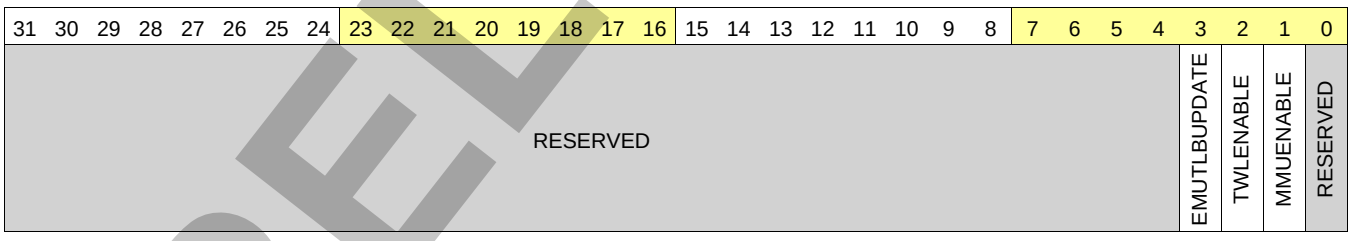
Table 20-29. Register Call Summary for Register MMU_WALKING_ST

MMU Register Manual

- MMU Register Summary: [0]

Table 20-30. MMU_CNTL

Address Offset	0x0000 0044		
Physical Address	0x5508 2044 0x4A06 6044	**Instance**	MMU_IPU MMU_DSP
Description	This register programs the MMU features		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Write 0's for future compatibility Reads return 0	R	0x0000000
3	EMUTLBUPDATE	Enable TLB update on emulator table walk 0x0: Emulator TLB update disabled 0x1: Emulator TLB update enabled	RW	0
2	TWLENABLE	Table Walking Logic enable 0x0: TWL disabled 0x1: TWL enabled	RW	0
1	MMUENABLE	MMU enable 0x0: MMU disabled 0x1: MMU enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	RESERVED	Write 0's for future compatibility Reads return 0	R	0

Table 20-31. Register Call Summary for Register MMU_CNTL

MMU Low-level Programming Models
- Main Sequence - MMU Global Initialization: [0]
- Main Sequence - Writing TLB Entries Statically: [1]

MMU Register Manual
- MMU Register Summary: [2] [3]

Table 20-32. MMU_FAULT_AD

Address Offset	0x0000 0048		
Physical Address	0x5508 2048 0x4A06 6048	**Instance**	MMU_IPU MMU_DSP
Description	This register contains the virtual address that generated the interrupt		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULTADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	FAULTADDRESS	Virtual address of the access that generated a fault	R	0x0000 0000

Table 20-33. Register Call Summary for Register MMU_FAULT_AD

MMU Register Manual
- MMU Register Summary: [0]

Table 20-34. MMU_TTB

Address Offset	0x0000 004C		
Physical Address	0x5508 204C 0x4A06 604C	**Instance**	MMU_IPU MMU_DSP
Description	This register contains the Translation Table Base address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTBADDRESS																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:7	TTBADDRESS	Translation Table Base Address	RW	0x0000000
6:0	RESERVED	Write 0's for future compatibility Reads retiurn 0	R	0x00

Table 20-35. Register Call Summary for Register MMU_TTB

MMU Register Manual
- MMU Register Summary: [0] [1]

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Table 20-36. MMU_LOCK

Address Offset	0x0000 0050		
Physical Address	0x5508 2050 0x4A06 6050	**Instance**	MMU_IPU MMU_DSP
Description	This register locks some of the TLB entries		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASEVALUE						RESERVED		CURRENTVICTIM				RESERVED			

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Write 0's for future compatibility Reads return 0	R	0x00000
14:10	BASEVALUE	Locked entries base value	RW	0x00
9	RESERVED	Write 0's for future compatibility Read returns 0	R	0
8:4	CURRENTVICTIM	Current entry to be updated either by the TWL or by the software Write value : TLB entry to be updated by software, Read value : TLB entry that will be updated by table walk logic	RW	0x00
3:0	RESERVED	Write 0's for future compatibility Reads return 0	R	0x0

Table 20-37. Register Call Summary for Register MMU_LOCK

MMU Low-level Programming Models

- Main Sequence - MMU Global Initialization: [0]
- Main Sequence - Writing TLB Entries Statically: [1]
- Main Sequence - Protecting TLB Entries: [2]
- Main Sequence - Read TLB Entries: [3]

MMU Register Manual

- MMU Register Summary: [4]

Table 20-38. MMU_LD_TLB

Address Offset	0x0000 0054		
Physical Address	0x5508 2054 0x4A06 6054	**Instance**	MMU_IPU MMU_DSP
Description	This register loads a TLB entry (CAM+RAM)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															LDTLBITEM

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility Reads return 0	RW	0x0000 0000
0	LDTLBITEM	Write (load) data in the TLB Read 0x0: always return 0 Write 0x0: no functional effect Write 0x1: load TLB data Read 0x1: never happens	RW	0

Table 20-39. Register Call Summary for Register MMU_LD_TLB

MMU Low-level Programming Models • Main Sequence - MMU Global Initialization: [0] • Main Sequence - Writing TLB Entries Statically: [1]
MMU Register Manual • MMU Register Summary: [2]

Table 20-40. MMU_CAM

Address Offset	0x0000 0058		
Physical Address	0x5508 2058 0x4A06 6058	**Instance**	MMU_IPU MMU_DSP
Description	This register holds a CAM entry		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VATAG																RESERVED								P	V	PAGESIZE					

Bits	Field Name	Description	Type	Reset
31:12	VATAG	Virtual address tag	RW	0x00000
11:4	RESERVED	Write 0's for future compatibility Reads return 0	R	0x00
3	P	Preserved bit 0x0: TLB entry may be flushed 0x1: TLB entry is protected against flush	RW	0
2	V	Valid bit 0x0: TLB entry is invalid 0x1: TLB entry is valid	RW	0
1:0	PAGESIZE	Page size 0x0: Section (1 MiB) 0x1: Large page (64 KiB) 0x2: Small page (4 KiB) 0x3: Supersection (16 MiB)	RW	0x0

Table 20-41. Register Call Summary for Register MMU_CAM

MMU Functional Description • TLB Entry Format: [0]
MMU Low-level Programming Models • Subsequence - Configure a TLB entry: [1] [2] [3] [4]
MMU Register Manual • MMU Register Summary: [5] • MMU Register Description: [6]

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Table 20-42. MMU_RAM

Address Offset	0x0000 005C		
Physical Address	0x5508 205C 0x4A06 605C	**Instance**	MMU_IPU MMU_DSP
Description	This register holds a RAM entry		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICALADDRESS																				RESERVED		ENDIANNESS		ELEMENTSIZE		MIXED	RESERVED					

Bits	Field Name	Description	Type	Reset
31:12	PHYSICALADDRESS	Physical address of the page	RW	0x00000
11:10	RESERVED	Write 0's for future compatibility Reads return 0	R	0x0
9	ENDIANNESS	Endianness of the page 0x0: Little Endian 0x1: Big endian	RW	0
8:7	ELEMENTSIZE	Element size of the page (8, 16, 32, no translation) 0x0: 8-bits 0x1: 16-bits 0x2: 32-bits 0x3: No translation	RW	0x0
6	MIXED	Mixed page attribute (use CPU element size) 0x0: Use TLB element size 0x1: Use CPU element size	RW	0
5:0	RESERVED	Write 0's for future compatibility Reads return 0	R	0x00

Table 20-43. Register Call Summary for Register MMU_RAM

MMU Functional Description • TLB Entry Format: [0]
MMU Low-level Programming Models • Main Sequence - Writing TLB Entries Statically: [1] [2] [3] [4]
MMU Register Manual • MMU Register Summary: [5]

Table 20-44. MMU_GFLUSH

Address Offset	0x0000 0060		
Physical Address	0x5508 2060 0x4A06 6060	**Instance**	MMU_IPU MMU_DSP
Description	This register flushes all the non-protected TLB entries		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															GLOBALFLUSH

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility Reads return 0	RW	0x0000 0000
0	GLOBALFLUSH	Flush all the non-protected TLB entries when set Read 0x0: always return 0 Write 0x0: no functional effect Write 0x1: flush all the non-protected TLB entries Read 0x1: never happens	RW	0

Table 20-45. Register Call Summary for Register MMU_GFLUSH

MMU Functional Description • TLB Entry Format: [0]
MMU Low-level Programming Models • Main Sequence - Deleting TLB Entries: [1]
MMU Register Manual • MMU Register Summary: [2]

Table 20-46. MMU_FLUSH_ENTRY

Address Offset	0x0000 0064		
Physical Address	0x5508 2064 0x4A06 6064	**Instance**	MMU_IPU MMU_DSP
Description	This register flushes the entry pointed to by the CAM virtual address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															FLUSHENTRY

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Write 0's for future compatibility Reads return 0	RW	0x0000 0000
0	FLUSHENTRY	Flush the TLB entry pointed by the virtual address (VATag) in MMU_CAM register, even if this entry is set protected Read 0x0: always return 0 Write 0x0: no functional effect Write 0x1: flush all the TLB entries specified by the CAM register Read 0x1: never happens	RW	0

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Table 20-47. Register Call Summary for Register MMU_FLUSH_ENTRY

MMU Low-level Programming Models • Main Sequence - Deleting TLB Entries: [0]
MMU Register Manual • MMU Register Summary: [1]

Table 20-48. MMU_READ_CAM

Address Offset	0x0000 0068		
Physical Address	0x5508 2068 0x4A06 6068	**Instance**	MMU_IPU MMU_DSP
Description	This register reads CAM data from a CAM entry		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VATAG																RESERVED								P	V	PAGESIZE					

Bits	Field Name	Description	Type	Reset
31:12	VATAG	Virtual address tag	R	0x00000
11:4	RESERVED	Reads return 0	R	0x00
3	P	Preserved bit Read 0x0: TLB entry may be flushed Read 0x1: TLB entry is protected against flush	R	0
2	V	Valid bit Read 0x0: TLB entry is invalid Read 0x1: TLB entry is valid	R	0
1:0	PAGESIZE	Page size Read 0x0: Section (1 MiB) Read 0x1: Large page (64 KiB) Read 0x2: Small page (4 KiB) Read 0x3: Supersection (16 MiB)	R	0x0

Table 20-49. Register Call Summary for Register MMU_READ_CAM

MMU Low-level Programming Models • Main Sequence - Read TLB Entries: [0]
MMU Register Manual • MMU Register Summary: [1]

Table 20-50. MMU_READ_RAM

Address Offset	0x0000 006C		
Physical Address	0x5508 206C 0x4A06 606C	**Instance**	MMU_IPU MMU_DSP
Description	This register reads RAM data from a RAM entry		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSICALADDRESS																				RESERVED		ENDIANNESS	ELEMENTSIZE		MIXED	RESERVED						

Bits	Field Name	Description	Type	Reset
31:12	PHYSICALADDRESS	Physical address of the page	R	0x00000
11:10	RESERVED	Reads return 0	R	0x0
9	ENDIANNESS	Endianness of the page Read 0x0: Little Endian Read 0x1: Big endian	R	0
8:7	ELEMENTSIZE	Element size of the page (8, 16, 32, no translation) Read 0x0: 8-bits Read 0x1: 16-bits Read 0x2: 32-bits Read 0x3: No translation	R	0x0
6	MIXED	Mixed page attribute (use CPU element size) Read 0x0: Use TLB element size Read 0x1: Use CPU element size	R	0
5:0	RESERVED	Reads return 0	R	0x00

Table 20-51. Register Call Summary for Register MMU_READ_RAM

MMU Low-level Programming Models
- Main Sequence - Read TLB Entries: [0]

MMU Register Manual
- MMU Register Summary: [1]

Table 20-52. MMU_EMU_FAULT_AD

Address Offset	0x0000 0070		
Physical Address	0x5508 2070 0x4A06 6070	**Instance**	MMU_IPU MMU_DSP
Description	This register contains the last virtual address of a fault caused by the debugger		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMUFAULTADDRESS																															

Bits	Field Name	Description	Type	Reset
31:0	EMUFAULTADDRESS	Virtual address of the last emulator access that generated a fault	R	0x0000 0000

Table 20-53. Register Call Summary for Register MMU_EMU_FAULT_AD

MMU Register Manual
- MMU Register Summary: [0]
- MMU Register Description: [1]

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Table 20-54. MMU_FAULT_PC

Address Offset	0x0000 0080		
Physical Address	0x5508 2080 0x4A06 6080	**Instance**	MMU_IPU MMU_DSP
Description	Capture first fault PC value, controlled by MMU_FAULT_STATUS[0] FAULTINDICATION. Notes: The address value is captured at MMU_EMU_FAULT_AD[31:0] EMUFAULTADDRESS. Data-Read-access : corresponding PC. Data-write-access : not perfect accuracy due to Posted-write. All this description is valid only for the DSP MMU. The Cortex-M3 L2 MMU always reads zero from this register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC																															

Bits	Field Name	Description	Type	Reset
31:0	PC	CPU program counter value where cause MMU fault	R	0x0000 0000

Table 20-55. Register Call Summary for Register MMU_FAULT_PC

MMU Register Manual

- MMU Register Summary: [0]

Table 20-56. MMU_FAULT_STATUS

Address Offset	0x0000 0084		
Physical Address	0x5508 2084 0x4A06 6084	**Instance**	MMU_IPU MMU_DSP
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MMU_FAULT_TRANS_ID				RD_WR	MMU_FAULT_TYPE		FAULTINDICATION

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:4	MMU_FAULT_TRANS_ID	Master ID who cause a fault Read 0x0: posted writes out of shared cache for MMU_IPU / DMA_DSP read port 1 for MMU_DSP Read 0x1: IPU_C0 processor I/D bus access for MMU_IPU / DMA_DSP read port 2 for MMU_DSP Read 0x2: IPU_C0 processor S bus access for MMU_IPU / DMA_DSP write port 1 for MMU_DSP Read 0x3: IPU_C1 processor I/D bus access for MMU_IPU / DMA_DSP write port 2 for MMU_DSP Read 0x4: IPU_C1 processor S bus access for MMU_IPU / shared cache Evictions/stores/Non-cacheable for MMU_DSP Read 0x5: reserved for MMU_IPU / shared cache request for Program/Data for MMU_DSP Read 0x6: reserved for MMU_IPU / shared cache request for DMA for MMU_DSP Read 0x7: reserved (for both MMU_IPU and MMU_DSP) Read 0x8: MMU hardware table walk (for both MMU_IPU and MMU_DSP) Read 0x9 to 0xF: reserved (for both MMU_IPU and MMU_DSP)	R	0x0
3	RD_WR	indicates read or write	R	0
2:1	MMU_FAULT_TYPE	MReq Type[1:0] Read 0x2: reserved for MMU_IPU / DMA address for MMU_DSP Read 0x1: Fetch address Read 0x0: Data Load/Store	R	0x0
0	FAULTINDICATION	indicates a MMU fault	RW W1toClr	0

Table 20-57. Register Call Summary for Register MMU_FAULT_STATUS

MMU Register Manual

- MMU Register Summary: [0]
- MMU Register Description: [1]

Table 20-58. MMU_GP_REG

Address Offset	0x0000 0088		
Physical Address	0x5508 2088	**Instance**	MMU_IPU
Description	Bus-error back response enable register. For more information about the register usage, see Section 7.3.5, *L2 MMU*, in Chapter 7, *Dual Cortex-M4 IPU Subsystem*.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															BUS_ERR_BACK_EN

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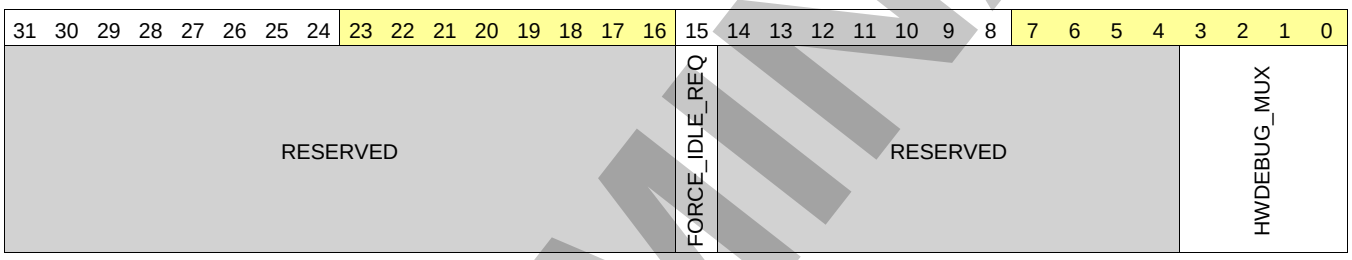
Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0
0	BUS_ERR_BACK_EN	Bus-error back response enable bit 0x0: Default behaviour for MMU page Faults 0x1: All MMU faults return bus-error back	RW	0x0

Table 20-59. Register Call Summary for Register MMU_GP_REG

MMU Register Manual
- MMU Register Summary: [0]

Table 20-60. DSPSS_MMU_GPR

Address Offset	0x0000 0088		
Physical Address	0x4A06 6088	**Instance**	MMU_DSP
Description	This register controls the MMU_DSP hardware debug output multiplexer. It also controls force-idle request generation. For more information about the use of this register, see Control Module chapter.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	FORCE_IDLE_REQ	Force-idle request to see existence of pending bus request. This bit must be used only for debug purposes, not in functional mode.	RW	0x0
14:4	RESERVED	Reserved	R	0x0
3:0	HWDEBUG_MUX	Control HWDEBUG output MUX	RW	0x0

Table 20-61. Register Call Summary for Register DSPSS_MMU_GPR

MMU Register Manual
- MMU Register Summary: [0]

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Spinlock

This chapter describes the Spinlock module of the device.

Topic **Page**

21.1 Spinlock Overview **4504**
21.2 Spinlock Integration **4505**
21.3 Spinlock Functional Description **4506**
21.4 Spinlock Programming Guide **4509**
21.5 Spinlock Register Manual **4512**

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21.1 Spinlock Overview

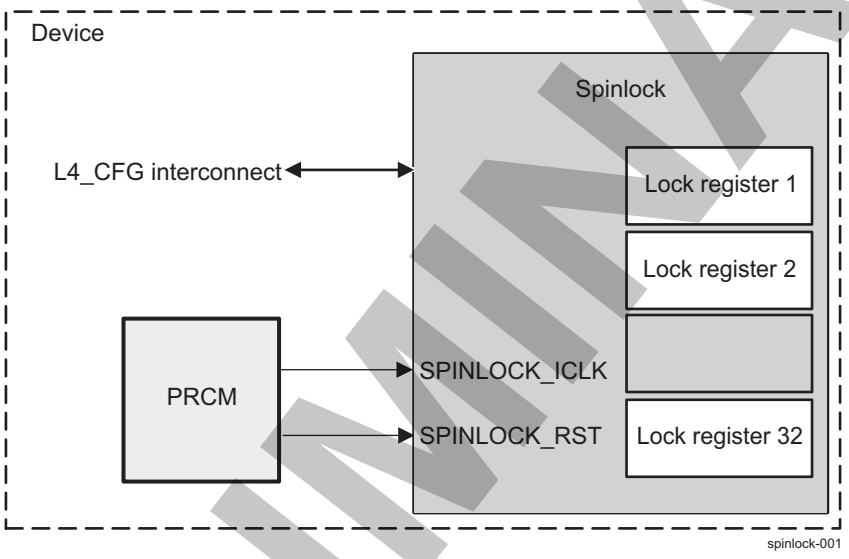
The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device:

- Dual Cortex™-A15 microprocessor unit (MPU) subsystem
- Digital signal processor (DSP) subsystem
- Dual Cortex-M4 image processing unit (IPU) subsystem

The Spinlock module implements 32 spinlocks (or hardware semaphores), which provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need of a read-modify-write bus transfer that the programmable cores are not capable of.

Figure 21-1 shows the Spinlock module.

Figure 21-1. Spinlock Overview



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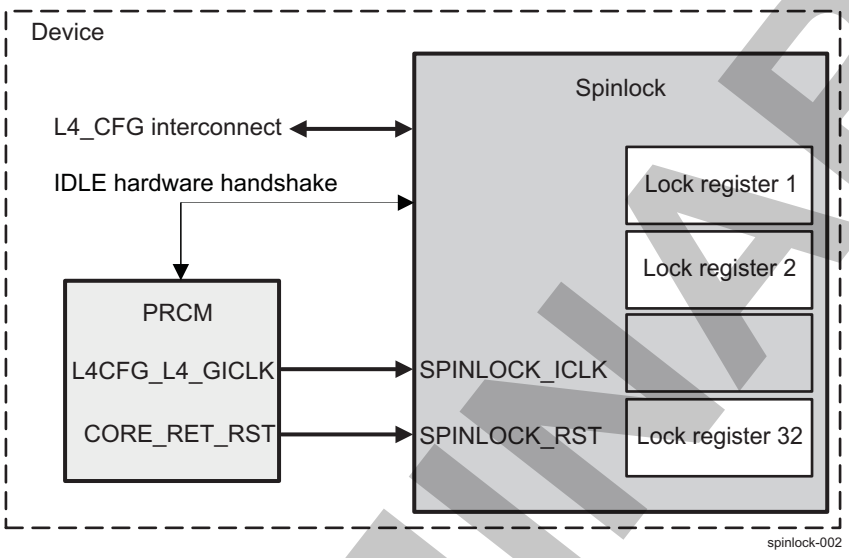
21.2 Spinlock Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 21-2 shows the Spinlock integration.

Figure 21-2. Spinlock Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Module-Level Clock Management, in *Power, Reset, and Clock Management* chapter.

Table 21-1 and Table 21-2 summarize the integration of the module in the device.

Table 21-1. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
SPINLOCK	PD_CORE	L4_CFG

Table 21-2. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SPINLOCK	SPINLOCK_ICLK	L4CFG_L4_GICLK	PRCM	Spinlock interface clock. This clock is used for all interface and functional operations.
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SPINLOCK	SPINLOCK_RST	CORE_RET_RST	PRCM	Spinlock hardware reset. This reset is asynchronously applied to the Spinlock internal registers.

NOTE: The Spinlock module does not support any interrupt and DMA requests.

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21.3 Spinlock Functional Description

21.3.1 Spinlock Software Reset

The Spinlock module can be reset by software through the SPINLOCK_SYSCONFIG[1] SOFTRESET bit. Setting this bit to 1 enables an active software reset that is functionally equivalent to a hardware reset. The SPINLOCK_SYSTATUS[0] RESETDONE bit can be polled to check the reset status (reading 1 indicates that reset sequence is done; reading 0 indicates that reset sequence is in progress). The software must ensure that the software reset completes before doing Spinlock operations.

21.3.2 Spinlock Power Management

Table 21-3 describes power-management features available to the Spinlock module.

NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see Clock Domain-Level Clock Management, in *Power, Reset, and Clock Management* chapter.
- For descriptions of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Module-Level Clock Management, in *Power, Reset, and Clock Management* chapter.

Table 21-3. Local Power Management Features

Feature	Registers	Description
Clock auto gating	SPINLOCK_SYSCONFIG[0] AUTOGATING bit	This bit indicates that the module uses an automatic internal interface clock gating strategy, based on interface activity.
Slave idle modes	SPINLOCK_SYSCONFIG[4:3] SIDLEMODE bit field	This bit field indicates that the module uses smart-idle mode.
Clock activity	SPINLOCK_SYSCONFIG[8] CLOCKACTIVITY bit	This bit indicates that the interface clock is not required by the module during idle mode and may be switched off.
Global wake-up enable	SPINLOCK_SYSCONFIG[2] ENAWAKEUP bit	This bit indicates that the wake-up generation feature (at module level) is disabled.

NOTE: All the local power management features are non-configurable (that is, their respective bits or bit fields are read-only).

CAUTION

The PRCM module has no hardware means of reading CLOCKACTIVITY settings. Thus, software must ensure consistent programming between the CLOCKACTIVITY bit and Spinlock clock PRCM control bits.

The Spinlock module is normally idle, except when processing a request from its slave interface port. The smart-idle mode acknowledges idle requests from the PRCM only when the module is prepared to go idle. The Spinlock module is always ready to go idle if it does not have any request that it is processing.

The Spinlock module uses retention flops to retain state including the Taken state of each lock register. This means that the module can be placed in retention at any time when it is not processing a request and it is known that the system will not need to access the module.

Software must ensure to only power off the Spinlock module when no locks would be lost. In general, the steps to powering down the Spinlock module are:

- Check that all masters which might use the Spinlock module are either:

  (a) Already powered off, or

  (b) Notified that Spinlock is not available and the notification is acknowledged.

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- If desired, check that no locks are currently held in the Spinlock module. The status of each bank of 32 locks can be read from the SPINLOCK_SYSTATUS register. If any locks are held, they are orphaned because they are not held by any master that is still active. Alternatively, you may decide to wait a timeout period to allow any active master to clean up its locks before powering down.
- The Spinlock module can now be powered off by writing the appropriate status to the PRCM.

In the case of powering off the whole system, these steps are unnecessary.

21.3.3 About Spinlocks

Spinlocks are present to solve the need for synchronization and mutual exclusion between heterogeneous processors and those not operating under a single, shared operating system. There is no alternative mechanism to accomplish these operations between processors in separate subsystems.

Spinlocks are not the best way to synchronize between tasks or threads on one CPU. Instead, spinlocks are for use in synchronization between different subsystems in the device that don't have any other means of hardware-based synchronization.

Spinlocks do not solve all system synchronization issues. They have limited applicability and should be used with care to implement higher level synchronization protocols.

A spinlock is appropriate for mutual exclusion for access to a shared data structure. It should be used only when:

1. The time to hold the lock is predictable and small (for example, a maximum hold time of less than 200 CPU cycles may be acceptable).
2. The locking task cannot be preempted, suspended, or interrupted while holding the lock (this would make the hold time large and unpredictable).
3. The lock is lightly contended, that is the chance of any other process (or processor) trying to acquire the lock while it is held is small.

If these conditions are met, then the locking code can retry a failed attempt to acquire the lock until success.

If the conditions are not met, then a spinlock is not a good candidate. One alternative is to use a spinlock for critical section control (engineered to meet the conditions) to implement a higher level semaphore that can support preemption, notification, timeout or other higher level properties.

21.3.4 Spinlock Functional Operation

The Spinlock module supports 32 spinlocks. It accepts only a single command at a time and processes the command fully before accepting the next command. A lock is requested by reading the SPINLOCK_LOCK_REG_i[0] TAKEN bit. There are two states: Taken (SPINLOCK_LOCK_REG_i[0] TAKEN = 1) or Not Taken (SPINLOCK_LOCK_REG_i[0] TAKEN = 0).

When the status of lock *i* (where i = 0 to 31) is Not Taken (free), a read from the SPINLOCK_LOCK_REG_i register returns 0 and sets the lock to Taken (locked). When the status of lock *i* is Taken, a read returns 1 and does not change the state of the lock.

A write to the SPINLOCK_LOCK_REG_i register does not change the state of lock, unless when writing 0 when the lock is in Taken state. By doing this, the requester frees the lock.

CAUTION

Only 32-bit reads and writes are supported.

Figure 21-3 shows the SPINLOCK_LOCK_REG_i register state diagram.

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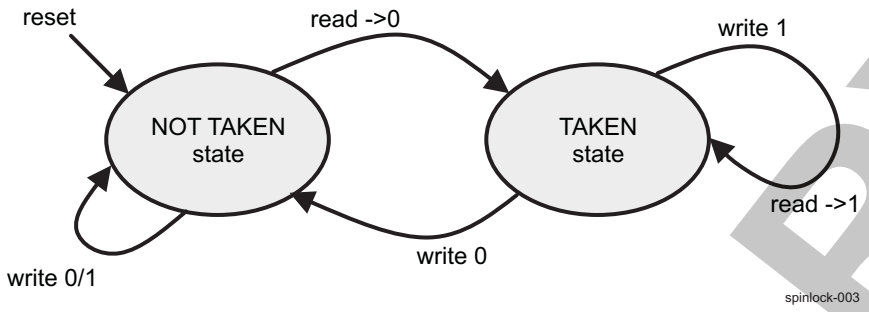
Figure 21-3. Lock Register State Diagram



NOTE:

- There is no support to ensure that a lock register is locked and unlocked by the same process. This must be ensured in software.
- There is no support to check that the same initiator that acquired the lock is the one that is freeing the lock.

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21.4 Spinlock Programming Guide

21.4.1 Spinlock Low-level Programming Models

This section covers the low-level hardware programming sequences for configuration and usage of the module.

21.4.1.1 Surrounding Modules Global Initialization

This procedure initializes the surrounding modules when the Spinlock module is used for the first time after a device reset.

Table 21-4. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Spinlock interface clock must be enabled. For more information, see CD_L4_CFG Clock Domain, in *Power, Reset, and Clock Management* chapter.
Interconnect	For more information about the L4_CFG interconnect configuration, see L4 Interconnects chapter.

21.4.1.2 Basic Spinlock Operations

The main spinlock operations are:

- Clear all the Taken spinlocks (only after a system bug recovery)
- Take a spinlock
- Release spinlock

21.4.1.2.1 Spinlocks Clearing After a System Bug Recovery

Module initialization (after reset) is not needed, except after system bug recovery. The following table presents the Spinlock initialization after a system bug recovery. Software should store 0 into each of the SPINLOCK_LOCK_REG_i registers at system startup to insure that all locks are initialized to Not Taken.

Table 21-5. Spinlock System Bug Recovery

Step	Register	Value
IF: SPINLOCK_SYSTATUS[0] IU0 = = 1?	SPINLOCK_SYSTATUS[0] IU0	
Free the 32 locks	SPINLOCK_LOCK_REG_i[0] TAKEN (i=0 to 31)	0x0
END		

21.4.1.2.2 Take and Release Spinlock

This procedure configures the take and release (free) operations for the Spinlock module. A spinlock should only be held with interrupts disabled. So, before attempting to obtain the spinlock, software should disable interrupts. Then it should read the SPINLOCK_LOCK_REG_i[0] TAKEN bit to attempt to obtain the lock. If it succeeds, it should proceed directly through the critical section then unlock and re-enable interrupts. If the acquisition attempt fails, the acquisition should be reattempted. To prevent unknown interrupt disabled time, interrupts should be re-enabled and then disabled before reattempting to acquire the lock. Figure 21-4 shows the described above procedure.

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Figure 21-4. Take and Release Spinlock

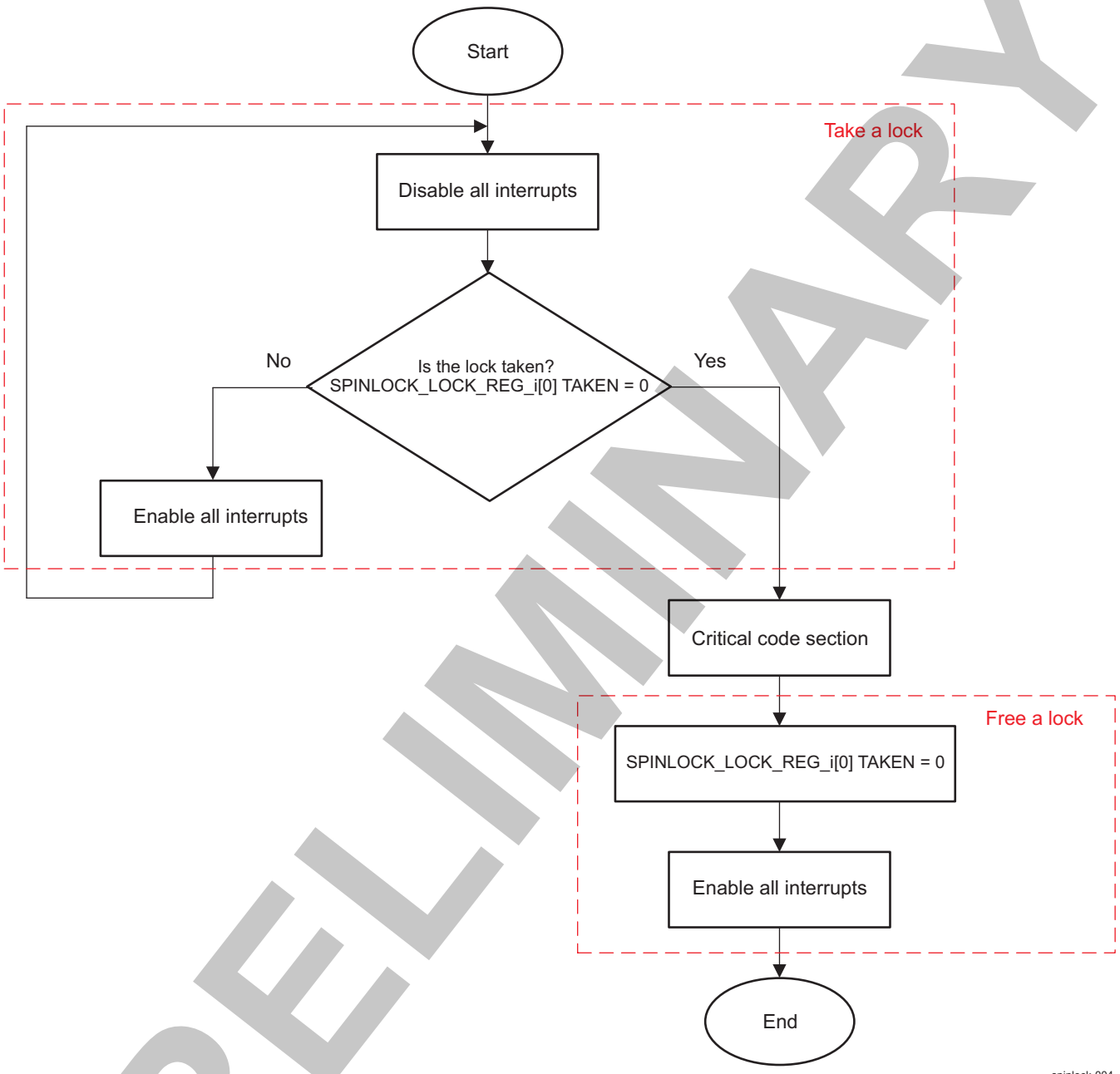

Table 21-6. Register Call Summary

Register Name
SPINLOCK_LOCK_REG_i[0] TAKEN

Table 21-7. Subprocess Call Summary

Subprocess Name	Cross Reference
Disable Interrupts	For information about disabling interrupts in INTC_MPU, see the ARM *Cortex-A15 MPCore Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp). For information about disabling interrupts in INTC_IPU, see the ARM *Cortex-M4 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp). For information about disabling interrupts in INTC_DSP, see DSP Subsystem chapter.

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Table 21-7. Subprocess Call Summary (continued)

Subprocess Name	Cross Reference
Enable Interrupts	For information about enabling interrupts in INTC_MPU, see the ARM *Cortex-A15 MPCore Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp). For information about enabling interrupts in INTC_IPU, see the ARM*Cortex-M4 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp). For information about enabling interrupts in INTC_DSP, see DSP Subsystem chapter.

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21.5 Spinlock Register Manual

21.5.1 Spinlock Instance Summary

Table 21-8. Spinlock Instance Summary

Module Name	Base Address	Size
Spinlock	0x4A0F 6000	4K bytes

21.5.2 Spinlock Registers

21.5.2.1 Spinlock Register Summary

Table 21-9. Spinlock Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Spinlock L4_CFG Base Address
SPINLOCK_REVISION	R	32	0x0000 0000	0x4A0F 6000
SPINLOCK_SYSCONFIG	RW	32	0x0000 0010	0x4A0F 6010
SPINLOCK_SYSTATUS	R	32	0x0000 0014	0x4A0F 6014
SPINLOCK_LOCK_REG_i [(1)]	RW	32	0x0000 0800 + (0x4 * i)	0x4A0F 6800 + (0x4 * i)

(1) i = 0 to 31

21.5.2.2 Spinlock Register Description

Table 21-10. SPINLOCK_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A0F 6000	**Instance**	Spinlock
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 21-11. Register Call Summary for Register SPINLOCK_REVISION

Spinlock Register Manual

- Spinlock Register Summary: [0]

Table 21-12. SPINLOCK_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A0F 6010	**Instance**	Spinlock
Description	This register controls the various parameters of the L4_CFG interface. Note that most fields are read-only.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLOCKACTIVITY	RESERVED			SIDLEMODE		ENWAKEUP	SOFTRESET	AUTOGATING

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved. Reads return 0.	R	0x000000
8	CLOCKACTIVITY	Indicates whether the module requires the interface clock when in IDLE mode. Read 0x0: Interface clock is not required by the module during IDLE mode and may be switched off. Read 0x1: Interface clock is required by the module, even during idle mode.	R	0
7:5	RESERVED	Reserved. Reads return 0.	R	0x0
4:3	SIDLEMODE	Slave interface power management (IDLE request/acknowledgement control). Read 0x0: Force-idle. IDLE request is acknowledged unconditionally and immediately. Read 0x1: No-idle. IDLE request is never acknowledged. Read 0x2: Smart-idle. IDLE request acknowledgement is based on the internal module activity. Read 0x3: Reserved. Do not use.	R	0x2
2	ENWAKEUP	Asynchronous wakeup gereration. Read 0x0: Wakeup generation is disabled. Read 0x1: Wakeup generation is enabled.	R	0
1	SOFTRESET	Module software reset. Write 0x0: No action Write 0x1: Start soft reset sequence	W	0
0	AUTOGATING	Internal interface clock gating strategy. Read 0x0: Interface clock is not gated when the L4_CFG interface is idle. Read 0x1: Automatic internal interface clock gating strategy is applied, based on the L4_CFG interface activity.	R	1

Table 21-13. Register Call Summary for Register SPINLOCK_SYSCONFIG

Spinlock Functional Description • Spinlock Software Reset: [0] • Spinlock Power Management: [1] [2] [3] [4]
Spinlock Register Manual • Spinlock Register Summary: [5]

Table 21-14. SPINLOCK_SYSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A0F 6014	**Instance**	Spinlock
Description	This register provides status information about this instance of the Spinlock module.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUMLOCKS								RESERVED								IU7	IU6	IU5	IU4	IU3	IU2	IU1	IU0	RESERVED							RESETDONE

Bits	Field Name	Description	Type	Reset
31:24	NUMLOCKS	Number of lock registers implemeted. Read 0x1: This instance has 32 lock registers. Read 0x2: This instance has 64 lock registers. Read 0x4: This instance has 128 lock registers. Read 0x8: This instance has 256 lock registers.	R	0x01
23:16	RESERVED	Reserved. Reads return 0.	R	0x00
15	IU7	In-Use flag 7. Reads always return 0.	R	0
14	IU6	In-Use flag 6. Reads always return 0.	R	0
13	IU5	In-Use flag 5. Reads always return 0.	R	0
12	IU4	In-Use flag 4. Reads always return 0.	R	0
11	IU3	In-Use flag 3. Reads always return 0.	R	0
10	IU2	In-Use flag 2. Reads always return 0.	R	0
9	IU1	In-Use flag 1. Reads always return 0.	R	0
8	IU0	In-Use flag 0, covering lock registers 0 - 31. Read 0x0: All lock registers 0 31 are in the Not Taken state. Read 0x1: At least one of the lock registers 0 31 is in the Taken state.	R	0
7:1	RESERVED	Reserved. Reads return 0.	R	0x00
0	RESETDONE	Reset done status. Read 0x0: Reset in progress. Read 0x1: Reset is completed.	R	1

Table 21-15. Register Call Summary for Register SPINLOCK_SYSTATUS

Spinlock Functional Description
- Spinlock Software Reset: [0]
- Spinlock Power Management: [1]

Spinlock Programming Guide
- Spinlocks Clearing After a System Bug Recovery: [2] [3]

Spinlock Register Manual
- Spinlock Register Summary: [4]

Table 21-16. SPINLOCK_LOCK_REG_i

Address Offset	0x0000 0800	**index**	i = 0 to 31
Physical Address	0x4A0F 6800 + (0x4 * i)	**Instance**	Spinlock
Description	This register contains the state of one lock.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															TAKEN

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved. Reads return 0. Writes are ignored.	R	0x0000 0000
0	TAKEN	Lock State Read 0x0: Lock was previously Not Taken (free). The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: Lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.	RW	0

Table 21-17. Register Call Summary for Register SPINLOCK_LOCK_REG_i

Spinlock Functional Description • Spinlock Functional Operation: [0] [1] [2] [3] [4] [5]
Spinlock Programming Guide • Spinlocks Clearing After a System Bug Recovery: [6] [7] • Take and Release Spinlock: [8] [9]
Spinlock Register Manual • Spinlock Register Summary: [10]

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Timers

This chapter describes the timer modules for the device.

Topic **Page**

22.1 Timers Overview **4517**
22.2 General-Purpose Timers **4518**
22.3 Watchdog Timers **4572**
22.4 32-kHz Synchronized Timer **4598**

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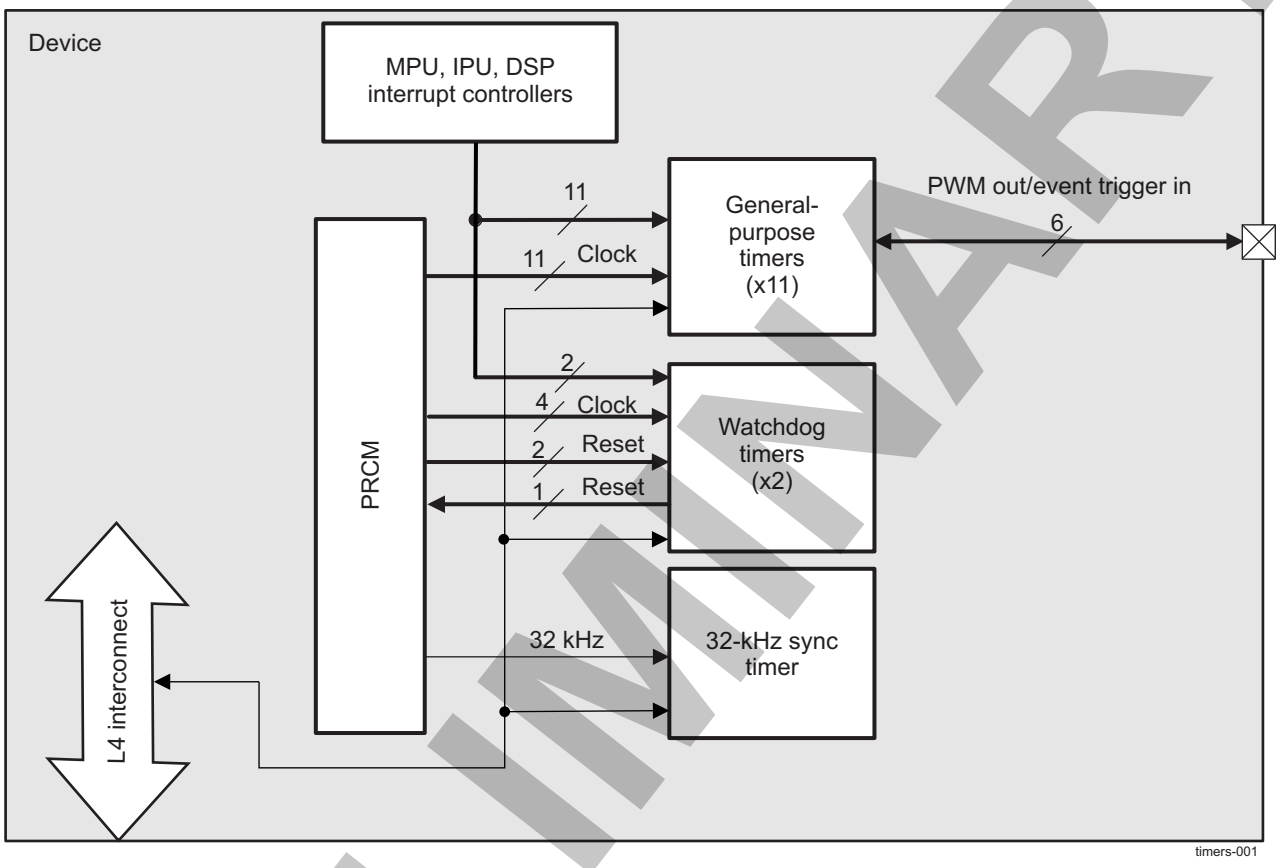
22.1 Timers Overview

The device includes several types of timers used by the system software, including 11 general-purpose (GP) timers, two watchdog timers, and a 32-kHz synchronized timer (COUNTER_32K). Figure 22-1 is a high-level block diagram of the device timers.

Figure 22-1. Timers Overview



The two watchdog timers are clocked with 32-kHz clocks. The 32-kHz sync timer, which is reset only at power up, provides the operating system (OS) with a stable timing source that stores the relative time since the last power cycle of the product. Finally, 11 GP timers, which are useful simply as basic timers, are included to generate time-stamp-based interrupts to the system software or to use as a source of pulse-width modulation (PWM) signals.

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22.2 General-Purpose Timers

22.2.1 General-Purpose Timers Overview

The device has 11 GP timers: TIMER1 through TIMER11.

- TIMER1(1ms tick): has its event capture pin tied to 32KHz clock and can be used to gauge the system clock input and detects its frequency among 12, 16.8, 19.2, 26 or 38.4 MHz. It includes a specific functions to generate accurat tick interrupts to the operating system and it belons to the WKUP domain
- TIMER2 and TIMER10:(1ms tick timers): they include a specific functions to generate accurate tick interrupts to the operating system, TIMER2 & TIMER10 belong to the L4_PER domain
- TIMER3/4/9/11: they belong to the L4_PER domain
- TIMER5 trough TIMER8: belong to the Audio domain and are part of the ABE module

Each timer can be clocked from the system clock (12, 16.8, 19.2, 26, or 38.4 MHz) or the 32-kHz clock. The selection of clock source is made at the power, reset, and clock management (PRCM) module level. For more information, see Section 3.6.3.1, *PRM Clock Source*.

Each timer can provide an interrupt to the microprocessor unit (MPU) subsystem. In addition TIMER3/4/9/11 can generate interrupt to IPU subsystem and TIMER5/6/7/8 can generate interrupts to the DSP subsystem.

TIMER5, TIMER6 and TIMER8 through TIMER11 are connected to external pins by their PWM output or their event capture input pin (for external timer triggering). Figure 22-2 is an overview of the GP timers.

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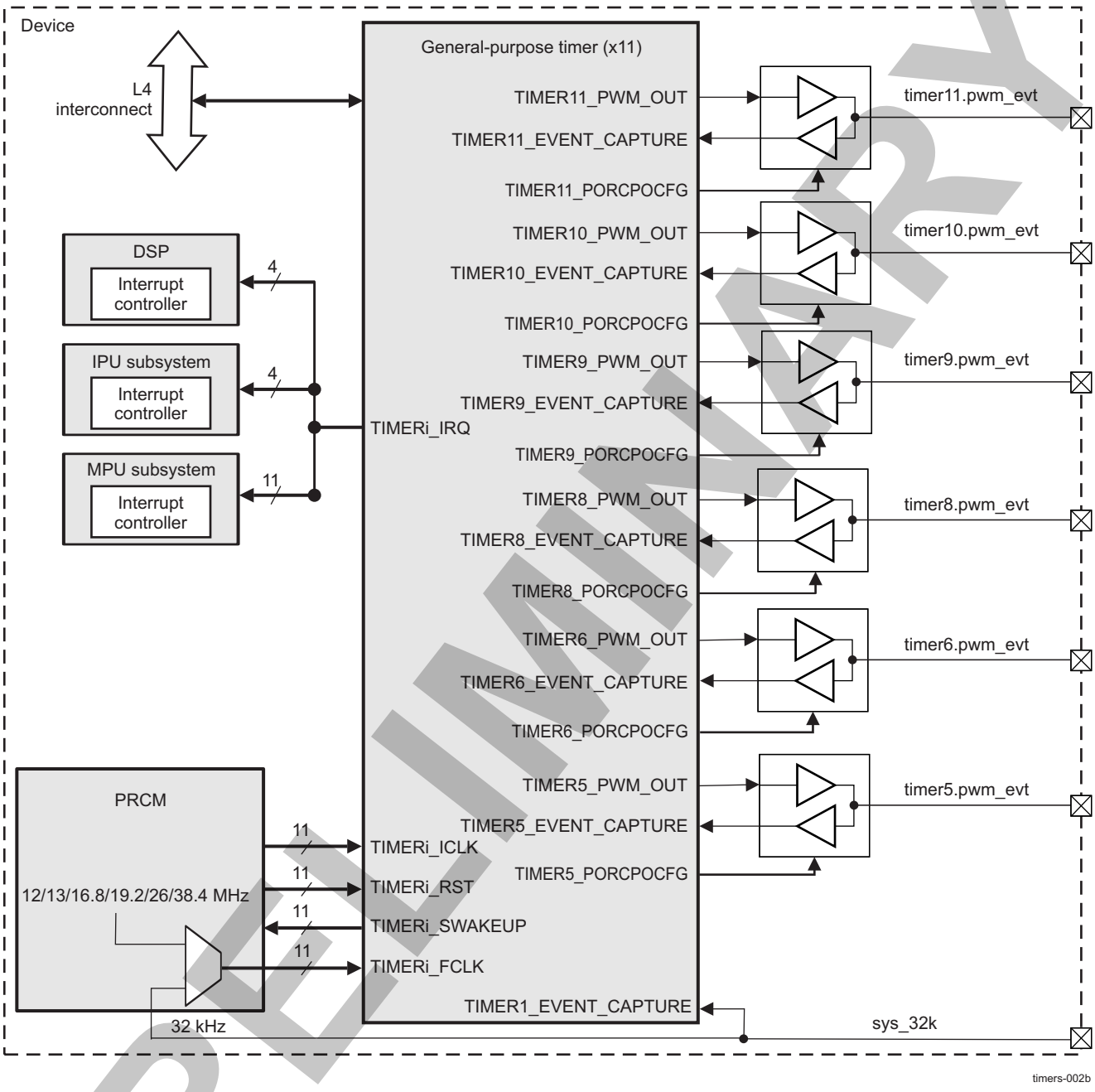
Figure 22-2. GP Timers Overview



22.2.1.1 GP Timer Features

The following are the main features of the GP timer controllers:

- Level 4 (L4) slave interface support:
  - 32-bit data bus width
  - 32-/16-bit access supported
  - 8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Write nonposted transaction mode supported

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- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start/stop mode
- Programmable divider clock source (2^n, where n = [0:8])
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- On-the-fly read/write register (while counting)
- 1-ms tick with 32.768-Hz functional clock generated (only TIMER1, TIMER2, and TIMER10)

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22.2.2 GP Timer Environment

22.2.2.1 GP Timer External System Interface

Six of the 11 GP timers can send or receive stimulus to/from the external (off-chip) system. In the device, however, only TIMER5, TIMER6, and TIMER8 through TIMER11 are configured to output a PWM pulse or receive an external event signal used as a trigger to capture the current timer count. TIMER1 is also configured to receive an event trigger input (TIMER1_EVENT_CAPTURE) tied to the internal 32-kHz clock. This event signal gauges the system clock input, detecting its frequency among 12, 16.8, 19.2, 26, or 38.4 MHz.

Figure 22-3 shows the external system interface for the GP timers, and Table 22-1 describes the GP timer inputs and outputs.

NOTE: Software control must ensure that MUX mode is configured to select the timerx_pwm_evt (where x = 5, 6, 8 to 11) signal on only one pad. Other pads on which the same signal is multiplexed must be configured in safe mode or non-dmtimer mode to avoid two different pads driving the same signal.

For more information about the configuration of the timerx_pwm_evt I/O pads, see Section 18.4.8, *PAD Functional Multiplexing and Configuration*.

Figure 22-3. GP Timers External System Interface

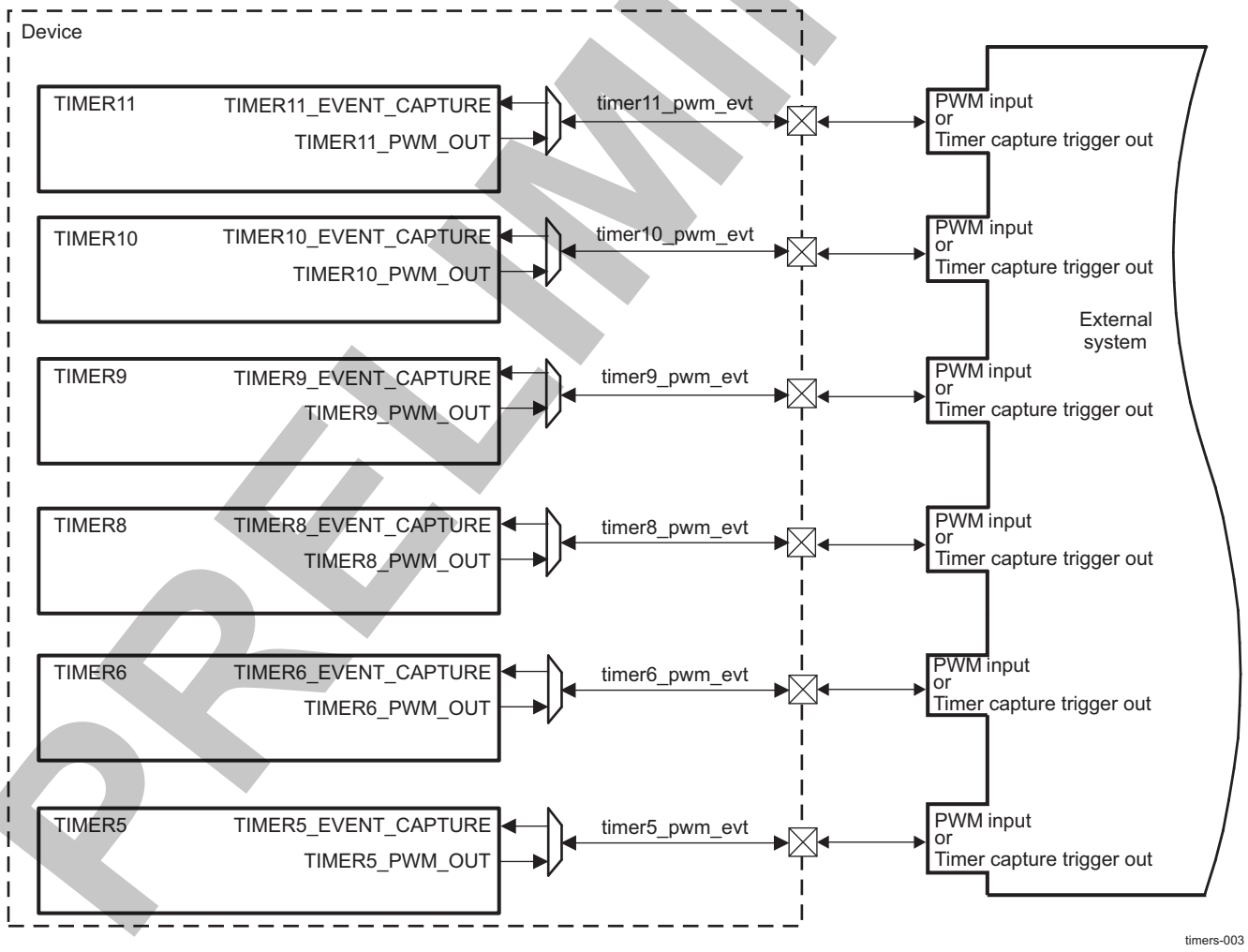

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Table 22-1. Input/Output Description

Pin Name	Type [1]	Reset Value	Signal Name	Description
timer5_pwm_evt	I/O	0	TIMER5_EVENT_CAPTURE TIMER5_PWM_OUT	TIMER5 trigger input/ PWM output
timer6_pwm_evt	I/O	0	TIMER6_EVENT_CAPTURE TIMER6_PWM_OUT	TIMER6 trigger input/ PWM output
timer8_pwm_evt	I/O	0	TIMER8_EVENT_CAPTURE TIMER8_PWM_OUT	TIMER8 trigger input/ PWM output
timer9_pwm_evt	I/O	0	TIMER9_EVENT_CAPTURE TIMER9_PWM_OUT	TIMER9 trigger input/ PWM output
timer10_pwm_evt	I/O	0	TIMER10_EVENT_CAPTURE TIMER10_PWM_OUT	TIMER10 trigger input/ PWM output
timer11_pwm_evt	I/O	0	TIMER11_EVENT_CAPTURE TIMER11_PWM_OUT	TIMER11 trigger input/ PWM output

(1) When configured for that function; I = Input, O = Output

NOTE: The event trigger input (TIMERi_EVENT_CAPTURE) for TIMER2 through TIMER4, and TIMER7 is internally tied low, and the PWM output (TIMERi_PWM_OUT) is not connected.

NOTE: For TIMER5, TIMER6, and TIMER8 through TIMER11, the TIMERi_PORGPOCFG signal selects to connect the general purpose timer(GPT) PWM output or the GPTcapture input to the timerx_pwm_evt (where x = 5, 6, 8 to 11) pad at the top level.

When the TCLR[14] GPO_CFG bit = 0b1, the timerx_pwm_evt functions as a capture input.

When the TCLR[14] GPO_CFG bit = 0b0, the timerx_pwm_evt functions as a PWM output (GPO_CFG = 0b0).

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22.2.3 GP Timer Integration

Figure 22-4 shows the integration of the GP timer in the device.

Figure 22-4. GP Timer Integration

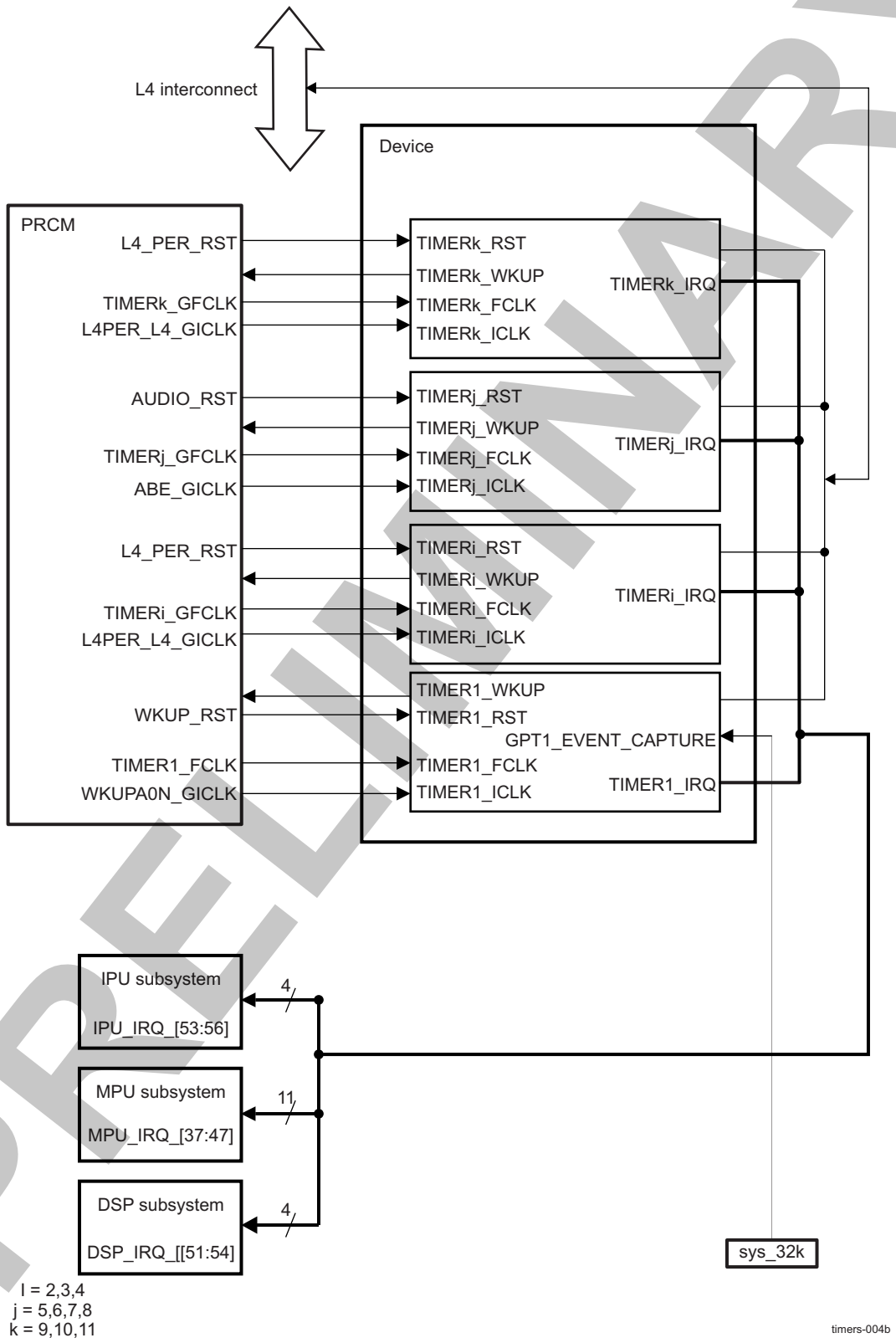

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Table 22-2 through Table 22-4 summarize the integration of the module in the device.

Table 22-2. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
TIMER1	PD_WKUP	Yes	L4_WKUP
TIMER2	PD_L4_PER	Yes	L4_PER
TIMER3	PD_L4_PER	Yes	L4_PER
TIMER4	PD_L4_PER	Yes	L4_PER
TIMER5	PD_AUDIO	Yes	L4_ABE
TIMER6	PD_AUDIO	Yes	L4_ABE
TIMER7	PD_AUDIO	Yes	L4_ABE
TIMER8	PD_AUDIO	Yes	L4_ABE
TIMER9	PD_L4_PER	Yes	L4_PER
TIMER10	PD_L4_PER	Yes	L4_PER
TIMER11	PD_L4_PER	Yes	L4_PER

Table 22-3. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
TIMER1	TIMER1_FCLK	TIMER1_GFCLK	PRCM	TIMER1 functional clock
	TIMER1_ICLK	WKUPAON_GICLK	PRCM	TIMER1 interface clock
TIMER2	TIMER2_FCLK	TIMER2_GFCLK	PRCM	TIMER2 functional clock
	TIMER2_ICLK	L4PER_L4_GICLK	PRCM	TIMER2 interface clock
TIMER3	TIMER3_FCLK	TIMER3_GFCLK	PRCM	TIMER3 functional clock
	TIMER3_ICLK	L4PER_L4_GICLK	PRCM	TIMER3 interface clock
TIMER4	TIMER4_FCLK	TIMER4_GFCLK	PRCM	TIMER4 functional clock
	TIMER4_ICLK	L4PER_L4_GICLK	PRCM	TIMER4 interface clock
TIMER5	TIMER5_FCLK	TIMER5_GFCLK	PRCM	TIMER5 functional clock
	TIMER5_ICLK	ABE_GICLK	PRCM	TIMER5 interface clock
TIMER6	TIMER6_FCLK	TIMER6_GFCLK	PRCM	TIMER6 functional clock
	TIMER6_ICLK	ABE_GICLK	PRCM	TIMER6 interface clock
TIMER7	TIMER7_FCLK	TIMER7_GFCLK	PRCM	TIMER7 functional clock
	TIMER7_ICLK	ABE_GICLK	PRCM	TIMER7 interface clock
TIMER8	TIMER8_FCLK	TIMER8_GFCLK	PRCM	TIMER8 functional clock
	TIMER8_ICLK	ABE_GICLK	PRCM	TIMER8 interface clock
TIMER9	TIMER9_FCLK	TIMER9_GFCLK	PRCM	TIMER9 functional clock
	TIMER9_ICLK	L4PER_L4_GICLK	PRCM	TIMER9 interface clock
TIMER10	TIMER10_FCLK	TIMER10_GFCLK	PRCM	TIMER10 functional clock
	TIMER10_ICLK	L4PER_L4_GICLK	PRCM	TIMER10 interface clock
TIMER11	TIMER11_FCLK	TIMER11_GFCLK	PRCM	TIMER11 functional clock
	TIMER11_ICLK	L4PER_L4_GICLK	PRCM	TIMER11 interface clock
Resets				
TIMER1	TIMER1_RST	WKUPAON_RST	PRM	Reset to TIMER1
TIMER2	TIMER2_RST	L4_PER_RST	PRM	Reset to TIMER2
TIMER3	TIMER3_RST	L4_PER_RST	PRM	Reset to TIMER3
TIMER4	TIMER4_RST	L4_PER_RST	PRM	Reset to TIMER4
TIMER5	TIMER5_RST	ABE_RST	PRM	Reset to TIMER5
TIMER6	TIMER6_RST	ABE_RST	PRM	Reset to TIMER6

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Table 22-3. Clocks and Resets (continued)

TIMER7	TIMER7_RST	ABE_RST	PRM	Reset to TIMER7
TIMER8	TIMER8_RST	ABE_RST	PRM	Reset to TIMER8
TIMER9	TIMER9_RST	L4_PER_RST	PRM	Reset to TIMER9
TIMER10	TIMER10_RST	L4_PER_RST	PRM	Reset to TIMER10
TIMER11	TIMER11_RST	L4_PER_RST	PRM	Reset to TIMER11

Table 22-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
TIMER1	TIMER1_IRQ	MPU_IRQ_37	MPU	TIMER1 interrupt
TIMER2	TIMER2_IRQ	MPU_IRQ_38	MPU	TIMER2 interrupt
TIMER3	TIMER3_IRQ	MPU_IRQ_39	MPU	TIMER3 interrupt
		IPU_IRQ_53	IPU	
TIMER4	TIMER4_IRQ	MPU_IRQ_40	MPU	TIMER4 interrupt
		IPU_IRQ_54	IPU	
TIMER5	TIMER5_IRQ	DSP_IRQ_51	DSP	TIMER5 interrupt
		MPU_IRQ_41	MPU	
TIMER6	TIMER6_IRQ	DSP_IRQ_52	DSP	TIMER6 interrupt
		MPU_IRQ_42	MPU	
TIMER7	TIMER7_IRQ	DSP_IRQ_53	DSP	TIMER7 interrupt
		MPU_IRQ_43	MPU	
TIMER8	TIMER8_IRQ	DSP_IRQ_54	DSP	TIMER8 interrupt
		MPU_IRQ_44	MPU	
TIMER9	TIMER9_IRQ	MPU_IRQ_45	MPU	TIMER9 interrupt
		IPU_IRQ_55	IPU	
TIMER10	TIMER10_IRQ	MPU_IRQ_46	MPU	TIMER10 interrupt
TIMER11	TIMER11_IRQ	MPU_IRQ_47	MPU	TIMER11 interrupt
		IPU_IRQ_56	IPU	
No DMA Requests				

NOTE: For the description of the interrupt source, see Section 22.2.4.4, *GP Timer Interrupts*.

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22.2.4 GP Timer Functional Description

Each GP timer contains a free-running upward counter with autoreload capability on overflow. The timer counter can be read and written on-the-fly (while counting). Each GP timer includes compare logic to allow an interrupt event on a programmable counter matching value. A dedicated output signal can be pulsed or toggled on either an overflow or a match event. This offers time-stamp trigger signaling or PWM signal sources. A dedicated input signal can be used to trigger an automatic timer counter capture or an interrupt event on a programmable input signal transition. A programmable clock divider (prescaler) allows reduction of the timer input clock frequency. All internal timer interrupt sources are merged into one module interrupt line and one wake-up line.

Each internal interrupt source can be independently enabled and disabled by a dedicated bit in the IRQSTATUS_SET and IRQSTATUS_CLR register for the interrupt features, and a dedicated bit of the IRQWAKEEN register for the wake-up of TIMER1, TIMER2, and TIMER10. In addition, these timers have a mechanism implemented to generate an accurate tick interrupt.

For GP timers 3 through 9 and timer 11, each internal interrupt source can be independently enabled and disabled through the IRQENABLE_SET and IRQENABLE_CLR register for the interrupt features, and a dedicated bit of the IRQWAKEEN register for the wake-up features.

For each GP timer implemented in the device, there are two possible clock sources:

- 32-kHz clock
- System clock

Selection of the input clock source is done in the registers in the PRCM configuration (see Section 22.2.1, *GP Timer Overview*).

Each GP timer supports three functional modes:

- Timer mode
- Capture mode
- Compare mode

The capture and compare modes are disabled by default after core reset.

22.2.4.1 GP Timer Block Diagram

Figure 22-5 is a block diagram of the common GP timers, and Figure 22-6 is a block diagram of the GP timers with a 1-ms tick generation module.

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Figure 22-5. Block Diagram of TIMER3 Through TIMER9, and TIMER11

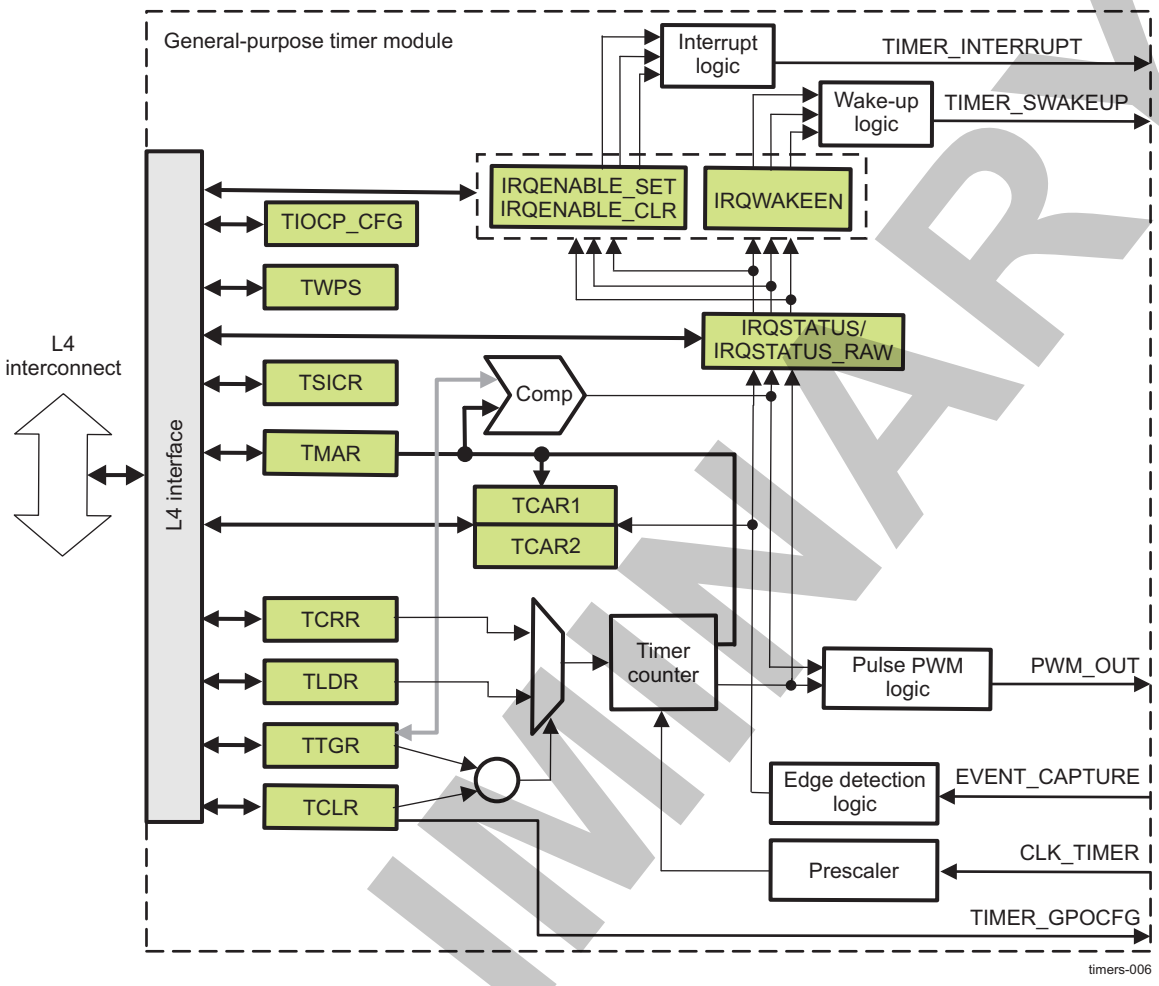

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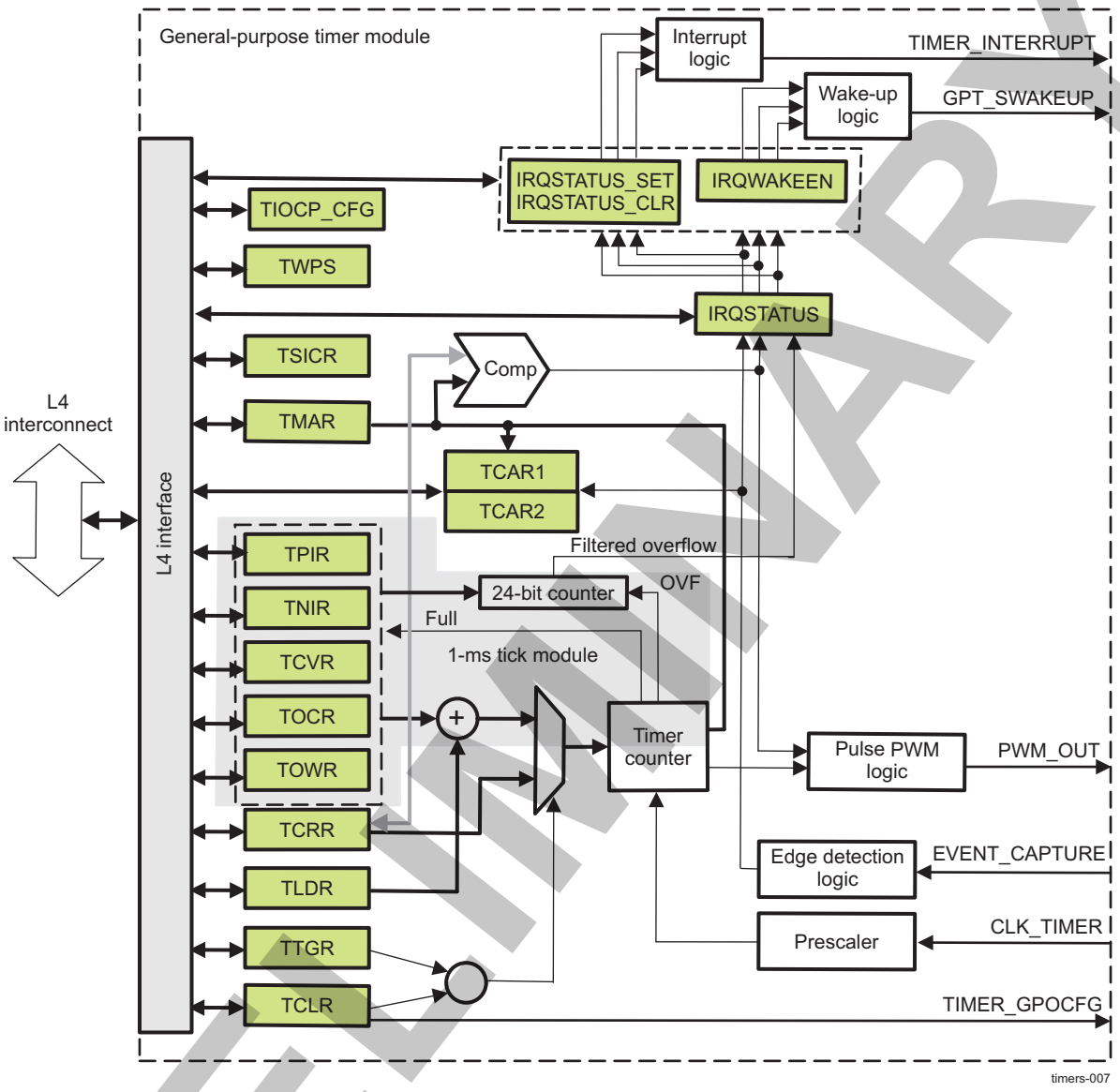
Figure 22-6. Block Diagram of TIMER1, TIMER2, and TIMER10



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22.2.4.2 Power Management

At the PRCM module level, when all conditions to shut off the functional or interface output clocks in the PRCM module are met (see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*), the PRCM module automatically launches a hardware handshake protocol to ensure the GP timer is ready to have its clocks switched off. Namely, the PRCM module asserts an IDLE request to the GP timer.

Although this handshake is a hardware function and is out of software control, the way the GP timer acknowledges the PRCM IDLE request is configurable through the TIOCP_CFG[3:2] IDLEMODE bit field.

Table 22-5 lists the IDLEMODE settings and the related acknowledgment modes.

Table 22-5. IDLEMODE Settings

IDLEMODE Value	Selected Mode	Description
00	Force-idle	The GP timer unconditionally acknowledges the IDLE request from the PRCM module, regardless of its internal operations. This mode must be used carefully, because it does not prevent the loss of data when the clock is switched off.
01	No-idle	The GP timer never acknowledges an IDLE request from the PRCM module. This mode is safe from a module point of view, because it ensures that the clocks remain active. It is not efficient from a power-saving perspective, because it does not allow the PRCM output clock to be shut off, and thus the power domain to be set to a lower power state.
10	Smart-idle	The GP timer acknowledges the IDLE request, basing its decision on its internal activity. The acknowledge signal is asserted only when all pending transactions and IRQ requests are treated. This is the best approach to efficient system power management.
11	Smart-idleWakeup	The module behaves like in Smart-idle mode, with the exception, that it can issue a wake-up request in sleep mode, if the functional clock is not cut off.

22.2.4.2.1 Wake-Up Capability

If the TIOCP_CFG[3:2] IDLEMODE bit field sets the smart-idle mode, the timer evaluates its internal capability to have the interface clock switched off. When there is no further internal activity (no pending interrupt sources: match, overflow, or timer capture events), the idle acknowledge signal is asserted and the timer enters sleep mode, ready to issue a wake-up request. This wake-up request is sent only if the wake up capability is enabled by the corresponding bit field in IRQWAKEEN register.

Figure 22-7 shows the wake-up request generation. For more information about the GP timer clock control, Section 3.6, *Clock Management Functional Description*, in Chapter 3, *Power, Reset and Clock Management*.

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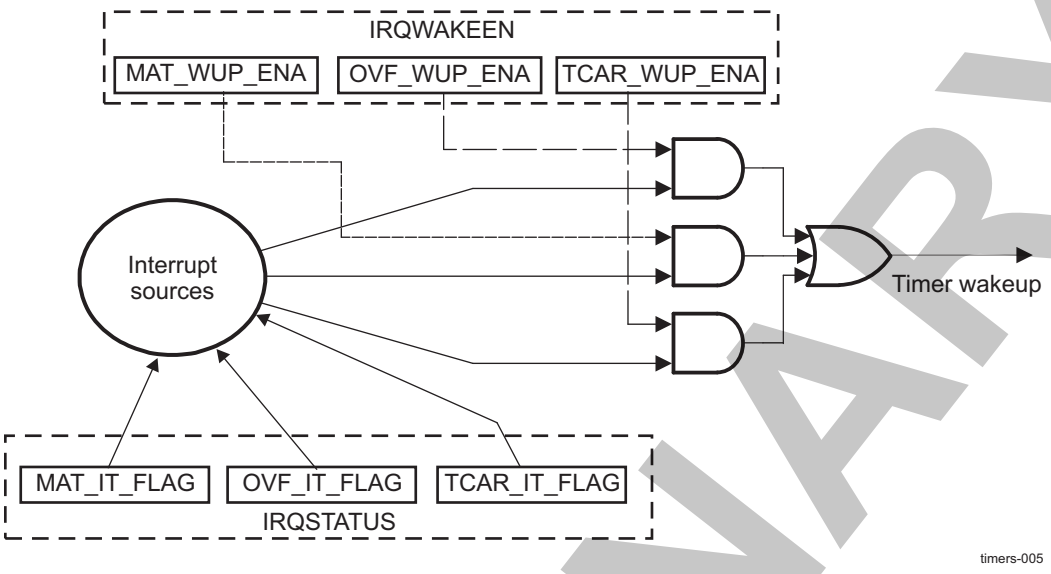
Figure 22-7. Wake-Up Request Generation



The expected source of the wake-up event is an overflow (TCRR), a timer match (the compare result of TCRR and TMAR matches the counter value), and a timer capture.

When the wake-up event is issued, the associated interrupt status bit is set in the timer status register (IRQSTATUS). The pending wake-up event is reset when the set status bit is overwritten with 1.

NOTE: The status bit must be reset to re-enter idle mode.

22.2.4.3 Software Reset

Two bits can generate a software reset of the GP timer:

- TIOCP_CFG[0] SOFTRESET
- TSICR[1] SFT

For both bits, all read accesses return 0.

The TIOCP_CFG[0] SOFTRESET bit allows resetting of the functional and interface domains. The TSICR[1] SFT bit allows resetting the functional part of the GP timer.

Before accessing or using the GP timer, the local host must ensure that both internal resets are released by reading the TIOCP_CFG[0] SOFTRESET bit. This bit monitors the internal reset status.

22.2.4.4 GP Timer Interrupts

The timer can issue an overflow interrupt, a timer match interrupt, and a timer capture interrupt. Each internal interrupt source can be independently enabled and disabled in the interrupt-enable register (IRQSTATUS_SET for TIMER1/2/10 and IRQENABLE_SET for other timers) and disabled in the interrupt-disable register (IRQSTATUS_CLR for TIMER1/2/10 and IRQENABLE_CLR for other timers). When the interrupt event is issued, the associated interrupt status bit is set in the timer status register (IRQSTATUS).

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22.2.4.5 Timer Mode Functionality

The timer is an upward counter that can be started and stopped at any time through the timer control register (the TCLR[0] ST bit). The timer counter register (TCRR) can be loaded when stopped or on-the-fly (while counting). TCRR can be loaded directly by a TCRR write access with a new timer value. TCRR can also be loaded with the value held in the timer load register (TLDR) by a trigger register (TTGR) write access. The loading of TCRR is done regardless of the written value of TTGR. The value of TCRR can be read when stopped or captured on-the-fly by a TCRR read access. The timer is stopped and the counter value is set to 0 when the module reset is asserted. The timer is maintained at stop after the reset is released.

In one-shot mode (the TCLR[1] AR bit is set to 0), the counter is stopped after counting overflow occurs (the counter value remains at 0).

When the autoreload mode is enabled (the TCLR[1] AR bit is set to 1), TCRR is reloaded with the value of TLDR after a counting overflow occurs.

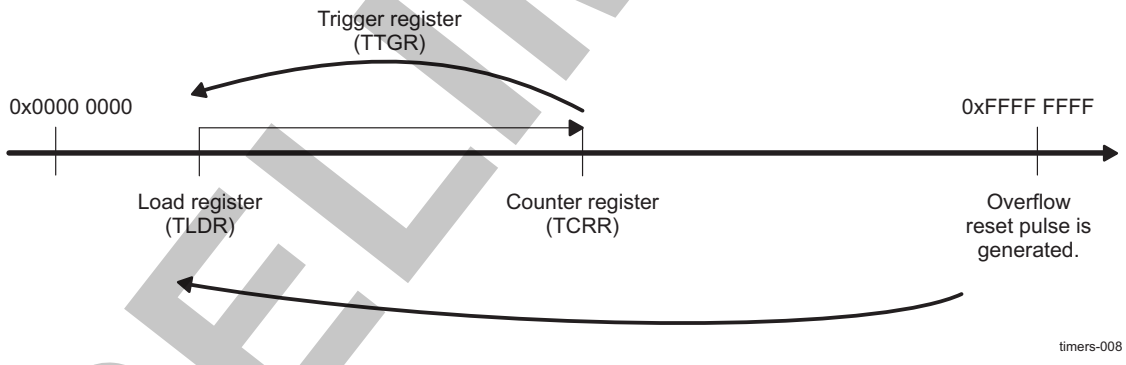
CAUTION

Do not put the overflow value (0xFFFF FFFF) in the TLDR register because it can lead to undesirable results.

An interrupt can be issued on overflow if the overflow interrupt-enable bit is set in the timer interrupt-enable register (the IRQSTATUS_SET[1] OVF_EN_FLAG bit is set to 1for TIMER1/2/10 and the IRQENABLE_SET[1]OVF_EN_FLAG bit is set to 1 for other timers). A dedicated output pin (timer PWM) can be programmed in the TCLR[12] PT bit through the TCLR[11:10] (PT and TRG bits) to generate one positive pulse (prescaler duration) or to invert the current value (toggle mode) when an overflow occurs. The TCLR[12] PT bit selects pulse/toggle modulation (the TCLR[11:10] TRG bit field selects trigger mode).

Figure 22-8 shows the TCRR timing value.

Figure 22-8. TCRR Timing Value



22.2.4.5.1 1-ms Tick Generation (Only TIMER1, TIMER2, and TIMER10)

The interrupt period is not exactly 1 ms, because the timer input clock is 32.768 Hz. If the clock counts up to 32, it obtains a 0.977-ms period; if it counts up to 33, it obtains a 1.007-ms period. For large granularity, the error is cumulative and can generate important deviations from the standard value.

To minimize the error between a true 1-ms tick and the tick generated by the 32.768-Hz timer, the sequencing of periods less than 1 ms and periods greater than 1 ms must be shuffled. An additional 1-ms block is used to correct this error. See Figure 22-9.

In this implementation, the increment sequencing is automatically managed by the timer to minimize the error. The user must define only the value of the timer positive increment register (the TPIR[31:0] POSITIVE_INC_VALUE bit field) and the timer negative increment register (the TNIR[31:0] NEGATIVE_INC_VALUE bit field). An automatic adaptation mechanism is used to simplify the programming model.

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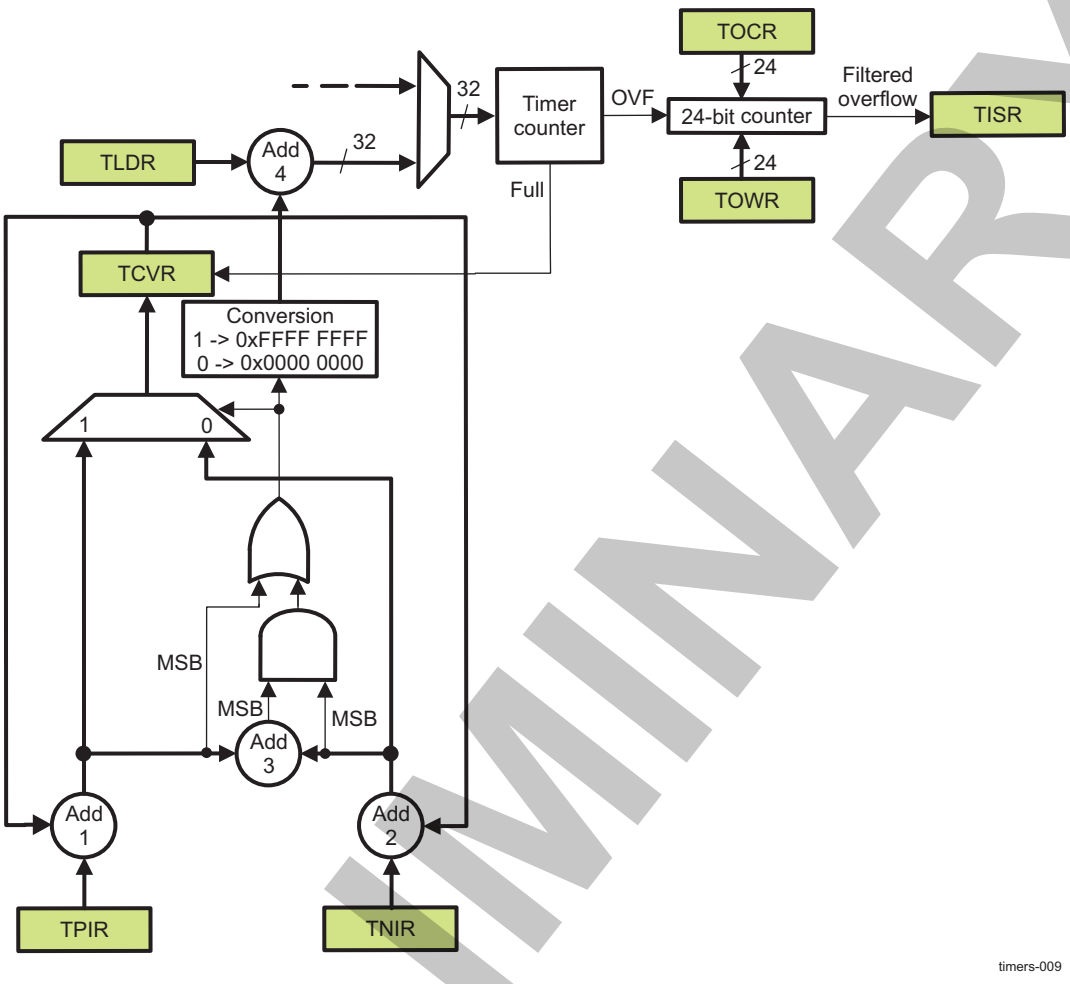
Figure 22-9. Block Diagram of the 1-ms Tick Module



The TPIR, TNIR, and TCVR registers and adders Add1, Add2, and Add3 are used to define whether the next value loaded in the timer counter register (the TCRR[31:0] TIMER_COUNTER bit field) is the value of the TLDR[31:0] LOAD_VALUE bit field (period less than 1 ms) or the value of TLDR[31:0] LOAD_VALUE –1 (period greater than 1 ms).

Table 22-6 lists the value loaded in the TCRR according to the sign of the result of Add1, Add2, and Add3.

MSB = 0: Positive value; MSB = 1: Negative value

Table 22-6. Value Loaded in TCRR to Generate 1-ms Tick

Add1 MSB	Add2 MSB	Add3 MSB	Value of TCRR Register
0	0	0	TLDR[31:0] LOAD_VALUE bit field
0	0	1	TLDR[31:0] LOAD_VALUE bit field
0	1	0	TLDR[31:0] LOAD_VALUE bit field
0	1	1	TLDR[31:0] LOAD_VALUE –1
1	0	0	N/A
1	0	1	N/A
1	1	0	TLDR[31:0] LOAD_VALUE –1
1	1	1	TLDR[31:0] LOAD_VALUE –1

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The values of the TPIR and TNIR registers are calculated using the following formulas:

- Positive increment value = ((INTEGER[F_{clk} × T_{tick}] + 1) × 1e6) – (F_{clk} × T_{tick} × 1e6)
- Negative increment value = (INTEGER[F_{clk} × T_{tick}] × 1e6) – (F_{clk} × T_{tick} × 1e6)

NOTE: F_{clk} clock frequency (kHz)

T_{tick} tick period (ms)

The timer overflow counter register (TOCR) and the timer overflow wrapping register (TOWR) are used to filter interrupts. When the timer overflows, it increments the 24-bit TOCR. When the values in the 24-bit TOCR match the values in the 24-bit TOWR and the timer overflow is asserted, the TOCR is reset and an interrupt is generated to the IRQSTATUS register.

NOTE: TOWR has to be set to requested value + 1. For example, if no interrupt needs to be masked TOWR must be set to 0, if one interrupt needs to TOWR must be set to 2, if two interrupts need to be masked TOWR must be set to 3 and so on.

It is important to have in mind that the case when FFFFFF interrupts need to be masked is not possible.

With the conversion block in reset state (the positive increment register, negative increment register, and counter value register are zeroed), the programming model and the behavior of TIMER1, TIMER2, and TIMER10 remain unchanged.

For 1-ms tick with a 32.768-Hz clock:

- TPIR[31:0] POSITIVE_INC_VALUE = 232,000
- TNIR[31:0] NEGATIVE_INC_VALUE = –768,000
- TLDR[31:0] LOAD_VALUE = 0xFFFF FFE0

NOTE: Any value of the tick period can be generated with the appropriate value of the TPIR, TNIR, and TLDR.

By default, the TPIR, TNIR, TCVR, TOCR, and TOWR and the associated logic are in reset mode (all 0s) and have no effect on the programming model.

22.2.4.6 Capture Mode Functionality

When a transition is detected on the module input pin (EVENT_CAPTURE), the timer value in the TCRR can be captured and saved in the TCAR1 or TCAR2 register function of the mode selected in the TCLR[13] CAPT_MODE bit. The edge detection circuitry monitors transitions on the input pin (EVENT_CAPTURE).

The rising edge, falling edge, or both, can be selected in the TCLR[9:8] TCM bit field to trigger the timer counter capture. The module sets the IRQSTATUS[2] TCAR_IT_FLAG bit when an active edge is detected, and at the same time, the counter value TCRR is stored in timer capture register TCAR1 or TCAR2, as follows:

- If the TCLR[13] CAPT_MODE bit is 0, on the first enabled capture event, the value of the counter register is saved in the TCAR1 register, and the next events are ignored (no update on the TCAR1 register and no interrupt triggering) until the detection logic is reset or the IRQSTATUS[2] TCAR_IT_FLAG is cleared by writing 1 to it.
- If the TCLR[13] CAPT_MODE bit is 1, on the first enabled capture event, the value of the counter register is saved in the TCAR1 register, and on the second enabled capture event, the value of the counter register is saved in the TCAR2 register. If a capture interrupt is enabled, the interrupt triggers on the second event capture. All other events are ignored (no update on TCAR1/TCAR2 and no interrupt triggering) until the detection logic is reset or the IRQSTATUS[2] TCAR_IT_FLAG bit is cleared by writing 1 to it. This mechanism is useful for period calculation of a clock, if that clock is connected to the EVENT_CAPTURE input pin.

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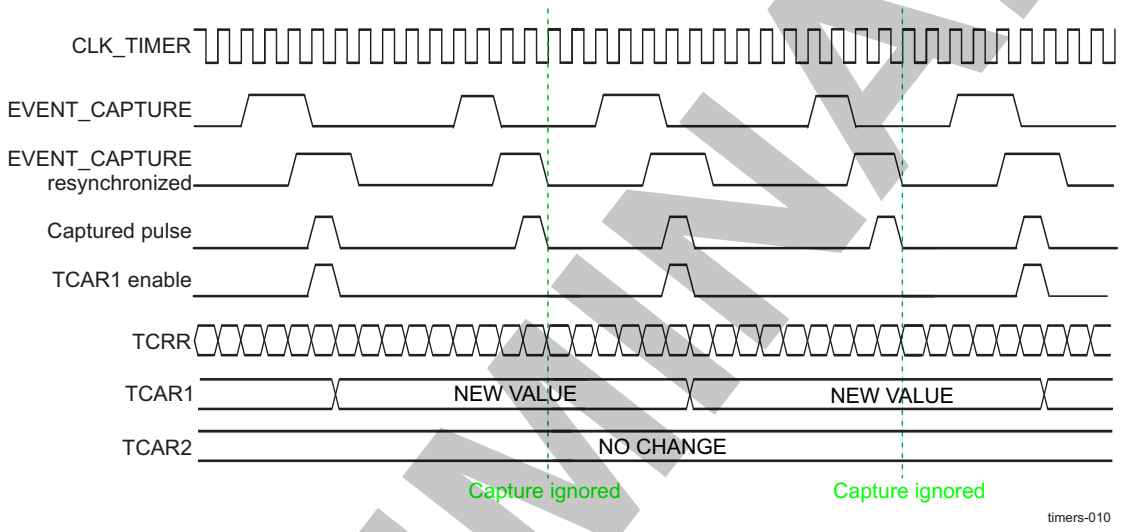
The edge detection logic is reset (a new capture is enabled) when the active capture interrupt is served. The IRQSTATUS[2] TCAR_IT_FLAG bit is cleared by writing 1 to it or when the edge detection mode bits (the TCLR[9:8] TCM bit field) are changed from no-capture mode detection to any other mode. The timer functional clock (input to prescaler) is used to sample the input pin (EVENT_CAPTURE). A negative or positive pulse input can be detected when the pulse time is greater than the functional clock period. An interrupt is issued on edge detection if the capture interrupt-enable bit is set in the IRQSTATUS_SET[2] TCAR_EN_FLAG bit (for TIMER1/2/10) or in the IRQENABLE_SET[2] TCAR_EN_FLAG bit (for other timers). See the examples in Figure 22-10 and Figure 22-11.

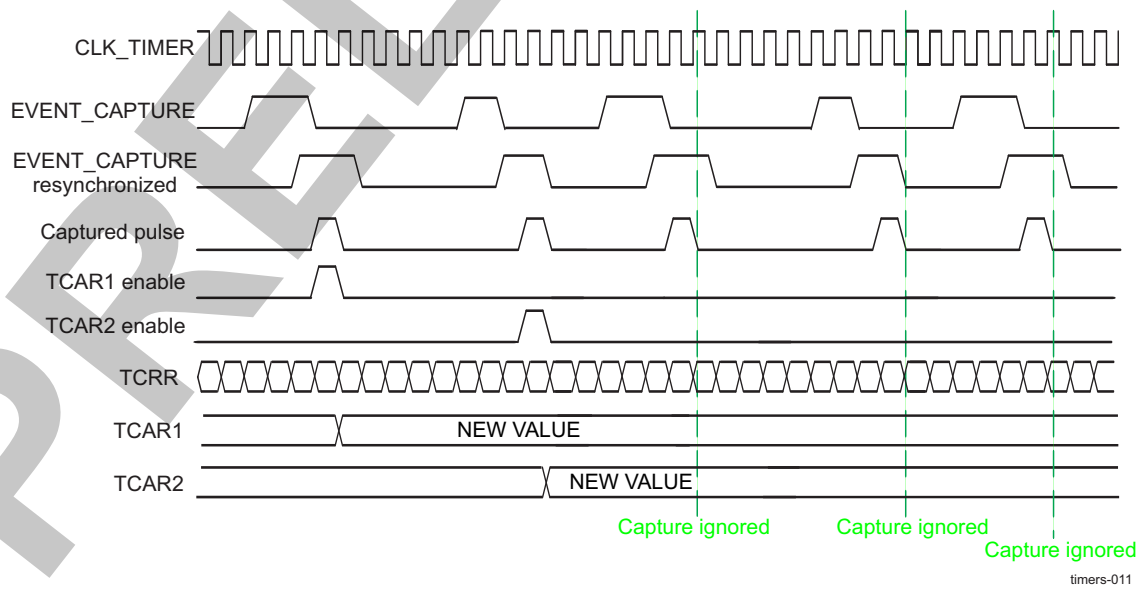
In Figure 22-10, the value of the TCLR[9:8] TCM bit field is 0b01, and the TCLR[13] CAPT_MODE bit is 0. Only the rising edge of EVENT_CAPTURE triggers a capture in the TCAR1 and TCAR2 registers, and only the TCAR1 register updates.

Figure 22-10. Capture Wave Example for TCLR[13] CAPT_MODE = 0



In Figure 22-11, the value of the TCLR[9:8] TCM bit field is 0b01, and the TCLR[13] CAPT_MODE bit is 1. Only the rising edge of EVENT_CAPTURE triggers a capture in the TCAR1 register on the first enabled event, and the TCAR2 register updates on the second enabled event.

Figure 22-11. Capture Wave Example for TCLR[13] CAPT_MODE = 1



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22.2.4.7 Compare Mode Functionality

When the compare-enable register TCLR[6] CE bit is set to 1, the timer value (the TCRR[31:0] TIMER_COUNTER bit field) is continuously compared to the value held in the timer match register (TMAR). The value of the TMAR[31:0] COMPARE_VALUE bit field can be loaded at any time (timer counting or stopped). When the TCRR and the TMAR values match, an interrupt is issued, if the IRQSTATUS_SET[0] MAT_EN_FLAG bit (for TIMER1, TIMER2, and TIMER10), or the IRQENABLE_SET[0] MAT_EN_FLAG bit (for other timers) is set.

To prevent any unwanted interrupts due to reset value matching effect, write a compare value to the TMAR before setting the TCLR[6] CE bit.

The dedicated output pin (timer PWM) can be programmed in the TCLR[12] PT bit through the TCLR[11:10] TRG bit field to generate one positive pulse (timer clock duration) or to invert the current value (toggle mode) when an overflow or a match occurs.

22.2.4.8 Prescaler Functionality

A prescaler can be used to divide the timer counter input clock frequency. The prescaler is enabled when the TCLR[5] PRE bit is set. The TCLR[4:2] PTV bit field sets the second prescaler ratio. The prescaler counter is reset when the timer counter is stopped or reloaded on-the-fly.

Table 22-7 lists the prescaler/timer reload values versus contexts.

Table 22-7. Prescaler/Timer Reload Values Versus Contexts

Context	Prescaler	Timer Counter
Overflow (when autoreload is on)	Reset	TLDR[31:0]
TCRR write	Reset	TCRR[31:0]
TTGR write	Reset	TLDR[31:0]
Stop	Reset	Frozen

22.2.4.9 Pulse-Width Modulation

The timer can be configured to provide a programmable PWM output. The timer PWM output pin can be configured to toggle on an event. The TCLR[11:10] TRG bit field determines on which register value the PWM pin toggles. Either overflow or both overflow and match can be selected to toggle the timer PWM pin when a compare condition occurs.

NOTE: In toggle mode, when TCLR[11:10] TRG = 0x2 (overflow and match), the first event that toggles the PWM line is an overflow event. If a match event occurs first, it does not toggle the PWM line (see Figure 22-13).

The TCLR[7] SCPWM bit can be programmed to set or clear the timer PWM output signal only while the counter is stopped or the trigger is off. This allows setting the output pin to a known state before modulation starts. Modulation synchronously stops when the TCLR[11:10] TRG bit field is cleared and overflow occurs. This allows fixing a deterministic state of the output pin when modulation stops.

In Figure 22-12, the internal overflow pulse is set each time the (0xFFFF FFFF – TLDR[31:0] LOAD_VALUE + 1) value is reached, and the internal match pulse is set when the counter reaches the value of TMAR. Depending on the value of the TCLR[12] PT bit and TCLR[11:10] TRG bit field, the timer provides pulse or PWM event on the output pin (timer PWM).

The TLDR and TMAR must keep values below the overflow value (0xFFFF FFFF) by at least two units. If the PWM trigger events are both overflow and match, the difference between the values kept in the TMAR and the value in theTLDR must be at least two units. When match event is used, the compare mode TCLR[6] CE bit must be set.

In Figure 22-12, the TCLR[7] SCPWM bit is set to 0. In Figure 22-13, the TCLR[7] SCPWM bit is set to 1. To obtain the desired wave form, start the counter at 0xFFFF FFFE value (to ensure an overflow first) or adjust the line polarity (TCLR[7] SCPWM bit).

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Figure 22-12. Timing Diagram of PWM With TCLR[7] SCPWM Bit = 0

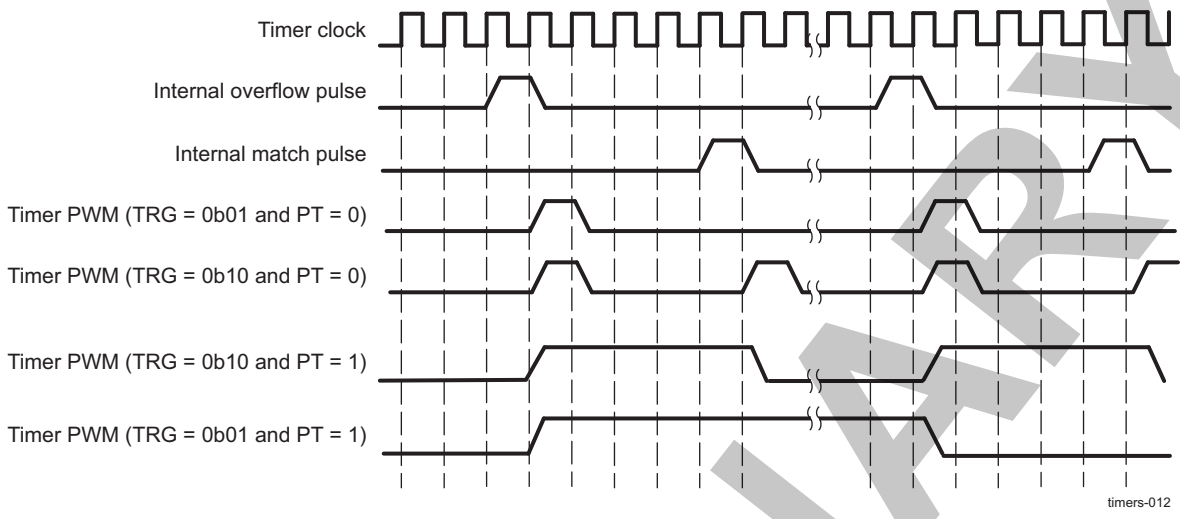
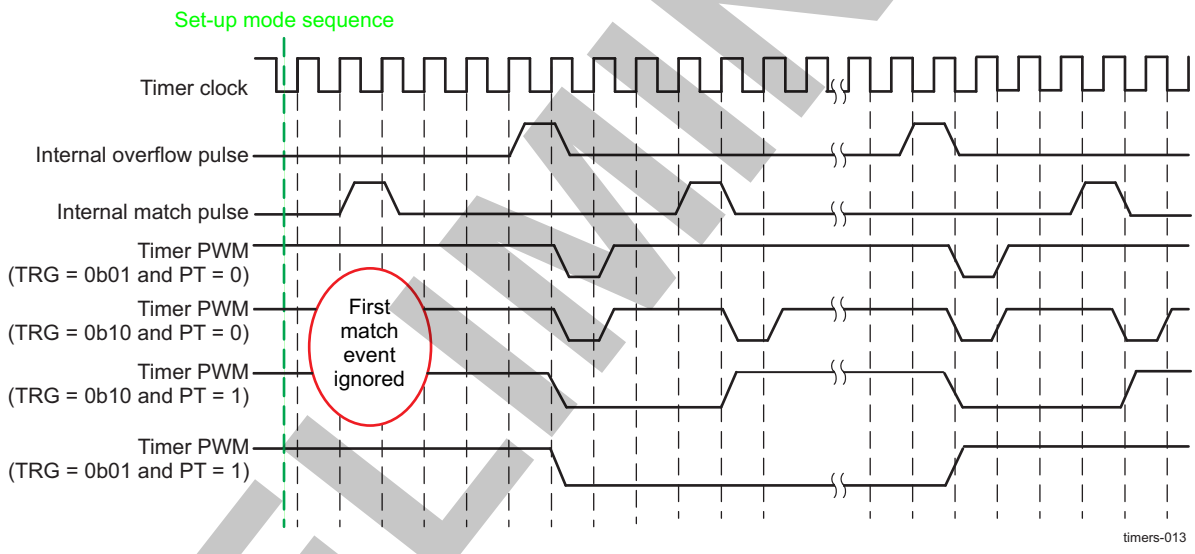


Figure 22-13. Timing Diagram of PWM With TCLR[7] SCPWM Bit = 1



22.2.4.10 Timer Counting Rate

The timer rate is defined by the following values:

- Value of the prescaler fields (the TCLR[5] PRE bit and TCLR[4:2] PTV bit field)
- Value loaded into the TLDR

Table 22-8 lists the prescaler clock ratio values.

Table 22-8. Prescaler Clock Ratio Values

TCLR[5] PRE	TCLR[4:2] PTV	Divisor (PS)
0	X	1
1	0	2
1	1	4
1	2	8
1	3	16
1	4	32

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Table 22-8. Prescaler Clock Ratio Values (continued)

TCLR[5] PRE	TCLR[4:2] PTV	Divisor (PS)
1	5	64
1	6	128
1	7	256

Thus, the timer overflow rate is expressed as:

OVF_Rate = (0xFFFF FFFF – TLDR + 1) × (timer-functional clock period) × PS

With (timer-functional clock period) = 1/(timer-functional clock frequency) and PS = $2^{(PTV + 1)}$ if prescaler is enabled, or PS = 1 if prescaler is disabled.

CAUTION

Internal resynchronization causes any write to the TCLR[1] ST bit to have some latency before the register is updated:

2.5 × functional clock cycles write_TIMER_TCLR_latency 3.5 × functional clock cycles

Remember to consider this latency whenever the timer must be started or stopped by a software change to the TCLR[1] ST bit.

CAUTION

- In non-PWM mode, TLDR must be maintained at less than or equal to 0xFFFF FFFE.
- In PWM mode, TLDR must be maintained at less than or equal to 0xFFFF FFFD.

For example, with a timer clock input of 32 kHz and the TCLR[5] PRE bit set to 0, the timer output period is as listed in Table 22-9.

Table 22-9. Value and Corresponding Interrupt Period

TLDR[31:0] LOAD_VALUE	Interrupt Period
0x0000 0000	39 h
0xFFFF 0000	2.1 s
0xFFFF FFF0	524 µs
0xFFFF FFFE	65.5 µs

22.2.4.11 Timer Under Emulation

During emulation mode, the timer continues to run according to the value of the TIOCP_ CFG[1] EMUFREE bit.

If the TIOCP_CFG[1] EMUFREE bit is set to 1, timer execution is not stopped in emulation mode and the interrupt is still generated when overflow or match is reached.

If the TIOCP_CFG[1] EMUFREE bit is set to 0, the prescaler and timer are frozen and both resume on exit from emulation mode. The asynchronous external input pin (timerx_pwm_evt, where x = [8:11]) is internally synchronized on two timer-clock rising edges.

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22.2.4.12 Accessing GP Timer Registers

All accesses are nonposted until software reconfiguration. All registers are 32 bits wide, accessible through the OCP interface with 16- or 32-bit access (read/write).

Any 16-bit write access must be least-significant bit (LSB) first, and the second write access must be most-significant bit (MSB) first. Write operations to the following GP timer registers can skip the MSB access if it is not necessary to update the 16 MSBs of the register:

- TIDR (all GP timers)
- TIOCP_CFG (all GP timers)
- IRQSTATUS_SET (GP timers 1, 2, 10)
- IRQSTATUS_RAW (all GP timers)
- IRQSTATUS (all GP timers)
- IRQENABLE_SET(all GP timers except 1,2,10)
- IRQENABLE_CLR(all GP timers except 1,2,10)
- IRQSTATUS_SET (GP timers 1, 2, 10)
- IRQSTATUS_CLR (GP timers 1, 2, 10)
- IRQWAKEEN (all GP timers)
- TSICR (all GP timers)

Write operations to the following functional registers must be complete (the MSB must be written even if the MSB data is not used):

- TCLR (all GP timers)
- TCRR (all GP timers)
- TLDR (all GP timers)
- TTGR (all GP timers)
- TMAR (all GP timers)
- TPIR (GP timers 1, 2, 10)
- TNIR (GP timers 1, 2, 10)
- TCVR (GP timers 1, 2, 10)
- TOCR (GP timers 1, 2, 10)
- TOWR (GP timers1, 2, 10)

The following L4 synchronous registers are not affected by the posted/nonposted mode selection; the write/read operation is effective and acknowledged (command accepted) after one L4 clock cycle from command assertion:

- TIDR
- TIOCP_CFG
- IRQSTATUS
- IRQSTATUS_RAW
- IRQENABLE_SET
- IRQENABLE_CLR
- IRQSTATUS_SET
- IRQSTATUS_CLR
- IRQWAKEEN
- TWPS
- TSICR

22.2.4.12.1 Writing to Timer Registers

The host uses the OCP interface to write to the following registers synchronously with the timer interface clock:

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- TLDR
- TCRR
- TCLR
- TIOCP_CFG
- IRQSTATUS
- IRQENABLE_SET
- IRQENABLE_CLR
- IRQWAKEEN
- TTGR
- TSICR
- TMAR

TIMER1, TIMER2, and TIMER10 also have the following registers:

- IRQSTATUS_SET
- IRQSTATUS_CLR
- TPIR
- TNIR
- TCVR
- TOCR
- TOWR

In 16-bit access mode, the 16 LSBs must be written before writing to the 16 MSBs.

22.2.4.12.1.1 Write Posting Synchronization Mode

This mode is used if the TSICR[2] POSTED bit is set to 1.

This mode uses a posted write scheme to update any internal register (TCLR, TCRR, TLDR, TTGR, TMAR, and TPIR, TNIR, TCVR, TOCR, and TOWR for TIMER1, TIMER2, and TIMER10). Therefore, the write transaction is immediately acknowledged on the open-core protocol (OCP) interface, although the effective write operation occurs later because of a resynchronization in the timer clock domain. The advantage is that neither the interconnect nor the device that requested the write transaction is stalled.

For each register, a status bit is provided in the tImer write-posted status (TWPS) register. In this mode, it is mandatory that software check this status bit before any write access. If a write is attempted to a register with a previous access pending, the previous access is discarded without notice.

The timer module updates the value of the timer counter register synchronously with the OCP clock. Consequently, any read access to TCRR does not add any resynchronization latency; the current value is always available.

NOTE: Because the overflow IRQ is generated when the value of TCRR reaches 0xFFFF FFFF, and not when it changes its value to the value after overflow, it is necessary to wait a delay of (1 × PS × timer functional clock period) before any read access to TCRR to ensure a correct reading of its content.

NOTE: If TTGR register is written during posted write to TCRR , the value to be written to TCRR will be discarded.

If a posted write to TCVR is started, the user must not write to TPIR or TNIR before the TCVR write is finished, because the value of TCVR is re-evaluated, so both the value to be written, and the recalculated value will be discarded.

If a write access is pending for a register, reading from this register does not yield a correct result. Software synchronization must be used to avoid incorrect results.

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The drawback of this automatic update mechanism is that it assumes a given relationship between the timer interface frequency and the timer clock frequency.

Functional frequency range: freq(timer clock) < freq(OCP interface clock) / 4.

22.2.4.12.1.2 Write Nonposting Synchronization Mode

This mode is used if the TSICR[2] POSTED bit is set to 0. It uses a nonposted write scheme to update any internal register. Therefore, the write transaction is not acknowledged on the L4 interface until the effective write operation occurs after the resynchronization in the timer functional clock domain. The drawback is that the interconnect and the device that requested the write transaction are stalled during this period.

The same full resynchronization scheme is used for a read transaction, and the same stall period applies. A register read following a write to the same register is always coherent.

This mode is functional regardless of the ratio between the OCP interface frequency and the timer clock frequency. Recommended frequency range is freq(timer clock) > = freq (OCP interface clock) / 4.

22.2.4.12.2 Reading From Timer Counter Registers

In 16-bit access mode, reading the 16 LSBs from the timer counter registers (TCRR, TCAR1, and TCAR2) captures the current timer counter value. This must be followed by reading the 16 MSBs. The synchronization schemes for read posted and read non-posted transactions are the same as the corresponded write transactions described before.

NOTE: LSB/MSB accesses cannot be interleaved (that is, the sequence LSB register 1, LSB register 2, MSB register 1, MSB register 2 is not supported).

22.2.4.12.2.1 Read Posted

Read posted mode is functional regardless of the ratio between the OCP interface frequency and the functional clock frequency. The following functional frequency range is recommended:

freq(timer) < freq(OCP) / 4

Read posted mode is used if TSICR[2] POSTED is set to 0x1, or if TSICR[3]READ_MODE is set to 0. Read posted mode uses a posted-read scheme for reading any internal timer register. The read transaction is immediately acknowledged on the OCP interface. Because the value to be read has been previously resynchronized, neither the interconnect nor the device that requested the read transaction are stalled.

Read posted mode applies to the following registers:

- TCRR
- TCAR1
- TCAR2
- TCVR
- TOWR

These registers require resynchronization from functional to OCP clock domains.

22.2.4.12.2.2 Read Non-posted

Read non-posted mode is functional regardless of the ratio between the OCP interface frequency and the functional clock frequency. The following functional frequency range is recommended:

freq(timer) ≥ freq(OCP) / 4

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Read non-posted mode is used if TSICR[2] POSTED = 0x0 and TSICR[3] READ_MODE = 0x1 . Read non-posted mode uses a non-posted read scheme for reading internal timer registers. The read transaction is not acknowledged on the OCP interface until the effective read operation occurs, after the resynchronization in the timer clock domain. The result is that both the interconnect and the device that requested the read transaction are stalled during this period.

Read non-posted mode applies to the following registers:

- TCRR
- TCAR1
- TCAR2
- TCVR
- TOWR

These registers require resynchronization from functional to OCP clock domains.

22.2.4.13 Posted Mode Selection

A choice between two synchronization modes is made. This choice takes into account the frequency ratio and the stall periods that can be supported by the system without impacting the global performance.

The posted mode selection applies only to registers that require synchronization on or from the timer clock domain.

For write operation, the following registers are affected by posted or non-posted selection:

- TCLR
- TLDR
- TCRR
- TTGR
- TMAR
- TPIR
- TNIR
- TCVR
- TOCR
- TOWR

For read operation, the following registers are affected by posted or non-posted selection:

- TCRR
- TCAR1
- TCAR2
- TCVR
- TOWR

The OCP clock domain synchronous registers (TIDR, TIOCP_CFG, IRQSTATUS, IRQSTATUS_SET, IRQWAKEEN, TWPS and TSICR) are not affected by the posted or non-posted mode selection. The operation (read or write) is effective and acknowledged one OCP clock cycle after the command assertion.

The configuration of the posted or non-posted mode can be changed (overwritten) by software by setting the TSICR[2] POSTED bit. The TSICR[3] READ_MODE bit defines how the read operation is performed when the module is configured in non-posted mode. The following cases are possible:

- TSICR[2] POSTED = 0x1 and TSICR[3]READ_MODE = x (don’t care): Read and write operations are expected in posted mode.
- TSICR[2] POSTED = 0x0 and TSICR[3]READ_MODE = 0x0: The write operation is executed in non-posted mode and read is executed in posted mode.
- TSICR[2] POSTED = 0x0 and TSICR[3]READ_MODE = 0x1: Write is executed in non-posted mode and read is executed in non-posted mode.

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22.2.5 GP Timer Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

22.2.5.1 Global Initialization

22.2.5.1.1 Global Initialization of Surrounding Modules

This section identifies the requirements for initializing the surrounding modules when the GP timer module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the GP timer. For more information, see Section 22.2.3, *GP Timers Integration*, and Section 22.2.2, *GP Timers Environment*. Table 22-10 summarizes the surrounding modules.

Table 22-10. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface and functional clocks must be enabled. For more information about the module configuration, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
Control module	The module-specific pad muxing must be set in the control module. For more information about the module configuration, see Section 18.4.8 *PAD Functional Multiplexing and Configuration,* in Chapter 18, *Control Module*.
MPU INTC	The MPU INTC configuration must be done to enable the interrupts from the GP timer module. See Chapter 4, *MPU Subsystem*.
DSP INTC	The DSP INTC configuration must be done to enable the interrupts from GP timer module. See Section 5.3.2.6, *INTC,* in Chapter 5, *DSP Subsystem*.

22.2.5.1.2 GP Timer Module Global Initialization

22.2.5.1.2.1 Main Sequence – GP Timer Module Global Initialization

Table 22-11 identifies the main steps for initializing the GP timer module when the module is to be used for the first time.

Table 22-11. GP Timer Module Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	TIOCP_CFG[0] SOFTRESET	0x1
Wait until reset release?	TIOCP_CFG[0] SOFTRESET	0x0
Configure idle mode.	TIOCP_CFG[3:2] IDLEMODE	xx
Enable wake-up interrupt events.	IRQWAKEEN[2:0]	x
Select posted mode.	TSICR[2] POSTED	x

22.2.5.2 Operational Mode Configuration

22.2.5.2.1 GP Timer Mode

22.2.5.2.1.1 Main Sequence – GP Timer Mode Configuration

Table 22-12 lists the steps in the GP timer mode configuration.

Table 22-12. GP Timer Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	TCLR[1] AR	x
Set prescale timer value.	TCLR[4:2] PTV	xxx

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Table 22-12. GP Timer Mode Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Enable prescaler.	TCLR[5] PRE	0x1
Enable overflow interrupt.	IRQSTATUS_SET[1] OVF_EN_FLAG(1) IRQENABLE_SET[1] OVF_EN_FLAG(2)	0x1
Load timer counter value.	TCRR	xxx
Load timer load value.	TLDR	xxx
Start the timer.	TCLR[0] ST	0x1

(1) Applies only to TIMER1, TIMER2, and TIMER10.
(2) Applies to TIMER3 through TIMER 9, and TIMER11.

22.2.5.2.2 GP Timer Compare Mode

22.2.5.2.2.1 Main Sequence – GP Timer Compare Mode Configuration

Table 22-13 lists the steps in the GP timer compare mode configuration.

Table 22-13. GP Timer Compare Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	TCLR[1] AR	x
Set prescale timer value.	TCLR[4:2] PTV	xxx
Enable prescaler.	TCLR[5] PRE	0x1
Enable match interrupt.	IRQSTATUS_SET[0] MAT_EN_FLAG(1) IRQENABLE_SET[0]MAT_EN_FLAG(2)	0x1
Load timer counter value.	TCRR	xxx
Load timer compare value.	TMAR	xxx
Enable compare mode.	TCLR[6] CE	0x1
Start the timer.	TCLR[0] ST	0x1

(1) Applies only to TIMER1, TIMER2, and TIMER10.
(2) Applies to TIMER3 through TIMER9, and TIMER11.

22.2.5.2.3 GP Timer Capture Mode

22.2.5.2.3.1 Main Sequence – GP Timer Capture Mode Configuration

Table 22-14 lists the steps in the GP timer capture mode configuration.

Table 22-14. GP Timer Capture Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Initialize capture mode.	See Section 22.2.5.2.3.2.	
Enable capture interrupt.	IRQENABLE_SET[2] TCAR_EN_FLAG (1) or IRQSTATUS_SET[2] TCAR_EN_FLAG (2)	0x1
Start the timer.	TCLR[0] ST	0x1
Detect event.	See Section 22.2.5.2.3.3.	

(1) Applies only to TIMER3 through TIMER9, and TIMER11.
(2) Applies only to TIMER1, TIMER2, and TIMER10.

22.2.5.2.3.2 Subsequence – Initialize Capture Mode

Table 22-15 lists the steps to initialize capture mode.

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Table 22-15. Initialize Capture Mode

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	TCLR[1] AR	x
Set prescale timer value.	TCLR[4:2] PTV	xxx
Enable prescaler.	TCLR[5] PRE	0x1
Select TIMERx (where x = 8 to 11). Capture input at device pin dmtimerx_pwm_evt.	TCLR[14] GPO_CFG(1)	0x1
Select single or second event capture.	TCLR[13] CAPT_MODE	x
Select transition capture mode.	TCLR[9:8] TCM	xx

(1) TIMER5, TIMER6, and TIMER8 through TIMER11

22.2.5.2.3.3 Subsequence – Detect Event

Table 22-16 lists the steps in detecting an event.

Table 22-16. Detect Event

Step	Register/Bit Field/Programming Model	Value
Wait until event detected?	IRQSTATUS[2] TCAR_IT_FLAG	= 0x1
Read timer capture value.	TCAR1 and/or TCAR2	
Clear capture interrupt request.	IRQSTATUS[2] TCAR_IT_FLAG	0x1

22.2.5.2.4 GP Timer PWM Mode

22.2.5.2.4.1 Main Sequence – GP Timer PWM Mode Configuration

Table 22-17 lists the steps in the GP timer PWM mode configuration.

Table 22-17. GP Timer PWM Mode Configuration

Step	Register/Bit Field/Programming Model	Value
Select autoreload mode.	TCLR[1] AR	x
Set prescale timer value.	TCLR[4:2] PTV	xxx
Enable prescaler.	TCLR[5] PRE	0x1
Select trigger output mode.	TCLR[11:10] TRG	xx
Select pulse or toggle modulation PWM mode.	TCLR[12] PT	x
Select TIMERx (where x = 8 to 11) PWM output at device pin dmtimerx_pwm_evt.	TCLR[14] GPO_CFG(1)	0x0
Configure PWM output pin default value.	TCLR[7] SCPWM	x
Load timer load value.	TLDR	xxx
Load timer compare value.	TMAR	xxx
Enable compare.	TCLR[6] CE	0x1
Start the timer.	TCLR[0] ST	0x1

(1) Applies only to TIMER8 through TIMER11

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22.2.6 GP Timer Register Manual

22.2.6.1 GP Timer Instance Summary

Table 22-18 lists the base address and block size for the GP timer module instances.

Table 22-18. GP Timer Instance Summary

Module Name	Base Address L4 Interconnect	Base Address L3_MAIN Interconnect	Base Address Cortex-A15 Private Access	Base Address DSP Private Access	Size
TIMER2	0x4803 2000	–	–	–	4 KiB
TIMER3	0x4803 4000	–	–	–	4 KiB
TIMER4	0x4803 6000	–	–	–	4 KiB
TIMER9	0x4803 E000	–	–	–	4 KiB
TIMER10	0x4808 6000	–	–	–	4 KiB
TIMER11	0x4808 8000	–	–	–	4 KiB
TIMER5	–	0x4903 8000	0x4013 8000	0x3 8000	4 KiB
TIMER6	–	0x4903 A000	0x4013 A000	0x3 A000	4 KiB
TIMER7	–	0x4903 C000	0x4013 C000	0x3 C000	4 KiB
TIMER8	–	0x4903 E000	0x4013 E000	0x3 E000	4 KiB
TIMER1	0x4AE1 8000	–	–	–	4 KiB

NOTE: Private access is access that does not use the L3/L4 interconnects.

22.2.6.2 GP Timer Registers

22.2.6.2.1 GP Timer Register Summary

CAUTION

The GP timer registers are limited to 32- and 16-bit data accesses; 8-bit access is not allowed and can corrupt the register content.

Table 22-19 through Table 22-25 provide the register summary and associated offset addresses for the 11 GP timer internal registers.

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Table 22-19. TIMER1, TIMER2, and TIMER10 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TIMER1 Physical Address L4 Interconnect	TIMER2 Physical Address L4 Interconnect	TIMER10 Physical Address L4 Interconnect
TIDR	RO	32	0x0000 0000	0x4AE1 8000	0x4803 2000	0x4808 6000
TIOCP_CFG	RW	32	0x0000 0010	0x4AE1 8010	0x4803 2010	0x4808 6010
RESERVED	R	32	0x0000 0020	0x4AE1 8020	0x4803 2020	0x4808 6020
IRQSTATUS_RAW	RW	32	0X0000 0024	0x4AE1 8024	0x4803 2024	0x4808 6024
IRQSTATUS	RW	32	0X0000 0028	0x4AE1 8028	0x4803 2028	0x4808 6028
IRQSTATUS_SET	RW	32	0X0000 002C	0x4AE1 802C	0x4803 202C	0x4808 602C
IRQSTATUS_CLR	RW	32	0X0000 0030	0x4AE1 8030	0x4803 2030	0x4808 6030
IRQWAKEEN	RW	32	0X0000 0034	0x4AE1 8034	0x4803 2034	0x4808 6034
TCLR	RW	32	0x0000 0038	0x4AE1 8038	0x4803 2038	0x4808 6038
TCRR	RW	32	0x0000 003C	0x4AE1 803C	0x4803 203C	0x4808 603C
TLDR	RW	32	0x0000 0040	0x4AE1 8040	0x4803 2040	0x4808 6040
TTGR	RW	32	0x0000 0044	0x4AE1 8044	0x4803 2044	0x4808 6044
TWPS	R0	32	0x0000 0048	0x4AE1 8048	0x4803 2048	0x4808 6048
TMAR	RW	32	0x0000 004C	0x4AE1 804C	0x4803 204C	0x4808 604C
TCAR1	RO	32	0x0000 0050	0x4AE1 8050	0x4803 2050	0x4808 6050
TSICR	RW	32	0x0000 0054	0x4AE1 8054	0x4803 2054	0x4808 6054
TCAR2	RO	32	0x0000 0058	0x4AE1 8058	0x4803 2058	0x4808 6058
TPIR	RW	32	0x0000 005C	0x4AE1 805C	0x4803 205C	0x4808 605C
TNIR	RW	32	0x0000 0060	0x4AE1 8060	0x4803 2060	0x4808 6060
TCVR	RW	32	0x0000 0064	0x4AE1 8064	0x4803 2064	0x4808 6064
TOCR	RW	32	0x0000 0068	0x4AE1 8068	0x4803 2068	0x4808 6068
TOWR	RW	32	0x0000 006C	0x4AE1 806C	0x4803 206C	0x4808 606C

Table 22-20. TIMER3 and TIMER4 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TIMER3 Physical Address L4 Interconnect	TIMER4 Physical Address L4 Interconnect
TIDR	R	32	0x0000 0000	0x4803 4000	0x4803 6000
TIOCP_CFG	RW	32	0x0000 0010	0x4803 4010	0x4803 6010
RESERVED	R	32	0x0000 0020	0x4803 401C	0x4803 601C
IRQSTATUS_RAW	RW	32	0x0000 0024	0x4803 4024	0x4803 6024
IRQSTATUS	RW	32	0x0000 0028	0x4803 4028	0x4803 6028
IRQENABLE_SET	RW	32	0x0000 002C	0x4803 402C	0x4803 602C
IRQENABLE_CLR	RW	32	0x0000 0030	0x4803 4030	0x4803 6030
IRQWAKEEN	RW	32	0x0000 0034	0x4803 4034	0x4803 6034
TCLR	RW	32	0x0000 0038	0x4803 4038	0x4803 6038
TCRR	RW	32	0x0000 003C	0x4803 403C	0x4803 603C
TLDR	RW	32	0x0000 0040	0x4803 4040	0x4803 6040
TTGR	RW	32	0x0000 0044	0x4803 4044	0x4803 6044
TWPS	R	32	0x0000 0048	0x4803 4048	0x4803 6048
TMAR	RW	32	0x0000 004C	0x4803 404C	0x4803 604C
TCAR1	R	32	0x0000 0050	0x4803 4050	0x4803 6050
TSICR	RW	32	0x0000 0054	0x4803 4054	0x4803 6054
TCAR2	R	32	0x0000 0058	0x4803 4058	0x4803 6058

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Table 22-21. TIMER5 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TIMER5 Physical Address L3_MAIN Interconnect	TIMER5 Physical Address Cortex-A15 Private Access	TIMER5 Physical Address DSP Private Access
TIDR	R	32	0x0000 0000	0x4903 8000	0x4013 8000	0x3 8000
TIOCP_CFG	RW	32	0x0000 0010	0x4903 8010	0x4013 8010	0x3 8010
RESERVED	R	32	0x0000 0020	0x4903 8020	0x4013 8020	0x3 8020
IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 8024	0x4013 8024	0x3 8024
IRQSTATUS	RW	32	0x0000 0028	0x4903 8028	0x4013 8028	0x3 8028
IRQENABLE_SET	RW	32	0x0000 002C	0x4903 802C	0x4013 802C	0x3 802C
IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 8030	0x4013 8030	0x3 8030
IRQWAKEEN	RW	32	0x0000 0034	0x4903 8034	0x4013 8034	0x3 8034
TCLR	RW	32	0x0000 0038	0x4903 8038	0x4013 8038	0x3 8038
TCRR	RW	32	0x0000 003C	0x4903 803C	0x4013 803C	0x3 803C
TLDR	RW	32	0x0000 0040	0x4903 8040	0x4013 8040	0x3 8040
TTGR	RW	32	0x0000 0044	0x4903 8044	0x4013 8044	0x3 8044
TWPS	R	32	0x0000 0048	0x4903 8048	0x4013 8048	0x3 8048
TMAR	RW	32	0x0000 004C	0x4903 804C	0x4013 804C	0x3 804C
TCAR1	R	32	0x0000 0050	0x4903 8050	0x4013 8050	0x3 8050
TSICR	RW	32	0x0000 0054	0x4903 8054	0x4013 8054	0x3 8054
TCAR2	R	32	0x0000 0058	0x4903 8058	0x4013 8058	0x3 8058

Table 22-22. TIMER6 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TIMER6 Physical Address L3_MAIN Interconnect	TIMER6 Physical Address Cortex-A15 Private Access	TIMER6 Physical Address DSP Private Access
TIDR	R	32	0x0000 0000	0x4903 A000	0x4013 A000	0x3 A000
TIOCP_CFG	RW	32	0x0000 0010	0x4903 A010	0x4013 A010	0x3 A010
RESERVED	R	32	0x0000 0020	0x4903 A020	0x4013 A020	0x3 A020
IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 A024	0x4013 A024	0x3 A024
IRQSTATUS	RW	32	0x0000 0028	0x4903 A028	0x4013 A028	0x3 A028
IRQENABLE_SET	RW	32	0x0000 002C	0x4903 A02C	0x4013 A02C	0x3 A02C
IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 A030	0x4013 A030	0x3 A030
IRQWAKEEN	RW	32	0x0000 0034	0x4903 A034	0x4013 A034	0x3 A034
TCLR	RW	32	0x0000 0038	0x4903 A038	0x4013 A038	0x3 A038
TCRR	RW	32	0x0000 003C	0x4903 A03C	0x4013 A03C	0x3 A03C
TLDR	RW	32	0x0000 0040	0x4903 A040	0x4013 A040	0x3 A040
TTGR	RW	32	0x0000 0044	0x4903 A044	0x4013 A044	0x3 A044
TWPS	R	32	0x0000 0048	0x4903 A048	0x4013 A048	0x3 A048
TMAR	RW	32	0x0000 004C	0x4903 A04C	0x4013 A04C	0x3 A04C
TCAR1	R	32	0x0000 0050	0x4903 A050	0x4013 A050	0x3 A050
TSICR	RW	32	0x0000 0054	0x4903 A054	0x4013 A054	0x3 A054
TCAR2	R	32	0x0000 0058	0x4903 A058	0x4013 A058	0x3 A058

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Table 22-23. TIMER7 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TIMER7 Physical Address L3_MAIN Interconnect	TIMER7 Physical Address Cortex-A15 Private Access	TIMER7 Physical Address DSP Private Access
TIDR	R	32	0x0000 0000	0x4903 C000	0x4013 C000	0x3 C000
TIOCP_CFG	RW	32	0x0000 0010	0x4903 C010	0x4013 C010	0x3 C010
RESERVED	R	32	0x0000 0020	0x4903 C020	0x4013 C020	0x3 C020
IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 C024	0x4013 C024	0x3 C024
IRQSTATUS	RW	32	0x0000 0028	0x4903 C028	0x4013 C028	0x3 C028
IRQENABLE_SET	RW	32	0x0000 002C	0x4903 C02C	0x4013 C02C	0x3 C02C
IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 C030	0x4013 C030	0x3 C030
IRQWAKEEN	RW	32	0x0000 0034	0x4903 C034	0x4013 C034	0x3 C034
TCLR	RW	32	0x0000 0038	0x4903 C038	0x4013 C038	0x3 C038
TCRR	RW	32	0x0000 003C	0x4903 C03C	0x4013 C03C	0x3 C03C
TLDR	RW	32	0x0000 0040	0x4903 C040	0x4013 C040	0x3 C040
TTGR	RW	32	0x0000 0044	0x4903 C044	0x4013 C044	0x3 C044
TWPS	R	32	0x0000 0048	0x4903 C048	0x4013 C048	0x3 C048
TMAR	RW	32	0x0000 004C	0x4903 C04C	0x4013 C04C	0x3 C04C
TCAR1	R	32	0x0000 0050	0x4903 C050	0x4013 C050	0x3 C050
TSICR	RW	32	0x0000 0054	0x4903 C054	0x4013 C054	0x3 C054
TCAR2	R	32	0x0000 0058	0x4903 C058	0x4013 C058	0x3 C058

Table 22-24. TIMER8 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TIMER8 Physical Address L3_MAIN Interconnect	TIMER8 Physical Address Cortex-A15 Private Access	TIMER8 Physical Address DSP Private Access
TIDR	R	32	0x0000 0000	0x4903 E000	0x4013 E000	0x3 E000
TIOCP_CFG	RW	32	0x0000 0010	0x4903 E010	0x4013 E010	0x3 E010
RESERVED	R	32	0x0000 0020	0x4903 E020	0x4013 E020	0x3 E020
IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 E024	0x4013 E024	0x3 E024
IRQSTATUS	RW	32	0x0000 0028	0x4903 E028	0x4013 E028	0x3 E028
IRQENABLE_SET	RW	32	0x0000 002C	0x4903 E02C	0x4013 E02C	0x3 E02C
IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 E030	0x4013 E030	0x3 E030
IRQWAKEEN	RW	32	0x0000 0034	0x4903 E034	0x4013 E034	0x3 E034
TCLR	RW	32	0x0000 0038	0x4903 E038	0x4013 E038	0x3 E038
TCRR	RW	32	0x0000 003C	0x4903 E03C	0x4013 E03C	0x3 E03C
TLDR	RW	32	0x0000 0040	0x4903 E040	0x4013 E040	0x3 E040
TTGR	RW	32	0x0000 0044	0x4903 E044	0x4013 E044	0x3 E044
TWPS	R	32	0x0000 0048	0x4903 E048	0x4013 E048	0x3 E048
TMAR	RW	32	0x0000 004C	0x4903 E04C	0x4013 E04C	0x3 E04C
TCAR1	R	32	0x0000 0050	0x4903 E050	0x4013 E050	0x3 E050
TSICR	RW	32	0x0000 0054	0x4903 E054	0x4013 E054	0x3 E054
TCAR2	R	32	0x0000 0058	0x4903 E058	0x4013 E058	0x3 E058

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Table 22-25. TIMER9 and TIMER11 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	TIMER9 Physical Address L4 Interconnect	TIMER11 Physical Address L4 Interconnect
TIDR	R	32	0x0000 0000	0x4803 E000	0x4808 8000
TIOCP_CFG	RW	32	0x0000 0010	0x4803 E010	0x4808 8010
RESERVED	R	32	0x0000 0020	0x4803 E020	0x4808 8020
IRQSTATUS_RAW	RW	32	0x0000 0024	0x4803 E024	0x4808 8024
IRQSTATUS	RW	32	0x0000 0028	0x4803 E028	0x4808 8028
IRQENABLE_SET	RW	32	0x0000 002C	0x4803 E02C	0x4808 802C
IRQENABLE_CLR	RW	32	0x0000 0030	0x4803 E030	0x4808 8030
IRQWAKEEN	RW	32	0x0000 0034	0x4803 E034	0x4808 8034
TCLR	RW	32	0x0000 0038	0x4803 E038	0x4808 8038
TCRR	RW	32	0x0000 003C	0x4803 E03C	0x4808 803C
TLDR	RW	32	0x0000 0040	0x4803 E040	0x4808 8040
TTGR	RW	32	0x0000 0044	0x4803 E044	0x4808 8044
TWPS	R	32	0x0000 0048	0x4803 E048	0x4808 8048
TMAR	RW	32	0x0000 004C	0x4803 E04C	0x4808 804C
TCAR1	R	32	0x0000 0050	0x4803 E050	0x4808 8050
TSICR	RW	32	0x0000 0054	0x4803 E054	0x4808 8054
TCAR2	R	32	0x0000 0058	0x4803 E058	0x4808 8058

22.2.6.2.2 GP Timer Register Description

through describe the individual GP timer registers.

Table 22-26. TIDR

Address Offset	0x0000 0000		
Physical Address	0x4AE1 8000	**Instance**	TIMER1_L4
	0x4803 2000		TIMER2_L4
	0x4808 6000		TIMER10_L4
	0x4803 4000		TIMER3_L4
	0x4803 6000		TIMER4_L4
	0x4903 8000		TIMER5_MAIN_L3
	0x4013 8000		TIMER5_CORTEX-A15
	0x3 8000		TIMER5_DSP
	0x4903 A000		TIMER6_MAIN_L3
	0x4013 A000		TIMER6_CORTEX-A15
	0x3 A000		TIMER6_DSP
	0x4903 C000		TIMER7_MAIN_L3
	0x4013 C000		TIMER7_CORTEX-A15
	0x3 C000		TIMER7_DSP
	0x4903 E000		TIMER8_MAIN_L3
	0x4013 E000		TIMER8_CORTEX-A15
	0x3 E000		TIMER8_DSP
	0x4803 E000		TIMER9_L4
	0x4808 8000		TIMER11_L4
Description	This read-only register contains the revision number of the module. A write to this register has no effect. This register is used by software to track features, bugs, and compatibility.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

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Bits	Field Name	Description	Type	Reset
31: 0	REVISION	IP Revision	R	0x– [1]

[1] TI internal data

Table 22-27. Register Call Summary for Register TIDR

General-Purpose Timers

- Accessing GP Timer Registers: [0] [1]
- Posted Mode Selection: [2]
- GP Timer Register Summary: [3] [4] [5] [6] [7] [8] [9]

Table 22-28. TIOCP_CFG

Address Offset	0x0000 0010		
Physical Address	0x4AE1 8010	**Instance**	TIMER1_L4
	0x4803 2010		TIMER2_L4
	0x4808 6010		TIMER10_L4
	0x4803 4010		TIMER3_L4
	0x4803 6010		TIMER4_L4
	0x4903 8010		TIMER5_MAIN_L3
	0x4013 8010		TIMER5_CORTEX-A15
	0x3 8010		TIMER5_DSP
	0x4903 A010		TIMER6_MAIN_L3
	0x4013 A010		TIMER6_CORTEX-A15
	0x3 A010		TIMER6_DSP
	0x4903 C010		TIMER7_MAIN_L3
	0x4013 C010		TIMER7_CORTEX-A15
	0x3 C010		TIMER7_DSP
	0x4903 E010		TIMER8_MAIN_L3
	0x4013 E010		TIMER8_CORTEX-A15
	0x3 E010		TIMER8_DSP
	0x4803 E010		TIMER9_L4
	0x4808 8010		TIMER11_L4
Description	This register controls the various parameters of the L4 interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IDLEMODE		EMUFREE	SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:2	IDLEMODE	Power management, req/ack control 0x0: Force-idle mode: local target idle state follows (acknowledges) the system idle requests unconditionally, that is, regardless of the IP module internal requirements. Back-up mode, for debug only. 0x1: No-idle mode: local target never enters idle state. Back-up mode, for debug only. 0x2: Smart-idle mode: local target idle state eventually follows (acknowledges) the system idle requests, depending on the IP module internal requirements. IP module should not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Smart-idle wake-up-capable mode: local target idle state eventually follows (acknowledges) the system idle requests, depending on the IP module internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state. Mode is relevant only if the appropriate IP module s*wake-up* output(s) is (are) implemented.	RW	0x0
1	EMUFREE	Emulation mode 0x0: The timer is frozen in emulation mode (PINSUSPENDN signal active). 0x1: The timer runs free, regardless of PINSUSPENDN value.	RW	0
0	SOFTRESET	Software reset 0x0: Read 0: reset done, no pending action Write 0: No action 0x1: Read 1: initiate software reset Write 1: Reset ongoing	RW	0

Table 22-29. Register Call Summary for Register TIOCP_CFG

General-Purpose Timers

- Power Management: [0]
- Wake-Up Capability: [1]
- Software Reset: [2] [3] [4]
- Timer Under Emulation: [5] [6]
- Accessing GP Timer Registers: [7] [8]
- Writing to Timer Registers: [9]
- Posted Mode Selection: [10]
- Main Sequence – GP Timer Module Global Initialization: [11] [12] [13]
- GP Timer Register Summary: [14] [15] [16] [17] [18] [19] [20]

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Table 22-30. IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x4AE1 8024	**Instance**	TIMER1_L4
	0x4803 2024		TIMER2_L4
	0x4808 6024		TIMER10_L4
	0x4803 4024		TIMER3_L4
	0x4803 6024		TIMER4_L4
	0x4903 8024		TIMER5_MAIN_L3
	0x4013 8024		TIMER5_CORTEX-A15
	0x3 8024		TIMER5_DSP
	0x4903 A024		TIMER6_MAIN_L3
	0x4013 A024		TIMER6_CORTEX-A15
	0x3 A024		TIMER6_DSP
	0x4903 C024		TIMER7_MAIN_L3
	0x4013 C024		TIMER7_CORTEX-A15
	0x3 C024		TIMER7_DSP
	0x4903 E024		TIMER8_MAIN_L3
	0x4013 E024		TIMER8_CORTEX-A15
	0x3 E024		TIMER8_DSP
	0x4803 E024		TIMER9_L4
	0x4808 8024		TIMER11_L4
Description	Component interrupt-request status. Check the corresponding secondary status register. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_IT_FLAG	IRQ status for capture Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Trigger IRQ event by software.	RW	0
1	OVF_IT_FLAG	IRQ status for overflow Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Trigger IRQ event by software.	RW	0
0	MAT_IT_FLAG	IRQ status for match Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Trigger IRQ event by software.	RW	0

Table 22-31. Register Call Summary for Register IRQSTATUS_RAW

General-Purpose Timers

- Accessing GP Timer Registers: [0] [1]
- GP Timer Register Summary: [2] [3] [4] [5] [6] [7] [8]

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Table 22-32. IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4AE1 8028	**Instance**	TIMER1_L4
	0x4803 2028		TIMER2_L4
	0x4808 6028		TIMER10_L4
	0x4803 4028		TIMER3_L4
	0x4803 6028		TIMER4_L4
	0x4903 8028		TIMER5_MAIN_L3
	0x4013 8028		TIMER5_CORTEX-A15
	0x3 8028		TIMER5_DSP
	0x4903 A028		TIMER6_MAIN_L3
	0x4013 A028		TIMER6_CORTEX-A15
	0x3 A028		TIMER6_DSP
	0x4903 C028		TIMER7_MAIN_L3
	0x4013 C028		TIMER7_CORTEX-A15
	0x3 C028		TIMER7_DSP
	0x4903 E028		TIMER8_MAIN_L3
	0x4013 E028		TIMER8_CORTEX-A15
	0x3 E028		TIMER8_DSP
	0x4803 E028		TIMER9_L4
	0x4808 8028		TIMER11_L4
Description	Component interrupt-request status. Check the corresponding secondary status register. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_IT_FLAG	IRQ status for capture Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Clear any pending event.	RW	0
1	OVF_IT_FLAG	IRQ status for overflow Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Clear any pending event.	RW	0
0	MAT_IT_FLAG	IRQ status for match Read 0: No event pending Write 0: No action Read 1: IRQ event pending Write 1: Clear any pending event.	RW	0

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Table 22-33. Register Call Summary for Register IRQSTATUS

General-Purpose Timers

- Wake-Up Capability: [0]
- GP Timer Interrupts: [1]
- 1-ms Tick Generation (Only TIMER1, TIMER2, and TIMER10): [2]
- Capture Mode Functionality: [3] [4] [5] [6]
- Accessing GP Timer Registers: [7] [8]
- Writing to Timer Registers: [9]
- Posted Mode Selection: [10]
- Subsequence – Detect Event: [11] [12]
- GP Timer Register Summary: [13] [14] [15] [16] [17] [18] [19]

Table 22-34. IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x4803 402C	**Instance**	TIMER3_L4
	0x4803 602C		TIMER4_L4
	0x4903 802C		TIMER5_MAIN_L3
	0x4013 802C		TIMER5_CORTEX-A15
	0x3 802C		TIMER5_DSP
	0x4903 A02C		TIMER6_MAIN_L3
	0x4013 A02C		TIMER6_CORTEX-A15
	0x3 A02C		TIMER6_DSP
	0x4903 C02C		TIMER7_MAIN_L3
	0x4013 C02C		TIMER7_CORTEX-A15
	0x3 C02C		TIMER7_DSP
	0x4903 E02C		TIMER8_MAIN_L3
	0x4013 E02C		TIMER8_CORTEX-A15
	0x3 E02C		TIMER8_DSP
	0x4803 E02C		TIMER9_L4
	0x4808 802C		TIMER11_L4
Description	Component interrupt-request enable. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_EN_FLAG	OVF_EN_FLAG	MAT_EN_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_EN_FLAG	IRQ enable for compare Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled Write 1: Set IRQ enable.	RW	0
1	OVF_EN_FLAG	IRQ enable for overflow Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Set IRQ enable.	RW	0
0	MAT_EN_FLAG	IRQ enable for match Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Set IRQ enable.	RW	0

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Table 22-35. Register Call Summary for Register IRQENABLE_SET

General-Purpose Timers

- GP Timer Functional Description: [0]
- GP Timer Interrupts: [1]
- Timer Mode Functionality: [2]
- Capture Mode Functionality: [3]
- Compare Mode Functionality: [4]
- Accessing GP Timer Registers: [5] [6]
- Writing to Timer Registers: [7]
- Main Sequence – GP Timer Mode Configuration: [8]
- Main Sequence – GP Timer Compare Mode Configuration: [9]
- Main Sequence – GP Timer Capture Mode Configuration: [10]
- GP Timer Register Summary: [11] [12] [13] [14] [15] [16]

Table 22-36. IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x4803 4030	**Instance**	TIMER3_L4
	0x4803 6030		TIMER4_L4
	0x4903 8030		TIMER5_MAIN_L3
	0x4013 8030		TIMER5_CORTEX-A15
	0x3 8030		TIMER5_DSP
	0x4903 A030		TIMER6_MAIN_L3
	0x4013 A030		TIMER6_CORTEX-A15
	0x3 A030		TIMER6_DSP
	0x4903 C030		TIMER7_MAIN_L3
	0x4013 C030		TIMER7_CORTEX-A15
	0x3 C030		TIMER7_DSP
	0x4903 E030		TIMER8_MAIN_L3
	0x4013 E030		TIMER8_CORTEX-A15
	0x3 E030		TIMER8_DSP
	0x4803 E030		TIMER9_L4
	0x4808 8030		TIMER11_L4
Description	Component interrupt-request enable. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_EN_FLAG	OVF_EN_FLAG	MAT_EN_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_EN_FLAG	IRQ enable for compare Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Clear IRQ enable.	RW	0
1	OVF_EN_FLAG	IRQ enable for overflow Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Clear IRQ enable.	RW	0

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Bits	Field Name	Description	Type	Reset
0	MAT_EN_FLAG	IRQ enable for match Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Clear IRQ enable.	RW	0

Table 22-37. Register Call Summary for Register IRQENABLE_CLR

General-Purpose Timers

- GP Timer Functional Description: [0]
- GP Timer Interrupts: [1]
- Accessing GP Timer Registers: [2] [3]
- Writing to Timer Registers: [4]
- GP Timer Register Summary: [5] [6] [7] [8] [9] [10]

Table 22-38. IRQWAKEEN

Address Offset	0x0000 0034		
Physical Address	0x4AE1 8034	**Instance**	TIMER1_L4
	0x4803 2034		TIMER2_L4
	0x4808 6034		TIMER10_L4
	0x4803 4034		TIMER3_L4
	0x4803 6034		TIMER4_L4
	0x4903 8034		TIMER5_MAIN_L3
	0x4013 8034		TIMER5_CORTEX-A15
	0x3 8034		TIMER5_DSP
	0x4903 A034		TIMER6_MAIN_L3
	0x4013 A034		TIMER6_CORTEX-A15
	0x3 A034		TIMER6_DSP
	0x4903 C034		TIMER7_MAIN_L3
	0x4013 C034		TIMER7_CORTEX-A15
	0x3 C034		TIMER7_DSP
	0x4903 E034		TIMER8_MAIN_L3
	0x4013 E034		TIMER8_CORTEX-A15
	0x3 E034		TIMER8_DSP
	0x4803 E034		TIMER9_L4
	0x4808 8034		TIMER11_L4
Description	Wake-up-enabled events taking place when module is idle should generate an asynchronous wake-up.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_WUP_ENA	OVF_WUP_ENA	MAT_WUP_ENA

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_WUP_ENA	Wake-up generation for compare 0x0: Wake-up disabled 0x1: Wake-up enabled	RW	0
1	OVF_WUP_ENA	Wake-up generation for overflow 0x0: Wake-up disabled 0x1: Wake-up enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	MAT_WUP_ENA	Wake-up generation for match 0x0: Wake-up disabled 0x1: Wake-up enabled	RW	0

Table 22-39. Register Call Summary for Register IRQWAKEEN

General-Purpose Timers

- GP Timer Functional Description: [0] [1]
- Wake-Up Capability: [2]
- Accessing GP Timer Registers: [3] [4]
- Writing to Timer Registers: [5]
- Posted Mode Selection: [6]
- Main Sequence – GP Timer Module Global Initialization: [7]
- GP Timer Register Summary: [8] [9] [10] [11] [12] [13] [14]

Table 22-40. TCLR

Address Offset	0x0000 0038		
Physical Address	0x4AE1 8038	**Instance**	TIMER1_L4
	0x4803 2038		TIMER2_L4
	0x4808 6038		TIMER10_L4
	0x4803 4038		TIMER3_L4
	0x4803 6038		TIMER4_L4
	0x4903 8038		TIMER5_MAIN_L3
	0x4013 8038		TIMER5_CORTEX-A15
	0x3 8038		TIMER5_DSP
	0x4903 A038		TIMER6_MAIN_L3
	0x4013 A038		TIMER6_CORTEX-A15
	0x3 A038		TIMER6_DSP
	0x4903 C038		TIMER7_MAIN_L3
	0x4013 C038		TIMER7_CORTEX-A15
	0x3 C038		TIMER7_DSP
	0x4903 E038		TIMER8_MAIN_L3
	0x4013 E038		TIMER8_CORTEX-A15
	0x3 E038		TIMER8_DSP
	0x4803 E038		TIMER9_L4
	0x4808 8038		TIMER11_L4
Description	This register controls optional features specific to the timer functionality.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	GPO_CFG	CAPT_MODE	PT	TRG		TCM		SCPWM	CE	PRE	PTV			AR	ST

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	GPO_CFG	General-purpose output - this register directly drives the TIMERi_PORGPOCFG output pin. For specific use of the GPO_CFG bit, see Section 22.2.2.1, *GP Timer External System Interface*. 0x0: TIMERi_PORGPOCFG drives 0. 0x1: TIMERi_PORGPOCFG drives 1.	RW	0

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Bits	Field Name	Description	Type	Reset
13	CAPT_MODE	Capture mode select bit (first/second) 0x0: Single capture: Capture the first enabled capture event in TCAR1. 0x1: Capture on second event: Capture the second enabled capture event in TCAR2.	RW	0
12	PT	Pulse or toggle mode on TIMERi_PWM_out output pin 0x0: Pulse modulation 0x1: Toggle modulation	RW	0
11:10	TRG	Trigger output mode on TIMERi_PWM_out output pin 0x0: No trigger 0x1: Trigger on overflow. 0x2: Trigger on overflow and match. 0x3: Reserved	RW	0x0
9:8	TCM	Transition capture mode on TIMERi_EVENT_CAPTURE input pin (When the TCM field passed from (00) to any other combination, the TCAR_IT_FLAG and the edge detection logic are cleared.) 0x0: No capture 0x1: Capture on rising edges of TIMERi_EVENT_CAPTURE pin 0x2: Capture on falling edges of TIMERi_EVENT_CAPTURE pin 0x3: Capture on both edges of TIMERi_EVENT_CAPTURE pin	RW	0x0
7	SCPWM	Pulse width modulation output pin default setting This bit must be set or clear while the timer is stopped or the trigger is off. 0x0: Clear the TIMERi_PWM_out output pin and select positive pulse for pulse mode. 0x1: Set the TIMERi_PWM_out output pin and select negative pulse for pulse mode.	RW	0
6	CE	Compare enable 0x0: Compare mode is disable. 0x1: Compare mode is enable.	RW	0
5	PRE	Prescaler enable 0x0: The TIMER clock input pin clocks the counter. 0x1: The divided input pin clocks the counter.	RW	0
4:2	PTV	Prescale clock timer value The timer counter is prescaled with the value $2^{(PTV+1)}$. Example: PTV = 3, counter increases value (if started) after 16 functional clock periods.	RW	0x0
1	AR	Autoreload mode 0x0: One shot timer 0x1: Autoreload timer	RW	0
0	ST	Start/stop timer control 0x0: Stop timer: Only the counter is frozen. If one-shot mode selected (AR =0), this bit is automatically reset by internal logic when the counter is overflowed. 0x1: Start timer	RW	0

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Table 22-41. Register Call Summary for Register TCLR

General-Purpose Timers

- GP Timer External System Interface: [0] [1]
- Timer Mode Functionality: [2] [3] [4] [5] [6] [7] [8]
- Capture Mode Functionality: [9] [10] [11] [12] [13] [14] [15] [16] [17]
- Compare Mode Functionality: [18] [19] [20] [21]
- Prescaler Functionality: [22] [23]
- Pulse-Width Modulation: [24] [25] [26] [27] [28] [29] [30] [31] [32] [33]
- Timer Counting Rate: [34] [35] [36] [37] [38] [39] [40]
- Accessing GP Timer Registers: [41]
- Writing to Timer Registers: [42]
- Write Posting Synchronization Mode: [43]
- Posted Mode Selection: [44]
- Main Sequence – GP Timer Mode Configuration: [45] [46] [47] [48]
- Main Sequence – GP Timer Compare Mode Configuration: [49] [50] [51] [52] [53]
- Main Sequence – GP Timer Capture Mode Configuration: [54]
- Subsequence – Initialize Capture Mode: [55] [56] [57] [58] [59] [60]
- Main Sequence – GP Timer PWM Mode Configuration: [61] [62] [63] [64] [65] [66] [67] [68] [69]
- GP Timer Register Summary: [70] [71] [72] [73] [74] [75] [76]
- GP Timer Register Description: [77] [78]

Table 22-42. TCRR

Address Offset	0x0000 003C		
Physical Address	0x4AE1 803C	**Instance**	TIMER1_L4
	0x4803 203C		TIMER2_L4
	0x4808 603C		TIMER10_L4
	0x4803 403C		TIMER3_L4
	0x4803 603C		TIMER4_L4
	0x4903 803C		TIMER5_MAIN_L3
	0x4013 803C		TIMER5_CORTEX-A15
	0x3 803C		TIMER5_DSP
	0x4903 A03C		TIMER6_MAIN_L3
	0x4013 A03C		TIMER6_CORTEX-A15
	0x3 A03C		TIMER6_DSP
	0x4903 C03C		TIMER7_MAIN_L3
	0x4013 C03C		TIMER7_CORTEX-A15
	0x3 C03C		TIMER7_DSP
	0x4903 E03C		TIMER8_MAIN_L3
	0x4013 E03C		TIMER8_CORTEX-A15
	0x3 E03C		TIMER8_DSP
	0x4803 E03C		TIMER9_L4
	0x4808 803C		TIMER11_L4
Description	This register holds the value of the internal counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER_COUNTER																															

Bits	Field Name	Description	Type	Reset
31:0	TIMER_COUNTER	Value of TIMER counter	RW	0x0000 0000

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Table 22-43. Register Call Summary for Register TCRR

General-Purpose Timers

- Wake-Up Capability: [0] [1]
- Timer Mode Functionality: [2] [3] [4] [5] [6] [7] [8] [9] [10]
- 1-ms Tick Generation (Only TIMER1, TIMER2, and TIMER10): [11] [12] [13]
- Capture Mode Functionality: [14] [15]
- Compare Mode Functionality: [16] [17]
- Prescaler Functionality: [18] [19]
- Accessing GP Timer Registers: [20]
- Writing to Timer Registers: [21]
- Write Posting Synchronization Mode: [22] [23] [24] [25] [26] [27]
- Reading From Timer Counter Registers: [28]
- Read Posted: [29]
- Read Non-posted: [30]
- Posted Mode Selection: [31] [32]
- Main Sequence – GP Timer Mode Configuration: [33]
- Main Sequence – GP Timer Compare Mode Configuration: [34]
- GP Timer Register Summary: [35] [36] [37] [38] [39] [40] [41]
- GP Timer Register Description: [42] [43]
- TIMER1, TIMER2 , and TIMER10 Register Description: [44] [45] [46]

Table 22-44. TLDR

Address Offset	0x0000 0040		
Physical Address	0x4AE1 8040	**Instance**	TIMER1_L4
	0x4803 2040		TIMER2_L4
	0x4808 6040		TIMER10_L4
	0x4803 4040		TIMER3_L4
	0x4803 6040		TIMER4_L4
	0x4903 8040		TIMER5_MAIN_L3
	0x4013 8040		TIMER5_CORTEX-A15
	0x3 8040		TIMER5_DSP
	0x4903 A040		TIMER6_MAIN_L3
	0x4013 A040		TIMER6_CORTEX-A15
	0x3 A040		TIMER6_DSP
	0x4903 C040		TIMER7_MAIN_L3
	0x4013 C040		TIMER7_CORTEX-A15
	0x3 C040		TIMER7_DSP
	0x4903 E040		TIMER8_MAIN_L3
	0x4013 E040		TIMER8_CORTEX-A15
	0x3 E040		TIMER8_DSP
	0x4803 E040		TIMER9_L4
	0x4808 8040		TIMER11_L4
Description	This register holds the timer load value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOAD_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	LOAD_VALUE	Timer counter value loaded on overflow in autoreload mode or on TTGR write access. LOAD_VALUE must be different than the timer overflow value (0xFFFF FFFF).	RW	0x0000 0000

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Table 22-45. Register Call Summary for Register TLDR

General-Purpose Timers

- Timer Mode Functionality: [0] [1] [2]
- 1-ms Tick Generation (Only TIMER1, TIMER2, and TIMER10): [3] [4] [5] [6] [7] [8] [9] [10] [11] [12]
- Prescaler Functionality: [13] [14]
- Pulse-Width Modulation: [15] [16] [17]
- Timer Counting Rate: [18] [19] [20] [21] [22]
- Accessing GP Timer Registers: [23]
- Writing to Timer Registers: [24]
- Write Posting Synchronization Mode: [25]
- Posted Mode Selection: [26]
- Main Sequence – GP Timer Mode Configuration: [27]
- Main Sequence – GP Timer PWM Mode Configuration: [28]
- GP Timer Register Summary: [29] [30] [31] [32] [33] [34] [35]
- GP Timer Register Description: [36] [37]

Table 22-46. TTGR

Address Offset	0x0000 0044		
Physical Address	0x4AE1 8044	**Instance**	TIMER1_L4
	0x4803 2044		TIMER2_L4
	0x4808 6044		TIMER10_L4
	0x4803 4044		TIMER3_L4
	0x4803 6044		TIMER4_L4
	0x4903 8044		TIMER5_MAIN_L3
	0x4013 8044		TIMER5_CORTEX-A15
	0x3 8044		TIMER5_DSP
	0x4903 A044		TIMER6_MAIN_L3
	0x4013 A044		TIMER6_CORTEX-A15
	0x3 A044		TIMER6_DSP
	0x4903 C044		TIMER7_MAIN_L3
	0x4013 C044		TIMER7_CORTEX-A15
	0x3 C044		TIMER7_DSP
	0x4903 E044		TIMER8_MAIN_L3
	0x4013 E044		TIMER8_CORTEX-A15
	0x3 E044		TIMER8_DSP
	0x4803 E044		TIMER9_L4
	0x4808 8044		TIMER11_L4
Description	The read value of this register is always 0xFFFF FFFF.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTGR_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	TTGR_VALUE	Writing to the TTGR register causes the TCRR to be loaded from TLDR and the prescaler counter to be cleared. Reload is done regardless of the AR field value of the TCLR register.	RW Rreturns 1s	0xFFFF FFFF

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Table 22-47. Register Call Summary for Register TTGR

General-Purpose Timers

- Timer Mode Functionality: [0] [1]
- Prescaler Functionality: [2]
- Accessing GP Timer Registers: [3]
- Writing to Timer Registers: [4]
- Write Posting Synchronization Mode: [5] [6]
- Posted Mode Selection: [7]
- GP Timer Register Summary: [8] [9] [10] [11] [12] [13] [14]
- GP Timer Register Description: [15] [16] [17]

Table 22-48. TWPS

Address Offset	0x0000 0048		
Physical Address	0x4AE1 8048	**Instance**	TIMER1_L4
	0x4803 2048		TIMER2_L4
	0x4808 6048		TIMER10_L4
	0x4803 4048		TIMER3_L4
	0x4803 6048		TIMER4_L4
	0x4903 8048		TIMER5_MAIN_L3
	0x4013 8048		TIMER5_CORTEX-A15
	0x3 8048		TIMER5_DSP
	0x4903 A048		TIMER6_MAIN_L3
	0x4013 A048		TIMER6_CORTEX-A15
	0x3 A048		TIMER6_DSP
	0x4903 C048		TIMER7_MAIN_L3
	0x4013 C048		TIMER7_CORTEX-A15
	0x3 C048		TIMER7_DSP
	0x4903 E048		TIMER8_MAIN_L3
	0x4013 E048		TIMER8_CORTEX-A15
	0x3 E048		TIMER8_DSP
	0x4803 E048		TIMER9_L4
	0x4808 8048		TIMER11_L4
Description	This register contains the write posting bits for all writable functional registers.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						W_PEND_TOWR	W_PEND_TOCR	W_PEND_TCVR	W_PEND_TNIR	W_PEND_TPIR	W_PEND_TMAR	W_PEND_TTGR	W_PEND_TLDR	W_PEND_TCRR	W_PEND_TCLR

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x0000000
9	W_PEND_TOWR	Write pending for the TOWR register	R	0
		Read 1: Write pending		
		Read 0: No write pending		
8	W_PEND_TOCR	Write pending for the TOCR register	R	0
		Read 1: Write pending		
		Read 0: No write pending		
7	W_PEND_TCVR	Write pending for the TCVR register	R	0
		Read 1: Write pending		
		Read 0: No write pending		

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Bits	Field Name	Description	Type	Reset
6	W_PEND_TNIR	Write pending for the TNIR register	R	0
		Read 1: Negative increment register write pending		
		Read 0: No negative increment register write pending		
5	W_PEND_TPIR	Write pending for the TPIR register	R	0
		Read 1: Positive increment register write pending		
		Read 0: No positive increment register write pending		
4	W_PEND_TMAR	When equal to 1, a write is pending to the TMAR register.	R	0
3	W_PEND_TTGR	When equal to 1, a write is pending to the TTGR register.	R	0
2	W_PEND_TLDR	When equal to 1, a write is pending to the TLDR register.	R	0
1	W_PEND_TCRR	When equal to 1, a write is pending to the TCRR register.	R	0
0	W_PEND_TCLR	When equal to 1, a write is pending to the TCLR register.	R	0

Table 22-49. Register Call Summary for Register TWPS

General-Purpose Timers

- Accessing GP Timer Registers: [0]
- Write Posting Synchronization Mode: [1]
- Posted Mode Selection: [2]
- GP Timer Register Summary: [3] [4] [5] [6] [7] [8] [9]

Table 22-50. TMAR

Address Offset	0x0000 004C		
Physical Address	0x4AE1 804C	**Instance**	TIMER1_L4
	0x4803 204C		TIMER2_L4
	0x4808 604C		TIMER10_L4
	0x4803 404C		TIMER3_L4
	0x4803 604C		TIMER4_L4
	0x4903 804C		TIMER5_MAIN_L3
	0x4013 804C		TIMER5_CORTEX-A15
	0x3 804C		TIMER5_DSP
	0x4903 A04C		TIMER6_MAIN_L3
	0x4013 A04C		TIMER6_CORTEX-A15
	0x3 A04C		TIMER6_DSP
	0x4903 C04C		TIMER7_MAIN_L3
	0x4013 C04C		TIMER7_CORTEX-A15
	0x3 C04C		TIMER7_DSP
	0x4903 E04C		TIMER8_MAIN_L3
	0x4013 E04C		TIMER8_CORTEX-A15
	0x3 E04C		TIMER8_DSP
	0x4803 E04C		TIMER9_L4
	0x4808 804C		TIMER11_L4
Description	The compare logic consists of a 32-bit-wide, read/write data TMAR register and logic to compare counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPARE_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	COMPARE_VALUE	Value to be compared to the timer counter	RW	0x0000 0000

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Table 22-51. Register Call Summary for Register TMAR

General-Purpose Timers

- Wake-Up Capability: [0]
- Compare Mode Functionality: [1] [2] [3] [4]
- Pulse-Width Modulation: [5] [6] [7]
- Accessing GP Timer Registers: [8]
- Writing to Timer Registers: [9]
- Write Posting Synchronization Mode: [10]
- Posted Mode Selection: [11]
- Main Sequence – GP Timer Compare Mode Configuration: [12]
- Main Sequence – GP Timer PWM Mode Configuration: [13]
- GP Timer Register Summary: [14] [15] [16] [17] [18] [19] [20]
- GP Timer Register Description: [21] [22]

Table 22-52. TCAR1

Address Offset	0x0000 0050		
Physical Address	0x4AE1 8050	**Instance**	TIMER1_L4
	0x4803 2050		TIMER2_L4
	0x4808 6050		TIMER10_L4
	0x4803 4050		TIMER3_L4
	0x4803 6050		TIMER4_L4
	0x4903 8050		TIMER5_MAIN_L3
	0x4013 8050		TIMER5_CORTEX-A15
	0x3 8050		TIMER5_DSP
	0x4903 A050		TIMER6_MAIN_L3
	0x4013 A050		TIMER6_CORTEX-A15
	0x3 A050		TIMER6_DSP
	0x4903 C050		TIMER7_MAIN_L3
	0x4013 C050		TIMER7_CORTEX-A15
	0x3 C050		TIMER7_DSP
	0x4903 E050		TIMER8_MAIN_L3
	0x4013 E050		TIMER8_CORTEX-A15
	0x3 E050		TIMER8_DSP
	0x4803 E050		TIMER9_L4
	0x4808 8050		TIMER11_L4
Description	This register holds the first captured value of the counter register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_VALUE1																															

Bits	Field Name	Description	Type	Reset
31:0	CAPTURE_VALUE1	First timer counter value captured on an external event trigger	R	0x0000 0000

Table 22-53. Register Call Summary for Register TCAR1

General-Purpose Timers

- Capture Mode Functionality: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- Reading From Timer Counter Registers: [9]
- Read Posted: [10]
- Read Non-posted: [11]
- Posted Mode Selection: [12]
- Subsequence – Detect Event: [13]
- GP Timer Register Summary: [14] [15] [16] [17] [18] [19] [20]
- GP Timer Register Description: [21]

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Table 22-54. TSICR

Address Offset	0x0000 0054		
Physical Address	0x4AE1 8054	**Instance**	TIMER1_L4
	0x4803 2054		TIMER2_L4
	0x4808 6054		TIMER10_L4
	0x4803 4054		TIMER3_L4
	0x4803 6054		TIMER4_L4
	0x4903 8054		TIMER5_MAIN_L3
	0x4013 8054		TIMER5_CORTEX-A15
	0x3 8054		TIMER5_DSP
	0x4903 A054		TIMER6_MAIN_L3
	0x4013 A054		TIMER6_CORTEX-A15
	0x3 A054		TIMER6_DSP
	0x4903 C054		TIMER7_MAIN_L3
	0x4013 C054		TIMER7_CORTEX-A15
	0x3 C054		TIMER7_DSP
	0x4903 E054		TIMER8_MAIN_L3
	0x4013 E054		TIMER8_CORTEX-A15
	0x3 E054		TIMER8_DSP
	0x4803 E054		TIMER9_L4
	0x4808 8054		TIMER11_L4
Description	Timer synchronous interface control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												READ_MODE	POSTED	SFT	RESERVED

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000 0000
3	READ_MODE	Select posted/non-posted mode for read operation: 0x0: When the module is configured in non-posted mode(POSTED = '0'), the read operation is executed as read posted. 0x1: When the module is configured in non-posted mode(POSTED = '0'), the read operation is executed as read non-posted. NOTE: When the module is configured in posted mode (POSTED = '1'), this bit is not used.	RW	-
2	POSTED	Posted mode selection 0x0: Posted mode inactive: Delay the command accept output signal. 0x1: Posted mode active	RW	-
1	SFT	This bit resets all the functional part of the module. 0x0: Software reset is disabled. 0x1: Software reset is enabled.	RW	0
0	RESERVED	Reserved	R	0

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Table 22-55. Register Call Summary for Register TSICR

General-Purpose Timers

- Software Reset: [0] [1]
- Accessing GP Timer Registers: [2] [3]
- Writing to Timer Registers: [4]
- Write Posting Synchronization Mode: [5]
- Write Nonposting Synchronization Mode: [6]
- Read Posted: [7] [8]
- Read Non-posted: [9] [10]
- Posted Mode Selection: [11] [12] [13] [14] [15] [16] [17] [18] [19]
- Main Sequence – GP Timer Module Global Initialization: [20]
- GP Timer Register Summary: [21] [22] [23] [24] [25] [26] [27]

Table 22-56. TCAR2

Address Offset	0x0000 0058		
Physical Address	0x4AE1 8058	**Instance**	TIMER1_L4
	0x4803 2058		TIMER2_L4
	0x4808 6058		TIMER10_L4
	0x4803 4058		TIMER3_L4
	0x4803 6058		TIMER4_L4
	0x4903 8058		TIMER5_MAIN_L3
	0x4013 8058		TIMER5_CORTEX-A15
	0x3 8058		TIMER5_DSP
	0x4903 A058		TIMER6_MAIN_L3
	0x4013 A058		TIMER6_CORTEX-A15
	0x3 A058		TIMER6_DSP
	0x4903 C058		TIMER7_MAIN_L3
	0x4013 C058		TIMER7_CORTEX-A15
	0x3 C058		TIMER7_DSP
	0x4903 E058		TIMER8_MAIN_L3
	0x4013 E058		TIMER8_CORTEX-A15
	0x3 E058		TIMER8_DSP
	0x4803 E058		TIMER9_L4
	0x4808 8058		TIMER11_L4
Description	This register holds the second captured value of the counter register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE_VALUE2																															

Bits	Field Name	Description	Type	Reset
31:0	CAPTURE_VALUE2	Second timer counter value captured on an external event trigger	R	0x0000 0000

Table 22-57. Register Call Summary for Register TCAR2

General-Purpose Timers

- Capture Mode Functionality: [0] [1] [2] [3] [4] [5]
- Reading From Timer Counter Registers: [6]
- Read Posted: [7]
- Read Non-posted: [8]
- Posted Mode Selection: [9]
- Subsequence – Detect Event: [10]
- GP Timer Register Summary: [11] [12] [13] [14] [15] [16] [17]
- GP Timer Register Description: [18]

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22.2.6.2.3 TIMER1, TIMER2 , and TIMER10 Register Description

Table 22-58. TPIR

Address Offset	0x0000 005C		
Physical Address	0x4AE1 805C 0x4803 205C 0x4808 605C	**Instance**	TIMER1_L4 TIMER2_L4 TIMER10_L4
Description	This register is used for 1-ms tick generation. The TPIR register holds the value of the positive increment. The value of this register is added to the value of TCVR to determine whether next value loaded in TCRR is the subperiod value or the overperiod value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POSITIVE_INC_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	POSITIVE_INC_VALUE	Value of the positive increment	RW	0x0000 0000

Table 22-59. Register Call Summary for Register TPIR

General-Purpose Timers

- 1-ms Tick Generation (Only TIMER1, TIMER2, and TIMER10): [0] [1] [2] [3] [4] [5]
- Accessing GP Timer Registers: [6]
- Writing to Timer Registers: [7]
- Write Posting Synchronization Mode: [8] [9]
- Posted Mode Selection: [10]
- GP Timer Register Summary: [11]
- GP Timer Register Description: [12]
- TIMER1, TIMER2 , and TIMER10 Register Description: [13]

Table 22-60. TNIR

Address Offset	0x0000 0060		
Physical Address	0x4AE1 8060 0x4803 2060 0x4808 6060	**Instance**	TIMER1_L4 TIMER2_L4 TIMER10_L4
Description	This register is used for 1-ms tick generation. The TNIR register holds the value of the negative increment. The value of this register is added to the value of the TCVR to determine whether next value loaded in TCRR is the subperiod value or the overperiod value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEGATIVE_INV_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	NEGATIVE_INV_VALUE	Value of the negative increment	RW	0x0000 0000

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Table 22-61. Register Call Summary for Register TNIR

General-Purpose Timers

- 1-ms Tick Generation (Only TIMER1, TIMER2, and TIMER10): [0] [1] [2] [3] [4] [5]
- Accessing GP Timer Registers: [6]
- Writing to Timer Registers: [7]
- Write Posting Synchronization Mode: [8] [9]
- Posted Mode Selection: [10]
- GP Timer Register Summary: [11]
- GP Timer Register Description: [12]
- TIMER1, TIMER2 , and TIMER10 Register Description: [13]

Table 22-62. TCVR

Address Offset	0x0000 0064		
Physical Address	0x4AE1 8064 0x4803 2064 0x4808 6064	**Instance**	TIMER1_L4 TIMER2_L4 TIMER10_L4
Description	This register is used for 1-ms tick generation. The TCVR register determines whether next value loaded in TCRR is the subperiod value or the overperiod value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	COUNTER_VALUE	Value of CVR counter	RW	0x0000 0000

Table 22-63. Register Call Summary for Register TCVR

General-Purpose Timers

- 1-ms Tick Generation (Only TIMER1, TIMER2, and TIMER10): [0] [1]
- Accessing GP Timer Registers: [2]
- Writing to Timer Registers: [3]
- Write Posting Synchronization Mode: [4] [5] [6] [7]
- Read Posted: [8]
- Read Non-posted: [9]
- Posted Mode Selection: [10] [11]
- GP Timer Register Summary: [12]
- GP Timer Register Description: [13]
- TIMER1, TIMER2 , and TIMER10 Register Description: [14] [15] [16]

Table 22-64. TOCR

Address Offset	0x0000 0068		
Physical Address	0x4AE1 8068 0x4803 2068 0x4808 6068	**Instance**	TIMER1_L4 TIMER2_L4 TIMER10_L4
Description	This register is used to mask the tick interrupt for a selected number of ticks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OVF_COUNTER_VALUE																							

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Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reads return 0.	R	0x00
23:0	OVF_COUNTER_VALUE	Number of overflow events	RW	0x000000

Table 22-65. Register Call Summary for Register TOCR

General-Purpose Timers

- 1-ms Tick Generation (Only TIMER1, TIMER2, and TIMER10): [0] [1] [2] [3] [4]
- Accessing GP Timer Registers: [5]
- Writing to Timer Registers: [6]
- Write Posting Synchronization Mode: [7]
- Posted Mode Selection: [8]
- GP Timer Register Summary: [9]
- GP Timer Register Description: [10]

Table 22-66. TOWR

Address Offset	0x0000 006C		
Physical Address	0x4AE1 806C 0x4803 206C 0x4808 606C	**Instance**	TIMER1_L4 TIMER2_L4 TIMER10_L4
Description	This register holds the number of masked overflow interrupts.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OVF_WRAPPING_VALUE																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reads return 0.	R	0x00
23:0	OVF_WRAPPING_VALUE	Number of masked interrupts	RW	0x000000

Table 22-67. Register Call Summary for Register TOWR

General-Purpose Timers

- 1-ms Tick Generation (Only TIMER1, TIMER2, and TIMER10): [0] [1] [2] [3] [4] [5] [6]
- Accessing GP Timer Registers: [7]
- Writing to Timer Registers: [8]
- Write Posting Synchronization Mode: [9]
- Read Posted: [10]
- Read Non-posted: [11]
- Posted Mode Selection: [12] [13]
- GP Timer Register Summary: [14]
- GP Timer Register Description: [15]

Table 22-68. IRQSTATUS_SET

Address Offset	0x0000 002C		
Physical Address	0x4AE1 802C 0x4803 202C 0x4808 602C	**Instance**	TIMER1_L4 TIMER2_L4 TIMER10_L4
Description	Component interrupt-request enable. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_EN_FLAG	OVF_EN_FLAG	MAT_EN_FLAG

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_EN_FLAG	IRQ enable for compare Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled Write 1: Set IRQ enable.	RW	0
1	OVF_EN_FLAG	IRQ enable for overflow Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Set IRQ enable.	RW	0
0	MAT_EN_FLAG	IRQ enable for match Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Set IRQ enable.	RW	0

Table 22-69. Register Call Summary for Register IRQSTATUS_SET

General-Purpose Timers

- GP Timer Functional Description: [0]
- GP Timer Interrupts: [1]
- Timer Mode Functionality: [2]
- Capture Mode Functionality: [3]
- Compare Mode Functionality: [4]
- Accessing GP Timer Registers: [5] [6] [7]
- Writing to Timer Registers: [8]
- Posted Mode Selection: [9]
- Main Sequence – GP Timer Mode Configuration: [10]
- Main Sequence – GP Timer Compare Mode Configuration: [11]
- Main Sequence – GP Timer Capture Mode Configuration: [12]
- GP Timer Register Summary: [13]

Table 22-70. IRQSTATUS_CLR

Address Offset	0x0000 0030		
Physical Address	0x4AE1 8030 0x4803 2030 0x4808 6030	**Instance**	TIMER1_L4 TIMER2_L4 TIMER10_L4
Description	Component interrupt-request enable. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TCAR_EN_FLAG	OVF_EN_FLAG	MAT_EN_FLAG

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	TCAR_EN_FLAG	IRQ enable for compare Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Clear IRQ enable.	RW	0
1	OVF_EN_FLAG	IRQ enable for overflow Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Clear IRQ enable.	RW	0
0	MAT_EN_FLAG	IRQ enable for match Read 0: IRQ event is disabled. Write 0: No action Read 1: IRQ event is enabled. Write 1: Clear IRQ enable.	RW	0

Table 22-71. Register Call Summary for Register IRQSTATUS_CLR

General-Purpose Timers

- GP Timer Functional Description: [0]
- GP Timer Interrupts: [1]
- Accessing GP Timer Registers: [2] [3]
- Writing to Timer Registers: [4]
- GP Timer Register Summary: [5]

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22.3 Watchdog Timers

22.3.1 Watchdog Timers Overview

The device includes two instances of the 32-bit watchdog timer: WD_TIMER2 and WD_TIMER3. Figure 22-14 shows how each timer is connected in the device.

NOTE: WD_TIMERi (where i is the watchdog timer instance: i = 2 or 3) stands for the following:

- WD_TIMER2: Watchdog timer 2, also called the MPU watchdog timer
- WD_TIMER3: IVA3 (IVA + DSP) watchdog, clocked by the SYS_32K clock, generates an MPU interrupt on overflow, which can be used by application software to trigger a reset condition to IVA3 (IVA + DSP). Embedded in ABE.

Each watchdog timer is an upward counter capable of generating a pulse on the reset pin and an interrupt to the device system modules following an overflow condition. The WD_TIMER2 timer serves resets to the PRCM module (its interrupt outputs are unused), and the WD_TIMER3 timer serves watchdog interrupts to the MPU (its reset outputs are unused).

The watchdog timers can be accessed, loaded, and cleared by registers through the L4 interface. The watchdog timers have the 32-kHz clock for their timer clock input.

The MPU watchdog timer directly generates a warm reset condition on overflow. WD_TIMER3 generates an MPU interrupt condition on overflow, which can be used by the application software through the PRCM module to indirectly trigger a reset condition (that is, to the IVA subsystem).

The MPU watchdog timer connects to a single target agent port on the L4 interconnect.

Figure 22-14. Watchdog Timers Block Diagram

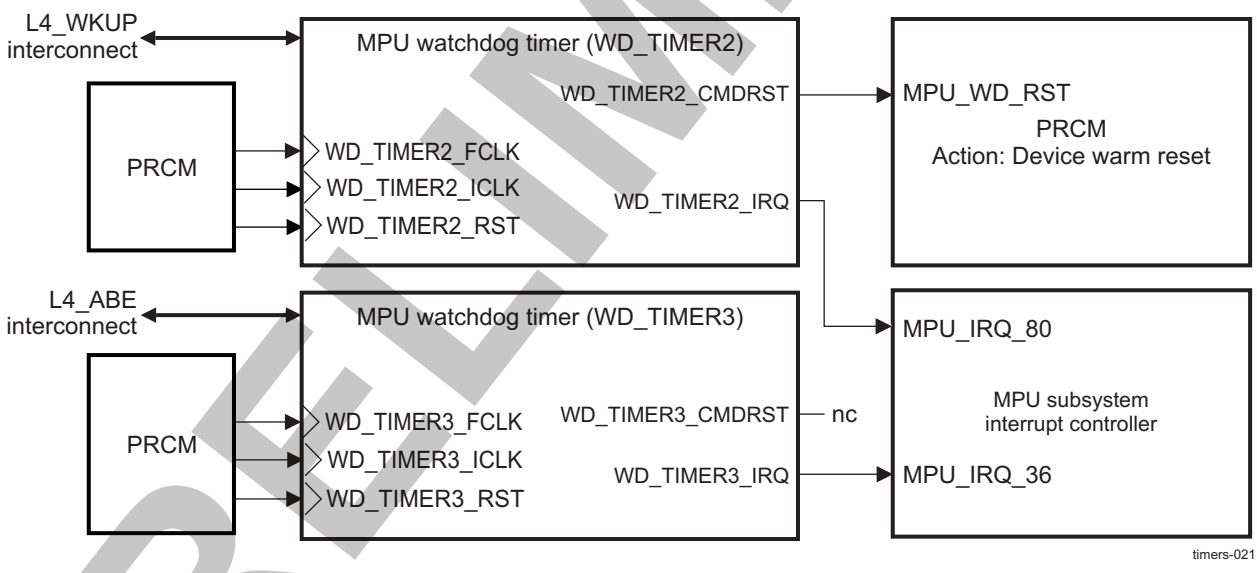

Table 22-72 lists the default state of the watchdog timers in the device.

Table 22-72. Watchdog Timers Default State

Timer	Default State	
WD_TIMER2	Enabled	Not running
WD_TIMER3	Enabled	Not running

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NOTE: The default state of the watchdog timers described in Table 22-72 is considered to be their state immediately after ROM code execution. For more information, see Section 28.1, *Initialization*.

22.3.1.1 Watchdog Timers Features

The main features of the watchdog timer controllers are:

- L4 slave interface support:
  - 32-bit data bus width
  - 32-/16-bit access supported
  - 8-bit access not supported
  - 11-bit address bus width
  - Burst mode not supported
  - Write nonposted mode supported
- Free-running 32-bit upward counter
- Programmable divider clock source (2^n where n = [0:7])
- On-the-fly read/write register (while counting)
- Subset programming model of the GP timer
- The watchdog timers are reset either on power on or after a warm reset before they start counting.
- Reset or interrupt actions when a timer overflow condition occurs
- The watchdog timer generates a reset or an interrupt in its hardware integration (WD_TIMER2 or WD_TIMER3).

22.3.2 Watchdog Timer Environment

The watchdog timers are accessible through the L4 interface.

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22.3.3 Watchdog Timer Integration

Figure 22-15 shows the integration of the watchdog timers in the device.

Figure 22-15. Watchdog Timers Integration

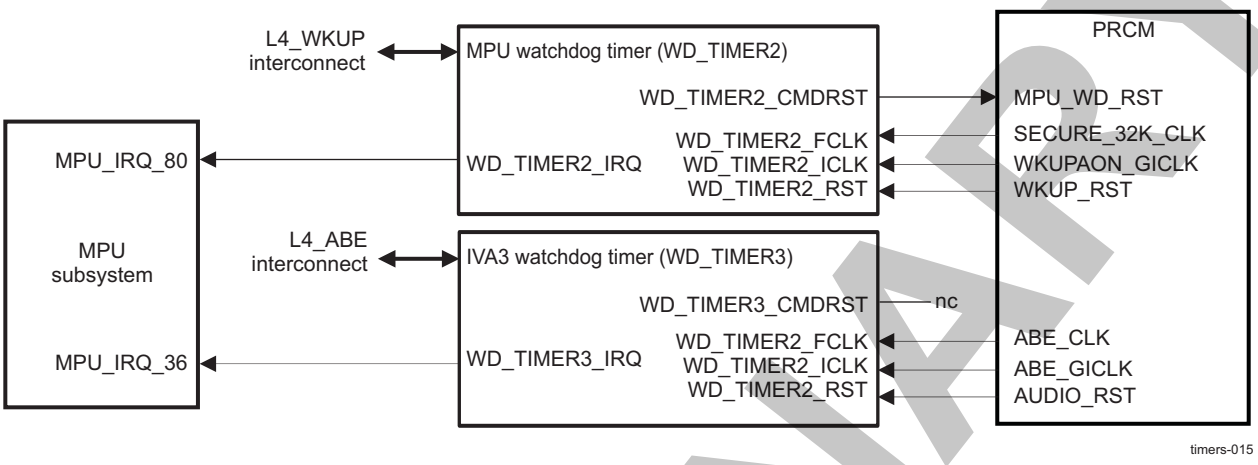

Table 22-73 through Table 22-75 summarize the integration of the module in the device.

Table 22-73. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
WD_TIMER2	PD_WKUP	Yes	L4_WKUP
WD_TIMER3	PD_AUDIO	Yes	L4_ABE

Table 22-74. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
WD_TIMER2	WD_TIMER2_FCLK	WKUPAON_32K_GFCLK	PRCM	WD_TIMER2 functional clock
WD_TIMER2	WD_TIMER2_ICLK	WKUPAON_GICLK	PRCM	WD_TIMER2 interface clock
WD_TIMER3	WD_TIMER3_FCLK	ABE_32K_CLK	PRCM	WD_TIMER3 functional clock
WD_TIMER3	WD_TIMER3_ICLK	ABE_GICLK	PRCM	WD_TIMER3 interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
WD_TIMER2	WD_TIMER2_RST	WKUPAON_RST	PRM	Reset to WD_TIMER2
WD_TIMER2	MPU_WD_TIMER2_RST	WD_TIMER2_CMDRST	WD_TIMER2	Reset to MPU
WD_TIMER3	WD_TIMER3_RST	ABE_RST	PRM	Reset to WD_TIMER3

NOTE: WD_TIMER2 is reset on power on or after a warm reset before it starts counting.

WD_TIMER3 is reset on power on or after a warm reset, and then it does not start counting.

Table 22-75. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**

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Table 22-75. Hardware Requests (continued)

WD_TIMER2	WD_TIMER2_IRQ	MPU_IRQ_80	MPU	WD_TIMER2 interrupt to MPU
WD_TIMER3	WD_TIMER3_IRQ	MPU_IRQ_36	MPU	ABE watchdog overflow
No DMA Requests				

NOTE: For the description of the interrupt source, see Section 22.3.4.2, *Interrupts*.

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22.3.4 Watchdog Timers Functional Description

22.3.4.1 Power Management

There are two clock domains in the watchdog timers:

- Functional clock domain: WD_TIMERi_FCLK is the watchdog timer functional clock. It is used to clock the watchdog timer internal logic.
- Interface clock domain: WD_TIMERi_ICLK is the watchdog timer interface clock. It is used to synchronize the watchdog timer L4 port to the L4 interconnect. All accesses from the interconnect are synchronous to WD_TIMERi_ICLK.

Table 22-74 lists the source clocks for each watchdog timer in the device. For more information about clock control and domains, see Section 3.6, *Clock Management Functional Description,* in Section 3.1.1, *Power, Reset, and Clock Management*.

From a global system power-management perspective, when one or both of the watchdog timer clocks is no longer required, the watchdog timers can be deactivated at the PRCM module level in the corresponding registers.

At the PRCM module level, when the conditions to shut off the PRCM module functional or interface output clocks are met (for more information, seeSection 3.1.1.1.4, *Clock Domain-Level Clock Management*), the PRCM module automatically launches a hardware handshake protocol to ensure the watchdog timer is ready to have its clocks switched off. Namely, the PRCM module asserts an IDLE request to the watchdog timer.

Although this handshake is a hardware function and out of software control, the way on which the watchdog timer acknowledges the PRCM IDLE request is configurable through the WDSC[4:3] IDLEMODE bit field. Table 22-76 lists the settings and related acknowledgment modes of the IDLEMODE bit field.

Table 22-76. IDLEMODE Settings

IDLEMODE Value	Selected Mode	Description
00	Force-idle	The watchdog timer unconditionally acknowledges the IDLE request from the PRCM module, regardless of its internal operations. This mode must be used carefully, because it does not prevent loss of data when the clock is switched off.
01	No-idle	The watchdog timer never acknowledges an IDLE request from the PRCM module. This mode is safe from a module point of view, because it ensures that the clocks remain active. It is not efficient from a power-saving perspective, however, because it does not allow the PRCM module output clock to be shut off and thus the power domain to be set to a lower power state.
10	Smart-idle	The watchdog timer acknowledges the IDLE request, basing its decision on its internal activity. The acknowledge signal is asserted only when all pending transactions and IRQ requests are treated. This is the best approach for efficient system power management.
11	Smart-idle wakeup-capable mode	The watchdog timer acknowledges the IDLE request, basing its decision on its internal activity. The timer generates (IRQ-request-related) wake-up events when in IDLE state if the WIRQWAKEEN[1:0] bit field is set to 1.

22.3.4.1.1 Wake-Up Capability

If the WDSC[4:3] IDLEMODE bit field sets smart-idle wakeup-capable mode (= 0 × 3), the timer evaluates its internal capability to have the interface clock switched off. When there is no more internal activity (no pending interrupt sources: match, overflow, or timer capture events), the idle acknowledge signal is asserted and the timer enters into sleep mode, ready to issue a wake-up request. This wake-up request is sent only if the WIRQWAKEEN[0] OVF_WK_ENA and/or the WIRQWAKEEN[1] DLY_WK_ENA bits enable the overflow and/or the delay wake-up capability.

22.3.4.2 Interrupts

Table 22-77 list the event flags, and their masks that cause module interrupts.

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Table 22-77. Watchdog Timer Events

Event Flag	Event Mask	Mapping	Comments
WIRQSTAT[0] EVENT_OVF	WIRQENSET/WIRQENCLR[0] OVF_IT_ENA	WD_TIMERi_IRQ	Watchdog timer overflow
WIRQSTAT[1] EVENT_DLY	WIRQENSET/WIRQENCLR[1] DLY_IT_ENA	WD_TIMERi_IRQ	Watchdog delay value reached

22.3.4.3 General Watchdog Timer Operation

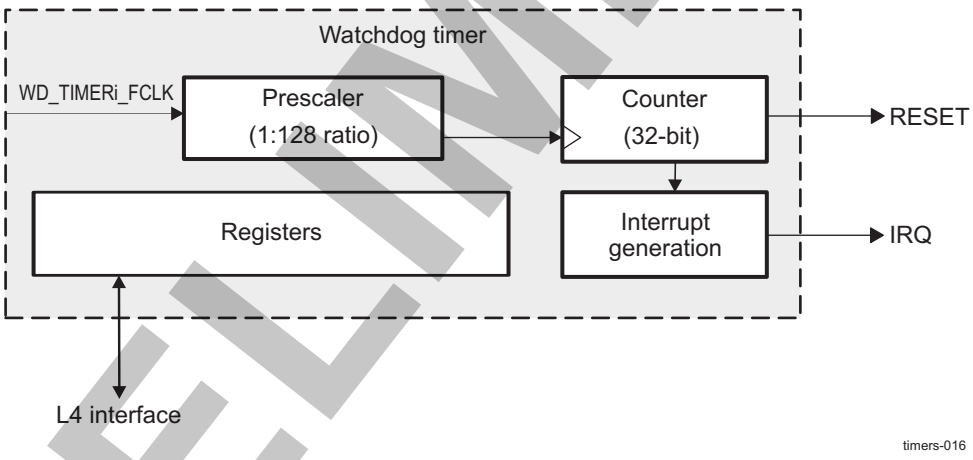
The watchdog timers are based on an upward 32-bit counter coupled with a prescaler. The counter overflow is signaled through two independent signals: a simple reset signal and an interrupt signal, both active low. The use of these signals depends on whether they are connected or not. For this information, see Figure 22-14. The interrupt generation mechanism is controlled through the WIRQENSET/WIRQENCLR and WIRQSTAT registers.

The prescaler ratio can be set from 1 to 128 by accessing the WCLR[4:2] PTV bit field and the WCLR[5] PRE bit of the watchdog control register (WCLR).

The current timer value can be accessed on-the-fly by reading the watchdog timer counter register (WCRR), modified by accessing the watchdog timer load register (WLDR) (no on-the-fly update), or reloaded by following a specific reload sequence on the watchdog timer trigger register (WTGR). A start/stop sequence applied to the watchdog timer start/stop register (WSPR) can start and stop the watchdog timers.

Figure 22-16 is a functional block diagram of the watchdog timer.

Figure 22-16. 32-Bit Watchdog Timer Functional Block Diagram



22.3.4.4 Reset Context

The watchdog timers are enabled after reset. Table 22-78 lists the default reset values of the two watchdog timer load registers (WLDR) and prescaler ratios (the WCLR[4:2] PTV bit field). To get these values, software must read the corresponding WCLR[4:2] PTV bit field and the 32-bit register to retrieve the static configuration of the module.

Table 22-78. Count and Prescaler Default Reset Values

Timer	WLDR Reset Value	PTV Reset Value
MPU watchdog timer (WD_TIMER2)	0xFFFB 0000	0
IVA3 (IVA + DSP) watchdog timer (WD_TIMER3)	0xFFFB 0000	0

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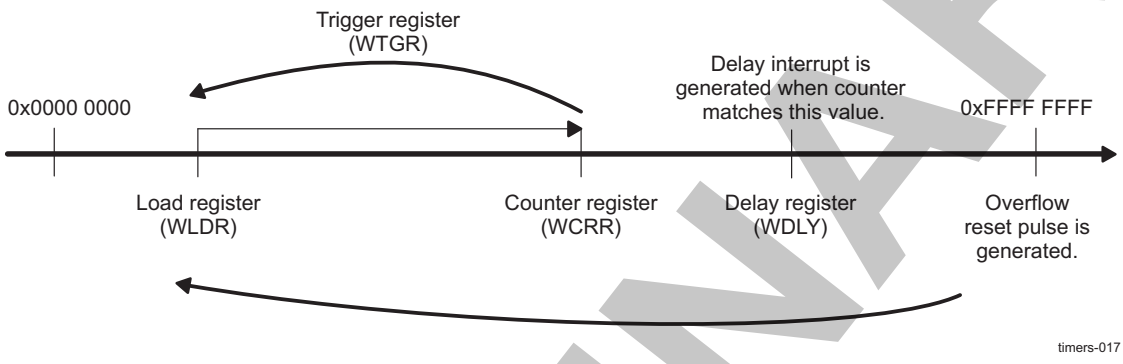
22.3.4.5 Overflow/Reset Generation

When the WCRR overflows, an active-low reset pulse is generated to the PRCM module. This pulse is one prescaled timer clock cycle wide and occurs at the same time as the timer counter overflow.

After reset generation, the counter is automatically reloaded with the value stored in the WLDR and the prescaler is reset (the prescaler ratio remains unchanged). When the reset pulse output is generated, the timer counter begins incrementing again.

Figure 22-17 shows a general functional view of the watchdog timers.

Figure 22-17. Watchdog Timers General Functional View



22.3.4.6 Prescaler Value/Timer Reset Frequency

Each watchdog timer is composed of a prescaler stage and a timer counter.

The timer rate is defined by the following values:

- Value of the prescaler fields (the WCLR[5] PRE bit and the WCLR[4:2] PTV bit field)
- Value loaded into WLDR

The prescaler stage is clocked with the timer clock and acts as a clock divider for the timer counter stage. The ratio is managed by accessing the ratio definition field (the WCLR [4:2] PTV bit field) and is enabled with the WCLR[5] PRE bit.

Table 22-79 lists the prescaler clock ratio values.

Table 22-79. Prescaler Clock Ratio Values

WLCR[5] PRE	WCLR[4:2] PTV	Clock Divider (PS)
0	X	1
1	0	1
1	1	2
1	2	4
1	3	8
1	4	16
1	5	32
1	6	64
1	7	128

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Thus the watchdog timer overflow rate is expressed as:

OVF_Rate = (0xFFFF FFFF – WLDR + 1) × (timer clock period) × PS

where wd-functional clock period = 1 / (timer clock frequency) and PS = $2^{(PTV)}$

CAUTION

Internal resynchronization causes some latency in any software write to WSPR before WSPR is updated with the programmed value:

1.5 × functional clock cycles ≤ write_WD_TIMER_WSPR_latency ≤ 2.5 × functional clock cycles

Remember to consider this latency whenever the watchdog timer must be started or stopped.

For example, for a timer clock input of 32 kHz with a prescaler ratio value of 0x1 (clock divided by 2) and WCLR[5] PRE = 1 (clock divider enabled), the reset period is as listed in Table 22-80.

Table 22-80. Reset Period Examples

WLDR Value	Reset Period
0x0000 0000	74 h 56 min
0xFFFF 0000	4 s
0xFFFF FFF0	1 ms
0xFFFF FFFF	62.5 µs

CAUTION

- Ensure that the reloaded value allows the correct operation of the application. When a watchdog timer is enabled, software must periodically trigger a reload before the counter overflows. Hence, the value of the WLDR[31:0] bit field must be chosen according to the ongoing activity preceding the watchdog reload.
- Due to design reasons, WLDR[31:0] = 0xFFFF FFFF is a special case, although such value of WLDR is meaningless. When WLDR is programmed with the overflow value, a triggering event generates a reset/interrupt one functional clock cycle later, even if the watchdog timer is stopped.

Table 22-81 lists the default reset periods for the watchdog timers.

Table 22-81. Default Watchdog Timer Reset Periods

Watchdog Timers	Clock Source	Default Reset Period
MPU/ABE	32 kHz	10 s

22.3.4.7 Triggering a Timer Reload

To reload the timer counter and reset the prescaler before reaching overflow, a reload command is executed by accessing the WTGR using a specific reload sequence.

The specific reload sequence is performed whenever the written value on the WTGR differs from its previous value. In this case, reload is executed in the same way as an overflow autoreload, but without the generation of a reset pulse.

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The timer counter is loaded with the value of the watchdog timer load register (the WLDR[31:0] TIMER_LOAD bit field), and the prescaler is reset.

22.3.4.8 Start/Stop Sequence for Watchdog Timers (Using the WSPR Register)

To start and stop a watchdog timer, access must be made through the WSPR using a specific sequence.

To disable the timer, follow this sequence:

1. Write 0xXXXX AAAA in the WSPR.
2. Write 0xXXXX 5555 in the WSPR.

To enable the timer, follow this sequence:

1. Write 0xXXXX BBBB in the WSPR.
2. Write 0xXXXX 4444 in the WSPR.

All other write sequences on the WSPR have no effect on the start/stop feature of the module.

22.3.4.9 Modifying Timer Count/Load Values and Prescaler Setting

To modify the timer counter value (the WCRR), the prescaler ratio (the WCLR[4:2] PTV bit field), delay configuration value (the WDLY[31:0] DLY_VALUE bit field), or the load value (the WLDR[31:0] TIMER_LOAD bit field), the watchdog timer must be disabled by using the start/stop sequence (the WSPR).

After a write access, the load register value and prescaler ratio registers are updated immediately, but new values are considered only after the next consecutive counter overflow or after a new trigger command (the WTGR).

22.3.4.10 Watchdog Counter Register Access Restriction (WCRR)

A 32-bit shadow register is implemented to read a coherent value of the WCRR because the WCRR is directly related to the timer counter value and is updated on the timer clock (WD_TIMER_FCLK). The shadow register is updated by a 16-bit LSB read command.

NOTE: Although the L4 clock (WD_TIMER_ICLK) is completely asynchronous with the timer clock (WD_TIMER_FCLK), some synchronization is performed to ensure that the value of the WCRR is not read while it is being incremented.

When 32-bit read access is performed, the shadow register is not updated. Read access is performed directly from the accessed register.

To ensure that a coherent value is read inside the WCRR, the first read access is to the lower 16 bits (offset = 0x08), followed by read access to the upper 16 bits (offset = 0x0A).

22.3.4.11 Watchdog Timer Interrupt Generation

When an interrupt source occurs, the interrupt status bit (the WISR[0] OVF_IT_FLAG or WISR[1] DLY_IT_FLAG bit) is set to 1. The output interrupt line (WD_TIMERi_IRQ) is asserted (active low) when status (the EVENT_xxx bit) and enable (the xxx_IT_ENA bit) flags are set to 1; the order is not relevant. Writing 1 to the enable bit (the status is already set at 1) also triggers the interrupt in the normal order (enable first, status next). The pending interrupt event is cleared when the set status bit is overwritten by a value of 1 by a write command in the WISR. Reading the WISR and writing the value back allows a fast interrupt acknowledge process.

The watchdog timer issues an overflow interrupt if this interrupt is enabled in the watchdog interrupt-enable register (WIER[0] OVF_IT_ENA = 1). When the overflow occurs, the interrupt status bit (the WISR[0] OVF_IT_FLAG bit) is set to 1. The output interrupt line (WD_TIMER_IRQ) is asserted (active low) when status (OVF_IT_FLAG) and enable (OVF_IT_ENA) flags are set to 1; the order is not relevant. This interrupt can be disabled by setting the WIER [0] OVF_IT_ENA bit to 1.

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The watchdog can issue the delay interrupt if this interrupt is enabled in the interrupt-enable register (WIER[1] DLY_IT_ENA = 1). When the counter is running and the counter value matches the value stored in the delay configuration register (WDLY), the corresponding interrupt status bit is set in the watchdog status register (WISR) and the output interrupt line is asserted (active low) when the flag (DLY_IT_FLAG) and enable (DLY_IT_ENA) bits are set to 1 in the WISR and WIER registers, respectively; the order (normally enable, then flag) is not relevant. This interrupt can be disabled by setting the WIER[1] DLY_IT_ENA bit to 1.

NOTE: Writing 0 to the WISR[0] OVF_IT_FLAG or WISR[1] DLY_IT_FLAG bit has no effect.

The two clock domains are resynchronized because the interrupt event is generated on the functional clock domain (WD_TIMERi_FCLK) during the updating of the interrupt status register.

The WDLY register is used to specify the value of the delay configuration register. The delay time to interrupt is the difference between the reload value stored in the counter load register (WLDR) and the programmed value in this register (WDLY).

Use the following formula to estimate the delay time:

Delay time period = (WDLY – WLDR + 1) × Timer clock period × Clock divider

Where:

- Timer clock period = 1 / (Timer clock frequency)
- Clock divider = 2PTV

If the counter value (WCRR) reaches the programmed value (WDLY), the status bit (EVENT_DLY) is set in the interrupt status register (WIRQSTAT), and an interrupt occurs if the corresponding enable bit is set in the interrupt enable register (WIRQENSET).

CAUTION

If the reload event occurs (after a triggering sequence or after a reset sequence) before reaching the programmed value (the WDLY[31:0] WDLY_VALUE bit field), no interrupt is generated.

Also, no interrupt is generated if the value programmed in the WDLY register is less than the value stored in the WLDR.

22.3.4.12 Watchdog Timers Under Emulation

During emulation mode, the watchdog timer can or cannot continue to run, according to the value of the WDSC[5] EMUFREE bit of the system configuration register (WDSC).

- When EMUFREE is 1, watchdog timer execution is not stopped and a reset pulse is still generated when overflow is reached.
- When EMUFREE is 0, the counters (prescaler/timer) are frozen and incrementation restarts after exiting emulation mode.

22.3.4.13 Accessing Watchdog Timer Registers

Posted/nonposted selection applies only to functional registers that require synchronization on/from the timer functional clock domain (WD_TIMERi_FCLK). For write/read operation, the following registers are affected:

- WCLR
- WCRR
- WLDR
- WTGR
- WDLY
- WSPR

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The timer interface clock domain synchronous registers are not affected by the posted/nonposted selection; the write/read operation is effective and acknowledged (command accepted) after one WD_TIMER_ICLK cycle from the command assertion. The timer interface clock domain synchronous registers are:

- WIDR
- WDSC
- WDST
- WISR
- WIER
- WWER
- WWPS

NOTE: Accesses to WD_TIMER2 and WD_TIMER3 are posted.

22.3.5 Watchdog Timer Low-Level Programming Model

This section covers the low-level hardware programming sequences for the configuration and use of the module.

22.3.5.1 Global Initialization

22.3.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the watchdog timer is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the watchdog timer (see Table 22-82). For more information, see Section 22.3.2, *Watchdog Timer Environment*, and Section 22.3.3, *Watchdog Timer Integration.*

Table 22-82. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface and functional clocks must be enabled. For more information about the module configuration, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Section 3.1.1, *Power, Reset, and Clock Management*.
Control module	Module-specific pad muxing must be set in the control module. For more information about the module configuration, see Section 18.4.8, *PAD Functional Multiplexing and Configuration* in Figure 18-1, *Control Module*.
MPU INTC	The MPU INTC configuration must be performed to enable the interrupts from the watchdog timer. See Section 4.1, *Dual Cortex-A15 MPU Subsystem*.

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22.3.5.1.2 Watchdog Timer Module Global Initialization

22.3.5.1.2.1 Main Sequence – Watchdog Timer Module Global Initialization

Table 22-83 lists the steps for initializing the watchdog timer module when the module is to be used for the first time.

Table 22-83. Watchdog Timer Module Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	WDSC[1] SOFTRESET	0x1
Wait until reset release?	WDSC[1] SOFTRESET	0x0
Configure idle mode.	WDSC[4:3] IDLEMODE	xx
Enable delay wakeup.	WIRQWAKEEN[1] DLY_WK_ENA	0x1
Enable overflow wakeup.	WIRQWAKEEN[0] OVF_WK_ENA	0x1
Enable delay interrupt.	WIRQENSET[1] ENABLE_DLY	0x1
Enable overflow interrupt.	WIRQENSET[0] ENABLE_OVF	0x1

22.3.5.2 Operational Mode Configuration

22.3.5.2.1 Watchdog Timer Basic Configuration

22.3.5.2.1.1 Main Sequence – Watchdog Timer Basic Configuration

Table 22-84 lists the steps for the basic configuration of the watchdog timer.

Table 22-84. Watchdog Timer Basic Configuration

Step	Register/Bit Field/Programming Model	Value
Disable the watchdog timer.	See Section 22.3.5.2.1.2.	
Set prescaler value.	WCLR[4:2] PTV	xxx
Enable prescaler.	WCLR[5] PRE	0x1
Load delay configuration value.	WDLY	xxx
Load timer counter value.	WCRR	xxx
Enable the watchdog timer.	See Section 22.3.5.2.1.3.	

22.3.5.2.1.2 Subsequence – Disable the Watchdog Timer

Table 22-85 lists the steps to disable the watchdog timer.

Table 22-85. Disable the Watchdog Timer

Step	Register/Bit Field/Programming Model	Value
Write disable sequence Data1.	WSPR	0xXXXX AAAA
Write disable sequence Data2.	WSPR	0xXXXX 5555

22.3.5.2.1.3 Subsequence – Enable the Watchdog Timer

Table 22-86 lists the steps to enable the watchdog timer.

Table 22-86. Enable the Watchdog Timer

Step	Register/Bit Field/Programming Model	Value
Write enable sequence Data1.	WSPR	0xXXXX BBBB
Write enable sequence Data2.	WSPR	0xXXXX 4444

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22.3.6 Watchdog Timer Register Manual

22.3.6.1 Watchdog Timer Instance Summary

Table 22-87 lists the base address and address space for the watchdog timer module instances.

Table 22-87. Watchdog Timer Instance Summary

Module Name	Base Address L4 Interconnect	Base Address L3 Interconnect	Base Address Cortex-A15 Private Access	Base Address DSP Private Access	Size
WD_TIMER2	0x4AE1 4000	–	–	–	4 KiB
WD_TIMER3	–	0x4903 0000	0x4013 0000	0x3 0000	4 KiB

NOTE: Private access is access that does not use the L3/L4 interconnects.

22.3.6.2 Watchdog Timer Registers

22.3.6.2.1 Watchdog Timer Register Summary

CAUTION

The watchdog timers registers are limited to 32- and 16-bit data accesses; 8-bit access is not allowed and can corrupt register content.

Table 22-88 lists the WD_TIMER2 registers.

Table 22-88. WD_TIMER2 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L4 Interconnect
WIDR	R	32	0x0000 0000	0x4AE1 4000
WDSC	RW	32	0x0000 0010	0x4AE1 4010
WDST	R	32	0x0000 0014	0x4AE1 4014
WISR	RW	32	0x0000 0018	0x4AE1 4018
WIER	RW	32	0x0000 001C	0x4AE1 401C
WWER	RW	32	0x0000 0020	0x4AE1 4020
WCLR	RW	32	0x0000 0024	0x4AE1 4024
WCRR	RW	32	0x0000 0028	0x4AE1 4028
WLDR	RW	32	0x0000 002C	0x4AE1 402C
WTGR	RW	32	0x0000 0030	0x4AE1 4030
WWPS	R	32	0x0000 0034	0x4AE1 4034
WDLY	RW	32	0x0000 0044	0x4AE1 4044
WSPR	RW	32	0x0000 0048	0x4AE1 4048
RESERVED	R	32	0x0000 0050	0x4AE1 4050
WIRQSTATRAW	RW	32	0x0000 0054	0x4AE1 4054
WIRQSTAT	RW	32	0x0000 0058	0x4AE1 4058
WIRQENSET	RW	32	0x0000 005C	0x4AE1 405C
WIRQENCLR	RW	32	0x0000 0060	0x4AE1 4060
WIRQWAKEEN	RW	32	0x0000 0064	0x4AE1 4064

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Table 22-89 lists the WD_TIMERIMER3 registers.

Table 22-89. WD_TIMER3 Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A15 Private Access	Physical Address DSP Private Access
WIDR	R	32	0x0000 0000	0x4903 0000	0x4013 0000	0x3 0000
WDSC	RW	32	0x0000 0010	0x4903 0010	0x4013 0010	0x3 0010
WDST	R	32	0x0000 0014	0x4903 0014	0x4013 0014	0x3 0014
WISR	RW	32	0x0000 0018	0x4903 0018	0x4013 0018	0x3 0018
WIER	RW	32	0x0000 001C	0x4903 001C	0x4013 001C	0x3 001C
WWER	RW	32	0x0000 0020	0x4903 0020	0x4013 0020	0x3 0020
WCLR	RW	32	0x0000 0024	0x4903 0024	0x4013 0024	0x3 0024
WCRR	RW	32	0x0000 0028	0x4903 0028	0x4013 0028	0x3 0028
WLDR	RW	32	0x0000 002C	0x4903 002C	0x4013 002C	0x3 002C
WTGR	RW	32	0x0000 0030	0x4903 0030	0x4013 0030	0x3 0030
WWPS	R	32	0x0000 0034	0x4903 0034	0x4013 0034	0x3 0034
WDLY	RW	32	0x0000 0044	0x4903 0044	0x4013 0044	0x3 0044
WSPR	RW	32	0x0000 0048	0x4903 0048	0x4013 0048	0x3 0048
RESERVED	R	32	0x0000 0050	0x4903 0050	0x4013 0050	0x3 0050
WIRQSTATRAW	RW	32	0x0000 0054	0x4903 0054	0x4013 0054	0x3 0054
WIRQSTAT	RW	32	0x0000 0058	0x4903 0058	0x4013 0058	0x3 0058
WIRQENSET	RW	32	0x0000 005C	0x4903 005C	0x4013 005C	0x3 005C
WIRQENCLR	RW	32	0x0000 0060	0x4903 0060	0x4013 0060	0x3 0060
WIRQWAKEEN	RW	32	0x0000 0064	0x4903 0064	0x4013 0064	0x3 0064

NOTE:

- The WISR and WIRQSTATRAW registers have the same functionality. The WISR register is used for software backward compatibility.
- The WIER and WIRQENSET/WIRQENCLR registers have the same functionality. The WIER register is used for software backward compatibility.
- The WWER and WIRQWAKEEN registers have the same functionality. The WWER is used for software backward compatibility.
- The WIRQSTATRAW and WIRQSTAT registers give the same information when read. The WIRQSTATRAW register is used for debug.

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22.3.6.2.2 Watchdog Timer Register Description

through describe the watchdog timer registers.

Table 22-90. WIDR

Address Offset	0x0000 0000		
Physical Address	0x4AE1 4000 0x4AE1 4000 0x3 0000	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	IP revision identifier		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	IP Revision	R	0x– [1]

[1] TI internal data.

Table 22-91. Register Call Summary for Register WIDR

Watchdog Timers

- Accessing Watchdog Timer Registers: [0]
- Watchdog Timer Register Summary: [1] [2]

Table 22-92. WDSC

Address Offset	0x0000 0010		
Physical Address	0x4AE1 4010 0x4AE1 4010 0x3 0010	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register controls the various parameters of the L4 interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										EMUFREE	IDLEMODE	RESERVED	SOFTRESET	RESERVED	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000000
5	EMUFREE	Emulation mode 0x0: Timer counter frozen in emulation 0x1: Timer counter free-running in emulation	RW	0

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Bits	Field Name	Description	Type	Reset
4:3	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target IDLE state follows (acknowledges) the system idle requests unconditionally, that is, regardless of the IP module internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters IDLE state. Backup mode, for debug only. 0x2: Smart-idle mode: local target IDLE state eventually follows (acknowledges) the system idle requests, depending on the IP module internal requirements. IP module should not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Smart-idle wake-up-capable mode: local target IDLE state eventually follows (acknowledges) the system idle requests, depending on the IP module internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state. Mode is relevant only if the appropriate IP module *swake-up* output(s) is (are) implemented.	RW	0x2
2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
1	SOFTRESET	Software reset. (Optional) Read 0x0: Reset done, no pending action Write 0x0: No action Write 0x1: Initiate software reset. Read 0x1: Reset (software or other) ongoing	RW	0
0	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0

Table 22-93. Register Call Summary for Register WDSC

Watchdog Timers

- Power Management: [0]
- Wake-Up Capability: [1]
- Watchdog Timers Under Emulation: [2] [3]
- Accessing Watchdog Timer Registers: [4]
- Watchdog Timer Module Global Initialization: [5] [6] [7]
- Watchdog Timer Register Summary: [8] [9]

Table 22-94. WDST

Address Offset	0x0000 0014		
Physical Address	0x4AE1 4014 0x4AE1 4014 0x3 0014	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register provides status information about the module.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return 0.	R	0x0000 0000
0	RESETDONE	Internal module reset monitoring Read 0x0: Internal module reset is ongoing. Read 0x1: Reset completed	R	1

Table 22-95. Register Call Summary for Register WDST

Watchdog Timers
- Accessing Watchdog Timer Registers: [0]
- Watchdog Timer Register Summary: [1] [2]

Table 22-96. WISR

Address Offset	0x0000 0018		
Physical Address	0x4AE1 4018 0x4AE1 4018 0x3 0018	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register shows which interrupt events are pending inside the module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DLY_IT_FLAG	OVF_IT_FLAG

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads return 0.	R	0x0000 0000
1	DLY_IT_FLAG	Pending delay interrupt status. Read 0x0: No delay interrupt pending Write 0x0: Status unchanged Write 0x1: Status bit cleared Read 0x1: Delay interrupt pending	RW W1toClr	0
0	OVF_IT_FLAG	Pending overflow interrupt status. Read 0x0: No overflow interrupt pending Write 0x0: Status unchanged Write 0x1: Status bit cleared Read 0x1: Overflow interrupt pending	RW W1toClr	0

Table 22-97. Register Call Summary for Register WISR

Watchdog Timers
- Watchdog Timer Interrupt Generation: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- Accessing Watchdog Timer Registers: [9]
- Watchdog Timer Register Summary: [10] [11] [12] [13]

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Table 22-98. WIER

Address Offset	0x0000 001C		
Physical Address	0x4AE1 401C 0x4AE1 401C 0x3 001C	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register controls (enable/disable) the interrupt events.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DLY_IT_ENA	OVF_IT_ENA

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads return 0.	R	0x0000 0000
1	DLY_IT_ENA	Delay interrupt enable/disable 0x0: Disable delay interrupt. 0x1: Enable delay interrupt.	RW	0
0	OVF_IT_ENA	Overflow interrupt enable/disable 0x0: Disable overflow interrupt. 0x1: Enable overflow interrupt.	RW	0

Table 22-99. Register Call Summary for Register WIER

Watchdog Timers

- Watchdog Timer Interrupt Generation: [0] [1] [2] [3] [4]
- Accessing Watchdog Timer Registers: [5]
- Watchdog Timer Register Summary: [6] [7] [8] [9]

Table 22-100. WWER

Address Offset	0x0000 0020		
Physical Address	0x4AE1 4020 0x4AE1 4020 0x3 0020	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register controls (enable/disable) the wake-up events.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DLY_WK_ENA	OVF_WK_ENA

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	DLY_WK_ENA	Delay wake-up enable 0x0: Disable delay wakeup. 0x1: Enable delay wakeup.	RW	0

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Bits	Field Name	Description	Type	Reset
0	OVF_WK_ENA	Overflow wake-up enable 0x0: Disable overflow wakeup. 0x1: Enable overflow wakeup.	RW	0

Table 22-101. Register Call Summary for Register WWER

Watchdog Timers

- Accessing Watchdog Timer Registers: [0]
- Watchdog Timer Register Summary: [1] [2] [3] [4]

Table 22-102. WCLR

Address Offset	0x0000 0024		
Physical Address	0x4AE1 4024 0x4AE1 4024 0x3 0024	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register controls the prescaler stage of the counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										PRE	PTV			RESERVED	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reads return 0.	R	0x0000000
5	PRE	Prescaler enable/disable configuration 0x0: Prescaler disabled 0x1: Prescaler enabled	RW	1
4:2	PTV	Prescaler value The timer counter is prescaled with the value: 2^{PTV}. Example: PTV = 3 -> counter increases value if started after 8 functional clock periods. On reset, it is loaded from PI_PTV_RESET_VALUE input port.	RW	0x0
1:0	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0

Table 22-103. Register Call Summary for Register WCLR

Watchdog Timers

- General Watchdog Timer Operation: [0] [1] [2]
- Reset Context: [3] [4]
- Prescaler Value/Timer Reset Frequency: [5] [6] [7] [8] [9] [10]
- Modifying Timer Count/Load Values and Prescaler Setting: [11]
- Accessing Watchdog Timer Registers: [12]
- Watchdog Timer Basic Configuration: [13] [14]
- Watchdog Timer Register Summary: [15] [16]
- Watchdog Timer Register Description: [17]

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Table 22-104. WCRR

Address Offset	0x0000 0028		
Physical Address	0x4AE1 4028 0x4AE1 4028 0x3 0028	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register holds the value of the internal counter.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER_COUNTER																															

Bits	Field Name	Description	Type	Reset
31:0	TIMER_COUNTER	Value of the timer counter register	RW	0x0000 0000

Table 22-105. Register Call Summary for Register WCRR

Watchdog Timers

- General Watchdog Timer Operation: [0]
- Overflow/Reset Generation: [1]
- Modifying Timer Count/Load Values and Prescaler Setting: [2]
- Watchdog Counter Register Access Restriction (WCRR): [3] [4] [5] [6]
- Watchdog Timer Interrupt Generation: [7]
- Accessing Watchdog Timer Registers: [8]
- Watchdog Timer Basic Configuration: [9]
- Watchdog Timer Register Summary: [10] [11]
- Watchdog Timer Register Description: [12]

Table 22-106. WLDR

Address Offset	0x0000 002C		
Physical Address	0x4AE1 402C 0x4AE1 402C 0x3 002C	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register holds the timer load value.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER_LOAD																															

Bits	Field Name	Description	Type	Reset
31:0	TIMER_LOAD	Value of the timer load register	RW	0x0000 0000

Table 22-107. Register Call Summary for Register WLDR

Watchdog Timers

- General Watchdog Timer Operation: [0]
- Reset Context: [1] [2]
- Overflow/Reset Generation: [3]
- Prescaler Value/Timer Reset Frequency: [4] [5] [6] [7] [8] [9] [10]
- Triggering a Timer Reload: [11]
- Modifying Timer Count/Load Values and Prescaler Setting: [12]
- Watchdog Timer Interrupt Generation: [13] [14] [15]
- Accessing Watchdog Timer Registers: [16]
- Watchdog Timer Register Summary: [17] [18]
- Watchdog Timer Register Description: [19]

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Table 22-108. WTGR

Address Offset	0x0000 0030		
Physical Address	0x4AE1 4030 0x4AE1 4030 0x3 0030	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	Writing a different value than the one already written in this register does a watchdog counter reload.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTGR_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	TTGR_VALUE	Value of the trigger register	RW	0x0000 0000

Table 22-109. Register Call Summary for Register WTGR

Watchdog Timers

- General Watchdog Timer Operation: [0]
- Triggering a Timer Reload: [1] [2]
- Modifying Timer Count/Load Values and Prescaler Setting: [3]
- Accessing Watchdog Timer Registers: [4]
- Watchdog Timer Register Summary: [5] [6]
- Watchdog Timer Register Description: [7]

Table 22-110. WWPS

Address Offset	0x0000 0034		
Physical Address	0x4AE1 4034 0x4AE1 4034 0x3 0034	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register contains the write posting bits for all writeable functional registers.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										W_PEND_WDLY	W_PEND_WSPR	W_PEND_WTGR	W_PEND_WLDR	W_PEND_WCRR	W_PEND_WCLR

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000000
5	W_PEND_WDLY	Write pending for register WDLY Read 0x0: No register write pending Read 0x1: Register write pending	R	0
4	W_PEND_WSPR	Write pending for register WSPR Read 0x0: No register write pending Read 0x1: Register write pending	R	0
3	W_PEND_WTGR	Write pending for register WTGR Read 0x0: No register write pending Read 0x1: Register write pending	R	0

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Bits	Field Name	Description	Type	Reset
2	W_PEND_WLDR	Write pending for register WLDR Read 0x0: No register write pending Read 0x1: Register write pending	R	0
1	W_PEND_WCRR	Write pending for register WCRR Read 0x0: No register write pending Read 0x1: Register write pending	R	0
0	W_PEND_WCLR	Write pending for register WCLR Read 0x0: No register write pending Read 0x1: Register write pending	R	0

Table 22-111. Register Call Summary for Register WWPS

Watchdog Timers
- Accessing Watchdog Timer Registers: [0]
- Watchdog Timer Register Summary: [1] [2]

Table 22-112. WDLY

Address Offset	0x0000 0044		
Physical Address	0x4AE1 4044 0x4AE1 4044 0x3 0044	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register holds the delay value that controls the internal pre-overflow event detection.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDLY_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	WDLY_VALUE	Value of the delay register	RW	0x0000 0000

Table 22-113. Register Call Summary for Register WDLY

Watchdog Timers
- Modifying Timer Count/Load Values and Prescaler Setting: [0]
- Watchdog Timer Interrupt Generation: [1] [2] [3] [4] [5] [6] [7] [8]
- Accessing Watchdog Timer Registers: [9]
- Watchdog Timer Basic Configuration: [10]
- Watchdog Timer Register Summary: [11] [12]
- Watchdog Timer Register Description: [13]

Table 22-114. WSPR

Address Offset	0x0000 0048		
Physical Address	0x4AE1 4048 0x4AE1 4048 0x3 0048	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register holds the start-stop value that controls the internal start-stop FSM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WSPR_VALUE																															

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Bits	Field Name	Description	Type	Reset
31:0	WSPR_VALUE	Value of the start-stop register	RW	0x0000 0000

Table 22-115. Register Call Summary for Register WSPR

Watchdog Timers

- General Watchdog Timer Operation: [0]
- Prescaler Value/Timer Reset Frequency: [1] [2]
- Start/Stop Sequence for Watchdog Timers (Using the WSPR Register): [3] [4] [5] [6] [7] [8]
- Modifying Timer Count/Load Values and Prescaler Setting: [9]
- Accessing Watchdog Timer Registers: [10]
- Watchdog Timer Basic Configuration: [11] [12] [13] [14]
- Watchdog Timer Register Summary: [15] [16]
- Watchdog Timer Register Description: [17]

Table 22-116. WIRQSTATRAW

Address Offset	0x0000 0054		
Physical Address	0x4AE1 4054 0x4AE1 4054 0x3 0054	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	IRQ unmasked status, status set per-event raw interrupt status vector, line 0. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVENT_DLY	EVENT_OVF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	EVENT_DLY	Settable raw status for delay event Read 0x0: No event pending Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending	RW W1toSet	0
0	EVENT_OVF	Settable raw status for overflow event Read 0x0: No event pending Write 0x0: No action Write 0x1: Set event (debug) Read 0x1: Event pending	RW W1toSet	0

Table 22-117. Register Call Summary for Register WIRQSTATRAW

Watchdog Timers

- Watchdog Timer Register Summary: [0] [1] [2] [3] [4]

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Table 22-118. WIRQSTAT

Address Offset	0x0000 0058		
Physical Address	0x4AE1 4058 0x4AE1 4058 0x3 0058	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	IRQ masked status, status clear per-event enabled interrupt status vector, line 0. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EVENT_DLY	EVENT_OVF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	EVENT_DLY	Clearable, enabled status for delay event Read 0x0: No (enabled) event pending Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending	RW W1toClr	0
0	EVENT_OVF	Clearable, enabled status for overflow event Read 0x0: No (enabled) event pending Write 0x0: No action Write 0x1: Clear (raw) event Read 0x1: Event pending	RW W1toClr	0

Table 22-119. Register Call Summary for Register WIRQSTAT

Watchdog Timers

- Interrupts: [0] [1]
- General Watchdog Timer Operation: [2]
- Watchdog Timer Interrupt Generation: [3]
- Watchdog Timer Register Summary: [4] [5] [6]

Table 22-120. WIRQENSET

Address Offset	0x0000 005C		
Physical Address	0x4AE1 405C 0x4AE1 405C 0x3 005C	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	IRQ enable set per-event interrupt enable bit vector, line 0. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ENABLE_DLY	ENABLE_OVF

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	ENABLE_DLY	Enable for delay event Read 0x0: Interrupt disabled (masked) Write 0x0: No action Write 0x1: Enable interrupt. Read 0x1: Interrupt enabled	RW W1toSet	0
0	ENABLE_OVF	Enable for overflow event Read 0x0: Interrupt disabled (masked) Write 0x0: No action Write 0x1: Enable interrupt. Read 0x1: Interrupt enabled	RW W1toSet	0

Table 22-121. Register Call Summary for Register WIRQENSET

Watchdog Timers

- Interrupts: [0] [1]
- General Watchdog Timer Operation: [2]
- Watchdog Timer Interrupt Generation: [3]
- Watchdog Timer Module Global Initialization: [4] [5]
- Watchdog Timer Register Summary: [6] [7] [8]

Table 22-122. WIRQENCLR

Address Offset	0x0000 0060		
Physical Address	0x4AE1 4060 0x4AE1 4060 0x3 0060	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	IRQ enable clear per-event interrupt enable bit vector, line 0. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ENABLE_DLY	ENABLE_OVF

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	ENABLE_DLY	Enable for delay event Read 0x0: Interrupt disabled (masked) Write 0x0: No action Write 0x1: Disable interrupt. Read 0x1: Interrupt enabled	RW W1toClr	0
0	ENABLE_OVF	Enable for overflow event Read 0x0: Interrupt disabled (masked) Write 0x0: No action Write 0x1: Disable interrupt. Read 0x1: Interrupt enabled	RW W1toClr	0

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Table 22-123. Register Call Summary for Register WIRQENCLR

Watchdog Timers

- Interrupts: [0] [1]
- General Watchdog Timer Operation: [2]
- Watchdog Timer Register Summary: [3] [4] [5]

Table 22-124. WIRQWAKEEN

Address Offset	0x0000 0064		
Physical Address	0x4AE1 4064 0x4AE1 4064 0x3 0064	**Instance**	TIMER2_L4 WD_TIMER2_L4 WD_TIMER3_DSP
Description	This register controls (enable/disable) the wake-up events.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DLY_WK_ENA	OVF_WK_ENA

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x0000 0000
1	DLY_WK_ENA	Enable delay wake-up 0x0: Disable delay wakeup 0x1: Enable delay wakeup	RW	0
0	OVF_WK_ENA	Enable overflow wakeup 0x0: Disable overflow wakeup 0x1: Enable overflow wakeup	RW	0

Table 22-125. Register Call Summary for Register WIRQWAKEEN

Watchdog Timers

- Power Management: [0]
- Wake-Up Capability: [1] [2]
- Watchdog Timer Module Global Initialization: [3] [4]
- Watchdog Timer Register Summary: [5] [6] [7]

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22.4 32-kHz Synchronized Timer

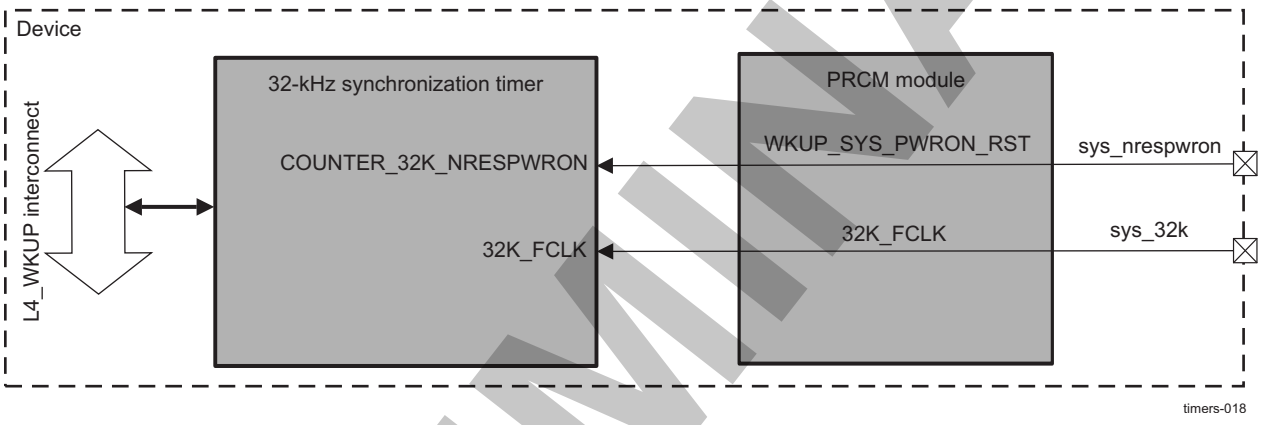
22.4.1 32-kHz Synchronized Timer Overview

The 32-kHz synchronized timer is a 32-bit counter clocked by the falling edge of the 32-kHz system clock. It is reset while the external asynchronous power-up reset (sys_nrespwron) primary I/O is active (main device reset). When sys_nrespwron is released (on the rising edge of sys_nrespwron), after three 32-kHz clock periods, the counter starts counting up from the reset value of the counter register on the falling edge of the 32-kHz system clock. After reaching its highest value, the counter wraps back to 0 and starts counting again.

Figure 22-18 is the block diagram of the 32-kHz synchronized timer.

NOTE: sys_nrespwron is an active-low I/O.

Figure 22-18. 32-kHz Synchronized Timer Block Diagram



22.4.1.1 32-kHz Synchronized Timer Features

The main features of the 32-kHz synchronized timer controller are:

- L4 slave interface (OCP) support:
  - 32-bit data bus width
  - 32-/16-bit access supported
  - 8-bit access not supported
  - 16-bit address bus width
  - Burst mode not supported
  - Write nonposted transaction mode not supported
- Only read operations are supported on the module registers; no write operation is supported (no error/no action on write).
- Free-running 32-bit upward counter
- Start and keep counting after power-on reset
- Automatic roll over to 0; highest value reached: 0xFFFF FFFF
- On-the-fly read (while counting)

22.4.2 32-kHz Synchronized Timer Environment

The synchronized timer is accessible only through the L4 interface.

22.4.3 32-kHz Synchronized Timer Integration

Table 22-126 through Table 22-128 summarize the integration of the module in the device.

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Table 22-126. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
COUNTER_32K	PD_WKUP	No	L4_WKUP

Table 22-127. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
COUNTER_32K	COUNTER_32K_FCLK	APE_32KCLK	PRCM	COUNTER_32K functional clock
COUNTER_32K	COUNTER_32K_ICLK	WKUPAON_GICLK	PRCM	COUNTER_32K interface clock
Resets				
COUNTER_32K	COUNTER_32K_NRESPWRON	WKUPAON_SYS_PWRON_RST	PRM	Reset to COUNTER_32K
COUNTER_32K	COUNTER_32K_WKUP_RST	WKUPAON_RST	PRM	Reset to COUNTER_32K

Table 22-128. Hardware Requests

No Interrupt Requests
No DMA Requests

22.4.4 32-kHz Synchronized Timer Functional Description

The synchronized timer is a counter that starts on the rising edge of an external asynchronous signal (sys_nrespwron). When sys_nrespwron is released (on the rising edge of sys_nrespwron), the counter starts counting up from the reset value of the counter register on the falling edge of the 32-kHz system clock after three inverted 32-kHz clock periods. After reaching its highest value, the counter wraps back to 0 and starts counting again with no additional delay. When sys_nrespwron is released (on the rising edge of sys_nrespwron), after three inverted 32-kHz clock periods, the counter starts counting up from the reset value of the counter register on the falling edge of the 32-kHz system clock.

Figure 22-19 shows the reset synchronization timing diagram. After reaching its highest value, the counter wraps back to 0 and starts counting again without any extra delay.

Figure 22-19. Reset Resynchronization Timing Diagram

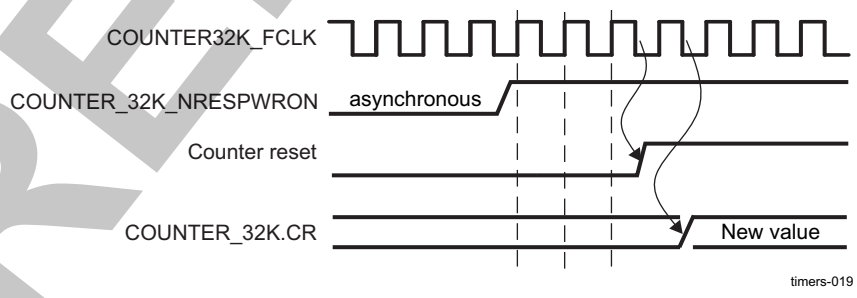

Figure 22-20 is the block diagram of the synchronized timer.

NOTE: sys_nrespwron is an active-low input.

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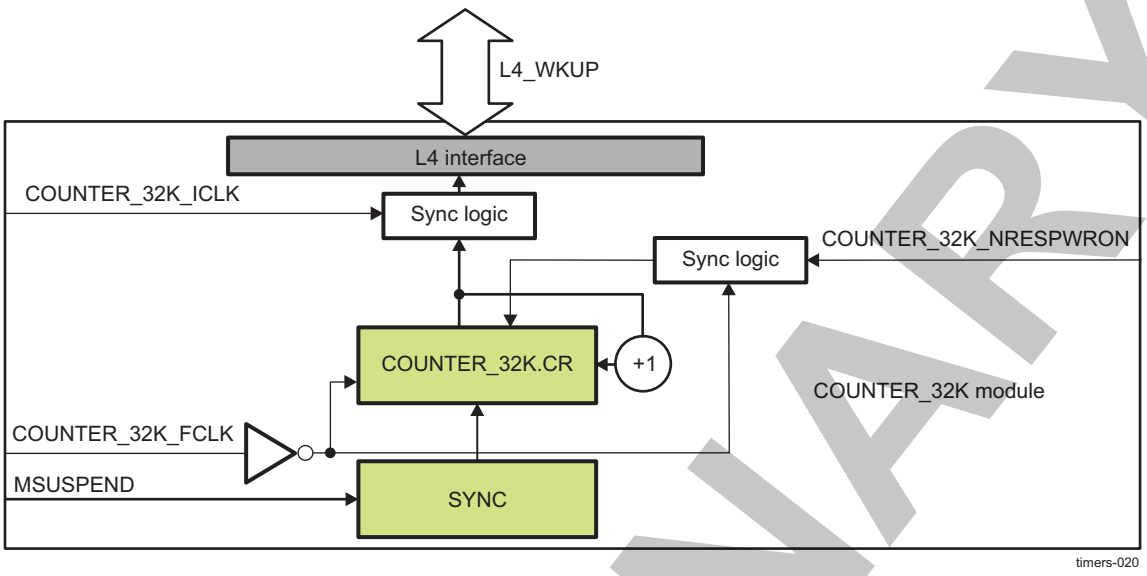
Figure 22-20. CONTER_32K Block Diagram



The sync logic ensures the correctness of the read transaction by synchronizing the counter register read access on COUNTER_32K_ICLK, because the COUNTER_32K_ICLK clock signal is completely asynchronous with COUNTER_32K_FCLK. The sys_nrespwron input resets the counter register (CR). The inverted COUNTER_32K_FCLK clocks the sys_nrespwron reset signal.

22.4.4.1 Reading the 32-kHz Synchronized Timer

The counter register (CR) is 32 bits wide. For correct count capture, it must be accessed as 16-bit LSB access first and 16-bit MSB access next.The value of the counter is read through the L4 interconnect slave interface. Internal synchronization logic allows the reading of the counter value with COUNTER_32K_ICLK while the counter is running. The time latency to read the synchronized counter register is one COUNTER_32K_ICLK clock period.

The user can select between two syncronization schemes by setting SYSCONFIG[0]SYNCMODE bit.

- SYSCONFIG[0] SYNCMODE = 0x0 - default mode. In this mode the COUNTER_32K timer uses Gray encode/decode scheme. When the L4 interface sends a LSB16 read request command, the 32 bit coded value is registered directly to the interface domain. Due to the characteristics of this encoding if a read command arrives during a count up event either the old or the new value of CR is captured, not a transient value. The captured value will be decoded and sent on the SDATA bus. The MSB16 read command reads upper 16 bits of the 32 bit value of counter register captured during the last LSB16 read access.
- SYSCONFIG[0] SYNCMODE = 0x1 - legacy synchronization scheme. In this mode the value of the CR is synchronized to the OCP domain at every count up event. This synchronization is possible because the COUNTER_32K_ICLK is much faster than the 32KHz clock. The drawback of this method is that if the interface clock is switched off by PRCM during idle mode, the synchronization stops until the interface clock is switched back. The syncronized value will be updated the next count up event after wake up from idle mode, until then it will be incorrect.

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22.4.5 COUNTER_32K Timer Register Manual

Table 22-129 lists the base address and block size for the 32-kHz synchronized timer. It is memory-mapped to the L4 peripheral bus memory space.

Table 22-129. COUNTER_32KTimer Instance Summary

Module Name	Base Address L4 Interconnect	Size
COUNTER_32K	0x4AE0 4000	4 KiB

22.4.5.1 COUNTER_32K Timer Register Mapping Summary

CAUTION

The 32-kHz synchronized timer registers are limited to 32- and 16-bit data accesses; 8-bit access is not allowed and can corrupt the register content.

Table 22-130 lists the 32-kHz synchronized timer registers. Table 22-131 through Table 22-135 describe the register bits.

Table 22-130. COUNTER_32KTimer Register Summary

Register Name	Type	Register Width (Bits)	Offset Address	Physical Address L4 Interconnect
REVISION	RO	32	0x0000	0x4AE0 4000
SYSCONFIG	R/W	32	0x00010	0x4AE0 4010
CR	RO	32	0x0030	0x4AE0 4030

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22.4.5.2 COUNTER_32K Timer Register Description

Table 22-131. REVISION

Address Offset	0x0000
Physical Address	0x4AE0 4000
Description	This register contains the sync counter IP revision code.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	IP revision	R	0x-(1)

(1) TI internal data

Table 22-132. Register Call Summary for Register REVISION

32-kHz Synchronized Timer

- COUNTER_32K Timer Register Mapping Summary: [0]

Table 22-133. SYSCONFIG

Address Offset	0x0004
Physical Address	0x4AE0 4010
Description	This register is used for idle modes only.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											IDLEMODE		Reserved		SYNCMODE

Bits	Field Name	Description	Type	Reset
31:5	Reserved	Reads return 0.	R	0x0
4:3	IDLEMODE	Power management REQ/ACK control	RW	0x0
		0x0: Force-idle. An IDLE request is acknowledged unconditionally.		
		0x1: No-idle. An IDLE request is never acknowledged.		
		0x2: Reserved		
		0x3: Reserved		
2:1	Reserved	Reads return 0.	R	0x0
0	SYNCMODE	Synchronization scheme	RW	0x0
		0x0: Gray syncrhonization scheme. Ensures that a stable value of the CR register is read.		
		0x1 Legacy synchronization scheme.		

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Table 22-134. Register Call Summary for Register SYSCONFIG

32-kHz Synchronized Timer

- Reading the 32-kHz Synchronized Timer: [0] [1] [2]
- COUNTER_32K Timer Register Mapping Summary: [3]

Table 22-135. CR

Address Offset	0x0010
Physical Address	0x4AE0 4030
Description	This register contains the 32-kHz sync counter value.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER_VALUE																															

Bits	Field Name	Description	Type	Reset
31:0	COUNTER_VALUE	Counter register value	R	0x00000003

Table 22-136. Register Call Summary for Register CR

32-kHz Synchronized Timer

- 32-kHz Synchronized Timer Functional Description: [0]
- Reading the 32-kHz Synchronized Timer: [1] [2] [3]
- COUNTER_32K Timer Register Mapping Summary: [4]
- COUNTER_32K Timer Register Description: [5]

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Serial Communication Interfaces

This chapter describes the features and operation of the device serial communication interfaces (SCI).

NOTE: Some of the serial interfaces and some of their features, primarily those concerning the device I/O pads, are not available in all OMAP54xx devices.

For details, see Section 1.5, *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

Topic **Page**

23.1 Multimaster High-Speed I²C Controller 4605
23.2 HDQ1W 4682
23.3 UART/IrDA/CIR 4701
23.4 Multichannel Serial Port Interface 4817
23.5 Multichannel Buffered Serial Port (MCBSP) 4882
23.6 Multichannel PDM Controller 4988
23.7 Digital Microphone Module 5033
23.8 Multichannel Audio Serial Port 5064
23.9 MIPI-HSI 5179
23.10 High-Speed Multiport USB Host Subsystem 5253
23.11 Super-Speed USB OTG Subsystem 5369
23.12 SATA Controller 5530

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23.1 Multimaster High-Speed I²C Controller

This section describes the five high-speed inter-integrated circuit (I²C™) controller modules in the device.

23.1.1 HS I²C Overview

The device contains five multimaster high-speed (HS) inter-integrated circuit (I²C) controllers (I2C*i* modules, where *i* = 1, 2, 3, 4, 5), each of which provides an interface between a local host (LH), such as a digital signal processor (DSP), and any I²C-bus-compatible device that connects through the I²C serial bus. External components attached to the I²C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I²C interface.

Each multimaster HS I²C controller can be configured to act like a slave or master I²C-compatible device.

The device contains additional sixth I2C for SmartReflex1.5™ voltage control, and seventh in HDMI interface which are not described in this section but in the PRCM and Display SubSystem respectively.

The I2C1 instance is typically reserved for platform specific usage to control the power-management-, audio-, and battery-management- companion integrated circuits (ICs)

Figure 23-1 shows the I²C.

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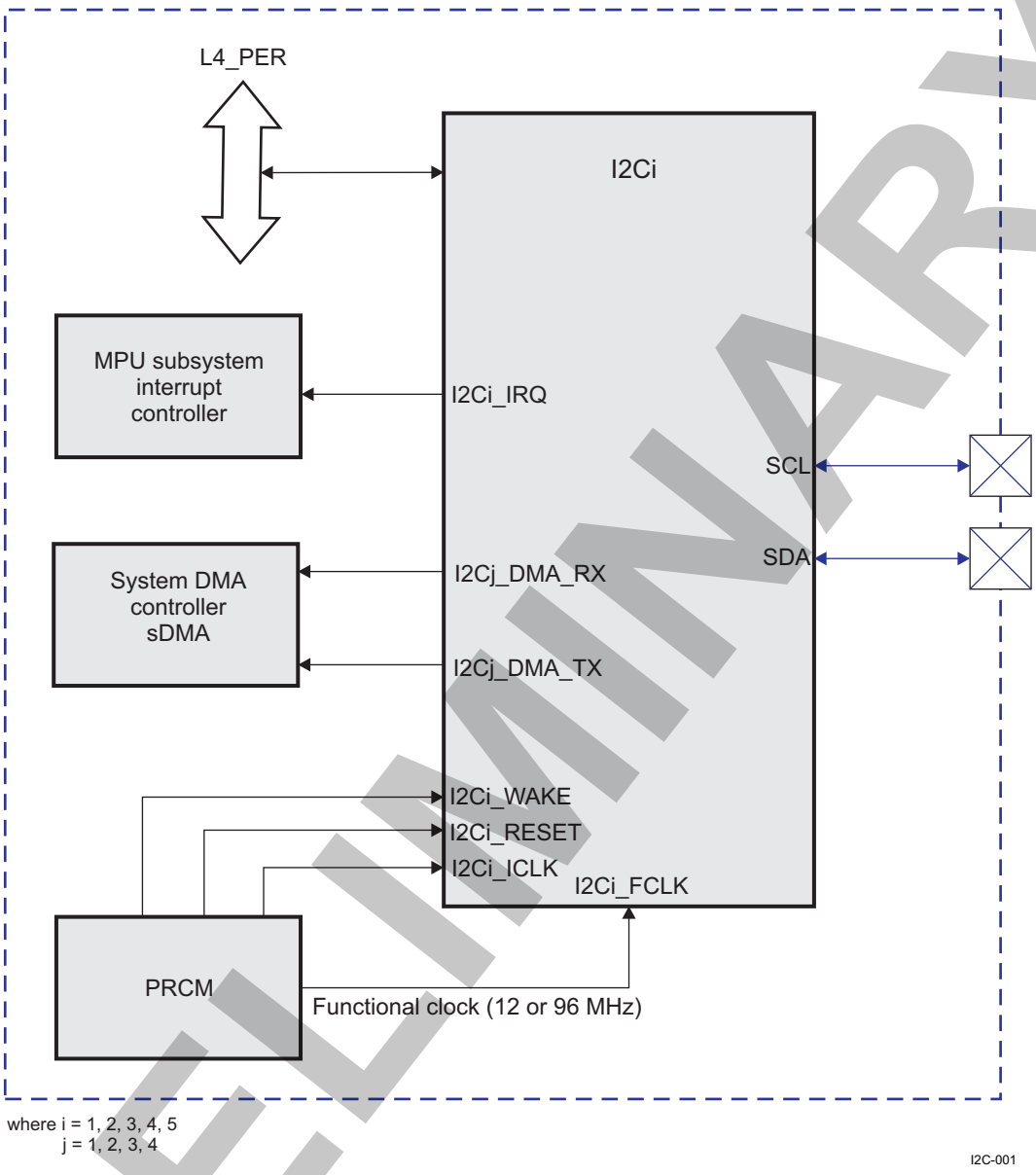
Figure 23-1. HS I²C Controllers



The multimaster HS I²C controllers have the following features:

- Compliant with Philips I²C specification version 2.1
- Supports a standard mode (up to 100 kbps) and fast mode (up to 400 kbps)
- Supports HS mode for transfer up to 3.4 Mbps
- 7-bit and 10-bit device addressing modes
- General call
- Start/Restart/Stop
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit mode
- Built-in configurable FIFOs (8, 16, 32, 64 bytes) for buffered read or write
- Module enable/disable capability

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- Programmable multislave channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Designed for low power consumption
- Implement Auto Idle mechanism
- Implement Idle Request/Idle Acknowledge handshake mechanism
- Support for asynchronous wakeup mechanism
- Two direct memory access (DMA) channels
- Wide interrupt capability

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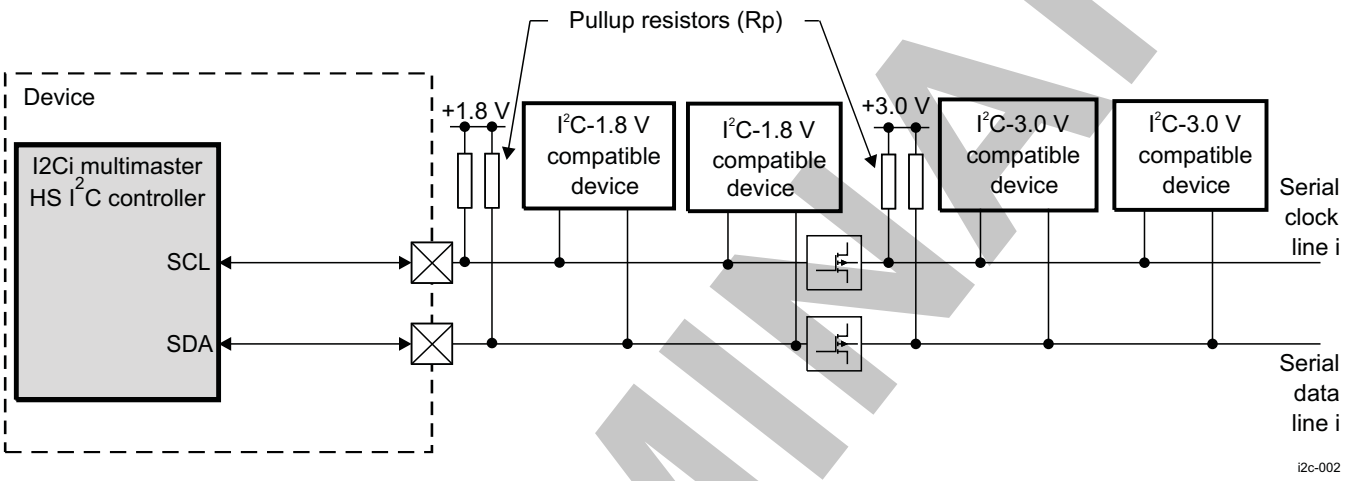
23.1.2 HS I²C Environment

This section describes the HS I²C application fields from an environment point of view (external connections). It describes HS I²C connectivity options, lists all possible interfaces, and describes the protocol and data format used in each case.

23.1.2.1 HS I²C Typical Application

Figure 23-2 shows the multimaster HS I²C controllers and their related connections with I²C-compliant devices.

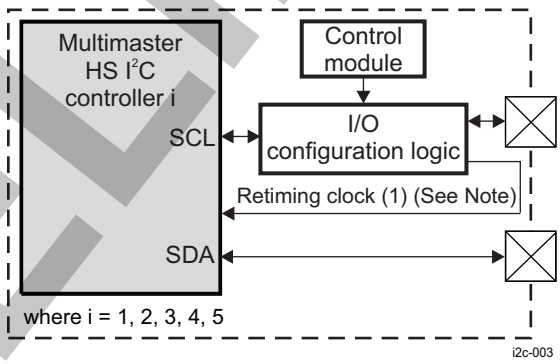
Figure 23-2. HS I²C and Typical Connections to I²C Devices



23.1.2.1.1 HS I²C Pins for Typical Connections in I²C Mode

Figure 23-3 shows the multimaster HS I²C controller pins used for typical connections with I²C devices.

Figure 23-3. HS I²C Interface Signals



(1) In master mode, the clock signal (IP clk configured as output) is also used as a retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

23.1.2.1.2 HS I²C Interface Typical Connections

Table 23-1 lists the pins associated with the I²C interface.

Table 23-1. HS I²C Input/Output

Signal	Device Level Signal	I/O(1)	Description	Reset Value
SCL	i2c1_pmic_scl	I/O	Master platform I2C clock	1

(1) I = Input; O = Output

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Table 23-1. HS I²C Input/Output (continued)

Signal	Device Level Signal	I/O[1]	Description	Reset Value
SDA	i2c1_pmic_sda	I/O	Master platform I2C data	1
SCL	i2c*i*_scl[2]	I/O	I²C serial clock line[3]. Open-drain output buffer. Requires external pullup resistor (Rp).	1
SDA	i2c*i*_sda[2]	I/O	I²C serial data line. Open-drain output buffer. Requires external Rp.	1

(2) i= 2 to 5

(3) This output signal is also used as retiming input.

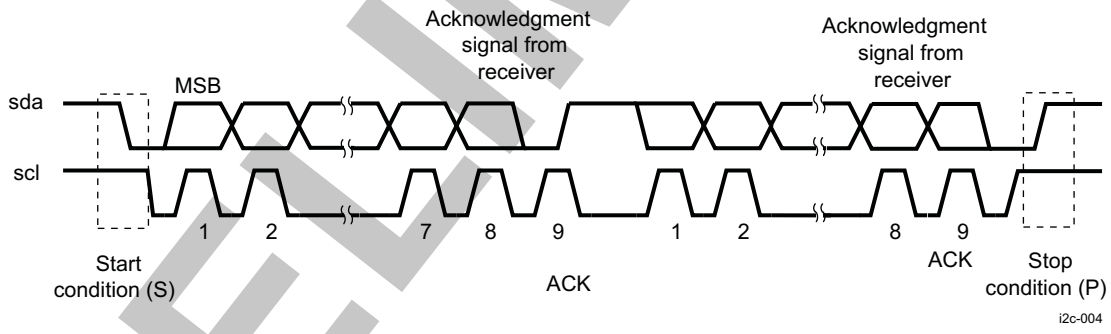
NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and is programmable in the Control Module registers. Refer to the sections Section 18.4.8 *Pad Functional Multiplexing and* Section 18.4.12.7.5 *Configuration* and *Device Interfaces Signal Group Controls Mapping* of the chapter *Figure 18-1 Control Module*, for more information.

23.1.2.1.3 HS I²C Typical Connection Protocol and Data Format

23.1.2.1.3.1 HS I²C Serial Data Format

The I²C controller operates in 8-bit word data format (byte write access supported for the last access). Each byte transmitted or received on the serial data line is 8 bits long. The number of bytes that can be transmitted or received is not restricted. The data is transferred with the most-significant bit (MSB) first. In receiver mode, each byte is followed by an acknowledge bit from the I²C. Figure 23-4 shows a typical I²C communication format.

Figure 23-4. HS I²C Data Transfer



23.1.2.1.3.2 HS I²C Data Validity

The data on the serial data line (SDA) must be stable during the high period of the serial clock line. The high and low states of the data line can change only when the clock signal on the serial clock line (SCL) is low.

Figure 23-5 is an example of data validity requirements.

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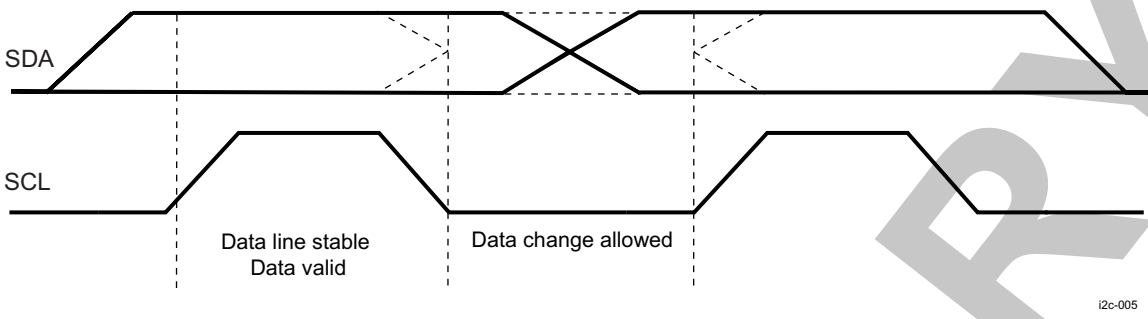
Figure 23-5. HS I²C Bit Transfer on the I²C Bus



23.1.2.1.3.3 HS I²C Start and Stop Conditions

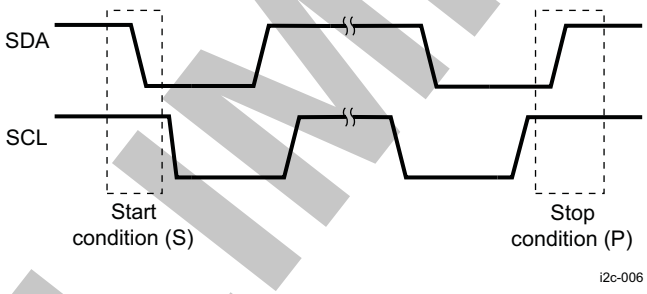
The I²C module generates start (S) and stop (P) conditions when it is configured as a master.

- An S condition is a high-to-low transition on the serial data line while serial clock line is high.
- A P condition is a low-to-high transition on the serial data line while serial clock line is high.

The bus is considered busy after the S condition (the I2C*i*.I2C_IRQSTATUS_RAW [12] BB bit is 1 to indicate that the bus is busy) and free after the P condition (the I2C*i*.I2C_IRQSTATUS_RAW [12] BB bit is 0 to indicate that the bus is free).

Figure 23-6 shows the waveforms that occur during an S and a P condition.

Figure 23-6. HS I²C S and P Condition Events



23.1.2.1.3.4 HS I²C Addressing

The I²C module supports two data formats in fast/standard (F/S) and HS modes:

- 7-bit/10-bit addressing format
- 7-bit/10-bit addressing format with repeated start (Sr) condition

23.1.2.1.3.4.1 Data Transfer Formats in F/S Mode

Figure 23-7 shows the I²C data transfer formats in F/S mode.

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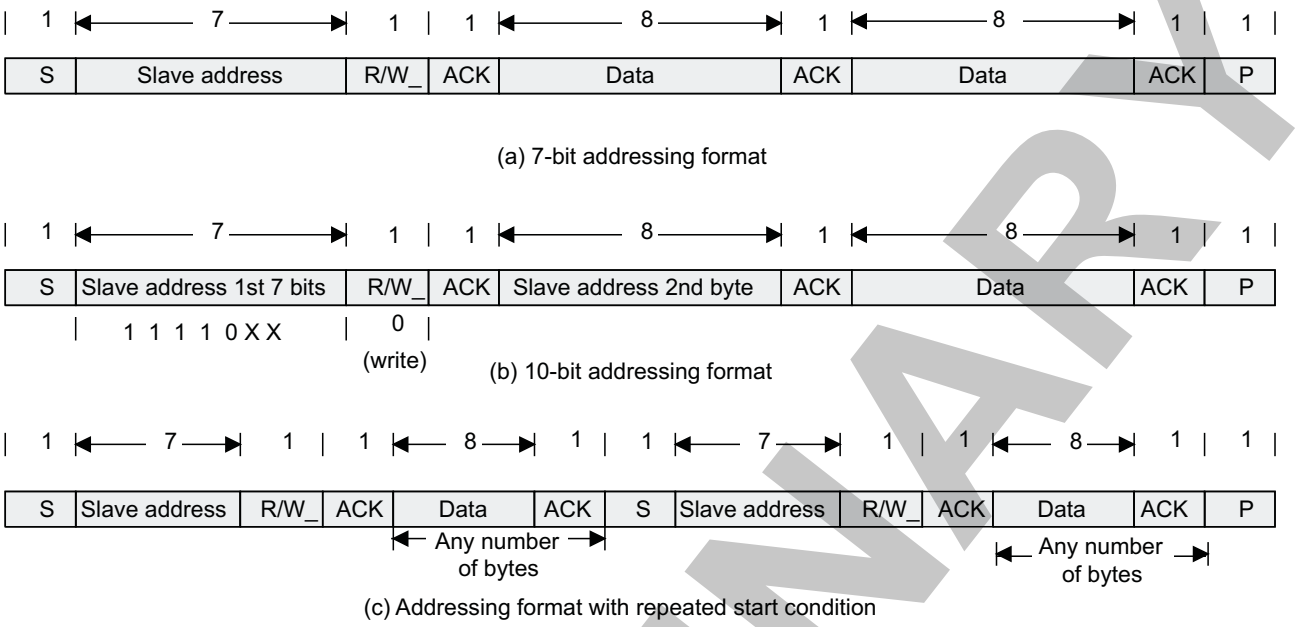
Figure 23-7. HS I²C Data Transfer Formats in F/S Mode



The first word after an S condition consists of 8 bits. In acknowledge mode, an extra dedicated acknowledgment bit is inserted after each byte.

In addressing formats with 7-bit addresses, the first byte is composed of 7 MSB slave address bits and 1 least-significant bit (LSB) R/W_ bit.

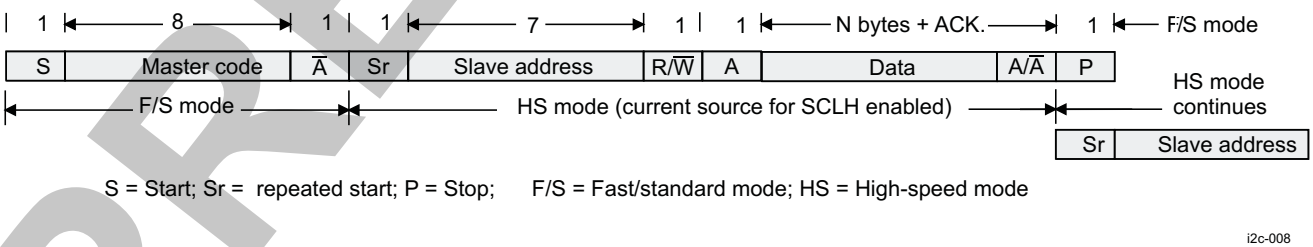
The LSB R/W_ bit of the address byte indicates the transmission direction of the data bytes that follow it. If R/W_ is 0, the master writes data to the selected slave; if it is 1, the master reads data from the slave.

In addressing formats with 10-bit addresses, the structure of the first byte is 11110XXY, where XX is the two MSBs of the 10-bit addresses, and Y is the R/W_ bit. If the R/W_ bit is 0, the next byte contains the last 8 bits of the slave address. If the R/W_ bit is 1, the next byte contains data transmitted from the slave to the master.

23.1.2.1.3.4.2 Data Transfer Format in HS Mode

Figure 23-8 shows the I²C data transfer format in HS mode.

Figure 23-8. HS I²C Data Transfer in HS Mode



Each multimaster HS I²C controller can also operate in HS mode. In this case, after the S condition, the module, which is in F/S mode, writes the master code address (000001XXX, where XXX is the variable portion of the master code) on the bus. No device connected on the same bus acknowledges this address. The module switches the clock to the HS clock and after an Sr condition, and sends the slave address and the data, as shown in Figure 23-8.

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23.1.2.1.3.5 HS I²C Master Transmitter

In master transmitter mode, data assembled in one of the previously described data formats is shifted out on the serial data line SDA in sync with the self-generated clock pulses on the serial clock line SCL. The clock pulses are inhibited and SCL is held low when the intervention of the processor is required (XUDF) after a byte is transmitted.

23.1.2.1.3.6 HS I²C Master Receiver

Master receiver mode can be entered only from master transmitter mode. With any of the address formats (a), (b), or (c) (see Figure 23-7), if R/W_ is high, the module enters master receiver mode after the slave address byte and bit R/W_ are transmitted. Serial data bits received on bus line SDAI are shifted in synchronization with the self-generated clock pulses on SCLI.

23.1.2.1.3.7 HS I²C Slave Transmitter

Slave transmitter mode can be entered only from slave receiver mode. With any of the address formats (a), (b), or (c) (see Figure 23-7), the slave transmitter is entered if the slave address byte is the same as its own address and bit R/W_ is transmitted, if R/W_ is high. The slave transmitter shifts the serial data out on the data line SDA in sync with the clock pulses that are generated by the master device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (XUDF).

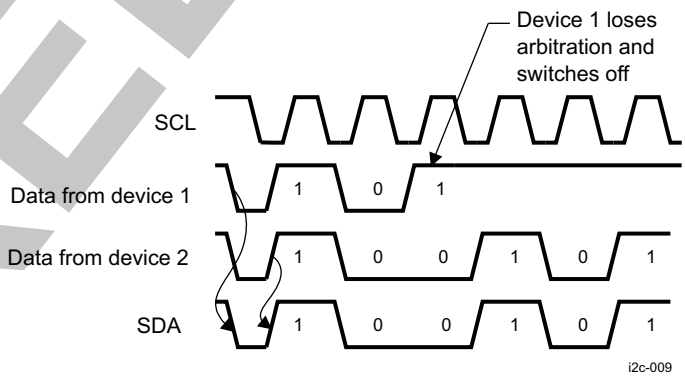
23.1.2.1.3.8 HS I²C Slave Receiver

In this mode, serial data bits received on the bus line SDA are shifted-in in sync with the clock pulses on SCL that are generated by the master device. It does not generate the clock but it can hold clock line SCL low while intervention of the LH is required (ROVR) after a byte is received.

23.1.2.1.3.9 HS I²C Bus Arbitration

If two or more master transmitters start a transmission on the same bus almost simultaneously, an arbitration procedure is invoked. The arbitration procedure uses the data presented on the serial bus by the competing transmitters. When a transmitter senses that a high signal it has presented on the bus has been overruled by a low signal, it switches to the slave receiver mode, sets the arbitration lost (AL) flag, and generates the arbitration lost interrupt. Figure 23-9 shows the arbitration procedure between two devices. The arbitration procedure gives priority to the device that transmits the serial data stream with the lowest binary value. If two or more devices send identical first bytes, arbitration continues on the subsequent bytes.

Figure 23-9. HS I²C Arbitration Between Master Transmitters



23.1.2.1.3.10 HS I²C Clock Generation and Synchronization

Under normal conditions, only one master device generates the clock signal, SCL. However, there are two or more master devices during the arbitration procedure, and the clock must be synchronized so that the data output can be compared. The wired-AND property of the clock line means that a device that first generates a low period of the clock line overrules the other devices. At this high/low transition, the clock generators of the other devices are forced to start generation of their own low period. The clock line is

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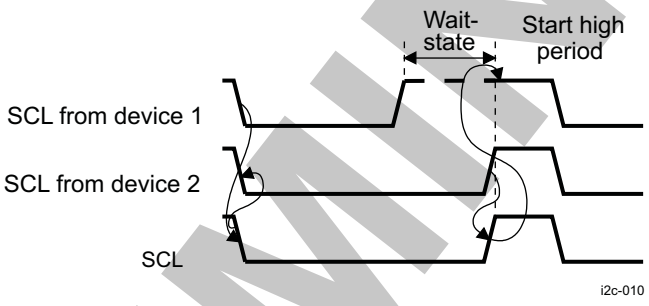
then held low by the device with the longest low period, while the other devices that finish their low periods must wait for the clock line to be released before starting their high periods. A synchronized signal on the clock line is thus obtained, where the slowest device determines the length of the low period and the fastest device determines the length of the high period. If a device pulls down the clock line for a longer time, the result is that all clock generators must enter the WAIT-state. In this way a slave can slow down a fast master and the slow device can create enough time to store a received byte or prepare a byte to be transmitted (clock stretching).

NOTE: In case the SCL or SDA lines are stuck low, a bus clearing operation is supported:

- If the clock line (SCL) is stuck low, the preferential procedure is to reset the bus using the hardware reset signal if your I²C devices have hardware reset inputs. If the I²C devices do not have hardware reset inputs, cycle power to the devices to activate the mandatory internal power-on reset (POR) circuit.
- If the data line (SDA) is stuck low, the master should send nine clock pulses. The device that held the bus low should release it sometime within those nine clocks. If not, then use the hardware reset or cycle power to clear the bus.

Figure 23-10 shows clock synchronization.

Figure 23-10. HS I²C Clock Generators Synchronization



23.1.2.1.3.11 HS I²C External Clock Configuration

Each multimaster HS I²C controller is clocked with an independent functional clock (I2C*i*_FCLK) and an interface clock (I2C*i*_ICLK) for interfacing with the L4_PER interconnect. These clocks are provided by the APE PRCM module for I2C*i* (where *i* = 1, 2, 3, 4, 5).

The SYS_CLK clock provided by the clock generator of the PRCM module is connected to the functional and interface clocks of the HS I²C controller. For detailed information about the module clocking, see Section 3.6 *Clock Management Functional Description, in* Section 3.1.1, *Power, Reset, and Clock Management*.

The functional clock is processed by a prescaler block to produce the internal sampling clock. This clock is generated by the I²C prescaler block. The prescaler block consists of the I2C*i*.I2C_PSC[7:0] PSC bit field (where *i* = 1, 2, 3, 4, 5) that is used to divide down the functional clock to obtain an internal sampling clock with a frequency value of I2C*i*_FCLK/(I2C*i*.I2C_PSC[7:0] PSC bit field value + 1, where *i* = 1, 2, 3, 4, 5).

23.1.2.2 HS I²C for Communication With Power Chip(s)

The device contains additional sixth I²C for SmartReflex1.5™ voltage control. Figure 23-11 shows a typical connection between the SmartReflex1.5™ and external power chip using I2C interface. For more information about communicationg with power chips through I2C interface, see Section 3.1.1, *Power, Reset, and Clock Management.*

Figure 23-11 shows a typical connection with power chip using the I2C interface.

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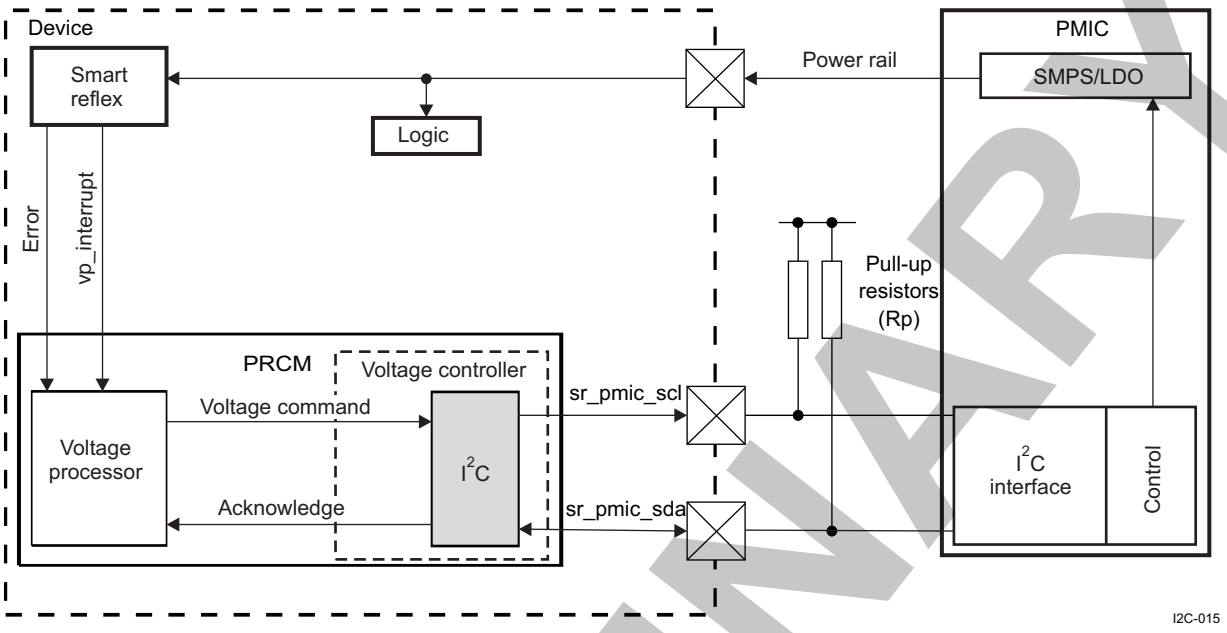
Figure 23-11. HS I²C and Typical Connection Between the HS I²C and Power Chip(s)



23.1.2.2.1 HS I²C Typical Connections Protocol and Data Format for SR I2C

23.1.2.2.1.1 Serial Data Format for SR I2C

Serial data format for Smart Reflex I2C controller is the same as described in Section 23.1.2.1.3.1

23.1.2.2.1.2 SR I2C Data Validity

Data validity is the same as described in Section 23.1.2.1.3.2

23.1.2.2.1.3 Start and Stop Conditions

Start and Stop conditions for SR I2C are the same as described in Section 23.1.2.1.3.3

23.1.2.2.1.4 HS I²C Addressing for SR I²C

The master transmitter SR I2C controller supports only the 7-bit addressing mode. For each frame, the master writes the 8-bit value (DATA) in the register specified by the 8-bit register address (RA) of the slave addressed by the slave address (SA).

The following figure shows the SR I²C frame types for F/S and HS mode.

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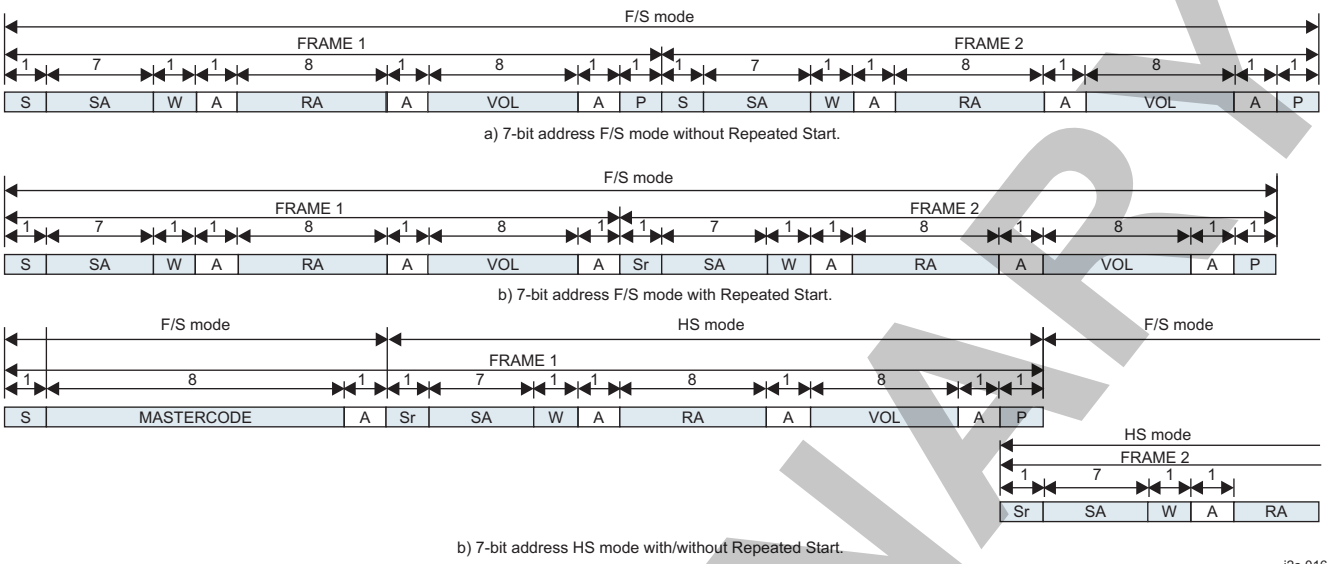
Figure 23-12. SR I2C Frame Types



a) 7-bit address F/S mode without Repeated Start.

b) 7-bit address F/S mode with Repeated Start.

b) 7-bit address HS mode with/without Repeated Start.

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23.1.3 HS I2C Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-13 shows the integration of the five HS I2C controllers in the device.

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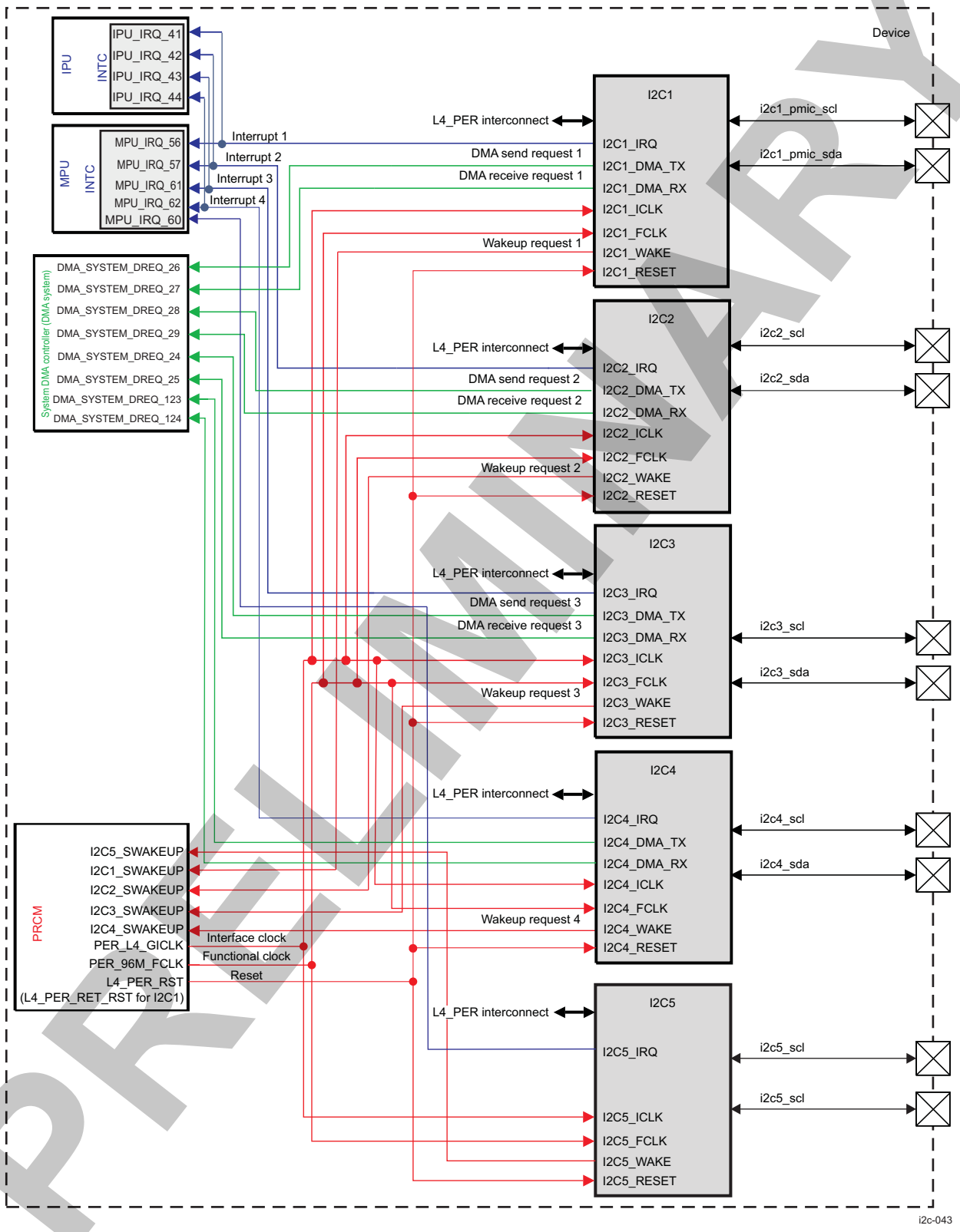
Figure 23-13. HS I²C Integration



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NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.2, *Power Management Functional Description*, in Section 3.1.1, *Power, Reset, and Clock Management*.

Table 23-2 through Table 23-4 summarize the integration of the module in the device.

Table 23-2. HS I²C Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
I2C1	PD_L4_PER	L4_PER
I2C2	PD_L4_PER	L4_PER
I2C3	PD_L4_PER	L4_PER
I2C4	PD_L4_PER	L4_PER
I2C5	PD_L4_PER	L4_PER

Table 23-3. HS I²C Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
I2C1	I2C1_ICLK	PER_L4_GICLK	PRCM	I2C1 interface clock
	I2C1_FCLK	PER_96M_GFCLK	PRCM	I2C1 functional clock
I2C2	I2C2_ICLK	L4PER_L4_GICLK	PRCM	I2C2 interface clock
	I2C2_FCLK	PER_96M_GFCLK	PRCM	I2C2 functional clock
I2C3	I2C3_ICLK	L4PER_L4_GICLK	PRCM	I2C3 interface clock
	I2C3_FCLK	PER_96M_GFCLK	PRCM	I2C3 functional clock
I2C4	I2C4_ICLK	L4PER_L4_GICLK	PRCM	I2C4 interface clock
	I2C4_FCLK	PER_96M_GFCLK	PRCM	I2C4 functional clock
I2C5	I2C5_ICLK	L4PER_L4_GICLK	PRCM	I2C5 interface clock
	I2C5_FCLK	PER_96M_GFCLK	PRCM	I2C5 functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
I2C1	I2C1_RESET	L4_PER_RET_RST	PRCM	I2C1 reset
I2C2	I2C2_RESET	L4_PER_RST	PRCM	I2C2 reset
I2C3	I2C3_RESET	L4_PER_RST	PRCM	I2C3 reset
I2C4	I2C4_RESET	L4_PER_RST	PRCM	I2C4 reset
I2C5	I2C5_RESET	L4_PER_RST	PRCM	I2C5 reset

Table 23-4. HS I²C Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
I2C1	I2C1_IRQ	MPU_IRQ_56	MPU	I2C1 interrupt request
	I2C1_IRQ	IPU_IRQ_41	IPU	I2C1 interrupt request
I2C2	I2C2_IRQ	MPU_IRQ_57	MPU	I2C2 interrupt request
	I2C2_IRQ	IPU_IRQ_42	IPU	I2C2 interrupt request
I2C3	I2C3_IRQ	MPU_IRQ_61	MPU	I2C3 interrupt request
	I2C3_IRQ	IPU_IRQ_43	IPU	I2C3 interrupt request
I2C4	I2C4_IRQ	MPU_IRQ_62	MPU	I2C4 interrupt request
	I2C4_IRQ	IPU_IRQ_44	IPU	I2C4 interrupt request

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Table 23-4. HS I²C Hardware Requests (continued)

I2C5	I2C5_IRQ	MPU_IRQ_60	MPU	I2C5 interrupt request
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
I2C1	I2C1_DMA_TX	DMA_SYSTEM_DREQ_26	sDMA	I2C1 DMA transmit request
	I2C1_DMA_RX	DMA_SYSTEM_DREQ_27	sDMA	I2C1 DMA receive request
I2C2	I2C2_DMA_TX	DMA_SYSTEM_DREQ_28	sDMA	I2C2 DMA transmit request
	I2C2_DMA_RX	DMA_SYSTEM_DREQ_29	sDMA	I2C2 DMA receive request
I2C3	I2C3_DMA_TX	DMA_SYSTEM_DREQ_24	sDMA	I2C3 DMA transmit request
	I2C3_DMA_RX	DMA_SYSTEM_DREQ_25	sDMA	I2C3 DMA receive request
I2C4	I2C4_DMA_TX	DMA_SYSTEM_DREQ_123	sDMA	I2C4 DMA transmit request
	I2C4_DMA_RX	DMA_SYSTEM_DREQ_124	sDMA	I2C4 DMA receive request

NOTE:

- For a description of interrupt source, see Table 23-10.
- For a description of DMA source, see Table 23-11.

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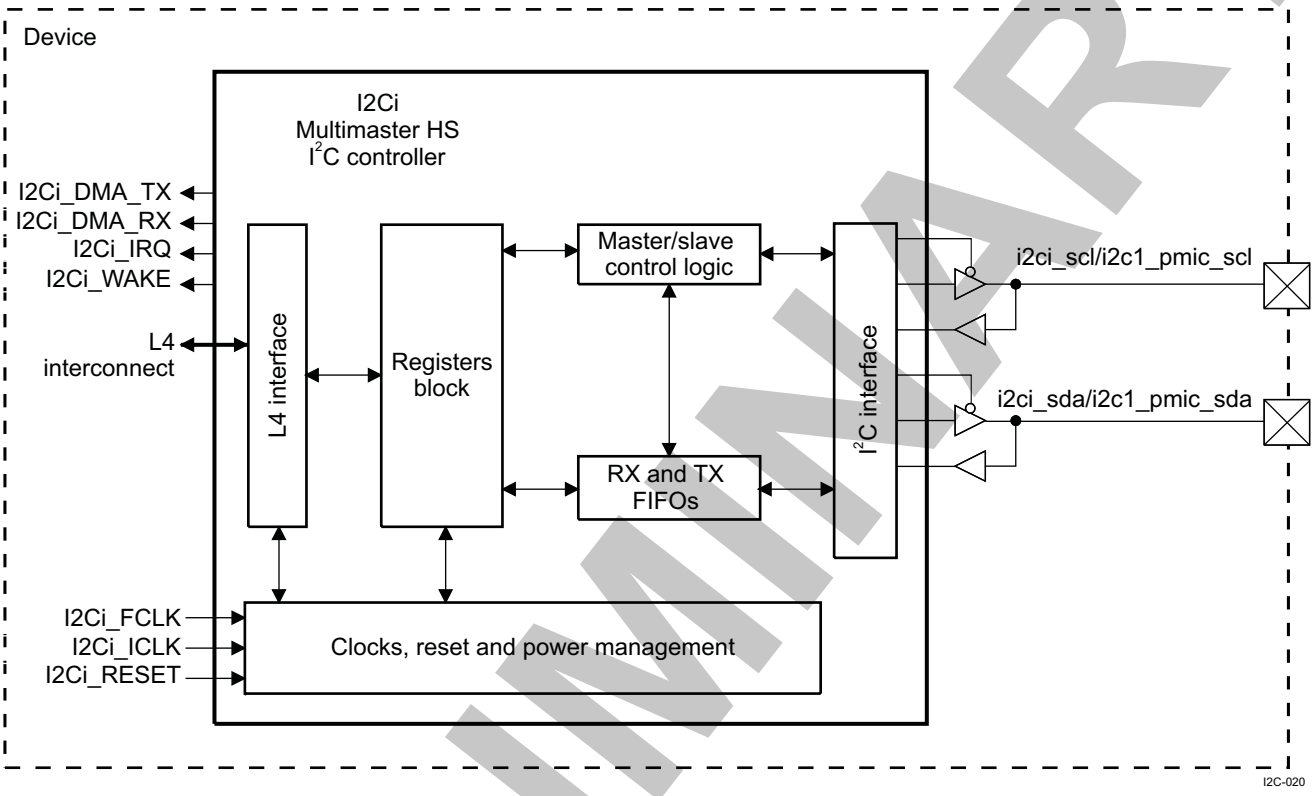
23.1.4 HS I²C Functional Description

23.1.4.1 HS I²C Block Diagram

Figure 23-14 is the multimaster I²C HS controller block diagram.

Figure 23-14. HS I²C Block Diagram



The five multimaster HS I²C controllers can be configured in F/S I²C mode or HS I²C mode. The operation mode is selected by configuring the I2C*i*.I2C_CON[13:12] OPMODE bit field. Table 23-5 lists the available operation modes.

NOTE: The sixth master transmitter HS I²C interface in the power, reset, and clock management (PRCM) could also be configured in High-speed mode.

Table 23-5. HS I²C Operation Mode Selection

Operation Mode	Value of I2C*i*.I2C_CON[13:12] OPMODE Bit Field
F/S I²C	0x0
HS I²C	0x1
Reserved	0x2
Reserved (not used)	0x3

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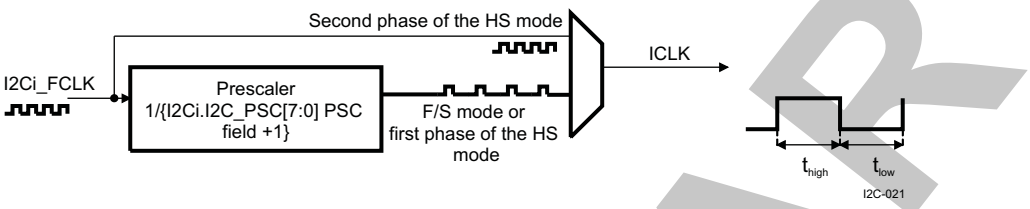
23.1.4.2 HS I²C Clocks

23.1.4.2.1 HS I²C Clocking

Figure 23-15 shows the I²C clock generation of the HS I²C controllers.

Figure 23-15. HS I²C Clock Generation



Each multimaster HS I²C controller uses the I2C*i*_FCLK functional clock in the PRCM module. The internal sampling clock I2C*i*_INTERNAL_CLK is generated by dividing the functional clock by the I2C*i*.I2C_PSC[7:0] PSC bit field value + 1 in F/S mode, or in the first phase of HS mode; or by directly using the functional clock in the second phase of HS mode (prescaler is bypassed).

The low time of the I2C*i*_SCL signal is determined by the I2C*i*.I2C_SCLL[7:0] SCLL bit field in F/S mode and in the first phase of HS mode; or by the I2C*i*.I2C_SCLL[15:8] HSSCLL bit field in the second phase of HS mode.

The high time of the I2C*i*_SCL signal is determined by the I2C*i*.I2C_SCLH[7:0] SCLH bit field in F/S mode and in the first phase of HS mode; or by the I2C*i*.I2C_SCLH[15:8] HSSCLH bit field in the second phase of HS mode.

The low time of the SR I2C signal is determined by the PRM_VC_CFG_I2C_CLK[15:8] SCLL bit field in F/S mode or in the first phase of HS mode; or by the PRM_VC_CFG_I2C_CLK[31:24] HSSCLL bit field in the second phase of HS mode.

The high time of the SR I2C signal is determined by the PRM_VC_CFG_I2C_CLK[7:0] SCLH bit field in F/S mode or in the first phase of HS mode; or by the PRM_VC_CFG_I2C_CLK[23:16] HSSCLH bit field in the second phase of HS mode.

Table 23-6 lists the t_{LOW} and t_{high} values in master mode only (in slave mode, the I²C controller does not generate the I²C clock).

Table 23-6. HS I²C t_{LOW} and t_{high} Values of the I²C Clock

Mode	I2C*i* Clock	t_{LOW}	t_{high}	
			DFILTEREN = 0	DFILTEREN = 1
F/S or HS first phase	I2C*i*_INTERNAL_CLK = I2C*i*_FCLK / (I2C*i*.I2C_PSC[7:0] PSC bit field + 1)	(I2C*i*.I2C_SCLL[7:0] SCLL bit field value + 7) x I2C*i*_INTERNAL_CLK period	(I2C*i*.I2C_SCLH[7:0] SCLH bit field value + 5 + PROP_DELAY0) x I2C*i*_INTERNAL_CLK period	(I2Ci.I2C_SCLH [7:0] SCLH bit filed value + 5 + PROP_DELAY1) x I2Ci_INTERNAL_CLK period
HS second phase	I2C*i*_FCLK	(I2C*i*.I2C_SCLL[15:8] HSSCLL bit field value + 7) x I2C*i*_FCLK period	(I2C*i*.I2C_SCLH[15:8] HSSCLH bit field value + 5 + PROP_DELAY0) x I2C*i*_FCLK period	(I2Ci.I2CSCLL [15:8] HSSCLH bit field value + 5 + PROP_DELAY1) x I2Ci_FCLK period
FS or first phase of HS mode for SR I2C	SR I2C_FCLK	(VC_CFG_I2C_CLK[15:8]SCLL + 1) x SR I2C_FCLK period	(VC_CFG_I2C_CLK [7:0] SCLH + 5 + PROP_DELAY0) xSR I2C_FCLK period	(VC_CFG_I2C_CLK [7:0] SCLH + 5 + PROP_DELAY1) x SR I2C_FCLK period
Second phase of HS mode for SR I2C	SR I2C_FCLK	(VC_CFG_I2C_CLK [31:24] HSSCLL + 1) x SR I2C_FCLK period	(VC_CFG_I2C_CLK [23:16] HSSCLH +5 + PROP_DELAY0) x SR I2C_FCLK period	(VC_CFG_I2C_CLK [23:16] HSSCLH +5 + PROP_DELAY1) x SR I2C_FCLK period

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NOTE: For HS mode, the I2C*i*.I2C_SCLL[15:8] HSSCLL and I2C*i*.I2C_SCLL[7:0] SCLL bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

For HS mode, the I2C*i*.I2C_SCLH[15:8] HSSCLH and I2C*i*.I2C_SCLH[7:0] SCLH bit fields must be programmed (the first phase of an HS transaction is performed at F/S speed).

NOTE: The equations in Table 23-6 give the SCL timing values for SCLL/SCLH/HSSCLL/HSSCLH at HS I²C controller outputs. Actual tlow and thigh periods may vary depending on the board (the load capacitance on the SCL signal). If necessary, any adjustments to the SCLL/SCLH/HSSCLL/HSSCLH values must be determined by measurements of actual SCL signal on the board.

CAUTION

During active mode (the I2C*i*.I2C_CON[15] I2C_EN bit is set to 1), make no changes to the I2C*i*.I2C_SCLL and I2C*i*.I2C_SCLH registers. Changes may result in unpredictable behavior.

NOTE: Each multimaster HS I²C controller can be used with an internal secondary pullup. Pullups can be programmed through the CONTROL_I2C_0[16] I2C1_PMIC_SCL_PULLUPRESX bit or CONTROL_I2C_0[24] I2C1_PMIC_SDA_PULLUPRESX bit for I2C1, the CONTROL_I2C_0[18] I2C2_SCL_PULLUPRESX bit or CONTROL_I2C_0[26] I2C2_SDA_PULLUPRESX bit for I2C2, the CONTROL_I2C_0[20] I2C3_SCL_PULLUPRESX bit or CONTROL_I2C_0[28] I2C3_SDA_PULLUPRESX bit for I2C3, the CONTROL_I2C_0[22] I2C4_SCL_PULLUPRESX bit or CONTROL_I2C_0[30] I2C4_SDA_PULLUPRESX bit for I2C4, and the CONTROL_I2C_0[12] I2C5_SCL_PULLUPRESX bit or CONTROL_I2C_0[14] I2C5_SDA_PULLUPRESX bit for I2C5.

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Table 23-7 lists the register values for obtaining the maximum I²C bit rates and the maximum period of the filtered spikes in F/S mode and HS mode.

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Table 23-7. HS I²C Register Values for Maximum I²C Bit Rates in I²C F/S, I²C HS Modes(1)

	I²C Mode for I2C*i*,			Description	I²C Mode for SmartReflex I2C Fast and High-Speed Mode		
	Standart Mode	**Fast Mode**	**High-Speed Mode**				
I2C*i*_FCLK frequency (MHz)	96					38.4	SYS_CLK clock frequency
I2C *i* .I2C_PSC[7:0] PSC bit field value	**23**	**9**	**1**	Prescaler value for F/S and HS modes	Not accessible by software		
I2C*i*_INTERNAL_CLK frequency (MHz)	4	9.6	96				
I2C *i* .I2C_SCLL[7:0] SCLL bit field value	**13**	**7**	**115**	Value for F/S mode and first phase of HS mode	**PRM_VC_CFG_I2C_CLK[15:8] SCLL** see Section 3.1.1, *Power, Reset, and Clock Management*	**43**	Value for F/S mode and first phase of HS mode
I2C *i* .I2C_SCLH[7:0] SCLH bit field value	**15**	**5**	**113**	Value for F/S mode and first phase of HS mode	**PRM_VC_CFG_I2C_CLK[7:0] SCLH** see Section 3.1.1, *Power, Reset, and Clock Management*	**41**	Value for F/S mode and first phase of HS mode
Maximum bit rate (Mbps)	0.1	0.4	0.4	F/S mode and first phase in HS mode maximum bit rate		0.4	F/S mode and first phase in HS mode maximum bit rate
Maximum filter period (ns)	250	104.2	10			50	
I2C *i* .I2C_SCLL[15:8] HSSCLL bit field value			**12**	Values for second phase of HS mode	**PRM_VC_CFG_I2C_CLK[31:24] HSSCLL** see Section 3.1.1, *Power, Reset, and Clock Management*	**14**	Values for second phase of HS mode
I2C *i* .I2C_SCLH[15:8] HSSCLH bit field value			**5**	Values for second phase of HS mode	**PRM_VC_CFG_I2C_CLK[23:16] HSSCLH** see Section 3.1.1, *Power, Reset, and Clock Management*	**0**	Values for second phase of HS mode
HS mode maximum bit rate (Mbps)			3.31	HS mode maximum bit rate		3.2	HS mode maximum bit rate according to the corresponding SYS_CLK clock frequency
Maximum filter period (ns)			10			10	

(1) Programmable fields are in bold.

NOTE: There is only one clock domain for Voltage Controller module. PRM module can provide only one clock signal(system clock signal) which is used for SR I2C FS and HS mode. The clock frequencies are only some examples.

NOTE: This table presents informative values only for the configuration parameters and the I²C bus performance obtained according to these values. The delays added by the analog pads are not considered in these figures.For further information regarding the delays added by the pads, refer to the device Data Manual, available through your TI representative.

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NOTE: Fof I2Ci (where i=1, 2, 3, 4, 5)

I2Ci_INTERNAL_CLK freq = SYS_CLK / (PSC +1)

F/S filter period = 1 / I2Ci_INTERNAL_CLK

HS filter period = 1 / SYS_CLK freq

If DFILTEREN bit = 0:

HS bit rate = I2Ci_FCLK freq / (HSSCLL+7 + HSSCLH+5 + PROP_DELAY0)

FS bit rate = I2Ci_INTERNAL_CLK / (SCLL+7 + SCLH+5 + PROP_DELAY0)

- If DFILTEREN bit = 1:

HS bit rate = I2Ci_FCLK freq / (HSSCLL+7 + HSSCLH+5 + PROP_DELAY1)

FS bit rate = I2Ci_INTERNAL_CLK / (SCLL+7 + SCLH+5 + PROP_DELAY1)

For SR I2C (SmartReflex I2C) :

SR I2C_FCLK freq = SYS_CLK freq

HS/FS filter period = 1 / SR I2C_FCLK freq

- If DFILTEREN bit = 0:

HS bit rate = SR I2C_FCLK freq / (HSSCLL+1 + HSSCLH+5 +PROP_DELAY0)

FS bit rate = SR I2C_FCLK freq / (SCLL+1 + SCLH+5 + PROP_DELAY0)

- If DFILTEREN bit = 1:

HS bit rate = SR I2C_FCLK freq / (HSSCLL+1 + HSSCLH+5 + PROP_DELAY1)

FS bit rate = SR I2C_FCLK freq / (SCLL+1 + SCLH+5 + PROP_DELAY1)

DFILTEREN refers to VC_CFG_I2C_MODE [6] DFILTEREN bit field. PROP_DELAYx (x= 0 or 1) represents frequency normalized IO low to high propagation delay.

PROP_DELAY0= 0 or 3 (values for bit rate max/min range)

PROP_DELAY1= 1 or 4 (values for bit rate max/min range)

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23.1.4.2.2 HS I²C Automatic Blocking of the I²C Clock Feature

This feature offers the possibility for the LH to command the blocking of the I²C clock after the slave addressing phase, when the I²C controller is addressed by an external master device using a certain Own Address.

The release of the I²C clock can be performed independently for each Own Address (I2C*i*.I2C_OA, where *i* = 1, 2, 3, 4, 5 and I2C*i*.I2C_OAx registers) by deasserting the corresponding bit in the I2C*i*.I2C_SBLOCK register.

23.1.4.3 HS I²C Software Reset

Each multimaster HS I²C controller supports the software reset by accessing the I2C*i*.I2C_SYSC[1] SRST bit (1: reset; 0: normal mode).

The software reset status can be checked by accessing the I2C*i*.I2C_SYSS[0] RDONE bit (1: reset is done; 0: reset is ongoing).

To do a software reset, the following steps must be done:

1. Ensure that the module is disabled (clear the I2C*i*.I2C_CON[15] I2C_EN bit to 0).
2. Set the I2C*i*.I2C_SYSC[1] SRST bit to 1.
3. Enable the module by setting I2C*i*.I2C_CON[15] I2C_EN bit to 1.
4. Check the I2C*i*.I2C_SYSS[0] RDONE bit until it is set to 1 to indicate the software reset is complete.

NOTE: The I2C*i*.I2C_CON[15] I2C_EN bit can hold the functional clock domain of the multimaster HS I²C controller in reset after the device reset has been released. When the system bus reset is removed, this bit remains cleared. The functional part of the I²C controller is held in reset state while this bit is 0, and all configuration registers can be accessed.

The I2C*i*.I2C_CON[15] I2C_EN bit must be set to 1 to enable the functional part of the I²C controller.

The I2C*i*.I2C_SYSS[0] RDONE bit is asserted only after the module is enabled by setting the I2C*i*.I2C_CON[15] I2C_EN bit to 1.

23.1.4.4 HS I²C Power Management

Table 23-8 describes power-management features available for the multimaster HS I²C controllers.

NOTE:

- For information about source clock gating and sleep/wake-up transitions description, see Section 3.1.1.1.2, *Module Level Clock Management*, in Section 3.1.1, *Power, Reset, and Clock Management*.
- For descriptions of EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.1.1.1.2, *Module Level Clock Management*, in Section 3.1.1, *Power, Reset, and Clock Management*.

Table 23-8. HS I²C Local Power-Management Features

Feature	Registers	Description
Clock auto gating	I2C*i*.I2C_SYSC[0] AUTOIDLE	This bit allows a local power optimization inside the module.
Slave idle modes	I2C*i*.I2C_SYSC[4:3] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available.
Clock activity	I2C*i*.I2C_SYSC[9:8] CLOCKACTIVITY	For configuration details, see Table 23-9.
Global wake-up enable	I2C*i*.I2C_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.

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NOTE: The voltage controllers, in which the HS I²C controller is implemented, have no idle request/acknowledge mechanism. The idle modes for the voltage controllers are directly managed by the PRCM module.

Table 23-9. HS I²C Clock Activity Settings

I2C*i*.I2C_SYSC[9:8] CLOCKACTIVITY	Clock State When Module is in IDLE State		Features Available/Unavailable When Module is in IDLE State
	I2C*i*_ICLK	I2C*i*_ FCLK	
00	OFF	OFF	Both clocks are disabled.
10	OFF	ON	Interface clock is disabled; functional clock is enabled
01	ON	OFF	Functional clock is disabled; interface clock is enabled
11	ON	ON	Both clocks are enabled.

CAUTION

The PRCM module has no hardware means of reading the settings of CLOCKACTIVITY. Thus, software must ensure consistent programming between the I²C CLOCKACTIVITY and I²C clock PRCM control bits. For a description of the ClockActivity feature, see Section 3.1.1.1.2, *Module Level Clock Management* in Section 3.1.1, *Power, Reset, and Clock Management*.

23.1.4.5 HS I²C Interrupt Requests

Table 23-10 lists the event flags, and their mask, that can cause module interrupts.

Table 23-10. HS I²C Events

Event Flag	Event Mask	Event Unmask	Map to	Description
I2C*i*.I2C_IRQSTATUS[0] AL	I2C*i*.I2C_IRQENABLE_SET[0] AL_IE	I2C*i*.I2C_IRQENABLE_CLR[0] AL_IE	I2C*i*_IRQ	Arbitration lost IRQ enabled status. This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to the microprocessor unit (MPU) subsystem. During reads, it always returns 0.
I2C*i*.I2C_IRQSTATUS[1] NACK	I2C*i*.I2C_IRQENABLE_SET[1] NACK_IE	I2C*i*.I2C_IRQENABLE_CLR[1] NACK_IE	I2C*i*_IRQ	No acknowledgement IRQ enabled status. Bit is set when No Acknowledge is received, an interrupt is signaled to the MPU subsystem. Write 1 to clear this bit.
I2C*i*.I2C_IRQSTATUS[2] ARDY	I2C*i*.I2C_IRQENABLE_SET[2] ARDY_IE	I2C*i*.I2C_IRQENABLE_CLR[2] ARDY_IE	I2C*i*_IRQ	Register access ready IRQ enabled status. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to the MPU subsystem. Write 1 to clear.
I2C*i*.I2C_IRQSTATUS[3] RRDY	I2C*i*.I2C_IRQENABLE_SET[3] RRDY_IE	I2C*i*.I2C_IRQENABLE_CLR[3] RRDY_IE	I2C*i*_IRQ	Receive data ready IRQ enabled status. Set to 1 by core when receiver mode, a new data can be read. When set to 1 by core, an interrupt is signaled to the MPU subsystem. Write 1 to clear.

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Table 23-10. HS I²C Events (continued)

Event Flag	Event Mask	Event Unmask	Map to	Description
I2C*i*.I2C_IRQSTATUS[4] XRDY	I2C*i*.I2C_IRQENABLE_SET[4] XRDY_IE	I2C*i*.I2C_IRQENABLE_CLR[4] XRDY_IE	I2C*i*_IRQ	Transmit data ready IRQ enabled status. Set to 1 by core when transmitter and when new data is requested. When set to 1 by core, an interrupt is signaled to the MPU subsystem. Write 1 to clear.
I2C*i*.I2C_IRQSTATUS[5] GC	I2C*i*.I2C_IRQENABLE_SET[5] GC_IE	I2C*i*.I2C_IRQENABLE_CLR[5] GC_IE	I2C*i*_IRQ	General call IRQ enabled status. Set to 1 by core when General call address detected and interrupt signaled to the MPU subsystem. Write 1 to clear.
I2C*i*.I2C_IRQSTATUS[6] STC	I2C*i*.I2C_IRQENABLE_SET[6] STC_IE	I2C*i*.I2C_IRQENABLE_CLR[6] STC_IE	I2C*i*_IRQ	Start condition IRQ enabled status.
I2C*i*.I2C_IRQSTATUS[7] AERR	I2C*i*.I2C_IRQENABLE_SET[7] AERR_IE	I2C*i*.I2C_IRQENABLE_CLR[7] AERR_IE	I2C*i*_IRQ	Access Error IRQ enabled status.
I2C*i*.I2C_IRQSTATUS[8] BF	I2C*i*.I2C_IRQENABLE_SET[8] BF_IE	I2C*i*.I2C_IRQENABLE_CLR[8] BF_IE	I2C*i*_IRQ	Access Error IRQ enabled status.
I2C*i*.I2C_IRQSTATUS[9] AAS	I2C*i*.I2C_IRQENABLE_SET[9] AAS_IE	I2C*i*.I2C_IRQENABLE_CLR[9] AAS_IE	I2C*i*_IRQ	Address recognized as slave IRQ enabled status.
I2C*i*.I2C_IRQSTATUS[10] XUDF	I2C*i*.I2C_IRQENABLE_SET [10] XUDF_IE	I2C*i*.I2C_IRQENABLE_CLR[10] XUDF_IE	I2C*i*_IRQ	Transmit underflow enabled status. Writing into this bit has no effect.
I2C*i*.I2C_IRQSTATUS[11] ROVR	I2C*i*.I2C_IRQENABLE_SET [11] ROVR_IE	I2C*i*.I2C_IRQENABLE_CLR[11] ROVR_IE	I2C*i*_IRQ	Receive overrun enabled status. Writing into this bit has no effect.
I2C*i*.I2C_IRQSTATUS[12] BB	Reserved	Reserved	I2C*i*_IRQ	Bus busy status.
I2C*i*.I2C_IRQSTATUS[13] RDR	I2C*i*.I2C_IRQENABLE_SET [13] RDR_IE	I2C*i*.I2C_IRQENABLE_CLR[13] RDR_IE	I2C*i*_IRQ	Receive draining IRQ enabled status.
I2C*i*.I2C_IRQSTATUS[14] XDR	I2C*i*.I2C_IRQENABLE_SET [14] XDR_IE	I2C*i*.I2C_IRQENABLE_CLR[14] XDR_IE	I2C*i*_IRQ	Transmit draining IRQ enabled status.

23.1.4.6 HS I²C DMA Requests

Each multimaster HS I²C controller can generate two DMA requests to the system DMA (sDMA) controller. Table 23-11 lists the DMA requests with mapping on the sDMA controller. For information about DMA generation, see Section 23.1.4.8.3, *HS I²C FIFO DMA Mode (I²C Mode Only)*.

Table 23-11. HS I²C DMA Requests

Name	Source	Destination	Description
I2C1_DMA_TX	I2C1	DMA_SYSTEM_DREQ_26	I2C1 DMA write request to inform the sDMA to write new data in the I2C1.I2C_DATA[7:0] register
I2C1_DMA_RX	I2C1	DMA_SYSTEM_DREQ_27	I2C1 DMA read request to inform the sDMA to read the data in the I2C1.I2C_DATA[7:0] register
I2C2_DMA_TX	I2C2	DMA_SYSTEM_DREQ_28	I2C2 DMA write request to inform the sDMA to write new data in the I2C2.I2C_DATA[7:0] register
I2C2_DMA_RX	I2C2	DMA_SYSTEM_DREQ_29	I2C2 DMA read request to inform the sDMA to read the data in the I2C2.I2C_DATA[7:0] register
I2C3_DMA_TX	I2C3	DMA_SYSTEM_DREQ_24	I2C3 DMA write request to inform the sDMA to write new data in the I2C3.I2C_DATA[7:0] register
I2C3_DMA_RX	I2C3	DMA_SYSTEM_DREQ_25	I2C3 DMA read request to inform the sDMA to read the data in the I2C3.I2C_DATA[7:0] register
I2C4_DMA_TX	I2C4	DMA_SYSTEM_DREQ_123	I2C4 DMA write request to inform the sDMA to write new data in the I2C4.I2C_DATA[7:0] register
I2C4_DMA_RX	I2C4	DMA_SYSTEM_DREQ_124	I2C4 DMA read request to inform the sDMA to read the data in the I2C4.I2C_DATA[7:0] register

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NOTE: The HS I²C controller I2C5 does not generate any DMA requests.

23.1.4.7 HS I²C Programmable Multislave Channel Feature

This feature allows each multimaster HS I²C controller to be addressed using four separate Own Addresses configured in the I2C*i*.I2C_OA and I2C*i*.I2C_OAx registers (where *i* = 1, 2, 3). An additional register (I2C*i*.I2C_ACTOA) is used to indicate to the LH which address is used by the external master to communicate with the I²C controller.

Each Own Address can be independently configured in 7-bit or 10-bit mode by setting the corresponding bit (I2C*i*.I2C_CON[7] XOA, I2C*i*.I2C_CON[6] XOA1, I2C*i*.I2C_CON[5] XOA2, or I2C*i*.I2C_CON[4] XOA3).

23.1.4.8 HS I²C FIFO Management

Each multimaster HS I²C controller implements two internal 8-bit FIFOs, the RX and TX FIFOs.

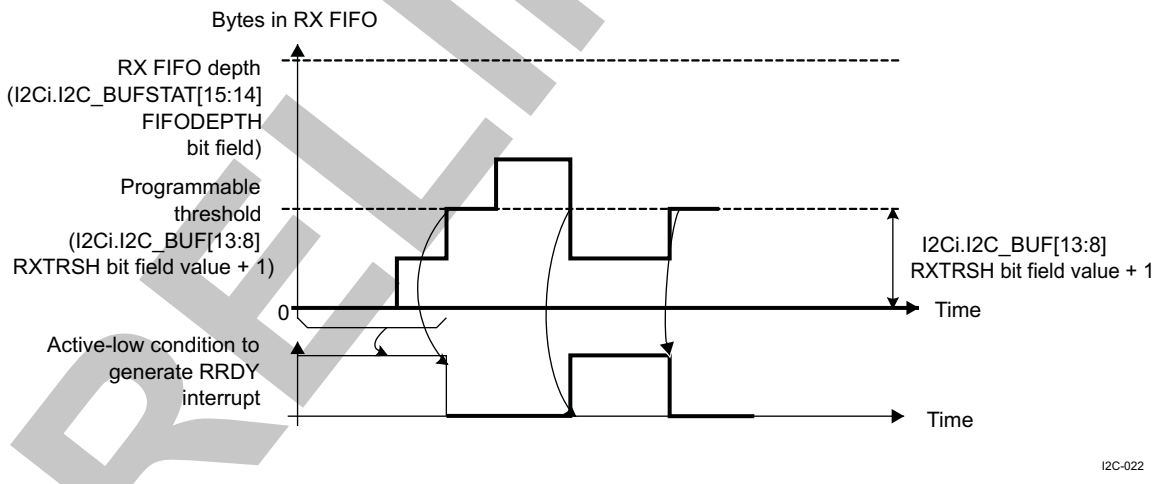
The depth of the RX and TX FIFOs can be checked by reading the I2C*i*.I2C_BUFSTAT[15:14] FIFODEPTH bit field (0x0: 8 bytes, 0x1: 16 bytes, 0x2: 32 bytes, and 0x3: 64 bytes).

23.1.4.8.1 HS I²C FIFO Interrupt Mode

In FIFO interrupt mode (relevant interrupts enabled by the I2C*i*.I2C_IRQENABLE_SET register), an interrupt signal informs the processor of the receiver and transmitter status. These interrupts are raised when the RX/TX FIFO thresholds (defined by the I2C*i*.I2C_BUF[13:8] RTRSH bit field value + 1 for the RX FIFO or the I2C*i*.I2C_BUF[5:0] XTRSH bit field value + 1 for the TX FIFO) are reached; the interrupt signals instruct the LH to transfer data to the destination (from the I²C controller in receive mode and/or from any source to the I²C controller FIFO in transmit mode).

Figure 23-16 and Figure 23-17 show receive and transmit operations, respectively, from a FIFO management point of view.

Figure 23-16. HS I²C Receive FIFO Interrupt Request Generation



In Figure 23-16, the RRDY interrupt condition shows that the condition for generating an RRDY interrupt is achieved. The interrupt request is generated when this signal is active, and it can be cleared only by the LH by writing 1 in the corresponding bit. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In receive mode, an RRDY interrupt is generated as soon as the FIFO reaches its receive threshold (I2C*i*.I2C_BUF[13:8] RTRSH bit field value + 1). The interrupt can be deasserted only when the LH has handled enough bytes to make the number of bytes in the RX FIFO lower than the programmed threshold. For each interrupt, the LH can be configured to read a number of bytes equal to the value of the RX FIFO threshold.

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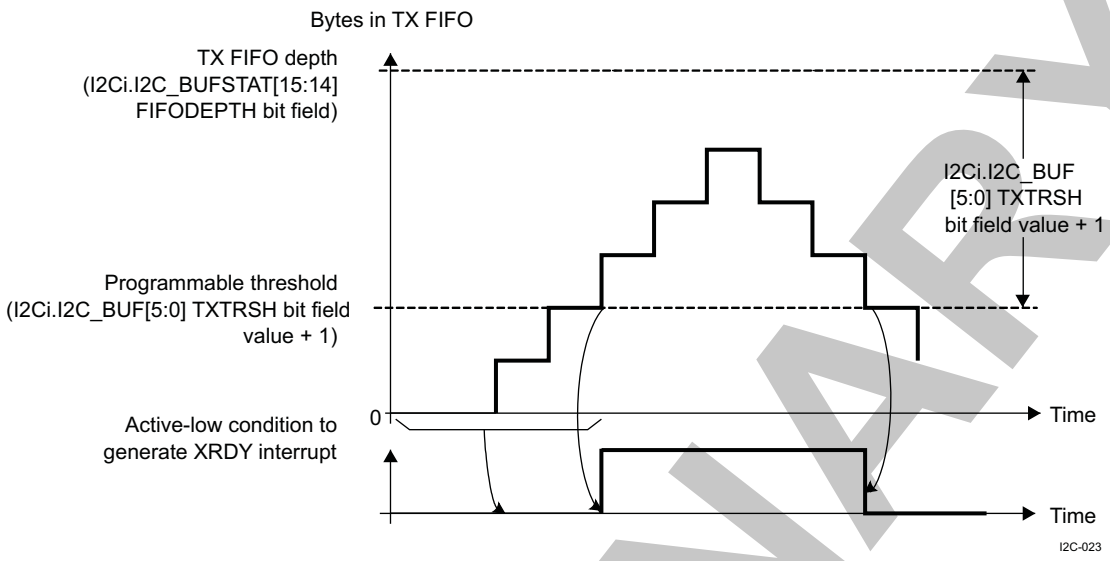
Figure 23-17. HS I²C Transmit FIFO Interrupt Request Generation



In Figure 23-17, the XRDY interrupt condition shows that the condition for generating an XRDY interrupt is achieved. The interrupt request is generated when TX FIFO is empty or when the TX FIFO threshold is not reached, and the LH can clear the XRDY status bit by setting the I2C*i*.I2C_IRQENABLE_CLR [4] XRDY_IE bit to 1 after transmitting the configured number of bytes. If the condition is still present after clearing the previous interrupt, another interrupt request is generated.

In interrupt mode, the module offers two options for the LH application to handle the interrupts:

- When detecting an interrupt request (XRDY or RRDY type), the LH can write/read 1 data byte to/from the TX/RX FIFO and then clear the interrupt. The module reasserts the interrupt until the interrupt condition is not met.
- When detecting an interrupt request (XRDY or RRDY type), the LH can be programmed to write/read the amount of data bytes specified by the corresponding FIFO threshold (I2C_BUF[5:0] TXTRSH + 1 or I2C_BUF[5:0] RXTRSH + 1). In this case, the interrupt condition is cleared and the next interrupt is asserted again when the XRDY or RRDY condition is met again.

If the second-interrupt-serving approach is used, an additional mechanism (draining feature) is implemented for cases where the transfer length is not a multiple of the FIFO threshold value (see Section 23.1.4.8.4, *Draining Feature [I²C Mode Only]*).

NOTE: In slave transmit mode (the I2C*i*.I2C_CON[10] MST bit is cleared and the I2C*i*.I2C_CON[9] TRX bit is set to 1), the draining feature must not be used, because the transfer length is not known at configuration time, and the external master can end the transfer at any point by not acknowledging 1 data byte. If the draining feature is used in slave transmit mode, data can remain in the TX FIFO without being transmitted over the I²C bus. In this case, the TX FIFO must be cleared by setting the I2C*i*.I2C_BUF[6] TXFIFO_CLR bit.

23.1.4.8.2 HS I²C FIFO Polling Mode

In FIFO polling mode (the I2C*i*.I2C_IRQENABLE_SET [4] XRDY_IE and I2C*i*.I2C_IRQENABLE_SET [3] RRDY_IE bits are disabled), the status of the module (receiver or transmitter) can be checked by polling the I2C*i*.I2C_IRQSTATUS_RAW [4] XRDY and the I2C*i*.I2C_IRQSTATUS_RAW [3] RRDY bits (the I2C*i*.I2C_IRQSTATUS_RAW [13] RDR and I2C*i*.I2C_IRQSTATUS_RAW [14] XDR bits can also be polled if the draining feature is enabled). The I2C*i*.I2C_IRQSTATUS_RAW [4] XRDY and I2C*i*.I2C_IRQSTATUS_RAW [3] RRDY bits accurately reflect the interrupt conditions described in the discussion of FIFO interrupt mode.

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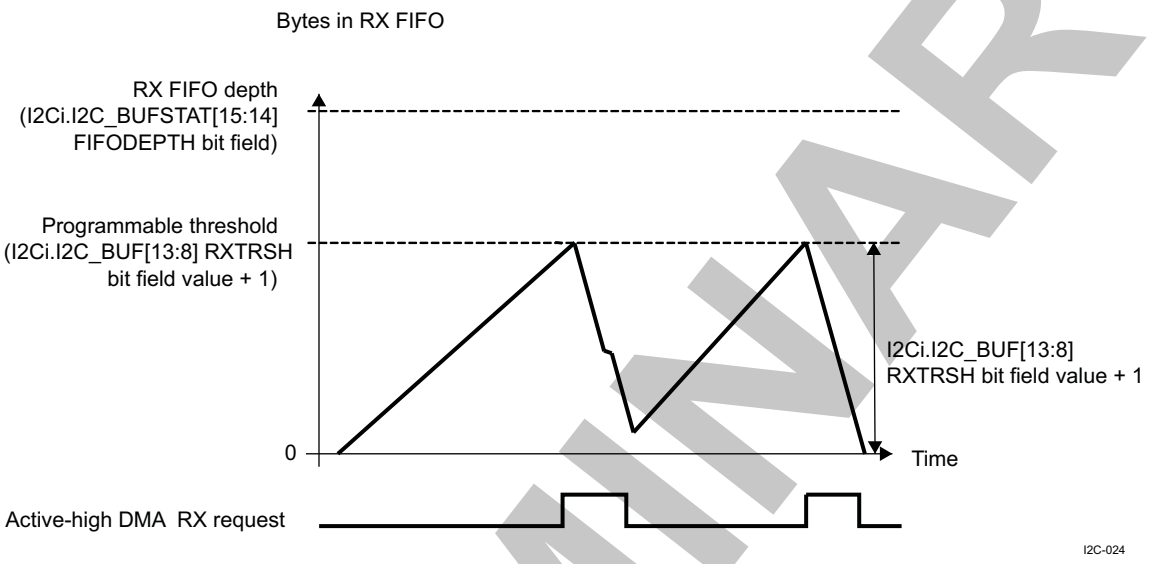
23.1.4.8.3 HS I²C FIFO DMA Mode

In receive mode, a DMA request is generated by the I2C*i*_DMA_RX signal as soon as the RX FIFO exceeds its threshold level (the I2C*i*.I2C_BUF[13:8] RTRSH bit field value + 1). This request is deasserted when the number of bytes defined by the threshold level is read by the DMA controller.

Figure 23-18 shows the DMA request generation in receive mode.

Figure 23-18. HS I²C Receive FIFO DMA Request Generation



In transmit mode, a DMA request is automatically asserted by the I2C*i*_DMA_TX signal when the TX FIFO is empty. This request is deasserted when the number of bytes (the I2C*i*.I2C_BUF[5:0] XTRSH bit field value + 1) is written in the FIFO by the sDMA controller. If an insufficient number of bytes is written, the DMA request remains active. Figure 23-19 and Figure 23-20 show the DMA TX transfers with different values for the I2C*i*.I2C_BUF[5:0] XTRSH bit field.

Figure 23-19. HS I²C Transmit FIFO Request Generation (High Threshold)

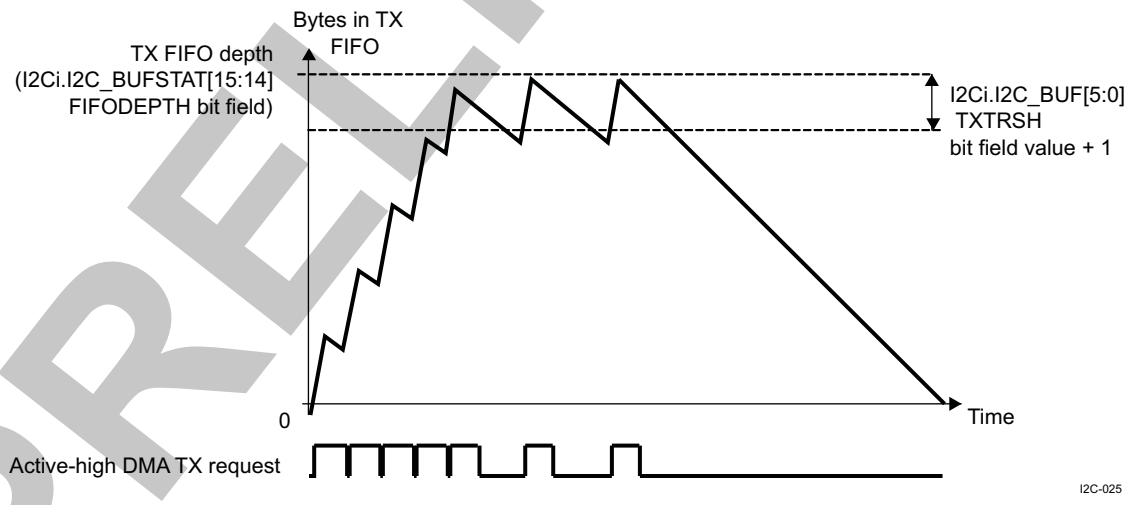


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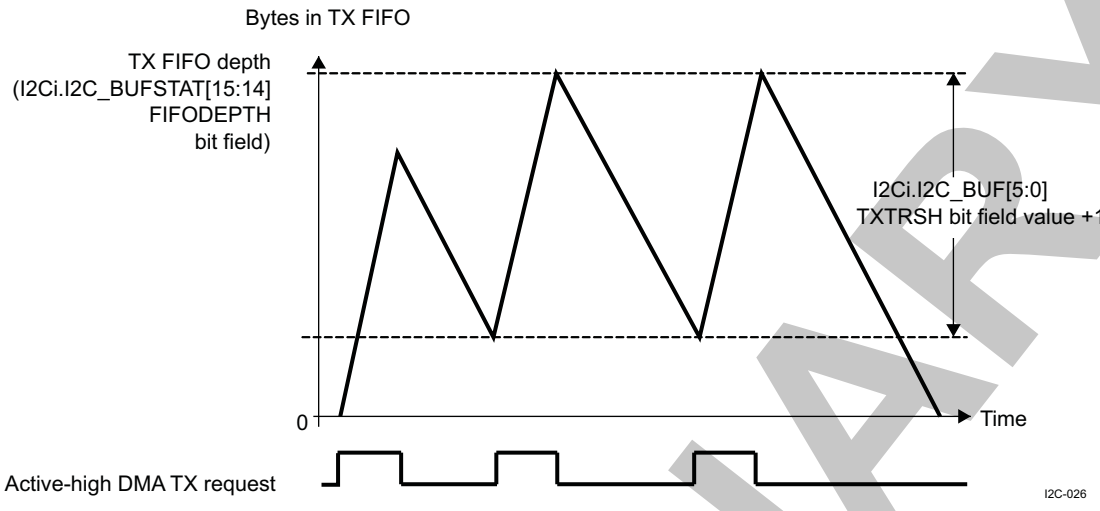
Figure 23-20. HS I²C Transmit FIFO Request Generation (Low Threshold)



The I2C module provides the possibility to the user to clear the RX or TX FIFO, by setting the I2Ci.I2C_BUF[14]RXFIFO_CLR and I2Ci.I2C_BUF[6]TXFIFO_CLR registers, which act like software reset for the FIFOs. In DMA mode, these bits will also reset the DMA state machines.

The FIFO clearing feature can be used when the following conditions are met:

1. The module is configured as a transmitter
2. The external receiver responds with a NACK in the middle of the transfer
3. There is still data in TX FIFO waiting to be transferred

23.1.4.8.4 HS I²C Draining Feature

The draining feature is implemented to handle the end of a transfer whose length is not a multiple of the FIFO threshold values (the I2C*i*.I2C_BUF[13:8] RTRSH bit field value + 1 for the RX threshold and the I2C*i*.I2C_BUF[5:0] XTRSH field value + 1 for the TX threshold). It can also transfer the remaining number of bytes (because the threshold is not reached).

This feature prevents the LH or the sDMA controller from trying more FIFO accesses than necessary (for example, to generate at the end of a transfer a DMA RX request having fewer bytes in the FIFO than the configured DMA transfer length). Otherwise, an AERR interrupt is generated by the I2C*i*.I2C_IRQSTATUS_RAW [7] AERR bit.

The draining mechanism generates an interrupt using the I2C*i*.I2C_IRQSTATUS_RAW [13] RDR or I2C*i*.I2C_IRQSTATUS_RAW [14] XDR bit at the end of the transfer, informing the LH that it must check the amount of data left to be transferred (the I2C*i*.I2C_BUFSTAT[13:8] RXSTAT or I2C*i*.I2C_BUFSTAT[5:0] TXSTAT bit fields) and enable the draining feature of the DMA controller by reconfiguring the DMA transfer length according to this value (when the DMA mode is enabled) or perform only the required number of data accesses (when the DMA mode is disabled).

In receive mode (master or slave), if the RX FIFO threshold (the I2C*i*.I2C_BUF[13:8] RTRSH bit field value + 1) is not reached, but the transfer ends on the I²C bus and data remains in the RX FIFO (less than the threshold), the receive draining interrupt (the I2C*i*.I2C_IRQSTATUS_RAW [13] RDR bit) is asserted to inform the LH that it can read the amount of data in the RX FIFO (the I2C*i*.I2C_BUFSTAT[13:8] RXSTAT bit field). The LH performs a number of data read accesses equal to the I2C*i*.I2C_BUFSTAT[13:8] RXSTAT bit field (interrupt or polling mode), or reconfigures the sDMA controller with the required value to drain the FIFO.

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In master transmit mode, if the TX FIFO threshold (the I2C*i*.I2C_BUF[5:0] TXTRSH bit field value + 1) is not reached, but the amount of data remaining to be written in the TX FIFO is less than the threshold, the transmit draining interrupt (the I2C*i*.I2C_IRQSTATUS_RAW [14] XDR bit) is asserted to inform the LH that it can read the amount of data remaining to be written in the TX FIFO (the I2C*i*.I2C_BUFSTAT[5:0] TXSTAT bit field). The LH must write the required number of data bytes specified by the I2C*i*.I2C_BUFSTAT[5:0] TXSTAT bit field value or reconfigure the sDMA controller with the value required to transfer the last bytes to the FIFO.

In master mode, the LH can alternately not check the values of the I2C*i*.I2C_BUFSTAT[5:0] TXSTAT and I2C*i*.I2C_BUFSTAT[13:8] RXSTAT bit fields, because it can obtain this information internally (by computing the I2C*i*.I2C_CNT[15:0] DATACOUNT bit field value modulo I2C*i*.I2C_BUF[13:8] RXTRSH or I2C*i*.I2C_BUF[5:0] TXTRSH).

By default, the draining feature is disabled; it can be enabled using the I2C*i*.I2C_IRQENABLE_SET [14] XDR_IE or I2C*i*.I2C_IRQENABLE_SET [13] RDR_IE bits (default disabled) only for transfers with lengths not equal to the threshold values (I2C*i*.I2C_BUF[5:0] TXTRSH bit field value + 1 for the TX threshold or the I2C*i*.I2C_BUF[13:8] RXTRSH bit field value + 1 for the RX threshold).

23.1.4.9 HS I²C Noise Filter

The noise filter is used to suppress any noise that is 50 ns or less in case of F/S operation modes, and any noise that is 10 ns or less in case of HS mode operation. The noise filter is always one period of the I2C*i*_INTERNAL_CLK clock. This way, for HS mode operation (prescaler bypassed), the filter suppresses spikes of less than 10.4 ns.

For standard mode (for example, the I2C*i*.I2C_PSC[7:0] PSC bit field = 4), the maximum width of suppressed spikes is 52 ns.

To ensure correct filtering, the prescaler must be programmed accordingly by the 2C*i*.I2C_PSC[7:0] PSC bit field.

23.1.4.10 HS I²C System Test Mode

A system test mode is available for multimaster HS I²C controller module testing. This mode is enabled by setting the I2C*i*.I2C_SYSTEST[15] ST_EN bit to 1. When this bit is cleared to 0, the I²C controller is configured in normal operation mode.

In system test mode, the I2C*i*.I2C_SYSTEST [13:12] TMODE bit field selects the type of test. Table 23-12 lists the tests available for the multimaster HS I²C controllers.

Table 23-12. HS I²C List of Tests

I2C*i*.I2C_SYSTEST[13:12] TMODE	Test	Description
00	Functional mode	Normal operation mode
01	Reserved (not used)	
10	Test of i2c*i*_scl serial clock line	The i2c*i*_scl line is driven with a permanent clock as if mastered with the parameters set in the I2C*i*.I2C_PSC, I2C*i*.I2C_SCLL, and I2C*i*.I2C_SCLH registers.
11	Loop-back mode + i2c*i*_scl/ i2c*i*_sda I/O	In master transmit mode only, data transmitted out of the I2C*i*.I2C_DATA register (write action) is received in the same I2C*i*.I2C_DATA register through an internal path through the FIFO buffers. The DMA and interrupt requests are normally generated if they are enabled. Moreover, the i2c*i*_scl and i2c*i*_sda are controlled with the I2C*i*.I2C_SYSTEST[4:0] bits.

NOTE: When the I2C*i*.I2C_SYSTEST[13:12] TMODE bit field is set to 11, the I²C controller must be configured in I²C F/S (I2C*i*.I2C_CON[13:12] OPMODE set to 00) or I²C HS mode (I2C*i*.I2C_CON[13:12] OPMODE set to 01).

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NOTE: In normal operation mode (the I2C*i*.I2C_SYSTEST[15] ST_EN bit cleared to 0), the I2C*i*.I2C_SYSTEST[4:0] bits that control the i2c*i*_scl, i2c*i*_sda lines in system test mode are read-only bits.

In system test mode (the I2C*i*.I2C_SYSTEST[15] ST_EN bit set to 1), the I2C*i*.I2C_IRQSTATUS_RAW.XRDY, I2C_IRQSTATUS_RAW.RRDY, I2C_IRQSTATUS_RAW.XUDF, I2C_IRQSTATUS_RAW.ROVR, I2C_IRQSTATUS_RAW.ARDY and I2C_IRQSTATUS_RAW.NACK status bits can be set to 1 when the I2C*i*.I2C_SYSTEST[11] SSB bit is set to 1. Clearing the I2C*i*.I2C_SYSTEST[11] SSB bit to 0 does not clear the I2C*i*.I2C_IRQSTATUS_RAW bits to 0. The I2C*i*.I2C_IRQSTATUS_RAW bit field can be cleared to 0 only by writing 1 in the corresponding bits.

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23.1.5 HS I²C Programming Guide

23.1.5.1 HS I²C Low-Level Programming Models

23.1.5.1.1 HS I²C Programming Model

This section describes the programming model of the multimaster HS I²C controllers configured in I²C mode.

23.1.5.1.1.1 Main Program

23.1.5.1.1.1.1 Configure the Module Before Enabling the I²C Controller

Before enabling the I²C controller, perform the following steps:

1. Enable the functional and interface clocks (see Table 23-3).
2. Program the prescaler to obtain an approximately 12-MHz internal sampling clock by programming the corresponding value in the I2C*i*.I2C_PSC[7:0] PSC bit field. This value depends on the frequency of the functional clock (I2C*i*_FCLK).
3. Program the I2C*i*.I2C_SCLL[7:0] SCLL and I2C*i*.I2C_SCLH[7:0] SCLH bit fields to obtain a bit rate of 100 kbps, 400 kbps, or 1 Mbps. These values depend on the internal sampling clock frequency (see Table 23-6).
4. (Optional) Program the I2C*i*.I2C_SCLL[15:8] HSSCLL and I2C*i*.I2C_SCLH[15:8] HSSCLH bit fields to obtain a bit rate of 400 kbps or 3.4 Mbps (for the second phase of HS mode). These values depend on the internal sampling clock frequency (see Table 23-6).
5. Configure the Own Address of the I²C controller by storing it in the I2C*i*.I2C_OA register. Up to four Own Addresses can be programmed in the I2C*i*.I2C_OAx registers (where x = 0, 1, 2, 3) for each I²C controller.

NOTE: For a 10-bit address, set the corresponding expand Own Address bit in the I2C*i*.I2C_CON register.

6. Set the TX threshold (in transmitter mode) and the RX threshold (in receiver mode) by setting the I2C*i*.I2C_BUF[5:0] XTRSH bit field to (TX threshold – 1) and the I2C*i*.I2C_BUF[13:8]RTRSH bit field to (RX threshold – 1), where the TX and RX thresholds are greater than or equal to 1.
7. Take the I²C controller out of reset by setting the I2C*i*.I2C_CON[15] I2C_EN bit to 1.

23.1.5.1.1.1.2 Initialize the I²C Controller

To initialize the I²C controller, perform the following steps:

1. Configure the I2C*i*.I2C_CON register:
   - For master or slave mode, set the I2C*i*.I2C_CON[10] MST bit (0: slave; 1: master).
   - For transmitter or receiver mode, set the I2C*i*.I2C_CON[9] TRX bit (0: receiver; 1: transmitter).
2. If using an interrupt to transmit and receive data, set the corresponding bit in the I2C*i*.I2C_IRQENABLE_SET register to 1 (the I2C*i*.I2C_IRQENABLE_SET [4] XRDY_IE bit for the transmit interrupt, the I2C*i*.I2C_IRQENABLE_SET [3] RRDY bit for the receive interrupt).
3. If using DMA to receive and transmit data, set the corresponding bit in the I2C*i*.I2C_BUF register to 1 (the I2C*i*.I2C_BUF[15] RDMA_EN bit for the receive DMA channel, the I2C*i*.I2C_BUF[7] XDMA_EN bit for the transmit DMA channel).

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23.1.5.1.1.1.3 Configure Slave Address and the Data Control Register

In master mode, configure the slave address register by programming the I2C*i*.I2C_SA[9:0] SA bit field and the number of data bytes (I²C data payload) associated with the transfer by programming the I2C*i*.I2C_CNT[15:0] DCOUNT bit field.

NOTE: For a 10-bit address, set the I2C*i*.I2C_CON[8] XSA bit to 1.

23.1.5.1.1.1.4 Initiate a Transfer

Poll the I2C*i*.I2C_IRQSTATUS_RAW [12] BB bit. If it is cleared to 0 (bus not busy), configure the I2C*i*.I2C_CON[0] STT and I2C*i*.I2C_CON[1] STP bits. To initiate a transfer, the I2C*i*.I2C_CON[0] STT bit must be set to 1, and it is not mandatory to set the I2C*i*.I2C_CON[1] STP bit to 1.

23.1.5.1.1.1.5 Receive Data

Poll the I2C*i*.I2C_IRQSTATUS_RAW [3] RRDY bit, or use the RRDY interrupt (the I2C*i*.I2C_IRQENABLE_SET [3] RRDY_IE bit must be set to 1) or the DMA RX channel (the I2C*i*.I2C_BUF[15] RDMA_EN bit must be set to 1 together with I2C_DMARXENABLE_SET) to read the receive data in the I2C*i*.I2C_DATA register.

If the transfer length does not equal the RX FIFO threshold (the I2C*i*.I2C_BUF[13:8] RTRSH bit field + 1), use the draining feature (enable the RDR interrupt by setting the I2C*i*.I2C_IRQENABLE_SET [13] RDR_IE bit to 1).

NOTE: In receive mode only, the I2C*i*.I2C_IRQSTATUS_RAW [11] ROVR (receive overrun) bit indicates whether the receiver has experienced overrun. An overrun condition occurs when the shift register and the RX FIFO are full. An overrun condition does not result in data loss; the I²C controller simply holds i2c*i*_scl to low to prevent other bytes from being received.

The I2C*i*.I2C_IRQSTATUS_RAW[7] AERR bit is set to 1 when a read access is performed in the I2C*i*.I2C_DATA register while the RX FIFO is empty. The corresponding interrupt can be enabled by setting the I2C*i*.I2C_IRQENABLE_SET [7] AERR_IE bit to 1.

23.1.5.1.1.1.6 Transmit Data

Poll the I2C*i*.I2C_IRQSTATUS_RAW [4] XRDY bit, or use the XRDY interrupt (the I2C*i*.I2C_IRQENABLE_SET [4] XRDY_IE bit must be set to 1) or the DMA TX channel (the I2C*i*.I2C_BUF[7] XDMA_EN bit must be set to 1 together with I2C_DMATXENABLE_SET) to write data to the I2C*i*.I2C_DATA register.

If the transfer length does not equal the TX FIFO threshold (the I2C*i*.I2C_BUF[5:0] TXTRSH bit field + 1), use the draining feature (enable the XDR interrupt by setting the I2C*i*.I2C_IRQENABLE_SET [14] XDR_IE bit to 1).

NOTE: In transmit mode only, the I2C*i*.I2C_IRQSTATUS_RAW [10] XUDF bit indicates whether the transmitter has experienced underflow.

In master transmit mode, underflow occurs when the shift register and the TX FIFO are empty and there are still some bytes to transmit (the value of the I2C*i*.I2C_CNT[15:0] DCOUNT bit field is not 0).

In slave transmit mode, underflow occurs when the shift register and the TX FIFO are empty and the external I²C master device still requests data bytes to be read.

The I2C*i*.I2C_IRQSTATUS_RAW [7] AERR bit is set to 1 when a write access is performed in the I2C*i*.I2C_DATA register while the TX FIFO is full. The corresponding interrupt can be enabled by setting the I2C*i*.I2C_IRQENABLE_SET [7] AERR_IE bit to 1.

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23.1.5.1.1.2 Interrupt Subroutine Sequence

1. Test for arbitration lost (the I2C*i*.I2C_IRQSTATUS_RAW [0] AL bit) and resolve accordingly.
2. Test for no acknowledgment (the I2C*i*.I2C_IRQSTATUS_RAW [1] NACK bit) and resolve accordingly.
3. Test for register access ready (the I2C*i*.I2C_IRQSTATUS_RAW [2] ARDY bit) and resolve accordingly.
4. Test for receive data ready (the I2C*i*.I2C_IRQSTATUS_RAW [3] RRDY bit) and resolve accordingly.
5. Test for transmit data ready (the I2C*i*.I2C_IRQSTATUS_RAW [4] XRDY bit) and resolve accordingly.
6. Test for general call (the I2C*i*.I2C_IRQSTATUS_RAW [5] GC bit) and resolve accordingly.
7. Test for start (S) condition (the I2C*i*.I2C_IRQSTATUS_RAW [6] STC bit) and resolve accordingly. For this test, the functional clock must be inactive.
8. Test for access error (the I2C*i*.I2C_IRQSTATUS_RAW [7] AERR bit) and resolve accordingly.
9. Test for bus free (the I2C*i*.I2C_IRQSTATUS_RAW [8] BF bit) and resolve accordingly.

23.1.5.1.1.3 Programming Flow Diagrams

Figure 23-21 through Figure 23-29 are procedure flow charts for programming the F/S and HS I²C modes.

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Figure 23-21. HS I²C Setup Procedure

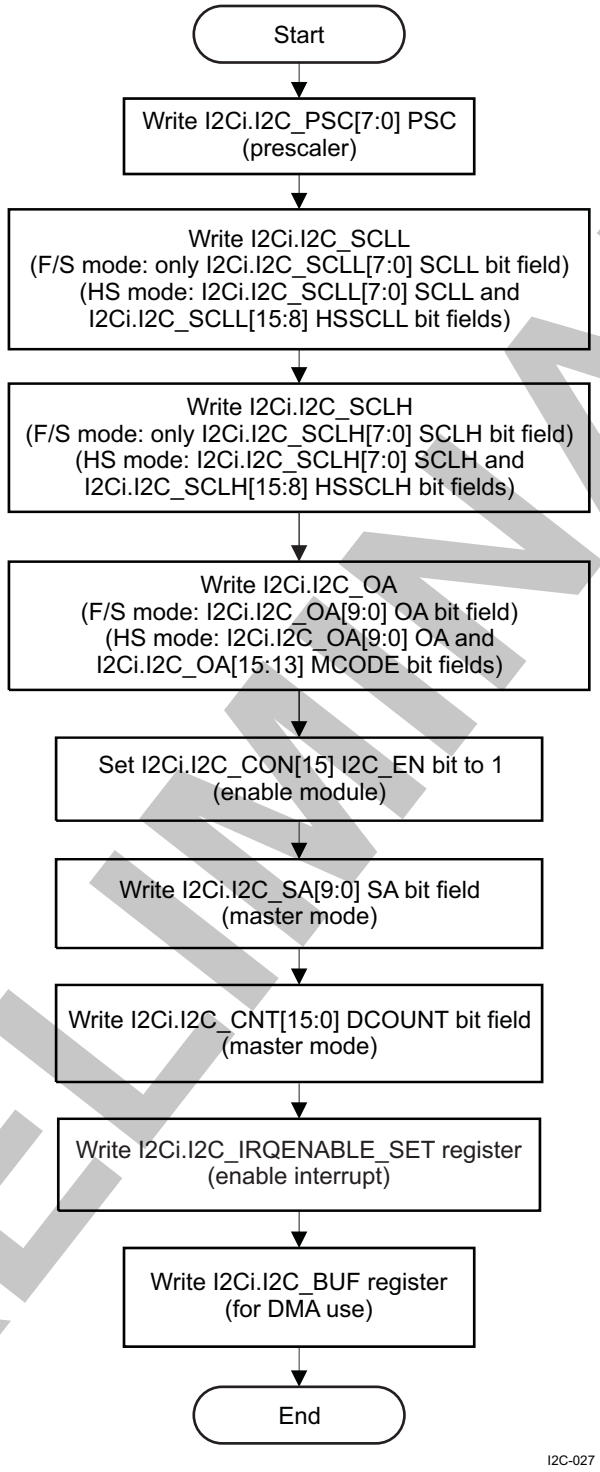

Table 23-13. Subprocess Call Summary for Sequence – I²C Setup Procedure

Subprocess Name	Cross-Reference
Pad configuration	See Section 18.4.8, *PAD Functional Multiplexing and Configuration* in *Figure 18-1Control Module*

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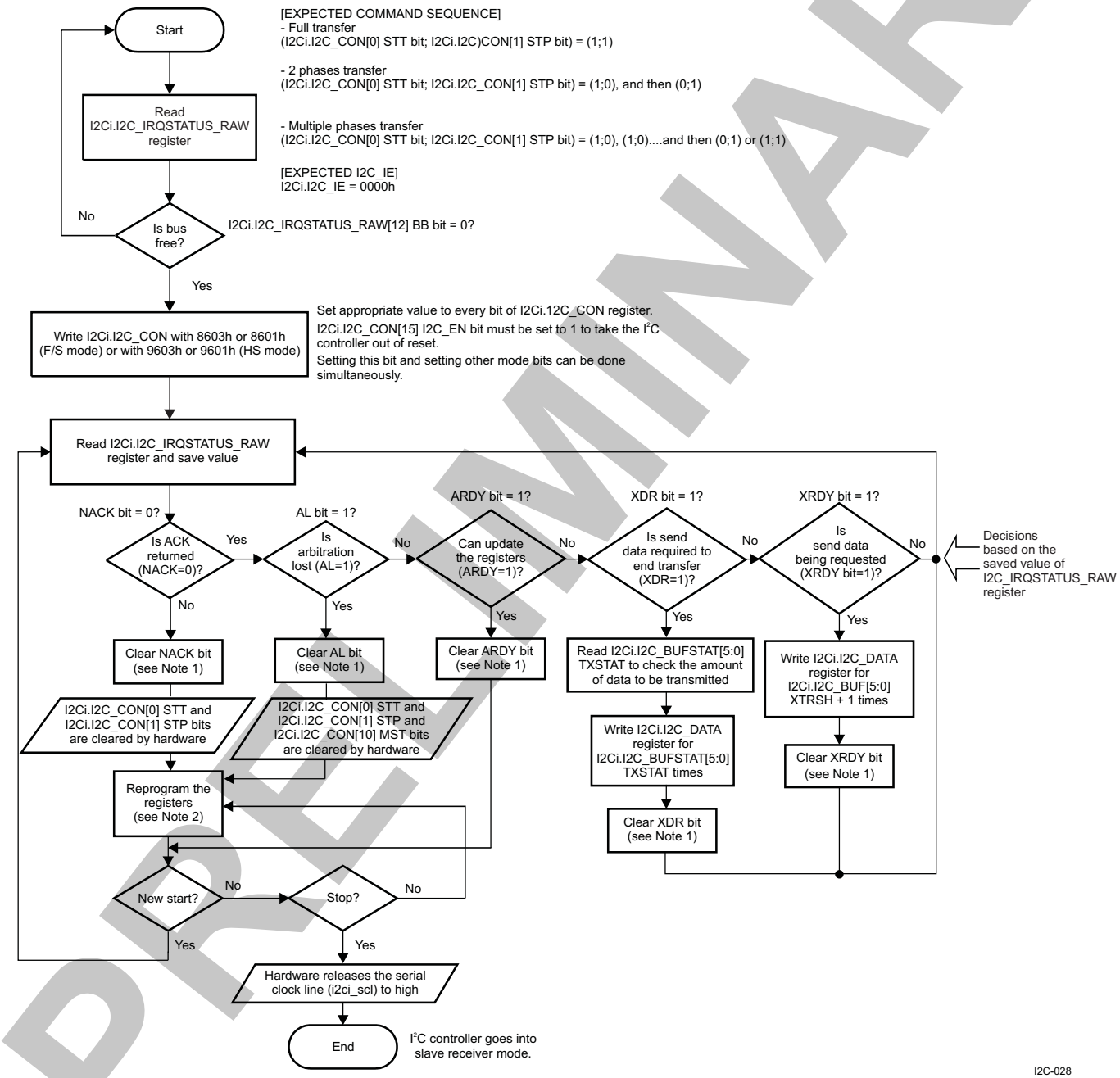
Table 23-14. HS I²C Register Call Summary for Sequence – Setup Procedure

Register Name	Register Name	Register Name
I2C*i*.I2C_PSC (1)	I2C*i*.I2C_CON (1)	I2C*i*.I2C_BUF (1)
I2C*i*.I2C_SCLL (1)	I2C*i*.I2C_SA (1)	I2C*i*.I2C_IRQENABLE_SET (1)
I2C*i*.I2C_SCLH (1)	I2C*i*.I2C_CNT (1)	I2C*i*.I2C_OA (1)

(1) *i* = 1 to 4

Figure 23-22. HS I²C Master Transmitter Mode, Polling Method, in F/S and HS Modes



(1) The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2C*i*.I2C_IRQSTATUS_RAW register.

(2) Reprogram the registers means: I2C*i*.I2C_CON[11] STB and/or I2C*i*.I2C_CON[10] MST bit and/or I2C*i*.I2C_SA[9:0] SA register and/or I2C*i*.I2C_CNT[15:0] DCOUNT register and/or I2C*i*.I2C_CON[0] STT bit and/or I2C*i*.I2C_CON[1] STP bit.

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NOTE: The FIFO clearing can be made when the module is configured as transmitter, the receiver send a NACK in the middle of the transfer, and there is still data in the FIFO.

Table 23-15. HS I²C Register Call Summary for Sequence – Master Transmitter Mode, Polling Method, in F/S and HS Modes

Register Name	Register Name	Register Name
I2C*i*.I2C_IRQSTATUS_RAW (1)	I2C*i*.I2C_DATA (1)	I2C*i*.I2C_CON (1)
I2C*i*.I2C_BUFSTAT (1)	I2C*i*.I2C_CON (1)	I2C*i*.I2C_BUF (1)

(1) *i* = 1 to 4

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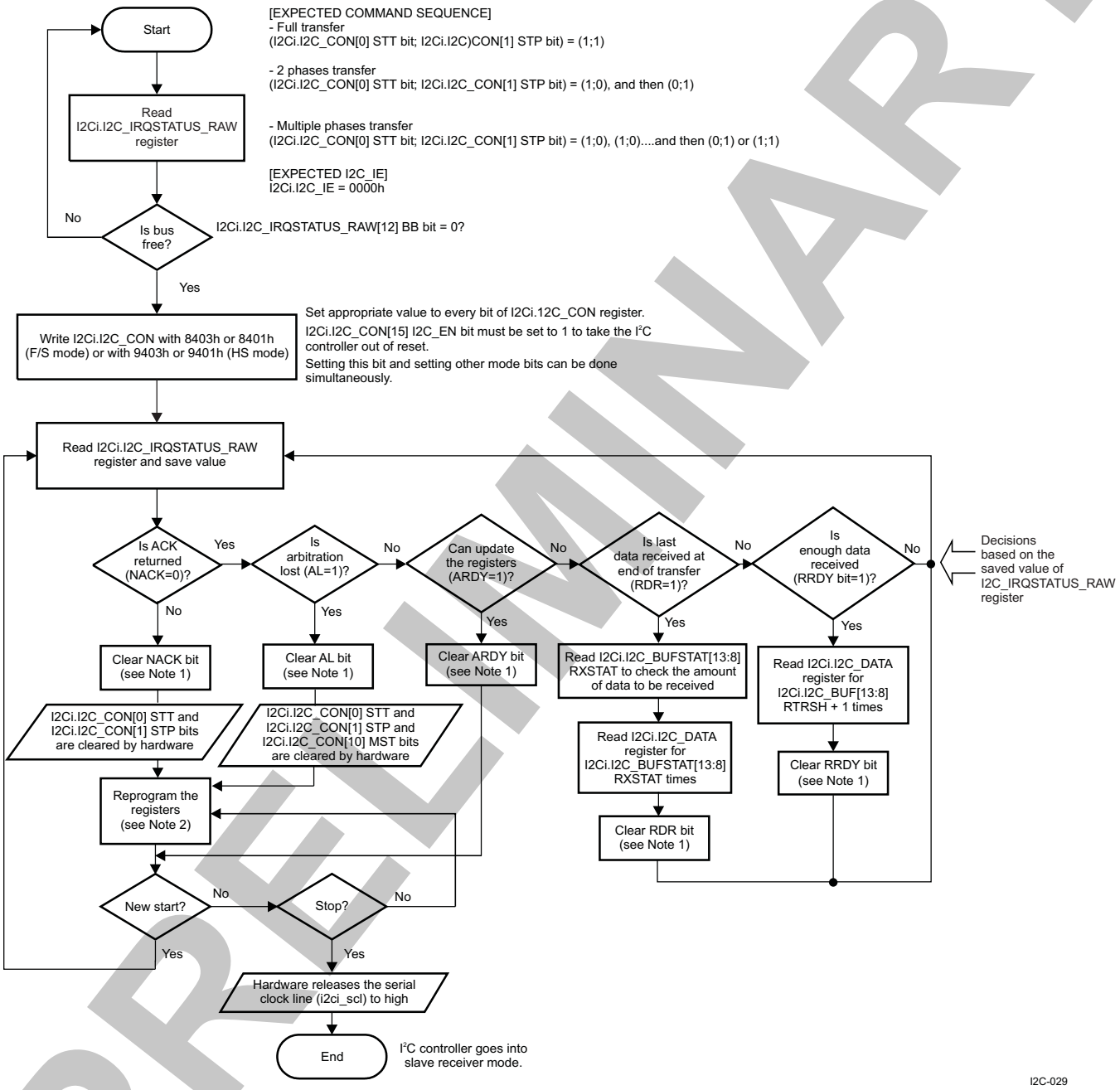
NOTE: In HS mode, the Sr condition and clock frequency switching are automatically generated by the multimaster HS I²C controller.

Figure 23-23. HS I²C Master Receiver Mode, Polling Method, in F/S and HS Modes



(1) The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2C*i*.I2C_IRQSTATUS_RAW register.

(2) Reprogram registers means: I2C*i*.I2C_CON[11] STB and/or I2C*i*.I2C_CON[10] MST bit and/or I2C*i*.I2C_SA[9:0] SA register and/or I2C*i*.I2C_CNT[15:0] DCOUNT register and/or I2C*i*.I2C_CON[0] STT bit and/or I2C*i*.I2C_CON[1] STP bit.

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Table 23-16. HS I²C Register Call Summary for Sequence – Master Receiver Mode, Polling Method, in F/S and HS Modes

Register Name	Register Name	Register Name
I2C*i*.I2C_IRQSTATUS_RAW [(1)]	I2C*i*.I2C_BUFSTAT [(1)]	I2C*i*.I2C_BUF [(1)]
I2C*ii*.I2C_CON [(1)]	I2C*i*.I2C_DATA [(1)]	

(1) *i* = 1 to 4

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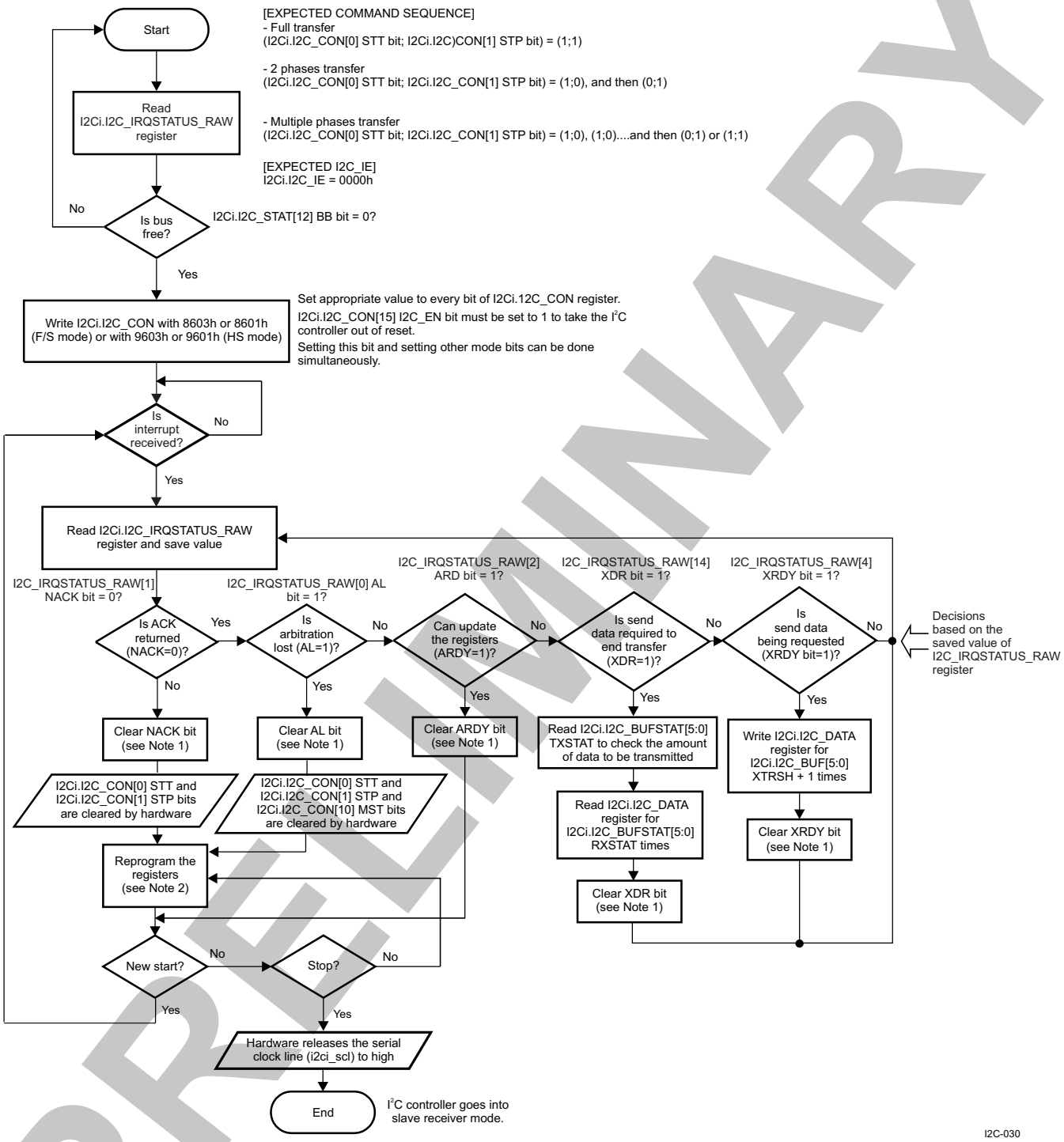
Figure 23-24. HS I²C Master Transmitter Mode, Interrupt Method, in F/S and HS Modes



(1) The NACK, AL, ARDY, XDR, and XRDY bits are cleared by writing 1 to each corresponding bit in the I2C*i*.I2C_IRQSTATUS_RAW register.

(2) Reprogram registers means: I2C*i*.I2C_CON[11] STB and/or I2C*i*.I2C_CON[10] MST bit and/or I2C*i*.I2C_SA[9:0] SA register and/or I2C*i*.I2C_CNT[15:0] DCOUNT register and/or I2C*i*.I2C_CON[0] STT bit and/or I2C*i*.I2C_CON[1] STP bit.

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NOTE: The FIFO clearing can be made when the module is configured as transmitter, the receiver send a NACK in the middle of the transfer, and there is still data in the FIFO.

Table 23-17. HS I²C Register Call Summary for Sequence – Master Transmitter Mode, Interrupt Method, in F/S and HS Modes

Register Name	Register Name	Register Name
I2C*i*.I2C_IRQSTATUS_RAW [(1)]	I2C*i*.I2C_BUFSTAT [(1)]	I2C*i*.I2C_BUF [(1)]
I2C*i*.I2C_CON [(1)]	I2C*i*.I2C_DATA [(1)]	

(1) *i* = 1 to 4

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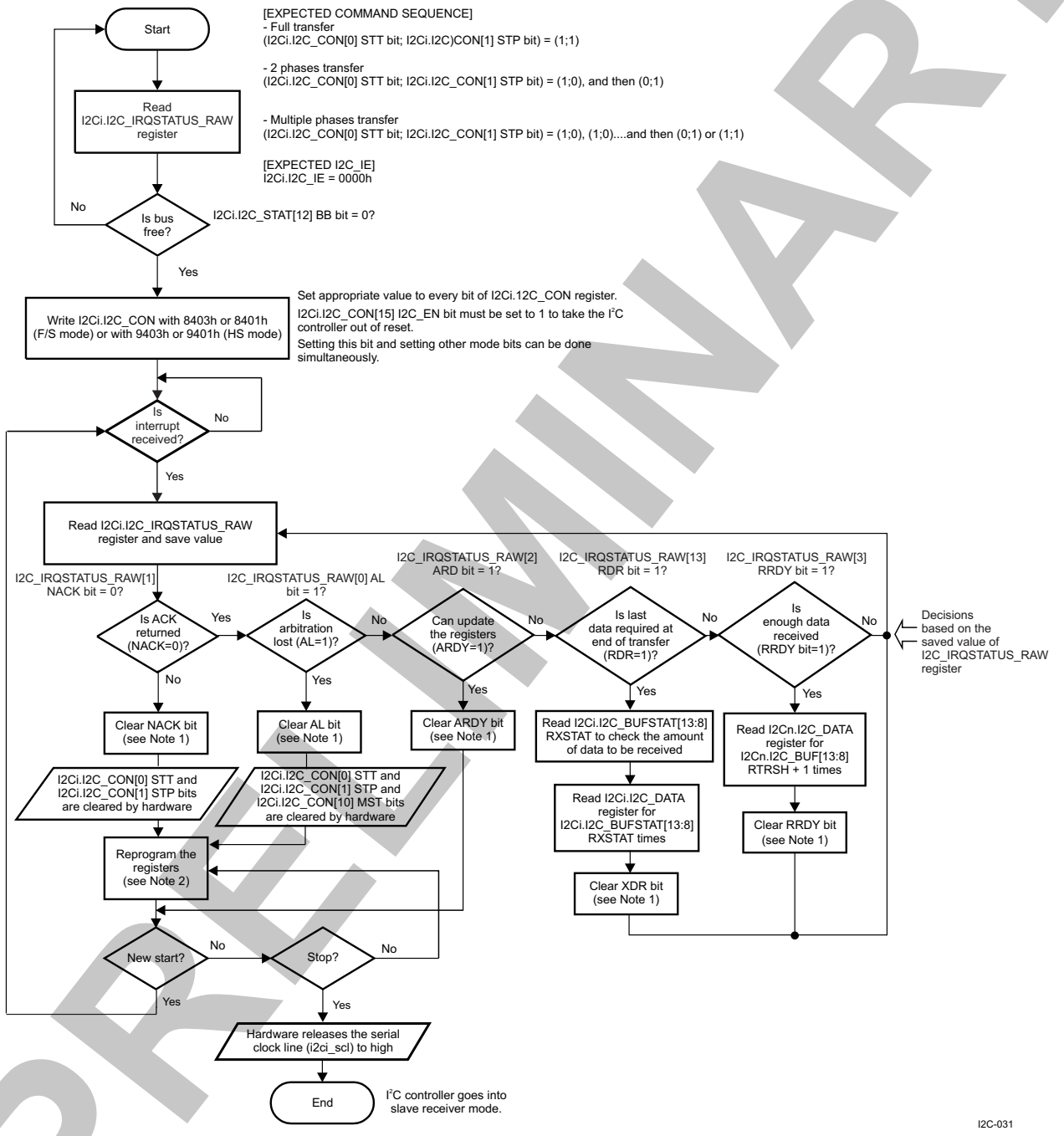
NOTE: In HS mode, the Sr condition and clock frequency switching are automatically generated by the multimaster HS I²C controller.

Figure 23-25. HS I²C Master Receiver Mode, Interrupt Method, in F/S and HS Modes



(1) The NACK, AL, ARDY, RDR, and RRDY bits are cleared by writing 1 to each corresponding bit in the I2C*i*.I2C_IRQSTATUS_RAW register.

(2) Reprogram registers means: I2C*i*.I2C_CON[11] STB and/or I2C*i*.I2C_CON[10] MST bit and/or I2C*i*.I2C_SA[9:0] SA register and/or I2C*i*.I2C_CNT[15:0] DCOUNT register and/or I2C*i*.I2C_CON[0] STT bit and/or I2C*i*.I2C_CON[1] STP bit.

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Table 23-18. HS I²C Register Call Summary for Sequence – Master Receiver Mode, Interrupt Method, in F/S and HS Modes

Register Name	Register Name	Register Name
I2C*i*.I2C_IRQSTATUS_RAW [(1)]	I2C*i*.I2C_BUFSTAT [(1)]	I2C*i*.I2C_BUF [(1)]
I2C*i*.I2C_CON [(1)]	I2C*i*.I2C_DATA [(1)]	

(1) *i* = 1 to 4

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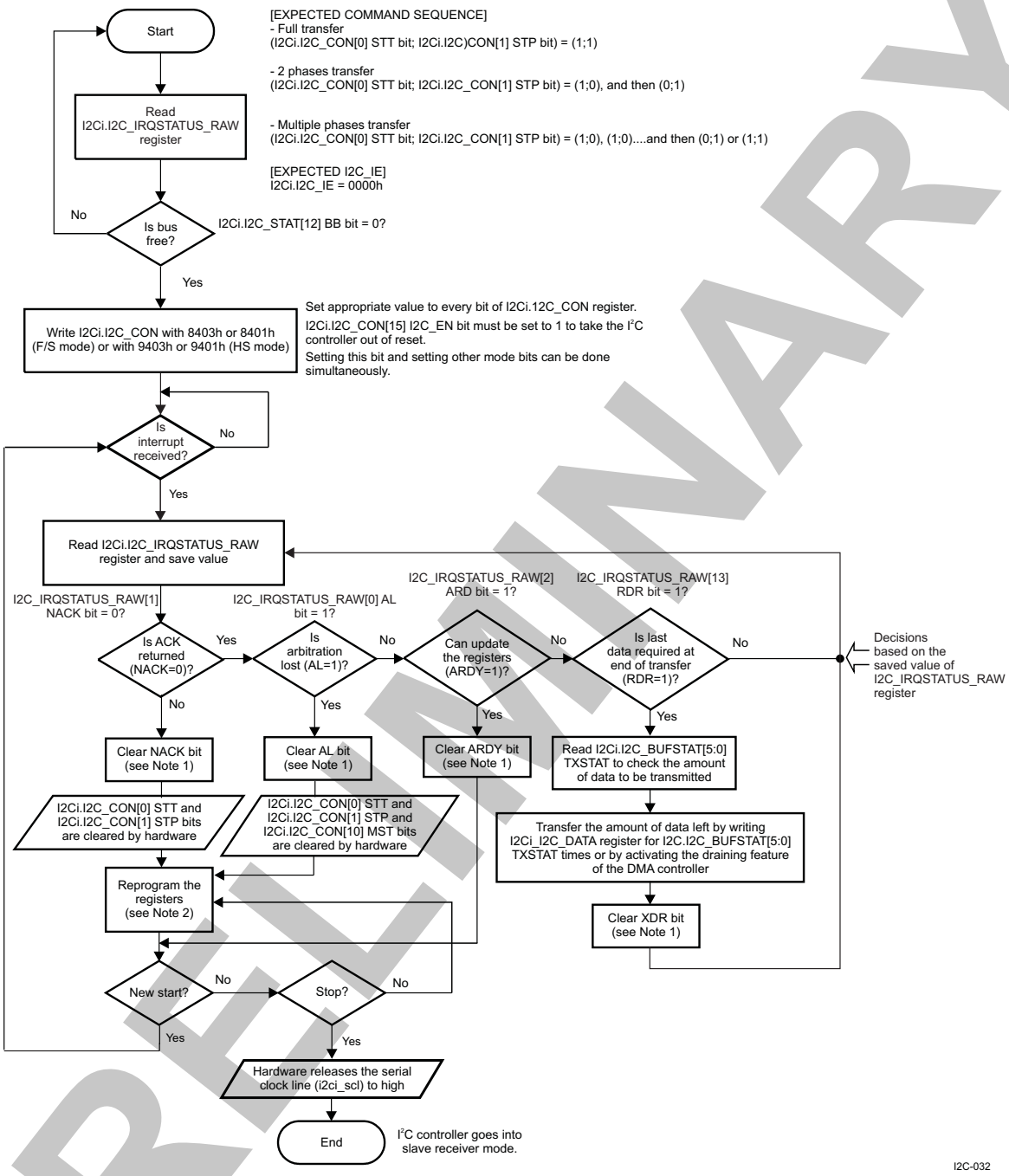
Figure 23-26. HS I²C Master Transmitter Mode, DMA Method in F/S and HS Modes



(1) The NACK, AL, ARDY, and XDR bits are cleared by writing 1 to each corresponding bit in the I2C*i*.I2C_IRQSTATUS_RAW register.

(2) Reprogram registers means: I2C*i*.I2C_CON[11] STB and/or I2Ci.I2C_CON[10] MST bit and/or I2C*i*.I2C_SA[9:0] SA register and/or I2C*i*.I2C_CNT[15:0] DCOUNT register and/or I2C*i*.I2C_CON[0] STT bit and/or I2C*i*.I2C_CON[1] STP bit.

NOTE: The FIFO clearing can be made when the module is configured as transmitter, the receiver send a NACK in the middle of the transfer, and there is still data in the FIFO.

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Table 23-19. HS I²C Register Call Summary for Sequence – Master Transmitter Mode, DMA Method in F/S and HS Modes

Register Name	Register Name
I2C*i*.I2C_IRQSTATUS_RAW (1)	I2Ci.I2C_BUFSTAT (1)
I2C*i*.I2C_CON (1)	I2Ci.I2C_DATA (1)

(1) *i* = 1 to 4

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NOTE: In HS mode, the Sr condition and clock frequency switching are automatically generated by the multimaster HS I²C controller.

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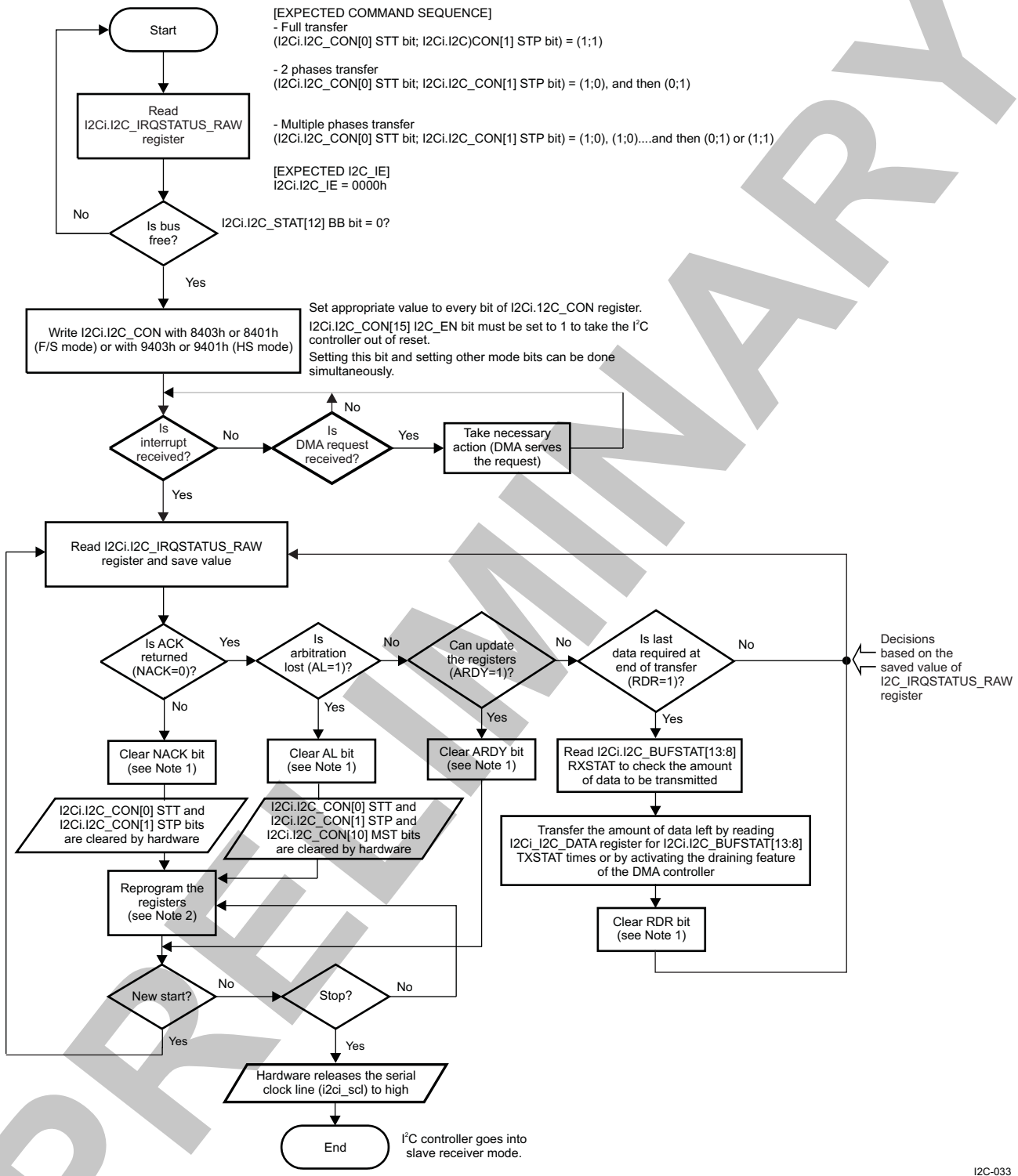
Figure 23-27. HS I²C Master Receiver Mode, DMA Method in F/S and HS Modes



(1) The NACK, AL, ARDY, and RDR bits are cleared by writing 1 to each corresponding bit in the I2C*i*.I2C_IRQSTATUS_RAW register.

(2) Reprogram registers means: I2C*i*.I2C_CON[11] STB and/or I2C*i*.I2C_CON[10] MST bit and/or I2C*i*.I2C_SA[9:0] SA register and/or I2C*i*.I2C_CNT[15:0] DCOUNT register and/or I2C*i*.I2C_CON[0] STT bit and/or I2C*i*.I2C_CON[1] STP bit.

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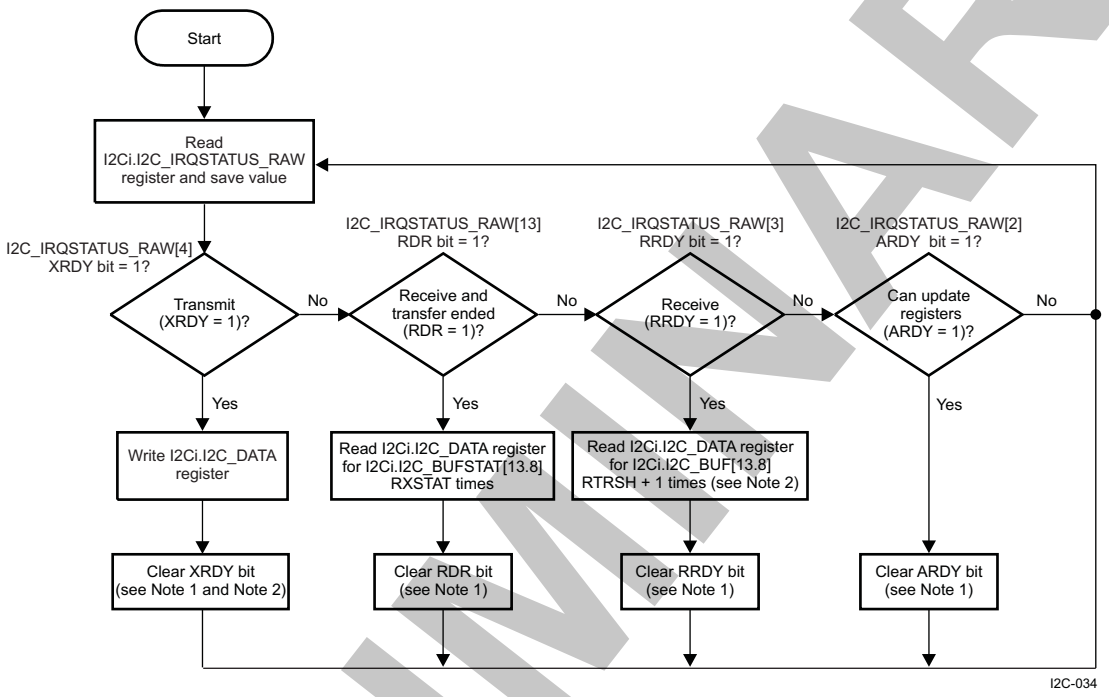
Table 23-20. HS I²C Register Call Summary for Sequence – Master Receiver Mode, DMA Method in F/S and HS Modes

Register Name	Register Name
I2C*i*.I2C_IRQSTATUS_RAW (1)	I2C*i*.I2C_BUFSTAT (1)
I2Ci.I2C_CON (1)	I2C*i*.I2C_DATA (1)

(1) *i* = 1 to 4

Figure 23-28. HS I²C Slave Transmitter/Receiver Mode, Polling



(1) The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2C*i*.I2C_IRQSTATUS_RAW register.

(2) In slave transmitter mode, the amount of data requested by the external master I²C device is unknown; thus, the I2C*i*.I2C_BUF[5:0] XTRSH bit field must be configured to 0x0 (TX threshold = 1).

Table 23-21. HS I²C Register Call Summary for Sequence – Slave Transmitter/Receiver Mode, Polling

Register Name	Register Name
I2C*i*.I2C_IRQSTATUS_RAW (1)	I2C*i*.I2C_BUFSTAT (1)
I2C*i*.I2C_DATA (1)	I2C*i*.I2C_BUF (1)

(1) *i* = 1 to 4

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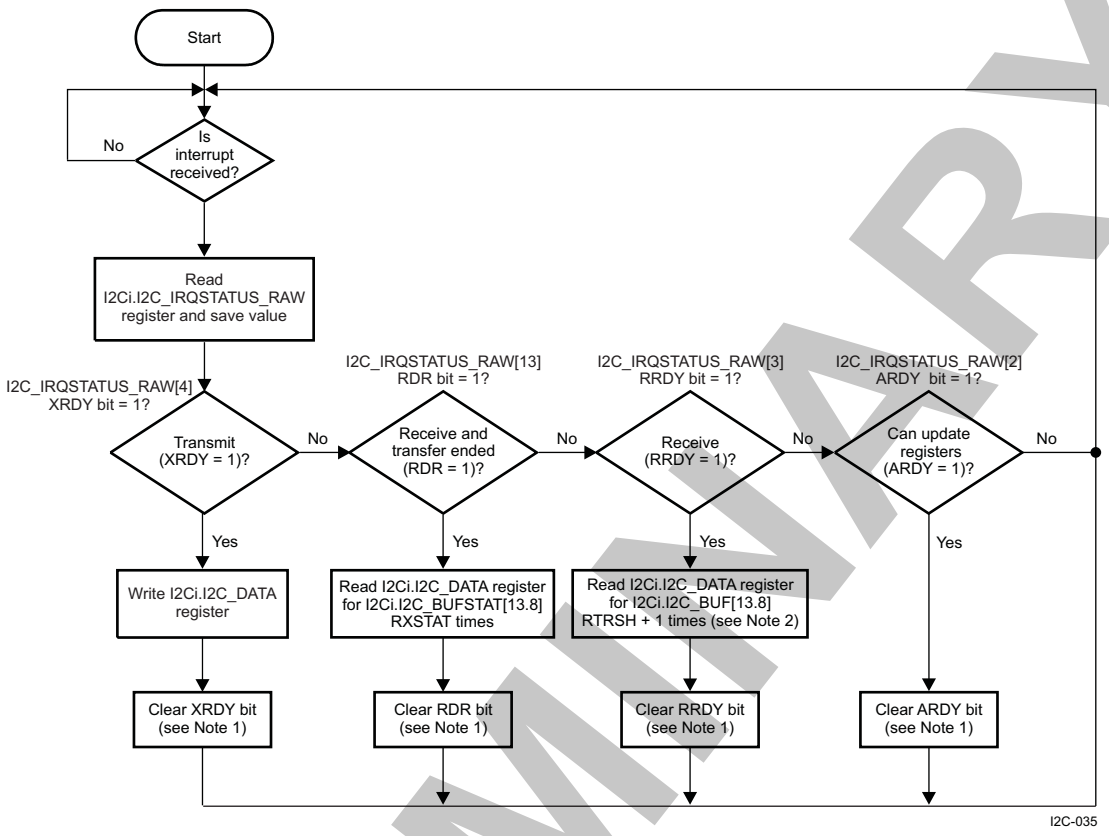
Figure 23-29. HS I²C Slave Transmitter/Receiver Mode, Interrupt



(1) The XRDY, RDR, RRDY, and ARDY bits are cleared by writing 1 to each corresponding bit in the I2C*i*.I2C_IRQSTATUS_RAW register.

(2) In slave transmitter mode, the amount of data requested by the external master I²C device is unknown; thus, the I2C*i*.I2C_BUF[5:0] XTRSH bit field must be configured to 0x0 (TX threshold = 1).

Table 23-22. HS I²C Register Call Summary for Sequence – Slave Transmitter/Receiver Mode, Interrupt

Register Name	Register Name
I2C*i*.I2C_IRQSTATUS_RAW (1)	I2C*i*.I2C_BUFSTAT (1)
I2C*i*.I2C_DATA (1)	I2C*i*.I2C_BUF (1)

(1) *i* = 1 to 4

23.1.6 HS I²C Register Manual

23.1.6.1 HS I²C Instance Summary

Table 23-23. HS I²C Instance Summary

Module Name	Module Base Address	Size
I2C3	0x4806 0000	4 KiB
I2C1	0x4807 0000	4 KiB
I2C2	0x4807 2000	4 KiB
I2C4	0x4807 A000	4 KiB
I2C5	0x4807 C000	4 KiB

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23.1.6.2 HS I²C Registers

CAUTION

The HS I2C*i* registers are limited to 16-bit and 8-bit data accesses; 32-bit data access is not allowed and can corrupt register content.

23.1.6.2.1 HS I²C Register Summary

Table 23-24. HS I²C Registers Mapping Summary 1

Register Name	Type	Register Width (Bits)	Address Offset	I2C3 Physical Address	I2C1 Physical Address
I2C_REVNB_LO	R	16	0x0000 0000	0x4806 0000	0x4807 0000
I2C_REVNB_HI	R	16	0x0000 0004	0x4806 0004	0x4807 0004
I2C_SYSC	RW	16	0x0000 0010	0x4806 0010	0x4807 0010
RESERVED	W	16	0x0000 0020	0x4806 0020	0x4807 0020
I2C_IRQSTATUS_RAW	RW	16	0x0000 0024	0x4806 0024	0x4807 0024
I2C_IRQSTATUS	RW	16	0x0000 0028	0x4806 0028	0x4807 0028
I2C_IRQENABLE_SET	RW	16	0x0000 002C	0x4806 002C	0x4807 002C
I2C_IRQENABLE_CLR	RW	16	0x0000 0030	0x4806 0030	0x4807 0030
I2C_WE	RW	16	0x0000 0034	0x4806 0034	0x4807 0034
I2C_DMARXENABLE_SET	RW	16	0x0000 0038	0x4806 0038	0x4807 0038
I2C_DMATXENABLE_SET	RW	16	0x0000 003C	0x4806 003C	0x4807 003C
I2C_DMARXENABLE_CLR	RW	16	0x0000 0040	0x4806 0040	0x4807 0040
I2C_DMATXENABLE_CLR	RW	16	0x0000 0044	0x4806 0044	0x4807 0044
I2C_DMARXWAKE_EN	RW	16	0x0000 0048	0x4806 0048	0x4807 0048
I2C_DMATXWAKE_EN	RW	16	0x0000 004C	0x4806 004C	0x4807 004C
RESERVED	RW	16	0x0000 0084	0x4806 0084	0x4807 0084
RESERVED	RW	16	0x0000 0088	0x4806 0088	0x4807 0088
I2C_SYSS	RW	16	0x0000 0090	0x4806 0090	0x4807 0090
I2C_BUF	RW	16	0x0000 0094	0x4806 0094	0x4807 0094
I2C_CNT	RW	16	0x0000 0098	0x4806 0098	0x4807 0098
I2C_DATA	RW	16	0x0000 009C	0x4806 009C	0x4807 009C
I2C_CON	RW	16	0x0000 00A4	0x4806 00A4	0x4807 00A4
I2C_OA	RW	16	0x0000 00A8	0x4806 00A8	0x4807 00A8
I2C_SA	RW	16	0x0000 00AC	0x4806 00AC	0x4807 00AC
I2C_PSC	RW	16	0x0000 00B0	0x4806 00B0	0x4807 00B0
I2C_SCLL	RW	16	0x0000 00B4	0x4806 00B4	0x4807 00B4
I2C_SCLH	RW	16	0x0000 00B8	0x4806 00B8	0x4807 00B8
I2C_SYSTEST	RW	16	0x0000 00BC	0x4806 00BC	0x4807 00BC
I2C_BUFSTAT	R	16	0x0000 00C0	0x4806 00C0	0x4807 00C0
I2C_OA1	RW	16	0x0000 00C4	0x4806 00C4	0x4807 00C4
I2C_OA2	RW	16	0x0000 00C8	0x4806 00C8	0x4807 00C8
I2C_OA3	RW	16	0x0000 00CC	0x4806 00CC	0x4807 00CC
I2C_ACTOA	R	16	0x0000 00D0	0x4806 00D0	0x4807 00D0
I2C_SBLOCK	RW	16	0x0000 00D4	0x4806 00D4	0x4807 00D4

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Table 23-25. HS I²C Registers Mapping Summary 2

Register Name	Type	Register Width (Bits)	Address Offset	I2C2 Physical Address	I2C4 Physical Address	I2C5 Physical Address
I2C_REVNB_LO	R	16	0x0000 0000	0x4807 2000	0x4807 A000	0x4807 C000
I2C_REVNB_HI	R	16	0x0000 0004	0x4807 2004	0x4807 A004	0x4807 C004
I2C_SYSC	RW	16	0x0000 0010	0x4807 2010	0x4807 A010	0x4807 C010
RESERVED	W	16	0x0000 0020	0x4807 2020	0x4807 A020	0x4807 C020
I2C_IRQSTATUS_RAW	RW	16	0x0000 0024	0x4807 2024	0x4807 A024	0x4807 C024
I2C_IRQSTATUS	RW	16	0x0000 0028	0x4807 2028	0x4807 A028	0x4807 C028
I2C_IRQENABLE_SET	RW	16	0x0000 002C	0x4807 202C	0x4807 A02C	0x4807 C02C
I2C_IRQENABLE_CLR	RW	16	0x0000 0030	0x4807 2030	0x4807 A030	0x4807 C030
I2C_WE	RW	16	0x0000 0034	0x4807 2034	0x4807 A034	0x4807 C034
I2C_DMARXENABLE_SET	RW	16	0x0000 0038	0x4807 2038	0x4807 A038	0x4807 C038
I2C_DMATXENABLE_SET	RW	16	0x0000 003C	0x4807 203C	0x4807 A03C	0x4807 C03C
I2C_DMARXENABLE_CLR	RW	16	0x0000 0040	0x4807 2040	0x4807 A040	0x4807 C040
I2C_DMATXENABLE_CLR	RW	16	0x0000 0044	0x4807 2044	0x4807 A044	0x4807 C044
I2C_DMARXWAKE_EN	RW	16	0x0000 0048	0x4807 2048	0x4807 A048	0x4807 C048
I2C_DMATXWAKE_EN	RW	16	0x0000 004C	0x4807 204C	0x4807 A04C	0x4807 C04C
RESERVED	RW	16	0x0000 0084	0x4807 2084	0x4807 A084	0x4807 C084
RESERVED	RW	16	0x0000 0088	0x4807 2088	0x4807 A088	0x4807 C088
I2C_SYSS	RW	16	0x0000 0090	0x4807 2090	0x4807 A090	0x4807 C090
I2C_BUF	RW	16	0x0000 0094	0x4807 2094	0x4807 A094	0x4807 C094
I2C_CNT	RW	16	0x0000 0098	0x4807 2098	0x4807 A098	0x4807 C098
I2C_DATA	RW	16	0x0000 009C	0x4807 209C	0x4807 A09C	0x4807 C09C
I2C_CON	RW	16	0x0000 00A4	0x4807 20A4	0x4807 A0A4	0x4807 C0A4
I2C_OA	RW	16	0x0000 00A8	0x4807 20A8	0x4807 A0A8	0x4807 C0A8
I2C_SA	RW	16	0x0000 00AC	0x4807 20AC	0x4807 A0AC	0x4807 C0AC
I2C_PSC	RW	16	0x0000 00B0	0x4807 20B0	0x4807 A0B0	0x4807 C0B0
I2C_SCLL	RW	16	0x0000 00B4	0x4807 20B4	0x4807 A0B4	0x4807 C0B4
I2C_SCLH	RW	16	0x0000 00B8	0x4807 20B8	0x4807 A0B8	0x4807 C0B8
I2C_SYSTEST	RW	16	0x0000 00BC	0x4807 20BC	0x4807 A0BC	0x4807 C0BC
I2C_BUFSTAT	R	16	0x0000 00C0	0x4807 20C0	0x4807 A0C0	0x4807 C0C0
I2C_OA1	RW	16	0x0000 00C4	0x4807 20C4	0x4807 A0C4	0x4807 C0C4
I2C_OA2	RW	16	0x0000 00C8	0x4807 20C8	0x4807 A0C8	0x4807 C0C8
I2C_OA3	RW	16	0x0000 00CC	0x4807 20CC	0x4807 A0CC	0x4807 C0CC
I2C_ACTOA	R	16	0x0000 00D0	0x4807 20D0	0x4807 A0D0	0x4807 C0D0
I2C_SBLOCK	RW	16	0x0000 00D4	0x4807 20D4	0x4807 A0D4	0x4807 C0D4

23.1.6.2.2 HS I²C Register Description

Table 23-26. I2C_REVNB_LO

Address Offset	0x0000 0000
Physical Address	0x4806 0000 0x4807 0000 0x4807 2000 0x4807 A000 0x4807 C000
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility
Type	R

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 23-27. Register Call Summary for Register I2C_REVNB_LO

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-28. I2C_REVNB_HI

Address Offset	0x0000 0004
Physical Address	0x4806 0004 0x4807 0004 0x4807 2004 0x4807 A004 0x4807 C004
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 23-29. Register Call Summary for Register I2C_REVNB_HI

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-30. I2C_SYSC

Address Offset	0x0000 0010
Physical Address	0x4806 0010 0x4807 0010 0x4807 2010 0x4807 A010 0x4807 C010
Description	System Configuration register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CLKACTIVITY		RESERVED			IDLEMODE		ENAWAKEUP	SRST	AUTOIDLE

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Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved	R	0x00
9:8	CLKACTIVITY	Clock Activity selection bits 0x0: Both clocks can be cut off 0x1: Only OCP clock must be kept active; system clock can be cut off 0x3: Both clocks must be kept active 0x2: Only system clock must be kept active; OCP clock can be cut off	RW	0x0
7:5	RESERVED	Reads return 0.	R	0x0
4:3	IDLEMODE	Idle Mode selection bits 0x0: Force Idle mode 0x1: No Idle mode 0x3: smartidle_wakeup 0x2: Smart Idle mode	RW	0x0
2	ENAWAKEUP	Enable Wakeup control bit 0x0: Wakeup mechanism is disabled 0x1: Wakeup mechanism is enabled	RW	0
1	SRST	SoftReset bit 0x0: Normal mode 0x1: The module is reset	RW	0
0	AUTOIDLE	Autoidle bit 0x0: Auto Idle mechanism is disabled 0x1: Auto Idle mechanism is enabled	RW	1

Table 23-31. Register Call Summary for Register I2C_SYSC

Multimaster High-Speed I2C Controller

- HS I2C Software Reset: [0] [1]
- HS I2C Power Management: [2] [3] [4] [5] [6]
- HS I2C Register Summary: [7] [8]

Table 23-32. I2C_IRQSTATUS_RAW

Address Offset	0x0000 0024
Physical Address	0x4806 0024 0x4807 0024 0x4807 2024 0x4807 A024 0x4807 C024
Description	Per-event raw interrupt status vector. The raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF	AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL

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Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR	Transmit draining IRQ status. 0x0: Transmit draining inactive. 0x1: Transmit draining enabled.	RW	0
13	RDR	Receive draining IRQ status. 0x0: Receive draining inactive. 0x1: Receive draining enabled.	RW	0
12	BB	Bus busy status. Writing into this bit has no effect. Read 0x1: Bus is occupied. Read 0x0: Bus is free.	R	0
11	ROVR	Receive overrun status. Writing into this bit has no effect. Read 0x1: Receiver overrun. Read 0x0: Normal operation.	RW	0
10	XUDF	Transmit underflow status. Writing into this bit has no effect. Read 0x1: Transmit underflow. Read 0x0: Normal operation.	RW	0
9	AAS	Address recognized as slave IRQ status. 0x0: No action. 0x1: Address recognized.	RW	0
8	BF	Bus Free IRQ status. 0x0: No action. 0x1: Bus Free.	RW	0
7	AERR	Access Error IRQ status. 0x0: No action. 0x1: Access Error.	RW	0
6	STC	Start Condition IRQ status. 0x0: No action. 0x1: Start Condition detected.	RW	0

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Bits	Field Name	Description	Type	Reset
5	GC	General call IRQ status. Set to 1 by core when General call address detected and interrupt signaled to MPUSS. (1) 0x0: No general call detected. 0x1: General call address detected.	RW	0
4	XRDY	Transmit data ready IRQ status. Set to 1 by core when transmitter and when new data is requested. When set to 1 by core, an interrupt is signaled to MPUSS. (1) 0x0: Transmision ongoing. 0x1: Transmit data ready.	RW	0
3	RRDY	Receive data ready IRQ status. Set to 1 by core when receiver mode, a new data is able to be read. When set to 1 by core, an interrupt is signaled to MPUSS. (1) 0x0: No data available. 0x1: Receive data available.	RW	0
2	ARDY	Register access ready IRQ status. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to MPUSS. (1) 0x0: Module busy. 0x1: Access ready.	RW	0
1	NACK	No acknowledgement IRQ status. Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS. (1) 0x0: Normal operation. 0x1: Not Acknowledge detected.	RW	0
0	AL	Arbitration lost IRQ status. This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to MPUSS. During reads, it always returns 0. 0x0: Normal operation. 0x1: Arbitration lost detected.	RW	0

(1) Writing 1 in the bit field will only set the respective field to 1, used mainly for debug.

Table 23-33. Register Call Summary for Register I2C_IRQSTATUS_RAW

Multimaster High-Speed I2C Controller

- HS I2C Start and Stop Conditions: [0] [1]
- HS I2C FIFO Polling Mode: [2] [3] [4] [5] [6] [7]
- HS I2C Draining Feature: [8] [9] [10] [11] [12]
- HS I2C System Test Mode: [13] [14] [15] [16] [17] [18] [19] [20]
- Main Program: [21] [22] [23] [24] [25] [26] [27]
- Interrupt Subroutine Sequence: [28] [29] [30] [31] [32] [33] [34] [35] [36]
- Programming Flow Diagrams: [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52]
- HS I2C Register Summary: [53] [54]
- HS I2C Register Description: [55] [56] [57] [58] [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74] [75]

Table 23-34. I2C_IRQSTATUS

Address Offset	0x0000 0028
Physical Address	0x4806 0028 0x4807 0028 0x4807 2028 0x4807 A028 0x4807 C028
Description	Per-event enabled interrupt status vector
Type	RW

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF	AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL

Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR	Transmit draining IRQ enabled status. 0x0: Transmit draining inactive. 0x1: Transmit draining enabled.	RW W1toClr	0
13	RDR	Receive draining IRQ enabled status. 0x0: Receive draining inactive. 0x1: Receive draining enabled.	RW W1toClr	0
12	BB	Bus busy status. Read 0x1: Bus is occupied. Read 0x0: Bus is free.	R	0
11	ROVR	Receive overrun enabled status. Writing into this bit has no effect. Read 0x1: Receiver overrun. Read 0x0: Normal operation.	RW W1toClr	0
10	XUDF	Transmit underflow enabled status. Writing into this bit has no effect. Read 0x1: Transmit underflow. Read 0x0: Normal operation.	RW W1toClr	0
9	AAS	Address recognized as slave IRQ enabled status. 0x0: No action. 0x1: Address recognized.	RW W1toClr	0
8	BF	Bus Free IRQ enabled status. 0x0: No action. 0x1: Bus Free.	RW W1toClr	0
7	AERR	Access Error IRQ enabled status. 0x0: No action. 0x1: Access Error.	RW W1toClr	0
6	STC	Start Condition IRQ enabled status. 0x0: No action. 0x1: Start Condition detected.	RW W1toClr	0
5	GC	General call IRQ enabled status. Set to 1 by core when General call address detected and interrupt signaled to MPUSS. Write 1 to clear. 0x0: No general call detected. 0x1: General call address detected.	RW W1toClr	0
4	XRDY	Transmit data ready IRQ enabled status. Set to 1 by core when transmitter and when new data is requested. When set to 1 by core, an interrupt is signaled to MPUSS. Write 1 to clear. 0x0: Transmision ongoing. 0x1: Transmit data ready.	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
3	RRDY	Receive data ready IRQ enabled status. Set to 1 by core when receiver mode, a new data is able to be read. When set to 1 by core, an interrupt is signaled to MPUSS. Write 1 to clear. 0x0: No data available. 0x1: Receive data available.	RW W1toClr	0
2	ARDY	Register access ready IRQ enabled status. When set to 1 it indicates that previous access has been performed and registers are ready to be accessed again. An interrupt is signaled to MPUSS. Write 1 to clear. 0x0: Module busy. 0x1: Access ready.	RW W1toClr	0
1	NACK	No acknowledgement IRQ enabled status. Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS. Write 1 to clear this bit. 0x0: Normal operation. 0x1: Not Acknowledge detected.	RW W1toClr	0
0	AL	Arbitration lost IRQ enabled status. This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to MPUSS. During reads, it always returns 0. 0x0: Normal operation. 0x1: Arbitration lost detected.	RW W1toClr	0

Table 23-35. Register Call Summary for Register I2C_IRQSTATUS

Multimaster High-Speed I2C Controller

- HS I2C Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- HS I2C Register Summary: [15] [16]

Table 23-36. I2C_IRQENABLE_SET

Address Offset	0x0000 002C
Physical Address	0x4806 002C 0x4807 002C 0x4807 202C 0x4807 A02C 0x4807 C02C
Description	Per-event interrupt enable bit vector.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE	AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE

Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR_IE	Transmit Draining interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW[XDR]. 0x0: Transmit Draining interrupt disabled 0x1: Transmit Draining interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	RDR_IE	Receive Draining interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [RDR]. 0x0: Receive Draining interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
12	RESERVED	Reserved	R	0
11	ROVR	Receive overrun enable set. 0x0: Receive overrun interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
10	XUDF	Transmit underflow enable set. 0x0: Transmit underflow interrupt disabled 0x1: Transmit underflow interrupt enabled	RW	0
9	ASS_IE	Addressed as Slave interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [AAS]. 0x0: Addressed as Slave interrupt disabled 0x1: Addressed as Slave interrupt enabled	RW	0
8	BF_IE	Bus Free interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [BF]. 0x0: Bus Free interrupt disabled 0x1: Bus Free interrupt enabled	RW	0
7	AERR_IE	Access Error interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [AERR]. 0x0: Access Error interrupt disabled 0x1: Access Error interrupt enabled	RW	0
6	STC_IE	Start Condition interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [STC]. 0x0: Start Condition interrupt disabled 0x1: Start Condition interrupt enabled	RW	0
5	GC_IE	General call Interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [GC] 0x0: General call interrupt disabled 0x1: General call interrupt enabled	RW	0
4	XRDY_IE	Transmit data ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [XRDY] 0x0: Transmit data ready interrupt disabled 0x1: Transmit data ready interrupt enabled	RW	0
3	RRDY_IE	Receive data ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTTUS_RAW [RRDY] 0x0: Receive data ready interrupt disabled 0x1: Receive data ready interrupt enabled	RW	0
2	ARDY_IE	Register access ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [ARDY] 0x0: Register access ready interrupt disabled 0x1: Register access ready interrupt enabled	RW	0
1	NACK_IE	No acknowledgement interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [NACK] 0x0: Not Acknowledge interrupt disabled 0x1: Not Acknowledge interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	AL_IE	Arbitration lost interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [AL] 0x0: Arbitration lost interrupt disabled 0x1: Arbitration lost interrupt enabled	RW	0

Table 23-37. Register Call Summary for Register I2C_IRQENABLE_SET

Multimaster High-Speed I2C Controller

- HS I2C Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- HS I2C FIFO Interrupt Mode: [14]
- HS I2C FIFO Polling Mode: [15] [16]
- HS I2C Draining Feature: [17] [18]
- Main Program: [19] [20] [21] [22] [23] [24] [25] [26] [27]
- Programming Flow Diagrams: [28]
- HS I2C Register Summary: [29] [30]

Table 23-38. I2C_IRQENABLE_CLR

Address Offset	0x0000 0030
Physical Address	0x4806 0030 0x4807 0030 0x4807 2030 0x4807 A030 0x4807 C030
Description	Per-event interrupt clear bit vector.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE	AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE

Bits	Field Name	Description	Type	Reset
15	RESERVED	Write 0s for future compatibility. Read returns 0.	RW	0
14	XDR_IE	Transmit Draining interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [XDR]. 0x0: Transmit Draining interrupt disabled 0x1: Transmit Draining interrupt enabled	RW	0
13	RDR_IE	Receive Draining interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTAUS_RAW [RDR]. 0x0: Receive Draining interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
12	RESERVED	Reserved	R	0
11	ROVR	Receive overrun enable clear. 0x0: Receive overrun interrupt disabled 0x1: Receive Draining interrupt enabled	RW	0
10	XUDF	Transmit underflow enable clear. 0x0: Transmit underflow interrupt disabled 0x1: Transmit underflow interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
9	ASS_IE	Addressed as Slave interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [AAS]. 0x0: Addressed as Slave interrupt disabled 0x1: Addressed as Slave interrupt enabled	RW	0
8	BF_IE	Bus Free interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [BF]. 0x0: Bus Free interrupt disabled 0x1: Bus Free interrupt enabled	RW	0
7	AERR_IE	Access Error interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [AERR]. 0x0: Access Error interrupt disabled 0x1: Access Error interrupt enabled	RW	0
6	STC_IE	Start Condition interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [STC]. 0x0: Start Condition interrupt disabled 0x1: Start Condition interrupt enabled	RW	0
5	GC_IE	General call Interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [GC] 0x0: General call interrupt disabled 0x1: General call interrupt enabled	RW	0
4	XRDY_IE	Transmit data ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [XRDY] 0x0: Transmit data ready interrupt disabled 0x1: Transmit data ready interrupt enabled	RW	0
3	RRDY_IE	Receive data ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTAUS_RAW [RRDY] 0x0: Receive data ready interrupt disabled 0x1: Receive data ready interrupt enabled	RW	0
2	ARDY_IE	Register access ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [ARDY] 0x0: Register access ready interrupt disabled 0x1: Register access ready interrupt enabled	RW	0
1	NACK_IE	No acknowledgement interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW [NACK] 0x0: Not Acknowledge interrupt disabled 0x1: Not Acknowledge interrupt enabled	RW	0
0	AL_IE	Arbitration lost interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_IRQSTATUS_RAW[AL] 0x0: Arbitration lost interrupt disabled 0x1: Arbitration lost interrupt enabled	RW	0

Table 23-39. Register Call Summary for Register I2C_IRQENABLE_CLR

Multimaster High-Speed I2C Controller

- HS I2C Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- HS I2C FIFO Interrupt Mode: [14]
- HS I2C Register Summary: [15] [16]

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Table 23-40. I2C_WE

Address Offset	0x0000 0034
Physical Address	0x4806 0034 0x4807 0034 0x4807 2034 0x4807 A034 0x4807 C034
Description	I2C wakeup enable vector.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF	RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL

Bits	Field Name	Description	Type	Reset
15	RESERVED	Reserved	R	0
14	XDR	Transmit Draining wakeup set. 0x0: Transmit draining wakeup disabled 0x1: Transmit draining wakeup enabled	RW	0
13	RDR	Receive Draining wakeup set. 0x0: Receive draining wakeup disabled 0x1: Receive draining wakeup enabled	RW	0
12	RESERVED	Reserved	R	0
11	ROVR	Receive overrun wakeup set. 0x0: Receive overrun wakeup disabled 0x1: Receive overrun wakeup enabled	RW	0
10	XUDF	Transmit underflow wakeup set. 0x0: Transmit underflow wakeup disabled 0x1: Transmit underflow wakeup enabled	RW	0
9	AAS	Address as slave IRQ wakeup set. 0x0: Addressed as slave wakeup disabled 0x1: Addressed as slave wakeup enabled	RW	0
8	BF	Bus Free IRQ wakeup set. 0x0: Bus Free wakeup disabled 0x1: Bus Free wakeup enabled	RW	0
7	RESERVED	Reserved	R	0
6	STC	Start Condition IRQ wakeup set. 0x0: Start condition wakeup disabled 0x1: Start condition wakeup enabled	RW	0
5	GC	General call IRQ wakeup set. 0x0: General call wakeup disabled 0x1: General call wakeup enabled	RW	0
4	RESERVED	Reserved	R	0
3	DRDY	Receive/Transmit data ready IRQ wakeup set. 0x0: Transmit/receive data ready wakeup disabled 0x1: Transmit/receive data ready wakeup enabled	RW	0
2	ARDY	Register access ready IRQ wakeup set. 0x0: Register access ready wakeup disabled 0x1: Register access ready wakeup enabled	RW	0

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Bits	Field Name	Description	Type	Reset
1	NACK	No acknowledgment IRQ wakeup set. 0x0: Not Acknowledge wakeup disabled 0x1: Not Acknowledge wakeup enabled	RW	0
0	AL	Arbitration lost IRQ wakeup set. 0x0: Arbitration lost wakeup disabled 0x1: Arbitration lost wakeup enabled	RW	0

Table 23-41. Register Call Summary for Register I2C_WE

Multimaster High-Speed I2C Controller
- HS I2C Register Summary: [0] [1]

Table 23-42. I2C_DMARXENABLE_SET

Address Offset	0x0000 0038
Physical Address	0x4806 0038 0x4807 0038 0x4807 2038 0x4807 A038 0x4807 C038
Description	Per-event DMA RX enable set.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMARX_ENABLE_SET

Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved	R	0x0000
0	DMARX_ENABLE_SET	Receive DMA channel enable set.	RW	0

Table 23-43. Register Call Summary for Register I2C_DMARXENABLE_SET

Multimaster High-Speed I2C Controller
- Main Program: [0]
- HS I2C Register Summary: [1] [2]

Table 23-44. I2C_DMATXENABLE_SET

Address Offset	0x0000 003C
Physical Address	0x4806 003C 0x4807 003C 0x4807 203C 0x4807 A03C 0x4807 C03C
Description	Per-event DMA TX enable set.
Type	RW

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMATX_ENABLE_SET

Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved	R	0x0000
0	DMATX_ENABLE_SET	Transmit DMA channel enable set.	RW	0

Table 23-45. Register Call Summary for Register I2C_DMATXENABLE_SET

Multimaster High-Speed I2C Controller
- Main Program: [0]
- HS I2C Register Summary: [1] [2]

Table 23-46. I2C_DMARXENABLE_CLR

Address Offset	0x0000 0040
Physical Address	0x4806 0040 0x4807 0040 0x4807 2040 0x4807 A040 0x4807 C040
Description	Per-event DMA RX enable clear.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMARX_ENABLE_CLEAR

Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved	R	0x0000
0	DMARX_ENABLE_CLEAR	Receive DMA channel enable clear.	RW	0

Table 23-47. Register Call Summary for Register I2C_DMARXENABLE_CLR

Multimaster High-Speed I2C Controller
- HS I2C Register Summary: [0] [1]

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Table 23-48. I2C_DMATXENABLE_CLR

Address Offset	0x0000 0044
Physical Address	0x4806 0044 0x4807 0044 0x4807 2044 0x4807 A044 0x4807 C044
Description	Per-event DMA TX enable clear.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DMATX_ENABLE_CLEAR

Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved	R	0x0000
0	DMATX_ENABLE_CLEAR	Transmit DMA channel enable clear.	RW	0

Table 23-49. Register Call Summary for Register I2C_DMATXENABLE_CLR

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-50. I2C_DMARXWAKE_EN

Address Offset	0x0000 0048
Physical Address	0x4806 0048 0x4807 0048 0x4807 2048 0x4807 A048 0x4807 C048
Description	Per-event DMA RX wakeup enable.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF	RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL

Bits	Field Name	Description	Type	Reset
15	RESERVED	Reserved	R	0
14	XDR	Transmit Draining wakeup set. 0x0: Transmit draining wakeup disabled 0x1: Transmit draining wakeup enabled	RW	0
13	RDR	Receive Draining wakeup set. 0x0: Receive draining wakeup disabled 0x1: Receive draining wakeup enabled	RW	0

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Bits	Field Name	Description	Type	Reset
12	RESERVED	Reserved	R	0
11	ROVR	Receive overrun wakeup set. 0x0: Receive overrun wakeup disabled 0x1: Receive overrun wakeup enabled	RW	0
10	XUDF	Transmit underflow wakeup set. 0x0: Transmit underflow wakeup disabled 0x1: Transmit underflow wakeup enabled	RW	0
9	AAS	Address as slave IRQ wakeup set. 0x0: Addressed as slave wakeup disabled 0x1: Addressed as slave wakeup enabled	RW	0
8	BF	Bus Free IRQ wakeup set. 0x0: Bus Free wakeup disabled 0x1: Bus Free wakeup enabled	RW	0
7	RESERVED	Reserved	R	0
6	STC	Start Condition IRQ wakeup set. 0x0: Start condition wakeup disabled 0x1: Start condition wakeup enabled	RW	0
5	GC	General call IRQ wakeup set. 0x0: General call wakeup disabled 0x1: General call wakeup enabled	RW	0
4	RESERVED	Reserved	R	0
3	DRDY	Receive/Transmit data ready IRQ wakeup set. 0x0: Transmit/receive data ready wakeup disabled 0x1: Transmit/receive data ready wakeup enabled	RW	0
2	ARDY	Register access ready IRQ wakeup set. 0x0: Register access ready wakeup disabled 0x1: Register access ready wakeup enabled	RW	0
1	NACK	No acknowledgment IRQ wakeup set. 0x0: Not Acknowledge wakeup disabled 0x1: Not Acknowledge wakeup enabled	RW	0
0	AL	Arbitration lost IRQ wakeup set. 0x0: Arbitration lost wakeup disabled 0x1: Arbitration lost wakeup enabled	RW	0

Table 23-51. Register Call Summary for Register I2C_DMARXWAKE_EN

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-52. I2C_DMATXWAKE_EN

Address Offset	0x0000 004C
Physical Address	0x4806 004C 0x4807 004C 0x4807 204C 0x4807 A04C 0x4807 C04C
Description	Per-event DMA TX wakeup enable.
Type	RW

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF	RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL

Bits	Field Name	Description	Type	Reset
15	RESERVED	Reserved	R	0
14	XDR	Transmit Draining wakeup set. 0x0: Transmit draining wakeup disabled 0x1: Transmit draining wakeup enabled	RW	0
13	RDR	Receive Draining wakeup set. 0x0: Receive draining wakeup disabled 0x1: Receive draining wakeup enabled	RW	0
12	RESERVED	Reserved	R	0
11	ROVR	Receive overrun wakeup set. 0x0: Receive overrun wakeup disabled 0x1: Receive overrun wakeup enabled	RW	0
10	XUDF	Transmit underflow wakeup set. 0x0: Transmit underflow wakeup disabled 0x1: Transmit underflow wakeup enabled	RW	0
9	AAS	Address as slave IRQ wakeup set. 0x0: Addressed as slave wakeup disabled 0x1: Addressed as slave wakeup enabled	RW	0
8	BF	Bus Free IRQ wakeup set. 0x0: Bus Free wakeup disabled 0x1: Bus Free wakeup enabled	RW	0
7	RESERVED	Reserved	R	0
6	STC	Start Condition IRQ wakeup set. 0x0: Start condition wakeup disabled 0x1: Start condition wakeup enabled	RW	0
5	GC	General call IRQ wakeup set. 0x0: General call wakeup disabled 0x1: General call wakeup enabled	RW	0
4	RESERVED	Reserved	R	0
3	DRDY	Receive/Transmit data ready IRQ wakeup set. 0x0: Transmit/receive data ready wakeup disabled 0x1: Transmit/receive data ready wakeup enabled	RW	0
2	ARDY	Register access ready IRQ wakeup set. 0x0: Register access ready wakeup disabled 0x1: Register access ready wakeup enabled	RW	0
1	NACK	No acknowledgment IRQ wakeup set. 0x0: Not Acknowledge wakeup disabled 0x1: Not Acknowledge wakeup enabled	RW	0
0	AL	Arbitration lost IRQ wakeup set. 0x0: Arbitration lost wakeup disabled 0x1: Arbitration lost wakeup enabled	RW	0

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Table 23-53. Register Call Summary for Register I2C_DMATXWAKE_EN

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-54. I2C_SYSS

Address Offset	0x0000 0090
Physical Address	0x4806 0090 0x4807 0090 0x4807 2090 0x4807 A090 0x4807 C090
Description	System Status register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															RDONE

Bits	Field Name	Description	Type	Reset
15:1	RESERVED	Reserved	R	0x0000
0	RDONE	Reset done bit Read 0x1: Reset completed Read 0x0: Internal module reset in on-going	RW	1

Table 23-55. Register Call Summary for Register I2C_SYSS

Multimaster High-Speed I2C Controller

- HS I2C Software Reset: [0] [1] [2]
- HS I2C Register Summary: [3] [4]

Table 23-56. I2C_BUF

Address Offset	0x0000 0094
Physical Address	0x4806 0094 0x4807 0094 0x4807 2094 0x4807 A094 0x4807 C094
Description	Buffer Configuration register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDMA_EN	RXFIFO_CLR	RXTRSH						XDMA_EN	TXFIFO_CLR	TXTRSH					

Bits	Field Name	Description	Type	Reset
15	RDMA_EN	Receive DMA channel enable 0x0: Receive DMA channel disabled 0x1: Receive DMA channel enabled	RW	0

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Bits	Field Name	Description	Type	Reset
14	RXFIFO_CLR	Receive FIFO clear 0x0: Normal mode 0x1: Rx FIFO is reset	RW	0
13:8	RXTRSH	Threshold value for FIFO buffer in RX mode	RW	0x00
7	XDMA_EN	Transmit DMA channel enable 0x0: Transmit DMA channel disabled 0x1: Transmit DMA channel enabled	RW	0
6	TXFIFO_CLR	Transmit FIFO clear 0x0: Normal mode 0x1: Tx FIFO is reset	RW	0
5:0	TXTRSH	Threshold value for FIFO buffer in TX mode	RW	0x00

Table 23-57. Register Call Summary for Register I2C_BUF

Multimaster High-Speed I2C Controller

- HS I2C FIFO Interrupt Mode: [0] [1] [2] [3] [4] [5]
- HS I2C FIFO DMA Mode: [6] [7] [8] [9] [10]
- HS I2C Draining Feature: [11] [12] [13] [14] [15] [16] [17] [18]
- Main Program: [19] [20] [21] [22] [23] [24] [25] [26] [27]
- Programming Flow Diagrams: [28] [29] [30] [31] [32] [33] [34] [35] [36]
- HS I2C Register Summary: [37] [38]

Table 23-58. I2C_CNT

Address Offset	0x0000 0098
Physical Address	0x4806 0098 0x4807 0098 0x4807 2098 0x4807 A098 0x4807 C098
Description	Data counter register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCOUNT															

Bits	Field Name	Description	Type	Reset
15:0	DCOUNT	Data count	RW	0x0000

Table 23-59. Register Call Summary for Register I2C_CNT

Multimaster High-Speed I2C Controller

- HS I2C Draining Feature: [0]
- Main Program: [1] [2]
- Programming Flow Diagrams: [3] [4] [5] [6] [7] [8] [9]
- HS I2C Register Summary: [10] [11]

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Table 23-60. I2C_DATA

Address Offset	0x0000 009C
Physical Address	0x4806 009C 0x4807 009C 0x4807 209C 0x4807 A09C 0x4807 C09C
Description	Data access register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DATA							

Bits	Field Name	Description	Type	Reset
15:8	RESERVED	Reserved	R	0x00
7:0	DATA	Transmit/Receive data FIFO endpoint	RW	0x--

Table 23-61. Register Call Summary for Register I2C_DATA

Multimaster High-Speed I2C Controller

- HS I2C DMA Requests: [0] [1] [2] [3] [4] [5] [6] [7]
- HS I2C System Test Mode: [8] [9]
- Main Program: [10] [11] [12] [13]
- Programming Flow Diagrams: [14] [15] [16] [17] [18] [19] [20] [21]
- HS I2C Register Summary: [22] [23]

Table 23-62. I2C_CON

Address Offset	0x0000 00A4
Physical Address	0x4806 00A4 0x4807 00A4 0x4807 20A4 0x4807 A0A4 0x4807 C0A4
Description	I2C configuration register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C_EN	RESERVED	OPMODE		STB	MST	TRX	XSA	XOA0	XOA1	XOA2	XOA3	RESERVED		STP	STT

Bits	Field Name	Description	Type	Reset
15	I2C_EN	I2C module enable. 0x0: Controller in reset. FIFO are cleared and status bits are set to their default value 0x1: Module enabled	RW	0
14	RESERVED	Reserved	R	0
13:12	OPMODE	Operation mode selection. 0x0: I2C Fast/Standard mode. 0x1: I2C High Speed mode. 0x3: Reserved. 0x2: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
11	STB	Start byte mode (master mode only). 0x0: Normal mode 0x1: Start byte mode	RW	0
10	MST	Master/slave mode. 0x0: Slave mode 0x1: Master mode	RW	0
9	TRX	Transmitter/Receiver mode (master mode only). 0x0: Receiver mode 0x1: Transmitter mode	RW	0
8	XSA	Expand Slave address. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
7	XOA0	Expand Own address 0. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
6	XOA1	Expand Own address 1. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
5	XOA2	Expand Own address 2. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
4	XOA3	Expand Own address 3. 0x0: 7-bit address mode 0x1: 10-bit address mode	RW	0
3:2	RESERVED	Reserved	R	0x0
1	STP	Stop condition (master mode only). 0x0: No action or stop condition detected 0x1: Stop condition queried	RW	0
0	STT	Start condition (master mode only). 0x0: No action or start condition detected 0x1: Start condition queried	RW	0

Table 23-63. Register Call Summary for Register I2C_CON

Multimaster High-Speed I2C Controller

- HS I2C Block Diagram: [0] [1]
- HS I2C Clocking: [2]
- HS I2C Software Reset: [3] [4] [5] [6] [7]
- HS I2C Programmable Multislave Channel Feature: [8] [9] [10] [11]
- HS I2C FIFO Interrupt Mode: [12] [13]
- HS I2C System Test Mode: [14] [15]
- Main Program: [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- Programming Flow Diagrams: [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57]
- HS I2C Register Summary: [58] [59]

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Table 23-64. I2C_OA

Address Offset	0x0000 00A8
Physical Address	0x4806 00A8 0x4807 00A8 0x4807 20A8 0x4807 A0A8 0x4807 C0A8
Description	Own address register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCODE			RESERVED					OA							

Bits	Field Name	Description	Type	Reset
15:13	MCODE	Master Code	RW	0x0
12:10	RESERVED	Reserved	R	0x0
9:0	OA	Own address	RW	0x000

Table 23-65. Register Call Summary for Register I2C_OA

Multimaster High-Speed I2C Controller

- HS I2C Automatic Blocking of the I2C Clock Feature: [0] [1]
- HS I2C Programmable Multislave Channel Feature: [2] [3]
- Main Program: [4] [5]
- Programming Flow Diagrams: [6]
- HS I2C Register Summary: [7] [8]

Table 23-66. I2C_SA

Address Offset	0x0000 00AC
Physical Address	0x4806 00AC 0x4807 00AC 0x4807 20AC 0x4807 A0AC 0x4807 C0AC
Description	Slave address register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SA							

Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved	R	0x00
9:0	SA	Slave address	RW	0x3FF

Table 23-67. Register Call Summary for Register I2C_SA

Multimaster High-Speed I2C Controller

- Main Program: [0]
- Programming Flow Diagrams: [1] [2] [3] [4] [5] [6] [7]
- HS I2C Register Summary: [8] [9]

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Table 23-68. I2C_PSC

Address Offset	0x0000 00B0
Physical Address	0x4806 00B0 0x4807 00B0 0x4807 20B0 0x4807 A0B0 0x4807 C0B0
Description	I2C Clock Prescaler Register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PSC							

Bits	Field Name	Description	Type	Reset
15:8	RESERVED	Reserved	R	0x00
7:0	PSC	Fast/Standard mode prescale sampling clock divider value 0x0: Divide by 1 0x1: Divide by 2 ..... 0xFF: Divide by 256	RW	0x00

Table 23-69. Register Call Summary for Register I2C_PSC

Multimaster High-Speed I2C Controller

- HS I2C External Clock Configuration: [0] [1]
- HS I2C Clocking: [2] [3] [4]
- HS I2C Noise Filter: [5] [6]
- HS I2C System Test Mode: [7]
- Main Program: [8]
- Programming Flow Diagrams: [9]
- HS I2C Register Summary: [10] [11]

Table 23-70. I2C_SCLL

Address Offset	0x0000 00B4
Physical Address	0x4806 00B4 0x4807 00B4 0x4807 20B4 0x4807 A0B4 0x4807 C0B4
Description	I2C SCL Low Time Register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSSCLL								SCLL							

Bits	Field Name	Description	Type	Reset
15:8	HSSCLL	High speed mode SCL low time The value of the bit field is automatically increased by 7.	RW	0x00
7:0	SCLL	Fast/standard mode SCL low time The value of the bit field is automatically increased by 7.	RW	0x00

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Table 23-71. Register Call Summary for Register I2C_SCLL

Multimaster High-Speed I2C Controller

- HS I2C Clocking: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- HS I2C System Test Mode: [9]
- Main Program: [10] [11]
- Programming Flow Diagrams: [12]
- HS I2C Register Summary: [13] [14]

Table 23-72. I2C_SCLH

Address Offset	0x0000 00B8
Physical Address	0x4806 00B8 0x4807 00B8 0x4807 20B8 0x4807 A0B8 0x4807 C0B8
Description	I2C SCL High Time Register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSSCLH								SCLH							

Bits	Field Name	Description	Type	Reset
15:8	HSSCLH	High speed mode SCL high time The value of the bit field is automatically increased by 5.	RW	0x00
7:0	SCLH	Fast/standard mode SCL high time The value of the bit field is automatically increased by 5.	RW	0x00

Table 23-73. Register Call Summary for Register I2C_SCLH

Multimaster High-Speed I2C Controller

- HS I2C Clocking: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- HS I2C System Test Mode: [10]
- Main Program: [11] [12]
- Programming Flow Diagrams: [13]
- HS I2C Register Summary: [14] [15]

Table 23-74. I2C_SYSTEST

Address Offset	0x0000 00BC
Physical Address	0x4806 00BC 0x4807 00BC 0x4807 20BC 0x4807 A0BC 0x4807 C0BC
Description	I2C System Test Register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST_EN	FREE	TMODE		SSB	RESERVED		SCL_I_FUNC	SCL_O_FUNC	SDA_I_FUNC	SDA_O_FUNC	RESERVED	SCL_I	SCL_O	SDA_I	SDA_O

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Bits	Field Name	Description	Type	Reset
15	ST_EN	System test enable. 0x0: Normal mode. All others bits in register are read only 0x1: System test enabled. Permit other system test registers bits to be set	RW	0
14	FREE	Free running mode (on breakpoint) 0x0: Stop mode (on breakpoint condition). If Master mode, it stops after completion of the ongoing bit transfer. In slave mode, it stops during the phase transfer when 1 byte is completely transmitted/received. 0x1: Free running mode	RW	0
13:12	TMODE	Test mode select. 0x0: Functional mode (default) 0x1: Reserved 0x3: Loop back mode select + SDA/SCL IO mode select 0x2: Test of SCL counters (SCLL, SCLH, PSC). SCL provides a permanent clock with master mode.	RW	0x0
11	SSB	Set status bits from 0 to 5. 0x0: No action 0x1: Set interrupt status bits to 1.	RW	0
10:9	RESERVED	Reserved	R	0x0
8	SCL_I_FUNC	SCL line input value (functional mode). Read 0x1: Read 1 from SCL line Read 0x0: Read 0 from SCL line	R	1
7	SCL_O_FUNC	SCL line output value (functional mode). Read 0x1: Driven 1 on SCL line Read 0x0: Driven 0 on SCL line	R	1
6	SDA_I_FUNC	SDA line input value (functional mode). Read 0x1: Read 1 from SDA line Read 0x0: Read 0 from SDA line	R	1
5	SDA_O_FUNC	SDA line output value (functional mode). Read 0x1: Driven 1 to SDA line Read 0x0: Driven 0 to SDA line	R	1
4	RESERVED	RESERVED	RW	0
3	SCL_I	SCL line sense input value Read 0x1: Read 1 from SCL line Read 0x0: Read 0 from SCL line	R	0
2	SCL_O	SCL line drive output value. 0x0: Write 0 to SCL line 0x1: Write 1 to SCL line	RW	0
1	SDA_I	SDA line sense input value. Read 0x1: Read 1 from SDA line Read 0x0: Read 0 from SDA line	R	0
0	SDA_O	SDA line drive output value. 0x0: Write 0 to SDA line 0x1: Write 1 to SDA line	RW	0

Table 23-75. Register Call Summary for Register I2C_SYSTEST

Multimaster High-Speed I2C Controller

- HS I2C System Test Mode: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- HS I2C Register Summary: [10] [11]

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Table 23-76. I2C_BUFSTAT

Address Offset	0x0000 00C0
Physical Address	0x4806 00C0 0x4807 00C0 0x4807 20C0 0x4807 A0C0 0x4807 C0C0
Description	I2C Buffer Status Register.
Type	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFODEPTH		RXSTAT						RESERVED		TXSTAT					

Bits	Field Name	Description	Type	Reset
15:14	FIFODEPTH	Internal FIFO buffers depth.	R	0x3
13:8	RXSTAT	RX Buffer Status	R	0x00
7:6	RESERVED	Reserved	R	0x0
5:0	TXSTAT	TX Buffer Status.	R	0x00

Table 23-77. Register Call Summary for Register I2C_BUFSTAT

Multimaster High-Speed I2C Controller

- HS I2C FIFO Management: [0]
- HS I2C Draining Feature: [1] [2] [3] [4] [5] [6] [7] [8]
- Programming Flow Diagrams: [9] [10] [11] [12] [13] [14] [15] [16]
- HS I2C Register Summary: [17] [18]

Table 23-78. I2C_OA1

Address Offset	0x0000 00C4
Physical Address	0x4806 00C4 0x4807 00C4 0x4807 20C4 0x4807 A0C4 0x4807 C0C4
Description	I2C Own Address 1 Register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OA1							

Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved	R	0x00
9:0	OA1	Own address 1	RW	0x000

Table 23-79. Register Call Summary for Register I2C_OA1

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

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Table 23-80. I2C_OA2

Address Offset	0x0000 00C8
Physical Address	0x4806 00C8 0x4807 00C8 0x4807 20C8 0x4807 A0C8 0x4807 C0C8
Description	I2C Own Address 2 Register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OA2							

Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved	R	0x00
9:0	OA2	Own address 2	RW	0x000

Table 23-81. Register Call Summary for Register I2C_OA2

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-82. I2C_OA3

Address Offset	0x0000 00CC
Physical Address	0x4806 00CC 0x4807 00CC 0x4807 20CC 0x4807 A0CC 0x4807 C0CC
Description	I2C Own Address 3 Register
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OA3							

Bits	Field Name	Description	Type	Reset
15:10	RESERVED	Reserved	R	0x00
9:0	OA3	Own address 3	RW	0x000

Table 23-83. Register Call Summary for Register I2C_OA3

Multimaster High-Speed I2C Controller

- HS I2C Register Summary: [0] [1]

Table 23-84. I2C_ACTOA

Address Offset	0x0000 00D0
Physical Address	0x4806 00D0 0x4807 00D0 0x4807 20D0 0x4807 A0D0 0x4807 C0D0
Description	I2C Active Own Address Register.
Type	R

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												OA3_ACT	OA2_ACT	OA1_ACT	OA0_ACT

Bits	Field Name	Description	Type	Reset
15:4	RESERVED	Reserved	R	0x000
3	OA3_ACT	Own Address 3 active. Read 0x1: Own Address active. Read 0x0: Own Address inactive.	R	0
2	OA2_ACT	Own Address 2 active. Read 0x1: Own Address active. Read 0x0: Own Address inactive.	R	0
1	OA1_ACT	Own Address 1 active. Read 0x1: Own Address active. Read 0x0: Own Address inactive.	R	0
0	OA0_ACT	Own Address 0 active. Read 0x1: Own Address active. Read 0x0: Own Address inactive.	R	0

Table 23-85. Register Call Summary for Register I2C_ACTOA

Multimaster High-Speed I2C Controller

- HS I2C Programmable Multislave Channel Feature: [0]
- HS I2C Register Summary: [1] [2]

Table 23-86. I2C_SBLOCK

Address Offset	0x0000 00D4
Physical Address	0x4806 00D4 0x4807 00D4 0x4807 20D4 0x4807 A0D4 0x4807 C0D4
Description	I2C Clock Blocking Enable Register.
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												OA3_EN	OA2_EN	OA1_EN	OA0_EN

Bits	Field Name	Description	Type	Reset
15:4	RESERVED	Reserved	R	0x000
3	OA3_EN	Enable I2C Clock Blocking for Own Address 3. 0x0: I2C Clock Released. 0x1: I2C Clock Blocked.	RW	0
2	OA2_EN	Enable I2C Clock Blocking for Own Address 2. 0x0: I2C Clock Released. 0x1: I2C Clock Blocked.	RW	0

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Bits	Field Name	Description	Type	Reset
1	OA1_EN	Enable I2C Clock Blocking for Own Address 1. 0x0: I2C Clock Released. 0x1: I2C Clock Blocked.	RW	0
0	OA0_EN	Enable I2C Clock Blocking for Own Address 0. 0x0: I2C Clock Released. 0x1: I2C Clock Blocked.	RW	0

Table 23-87. Register Call Summary for Register I2C_SBLOCK

Multimaster High-Speed I2C Controller

- HS I2C Automatic Blocking of the I2C Clock Feature: [0]
- HS I2C Register Summary: [1] [2]

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23.2 HDQ1W

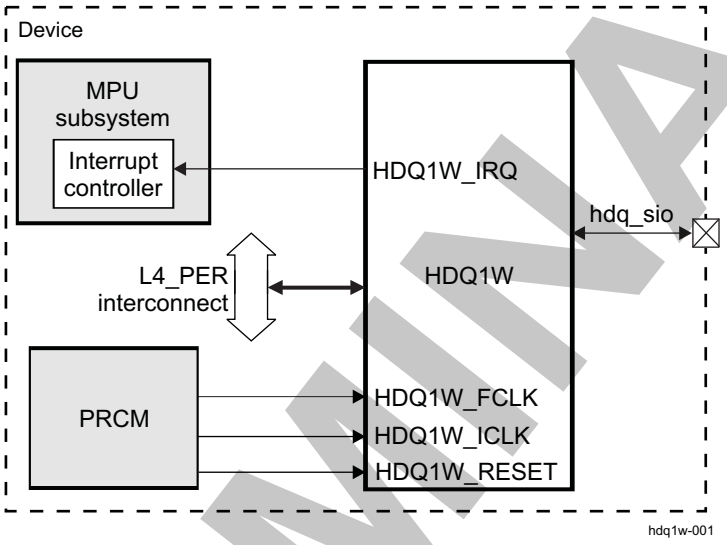
This section describes the HDQ™/1-Wire® interface for the device.

23.2.1 HDQ1W Overview

The HDQ1W module implements the hardware protocol of the master functions of the TI/Benchmarq HDQ and the Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire for communication between the master (HDQ1W controller) and the slaves (HDQ/1-Wire external compliant devices).

Figure 23-30 shows the HDQ1W.

Figure 23-30. HDQ1W Overview



The HDQ1W has a generic L4 interface and is intended to be used in an interrupt-driven fashion. The 1-pin interface is implemented as an open-drain output at the device level.

The main features supported by the HDQ1W are the following:

- Benchmarq HDQ protocol
- Dallas Semiconductor 1-Wire protocol
- Power-down mode

The HDQ1W provides a communication rate of 5 Kbps over an address space of 128 bytes.

A typical application of the HDQ1W is the communication with battery monitor (gas gauge) integrated circuits.

23.2.2 HDQ1W Environment

23.2.2.1 HDQ1W Functional Modes

The HDQ1W has two main modes: HDQ and 1-Wire. Each of these modes includes idle, active, and power-down submodes. Table 23-88 lists the HDQ1W functional modes, and Figure 23-31 shows an overview of a typical application.

Table 23-88. Functional Modes

Functions	Description
HDQ	Benchmarq HDQ protocol
1-Wire	Dallas Semiconductor 1-Wire protocol

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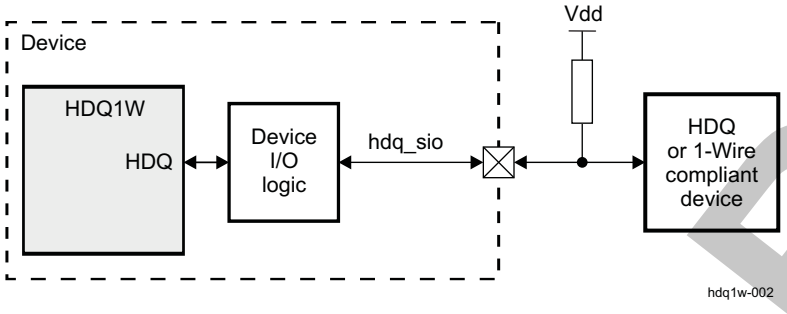
Figure 23-31. HDQ1W Typical Application System Overview



An external pullup is required, because the two protocols use a return-to-1 mechanism (that is, after any command by any of the connected devices, the line is pulled to a logical high level).

The HDQ1W operates according to a command structure that is programmed into transmit command registers (as described in Section 23.2.5.1.2, *HDQ1W Low-level Programming Model*).

The 1-Wire mode runs at slower speeds than the capabilities of the mode.

Table 23-89 describes the external signal of the HDQ/1-Wire compliant module.

Table 23-89. I/O Description

Signal	I/O[1]	Description	Value at Reset
hdq_sio	I/O	Serial data input/output. Output is open drain type.	HiZ (pulled to 1 by pullup)

(1) I = Input; O = Output

NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The control module registers assign the specific function to the device pads. For more information on control module settings, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, of *Chapter 18, Control Module*.

23.2.2.2 HDQ and 1-Wire (SDQ) Protocols

23.2.2.2.1 HDQ Protocol Initialization (Default)

In HDQ mode, the firmware does not require the host to create an initialization pulse to the slave. However, the slave can be reset by using an initialization pulse (also referred to as a break pulse). The initialization pulse is generated by setting the HDQ_CTRL_STATUS[2] INITIALIZATION bit and then setting the HDQ_CTRL_STATUS[4] GO bit. The slave does not respond with a presence pulse as it does in the 1-Wire protocol.

The HDQ is a command-based protocol in which the host sends a command byte to the slave. The command directs the slave either to store the next eight bits of data received to a register specified by the command byte (write operation) or to output the eight bits of data from a register specified by the command byte (read operation). The master implementation is a simple byte engine. Sending of the ID, command/address, and data is controlled by firmware. The master engine provides only a single HDQ_TX_DATA register.

The command and data bytes consist of a stream of eight bits with a maximum transmission rate of 5 Kbps. The least-significant bit (LSB) of a command or data byte is transmitted first. If a communication time-out occurs between the host and the slave (for example, if the host waits longer than the specified time for the slave to respond, or if this is the first access command), then the host must send an initialization pulse (BREAK) before sending the command again.

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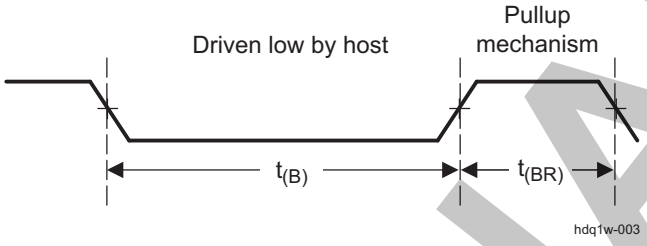
The slave detects a break when the HDQ pin is driven to a logic-low state for a specified break time t(B) or greater. The HDQ pin then returns to its normal ready-high logic state for a specified break-recovery time t(BR). The slave is then ready for a command from the host processor. Figure 23-32 shows this behavior.

An interrupt condition indicates a TX-complete, an RX-complete, or a time-out condition. Reading the interrupt status register clears all interrupt conditions. Only one interrupt signal is sent to the microcontroller, and only one overall mask bit can enable or disable the interrupt. The interrupt conditions cannot be individually masked.

Figure 23-32. HDQ Break-Pulse Timing Diagram

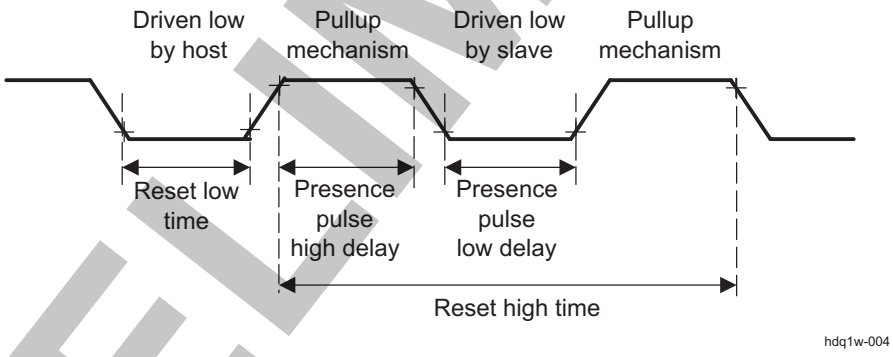


23.2.2.2.2 1-Wire (SDQ) Protocol Initialization

In 1-Wire (SDQ) protocol, the host first sends an initialization pulse (by pulling the line to a logic-low state) and then waits for the slave to respond with a presence pulse before enabling any communication sequence.

As for the initialization pulse, the presence pulse is a low-level pulse on the line initiated by the slave. The timing diagram in Figure 23-33 shows the 1-Wire (SDQ) reset sequence.

Figure 23-33. 1-Wire (SDQ) Reset Timing Diagram



The host drives the line to a logic-low state for a minimum of reset low time. Once the slave detects this pulse, it must drive the line to a logic-low state within the presence pulse high delay for a minimum period of presence pulse low time.

If the slave does not respond within this interval of time, a time-out event occurs and no transaction can be initiated. The host must initiate the reset sequence again before sending any command to the slave.

On the other hand, if the slave sends back its presence pulse within the specified time interval, the communication can be enabled after the reset high time.

23.2.2.2.3 Communication Sequence (HDQ and 1-Wire Protocols)

The description in this section applies to both protocols.

After a successful break pulse (HDQ mode) or initialization sequence (1-Wire protocol), the host and slave are ready for bit transmission. Each bit to transmit (either from the host to the slave or from the slave to the host) is preceded by a low-going edge on the line, as shown in Figure 23-34.

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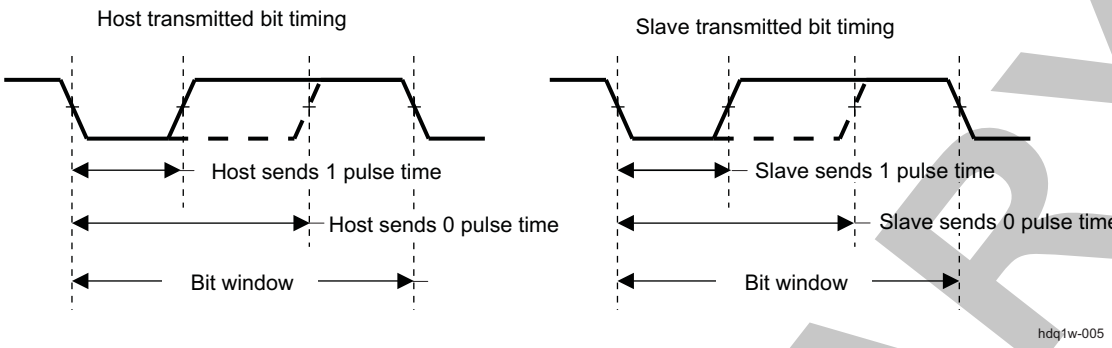
Figure 23-34. HDQ1W Transmitted Bit Timing



The return-to-1 data-bit frame consists of three distinct sections. The first section starts the transmission when either the slave or the host takes the line to a logic-low state. The next section is the actual data transmission in which the data must be valid during a specified period of time after the negative edge that starts the communication. The final section stops the transmission by returning the HDQ/1-Wire line to a logic-high state. Communication with an HDQ/1-Wire slave always occurs with the LSB being transmitted first.

The command byte of the HDQ/1-Wire protocols consists of eight contiguous valid command bits. The command byte contains two fields: R/W command and address. The R/W bit of the command byte determines whether the command is a read or a write, and the address field containing bits AD6-AD0 indicates the address to be read or written. Table 23-90 lists the command byte values.

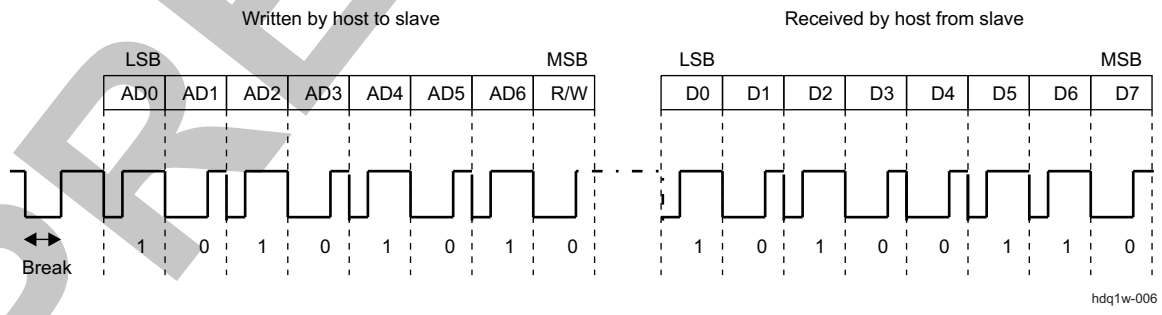
Table 23-90. HDQ/1-Wire Command Byte

7	6	5	4	3	2	1	0
R/W	AD6	AD5	AD4	AD3	AD2	AD1	AD0

R/W Indicates whether the command byte is a read or a write. A 1 indicates a write command; the following eight bits must be written to the register specified by the address field of the command byte. A 0 indicates that the command is a read. On a read command, the slave outputs the requested register contents.

AD6-AD0 Represent the seven bits labeled AD6-AD0 containing the address portion of the register to be accessed.
The communication sequence example in Figure 23-35 shows a read command at address 0x55; the received data is 0x65.

Figure 23-35. HDQ/1-Wire Communication Sequence



23.2.3 HDQ1W Integration

Figure 23-36 shows HDQ1W integration in the device.

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Figure 23-36. HDQ1W Integration

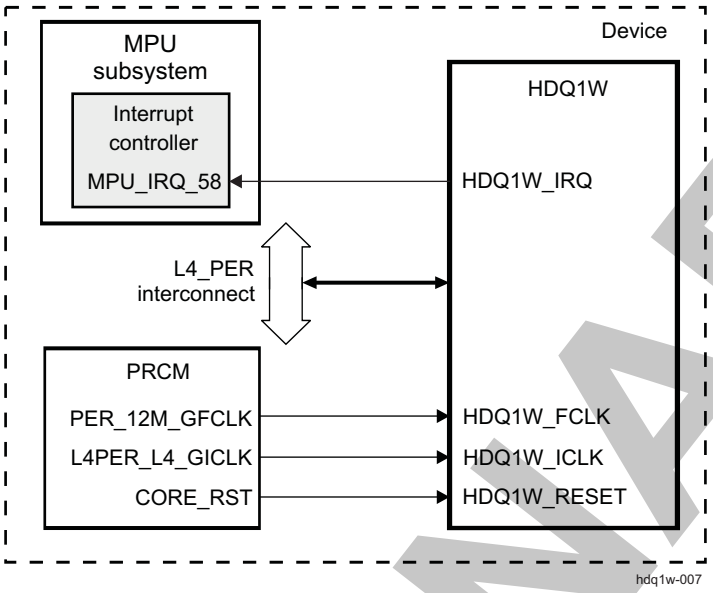

Table 23-91 through Table 23-93 summarize the integration of the module in the device.

Table 23-91. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
HDQ1W	PD_CORE	No	L4_PER

Table 23-92. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HDQ1W	HDQ1W_ICLK	L4PER_L4_GICLK	PRCM	Interface clock
HDQ1W	HDQ1W_FCLK	PER_12M_GFCLK	PRCM	Functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HDQ1W	HDQ1W_RESET	CORE_RST	PRCM	HDQ1W reset signal

Table 23-93. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
HDQ1W	HDQ1W_IRQ	MPU_IRQ_58	MPU	Interrupt to the MPU subsystem interrupt controller (INTC).

NOTE: For the description of the interrupt source, see Section 17.4.1, *INTC_MPU Functional Description*, in chapter *Interrupt Controllers*.

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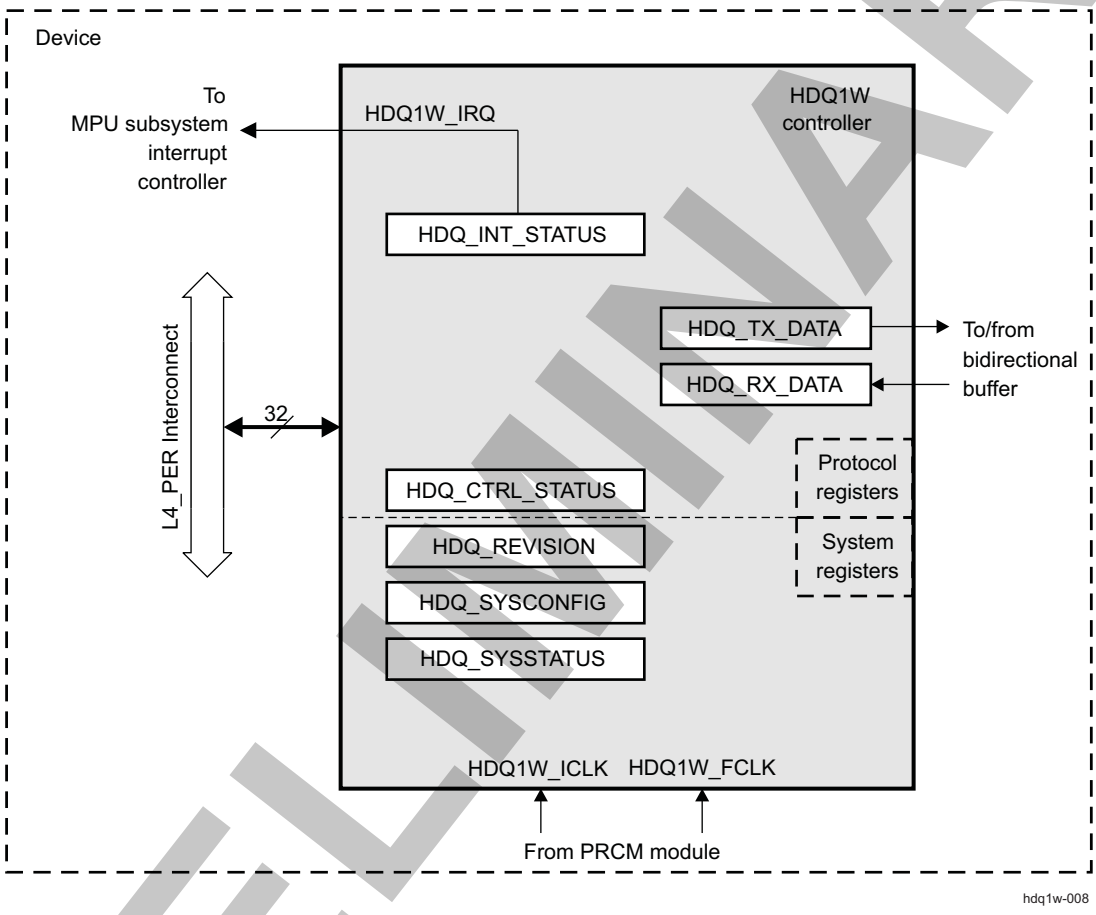
23.2.4 HDQ1W Functional Description

The HDQ1W works with HDQ and 1-Wire protocols. The protocols use a single wire to establish communication between the master and the slave. Both protocols use a return-to-1 mechanism; that is, after any command is driven, the line is pulled to a high level. This mechanism requires an external pullup.

23.2.4.1 HDQ1W Block Diagram

Figure 23-37 is the HDQ1W block diagram.

Figure 23-37. HDQ1W Block Diagram



The HDQ_CTRL_STATUS[0] MODE bit allows selection between the HDQ and 1-Wire protocols. This bit is assumed static for design purposes. The configuration is in HDQ mode by default.

Figure 23-38 shows the protocol-dedicated register scheme.

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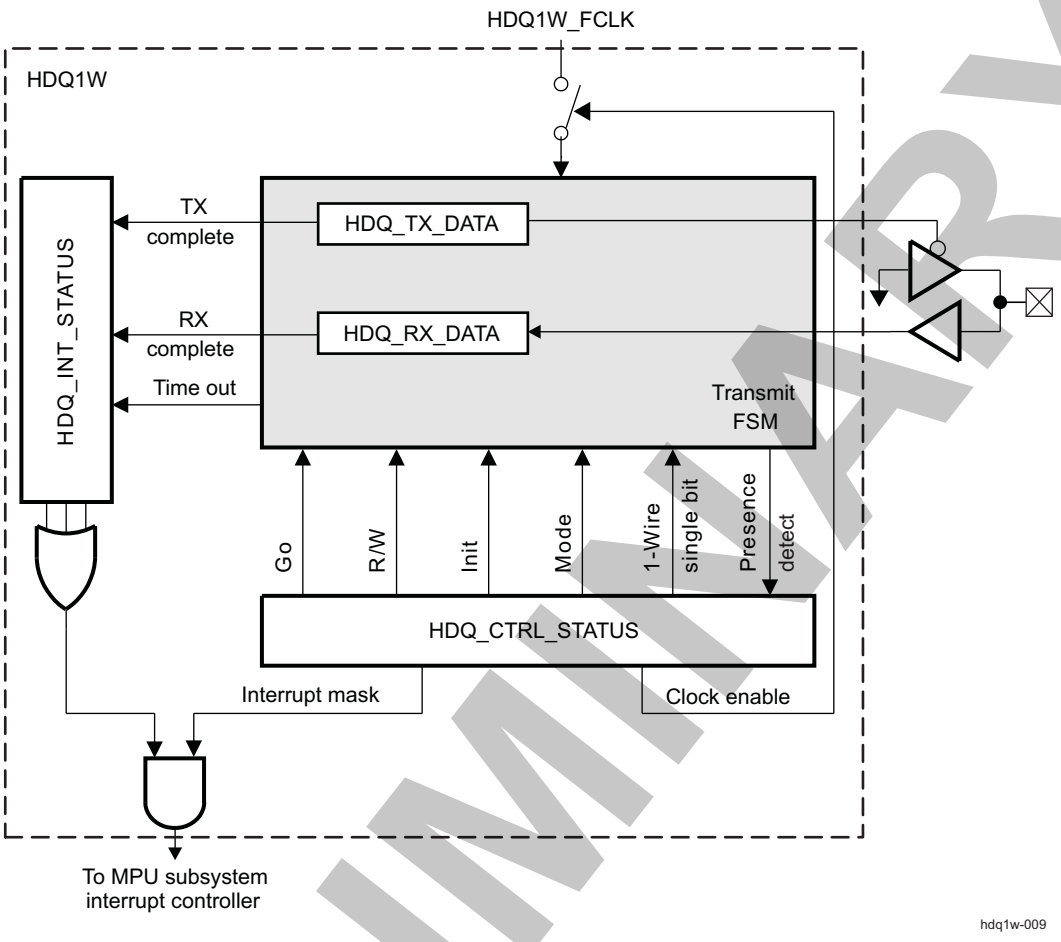
Figure 23-38. Protocol Registers Description



The receive and transmit operations of the HDQ1W module are performed with respect to the timing of the slower HDQ protocol. When the 1-Wire protocol is used, it runs at lower speed than its full capabilities, but is still able to meet the timing requirements and practical considerations.

23.2.4.2 HDQ1W Clocking Configuration

23.2.4.2.1 HDQ1W Clocks

The HDQ1W module operates from two clocks: a functional clock (HDQ1W_FCLK) and an interface clock (HDQ1W_ICLK). When these clocks are set in the PRCM module, the following rule must be observed: HDQ1W_ICLK ≥ HDQ1W_FCLK.

- The HDQ1W_FCLK functional clock is a fixed clock provided by the PRCM module. It is used to clock the internal module logic.

  For more information about the clock and the PRCM register settings, see Section 3.6.15, *CD_L4_PER Clock Domain*, in chapter *Power, Reset, and Clock Management*.

  When the HDQ1W no longer requires the HDQ1W_FCLK, the software can disable it at the PRCM level. The clock is effectively cut, provided the other modules that receive it do not require it either.
- The HDQ1W_ICLK interface clock runs at L4 interconnect clock speed and is used to trigger access to the HDQ1W L4 interface.

  When the HDQ1W no longer requires the HDQ1W_ICLK (no transfer is in progress), the software can disable it at the PRCM level. The clock is effectively cut, provided the other modules that receive it do not require it either.

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23.2.4.3 HDQ1W Hardware and Software Reset

Global reset of the module is done at the power, reset, and clock management (PRCM) module level (for more information, see Section 3.6.15, *CD_L4_PER Clock Domain*) or by setting the HDQ_SYSCONFIG[1] SOFTRESET bit to 1. Setting this bit enables an active software reset functionality equivalent to a hardware reset. The HDQ1W_FCLK functional clock must be enabled from the PRCM level and locally through the HDQ_CTRL_STATUS[5] CLOCKENABLE bit (set to 1) for the software reset to complete.

23.2.4.4 HDQ1W Power Management

Table 23-94 describes power-management features available to the HDQ1W.

Table 23-94. Local Power-Management Features

Feature	Registers	Description
Clock auto gating	HDQ_SYSCONFIG [0] AUTOIDLE bit	Auto-idle mode
Slave idle modes	N/A	N/A
Clock enable	HDQ_CTRL_STATUS[5] CLOCKENABLE bit	Power-down mode
Master standby modes	N/A	N/A
Global wake-up enable	N/A	N/A
Wake-up sources enable	N/A	N/A

23.2.4.4.1 Auto-Idle Mode

The HDQ1W provides an auto-idle function in its interconnect clock domain.

The interconnect clock auto-idle power-saving mode is enabled or disabled through the HDQ_SYSCONFIG[0] AUTOIDLE bit. When this mode is enabled and there is no activity on the interconnect interface, the interconnect clock (HDQ1W_ICLK) is disabled inside the module, thereby reducing power consumption. When there is new activity on the interconnect interface, the interconnect clock is restarted with no latency penalty. This mode is disabled by default after a reset.

The auto-idle mode can be enabled in order to reduce power consumption.

23.2.4.4.2 Power-Down Mode

The HDQ1W also provides a power-saving function in its functional clock domain.

Setting the CLOCKENABLE bit in the control and status register (HDQ_CTRL_STATUS[5] CLOCKENABLE bit) to 0 shuts off the functional clock (HDQ1W_FCLK) to the state-machine. The state-machine is reset when the functional clock is disabled; if any transaction is ongoing, it is aborted into the reset state.

Before shutting off the functional clock, the software must wait for transaction-complete interrupt. In write operation the software must check whether the interrupt was generated after address/command byte was sent or after data byte was sent. The functional clock must not be shut off after address/command byte is sent; otherwise, the data is not written to the slave.

The register values are not affected by disabling the functional clock.

CAUTION

There is no hardware mechanism to prevent cutting off the HDQ1W clocks while the module is performing a transfer. This would result in loss of data being transferred.

23.2.4.5 HDQ Interrupt Requests

The HDQ1W can generate one interrupt:

- HDQ1W_IRQ: This is an interrupt to the MPU subsystem INTC. It is mapped on MPU_IRQ_58.

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Table 23-95 lists the events that can generate this interrupt.

Table 23-95. Events

Event Flag	Event Mask	Sync	Sensitivity	Description
HDQ_INT_STATUS[2] TXCOMPLETE	HDQ_CTRL_STATUS[31] INTERRUPTMASK	Yes	Level	A write operation of one byte was completed.
HDQ_INT_STATUS[1] RXCOMPLETE	HDQ_CTRL_STATUS[31] INTERRUPTMASK	Yes	Level	A byte has been successfully read.
HDQ_INT_STATUS[0] TIMEOUT	HDQ_CTRL_STATUS[31] INTERRUPTMASK	Yes	Level	After a read command initiated by the host, the slave did not pull the line low within the specified time.

23.2.4.6 HDQ Mode (Default)

23.2.4.6.1 HDQ Mode Features

The HDQ mode supports the following:

- Benchmarq HDQ protocol
- Power-down mode

23.2.4.6.2 Description

In the HDQ mode, there is no need for the host to create an initialization pulse to the slave. However, the host can reset the slave by using an initialization pulse (also known as a break pulse). Setting the HDQ_CTRL_STATUS[2] INITIALIZATION bit and then setting the HDQ_CTRL_STATUS[4] GO bit creates this pulse by pulling the line down for a defined duration. When the slave receives the pulse, it is ready for communication but does not respond with a presence pulse.

In a typical write operation, two bytes are sent to the slave. The first byte corresponds to the command/address byte, and the second byte corresponds to the data to be written.

In a typical read operation, the host sends a command/address byte and the slave returns a byte of data.

The master is implemented to send and receive bytes. Sending the command/address and data is controlled by the firmware. The master provides only a single data TX register.

The HDQ protocol is a return-to-1 protocol. Consequently, after a byte is sent to the slave (either command/address + data for a write, or just command/address for a read), the host pulls the line up. The line is set to the high-impedance state in the device and an external pullup brings it to a logical high level.

In the case of a read operation, the slave also drives the line to a logic-low state before sending the requested data.

If the host initiates a read and does not receive data within a specified interval of time (that is, the slave does not drive the line low within this interval), the HDQ_INT_STATUS[0] TIMEOUT bit is set, thereby indicating a read failure. The TIMEOUT bit remains set until the host reads the interrupt status register (HDQ_INT_STATUS).

An interrupt condition indicates either a TX-complete, an RX-complete, or a time-out on a transaction. The corresponding bit is set in the interrupt status register (HDQ_INT_STATUS). This register is cleared as soon as it is read.

Only one interrupt signal is sent to the MPU, and only an overall mask can enable or disable the interrupts. These interrupts cannot be individually masked.

23.2.4.6.3 Single-Bit Mode

In HDQ mode, the single-bit mode (HDQ_CTRL_STATUS[7] ONE_WIRE_SINGLE_BIT bit set to 1) has no effect because the HDQ protocol supports only byte transfers.

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23.2.4.6.4 Interrupt Conditions

The HDQ1W provides the following interrupt status:

- Transmission complete:

  A write operation of one byte was completed. Successful or failed completion is not indicated, because there is no acknowledgment from the slave in HDQ protocol. This interrupt condition is cleared by reading the interrupt status register (HDQ_INT_STATUS).

- Read complete:

  In HDQ mode, the interrupt status indicates that a byte has been successfully read. This interrupt condition is cleared by reading the interrupt status register (HDQ_INT_STATUS).

- Presence detect/time-out:

  In HDQ mode, the interrupt status indicates that after a read command initiated by the host, the slave did not pull the line low within the specified time. This interrupt condition is cleared by reading the interrupt status register (HDQ_INT_STATUS).

  In HDQ mode, a time-out condition is also used to indicate the successful completion of a break pulse. That is, if the master has sent the break pulse, it is indicated with a time-out instead of a TX-complete.

Only one interrupt is generated to the MPU based on any of these interrupt conditions. A read operation on the interrupt status register clears all the interrupt status bits that were previously set.

23.2.4.7 1-Wire Mode

23.2.4.7.1 1-Wire Mode Features

The 1-Wire mode supports the following:

- Dallas Semiconductor 1-Wire protocol
- Power-down mode
- Single-bit mode

23.2.4.7.2 Description

The 1-Wire mode requires an initialization pulse to be sent to the slave(s) connected on the interface. If a slave is present, it responds with a presence pulse.

The initialization pulse is sent when the HDQ_CTRL_STATUS[2] INITIALIZATION bit is set and the HDQ_CTRL_STATUS[4] GO bit is set afterwards.

When the slave receives the initialization pulse, it sends back its presence pulse by pulling down the line for a defined duration. The module detects this low-level pulse and sets the HDQ_CTRL_STATUS[3] PRESENCEDETECT bit.

In a similar way, if a presence pulse is not received from the slave after an initialization pulse is sent, the PRESENCEDETECT bit remains cleared.

Whether or not a presence pulse is detected after an initialization pulse is sent, the HDQ_INT_STATUS[0] TIMEOUT bit is set and an interrupt condition is generated.

In 1-Wire mode, the generated interrupt condition means the maximum time allowed for receiving the response has elapsed and the software must check the PRESENCEDETECT bit to determine whether or not there was a presence pulse.

The INITIALIZATION bit is cleared at the end of the initialization pulse at the same time as the TIMEOUT bit is set. The TIMEOUT bit is cleared when the interrupt status register (HDQ_INT_STATUS) is read.

For read operations, 1-Wire is a bit-by-bit protocol, which means the slave must be clocked by the host for each bit of the byte to read.

The line is pulled up at the end of the command/address byte. On the first read, the host creates a low-going edge to initiate a bit read. The line is then pulled up (pulled to the high-impedance state by the host and set to a high logical level by the external pullup) and the slave either drives the line low to transmit a 0, or does not drive the line to transmit a 1. This sequence is repeated for each bit to read.

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The first bit the host receives is the LSB, and the last bit is the most-significant bit (MSB) in the receive data register (HDQ_RX_DATA).

An interrupt condition indicates either a TX-complete, an RX-complete, or a time-out condition (that is, the time allowed for the slave to indicate its presence has elapsed). A read operation on the interrupt status register clears the interrupt conditions previously set. As in the HDQ mode, only one interrupt signal is sent to the MPU. Only an overall mask bit can enable or disable the interrupt (the interrupt conditions cannot be masked individually).

23.2.4.7.3 1-Wire Single-Bit Mode Operation

A single-bit mode can be entered by setting the appropriate bit in the control and status register (ONE_WIRE_SINGLE_BIT bit HDQ_CTRL_STATUS[7]). In this mode, only one bit of data at a time is transferred between the master and the slave. After the bit is transferred, an interrupt is generated (that is, there is an RX-complete for a read operation and a TX-complete for a write operation). The ONE_WIRE_SINGLE_BIT bit is cleared by hardware after every single bit is received. Software must set this bit to re-enable reception in single-bit mode. Bit 0 of the RX register (HDQ_RX_DATA) is updated each time a bit is received from the slave; bit 0 of the TX register (HDQ_TX_DATA) contains the bit to be sent.

23.2.4.7.4 Interrupt Conditions

The HDQ1W provides the following interrupt status:

- Transmission complete:

  A write operation of one byte was completed. Successful or failed completion is not indicated, because there is no acknowledgment from the slave in 1-Wire protocol. This interrupt condition is cleared by reading the interrupt status register (HDQ_INT_STATUS).
- Read complete:

  In 1-Wire mode, the interrupt status indicates that a byte has been successfully read. This interrupt condition is cleared by reading the interrupt status register (HDQ_INT_STATUS).
- Presence detect/time-out:

  In 1-Wire mode, the interrupt status indicates that it is now valid to check the PRESENCEDETECT bit. This interrupt condition is cleared by reading the interrupt status register (HDQ_INT_STATUS).

Only one interrupt is generated to the MPU based on any of these interrupt conditions. A read operation on the interrupt status register clears all interrupt status bits that were previously set.

23.2.4.7.5 Status Flags

The presence-condition-detected status flag is contained in the HDQ_CTRL_STATUS[3] PRESENCEDETECT bit. This is valid only in 1-Wire mode. The flag is updated when the HDQ_INT_STATUS[0] TIMEOUT bit is set. Therefore, its correct value shows only after the interrupt is generated. The firmware must wait for the time-out condition; otherwise, the flag keeps its previous value and is undefined.

23.2.4.8 BITFSM Delay

The return-to-one mechanism on the HDQ/1-Wire bus is a simple pull-up resistor. Consequently, an excessive wire load of the HDQ/1-Wire bus can cause a significant delay to the bus rise time. This can prevent the module state machine from working correctly by reading back an improper value caused by the line delay. To correct such condition by software, it is possible to configure the HDQ_CTRL_STATUS[10:8] BITFSM register bitfield with the expected line delay. This way the module state machine waits the proper time interval, before reading back the line value. The delay can be adjusted in 1.33 µs steps. The default value of BITFSM = 0x0 corresponds to 1.33 µs delay.

Bus delay can be calculated as follows: $T_{delay} \sim= 2.2 \times R_{pullup} \times C_{line}$

See more information in the *Device Data Manual*.

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23.2.5 HDQ1W Low-Level Programming Model

This section describes the low-level hardware programming sequences for configuration and usage of the module. The basic protocol functions, such as slave initialization (reset), read-byte, and write-byte operations, are described. For a description of the high-level functions, see the HDQ/1-Wire protocol documentation and the slave device datasheet.

23.2.5.1 Global Initialization

23.2.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the HDQ1W module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the HDQ1W. Refer to the HDQ1W Module Integration and Environment Sections for further information.

Table 23-96. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. The interface clock must not be slower than the functional clock (HDQ1W_ICLK ≥ HDQ1W_FCLK). For more information about the module configuration, see Section 3.1.1, *Power, Reset, and Clock Management*.
Control Module	Module specific pad muxing and pullup must be set in the control module. For more information about the module configuration, see Figure 18-1, *Control Module*.
MPU INTC	MPU INTC configuration must be done to enable the interrupts from HDQ1W module. See Section 17.4.1, *INTC_MPU Functional Description,* in Section 17.1, *Interrupt Controllers*.

23.2.5.1.2 HDQ1W Module Global Initialization

Table 23-97. HDQ1W Module Global Initialization

Step	Register/Bit Field/Programming Model	Value
Initiate software reset.	HDQ_SYSCONFIG[1] SOFTRESET	0x1
Disable power-down mode.	HDQ_CTRL_STATUS[5] CLOCKENABLE	0x1
Wait until reset complete?	HDQ_SYSSTATUS[0] RESETDONE	= 0x1
Disable power-down mode.	HDQ_CTRL_STATUS[5] CLOCKENABLE	0x1
Configure auto-idle mode.	HDQ_SYSCONFIG[0] AUTOIDLE	x

23.2.5.2 HDQ Operational Modes Configuration

23.2.5.2.1 Main Sequence - HDQ Write Operation Mode

Table 23-98. HDQ Mode Selection

Step	Register/Bit Field/Programming Model	Value
Select HDQ mode.	HDQ_CTRL_STATUS[0] MODE	0x0
Enable interrupt generation.	HDQ_CTRL_STATUS[6] INTERRUPTMASK	0x1
Initialize HDQ slave.	See Section 23.2.5.2.2.1	

Table 23-99. HDQ Write Operation Mode

Step	Register/Bit Field/Programming Model	Value
Write command/address or data value.	HDQ_TX_DATA[7:0]	0x-
Select write operation.	HDQ_CTRL_STATUS[1] DIR	0x0

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Table 23-99. HDQ Write Operation Mode (continued)

Step	Register/Bit Field/Programming Model	Value
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		
Reading HDQ_INT_STATUS clears interrupt conditions.	HDQ_INT_STATUS[2] TXCOMPLETE	0x1

23.2.5.2.2 Main Sequence - HDQ Read Operation Mode

23.2.5.2.2.1 Sub-sequence - Initialize HDQ Slave

Table 23-100. HDQ Read Operation Mode

Step	Register/Bit Field/ Programming Model	Value
Select read operation.	HDQ_CTRL_STATUS[1] DIR	0x1
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		
Read and store HDQ_INT_STATUS. Reading HDQ_INT_STATUS clears interrupt conditions.	HDQ_INT_STATUS	0x-
IF: Read operation successful?	HDQ_INT_STATUS[1] RXCOMPLETE HDQ_INT_STATUS[0] TIMEOUT	= 0x1 = 0x0
Get received data.	HDQ_RX_DATA[7:0]	0x-
ENDIF		

Table 23-101. Initialize HDQ Slave

Step	Register/Bit Field/Programming Model	Value
Send Initialization Pulse	HDQ_CTRL_STATUS[2] INITIALIZATION	0x1
Send Command	HDQ_CTRL_STATUS[4] GO	0x1

23.2.5.3 1-Wire Operational Modes Configuration

23.2.5.3.1 Main Sequence - 1-Wire Write Operation Mode

Table 23-102. 1-Wire Mode Selection

Step	Register/Bit Field/Programming Model	Value
Reset HDQ1W module.	See Section 23.2.5.1.2.	
Select 1-Wire mode.	HDQ_CTRL_STATUS[0] MODE	0x1
Enable interrupt generation.	HDQ_CTRL_STATUS[6] INTERRUPTMASK	0x1
Initialize 1-Wire slave, check for slave presence.	See Section 23.2.5.3.3.	

Table 23-103. 1-Wire Write Operation Mode

Step	Register/Bit Field/ Programming Model	Value
Write ID/command or data value.	HDQ_TX_DATA[7:0]	0x-
Select write operation.	HDQ_CTRL_STATUS[1] DIR	0x0
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		
Reading HDQ_INT_STATUS clears interrupt conditions.	HDQ_INT_STATUS[2] TXCOMPLETE	0x1

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23.2.5.3.2 Main Sequence - 1-Wire Read Operation Mode

Table 23-104. 1-Wire Read Operation Mode

Step	Register/Bit Field/Programming Model	Value
Select read operation.	HDQ_CTRL_STATUS[1] DIR	0x1
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		
Read and store HDQ_INT_STATUS. Reading HDQ_INT_STATUS clears interrupt conditions.	HDQ_INT_STATUS	0x-
IF: Read operation successful?	HDQ_INT_STATUS[1] RXCOMPLETE	= 0x1
Get received data.	HDQ_RX_DATA[7:0]	0x-
ENDIF		

23.2.5.3.3 Sub-sequence - Initialize 1-Wire Slave

Table 23-105. Initialize 1-Wire Slave

Step	Register/Bit Field/Programming Model	Value
Select sending initialization pulse operation.	HDQ_CTRL_STATUS[2] INITIALIZATION	0x1
Start operation.	HDQ_CTRL_STATUS[4] GO	0x1
Wait for interrupt.		
IF: Presence pulse detected?	HDQ_INT_STATUS[0] TIMEOUT HDQ_CTRL_STATUS[3] PRESENCEDETECT	= 0x1 = 0x1
Slave is present and initialized.		
ELSE		
Repeat initialization subsequence.		
ENDIF		

23.2.6 HDQ1W Register Manual

23.2.6.1 HDQ1W Instance Summary

Table 23-106. HDQ1W Instance Summary

Module Name	Base Address	Size
HDQ1W	0x480B 2000	4 KiB

23.2.6.2 HDQ1W Registers

CAUTION

The following rules must be observed when accessing the module registers:

- A read from the HDQ_INT_STATUS register or the HDQ_RX_DATA register is not allowed unless the processor has been interrupted by the module.
- After the release of the GO bit in the HDQ_CTRL_STATUS register, no access to the HDQ_TX_DATA or HDQ_CTRL_STATUS register is allowed until the processor has been interrupted by the module.
- Polling of the HDQ_INT_STATUS register by software to determine whether an interrupt was generated is not allowed.

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CAUTION

The HDQ1W registers are limited to 32-bit data accesses; 16-bit and 8-bit data accesses are not allowed and can corrupt register content.

23.2.6.2.1 HDQ1W Register Summary

Table 23-107. HDQ1W Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
HDQ_REVISION	R	32	0x0000 0000	0x480B 2000
HDQ_TX_DATA	RW	32	0x0000 0004	0x480B 2004
HDQ_RX_DATA	R	32	0x0000 0008	0x480B 2008
HDQ_CTRL_STATUS	RW	32	0x0000 000C	0x480B 200C
HDQ_INT_STATUS	R	32	0x0000 0010	0x480B 2010
HDQ_SYSCONFIG	RW	32	0x0000 0014	0x480B 2014
HDQ_SYSSTATUS	R	32	0x0000 0018	0x480B 2018

23.2.6.2.2 HDQ1W Register Description

Table 23-108. HDQ_REVISION

Address Offset	0x0000 0000		
Physical Address	0x480B 2000	**Instance**	HDQ1W
Description	This register contains the IP revision code		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REV							

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 23-109. Register Call Summary for Register HDQ_REVISION

HDQ1W

- HDQ1W Register Summary: [0]

Table 23-110. HDQ_TX_DATA

Address Offset	0x0000 0004		
Physical Address	0x480B 2004	**Instance**	HDQ1W
Description	This register contains the data to be transmitted.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TX_DATA							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reads returns 0	R	0x000000
7:0	TX_DATA	Transmit data (used in both HDQ and 1-Wire modes)	RW	0x00

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Table 23-111. Register Call Summary for Register HDQ_TX_DATA

HDQ1W

- HDQ Protocol Initialization (Default): [0]
- 1-Wire Single-Bit Mode Operation: [1]
- Main Sequence - HDQ Write Operation Mode: [2]
- Main Sequence - 1-Wire Write Operation Mode: [3]
- HDQ1W Registers: [4]
- HDQ1W Register Summary: [5]

Table 23-112. HDQ_RX_DATA

Address Offset	0x0000 0008		
Physical Address	0x480B 2008	**Instance**	HDQ1W
Description	This register contains the data to be received.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_DATA							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reads returns 0	R	0x000000
7:0	RX_DATA	Receive data (used in both HDQ and 1-Wire modes)	R	0x00

Table 23-113. Register Call Summary for Register HDQ_RX_DATA

HDQ1W

- Description: [0]
- 1-Wire Single-Bit Mode Operation: [1]
- Sub-sequence - Initialize HDQ Slave: [2]
- Main Sequence - 1-Wire Read Operation Mode: [3]
- HDQ1W Registers: [4]
- HDQ1W Register Summary: [5]

Table 23-114. HDQ_CTRL_STATUS

Address Offset	0x0000 000C		
Physical Address	0x480B 200C	**Instance**	HDQ1W
Description	This register provides status information about the module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					BITFSM			ONE_WIRE_SINGLE_BIT	INTERRUPTMASK	CLOCKENABLE	GO	PRESENCEDETECT	INITIALIZATION	DIR	MODE

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Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reads returns 0	RW	0x000000
10:8	BITFSM	BITFSM delay value in 1.33 µs steps. 0x0 value corresponds to 1.33 µs.	RW	0x00
7	ONE_WIRE_SINGLE_BIT	Single-bit mode for 1-Wire 0x0: Disabled 0x1: Enabled	RW	0
6	INTERRUPTMASK	Interrupt masking bit 0x0: Interrupts disable 0x1: Interrupts enable	RW	0
5	CLOCKENABLE	Power-down mode bit 0x0: Clock disable (power down) 0x1: Clock enable	RW	0
4	GO	Go bit. Write 1 to start the appropriate operation. Bit returns to 0 after the operation is complete.	RW	0
3	PRESENCEDETECT	Slave presence indicator. Actual only just after initialization time-out. Used in 1-Wire mode. Read-only flag. 0x0: No slave detected 0x1: Slave detected	R	0
2	INITIALIZATION	Write 1 to send initialization pulse. Bit returns to 0 after pulse is sent.	RW	0
1	DIR	DIR bit, determines if next command is read or write 0x0: Write 0x1: Read	RW	0
0	MODE	Mode selection bit 0x0: HDQ mode 0x1: 1-Wire mode	RW	0

Table 23-115. Register Call Summary for Register HDQ_CTRL_STATUS

HDQ1W

- HDQ Protocol Initialization (Default): [0] [1]
- HDQ1W Block Diagram: [2]
- HDQ1W Hardware and Software Reset: [3]
- HDQ1W Power Management: [4]
- Power-Down Mode: [5]
- HDQ Interrupt Requests: [6] [7] [8]
- Description: [9] [10]
- Single-Bit Mode: [11]
- Description: [12] [13] [14]
- 1-Wire Single-Bit Mode Operation: [15]
- Status Flags: [16]
- BITFSM Delay: [17]
- HDQ1W Module Global Initialization: [18] [19]
- Main Sequence - HDQ Write Operation Mode: [20] [21] [22] [23]
- Sub-sequence - Initialize HDQ Slave: [24] [25] [26] [27]
- Main Sequence - 1-Wire Write Operation Mode: [28] [29] [30] [31]
- Main Sequence - 1-Wire Read Operation Mode: [32] [33]
- Sub-sequence - Initialize 1-Wire Slave: [34] [35] [36]
- HDQ1W Registers: [37] [38]
- HDQ1W Register Summary: [39]

Table 23-116. HDQ_INT_STATUS

Address Offset	0x0000 0010		
Physical Address	0x480B 2010	**Instance**	HDQ1W
Description	This register controls interrupts status		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													TXCOMPLETE	RXCOMPLETE	TIMEOUT

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads returns 0	R	0x0000 0000
2	TXCOMPLETE	TX-complete interrupt flag. Set to 1 if cause of interrupt. Set to 0 when register read.	R	0
1	RXCOMPLETE	Read-complete interrupt flag. Set to 1 if cause of interrupt. Set to 0 when register read.	R	0
0	TIMEOUT	Presence detect/timeout interrupt flag. In 1-Wire mode, set to 1 if slave's presence detected. In HDQ mode, set to 1 if timeout on read occurs. Set to 0 when register read.	R	0

Table 23-117. Register Call Summary for Register HDQ_INT_STATUS

HDQ1W

- HDQ Interrupt Requests: [0] [1] [2]
- Description: [3] [4] [5]
- Interrupt Conditions: [6] [7] [8]
- Description: [9] [10]
- Interrupt Conditions: [11] [12] [13]
- Status Flags: [14]
- Main Sequence - HDQ Write Operation Mode: [15] [16]
- Sub-sequence - Initialize HDQ Slave: [17] [18] [19] [20] [21]
- Main Sequence - 1-Wire Write Operation Mode: [22] [23]
- Main Sequence - 1-Wire Read Operation Mode: [24] [25] [26] [27]
- Sub-sequence - Initialize 1-Wire Slave: [28]
- HDQ1W Registers: [29] [30]
- HDQ1W Register Summary: [31]

Table 23-118. HDQ_SYSCONFIG

Address Offset	0x0000 0014		
Physical Address	0x480B 2014	**Instance**	HDQ1W
Description	This register controls various bits		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reads returns 0	RW	0x0000 0000
1	SOFTRESET	Start soft reset sequence. 0x0: Disabled 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
0	AUTOIDLE	Interconnect idle. 0x0: Module clock is free-running. 0x1: Module is in power saving mode: Clock is running only when module is accessed or inside logic is in function to process events.	RW	0

Table 23-119. Register Call Summary for Register HDQ_SYSCONFIG

HDQ1W

- HDQ1W Hardware and Software Reset: [0]
- HDQ1W Power Management: [1]
- Auto-Idle Mode: [2]
- HDQ1W Module Global Initialization: [3] [4]
- HDQ1W Register Summary: [5]

Table 23-120. HDQ_SYSSTATUS

Address Offset	0x0000 0018		
Physical Address	0x480B 2018	**Instance**	HDQ1W
Description	This register monitors the reset sequence.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0	R	0x0000 0000
0	RESETDONE	Reset monitoring. 0x0: The module is currently performing its reset. When the module is in power-down mode, set to 0 to indicate this fact. 0x1: The module has finished its reset.	R	1

Table 23-121. Register Call Summary for Register HDQ_SYSSTATUS

HDQ1W

- HDQ1W Module Global Initialization: [0]
- HDQ1W Register Summary: [1]

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23.3 UART/IrDA/CIR

This chapter describes the function, operation, and configuration of the universal asynchronous receiver/transmitter (UART)/infrared data association (IrDA)/consumer infrared (CIR) module in the device.

23.3.1 UART/IrDA/CIR Overview

The device contains four UART devices controlled by the microprocessor unit (MPU) (see Figure 23-39):

- Five UART-only modules (UART1, UART2, UART4, UART5, and UART6) are pinned out for use as UART devices only.
- UART3, which adds infrared communication support, is pinned out for use as a UART, IrDA, or CIR device, and can be programmed to any available operating mode.

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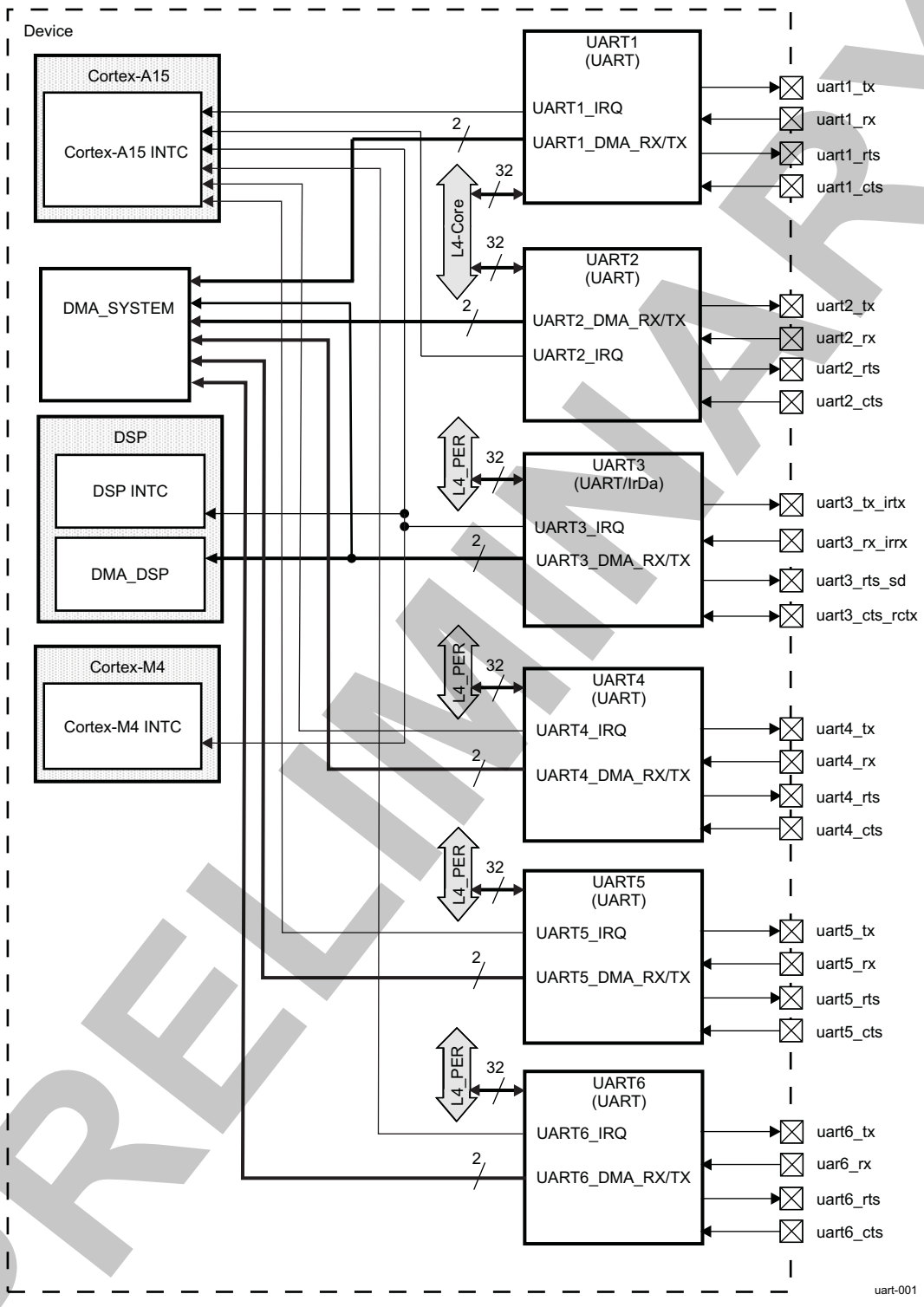
Figure 23-39. UART Module



23.3.1.1 UART Features

The UARTs (UART1, UART2, UART3 when in UART mode, UART4, UART5, and UART6) include the following features:

- 16C750 compatibility

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- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Programmable interrupt trigger levels for FIFOs
- Baud generation based on programmable divisors N (where N = 1…16,384) operating from a fixed functional clock of 48 MHz

Oversampling is programmed by software as 16 or 13; thus, the baud rate computation is one of two options:

- Baud rate = (functional clock / 16) / N
- Baud rate = (functional clock / 13) / N

This software programming mode enables higher baud rates with the same error amount without changing the clock source:

- Break character detection and generation
- Configurable data format:
  - Data bit: 5, 6, 7, or 8 bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)

The UART clocks are connected to produce a baud rate of up to 3.6864 Mbps. Table 23-122 lists the supported baud rates, requested divisor, and corresponding error versus the standard baud rate.

Table 23-122. UART Mode Baud Rates, Divisor Values, and Error Rates

Baud Rate	Oversampling	Divisor	Error (%)
300	16	10,000	0
600	16	5000	0
1200	16	2500	0
2400	16	1250	0
4800	16	625	0
9600	16	312	0.16
14,400	16	208	0.16
19,200	16	156	0.16
28,800	16	704	0.16
38,400	16	78	0.16
57,600	16	52	0.16
115,200	16	26	0.16
230,400	16	13	0.16
460,800	13	8	0.16
921,600	13	4	0.16
1,843,200	13	2	0.16
3,000,000	16	1	0
3,686,400	13	1	0.16

23.3.1.2 IrDA Features

The IrDA (UART3 only) includes the following key features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications:
  - Frame formatting: Addition of variable beginning-of-frame (xBOF) characters and end-of-frame (EOF) characters
  - Uplink/downlink cyclic redundancy check (CRC) generation/detection
  - Asynchronous transparency (automatic insertion of break character)

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– Eight-entry status FIFO (with selectable trigger levels) to monitor frame length and frame errors
– Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection

Table 23-123 lists the supported baud rates, requested divisor, and corresponding error versus the standard baud rate.

Table 23-123. UART IrDA Mode Baud Rates, Divisor Values, and Error Rates

Baud Rate	IR Mode	Encoding	Divisor	Error (%)
2400	SIR	3/16	1250	0
9600	SIR	3/16	312	0.16
19,200	SIR	3/16	156	0.16
38,400	SIR	3/16	78	0.16
57,600	SIR	3/16	52	0.16
115,200	SIR	3/16	26	0.16
576,000	MIR	1/4	2	0
1,152,000	MIR	1/4	1	0
4,000,000	FIR	4 PPM(1)	1	0

(1) PPM = Pulse-position modulation

23.3.1.3 CIR Features

The CIR mode uses a variable pulse-width modulation (PWM) technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on a user-definable frame structure and packet content.

The CIR (UART3 only) includes the following features to provide CIR support for remote-control applications:

- Transmit mode only (receive mode is not supported)
- Free data format (supports any remote-control private standards)
- Selectable bit rate
- Configurable carrier frequency
- 1/2, 5/12, 1/3, or 1/4 carrier duty cycle

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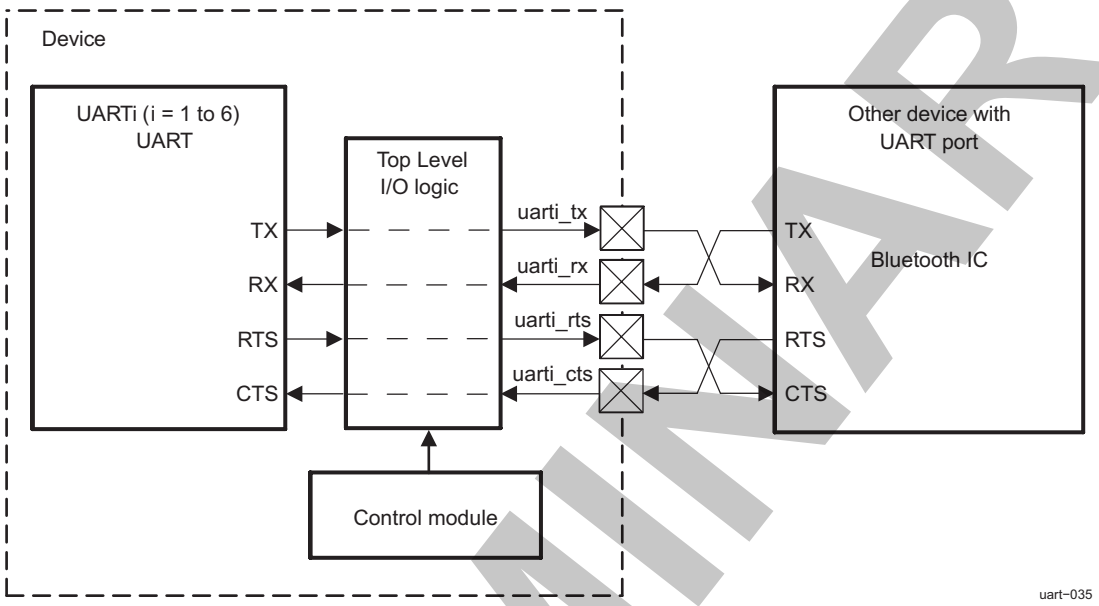
23.3.2 UART/IrDA/CIR Environment

This section describes the UART/IrDA/CIR connection with an external device.

Figure 23-40 *UART Controller I/O signals*, illustrates module pin signals mapping to signals visible at device pad level.

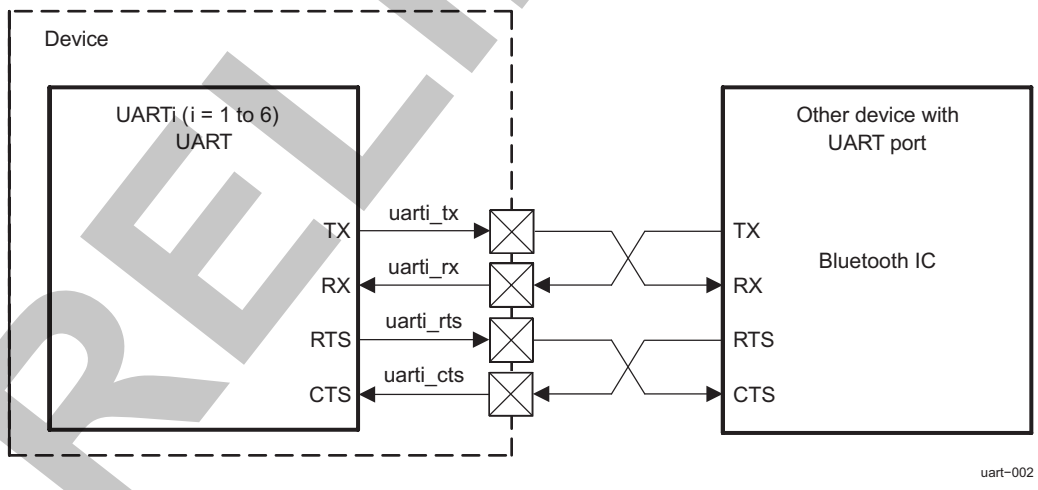
Figure 23-40. UART Controller I/O signals



23.3.2.1 System Using UART Communication With Hardware Handshake

Each UART instance can be easily connected to the UART port of an external IC (see Figure 23-41).

Figure 23-41. UART Mode Bus System Overview



23.3.2.2 System Using IrDA Communication Protocol

As Figure 23-42 shows, UART3 can be connected to an external infrared transceiver in the IrDA modes (FIR, SIR, and MIR).

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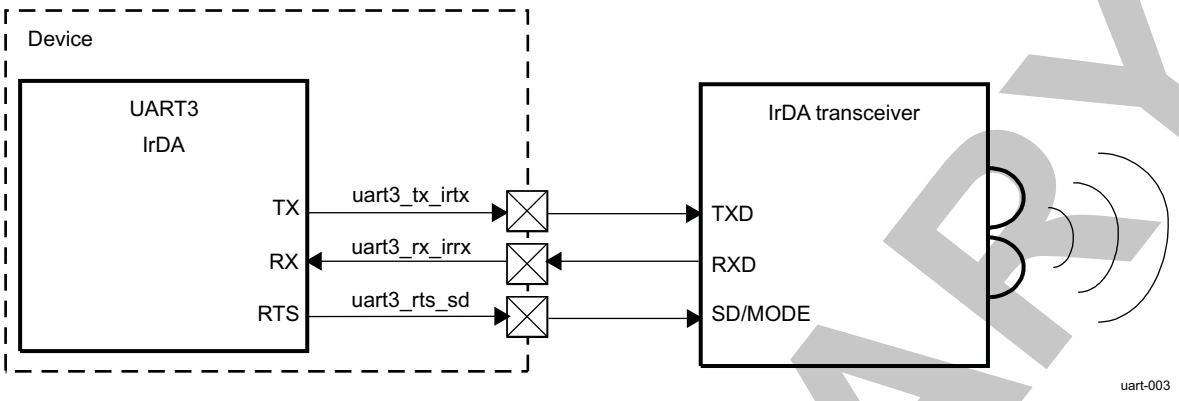
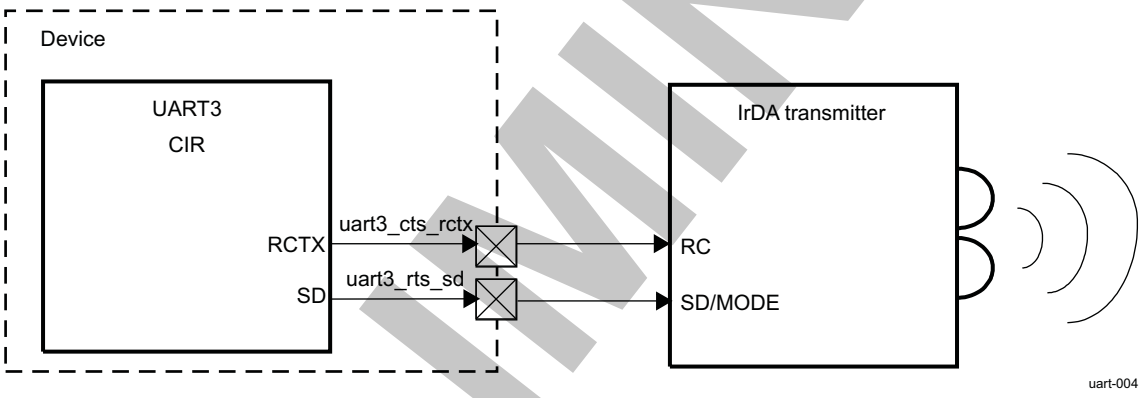
Figure 23-42. IrDA System Overview



23.3.2.3 System Using CIR Communication Protocol With Remote Control

UART3 can be connected to an external infrared transceiver in CIR mode (see Figure 23-43).

Figure 23-43. CIR System Overview



23.3.2.4 UART Interface

23.3.2.4.1 Description

Table 23-124 lists the UART interface input/output (I/O) signals.

Table 23-124. UART I/O Pins

Signal	I/O[1]	Description	Reset
UART Modem Signals			
uarti_rx	I	Serial data input	Unknown
uarti_tx	O	Serial data output Because this pin is active high in IrDA mode and the output is muxed, this pin is set to low on reset (when the UARTi.UART_MDR1[2:0] bit field is set to 0x7) and takes the defined inactive level of that signal corresponding to when and how the UARTi.UART_MDR1 register is programmed; that is, the output is 1 (inactive for UART modem modes) and 0 (inactive for IrDA modes).	1
uarti_cts	I	Clear to send	Unknown

(1) I = Input; O = Output; I/O = Bidirectional

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Table 23-124. UART I/O Pins (continued)

Signal	I/O[1]	Description	Reset
		Active-low modem status signal. Reading the UARTi.UART_MSR[4] NCTS_STS bit checks the condition of uarti_cts. Reading the UARTi.UART_MSR[0] CTS_STS bit checks a change of state of uarti_cts since the last read of the modem status register. The auto-nCTS mode uses uarti_cts to control the transmitter.	
uarti_rts	O	Request to send When active (low), the module is ready to receive data. Setting the UARTi.UART_MCR[1] RTS bit activates uarti_rts, which becomes inactive as the result of a module reset, loopback mode, or clearing the UARTi.UART_MCR[1] RTS bit. In auto-RTS mode, uarti_rts becomes inactive as a result of the receiver threshold logic.	1

NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and is programmable in the Control Module registers. For more information on control module settings, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*.

23.3.2.4.2 UART Protocol and Data Format

The UART device operates in three modes:

- UART 16x (<= 230.4 kbps)
- UART 16x with autobauding (>= 1200 bps and >= 115.2 kbps)
- UART 13x (>= 460.8 kbps)

CAUTION

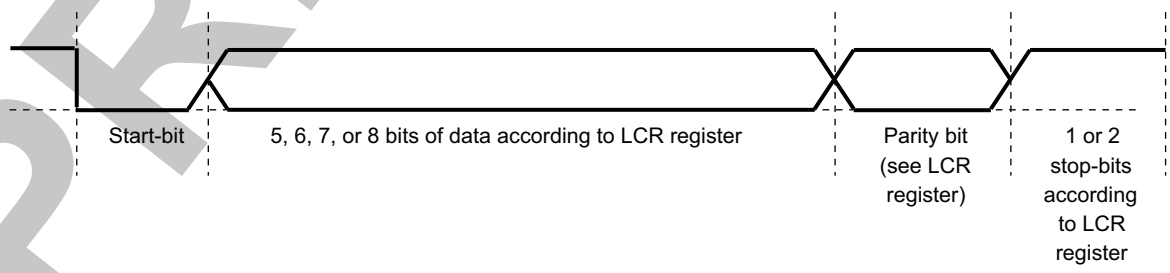
To be used as a UART, the operating mode must be programmed appropriately in the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to select UART, IrDA, or CIR mode.

The UART uses a wired interface for serial communication with a remote device.

The UART is functionally compatible with the TL16C750 UART and earlier designs such as the TL16C550.

Figure 23-44 shows the UART frame data format.

Figure 23-44. UART Frame Data Format



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23.3.2.5 IrDA Functional Interfaces

23.3.2.5.1 UART3 Interface Description

Table 23-125 lists the UART3 interface I/O signals.

Table 23-125. UART3 I/O Signals

Signal	I/O[1]	Description	Reset
IrDA Signals			
uart3_rx_irrx	I	Serial data input	Unknown
uart3_tx_irtx	O	Serial data output in IrDA modes (SIR, MIR, and FIR). In other modes, this pin is set to the reset value (inactive state).	0
uart3_rts_sd	O	SD mode is used to configure the transceivers. The SD pinout is an inverted value of the UART3.UART_ACREG[6] SD_MOD bit.	1

(1) I = Input; O = Output

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23.3.2.5.2 IrDA Protocol and Data Format

23.3.2.5.2.1 SIR Mode

In SIR mode, data is transferred between the MPU and peripheral devices at speeds of up to 115,200 baud. A SIR transmit frame begins with start flags (a single 0xC0, a multiple 0xC0, or a single 0xC0 preceded by a number of 0xFF flags), is followed by frame data and a CRC-16, and ends with a stop flag (0xC1).

The bit format for a single word uses 1 start-bit, 8 data bits, and 1 stop-bit, and is unaffected by the use and settings of the UART3.UART_LCR register.

The UART3.UART_BLR[6] XBOF_TYPE bit selects whether the 0xC0 or 0xFF start patterns are used when multiple start flags are required.

The SIR transmit state-machine attaches start flags, CRC-16, and stop flags, and checks the outgoing data to establish whether data transparency is required.

SIR transparency is carried out if the outgoing data between the start and stop flags contains 0xC0, 0xC1, or 0x7D. If one of these start flags is about to be transmitted, the SIR state-machine sends an escape character (0x7D), inverts the fifth bit of the real data to be sent, and then sends this data immediately after the 0x7D character.

The SIR receive state-machine recovers the receive clock, removes the start flags and any transparency from the incoming data, and determines the frame boundary with reception of the stop flag. The SIR state-machine also checks for errors such as a frame abort (0x7D character followed immediately by a 0xC1 stop flag without transparency), a CRC error, or a frame-length error. At the end of a frame reception, the MPU reads the line status register (UART3.UART_LSR) to find possible errors of the received frame.

NOTE: The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. See the description of the UART3.UART_ACREG[5] DIS_IR_RX bit. This applies to all three modes: SIR, MIR, and FIR.

Infrared output in SIR mode can be 1.6-µs or 3/16 encoding, selected by the UART3.UART_ACREG[7] PULSE_TYPE bit. In 1.6-µs encoding, the infrared pulse width is 1.6 µs; and in 3/16th encoding, the infrared pulse width is 3/16th of a bit duration (1/baud rate).

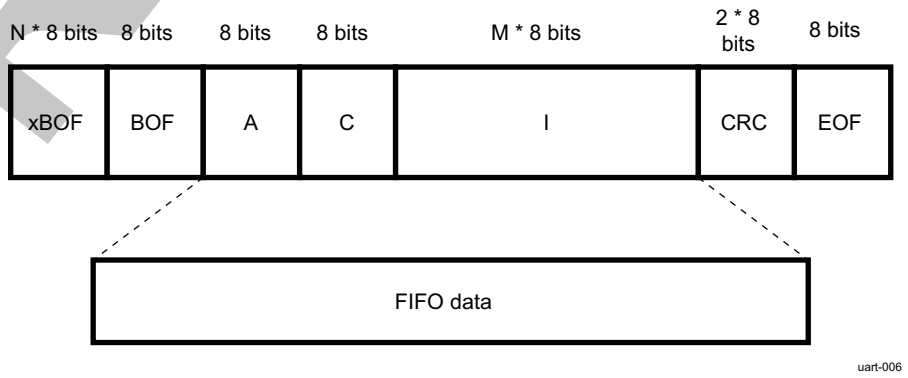
For back-to-back frames, the transmitting device must send at least two start flags at the start of each frame.

NOTE: Reception supports variable-length stop-bits.

23.3.2.5.2.1.1 Frame Format

Figure 23-45 shows the IrDA SIR frame format.

Figure 23-45. IrDA SIR Frame Format



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The CRC is applied on the address (A), control (C), and information (I) bytes.

NOTE: The two words of CRC are written to the FIFO in reception.

23.3.2.5.2.1.2 Asynchronous Transparency

Before transmitting a byte, the UART IrDA controller examines each byte of the payload and the CRC field (between BOF and EOF). For each byte equal to 0xC0 (BOF), 0xC1 (EOF), or 0x7D (control escape), the controller performs certain tasks:

- In transmission:
  - Inserts a control escape (CE) byte preceding the byte
  - Complements bit 5 of the byte (that is, exclusive ORs the byte with 0x20)

  The byte sent for the CRC computation is the initial byte written in the TX FIFO (before the XOR with 0x20).
- In reception:

  For the A, C, I, and CRC fields:
  - Compares the byte with the CE byte; if they are not equal, sends the byte to the CRC detector and stores it in the RX FIFO.
  - If the byte is equal to the CE byte, discards the CE byte
  - Complements bit 5 of the byte following the CE
  - Sends the complemented byte to the CRC detector and stores it in the RX FIFO

23.3.2.5.2.1.3 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

When a 0x7D character that is followed immediately by a 0xC1 character is received without transparency, the receiver treats the frame as an aborted frame.

23.3.2.5.2.1.4 Pulse Shaping

The SIR mode supports the 3/16 and the 1.6-µs pulse duration methods. The UART3.UART_ACREG[7] PULSE_TYPE bit selects the pulse-width method in transmit mode.

23.3.2.5.2.1.5 Encoder

Serial data from the transmit state-machine are encoded to transmit data to the optoelectronics. While the TX FIFO output is high, the uart3_tx_irtx line is always low, and the counter used to form a pulse on uart3_tx_irtx is cleared continuously.

After the TX FIFO output resets to 0, uart3_tx_irtx rises on the falling edge of the seventh 16XCLK. On the falling edge of the tenth 16XCLK pulse, uart3_tx_irtx falls, creating a 3-clock-wide pulse. While the TX FIFO output stays low, a pulse is transmitted during the seventh clock to the tenth clock of each 16-clock bit cycle.

Figure 23-46 shows the IrDA SIR encoding mechanism.

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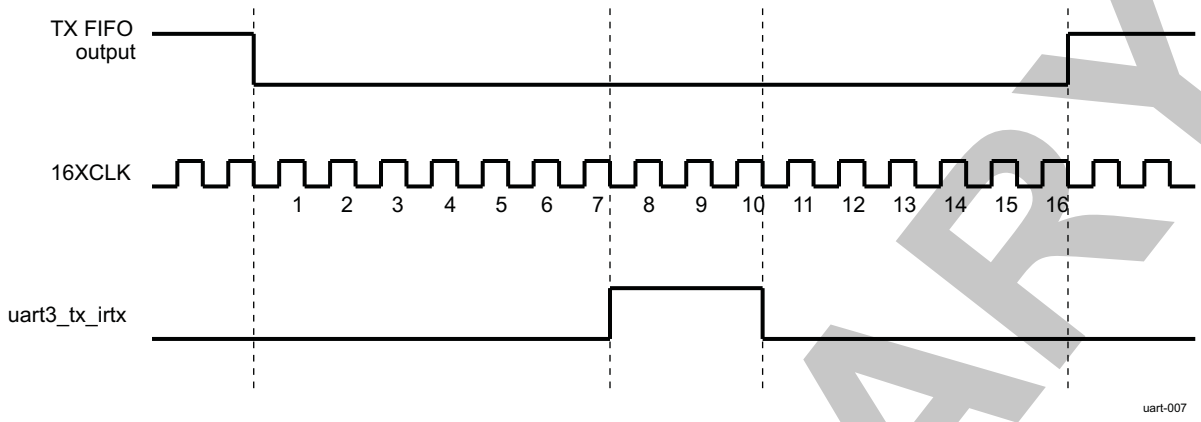
Figure 23-46. IrDA SIR Encoding Mechanism

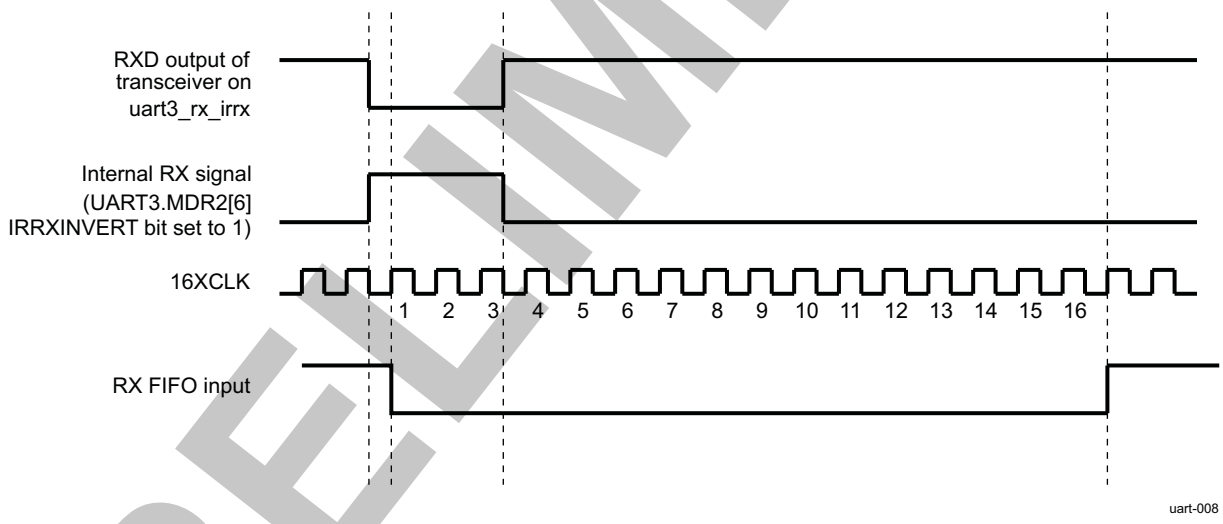


23.3.2.5.2.1.6 Decoder

After reset, the RX FIFO input is high and the 4-bit counter is cleared. When a rising edge is detected on RX, the RX FIFO input falls on the next rising edge of 16XCLK with sufficient setup time. The RX FIFO input stays low for 16 cycles (16XCLK) and then returns to high as required by the IrDA specification. As long as no pulses (rising edges) are detected on the RX, the RX FIFO input remains high.

Figure 23-47 shows the IrDA SIR decoding mechanism.

Figure 23-47. IrDA SIR Decoding Mechanism



The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware. The operation of the uart3_rx_irrx input can be disabled using the UART3.UART_ACREG[5] DIS_IR_RX bit. The UART3.UART_MDR2[6] IRRXINVERT bit can invert the signal from the transceiver (RXD) pin to the IR RX logic in the UART. This inversion is performed by default.

23.3.2.5.2.1.7 IR Address Checking

In all IR modes, when address checking is enabled by setting the UART_EFR[1:0] bit field (see Table 23-126), only frames intended for the device are written to the RX FIFO. This is to avoid receiving frames not meant for this device in a multipoint infrared environment. To program two frame addresses that the UART3 receives in IrDA mode, use the UART3.UART_XON1_ADDR1[7:0] and UART3.UART_XON2_ADDR2[7:0] bit fields.

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Table 23-126. UART_EFR[1:0] IR Address Checking Options

UART_EFR[1]	UART_EFR[0]	IR Address Checking
0	0	All address-checking operations disabled
0	1	Only address 1 checking enabled
1	0	Only address 2 checking enabled
1	1	All address-checking operations enabled

23.3.2.5.2.2 SIR Free-Format Mode

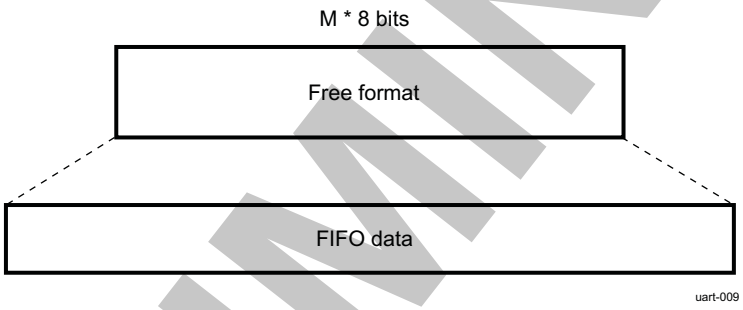
To allow complete software flexibility when transmitting and receiving infrared data packets, the SIR free-format (FF) mode is a subfunction of the existing SIR mode. In FF mode, all frames going to and from the FIFO buffers are untouched with respect to appending and removing control characters and CRC values.

The FF mode corresponds to a UART mode with a pulse modulation of 3/16 of baud rate pulse width.

For example, a normal SIR packet has BOF control and CRC error-checking data appended (transmitting) or removed (receiving) from the data going to and from the FIFOs.

Figure 23-48 shows SIR FF mode.

Figure 23-48. SIR FF Mode

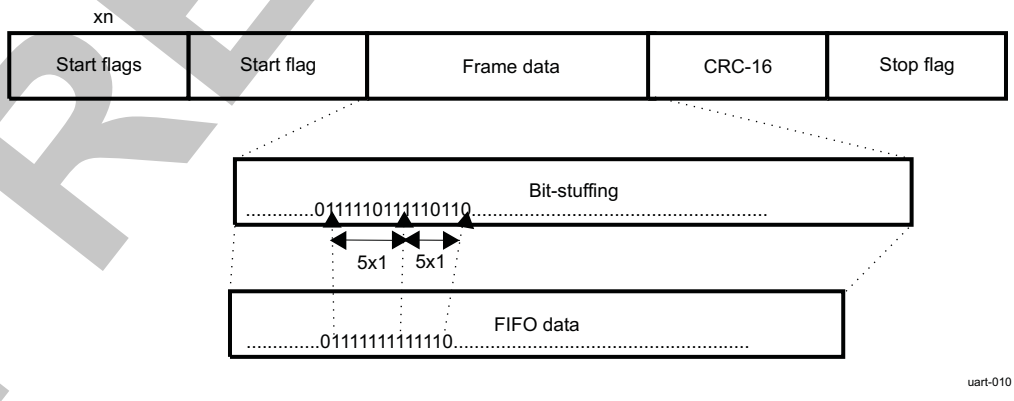


In SIR FF mode, the MPU software must construct (that is, encode and decode) the entire FIFO data packet.

23.3.2.5.2.3 MIR Mode

In MIR mode, data is transferred between the MPU and the peripheral devices at 0.576 or 1.152 Mbps. A MIR transmit frame starts with at least two start flags, followed by a frame data and a CRC-16, and ends with a stop flag (see Figure 23-49).

Figure 23-49. MIR Transmit Frame Format



On transmit, the MIR state-machine attaches start flags, a CRC-16, and stop flags, as in SIR mode. All fields are transmitted least-significant bit (LSB) of each byte first.

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In MIR mode:

- The state-machine looks for consecutive 1s in the frame data and automatically inserts 0 after five consecutive 1s (this is called bit-stuffing).
- 0x7E is used for start and stop flags (unambiguously, not data, because of bit-stuffing).
- An abort sequence requires a minimum of seven consecutive 1s (unambiguously, not data, because of bit-stuffing).
- Back-to-back frames are allowed with three or more stop flags between them. If two consecutive frames are not back to back, the gap between the last stop flag of the first frame and the start flag of the second frame must be separated by at least seven bit durations.

On receive, the MIR receive state-machine recovers the receive clock, removes the start flags, destuffs the incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as frame abort, CRC error, and frame-length error. At the end of a frame reception, the MPU reads the line status register (UART3.UART_LSR) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

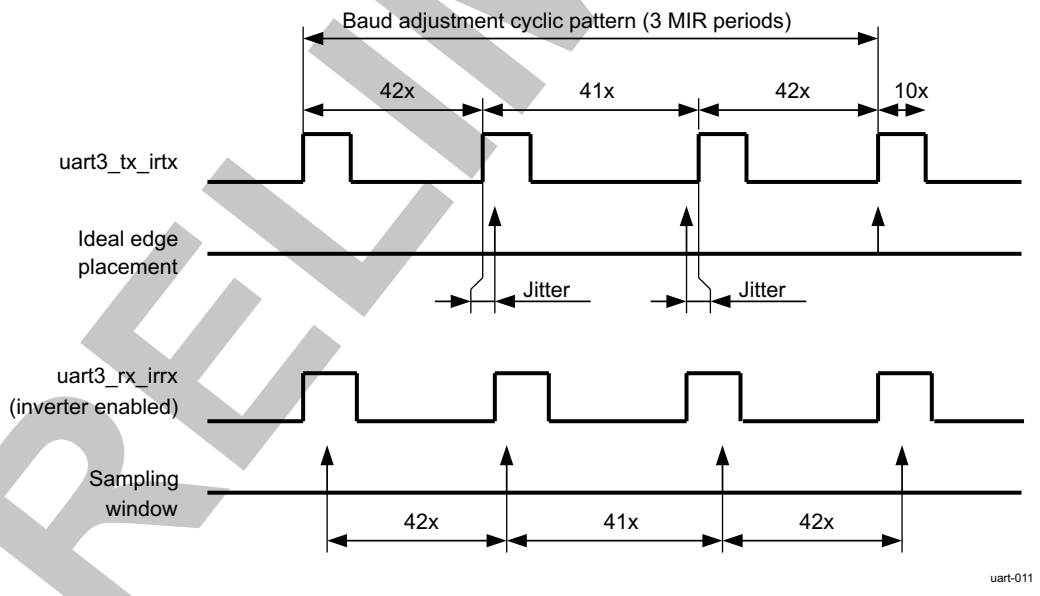
23.3.2.5.2.3.1 MIR Encoder/Decoder

To meet the MIR baud rate tolerance of 0.1 percent with a 48-MHz clock input, a 42-41-42 encoding/decoding adjustment is performed. The reference start point is the first start flag, and the 42-41-42 cyclic pattern is repeated until the stop flag is sent or detected.

The jitter created this way is within MIR tolerances. The pulse width is not exactly 1/4, but it is within the tolerances defined by IrDA specifications.

Figure 23-50 shows the MIR baud rate adjustment mechanism.

Figure 23-50. MIR Baud Rate Adjustment Mechanism



23.3.2.5.2.3.2 SIP Generation

In the MIR and FIR operation modes, the transmitter must send a serial infrared interaction pulse (SIP) at least once every 500 ms. The SIP informs slow devices (operating in SIR mode) that the medium is occupied.

Figure 23-51 shows the SIP.

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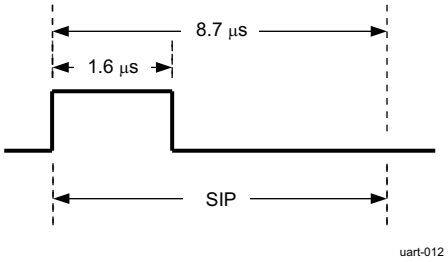
Figure 23-51. SIP



23.3.2.5.2.4 FIR Mode

In FIR mode, data is transferred between the MPU and the peripheral devices at 4 Mbps. A FIR transmit frame starts with a preamble that is followed by a start flag, frame data, CRC-32, and ends with a stop flag.

Figure 23-52 shows the FIR transmit frame format.

Figure 23-52. FIR Transmit Frame Format

Preamble (16x)	Start flag	Frame data	CRC-32	Stop flag

On transmit, the FIR transmit state-machine attaches the preamble, start flag, CRC-32, and stop flag. An abort sequence requires at least two transmissions of 0000. Back-to-back frames are allowed, but each frame must be complete.

The state-machine also encodes the transmit data into 4-PPM format (see Table 23-127) and generates the SIP (see Section 23.3.2.5.2.3.2, *SIP Generation*).

Table 23-127. 4-PPM Format

Data Bit Pair (Bin)	4-PPM Data Symbol (Bin)
00	1000
01	0100
10	0010
11	0001

The four symbols described in Table 23-127 are the legal, encoded data symbols. All other combinations are illegal for encoding data. Some of these illegal symbols are used in the definition of the preamble, start flag, and stop flag because they are unambiguously not data (see Table 23-128).

Table 23-128. FIR Preamble, Start Flag, and Stop Flag

Frame Part	Transmitted Frame (Bin)
Preamble	1000 0000 1010 1000 (16 repeated transmissions)
Start flag	0000 1100 0000 1100 0110 0000 0110 0000
Stop flag	0000 1100 0000 1100 0000 0110 0000 0110

All fields are transmitted LSBs of each byte first (see Table 23-129).

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Table 23-129. FIR Data Byte Transmission Order Example

Data Byte (Hex)	Data Byte Pair (Bin)	4-PPM Data Symbol (Bin)	Transmission Order
0x0B	00	1000	4
	00	1000	3
	10	0010	2
	11	0001	1

On receive, the FIR receive state-machine recovers the receive clock, removes the preamble and the start flag, decodes the 4-PPM incoming data, and determines the frame boundary with reception of the stop flag. The state-machine also checks for errors such as illegal symbol, CRC error, and frame-length error. At the end of a frame reception, the MPU reads the line status register (UART3.UART_LSR) to detect errors of the received frame.

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

23.3.2.6 CIR Functional Interfaces

23.3.2.6.1 CIR Interface Description

Table 23-130 lists the CIR interface I/O signals.

Table 23-130. CIR I/O Signals

Signal	I/O[1]	Description	Reset
CIR Signals			
uart3_rx_irrx	I	Serial data input	Unknown
uart3_cts_rctx	O	Serial data output in CIR mode. In other modes, this pin is set to the reset value (inactive state).	0
uart3_rts_sd	O	SD mode is used to configure the transceivers. The SD pinout is an inverted value of the UART3.UART_ACREG[6] SD_MOD bit.	1

(1) I = Input; O = Output

23.3.2.6.2 CIR Protocol and Data Format

In CIR mode, the infrared operation functions as a programmable (universal) remote control.

CIR mode uses a variable PWM technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on user-defined frame structure and packet content.

23.3.2.6.2.1 Carrier Modulation

Each modulated pulse that constitutes a digit is a train of on/off pulses (see Figure 23-53).

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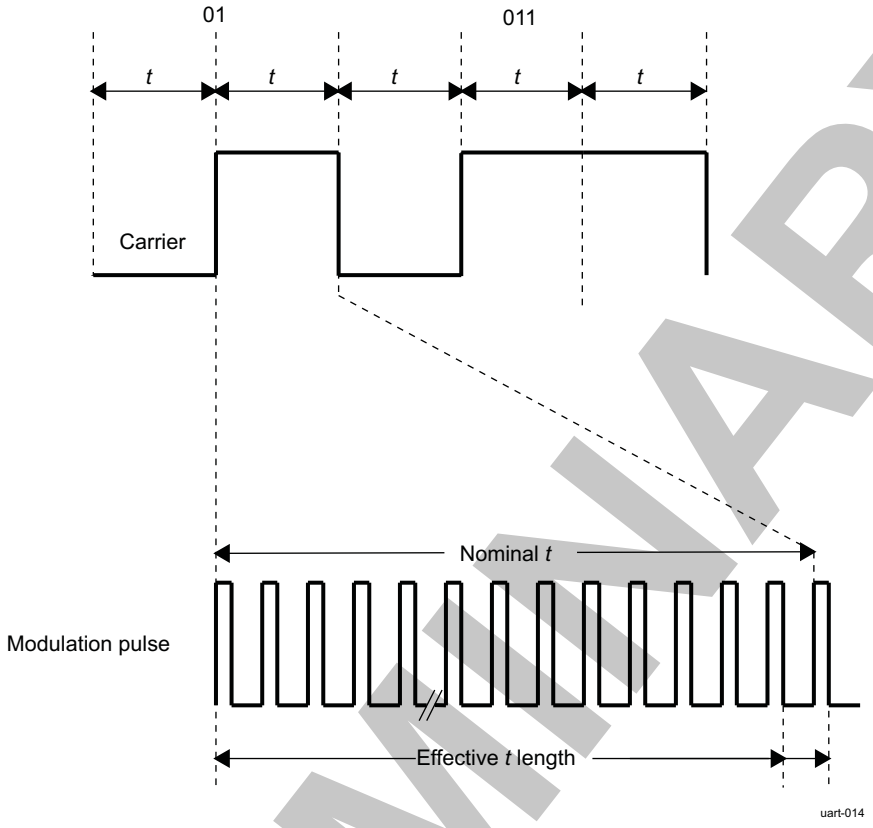
Figure 23-53. CIR Pulse Modulation

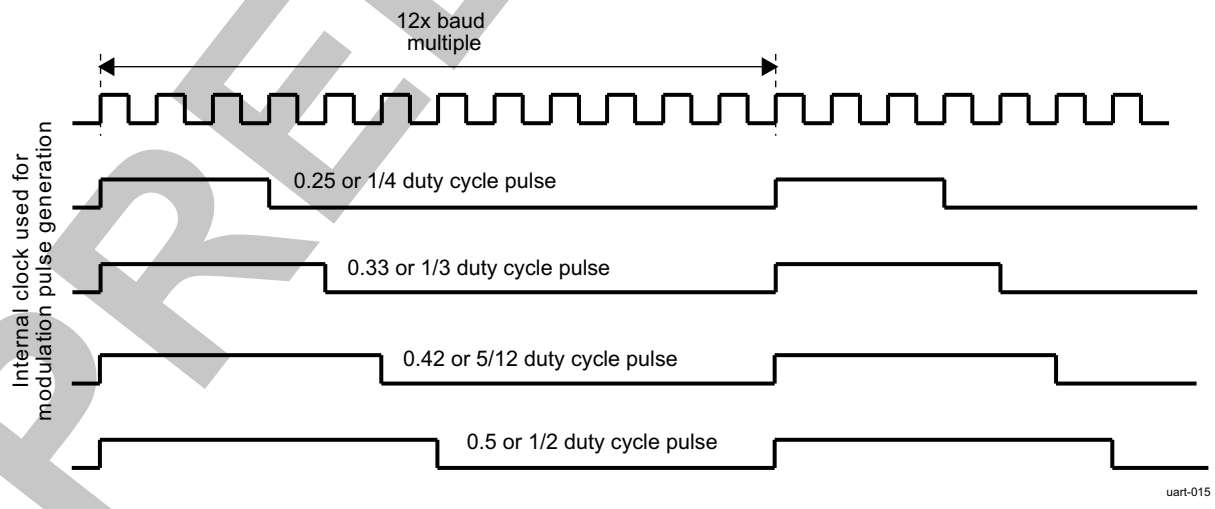


23.3.2.6.2.2 Pulse Duty Cycle

The programmer can choose one of four duty cycles for modulation pulses by setting the appropriate value in the UART3.UART_MDR2[5:4] CIR_PULSE_MODE bit field (1/4, 1/3, 5/12, or 1/2).

Figure 23-54 shows the CIR modulation duty cycles.

Figure 23-54. CIR Modulation Duty Cycle



The transmission logic ensures that all pulses are transmitted completely (no cutoff during transmission). While transmitting continuous bytes back-to-back, no delay is inserted between 2 transmitted bytes. Thus, software must handle the delay between consecutively transmitted bytes if the receiving end requires it.

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23.3.2.6.2.3 Consumer IR Encoding/Decoding

There are two methods of encoding for remote-control applications:

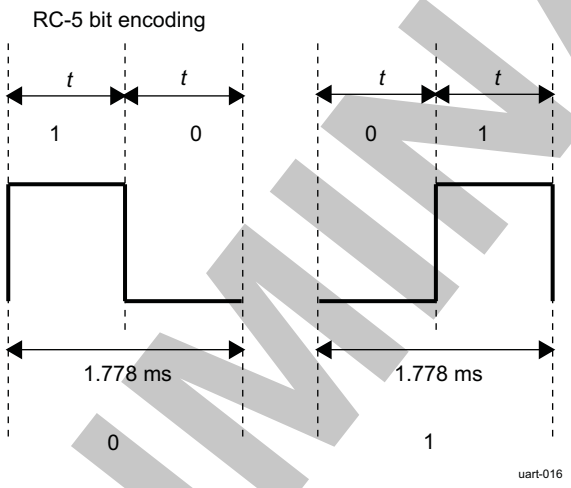
- Pulse duration encoding (time-extended bit forms): A variable pulse distance, or duration, in which the difference between logic 1 and logic 0 is the length of the pulse width
- Biphase encoding: The encoding of logic 0 and logic 1 is in the change of signal level from 1 to 0 or 0 to 1, respectively.

Japanese manufacturers favor pulse duration encoding; European manufacturers favor biphase encoding.

CIR mode uses a completely flexible free-format encoding in which 1 is transmitted from the TX FIFO as a modulated pulse with duration *t*.

Similarly, 0 is transmitted as a blank duration T. The MPU constructs and deciphers the protocol of the data. For example, the RC-5 protocol using Manchester encoding can be emulated as using a 01 pair for 1 and a 10 pair for 0 (see Figure 23-55).

Figure 23-55. RC-5 Bit Encoding



Because CIR mode logic does not impose a fixed format for infrared packets of data, the MPU software can define the format using simple data structures that are then modulated into an industry standard, such as RC-5 or SIRC. To send a sequence of 0101 in RC-5, the MPU software must write an 8-bit binary character of 10011001 to the data FIFO of the UART.

For SIRC, the modulation length (multiples of *t*) is used to distinguish between 1 and 0. The subsequent SIRC digits show the difference in encoding between this and, for example, RC-5. The pulse width is extended for one digit.

Figure 23-56 shows SIRC bit encoding.

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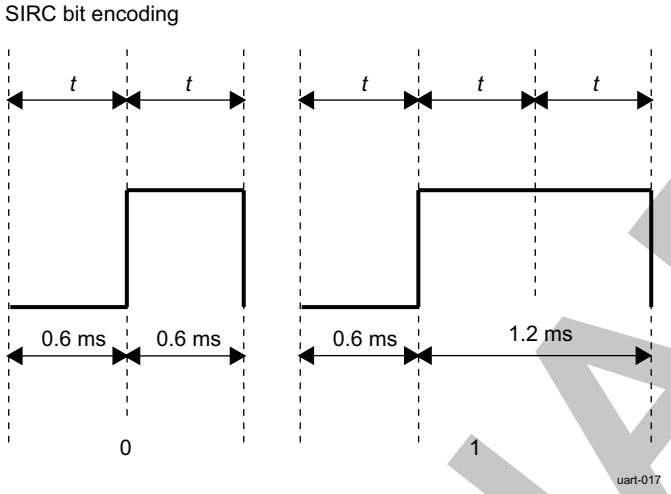
Figure 23-56. SIRC Bit Encoding



To construct comprehensive packets constituting remote-control commands, the MPU software must combine a number of 8-bit data characters in a sequence that follows one of the universally accepted formats.

Figure 23-57 shows a standard RC-5 frame as detected by UART3 in CIR mode (the SIRC format follows this). Each field in RC-5 can be considered as two *t* pulses (digital bits) from the TX FIFO.

Figure 23-57. RC-5 Standard Packet Format

S1	S2	T	A4	A3	A2	A1	A0	C5	C4	C3	C2	C1	C0

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Where:

S1, S2:	Start-bits (always 1)
T:	Toggle bit
A4..A0:	Address (or system) bits
C5..C0:	Command bits

The toggle bit T changes when a new command is transmitted to detect when the same key is pressed twice (effectively receiving the same data from the host consecutively). A brief delay in the transmission of the same command is detected by the use of the toggle bit because a code is sent while the MPU transmits characters to the UART for transmission. The address bits define the machine or device for which the infrared transmission is intended, and the command defines the operation.

To accommodate an extended RC-5 format, the S2 bit is replaced by an additional command bit (C6) that lets the command range increase to 7 bits. This format is known as the extended RC-5 format.

SIRC encoding uses the duration of modulation for mark and space; therefore, the duration of data bits in the standard frame length varies.

Figure 23-58 shows the packet format and bit encoding. As Figure 23-59 shows, 1 start-bit of 2.4 ms and control codes are followed by data that constitute the entire frame.

Figure 23-58. SIRC Packet Format

S	C0	C1	C2	C3	C4	C5	C6	D0	D1	D2	D3	D4

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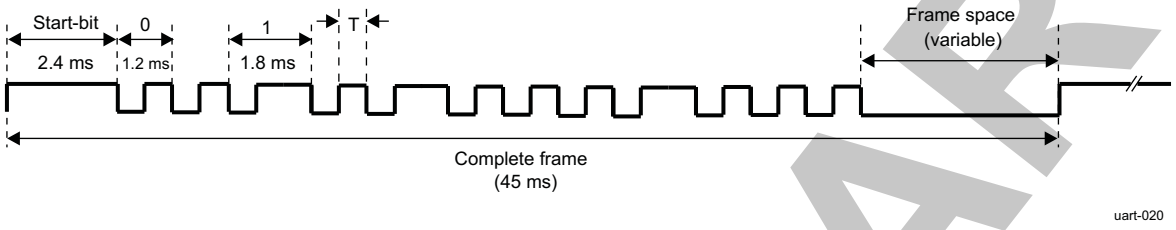
NOTE: The encoding must take a standard duration, but the contents of the data can vary. This implies that the control software for sending and receiving data packets must exercise a scheme of interpacket delay, where successive packets can be sent only after a real-time delay expires.

Figure 23-59. SIRC Bit Transmission Example



This document does not describe all encoding methods and techniques; the previous information discusses the considerations required to employ different encoding methods for different industry-standard protocols. See industry-standard documentation for specific methods of encoding and protocol use.

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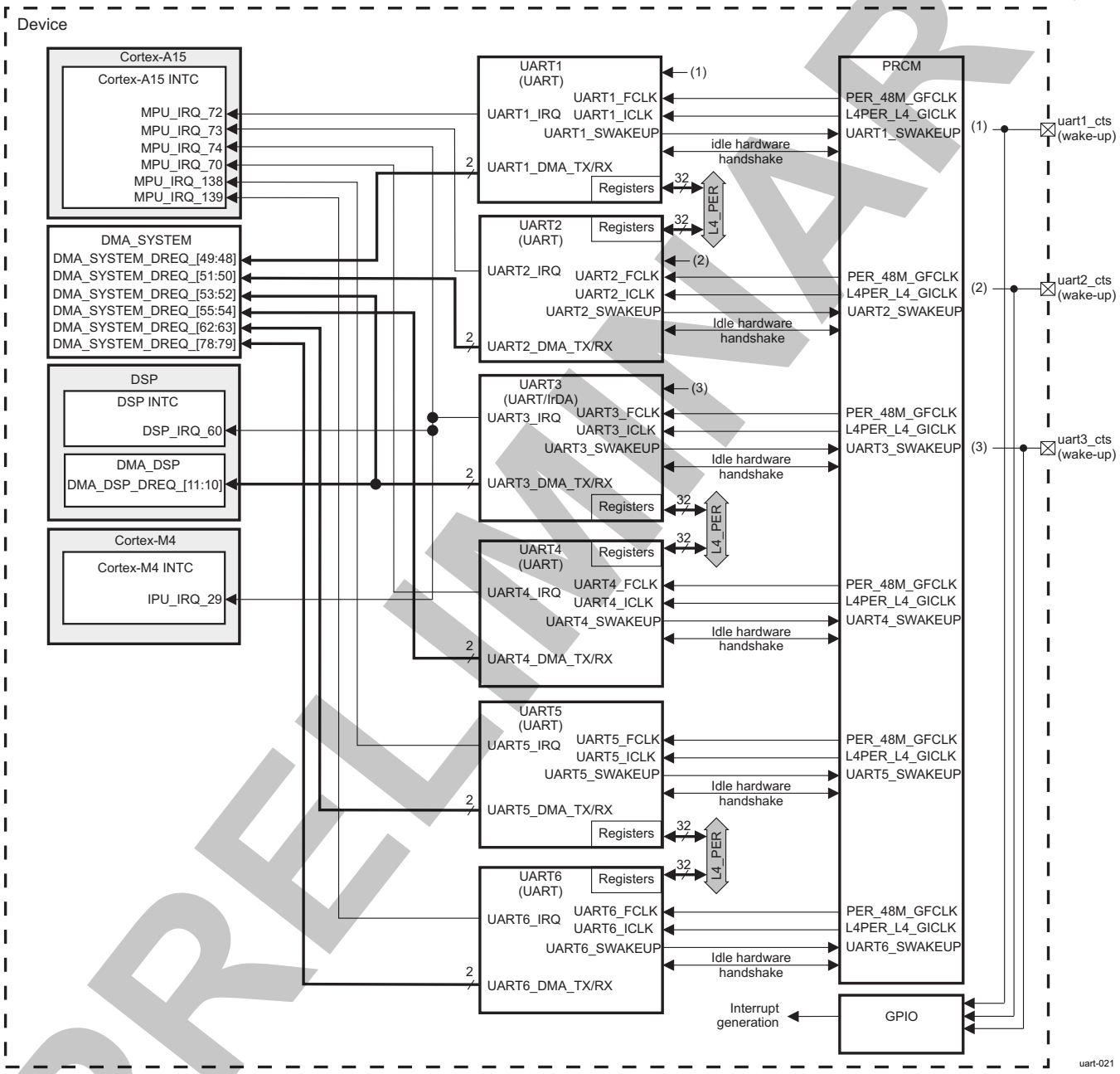
23.3.3 UART/IrDA/CIR Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-60 shows the device internal connections with related modules for UART functions.

Figure 23-60. UART/IrDA/CIR Integration



NOTE: For more information about the idle and standby hardware handshakes and the wake-up request, see Section 3.1.1.1.4, *Clock Domain Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*

Table 23-131 through Table 23-133 summarize the integration of the module in the device.

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Table 23-131. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
UART1	PD_CORE	Yes	L4_PER
UART2	PD_CORE	Yes	L4_PER
UART3	PD_CORE	Yes	L4_PER
UART4	PD_CORE	Yes	L4_PER
UART5	PD_CORE	Yes	L4_PER
UART6	PD_CORE	Yes	L4_PER

Table 23-132. Clocks and Resets

Clocks				
Module Instance	**Destination Signal**	**Source Signal**	**Source**	**Description**
UART1	UART1_ICLK	L4PER_L4_GICLK	PRCM	UART1 interface clock
	UART1_FCLK	PER_48M_GFCLK	PRCM	UART1 functional clock
UART2	UART2_ICLK	L4PER_L4_GICLK	PRCM	UART2 interface clock
	UART2_FCLK	PER_48M_GFCLK	PRCM	UART2 functional clock
UART3	UART3_ICLK	L4PER_L4_GICLK	PRCM	UART3 interface clock
	UART3_FCLK	PER_48M_GFCLK	PRCM	UART3 functional clock
UART4	UART4_ICLK	L4PER_L4_GICLK	PRCM	UART4 interface clock
	UART4_FCLK	PER_48M_GFCLK	PRCM	UART4 functional clock
Resets				
Module Instance	**Destination Signal**	**Source Signal**	**Source**	**Description**
UART1	UART1_RST	CORE_RST	PRCM	UART1 reset
UART2	UART2_RST	CORE_RST	PRCM	UART2 reset
UART3	UART3_RST	CORE_RST	PRCM	UART3 reset
UART4	UART4_RST	CORE_RST	PRCM	UART4 reset

Table 23-133. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal**	**Destination Signal**	**Destination**	**Description**
UART1	UART1_IRQ	MPU_IRQ_72	Cortex-A15	UART module 1
UART2	UART2_IRQ	MPU_IRQ_73	Cortex-A15	UART module 2
UART3	UART3_IRQ	DSP_IRQ_60	DSP	UART module 3 (also infrared)
	UART3_IRQ	MPU_IRQ_74	Cortex-A15	UART module 3 (also infrared)
	UART3_IRQ	IPU_IRQ_29	Cortex-M4	UART module 3 (also infrared)
UART4	UART4_IRQ	MPU_IRQ_70	Cortex-A15	UART module 4
UART5	UART5_IRQ	MPU_IRQ_138	Cortex-A15	UART module 5
UART6	UART6_IRQ	MPU_IRQ_139	Cortex-A15	UART module 6
Direct Memory Access (DMA) Requests				
Module Instance	**Source Signal**	**Destination Signal**	**Destination**	**Description**
UART1	UART1_DMA_TX	DMA_SYSTEM_DREQ_48	DMA_SYSTEM	UART module 1 – transmit request
	UART1_DMA_RX	DMA_SYSTEM_DREQ_49	DMA_SYSTEM	UART module 1 – receive request
UART2	UART2_DMA_TX	DMA_SYSTEM_DREQ_50	DMA_SYSTEM	UART module 2 – transmit request

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Table 23-133. Hardware Requests (continued)

	UART2_DMA_RX	DMA_SYSTEM_DREQ_51	DMA_SYSTEM	UART module 2 – receive request
UART3	UART3_DMA_TX	DMA_SYSTEM_DREQ_52	DMA_SYSTEM	UART module 3 – transmit request (also infrared)
	UART3_DMA_RX	DMA_SYSTEM_DREQ_53	DMA_SYSTEM	UART module 3 – receive request (also infrared)
	UART3_DMA_TX	DMA_DSP_DREQ_10	DMA_DSP	UART module 3 – transmit request
	UART3_DMA_RX	DMA_DSP_DREQ_11	DMA_DSP	UART module 3 – receive request
UART4	UART4_DMA_TX	DMA_SYSTEM_DREQ_54	DMA_SYSTEM	UART module 4 – transmit request
	UART4_DMA_RX	DMA_SYSTEM_DREQ_55	DMA_SYSTEM	UART module 4 – receive request
UART5	UART5_DMA_TX	DMA_SYSTEM_DREQ_62	DMA_SYSTEM	UART module 5 – transmit request
	UART5_DMA_RX	DMA_SYSTEM_DREQ_63	DMA_SYSTEM	UART module 5 – receive request
UART6	UART6_DMA_TX	DMA_SYSTEM_DREQ_78	DMA_SYSTEM	UART module 6 – transmit request
	UART6_DMA_RX	DMA_SYSTEM_DREQ_79	DMA_SYSTEM	UART module 6 – receive request

23.3.4 UART/IrDA/CIR Functional Description

23.3.4.1 Block Diagram

The UART/IrDA/CIR module can be divided into three main blocks:

- FIFO management
- Mode selection
- Protocol formatting

FIFO management is common to all functions and enables the transmission and reception of data from the host processor point of view.

There are two modes:

- Function mode: Routes the data to the chosen function (UART, IrDA, or CIR) and enables the mechanism corresponding to the chosen function
- Register mode: Enables conditional access to registers

For more information about mode configuration, see Section 23.3.4.7, *Mode Selection*.

Protocol formatting has three subcategories:

- Clock generation: The 48-MHz input clock generates all necessary clocks.
- Data formatting: Each function uses its own state-machine that is responsible for the transition between FIFO data and frame data associated with it.
- Interrupt management: Different interrupt types are generated depending on the chosen function:
  - UART mode interrupts: Seven interrupts prioritized in six different levels
  - IrDA mode interrupts: Eight interrupts. The interrupt line is activated when any interrupt is generated (there is no priority).
  - CIR mode interrupts: A subset of existing IrDA mode interrupts is used.

  In each mode, when an interrupt is generated, the UART_IIR register indicates the interrupt type.

In parallel with these functional blocks, a power-saving strategy exists for each function.

Figure 23-61 is the UART/IrDA/CIR block diagram.

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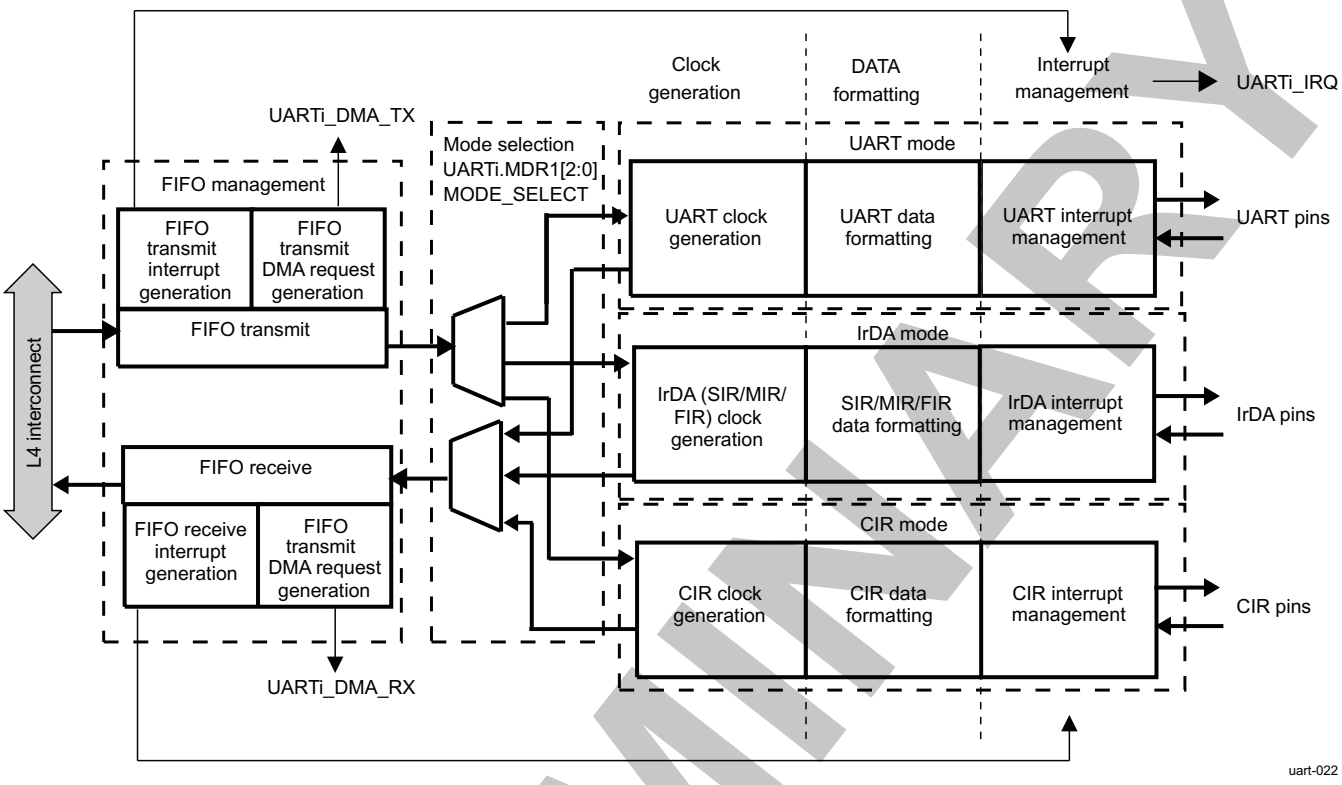
Figure 23-61. UART/IrDA/CIR Functional Specification Block Diagram



23.3.4.2 Clock Configuration

Each UART uses a 48-MHz functional clock for its logic and to generate external interface signals. Each UART uses an interface clock for register accesses. The PRCM module generates and controls all these clocks (for more information, see Section 3.1.1.1.4, *Clock Domain Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*).

The idle and wake-up processes use a handshake protocol between the PRCM and the UART (for a description of the protocol, see Section 3.1.1.1.4, *Clock Domain Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*). The UARTi.UART_SYSC[4:3] IDLEMODE bit field controls UART idle mode.

23.3.4.3 Software Reset

The UARTi.UART_SYSC[1] SOFTRESET bit controls the software reset; setting this bit to 1 triggers a software reset functionally equivalent to hardware reset.

23.3.4.4 Power Management

23.3.4.4.1 UART Mode Power Management

23.3.4.4.1.1 Module Power Saving

In UART modes, sleep mode is enabled by setting the UARTi.UART_IER[4] SLEEP_MODE bit to 1 (when the UARTi.UART_EFR[4] ENHANCED_EN bit is set to 1).

Sleep mode is entered when all of the following conditions exist:

- The serial data input line, uarti_rx, is idle.
- The TX FIFO and TX shift register are empty.
- The RX FIFO is empty.

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- The only pending interrupts are THR interrupts.

Sleep mode is a good way to lower UART power consumption, but this state can be achieved only when the UART is set to modem mode. Therefore, even if the UART has no key role functionally, it must be initialized in a functional mode to take advantage of sleep mode.

In sleep mode, the module clock and baud rate clock are stopped internally. Because most registers are clocked by these clocks, this greatly reduces power consumption. The module wakes up when a change is detected on the uarti_rx line, when data is written to the TX FIFO, and when there is a change in the state of the modem input pins.

An interrupt can be generated on a wake-up event by setting the UARTi.UART_SCR[4] RX_CTS_WU_EN bit to 1. To understand how to manage the interrupt, see Section 23.3.4.5.1.2, *Wake-Up Interrupt*.

NOTE: There must be no writing to the divisor latches, UARTi.UART_DLL and UARTi.UART_DLH, to set the baud clock (BCLK) while in sleep mode. It is advisable to disable sleep mode using the UARTi.UART_IER[4] SLEEP_MODE bit before writing to the UARTi.UART_DLL or UARTi.UART_DLH register.

23.3.4.4.1.2 System Power Saving

Sleep and auto-idle modes are embedded power-saving features. Power-reduction techniques can be applied at the system level by shutting down certain internal clock and power domains of the device.

The UART supports an idle req/idle ack handshaking protocol used at the system level to shut down the UART clocks in a clean and controlled manner and to switch the UART from interrupt-generation mode to wake-up generation mode for unmasked events (see the UARTi.UART_SYSC[2] ENAWAKEUP bit and the UARTi.UART_WER register).

For more information, see Section 3.1.1.1.2, *Module Level Clock Management*, Chapter 3, *Power, Reset, and Clock Management*.

23.3.4.4.2 IrDA Mode Power Management (UART3 Only)

23.3.4.4.2.1 Module Power Saving

In IrDA modes, sleep mode is enabled by setting the UART3.MDR[3] IR_SLEEP bit to 1.

Sleep mode is entered when all of the following conditions exist:

- The serial data input line, uart3.rx_irrx, is idle.
- The TX FIFO and TX shift register are empty.
- The RX FIFO is empty.
- No interrupts are pending except THR interrupts.

The module wakes up when a change is detected on the uart3_rx_irrx line or when data is written to the TX FIFO.

23.3.4.4.2.2 System Power Saving

System power saving for the IrDA mode has the same function as for the UART mode (see Section 23.3.4.4.1.2, *System Power Saving*).

23.3.4.4.3 CIR Mode Power Management (UART3 Only)

23.3.4.4.3.1 Module Power Saving

Module power saving for the CIR mode has the same function as for the IrDA mode (see Section 23.3.4.4.2.1, *Module Power Saving*).

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23.3.4.4.3.2 System Power Saving

System power saving for the CIR mode has the same function as for the UART mode (see Section 23.3.4.4.1.2, *System Power Saving*).

23.3.4.4.4 Local Power Management

Table 23-134 describes power-management features available for the UART.

NOTE: For information about source clock gating and the sleep/wake-up transitions description, see Section 3.1.1.1.2, *Module Level Clock Management*, Chapter 3, *Power, Reset, and Clock Management*.

Table 23-134. Local Power-Management Features

Feature	Registers	Description
Clock autogating	UART_SYSC[0] AUTOIDLE	This bit allows local power optimization in the module by gating the UARTi_ICLK clock on interface activity or gating the UARTi_FCLK clock on internal activity.
Slave idle modes	UART_SYSC[4:3] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available.
Clock activity	N/A	Feature not available
Master standby modes	N/A	Feature not available
Global wake-up enable	UART_SYSC[2] ENAWAKEUP	This bit enables the wake-up feature at module level.
Wake-Up sources enable	N/A	Feature not available

23.3.4.5 Interrupt Requests

23.3.4.5.1 UART Mode Interrupt Management

23.3.4.5.1.1 UART Interrupts

UART mode includes seven possible interrupts prioritized to six levels.

When an interrupt is generated, the interrupt identification register (UARTi.UART_IIR) sets the UARTi.UART_IIR[0] IT_PENDING bit to 0 to indicate that an interrupt is pending, and indicates the type of interrupt through the UARTi.UART_IIR[5:1] bit field. Table 23-135 summarizes the interrupt control functions.

Table 23-135. UART Mode Interrupts

UART_IIR[5:0]	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
000001	None	None	None	None
000110	1	Receiver line status	OE, FE, PE, or BI errors occur in characters in the RX FIFO.	FE, PE, BI: Read the UART_RHR register. OE: Read the UART_LSR register.
001100	2	RX time-out	Stale data in RX FIFO	Read the UART_RHR register.
000100	2	RHR interrupt	DRDY (data ready) (FIFO disable)	Read the UART_RHR register until the interrupt condition disappears.
			RX FIFO above trigger level (FIFO enable)	
000010	3	THR interrupt	TFE (UART_THR empty) (FIFO disable)	Write to the UART_THR until the interrupt condition disappears.
			TX FIFO below trigger level (FIFO enable)	

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Table 23-135. UART Mode Interrupts (continued)

UART_IIR[5:0]	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
000000	4	Modem status	See the UART_MSR register.	Read the UART_MSR register.
010000	5	XOFF interrupt/special character interrupt	Receive XOFF characters/special character	Receive XON character(s), if XOFF interrupt/read of the UART_IIR register, if special character interrupt.
100000	6	CTS, RTS	RTS pin or CTS pin change state from active (low) to inactive (high).	Read the UART_IIR register.

For the receiver-line status interrupt, the RX_FIFO_STS bit (UARTi.UART_LSR[7]) generates the interrupt.

For the XOFF interrupt, if an XOFF flow character detection caused the interrupt, the interrupt is cleared by an XON flow character detection. If special character detection caused the interrupt, the interrupt is cleared by a read of the UARTi.UART_IIR register.

23.3.4.5.1.2 Wake-Up Interrupt

Wake-up interrupt is a special interrupt that works differently from other interrupts. This interrupt is enabled when the UARTi.UART_SCR[4] RX_CTS_WU_EN bit is set to 1. The UARTi.UART_IIR register is not modified when this occurs; the UART3.UART_SSR[1] RX_CTS_WU_STS bit must be checked to detect a wake-up event.

When a wake-up interrupt occurs, it can be cleared only by resetting the UARTi.UART_SCR[4] RX_CTS_WU_EN bit. This bit must be reenabled (set to 1) after the current wake-up interrupt event is processed to detect the next incoming wake-up event.

23.3.4.5.2 IrDA Mode Interrupt Management

23.3.4.5.2.1 IrDA Interrupts

The IrDA function generates interrupts. All interrupts can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART3.UART_IER). The interrupt status of the device can be checked by reading the interrupt identification register (UART3.UART_IIR).

UART, IrDA, and CIR modes have different interrupts in the UART/IrDA/CIR module and, therefore, different UART3.UART_IER and UART3.UART_IIR mappings, depending on the selected mode.

IrDA modes have eight possible interrupts (see Table 23-136). The interrupt line is activated when any interrupt is generated (there is no priority).

Table 23-136. IrDA Mode Interrupts

UART_IIR Bit	Interrupt Type	Interrupt Source	Interrupt Reset Method
0	RHR interrupt	DRDY (data ready) (FIFO disable) RX FIFO above trigger level (FIFO enable)	Read the UART_RHR register until the interrupt condition disappears.
1	THR interrupt	TFE (UART_THR empty) (FIFO disable) TX FIFO below trigger level (FIFO enable)	Write to the UART_THR until the interrupt condition disappears.
2	Last byte in RX FIFO	Last byte of frame in RX FIFO is available to be read at the RHR port.	Read the UART_RHR register.
3	RX overrun	Write to the UART_RHR register when the RX FIFO is full.	Read UART_RESUME register.

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Table 23-136. IrDA Mode Interrupts (continued)

UART_IIR Bit	Interrupt Type	Interrupt Source	Interrupt Reset Method
4	Status FIFO interrupt	Status FIFO triggers level reached.	Read STATUS FIFO.
5	TX status	1. UART_THR empty before EOF sent. Last bit of transmission of the IrDA frame occurred, but with an underrun error. OR 2. Transmission of the last bit of the IrDA frame completed successfully.	1. Read the UART_RESUME register. OR 2. Read the UART_IIR register.
6	Receiver line status interrupt	CRC, ABORT, or frame-length error is written into the STATUS FIFO.	Read the STATUS FIFO (read until empty - maximum of eight reads required).
7	Received EOF	Received end-of-frame	Read the UART_IIR register.

23.3.4.5.2.2 Wake-Up Interrupts

The wake-up interrupt for IrDA mode has the same function as that for UART mode (see Section 23.3.4.5.1.2, *Wake-Up Interrupt*).

CAUTION

Wake-up interface implementation in this mode is based on the UARTi_SIDLEACK low-to-high transition instead of the UARTi_SIDLEACK state.

This does not ensure wake-up event generation as expected when configured in smart-idle mode, and the system wakes up for a short period.

23.3.4.5.3 CIR Mode Interrupt Management

23.3.4.5.3.1 CIR Interrupts

The CIR function generates interrupts that can be enabled and disabled by writing to the appropriate bit in the interrupt enable register (UART3.UART_IER). The interrupt status of the device can be checked by reading the interrupt identification register (UART3.UART_IIR).

UART, IrDA, and CIR modes have different interrupts in the UART/IrDA/CIR module and, therefore, different UART3.UART_IER and UART3.UART_IIR mappings, depending on the selected mode.

Table 23-137 lists the interrupt modes to be maintained. In CIR mode, the sole purpose of the UART3.UART_IIR[5] bit is to indicate that the last bit of infrared data was passed to the uart3_cts_rctx pin.

Table 23-137. CIR Mode Interrupts

UART_IIR Bit Number	Interrupt Type	Interrupt Source	Interrupt Reset Method
0	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
1	THR interrupt	TFE (UART_THR empty) (FIFO disable) TX FIFO below trigger level (FIFO enable)	Write to the UART_THR register until the interrupt condition disappears.
2	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
3	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
4	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode

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Table 23-137. CIR Mode Interrupts (continued)

UART_IIR Bit Number	Interrupt Type	Interrupt Source	Interrupt Reset Method
5	TX status	Transmission of the last bit of the frame is complete successfully.	Read the UART_IIR register.
6	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode
7	N/A for CIR mode	N/A for CIR mode	N/A for CIR mode

23.3.4.5.3.2 Wake-Up Interrupts

The wake-up interrupt for CIR mode has the same function as that for UART mode (see Section 23.3.4.5.1.2, *Wake-Up Interrupt*).

23.3.4.6 FIFO Management

The FIFO is accessed by reading and writing the UARTi.UART_RHR and UARTi.UART_THR registers. Parameters are controlled using the FIFO control register (UARTi.UART_FCR) and supplementary control register (UARTi.UART_SCR). Reading the UARTi.UART_SSR[0] TX_FIFO_FULL bit at 1 means the FIFO is full.

The UARTi.UART_TLR register controls the FIFO trigger level, which enables DMA and interrupt generation. After reset, transmit (TX) and receive (RX) FIFOs are disabled; thus, the trigger level is the default value of 1 byte. Figure 23-62 shows the FIFO management registers.

NOTE: Data in the UARTi.UART_RHR register is not overwritten when an overflow occurs.

NOTE: The UARTi.UART_SFLSR, UARTi.UART_SFREGL, and UARTi.UART_SFREGH status registers are used in IrDA mode only. For information about their use, see Section 23.3.4.8.2.3, *IrDA Data Formatting*.

NOTE: Bits UART_FCR[2] TX_FIFO_CLEAR and UART_FCR[1] RX_FIFO_CLEAR are automatically cleared by hardware after 4* L4PER_L4_GICLK + 5* PER_48M_GFCLK clock cycles. This delay is needed to finish the resetting of the corresponding FIFO and DMA control registers.

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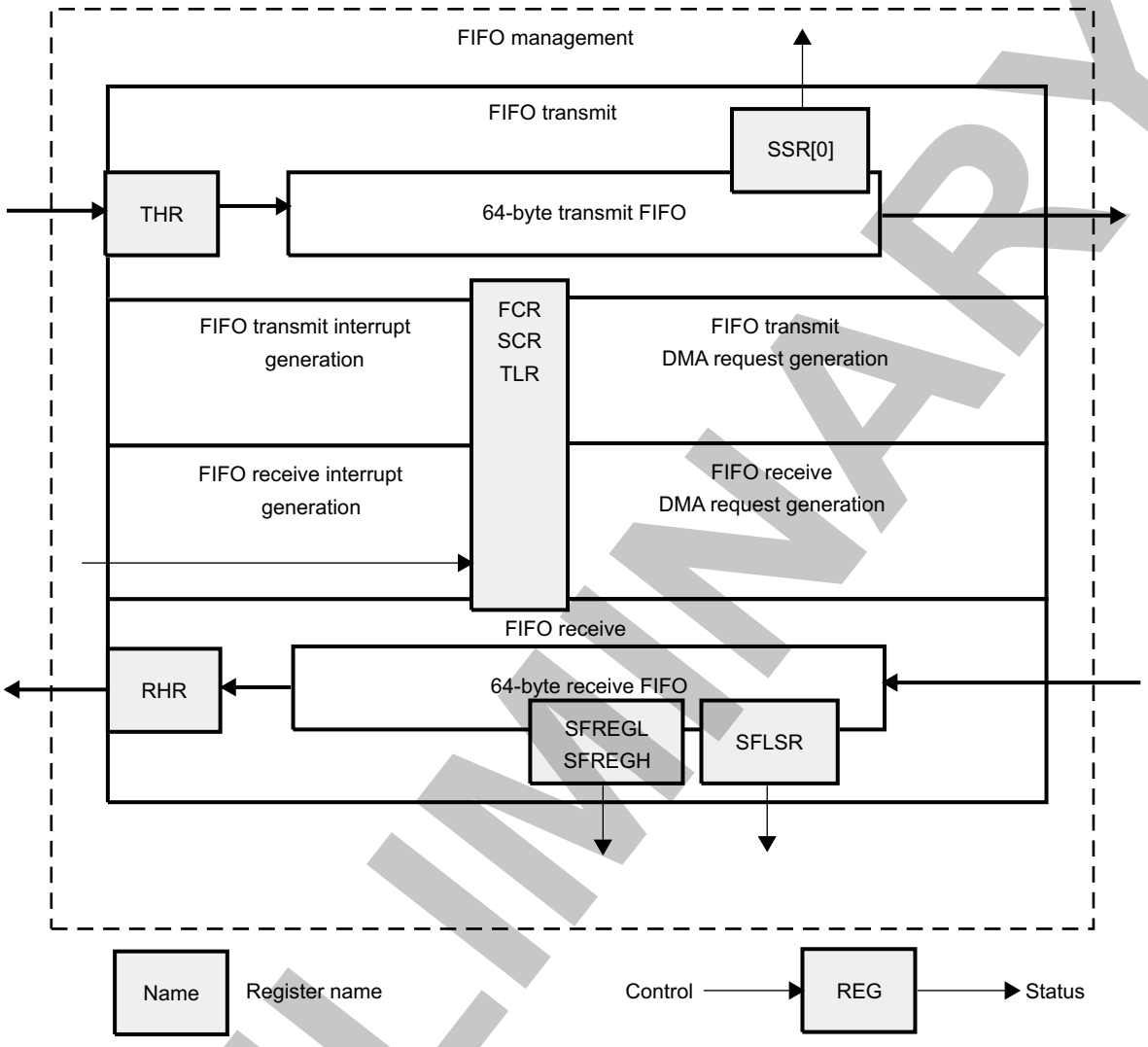
Figure 23-62. FIFO Management Registers



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23.3.4.6.1 FIFO Trigger

23.3.4.6.1.1 Transmit FIFO Trigger

Table 23-138 lists the TX FIFO trigger level settings.

Table 23-138. TX FIFO Trigger Level Setting Summary

UART_SCR[6]	UART_TLR[3:0]	TX FIFO Trigger Level
0	= 0x0	Defined by the UARTi.UART_FCR[5:4] TX_FIFO_TRIG bit field (8,16, 32, or 56 spaces)
0	!= 0x0	Defined by the UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA bit field (from 4 to 60 spaces with a granularity of 4 spaces)
1	Value	Defined by the concatenated value of TX_FIFO_TRIG_DMA and TX_FIFO_TRIG (from 1 to 63 spaces with a granularity of 1 space) **Note:** The combination of TX_FIFO_TRIG_DMA = 0x0 and TX_FIFO_TRIG = 0x0 (all zeros) is not supported (minimum of 1 space required). All zeros result in unpredictable behavior.

23.3.4.6.1.2 Receive FIFO Trigger

Table 23-139 lists the RX FIFO trigger-level settings.

Table 23-139. RX FIFO Trigger-Level Setting Summary

UART_SCR[7]	UART_TLR[7:4]	RX FIFO Trigger Level
0	= 0x0	Defined by the UARTi.UART_FCR[7:6] RX_FIFO_TRIG bit field (8,16, 56, or 60 characters)
0	!= 0x0	Defined by the UARTi.UART_TLR[7:4] RX_FIFO_TRIG_DMA bit field (from 4 to 60 characters with a granularity of 4 characters)
1	Value	Defined by the concatenated value of RX_FIFO_TRIG_DMA and RX_FIFO_TRIG (from 1 to 63 characters with a granularity of 1 character) **Note:** The combination of RX_FIFO_TRIG_DMA = 0x0 and RX_FIFO_TRIG = 0x0 (all zeros) is not supported (minimum of 1 character required). All zeros result in unpredictable behavior.

The receive threshold is programmed using the UARTi.UART_TCR[7:4] RX_FIFO_TRIG_START and UARTi.UART_TCR[3:0] RX_FIFO_TRIG_HALT bit fields:

- Trigger levels from 0 to 60 bytes are available with a granularity of 4 (trigger level = 4 × [4-bit register value]).
- To ensure correct device operation, ensure that RX_FIFO_TRIG_HALT > RX_FIFO_TRIG when auto-RTS is enabled.

  Delay = [4 + 16 × (1 + CHAR_LENGTH + Parity + Stop – 0.5)] × Baud_rate + 4 × FCLK

  NOTE: The RTS signal is deasserted after the UART module receives the data over RX_FIFO_TRIG_HALT. Delay means how long the UART module takes to deassert the RTS signal after reaching RX_FIFO_TRIG_HALT.

- In FIFO interrupt mode with flow control, ensure that the trigger level to HALT transmission is greater than or equal to the RX FIFO trigger level (the UARTi.UART_TCR[7:4] RX_FIFO_TRIG_START bit field or the UARTi.UART_FCR[7:6] RX_FIFO_TRIG bit field); otherwise, FIFO operation stalls. In FIFO DMA mode with flow control, this concept does not exist, because a DMA request is sent when a byte is received.

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23.3.4.6.2 FIFO Interrupt Mode

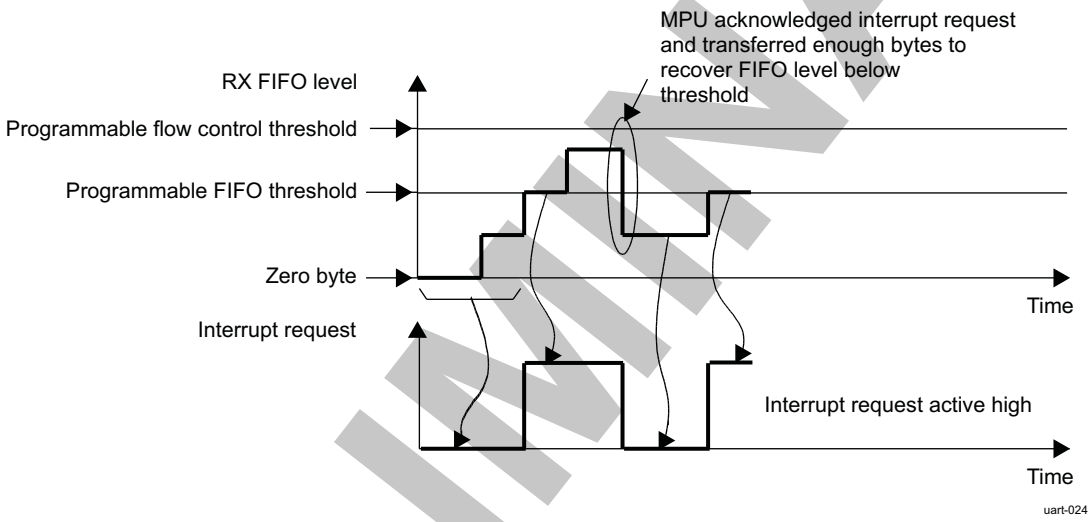
In FIFO interrupt mode (the FIFO control register UARTi.UART_FCR[0] FIFO_EN bit is set to 1 and relevant interrupts are enabled by the UARTi.UART_IER register), an interrupt signal informs the processor of the status of the receiver and transmitter. These interrupts are raised when the RX/TX FIFO threshold (the UARTi.UART_TLR[7:4] RX_FIFO_TRIG_DMA and UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA bit fields or the UARTi.UART_FCR[7:6] RX_FIFO_TRIG and UARTi.UART_FCR[5:4] TX_FIFO_TRIG bit fields, respectively) is reached.

The interrupt signals instruct the MPU to transfer data to the destination (from the UART in receive mode and/or from any source to the UART FIFO in transmit mode).

When UART flow control is enabled with interrupt capabilities, the UART flow control FIFO threshold (the UARTi.UART_TCR[3:0] RX_FIFO_TRIG_HALT bit field) must be greater than or equal to the RX FIFO threshold.

Figure 23-63 shows the generation of the RX FIFO interrupt request.

Figure 23-63. RX FIFO Interrupt Request Generation



In receive mode, no interrupt is generated until the RX FIFO reaches its threshold. Once low, the interrupt can be deasserted only when the MPU has handled enough bytes to put the FIFO level below threshold. The flow control threshold is set at a higher value than the FIFO threshold.

Figure 23-64 shows the generation of the TX FIFO interrupt request.

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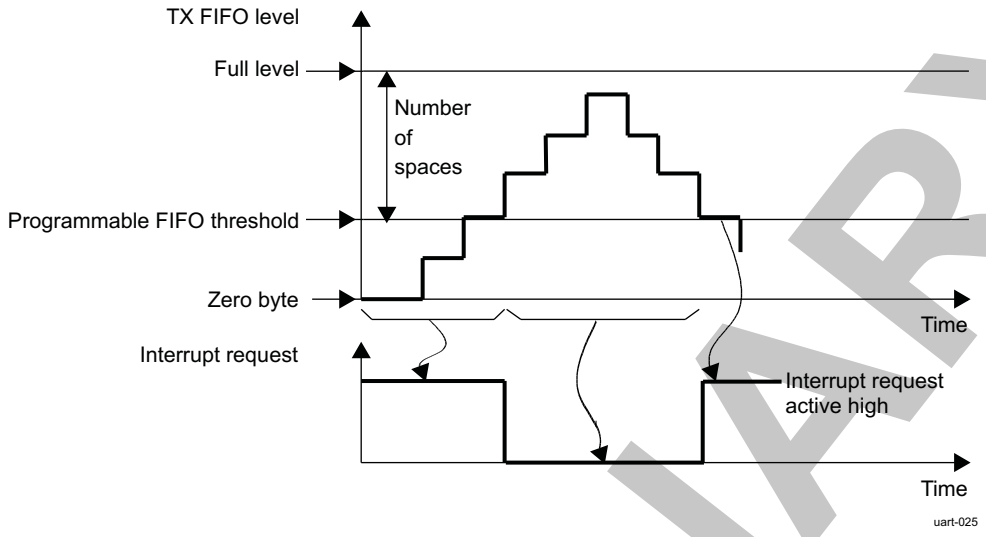
Figure 23-64. TX FIFO Interrupt Request Generation



In transmit mode, an interrupt request is automatically asserted when the TX FIFO is empty. This request is deasserted when the TX FIFO crosses the threshold level. The interrupt line is deasserted until a sufficient number of elements is transmitted to go below the TX FIFO threshold.

23.3.4.6.3 FIFO Polled Mode Operation

In FIFO polled mode (the UARTi.UART_FCR[0] FIFO_EN bit is set to 0 and the relevant interrupts are disabled by the UARTi.UART_IER register), the status of the receiver and transmitter can be checked by polling the line status register (UARTi.UART_LSR).

This mode is an alternative to the FIFO interrupt mode of operation in which the status of the receiver and transmitter is automatically determined by sending interrupts to the MPU.

23.3.4.6.4 FIFO DMA Mode Operation

Although the DMA operation includes four modes (DMA modes 0 through 3), the information in Table 23-133 assumes that mode 1 is used. (Mode 2 and mode 3 are legacy modes that use only one DMA request for each module.)

In mode 2, the remaining DMA request is used for RX. In mode 3, the remaining DMA request is used for TX.

DMA requests in mode 2 and mode 3 use the following signals:

- S_DMA_48
- S_DMA_50
- S_DMA_52/D_DMA_10
- S_DMA_54

The following signals are not used by the module in mode 2 and mode 3:

- S_DMA_49
- S_DMA_51
- S_DMA_53/D_DMA_11
- S_DMA_55

These signals can be selected as follows:

- When the UARTi.UART_SCR[0] DMA_MODE_CTL bit is set to 0, setting the UARTi.UART_FCR[3] DMA_MODE_CTL bit to 0 enables DMA mode 0. Setting the DMA_MODE_CTL bit to 1 enables DMA mode 1.
- When the DMA_MODE_CTL bit is set to 1, the UARTi.UART_FCR[2:1] DMA_MODE_2 bit field

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determines DMA mode 0 to mode 3 based on the supplementary control register (UART_SCR) description.

For example:

- If no DMA operation is desired, set the DMA_MODE_CTL bit to 1 and the DMA_MODE_2 bit field to 0x0. (The DMA_MODE bit is discarded.)
- If DMA mode 1 is desired, set the DMA_MODE_CTL bit to 0 and the DMA_MODE bit to 1, or set the DMA_MODE_CTL bit to 1 and the DMA_MODE_2 bit field to 01. (The DMA_MODE bit is discarded.)

If the FIFOs are disabled (the UARTi.UART_FCR[0] FIFO_EN bit is set to 0), the DMA occurs in single-character transfers.

When DMA mode 0 is programmed, the signals associated with DMA operation are not active.

Depending on UART_MDR3[2] SET_DMA_TX_THRESHOLD, the threshold can be programmed different ways:

- SET_TX_DMA_THRESHOLD = 1:

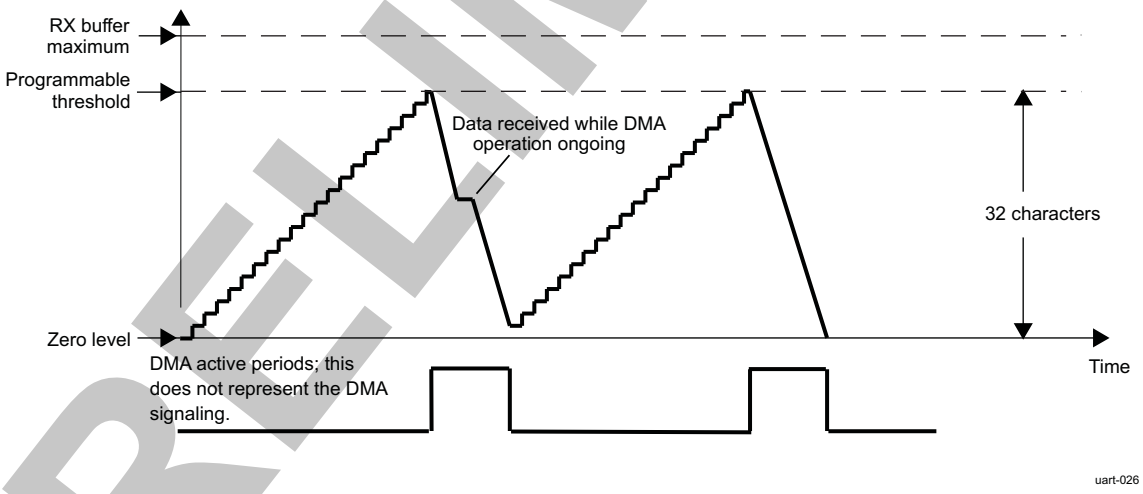
  The threshold value will be the value of the UART_TX_DMA_THRESHOLD register. If SET_TX_DMA_THRESHOLD + TX trigger spaces 64, then the default method of threshold is used: threshold value = TX FIFO size.
- SET_TX_DMA_THRESHOLD = 0:

  The threshold value = TX FIFO size TX trigger space. The TX DMA line is asserted if the TX FIFO level is lower then the threshold. It remains asserted until TX trigger spaces number of bytes are written into the FIFO. The DMA line is then deasserted and the FIFO level is compared with the threshold value.

23.3.4.6.4.1 DMA Transfers (DMA Mode 1, 2, or 3)

Figure 23-65 through Figure 23-68 show the supported DMA operations.

Figure 23-65. Receive FIFO DMA Request Generation (32 Characters)



In receive mode, a DMA request is generated when the RX FIFO reaches its threshold level defined in the trigger level register (UARTi.UART_TLR). This request is deasserted when the number of bytes defined by the threshold level is read by the sDMA.

In transmit mode, a DMA request is automatically asserted when the TX FIFO is empty. This request is deasserted when the number of bytes defined by the number of spaces in the UARTi.UART_TLR register is written by the sDMA. If an insufficient number of characters is written, the DMA request stays active.

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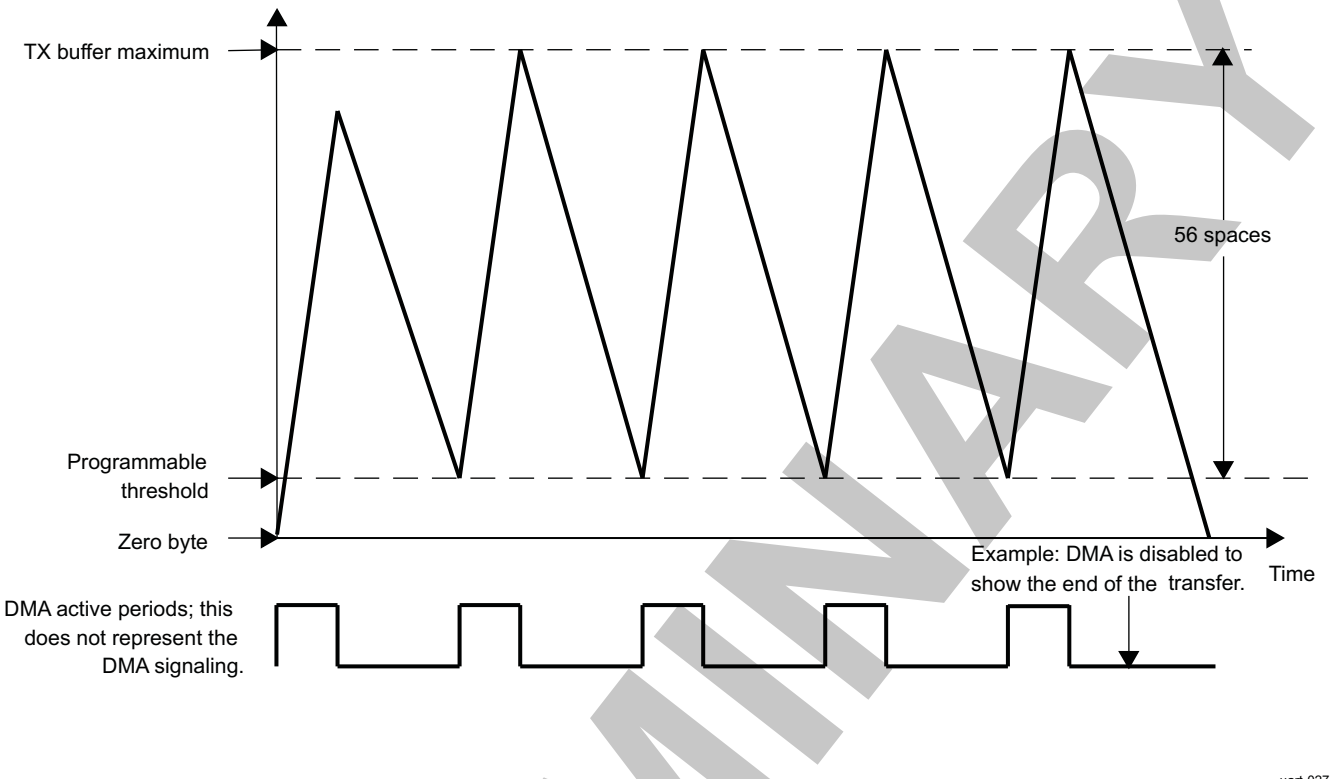
Figure 23-66. Transmit FIFO DMA Request Generation (56 Spaces)



The DMA request is again asserted if the FIFO can receive the number of bytes defined by the UARTi.UART_TLR register.

The threshold can be programmed in a number of ways. Figure 23-66 shows a DMA transfer operating with a space setting of 56 that can arise from using the auto settings in the UARTi.UART_FCR[5:4] TX_FIFO_TRIG bit field or the UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA bit field concatenated with the TX_FIFO_TRIG bit field.

The setting of 56 spaces in the UART/IrDA/CIR module must correlate with the settings of the sDMA so that the buffer does not overflow (program the DMA request size of the LH controller to equal the number of spaces in the UART/IrDA/CIR module).

Figure 23-67 shows an example with eight spaces to show the buffer level crossing the space threshold. The LH DMA controller settings must correspond to those of the UART/IrDA/CIR module.

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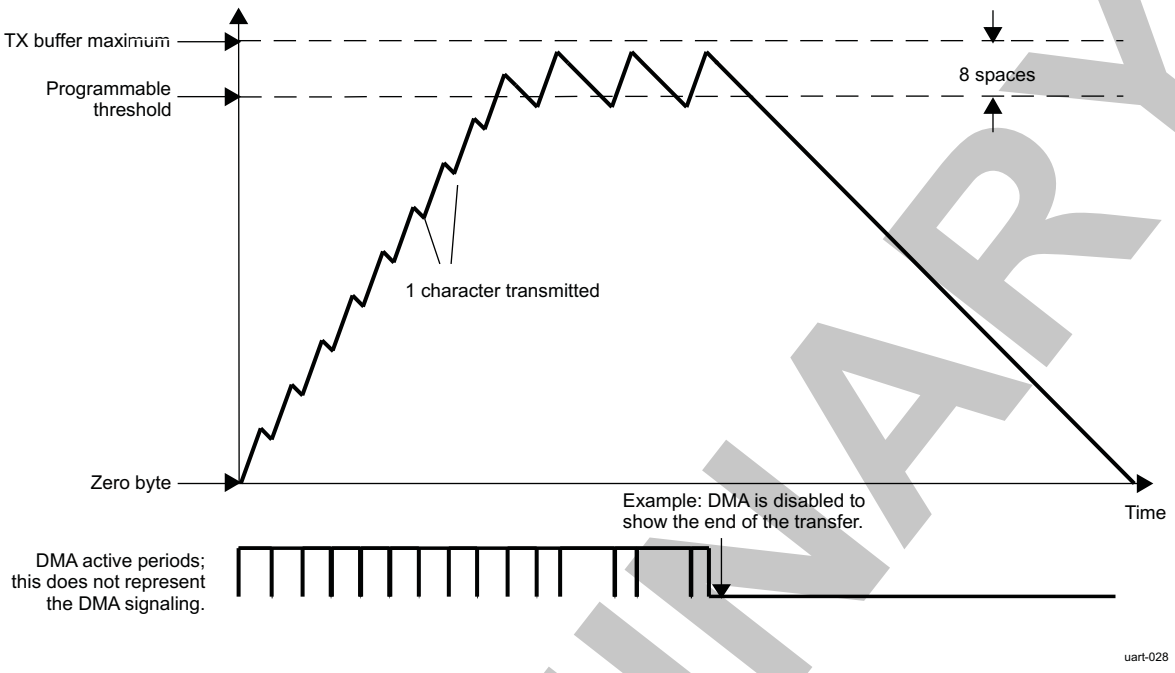
Figure 23-67. Transmit FIFO DMA Request Generation (8 Spaces)



The next example shows the setting of one space that uses the DMA for each transfer of one character to the transmit buffer (see Figure 23-68). The buffer is filled faster than the baud rate at which data is transmitted to the TX pin. Eventually, the buffer is completely full and the DMA operations stop transferring data to the transmit buffer.

On two occasions, the buffer holds the maximum amount of data words; shortly after this, the DMA is disabled to show the slower transmission of the data words to the TX pin. Eventually, the buffer is emptied at the rate specified by the baud rate settings of the UARTi.UART_DLL and UARTi.UART_DLH registers.

The DMA settings must correspond to the system LH DMA controller settings to ensure correct operation of this logic.

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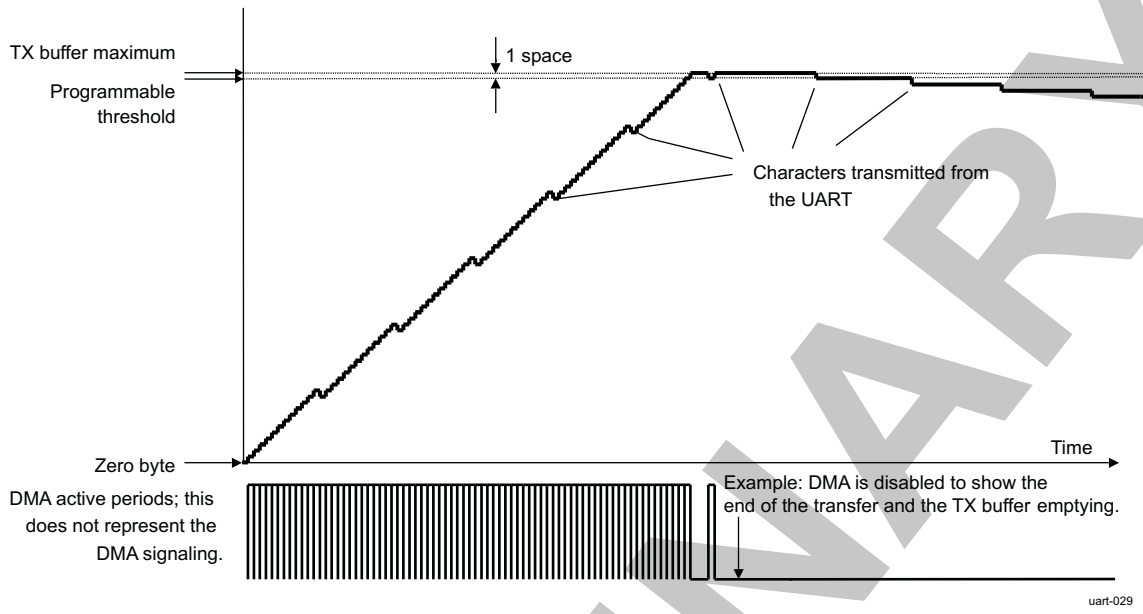
Figure 23-68. Transmit FIFO DMA Request Generation (1 Space)



The final example illustrates the setting of eight spaces but setting the TX DMA threshold directly by setting UART_MDR3[1] NONDEFAULT_FREQ bit and UART_TX_DMA_THRESHOLD register (see Figure 23-69). In the example UART_TX_DMA_THRESHOLD[5:0] TX_DMA_THRESHOLD = 3 and the trigger level is 8. The buffer is filled at a faster rate than the BAUD rate transmits data to the TX pin. The buffer is filled with 8 bytes and the DMA operations stop transferring data to the transmit buffer. When the buffer is emptied to the threshold level by transmission, the DMA operation activates again to fill the buffer with 8 bytes.

Eventually, the buffer will be emptied at the rate specified by the BAUD Rate settings of the UART_DLL and UART_DLH registers.

If the selected threshold level + trigger level exceeds max buffer size, then the original TX DMA threshold method is used to prevent TX overrun, regardless of the UART_MDR3[1] value.

The DMA settings should correspond to the system's Local Host DMA controller settings in order to ensure the correct operation of this logic.

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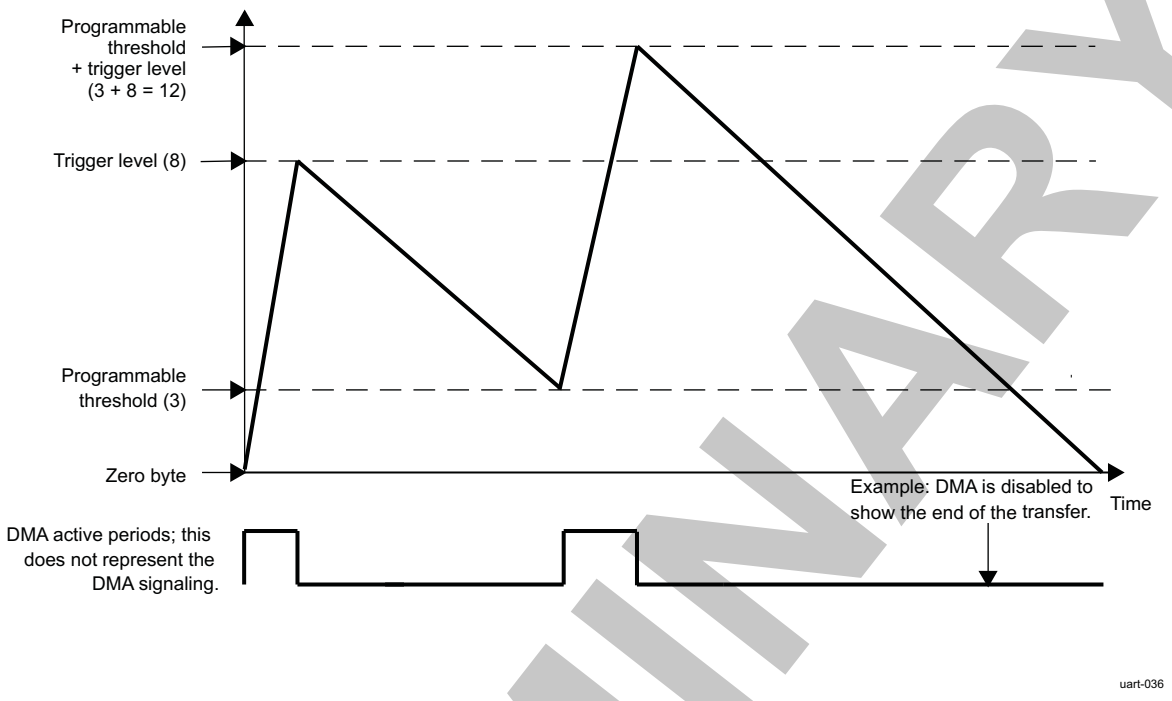
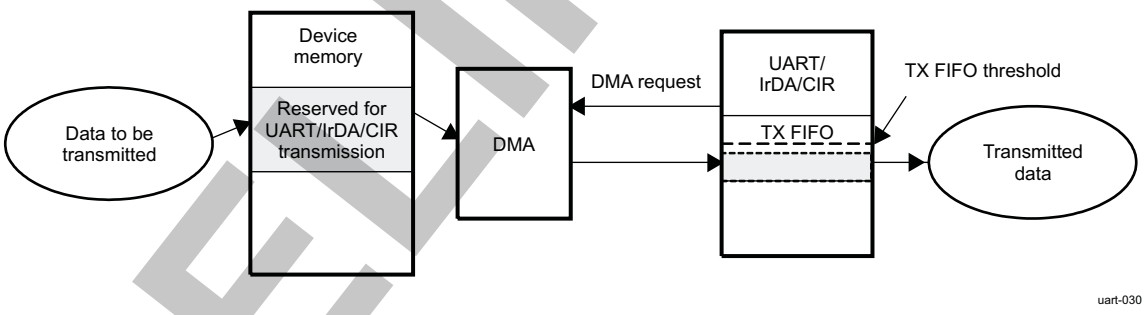
Figure 23-69. Transmit FIFO DMA Request Generation Using Direct TX DMA Threshold Programming. (Threshold = 3; Spaces = 8)



23.3.4.6.4.2 DMA Transmission

Figure 23-70 shows DMA transmission.

Figure 23-70. DMA Transmission



1. Data to be transmitted are put in the device memory reserved for UART/IrDA/CIR transmission by the DMA:
   (a) Until the TX FIFO trigger level is not reached, a DMA request is generated
   (b) An element (1 byte) is transferred from the SDRAM to the TX FIFO at each DMA request (DMA element synchronization).
2. Data in the TX FIFO are automatically transmitted.
3. The end of the transmission is signaled by the UARTi.UART_THR empty (TX FIFO empty).

NOTE: In IrDA mode, the transmission does not end immediately after the TX FIFO empties, at which point the last data byte, the CRC field, and the stop flag still must be transmitted; thus, the end of transmission occurs a few milliseconds after the UARTi.UART_THR register empties.

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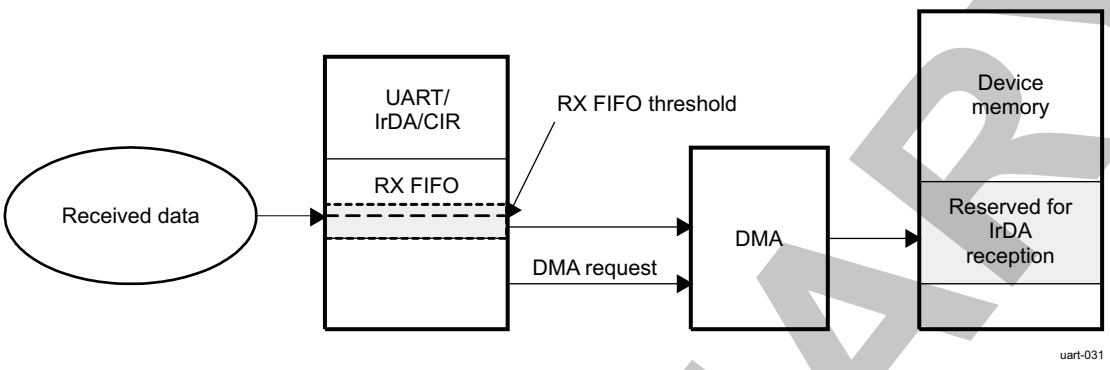
23.3.4.6.4.3 DMA Reception

Figure 23-71 shows DMA reception.

Figure 23-71. DMA Reception



1. Enable the reception.
2. Received data are put in the RX FIFO.
3. Data are transferred from the RX FIFO to the device memory by the DMA:
   (a) At each received byte, the RX FIFO trigger level (one character) is reached and a DMA request is generated.
   (b) An element (1 byte) is transferred from the RX FIFO to the SDRAM at each DMA request (DMA element synchronization).
4. The end of the reception is signaled by the EOF interrupt.

23.3.4.7 Mode Selection

23.3.4.7.1 Register Access Modes

23.3.4.7.1.1 Operational Mode and Configuration Modes

Register access depends on the register access mode, although register access modes are not correlated to functional mode selection. Three different modes are available:

- Operational mode
- Configuration mode A
- Configuration mode B

Operational mode is the selected mode when the function is active; serial data transfer can be performed in this mode.

Configuration mode A and configuration mode B are used during module initialization steps. These modes enable access to configuration registers, which are hidden in the operational mode. The modes are used when the module is inactive (no serial data transfer processed) and only for initialization or reconfiguration of the module.

The value of the UARTi.UART_LCR register determines the register access mode (see Table 23-140).

Table 23-140. UART/IrDA/CIR Register Access Mode Programming (Using UART_LCR)

Mode	Condition
Configuration mode A	UART_LCR[7] = 0x1 and UART_LCR[7:0] != 0xBF
Configuration mode B	UART_LCR[7] = 0x1 and UART_LCR[7:0] = 0xBF
Operational mode	UART_LCR[7] = 0x0

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23.3.4.7.1.2 Register Access Submode

In each access register mode (operational mode or configuration mode A/B), some register accesses are conditional on the programming of a submode (MSR_SPR, TCR_TLR, and XOFF). These registers are identified in Section 23.3.6, *UART/IrDA/CIR Register Manual*.

Table 23-141 through Table 23-143 summarize the register access submodes.

Table 23-141. Subconfiguration Mode A Summary

Mode	Condition
MSR_SPR	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

Table 23-142. Subconfiguration Mode B Summary

Mode	Condition
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1
XOFF	(UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0)

Table 23-143. Suboperational Mode Summary

Mode	Condition
MSR_SPR	UART_EFR[4] = 0x0 or UART_MCR[6] = 0x0
TCR_TLR	UART_EFR[4] = 0x1 and UART_MCR[6] = 0x1

23.3.4.7.1.3 Registers Available for the Register Access Modes

Table 23-144 lists the names of the register bits in each access register mode. Gray shading indicates that the register does not depend on the register access mode (available in all modes).

Table 23-144. UART/IrDA/CIR Register Access Mode Overview

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER	UART_IER
0x008	UART_IIR	UART_FCR	UART_EFR	UART_EFR	UART_IIR	UART_FCR
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR	–
0x018	UART_MSR (1)/UART_TCR (2)	UART_TCR (2)	UART_TCR (2)/UART_XOFF1 (3)	UART_TCR (2)/UART_XOFF1 (3)	UART_MSR (1)/UART_TCR (2)	UART_TCR (2)
0x01C	UART_SPR (1)/UART_TLR (2)	UART_SPR (1)/UART_TLR (2)	UART_TLR (2)/UART_XOFF2 (3)	UART_TLR (2)/UART_XOFF2 (3)	UART_SPR (1)/UART_TLR (2)	UART_SPR (1)/UART_TLR (2)
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL

(1) MSR_SPR mode is active (see Section 23.3.4.7.1.2, *Register Access Submode*)
(2) TCR_TLR mode is active (see Section 23.3.4.7.1.2, *Register Access Submode*)
(3) XOFF mode is active (see Section 23.3.4.7.1.2, *Register Access Submode*)

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Table 23-144. UART/IrDA/CIR Register Access Mode Overview (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	UART_UASR	–	UART_UASR	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

23.3.4.7.2 UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection

To select a mode, set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field (see Table 23-145).

Table 23-145. UART Mode Selection

Value	Mode
0x0:	UART 16x mode
0x1:	SIR mode (UART3 only)
0x2:	UART 16x auto-baud
0x3:	UART 13x mode
0x4:	MIR mode (UART3 only)
0x5:	FIR mode (UART3 only)
0x6:	CIR mode (UART3 only)

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MODE_SELECT is effective when the module is in operational mode (see Section 23.3.4.7.1, *Register Access Modes*).

23.3.4.7.2.1 Registers Available for the UART Function

Only the registers listed in Table 23-146 are used for the UART function.

Table 23-146. UART Mode Register Overview(1) (2)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER(UART)	UART_IER(UART)
0x008	UART_IIR	UART_FCR	UART_EFR[4]	UART_EFR[4]	UART_IIR(UART)	UART_FCR(UART)
0x00C	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR	UART_LCR
0x010	UART_MCR	UART_MCR	UART_XON1_ADDR1	UART_XON1_ADDR1	UART_MCR	UART_MCR
0x014	UART_LSR(UART)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR(UART)	–
0x018	UART_MSR/UART_TCR	UART_TCR	UART_XOFF1/UART_TCR	UART_XOFF1/UART_TCR	UART_MSR/UART_TCR	UART_TCR
0x01C	UART_TLR/UART_SPR	UART_TLR/UART_SPR	UART_TLR/UART_XOFF2	UART_TLR/UART_XOFF2	UART_TLR/UART_SPR	UART_TLR/UART_SPR
0x020	UART_MDR1	UART_MDR1[2:0]	UART_MDR1[2:0]	UART_MDR1[2:0]	UART_MDR1[2:0]	UART_MDR1[2:0]
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	–	–	–	–	–	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	UART_UASR	–	UART_UASR	–	–	–
0x03C	–	–	–	–	–	–
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	–	–
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER	UART_WER
0x060	–	–	–	–	–	–
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3

(1) REGISTER_NAME(UART) notation indicates that the register exists for other functions (IrDA or CIR), but fields have different meanings for other functions (described separately in Section 23.3.6, *UART/IrDA/CIR Register Manual*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the UART function.

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Table 23-146. UART Mode Register Overview[1] [2] (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

23.3.4.7.2.2 Registers Available for the IrDA Function (UART3 Only)

Only the registers listed in Table 23-147 are used for the IrDA function.

Table 23-147. IrDA Mode Register Overview[1] [2]

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	UART_RHR	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER(IrDA)	UART_IER(IrDA)
0x008	UART_IIR	UART_FCR	UART_EFR[4]	UART_EFR[4]	UART_IIR(IrDA)	UART_FCR(IrDA)
0x00C	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]
0x010	–	–	UART_XON1_ADDR1	UART_XON1_ADDR1	–	–
0x014	UART_LSR(IrDA)	–	UART_XON2_ADDR2	UART_XON2_ADDR2	UART_LSR(IrDA)	–
0x018	UART_MSR/UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/UART_TCR	UART_TCR
0x01C	UART_TLR/UART_SPR	UART_TLR/UART_SPR	UART_TLR	UART_TLR	UART_TLR/UART_SPR	UART_TLR/UART_SPR
0x020	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1	UART_MDR1
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL	UART_SFLSR	UART_TXFLL
0x02C	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH	UART_RESUME	UART_TXFLH
0x030	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL	UART_SFREGL	UART_RXFLL
0x034	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH	UART_SFREGH	UART_RXFLH
0x038	–	–	–	–	UART_BLR	UART_BLR
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]
0x060	–	–	–	–	–	–

(1) REGISTER_NAME(UART) notation indicates that the register exists for other functions (IrDA or CIR), but fields have different meanings for other functions (described separately in Section 23.3.6, *UART/IrDA/CIR Register Manual*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the UART function.

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Table 23-147. IrDA Mode Register Overview[1] [2] (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

23.3.4.7.2.3 Registers Available for the CIR Function (UART3 Only)

Only the registers listed in Table 23-148 are used for the CIR function.

Table 23-148. CIR Mode Register Overview[1] [2]

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x000	UART_DLL	UART_DLL	UART_DLL	UART_DLL	–	UART_THR
0x004	UART_DLH	UART_DLH	UART_DLH	UART_DLH	UART_IER(CIR)	UART_IER(CIR)
0x008	UART_IIR	UART_FCR	UART_EFR	UART_EFR	UART_IIR(CIR)	UART_FCR(CIR)
0x00C	UART_LCR	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]	UART_LCR[7]
0x010	–	–	–	–	–	–
0x014	UART_LSR(IrDA)	–	–	–	UART_LSR(IrDA)	–
0x018	UART_MSR/UART_TCR	UART_TCR	UART_TCR	UART_TCR	UART_MSR/UART_TCR	UART_TCR
0x01C	UART_TLR/UART_SPR	UART_TLR/UART_SPR	UART_TLR	UART_TLR	UART_TLR/UART_SPR	UART_TLR/UART_SPR
0x020	UART_MDR1[3:0]	UART_MDR1[3:0]	UART_MDR1[3:0]	UART_MDR1[3:0]	UART_MDR1[3:0]	UART_MDR1[3:0]
0x024	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2	UART_MDR2
0x028	–	–	–	–	–	–
0x02C	UART_RESUME	–	UART_RESUME	–	UART_RESUME	–
0x030	–	–	–	–	–	–
0x034	–	–	–	–	–	–
0x038	–	–	–	–	–	–
0x03C	–	–	–	–	UART_ACREG	UART_ACREG
0x040	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR	UART_SCR
0x044	UART_SSR	–	UART_SSR	–	UART_SSR	–

(1) REGISTER_NAME(UART) notation indicates that the register exists for other functions (IrDA or CIR), but fields have different meanings for other functions (described separately in Section 23.3.6, *UART/IrDA/CIR Register Manual*).

(2) REGISTER_NAME[m:n] notation indicates that only register bits numbered m to n apply to the UART function.

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Table 23-148. CIR Mode Register Overview[1] [2] (continued)

Address Offset	Registers					
	Configuration Mode A		Configuration Mode B		Operational Mode	
	Read	Write	Read	Write	Read	Write
0x048	–	–	–	–	UART_EBLR	UART_EBLR
0x050	UART_MVR	–	UART_MVR	–	UART_MVR	–
0x054	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC	UART_SYSC
0x058	UART_SYSS	–	UART_SYSS	–	UART_SYSS	–
0x05C	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]	UART_WER[6:4]
0x060	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS	UART_CFPS
0x064	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL	UART_RXFIFO_LVL
0x068	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL	UART_TXFIFO_LVL
0x06C	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2	UART_IER2
0x070	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2	UART_ISR2
0x074	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL	UART_FREQ_SEL
0x080	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3	UART_MDR3
0x084	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD	UART_TX_DMA_THRESHOLD

23.3.4.8 Protocol Formatting

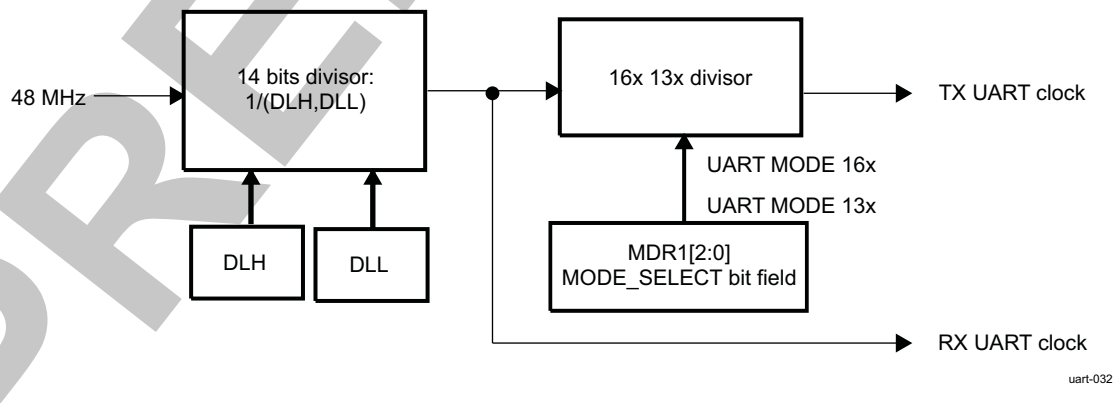
23.3.4.8.1 UART Mode

23.3.4.8.1.1 UART Clock Generation: Baud Rate Generation

The UART function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 23-72 shows the baud rate generator and associated controls.

Figure 23-72. Baud Rate Generation



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CAUTION

Before initializing or modifying clock parameter controls (UARTi.UART_DLH, UARTi.UART_DLL), MODE_SELECT = DISABLE (UARTi.UART_MDR1[2:0]) must be set to 0x7. Failure to observe this rule can result in unpredictable module behavior.

23.3.4.8.1.2 Choosing the Appropriate Divisor Value

Two divisor values are:

- UART 16x mode: Divisor value = Operating frequency / (16x baud rate)
- UART 13x mode: Divisor value = Operating frequency / (13x baud rate)

Table 23-149 describes the UART baud rate settings.

Table 23-149. UART Baud Rate Settings (48-MHz Clock)

Baud Rate	Baud Multiple	DLH, DLL (Decimal)	DLH, DLL (Hex)	Actual Baud Rate	Error (%)
0.3 kbps	16x	10000	0x27, 0x10	0.3 kbps	0
0.6 kbps	16x	5000	0x13, 0x88	0.6 kbps	0
1.2 kbps	16x	2500	0x09, 0xC4	1.2 kbps	0
2.4 kbps	16x	1250	0x04, 0xE2	2.4 kbps	0
4.8 kbps	16x	625	0x02, 0x71	4.8 kbps	0
9.6 kbps	16x	312	0x01, 0x38	9.6153 kbps	+0.16
14.4 kbps	16x	208	0x00, 0xD0	14.423 kbps	+0.16
19.2 kbps	16x	156	0x00, 0x9C	19.231 kbps	+0.16
28.8 kbps	16x	104	0x00, 0x68	28.846 kbps	+0.16
38.4 kbps	16x	78	0x00, 0x4E	38.462 kbps	+0.16
57.6 kbps	16x	52	0x00, 0x34	57.692 kbps	+0.16
115.2 kbps	16x	26	0x00, 0x1A	115.38 kbps	+0.16
230.4 kbps	16x	13	0x00, 0x0D	230.77 kbps	+0.16
460.8 kbps	13x	8	0x00, 0x08	461.54 kbps	+0.16
921.6 kbps	13x	4	0x00, 0x04	923.08 kbps	+0.16
1.843 Mbps	13x	2	0x00, 0x02	1.846 Mbps	+0.16
3.6884 Mbps	13x	1	0x00, 0x01	3.6923 Mbps	+0.16

23.3.4.8.1.3 UART Data Formatting

The UART can use hardware flow control to manage transmission and reception. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the RTS output and CTS input signals.

The UART is enhanced with the autobauding function. In control mode, autobauding lets the speed, the number of bits per character, and the parity selected be set automatically.

23.3.4.8.1.3.1 Frame Formatting

When autobauding is not used, frame format attributes must be defined in the UARTi.UART_LCR register.

Character length is specified using the UARTi.UART_LCR[1:0] CHAR_LENGTH bit field.

The number of stop-bits is specified using the UARTi.UART_LCR[2] NB_STOP bit.

The parity bit is programmed using the UARTi.UART_LCR[5:3] PARITY_EN, PARITY_TYPE_1, and PARITY_TYPE_2 bit fields (see Table 23-150).

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Table 23-150. UART Parity Bit Encoding

PARITY_EN	PARITY_TYPE_1	PARITY_TYPE_2	Parity
0	N/A	N/A	No parity
1	0	0	Odd parity
1	1	0	Even parity
1	0	1	Forced 1
1	1	1	Forced 0

23.3.4.8.1.3.2 Hardware Flow Control

Hardware flow control is composed of auto-CTS and auto-RTS. Auto-CTS and auto-RTS can be enabled and disabled independently by programming the UARTi.UART_EFR[7:6] AUTO_CTS_EN and AUTO_RTS_EN bit fields, respectively.

With auto-CTS, uarti_cts must be active before the module can transmit data.

Auto-RTS activates the uarti_rts output only when there is enough room in the RX FIFO to receive data. It deactivates the uarti_rts output when the RX FIFO is sufficiently full. The HALT and RESTORE trigger levels in the UARTi.UART_TCR register determine the levels at which uarti_rts is activated and deactivated.

If auto-CTS and auto-RTS are enabled, data transmission does not occur unless the RX FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If auto-CTS and auto-RTS are not enabled, overrun errors occur if the transmit data rate exceeds the RX FIFO latency.

- Auto-RTS:

  Auto-RTS data flow control originates in the receiver block. The RX FIFO trigger levels used in auto-RTS are stored in the UARTi.UART_TCR register. uarti_rts is active if the RX FIFO level is below the HALT trigger level in the UARTi.UART_TCR[3:0] RX_FIFO_TRIG_HALT bit field. When the RX FIFO HALT trigger level is reached, uarti_rts is deasserted. The sending device (for example, another UART) can send an additional byte after the trigger level is reached because it may not recognize the deassertion of RTS until it begins sending the additional byte.

  uarti_rts is automatically reasserted when the RX FIFO reaches the RESUME trigger level programmed by the UARTi.UART_TCR[7:4] RX_FIFO_TRIG_START bit field. This reassertion requests the sending device to resume transmission.

  In this case, uarti_rts is an active-low signal.

- Auto-CTS:

  The transmitter circuitry checks uarti_cts before sending the next data byte. When uarti_cts is active, the transmitter sends the next byte. To stop the transmitter from sending the next byte, uarti_cts must be deasserted before the middle of the last stop-bit currently sent.

  The auto-CTS function reduces interrupts to the host system. When auto-CTS flow control is enabled, the uarti_cts state changes do not have to trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTS, the transmitter sends any data present in the transmit FIFO, and a receiver overrun error can result.

  In this case, uarti_cts is an active-low signal.

23.3.4.8.1.3.3 Software Flow Control

Software flow control is enabled through the enhanced feature register (UARTi.UART_EFR) and the modem control register (UARTi.UART_MCR). Different combinations of software flow control can be enabled by setting different combinations of the UARTi.UART_EFR[3:0] bit field (see Table 23-151).

Two other enhanced features relate to software flow control:

- XON-any function (UARTi.UART_MCR[5]): Operation resumes after receiving any character after the XOFF character is recognized. If special character detect is enabled and special character is received after XOFF1, it does not resume transmission. The special character is stored in the RX FIFO.

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NOTE: The XON-any character is written into the RX FIFO even if it is a software flow character.

- Special character (UARTi.UART_EFR[5]): Incoming data is compared to XOFF2. When the special character is detected, the XOFF interrupt (UARTi.UART_IIR[4]) is set, but it does not halt transmission. The XOFF interrupt is cleared by a read of UARTi.UART_IIR. The special character is transferred to the RX FIFO. Special character does not work with XON2, XOFF2, or sequential XOFFs.

Table 23-151. UART_EFR[3:0] Software Flow Control Options

Bit 3	Bit 2	Bit 1	Bit 0	TX, RX Software Flow Controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit XON1, XOFF1
0	1	X	X	Transmit XON2, XOFF2
1	1	X	X	Transmit XON1, XON2: XOFF1, XOFF2(1)
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares XON1, XOFF1
X	X	0	1	Receiver compares XON2, XOFF2
X	X	1	1	Receiver compares XON1, XON2: XOFF1, XOFF2(1)

(1) In these cases, the XON1 and XON2 characters or the XOFF1 and XOFF2 characters must be transmitted/received sequentially with XON1/XOFF1 followed by XON2/XOFF2.
XON1 is defined in the UARTi.UART_XON1_ADDR1[7:0] XON_WORD1 bit field. XON2 is defined in the UARTi.UART_XON2_ADDR2[7:0] XON_WORD2 bit field.
XOFF1 is defined in the UARTi.UART_XOFF1[7:0] XOFF_WORD1 bit field. XOFF2 is defined in the UARTi.UART_XOFF2[7:0] XOFF_WORD2 bit field.

23.3.4.8.1.3.3.1 Receive (RX)

When software flow control operation is enabled, the UART compares incoming data with XOFF1/2 programmed characters (in certain cases, XOFF1 and XOFF2 must be received sequentially). When the correct XOFF characters are received, transmission stops after transmission of the current character completes. Detection of XOFF also sets the UARTi.UART_IIR[4] bit (if enabled by UARTi.UART_IER[5]) and causes the interrupt line to go low.

To resume transmission, an XON1/2 character must be received (in certain cases, XON1 and XON2 must be received sequentially). When the correct XON characters are received, the UARTi.UART_IIR[4] bit is cleared and the XOFF interrupt disappears.

NOTE: When a parity, framing, or break error occurs while receiving a software flow control character, this character is treated as normal data and is written to the RX FIFO.

When XON-any and special character detect are disabled and software flow control is enabled, no valid XON or XOFF characters are written to the RX FIFO. For example, when UARTi.UART_EFR[1:0] = 0x2, if XON1 and XOFF1 characters are received, they are not written to the RX FIFO.

When pairs of software flow characters are programmed to be received sequentially (UARTi.UART_EFR[1:0] = 0x3), the software flow characters are not written to the RX FIFO if they are received sequentially. However, received XON1/XOFF1 characters must be written to the RX FIFO if the subsequent character is not XON2/XOFF2.

23.3.4.8.1.3.3.2 Transmit (TX)

Two XOFF1 characters are transmitted when the RX FIFO passes the trigger level programmed by UARTi.UART_TCR[3:0]. As soon as the RX FIFO reaches the trigger level programmed by UARTi.UART_TCR[7:4], two XON1 characters are sent, so the data transfer recovers.

NOTE: If software flow control is disabled after an XOFF character is sent, the module transmits XON characters automatically to enable normal transmission.

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The transmission of XOFF(s)/XON(s) follows the same protocol as transmission of an ordinary byte from the TX FIFO. This means that even if the word length is 5, 6, or 7 characters, the 5, 6, or 7 LSBs of XOFF1/2 and XON1/2 are transmitted. The 5, 6, or 7 bits of a character are seldom transmitted, but this function is included to maintain compatibility with earlier designs.

It is assumed that software flow control and hardware flow control are never enabled simultaneously.

23.3.4.8.1.3.4 Autobauding Modes

In autobauding mode, the UART can extract transfer characteristics (speed, length, and parity) from an "at" (AT) command (ASCII code). These characteristics are used to receive data after an AT and to send data.

The following AT commands are valid:

AT	DATA	<CR>
at	DATA	<CR>
A/		
a/		

A line break during the acquisition of the sequence AT is not recognized, and an echo function is not implemented in hardware.

A/ and a/ are not used to extract characteristics, but they must be recognized because of their special meaning. A/ or a/ is used to instruct the software to repeat the last received AT command; therefore, an a/ always follows an AT, and transfer characteristics are not expected to change between an AT and an a/.

When a valid AT is received, AT and all subsequent data, including the final <CR> (0x0D), are saved to the RX FIFO. The autobaud state-machine waits for the next valid AT command. If an a/ (A/) is received, the a/ (A/) is saved in the RX FIFO and the state-machine waits for the next valid AT command.

On the first successful detection of the baud rate, the UART activates an interrupt to signify that the AT (upper or lower case) sequence is detected. The UARTi.UART_UASR register reflects the correct settings for the baud rate detected. Interrupt activity can continue in this fashion when a subsequent character is received. Therefore, it is recommended that the software enable the RHR interrupt when using the autobaud mode.

The following settings are detected in autobaud mode with a module clock of 48 MHz:

- Speed:
  - 115.2K baud
  - 57.6K baud
  - 38.4K baud
  - 28.8K baud
  - 19.2K baud
  - 14.4K baud
  - 9.6K baud
  - 4.8K baud
  - 2.4K baud
  - 1.2K baud
- Length: 7 or 8 bits
- Parity: Odd, even, or space

NOTE: The combination of 7-bit character plus space parity is not supported.

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Autobauding mode is selected when the UARTi.UART_MDR1[2:0] MODE_SELECT bit field is set to 0x2. In UART autobauding mode, UARTi.UART_DLL, UARTi.UART_DLH, and UARTi.UART_LCR[5:0] bit field settings are not used; instead, UART_UASR is updated with the configuration detected by the autobauding logic.

UART_UASR Autobauding Status Register Use

This register is used to set up transmission according to the characteristics of the previous reception instead of the UARTi.UART_LCR, UARTi.UART_DLL, and UARTi.UART_DLH registers when the UART is in autobauding mode.

To reset the autobauding hardware (to start a new AT detection) or to set the UART in standard mode (no autobaud), the UARTi.UART_MDR1[2:0] MODE_ SELECT bit field must be set to reset state (0x7) and then to the UART in autobauding mode (0x2) or to the UART in standard mode (0x0).

Use limitation:

- Only 7- and 8-bit characters (5- and 6-bit not supported)
- 7-bit character with space parity not supported
- Baud rate between 1200 and 115,200 bps (10 possibilities)

23.3.4.8.1.3.5 Error Detection

When the UARTi.UART_LSR register is read, the UARTi.UART_LSR[4:2] bit field reflects the error bits (BI: break condition, FE: framing error, PE: parity error) of the character at the top of the RX FIFO (the next character to be read). Therefore, reading the UARTi.UART_LSR register and then reading the UARTi.UART_RHR register identifies errors in a character.

Reading the UARTi.UART_RHR register updates the BI, FE, and PE bits (see Table 23-135 for the UART mode interrupts).

The UARTi.UART_LSR[7] RX_FIFO_STS bit is set when there is an error in the RX FIFO and is cleared only when no errors remain in the RX FIFO.

NOTE: Reading the UARTi.UART_LSR register does not cause an increment of the RX FIFO read pointer. The RX FIFO read pointer is incremented by reading the UARTi.UART_RHR register.

Reading the UARTi.UART_LSR register clears the OE bit if it is set (see Table 23-135 for the UART mode interrupts).

23.3.4.8.1.3.6 Overrun During Receive

Overrun during receive occurs if the RX state-machine tries to write data into the RX FIFO when it is already full. When overrun occurs, the device interrupts the MPU with the UARTi.UART_IIR[5:1] IT_TYPE bit field set to 0x3 (receiver line status error) and discards the remaining portion of the frame.

Overrun also causes an internal flag to be set, which disables further reception. Before the next frame can be received, the MPU must:

- Reset the RX FIFO.
- Read the UARTi.UART_RESUME register, which clears the internal flag.

23.3.4.8.1.3.7 Time-Out and Break Conditions

23.3.4.8.1.3.7.1 Time-Out Counter

An RX idle condition is detected when the receiver line (uarti_rx) is high for a time that equals 4x the programmed word length + 12 bits. uarti_rx is sampled midway through each bit.

For sleep mode, the counter is reset when there is activity on uarti_rx.

For the time-out interrupt, the counter counts only when there is data in the RX FIFO, and the count is reset when there is activity on uarti_rx or when the UARTi.UART_RHR register is read.

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23.3.4.8.1.3.7.2 Break Condition

When a break condition occurs, uarti_tx is pulled low. A break condition is activated by setting the UARTi.UART_LCR[6] BREAK_EN bit. The break condition is not aligned on word stream (a break condition can occur in the middle of a character). The only way to send a break condition on a full character is:

1. Reset the TX FIFO (if enabled).
2. Wait for the transmit shift register to empty (the UARTi.UART_LSR[6] TX_SR_E bit is set to 1).
3. Take a guard time according to stop-bit definition.
4. Set the BREAK_EN bit to 1.

The break condition is asserted while the BREAK_EN bit is set to 1.

The time-out counter and break condition apply only to UART modem operation and not to IrDA/CIR mode operation.

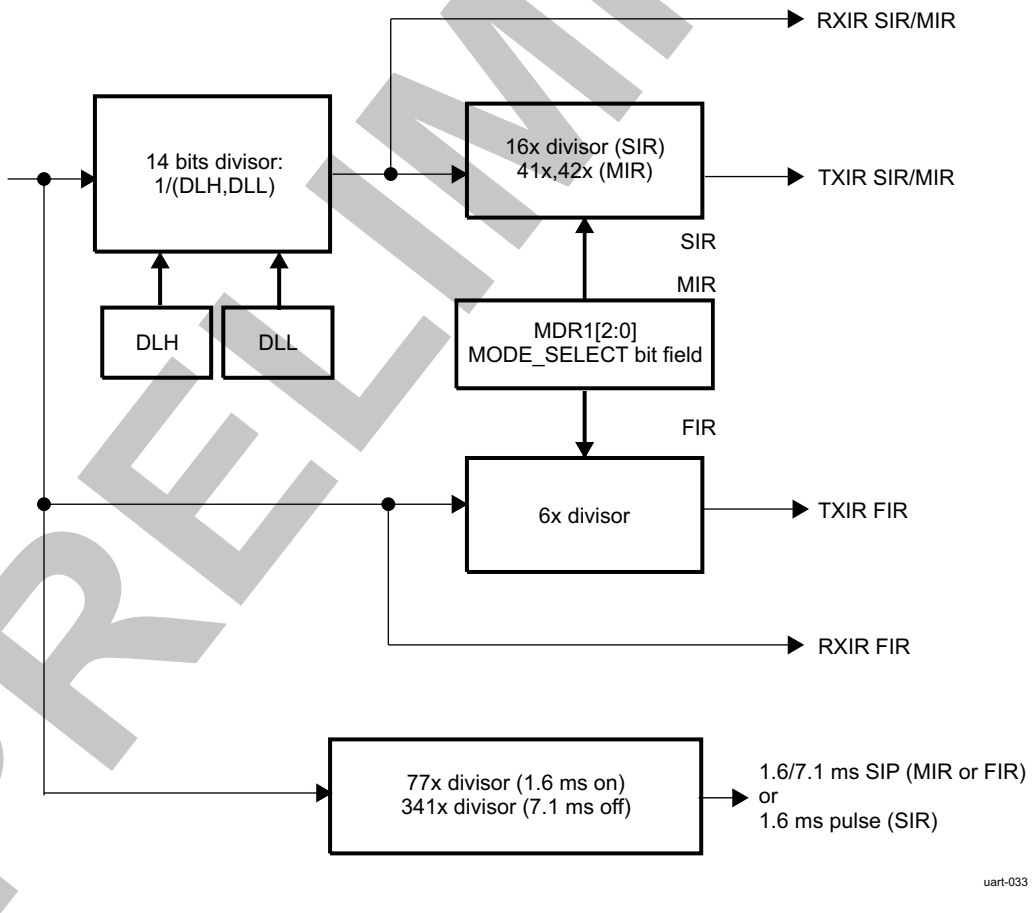
23.3.4.8.2 IrDA Mode (UART3 Only)

23.3.4.8.2.1 IrDA Clock Generation: Baud Generator

The IrDA function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate.

Figure 23-73 shows the baud rate generator and associated controls.

Figure 23-73. Baud Rate Generator



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CAUTION

Before initializing or modifying clock parameter controls (UARTi.UART_DLH, UARTi.UART_DLL), MODE_SELECT=DISABLE (UARTi.UART_MDR1[2:0]) must be set to 0x7). Failure to observe this rule can result in unpredictable module behavior.

23.3.4.8.2.2 Choosing the Appropriate Divisor Value

Three divisor values are:

- SIR mode: Divisor value = Operating frequency/(16x baud rate)
- MIR mode: Divisor value = Operating frequency/(41x/42x baud rate)
- FIR mode: Divisor value = None

Table 23-152 lists the IrDA baud rate settings.

Table 23-152. IrDA Baud Rate Settings

Baud Rate	IR Mode	Baud Multiple	Encoding	DLH, DLL (Decimal)	Actual Baud Rate	Error (%)	Source Jitter (%)	Pulse Duration
2.4 kbps	SIR	16x	3/16	1250	2.4 kbps	0	0	78.1 µs
9.6 kbps	SIR	16x	3/16	312	9.6153 kbps	+0.16	0	19.5 µs
19.2 kbps	SIR	16x	3/16	156	19.231 kbps	+0.16	0	9.75 µs
38.4 kbps	SIR	16x	3/16	78	38.462 kbps	+0.16	0	4.87 µs
57.6 kbps	SIR	16x	3/16	52	57.692 kbps	+0.16	0	3.25 µs
115.2 kbps	SIR	16x	3/16	26	115.38 kbps	+0.16	0	1.62 µs
0.576 Mbps	MIR	41x/42x	1/4	2	0.5756 Mbps(1)	0	+1.63/–0.80	416 ns
1.152 Mbps	MIR	41x/42x	1/4	1	1.1511 Mbps(1)	0	+1.63/–0.80	208 ns
4 Mbps	FIR	6x	4 PPM	–	4 Mbps	0	0	125 ns

(1) Average value

NOTE: Baud rate error and source jitter table values do not include 48-MHz reference clock error and jitter.

23.3.4.8.2.3 IrDA Data Formatting

The methods described in this section apply to all IrDA modes (SIR, MIR, and FIR).

23.3.4.8.2.3.1 IR RX Polarity Control

The UART3.UART_MDR2[6] IRRXINVERT bit provides the flexibility to invert the uart3_rx_irrx pin in the UART to ensure that the protocol at the output of the transceiver has the same polarity at module level. By default, the uart3_rx_irrx pin is inverted because most transceivers invert the IR receive pin.

23.3.4.8.2.3.2 IrDA Reception Control

The module can transmit and receive data, but when the device is transmitting, the IR RX circuitry is automatically disabled by hardware.

Operation of the uart3_rx_irrx input can be disabled by the UART3.UART_ACREG[5] DIS_IR_RX bit.

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23.3.4.8.2.3.3 IR Address Checking

In all IR modes, when address checking is enabled, only frames intended for the device are written to the RX FIFO. This restriction avoids receiving frames not meant for this device in a multipoint infrared environment. It is possible to program two frame addresses that the UART IrDA receives, with the UART3.UART_XON1_ADDR1[7:0] XON_WORD1 and UART3.UART_XON2_ADDR2[7:0] XON_WORD2 bit fields.

Setting the UART_EFR[0] bit to 1 selects address1 checking. Setting the UART_EFR[1] bit to 1 selects address2 checking. Setting the UART_EFR[1:0] bit field to 0 disables all address checking operations. If both bits are set, the incoming frame is checked for private and public addresses.

If address checking is disabled, all received frames write to the RX FIFO.

23.3.4.8.2.3.4 Frame Closing

A transmission frame can be terminated in two ways:

- Frame-length method: Set the UART3.UART_MDR1[7] FRAME_END_MODE bit to 0. The MPU writes the value of the frame length to the UART3.UART_TXFLH and UART3.UART_TXFLL registers. The device automatically attaches end flags to the frame when the number of bytes transmitted equals the value of the frame length.
- Set-EOT bit method: Set the FRAME_END_MODE bit to 1. The MPU writes 1 to the UART3.UART_ACREG[0] EOT bit just before it writes the last byte to the TX FIFO. When the MPU writes the last byte to the TX FIFO, the device internally sets the tag bit for that character in the TX FIFO. As the TX state-machine reads data from the TX FIFO, it uses this tag-bit information to attach end flags and correctly terminate the frame.

23.3.4.8.2.3.5 Store and Controlled Transmission

In store and controlled transmission (SCT) mode, the MPU starts writing data to the TX FIFO. Then, after writing a part of a frame (for a bigger frame) or an entire frame (a small frame; that is, a supervisory frame), the MPU writes 1 to the UART3.UART_ACREG[2] SCTX_EN bit (deferred TX start) to start transmission.

SCT mode is enabled by setting the UART3.UART_MDR1[5] SCT bit to 1. This transmission method differs from normal mode, in which data transmission starts immediately after data is written to the TX FIFO. SCT mode is useful for sending short frames without TX underrun.

23.3.4.8.2.3.6 Error Detection

When the UART3.UART_LSR register is read, the UART3.UART_LSR[4:2] bit field reflects the error bits [FL, CRC, ABORT] of the frame at the top of the STATUS FIFO (the next frame status to be read).

The error is triggered by an interrupt (for IrDA mode interrupts, see Table 23-136). The STATUS FIFO must be read until empty (a maximum of eight reads is required).

23.3.4.8.2.3.7 Underrun During Transmission

Underrun during transmission occurs when the TX FIFO is empty before the end of the frame is transmitted. When underrun occurs, the device closes the frame with end flags but attaches an incorrect CRC value. The receiving device detects a CRC error and discards the frame; it can then ask for a retransmission.

Underrun also causes an internal flag to be set, which disables additional transmissions. Before the next frame can be transmitted, the MPU must:

- Reset the TX FIFO.
- Read the UART3.UART_RESUME register, which clears the internal flag.

This function can be disabled by the UART3.UART_ACREG[4] DIS_TX_UNDERRUN bit, compensated by the extension of the stop-bit in transmission if the TX FIFO is empty.

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23.3.4.8.2.3.8 Overrun During Receive

Overrun during receive for the IrDA mode has the same function as that for the UART mode (see Section 23.3.4.8.1.3.6, *Overrun During Receive*).

23.3.4.8.2.3.9 Status FIFO

In IrDA modes, a status FIFO records the received frame status. When a complete frame is received, the length of the frame and the error bits associated with the frame are written to the status FIFO.

Reading the UART3.UART_SFREGH[3:0] MSB and UART3.UART_SFREGL[3:0] (LSB) bit fields obtains the frame length. The frame error status is read in the UART3.UART_SFLSR register. Reading the UART3.UART_SFLSR register increments the status FIFO read pointer. Because the status FIFO is eight entries deep, it can hold the status of eight frames.

The MPU uses the frame-length information to locate the frame boundary in the received frame data. The MPU can screen bad frames using the error status information and can later request the sender to resend only the bad frames.

This status FIFO can be used effectively in DMA mode because the MPU must be interrupted only when the programmed status FIFO trigger level is reached, not each time a frame is received.

23.3.4.8.2.4 SIR Mode Data Formatting

This section provides specific instructions for SIR mode programming.

23.3.4.8.2.4.1 Abort Sequence

The transmitter can prematurely close a frame (abort) by sending the sequence 0x7DC1. The abort pattern closes the frame without a CRC field or an ending flag.

A transmission frame can be aborted by setting the UART3.UART_ACREG[1] ABORT_EN bit to 1. When this bit is set to 1, 0x7D and 0xC1 are transmitted and the frame is not terminated with CRC or stop flags.

When a 0x7D character followed immediately by a 0xC1 character is received without transparency, the receiver treats a frame as an aborted frame.

CAUTION

When the TX FIFO is not empty and the UART3.UART_MDR1[5] SCT bit is set to 1, the UART IrDA starts a new transfer with data of a previous frame when the aborted frame is sent. Therefore, the TX FIFO must be reset before sending an aborted frame.

23.3.4.8.2.4.2 Pulse Shaping

SIR mode supports the 3/16 or the 1.6-µs pulse duration methods. The UART3.UART_ACREG[7] PULSE_TYPE bit selects the pulse width method in the transmit mode.

23.3.4.8.2.4.3 SIR Free Format Programming

The SIR FF mode is selected by setting the module in the UART mode (UART3.UART_MDR1[2:0] MODE_SELECT = 0x0) and the UART3.UART_MDR2[3] UART_PULSE bit to 1 to allow pulse shaping.

Because the bit format stays the same, some UART mode configuration registers must be set at specific values:

- UART3.UART_LCR[1:0] CHAR_LENGTH bit field = 0x3 (8 data bits)
- UART3.UART_LCR[2] NB_STOP bit = 0x0 (1 stop-bit)
- UART3.UART_LCR[3] PARITY_EN bit = 0x0 (no parity)

The UART mode interrupts are used for the SIR FF mode, but many are not relevant (XOFF, RTS, CTS, modem status register, etc.).

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23.3.4.8.2.5 MIR and FIR Mode Data Formatting

This section describes common instructions for FIR and MIR mode programming.

At the end of a frame reception, the MPU reads the line status register (UART3.UART_LSR) to detect errors in the received frame.

When the UART3.UART_MDR1[6] SIP_MODE bit is set to 1, the TX state-machine always sends one SIP at the end of a transmission frame. However, when the SIP_MODE bit is set to 0, SIP transmission depends on the UART3.UART_ACREG[3] SEND_SIP bit.

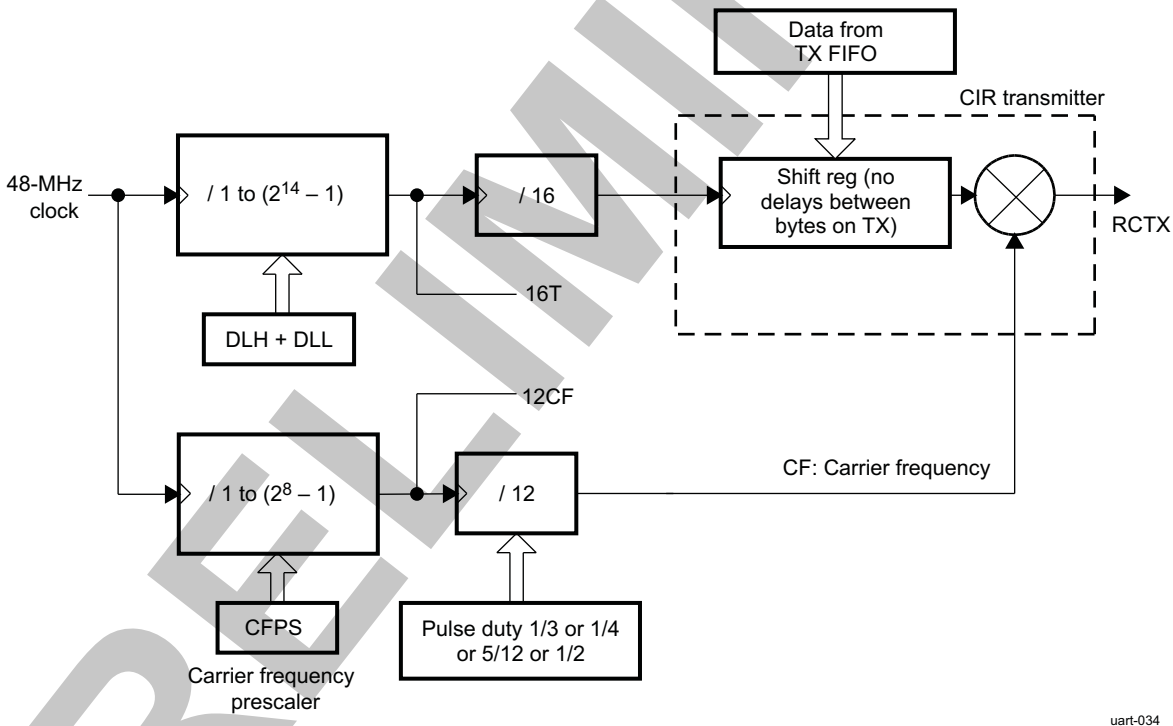
The MPU can set the SEND_SIP bit at least once every 500 ms. The advantage of this approach over the default approach is that the TX state-machine does not have to send the SIP at the end of each frame, thus reducing the overhead required.

23.3.4.8.3 CIR Mode (UART3 Only)

23.3.4.8.3.1 CIR Mode Clock Generation

Depending on the encoding method (variable pulse distance/biphase), the MPU must develop a data structure that combines 1 and 0 with a *t* period to encode the complete frame to transmit. This can then be transmitted to the infrared output with a modulation method, as shown in Figure 23-74.

Figure 23-74. CIR Mode Block Components



Based on the requested modulation frequency, the UART3.UART_CFPS register must be set with the correct dividing value to provide an accurate pulse frequency:

Dividing value = (FCLK / 12) / MODfreq

Where:

FCLK = System clock frequency (48 MHz)

12 = Real value of baud multiple

MODfreq = Effective frequency of the modulation (MHz)

Example: For a targeted modulation frequency of 36 kHz, the value of UART_CFPS must be set to 0x7 (decimal), which provides a modulation frequency of 36.04 kHz.

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NOTE: The UART3.UART_CFPS register starts with a reset value of 105 (decimal), which translates to a frequency of 38.1 kHz.

The duty cycle of these pulses is user-defined by the pulse duty register bits in the UART3.UART_MDR2 register. Table 23-153 shows the duty cycle.

Table 23-153. Duty Cycle

UART_MDR2[5:4]	Duty Cycle (High-Level)
00	1/4
01	1/3
10	5/12
11	1/2

23.3.4.8.3.2 CIR Data Formatting

The methods described in this section apply to all CIR modes.

23.3.4.8.3.2.1 IR RX Polarity Control

The IR RX polarity control for CIR mode has the same function as that for IrDA mode (see Section 23.3.4.8.2.3.1, *IR RX Polarity Control*).

23.3.4.8.3.2.2 CIR Transmission

In transmission, the MPU software must exercise an element of real-time control to transmit data packets, each of which must be emitted at a constant delay from the start-bits of each individual packet. Thus, when sending a series of packets, the packet-to-packet delay must respect a specific delay. Two methods can be used to control this delay:

- Filling the TX FIFO with a number of zero bits that are transmitted with a *t* period
- Using an external system timer to control the delay between each start-of-frame or between the end of a frame and the start of the next one. This can be performed by:
  - Controlling the start of the frame using the UART3.UART_MDR1[5] SCT bit and the UART3.UART_ACREG[2] SCTX_EN bit, depending on the timer status
  - Using the UART3.UART_IIR[5] TX_STATUS_IT interrupt bit to preload the next frame in the TX FIFO and to control the start of the timer (in case of control delay between the end of a frame and the start of the next frame)

23.3.5 UART/IrDA/CIR Basic Programming Model

23.3.5.1 UART Programming Model

23.3.5.1.1 Quick Start

This section describes the procedure for operating the UART with FIFO and DMA or interrupts. This three-part procedure ensures the quick start of the UART. It does not cover every UART feature.

The first programming model covers software reset of the UART. The second programming model describes FIFO and DMA configuration. The last programming model describes protocol, baud rate, and interrupt configuration.

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NOTE: Each programming model can be used independently of the other two; for instance, reconfiguring the FIFOs and DMA settings only.

Each programming model can be executed starting from any UART register access mode (register modes, submodes, and other register dependencies). However, if the UART register access mode is known before executing the programming model, some steps that enable or restore register access are optional. For more information, see Section 23.3.4.7.1, *Register Access Modes*.

23.3.5.1.1.1 Software Reset

To clear the UART registers, perform the following steps:

1. Initiate a software reset:
   Set the UARTi.UART_SYSC[1] SOFTRESET bit to 1.
2. Wait for the end of the reset operation:
   Poll the UARTi.UART_SYSS[0] RESETDONE bit until it equals 1.

23.3.5.1.1.2 FIFOs and DMA Settings

To enable and configure the receive and transmit FIFOs and program the DMA mode, perform the following steps:

1. Switch to register configuration mode B to access the UARTi.UART_EFR register:
   (a) Save the current UARTi.UART_LCR register value.
   (b) Set the UARTi.UART_LCR register value to 0x00BF.
2. Enable register submode TCR_TLR to access the UARTi.UART_TLR register (part 1 of 2):
   (a) Save the UARTi.UART_EFR[4] ENHANCED_EN value.
   (b) Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 1.
3. Switch to register configuration mode A to access the UARTi.UART_MCR register:
   Set the UARTi.UART_LCR register value to 0x0080.
4. Enable register submode TCR_TLR to access the UARTi.UART_TLR register (part 2 of 2):
   (a) Save the UARTi.UART_MCR[6] TCR_TLR value.
   (b) Set the UARTi.UART_MCR[6] TCR_TLR bit to 1.
5. Enable the FIFO; load the new FIFO triggers (part 1 of 3) and the new DMA mode (part 1 of 2):
   Set the following bits to the desired values:
   - UARTi.UART_FCR[7:6] RX_FIFO_TRIG
   - UARTi.UART_FCR[5:4] TX_FIFO_TRIG
   - UARTi.UART_FCR[3] DMA_MODE
   - UARTi.UART_FCR[0] FIFO_ENABLE (0: Disable the FIFO; 1: Enable the FIFO)

   NOTE: The UARTi.UART_FCR register is not readable.
6. Switch to register configuration mode B to access the UARTi.UART_EFR register:
   Set the UARTi.UART_LCR register value to 0x00BF.
7. Load the new FIFO triggers (part 2 of 3):
   Set the following bits to the desired values:
   - UARTi.UART_TLR[7:4] RX_FIFO_TRIG_DMA
   - UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA
8. Load the new FIFO triggers (part 3 of 3) and the new DMA mode (part 2 of 2):
   Set the following bits to the desired values:
   - UARTi.UART_SCR[7] RX_TRIG_GRANU1

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- UARTi.UART_SCR[6] TX_TRIG_GRANU1
- UARTi.UART_SCR[2:1] DMA_MODE_2
- UARTi.UART_SCR[0] DMA_MODE_CTL

9. Restore the UARTi.UART_EFR[4] ENHANCED_EN value saved in Step 2a.
10. Switch to register configuration mode A to access the UARTi.UART_MCR register:
    Set the UARTi.UART_LCR register value to 0x0080.
11. Restore the UARTi.UART_MCR[6] TCR_TLR value saved in Step 4a.
12. Restore the UARTi.UART_LCR value saved in Step 1a.

Triggers are used to generate interrupt and DMA requests. See Section 23.3.4.6.1.1, *Transmit FIFO Trigger,* to choose the following values:

- UARTi.UART_FCR[5:4] TX_FIFO_TRIG
- UARTi.UART_TLR[3:0] TX_FIFO_TRIG_DMA
- UARTi.UART_SCR[6] TX_TRIG_GRANU1

Triggers are used to generate interrupt and DMA requests. See Section 23.3.4.6.1.2, *Receive FIFO Trigger*, to choose the following values:

- UARTi.UART_FCR[7:6] RX_FIFO_TRIG
- UARTi.UART_TLR[7:4] RX_FIFO_TRIG_DMA
- UARTi.UART_SCR[7] RX_TRIG_GRANU1

DMA mode enables DMA requests. See Section 23.3.4.6.4, *FIFO DMA Mode Operation*, to choose the following values:

- UARTi.UART_FCR[3] DMA_MODE
- UARTi.UART_SCR[2:1] DMA_MODE_2
- UARTi.UART_SCR[0] DMA_MODE_CTL

23.3.5.1.1.3 Protocol, Baud Rate, and Interrupt Settings

To program the protocol, baud rate, and interrupt settings, perform the following steps:

1. Disable UART to access the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Switch to register configuration mode B to access the UARTi.UART_EFR register:
   Set the UARTi.UART_LCR register value to 0x00BF.
3. Enable access to the UARTi.UART_IER[7:4] bit field:
   (a) Save the UARTi.UART_EFR[4] ENHANCED_EN value.
   (b) Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 1.
4. Switch to register operational mode to access the UARTi.UART_IER register:
   Set the UARTi.UART_LCR register value to 0x0000.
5. Clear the UARTi.UART_IER register (set the UARTi.UART_IER[4] SLEEP_MODE bit to 0 to change the UARTi.UART_DLL and UARTi.UART_DLH registers). Set the UARTi.UART_IER register value to 0x0000.
6. Switch to register configuration mode B to access the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_LCR register value to 0x00BF.
7. Load the new divisor value:
   Set the UARTi.UART_DLL[7:0] CLOCK_LSB and UARTi.UART_DLH[5:0] CLOCK_MSB bit fields to the desired values.
8. Switch to register operational mode to access the UARTi.UART_IER register:
   Set the UARTi.UART_LCR register value to 0x0000.
9. Load the new interrupt configuration (0: Disable the interrupt; 1: Enable the interrupt):

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Set the following bits to the desired values:

- UARTi.UART_IER[7] CTS_IT
- UARTi.UART_IER[6] RTS_IT
- UARTi.UART_IER[5] XOFF_IT
- UARTi.UART_IER[4] SLEEP_MODE
- UARTi.UART_IER[3] MODEM_STS_IT
- UARTi.UART_IER[2] LINE_STS_IT
- UARTi.UART_IER[1] THR_IT
- UARTi.UART_IER[0] RHR_IT

10. Switch to register configuration mode B to access the UARTi.UART_EFR register:

    Set the UARTi.UART_LCR register value to 0x00BF.

11. Restore the UARTi.UART_EFR[4] ENHANCED_EN value saved in Step 3a.
12. Load the new protocol formatting (parity, stop-bit, character length) and switch to register operational mode:

    Set the UARTi.UART_LCR[7] DIV_EN bit to 0.

    Set the UARTi.UART_LCR[6] BREAK_EN bit to 0.

    Set the following bits to the desired values:

    - UARTi.UART_LCR[5] PARITY_TYPE_2
    - UARTi.UART_LCR[4] PARITY_TYPE_1
    - UARTi.UART_LCR[3] PARITY_EN
    - UARTi.UART_LCR[2] NB_STOP
    - UARTi.UART_LCR[1:0] CHAR_LENGTH

13. Load the new UART mode:

    Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to the desired value.

See Section 23.3.4.8.1.2, *Choosing the Appropriate Divisor Value*, to choose the following values:

- UARTi.UART_DLL[7:0] CLOCK_LSB
- UARTi.UART_DLH[5:0] CLOCK_MSB
- UARTi.UART_MDR1[2:0] MODE_SELECT

See Section 23.3.4.8.1.3.1, *Frame Formatting*, to choose the following values:

- UARTi.UART_LCR[5] PARITY_TYPE_2
- UARTi.UART_LCR[4] PARITY_TYPE_1
- UARTi.UART_LCR[3] PARITY_EN
- UARTi.UART_LCR[2] NB_STOP
- UARTi.UART_LCR[1:0] CHAR_LENGTH

23.3.5.1.2 Hardware and Software Flow Control Configuration

This section describes the programming steps to enable and configure hardware and software flow control. Hardware and software flow control cannot be used at the same time.

NOTE: Each programming model can be executed starting from any UART register access mode (register modes, submodes, and other register dependencies). However, if the UART register access mode is known before executing the programming model, some steps that enable or restore register access are optional. For more information, see Section 23.3.4.7.1, *Register Access Modes*.

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23.3.5.1.2.1 Hardware Flow Control Configuration

To enable and configure hardware flow control, perform the following steps:

1. Switch to register configuration mode A to access the UARTi.UART_MCR register:
   (a) Save the current UARTi.UART_LCR register value.
   (b) Set the UARTi.UART_LCR register value to 0x0080.
2. Enable register submode TCR_TLR to access the UARTi.UART_TCR register (part 1 of 2):
   (a) Save the UARTi.UART_MCR[6] TCR_TLR value.
   (b) Set the UARTi.UART_MCR[6] TCR_TLR bit to 1.
3. Switch to register configuration mode B to access the UARTi.UART_EFR register:
   Set the UARTi.UART_LCR register value to 0x00BF.
4. Enable register submode TCR_TLR to access the UARTi.UART_TCR register (part 2 of 2):
   (a) Save the UARTi.UART_EFR[4] ENHANCED_EN value.
   (b) Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 1.
5. Load the new start and halt trigger values for hardware flow control:
   Set the following bits to the desired values:
   - UARTi.UART_TCR[7:4] AUTO_RTS_START
   - UARTi.UART_TCR[3:0] AUTO_RTS_HALT
6. Enable or disable receive and transmit hardware flow control mode and restore the UARTi.UART_EFR[4] ENHANCED_EN value saved in Step 4a.
   Set the following bits to the desired values:
   - UARTi.UART_EFR[7] AUTO_CTS_EN (0: Disable; 1: Enable)
   - UARTi.UART_EFR[6] AUTO_RTS_EN (0: Disable; 1: Enable)

   Restore the UARTi.UART_EFR[4] ENHANCED_EN bit to the saved value.
7. Switch to register configuration mode A to access the UARTi.UART_MCR register:
   Set the UARTi.UART_LCR register value to 0x0080.
8. Restore the UARTi.UART_MCR[6] TCR_TLR value saved in Step 2a.
9. Restore the UARTi.UART_LCR value saved in Step 1a.

See Section 23.3.4.8.1.3.2, *Hardware Flow Control*, to choose the following values:

- UARTi.UART_EFR[7] AUTO_CTS_EN
- UARTi.UART_EFR[6] AUTO_RTS_EN
- UARTi.UART_TCR[7:4] AUTO_RTS_START
- UARTi.UART_TCR[3:0] AUTO_RTS_HALT

23.3.5.1.2.2 Software Flow Control Configuration

To enable and configure software flow control, perform the following steps:

1. Switch to register configuration mode B to access the UARTi.UART_EFR register.
   (a) Save the current UARTi.UART_LCR register value.
   (b) Set the UARTi.UART_LCR register value to 0x00BF.
2. Enable register submode XOFF to access the UARTi.UART_XOFF1 and UARTi.UART_XOFF2 registers:
   (a) Save the UARTi.UART_EFR[4] ENHANCED_EN value.
   (b) Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 0.
3. Load the new software flow control characters:
   Set the following bits to the desired values:
   - UARTi.UART_XON1_ADDR1[7:0] XON_WORD1
   - UARTi.UART_XON2_ADDR2[7:0] XON_WORD2

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- UARTi.UART_XOFF1[7:0] XOFF_WORD1
- UARTi.UART_XOFF2[7:0] XOFF_WORD2

4. Enable access to the UARTi.UART_MCR[7:5] bit field and enable register submode TCR_TLR to access the UARTi.UART_TCR register (part 1 of 2):

   Set the UARTi.UART_EFR[4] ENHANCED_EN bit to 1.
5. Switch to register configuration mode A to access the UARTi.UART_MCR register:

   Set the UARTi.UART_LCR register value to 0x0080.
6. Enable register submode TCR_TLR to access the UARTi.UART_TCR register (part 2 of 2) and enable or disable XON any function:

   (a) Save the UARTi.UART_MCR[6] TCR_TLR value.

   (b) Set the UARTi.UART_MCR[6] TCR_TLR bit to 1.

   (c) Set the UARTi.UART_MCR[5] XON_EN bit to the desired value (0: Disable; 1: Enable).
7. Switch to register configuration mode B to access the UARTi.UART_EFR register:

   Set the UARTi.UART_LCR register value to 0x00BF.
8. Load the new start and halt trigger values for software flow control:

   Set the following bits to the desired values:
   - UARTi.UART_TCR[7:4] AUTO_RTS_START
   - UARTi.UART_TCR[3:0] AUTO_RTS_HALT
9. Enable or disable special character function and load the new software flow control mode and restore the UARTi.UART_EFR[4] ENHANCED_EN value saved in Step 2a:

   Set the following bits to the desired values:
   - UARTi.UART_EFR[5] SPEC_CHAR (0: Disable; 1: Enable)
   - UARTi.UART_EFR[3:0] SW_FLOW_CONTROL

   Restore the UARTi.UART_EFR[4] ENHANCED_EN bit to the saved value.
10. Switch to register configuration mode A to access the UARTi.UART_MCR register:

    Set the UARTi.UART_LCR register value to 0x0080.
11. Restore the UARTi.UART_MCR[6] TCR_TLR bit value saved in Step 6a.
12. Restore the UARTi.UART_LCR value saved in Step 1a.

See Section 23.3.4.8.1.3.3, *Software Flow Control*, to choose the following values:

- UARTi.UART_EFR[5] SPEC_CHAR
- UARTi.UART_EFR[3:0] SW_FLOW_CONTROL
- UARTi.UART_TCR[7:4] AUTO_RTS_START
- UARTi.UART_TCR[3:0] AUTO_RTS_HALT
- UARTi.UART_XON1_ADDR1[7:0] XON_WORD1
- UARTi.UART_XON2_ADDR2[7:0] XON_WORD2
- UARTi.UART_XOFF1[7:0] XOFF_WORD1
- UARTi.UART_XOFF2[7:0] XOFF_WORD2

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23.3.5.2 IrDA Programming Model (UART3 Only)

23.3.5.2.1 SIR Mode

23.3.5.2.1.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with parity forced to 1, baud rate = 112.5 kbps, FIFOs disabled, 2 stop-bits, and 8-bit word length:

1. Disable the UART before accessing the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_DLL and UART_DLH registers (the UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
3. Load the new baud rate (115.2 kbps):
   UART3.UART_DLL = 0x1A
   UART3.UART_DLH = 0x00
4. Set SIR mode:
   UART3.UART_MDR1[2:0] MODE_SELECT = 0x1
5. Disable access to the UART_DLL and UART_DLH registers and switch to register operational mode:
   UART3.UART_LCR = 0x00
6. Optional: Enable the RHR interrupt:
   UART3.UART_IER[0] RHR_IT = 0x1

23.3.5.2.1.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 6-byte frame with no parity, baud rate = 112.5 kbps, FIFOs disabled, 3/16 encoding, 2 stop-bits, and 7-bit word length:

1. Disable the UART before accessing the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_EFR register:
   UART3.UART_LCR = 0xBF
3. Enable the enhanced features (the UART_EFR[4] ENAHNCED_EN bit = 1):
   Set the UART3.UART_EFR register value to 0x10.
4. Grant access to the UART_DLL and UART_DLH registers (the UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
5. Load the new baud rate (115.2 kbps):
   UART3.UART_DLL = 0x1A
   UART3.UART_DLH = 0x00
6. Set SIR mode (the UART_MDR1[2:0] MODE_SELECT bit field = 0x1):
   UART3.UART_MDR1 = 0x01
7. Disable access to the UART_DLL and UART_DLH registers and switch to register operational mode:
   UART3.UART_LCR = 0x00
8. Force DTR output to active:
   UART3.UART_MCR[0] DTR = 1
9. Optional: Enable the THR interrupt:
   UART3.UART_IER[1] THR_IT = 1
10. Set transmit frame length to 6 bytes:
    UART3.UART_TXFLL = 0x06

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11. Set 7 starts of frame transmission:
    UART3.UART_EBLR = 0x08
12. Optional: Set SIR pulse width to be 1.6 µs:
    UART3.UART_ACREG[7] PULSE_TYPE = 1
13. Load the UART_THR register with the data to be transmitted.

23.3.5.2.2 MIR Mode

23.3.5.2.2.1 Receive

The following programming model explains how to program the module to receive an IrDA frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled.

1. Disable the UART before accessing the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_DLL and UART_DLH registers (UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
3. Load the new baud rate (1.152 Mpbs):
   UART3.UART_DLL = 0x01
   UART3.UART_DLH = 0x00
4. Set MIR mode:
   UART3.UART_MDR1[2:0] MODE_SELECT = 0x4
5. Disable access to the UART_DLL and UART_DLH registers and switch to register operational mode:
   UART3.UART_LCR = 0x00
6. Force DTR output to active (UART_MCR[0] DTR = 1):
   Force RTS output to active (UART_MCR[1] RTS = 1).
   UART3.UART_MCR = 0x3
7. Optional: Enable the RHR interrupt:
   UART3.UART_IER[0] RHR_IT = 1

23.3.5.2.2.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 60-byte frame with no parity, baud rate = 1.152 Mpbs, and FIFOs disabled:

1. Disable the UART before accessing the UARTi.UART_DLL and UARTi.UART_DLH registers:
   Set the UARTi.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_DLL and UART_DLH registers (UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
3. Load the new baud rate (1.152 Mpbs):
   UART3.UART_DLL = 0x01
   UART3.UART_DLH = 0x00
4. Set MIR mode:
   UART3.UART_MDR1[2:0] MODE_SELECT = 0x4
5. Disable access to the UART_DLL and UART_DLH registers and switch to register operational mode:
   UART3.UART_LCR = 0x00
6. Force DTR output to active:
   UART3.UART_MCR[0] DTR = 1
7. Optional: Enable the THR interrupt:

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UART3.UART_IER[1] THR_IT = 1

8. Set the frame length to 60 bytes:
   UART3.UART_TXFLL = 0x3C
9. Optional: Transmit eight additional starts of frame (MIR mode requires two starts):
   UART3.UART_EBLR = 0x08
10. SIP is sent at the end of transmission:
    UART3.UART_ACREG[3] = 1
11. Load the UART_THR register with the data to be transmitted.

23.3.5.2.3 FIR Mode

23.3.5.2.3.1 Receive

The following programming model explains how to program the module to receive the IrDA frame with no parity, baud rate = 4 Mbps, FIFOs enabled, 8-bit word length.

1. Disable the UART before accessing the UART3.UART_DLL and UART3.UART_DLH registers:
   Set the UART3.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to the UART_DLL and UART_DLH registers (UART_LCR[7] DIV_EN bit = 1):
   UART3.UART_LCR = 0x80 (Data format is unaffected by the use and settings of the UART3.UART_LCR register in IrDA mode.)
3. FIFO clear and enable:
   UART3.UART_FCR = 0x7 (TX/RX FIFO trigger: UART_FCR[7:6] and UART_FCR[5:4])
   UART3.UART_LCR[7] = 0
4. Set FIR mode:
   UART3.UART_MDR1[2:0] MODE_SELECT = 0x5
5. Set frame length:
   UART3.UART_RXFLL = 0xA (Data + CRC + STOP)
6. Disable access to the UART3.UART_DLL registers and UART3.UART_DLH and switch to register operational mode:
   UART3.UART_LCR[7] DIV_EN = 0x0
7. Optional: Enable the RHR interrupt:
   UART3.UART_IER[0] RHR_IT = 1

23.3.5.2.3.2 Transmit

The following programming model explains how to program the module to transmit an IrDA 4-byte frame with no parity, baud rate = 4 Mbps, FIFOs enabled, and 8-bit word length.

1. Disable the UART before accessing the UART3.UART_DLL and UART3.UART_DLH registers:
   Set the UART3.UART_MDR1[2:0] MODE_SELECT bit field to 0x7.
2. Grant access to EFR_REG:
   UART3.UART_LCR = 0xBF
3. Enable the enhanced features (EFR_REG[4] ENAHNCED_EN = 0x1):
   UART3.UART_EFR = 0x10
4. FIFO clear and enable:
   UART3.UART_FCR = 0x7 (TX/RX FIFO trigger: UART_FCR[7:6] and UART_FCR[5:4]).
   UART3.UART_LCR[7] = 0
5. Set FIR mode and enable auto-SIP mode:
   UART3.UART_MDR1 = 0x45
6. Set frame length:

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UART3.UART_TXFLL = 0x4
UART3.UART_TXFLH = 0x0
UART3.UART_RXFLL = 0xA (Data + CRC + STOP)
UART3.UART_RXFLH = 0x0

7. Force DTR output to active:
   UART3.UART_MCR[0] DTR = 0x1
8. Optional: Enable the THR interrupt:
   UART3.UART_IER[1] THR_IT = 0x1
9. Optional: Transmit eight additional starts of frame (MIR mode requires two starts):
   UART3.UART_EBLR = 0x08
10. SIP is sent at the end of transmission:
    UART3.UART_ACREG[3] = 1
11. Load the UART_THR register with the data to be transmitted.

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23.3.6 UART/IrDA/CIR Register Manual

23.3.6.1 UART/IrDA/CIR Instance Summary

Table 23-154 shows the base address and address space for the UART/IrDA/CIR module instances.

Table 23-154. UART/IrDA/CIR Instance Summary

Module Name	Base Address	Size
UART1[(1)]	0x4806 A000	4 KiB
UART2[(1)]	0x4806 C000	4 KiB
UART3[(2)]	0x4802 0000	4 KiB
UART4[(1)]	0x4806 E000	4 KiB
UART5[(1)]	0x4806 6000	4 KiB
UART6[(1)]	0x4806 8000	4 KiB

(1) UART mode only
(2) UART, IrDA, or CIR mode

23.3.6.2 UART/IrDA/CIR Registers

23.3.6.2.1 UART/IrDA/CIR Register Summary

Table 23-155. UART/IrDA/CIR Register Mapping Summary (UART1 and UART2)

Register Name	Type	Register Width (Bits)	Address Offset	UART1 Base Address	UART2 Base Address
UART_THR	W	32	0x0000 0000	0x4806 A000	0x4806 C000
UART_RHR	R	32	0x0000 0000	0x4806 A000	0x4806 C000
UART_DLL	RW	32	0x0000 0000	0x4806 A000	0x4806 C000
UART_IER	RW	32	0x0000 0004	0x4806 A004	0x4806 C004
UART_IER_IRDA	RW	32	0x0000 0004	0x4806 A004	0x4806 C004
UART_IER_CIR	RW	32	0x0000 0004	0x4806 A004	0x4806 C004
UART_DLH	RW	32	0x0000 0004	0x4806 A004	0x4806 C004
UART_IIR	R	32	0x0000 0008	0x4806 A008	0x4806 C008
UART_IIR_IRDA	R	32	0x0000 0008	0x4806 A008	0x4806 C008
UART_IIR_CIR	R	32	0x0000 0008	0x4806 A008	0x4806 C008
UART_FCR	W	32	0x0000 0008	0x4806 A008	0x4806 C008
UART_EFR	RW	32	0x0000 0008	0x4806 A008	0x4806 C008
UART_LCR	RW	32	0x0000 000C	0x4806 A00C	0x4806 C00C
UART_XON1_ADDR1	RW	32	0x0000 0010	0x4806 A010	0x4806 C010
UART_MCR	RW	32	0x0000 0010	0x4806 A010	0x4806 C010
UART_LSR	R	32	0x0000 0014	0x4806 A014	0x4806 C014
UART_LSR_IRDA	R	32	0x0000 0014	0x4806 A014	0x4806 C014
UART_LSR_CIR	R	32	0x0000 0014	0x4806 A014	0x4806 C014
UART_XON2_ADDR2	RW	32	0x0000 0014	0x4806 A014	0x4806 C014
UART_TCR	RW	32	0x0000 0018	0x4806 A018	0x4806 C018
UART_XOFF1	RW	32	0x0000 0018	0x4806 A018	0x4806 C018
UART_MSR	R	32	0x0000 0018	0x4806 A018	0x4806 C018
UART_SPR	RW	32	0x0000 001C	0x4806 A01C	0x4806 C01C
UART_TLR	RW	32	0x0000 001C	0x4806 A01C	0x4806 C01C
UART_XOFF2	RW	32	0x0000 001C	0x4806 A01C	0x4806 C01C
UART_MDR1	RW	32	0x0000 0020	0x4806 A020	0x4806 C020
UART_MDR2	RW	32	0x0000 0024	0x4806 A024	0x4806 C024

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Table 23-155. UART/IrDA/CIR Register Mapping Summary (UART1 and UART2) (continued)

Register Name	Type	Register Width (Bits)	Address Offset	UART1 Base Address	UART2 Base Address
UART_SFLSR	R	32	0x0000 0028	0x4806 A028	0x4806 C028
UART_TXFLL	W	32	0x0000 0028	0x4806 A028	0x4806 C028
UART_RESUME	R	32	0x0000 002C	0x4806 A02C	0x4806 C02C
UART_TXFLH	W	32	0x0000 002C	0x4806 A02C	0x4806 C02C
UART_SFREGL	R	32	0x0000 0030	0x4806 A030	0x4806 C030
UART_RXFLL	W	32	0x0000 0030	0x4806 A030	0x4806 C030
UART_SFREGH	R	32	0x0000 0034	0x4806 A034	0x4806 C034
UART_RXFLH	W	32	0x0000 0034	0x4806 A034	0x4806 C034
UART_BLR	RW	32	0x0000 0038	0x4806 A038	0x4806 C038
UART_UASR	R	32	0x0000 0038	0x4806 A038	0x4806 C038
UART_ACREG	RW	32	0x0000 003C	0x4806 A03C	0x4806 C03C
UART_SCR	RW	32	0x0000 0040	0x4806 A040	0x4806 C040
UART_SSR	R	32	0x0000 0044	0x4806 A044	0x4806 C044
UART_EBLR	RW	32	0x0000 0048	0x4806 A048	0x4806 C048
UART_MVR	R	32	0x0000 0050	0x4806 A050	0x4806 C050
UART_SYSC	RW	32	0x0000 0054	0x4806 A054	0x4806 C054
UART_SYSS	R	32	0x0000 0058	0x4806 A058	0x4806 C058
UART_WER	RW	32	0x0000 005C	0x4806 A05C	0x4806 C05C
UART_CFPS	RW	32	0x0000 0060	0x4806 A060	0x4806 C060
UART_RXFIFO_LVL	R	32	0x0000 0064	0x4806 A064	0x4806 C064
UART_TXFIFO_LVL	R	32	0x0000 0068	0x4806 A068	0x4806 C068
UART_IER2	RW	32	0x0000 006C	0x4806 A06C	0x4806 C06C
UART_ISR2	RW	32	0x0000 0070	0x4806 A070	0x4806 C070
UART_FREQ_SEL	RW	32	0x0000 0074	0x4806 A074	0x4806 C074
RESERVED	RW	32	0x0000 0078	0x4806 A078	0x4806 C078
RESERVED	RW	32	0x0000 007C	0x4806 A07C	0x4806 C07C
UART_MDR3	RW	32	0x0000 0080	0x4806 A080	0x4806 C080
UART_TX_DMA_THRESHOLD	RW	32	0x0000 0084	0x4806 A084	0x4806 C084

Table 23-156. UART/IrDA/CIR Register Mapping Summary (UART3 and UART4)

Register Name	Type	Register Width (Bits)	Address Offset	UART3 Base Address	UART4 Base Address
UART_THR	W	32	0x0000 0000	0x4802 0000	0x4806 E000
UART_RHR	R	32	0x0000 0000	0x4802 0000	0x4806 E000
UART_DLL	RW	32	0x0000 0000	0x4802 0000	0x4806 E000
UART_IER	RW	32	0x0000 0004	0x4802 0004	0x4806 E004
UART_IER_IRDA	RW	32	0x0000 0004	0x4802 0004	0x4806 E004
UART_IER_CIR	RW	32	0x0000 0004	0x4802 0004	0x4806 E004
UART_DLH	RW	32	0x0000 0004	0x4802 0004	0x4806 E004
UART_IIR	R	32	0x0000 0008	0x4802 0008	0x4806 E008
UART_IIR_IRDA	R	32	0x0000 0008	0x4802 0008	0x4806 E008
UART_IIR_CIR	R	32	0x0000 0008	0x4802 0008	0x4806 E008
UART_FCR	W	32	0x0000 0008	0x4802 0008	0x4806 E008
UART_EFR	RW	32	0x0000 0008	0x4802 0008	0x4806 E008
UART_LCR	RW	32	0x0000 000C	0x4802 000C	0x4806 E00C
UART_XON1_ADDR1	RW	32	0x0000 0010	0x4802 0010	0x4806 E010

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Table 23-156. UART/IrDA/CIR Register Mapping Summary (UART3 and UART4) (continued)

Register Name	Type	Register Width (Bits)	Address Offset	UART3 Base Address	UART4 Base Address
UART_MCR	RW	32	0x0000 0010	0x4802 0010	0x4806 E010
UART_LSR	R	32	0x0000 0014	0x4802 0014	0x4806 E014
UART_LSR_IRDA	R	32	0x0000 0014	0x4802 0014	0x4806 E014
UART_LSR_CIR	R	32	0x0000 0014	0x4802 0014	0x4806 E014
UART_XON2_ADDR2	RW	32	0x0000 0014	0x4802 0014	0x4806 E014
UART_TCR	RW	32	0x0000 0018	0x4802 0018	0x4806 E018
UART_XOFF1	RW	32	0x0000 0018	0x4802 0018	0x4806 E018
UART_MSR	R	32	0x0000 0018	0x4802 0018	0x4806 E018
UART_SPR	RW	32	0x0000 001C	0x4802 001C	0x4806 E01C
UART_TLR	RW	32	0x0000 001C	0x4802 001C	0x4806 E01C
UART_XOFF2	RW	32	0x0000 001C	0x4802 001C	0x4806 E01C
UART_MDR1	RW	32	0x0000 0020	0x4802 0020	0x4806 E020
UART_MDR2	RW	32	0x0000 0024	0x4802 0024	0x4806 E024
UART_SFLSR	R	32	0x0000 0028	0x4802 0028	0x4806 E028
UART_TXFLL	W	32	0x0000 0028	0x4802 0028	0x4806 E028
UART_RESUME	R	32	0x0000 002C	0x4802 002C	0x4806 E02C
UART_TXFLH	W	32	0x0000 002C	0x4802 002C	0x4806 E02C
UART_SFREGL	R	32	0x0000 0030	0x4802 0030	0x4806 E030
UART_RXFLL	W	32	0x0000 0030	0x4802 0030	0x4806 E030
UART_SFREGH	R	32	0x0000 0034	0x4802 0034	0x4806 E034
UART_RXFLH	W	32	0x0000 0034	0x4802 0034	0x4806 E034
UART_BLR	RW	32	0x0000 0038	0x4802 0038	0x4806 E038
UART_UASR	R	32	0x0000 0038	0x4802 0038	0x4806 E038
UART_ACREG	RW	32	0x0000 003C	0x4802 003C	0x4806 E03C
UART_SCR	RW	32	0x0000 0040	0x4802 0040	0x4806 E040
UART_SSR	R	32	0x0000 0044	0x4802 0044	0x4806 E044
UART_EBLR	RW	32	0x0000 0048	0x4802 0048	0x4806 E048
UART_MVR	R	32	0x0000 0050	0x4802 0050	0x4806 E050
UART_SYSC	RW	32	0x0000 0054	0x4802 0054	0x4806 E054
UART_SYSS	R	32	0x0000 0058	0x4802 0058	0x4806 E058
UART_WER	RW	32	0x0000 005C	0x4802 005C	0x4806 E05C
UART_CFPS	RW	32	0x0000 0060	0x4802 0060	0x4806 E060
UART_RXFIFO_LVL	R	32	0x0000 0064	0x4802 0064	0x4806 E064
UART_TXFIFO_LVL	R	32	0x0000 0068	0x4802 0068	0x4806 E068
UART_IER2	RW	32	0x0000 006C	0x4802 006C	0x4806 E06C
UART_ISR2	RW	32	0x0000 0070	0x4802 0070	0x4806 E070
UART_FREQ_SEL	RW	32	0x0000 0074	0x4802 0074	0x4806 E074
RESERVED	RW	32	0x0000 0078	0x4802 0078	0x4806 E078
RESERVED	RW	32	0x0000 007C	0x4802 007C	0x4806 E07C
UART_MDR3	RW	32	0x0000 0080	0x4802 0080	0x4806 E080
UART_TX_DMA_THRESHOLD	RW	32	0x0000 0084	0x4802 0084	0x4806 E084

Table 23-157. UART/IrDA/CIR Register Mapping Summary (UART5 and UART6)

Register Name	Type	Register Width (Bits)	Address Offset	UART5 Base Address	UART6 Base Address
UART_THR	W	32	0x0000 0000	0x4806 6000	0x4806 8000

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Table 23-157. UART/IrDA/CIR Register Mapping Summary (UART5 and UART6) (continued)

Register Name	Type	Register Width (Bits)	Address Offset	UART5 Base Address	UART6 Base Address
UART_RHR	R	32	0x0000 0000	0x4806 6000	0x4806 8000
UART_DLL	RW	32	0x0000 0000	0x4806 6000	0x4806 8000
UART_IER	RW	32	0x0000 0004	0x4806 6004	0x4806 8004
UART_IER_IRDA	RW	32	0x0000 0004	0x4806 6004	0x4806 8004
UART_IER_CIR	RW	32	0x0000 0004	0x4806 6004	0x4806 8004
UART_DLH	RW	32	0x0000 0004	0x4806 6004	0x4806 8004
UART_IIR	R	32	0x0000 0008	0x4806 6008	0x4806 8004
UART_IIR_IRDA	R	32	0x0000 0008	0x4806 6008	0x4806 8004
UART_IIR_CIR	R	32	0x0000 0008	0x4806 6008	0x4806 8004
UART_FCR	W	32	0x0000 0008	0x4806 6008	0x4806 8008
UART_EFR	RW	32	0x0000 0008	0x4806 6008	0x4806 8008
UART_LCR	RW	32	0x0000 000C	0x4806 600C	0x4806 800C
UART_XON1_ADDR1	RW	32	0x0000 0010	0x4806 6010	0x4806 8010
UART_MCR	RW	32	0x0000 0010	0x4806 6010	0x4806 8010
UART_LSR	R	32	0x0000 0014	0x4806 6014	0x4806 8014
UART_LSR_IRDA	R	32	0x0000 0014	0x4806 6014	0x4806 8014
UART_LSR_CIR	R	32	0x0000 0014	0x4806 6014	0x4806 8014
UART_XON2_ADDR2	RW	32	0x0000 0014	0x4806 6014	0x4806 8014
UART_TCR	RW	32	0x0000 0018	0x4806 6018	0x4806 8018
UART_XOFF1	RW	32	0x0000 0018	0x4806 6018	0x4806 8018
UART_MSR	R	32	0x0000 0018	0x4806 6018	0x4806 8018
UART_SPR	RW	32	0x0000 001C	0x4806 601C	0x4806 801C
UART_TLR	RW	32	0x0000 001C	0x4806 601C	0x4806 801C
UART_XOFF2	RW	32	0x0000 001C	0x4806 601C	0x4806 801C
UART_MDR1	RW	32	0x0000 0020	0x4806 6020	0x4806 8020
UART_MDR2	RW	32	0x0000 0024	0x4806 6024	0x4806 8024
UART_SFLSR	R	32	0x0000 0028	0x4806 6028	0x4806 8028
UART_TXFLL	W	32	0x0000 0028	0x4806 6028	0x4806 8028
UART_RESUME	R	32	0x0000 002C	0x4806 602C	0x4806 802C
UART_TXFLH	W	32	0x0000 002C	0x4806 602C	0x4806 802C
UART_SFREGL	R	32	0x0000 0030	0x4806 6030	0x4806 8030
UART_RXFLL	W	32	0x0000 0030	0x4806 6030	0x4806 8030
UART_SFREGH	R	32	0x0000 0034	0x4806 6034	0x4806 8034
UART_RXFLH	W	32	0x0000 0034	0x4806 6034	0x4806 8034
UART_BLR	RW	32	0x0000 0038	0x4806 6038	0x4806 8038
UART_UASR	R	32	0x0000 0038	0x4806 6038	0x4806 8038
UART_ACREG	RW	32	0x0000 003C	0x4806 603C	0x4806 803C
UART_SCR	RW	32	0x0000 0040	0x4806 6040	0x4806 8040
UART_SSR	R	32	0x0000 0044	0x4806 6044	0x4806 8044
UART_EBLR	RW	32	0x0000 0048	0x4806 6048	0x4806 8048
UART_MVR	R	32	0x0000 0050	0x4806 6050	0x4806 8050
UART_SYSC	RW	32	0x0000 0054	0x4806 6054	0x4806 8054
UART_SYSS	R	32	0x0000 0058	0x4806 6058	0x4806 8058
UART_WER	RW	32	0x0000 005C	0x4806 605C	0x4806 805C
UART_CFPS	RW	32	0x0000 0060	0x4806 6060	0x4806 8060
UART_RXFIFO_LVL	R	32	0x0000 0064	0x4806 6064	0x4806 8064
UART_TXFIFO_LVL	R	32	0x0000 0068	0x4806 6068	0x4806 8068

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Table 23-157. UART/IrDA/CIR Register Mapping Summary (UART5 and UART6) (continued)

Register Name	Type	Register Width (Bits)	Address Offset	UART5 Base Address	UART6 Base Address
UART_IER2	RW	32	0x0000 006C	0x4806 606C	0x4806 806C
UART_ISR2	RW	32	0x0000 0070	0x4806 6070	0x4806 8070
UART_FREQ_SEL	RW	32	0x0000 0074	0x4806 6074	0x4806 8074
RESERVED	RW	32	0x0000 0078	0x4806 6078	0x4806 8078
RESERVED	RW	32	0x0000 007C	0x4806 607C	0x4806 807C
UART_MDR3	RW	32	0x0000 0080	0x4806 6080	0x4806 8080
UART_TX_DMA_THRESHOLD	RW	32	0x0000 0084	0x4806 6084	0x4806 8084

23.3.6.2.2 UART/IrDA/CIR Register Description

Table 23-158. UART_THR

Address Offset	0x0000 0000		
Physical Address	0x4806 A000	**Instance**	UART1
	0x4806 C000		UART2
	0x4802 0000		UART3
	0x4806 E000		UART4
	0x4806 6000		UART5
	0x4806 8000		UART6
Description	The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The THR is a 64-byte FIFO. The local host (LH) writes data to the THR. The data is placed in the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled, location 0 of the FIFO stores the data.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								THR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:0	THR	Transmit holding register	W	0x-

Table 23-159. Register Call Summary for Register UART_THR

UART/IrDA/CIR

- UART Interrupts: [0] [1]
- IrDA Interrupts: [2] [3] [4]
- CIR Interrupts: [5] [6]
- FIFO Management: [7]
- DMA Transmission: [8] [9]
- Registers Available for the Register Access Modes: [10]
- Registers Available for the UART Function: [11]
- Registers Available for the IrDA Function (UART3 Only): [12]
- Registers Available for the CIR Function (UART3 Only): [13]
- Transmit: [14]
- Transmit: [15]
- Transmit: [16]
- UART/IrDA/CIR Register Summary: [17] [18] [19]

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Table 23-160. UART_RHR

Address Offset	0x0000 0000		
Physical Address	0x4806 A000 0x4806 C000 0x4802 0000 0x4806 E000 0x4806 6000 0x4806 8000	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled, location 0 of the FIFO stores the single data character. **Note:** If an overflow occurs, the data in the RHR is not overwritten.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RHR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0	R	0x000000
7:0	RHR	Receive holding register	R	0x-

Table 23-161. Register Call Summary for Register UART_RHR

UART/IrDA/CIR

- UART Interrupts: [0] [1] [2]
- IrDA Interrupts: [3] [4] [5]
- FIFO Management: [6] [7]
- Registers Available for the Register Access Modes: [8]
- Registers Available for the UART Function: [9]
- Registers Available for the IrDA Function (UART3 Only): [10]
- UART Data Formatting: [11] [12] [13] [14]
- UART/IrDA/CIR Register Summary: [15] [16] [17]

Table 23-162. UART_DLL

Address Offset	0x0000 0000		
Physical Address	0x4806 A000 0x4806 C000 0x4802 0000 0x4806 E000 0x4806 6000 0x4806 8000	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	This register, with UART_DLH, stores the 14-bit divisor for generation of the baud clock in the baud rate generator. DLH stores the most-significant part of the divisor. DLL stores the least-significant part of the divisor.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CLOCK_LSB							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	CLOCK_LSB	Stores the 8-bit LSB divisor value	RW	0x00

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Table 23-163. Register Call Summary for Register UART_DLL

UART/IrDA/CIR

- Module Power Saving: [0] [1]
- DMA Transfers (DMA Mode 1, 2, or 3): [2] [3]
- Registers Available for the Register Access Modes: [4] [5] [6] [7]
- Registers Available for the UART Function: [8] [9] [10] [11]
- Registers Available for the IrDA Function (UART3 Only): [12] [13] [14] [15]
- Registers Available for the CIR Function (UART3 Only): [16] [17] [18] [19]
- UART Clock Generation: Baud Rate Generation: [20]
- UART Data Formatting: [21] [22]
- IrDA Clock Generation: Baud Generator: [23]
- Protocol, Baud Rate, and Interrupt Settings: [24] [25] [26] [27] [28]
- Receive: [29] [30] [31] [32]
- Transmit: [33] [34] [35] [36]
- Receive: [37] [38] [39] [40]
- Transmit: [41] [42] [43] [44]
- Receive: [45] [46] [47]
- Transmit: [48]
- UART/IrDA/CIR Register Summary: [49] [50] [51]
- UART/IrDA/CIR Register Description: [52] [53]

Table 23-164. UART_IER

Address Offset	0x0000 0004		
Physical Address	0x4806 A004	**Instance**	UART1
	0x4806 C004		UART2
	0x4802 0004		UART3
	0x4806 E004		UART4
	0x4806 6004		UART5
	0x4806 8004		UART6
Description	Interrupt enable register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_IT	LINE_STS_IT	THR_IT	RHR_IT

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	CTS_IT	0x0: Disables the CTS* interrupt 0x1: Enables the CTS* interrupt	RW	0
6	RTS_IT	0x0: Disables the RTS* interrupt 0x1: Enables the RTS* interrupt	RW	0
5	XOFF_IT	0x0: Disables the XOFF interrupt 0x1: Enables the XOFF interrupt	RW	0
4	SLEEP_MODE	0x0: Disables sleep mode 0x1: Enables sleep mode (stop baud rate clock when the module is inactive)	RW	0
3	MODEM_STS_IT	0x0: Disables the modem status register interrupt 0x1: Enables the modem status register interrupt	RW	0

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Bits	Field Name	Description	Type	Reset
2	LINE_STS_IT	0x0: Disables the receiver line status interrupt 0x1: Enables the receiver line status interrupt	RW	0
1	THR_IT	0x0: Disables the THR interrupt 0x1: Enables the THR interrupt	RW	0
0	RHR_IT	0x0: Disables the RHR interrupt and time-out interrupt 0x1: Enables the RHR interrupt and time-out interrupt	RW	0

Table 23-165. Register Call Summary for Register UART_IER

UART/IrDA/CIR

- Module Power Saving: [0] [1]
- IrDA Interrupts: [2] [3]
- CIR Interrupts: [4] [5]
- FIFO Interrupt Mode: [6]
- FIFO Polled Mode Operation: [7]
- Registers Available for the Register Access Modes: [8] [9]
- Registers Available for the UART Function: [10] [11]
- Registers Available for the IrDA Function (UART3 Only): [12] [13]
- Registers Available for the CIR Function (UART3 Only): [14] [15]
- UART Data Formatting: [16]
- Protocol, Baud Rate, and Interrupt Settings: [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]
- Receive: [31]
- Transmit: [32]
- Receive: [33]
- Transmit: [34]
- Receive: [35]
- Transmit: [36]
- UART/IrDA/CIR Register Summary: [37] [38] [39]

Table 23-166. UART_IER_IRDA

Address Offset	0x0000 0004		
Physical Address	0x4806 A004	**Instance**	UART1
	0x4806 C004		UART2
	0x4802 0004		UART3
	0x4806 E004		UART4
	0x4806 6004		UART5
	0x4806 8004		UART6
Description	There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually. Note: The TX_STATUS_IT interrupt reflects two possible conditions. The MDR2[0] should be read to determine the status in the event of this interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRIG_IT	RX_OVERRUN_IT	LAST_RX_BYTE_IT	THR_IT	RHR_IT

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	EOF_IT	0x0: Disables the received EOF interrupt 0x1: Enables the received EOF interrupt	RW	0
6	LINE_STS_IT	0x0: Disables the receiver line status interrupt 0x1: Enables the receiver line status interrupt	RW	0
5	TX_STATUS_IT	0x0: Disables the TX status interrupt 0x1: Enables the TX status interrupt	RW	0
4	STS_FIFO_TRIG_IT	0x0: Disables status FIFO trigger level interrupt 0x1: Enables status FIFO trigger level interrupt	RW	0
3	RX_OVERRUN_IT	0x0: Disables the RX overrun interrupt 0x1: Enables the RX overrun interrupt	RW	0
2	LAST_RX_BYTE_IT	0x0: Disables the last byte of frame in RX FIFO interrupt 0x1: Enables the last byte of frame in RX FIFO interrupt	RW	0
1	THR_IT	0x0: Disables the THR interrupt 0x1: Enables the THR interrupt	RW	0
0	RHR_IT	0x0: Disables the RHR interrupt and time-out interrupt 0x1: Enables the RHR interrupt and time-out interrupt	RW	0

Table 23-167. Register Call Summary for Register UART_IER_IRDA

UART/IrDA/CIR
- UART/IrDA/CIR Register Summary: [0] [1] [2]

Table 23-168. UART_IER_CIR

Address Offset	0x0000 0004		
Physical Address	0x4806 A004	**Instance**	UART1
	0x4806 C004		UART2
	0x4802 0004		UART3
	0x4806 E004		UART4
	0x4806 6004		UART5
	0x4806 8004		UART6
Description	There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually. Notes: The RX_STOP_IT interrupt is generated based on the value set in the BOF Length register (EBLR). In IR-CIR mode, contrary to the IR-IRDA mode, the TX_STATUS_IT has only one meaning corresponding to the case MDR2[0] = 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED		TX_STATUS_IT	RESERVED	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:6	RESERVED	Not used in CIR mode	RW	0x0
5	TX_STATUS_IT	0x0: Disables the TX status interrupt 0x1: Enables the TX status interrupt	RW	0
4	RESERVED	Not used in CIR mode	RW	0
3	RX_OVERRUN_IT	0x0: Disables the RX overrun interrupt 0x1: Enables the RX overrun interrupt	RW	0
2	RX_STOP_IT	0x0: Disables the receive stop interrupt 0x1: Enables the receive stop interrupt	RW	0
1	THR_IT	0x0: Disables the THR interrupt 0x1: Enables the THR interrupt	RW	0
0	RHR_IT	0x0: Disables the RHR interrupt 0x1: Enables the RHR interrupt	RW	0

Table 23-169. Register Call Summary for Register UART_IER_CIR

UART/IrDA/CIR

- UART/IrDA/CIR Register Summary: [0] [1] [2]

Table 23-170. UART_DLH

Address Offset	0x0000 0004		
Physical Address	0x4806 A004	**Instance**	UART1
	0x4806 C004		UART2
	0x4802 0004		UART3
	0x4806 E004		UART4
	0x4806 6004		UART5
	0x4806 8004		UART6
Description	This register, with UART_DLL, stores the 14-bit divisor for generating the baud clock in the baud rate generator. DLH stores the most-significant part of the divisor. DLL stores the least-significant part of the divisor.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED						CLOCK_MSB	

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:6	RESERVED	Read returns 0. Write has no effect.	RW	0x0
5:0	CLOCK_MSB	Stores the 6-bit MSB divisor value	RW	0x00

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Table 23-171. Register Call Summary for Register UART_DLH

UART/IrDA/CIR

- Module Power Saving: [0] [1]
- DMA Transfers (DMA Mode 1, 2, or 3): [2] [3]
- Registers Available for the Register Access Modes: [4] [5] [6] [7]
- Registers Available for the UART Function: [8] [9] [10] [11]
- Registers Available for the IrDA Function (UART3 Only): [12] [13] [14] [15]
- Registers Available for the CIR Function (UART3 Only): [16] [17] [18] [19]
- UART Clock Generation: Baud Rate Generation: [20]
- UART Data Formatting: [21] [22]
- IrDA Clock Generation: Baud Generator: [23]
- Protocol, Baud Rate, and Interrupt Settings: [24] [25] [26] [27] [28]
- Receive: [29] [30] [31] [32]
- Transmit: [33] [34] [35] [36]
- Receive: [37] [38] [39] [40]
- Transmit: [41] [42] [43] [44]
- Receive: [45] [46] [47]
- Transmit: [48]
- UART/IrDA/CIR Register Summary: [49] [50] [51]
- UART/IrDA/CIR Register Description: [52] [53]

Table 23-172. UART_IIR

Address Offset	0x0000 0008		
Physical Address	0x4806 A008	**Instance**	UART1
	0x4806 C008		UART2
	0x4802 0008		UART3
	0x4806 E008		UART4
	0x4806 6008		UART5
	0x4806 8004		UART6
Description	Interrupt identification register.		
	The IIR is a read-only register that provides the source of the interrupt in a prioritized manner.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FCR_MIRROR		IT_TYPE					IT_PENDING

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	R	0x000000
7:6	FCR_MIRROR	Mirror the contents of UART_FCR[0] on both bits.	R	0x0
5:1	IT_TYPE	Read 0x0: Modem interrupt. Priority = 4	R	0x00
		Read 0x1: THR interrupt. Priority = 3		
		Read 0x2: RHR interrupt. Priority = 2		
		Read 0x3: Receiver line status error. Priority = 3		
		Read 0x6: Rx time-out. Priority = 2		
		Read 0x8: XOFF/special character. Priority = 5		
		Read 0x10: CTS, RTS, DSR change state from active (low) to inactive (high) Priority = 6		
0	IT_PENDING	Read 0x0: An interrupt is pending.	R	1
		Read 0x1: No interrupt is pending.		

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Table 23-173. Register Call Summary for Register UART_IIR

UART/IrDA/CIR

- Block Diagram: [0]
- UART Interrupts: [1] [2] [3] [4] [5] [6] [7]
- Wake-Up Interrupt: [8]
- IrDA Interrupts: [9] [10] [11] [12] [13]
- CIR Interrupts: [14] [15] [16] [17] [18]
- Registers Available for the Register Access Modes: [19] [20]
- Registers Available for the UART Function: [21] [22]
- Registers Available for the IrDA Function (UART3 Only): [23] [24]
- Registers Available for the CIR Function (UART3 Only): [25] [26]
- UART Data Formatting: [27] [28] [29] [30] [31]
- CIR Data Formatting: [32]
- UART/IrDA/CIR Register Summary: [33] [34] [35]
- UART/IrDA/CIR Register Description: [36] [37] [38] [39] [40] [41] [42] [43]

Table 23-174. UART_IIR_IRDA

Address Offset	0x0000 0008		
Physical Address	0x4806 A008	**Instance**	UART1
	0x4806 C008		UART2
	0x4802 0008		UART3
	0x4806 E008		UART4
	0x4806 6008		UART5
	0x4806 8004		UART6
Description	The interrupt line is activated whenever one of the 8 interrupts is active.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAST_BYTE_IT	THR_IT	RHR_IT

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	R	0x000000
7	EOF_IT	Read 0x0: Receive EOF interrupt inactive Read 0x1: Received EOF interrupt active	R	0
6	LINE_STS_IT	Read 0x0: Receiver line status interrupt inactive Read 0x1: Receiver line status interrupt active	R	0
5	TX_STATUS_IT	Read 0x0: TX status interrupt inactive Read 0x1: TX status interrupt active	R	0
4	STS_FIFO_IT	Read 0x0: Status FIFO trigger level interrupt inactive Read 0x1: Status FIFO trigger level interrupt active	R	0
3	RX_OE_IT	Read 0x0: RX overrun interrupt inactive Read 0x1: RX overrun interrupt active	R	0

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Bits	Field Name	Description	Type	Reset
2	RX_FIFO_LAST_BYTE_IT	Read 0x0: Last byte of frame in RX FIFO interrupt inactive Read 0x1: Last byte of frame in RX FIFO interrupt active	R	0
1	THR_IT	Read 0x0: THR interrupt inactive Read 0x1: THR interrupt active	R	0
0	RHR_IT	Read 0x0: RHR interrupt inactive Read 0x1: RHR interrupt active	R	1

Table 23-175. Register Call Summary for Register UART_IIR_IRDA

UART/IrDA/CIR
- UART/IrDA/CIR Register Summary: [0] [1] [2]

Table 23-176. UART_IIR_CIR

Address Offset	0x0000 0008		
Physical Address	0x4806 A008 0x4806 C008 0x4802 0008 0x4806 E008 0x4806 6008 0x4806 8004	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	The interrupt line is activated whenever one of the 6 interrupts is active.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED		TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	R	0x000000
7:6	RESERVED	Not used in CIR mode	R	0x0
5	TX_STATUS_IT	Read 0x0: TX status interrupt inactive Read 0x1: TX status interrupt active	R	0
4	RESERVED	Not used in CIR mode	R	0
3	RX_OE_IT	Read 0x0: RX overrun interrupt inactive Read 0x1: RX overrun interrupt active	R	0
2	RX_STOP_IT	Read 0x0: Receive stop interrupt inactive Read 0x1: Receive stop interrupt active	R	0
1	THR_IT	Read 0x0: THR interrupt inactive Read 0x1: THR interrupt active	R	0
0	RHR_IT	Read 0x0: RHR interrupt inactive Read 0x1: RHR interrupt active	R	0

Table 23-177. Register Call Summary for Register UART_IIR_CIR

UART/IrDA/CIR
- UART/IrDA/CIR Register Summary: [0] [1] [2]

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Table 23-178. UART_FCR

Address Offset	0x0000 0008		
Physical Address	0x4806 A008 0x4806 C008 0x4802 0008 0x4806 E008 0x4806 6008 0x4806 8008	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	FIFO control register **Notes:** Bits 4 and 5 can only be written to when UART_EFR[4] = 1. Bits 0 and 3 can be changed only when the baud clock is not running (DLL and DLH set to 0). See Table 23-138 for UART_FCR[5:4] setting restriction when UART_SCR[6] = 1. See Table 23-139 for UART_FCR[7:6] setting restriction when UART_SCR[7] = 1.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLEAR	RX_FIFO_CLEAR	FIFO_EN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:6	RX_FIFO_TRIG	Sets the trigger level for the RX FIFO: If UART_SCR[7] = 0 and UART_TLR[7:4] = 0000: 00: 8 characters 01: 16 characters 10: 56 characters 11: 60 characters If UART_SCR[7] = 0 and UART_TLR[7:4] != 0000, RX_FIFO_TRIG is not considered. If UART_SCR[7] = 1, RX_FIFO_TRIG is 2 LSBs of the trigger level (1-63 on 6 bits) with the granularity 1.	W	0x0
5:4	TX_FIFO_TRIG	Sets the trigger level for the TX FIFO: If UART_SCR[6] = 0 and UART_TLR[3:0] = 0000: 00: 8 spaces 01: 16 spaces 10: 32 spaces 11: 56 spaces If UART_SCR[6] = 0 and UART_TLR[3:0] != 0000, TX_FIFO_TRIG is not considered. If UART_SCR[6] = 1, TX_FIFO_TRIG is 2 LSBs of the trigger level (1-63 on 6 bits) with the granularity 1	W	0x0
3	DMA_MODE	This register is considered if UART_SCR[0] = 0. Write 0x0: DMA_MODE 0 (No DMA) Write 0x1: DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)	W	0
2	TX_FIFO_CLEAR	Write 0x0: No change Write 0x1: Clears the TX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO.	W	0
1	RX_FIFO_CLEAR	Write 0x0: No change Write 0x1: Clears the RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO.	W	0
0	FIFO_EN	Write 0x0: Disables the transmit and RX FIFOs. The transmit and receive holding registers are 1-byte FIFOs. Write 0x1: Enables the transmit and RX FIFOs. The transmit and receive holding registers are 64-byte FIFOs.	W	0

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Table 23-179. Register Call Summary for Register UART_FCR

UART/IrDA/CIR

- FIFO Management: [0] [1] [2]
- Transmit FIFO Trigger: [3]
- Receive FIFO Trigger: [4] [5]
- FIFO Interrupt Mode: [6] [7] [8]
- FIFO Polled Mode Operation: [9]
- FIFO DMA Mode Operation: [10] [11] [12]
- DMA Transfers (DMA Mode 1, 2, or 3): [13]
- Registers Available for the Register Access Modes: [14] [15]
- Registers Available for the UART Function: [16] [17]
- Registers Available for the IrDA Function (UART3 Only): [18] [19]
- Registers Available for the CIR Function (UART3 Only): [20] [21]
- FIFOs and DMA Settings: [22] [23] [24] [25] [26] [27] [28] [29]
- Receive: [30] [31] [32]
- Transmit: [33] [34] [35]
- UART/IrDA/CIR Register Summary: [36] [37] [38]
- UART/IrDA/CIR Register Description: [39] [40] [41] [42] [43] [44] [45] [46]

Table 23-180. UART_EFR

Address Offset	0x0000 0008		
Physical Address	0x4806 A008	**Instance**	UART1
	0x4806 C008		UART2
	0x4802 0008		UART3
	0x4806 E008		UART4
	0x4806 6008		UART5
	0x4806 8008		UART6
Description	Enhanced feature register This register enables or disables enhanced features. Most of the enhanced functions apply only to UART modes, but UART_EFR[4] enables write accesses to UART_FCR[5:4], the TX trigger level, which is also used in IrDA modes.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHAR_DETECT	ENHANCED_EN	SW_FLOW_CONTROL			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	AUTO_CTS_EN	Auto-CTS enable bit 0x0: Normal operation 0x1: Auto-CTS flow control is enabled. Transmission is halted when the CTS* pin is high (inactive).	RW	0

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Bits	Field Name	Description	Type	Reset
6	AUTO_RTS_EN	Auto-RTS enable bit 0x0: Normal operation 0x1: Auto-RTS flow control is enabled. RTS* pin goes high (inactive) when the RX FIFO HALT trigger level, UART_TCR[3:0], is reached, and goes low (active) when the RX FIFO RESTORE transmission trigger level is reached.	RW	0
5	SPECIAL_CHAR_DETECT	0x0: Normal operation 0x1: Special character detect enable. Received data is compared with XOFF2 data. If a match occurs, the received data is transferred to the RX FIFO and the UART_IIR[4] bit is set to 1 to indicate that a special character was detected.	RW	0
4	ENHANCED_EN	Enhanced functions write enable bit 0x0: Disables writing to IER bits 4-7, UART_FCR bits 4-5, and MCR bits 5-7. 0x1: Enables writing to IER bits 4-7, UART_FCR bits 4-5, and MCR bits 5-7.	RW	0
3:0	SW_FLOW_CONTROL	Combinations of software flow control can be selected by programming bit 3 - bit 0. See Table 23-151.	RW	0x0

Table 23-181. Register Call Summary for Register UART_EFR

UART/IrDA/CIR

- SIR Mode: [0] [1] [2]
- Module Power Saving: [3]
- Register Access Submode: [4] [5] [6] [7] [8] [9]
- Registers Available for the Register Access Modes: [10] [11]
- Registers Available for the UART Function: [12] [13]
- Registers Available for the IrDA Function (UART3 Only): [14] [15]
- Registers Available for the CIR Function (UART3 Only): [16] [17]
- UART Data Formatting: [18] [19] [20] [21] [22] [23]
- IrDA Data Formatting: [24] [25] [26]
- FIFOs and DMA Settings: [27] [28] [29] [30] [31]
- Protocol, Baud Rate, and Interrupt Settings: [32] [33] [34] [35] [36]
- Hardware Flow Control Configuration: [37] [38] [39] [40] [41] [42] [43] [44] [45]
- Software Flow Control Configuration: [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56]
- Transmit: [57] [58] [59]
- Transmit: [60]
- UART/IrDA/CIR Register Summary: [61] [62] [63]
- UART/IrDA/CIR Register Description: [64] [65]

Table 23-182. UART_LCR

Address Offset	0x0000 000C		
Physical Address	0x4806 A00C	**Instance**	UART1
	0x4806 C00C		UART2
	0x4802 000C		UART3
	0x4806 E00C		UART4
	0x4806 600C		UART5
	0x4806 800C		UART6
Description	Line control register		
	LCR[6:0] define transmission and reception parameters. **Note:** When LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DIV_EN	BREAK_EN	PARITY_TYPE2	PARITY_TYPE1	PARITY_EN	NB_STOP	CHAR_LENGTH	

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	DIV_EN	0x0: Normal operating condition 0x1: Divisor latch enable. Allows access to DLL, DLH, and other registers (see Table 23-155 and Table 23-156).	RW	0
6	BREAK_EN	Break control bit 0x0: Normal operating condition 0x1: Forces the transmitter output to go low to alert the communication terminal	RW	0
5	PARITY_TYPE2	Selects the forced parity format (if UART_LCR[3] = 1). If UART_LCR[5] = 1 and UART_LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If UART_LCR[5] = 1 and UART_LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data.	RW	0
4	PARITY_TYPE1	0x0: Odd parity is generated (if UART_LCR[3] = 1). 0x1: Even parity is generated (if UART_LCR[3] = 1).	RW	0
3	PARITY_EN	0x0: No parity 0x1: A parity bit is generated during transmission and the receiver checks for received parity.	RW	0
2	NB_STOP	Specifies the number of stop-bits 0x0: 1 stop-bit (word length = 5, 6, 7, 8) 0x1: 1.5 stop-bits (word length = 5) 2 stop-bits (word length = 6, 7, 8)	RW	0
1:0	CHAR_LENGTH	Specifies the word length to be transmitted or received 0x0: 5 bits 0x1: 6 bits 0x2: 7 bits 0x3: 8 bits	RW	0x0

UART_LCR[3]	UART_LCR[4]	UART_LCR[5]	Parity
0	N/A	N/A	No parity
1	0	0	Odd parity
1	1	0	Even parity
1	0	1	Forced 1
1	1	1	Forced 0

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Table 23-183. Register Call Summary for Register UART_LCR

UART/IrDA/CIR

- SIR Mode: [0]
- Operational Mode and Configuration Modes: [1] [2] [3] [4] [5] [6]
- Registers Available for the Register Access Modes: [7] [8] [9] [10] [11] [12]
- Registers Available for the UART Function: [13] [14] [15] [16] [17] [18]
- Registers Available for the IrDA Function (UART3 Only): [19] [20] [21] [22] [23] [24]
- Registers Available for the CIR Function (UART3 Only): [25] [26] [27] [28] [29] [30]
- UART Data Formatting: [31] [32] [33] [34] [35] [36] [37]
- SIR Mode Data Formatting: [38] [39] [40]
- FIFOs and DMA Settings: [41] [42] [43] [44] [45] [46]
- Protocol, Baud Rate, and Interrupt Settings: [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60] [61] [62] [63]
- Hardware Flow Control Configuration: [64] [65] [66] [67] [68]
- Software Flow Control Configuration: [69] [70] [71] [72] [73] [74]
- Receive: [75] [76] [77] [78]
- Transmit: [79] [80] [81] [82] [83]
- Receive: [84] [85] [86] [87]
- Transmit: [88] [89] [90] [91]
- Receive: [92] [93] [94] [95] [96]
- Transmit: [97] [98]
- UART/IrDA/CIR Register Summary: [99] [100] [101]
- UART/IrDA/CIR Register Description: [102] [103] [104] [105] [106] [107] [108] [109] [110] [111] [112]

Table 23-184. UART_XON1_ADDR1

Address Offset	0x0000 0010		
Physical Address	0x4806 A010	**Instance**	UART1
	0x4806 C010		UART2
	0x4802 0010		UART3
	0x4806 E010		UART4
	0x4806 6010		UART5
	0x4806 8010		UART6
Description	UART mode: XON1 character, IrDA mode: ADDR1 address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XON_WORD1							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	XON_WORD1	Stores the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes	RW	0x00

Table 23-185. Register Call Summary for Register UART_XON1_ADDR1

UART/IrDA/CIR

- SIR Mode: [0]
- Registers Available for the Register Access Modes: [1] [2]
- Registers Available for the UART Function: [3] [4]
- Registers Available for the IrDA Function (UART3 Only): [5] [6]
- IrDA Data Formatting: [7]
- Software Flow Control Configuration: [8] [9]
- UART/IrDA/CIR Register Summary: [10] [11] [12]

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Table 23-186. UART_MCR

Address Offset	0x0000 0010		
Physical Address	0x4806 A010 0x4806 C010 0x4802 0010 0x4806 E010 0x4806 6010 0x4806 8010	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Modem control register MCR[3:0] controls the interface with the modem, data set, or peripheral device that emulates the modem.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED	TCR_TLR	XON_EN	LOOPBACK_EN	CD_STS_CH	RI_STS_CH	RTS	DTR

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	RESERVED	Read returns 0. Write has no effect.	RW	0
6	TCR_TLR	0x0: No action 0x1: Enables access to the UART_TCR and UART_TLR registers	RW	0
5	XON_EN	0x0: Disable XON any function. 0x1: Enable XON any function.	RW	0
4	LOOPBACK_EN	0x0: Normal operating mode 0x1: Enable local loopback mode (internal). In this mode, the MCR[3:0] signals are looped back into the UART_MSR[7:4] bit field. The transmit output is looped back to the receive input internally.	RW	0
3	CD_STS_CH	0x0: In loopback, forces DCD* input high and IRQ outputs to inactive state 0x1: In loopback, forces DCD* input low and IRQ outputs to inactive state	RW	0
2	RI_STS_CH	0x0: In loopback, forces RI* input high 0x1: In loopback, forces RI* input low	RW	0
1	RTS	In loopback, controls the UART_MSR[4] bit. If auto-RTS is enabled, the RTS* output is controlled by hardware flow control. 0x0: Force RTS* output to inactive (high). 0x1: Force RTS* output to active (low).	RW	0
0	DTR	0x0: Force DTR* output to inactive (high). 0x1: Force DTR* output to active (low).	RW	0

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Table 23-187. Register Call Summary for Register UART_MCR

UART/IrDA/CIR

- Description: [0] [1]
- Register Access Submode: [2] [3] [4] [5] [6] [7]
- Registers Available for the Register Access Modes: [8] [9] [10] [11]
- Registers Available for the UART Function: [12] [13] [14] [15]
- UART Data Formatting: [16] [17]
- FIFOs and DMA Settings: [18] [19] [20] [21] [22]
- Hardware Flow Control Configuration: [23] [24] [25] [26] [27]
- Software Flow Control Configuration: [28] [29] [30] [31] [32] [33] [34]
- Transmit: [35]
- Receive: [36] [37] [38]
- Transmit: [39]
- Transmit: [40]
- UART/IrDA/CIR Register Summary: [41] [42] [43]
- UART/IrDA/CIR Register Description: [44] [45] [46] [47] [48] [49] [50] [51]

Table 23-188. UART_LSR

Address Offset	0x0000 0014		
Physical Address	0x4806 A014	**Instance**	UART1
	0x4806 C014		UART2
	0x4802 0014		UART3
	0x4806 E014		UART4
	0x4806 6014		UART5
	0x4806 8014		UART6
Description	Line status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7	RX_FIFO_STS	Read 0x0: Normal operation Read 0x1: At least one parity error, framing error, or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.	R	0
6	TX_SR_E	Read 0x0: Transmitter hold (TX FIFO) and shift registers are not empty. Read 0x1: Transmitter hold (TX FIFO) and shift registers are empty.	R	1
5	TX_FIFO_E	Read 0x0: Transmit hold register (TX FIFO) is not empty. Read 0x1: Transmit hold register (TX FIFO) is empty. The transmission is not necessarily complete.	R	1
4	RX_BI	Read 0x0: No break condition Read 0x1: A break was detected while the data from the RX FIFO was received (for example, RX input was low for one character + 1 bit time frame).	R	0
3	RX_FE	Read 0x0: No framing error in data RX FIFO Read 0x1: Framing error occurred in data from RX FIFO (received data did not have a valid stop-bit).	R	0

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Bits	Field Name	Description	Type	Reset
2	RX_PE	Read 0x0: No parity error in data from RX FIFO Read 0x1: Parity error in data from RX FIFO	R	0
1	RX_OE	Read 0x0: No overrun error Read 0x1: Overrun error occurred. Set when the character in the receive shift register is not transferred to the RX FIFO. This occurs only when the RX FIFO is full.	R	0
0	RX_FIFO_E	Read 0x0: No data in the RX FIFO Read 0x1: At least one data character in the RX FIFO	R	0

Table 23-189. Register Call Summary for Register UART_LSR

UART/IrDA/CIR

- SIR Mode: [0]
- MIR Mode: [1]
- FIR Mode: [2]
- UART Interrupts: [3] [4]
- FIFO Polled Mode Operation: [5]
- Registers Available for the Register Access Modes: [6] [7]
- Registers Available for the UART Function: [8] [9]
- Registers Available for the IrDA Function (UART3 Only): [10] [11]
- Registers Available for the CIR Function (UART3 Only): [12] [13]
- UART Data Formatting: [14] [15] [16] [17] [18] [19] [20]
- IrDA Data Formatting: [21] [22]
- MIR and FIR Mode Data Formatting: [23]
- UART/IrDA/CIR Register Summary: [24] [25] [26]
- UART/IrDA/CIR Register Description: [27]

Table 23-190. UART_LSR_IRDA

Address Offset	0x0000 0014		
Physical Address	0x4806 A014	**Instance**	UART1
	0x4806 C014		UART2
	0x4802 0014		UART3
	0x4806 E014		UART4
	0x4806 6014		UART5
	0x4806 8014		UART6
Description	When the LSR is read, LSR[4:2] reflect the error bits [FL, CRC, ABORT] of the frame at the top of the STATUS FIFO (next frame status to be read).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7	THR_EMPTY	Read 0x0: Transmit holding register (TX FIFO) is not empty. Read 0x1: Transmit hold register (TX FIFO) is empty. The transmission is not necessarily complete.	R	1
6	STS_FIFO_FULL	Read 0x0: Status FIFO not full	R	0

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Bits	Field Name	Description	Type	Reset
		Read 0x1: Status FIFO full		
5	RX_LAST_BYTE	Read 0x0: The RX FIFO (RHR) does not contain the last byte of the frame to be read. Read 0x1: The RX FIFO (RHR) contains the last byte of the frame to be read. This bit is set only when the last byte of a frame is available to be read. It determines the frame boundary. It is cleared on a single read of the LSR register. See the note below.	R	0
4	FRAME_TOO_LONG	Read 0x0: No frame-too-long error in frame Read 0x1: Frame-too-long error in the frame at the top of the STATUS FIFO, (next character to be read). This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) is received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected.	R	0
3	ABORT	Read 0x0: No abort pattern error in frame Read 0x1: Abort pattern is received. SIR and MIR: Abort pattern FIR: Illegal symbol	R	0
2	CRC	Read 0x0: No CRC error in frame Read 0x1: CRC error in the frame at the top of the STATUS FIFO (next character to be read)	R	0
1	STS_FIFO_E	Read 0x0: Status FIFO not empty Read 0x1: Status FIFO empty	R	1
0	RX_FIFO_E	Read 0x0: No data in the RX FIFO Read 0x1: At least one data character in the RX FIFO	R	1

Table 23-191. Register Call Summary for Register UART_LSR_IRDA

UART/IrDA/CIR

- UART/IrDA/CIR Register Summary: [0] [1] [2]

Table 23-192. UART_LSR_CIR

Address Offset	0x0000 0014		
Physical Address	0x4806 A014 0x4806 C014 0x4802 0014 0x4806 E014 0x4806 6014 0x4806 8014	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Line status register in CIR mode		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								THR_EMPTY	RESERVED	RX_STOP	RESERVED				RX_FIFO_E

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7	THR_EMPTY	Read 0x0: Transmit holding register (TX FIFO) is not empty. Read 0x1: Transmit hold register (TX FIFO) is empty. The transmission is not necessarily complete.	R	1

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Bits	Field Name	Description	Type	Reset
6	RESERVED	Not used in CIR mode	R	0
5	RX_STOP	The RX_STOP is generated based on the value set in the BOF Length register (UART_EBLR). It is cleared on a single read of the UART_LSR register. Read 0x0: Reception is ongoing or waiting for a new frame. Read 0x1: Reception is complete.	R	0
4:1	RESERVED	Not used in CIR mode	R	0x0
0	RX_FIFO_E	Read 0x0: At least one data character in the RX FIFO Read 0x1: No data in the RX FIFO	R	1

Table 23-193. Register Call Summary for Register UART_LSR_CIR

UART/IrDA/CIR
- UART/IrDA/CIR Register Summary: [0] [1] [2]

Table 23-194. UART_XON2_ADDR2

Address Offset	0x0000 0014		
Physical Address	0x4806 A014 0x4806 C014 0x4802 0014 0x4806 E014 0x4806 6014 0x4806 8014	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Stores the 8-bit XON2 character in UART moldes and ADDR2 address 2 for IrDA modes		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XON_WORD2							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	XON_WORD2	Stores the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes	RW	0x00

Table 23-195. Register Call Summary for Register UART_XON2_ADDR2

UART/IrDA/CIR
- SIR Mode: [0]
- Registers Available for the Register Access Modes: [1] [2]
- Registers Available for the UART Function: [3] [4]
- Registers Available for the IrDA Function (UART3 Only): [5] [6]
- IrDA Data Formatting: [7]
- Software Flow Control Configuration: [8] [9]
- UART/IrDA/CIR Register Summary: [10] [11] [12]

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Table 23-196. UART_TCR

Address Offset	0x0000 0018		
Physical Address	0x4806 A018	**Instance**	UART1
	0x4806 C018		UART2
	0x4802 0018		UART3
	0x4806 E018		UART4
	0x4806 6018		UART5
	0x4806 8018		UART6
Description	Transmission control register		
	This register stores the RX FIFO threshold levels to start/stop transmission during hardware/software flow control. Notes: Trigger levels from 0 to 60 bytes are available with a granularity of 4. (Trigger level = 4 x [4-bit register value]) The programmer must ensure that UART_TCR[3:0] > UART_TCR[7:4] when auto-RTS or software flow control is enabled to avoid a mis-operation of the device. In FIFO interrupt mode with flow control, the programmer must ensure that the trigger level to halt transmission is greater than or equal to the RX FIFO trigger level (UART_TLR[7:4] or UART_FCR[7:6]); otherwise, FIFO operation stalls. In FIFO DMA mode with flow control, this concept does not exist because a DMA request is sent each time a byte is received.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_FIFO_TRIG_START				RX_FIFO_TRIG_HALT			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:4	RX_FIFO_TRIG_START	RX FIFO trigger level to RESTORE transmission (0 - 60)	RW	0x0
3:0	RX_FIFO_TRIG_HALT	RX FIFO trigger level to HALT transmission (0 - 60)	RW	0xF

Table 23-197. Register Call Summary for Register UART_TCR

UART/IrDA/CIR

- Receive FIFO Trigger: [0] [1] [2]
- FIFO Interrupt Mode: [3]
- Registers Available for the Register Access Modes: [4] [5] [6] [7] [8] [9]
- Registers Available for the UART Function: [10] [11] [12] [13] [14] [15]
- Registers Available for the IrDA Function (UART3 Only): [16] [17] [18] [19] [20] [21]
- Registers Available for the CIR Function (UART3 Only): [22] [23] [24] [25] [26] [27]
- UART Data Formatting: [28] [29] [30] [31] [32] [33]
- Hardware Flow Control Configuration: [34] [35] [36] [37] [38] [39]
- Software Flow Control Configuration: [40] [41] [42] [43] [44] [45]
- UART/IrDA/CIR Register Summary: [46] [47] [48]
- UART/IrDA/CIR Register Description: [49] [50] [51] [52]

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Table 23-198. UART_XOFF1

Address Offset	0x0000 0018		
Physical Address	0x4806 A018 0x4806 C018 0x4802 0018 0x4806 E018 0x4806 6018 0x4806 8018	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	UART mode XOFF1 character		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XOFF_WORD1							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	XOFF_WORD1	Stores the 8-bit XOFF1 character used in UART modes	RW	0x00

Table 23-199. Register Call Summary for Register UART_XOFF1

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1]
- Registers Available for the UART Function: [2] [3]
- Software Flow Control Configuration: [4] [5] [6]
- UART/IrDA/CIR Register Summary: [7] [8] [9]

Table 23-200. UART_MSR

Address Offset	0x0000 0018		
Physical Address	0x4806 A018 0x4806 C018 0x4802 0018 0x4806 E018 0x4806 6018 0x4806 8018	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Modem status register. UART mode only. This register provides information about the current state of the control lines from the modem, data set, or peripheral device to the LH. It also indicates when a control input from the modem changes state.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7	NCD_STS	This bit is the complement of the DCD* input. In loopback mode, it is equivalent to UART_MCR[3].	R	-
6	NRI_STS	This bit is the complement of the RI* input. In loopback mode, it is equivalent to UART_MCR[2].	R	-
5	NDSR_STS	This bit is the complement of the DSR* input. In loopback mode, it is equivalent to UART_MCR[0].	R	-
4	NCTS_STS	This bit is the complement of the CTS* input. In loopback mode, it is equivalent to UART_MCR[1].	R	-

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Bits	Field Name	Description	Type	Reset
3	DCD_STS	Indicates that DCD* input (or UART_MCR[3] in loopback) changed. Cleared on a read.	R	0
2	RI_STS	Indicates that RI* input (or UART_MCR[2] in loopback) changed state from low to high. Cleared on a read.	R	0
1	DSR_STS	Read 0x1: Indicates that DSR* input (or UART_MCR[0] in loopback) changed state. Cleared on a read.	R	0
0	CTS_STS	Read 0x1: Indicates that CTS* input (or UART_MCR[1] in loopback) changed state. Cleared on a read.	R	0

Table 23-201. Register Call Summary for Register UART_MSR

UART/IrDA/CIR

- Description: [0] [1]
- UART Interrupts: [2] [3]
- Registers Available for the Register Access Modes: [4] [5]
- Registers Available for the UART Function: [6] [7]
- Registers Available for the IrDA Function (UART3 Only): [8] [9]
- Registers Available for the CIR Function (UART3 Only): [10] [11]
- UART/IrDA/CIR Register Summary: [12] [13] [14]
- UART/IrDA/CIR Register Description: [15] [16]

Table 23-202. UART_SPR

Address Offset	0x0000 001C		
Physical Address	0x4806 A01C	**Instance**	UART1
	0x4806 C01C		UART2
	0x4802 001C		UART3
	0x4806 E01C		UART4
	0x4806 601C		UART5
	0x4806 801C		UART6
Description	Scratchpad register This read/write register does not control the module. It is a scratchpad register to be used by the programmer to hold temporary data.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SPR_WORD							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	SPR_WORD	Scratchpad register	RW	0x00

Table 23-203. Register Call Summary for Register UART_SPR

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2] [3]
- Registers Available for the UART Function: [4] [5] [6] [7]
- Registers Available for the IrDA Function (UART3 Only): [8] [9] [10] [11]
- Registers Available for the CIR Function (UART3 Only): [12] [13] [14] [15]
- UART/IrDA/CIR Register Summary: [16] [17] [18]

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Table 23-204. UART_TLR

Address Offset	0x0000 001C		
Physical Address	0x4806 A01C 0x4806 C01C 0x4802 001C 0x4806 E01C 0x4806 601C 0x4806 801C	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Trigger level register This register stores the programmable transmit and RX FIFO trigger levels for DMA and IRQ generation.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_FIFO_TRIG_DMA				TX_FIFO_TRIG_DMA			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:4	RX_FIFO_TRIG_DMA	Receive FIFO trigger level	RW	0x0
3:0	TX_FIFO_TRIG_DMA	Transmit FIFO trigger level	RW	0x0

Table 23-205. Register Call Summary for Register UART_TLR

UART/IrDA/CIR

- FIFO Management: [0]
- Transmit FIFO Trigger: [1] [2]
- Receive FIFO Trigger: [3] [4]
- FIFO Interrupt Mode: [5] [6]
- DMA Transfers (DMA Mode 1, 2, or 3): [7] [8] [9] [10]
- Registers Available for the Register Access Modes: [11] [12] [13] [14] [15] [16]
- Registers Available for the UART Function: [17] [18] [19] [20] [21] [22]
- Registers Available for the IrDA Function (UART3 Only): [23] [24] [25] [26] [27] [28]
- Registers Available for the CIR Function (UART3 Only): [29] [30] [31] [32] [33] [34]
- FIFOs and DMA Settings: [35] [36] [37] [38] [39] [40]
- UART/IrDA/CIR Register Summary: [41] [42] [43]
- UART/IrDA/CIR Register Description: [44] [45] [46] [47] [48] [49]

Table 23-206. UART_XOFF2

Address Offset	0x0000 001C		
Physical Address	0x4806 A01C 0x4806 C01C 0x4802 001C 0x4806 E01C 0x4806 601C 0x4806 801C	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	UART mode XOFF2 character		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XOFF_WORD2							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	XOFF_WORD2	Stores the 8-bit XOFF2 character used in UART modes.	RW	0x00

Table 23-207. Register Call Summary for Register UART_XOFF2

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1]
- Registers Available for the UART Function: [2] [3]
- Software Flow Control Configuration: [4] [5] [6]
- UART/IrDA/CIR Register Summary: [7] [8] [9]

Table 23-208. UART_MDR1

Address Offset	0x0000 0020		
Physical Address	0x4806 A020	**Instance**	UART1
	0x4806 C020		UART2
	0x4802 0020		UART3
	0x4806 E020		UART4
	0x4806 6020		UART5
	0x4806 8020		UART6
Description	Mode definition register 1		
	The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on startup after configuration of the configuration registers (UART_DLL, UART_DLH, and UART_LCR). The value of MDR1[2:0] must not be changed again during normal operation. **Note:** If the module is disabled by setting the MODE_SELECT field to 111, interrupt requests can still be generated unless disabled through the interrupt enable register (IER). In this case, UART mode interrupts are visible. Reading the interrupt identification register (IIR) shows UART mode interrupt flags.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	FRAME_END_MODE	IrDA mode only 0x0: Frame-length method 0x1: Set EOT bit method	RW	0
6	SIP_MODE	MIR/FIR modes only 0x0: Manual SIP mode: SIP is generated with the control of ACREG[3]. 0x1: Automatic SIP mode: SIP is generated after each transmission.	RW	0

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Bits	Field Name	Description	Type	Reset
5	SCT	Store and control the transmission. 0x0: Starts the infrared transmission when a value is written to THR 0x1: Starts the infrared transmission with the control of ACREG[2]. **Note:** Before starting any transmission, there must be no reception ongoing.	RW	0
4	SET_TXIR	Used to configure the infrared transceiver 0x0: a) No action if MDR2[7] = 0 b) TXIR pin output is forced low if MDR2[7] = 1. 0x1: IRTX pin output is forced high (not dependent on MDR2[7] value).	RW	0
3	IR_SLEEP	0x0: IrDA/CIR sleep mode disabled 0x1: IrDA/CIR sleep mode enabled	RW	0
2:0	MODE_SELECT	0x0: UART 16x mode 0x1: SIR mode 0x2: UART 16x auto-baud 0x3: UART 13x mode 0x4: MIR mode 0x5: FIR mode 0x6: CIR mode 0x7: Disable (default state)	RW	0x7

Table 23-209. Register Call Summary for Register UART_MDR1

UART/IrDA/CIR

- Description: [0] [1]
- UART Protocol and Data Format: [2]
- Registers Available for the Register Access Modes: [3] [4] [5] [6] [7] [8]
- UART/IrDA (SIR, MIR, FIR)/CIR Mode Selection: [9]
- Registers Available for the UART Function: [10] [11] [12] [13] [14] [15]
- Registers Available for the IrDA Function (UART3 Only): [16] [17] [18] [19] [20] [21]
- Registers Available for the CIR Function (UART3 Only): [22] [23] [24] [25] [26] [27]
- UART Clock Generation: Baud Rate Generation: [28]
- UART Data Formatting: [29] [30]
- IrDA Clock Generation: Baud Generator: [31]
- IrDA Data Formatting: [32] [33]
- SIR Mode Data Formatting: [34] [35]
- MIR and FIR Mode Data Formatting: [36]
- CIR Data Formatting: [37]
- Protocol, Baud Rate, and Interrupt Settings: [38] [39] [40]
- Receive: [41] [42]
- Transmit: [43] [44] [45]
- Receive: [46] [47]
- Transmit: [48] [49]
- Receive: [50] [51]
- Transmit: [52] [53]
- UART/IrDA/CIR Register Summary: [54] [55] [56]
- UART/IrDA/CIR Register Description: [57]

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Table 23-210. UART_MDR2

Address Offset	0x0000 0024		
Physical Address	0x4806 A024	**Instance**	UART1
	0x4806 C024		UART2
	0x4802 0024		UART3
	0x4806 E024		UART4
	0x4806 6024		UART5
	0x4806 8024		UART6
Description	Mode definition register 2		
	IR-IrDA and IR-CIR modes only. UART_MDR2[0] describes the status of the interrupt in UART_IIR[5]. The IRTX_UNDERRUN bit should be read after an UART_IIR[5] TX_STATUS_IT interrupt. The bits [2:1] of this register set the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in UART_MDR1[2:0]. **Note:** The UART_MDR2[6] gives the flexibility to invert the RX pin in the UART to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most transceivers invert the IR receive pin.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	SET_TXIR_ALT	Provide alternate function for MDR1[4] (SET_TXIR). 0x0: Normal mode 0x1: Alternate mode for SET_TXIR	R	0
6	IRRXINVERT	IR mode only (IrDA and CIR). Invert RX pin in the module before the voting or sampling system logic of the infrared block. This does not affect the RX path in UART modem modes. 0x0: Inversion is performed. 0x1: No inversion is performed.	RW	0
5:4	CIR_PULSE_MODE	CIR pulse modulation definition. Defines high level of the pulse width associated with a digit: 0x0: Pulse width of 3 from 12 cycles 0x1: Pulse width of 4 from 12 cycles 0x2: Pulse width of 5 from 12 cycles 0x3: Pulse width of 6 from 12 cycles	RW	0x0
3	UART_PULSE	UART mode only. Allows pulse shaping in UART mode. 0x0: Normal UART mode 0x1: UART mode with a pulse shaping	RW	0
2:1	STS_FIFO_TRIG	IR-IrDA mode only. Frame status FIFO threshold select: 0x0: 1 entry 0x1: 4 entries 0x2: 7 entries 0x3: 8 entries	RW	0x0

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Bits	Field Name	Description	Type	Reset
0	IRTX_UNDERRUN	IrDA transmission status interrupt. When the UART_IIR[5] interrupt occurs, the meaning of the interrupt is: Read 0x0: The last bit of the frame transmitted successfully without error. Read 0x1: An underrun occurred. The last bit of the frame was transmitted but with an underrun error. The bit is reset to 0 when the UART_RESUME register is read.	R	0

Table 23-211. Register Call Summary for Register UART_MDR2

UART/IrDA/CIR

- SIR Mode: [0]
- Pulse Duty Cycle: [1]
- Registers Available for the Register Access Modes: [2] [3] [4] [5] [6] [7]
- Registers Available for the UART Function: [8] [9] [10] [11] [12] [13]
- Registers Available for the IrDA Function (UART3 Only): [14] [15] [16] [17] [18] [19]
- Registers Available for the CIR Function (UART3 Only): [20] [21] [22] [23] [24] [25]
- IrDA Data Formatting: [26]
- SIR Mode Data Formatting: [27]
- CIR Mode Clock Generation: [28] [29]
- UART/IrDA/CIR Register Summary: [30] [31] [32]
- UART/IrDA/CIR Register Description: [33] [34]

Table 23-212. UART_SFLSR

Address Offset	0x0000 0028		
Physical Address	0x4806 A028	**Instance**	UART1
	0x4806 C028		UART2
	0x4802 0028		UART3
	0x4806 E028		UART4
	0x4806 6028		UART5
	0x4806 8028		UART6
Description	Status FIFO line status register IrDA modes only. Reading this register effectively reads frame status information from the status FIFO (this register does not physically exist). Reading this register increments the status FIFO read pointer (SFREGL and SFREGH must be read first).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED			OE_ERROR	FRAME_TOO_LONG_ERROR	ABORT_DETECT	CRC_ERROR	RESERVED

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:5	RESERVED	Read returns 0.	R	0x0
4	OE_ERROR	Read 0x1: Overrun error in RX FIFO when frame at top of RX FIFO was received **Note:** Top of RX FIFO = Next frame to be read from RX FIFO	R	-

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Bits	Field Name	Description	Type	Reset
3	FRAME_TOO_LONG_ERROR	Read 0x1: Frame-length too long error in frame at top of RX FIFO	R	-
2	ABORT_DETECT	Read 0x1: Abort pattern detected in frame at top of RX FIFO	R	-
1	CRC_ERROR	Read 0x1: CRC error in frame at top of RX FIFO	R	-
0	RESERVED		R	0

Table 23-213. Register Call Summary for Register UART_SFLSR

UART/IrDA/CIR

- FIFO Management: [0]
- Registers Available for the Register Access Modes: [1] [2] [3]
- Registers Available for the IrDA Function (UART3 Only): [4] [5] [6]
- IrDA Data Formatting: [7] [8]
- UART/IrDA/CIR Register Summary: [9] [10] [11]
- UART/IrDA/CIR Register Description: [12] [13]

Table 23-214. UART_TXFLL

Address Offset	0x0000 0028		
Physical Address	0x4806 A028	**Instance**	UART1
	0x4806 C028		UART2
	0x4802 0028		UART3
	0x4806 E028		UART4
	0x4806 6028		UART5
	0x4806 8028		UART6
Description	Transmit frame length register low IrDA modes only. The UART_TXFLL and UART_TXFLH registers hold the 13-bit transmit frame length (expressed in bytes). UART_TXFLL holds the LSBs and UART_TXFLH holds the MSBs. The frame length value is used if the frame length method of frame closing is used.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TXFLL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:0	TXFLL	LSB register used to specify the frame length	W	0x00

Table 23-215. Register Call Summary for Register UART_TXFLL

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2]
- Registers Available for the IrDA Function (UART3 Only): [3] [4] [5]
- IrDA Data Formatting: [6]
- Transmit: [7]
- Transmit: [8]
- Transmit: [9]
- UART/IrDA/CIR Register Summary: [10] [11] [12]
- UART/IrDA/CIR Register Description: [13] [14] [15] [16]

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Table 23-216. UART_RESUME

Address Offset	0x0000 002C		
Physical Address	0x4806 A02C 0x4806 C02C 0x4802 002C 0x4806 E02C 0x4806 602C 0x4806 802C	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	IR-IrDA and IR-CIR modes only. This register is used to clear internal flags, which halt transmission/reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESUME							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:0	RESUME	Dummy read to restart the TX or RX	R	0x00

Table 23-217. Register Call Summary for Register UART_RESUME

UART/IrDA/CIR

- IrDA Interrupts: [0] [1]
- Registers Available for the Register Access Modes: [2] [3] [4]
- Registers Available for the IrDA Function (UART3 Only): [5] [6] [7]
- Registers Available for the CIR Function (UART3 Only): [8] [9] [10]
- UART Data Formatting: [11]
- IrDA Data Formatting: [12]
- UART/IrDA/CIR Register Summary: [13] [14] [15]
- UART/IrDA/CIR Register Description: [16]

Table 23-218. UART_TXFLH

Address Offset	0x0000 002C		
Physical Address	0x4806 A02C 0x4806 C02C 0x4802 002C 0x4806 E02C 0x4806 602C 0x4806 802C	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Transmit frame length register high IrDA modes only. The UART_TXFLL and UART_TXFLH registers hold the 13-bit transmit frame length (expressed in bytes). UART_TXFLL holds the LSBs and UART_TXFLH holds the MSBs. The frame length value is used if the frame length method of frame closing is used.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED			TXFLH				

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Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:5	RESERVED	Write has no effect.	W	0x0
4:0	TXFLH	MSB register used to specify the frame length	W	0x00

Table 23-219. Register Call Summary for Register UART_TXFLH

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2]
- Registers Available for the IrDA Function (UART3 Only): [3] [4] [5]
- IrDA Data Formatting: [6]
- Transmit: [7]
- UART/IrDA/CIR Register Summary: [8] [9] [10]
- UART/IrDA/CIR Register Description: [11] [12] [13] [14]

Table 23-220. UART_SFREGL

Address Offset	0x0000 0030		
Physical Address	0x4806 A030	**Instance**	UART1
	0x4806 C030		UART2
	0x4802 0030		UART3
	0x4806 E030		UART4
	0x4806 6030		UART5
	0x4806 8030		UART6
Description	Status FIFO register low		
	IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the UART_SFREGL and UART_SFREGH registers (these registers do not physically exist). The LsBs are read from UART_SFREGL and the MSBs are read from UART_SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the UART_SFLSR register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SFREGL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:0	SFREGL	LSB part of the frame length	R	0x-

Table 23-221. Register Call Summary for Register UART_SFREGL

UART/IrDA/CIR

- FIFO Management: [0]
- Registers Available for the Register Access Modes: [1] [2] [3]
- Registers Available for the IrDA Function (UART3 Only): [4] [5] [6]
- IrDA Data Formatting: [7]
- UART/IrDA/CIR Register Summary: [8] [9] [10]
- UART/IrDA/CIR Register Description: [11] [12] [13] [14]

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Table 23-222. UART_RXFLL

Address Offset	0x0000 0030		
Physical Address	0x4806 A030 0x4806 C030 0x4802 0030 0x4806 E030 0x4806 6030 0x4806 8030	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Received frame length register low IrDA modes only. The UART_RXFLL and UART_RXFLH registers hold the 12-bit receive maximum frame length. UART_RXFLL holds the LSBs and UART_RXFLH holds the MSBs. If the intended maximum receive frame length is n bytes, program the UART_RXFLL and UART_RXFLH registers to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are the result of frame format with CRC and stop flag; 2 bytes are associated with the FIR stop flag).		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RXFLL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:0	RXFLL	LSB register used to specify the frame length in reception	W	0x00

Table 23-223. Register Call Summary for Register UART_RXFLL

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2]
- Registers Available for the IrDA Function (UART3 Only): [3] [4] [5]
- Receive: [6]
- Transmit: [7]
- UART/IrDA/CIR Register Summary: [8] [9] [10]
- UART/IrDA/CIR Register Description: [11] [12] [13] [14] [15] [16]

Table 23-224. UART_SFREGH

Address Offset	0x0000 0034		
Physical Address	0x4806 A034 0x4806 C034 0x4802 0034 0x4806 E034 0x4806 6034 0x4806 8034	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Status FIFO register high IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the UART_SFREGL and UART_SFREGH registers (these registers do not physically exist). The LSBs are read from UART_SFREGL and the MSBs are read from UART_SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the UART_SFLSR register.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED				SFREGH			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:4	RESERVED	Read returns 0.	R	0x0
3:0	SFREGH	MSB part of the frame length	R	0x-

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Table 23-225. Register Call Summary for Register UART_SFREGH

UART/IrDA/CIR

- FIFO Management: [0]
- Registers Available for the Register Access Modes: [1] [2] [3]
- Registers Available for the IrDA Function (UART3 Only): [4] [5] [6]
- IrDA Data Formatting: [7]
- UART/IrDA/CIR Register Summary: [8] [9] [10]
- UART/IrDA/CIR Register Description: [11] [12] [13] [14]

Table 23-226. UART_RXFLH

Address Offset	0x0000 0034		
Physical Address	0x4806 A034 0x4806 C034 0x4802 0034 0x4806 E034 0x4806 6034 0x4806 8034	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Received frame length register high IrDA modes only. The UART_RXFLL and UART_RXFLH registers hold the 12-bit receive maximum frame length. UART_RXFLL holds the LSBs and UART_RXFLH holds the MSBs. If the intended maximum receive frame length is n bytes, program the UART_RXFLL and UART_RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are the result of frame format with CRC and stop flag; 2 bytes are associated with the FIR stop flag).		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED				RXFLH			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Write has no effect.	W	0x000000
7:4	RESERVED	Write has no effect.	W	0x0
3:0	RXFLH	MSB register used to specify the frame length in reception	W	0x0

Table 23-227. Register Call Summary for Register UART_RXFLH

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2]
- Registers Available for the IrDA Function (UART3 Only): [3] [4] [5]
- Transmit: [6]
- UART/IrDA/CIR Register Summary: [7] [8] [9]
- UART/IrDA/CIR Register Description: [10] [11] [12] [13] [14] [15]

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Table 23-228. UART_BLR

Address Offset	0x0000 0038		
Physical Address	0x4806 A038 0x4806 C038 0x4802 0038 0x4806 E038 0x4806 6038 0x4806 8038	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	BOF control register IrDA modes only. The UART_BLR[6] bit selects whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR mode. If only one start flag is required, this is always 0xC0. If n start flags are required, (-1) 0xC0 or (-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STS_FIFO_RESET	XBOF_TYPE	RESERVED					

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	STS_FIFO_RESET	Status FIFO reset. This bit is self-clearing.	RW	0
6	XBOF_TYPE	SIR xBOF select 0x0: 0xFF 0x1: 0xC0	RW	1
5:0	RESERVED	Read returns 0.	R	0x00

Table 23-229. Register Call Summary for Register UART_BLR

UART/IrDA/CIR

- SIR Mode: [0]
- Registers Available for the Register Access Modes: [1] [2]
- Registers Available for the IrDA Function (UART3 Only): [3] [4]
- UART/IrDA/CIR Register Summary: [5] [6] [7]
- UART/IrDA/CIR Register Description: [8]

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Table 23-230. UART_UASR

Address Offset	0x0000 0038		
Physical Address	0x4806 A038	**Instance**	UART1
	0x4806 C038		UART2
	0x4802 0038		UART3
	0x4806 E038		UART4
	0x4806 6038		UART5
	0x4806 8038		UART6
Description	UART autobauding status register		
	UART autobauding mode only. This status register returns the speed, the number of bits by characters, and the type of the parity in UART autobauding mode. In autobauding mode, the input frequency of the UART modem must be fixed to 48 MHz. Any other module clock frequency results in incorrect baud rate recognition. **Note:** When the UART is in autobauding mode, this register, instead of the LCR, DLL, and DLH registers, is used to set up transmission according to the characteristics of the previous reception. To reset the autobauding hardware (to start a new AT detection), set MDR1[2:0] to 111 (reset value), then set MDR1[2:1] to 010 (UART in autobaud mode). To set the UART to standard mode (no autobaud), set MDR1[2:1] to 000.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PARITY_TYPE		BIT_BY_CHAR	SPEED				

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:6	PARITY_TYPE	Read 0x0: No parity identified	R	0x0
		Read 0x1: Parity space		
		Read 0x2: Even parity		
		Read 0x3: Odd parity		
5	BIT_BY_CHAR	Read 0x0: 7-bit character identified	R	0
		Read 0x1: 8-bit character identified		
4:0	SPEED	Used to report the speed identified	R	0x00
		Read 0x0: No speed identified		
		Read 0x1: 115,200 baud		
		Read 0x2: 57,600 baud		
		Read 0x3: 38,400 baud		
		Read 0x4: 28,800 baud		
		Read 0x5: 19,200 baud		
		Read 0x6: 14,400 baud		
		Read 0x7: 9,600 baud		
		Read 0x8: 4,800 baud		
		Read 0x9: 2,400 baud		
		Read 0xA: 1,200 baud		

Table 23-231. Register Call Summary for Register UART_UASR

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1]
- Registers Available for the UART Function: [2] [3]
- UART Data Formatting: [4] [5] [6]
- UART/IrDA/CIR Register Summary: [7] [8] [9]

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Table 23-232. UART_ACREG

Address Offset	0x0000 003C		
Physical Address	0x4806 A03C 0x4806 C03C 0x4802 003C 0x4806 E03C 0x4806 603C 0x4806 803C	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Auxiliary control register. IR-IrDA and IR-CIR modes only.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDERRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	PULSE_TYPE	SIR pulse width select 0x0: 3/16 of baud-rate pulse width 0x1: 1.6 µs	RW	0
6	SD_MOD	Primary output used to configure transceivers. Connected to the SD/MODE input pin of IrDA transceivers. 0x0: SD pin is set to high. 0x1: SD pin is set to low.	RW	0
5	DIS_IR_RX	0x0: Normal operation (RX input automatically disabled during transmit but enabled outside of transmit operation) 0x1: Disables RX input (permanent state - independent of transmit)	RW	0
4	DIS_TX_UNDERRUN	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4] = 1, garbage data is sent over TX line. 0x0: Long stop-bits cannot be transmitted; TX underrun is enabled. 0x1: Long stop-bits can be transmitted; TX underrun is disabled.	RW	0
3	SEND_SIP	MIR/FIR modes only. Send serial infrared interaction pulse (SIP). If this bit is set during an MIR/FIR transmission, the SIP is sent at the end of it. This bit is cleared automatically at the end of the SIP transmission. 0x0: No action 0x1: Send SIP pulse.	RW	0
2	SCTX_EN	Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit, the TX state-machine starts frame transmission. This bit is self-clearing.	RW	0
1	ABORT_EN	Frame abort. The LH can intentionally abort transmission of a frame by writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If TX FIFO is not empty and MDR1[5] = 1, UART IrDA starts a new transfer with data of the previous frame when the abort frame is sent. Therefore, TX FIFO must be reset before sending an abort frame.	RW	0

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Bits	Field Name	Description	Type	Reset
0	EOT_EN	EOT (end of transmission) bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit is cleared automatically when the LH writes to the THR (TX FIFO).	RW	0

Table 23-233. Register Call Summary for Register UART_ACREG

UART/IrDA/CIR

- UART3 Interface Description: [0]
- SIR Mode: [1] [2] [3] [4]
- CIR Interface Description: [5]
- Registers Available for the Register Access Modes: [6] [7]
- Registers Available for the IrDA Function (UART3 Only): [8] [9]
- Registers Available for the CIR Function (UART3 Only): [10] [11]
- IrDA Data Formatting: [12] [13] [14] [15]
- SIR Mode Data Formatting: [16] [17]
- MIR and FIR Mode Data Formatting: [18]
- CIR Data Formatting: [19]
- Transmit: [20]
- Transmit: [21]
- Transmit: [22]
- UART/IrDA/CIR Register Summary: [23] [24] [25]

Table 23-234. UART_SCR

Address Offset	0x0000 0040		
Physical Address	0x4806 A040	**Instance**	UART1
	0x4806 C040		UART2
	0x4802 0040		UART3
	0x4806 E040		UART4
	0x4806 6040		UART5
	0x4806 8040		UART6
Description	Supplementary control register		
	Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the UART_IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the UART_IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit UART_SCR[4] must be reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_TRIG_GRANU1	TX_TRIG_GRANU1	DSR_IT	RX_CTS_DSR_WAKE_UP_ENABLE	TX_EMPTY_CTL_IT	DMA_MODE_2	DMA_MODE_CTL	

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	RX_TRIG_GRANU1	0x0: Disables the granularity of 1 for trigger RX level 0x1: Enables the granularity of 1 for trigger RX level	RW	0
6	TX_TRIG_GRANU1	0x0: Disables the granularity of 1 for trigger TX level	RW	0

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Bits	Field Name	Description	Type	Reset
		0x1: Enables the granularity of 1 for trigger TX level		
5	DSR_IT	0x0: Disables DSR* interrupt	RW	0
		0x1: Enables DSR* interrupt		
4	RX_CTS_DSR_WAKE_UP_ENABLE	0x0: Disables the wake-up interrupt and clears SSR[1]	RW	0
		0x1: Waits for a falling edge of pins RX, CTS*, or DSR* to generate an interrupt		
3	TX_EMPTY_CTL_IT	0x0: Normal mode for THR interrupt (see UART mode interrupts table)	RW	0
		0x1: The THR interrupt is generated when TX FIFO and TX shift register are empty.		
2:1	DMA_MODE_2	Used to specify the DMA mode valid if the UART_SCR[0] bit = 1	RW	0x0
		0x0: DMA mode 0 (no DMA)		
		0x1: DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)		
		0x2: DMA mode 2 (UART_nDMA_REQ[0] in RX)		
		0x3: DMA mode 3 (UART_nDMA_REQ[0] in TX)		
0	DMA_MODE_CTL	0x0: The DMA_MODE is set with UART_FCR[3].	RW	0
		0x1: The DMA_MODE is set with UART_SCR[2:1].		

Table 23-235. Register Call Summary for Register UART_SCR

UART/IrDA/CIR

- Module Power Saving: [0]
- Wake-Up Interrupt: [1] [2]
- FIFO Management: [3]
- Transmit FIFO Trigger: [4]
- Receive FIFO Trigger: [5]
- FIFO DMA Mode Operation: [6] [7]
- Registers Available for the Register Access Modes: [8] [9] [10] [11] [12] [13]
- Registers Available for the UART Function: [14] [15] [16] [17] [18] [19]
- Registers Available for the IrDA Function (UART3 Only): [20] [21] [22] [23] [24] [25]
- Registers Available for the CIR Function (UART3 Only): [26] [27] [28] [29] [30] [31]
- FIFOs and DMA Settings: [32] [33] [34] [35] [36] [37] [38] [39]
- UART/IrDA/CIR Register Summary: [40] [41] [42]
- UART/IrDA/CIR Register Description: [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55]

Table 23-236. UART_SSR

Address Offset	0x0000 0044		
Physical Address	0x4806 A044	**Instance**	UART1
	0x4806 C044		UART2
	0x4802 0044		UART3
	0x4806 E044		UART4
	0x4806 6044		UART5
	0x4806 8044		UART6
Description	Supplementary status register		
	Note: Bit 1 is reset only when UART_SCR[4] is reset to 0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED					DMA_COUNTER_RST	RX_CTS_DSR_WAKE_UP_STS	TX_FIFO_FULL

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:3	RESERVED	Read returns 0.	R	0x00
2	DMA_COUNTER_RST	0x0: The DMA counter will not be reset if the corresponding FIFO is reset (through FCR[1] or FCR[2]). 0x1: The DMA counter will be reset if corresponding FIFO is reset (through FCR[1] or FCR[2]).	RW	1
1	RX_CTS_DSR_WAKE_UP_STS	Read 0x0: No falling edge event on RX, CTS*, and DSR* Read 0x1: A falling edge occurred on RX, CTS*, or DSR*.	R	0
0	TX_FIFO_FULL	Read 0x0: TX FIFO is not full. Read 0x1: TX FIFO is full.	R	0

Table 23-237. Register Call Summary for Register UART_SSR

UART/IrDA/CIR

- Wake-Up Interrupt: [0]
- FIFO Management: [1]
- Registers Available for the Register Access Modes: [2] [3] [4]
- Registers Available for the UART Function: [5] [6] [7]
- Registers Available for the IrDA Function (UART3 Only): [8] [9] [10]
- Registers Available for the CIR Function (UART3 Only): [11] [12] [13]
- UART/IrDA/CIR Register Summary: [14] [15] [16]

Table 23-238. UART_EBLR

Address Offset	0x0000 0048		
Physical Address	0x4806 A048	**Instance**	UART1
	0x4806 C048		UART2
	0x4802 0048		UART3
	0x4806 E048		UART4
	0x4806 6048		UART5
	0x4806 8048		UART6
Description	BOF length register IR-IrDA and IR-CIR modes only. In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must account for the BOF character; therefore, to send only one BOF with no XBOF, this register must be set to 1. To send one BOF with N XBOF, this register must be set to N + 1. The value 0 sends 1 BOF plus 255 XBOF. In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags). In IR-CIR mode, this register specifies the number of consecutive 0s to be received before generating the RX_STOP interrupt (UART_IIR[2]). All received 0s are stored in the RX FIFO. When the register is set to 0, this feature is deactivated and always in reception state, which can be disabled by setting the ACREG[5] to 1. **Note:** If the RX_STOP interrupt occurs before a byte boundary, the remaining bits of the last byte are filled with 0s and passed into the RX FIFO.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								EBLR							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:0	EBLR	IR-IrDA mode: This register allows definition of up to 176 xBOFs, the maximum required by IrDA specification. IR-CIR mode: This register specifies the number of consecutive 0s to be received before generating the RX_STOP interrupt (UART_IIR[2]). 0x00: Feature disabled 0x01: Generate RX_STOP interrupt after receiving one zero bit. ... 0xFF: Generate RX_STOP interrupt after receiving 255 zero bits.	RW	0x00

Table 23-239. Register Call Summary for Register UART_EBLR

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1]
- Registers Available for the IrDA Function (UART3 Only): [2] [3]
- Registers Available for the CIR Function (UART3 Only): [4] [5]
- Transmit: [6]
- Transmit: [7]
- Transmit: [8]
- UART/IrDA/CIR Register Summary: [9] [10] [11]
- UART/IrDA/CIR Register Description: [12]

Table 23-240. UART_MVR

Address Offset	0x0000 0050		
Physical Address	0x4806 A050	**Instance**	UART1
	0x4806 C050		UART2
	0x4802 0050		UART3
	0x4806 E050		UART4
	0x4806 6050		UART5
	0x4806 8050		UART6
Description	Module version register The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															

Bits	Field Name	Description	Type	Reset
31:0	REV	Revision number	R	0x-- TI internal data

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Table 23-241. Register Call Summary for Register UART_MVR

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2]
- Registers Available for the UART Function: [3] [4] [5]
- Registers Available for the IrDA Function (UART3 Only): [6] [7] [8]
- Registers Available for the CIR Function (UART3 Only): [9] [10] [11]
- UART/IrDA/CIR Register Summary: [12] [13] [14]

Table 23-242. UART_SYSC

Address Offset	0x0000 0054		
Physical Address	0x4806 A054 0x4806 C054 0x4802 0054 0x4806 E054 0x4806 6054 0x4806 8054	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	System configuration register The AUTOIDLE bit controls a power-saving technique to reduce the logic power consumption of the open-core protocol (OCP) interface. When the feature is enabled, the clock is gated off until an OCP command for this device is detected. When the software reset bit is set high, it causes a full device reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7:5	RESERVED	Read returns 0.	R	0x0
4:3	IDLEMODE	Power management req/ack control ref: OCP Design Guidelines Version 1.1 0x0: Force-idle: Idle request is acknowledged unconditionally. 0x1: No-idle: Idle request is never acknowledged. 0x2: Smart-idle: Idle request is acknowledged based in module internal activity. 0x3: Smart-idle Wake-up: Acknowledgement to an idle request is given based in the internal activity of the module. The module is allowed to generate wake-up request.	RW	0x0
2	ENAWAKEUP	Wake-up feature control 0x0: Wakeup is disabled. 0x1: Wake-up capability is enabled.	RW	0
1	SOFTRESET	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. Read returns 0. 0x0: Normal mode 0x1: The module is reset.	RW	0
0	AUTOIDLE	Internal OCP clock gating strategy 0x0: Clock is running. 0x1: Automatic OCP clock gating strategy is applied, based on OCP interface activity	RW	0

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Table 23-243. Register Call Summary for Register UART_SYSC

UART/IrDA/CIR

- Clock Configuration: [0]
- Software Reset: [1]
- System Power Saving: [2]
- Local Power Management: [3] [4] [5]
- Registers Available for the Register Access Modes: [6] [7] [8] [9] [10] [11]
- Registers Available for the UART Function: [12] [13] [14] [15] [16] [17]
- Registers Available for the IrDA Function (UART3 Only): [18] [19] [20] [21] [22] [23]
- Registers Available for the CIR Function (UART3 Only): [24] [25] [26] [27] [28] [29]
- Software Reset: [30]
- UART/IrDA/CIR Register Summary: [31] [32] [33]

Table 23-244. UART_SYSS

Address Offset	0x0000 0058		
Physical Address	0x4806 A058 0x4806 C058 0x4802 0058 0x4806 E058 0x4806 6058 0x4806 8058	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	System status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RESERVED							RESETDONE

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:1	RESERVED	Read returns 0.	R	0x00
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is ongoing. Read 0x1: Reset complete	R	0

Table 23-245. Register Call Summary for Register UART_SYSS

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2]
- Registers Available for the UART Function: [3] [4] [5]
- Registers Available for the IrDA Function (UART3 Only): [6] [7] [8]
- Registers Available for the CIR Function (UART3 Only): [9] [10] [11]
- Software Reset: [12]
- UART/IrDA/CIR Register Summary: [13] [14] [15]

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Table 23-246. UART_WER

Address Offset	0x0000 005C		
Physical Address	0x4806 A05C	**Instance**	UART1
	0x4806 C05C		UART2
	0x4802 005C		UART3
	0x4806 E05C		UART4
	0x4806 605C		UART5
	0x4806 805C		UART6
Description	Wake-up enable register		
	The UART wake-up enable register is used to mask and unmask a UART event that would subsequently notify the system. An event is any activity in the logic that could cause an interrupt and/or an activity that would require the system to wake up. Even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, the UART registers the interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TX_WAKEUP_EN	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	EVENT_5_RHR_INTERRUPT	EVENT_4_RX_ACTIVITY	EVENT_3_DCD_CD_ACTIVITY	EVENT_2_RI_ACTIVITY	EVENT_1_DSR_ACTIVITY	EVENT_0_CTS_ACTIVITY	

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x000000
7	TX_WAKEUP_EN	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system: it can be THR_IT or TX_DMA request and/or TX_SATUS_IT.	RW	0
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1
5	EVENT_5_RHR_INTERRUPT	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1
4	EVENT_4_RX_ACTIVITY	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1
3	EVENT_3_DCD_CD_ACTIVITY	0x0: Event is not allowed to wake up the system 0x1: Event can wake up the system	RW	1
2	EVENT_2_RI_ACTIVITY	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1
1	EVENT_1_DSR_ACTIVITY	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1
0	EVENT_0_CTS_ACTIVITY	0x0: Event is not allowed to wake up the system. 0x1: Event can wake up the system.	RW	1

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Table 23-247. Register Call Summary for Register UART_WER

UART/IrDA/CIR

- System Power Saving: [0]
- Registers Available for the Register Access Modes: [1] [2] [3] [4] [5] [6]
- Registers Available for the UART Function: [7] [8] [9] [10] [11] [12]
- Registers Available for the IrDA Function (UART3 Only): [13] [14] [15] [16] [17] [18]
- Registers Available for the CIR Function (UART3 Only): [19] [20] [21] [22] [23] [24]
- UART/IrDA/CIR Register Summary: [25] [26] [27]

Table 23-248. UART_CFPS

Address Offset	0x0000 0060		
Physical Address	0x4806 A060 0x4806 C060 0x4802 0060 0x4806 E060 0x4806 6060 0x4806 8060	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Carrier frequency prescaler Because the consumer IR works at modulation rates of 30 to 56.8 kHz, the 48-MHz clock must be prescaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote-control requirements in baud multiples of 12x. The value of the CFPS at reset is 0105 decimal, which equals 38.1 kHz output from starting conditions. The 48-MHz carrier is prescaled by the CFPS, which is then divided by the 12x baud multiple.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CFPS							

Bits	Field Name	Description			Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.			RW	0x000000
7:0	CFPS	System clock frequency prescaler at (12x multiple). Examples for CFPS values:			RW	0x69
		Target Freq (kHz)	**CFPS (decimal)**	**Actual Freq (kHz)**		
		30	133	30.08		
		32.75	122	32.79		
		36	111	36.04		
		36.7	109	36.69		
		38*	105	38.1		
		40	100	40		
		56.8	70	57.14		
		*configured at reset to this value				
		Note: CFPS = 0 is not supported.				

Table 23-249. Register Call Summary for Register UART_CFPS

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2] [3] [4] [5]
- Registers Available for the CIR Function (UART3 Only): [6] [7] [8] [9] [10] [11]
- CIR Mode Clock Generation: [12] [13] [14]
- UART/IrDA/CIR Register Summary: [15] [16] [17]

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Table 23-250. UART_RXFIFO_LVL

Address Offset	0x0000 0064		
Physical Address	0x4806 A064 0x4806 C064 0x4802 0064 0x4806 E064 0x4806 6064 0x4806 8064	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Level of the RX FIFO		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RXFIFO_LVL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:0	RXFIFO_LVL	Shows the number of received bytes in the RX FIFO	R	0x00

Table 23-251. Register Call Summary for Register UART_RXFIFO_LVL

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2] [3] [4] [5]
- Registers Available for the UART Function: [6] [7] [8] [9] [10] [11]
- Registers Available for the IrDA Function (UART3 Only): [12] [13] [14] [15] [16] [17]
- Registers Available for the CIR Function (UART3 Only): [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25] [26]

Table 23-252. UART_TXFIFO_LVL

Address Offset	0x0000 0068		
Physical Address	0x4806 A068 0x4806 C068 0x4802 0068 0x4806 E068 0x4806 6068 0x4806 8068	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Level of the TX FIFO		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TXFIFO_LVL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0.	R	0x000000
7:0	TXFIFO_LVL	Shows the number of written bytes in the TX FIFO	R	0x00

Table 23-253. Register Call Summary for Register UART_TXFIFO_LVL

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2] [3] [4] [5]
- Registers Available for the UART Function: [6] [7] [8] [9] [10] [11]
- Registers Available for the IrDA Function (UART3 Only): [12] [13] [14] [15] [16] [17]
- Registers Available for the CIR Function (UART3 Only): [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25] [26]

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Table 23-254. UART_IER2

Address Offset	0x0000 006C		
Physical Address	0x4806 A06C 0x4806 C06C 0x4802 006C 0x4806 E06C 0x4806 606C 0x4806 806C	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Enables RX/TX FIFOs empty corresponding interrupts		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														EN_TXFIFO_EMPTY	EN_RXFIFO_EMPTY

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Read returns 0. Write has no effect.	RW	0x0000 0000
1	EN_TXFIFO_EMPTY	Enables TX FIFO empty corresponding interrupt 0x0: Enables EN_TXFIFO_EMPTY interrupt 0x1: Disables EN_TXFIFO_EMPTY interrupt	RW	0
0	EN_RXFIFO_EMPTY	Enables RX FIFO empty corresponding interrupt 0x0: Enables EN_RXFIFO_EMPTY interrupt 0x1: Disables EN_RXFIFO_EMPTY interrupt	RW	0

Table 23-255. Register Call Summary for Register UART_IER2

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2] [3] [4] [5]
- Registers Available for the UART Function: [6] [7] [8] [9] [10] [11]
- Registers Available for the IrDA Function (UART3 Only): [12] [13] [14] [15] [16] [17]
- Registers Available for the CIR Function (UART3 Only): [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25] [26]

Table 23-256. UART_ISR2

Address Offset	0x0000 0070		
Physical Address	0x4806 A070 0x4806 C070 0x4802 0070 0x4806 E070 0x4806 6070 0x4806 8070	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Status of RX/TX FIFOs empty corresponding interrupts		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TXFIFO_EMPTY_STS	RXFIFO_EMPTY_STS

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Read returns 0. Write has no effect.	RW	0x0000 0000
1	TXFIFO_EMPTY_STS	Used to generate interrupt if the TX_FIFO is empty (software flow control) 0x0: TXFIFO_EMPTY interrupt not pending. 0x1: TXFIFO_EMPTY interrupt pending.	RW	1
0	RXFIFO_EMPTY_STS	Used to generate interrupt if the RX_FIFO is empty (software flow control) 0x0: RXFIFO_EMPTY interrupt not pending. 0x1: RXFIFO_EMPTY interrupt pending.	RW	1

Table 23-257. Register Call Summary for Register UART_ISR2

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2] [3] [4] [5]
- Registers Available for the UART Function: [6] [7] [8] [9] [10] [11]
- Registers Available for the IrDA Function (UART3 Only): [12] [13] [14] [15] [16] [17]
- Registers Available for the CIR Function (UART3 Only): [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25] [26]

Table 23-258. UART_FREQ_SEL

Address Offset	0x0000 0074		
Physical Address	0x4806 A074 0x4806 C074 0x4802 0074 0x4806 E074 0x4806 6074 0x4806 8074	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Sample per bit selector		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FREQ_SEL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Read returns 0. Write has no effect.	RW	0x0000 0000
7:0	FREQ_SEL	Sets the sample per bit if nondefault frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal to or higher then 6.	RW	0x1A

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Table 23-259. Register Call Summary for Register UART_FREQ_SEL

UART/IrDA/CIR

- Registers Available for the Register Access Modes: [0] [1] [2] [3] [4] [5]
- Registers Available for the UART Function: [6] [7] [8] [9] [10] [11]
- Registers Available for the IrDA Function (UART3 Only): [12] [13] [14] [15] [16] [17]
- Registers Available for the CIR Function (UART3 Only): [18] [19] [20] [21] [22] [23]
- UART/IrDA/CIR Register Summary: [24] [25] [26]

Table 23-260. UART_MDR3

Address Offset	0x0000 0080		
Physical Address	0x4806 A080 0x4806 C080 0x4802 0080 0x4806 E080 0x4806 6080 0x4806 8080	**Instance**	UART1 UART2 UART3 UART4 UART5 UART6
Description	Mode definition register 3		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													SET_DMA_TX_THRESHOLD	NONDEFAULT_FREQ	DISABLE_CIR_RX_DEMOD

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Read returns 0. Write has no effect.	RW	0x0000 0000
2	SET_DMA_TX_THRESHOLD	Enable to set different TXDMA threshold in UART_TX_DMA_THRESHOLD register.	RW	0
1	NONDEFAULT_FREQ	Used to enable the NONDEFAULT fclk frequencies. 0x0: Disables using NONDEFAULT fclk frequencies. 0x1: Enables using NONDEFAULT fclk frequencies (set FREQ_SEL and DLH/DLL).	RW	0
0	DISABLE_CIR_RX_DEMOD	Used to enable CIR RX demodulation. 0x0: Enables CIR RX demodulation. 0x1: Disables CIR RX demodulation.	RW	0

Table 23-261. Register Call Summary for Register UART_MDR3

UART/IrDA/CIR

- FIFO DMA Mode Operation: [0]
- DMA Transfers (DMA Mode 1, 2, or 3): [1] [2]
- Registers Available for the Register Access Modes: [3] [4] [5] [6] [7] [8]
- Registers Available for the UART Function: [9] [10] [11] [12] [13] [14]
- Registers Available for the IrDA Function (UART3 Only): [15] [16] [17] [18] [19] [20]
- Registers Available for the CIR Function (UART3 Only): [21] [22] [23] [24] [25] [26]
- UART/IrDA/CIR Register Summary: [27] [28] [29]
- UART/IrDA/CIR Register Description: [30]

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Table 23-262. UART_TX_DMA_THRESHOLD

Address Offset	0x0000 0084		
Physical Address	0x4806 A084	**Instance**	UART1
	0x4806 C084		UART2
	0x4802 0084		UART3
	0x4806 E084		UART4
	0x4806 6084		UART5
	0x4806 8084		UART6
Description	Use to manually set the TX DMA threshold level. UART_MDR3[2] SET_TX_DMA_THRESHOLD must be 1 and must be value + tx_trigger_level = 64 (TX FIFO size). If not, 64-tx_trigger_level will be used without modifying the value of this register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TX_DMA_THRESHOLD							

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	RW	0x0000000
5:0	TX_DMA_THRESHOLD	Used to manually set the TX DMA threshold level	RW	0x00

Table 23-263. Register Call Summary for Register UART_TX_DMA_THRESHOLD

UART/IrDA/CIR

- FIFO DMA Mode Operation: [0]
- DMA Transfers (DMA Mode 1, 2, or 3): [1] [2]
- Registers Available for the Register Access Modes: [3] [4] [5] [6] [7] [8]
- Registers Available for the UART Function: [9] [10] [11] [12] [13] [14]
- Registers Available for the IrDA Function (UART3 Only): [15] [16] [17] [18] [19] [20]
- Registers Available for the CIR Function (UART3 Only): [21] [22] [23] [24] [25] [26]
- UART/IrDA/CIR Register Summary: [27] [28] [29]
- UART/IrDA/CIR Register Description: [30]

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23.4 Multichannel Serial Port Interface

This section describes the four multichannel serial port interface (MCSPI) modules for the device.

23.4.1 MCSPI Overview

The MCSPI is a master/slave synchronous serial bus. The MCSPI has four separate modules (SPI1, SPI2, SPI3, and SPI4) in the device (see Figure 23-75). The MCSPI modules differ as follows: SPI1 supports up to four peripherals and master mode only, SPI2 supports up to two peripherals and master mode only, SPI3 and SPI4 supports only one peripheral and master and slave mode.

NOTE: In this chapter, *m = [1,4]* represents the module instance and *x* represents the channel in signal and register naming. The MCSPI has four instances, with each module instance having different channel numbers:

- SPI1: 4 channels (if *m = 1*, *x = 4*)
- SPI2: 2 channels (if *m = 2*, *x = 2*)
- SPI3: 1 channel (if *m = 3*, *x = 1*)
- SPI4: 1 channel (if *m = 4*, *x = 1*)

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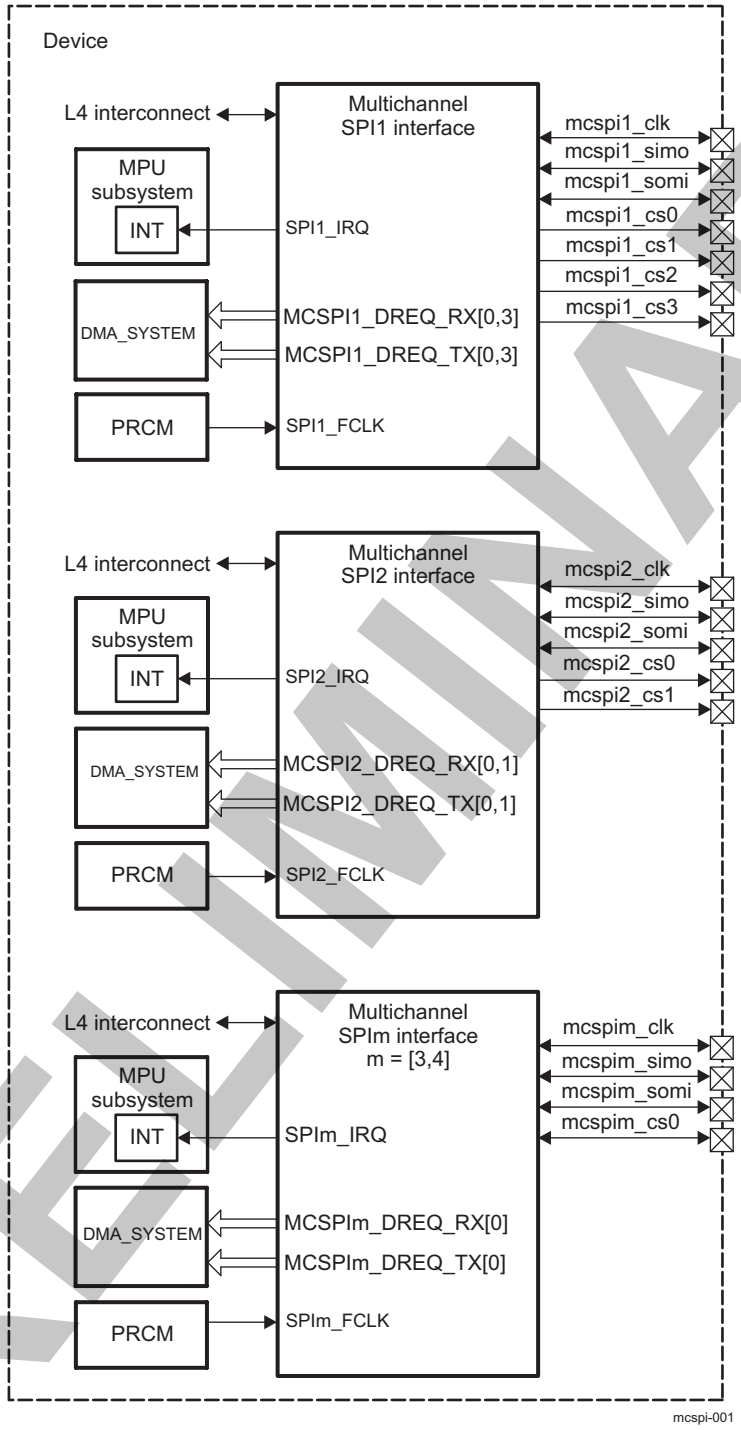
Figure 23-75. Multichannel Modules SPI1, SPI2, SPI3, and SPI4



The MCSPI instances include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes

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  - Flexible input/output (I/O) port controls per channel
  - Two direct memory access (DMA) requests (read/write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- 64-byte built-in FIFO available for a single channel
- Force CS mode for continuous transfers

23.4.2 MCSPI Environment

Figure 23-76 shows a simplified overview of a typical application system using the MCSPI. This example is based on a TFS chipset, including a 2.2-inch color-active matrix thin-film transistor (TFT) liquid crystal display (LCD) with a light-emitting diode (LED) front light, a 4-wire resistive touch-screen panel, and LCD controllers. This chipset is associated with a touch-screen controller, powered by a power-management unit, and driven by the device. The MCSPI device interface is set to master mode; the touch-screen MCSPI controller interface operates in slave mode.

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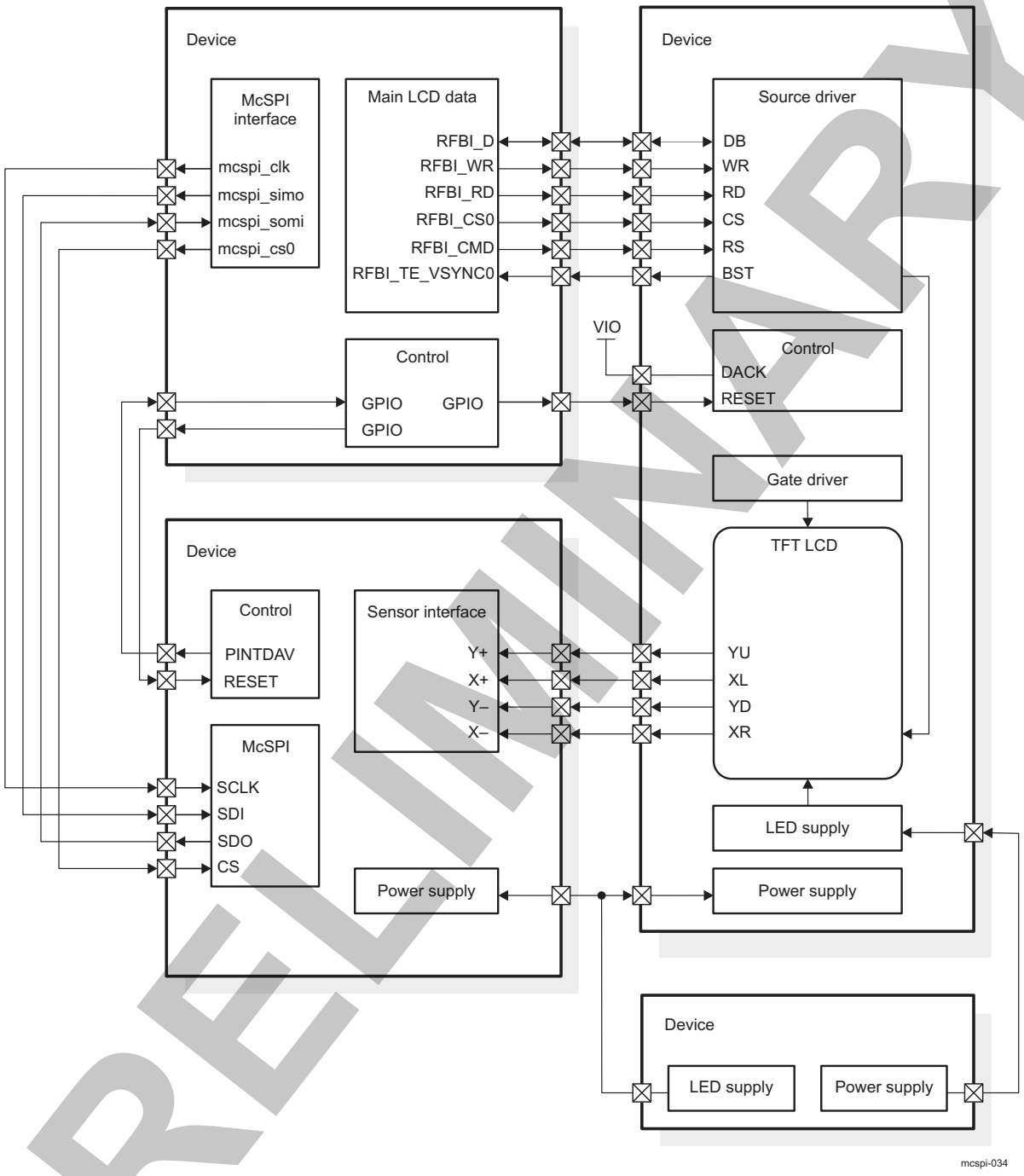
Figure 23-76. Typical Application Using the MCSPI



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23.4.2.1 MCSPI Interface

23.4.2.1.1 Basic MCSPI Pins for Master Mode

Figure 23-77 shows all of the MCSPI interface signals in master mode.

Figure 23-77. MCSPI Interface Signals in Master Mode

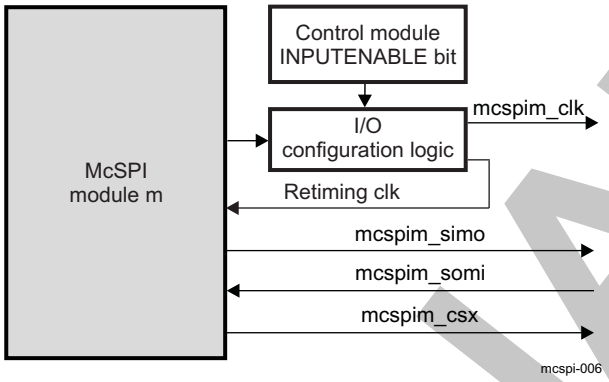

Table 23-264 describes the MCSPI I/O in master mode.

Table 23-264. MCSPI I/O Description (Master Mode)

Signal Name	I/O[1]	Description	Reset [2]
mcspim_clk	O	SPIm module serial clock[3]	Unknown
mcspim_simo	O	SPIm module serial data master out (slave input, master output)	Unknown
mcspim_somi	I	SPIm module serial data master input (slave output, master input)	–
mcspim_csx	O	SPIm module chip-select x output	Low

(1) I = Input; O = Output

(2) After reset, the SPI modules are in slave mode by default. This paragraph implies that the MCSPI module is configured in slave mode. (See the MCSPI_MODULCTRL[2] MS bit in the module control register [MCSPI_MODULCTRL].)

(3) This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

23.4.2.1.2 Basic MCSPI Pins for Slave Mode

Figure 23-78 shows all of the MCSPI interface signals in slave mode.

Figure 23-78. MCSPI Interface Signals in Slave Mode

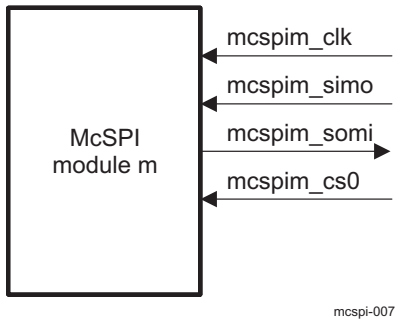

Table 23-265 describes the MCSPI I/O in slave mode.

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Table 23-265. MCSPI I/O Description (Slave Mode)

Signal Name	I/O[1]	Description	Reset [2]
mcspim_clk	I	SPIm module serial clock	Unknown
mcspim_simo	I	SPIm module serial data master out (slave input, master output)	Unknown
mcspim_somi	O	SPIm module serial data master input (slave output, master input)	–
mcspim_csx	I	SPIm module chip-select x output	Low

(1) I = Input; O = Output

(2) After reset, the SPI modules are in slave mode by default. This paragraph implies that the MCSPI module is configured in slave mode. (See the MCSPI_MODULCTRL[2] MS bit in the module control register [MCSPI_MODULCTRL].)

23.4.2.1.3 Multichannel SPI Protocol and Data Format

The synchronous SPI protocol allows a master device to initiate serial data transfers to a slave device. A slave select line (mcspim_csx) allows selection of an individual slave SPI device. Slave devices that are not selected do not interfere with SPI bus activities.

MCSPI offers the flexibility to modify the following parameters to adapt to the device features:

- Word length

  MCSPI supports any SPI word ranging from 4 bits to 32 bits long (the SPIm.MCSPI_CHxCONF[11:7] WL bit field).

  SPI word length can be changed between transmissions to allow the master device to communicate with peripheral slaves that have different requirements.

- SPI enable (mcspim_csx, for channel x of instance m)

  The polarity of the SPI enable signals is programmable (the SPIm.MCSPI_CHxCONF[6] EPOL bit). mcspim_csx signals can be active high or low.

  Assertion of the mcspim_csx signals is programmable and can be done manually or automatically. The manual assertion mode is available in single master mode only. mcspim_csx can be kept active between words with the SPIm.MCSPI_CHxCONF[20] FORCE bit.

  Two consecutive words for two different slave devices can go along with active mcspim_csx signals with different polarity.

- Programmable start-bit

  In start-bit mode a start-bit is added before the SPI word length to indicate how the next SPI word must be handled. The start-bit is enabled by setting the SPIm.MCSPI_CHxCONF[23] SBE bit to 1. The SPIm.MCSPI_CHxCONF[24] SBPOL bit defines the polarity of the start-bit.

- Programmable SPI clock
  - Bit rate

    In master mode, the baud rate of the SPI serial clock is programmable using the 48-MHz reference clock (from the power, reset, and clock managment [PRCM] module). Table 23-266 lists the spim_clk bit rates obtained for data transfer when programming the clock divider (the SPIm.MCSPI_CHxCONF[5:2] CLKD bit field).

Table 23-266. SPI Master Clock Rates

Divider	Clock Rate
1	48 MHz
2	24 MHz
4	12 MHz
8	6 MHz
16	3 MHz
32	1.5 MHz
64	750 kHz
128	375 kHz

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Table 23-266. SPI Master Clock Rates (continued)

Divider	Clock Rate
256	~187 kHz
512	~93.7 kHz
1024	~46.8 kHz
2048	~23.4 kHz
4096	~11.7 kHz

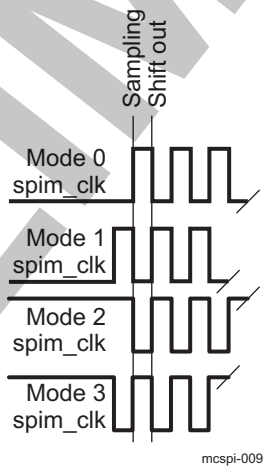
– Polarity and phase

The polarity (the SPIm.MCSPI_CHxCONF[1] POL bit) and the phase (the SPIm.MCSPI_CHxCONF[0] PHA bit) of the SPI serial clock (mcspim_clk) are configurable to offer four combinations. Software selects the right combination, depending on the device. See Table 23-267 and Figure 23-79.

Table 23-267. Phase and Polarity Combinations

Polarity (POL)	Phase (PHA)	SPI Mode	Comments
0	0	Mode 0	mcspim_clk is active high and sampling occurs on the rising edge.
0	1	Mode 1	mcspim_clk is active high and sampling occurs on the falling edge.
1	0	Mode 2	mcspim_clk is active low and sampling occurs on the falling edge.
1	1	Mode 3	mcspim_clk is active low and sampling occurs on the rising edge.

Figure 23-79. Phase and Polarity Combinations



23.4.2.1.3.1 Transfer Format

In master and slave modes, the MCSPI drives the data lines when spim_csx is asserted.

Each word is transmitted starting with the most-significant bit (MSB).

This section explains the two cases of data transmission determined by the clock phase (PHA) and the type of data transmission using a start-bit (SBE) called the start-bit mode:

- Transmission in mode 0 and mode 2 (PHA = 0)

  When PHA = 0, the first bit of the SPI word to transmit (on the master or the slave data output pin) is valid one-half cycle of spim_clk after the assertion of spim_csx.

  Therefore, the first edge of the mcspim_clk line is used by the master to sample the first data bit sent by the slave. On the same edge, the first data bit sent by the master is sampled by the slave.

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On the next mcspim_clk edge, the received data bit is shifted into the receive shift register and a new data bit is transmitted on the serial data line.

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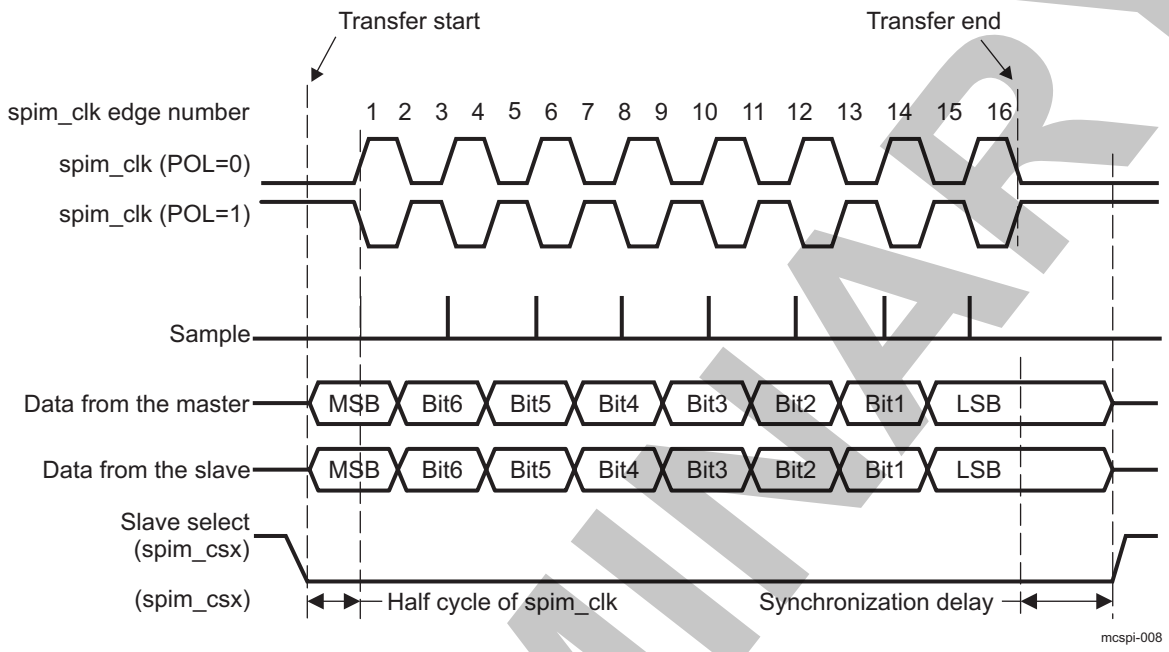
This process continues for a number of pulses on the spim_clk line defined by the SPI word length programmed in the master device, with data being latched on odd-numbered edges and shifted on even-numbered edges. See Figure 23-80.

Figure 23-80. Full-Duplex Transfer Format With PHA = 0



- Transmission in mode 1 and mode 3 (PHA = 1)

  When PHA = 1, the first bit of the SPI word to transmit (on the master or the slave data output pin) is valid on the following mcspim_clk edge (one-half cycle later). This is the sampling edge for the master and slave. A synchronization delay is added between the activation of mcspim_csx and the first mcspim_clk edge.

  The received data bit is shifted into the shift register on the third mcspim_clk edge.

  This process continues for a number of pulses on the mcspim_clk line defined by the SPI word length programmed in the master device, with data being latched on even-numbered edges and shifted on odd-numbered edges.

  NOTE: The minimum synchronization delay is one cycle of mcspim_clk, if the frequency of mcspim_clk equals the frequency of SPIm_FCLK (MCSPIm functional clock) in master mode. The minimum synchronization delay is one-half cycle of mcspim_clk, if the frequency of mcspim_clk is lower than the frequency of SPIm_FCLK in the master and slave modes.

- Transmission with a start-bit (SBE = 1)

  When the SPIm.MCSPI_CHxCONF[23] SBE bit is set to 1, a start-bit is added before the MSB to indicate whether the next SPI word must be handled as a command or as data.

  Figure 23-81 shows an example of a data transfer with an extra start-bit.

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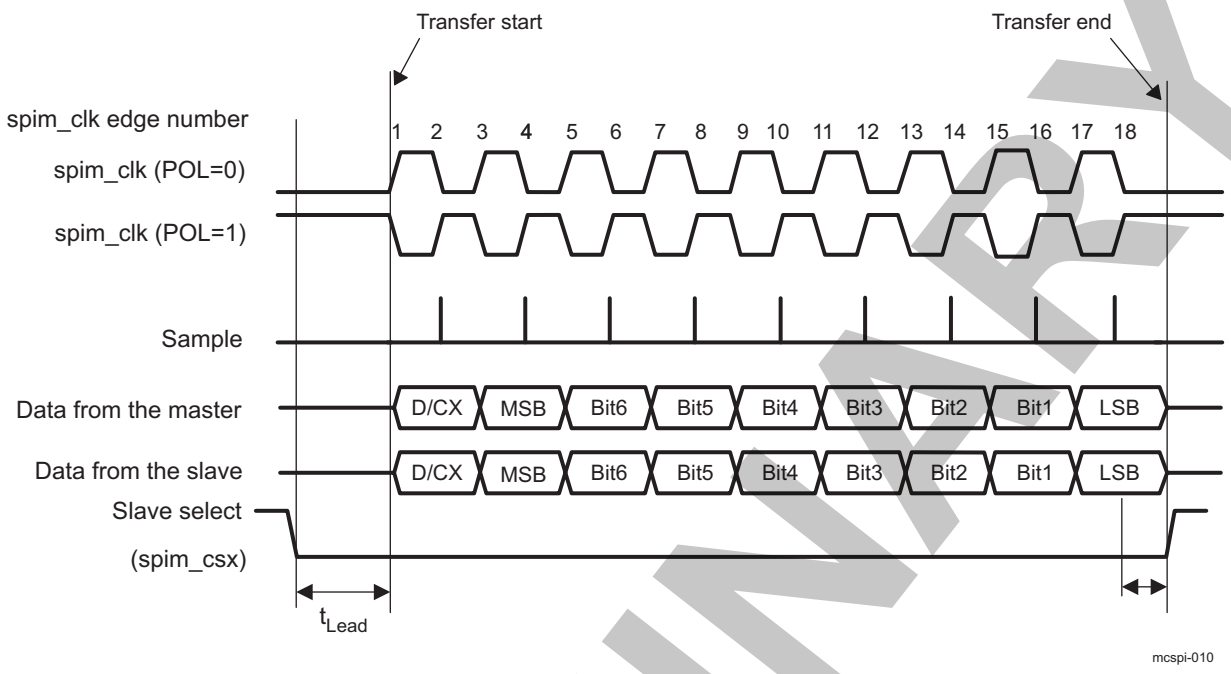
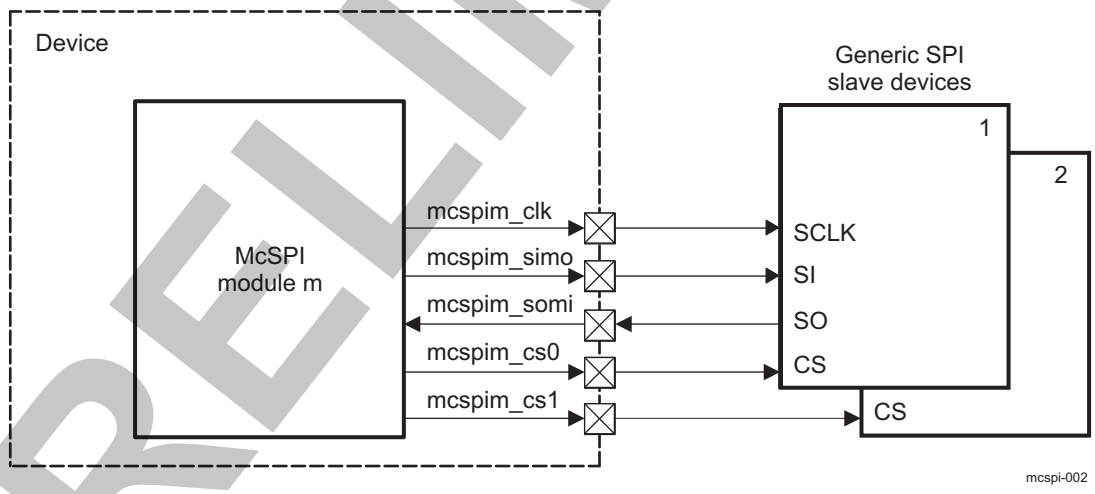
Figure 23-81. Extended SPI Transfer With a Start-Bit (SBE = 1)



23.4.2.2 SPI in Master Mode

Figure 23-82 shows a case in master mode (full-duplex) where the MCSPI module is connected with two slave devices.

Figure 23-82. MCSPI Master Mode (Full Duplex)



NOTE: In this case m = [1,3].

Figure 23-83 shows the master single mode, which can also be configured in receive-only mode.

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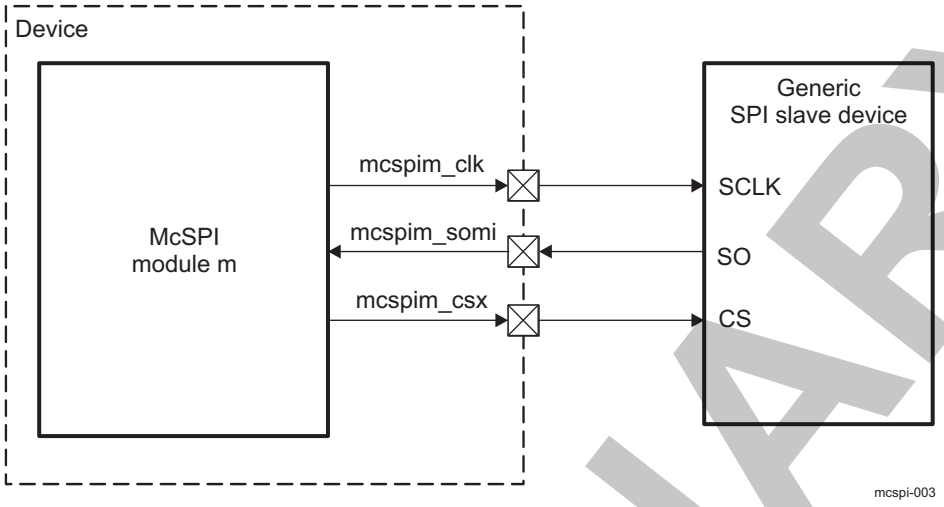
Figure 23-83. MCSPI Master Single Mode (Receive Only)



23.4.2.3 SPI in Slave Mode

Figure 23-84 shows a case in slave mode (full-duplex).

NOTE: Only channel 0 can be configured as slave, but the chip-enable signal can be connected to any mcspim_csx pin and then rerouted internally to channel 0 (the SPIm.MCSPI_CHxCONF[22:21] SPIENSLV bit field [where x = 0]). For more information, see Section 23.4.4.3, *Slave Mode*.

Figure 23-84. MCSPI Slave Mode (Full Duplex)

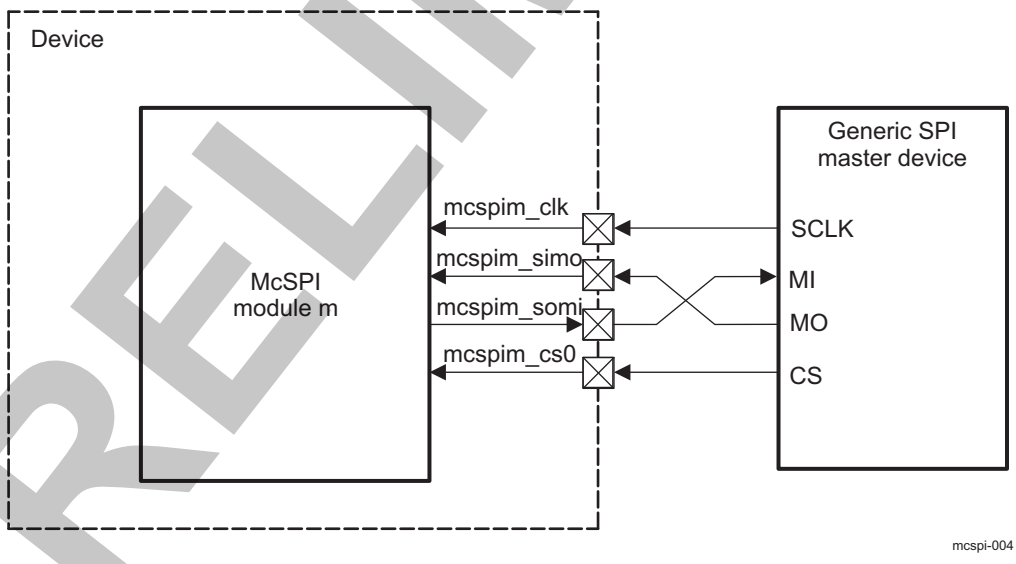


Figure 23-85 shows the slave single mode, which can also be configured in transmit-only mode.

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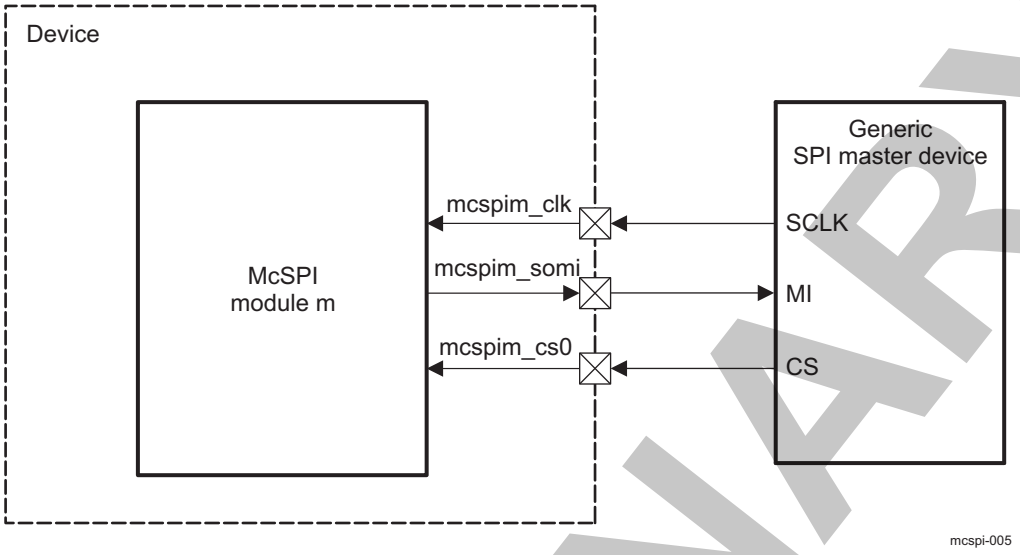
Figure 23-85. MCSPI Slave Single Mode (Transmit Only)

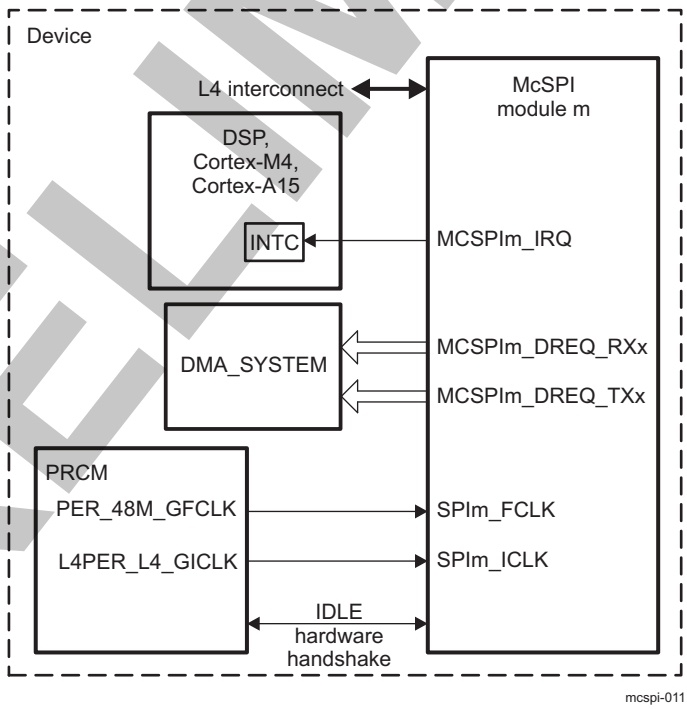


23.4.3 MCSPI Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-86 shows MCSPI integration.

Figure 23-86. MCSPI Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1 Device Power-Management Architecture Building Blocks in Chapter PRCM.

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NOTE: For the names of the signals going from the MCSPI to the DSP, Cortex-M4, and Cortex-A15 interrupt controllers (INTCs), see Section 17.1.

Table 23-268 through Table 23-270 summarize the integration of the module in the device.

Table 23-268. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
MCSPI1	PD_CORE	L4_PER
MCSPI2	PD_CORE	L4_PER
MCSPI3	PD_CORE	L4_PER
MCSPI4	PD_CORE	L4_PER

Table 23-269. Clocks

	Clocks			
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MCSPI1	SPI1_ICLK	L4PER_L4_GICLK	PRCM	Interface clock
	SPI1_FCLK	PER_48M_GFCLK	PRCM	Functional clock
MCSPI2	SPI2_ICLK	L4PER_L4_GICLK	PRCM	Interface clock
	SPI2_FCLK	PER_48M_GFCLK	PRCM	Functional clock
MCSPI3	SPI3_ICLK	L4PER_L4_GICLK	PRCM	Interface clock
	SPI3_FCLK	PER_48M_GFCLK	PRCM	Functional clock
MCSPI4	SPI4_ICLK	L4PER_L4_GICLK	PRCM	Interface clock
	SPI4_FCLK	PER_48M_GFCLK	PRCM	Functional clock

Table 23-270. Hardware Requests

	Interrupt Requests			
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MCSPI1	MCSPI1_IRQ	DSP_IRQ_87	DSP INTC	Interrupt request to the DSP INTC
	MCSPI1_IRQ	MPU_IRQ_65	Cortex-A15 INTC	Interrupt request to the Cortex-A15 INTC
	MCSPI1_IRQ	IPU_IRQ_57	Cortex-M4 INTC	Interrupt request to the Cortex-M4 INTC
MCSPI2	MCSPI2_IRQ	MPU_IRQ_66	Cortex-A15 INTC	Interrupt request to the Cortex-A15 INTC
	MCSPI2_IRQ	IPU_IRQ_58	Cortex-M4 INTC	Interrupt request to the Cortex-M4 INTC
MCSPI3	MCSPI3_IRQ	MPU_IRQ_91	Cortex-A15 INTC	Interrupt request to the Cortex-A15 INTC
MCSPI4	MCSPI4_IRQ	MPU_IRQ_48	Cortex-A15 INTC	Interrupt request to the Cortex-A15 INTC
	DMA_SYSTEM Requests			
MCSPI1	MCSPI1_DREQ_TX0	DMA_SYSTEM_DREQ_34	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI1_DREQ_RX0	DMA_SYSTEM_DREQ_35	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI1_DREQ_TX1	DMA_SYSTEM_DREQ_36	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI1_DREQ_RX1	DMA_SYSTEM_DREQ_37	DMA_SYSTEM	Destination is DMA_SYSTEM

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Table 23-270. Hardware Requests (continued)

	MCSPI1_DREQ_TX2	DMA_SYSTEM_DREQ_38	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI1_DREQ_RX2	DMA_SYSTEM_DREQ_39	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI1_DREQ_TX3	DMA_SYSTEM_DREQ_40	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI1_DREQ_RX3	DMA_SYSTEM_DREQ_41	DMA_SYSTEM	Destination is DMA_SYSTEM
MCSPI2	MCSPI2_DREQ_TX0	DMA_SYSTEM_DREQ_42	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI2_DREQ_RX0	DMA_SYSTEM_DREQ_43	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI2_DREQ_TX1	DMA_SYSTEM_DREQ_44	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI2_DREQ_RX1	DMA_SYSTEM_DREQ_45	DMA_SYSTEM	Destination is DMA_SYSTEM
MCSPI3	MCSPI3_DREQ_TX0	DMA_SYSTEM_DREQ_14	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI3_DREQ_RX0	DMA_SYSTEM_DREQ_15	DMA_SYSTEM	Destination is DMA_SYSTEM
MCSPI4	MCSPI4_DREQ_TX0	DMA_SYSTEM_DREQ_69	DMA_SYSTEM	Destination is DMA_SYSTEM
	MCSPI4_DREQ_RX0	DMA_SYSTEM_DREQ_70	DMA_SYSTEM	Destination is DMA_SYSTEM

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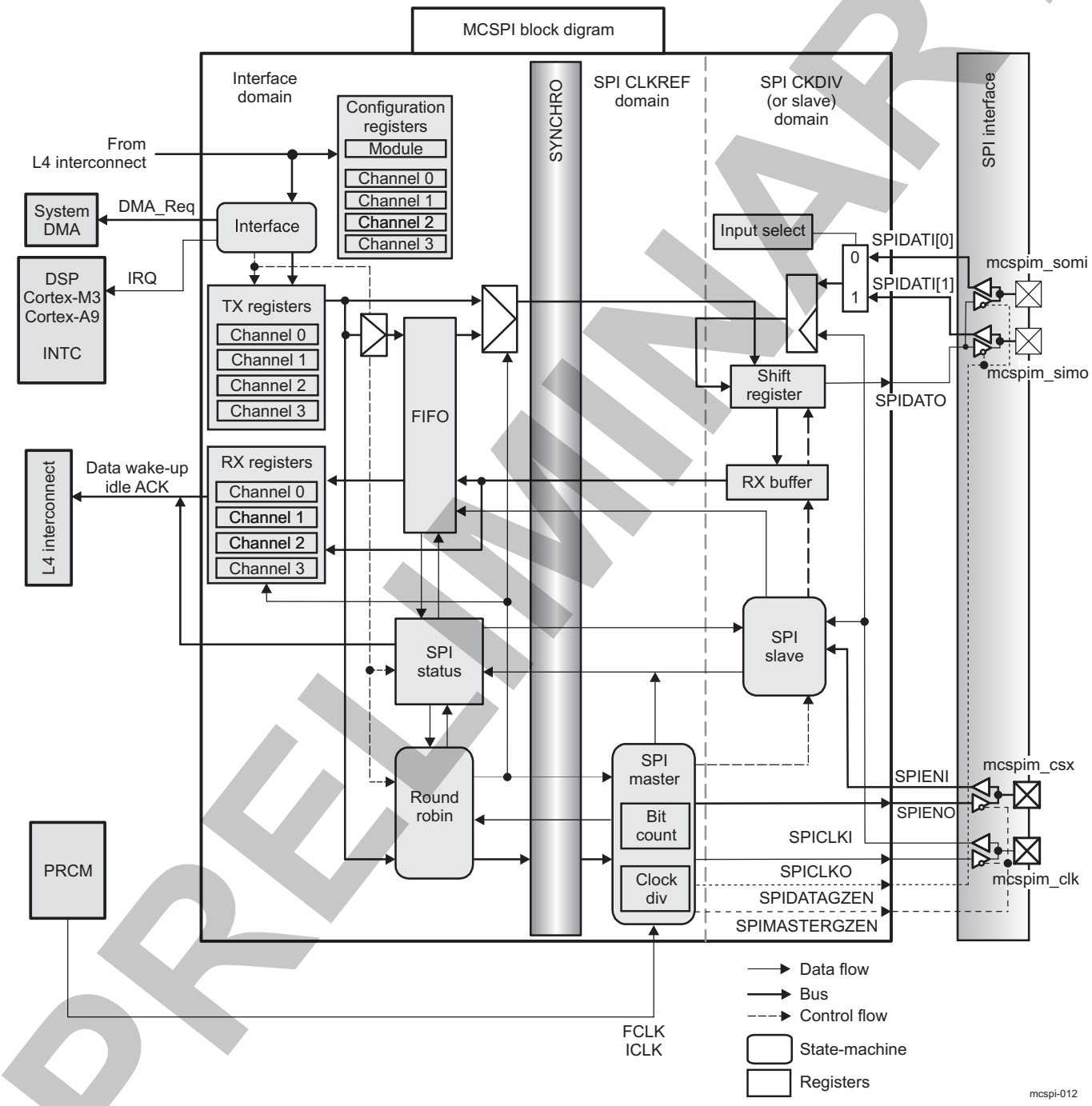
23.4.4 MCSPI Functional Description

23.4.4.1 MCSPI Block Diagram

Figure 23-87 shows the MCSPI module.

Figure 23-87. MCSPI Block Diagram



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23.4.4.2 Master Mode

23.4.4.2.1 Master Mode Features

The MCSPI master mode supports multichannel communication with up to four independent SPI communication channel contexts. The MCSPI initiates a data transfer on the data lines (mcspim_simo and mcspim_somi) and generates clock (mcspim_clk) and control (mcspim_csx) signals.

Connected to multiple external devices, the MCSPI exchanges data with one SPI device at a time through two main modes (available in slave mode):

- Two-data-pins interface mode (transmit-and-receive mode for full-duplex transmission)
- Single-data-pin interface mode (recommended for half-duplex transmission)

Two DMA request events (read and write) allow synchronized accesses of the DMA controller with the activity of MCSPI.

Three interrupt events can be used for data transmission and reception in master mode (for more information about interrupts, see Section 23.4.4.5.1, *Interrupt Events in Master Mode*).

23.4.4.2.2 Master Transmit-and-Receive Mode (Full Duplex)

In full-duplex transmission, data is transmitted (shifted out serially on mcspim_simo) and received (shifted in serially on mcspim_somi) simultaneously on separate data lines.

The master transmit-and-receive mode is programmable per channel (the SPIm.MCSPI_CHxCONF[13:12] TRM bit field).

Channel access to the shift registers for transmission/reception is based on the MCSPI_TXx transmitter register state, the MCSPI_RXx receiver register state, and round-robin arbitration.

Channels that meet the following rules are included in the round-robin list of active channels scheduled for transmission and/or reception. The arbiter skips channels that do not meet the rules and searches in the rotation for the next enabled channel.

- Rule 1: Only enabled channels (the SPIm.MCSPI_CHxCTRL[0] EN bit) can be scheduled for transmission and/or reception.
- Rule 2: If its MCSPI_TXx transmitter register is not empty (the SPIm.MCSPI_CHxSTAT[1] TXS bit), an enabled channel can be scheduled when the shift register is assigned. If the MCSPI_TXx register is empty when the shift register is assigned, the TXx_UNDERFLOW event is activated, and the next enabled channel with new data to transmit is scheduled (see also transmit-only mode).
- Rule 3: An enabled channel can be scheduled if its receive register is not full (the SPIm.MCSPI_CHxSTAT[0] RXS bit) when the shift register is assigned (see also receive-only mode). Therefore, the MCSPI_RXx register cannot be overwritten. The SPI1.MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set to this mode.

When SPI word transfer completes (the SPIm.MCSPI_CHxSTAT[2] EOT bit is set), the updated MCSPI_TXx register of the next scheduled channel is loaded into the shift register. The serialization (transmit-and-receive) starts depending on the channel communication configuration. When serialization completes, the received data transfers to the channel receive register.

The serial clock (mcspim_clk) synchronizes shifting and sampling of the information on the two serial data lines (mcspim_simo and mcspim_somi). Each time a bit transfers out from the master, 1 bit transfers in from the slave.

Figure 23-88 shows an example of a full-duplex system with a master device (MCSPI module *m*) on the left and a slave device on the right. After eight cycles of the serial clock mcspim_clk, WordA transfers from the master to the slave. At the same time, WordB transfers from the slave to the master.

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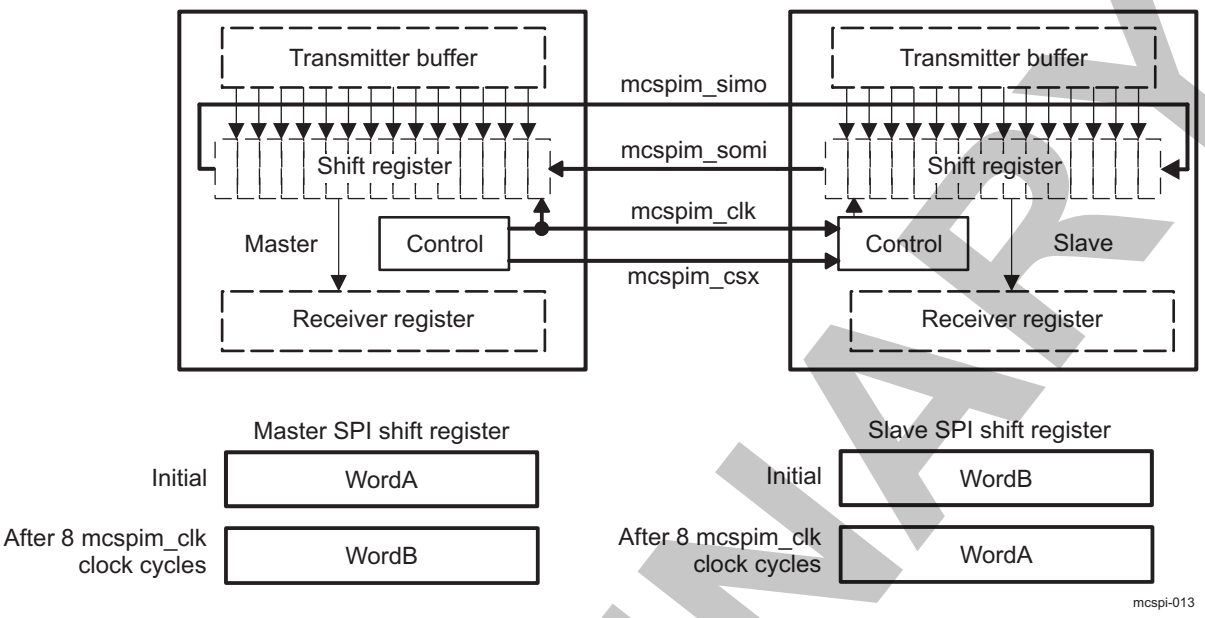
Figure 23-88. SPI Full-Duplex Transmission (Example)



23.4.4.2.3 Master Transmit-Only Mode (Half Duplex)

The master transmit-only mode prevents the microprocessor unit (MPU) from reading the MCSPI_RXx register (minimizing data movement) when only transmission is meaningful.

The master transmit-only mode is programmable per channel (the SPIm.MCSPI_CHxCONF[13:12] TRM bit field). Transmission starts only after data is loaded into the MCSPI_TXx register.

Rule 1 and Rule 2, defined in Section 23.4.4.2.2, apply in this mode.

Rule 3, defined in Section 23.4.4.2.2, does not apply.

In master transmit-only mode, the MCSPI_RXx register state FULL does not prevent transmission and the MCSPI_RXx register is always overwritten with the new SPI word. This event is not significant when only transmission is meaningful. Thus, the RX0_OVERFLOW bit in the SPIm.MCSPI_IRQSTATUS register is never set in this mode.

The hardware automatically disables the RX_FULL interrupt and the DMA read requests.

The transfer status is given by the SPIm.MCSPI_CHxSTAT[2] EOT bit.

23.4.4.2.4 Master Receive-Only Mode (Half Duplex)

The master receive mode prevents the MPU from refilling the MCSPI_TXx register (minimizing data movement) when only reception is meaningful.

The master receive mode is programmable per channel (the SPIm.MCSPI_CHxCONF[13:12] TRM bit field).

The master receive-only mode enables channel scheduling only on the empty state of the MCSPI_RXx register.

Rule 1 and Rule 3, defined in Section 23.4.4.2.2, apply in this mode.

Rule 2, defined in Section 23.4.4.2.2, does not apply.

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In the master receive-only mode, software must write dummy data to the MCSPI_TXx register. Only one dummy write is enough to receive any number of words from the slave. Software must ensure that the MCSPI_TXx register is always full (the TXx_EMPTY bits of SPIm.MCSPI_IRQSTATUS) when receiving. The content of the MCSPI_TXx register is always loaded into the shift register when the shift register is assigned. After writing the dummy data to the MCSPI_TXx register, the TXx_EMPTY and TXx_UNDERFLOW bits in the SPIm.MCSPI_IRQSTATUS register are never set in receive-only mode.

The SPIm.MCSPI_CHxSTAT[2] EOT bit gives the status of serialization. The RXx_FULL bits of the SPIm.MCSPI_IRQSTATUS register are set when received data is loaded from the shift register to the corresponding MCSPI_RXx register. The SPIm.MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

23.4.4.2.5 Single-Channel Master Mode

When the MCSPI is configured as a master device with a single enabled channel, the assertion of the mcspim_csx signal can be controlled in two different ways:

- If the MCSPI_MODULCTRL[0] SINGLE bit is set to 0, mcspim_csx assertion and deassertion after each SPI word is automatically controlled by the MCSPI (see the subsections of Section 23.4.4.2.1, *Master Mode Features*).
- If the MCSPI_MODULCTRL[0] SINGLE and MCSPI_CHxCONF[20] FORCE bits are set to 1, mcspim_csx assertion and deassertion is controlled by software (see Section 23.4.4.2.5.1, *Programming Tips When Switching to Another Channel*).

23.4.4.2.5.1 Programming Tips When Switching to Another Channel

When a single channel is enabled and data transfer is ongoing:

- Wait for the SPI word transfer to complete (wait until the SPIm.MCSPI_CHxSTAT[2] EOT bit is set to 1) before disabling the current channel and enabling a different channel.
- Disable the current channel, and then enable the other channel.

23.4.4.2.5.2 Force mcspim_csx Mode

Continuous transfers are allowed manually by keeping the mcspim_csx signal active for successive SPI words transfer. Several sequences (configuration/enable/disable of the channel) can be run without deactivating the mcspim_csx line. This mode is supported by all channels and any master sequence can be used (transmit-receive, transmit-only, receive-only).

Keeping the mcspim_csx active mode is supported when:

- A single channel is used (with the SPIm.MCSPI_MODULCTRL[0] SINGLE bit set to 1).
- Transfer parameters are loaded in the configuration register of the appropriate channel (SPIm.MCSPI_CHxCONF).

  The state of the mcspim_csx signal is programmable:

  – Writing 1 to the SPIm.MCSPI_CHxCONF[20] FORCE bit drives the mcspim_csx line high when the SPIm.MCSPI_CHxCONF[6] EPOL bit is set to 0. mcspim_csx is driven low when the SPIm.MCSPI_CHxCONF[6] EPOL bit is set to 1.

  – Writing 0 to the SPIm.MCSPI_CHxCONF[20] FORCE bit drives the mcspim_csx line low when the SPIm.MCSPI_CHxCONF[6] EPOL bit is set to 0. mcspim_csx is driven high when the SPIm.MCSPI_CHxCONF[6] EPOL bit is set to 1.
- A single channel is enabled (the SPIm.MCSPI_CHxCTRL[0] EN bit is set to 1). The first enabled channel activates the mcspim_csx line.

When the channel is enabled, the mcspim_csx signal activates with the programmed polarity. As in the multichannel master mode, the transfer start depends on the status of the MCSPI_TXx register (the SPIm.MCSPI_CHxSTAT[1] TXS bit), the status of the MCSPI_RXx register (the SPIm.MCSPI_CHxSTAT[1] RXS bit), and the defined mode (the SPIm.MCSPI_CHxCONF[13:12] TRM bit field) of the channel enabled.

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The SPIm.MCSPI_CHxSTAT[2] EOT bit gives the transfer status of each SPI word. The RXx_FULL bit in the SPIm.MCSPI_IRQSTATUS register is set when received data is loaded from the shift register to the MCSPI_RXx register.

A change in the configuration parameters is propagated directly on the SPI interface. If the mcspim_csx signal is activated, ensure that the configuration is changed only between SPI words to avoid corrupting the current transfer.

NOTE: To avoid data corruption, mcspim_csx polarity and mcspim_clk phase and mcspim_clk polarity must not be modified when the mcspim_csx signal is activated.

A delay between SPI words that requires the connected SPI slave device to switch from one configuration to another (for instance, from transmit-only to receive-only) must be handled by software.

At the end of the last SPI word, the channel must be deactivated (the SPIm.MCSPI_CHxCTRL[0] EN bit set to 0) and mcspim_csx can be forced to its INACTIVE state using the SPIm.MCSPI_CHxCONF[20] FORCE bit.

Figure 23-89 and Figure 23-90 show successive transfers with mcspim_csx maintained active low with a different configuration for each SPI word in single-data-pin and dual-data-pin interface modes, respectively.

Figure 23-89. Continuous Transfers With mcspim_csx Maintained Active (Single-Data-Pin Interface Mode)

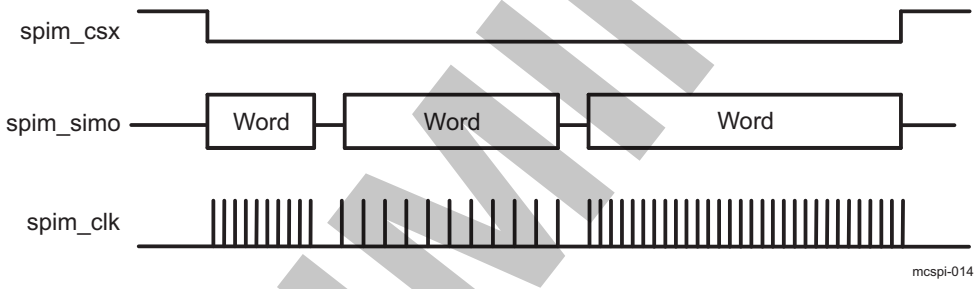
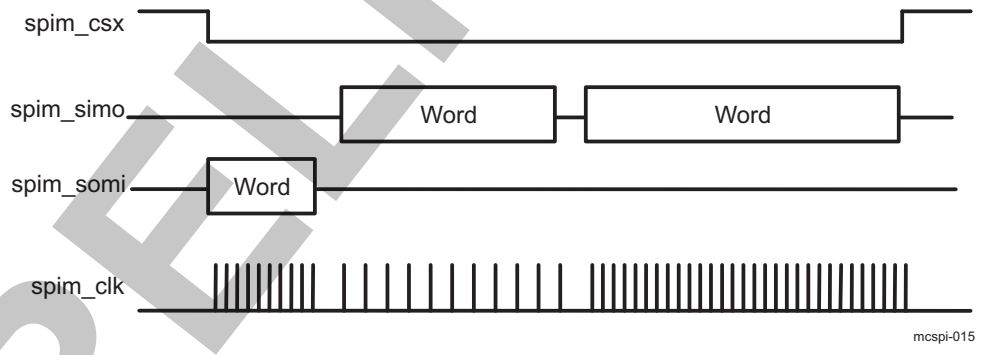


Figure 23-90. Continuous Transfers With mcspim_csx Maintained Active (Dual-Data-Pin Interface Mode)



NOTE: Turbo mode, described in Section 23.4.4.2.5.3, *Turbo Mode*, maintains mcspim_csx in active mode when the following conditions are met:

- A single channel is explicitly used (the SPIm.MCSPI_MODULCTRL[0] SINGLE bit is set to 1).
- Turbo mode is enabled in the configuration of the channel (the SPIm.MCSPI_CHxCONF[19] TURBO bit is set to 1).

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23.4.4.2.5.3 Turbo Mode

Turbo mode improves the throughput of the SPI interface when a single channel is enabled by allowing transfers until the shift register and the MCSPI_RXx register are full. Turbo mode is time saving when a transfer exceeds two words. This mode is programmable per channel (through the SPI1.MCSPI_CHxCONF[9] TURBO bit).

When several channels are enabled, the TURBO bit has no effect and the channel access to the shift registers remains as previously described.

In turbo mode, Rule 1 and Rule 2 apply, but Rule 3 does not (see Section 23.4.4.2.2, *Master Transmit-and-Receive Mode (Full Duplex)*). An enabled channel can be scheduled if its receive register is full (the SPIm.MCSPI_CHxSTAT[0] RXS bit) when the shift-register is assigned until the shift register is full.

The MCSPI_RXx register cannot be overwritten in turbo mode. Consequently, the SPIm.MCSPI_IRQSTATUS[3] RX0_OVERFLOW bit is never set in this mode.

23.4.4.2.6 Start-Bit Mode

In start-bit mode, an extended bit is added before the SPI word to indicate whether the next SPI word must be handled as a command or as data. This feature is available only in master mode. Start-bit mode cannot be used at the same time as turbo mode and/or force mcspim_csx mode. In this case, only one channel can be used; round-robin arbitration is not possible.

This mode is programmable per channel by setting the SPIm.MCSPI_CHxCONF[23] SBE bit to 1. The polarity of the extended bit is programmable per channel. When the SPIm.MCSPI_CHxCONF[24] SBPOL bit is set to 0, the SPI word must be handled as a command. When the SPIm.MCSPI_CHxCONF[24] SBPOL bit is set to 1, the SPI word must be handled as data. Moreover, start-bit polarity can be changed dynamically during start-bit transfer without disabling the channel for reconfiguration; in this case, users must configure the SPIm.MCSPI_CHxCONF[24] SBPOL bit before writing the SPI word to be transmitted to the TX register.

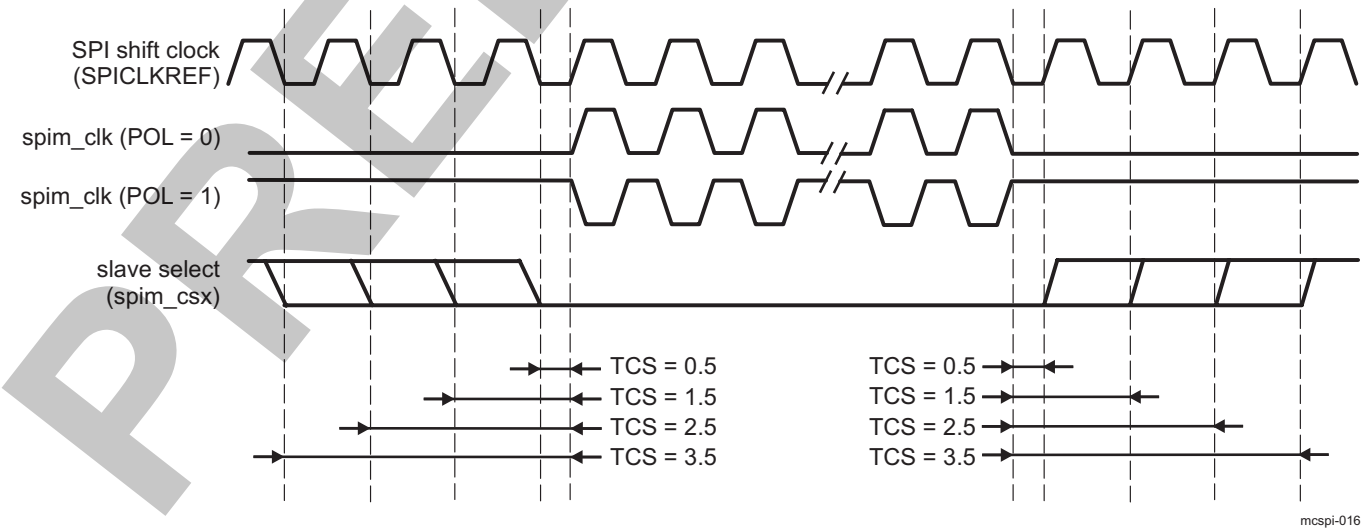
23.4.4.2.7 Chip-Select Timing Control

The chip-select (CS) timing control is available only in master mode with automatic CS generation (the MCSPI_MODULCTRL[0] SINGLE bit set to 0) to add a programmable delay between CS assertion and first clock edge, or CS removal and last clock edge.

This mode is programmable per channel (the SPIm.MCSPI_CHxCONF TCS bit).

Figure 23-91 shows the CS SPIEN timing controls.

Figure 23-91. CS SPIEN Timing Controls



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NOTE: Because of the design implementation for transfers using a clock divider ratio set to 1 (clock bypassed), a half cycle must be added to the value between CS assertion and the first clock edge with PHA = 1 or between CS removal and the last clock edge with PHA = 0.

23.4.4.2.8 Programmable SPI Clock (mcspim_clk)

In master mode, the baud rate of the SPI serial clock is programmable.

An internal reference clock, SPIm_FCLK, is used as input of a programmable divider (the SPIm.MCSPI_CHxCONF[5:2] CLKD bit field) to generate the bit rate of the serial output clock mcspim_clk. Table 23-271 summarizes the supported divisor values.

Table 23-271. SPI Master Clock Rates

Divider	Clock Rate
1	48 MHz
2	24 MHz
4	12 MHz
8	6 MHz
16	3 MHz
32	1.5 MHz
64	750 kHz
128	375 kHz
256	~187 kHz
512	~93.7 kHz
1024	~46.8 kHz
2048	~23.4 kHz
4096	~11.7 kHz
8192 and higher: Division not supported	–

23.4.4.2.8.1 Clock Ratio Granularity

By default, the clock division ratio is defined by the SPIm.MCSPI_CHxCONF[5:2] CLKD bit field with power-of-2 granularity leading to a clock division in the range 1 to 4096; in this case, the duty cycle is always 50 percent. With the SPIm.MCSPI_CHxCONF[29] CLKG bit, clock division granularity can be changed to one clock cycle; in that case the SPIm.MCSPI_CHxCTRL[15:8] EXTCLK bit field is concatenated with the SPIm.MCSPI_CHxCONF[5:2] CLKD bit field to give a 12-bit-wide division ratio in the range 1 to 4096.

When granularity is one clock cycle (the CLKG bit set to 1), for the odd value of the clock ratio, the clock high level lasts one clock cycle more than the low level, depending on the SPIm.MCSPI_CHxCONF[1] POL and SPIm.MCSPI_CHxCONF[0] PHA bits (see Table 23-272).

Table 23-272. CLKSPIO High/Low Time Computation

Clock Ratio F_{RATIO}	CLKSPIO High Time	CLKSPIO Low Time
1	T_{HIGH_REF}	T_{LOW_REF}
Even >= 2	T_ref * (F_{RATIO}/2)	T_ref * (F_{RATIO}/2)
Odd >= (POL = PHA)	T_ref * (F_{RATIO}– 1)/2	T_ref * (F_{RATIO} + 1)/2
Odd >= (POL =! PHA)	T_ref * (F_{RATIO}+ 1)/2	T_ref * (F_{RATIO} – 1)/2

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NOTE: F_{RATIO} = spi1_clk frequency (F_{OUT}) division ratio
T_{HIGH} = spi1_clk high time period
T_{LOW} = spi1_clk low time period
T_ref = SPI1_FCLK period
T_{HIGH_REF} = SPI1_FCLK high time period
T_{LOW_REF} = SPI1_FCLK low time period

If the CLKG bit is set to 1; F_{RATIO} = EXTCLK concatenated with CLKD + 1.

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For odd ratio values, the duty cycle is calculated as follows:

Duty_cycle = $(1 – 1/F_{RATIO})/2$

Table 23-273 shows examples of clock granularity with a clock source frequency of 48 MHz.

Table 23-273. Clock Granularity Examples

EXTCLK	CLKD	CLKG	F_{RATIO}	PHA	POL	T_{HIGH} (ns)	T_{LOW} (ns)	T_{PERIOD} (ns)	Duty Cycle	F_{OUT} (MHz)
X	0	0	1	X	X	10.4	10.4	20.8	50–50	48
X	1	0	2	X	X	20.8	20.8	41.6	50–50	24
X	2	0	4	X	X	41.6	41.6	83.2	50–50	12
X	3	0	8	X	X	83.2	83.2	166.4	50–50	6
0	0	1	1	X	X	10.4	10.4	20.8	50–50	48
0	1	1	2	X	X	20.8	20.8	41.6	50–50	24
0	2	1	3	1	0	41.6	20.8	62.4	66–33	16
0	2	1	3	1	1	20.8	41.6	62.4	33–66	16
0	3	1	4	X	X	41.6	41.6	83.2	50–50	12
5	0	1	81	1	0	852.8	832	1684.8	50.6–49.4	0.592
5	7	1	88	X	X	915.2	915.2	1830.4	50–50	0.545

23.4.4.3 Slave Mode

To select the MCSPI slave mode, set the SPIm.MCSPI_MODULCTRL[2] MS bit.

A MCSPI slave device can be connected to up to four external SPI master devices but handles transactions with one SPI master device at a time.

In slave mode, the MCSPI initiates data transfer on the data lines (mcspim_simo and mcspim_somi) when it is selected by an active control signal (mcspim_csx) and receives an SPI clock (mcspim_clk) from the external SPI master device. Only channel 0 can be configured as a slave. In slave mode, the MCSPI uses the edge of mcspim_csx to detect word length. For this reason, mcspim_csx must become inactive between each word.

The MCSPI does not support mcspim_csx active between SPI words. It uses the edge to detect word length.

23.4.4.3.1 Dedicated Resources

Only channel 0 can be enabled in slave mode. In this section, register names such as SPI1.MCSPI_CHxCTRL stand for SPI1.MCSPI_CH0CTRL, where x = 0 (channel 0 control register).

Figure 23-92 shows an example of four slaves wired on a single master device.

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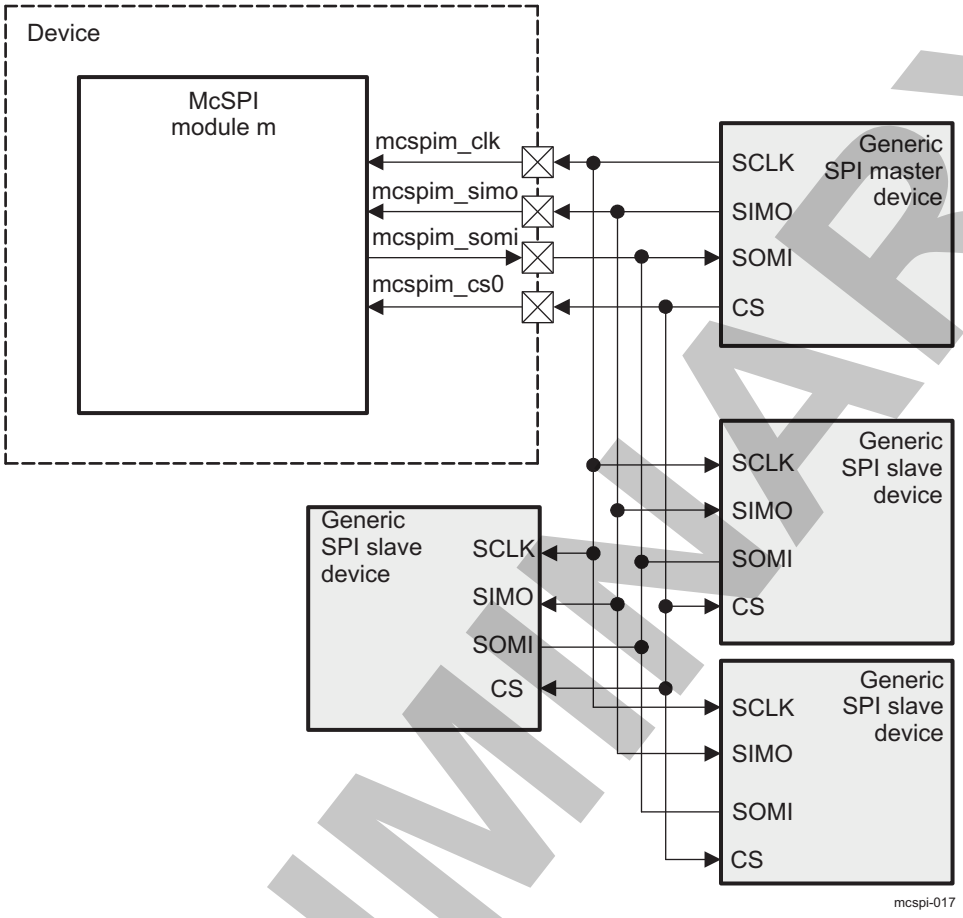
Figure 23-92. Example of MCSPI Slave With One Master and Multiple Slave Devices on Channel 0



Channel 0 in slave mode has the following resources:

- Its own channel enable, programmable with the SPIm.MCSPI_CHxCTRL[0] EN bit (where x = 0). This channel must be enabled before transmission and reception.
- For this mode, the slave-select signal can be detected on any of the mcspim_csx ports. This is programmable with the SPIm.MCSPI_CHxCONF[22:21] SPIENSLV bit field (where x = 0).
- Its own transmitter register, SPIm.MCSPI_TXx (where x = 0), on top of the common transmit shift register. If the MCSPI_TXx register is empty, the SPIm.MCSPI_CHxSTAT[1] TXS bit (where x = 0) is set. If MCSPI is selected by an external master (the active signal on the mcspim_csx port assigned to channel 0), the MCSPI_TXx register content of channel 0 is always loaded into the shift register, whether its content is updated or not. The MCSPI_TXx register must be loaded before MCSPI is selected by a master.
- Its own receiver register, SPIm.MCSPI_RXx (where x = 0), on top of the common receive shift register. If the MCSPI_RXx register is full, the SPIm.MCSPI_CHxSTAT[0] RXS bit (where x = 0) is set.

NOTE: The MCSPI_TXx and MCSPI_RXx registers of the other channels are not used. Reading from or writing to a channel register other than channel 0 has no effect.

- Its own communication configuration with the following parameters through the SPIm. MCSPI_CHxCONF register (where x = 0):
  - Transmit and receive modes, programmable with the TRM field
  - Interface mode (two data pins or single data pin) and data pins assignment, both programmable with the IS and DPE bits. (The SPIm modules are in slave mode after reset and must be properly configured for the modules to act in master mode.)

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– SPI word length, programmable with the WL bit
– mcspim_csx polarity, programmable with the EPOL bit
– mcspim_clk polarity, programmable with the POL bit
– mcspim_clk phase, programmable with the PHA bit

The mcspim_clk frequency of a transfer is controlled by the external SPI master connected to the MCSPI slave device. The SPIm.MCSPI_CHxCONF[5:2] CLKD bit field (where x = 0) is not used in slave mode.

NOTE: The configuration of the channel can be loaded in the SPIm.MCSPI_CHxCONF register (where x = 0) only when the channel is disabled.

- Two DMA request events, read and write, synchronize read/write accesses of the DMA controller with the activity of MCSPI. DMA requests are asserted using the SPIm.MCSPI_CHxCONF[15] DMAR bit (where x = 0) for reading and the SPIm.MCSPI_CHxCONF[14] DMAW bit (where x = 0) for writing.
- Four interrupt events (see Section 23.4.4.5.2, *Interrupt Events in Slave Mode*)

23.4.4.3.2 Slave Transmit-and-Receive Mode

The slave receive mode is programmable (set the SPIm.MCSPI_CHxCONF[13:12] TRM bit field [where x = 0] to 0x0).

In slave transmit-and-receive mode, the MCSPI_TXx register must be loaded before MCSPI is selected by an external SPI master device.

After a channel is enabled, transmission and reception proceed with interrupt and DMA request events.

The MCSPI_TXx register content is always loaded in the shift register whether it is updated or not. The event TXx_UNDERFLOW is activated accordingly and does not prevent transmission.

When the SPI word transfer completes (the SPIm.MCSPI_CHxSTAT0[2] EOT bit [where x = 0] is set to 1), the received data is transferred to the channel receive register.

To use MCSPI as a slave transmit-only device, the RXx_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the state of the MCSPI_RXx register (see Section 23.4.4.5.2, *Interrupt Events in Slave Mode*).

23.4.4.3.3 Slave Transmit-Only Mode

The slave transmit-only mode is programmable (set the SPIm.MCSPI_CHxCONF[13:12] TRM bit field [where x = 0] to 0x2) and avoids the requirement for the MPU to read the MCSPI_RXx register (minimizing data movement) only when transmission is meaningful.

To use the MCSPI as a slave transmit-only device, the RXx_FULL and RX0_OVERFLOW interrupts and DMA read requests must be disabled due to the state of the MCSPI_RXx register.

When the SPI word transfer completes, the SPIm.MCSPI_CHxSTAT[2] EOT bit is set (where x = 0).

Figure 23-93 shows a half-duplex system with a master device on the left and a transmit-only slave device on the right. Each time a bit transfers out from the slave, 1 bit transfers in the master. After eight cycles of the serial clock mcspim_clk, WordB transfers from the slave to the master.

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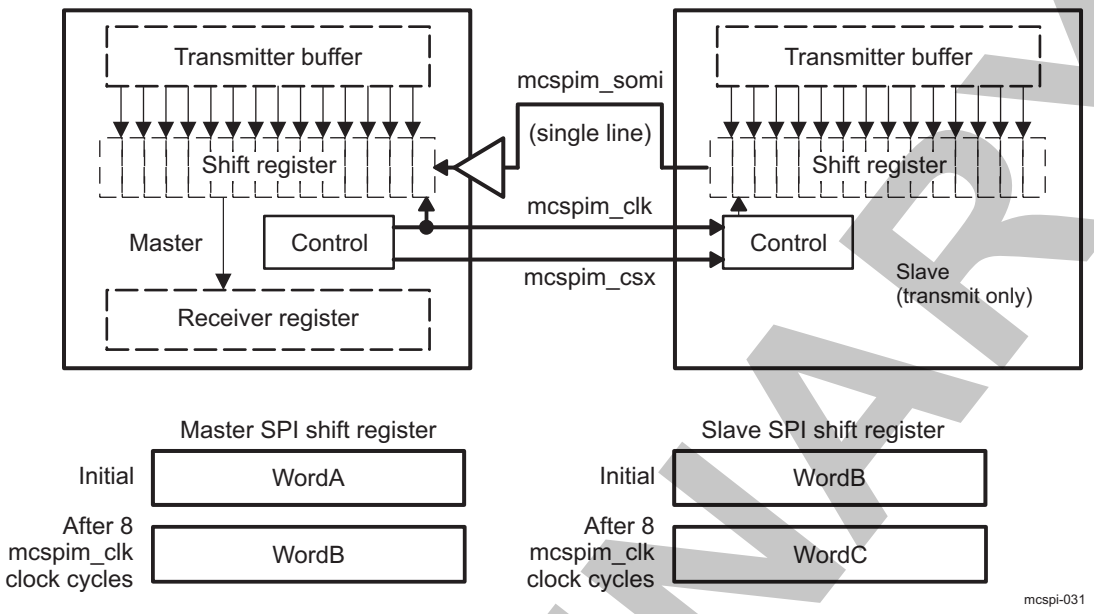
Figure 23-93. SPI Half-Duplex Transmission (Transmit-Only Slave)



23.4.4.3.4 Slave Receive-Only Mode

The slave receive mode is programmable (set the SPIm.MCSPI_CHxCONF[13:12] TRM bit field [where x = 0] to 0x1).

In receive-only mode, the MCSPI_TXx register must be loaded before the MCSPI is selected by an external SPI master device. The MCSPI_TXx register content is always loaded into the shift register whether it is updated or not. The TXx_UNDERFLOW event is activated accordingly and does not prevent transmission.

When the SPI word transfer completes (the SPIm.MCSPI_CHxSTAT0[2] EOT bit [where x = 0] is set to 1), the received data is transferred to the channel receive register.

To use the MCSPI as a slave receive-only device, the TXx_EMPTY and TXx_UNDERFLOW interrupts and the DMA write requests must be disabled due to the state of the MCSPI_TXx register.

For a full-duplex transmission, the serial clock (mcspim_clk) synchronizes shifting and sampling of the information on the single serial data line. For full duplex, two data lines are required. If mcspim_clk synchronizes on a single serial data line, the data line should be half-duplex.

Figure 23-94 shows a half-duplex system with a master device on the left and a receive-only slave device on the right. Each time a bit transfers out from the master, 1 bit transfers in from the slave. After eight cycles of the serial clock mcspim_clk, WordA transfers from the master to the slave.

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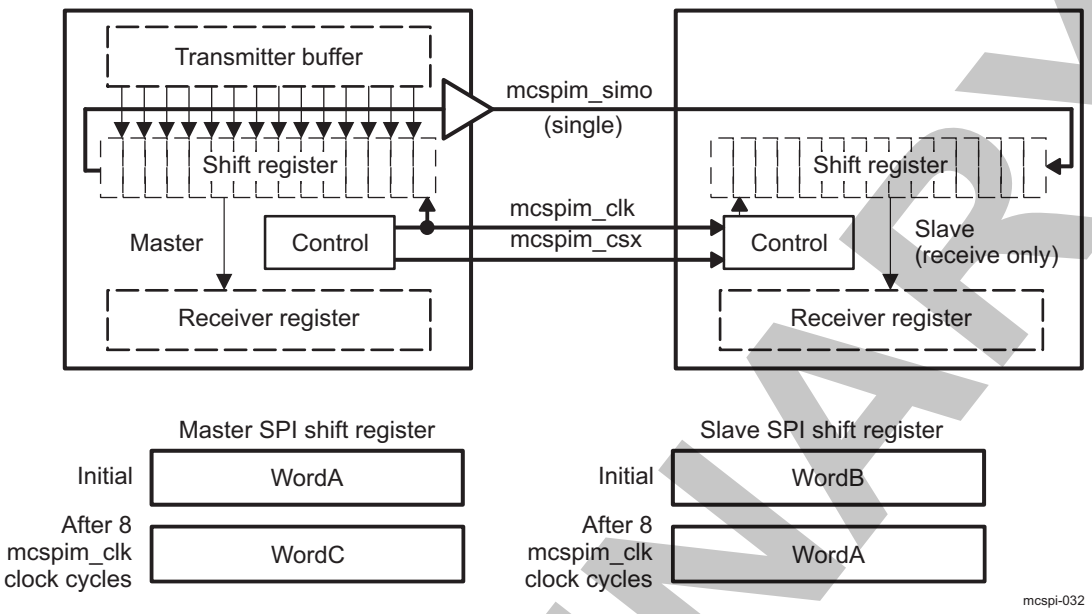
Figure 23-94. SPI Half-Duplex Transmission (Receive-Only Slave)



23.4.4.4 FIFO Buffer Management

The MCSPI controller has a built-in 64-byte buffer to unload the DMA or interrupt handler and improve data throughput.

This buffer can be used by only one channel at a time and is selected by setting the SPIm.MCSPI_CHxCONF[28] FFER or SPIm.MCSPI_CHxCONF[27] FFEW bit to 1. If several channels are selected and several FIFO enable bit fields are set to 1, the controller forces the buffer not to be used; the driver must set only one FIFO enable bit field.

The buffer can be used in the following modes:

- Master or slave mode
- Transmit-only, receive-only, or transmit-and-receive mode
- Single channel or turbo mode, or normal round-robin mode. In round-robin mode the buffer is used by only one channel.

Every word length (SPIm.MCSPI_CHxCONF[11:7] WL) is supported.

In transmit-and-receive mode, the buffer can be used in transmit (see Figure 23-95) or receive (see Figure 23-96) directions, or in both directions. If only one direction is chosen in transmit-and-receive mode, the full buffer is used for this direction. In both directions, the buffer is split into two 32-byte buffers, one for each direction (see Figure 23-97).

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Figure 23-95. Buffer Used in Transmit Direction Only

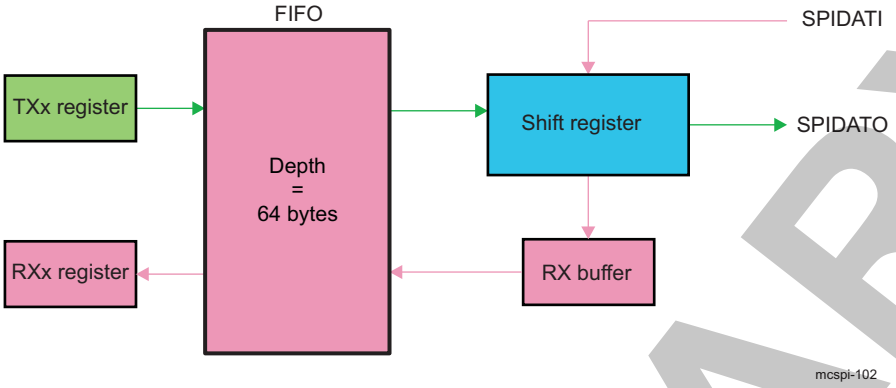


Figure 23-96. Buffer Used in Receive Direction Only

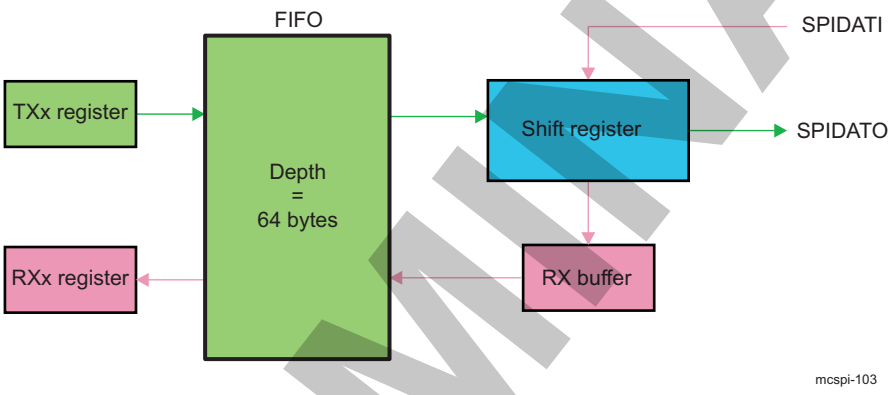
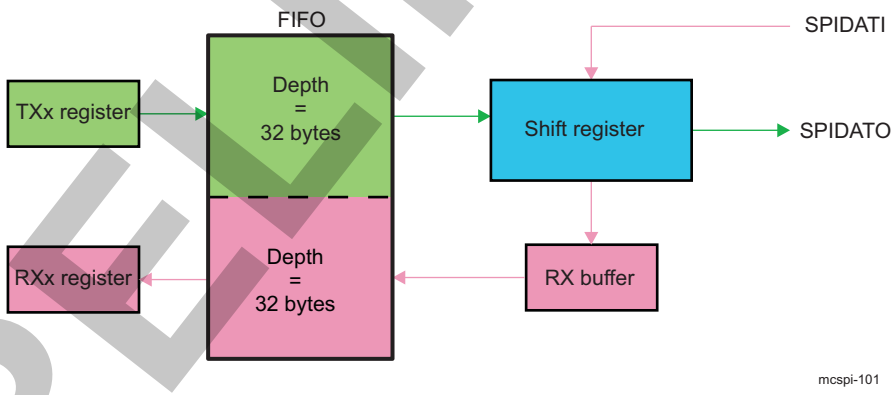


Figure 23-97. Buffer Used for Transmit and Receive Directions



Two levels (SPIm.MCSPI_XFERLEVEL[5:0] AEL and SPIm.MCSPI_XFERLEVEL[13:8] AFL) rule the buffer management. The granularity of these levels is 1 byte; it is not aligned with the SPI word length. The driver must set these values as a multiple of the SPI word length defined in WL. Table 23-274 lists the number of bytes written in the FIFO, depending on the word length.

Table 23-274. FIFO Writes, Word Length Relationship

SPI Word Length WL	3 <= WL<= 7	8 <= WL <= 15	16 <= WL <= 31
Number of bytes written in the FIFO	1 byte	2 bytes	4 bytes

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The FIFO buffer pointers are reset when the corresponding channel is enabled or the FIFO configuration changes.

23.4.4.4.1 Buffer Almost Full

The MCSPI_XFERLEVEL[15:8] AFL bit field is needed when the buffer is used to receive an SPI word from a slave (the MCSPI_CHxCONF[28] FFER bit must be set to 1). It defines the almost-full buffer status. See Figure 23-98.

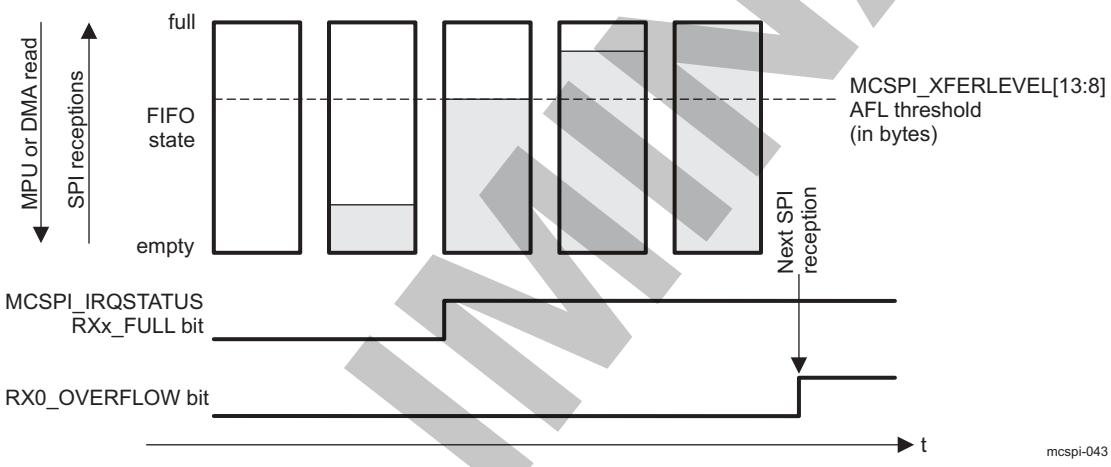
When the FIFO pointer reaches this level, an interrupt or a DMA request is sent to the MPU to enable the system to read AFL + 1 bytes from the receive register.

NOTE: AFL + 1 must correspond to a multiple value of the MCSPI_CHxCONF[11:7] WL bit field.

When DMA is used, the request is deasserted after the first receive register read.

No new request is asserted again as long as the system has not performed the correct number of read accesses.

Figure 23-98. Buffer Almost Full Level (AFL)



NOTE: The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the SPIm_DMA_RXx request is asserted on the same conditions as the MCSPI_IRQSTATUS RXx_FULL flag.

23.4.4.4.2 Buffer Almost Empty

The MCSPI_XFERLEVEL[7:0] AEL bit field is needed when the buffer is used to transmit an SPI word to a slave (the MCSPI_CHxCONF[27] FFEW bit must be set to 1). It defines the almost-empty buffer status. See Figure 23-99.

When the FIFO pointer does not reach this level, an interrupt or a DMA request is sent to the MPU to enable the system to write AEL + 1 bytes to the transmit register.

NOTE: AEL + 1 must correspond to a multiple value of the MCSPI_CHxCONF[11:7] WL bit field.

When DMA is used, the request is deasserted after the first transmit register write.

No new request is asserted again as long as the system has not performed the correct number of write accesses.

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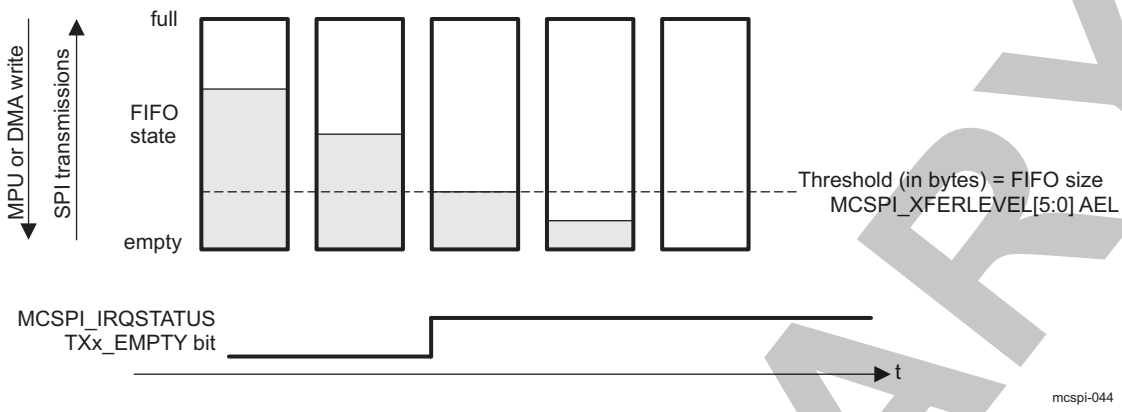
Figure 23-99. Buffer Almost Empty Level (AEL)



NOTE: The MCSPI_IRQSTATUS register bits are not available in DMA mode. In DMA mode, the SPIm_DMA_TXx request is asserted on the same conditions as the MCSPI_IRQSTATUS TXx_EMPTY flag.

23.4.4.4.3 End of Transfer Management

When the FIFO buffer is enabled for a channel, the user must previously configure in the MCSPI_XFERLEVEL register the AEL and AFL levels and especially the MCSPI_XFERLEVEL[31:16] WCNT bit field to define the number of SPI words to be transferred using the FIFO before enabling the channel.

This counter lets the controller stop the transfer correctly after a defined number of SPI word transfers. If WNCT is set to 0x0000, the counter is not used and the user must stop the transfer manually by disabling the channel; in this case, the user does not know how many SPI transfers have been done. For received words, software must poll the CHxSTAT[5] RXFFE bit and read the MCSPI_RXx receive register to empty the FIFO buffer.

When the end-of-word count interrupt is generated (the MCSPI_IRQSTATUS[17] EOW bit is set), the user can disable the channel and poll the MCSPI_CHxSTAT[5] RXFFE bit to know the last SPI words in the FIFO buffer and read them.

No new request is asserted as long as the system has not performed the correct number of write accesses.

23.4.4.5 Interrupts

Each channel can issue interrupt events.

Each interrupt event has status bits in the SPIm.MCSPI_IRQSTATUS register (RXx_FULL, TXx_UNDERFLOW, TXx_EMPTY, etc.) (where x = 0, 3) that indicate whether service is required. Each status bit has an interrupt enable bit (a mask) in the SPIm.MCSPI_IRQENABLE register (RXx_FULL_ENABLE, TXx_UNDERFLOW_ENABLE, TXx_EMPTY_ENABLE, etc.).

When an interrupt occurs and a mask is later applied on it, the interrupt line is not asserted again, even if the interrupt source is not serviced.

The MCSPI supports interrupt-driven and polling operations.

23.4.4.5.1 Interrupt Events in Master Mode

In master mode, the interrupt events related to the state of the MCSPI_TXx register are TXx_EMPTY and TXx_UNDERFLOW. The interrupt event related to the state of the MCSPI_RXx register is RXx_FULL.

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23.4.4.5.1.1 TXx_EMPTY

The TXx_EMPTY event is activated when a channel is enabled and its MCSPI_TXx register is empty (transient event). Enabling a channel automatically triggers this event, except in master receive-only mode (see Section 23.4.4.2.4, *Master Receive-Only Mode*). When the FIFO buffer is enabled (the MCSPI_CHxCONF[27] FFEW bit is set to 1), the MCSPI_IRQSTATUS TXx_EMPTY bit is set as soon as there is enough space in the buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5:0] AEL bit field.

The MCSPI_TXx register must be loaded with data to remove the source of the interrupt; the SPIm.MCSPI_IRQSTATUS TXx_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXx_EMPTY event is asserted as long as the MPU has not performed the number of writes into the MCSPI_TXx register defined by the MCSPI_XFERLEVEL[5:0] AEL bit field. The MPU must perform the correct number of writes.

23.4.4.5.1.2 TXx_UNDERFLOW

The event TXx_UNDERFLOW is activated when the channel is enabled and if the MCSPI_TXx register or the FIFO is empty (not updated with new data) when an external master device starts a data transfer with the MCSPI (transmit and receive).

The TXx_UNDERFLOW is a harmless warning in master mode.

To avoid having a TXx_UNDERFLOW event at the beginning of a transmission, the TXx_UNDERFLOW event is not activated when no data has been loaded into the MCSPI_TXx register, because the channel is enabled. To avoid having a TXx_UNDERFLOW event, the MCSPI_TXx register must seldom be loaded.

The SPIm.MCSPI_IRQSTATUS TXx_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

23.4.4.5.1.3 RXx_ FULL

The RXx_FULL event is activated when a channel is enabled and the MCSPI_RXx register becomes filled (transient event). When the FIFO buffer is enabled (the MCSPI_CHxCONF[28] FFER bit is set to 1), RXx_ FULL is asserted as soon as the number of bytes held in the FIFO to be read reaches the MCSPI_XFERLEVEL[13:8] AFL threshold.

The MCSPI_RXx register must be read to remove the source of the interrupt; the MCSPI_IRQSTATUS RXx_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXx_FULL event is asserted as long as the MPU has not performed AFL + 1 reads into MCSPI_RXx. The MPU must perform the correct number of reads.

23.4.4.5.1.4 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfers defined in the MCSPI_XFERLEVEL[31:16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the SPI transfer is halted on the channel using the FIFO buffer as soon as MCSPI_XFERLEVEL[31:16] WCNT is not reloaded and the channel is not re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

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23.4.4.5.2 Interrupt Events in Slave Mode

In slave mode, the interrupt events related to the state of the MCSPI_TXx register are TXx_EMPTY and TXx_UNDERFLOW. The interrupt events related to the state of the MCSPI_RXx are RXx_FULL and RX0_OVERFLOW (channels 1, 2, and 3 do not have a receiver overflow status bit). See the MCSPI_IRQSTATUS register.

23.4.4.5.2.1 TXx_EMPTY

The TXx_EMPTY event is activated when a channel is enabled and its MCSPI_TXx register is empty. Enabling the channel automatically raises this event. If the FIFO buffer is enabled (the MCSPI_CHxCONF[27] FFEW bit is set to 1), the TXx_EMPTY event is asserted as soon as there is enough space in buffer to write a number of bytes defined by the MCSPI_XFERLEVEL[5:0] AEL bit field.

The MCSPI_TXx register must be loaded with data to remove the source of the interrupt; the SPIm.MCSPI_IRQSTATUS TXx_EMPTY interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new TXx_EMPTY event is asserted as long as the MPU has not performed the number of writes into the MCSPI_TXx register defined by MCSPI_XFERLEVEL[5:0] AEL bit field. The MPU must perform the correct number of writes.

23.4.4.5.2.2 TXx_UNDERFLOW

The TXx_UNDERFLOW event is activated when a channel is enabled and if the MCSPI_TXx register is empty (not updated with new data) when an external master device starts a data transfer with the MCSPI (transmit and receive).

When FIFO is enabled, the data emitted while the underflow event is raised is not the last data written in the FIFO but the next data in the FIFO (an old transmitted value or a dummy data in the FIFO has been reset).

TXx_UNDERFLOW indicates an error (data loss) in slave mode.

To avoid having a TXx_UNDERFLOW event at the beginning of a transmission, the TXx_UNDERFLOW event is not activated when no data has been loaded into the MCSPI_TXx register because the channel is enabled.

The SPIm.MCSPI_IRQSTATUS TXx_UNDERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

23.4.4.5.2.3 RXx_FULL

The RXx_FULL event is activated when a channel is enabled and the MCSPI_RXx register is being filled (transient event). When the FIFO buffer is enabled (the MCSPI_CHxCONF[28] FFER bit is set to 1), RXx_FULL is asserted as soon as the number of bytes held in the buffer to read defined by the MCSPI_XFERLEVEL[13:8] AFL bit field.

The MCSPI_RXx register must be read to remove the source of the interrupt; the SPIm.MCSPI_IRQSTATUS RXx_FULL interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

When FIFO is enabled, no new RXx_FULL event is asserted as long as the MPU has not performed AFL + 1 reads into MCSPI_RXx. The MPU must perform the correct number of reads.

23.4.4.5.2.4 RX0_OVERFLOW

The RX0_OVERFLOW event is activated in slave mode in transmit-and-receive mode or receive-only mode when a channel is enabled and the MCSPI_RXx register or FIFO is full when a new SPI word is received. The MCSPI_RXx register is always overwritten with the new SPI word. If the FIFO is enabled, data within the FIFO are overwritten; it must be considered as corrupted. The RX0_OVERFLOW event should not appear in slave mode using the FIFO.

The RX0_OVERFLOW event indicates an error (data loss) in slave mode.

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The MCSPI_IRQSTATUS[3] RX0_OVERFLOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

23.4.4.5.2.5 End Of Word Count

The MCSPI_IRQSTATUS[17] EOW event (end of word count) is activated when the channel is enabled and configured to use the built-in FIFO. This interrupt is raised when the controller performs the number of transfers defined in the MCSPI_XFERLEVEL[31:16] WCNT bit field. If WCNT is set to 0x0000, the counter is not enabled and this interrupt is not generated.

The end of word count interrupt also indicates that the SPI transfer is halted on the channel using the FIFO buffer as soon as WCNT is not reloaded and the channel is not re-enabled.

The MCSPI_IRQSTATUS[17] EOW interrupt status bit must be cleared for interrupt line deassertion (if the event is enabled as the interrupt source).

23.4.4.5.3 Interrupt-Driven Operation

An interrupt enable bit in the SPIm.MCSPI_IRQENABLE register can be set to enable each event to generate interrupt requests when the corresponding event occurs. Status bits are automatically set by hardware logic conditions.

When an event occurs (the single interrupt line is asserted), the MPU must:

1. Read the SPIm.MCSPI_IRQSTATUS register to identify which event occurred.
2. Read the MCSPI_RXx register that corresponds to the event to remove the source of an RXx_FULL event or write into the MCSPI_TXx register that corresponds to the event to remove the source of a TXx_EMPTY event. No action is required to remove the source of the WKS (wake-up), TXx_UNDERFLOW, and RX0_OVERFLOW events.
3. Set the corresponding bit of the SPIm.MCSPI_IRQSTATUS register to 1 to clear an interrupt status and then release the interrupt line.

The interrupt status bit must always be reset after channel enabling and before events are enabled as interrupt sources.

23.4.4.5.4 Polling

When the interrupt capability of an event is disabled in the SPIm.MCSPI_IRQENABLE register, the interrupt line is not asserted, but the status bits in the SPIm.MCSPI_IRQSTATUS register can be polled by software to detect when the corresponding event occurs.

Once the expected event occurs:

- RXx_FULL: To remove the source of the event, the MPU must read the corresponding MCSPI_RXx register.
- TXx_EMPTY: To remove the source of the event, the MPU must write into the corresponding MCSPI_TXx register.
- WKS (wake-up), TXx_UNDERFLOW, and RX0_OVERFLOW: No action is required to remove the source of the event.

To clear an interrupt, set the corresponding status bit of the SPIm.MCSPI_IRQSTATUS register to 1. This does not affect the interrupt line state.

23.4.4.6 DMA Requests

The DMA_SYSTEM controller module manages DMA accesses. The DMA_SYSTEM controller reduces the MPU charge for data transfers.

Each MCSPI channel, if enabled, can issue DMA requests. There are two DMA request lines per MCSPI channel (one for read and one for write).

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The DMA read request line is asserted when the MCSPI channel is enabled and new data is available in the receive register of the MCSPI channel. A DMA read request can be individually masked with the SPI1.MCSPI_CHxCONF[15] DMAR bit. The DMA read request line is deasserted when reading of the MCSPI_RXx register of the MCSPI channel completes.

The DMA write request line is asserted when the MCSPI channel is enabled and the MCSPI_TXx register of the MCSPI channel is empty. A DMA write request can be individually masked with the SPI1.MCSPI_CHxCONF[14] DMAW bit. The DMA write request line is deasserted when loading of the MCSPI_TXx register of the channel completes.

23.4.4.7 Power Saving Management

Power consumption can be optimized by switching off internal clocks (interface and functional clock) when there is no activity. The MCSPI is compliant with the idle and wake-up system handshake protocol.

23.4.4.7.1 Normal Mode

In normal mode, internal SPI module clocks are automatically switched off (autogated) when there is no activity in slave or master mode.

Autogating of the module interface clock and functional clock occurs when the following conditions are met:

- The SPIm.MCSPI_SYSCONFIG[0] AUTOIDLE bit is set.
- In master mode, there is no data to transmit or receive in all channels.
- In slave mode, the MCSPI is not selected by the external master and there are no register accesses.

Autogating of the module interface clock and functional clock stops when the following conditions are met:

- In master mode, an internal access occurs.
- In slave mode, an internal access occurs or the MCSPI is selected by the external master.

23.4.4.7.2 Idle Mode

At the PRCM module level, when all conditions are met to shut off the CORE_48M_FCLK or CORE_L4_ICLK output clock, the PRCM module automatically launches a hardware handshake protocol to ensure that the MCSPI is ready to have its clocks switched off. Namely, the PRCM module asserts an IDLE request to the MCSPI.

Although this handshake is completely hardware-oriented and out of software control, the method in which the MCSPI module acknowledges the PRCM IDLE request is configurable through the MCSPI.SYSCONFIG[4:3] SIDLEMODE bit field.

The settings of the SIDLEMODE bit field and the related acknowledgment modes are:

- Force-idle mode (the SPIm.MCSPI_SYSCONFIG[4:3] SIDLEMODE bit field is set to 0x0): The MCSPI module acknowledges unconditionally the IDLE request from the PRCM module, regardless of its internal operations. This mode must be used carefully in this case because it does not prevent the loss of data when the clock is switched off.
- No-idle mode (the SIDLEMODE bit field is set to 0x1): The MCSPI never acknowledges an IDLE request from the PRCM module and is safe from a module point of view because it ensures that the clocks remain active. However, it is not efficient to save power because it does not allow the PRCM output clock to be shut off and thus the power domain to be set to a lower power state.
- Smart-idle mode (the SIDLEMODE bit field is set to 0x2): The MCSPI acknowledges the IDLE request, basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions, IRQs, or DMA requests are treated. This is the best approach for efficient system power management.

When configured in smart-idle mode, the MCSPI also offers an additional granularity on the CORE_48M_FCLK and CORE_L4_ICLK gating. The SPIm.SYSCONFIG[9:8] CLOCKACTIVITY bit field determines which clock shuts down (the CORE_48M_FCLK, CORE_L4_ICLK, neither clock, or both clocks).

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The setting of the CLOCKACTIVITY bit field is used internally to the MCSPI to determine on which part of the module the conditions to acknowledge the PRCM IDLE request are tested. For example, if CORE_48M_FCLK is not shut down on a PRCM IDLE request, the MCSPI considers only CORE_L4_ICLK and the associated pending activities before acknowledging the request.

Some MCSPI features are associated with CORE_L4_ICLK and others with CORE_48M_FCLK. Using the CLOCKACTIVITY bit field with the smart-idle mode ensures that the features associated with the clock that remains active are always enabled, even if the MCSPI acknowledges an IDLE request.

The settings of the CLOCKACTIVITY bit field and the associated features are:

- CLOCKACTIVITY set to 00: ICLK off and FCLK off, ICLK and FCLK are considered for generating the acknowledge. This setting also means that FCLK and ICLK are likely to be shut down on a PRCM IDLE request.
- CLOCKACTIVITY set to 01: ICLK on and FCLK off, ICLK is not shut down on a PRCM IDLE request; only FCLK is concerned.
- CLOCKACTIVITY set to 10: ICLK off and FCLK on, FCLK is not shut down on a PRCM IDLE request; only ICLK is concerned.
- CLOCKACTIVITY set to 11: ICLK on and FCLK on, none of the clocks are shut down. This means the MCSPI can potentially acknowledge the IDLE request without checking the internal functions linked to its clocks.

CAUTION

The PRCM module does not have a hardware means of reading the CLOCKACTIVITY settings. Therefore, software must ensure consistent programming between CLOCKACTIVITY and the CORE_48M_FCLK and CORE_L4_ICLK control bits in the PRCM module. If the MCSPI is disabled in the CM_FCLKEN and CM_ICLKEN PRCM registers while CLOCKACTIVITY is set to 11, nothing prevents the PRCM module from asserting its IDLE request, which is acknowledged regardless of the features associated with the MCSPI clocks. This can lead to unpredictable behavior.

23.4.4.7.2.1 Wake-Up Event in Smart-Idle Mode

The module wake-up feature is enabled when the SPIm.MCSPI_SYSCONFIG[2] ENAWAKEUP and SPIm.MCSPI_WAKEUPENABLE[0] WKEN bits are set. Wake-up capability is relevant only when the module is configured in slave mode.

The module generates an asynchronous wake-up request to the system power manager to switch back the interface clock and the functional clock. A wakeup is requested when channel 0 is enabled and an asynchronous selection occurs on the mcspim.csx port associated with channel 0 (see the definition for the SPIm.MCSPI_CHxCONF[22:21] SPIENSLV bit field [where x = 0] in the register table description).

After the McSPI wake-up request, the system power manager must reactivate the interface clock:

- Before the beginning of the second SPI word serialization when the McSPI is in slave transmit-only mode or in slave transmit-and-receive mode
- Before the end of the second received SPI word in slave receive-only mode. To avoid data loss, the first received SPI word must be read from the SPIm.MCSPI_RXx register (where x = 0) before the completion of the second SPI word serialization.

Table 23-275 lists the supported cases in smart-idle mode.

Table 23-275. Smart-Idle Mode and Wake-Up Capabilities

Mode	Interface Clock	SPI Clock Ref	Functionality	Wake-Up Event
Master	Must be maintained	Must be maintained	Full functionality, but the module does not generate a new interrupt or DMA request until the system exits wake-up mode	No wake-up event

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Table 23-275. Smart-Idle Mode and Wake-Up Capabilities (continued)

Mode	Interface Clock	SPI Clock Ref	Functionality	Wake-Up Event
Slave	Can be switched off	Can be switched off	An SPI word can be transmitted and/or received, but the module does not generate any new interrupts or DMA requests until the system exits wake-up mode.	The module asynchronously sends a wake-up request if an event on the mcspim_csx port associated with channel 0 is detected.

In wake-up mode, the interrupt and DMA request lines are no longer asserted.

Any access to the module in wake-up mode generates an error as long as the interface clock is alive.

23.4.4.7.2.2 Transitions From Smart-Idle Mode to Normal Mode

The MCSPI detects the end of the wake period through the idle and wake-up hardware handshake protocol.

The interrupt status register (the SPIm.MCSPI_IRQSTATUS[16] WKS bit) is updated with the event causing the wakeup; the wake-up event at the origin of the transition to the normal mode is converted to its corresponding interrupt when enabled by the SPIm.MCSPI_IRQENABLE[16] WKE bit or the DMA request.

Interrupts and wake-up events have independent enable and disable controls, accessible through the SPIm.MCSPI_IRQENABLE and SPIm.MCSPI_WAKEUPENABLE registers. Software must ensure the overall consistency.

The interrupt status register SPIm.MCSPI_IRQSTATUS is updated with the event causing the wakeup; the wake-up event at the origin of the transition to normal mode is converted to its corresponding interrupt request or DMA request. The module is fully operational.

23.4.4.7.2.3 Force-Idle Mode

Force-idle mode is enabled and exited as follows:

- Force-idle mode is enabled when the SPIm.MCSPI_SYSCONFIG[4:3] SIDLEMODE bit field is set to 0x0.
  - In force-idle mode, the MCSPI responds unconditionally to the IDLE request by deasserting unconditionally the interrupt and DMA request lines, if asserted. In addition, the wake-up capability is totally inhibited even if the SPIm.MCSPI_SYSCONFIG[2] ENAWAKEUP and SPIm.MCSPI_WAKEUPENABLE[0] WKEN bits are set.
  - The transition from normal mode to idle mode does not affect the interrupt event bits of the SPIm.MCSPI_IRQSTATUS register.
  - In force-idle mode, because the module must be disabled, the interrupt and DMA request lines are likely deasserted. The interface clock and SPI clock provided to the MCSPI can be switched off.
  - An IDLE request during an SPI data transfer can lead to an unexpected and unpredictable result. Software must avoid such a request.
- The module exits force-idle mode through the idle and wake-up hardware handshake protocol.

  The module is fully operational. The interrupt and DMA request lines are optionally asserted one clock cycle later.

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23.4.5 MCSPI Programming Guide

23.4.5.1 MCSPI Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the MCSPI module.

23.4.5.1.1 Global Initialization

23.4.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the I^2C module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the I^2C. For further information, see Section 23.1.2, *HS I^2C Environment* Section 23.1.3, *and HS I^2C Integration*.

For more information, see Section 23.4.3, *MCSPI Integration*.

Table 23-276 lists the information on the global initialization of the surrounding modules.

Table 23-276. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	MCSPI_FCLK functional clock must be enabled. See Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
L4 Interconnect	For information about L4_PER interconnect configuration, see Section 14.3, *L4 Interconnects*, in Chapter 14, *Interconnect*.
DMA_SYSTEM	DMA configuration must be done to enable the module DMA channel requests. See Chapter 16, *DMA_SYSTEM*.
MPU INTC	Cortex-A15 MPU, Cortex-M4 MPU, or DSP INTC must be configured to enable the interrupt request generation to the Cortex-A15 MPU or Cortex-M4 MPU, or in Section 5.3.2.6, *DSP INTC*, in Chapter 5, *DSP Subsystem*.

23.4.5.1.1.2 MCSPI Global Initialization

23.4.5.1.1.2.1 Main Sequence – MCSPI Global Initialization

This procedure initializes the MCSPI module after a POR or software reset.

Table 23-277. MCSPI Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	SPIm.MCSPI_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is finished?	SPIm.MCSPI_SYSSTATUS[0] RESETDONE	=0x1

23.4.5.1.2 Operational Mode Configuration

23.4.5.1.2.1 MCSPI Operational Modes

The selection of the working mode is done with the SPIm.MCSPI_CHxCONF register. Table 23-278 through Table 23-280 list the possible operating modes and their configurations.

Table 23-278. MCSPI Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set receive mode.	SPIm.MCSPI_CHxCONF[13:12] TRM	0x1
Set the word length.	SPIm.MCSPI_CHxCONF[11:7] WL	0x8
Clock initialization and channel enabling	SPIm.MCSPI_MODULCTRL[2] MS SPIm.MCSPI_CHxCTRL[0] EN	0x0 0x1

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Table 23-278. MCSPI Receive Mode Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Channels activated low during ACTIVE state	SPIm.MCSPI_CHxCONF[6] EPOL	0x1
Clock held low during INACTIVE state	SPIm.MCSPI_CHxCONF[1] POL	0x0
Data latched on odd-numbered edges of the SPI clock	SPIm.MCSPI_CHxCONF[0] PHA	0x0
Reset the status bits.	SPIm.MCSPI_IRQSTATUS	0x0

Table 23-279. MCSPI Transmit Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit mode.	SPIm.MCSPI_CHxCONF[13:12] TRM	0x2
Set the word length.	SPIm.MCSPI_CHxCONF[11:7] WL	0x8
Clock initialization and channel enabling	SPIm.MCSPI_MODULCTRL[2] MS SPIm.MCSPI_CHxCTRL[0] EN	0x0 0x1
Channels activated low during ACTIVE state	SPIm.MCSPI_CHxCONF[6] EPOL	0x1
Clock held low during INACTIVE state	SPIm.MCSPI_CHxCONF[1] POL	0x0
Data latched on odd-numbered edges of the SPI clock	SPIm.MCSPI_CHxCONF[0] PHA	0x0
Reset the status bits.	SPIm.MCSPI_IRQSTATUS	0x0

Table 23-280. MCSPI Transmit-and-Receive Mode Initialization

Step	Register/Bit Field/Programming Model	Value
Set transmit and receive mode.	SPIm.MCSPI_CHxCONF[13:12] TRM	0x0
Set the word length.	SPIm.MCSPI_CHxCONF[11:7] WL	0x8
Clock initialization and channel enabling	SPIm.MCSPI_MODULCTRL[2] MS SPIm.MCSPI_CHxCTRL[0] EN	0x0 0x1
Channels activated low during ACTIVE state	SPIm.MCSPI_CHxCONF[6] EPOL	0x1
Clock held low during INACTIVE state	SPIm.MCSPI_CHxCONF[1] POL	0x0
Data latched on odd-numbered edges of the SPI clock	SPIm.MCSPI_CHxCONF[0] PHA	0x0
Reset the status bits.	SPIm.MCSPI_IRQSTATUS	0x0

23.4.5.1.2.1.1 Common Transfer Procedures Without FIFO – Polling Method

23.4.5.1.2.1.1.1 Receive-Only Procedure – Polling Method

Table 23-281 lists the receive-only procedure using the polling method. The MCSPI is acting as slave.

Table 23-281. Receive-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode	See Table 23-278.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until receive register is full?	SPIm.MCSPI_RXx	=0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.2.1.1.2 Receive-Only Procedure – Interrupt Method

Table 23-282 lists the receive-only procedure using the interrupt method. The MCSPI is acting as slave.

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Table 23-282. Receive-Only Procedure – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-278.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Enable the interrupt for the receiver register.	SPIm.MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0x1
Read the status register.	SPIm.MCSPI_IRQSTATUS[2] RX_FULL	0x0
Disable the interrupt.	SPIm.MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0x0
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read the receiver register.	SPIm.MCSPI_RXx	xxxx

23.4.5.1.2.1.1.3 Transmit-Only Procedure – Polling Method

Table 23-283 lists the transmit-only procedure using the polling method. The MCSPI is acting as master.

Table 23-283. Transmit-Only Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-279	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of transfer?	SPIm.MCSPI_CHxSTAT[2:1]	=0x2
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.2.1.1.4 Transmit-and-Receive Procedure – Polling Method

Table 23-283 lists the transmit-and-receive procedure using the polling method. The MCSPI is acting as master and slave.

Table 23-284. Transmit-and-Receive Procedure – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-280.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until transmit/receive word?	SPIm.MCSPI_CHxSTAT[2:0]	=0x3
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.3 Common Transfer Procedures With FIFO – Polling Method

When using FIFO the MCSPI module can start the transfer only after the first write request is released by writing the MCSPI_TXx register. The first write request can be managed by the IRQ routine or DMA handler. The end of transfer is more complex and depends on the transfer type. See Table 23-283 through Table 23-290.

23.4.5.1.3.1 Receive-Only Procedure With Word Count – Polling Method

Table 23-285. Receive-Only Procedure With Word Count – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-278.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of word count?	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read from the receiver register.	SPIm.MCSPI_RXx	xxxx

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23.4.5.1.3.2 Transmit-Only Procedure With and Without Word Count – Polling Method

Table 23-286. Transmit-Only Procedure Without Word Count – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-279.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of word count?	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
Wait until end of transfer?	SPIm.MCSPI_CHxSTAT[2] EOT SPIm.MCSPI_CHxSTAT[3] TXFFE	=0x1 =0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.3.3 Transmit-Only Procedure With and Without Word Count – Interrupt Method

Table 23-287. Transmit-Only Procedure With Word Count – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-279.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Enable the interrupt for the transmit register.	SPIm.MCSPI_IRQENABLE[4] TX_EMPTY_ENABLE	0x1
End of word count.	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
End of transfer	SPIm.MCSPI_CHxSTAT[2] EOT SPIm.MCSPI_CHxSTAT[3] TXFFE	=0x1 =0x1
Clear the interrupt.	SPIm.MCSPI_IRQENABLE[17] EOW_ENABLE	=0x0
Disable the interrupt for the transmit register.	SPIm.MCSPI_IRQENABLE[4] TX_EMPTY_ENABLE	0x0
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0

23.4.5.1.3.4 Transmit-and-Receive Procedure With Word Count – Polling Method

Table 23-288. Transmit-and-Receive Procedure With Word Count – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-280.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of word count?	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read from the receiver register.	SPIm.MCSPI_RXx	xxxx

23.4.5.1.3.5 Transmit-and-Receive Procedure With Word Count – Interrupt Method

Table 23-289. Transmit-and-Receive Procedure With Word Count – Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-280.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Enable the interrupt for the receiver register.	SPIm.MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0x1
Enable the interrupt for the transmit register.	SPIm.MCSPI_IRQENABLE[4] TX_EMPTY_ENABLE	0x1
End of word count?	SPIm.MCSPI_IRQSTATUS[17] EOW	=0x1
Clear the interrupt.	SPIm.MCSPI_IRQENABLE[17] EOW_ENABLE	=0x0

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Table 23-289. Transmit-and-Receive Procedure With Word Count – Interrupt Method (continued)

Step	Register/Bit Field/Programming Model	Value
Disable the interrupt for the receiver register.	SPIm.MCSPI_IRQENABLE[4] TX_EMPTY_ENABLE	0x0
Disable the interrupt for the transmit register.	SPIm.MCSPI_IRQENABLE[2] RX_FULL_ENABLE	0x0
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read from the receiver register.	SPIm.MCSPI_RXx	xxxx

23.4.5.1.3.6 Transmit-and-Receive Procedure Without Word Count – Polling Method

Table 23-290. Transmit-and-Receive Procedure Without Word Count – Polling Method

Step	Register/Bit Field/Programming Model	Value
Configure the channel according to the mode.	See Table 23-280.	
Start the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x1
Wait until end of transfer?	SPIm.MCSPI_CHxSTAT[2] EOT SPIm.MCSPI_CHxSTAT[3] TXFFE	=0x1 =0x1
Stop the channel.	SPIm.MCSPI_CHxCTRL[0] EN	0x0
Read from the receiver register.	SPIm.MCSPI_RXx	xxxx

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23.4.6 MCSPI Register Manual

23.4.6.1 MCSPI Instance Summary

Table 23-291. MCSPI Instance Summary

Module Name	Base Address	Size
MCSPI1	0x4809 8000	4 KiB
MCSPI2	0x4809 A000	4 KiB
MCSPI3	0x480B 8000	4 KiB
MCSPI4	0x480B A000	4 KiB

23.4.6.2 MCSPI Registers

23.4.6.2.1 MCSPI Register Summary

Table 23-292 lists the MCSPI registers. Each register is 32 bits wide.

Table 23-292. MCSPI Register Summary

Register	Type	Offset Address	MCSPI1 L3 Physical Address	MCSPI2 L3 Physical Address	MCSPI3 L3 Physical Address	MCSPI4 L3 Physical Address
MCSPI_HL_REV	Rw	0x00	0x4809 8000	0x4809 A000	0x480B 8000	0x480B A000
MCSPI_HL_HWINFO	Rw	0x04	0x4809 8004	0x4809 A004	0x480B 8004	0x480B A004
MCSPI_HL_SYSCONFIG	Rw	0x10	0x4809 8010	0x4809 A010	0x480B 8010	0x480B A010
MCSPI_REVISION	R	0x100	0x4809 8100	0x4809 A100	0x480B 8100	0x480B A100
MCSPI_SYSCONFIG	RW	0x110	0x4809 8110	0x4809 A110	0x480B 8110	0x480B A110
MCSPI_SYSSTATUS	R	0x114	0x4809 8114	0x4809 A114	0x480B 8114	0x480B A114
MCSPI_IRQSTATUS	RW	0x118	0x4809 8118	0x4809 A118	0x480B 8118	0x480B A118
MCSPI_IRQENABLE	RW	0x1C	0x4809 811C	0x4809 A11C	0x480B 811C	0x480B A11C
MCSPI_WAKEUPENABLE	RW	0x120	0x4809 8120	0x4809 A120	0x480B 8120	0x480B A120
MCSPI_SYST	RW	0x124	0x4809 8124	0x4809 A124	0x480B 8124	0x480B A124
MCSPI_MODULCTRL	RW	0x128	0x4809 8128	0x4809 A128	0x480B 8128	0x480B A128
MCSPI_CHxCONF (1)	RW	0x12C + (0x14 * x)	0x4809 812C + (0x14 * x)	0x4809 A12C + (0x14 * x)	0x480B 812C + (0x14 * x)	0x480B A12C + (0x14 * x)
MCSPI_CHxSTAT (1)	R	0x130 + (0x14 * x)	0x4809 8130 + (0x14 * x)	0x4809 A130 + (0x14 * x)	0x480B 8130 + (0x14 * x)	0x480B A130 + (0x14 * x)
MCSPI_CHxCTRL (1)	RW	0x134 + (0x14 * x)	0x4809 8134 + (0x14 * x)	0x4809 A134 + (0x14 * x)	0x480B 8134 + (0x14 * x)	0x480B A134 + (0x14 * x)
MCSPI_TXx (1)	RW	0x138 + (0x14 * x)	0x4809 8138 + (0x14 * x)	0x4809 A138 + (0x14 * x)	0x480B 8138 + (0x14 * x)	0x480B A138 + (0x14 * x)
MCSPI_RXx (1)	R	0x13C + (0x14 * x)	0x4809 813C + (0x14 * x)	0x4809 A13C + (0x14 * x)	0x480B 813C + (0x14 * x)	0x480B A13C + (0x14 * x)
MCSPI_XFERLEVEL	RW	0x17C	0x4809 817C	0x4809 A17C	0x480B 817C	0x480B A17C

(1) x = 0 to 3 for MCSPI1
x = 0 to 1 for MCSPI2
x = 0 for MCSPI3
x = 0 for MCSPI4

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23.4.6.2.2 MCSPI Register Description

Table 23-293 through Table 23-325 describe the individual MCSPI register bits.

Table 23-293. MCSPI_HL_REV

Address Offset	0x00		
Physical Address	0x4809 8000 0x4809 A000 0x480B 8000 0x480B A000	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 23-294. Register Call Summary for Register MCSPI_HL_REV

Multichannel Serial Port Interface

- MCSPI Register Summary: [0]

Table 23-295. MCSPI_HL_HWINFO

Address Offset	0x04		
Physical Address	0x4809 8004 0x4809 A004 0x480B 8004 0x480B A004	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	Information about the IP module's hardware configuration, that is, typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																								RETMODE	FFNBYTE						USEFIFO

Bits	Field Name	Description	Type	Reset
31:7	RSVD	Reserved These bits are initialized to 0, and writes to them are ignored.	R	0x0000000
6	RETMODE	Retention Mode generic parameter. This bit field indicates whether the retention mode is supported using the pin PIRFFRET. 0x0: Retention mode disabled 0x1: Retention mode enabled	R	RETMODE

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Bits	Field Name	Description	Type	Reset
5:1	FFNBYTE	FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account. Read 0x1: FIFO 16 bytes depth Read 0x2: FIFO 32 bytes depth Read 0x4: FIFO 64 bytes depth Read 0x8: FIFO 128 bytes depth Read 0x10: FIFO 256 bytes depth	R	0x04
0	USEFIFO	Use of a FIFO enable: This bit indicates if a FIFO is integrated within controller design with its management. Read 0x0: FIFO not implemented in design Read 0x1: FIFO and its management implemented in design with depth defined by FFNBYTE generic	R	0

Table 23-296. Register Call Summary for Register MCSPI_HL_HWINFO

Multichannel Serial Port Interface

- MCSPI Register Summary: [0]

Table 23-297. MCSPI_HL_SYSCONFIG

Address Offset	0x10		
Physical Address	0x4809 8010 0x4809 A010 0x480B 8010 0x480B A010	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																												IDLEMODE		FREEEMU	SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:4	RSVD		R	0x0000000
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's IDLE state follows (acknowledges) the system's IDLE requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters IDLE state. Backup mode, for debug only. 0x2: Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's IDLE requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Smart-idle wake-up-capable mode: local target's IDLE state eventually follows (acknowledges) the system's IDLE requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state. Mode is relevant only if the appropriate IP module "swake-up" output(s) is (are) implemented.	RW	0x2
1	FREEEMU	Sensitivity to emulation (debug) suspend input signal. 0x0: IP module is sensitive to emulation suspend. 0x1: IP module is not sensitive to emulation suspend.	RW	0
0	SOFTRESET	Software reset. (Optional) Write 0x0: No action Read 0x0: Reset done, no pending action Read 0x1: Reset (software or other) ongoing Write 0x1: Initiate software reset	RW	0

Table 23-298. Register Call Summary for Register MCSPI_HL_SYSCONFIG

Multichannel Serial Port Interface

- MCSPI Register Summary: [0]

Table 23-299. MCSPI_REVISION

Address Offset	0x100		
Physical Address	0x4809 8100 0x4809 A100 0x480B 8100 0x480B A100	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register contains the revision number.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI Internal data

Table 23-300. Register Call Summary for Register MCSPI_REVISION

Multichannel Serial Port Interface

- MCSPI Register Summary: [0]

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Table 23-301. MCSPI_SYSCONFIG

Address Offset	0x110		
Physical Address	0x4809 8110 0x4809 A110 0x480B 8110 0x480B A110	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register allows controlling various parameters of the OCP interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reads returns 0	RW	0x000000
9:8	CLOCKACTIVITY	Clocks activity during wake-up mode period 0x0: OCP and functional clocks may be switched off. 0x1: OCP clock is maintained. Functional clock may be switched off. 0x2: Functional clock is maintained. OCP clock may be switched off. 0x3: OCP and functional clocks are maintained.	RW	0x0
7:5	RESERVED	Reads returns 0	RW	0x0
4:3	SIDLEMODE	Power management 0x0: If an IDLE request is detected, the McSPI acknowledges it unconditionally and goes in inactive mode. Interrupt, DMA requests and wake-up lines are unconditionally deasserted and the module wake-up capability is deactivated even if the MCSPI_SYSCONFIG[EnaWakeUp] bit is set. 0x1: If an IDLE request is detected, the request is ignored and the module does not switch to wake-up mode, and keeps on behaving normally. 0x2: If an IDLE request is detected, the module will switch to wake-up mode based on its internal activity, and the wake-up capability can be used if the bit MCSPI_SYSCONFIG[EnaWakeUp] is set. 0x3: Reserved - do not use.	RW	0x2
2	ENAWAKEUP	Wake-up feature control 0x0: Wake-up capability is disabled. 0x1: Wake-up capability is enabled.	RW	1
1	SOFTRESET	Software reset. During reads it always returns 0. 0x0: (write) Normal mode 0x1: (write) Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware.	RW	0
0	AUTOIDLE	Internal OCP clock-gating strategy 0x0: OCP clock is free-running. 0x1: Automatic OCP clock gating strategy is applied, based on the OCP interface activity.	RW	1

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Table 23-302. Register Call Summary for Register MCSPI_SYSCONFIG

Multichannel Serial Port Interface

- Normal Mode: [0]
- Idle Mode: [1]
- Wake-Up Event in Smart-Idle Mode: [2]
- Force-Idle Mode: [3] [4]
- MCSPI Global Initialization: [5]
- MCSPI Register Summary: [6]
- MCSPI Register Description: [7] [8]

Table 23-303. MCSPI_SYSSTATUS

Address Offset	0x114		
Physical Address	0x4809 8114 0x4809 A114 0x480B 8114 0x480B A114	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register provides status information about the module excluding the interrupt status information.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE
R-0																															R-0

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved for module specific status information. Read returns 0.	R	0x0000 0000
0	RESETDONE	Internal reset monitoring Read 0x0: Internal module reset is ongoing Read 0x1: Reset completed	R	0

Table 23-304. Register Call Summary for Register MCSPI_SYSSTATUS

Multichannel Serial Port Interface

- MCSPI Global Initialization: [0]
- MCSPI Register Summary: [1]

Table 23-305. MCSPI_IRQSTATUS

Address Offset	0x118		
Physical Address	0x4809 8118 0x4809 A118 0x480B 8118 0x480B A118	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	The interrupt status regroups all the status of the module internal events that can generate an interrupt.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EOW	WKS	RESERVED	RX3_FULL	TX3_UNDERFLOW	TX3_EMPTY	RESERVED	RX2_FULL	TX2_UNDERFLOW	TX2_EMPTY	RESERVED	RX1_FULL	TX1_UNDERFLOW	TX1_EMPTY	RX0_OVERFLOW	RX0_FULL	TX0_UNDERFLOW	TX0_EMPTY

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reads returns 0	RW	0x0000
17	EOW	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT]. Write 0x0: w:Event status bit unchanged Read 0x0: r: Event false Read 0x1: r: Event is pending Write 0x1: w:Event status bit is reset	RW W1toClr	0
16	WKS	Wake-up event in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
15	RESERVED	Reads returns 0	RW	0
14	RX3_FULL	Receiver register is full or almost full. Only when Channel 3 is enabled Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
13	TX3_UNDERFLOW	Transmitter register underflow. Only when Channel 3 is enabled. The transmitter register is empty (not updated by host or DMA with new data) before its time slot assignment. Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled. Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
12	TX3_EMPTY	Transmitter register is empty or almost empty. Note: Enabling the channel automatically rises this event. Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
11	RESERVED	Reads returns 0.	RW	0

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Bits	Field Name	Description	Type	Reset
10	RX2_FULL	Receiver register full or almost full. Channel 2 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
9	TX2_UNDERFLOW	Transmitter register underflow. Channel 2 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
8	TX2_EMPTY	Transmitter register empty or almost empty. Channel 2 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
7	RESERVED	Reads returns 0	RW	0
6	RX1_FULL	Receiver register full or almost full. Channel 1 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
5	TX1_UNDERFLOW	Transmitter register underflow. Channel 1 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
4	TX1_EMPTY	Transmitter register empty or almost empty. Channel 1 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
3	RX0_OVERFLOW	Receiver register overflow (slave mode only). Channel 0 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
2	RX0_FULL	Receiver register full or almost full. Channel 0 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0
1	TX0_UNDERFLOW	Transmitter register underflow. Channel 0 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	TX0_EMPTY	Transmitter register empty or almost empty. Channel 0 Read 0x0: r: Event false Write 0x0: w:Event status bit unchanged Write 0x1: w:Event status bit is reset Read 0x1: r: Event is pending	RW W1toClr	0

Table 23-306. Register Call Summary for Register MCSPI_IRQSTATUS

Multichannel Serial Port Interface

- Master Transmit-and-Receive Mode (Full Duplex): [0]
- Master Transmit-Only Mode (Half Duplex): [1]
- Master Receive-Only Mode (Half Duplex): [2] [3] [4] [5]
- Force mcspim_csx Mode: [6]
- Turbo Mode: [7]
- Buffer Almost Full: [8] [9]
- Buffer Almost Empty: [10] [11]
- End of Transfer Management: [12]
- Interrupts: [13]
- TXx_EMPTY: [14] [15]
- TXx_UNDERFLOW: [16]
- RXx_ FULL: [17]
- End Of Word Count: [18] [19]
- Interrupt Events in Slave Mode: [20]
- TXx_EMPTY: [21]
- TXx_UNDERFLOW: [22]
- RXx_FULL: [23]
- RX0_OVERFLOW: [24]
- End Of Word Count: [25] [26]
- Interrupt-Driven Operation: [27] [28]
- Polling: [29] [30]
- Transitions From Smart-Idle Mode to Normal Mode: [31] [32]
- Force-Idle Mode: [33]
- MCSPI Operational Modes: [34] [35] [36] [37]
- Receive-Only Procedure With Word Count – Polling Method: [38]
- Transmit-Only Procedure With and Without Word Count – Polling Method: [39]
- Transmit-Only Procedure With and Without Word Count – Interrupt Method: [40]
- Transmit-and-Receive Procedure With Word Count – Polling Method: [41]
- Transmit-and-Receive Procedure With Word Count – Interrupt Method: [42]
- MCSPI Register Summary: [43]
- MCSPI Register Description: [44] [45] [46]

Table 23-307. MCSPI_IRQENABLE

Address Offset	0x11C		
Physical Address	0x4809 811C 0x4809 A11C 0x480B 811C 0x480B A11C	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register allows enabling/disabling of the module internal sources of interrupt, on an event-by-event basis.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EOW_ENABLE	WKE	RESERVED	RX3_FULL_ENABLE	TX3_UNDERFLOW_ENABLE	TX3_EMPTY_ENABLE	RESERVED	RX2_FULL_ENABLE	TX2_UNDERFLOW_ENABLE	TX2_EMPTY_ENABLE	RESERVED	RX1_FULL_ENABLE	TX1_UNDERFLOW_ENABLE	TX1_EMPTY_ENABLE	RX0_OVERFLOW_ENABLE	RX0_FULL_ENABLE	TX0_UNDERFLOW_ENABLE	TX0_EMPTY_ENABLE

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reads return 0.	RW	0x0000
17	EOW_ENABLE	End of Word count Interrupt Enable. 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
16	WKE	Wake-up event interrupt enable in slave mode when an active control signal is detected on the SPIEN line programmed in the MCSPI_CH0CONF[SPIENSLV] bit 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
15	RESERVED	Reads returns 0.	RW	0
14	RX3_FULL_ENABLE	Receiver register Full Interrupt Enable. Channel 3 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
13	TX3_UNDERFLOW_ENABLE	Transmitter register Underflow Interrupt Enable. Channel 3 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
12	TX3_EMPTY_ENABLE	Transmitter register Empty Interrupt Enable. Channel 3 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
11	RESERVED	Reads return 0.	RW	0
10	RX2_FULL_ENABLE	Receiver register Full Interrupt Enable. Channel 2 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
9	TX2_UNDERFLOW_ENABLE	Transmitter register Underflow Interrupt Enable. Channel 2 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
8	TX2_EMPTY_ENABLE	Transmitter register Empty Interrupt Enable. Channel 2 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
7	RESERVED	Reads return 0.	RW	0
6	RX1_FULL_ENABLE	Receiver register Full Interrupt Enable. Channel 1 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
5	TX1_UNDERFLOW_ENABLE	Transmitter register Underflow Interrupt Enable. Channel 1 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
4	TX1_EMPTY_ENABLE	Transmitter register Empty Interrupt Enable. Channel 1 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
3	RX0_OVERFLOW_ENABLE	Receiver register Overflow Interrupt Enable. Channel 0 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
2	RX0_FULL_ENABLE	Receiver register Full Interrupt Enable. Channel 0 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
1	TX0_UNDERFLOW_ENABLE	Transmitter register Underflow Interrupt Enable. Channel 0 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
0	TX0_EMPTY_ENABLE	Transmitter register Empty Interrupt Enable. Channel 0 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0

Table 23-308. Register Call Summary for Register MCSPI_IRQENABLE

Multichannel Serial Port Interface

- Interrupts: [0]
- Interrupt-Driven Operation: [1]
- Polling: [2]
- Transitions From Smart-Idle Mode to Normal Mode: [3] [4]
- MCSPI Operational Modes: [5] [6]
- Transmit-Only Procedure With and Without Word Count – Interrupt Method: [7] [8] [9]
- Transmit-and-Receive Procedure With Word Count – Interrupt Method: [10] [11] [12] [13] [14]
- MCSPI Register Summary: [15]

Table 23-309. MCSPI_WAKEUPENABLE

Address Offset	0x120		
Physical Address	0x4809 8120 0x4809 A120 0x480B 8120 0x480B A120	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	The wake-up enable register allows enabling and disabling of the module internal sources of wakeup on event-by-event basis.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															WKEN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads returns 0.	RW	0x0000 0000
0	WKEN	Wake-up functionality in slave mode when an active control signal is detected on the SPIEN line programmed in the MCSPI_CH0CONF[SPIENSLV] bit 0x0: The event is not allowed to wake-up the system, even if the global control bit MCSPI_SYSCONF[EnaWakeUp] is set. 0x1: The event is allowed to wake-up the system if the global control bit MCSPI_SYSCONF[EnaWakeUp] is set.	RW	0

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Table 23-310. Register Call Summary for Register MCSPI_WAKEUPENABLE

Multichannel Serial Port Interface

- Wake-Up Event in Smart-Idle Mode: [0]
- Transitions From Smart-Idle Mode to Normal Mode: [1]
- Force-Idle Mode: [2]
- MCSPI Register Summary: [3]

Table 23-311. MCSPI_SYST

Address Offset	0x124		
Physical Address	0x4809 8124 0x4809 A124 0x480B 8124 0x480B A124	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device I/O pads, when the module is configured in system test (SYSTEST) mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0	WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reads returns 0.	RW	0x00000
11	SSB	Set status bit 0x0: No action. Writing 0 does not clear already set status bits. This bit must be cleared before trying to clear a status bit of the <MCSPI_IRQSTATUS> register. 0x1: Force to 1 all status bits of MCSPI_IRQSTATUS register. Writing 1 into this bit sets to 1 all status bits in the <MCSPI_IRQSTATUS> register.	RW	0
10	SPIENDIR	Set the direction of the SPIEN[3:0] lines and SPICLK line. 0x0: Output (as in master mode) 0x1: Input (as in slave mode)	RW	0
9	SPIDATDIR1	Set the direction of the SPIDAT[1]. 0x0: Output 0x1: Input	RW	0
8	SPIDATDIR0	Set the direction of the SPIDAT[0]. 0x0: Output 0x1: Input	RW	0
7	WAKD	SWAKEUP output (signal data value of internal signal to system). The signal is driven high or low according to the value written into this register bit. 0x0: The pin is driven low. 0x1: The pin is driven high.	RW	0

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Bits	Field Name	Description	Type	Reset
6	SPICLK	SPICLK line (signal data value) If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the CLKSPI line (high or low), and a write into this bit has no effect. If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the CLKSPI line is driven high or low according to the value written into this register.	RW	0
5	SPIDAT_1	SPIDAT[1] line (signal data value) If MCSPI_SYST[SPIDATDIR1] = 0 (output mode direction), the SPIDAT[1] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIDATDIR1] = 1 (input mode direction), this bit returns the value on the SPIDAT[1] line (high or low), and a write into this bit has no effect.	RW	0
4	SPIDAT_0	SPIDAT[0] line (signal data value) If MCSPI_SYST[SPIDATDIR0] = 0 (output mode direction), the SPIDAT[0] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIDATDIR0] = 1 (input mode direction), this bit returns the value on the SPIDAT[0] line (high or low), and a write into this bit has no effect.	RW	0
3	SPIEN_3	SPIEN[3] line (signal data value) If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the SPIENT[3] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the SPIEN[3] line (high or low), and a write into this bit has no effect.	RW	0
2	SPIEN_2	SPIEN[2] line (signal data value) If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the SPIENT[2] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the SPIEN[2] line (high or low), and a write into this bit has no effect.	RW	0
1	SPIEN_1	SPIEN[1] line (signal data value) If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the SPIENT[1] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the SPIEN[1] line (high or low), and a write into this bit has no effect.	RW	0
0	SPIEN_0	SPIEN[0] line (signal data value) If MCSPI_SYST[SPIENDIR] = 0 (output mode direction), the SPIENT[0] line is driven high or low according to the value written into this register. If MCSPI_SYST[SPIENDIR] = 1 (input mode direction), this bit returns the value on the SPIEN[0] line (high or low), and a write into this bit has no effect.	RW	0

Table 23-312. Register Call Summary for Register MCSPI_SYST

Multichannel Serial Port Interface

- MCSPI Register Summary: [0]
- MCSPI Register Description: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Table 23-313. MCSPI_MODULCTRL

Address Offset	0x128		
Physical Address	0x4809 8128 0x4809 A128 0x480B 8128 0x480B A128	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register is dedicated to the configuration of the serial port interface.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FDAA	MOA	INITDLY			SYSTEM_TEST	MS	PIN34	SINGLE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reads returns 0.	RW	0x000000
8	FDAA	FIFO DMA address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256-bit aligned address. If this bit is set the enabled channel which uses the FIFO has its data managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX(i) and MCSPI_RX(i) registers. 0x0: FIFO data managed by MCSPI_TX(i) and MCSPI_RX(i) registers. 0x1: FIFO data managed by MCSPI_DAFTX and MCSPI_DAFRX registers.	RW	0
7	MOA	Multiple word OCP access: This register can only be used when a channel is enabled using a FIFO. It allows the system to perform multiple SPI word access for a single 32-bit OCP word access. This is possible for WL < 16. 0x0: Multiple word access disabled 0x1: Multiple word access enabled with FIFO	RW	0
6:4	INITDLY	Initial SPI delay for first transfer: This register is an option only available in SINGLE master mode. The controller waits for a delay to transmit the first SPI word after channel enabled and corresponding TX register filled. This delay is based on SPI output frequency clock. No clock output provided to the boundary and chip select is not active in 4-pin mode within this period. 0x0: No delay for first spi transfer. 0x1: The controller wait 4 SPI bus clock 0x2: The controller wait 8 SPI bus clock 0x3: The controller wait 16 SPI bus clock 0x4: The controller wait 32 SPI bus clock	RW	0x0
3	SYSTEM_TEST	Enables the system test mode 0x0: Functional mode 0x1: System test mode (SYSTEST)	RW	0
2	MS	Master/slave 0x0: Master - The module generates the SPICLK and SPIEN[3:0]. 0x1: Slave - The module receives the SPICLK and SPIEN[3:0].	RW	1
1	PIN34	Pin mode selection: This register is used to configure the SPI pin mode, in master or slave mode. If asserted the controller only use SIMO, SOMI, and SPICLK clock pin for SPI transfers. 0x0: SPIEN is used as a chip-select. 0x1: SPIEN is not used. In this mode all related options to chip-select have no meaning.	RW	0

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Bits	Field Name	Description	Type	Reset
0	SINGLE	Single channel/Multi Channel (master mode only) 0x0: More than one channel will be used in master mode. 0x1: Only one channel will be used in master mode. This bit must be set in Force SPIEN mode.	RW	0

Table 23-314. Register Call Summary for Register MCSPI_MODULCTRL

Multichannel Serial Port Interface

- Single-Channel Master Mode: [0] [1]
- Force mcspim_csx Mode: [2] [3]
- Chip-Select Timing Control: [4]
- Slave Mode: [5]
- MCSPI Operational Modes: [6] [7] [8]
- MCSPI Register Summary: [9]

Table 23-315. MCSPI_CHxCONF

Address Offset	0x12C + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	0x4809 812C + (0x14 * x) 0x4809 A12C + (0x14 * x) 0x480B 812C + (0x14 * x) 0x480B A12C + (0x14 * x)	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register is dedicated to the configuration of the channel 0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		CLKG	FFER	FFEW	TCS0		SBPOL	SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0	DMAR	DMAW	TRM		WL				EPOL	CLKD					POL	PHA

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Read returns 0.	R	0x0
29	CLKG	Clock divider granularity This register defines the granularity of channel clock divider: power of 2 or one clock cycle granularity. When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio. Then the clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0x0: Clock granularity of power of 2 0x1: One clock cycle granularity	RW	0
28	FFER	FIFO enabled for receive: Only one channel can have this bit field set. 0x0: The buffer is not used to receive data. 0x1: The buffer is used to receive data.	RW	0
27	FFEW	FIFO enabled for transmit: Only one channel can have this bit field set. 0x0: The buffer is not used to transmit data. 0x1: The buffer is used to transmit data.	RW	0

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Bits	Field Name	Description	Type	Reset
26:25	TCS0	Chip-select time control This 2-bit field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock. 0x0: 0.5 clock cycle 0x1: 1.5 clock cycles 0x2: 2.5 clock cycles 0x3: 3.5 clock cycles	RW	0x0
24	SBPOL	Start-bit polarity 0x0: Start-bit polarity is held to 0 during SPI transfer. 0x1: Start-bit polarity is held to 1 during SPI transfer.	RW	0
23	SBE	Start-bit enable for SPI transfer 0x0: Default SPI transfer length as specified by WL bit field 0x1: Start bit D/CX added before SPI transfer polarity is defined by MCSPI_CH0CONF[SBPOL]	RW	0
22:21	SPIENSLV	Channel 0 only and slave mode only: SPI slave select signal detection. Reserved bits for other cases. 0x0: Detection enabled only on SPIEN[0] 0x1: Detection enabled only on SPIEN[1] 0x2: Detection enabled only on SPIEN[2] 0x3: Detection enabled only on SPIEN[3]	RW	0x0
20	FORCE	Manual SPIEN assertion to keep SPIEN active between SPI words (single channel master mode only). 0x0: Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF(i)[EPOL]=0, and drives it high when MCSPI_CHCONF(i)[EPOL]=1. 0x1: Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF(i)[EPOL]=0, and drives it low when MCSPI_CHCONF(i)[EPOL]=1.	RW	0
19	TURBO	Turbo mode 0x0: Turbo is deactivated (recommended for single SPI word transfer). 0x1: Turbo is activated to maximize the throughput for multiple SPI words transfer.	RW	0
18	IS	Input Select 0x0: Data line 0 (SPIDAT[0]) selected for reception 0x1: Data line 1 (SPIDAT[1]) selected for reception	RW	1
17	DPE1	Transmission enable for data line 1 (SPIDATAGZEN[1]) 0x0: Data line 1 (SPIDAT[1]) selected for transmission 0x1: No transmission on Data Line1 (SPIDAT[1])	RW	1
16	DPE0	Transmission Enable for data line 0 (SPIDATAGZEN[0]) 0x0: Data Line0 (SPIDAT[0]) selected for transmission 0x1: No transmission on data line 0 (SPIDAT[0])	RW	0
15	DMAR	DMA read request The DMA read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel. The DMA read request line is deasserted on read completion of the receive register of the channel. 0x0: DMA read request disabled 0x1: DMA read request enabled	RW	0

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Bits	Field Name	Description	Type	Reset
14	DMAW	DMA write request. The DMA write request line is asserted when The channel is enabled and the transmitter register of the channel is empty. The DMA write request line is deasserted on load completion of the transmitter register of the channel. 0x0: DMA write request disabled 0x1: DMA write request enabled	RW	0
13:12	TRM	Transmit/receive modes 0x0: Transmit-and-receive mode 0x1: Receive-only mode 0x2: Transmit-only mode 0x3: Reserved	RW	0x0
11:7	WL	SPI word length 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: The SPI word is 4 bits long 0x4: The SPI word is 5 bits long 0x5: The SPI word is 6 bits long 0x6: The SPI word is 7 bits long 0x7: The SPI word is 8 bits long 0x8: The SPI word is 9 bits long 0x9: The SPI word is 10 bits long 0xA: The SPI word is 11 bits long 0xB: The SPI word is 12 bits long 0xC: The SPI word is 13 bits long 0xD: The SPI word is 14 bits long 0xE: The SPI word is 15 bits long 0xF: The SPI word is 16 bits long 0x10: The SPI word is 17 bits long 0x11: The SPI word is 18 bits long 0x12: The SPI word is 19 bits long 0x13: The SPI word is 20 bits long 0x14: The SPI word is 21 bits long 0x15: The SPI word is 22 bits long 0x16: The SPI word is 23 bits long 0x17: The SPI word is 24 bits long 0x18: The SPI word is 25 bits long 0x19: The SPI word is 26 bits long 0x1A: The SPI word is 27 bits long 0x1B: The SPI word is 28 bits long 0x1C: The SPI word is 29 bits long 0x1D: The SPI word is 30 bits long 0x1E: The SPI word is 31 bits long 0x1F: The SPI word is 32 bits long	RW	0x00
6	EPOL	SPIEN polarity 0x0: SPIEN is held high during the ACTIVE state. 0x1: SPIEN is held low during the ACTIVE state.	RW	0

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Bits	Field Name	Description	Type	Reset
5:2	CLKD	Frequency divider for SPICLK (only when the module is a Master SPI device). A programmable clock divider divides the SPI reference clock (CLKSPIREF) with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data. By default the clock divider ratio has a power of 2 granularity when MCSPI_CHCONF[CLKG] is cleared. Otherwise this register is the 4-LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] register. The value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0. 0x0: 1 0x1: 2 0x2: 4 0x3: 8 0x4: 16 0x5: 32 0x6: 64 0x7: 128 0x8: 256 0x9: 512 0xA: 1024 0xB: 2048 0xC: 4096 0xD: 8192 0xE: 16384 0xF: 32768	RW	0x0
1	POL	SPICLK polarity, see Section 23.4.2.1.3.1, *Transfer Format*. 0x0: SPICLK is held low during the INACTIVE state 0x1: SPICLK is held high during the INACTIVE state	RW	0
0	PHA	SPICLK phase, see Section 23.4.2.1.3.1, *Transfer Format*. 0x0: Data are latched on odd-numbered edges of SPICLK. 0x1: Data are latched on even-numbered edges of SPICLK.	RW	0

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Table 23-316. Register Call Summary for Register MCSPI_CHxCONF

Multichannel Serial Port Interface

- Multichannel SPI Protocol and Data Format: [0] [1] [2] [3] [4] [5] [6] [7]
- Transfer Format: [8]
- SPI in Slave Mode: [9]
- Master Transmit-and-Receive Mode (Full Duplex): [10]
- Master Transmit-Only Mode (Half Duplex): [11]
- Master Receive-Only Mode (Half Duplex): [12]
- Single-Channel Master Mode: [13]
- Force mcspim_csx Mode: [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]
- Turbo Mode: [24]
- Start-Bit Mode: [25] [26] [27] [28]
- Chip-Select Timing Control: [29]
- Programmable SPI Clock (mcspim_clk): [30]
- Clock Ratio Granularity: [31] [32] [33] [34] [35]
- Dedicated Resources: [36] [37] [38] [39] [40] [41]
- Slave Transmit-and-Receive Mode: [42]
- Slave Transmit-Only Mode: [43]
- Slave Receive-Only Mode: [44]
- FIFO Buffer Management: [45] [46] [47]
- Buffer Almost Full: [48] [49]
- Buffer Almost Empty: [50] [51]
- TXx_EMPTY: [52]
- RXx_ FULL: [53]
- TXx_EMPTY: [54]
- RXx_FULL: [55]
- DMA Requests: [56] [57]
- Wake-Up Event in Smart-Idle Mode: [58]
- MCSPI Operational Modes: [59] [60] [61] [62] [63] [64] [65] [66] [67] [68] [69] [70] [71] [72] [73] [74]
- MCSPI Register Summary: [75]

Table 23-317. MCSPI_CHxSTAT

Address Offset	0x130 + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	0x4809 8130 + (0x14 * x) 0x4809 A130 + (0x14 * x) 0x480B 8130 + (0x14 * x) 0x480B A130 + (0x14 * x)	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register provides status information about transmitter and receiver registers of channel 0.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Read returns 0.	R	0x0000000
6	RXFFF	Channel "i" FIFO receive buffer full status Read 0x0: FIFO receive buffer is not full Read 0x1: FIFO receive buffer is full	R	0
5	RXFFE	Channel "i" FIFO receive buffer empty status Read 0x0: FIFO receive buffer is not empty Read 0x1: FIFO receive buffer is empty	R	0

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Bits	Field Name	Description	Type	Reset
4	TXFFF	Channel "i" FIFO transmit buffer full status Read 0x0: FIFO transmit buffer is not full Read 0x1: FIFO transmit buffer is full	R	0
3	TXFFE	Channel "i" FIFO transmit buffer empty status Read 0x0: FIFO transmit buffer is not empty Read 0x1: FIFO transmit buffer is empty	R	0
2	EOT	Channel "i" end of transfer status. The definitions of beginning and end of transfer vary with master versus slave and the transfer format (transmit/receive modes, turbo mode). See dedicated chapters for details. Read 0x0: This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). Read 0x1: This flag is automatically set to one at the end of an SPI transfer.	R	0
1	TXS	Channel "i" transmitter register status Read 0x0: Register is full. Read 0x1: Register is empty.	R	0
0	RXS	Channel "i" receiver register status Read 0x0: Register is empty. Read 0x1: Register is full.	R	0

Table 23-318. Register Call Summary for Register MCSPI_CHxSTAT

Multichannel Serial Port Interface

- Master Transmit-and-Receive Mode (Full Duplex): [0] [1] [2]
- Master Transmit-Only Mode (Half Duplex): [3]
- Master Receive-Only Mode (Half Duplex): [4]
- Programming Tips When Switching to Another Channel: [5]
- Force mcspim_csx Mode: [6] [7] [8]
- Turbo Mode: [9]
- Dedicated Resources: [10] [11]
- Slave Transmit-and-Receive Mode: [12]
- Slave Transmit-Only Mode: [13]
- Slave Receive-Only Mode: [14]
- End of Transfer Management: [15]
- MCSPI Operational Modes: [16] [17]
- Transmit-Only Procedure With and Without Word Count – Polling Method: [18] [19]
- Transmit-Only Procedure With and Without Word Count – Interrupt Method: [20] [21]
- Transmit-and-Receive Procedure Without Word Count – Polling Method: [22] [23]
- MCSPI Register Summary: [24]

Table 23-319. MCSPI_CHxCTRL

Address Offset	0x134 + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	0x4809 8134 + (0x14 * x) 0x4809 A134 + (0x14 * x) 0x480B 8134 + (0x14 * x) 0x480B A134 + (0x14 * x)	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register is dedicated to enable channel 0.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EXTCLK								RESERVED							EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Read returns 0.	RW	0x0000
15:8	EXTCLK	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle (MCSPI_CHCONF[CLKG] set to 1). Then the maximum value reached is 4096 clock divider ratio. 0x0: Clock ratio is CLKD + 1. 0x1: Clock ratio is CLKD + 1 + 16. 0xFF: Clock ratio is CLKD + 1 + 4080.	RW	0x00
7:1	RESERVED	Read returns 0.	RW	0x00
0	EN	Channel enable 0x0: Channel "i" is not active. 0x1: Channel "i" is active.	RW	0

Table 23-320. Register Call Summary for Register MCSPI_CHxCTRL

Multichannel Serial Port Interface

- Master Transmit-and-Receive Mode (Full Duplex): [0]
- Force mcspim_csx Mode: [1] [2]
- Clock Ratio Granularity: [3]
- Dedicated Resources: [4] [5]
- MCSPI Operational Modes: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]
- Receive-Only Procedure With Word Count – Polling Method: [17] [18]
- Transmit-Only Procedure With and Without Word Count – Polling Method: [19] [20]
- Transmit-Only Procedure With and Without Word Count – Interrupt Method: [21] [22]
- Transmit-and-Receive Procedure With Word Count – Polling Method: [23] [24]
- Transmit-and-Receive Procedure With Word Count – Interrupt Method: [25] [26]
- Transmit-and-Receive Procedure Without Word Count – Polling Method: [27] [28]
- MCSPI Register Summary: [29]

Table 23-321. MCSPI_TXx

Address Offset	0x138 + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	0x4809 8138 + (0x14 * x) 0x4809 A138 + (0x14 * x) 0x480B 8138 + (0x14 * x) 0x480B A138 + (0x14 * x)	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA																															

Bits	Field Name	Description	Type	Reset
31:0	TDATA	Channel 0 data to transmit	RW	0x0000 0000

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Table 23-322. Register Call Summary for Register MCSPI_TXx

Multichannel Serial Port Interface

- Master Transmit-and-Receive Mode (Full Duplex): [0] [1] [2] [3]
- Master Transmit-Only Mode (Half Duplex): [4]
- Master Receive-Only Mode (Half Duplex): [5] [6] [7] [8] [9]
- Force mcspim_csx Mode: [10]
- Dedicated Resources: [11] [12] [13] [14] [15]
- Slave Transmit-and-Receive Mode: [16] [17]
- Slave Receive-Only Mode: [18] [19] [20]
- Interrupt Events in Master Mode: [21]
- TXx_EMPTY: [22] [23] [24]
- TXx_UNDERFLOW: [25] [26] [27]
- Interrupt Events in Slave Mode: [28]
- TXx_EMPTY: [29] [30] [31]
- TXx_UNDERFLOW: [32] [33]
- Interrupt-Driven Operation: [34]
- Polling: [35]
- DMA Requests: [36] [37]
- Common Transfer Procedures With FIFO – Polling Method: [38]
- MCSPI Register Summary: [39]

Table 23-323. MCSPI_RXx

Address Offset	0x13C + (0x14 * x)	**Index**	x= 0 to 3 for MCSPI1. x= 0 to 1 for MCSPI2 . x= 0 for MCSPI4 and MCSPI3.
Physical Address	0x4809 813C + (0x14 * x) 0x4809 A13C + (0x14 * x) 0x480B 813C + (0x14 * x) 0x480B A13C + (0x14 * x)	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register contains a single SPI word received through the serial link, what ever SPI word length is.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															

Bits	Field Name	Description	Type	Reset
31:0	RDATA	Channel 0 received data	R	0x0000 0000

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Table 23-324. Register Call Summary for Register MCSPI_RXx

Multichannel Serial Port Interface

- Master Transmit-and-Receive Mode (Full Duplex): [0] [1]
- Master Transmit-Only Mode (Half Duplex): [2] [3] [4]
- Master Receive-Only Mode (Half Duplex): [5] [6]
- Force mcspim_csx Mode: [7] [8]
- Turbo Mode: [9] [10]
- Dedicated Resources: [11] [12] [13]
- Slave Transmit-and-Receive Mode: [14]
- Slave Transmit-Only Mode: [15] [16]
- End of Transfer Management: [17]
- Interrupt Events in Master Mode: [18]
- RXx_ FULL: [19] [20] [21]
- Interrupt Events in Slave Mode: [22]
- RXx_FULL: [23] [24] [25]
- RX0_OVERFLOW: [26] [27]
- Interrupt-Driven Operation: [28]
- Polling: [29]
- DMA Requests: [30]
- Wake-Up Event in Smart-Idle Mode: [31]
- MCSPI Operational Modes: [32] [33]
- Receive-Only Procedure With Word Count – Polling Method: [34]
- Transmit-and-Receive Procedure With Word Count – Polling Method: [35]
- Transmit-and-Receive Procedure With Word Count – Interrupt Method: [36]
- Transmit-and-Receive Procedure Without Word Count – Polling Method: [37]
- MCSPI Register Summary: [38]

Table 23-325. MCSPI_XFERLEVEL

Address Offset	0x17C		
Physical Address	0x4809 817C 0x4809 A17C 0x480B 817C 0x480B A17C	**Instance**	MCSPI1 MCSPI2 MCSPI3 MCSPI4
Description	This register provides transfer levels needed while using FIFO buffer during transfer.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WCNT																AFL								AEL							

Bits	Field Name	Description	Type	Reset
31:16	WCNT	SPI word counter. This register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO buffer. When transfer had started, a read back in this register returns the current SPI word transfer index. 0x0: Counter not used 0x1: One word 0xFFFE: 65534 SPI word 0xFFFF: 65535 SPI word	RW	0x0000

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Bits	Field Name	Description	Type	Reset
15:8	AFL	Buffer almost full This register holds the programmable almost full level value used to determine almost full buffer condition. If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_XFERLEVEL[AFL] must be set with n–1.The size of this register is defined by the generic parameter FFNBYTE. 0x0: 1 byte 0x1: 2 bytes 0xFE: 255bytes 0xFF: 256bytes	RW	0x00
7:0	AEL	Buffer almost empty. This register holds the programmable almost empty level value used to determine almost empty buffer condition. If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_XFERLEVEL[AEL] must be set with – 1. 0x0: 1 byte 0x1: 2 bytes 0xFE: 255 bytes 0xFF: 256bytes	RW	0x00

Table 23-326. Register Call Summary for Register MCSPI_XFERLEVEL

Multichannel Serial Port Interface

- FIFO Buffer Management: [0] [1]
- Buffer Almost Full: [2]
- Buffer Almost Empty: [3]
- End of Transfer Management: [4] [5]
- TXx_EMPTY: [6] [7]
- RXx_ FULL: [8]
- End Of Word Count: [9] [10]
- TXx_EMPTY: [11] [12]
- RXx_FULL: [13]
- End Of Word Count: [14]
- MCSPI Register Summary: [15]
- MCSPI Register Description: [16] [17] [18]

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23.5 Multichannel Buffered Serial Port (MCBSP)

This section introduces the multichannel buffered serial port (MCBSP)

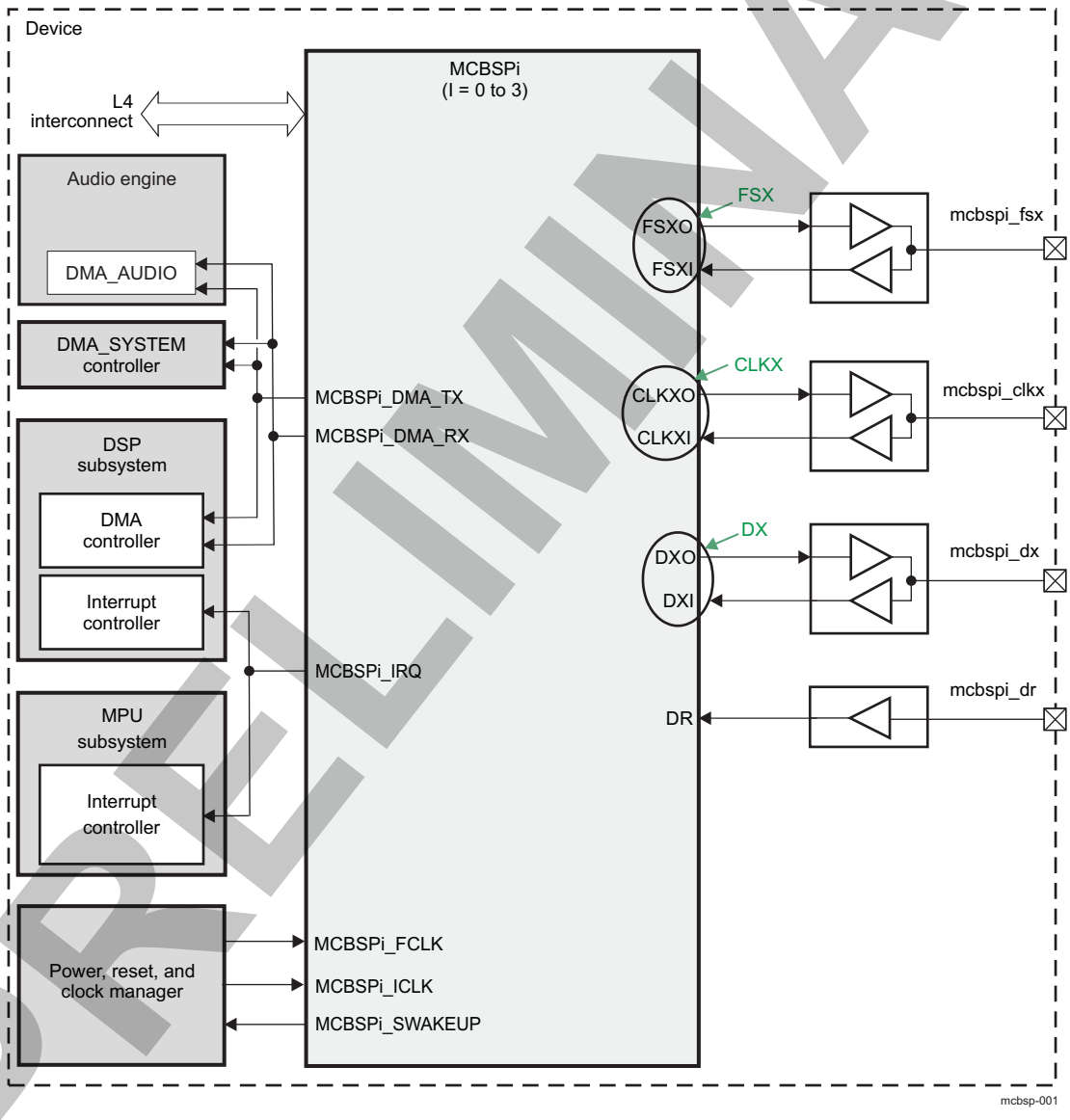
23.5.1 MCBSP Overview

The MCBSP provides a full-duplex direct serial interface between the device and other devices in a system such as other application devices (digital base band), audio and voice codec, etc. Because of its high level of versatility, it can accommodate a wide range of peripherals and clocked frame oriented protocols (for more information, see Section 23.5.1.1, *MCBSP Features*).

The device provides three instances of the MCBSP module.

Figure 23-100 is an overview of the MCBSP in the device.

Figure 23-100. MCBSP Highlight



23.5.1.1 MCBSP Features

The main features of the MCBSP modules are:

- L4 interconnect slave interface supports:

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  - 32-bit data bus width
  - 32-bit access supported
  - 16-/8-bit access not supported
  - 10-bit address bus width
  - Burst mode not supported
  - Write nonposted transaction mode supported
- 128 × 32-bit words (512 bytes) for each buffer for transmit/receive operations
- Transmit and receive direct memory access (DMA) requests triggered with programmable FIFO thresholds
- Serial interface description
  - 4-pin configuration
  - Full-duplex communication
  - Multichannel selection modes
    - Support to enable or block transfers in each channel
    - 128 channels for transmission and reception
  - Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected A/D and D/A devices:
    - Inter-IC sound (I2S™) compliant devices
    - Pulse code modulation (PCM) devices
    - Time division multiplexed (TDM) bus devices

CAUTION

MCBSP modules do not offer support for μ-law and A-law companding, two partitions mode dynamic reassignment, AC'97, and SPI protocol.

  - A wide selection of data sizes: 8, 12, 16, 20, 24, and 32 bits
  - Bit reordering (send/receive least-significant bit [LSB])
- Clock and frame-synchronization generation support:
  - Independent clocking and framing for reception and for transmission up to 48 MHz
  - Support for external generation of clock signals and frame-synchronization (frame-sync) signals
  - A programmable sample rate generator (SRG) for internal generation and control of clock signals and frame-sync signals
  - Programmable polarity for frame-sync pulses and clock signals

NOTE:

- MCBSP modules do not support features such as retransmit or re-receive of an erroneous frame or word.
- MCBSP modules support dual-phase frames to provide I2S fully compliant capabilities. This dual-phase mode, however, is limited to one channel (or word) for each phase instead of 128 channels maximum for single-phase mode.

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23.5.2 MCBSP Environment

This section describes the intended functions for the MCBSP module from an environment point of view (that is, external connections). It presents the MCBSP connectivity options, lists the possible interfaces, and details the protocol and data format used in each case.

23.5.2.1 MCBSP Functions

The device provides four instances of the MCBSP module called MCBSP1, MCBSP2 and MCBSP3.

The recommended use (nonexhaustive) for each MCBSP module in the device is:

- MCBSP1: Digital baseband (DBB) data
- MCBSP2: Audio data
- MCBSP3: Bluetooth® voice data

Table 23-327 describes the functions and the corresponding application fields.

Table 23-327. Functions Description

Function	Application Field	Recommended MCBSP Module	Description
Control and data	DBB data	MCBSP1	Serial interface to transfer data
Audio data	Audio data without audio buffer and sidetone feature	MCBSP2	Audio interface to transfer audio data with I2S
Voice data	Bluetooth voice data without sidetone feature	MCBSP3	Voice interface to transfer voice data with PCM

23.5.2.2 MCBSP Signals Descriptions

The MCBSP modules consist of a data-flow path and a control path connected to external devices by a serial interface with 4-pin configuration.

The internal multiplexers are controlled through the system control module on the device (see Section 23.5.3, *MCBSP Integration*). Table 23-328 describes the inputs/outputs (I/Os).

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Table 23-328. I/O Description

Pin Name	I/O	Description	Internal Signal Name	Reset Value[1]	Control and Data	Audio Data	Voice Data
abe_MCBSPi_dr	I	Receive serial data	DR	Hi-Z	✓	✓	✓
abe_MCBSPi_dx	(I)O[2]	Transmit serial data	DX	Hi-Z	✓	✓	✓
abe_MCBSPi_clkx	I/O [3]	Transmit clock[4]	CLKX	Hi-Z	✓	✓	✓
abe_MCBSPi_fsx	I/O [3]	Transmit frame synchronization [5]	FSX	Hi-Z	✓	✓	✓

(1) Hi-Z = High Impedance
(2) i = 1 to 3; I = Input, O = Output; I/O = Bidirectional
(3) For details of the I/O selection, see Section 23.5.2.3.1, *MCBSP Modes*.
(4) This signal is also used as CLKR when it is configured as output.
(5) This signal is also used as FSR when it is configured as output.

NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The control module registers assign the specific function to the device pads. For more information on control module settings, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, of *Chapter 18, Control Module*.

- The abe_clks pin can be used to inject an external clock. This clock is used to generate control signals depending on the module internal configuration (see Section 23.5.4.9, *MCBSP SRG*). The CLKS signal of the MCBSP modules is linked to an external signal through the abe_clks pin, but the CLKS signal can also be linked to an internal clock provided by the power, reset, and clock management (PRCM) module of the device. For more information, see Section 23.5.3, *MCBSP Integration*.
- Data are transmitted to external devices interfacing with MCBSP modules through the MCBSPi_dx pin. Data from those devices are received on the MCBSPi_dr pin.

NOTE: The MCBSPi_dx pin is an I/O signal to use the MCBSP module in half-duplex mode.

- Control information is communicated by the following pins:
  - MCBSPi_clkx (transmit clock)
  - MCBSPi_fsx (transmit frame-sync)

CAUTION

There is a light restriction on MCBSP modules when used in full-duplex mode. Reception and transmission use the same clock signal and the same frame-sync signal.

23.5.2.3 MCBSP Functions Description

23.5.2.3.1 MCBSP Modes

For all MCBSP functions, MCBSP modules can operate in master or slave mode. The difference between these modes is the definition of the source of MCBSP clocks and MCBSP frames synchronization:

- Master mode: MCBSP module provides them to the external device
- Slave mode: MCBSP module receives them from the external device

The choice between the two modes depends on technical data of the external device and the type of interface (protocols and data formats). For one MCBSP module, there are four possible functions:

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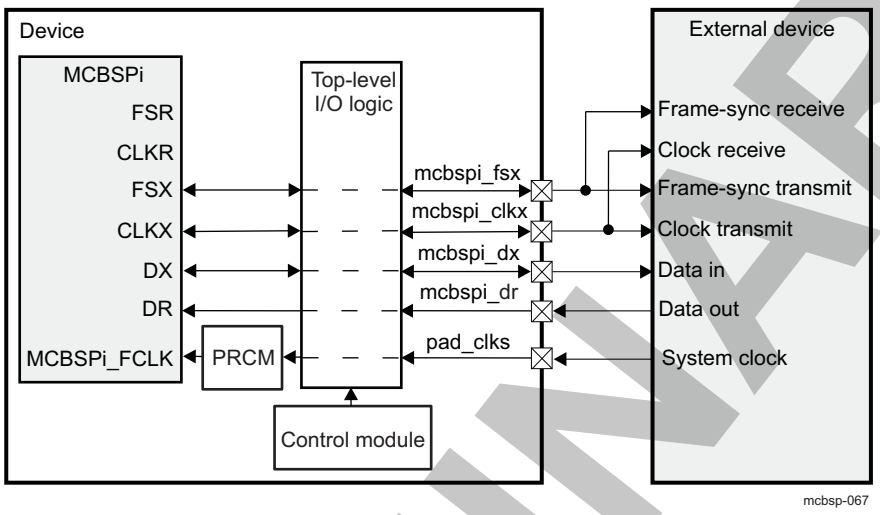
- Transmit-and-receive master mode
- Transmit-and-receive slave mode

Figure 23-101 shows the connection between the MCBSPi module, where i = 1, 2, or 3 (4-pin configuration) and an external device in transmit and receive master mode.

Figure 23-101. Mode Overview of MCBSPi



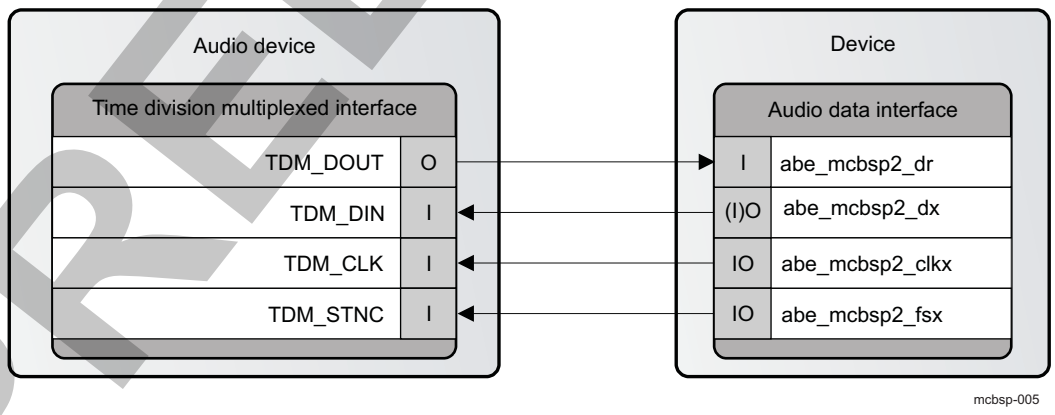
23.5.2.3.2 MCBSP Functions

23.5.2.3.2.1 MCBSP Function 1: Audio Data

The MCBSP module is connected to audio devices through the I2S interface. The I2S link serial interface is a TDM slot-based serial interface that is used to transfer audio data. Those audio devices can be either AICs or other serially connected A/D and D/A devices.

Figure 23-102 shows typical connections between a device and a typical device of analog audio interface to show the audio data application. The typical device contains several audio analog inputs and outputs and digital microphone inputs.

Figure 23-102. Audio Data Application



In Figure 23-102, MCBSP2 is configured in transmit-and-receive master mode.

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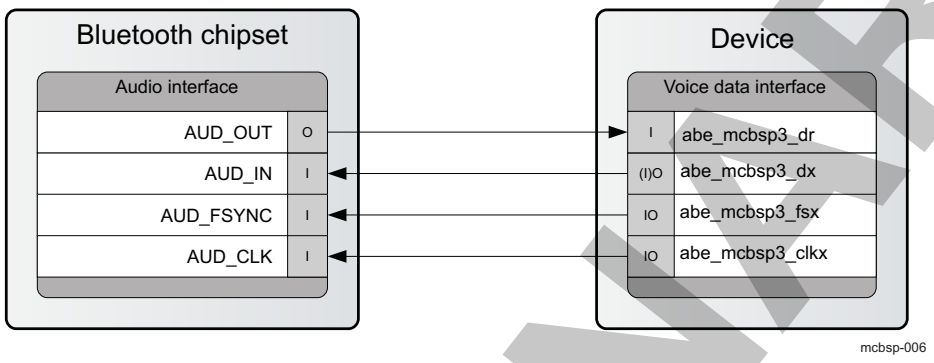
23.5.2.3.2.2 MCBSP Function 2: Voice Data

The MCBSP module is connected to a voice device through the PCM interface. The PCM link serial interface is a TDM slot-based serial interface that is used to transfer voice data. The voice devices can be modem chipsets, Bluetooth chipsets, or other devices with voice data interface.

Figure 23-103 shows typical connections between a device and a Bluetooth chipset (TI BRF6300 or TI BRF6350) to show voice data application.

Figure 23-103. Voice Data Application



In Figure 23-103, MCBSP3 is configured in transmit-and-receive master mode.

23.5.2.4 MCBSP Protocols and Data Formats

The MCBSP module can use one of the three protocols with associated data formats:

- Serial protocol to exchange serial data
- Audio protocol to exchange the audio samples
- Voice protocol to exchange the voice samples

The MCBSP modules offer the flexibility to modify the following parameters to adapt to the device features as described in the following subsections.

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23.5.2.4.1 Words, Frames, and Phases Definitions

23.5.2.4.1.1 Words or Channels

The data bits are transferred (transmission or reception) in a group called a serial word or channel. The number of bits in a word (length) is programmable through bit fields (MCBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1 and MCBSPi.MCBSPLP_RCR2_REG[7:5] RWDLEN2, MCBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1 and MCBSPi.MCBSPLP_XCR2_REG[7:5] XWDLEN2) and can be 8, 12, 16, 20, 24, or 32 bits (see Section 23.5.4.8.3, *Clocking and Framing Data*). The MCBSP module uses clock signals to control the time for each bit transfer. Data are sampled/driven on the rising or falling edge of clock signals. This clock polarity is programmable through bit fields of the pin-control register (MCBSPi.MCBSPLP_PCR_REG).

For more information, see Section 23.5.4.8.4, *Frame Phases (Dual-Phase Frame I2S Support)*.

23.5.2.4.1.2 Frames

One or more words (maximum 128) are transferred in a group called a frame. The MCBSP module can transmit and receive a maximum of 128 words per frame, programmable through bit fields of transmit-and-receive control registers (MCBSPi.MCBSPLP_XCR1_REG/MCBSPi.MCBSPLP_XCR2_REG and MCBSPi.MCBSPLP_RCR1_REG/MCBSPi.MCBSPLP_RCR2_REG). For more details, see Section 23.5.4.8.3, *Clocking and Framing Data*.

All the words in a frame are sent in a continuous stream. However, there can be pauses between frame transfers. The MCBSP module uses frame-sync signals to determine when each frame is received or transmitted. When a pulse occurs on a frame-sync signal, the MCBSP module begins receiving or transmitting a frame of data. When the next pulse occurs, the MCBSP module receives or transmits the next frame, and so on. The frame-sync pulse is active high or low. This pulse polarity is programmable through bit fields of the pin control register (MCBSPi.MCBSPLP_PCR_REG).

Each frame transfer can be delayed by 0, 1, or 2 clock cycles, depending on the value of bits for transmit and receive control registers (MCBSPi.MCBSPLP_XCR2_REG and MCBSPi.MCBSPLP_RCR2_REG). For more information, see Section 23.5.4.10.6.3, *Preventing Unexpected Transmit Frame-sync Pulses* and Section 23.5.4.10.3.3, *Preventing Unexpected Receive Frame-sync Pulses*.

23.5.2.4.1.3 Phases

The MCBSP module allows configuring of each frame to contain one or two phases. The MCBSP module supports dual-phase frames to provide I2S fully compliant capabilities. These two phases represent left and right channels of audio stereo signals.

The limitation on dual-phase frame is that the number of words per phase must be set to 1 for both first and second phases. The number of bits per word, however, can be specified differently for each of the two phases of a frame, allowing greater flexibility in structuring data transfers.

For example, software may define a frame composed of a first phase with one 12-bit word and a second phase with one 16-bit word. This configuration allows the software to compose frames for custom applications. For more details, see Section 23.5.4.8.4, *Frame Phases (Dual-Phase Frame I2S Support)*.

Figure 23-104 shows signal activity for two possible reception/transmission scenarios.

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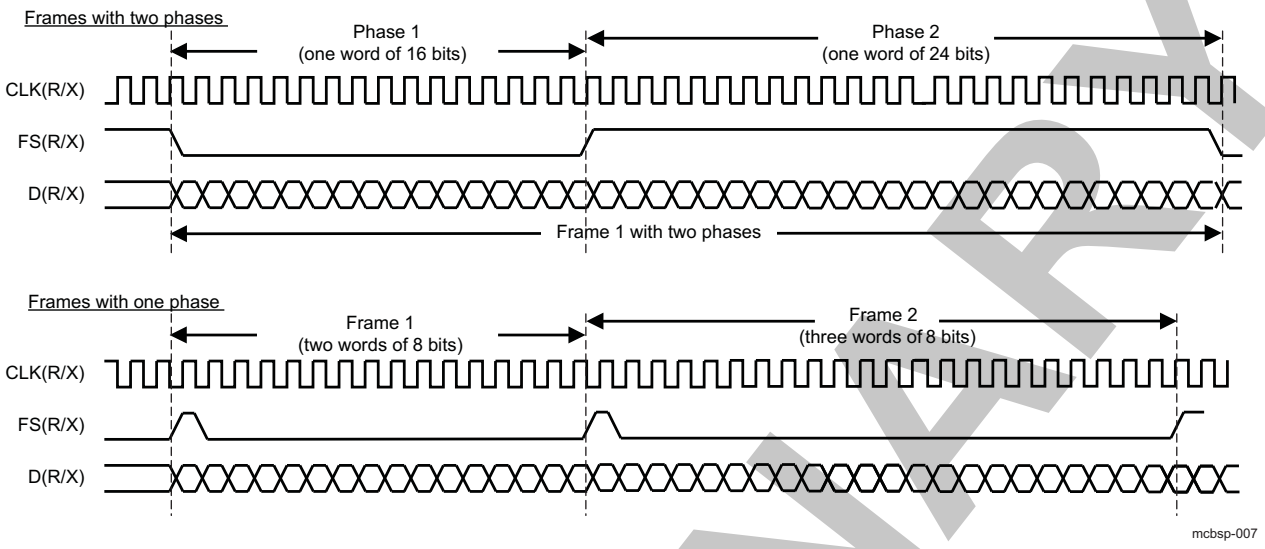
Figure 23-104. MCBSP Reception/Transmission Signal Activity



23.5.2.4.2 Serial Protocol and Data Formats

23.5.2.4.2.1 Protocol

The serial protocol is used to send and receive control data without specific formats. This allows the MCBSP module to accommodate all serial devices and their protocols.

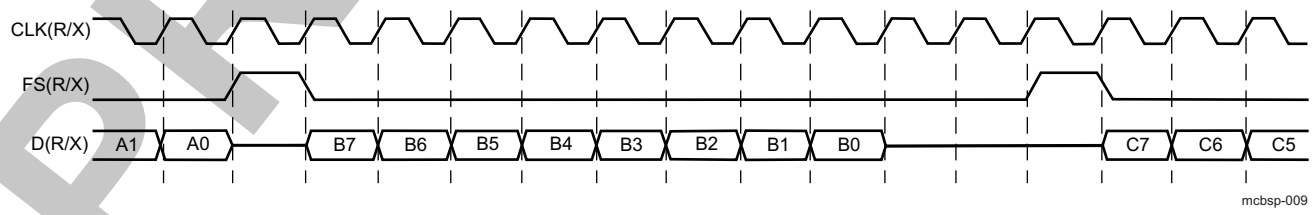
23.5.2.4.2.2 Data Format

Figure 23-105 shows typical operation of the MCBSP clock and frame-sync signals. Serial clocks CLKR and CLKX define the boundaries between bits for receive and transmit, respectively. Similarly, frame-sync signals FSR and FSX define the beginning of an element and/or frame transfer. The MCBSP module allows the configuration of the following parameters for data and frame synchronization:

- Polarity of FSR, FSX, CLKX, and CLKR
- The number of words per frame
- The number of bits per word
- Whether subsequent frame synchronization restarts the serial data stream or is ignored
- The data delay from frame synchronization to first data bit which can be 0- , 1- , or 2-bit delays

The configuration is independent for receive and transmit parts. For more details and configuration examples, see Section 23.5.4, *MCBSP Functional Description*, and Section 23.5.5, *MCBSP Basic Programming Model*.

Figure 23-105. Serial Data Formats



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23.5.2.4.3 Audio Protocol and Data Formats

23.5.2.4.3.1 Protocol

The I2S protocol is used to send and receive audio data from 8-kHz to 48-kHz sampling rate (frame-sync frequency), with 16 bits or 32 bits per words (two standard sample rate groups that are used in audio applications are supported: 48 and 44.1 KHz). The 48-KHz sample rate group includes 8, 16, 24, 32 and 48 KHz frequencies. The 44.1-KHz sample rate group includes 11.025, 22.05, and 44.1 KHz frequencies.

Based on required sample rate, it is recommended the I2S clock to be configured as multiple of 44.1 or 96 KHz (48KHz × 2).

For example:

The McBSP clock is provided by the system clock and is set to 12.288 MHz (48KHz × 256) for the first group and 11.2896 MHz (44.1 × 256) for the second group. In this case, 256 is the value for Sample Rate Generator Clock Divider, which should be set in the MCBSPLP_SRGR1_REG[7:0] CLKGDIV bit field.

The frame-sync signal defines the frame length in the I2S protocol. Each frame consists of a fixed number of words. In dual-phase frame, the frame-sync signal is low for the left phase time slot and is high for the right phase time slot. In addition, the frame-sync signal is synchronous to the falling edge of the clock signal.

23.5.2.4.3.2 Data Formats

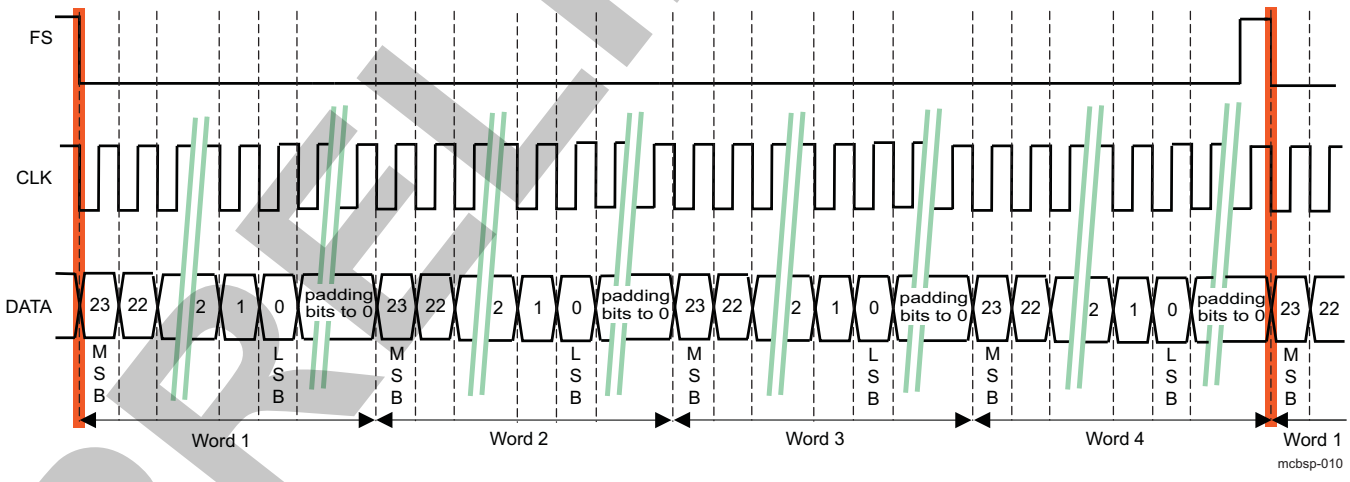
The I2S protocol supports TDM, I2S, left-justified, and right-justified data formats.

Bits of each word (sample) are clocked using the clock signal. For each word, the most-significant bit (MSB) is first. LSBs are padded to 0 when the data length (8, 12, 16, 20, or 24 bits) is less than the sample word width (16 or 32 bits).

23.5.2.4.3.2.1 TDM Data Format

Figure 23-106 shows that each frame of TDM data format is composed of four words (or channels).

Figure 23-106. TDM Data Format; Word Width: 32 Bits; Data Length: 24 Bits



23.5.2.4.3.2.2 I2S Data Format

Figure 23-107 shows an example with 24-bit data (MSB first) and 8 padding bits at 0.

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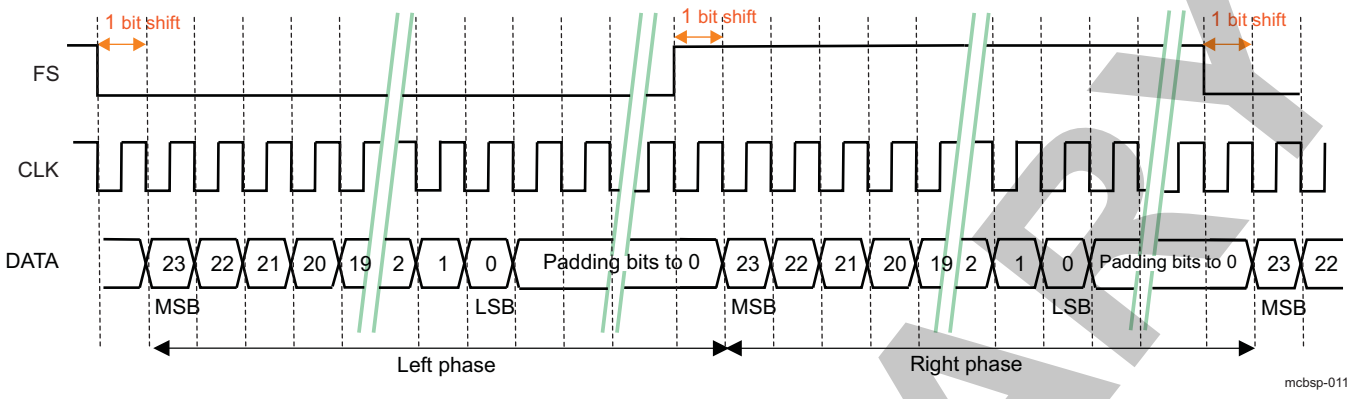
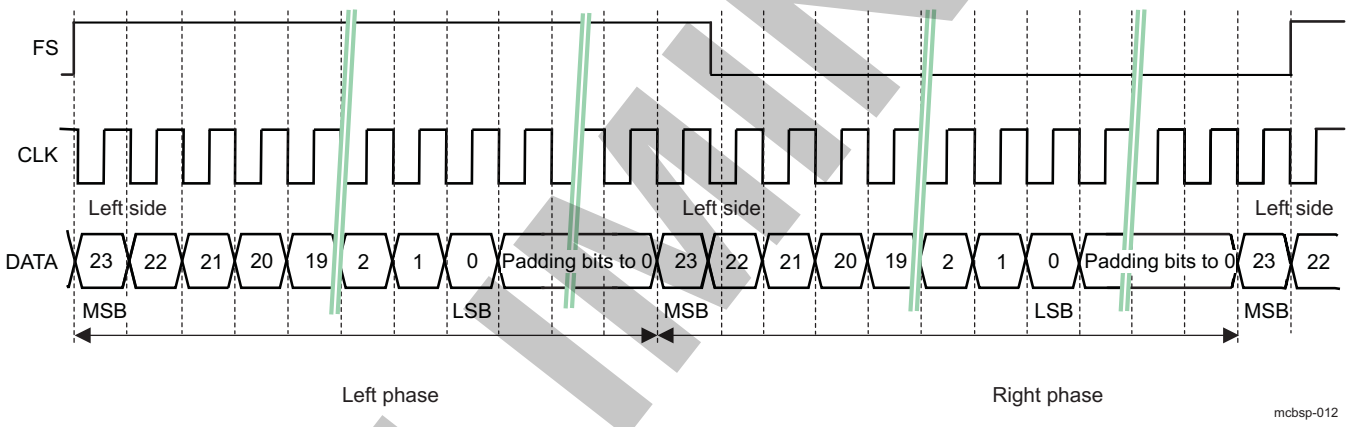
Figure 23-107. I2S Data Format; Word Width: 32 Bits; Data Length: 24 Bits



23.5.2.4.3.2.3 Left-Justified Data Format

Figure 23-108 shows an example with 24-bit data (MSB first) and 8 padding bits at 0.

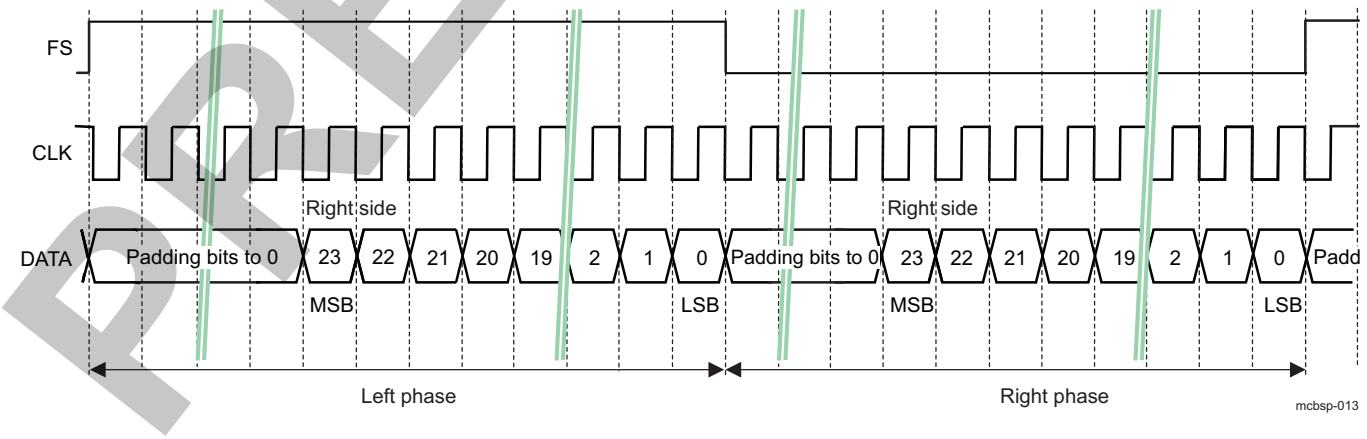
Figure 23-108. Left-Justified Data Format; Word Width: 32 Bits; Data Length: 24 Bits



23.5.2.4.3.2.4 Right-Justified Data Format

Figure 23-109 shows an example with 24-bit data (MSB first) and 8 padding bits at 0.

Figure 23-109. Right-Justified Data Format; Word Width: 32 Bits; Data Length: 24 Bits



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23.5.2.4.4 Voice Protocol and Data Formats

23.5.2.4.4.1 Protocol

The PCM protocol is intended to transfer voice data at 8-kHz (default narrowband mode) or 16-kHz (wideband mode) sample rate (frame-sync frequency). PCM protocol can act as a slave or master, and is used by the Bluetooth interface and the modem generic interface. The frame synchronization defines the frame length in the PCM protocol. Bits are clocked using the PCM clock signal, with the MSB first.

23.5.2.4.4.2 Data Formats

Two modes are available for the PCM protocol: mode 1 and mode 2. Both modes have two types of operations: mono or stereo channels. The difference between PCM mode 1 and PCM mode 2 is in the way in which they use the rising or the falling edge of the clock signal, and the frame-sync polarity.

- PCM mode 1: Input data is latched on the falling edge of the clock, and the transmitted data starts on the rising edge of the clock. The frame-sync pulse is active high.
- PCM mode 2: Input data is latched on the rising edge of the clock, and the transmitted data starts on the falling edge of the clock. The frame-sync pulse is active low.

Figure 23-110 and Figure 23-111 show an example of PCM protocol, mode 1 and mode 2, respectively, for a frame composed of one word (32 bits wide) with 16 bits of data.

Figure 23-110. PCM Protocol – Mode 1 Data Format

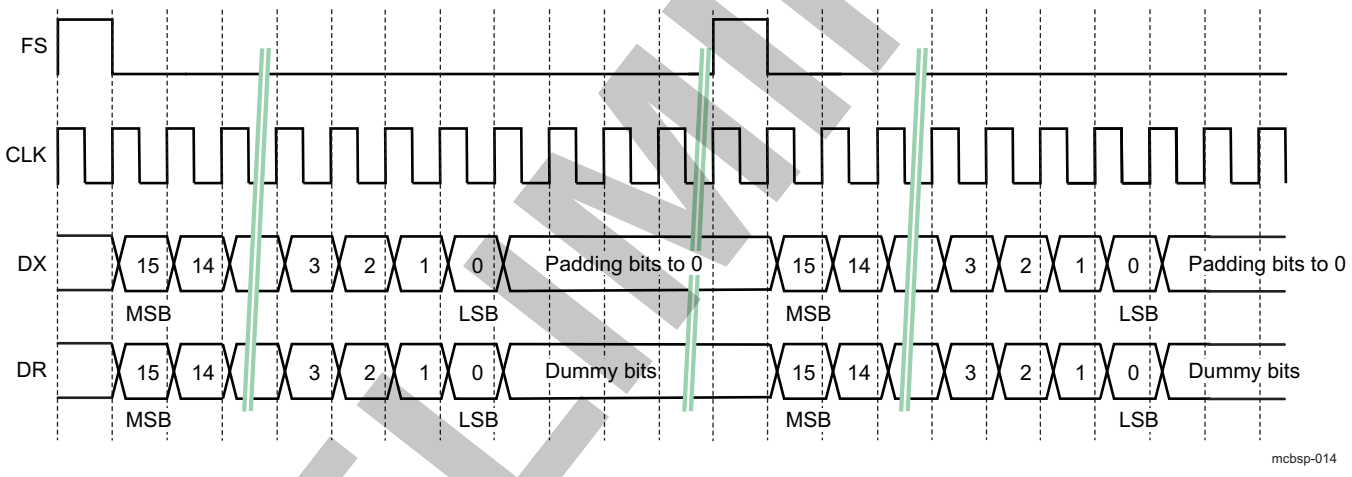
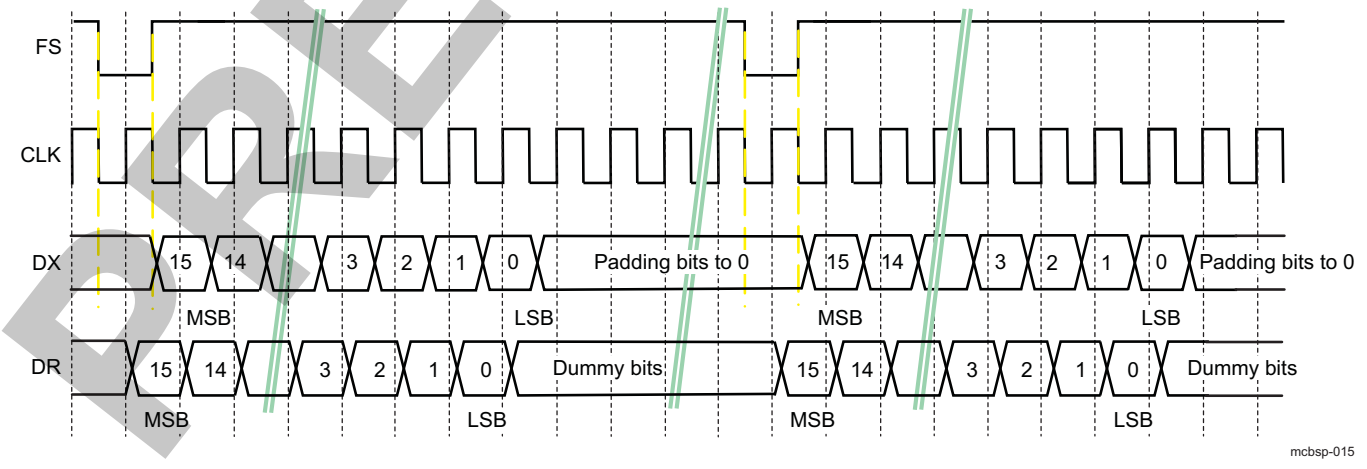


Figure 23-111. PCM Protocol – Mode 2 Data Format



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23.5.3 MCBSP Integration

This section describes the integration of the MCBSP module in the device, including information about clocks, resets, and hardware requests.

MCBSP modules are divided into two families: MCBSP modules that are gated in the AUDIO power domain (MCBSP1, 2, and 3).

Figure 23-112 shows the integration of the MCBSP modules in the device, including interrupt handlers, DMA requests, clock generators, and interconnections.

The features of the MCBSP modules are:

- Wake-up request
- Two DMA requests
- One IRQ
- One functional clock
- One interface clock

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Figure 23-112. MCBSPi Integration

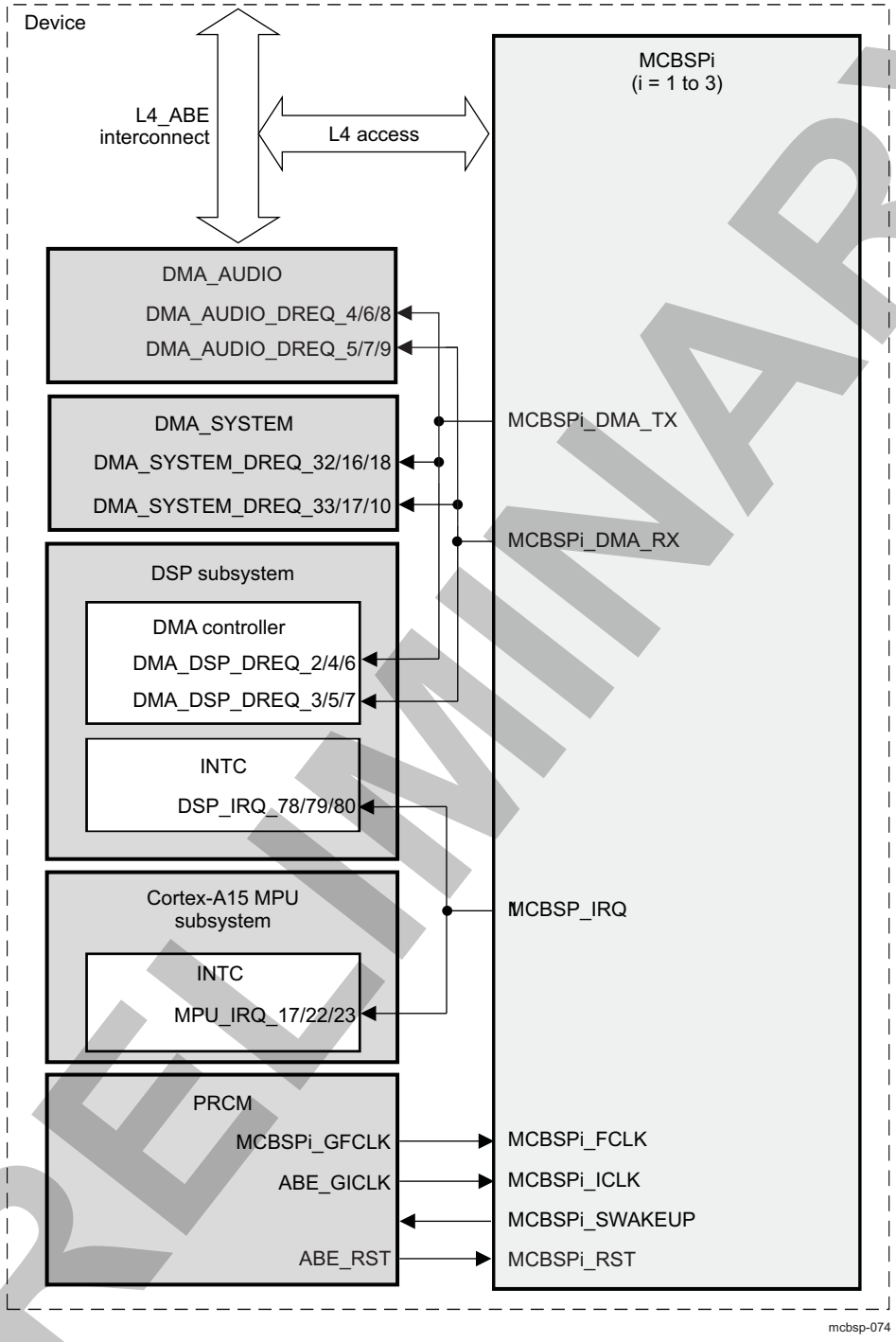

Table 23-329 through Table 23-331 summarize the integration of the module in the device.

Table 23-329. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
MCBSP1	PD_ABE	Yes	L4_ABE
MCBSP2	PD_ABE	Yes	L4_ABE

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Table 23-329. Integration Attributes (continued)

MCBSP3	PD_ABE	Yes	L4_ABE

Table 23-330. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MCBSP1	MCBSP1_ICLK	ABE_GICLK	PRCM	MCBSP1 interface clock
	MCBSP1_FCLK	MCBSP1_GFCLK	PRCM	MCBSP1 functional clock
MCBSP2	MCBSP2_ICLK	ABE_GICLK	PRCM	MCBSP2 interface clock
	MCBSP2_FCLK	MCBSP2_GFCLK	PRCM	MCBSP2 functional clock
MCBSP3	MCBSP3_ICLK	ABE_GICLK	PRCM	MCBSP3 interface clock
	MCBSP3_FCLK	MCBSP3_GFCLK	PRCM	MCBSP3 functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MCBSP1	MCBSP1_RST	ABE_RST	PRCM	ABE power domain reset
MCBSP2	MCBSP2_RST	ABE_RST	PRCM	ABE power domain reset
MCBSP3	MCBSP3_RST	ABE_RST	PRCM	ABE power domain reset

Table 23-331. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MCBSP1	MCBSP1_IRQ	DSP_IRQ_78	DSP INTC	Common synchronous interrupt request line
	MCBSP1_IRQ	MPU_IRQ_17	Cortex-A15 MPU INTC	Common synchronous interrupt request line
MCBSP2	MCBSP2_IRQ	DSP_IRQ_79	DSP INTC	Common synchronous interrupt request line
	MCBSP2_IRQ	MPU_IRQ_22	Cortex-A15 MPU INTC	Common synchronous interrupt request line
MCBSP3	MCBSP3_IRQ	DSP_IRQ_80	DSP INTC	Common synchronous interrupt request line
	MCBSP3_IRQ	MPU_IRQ_23	Cortex-A15 MPU INTC	Common synchronous interrupt request line
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MCBSP1	MCBSP1_DMA_TX	DMA_AUDIO_DREQ_4	DMA_AUDIO	Transmit DMA request
	MCBSP1_DMA_RX	DMA_AUDIO_5	DMA_AUDIO	Receive DMA request
	MCBSP1_DMA_TX	DMA_SYSTEM_DREQ_32	DMA_SYSTEM	Transmit DMA request
	MCBSP1_DMA_RX	DMA_SYSTEM_DREQ_33	DMA_SYSTEM	Receive DMA request
	MCBSP1_DMA_TX	DMA_DSP_DREQ_2	DMA_DSP	Transmit DMA request
	MCBSP1_DMA_RX	DMA_DSP_DREQ_3	DMA_DSP	Receive DMA request
MCBSP2	MCBSP2_DMA_TX	DMA_AUDIO_6	DMA_AUDIO	Transmit DMA request

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Table 23-331. Hardware Requests (continued)

	MCBSP2_DMA_RX	DMA_AUDIO_7	DMA_AUDIO	Receive DMA request
	MCBSP2_DMA_TX	DMA_SYSTEM_DREQ_16	DMA_SYSTEM	Transmit DMA request
	MCBSP2_DMA_RX	DMA_SYSTEM_DREQ_17	DMA_SYSTEM	Receive DMA request
	MCBSP2_DMA_TX	DMA_DSP_DREQ_4	DMA_DSP	Transmit DMA request
	MCBSP2_DMA_RX	DMA_DSP_DREQ_5	DMA_DSP	Receive DMA request
MCBSP3	MCBSP3_DMA_TX	DMA_AUDIO_8	DMA_AUDIO	Transmit DMA request
	MCBSP3_DMA_RX	DMA_AUDIO_9	DMA_AUDIO	Receive DMA request
	MCBSP3_DMA_TX	DMA_SYSTEM_DREQ_18	DMA_SYSTEM	Transmit DMA request
	MCBSP3_DMA_RX	DMA_SYSTEM_DREQ_19	DMA_SYSTEM	Receive DMA request
	MCBSP3_DMA_TX	DMA_DSP_DREQ_6	DMA_DSP	Transmit DMA request
	MCBSP3_DMA_RX	DMA_DSP_DREQ_7	DMA_DSP	Receive DMA request

NOTE:

- For more information about the interrupt source, see Section 23.5.4.6, *Interrupt Requests*.
- For more information about the DMA source, see Section 23.5.4.7, *DMA Requests*.

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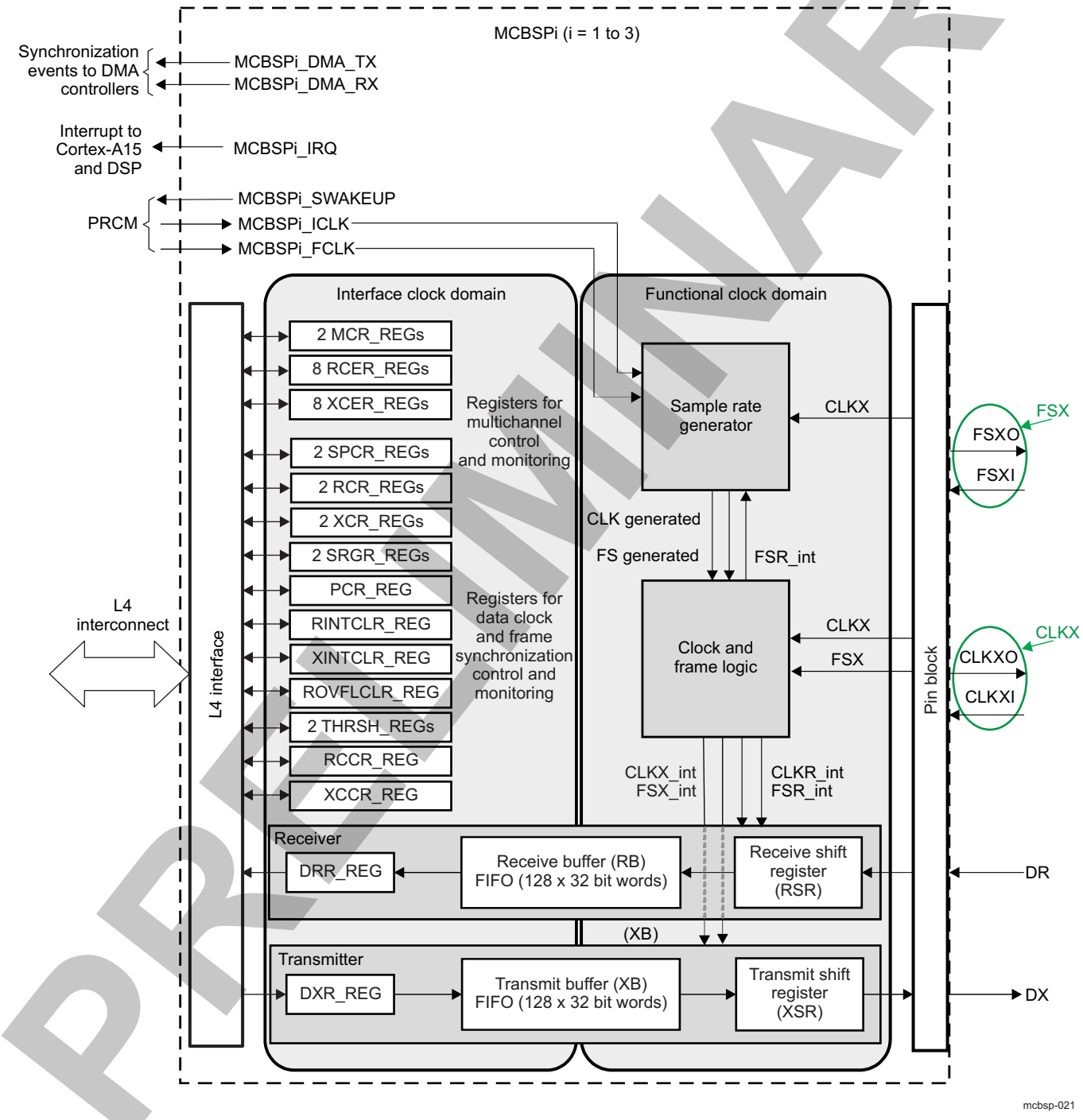
23.5.4 MCBSP Functional Description

This section is a functional description of the MCBSP module.

23.5.4.1 Block Diagram

Figure 23-113 shows the functional block diagram of the four instances of the MCBSP modules.

Figure 23-113. MCBSPi Block Diagram



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23.5.4.2 Signal Source Control

The sources of the CLKX, DX, DR, FSX signals are defined by the system control module. The control registers of the system control module are used to select these signal sources. For more information, see Section 18.4.12.7.5, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*.

23.5.4.3 MCBSP Clock Configuration

23.5.4.3.1 MCBSP1 Clocks

MCBSP1 is clocked by a functional clock (MCBSP1_FCLK and CLKX) and an interface clock (MCBSP1_ICLK).

- The functional clock is used to generate control signals depending on the internal configuration of the module (see Section 23.5.4, *MCBSP Functional Description*). For MCBSP1, the functional clock comes from the CLKS and CLKX signals. The choice between these two clocks is defined by the MCBSP1.MCBSPLP_PCR_REG[7] SCLKME bit and the MCBSP1.MCBSPLP_SRGR2_REG[13] CLKSM bit.

  The CLKS signal of MCBSP1 is linked to an internal clock (MCBSP1_FCLK) provided by the PRCM module. The CLKS signal can also be linked to an external signal through the abe_clks pin of the device boundary.

  NOTE: When MCBSP1 no longer requires the functional clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field to 0x0 (PRCM.CM1_ABE_MCBSP1_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

  At the PRCM level, when all the conditions to shut off the MCBSP1_FCLK clock are met, the PRCM module automatically launches a hardware handshake protocol to ensure MCBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the MCBSP module. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

  Only the CLKX signal is connected by MCBSP1_clkx pads. The CLKR signal is connected to the CLKX signal. These signals are used like functional clocks by the intermediary of SRG.
- The MCBSP1_ICLK runs at the L4 core interconnect clock speed. It is used to trigger access to the MCBSP1 L4 interface and MCBSP1 configuration interface through the Cortex-A15 MPU/DSP shared bus. It can also be an input clock for the MCBSP SRG (clock divider), depending on the module configuration (see Section 23.5.4.9, *MCBSP SRG*). Its source is the ABE_GICLK signal.

  NOTE: When MCBSP1 no longer requires the interface clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field (PRCM.CM_ABE_MCBSP1_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

  At the PRCM level, when all the conditions to shut off the ABE_GICLK clock are met the PRCM module automatically launches a hardware handshake protocol to ensure MCBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the MCBSP module. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

23.5.4.3.2 MCBSP2 Clocks

MCBSP2 is clocked by a functional clock (MCBSP2_FCLK or CLKX) and an interface clock (MCBSP2_ICLK).

- The functional clock is used to generate control signals depending on the internal configuration of the module (see Section 23.5.4, *MCBSP Functional Description*). For MCBSP2, the functional clock comes from the MCBSP2_FCLK and CLKX signals. The choice between these two clocks is defined by the MCBSP2.MCBSPLP_PCR_REG[7] SCLKME bit and the MCBSP2.MCBSPLP_SRGR2_REG[13]

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CLKSM bit.

NOTE: When MCBSP2 no longer requires the functional clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field to 0x0 (PRCM.CM_ABE_MCBSP2_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

At the PRCM level, when all the conditions to shut off the MCBSP2_GFCLK clock are met the PRCM automatically launches a hardware handshake protocol to ensure MCBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the MCBSP module. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

Only the CLKX signal is connected by MCBSP2_clkx pads. The CLKR signal is connected to the CLKX signal. These signals are used like functional clocks by the intermediary of the SRG.

- The MCBSP2_ICLK runs at the L4 core interconnect clock speed. It is used to trigger access to the MCBSP2 L4 interface and MCBSP2 configuration interface through the Cortex-A15 MPU/DSP shared bus. It can also be an input clock for the MCBSP SRG (clock divider), depending on the module configuration (see Section 23.5.4.9, *MCBSP SRG*). Its source is the ABE_GICLK signal.

NOTE: When MCBSP2 no longer requires the interface clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field (PRCM.CM_ABE_MCBSP2_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

At the PRCM level, when all the conditions to shut off the ABE_ICLK2 clock are met the PRCM module automatically launches a hardware handshake protocol to ensure MCBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the MCBSP module. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

23.5.4.3.3 MCBSP3 Clocks

MCBSP3 is clocked by a functional clock (MCBSP3_FCLK or CLKX) and an interface clock (MCBSP3_ICLK).

- The functional clock is used to generate control signals depending on the internal configuration of the module (see Section 23.5.4, *MCBSP Functional Description*). For MCBSP3, the functional clock comes from the CLKS and CLKX signals. The choice between these two clocks is defined by the MCBSP3.MCBSPLP_PCR_REG[7] SCLKME bit and the MCBSP3.MCBSPLP_SRGR2_REG[13] CLKSM bit.

NOTE: When MCBSP3 no longer requires the functional clock, software can disable it at the PRCM level by configuring the MODULEMODE bit field to 0x0 (PRCM.CM_ABE_MCBSP3_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

At the PRCM level, when all the conditions to shut off the MCBSP3_FCLK clock are met the PRCM module automatically launches a hardware handshake protocol to ensure MCBSP is ready to have this clock switched off. Namely, the PRCM module asserts an IDLE request to the MCBSP module. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

Only, the CLKX signal is connected by MCBSP3_clkx pads. The CLKR signal is connected to the CLKX signal. These signals are used like functional clocks by the intermediary of SRG.

- The MCBSP3_ICLK runs at the L4 core interconnect clock speed. It is used to trigger access to the MCBSP3 L4 interface and MCBSP3 configuration interface via the Cortex-A15 MPU/DSP shared bus. It can also be an input clock for the MCBSP sample-rate generator (clock divider), depending on the module configuration (see Section 23.5.4.9, *MCBSP SRG*). Its source is either the ABE_GICLK signal.

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NOTE: When the MCBSP2 module does not require the interface clock anymore, the software can disable it at the PRCM level by configuring the MODULEMODE bit field (PRCM.CM_ABE_MCBSP3_CLKCTRL[1:0]) in the PRCM registers. The clock is effectively cut, provided the other modules that receive it do not require it.

At PRCM level, when all the conditions to shut-off ABE_GICLK clock are met the PRCM automatically launches a hardware handshake protocol to ensure MCBSP is ready to have this clock switched off. Namely, the PRCM asserts an IDLE request to MCBSP module. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

It is also possible to activate an autoidle mode for this clock (PRCM.CM_AUTOIDLE_PER[1] register AUTO_MCBSP3 bit set to 1). In this case, MCBSP3_ICLK follows the AUDIO_L4 clock domain behavior on the device. For more information, see Chapter 3, *Power, Reset, and Clock Management*.

23.5.4.4 MCBSP Software Reset

The MCBSP1, 2, and 3 modules belong to the AUDIO domain and their reset signal is AUDIO_RST from the PRCM module. Table 23-332 lists the software reset signals to all MCBSP modules.

Table 23-332. Software Reset Signals to All MCBSP Modules

Type	Bit Field	Register Source	Activation	Description
Software	SOFTRESET	MCBSPi.MCBSPLP_SYSCONFIG_REG[1]	Active high	MCBSP global software reset
	RRST	MCBSPi.MCBSPLP_SPCR1_REG[0]	Active low	This resets and disables the receiver, including the RB.
	XRST	MCBSPi.MCBSPLP_SPCR2_REG[0]		This resets and disables the transmitter, including the XB.
	GRST	MCBSPi.MCBSPLP_SPCR2_REG[6]		SRG is reset.
	FRST	MCBSPi.MCBSPLP_SPCR2_REG[7]		Frame-sync logic is reset. Frame-sync generated signal is not generated by the SRG.

For a complete description of the MCBSP initialization procedure, see Section 23.5.5.1, *MCBSP Initialization Procedure*.

23.5.4.5 MCBSP Power Management

23.5.4.5.1 MCBSP Operating States

Two operating states are defined for all the MCBSP modules:

- ACTIVE state: The module is running synchronously on the interface and functional clocks. Interrupts and DMA requests can be generated according to the configuration (register, master or slave mode, etc) and the external signals.
- IDLE state: As part of the system power management, the PRCM module can request the MCBSP modules to enter IDLE state. Depending on the configured acknowledgment mode (force-idle, no-idle and smart-idle modes), a MCBSP module effectively enters IDLE state or not. As soon as a MCBSP module enters IDLE state, its only activities are those unrelated to clock activity (for example, wake-up features) and its clocks are likely to be switched off at the PRCM level.

NOTE: IDLE request and IDLE acknowledge are only internal signals, with no means to observe or to control. The generation and control of the signals is purely hardware (managed automatically by the PRCM module and the MCBSP depending on the SIDLEMODE settings).

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23.5.4.5.2 MCBSP Acknowledgment Modes

During initialization or configuration of the MCBSP module, software must configure how the MCBSP module will answer an IDLE solicitation from the PRCM module (that is, the way IDLE acknowledge is asserted following assertion of an idle request).

Each MCBSP module can be configured through the MCBSPi.MCBSPLP_SYSCONFIG_REG[4:3] SIDLEMODE bit field as one of the following acknowledgment modes:

- Force-idle mode (SIDLEMODE bit = 0x0): An IDLE request is acknowledged unconditionally, regardless of the internal state of the module. The MCBSP module immediately enters IDLE state (no activity), interface and PRCM functional clocks can be stopped, and no interrupts and DMA requests can be generated. In this mode, the MCBSP module freezes all the internal activity when the PRCM clocks are switched off by the PRCM module, leading to a potential loss of data.

CAUTION

In force-idle mode, the wake-up feature is inhibited.

CAUTION

If the MCBSP functional part, transmitter or receiver, is running within this period of time (the functional clock source is not the PRCM functional clock), the internal state of the MCBSP module will not be idle (FSM states, processes, etc.), and when the MCBSP module exits from the Force Idle state unexpected behavior may happen in both receiver and transmitter. To avoid this, both receive and transmit parts, must be disabled by software prior to idle request assertion (all functional clock external sources must be disabled).

- No-idle mode (SIDLEMODE bit = 0x1): An IDLE request is never acknowledged, meaning it prevents the PRCM module from switching off its related clocks and from putting in a lower power state than the power domain to which it belongs. The MCBSP module never enters IDLE state (is active).
- Smart-idle mode (SIDLEMODE bit = 0x2): Acknowledgement to an IDLE request is given based on the internal activity of the MCBSP module. The MCBSP module is in a waiting state, interface and functional clocks can be stopped, no interrupts can be generated, and a wake-up signal can be generated according to the configuration (see Section 23.5.4.5.4, *Analysis of the Receiver Smart-Idle Behavior*) and external signals.

NOTE: The value MCBSPi.MCBSPLP_SYSCONFIG_REG[4:3] SIDLEMODE field = 0x3 must not be used.

When configured in smart-idle mode, the MCBSP module also offers an additional granularity on MCBSPi_FCLK and MCBSPi_ICLK gating. The MCBSPi.MCBSPLP_SYSCONFIG_REG[9:8] CLOCKACTIVITY bit field is used to determine which clock will be shut down (MCBSPi_FCLK, MCBSPi_ICLK, none of them, or both of them).

CLOCKACTIVITY setting is used in the MCBSP module to determine on which part of the module the conditions to acknowledge the PRCM IDLE request will be tested. As an example, if MCBSPi_FCLK is said not to be shut down upon a PRCM IDLE request, this means the MCBSP module will consider only MCBSPi_ICLK and the associated pending activities before acknowledging the request.

NOTE: Some MCBSP features are associated with MCBSPi_ICLK and others with MCBSPi_FCLK. Using CLOCKACTIVITY along with the smart-idle mode ensures that the features associated with the clock that remain active are always enabled, even if the MCBSP has acknowledged an IDLE request. For more information, see Section 23.5.4.5.4, *Analysis of the Receiver Smart-Idle Behavior*.

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Table 23-333 lists the value of the bit field and indicates whether the interface (MCBSPi_ICLK) and PRCM functional (MCBSPi_FCLK) clocks can be switched off or not when an IDLE request is received by the MCBSP module.

Table 23-333. State of Clocks When the Module is in Idle State

CLOCKACTIVITY Value	Interface Clock (MCBSPi_ICLK)	PRCM Functional Clock
0b00	Off	Off
0b01	Off	On
0b10	On	Off
0b11	On	On

NOTE: Off means this clock can be switched off.

On means this clock must be maintained during the wake-up period.

CAUTION

The PRCM module does not have any hardware means to read CLOCKACTIVITY settings. Software must ensure a consistent programming between the MCBSPi.MCBSPLP_SYSCONFIG_REG[9:8] CLOCKACTIVITY bit field and the PRCM MCBSPi_GFCLK and L4_ICLK control bits (see notes in Section 23.5.4.3, *MCBSP Clock Configuration*). If the MCBSP module is disabled while CLOCKACTIVITY is set to 0x3, nothing prevents the PRCM module from asserting its IDLE request, which is acknowledged regardless of the features associated with the MCBSP clocks. This may lead to unpredictable behaviors.

23.5.4.5.3 Wake-Up Capability

When configured in smart-idle mode, the sources for wake-up generation are a subset of the interrupt sources. The wake-up sources are enabled by setting the MCBSPi.MCBSPLP_SYSCONFIG_REG[2] ENAWAKEUP bit (wake-up feature control):

- Set to 0, wake-up capability is disabled.
- Set to 1, wake-up capability is enabled.

The MCBSPi_SWAKEUP signal is the MCBSP module asynchronous wake-up signal sent to the PRCM module when a wake-up generation is requested.

The wake-up configurations are defined by setting the corresponding bits in the MCBSPi.MCBSPLP_WAKEUPEN_REG register.

23.5.4.5.3.1 Receive Wakeup

There are four receive possible wake-up configurations:

- MCBSPi.MCBSPLP_WAKEUPEN_REG[3] RRDYEN bit: The MCBSP module asserts the MCBSPi_SWAKEUP request when the receive buffer reaches the high threshold value (RTHRESHOLD value + 1) of the MCBSPi.MCBSPLP_THRSH1_REG register. If the MCBSPi.MCBSPLP_IRQENABLE_REG[3] RRDYEN bit is set to 1, the MCBSP module sends an interrupt (MCBSPi_IRQ) request to the MPU or DSP subsystems when exiting from idle mode (interrupt will be asserted once the MCBSPi.MCBSPLP_IRQSTATUS_REG[3] RRDY bit changes from 0 to 1, indicating that received data is ready to be read).
- MCBSPi.MCBSPLP_WAKEUPEN_REG[2] REOFEN bit: The MCBSP module asserts the MCBSPi_SWAKEUP request at the end of the frame. If the MCBSPi.MCBSPLP_IRQENABLE_REG[2] REOFEN bit is set to 1, the MCBSP module sends an interrupt (MCBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.

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- MCBSPi.MCBSPLP_WAKEUPEN_REG[1] RFSREN bit: The MCBSP module sends a MCBSPi_SWAKEUP request to the PRCM module when a receive frame-sync pulse is detected while the MCBSP module is in idle mode. If the MCBSPi.MCBSPLP_IRQENABLE_REG[1] RFSREN bit is set to 1, the MCBSP module sends an interrupt (MCBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.
- MCBSPi.MCBSPLP_WAKEUPEN_REG[0] RSYNCERREN bit: The MCBSP module asserts the MCBSPi_SWAKEUP request when an unexpected receive frame-sync pulse is detected. If the MCBSPi.MCBSPLP_IRQENABLE_REG[0] RSYNCERREN bit is set to 1, the MCBSP module sends an interrupt (MCBSPi_IRQ) request to the MPU or DSP subsystems when exiting from idle mode (interrupt is asserted once the MCBSPi.MCBSPLP_IRQSTATUS_REG[0] RSYNCERR bit changes from 0 to 1, indicating that a receive error occurred).

23.5.4.5.3.2 Transmit Wakeup

For transmit, there are five possible wake-up configuration scenarios:

- MCBSPi.MCBSPLP_WAKEUPEN_REG[14] XEMPTYEOFEN bit: The MCBSP module asserts the MCBSPi_SWAKEUP request when a complete frame was transmitted and the transmit buffer is empty. If the MCBSPi.MCBSPLP_IRQENABLE_REG[14] XEMPTYEOFEN bit is set to 1, the MCBSP module sends an interrupt (MCBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.
- MCBSPi.MCBSPLP_WAKEUPEN_REG[10] XRDYEN bit: The MCBSP module asserts the MCBSPi_SWAKEUP request when the transmit buffer reaches the high threshold value (XTHRESHOLD value + 1) of the MCBSPi.MCBSPLP_THRSH2_REG register. If the MCBSPi.MCBSPLP_IRQENABLE_REG[10] XRDYEN bit is set to 1, the MCBSP module sends an interrupt (MCBSPi_IRQ) request to the MPU or DSP subsystems when exiting from idle mode (interrupt is asserted once the MCBSPi.MCBSPLP_IRQSTATUS_REG[10] XRDY bit changes from 0 to 1, indicating that transmit buffer data is ready to accept new data).
- MCBSPi.MCBSPLP_WAKEUPEN_REG[9] XEOFEN bit: The MCBSP module asserts the MCBSPi_SWAKEUP request at the end of the frame. If the MCBSPi.MCBSPLP_IRQENABLE_REG[9] XEOFEN bit is set to 1, the MCBSP module sends an interrupt (MCBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.
- MCBSPi.MCBSPLP_WAKEUPEN_REG[8] XFSXEN bit: The MCBSP module sends a MCBSPi_SWAKEUP request when a transmit frame-sync pulse is detected while the module is in idle mode. If the MCBSPi.MCBSPLP_IRQENABLE_REG[8] XFSXEN bit is set to 1, the MCBSP module sends an interrupt (MCBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode.
- MCBSPi.MCBSPLP_WAKEUPEN_REG[7] XSYNCERREN bit: The MCBSP module asserts the MCBSPi_SWAKEUP request when an unexpected transmits frame-sync pulse is detected. If the MCBSPi.MCBSPLP_IRQENABLE_REG[7] XSYNCERREN bit is set to 1, the MCBSP module sends an interrupt (MCBSPi_IRQ) request to the MPU or DSP subsystems when exiting idle mode (interrupt is asserted once the MCBSPi.MCBSPLP_IRQSTATUS_REG[7] XSYNCERR bit changes from 0 to 1, indicating that a transmit error occurred).

23.5.4.5.3.3 Notes

The module does not implement interrupt request (IRQ) assertion when configured as GPIO (pins that can be used to accept input signals and/or send output signals but are not linked to specific uses); also a wake-up capability in this mode is not available.

23.5.4.5.4 Analysis of the Receiver Smart-Idle Behavior

Table 23-334 provides an analysis of the power mode behavior.

In this table, the CLKRM bit is in the MCBSPi.MCBSPLP_PCR_REG register on position 8, the CLKXM bit is in the MCBSPi.MCBSPLP_PCR_REG[9] register, and the CLOCKACTIVITY bit is in the MCBSPi.MCBSPLP_SYSCONFIG_REG[9:8] register.

The value X indicates that the bit value is not significant.

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Table 23-334. MCBSP Smart-Idle Mode Configuration Behavior

CLKRM Bit	CLKXM Bit	MCBSP Mode	Source of Functional Clock	CLOCKACTIVITY Bit	Behavior
0	0	Slave	Outside	0bXX	The module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit buffer threshold synchronization (only when wake-up event is set on transmit threshold reached), regardless of the CLOCKACTIVITY settings or receive and transmit activity.
0	1	Transmit master	MCBSPi_ICLK	0b0X	The MCBSP does not acknowledge the IDLE request unless: • The transmit part is disabled (XDISABLE) or under software reset (XRST). • Transmit and receive parts are disabled (XDISABLE/RDISABLE) or under software reset (XRST/RRST). The IDLE acknowledge is asserted as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached) and the pending transmit and/or receive frames were completed in case of transmit and/or receive disable.
			MCBSPi_FCLK	0bX0	
			MCBSPi_ICLK	0b1X	The module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached).
			MCBSPi_FCLK	0bX1	
			CLKR (outside)	0bXX	The module acknowledges the idle request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached), regardless of the CLOCKACTIVITY settings.
1	0	Receive master	MCBSPi_ICLK	0b0X	The MCBSP does not acknowledge the IDLE request unless the receive part is disabled (RDISABLE) or under software reset (RRST). The IDLE acknowledge is asserted as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached) and the pending transmit and/or receive frames were completed in case of transmit and/or receive disable.
			MCBSPi_FCLK	0bX0	
			MCBSPi_ICLK	0b1X	The module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when wake-up event is set on transmit/receive threshold reached).
			MCBSPi_FCLK	0bX1	
			CLKX	0bXX	When CLKX is used as source (the functional clock is provided from outside), the module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached), regardless of the CLOCKACTIVITY settings.

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Table 23-334. MCBSP Smart-Idle Mode Configuration Behavior (continued)

CLKRM Bit	CLKXM Bit	MCBSP Mode	Source of Functional Clock	CLOCKACTIVITY Bit	Behavior
1	1	Transmit and receive master	MCBSPi_ICLK	0b0X	The MCBSP does not acknowledge the IDLE request unless transmit and receive parts are disabled (XDISABLE/RDISABLE) or under software reset (XRST/RRST). The IDLE acknowledge is asserted as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached) and the pending transmit and/or receive frames were completed in case of transmit and/or receive disable. No wake-up event is available in this mode, because the entire MCBSP and remote device activity is frozen.
			MCBSPi_FCLK	0bX0	
			MCBSPi_ICLK	0b1X	The module acknowledges the IDLE request as soon as there is no pending DMA, interrupt request, or transmit/receive buffer threshold synchronization (only when the wake-up event is set on transmit/receive threshold reached).
			MCBSPi_FCLK	0bX1	

NOTE: The RSYNCERREN/XSYNCERREN mode can be used to wake up the MCBSP module only by a remote module implementing such a feature to trigger a wakeup. In this mode, the functional clock must be active.

23.5.4.6 MCBSP Interrupt Requests

Each of the four MCBSP modules can generate one common interrupt (MCBSPi_IRQ), shared between the Cortex-A15 MPU subsystem and DSP subsystem interrupt controllers (INTCs).

An event can generate an interrupt request when the corresponding mask bit in the MCBSPi.MCBSPLP_IRQENABLE_REG register is set to 1.

Once an interrupt request is generated, software must read the MCBSPi.MCBSPLP_IRQSTATUS_REG register to check which event has caused the interrupt request generation, and acknowledge each processed event by setting the corresponding bit in the MCBSPi.MCBSPLP_IRQSTATUS_REG register to 1.

23.5.4.7 MCBSP DMA Requests

The DMA requests are shared between the DSP subsystem DMA (DMA_DSP) controller, system DMA (DMA_SYSTEM) controller, and audio engine DMA (DMA_AUDIO) controller. Each of the four MCBSP modules can generate two DMA events:

- MCBSPi_DMA_TX: MCBSPi module transmit DMA request
- MCBSPi_DMA_RX: MCBSPi module receive DMA request

Table 23-331 summaries the DMA events with the mapping on both DMA controllers.

The receive and transmit DMA requests can be individually disabled by setting the MCBSPi.MCBSPLP_RCCR_REG[3] RDMAEN and MCBSPi.MCBSPLP_XCCR_REG[3] XDMAEN bits to 0. When disabling the DMA, the DMA request line is deasserted even if a DMA transfer is pending and the DMA state-machine is not reset.

For more information, see Section 23.5.4.11, *MCBSP DMA Configuration*.

23.5.4.8 MCBSP Data Transfer Process

For MCBSP modules, receive and transmit operations are triple-buffered (512 bytes buffers organized in 32-bit words are used).

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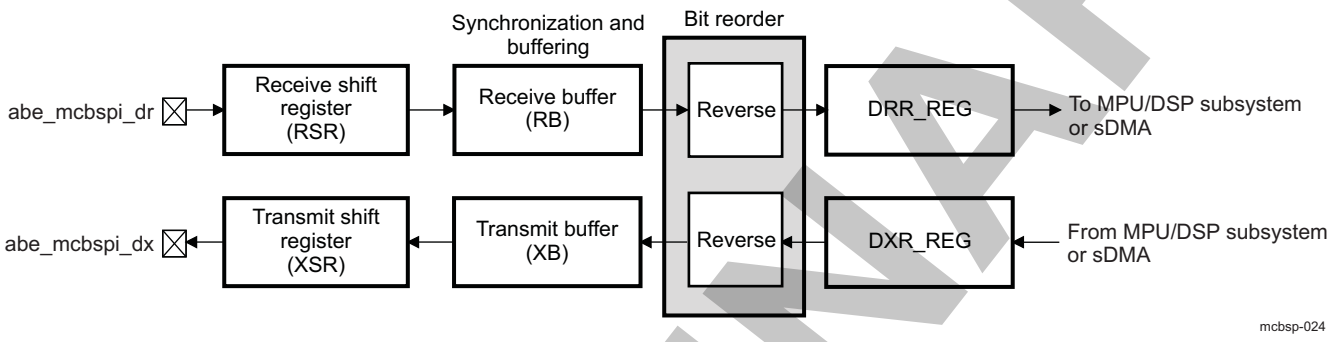
All registers of MCBSP data transfer paths are 32 bits wide. Figure 23-114 shows the MCBSP data transfer paths.

CAUTION

The MCBSP registers (DRR_REG and DXR_REG) are limited to 32-bit data accesses (L4 Interconnect); 16-and 8-bit accesses are not allowed and can corrupt register content.

Figure 23-114. MCBSP Data Transfer Paths



23.5.4.8.1 Data Transfer Process for 8-/12-/16-/20-/24-/32-Bit-Long Words

NOTE: For each data word length, one data occupies one 32-bit buffer word.

Receive data arrives on the MCBSPi_dr pin and is shifted into the receive shift register (RSR). When a full word (depending on the data length configuration) is received, the content of the shift register is copied into the receive buffer (RB) if it is not full. When the threshold of the RB is reached, the MCBSP module asserts DMA or interrupt request and the content of the RB is then transferred (the DMA_SYSTEM or the DMA_DSP controller reads the data receive register MCBSPi.MCBSPLP_DRR_REG).

Transmit data is written by the MPU subsystem, DSP subsystem, or the DMA controller to the data transmit register (MCBSPi.MCBSPLP_DXR_REG) using the MCBSPi.MCBSPLP_SPCR2_REG[1] XRDY bit enable input (when a byte is not enabled, the byte value in the memory contains the previous written value). If there is no previous data in the transmit shift register (XSR), the value from the transmit buffer (XB) is copied to the XSR; otherwise, the content is copied to the XSR when the last bit of the previous data is shifted out on the MCBSPi_dx pin.

23.5.4.8.2 Bit Reordering (Option to Transfer LSB First)

Generally, the MCBSP module transmits or receives all data with the MSB first. However, some data protocols require the LSB to be transferred first.

If the MCBSPi.MCBSPLP_XCR2_REG[4:3] XREVERSE bit field is set to 0b01, the bit ordering of the data words is reversed (LSB first) before being sent to the serial port. If MCBSPi.MCBSPLP_RCR2_REG[4:3] RREVERSE bit field is set to 0b01, the bit ordering of the data words is reversed during reception (LSB first).

This feature is available for all the data formats from 8- to 32-bit data length.

23.5.4.8.3 Clocking and Framing Data

This section explains basic concepts and terminology important for understanding how MCBSP data transfers are timed and delimited.

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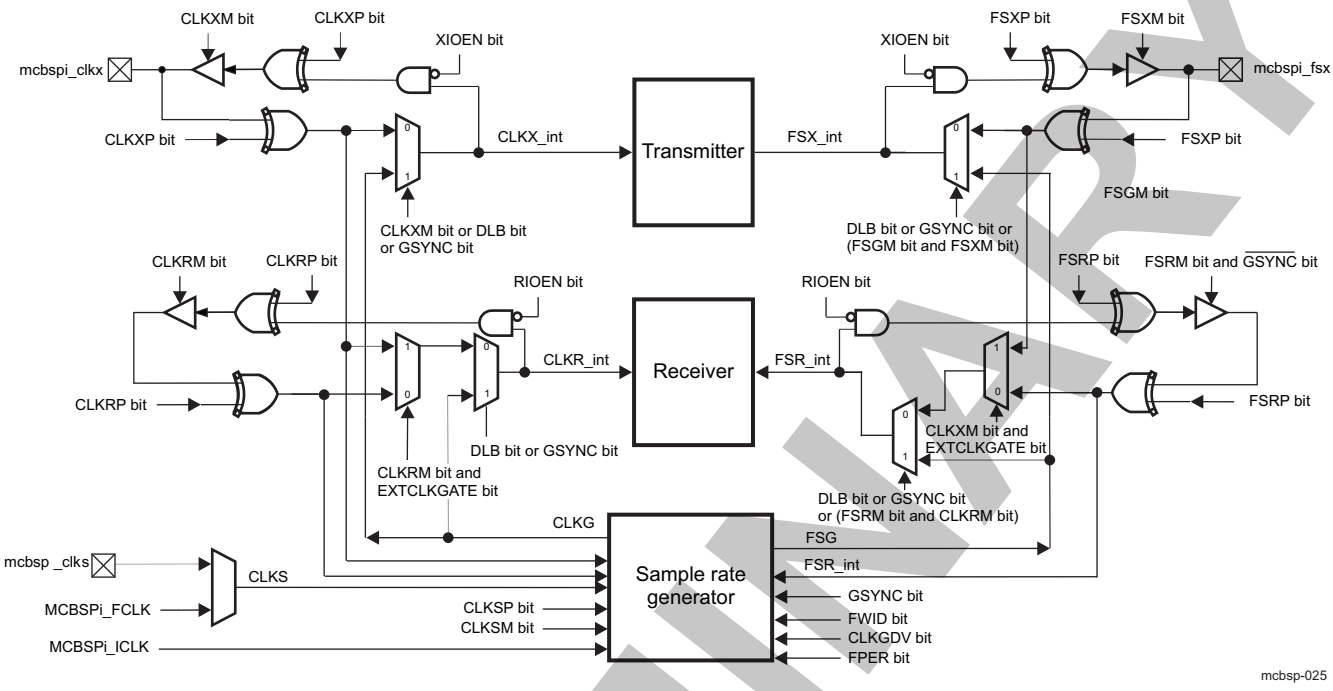
Figure 23-115. Conceptual Block Diagram for Clock and Frame Generation When MCBSPLP_SPCR1_REG[15] ALB = 0



The CLKR_int clock signal can be derived from three sources:

- The sample rate generator (CLKG): When MCBSPLP_XCCR_REG[5] DLB = 1 or MCBSPLP_SRGR2_REG[15] GSYNC = 1
- MCBSP1_clkr pin (CLKR): When MCBSPLP_PCR_REG[9] CLKXM = 0 and MCBSPLP_XCCR_REG[15] EXTCLKGATE = 0 and (MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0)
- MCBSPi_clkx pin (CLKX) : When MCBSPLP_PCR_REG[9] CLKXM = 1 and MCBSPLP_XCCR_REG[15] EXTCLKGATE = 1 and (MCBSPLP_XCCR_REG[5]DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0)

The CLKX_int clock signal can be derived from two sources:

- The sample rate generator (CLKG): When MCBSPLP_PCR_REG[9] CLKXM = 1 or MCBSPLP_XCCR_REG[5] DLB = 1 or MCBSPLP_SRGR2_REG[15] GSYNC = 1
- MCBSPi_clkx pin (CLKX) – when MCBSPLP_PCR_REG[9] CLKXM = 0 or MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0

The FSR_int frame-sync signal can be derived from three sources:

- The sample rate generator (FSG): When MCBSPLP_XCCR_REG[5] DLB = 1 or MCBSPLP_SRGR2_REG[15] GSYNC = 1 or (MCBSPLP_PCR_REG[10] FSRM = 1 and MCBSPLP_PCR_REG[8] CLKRM = 1)
- MCBSP1_fsr pin (FSR): When MCBSPLP_PCR_REG[9] CLKXM = 0 and MCBSPLP_XCCR_REG[15] EXTCLKGATE = 0 and (MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0 or (MCBSPLP_PCR_REG[10] FSRM = 0 and MCBSPLP_PCR_REG[8] CLKRM = 0))
- MCBSPi_fsx pin (FSX): When MCBSPLP_PCR_REG[9] CLKXM = 1 and MCBSPLP_XCCR_REG[15] EXTCLKGATE = 1 and (MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0 or (MCBSPLP_PCR_REG[10] FSRM = 0 and MCBSPLP_PCR_REG[8] CLKRM = 0))

The FSX_int frame-sync signal can be derived from two sources:

- The sample rate generator (FSG): When MCBSPLP_XCCR_REG[5] DLB = 1 or MCBSPLP_SRGR2_REG[15] GSYNC = 1 or (MCBSPLP_SRGR2_REG[12] FSGM = 1 and MCBSPLP_PCR_REG[11] FSXM = 1)

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- MCBSPi_fsx pin (FSX): When MCBSPLP_XCCR_REG[5] DLB = 0 or MCBSPLP_SRGR2_REG[15] GSYNC = 0 or (MCBSPLP_SRGR2_REG[12] FSGM = 0 and MCBSPLP_PCR_REG[11] FSXM = 0)

23.5.4.8.3.1 Clocking

Data is shifted 1 bit at a time from the MCBSPi_dr pin to the RSRs or from the XSRs to the MCBSPi_dx pin. The time for each bit transfer is controlled by the rising or falling edge of a clock signal.

The receive clock signal (CLKR_int) controls bit transfers from the MCBSPi_dr pin to the RSRs. The transmit clock signal (CLKX_int) controls bit transfers from the XSRs to the MCBSPi_dx pin. The CLKR_int and CLKX_int signals can be derived from inside the MCBSP module (see Figure 23-115). The clock source is selected by programming the MCBSPi.MCBSPLP_PCR_REG[9] CLKXM and MCBSPi.MCBSPLP_PCR_REG[8] CLKRM bits, respectively.

When the MCBSPi.MCBSPLP_PCR_REG[9] CLKXM bit (transmitter clock mode) is set to:

- 0: CLKX_int is driven by an external clock and MCBSPi_clkx is an input pin.
- 1: CLKX_int is driven by the internal SRG and MCBSPi_clkx is an output pin.

For the MCBSPi.MCBSPLP_PCR_REG[8] CLKRM bit (receiver clock mode), see .

The polarities of CLKR and CLKX signals are configured in MCBSPi.MCBSPLP_PCR_REG register.

The MCBSPi.MCBSPLP_PCR_REG[1] CLKXP bit defines the transmit clock polarity:

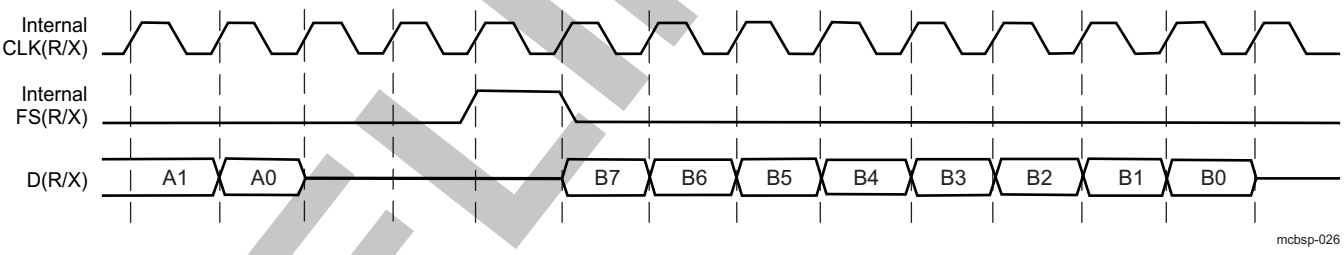
- When set to 0, transmit data is driven on the rising edge of the CLKX signal.
- When set to 1, transmit data is driven on the falling edge of the CLKX signal.

The MCBSPi.MCBSPLP_PCR_REG[0] CLKRP bit defines the receive clock polarity:

- When set to 0, receive data is sampled on the falling edge of the CLKX signal.
- When set to 1, transmit data sampled on the rising edge of the CLKX signal.

Figure 23-116 shows an example in which the clock signal controls the timing of each bit transfer on the pin.

Figure 23-116. Clock Signal Control of Bit Transfer Timing



NOTE: The MCBSP module is constrained to operate at an internal functional frequency of up to L4 interface frequency divided by 2. When driving CLKX or CLKR at the pin, choose an appropriate input clock frequency. When using the internal SRG for CLKX/CLKR/CLKS, choose an appropriate input clock frequency (up to L4 interface frequency) and divide down value by programming the MCBSPi.MCBSPLP_SRGR1_REG[7:0] CLKGDV bit field.

23.5.4.8.3.2 Serial Words

Bits traveling between a shift register (RSR or XSR) and a data pin (MCBSPi_dr or MCBSPi_dx) are transferred in a group called a serial word. Software defines how many bits are in a word by programming:

- For the receiver: The MCBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1 and MCBSPi.MCBSPLP_RCR2_REG[7:5] RWDLEN2 bit fields
- For the transmitter: The MCBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1 and MCBSPi.MCBSPLP_XCR2_REG[7:5] XWDLEN2 bit fields

The difference of use is explained in Section 23.5.4.8.4.1, *Number of Phases, Words, and Bits per Frame*.

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The various possibilities of word length are 8, 12, 16, 20, 24, and 32 bits (for field values, see Section 23.5.6, *MCBSP Register Manual*)

Bits coming from the MCBSPi_dr pin are held in the RSR until it holds a full serial word, and then the word is passed to the RB and the MCBSPi.MCBSPLP_DRR_REG register.

During transmission, the XSR accepts new data from the XB after a full serial word has been passed from the XSR to the MCBSPi_dx pin.

In the example in Figure 23-119, an 8-bit word size was defined (see the transfer of the 8-bit word B).

23.5.4.8.3.3 Frames and Frame Synchronization

One or more words (up to 128) are transferred in a group called a frame. Software defines how many words are in a frame by programming:

- For the receiver: The MCBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1 and MCBSPi.MCBSPLP_RCR2_REG[14:8] RFRLEN2 bit fields
- For the transmitter: The MCBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1 and MCBSPi.MCBSPLP_XCR2_REG[14:8] XFRLEN2 bit fields

The difference between these registers is explained in Section 23.5.4.8.4.1, *Number of Phases, Words, and Bits per Frame*. For the corresponding field values and number of words, see Section 23.5.6, *MCBSP Register Manual*.

All the words in a frame are sent in a continuous stream. However, there can be pauses between frame transfers. The MCBSP module uses frame-sync signals (FSG) to determine when each frame is received/transmitted. When a pulse occurs on a frame-sync signal, the MCBSP module begins receiving/transmitting a frame of data. When the next pulse occurs, the MCBSP module receives/transmits the next frame, and so on.

Pulses on the receive frame-sync (FSR_int) signal initiate frame transfers on MCBSPi_dr. Pulses on the transmit frame-sync (FSX_int) signal initiate frame transfers on MCBSPi_dx. FSR_int or FSX_int signals can be derived from inside the MCBSP module (see Figure 23-114). The frame-sync source is selected by programming the MCBSPi.MCBSPLP_PCR_REG[11] FSXM and MCBSPi.MCBSPLP_PCR_REG[10] FSRM bits, respectively.

When the MCBSPi.MCBSPLP_PCR_REG[11] FSXM bit (transmitter frame-sync mode) is set to:

- 0: FSX_int is derived from an external source and MCBSPi_fsx is an input pin.
- 1: FSX_int is determined by the MCBSPi.MCBSPLP_SRGR2_REG[12] FSGM bit and MCBSPi_fsx is an output pin.

For the MCBSPi.MCBSPLP_PCR_REG[10] FSRM bit (receiver frame-sync mode), is set to:

- 0: Reserved.
- 1: FSR_int is generated internally by the SRG.

In the example in Figure 23-115, a one-word frame is transferred when a frame-sync pulse occurs. The polarities of FSR and FSX signals are programmable by bits in the MCBSPi.MCBSPLP_PCR_REG register.

The MCBSPi.MCBSPLP_PCR_REG[3] FSXP bit defines the transmit frame-sync polarity:

- When set to 0, frame-sync pulse FSX is active high.
- When set to 1, frame-sync pulse FSX is active low.

The MCBSPi.MCBSPLP_PCR_REG[2] FSRP bit defines the receive frame-sync polarity:

- When set to 0, frame-sync pulse FSR is active high.
- When set to 1, frame-sync pulse FSR is active low.

In MCBSP operation, the inactive-to-active transition of the frame-sync signal indicates the start of the next frame. For this reason, the frame-sync signal may be high for an arbitrary number of clock cycles. Only after the signal is recognized to have gone inactive, and then active again, does the next frame synchronization occur.

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23.5.4.8.3.4 Detecting Frame-Sync Pulses, Even in Reset State

The MCBSP module can generate receive and transmit interrupts to the Cortex-A15 MPU/DSP subsystems to indicate specific events in the MCBSP module. To facilitate detection of frame synchronization, these interrupts can be sent in response to frame-sync pulses (see Section 23.5.5, *MCBSP Basic Programming Model* for more information).

Unlike other serial port interrupt modes, this mode can operate while the associated portion of the serial port is in reset (such as activating receive interrupt when the receiver is in reset). In this case, the MCBSPi.MCBSPLP_PCR_REG[0] FSRM/MCBSPi.MCBSPLP_PCR_REG[1] FSXM bit and the MCBSPi.MCBSPLP_PCR_REG[2] FSRP/MCBSPi.MCBSPLP_PCR_REG[3] FSXP bit still selects the appropriate source and polarity of frame synchronization. Thus, even when the serial port is in reset state, these signals are synchronized to the interface clock (MCBSPi_ICLK) and then sent to the Cortex-A15 MPU/DSP subsystem in the form of receive interrupt and transmit interrupt at the point where they feed the receiver and transmitter of the serial port. Consequently, a new frame-sync pulse can be detected, and then the Cortex-A15 MPU/DSP subsystem can take the serial port out of reset safely.

23.5.4.8.3.5 Ignoring Frame-Sync Pulses

The MCBSP module ignores transmit and/or receive frame-sync pulses if the frame transfer was started by a previous frame-sync pulse (unexpected frame-sync pulses). The MCBSP module does not support features such as retransmit or re-receive of an erroneous frame or word. The receiver or transmitter ignores frame-sync pulses until the desired frame length or number of words is reached. For more information about unexpected frame-sync pulses, see Section 23.5.4.10.3, *Unexpected Receive Frame-Sync Pulse*, or Section 23.5.4.10.6, *Unexpected Transmit Frame-Sync Pulse*.

23.5.4.8.3.6 Frame Frequency

The frame frequency is determined by the period between frame-sync pulses and is defined as shown in the following equation:

Frame frequency = Clock frequency/(number of clock cycles between two rising edges [or falling edges] of two consecutive frame-sync pulses)

The frame frequency can be increased by decreasing the time between frame-sync pulses (limited only by the number of bits per frame). As the frame transmit frequency increases, the inactivity period between the data packets for adjacent transfers decreases to zero.

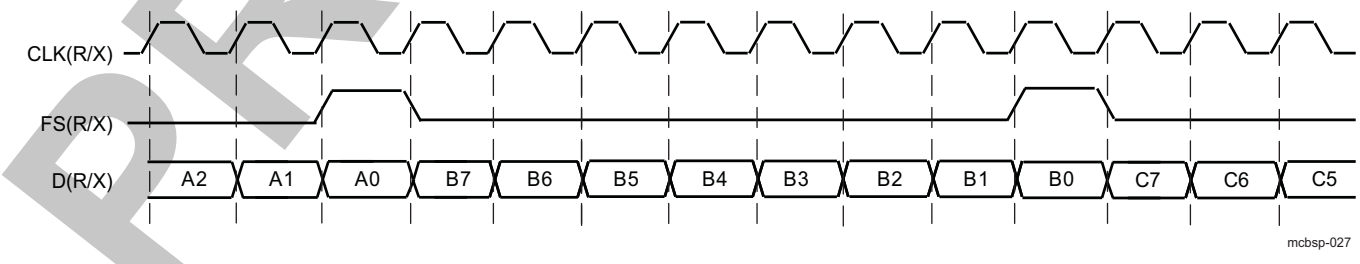
23.5.4.8.3.7 Maximum Frame Frequency

The minimum number of clock cycles between frame-sync pulses is equal to the number of bits transferred per frame. The maximum frame frequency is defined as shown in the following equation:

Maximum frame frequency = Clock frequency/number of bits per frame

Figure 23-117 shows the MCBSP operating at maximum packet frequency. At maximum packet frequency, the data bits in consecutive packets are transmitted contiguously with no inactivity between bits.

Figure 23-117. MCBSP Operating at Maximum Packet Frequency



If there is a 1-bit data delay as shown in Figure 23-117, the frame-sync pulse overlaps the last bit transmitted in the previous frame. Effectively, this permits a continuous stream of data, back-to-back transfers.

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NOTE: When the MCBSPi.MCBSPLP_XCR2_REG[1:0] XDATDLY bit field is se to 0x0 (0-bit data delay), the first bit of data is transmitted asynchronously to the internal transmit clock signal (CLKX_int). For more information, see Table 23-383.

23.5.4.8.4 Frame Phases (Dual-Phase Frame I2S Support)

The MCBSP module allows configuration of each frame to contain one or two phases. The support for dual-phase frames is required to provide I2S fully compliant capabilities (audio left and right channels—stereo audio stream).

CAUTION

The limitation on dual-phase frame support is that the number of words per phase must be set to 1 for both first and second phases. It is the only possible value for word per frame when using the dual-phase frame.

The number of bits per word can be specified differently for each of the two phases of a frame, allowing greater flexibility in structuring data transfers. For example, a user may define a frame as consisting of one phase containing one 16-bit word, followed by a second phase consisting of one 32-bit word. This configuration allows the user to compose frames for custom applications such as I2S protocol.

23.5.4.8.4.1 Number of Phases, Words, and Bits per Frame

Table 23-335 shows which bit fields in the receive control registers (MCBSPi.MCBSPLP_RCR1_REG and MCBSPi.MCBSPLP_RCR2_REG) and in the transmit control registers (MCBSPi.MCBSPLP_XCR1_REG and MCBSPi.MCBSPLP_XCR2_REG) determine the number of phases per frame, the number of words per frame, and the number of bits per word for each phase, for both receiver and transmitter. The maximum number of words per frame is limited to 2 when using dual-phase frames (one word for each phase), and to 128 for a single-phase frame. The number of bits per word can be 8, 12, 16, 20, 24, or 32 bits.

The following legend applies to Table 23-335:

- RPHASE => MCBSPi.MCBSPLP_RCR2_REG[15] RPHASE bit
- XPHASE => MCBSPi.MCBSPLP_XCR2_REG[15] XPHASE bit
- RFRLEN1 => MCBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1 bit field
- RFRLEN2 => MCBSPi.MCBSPLP_RCR2_REG[14:8] RFRLEN2 bit field
- XFRLEN1 => MCBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1 bit field
- XFRLEN2 => MCBSPi.MCBSPLP_XCR2_REG[14:8] XFRLEN2 bit field
- RWDLEN1 => MCBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1 bit field
- RWDLEN2 => MCBSPi.MCBSPLP_RCR2_REG[7:5] RWDLEN2 bit field
- XWDLEN1 => MCBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1 bit field
- XWDLEN2 => MCBSPi.MCBSPLP_XCR2_REG[7:5] XWDLEN2 bit field

Table 23-335. Phases, Words and Bits per Frame Control Bit

Operation	Number of Phases	Words per Frame Set With	Bits per Word Set With
Reception	1 (RPHASE = 0)	RFRLEN1	RWDLEN1
Reception	2 (RPHASE = 1)	RFRLEN1 = 0x0 and RFRLEN2 = 0x0	RWDLEN1 for phase 1 RWDLEN2 for phase 2
Transmission	1 (XPHASE = 0)	XFRLEN1	XWDLEN1
Transmission	2 (XPHASE = 1)	XFRLEN1 = 0x0 and XFRLEN2 = 0x0	XWDLEN1 for phase 1 XWDLEN2 for phase 2

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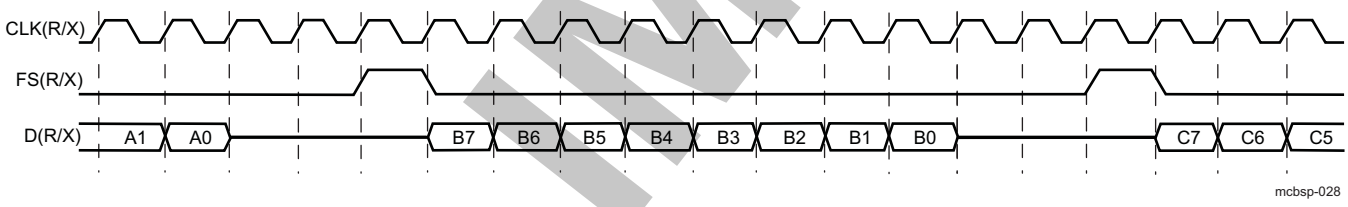
23.5.4.8.4.2 Single-Phase Frame Example

Figure 23-118 shows an example of a single-phase data frame containing one 8-bit word. Because the transfer is configured for one data bit delay, the data on the MCBSPi_dx and MCBSPi_dr pins are available one clock cycle after FS(R/X) goes active. Table 23-336 lists the assumptions used in the example in Figure 23-118.

Table 23-336. Assumptions for the Single-Phase Frame Example

Assumption	Value	Bit or Field Name
Single-phase frame	0	MCBSPi.MCBSPLP_RCR2_REG[15] RPHASE
		MCBSPi.MCBSPLP_XCR2_REG[15] XPHASE
One word per frame	0x0	MCBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1
		MCBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1
8-bit word length	0x0	MCBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1
		MCBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1
Word length in register2	Ignored	MCBSPi.MCBSPLP_RCR2_REG[14:8] RFRLEN2
		MCBSPi.MCBSPLP_XCR2_REG[14:8] XWDLEN2
Receive data clocked on falling edge	0	MCBSPi.MCBSPLP_PCR_REG[0] CLKRP
Transmit data clocked on rising edge		MCBSPi.MCBSPLP_PCR_REG[1] CLKXP
Active-high frame-sync signals	0	MCBSPi.MCBSPLP_PCR_REG[2] FSRP
		MCBSPi.MCBSPLP_PCR_REG[3] FSXP
1-bit data delay	01b	MCBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY
		MCBSPi.MCBSPLP_XCR2_REG[1:0] XDARDLY

Figure 23-118. Single-Phase Frame for a MCBSP Data Transfer



23.5.4.8.4.3 Dual-Phase Frame Example

Figure 23-119 shows an example of a frame. The first phase consists of one word of 16 bits, followed by a second phase of one word of 8 bits. The entire bitstream in the frame is contiguous. There are no gaps between words/phases. Table 23-337 lists the assumptions used in the example in Figure 23-119.

Table 23-337. Assumptions for the Dual-Phase Frame Example

Assumption	Value	Bit or Field Name
Single-phase frame	1	MCBSPi.MCBSPLP_RCR2_REG[15] RPHASE
		MCBSPi.MCBSPLP_XCR2_REG[15] XPHASE
One word per frame	0x0	MCBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1
		MCBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1
16-bit word length	0x0	MCBSPi.MCBSPLP_RCR1_REG[7:5] RWDLEN1
		MCBSPi.MCBSPLP_XCR1_REG[7:5] XWDLEN1
8-bit word length	0x2	MCBSPi.MCBSPLP_RCR2_REG[14:8] RFRLEN2
		MCBSPi.MCBSPLP_XCR2_REG[14:8] XWDLEN2
Receive data clocked on falling edge	0	MCBSPi.MCBSPLP_PCR_REG[0] CLKRP
Transmit data clocked on rising edge		MCBSPi.MCBSPLP_PCR_REG[1] CLKXP
Active-high frame-sync signals	0	MCBSPi.MCBSPLP_PCR_REG[2] FSRP
		MCBSPi.MCBSPLP_PCR_REG[3] FSXP

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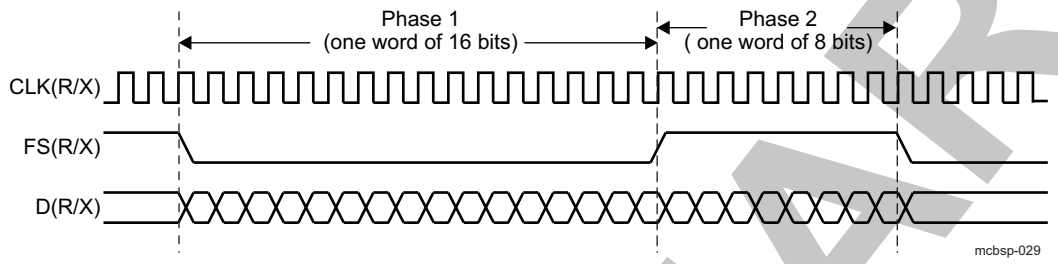
Table 23-337. Assumptions for the Dual-Phase Frame Example (continued)

Assumption	Value	Bit or Field Name
0-bit data delay	00b	MCBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY
		MCBSPi.MCBSPLP_XCR2_REG[1:0] XDARDLY

Figure 23-119. Dual-Phase Frame for a MCBSP Data Transfer



23.5.4.8.5 MCBSP Reception

This section explains the fundamental process of reception in the MCBSP module. For information about how to program the MCBSP receiver, see Section 23.5.5, *MCBSP Basic Programming Model*, Section 23.5.5.4, *Interrupt Configuration*, and Section 23.5.5.5, *Receiver Configuration*.

Figure 23-120 and Figure 23-121 show how reception occurs in the MCBSP module. A description of the process follows the figures. Figure 23-120 shows the physical path for the data.

Figure 23-120. MCBSP Reception Physical Data Path

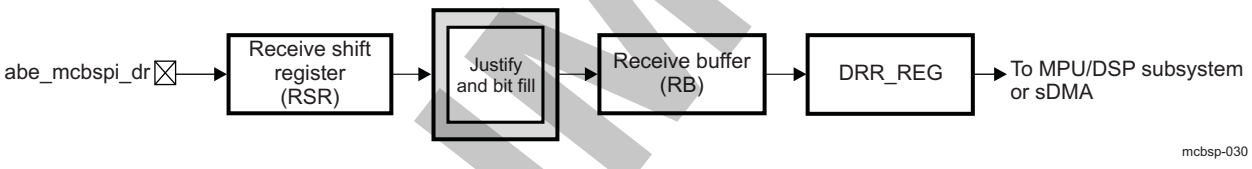
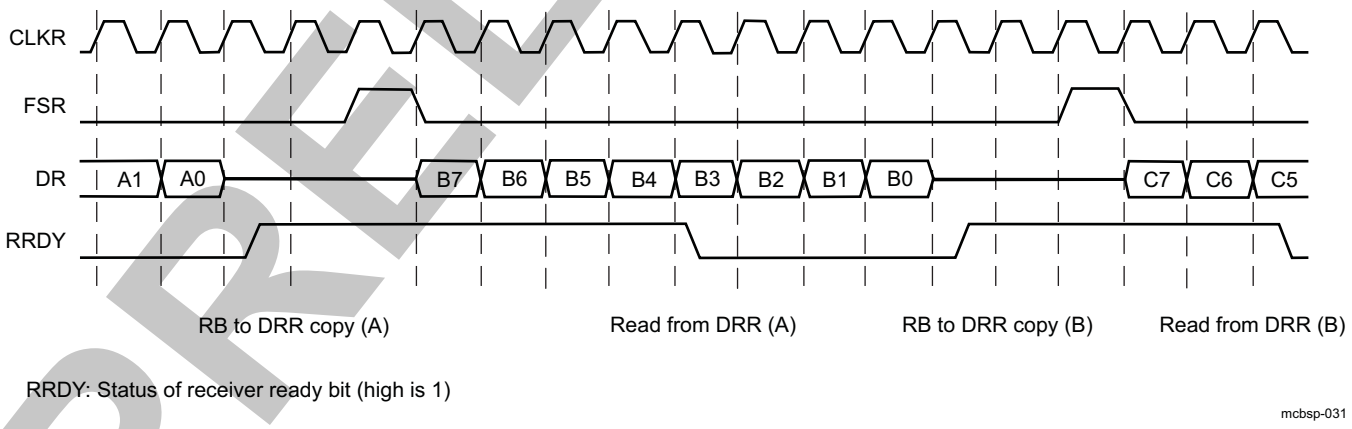


Figure 23-121 is a timing diagram showing signal activity for one possible reception scenario.

Figure 23-121. MCBSP Reception Signal Activity



The following process describes how data travels from the MCBSPi_dr pin to the MPU/DSP subsystem or to the sDMA controller:

1. The MCBSP module waits for a receive frame-sync pulse on FSR_int.
2. When the pulse arrives, the MCBSP module inserts the appropriate data delay that is selected with the MCBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY bit field. In the preceding timing diagram a 1-bit data delay is selected.

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3. The MCBSP module accepts data bits on the MCBSPi_dr pin and shifts them into the RSR. For information about choosing a word length, see Section 23.5.5.6, *Transmitter Configuration*.
4. When a full word is received, the MCBSP module copies the contents of the RSR to the RB, provided that RB is not full.
5. When the programmed receive threshold is reached (MCBSPi.MCBSPLP_THRSH1_REG[6:0] RTHRESHOLD bit field), the MCBSP module asserts the receiver ready bit (MCBSPi.MCBSPLP_SPCR1_REG[1] RRDY). This indicates that receive data is ready to be read by the Cortex-A15 MPU/DSP subsystem or the sDMA controller by accessing the MCBSPi.MCBSPLP_DRR_REG register.

   The data copied from RB to MCBSPi.MCBSPLP_DRR_REG is justified and bit-filled according to the MCBSPi.MCBSPLP_SPCR1_REG[14:13] RJUST bit field.
6. The Cortex-A15 MPU/DSP subsystem or the sDMA controller reads the data from the data receive register. When the RB is empty, the MCBSPi.MCBSPLP_SPCR1_REG[1] RRDY bit is cleared.

23.5.4.8.6 MCBSP Transmission

This section explains the fundamental process of transmission in the MCBSP module. For information about how to program the MCBSP transmitter, see Section 23.5.5, *MCBSP Basic Programming Model* and Section 23.5.5.6, *Transmitter Configuration*.

Figure 23-122 and Figure 23-123 show how transmission occurs in the MCBSP module. A description of the process follows the figures. Figure 23-122 shows the physical path for the data.

Figure 23-122. MCBSP Transmission Physical Data Path

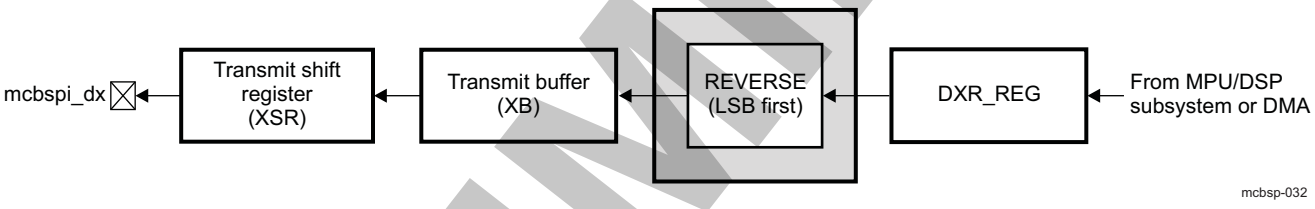
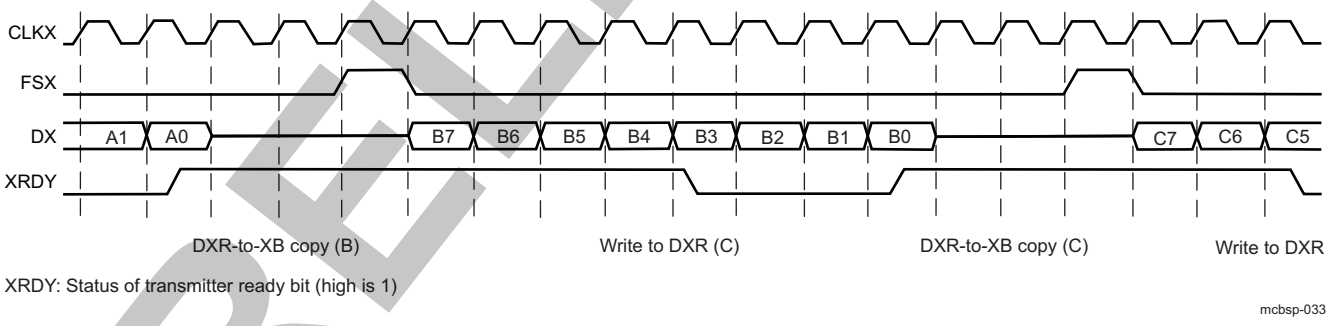


Figure 23-123 is a timing diagram showing signal activity for one possible transmission scenario.

Figure 23-123. MCBSP Transmission Signal Activity



1. The Cortex-A15 MPU/DSP subsystem or the sDMA controller writes data to the data transmit register (MCBSPi.MCBSPLP_DXR_REG). When the XB is reached the transmitter ready bit (MCBSPi.MCBSPLP_SPCR2_REG[1] XRDY) is cleared to indicate that the transmitter is not ready for new data. For information about choosing a word length, see Table 23-379.
2. When new data arrives in the MCBSPi.MCBSPLP_DXR_REG register, the MCBSP module copies the content of the data transmit register to the XB. In addition, the transmit ready bit (MCBSPi.MCBSPLP_SPCR2_REG[1] XRDY) is set as long as the buffer contains at least the transmit threshold number of free locations (the MCBSPi.MCBSPLP_THRSH2_REG[6:0] XTHRESHOLD bit field). This indicates that the transmitter is ready to accept new data from the MPU/DSP subsystem or the sDMA controller.
3. The MCBSP module waits for a transmit frame-sync pulse on FSX_int.
4. When the pulse arrives, the MCBSP module inserts the appropriate data delay that is selected with the

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MCBSPi.MCBSPLP_XCR2_REG[1:0] XDATDLY bit field.

In the preceding timing diagram, a 1-bit data delay is selected.

5. The MCBSP module shifts data bits from the XSR to the MCBSPi_dx pin.

23.5.4.8.7 Enable/Disable the Transmit and Receive Processes

The MCBSP module has the option to stop and resume the transmit/receive process while the module is in functional mode (out of transmit/receive reset).

When the transmit/receive disable bit (MCBSPi.MCBSPLP_XCCR_REG[0] XDISABLE/MCBSPi.MCBSPLP_RCCR_REG[0] RDISABLE) is set, the MCBSP module stops the transmit/receive operation at the next frame boundary (frame corruption avoided).

During the receive disable state, the frames that are sent (when the FSR signal is asserted while receive disable) by the remote device are lost, and the receive buffer overflow status bit (MCBSPi.MCBSPLP_IRQSTATUS_REG[5] ROVFLSTAT) is not set. Also, the frames received by the remote device while the MCBSPi.MCBSPLP_XCCR_REG[0] XDISABLE bit is set (when the FSX signal is asserted while transmit disable) are meaningless undefined data frames, and transmit buffer underflow status bit (MCBSPi.MCBSPLP_IRQSTATUS_REG[11] XUNDFLSTAT) is not set. The presence of the frame synchronization while transmit/receive process is disabled can be checked by reading the transmit/receive frame-sync interrupt status: MCBSPi.MCBSPLP_IRQSTATUS_REG[8] XFSX/MCBSPi.MCBSPLP_IRQSTATUS_REG[1] RFSR bits.

As soon as the MCBSPi.MCBSPLP_XCCR_REG[0] XDISABLE/MCBSPi.MCBSPLP_RCCR_REG[0] RDISABLE bit is cleared, the transmit/receive process resumes at the next frame boundary.

NOTE: It is not recommended to use this mechanism together with the possibility to interrogate the transmit/receive buffer status register (MCBSPi.MCBSPLP_XBUFFSTAT_REG[7:0] XBUFFSTAT/MCBSPi.MCBSPLP_RBUFFSTAT_REG[7:0] RBUFFSTAT bit field indicating the occupied/available buffer locations), because this register is an interface clock (MCBSPi_ICLK) synchronous register and does not reflect the exact number of occupied/free locations available in the functional clock domain.

23.5.4.8.8 MCBSP Data Transfer Mode

NOTE: For all examples in this section, the configured CLKX edge is the rising edge (MCBSPi.MCBSPLP_PCR_REG[1] CLKXP = 0x0) and the configured CLKR edge is the falling edge (MCBSPi.MCBSPLP_PCR_REG[0] CLKRP = 0x0). These are the reset values.

In the following timing diagrams, a 1-bit data delay is selected (MCBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY = 0x01 and MCBSPi.MCBSPLP_XCR2_REG[1:0] XDATDLY = 0x01), because data often follows a 1-cycle active frame-synchronization.

MCBSP modules can support two edge selection modes for transmit and receive data transfer at the system level:

- The full-cycle mode, for which one clock period is used to transfer the data, generated on one edge and captured on the same edge (one clock period later)
- The half-cycle mode, for which one-half clock period is used to transfer the data, generated on one edge and captured on the opposite edge (one-half clock period later). New data are generated only every clock period, which ensures the required hold time.

23.5.4.8.8.1 Transmit Full-Cycle Mode

When configured in full-cycle mode (MCBSPi.MCBSPLP_XCCR_REG[11] XFULL_CYCLE = 0x1), the FSX signal is sampled on the configured CLKX edge and the data is driven on the same configured edge. See Figure 23-124.

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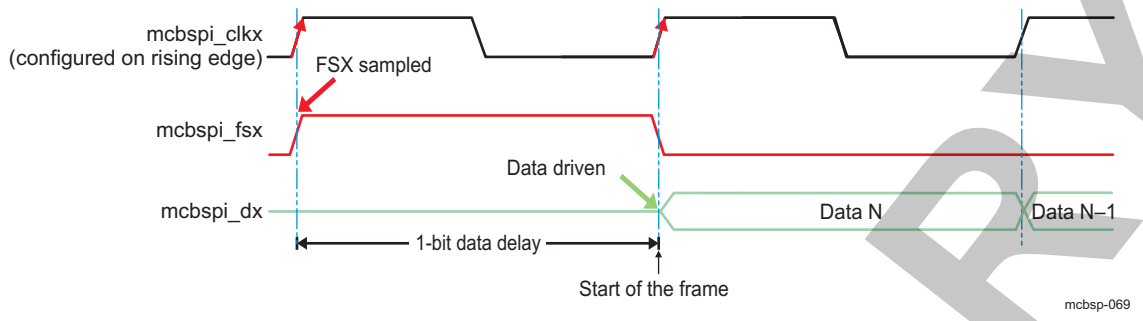
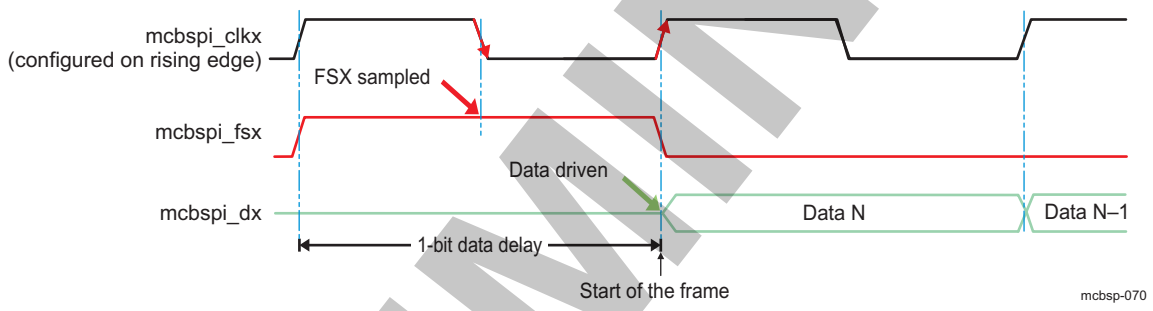
Figure 23-124. Transmit Full-Cycle Timing Diagram



23.5.4.8.8.2 Transmit Half-Cycle Mode

When configured in half-cycle mode (MCBSPi.MCBSPLP_XCCR_REG[11] XFULL_CYCLE = 0x0, reset value), the FSX signal is sampled on the opposite configured CLKX edge and the data is driven on the next configured edge. See Figure 23-125.

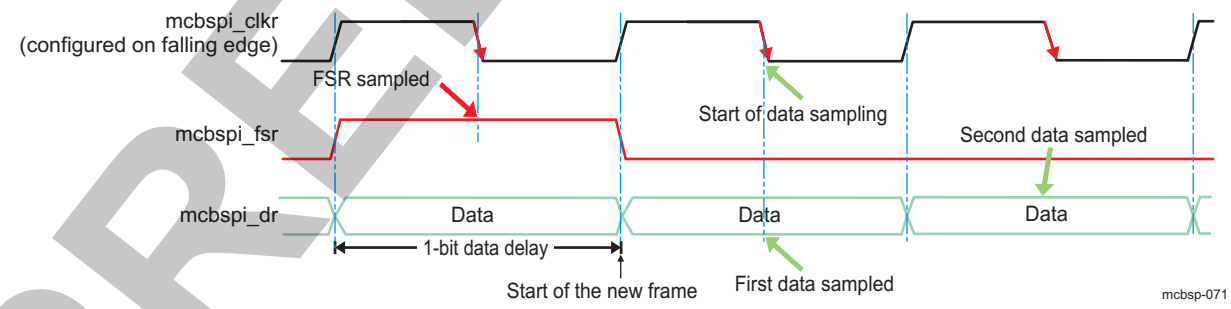
Figure 23-125. Transmit Half-Cycle Timing Diagram



23.5.4.8.8.3 Receive Full-Cycle Mode

When configured in full-cycle mode (MCBSPi.MCBSPLP_RCCR_REG[11] RFULL_CYCLE = 0x1, reset value), the FSR signal is sampled on the configured CLKR edge and the data is driven on the same configured edge. See Figure 23-126.

Figure 23-126. Receive Full-Cycle Timing Diagram



23.5.4.8.8.4 Receive Half-Cycle Mode

When configured in half-cycle mode (MCBSPi.MCBSPLP_RCCR_REG[11] RFULL_CYCLE = 0x0), the FSR signal is sampled on the opposite configured CLKR edge and the data is driven on the next configured edge. See Figure 23-127.

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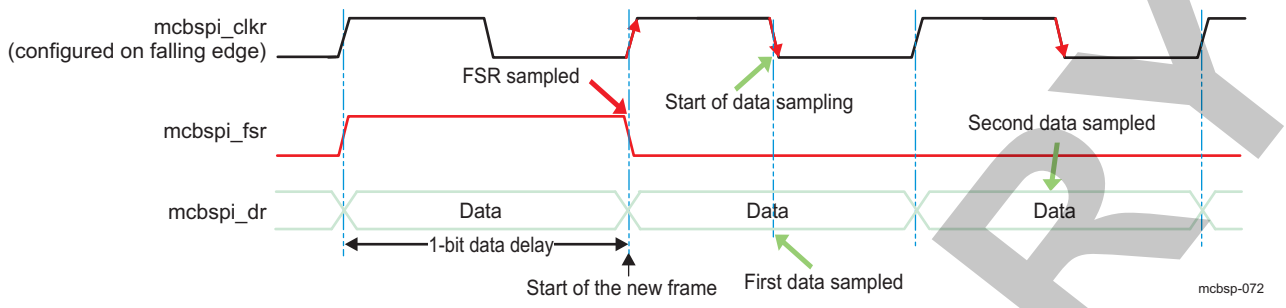
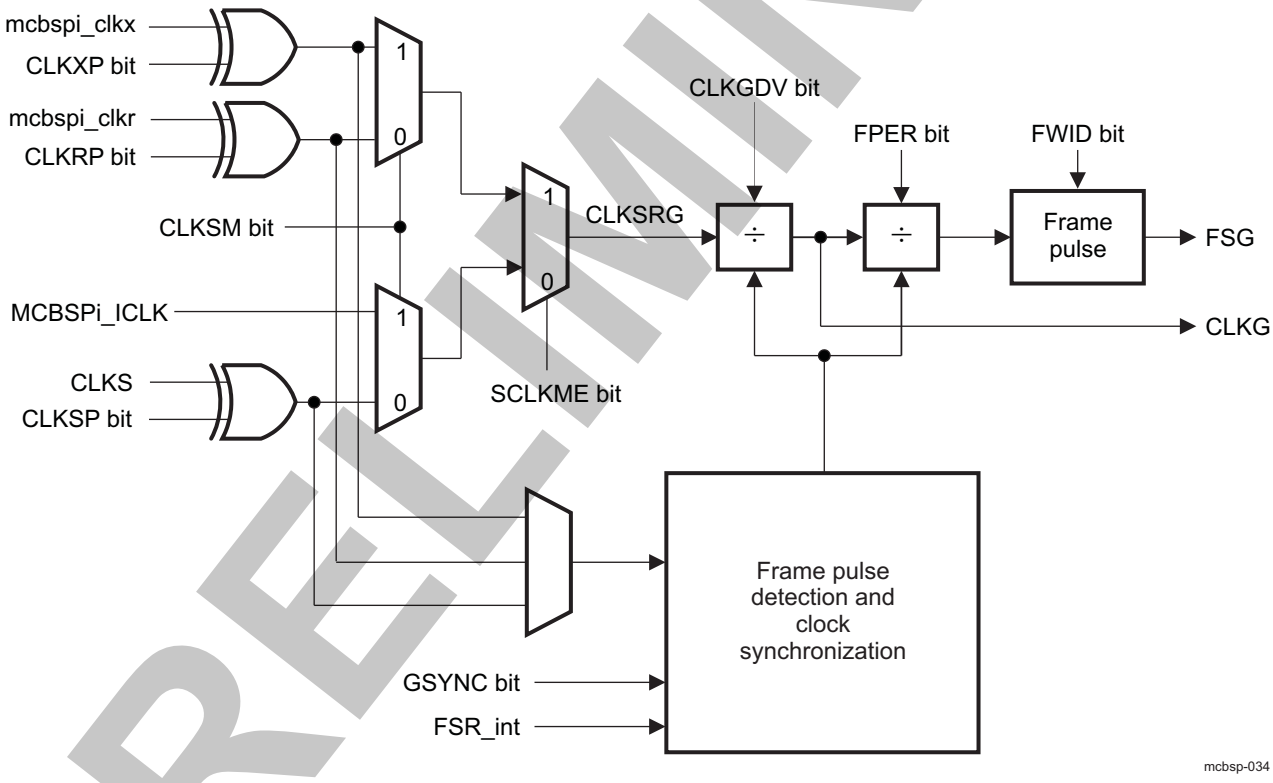
Figure 23-127. Receive Half-Cycle Timing Diagram



23.5.4.9 MCBSP SRG

The MCBSP module contains an internal SRG that can be used to generate an internal data clock (CLKG) and an internal frame-sync signal (FSG). CLKG can be used for bit shifting on the data receive pin (MCBSPi_dr) and/or the data transmit pin (MCBSPi_dx). FSG can be used to initiate frame transfers on the MCBSPi_dr pin and/or MCBSPi_dx pin. Figure 23-128 is a conceptual block diagram of the SRG.

Figure 23-128. Conceptual Block Diagram of the SRG



The source clock for the SRG (labeled CLKSRG in the diagram) can be supplied by the interface clock (MCBSPi_ICLK) or the functional clock (MCBSPi_FCLK input), or by an external pin (MCBSPi_clkx). The source is selected with the MCBSPi.MCBSPLP_PCR_REG[7] SCLKME bit and the MCBSPi.MCBSPLP_SRGR2_REG[13] CLKSM bit.

If a pin or CLKS signal is used, the polarity of the incoming signal can be inverted with the appropriate polarity bit (MCBSPi.MCBSPLP_SRGR2_REG[14] CLKSP, MCBSPi.MCBSPLP_PCR_REG[1] CLKXP, or MCBSPi.MCBSPLP_PCR_REG[0] CLKRP).

The SRG has a 3-stage clock divider that gives CLKG and FSG programmability.

The three stages provide:

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- Clock divide-down: The source clock (CLKSRG) is divided according to the MCBSPi.MCBSPLP_SRGR1_REG[7:0] CLKGDV bit field to produce the CLKG signal.
- Frame period divide-down: CLKG is divided according to the MCBSPi.MCBSPLP_SRGR2_REG[11:0] FPER bit field to control the period from the start of a frame-pulse to the start of the next pulse.
- Frame-sync pulse-width countdown: CLKG cycles are counted according to the MCBSPi.MCBSPLP_SRGR1_REG[15:8] FWID bit field to control the width of each frame-sync pulse.

NOTE: The MCBSP module cannot operate at an internal functional frequency faster than L4 interface frequency divided by 2. Choose an input clock frequency and a MCBSPi.MCBSPLP_SRGR1_REG[7:0] CLKGDV value such that CLKG is less than or equal to L4 interface frequency divided by 2.

CLKG is used as source to generate the output clocks CLKX and CLKR when the MCBSPi.MCBSPLP_PCR_REG[9] CLKXM/MCBSPi.MCBSPLP_PCR_REG[8] CLKRM bit indicates that the clock is an output. The output CLKX/CLKR is generated according to the clock polarity setting (see Figure 23-115).

For information about preparing the SRG for operation, see Section 23.5.5, *MCBSP Basic Programming Model*.

23.5.4.9.1 Clock Generation in the SRG

The SRG can produce a clock signal (CLKG) for use by the receiver, the transmitter, or both. Use of the SRG to drive clocking is controlled by the clock mode bits (MCBSPi.MCBSPLP_PCR_REG[9] CLKXM and MCBSPi.MCBSPLP_PCR_REG[8] CLKRM) and polarity mode bits (MCBSPi.MCBSPLP_PCR_REG[1] CLKXP and MCBSPi.MCBSPLP_PCR_REG[0] CLKRP).

When a clock mode bit is set to 1 (CLKRM = 1 for reception, CLKXM = 1 for transmission), the corresponding data clock (CLKR for reception, CLKX for transmission) is driven by the internal SRG output clock (CLKG) according to the polarity setting.

The effects of this setting on the MCBSP module are partially affected by use of the digital loopback (DLB) mode, the analog loopback (ALB) mode, and by the synchronous receive/transmit setting, respectively, as described in Table 23-338. ALB mode is selected with the MCBSPi.MCBSPLP_SPCR1_REG[15] ALB bit. DLB mode is selected with the MCBSPi.MCBSPLP_XCCR_REG[5] DLB bit. The synchronous setting is controlled by input signals. These signals are defined by the control registers of the control module (for more information, see Section 18.4.8*Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, of *Chapter 18, Control Module*).

When using the SRG as a clock source, ensure that the SRG is enabled (the MCBSPi.MCBSPLP_SPCR2_REG[6] GRST bit is set to1).

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Table 23-338. Effects of DLB and ALB Bits on Clock Modes

Mode Bit Settings		Effect
CLKRM=1	DLB = 0 and ALB = 0 (Digital and analog loopback mode disabled)	MCBSP1_clkr is an output pin driven by the SRG output clock (CLKG).
	DLB = 0 and ALB = 1 (Digital loopback mode disabled and analog loopback mode enabled)	MCBSP1_clkr is an output pin driven by the SRG output clock (CLKG). The receiver functional part internal clock is driven by the CLKX input signal provided by the MCBSPi_clkx pin. The source of CLKX depends on the CLKXM bit. The receive frame synchronization is driven by the FSX input signal provided by the MCBSPi_fsx pin. The receive data is driven by the DX input loopback pin (MCBSPi_dx).
	DLB = 1 and ALB = 0 (Digital loopback mode enabled and analog loopback mode disabled)	The SRG and the frame-sync generator must be enabled. The internal transmit and receive clocks are driven by the SRG (CLKG having the appropriate CLKXP polarity). The transmit and receive frame-sync signals are driven by the FSG (having the appropriate FSXP polarity). The transmit data is connected to the DR input data. In digital loopback mode, no serial link activity is seen by the remote device.
	DLB = 1 and ALB = 1 (Reserved mode)	Undefined functionality.
CLKXM=1	DLB = 0 and ALB = 0 (Digital and analog loopback mode disabled)	MCBSPi_clkx is an output pin driven by the SRG output clock (CLKG).
	DLB = 0 and ALB = 1 (Digital loopback mode disabled and analog loopback mode enabled)	MCBSPi_clkx is an output pin driven by the SRG output clock (CLKG).
	DLB = 1 and ALB = 0 (Digital loopback mode enabled and analog loopback mode disabled)	The SRG and the frame-sync generator must be enabled. The internal transmit and receive clocks are driven by the SRG (CLKG having the appropriate CLKXP polarity). The transmit and receive frame-sync signals are driven by the FSG (having the appropriate FSXP polarity). The transmit data is connected to the DR input data. In digital loopback mode, no serial link activity is seen by the remote device.
	DLB = 1 and ALB = 1 (Reserved mode)	Undefined functionality
	CONTROL_MCBSPLP[30] ALBCTRLRX_CLKX bit = 1 (synchronous setting and DLB = 0 and ALB = 0)	CLKX is an output pin driven by the SRG output clock (CLKG). CLKR is connected to the CLKX.

23.5.4.9.2 Frame-Sync Generation in the SRG

The SRG can produce a frame-sync signal (FSG) for use by the receiver, the transmitter, or both.

For the receiver to use FSG for frame synchronization, make sure the MCBSPi.MCBSPLP_PCR_REG[10] FSRM bit is set to 1.

For the transmitter to use FSG for frame synchronization, the following bits must be set:

- MCBSPi.MCBSPLP_PCR_REG[11] FSXM = 1: This indicates that transmit frame synchronization is supplied by the MCBSP module rather than from the MCBSPi_fsx pin.
- MCBSPi.MCBSPLP_SRGR2_REG[12] FSGM = 1: This indicates that when FSXM is set to 1, transmit frame synchronization is supplied by the SRG.

NOTE: When FSGM = 0 and FSXM = 1, the transmit frame-sync signal (FSX) is generated when XB is not empty. When FSGM = 0, the MCBSPi.MCBSPLP_SRGR2_REG[11:0] FPER and MCBSPi.MCBSPLP_SRGR1_REG[15:8] FWID bit fields are used to determine the frame-sync period and width (external FSX is gated by the buffer empty condition).

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In either case, the SRG must be enabled (the MCBSPi.MCBSPLP_SPCR2_REG[6] GRST bit is set to 1) and the frame-sync logic in the SRG must be enabled (the MCBSPi.MCBSPLP_SPCR2_REG[7] FRST bit is set to 0).

23.5.4.9.2.1 Choosing the Width of the Frame-Sync Pulse

Each pulse on FSG has a programmable width. Program the MCBSPi.MCBSPLP_SRGR1_REG[15:8] FWID bit field, and the resulting pulse width is (FWID + 1) CLKG cycles, where CLKG is the output clock of the SRG. The range is from 1 to 256 clock periods.

23.5.4.9.2.2 Controlling the Period Between the Starting Edges of Frame-Sync Pulses

The user can control the amount of time from the starting edge of one FSG pulse to the starting edge of the next FSG pulse. This period is controlled in one of two ways, depending on the configuration of the SRG:

- Software programs the MCBSPi.MCBSPLP_SRGR2_REG[11:0] FPER bit field, and the resulting frame-sync period is (FPER + 1) CLKG cycles, where CLKG is the output clock of the SRG. The range is from 1 to 4096 clock periods.

23.5.4.9.3 Synchronizing SRG Outputs to an External Clock

The SRG can produce a clock signal (CLKG) and an FSG based on an input clock signal that is either:

- The interface clock signal (MCBSPi_ICLK)
- The functional clock signal (MCBSPi_FCLK)
- The MCBSPi_clkx pin

If the MCBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit is set to 0, the CLKG signal runs freely and is not resynchronized, and the frame-sync period on the FSG signal is determined by the MCBSPi.MCBSPLP_SRGR2_REG[11:0] FPER bit field.

23.5.4.9.3.1 Operating the Transmitter Synchronously With the Receiver

When the MCBSPi.MCBSPLP_SRGR2_REG[15] GSYNC bit is set to 1, the transmitter can operate synchronously with the receiver, provided that the FSX signal is programmed to be driven by the FSG signal (MCBSPi.MCBSPLP_SRGR2_REG[12] FSGM = 1 and MCBSPi.MCBSPLP_PCR_REG[11] FSXM = 1). If the FSR input signal has appropriate timing so that it can be sampled by the falling edge of the CLKG signal, it can be used, instead, by setting the MCBSPi.MCBSPLP_PCR_REG[11] FSXM bit to 0 and connecting the FSR signal to FSX externally.

The SRG clock drives the transmit and receive clocking (the MCBSPi.MCBSPLP_PCR_REG[8] CLKRM and MCBSPi.MCBSPLP_PCR_REG[9] CLKXM bits are set to 1). Therefore, the CLK(R/X) pin must not be driven by any other driving source.

23.5.4.10 MCBSP Exception/Error Conditions

23.5.4.10.1 Introduction

Several serial port events can constitute a system error. Any error condition can be a source of an interrupt:

- Receiver overrun (the MCBSPi.MCBSPLP_IRQSTATUS_REG[5] ROVFLSTAT bit is set to 1, and the legacy mode MCBSPi.MCBSPLP_SPCR1_REG[2] RFULL bit is set to 1)

  This occurs when the RB is full and the RSR is full with another new word shifted in from MCBSPi_dr. Therefore, the MCBSPi.MCBSPLP_IRQSTATUS_REG[5] ROVFLSTAT bit (MCBSPi.MCBSPLP_SPCR1_REG[2] RFULL) indicates an error condition wherein any new data that can arrive at this time on MCBSPi_dr replaces the contents of the RSR, and the previous word is lost. The RSR continues to be overwritten as long as new data arrives on MCBSPi_dr and the MCBSPi.MCBSPLP_DRR_REG register is not read. For more information about overrun in the receiver, see Section 23.5.4.10.2, *Overrun in the Receiver*.
- Unexpected receive frame-sync pulse (the MCBSPi.MCBSPLP_IRQSTATUS_REG[0] RSYNCERR bit

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is set to 1, and the legacy mode MCBSPi.MCBSPLP_SPCR1_REG[3] RSYNCERR bit is set to 1)

This occurs during reception when an unexpected frame-sync pulse arrives. An unexpected frame-sync pulse is one that is supposed to begin the next frame transfer before all the bits of the current frame are received. Such a pulse is ignored by the receiver, but sets the MCBSPi.MCBSPLP_SPCR1_REG[3] RSYNCERR bit. For more information about receive frame-sync errors, see Section 23.5.4.10.3, *Unexpected Receive Frame-Sync Pulse*.

- Receiver underflow (the MCBSPi.MCBSPLP_IRQSTATUS_REG[4] RUNDFLSTAT bit is set to 1)

  This occurs when the sDMA controller or MPU/DSP subsystem reads data from an empty receive buffer. For more information about underflow in the receiver, see Section 23.5.4.10.4, *Underflow in the Receiver*.

- Transmitter underflow (the MCBSPi.MCBSPLP_IRQSTATUS_REG[11] XUNDFLSTAT bit is set to 1, and the legacy mode MCBSPi.MCBSPLP_SPCR2_REG[2] XEMPTY bit is set to 0)

  If a new frame-sync signal arrives when the XB is empty, the previous data in the XSR is re-sent. This procedure continues for every new frame-sync pulse that arrives until the MCBSPi.MCBSPLP_DXR_REG register is loaded with new data (and the XB is no longer empty). For more information about underflow in the transmitter, see Section 23.5.4.10.5, *Underflow in the Transmitter*.

- Unexpected transmit frame-sync pulse (the MCBSPi.MCBSPLP_IRQSTATUS_REG[7] XSYNCERR bit is set to 1, and the legacy mode MCBSPi.MCBSPLP_SPCR2_REG[3] XSYNCERRbit is set to 1)

  This occurs during transmission when an unexpected frame-sync pulse arrives. An unexpected frame-sync pulse is one that is supposed to begin the next frame transfer before all the bits of the current frame are transferred. Such a pulse is ignored by the transmitter, but sets the MCBSPi.MCBSPLP_SPCR2_REG[3] XSYNCERR bit. For more information, see Section 23.5.4.10.6, *Unexpected Transmit Frame-Sync Pulse*.

- Transmitter overflow (the MCBSPi.MCBSPLP_IRQSTATUS_REG[12] XOVFLSTAT bit is set to 1)

  This occurs when the sDMA controller or MPU/DSP subsystem writes data to a full XB. For more information about underflow in the receiver, see Section 23.5.4.10.7, *Overflow in the Transmitter*.

23.5.4.10.2 Overrun in the Receiver

When the MCBSPi.MCBSPLP_IRQSTATUS_REG[5] ROVFLSTAT bit is set to 1, and the MCBSPi.MCBSPLP_SPCR1_REG[2] RFULL bit is set to 1 (legacy mode) indicates that the receiver has experienced overrun and is in an error condition. Receive overrun is set when all of the following conditions are met:

1. MCBSPi.MCBSPLP_DRR_REG is not read even if the MCBSPi.MCBSPLP_IRQSTATUS_REG[3] RRDY bit is set (legacy mode) and DMA or interrupt request has been asserted.
2. RB is full.
3. RSR is full.

As previously described, data arriving on MCBSPi_dr is continuously shifted into the RSR. Once a complete word is shifted into the RSR, an RSR-to-RB copy can occur only if the RB is not full.

Either of the following events clears the legacy mode MCBSPi.MCBSPLP_SPCR1_REG[2] RFULL bit and allows subsequent transfers to be read properly:

- The MPU/DSP subsystems or sDMA controller reads the MCBSPi.MCBSPLP_DRR_REG register.
- The receiver is reset individually (the MCBSPi.MCBSPLP_SPCR1_REG[0] RRST bit is set to 0) or as part of a global reset.

Another frame-sync pulse is required to restart the receiver.

According to the MCBSPi.MCBSPLP_IRQENABLE_REG register setting, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in the MCBSPi.MCBSPLP_IRQSTATUS_REG register clears the interrupt.

Figure 23-129 shows the receive overrun condition.

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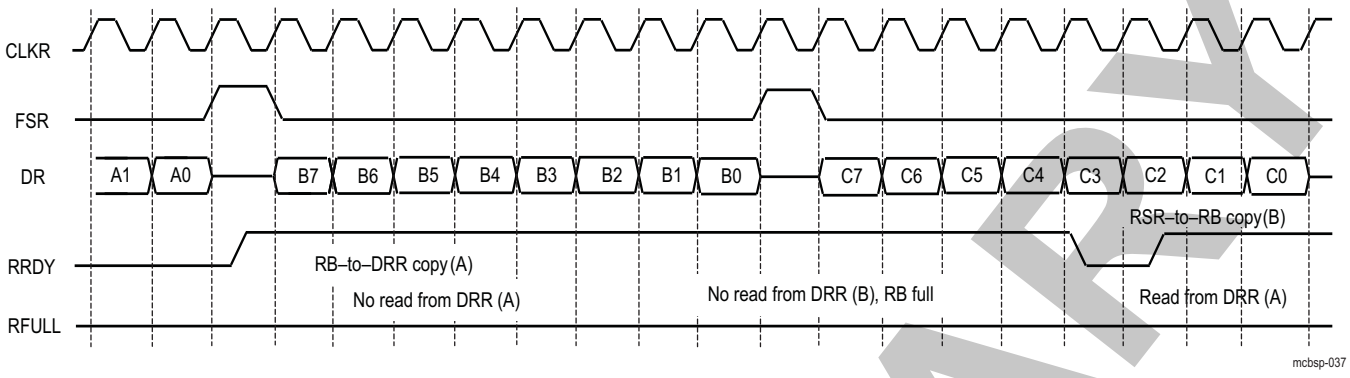
Figure 23-129. Overrun in the MCBSP Receiver



23.5.4.10.3 Unexpected Receive Frame-Sync Pulse

23.5.4.10.3.1 Possible Responses to Receive Frame-Sync Pulses

If a frame-sync pulse starts the transfer of a new frame before the current frame is fully received, this pulse is treated as an unexpected frame-sync pulse, and the receiver sets the receive frame-sync error bit MCBSPi.MCBSPLP_IRQSTATUS_REG[0] RSYNCERR (and the legacy MCBSPi.MCBSPLP_SPCR1_REG[3] RSYNCERR bit).

According to the settings of the MCBSPi.MCBSPLP_IRQENABLE_REG register, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in the MCBSPi.MCBSPLP_IRQSTATUS_REG register clears the interrupt.

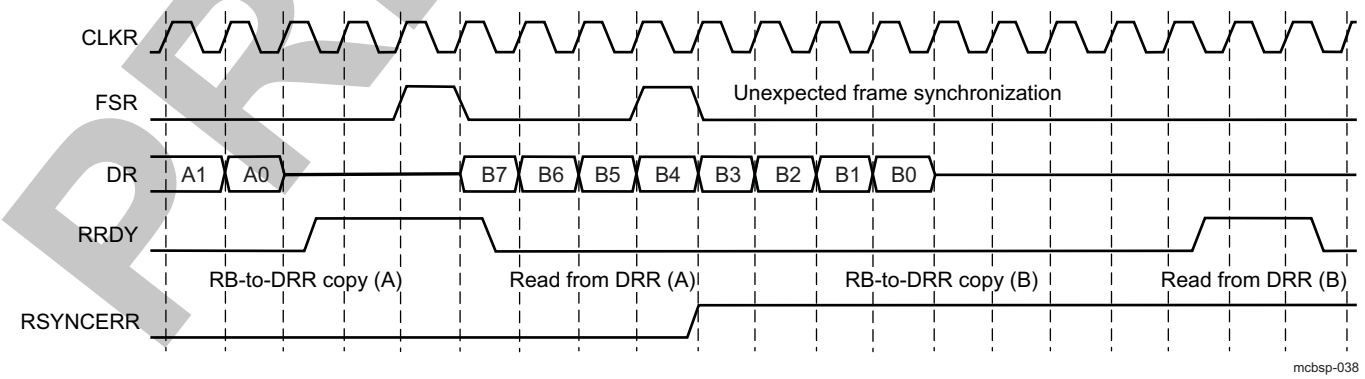
Using the legacy mode, the MCBSPi.MCBSPLP_SPCR1_REG[3] RSYNCERR bit can be cleared only by a receiver reset or by setting this bit to 0. For the MCBSP module to notify the MPU/DSP subsystem of receive frame-sync errors, set the legacy mode receive interrupt with the MCBSPi.MCBSPLP_SPCR1_REG[5:4] RINTM bit field. When RINTM is set to 0b11, the MCBSP module sends a receive interrupt (legacy mode) request to the MPU/DSP subsystems each time that RSYNCERR is set.

23.5.4.10.3.2 Example of an Unexpected Receive Frame-Sync Pulse

Figure 23-130 shows an unexpected receive frame-sync pulse during normal operation of the serial port with time intervals between data packets.

NOTE: The unexpected receive frame-sync pulse does not influence the data receive process, being ignored by the data receive state-machine.

Figure 23-130. Unexpected Frame-Sync Pulse During a MCBSP Reception



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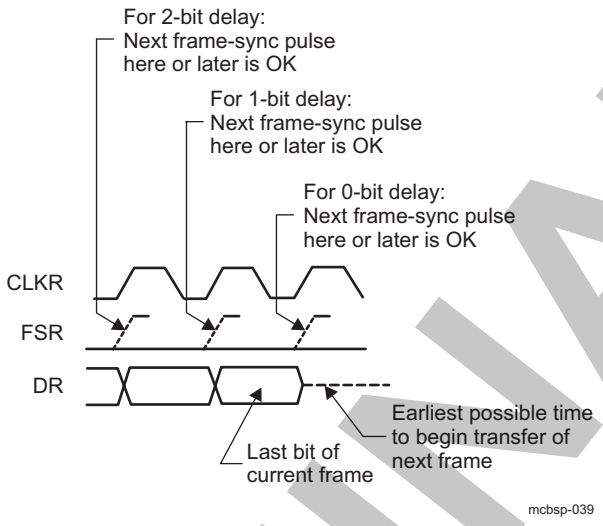
23.5.4.10.3.3 Preventing Unexpected Receive Frame-Sync Pulses

Each frame transfer can be delayed by 0, 1, or 2 CLKR cycles, depending on the value of the MCBSPi.MCBSPLP_RCR2_REG[1:0] RDATDLY bit field. For each possible data delay, Figure 23-131 shows when a new frame-sync pulse on FSR can safely occur relative to the last bit of the current frame.

Figure 23-131. Proper Positioning of Receive Frame-Sync Pulses



23.5.4.10.4 Underflow in the Receiver

The MCBSP module indicates a receiver underflow condition by setting the MCBSPi.MCBSPLP_IRQSTATUS_REG[4] RUNDFLSTAT bit. This error occurs when sDMA controller or MPU/DSP subsystem reads data from an empty RB this happens only if the MPU/DSP subsystem or sDMA controller does not respect the DMA length, does not wait for DMA request, or does not check the buffer status before reading data. According to the MCBSPi.MCBSPLP_IRQENABLE_REG register settings this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in MCBSPi.MCBSPLP_IRQSTATUS_REG register clears the interrupt.

23.5.4.10.5 Underflow in the Transmitter

The MCBSP module indicates a transmitter empty (or underflow) condition by setting the MCBSPi.MCBSPLP_IRQSTATUS_REG[11] XUNDFLSTAT bit. The legacy mode MCBSPi.MCBSPLP_SPCR2_REG[2] XEMPTY bit is also cleared. Either of the following events activates the XEMPTY bit (XEMPTY = 0):

- The MCBSPi.MCBSPLP_DXR_REG register has not been loaded and the XB is empty, and all bits of the data word in the XSR have been shifted out on the MCBSPi_dx pin.
- The transmitter is reset (by forcing MCBSPi.MCBSPLP_SPCR2_REG[0] XRST to 0, or by a global reset) and is then restarted.

The XEMPTY bit is deactivated (XEMPTY = 1) when a new word in the MCBSPi.MCBSPLP_DXR_REG register is transferred to the XB. If the MCBSPi.MCBSPLP_PCR_REG[11] FSXM bit is set to 1 and the MCBSPi.MCBSPLP_SRGR2_REG[12] FSGM bit is set to 0, the FSX signal is generated when the XB is not empty. When the MCBSPi.MCBSPLP_SRGR2_REG[12] FSGM bit is set to 0, the MCBSPi.MCBSPLP_SRGR2_REG[11:0] FPER and MCBSPi.MCBSPLP_SRGR1_REG[15:8] FWID bit fields are used to determine the frame-sync period and width (external FSX is gated by the buffer empty condition). Otherwise, the transmitter waits for the next frame-sync pulse before sending the next frame on the MCBSPi_dx pin.

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When the transmitter is taken out of reset (the cBSPi.MCBSPLP_SPCR2_REG[0] XRST bit is set to 1), it is in a transmitter ready state (the MCBSPi.MCBSPLP_SPCR2_REG[1] XRDY bit is set to 1) and transmitter empty (the MCBSPi.MCBSPLP_SPCR2_REG[2] XEMPTY bit is set to 0) state. If the MCBSPi.MCBSPLP_DXR_REG register is loaded by the MPU/DSP subsystem or the sDMA controller before internal the FSX goes active high, a valid XB-to-XSR transfer occurs. This allows for the first word of the first frame to be valid even before the transmit frame-sync pulse is generated or detected. Alternatively, if a transmit frame-sync pulse is detected before MCBSPi.MCBSPLP_DXR_REG is loaded, zeros are output on the MCBSPi_dx pin.

The MCBSPi.MCBSPLP_IRQSTATUS_REG[11] XUNDFLSTAT bit indicates a real underflow condition, in which the frame is corrupted due to lack of data availability during the transmit process. According to the settings of the MCBSPi.MCBSPLP_IRQENABLE_REG register, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in MCBSPi.MCBSPLP_IRQSTATUS_REG register clears the interrupt.

23.5.4.10.6 Unexpected Transmit Frame-Sync Pulse

23.5.4.10.6.1 Possible Responses to Transmit Frame-Sync Pulses

If a frame-sync pulse starts the transfer of a new frame before the current frame is fully transmitted, this pulse is treated as an unexpected frame-sync pulse, and the transmitter sets the transmit frame-sync error bit MCBSPi.MCBSPLP_IRQSTATUS_REG[7] XSYNCERR (and the legacy MCBSPi.MCBSPLP_SPCR2_REG[3] XSYNCERR bit).

According to the settings of the MCBSPi.MCBSPLP_IRQENABLE_REG register, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in the status register clears the interrupt.

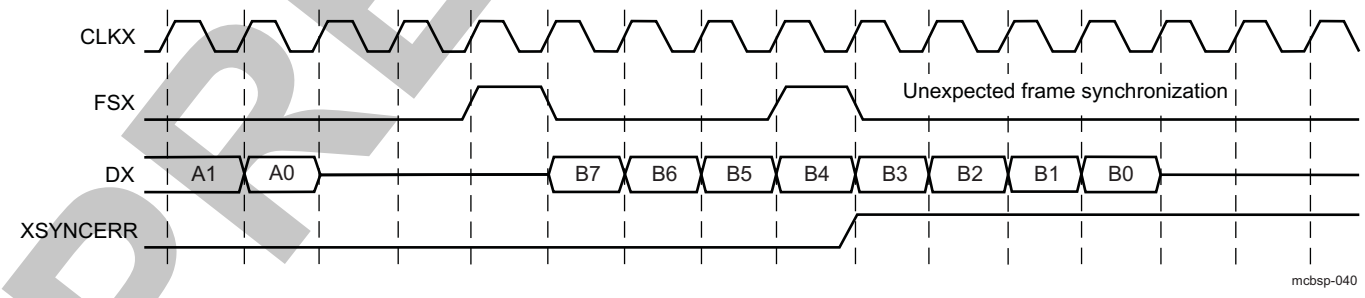
Using the legacy mode, the MCBSPi.MCBSPLP_SPCR2_REG[3] XSYNCERR bit can be cleared only by a transmitter reset or by setting this bit to 0. For the MCBSP module to notify the MPU/DSP subsystem of frame-sync errors, set a special transmit interrupt mode with the MCBSPi.MCBSPLP_SPCR2_REG[5:4] XINTM bit field. When XINTM is set to 0b11, the MCBSP module sends a transmit interrupt request to the MPU/DSP subsystem each time XSYNCERR is set.

23.5.4.10.6.2 Example of Unexpected Transmit Frame-Sync Pulse

Figure 23-132 shows an unexpected transmit frame-sync pulse during normal operation of the serial port with intervals between the data packets.

NOTE: The unexpected transmit frame-sync pulse does not influence the data transmit process, being ignored by the data transmit state-machine.

Figure 23-132. Unexpected Frame-Sync Pulse During a MCBSP Transmission



23.5.4.10.6.3 Preventing Unexpected Transmit Frame-Sync Pulses

Each frame transfer can be delayed by 0, 1, or 2 CLKX cycles, depending on the value in the MCBSPi.MCBSPLP_XCR2_REG[1:0] XDATDLY bit field. For each possible data delay, Figure 23-133 shows when a new frame-sync pulse on FSX can safely occur relative to the last bit of the current frame.

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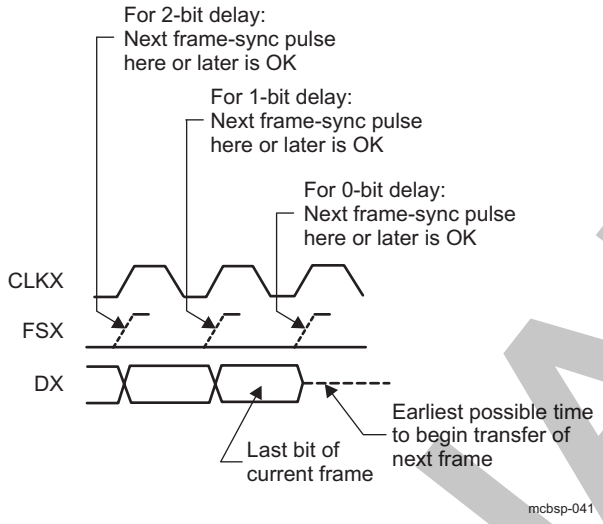
Figure 23-133. Proper Positioning of Transmit Frame-Sync Pulses



23.5.4.10.7 Overflow in the Transmitter

The MCBSP module indicates a transmitter overflow condition by setting the MCBSPi.MCBSPLP_IRQSTATUS_REG[12] XOVFLSTAT bit. This error occurs when the sDMA controller or MPU/DSP subsystem writes data to a full XB (this happens only if the MPU/DSP subsystem or sDMA controller does not respect the DMA length, does not wait for DMA request, or does not check the buffer status before writing data). According to the settings of the MCBSPi.MCBSPLP_IRQENABLE_REG register, this condition can generate the MCBSPi_IRQ line to be asserted low. Writing 1 to the corresponding bit in the status register clears the interrupt.

23.5.4.11 MCBSP DMA Configuration

The MCBSP receive and transmit data DMA requests are active after the receive MCBSPi.MCBSPLP_SPCR1_REG[0] RRST and transmit MCBSPi.MCBSPLP_SPCR2_REG[0] XRST bits are released. After reset the default DMA threshold (and length) is one.

The receive and transmit DMA requests can be individually disabled by setting the MCBSPi.MCBSPLP_RCCR_REG[3] RDMAEN and MCBSPi.MCBSPLP_XCCR_REG[3] XDMAEN bits to 0. When disabling the DMA, the DMA request line is deasserted even if a DMA transfer is pending and the DMA state-machine is not reset.

The DMA threshold and length configuration is done through the MCBSPi.MCBSPLP_THRSH1_REG and MCBSPi.MCBSPLP_THRSH2_REG registers as follows:

- (THRSH1_REG + 1) value represents the required receive DMA request length (the length of the transfer is the same as the threshold value plus 1). As long as the RB occupied locations level is greater than or equal to the THRSH1_REG value + 1, the DMA request is asserted. After transferring the configured (THRSH1_REG + 1) number of words, the receive DMA request is de-asserted and reasserted as soon as the conditions are met again.
- (THRSH2_REG + 1) value represents the required transmit DMA request length (the length of the transfer is the same as the threshold value plus 1). As long as the XB free locations level is greater than or equal to the THRSH2_REG value + 1, the DMA request is asserted. After transferring the configured (THRSH2_REG + 1) number of words, the transmit DMA request is deasserted and reasserted as soon as the conditions are met.

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NOTE: The MPU/DSP subsystem can decide not to use the DMA to transfer the data. In this case, the DMA must be disabled (or the DMA request can be ignored by MPU/DSP subsystem) and the common interrupt line (MCBSPi_IRQ) can be used. The MCBSPi.MCBSPLP_SPCR1_REG[1] RRDY bit for receive and the MCBSPi.MCBSPLP_SPCR2_REG[1] XRDY bit for transmit indicate when the threshold values are reached. Also, by reading the receive buffer status MCBSPi.MCBSPLP_RBUFFSTAT_REG register and transmit buffer status MCBSPi.MCBSPLP_XBUFFSTAT_REG register, the MPU/DSP subsystem can decide to transfer data even if the threshold is not reached. This mechanism is useful on the last transfer on the receive side when the threshold value is bigger than the occupied locations inside the receive buffer and the MPU/DSP subsystem needs to read this data. Because no interrupt or DMA request is asserted, the only option in this case is to read the value of the RB status register and to transfer the remaining data without using the DMA or interrupt indication.

23.5.4.12 Multichannel Selection Modes

23.5.4.12.1 Channels, Blocks and Partitions

A MCBSP channel is a time slot for shifting in/out the bits of one serial word. The MCBSP module supports up to 128 channels for reception and 128 channels for transmission. In the receiver and in the transmitter, the 128 available channels are divided into eight blocks that contain 16 contiguous channels each (see Table 23-339).

Table 23-339. MCBSP Channels

Block 0: Channels 0–15	**Block 4: Channels 64–79**
Block 1: Channels 16–31	**Block 5: Channels 80–95**
Block 2: Channels 32–47	**Block 6: Channels 96–111**
Block 3: Channels 48–63	**Block 6: Channels 112–127**

The blocks are assigned to partitions according to the selected partition mode. In the 2-partition mode described in Section 23.5.4.12.6, *Using Two Partitions (Legacy Only)*, assign one even-numbered block (0, 2, 4, or 6) to partition A and one odd-numbered block (1, 3, 5, or 7) block to partition B. In the 8-partition mode described in Section 23.5.4.12.4, *Using Eight Partitions*, blocks 0 through 7 are automatically assigned to partitions A through H, respectively.

The number of partitions for reception and the number of partitions for transmission are independent of one another. For example, it is possible to use two receive partitions (A and B) and eight transmit partitions (A–H).

23.5.4.12.2 Multichannel Selection

When a MCBSP module uses a time-division multiplexed (TDM) data stream while communicating with other MCBSP modules or serial devices, the MCBSP module may need to receive and/or transmit on only a few channels. To save memory and bus bandwidth, use a multichannel selection mode to prevent data flow in some of the channels.

Each channel partition has a dedicated channel enable register. If the appropriate multichannel selection mode is on, each bit in the register controls whether data flow is allowed or prevented in one of the channels that is assigned to that partition.

The MCBSP module has one receive multichannel selection mode (see Section 23.5.4.12.5, *Receive Multichannel Selection Mode*) and three transmit multichannel selection modes (see Section 23.5.4.12.7, *Transmit Multichannel Selection Modes*).

23.5.4.12.3 Configuring a Frame for Multichannel Selection

Before enabling a multichannel selection mode, ensure that the data frame is properly configured:

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- Select a single-phase frame (the MCBSPi.MCBSPLP_RCR2_REG[15] RPHASE and MCBSPi.MCBSPLP_XCR2_REG[15] XPHASE bits are set to 0). Each frame represents a TDM data stream.
- Set a frame length (in the MCBSPi.MCBSPLP_RCR1_REG[14:8] RFRLEN1 and MCBSPi.MCBSPLP_XCR1_REG[14:8] XFRLEN1 bit fields) that includes the highest numbered channel to be used. For example, to use channels 0, 15, and 39 for reception, the receive frame length must be at least 40 (RFRLEN1 = 39). In this case, If XFRLEN1= 39, the receiver creates 40 time slots per frame but receives data only during time slots 0, 15, and 39 of each frame.

23.5.4.12.4 Using Eight Partitions

For multichannel selection operation in the receiver and/or transmitter, eight partitions or two partitions (as previously described) can be used. If 8-partition mode (MCBSPi.MCBSPLP_MCR1_REG[9] RMCME = 1 for reception, and MCBSPi.MCBSPLP_MCR2_REG[9] XMCME = 1 for transmission) is selected, MCBSP channels are activated in the following order: A, B, C, D, E, F, G, H.

In response to a frame-sync pulse, the receiver or transmitter begins with the channels in partition A and then continues with the other partitions, in order, until the complete frame is transferred. When the next frame-sync pulse occurs, the next frame is transferred, beginning with the channels in partition A.

In 8-partition mode, the MCBSPi.MCBSPLP_MCR1_REG[6:5] RPABLK/MCBSPi.MCBSPLP_MCR2_REG[6:5] XPABLK bit fields, and the MCBSPi.MCBSPLP_MCR1_REG[8:7] RPBBLK/MCBSPi.MCBSPLP_MCR2_REG[8:7] XPBBLK bit fields are ignored and the 16-channel blocks are assigned to the partitions as shown in Table 23-340 and Table 23-341. These assignments cannot be changed. The tables also show the registers used to control the channels in the partitions.

Table 23-340. Eight Partitions – Receive Channel Assignment and Control

Receive Partition	Assigned Block of Receive Channels	Register Used for Channel Control
A	Block 0: Channels 0–15	MCBSPi.MCBSPLP_RCERA_REG
B	Block 1: Channels 16–31	MCBSPi.MCBSPLP_RCERB_REG
C	Block 2: Channels 32–47	MCBSPi.MCBSPLP_RCERC_REG
D	Block 3: Channels 48–63	MCBSPi.MCBSPLP_RCERD_REG
E	Block 4: Channels 64–79	MCBSPi.MCBSPLP_RCERE_REG
F	Block 5: Channels 80–95	MCBSPi.MCBSPLP_RCERF_REG
G	Block 6: Channels 96–111	MCBSPi.MCBSPLP_RCERG_REG
H	Block 7: Channels 112–127	MCBSPi.MCBSPLP_RCERH_REG

Table 23-341. Eight Partitions – Transmit Channel Assignment and Control

Transmit Partition	Assigned Block of Receive Channels	Register Used for Channel Control
A	Block 0: Channels 0–15	MCBSPi.MCBSPLP_XCERA_REG
B	Block 1: Channels 16–31	MCBSPi.MCBSPLP_XCERB_REG
C	Block 2: Channels 32–47	MCBSPi.MCBSPLP_XCERC_REG
D	Block 3: Channels 48–63	MCBSPi.MCBSPLP_XCERD_REG
E	Block 4: Channels 64–79	MCBSPi.MCBSPLP_XCERE_REG
F	Block 5: Channels 80–95	MCBSPi.MCBSPLP_XCERF_REG
G	Block 6: Channels 96–111	MCBSPi.MCBSPLP_XCERG_REG
H	Block 7: Channels 112–127	MCBSPi.MCBSPLP_XCERH_REG

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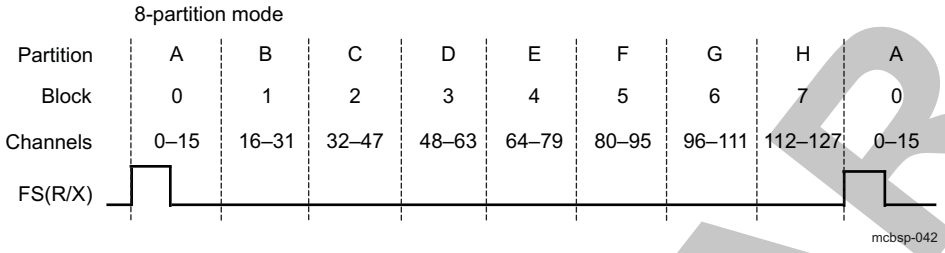
Figure 23-134 shows an example of the MCBSP using 8-partition mode. In response to a frame-sync pulse, the MCBSP module begins a frame transfer with partition A and then activates B, C, D, E, F, G, and H to complete a 128-word frame.

Figure 23-134. MCBSP Data Transfer in 8-Partition Mode



23.5.4.12.5 Receive Multichannel Selection Mode

The MCBSPi.MCBSPLP_MCR1_REG[0] RMCM bit determines whether all channels or only selected channels are enabled for reception.

- When RMCM = 0, all 128 receive channels are enabled and cannot be disabled.
- When RMCM = 1, the receive multichannel selection mode is enabled. In this mode:
  - Channels can be individually enabled or disabled. The enabled channels are those selected in the appropriate receive channel enable registers (MCBSPi.MCBSPLP_RCERA_REG/MCBSPi.MCBSPLP_RCERH_REG). The channels assigned to the MCBSPi.MCBSPLP_RCERA_REG/MCBSPi.MCBSPLP_RCERH_REG registers depend on the number of receive channel partitions (2 or 8), as defined by the MCBSPi.MCBSPLP_MCR1_REG[9] RMCME bit.
  - If a receive channel is disabled, any bits received in that channel are not transferred to the RB, and as a result, the receiver ready bit (RRDY) is not set. Therefore, no DMA synchronization event is generated and, if the receiver interrupt mode depends on RRDY (MCBSPi.MCBSPLP_SPCR1_REG[5:4] RINTM = 0b00), no interrupt is generated.

As an example of how the MCBSP module behaves in the receive multichannel selection mode, suppose only channels 0, 15, and 39 are enabled and that the frame length is 40. The MCBSP module:

1. Accepts bits shifted in from the MCBSPi_dr pin in channel 0
2. Ignores bits received in channels 1–14
3. Accepts bits shifted in from the MCBSPi_dr pin in channel 15
4. Ignores bits received in channels 16–38
5. Accepts bits shifted in from the MCBSPi_dr pin in channel 39

23.5.4.12.6 Using Two Partitions (Legacy Only)

For multichannel selection operation in the receiver and/or the transmitter, two partitions or eight partitions can be used. If 2-partition mode (the MCBSPi.MCBSPLP_MCR1_REG[9] RMCME bit is set to 0 for reception, and the MCBSPi.MCBSPLP_MCR2_REG[9] XMCME bit is set to 0 for transmission) is selected, the MCBSP channels are activated using an alternating scheme. In response to a frame-sync pulse, the receiver or transmitter begins with the channels in partition A and then alternates between partitions B and A until the complete frame is transferred. When the next frame-sync pulse occurs, the next frame is transferred beginning with the channels in partition A.

For reception, any two of the eight receive-channel blocks can be assigned to receive partitions A and B, which means up to 32 receive channels can be enabled at any given point. Similarly, any two of the eight transmit-channel blocks (up to 32 enabled transmit channels) can be assigned to transmit partitions A and B.

For reception:

- Assign an even-numbered channel block (0, 2, 4, or 6) to receive partition A by writing to the MCBSPi.MCBSPLP_MCR1_REG[6:5] RPABLK bit field. In the receive multichannel selection mode,

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the channels in this partition are controlled by receive channel enable register A (MCBSPi.MCBSPLP_RCERA_REG).

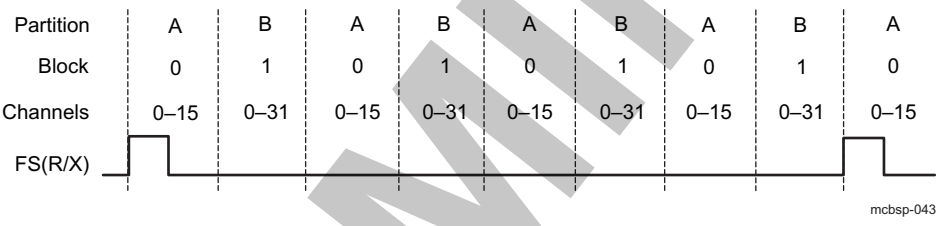
- Assign an odd-numbered block (1, 3, 5, or 7) to receive partition B with the MCBSPi.MCBSPLP_MCR1_REG[8:7] RPBBLK bit field. In the receive multichannel selection mode, the channels in this partition are controlled by receive channel enable register B (MCBSPi.MCBSPLP_RCERB_REG).

For transmission:

- Assign an even-numbered channel block (0, 2, 4, or 6) to transmit partition A by writing to the MCBSPi.MCBSPLP_MCR2_REG[6:5] XPABLK bit field. In one of the transmit multichannel selection modes, the channels in this partition are controlled by transmit channel enable register A (MCBSPi.MCBSPLP_XCERA_REG).
- Assign an odd-numbered block (1, 3, 5, or 7) to transmit partition B with the MCBSPi.MCBSPLP_MCR1_REG[8:7] XPBBLK bit field. In one of the transmit multichannel selection modes, the channels in this partition are controlled by transmit channel enable register B (MCBSPi.MCBSPLP_XCERB_REG).

Figure 23-135 shows an example of alternating between the channels of partition A and the channels of partition B. Channels 0–15 have been assigned to partition A, and channels 16–31 have been assigned to partition B. In response to a frame-sync pulse, the MCBSP module begins a frame transfer with partition A and then alternates between partitions B and A until the complete frame is transferred.

Figure 23-135. Alternating Between Partitions A and B Channels



23.5.4.12.7 Transmit Multichannel Selection Modes

The MCBSPi.MCBSPLP_MCR2_REG[1:0] XMCM bit field determines whether all channels or only selected channels are enabled and unmasked for transmission. The MCBSP module has three transmit multichannel selection modes (XMCM = 0b01, XMCM = 0b10, and XMCM = 0b11), which are described in Table 23-342.

Table 23-342. Selecting a Transmit Multichannel Selection Mode With the XMCM Bit Field

XMCM	Transmit Multichannel Selection Mode
0b00	No transmit multichannel selection mode is on. All channels are enabled and unmasked. No channels can be disabled or masked.
0b01	All channels are disabled unless they are selected in the appropriate transmit channel enable registers (MCBSPi.MCBSPLP_XCERA_REG/MCBSPi.MCBSPLP_XCERH_REG). If enabled, a channel in this mode is also unmasked. The MCBSPi.MCBSPLP_MCR2_REG[9] XMCME bit determines whether 32 or 128 channels are selectable in the MCBSPi.MCBSPLP_XCERA_REG/MCBSPi.MCBSPLP_XCERH_REG registers.
0b10	All channels are enabled, but they are masked unless they are selected in the appropriate transmit channel enable registers (MCBSPi.MCBSPLP_XCERA_REG/MCBSPi.MCBSPLP_XCERH_REG). The MCBSPi.MCBSPLP_MCR2_REG[9] XMCME bit determines whether 32 or 128 channels are selectable in the MCBSPi.MCBSPLP_XCERA_REG/MCBSPi.MCBSPLP_XCERH_REG registers.
0b11	This mode is used for symmetric transmission and reception. All channels are disabled for transmission unless they are enabled for reception in the appropriate receive channel enable registers (MCBSPi.MCBSPLP_RCERA_REG/MCBSPi.MCBSPLP_RCERH_REG). Once enabled, they are masked unless they are also selected in the appropriate transmit channel enable registers (MCBSPi.MCBSPLP_XCERA_REG/MCBSPi.MCBSPLP_XCERH_REG). The MCBSPi.MCBSPLP_MCR2_REG[9] XMCME bit determines whether 32 or 128 channels are selectable in the MCBSPi.MCBSPLP_RCERA_REG/MCBSPi.MCBSPLP_RCERH_REG registers and the MCBSPi.MCBSPLP_XCERA_REG/MCBSPi.MCBSPLP_XCERH_REG registers.

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As an example of how the MCBSP module behaves in a transmit multichannel selection mode, suppose that XMCM = 0b01 (all channels disabled unless individually enabled) and that only channels 0, 15, and 39 are enabled. Suppose also that the frame length is 40. The MCBSP module:

1. Shifts data to the MCBSPi_dx pin in channel 0
2. Places the MCBSPi_dx pin in the high-impedance state in channels 1–14
3. Shifts data to the MCBSPi_dx pin in channel 15
4. Places the MCBSPi_dx pin in the high-impedance state in channels 16–38
5. Shifts data to the MCBSPi_dx pin in channel 39

23.5.4.12.7.1 Disabling/Enabling Versus Masking/Unmasking

For transmission, a channel can be:

- Enabled and unmasked (transmission can begin and can be completed)
- Enabled but masked (transmission can begin but cannot be completed)
- Disabled (transmission cannot occur)

The definitions in Table 23-343 explain the channel control options:

Table 23-343. MCBSP Channel Control Options

Enabled channel	A channel that can begin transmission by passing data from the data transmit register (MCBSPi.MCBSPLP_DXR_REG) to the XSR through the XB.
Masked channel	A channel that cannot complete transmission. The MCBSPi_dx pin is held in high-impedance state; data cannot be shifted out on the MCBSPi_dx pin. In systems where symmetric transmit and receive provide software benefits, this feature allows transmit channels to be disabled on a shared serial bus. A similar feature is not needed for reception because multiple receptions cannot cause serial bus contention.
Disabled channel	A channel that is not enabled. A disabled channel is also masked. Because no DXR-to-XB copy occurs, the MCBSPi.MCBSPLP_SPCR2_REG[1] XRDY bit is not set. Therefore, no DMA synchronization event is generated, and if the transmit interrupt mode depends on XRDY (MCBSPi.MCBSPLP_SPCR2_REG[5:4] XINTM = 00b), no interrupt is generated. The MCBSPi.MCBSPLP_SPCR2_REG[2] XEMPTY bit is not affected.
Unmasked channel	A channel that is not masked. Data in the XSR(s) is shifted out on the MCBSPi_dx pin.

23.5.4.12.7.2 Activity on MCBSP Pins for Different Values of XMCM

Figure 23-136 shows the activity on the MCBSP pins for the various values of the MCBSPi.MCBSPLP_MCR2_REG[1:0] XMCM bit field. In all cases, the transmit frame is configured as follows:

- XPHASE = 0: Single-phase frame (required for multichannel selection modes)
- XFRLEN1 = 0b0000011: 4 words per frame
- XWDLEN1 = 0b000: 8 bits per word
- XMCME = 0: 2-partition mode (only partitions A and B are used)

In the case where MCBSPi.MCBSPLP_MCR2_REG[1:0] XMCM = 0b11, transmission and reception are symmetric, which means the corresponding bits for the receiver (RPHASE, RFRLEN1, RWDLEN1, and RMCME) must have the same values as XPHASE, XFRLEN1, and XWDLEN1, respectively.

In Figure 23-136, the arrows showing where the various events occur are only sample indications. Wherever possible, there is a time window in which these events can occur.

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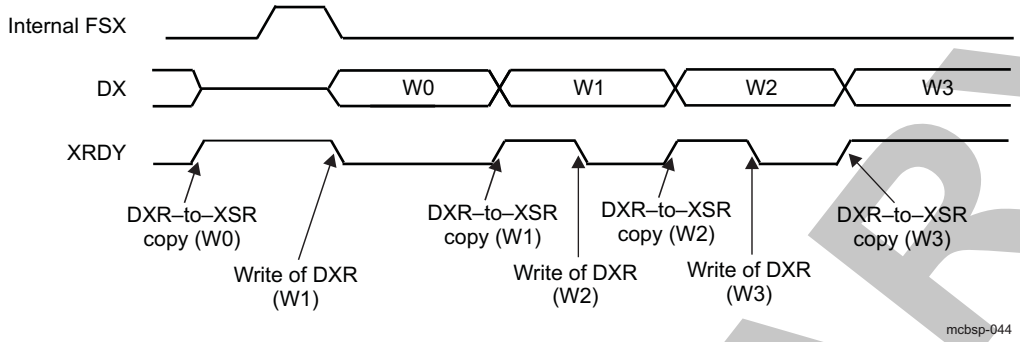
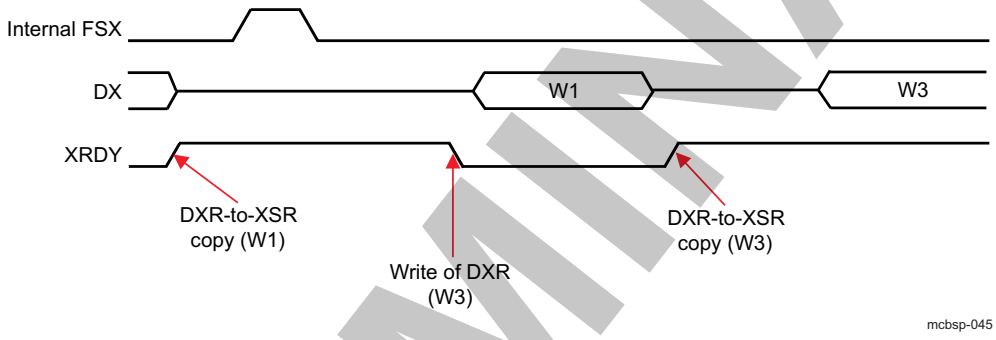
Figure 23-136. Activity on MCBSP Pins When XMCM = 0b00



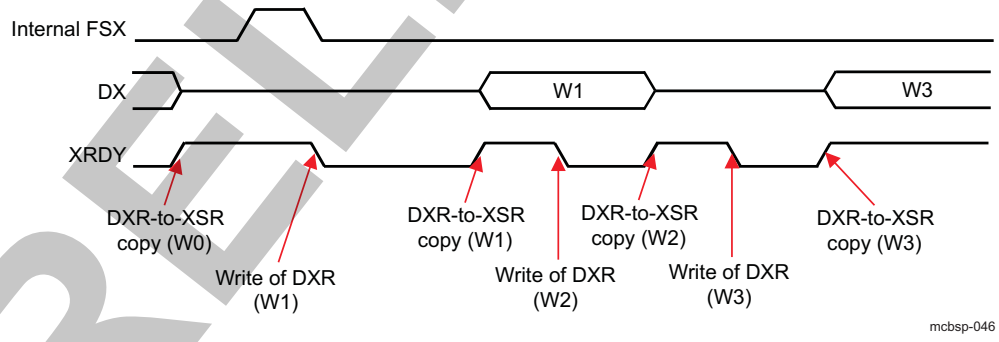
If XMCM = 0b00, all channels are enabled and unmasked. Words W0, W1, W2, and W3 are written to the XB, and then, from the XB, they are transferred by MCBSPi_dx.

Figure 23-137. Activity on MCBSP Pins When XMCM = 0b01



In Figure 23-137 if XMCM = 0b01, XPABLK = 0b00, and XCERA = 0b1010, only channels 1 and 3 are enabled and unmasked. Words W1 and W3 are written to the XB, and then, from the XB, they are transferred by MCBSPi_dx.

Figure 23-138. Activity on MCBSP Pins When XMCM = 0b10



In Figure 23-138 if XMCM = 0b10, XPABLK = 0b00, and XCERA = 0b1010, all channels are enabled, and only 1 and 3 are unmasked. Words W0, W1, W2, and W3 are written to the XB, but only W1 and W3, from the XB, are transferred by MCBSPi_dx.

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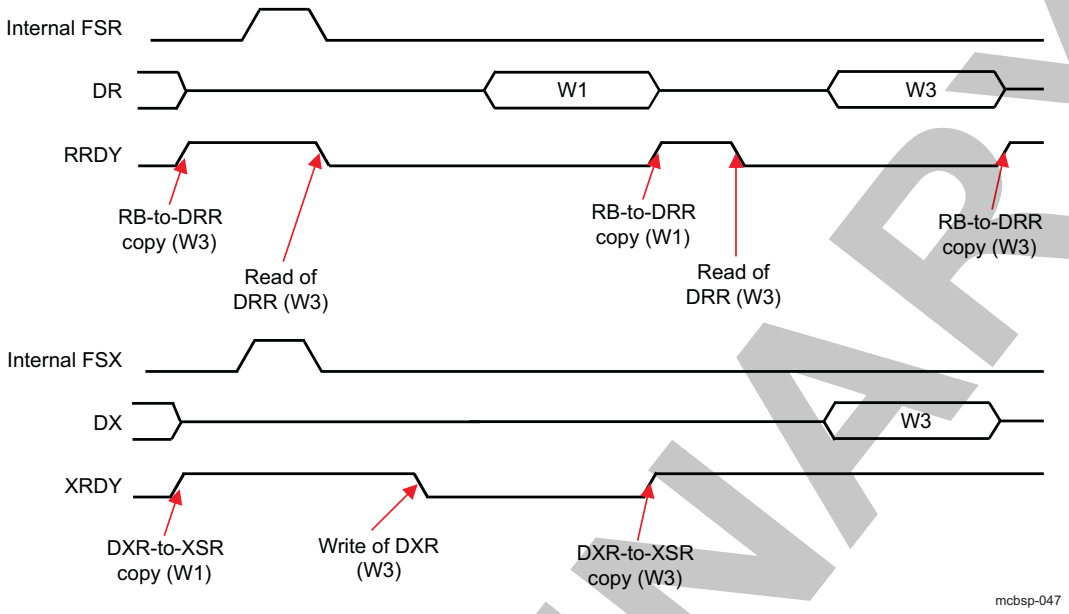
Figure 23-139. Activity on MCBSP Pins When XMCM = 0b11



In Figure 23-139 if XMCM = 0b11, RPABLK = 0b00, XPABLK = 0bX, RCERA = 0b1010, and XCERA = 0b1000, channels 1 and 3 are enabled in receive and transmit mode, but only 3 is unmasked. Words W1 and W3 are written to the XB, but only W3, from the XB, is transferred by MCBSPi_dx.

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23.5.5 MCBSP Basic Programming Model

This section describes the programming model of a typical MCBSP module.

CAUTION

For all descriptions in this section, the MCBSPi.MCBSPLP_XCCR_REG[11] XFULL_CYCLE and MCBSPi.MCBSPLP_RCCR_REG[11] RFULL_CYCLE bits are their reset value (XFULL_CYCLE is set to 0 and RFULL_CYCLE is set to 1).

23.5.5.1 MCBSP Initialization Procedure

This procedure for reset/initialization can be applied in general when the receiver or transmitter must be reset during its normal operation, and also when the SRG is not used for either operation.

Figure 23-140 shows the serial port initialization procedure for master mode.

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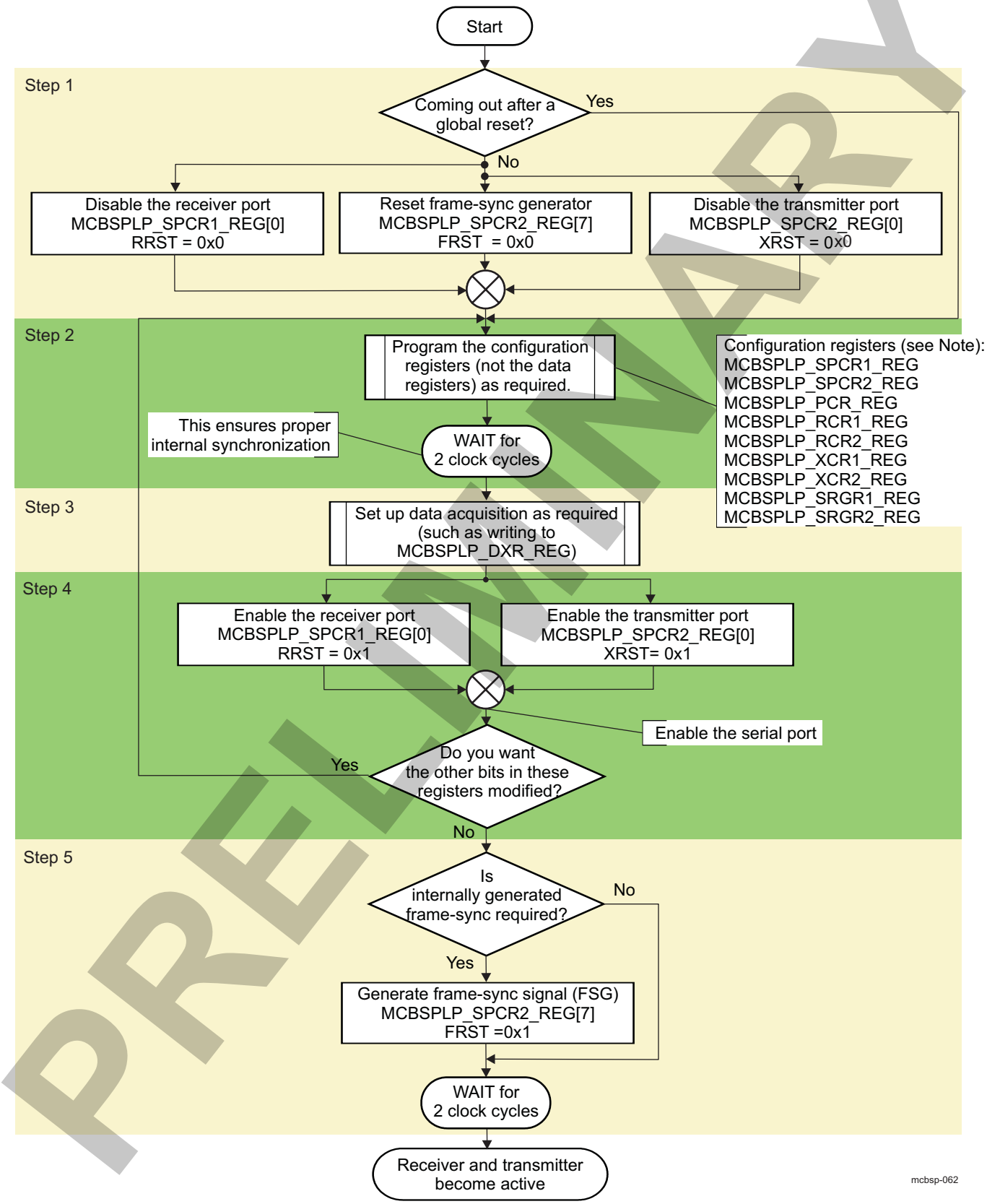
Figure 23-140. Flow Diagram of MCBSP Initialization Procedure for Master Mode



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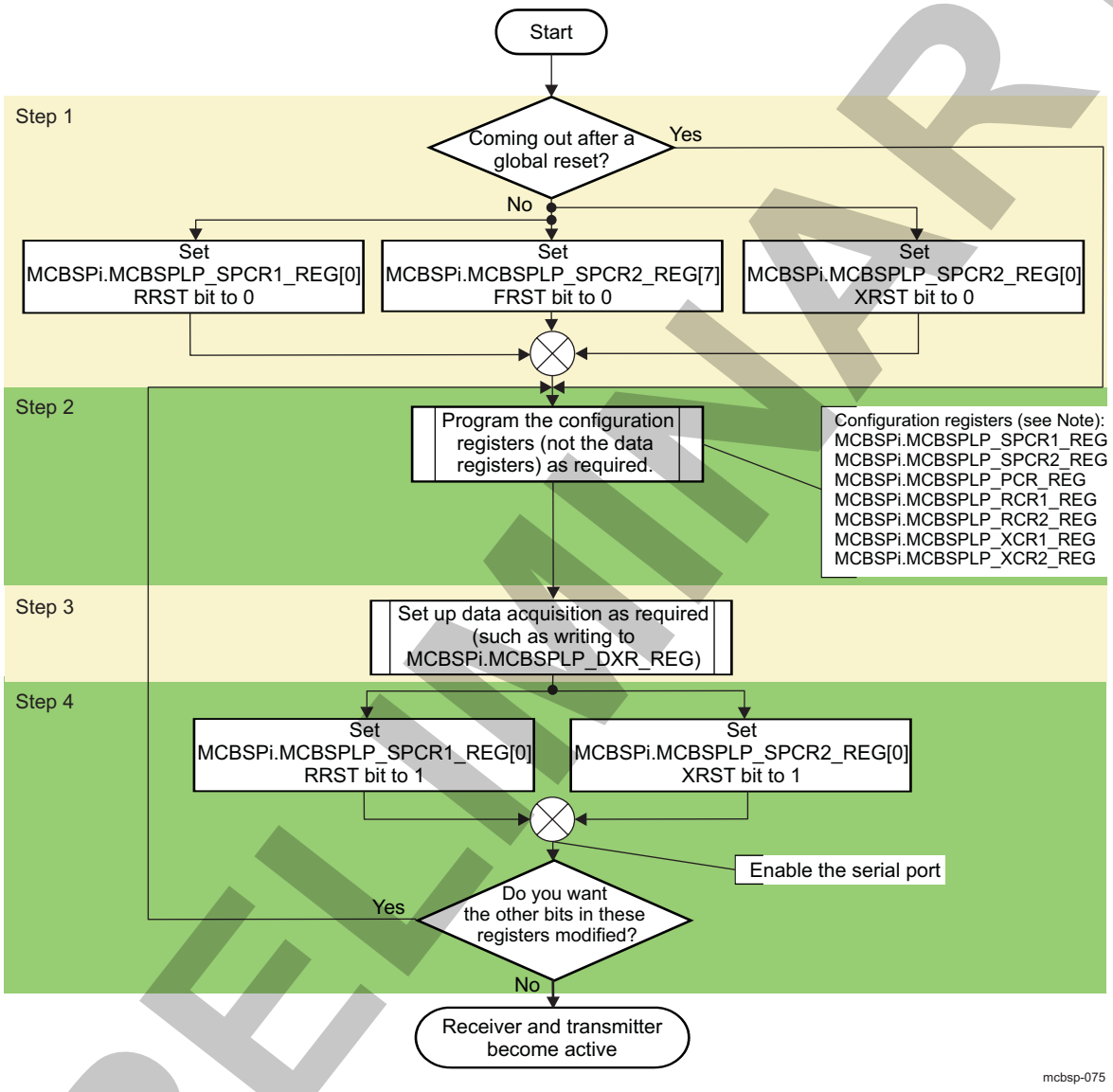
Alternatively, on write (Step 1 or Step 4), the transmitter and receiver can be placed in or taken out of reset by modifying the MCBSPi.MCBSPLP_SPCR2_REG[0] XRST and MCBSPi.MCBSPLP_SPCR1_REG[0] RRST bits, respectively.
Figure 23-141 shows the flow diagram of the MCBSP initialization procedure for slave mode.

Figure 23-141. Flow Diagram of MCBSP Initialization Procedure for Slave Mode



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NOTE:

- Alternatively, on write (Step 1 or Step 4), the transmitter and receiver can be placed in or taken out of reset by modifying the MCBSPi.MCBSPLP_SPCR2_REG[0] XRST and MCBSPi.MCBSPLP_SPCR1_REG[0] RRST bits, respectively.
- The necessary duration of the active-low period of XRST or RRST is at least two CLKR/CLKX cycles.
- The appropriate bits in serial port configuration registers (MCBSPi.MCBSPLP_SPCR1_REG, MCBSPi.MCBSPLP_SPCR2_REG, MCBSPi.MCBSPLP_PCR_REG, MCBSPi.MCBSPLP_RCR1_REG, MCBSPi.MCBSPLP_RCR2_REG, MCBSPi.MCBSPLP_XCR1_REG, MCBSPi.MCBSPLP_XCR2_REG, MCBSPi.MCBSPLP_THRSH2_REG, MCBSPi.MCBSPLP_XCCR_REG, MCBSPi.MCBSPLP_SYSCONFIG_REG, MCBSPi.MCBSPLP_SRGR1_REG and MCBSPi.MCBSPLP_SRGR2_REG) should be modified only when the affected portion of the serial port is in its reset state.
- In most cases, the data transmit register (MCBSPi.MCBSPLP_DXR_REG) should be loaded by the MPU/DSP subsystem or the sDMA controller only when the transmitter is enabled (MCBSPi.MCBSPLP_SPCR2_REG[0] XRST = 1). An exception to this rule is when these registers are used for loopback internal data.
- The bits of the channel control registers (MCBSPi.MCBSPLP_MCR1_REG, MCBSPi.MCBSPLP_MCR2_REG, MCBSPi.MCBSPLP_RCER{A-H}_REG and MCBSPi.MCBSPLP_XCER{A-H}_REG) can be modified at any time as long as they are not being used by the current reception/transmission in a multichannel selection mode.
- The SRG is reset by setting the MCBSPi.MCBSPLP_SPCR2_REG[6] GRST bit to 0.
- It is not necessary to wait if SRG is not used.
- The necessary duration of the active-low period of XRST or RRST is at least two
- Modification on-the-fly has no effect if a reset is not performed first.

Table 23-344. Register Call Summary for Flow Diagram of MCBSP Initialization Procedure

Register Name	Register Name	Register Name
MCBSPLP_SPCR1_REG	MCBSPLP_RCR1_REG	MCBSPLP_XCR2_REG
MCBSPLP_SPCR2_REG	MCBSPLP_RCR2_REG	MCBSPLP_SRGR1_REG
MCBSPLP_PCR_REG	MCBSPLP_XCR1_REG	MCBSPLP_SRGR2_REG

23.5.5.2 Reset and Initialization Procedure for the SRG

To reset and initialize the SRG:

1. Place the MCBSP SRG in reset.
2. Program the registers that affect the SRG.
3. Enable the SRG (take it out of reset).
4. If necessary, enable the receiver and/or the transmitter.
5. If necessary, remove the receiver and/or transmitter from reset

Figure 23-142 shows the flow diagram for programming the SRG registers.

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Figure 23-142. Flow Diagram for the SRG Registers Programmation

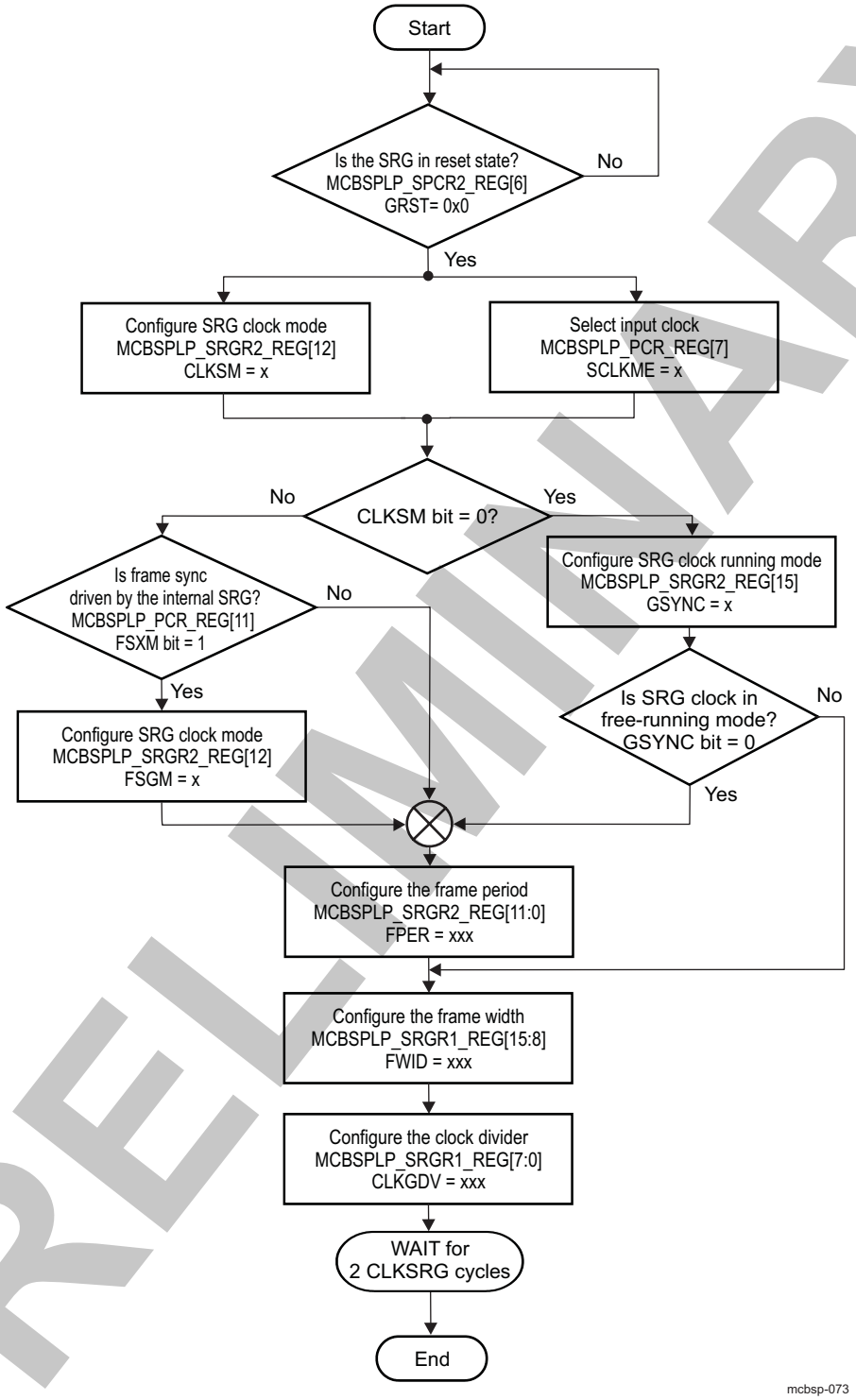

Table 23-345. Register Call Summary for Flow Diagram for the SRG Registers Programmation

Register Name	Register Name
MCBSPLP_SPCR2_REG	MCBSPLP_PCR_REG
MCBSPLP_SRGR2_REG	MCBSPLP_SRGR1_REG

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23.5.5.3 Data Transfer DMA Request Configuration

This procedure configures the MCBSP receive/transmit data DMA requests (MCBSPi_DMA_RX and MCBSPi_DMA_TX) (see Table 23-346).

Table 23-346. Data Transfer DMA Request Configuration

Step	Register/Bit Field/Programming Model	Value
Write the required receive DMA request length.	MCBSPLP_THRSH1_REG[6:0] RTHRESHOLD	x..x
Write the required transmit DMA request length.	MCBSPLP_THRSH2_REG[6:0] RTHRESHOLD	x..x

NOTE:

- The length of the transfer is the same as the threshold value + 1
- In case of a number of transfers that exceed the number of the programmed DMA length, the MCBSP module will respond to the command and will perform the transfer regardless of the receive buffer empty condition.
- In case of a number of transfers that exceed the number of the programmed DMA length, the MCBSP module will respond to the command and will perform the transfer regardless of the transmit buffer full condition.

23.5.5.4 Interrupt Configuration

This procedure configures the common receive/transmit interrupt request line (see Table 23-347).

Table 23-347. Interruption Configuration

Step	Register/Bit Field/Programming Model	Value
Enable the required IRQ events.	MCBSPLP_IRQENABLE_REG	x..x

23.5.5.5 Receiver Configuration

To configure the MCBSP receiver, perform the following steps:

Step 1. Place the MCBSP receiver in reset.

Step 2. Program the MCBSP registers for the desired receiver operation.

Step 3. Take the receiver out of reset.

23.5.5.5.1 Place the Receiver in Reset (Step 1)

Table 23-348. Receiver Reset

Step	Register/Bit Field/Programming Model	Value
Place the receiver in reset.	MCBSPLP_SPCR1_REG[0] RST	0x0

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23.5.5.5.2 Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2)

This section describes the steps to be performed when software configures the MCBSP receiver.

Global Configuration

Table 23-349 describes the steps to perform the global configuration.

Table 23-349. Global Configuration

Step	Register/Bit Field/Programming Model	Value
Set the receiver pins to operate as MCBSP pins.	MCBSPLP_PCR_REG[12] RIOEN	0x0
Enable/disable DLB mode(1).	MCBSPLP_XCCR_REG[5] DLB	0x0 or 0x1
Enable/disable ALB mode(1).	MCBSPLP_SPCR1_REG[5] ALB	0x0 or 0x1
Enable/disable the receive multichannel selection Mode(1).	MCBSPLP_MCR1_REG[0] RMCM	0x0 or 0x1

(1) Software decision

NOTE: In DLB mode the SRG and frame-sync generator must be enabled to generate the CLKX and FSX signals.

Data Configuration

Table 23-350 describes the steps to perform the data configuration.

Table 23-350. Data Configuration

Step	Register/Bit Field/Programming Model	Value
Select single/dual-phase frame (1).	MCBSPLP_RCR2_REG[15] RPHASE	0x0 or 0x1
Set the receive word length(s) for phase 1(1).	MCBSPLP_RCR1_REG[7:5] RWDLEN1	xxx
Set the receive word length(s) for phase 2(1).	MCBSPLP_RCR2_REG[7:5] XWDLEN2	xxx
Set the receive frame length*.	MCBSPLP_RCR1_REG[14:8] RFRLEN1 MCBSPLP_RCR2_REG[14:8] RFRLEN2	xxx
Set the receive reverse mode(1).	MCBSPLP_RCR2_REG[4:3] RREVERSE	xx
Set the receive data delay(1).	MCBSPLP_RCR2_REG[1:0] RDATLY	xx
Set the receive sign-extension and justification mode(1).	MCBSPLP_SPCR1_REG[14:13] RJUST	xx
Enable the serial receiver port.	MCBSPLP_SPCR1_REG[0] RRST	0x1
Configure the receive buffer threshold value(1).	MCBSPLP_THRSH1_REG[6:0] RTHRESHOLD	x..x

(1) Software decision

NOTE:

- When dual-phase frame is selected, the number of words per phase must be set to 1.
- If a single-phase frame is selected, RWDLEN1 selects the length for every serial word received in the frame. If a dual-phase frame is selected, RWDLEN1 and RWDLEN2 must be set to select both lengths. These bits can have different values.
- If a dual-phase frame is selected, the frame length must be two words.

Frame-Sync Configuration

Table 23-351 describes the steps to perform the frame-sync configuration.

Table 23-351. Frame-Sync Configuration

Step	Register/Bit Field/Programming Model	Value
Set the receive frame-sync mode(1).	MCBSPLP_PCR_REG[10] FSRM	0x0 or 0x1
Select SRG synchronization(1).	MCBSPLP_SRGR2_REG[15] GSYNC	0x0 or 0x1

(1) Software decision

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Table 23-351. Frame-Sync Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Set the receive frame-sync polarity [(1)].	MCBSPLP_PCR_REG[2] FSRP	0x0 or 0x1
Set the SRG frame-sync period[(1)].	MCBSPLP_SRGR2_REG[11:0] FPER	x..x
Set the SRG frame-sync pulse width[(1)].	MCBSPLP_SRGR1_REG[15:8] FWID	x..x

Clock Configuration

Table 23-352 describes the steps to perform clock configuration.

Table 23-352. Clock Configuration

Step	Register/Bit Field/Programming Model	Value
Set the receive clock mode[(1)].	MCBSPLP_PCR_REG[8] CLKRM	0x0 or 0x1
Set the receive clock polarity[(1)].	MCBSPLP_PCR_REG[0] CLKRP	0x0 or 0x1
Set the SRG clock divide-down value[(1)].	MCBSPLP_SRGR1_REG[7:0] CLKGDV	x..x
Set the SRG clock synchronization mode[(1)].	MCBSPLP_SRGR2_REG[15] GSYNC	0x0 or 0x1
Set the SRG input clock mode[(1)].	MCBSPLP_PCR_REG[7] SCKLME MCBSPLP_SRGR2_REG[13] CLKSM	0x0 or 0x1
Set the SRG input clock polarity[(1)].	MCBSPLP_SRGR2_REG[14] CLKSP MCBSPLP_PCR_REG[1] CLKXP MCBSPLP_PCR_REG[0] CLKRP	0x0 or 0x1

(1) Software decision

NOTE: CLKRP = CLKXP in a system in which the same clock (internal or external) is used to clock the receiver and transmitter. The receiver uses the opposite edge as the transmitter to ensure valid setup and hold of data around this edge.

23.5.5.5.3 Take the Receiver Out of Reset (Step 3)

Table 23-353. Take the Receiver Out of Reset

Step	Register/Bit Field/Programming Model	Value
Enable the receiver.	MCBSPLP_SPCR1_REG[0] RST	0x1

23.5.5.6 Transmitter Configuration

To configure the MCBSP transmitter, perform the following steps:

Step 1. Place the MCBSP transmitter in reset.

Step 2. Program the MCBSP registers for the desired transmitter operation.

Step 3. Take the transmitter out of reset.

23.5.5.6.1 Place the Transmitter in Reset (Step 1)

Table 23-354. Transmitter Reset

Step	Register/Bit Field/Programming Model	Value
Place the transmitter in reset.	MCBSPLP_SPCR2_REG[0] RST	0x0

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23.5.5.6.2 Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2)

This section describes the steps to be performed when software configures the MCBSP transmitter.

Global Configuration

Table 23-355 describes the steps to perform the global configuration.

Table 23-355. Global Configuration

Step	Register/Bit Field/Programming Model	Value
Set the transmitter pins to operate as MCBSP pins.	MCBSPLP_PCR_REG[13] XIOEN	0x0
Enable/disable DLB mode(1).	MCBSPLP_XCCR_REG[5] DLB	0x0 or 0x1
Enable/disable ALB mode(1).	MCBSPLP_SPCR1_REG[5] ALB	0x0 or 0x1
Enable/disable the transmit multichannel selection mode(1).	MCBSPLP_MCR1_REG[0] RMCM	0x0 or 0x1

(1) Software decision

Data Configuration

Table 23-356 describes the steps to perform the data configuration.

Table 23-356. Data Configuration

Step	Register/Bit Field/Programming Model	Value
Select single/dual-phase frame (1).	MCBSPLP_RCR2_REG[15] XPHASE	0x0 or 0x1
Set the transmit word length(s) for phase 1(1).	MCBSPLP_XCR1_REG[7:5] XWDLEN1	xxx
Set the transmit word length(s) for phase 2(1).	MCBSPLP_XCR2_REG[7:5] XWDLEN2	xxx
Set the transmit frame length(1).	MCBSPLP_XCR1_REG[14:8] XFRLEN1 MCBSPLP_XCR2_REG[14:8] XFRLEN2	xxx
Set the transmit reverse mode(1).	MCBSPLP_XCR2_REG[4:3] XREVERSE	xx
Set the transmit data delay(1).	MCBSPLP_XCR2_REG[1:0] XDATLY	xx
Set the extra delay (DX delay) mode(1).	MCBSPLP_SPCR1_REG[7] DXENA	xx
Select the inserted delay value(1).	MCBSPLP_XCCR_REG[13:12] DXENDLY	xx
Set the interrupt line.	MCBSPLP_IRQENABLE_REG	x..x
Configure the transmit buffer threshold value(1)	MCBSPLP_THRSH2_REG[6:0] XTHRESHOLD	x..x

(1) Software decision

NOTE:

- When dual-phase frame is selected, the number of words per phase must be set to 1.
- If a single-phase frame is selected, XWDLEN1 selects the length for every serial word transmit in the frame. If a dual–phase frame is selected, XWDLEN1 and XWDLEN2 must be set to select both lengths. These bits can have different values.
- If a dual-phase frame is selected, the frame length must be two words.

The DXENA bit controls the delay enabler on the MCBSP_dx pin. Set DXENA to enable an extra delay for turn-on time. Because this bit does not control the data itself, only the first bit is delayed (the delay is given by a combinatorial delay buffer). The inserted delay, 80 ps, 160 ps (default), 240 ps, or 320 ps, can be set using the MCBSPi.MCBSPLP_XCCR_REG[13:12] DXENDLY bit field. If the MCBSP_dx pins of multiple MCBSP modules are tied together, ensure that DXENA is set to 1 to avoid having more than one MCBSP at a time transmitting on the data line.

Frame-Sync Configuration

Table 23-357 describes the steps to perform the frame-sync configuration.

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Table 23-357. Frame-Sync Configuration

Step	Register / Bit Field / Programming Model	Value
Set the transmit frame-sync mode(1).	MCBSPLP_PCR_REG[11] FSXM MCBSPLP_SRGR2_REG[12] FSGM	0x0 or 0x1
Set the transmit frame-sync polarity(1).	MCBSPLP_PCR_REG[3] FSXP	0x0 or 0x1
Set the SRG frame-sync period(1).	MCBSPLP_SRGR2_REG[11:0] FPER	x..x
Set the SRG frame-sync pulse width(1).	MCBSPLP_SRGR1_REG[15:8] FWID	x..x

(1) Software decision

Clock Configuration

Table 23-358 describes the steps to perform the clock configuration.

Table 23-358. Clock Configuration

Step	Register / Bit Field / Programming Model	Value
Set the transmit clock mode (1).	MCBSPLP_PCR_REG[9] CLKXM	0x0 or 0x1
Set the transmit clock polarity(1).	MCBSPLP_PCR_REG[1] CLKXP	0x0 or 0x1
Set the SRG clock divide-down value(1).	MCBSPLP_SRGR1_REG[7:0] CLKGDV	x..x
Set the SRG clock synchronization mode(1).	MCBSPLP_SRGR2_REG[15] GSYNC	0x0 or 0x1
Set the SRG input clock mode(1).	MCBSPLP_PCR_REG[7] SCKLME MCBSPLP_SRGR2_REG[13] CLKSM	0x0 or 0x1
Set the SRG input clock polarity(1)	MCBSPLP_SRGR2_REG[14] CLKSP MCBSPLP_PCR_REG[1] CLKXP MCBSPLP_PCR_REG[0] CLKRP	0x0 or 0x1

(1) Software decision

NOTE: CLKRP = CLKXP in a system in which the same clock (internal or external) is used to clock the receiver and transmitter. The receiver uses the opposite edge as the transmitter to ensure valid setup and hold of data around this edge.

23.5.5.6.3 Take the Receiver Out of Reset (Step 3)

Table 23-359. Take the Receiver Out of Reset

Step	Register/Bit Field/Programming Model	Value
Enable the transmitter.	MCBSPLP_SPCR2_REG[0] RST	0x1

23.5.5.7 GPIO on the MCBSP Pins (Legacy Only)

To use MCBSP pins as GPIO pins rather than as serial port pins, follow these steps:

- **For the receive pins (MCBSP_clkr, MCBSP_fsr, and MCBSP_dr as)**

Table 23-360. Use Serial Receive Pins as GPIO Pins

Step	Register/Bit Field/Programming Model	Value
Place the receiver in reset.	MCBSPLP_SPCR1_REG[0] RRST	0x0
Enable GPIO for the serial port receiver.	MCBSPLP_PCR_REG[12] RIOEN	0x1

- **For the transmitter pins (MCBSP_clkx, MCBSP_fsx, and MCBSP_dx)**

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Table 23-361. Use Serial Transmit Pins as GPIO Pins

Step	Register/Bit Field/ Programming Model	Value
Place the transmit in reset.	MCBSPLP_SPCR2_REG[0] XRST	0x0
Enable GPIO for the serial port transmitter.	MCBSPLP_PCR_REG[12] XIOEN	0x1

- **For the external clock pins (abe_clks)**

  For the abe_clks pin (common to all MCBSP modules), all of the reset and I/O conditions must be met as follows:

Table 23-362. Use External Clock Pin as GPIO Pin

Step	Register/Bit Field/Programming Model	Value
Place the receiver in reset.	MCBSPLP_SPCR1_REG[0] RRST	0x0
Place the transmit in reset.	MCBSPLP_SPCR2_REG[0] XRST	0x0
Enable GPIO for the serial port receiver.	MCBSPLP_PCR_REG[12] RIOEN	0x1
Enable GPIO for the serial port transmitter.	MCBSPLP_PCR_REG[12] XIOEN	0x1

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23.5.6 MCBSP Register Manual

Table 23-363 shows the base address and address space for the device module instances.

23.5.6.1 MCBSP Instance Summary

Table 23-363. MCBSP Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-A15 Private Access	Base Address DSP Private Access	Size
MCBSP1	0x4902 2000	0x4012 2000	0x2 2000	4 KiB
MCBSP2	0x4902 4000	0x4012 4000	0x2 4000	4 KiB
MCBSP3	0x4902 6000	0x4012 6000	0x2 6000	4 KiB

NOTE: Private access is an access that does not use the L3/L4 interconnects.

23.5.6.2 MCBSP Registers

CAUTION

The MCBSP registers are limited to 32-bit data accesses; 16- and 8-bit accesses are not allowed and can corrupt register content.

23.5.6.2.1 MCBSP Register Summary

Table 23-364 through summarize the MCBSP1, MCBSP2 and MCBSP3 registers, respectively.

Table 23-364. MCBSP1 Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A15 Private Access	Physical Address DSP Private Access
MCBSPLP_DRR_REG	R	32	0x0000 0000	0x4902 2000	0x4012 2000	0x2 2000
MCBSPLP_DXR_REG	W	32	0x0000 0008	0x4902 2008	0x4012 2008	0x2 2008
MCBSPLP_SPCR2_REG	RW	32	0x0000 0010	0x4902 2010	0x4012 2010	0x2 2010
MCBSPLP_SPCR1_REG	RW	32	0x0000 0014	0x4902 2014	0x4012 2014	0x2 2014
MCBSPLP_RCR2_REG	RW	32	0x0000 0018	0x4902 2018	0x4012 2018	0x2 2018
MCBSPLP_RCR1_REG	RW	32	0x0000 001C	0x4902 201C	0x4012 201C	0x2 201C
MCBSPLP_XCR2_REG	RW	32	0x0000 0020	0x4902 2020	0x4012 2020	0x2 2020
MCBSPLP_XCR1_REG	RW	32	0x0000 0024	0x4902 2024	0x4012 2024	0x2 2024
MCBSPLP_SRGR2_REG	RW	32	0x0000 0028	0x4902 2028	0x4012 2028	0x2 2028
MCBSPLP_SRGR1_REG	RW	32	0x0000 002C	0x4902 202C	0x4012 202C	0x2 202C
MCBSPLP_MCR2_REG	RW	32	0x0000 0030	0x4902 2030	0x4012 2030	0x2 2030
MCBSPLP_MCR1_REG	RW	32	0x0000 0034	0x4902 2034	0x4012 2034	0x2 2034
MCBSPLP_RCERA_REG	RW	32	0x0000 0038	0x4902 2038	0x4012 2038	0x2 2038
MCBSPLP_RCERB_REG	RW	32	0x0000 003C	0x4902 203C	0x4012 203C	0x2 203C
MCBSPLP_XCERA_REG	RW	32	0x0000 0040	0x4902 2040	0x4012 2040	0x2 2040
MCBSPLP_XCERB_REG	RW	32	0x0000 0044	0x4902 2044	0x4012 2044	0x2 2044
MCBSPLP_PCR_REG	RW	32	0x0000 0048	0x4902 2048	0x4012 2048	0x2 2048
MCBSPLP_RCERC_REG	RW	32	0x0000 004C	0x4902 204C	0x4012 204C	0x2 204C
MCBSPLP_RCERD_REG	RW	32	0x0000 0050	0x4902 2050	0x4012 2050	0x2 2050
MCBSPLP_XCERC_REG	RW	32	0x0000 0054	0x4902 2054	0x4012 2054	0x2 2054

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Table 23-364. MCBSP1 Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A15 Private Access	Physical Address DSP Private Access
MCBSPLP_XCERD_REG	RW	32	0x0000 0058	0x4902 2058	0x4012 2058	0x2 2058
MCBSPLP_RCERE_REG	RW	32	0x0000 005C	0x4902 205C	0x4012 205C	0x2 205C
MCBSPLP_RCERF_REG	RW	32	0x0000 0060	0x4902 2060	0x4012 2060	0x2 2060
MCBSPLP_XCERE_REG	RW	32	0x0000 0064	0x4902 2064	0x4012 2064	0x2 2064
MCBSPLP_XCERF_REG	RW	32	0x0000 0068	0x4902 2068	0x4012 2068	0x2 2068
MCBSPLP_RCERG_REG	RW	32	0x0000 006C	0x4902 206C	0x4012 206C	0x2 206C
MCBSPLP_RCERH_REG	RW	32	0x0000 0070	0x4902 2070	0x4012 2070	0x2 2070
MCBSPLP_XCERG_REG	RW	32	0x0000 0074	0x4902 2074	0x4012 2074	0x2 2074
MCBSPLP_XCERH_REG	RW	32	0x0000 0078	0x4902 2078	0x4012 2078	0x2 2078
MCBSPLP_REV_REG	R	32	0x0000 007C	0x4902 207C	0x4012 207C	0x2 207C
MCBSPLP_RINTCLR_REG	RW	32	0x0000 0080	0x4902 2080	0x4012 2080	0x2 2080
MCBSPLP_XINTCLR_REG	RW	32	0x0000 0084	0x4902 2084	0x4012 2084	0x2 2084
MCBSPLP_ROVFLCLR_REG	RW	32	0x0000 0088	0x4902 2088	0x4012 2088	0x2 2088
MCBSPLP_SYSCONFIG_REG	RW	32	0x0000 008C	0x4902 208C	0x4012 208C	0x2 208C
MCBSPLP_THRSH2_REG	RW	32	0x0000 0090	0x4902 2090	0x4012 2090	0x2 2090
MCBSPLP_THRSH1_REG	RW	32	0x0000 0094	0x4902 2094	0x4012 2094	0x2 2094
MCBSPLP_IRQSTATUS_REG	RW	32	0x0000 00A0	0x4902 20A0	0x4012 20A0	0x2 20A0
MCBSPLP_IRQENABLE_REG	RW	32	0x0000 00A4	0x4902 20A4	0x4012 20A4	0x2 20A4
MCBSPLP_WAKEUPEN_REG	RW	32	0x0000 00A8	0x4902 20A8	0x4012 20A8	0x2 20A8
MCBSPLP_XCCR_REG	RW	32	0x0000 00AC	0x4902 20AC	0x4012 20AC	0x2 20AC
MCBSPLP_RCCR_REG	RW	32	0x0000 00B0	0x4902 20B0	0x4012 20B0	0x2 20B0
MCBSPLP_XBUFFSTAT_REG	R	32	0x0000 00B4	0x4902 20B4	0x4012 20B4	0x2 20B4
MCBSPLP_RBUFFSTAT_REG	R	32	0x0000 00B8	0x4902 20B8	0x4012 20B8	0x2 20B8

Table 23-365. MCBSP2 Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A15 Private Access	Physical Address DSP Private Access
MCBSPLP_DRR_REG	R	32	0x0000 0000	0x4902 4000	0x4012 4000	0x2 4000
MCBSPLP_DXR_REG	W	32	0x0000 0008	0x4902 4008	0x4012 4008	0x2 4008
MCBSPLP_SPCR2_REG	RW	32	0x0000 0010	0x4902 4010	0x4012 4010	0x2 4010
MCBSPLP_SPCR1_REG	RW	32	0x0000 0014	0x4902 4014	0x4012 4014	0x2 4014
MCBSPLP_RCR2_REG	RW	32	0x0000 0018	0x4902 4018	0x4012 4018	0x2 4018
MCBSPLP_RCR1_REG	RW	32	0x0000 001C	0x4902 401C	0x4012 401C	0x2 401C
MCBSPLP_XCR2_REG	RW	32	0x0000 0020	0x4902 4020	0x4012 4020	0x2 4020
MCBSPLP_XCR1_REG	RW	32	0x0000 0024	0x4902 4024	0x4012 4024	0x2 4024
MCBSPLP_SRGR2_REG	RW	32	0x0000 0028	0x4902 4028	0x4012 4028	0x2 4028
MCBSPLP_SRGR1_REG	RW	32	0x0000 002C	0x4902 402C	0x4012 402C	0x2 402C
MCBSPLP_MCR2_REG	RW	32	0x0000 0030	0x4902 4030	0x4012 4030	0x2 4030
MCBSPLP_MCR1_REG	RW	32	0x0000 0034	0x4902 4034	0x4012 4034	0x2 4034
MCBSPLP_RCERA_REG	RW	32	0x0000 0038	0x4902 4038	0x4012 4038	0x2 4038
MCBSPLP_RCERB_REG	RW	32	0x0000 003C	0x4902 403C	0x4012 403C	0x2 403C

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Table 23-365. MCBSP2 Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A15 Private Access	Physical Address DSP Private Access
MCBSPLP_XCERA_REG	RW	32	0x0000 0040	0x4902 4040	0x4012 4040	0x2 4040
MCBSPLP_XCERB_REG	RW	32	0x0000 0044	0x4902 4044	0x4012 4044	0x2 4044
MCBSPLP_PCR_REG	RW	32	0x0000 0048	0x4902 4048	0x4012 4048	0x2 4048
MCBSPLP_RCERC_REG	RW	32	0x0000 004C	0x4902 404C	0x4012 404C	0x2 404C
MCBSPLP_RCERD_REG	RW	32	0x0000 0050	0x4902 4050	0x4012 4050	0x2 4050
MCBSPLP_XCERC_REG	RW	32	0x0000 0054	0x4902 4054	0x4012 4054	0x2 4054
MCBSPLP_XCERD_REG	RW	32	0x0000 0058	0x4902 4058	0x4012 4058	0x2 4058
MCBSPLP_RCERE_REG	RW	32	0x0000 005C	0x4902 405C	0x4012 405C	0x2 405C
MCBSPLP_RCERF_REG	RW	32	0x0000 0060	0x4902 4060	0x4012 4060	0x2 4060
MCBSPLP_XCERE_REG	RW	32	0x0000 0064	0x4902 4064	0x4012 4064	0x2 4064
MCBSPLP_XCERF_REG	RW	32	0x0000 0068	0x4902 4068	0x4012 4068	0x2 4068
MCBSPLP_RCERG_REG	RW	32	0x0000 006C	0x4902 406C	0x4012 406C	0x2 406C
MCBSPLP_RCERH_REG	RW	32	0x0000 0070	0x4902 4070	0x4012 4070	0x2 4070
MCBSPLP_XCERG_REG	RW	32	0x0000 0074	0x4902 4074	0x4012 4074	0x2 4074
MCBSPLP_XCERH_REG	RW	32	0x0000 0078	0x4902 4078	0x4012 4078	0x2 4078
MCBSPLP_REV_REG	R	32	0x0000 007C	0x4902 407C	0x4012 407C	0x2 407C
MCBSPLP_RINTCLR_REG	RW	32	0x0000 0080	0x4902 4080	0x4012 4080	0x2 4080
MCBSPLP_XINTCLR_REG	RW	32	0x0000 0084	0x4902 4084	0x4012 4084	0x2 4084
MCBSPLP_ROVFLCLR_REG	RW	32	0x0000 0088	0x4902 4088	0x4012 4088	0x2 4088
MCBSPLP_SYSCONFIG_REG	RW	32	0x0000 008C	0x4902 408C	0x4012 408C	0x2 408C
MCBSPLP_THRSH2_REG	RW	32	0x0000 0090	0x4902 4090	0x4012 4090	0x2 4090
MCBSPLP_THRSH1_REG	RW	32	0x0000 0094	0x4902 4094	0x4012 4094	0x2 4094
MCBSPLP_IRQSTATUS_REG	RW	32	0x0000 00A0	0x4902 40A0	0x4012 40A0	0x2 40A0
MCBSPLP_IRQENABLE_REG	RW	32	0x0000 00A4	0x4902 40A4	0x4012 40A4	0x2 40A4
MCBSPLP_WAKEUPEN_REG	RW	32	0x0000 00A8	0x4902 40A8	0x4012 40A8	0x2 40A8
MCBSPLP_XCCR_REG	RW	32	0x0000 00AC	0x4902 40AC	0x4012 40AC	0x2 40AC
MCBSPLP_RCCR_REG	RW	32	0x0000 00B0	0x4902 40B0	0x4012 40B0	0x2 40B0
MCBSPLP_XBUFFSTAT_REG	R	32	0x0000 00B4	0x4902 40B4	0x4012 40B4	0x2 40B4
MCBSPLP_RBUFFSTAT_REG	R	32	0x0000 00B8	0x4902 40B8	0x4012 40B8	0x2 40B8

Table 23-366. MCBSP3 Register Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A15 Private Access	Physical Address DSP Private Access
MCBSPLP_DRR_REG	R	32	0x0000 0000	0x4902 6000	0x4012 6000	0x2 6000
MCBSPLP_DXR_REG	W	32	0x0000 0008	0x4902 6008	0x4012 6008	0x2 6008
MCBSPLP_SPCR2_REG	RW	32	0x0000 0010	0x4902 6010	0x4012 6010	0x2 6010
MCBSPLP_SPCR1_REG	RW	32	0x0000 0014	0x4902 6014	0x4012 6014	0x2 6014
MCBSPLP_RCR2_REG	RW	32	0x0000 0018	0x4902 6018	0x4012 6018	0x2 6018
MCBSPLP_RCR1_REG	RW	32	0x0000 001C	0x4902 601C	0x4012 601C	0x2 601C
MCBSPLP_XCR2_REG	RW	32	0x0000 0020	0x4902 6020	0x4012 6020	0x2 6020
MCBSPLP_XCR1_REG	RW	32	0x0000 0024	0x4902 6024	0x4012 6024	0x2 6024

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Table 23-366. MCBSP3 Register Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A15 Private Access	Physical Address DSP Private Access
MCBSPLP_SRGR2_REG	RW	32	0x0000 0028	0x4902 6028	0x4012 6028	0x2 6028
MCBSPLP_SRGR1_REG	RW	32	0x0000 002C	0x4902 602C	0x4012 602C	0x2 602C
MCBSPLP_MCR2_REG	RW	32	0x0000 0030	0x4902 6030	0x4012 6030	0x2 6030
MCBSPLP_MCR1_REG	RW	32	0x0000 0034	0x4902 6034	0x4012 6034	0x2 6034
MCBSPLP_RCERA_REG	RW	32	0x0000 0038	0x4902 6038	0x4012 6038	0x2 6038
MCBSPLP_RCERB_REG	RW	32	0x0000 003C	0x4902 603C	0x4012 603C	0x2 603C
MCBSPLP_XCERA_REG	RW	32	0x0000 0040	0x4902 6040	0x4012 6040	0x2 6040
MCBSPLP_XCERB_REG	RW	32	0x0000 0044	0x4902 6044	0x4012 6044	0x2 6044
MCBSPLP_PCR_REG	RW	32	0x0000 0048	0x4902 6048	0x4012 6048	0x2 6048
MCBSPLP_RCERC_REG	RW	32	0x0000 004C	0x4902 604C	0x4012 604C	0x2 604C
MCBSPLP_RCERD_REG	RW	32	0x0000 0050	0x4902 6050	0x4012 6050	0x2 6050
MCBSPLP_XCERC_REG	RW	32	0x0000 0054	0x4902 6054	0x4012 6054	0x2 6054
MCBSPLP_XCERD_REG	RW	32	0x0000 0058	0x4902 6058	0x4012 6058	0x2 6058
MCBSPLP_RCERE_REG	RW	32	0x0000 005C	0x4902 605C	0x4012 605C	0x2 605C
MCBSPLP_RCERF_REG	RW	32	0x0000 0060	0x4902 6060	0x4012 6060	0x2 6060
MCBSPLP_XCERE_REG	RW	32	0x0000 0064	0x4902 6064	0x4012 6064	0x2 6064
MCBSPLP_XCERF_REG	RW	32	0x0000 0068	0x4902 6068	0x4012 6068	0x2 6068
MCBSPLP_RCERG_REG	RW	32	0x0000 006C	0x4902 606C	0x4012 606C	0x2 606C
MCBSPLP_RCERH_REG	RW	32	0x0000 0070	0x4902 6070	0x4012 6070	0x2 6070
MCBSPLP_XCERG_REG	RW	32	0x0000 0074	0x4902 6074	0x4012 6074	0x2 6074
MCBSPLP_XCERH_REG	RW	32	0x0000 0078	0x4902 6078	0x4012 6078	0x2 6078
MCBSPLP_REV_REG	R	32	0x0000 007C	0x4902 607C	0x4012 607C	0x2 607C
MCBSPLP_RINTCLR_REG	RW	32	0x0000 0080	0x4902 6080	0x4012 6080	0x2 6080
MCBSPLP_XINTCLR_REG	RW	32	0x0000 0084	0x4902 6084	0x4012 6084	0x2 6084
MCBSPLP_ROVFLCLR_REG	RW	32	0x0000 0088	0x4902 6088	0x4012 6088	0x2 6088
MCBSPLP_SYSCONFIG_REG	RW	32	0x0000 008C	0x4902 608C	0x4012 608C	0x2 608C
MCBSPLP_THRSH2_REG	RW	32	0x0000 0090	0x4902 6090	0x4012 6090	0x2 6090
MCBSPLP_THRSH1_REG	RW	32	0x0000 0094	0x4902 6094	0x4012 6094	0x2 6094
MCBSPLP_IRQSTATUS_REG	RW	32	0x0000 00A0	0x4902 60A0	0x4012 60A0	0x2 60A0
MCBSPLP_IRQENABLE_REG	RW	32	0x0000 00A4	0x4902 60A4	0x4012 60A4	0x2 60A4
MCBSPLP_WAKEUPEN_REG	RW	32	0x0000 00A8	0x4902 60A8	0x4012 60A8	0x2 60A8
MCBSPLP_XCCR_REG	RW	32	0x0000 00AC	0x4902 60AC	0x4012 60AC	0x2 60AC
MCBSPLP_RCCR_REG	RW	32	0x0000 00B0	0x4902 60B0	0x4012 60B0	0x2 60B0
MCBSPLP_XBUFFSTAT_REG	R	32	0x0000 00B4	0x4902 60B4	0x4012 60B4	0x2 60B4
MCBSPLP_RBUFFSTAT_REG	R	32	0x0000 00B8	0x4902 60B8	0x4012 60B8	0x2 60B8

23.5.6.2.2 MCBSP Register Description

Table 23-367 through Table 23-451 describe the individual MCBSP registers.

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Table 23-367. MCBSPLP_DRR_REG

Address Offset	0x0000 0000		
Physical Address	0x4902 2000 0x4012 2000 0x2 2000 0x4902 4000 0x4012 4000 0x2 4000 0x4902 6000 0x4012 6000 0x2 6000	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP data receive register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRR																															

Bits	Field Name	Description	Type	Reset
31:0	DRR	Data receive register	R	0x0000 0000

Table 23-368. Register Call Summary for Register MCBSPLP_DRR_REG

Multichannel Buffered Serial Port (MCBSP)

- Data Transfer Process for 8-/12-/16-/20-/24-/32-Bit-Long Words: [0]
- Serial Words: [1]
- MCBSP Reception: [2] [3]
- Introduction: [4]
- Overrun in the Receiver: [5] [6]
- MCBSP Register Summary: [7] [8] [9]

Table 23-369. MCBSPLP_DXR_REG

Address Offset	0x0000 0008		
Physical Address	0x4902 2008 0x4012 2008 0x2 2008 0x4902 4008 0x4012 4008 0x2 4008 0x4902 6008 0x4012 6008 0x2 6008	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP data transmit register		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DXR																															

Bits	Field Name	Description	Type	Reset
31:0	DXR	Data transmit register	W	0x0000 0000

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Table 23-370. Register Call Summary for Register MCBSPLP_DXR_REG

Multichannel Buffered Serial Port (MCBSP)

- Data Transfer Process for 8-/12-/16-/20-/24-/32-Bit-Long Words: [0]
- MCBSP Transmission: [1] [2]
- Introduction: [3]
- Underflow in the Transmitter: [4] [5] [6] [7]
- Disabling/Enabling Versus Masking/Unmasking: [8]
- MCBSP Initialization Procedure: [9]
- MCBSP Register Summary: [10] [11] [12]

Table 23-371. MCBSPLP_SPCR2_REG

Address Offset	0x0000 0010		
Physical Address	0x4902 2010	**Instance**	MCBSP1_L3
	0x4012 2010		MCBSP1_CORTEX-A15
	0x2 2010		MCBSP1_DSP
	0x4902 4010		MCBSP2_L3
	0x4012 4010		MCBSP2_CORTEX-A15
	0x2 4010		MCBSP2_DSP
	0x4902 6010		MCBSP3_L3
	0x4012 6010		MCBSP3_CORTEX-A15
	0x2 6010		MCBSP3_DSP
Description	MCBSPLP serial port control register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						FREE	SOFT	FRST	GRST	XINTM		XSYNCERR	XEMPTY	XRDY	XRST

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9	FREE	Free Running Mode (When this bit is set, the module ignores the Msuspend input) 0x0: Free running mode is disabled 0x1: Free running mode is enabled	RW	0
8	SOFT	Soft Bit 0x0: SOFT mode is disabled: the module stops its activity immediately following MSuspend assertion 0x1: SOFT mode is enabled: the module freezes its state after completion of the current operation when MSuspend is asserted	RW	0
7	FRST	Frame-Sync Generator Reset 0x0: Frame-sync logic is reset. Frame-sync signal FSG is not generated by the sample-rate generator 0x1: Frame-sync signal FSG is generated after (FPER+1) number of CLKG clocks; that is, all frame counters are loaded with their programmed values	RW	0
6	GRST	Sample-Rate Generator Reset 0x0: SRG is reset 0x1: SRG is pulled out of reset. CLKG is driven as per programmed value in SRG registers (SRGR[1,2])	RW	0

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Bits	Field Name	Description	Type	Reset
5:4	XINTM	Transmit Interrupt Mode (legacy) 0x0: XINT is driven by XRDY 0x1: XINT generated by end-of-frame 0x2: XINT generated by a new frame synchronization 0x3: XINT generated by XSYNCERR	RW	0x0
3	XSYNCERR	Transmit Synchronization Error (writing 0 to this bit clear the legacy transmit interrupt if asserted due to XSYNCERR condition) 0x0: No synchronization error 0x1: Synchronization error detected by MCBSP	RW	0
2	XEMPTY	Transmit Shift Register XSR Empty Read 0x0: XSR is empty Read 0x1: XSR is not empty	R	0
1	XRDY	Transmitter ready Read 0x0: Transmitter is not ready. Read 0x1: Transmitter is ready for new data in DXR	R	0
0	XRST	Transmitter reset. This resets and enables the transmitter. 0x0: The serial port transmitter is disabled and in reset state. 0x1: The serial port transmitter is enabled.	RW	0

Table 23-372. Register Call Summary for Register MCBSPLP_SPCR2_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP Software Reset: [0] [1] [2]
- Data Transfer Process for 8-/12-/16-/20-/24-/32-Bit-Long Words: [3]
- MCBSP Transmission: [4] [5]
- Clock Generation in the SRG: [6]
- Frame-Sync Generation in the SRG: [7] [8]
- Introduction: [9] [10] [11]
- Underflow in the Transmitter: [12] [13] [14] [15] [16]
- Possible Responses to Transmit Frame-Sync Pulses: [17] [18] [19]
- MCBSP DMA Configuration: [20] [21]
- Disabling/Enabling Versus Masking/Unmasking: [22] [23] [24]
- MCBSP Initialization Procedure: [25] [26] [27] [28] [29] [30]
- Reset and Initialization Procedure for the SRG: [31]
- Place the Transmitter in Reset (Step 1): [32]
- Take the Receiver Out of Reset (Step 3): [33]
- GPIO on the MCBSP Pins (Legacy Only): [34] [35]
- MCBSP Register Summary: [36] [37] [38]

Table 23-373. MCBSPLP_SPCR1_REG

Address Offset	0x0000 0014		
Physical Address	0x4902 2014 0x4012 2014 0x2 2014 0x4902 4014 0x4012 4014 0x2 4014 0x4902 6014 0x4012 6014 0x2 6014	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP serial port control register 1		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ALB	RJUST	RESERVED						DXENA	RESERVED	RINTM		RSYNCERR	RFULL	RRDY	RRST

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	ALB	Analog Loopback Mode 0x0: Analog loopback mode disabled 0x1: Analog loopback mode enabled	RW	0
14:13	RJUST	Receive Sign-Extension and Justification Mode 0x0: Right-justify and zero-fill MSBs in DRR 0x1: Right-justify and sign-extend MSBs in DRR 0x2: Left-justify and zero-fill LSBs in DRR 0x3: Reserved	RW	0x0
12:8	RESERVED	Reserved	R	0x00
7	DXENA	DX Enabler 0x0: DX enabler is off 0x1: DX enabler is on	RW	0
6	RESERVED	Reserved	R	0
5:4	RINTM	Receive Interrupt Mode (legacy) 0x0: RINT driven by RRDY (that is, end of word) and end of frame in A-bis mode 0x1: RINT generated by end-of-block or end-of-frame in multichannel operation 0x2: RINT generated by a new frame synchronization 0x3: RINT generated by RSYNCERR	RW	0x0
3	RSYNCERR	Receive Synchronization Error (writing 0 to this bit clear the legacy receive interrupt if asserted due to RSYNCERR condition) 0x0: No synchronization error 0x1: Synchronization error detected by MCBSP	RW	0
2	RFULL	Receive Shift Register (RSR]) Full Read 0x0: DRR is not read, RB is full and RSR is also full with new word Read 0x1: RB is not in overrun condition	R	0
1	RRDY	Receiver Ready Read 0x0: Receiver is not ready Read 0x1: Receiver is ready with data to be read from DRR	R	0
0	RRST	Receiver reset. This resets and enables the receiver. 0x0: The serial port receiver is disabled and in reset state. 0x1: The serial port receiver is enabled.	RW	0

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Table 23-374. Register Call Summary for Register MCBSPLP_SPCR1_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP Software Reset: [0]
- MCBSP Reception: [1] [2] [3]
- Clock Generation in the SRG: [4]
- Introduction: [5] [6] [7] [8]
- Overrun in the Receiver: [9] [10] [11]
- Possible Responses to Receive Frame-Sync Pulses: [12] [13] [14]
- MCBSP DMA Configuration: [15] [16]
- Receive Multichannel Selection Mode: [17]
- MCBSP Initialization Procedure: [18] [19] [20] [21]
- Place the Receiver in Reset (Step 1): [22]
- Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2): [23] [24] [25]
- Take the Receiver Out of Reset (Step 3): [26]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [27] [28]
- GPIO on the MCBSP Pins (Legacy Only): [29] [30]
- MCBSP Register Summary: [31] [32] [33]

Table 23-375. MCBSPLP_RCR2_REG

Address Offset	0x0000 0018		
Physical Address	0x4902 2018	**Instance**	MCBSP1_L3
	0x4012 2018		MCBSP1_CORTEX-A15
	0x2 2018		MCBSP1_DSP
	0x4902 4018		MCBSP2_L3
	0x4012 4018		MCBSP2_CORTEX-A15
	0x2 4018		MCBSP2_DSP
	0x4902 6018		MCBSP3_L3
	0x4012 6018		MCBSP3_CORTEX-A15
	0x2 6018		MCBSP3_DSP
Description	MCBSPLP receive control register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RPHASE	RFRLEN2							RWDLEN2			RREVERSE		RESERVED		RDATDLY
R-0																RW-0	RW-0							RW-0			RW-0		R-0		RW-0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	RPHASE	Receive Phases 0x0: Single-phase frame 0x1: Dual-phase frame	RW	0
14:8	RFRLEN2	Receive Frame Length 2 Single-phase frame selected: RFRLEN2=don't care Dual-phase frame selected: RFRLEN2=000 0000 - 1 word per second phase (other values are reserved)	RW	0x00

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Bits	Field Name	Description	Type	Reset
7:5	RWDLEN2	Receive Word Length 2 0x0: 8 bits 0x1: 12 bits 0x2: 16 bits 0x3: 20 bits 0x4: 24 bits 0x5: 32 bits 0x6: Reserved (do not use) 0x7: Reserved (do not use)	RW	0x0
4:3	RREVERSE	Receive reverse mode. 0x0: Data transfer starts with MSB first. 0x1: Data transfer starts with LSB first. 0x2: Reserved (do not use) 0x3: Reserved (do not use)	RW	0x0
2	RESERVED	Reserved	R	0
1:0	RDATDLY	Receive Data Delay 0x0: 0-bit data delay 0x1: 1-bit data delay 0x2: 2-bit data delay 0x3: Reserved	RW	0x0

Table 23-376. Register Call Summary for Register MCBSPLP_RCR2_REG

Multichannel Buffered Serial Port (MCBSP)

- Words or Channels: [0]
- Frames: [1] [2]
- Bit Reordering (Option to Transfer LSB First): [3]
- Serial Words: [4]
- Frames and Frame Synchronization: [5]
- Number of Phases, Words, and Bits per Frame: [6] [7] [8] [9]
- Single-Phase Frame Example: [10] [11] [12]
- Dual-Phase Frame Example: [13] [14] [15]
- MCBSP Reception: [16]
- MCBSP Data Transfer Mode: [17]
- Preventing Unexpected Receive Frame-Sync Pulses: [18]
- Configuring a Frame for Multichannel Selection: [19]
- MCBSP Initialization Procedure: [20] [21]
- Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2): [22] [23] [24] [25] [26]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [27]
- MCBSP Register Summary: [28] [29] [30]

Table 23-377. MCBSPLP_RCR1_REG

Address Offset	0x0000 001C		
Physical Address	0x4902 201C 0x4012 201C 0x2 201C 0x4902 401C 0x4012 401C 0x2 401C 0x4902 601C 0x4012 601C 0x2 601C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP receive control register 1		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RFRLEN1								RWDLEN1			RESERVED				

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14:8	RFRLEN1	Receive Frame Length 1 Single-phase frame selected: RFRLEN1=000 0000 - 1 word per frame RFRLEN1=000 0001 - 2 words per frame RFRLEN1=111 1111 - 128 words per frame Dual-phase frame selected: RFRLEN1=000 0000 - 1 word per phase (other values are reserved)	RW	0x00
7:5	RWDLEN1	Receive Word Length 1 0x0: 8 bits 0x1: 12 bits 0x2: 16 bits 0x3: 20 bits 0x4: 24 bits 0x5: 32 bits 0x6: Reserved (do not use) 0x7: Reserved (do not use)	RW	0x0
4:0	RESERVED	Reserved	R	0x00

Table 23-378. Register Call Summary for Register MCBSPLP_RCR1_REG

Multichannel Buffered Serial Port (MCBSP)

- Words or Channels: [0]
- Frames: [1]
- Serial Words: [2]
- Frames and Frame Synchronization: [3]
- Number of Phases, Words, and Bits per Frame: [4] [5] [6]
- Single-Phase Frame Example: [7] [8]
- Dual-Phase Frame Example: [9] [10]
- Configuring a Frame for Multichannel Selection: [11]
- MCBSP Initialization Procedure: [12] [13]
- Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2): [14] [15]
- MCBSP Register Summary: [16] [17] [18]

Table 23-379. MCBSPLP_XCR2_REG

Address Offset	0x0000 0020		
Physical Address	0x4902 2020 0x4012 2020 0x2 2020 0x4902 4020 0x4012 4020 0x2 4020 0x4902 6020 0x4012 6020 0x2 6020	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit control register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XPHASE	XFRLEN2							XWDLEN2			XREVERSE		RESERVED		XDATDLY

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	XPHASE	Transmit Phases	RW	0
		0x0: Single-phase frame		
		0x1: Dual-phase frame		
14:8	XFRLEN2	Transmit Frame Length 2 Single-phase frame selected: XFRLEN2=don't care Dual-phase frame selected: XFRLEN2=000 0000 - 1 word per second phase (other values are reserved)	RW	0x00
7:5	XWDLEN2	Transmit Word Length 2	RW	0x0
		0x0: 8 bits		
		0x1: 12 bits		
		0x2: 16 bits		
		0x3: 20 bits		
		0x4: 24 bits		
		0x5: 32 bits		
		0x6: Reserved (do not use)		
		0x7: Reserved (do not use)		
4:3	XREVERSE	Transmit reverse mode.	RW	0x0
		0x0: Data transfer starts with MSB first.		
		0x1: Data transfer starts with LSB first.		
		0x2: Reserved (do not use)		
		0x3: Reserved (do not use)		
2	RESERVED	Reserved	R	0
1:0	XDATDLY	Transmit Data Delay	RW	0x0
		0x0: 0-bit data delay		
		0x1: 1-bit data delay		
		0x2: 2-bit data delay		
		0x3: Reserved		

Table 23-380. Register Call Summary for Register MCBSPLP_XCR2_REG

Multichannel Buffered Serial Port (MCBSP)

- Words or Channels: [0]
- Frames: [1] [2]
- Bit Reordering (Option to Transfer LSB First): [3]
- Serial Words: [4]
- Frames and Frame Synchronization: [5]
- Maximum Frame Frequency: [6]
- Number of Phases, Words, and Bits per Frame: [7] [8] [9] [10]
- Single-Phase Frame Example: [11] [12] [13]
- Dual-Phase Frame Example: [14] [15] [16]
- MCBSP Transmission: [17]
- MCBSP Data Transfer Mode: [18]
- Preventing Unexpected Transmit Frame-Sync Pulses: [19]
- Configuring a Frame for Multichannel Selection: [20]
- MCBSP Initialization Procedure: [21] [22]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [23] [24] [25] [26]
- MCBSP Register Summary: [27] [28] [29]

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Table 23-381. MCBSPLP_XCR1_REG

Address Offset	0x0000 0024		
Physical Address	0x4902 2024 0x4012 2024 0x2 2024 0x4902 4024 0x4012 4024 0x2 4024 0x4902 6024 0x4012 6024 0x2 6024	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit control register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XFRLEN1								XWDLEN1			RESERVED				

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14:8	XFRLEN1	Transmit Frame Length 1 Single-phase frame selected: XFRLEN1=000 0000 - 1 word per frame XFRLEN1=000 0001 - 2 words per frame XFRLEN1=111 1111 - 128 words per frame Dual-phase frame selected: XFRLEN1=000 0000 - 1 word per phase (other values are reserved)	RW	0x00
7:5	XWDLEN1	Transmit Word Length 1 0x0: 8 bits 0x1: 12 bits 0x2: 16 bits 0x3: 20 bits 0x4: 24 bits 0x5: 32 bits 0x6: Reserved (do not use) 0x7: Reserved (do not use)	RW	0x0
4:0	RESERVED	Reserved	R	0x00

Table 23-382. Register Call Summary for Register MCBSPLP_XCR1_REG

Multichannel Buffered Serial Port (MCBSP)

- Words or Channels: [0]
- Frames: [1]
- Serial Words: [2]
- Frames and Frame Synchronization: [3]
- Number of Phases, Words, and Bits per Frame: [4] [5] [6]
- Single-Phase Frame Example: [7] [8]
- Dual-Phase Frame Example: [9] [10]
- Configuring a Frame for Multichannel Selection: [11]
- MCBSP Initialization Procedure: [12] [13]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [14] [15]
- MCBSP Register Summary: [16] [17] [18]

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Table 23-383. MCBSPLP_SRGR2_REG

Address Offset	0x0000 0028		
Physical Address	0x4902 2028	**Instance**	MCBSP1_L3
	0x4012 2028		MCBSP1_CORTEX-A15
	0x2 2028		MCBSP1_DSP
	0x4902 4028		MCBSP2_L3
	0x4012 4028		MCBSP2_CORTEX-A15
	0x2 4028		MCBSP2_DSP
	0x4902 6028		MCBSP3_L3
	0x4012 6028		MCBSP3_CORTEX-A15
	0x2 6028		MCBSP3_DSP
Description	MCBSPLP sample rate generator register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																GSYNC	CLKSP	CLKSM	FSGM	FPER											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	GSYNC	0x0: The SRG clock (CLKG) is free running. 0x1: The SRG clock (CLKG) is running. But CLKG is resynchronized and frame-sync signal (FSG) is generated only after detecting the receive frame-sync signal (FSR). Also, frame period, FPER, is a don't care because the period is dictated by the external frame-sync pulse.	RW	0
14	CLKSP	CLKS Polarity Clock Edge Select Only used when the external clock CLKS drives the SRG clock (CLKSM=0). 0x0: Rising edge of CLKG and FSG. 0x1: Falling edge of CLKG and FSG.	RW	0
13	CLKSM	MCBSPLP Sample Rate Generator Clock Mode 0x0: SCLKME=0: SRG clock derived from the CLKS pin. SCLKME=1: SRG clock derived from the CLKRI pin. 0x1: SCLKME=0: SRG clock derived from the CPU clock. SCLKME=1: SRG clock derived from the CLKXI clock.	RW	1
12	FSGM	Sample Rate Generator Transmit Frame-Synchronization Mode Used when FSXM=1 in the PCR. 0x0: Transmit frame-sync signal (FSX) is generated when transmit buffer is not empty When FSGM=0, FPER and FWID are used to determine the frame-sync period and width (external FSX is gated by the buffer empty condition). 0x1: Transmit frame-sync signal driven by the SRG frame-sync signal, FSG.	RW	0
11:0	FPER	Frame Period. This field plus 1 determines when the next frame-sync signal becomes active. Range: 1 to 4096 CLKG periods	RW	0x000

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Table 23-384. Register Call Summary for Register MCBSPLP_SRGR2_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP1 Clocks: [0]
- MCBSP2 Clocks: [1]
- MCBSP3 Clocks: [2]
- Clocking and Framing Data: [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- Frames and Frame Synchronization: [15]
- MCBSP SRG: [16] [17] [18]
- Frame-Sync Generation in the SRG: [19] [20]
- Controlling the Period Between the Starting Edges of Frame-Sync Pulses: [21]
- Synchronizing SRG Outputs to an External Clock: [22] [23]
- Operating the Transmitter Synchronously With the Receiver: [24] [25]
- Underflow in the Transmitter: [26] [27] [28]
- MCBSP Initialization Procedure: [29] [30]
- Reset and Initialization Procedure for the SRG: [31]
- Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2): [32] [33] [34] [35] [36]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [37] [38] [39] [40] [41]
- MCBSP Register Summary: [42] [43] [44]

Table 23-385. MCBSPLP_SRGR1_REG

Address Offset	0x0000 002C		
Physical Address	0x4902 202C	**Instance**	MCBSP1_L3
	0x4012 202C		MCBSP1_CORTEX-A15
	0x2 202C		MCBSP1_DSP
	0x4902 402C		MCBSP2_L3
	0x4012 402C		MCBSP2_CORTEX-A15
	0x2 402C		MCBSP2_DSP
	0x4902 602C		MCBSP3_L3
	0x4012 602C		MCBSP3_CORTEX-A15
	0x2 602C		MCBSP3_DSP
Description	MCBSPLP sample rate generator register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FWID								CLKGDV							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:8	FWID	Frame Width. This field plus 1 determines the width of the frame-sync pulse, FSG, during its active period. Range: 1 to 256 CLKG periods.	RW	0x00
7:0	CLKGDV	Sample Rate Generator Clock Divider This value is used as the divide-down number to generate the required SRG clock frequency. Default value is 1.	RW	0x01

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Table 23-386. Register Call Summary for Register MCBSPLP_SRGR1_REG

Multichannel Buffered Serial Port (MCBSP)

- Protocol: [0]
- Clocking: [1]
- MCBSP SRG: [2] [3] [4]
- Frame-Sync Generation in the SRG: [5]
- Choosing the Width of the Frame-Sync Pulse: [6]
- Underflow in the Transmitter: [7]
- MCBSP Initialization Procedure: [8] [9]
- Reset and Initialization Procedure for the SRG: [10]
- Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2): [11] [12]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [13] [14]
- MCBSP Register Summary: [15] [16] [17]

Table 23-387. MCBSPLP_MCR2_REG

Address Offset	0x0000 0030		
Physical Address	0x4902 2030	**Instance**	MCBSP1_L3
	0x4012 2030		MCBSP1_CORTEX-A15
	0x2 2030		MCBSP1_DSP
	0x4902 4030		MCBSP2_L3
	0x4012 4030		MCBSP2_CORTEX-A15
	0x2 4030		MCBSP2_DSP
	0x4902 6030		MCBSP3_L3
	0x4012 6030		MCBSP3_CORTEX-A15
	0x2 6030		MCBSP3_DSP
Description	MCBSPLP multi channel register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						XMCME	XPBBLK	XPABLK	RESERVED						XMCM	

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9	XMCME	0x0: 2-partition mode: Only partitions A and B are used. You can control up to 32 channels in the transmit multichannel selection mode selected with the XMCM bits. If XMCM = 01b or 10b, assign 16 channels to partition A with the XPABLK bits. Assign 16 channels to partition B with the XPBBLK bits. If XMCM = 11b (for symmetric transmission and reception), assign 16 channels to receive partition A with the RPABLK bits. Assign 16 channels to receive partition B with the RPBBLK bits. You control the channels with the appropriate transmit channel enable registers: XCERA: Channels in partition A XCERB: Channels in partition B 0x1: 8-partition mode: All partitions (A through H) are used. You can control up to 128 channels in the transmit multichannel selection mode selected with the XMCM bits. You control the channels with the appropriate transmit channel enable registers: XCERA: Channels 0 through 15 XCERB: Channels 16 through 31 XCERC: Channels 32 through 47 XCERD: Channels 48 through 63 XCERE: Channels 64 through 79 XCERF: Channels 80 through 95 XCERG: Channels 96 through 111 XCERH: Channels 112 through 127	RW	0

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Bits	Field Name	Description	Type	Reset
8:7	XPBBLK	Transmit Partition B Block (legacy) 0x0: Block 1. Channel 16 to channel 31 0x1: Block 3. Channel 48 to channel 63 0x2: Block 5. Channel 80 to channel 95 0x3: Block 7. Channel 112 to channel 127	RW	0x0
6:5	XPABLK	Transmit Partition A Block (legacy) 0x0: Block 0. Channel 0 to channel 15 0x1: Block 2. Channel 32 to channel 47 0x2: Block 4. Channel 64 to channel 79 0x3: Block 6. Channel 96 to channel 111	RW	0x0
4:2	RESERVED	Reserved	R	0x0
1:0	XMCM	Transmit Multichannel Selection Enable 0x0: All channels enabled without masking (DX is always driven during transmission of data). 0x1: All channels disabled and therefore masked by default. Required channels are selected by enabling XP(A/B)BLK and XCER(A/B) appropriately. Also, these selected channels are not masked and therefore DX is always driven. 0x2: All channels enabled, but masked. Selected channels enabled via XP(A/B)BLK and XCER(A/B) are unmasked. 0x3: All channels disabled and therefore masked by default. Required channels are selected by enabling RP(A/B)BLK and RCER(A/B) appropriately. Selected channels can be unmasked by RP(A/B)BLK and XCER(A/B). This mode is used for symetric transmit and receive operation.	RW	0x0

Table 23-388. Register Call Summary for Register MCBSPLP_MCR2_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0] [1] [2]
- Using Two Partitions (Legacy Only): [3] [4]
- Transmit Multichannel Selection Modes: [5] [6] [7] [8]
- Activity on MCBSP Pins for Different Values of XMCM: [9] [10]
- MCBSP Initialization Procedure: [11]
- MCBSP Register Summary: [12] [13] [14]

Table 23-389. MCBSPLP_MCR1_REG

Address Offset	0x0000 0034		
Physical Address	0x4902 2034 0x4012 2034 0x2 2034 0x4902 4034 0x4012 4034 0x2 4034 0x4902 6034 0x4012 6034 0x2 6034	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP multi channel register 1		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						RMCME	RPBBLK	RPABLK			RESERVED				RMCM

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9	RMCME	(legacy) 0x0: 2-partition mode. Only partitions A and B are used. You can control up to 32 channels in the receive multichannel selection mode (RMCM = 1). Assign 16 channels to partition A with the RPABLK bits. Assign 16 channels to partition B with the RPBBLK bits. You control the channels with the apropriate receive channel enable registers: RCERA: Channels in partition A RCERB: Channels in partition B 0x1: 8-partition mode: All partitions (A through H) are used. You can control up to 128 channels in the receive multichannel selection mode. You control the channels with the appropriate receive channel enable registers: RCERA: Channels 0 through 15 RCERB: Channels 16 through 31 RCERC: Channels 32 through 47 RCERD: Channels 48 through 63 RCERE: Channels 64 through 79 RCERF: Channels 80 through 95 RCERG: Channels 96 through 111 RCERH: Channels 112 through 127	RW	0
8:7	RPBBLK	Receive Partition B Block (legacy) 0x0: Block 1. Channel 16 to channel 31 0x1: Block 3. Channel 48 to channel 63 0x2: Block 5. Channel 80 to channel 95 0x3: Block 7. Channel 112 to channel 127	RW	0x0
6:5	RPABLK	Receive Partition A Block (legacy) 0x0: Block 0. Channel 0 to channel 15 0x1: Block 2. Channel 32 to channel 47 0x2: Block 4. Channel 64 to channel 79 0x3: Block 6. Channel 96 to channel 111	RW	0x0
4:1	RESERVED	Reserved	R	0x0
0	RMCM	Receive Multichannel Selection Enable 0x0: All 128 channels 0x1: All channels disabled by default. Required channels are selected by enabling RP(A/B)BLK and RCER(A/B) appropriately	RW	0

Table 23-390. Register Call Summary for Register MCBSPLP_MCR1_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0] [1] [2]
- Receive Multichannel Selection Mode: [3] [4]
- Using Two Partitions (Legacy Only): [5] [6] [7] [8]
- MCBSP Initialization Procedure: [9]
- Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2): [10]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [11]
- MCBSP Register Summary: [12] [13] [14]

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Table 23-391. MCBSPLP_RCERA_REG

Address Offset	0x0000 0038		
Physical Address	0x4902 2038 0x4012 2038 0x2 2038 0x4902 4038 0x4012 4038 0x2 4038 0x4902 6038 0x4012 6038 0x2 6038	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP receive channel enable register partition A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERA															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERA	Receive Channel Enable RCERA n=0 Disables reception of n-th channel in an even-numbered block in partition A RCERA n=1 Enables reception of n-th channel in an even-numbered block in partition A	RW	0x0000

Table 23-392. Register Call Summary for Register MCBSPLP_RCERA_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- Receive Multichannel Selection Mode: [1] [2]
- Using Two Partitions (Legacy Only): [3]
- Transmit Multichannel Selection Modes: [4] [5]
- MCBSP Register Summary: [6] [7] [8]

Table 23-393. MCBSPLP_RCERB_REG

Address Offset	0x0000 003C		
Physical Address	0x4902 203C 0x4012 203C 0x2 203C 0x4902 403C 0x4012 403C 0x2 403C 0x4902 603C 0x4012 603C 0x2 603C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP receive channel enable register partition B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERB															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERB	Receive Channel Enable RCERB n=0 Disables reception of n-th channel in a even-numbered block in partition B RCERB n=1 Enables reception of n-th channel in a even-numbered block in partition B	RW	0x0000

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Table 23-394. Register Call Summary for Register MCBSPLP_RCERB_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- Using Two Partitions (Legacy Only): [1]
- MCBSP Register Summary: [2] [3] [4]

Table 23-395. MCBSPLP_XCERA_REG

Address Offset	0x0000 0040		
Physical Address	0x4902 2040 0x4012 2040 0x2 2040 0x4902 4040 0x4012 4040 0x2 4040 0x4902 6040 0x4012 6040 0x2 6040	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit channel enable register partition A		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERA															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERA	Transmit Channel Enable XCERA n=0 Disables transmission of n-th channel in an event-numbered block in partition A XCERA n=1 Enables transmission of n-th channel in an event-numbered block in partition A	RW	0x0000

Table 23-396. Register Call Summary for Register MCBSPLP_XCERA_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- Using Two Partitions (Legacy Only): [1]
- Transmit Multichannel Selection Modes: [2] [3] [4] [5] [6] [7]
- MCBSP Register Summary: [8] [9] [10]

Table 23-397. MCBSPLP_XCERB_REG

Address Offset	0x0000 0044		
Physical Address	0x4902 2044 0x4012 2044 0x2 2044 0x4902 4044 0x4012 4044 0x2 4044 0x4902 6044 0x4012 6044 0x2 6044	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit channel enable register partition B		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERB															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERB	Transmit Channel Enable XCERB n=0 Disables transmission of n-th channel in an even-numbered block in partition B XCERB n=1 Enables transmission of n-th channel in an even-numbered block in partition B	RW	0x0000

Table 23-398. Register Call Summary for Register MCBSPLP_XCERB_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- Using Two Partitions (Legacy Only): [1]
- MCBSP Register Summary: [2] [3] [4]

Table 23-399. MCBSPLP_PCR_REG

Address Offset	0x0000 0048		
Physical Address	0x4902 2048 0x4012 2048 0x2 2048 0x4902 4048 0x4012 4048 0x2 4048 0x4902 6048 0x4012 6048 0x2 6048	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP pin control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																IDLE_EN	XIOEN	RIOEN	FSXM	FSRM	CLKXM	CLKRM	SCLKME	CLKS_STAT	DX_STAT	DR_STAT	FSXP	FSRP	CLKXP	CLKRP	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	IDLE_EN	Idle enable. This bit allows stopping all the clocks in the MCBSPLP. (legacy) 0x0: The MCBSP is running 0x1: The clocks in the MCBSP are shut off when both IDLE_EN=1 and peripheral domain is in idle mode	RW	0
13	XIOEN	Transmit General Purpose I/O Mode only when XRST=0 in SPCR[1,2] (legacy) 0x0: DX, FSX and CLKX are configured as serial port pins and do not function as general-purpose I/Os. 0x1: DX pin is a general purpose output. FSX and CLKX are general purpose I/Os. These serial port pins do not perform serial port operation.	RW	0
12	RIOEN	Receive General Purpose I/O Mode when RRST=0 in SPCR[1,2] (legacy) 0x0: DR, FSR, CLKR and CLKS are configured as serial port pins and do not function as general-purpose I/Os. 0x1: DR and CLKS pins are general purpose inputs; FSR and CLKR are general purpose I/Os. These serial port pins do not perform serial port operation. The CLKS pin is affected by a combination of RRST and RIOEN signals of the receiver.	RW	0

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Bits	Field Name	Description	Type	Reset
11	FSXM	Transmit Frame-Synchronization Mode 0x0: Frame-sync signal derived from an external source 0x1: Frame synchronization is determined by the SRG frame-sync mode bit FSGM in SRGR2.	RW	0
10	FSRM	Receive Frame-Synchronization Mode 0x0: Frame-sync pulses generated by an external device. FSR is an input pin. 0x1: Frame synchronization generated internally by SRG. FSR is an output pin except when GSYNC=1 in SRGR.	RW	0
9	CLKXM	Transmitter Clock Mode 0x0: Transmitter clock is driven by an external clock with CLKX as an input pin. 0x1: CLKX is an output pin and is driven by the internal sample rate generator.	RW	0
8	CLKRM	Receiver Clock Mode 0x0: Case 1: Digital loopback mode not set (DLB=0) in SPCR1: Receive clock (CLKR) is an input driven by an externaal clock. Case 2: Digital loopback mode set (DLB=1) in SPCR1: Receive clock (not the CLKR pin) is driven by transmit clock (CLKX) which is based on the CLKXM bit in the PCR. CLKR pin is in high-impedance. 0x1: Case 1: Digital loopback mode not set (DLB=0) in SPCR1: CLKR is an output pin and is driven by the internal SRG. Case 2: Digital loopback mode set (DLB=1) in SPCR1: CLKR is an output pin and is driven by the transmit clock. The transmit clock is derived based on the CLKRM bit in the PCR.	RW	0
7	SCLKME	The frequency of CLKG is: CLKG frequency = (Input clock frequency) / (CLKGDV + 1) SCLKME is used in conjunction with the CLKSM bit to select the input clock: 0x0: CLKSM = 0: Signal on CLKS pin CLKSM = 1: CPU clock 0x1: CLKSM = 0: Signal on CLKR pin CLKSM = 1: Signal on CLKX pin	RW	0
6	CLKS_STAT	CLKS pin status. Reflects value on CLKS pin when selected as a general purpose input. (legacy) Read 0x0: The signal on the CLKS pin is low Read 0x1: The signal on the CLKS pin is high	R	0
5	DX_STAT	DX pin status. Reflects value driven on to DX pin when selected as a general purpose output. (legacy) 0x0: Drive the signal on the DX pin low 0x1: Drive the signal on the DX pin high	RW	0
4	DR_STAT	DR pin status. Reflects value on DR pin when selected as a general purpose input. (legacy) Read 0x0: The signal on DR pin is low Read 0x1: The signal on DR pin is high	R	0
3	FSXP	Transmit Frame-Synchronization Polarity 0x0: Frame-sync pulse FSX is active high 0x1: Frame-sync pulse FSX is active low	RW	0
2	FSRP	Receive Frame-Synchronization Polarity 0x0: Frame-sync pulse FSR is active high 0x1: Frame-sync pulse FSR is active low	RW	0
1	CLKXP	Transmit Clock Polarity 0x0: Transmit data driven on rising edge of CLKX 0x1: Transmit data driven on falling edge of CLKX	RW	0

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Bits	Field Name	Description	Type	Reset
0	CLKRP	Receive Clock Polarity 0x0: Receive data sampled on falling edge of CLKR 0x1: Receive data sampled on rising edge of CLKR	RW	0

Table 23-400. Register Call Summary for Register MCBSPLP_PCR_REG

Multichannel Buffered Serial Port (MCBSP)

- Words or Channels: [0]
- Frames: [1]
- MCBSP1 Clocks: [2]
- MCBSP2 Clocks: [3]
- MCBSP3 Clocks: [4]
- Analysis of the Receiver Smart-Idle Behavior: [5] [6]
- Clocking and Framing Data: [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
- Clocking: [21] [22] [23] [24] [25] [26] [27]
- Frames and Frame Synchronization: [28] [29] [30] [31] [32] [33] [34]
- Detecting Frame-Sync Pulses, Even in Reset State: [35] [36] [37] [38]
- Single-Phase Frame Example: [39] [40] [41] [42]
- Dual-Phase Frame Example: [43] [44] [45] [46]
- MCBSP Data Transfer Mode: [47] [48]
- MCBSP SRG: [49] [50] [51] [52] [53]
- Clock Generation in the SRG: [54] [55] [56] [57]
- Frame-Sync Generation in the SRG: [58] [59]
- Operating the Transmitter Synchronously With the Receiver: [60] [61] [62] [63]
- Underflow in the Transmitter: [64]
- MCBSP Initialization Procedure: [65] [66]
- Reset and Initialization Procedure for the SRG: [67]
- Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2): [68] [69] [70] [71] [72] [73] [74] [75]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [76] [77] [78] [79] [80] [81] [82] [83]
- GPIO on the MCBSP Pins (Legacy Only): [84] [85] [86] [87]
- MCBSP Register Summary: [88] [89] [90]

Table 23-401. MCBSPLP_RCERC_REG

Address Offset	0x0000 004C		
Physical Address	0x4902 204C 0x4012 204C 0x2 204C 0x4902 404C 0x4012 404C 0x2 404C 0x4902 604C 0x4012 604C 0x2 604C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP receive channel enable register partition C		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERC															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERC	Receive Channel Enable RCERC n=0 Disables reception of n-th channel in an even-numbered block in partition C RCERC n=1 Enables reception of n-th channel in an even-numbered block in partition C	RW	0x0000

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Table 23-402. Register Call Summary for Register MCBSPLP_RCERC_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

Table 23-403. MCBSPLP_RCERD_REG

Address Offset	0x0000 0050		
Physical Address	0x4902 2050	**Instance**	MCBSP1_L3
	0x4012 2050		MCBSP1_CORTEX-A15
	0x2 2050		MCBSP1_DSP
	0x4902 4050		MCBSP2_L3
	0x4012 4050		MCBSP2_CORTEX-A15
	0x2 4050		MCBSP2_DSP
	0x4902 6050		MCBSP3_L3
	0x4012 6050		MCBSP3_CORTEX-A15
	0x2 6050		MCBSP3_DSP
Description	MCBSPLP receive channel enable register partition D		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERD															
R-0																RW-0															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERD	Receive Channel Enable RCERD n=0 Disables reception of n-th channel in an even-numbered block in partition D RCERD n=1 Enables reception of n-th channel in an even-numbered block in partition D	RW	0x0000

Table 23-404. Register Call Summary for Register MCBSPLP_RCERD_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

Table 23-405. MCBSPLP_XCERC_REG

Address Offset	0x0000 0054		
Physical Address	0x4902 2054	**Instance**	MCBSP1_L3
	0x4012 2054		MCBSP1_CORTEX-A15
	0x2 2054		MCBSP1_DSP
	0x4902 4054		MCBSP2_L3
	0x4012 4054		MCBSP2_CORTEX-A15
	0x2 4054		MCBSP2_DSP
	0x4902 6054		MCBSP3_L3
	0x4012 6054		MCBSP3_CORTEX-A15
	0x2 6054		MCBSP3_DSP
Description	MCBSPLP transmit channel enable register partition C		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERC															
R-0																RW-0															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERC	Transmit Channel Enable XCERC n=0 Disables transmission of n-th channel in an event-numbered block in partition C XCERC n=1 Enables transmission of n-th channel in an event-numbered block in partition C	RW	0x0000

Table 23-406. Register Call Summary for Register MCBSPLP_XCERC_REG

Multichannel Buffered Serial Port (MCBSP)
- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

Table 23-407. MCBSPLP_XCERD_REG

Address Offset	0x0000 0058		
Physical Address	0x4902 2058	**Instance**	MCBSP1_L3
	0x4012 2058		MCBSP1_CORTEX-A15
	0x2 2058		MCBSP1_DSP
	0x4902 4058		MCBSP2_L3
	0x4012 4058		MCBSP2_CORTEX-A15
	0x2 4058		MCBSP2_DSP
	0x4902 6058		MCBSP3_L3
	0x4012 6058		MCBSP3_CORTEX-A15
	0x2 6058		MCBSP3_DSP
Description	MCBSPLP transmit channel enable register partition D		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERD															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERD	Transmit Channel Enable XCERD n=0 Disables transmission of n-th channel in an even-numbered block in partition D XCERD n=1 Enables transmission of n-th channel in an even-numbered block in partition D	RW	0x0000

Table 23-408. Register Call Summary for Register MCBSPLP_XCERD_REG

Multichannel Buffered Serial Port (MCBSP)
- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

Table 23-409. MCBSPLP_RCERE_REG

Address Offset	0x0000 005C		
Physical Address	0x4902 205C	**Instance**	MCBSP1_L3
	0x4012 205C		MCBSP1_CORTEX-A15
	0x2 205C		MCBSP1_DSP
	0x4902 405C		MCBSP2_L3
	0x4012 405C		MCBSP2_CORTEX-A15
	0x2 405C		MCBSP2_DSP
	0x4902 605C		MCBSP3_L3
	0x4012 605C		MCBSP3_CORTEX-A15
	0x2 605C		MCBSP3_DSP
Description	MCBSPLP receive channel enable register partition E		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERE	Receive Channel Enable RCERE n=0 Disables reception of n-th channel in an even-numbered block in partition E RCERE n=1 Enables reception of n-th channel in an even-numbered block in partition E	RW	0x0000

Table 23-410. Register Call Summary for Register MCBSPLP_RCERE_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

Table 23-411. MCBSPLP_RCERF_REG

Address Offset	0x0000 0060		
Physical Address	0x4902 2060 0x4012 2060 0x2 2060 0x4902 4060 0x4012 4060 0x2 4060 0x4902 6060 0x4012 6060 0x2 6060	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP receive channel enable register partition F		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERF															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERF	Receive Channel Enable RCERF n=0 Disables reception of n-th channel in an even-numbered block in partition F RCERF n=1 Enables reception of n-th channel in an even-numbered block in partition F	RW	0x0000

Table 23-412. Register Call Summary for Register MCBSPLP_RCERF_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

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Table 23-413. MCBSPLP_XCERE_REG

Address Offset	0x0000 0064		
Physical Address	0x4902 2064 0x4012 2064 0x2 2064 0x4902 4064 0x4012 4064 0x2 4064 0x4902 6064 0x4012 6064 0x2 6064	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit channel enable register partition E		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERE	Transmit Channel Enable XCERE n=0 Disables transmission of n-th channel in an event-numbered block in partition E XCERE n=1 Enables transmission of n-th channel in an event-numbered block in partition E	RW	0x0000

Table 23-414. Register Call Summary for Register MCBSPLP_XCERE_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

Table 23-415. MCBSPLP_XCERF_REG

Address Offset	0x0000 0068		
Physical Address	0x4902 2068 0x4012 2068 0x2 2068 0x4902 4068 0x4012 4068 0x2 4068 0x4902 6068 0x4012 6068 0x2 6068	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit channel enable register partition F		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERF															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERF	Transmit Channel Enable XCERF n=0 Disables transmission of n-th channel in an even-numbered block in partition F XCERF n=1 Enables transmission of n-th channel in an even-numbered block in partition F	RW	0x0000

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Table 23-416. Register Call Summary for Register MCBSPLP_XCERF_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

Table 23-417. MCBSPLP_RCERG_REG

Address Offset	0x0000 006C		
Physical Address	0x4902 206C 0x4012 206C 0x2 206C 0x4902 406C 0x4012 406C 0x2 406C 0x4902 606C 0x4012 606C 0x2 606C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP receive channel enable register partition G		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERG															
R-0																RW-0															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERG	Receive Channel Enable RCERG n=0 Disables reception of n-th channel in an even-numbered block in partition G RCERG n=1 Enables reception of n-th channel in an even-numbered block in partition G	RW	0x0000

Table 23-418. Register Call Summary for Register MCBSPLP_RCERG_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

Table 23-419. MCBSPLP_RCERH_REG

Address Offset	0x0000 0070		
Physical Address	0x4902 2070 0x4012 2070 0x2 2070 0x4902 4070 0x4012 4070 0x2 4070 0x4902 6070 0x4012 6070 0x2 6070	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP receive channel enable register partition H		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RCERH															
R-0																RW-0															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	RCERH	Receive Channel Enable RCERH n=0 Disables reception of n-th channel in an even-numbered block in partition H RCERH n=1 Enables reception of n-th channel in an even-numbered block in partition H	RW	0x0000

Table 23-420. Register Call Summary for Register MCBSPLP_RCERH_REG

Multichannel Buffered Serial Port (MCBSP)
- Using Eight Partitions: [0]
- Receive Multichannel Selection Mode: [1] [2]
- Transmit Multichannel Selection Modes: [3] [4]
- MCBSP Register Summary: [5] [6] [7]

Table 23-421. MCBSPLP_XCERG_REG

Address Offset	0x0000 0074		
Physical Address	0x4902 2074 0x4012 2074 0x2 2074 0x4902 4074 0x4012 4074 0x2 4074 0x4902 6074 0x4012 6074 0x2 6074	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit channel enable register partition G		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERG															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERG	Transmit Channel Enable XCERG n=0 Disables transmission of n-th channel in an event-numbered block in partition G XCERG n=1 Enables transmission of n-th channel in an event-numbered block in partition G	RW	0x0000

Table 23-422. Register Call Summary for Register MCBSPLP_XCERG_REG

Multichannel Buffered Serial Port (MCBSP)
- Using Eight Partitions: [0]
- MCBSP Register Summary: [1] [2] [3]

Table 23-423. MCBSPLP_XCERH_REG

Address Offset	0x0000 0078		
Physical Address	0x4902 2078 0x4012 2078 0x2 2078 0x4902 4078 0x4012 4078 0x2 4078 0x4902 6078 0x4012 6078 0x2 6078	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit channel enable register partition H		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XCERH															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	XCERH	Transmit Channel Enable XCERH n=0 Disables transmission of n-th channel in an even-numbered block in partition H XCERH n=1 Enables transmission of n-th channel in an even-numbered block in partition H	RW	0x0000

Table 23-424. Register Call Summary for Register MCBSPLP_XCERH_REG

Multichannel Buffered Serial Port (MCBSP)

- Using Eight Partitions: [0]
- Transmit Multichannel Selection Modes: [1] [2] [3] [4] [5] [6]
- MCBSP Register Summary: [7] [8] [9]

Table 23-425. MCBSPLP_REV_REG

Address Offset	0x0000 007C		
Physical Address	0x4902 207C 0x4012 207C 0x2 207C 0x4902 407C 0x4012 407C 0x2 407C 0x4902 607C 0x4012 607C 0x2 607C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP Revision number register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REV							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	REV	Revision number	R	0x11

Table 23-426. Register Call Summary for Register MCBSPLP_REV_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP Register Summary: [0] [1] [2]

Table 23-427. MCBSPLP_RINTCLR_REG

Address Offset	0x0000 0080		
Physical Address	0x4902 2080 0x4012 2080 0x2 2080 0x4902 4080 0x4012 4080 0x2 4080 0x4902 6080 0x4012 6080 0x2 6080	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP receive interrupt clear		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RINTCLR																															

Bits	Field Name	Description	Type	Reset
31:0	RINTCLR	Read from this register will clear the IRQ generated by receive end-of-frame indication or MCBSPLP.FSR detection. Write to this register has no effect. (legacy)	RW	0x0000 0000

Table 23-428. Register Call Summary for Register MCBSPLP_RINTCLR_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP Register Summary: [0] [1] [2]

Table 23-429. MCBSPLP_XINTCLR_REG

Address Offset	0x0000 0084		
Physical Address	0x4902 2084	**Instance**	MCBSP1_L3
	0x4012 2084		MCBSP1_CORTEX-A15
	0x2 2084		MCBSP1_DSP
	0x4902 4084		MCBSP2_L3
	0x4012 4084		MCBSP2_CORTEX-A15
	0x2 4084		MCBSP2_DSP
	0x4902 6084		MCBSP3_L3
	0x4012 6084		MCBSP3_CORTEX-A15
	0x2 6084		MCBSP3_DSP
Description	MCBSPLP transmit interrupt clear (legacy)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XINTCLR																															

Bits	Field Name	Description	Type	Reset
31:0	XINTCLR	Read from this register will clear the IRQ generated by transmit end-of-frame indication or MCBSPLP.FSX detection. Write to this register has no effect.	RW	0x0000 0000

Table 23-430. Register Call Summary for Register MCBSPLP_XINTCLR_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP Register Summary: [0] [1] [2]

Table 23-431. MCBSPLP_ROVFLCLR_REG

Address Offset	0x0000 0088		
Physical Address	0x4902 2088	**Instance**	MCBSP1_L3
	0x4012 2088		MCBSP1_CORTEX-A15
	0x2 2088		MCBSP1_DSP
	0x4902 4088		MCBSP2_L3
	0x4012 4088		MCBSP2_CORTEX-A15
	0x2 4088		MCBSP2_DSP
	0x4902 6088		MCBSP3_L3
	0x4012 6088		MCBSP3_CORTEX-A15
	0x2 6088		MCBSP3_DSP
Description	MCBSPLP receive overflow interrupt clear		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROVFLCLR																															

Bits	Field Name	Description	Type	Reset
31:0	ROVFLCLR	Read from this register will clear the IRQ generated by the receive overflow condition. Write to this register has no effect.	RW	0x0000 0000

Table 23-432. Register Call Summary for Register MCBSPLP_ROVFLCLR_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP Register Summary: [0] [1] [2]

Table 23-433. MCBSPLP_SYSCONFIG_REG

Address Offset	0x0000 008C		
Physical Address	0x4902 208C 0x4012 208C 0x2 208C 0x4902 408C 0x4012 408C 0x2 408C 0x4902 608C 0x4012 608C 0x2 608C	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP System Configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						CLOCKACTIVITY		RESERVED			SIDLEMODE		ENAWAKEUP	SOFTRESET	RESERVED

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved	R	0x000000
9:8	CLOCKACTIVITY	0x0: The MCBSPi_ICLK clock can be switched off. The PRCM functional clock can be switched off. 0x1: The MCBSPi_ICLK clock must be maintained during wakeup. The PRCM functional clock can be switched off. 0x2: The MCBSPi_ICLK clock can be switched off. The PRCM functional clock must be maintained during wakeup. 0x3: The MCBSPi_ICLK clock must be maintained during wakeup. The PRCM functional clock must be maintained during wakeup	RW	0x0
7:5	RESERVED	Reserved	R	0x0
4:3	SIDLEMODE	Slave interface power management, req/ack control: 0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged. 0x2: Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
2	ENAWAKEUP	WakeUp feature control: 0x0: WakeUp is disabled 0x1: WakeUp capability is enabled	RW	0
1	SOFTRESET	MCBSPLP global software reset 0x0: NO soft reset 0x1: Soft reset triggered	RW	0
0	RESERVED	Reserved	R	0

Table 23-434. Register Call Summary for Register MCBSPLP_SYSCONFIG_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP Software Reset: [0]
- MCBSP Acknowledgment Modes: [1] [2] [3] [4]
- Wake-Up Capability: [5]
- Analysis of the Receiver Smart-Idle Behavior: [6]
- MCBSP Initialization Procedure: [7]
- MCBSP Register Summary: [8] [9] [10]

Table 23-435. MCBSPLP_THRSH2_REG

Address Offset	0x0000 0090		
Physical Address	0x4902 2090 0x4012 2090 0x2 2090 0x4902 4090 0x4012 4090 0x2 4090 0x4902 6090 0x4012 6090 0x2 6090	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit buffer threshold (DMA or IRQ trigger)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XTHRESHOLD							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	XTHRESHOLD	Transmit buffer threshold value. The DMA request (if enabled) of interrupt assertion (if enabled) will be triggered if the number of free locations inside transmit buffer are above or equal to the XTHRESHOLD value + 1. Also, this value (XTHRESHOLD value + 1) indicates the number of words transferred during a transmit data DMA request, if transmit DMA is enabled	RW	0x00

Table 23-436. Register Call Summary for Register MCBSPLP_THRSH2_REG

Multichannel Buffered Serial Port (MCBSP)

- Transmit Wakeup: [0]
- MCBSP Transmission: [1]
- MCBSP DMA Configuration: [2]
- MCBSP Initialization Procedure: [3]
- Data Transfer DMA Request Configuration: [4]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [5]
- MCBSP Register Summary: [6] [7] [8]

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Table 23-437. MCBSPLP_THRSH1_REG

Address Offset	0x0000 0094		
Physical Address	0x4902 2094	**Instance**	MCBSP1_L3
	0x4012 2094		MCBSP1_CORTEX-A15
	0x2 2094		MCBSP1_DSP
	0x4902 4094		MCBSP2_L3
	0x4012 4094		MCBSP2_CORTEX-A15
	0x2 4094		MCBSP2_DSP
	0x4902 6094		MCBSP3_L3
	0x4012 6094		MCBSP3_CORTEX-A15
	0x2 6094		MCBSP3_DSP
Description	MCBSPLP receive buffer threshold (DMA or IRQ trigger)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RTHRESHOLD							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	RTHRESHOLD	Receive buffer threshold value. The DMA request (if enabled) of interrupt assertion (if enabled) will be triggered if the number of occupied locations inside receive buffer are above or equal to the RTHRESHOLD value + 1. Also, this value (RTHRESHOLD value + 1) indicates the number of words transferred during a receive data DMA request, if receive DMA is enabled.	RW	0x00

Table 23-438. Register Call Summary for Register MCBSPLP_THRSH1_REG

Multichannel Buffered Serial Port (MCBSP)

- Receive Wakeup: [0]
- MCBSP Reception: [1]
- MCBSP DMA Configuration: [2]
- Data Transfer DMA Request Configuration: [3]
- Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2): [4]
- MCBSP Register Summary: [5] [6] [7]

Table 23-439. MCBSPLP_IRQSTATUS_REG

Address Offset	0x0000 00A0		
Physical Address	0x4902 20A0	**Instance**	MCBSP1_L3
	0x4012 20A0		MCBSP1_CORTEX-A15
	0x2 20A0		MCBSP1_DSP
	0x4902 40A0		MCBSP2_L3
	0x4012 40A0		MCBSP2_CORTEX-A15
	0x2 40A0		MCBSP2_DSP
	0x4902 60A0		MCBSP3_L3
	0x4012 60A0		MCBSP3_CORTEX-A15
	0x2 60A0		MCBSP3_DSP
Description	MCBSPLP Interrupt Status register (interconnect compliant IRQ line)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XEMPTYEOF	RESERVED	XOVFLSTAT	XUNDFLSTAT	XRDY	XEOF	XFSX	XSYNCERR	RESERVED	ROVFLSTAT	RUNDFLSTAT	RRDY	REOF	RFSR	RSYNCERR	

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Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	XEMPTYEOF	Transmit Buffer Empty at end of frame (XEMPTYEOF is set to 1 when a complete frame was transmitted and the transmit buffer is empty). 0x0: XEMPTYEOF is NOT set to when a complete frame was transmitted and the transmit buffer is empty 0x1: XEMPTYEOF is set to 1 when a complete frame was transmitted and the transmit buffer is empty. Writing 1 to this bit clears the bit.	RW	0
13	RESERVED	Reserved	R	0
12	XOVFLSTAT	Transmit Buffer Overflow (XOVFLSTAT bit is set to 1 when transmit buffer overflow; the data which is written while overflow condition is discarded). Writing 1 to this bit clears the bit. 0x0: Transmit buffer NOT overflow 0x1: Transmit buffer overflow; Writing 1 to this bit clears the bit.	RW	0
11	XUNDFLSTAT	Transmit Buffer Underflow (XUNDFLSTAT bit is set to 1 when the transmit data buffer is empty new data is required to be transmitted). Writing 1 to this bit clears the bit. 0x0: the transmit data buffer is NOT empty new data is required to be transmitted. 0x1: the transmit data buffer is empty new data is required to be transmitted. Writing 1 to this bit clears the bit.	RW	0
10	XRDY	Transmit Buffer Threshold Reached (XRDY bit is set to 1 when the transmit buffer free locations are equal or above the THRSH2_REG value). Writing 1 to this bit clears the bit. 0x0: Transmit buffer occupied locations are below the THRSH2_REG value). 0x1: Transmit buffer occupied locations are equal or above the THRSH2_REG value). Writing 1 to this bit clears the bit.	RW	0
9	XEOF	Transmit End Of Frame (XEOF is set to 1 when a complete frame was transmitted). Writing 1 to this bit clears the bit. 0x0: complete frame was NOT transmitted 0x1: complete frame was transmitted; Writing 1 to this bit clears the bit.	RW	0
8	XFSX	Transmit Frame Synchronization (XFSX bit is set to 1 when a new transmit frame synchronization is asserted). Writing 1 to this bit clears the bit. 0x0: new transmit frame synchronization is NOT asserted 0x1: new transmit frame synchronization is asserted; Writing 1 to this bit clears the bit.	RW	0
7	XSYNCERR	Transmit Frame Synchronization Error (XSYNCERR is set to 1 when a transmit frame-sync error is detected). Writing 1 to this bit clears the bit. 0x0: Transmit frame-sync error is NOT detected 0x1: Transmit frame-sync error is detected. Writing 1 to this bit clears the bit.	RW	0
6	RESERVED	Reserved	R	0

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Bits	Field Name	Description	Type	Reset
5	ROVFLSTAT	Receive Buffer Overflow (ROVFLSTAT bit is set to 1 when receive buffer overflow; the data which is written while overflow condition is discarded). Writing 1 to this bit clears the bit. 0x0: receive buffer NOT overflow 0x1: receive buffer overflow; Writing 1 to this bit clears the bit.	RW	0
4	RUNDFLSTAT	Receive Buffer Underflow (RUNDFLSTAT bit is set to 1 when read operation is performed to the receive data register while receive buffer is empty; data read while underflow condition is undefined). Writing 1 to this bit clears the bit. 0x0: read operation is performed to the receive data register while receive buffer is NOT empty 0x1: read operation is performed to the receive data register while receive buffer is empty; Writing 1 to this bit clears the bit.	RW	0
3	RRDY	Receive Buffer Threshold Reached (RRDY bit is set to 1 when the receive buffer occupied locations are equal or above the THRSH1_REG value). Writing 1 to this bit clears the bit. 0x0: receive buffer occupied locations are below the THRSH1_REG value). 0x1: receive buffer occupied locations are equal or above the THRSH1_REG value). Writing 1 to this bit clears the bit.	RW	0
2	REOF	Receive End Of Frame (REOF is set to 1 when a complete frame was received). Writing 1 to this bit clears the bit. 0x0: complete frame was NOT received 0x1: complete frame was received; Writing 1 to this bit clears the bit.	RW	0
1	RFSR	Receive Frame Synchronization (RFSR bit is set to 1 when a new receive frame synchronization is asserted). Writing 1 to this bit clears the bit. 0x0: new receive frame synchronization is NOT asserted 0x1: new receive frame synchronization is asserted; Writing 1 to this bit clears the bit.	RW	0
0	RSYNCERR	Receive Frame Synchronization Error (RSYNCERR is set to 1 when a receive frame-sync error is detected). Writing 1 to this bit clears the bit. 0x0: Receive frame-synchronization error is NOT detected 0x1: Receive frame-synchronization error is detected. Writing 1 to this bit clears the bit.	RW	0

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Table 23-440. Register Call Summary for Register MCBSPLP_IRQSTATUS_REG

Multichannel Buffered Serial Port (MCBSP)

- Receive Wakeup: [0] [1]
- Transmit Wakeup: [2] [3]
- MCBSP Interrupt Requests: [4] [5]
- Enable/Disable the Transmit and Receive Processes: [6] [7] [8] [9]
- Introduction: [10] [11] [12] [13] [14] [15] [16]
- Overrun in the Receiver: [17] [18] [19]
- Possible Responses to Receive Frame-Sync Pulses: [20] [21]
- Underflow in the Receiver: [22] [23]
- Underflow in the Transmitter: [24] [25] [26]
- Possible Responses to Transmit Frame-Sync Pulses: [27]
- Overflow in the Transmitter: [28]
- MCBSP Register Summary: [29] [30] [31]

Table 23-441. MCBSPLP_IRQENABLE_REG

Address Offset	0x0000 00A4		
Physical Address	0x4902 20A4 0x4012 20A4 0x2 20A4 0x4902 40A4 0x4012 40A4 0x2 40A4 0x4902 60A4 0x4012 60A4 0x2 60A4	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP Interrupt Enable register (interconnect compliant IRQ line)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XEMPTYEOFEN	RESERVED	XOVFLEN	XUNDFLEN	XRDYEN	XEOFEN	XFSXEN	XSYNCERREN	RESERVED	ROVFLEN	RUNDFLEN	RRDYEN	REOFEN	RFSREN	RSYNCERREN	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	XEMPTYEOFEN	Transmit buffer empty at end of frame enable bit. 0x0: Transmit Buffer Empty at End Of Frame NOT enabled 0x1: Transmit Buffer Empty at End Of Frame enabled	RW	0
13	RESERVED	Reserved	R	0
12	XOVFLEN	Transmit Buffer Overflow enable bit. 0x0: Transmit Buffer Overflow NOT enabled 0x1: Transmit Buffer Overflow enabled	RW	0
11	XUNDFLEN	Transmit Buffer Underflow enable bit. 0x0: Transmit Buffer Underflow NOT enabled 0x1: Transmit Buffer Underflow enabled	RW	0
10	XRDYEN	Transmit Buffer Threshold Reached enable bit. 0x0: Transmit Buffer Threshold Reached NOT enabled 0x1: Transmit Buffer Threshold Reached enabled	RW	0

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Bits	Field Name	Description	Type	Reset
9	XEOFEN	Transmit End Of Frame enable bit. 0x0: Transmit End Of Frame NOT enabled 0x1: Transmit End Of Frame enabled	RW	0
8	XFSXEN	Transmit Frame Synchronization enable bit. 0x0: Transmit Frame Synchronization NOT enabled 0x1: Transmit Frame Synchronization enabled	RW	0
7	XSYNCERREN	Transmit Frame Synchronization Error enable bit. 0x0: Transmit Frame Synchronization Error NOT enabled 0x1: Transmit Frame Synchronization Error enabled	RW	0
6	RESERVED	Reserved	R	0
5	ROVFLEN	Receive Buffer Overflow enable bit. 0x0: Receive Buffer Overflow NOT enabled 0x1: Receive Buffer Overflow enabled	RW	0
4	RUNDFLEN	Receive Buffer Underflow enable bit. 0x0: Receive Buffer Underflow NOT enabled 0x1: Receive Buffer Underflow enabled	RW	0
3	RRDYEN	Receive Buffer Threshold enable bit. 0x0: Receive Buffer Threshold NOT enabled 0x1: Receive Buffer Threshold enabled	RW	0
2	REOFEN	Receive End Of Frame enable bit. 0x0: Receive End Of Frame NOT enabled 0x1: Receive End Of Frame enabled	RW	0
1	RFSREN	Receive Frame Synchronization enable bit. RW 0x0: Receive Frame Synchronization NOT enabled 0x1: Receive Frame Synchronization enabled	RW	0
0	RSYNCERREN	Receive Frame Synchronization Error enable bit. 0x0: Receive Frame Synchronization Error NOT enabled 0x1: Receive Frame Synchronization Error enabled	RW	0

Table 23-442. Register Call Summary for Register MCBSPLP_IRQENABLE_REG

Multichannel Buffered Serial Port (MCBSP)

- Receive Wakeup: [0] [1] [2] [3]
- Transmit Wakeup: [4] [5] [6] [7] [8]
- MCBSP Interrupt Requests: [9]
- Overrun in the Receiver: [10]
- Possible Responses to Receive Frame-Sync Pulses: [11]
- Underflow in the Receiver: [12]
- Underflow in the Transmitter: [13]
- Possible Responses to Transmit Frame-Sync Pulses: [14]
- Overflow in the Transmitter: [15]
- Interrupt Configuration: [16]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [17]
- MCBSP Register Summary: [18] [19] [20]

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Table 23-443. MCBSPLP_WAKEUPEN_REG

Address Offset	0x0000 00A8		
Physical Address	0x4902 20A8 0x4012 20A8 0x2 20A8 0x4902 40A8 0x4012 40A8 0x2 40A8 0x4902 60A8 0x4012 60A8 0x2 60A8	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP Wakeup Enable register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	XEMPTYEOFEN	RESERVED			XRDYEN	XEOFEN	XFSXEN	XSYNCERREN	RESERVED				RRDYEN	REOFEN	RFSREN	RSYNCERREN

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	XEMPTYEOFEN	Transmit Buffer Empty at End Of Frame enable bit. 0x0: Transmit Buffer Empty at End Of Frame WK enable is NOT active 0x1: Transmit Buffer Empty at End Of Frame WK enable is active	RW	0
13:11	RESERVED	Reserved	R	0x0
10	XRDYEN	Transmit Buffer Threshold Reached WK enable bit. 0x0: Transmit Buffer Threshold WK enable is NOT active 0x1: Transmit Buffer Threshold WK enable is active	RW	0
9	XEOFEN	Transmit End Of Frame WK enable bit. 0x0: Transmit End Of Frame WK enable is NOT active 0x1: Transmit End Of Frame WK enable is active	RW	0
8	XFSXEN	Transmit Frame Synchronization WK enable bit. 0x0: Transmit Frame Synchronization WK enable is NOT active 0x1: Transmit Frame Synchronization WK enable is active	RW	0
7	XSYNCERREN	Transmit Frame Synchronization Error WK enable bit. 0x0: Transmit Frame Synchronization Error WK enable is NOT active 0x1: Transmit Frame Synchronization Error WK enable is active	RW	0
6:4	RESERVED	Reserved	R	0x0
3	RRDYEN	Receive Buffer Threshold wakeup enable bit. 0x0: Receive Buffer Threshold WK enable is NOT active 0x1: Receive Buffer Threshold WK enable is active	RW	0
2	REOFEN	Receive End Of Frame WK enable bit. 0x0: Receive End Of Frame WK enable is NOT active 0x1: Receive End Of Frame WK enable is active	RW	0

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Bits	Field Name	Description	Type	Reset
1	RFSREN	Receive Frame Synchronization WK enable bit. 0x0: Receive Frame Synchronization WK enable is NOT active 0x1: Receive Frame Synchronization WK enable is active	RW	0
0	RSYNCERREN	Receive Frame Synchronization Error WK enable bit. 0x0: Receive Frame Synchronization Error WK enable is NOT active 0x1: Receive Frame Synchronization Error WK enable is active	RW	0

Table 23-444. Register Call Summary for Register MCBSPLP_WAKEUPEN_REG

Multichannel Buffered Serial Port (MCBSP)

- Wake-Up Capability: [0]
- Receive Wakeup: [1] [2] [3] [4]
- Transmit Wakeup: [5] [6] [7] [8] [9]
- MCBSP Register Summary: [10] [11] [12]

Table 23-445. MCBSPLP_XCCR_REG

Address Offset	0x0000 00AC		
Physical Address	0x4902 20AC 0x4012 20AC 0x2 20AC 0x4902 40AC 0x4012 40AC 0x2 40AC 0x4902 60AC 0x4012 60AC 0x2 60AC	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit configuration control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EXTCLKGATE	PPCONNECT	DXENDLY		XFULL_CYCLE	RESERVED			DLB	RESERVED	XDMAEN	RESERVED		XDISABLE		

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	EXTCLKGATE	External clock gating enable (CLKX and FSX master only). When this bit is set and the transmit clock and FSX are set as output, the CLKX is enabled when FSX is active plus 3 clock cycles after (clock is provided for FWID + 4 clock cycles, assuming that the FSX width, active, is FWID + 1 clock cycles); outside this window the external transmit clock is gated. The receive use the same gated transmit clock and transmit frame synchronization signals regardless of the CLKRM/FSRM settings. When using this mode the frame synchronization signal must be active during reception of the entire frame (FWID must be programmed accordingly) to ensure the proper receive process, which requires at least 3 cycles after the frame complete to transfer the data into the receive buffer. 0x0: External clock gating disabled. 0x1: External clock gating enable.	RW	0

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Bits	Field Name	Description	Type	Reset
14	PPCONNECT	Pair to pair connection. When set the DXENO pin is always set to 0 regardless of the frame boundary, setting the tree state buffer as output 0x0: Pair to pair connection. When set the DXENO pin is always set to 0 regardless of the frame boundary, setting the tree state buffer as output 0x1: Pair to pair connection. When set the DXENO pin is always set to 0 regardless of the frame boundary, setting the tree state buffer as output	RW	0
13:12	DXENDLY	When DXENA bit in SPCR1 is set to 1 this field selects the added delay as follow: 0x0: 80 ps 0x1: 160 ps (default) 0x2: 240 ps 0x3: 320 ps	RW	0x1
11	XFULL_CYCLE	Transmit full-cycle mode select. 0x0: MCBSPLP operates in transmit half-cycle mode (transmit frame synchronization is sampled by the opposite edge of the clock used to drive transmit data). 0x1: MCBSPLP operates in transmit full-cycle mode (transmit frame synchronization is sampled by the same edge of the clock used to drive transmit data).	RW	0
10:6	RESERVED	Reserved	R	0x00
5	DLB	Digital Loop-Back 0x0: No DLB 0x1: DLB	RW	0
4	RESERVED	Reserved	R	0
3	XDMAEN	Transmit DMA Enable bit. When set to 0 this bit will gate the external transmit DMA request, without resetting the DMA state machine. It is recommended to change this bit value only during transmit reset. 0x0: When set to 0 this bit will gate the external transmit DMA request, 0x1: When set to 1 this bit will NOT gate the external transmit DMA request,	RW	1
2:1	RESERVED	Reserved	R	0
0	XDISABLE	Transmit Disable bit. When this bit is set the transmit process will stop at the next frame boundary. 0x0: The transmit process will NOT stop at the next frame boundary. 0x1: The transmit process will stop at the next frame boundary.	RW	0

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Table 23-446. Register Call Summary for Register MCBSPLP_XCCR_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP DMA Requests: [0]
- Clocking and Framing Data: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- Enable/Disable the Transmit and Receive Processes: [15] [16] [17]
- Transmit Full-Cycle Mode: [18]
- Transmit Half-Cycle Mode: [19]
- Clock Generation in the SRG: [20]
- MCBSP DMA Configuration: [21]
- MCBSP Basic Programming Model: [22]
- MCBSP Initialization Procedure: [23]
- Programming the MCBSP Registers for the Desired Receiver Configuration (Step 2): [24]
- Programming the MCBSP Registers for the Desired Transmitter Operation (Step 2): [25] [26] [27]
- MCBSP Register Summary: [28] [29] [30]

Table 23-447. MCBSPLP_RCCR_REG

Address Offset	0x0000 00B0		
Physical Address	0x4902 20B0	**Instance**	MCBSP1_L3
	0x4012 20B0		MCBSP1_CORTEX-A15
	0x2 20B0		MCBSP1_DSP
	0x4902 40B0		MCBSP2_L3
	0x4012 40B0		MCBSP2_CORTEX-A15
	0x2 40B0		MCBSP2_DSP
	0x4902 60B0		MCBSP3_L3
	0x4012 60B0		MCBSP3_CORTEX-A15
	0x2 60B0		MCBSP3_DSP
Description	MCBSPLP receive configuration control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				RFULL_CYCLE	RESERVED							RDMAEN	RESERVED		RDISABLE

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11	RFULL_CYCLE	Receive full-cycle mode select. 0x0: MCBSPLP operates in receive half-cycle mode (receive frame synchronization is sampled by the opposite edge of the clock used to sample receive data). 0x1: MCBSPLP operates in receive full-cycle mode (receive frame synchronization is sampled by the same edge of the clock used to sample receive data).	RW	1
10:4	RESERVED	Reserved	R	0x00
3	RDMAEN	Receive DMA Enable bit. When set to 0 this bit will gate the external transmit DMA request, without resetting the DMA state machine. It is recommended to change this bit value only during receive reset. 0x0: When set to 0 this bit will gate the external transmit DMA request 0x1: When set to 1 this bit will NOT gate the external transmit DMA request	RW	1
2:1	RESERVED	Reserved	R	0

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Bits	Field Name	Description	Type	Reset
0	RDISABLE	Receive Disable bit. When this bit is set the receive process will stop at the next frame boundary. 0x0: the receive process will NOT stop at the next frame boundary. 0x1: When this bit is set the receive process will stop at the next frame boundary.	RW	0

Table 23-448. Register Call Summary for Register MCBSPLP_RCCR_REG

Multichannel Buffered Serial Port (MCBSP)

- MCBSP DMA Requests: [0]
- Enable/Disable the Transmit and Receive Processes: [1] [2]
- Receive Full-Cycle Mode: [3]
- Receive Half-Cycle Mode: [4]
- MCBSP DMA Configuration: [5]
- MCBSP Basic Programming Model: [6]
- MCBSP Register Summary: [7] [8] [9]

Table 23-449. MCBSPLP_XBUFFSTAT_REG

Address Offset	0x0000 00B4		
Physical Address	0x4902 20B4 0x4012 20B4 0x2 20B4 0x4902 40B4 0x4012 40B4 0x2 40B4 0x4902 60B4 0x4012 60B4 0x2 60B4	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP transmit buffer status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XBUFFSTAT							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x0
7:0	XBUFFSTAT	Transmit Buffer Status (indicates the number of free locations inside transmit buffer). The XBUFFSTAT value reflects the buffer status on the interface clock domain and it can be smaller than the number of free locations which are seen by the transmit state machine.	R	0x80

Table 23-450. Register Call Summary for Register MCBSPLP_XBUFFSTAT_REG

Multichannel Buffered Serial Port (MCBSP)

- Enable/Disable the Transmit and Receive Processes: [0]
- MCBSP DMA Configuration: [1]
- MCBSP Register Summary: [2] [3] [4]

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Table 23-451. MCBSPLP_RBUFFSTAT_REG

Address Offset	0x0000 00B8		
Physical Address	0x4902 20B8 0x4012 20B8 0x2 20B8 0x4902 40B8 0x4012 40B8 0x2 40B8 0x4902 60B8 0x4012 60B8 0x2 60B8	**Instance**	MCBSP1_L3 MCBSP1_CORTEX-A15 MCBSP1_DSP MCBSP2_L3 MCBSP2_CORTEX-A15 MCBSP2_DSP MCBSP3_L3 MCBSP3_CORTEX-A15 MCBSP3_DSP
Description	MCBSPLP receive buffer status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RBUFFSTAT							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x0
7:0	RBUFFSTAT	Receive Buffer Status (indicates the number of occupied locations inside receive buffer). The RBUFFSTAT value reflects the buffer status on the interface clock domain and it can be smaller than the real number of the occupied locations which are seen by the receive state machine.	R	0x00

Table 23-452. Register Call Summary for Register MCBSPLP_RBUFFSTAT_REG

Multichannel Buffered Serial Port (MCBSP)

- Enable/Disable the Transmit and Receive Processes: [0]
- MCBSP DMA Configuration: [1]
- MCBSP Register Summary: [2] [3] [4]

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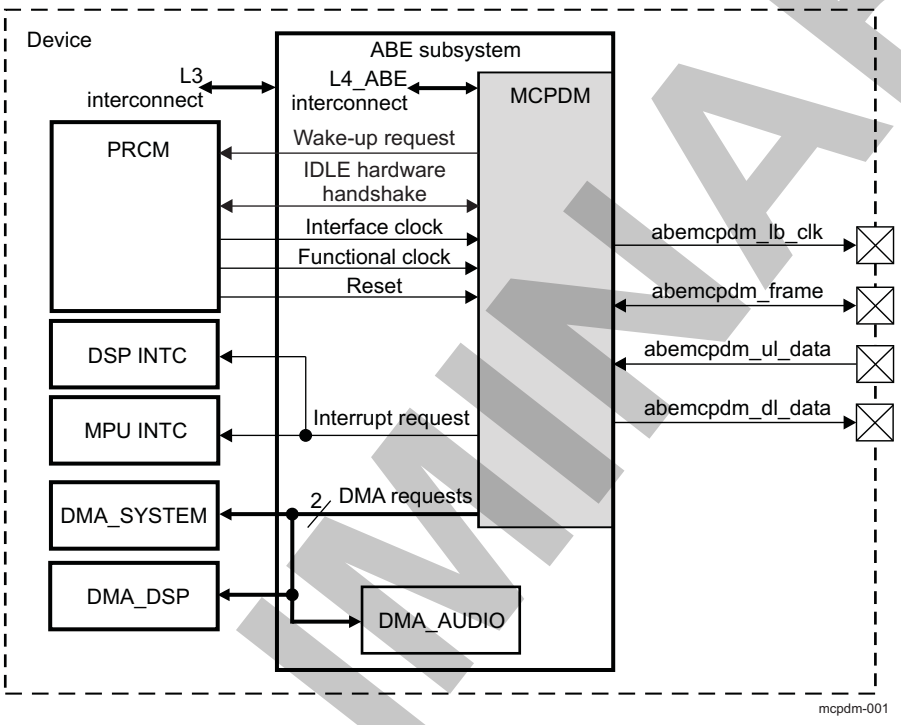
23.6 Multichannel PDM Controller

23.6.1 MCPDM Overview

The multichannel pulse density modulation (MCPDM) module consists of a proprietary audio module dedicated to mobile phone terminals and includes audio uplink and downlink paths communicating with an external audio companion chip through a dedicated interface.

Figure 23-143 shows an overview of the MCPDM module.

Figure 23-143. MCPDM Overview



The MCPDM module supports the following features:

- Full-duplex communication:
  - Five audio downlink channels with up to 3.84 Mbps each
  - Three audio uplink channels with up to 3.84 Mbps each
  - One command channel with up to 3.84 Mbps
  - One status channel with up to 3.84 Mbps
- Uplink and downlink FIFO operations:
  - 16 × 96-bit words for FIFO uplink, where a 96-bit word contains three 24-bit words for the audio uplink channels (one 24-bit word per audio uplink channel) and one 16-bit word for status information
  - 16 × 144-bit words for FIFO downlink, where a 144-bit word contains five 24-bit words for the audio downlink channels (one 24-bit word per audio downlink channel) and one 16-bit word for the command data.
- Interrupt request to MPU and DSP subsystems
- DMA requests with programmable FIFO thresholds:
  - One DMA request for downlink path
  - One DMA request for uplink path
- Upsampling and pulse-density modulators for each audio downlink channel (five channels)
- Offset cancellation feature for audio downlink channels 1 and 2

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- Decimation filter and downsampling for each audio uplink channel (three channels)
- IDLE state hardware handshake
- Wake-up request

23.6.2 MCPDM Environment

This section describes the MCPDM application fields from an environmental point of view (external connections), the MCPDM connectivity options, the protocol and data format used in each case, and lists all possible interfaces.

23.6.2.1 MCPDM Modes

Table 23-453 describes the modes and application fields of the MCPDM module.

Table 23-453. Modes

Mode	Description
Normal mode	Up to five audio channels are transmitted to, and up to three audio channels are received from, the audio companion chip.
Command mode	In addition to the audio channels, commands are transmitted to the audio companion chip.
Status mode	In addition to the audio channels, status information is received from the audio companion chip.

23.6.2.2 MCPDM Signals

Table 23-454 describes the MCPDM module signals and specifies their links to modes.

Table 23-454. I/O

Signal	I/O[1]	Description	Reset Value[2]	Normal Mode	Command Mode	Status Mode
abeMCPDM_lb_clk	O	Clock loopback to the audio companion chip from the abe_clks clock signal. The frequency is the same as abe_clks frequency.[3]	Hi-Z	x	x	x
abeMCPDM_frame	I/O	Frame synchronization and command/status data	Hi-Z	x	x	x
abeMCPDM_ul_data	I	Audio uplink path data	Hi-Z	x	x	x
abeMCPDM_dl_data	O	Audio downlink path data	Hi-Z	x	x	x

(1) I = Input; O = Output; I/O = Bidirectional
(2) Hi-Z = High Impedance
(3) This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The control module registers assign the specific function to the device pads. For more information on control module settings, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, of *Chapter 18, Control Module*.

23.6.2.3 MCPDM Configurations

Figure 23-144 shows the MCPDM generic configuration.

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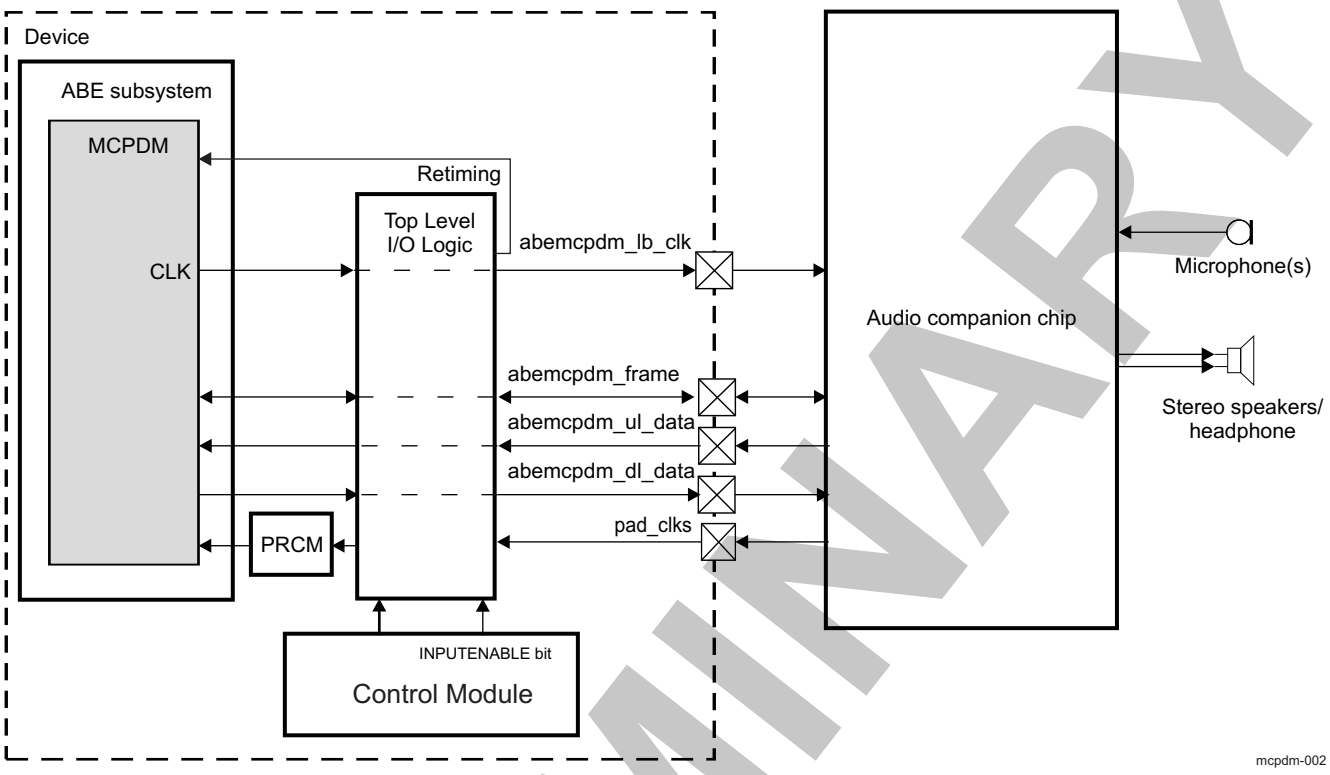
Figure 23-144. MCPDM Generic Configuration



23.6.2.4 Protocols and Data Formats

23.6.2.4.1 Protocols and Data Formats in Normal Mode

This section describes data transfer on the interface in normal mode. In this mode, the abeMCPDM_frame signal is used only for frame synchronization purposes. Figure 23-145 shows the protocols and data formats in normal mode for two examples:

(a) With two downlink and three uplink channels enabled

(b) With five downlink and three uplink channels enabled

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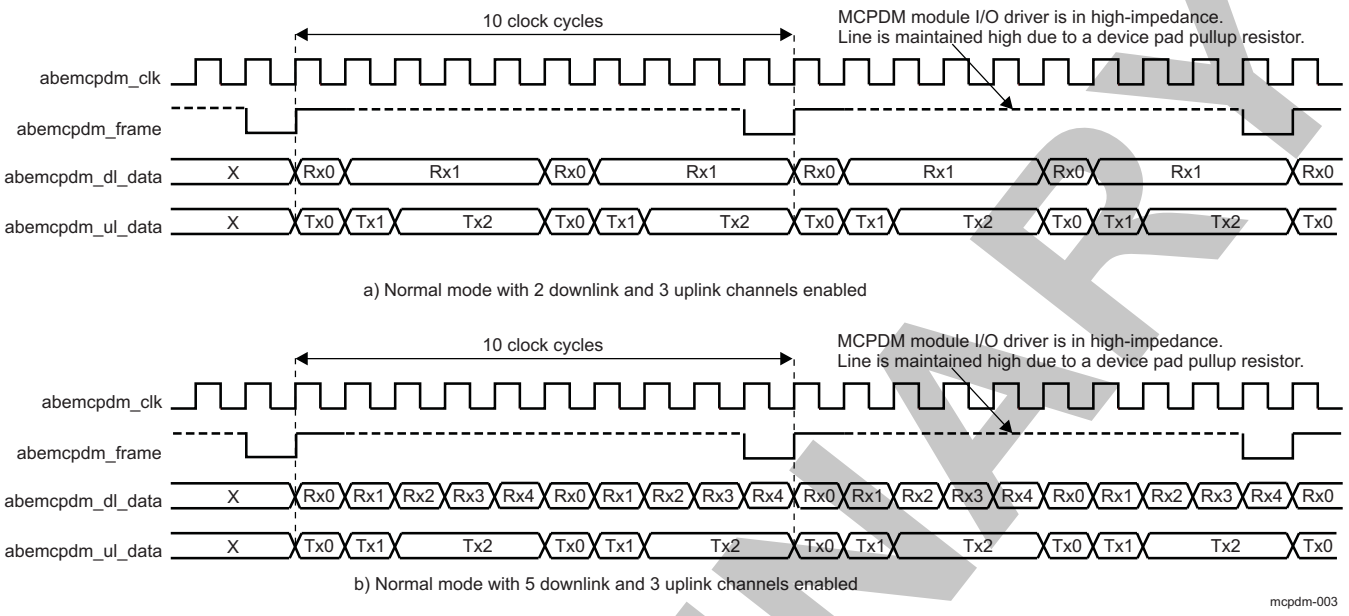
Figure 23-145. Protocols and Data Formats in Normal Mode



In normal mode, the frequency ratio between the abeMCPDM_frame and abeMCPDM_lb_clk signals is 10. This ratio is static and the abeMCPDM_frame signal low-pulse width is one clock period longer than the abeMCPDM_lb_clk signal.

The abeMCPDM_frame signal is driven by the MCPDM module in the device to the external audio companion chip. The MCPDM module drives the abeMCPDM_frame signal low during one clock period of the abeMCPDM_lb_clk signal, and then drives it high during one clock period of the abeMCPDM_lb_clk signal before releasing the abeMCPDM_frame I/O driver in high-impedance state. The MCPDM module pad internal pullup resistor allows a high-level state to be maintained on the abeMCPDM_frame line when the abeMCPDM_frame I/O driver is in high-impedance state.

A maximum of two samples × five downlink channels (10 samples) can be transmitted by the MCPDM module to the external audio companion chip during a frame period.

A maximum of two samples × three uplink channels (six samples) can be received by the MCPDM module from the external audio companion chip during a frame period.

Each downlink and uplink channel can be independently enabled or disabled by setting to 1 or clearing to 0 the corresponding bit in the MCPDM_CTRL register.

23.6.2.4.2 Protocols and Data Formats in Command Mode

This section describes data transfer on the interface in command mode. In this mode, the abeMCPDM_frame signal transmits command words to the external audio companion chip and allows audio registers to be configured in the external audio companion chip (that is, amplifier gains) without using the legacy I^2C interface, which can be busy and thus add latency to gain correction.

NOTE: In command mode, uplink channel samples are transmitted to and downlink channel samples are received from the external audio companion chip as in normal mode.

Figure 23-146 shows the protocols and data formats in command mode.

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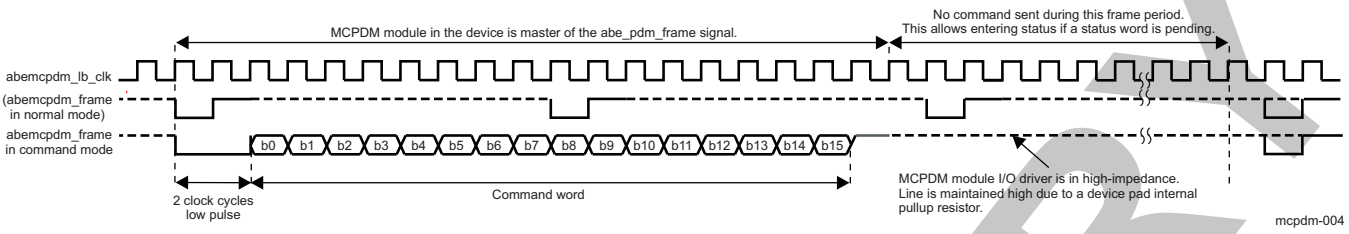
Figure 23-146. Protocols and Data Formats in Command Mode



23.6.2.4.2.1 Entering Command Mode

Command mode can be entered when command data are pending and no status mode is ongoing or detected.

If both conditions are met and the MCPDM_CTRL[9] CMD_INT bit is set to 1, the MCPDM module enters command mode automatically.

To enter command mode, the MCPDM module must drive the abeMCPDM_frame signal low during two periods of the abeMCPDM_lb_clk clock signal.

The external audio companion chip detects a command mode request from the MCPDM module when a low state is detected during two periods of the abeMCPDM_lb_clk clock signal. Once a command mode request is detected, the external audio companion chip enters command mode. In this mode, the status mode cannot be entered during at least four frame cycles.

If a status mode is detected or ongoing while a command is ready to be sent, the command data are stored in an internal register.

If one or more command data are written before the previous one is sent, the previous one is overwritten with the new one and only the last stored 16-bit command data are sent.

If new command data are available while the system is already in command mode, the current command completes normally and exits before re-entering command mode and transmitting the new command data a frame period later.

23.6.2.4.2.2 Command Data Transmission

The 16-bit command data are transmitted directly after the abeMCPDM_frame signal is driven low during two periods of the abeMCPDM_lb_clk clock signal.

When the MCPDM_CTRL[9] CMD_INT bit is set to 1, 16-bit command data must be written to the MCPDM_DN_DATA register. Only the 16 lower bits are significant. When no command must be transmitted on the abeMCPDM_frame line, a null word (0x00000000) must be written as the command data.

When the MCPDM_CTRL[9] CMD_INT bit is cleared to 0, no 16-bit command data must be written to the MCPDM_DN_DATA register.

23.6.2.4.2.3 Exiting Command Mode

After the 16-bit command data is sent, the MCPDM module drives the abeMCPDM_frame signal high during one period of the abeMCPDM_lb_clk clock signal before releasing the abeMCPDM_frame I/O driver in high-impedance state. The MCPDM module pad internal pullup resistor allows a high-level state to be maintained on the abeMCPDM_frame line when the abeMCPDM_frame I/O driver is in high-impedance state.

The MCPDM module exits automatically from command mode one period of the abeMCPDM_lb_clk clock signal after the last bit of the command data is transmitted on the abeMCPDM_frame line.

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NOTE: Because of this protocol mechanism, frame synchronization is lost (and replaced by the ninth bit of the command data) during one frame period. The external audio companion chip must internally emulate a frame synchronization to send uplink channel samples and received downlink channel samples as in normal mode while receiving command data on the abeMCPDM_frame line.

23.6.2.4.2.4 Multiple Command Data Access

As shown in Figure 23-146, two consecutive command data can be sent every three frames. If no status mode is entered after a command data has been sent, the next command data is sent three frames after starting to send the current command data.

23.6.2.4.3 Protocols and Data Formats in Status Mode

This section describes data transfer on the interface in status mode. In this mode, the abeMCPDM_frame signal receives status information from the external audio companion chip.

NOTE: In status mode, as in normal mode, uplink channel samples are transmitted to and downlink channel samples are received from the external audio companion chip.

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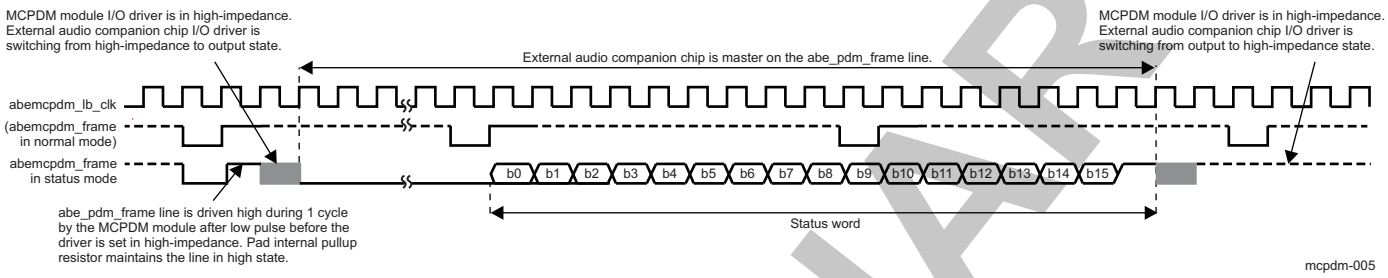
Figure 23-147 shows the protocols and data formats in status mode.

Figure 23-147. Protocols and Data Formats in Status Mode



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23.6.2.4.3.1 Entering Status Mode

Status mode can be entered when no command mode is detected during the last frame low pulse and no command mode is ongoing.

If both conditions are met and the MCPDM_CTRL[10] STATUS_INT bit is set to 1, the MCPDM module enters status mode automatically when the command mode is complete.

In status mode, status information data are sent by the external audio companion chip to the MCPDM module and stored in an internal register.

If one or more status information packages are received before the previous status information is read, the status information stored in the internal register is overwritten with the new one.

In status mode, the external audio companion chip drives the abeMCPDM_frame line low until the next frame synchronization low pulse, and then sends the 16-bit status information data on the abeMCPDM_frame line. During transmission of the status information, the MCPDM module does not generate any frame-sync low pulse on the abeMCPDM_frame line for one frame period.

23.6.2.4.3.2 Status Information Data Reception

The 16-bit status information data are received directly after the second frame-sync low pulse on the abeMCPDM_frame line.

When the MCPDM_CTRL[10] STATUS_INT bit is set to 1, 16 bits of status information data must be read from the MCPDM_UP_DATA register. Only the 16 lower bits are significant. When the value of the status information is a null word (0x00000000), it means that no status information has been sent by the external audio companion chip.

When the MCPDM_CTRL[10] STATUS_INT bit is cleared to 0, no status information data must be read from the MCPDM_UP_DATA register.

23.6.2.4.3.3 Exiting Status Mode

After the 16-bit status information data is sent, the external audio companion chip drives the abeMCPDM_frame line high during one period of the abeMCPDM_lb_clk clock signal before releasing its I/O driver in high-impedance state.

The MCPDM module automatically exits status mode one period of the abeMCPDM_lb_clk clock signal after the last bit of the status information data is transmitted on the abeMCPDM_frame line. After exiting status mode, the MCPDM module generates frame-sync low pulses.

NOTE: Because of the protocol mechanism, frame synchronization is lost during three frame periods. The external audio companion chip must internally emulate a frame synchronization to send uplink channel samples and received downlink channel samples as in normal mode while transmitting status information data on the abeMCPDM_frame line.

23.6.2.4.3.4 Multiple Status Information Data Access

Multiple status information data can be sent by the external audio companion chip to the MCPDM module every four frames.

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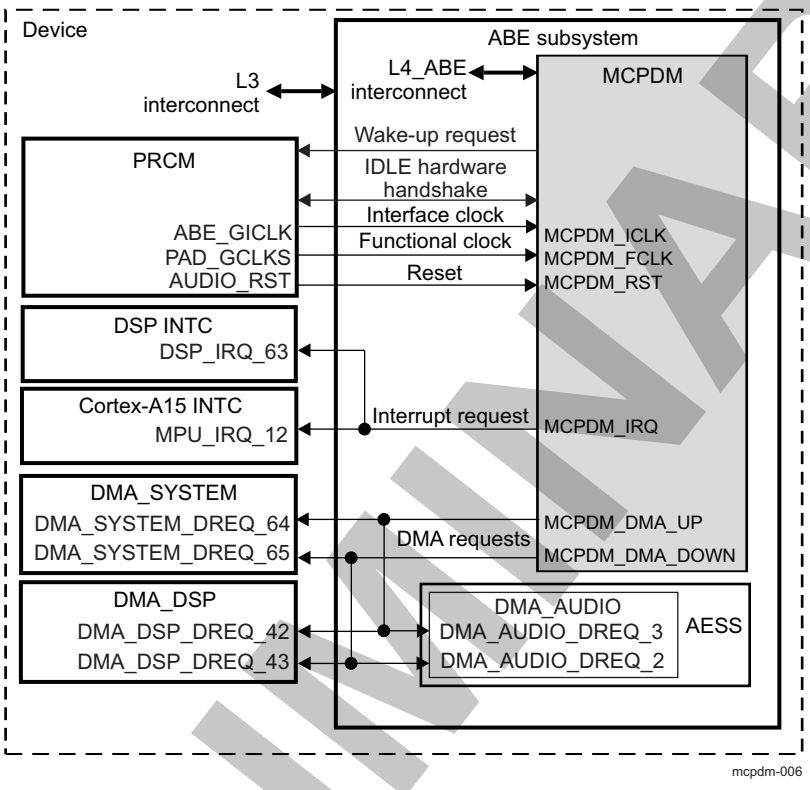
23.6.3 MCPDM Integration

This section describes the MCPDM module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-148 shows the MCPDM integration.

Figure 23-148. MCPDM Integration



NOTE: For more information about the IDLE state hardware handshake and the wake-up request, see Chapter 3, *Power, Reset, and Clock Management*.

Table 23-455 through Table 23-457 summarize the integration of the module in the device.

Table 23-455. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
MCPDM	PD_AUDIO	Yes	L4_ABE

Table 23-456. Clocks and Resets

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
MCPDM	MCPDM_ICLK	ABE_GICLK	PRCM module	MCPDM interface clock
	MCPDM_FCLK	PAD_GCLKS	PRCM module	Common external functional clock
Resets				
MCPDM	MCPDM_RST	AUDIO_RST	PRCM module	MCPDM hardware reset

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Table 23-457. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MCPDM	MCPDM_IRQ	DSP_IRQ_63	DSP	MCPDM interrupt request to the DSP INTC
	MCPDM_IRQ	MPU_IRQ_112	Cortex-A15	MCPDM interrupt request to the Cortex-A15 MPU INTC
DMA Requests				
MCPDM	MCPDM_DMA_UP	DMA_SYSTEM_DREQ_64	DMA_SYSTEM	MCPDM uplink path DMA request to the DMA_SYSTEM
	MCPDM_DMA_DOWN	DMA_SYSTEM_DREQ_65	DMA_SYSTEM	MCPDM downlink path DMA request to the DMA_SYSTEM
	MCPDM_DMA_UP	DMA_DSP_DREQ_42	DMA_DSP	MCPDM uplink path DMA request to the DMA_DSP
	MCPDM_DMA_DOWN	DMA_DSP_DREQ_43	DMA_DSP	MCPDM downlink path DMA request to the DMA_DSP
	MCPDM_DMA_UP	DMA_AUDIO_DREQ_3	DMA_AUDIO	MCPDM uplink path DMA request to the DMA_AUDIO
	MCPDM_DMA_DOWN	DMA_AUDIO_DREQ_2	DMA_AUDIO	MCPDM downlink path DMA request to the DMA_AUDIO

NOTE:

- For the description of the interrupt source, see Section 23.6.4.5, *Interrupt Requests*.
- For the description of the DMA source, see Section 23.6.4.6, *DMA Requests*.

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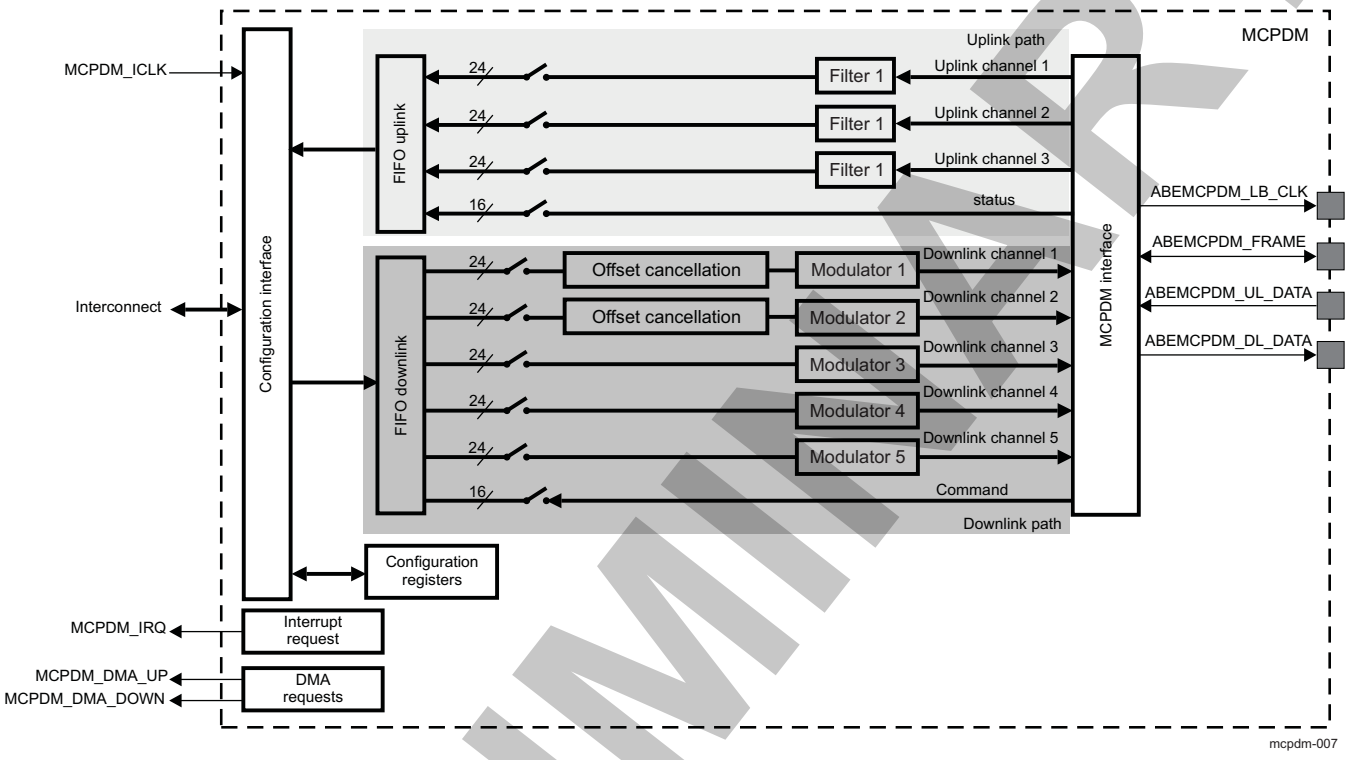
23.6.4 MCPDM Functional Description

23.6.4.1 MCPDM Block Diagram

Figure 23-149 shows the MCPDM block diagram.

Figure 23-149. MCPDM Block Diagram



23.6.4.2 MCPDM Clock Configuration

The functional clock MCPDM_FCLK is provided by the external audio companion chip. Its frequency can be either 17.64 MHz (for a sampling frequency of 88.2/176.4 kHz) or 19.2 MHz (for a sampling frequency of 96/192 kHz).

For resynchronization purposes, the functional clock is also looped back to the audio companion chip through ABEMCPDM_LB_CLK.

23.6.4.3 MCPDM Software Reset

To perform a software reset of the MCPDM module, the MCPDM_SYSCONFIG[0] SOFTRESET bit must be set to 1. Reading the MCPDM_SYSCONFIG[0] SOFTRESET bit gives the status of the software reset:

- Read 1: The software reset is ongoing.
- Read 0: The software reset is complete.

Software must ensure that the software reset completes before doing MCPDM operations. Moreover, uplink and downlink paths can be software reset independently by setting the MCPDM_CTRL[11] SW_UP_RST bit for the uplink path and the MCPDM_CTRL[12] SW_DN_RST bit for the downlink path to 1. The software reset is stopped by clearing the MCPDM_CTRL[11] SW_UP_RST bit for the uplink path, and the MCPDM_CTRL[12] SW_DN_RST bit for the downlink path to 0.

After completion, the software reset of the MCPDM module puts all MCPDM registers in their default state. The downlink/uplink reset resets only the downlink/uplink hardware logic (no registers are affected).

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23.6.4.4 MCPDM Power Management

Table 23-458 describes the power-management features available to the MCPDM module.

Table 23-458. Local Power-Management Features

Feature	Registers	Description
Clock autogating	N/A	Feature not available
Slave idle modes	MCPDM_SYSCONFIG[3:2] IDLEMODE bit field	Force-idle, no-idle, smart-idle, and smart-idle wake-up capable modes are available for the interface clock.
Clock activity	N/A	Feature not available
Master standby modes	N/A	Feature not available
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	MCPDM_IRQWAKEEN and MCPDM_DMAWAKEEN registers	Each register holds one active-high enable bit per event source able to generate wake-up signal.
Audio channel enable	MCPDM_CTRL[0] PDM_UP1_EN to MCPDM_CTRL[2] PDM_UP3_EN bits for audio uplink channels MCPDM_CTRL[3] PDM_DN1_EN to MCPDM_CTRL[7] PDM_DN5_EN bits for audio downlink channels	Each of these bits allows the corresponding audio channel to be enabled (set to 1) or disabled (cleared to 0).
Status channel enable	MCPDM_CTRL[10] STATUS_INT bit for the status channel	This bit allows the status channel to be enabled (set to 1) or disabled (cleared to 0).
Command channel enable	MCPDM_CTRL[9] CMD_INT bit for the command channel	This bit allows the command channel to be enabled (set to 1) or disabled (cleared to 0).

The MCPDM_ICLK interface clock is controlled though the PRCM module using the IDLE request and acknowledge signals. The MCPDM_SYSCONFIG[3:2] IDLEMODE bit field allows the interface clock gating to be controlled in idle mode.

For the uplink path, the interface clock can be put in idle after the uplink path is enabled. Wakeup is available based on the settings of the MCPDM_IRQWAKEEN and MCPDM_DMAWAKEEN registers and the FIFO uplink threshold configured in the MCPDM_FIFO_CTRL_UP[3:0] UP_TRESH bit field. The wake-up signal is asserted when the FIFO uplink level equals or is greater than the FIFO uplink threshold value.

For the downlink path, the interface clock can be put in idle after the FIFO downlink level reaches the FIFO downlink threshold at least once. Wakeup is available according to the settings of the MCPDM_IRQWAKEEN and MCPDM_DMAWAKEEN registers and the FIFO downlink threshold configured in the MCPDM_FIFO_CTRL_DN[3:0] DN_TRESH bit field. The wake-up signal is asserted when the FIFO downlink level is below the FIFO downlink threshold value.

23.6.4.5 MCPDM Interrupt Requests

The MCPDM can generate interrupt requests to the Cortex-A15 MPU and DSP INTCs through the MCPDM_IRQ signal.

Table 23-459 lists the nonmaskable and maskable event flags and their mask that can cause the MCPDM module to generate interrupts.

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Table 23-459. Interrupt Events

Nonmaskable Event Flag[1]	Maskable Event Flag	Event Mask Bit	Event Unmask Bit	Description
MCPDM_IRQSTATUS_RAW[11] UP_IRQ_FULL	MCPDM_IRQSTATUS[11] UP_IRQ_FULL	MCPDM_IRQENABLE_CLR[11] UP_IRQ_FULL_MASK	MCPDM_IRQENABLE_SET[11] UP_IRQ_FULL_MASK	FIFO-uplink-full event. This event occurs when the FIFO uplink is full and a new word is written to the FIFO uplink by the uplink part of the MCPDM module.
MCPDM_IRQSTATUS_RAW[10] UP_IRQ_ALST_FULL	MCPDM_IRQSTATUS[10] UP_IRQ_ALST_FULL	MCPDM_IRQENABLE_CLR[10] UP_IRQ_ALST_FULL_MASK	MCPDM_IRQENABLE_SET[10] UP_IRQ_ALST_FULL_MASK	FIFO-uplink-almost-full event. This event occurs when the FIFO uplink contains (FIFO uplink size – 1) words and a new word is written to the FIFO uplink by the uplink part of the MCPDM module.
MCPDM_IRQSTATUS_RAW[9] UP_IRQ_EMPTY	MCPDM_IRQSTATUS[9] UP_IRQ_EMPTY	MCPDM_IRQENABLE_CLR[9] UP_IRQ_EMPTY_MASK	MCPDM_IRQENABLE_SET[9] UP_IRQ_EMPTY_MASK	FIFO-uplink-empty event. This event occurs when the FIFO uplink is already empty and a new word is read from the FIFO uplink by software.
MCPDM_IRQSTATUS_RAW[8] UP_IRQ	MCPDM_IRQSTATUS[8] UP_IRQ	MCPDM_IRQENABLE_CLR[8] UP_IRQ_MASK	MCPDM_IRQENABLE_SET[8] UP_IRQ_MASK	FIFO-uplink-read-request event. This event occurs when the number of words stored in the FIFO uplink equals or is greater than the FIFO uplink threshold.
MCPDM_IRQSTATUS_RAW[3] DN_IRQ_FULL	MCPDM_IRQSTATUS[3] DN_IRQ_FULL	MCPDM_IRQENABLE_CLR[3] DN_IRQ_FULL_MASK	MCPDM_IRQENABLE_SET[3] DN_IRQ_FULL_MASK	FIFO-downlink-full event. This event occurs when FIFO downlink is already full and a new word is written to the FIFO downlink by software.
MCPDM_IRQSTATUS_RAW[2] DN_IRQ_ALST_EMPTY	MCPDM_IRQSTATUS[2] DN_IRQ_ALST_EMPTY	MCPDM_IRQENABLE_CLR[2] DN_IRQ_ALST_EMPTY_MASK	MCPDM_IRQENABLE_SET[2] DN_IRQ_ALST_EMPTY_MASK	FIFO-downlink-almost-empty event. This event occurs when FIFO downlink contains one word and a new word is read from the FIFO downlink by the downlink part of the MCPDM module.
MCPDM_IRQSTATUS_RAW[1] DN_IRQ_EMPTY	MCPDM_IRQSTATUS[1] DN_IRQ_EMPTY	MCPDM_IRQENABLE_CLR[1] DN_IRQ_EMPTY_MASK	MCPDM_IRQENABLE_SET[1] DN_IRQ_EMPTY_MASK	FIFO-downlink-empty event. This event occurs when FIFO downlink is empty and a new word is read from the FIFO downlink by the downlink part of the MCPDM module.
MCPDM_IRQSTATUS_RAW[0] DN_IRQ	MCPDM_IRQSTATUS[0] DN_IRQ	MCPDM_IRQENABLE_CLR[0] DN_IRQ_MASK	MCPDM_IRQENABLE_SET[0] DN_IRQ_MASK	FIFO-downlink-write-request event. This event occurs when the number of words stored in the FIFO downlink is less than the FIFO downlink threshold.

(1) The MCPDM_IRQSTATUS_RAW register is used mainly for debug purposes.

CAUTION

Once an event generating the interrupt request is processed by software, the event must be cleared by writing a logical 1 to the corresponding bit of the MCPDM_IRQSTATUS register.

Writing a logical 1 in a bit of the MCPDM_IRQSTATUS register also clears the corresponding bit in the MCPDM_IRQSTATUS_RAW register to 0.

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An event can generate an interrupt request when a logical 1 is written to the corresponding mask bit in the MCPDM_IRQENABLE_SET register. Events are reported in the MCPDM_IRQSTATUS and MCPDM_IRQSTATUS_RAW registers.

An event stops generating interrupt requests when a logical 1 is written to the corresponding mask bit in the MCPDM_IRQENABLE_CLR register. Events are reported only in the MCPDM_IRQSTATUS_RAW register.

For the MCPDM_IRQSTATUS_RAW register, the event is reported in the corresponding bit, even if the interrupt request generation is disabled for this event.

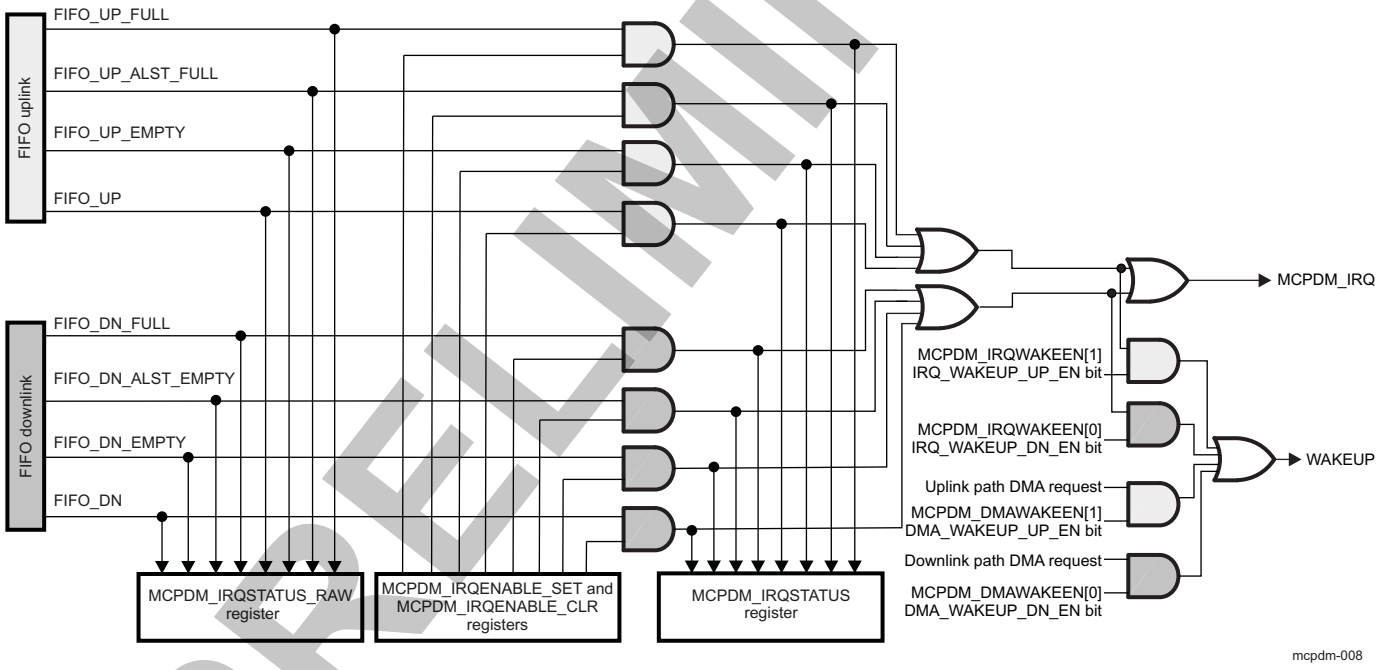
Writing a logical 1 in a bit of the MCPDM_IRQSTATUS_RAW register sets the corresponding bit in the MCPDM_IRQSTATUS register to 1.

The MCPDM_IRQSTATUS_RAW register is used primarily for debug purposes.

For more information about interrupt request signal mapping, see Table 23-457.

Figure 23-150 shows the interrupt tree of the MCPDM module.

Figure 23-150. Interrupt Tree



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23.6.4.6 MCPDM DMA Requests

The MCPDM module can generate two DMA requests to the DMA_SYSTEM, DMA_AUDIO, and DMA_DSP controllers:

- The uplink path can generate a DMA request through the MCPDM_DMA_UP signal.
- The downlink path can generate a DMA request through the MCPDM_DMA_DOWN signal.

Table 23-460 lists the DMA requests of the MCPDM module.

Table 23-460. MCPDM DMA Requests

DMA Request Signal	DMA Request Generation Enabling Bit	DMA Request Generation Disabling Bit	Description
MCPDM_DMA_UP	MCPDM_DMAENABLE_SET [1] DMA_UP_ENABLE	MCPDM_DMAENABLE_CLR [1] DMA_UP_ENABLE	Uplink path DMA request. This request is generated when the number of words in the FIFO uplink equals or is above the FIFO uplink threshold.
MCPDM_DMA_DOWN	MCPDM_DMAENABLE_SET [0] DMA_DN_ENABLE	MCPDM_DMAENABLE_CLR [0] DMA_DN_ENABLE	Downlink path DMA request. This request is generated when the number of words in the FIFO downlink is below the FIFO downlink threshold.

To enable or disable the DMA request generation on the MCPDM_DMA_UP signal, one of the following actions must be performed:

- Write a logical 1 to the MCPDM_DMAENABLE_SET[1] DMA_UP_ENABLE bit to enable DMA request generation on the MCPDM_DMA_UP signal.
- Write a logical 1 to the MCPDM_DMAENABLE_CLR[1] DMA_UP_ENABLE bit to disable DMA request generation on the MCPDM_DMA_UP signal.

To enable or disable the DMA request generation on the MCPDM_DMA_DOWN signal, one of the following actions must be performed:

- Write a logical 1 to the MCPDM_DMAENABLE_SET[0] DMA_DN_ENABLE bit to enable DMA request generation on the MCPDM_DMA_DOWN signal.
- Write a logical 1 to the MCPDM_DMAENABLE_CLR[0] DMA_DN_ENABLE bit to disable DMA request generation on the MCPDM_DMA_DOWN signal.

For more information about DMA request signals mapping, see Table 23-457.

23.6.4.7 Uplink Path

Figure 23-151 shows a detailed block diagram of the uplink path in the MCPDM module.

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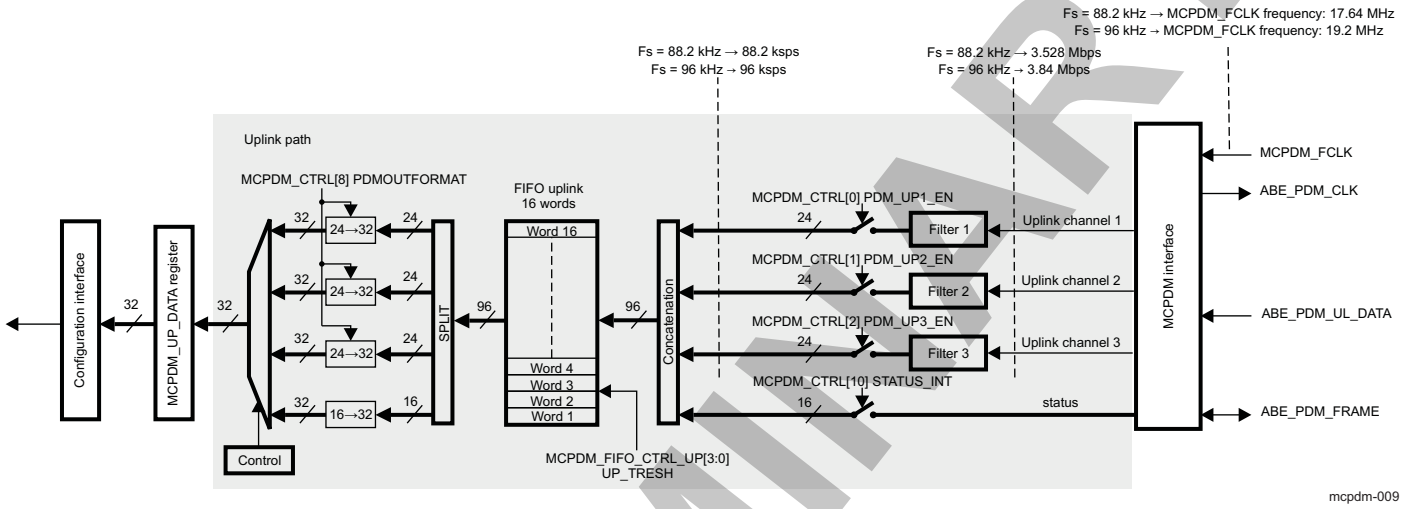
Figure 23-151. Uplink Path Detailed Block Diagram



- The McPDM uplink input PDM data are provided by a 1-bit ADC Sigma-Delta (for each uplink channel).
- The McPDM uplink output PCM linear data format is equal to 24 bits signed format.
- It can be define 0dBpcm = maximum digital level allowed by the 24 bits data format is equal to amplitude peak ($2^{23} – 1$).
- McPDM uplink gain is product from filter decimation factor and filter gain → $G = 40^4 \times 4.89 = 12518400$ (decimal).
- 0dBpdm at McPDM uplink input (all PDM bits at '1' state) is not allowed on real silicon because it will overload the McPDM uplink output:
  - For 0dBpdm McPDM input follows McPDM uplink theoretical decimal output should be: 12518400 = +3.48 dBpcm. The result is calculated by → 20log (12518400 / ($2^{23} – 1$)).
- –4dBpdm level at McPDM input will produce a McPDM uplink output equal to 7898610 = –0.52 dBpcm.

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23.6.4.7.1 Uplink Path Features

The uplink path has the following features:

- Three audio uplink channels
- One status channel
- Decimation filter for each audio uplink channel
- 16-word FIFO uplink with threshold setting
- Audio channel data formatting
- High-frequency sampling feature

23.6.4.7.2 Uplink Path Description

23.6.4.7.2.1 Uplink Data Received From the External Audio Companion Chip

The MCPDM interface receives audio uplink channel data and status information data from the external audio companion chip at a clock rate of 17.64 MHz (for a sampling frequency of 88.2 kHz) or 19.2 MHz (for a sampling frequency of 96 kHz). This low-frequency sampling feature is enabled by default. The uplink path supports a high-frequency sampling feature to work with an ultrasonic external microphone. This feature is enabled by setting the MCPDM_CTRL[13] DIV_SEL bit to 1. Thus, the MCPDM interface receives audio uplink channel data and status information data from the external audio companion chip at a clock rate of 17.64 MHz (for a sampling frequency of 176.4 kHz) or 19.2 MHz (for a sampling frequency of 192 kHz).

The MCPDM interface extracts each data bit related to audio and sends it to the decimation filter of the corresponding channel. Therefore, for each audio uplink channel, the MCPDM interface generates 1 bit data flow to the corresponding decimation filter at a rate of 3.528 Mbps (for a sampling frequency of 88.2 kHz) or 3.84 Mbps (for a sampling frequency of 96 kHz).

Moreover, when status information data are detected on the frame-sync signal (ABEMCPDM_FRAME), the status information data are recovered and sent to the status channel. When no status information data are detected on the frame-sync signal, a null word (0x0000) is sent on the status channel.

For more information about protocols and data formats in normal mode, see Section 23.6.2.4.1, *Protocols and Data Formats in Normal Mode*. For more information about protocols and data formats in status mode, see Section 23.6.2.4.3, *Protocols and Data Formats in Status Mode*.

23.6.4.7.2.2 Decimation Filter

Each bit data flow is related to an audio uplink channel and is provided by the MCPDM interface is processed by a decimation filter. The purpose of this filter is to band-limit the noise and downsample the incoming bit data flow to generate a 24-bit-wide signed data flow at a rate of 88.2 kbps (for a sampling frequency of 88.2 kHz) or 96 kbps (for a sampling frequency of 96 kHz).

23.6.4.7.2.3 FIFO Uplink Management

23.6.4.7.2.3.1 General Description

The MCPDM module implements a FIFO for the uplink path for communication with the host processor in the device. The FIFO uplink can store up to 16 words. Each word is 96 bits wide and is a combination of 24-bit-wide signed audio uplink channel data coming from decimation filters and 16-bit-wide status information data coming from the MCPDM interface.

Figure 23-152 shows the FIFO uplink overview.

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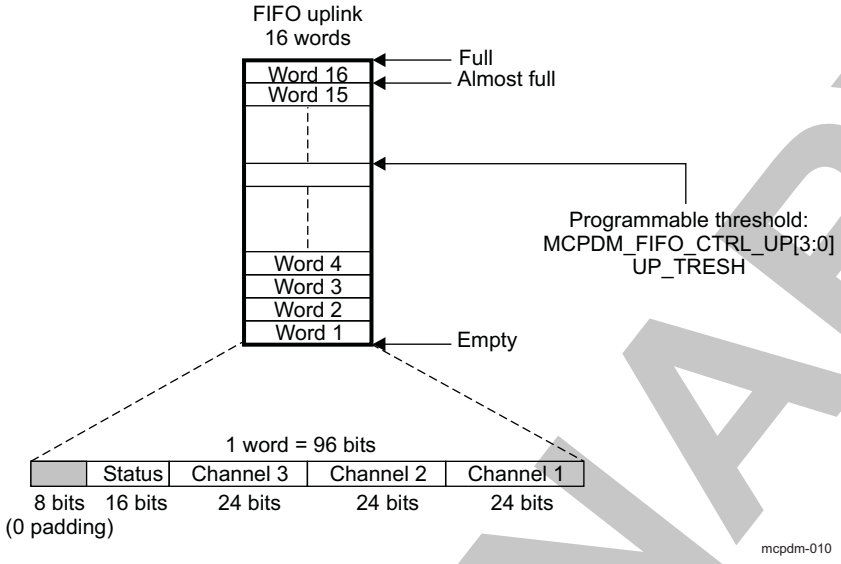
Figure 23-152. FIFO Uplink Overview



23.6.4.7.2.3.2 FIFO Operations

The FIFO uplink is filled with audio uplink channel data coming from decimation filters and status information data from the MCPDM interface. Once the FIFO uplink threshold (MCPDM_FIFO_CTRL_UP[3:0] UP_TRESH bit field) is reached, an event occurs (depending on conditions) and generates an interrupt or DMA request.

NOTE: For more information about events generating an interrupt request, see Section 23.6.4.5, *MCPDM Interrupt Requests*.

For more information about conditions for DMA request generation, see Section 23.6.4.6, *MCPDM DMA Requests*.

When an interrupt request on a FIFO uplink read-request event or an MCPDM_DMA_UP request occurs, the host processor or the DMA controller must read the words from the FIFO uplink (MCPDM_UP_DATA register). The number of read accesses from the host/DMA is determined by the following equation:

Num_read_access = (PDM_UP1_EN + PDM_UP2_EN + PDM_UP3_EN + STAT_INT) * (UP_THRESH), where the PDM_UP_THRESHOLD is programmed through the MCPDM_FIFO_CTRL_UP[3:0] UP_TRESH bit field.

PDM_UP1_EN, PDM_UP2_EN, PDM_UP3_EN, and STAT_INT are boolean values representing whether or not the corresponding channel is enabled.

For example, if audio uplink channels 1 and 3 are enabled, audio uplink channel 2 is disabled, the status channel is enabled, and the uplink threshold is programmed for one line only (MCPDM_FIFO_CTRL_UP[3:0] UP_THRESH = 0x0):

- Num_read_access = 3 because two audio uplink and the status channels are enabled.
- The first reading of the MCPDM_UP_DATA register should correspond to the audio uplink channel 1 data.
- The second reading of the MCPDM_UP_DATA register should correspond to the audio uplink channel 3 data.
- The third reading of the MCPDM_UP_DATA register should correspond to the status information data.

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NOTE: No status information is sent by the external audio companion chip if the status channel is enabled and the 16 lower bits of the corresponding data read from the MCPDM_UP_DATA register is 0x0000 .

The audio uplink and status channels cannot be enabled or disabled on the fly during uplink signaling. The uplink path must first be forced to reset by setting the MCPDM_CTRL[11] SW_UP_RST bit to 1 before enabling or disabling any channels.

Because the audio uplink channel data are 24 bits wide and the MCPDM_UP_DATA register is 32 bits wide, the MCPDM_CTRL[8] PDMOUTFORMAT bit allows the justification of the 24-bit audio uplink channel data in the MCPDM_UP_DATA register to be selected:

- When the MCPDM_CTRL[8] PDMOUTFORMAT bit is cleared to 0, the 24-bit-wide signed audio uplink channel data are left-justified with eight 0 padding bits for the lower bits (24 bits data Left Justified + 8 bits pad)..
- When the MCPDM_CTRL[8] PDMOUT FORMAT is set to 1, the 24-bit-wide signed audio uplink channel data are right-justified and sign-extended (8 bits Pad + 24 bits data Right Justified). For both cases (right or left-justified), 24 bits data transfer starts with MSB First format.

NOTE: The MCPDM_CTRL[8] PDMOUTFORMAT bit does not affect the status information format. When the status information data are read from the MCPDM_UP_DATA register, only the 16 lower bits are significant.

The setting of the MCPDM_CTRL[8] PDMOUTPUTFORMAT bit also affects the audio downlink channel data format.

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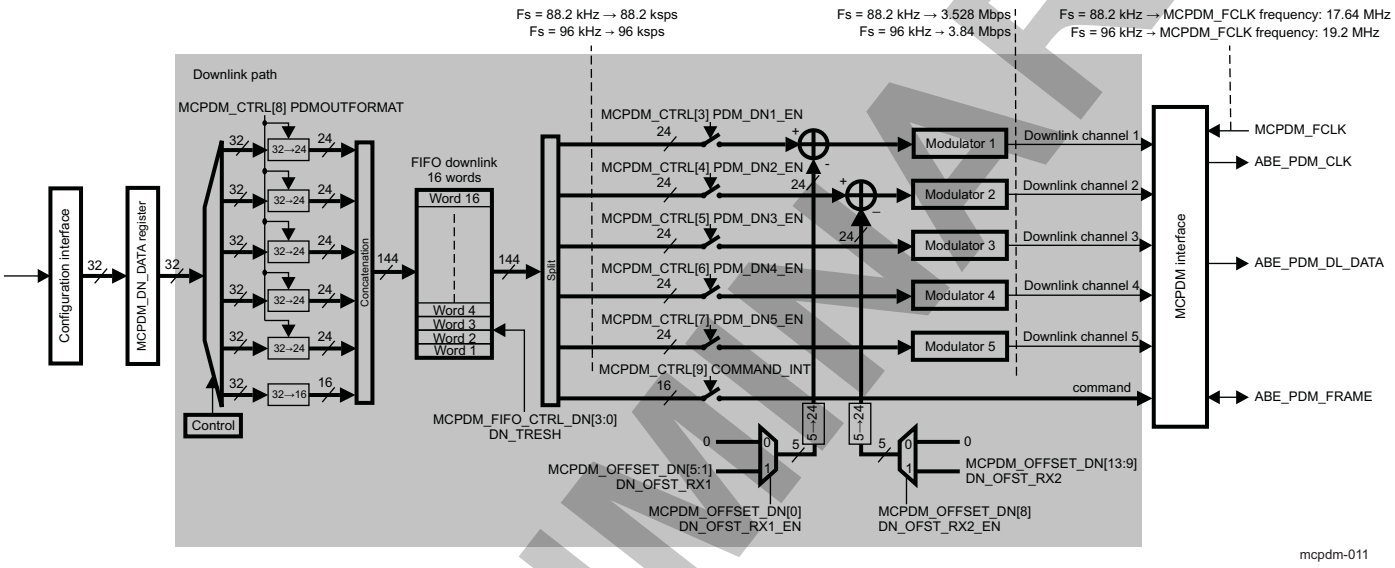
23.6.4.8 Downlink Path

Figure 23-153 shows a detailed block diagram of the downlink path in the MCPDM module.

Figure 23-153. Downlink Path Detailed Block Diagram



- The McPDM downlink and dBpcm is relative to the 24 bits signed format (ABE data format): 0dBpcm amplitude peak is equal to (2^{23} – 1)
- dBpdm is defined by the gain provided by the McPDM total gain is equal to –6.35dB:
  - There is a –6dB attenuation at the input of the Sigma-Delta modulator.
  - The Sigma-Delta has an intrinsic gain of –0.35dB.
- Then the gain between McPDM PDM output and McPDM PCM linear input is constant and equal to –6.35dB.

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23.6.4.8.1 Downlink Path Features

The downlink path has the following features:

- Five audio downlink channels
- Offset cancellation for audio downlink channels 1 and 2
- One command channel
- Delta-sigma modulator for each audio downlink channel
- 16-word FIFO downlink with threshold setting
- Audio channel data formatting

23.6.4.8.2 Downlink Path Description

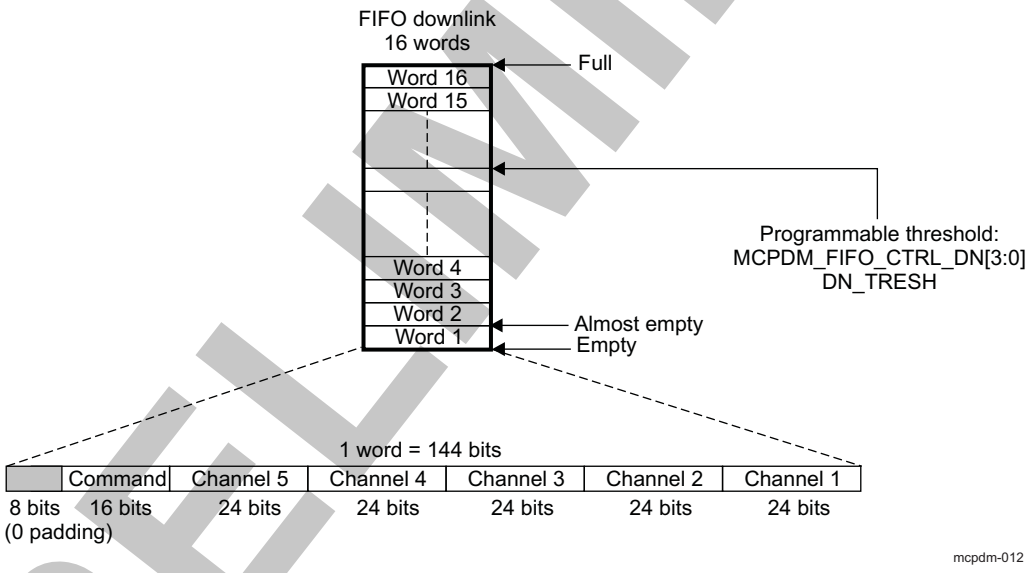
23.6.4.8.2.1 FIFO Downlink Management

23.6.4.8.2.1.1 General Description

The MCPDM module implements a FIFO for the downlink path to communicate with the host processor in the device. The FIFO downlink can store up to 16 words. Each word is 144 bits wide and is a combination of 24-bit-wide signed audio downlink channels data and 16-bit-wide command information data.

Figure 23-154 shows the FIFO downlink overview.

Figure 23-154. FIFO Downlink Overview



23.6.4.8.2.1.2 FIFO Operations

The FIFO downlink is read by the MCPDM module and data related to the audio downlink channels are sent to the delta-sigma modulators, while the data related to the command information is sent to the MCPDM interface. Once the FIFO pointer goes below the programmed threshold (the MCPDM_FIFO_CTRL_DN[3:0] DN_TRESH bit field), a DMA or interrupt request is sent to the DMA or interrupt handler and, depending on conditions, an event occurs and generates an interrupt or DMA request.

NOTE: For more information about events generating an interrupt request, see Section 23.6.4.5, *MCPDM Interrupt Requests*.

For more information about conditions for DMA request generation, see Section 23.6.4.6, *MCPDM DMA Requests*.

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When an interrupt request upon a FIFO downlink write-request event or a MCPDM_DMA_DOWN request occurs, it indicates that the next words are available to be written to the MCPDM_DN_DATA register. The minimum number of write accesses from the host/DMA is determined by the following equation:

Num_min_write_access = PDM_DN1_EN + PDM_DN2_EN + PDM_DN3_EN + PDM_DN4_EN + PDM_DN5_EN + CMD_INT

PDM_DN1_EN, PDM_DN2_EN, PDM_DN3_EN, PDM_DN4_EN, PDM_DN5_EN and CMD_INT are boolean values representing whether the corresponding channel is enabled or not.

The maximum number of write accesses (before overwriting the data in the FIFO still to be transmitted) from the host/DMA is determined by the following equation:

Num_max_write_access = (FIFO_SIZE – DN_THRESH + 1) * (PDM_DN1_EN + PDM_DN2_EN + PDM_DN3_EN + PDM_DN4_EN + PDM_DN5_EN +CMD_INT)

FIFO_SIZE is the size of the downlink FIFO and DN_THRESH is the downlink FIFO threshold, programmed through the MCPDM_FIFO_CTRL_DN[3:0] DN_THRESHOLD bit field.

For example, if audio downlink channels 1, 2, and 3 are enabled, audio downlink channels 4 and 5 are disabled, and the command channel is enabled:

- Num_min_write_access = 4, because three audio downlinks and the command channels are enabled.
- The first writing to the MCPDM_DN_DATA register should correspond to the audio downlink channel 1 data.
- The second writing to the MCPDM_DN_DATA register should correspond to the audio downlink channel 2 data.
- The third writing to the MCPDM_DN_DATA register should correspond to the audio downlink channel 3 data.
- The fourth writing to the MCPDM_DN_DATA register should correspond to the command information data.

NOTE: When the command channel is enabled and no command data must be sent to the external audio companion chip, 0x0000 must be written to the 16 lower bits of the MCPDM_DN_DATA register as command data.

The audio downlink and command channels cannot be enabled or disabled on the fly during downlink signaling. The downlink path must first be forced to reset by setting the MCPDM_CTRL[12] SW_DN_RST bit to 1 before enabling or disabling any channels.

Because the audio downlink channel data are 24 bits wide and the MCPDM_DN_DATA register is 32 bits wide, the MCPDM_CTRL[8] PDMOUTFORMAT bit indicates the justification of the 24-bit audio downlink channel data in the MCPDM_DN_DATA register:

- When the MCPDM_CTRL[8] PDMOUTFORMAT is cleared to 0, the 24-bit-wide signed audio downlink channel data are left-justified with eight 0 padding bits for the lower bits (24 bits data Left Justified + 8 bits pad).
- When MCPDM_CTRL[8] PDMOUT FORMAT is set to 1, the 24-bit-wide signed audio downlink channel data are right-justified and sign-extended (8 bits Pad + 24 bits data Right Justified). For both cases (right or left-justified), 24 bits data transfer starts with MSB First format.

NOTE: The MCPDM_CTRL[8] PDMOUTFORMAT bit does not affect the command information format. When the command information data are written to the MCPDM_DN_DATA register, only the 16 lower bits are significant.

The setting of the MCPDM_CTRL[8] PDMOUTPUTFORMAT bit also affects the audio uplink channel data format.

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23.6.4.8.2.1.3 Offset Cancellation

Because audio downlink channels 1 and 2 are related to the analog headset downlink path within the external audio companion chip, an offset cancellation feature is available for these channels to eliminate the offset of the analog headset downlink path.

When the offset cancellation feature is enabled, an offset value is subtracted from the audio data before being sent to the pulse-density modulator. The offset values are read from registers within the external audio companion chip and configured in the MCPDM_DN_OFFSET[5:1] DN_OFST_RX1 bit field for the audio downlink channel 1, and in the MCPDM_DN_OFFSET[13:9] DN_OFST_RX2 bit field for the audio downlink channel 2.

The offset cancellation feature is enabled or disabled by configuring the MCPDM_DN_OFFSET[0] DN_OFST_RX1_EN bit for the audio downlink channel 1, and the MCPDM_DN_OFFSET[8] DN_OFST_RX2_EN bit for the audio downlink channel 2 (00: Disabled; 10: Enabled).

23.6.4.8.2.1.4 Pulse-Density Modulators

Each 24-bit-wide data related to an audio downlink channel is processed by a pulse-density modulator. The purpose of this modulator is to upsample the incoming audio data and then perform a 1-bit pulse-density modulation to generate a 1-bit data flow at a rate of 3.528 Mbps (for a sampling frequency of 88.2 kHz) or 3.84 Mbps (for a sampling frequency of 96 kHz). The 1-bit pulse-density modulation allows using a 1-bit analog-to-digital converter (ADC) implemented in the external audio companion chip to convert the audio digital data to an audio analog signal.

23.6.4.8.2.1.4.1 Pulse-Density Modulators Watchdog Logic

If the 1-bit data flow coming out of the pulse-density modulator has 12 or more consecutive 1s or 0s, the pulse-density modulator had entered into an unstable or saturated condition. An unstable or saturated condition leads to unpredictable behavior of the pulse-density modulator, thereby producing random noise. To prevent this unstable or saturated condition from occurring, a watchdog logic is used to monitor the 1-bit output of the pulse-density modulator for 12 consecutive 1s or 12 consecutive 0s. If entry to an unstable condition is detected, the watchdog logic asserts the reset of the MCPDM downlink paths for one clock pulse to put the MCPDM hardware logic, related to the downlink mechanism, to initial state.

The watchdog logic is disabled by default. To enable it, the MCPDM_CTRL[14] WD_EN bit must be set to 0x1. If the watchdog logic is disabled, only the assertion of the downlink path reset MCPDM_CTRL[12] SW_DN_RST bit is allowed to reset the MCPDM hardware logic, which is related to the downlink mechanism. If the watchdog logic is enabled, the downlink mechanism logic is reset when the downlink path reset or the watchdog reset is asserted.

Figure 23-155 shows the MCPDM watchdog logic mechanism.

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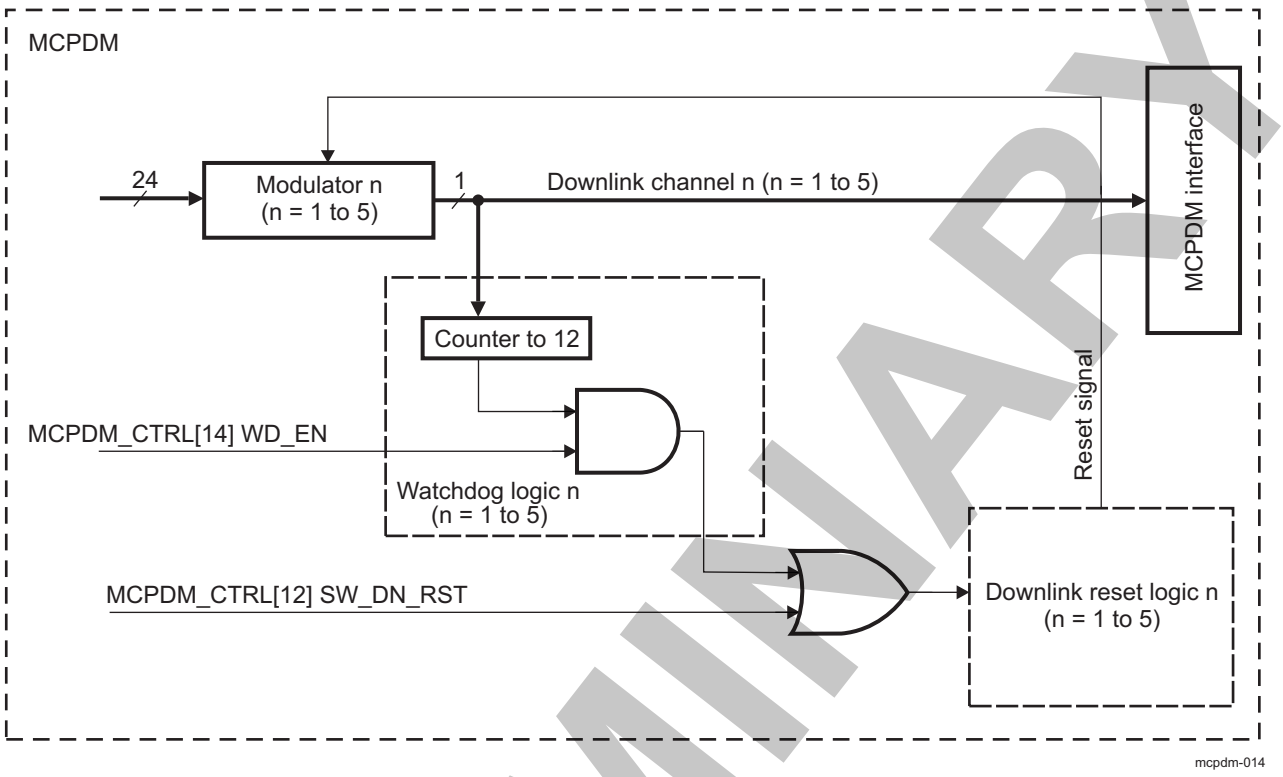
Figure 23-155. MCPDM Watchdog Logic



23.6.4.8.2.1.5 Downlink Data Sent to the External Audio Companion Chip

The MCPDM interface transmits the audio downlink channel data and command data to the external audio companion chip at a clock rate of 17.64 MHz (for a sampling frequency of 88.2 kHz) or 19.2 MHz (for a sampling frequency of 96 kHz).

The command data are sent on the frame-sync signal (ABEMCPDM_FRAME) when the command channel is enabled. When the command channel is disabled or the command data is 0x0000, no command data is sent on the frame-sync signal.

NOTE: For more information about protocols and data formats in normal mode, see Section 23.6.2.4.1, *Protocols and Data Formats in Normal Mode*.

For more information about protocols and data formats in command mode, see Section 23.6.2.4.2, *Protocols and Data Formats in Command Mode*.

23.6.4.9 Error Reporting

During normal operation, when interrupt and DMA requests are properly served, no FIFO-uplink-full and no FIFO-downlink-empty events should occur.

Nevertheless, if one of these events occurs, the corresponding path must be forced to reset by software before being reconfigured. For more information about events servicing, see Section 23.6.5.1.2, *MCPDM Events Servicing*.

Moreover, a FIFO-uplink-empty or FIFO-downlink-full event occurs only when all the channels of the corresponding path have been disabled during normal operation.

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NOTE: Channels must not be enabled or disabled during normal operation.

Channels can be enabled or disabled when the corresponding path is forced to reset. For more information about MCPDM software reset, see Section 23.6.4.3, *MCPDM Software Reset*.

23.6.5 MCPDM Programming Guide

23.6.5.1 MCPDM Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

23.6.5.1.1 Global Initialization

23.6.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules in the device when the MCPDM module is to be used for the first time after a device reset. Initialization of surrounding modules is based on the environment and integration of the MCPDM. For more information, see Section 23.6.2, *MCPDM Environment*, and Section 23.6.3, *MCPDM Integration*.

Table 23-461 describes the global initialization of surrounding modules.

Table 23-461. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM module	The MCPDM interface clock must be enabled and the functional clock must not be gated.
Control module	The MCPDM-specific pad muxing must be configured in the device control module.
(Optional) Cortex-A15 MPU INTC (or DSP INTC)	The Cortex-A15 MPU (or DSP) INTC must be configured to enable the interrupt request generation to the Cortex-A15 MPU (or DSP) subsystem when interrupt requests are generated by the MCPDM module.
(Optional) sDMA (or eDMA or aDMA)	The sDMA (or eDMA or aDMA) controller must be configured to account for the DMA requests generated by the MCPDM module in the case of autonomous data transfers from/to memory.
(Optional) Interconnect	For more information about the interconnect configuration, see Chapter 14, *Interconnect*.
External audio chip	Initialize the external audio chip based on specific needs.
I^2C controller	For more information about I^2C initialization, see Section 23.1, *Multimaster High-Speed I^2C Controller*.

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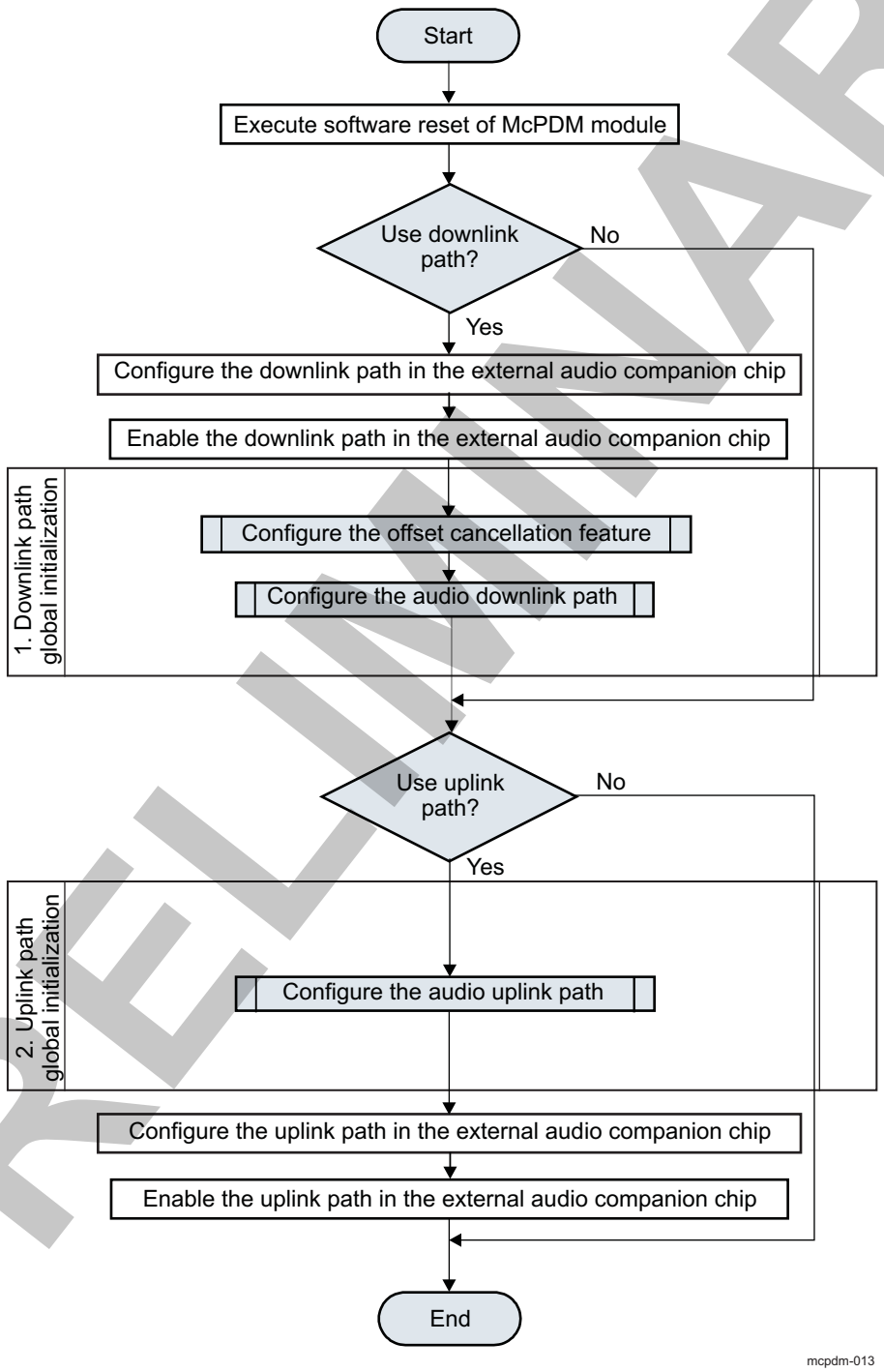
23.6.5.1.1.2 MCPDM Global Initialization

23.6.5.1.1.2.1 Main Sequence—MCPDM Global Initialization

This procedure initializes the MCPDM after a power-on reset (POR) or software reset. Figure 23-156 shows a flow chart for the global initialization of the MCPDM module.

Figure 23-156. MCPDM Global Initialization Flow Chart



The MCPDM software reset is executed by setting the MCPDM_SYSCONFIG[0] SOFTRESET bit to 0x1. To detect the reset done event, user software must check this bit until it is cleared to 0x0 by the hardware.

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Configuration of the offset cancellation feature is optional. The use of that feature depends on the characteristics of the external audio chip attached to the MCPDM interface. If the external chip adds some DC offset on its output, then the offset cancellation feature of the MCPDM must be used.

Table 23-462 describes the steps of the downlink path global initialization.

Table 23-462. MCPDM Downlink Path Global Initialization

Procedure	Step	Access Type	Register/Bit Field/Programming Model	Value
Configure the offset cancellation feature. Only downlink path 1 and downlink path 2 can use the offset cancellation feature.	1. Read the offset value for audio downlink path 1 from the external audio companion chip through the I^2C interface.	R	Offset register 1 in the external audio companion chip	OFFSET1
	2. Configure the offset of audio downlink path 1.	W	MCPDM_DN_OFFSET[5:1] DN_OFST_RX1	OFFSET1
	3. Enable the offset cancellation feature for audio downlink path 1.	W	MCPDM_DN_OFFSET[0] DN_OFST_RX1_EN	0x1
	4. Read the offset value for audio downlink path 2 from the external audio companion chip through the I^2C interface.	R	Offset register 2 in the external audio companion chip	OFFSET2
	5. Configure the offset of audio downlink path 2.	W	MCPDM_DN_OFFSET[13:9] DN_OFST_RX2	OFFSET2
	6. Enable the offset cancellation feature for audio downlink path 2.	W	MCPDM_DN_OFFSET[8] DN_OFST_RX2_EN	0x1
Configure the audio downlink path.	1. Enable the interrupt request generation for the downlink path.	W	a. MCPDM_IRQENABLE_SET[3] DN_IRQ_FULL_MASK b. MCPDM_IRQENABLE_SET[2] DN_IRQ_ALMST_EMPTY_MASK c. MCPDM_IRQENABLE_SET[1] DN_IRQ_EMPTY_MASK d. MCPDM_IRQENABLE_SET[0] DN_IRQ_MASK	When downlink DMA request not used: 0xF When downlink DMA request used: 0xE
	2. Configure the FIFO downlink threshold.	W	MCPDM_FIFO_CTRL_DN[3:0] DN_TRESH	FIFO downlink threshold
	3. Enable the DMA request generation for the downlink path (optional: only if DMA request generation for the downlink path is required).	W	MCPDM_DMAENABLE_SET[0] DMA_DN_ENABLE	0x1
	4. Enable the downlink channels.	W	MCPDM_CTRL	See Table 23-458.

Table 23-463 describes the steps of the uplink path global initialization.

Table 23-463. MCPDM Uplink Path Global Initialization

Step	Access Type	Register/Bit Field/Programming Model	Value
1. Enable the interrupt request generation for the uplink path.	W	a. MCPDM_IRQENABLE_SET[11] UP_IRQ_FULL_MASK b. MCPDM_IRQENABLE_SET[10] UP_IRQ_ALMST_FULL_MASK c. MCPDM_IRQENABLE_SET[9] UP_IRQ_EMPTY_MASK d. MCPDM_IRQENABLE_SET[8] UP_IRQ_MASK	When uplink DMA request not used: 0xF When uplink DMA request used: 0xE
2. Configure the FIFO uplink threshold.	W	MCPDM_FIFO_CTRL_UP[3:0] UP_TRESH	FIFO uplink threshold
3. Enable the DMA request generation for the uplink path (optional: only if DMA request generation for the uplink path is required).	W	MCPDM_DMAENABLE_SET[1] DMA_UP_ENABLE	0x1
4. Configure the FIFO uplink sampling frequency.	W	MCPDM_CTRL[13] DIV_SEL	0x-

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Table 23-463. MCPDM Uplink Path Global Initialization (continued)

Step	Access Type	Register/Bit Field/Programming Model	Value
5. Enable the uplink channels.	W	MCPDM_CTRL	See Table 23-458.

23.6.5.1.2 MCPDM Events Servicing

23.6.5.1.2.1 Downlink Path Event Servicing

Table 23-464 to Table 23-467 describe the downlink path event servicing.

When the four downlink interrupts are enabled and then the downlink channel(s) is enabled, the FIFO-downlink-write request (MCPDM_IRQSTATUS = 0x1) is generated instead of the FIFO-downlink-empty request (MCPDM_IRQSTATUS = 0x2). The first audio data to be sent is written from the interrupt handler. The MCPDM module can work in two ways:

- Enable the desired downlink channels, and then write in the downlink FIFO the audio data that is going to be sent.
- Write the audio data in the downlink FIFO, and then enable the desired downlink channels to send this audio data.

Either way, the FIFO-downlink-write request is generated.

Table 23-464. FIFO-Downlink-Full Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO downlink full?	R	MCPDM_IRQSTATUS[3] DN_IRQ_FULL	
IF: TRUE			0x1
Acknowledge event	W	MCPDM_IRQSTATUS[3] DN_IRQ_FULL	0x1
Downlink path reset	W	MCPDM_CTRL[12] SW_DN_RST	0x1
Downlink path global initialization		See Table 23-462.	
Downlink path reset release	W	MCPDM_CTRL[12] SW_DN_RST	0x0
END			
ELSE			0x0
END			
END TEST TA			

Table 23-465. FIFO-Downlink-Empty Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO downlink empty?	R	MCPDM_IRQSTATUS[1] DN_IRQ_EMPTY	
IF: TRUE			0x1
Acknowledge event	W	MCPDM_IRQSTATUS[1] DN_IRQ_EMPTY	0x1
Downlink path reset	W	MCPDM_CTRL[12] SW_DN_RST	0x1
Downlink path reconfiguration		See Table 23-462.	
Downlink path reset release	W	MCPDM_CTRL[12] SW_DN_RST	0x0
END			
ELSE			0x0
END			
END TEST TA			

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Table 23-466. FIFO-Downlink-Almost-Empty Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO downlink almost empty?	R	MCPDM_IRQSTATUS[2] DN_IRQ_ALST_EMPTY	
IF: TRUE			0x1
Acknowledge event	W	MCPDM_IRQSTATUS[2] DN_IRQ_ALST_EMPTY	0x1
Downlink path reset	W	MCPDM_CTRL[12] SW_DN_RST	0x1
Downlink path reconfiguration		See Table 23-462.	
Downlink path reset release	W	MCPDM_CTRL[12] SW_DN_RST	0x0
END			
ELSE			0x0
END			
END TEST TA			

Table 23-467. FIFO Downlink Write-Request Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO downlink write requested?	R	MCPDM_IRQSTATUS[0] DN_IRQ	
IF: TRUE			0x1
Write FIFO downlink register (see Section 23.6.4.8.2.1.2 for more information).	W	MCPDM_DN_DATA	
Acknowledge event	W	MCPDM_IRQSTATUS[0] DN_IRQ	0x1
END			
ELSE			0x0
END			
END TEST TA			

23.6.5.1.2.2 Uplink Path Events Servicing

Table 23-468 to Table 23-470 describe the downlink path event servicing.

Table 23-468. FIFO-Uplink-Full Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO-uplink-full?	R	MCPDM_IRQSTATUS[11] UP_IRQ_FULL	
IF: TRUE			0x1
Acknowledge event	W	MCPDM_IRQSTATUS[11] UP_IRQ_FULL	0x1
Uplink path reset	W	MCPDM_CTRL[11] SW_UP_RST	0x1
Uplink path global initialization		See Table 23-463.	
Uplink path reset release	W	MCPDM_CTRL[11] SW_UP_RST	0x0
END			
ELSE			0x0
END			
END TEST TA			

Table 23-469. FIFO-Uplink-Almost-Full Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO-uplink-almost-full?	R	MCPDM_IRQSTATUS[10] UP_IRQ_ALST_FULL	
IF: TRUE			0x1

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Table 23-469. FIFO-Uplink-Almost-Full Event Servicing (continued)

Step	Access Type	Register/Bit Field/Programming Model	Value
Acknowledge event	W	MCPDM_IRQSTATUS[10] UP_IRQ_ALST_FULL	0x1
Downlink path reset	W	MCPDM_CTRL[12] SW_DN_RST	0x1
Downlink path reconfiguration		SeeTable 23-462.	
Downlink path reset release	W		0x0
END			
ELSE			0x0
END			
END TEST TA			

Table 23-470. FIFO-Uplink-Empty Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO uplink empty?	R	MCPDM_IRQSTATUS[9] UP_IRQ_EMPTY	
IF: TRUE			0x1
Acknowledge event	W	MCPDM_IRQSTATUS[9] UP_IRQ_EMPTY	0x1
Uplink path reset	W	MCPDM_CTRL[11] SW_UP_RST	0x1
Uplink path reconfiguration		See Table 23-463	
Uplink path reset release	W	MCPDM_CTRL[11] SW_UP_RST	0x0
END			
ELSE			0x0
END			
END TEST TA			

Table 23-471. FIFO-Uplink-Read-Request Event Servicing

Step	Access Type	Register/Bit Field/Programming Model	Value
TEST TA: Is FIFO uplink read requested?	R	MCPDM_IRQSTATUS[8] UP_IRQ	
IF: TRUE			0x1
Read FIFO uplink register (see Section 23.6.4.7.2.3.2 for more information).	R	MCPDM_UP_DATA	
Acknowledge event	W	MCPDM_IRQSTATUS[8] UP_IRQ	0x1
END			
ELSE			0x0
END			
END TEST TA			

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23.6.6 MCPDM Register Manual

23.6.6.1 MCPDM Instance Summary

Table 23-472 summarizes the MCPDM instance.

Table 23-472. MCPDM Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-A15 Private Access	Base Address DSP Private Access	Size
MCPDM	0x4903 2000	0x4013 2000	0x3 2000	4 KiB

NOTE: Private access is an access that does not use the L3/L4 interconnects.

23.6.6.2 MCPDM Registers

23.6.6.2.1 MCPDM Register Summary

Table 23-473 summarizes the MCPDM register mapping.

Table 23-473. MCPDM Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A15 Private Access	Physical Address DSP Private Access
MCPDM_REVISION	R	32	0x0000 0000	0x4903 2000	0x4013 2000	0x3 2000
MCPDM_SYSCONFIG	RW	32	0x0000 0010	0x4903 2010	0x4013 2010	0x3 2010
RESERVED	RW	32	0x0000 0020	0x4903 2020	0x4013 2020	0x3 2020
MCPDM_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4903 2024	0x4013 2024	0x3 2024
MCPDM_IRQSTATUS	RW	32	0x0000 0028	0x4903 2028	0x4013 2028	0x3 2028
MCPDM_IRQENABLE_SET	RW	32	0x0000 002C	0x4903 202C	0x4013 202C	0x3 202C
MCPDM_IRQENABLE_CLR	RW	32	0x0000 0030	0x4903 2030	0x4013 2030	0x3 2030
MCPDM_IRQWAKEEN	RW	32	0x0000 0034	0x4903 2034	0x4013 2034	0x3 2034
MCPDM_DMAENABLE_SET	RW	32	0x0000 0038	0x4903 2038	0x4013 2038	0x3 2038
MCPDM_DMAENABLE_CLR	RW	32	0x0000 003C	0x4903 203C	0x4013 203C	0x3 203C
MCPDM_DMAWAKEEN	RW	32	0x0000 0040	0x4903 2040	0x4013 2040	0x3 2040
MCPDM_CTRL	RW	32	0x0000 0044	0x4903 2044	0x4013 2044	0x3 2044
MCPDM_DN_DATA	RW	32	0x0000 0048	0x4903 2048	0x4013 2048	0x3 2048
MCPDM_UP_DATA	R	32	0x0000 004C	0x4903 204C	0x4013 204C	0x3 204C
MCPDM_FIFO_CTRL_DN	RW	32	0x0000 0050	0x4903 2050	0x4013 2050	0x3 2050
MCPDM_FIFO_CTRL_UP	RW	32	0x0000 0054	0x4903 2054	0x4013 2054	0x3 2054
MCPDM_DN_OFFSET	RW	32	0x0000 0058	0x4903 2058	0x4013 2058	0x3 2058
RESERVED	RW	32	0x0000 005C	0x4903 205C	0x4013 205C	0x3 205C
RESERVED	RW	32	0x0000 0060	0x4903 2060	0x4013 2060	0x3 2060
RESERVED	RW	32	0x0000 0064	0x4903 2064	0x4013 2064	0x3 2064
RESERVED	R	32	0x0000 0068	0x4903 2068	0x4013 2068	0x3 2068
RESERVED	RW	32	0x0000 006C	0x4903 206C	0x4013 206C	0x3 206C
RESERVED	RW	32	0x0000 0070	0x4903 2070	0x4013 2070	0x3 2070
RESERVED	R	32	0x0000 0074	0x4903 2074	0x4013 2074	0x3 2074

23.6.6.2.2 MCPDM Register Description

Table 23-474 through Table 23-504 describe the individual MCPDM registers.

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Table 23-474. MCPDM_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4903 2000 0x4013 2000 0x3 2000	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	IP revision identifier (X.Y.R) used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 23-475. Register Call Summary for Register MCPDM_REVISION

Multichannel PDM Controller

- MCPDM Register Summary: [0]

Table 23-476. MCPDM_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4903 2010 0x4013 2010 0x3 2010	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	This register allows controlling various parameters of the OCP interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IDLEMODE		FREEMU	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:2	IDLEMODE	Configuration of the idle mode 0x0: Force- idle. Idle request is acknowledged unconditionally and immediately. No wake-up capability. 0x1: No-idle. Idle request is never acknowledged. No wake-up capability. 0x2: Smart-idle. The acknowledgment to an idle request is given based on the internal activity. No wake-up capability. 0x3: Idle request acknowledged pending internal conditions, asynchronous wake-up enabled. Wakeup capability.	RW	0x2
1	FREEMU	Sensitivity to emulation (debug) suspend input signal 0x0: MCPDM module is sensitive to emulation suspend. 0x1: MCPDM module is not sensitive to emulation suspend.	RW	0

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Bits	Field Name	Description	Type	Reset
0	SOFTRESET	MCPDM software reset Write 0x0: No action Read 0x0: No ongoing software reset. Read 0x1: Reset is ongoing. Write 0x1: Start software reset.	RW	0

Table 23-477. Register Call Summary for Register MCPDM_SYSCONFIG

Multichannel PDM Controller

- MCPDM Software Reset: [0] [1]
- MCPDM Power Management: [2] [3]
- MCPDM Global Initialization: [4]
- MCPDM Register Summary: [5]

Table 23-478. MCPDM_IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x4903 2024 0x4013 2024 0x3 2024	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	Interrupt request raw status register (for debug purpose)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				UP_IRQ_FULL	UP_IRQ_ALST_FULL	UP_IRQ_EMPTY	UP_IRQ	RESERVED				DN_IRQ_FULL	DN_IRQ_ALST_EMPTY	DN_IRQ_EMPTY	DN_IRQ

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	UP_IRQ_FULL	FIFO-uplink-full signal appears when a write access is performed and the FIFO uplink is already full. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug). Read 0x10: Event pending	RW	0
10	UP_IRQ_ALST_FULL	FIFO-uplink-almost-full signal appears when the FIFO uplink contains (FIFO uplink size – 1) elements. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug). Read 0x10: Event pending	RW	0
9	UP_IRQ_EMPTY	FIFO-uplink-empty signal appears when a read access is done and FIFO uplink already empty. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug). Read 0x10: Event pending	RW	0

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Bits	Field Name	Description	Type	Reset
8	UP_IRQ	FIFO-uplink interrupt appears when the number of data present in the FIFO uplink has reached the value of the FIFO uplink threshold. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug). Read 0x10: Event pending	RW	0
7:4	RESERVED	Reserved	R	0x0
3	DN_IRQ_FULL	FIFO-downlink-full signal appears when the FIFO uplink is full and another a write access is performed. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug). Read 0x10: Event pending	RW	0
2	DN_IRQ_ALST_EMPTY	FIFO-downlink-almost-empty signal appears when the FIFO downlink contains only one element. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x10: Event pending	RW	0
1	DN_IRQ_EMPTY	FIFO-downlink-empty signal appears when read access is performed and FIFO downlink is already empty. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x10: Event pending	RW	0
0	DN_IRQ	FIFO-downlink status is set when the number of data is below the FIFO downlink threshold value. Read 0x0: No event pending Write 0x0: No action Write 0x1: Set the event (for debug) Read 0x10: Event pending	RW	0

Table 23-479. Register Call Summary for Register MCPDM_IRQSTATUS_RAW

Multichannel PDM Controller

- MCPDM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
- MCPDM Register Summary: [14]

Table 23-480. MCPDM_IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4903 2028 0x4013 2028 0x3 2028	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	Interrupt request status register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				UP_IRQ_FULL	UP_IRQ_ALST_FULL	UP_IRQ_EMPTY	UP_IRQ	RESERVED				DN_IRQ_FULL	DN_IRQ_ALST_EMPTY	DN_IRQ_EMPTY	DN_IRQ

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	UP_IRQ_FULL	FIFO-uplink-full signal appears when a write access is performed and the FIFO uplink is already full. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event. Read 0x10: Event pending	RW	0
10	UP_IRQ_ALST_FULL	FIFO-uplink-almost-full signal appears when the FIFO uplink contains (FIFO uplink size – 1) elements. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event. Read 0x10: Event pending	RW	0
9	UP_IRQ_EMPTY	FIFO-uplink-empty signal appears when a read access is done and FIFO uplink already empty. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event. Read 0x10: Event pending	RW	0
8	UP_IRQ	FIFO-uplink interrupt appears when the number of data present in the FIFO uplink has reached the value of the FIFO uplink threshold. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event. Read 0x10: Event pending	RW	0
7:4	RESERVED		R	0x0
3	DN_IRQ_FULL	FIFO-downlink-full signal appears when the FIFO uplink is full and another a write access is performed. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event. Read 0x10: Event pending	RW	0
2	DN_IRQ_ALST_EMPTY	FIFO-downlink-almost-empty signal appears when the FIFO downlink contains only one element. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event. Read 0x10: Event pending	RW	0

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Bits	Field Name	Description	Type	Reset
1	DN_IRQ_EMPTY	FIFO-downlink-empty signal appears when read access is performed and FIFO downlink is already empty. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event. Read 0x10: Event pending	RW W1toSet	0
0	DN_IRQ	FIFO-downlink status is set when the number of data is below the FIFO downlink threshold value. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event. Read 0x10: Event pending	RW	0

Table 23-481. Register Call Summary for Register MCPDM_IRQSTATUS

Multichannel PDM Controller

- MCPDM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11]
- Downlink Path Event Servicing: [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]
- Uplink Path Events Servicing: [22] [23] [24] [25] [26] [27] [28] [29]
- MCPDM Register Summary: [30]

Table 23-482. MCPDM_IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x4903 202C 0x4013 202C 0x3 202C	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	Interrupt request enable set register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				UP_IRQ_FULL_MASK	UP_IRQ_ALST_FULL_MASK	UP_IRQ_EMPTY_MASK	UP_IRQ_MASK	RESERVED				DN_IRQ_FULL_MASK	DN_IRQ_ALST_EMPTY_MASK	DN_IRQ_EMPTY_MASK	DN_IRQ_MASK

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	UP_IRQ_FULL_MASK	FIFO-uplink-full event interrupt enabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Enable interrupt Read 0x1: Interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
10	UP_IRQ_ALST_FULL_MASK	FIFO-uplink-almost-full event interrupt enabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Enable interrupt Read 0x1: Interrupt enabled	RW	0
9	UP_IRQ_EMPTY_MASK	FIFO-uplink-empty event interrupt enabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Enable interrupt Read 0x1: Interrupt enabled	RW	0
8	UP_IRQ_MASK	FIFO-uplink-read-request event interrupt enabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Enable interrupt Read 0x1: Interrupt enabled	RW	0
7:4	RESERVED		R	0x0
3	DN_IRQ_FULL_MASK	FIFO-downlink-full event interrupt enabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Enable interrupt Read 0x1: Interrupt enabled	RW	0
2	DN_IRQ_ALST_EMPTY_MASK	FIFO downlink almost-empty event interrupt enabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Enable interrupt Read 0x1: Interrupt enabled	RW	0
1	DN_IRQ_EMPTY_MASK	FIFO-downlink-empty event interrupt enabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Enable interrupt Read 0x1: Interrupt enabled	RW	0
0	DN_IRQ_MASK	FIFO downlink write-request event interrupt enabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Enable interrupt Read 0x1: Interrupt enabled	RW	0

Table 23-483. Register Call Summary for Register MCPDM_IRQENABLE_SET

Multichannel PDM Controller

- MCPDM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- MCPDM Global Initialization: [9] [10] [11] [12] [13] [14] [15] [16]
- MCPDM Register Summary: [17]

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Table 23-484. MCPDM_IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x4903 2030 0x4013 2030 0x3 2030	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	Interrupt request enable clear register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				UP_IRQ_FULL_MASK	UP_IRQ_ALST_FULL_MASK	UP_IRQ_EMPTY_MASK	UP_IRQ_MASK	RESERVED				DN_IRQ_FULL_MASK	DN_IRQ_ALST_EMPTY_MASK	DN_IRQ_EMPTY_MASK	DN_IRQ_MASK

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11	UP_IRQ_FULL_MASK	FIFO-uplink-full event interrupt disabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Disable interrupt Read 0x1: Interrupt enabled	RW	0
10	UP_IRQ_ALST_FULL_MASK	FIFO-uplink-almost-full event interrupt disabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Disable interrupt Read 0x1: Interrupt enabled	RW	0
9	UP_IRQ_EMPTY_MASK	FIFO-uplink-empty event interrupt disabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Disable interrupt Read 0x1: Interrupt enabled	RW	0
8	UP_IRQ_MASK	FIFO-uplink-read-request event interrupt disabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Disable interrupt Read 0x1: Interrupt enabled	RW	0
7:4	RESERVED		R	0x0
3	DN_IRQ_FULL_MASK	FIFO-downlink-full event interrupt disabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Disable interrupt Read 0x1: Interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
2	DN_IRQ_ALST_EMPTY_MASK	FIFO downlink almost-empty event interrupt disabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Disable interrupt Read 0x1: Interrupt enabled	RW	0
1	DN_IRQ_EMPTY_MASK	FIFO-downlink-empty event interrupt disabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Disable interrupt Read 0x1: Interrupt enabled	RW	0
0	DN_IRQ_MASK	FIFO downlink write-request event interrupt disabling bit Read 0x0: Interrupt disabled Write 0x0: No action Write 0x10: Disable interrupt Read 0x1: Interrupt enabled	RW	0

Table 23-485. Register Call Summary for Register MCPDM_IRQENABLE_CLR

Multichannel PDM Controller

- MCPDM Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- MCPDM Register Summary: [9]

Table 23-486. MCPDM_IRQWAKEEN

Address Offset	0x0000 0034		
Physical Address	0x4903 2034 0x4013 2034 0x3 2034	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	Interrupt request wake-up enable register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														IRQ_WAKEUP_UP_EN	IRQ_WAKEUP_DN_EN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	IRQ_WAKEUP_UP_EN	Enabling/disabling bit for wake-up request generation on a FIFO-uplink-read-request event 0x00: Disable the wake-up request generation. 0x10: Enable the wake-up request generation.	RW	1
0	IRQ_WAKEUP_DN_EN	Enabling/disabling bit for wake-up by FIFO downlink write-request event 0x00: Disable the wake-up request generation. 0x10: Enable the wake-up request generation.	RW	1

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Table 23-487. Register Call Summary for Register MCPDM_IRQWAKEEN

Multichannel PDM Controller

- MCPDM Power Management: [0] [1] [2]
- MCPDM Register Summary: [3]

Table 23-488. MCPDM_DMAENABLE_SET

Address Offset	0x0000 0038		
Physical Address	0x4903 2038 0x4013 2038 0x3 2038	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	DMA request enable set register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DMA_UP_ENABLE	DMA_DN_ENABLE

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	DMA_UP_ENABLE	Uplink path DMA request generation enabling bit Read 0x00: DMA request disabled Write 0x0: No action Write 0x10: Enable DMA request Read 0x10: DMA request enabled	RW	0
0	DMA_DN_ENABLE	Downlink path DMA request generation enabling bit Read 0x00: DMA request disabled Write 0x0: No action Write 0x10: Enable DMA request Read 0x10: DMA request enabled	RW	0

Table 23-489. Register Call Summary for Register MCPDM_DMAENABLE_SET

Multichannel PDM Controller

- MCPDM DMA Requests: [0] [1] [2] [3]
- MCPDM Global Initialization: [4] [5]
- MCPDM Register Summary: [6]

Table 23-490. MCPDM_DMAENABLE_CLR

Address Offset	0x0000 003C		
Physical Address	0x4903 203C 0x4013 203C 0x3 203C	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	DMA request enable clear register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DMA_UP_ENABLE	DMA_DN_ENABLE

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	DMA_UP_ENABLE	Uplink path DMA request generation disabling bit Read 0x00: DMA request disabled Write 0x0: No action Write 0x10: Disable DMA request Read 0x10: DMA request enabled	RW	0
0	DMA_DN_ENABLE	Downlink path DMA request generation disabling bit Read 0x00: DMA request disabled Write 0x0: No action Write 0x10: Disable DMA request Read 0x10: DMA request enabled	RW	0

Table 23-491. Register Call Summary for Register MCPDM_DMAENABLE_CLR

Multichannel PDM Controller

- MCPDM DMA Requests: [0] [1] [2] [3]
- MCPDM Register Summary: [4]

Table 23-492. MCPDM_DMAWAKEEN

Address Offset	0x0000 0040		
Physical Address	0x4903 2040 0x4013 2040 0x3 2040	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	DMA request wake-up enable register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														DMA_WAKEUP_UP_EN	DMA_WAKEUP_DN_EN

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	DMA_WAKEUP_UP_EN	Enabling/disabling bit for wake-up request generation upon an uplink path DMA request 0x00: Disable the wake-up request generation 0x10: Enable the wake-up request generation	RW	1

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Bits	Field Name	Description	Type	Reset
0	DMA_WAKEUP_DN_EN	Enabling/disabling bit for wake-up request generation on a downlink path DMA request 0x00: Disable the wake-up request generation. 0x10: Enable the wake-up request generation.	RW	1

Table 23-493. Register Call Summary for Register MCPDM_DMAWAKEEN

Multichannel PDM Controller

- MCPDM Power Management: [0] [1] [2]
- MCPDM Register Summary: [3]

Table 23-494. MCPDM_CTRL

Address Offset	0x0000 0044		
Physical Address	0x4903 2044 0x4013 2044 0x3 2044	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	MCPDM control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DS4_WD_EN	DIV_SEL	SW_DN_RST	SW_UP_RST	STATUS_INT	CMD_INT	PDMOUTFORMAT	PDM_DN5_EN	PDM_DN4_EN	PDM_DN3_EN	PDM_DN2_EN	PDM_DN1_EN	PDM_UP3_EN	PDM_UP2_EN	PDM_UP1_EN	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x00000
14	DS4_WD_EN	This bit is used to enable or disable the delta sigma watchdog logic. 0x0: Disabled (default after reset) 0x1: Enabled	RW	0
13	DIV_SEL	Multiply by 2 the FS of the uplink path. 0x0: FS = 88.2 kHz or 96 kHz 0x1: FS = 176.4 kHz or 192 kHz	RW	0
12	SW_DN_RST	Software reset of the downlink path 0x00: Downlink path is out of reset. 0x1: Reset of the downlink path	RW	0
11	SW_UP_RST	Software reset of the uplink path 0x0: Uplink path is out of reset. 0x1: Reset of the uplink path	RW	0
10	STATUS_INT	Status channel enabling/disabling bit 0x0: Status channel is disabled. 0x1: Status channel is enabled.	RW	0
9	CMD_INT	Command channel enabling/disabling bit 0x0: Command channel is disabled. 0x1: Command channel is enabled.	RW	0
8	PDMOUTFORMAT	Audio format selection: 0x0:Left justification with eight 0-bit padding added for the LSBs 0x1: Right justification with sign bit extended to the 8 MSBs	RW	0

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Bits	Field Name	Description	Type	Reset
7	PDM_DN5_EN	Audio downlink channel 5 enabling/disabling bit	RW	0
6	PDM_DN4_EN	Audio downlink channel 4 enabling/disabling bit	RW	0
5	PDM_DN3_EN	Audio downlink channel 3 enabling/disabling bit	RW	0
4	PDM_DN2_EN	Audio downlink channel 2 enabling/disabling bit	RW	0
3	PDM_DN1_EN	Audio downlink channel 1 enabling/disabling bit	RW	0
2	PDM_UP3_EN	Audio uplink channel 3 enabling/disabling bit	RW	0
1	PDM_UP2_EN	Audio uplink channel 2 enabling/disabling bit	RW	0
0	PDM_UP1_EN	Audio uplink channel 1 enabling/disabling bit	RW	0

Table 23-495. Register Call Summary for Register MCPDM_CTRL

Multichannel PDM Controller

- Protocols and Data Formats in Normal Mode: [0]
- Entering Command Mode: [1]
- Command Data Transmission: [2] [3]
- Entering Status Mode: [4]
- Status Information Data Reception: [5] [6]
- MCPDM Software Reset: [7] [8] [9] [10]
- MCPDM Power Management: [11] [12] [13] [14] [15] [16]
- Uplink Data Received From the External Audio Companion Chip: [17]
- FIFO Uplink Management: [18] [19] [20] [21] [22] [23]
- FIFO Downlink Management: [24] [25] [26] [27] [28] [29] [30] [31]
- MCPDM Global Initialization: [32] [33] [34]
- Downlink Path Event Servicing: [35] [36] [37] [38] [39] [40]
- Uplink Path Events Servicing: [41] [42] [43] [44] [45]
- MCPDM Register Summary: [46]

Table 23-496. MCPDM_DN_DATA

Address Offset	0x0000 0048		
Physical Address	0x4903 2048 0x4013 2048 0x3 2048	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	Downlink path data register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DN_DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DN_DATA	Downlink path data value	RW	0x0000 0000

Table 23-497. Register Call Summary for Register MCPDM_DN_DATA

Multichannel PDM Controller

- Command Data Transmission: [0] [1]
- FIFO Downlink Management: [2] [3] [4] [5] [6] [7] [8] [9] [10]
- Downlink Path Event Servicing: [11]
- MCPDM Register Summary: [12]

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Table 23-498. MCPDM_UP_DATA

Address Offset	0x0000 004C		
Physical Address	0x4903 204C 0x4013 204C 0x3 204C	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	Uplink path data register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UP_DATA																															

Bits	Field Name	Description	Type	Reset
31:0	UP_DATA	Uplink path data value	R	0x0000 0000

Table 23-499. Register Call Summary for Register MCPDM_UP_DATA

Multichannel PDM Controller

- Status Information Data Reception: [0] [1]
- FIFO Uplink Management: [2] [3] [4] [5] [6] [7] [8] [9]
- Uplink Path Events Servicing: [10]
- MCPDM Register Summary: [11]

Table 23-500. MCPDM_FIFO_CTRL_DN

Address Offset	0x0000 0050		
Physical Address	0x4903 2050 0x4013 2050 0x3 2050	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	FIFO downlink control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DN_TRESH			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000
3:0	DN_TRESH	FIFO downlink threshold value	RW	0x2

Table 23-501. Register Call Summary for Register MCPDM_FIFO_CTRL_DN

Multichannel PDM Controller

- MCPDM Power Management: [0]
- FIFO Downlink Management: [1] [2]
- MCPDM Global Initialization: [3]
- MCPDM Register Summary: [4]

Table 23-502. MCPDM_FIFO_CTRL_UP

Address Offset	0x0000 0054		
Physical Address	0x4903 2054 0x4013 2054 0x3 2054	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description	FIFO uplink control register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												UP_TRESH			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000
3:0	UP_TRESH	FIFO uplink threshold value	RW	0x2

Table 23-503. Register Call Summary for Register MCPDM_FIFO_CTRL_UP

Multichannel PDM Controller

- MCPDM Power Management: [0]
- FIFO Uplink Management: [1] [2] [3]
- MCPDM Global Initialization: [4]
- MCPDM Register Summary: [5]

Table 23-504. MCPDM_DN_OFFSET

Address Offset	0x0000 0058		
Physical Address	0x4903 2058 0x4013 2058 0x3 2058	**Instance**	MCPDM_L3 MCPDM_CORTEX-A15 MCPDM_DSP
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		DN_OFST_RX2					DN_OFST_RX2_EN	RESERVED						DN_OFST_RX1				DN_OFST_RX1_EN

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:9	DN_OFST_RX2	Offset value for the audio downlink channel 2	RW	0x00
8	DN_OFST_RX2_EN	Offset cancellation feature enabling/disabling bit for the audio downlink channel 2 0x0: Offset cancellation disabled 0x1: Offset cancellation enabled	RW	0
7:6	RESERVED		R	0x0
5:1	DN_OFST_RX1	Offset value for the audio downlink channel 1	RW	0x00
0	DN_OFST_RX1_EN	Offset cancellation feature enabling/disabling bit for the audio downlink channel 1 0x0: Offset cancellation disabled 0x1: Offset cancellation enabled	RW	0

Table 23-505. Register Call Summary for Register MCPDM_DN_OFFSET

Multichannel PDM Controller

- FIFO Downlink Management: [0] [1] [2] [3]
- MCPDM Global Initialization: [4] [5] [6] [7]
- MCPDM Register Summary: [8]

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23.7 Digital Microphone Module

This section describes the digital microphone (DMIC) module.

23.7.1 DMIC Overview

The DMIC module consists of an audio module dedicated to a mobile telephone terminal. The DMIC allows the support of up to six digital microphones. It provides an interface between the audio backend (ABE) module and microphones connected through the 6-wire DMIC serial interface.

The DMIC supports six paths. Because each path is composed of two digital microphone channels, the DMIC can be used with three stereo or six mono microphones. Each path is enabled or disabled independently.

The DMIC generates a pulse-density modulated (PDM) stream of bits and transfers it in one period or one half-period of the clock provided by the DMIC (oversampling clock).

Each microphone is directly connected to a filter decimator to extract the audio samples at the desired accuracy and sample rate. Data are stored in the first in first out (FIFO), which is controlled by interrupt request (IRQ) and direct memory access (DMA) request.

The DMIC pads are supplied with 1.8 V. These pads assure the transition to the host supply.

Figure 23-157 shows the DMIC in the device.

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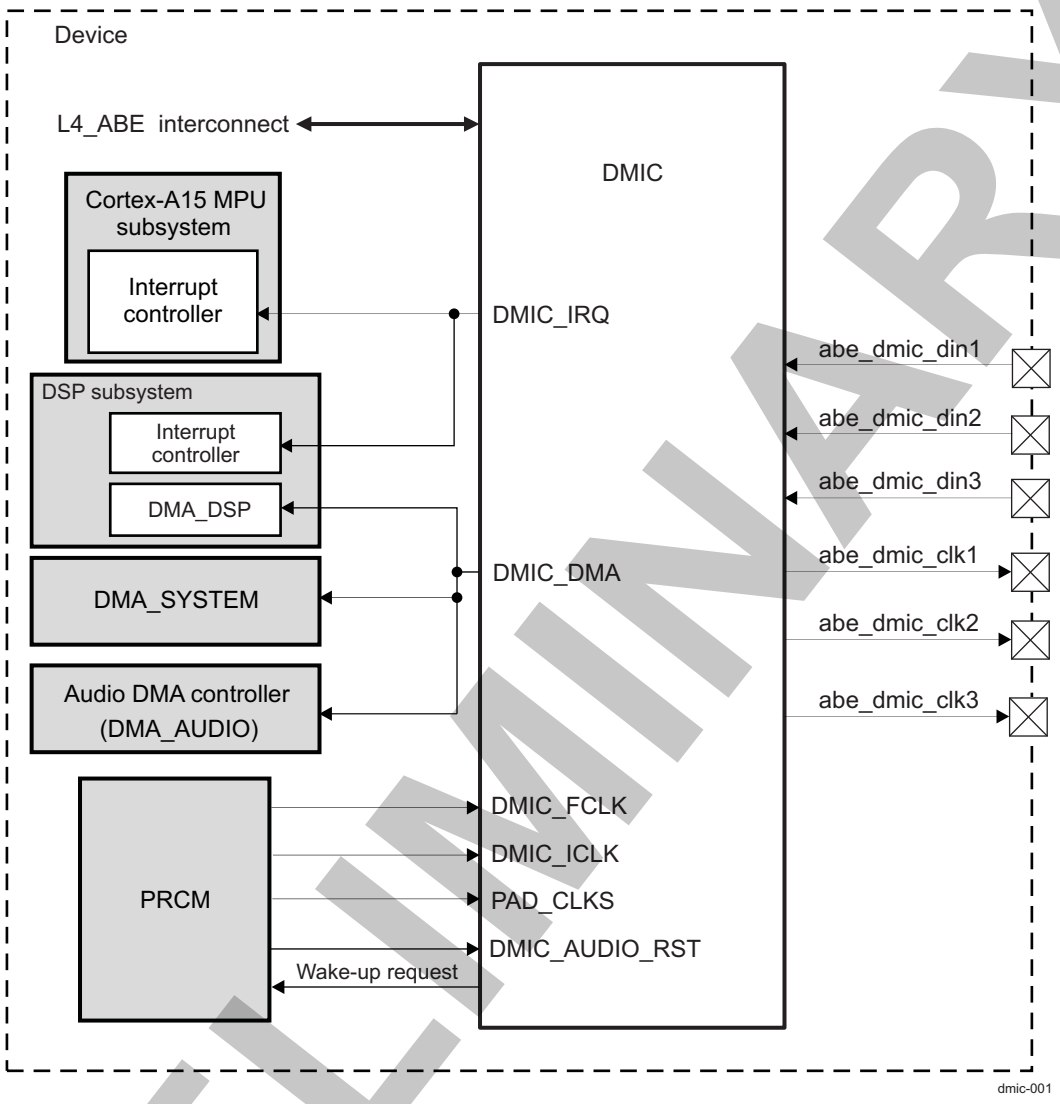
Figure 23-157. DMIC



The main features of the DMIC are:

- Six external pin connections (three data lines and three clock lines)
- Using the three clock lines, the DMIC delivers three clock signals (same frequency, individually gateable) for all digital microphones.
- Using the three data lines, the DMIC receives audio data from external microphones.
- Supports stereo (up to three) and mono (up to six) digital microphones
- Each line can support two microphones working in clock phase opposition.
- Selectable functional clock source
- Programmable output clock frequency (32 × FS, 50 × FS, 64 × FS, or 80 × FS, where FS = 48 kHz)
- Programmable data sampling sensibility (rising or falling edge)
- One RX FIFO (16 words of 144 bits)
- Supports IDLE request/acknowledge power, reset, and clock management (PRCM) module protocol
- Interconnect sample format: 32 bits (only 24 are significant)
- One IRQ to the microprocessor unit (Cortex™-A15 microprocessor unit [MPU]) and digital signal processor (DSP) subsystems
- One DMA request capability on programmable FIFO threshold

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23.7.2 DMIC Environment

This section describes the DMIC application fields from an environment point of view (that is, external connections). It presents the DMIC connectivity options, lists possible interfaces, and details the protocol and data format used in each case.

23.7.2.1 DMIC Interface With External MIC

23.7.2.1.1 DMIC Interface Overview

The DMIC interface is a 6-wire interface. The DMIC can support up to three external stereo and six mono digital microphones. A DMIC is an external module that can deliver data. A clock is sent from the host to the microphone.

Figure 23-158 and Figure 23-159 show two cases of use of the DMIC, but all configurations are possible with stereo and mono digital microphones. The output of the DMIC is in 32-bit format.

Figure 23-158 shows the DMIC used with three stereo DMICs.

Figure 23-158. DMIC With Three Stereo DMICs

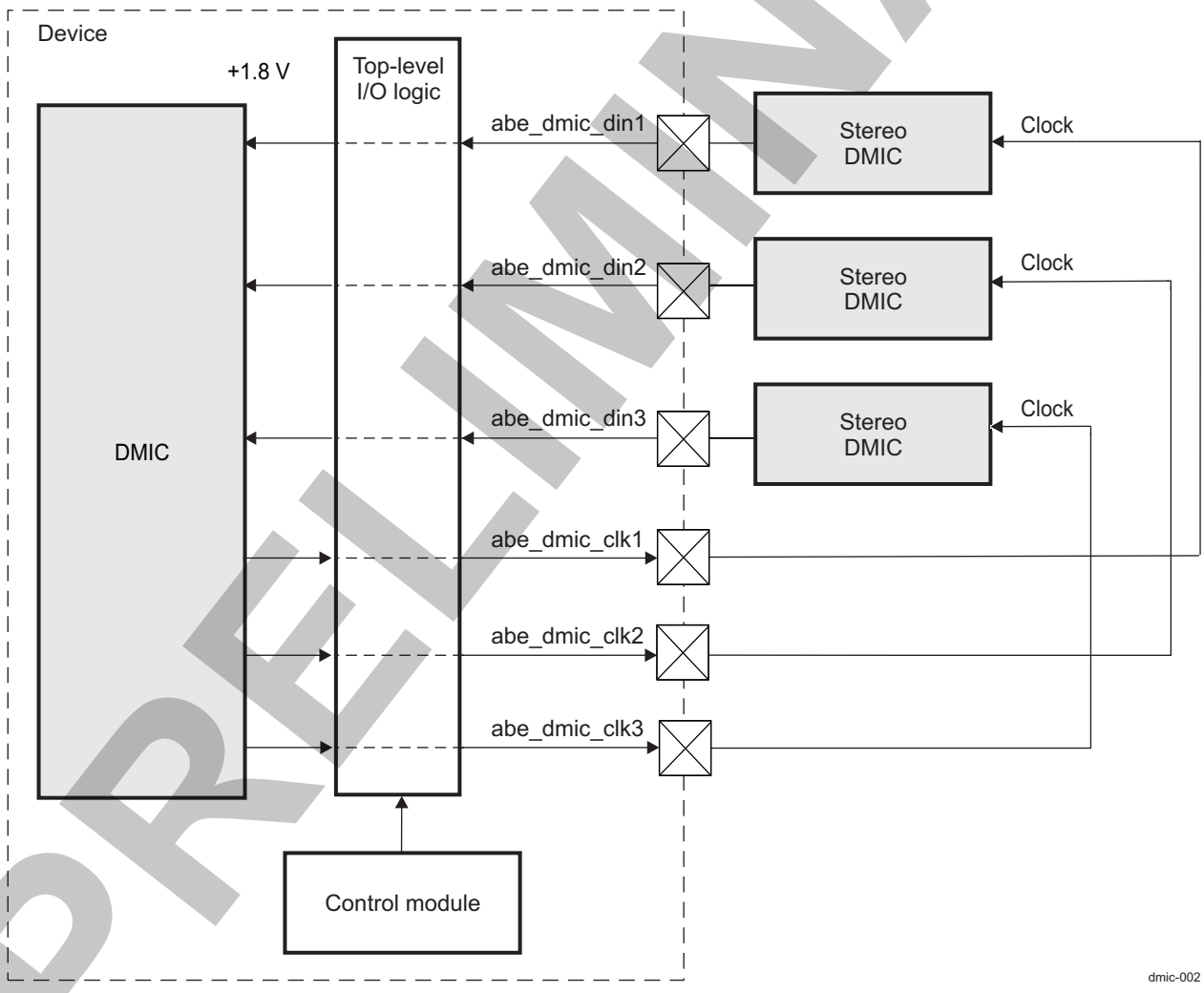

Figure 23-159 shows the DMIC used with six mono DMICs.

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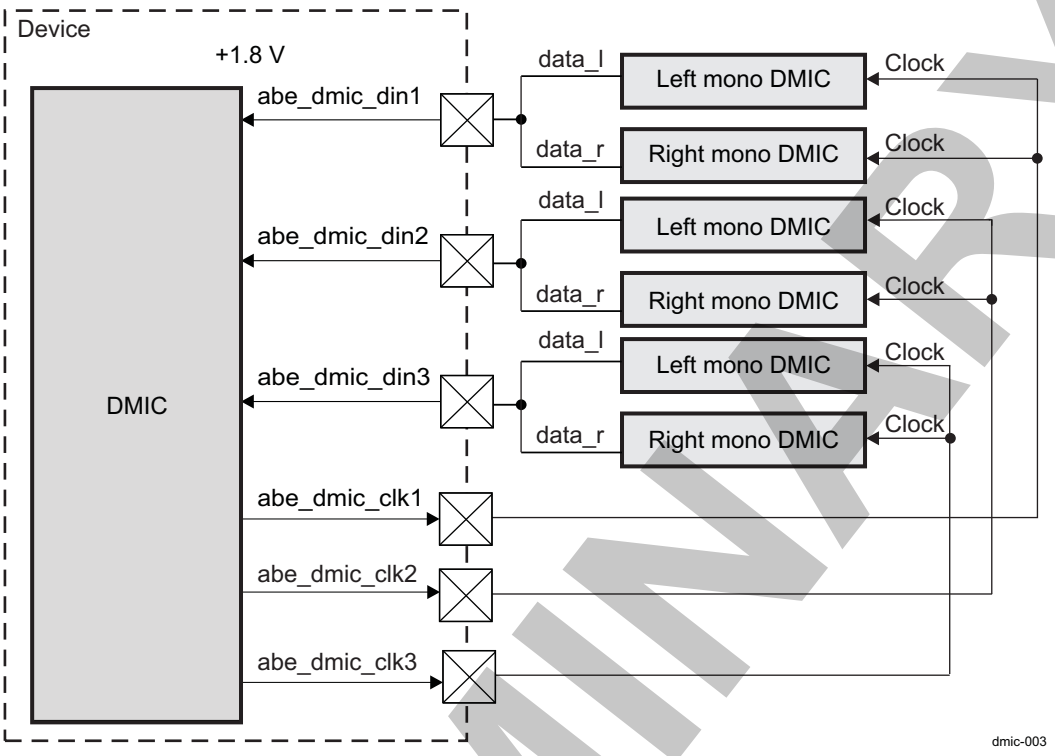
Figure 23-159. DMIC With Six Mono DMICs



23.7.2.1.2 DMIC Signals

Table 23-506 describes the signals in the DMIC.

Table 23-506. Input/Output

Signal Name	I/O[1]	Description	Reset Value[2]
abe_dmic_clk1	O	Digital (stereo) microphone clock output 1	Hi-Z
abe_dmic_clk2	O	Digital (stereo) microphone clock output 2	Hi-Z
abe_dmic_clk3	O	Digital (stereo) microphone clock output 3	Hi-Z
abe_dmic_din1	I	Digital (stereo) microphone data input 1	Hi-Z
abe_dmic_din2	I	Digital (stereo) microphone data input 2	Hi-Z
abe_dmic_din3	I	Digital (stereo) microphone data input 3	Hi-Z

(1) I = Input; O = Output; I/O = Bidirectional
(2) Hi-Z = High impedance

NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The control module registers assign the specific function to the device pads. For more information on control module settings, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, of *Chapter 18, Control Module*.

All DMIC external connections have pullup or pulldown resistors, selected and configured in the control module registers.

23.7.2.1.3 Serial Data Format

The DMIC generates a PDM stream of bits and transfers it in one period or one half-period of the clock. Then, the filter decimator extracts the 24-bit audio samples.

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23.7.2.1.3.1 DMIC Clock Generation and Synchronization

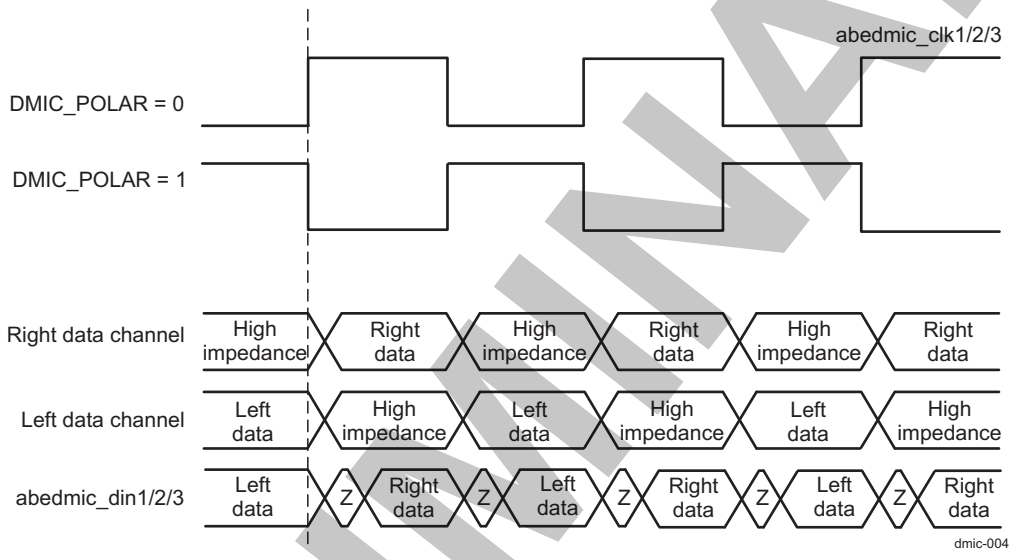
When the DMIC_POLAR bit is set to 0, the microphone left data is generated on the abe_dmic_clk low level. When DMIC_POLAR is set to 1, the microphone left data is generated on the abe_dmic_clk high level. There are three DMIC_POLARx bits (where x = 1, 2, or 3) corresponding to the three stereo paths:

- DMIC_CTRL[4] for path 1
- DMIC_CTRL[5] for path 2
- DMIC_CTRL[6] for path 3

The DMIC_POLARx bits are set depending on the configuration of the external digital microphone.

Figure 23-160 is a diagram of the DMIC interface with a DMIC.

Figure 23-160. DMIC Interface Diagram With External DMICs



23.7.2.2 DMIC Functional Path

The DMIC path processes, decimates, and filters the data from the DMIC interface, and stores the processed data in the FIFO. The FIFO is controlled by IRQ and DMA requests and is fed outside of the DMIC.

For more information about microphone data processing, see Section 23.7.4.7, *Audio Data Processing*.

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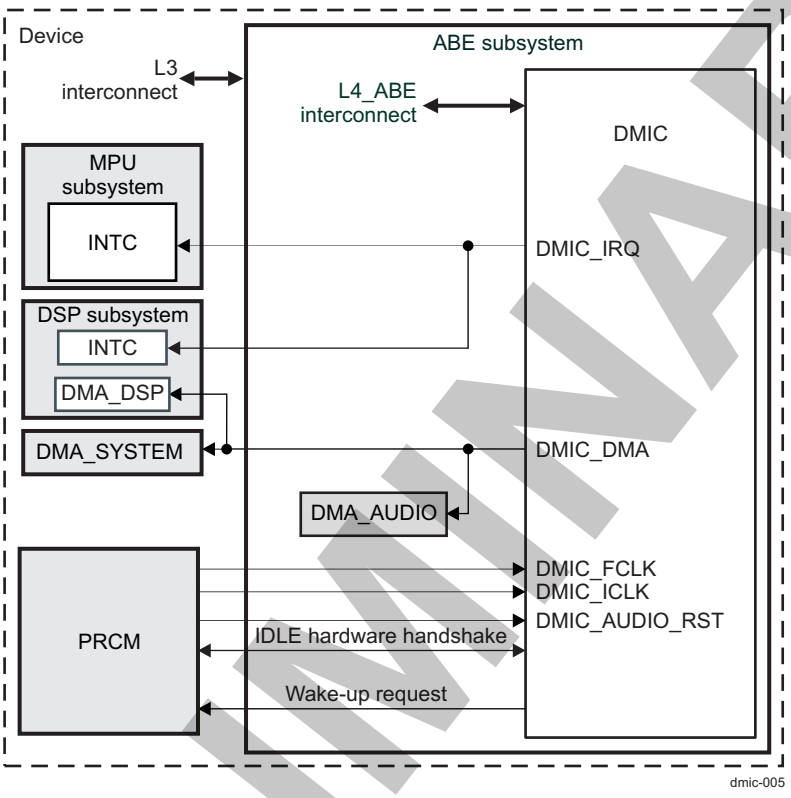
23.7.3 DMIC Integration

This section describes the integration of the DMIC in the device, and includes information about clocks, resets, and hardware requests.

Figure 23-161 shows the DMIC integration.

Figure 23-161. DMIC Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Chapter 3, *Power, Reset, and Clock Management*.

The DMIC integration includes:

- One functional clock
- One interface clock
- One IRQ
- One DMA_SYSTEM/DMA_AUDIO/DMA_DSP request
- IDLE hardware handshake
- Wake-up request

Table 23-507 through Table 23-509 summarize the integration of the module in the device.

Table 23-507. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
DMIC	PD_AUDIO	Yes	L4_ABE

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Table 23-508. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMIC	DMIC_ICLK	ABE_GICLK	PRCM	Interface clock
	DMIC_FCLK	DMIC_GFCLK	PRCM	Functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DMIC	DMIC_AUDIO_RST	AUDIO_RST	PRCM	Module hardware reset, nonretention

Table 23-509. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DMIC	DMIC_IRQ	DSP_IRQ_83	DSP	DMIC interrupt to the DSP subsystem
	DMIC_IRQ	MPU_IRQ_114	Cortex™-A15 MPU	DMIC interrupt to the Cortex-A15 MPU subsystem
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
DMIC	DMIC_DMA	DMA_SYSTEM_DREQ_66	DMA_SYSTEM	DMA request to the system DMA (DMA_SYSTEM)
	DMIC_DMA	DMA_AUDIO_DREQ_1	DMA_AUDIO	DMA request to the audio DMA (aDMA)
	DMIC_DMA	DMA_DSP_DREQ_44	DMA_DSP	DMA request to the DSP DMA (eDMA)

NOTE:

- For a description of the interrupt source, see Section 23.7.4.5, *Interrupt Requests*.
- For a description of the DMA source, see Section 23.7.4.6, *DMA Requests*.
- For information about PRCM clock gating and management and PRCM reset sources and distribution, see Chapter 3, *Power, Reset, and Clock Management*.

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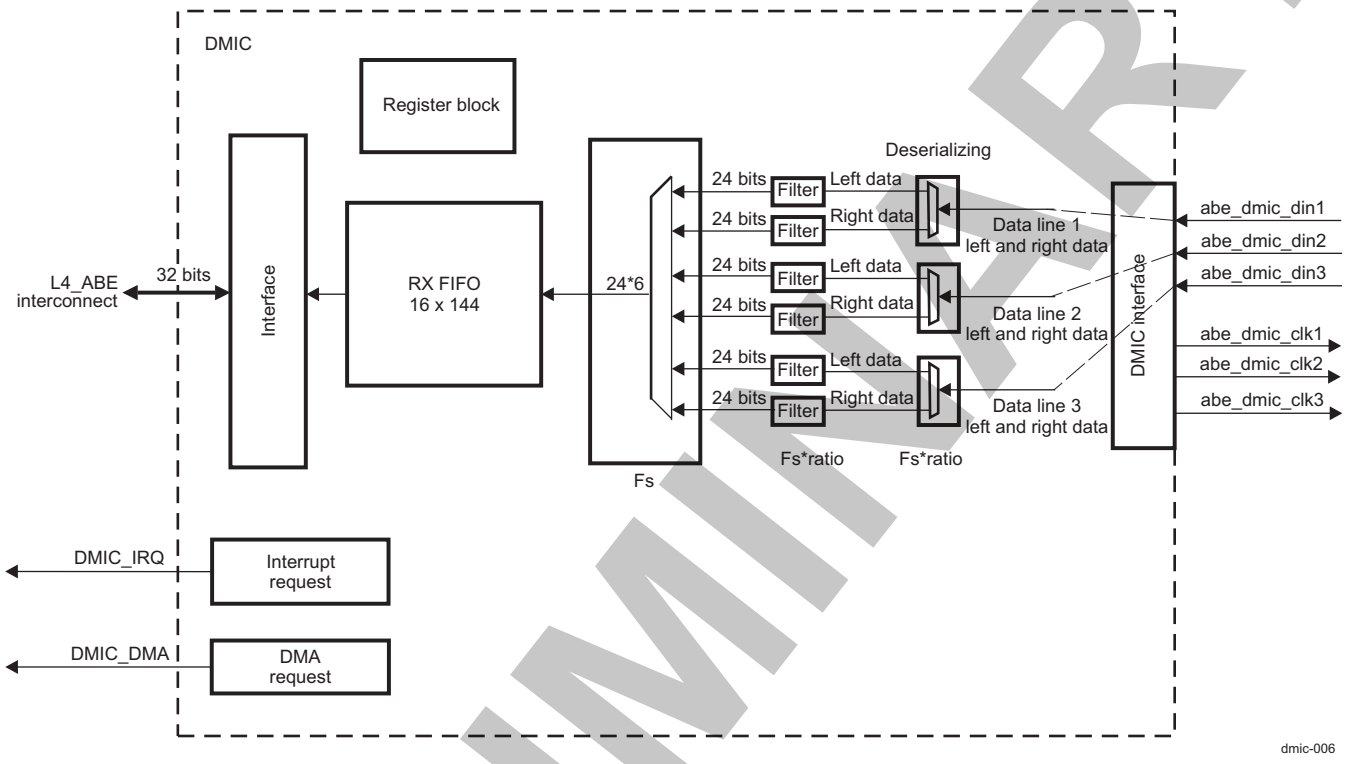
23.7.4 DMIC Functional Description

23.7.4.1 Block Diagram

Figure 23-162 is the DMIC block diagram.

Figure 23-162. DMIC Block Diagram

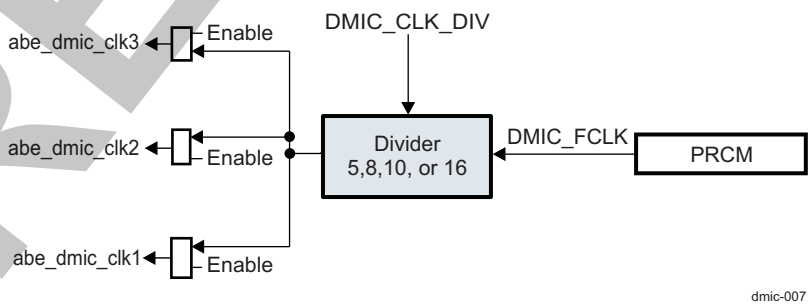


23.7.4.2 DMIC Clock Configuration

The DMIC operates from one interface clock to interface with the L4_ABE interconnect and one selectable (among three) functional clock. These clocks are provided by the PRCM module. For the interface clock, request and acknowledge are set up between the PRCM module and the DMIC.

Figure 23-163 shows the DMIC clock selection.

Figure 23-163. DMIC Clock Selection



DMIC_FCLK is the source clock signal. Several source clocks are available and are selected according to the configuration of the DMIC_CTRL[9:7] DMIC_CLK_DIV bit field. For more information about DMIC_FCLK selection, see Figure 23-163. abe_dmic_clkx are the output clocks generated in the DMIC and are fed to the external microphones. They are also the internal clocks of the external microphones. The performance in terms of signal-to-noise ratio (SNR) depends on these clocks. Users must take care

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about the value of abe_dmic_clkx (the analog-to-digital converter [ADC] clock) when selecting the source clock (DMIC_FCLK). FS is the output sample rate from DMIC. For example, when DMIC_FCLK = 19.2 MHz and DMIC_CTRL[9:7] DMIC_CLK_DIV = 000, the Ratio is 25, DMIC is providing a 96-KHz sampling rate to the Audio Engine Subsystem or DMA_SYSTEM. Table 23-510 describes the abe_dmic_clkx generation.

Table 23-510. abe_dmic_clkx Generation

DMIC_FCLK	DMIC_ CLK_DIV	Ratio DMIC_FCLK/ abe_dmic_clk	abe_dmic_clk = ADC Clock	FS	Ratio = abe_dmic_clk/FS = 96 kHz
19.2/17.64 MHz	000	8	2.4/2.205 MHz	96/88.2 kHz	25
	001	5	3.84/3.528 MHz	96/88.2 kHz	40
19.2 MHz	110	5	3.84 MHz	192 kHz	20
24 MHz	010	10	2.4 MHz	96 kHz	25
24.576 MHz	011	8	3.072 MHz	96 kHz	32
	100	16	1.536 MHz	96 kHz	16
12 MHz	101	5	2.4 MHz	96 kHz	25

The maximum clock on the interface is 3.84 MHz, with a source clock of 19.2 MHz.

23.7.4.3 DMIC Software Reset

Table 23-511 lists the different types of software reset available at the module level.

Table 23-511. Reset Description

Type	Name	Source	Description
Software	DMIC_SYSCONFIG[1] SOFTRESET	–	Module software reset
Software	DMIC_CTRL[10] SW_DMIC_RST	–	Reset-enabled DMIC paths

The software path reset is gated by:

- DMIC_CTRL[0] DMIC_UP1_EN for path 1
- DMIC_CTRL[1] DMIC_UP2_EN for path 2
- DMIC_CTRL[2] DMIC_UP3_EN for path 3
- DMIC_CTRL[10] SW_DMIC_RST

When the DMIC_CTRL[10] SW_DMIC_RST bit is set to 1, the corresponding enabled DMIC paths are reset. Resets are cleared by writing 0.

NOTE: A software reset is required to change the configuration of enabled paths; for example, to disable path 3, a software reset of path 3 is mandatory for the change to be considered.

A module software reset can be performed by setting the DMIC_SYSCONFIG[1] SOFTRESET bit. This action starts a soft reset sequence.

The software reset status of the module can be checked by reading the DMIC_SYSCONFIG[0] SOFTRESET bit (0: reset is done; 1: reset is ongoing).

23.7.4.4 DMIC Power Management

Table 23-512 describes the power-management features available for the DMIC.

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Table 23-512. Local Power-Management Features

Feature	Registers	Description
Clock autogating	N/A	Feature not available
Slave idle modes	DMIC_SYSCONFIG[3:2] SIDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup capable modes are available.
Clock activity	N/A	Feature not available
Master standby modes	N/A	Feature not available
Global wake-up enable	N/A	Feature not available
Wake-up sources enable	DMIC_IRQWAKEEN[0] IRQ_WAKEUP_EN DMIC_DMAWAKEEN[0] DMA_WAKEUP_EN	This register holds one active-high enable bit per event source that can generate a wake-up signal.

23.7.4.5 DMIC Interrupt Requests

Table 23-513 lists the event flags, and their mask, that can cause module interrupts.

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Table 23-513. Interrupt Events

Nonmaskable Event Flag[1]	Maskable Event Flag	Event Mask Bit	Event Unmask Bit	Description
DMIC_IRQSTATUS_RAW[3] DMIC_IRQ_EMPTY	DMIC_IRQSTATUS[3] DMIC_IRQ_EMPTY	DMIC_IRQENABLE_CLR[3] DMIC_IRQ_EMPTY_MASK	DMIC_IRQENABLE_SET[3] DMIC_IRQ_EMPTY_MASK	FIFO empty event. This event occurs when the FIFO is already empty and a new word is read from the FIFO by software.
DMIC_IRQSTATUS_RAW[2] DMIC_IRQ_ALST_FULL	DMIC_IRQSTATUS[2] DMIC_IRQ_ALST_FULL	DMIC_IRQENABLE_CLR[2] DMIC_IRQ_ALST_FULL_MASK	DMIC_IRQENABLE_SET[2] DMIC_IRQ_ALST_FULL_MASK	FIFO almost-full event. This event occurs when the FIFO contains (FIFO size – 1) words and a new word is written to the FIFO.
DMIC_IRQSTATUS_RAW[1] DMIC_IRQ_FULL	DMIC_IRQSTATUS[1] DMIC_IRQ_FULL	DMIC_IRQENABLE_CLR[1] DMIC_IRQ_FULL_MASK	DMIC_IRQENABLE_SET[1] DMIC_IRQ_FULL_MASK	FIFO full event. This event occurs when the FIFO is already full and a new word is written to the FIFO.
DMIC_IRQSTATUS_RAW[0] DMIC_IRQ	DMIC_IRQSTATUS[0] DMIC_IRQ	DMIC_IRQENABLE_CLR[0] DMIC_IRQ_MASK	DMIC_IRQENABLE_SET[0] DMIC_IRQ_MASK	FIFO read request event. This event occurs when the number of words stored in the FIFO is equal to or greater than the FIFO threshold.

(1) The DMIC_IRQSTATUS_RAW register is used primarily for debug purposes.

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The interrupt line is asserted (active high) when one of the following signals appears:

- DMIC_IRQ_EMPTY
- DMIC_IRQ_ALST_FULL
- DMIC_IRQ_FULL
- DMIC_IRQ

Read the DMIC_IRQSTATUS register to determine which event occurred.

CAUTION

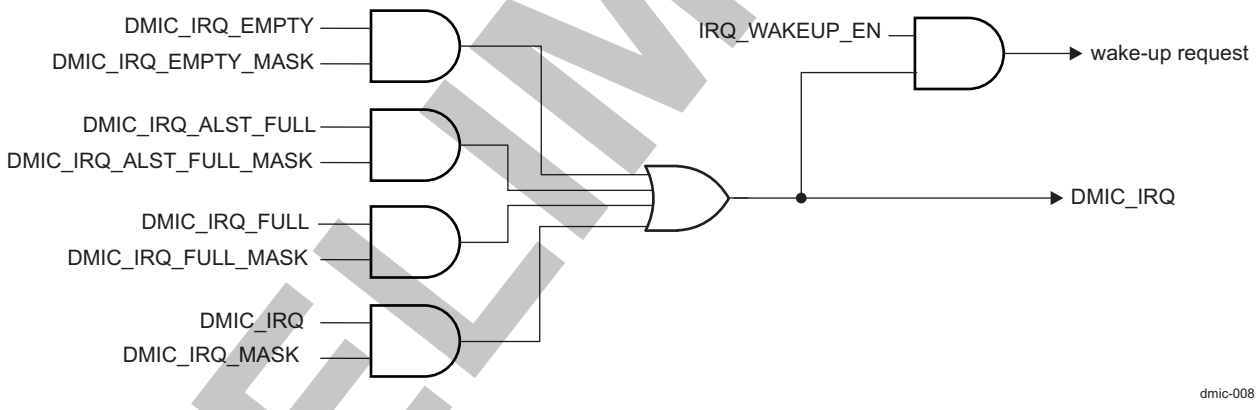
Interrupt lines must be cleared by software. Write 1 in the DMIC_IRQSTATUS register to clear the corresponding event.

An event can generate an IRQ when the corresponding mask bit in the DMIC_IRQENABLE_SET register is set to 1. Events are register bits that belong to the DMIC_IRQSTATUS and DMIC_IRQSTATUS_RAW registers (the same register accessed by two interconnect addresses). In the case of the DMIC_IRQSTATUS_RAW register, status event is set even if it is not enabled (used primarily for debug purposes). The DMIC_IRQSTATUS register is set by writing 1 to the DMIC_IRQSTATUS_RAW register.

Each internal interrupt signal can be masked by enabling the corresponding mask in the DMIC_IRQENABLE_SET register or disabling it in the DMIC_IRQENABLE_CLR register. This mechanism is defined in Section 23.7.6, *DMIC Register Manual*.

Figure 23-164 shows the interrupt tree with the event generated and the mask that enables or disables the event. All events are summarized to give the single interrupt generation.

Figure 23-164. Interrupt Tree



23.7.4.6 DMIC DMA Requests

The DMIC can generate one DMA request to the DMA_SYSTEM, DMA_AUDIO, and DMA_DSP controllers (see Table 23-514).

Table 23-514. DMIC DMA Request

Name	Description	Enable DMA Bit	Disable DMA Bit
DMIC_DMA_ENABLE	Data ready in FIFO (threshold is reached)	DMIC_DMAENABLE_SET[0] DMA_ENABLE	DMIC_DMAENABLE_CLR[0] DMA_ENABLE

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The DMA lines can be enabled or disabled depending on the value of the bits in the DMIC_DMAENABLE_SET and DMIC_DMAENABLE_CLR registers, respectively.

A DMA request is sent when data is ready in the FIFO. This request is used only to notify the host that data are ready in the FIFO.

23.7.4.7 Audio Data Processing

The DMIC supports six audio paths and can be used with three stereo or six mono microphones. Each path is independent and is enabled or disabled by using the following bits:

- DMIC_CTRL[0] DMIC_UP1_EN
- DMIC_CTRL[1] DMIC_UP2_EN
- DMIC_CTRL[2] DMIC_UP3_EN

23.7.4.7.1 Filtering

The external DMIC generates a PDM stream of bits and transfers it in one period or one half-period of the clock provided by the DMIC inside the device. The aim of the DMIC audio path is to process data from the DMIC interface, decimate and filter the data, and store the processed data in the FIFO.

The format of the DMIC data is 24 bits (the transfer format is 32 bits long). The following bits allow switching the polarity of the interface:

- DMIC_CTRL[4] DMIC_POLAR1
- DMIC_CTRL[5] DMIC_POLAR2
- DMIC_CTRL[6] DMIC_POLAR3

For more information, see Section 23.7.2.1.3.1, *DMIC Clock Generation and Synchronization*.

Processed data from the DMIC interface are stored in the FIFO. The FIFO is controlled by the IRQ and DMA request and externally fed by the DMIC using the following interconnect format.

The three uplink paths are identical. Each uplink path is composed of a left and a right channel. The DMIC interface delivers six parallel data of 1 bit (3 × 2 paths of stereo data that can be used at six mono paths). Each bit goes to a filter. The aim of the filter is to limit the noise and perform decimation by factor D. Factor D depends on the DMIC_CLK_DIV register bits, as described in the ratio defined in Table 23-510. The filters are sinc filter order 4. They are chosen with regard to the nature of the analog converter.

The format of the filter output is 24 bits.

23.7.4.8 FIFO Management

The DMIC implements an internal FIFO controlled by IRQ and DMA request. The host must read words in the FIFO. The interrupt line is used not only to inform the host that data are ready in the FIFO, but also to warn the host about events that can occur, such as FIFO full, almost full, or empty. A DMA request is used only to inform the host that data are ready in the FIFO.

23.7.4.8.1 FIFO General Description

The DMIC communicates with the host through L4_ABE interconnect access. DMIC audio data coming from external microphones are stored in the FIFO. The DMIC FIFO allows the exchange of information between the DMIC and the host. Each audio data is 24 bits long. The DMIC FIFO contains 16 words. Each word is the combination of six audio data (24 × 6 = 144 bits) coming from the interface. The FIFO is controlled by interrupt lines and DMA requests. For more information about IRQs and DMA controls, see Section 23.7.4.5, *DMIC Interrupt Requests*, and Section 23.7.4.6, *DMIC DMA Requests*.

FIFO write access is done in the functional clock domain, and read access is done in the interface clock domain.

Figure 23-165 is an overview of the DMIC FIFO.

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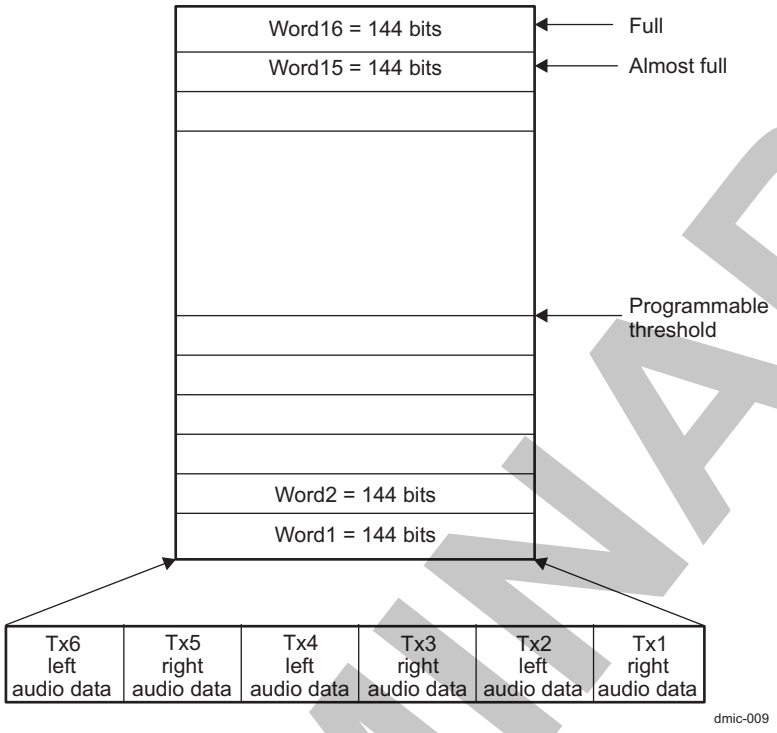
Figure 23-165. DMIC FIFO



23.7.4.8.2 FIFO Operations

Audio data are filled in the FIFO from DMIC internal filters. The host must read words in the FIFO. The number of reads depends on the application that is configured by the following bits:

- DMIC_CTRL[0] DMIC_UP1_EN
- DMIC_CTRL[2] DMIC_UP3_EN
- DMIC_CTRL[1] DMIC_UP2_EN
- DMIC_FIFO_CTRL[3:0] DMIC_TRESH (FIFO threshold)

If only uplink path 2 and path 3 are enabled, for example, the Tx1 and Tx2 words are left and right data for path 2, and Tx3 and Tx4 are left and right data for path 3.

When the FIFO threshold is reached, and depending on conditions, an event is sent to the DMA handler. The host must read the exact number of words in the FIFO.

Two accesses are required to read a complete stereo audio path.

The number of read accesses from the host is determined by the following equation:

Num_rd_access = (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 2 × (DMIC_TRESH)

The FIFO threshold is programmed through the DMIC_FIFO_CTRL[3:0] DMIC_TRESH bit field.

NOTE: If DMIC_TRESH = 1, the host is expected to perform 1 × (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 2 read access every 96 kHz (2 × FS).

If DMIC_TRESH = 2, the host is expected to perform (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 4 read access every 48 kHz (FS).

If DMIC_TRESH = 12, the host is expected to perform (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 12 read access every 8 kHz (FS/6).

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23.7.4.8.3 FIFO Output Range Definition

The DMIC_CTRL[3] DMICOUTFORMAT bit allows determining the format of the output of the DMIC uplink module.

When DMICOUTFORMAT = 0, the data going from the FIFO are left-shifted by 8 bits. When DMICOUTFORMAT = 1, the data are signed-extended on 32 bits.

The DMIC uplink modules process audio data based on twos complement format.

NOTE: When DMICOUTFORMAT = 0, the maximum positive swing analog voltage corresponds to a final DMIC output of 0x7FFF FF00. The maximum negative swing analog voltage corresponds to a final DMIC output of 0x8000 0000.

When DMICOUTFORMAT = 1, the sign is extended: The maximum positive swing analog voltage corresponds to a final DMIC output of 0x007F FFFF. The maximum negative swing analog voltage corresponds to a final DMIC output of 0xFF80 0000.

Reading the value of the corresponding audio data in the FIFO requires access to the DMIC_DATA_REG register. The first access gives the value of Tx1 right data, the second gives the value of Tx2 left data, up to Tx6 (the left audio data of the last audio path). If the path is disabled, 0x0 is read. All data are duplicated (for debug purposes) in their corresponding left or right data registers. Table 23-515 describes the audio data path registers.

Table 23-515. Audio Data Path Registers

Stereo Audio Path	Mono Audio Path	Data Register
Right path 1	Mono path 1	DMIC_FIFO_DMIC1R_DATA[23:0]
Left path 1	Mono path 2	DMIC_FIFO_DMIC1L_DATA[23:0]
Right path 2	Mono path 3	DMIC_FIFO_DMIC2R_DATA[23:0]
Left path 2	Mono path 4	DMIC_FIFO_DMIC2L_DATA[23:0]
Right path 3	Mono path 5	DMIC_FIFO_DMIC3R_DATA[23:0]
Left path 3	Mono path 6	DMIC_FIFO_DMIC3L_DATA[23:0]

The output of the DMIC path for interconnect access is in 32-bit format.

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23.7.5 DMIC Programming Guide

23.7.5.1 DMIC Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

23.7.5.1.1 Global Initialization

23.7.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the DMIC is used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the DMIC. For more information, see Section 23.7.3, *DMIC Integration*, and Section 23.7.2, *DMIC Environment*.

Table 23-516 describes the global initialization of surrounding modules.

Table 23-516. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. See Chapter 3, *Power, Reset, and Clock Management*.
Control module	Module-specific pad muxing must be set in the control module. See Chapter 18, *Control Module*.
(optional) Cortex-A15 MPU interrupt controller (INTC) (or DSP INTC)	INTC configuration must be done to enable the interrupts from the DMIC. See Chapter 17, *Interrupt Controllers*.
(optional) DMA_SYSTEM (or DMA_DSP or DMA_AUDIO)	DMA configuration must be done to enable the DMIC DMA channel requests.
(optional) Interconnect	For more information about the interconnect configuration, see Chapter 14, *Interconnect*.

NOTE: The INTC and DMA configurations are necessary if the interrupt and DMA-based communication modes are used.

23.7.5.1.2 DMIC Global Initialization

23.7.5.1.2.1 Main Sequence – DMIC Global Initialization

The procedure in Table 23-517 initializes the DMIC after a power-on reset (POR).

Table 23-517. DMIC Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute a software reset.	DMIC_SYSCONFIG[0] SOFTRESET	0x1
Wait for the software reset completion by polling.	DMIC_SYSCONFIG[0] SOFTRESET	==0x0
Configure the local power management.	DMIC_SYSCONFIG[3:2] SIDLEMODE	0x-
Select the DMIC FIFO threshold.	DMIC_FIFO_CTRL[3:0] DMIC_TRESH	0x-
Select the DMIC output clock frequency.	DMIC_CTRL[9:7] DMIC_CLK_DIV	0x-
Select the DMIC FIFO data output format.	DMIC_CTRL[3] DMICOUTFORMAT	0x-
Select the level (high or low) of the clock signal abe_dmic_clki when the left data is to be generated (extracted) from the external microphone i (where i = 1 to 3).	DMIC_CTRL[j] DMIC_POLARi (where j = 4 to 6, and i = 1 to 3)	0x-
Enable audio path i (where i = 1 to 3).	DMIC_CTRL[k] DMIC_POLARi (where k = 0 to 2, and i = 1 to 3)	0x1

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23.7.5.1.2 Operational Mode Configuration

23.7.5.1.2.1 DMIC Polling Mode

Figure 23-166 shows the polling mode. Table 23-518 summarizes the register calls for the polling mode. For the number of read accesses used while reading the received audio data, see Section 23.7.4.8, *FIFO Management*.

Figure 23-166. Polling Mode

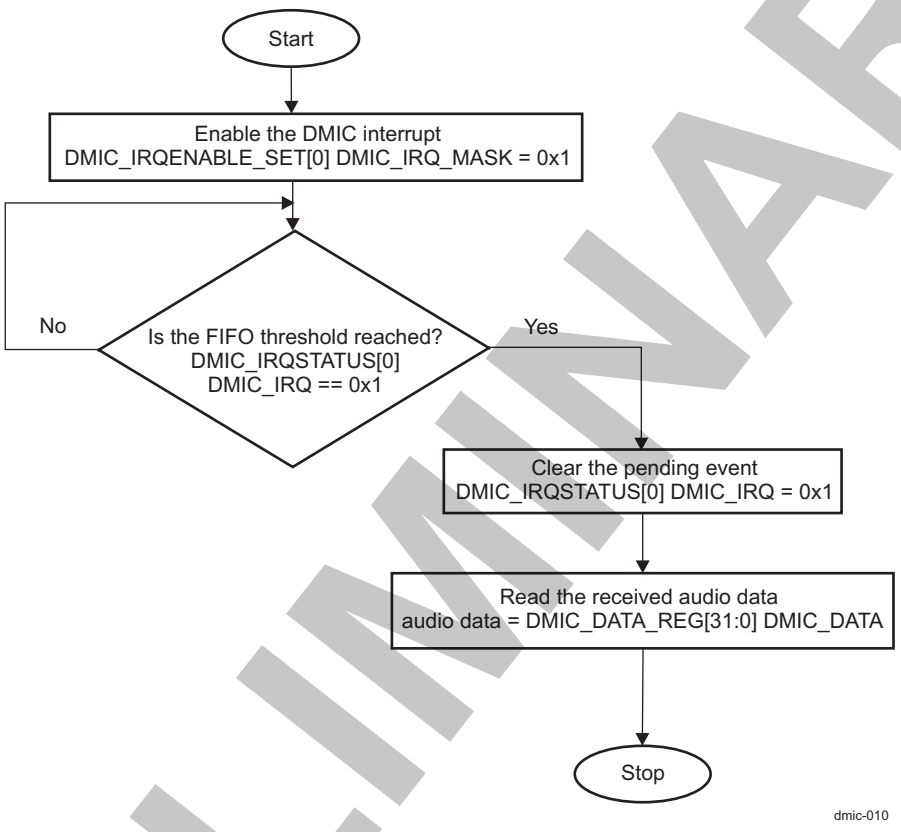

Table 23-518. Register Call Summary for Polling Mode

Register Name	Register Name	Register Name
DMIC_IRQENABLE_SET	DMIC_IRQSTATUS	DMIC_DATA_REG

23.7.5.1.2.2 DMIC Interrupt Mode

Table 23-519 lists the procedure to initialize interrupt mode.

Table 23-519. Interrupt Mode

Step	Register/Bit Field/Programming Model	Value
Enable the DMIC interrupts.	DMIC_IRQENABLE_SET[3:0]	0xF

23.7.5.1.2.3 DMIC DMA Mode

Table 23-520 lists the procedure to initialize DMA mode.

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Table 23-520. DMA Mode

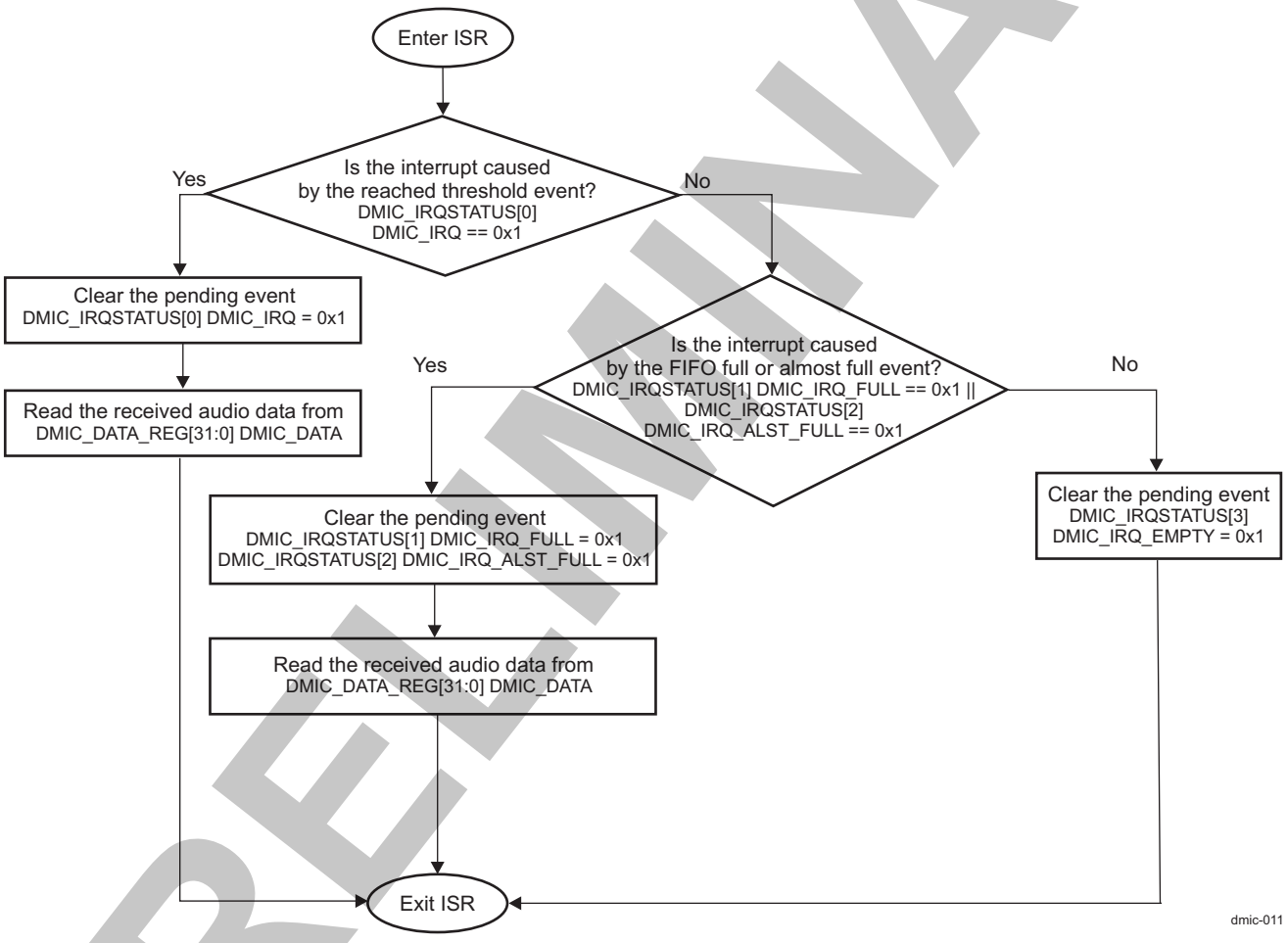
Step	Register/Bit Field/Programming Model	Value
Enable the DMIC DMA interrupt event.	DMIC_DMAENABLE_SET[0] DMA_ENABLE	0x1

23.7.5.1.3 DMIC Events Servicing

23.7.5.1.3.1 DMIC Interrupt Servicing

This section describes the interrupt event servicing of the module. Figure 23-167 shows the interrupt handler.

Figure 23-167. Interrupt Handler



When the interrupt is caused by the reached threshold event, for the number of read accesses used while reading the received audio data, see Section 23.7.4.8, *FIFO Management*.

When the interrupt is caused by a FIFO full or almost-full event, software must read all the available data in the FIFO. If a FIFO full event occurred, the number of read accesses must be the maximum:

Num_rd_access = (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 2 × 15

If a FIFO almost-full event occurred, the number of read accesses must be:

Num_rd_access = (DMIC_UP1_EN + DMIC_UP2_EN + DMIC_UP3_EN) × 2 × 14

Table 23-521 summarizes the register call for the interrupt handler.

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Table 23-521. Register Call Summary for the Interrupt Handler

Register Name	Register Name
DMIC_IRQSTATUS	DMIC_DATA_REG

23.7.6 DMIC Register Manual

23.7.6.1 DMIC Instance Summary

Table 23-522 is the DMIC instance summary.

Table 23-522. DMIC Instance Summary

Module Name	Base Address L3 Interconnect	Base Address Cortex-A15 Private Access	Base Address DSP Private Access	Size
DMIC	0x4902 E000	0x4012 E000	0x2 E000	4 KiB

NOTE: Private access is an access that does not use the L3/L4 interconnects.

23.7.6.2 DMIC Registers

23.7.6.2.1 DMIC Register Summary

Table 23-523 summarizes the DMIC register mapping.

Table 23-523. DMIC Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-A15 Private Access	Physical Address DSP Private Access
DMIC_REVISION	R	32	0x0000 0000	0x4902 E000	0x4012 E000	0x2 E000
DMIC_SYSCONFIG	RW	32	0x0000 0010	0x4902 E010	0x4012 E010	0x2 E010
RESERVED	RW	32	0x0000 0020	0x4902 E020	0x4012 E020	0x2 E020
DMIC_IRQSTATUS_RAW	RW	32	0x0000 0024	0x4902 E024	0x4012 E024	0x2 E024
DMIC_IRQSTATUS	RW	32	0x0000 0028	0x4902 E028	0x4012 E028	0x2 E028
DMIC_IRQENABLE_SET	RW	32	0x0000 002C	0x4902 E02C	0x4012 E02C	0x2 E02C
DMIC_IRQENABLE_CLR	RW	32	0x0000 0030	0x4902 E030	0x4012 E030	0x2 E030
DMIC_IRQWAKEEN	RW	32	0x0000 0034	0x4902 E034	0x4012 E034	0x2 E034
DMIC_DMAENABLE_SET	RW	32	0x0000 0038	0x4902 E038	0x4012 E038	0x2 E038
DMIC_DMAENABLE_CLR	RW	32	0x0000 003C	0x4902 E03C	0x4012 E03C	0x2 E03C
DMIC_DMAWAKEEN	RW	32	0x0000 0040	0x4902 E040	0x4012 E040	0x2 E040
DMIC_CTRL	RW	32	0x0000 0044	0x4902 E044	0x4012 E044	0x2 E044
DMIC_DATA_REG	R	32	0x0000 0048	0x4902 E048	0x4012 E048	0x2 E048
DMIC_FIFO_CTRL	RW	32	0x0000 004C	0x4902 E04C	0x4012 E04C	0x2 E04C
DMIC_FIFO_DMIC1R_DATA	R	32	0x0000 0050	0x4902 E050	0x4012 E050	0x2 E050
DMIC_FIFO_DMIC1L_DATA	R	32	0x0000 0054	0x4902 E054	0x4012 E054	0x2 E054
DMIC_FIFO_DMIC2R_DATA	R	32	0x0000 0058	0x4902 E058	0x4012 E058	0x2 E058
DMIC_FIFO_DMIC2L_DATA	R	32	0x0000 005C	0x4902 E05C	0x4012 E05C	0x2 E05C
DMIC_FIFO_DMIC3R_DATA	R	32	0x0000 0060	0x4902 E060	0x4012 E060	0x2 E060
DMIC_FIFO_DMIC3L_DATA	R	32	0x0000 0064	0x4902 E064	0x4012 E064	0x2 E064

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23.7.6.2.2 DMIC Register Descriptions

Table 23-524 through Table 23-560 describe the DMIC registers.

Table 23-524. DMIC_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4902 E000 0x4012 E000 0x2 E000	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	IP revision identifier (X.Y.R) used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1).

(1) TI internal data

Table 23-525. Register Call Summary for Register DMIC_REVISION

Digital Microphone Module
- DMIC Register Summary: [0]

Table 23-526. DMIC_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4902 E010 0x4012 E010 0x2 E010	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	This register allows controlling various parameters of the DMIC interface.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												SIDLEMODE		FREEMU	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:2	SIDLEMODE	Configuration of the local target state management (idlereq/idleack control) 0x0: Force-idle. IDLE request is acknowledged unconditionally and immediately. 0x1: No-idle. IDLE request is never acknowledged. 0x2: Smart-idle. The acknowledgment to an IDLE request is given based on the internal activity. 0x3: Smart-idle wakeup capable mode	RW	0x2
1	FREEMU	Sensitivity to emulation (debug) suspend input signal 0x0: IP module is sensitive to emulation suspend. 0x1: IP module is not sensitive to emulation suspend.	RW	0

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Bits	Field Name	Description	Type	Reset
0	SOFTRESET	Module software reset. The bit is automatically reset by the hardware. It has same effect as the main hardware reset. Write 0x0: No action Read 0x0: Reset done, no pending action Read 0x1: Reset (software or other) ongoing Write 0x1: Initiate software reset.	RW	0

Table 23-527. Register Call Summary for Register DMIC_SYSCONFIG

Digital Microphone Module

- DMIC Software Reset: [0] [1] [2]
- DMIC Power Management: [3]
- DMIC Global Initialization: [4] [5] [6]
- DMIC Register Summary: [7]

Table 23-528. DMIC_IRQSTATUS_RAW

Address Offset	0x0000 0024		
Physical Address	0x4902 E024 0x4012 E024 0x2 E024	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Component (that is, main) interrupt request status. Check the corresponding secondary status register. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_IRQ_EMPTY	DMIC_IRQ_ALST_FULL	DMIC_IRQ_FULL	DMIC_IRQ

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	DMIC_IRQ_EMPTY	Read 0x0: No event pending Write 0x0: No action Write 0x1: Set Read 0x1: IRQ event pending	RW	0
2	DMIC_IRQ_ALST_FULL	Read 0x0: No event pending Write 0x0: No action Write 0x1: Set Read 0x1: IRQ event pending	RW W1toSet	0
1	DMIC_IRQ_FULL	Read 0x0: No event pending Write 0x0: No action Write 0x1: Set Read 0x1: IRQ event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
0	DMIC_IRQ	Read 0x0: No event pending Write 0x0: No action Write 0x1: Set Read 0x1: IRQ event pending	RW W1toSet	0

Table 23-529. Register Call Summary for Register DMIC_IRQSTATUS_RAW

Digital Microphone Module

- DMIC Interrupt Requests: [0] [1] [2] [3] [4] [5] [6]
- DMIC Register Summary: [7]

Table 23-530. DMIC_IRQSTATUS

Address Offset	0x0000 0028		
Physical Address	0x4902 E028 0x4012 E028 0x2 E028	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Component (that is, main) interrupt request status. Check the corresponding secondary status register. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_IRQ_EMPTY	DMIC_IRQ_ALST_FULL	DMIC_IRQ_FULL	DMIC_IRQ

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	DMIC_IRQ_EMPTY	Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending	RW	0
2	DMIC_IRQ_ALST_FULL	This interrupt status is set when only one FIFO space is still available. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending	RW W1toClr	0
1	DMIC_IRQ_FULL	This interrupt status is set when FIFO is full and a new write access has been performed by filter. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	DMIC_IRQ	This interrupt status is set when FIFO threshold value defined in DMIC_FIFO_CTRL is reached. Read 0x0: No event pending Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending	RW W1toClr	0

Table 23-531. Register Call Summary for Register DMIC_IRQSTATUS

Digital Microphone Module

- DMIC Interrupt Requests: [0] [1] [2] [3] [4] [5] [6] [7]
- DMIC Polling Mode: [8]
- DMIC Interrupt Servicing: [9]
- DMIC Register Summary: [10]

Table 23-532. DMIC_IRQENABLE_SET

Address Offset	0x0000 002C		
Physical Address	0x4902 E02C 0x4012 E02C 0x2 E02C	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Component (that is, main) interrupt request enable. Write 1 to set (enable interrupt). Readout equal to corresponding _SET register. _SET register is cleared when writing 1 to _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_IRQ_EMPTY_MASK	DMIC_IRQ_ALST_FULL_MASK	DMIC_IRQ_FULL_MASK	DMIC_IRQ_MASK

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	DMIC_IRQ_EMPTY_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1:	RW W1toSet	0
2	DMIC_IRQ_ALST_FULL_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW W1toSet	0
1	DMIC_IRQ_FULL_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
0	DMIC_IRQ_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW W1toSet	0

Table 23-533. Register Call Summary for Register DMIC_IRQENABLE_SET

Digital Microphone Module

- DMIC Interrupt Requests: [0] [1] [2] [3] [4] [5]
- DMIC Polling Mode: [6]
- DMIC Interrupt Mode: [7]
- DMIC Register Summary: [8]

Table 23-534. DMIC_IRQENABLE_CLR

Address Offset	0x0000 0030		
Physical Address	0x4902 E030 0x4012 E030 0x2 E030	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Component (that is, main) interrupt request enable. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register. _SET register is cleared when writing 1 to _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_IRQ_EMPTY_MASK	DMIC_IRQ_ALST_FULL_MASK	DMIC_IRQ_FULL_MASK	DMIC_IRQ_MASK

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	DMIC_IRQ_EMPTY_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0
2	DMIC_IRQ_ALST_FULL_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0
1	DMIC_IRQ_FULL_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
0	DMIC_IRQ_MASK	Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0

Table 23-535. Register Call Summary for Register DMIC_IRQENABLE_CLR

Digital Microphone Module
- DMIC Interrupt Requests: [0] [1] [2] [3] [4]
- DMIC Register Summary: [5]

Table 23-536. DMIC_IRQWAKEEN

Address Offset	0x0000 0034		
Physical Address	0x4902 E034 0x4012 E034 0x2 E034	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	This register allows to enable the wake-up capability on interrupt event.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															IRQ_WAKEUP_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	IRQ_WAKEUP_EN	Write 1 to allow wake-up by IRQ source (register threshold value reached).	RW	1

Table 23-537. Register Call Summary for Register DMIC_IRQWAKEEN

Digital Microphone Module
- DMIC Power Management: [0]
- DMIC Register Summary: [1]

Table 23-538. DMIC_DMAENABLE_SET

Address Offset	0x0000 0038		
Physical Address	0x4902 E038 0x4012 E038 0x2 E038	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Component DMA enable (1 bit per DMA-capable channel)/Write 1 to set (enable DMA). Readout equal to corresponding _SET register. _SET register is cleared when writing 1 to _CLR register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DMA_ENABLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DMA_ENABLE	Write 1 to set (enable DMA request) Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Enable interrupt Read 0x1: Interrupt enabled	RW W1toSet	0

Table 23-539. Register Call Summary for Register DMIC_DMAENABLE_SET

Digital Microphone Module
- DMIC DMA Requests: [0] [1]
- DMIC DMA Mode: [2]
- DMIC Register Summary: [3]

Table 23-540. DMIC_DMAENABLE_CLR

Address Offset	0x0000 003C		
Physical Address	0x4902 E03C 0x4012 E03C 0x2 E03C	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Component DMA enable (1 bit per DMA-capable channel)/Write 1 to clear (disable DMA). Readout equal to corresponding _SET register. _SET register is cleared when writing 1 to _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DMA_ENABLE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DMA_ENABLE	Write 1 to clear (disable DMA request) Read 0x0: Interrupt disabled Write 0x0: No action Write 0x1: Disable interrupt Read 0x1: Interrupt enabled	RW W1toClr	0

Table 23-541. Register Call Summary for Register DMIC_DMAENABLE_CLR

Digital Microphone Module
- DMIC DMA Requests: [0] [1]
- DMIC Register Summary: [2]

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Table 23-542. DMIC_DMAWAKEEN

Address Offset	0x0000 0040		
Physical Address	0x4902 E040 0x4012 E040 0x2 E040	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	This register allows to enable the wake-up capability on DMA request event.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															DMA_WAKEUP_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	DMA_WAKEUP_EN	Write 1 to allow wakeup by DMA source (register threshold value reached).	RW	1

Table 23-543. Register Call Summary for Register DMIC_DMAWAKEEN

Digital Microphone Module

- DMIC Power Management: [0]
- DMIC Register Summary: [1]

Table 23-544. DMIC_CTRL

Address Offset	0x0000 0044		
Physical Address	0x4902 E044 0x4012 E044 0x2 E044	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	This register configures the various parameters of the DMIC module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					SW_DMIC_RST	DMIC_CLK_DIV			DMIC_POLAR3	DMIC_POLAR2	DMIC_POLAR1	DMICOUTFORMAT	DMIC_UP3_EN	DMIC_UP2_EN	DMIC_UP1_EN

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10	SW_DMIC_RST	Software reset of the DMIC path. When 1, the DMIC path is reset. Clearing the reset is done by writing 0 to the register.	RW	0
9:7	DMIC_CLK_DIV	Select the DMIC output clock frequency. See Table 23-510 for details.	RW	0x0

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Bits	Field Name	Description	Type	Reset
6	DMIC_POLAR3	0x0: When 0, the left data is generated in the external microphone 3 on abe_dmic_clk3 low level. 0x1: When 1, the left data is generated in the external microphone 3 on abe_dmic_clk3 high level.	RW	0
5	DMIC_POLAR2	0x0: When 0, the left data is generated in the external microphone 2 on abe_dmic_clk2 low level. 0x1: When 1, the left data is generated in the external microphone 2 on abe_dmic_clk2 high level.	RW	0
4	DMIC_POLAR1	0x0: When 0, the left data is generated in the external microphone 1 on abe_dmic_clk1 low level. 0x1: When 1, the left data is generated in the external microphone 1 on abe_dmic_clk1 high level.	RW	0
3	DMICOUTFORMAT	When 0, the data going out from the FIFO are left-shifted from 8 bits. When 1, the data going are signed extended on 32 bits.	RW	0
2	DMIC_UP3_EN	When 1, uplink path 3 is powered up.	RW	0
1	DMIC_UP2_EN	When 1, uplink path 2 is powered up.	RW	0
0	DMIC_UP1_EN	When 1, uplink path 1 is powered up.	RW	0

Table 23-545. Register Call Summary for Register DMIC_CTRL

Digital Microphone Module

- DMIC Clock Generation and Synchronization: [0] [1] [2]
- DMIC Clock Configuration: [3] [4]
- DMIC Software Reset: [5] [6] [7] [8] [9] [10]
- Audio Data Processing: [11] [12] [13]
- Filtering: [14] [15] [16]
- FIFO Operations: [17] [18] [19]
- FIFO Output Range Definition: [20]
- DMIC Global Initialization: [21] [22] [23] [24]
- DMIC Register Summary: [25]

Table 23-546. DMIC_DATA_REG

Address Offset	0x0000 0048		
Physical Address	0x4902 E048 0x4012 E048 0x2 E048	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	DMIC FIFO data		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMIC_DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DMIC_DATA	DMIC FIFO data	R	0x000000

Table 23-547. Register Call Summary for Register DMIC_DATA_REG

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Polling Mode: [1]
- DMIC Interrupt Servicing: [2]
- DMIC Register Summary: [3]

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Table 23-548. DMIC_FIFO_CTRL

Address Offset	0x0000 004C		
Physical Address	0x4902 E04C 0x4012 E04C 0x2 E04C	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	This register sets the FIFO threshold for the data-ready event.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DMIC_TRESH			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000
3:0	DMIC_TRESH	Uplink FIFO threshold	RW	0x2

Table 23-549. Register Call Summary for Register DMIC_FIFO_CTRL

Digital Microphone Module

- FIFO Operations: [0] [1]
- DMIC Global Initialization: [2]
- DMIC Register Summary: [3]
- DMIC Register Descriptions: [4]

Table 23-550. DMIC_FIFO_DMIC1R_DATA

Address Offset	0x0000 0050		
Physical Address	0x4902 E050 0x4012 E050 0x2 E050	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Data of the first FIFO DMIC right channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC1R_DAT																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC1R_DAT	Data of the right FIFO DMIC path 1	R	0x000000

Table 23-551. Register Call Summary for Register DMIC_FIFO_DMIC1R_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

Table 23-552. DMIC_FIFO_DMIC1L_DATA

Address Offset	0x0000 0054		
Physical Address	0x4902 E054 0x4012 E054 0x2 E054	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Data of the first FIFO DMIC left channel		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC1R_DAT																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC1R_DAT	Data of the left FIFO DMIC path 1	R	0x000000

Table 23-553. Register Call Summary for Register DMIC_FIFO_DMIC1L_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

Table 23-554. DMIC_FIFO_DMIC2R_DATA

Address Offset	0x0000 0058		
Physical Address	0x4902 E058 0x4012 E058 0x2 E058	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Data of the second FIFO DMIC right channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC2R_DAT																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC2R_DAT	Data of the right FIFO DMIC path 2	R	0x000000

Table 23-555. Register Call Summary for Register DMIC_FIFO_DMIC2R_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

Table 23-556. DMIC_FIFO_DMIC2L_DATA

Address Offset	0x0000 005C		
Physical Address	0x4902 E05C 0x4012 E05C 0x2 E05C	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Data of the second FIFO DMIC left channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC2L_DAT																									

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC2L_DAT	Data of the left FIFO DMIC path 2	R	0x000000

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Table 23-557. Register Call Summary for Register DMIC_FIFO_DMIC2L_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

Table 23-558. DMIC_FIFO_DMIC3R_DATA

Address Offset	0x0000 0060		
Physical Address	0x4902 E060 0x4012 E060 0x2 E060	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Data of the third FIFO DMIC right channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC3R_DAT																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC3R_DAT	Data of the right FIFO DMIC path 3	R	0x000000

Table 23-559. Register Call Summary for Register DMIC_FIFO_DMIC3R_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

Table 23-560. DMIC_FIFO_DMIC3L_DATA

Address Offset	0x0000 0064		
Physical Address	0x4902 E064 0x4012 E064 0x2 E064	**Instance**	DMIC_L3 DMIC_CORTEX-A15 DMIC_DSP
Description	Data of the third FIFO DMIC left channel		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FIFO_DMIC3R_DAT																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED	Reserved	R	0x00
23:0	FIFO_DMIC3R_DAT	Data of the left FIFO DMIC path 3	R	0x000000

Table 23-561. Register Call Summary for Register DMIC_FIFO_DMIC3L_DATA

Digital Microphone Module

- FIFO Output Range Definition: [0]
- DMIC Register Summary: [1]

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23.8 Multichannel Audio Serial Port

This section describes the multichannel audio serial port (MCASP).

23.8.1 MCASP Overview

This section introduces the multichannel audio serial port (MCASP) module and describes its main functions and connections in the device.

The MCASP functions as a general-purpose audio serial port optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time- division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an intercomponent digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony / Philips digital interface (S/PDIF) transmit physical layer component.

Although intercomponent digital audio interface reception (DIR) mode (i.e. S/PDIF stream receiving) is NOT natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

Figure 23-168 shows the MCASP module in the device.

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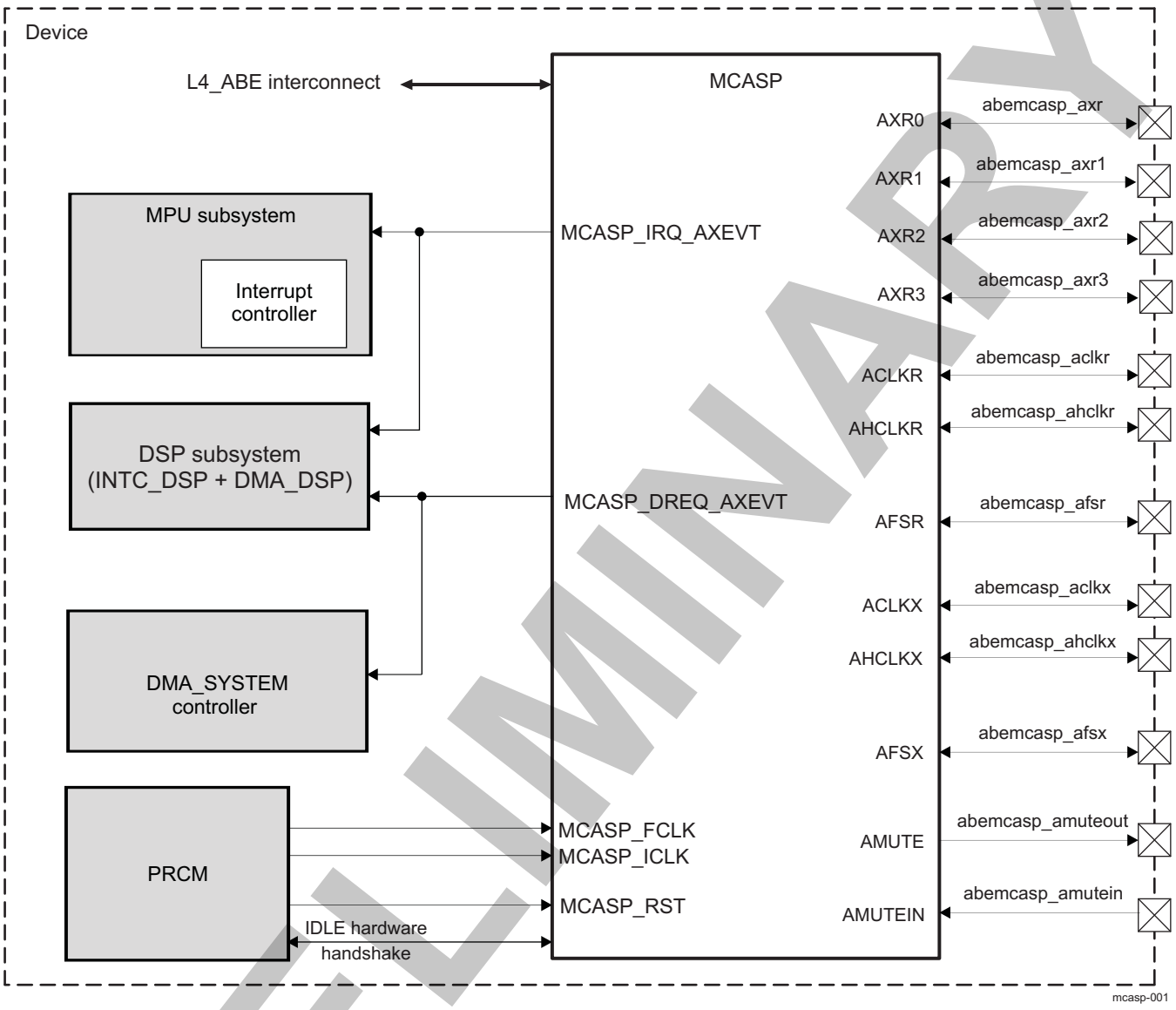
Figure 23-168. MCASP Module



The MCASP module includes the following main features:

- Support of the idle request/acknowledge protocol
- Four serializers - each serializer having associated one transmit (Tx) and one receive (Rx) channel, which allows support of :
  - 4 data channels, each configurable to either transmit or receive at a time
- A single 32-bit buffer per serializer for transmit and receive operations
- One transmit direct memory access (DMA) request linked with each of the 4 serializers
- One transmit interrupt request linked with each of the 4 serializers

NOTE: Because a serializer receive and transmit channels data is shared on the same MCASP data pin, user can choose to have either Tx or Rx function from a serializer, NOT both at the same time.

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23.8.2 MCASP Environment

This section describes the MCASP application fields from an environment point of view (external connections), along with the MCASP connectivity options. This section also lists all of the possible interfaces and describes the protocol and data format used in each case.

23.8.2.1 MCASP Signals

Table 23-562 describes the MCASP module pins, their corresponding signal names at device level and specifies their links to functions.

Table 23-562. MCASP I/O Signals

Module Pin Name	Device Level Signal Name	I/O[1]	Description	Module Pin Reset Value
AXR0	abemcasp_axr	I/O	Audio transmit / receive data - channel 0	HiZ
AXR1	abemcasp_axr1	I/O	Audio transmit / receive data - channel 1	HiZ
AXR2	abemcasp_axr2	I/O	Audio transmit / receive data - channel 2	HiZ
AXR3	abemcasp_axr3	I/O	Audio transmit / receive data - channel 3	HiZ
ACLKX	abemcasp_aclkx	I/O	Transmit bit clock	HiZ
AHCLKX	abemcasp_ahclkx	I/O	Transmit high-frequency master clock	HiZ
AFSX	abemcasp_afsx	I/O	Transmit frame synchronization	HiZ
ACLKR	abemcasp_aclkr	I/O	Receive bit clock	HiZ
AHCLKR	abemcasp_ahclkr	I/O	Receive high-frequency master clock	HiZ
AFSR	abemcasp_afsr	I/O	Receive frame synchronization	HiZ
AMUTE	abemcasp_amuteout	O	Mute out to external	HiZ
AMUTEIN	abemcasp_amutein	I	Mute in from external	HiZ

(1) I = Input; O = Output; I/O = Bidirectional

NOTE: The path from module pin to device pad(s) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and is programmable in the Control Module registers. For more information, refer to the Section 18.4.8, *Pad Functional Multiplexing and Configuration* and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, in *Chapter 18, Control Module*.

Figure 23-168, *MCASP Module*, also illustrates module pin signals mapping to MCASP signals visible at device pad level.

All MCASP pins on the device can be individually programmed as general-purpose input/output (GPIO) if they are not used for MCASP serial port functions.

The MCASP includes the following pins:

- Serializer 0 :
  - AXR0 : serial data transmission / reception pin 0. The corresponding MCASP signal at device level is named "abemcasp_axr".
- Serializer 1 :
  - AXR1 : serial data transmission / reception pin 1. The corresponding MCASP signal at device level is named "abemcasp_axr1".
- Serializer 2 :
  - AXR2 : serial data transmission / reception pin 2. The corresponding MCASP signal at device level is named "abemcasp_axr2".
- Serializer 3 :
  - AXR3 : serial data transmission / reception pin 3. The corresponding MCASP signal at device level is named "abemcasp_axr3".
- Transmit clock generator (one for all serializers) :

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  - ACLKX : MCASP transmit bit clock. The corresponding MCASP signal at device level is named "abemcasp_aclkx".
  - AHCLKX: MCASP transmit high-frequency master clock. The corresponding MCASP signal at device level is named "abemcasp_ahclkx".
- Transmit frame-sync generator (one for all serializers) :
  - AFSX: MCASP transmit frame sync. The corresponding MCASP signal at device level is named "abemcasp_afsx".
- Receive clock generator (one for all serializers):
  - ACLKR : MCASP receive bit clock. The corresponding MCASP signal at device level is named "abemcasp_aclkr".
  - AHCLKR: MCASP receive high-frequency master clock. The corresponding MCASP signal at device level is named "abemcasp_ahclkr".
- Receive frame-sync generator (one for all serializers):
  - AFSR: MCASP receive frame sync. The corresponding MCASP signal at device level is named "abemcasp_afsr".
- Mute in/out:
  - AMUTEIN: MCASP mute input (from external device). The corresponding MCASP signal at device level is named "abemcasp_amutein".
  - AMUTE: MCASP mute output. The corresponding MCASP signal at device level is named "abemcasp_amuteout".

NOTE: A serializer AXRn data pin (where n=0 to 3 in the device) is shared between the transmit and receive logic of this serializer. The direction of data is determined in the MCASP_PDIR and the function (Tx or Rx) is selected in the corresponding serializer control register MCASP_XRSRCTLn.

23.8.2.2 Protocols and Data Formats

23.8.2.2.1 Protocols Supported

The MCASP transmit section supports several industry formats, such as :

- various TDM streams from 2 to 32 slots
- a variety of I2S and similar bit-stream formats
- S/PDIF industry format supported in DIT-transfer mode of the module

The MCASP receive section supports several industry formats, such as :

- various TDM streams from 2 to 32 slots
- a variety of I2S and similar bit-stream formats
- A 384-slot TDM stream designed for easy interface to external DIR-chip component, transmitting DIR-frames to MCASP using the I2S protocol (one time slot for each DIR-subframe)

Programmable clock and frame-synchronization generator modules are individually available for the transmit and receive section, respectively. This allows the MCASP to receive and transmit at different rates. For example, the sample rate of MCASP received data can be 44.1 kHz but the output data can be sampled out at 96 kHz.

The MCASP transmit and receive sections can be independently programmed to support the following options on the basic serial protocol:

- Programmable clock and frame-sync polarity (rising or falling edge):
  - for the ACLKX, AHCLKX, and AFSX signals in the MCASP transmitting part
  - for the ACLKR, AHCLKR, and AFSR signals in the MCASP receiving part
- Slot length (number of bits per time slot): 8, 12, 16, 20, 24, 28, 32 bits supported
- Word length (bits per word): 8, 12, 16, 20, 24, 28, 32 bits; always less than or equal to the time slot

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length

- First-bit data delay: 0-, 1-, 2-bit clocks
- Left- / right- alignment of word inside slot
- Bit order: Most-significant bit (MSB) first or least-significant bit (LSB) first reception / transmission
- Bit mask/pad/rotate function
- Automatically aligns data in Q31- or integer format
- Automatically masks nonsignificant bits (sets to 0, 1, or extends value of another bit)

NOTE: In I2S mode, the transmit and receive sections can support simultaneous transfers on up to all the 4 serial data pins - AXR0 - AXR3 operating as 192 kHz stereo channels.

The DIT-transfer mode includes the following additional for a MCASP transmitter features:

- Transmit-only mode: 384 time slots (subframe) per frame
- Biphase encoded LVCMOS output
- Channel status RAM (384 bits)
- User data RAM (384 bits)
- Separate valid bit (V) for subframes A and B

NOTE: The MCASP does NOT natively support DIR-mode reception (i.e. receiving in the S/PDIF format). To allow this, the MCASP can use a DIR-input to I2S-output converter implemented by an external device (i.e. external DIR component). To facilitate reception in this case, the TDM mode of MCASP receivers logic is extended to support a non-standard 384-slot TDM stream.

NOTE: An external transceiver must be connected to the MCASP port in the device to translate the electrical signals delivered by the MCASP (1.2 V or 1.8 V LVCMOS levels) to the electrical levels of the S/PDIF standard.

23.8.2.2.2 Definition of Terms

The serial bitstream transmitted or received by a MCASP serializer is a long sequence of 1s and 0s on an audio transmit / receive pins: AXR0 through AXR3 (signals named "abemcasp_axr, abemcasp_axr1, abemcasp_axr2 and abemcasp_axr3" at device level). However, the sequence has a hierarchical organization that can be described in terms of frames of data, slots, words, and bits.

A basic synchronous serial interface consists of three important components: clock, frame sync, and data. Figure 23-169 shows two of the three basic components: the clock signal (ACLKX / ACLKR) and the data signals AXRn, where n=0 to 3. Figure 23-169 does not specify whether the clock is for transmit (ACLKX) or receive (ACLKR) because the definitions of terms apply to both receive and transmit interfaces. In operation, each transmitter and receiver uses the signals ACLKX and ACLKR as serial clock, respectively. Optionally, a receiver can use ACLKX as the serial clock when a transmitter and receiver (not from the same serializer) of the MCASP are configured to operate synchronously.

- Bit:

  A bit is the smallest entity in the serial data stream. The beginning and end of each bit is marked by an edge of the serial clock. The duration of a bit is a serial clock period. A '1' is represented by a logic high on AXRn (n=0 to 3) pins for the entire duration of the bit. A 0 is represented by a logic low on an AXRn pin for the entire duration of the bit.
- Word:

  A word is a group of bits that make up the data being transferred between the MCASP and the external device. Figure 23-169 shows an 8-bit word.
- Slot:

  A slot consists of the bits that make up the word and can consist of additional bits used to pad the

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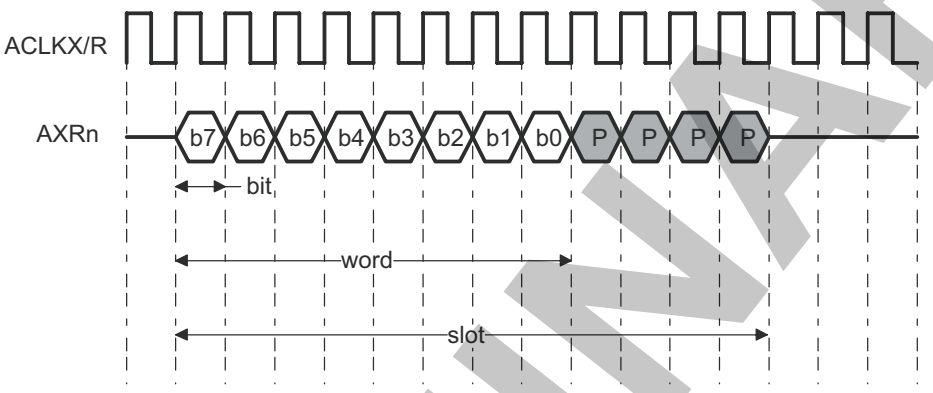
word to a convenient number of bits for the interface between the MCASP and the external device. In Figure 23-169, the audio data consists of only 8 bits of useful data (8-bit word), but it is padded with four 0s (12-bit slot) to satisfy the desired protocol in interfacing to an external device. Within a slot, the bits can be shifted out of the MCASP on an AXRn pin (n=0 to 3) with either MSB or LSB first.

When the word size is smaller than the slot size, the word can be aligned to the left of the slot (beginning) or to the right of the slot (end). The additional bits in the slot not belonging to the word can be padded with 0, 1, or with one of the bits (typically, the MSB or LSB) from the data word, i.e. left-aligned words within a slot are terminated with padding bits and right-aligned words within a slot are preceded by padding bits to fit in the slot size. Figure 23-170 shows these options.

Figure 23-169. Definition of Bit, Word, and Slot



(1) b7:b0 - bits. Bits b7 to b0 form a word.

(2) P - pad bits. Bits b7 to b0, together with the 4 pad bits, form a slot.

(3) In this example, the data is transmitted MSB first, left-aligned.

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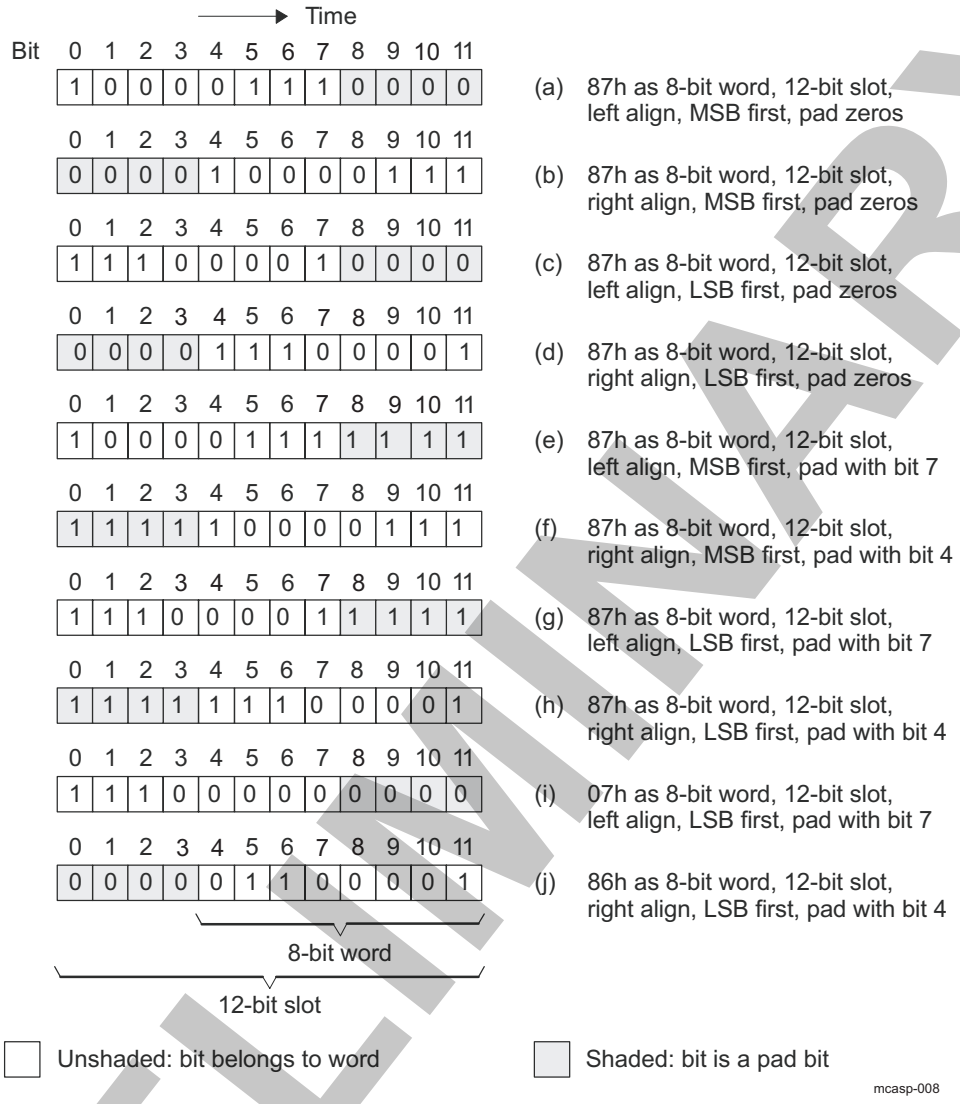
Figure 23-170. Bit Order and Word Alignment Within a Slot Examples



- Frame

  The third basic element of a synchronous serial interface is the frame synchronization signal, also referred to as frame sync in this chapter. A frame contains one or multiple slots, as determined by the desired protocol. Figure 23-171 shows an example frame of data and the frame definitions. In operation, the transmitter uses abemcasp_afsx, and the receiver - abemcasp_afsr signal. Figure 23-171 does NOT specify whether the frame sync (FS) is for transmit (AFSX) or receive (AFSR) because the definitions of terms apply to both receive and transmit interfaces. In operation, each transmitter / receiver uses AFSX / AFSR as a frame synchronization signal, respectively. Optionally, the receiver can use AFSX as the frame sync when the transmitter and receiver of the MCASP are configured to operate synchronously. This example shows two slots in a frame (I2S format) and a frame-sync (FS) duration of a slot length.

  This section shows only the generic definition of the frame sync. For more information about the frame-sync formats required for the transfer modes and protocols (TDM-mode and DIT-mode supported formats), see Section 23.8.2.2.3, *TDM Format* and Section 23.8.2.2.5, *S/PDIF-Coding Format*.

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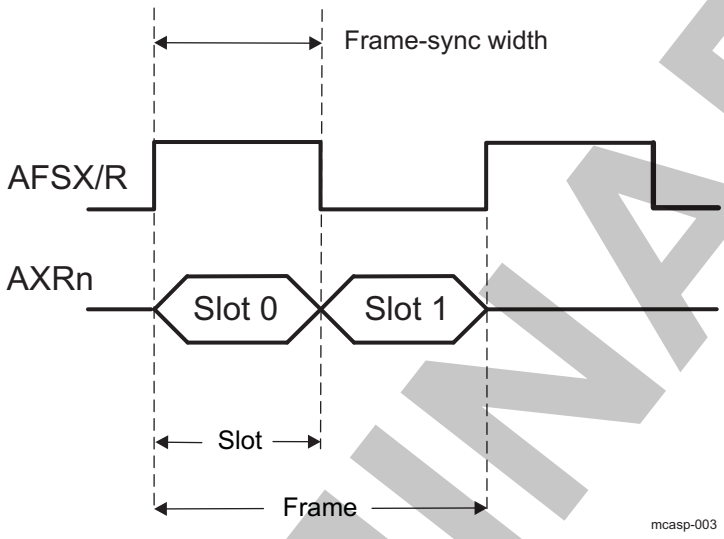
NOTE: All of the 4 MCASP serializers share the same, device pad accessible, clock and frame signals, as follows:

– AHCLKX, ACLKX and AFSX for the transmitting section

– AHCLKR, ACLKR and AFSR for the receiving section

Figure 23-171. Definition of Frame and Frame-Sync Width



The following terms are used throughout this chapter:

- DIT: Digital audio interface transmit. The MCASP supports transmitting in S/PDIF format on each AXRn (n=0 to 3) data pin.
- DIR: Digital audio interface receive. The MCASP does NOT natively support receiving in S/PDIF format on AXRn (n=0 to 3) data pins and requires an external DIR-to-TDM or DIR-to-I2S converter chip for a DIR-frame reception.
- Slot or time slot: For DIT / DIR format, a MCASP time slot corresponds to a DIT / DIR subframe.

23.8.2.2.3 TDM Format

The TDM format is used to transfer data between the MPU (or DSP) and one or more analog-to-digital converter (ADC), digital-to-analog converter (DAC), or S/PDIF receiver (DIR) devices. An example for a 6-slot (channel) TDM transmission on one MCASP data pin - AXRn is illustrated on Figure 23-172.

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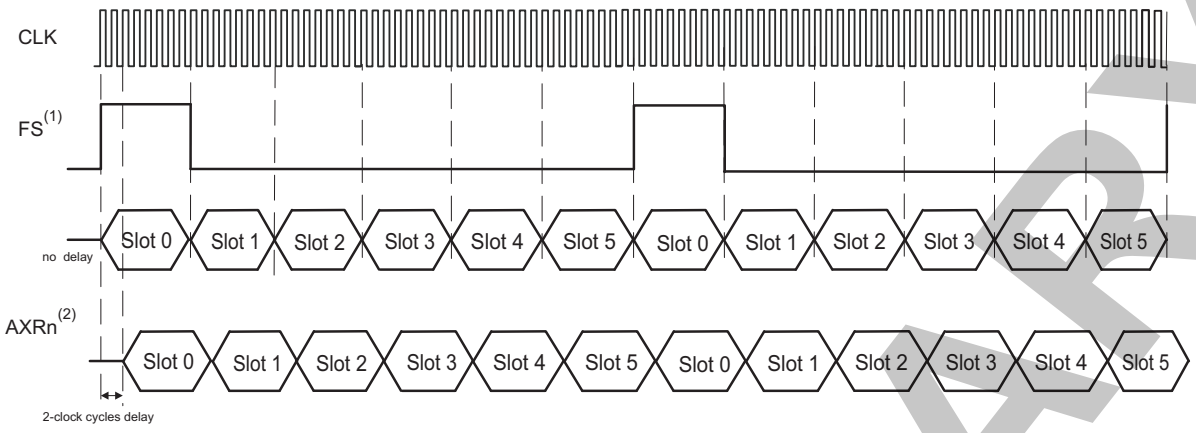
Figure 23-172. TDM Format - 6 channel example



The TDM format uses three signals In a basic synchronous serial interface : data (AXRn), clock (CLK) and frame sync (FS). The data signal present on AXRn pin is fully synchronous to the serial clock (ACLKX or ACLKR). The data bits are grouped into words and slots (see also Section 23.8.2.2.2), the latter being also refered to as the "time-slots" or "channels" in TDM terminology. A frame consists of multiple time-slots. Each TDM frame is marked by the frame sync signal (AFSX or AFSR). The TDM transfer is continuous and periodic, with no delays between slots.

Within a certain frame, the last bit of slot N is followed immediately on the next serial clock with the first bit of the next slot N+1. On the boundary between two adjacent TDM-frames, the last bit of the last slot from the frame M, is followed immediately on the next clock cycle with the first bit of the first slot from the next frame M+1. For MCASP, there is an option to offset the first bit of the first slot with a 0-,1- or 2-cycle delay from the frame sync signal.

The frame sync - AFSX/AFSR only marks the beginning of slot 0 and start of a new frame. Since it does NOT determine the boundaries of a slot, **there is a requirement for a connected transmitter and receiver to agree on the number of transfered bits per slot.**

In a typical audio system involving MCASP module, a single TDM data frame is transfered during each sample period Ts of a data converter. The user has following choices to implement multiple channels :

- Use more data slots (on a price of higher speed serial clock) per frame transmitted / received on just one of the available MCASP data pins (AXR0 - AXR3).
- Use less number of slots per TDM frame (requires a slower serial clock), making them available on several of the MCASP pins (AXR0 - AXR3).

23.8.2.2.4 I2S Format

The TDM transfer mode of the MCASP supports the I2S format when frame is configured to have 2 slots. I2S format is specifically designed to transfer a stereo channel (left and right) over a single data pin AXRn. "Slots" are also commonly referred to as "channels". The frame width duration in the I2S format equals size of a slot. The frame signal is also referred to as "word select" in the I2S format.

The I2S protocol is illustrated on Figure 23-173.

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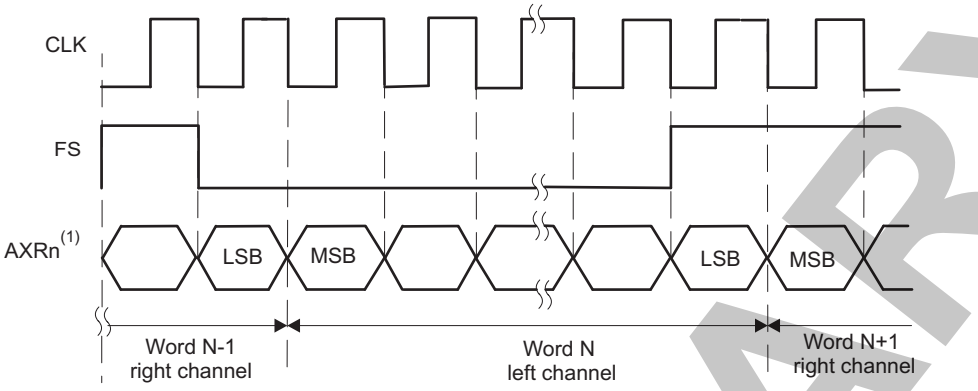
Figure 23-173. I2S Format Overview



(1) - The example shows I2S data MSB-first transmission with 1-clock cycle delay between FS and data MSB

mcasp-036

23.8.2.2.5 S/PDIF Coding Format

The MCASP transmitter supports the S/PDIF format with 1.2- and 1.8-V biphase-mark encoded output. The S/PDIF format is supported by the DIT- transfer mode of the MCASP. This section briefly discusses the S/PDIF coding format.

NOTE: The DIR- reception of S/PDIF format frames is NOT natively supported from the device MCASP. For this purpose, an external DIR-to-TDM transfer mode adapter can be used between the remote device S/PDIF transmitter output and the MCASP TDM-only compatible receiver input.

23.8.2.2.5.1 Biphase-Mark Code

In S/PDIF format, the digital signal is coded using the biphase-mark code (BMC). For each serializer transmitter n (where n=0 to 3), the clock, frame, and data are embedded in only one signal - the data signal AXRn. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin. These two logical states form a cell. The duration of the cell, which equals the duration of the data bit, is called a time interval. A logical 1 is represented by two transitions of the signal within a time interval, which corresponds to a cell with logical states 01 or 10. A logical 0 is represented by one transition within a time interval, which corresponds to a cell with logical states 00 or 11. In addition, the logical level at the start of a cell is inverted from the level at the end of the previous cell. Figure 23-174 and Table 23-563 show how data is encoded to the BMC format.

As shown in Figure 23-174, the clock frequency is twice the unencoded data bit rate. In addition, the clock is always programmed to 128 × f_s, where f_s is the sample rate (see Section 23.8.2.2.5.3, *Frame Format*, for details on how this clock rate is derived based on the S/PDIF format).

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Figure 23-174. Biphase-Mark Code

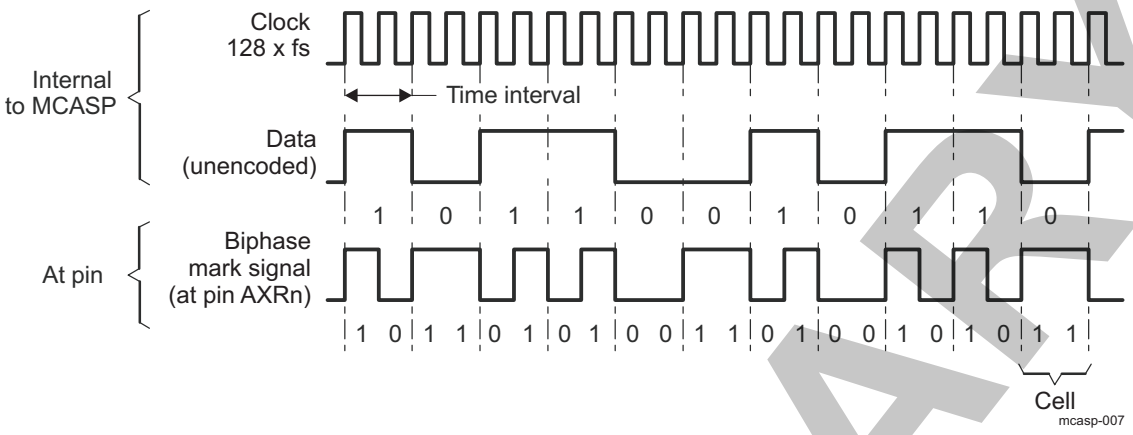

Table 23-563. Biphase-Mark Encoder

Data (Unencoded)	Previous State at Pin AXRn	BMC-Encoded Cell Output at Pin AXRn
0	0	11
0	1	00
1	0	10
1	1	01

23.8.2.2.5.2 S/PDIF Subframe Format

Every audio sample transmitted in a subframe consists of 32 S/PDIF time intervals (or cells), numbered 0 to 31. Figure 23-175 shows a subframe.

- Time intervals 0–3 carry one of the three permitted preambles to signify the type of audio sample in the current subframe. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0 or 1 logical states in a row. See Table 23-564.
- Time intervals 4–27 carry the audio sample word in linear 2s-complement representation. The MSB is carried by time interval 27. When a 24-bit coding range is used, the LSB is in time interval 4. When a 20-bit coding range is used, time intervals 8-27 carry the audio sample word with the LSB in time interval 8. Time intervals 4–7 may be used for other applications and are designated auxiliary sample bits.
- If the source provides fewer bits than the interface allows (20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field can carry any other information.
- Time interval 28 carries the validity bit (V) associated with the main data field in the subframe.
- Time interval 29 carries the user data channel (U) associated with the main data field in the subframe.
- Time interval 30 carries the channel status information (C) associated with the main data field in the subframe. The channel status indicates if the data in the subframe is digital audio or some other type of data.
- Time interval 31 carries a parity bit (P) such that time intervals 4–31 carry an even number of 1s and an even number of 0s (even parity). As listed in Table 23-564, the preambles (time intervals 0–3) are also defined with even parity.

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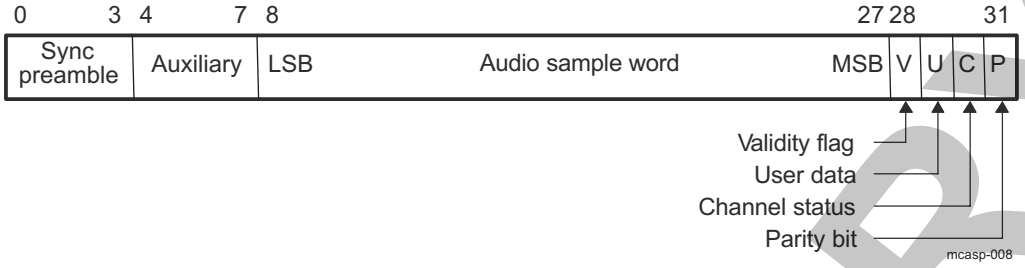
Figure 23-175. S/PDIF Subframe Format



As listed in Table 23-564, the MCASP DIT generates only one polarity of preambles, and it assumes the previous logical state is 0. This is because the MCASP assures an even-polarity encoding scheme when transmitting in DIT mode. If an underrun condition occurs, the DIT resynchronizes to the correct logic level on the AXRn pin before continuing with the next transmission.

Table 23-564. Preamble Codes

Preamble Code[1]	Previous Logical State	Logical States on pin AXRn[2]	Description
B (or Z)	0	1110 1000	Start of a block and subframe 1
M (or X)	0	1110 0010	Subframe 1
W (or Y)	0	1110 0100	Subframe 2

(1) Historically, preamble codes are referred to as B, M, and W. For use in professional applications, preambles are referred to as Z, X, and Y, respectively.

(2) The preamble is not BMC-encoded. Each logical state is synchronized to the serial clock. These eight logical states make up time slots (cells) 0 to 3 in the S/PDIF stream.

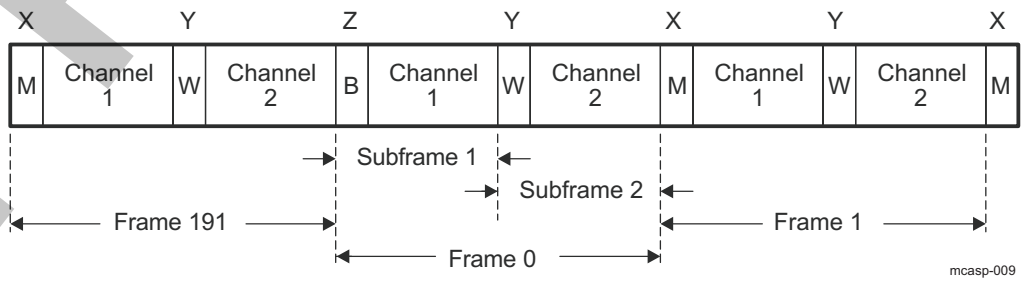
23.8.2.2.5.3 Frame Format

An S/PDIF frame is composed of two subframes (see Figure 23-176). For linear coded audio applications, the rate of frame transmission normally corresponds exactly to the source sampling frequency f_s. The S/PDIF format clock rate is therefore 128 × f_s (128 = 32 cells per subframe × 2 clocks per cell × 2 subframes per sample). For example, for an S/PDIF stream at a 192-kHz sampling frequency, the serial clock is 128 × 192 kHz = 24.58 MHZ.

In 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive subframes. Both subframes contain valid data (cell 28 validity bits for A- and B- channels, both set to '0'). The first subframe (left or A channel in stereophonic operation and primary channel in monophonic operation) normally starts with preamble M. However, the preamble of the first subframe changes to preamble B once every 192 frames to identify the start of the block structure used to organize the channel status information. The second subframe (right or B channel in stereophonic operation and secondary channel in monophonic operation) always starts with preamble W.

In single-channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried in the first subframe and may be duplicated in the second subframe. If the second subframe is not carrying duplicate data, cell 28 (validity bit) is set to logical 1.

Figure 23-176. S/PDIF Frame Format



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23.8.3 MCASP Integration

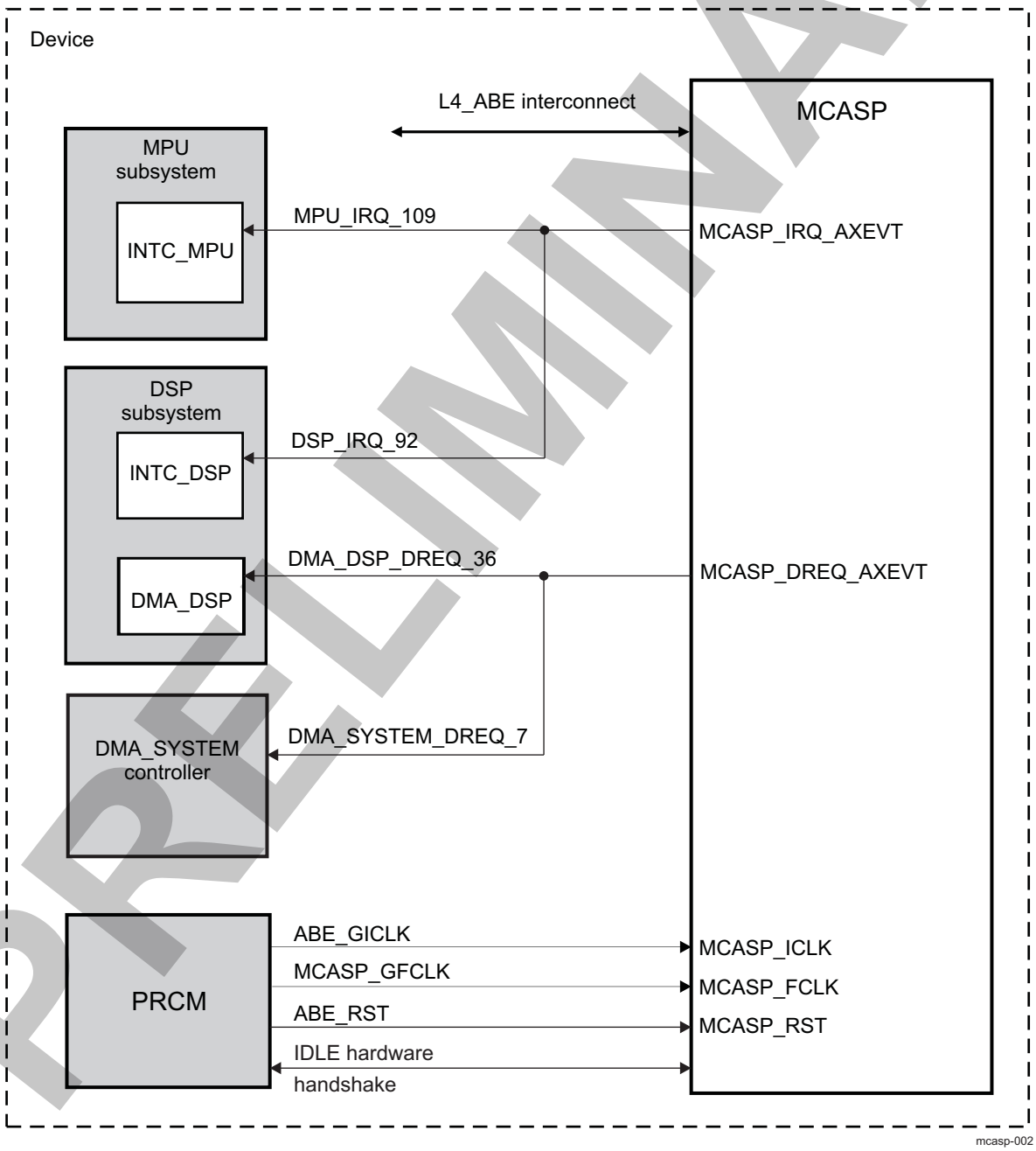
This section describes module integration in the device, including information about clocks, resets, and hardware requests.

The MCASP includes the following features:

- IDLE hardware handshake
- One DMA request for all transmitters
- One interrupt request (IRQ) for all transmitters
- NO interrupt (IRQ) and DMA requests are implemented for the MCASP receivers at device level.

Figure 23-177 shows MCASP integration.

Figure 23-177. MCASP Integration



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NOTE: For more information about the IDLE hardware handshake, see Section 3.1.1.1.2, *Module Level Clock Management* of Chapter 3, *Power, Reset, and Clock Management*.

Table 23-565 through Table 23-567 summarize the integration of the module in the device.

Table 23-565. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
MCASP	PD_ABE	NO	L4_ABE

Table 23-566. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MCASP	MCASP_ICLK	ABE_GICLK	PRCM	MCASP interface clock
	MCASP_FCLK	MCASP_GFCLK	PRCM	MCASP functional clock
Resets				
MCASP	MCASP_RST	ABE_RST	PRCM	AUDIO power domain reset

Table 23-567. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MCASP	MCASP_IRQ_AXEVT	DSP_IRQ_92	INTC_DSP	MCASP transmit interrupt to the DSP interrupt controller
		MPU_IRQ_109	INTC_MPU	MCASP transmit interrupt to the MPU interrupt controller
DMA Requests				
MCASP	MCASP_DREQ_AXEVT	DMA_SYSTEM_DREQ_7	DMA_SYSTEM	MCASP data transmit DMA request line to the system DMA (DMA_SYSTEM)
		DMA_DSP_DREQ_36	DMA_DSP	MCASP data transmit DMA request line to the DSP DMA (DMA_DSP)

NOTE:

- For the description of the interrupt source, see Section 23.8.4.11, *Interrupt Requests*.
- For the description of the DMA source, see Section 23.8.4.12, *DMA Requests*.

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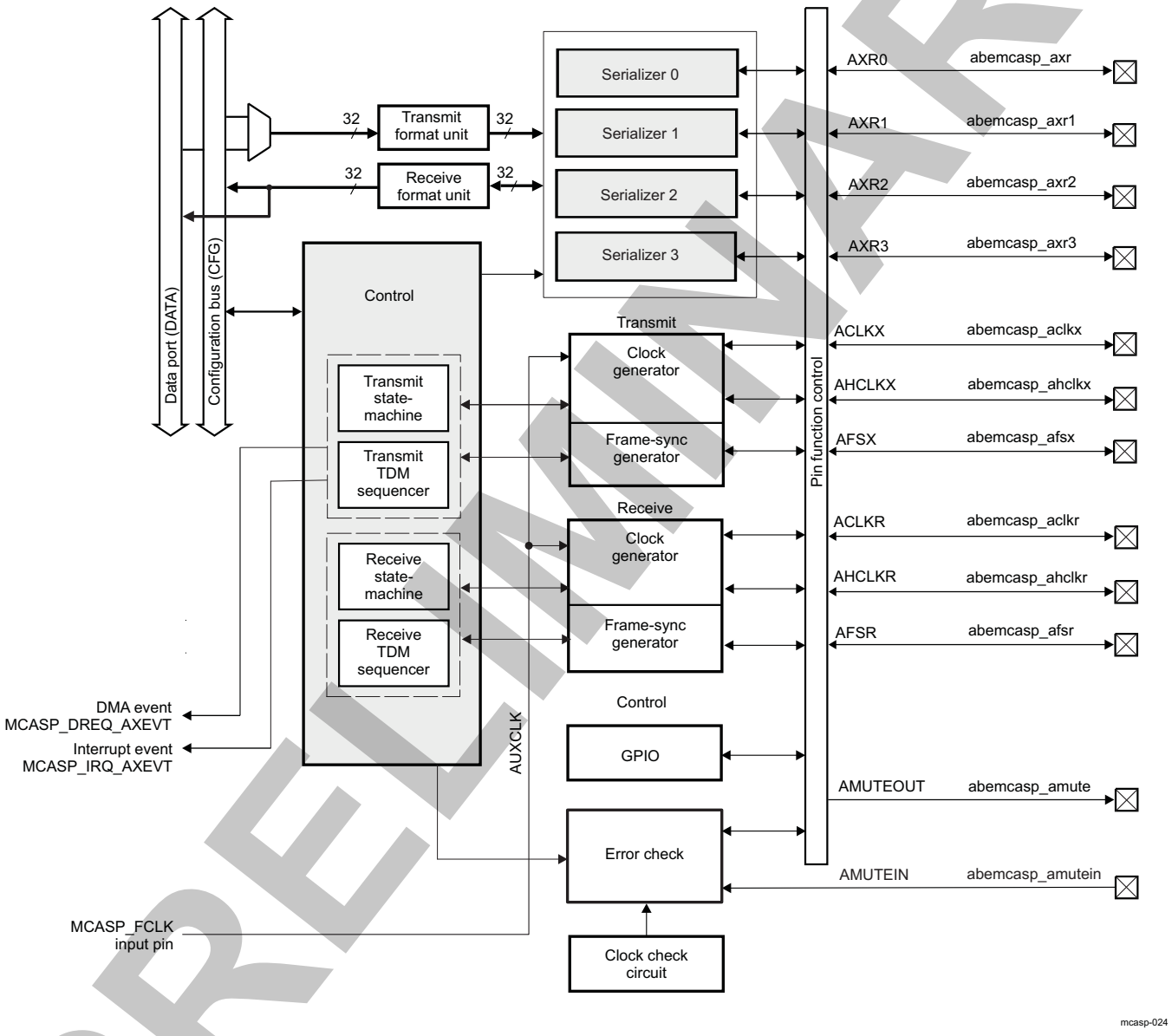
23.8.4 MCASP Functional Description

23.8.4.1 Block Diagram

Figure 23-178 shows the major blocks of the MCASP. The MCASP has a total of 4 serializers sharing a clock and frame-sync generator, format unit, and error-checking logic independently for the receive and transmit part.

Figure 23-178. MCASP Block Diagram



NOTE: The AUXCLK clock is sourced directly from the MCASP_FCLK functional clock input which is tied to the PRCM.MCASP_GFCLK clock. For more information, see Section 3.6, *Clock Management Functional Description* of Chapter 3, *Power, Reset and Clock Management*.

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23.8.4.2 MCASP Clock and Frame-Sync Configurations

There are three scenarios to provide clock source signals for the Tx part and four scenarios for the Rx part of the MCASP serializers. The first three scenarios are identical between the Tx and Rx part of the MCASP. They feature an asynchronous operation between receiver and transmitter channels using independent Tx / Rx bit rate clock sources (either internal or external).

In the first scenario, the transmit - XCLK and receive - RCLK serial clocks (clock at the bit rate) are generated internally by passing through a couple of clock dividers off the internal functional clock source (AUXCLK). In this case, the bit rate clock is generated internally and is driven out on the pin ACLKX for the Tx part (signal named - "abemcasp_aclkx at device level)" and pin ACLKR for the Rx part (signal named - abemcasp_aclkr at device level), respectively. An internally generated high-frequency clock can be optionally driven out onto the AHCLKX pin for the Tx part (signal named - "abemcasp_ahclkx" at device level) and AHCLKR pin for the Rx part (signal named - "abemcasp_ahclkr" at device level) to serve as a reference clock for other components in the system.

In the second scenario, an external for the device clock, is passed on the ACLKX (for the TX part) and ACLKR (for the RX part) pins which are configured as inputs. In this case the Rx- / Tx- high-speed clock logic is bypassed for the XCLK / RCLK generation.

In the third (mixed) scenario, an externally driven (master) high-frequency clock is applied on the AHCLKX (for the TX part) / AHCLKR (for the RX part) pins, which are configured as inputs. In this case the AHCLKX / AHCLKR clock frequency can be divided down via programming the ACLKX / ACLKR associated dividers to produce the necessary bit rate clock. The high-speed clock divider can NOT be used.

In the fourth clock generation scenario the bit rate clock for MCASP receivers - RCLK is derived from the bit rate clock of the MCASP transmitters - XCLK for a synchronous operation between transmitters and receivers. Hence, the whole receiver clock generator logic is bypassed.

A typical role of the MCASP frame sync signal is to carry the left/right clock (LRCLK) signal when transmitting and receiving stereo data.

For an asynchronous operation, the AFSX (Tx part) and AFSR (Rx part) frame synchronization signals can be sourced internally or delivered externally independently for the Tx and Rx channels. During synchronous operation the receive frame sync - AFSR signal is derived from the transmit frame sync - AFSX signal. A synchronous and asynchronous mode applies to bit rate clock and frame sync signals at the same time.

23.8.4.2.1 Transmit Clock

The transmit high-speed and transmit clock configuration is controlled by the following registers:

- MCASP_ACLKXCTL
- MCASP_AHCLKXCTL

In case, the transmit bit clock, ACLKX, is generated internally, the MCASP_ACLKXCTL[5] CLKXM bit must be set to 1. Thus, the clock is divided down by a programmable bit clock divider (the MCASP_ACLKXCTL[4:0] CLKXDIV bit field) from the source signal.

If the transmit high-frequency master clock, AHCLKX, is also sourced internally (that is first scenario described in Section 23.8.4.2, the MCASP_AHCLKXCTL[15] HCLKXM bit must be set to 1. Thus, the clock is divided down by a programmable high-clock divider (the MCASP_AHCLKXCTL[11:0] HCLKXDIV bit field) from the MCASP internal clock source AUXCLK.

Internally, the MCASP always shifts transmit data at the rising edge of the internal transmit clock - XCLK, (see Figure 23-179). The CLKXP mux determines if ACLKX needs to be inverted to become XCLK. If MCASP_ACLKXCTL[7] CLKXP = 0, the CLKXP mux directly passes ACLKX signal to XCLK. As a result, the MCASP shifts transmit data at the rising edge of ACLKX. If MCASP_ACLKXCTL[7] CLKXP = 1, the CLKX mux passes the inverted version of ACLKX to XCLK. As a result, the MCASP shifts transmit data at the falling edge of ACLKX.

It can be seen in Figure 23-179 that XCLK is propagated to the Rx clock logic, to allow an internally synchronous operation between MCASP transmitters and receivers. This is used for example in the MCASP loopback mode.

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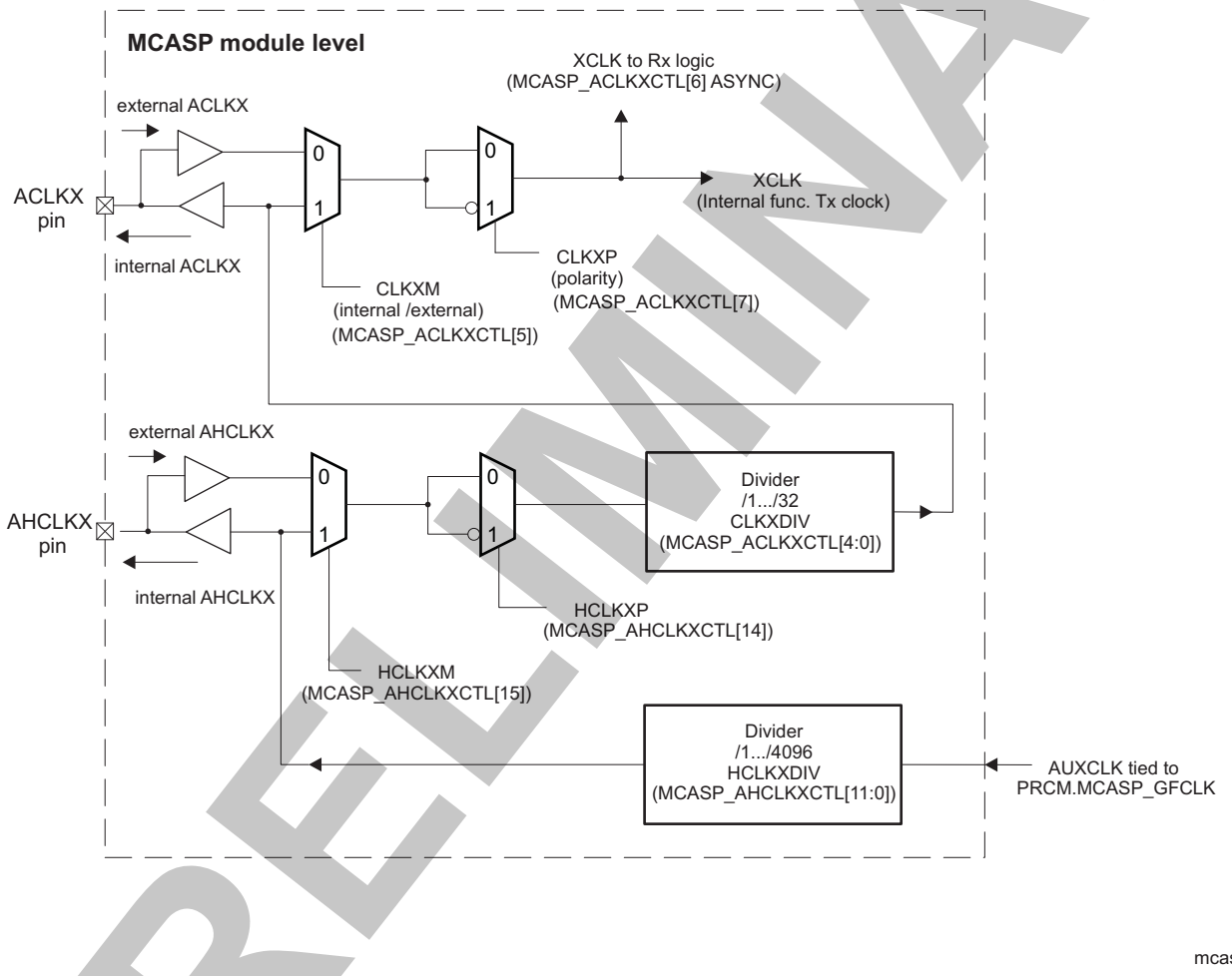
NOTE: The polarity of ACLKX can be controlled in MCASP_ACLKXCTL[7] CLKXP, regardless of ACLKX signal being internally or externally sourced.

In addition, there is an option to invert polarity of the AHCLKX master high speed clock via writing the MCASP_AHCLKXCTL[14] HCLKXP bit.

NOTE: In a similar way, the polarity of AHCLKX clock can be controlled in MCASP_AHCLKXCTL[14] HCLKXP, regardless of the AHCLKX signal being internally or externally sourced.

Figure 23-179 is the block diagram of the transmit clock generator.

Figure 23-179. Transmit Clock Generator Block Diagram



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23.8.4.2.2 Receive Clock

The MCASP receive clock generator is built on a very similar to the transmit clock generator (but independent) circuit.

The receive clock configuration is controlled by the following registers:

- MCASP_ACLKRCTL
- MCASP_AHCLKRCTL

In case, the receive bit clock, ACLKR, is generated internally (but asynchronously to XCLK), the MCASP_ACLKRCTL[5] CLKRM bit must be set to 1. Thus, the clock is divided down by a programmable bit clock divider (the MCASP_ACLKRCTL[4:0] CLKRDIV bit field) from the source signal.

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If the receive high-frequency master clock, AHCLKR, is also sourced internally (that is first scenario described in Section 23.8.4.2, the MCASP_AHCLKRCTL[15] HCLKRM bit must be set to 1. Thus, the clock is divided down by a programmable high-clock divider (the MCASP_AHCLKRCTL[11:0] HCLKRDIV bit field) from the MCASP internal clock source AUXCLK.

The receive high-frequency master clock - AHCLKR may be (but is not required to be) output on the AHCLKR pin where it is available to other devices in the system. Regardless if AHCLKR is either internally generated or externally sourced, polarity of the high-frequency clock may be programmed via bit MCASP_AHCLKRCTL [14] HCLKRP to be either rising or falling edge.

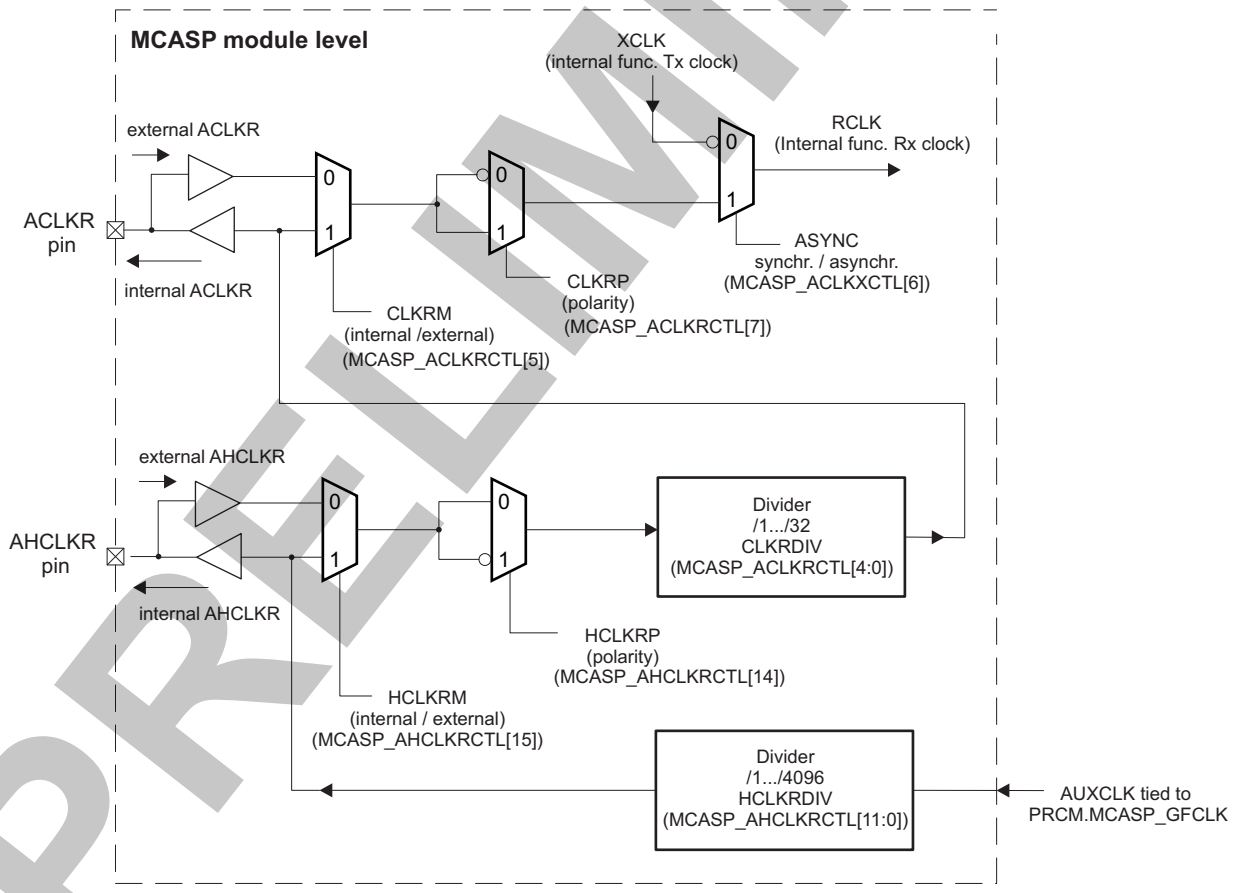
NOTE: The polarity of ACLKR can be controlled in MCASP_ACLKRCTL[7] CLKRP, regardless of ACLKR signal being internally or externally sourced.

In a similar way, the polarity of AHCLKR clock can be controlled in MCASP_AHCLKRCTL[14] HCLKRP, regardless of the AHCLKR signal being internally or externally sourced.

There is an option for the MCASP receiver to be configured to operate synchronously to the ACLKX and AFSX signals. The XCLK output of the Tx Clock generator (see Figure 23-179and Figure 23-180) becomes source of the receive clock (RCLK output), when the MCASP_ACLKXCTL[6] ASYNC bit in the transmit clock control register is set to '0b0'. For more information, refer to Section 23.8.4.2.4.

Figure 23-179 is the block diagram of the receive clock generator.

Figure 23-180. Receive Clock Generator Block Diagram



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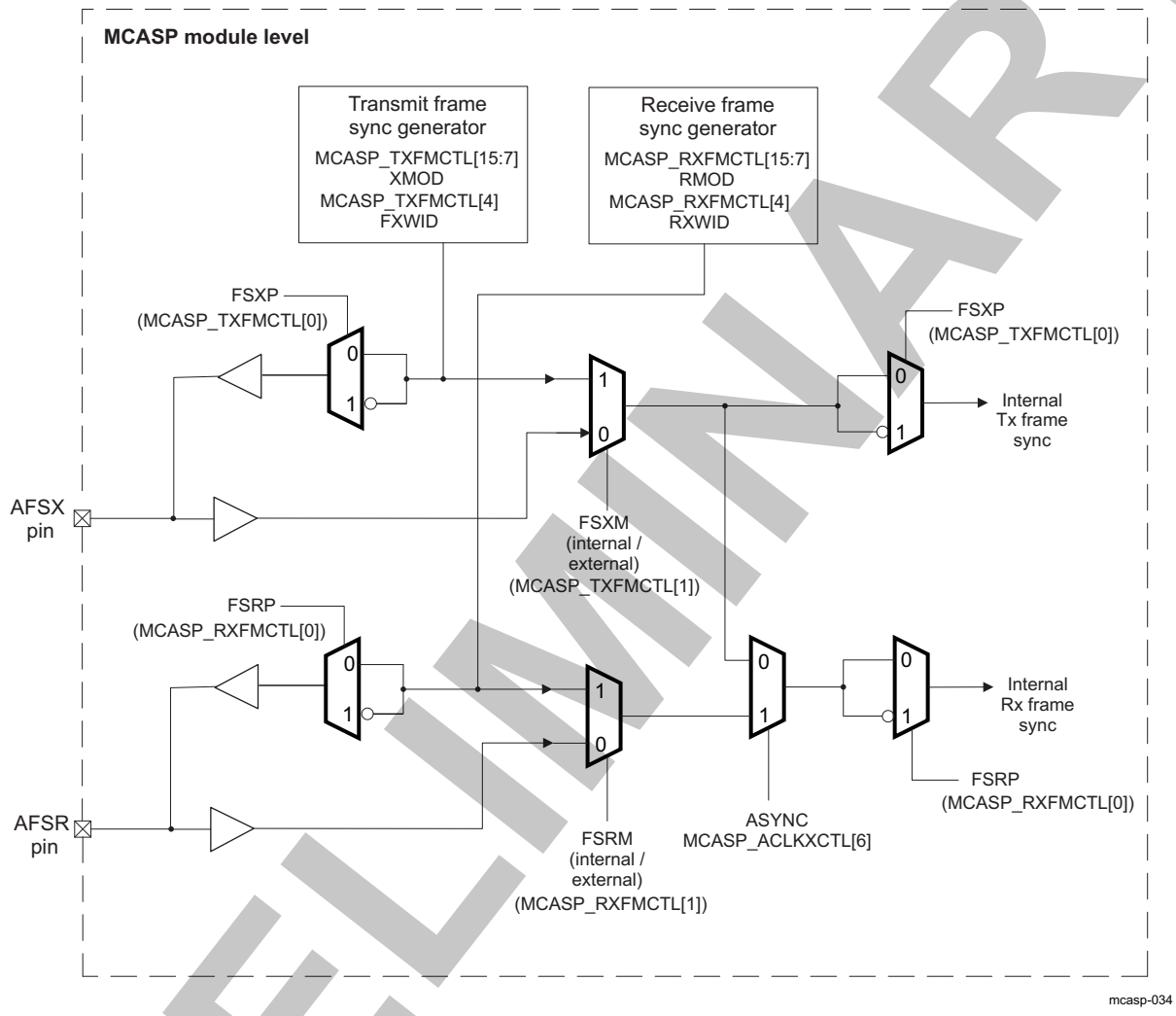
23.8.4.2.3 Frame-Sync Generator

The MCASP frame sync generator logic is illustrated in Figure 23-181. The transmit frame-sync pin is AFSX (signal named "abemcasp_afsx" at device level), and the receive frame-sync pin is AFSR (signal named "abemcasp_afsr" at device level) .

Figure 23-181. Frame Sync Generator Block Diagram



For the transmit logic, following frame-sync generator configurations can be selected :

- Internally / externally generated frame-sync via configuring bit MCASP_TXFMCTL[1] FSXM
- Frame-sync polarity: Rising edge or falling edge via configuring bit MCASP_TXFMCTL[0] FSXP
- Frame-sync width: "single bit" or "single word" via configuring bit MCASP_TXFMCTL[4] FXWID
- Frame sync mode - the appropriate frame sync generation pattern for the selected transfer mode is defined in the bitfield MCASP_TXFMCTL[15:7] XMOD, as follows:
  - For DIT mode (384 slots) - MCASP_TXFMCTL[15:7] XMOD = 0x180
  - For I2S mode (2 TDM slots) - MCASP_TXFMCTL[15:7] XMOD = 0x2
  - For TDM mode (from 3 to 32 TDM slots) - MCASP_TXFMCTL[15:7] XMOD set in range 0x3 - 0x20
- Bit delay: 0, 1, or 2 cycles before the first data bit. This delay is defined in MCASP_TXFMT[17:16] XDATDLY

For the receive logic, following frame-sync generator configurations can be selected :

- Internally / externally generated frame-sync via configuring bit MCASP_RXFMCTL[1] FSRM

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- Frame-sync polarity: Rising edge or falling edge via configuring bit MCASP_RXFMCTL[0] FSRP
- Frame-sync width: "single bit" or "single word" via configuring bit MCASP_RXFMCTL[4] FRWID
- Frame sync mode - the appropriate frame sync generation pattern for the selected transfer mode is defined in the bitfield MCASP_RXFMCTL[15:7] RMOD, as follows:
  - For I2S mode (2 TDM slots) - MCASP_RXFMCTL[15:7] RMOD = 0x2
  - For TDM mode (from 3 to 32 TDM slots) - MCASP_RXFMCTL[15:7] RMOD set in range 0x3 - 0x20
  - For the special 384-slot TDM mode - MCASP_RXFMCTL[15:7] RMOD=0x180
- Bit delay: 0, 1, or 2 cycles before the first data bit. This delay is defined in MCASP_RXFMT[17:16] RDATDLY
- Selecting the source (AFSX or AFSR) of receiver internal frame synchronization. This is done in the same bit - MCASP_ACLKXCTL[6] ASYNC, used to define the receiver internal clock source. For more details, refer to Section 23.8.4.2.4.

Regardless of the AFSX / AFSR being internally generated or externally sourced, the polarity of AFSX/AFSR is determined by FSXP/FSRP, respectively, to be either rising or falling edge. If FSXP/FSRP = 0, the frame sync polarity is rising edge. If FSXP/FSRP = 1, the frame sync polarity is falling edge.

NOTE: Certain restrictions apply to the receive and transmit logic settings, when MCASP_ACLKXCTL[6] ASYNC is set to 0b0. They are described in Section 23.8.4.2.4.

23.8.4.2.4 Synchronous and Asynchronous Transmit and Receive Operations

Synchronous Transmit and Receive Operations -

When MCASP_ACLKXCTL[6] ASYNC is written to 0b0, the transmit and receive sections operate synchronously to the transmit section clock and transmit frame sync signals.

Though Rx section may have a different data format , it has to be configured to have the same slot size than the transmit section one. As shown on the Figure 23-180, with the ASYNC bit set to 0b0, the RCLK becomes an inverted version of the transmit clock generator XCLK output.

When MCASP_ACLKXCTL[6] ASYNC = 0b0, both Rx and Tx sections use the same clock and frame sync signals. For this reason, they must be aligned on the following settings:

- MCASP_TXDITCTL[0] DITEN = 0 (that is, transmission in TDM mode is enabled)
- The total number of bits per frame must be the same (that is, RSSZ * RMOD product value must equal XSSZ * XMOD product value)
- The settings in MCASP_ACLKRCTL are NOT considered
- FSXM must match FSRM
- FXWID must match FRWID

For all other settings, the transmit and receive sections may be programmed independently.

Asynchronous Transmit and Receive Operations -

When MCASP_ACLKXCTL[6] ASYNC = 0b1, Tx and Rx operate independently from each other with separate clock and frame sync signals.

NOTE: Synchronous transmit and receive operations are allowed only in the MCASP TDM (I2S) mode (i.e. when MCASP_TXDITCTL[0] DITEN=0b0).

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23.8.4.3 Serializers

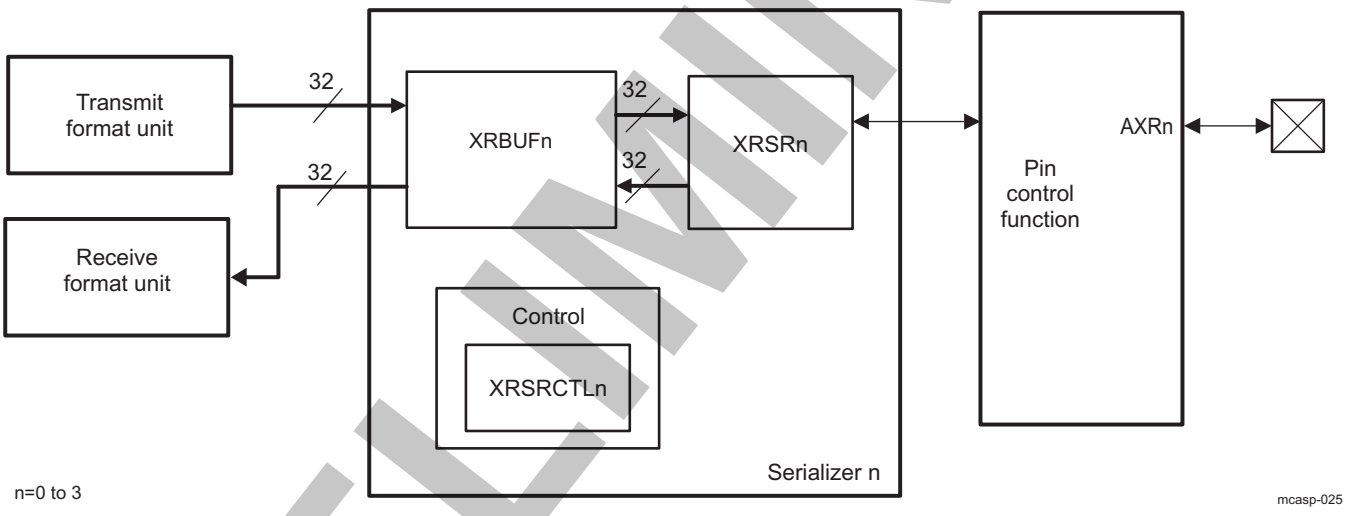
The four MCASP serializers shift serial data in (Rx) and out (Tx) of the MCASP. A given serializer n (where n=0 to 3) consists of a shift register (XRSRn) with a single-entry data buffer XRBUFn used either for transmitting (write accessible in register MCASP_TXBUFn) or for receiving (read accessible in register MCASP_RXBUFn) data. In addition, each serializer has a dedicated control register (MCASP_XRSRCTLn) and a serial bidirectional data pin - AXRn. The register MCASP_XRSRCTLn allows n-th serializer to be configured as a transmitter, receiver, or as inactive. There are transmit and receive data formatting units to support data alignment options of the MCASP which are shared between all Tx and Rx serializers, respectively.

A given serializer XRSRn shifter configured as a receiver in MCASP_XRSRCTLn, shifts in data through MCASP corresponding device level bidirectional data pad- (abemcasp_axr through abemcasp_axr3). A given serializer XRSRn shifter configured as a transmitter in MCASP_XRSRCTLn, shifts out data on MCASP corresponding device level bidirectional data pad -(abemcasp_axr through abemcasp_axr3).

The serializer is clocked from the transmit section clock (ACLKX signal) if configured to transmit or clocked from the receive section clock (ACLKR signal) if configured to receive. A serializer configured to transmit and receive operates in lockstep, which means that for MCASP there are at most a couple of zones, one for transmit and one for receive.

Figure 23-182 is the serializer block diagram.

Figure 23-182. Individual Serializer and Connections Within MCASP



Transmission on the n-th serializer (where n=0 to 3 for the device) is performed as follows: the microprocessor unit (MPU) services the MCASP by writing data into the register MCASP_TXBUFn, which is an alias of the serializer data buffer - XRBUFn for transmit function. The data automatically passes through the transmit format unit before reaching the XRBUFn register in the serializer. The data is then copied from the XRBUFn to XRSRn and shifted out from AXRn synchronously to the serial clock.

Reception from the n-th serializer (where n=0 to 3 for the device) is performed as follows: the data is shifted into the MCASP XRSRn serializer register through the AXRn pin, bit by bit. Once the entire slot becomes available within the XRSRn shift register, the data is copied into the serializer data buffer - XRBUFn ,and can be accessed in the MCASP_RXBUFn register, which is an alias of the serializer data buffer - XRBUFn for receive function. When MPU reads data from this register, the MCASP passes the data through the receive format unit, hence it returns formatted data to the MPU.

Serializer controls:

A serializer n is configured as inactive via setting bitfield MCASP_XRSRCTLn[1:0] SRMOD to 0x0.

For a transmitting serializer, the MCASP_XRSRCTLn[3:2] DISMOD bitfield, defines the AXRn pin output state, during inactive slots (HIGH, LOW or Hi-Z).

Transmit function for the n-th serializer is selected via setting bitfield MCASP_XRSRCTLn[1:0] SRMOD to 0x1.

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Receive function for the n-th serializer is selected via setting bitfield MCASP_XRSRCTLn[1:0] SRMOD to 0x2.

In the DIT-transmission mode (that is S/PDIF format data transmission) : in addition to the data, the serializer shifts out other DIT-specific information accordingly (preamble, user data, etc.). For more information, see Section 23.8.2.2.5

23.8.4.4 Format Units

The MCASP has one transmit data formatting unit and one receive data formatting unit, shared between the device 4 MCASP serializers. These units automatically remap the data bits within the transmitted or received words between a natural format for the MPU (such as a Q31 representation) and the required format for the external serial device (for example I2S format). During the remapping process, the format unit can also mask off certain bits.

Since all transmitters share the same data formatting unit, the MCASP only supports one transmit format at a time. For example, the MCASP does NOT transmit in "I2S format" on serializer 0, while transmitting "Left Justified" on serializer 1. Likewise, the receiver section of the MCASP only supports one data format at a time, and this format applies to all receiving serializers.

NOTE: The MCASP can transmit in one format while receiving in a completely different format.

The bit mask and pad stage of each of Tx and Rx format units includes a full 32-bit mask register, allowing selected individual bits to either pass through the stage unchanged, or be masked off. The bit mask and pad then pad the value of the masked off bits by inserting either a 0, a 1, or one of the original 32 bits as the pad value. The last option allows for sign-extension when the sign bit is selected to pad the remaining bits. The rotate right stage performs bitwise rotation by a multiple of 4 bits (between 0 and 28 bits), programmable by the MCASP_RXFMT / MCASP_TXFMT register. Note that this is a rotation process, not a shifting process, so bit 0 gets shifted back into bit 31 during the rotation. The bit order - reversal stage either passes all 32 bits directly through, or swaps them. This allows for either MSB or LSB first data formats. If bit order reversal is not enabled, then the MCASP will naturally transmit and receive in an LSB first order. Finally, note that the RDATDLY / XDATDLY bits in the MCASP_RXFMT / MCASP_TXFMT also determine the data format. For example, the difference between I2S format and left-justified is determined by the delay between the frame sync edge and the first data bit of a given time slot. For I2S format, RDATDLY / XDATDLY should be set to a 1-bit delay, whereas for left-justified format, it should be set to a 0-bit delay. The combination of all the options in MCASP_RXFMT / MCASP_TXFMT means that the MCASP supports a wide variety of data formats, both on the serial data lines, and in the internal CPU (MPU or DSP) data representation.

23.8.4.4.1 Transmit Format Unit

The MCASP transmit formatting unit consists of three stages :

- Bit mask (masks off bits)
- Rotate right (aligns data within word)
- Bit reversal (selects between MSB-first or LSB-first)

Figure 23-183 shows the transmit formatting unit.

The MCASP transmitter supports serial formats of :

- Slot (or Time slot) size = 8, 12, 16, 20, 24, 28, 32 bits
- Word size <= Slot size
- Alignment: when more bits/slot than bits/words, then:
  - Left aligned = word shifted first, remaining bits are pad
  - Right aligned = pad bits are shifted first, word occupies the last bits in slot
- Order of bits shifted out:
  - MSB: most-significant bit of word is shifted out first, last bit is LSB
  - LSB: least-significant bit of word is shifted out last, last bit is MSB

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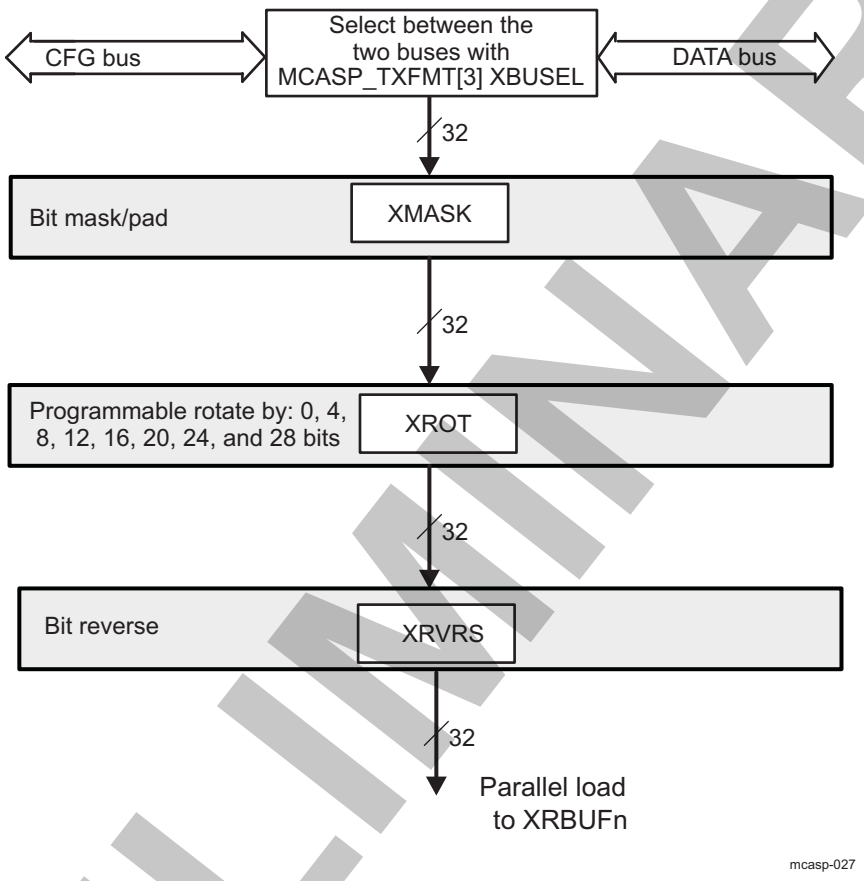
Hardware support for these serial formats comes from the programmable options in the bitstream format register - MCASP_TXFMT:

- XRVRS: bit reverse (1) or no bit reverse (0)
- XROT: rotate right by 0, 4, 8, 12, 16, 20, 24, or 28 bits
- XSSZ: receive slot size of 8, 12, 16, 20, 24, 28, or 32 bits

Figure 23-183. Transmit Format Unit



As shown in Figure 23-183, the data to the transmit format unit can come from the configuration port (CFG) or the data port (DATA). The selection is made through the MCASP_TXFMT[3] XBUSEL bit. According to port type selected, data transfer has different behaviour. For more details, refer to the Section 23.8.4.10.1.3, *Transfers Through the DATA Port*, and Section 23.8.4.10.1.4, *Transfers Through the Configuration (CFG) Bus*.

In the transmit format unit (TFU), the input data bits are first masked-off with the MCASP_TXMASK[31:0] XMASK contents. The masked data is then right-rotated to MCASP_TXFMT[2:0] XROT positions, to produce the output word for a TDM- or DIT- transmission.

The bit mask stage includes a full 32-bit mask register, allowing selected individual bits to pass through the stage unchanged or be masked off.

23.8.4.4.1.1 TDM Mode Transmission Data Alignment Settings

The TDM-mode transmission settings are relevant for I2S-protocol and protocols using more than 2 TDM-slots.

XSSZ should always be programmed to match the slot size of the serial stream. **Note that, TDM word size is not directly programmed into the MCASP, but rather is used to determine the rotation needed in the XROT field.**

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The Table 23-568 show the XRVRS and XROT fields for each serial format and for both integer and Q31 fractional internal representations.

The Table 23-568 assumes that all slot size (SLOT in Table 23-568) and word size (WORD in Table 23-568) options are multiples of 4, since the transmit rotate right unit only supports rotation by multiples of 4. However, the bit mask/pad unit does allow for any number of significant digits. For example, a Q31 number may have 19 significant digits (word) and be transmitted in a 24-bit slot; this would be formatted as a word size of 20 bits and a slot size of 24 bits. However, it is possible to set the bit mask unit to only pass the 19 most-significant digits (program the mask value to FFFF E000h). The digits that are not significant can be set to a selected pad value, which can be any one of the significant digits, a fixed value of 0, or a fixed value of 1.

The transmit bit mask/pad unit operates on data as an initial step of the transmit format unit, and the data is aligned in the same representation as it is written to the transmitter by the MPU or DSP (typically Q31 or integer).

Table 23-568. MCASP TFU TDM Mode Settings

Bit Stream Order	Bit Stream Alignment	Internal Numeric Representation	MCASP_TXFMT bits	
			XROT[1]	XRVRS
MSB first[2]	Left aligned	Q31 fraction	0	1
MSB first	Right aligned	Q31 fraction	SLOT - WORD	1
LSB first	Left aligned	Q31 fraction	32 - WORD	0
LSB first	Right aligned	Q31 fraction	32 - SLOT	0
MSB first[2]	Left aligned	Integer	WORD	1
MSB first	Right aligned	Integer	SLOT	1
LSB first	Left aligned	Integer	0	0
LSB first	Right aligned	Integer	(32 - (SLOT - WORD)) % 32	0

(1) WORD = Word size rounded up to the nearest multiple of 4; SLOT = slot size; % = modulo operator

(2) To transmit in I2S format, select MSB first, left aligned, and also select XDATDLY = 01 (1 bit delay)

23.8.4.4.1.2 DIT Mode Transmission Data Alignment Settings

In case of a DIT-mode (S/PDIF protocol) transmission, while left-aligned Q31 data should be right-rotated to a multiple by 4 positions, no right-rotation is required for a right-aligned Q31 data. Because this is a rotation process, not a shifting process, bit 0 gets shifted back into bit 31 during the process.

The MCASP_TXFMT[17:16] XDATDLY bit field must be set to a 0-bit delay (0x0 value).

For left-aligned Q31 data, the following transmit format unit settings process the data into right-aligned data, ready for transmission:

- MCASP_TXFMT[2:0] XROT =
  - 0x2 (rotate right by 8 bits) - for a 24-bit output audio data
  - 0x3 (rotate right by 12 bits) - for a 20-bit output audio data
  - 0x4 (rotate right by 16 bits) - for a 16-bit output audio data
- MCASP_TXFMT[15] XRVRS = 0x0 – Bit reversal is not enabled; the MCASP naturally transmits and receives in a LSB-first order.
- MCASP_TXMASK[32] XMASK = 0xFFFFFF00 – 0xFFFF0000
- MCASP_TXFMT[14:13] XPAD = 0x0 (Pad extra bits with 0s.)

For right-aligned data, the following transmit format unit settings process the data into right-aligned audio data ready for transmission:

- MCASP_TXFMT[2:0] XROT = 0x0 (rotate right by 0 bits regardless of the audio word length)
- MCASP_TXFMT[15] XRVRS = 0x0 – Bit reversal is not enabled; the MCASP naturally transmits and receives in a LSB-first order.
- MCASP_TXMASK[32] XMASK = 0x00FFFFFF – 0x0000FFFF

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- MCASP_TXFMT[14:13] XPAD = 0x0 (Pad extra bits with 0s.)

The example settings provided in Table 23-569 should be applied to MCASP in cases of DIT-transmitting a Q31 data as a 24-bit, 20-bit and 16-bit left- or right- aligned audio word, respectively. Note that the listed settings let the MCASP TFU preserve the most significant bits and cut only the LSBs of the original Q31 MPU data:

Table 23-569. MCASP TFU DIT-Mode Example Settings

Output Audio Word Alignment	Audio Word Length	Right-rotation (multiple of 4-bit positions)	XMASK	XROT
LEFT	16	16	0xFFFF0000	0x4
LEFT	20	12	0xFFFFF000	0x3
LEFT	24	8	0xFFFFFF00	0x2
RIGHT	16	0	0x0000FFFF	0x0
RIGHT	20	0	0x000FFFFF	0x0
RIGHT	24	0	0x00FFFFFF	0x0

Assuming that a Q31 data word 0xFA5AFxxx (where x-marked nibbles of the data are applied as padding bits of the word) is generated by MPU on the MCASP CFG (peripheral) port. To transmit a left-aligned 20-bit version of same word, preserving the MSBs, according to the Table 23-569, the user must set XMASK=0xFFFFF000, and to select a right-rotation to 12 positions (XROT=0x3).

- After applying 0-s (XPAD=0) as masking-off bits at the first TFU stage, word is transformed to the word 0xFA5AF000.
- After a rotation by 12 positions to the right is performed in TFU, the 20-bit output word obtained is : 0x000FA5AF.Thus the word gets ready for transmission being mapped with its LS-bit as bit 8 and its MS-bit as bit 27 within a S/PDIF bitstream. This word is shifted in a LSB-to-MSB order (XRVRS = 0x0) out of the XRSR register during a DIT-transmission.

Assuming that a right-aligned Q31 data word - 0x yyyyE4B4 is generated by MPU on the MCASP CFG (peripheral) port (with the presumption that y-marked nibbles of the input data are applied as padding bits). To transmit a right-aligned 16-bit version of same word, preserving the MSBs, according to the table MCASP TFU Example Settings, user is supposed to set XMASK=0x0000FFFF, and to select right-rotation to 0 positions (XROT=0x0).

- After masking-off with 0s at first TFU stage, word is transformed to 0x0000E4B4.
- Since no rotation is applied, the 16-bit output word obtained is actually the one obtained in the masking stage – 0x0000E4B4.

The above examples use internal representation in integer and Q31 notation, but other fractional notations are also possible.

23.8.4.4.2 Receive Format Unit

The MCASP receive formatting unit consists of three stages:

- Bit mask (masks off bits)
- Rotate right (aligns data within word)
- Bit reversal (selects between MSB first or LSB first)

Figure 23-184 shows the receive format unit (RFU).

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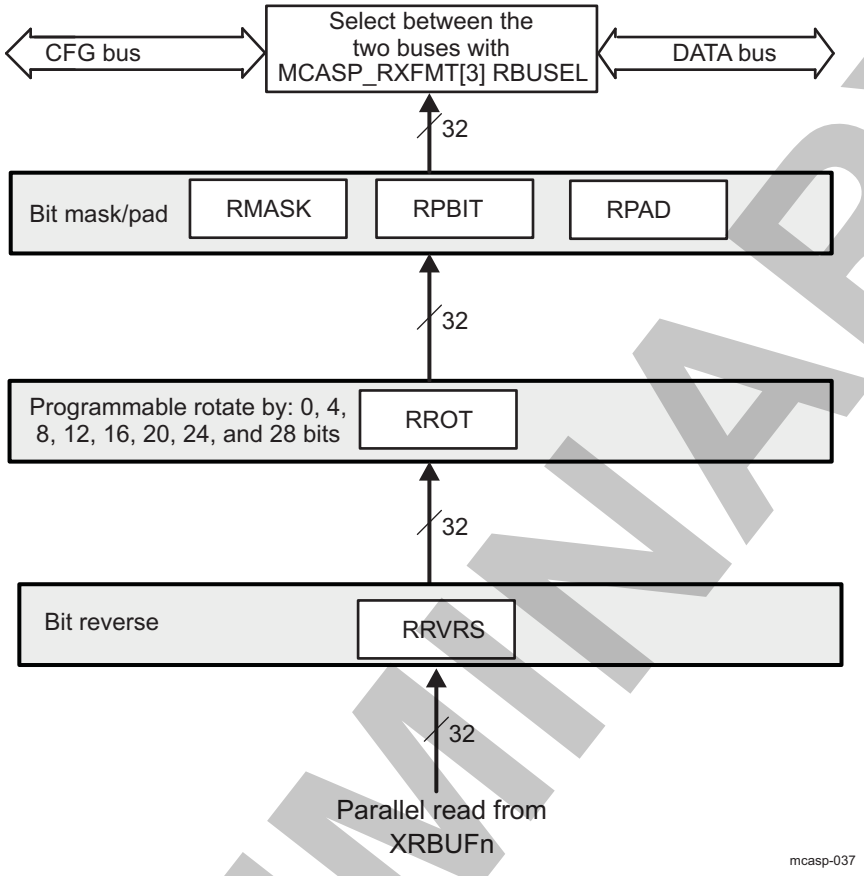
Figure 23-184. Receive Format Unit



The MCASP receiver supports serial formats of:

- Slot or time slot size = 8, 12, 16, 20, 24, 28, 32 bits
- Word size <= Slot size
- Alignment when more bits are available per slot than bits per word within the slot, then:
  - Left aligned = word shifted first, remaining bits are pad
  - Right aligned = pad bits are shifted first, word occupies the last bits in slot
- Order of bits shifted out:
  - MSB: most-significant bit of word is shifted out first, last bit is LSB
  - LSB: least-significant bit of word is shifted out last, last bit is MSB

Hardware support for these serial formats comes from the programmable options in the receive bitstream format register - MCASP_RXFMT:

- RRVRS: bit reverse (1) or no bit reverse (0)
- RROT: rotate right by 0, 4, 8, 12, 16, 20, 24, or 28 bits
- RSSZ: receive slot size of 8, 12, 16, 20, 24, 28, or 32 bits

As shown on Figure 23-184, the data processed in the RFU can be output to CPUs (device MPU / DSP) through the configuration port (CFG) or the data port (DATA). The selection is made through the MCASP_RXFMT[3] RBUSEL bit. According to port type selected, data transfer has different behaviour. For more details, refer to the Section 23.8.4.10.1.3, *Transfers Through the DATA Port*, and Section 23.8.4.10.1.4, *Transfers Through the Configuration (CFG) Bus*.

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23.8.4.4.2.1 TDM Mode Reception Data Alignment Settings

RSSZ should always be programmed to match the slot size of the serial stream. **Note that the word size is not directly programmed into the MCASP, but rather is used to determine the rotation needed in the RROT field.**

Table 23-570shows the RRVRS and RROT fields for each serial format and for both integer and Q31 fractional internal representations.

Table 23-570. MCASP RFU Settings

Bit Stream Order	Bit Stream Alignment	Internal Numeric Representation	MCASP_RXFMT bits	
			RROT(1)	RRVRS
MSB first(2)	Left aligned	Q31 fraction	SLOT	1
MSB first	Right aligned	Q31 fraction	WORD	1
LSB first	Left aligned	Q31 fraction	(32 - (SLOT - WORD)) % 32	0
LSB first	Right aligned	Q31 fraction	0	0
MSB first(2)	Left aligned	Integer	SLOT - WORD	1
MSB first	Right aligned	Integer	0	1
LSB first	Left aligned	Integer	32 - SLOT	0
LSB first	Right aligned	Integer	32 - WORD	0

(1) WORD = Word size rounded up to the nearest multiple of 4; SLOT = slot size; % = modulo operator

(2) To receive in I2S format, select MSB first, left aligned, and also select RDATDLY = 01 (1 bit delay)

The Table 23-570 assumes that all slot size and word size options are multiples of 4; since the receive rotate right unit only supports rotation by multiples of 4. However, the bit mask / pad unit does allow for any number of significant digits. For example, a Q31 number may have 19 significant digits (word) and be transmitted in a 24-bit slot; this would be formatted as a word size of 20 bits and a slot size of 24 bits. However, it is possible to set the bit mask unit to only pass the 19 most-significant digits (program the mask value to FFFF E000h). The digits that are not significant can be set to a selected pad value, which can be any one of the significant digits, a fixed value of 0, or a fixed value of 1. The receive bit mask / pad unit operates on data as the final step of the receive format unit (see Figure 23-184), and the data is aligned in the same representation as it is read from the receiver by the DSP (typically Q31 or integer).

23.8.4.5 State-Machines

The receive and transmit sections have independent state machines.

Each state-machine controls the interactions between the various units in the MCASP Rx and Tx sections, respectively. In addition, each state-machine keeps track of error conditions and serial port status. No serial transfers can occur until the RX / TX state-machine is released from reset.

The transmit state-machine is controlled by the transmit bitstream format register (MCASP_TXFMT) and it reports the MCASP status and error conditions in the transmitter status register (MCASP_TXSTAT).

Similarly, the receive state-machine is controlled by the receive bitstream format register (MCASP_RXFMT) and it reports the MCASP status and error conditions in the receiver status register (MCASP_RXSTAT).

23.8.4.6 TDM Sequencers

There are separate TDM sequencers for the transmit section and the receive section. Each TDM sequencer keeps track of the slot count. In addition, the TDM sequencer checks the bits of MCASP_RXTDM / MCASP_TXTDM and determines if the MCASP should receive/transmit in that time slot.

There are two possibilities for a slot: The MCASP either performs Rx / Tx operations during the time slot (transmit / receive bit is active), or the MCASP skips Rx / Tx operations during the time slot (transmit/receive bit is inactive). In the latter case, no transfers between the XRBUF and XRSR registers in the serializer would occur during that time slot.

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In addition, during time of inactive slots, the serializers programmed as transmitters place their data output pins - AXRn in a predetermined state - logic low, high, or high impedance (tri-stated) as programmed in each serializer control register MCASP_XRSRCTLn[3:2] DISMOD. Refer also to section Section 23.8.4.9.1.1, *TDM Time Slots Generation and Processing*, for details on how DMA event or interrupt generations are handled during inactive time slots in TDM mode.

In case of a DIT-transmission (S/PDIF transfers): the time division multiplexing (TDM) sequencer is used to count the 384 subframes (slots) in the DIT block. If currently transmitting slot 1, slot 2 (next value of the TDM slot counter) should be used during the encode phase to select the appropriate C, V, and U bit, because the data encoded and written to a MCASP_TXBUFn (where n=0 to 3) register during the current time slot (slot 1) is actually shifted out on the next time slot.

The transmit TDM sequencer is controlled by the MCASP_TXTDM register and reports the current transmit slot to the MCASP_TXTDMSLOT[8:0] XSLOTCNT bit field.

23.8.4.7 MCASP Software Reset

The MCASP can be put into reset through the global transmit and receive control register (MCASP_GBLCTL). A valid serial clock must be supplied to the MCASP to assert the software reset bits in the MCASP_GBLCTL register.

23.8.4.8 MCASP Power Management

Table 23-571 describes power-management features available to the MCASP.

Table 23-571. Local Power-Management Features

Feature	Registers	Description
Slave idle modes	MCASP_SYSCONFIG[1:0] IDLE_MODE	Force-idle, no-idle, and smart-idle modes are available.

CAUTION

No wakeup schema is supported for the MCASP. To ensure a correct behavior after enabling MCASP at device PRCM level, the user software is strongly recommended to choose **No Idle** mode, setting MCASP_SYSCONFIG[1:0] IDLE_MODE to 0x1. Before disabling MCASP at device PRCM level, user software is strongly recommended to choose a **Smart-Idle** mode, setting MCASP_SYSCONFIG[1:0] IDLE_MODE to 0x2.

23.8.4.9 Transfer Modes

23.8.4.9.1 Time-Division Multiplexed (TDM) Transfer Mode

The MCASP time-division multiplexed (TDM) transfer mode supports the TDM format discussed in Section 23.8.2.2.3.

Transmitting data in the TDM transfer mode requires a minimum set of pins:

- ACLKX - transmit bit clock
- AFSX - transmit frame sync (or commonly called left/right clock)
- One or more serial data pins, AXRn (where n=0 to 3 in the device), whose serializers are configured to transmit

For more details on MCASP transmitting serializers clock and frame sync options, refer to the section Section 23.8.4.2.1, *Transmit Clock*, and Section 23.8.4.2.3, *Frame-Sync Generator* .

Similarly, to receive data in the TDM transfer mode requires a minimum set of pins:

- ACLKR - receive bit clock
- AFSR - receive frame sync (or commonly called left/right clock)

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- One or more serial data pins, AXRn (where n= 0 to 3 for the device) , whose serializers are configured to receive

For more details on MCASP receiving serializers clock and frame sync options, refer to the Section 23.8.4.2.2, *Receive Clock*, and Section 23.8.4.2.3, *Frame-Sync Generator* .

The control registers must be configured as follows for the TDM mode. The TDM mode specific bit fields are highlighted in bold :

- MCASP_PFUNC : The clock, frame, data pins must be configured for MCASP function.
- MCASP_PDIR: The clock, frame, data pins must be configured to the direction desired.
- MCASP_PDOUT, MCASP_PDIN, MCASP_PDSET, MCASP_PDCLR : Not applicable. Leave at default.
- MCASP_GBLCTL : Follow the initialization sequence is described in the Section 23.8.5.2, *Operational Modes Configuration*.
- MCASP_AMUTE: Program all fields according to mute control desired.
- MCASP_LBCTL: If loopback mode is desired, configure this register according to Section 23.8.4.14, otherwise leave this register at default.
- MCASP_TXDITCTL: DITEN must be left at default 0 to select TDM mode (transmitters only).
- MCASP_RXMASK / MCASP_TXMASK: Mask desired bits according to Section 23.8.4.4, *Format Units*.
- MCASP_RXFMT / MCASP_TXFMT: Program all fields according to data format desired. See the Section 23.8.4.4, *Format Units*.
- MCASP_RXFMCTL / MCASP_TXFMCTL : Set RMOD / XMOD bits to (0x2 - 0x20) for Rx / Tx (2- 32 slots) TDM mode. In addition, set RMOD to 0x180 if 384-slot TDM stream has to be received by MCASP. Configure other fields as desired.
- MCASP_ACLKRCTL / MCASP_ACLKXCTL : Program all fields according to bit clock desired. For more inforamtion , refer to Section 23.8.4.2.
- MCASP_AHCLKRCTL / MCASP_AHCLKXCTL: Program all fields according to high-frequency clock desired. For more details, refer to Section 23.8.4.2.
- MCASP_RXTDM / MCASP_TXTDM : Program all fields according to the time slot characteristics desired.
- MCASP_EVTCTLX : Program all fields according to transmit interrupts desired.
- MCASP_RXCLKCHK / MCASP_TXCLKCHK: Program all fields according to clock checking desired.
- MCASP_XRSRCTLn : Program all fields according to serializer operation desired.

NOTE: The MCASP_DITCSRAi, MCASP_DITCSRBi, MCASP_DITUDRAi, MCASP_DITUDRBi (i=0 to 5) settings are NOT applicable in TDM transfer modes. They have to be kept at their default values.

23.8.4.9.1.1 TDM Time Slots Generation and Processing

TDM mode on the MCASP can extend to support multiprocessor applications, with up to 32 time slots per frame. For each of the time slots, the MCASP may be configured to participate or to be inactive by configuring MCASP_TXTDM and/or MCASP_RXTDM registers.

The TDM sequencer (separate ones for transmit and receive) functions in this mode. The TDM sequencer counts the slots beginning with the frame sync. For each slot, the TDM sequencer checks the respective bit in either MCASP_TXTDM or MCASP_RXTDM to determine if the MCASP transmits / receives in that time slot.

NOTE: If a MCASP_TXTDM / MCASP_RXTDM bit defines an active slot (number of slot matches the bit position), the MCASP functions normally during that time slot; otherwise, the MCASP is inactive during that time slot; no update to the buffer occurs, and no event is generated. MCASP (transmit only) data pins are automatically set to a high-impedance state, 0, or 1 during that slot, as determined by bitfield MCASP_XRSRCTLn[3:2] DISMOD.

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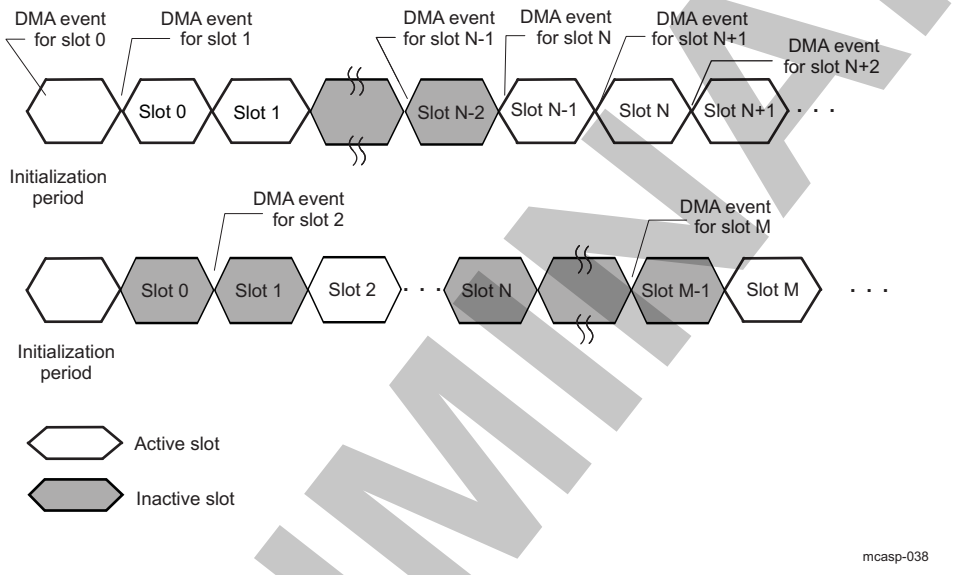
Figure 23-185 shows when the transmit DMA event - AXEVT is generated. See Section 23.8.4.10.1, *Data Ready Status and Event / Interrupt Generation* for details on data ready and the initialization period indication. The transmit DMA event for an active time slot (slot N) is generated during the previous time slot (slot N - 1), regardless of the previous time slot (slot N - 1) being active or inactive.

During an active transmit time slot (slot N), if the next time slot (slot N + 1) is configured to be active, the copy from XRBUFn to XRSRn generates the DMA event for time slot N + 1. If the next time slot (slot N + 1) is configured to be inactive, then the DMA event will be delayed to time slot M - 1. In this case, slot M is the next active time slot. The DMA event for time slot M is generated during the first bit time of slot M - 1.

The receive DMA event is generated after data is received in the buffer (looks back in time). If a time slot is disabled, then no data is copied to the buffer for that time slot and no DMA event is generated.

Figure 23-185. Transmit DMA Event (AXEVT) Generation in TDM Time Slots



23.8.4.9.1.2 Special 384-Slot TDM Mode for Connection to External DIR

The MCASP receiver also supports a 384 time slot TDM mode (DIR mode), to support S/PDIF receiver ICs whose natural block (block corresponds to MCASP frame) size is 384 samples. The receive TDM time slot register (MCASP_RXTDM) should be programmed to all 1s during reception of a DIR block. **Other TDM functionalities (for example, inactive slots) are not supported (only the slot counter counts the 384 subframes in a block).** To receive data in DIR mode, the following pins are typically needed:

- ACLKR - receive bit clock
- AFSR - receive frame sync (or commonly called left/right clock)
- In this mode, AFSR should be connected to a DIR which outputs a start of block signal, instead of LRCLK
- One or more serial data pins, AXRn, whose serializers have been configured to receive (n=0 to 3)
- For this special DIR mode, the control registers can be configured just as for TDM mode, except set RMOD in MCASP_RXFMCTL to 384 (0x180) to receive 384 time slots

23.8.4.9.2 DIT Transfer Mode

The DIT transfer mode of the MCASP also supports transmission of audio data in S/PDIF, AES-3, and IEC-60958 formats. These formats are designed to carry audio data between different systems through an optical or coaxial cable. **The DIT mode applies only to a serializer configured as transmitter, NOT receiver.** For a description of the S/PDIF format, see Section 23.8.2.2.5, *S/PDIF Coding Format*.

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23.8.4.9.2.1 Transmit DIT Encoding

When the MCASP operates in DIT mode, the data transmitted is output as a biphase-mark encoded bitstream, with preamble, channel status, user data, validity, and parity automatically stuffed into the bitstream by the MCASP. The MCASP includes separate validity bits for even/odd subframes and two 384-bit RAM modules to hold channel status and user data bits.

NOTE: The transmit TDM time slot register (MCASP_TXTDM) should be programmed to all 1s during DIT mode. TDM functionality is not supported in DIT mode, except that the TDM slot counter counts the DIT subframes.

To transmit data in DIT mode, the following pins are typically required:

- AHCLKX – transmit high-frequency master clock (The internal clock source can be used instead.)
- One serial data pin (AXRn) of a serializer n configured to transmit.

The actual 24-bit audio data must always be in bit positions 23–0 after passing through the first three stages of the transmit format unit.

23.8.4.9.2.2 Transmit DIT Clock and Frame-Sync Generation

The DIT transmitter works only in the following configuration:

- In the transmit frame control register (MCASP_TXFMCTL):
  - Internally generated transmit frame sync, FSXM = 1
  - Rising-edge frame sync, FSXP = 0
  - Bit-width frame sync, FXWID = 0
  - 384-slot TDM, XMOD = 1 1000 0000b
- In the transmit clock control register (MCASP_ACLKXCTL), ASYNC = 1
- In the transmit bitstream format register (MCASP_TXFMT), XSSZ = 1111 (32-bit slot size)

All combinations of abemcasp_ahclkx and abemcasp_aclkx are supported.

The following summarizes the register configurations required for DIT mode. DIT mode-specific bit fields are in bold face:

- MCASP_PFUNC: The data pin - AXRn (n=0 to 3) must be configured for MCASP function. If abemcasp_ahclkx is used, it must also be configured for MCASP function. Other pins can be configured to function as GPIOs, if desired.
- MCASP_PDIR: The data pin must be configured as output. If internal clock source AUXCLK is used as the reference clock, it may be output as the abemcasp_ahclkx device level signal by configuring AHCLKX pin as an output.
- MCASP_GBLCTL: Global initialization
- MCASP_AMUTE: Program all fields according to the mute control desired.
- MCASP_TXDITCTL: The **DITEN** bit must be set to 0b1 to enable DIT mode. Configure other bits as desired.
- **MCASP_TXMASK**: Mask the desired bits, depending upon left-aligned or right-aligned internal data.
- **MCASP_TXFMT: XDATDLY** = 0. **XRVRS** = 0. **XPAD** = 0. **XSSZ** = Fh (32-bit slot). XBUSEL = configured as desired. The **XROT** bit is configured, as described in the Section 23.8.4.4.1.2 .
- **MCASP_TXFMCTL**: Configure the bits according to former discussions.
- **MCASP_ACLKXCTL**: **ASYNC** = 1. Program the CLKXDIV bits to obtain the bit clock rate desired. CLKXM = 1.
- **MCASP_AHCLKXCTL**: Program the HCLKXDIV bits to obtain the high-frequency bit clock rate desired.
- **MCASP_TXTDM**: Set to FFFF FFFFh for all active slots for DIT transfers.
- MCASP_EVTCTLX: Program all fields according to the interrupts desired.
- MCASP_TXCLKCHK: Program all fields according to the clock checking desired.

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- MCASP_XRSRCTLn: Set **SRMOD** = 1 (transmitter) for the DIT pins.
- **MCASP_DITCSRAi** and **MCASP_DITCSRBi**: Program the channel status bits as desired.
- **MCASP_DITUDRAi** and **MCASP_DITUDRBi**: Program the user data bits as desired.

NOTE: In DIT mode, the transmitter can support a 192 kHz frame rate (stereo) on up to 2 serial data pins simultaneously (note that the internal bit clock for DIT runs two times faster than the equivalent bit clock for TDM (I2S) mode, due to the need to generate Biphase Mark Encoded Data - see Section 23.8.2.2.5.1).

23.8.4.9.2.3 DIT Channel Status and User Data Register Files

The channel status registers (MCASP_DITCSRAi and MCASP_DITCSRBi) and user data registers (MCASP_DITUDRAi and MCASP_DITUDRBi) are not double-buffered. Typically, programmers use one of the synchronizing interrupts, such as the last slot, to create an event at a safe time so the register may be updated. In addition, the MPU reads the transmit TDM slot counter to determine which word of the register is being used.

It is a software requirement to avoid writing to the word of user data and channel status that are being used to encode the current time slot; otherwise, it is undetermined whether old or new data is used to encode the bitstream.

The DIT subframe format is defined in Section 23.8.2.2.5.2, *S/PDIF Subframe Format*. The channel status information (C) and user data (U) are defined in the following DIT control registers:

- MCASP_DITCSRA0 to MCASP_DITCSRA5: The 192 bits in these six registers contain the channel status information for the left channel within each frame.
- MCASP_DITCSRB0 to MCASP_DITCSRB5: The 192 bits in these six registers contain the channel status information for the right channel within each frame.
- MCASP_DITUDRA0 to MCASP_DITUDRA5: The 192 bits in these six registers contain the user data information for the left channel within each frame.
- MCASP_DITUDRB0 to MCASP_DITUDRB5: The 192 bits in these six registers contain the user data information for the right channel within each frame.
- The S/PDIF block format is shown in Figure 23-176. There are 192 frames within a block (frame 0 to frame 191). There are two subframes within each frame (subframes 1 and 2 for the left and right channels, respectively).

The channel status and user data information sent on each subframe is summarized in Table 23-572.

Table 23-572. Channel Status and User Data for Each DIT Block

Frame	Subframe	Preamble	Channel Status Defined in:	User Data Defined in:
Defined by DITCSRA0, DITCSRB0, DITUDRA0, DITUDRB0				
0	1 (L)	B	DITCSRA0[0]	DITUDRA0[0]
0	2 (R)	W	DITCSRB0[0]	DITUDRB0[0]
1	1 (L)	M	DITCSRA0[1]	DITUDRA0[1]
1	2 (R)	W	DITCSRB0[1]	DITUDRB0[1]
2	1 (L)	M	DITCSRA0[2]	DITUDRA0[2]
2	2 (R)	W	DITCSRB0[2]	DITUDRB0[2]
…	…	…	…	…
31	1 (L)	M	DITCSRA0[31]	DITUDRA0[31]
31	2 (R)	W	DITCSRB0[31]	DITUDRB0[31]
Defined by DITCSRA1, DITCSRB1, DITUDRA1, DITUDRB1				
32	1 (L)	M	DITCSRA1[0]	DITUDRA1[0]
32	2 (R)	W	DITCSRB1[0]	DITUDRB1[0]
…	…	…	…	…
63	1 (L)	M	DITCSRA1[31]	DITUDRA1[31]

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Table 23-572. Channel Status and User Data for Each DIT Block (continued)

Frame	Subframe	Preamble	Channel Status Defined in:	User Data Defined in:
63	2 (R)	W	DITCSRB1[31]	DITUDRB1[31]
Defined by DITCSRA2, DITCSRB2, DITUDRA2, DITUDRB2				
64	1 (L)	M	DITCSRA2[0]	DITUDRA2[0]
64	2 (R)	W	DITCSRB2[0]	DITUDRB2[0]
…	…	…	…	…
95	1 (L)	M	DITCSRA2[31]	DITUDRA2[31]
95	2 (R)	W	DITCSRB2[31]	DITUDRB2[31]
Defined by DITCSRA3, DITCSRB3, DITUDRA3, DITUDRB3				
96	1 (L)	M	DITCSRA3[0]	DITUDRA3[0]
96	2 (R)	W	DITCSRB3[0]	DITUDRB3[0]
…	…	…	…	…
127	1 (L)	M	DITCSRA3[31]	DITUDRA3[31]
127	2 (R)	W	DITCSRB3[31]	DITUDRB3[31]
Defined by DITCSRA4, DITCSRB4, DITUDRA4, DITUDRB4				
128	1 (L)	M	DITCSRA4[0]	DITUDRA4[0]
128	2 (R)	W	DITCSRB4[0]	DITUDRB4[0]
…	…	…	…	…
159	1 (L)	M	DITCSRA4[31]	DITUDRA4[31]
159	2 (R)	W	DITCSRB4[31]	DITUDRB4[31]
Defined by DITCSRA5, DITCSRB5, DITUDRA5, DITUDRB5				
160	1 (L)	M	DITCSRA5[0]	DITUDRA5[0]
160	2 (R)	W	DITCSRB5[0]	DITUDRB5[0]
…	…	…	…	…
191	1 (L)	M	DITCSRA5[31]	DITUDRA5[31]
191	2 (R)	W	DITCSRB5[31]	DITUDRB5[31]

23.8.4.10 Data Transmission and Reception

The MPU services the MCASP by writing data to the MCASP_TXBUFn registers for transmit operations, and by reading data from the MCASP_RXBUFn registers for receive operations. The MCASP sets status flags and notifies the MPU whenever data is ready to be serviced. The Section 23.8.4.10.1, *Data Ready Status and Event/Interrupt Generation*, discusses data-ready status in details.

The MCASP transmit / receive XRBUFn buffer can be accessed through one of the two peripheral ports of the device:

- DATA port: This port is dedicated to DMA_SYSTEM and DMA_DSP initiated data transfers on the device for MCASP transmit (Tx) purposes.
- Configuration bus (CFG): The configuration bus- CFG port is used for peripheral configuration control and receive / transmit data transfers initiated by the CPU (MPU Cortex-A15 or DSP) in the device.

Section 23.8.4.10.1.3, *Transfers Through the Data Port (DATA)*, and Section 23.8.4.10.1.4, *Transfers Through the Configuration Bus (CFG),* discuss how to perform transfers through the data port (DATA) and the configuration port (CFG), respectively.

The MPU and DMA usages are discussed in Section 23.8.4.10.1.5, *Using the MPU for MCASP Servicing*, and Section 23.8.4.10.1.6, *Using the DMA for MCASP Servicing*, respectively.

MCASP DATA port allows DMAs (both DMA_DSP and DMA_SYSTEM) to access the MCASP transmit buffer more efficiently on the L3_MAIN-interconnect, using burst transfers. The physical addresses to access these registers are listed in Table 23-686.

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23.8.4.10.1 Data Ready Status and Event/Interrupt Generation

23.8.4.10.1.1 Transmit Data Ready

The transmit data ready flag - XDATA in the MCASP_TXSTAT register reflects the data ready status of XRBUFn buffers (where n=0 to 3 for the device) for all of the active slot transmitting serializers. The XDATA flag is set whenever data is transferred from a transmitting serializer buffer - XRBUFn (where n=0 to 3) to its corresponding XRSRn shift register. Thus, the XDATA bit indicates the global event that some of the serializers data buffer - XRBUFn is emptied and ready to accept new data from the host (MPU/ DSP or DMAs). The transmit data ready event is individually indicated per serializer in its corresponding control register MCASP_XRSRCTLn[4] XRDY status bit. When this bit is set to 0b1, it notifies to host that this serializer Tx buffer must be serviced (written). When MCASP_TXBUFn is written to by the host, the MCASP_XRSRCTLn[4] XRDY is deasserted to 0b0. As XDATA global flag is an OR-event of all active serializers XRDY flags, it indicates to software the moment, when write service operation has to be initiated by the MCASP host (XDATA=0b1). The XRDY flags have to be sequentially scanned by user software to determine which serializer MCASP_TXBUFn register has to be currently written. Once all requested MCASP_TXBUFn are written, the serializers control XRDY flags are cleared to 0b0. As a consequence, XDATA flag is deasserted to 0b0, to indicate to SW that write operation is completed for all serializers.

The global XDATA flag can be cleared when the MCASP_TXSTAT[5] XDATA bit is written to 0b1, or once MCASP_TXBUFn registers of all the serializers, that have previously raised their XRDY flags, are written with corresponding active slot data by the host.

Whenever XDATA is set, the DMA AXEVT event is automatically generated (if enabled in the MCASP_TXEVTCTL register) to notify the DMA of the MCASP_TXBUFn empty status. An interrupt - MCASP_IRQ_AXEVT can be also generated if the XDATA interrupt is enabled in the MCASP_EVTCTLX register (for details, see Section 23.8.4.11.1, *Transmit Data Ready Interrupt*).

For DMA requests, the MCASP does not require that MCASP_TXSTAT be read between DMA events. This means that, even if MCASP_TXSTAT already has the XDATA flag set to 1 from a previous request, the next transfer triggers another DMA request.

Because the serializer acts in lockstep, only one DMA event is generated to indicate that the transmit serializer is ready to be written to with new data.

Figure 23-186 shows the timing details of when AXEVT is generated at the MCASP boundary. In this example, as soon as the last bit (A0) of word A is transmitted, the MCASP sets the XDATA flag and generates an AXEVT event. However, it takes up to five MCASP system clocks (AXEVT latency) before AXEVT is active at the MCASP boundary. Upon AXEVT, the DSP / MPU can begin servicing the MCASP by writing word C into the MCASP_TXBUFn (service time). The MPU must write word C into the MCASP_TXBUFn within the setup time required by the MCASP (setup time).

The maximum service time (see Figure 23-186) can be calculated as:

Service Time = Time Slot – AXEVT Latency –Setup Time

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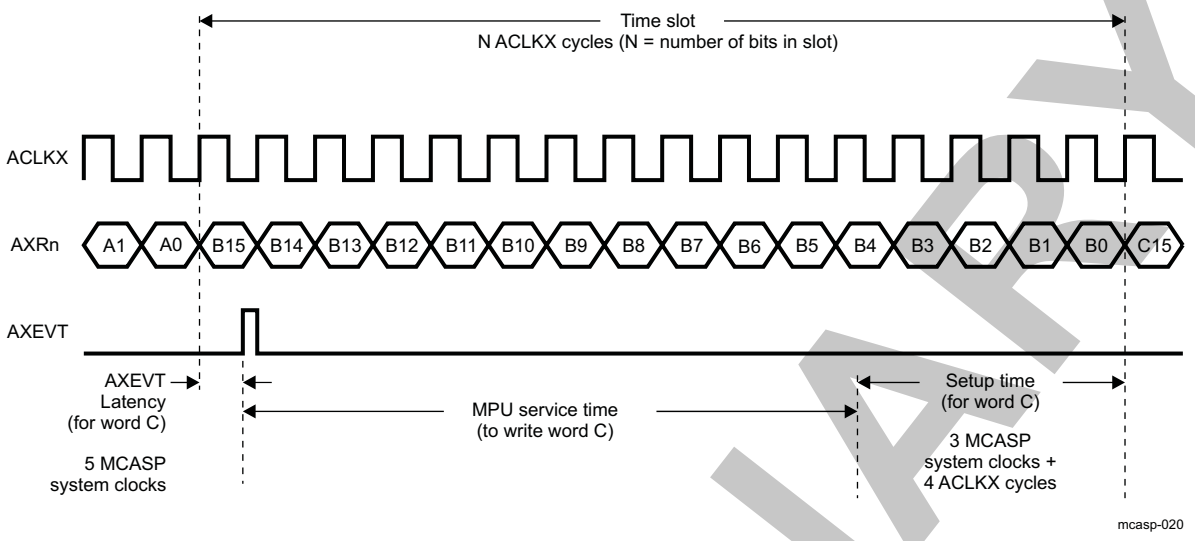
Figure 23-186. MPU Service Time Upon Transmit DMA Event (AXEVT)



23.8.4.10.1.2 Receive Data Ready

Similarly, the receive data ready flag - RDATA in the MCASP_RXSTAT register reflects the data ready status of XRBUFn buffers (where n=0 to 3 for the device) for all of the **active slot receiving serializers**. The RDATA flag is set whenever data is transferred from a receiving serializer shift register XRSRn to its corresponding XRBUFn data buffer. Thus, the RDATA bit indicates the global event that some of the receivers data buffer - RXBUFn already contains received data (i.e. a buffer is full) and is ready to transfer it to the host (MPU / DSP). The receive data ready event is individually indicated per serializer in its corresponding control register MCASP_XRSRCTLn [5] RRDY status bit. When this bit is set to 0b1, it notifies to host that this serializer Rx buffer must be serviced (read). When MCASP_RXBUFn is read from the host, the MCASP_XRSRCTLn [5] RRDY is deasserted to 0b0. As RDATA global flag is an OR-event of all active serializers RRDY flags, it indicates to software the moment, when read service operation has to be initiated by the MCASP host (RDATA=0b1). The RRDY flags have to be sequentially scanned by user software to determine which serializer MCASP_RXBUFn register has to be currently read. Once all requested MCASP_RXBUFn are read, the serializers control RRDY flags are cleared to 0b0. As a consequence, RDATA flag is deasserted to 0b0, to indicate to SW that read operation is completed for all serializers.

The global RDATA flag can be cleared when the MCASP_RXSTAT[5] RDATA bit is written to 0b1, or once MCASP_RXBUFn registers of all the serializers, that have previously raised their RRDY flags, are read by the host.

Figure 23-187 shows the timing details of when AREVT event is generated at the MCASP boundary. In this example, as soon as the last bit (bit A0) of Word A is received, the MCASP sets the RDATA flag and generates an AREVT event. However, it takes up to five MCASP system clocks (AREVT Latency) before AREVT is active at the MCASP boundary. Upon AREVT, the DSP / MPU can begin servicing the MCASP by reading Word A from the MCASP_RXBUFn (service time). The DSP / MPU must read Word A from the MCASP_RXBUFn register no later than the setup time required by the MCASP (Setup Time).

The maximum service time (see Figure 23-187) can be calculated as:
Service Time = Time Slot - AREVT Latency - Setup Time

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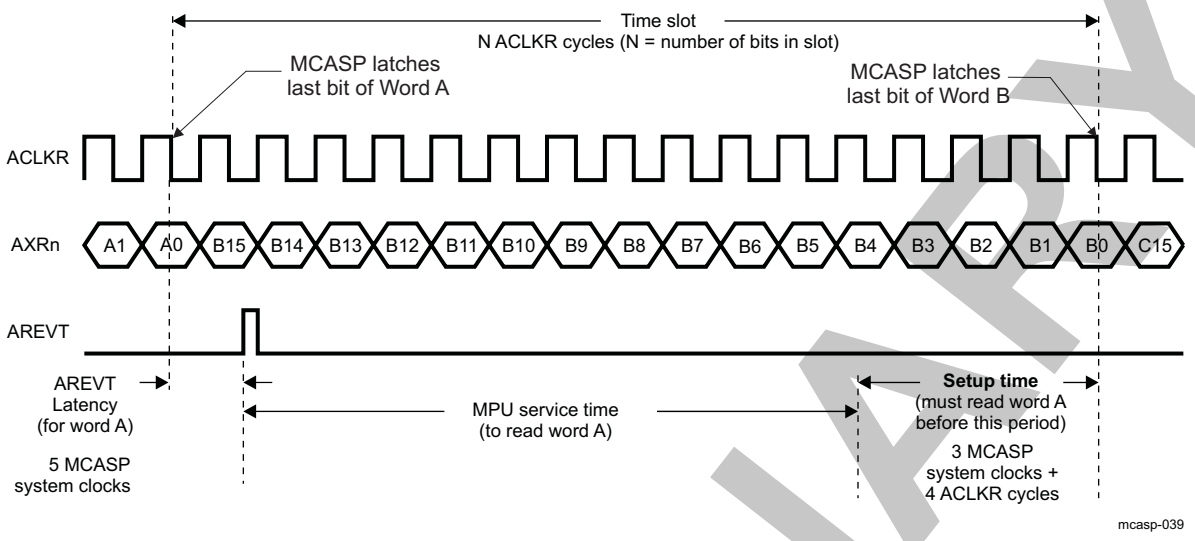
Figure 23-187. MPU Service Time Upon Receive Event (AREVT)



23.8.4.10.1.3 Transfers Through the Data Port (DATA)

CAUTION

To perform internal transfers through the DATA port, clear the XBUSEL / RBUSEL bit to 0b0 in the MCASP_TXFMT / MCASP_RXFMT register, respectively. Failure to do so may result in software malfunction.

In a typical MCASP transfer scenario, the DMA_SYSTEM or DMA_DSP write accesses the XRBUFn transmit buffer (where n= 0 to 3) through the MCASP data port (DATA) on L3_MAIN. MPU and DSP hosts can access both XRBUFn transmit and receive data buffers on their corresponding DATA port address for MPU / DSP private access or via DATA port corresponding address on L3_MAIN. To perform transfers through the DATA port, simply have the DMA_SYSTEM / DMA_DSP write the MCASP Tx buffer through L3_MAIN DATA port location. The MPU / DSP write or read access corresponding Tx / Rx buffer through L3_MAIN or MPU / DSP private access DATA port location, as specified in the Table 23-686.

NOTE: DMA_SYSTEM and DMA_DSP can be used to serve only **transmit (Tx) channel data transfers** through DATA port on L3_MAIN. This is because MCASP AREVT event is NOT linked to DMA_SYSTEM / DMA_DSP in the device.

For accesses through the DATA port, the DMAs / MPU or DSP service all the serializers through accessing only a single address. In addition, as can be seen in Table 23-686, **the same physical DATA port address is used regardless of a read or write access is performed** by device MPU / DSP. The MCASP automatically cycles through the **active slot** transmitting / receiving serializers, internally generating the appropriate offsets.

NOTE: DATA port allows the DMAs / MPU or DSP to automatically access only the data buffers. There is no way for DMAs / MPU or DSP to access the MCASP configuration registers addressing their corresponding MCASP DATA port.

For transmit operations through the DATA port, **the host must always write to the same transmit buffer DATA port address** (which is same than the receive buffer DATA port adress) to service all of the active slot transmitting serializers. Regardless of MCASP serializer 0 being configured inactive or active, the user software must always configure the DMAs (DMA_SYSTEM or DMA_DSP) / MPU or DSP destination address to match the **DATA port location of XRBUFn buffer**.

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In addition, the DMAs / MPU or DSP must write the buffers of all transmitting serializers in incremental (although not necessarily consecutive) order. For example, if only serializers 1 and 3 are set up as active transmitters, the DMAs / MPU or DSP should write to the same transmit buffer DATA port address twice - first data for serializer 1 and second data for serializer 3 upon each transmit data ready event. This exact servicing order must be followed so that data appears in the appropriate serializers.

NOTE: For write transfers through MCASP DATA port it is preferable to use DMA_SYSTEM / DMA_DSP on L3_MAIN. This is because DMAs initiated traffic gets better advantage of the burst transfers supported by DATA port.

For receive operations through the DATA port, **the MPU or DSP must always read from the same receive buffer DATA port address** (which is same than the transmit buffer DATA port adress) to service all of the active slot receiving serializers. Regardless of MCASP serializer 0 being configured inactive or active, the user software must always configure the MPU or DSP source address to match the **DATA port location of XRBUFn buffer**.

In addition, reads from the receive buffer for all active slot receiving serializers through the Rx DATA port return data in incremental (although not necessarily consecutive) order. For example, if serializers 0, 1 and 3 are set up as active receivers, the MPU or DSP should read from the same receive buffer DATA port address three times to obtain data for serializers 0,1 and 3 in this exact order, upon each receive data ready event.

NOTE: To service a serializer for a transmit or receive operation through the MCASP DATA port, the initiator always writes (preferably DMA_SYSTEM and DMA_DSP) and reads (MPU and DSP only) from the same address (refer to Table 23-686), respectively.

See Section 23.8.6.2.3, *MCASP_DATA Register Summary*, for more details about XRBUFn buffer physical address corresponding to the MCASP DATA port on:

- L3_MAIN.
- DSP private access bus.
- MPU private access bus.

NOTE: When transmitting through the DATA port, the DMAs / MPU or DSP must write data (at the same address) to each serializer configured as **active** (active slot selected in MCASP_TXTDM) and **transmit** (Tx enabled in MCASP_XRSRCTLn) within each time slot. Failure to do so results in a buffer underrun condition (see Section 23.8.4.15.1, *Buffer Underrun Error - Transmitter*). Similarly, when MPU / DSP receives, data must be read from each serializer configured as **active** (active slot selected in MCASP_RXTDM) and **receive** (Rx enabled in MCASP_XRSRCTLn) within each time slot. Failure to do results in a buffer overrun condition (see Section 23.8.4.15.2 , *Buffer Overrun Error - Receiver*).

23.8.4.10.1.4 Transfers Through the Configuration Bus (CFG)

CAUTION

To perform internal transfers through the configuration bus, set the XBUSEL / RBUSEL bit to 1 in the MCASP_TXFMT / MCASP_RXFMT registers, respectively. Failure to do so may result in software malfunction.

In this method, the DMAs / MPU or DSP accesses the XRBUFn transmit or receive buffer (only DSP and MPU) through corresponding configuration bus (CFG) address.

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The exact XRBUFn transmit / receive buffer physical address for any particular serializer is determined by adding the transmit / receive buffer alias register offset for that particular serializer to the base address of MCASP CFG port actual for L3_MAIN accesses or device MPU / DSP private accesses. The XRBUF buffer of the n-th serializer (n=0 to 3) configured as a transmitter is aliased - MCASP_TXBUFn in the CFG port address space. For example, the XRBUF2 transmit buffer is mapped as the MCASP_TXBUF2 register. Similarly, the XRBUF buffer of the n-th serializer (n=0 to 3) configured as a receiver is aliased - MCASP_RXBUFn in the CFG port address space. For example , the XRBUF3 receive buffer is mapped as the MCASP_RXBUF3 register.

Accessing the XRBUF through the DATA port (see Section 23.8.4.10.1.3) is different than CFG port accesses because the DATA port access demands the same physical address, regardless of transfer direction or current channel index , while accessing through the peripheral configuration port - CFG, the DMA, MPU or DSP must provide the exact MCASP_TXBUFn or MCASP_RXBUFn (MPU and DSP only) address upon accessing n-th serializer TX or RX buffer, respectively. For more details about MCASP_TXBUFn and MCASP_RXBUFn (where n=0 to 3) addresses corresponding to MCASP CFG port, see Section 23.8.6.2.1, *MCASP_CFG Register Summary*.

23.8.4.10.1.5 Using the MPU or DSP for MCASP Servicing

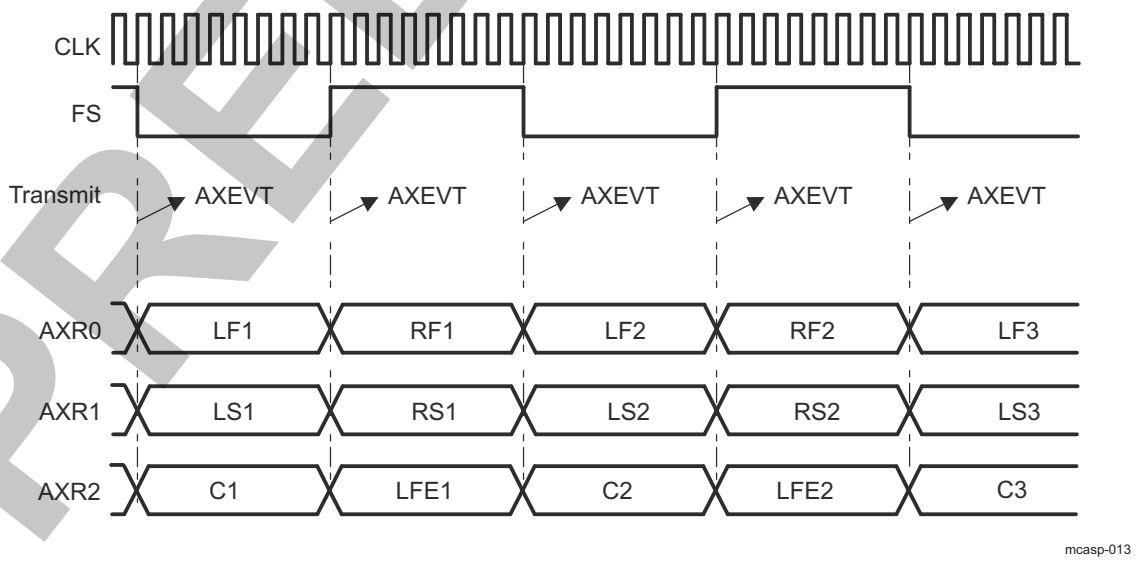
The MPU or DSP can be used to service the MCASP transmit channels through interrupts (upon MCASP_IRQ_AXEVT interrupt). Another way to service the transmit and receive channels, a polling of the XDATA bit in the MCASP_TXSTAT register and RDATA bit in the MCASP_RXSTAT register can be performed by device CPUs, respectively. As discussed in Section 23.8.4.10.1.3, *Transfers Through the Data Port (DATA)*, and Section 23.8.4.10.1.4, *Transfers Through the Configuration Bus (CFG)* , the MPU and DSP can access MCASP XRBUF serializer buffer through their corresponding DATA and CFG port locations.

To use the MPU or DSP to service the MCASP transmitter through interrupts, the XSTAT bit must be enabled in the MCASP_EVTCTLX register, to generate the MCASP_IRQ_AXEVT interrupt to the MPU / DSP subsystem interrupt controllers upon data ready.

23.8.4.10.1.6 Using the DMA for MCASP Servicing

The typical scenario is to use the DMA_SYSTEM / DMA_DSP to service the MCASP transmit logic through the DATA port, although the DMA can also service the MCASP transmit logic through the configuration bus (CFG). DMA_SYSTEM and DMA_DSP can NOT be used to service MCASP receive logic, and the device CPUs (device MPU / DSP) must directly read back MCASP_RXSTAT[5] RDATA flag and MCASP_XRSRCTLn[5] RRDY, to appropriately service the AREVT events.

Figure 23-188. DMA Transmit Event in an Audio Example – One Event



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The DMA event - AXEVT (MCASP_DREQ_AXEVT output), which is triggered upon each XDATA transition from 0 to 1, is used to service the MCASP XRBUFn transmit buffers.

Figure 23-188 is an example of an audio system with six audio channels (LF, RF, LS, RS, C and LFE) transmitted through the MCASP signals - AXR0 (device signal - abemcasp_axr), AXR1 (device signal - abemcasp_axr1) and AXR2 (device signal - abemcasp_axr2). It shows the points at which event AXEVT is triggered.

In Figure 23-188, a Tx DMA event AXEVT is triggered on each time slot. In the example, AXEVT is triggered for each of the transmit audio channel time slot (time slot for channels LF, LS, and C; and time slot for channels RF, RS, LFE). Transmit DMA events are generated automatically upon transmit data ready, **provided that DMA TX requests generation is enabled in the MCASP_TXEVTCTL register.**

23.8.4.11 Events and Interrupt Requests

Table 23-573 lists all the event flags. Only the transmit events are capable to generate MCASP module interrupts in the device. Source of each of these TX / RX events can be a TX / RX channel from MCASP serializer 0 through serializer 3.

Table 23-573. TX Events[1]

Event Mask	Event Flag	Map to	Description
MCASP_EVTCTLX[0] XUNDRN	MCASP_TXSTAT[0] XUNDRN	MCASP_IRQ_AXEVT	Transmit buffer underrun
MCASP_EVTCTLX[1] XSYNCERR	MCASP_TXSTAT[1] XSYNCERR	MCASP_IRQ_AXEVT	Unexpected transmit frame sync
MCASP_EVTCTLX[2] XCKFAIL	MCASP_TXSTAT[2] XCKFAIL	MCASP_IRQ_AXEVT	Transmit clock failure
MCASP_EVTCTLX[3] XDMAERR	MCASP_TXSTAT[7] XDMAERR	MCASP_IRQ_AXEVT	DATA port transmit error
MCASP_EVTCTLX[4] XLAST	MCASP_TXSTAT[4] XLAST	MCASP_IRQ_AXEVT	Transmit last slot interrupt
MCASP_EVTCTLX[5] XDATA	MCASP_TXSTAT[5] XDATA	MCASP_IRQ_AXEVT	Transmit data-ready interrupt
MCASP_EVTCTLX[7] XSTAFRM	MCASP_TXSTAT[6] XSTAFRM	MCASP_IRQ_AXEVT	Transmit start of frame interrupt
n.a.	MCASP_TXSTAT[8] XERR	n.a.	OR-event of all Tx-error events: (XDMAERR | XCKFAIL | XUNDRN | XSYNCERR). It is cleared ONLY when all error flags are cleared
n.a.	MCASP_TXSTAT[3] XTDMSLOT	n.a.	Qualifies the current TDM slot as an odd or an even slot.

(1) Global events for all transmitting serializers n (where n=0 to 3 in the device).

Table 23-574. RX Events[1]

Event Flag[2]	Description
MCASP_RXSTAT[0] ROVRN	Receive buffer overrun
MCASP_RXSTAT[1] RSYNCERR	Unexpected receive frame sync
MCASP_RXSTAT[2] RCKFAIL	Receive clock failure
MCASP_RXSTAT[7] RDMAERR	DATA port receive error
MCASP_RXSTAT[4] RLAST	Receive last slot
MCASP_RXSTAT[5] RDATA	Receive data-ready
MCASP_RXSTAT[6] RSTAFRM	Receive start of frame
MCASP_RXSTAT[8] RERR	OR-event of all Rx-error events: (RDMAERR | RCKFAIL | ROVRN | RSYNCERR). RERR event is cleared once all error flags are cleared.
MCASP_RXSTAT[3] RTDMSLOT	Qualifies the current TDM slot as an odd or an even slot.

(1) Global events for all receiving serializers n (where n=0 to 3 in the device).
(2) The MCASP receive logic events are not mapped to a MPU / DSP INTC interrupt line.

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Software has to read the MCASP_TXSTAT / MCASP_RXSTAT register to determine which event occurs at a global level for MCASP Tx / Rx logic. In addition user software has to scan the XRDY / RRDY read-only flags in the MCASP_XRSRCTLn (where n= 0 to 3 in the device) registers to determine which active serializer is the actual source of the event.

A Tx interrupt line (MCASP_IRQ_AXEVT) is asserted (active high) when one of the MCASP_TXSTAT notified events occurs, provided that it is enabled in its corresponding MCASP_EVTCTLX bit. See also Section 23.8.4.11.4, *Multiple Interrupts* and the Section 23.8.4.10.1, *Data Ready Status and Event / Interrupt Generation*.

NOTE: At device level, there is no interrupt line to MPU_INTC and INTC_DSP associated with the MCASP AREVT event.

23.8.4.11.1 Transmit Data Ready Event and Interrupt

The transmit data-ready interrupt (XDATA) is generated if XDATA is 1 in the MCASP_TXSTAT register and XDATA is enabled in MCASP_EVTCTLX. The Section 23.8.4.10.1, *Data Ready Status and Event/Interrupt Generation*, provides details on when XDATA is set in the MCASP_TXSTAT register.

A transmit-start-of-frame interrupt (XSTAFRM) is triggered by the recognition of a transmit frame sync.

A transmit-last-slot interrupt (XLAST) is a qualified version of the data-ready interrupt (XDATA). It has the same behavior than the data-ready interrupt, but is further qualified by having the data requested belonging to the last slot (the slot that just ended is the next-to-last TDM slot, the current slot is the last slot).

23.8.4.11.2 Receive Data Ready Event

The Section 23.8.4.10.1, *Data Ready Status and Event/Interrupt Generation*, provides details on when RDATA flag is set in the MCASP_RXSTAT register.

A receiver start of frame (RSTAFRM) event is triggered by the recognition of a receiver frame sync.

A receiver last slot (RLAST) event is a qualified version of the data ready (RDATA) event. It has the same behavior as the data ready event, but is further qualified by having the data in the buffer come from the last TDM time slot (the slot that just ended was last TDM slot).

23.8.4.11.3 Error Interrupt

Upon detection, the following error conditions generate interrupt flags:

In the transmit status register (MCASP_TXSTAT) :

- Transmit underrun (XUNDRN)
- Unexpected transmit frame sync (XSYNCERR)
- Transmit clock failure (XCKFAIL)
- Transmit DATA port error (XDMAERR)

Each interrupt source also has a corresponding enable bit in the transmit interrupt control register (MCASP_EVTCTLX). If the enable bit is set, an interrupt is requested when the interrupt flag is set in MCASP_TXSTAT. If the enable bit is not set, no interrupt request is generated. However, the interrupt flag may be polled.

In the receive status register (MCASP_RXSTAT) :

- Receiver overrun (ROVRN)
- Unexpected receive frame sync (RSYNCERR)
- Receive clock failure (RCKFAIL)
- Receive DATA port error (RDMAERR)

Because the MCASP receive error flags do NOT source interrupts in the device, these flags have to be explicitly polled by the CPUs (MPU / DSP) in the MCASP_RXSTAT register.

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23.8.4.11.4 Multiple Interrupts

This only applies to Tx interrupts and not to Tx DMA requests. The following terms are defined:

- **Active Interrupt Request:** a flag in MCASP_TXSTAT is set and the interrupt is enabled in MCASP_EVTCTLX.
- **Outstanding Interrupt Request:**An interrupt request has been issued on one of the MCASP transmit interrupt port, but that request has not yet been serviced.
- **Serviced:** The CPUs write to MCASP_TXSTAT to clear one or more of the active interrupt request flags.

The first interrupt request to become active for the transmitter with the interrupt flag set in MCASP_TXSTAT and the interrupt enabled in MCASP_EVTCTLX generates a request on the MCASP transmit interrupt port - AXINT.

If more than one interrupt request becomes active in the same cycle, a single interrupt request is generated on the MCASP transmit interrupt port. Subsequent interrupt requests that become active while the first interrupt request is outstanding do not immediately generate a new request pulse on the MCASP transmit interrupt port.

The transmit interrupt is serviced with the CPU writing to MCASP_TXSTAT. If any interrupt requests are active after the write, a new request is generated on the MCASP transmit interrupt port.

One outstanding interrupt request is allowed on Tx interrupt port.

23.8.4.12 DMA Requests

The MCASP can generate one DMA request to the DMA_SYSTEM and DMA_DSP controllers to transmit data (MCASP_DREQ_AXEVT). A DMA request to transmit data is generated if the XDATDMA bit in the MCASP_TXEVTCTL register is cleared.

NOTE: The MCASP receive logic AREVT event does NOT have associated DMA request line to the device DMA_SYSTEM and DMA_DSP.

23.8.4.13 Audio Mute (AMUTE) Function

The MCASP includes an automatic audio mute function (see Figure 23-189) that asserts, in hardware, the AMUTE pin (signal named "abemcasp_amuteout" at device level) to a preprogrammed output state, as selected by the MUTEN bit in the audio mute control register (MCASP_AMUTE). The AMUTE pin is asserted when one of the interrupt flags is set or an external device issues an error signal on the MCASP input pin AMUTEIN (signal named "abemcasp_amutein" at device level). Typically, the AMUTEIN input is shared with a device interrupt pin.

The device level abemcasp_amutein input signal (MCASP pin AMUTEIN) allows the on-chip logic to consider a mute input from other devices in the system so that all errors may be considered. The AMUTEIN input has a programmable polarity to allow it to adapt to different devices, as selected by the INPOL bit in the MCASP_AMUTE register, and it must be explicitly enabled.

In addition to the external abemcasp_amutein input, the device abemcasp_amuteout output signal (MCASP pin AMUTE) may be asserted when one of the error interrupt flags is set and its mute function is enabled in the MCASP_AMUTE register.

When one or more errors are detected and enabled, the abemcasp_amuteout signal is driven to an active state that is selected by MUTEN in the MCASP_AMUTE register. The active polarity of the MCASP AMUTE output is programmable by the MUTEN bit (the inactive polarity is the opposite of the active polarity). The AMUTE pin output remains driven active until software clears all the error interrupt flags that are enabled to mute, and until the MCASP AMUTEIN input is inactive.

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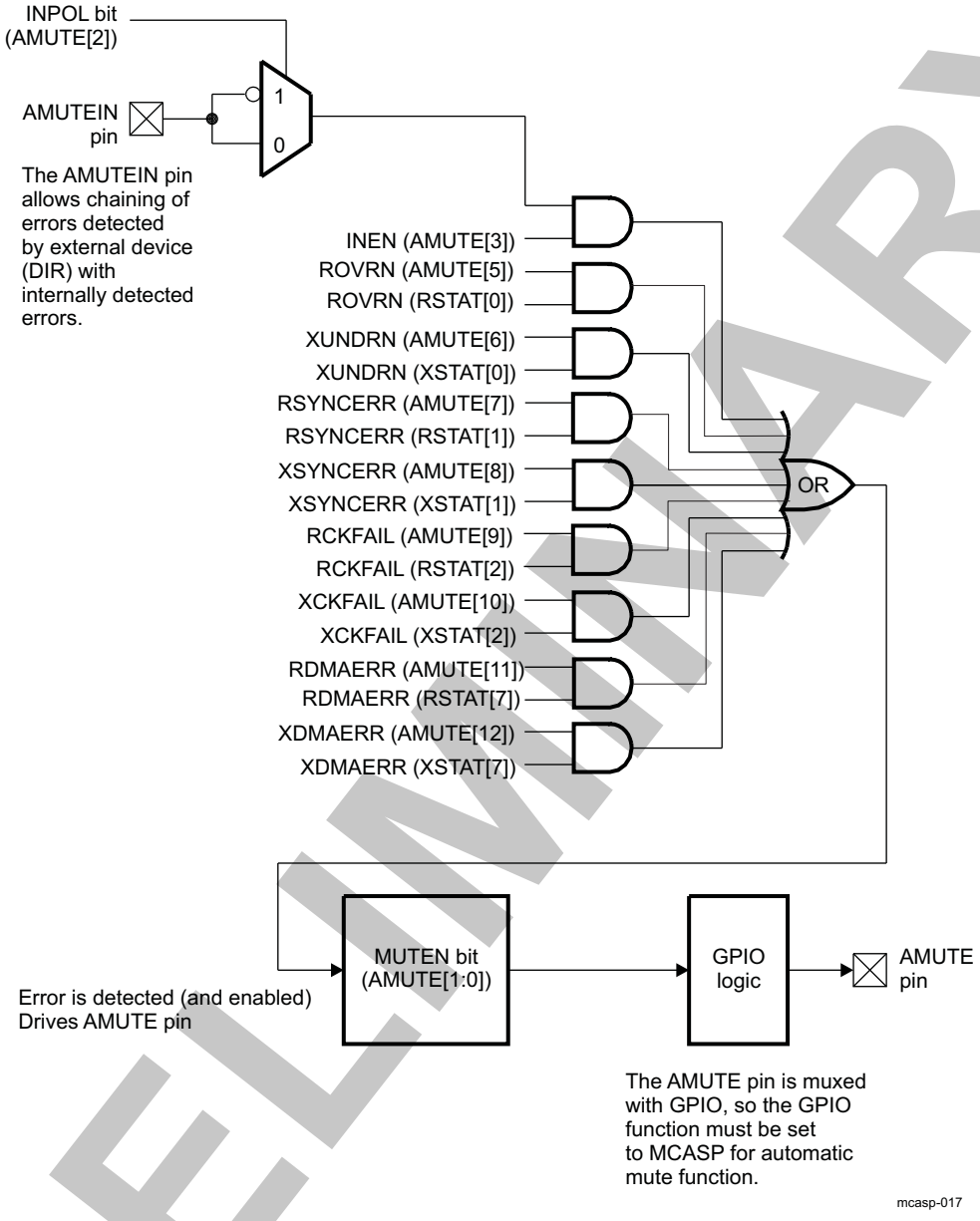
Figure 23-189. Audio Mute (AMUTE) Block Diagram



23.8.4.14 Loopback Modes

The MCASP features a digital loopback mode (DLB) that allows loopback test transfers in TDM mode between MCASP transmitters and receivers within the same device. In loopback mode, the output of a transmit serializer is connected internally to the input of a receive serializer. Therefore, a receiver data can be checked against a transmitter data to ensure that the MCASP settings are correct. Digital loopback mode applies to TDM mode only (2 to 32 slots in a frame). It does not apply to DIT mode (XMOD = 0x180).

Figure 23-190shows the basic logical connection of the serializers in loopback mode.

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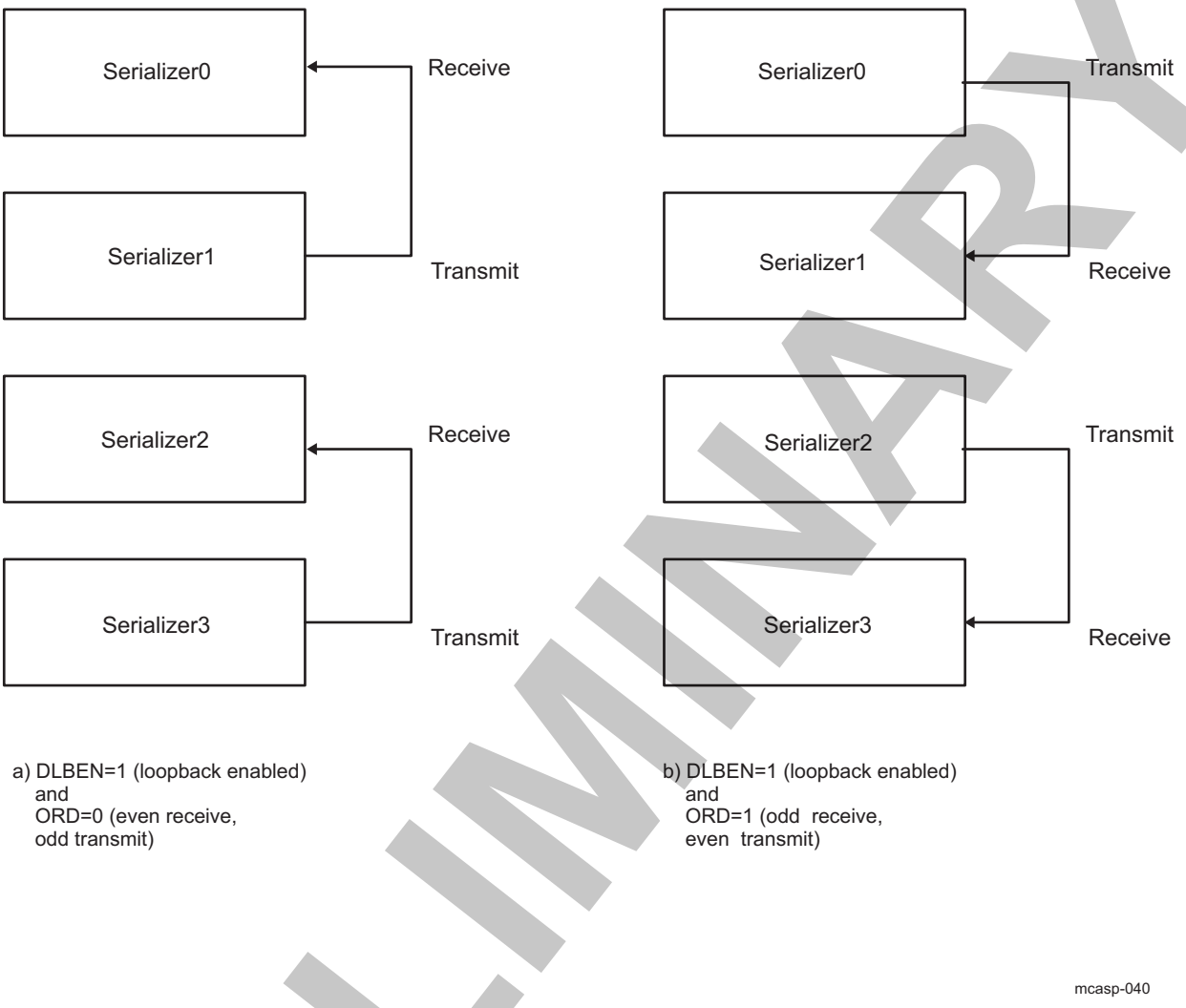
Figure 23-190. MCASP Serializers Operation in Loopback Mode



Two types of loopback connections are possible, selected by the ORD bit in the digital loopback control register - MCASP_LBCTL as follows:

- ORD = 0: Outputs of odd serializers are connected to inputs of even serializers. If this mode is selected, the odd serializers must be configured as transmitters and even serializers as receivers.
- ORD = 1: Outputs of even serializers are connected to inputs of odd serializers. If this mode is selected, the even serializers must be configured as transmitters and odd serializers as receivers.

User can choose in software (bit IOLBEN of the MCASP_LBCTL) between a MCASP module internal loopback and a device I/O level loopback.

When a **MCASP internal loopback** is selected (MCASP_LBCTL[4] IOLBEN=0b0), it is NOT necessary to configure MCASP_PFUNC and MCASP_PDIR registers for MCASP pin settings. Nevertheless, data can be optionally made externally visible at the I/O pin of the transmit serializer, if the pin is configured as a MCASP output pin by setting the corresponding MCASP_PFUNC bit to 0 (i.e. to function as MCASP, not GPIO) and MCASP_PDIR bit to 1 (output).

When a **device I/O level loopback** is selected (MCASP_LBCTL[4] IOLBEN=0b1), the MCASP_PFUNC and MCASP_PDIR registers must be configured with the appropriate settings for AXR0 through AXR3 pins, according to ORD bit configuration.

In case of device I/O loopback, the connectivity is externally applied between device pads (i.e. reaching device I/O buffers) corresponding to :

- abemcasp_axr

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- abemcasp_axr1 - abemcasp_axr3

Hence, the corresponding padconfiguration registers must be appropriately configured in the device Control Module - CTRL_MODULE_CORE_PAD. For more details, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in *Chapter 18, Control Module*.

When In loopback mode, the transmit clock and frame sync are used by both the transmit and receive sections of the MCASP. The transmit and receive sections operate synchronously. This is achieved by setting the MODE bitfield of the MCASP_LBCTL register to 0x1 and the ASYNC bit of the MCASP_ACLKXCTL register to 0b0.

23.8.4.14.1 Loopback Mode Configurations

This is a summary of the settings required for digital loopback mode for TDM format :

- The bit - MCASP_LBCTL[0] DLBEN must be set to 0b1 to enable a loopback mode. It must be kept at 0b0 during normal MCASP operation.
- The MCASP_LBCTL[4] IOLBEN bit must be set to select between internal (MCASP local) loopback mode or device I/O level loopback mode.
- The MCASP_LBCTL[3:2] MODE bitfield must be set to 0x1 for both the transmit and receive sections to use the transmit clock and frame sync generator.
- The MCASP_LBCTL[1] ORD must be programmed appropriately to select odd or even serializers to be transmitters or receivers.
- The corresponding serializers must be configured accordingly.
- The bit - MCASP_ACLKXCTL[6] ASYNC must be cleared to 0b0 to ensure synchronous transmit and receive operations.
- The bitfields - MCASP_RXFMCTL[15:7] RMOD and MCASP_TXFMCTL[15:7] XMOD must be set within range (0x2- 0x20) to indicate TDM mode.

NOTE: Loopback mode does not apply to DIT mode, because MCASP receivers do NOT natively support DIR - reception.

23.8.4.15 Error Reporting

The MCASP includes error-checking capability for the serial protocol and data underrun. In addition, the MCASP includes a timer that continually measures the high-frequency master clock every 32 AHCLKX / AHCLKR clock cycles. The value of the timer can be read to get a measurement of the clock frequency and has a minimum and maximum range setting that can set an error flag if the master clock goes out of a specified range.

When one or more errors (software selectable) are detected or the AMUTEIN input pin is asserted, the AMUTE output pin may be asserted to a high or low level to immediately mute the audio output. In addition, an interrupt can be generated if desired, based on one or more error sources.

23.8.4.15.1 Buffer Underrun Error -Transmitter

A buffer underrun occurs when a serializer (n=0 to 3) is instructed by the transmit state-machine to transfer data from XRBUFn buffer to XRSRn shift register, but the corresponding (MCASP_TXBUFn) register has not yet been written with new data since the last time the transfer occurred. When this occurs, the transmit state-machine sets the XUNDRN flag.

An underrun is checked only once per time slot. The MCASP_TXSTAT[0] XUNDRN flag is set when an underrun condition occurs. Once set, the XUNDRN flag remains set until the host explicitly writes 1 to the XUNDRN bit to clear it.

A pair of BMC zeros is shifted out when an underrun occurs (four bit times at 128 bfs). By shifting out a pair of zeros, a clock can be recovered on the receiver. To recover, reset the MCASP and restart with the proper initialization.

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23.8.4.15.2 Buffer Overrun Error-Receiver

A buffer overrun occurs when a serializer (n=0 to 3) is instructed to transfer data from XRSRn shift register to XRBUFn receiver buffer, but the corresponding MCASP_RXBUFn register has not yet been read since the last time the transfer occured. When this occurs, the receiver state machine sets the overrun flag - ROVRN. However, the individual serializer writes over the data in the XRBUFn buffer register (destroying the previous sample) and continues shifting.

An overrun is checked only once per time slot. The MCASP_RXSTAT[0] ROVRN flag is set when an overrun condition occurs. It is possible that an overrun occurs on one time slot but then the host catches up and does not cause an overrun on the following time slots. However, once the ROVRN flag is set, it remains set until the host - DSP / MPU explicitly writes a 1 to the ROVRN bit to clear the ROVRN bit.

23.8.4.15.3 DATA Port Error - Transmitter

A transmit DATA port error, as indicated by the XDMAERR flag in the MCASP_TXSTAT register, occurs when the DMA,MPU or DSP writes more words to the DATA port of the MCASP than it should.

The MCASP_TXSTAT[7] XDMAERR=0b1 indicates that the DMA , MPU or DSP wrote too many words to the MCASP DATA port for a given transmit DMA event. Writing too few words results in a transmit underrun error setting XUNDRN in MCASP_TXSTAT.

While XDMAERR occurs infrequently, an occurrence indicates a serious loss of synchronization between the MCASP and the DMA, MPU or DSP. The MCASP transmitter and the DMA must be reinitialized to resynchronize them.

23.8.4.15.4 DATA Port Error - Receiver

A receive DATA port error, as indicated by the RDMAERR flag in the MCASP_RXSTAT register, occurs when the MPU or DSP reads more words from the DATA port of the MCASP than it should.

The MCASP_RXSTAT[7] RDMAERR indicates that the MPU or DSP read too many words from the MCASP DATA port for a given receive AREVT event. Reading too few words results in a receiver overrun error setting ROVRN in MCASP_RXSTAT.

While RDMAERR occurs infrequently, an occurrence indicates a serious loss of synchronization between the MCASP and the MPU / DSP.

23.8.4.15.5 Unexpected Frame Sync Error

An unexpected frame sync occurs when the next active edge of the frame sync occurs early such that the current slot will not be completed by the time the next slot is scheduled to begin.

An unexpected frame sync occurs also if the frame sync does NOT occur exactly during the correct bit clock (not a cycle earlier or later) and before slot 0.

When an unexpected frame sync occurs, there are two possible actions depending upon when the unexpected frame sync occurs:

1. **Early:** An early unexpected frame sync occurs when the MCASP is in the process of completing the current frame and a new frame sync is detected (not including overlap that occurs due to a 1 or 2 bit frame sync delay). When an early unexpected frame sync occurs:
   - Error event flag is set (XSYNCERR, if an unexpected transmit frame sync occurs; RSYNCERR, if an unexpected receive frame sync occurs).
   - Current frame is not resynchronized. The number of bits in the current frame is completed. The next frame sync, which occurs after the current frame is completed, will be resynchronized.
1. **Late:** A late unexpected frame sync occurs when there is a gap or delay between the last bit of the previous frame and the first bit of the next frame. When a late unexpected frame sync occurs (as soon as the gap is detected):
   - Error event flag is set (XSYNCERR, if an unexpected transmit frame sync occurs; RSYNCERR, if an unexpected receive frame sync occurs).
   - Resynchronization occurs upon the arrival of the next frame sync.

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23.8.4.15.6 Clock Failure Detection

23.8.4.15.6.1 Clock Failure Check Startup

It is initially expected of the clock failure circuits to generate an error until at least one measurement is taken. Therefore, the clock failure interrupts, clock switch, and mute functions should not be enabled immediately, but only after a specific startup procedure.

To start the transmit clock failure check procedure:

1. Configure the transmit clock failure detect logic (XMIN, XMAX, XPS) in the transmit clock check control register (MCASP_TXCLKCHK).
2. Clear the transmit clock failure flag (XCKFAIL) in the transmit status register (MCASP_TXSTAT).
3. Wait until the first measurement is taken (> 32 AHCLKX clock periods).
4. Verify that no clock failure is detected.
5. Repeat Step 2 through Step 4 until the clock is running and is no longer issuing clock failure errors.
6. After the transmit clock is measured and falls within the acceptable range, the following can be enabled:
   (a) The transmit clock failure interrupt enable bit (XCKFAIL) in the transmitter interrupt control register (MCASP_EVTCTLX)
   (b) The mute option (XCKFAIL) in the mute control register (MCASP_AMUTE)

To start the receive clock failure check procedure:

1. Configure receive clock failure detect logic (RMIN, RMAX, RPS) in the receive clock check control register (MCASP_RXCLKCHK).
2. Clear receive clock failure flag (RCKFAIL) in the receive status register (MCASP_RXSTAT).
3. Wait until first measurement is taken (> 32 AHCLKR clock periods).
4. Verify no clock failure is detected.
5. Repeat steps 2–4 until clock is running and is no longer issuing clock failure errors.
6. After the receive clock is measured and falls within the acceptable range, the following may be enabled:
   (a) mute option (RCKFAIL) in the mute control register (MCASP_AMUTE)

23.8.4.15.6.2 Transmit Clock Failure Check and Recovery

The transmit clock failure check circuit (see Figure 23-191) works off the internal MCASP system clock and the external high-frequency serial clock (abemcasp_ahclkx). It continually counts the number of system clocks for every 32 high-rate serial clock (abemcasp_ahclkx) periods, and stores the count in XCNT of the transmit clock check control register (MCASP_TXCLKCHK) every 32 high-rate serial clock cycles.

The logic compares the count against a user-defined minimum allowable boundary (XMIN), and automatically flags an interrupt (XCKFAIL in MCASP_TXSTAT) when an out-of-range condition occurs. An out-of-range minimum condition occurs when the count is less than XMIN. The logic continually compares the current count (from the running system clock counter) to the maximum allowable boundary (XMAX). This is so that if the external clock completely stops, the counter value is not copied to XCNT. An out-of-range maximum condition occurs when the count is greater than XMAX. The XMIN and XMAX fields are 8-bit unsigned values, and the comparison is performed using unsigned arithmetic.

An out-of-range count may indicate that an unstable clock was detected or that the audio source has changed and a new sample rate is being used.

For the transmit clock failure check circuit to operate correctly, the high-frequency serial clock divider must be taken out of reset.

If a clock failure is detected, the transmit clock failure flag (XCKFAIL) in MCASP_TXSTAT is set. This causes an interrupt if the transmit clock failure interrupt enable bit (XCKFAIL) in MCASP_EVTCTLX is set.

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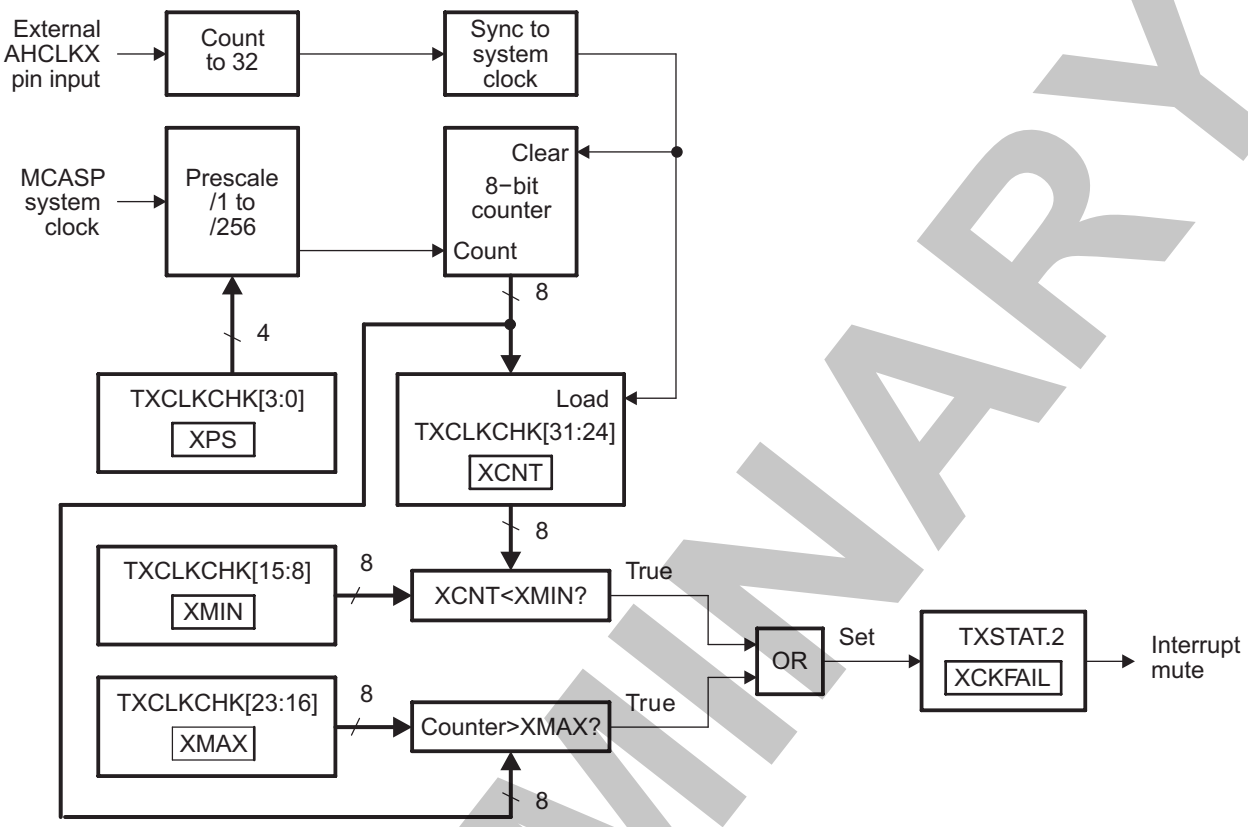
Figure 23-191. Transmit Clock Failure Detection Circuit Block Diagram



23.8.4.15.6.3 Receive Clock Failure Check and Recovery

The receive clock failure check circuit (see Figure 23-192) works off both the internal MCASP system clock and the external high-frequency serial clock (AHCLKR) coming from the device abemcasp_ahclkr input. It continually counts the number of system clocks for every 32 high rate serial clock (AHCLKR) periods, and stores the count in RCNT of the receive clock check control register (MCASP_RCLKCHK) every 32 high rate serial clock cycles.

The logic compares the count against a user-defined minimum allowable boundary (RMIN) and automatically flags an event (RCKFAIL in MCASP_RXSTAT) when an out-of-range condition occurs. An out-of-range minimum condition occurs when the count is smaller than RMIN. The logic continually compares the current count (from the running system clock counter) against the maximum allowable boundary (RMAX). This is in case the external clock completely stops, so that the counter value is not copied to RCNT. An out-of-range maximum condition occurs when the count is greater than RMAX. Note that the RMIN and RMAX fields are 8-bit unsigned values, and the comparison is performed using unsigned arithmetic.

An out-of-range count may indicate either that an unstable clock was detected or that the audio source has changed and a new sample rate is being used.

In order for the receive clock failure check circuit to operate correctly, the high-frequency serial clock divider must be taken out of reset regardless if AHCLKR signal is internally generated or externally sourced.

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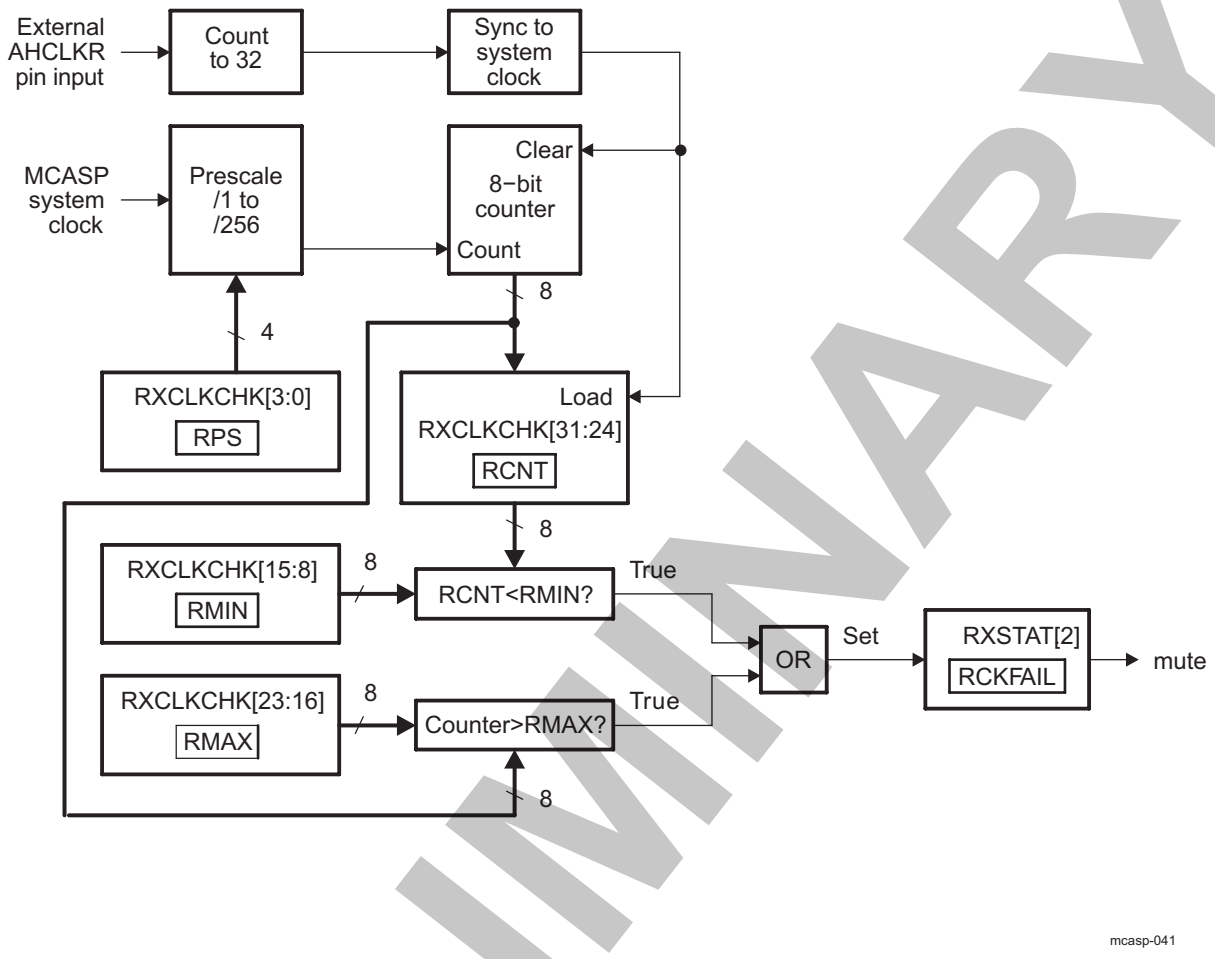
Figure 23-192. Receive Clock Failure Detection Circuit Block Diagram



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23.8.5 MCASP Low-Level Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the MCASP module.

23.8.5.1 Global Initialization

23.8.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the MCASP module is used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MCASP (for more information, see Section 23.8.3, *MCASP Integration*, and Section 23.8.2, *MCASP Environment*).

Table 23-575, describes the global initialization of surrounding modules.

Table 23-575. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module functional and interface clocks must be enabled. (See Section 3.6, *Clock Management Functional Description*, in Chapter 3, *Power, Reset, and Clock Management*.)
Control module	Module-specific pad muxing and other pad configurations must be set in the control module. (See Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*).
(Optional) INTC_MPU or INTC_DSP	Interrupt controllers (INTC_MPU and INTC_DSP) configuration must be done to enable the interrupts from the MCASP. (For more details on MPU interrupt controller requests, see Section 17.3.2, *Interrupt Requests to INTC_MPU* in Chapter 17, *Interrupt Controllers*. For more information on the DSP interrupt controller requests, see Section 5.3.2.6, *DSP INTC*, in Chapter 5, *DSP Subsystem*).
(Optional) DMA_SYSTEM or DMA_DSP	DMA configuration must be done to enable the MCASP DMA data channel requests. For more information on DMA_SYSTEM and DMA_DSP configuration, see Section 16.5, *DMA_SYSTEM Basic Programming Model,* in Chapter 16, *System DMA* and Section 5.2, *DSP Subsystem Integration*, in Chapter 5, *DSP Subsystem* .
(Optional) L4_ABE and L3_MAIN Interconnects	For more information about the interconnect configuration, see Section 14.2.1, *L3_MAIN Interconnect Overview* in Chapter 14, *Interconnect*.

NOTE: The INTC_MPU / INTC_DSP and the DMA_SYSTEM / DMA_DSP configurations are required when the interrupt and DMA-based communication modes are used.

23.8.5.1.2 MCASP Global Initialization

23.8.5.1.2.1 Main Sequence – MCASP Global Initialization for DIT-Transmission

The procedure in Table 23-576 initializes the MCASP serializers (0-3) transmitters to operate in DIT-mode (S/PDIF-transmission protocol) after a power-on reset (POR).

CAUTION

Before performing MCASP global initialization, If external clocks AHCLKR and/or ACLKR are used, they must be running already for proper synchronization of the MCASP_GBLCTL register.

Table 23-576. MCASP Transmitters Global Initialization for DIT-Mode Operation

Step	Register/Bit Field/Programming Model	Value
1. Apply software reset to different MCASP components.	MCASP_GBLCTL[12:8]	0x00

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Table 23-576. MCASP Transmitters Global Initialization for DIT-Mode Operation (continued)

Step	Register/Bit Field/Programming Model	Value
2. Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	MCASP_GBLCTL[12:8]	=0x00
3. Configure the local power management.	MCASP_SYSCONFIG[1:0] IDLE_MODE	0x1
4. Configure the transmit format unit.	See Section 23.8.5.1.2.1.1.	
5. Configure the transmit frame sync generator.	See Section 23.8.5.1.2.1.2.	
6. Configure the transmit clock generator.	See Section 23.8.5.1.2.1.3.	
7. Configure the TDM sequencer—set all slots active.	MCASP_TXTDM[31:0] XTDMS	0xFFFF FFFF
8. Configure the desired n-th serializer (n=0 to 3) for transmit mode operation. (1)	MCASP_XRSRCTLn [1:0] SRMOD, where n=0 to 3	0x1
9. Configure the MCASP pins functionality.	See Section 23.8.5.1.2.1.4.	
10. Configure the MCASP mute input / output conditions.	See Table 23-581.	
11. Enable the MCASP DIT - transmission mode.	MCASP_TXDITCTL[0] DITEN	0x1 (2)
12. Configure DIT-specific subframe fields.	See Table 23-582.	
13. Release from reset state the divider that outputs the AHCLKX clock. (3)	MCASP_GBLCTL[9] XHCLKRST	0x1
14. Poll the bit to ensure that it is successfully latched in the register.	MCASP_GBLCTL[9] XHCLKRST	=0x1
15. Release from reset state the divider that outputs the ACLKX clock. (3)	MCASP_GBLCTL[8] XCLKRST	0x1
16. Poll the bit to ensure that it is successfully latched in the register.	MCASP_GBLCTL[8] XCLKRST	=0x1

(1) For an unused serializer n (where n=0 to 3), write MCASP_XRSRCTLn [1:0] SRMOD=0x0 to disable it.
(2) This globally configures all active transmitters to operate in DIT-mode.
(3) During reset state the local MCASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the MCASP_AHCLKXCTL and MCASP_ACLKXCT registers are ignored; hence, the transmission clock does not stop during the reset state of the dividers.

23.8.5.1.2.1.1 Subsequence – Transmit Format Unit Configuration for DIT-Transmission

The procedure in Table 23-577 configures the transmit frame format unit of the MCASP module for a DIT-transmission.

NOTE:

- The first transmit data bit always has a 0-bit delay.
- The bitstream is always transmitted in least-significant-bit (LSB)-first order.
- Pad value for extra bits in a certain slot is always 0.

Table 23-577. Transmit Format Unit Configuration for DIT-Transmission

Step	Register/Bit Field/Programming Model	Value
Configure the slot size to 32 bits.	MCASP_TXFMT[7:4] XSSZ	0xF
IF: the MPU, DSP or DMA data to transmit is left-aligned	Software test condition	
Set data mask in the range 0xFFFF FF00 – 0xFFFF 0000.	MCASP_TXMASK[31:0] XMASK	0x- (1)
Rotate data right by a multiple-of-4- bit positions.	MCASP_TXFMT[2:0] XROT	0x- (1)
ELSE		
Set data mask in the range 0x00FF FFFF– 0x0000 FFFF.	MCASP_TXMASK[31:0] XMASK	0x- (1)
Rotate data right by 0-bit positions.	MCASP_TXFMT[2:0] XROT	0x0

(1) Refer to Section 23.8.4.4.1, *Transmit Fromat Unit* and Section 23.8.4.4.1.2, *DIT-Mode Transmission Data Alignment Settings.*

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Table 23-577. Transmit Format Unit Configuration for DIT-Transmission (continued)

Step	Register/Bit Field/Programming Model	Value
ENDIF		
Select to write data to active serializers transmit buffers using peripheral (CFG) or DATA port	MCASP_TXFMT[3] XBUSEL	0x-

23.8.5.1.2.1.2 Subsequence – Transmit Frame Synchronization Generator Configuration for DIT-Transmission

The procedure in Table 23-578 configures the transmit frame synchronization generator of the MCASP module.

NOTE: The frame synchronization signal is always rising-edge active and always has a single-bit width.

Table 23-578. Transmit Frame-Synchronization Generator Configuration for DIT-Transmission

Step	Register/Bit Field/Programming Model	Value
Select 384-slot size block.	MCASP_TXFMCTL[15:7] XMOD	0x180
Select internally-generated transmit frame sync.	MCASP_TXFMCTL[1] FSXM	0x1

23.8.5.1.2.1.3 Subsequence – Transmit Clock Generator Configuration for DIT-Transmission

NOTE: By default, the ACLKX and AHCLKX clocks are generated only from the MCASP internal clock source.

The procedure in Table 23-579 configures the transmit clock generator of the MCASP module.

Table 23-579. Transmit Clock Generator Configuration in DIT-Mode

Step	Register/Bit Field/Programming Model	Value
Set the divisor for the internally generated high frequency clock– AHCLKX.	MCASP_AHCLKXCTL[11:0] HCLKXDIV	0x-
Set he divisor for the internally generated transmission clock– ACLKX.	MCASP_ACLKXCTL[4:0] CLKXDIV	0x-
Configure the transmit clock failure detect logic.	See Section 23.8.4.15.6.1, *Clock Failure Check Startup*.	

23.8.5.1.2.1.4 Subsequence—MCASP Pins Functional Configuration

The procedure in Table 23-580 configures the MCASP pins for MCASP functionality.

Table 23-580. MCASP Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have MCASP functionality.	MCASP_PFUNC[31:0]	0x0
Configure the MCASP pins as outputs: AFSX (device level: abemcasp_afsx) AHCLKX (device level: abemcasp_ahclkx) ACLKX (device level: abemcasp_aclkx) AMUTE (device level: abemcasp_amuteout) Desired i-th MCASP data pin AXRi (i=0 to 3) (device level: abemcasp_axr - abemcasp_axr3) is configured as an output for DIT-transmission.	MCASP_PDIR[28] AFSX; MCASP_PDIR[27] AHCLKX; MCASP_PDIR[26] ACLKX; MCASP_PDIR[25] AMUTE; MCASP_PDIR [i] AXRi , where i=0 to 3	0x1 0x1 0x1 0x1 0x1

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23.8.5.1.2.1.5 Subsequence – MCASP Mute Input/Output Trigger Condition Settings

The procedure in Table 23-581 configures the behavior of the mute associated I/Os and different trigger conditions for the MCASP mute output functionality.

Table 23-581. MCASP Mute Input/Output Trigger Condition Settings

Step	Register/Bit Field/Programming Model	Value
Optional: Select to drive AMUTE active enable bit on transmit DATA port error.	MCASP_AMUTE[12] XDMAERR	0x1
Optional: Select to drive AMUTE active enable bit on transmit clock failure.	MCASP_AMUTE[10] XCKFAIL	0x1
Optional: Select to drive AMUTE active enable bit on transmit frame synchronization error.	MCASP_AMUTE[8] XSYNCERR	0x1
Optional: Select to drive AMUTE active enable bit on transmit underrun error.	MCASP_AMUTE[6] XUNDRN	0x1
Optional: Enable sensitivity of the abemcasp_amuteout output to abemcasp_amutein error source.	MCASP_AMUTE[3] INEN	0x1
Optional: Select the abemcasp_amutein input polarity.	MCASP_AMUTE[2] INPOL	0x1
Optional: Configure the behavior of the abemcasp_amuteout output.	MCASP_AMUTE[1:0] MUTEN	0x1

23.8.5.1.2.1.6 Subsequence – DIT-specific Subframe Fields Configuration

The procedure in Table 23-582 configures the DIT-specific subframe fields as part of the S/PDIF format data.

Table 23-582. DIT-Specific Subframe Fields Configuration

Step	Register/Bit Field/Programming Model	Value
Configure the valid bit value for odd time slots.	MCASP_TXDITCTL[3] VB	0x-
Configure the valid bit value for even time slots.	MCASP_TXDITCTL[2] VA	0x-
Configure the user data bit for each subframe A and B in a 384-slot S/PDIF block.	MCASP_DITUDRAi[31:0] DITUDRAi, where i = 0 to 5 MCASP_DITUDRBi[31:0] DITUDRBi, where i= 0 to 5	0x- 0x-
Configure the channel status bit for each subframe A and B in a 384-slot S/PDIF block.	MCASP_DITCSRAi[31:0] , where i = 0 to 5 MCASP_DITCSRBi[31:0] , where i = 0 to 5	0x- 0x-

23.8.5.1.2.2 Main Sequence – MCASP Global Initialization for TDM-Reception

The procedure in Table 23-583 initializes a MCASP serializer n (where n=0 to 3) receiver(s) to operate in TDM-mode (the only mode supported by MCASP receivers) after a power-on reset (POR). This is used for I2S (2-slot TDM) and other TDM-based audio protocols reception.

CAUTION

Before performing MCASP global initialization, If external clocks AHCLKR and/or ACLKR are used, they must be running already for proper synchronization of the MCASP_GBLCTL register.

NOTE: The MCASP receivers support only TDM-frames (including 384-TDM frames) reception. DIT-frames reception (i.e. S/PDIF stream) can be implemented indirectly via an external DIR-chip converter with DIT-input and TDM (I2S)-compatible output connected to device MCASP receiver input (TDM-only compatible).

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Table 23-583. MCASP Receivers Global Initialization for TDM-Mode Operation

Step	Register/Bit Field/Programming Model	Value
1. Apply software reset to different MCASP receive components.	MCASP_GBLCTL[4:0]	0x00
2. Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	MCASP_GBLCTL[4:0]	=0x00
3. Configure the local power management.	MCASP_SYSCONFIG[1:0] IDLE_MODE	0x1
4. Configure the receive format unit.	See Section 23.8.5.1.2.2.1.	
5. Configure the receive frame sync generator.	See Section 23.8.5.1.2.2.2.	
6. Configure the receive clock generator.	See Section 23.8.5.1.2.2.3.	
7. Program all bits -RTDMSk (where k=0 to 31) according to the time slot characteristics desired (positions of active versus inactive slots within a frame).	MCASP_RXTDM [k] RTDMSk , where k=0 to 31	0x-
8. Configure the desired n-th serializer (n=0 to 3) for receive mode operation. (1)	MCASP_XRSRCTLn [1:0] SRMOD , where n = 0 to 3	0x2
9. Configure the MCASP pins functionality.	See Section 23.8.5.1.2.2.4.	
10. Configure the MCASP mute input/output conditions.	See Table 23-588.	
11. Optional : Configure a MCASP Rx channel for a loopback operation (TDM mode only) in MCASP_LBCTL [31:0].	See Section 23.8.4.14.1, *Loopback Mode Configurations*.	0x- (2)
12. Release from reset state the divider that outputs the AHCLKR clock. (3) See also (4).	MCASP_GBLCTL[1] RHCLKRST	0x1
13. Poll the bit to ensure that it is successfully latched in the register. See also (4).	MCASP_GBLCTL[1] RHCLKRST	=0x1
14. Release from reset state the divider that outputs the ACLKR clock. (3) See also (5).	MCASP_GBLCTL[0] RCLKRST	0x1
15. Poll the bit to ensure that it is successfully latched in the register. See also (5).	MCASP_GBLCTL[0] RCLKRST	=0x1

(1) For an unused serializer n (where n=0 to 3), write MCASP_XRSRCTLn [1:0] SRMOD=0x0 to disable it.

(2) In this case the receiver clock and frame sync are derived from the MCASP transmitter logic, so MCASP_ACLKXCTL[6] ASYNC must be set to 0b0. Neither MCASP internal receiver clock and frame sync generators, nor external clock and frame sync source are used.

(3) During reset state the local MCASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the MCASP_AHCLKRCTL and MCASP_ACLKRCTL registers are ignored; hence, the reception clock does not stop during the reset state of the dividers.

(4) This step is necessary even if external high-frequency serial clocks are used.

(5) This step can be skipped if external serial clocks are used and they are running.

23.8.5.1.2.2.1 Subsequence – Receive Format Unit Configuration in TDM Mode

The procedure in Table 23-584 configures the receive frame format unit of the MCASP module for TDM slots reception.

Table 23-584. Receive Format Unit Configuration for TDM-Reception

Step	Register/Bit Field/Programming Model	Value
Configure the desired TDM-slot size	MCASP_RXFMT[7:4] RSSZ	0x- (1)
Set data mask out value (0x0000 0000 - 0xFFFF FFFF).	MCASP_RXMASK[31:0] RMASK	0x- (2)
Select a padding value for masked-out bits.	MCASP_RXFMT[14:13] RPAD	0x-

(1) Refer to Section 23.8.4.4.2, *Receive Format Unit*, regarding options for received TDM-slot sizes.

(2) For more details on Rx masking value, refer to Section 23.8.4.4.2.1, *TDM - Mode Reception Data Alignment Settings*

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Table 23-584. Receive Format Unit Configuration for TDM-Reception (continued)

Step	Register/Bit Field/Programming Model	Value
Specify position (0x0-0x1F) of the bit in corresponding register MCASP_RXBUFn which value to be used as a pad value in case MCASP_RXFMT[14:13] RPAD=0x2.	MCASP_RXFMT[12:8] RPBIT	0x-
Rotate data right by a multiple of 4- bit positions.	MCASP_RXFMT[2:0] RROT	0x- (3)
Received stream bit order (LSB- or MSB-first). **Must be set to 0x1 for an I2S stream reception (MSB-first).**	MCASP_RXFMT[15] RRVRS	0x- (3)
Specify a delay between frame sync and first bit of data in number of bits. **Must be set to 0x1 for an I2S stream reception.**	MCASP_RXFMT[17:16] RDATDLY	0x-
Select to read data from active serializers receive buffers using peripheral (CFG) or DATA port	MCASP_RXFMT[3] RBUSEL	0x-

(3) For more details on rotation and received TDM stream bit order, refer to Section 23.8.4.4.2.1, *TDM - Mode Reception Data Alignment Settings* and Table 23-570, *MCASP RFU Settings*.

23.8.5.1.2.2.2 Subsequence – Receive Frame Synchronization Generator Configuration in TDM Mode

The procedure in Table 23-585 configures the transmit frame synchronization generator of the MCASP module.

NOTE: The same bit - MCASP_ACLKXCTL[6] ASYNC which is used to determine if MCASP receivers and transmitters work synchronously on the same clock, is also used to define if receiver frame sync is derived from the transmit frame sync generator, or generated independently in the receiver (either inernally or externally sourced). Hence, the settings in below table Table 23-585 have no effect, if MCASP_ACLKXCTL[6] ASYNC = 0.

Table 23-585. Receive Frame-Synchronization Generator Configuration for TDM-Reception

Step	Register/Bit Field/Programming Model	Value
Select number of TDM slots per frame. Must be set to 0x2 , in case of an I2S-reception. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_RXFMCTL[15:7] RMOD	0x- (1)
Choose the receive frame sync width -single bit / single word. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_RXFMCTL[4] FRWID	0x-
Select start of received frame sync polarity - rising / falling edge. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_RXFMCTL[0] FSRP	0x-
IFreceive frame sync - FS is internally generated	Software test condition	
Select internally- generated receive frame sync. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_RXFMCTL[1] FSRM	0b1
If MCASP receiver is required to output internally generated frame, AFSR pin (device level: abemcasp_afsr) must be set as an output **in step 9 of the sequence documented in the** Table 23-583. This must NOT be done in current step because the frame control register - MCASP_TXFMCTL must be appropriately configured prior to AFSR pin outputting a frame to an external device.	MCASP_PDIR[31] AFSR	0b1
ELSE		

(1) Must be set to 0x180 in case of 384-TDM slot frame reception from a DIR component I2S-output. For more details on TDM-frame settings, refer to Section 23.8.4.9.1 .

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Table 23-585. Receive Frame-Synchronization Generator Configuration for TDM-Reception (continued)

Step	Register/Bit Field/Programming Model	Value
Select externally- generated receive frame sync. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_RXFMCTL[1] FSRM	0b0
Setup the AFSR pin as input (device level: abemcasp_afsr)	MCASP_PDIR[31] AFSR	0b0
ENDIF		
To generate MCASP receive frame sync in receiver logic , select an asynchronous frame sync.	MCASP_ACLKXCTL[6] ASYNC	0b1

23.8.5.1.2.2.3 Subsequence – Receive Clock Generator Configuration

The procedure in Table 23-586 configures the receive clock generator of the MCASP module.

NOTE: The settings in below table Table 23-586 have no effect, if MCASP_ACLKXCTL[6] ASYNC = 0 (i.e. receive clock is sourced from the inverted version of the transmit clock). For example, such is the case when MCASP loopback mode is used.

Table 23-586. Receive Clock Generator Configuration

Step	Register/Bit Field/Programming Model	Value
To use the MCASP receive clock generator or an external clock, select an asynchronous receiver clock schema (ASYNC=1). Otherwise an inverted version of transmit clock XCLK is used (receiver synchronized with transmitter).	MCASP_ACLKXCTL[6] ASYNC	0b1
IFreceive clock - RCLK is internally generated	Software test condition	
IF high-speed receive clock - AHCLKR is internally generated based on AUXCLK	Software test condition	
Select an internally-generated high-frequency clock.	MCASP_AHCLKRCTL[15] HCLKRM	0b1
Select the internal high-speed clock source polarity : non-inverted or inverted.	MCASP_AHCLKRCTL[14] HCLKRP	0x-
Set the divisor for the internally generated high-frequency clock – AHCLKR in range (1 - 4096).	MCASP_AHCLKRCTL[11:0] HCLKRDIV	0x-
Optional : If MCASP receiver is required to output internally generated high-frequency clock, AHCLKR pin (device level: abemcasp_ahclkr) must be set as an output **in step 9 of the sequence documented in the** Table 23-583. This must NOT be done in current step because the clock control register - MCASP_AHCLKRCTL must be appropriately configured prior to AHCLKR pin outputting a high-speed clock to an external device.	MCASP_PDIR[30] AHCLKR	0b1
ELSE		
Select an externally-generated high frequency clock (HCLKRDIV divider can not be used).	MCASP_AHCLKRCTL[15] HCLKRM	0b0
Select the external high-speed receive clock polarity : non-inverted or inverted.	MCASP_AHCLKRCTL[14] HCLKRP	0x-
Setup an input directon for the AHCLKR pin (device level abemcasp_ahclkr)	MCASP_PDIR[30] AHCLKR	0b0
ENDIF		
Select an internally-generated receive clock.	MCASP_ACLKRCTL[5] CLKRM	0b1
Receiver samples on rising / falling edge. **Select Rx sampling on the rising edge if transmitter shifts out on falling edge, and vice versa.**	MCASP_ACLKRCTL[7] CLKRP	0x-

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Table 23-586. Receive Clock Generator Configuration (continued)

Step	Register/Bit Field/Programming Model	Value
Set the divisor for the internally generated receive clock– ACLKR in range (1 - 32).	MCASP_ACLKRCTL[4:0] CLKRDIV	0x-
Optional: If MCASP receiver is required to output internally generated clock, ACLKR pin (device level: abemcasp_aclkr) must be set as an output **in step 9 of the sequence documented in the** Table 23-583. This must NOT be done in current step because the clock control register - MCASP_ACLKRCTL must be appropriately configured prior to ACLKR pin outputting a receive clock to an external device.	MCASP_PDIR[29] ACLKR	0b1
ELSE		
Select an externally-generated receive clock. Note that in this case the AHCLKR signal path and the CLKRDIV divider are NOT used.	MCASP_ACLKRCTL[5] CLKRM	0b0
Receiver samples on rising / falling edge. **Select Rx sampling on the rising edge if transmitter shifts out on falling edge, and vice versa.**	MCASP_ACLKRCTL[7] CLKRP	0x-
Setup an input directon for the ACLKR pin (device level abemcasp_aclkr)	MCASP_PDIR[29] ACLKR	0b0
ENDIF		
Configure the transmit clock failure detect logic.	See Section 23.8.4.15.6.1, *Clock Failure Check Startup*.	

23.8.5.1.2.2.4 Subsequence—MCASP Receiver Pins Functional Configuration

The procedure in Table 23-587 configures the MCASP pins for MCASP functionality.

Table 23-587. MCASP Receiver Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have MCASP functionality.	MCASP_PFUNC[31:0]	0x0
Configure the MCASP pins direction : AFSR (device level: abemcasp_afsr) AHCLKR (device level: abemcasp_ahclkr) ACLKR(device level: abemcasp_aclkr) Desired i-th MCASP data pin AXRi (i=0 to 3) (device level: abemcasp_axr - abemcasp_axr3) is configured as an input for receiving.	MCASP_PDIR[31] AFSR; MCASP_PDIR[30] AHCLKR; MCASP_PDIR[29] ACLKR; MCASP_PDIR[i] AXRi;	 0x-(1) 0x-(2) 0x- (2) 0x0

(1) See Table 23-585.

(2) For more details on MCASP clock configurations , refer to Table 23-586.

23.8.5.1.2.2.5 Subsequence – MCASP Receive Mute Input/Output Trigger Condition Settings

The procedure in Table 23-588 configures the behavior of the mute associated I/Os and different receive trigger conditions for the MCASP mute output functionality.

Table 23-588. MCASP Receive Mute Input/Output Trigger Condition Settings

Step	Register/Bit Field/Programming Model	Value
Optional: Select to drive AMUTE active enable bit on receive DATA port error.	MCASP_AMUTE[11] RDMAERR	0x1
Optional: Select to drive AMUTE active enable bit on receive clock failure.	MCASP_AMUTE[9] RCKFAIL	0x1
Optional: Select to drive AMUTE active enable bit on receive frame synchronization error.	MCASP_AMUTE[7] RSYNCERR	0x1

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Table 23-588. MCASP Receive Mute Input/Output Trigger Condition Settings (continued)

Step	Register/Bit Field/Programming Model	Value
Optional: Select to drive AMUTE active enable bit on receive overrun error.	MCASP_AMUTE[5] ROVRN	0x1
Optional: Enable sensitivity of the abemcasp_amuteout output to abemcasp_amutein error source.	MCASP_AMUTE[3] INEN	0x1
Optional: Select the abemcasp_amutein input polarity.	MCASP_AMUTE[2] INPOL	0x1
Optional: Configure the behavior of the abemcasp_amuteout output.	MCASP_AMUTE[1:0] MUTEN	0x1

23.8.5.1.2.3 Main Sequence – MCASP Global Initialization for TDM -Transmission

The procedure in Table 23-589 initializes a MCASP serializer n (where n=0 to 3) transmitter(s) to operate in TDM-mode after a power-on reset (POR). This is used for I2S (2-slot TDM) and other TDM-based audio protocols transmission.

CAUTION

Before performing MCASP global initialization, If external clocks AHCLKR and/or ACLKR are used, they must be running already for proper synchronization of the MCASP_GBLCTL register.

Table 23-589. MCASP Transmitters Global Initialization for TDM-Mode Operation

Step	Register/Bit Field/Programming Model	Value
1. Apply software reset to different MCASP transmit components.	MCASP_GBLCTL[12:8]	0x00
2. Poll the bits to ensure the active reset value (0x00) is successfully latched into the register.	MCASP_GBLCTL[12:8]	=0x00
3. Configure the local power management.	MCASP_SYSCONFIG[1:0] IDLE_MODE	0x1
4. Configure the transmit format unit.	See Section 23.8.5.1.2.3.1.	
5. Configure the transmit frame sync generator.	See Section 23.8.5.1.2.3.2.	
6. Configure the transmit clock generator.	See Section 23.8.5.1.2.3.3.	
7. Program all bits - XTDMSk , where k=0 to 31, according to the time slot characteristics desired (positions of active versus inactive slots within a frame).	MCASP_TXTDM [k] XTDMSk, where k=0 to 31(1)	0x-
8. Configure the desired n-th serializer (n=0 to 3) for transmit mode operation. (2)	MCASP_XRSRCTLn[1:0] SRMOD;	0x1
9. Setup all active transmitters to operate in TDM mode.	MCASP_TXDITCTL[0] DITEN	0x0(3)
10. Configure the MCASP pins functionality.	See Section 23.8.5.1.2.3.4.	
11. Configure the MCASP mute input/output conditions.	See Table 23-594.	
12. Optional : Configure a MCASP Tx channel for loopback operation (TDM mode only) in MCASP_LBCTL [31:0].	See Section 23.8.4.14.1, *Loopback Mode Configurations*.	0x-

(1) Appropriately program in bitfield MCASP_XRSRCTLn [3:2] DISMOD, the desired level (high-impedance state, 0, or 1) at AXRn (n=0 to 3) output, during time of inactive slots. Note, that this setting soes NOT apply when all slots are programmed to be active within a frame (in particular DIT-mode).

(2) For an unused serializer n (where n=0 to 3), write MCASP_XRSRCTLn [1:0] SRMOD=0x0 to disable it.

(3) All active transmit channels operate either in TDM mode or in DIT mode depending on DITEN value. There is no option to choose Tx Mode between DIT and TDM separately per serializer transmitter.

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Table 23-589. MCASP Transmitters Global Initialization for TDM-Mode Operation (continued)

Step	Register/Bit Field/Programming Model	Value
13. Release from reset state the divider that outputs the AHCLKR clock. See (4)	MCASP_GBLCTL[9] XHCLKRST	0x1
14. Poll the bit to ensure that it is successfully latched in the register.	MCASP_GBLCTL[9] XHCLKRST	=0x1
15. Release from reset state the divider that outputs the ACLKR clock. See (4)	MCASP_GBLCTL[8] XCLKRST	0x1
16. Poll the bit to ensure that it is successfully latched in the register.	MCASP_GBLCTL[8] XCLKRST	=0x1

(4) During reset state the local MCASP internal clock dividers maintain a 1:1 ratio at their outputs. The values stored in the MCASP_AHCLKX and MCASP_ ACLKX registers are ignored; hence, the transmission clock does not stop during the reset state of the dividers.

23.8.5.1.2.3.1 Subsequence – Transmit Format Unit Configuration in TDM Mode

The procedure in Table 23-590 configures the transmit frame format unit of the MCASP module for TDM slots transmission.

Table 23-590. Transmit Format Unit Configuration for TDM-Transmission

Step	Register/Bit Field/Programming Model	Value
Configure the desired TDM-slot size	MCASP_TXFMT[7:4] XSSZ	0x- (1)
Set data mask out value (0x0000 0000 - 0xFFFF FFFF).	MCASP_TXMASK[31:0] XMASK	0x- (2)
Select a padding value for masked-out bits.	MCASP_TXFMT[14:13] XPAD	0x-
Specify position (0x0-0x1F) of the bit in corresponding register MCASP_TXBUFn which value to be used as a pad value in case MCASP_TXFMT[14:13] XPAD=0x2.	MCASP_TXFMT[12:8] XPBIT	0x-
Rotate data right by a multiple of 4- bit positions.	MCASP_TXFMT[2:0] XROT	0x- (3)
transmitted stream bit order (LSB- or MSB-first). **Must be set to 0x1 for an I2S stream transmission (MSB-first).**	MCASP_TXFMT[15] XRVRS	0x- (3)
Specify a delay between frame sync and first bit of data in number of bits. **Must be set to 0x1 for an I2S stream transmission.**	MCASP_TXFMT[17:16] XDATDLY	0x-
Select to write data to active serializers transmit buffers using peripheral (CFG) or DATA port	MCASP_TXFMT[3] XBUSEL	0x-

(1) Refer to Section 23.8.4.4.1, *Transmit Format Unit* , regarding options for transmitted TDM-slot sizes.
(2) For more details on Tx masking value, refer to Section 23.8.4.4.1.1, *TDM - Mode Transmission Data Alignment Settings*
(3) For more details on rotation and transmitd TDM stream bit order, refer to Section 23.8.4.4.1.1, *TDM - Mode Transmission Data Alignment Settings* and Table 23-568, *MCASP TFU TDM Mode Settings*.

23.8.5.1.2.3.2 Subsequence – Transmit Frame Synchronization Generator Configuration in TDM Mode

The procedure in Table 23-591 configures the transmit frame synchronization generator of the MCASP module.

Table 23-591. Transmit Frame-Synchronization Generator Configuration for TDM-Transmission

Step	Register/Bit Field/Programming Model	Value
Select number of TDM slots per frame (2 - 32). Must be set to 0x2 , in case of an I2S-transmission. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_TXFMCTL[15:7] XMOD	0x-
Choose the transmit frame sync width -single bit / single word. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_TXFMCTL[4] FXWID	0x-

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Table 23-591. Transmit Frame-Synchronization Generator Configuration for TDM-Transmission (continued)

Step	Register/Bit Field/Programming Model	Value
Select start of transmit frame sync polarity - rising / falling edge. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_TXFMCTL[0] FSXP	0x-
IFtransmit frame sync - FS is internally generated	Software test condition	
Select internally- generated transmit frame sync. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_TXFMCTL[1] FSXM	0b1
If MCASP transmitter is required to output internally generated frame, AFSX pin (device level: abemcasp_afsx) must be set as an output **in step 10 of the sequence documented in the** Table 23-589. This must NOT be done in current step because the frame control register - MCASP_TXFMCTL must be appropriately configured prior to AFSX pin outputting a frame sync to an external device.	MCASP_PDIR[28] AFSX	0b1
ELSE		
Select externally- generated transmit frame sync. For more details on frame-sync generator, refer to Section 23.8.4.2.3.	MCASP_TXFMCTL[1] FSXM	0b0
Setup the AFSX pin as input (device level: abemcasp_afsx)	MCASP_PDIR[28] AFSX	0b0

23.8.5.1.2.3.3 Subsequence – Transmit Clock Generator Configuration for TDM Cases

The procedure in Table 23-592 configures the transmit clock generator of the MCASP module.

Table 23-592. Transmit Clock Generator Configuration for TDM Cases

Step	Register/Bit Field/Programming Model	Value
IFtransmit clock - XCLK is internally generated	Software test condition	
IF high-speed transmit clock - AHCLKX is internally generated based on AUXCLK	Software test condition	
Select an internally-generated high-frequency clock.	MCASP_AHCLKXCTL[15] HCLKXM	0b1
Select the high-frequency clock source polarity : non-inverted or inverted.	MCASP_AHCLKXCTL[14] HCLKXP	0x-
Set the divisor for the internally generated high-frequency clock – AHCLKX in range (1 - 4096).	MCASP_AHCLKXCTL[11:0] HCLKXDIV	0x-
Optional : If MCASP transmitter is required to output internally generated high-frequency clock, AHCLKX pin (device level: abemcasp_ahclkx) must be set as an output **in step 10 of the sequence documented in the** Table 23-589. This must NOT be done in current step because the clock control register - MCASP_AHCLKXCTL must be appropriately configured prior to AHCLKX pin outputting a high-speed clock to an external device.	MCASP_PDIR[27] AHCLKX	0b1
ELSE		
Select an externally-generated high frequency clock (HCLKXDIV divider can not be used).	MCASP_AHCLKXCTL[15] HCLKXM	0b0
Select the high-speed transmit clock source polarity : non-inverted or inverted.	MCASP_AHCLKXCTL[14] HCLKXP	0x-
Setup an input directon for the AHCLKX pin (device level abemcasp_ahclkx)	MCASP_PDIR[27] AHCLKX	0b0
ENDIF		

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Table 23-592. Transmit Clock Generator Configuration for TDM Cases (continued)

Step	Register/Bit Field/Programming Model	Value
Select an internally-generated transmit clock.	MCASP_ACLKXCTL[5] CLKXM	0b1
Transmitter samples on rising / falling edge. **Select Tx shifting out data on the rising edge if receiver samples on falling edge, and vice versa.**	MCASP_ACLKXCTL[7] CLKXP	0x-
Set the divisor for the internally generated transmit clock– ACLKX in range (1 - 32).	MCASP_ACLKXCTL[4:0] CLKXDIV	0x-
Optional: If MCASP transmitter is required to output internally generated clock, ACLKX pin (device level: abemcasp_aclkx) must be set as an output **in step 10 of the sequence documented in the** Table 23-589. This must NOT be done in current step because the clock control register - MCASP_ACLKXCTL must be appropriately configured prior to ACLKX pin outputting a transmit clock to an external device.	MCASP_PDIR[26] ACLKX	0b1
ELSE		
Select an externally-generated transmit clock. Note that in this case the AHCLKX signal path and the CLKXDIV divider are NOT used.	MCASP_ACLKXCTL[5] CLKXM	0b0
Transmitter samples on rising / falling edge. **Select Tx shifting out data on the rising edge if receiver samples on falling edge, and vice versa.**	MCASP_ACLKXCTL[7] CLKXP	0x-
Setup an input directon for the ACLKX pin (device level abemcasp_aclkr)	MCASP_PDIR[26] ACLKX	0b0
ENDIF		
Configure the transmit clock failure detect logic.	See Section 23.8.4.15.6.1, *Clock Failure Check Startup*.	

23.8.5.1.2.3.4 Subsequence—MCASP Transmit Pins Functional Configuration

The procedure in Table 23-593 configures the MCASP pins for MCASP functionality.

Table 23-593. MCASP Transmit Pins Functional Configuration

Step	Register/Bit Field/Programming Model	Value
Configure module different pins to have MCASP functionality.	MCASP_PFUNC[31:0]	0x0
Configure the MCASP pins direction : AFSX (device level: abemcasp_afsr) AHCLKX (device level: abemcasp_ahclkr) ACLKX (device level: abemcasp_aclkr) Desired i-th MCASP data pin AXRi (i=0 to 3) (device level: abemcasp_axr - abemcasp_axr3) is configured as an ouput for transmission.	MCASP_PDIR[28] AFSR; MCASP_PDIR[27] AHCLKR; MCASP_PDIR[26] ACLKR; MCASP_PDIR[i] AXRi, where i =0 to 3	0x-(1) 0x-(2) 0x- (2) 0x1

(1) See Table 23-591.

(2) For more details on MCASP clock configurations , refer to Table 23-586.

23.8.5.1.2.3.5 Subsequence – MCASP Transmit Mute Input / Output Trigger Condition Settings

The procedure in Table 23-594 configures the behavior of the mute associated I/Os and different transmit trigger conditions for the MCASP mute output functionality.

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Table 23-594. MCASP Transmit Mute Input / Output Trigger Condition Settings

Step	Register/Bit Field/Programming Model	Value
Optional: Select to drive AMUTE active enable bit on transmit DATA port error.	MCASP_AMUTE[12] XDMAERR	0x1
Optional: Select to drive AMUTE active enable bit on transmit clock failure.	MCASP_AMUTE[10] XCKFAIL	0x1
Optional: Select to drive AMUTE active enable bit on transmit frame synchronization error.	MCASP_AMUTE[8] XSYNCERR	0x1
Optional: Select to drive AMUTE active enable bit on transmit underrun error.	MCASP_AMUTE[6] XUNDRN	0x1
Optional: Enable sensitivity of the abemcasp_amuteout output to abemcasp_amutein error source.	MCASP_AMUTE[3] INEN	0x1
Optional: Select the abemcasp_amutein input polarity.	MCASP_AMUTE[2] INPOL	0x1
Optional: Configure the behavior of the abemcasp_amuteout output.	MCASP_AMUTE[1:0] MUTEN	0x1

23.8.5.2 Operational Modes Configuration

23.8.5.2.1 MCASP Transmission Modes

23.8.5.2.1.1 Main Sequence – MCASP DIT- / TDM- Polling Transmission Method

Figure 23-193 shows the MCASP DIT- / TDM- polling method.

NOTE:

- The MCASP polling transmission model considers the MPU/DSP as the source of audio data for the MCASP transmission buffer.
- The transmit DMA request is disabled and the XDMAERR event is not analyzed.

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Figure 23-193. MCASP DIT- / TDM- Transmission Polling Method

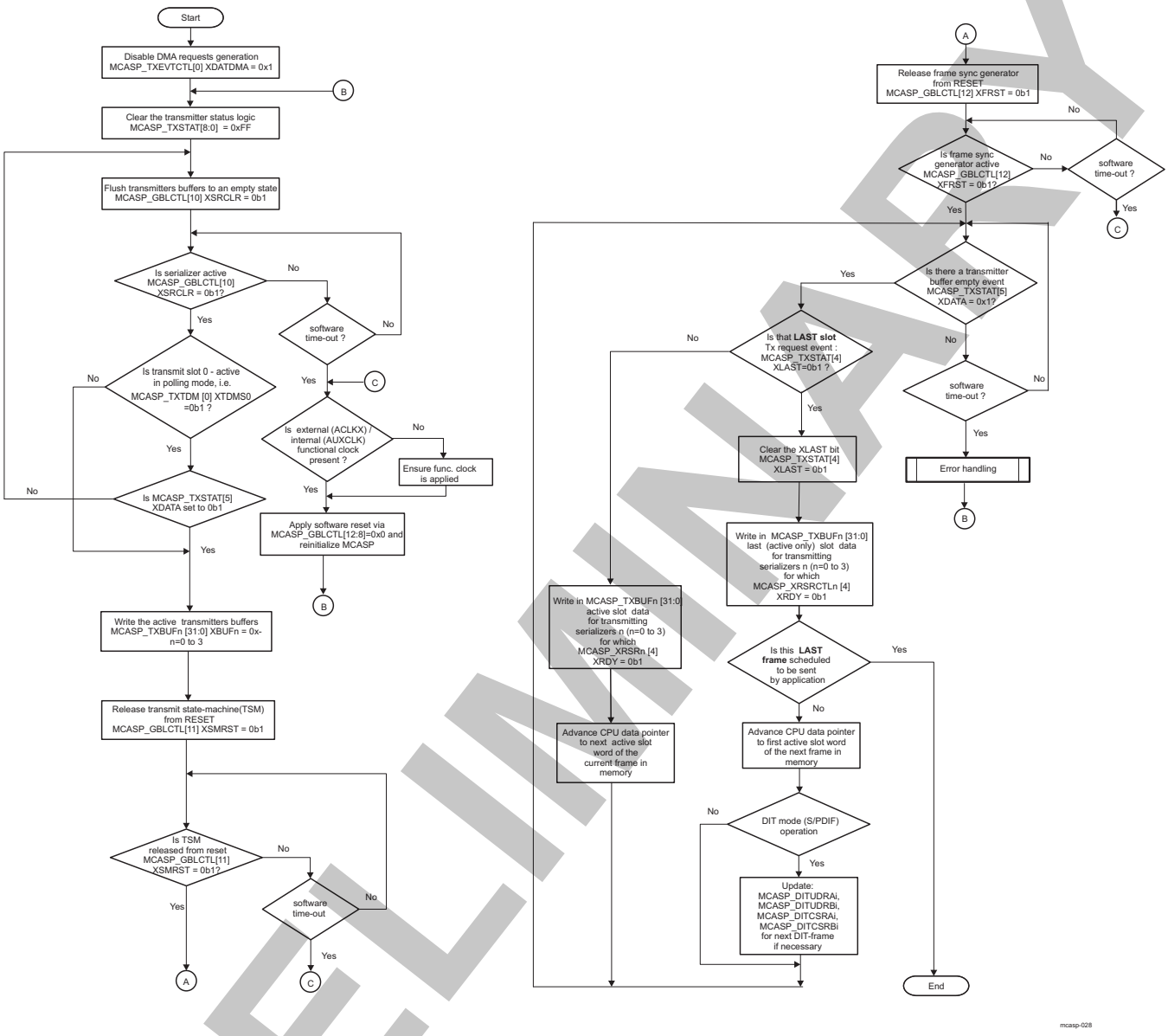

Table 23-595 summarizes the register call for the transmission DIT- / TDM- polling mode.

Table 23-595. Register Call Summary for Main Sequence – MCASP DIT- / TDM- Transmission Polling Method

Register Name
MCASP_TXEVTCTL
MCASP_TXSTAT
MCASP_GBLCTL
MCASP_TXTDM
MCASP_TXBUFn (n=0 to 3)
MCASP_XRSRCTLn (n=0 to 3)
MCASP_DITUDRAi (i=0 to 5)
MCASP_DITUDRBi (i=0 to 5)
MCASP_DITCSRAi (i=0 to 5)

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Table 23-595. Register Call Summary for Main Sequence – MCASP DIT- / TDM- Transmission Polling Method (continued)

Register Name
MCASP_DITCSRBi (i=0 to 5)

Table 23-596 summarizes the subprocess call for the DIT- / TDM- transmission polling mode.

Table 23-596. Subprocess Call Summary for Main Sequence – MCASP DIT- / TDM- Transmission Polling Method

Subprocess Name	Cross-Reference
Error handling	Figure 23-197

23.8.5.2.1.2 Main Sequence – MCASP DIT- / TDM - Interrupt Transmission Method

Figure 23-194 shows the initial setup for interrupt-based transmission.

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Figure 23-194. Subsequence – DIT- / TDM- Transmission Startup Procedure

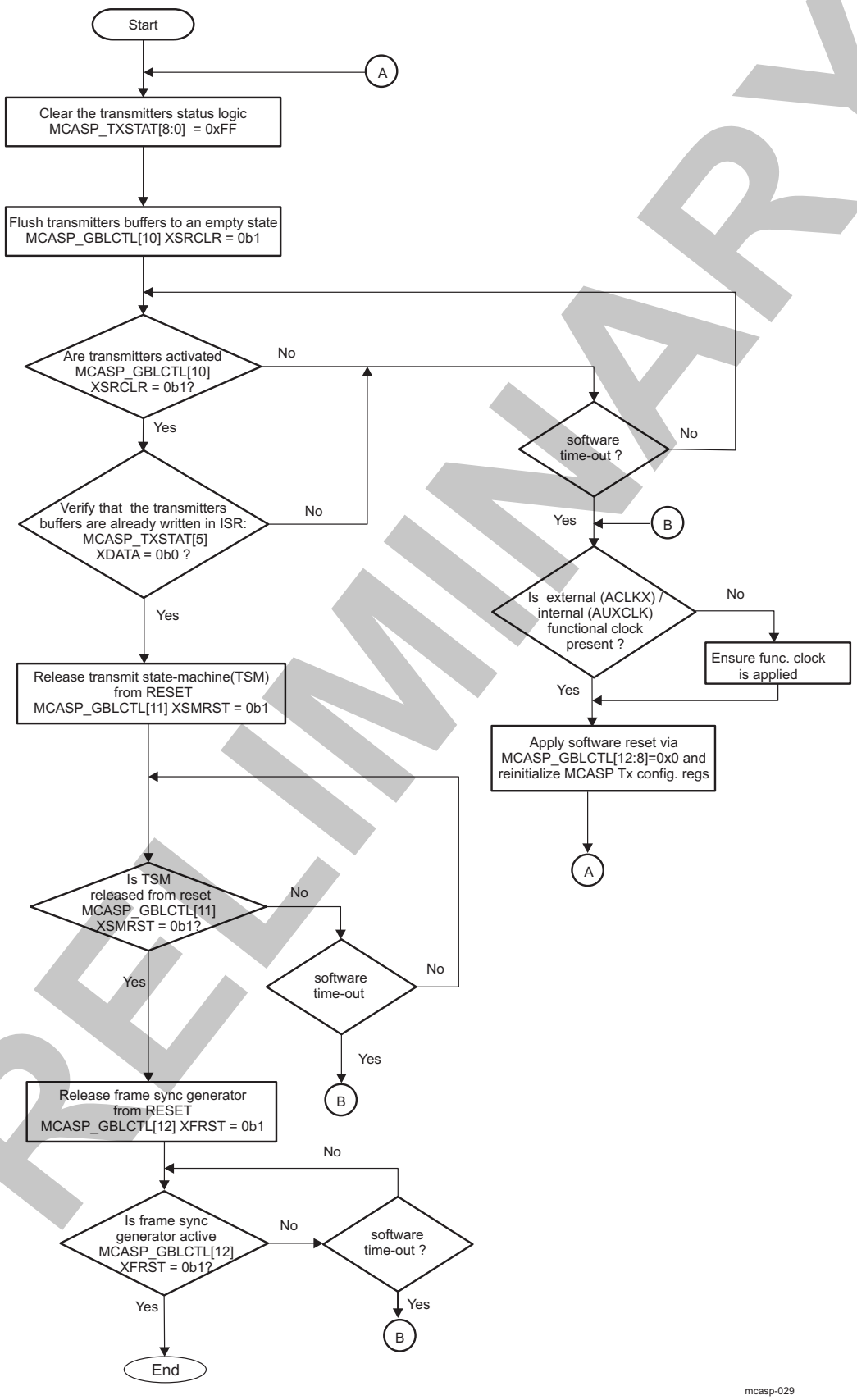

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Table 23-597 shows the configuration of the MCASP using an interrupt method for DIT- / TDM-transmission.

Table 23-597. MCASP DIT- / TDM- Interrupt Transmission Model

Step	Register/Bit Field/Programming Model	Value
Disable Tx DMA requests generation.	MCASP_TXEVTCTL[0] XDATDMA	0x1
Enable the data ready event transmit interrupt.	MCASP_EVTCTLX[5] XDATA	0x1
Optional: Enable the transmit error event interrupts.	MCASP_EVTCTLX[2] XCKFAIL MCASP_EVTCTLX[1] XSYNCERR MCASP_EVTCTLX[0] XUNDRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt (useful for DIT user data/ channel status next S/PDIF frame info update.)	MCASP_EVTCTLX [7] XSTAFRM MCASP_EVTCTLX[4] XLAST	0x1 0x1
IFwrite transfer is through the MCASP DATA port (MCASP_TXFMT[3] XBUSEL is set to 0b0).	Software test condition (setting is done in step4 of the *MCASP Transmitters Global Initialization* - see Table 23-577)	
Enable the DATA port error based interrupt.	MCASP_EVTCTLX[3] XDMAERR	0x1
ELSE		
Disable the DATA port error based interrupt.	MCASP_EVTCTLX[3] XDMAERR	0x0
ENDIF		
DIT / TDM - Transmission Startup Procedure	See Figure 23-194.	

Table 23-598 summarizes the register call to initialize the MCASP to transmit using interrupt events.

Table 23-598. Register Call Summary for Subsequence – MCASP DIT- / TDM- Transmission Startup Procedure

Register Name	Register Name
MCASP_GBLCTL	MCASP_TXSTAT

23.8.5.2.1.3 Main Sequence –MCASP DIT- / TDM - Mode DMA Transmission Method

Table 23-599 shows the configuration of the MCASP using the DMA method for transmission. Possible interrupt error event servicing is also considered. Table 23-598 shows the initial setup for DMA - based transmission.

NOTE: Because of the DATA port burst access capability with the DMA method, it is strongly recommended that DMA transfers are initiated through the MCASP DATA port.

Table 23-599. MCASP DMA Transmission Model with Interrupt Events Servicing

Step	Register/Bit Field/Programming Model	Value
Recommended: Select DATA port to access the transmit buffers.	MCASP_TXFMT[3] XBUSEL	0x0
Enable the Tx DMA requests generation.	MCASP_TXEVTCTL[0] XDATDMA	0x0
Enable the Tx DMA error event, because of MCASP DATA port usage.	MCASP_EVTCTLX[3] XDMAERR	0x1
Optional: Enable the transmit error event interrupts.	MCASP_EVTCTLX[2] XCKFAIL MCASP_EVTCTLX[1] XSYNCERR MCASP_EVTCTLX[0] XUNDRN	0x1 0x1 0x1
Optional: Enable the start of frame interrupt. Optional: Enable the last slot data interrupt.	MCASP_EVTCTLX [7] XSTAFRM MCASP_EVTCTLX[4] XLAST	0x1 0x1
Disable the data ready event transmit interrupt, as DMA is used to service this request.	MCASP_EVTCTLX[5] XDATA	0x0

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Table 23-599. MCASP DMA Transmission Model with Interrupt Events Servicing (continued)

Step	Register/Bit Field/Programming Model	Value
DMA startup transmission procedure. **This procedure is identical than the one shown in** Figure 23-194. The only difference is that DMA automatically services all the AXEVT events raised by the MCASP, and no CPU data processing intervention is required. The CPU is involved only in error handling shown in Figure 23-196.	See Figure 23-194.	

23.8.5.2.2 MCASP Reception Modes

23.8.5.2.2.1 Main Sequence – MCASP Polling Reception Method

Figure 23-195 shows the MCASP polling reception method.

NOTE: The MCASP polling reception model considers the MPU/DSP as the accessor of audio data from the MCASP receive buffers.

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Figure 23-195. MCASP Polling Reception Method

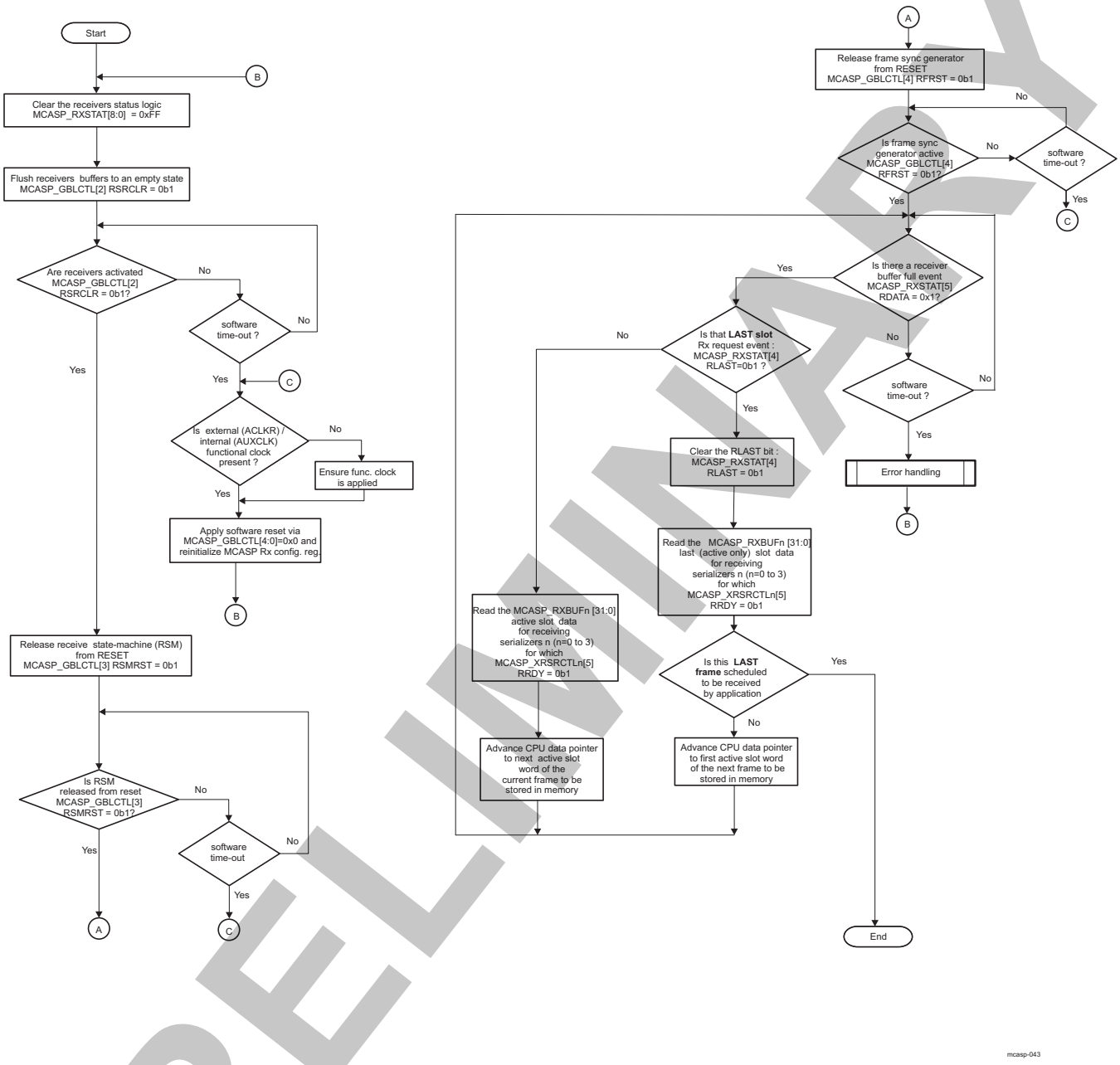

Table 23-600 summarizes the register call for the reception polling mode.

Table 23-600. Register Call Summary for Main Sequence – MCASP Reception Polling Method

Register Name
MCASP_RXSTAT
MCASP_GBLCTL
MCASP_RXBUFn (n=0 to 3)
MCASP_XRSRCTLn (n=0 to 3)

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Table 23-601 summarizes the subprocess call for the polling mode.

Table 23-601. Subprocess Call Summary for Main Sequence – MCASP Reception Polling Method

Subprocess Name	Cross-Reference
Error handling	Figure 23-198

23.8.5.2.3 MCASP Event Servicing

23.8.5.2.3.1 MCASP DIT- / TDM- Transmit Interrupt Events Servicing

Figure 23-196 shows the flow of DIT- / TDM- mode transmit interrupt events servicing for the MCASP module.

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Figure 23-196. MCASP Transmit Interrupt Events Servicing

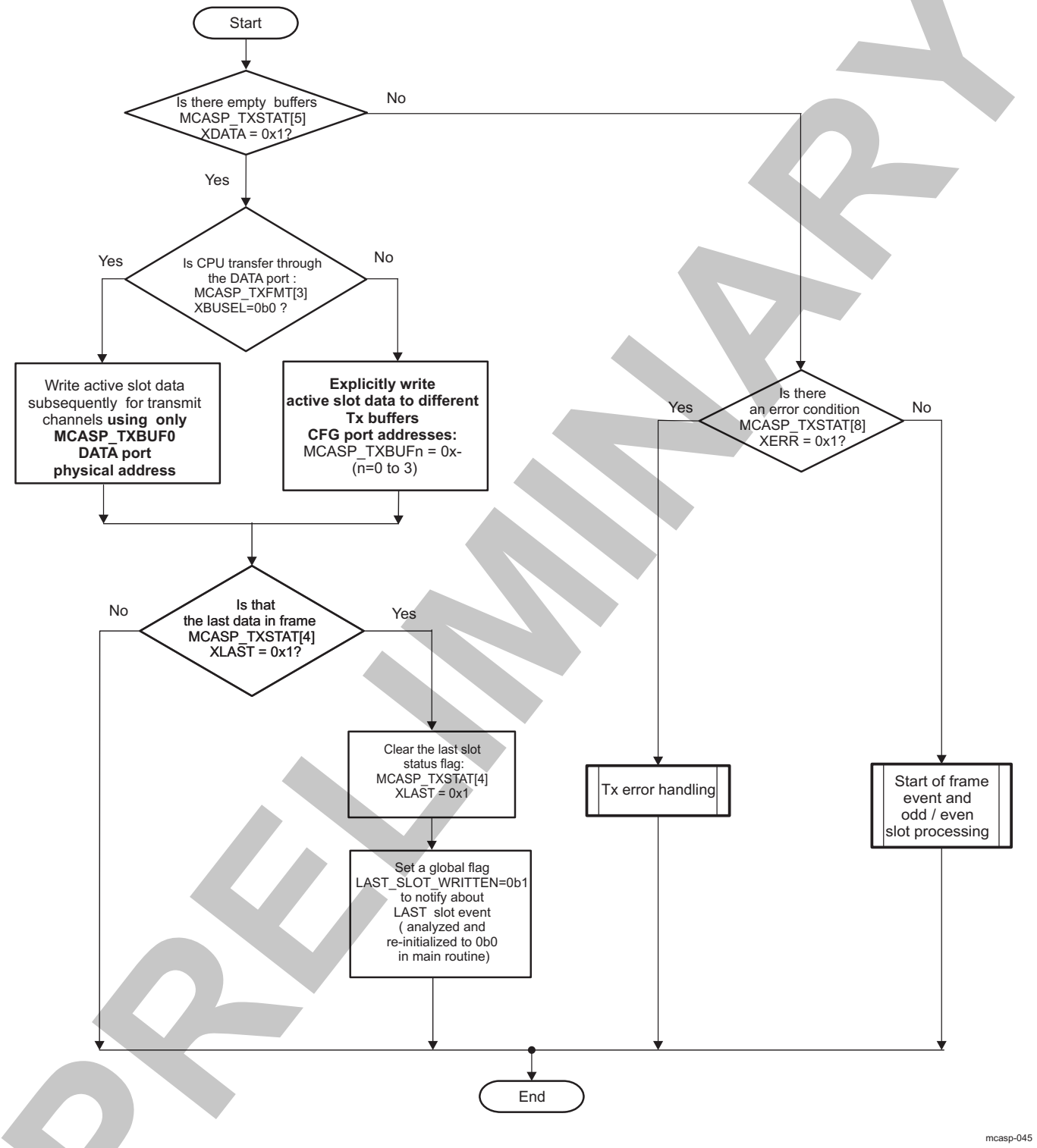

Table 23-602 lists the register call summary for the transmit interrupt events servicing.

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Table 23-602. Register Call Summary for MCASP Transmit Interrupt Events Servicing

Register Name	Register Name	Register Name
MCASP_TXSTAT	MCASP_TXBUFn	MCASP_TXFMT

Table 23-603 lists the subprocess call summary for transmit interrupt events servicing.

Table 23-603. Subprocess Call Summary for Transmit Interrupt Events Servicing

Subprocess Name	Cross-Reference
MCASP transmit error handling	Figure 23-197
Start of frame handling	Section 23.8.4.11.1

23.8.5.2.3.2 Subsequence – MCASP DIT- / TDM -Modes Transmit Error Handling

Figure 23-197 shows the transmit error handling schema for the MCASP, which can be implemented as part of the Tx interrupt service routine or as part of the Tx polling sequence.

Figure 23-197. MCASP Transmit Error Handling

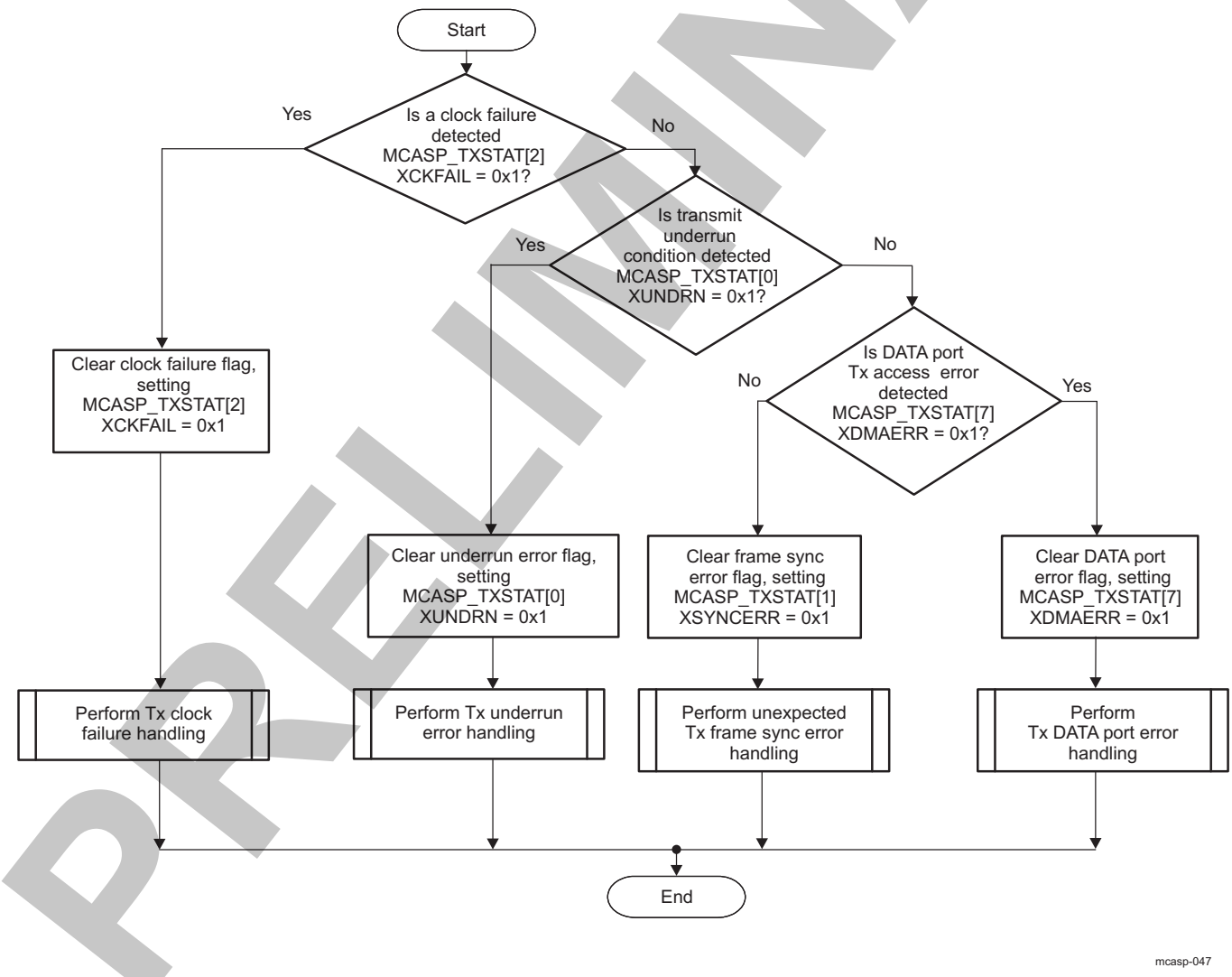

Table 23-604 lists the register call summary for the MCASP transmit error handling.

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Table 23-604. Register Call Summary for MCASP Transmit Error Handling

Register Name
MCASP_TXSTAT

NOTE:

- For more information about transmit clock failure handling, see Section 23.8.4.15.6.2, *Transmit Clock Failure Check and Recovery*.
- For more information about transmit buffer underrun handling, see Section 23.8.4.15.1, *Buffer Underrun Error -Transmitter*.
- For more information about DATA port Tx error handling, see Section 23.8.4.15.3, *DATA Port Error - Transmitter*.
- For more information about unexpected Tx frame sync error handling , see Section 23.8.4.15.5, *Unexpected Frame Sync Error*.

23.8.5.2.3.3 Subsequence – MCASP Receive Error Handling

Figure 23-198 shows the receive error handling schema for the MCASP, which can ONLY be implemented as part of the Rx polling sequence.

Figure 23-198. MCASP Receive Error Handling

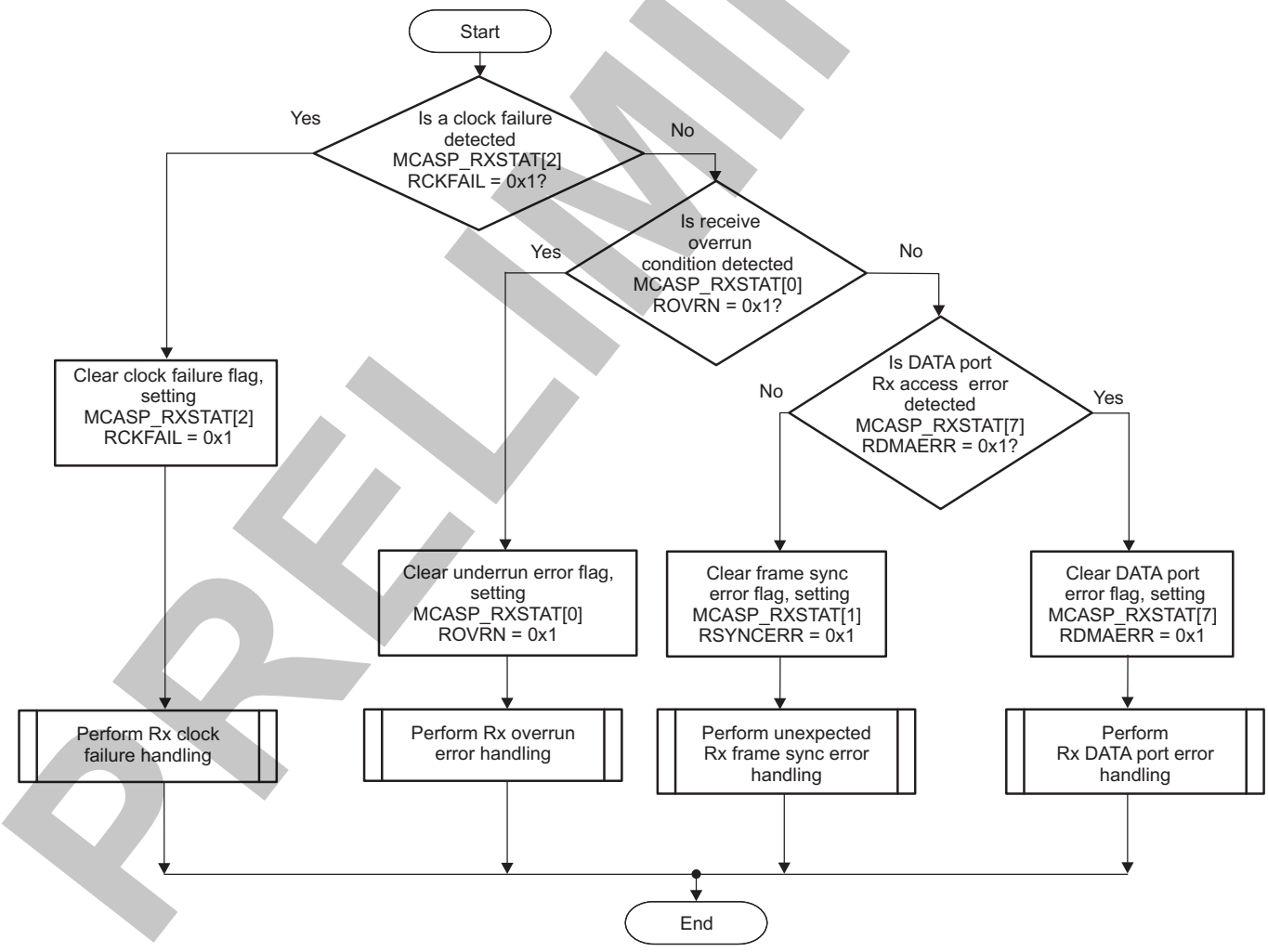

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Table 23-605 lists the register call summary for the MCASP receive error handling.

Table 23-605. Register Call Summary for MCASP Receive Error Handling

Register Name
MCASP_RXSTAT

NOTE:

- For more information about receive clock failure handling, see Section 23.8.4.15.6.3, *Receive Clock Failure Check and Recovery*.
- For more information about receive buffer overrun handling, see Section 23.8.4.15.2, *Buffer Overrun Error - Receiver* .
- For more information about DATA port Rx error handling, see Section 23.8.4.15.4, *DATA Port Error - Receiver* .
- For more information about unexpected Rx frame sync error handling , see Section 23.8.4.15.5, *Unexpected Frame Sync Error*.

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23.8.6 MCASP Register Manual

23.8.6.1 MCASP Instance Summary

Section 23.8.5.1.1 summarizes the MCASP instances.

Table 23-606. MCASP Instance Summary

Module Name	Base Address L3_MAIN Interconnect	Base Address Cortex-A15 Private Access	Base Address DSP Private Access	Size
MCASP_CFG	0x4902 8000	0x4012 8000	0x01D2 8000	4 KiB
MCASP_DATA	0x4902 A000	0x4012 A000	0x01D2 A000	4 KiB

NOTE: Private access is an access that does not use the L3_MAIN / L4 interconnects.

23.8.6.2 MCASP Registers

23.8.6.2.1 MCASP_CFG Register Summary

Table 23-607 summarizes the MCASP_CFG register mapping.

Table 23-607. MCASP_CFG Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MCASP_CFG Physical Address L3_MAIN Interconnect	MCASP_CFG Physical Address Cortex-A15 Private Access	MCASP_CFG Physical Address DSP Private Access
MCASP_PID	R	32	0x0000 0000	0x4902 8000	0x4012 8000	0x01D2 8000
MCASP_SYSCONFIG	RW	32	0x0000 0004	0x4902 8004	0x4012 8004	0x01D2 8004
MCASP_PFUNC	RW	32	0x0000 0010	0x4902 8010	0x4012 8010	0x01D2 8010
MCASP_PDIR	RW	32	0x0000 0014	0x4902 8014	0x4012 8014	0x01D2 8014
MCASP_PDOUT	RW	32	0x0000 0018	0x4902 8018	0x4012 8018	0x01D2 8018
MCASP_PDIN	R	32	0x0000 001C	0x4902 801C	0x4012 801C	0x01D2 801C
MCASP_PDSET	W	32	0x0000 001C	0x4902 801C	0x4012 801C	0x01D2 801C
MCASP_PDCLR	RW	32	0x0000 0020	0x4902 8020	0x4012 8020	0x01D2 8020
RESERVED	RW	32	0x0000 0030	0x4902 8030	0x4012 8030	0x01D2 8030
RESERVED	RW	32	0x0000 0034	0x4902 8034	0x4012 8034	0x01D2 8034
RESERVED	RW	32	0x0000 0038	0x4902 8038	0x4012 8038	0x01D2 8038
MCASP_GBLCTL	RW	32	0x0000 0044	0x4902 8044	0x4012 8044	0x01D2 8044
MCASP_AMUTE	RW	32	0x0000 0048	0x4902 8048	0x4012 8048	0x01D2 8048
MCASP_LBCTL	RW	32	0x0000 004C	0x4902 804C	0x4012 804C	0x01D2 804C
MCASP_TXDITCTL	RW	32	0x0000 0050	0x4902 8050	0x4012 8050	0x01D2 8050
RESERVED	RW	32	0x0000 0060	0x4902 8060	0x4012 8060	0x01D2 8060
MCASP_RXMASK	RW	32	0x0000 0064	0x4902 8064	0x4012 8064	0x01D2 8064
MCASP_RXFMT	RW	32	0x0000 0068	0x4902 8068	0x4012 8068	0x01D2 8068
MCASP_RXFMCTL	RW	32	0x0000 006C	0x4902 806C	0x4012 806C	0x01D2 806C
MCASP_ACLKRCTL	RW	32	0x0000 0070	0x4902 8070	0x4012 8070	0x01D2 8070
MCASP_AHCLKRCTL	RW	32	0x0000 0074	0x4902 8074	0x4012 8074	0x01D2 8074
MCASP_RXTDM	RW	32	0x0000 0078	0x4902 8078	0x4012 8078	0x01D2 8078
RESERVED	RW	32	0x0000 007C	0x4902 807C	0x4012 807C	0x01D2 807C
MCASP_RXSTAT	RW	32	0x0000 0080	0x4902 8080	0x4012 8080	0x01D2 8080
MCASP_RXTDMSLOT	R	32	0x0000 0084	0x4902 8084	0x4012 8084	0x01D2 8084

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Table 23-607. MCASP_CFG Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	MCASP_CFG Physical Address L3_MAIN Interconnect	MCASP_CFG Physical Address Cortex-A15 Private Access	MCASP_CFG Physical Address DSP Private Access
MCASP_RXCLKCHK	RW	32	0x0000 0088	0x4902 8088	0x4012 8088	0x01D2 8088
RESERVED	RW	32	0x0000 008C	0x4902 808C	0x4012 808C	0x01D2 808C
RESERVED	RW	32	0x0000 00A0	0x4902 80A0	0x4012 80A0	0x01D2 80A0
MCASP_TXMASK	RW	32	0x0000 00A4	0x4902 80A4	0x4012 80A4	0x01D2 80A4
MCASP_TXFMT	RW	32	0x0000 00A8	0x4902 80A8	0x4012 80A8	0x01D2 80A8
MCASP_TXFMCTL	RW	32	0x0000 00AC	0x4902 80AC	0x4012 80AC	0x01D2 80AC
MCASP_ACLKXCTL	RW	32	0x0000 00B0	0x4902 80B0	0x4012 80B0	0x01D2 80B0
MCASP_AHCLKXCTL	RW	32	0x0000 00B4	0x4902 80B4	0x4012 80B4	0x01D2 80B4
MCASP_TXTDM	RW	32	0x0000 00B8	0x4902 80B8	0x4012 80B8	0x01D2 80B8
MCASP_EVTCTLX	RW	32	0x0000 00BC	0x4902 80BC	0x4012 80BC	0x01D2 80BC
MCASP_TXSTAT	RW	32	0x0000 00C0	0x4902 80C0	0x4012 80C0	0x01D2 80C0
MCASP_TXTDMSLOT	R	32	0x0000 00C4	0x4902 80C4	0x4012 80C4	0x01D2 80C4
MCASP_TXCLKCHK	RW	32	0x0000 00C8	0x4902 80C8	0x4012 80C8	0x01D2 80C8
MCASP_TXEVTCTL	RW	32	0x0000 00CC	0x4902 80CC	0x4012 80CC	0x01D2 80CC
RESERVED	RW	32	0x0000 00D0	0x4902 80D0	0x4012 80D0	0x01D2 80D0
MCASP_DITCSRAi (1)	RW	32	0x0000 0100 + (0x04*i)	0x4902 8100 + (0x04*i)	0x4012 8100 + (0x04*i)	0x01D2 8100 + (0x04*i)
MCASP_DITCSRBi (1)	RW	32	0x0000 0118 + (0x04*i)	0x4902 8118 + (0x04*i)	0x4012 8118 + (0x04*i)	0x01D2 8118 + (0x04*i)
MCASP_DITUDRAi (1)	RW	32	0x0000 0130 + (0x04*i)	0x4902 8130 + (0x04*i)	0x4012 8130 + (0x04*i)	0x01D2 8130 + (0x04*i)
MCASP_DITUDRBi (1)	RW	32	0x0000 0148 + (0x04*i)	0x4902 8148 + (0x04*i)	0x4012 8148 + (0x04*i)	0x01D2 8148 + (0x04*i)
MCASP_XRSRCTLn(2)	RW	32	0x0000 0180 + (0x04*n)	0x4902 8180 + (0x04*n)	0x4012 8180 + (0x04*n)	0x01D2 8180 + (0x04*n)
RESERVED	RW	32	0x0000 0190 + (0x04*j) (3)	0x4902 8190 + (0x04*j)	0x4012 8190 + (0x04*j)	0x01D2 8190 + (0x04*j)
MCASP_TXBUFn (2)	RW	32	0x0000 0200 + (0x04*n)	0x4902 8200 + (0x04*n)	0x4012 8200 + (0x04*n)	0x01D2 8200 + (0x04*n)
RESERVED	RW	32	0x0000 0210 + (0x04*k) (4)	0x4902 8210 + (0x04*k)	0x4012 8210 + (0x04*k)	0x01D2 8210 + (0x04*k)
MCASP_RXBUFn (2)	RW	32	0x0000 0280 + (0x04*n)	0x4902 8280 + (0x04*n)	0x4012 8280 + (0x04*n)	0x01D2 8280 + (0x04*n)
RESERVED	RW	32	0x0000 0290 + (0x04*l) (5)	0x4902 8290 + (0x04*l)	0x4012 8290 + (0x04*l)	0x01D2 8290 + (0x04*l)

(1) i = 0 to 5
(2) n = 0 to 3
(3) j = 0 to 11
(4) k = 0 to 11
(5) l = 0 to 11

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NOTE: The address locations listed in Table 23-607, *MCASP_CFG Register Mapping Summary*, are relevant for accessing:

- all MCASP configuration registers
- MCASP_TXBUFn registers, (n=0 to 3)
- MCASP_RXBUFn registers, (n=0 to 3)

through the MCASP peripheral configuration (CFG) port.

The MCASP_TXFMT[3] XBUSEL bit must be set to 0b1, to allow CFG port write accesses to the MCASP XRBUFn buffer. The MCASP_RXFMT[3] RBUSEL bit must be set to 0b1, to allow CFG port read accesses to the MCASP XRBUFn buffer.

23.8.6.2.2 MCASP_CFG Register Description

Table 23-608 through Table 23-682 describe the individual MCASP_CFG register bits.

NOTE: For all of the below described regsiters, **the indexes n and N, when applying to serializers (NOT slots), vary in the range from 0 to 3**. The MCASP AXR0 - AXR3 I/Os match the device boundary level - abemcasp_axr - abemcasp_axr3 signals, respectively.

Table 23-608. MCASP_PID

Address Offset	0x0000 0000		
Physical Address	0x4902 8000 0x4012 8000 0x01D2 8000	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Peripheral identification register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI internal data

Table 23-609. Register Call Summary for Register MCASP_PID

Multichannel Audio Serial Port

- MCASP_CFG Register Summary: [0]

Table 23-610. MCASP_SYSCONFIG

Address Offset	0x0000 0004		
Physical Address	0x4902 8004 0x4012 8004 0x01D2 8004	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Power idle module configuration register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														IDLE_MODE	

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Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000000
1:0	IDLE_MODE	0x0: Force-idle mode 0x1: No-idle mode 0x2: Smart-idle mode - default state 0x3: Reserved	RW	0x2

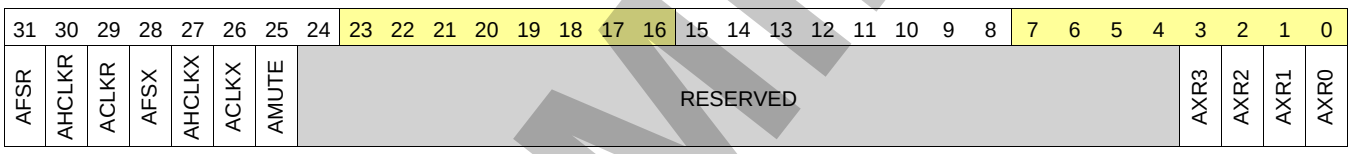
Table 23-611. Register Call Summary for Register MCASP_SYSCONFIG

Multichannel Audio Serial Port

- MCASP Power Management: [0] [1] [2]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [3]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [4]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [5]
- MCASP_CFG Register Summary: [6]

Table 23-612. MCASP_PFUNC

Address Offset	0x0000 0010		
Physical Address	0x4902 8010 0x4012 8010 0x01D2 8010	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Specifies the function of the pins as either a MCASP pin or a GPIO pin		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	AFSR	Determines if AFSR pin (device level abemcasp_afsr signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0
30	AHCLKR	Determines if AHCLKR pin (device level abemcasp_ahclkr signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0
29	ACLKR	Determines if ACLKR pin (device level abemcasp_aclkr signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0
28	AFSX	Determines if AFSX pin (device level abemcasp_afsx signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0
27	AHCLKX	Determines if AHCLKX pin (device level abemcasp_ahclkx signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0
26	ACLKX	Determines if ACLKX pin (device level abemcasp_aclkx signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0

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Bits	Field Name	Description	Type	Reset
25	AMUTE	Determines if AMUTE pin (device level abemcasp_amuteout signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0
24:4	RESERVED	Reserved	RW	0x000
3	AXR3	Determines if AXR3 pin (device level abemcasp_axr3 signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0
2	AXR2	Determines if AXR2 pin (device level abemcasp_axr2 signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0
1	AXR1	Determines if AXR1 pin (device level abemcasp_axr1 signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0
0	AXR0	Determines if AXR0 pin (device level abemcasp_axr signal) functions as MCASP or GPIO. 0x0: Pin functions as MCASP pin 0x1: Pin functions as GIO pin	RW	0

Table 23-613. Register Call Summary for Register MCASP_PFUNC

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Transmit DIT Clock and Frame-Sync Generation: [1]
- Loopback Modes: [2] [3] [4]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [5]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [6]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [7]
- MCASP_CFG Register Summary: [8]
- MCASP_CFG Register Description: [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26]

Table 23-614. MCASP_PDIR

Address Offset	0x0000 0014		
Physical Address	0x4902 8014 0x4012 8014 0x01D2 8014	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Pin direction register - specifies the direction of the MCASP pins as either an input or an output pin.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																					AXR3	AXR2	AXR1	AXR0

Bits	Field Name	Description	Type	Reset
31	AFSR	Determines if AFSR pin (device level abemcasp_afsr signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0

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Bits	Field Name	Description	Type	Reset
30	AHCLKR	Determines if AHCLKR pin (device level abemcasp_ahclkr signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0
29	ACLKR	Determines if ACLKR pin (device level abemcasp_aclkr signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0
28	AFSX	Determines if AFSX pin (device level abemcasp_afsx signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0
27	AHCLKX	Determines if AHCLKX pin (device level abemcasp_ahclkx signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0
26	ACLKX	Determines if ACLKX pin (device level abemcasp_aclkx signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0
25	AMUTE	Determines if AMUTE pin (device level abemcasp_amuteout signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0
24:4	RESERVED	Reserved	RW	0x000
3	AXR3	Determines if AXR3 pin (device level abemcasp_axr3 signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0
2	AXR2	Determines if AXR2 pin (device level abemcasp_axr2 signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0
1	AXR1	Determines if AXR1 pin (device level abemcasp_axr1 signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0
0	AXR0	Determines if AXR0 pin (device level abemcasp_axr signal) functions as an input or output. 0x0: Input 0x1: Output	RW	0

Table 23-615. Register Call Summary for Register MCASP_PDIR

Multichannel Audio Serial Port

- MCASP Signals: [0]
- Time-Division Multiplexed (TDM) Transfer Mode: [1]
- Transmit DIT Clock and Frame-Sync Generation: [2]
- Loopback Modes: [3] [4] [5]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [6] [7] [8] [9] [10]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [11] [12] [13] [14] [15] [16] [17] [18] [19] [20]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [21] [22] [23] [24] [25] [26] [27] [28] [29] [30]
- MCASP_CFG Register Summary: [31]
- MCASP_CFG Register Description: [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49]

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Table 23-616. MCASP_PDOUT

Address Offset	0x0000 0018		
Physical Address	0x4902 8018 0x4012 8018 0x01D2 8018	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP

Description

Pin data output register - holds a value for data out at all times, and may be read back at all times. The value held by MCASP_PDOUT is not affected by writing to MCASP_PDIR and MCASP_PFUNC. However, the data value in MCASP_PDOUT is driven out onto the MCASP pin only if the corresponding bit in MCASP_PFUNC is set to 1 (GPIO function) and the corresponding bit in MCASP_PDIR is set to 1 (output).

When reading data, it returns the corresponding bit value in MCASP_PDOUT[n]; it does not return the input from the I/O pin.

When writing data, writes to the corresponding MCASP_PDOUT[n] bit.

PDOUT has these aliases or alternate addresses:

- MCASP_PDSET - when written to at this address, writing a 1 to a bit in MCASP_PDSET sets the corresponding bit in MCASP_PDOUT to 1; writing a 0 has no effect and keeps the bits in MCASP_PDOUT unchanged.
- MCASP_PDCLR - when written to at this address, writing a 1 to a bit in MCASP_PDCLR clears the corresponding bit in MCASP_PDOUT to 0; writing a 0 has no effect and keeps the bits in MCASP_PDOUT unchanged

There is only one set of data-out bits, MCASP_PDOUT[31:0]. The other registers, MCASP_PDSET and MCASP_PDCLR, are just different addresses for the same control bits, with different behaviors during writes.

Type RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																					AXR3	AXR2	AXR1	AXR0

Bits	Field Name	Description	Type	Reset
31	AFSR	Determines drive on AFSR output pin when the corresponding MCASP_PFUNC[31] and MCASP_PDIR[31] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
30	AHCLKR	Determines drive on AHCLKR output pin when the corresponding MCASP_PFUNC[30] and MCASP_PDIR[30] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
29	ACLKR	Determines drive on ACLKR output pin when the corresponding MCASP_PFUNC[29] and MCASP_PDIR[29] bits are set to 1 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
28	AFSX	Determines drive on AFSX output pin when the corresponding MCASP_PFUNC[28] and MCASP_PDIR[28] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
27	AHCLKX	Determines drive on AHCLKX output pin when the corresponding MCASP_PFUNC[27] and MCASP_PDIR[27] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
26	ACLKX	Determines drive on ACLKX output pin when the corresponding MCASP_PFUNC[26] and MCASP_PDIR[26] bits are set to 1 0x0: The pin drives low. 0x1: The pin drives high.	RW	0

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Bits	Field Name	Description	Type	Reset
25	AMUTE	Determines drive on AMUTE output pin when the corresponding MCASP_PFUNC[25] and MCASP_PDIR[25] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
24:4	RESERVED	Reserved	RW	0x000
3	AXR3	Determines drive on AXR3 output pin when the corresponding MCASP_PFUNC[3] and MCASP_PDIR[3] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
2	AXR2	Determines drive on AXR2 output pin when the corresponding MCASP_PFUNC[2] and MCASP_PDIR[2] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
1	AXR1	Determines drive on AXR1 output pin when the corresponding MCASP_PFUNC[1] and MCASP_PDIR[1] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0
0	AXR0	Determines drive on AXR0 output pin when the corresponding MCASP_PFUNC[0] and MCASP_PDIR[0] bits are set to 1. 0x0: The pin drives low. 0x1: The pin drives high.	RW	0

Table 23-617. Register Call Summary for Register MCASP_PDOUT

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- MCASP_CFG Register Summary: [1]
- MCASP_CFG Register Description: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58]

Table 23-618. MCASP_PDIN

Address Offset	0x0000 001C		
Physical Address	0x4902 801C 0x4012 801C 0x01D2 801C	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Pin data input register - holds the state of all the MCASP pins. MCASP_PDIN allows reading the actual value of the pin, regardless of the state of MCASP_PFUNC and MCASP_PDIR.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																					AXR3	AXR2	AXR1	AXR0

Bits	Field Name	Description	Type	Reset
31	AFSR	Logic level on AFSR pin (device level abemcasp_afsr signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
30	AHCLKR	Logic level on AHCLKR pin (device level abemcasp_ahclkr signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0

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Bits	Field Name	Description	Type	Reset
29	ACLKR	Logic level on ACLKR pin (device level abemcasp_aclkr signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
28	AFSX	Logic level on AFSX pin (device level abemcasp_afsx signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
27	AHCLKX	Logic level on AHCLKX pin (device level abemcasp_ahclkx signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
26	ACLKX	Logic level on ACLKX pin (device level abemcasp_aclkx signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
25	AMUTE	Logic level on AMUTE pin (device level abemcasp_amuteout signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
24:4	RESERVED	Reserved	R	0x000
3	AXR3	Logic level on AXR3 pin (device level abemcasp_axr3 signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
2	AXR2	Logic level on AXR2 pin (device level abemcasp_axr2 signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
1	AXR1	Logic level on AXR1 pin (device level abemcasp_axr1 signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0
0	AXR0	Logic level on AXR0 pin (device level abemcasp_axr signal). 0x0: Pin is logic low. 0x1: Pin is logic high.	R	0

Table 23-619. Register Call Summary for Register MCASP_PDIN

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- MCASP_CFG Register Summary: [1]
- MCASP_CFG Register Description: [2]

Table 23-620. MCASP_PDSET

Address Offset	0x0000 001C		
Physical Address	0x4902 801C 0x4012 801C 0x01D2 801C	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The pin data set register is an alias of the pin data output register (MCASP_PDOUT) for writes only. Writing a 1 to the MCASP_PDSET bit sets the corresponding bit in MCASP_PDOUT and, if MCASP_PFUNC = 1 (GPIO function) and MCASP_PDIR = 1 (output), drives a logic high on the pin.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																					AXR3	AXR2	AXR1	AXR0

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Bits	Field Name	Description	Type	Reset
31	AFSR	Allows the corresponding AFSR bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[31] bit is set to 1.	W	0
30	AHCLKR	Allows the corresponding AHCLKR bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[30] bit is set to 1.	W	0
29	ACLKR	Allows the corresponding ACLKR bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[29] bit is set to 1.	W	0
28	AFSX	Allows the corresponding AFSX bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[28] bit is set to 1.	W	0
27	AHCLKX	Allows the corresponding AHCLKX bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[27] bit is set to 1.	W	0
26	ACLKX	Allows the corresponding ACLKX bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[26] bit is set to 1.	W	0
25	AMUTE	Allows the corresponding AMUTE bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[25] bit is set to 1.	W	0
24:4	RESERVED	Reserved	W	0x000
3	AXR3	Allows the AXR3 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[3] bit is set to 1.	W	0
2	AXR2	Allows the AXR2 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[2] bit is set to 1.	W	0
1	AXR1	Allows the AXR1 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[1] bit is set to 1.	W	0
0	AXR0	Allows the AXR0 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[0] bit is set to 1.	W	0

Table 23-621. Register Call Summary for Register MCASP_PDSET

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- MCASP_CFG Register Summary: [1]
- MCASP_CFG Register Description: [2] [3] [4] [5]

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Table 23-622. MCASP_PDCLR

Address Offset	0x0000 0020		
Physical Address	0x4902 8020 0x4012 8020 0x01D2 8020	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The pin data clear register is an alias of the pin data output register (MCASP_PDOUT) for writes only. Writing a 1 to the MCASP_PDCLR bit clears the corresponding bit in MCASP_PDOUT and, if MCASP_PFUNC = 1 (GPIO function) and MCASP_PDIR = 1 (output), drives a logic low on the pin.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSR	AHCLKR	ACLKR	AFSX	AHCLKX	ACLKX	AMUTE	RESERVED																					AXR3	AXR2	AXR1	AXR0

Bits	Field Name	Description	Type	Reset
31	AFSR	Allows the corresponding AFSR bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[31] bit is cleared to 0.	RW	0
30	AHCLKR	Allows the corresponding AHCLKR bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[30] bit is cleared to 0.	RW	0
29	ACLKR	Allows the corresponding ACLKR bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[29] bit is cleared to 0.	RW	0
28	AFSX	Allows the corresponding AFSX bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[28] bit is cleared to 0.	RW	0
27	AHCLKX	Allows the corresponding AHCLKX bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[27] bit is cleared to 0.	RW	0
26	ACLKX	Allows the corresponding ACLKX bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[26] bit is cleared to 0.	RW	0
25	AMUTE	Allows the corresponding AMUTE bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[25] bit is cleared to 0.	RW	0
24:4	RESERVED	Reserved	RW	0x000
3	AXR3	Allows the AXR3 bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[3] bit is cleared to 0.	RW	0

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Bits	Field Name	Description	Type	Reset
2	AXR2	Allows the AXR2 bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[2] bit is cleared to 0.	RW	0
1	AXR1	Allows the AXR1 bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[1] bit is cleared to 0.	RW	0
0	AXR0	Allows the AXR0 bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0x0: No effect 0x1: MCASP_PDOUT[0] bit is cleared to 0.	RW	0

Table 23-623. Register Call Summary for Register MCASP_PDCLR

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- MCASP_CFG Register Summary: [1]
- MCASP_CFG Register Description: [2] [3] [4] [5]

Table 23-624. MCASP_GBLCTL

Address Offset	0x0000 0044		
Physical Address	0x4902 8044 0x4012 8044 0x01D2 8044	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Global transmit control register - provides initialization of the transmit and receive sections. The bit fields in MCASP_GBLCTL are synchronized and latched by the transmitter and receiver corresponding clocks - abemcasp_aclkx clock (bits [12:8]) and abemcasp_aclkr (bits [4:0]), respectively. Before programming MCASP_GBLCTL, ensure that the serial clocks are running. If the corresponding external serial clocks - abemcasp_clkx and abemcasp_aclkr, are not yet running, select the internal serial clock source in AHCLKXCTL, AHCLKRCTL, ACLKXCTL and ACLKRCTL before programming the MCASP_GBLCTL. Also, after programming any bits in MCASP_GBLCTL, do not proceed until reading back from MCASP_GBLCTL and verifying that the bits in MCASP_GBLCTL are latched.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			XFRST	XSMRST	XSRCLR	XHCLKRST	XCLKRST	RESERVED				RFRST	RSMRST	RSRCLR	RHCLKRST	RCLKRST

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	RW	0x00000
12	XFRST	Transmit frame-sync generator reset enable bit 0x0: The transmit frame-sync generator is reset. 0x1: The transmit frame-sync generator is active. When released from reset, the transmit frame-sync generator begins counting serial clocks and generating frame sync as programmed.	RW	0

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Bits	Field Name	Description	Type	Reset
11	XSMRST	Transmit state-machine reset enable bit 0x0: The transmit state-machine is held in reset. AXR[n] pin state : If MCASP_PFUNC[n] = 0 and MCASP_PDIR[n] = 1, the corresponding serializer [n] drives the AXR[n] pin to the state specified for inactive time slot. 0x1: The transmit state-machine is released from reset. When released from reset, the transmit state-machine immediately transfers data from XBUF[n] to XRSR[n]. The transmit state-machine sets the underrun flag (XUNDRN) in MCASP_XSTAT, if XBUF[n] have not been preloaded with data before reset is released. The transmit state-machine also immediately begins detecting frame sync and is ready to transmit. Transmission of TDM time slot begins at slot 0 after reset is released.	RW	0
10	XSRCLR	Transmit serializer clear enable bit. By clearing and then setting this bit, the transmit buffer is flushed to an empty state (XDATA = 1). If XSMRST = 1, XSRCLR = 1, XDATA = 1, and XBUF is not loaded with new data before the start of the next active time slot, an underrun occurs. 0x0: The transmit serializer is cleared. 0x1: The transmit serializer is active. When the transmit serializer is first taken out of reset (XSRCLR changes from 0 to 1), the transmit data ready bit (XDATA) in MCASP_XSTAT is set to indicate XBUF is ready to be written.	RW	0
9	XHCLKRST	Transmit high-frequency clock divider reset enable bit 0x0: The transmitter high-frequency clock divider is held in reset. 0x1: The transmitter high-frequency clock divider is running.	RW	0
8	XCLKRST	Transmit clock divider reset enable bit 0x0: The transmit clock divider is held in reset. When the clock divider is in reset, it passes through a divide-by-1 of its input. 0x1: The transmit clock divider is running.	RW	0
7:5	RESERVED	Reserved	RW	0x0
4	RFRST	Receive frame sync generator reset enable bit. 0x0: Receive frame sync generator is reset. 0x1: Receive frame sync generator is active. When released from reset, the receive frame sync generator begins counting serial clocks and generating frame sync as programmed.	RW	0
3	RSMRST	Receive state machine reset enable bit. 0x0: Receive state machine is held in reset. 0x1: Receive state machine is released from reset. When released from reset, the receive state machine immediately begins detecting frame sync and is ready to receive. Receive TDM time slot begins at slot 0 after reset is released.	RW	0
2	RSRCLR	Receive serializer clear enable bit. By clearing then setting this bit, the receive buffer is flushed. 0x0: Receive serializers are cleared. 0x1: Receive serializers are active.	RW	0
1	RHCLKRST	Receive high-frequency clock divider reset enable bit. 0x0: Receive high-frequency clock divider is held in reset. 0x1: Receive high-frequency clock divider is running.	RW	0
0	RCLKRST	Receive clock divider reset enable bit. 0x0: Receive clock divider is held in reset. When the clock divider is in reset, it passes through a divide-by-1 of its input. 0x1: Receive clock divider is running.	RW	0

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Table 23-625. Register Call Summary for Register MCASP_GBLCTL

Multichannel Audio Serial Port

- MCASP Software Reset: [0] [1]
- Time-Division Multiplexed (TDM) Transfer Mode: [2]
- Transmit DIT Clock and Frame-Sync Generation: [3]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [4] [5] [6] [7] [8] [9] [10]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [11] [12] [13] [14] [15] [16] [17]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [18] [19] [20] [21] [22] [23] [24]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [25]
- Main Sequence – MCASP DIT- / TDM - Interrupt Transmission Method: [26]
- Main Sequence – MCASP Polling Reception Method: [27]
- MCASP_CFG Register Summary: [28]
- MCASP_CFG Register Description: [29] [30] [31] [32] [33] [34]

Table 23-626. MCASP_AMUTE

Address Offset	0x0000 0048		
Physical Address	0x4902 8048 0x4012 8048 0x01D2 8048	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Mute control register - Controls the MCASP mute output pin - AMUTE (device level - abemcasp_amuteout signal)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			XDMAERR	RDMAERR	XCKFAIL	RCKFAIL	XSYNCERR	RSYNCERR	XUNDRN	ROVRN	INSTAT	INEN	INPOL	MUTEN

Bits	Field Name	Description	Type	Reset
31:13	RESERVED	Reserved	RW	0x00000
12	XDMAERR	Drives AMUTE active enable bit on transmit DMA error (XDMAERR). 0x0: Drive is disabled. Detection of transmit DMA error is ignored by abemcasp_amuteout. 0x1: Drive is enabled (active). Upon detection of transmit DMA error, abemcasp_amuteout is active and is driven according to MUTEN bits.	RW	0
11	RDMAERR	If receive DMA error (RDMAERR), drive AMUTE active enable bit. 0x0: Drive is disabled. Detection of receive DMA error is ignored by AMUTE. 0x1: Drive is enabled (active). Upon detection of receive DMA error, AMUTE is active and is driven according to MUTEN bit.	RW	0
10	XCKFAIL	XMT bad clock. Drives AMUTE active enable bit on transmit clock failure (XCKFAIL). 0x0: Drive is disabled. Detection of transmit clock failure is ignored by abemcasp_amuteout. 0x1: Drive is enabled (active). Upon detection of transmit clock failure, abemcasp_amuteout is active and is driven according to MUTEN bits.	RW	0
9	RCKFAIL	If receive clock failure (RCKFAIL), drive AMUTE active enable bit. 0x0: Drive is disabled. Detection of receive clock failure is ignored by AMUTE. 0x1: Drive is enabled (active). Upon detection of receive clock failure, AMUTE is active and is driven according to MUTEN bit.	RW	0

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Bits	Field Name	Description	Type	Reset
8	XSYNCERR	XMT unexpected FS. Drives AMUTE active enable bit on unexpected transmit frame-sync error (XSYNCERR). 0x0: Drive is disabled. Detection of unexpected transmit frame-sync error is ignored by abemcasp_amuteout. 0x1: Drive is enabled (active). Upon detection of unexpected transmit frame-sync error, abemcasp_amuteout is active and is driven according to MUTEN bit.	RW	0
7	RSYNCERR	If unexpected receive frame sync error (RSYNCERR), drive AMUTE active enable bit. 0x0: Drive is disabled. Detection of unexpected receive frame sync error is ignored by AMUTE. 0x1: Drive is enabled (active). Upon detection of unexpected receive frame sync error, AMUTE is active and is driven according to MUTEN bit.	RW	0
6	XUNDRN	XMT underrun occurs. Drives AMUTE active enable bit on ransmit underrun error (XUNDRN). 0x0: Drive is disabled. Detection of transmit underrun error is ignored by abemcasp_amuteout. 0x1: Drive is enabled (active). Upon detection of transmit underrun error, abemcasp_amuteout is active and is driven according to MUTEN bit.	RW	0
5	ROVRN	If receiver overrun error (ROVRN), drive AMUTE active enable bit. 0x0: Drive is disabled. Detection of receiver overrun error is ignored by AMUTE. 0x1: Drive is enabled (active). Upon detection of receiver overrun error, AMUTE is active and is driven according to MUTEN bit.	RW	0
4	INSTAT	Status of mute in pin, determines drive on AXR[n] pin, when the MCASP_PFUNC[n] and MCASP_PDIR[n] bits are set to 1. Read 0x0: Inactive Read 0x1: Active. Audio mute in error is detected.	R	0
3	INEN	Drive the device level abemcasp_amuteout signal active when abemcasp_amutein error is active. 0x0: Drive is disabled. abemcasp_amutein is ignored by abemcasp_amuteout. 0x1: Drive is enabled (active). INSTAT = 1 drives abemcasp_amuteout active.	RW	0
2	INPOL	Audio mute in - AMUTEIN pin (device level abemcasp_amutein signal) polarity select bit 0x0: Polarity is active high. A high on abemcasp_amutein sets INSTAT to 1. 0x1: Polarity is active low. A low on abemcasp_amutein sets INSTAT to 1.	RW	0
1:0	MUTEN	AMUTE pin (device level abemcasp_amuteout signal) enable bit field (unless overridden by GPIO registers) 0x0: Disabled, pin goes to 3-state condition. 0x1: Pin is driven high if error is detected. 0x2: Pin is driven low if error is detected.	RW	0x0

Table 23-627. Register Call Summary for Register MCASP_AMUTE

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Transmit DIT Clock and Frame-Sync Generation: [1]
- Audio Mute (AMUTE) Function: [2] [3] [4] [5]
- Clock Failure Check Startup: [6] [7]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [8] [9] [10] [11] [12] [13] [14]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [15] [16] [17] [18] [19] [20] [21]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [22] [23] [24] [25] [26] [27] [28]
- MCASP_CFG Register Summary: [29]

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Table 23-628. MCASP_LBCTL

Address Offset	0x0000 004C		
Physical Address	0x4902 804C 0x4012 804C 0x01D2 804C	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The digital loopback control register (MCASP_LBCTL) controls the internal (MCASP module)-level and chip-level loopback settings of the MCASP in TDM mode. Note that loopback is NOT supported if MCASP is configured in DIT mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IOLBEN	MODE			ORD	DLBEN

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	RW	0x000 0000
4	IOLBEN	If DLBEN=0b1, the IOLBEN bit selects between **internal-level (MCASP module-level)** and **chip I/O-level** loopback modes. IOLBEN bit value is irrelevant, If DLBEN=0b0. 0x0: MCASP internal loopback mode enabled. This selects a direct loopback between corresponding MCASP AXRn and AXRn+1 pins, bypassing device pad I/O buffers. 0x1: Chip I/O-level loopback mode enabled. The MCASP data is looped back through the device pad I/O buffers.	RW	0
3:2	MODE	Loopback generator mode bits. 0x0: MODE must be set to 0x0 when MCASP is in non-loopback mode (DLBEN = 0b0) 0x1: MODE must be set to 0x1 when MCASP operates in loopback mode (DLBEN =0b1). This is necessary to allow transmit clock and frame sync generators to be used by both transmit and receive sections. 0x2, 0x3: Reserved	RW	0x0
1	ORD	Loopback order bit when loopback mode is enabled (DLBEN = 1). 0x0: Odd serializers N + 1 transmit to even serializers N that receive. The corresponding serializers must be programmed properly. 0x1: Even serializers N transmit to odd serializers N+1 that receive. The corresponding serializers must be programmed properly.	RW	0
0	DLBEN	Loop back mode. 0x0: Loop back mode is disabled (normal MCASP operation). 0x1: Loop back is enabled (TDM mode only). Loopback type is selected in IOLBEN bit.	RW	0

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Table 23-629. Register Call Summary for Register MCASP_LBCTL

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Loopback Modes: [1] [2] [3] [4] [5]
- Loopback Mode Configurations: [6] [7] [8] [9]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [10]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [11]
- MCASP_CFG Register Summary: [12]
- MCASP_CFG Register Description: [13]

Table 23-630. MCASP_TXDITCTL

Address Offset	0x0000 0050		
Physical Address	0x4902 8050 0x4012 8050 0x01D2 8050	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmit DIT mode control register, controls DIT operations of the MCASP		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												VB	VA	RESERVED	DITEN

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	RW	0x0000000
3	VB	Valid bit for odd time slots (DIT right subframe). 0x0: V bit is 0 during odd DIT subframes. 0x1: V bit is 1 during odd DIT subframes.	RW	0
2	VA	Valid bit for even time slots (DIT left subframe). 0x0: V bit is 0 during even DIT subframes. 0x1: V bit is 1 during even DIT subframes.	RW	0
1	RESERVED	Reserved	RW	0
0	DITEN	DIT mode enable bit 0x0: DIT mode is disabled. 0x1: DIT mode is enabled. Transmitter operates in DIT encoded mode.	RW	0

Table 23-631. Register Call Summary for Register MCASP_TXDITCTL

Multichannel Audio Serial Port

- Synchronous and Asynchronous Transmit and Receive Operations: [0] [1]
- Time-Division Multiplexed (TDM) Transfer Mode: [2]
- Transmit DIT Clock and Frame-Sync Generation: [3]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [4] [5] [6]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [7]
- MCASP_CFG Register Summary: [8]

Table 23-632. MCASP_RXMASK

Address Offset	0x0000 0064		
Physical Address	0x4902 8064 0x4012 8064 0x01D2 8064	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP

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Table 23-632. MCASP_RXMASK (continued)

Description	The receive format unit bit mask register (MCASP_RXMASK) determines which bits of the received data are masked off and padded with a known value before being read by the CPU.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RMASK[31:0]																															

Bits	Field Name	Description	Type	Reset
31: 0	RMASK[31:0]	Receive data mask enable bit. 0x0: Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in RFMT). 0x1: Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU.	RW	0

Table 23-633. Register Call Summary for Register MCASP_RXMASK

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [1]
- MCASP_CFG Register Summary: [2]
- MCASP_CFG Register Description: [3]

Table 23-634. MCASP_RXFMT

Address Offset	0x0000 0068		
Physical Address	0x4902 8068 0x4012 8068 0x01D2 8068	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The receive bit stream format register (MCASP_RXFMT) configures the receive data format.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														RDATDLY		RRVRS	RPAD			RPBIT				RSSZ				RBUSEL	RROT		

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		RW	0x0000
17:16	RDATDLY	Receive Frame sync delay of AXR[n] 0x0: 0-bit delay. The first receive data bit, AXR[n], occurs in same ACLKR cycle as the receive frame sync (AFSR). 0x1: 1-bit delay. The first receive data bit, AXR[n], occurs one ACLKR cycle after the receive frame sync (AFSR). 0x2: 2-bit delay. The first receive data bit, AXR[n], occurs two ACLKR cycles after the receive frame sync (AFSR). 0x3: Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
15	RRVRS	Receive serial bitstream order 0x0: Bitstream is LSB first. No bit reversal is performed in receive format bit reverse unit. 0x1: Bitstream is MSB first. Bit reversal is performed in receive format bit reverse unit.	RW	0
14:13	RPAD	Pad value for extra bits in slot not belonging to the word. This field only applies to bits when RMASK[n] = 0. 0x0: Pad extra bits with 0. 0x1: Pad extra bits with 1. 0x2: Pad extra bits with one of the bits from the word as specified by RPBIT bits. 0x3: Reserved	RW	0x0
12:8	RPBIT	RPBIT value determines which bit (as read by the CPU from RBUF[n]) is used to pad the extra bits. This field only applies when RPAD = 2h. 0x0: Pad with value of bit RBUFn[0]. 0x01 - 0x1F: Pad with value of the bit positioned within the range RBUFn[31:1].	RW	0x00
7:4	RSSZ	Receive slot size. 0x0 - 0x2 : Reserved 0x3: Slot size is 8 bits 0x4: Reserved 0x5: Slot size is 12 bits 0x6: Reserved 0x7: Slot size is 16 bits 0x8: Reserved 0x9: Slot size is 20 bits 0xA: Reserved 0xB: Slot size is 24 bits 0xC: Reserved 0xD: Slot size is 28 bits 0xE: Reserved 0xF: Slot size is 32 bits	RW	0x0
3	RBUSEL	Selects whether reads from serializer buffer RBUF[n] originate from the peripheral configuration CFG port or the DATA port. 0x0: Reads from XRBUF[n] originate on DATA port. Reads from XRBUF[n] on the peripheral configuration port are ignored. 0x1: Reads from XRBUF[n] originate on peripheral configuration port. Reads from XRBUF[n] on the DATA port are ignored.	RW	0
2:0	RROT	Right-rotation value for receive rotate right format unit. 0x0: Rotate right by 0 (no rotation). 0x1: Rotate right by 4 bit positions. 0x2: Rotate right by 8 bit positions. 0x3: Rotate right by 12 bit positions. 0x4: Rotate right by 16 bit positions. 0x5: Rotate right by 20 bit positions. 0x6: Rotate right by 24 bit positions. 0x7: Rotate right by 28 bit positions.	RW	0x0

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Table 23-635. Register Call Summary for Register MCASP_RXFMT

Multichannel Audio Serial Port

- Frame-Sync Generator: [0]
- Format Units: [1] [2] [3]
- Receive Format Unit: [4] [5]
- TDM Mode Reception Data Alignment Settings: [6]
- State-Machines: [7]
- Time-Division Multiplexed (TDM) Transfer Mode: [8]
- Transfers Through the Data Port (DATA): [9]
- Transfers Through the Configuration Bus (CFG): [10]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [11] [12] [13] [14] [15] [16] [17] [18]
- MCASP_CFG Register Summary: [19] [20]
- MCASP_CFG Register Description: [21]
- MCASP_DATA Register Summary: [22]
- MCASP_DATA Register Description: [23]

Table 23-636. MCASP_RXFMCTL

Address Offset	0x0000 006C		
Physical Address	0x4902 806C 0x4012 806C 0x01D2 806C	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The receive frame sync control register (MCASP_RXFMCTL) configures the receive frame sync (AFSR).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RMOD								RESERVED			FRWID	RESERVED		FSRM	FSRP
R-0																R/W-0								R-0			R/W-0	R-0		R/W-0	R/W-0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		RW	0x0000
15:7	RMOD	Receive frame sync mode select bits. 0x0 - 0x1: Reserved 0x2: 2-slot TDM mode**(I2S receive mode)** 0x3 - 0x20: 3-slot TDM to 32-slot TDM mode 0x21 - 0x17F: Reserved 0x180: 384-slot TDM (external DIR IC inputting 384-slot DIR frames to MCASP) 0x181 - 0x1FF: Reserved	RW	0x000
6:5	RESERVED		RW	0x0
4	FRWID	Receive frame sync width select bit indicates the width of the receive frame sync (AFSR) during its active period. 0x0: Single bit 0x1: Single word	RW	0
3:2	RESERVED		RW	0x0
1	FSRM	Receive frame sync generation select bit. 0x0: Externally-generated receive frame sync 0x1: Internally-generated receive frame sync	RW	0

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Bits	Field Name	Description	Type	Reset
0	FSRP	Receive frame sync polarity select bit. 0x0: A rising edge on receive frame sync (AFSR) indicates the beginning of a frame. 0x1: A falling edge on receive frame sync (AFSR) indicates the beginning of a frame.	RW	0

Table 23-637. Register Call Summary for Register MCASP_RXFMCTL

Multichannel Audio Serial Port

- Frame-Sync Generator: [0] [1] [2] [3] [4] [5] [6]
- Time-Division Multiplexed (TDM) Transfer Mode: [7]
- Special 384-Slot TDM Mode for Connection to External DIR: [8]
- Loopback Mode Configurations: [9]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [10] [11] [12] [13] [14]
- MCASP_CFG Register Summary: [15]
- MCASP_CFG Register Description: [16]

Table 23-638. MCASP_ACLKRCTL

Address Offset	0x0000 0070		
Physical Address	0x4902 8070 0x4012 8070 0x01D2 8070	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The receive clock control register (MCASP_ACLKRCTL) configures the receive bit clock (ACLKR) and the receive clock generator.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CLKRP	RESERVED	CLKRM	CLKRDIV				

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		RW	0x000000
7	CLKRP	Receive bitstream clock polarity select bit. Note that this bitfield does not have any effect, if MCASP_ACLKXCTL[6] ASYNC = 0 0x0: Falling edge. Receiver samples data on the falling edge of the serial clock, so the external transmitter driving this receiver must shift data out on the rising edge of the serial clock. 0x1: Rising edge. Receiver samples data on the rising edge of the serial clock, so the external transmitter driving this receiver must shift data out on the falling edge of the serial clock.	RW	0
6	RESERVED		RW	0
5	CLKRM	Receive bit clock source bit. Note that this bitfield does not have any effect, if MCASP_ACLKXCTL[6] ASYNC = 0 0x0: External receive clock source from ACLKR pin. 0x1: Internal receive clock source from output of programmable bit clock divider.	RW	1

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Bits	Field Name	Description	Type	Reset
4:0	CLKRDIV	Receive bit clock divide ratio bits determine the divide-down ratio from AHCLKR to ACLKR. Note that this bitfield does not have any effect, if MCASP_ACLKXCTL[6] ASYNC = 0. 0x0: Divide-by-1 0x1: Divide-by-2 0x2 - 0x1F: Divide-by-3 to divide-by-32	RW	0x00

Table 23-639. Register Call Summary for Register MCASP_ACLKRCTL

Multichannel Audio Serial Port

- Receive Clock: [0] [1] [2] [3]
- Synchronous and Asynchronous Transmit and Receive Operations: [4]
- Time-Division Multiplexed (TDM) Transfer Mode: [5]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [6] [7] [8] [9] [10] [11]
- MCASP_CFG Register Summary: [12]
- MCASP_CFG Register Description: [13]

Table 23-640. MCASP_AHCLKRCTL

Address Offset	0x0000 0074		
Physical Address	0x4902 8074 0x4012 8074 0x01D2 8074	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The receive high-frequency clock control register (MCASP_AHCLKRCTL) configures the receive high-frequency master clock (AHCLKR) and the receive clock generator.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HCLKRM	HCLKRP	RESERVED						HCLKRDIV							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		RW	0x000
15	HCLKRM	Receive high-frequency clock source bit. 0x0: External receive high-frequency clock source from AHCLKR pin. 0x1: Internal receive high-frequency clock source from output of programmable high clock divider.	RW	1
14	HCLKRP	Receive bitstream high-frequency clock polarity select bit. 0x0: Not inverted. AHCLKR is not inverted before programmable bit clock divider. 0x1: Inverted. AHCLKR is inverted before programmable bit clock divider.	RW	0
13:12	RESERVED		RW	0x0
11:0	HCLKRDIV	Receive high-frequency clock divide ratio bits determine the divide-down ratio from AUXCLK(1) to AHCLKR. 0x0: Divide-by-1 0x1: Divide-by-2 0x2 - 0xFFF: Divide-by-3 to divide-by-4096	RW	0x000

(1) The AUXCLK clock is sourced directly from MCASP_FCLK functional clock input which is tied to the PRCM.MCASP_GFCLK clock.

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Table 23-641. Register Call Summary for Register MCASP_AHCLKRCTL

Multichannel Audio Serial Port

- Receive Clock: [0] [1] [2] [3] [4]
- Time-Division Multiplexed (TDM) Transfer Mode: [5]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [6] [7] [8] [9] [10] [11]
- MCASP_CFG Register Summary: [12]
- MCASP_CFG Register Description: [13]

Table 23-642. MCASP_RXTDM

Address Offset	0x0000 0078		
Physical Address	0x4902 8078 0x4012 8078 0x01D2 8078	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The receive TDM time slot register (MCASP_RXTDM) specifies which TDM time slot the receiver is active.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTDMS[31:0]																															

Bits	Field Name	Description	Type	Reset
31:0	RTDMS[31:0]	Receiver mode during TDM time slot n. 0x0: Receive TDM time slot n is inactive. The receive serializer does not shift in data during this slot. 0x1: Receive TDM time slot n is active. The receive serializer shifts in data during this slot.	RW	0

Table 23-643. Register Call Summary for Register MCASP_RXTDM

Multichannel Audio Serial Port

- TDM Sequencers: [0]
- Time-Division Multiplexed (TDM) Transfer Mode: [1]
- TDM Time Slots Generation and Processing: [2] [3] [4]
- Special 384-Slot TDM Mode for Connection to External DIR: [5]
- Transfers Through the Data Port (DATA): [6]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [7]
- MCASP_CFG Register Summary: [8]
- MCASP_CFG Register Description: [9]

Table 23-644. MCASP_RXSTAT

Address Offset	0x0000 0080		
Physical Address	0x4902 8080 0x4012 8080 0x01D2 8080	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The receiver status register (MCASP_RXSTAT) provides the receiver status and receive TDM time slot number.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RERR	RDMAERR	RSTAFRM	RDATA	RLAST	RTDMSLOT	RCKFAIL	RSYNCERR	ROVRN

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Bits	Field Name	Description	Type	Reset
31:9	RESERVED		RW	0x00 0000
8	RERR	RERR bit always returns a logic-OR of: ROVRN | RSYNCERR | RCKFAIL | RDMAERR Allows a single bit to be checked to determine if a receiver error has occurred. 0x0: No errors have occurred. 0x1: An error has occurred.	RW	0
7	RDMAERR	Receive DMA error flag. RDMAERR is set when the CPU reads more serializers through the DMA port in a given time slot than were programmed as receivers. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0x0: Receive DMA error did not occur. 0x1: Receive DMA error did occur.	RW	0
6	RSTAFRM	Receive start of frame flag. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0x0: No new receive frame sync (AFSR) is detected. 0x1: A new receive frame sync (AFSR) is detected.	RW	0
5	RDATA	Receive data ready flag. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0x0: No new data in RBUF. 0x1: Data is transferred from XRSR to RBUF and ready to be serviced by the CPUs.	RW	0
4	RLAST	Receive last slot flag. RLAST is set along with RDATA, if the current slot is the last slot in a frame. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0x0: Current slot is not the last slot in a frame. 0x1: Current slot is the last slot in a frame. RDATA is also set.	RW	0
3	RTDMSLOT	Returns the LSB of RSLOT. Allows a single read of MCASP_RXSTAT to determine whether the current TDM time slot is even or odd. 0x0: Current TDM time slot is odd. 0x1: Current TDM time slot is even.	RW	0
2	RCKFAIL	Receive clock failure flag. RCKFAIL is set when the receive clock failure detection circuit reports an error. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0x0: Receive clock failure did not occur. 0x1: Receive clock failure did occur.	RW	0
1	RSYNCERR	Unexpected receive frame sync flag. RSYNCERR is set when a new receive frame sync (AFSR) occurs before it is expected. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0x0: Unexpected receive frame sync did not occur. 0x1: Unexpected receive frame sync did occur.	RW	0
0	ROVRN	Receiver overrun flag. ROVRN is set when the receive serializer is instructed to transfer data from XRSR to RBUF, but the former data in RBUF has not yet been read by the CPU. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0x0: Receiver overrun did not occur. 0x1: Receiver overrun did occur.	RW	0

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Table 23-645. Register Call Summary for Register MCASP_RXSTAT

Multichannel Audio Serial Port

- State-Machines: [0]
- Receive Data Ready: [1] [2]
- Using the MPU or DSP for MCASP Servicing: [3]
- Using the DMA for MCASP Servicing: [4]
- Events and Interrupt Requests: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]
- Receive Data Ready Event: [15]
- Error Interrupt: [16] [17]
- Buffer Overrun Error-Receiver: [18]
- DATA Port Error - Receiver: [19] [20] [21]
- Clock Failure Check Startup: [22]
- Receive Clock Failure Check and Recovery: [23]
- Main Sequence – MCASP Polling Reception Method: [24]
- Subsequence – MCASP Receive Error Handling: [25]
- MCASP_CFG Register Summary: [26]
- MCASP_CFG Register Description: [27] [28] [29]

Table 23-646. MCASP_RXTDMSLOT

Address Offset	0x0000 0084		
Physical Address	0x4902 8084 0x4012 8084 0x01D2 8084	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The current receive TDM time slot register (MCASP_RXTDMSLOT) indicates the current time slot for the receive data frame.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RSLOTCNT							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8:0	RSLOTCNT	0x0 - 0x17F: Current receive time slot count. Legal values: 0 to 383 (17Fh). TDM function is not supported for > 32 time slots. However, TDM time slot counter may count to 383 when used to receive a DIR block (transferred over TDM format).	R	0x000

Table 23-647. Register Call Summary for Register MCASP_RXTDMSLOT

Multichannel Audio Serial Port

- MCASP_CFG Register Summary: [0]
- MCASP_CFG Register Description: [1]

Table 23-648. MCASP_RXCLKCHK

Address Offset	0x0000 0088		
Physical Address	0x4902 8088 0x4012 8088 0x01D2 8088	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	The receive clock check control register (RCLKCHK) configures the receive clock failure detection circuit.		
Type	RW		

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RCNT	RMAX	RMIN	RESERVED RPS

Bits	Field Name	Description	Type	Reset
31:24	RCNT	0x0 - 0xFF: Receive clock count value (from previous measurement). The clock circuit continually counts the number of system clocks for every 32 receive high-frequency master clock (AHCLKR) signals, and stores the count in RCNT until the next measurement is taken.	R	0x00
23:16	RMAX	0x00-0xFF: Receive clock maximum boundary. This 8-bit unsigned value sets the maximum allowed boundary for the clock check counter after 32 receive high-frequency master clock (AHCLKR) signals have been received. If the current counter value is greater than RMAX after counting 32 AHCLKR signals, RCKFAIL in MCASP_RXSTAT is set. The comparison is performed using unsigned arithmetic.	RW	0x00
15:8	RMIN	0x00 - 0xFF: Receive clock minimum boundary. This 8-bit unsigned value sets the minimum allowed boundary for the clock check counter after 32 receive high-frequency master clock (AHCLKR) signals have been received. If RCNT is less than RMIN after counting 32 AHCLKR signals, RCKFAIL in RSTAT is set. The comparison is performed using unsigned arithmetic.	RW	0x00
7:4	RESERVED		RW	0x0
3:0	RPS	Receive clock check prescaler value. 0x0: MCASP system clock divided by 1 0x1: MCASP system clock divided by 2 0x2: MCASP system clock divided by 4 0x3: MCASP system clock divided by 8 0x4: MCASP system clock divided by 16 0x5: MCASP system clock divided by 32 0x6: MCASP system clock divided by 64 0x7: MCASP system clock divided by 128 0x8: MCASP system clock divided by 256 0x9 - 0xF: Reserved	RW	0x0

Table 23-649. Register Call Summary for Register MCASP_RXCLKCHK

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Clock Failure Check Startup: [1]
- MCASP_CFG Register Summary: [2]

Table 23-650. MCASP_TXMASK

Address Offset	0x0000 00A4		
Physical Address	0x4902 80A4 0x4012 80A4 0x01D2 80A4	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmit format unit bit mask register - Determines which bits of the transmitted data are masked off before being shifted out the MCASP		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
XMASK[31:0]			

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Bits	Field Name	Description	Type	Reset
31:0	XMASK[31:0]	Transmit data mask enable bit 0x0: The corresponding bit of transmit data is masked out and then transmitted out the MCASP in place of the original bit. 0x1: The corresponding bit of transmit data is transmitted out the MCASP.	RW	0

Table 23-651. Register Call Summary for Register MCASP_TXMASK

Multichannel Audio Serial Port

- Transmit Format Unit: [0]
- DIT Mode Transmission Data Alignment Settings: [1] [2]
- Time-Division Multiplexed (TDM) Transfer Mode: [3]
- Transmit DIT Clock and Frame-Sync Generation: [4]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [5] [6]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [7]
- MCASP_CFG Register Summary: [8]

Table 23-652. MCASP_TXFMT

Address Offset	0x0000 00A8		
Physical Address	0x4902 80A8 0x4012 80A8 0x01D2 80A8	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmit bitstream format register - configures the transmit data format		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														XDATDLY		XRVRS	XPAD			XPBIT				XSSZ				XBUSEL	XROT		

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	RW	0x0000
17:16	XDATDLY	Transmit sync bit delay 0x0: 0 bit delay - The first transmit data bit, on the AXR[n], occurs in the same abemcasp_aclkx cycle as the transmit frame sync (abemcasp_afsx). 0x1: 1-bit delay. The first transmit data bit, AXR[n], occurs one ACLKX cycle after the transmit frame sync (AFSX). 0x2: 2-bit delay. The first transmit data bit, AXR[n], occurs two ACLKX cycles after the transmit frame sync (AFSX). 0x3: Reserved	RW	0x0
15	XRVRS	Transmit serial bitstream order 0x0: Bitstream is LSB first. No bit reversal is performed in transmit format unit. 0x1: Bitstream is MSB first. Bit reversal is performed in transmit format bit reverse unit.	RW	0x0
14:13	XPAD	Pad value for extra bits in slot not belonging to word defined by XMASK. This field only applies to bits when XMASK[n] = 0. 0x0: Pad extra bits with 0. 0x1: Pad extra bits with 1. 0x2: Pad extra bits with one of the bits from the word as specified by XPBIT bits. 0x3: Reserved	RW	0x00

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Bits	Field Name	Description	Type	Reset
12:8	XPBIT	XPBIT value determines which bit (as written by the CPU or DMA to XBUF[n]) is used to pad the extra bits before shifting. This field only applies when XPAD = 0x2. 0x0: Pad with bit 0 value. 0x1 - 0x1F: Pad with bit 1 to bit 31 value.	RW	0x0
7:4	XSSZ	Transmit slot size 0x0 - 0x2 : Reserved 0x3: Slot size is 8 bits 0x4: Reserved 0x5: Slot size is 12 bits 0x6: Reserved 0x7: Slot size is 16 bits 0x8: Reserved 0x9: Slot size is 20 bits 0xA: Reserved 0xB: Slot size is 24 bits 0xC: Reserved 0xD: Slot size is 28 bits 0xE: Reserved 0xF: Slot size is 32 bits.	RW	0x0
3	XBUSEL	Selects whether writes to the serializer buffer XBUF[n] originate from the peripheral configuration CFG port or the DATA port. 0x0: Writes to XBUF[n] originate from the DATA port. Writes to XBUF[n] from the peripheral configuration port are ignored with no effect on the MCASP. 0x1: Writes to XBUF[n] originate from the peripheral configuration port - CFG port. Writes to XBUF[n] from the DATA port are ignored with no effect on the MCASP.	RW	0
2:0	XROT	Right-rotation value for transmit rotate right format unit 0x0: Rotate right by 0 (no rotation). 0x1: Rotate right by 4 bit positions. 0x2: Rotate right by 8 bit positions. 0x3: Rotate right by 12 bit positions. 0x4: Rotate right by 16 bit positions. 0x5: Rotate right by 20 bit positions. 0x6: Rotate right by 24 bit positions. 0x7: Rotate right by 28 bit positions.	RW	0x0

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Table 23-653. Register Call Summary for Register MCASP_TXFMT

Multichannel Audio Serial Port

- Frame-Sync Generator: [0]
- Format Units: [1] [2] [3]
- Transmit Format Unit: [4] [5] [6]
- TDM Mode Transmission Data Alignment Settings: [7]
- DIT Mode Transmission Data Alignment Settings: [8] [9] [10] [11] [12] [13] [14]
- State-Machines: [15]
- Time-Division Multiplexed (TDM) Transfer Mode: [16]
- Transmit DIT Clock and Frame-Sync Generation: [17] [18]
- Transfers Through the Data Port (DATA): [19]
- Transfers Through the Configuration Bus (CFG): [20]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [21] [22] [23] [24]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [25] [26] [27] [28] [29] [30] [31] [32]
- Main Sequence – MCASP DIT- / TDM - Interrupt Transmission Method: [33]
- Main Sequence –MCASP DIT- / TDM - Mode DMA Transmission Method: [34]
- MCASP DIT- / TDM- Transmit Interrupt Events Servicing: [35]
- MCASP_CFG Register Summary: [36] [37]
- MCASP_DATA Register Summary: [38]
- MCASP_DATA Register Description: [39]

Table 23-654. MCASP_TXFMCTL

Address Offset	0x0000 00AC		
Physical Address	0x4902 80AC 0x4012 80AC 0x01D2 80AC	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmit frame-sync control register - configures the transmit frame sync (abemcasp_afsx).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																XMOD								RESERVED			FXWID	RESERVED		FSXM	FSXP

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x0000
15:7	XMOD	Transmit frame-sync mode select bits 0x0 - 0x1: Reserved 0x2: 2-slot TDM mode (**I2S transmit mode**) 0x3 - 0x20: 3-slot TDM to 32-slot TDM mode 0x21 - 0x17F: Reserved 0x180: 384-slot DIT mode All other: Reserved	RW	0x000
6:5	RESERVED	Reserved	RW	0x0
4	FXWID	The transmit frame-sync width select bit indicates the width of the transmit frame sync (abemcasp_afsx) during its active period. 0x0: Single bit 0x1: Single word	RW	0
3:2	RESERVED	Reserved	RW	0x0
1	FSXM	Transmit frame-sync generation select bit 0x0: Externally-generated transmit frame 0x1: Internally-generated transmit frame sync	RW	0

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Bits	Field Name	Description	Type	Reset
0	FSXP	Transmit frame-sync polarity select bit 0x0: Rising Edge - A rising edge on transmit frame sync (abemcasp_afsx) indicates the beginning of a frame. 0x1: A falling edge on transmit frame sync (abemcasp_afsx) indicates the beginning of a frame.	RW	0

Table 23-655. Register Call Summary for Register MCASP_TXFMCTL

Multichannel Audio Serial Port

- Frame-Sync Generator: [0] [1] [2] [3] [4] [5] [6]
- Time-Division Multiplexed (TDM) Transfer Mode: [7]
- Transmit DIT Clock and Frame-Sync Generation: [8] [9]
- Loopback Mode Configurations: [10]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [11] [12]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [13]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [14] [15] [16] [17] [18] [19]
- MCASP_CFG Register Summary: [20]

Table 23-656. MCASP_ACLKXCTL

Address Offset	0x0000 00B0		
Physical Address	0x4902 80B0 0x4012 80B0 0x01D2 80B0	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmit clock control register - Configures the transmit bit clock (abemcasp_aclkx) and the transmit clock generator.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CLKXP	ASYNC	CLKXM	CLKXDIV				

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	RW	0x00
7	CLKXP	Transmit bitstream clock polarity select bit. 0x0: Rising edge. External receiver samples data on the falling edge of the serial clock, so the transmitter must shift data out on the rising edge of the serial clock. 0x1: Falling edge. External receiver samples data on the rising edge of the serial clock, so the transmitter must shift data out on the falling edge of the serial clock.	RW	0
6	ASYNC	Transmit operation asynchronous enable bit 0x0: Synchronous. Transmit clock and frame sync provides the source for both the transmit and receive sections. Note that in this mode, the receive bit clock is an inverted version of the transmit bit clock. 0x1: Asynchronous	RW	1
5	CLKXM	Transmit bit clock source bit 0x0: External transmit clock source from ACLKX pin. 0x1: Internal (output of divider)	RW	1
4:0	CLKXDIV	Transmit bit clock divide ratio bits, determine the divide-down ratio from AHCLKX to ACLKX. 0x0: Divide-by-1 0x1: Divide-by-2 0x2 to 0x1F: Divide-by-3 to divide-by-32	RW	0x00

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Table 23-657. Register Call Summary for Register MCASP_ACLKXCTL

Multichannel Audio Serial Port

- Transmit Clock: [0] [1] [2] [3] [4] [5]
- Receive Clock: [6]
- Frame-Sync Generator: [7] [8]
- Synchronous and Asynchronous Transmit and Receive Operations: [9] [10] [11]
- Time-Division Multiplexed (TDM) Transfer Mode: [12]
- Transmit DIT Clock and Frame-Sync Generation: [13] [14]
- Loopback Modes: [15]
- Loopback Mode Configurations: [16]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [17]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [18] [19] [20] [21] [22]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [23] [24] [25] [26] [27] [28]
- MCASP_CFG Register Summary: [29]
- MCASP_CFG Register Description: [30] [31] [32]

Table 23-658. MCASP_AHCLKXCTL

Address Offset	0x0000 00B4		
Physical Address	0x4902 80B4 0x4012 80B4 0x01D2 80B4	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	High-frequency transmit clock control register - Configures the transmit high-frequency master clock (abemcasp_ahclkx) and the transmit clock generator.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HCLKXM	HCLKXP	RESERVED		HCLKXDIV											

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	RW	0x000
15	HCLKXM	Transmit high-frequency clock source bit 0x0: External transmit high-frequency clock source from AHCLKX pin. 0x1: Internal transmit high-frequency clock source from output of programmable high clock divider	RW	1
14	HCLKXP	Transmit bitstream high-frequency clock polarity select bit. 0x0: Not inverted. AHCLKX is not inverted before programmable bit clock divider. 0x1: Inverted. AHCLKX is inverted before programmable bit clock divider.	RW	0
13:12	RESERVED	Reserved	RW	0x0
11:0	HCLKXDIV	Transmit high-frequency clock divide ratio bits determine the divide-down ratio from AUXCLK to abemcasp_ahclkx.(1) 0x0: Divide-by-1 0x1: Divide-by-2 0x2 to 0xFFF: Divide-by-3 to divide-by-4096	RW	0x000

(1) The AUXCLK clock is sourced directly from MCASP_FCLK functional clock input which is tied to the PRCM.MCASP_GFCLK clock.

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Table 23-659. Register Call Summary for Register MCASP_AHCLKXCTL

Multichannel Audio Serial Port

- Transmit Clock: [0] [1] [2] [3] [4]
- Time-Division Multiplexed (TDM) Transfer Mode: [5]
- Transmit DIT Clock and Frame-Sync Generation: [6]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [7]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [8] [9] [10] [11] [12] [13]
- MCASP_CFG Register Summary: [14]

Table 23-660. MCASP_TXTDM

Address Offset	0x0000 00B8		
Physical Address	0x4902 80B8 0x4012 80B8 0x01D2 80B8	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmit TDM slot 0-31 register - TDM time slot counter range is to 384 slots (to support SPDIF blocks of 384 subframes).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XTDMS[31:0]																															

Bits	Field Name	Description	Type	Reset
31:0	XTDMS[31:0]	Transmitter mode during TDM time slot n 0x0 : Transmit TDM time slot n is inactive. The transmit serializer does not shift out data during this slot. 0x1: The transmit TDM time slot n is active. The transmit serializer shifts out data during this slot according to the serializer control registers - MCASP_XRSRCTLn (where n=0 to 3).	RW	0

Table 23-661. Register Call Summary for Register MCASP_TXTDM

Multichannel Audio Serial Port

- TDM Sequencers: [0] [1]
- Time-Division Multiplexed (TDM) Transfer Mode: [2]
- TDM Time Slots Generation and Processing: [3] [4] [5]
- Transmit DIT Encoding: [6]
- Transmit DIT Clock and Frame-Sync Generation: [7]
- Transfers Through the Data Port (DATA): [8]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [9]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [10]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [11]
- MCASP_CFG Register Summary: [12]

Table 23-662. MCASP_EVTCTLX

Address Offset	0x0000 00BC		
Physical Address	0x4902 80BC 0x4012 80BC 0x01D2 80BC	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmitter Interrupt control register - controls generation of the MCASP transmit interrupt (XINT). When the register bit(s) is set to 1, the occurrence of the enabled MCASP condition(s) generates XINT.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XSTAFRM	RESERVED	XDATA	XLAST	XDMAERR	XCKFAIL	XSYNCERR	XUNDRN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	RW	0x000000
7	XSTAFRM	Transmit start of frame interrupt enable bit 0x0: Interrupt is disabled. A transmit-start-of-frame interrupt does not generate a MCASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit-start-of-frame interrupt generates a MCASP transmit interrupt (XINT).	RW	0
6	RESERVED	Reserved	RW	0
5	XDATA	Transmit data-ready interrupt enable bit 0x0: Interrupt is disabled. A transmit data-ready interrupt does not generate a MCASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit data-ready interrupt generates a MCASP transmit interrupt (XINT).	RW	0
4	XLAST	Transmit last slot interrupt enable bit 0x0: Interrupt is disabled. A transmit-last-slot interrupt does not generate a MCASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit-last-slot interrupt generates a MCASP transmit interrupt (XINT).	RW	0
3	XDMAERR	Transmit DMA error interrupt enable bit 0x0: Interrupt is disabled. A transmit DMA error interrupt does not generate a MCASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit DMA error interrupt generates a MCASP transmit interrupt (XINT).	RW	0
2	XCKFAIL	Transmit clock failure interrupt enable bit 0x0: Interrupt is disabled. A transmit clock failure interrupt does not generate a MCASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmit clock failure interrupt generates a MCASP transmit interrupt (XINT).	RW	0
1	XSYNCERR	Unexpected transmit frame-sync interrupt enable bit 0x0: Interrupt is disabled. An unexpected transmit frame-sync interrupt does not generate a MCASP transmit interrupt (XINT). 0x1: Interrupt is enabled. An unexpected transmit frame-sync interrupt generates a MCASP transmit interrupt (XINT).	RW	0
0	XUNDRN	Transmitter underrun interrupt enable bit 0x0: Interrupt is disabled. A transmitter underrun interrupt does not generate a MCASP transmit interrupt (XINT). 0x1: Interrupt is enabled. A transmitter underrun interrupt generates a MCASP transmit interrupt (XINT).	RW	0

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Table 23-663. Register Call Summary for Register MCASP_EVTCTLX

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Transmit DIT Clock and Frame-Sync Generation: [1]
- Transmit Data Ready: [2]
- Using the MPU or DSP for MCASP Servicing: [3]
- Events and Interrupt Requests: [4] [5] [6] [7] [8] [9] [10] [11]
- Transmit Data Ready Event and Interrupt: [12]
- Error Interrupt: [13]
- Multiple Interrupts: [14] [15]
- Clock Failure Check Startup: [16]
- Transmit Clock Failure Check and Recovery: [17]
- Main Sequence – MCASP DIT- / TDM - Interrupt Transmission Method: [18] [19] [20] [21] [22] [23] [24] [25]
- Main Sequence –MCASP DIT- / TDM - Mode DMA Transmission Method: [26] [27] [28] [29] [30] [31] [32]
- MCASP_CFG Register Summary: [33]
- MCASP_CFG Register Description: [34] [35] [36] [37] [38] [39] [40]

Table 23-664. MCASP_TXSTAT

Address Offset	0x0000 00C0		
Physical Address	0x4902 80C0 0x4012 80C0 0x01D2 80C0	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmitter status register - If the MCASP logic attempts to set an interrupt flag in the same cycle that the CPU writes to the flag to clear it, the MCASP logic has priority and the flag remains set. This also causes the generation of a new interrupt request.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							XERR	XDMAERR	XSTAFRM	XDATA	XLAST	XTDMSLOT	XCKFAIL	XSYNCERR	XUNDRN

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	RW	0x000000
8	XERR	XERR bit always returns a logic-OR of: XUNDRN | XSYNCERR | XCKFAIL | XDMAERR. Allows a single bit to be checked to determine if a transmitter error interrupt has occurred. 0x0: No errors have occurred. 0x1: An error has occurred.	RW	0
7	XDMAERR	Transmit DMA error flag. XDMAERR is set when the CPU or DMA writes more words to the DATA port of the MCASP in a given time slot than it should. Causes a transmit interrupt (XINT) if this bit and XDMAERR in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to it. Writing a 0 has no effect. 0x0: Transmit DMA error did not occur. 0x1: Transmit DMA error occurred.	RW	0
6	XSTAFRM	Transmit start of frame flag. Causes a transmit interrupt (XINT) if this bit and XSTAFRM in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to it. Writing a 0 has no effect. 0x0: No new transmit frame sync (AFSX) is detected. 0x1: A new transmit frame sync (AFSX) is detected.	RW	0

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Bits	Field Name	Description	Type	Reset
5	XDATA	Transmit data ready flag. Causes a transmit interrupt (XINT) if this bit and XDATA in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect 0x0: XBUF[n] is written and is full 0x1: Data is copied from XBUF[n] to XRSR[n]. XBUF[n] is empty and ready to be written. XDATA is also set when the transmit serializers are taken out of reset. When XDATA is set, it always causes a DMA event (AXEVT).	RW	0
4	XLAST	Transmit last slot flag. XLAST, along with XDATA, are set if the current slot is the last slot in a frame. Causes a transmit interrupt (XINT) if this bit and XLAST in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect. 0x0: Current slot is not the last slot in a frame. 0x1: Current slot is the last slot in a frame. XDATA is also set.	RW	0
3	XTDMSLOT	Returns the LSB of XSLOT. Allows a single read of XSTAT to determine whether the current TDM time slot is even or odd. read 0x0: Current TDM time slot is odd. read 0x1: Current TDM time slot is even.	R	0
2	XCKFAIL	Transmit clock failure flag. XCKFAIL is set when the transmit clock failure detection circuit reports an error. Causes a transmit interrupt (XINT) if this bit and XCKFAIL in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect. 0x0: Transmit clock failure did not occur. 0x1: Transmit clock failure occurred	RW	0
1	XSYNCERR	Unexpected transmit frame-sync flag. XSYNCERR is set when a new transmit frame sync (AFSX) occurs before it is expected. Causes a transmit interrupt (XINT) if this bit and XSYNCERR in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect. 0x0: Unexpected transmit frame sync did not occur 0x1: Unexpected transmit frame sync occurred.	RW	0
0	XUNDRN	Transmitter underrun flag. XUNDRN is set when the transmit serializer is instructed to transfer data from XBUF[n] to XRSR[n], but XBUF[n] has not yet been serviced with new data since the last transfer. Causes a transmit interrupt (XINT) if this bit and XUNDRN in MCASP_EVTCTLX are set. This bit is cleared by writing a 1 to iit. Writing a 0 has no effect. 0x0: Transmitter underrun did not occur 0x1: Transmitter underrun occurred.	RW	0

Table 23-665. Register Call Summary for Register MCASP_TXSTAT

Multichannel Audio Serial Port

- State-Machines: [0]
- Transmit Data Ready: [1] [2] [3] [4]
- Using the MPU or DSP for MCASP Servicing: [5]
- Events and Interrupt Requests: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]
- Transmit Data Ready Event and Interrupt: [17] [18]
- Error Interrupt: [19] [20]
- Multiple Interrupts: [21] [22] [23] [24]
- Buffer Underrun Error -Transmitter: [25]
- DATA Port Error - Transmitter: [26] [27] [28]
- Clock Failure Check Startup: [29]
- Transmit Clock Failure Check and Recovery: [30] [31]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [32]
- Main Sequence – MCASP DIT- / TDM - Interrupt Transmission Method: [33]
- MCASP DIT- / TDM- Transmit Interrupt Events Servicing: [34]
- Subsequence – MCASP DIT- / TDM -Modes Transmit Error Handling: [35]
- MCASP_CFG Register Summary: [36]

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Table 23-666. MCASP_TXTDMSLOT

Address Offset	0x0000 00C4		
Physical Address	0x4902 80C4 0x4012 80C4 0x01D2 80C4	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Current transmit TDM time slot register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								XSLOTCNT							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8:0	XSLOTCNT	Current transmit time slot count. the value of this register is 0b101111111 (0x17f) during reset and 0 after reset.	R	0x000

Table 23-667. Register Call Summary for Register MCASP_TXTDMSLOT

Multichannel Audio Serial Port

- TDM Sequencers: [0]
- MCASP_CFG Register Summary: [1]

Table 23-668. MCASP_TXCLKCHK

Address Offset	0x0000 00C8		
Physical Address	0x4902 80C8 0x4012 80C8 0x01D2 80C8	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmit clock check control register - configures the transmit clock failure detection circuit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCNT								XMAX								XMIN								RESERVED				XPS			

Bits	Field Name	Description	Type	Reset
31:24	XCNT	Transmit clock count value (from previous measurement). The clock circuit continually counts the number of system clocks for every 32 transmit high-frequency master clock (abemcasp_ahclkx) signals, and stores the count in XCNT until the next measurement is taken	R	0x00
23:16	XMAX	0x0 to 0xFF: Transmit clock maximum boundary. This 8-bit unsigned value sets the maximum allowed boundary for the clock check counter after 32 transmit high-frequency master clock (abemcasp_ahclkx) signals have been received. If the current counter value is greater than XMAX after counting 32 AHCLKX signals, XCKFAIL in XSTAT is set. The comparison is performed using unsigned arithmetic.	RW	0x00
15:8	XMIN	0x0 to 0xFF: Transmit clock minimum boundary. This 8-bit unsigned value sets the minimum allowed boundary for the clock check counter after 32 transmit high-frequency master clock (abemcasp_ahclkx) signals have been received. If XCNT is less than XMIN after counting 32 AHCLKX signals, XCKFAIL in XSTAT is set. The comparison is performed using unsigned arithmetic.	RW	0x00
7:4	RESERVED	Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
3:0	XPS	Transmit clock check prescaler value 0x0: MCASP system clock divided by 1 0x1: MCASP system clock divided by 2 0x2: MCASP system clock divided by 4 0x3: MCASP system clock divided by 8 0x4: MCASP system clock divided by 16 0x5: MCASP system clock divided by 32 0x6: MCASP system clock divided by 64 0x7: MCASP system clock divided by 128 0x8: MCASP system clock divided by 256 0x9 to 0xF: Reserved	RW	0x0

Table 23-669. Register Call Summary for Register MCASP_TXCLKCHK

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Transmit DIT Clock and Frame-Sync Generation: [1]
- Clock Failure Check Startup: [2]
- Transmit Clock Failure Check and Recovery: [3]
- MCASP_CFG Register Summary: [4]

Table 23-670. MCASP_TXEVTCTL

Address Offset	0x0000 00CC		
Physical Address	0x4902 80CC 0x4012 80CC 0x01D2 80CC	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmitter DMA event control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															XDATDMA

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	RW	0x0000 0000
0	XDATDMA	Transmit data DMA request enable bit. 0x0: The transmit data DMA request is enabled. 0x1: The transmit data DMA request is disabled.	RW	0

Table 23-671. Register Call Summary for Register MCASP_TXEVTCTL

Multichannel Audio Serial Port

- Transmit Data Ready: [0]
- Using the DMA for MCASP Servicing: [1]
- DMA Requests: [2]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [3]
- Main Sequence – MCASP DIT- / TDM - Interrupt Transmission Method: [4]
- Main Sequence –MCASP DIT- / TDM - Mode DMA Transmission Method: [5]
- MCASP_CFG Register Summary: [6]

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Table 23-672. MCASP_DITCSRAi

Address Offset	0x0000 0100 + (0x04*i)		
Physical Address	0x4902 8100 + (0x04*i) 0x4012 8100 + (0x04*i) 0x01D2 8100 + (0x04*i)	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	DIT left channel status register - All six 32-bit registers (I = 0 to 5) can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. Make sure to update the register file before a different set of data needs to be sent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DITCSRAi																															

Bits	Field Name	Description	Type	Reset
31:0	DITCSRAi	Left (even TDM slot) channel status	RW	0x0000 0000

Table 23-673. Register Call Summary for Register MCASP_DITCSRAi

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Transmit DIT Clock and Frame-Sync Generation: [1]
- DIT Channel Status and User Data Register Files: [2]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [3]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [4]
- MCASP_CFG Register Summary: [5]

Table 23-674. MCASP_DITCSRBi

Address Offset	0x0000 0118+ (0x04*i)		
Physical Address	0x4902 8118 + (0x04*i) 0x4012 8118 + (0x04*i) 0x01D2 8118 + (0x04*i)	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	DIT right channel status register - All six 32-bit registers (I = 0 to 5) can store 192 bits of channel status data for a complete block of transmission. The DIT reuses the same data for the next block. Make sure to update the register file before a different set of data needs to be sent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DITCSRBi																															

Bits	Field Name	Description	Type	Reset
31:0	DITCSRBi	Right (odd TDM slot) channel status	RW	0x0000 0000

Table 23-675. Register Call Summary for Register MCASP_DITCSRBi

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Transmit DIT Clock and Frame-Sync Generation: [1]
- DIT Channel Status and User Data Register Files: [2]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [3]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [4]
- MCASP_CFG Register Summary: [5]

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Table 23-676. MCASP_DITUDRAi

Address Offset	0x0000 0130 + (0x04*i)		
Physical Address	0x4902 8130 + (0x04*i) 0x4012 8130 + (0x04*i) 0x01D2 8130 + (0x04*i)	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	DIT left channel user data register - provides the user data of each left channel (even TDM time slot). All six 32-bit registers (I = 0 to 5) can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. Make sure to update the register before a different set of data needs to be sent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DITUDRAi																															

Bits	Field Name	Description	Type	Reset
31:0	DITUDRAi	Left (even TDM slot) user data	RW	0x0000 0000

Table 23-677. Register Call Summary for Register MCASP_DITUDRAi

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Transmit DIT Clock and Frame-Sync Generation: [1]
- DIT Channel Status and User Data Register Files: [2]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [3]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [4]
- MCASP_CFG Register Summary: [5]

Table 23-678. MCASP_DITUDRBi

Address Offset	0x0000 0148+ (0x04*i)		
Physical Address	0x4902 8148 + (0x04*i) 0x4012 8148 + (0x04*i) 0x01D2 8148 + (0x04*i)	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	DIT right user data register - provides the user data of each right channel (odd TDM time slot). All six 32-bit registers (I = 0 to 5) can store 192 bits of user data for a complete block of transmission. The DIT reuses the same data for the next block. Make sure to update the register before a different set of data needs to be sent.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DITUDRBi																															

Bits	Field Name	Description	Type	Reset
31:0	DITUDRBi	Right (odd TDM slot) user data	RW	0x0000 0000

Table 23-679. Register Call Summary for Register MCASP_DITUDRBi

Multichannel Audio Serial Port

- Time-Division Multiplexed (TDM) Transfer Mode: [0]
- Transmit DIT Clock and Frame-Sync Generation: [1]
- DIT Channel Status and User Data Register Files: [2]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [3]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [4]
- MCASP_CFG Register Summary: [5]

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Table 23-680. MCASP_XRSRCTLn

Address Offset	0x0000 0180 + (0x04 * n)		
Physical Address	0x4902 8180 + (0x04*n) 0x4012 8180 + (0x04*n) 0x01D2 8180 + (0x04*n)	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Serializer n control register, (where n=0 to 3 in the device).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										RRDY	XRDY	DISMOD		SRMOD	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	RW	0x0000000
5	RRDY	Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive (2h), RRDY switches from 0 to 1 whenever data is transferred from XRSRn to RBUFn. Read 0x0: Receive buffer (MCASP_RXBUFn) is empty. Read 0x1: Receive buffer (MCASP_RXBUFn) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs.	R	0
4	XRDY	Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit (1h), XRDY switches from 0 to 1 when XSRCLR in GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive (2h) or inactive (0). Read 0x0: The transmit buffer (MCASP_TXBUFn) contains data. Read 0x1: The transmit buffer (MCASP_TXBUFn) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs.	R	0
3:2	DISMOD	Serializer pin drive mode bit. Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive. This field only applies if the pin is configured as a MCASP pin (PFUNC = 0). 0x0: Drive on pin is 3-state. 0x1: Reserved 0x2: Drive on pin is logic low. 0x3: Drive on pin is logic high.	RW	0x0
1:0	SRMOD	Serializer mode bit 0x0:The serializer is inactive 0x1:The serializer is operating in transmit mode. 0x2: The serializer is operating in receive mode. 0x3: Reserved	RW	0x0

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Table 23-681. Register Call Summary for Register MCASP_XRSRCTLn

Multichannel Audio Serial Port

- MCASP Signals: [0]
- Serializers: [1] [2] [3] [4] [5] [6] [7] [8]
- TDM Sequencers: [9]
- Time-Division Multiplexed (TDM) Transfer Mode: [10]
- TDM Time Slots Generation and Processing: [11]
- Transmit DIT Clock and Frame-Sync Generation: [12]
- Transmit Data Ready: [13] [14]
- Receive Data Ready: [15] [16]
- Transfers Through the Data Port (DATA): [17] [18]
- Using the DMA for MCASP Servicing: [19]
- Events and Interrupt Requests: [20]
- Main Sequence – MCASP Global Initialization for DIT-Transmission: [21]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [22]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [23]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [24]
- Main Sequence – MCASP Polling Reception Method: [25]
- MCASP_CFG Register Summary: [26]
- MCASP_CFG Register Description: [27]

Table 23-682. MCASP_TXBUFn

Address Offset	0x0000 0200 + (0x04 * n)		
Physical Address	0x4902 8200 + (0x04*n) 0x4012 8200 + (0x04*n) 0x01D2 8200 + (0x04*n)	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Transmit buffer n (where n= 0 to 3 in the device) - The transmit buffer for the serializer n holds data from the transmit format unit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XBUFn																															

Bits	Field Name	Description	Type	Reset
31:0	XBUFn	Transmit buffer n, (where n=0 to 3)	RW	0x0000 0000

Table 23-683. Register Call Summary for Register MCASP_TXBUFn

Multichannel Audio Serial Port

- Serializers: [0] [1]
- TDM Sequencers: [2]
- Data Transmission and Reception: [3]
- Transmit Data Ready: [4] [5] [6] [7] [8] [9] [10]
- Transfers Through the Configuration Bus (CFG): [11] [12] [13]
- Buffer Underrun Error -Transmitter: [14]
- Main Sequence – MCASP Global Initialization for TDM -Transmission: [15]
- Main Sequence – MCASP DIT- / TDM- Polling Transmission Method: [16]
- MCASP DIT- / TDM- Transmit Interrupt Events Servicing: [17]
- MCASP_CFG Register Summary: [18] [19]
- MCASP_CFG Register Description: [20] [21]

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Table 23-684. MCASP_RXBUFn

Address Offset	0x0000 0280 + (0x04 * n)		
Physical Address	0x4902 8280 + (0x04*n) 0x4012 8280 + (0x04*n) 0x01D2 8280 + (0x04*n)	**Instance**	MCASP_CFG_MAIN_L3 MCASP_CFG_CORTEX-A15 MCASP_CFG_DSP
Description	Receive buffer n (where n= 0 to 3 in the device) - The receive buffer for the serializer n holds data from the receive format unit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBUFn																															

Bits	Field Name	Description	Type	Reset
31:0	RBUFn	Receive Buffer n, (where n=0 to 3)	RW	0x0000 0000

Table 23-685. Register Call Summary for Register MCASP_RXBUFn

Multichannel Audio Serial Port

- Serializers: [0] [1]
- Data Transmission and Reception: [2]
- Receive Data Ready: [3] [4] [5] [6] [7] [8]
- Transfers Through the Configuration Bus (CFG): [9] [10] [11]
- Buffer Overrun Error-Receiver: [12]
- Main Sequence – MCASP Global Initialization for TDM-Reception: [13]
- Main Sequence – MCASP Polling Reception Method: [14]
- MCASP_CFG Register Summary: [15] [16]
- MCASP_CFG Register Description: [17] [18]

23.8.6.2.3 MCASP_DATA Register Summary

Table 23-686 summarizes the MCASP_DATA register mapping.

Table 23-686. MCASP_DATA Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MCASP_DATA Physical Address L3_MAIN Interconnect	MCASP_DATA Physical Address Cortex-A15 Private Access	MCASP_DATA Physical Address DSP Private Access
MCASP_RXBUF	RW	32	0x0000 0000[(1)]	0x4902 A000	0x4012 A000	0x01D2 A000

(1) 0x000 is just an example DATA port offset value. Actually, whatever the offset value is added to 0x_2 A000 base address, it is ignored (don't care) when MPU / DSP perfomrs accesses to XRBUFn RX/TX buffers through the MCASP DATA port.

NOTE: For MCASP XRBUF buffer accesses through the MCASP DATA port, the destination physical address is always the same regardless of current channel index or transfer direction. The MCASP_TXFMT[3] XBUSEL bit must be set to 0b0, to allow write transfers through the DATA port. The MCASP_RXFMT[3] RBUSEL bit must be set to 0b0, to allow read transfers through the DATA port.

NOTE: The MCASP DATA port is exclusively assigned for DMAs / MPU and DSP accesses to the MCASP channels transmit and receive buffer (MPU / DSP only) registers. All other MCASP module registers must be accessed through the MCASP CFG (peripheral) port.

23.8.6.2.4 MCASP_DATA Register Description

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Table 23-687. MCASP_RXBUF

Address Offset	0x0000 0000		
Physical Address	0x4902 A000 0x4012 A000 0x01D2 A000	**Instance**	MCASP_DATA_MAIN_L3 MCASP_DATA_CORTEX-A15 MCASP_DATA_DSP
Description	Through the DATA port , the Host can service all serializers through a single address and the MCASP automatically cycles through the appropriate serializers. For transmit operations through the DATA port, the Host should write to the same DATA port address to service all of the active transmit serializers upon each transmit data ready event. Similarly, for receive operations through the DATA port, the Host should read from the same RBUF DATA port address to service all of the active receive serializers upon each receive data ready event. To enable accesses from the Host to the McASP XRBUF registers through the DATA port, one must clear the XBUSEL/RBUSEL bits to 0 in the respective MCASP_TXFMT /MCASP_RXFMT registers in the MCASP_CFG Memory Map.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXBUF																															

Bits	Field Name	Description	Type	Reset
31:0	RXBUF	Tx or Rx buffer data.	RW	0x0000 0000

Table 23-688. Register Call Summary for Register MCASP_RXBUF

Multichannel Audio Serial Port

- Transfers Through the Configuration Bus (CFG): [0]
- MCASP_DATA Register Summary: [1]

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23.9 MIPI-HSI

This section describes the MIPI high-speed synchronous serial interface (HSI).

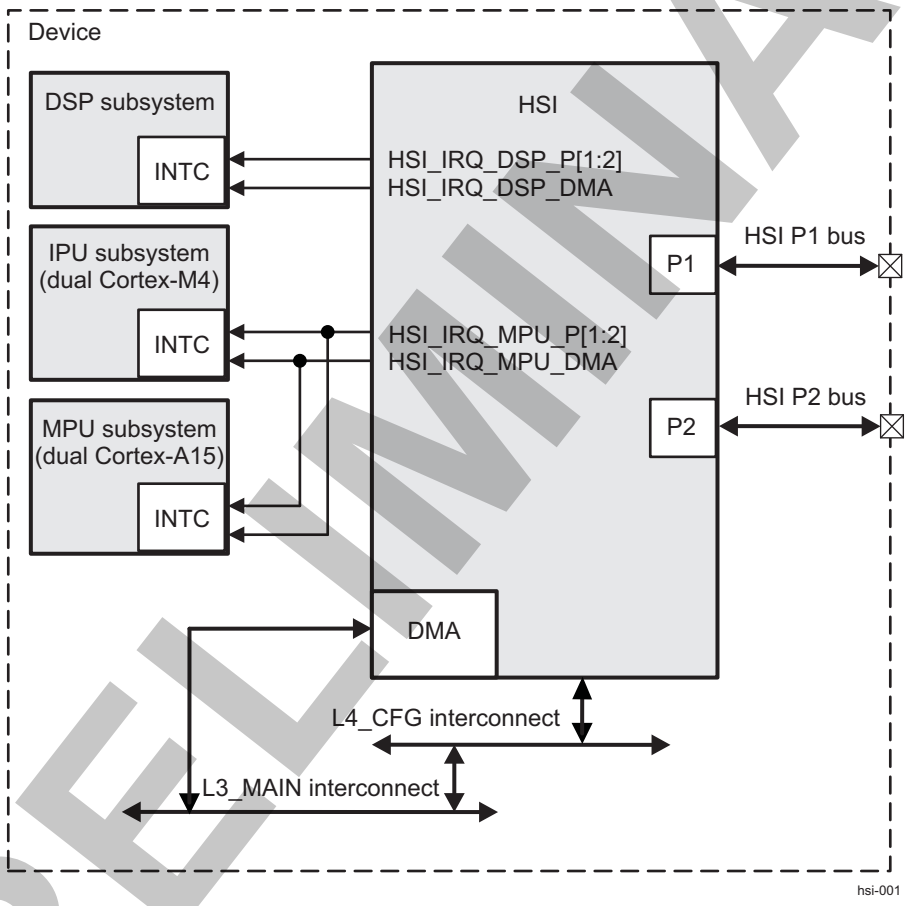
23.9.1 HSI Overview

The MIPI HSI module is a multichannel and full-duplex serial communications interface, composed of two transmitters (HST) in charge of the transmitted information and two receivers (HSR) in charge of the received information, sharing a 16-channel DMA.

The HSI peripheral is typically used to enable the device to exchange information with an external cellular modem.

Figure 23-199 is an overview of the HSI module.

Figure 23-199. HSI Overview



HSI supports the following features:

- Full duplex
- No static clock matching
- Interface speed up to 192 Mbps on transmitter and up to 225 Mbps on receiver
- Transmission speed and operation mode dynamically configurable
- Logical channels:
  - Up to 16 logical channels on receiver
  - Up to 16 logical channels on transmitter
- One 32-request DMA engine:
  - 16 transmit + 16 receive requests from HSI port
  - 16 logical DMA channels

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- Interrupt requests:
  - Three to each processor subsystem (two from HSI port, one from DMA)

23.9.2 HSI Environment

This section describes the HSI application fields from an environment point of view (external connections).

23.9.2.1 HSI Signals

Table 23-689 describes the HSI module I/O signals.

Table 23-689. HSI I/O Signals

Pin Name	I/O[1]	Description	Reset Value[2]
hsi1_cawake	I	HSI port 1 wake-up signal from an external serial transmitter	Hi-Z
hsi1_cadata	I	HSI port 1 receiver data from an external transmitter	Hi-Z
hsi1_caflag	I	HSI port 1 receiver flag from an external transmitter	Hi-Z
hsi1_acready	O	HSI port 1 synchronization signal to an external transmitter	0
hsi1_acwake	O	HSI port 1 wake-up signal to an external serial receiver	0
hsi1_acdata	O	HSI port 1 transmission data (level transmission signaling) to an external receiver	1
hsi1_acflag	O	HSI port 1 transmission flag (bit transition signaling) to an external receiver	1
hsi1_caready	I	HSI port 1 synchronization signal from an external receiver	Hi-Z
hsi2_cawake	I	HSI port 2 wake-up signal from an external serial transmitter	Hi-Z
hsi2_cadata	I	HSI port 2 receiver data from an external transmitter	Hi-Z
hsi2_caflag	I	HSI port 2 receiver flag from an external transmitter	Hi-Z
hsi2_acready	O	HSI port 2 synchronization signal to an external transmitter	0
hsi2_acwake	O	HSI port 2 wake-up signal to an external serial receiver	0
hsi2_acdata	O	HSI port 2 transmission data (level transmission signaling) to an external receiver	1
hsi2_acflag	O	HSI port 2 transmission flag (bit transition signaling) to an external receiver	1
hsi2_caready	I	HSI port 2 synchronization signal from an external receiver	Hi-Z

(1) I = Input; O = Output; I/O = Bidirectional
(2) Hi-Z = High impedance

NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The control module registers assign the specific function to the device pads. For more information on control module settings, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, of *Chapter 18, Control Module*.

23.9.2.2 HSI Typical Application

Figure 23-200 shows the HSI typical application.

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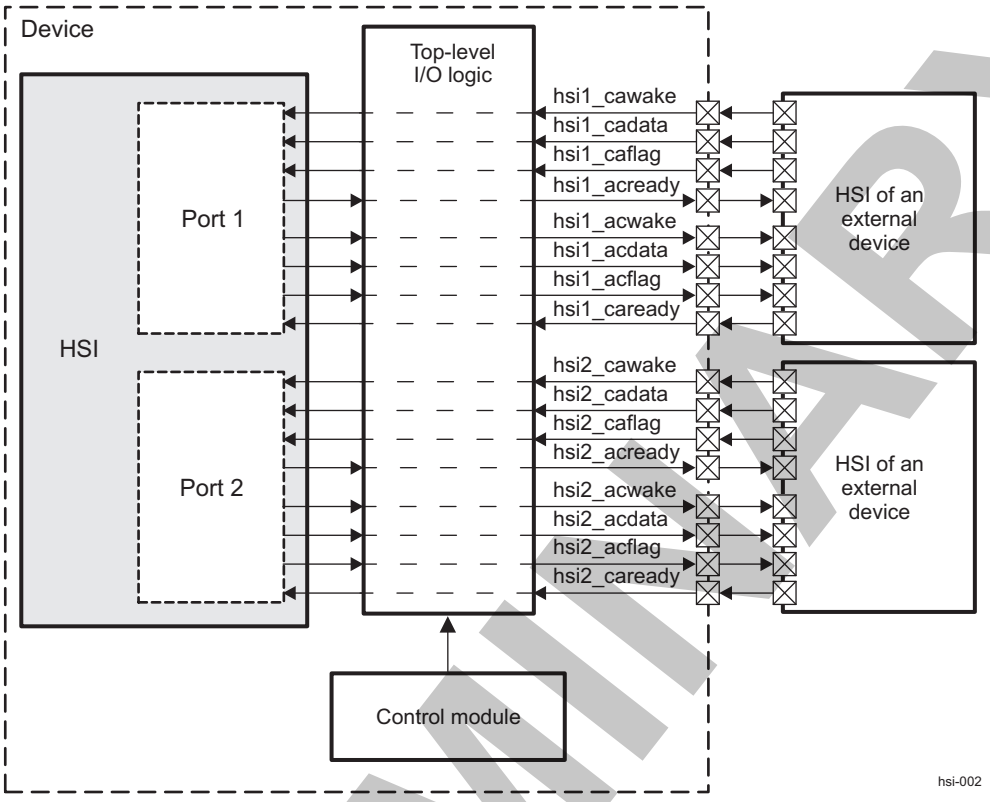
Figure 23-200. HSI Typical Application



23.9.3 HSI Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 23-201 shows the HSI module integration.

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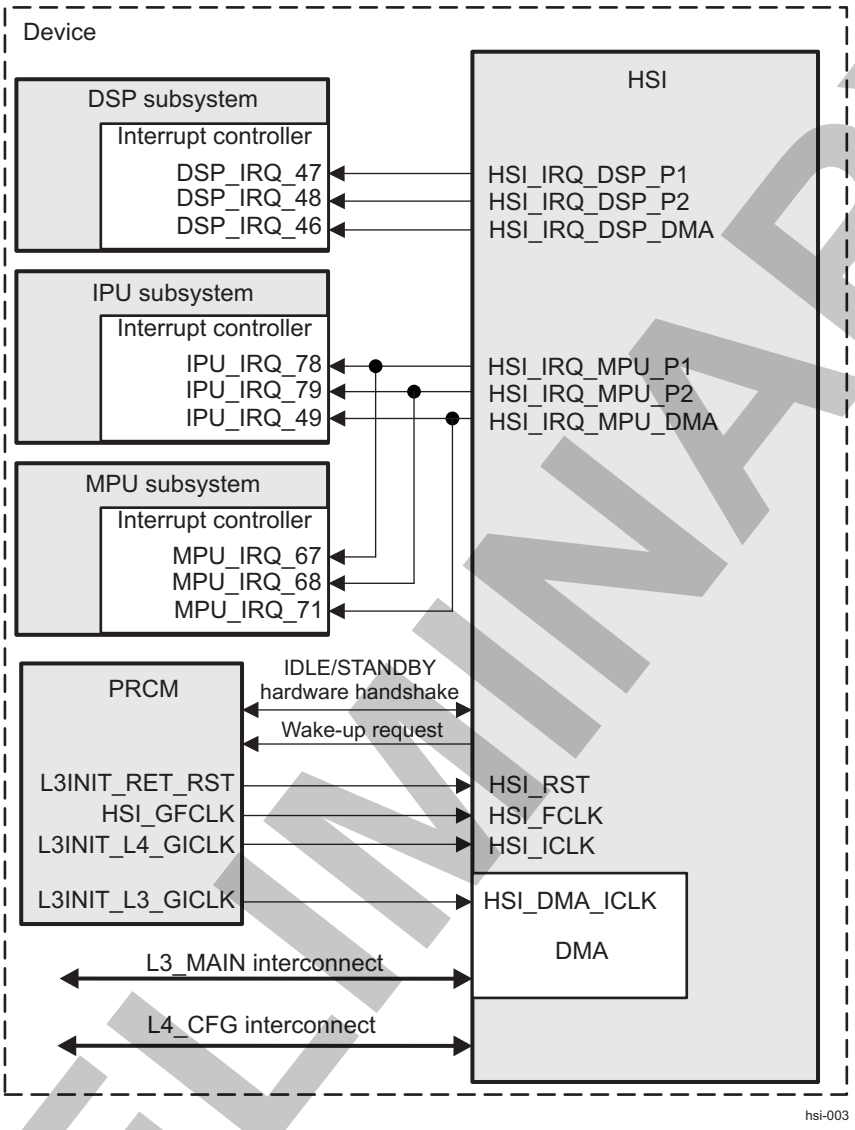
Figure 23-201. HSI Integration



NOTE: For more information about the IDLE/STANDBY hardware handshake and the wake-up request, see Chapter 3, *Power, Reset, and Clock Management*.

Interrupt lines HSI_IRQ_MPU_P[1:2] and HSI_IRQ_MPU_DMA are shared between the INTC_MPU and INTC_IPU. It is strongly recommended to unmask each interrupt source in only one INTC at a time.

Table 23-690 through Table 23-692 summarize the integration of the module in the device.

Table 23-690. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
HSI	PD_L3INIT	NA	L3_MAIN L4_CFG

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Table 23-691. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HSI	HSI_FCLK	HSI_GFCLK	PRCM	HSI module functional clock
	HSI_ICLK	L3INIT_L4_GICLK	PRCM	HSI module interface clock
	HSI_DMA_ICLK	L3INIT_L3_GICLK	PRCM	HSI DMA engine interface clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
HSI	HSI_RST	L3INIT_RET_RST	PRCM	HSI module asynchronous reset

Table 23-692. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
HSI	HSI_IRQ_MPU_DMA[(1)]	IPU_IRQ_49	IPU (dual Cortex-M4)	HSI DMA engine IPU request
	HSI_IRQ_MPU_P1[(1)]	IPU_IRQ_78	IPU	HSI IPU request – Port 1
	HSI_IRQ_MPU_P2[(1)]	IPU_IRQ_79	IPU	HSI IPU request – Port 2
	HSI_IRQ_DSP_DMA	DSP_IRQ_46	DSP	HSI DMA engine DSP request
	HSI_IRQ_DSP_P1	DSP_IRQ_47	DSP	HSI DSP request – Port 1
	HSI_IRQ_DSP_P2	DSP_IRQ_48	DSP	HSI DSP request – Port 2
	HSI_IRQ_MPU_DMA[(1)]	MPU_IRQ_71	MPU (dual Cortex-A15)	HSI DMA engine MPU request
	HSI_IRQ_MPU_P1[(1)]	MPU_IRQ_67	MPU	HSI MPU request – Port 1
	HSI_IRQ_MPU_P2[(1)]	MPU_IRQ_68	MPU	HSI MPU request – Port 2
No DMA Requests				

(1) Interrupts shared between the INTC_MPU and INTC_IPU

NOTE: For a description of interrupt sources, see Section 23.9.4.5, *Interrupt Requests*.

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23.9.4 HSI Functional Description

NOTE: In the functional description section, the following common internal signal names are used for the corresponding external HSI signals (for simplification):

- WAKE: hsi1_cawake, hsi1_acwake, hsi2_cawake, and hsi2_acwake
- DATA: hsi1_cadata, hsi1_acdata, hsi2_cadata, and hsi2_acdata
- FLAG: hsi1_caflag, hsi1_acflag, hsi2_caflag, and hsi2_acflag
- READY: hsi1_acready, hsi1_caready, hsi2_acready, and hsi2_caready

23.9.4.1 Block Diagram

The HSI controller is a subsystem built around two full-duplex multichannel synchronous serial interfaces. It contains a 16-bidirectional-logical-channel DMA in charge of handling data transfers between HSI modules and the L3_MAIN interconnect. Interrupt access to data is also available.

NOTE: Transmit data cannot be read back, and received data cannot be written in DMA and IRQ-based transfers.

Figure 23-202 shows most HSI module features.

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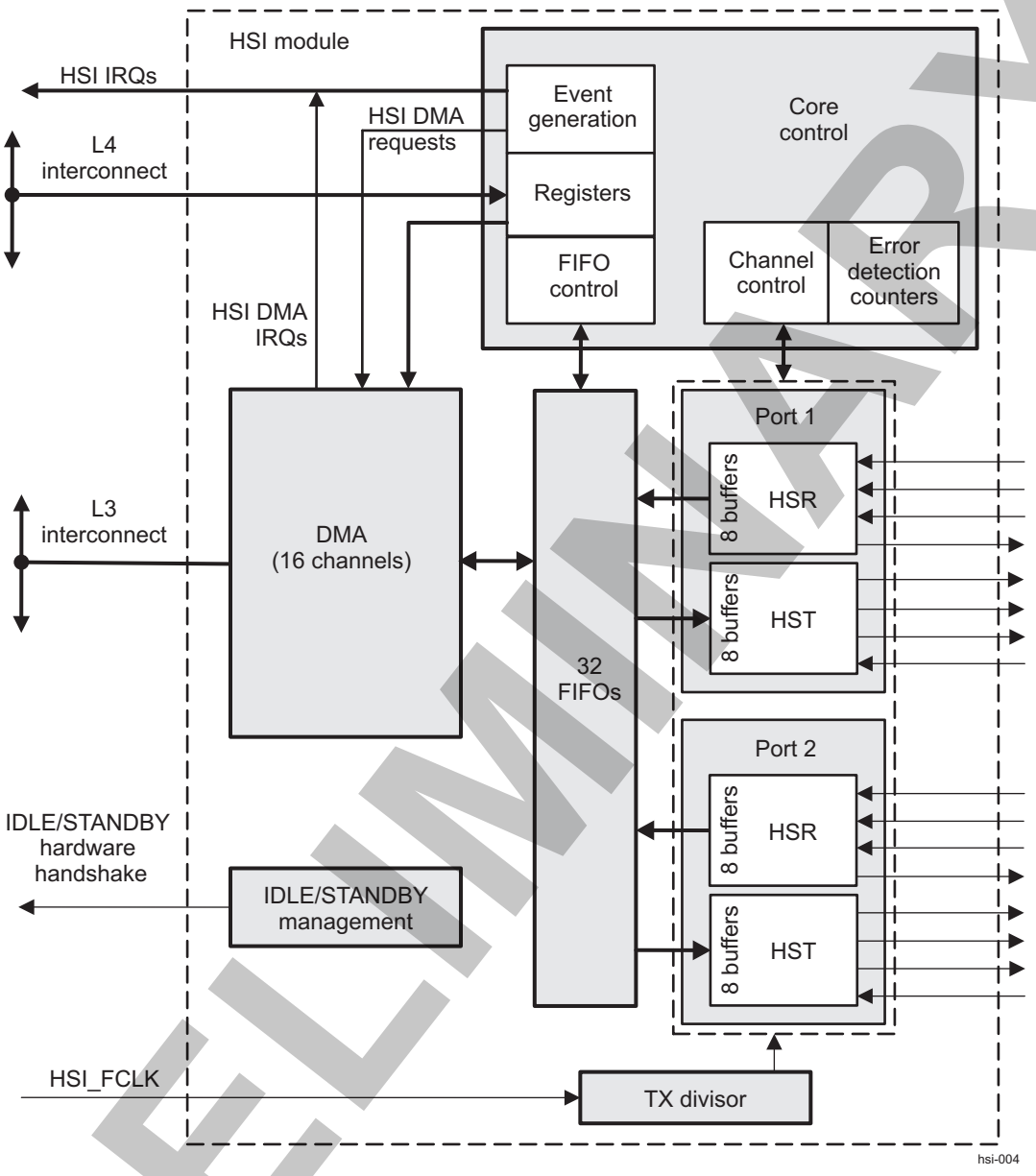
Figure 23-202. HSI Controller Architecture Overview



NOTE: A bypass path in the DMA allows a processor (MPU or DSP) to retrieve or provide data received or to be transmitted on an interrupt triggered access, when the DMA is not enabled.

23.9.4.2 Clock Configuration

The HSI module has four fully asynchronous clock domains:

- Interface clock domain
- Functional clock domain
- Receive clock domain on port 1
- Receive clock domain on port 2

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23.9.4.2.1 Interface Clock Domain

The following clocks are part of the interface clock domain:

- HSI_DMA_ICLK runs the interface master port (L3_MAIN). This clock is used for DMA master access to the L3_MAIN interconnect and also serves as the DMA functional clock.
- HSI_ICLK runs the interface slave port (L4). This clock is used to configure the module and to transmit and receive data through register access in an interrupt-based manner.

23.9.4.2.2 Functional Clock Domain

The functional clock (HSI_FCLK) runs the transmitter/receiver logic.

23.9.4.2.2.1 Transmit Clock

The transmit clock is obtained from the functional clock and is used to generate transmitter DATA and FLAG lines, according to the standard. Namely, the DATA line must always reflect the transmitted bit value, whereas the FLAG line must provide a transition (0 to 1, or 1 to 0) when the current DATA value is the same as the previous one.

The transmit data rate is programmable through the HST_DIVISOR_Pp[7:0] TX_RATE_DIV_VAL bit field.

Transmit clock = HSI_FCLK / (TX_RATE_DIV_VAL + 1).

23.9.4.2.2.2 Receive Error Detection Counters Clocks

The functional clock is also used to obtain clocks for receive error counters, which are independently divided versions of the functional clock. Division is set by software through the HSR_DIVISOR_Pp[7:0] RX_RATE_DIV_VAL bit field, which sets the bit rate clock for the frame time-out counter. This clock is further divided to generate an edge per frame to be sent to the frame burst counter.

23.9.4.2.3 Receive Clock Domain (Port 1 and Port 2)

The RX clock is retrieved from the DATA and FLAG signals available on the serial interface. A self-clocked source synchronous receiver implementation is done as follows: simple XOR of the DATA and FLAG signals recovers a signal displaying a transition on every bit time. From this signal, two clocks are generated with the appropriate phase, which can recover bit values, by sampling the DATA line, where the transmitted bit is always available.

23.9.4.3 Software Reset

The HSI module can be reset by software through the HSI_SYSCONFIG[1] SOFTRESET bit. Setting this bit to 1 enables an active global software reset that is functionally equivalent to a hardware reset. The HSI_SYSSTATUS[0] RESETDONE bit indicates that the software reset is complete when its value is set to 1. Software must ensure that the software reset completes before performing HSI operations.

The DMA engine can be independently reset by software through the DMA_GRST[0] SWRESET bit. Setting this bit to 1 resets the DMA registers and logic. This bit is automatically cleared when the DMA reset completes.

23.9.4.4 Power Management

Table 23-693 describes power-management features available for the HSI module.

NOTE: For descriptions of IdleMode and StandbyMode features, see Chapter 3, *Power, Reset, and Clock Management*.

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Table 23-693. Local Power-Management Features

Feature	Registers	Description
Clock auto gating	HSI_SYSCONFIG[0] AUTOIDLE	This bit allows a local power optimization inside the module by gating the HSI_ICLK clock upon the interface activity.
	DMA_GCR[3] AUTOGATING	This bit allows a local power optimization inside the module by gating the HSI_DMA_ICLK clock upon the interface activity.
Slave idle modes	HSI_SYSCONFIG[4:3] SIDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available.
Master standby modes	HSI_SYSCONFIG[13:12] MIDLEMODE	Force-standby, no-standby, smart-standby, and smart-standby wake-up modes are available.

23.9.4.4.1 HSI Module Power-Management Modes

23.9.4.4.1.1 Standby

When asserted, this signal informs the PRCM module that HSI is quiet and does not generate any traffic on the interconnect.

The HSI module supports four STANDBY handshake modes, selected through the HSI_SYSCONFIG[13:12] MIDLEMODE bit field:

- Force-standby (0x0): Selecting this mode asserts the standby signal unconditionally of the HSI activity. Software must ensure that HSI is disabled and does not generate any activity before activating this mode.
- No-standby (0x1): Standby signal is never asserted.
- Smart-standby (0x2): Standby signal is asserted when internal HSI DMA does not generate activity anymore (namely, upon DMA idle acknowledge signal assertion).
- Smart-standby wakeup (0x3): Standby signal is asserted when internal HSI DMA does not generate activity anymore (namely, upon DMA idle acknowledge signal assertion). It can also generate a wake-up request.

23.9.4.4.1.2 Idle

The PRCM module asserts an IDLE request signal when it requires the HSI slave port to be idled. Any access to this port after the IDLE request signal has been asserted generates an error.

The HSI module supports four IDLE handshake modes, selected through the HSI_SYSCONFIG[4:3] SIDLEMODE bit field:

- Force-idle (0x0): An IDLE request is acknowledged unconditionally.
- No-idle (0x1): An IDLE request is never acknowledged.
- Smart-idle (0x2): Acknowledgment to an IDLE request is given based on the internal HSI module activity.
- Smart-idle wakeup (0x3): Acknowledgment to an IDLE request is given based on the internal HSI module activity. Additionally, when in this mode, the HSI module is allowed to generate a wake-up request.

23.9.4.4.1.3 Auto-Idle

The HSI module provides an auto-idle option for the interface clock domain. Auto-idle mode is enabled by setting the HSI_SYSCONFIG[0] AUTOIDLE and/or DMA_GCR[3] AUTOGATING bits to 1. When this mode is enabled and there is no activity on the interconnect interface, the interface clock is disabled internally to the module to reduce power consumption. When there is new activity on the interconnect interface, the interface clock is restarted without any latency penalty.

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23.9.4.4.1.4 DMA Engine Switch Off Mode

The DMA interface clock (HSI_DMA_ICLK) can be switched off by setting the DMA_GCR[0] SWITCH_OFF bit to 1. DMA clock activity is then cut off. Software must ensure that ongoing transitions are complete before cutting off clocks. Once the DMA is switched off, access to reset this bit is possible only through the configuration port.

23.9.4.5 Interrupt Requests

Table 23-694 lists the event flags, and their mask, that can cause module interrupts.

Table 23-694. Events

Event Flag	Event Mask	Map to	Description
HSI_Pp_M_IRQrU_STATUS[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL	HSI_Pp_M_IRQrU_ENABLE[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Wake detected on any channel 8–15.
HSI_Pp_D_IRQrU_STATUS[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL	HSI_Pp_D_IRQrU_ENABLE[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQrU_STATUS[25] HSR_BREAK	HSI_Pp_M_IRQrU_ENABLE[25] HSR_BREAK	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Break detected on any channel 8–15.
HSI_Pp_D_IRQrU_STATUS[25] HSR_BREAK	HSI_Pp_D_IRQrU_ENABLE[25] HSR_BREAK	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQrU_STATUS[24] HSR_ERROR	HSI_Pp_M_IRQrU_ENABLE[24] HSR_ERROR	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Error detected on any channel 8–15
HSI_Pp_D_IRQrU_STATUS[24] HSR_ERROR	HSI_Pp_D_IRQrU_ENABLE[24] HSR_ERROR	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQrU_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_M_IRQrU_ENABLE[23:16] HSR_OVERRUN_ENI	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Data overrun in real time mode on any channel 8–15
HSI_Pp_D_IRQrU_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_D_IRQrU_ENABLE[23:16] HSR_OVERRUN_ENI	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQrU_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_M_IRQrU_ENABLE[15:8] HSR_AVAILABLE_ENI	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Data received on any channel 8–15
HSI_Pp_D_IRQrU_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_D_IRQrU_ENABLE[15:8] HSR_AVAILABLE_ENI	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQrU_STATUS[7:0] HST_ACCEPTED_CHI	HSI_Pp_M_IRQrU_ENABLE[7:0] HST_ACCEPTED_ENI	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Data transmitted on any channel 8–15
HSI_Pp_D_IRQrU_STATUS[7:0] HST_ACCEPTED_CHI	HSI_Pp_D_IRQrU_ENABLE[7:0] HST_ACCEPTED_ENI	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQr_STATUS[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL	HSI_Pp_M_IRQr_ENABLE[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Wake detected on any channel 0–7
HSI_Pp_D_IRQr_STATUS[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL	HSI_Pp_D_IRQr_ENABLE[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQr_STATUS[25] HSR_BREAK	HSI_Pp_M_IRQr_ENABLE[25] HSR_BREAK	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Break detected on any channel 0–7
HSI_Pp_D_IRQr_STATUS[25] HSR_BREAK	HSI_Pp_D_IRQr_ENABLE[25] HSR_BREAK	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQr_STATUS[24] HSR_ERROR	HSI_Pp_M_IRQr_ENABLE[24] HSR_ERROR	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Error detected on any channel 0–7
HSI_Pp_D_IRQr_STATUS[24] HSR_ERROR	HSI_Pp_D_IRQr_ENABLE[24] HSR_ERROR	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQr_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_M_IRQr_ENABLE[23:16] HSR_OVERRUN_ENI	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Data overrun in real time mode on any channel 0–7
HSI_Pp_D_IRQr_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_D_IRQr_ENABLE[23:16] HSR_OVERRUN_ENI	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	

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Table 23-694. Events (continued)

Event Flag	Event Mask	Map to	Description
HSI_Pp_M_IRQr_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_M_IRQr_ENABLE[15:8] HSR_AVAILABLE_ENI	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Data received on any channel 0–7
HSI_Pp_D_IRQr_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_D_IRQr_ENABLE[15:8] HSR_AVAILABLE_ENI	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_Pp_M_IRQr_STATUS[7:0] HST_ACCEPTED_CHI	HSI_Pp_M_IRQr_ENABLE[7:0] HST_ACCEPTED_ENI	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Data transmitted on any channel 0–7
HSI_Pp_D_IRQr_STATUS[7:0] HST_ACCEPTED_CHI	HSI_Pp_D_IRQr_ENABLE[7:0] HST_ACCEPTED_ENI	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
HSI_DMA_M_IRQSTATUS[15:0] DMA_CHI	HSI_DMA_M_IRQENABLE[15:0] DMA_EN_CHI	HSI_IRQ_MPU_P1 HSI_IRQ_MPU_P2	Channel 0–15 status
HSI_DMA_D_IRQSTATUS[15:0] DMA_CHI	HSI_DMA_D_IRQENABLE[15:0] DMA_EN_CHI	HSI_IRQ_DSP_P1 HSI_IRQ_DSP_P2	
DMA_CSR_CCIR_i[21] BLOCK_IS	DMA_CSR_CCIR_i[5] BLOCK_IE	HSI_IRQ_DSP_DMA HSI_IRQ_MPU_DMA	Block transferred
DMA_CSR_CCIR_i[18] HALF_IS	DMA_CSR_CCIR_i[2] HALF_IE	HSI_IRQ_DSP_DMA HSI_IRQ_MPU_DMA	Half block reached
DMA_CSR_CCIR_i[16] TOUT_IS	DMA_CSR_CCIR_i[0] TOUT_IE	HSI_IRQ_DSP_DMA HSI_IRQ_MPU_DMA	Time-out event

23.9.4.5.1 Interrupts

By default, there are 4 interrupt output lines per HSI port (Mpuirq_0, Mpuirq_1, Dspirq_0, and Dspirq_1), and 2 in case of DMA interrupt (MPU, DSP). The following registers are related to these interrupt outputs:

- Status registers:
  - HSI_Pp_M_IRQrU_STATUS / HSI_Pp_M_IRQr_STATUS for Mpuirq_r (where r = 0 or 1)
  - HSI_Pp_D_IRQrU_STATUS / HSI_Pp_D_IRQr_STATUS for Dspirq_r (where r = 0 or 1)
  - HSI_DMA_M_IRQSTATUS for DMA interrupt to MPU
  - HSI_DMA_D_IRQSTATUS for DMA interrupt to DSP
- Enable registers:
  - HSI_Pp_M_IRQrU_ENABLE / HSI_Pp_M_IRQr_ENABLE for Mpuirq_r (where r = 0 or 1)
  - HSI_Pp_D_IRQrU_ENABLE / HSI_Pp_D_IRQr_ENABLE for Dspirq_r (where r = 0 or 1)
  - HSI_DMA_M_IRQENABLE for DMA interrupt to MPU
  - HSI_DMA_D_IRQENABLE for DMA interrupt to DSP

However, Mpuirq_0 and Mpuirq_1 are further combined (logical OR) into one common interrupt output per port (HSI_P1_MPU_IRQ for port 1, and HSI_P2_MPU_IRQ for port 2). The same goes for Dspirq_0 and Dspirq_1 (HSI_P1_DSP_IRQ for port 1, and HSI_P2_DSP_IRQ for port 2).

This means that it is enough to enable one of the FIFO/WAKE/BREAK/ERROR interrupt events per port (for example, in HSI_Pp_M_IRQ0(U)_ENABLE) for the corresponding interrupt request to be raised. Enabling both HSI_Pp_M_IRQ0(U)_ENABLE and HSI_Pp_M_IRQ1(U)_ENABLE would only mean extra checks and clears (in the corresponding IRQ status register). The same is also valid for the DSP-related IRQ enable/status registers.

The HSI module outputs six interrupt signals (for more information, see Section 23.9.3, *MIPI HSI Integration*). All the interrupts are active-high level-sensitive. Each interrupt line is activated by a set of individual sources. All interrupt sources can individually be enabled and disabled.

For each interrupt, 2 status bits and 2 mask bits are provided, allowing independent masking for the different processors (that is, 1 status bit and 1 mask bit for the MPU [Cortex-A15 or Cortex-M4] interrupts, and 1 status bit and 1 mask bit for the DSP interrupts).

Interrupts in the HSI module are intended to:

- Signal any error condition in reception
- Support the WAKE condition detection

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- Support the BREAK condition detection
- Warn of DMA transfer status or problems
- Signal to processors when to read received data and to write data to transmit

Because DMA has only 16 channels, 16 RX FIFO and 16 TX FIFO are managed by a mix of DMA-driven and interrupt-driven read/write policies.

23.9.4.5.1.1 HSI Interrupt Generation

Five types of interrupt events can be generated by each HSI port:

- Transmit FIFO not full: Occurs when TX FIFO is not full, so data can be written for transmission
- Received data available: Occurs when one data frame has been received and is available on the RX FIFO for reading
- Overrun: Occurs when data overrun is detected on HSI port *p* channel *i*
- Error: Any error defined by the MIPI HSI protocol activates this source of interrupt if this source is enabled.
- Break condition detected: Occurs upon reception of a continuous string of 0s that exceed those possible in any FRAME mode frame (data + header). Because FRAME mode always put a 1 before any frame, the maximum number of 0s occurring during normal transmission is clearly 32 plus the base 2 logarithm of channels used. Hardware works out this number based on register information on channels and receive mode and issues an interrupt if this source is enabled.

All the events are cleared by software, upon setting the corresponding register bit to 1. Setting the bit to 0 has no effect.

23.9.4.5.1.2 DMA Interrupt Generation

Three types of interrupt events can be generated by each DMA channel:

- End of Block: Enabled through the DMA_CSR_CCIR_i[5] BLOCK_IE bit, it occurs when the last element of the transfer has been written into destination. The DMA_CEN_i[15:0] SIZE bit field defines the number of elements in a block.
- Half Block: Enabled through the DMA_CSR_CCIR_i[2] HALF_IE bit, it occurs when a half of the elements have been written into destination.
- Time-out error: Enabled through the DMA_CSR_CCIR_i[0] TOU_IE bit, it occurs when destination slave answers by an error code.

All interrupt events are generated on the same logical channel dedicated interrupt line. When an interrupt is issued by a logical channel, its DMA_CSR_CCIR_i status register is set to record the interrupt cause, if the interrupt event bit is enabled in the relevant DMA_CSR_CCIR_i register. The processor interrupt service routine can read this channel status register to identify the sources of the interrupt. The status bits are automatically cleared after they are read by the processor, unless it is an emulation read.

There are two classes of DMA interrupt events:

- Error events: Errors during the transfer
- Status events: DMA transfer status, such as end of block or half-block

The DMA manages the two classes differently.

For an enabled error event, the following sequence occurs:

1. The appropriate bit in the DMA_CSR_CCIR_i register is set.
2. An interrupt is generated.
3. The ports are released.
4. The currently active logical channel is disabled and must be reprogrammed.
5. Other channels are not affected, and a new channel can get over, according to programmed priorities.

For an enabled status event, the following sequence occurs:

1. The appropriate bit in the DMA_CSR_CCIR_i register is set.

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2. An interrupt is generated.
3. A new interrupt cannot be generated until the status register is read and thereby cleared.

All the events are cleared by software, upon setting the corresponding interrupt status register (HSI_DMA_M_IRQSTATUS or HSI_DMA_D_IRQSTATUS) to 1. Setting the interrupt status register to 0 has no effect.

23.9.4.6 DMA Module

23.9.4.6.1 DMA Overview

The DMA module transfers data between the HSI interfaces and the device on-chip memories. The DMA module supports 16 logical channels and is a dual-port initiator (peripheral port/memory port) with one slave port for configuration. The memory port provides an interface to the memory space and the peripheral port provides an interface to the HSI interfaces. In the HSI controller, the L4_CFG port accesses can be routed directly to the HSI interfaces. This is done by setting the DMA in bypass mode to route the DMA slave port to the DMA peripheral port.

DMA features:

- One target port, for configuration
- 16 logical channels: *n* for transmission and *16-n* for reception
- One initiator port, for transfer to/from memory
- One port to/from LCH memory (this memory holds some registers)
- 32-bit data handling only
- Constant addressing mode on peripheral port/FIFO
- Post-increment addressing mode with burst support on memory port
- Software enabling
- Hardware activation of data transfer on peripheral port
- Logical channels interleaving with only few-cycles-latency
- Fixed allocation of memory and peripheral port to a logical channel
- LCH first-come-first-served + fixed priority arbitration
- Low-power operation (hardware control for clock domains activity)
- Software reset

23.9.4.6.2 DMA Memories

DMA channel register memory is managed by the DMA. Only the DMA interfaces this memory. A processor must program the DMA registers included in this memory.

The DMA has access to 16 dual-port FIFO 8 × 32 bits for reception and 16 dual-port FIFO 8 × 32 bits for transmission. They are provided in the form of two separate memories.

23.9.4.6.3 DMA Basic Operation Outline

DMA write and read operations are helped by tags, to manage possibly disorderly answers. Posted or nonposted operations are possible. In any case, the interconnect always manages them as nonposted. This is consistent with DMA operations that need to know (for example, if main memory write was successful). If not, the error response from L3_MAIN interconnect slave produces a DMA error and the corresponding interrupt. DMA addressing of FIFO memories is always on a constant address, corresponding to 1 of the 16 HST_BUFFER_Pp_CHN_i (or HSR_BUFFER_Pp_CHN_i) registers.

These registers are associated with the 16 FIFOs, and the naming reflects only the reset value of the association FIFO, HSI logical channel. Therefore, at reset, the FIFO addressed on the HSR_BUFFER_P2_CHN_4 register is associated with the fourth logical channel of the second port. Nevertheless, software can change this mapping and associate the same FIFO (for example, to the seventh channel of the first port). This mapping is performed by software through the HST_MAPPINGf[4:1] CH_NUMBER or HSR_MAPPINGf[4:1] CH_NUMBER bit fields.

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23.9.4.6.4 DMA Configuration

Before performing a DMA transfer, the following DMA registers must be configured:

- DMA_CCR_CSDP_i: Sets source and destination parameters and channel control
  - DMA_CCR_CSDP_i[15:14] DST_BURST_EN: Destination burst enable (0x0 and 0x1: single access; 0x2: burst 4 × 32 bits; 0x3: burst 8 × 32 bits)
  - DMA_CCR_CSDP_i[12:9] DST: Transfer destination (0x8: transfer to memory port; 0x9: transfer to peripheral port)
  - DMA_CCR_CSDP_i[8:7] SRC_BURST_EN: Source burst enable (0x0 and 0x1: single access; 0x2: burst 4 × 32 bits; 0x3: burst 8 × 32 bits)
  - DMA_CCR_CSDP_i[5:2] SRC: Transfer source (0x8: transfer from memory port; 0x9: transfer from peripheral port)
  - DMA_CCR_CSDP_i[31:30] DST_ADD_MODE: Destination addressing mode (0x0: constant address mode; 0x1: post-incremented address mode)
  - DMA_CCR_CSDP_i[29:28] SRC_ADD_MODE: Source addressing mode (0x0: constant address mode; 0x1: post-incremented address mode)
- DMA_CSR_CCIR_i: Enables DMA sources of interrupt events
- DMA_CSSA_i[31:0] ADDR: Stores 32 bits of the source address
- DMA_CDSA_i[31:0] ADDR: Stores 32 bits of the destination address
- DMA_CEN_i[31:0] SIZE: Defines the number of elements in a block. The maximum number of elements is 65535.

To start a DMA transfer, the DMA channel to be used must be enabled by setting the DMA_CCR_CSDP_i[23] ENABLE bit to 1. Once the DMA transfer is finished, the DMA_CCR_CSDP_i[23] ENABLE bit is automatically reset by hardware.

The DMA_CDAC_CSAC_i[15:0] ADDRESS_CSAC (or DMA_CDAC_CSAC_i[31:15] ADDRESS_CDAC) bit field can be used to monitor the progress of a DMA transfer on the channel source (or destination). It is a snapshot of the source (or destination) address generated by the channel counter. It is incremented on each access made on channels.

23.9.4.7 HSR Module

The HSR module is the receiver part of the HSI module. It features 16 channels.

23.9.4.7.1 Receive Data

The value on the DATA line is always the transmitted bit, when sampled by the clock recovered. The double level of buffering allows the data to be safely transferred to the FIFO, while a new frame is stored. Data headers do not belong in FIFO and must be decoded to load data on the correct FIFO (there is one logical FIFO per logical channel).

Figure 23-203 shows the receive state-machine implemented in the HSI module.

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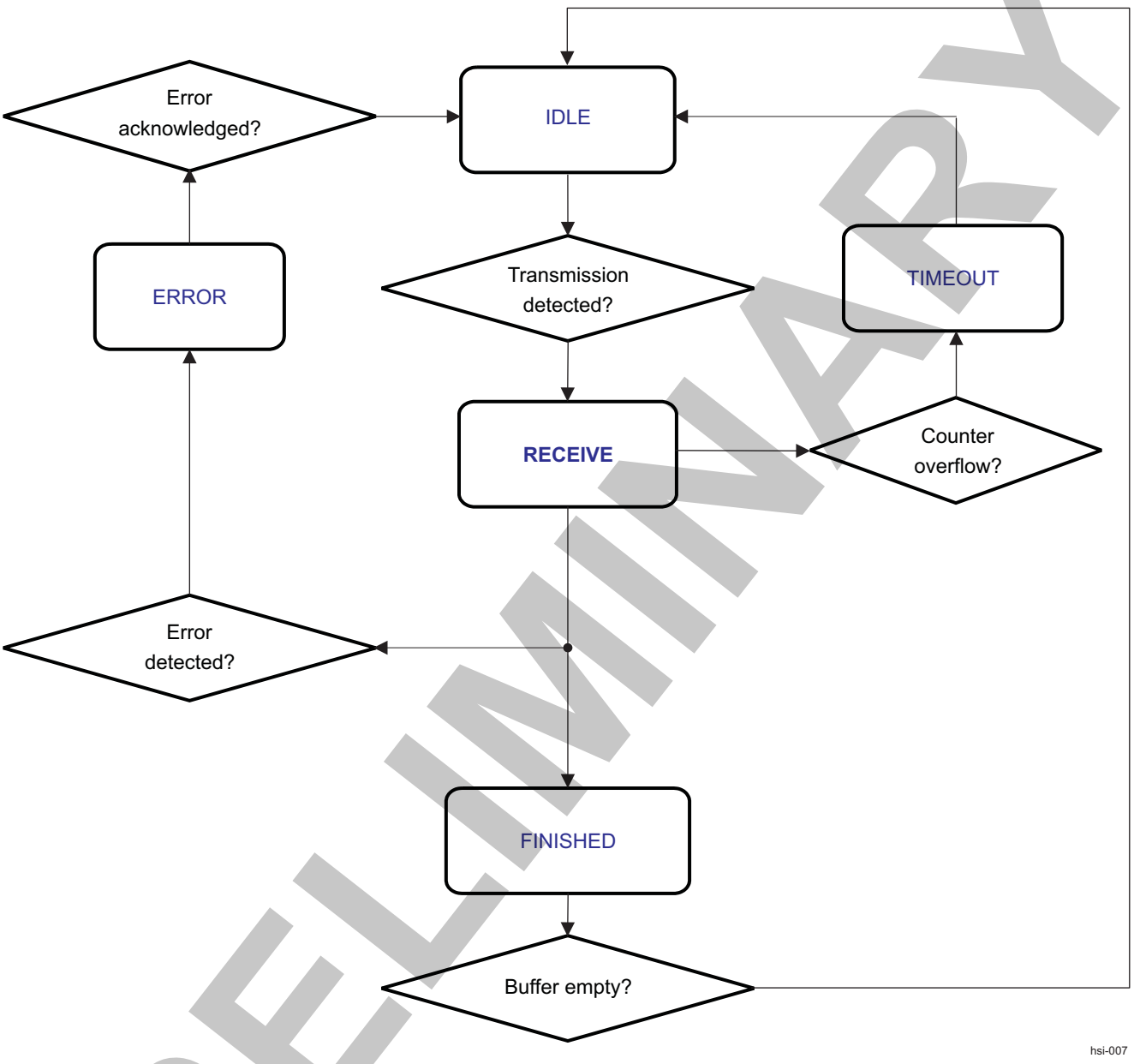
Figure 23-203. Receive FSM



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23.9.4.7.2 Transmission Detection

Reception starts upon two alternate conditions:

- The remote transmitter raises the WAKE line (in this case, it does not actually transmit until the local receiver raises the READY line).
- An activity (in the form of transitions) appears on the FLAG/DATA lines, in case the remote transmitter does not implement the WAKE signal. The receiver must then save and store the received data, at least one frame long, before preventing further transmission by setting READY to 0.

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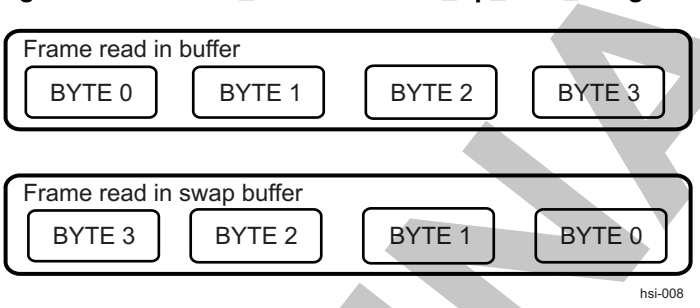
23.9.4.7.3 Receive Buffers

For each logical channel, the HSR_BUFFER_Pp_CHN_i[31:0] DATA bit field holds one frame. The appropriate bit in the HSR_BUFSTATE_Pp register is set to 1 by hardware when the corresponding HSR_BUFFER_Pp_CHN_i register holds one frame. Reading the HSR_BUFFER_Pp_CHN_i[31:0] DATA bit field automatically resets the appropriate bit in HSR_BUFSTATE_Pp. This lets the receiver put another data frame in HSR_BUFFER_Pp_CHN_i, setting again HSR_BUFSTATE_Pp.

Some applications need reversed byte ordering of frames. This is supported by the HSR_SWAPBUFFER_Pp_CHN_i register (see Figure 23-204). By reading this register instead of the corresponding HSR_BUFFER_Pp_CHN_i register on the same channel, byte ordering of the 4 bytes in a frame is reversed.

Figure 23-204. HSR_SWAPBUFFER_Pp_CHN_i Register



Reading the MSB of the HSR_SWAPBUFFER_Pp_CHN_i register sets the corresponding bit of HSR_BUFSTATE_Pp to empty.

NOTE: Read access to the register with 0x3 and 0xF byte-enable removes the receive FIFO-related item. If only 16-bit accesses are used, the upper 2 bytes must be read first (byte-enable 0xC). Between two consecutive 16-bit FIFO-related accesses there cannot be any other FIFO-related OCP access.

23.9.4.7.4 Receive Operations

Logically, the receiver amounts to the receiver shift register, double-buffering and the FSM. The current state of the FSM can be observed and controlled through the HSR_RXSTATE_Pp[2:0] RXSTATEVAL bit field. For the receive FSM, a functional description is shown in Figure 23-203.

The receiver FSM is in IDLE state when no transmission is detected, or the HSR_MODE_Pp[1:0] MODE_VAL bit field = FRAME and no synchronization bit is detected. Otherwise, it stores the first received bit and transitions to RECEIVING state, where it stops until a full frame is received.

Depending on the selected flow control, the READY line may have to go to 0 after the first bit is received.

Upon receiving a full frame, the FSM transitions to FINISHED state. Otherwise, the FSM transitions to TIMEOUT state as soon as a time-out value (if enabled and programmed in the HSR_COUNTERS_Pp[19:0] FT bit field) is reached. Then it moves to IDLE state.

After entering RECEIVED state, the FSM stays there until the received frame is correctly stored and there is room for another frame. At this point, READY is raised and the FSM goes to IDLE state. In pipelined flow, flow control by READY is not operating at each byte, and in real time flow it is never operating. In both cases, the FSM transitions immediately to IDLE, to receive more data. Illegal transitions or flags raised by error counters (see Section 23.9.4.11, *Error Reporting*), move the FSM to ERROR state, and then to HALT, to wait until the error is acknowledged by software, warned by an interrupt. Except for pipelined control flow, the READY output is always 1 in IDLE state and 0 anywhere else. In pipelined mode, the READY signal stays to 1, and is cleared by a condition on buffer full. The FSM state can be controlled by software by writing in the HSR_RXSTATE_Pp[2:0] RXSTATEVAL bit field. This can be useful to recover from an error condition.

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23.9.4.7.5 Receive Exceptions

23.9.4.7.5.1 Break

Remote transmitter can force synchronization by a long enough string of 0s (equal to the number of header + data bits in the frame + 1). In frame mode, this sends an interrupt.

23.9.4.7.5.2 Overrun

An overrun condition is possible during real-time flow, if received data occur when the FSM is in FINISHED state. Whenever this happens, the HSR_OVERRUN_Pp[15:0] OVERRUN_VAL bit field is set for the corresponding logical channel, which in turn generates an interrupt.

An overrun exception is a legacy condition required in previous SSI hardware, where reception without the READY signal had to be supported. In HSI the READY signal always exists, but it cannot be used during real-time flow and the last 8 bits of a frame during pipelined flow. During real-time data flow, overrun can occur at any time. The main goal of using real-time flow is flushing FIFOs after an error. In that case, an overrun interrupt does not seem worth to be raised. Data does not have to be discarded. The real-time data are discarded if the receiver cannot follow the transmission rate, otherwise, the real-time data is kept in FIFO.

23.9.4.7.5.3 Errors

Several sources of errors are possible. In any of them, the receiver FSM stays in ERROR state until the error interrupt is acknowledged by writing the HSR_ERRORACK_Pp registers. Sources of errors include receive FRAME TIMEOUT, other receive errors flagged by error counters, and any other abnormal condition, as explained in Section 23.9.4.11, *Error Reporting*.

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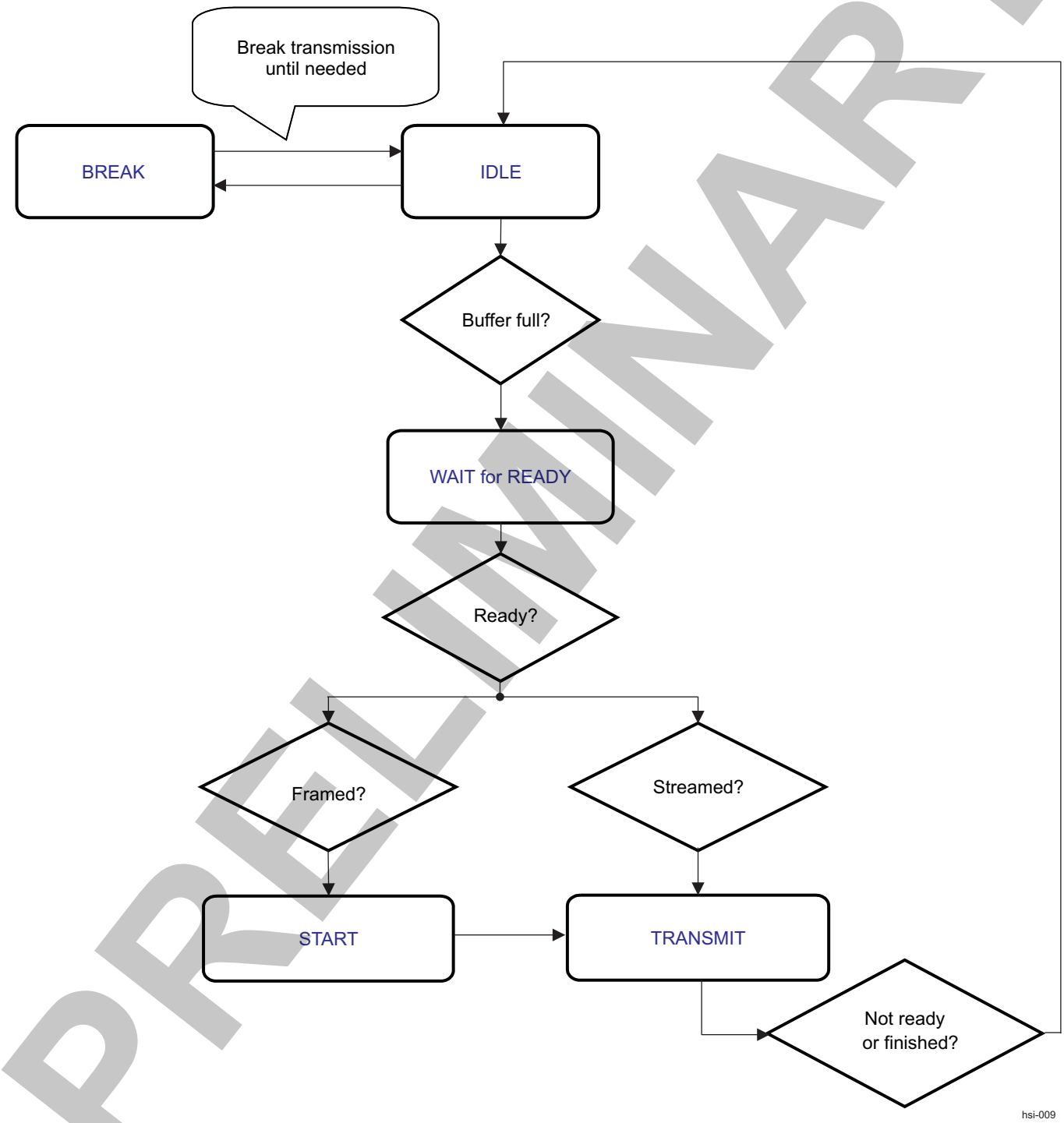
23.9.4.8 HST Block

The HST block is the transmitter part of the HSI module. It features 16 channels.

Figure 23-205 shows the receive state-machine implemented in the HSI module.

Figure 23-205. Transmit FSM



23.9.4.8.1 Configuration

Configuration of the component is expressed in terms of operation mode, number of logical channels, bit rate divisor, and arbitration mode.

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23.9.4.8.1.1 Mode Register

The HST_MODE_Pp register cannot be changed without stopping the link.

There is one HST_MODE_Pp[3:2] FLOW_VAL bit field for each active transmit channel and another HSR_MODE_Pp[3:2] FLOW_VAL bit field for each active receive channel. The local transmitter (communicating with the remote receiver) uses the HST_MODE_Pp[3:2] FLOW_VAL bit field for interpretation of the received READY line, for example to signal errors.

The HST_MODE_Pp register has the following bit fields:

- WAKE_CTRL selects between software (when 0x0) or automatic (when 0x1) control for the WAKE line. The default is software control.
- MODE_VAL defines the following operation modes:
  - Sleep: Specifies whether internal clocks must run and port be operating
  - Stream: Receiver does not use start-bits.
  - Frame: Allows break transmission/reception defined as a longer-than-frame 0 sequence
- FLOW_VAL defines the following data flows:
  - Synchronized flow: The READY signal from the receiver drops after every first frame bit, rising when data are stored, and transmission of a new frame is possible.
  - Pipelined flow: The receiver cannot drop the READY line at some times.
  - Real-time flow: The receiver drops the READY line at the first received bit and raises it at the last one.

NOTE: READY is activated when the module is going into active state (stream or frame mode). The receive mode must be selected at the end of module's configuration, because activates the transfer from the remote side. This will prevent the device from wrong received data, lost of data, fake start of communication.

23.9.4.8.1.2 Other Registers

- The HST_FRAMESIZE_Pp register is kept to offer legacy compatibility. It is a read-only register, returning 0x1F.
- The HST_DIVISOR_Pp[7:0] RX_RATE_DIV_VAL bit field sets the transmission bit rate, with 1 transmitted bit per clock cycle. Bit rate can be changed by software at any time.
- The HST_CHANNELS_Pp[4:0] CHAN_NUM_VAL bit field sets the number of logical channels. It must be a power of 2. The default value is 0x1. This corresponds to only one logical channel, always the same, and in that case, a header is not transmitted; It cannot be changed without stopping the link.
- HST_MAPPINGf contains important settings for each FIFO (one register per FIFO):
  - HST_MAPPINGf[0] ENABLE bit: FIFO is enabled or not.
  - HST_MAPPINGf[4:1] CH_NUMBER and HSR_MAPPINGf[7] PORT_NUMBER bit fields (channel number and port number): FIFO is assigned to an HSI logical channel on a physical port.
  - HST_MAPPINGf[13:10] THRESHOLD bit field is the number of empty TX FIFO locations that will activate interrupt automatically.
- The HST_ARBMODE_Pp[0] ARB_VAL bit allows choosing of the arbitration policy for time allocation to logical channels, when several channels have to transmit. Round-robin algorithm implements a circular scan: the same channel cannot transmit twice if another channel is ready to transmit. Scan proceeds in the same, unspecified direction (design choice). Fixed priority algorithm grants maximum priority to logical channel 0, minimum priority to channel 15. The right to transmit is assigned to the higher priority channel ready to transmit, independently of previous transmissions.

  The choice between algorithms must consider that round-robin sets a maximum wait time for each channel, but it may require a long time to transmit long sequences of frames, on any channel. On the other hand, fixed priority allows limiting of transmission time for high priority channels, while low priority channel may wait for a long time.

  It is important to understand that this register sets the allocation of one port resource (transmission lines) from 2 to 16 vying transmit FIFOs. Allocation of the 16 transmit FIFOs to 32 logical channels is

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done by the HST_MAPPINGf register. For this second kind of allocation, no arbitration makes sense, because software is in charge to ensure against more that 16 logical channels transmitting at the same time.

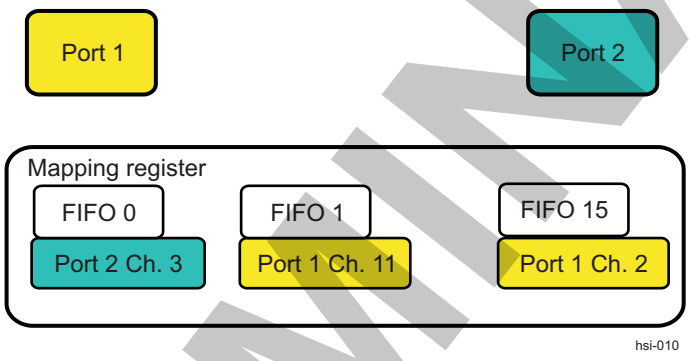
23.9.4.8.2 Mapping

Figure 23-206 shows an example of programming the HST_MAPPINGf register. No limitation is set on the choice of channel/FIFO/port association.

Each port has its HST_ARBMODE_Pp register so that it is also possible to program alternate algorithms on ports.

While the HST_MAPPINGf register cares only about FIFO, the HST_ARBMODE_Pp register is associated to a port and each port has its own one, which only selects a winner between ready-to-transmit channels of this port. For example, suppose that in Figure 23-206 only the three represented channels need to transmit; then a yellow (Port 1) arbiter chooses between channel 11 and channel 2, while the cyan (Port 2) arbiter has no decision to take and lets channel 3 transmit.

Figure 23-206. MAPPING Register



23.9.4.8.3 Transmission Buffer

The transmission buffer holds a frame to be transmitted for each channel. The HST_BUFSTATE_Pp[7:0] BUFSTATE_VAL bit field indicates whether the HST_BUFFER_Pp_CHN_i[31:0] DATA bit field holds significant data, and it is not be cleared until transmit FSM is in IDLE state and arbitration indicates the channel is the next in line to transmit. The HST_BUFSTATE_Pp register is automatically written by hardware.

NOTE: Write access to the register with 0x3 and 0xF byte-enable loads its value into the transmit FIFO. If only 16-bit accesses are used, the upper 2 bytes must be written first (byte-enable 0xC). Between two consecutive 16-bit FIFO-related accesses there cannot be any other FIFO-related OCP access.

Some applications need reversed byte ordering of frames. This is supported by the HST_SWAPBUFFER_Pp_CHN_i register. By reading this register instead of the corresponding HST_BUFFER_Pp_CHN_i register on the same channel, byte ordering of the 4 bytes in a frame is reversed (see Section 23.9.4.7.3, *Receive Buffers*).

23.9.4.8.4 Break Pattern Transmission

Break pattern transmission is an alternative to normal transmission mode, and is used when trying to recover lost synchronization. It is started by software by setting the HST_BREAK_Pp[0] BREAK_VAL bit. As soon as transmit FSM is in IDLE state (ready to accept another frame for transmission), a nonzero value on the HST_BREAK_Pp[0] BREAK_VAL bit starts the BREAK sequence, and automatically clears the HST_BREAK_Pp[0] BREAK_VAL bit. A sequence of 0, longer than a frame, is transmitted.

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23.9.4.8.5 Transmission Operations

The transmitter adds up to the transmit shift register, loaded from the transmission buffer, and the transmit FSM current state of the FSM can be observed and controlled through the HST_TXSTATE_Pp[2:0] TXSTATEVAL bit field. A functional description of the transmit FSM is shown in Figure 23-205.

After reset, the transmitter is in IDLE state. It starts transmission when there is data in one of the transmission HST_BUFFER_Pp_CHN_i registers, depending on the value of HST_BUFSTATE_Pp[7:0] BUFSTATE_VAL bit field, or when the value of BREAK is not 0.

When transmitting a data frame (not a BREAK sequence), the frame to be transmitted is clocked from the HST_BUFFER_Pp_CHN_i register to the transmission shift register, and the FSM enters WAIT state until it receives READY = 1. At this point, it starts driving the DATA and FLAG lines with a preliminary start-bit at 1, if in STREAM mode, or with the frame, which amounts to header and payload data.

In case of synchronized data flow, the TRANSMIT state is left after one frame is transmitted, because READY always drops after the first transmitted bit. Transmit FSM transitions through IDLE and WAIT states before retransmitting, when READY rises.

In case of pipelined data flow, transmit FSM remains in TRANSMIT state as long as READY = 1, and transmission goes on, always clocking data from the appropriate HST_BUFFER_Pp_CHN_i register, as selected by arbitration. Transmission is stopped by the condition READY = 0, forcing FSM to go into IDLE state. READY must not switch during the last 8 nominal bit times.

23.9.4.8.6 Transmission Exceptions

There are no transmission errors. Reception of READY = 0 in the last 8 bits of frames is not flagged. The DATA ACCEPTED interrupt is used to inform software that the HST_BUFFER_Pp_CHN_i[31:0] DATA bit field is empty and to request more data.

23.9.4.9 HSI Wake Generator

The WAKE line is used to create a wake-up event for the external module that interfaces with HSI before a data transfer through the HSI serial interface.

The 16 bits (1 per HSI channel) of the HSI_Pp_WAKE[15:0] WAKE_CHI bit field are ORed together to drive the WAKE line, as shown in Figure 23-207.

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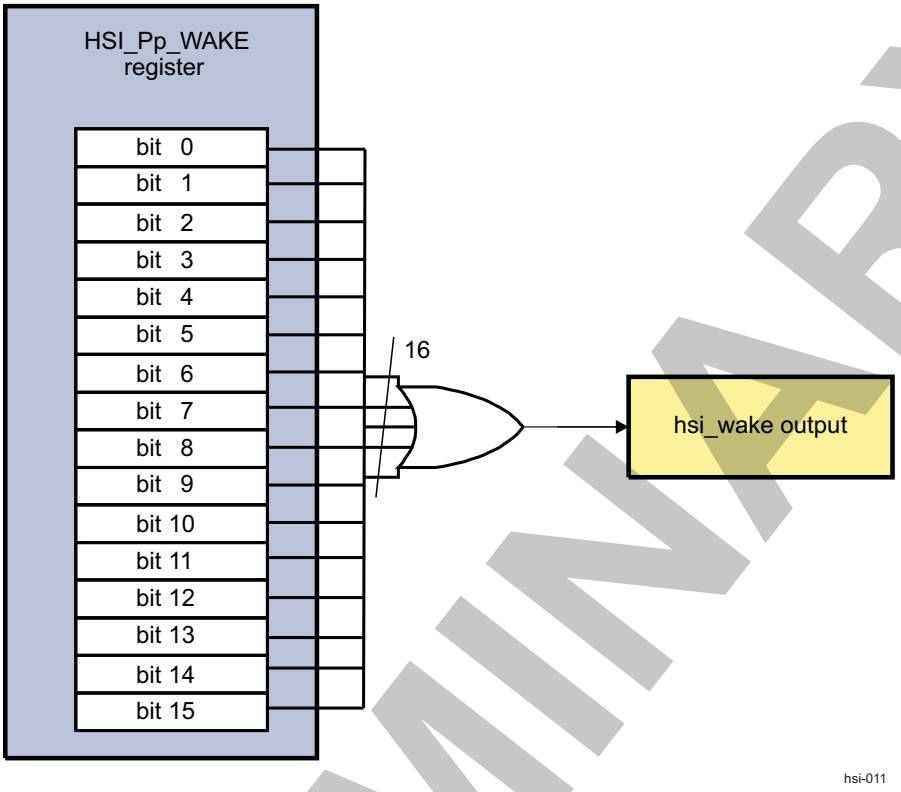
Figure 23-207. HSI_Pp_WAKE Control in Case of Managed Wake



The wake generator can be managed by software operations or automatically by hardware. If the wake generator is not managed, the WAKE signal is driven to 0 and the remote transmitter must wake itself upon activity detection on the DATA and FLAG lines.

23.9.4.9.1 Software Management of HSI Wake Generator

Software can get the responsibility to use and manage those bits to create and release wake-up events consistently with HSI use.

Because the HSI_Pp_WAKE[15:0] WAKE_CHI bit field can be managed by different threads/processors, this mechanism allows independent bit management by each thread. Without locking the HSI_Pp_WAKE register (as a read-modify-write does), it avoids one thread to overwrite the register change made by another thread. Each bit of the HSI_Pp_SET_WAKE[15:0] HSI_SET_WAKE_CHI bit field is owned by one thread at a time.

- The thread can set this bit by setting the corresponding bit of the HSI_Pp_SET_WAKE[15:0] HSI_SET_WAKE_CHI bit field to 1. This sets only this bit, thus leaving the other bits unchanged (no need of a read-modify-write).
- The thread can clear this bit by setting the corresponding bit of the HSI_Pp_CLEAR_WAKE[16:0] HSI_HSI_CLEAR_WAKE_CHI bit field to 1. This clears only this bit, thus leaving the other bits unchanged (no need of a read-modify-write).

23.9.4.9.2 Automatic Management of HSI Wake Generator

The wake generator is automatically managed when there is a transmission to be performed. When data are waiting for transmission in a FIFO TX, the hardware sets the corresponding bit of the HSI_Pp_WAKE[15:0] WAKE_CHI bit field, and this raises the WAKE signal on port *p*. Then WAKE is deasserted by the first occurrence of one event between a fixed time-out from the end of the last transfer, a transition to IDLE in idle-req protocol, a software clear of register.

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23.9.4.10 FIFO Subsystem

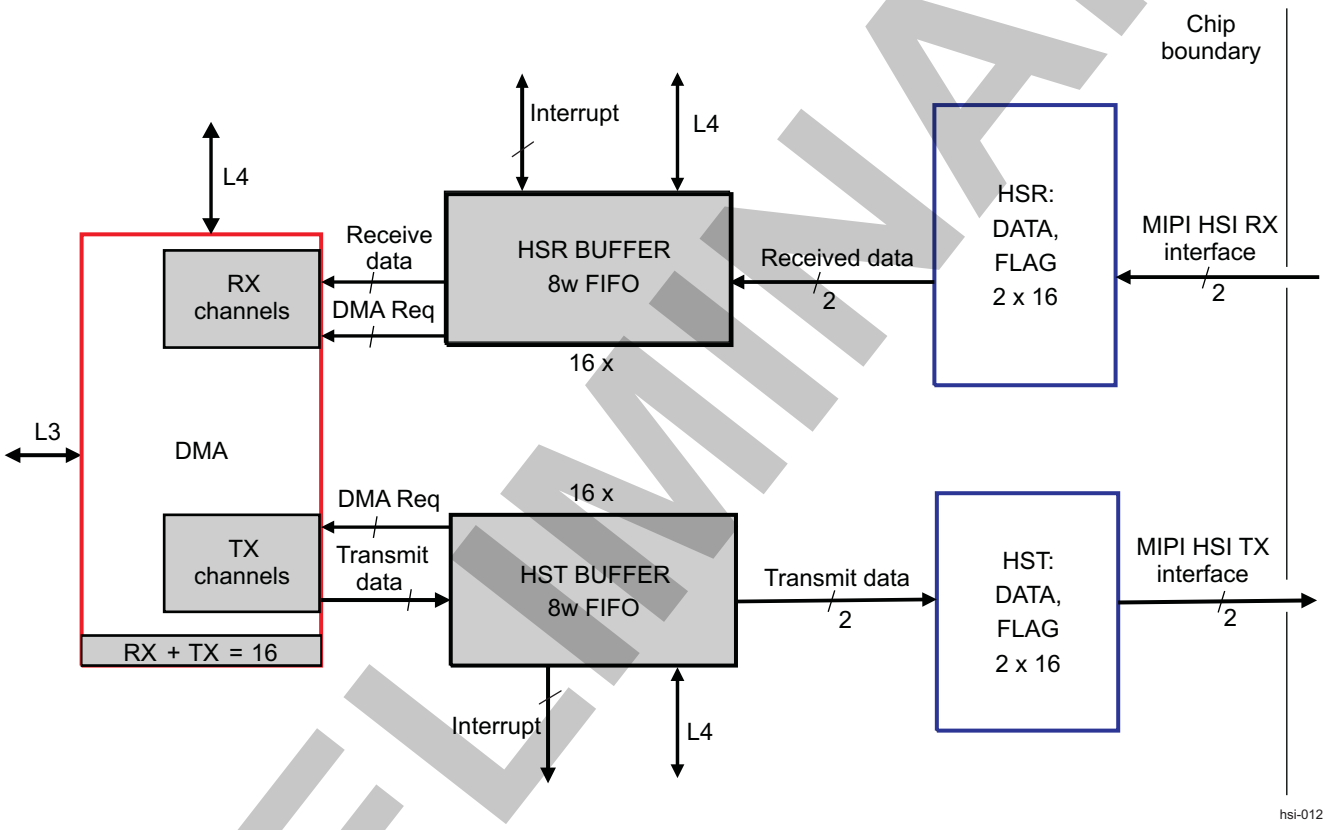
The FIFO subsystem allows temporary buffering while receive data is transferred from the receiver through DMA or the L4 interconnect to main memory, and the storing of transmit data read in main memory through DMA (or written by L4) before transmitting it. The FIFO depth is 8 × 32-bit words for each channel, yielding a total size of 1 KiB with 16 bidirectional channels.

RX FIFOs are clocked by interconnect clock, TX FIFOs are clocked by undivided functional clock.

23.9.4.10.1 FIFO Subsystem Architecture

Figure 23-208 shows the overall FIFO architecture.

Figure 23-208. Overall FIFO Architecture



There are 16 DMA channels available. They can be used for RX or TX in any combination; direction is programmable.

There are 16 RX FIFOs and 16 TX FIFOs. Not all FIFOs can be served by DMA, but all RX FIFOs (or else TX FIFOs) can be served by DMA, if needed. The other FIFOs, if used, must be read/written through the L4_CFG interconnect.

Both HSI ports provide up to 16 × 2 logical channels. This means that only one half of the HSI logical channels can be accommodated on the existing FIFOs. The others must not be used, and their use must flag an error. The 16 HST_MAPPINGf or HSR_MAPPINGf registers specify which HSI logical channel number is allowed to be received on RX FIFOs and/or fed for transmission by TX FIFOs. There is one mapping register for transmission and one for reception. Any attempt to transmit or process received data on HSI logical channels not previously mapped on mapping registers results in an error. In other words, some header values (bits 35 to 32) are not allowed at any given time, and generate an error when received. Software must ensure that the remote side sends payload on the allowed logical channels, specified by header values.

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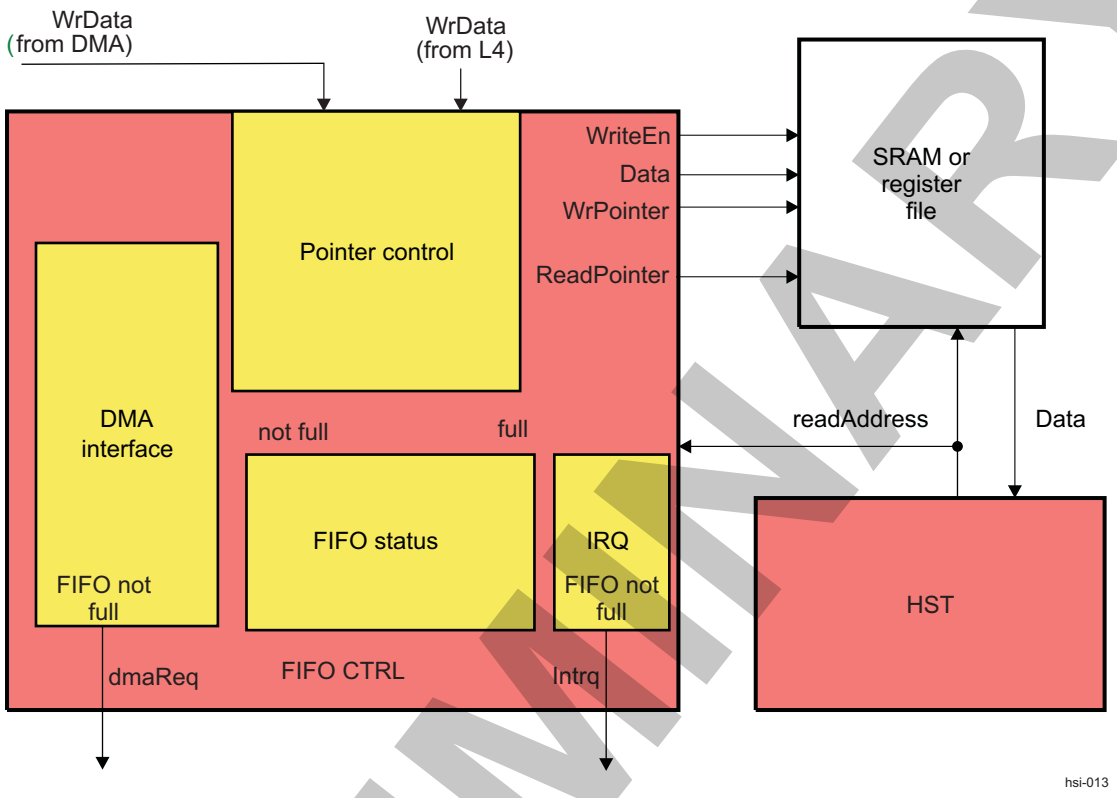
23.9.4.10.2 Transmit FIFO Architecture

Figure 23-209 shows the transmission FIFO architecture.

Figure 23-209. Transmission FIFO Architecture



The FIFO controller flags the condition of "room available in FIFO" or "FIFO not full" at any time when FIFO can host new data for transmission. This condition raises an interrupt request and a DMA request, if enabled. A programmable threshold in the corresponding HST_MAPPINGf[13:10] THRESHOLD bit field reduces the number of requests (they can be sent only when four words can be written in FIFO). The default value for the threshold is 0x0 (that is, a request rises as soon as one word can be written in FIFO). See Table 23-695.

Table 23-695. Threshold for Transmit FIFO Interrupt/DMA Request

HST_MAPPINGf[13:10] THRESHOLD	Number of Words in FIFO	Request
0 (legacy default)	Less than 8	Yes
1	Less than 1	Yes
2	Less than 2	Yes
3	Less than 3	Yes
4	Less than 4	Yes
5	Less than 5	Yes
6	Less than 6	Yes
7	Less than 7	Yes
8	Less than 8	Yes
9 to 15	Any	No

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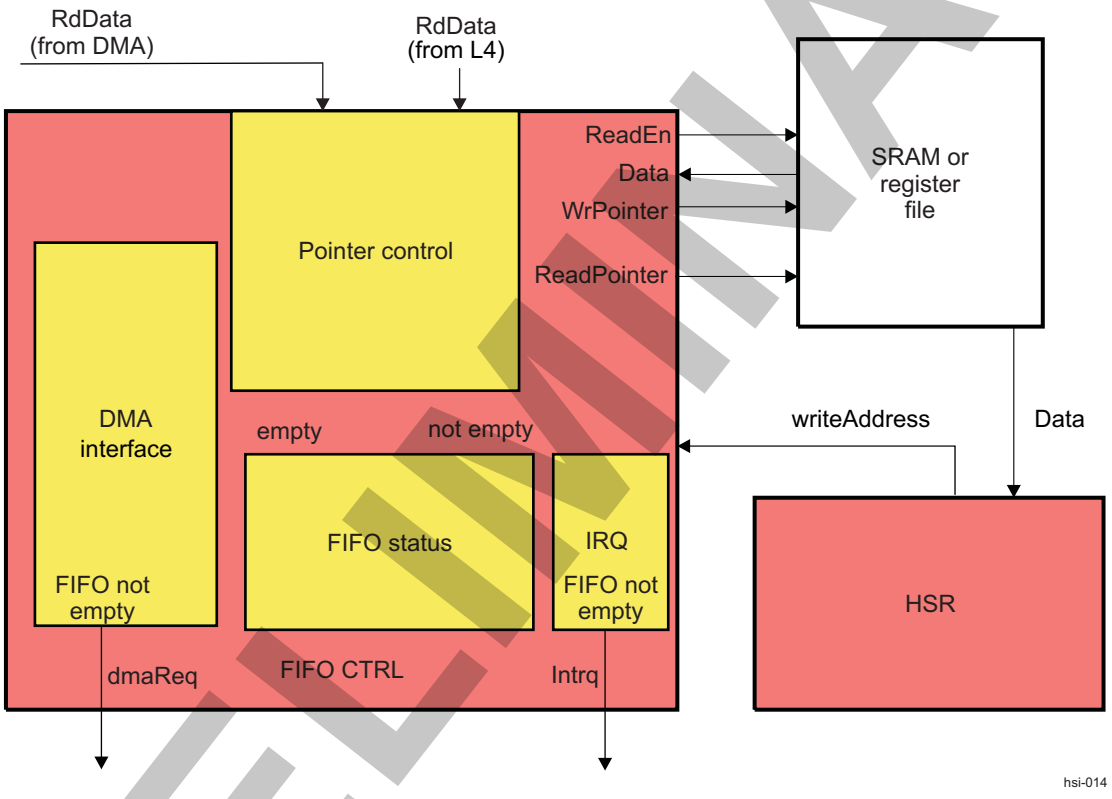
FIFO can be written by DMA and the L4 interconnect configuration port, but the L4 interconnect has fixed priority at any time. Software controls correct access. No hardware mechanism is provided to analyze and block concurrent operation, nor is any hardware control provided on reprogramming DMA registers during a transfer in which they are involved.

The address of FIFO is the corresponding HST_BUFFER_Pp_CHN_i register address. The FIFO controller generates the RAM addresses; namely, it manages the write pointer when DMA or the L4 interconnect access the HST_BUFFER_Pp_CHN_i address and it manages the read pointer when HST needs a data to transmit.

23.9.4.10.3 Receive FIFO Architecture

Figure 23-210 shows the reception FIFO architecture.

Figure 23-210. Reception FIFO Architecture



FIFO controller flags the condition of "unread data in FIFO" or "FIFO not empty" at any time when a FIFO hosts new data, received and not read. This condition can be simply the misalignment of the read pointer and write pointer. The condition raises an interrupt request and a DMA request, if enabled. The HSR_MAPPINGf[13:10] WORDS bit field informs software how many words must be read.

Unlike transmission, it is not possible here to filter requests through a threshold on the number of received words. If such a threshold is bigger than one, and a last single word is received after the last read, software is unaware that more data waits to be read.

The address of FIFO is the corresponding HSR_BUFFER_Pp_CHN_i register address. The FIFO controller generates the RAM addresses; namely, it manages the write pointer when HSR has received data, and it manages the read pointer when DMA or the L4 interconnect access the HSR_BUFFER_Pp_CHN_i register.

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23.9.4.10.4 FIFO Addressing

From a software point of view, a FIFO is seen at a single address, the corresponding HST_BUFFER_Pp_CHN_i or HSR_BUFFER_Pp_CHN_i register address. The HST_SWAPBUFFER_Pp_CHN_i or HSR_SWAPBUFFER_Pp_CHN_i register address is also provided to invert data endianness with byte granularity. FIFO overflow in RX is extremely unlikely, because of the large difference in HSI and L3_MAIN interconnect bit rate. However, if this occurs, the hardware prevents any loss of data by deasserting (setting to 0) the READY signal to the remote transmitter. FIFO overflow in TX is not flagged and must be avoided by software drivers.

23.9.4.11 Error Reporting

23.9.4.11.1 Detection of Errors

Error detection on the module is limited to the physical layer. No data corruption is checked, and no error is flagged as long as the receiver and transmitter agree on frame boundaries. Because clocking and data are recovered from alternate edges on the DATA and FLAG signals, three kinds of error can appear:

- Simultaneous edges
- Missing edges
- Additional edges

23.9.4.11.1.1 Simultaneous Edges

The transmitter is not supposed to produce simultaneous edges on the DATA and FLAG signals, but they can appear if the transmission rate is far higher than the receiver can handle. Given to the sampling protocol, this event may introduce errors in sampled data. Detecting this error is not easy, because the recovered clock is also affected, and in some configurations no other clock is available. One bit is available in the HSR_ERROR_Pp register, to report any hardware abnormal condition in data reception.

23.9.4.11.1.2 Missing Edges

Missing edges result in missing clock cycles, thus causing the receiver to get less data than expected on a given frame.

In synchronized flow, when the transmit side has completed transmission, the receiver side is still waiting for more data, and does not raise READY, thus stopping the transmitter from going on with more frames. A frame time-out counter (see Section 23.9.4.11.2.1, *Frame Time-Out Counter*) is used to escape this deadlock condition.

In pipelined flow, when the transmit side has completed transmission and has more data to transmit, the receiver accepts and processes this data as if they were part of the previous frame. Frame synchronization is then lost. It may randomly resume when in frame mode, as zeroes at the end of a frame are automatically discarded. But even in this case, a number of frames may be lost or corrupted. When in stream mode, no self-recovery is ever possible, and synchronization is lost forever. A frame burst counter (see Section 23.9.4.11.2.3, *Frame Burst Counter*) is used to limit the number of these potentially corrupted frames, simply by limiting the number of frames a transmitter can send back-to-back in a pipelined mode. A tailing bit counter (see Section 23.9.4.11.2.2, *Frame Tailing Bit Counter*) is used to check that the receiver and transmitter agree on being at the end of frame.

23.9.4.11.1.3 Additional Edges

Additional edges result in additional clock cycles, thus causing the receiver to get more data than expected on a given frame.

In synchronized flow, when the receive side thinks the frame is over, the transmitter keeps sending data until the end of frame is reached. In frame mode, if these additional bits are all 0s, they are discarded by the receiver, the transmission stops, and the receiver raises READY when it is available to receive a new frame. The transmit side starts a new frame and synchronization is recovered. But if at least one of the additional bits is set to 1, this can misguide the receiver that a new frame has already started and READY

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stays at 0. The transmit side stops, waiting for READY = 1, a never occurring condition, because the receiver has lost synchronization. In this case, the link is stuck. This is also the case in stream mode, when the receiver wrongly thinks that a new frame is started, so it is not available to receive a full new frame, and it does not set READY = 1. A frame time-out counter (see Section 23.9.4.11.2.1, *Frame Time-out Counter*) is used to escape this deadlock condition.

23.9.4.11.2 Error Counters

Clocks for these three counters are provided through a division of the functional clock. These counters can be set to a value and can be stopped when some events occur. Events flag errors and set a corresponding bit in the HSR_ERROR_Pp register.

23.9.4.11.2.1 Frame Time-Out Counter

This counter is clocked by the functional clock, divided by the factor specified in the HSR_DIVISOR_Pp[7:0] RX_RATE_DIV_VAL bit field, to provide a clock at receive bit rate. Receive bit rate is always communicated by the remote transmitter through the protocol layer. This counter starts when the first bit of the frame is found and stops when 36 (or 37 depending on the mode) bits are correctly received by the receiver. If the counter overflows, an error is generated (the HSR_ERROR_Pp[1] FTE bit is set to 0). In OPP reduction of the functional clock only (receive side kept in fixed voltage domain), software can decide to reduce either the division factor for the clock, or the count, to use a clock consistent with receive rate, or a reduced count of a slower clock. This is transparent for hardware. This counter is not started when the receive rate is outside the full error detection rate range.

23.9.4.11.2.2 Frame Tailing Bit Counter

This counter can be clocked by the same clock as the frame time-out counter, which has the receiver bit rate frequency. It starts after the last bit of a frame is received, and READY = 0; in pipelined flow, this counter is started only after the end of the last frame received. No event stops the counter, except its own overflow. It counts up to 8. An error is logged (the HSR_ERROR_Pp[4] TBE bit is set to 0) if a 1 bit is received in frame mode before counter overflow, or any bit is received in stream mode before counter overflow. In OPP reduction of functional clock only (receive side kept in fixed voltage domain), software can decide to reduce either the division factor for the clock, or the count, to use a clock consistent with receive rate, or a reduced count of a slower clock. This is transparent for hardware. This counter is not started when receive rate is outside the full error detection rate range.

23.9.4.11.2.3 Frame Burst Counter

Differently from previous counters, this counter is clocked by a frame-sync signal obtained directly by received data. Its goal is to reduce the number of contiguous frames sent in pipelined flow. As explained in Section 23.9.4.11.1, *Detection of Errors*, in some cases after missing/additional clock cycles, synchronization is lost and these pipelined frames can be corrupted. Software sets the count value, which can be as high as 256 (no higher values are supported by hardware). If READY is dropped to 0, for reasons other than counter expiration, the counter is stopped and restarted as soon as transmission resumes. At the end of the count, READY drops to 0. The tailing bit counter is started, and if it overflows without error detection and the receiver has enough room for another frame, READY is reset to 1. No error and no interrupt are generated on this counter.

23.9.4.11.3 Error Registers

One error register per port is provided to check the error source that issued an interrupt, with more details than the error bit in the interrupt status register.

- The HSR_ERROR_Pp[0] SIG bit: Signal error bits are kept for legacy reasons, and they can be used for any abnormal situation the hardware wants to flag.
- The HSR_ERROR_Pp[1] FTE bit: Frame time-out error bits flag the situation when not even a frame has been received in the time corresponding to two or more frames, depending on the FTE counter software setting.
- The HSR_ERROR_Pp[4] FBE bit: Tailing bit error bits flag the situation when at least one spurious bit is received after the end of a frame, in the time corresponding to two or more bit times.

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- The HSR_ERROR_Pp[7] RME bit: Receive mapping error bits flag the situation when data are received on a channel that is not mapped to any enabled FIFO.
- The HSR_ERROR_Pp[11] TME bit: Transmit mapping error bits flag the situation when DMA tries to access a FIFO that is not mapped to any logical channel, or is not enabled.

These two registers each have a companion HSR_ERRORACK_Pp register, where software must set the corresponding error bit to 1 to clear it.

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23.9.5 HSI Programming Guide

23.9.5.1 HSI Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the HSI module.

23.9.5.1.1 Global Initialization

23.9.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the HSI module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the HSI.

For more information, see Section 23.9.3, *HSI Integration*.

Table 23-696. Global Initialization of Surrounding Modules for HSI

Surrounding Modules	Comments
PRCM	HSI functional and interface clocks must be enabled. For more information, see Chapter 3, *Power, Reset, and Clock Management*.
Control module	Module-specific pad muxing must be set in the control module. For more information, see Chapter 18, *Control Module*.
(Optional) Interrupt controller	The MPU, IPU, or DSP INTC must be configured to enable the interrupt request generation to the MPU, IPU, or DSP subsystem. For information about enabling interrupts, see *Chapter 17, Interrupt Controller*.
(Optional) Interconnect	For information about the L4 interconnect configuration, see Chapter 14, *Interconnects*. For information about L3_MAIN interconnect configuration, see *Chapter 14, Interconnects*.

23.9.5.1.2 HSI Global Initialization

23.9.5.1.2.1 Main Sequence – HSI Global Initialization

This procedure initializes the HSI module after a power-on reset (POR) or software reset.

Table 23-697. HSI Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform an HSI software reset.	HSI_SYSCONFIG[1] SOFTRESET	0x1
WAIT UNTIL HSI reset is complete.	HSI_SYSSTATUS[0] RESETDONE	= 0x1
Set standby mode configuration.	HSI_SYSCONFIG[13:12] MIDLEMODE	0x-
Set idle mode configuration.	HSI_SYSCONFIG[4:3] SIDLEMODE	0x-
Clock auto gating.	HSI_SYSCONFIG[0] AUTOIDLE	0x-
Set the transmit data rate.	HST_DIVISOR_Pp[7:0] TX_RATE_DIV_VAL	0x-
(Optional) Enable DMA.	DMA_GCR[0] SWITCH_OFF	0x0

23.9.5.1.2 HSI Operational Modes Configuration

23.9.5.1.2.1 HSI Transmit Mode/Receive Mode

23.9.5.1.2.1.1 Main Sequence – Configure HSI Transmitter

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Table 23-698. HSI Configure HSI Transmitter

Step	Register/Bit Field/Programming Model	Value
Set the mode.	HST_MODE_Pp[1:0] MODE_VAL	0x-
Set the data flow type.	HST_MODE_Pp[3:2] FLOW_VAL	0x-
Set the hsi_wake line control.	HST_MODE_Pp[4] WAKE_CTRL	0x-
Set the transmission bit rate	HST_DIVISOR_Pp[7:0] TX_RATE_DIV_VAL	0x-
Set the arbitration mode.	HST_ARBMODE_Pp[0] ARB_VAL	0x-
Set the number of active HSI logical channels.	HST_CHANNELS_Pp[4:0] CHAN_NUM_VAL	0x-
Set the TX FIFO threshold.	HST_MAPPINGf[13:10] THRESHOLD	0x-
Associate the TX FIFO to an HSI port.	HST_MAPPINGf[7] PORT_NUMBER	0x-
Associate the TX FIFO to an HSI logical channel.	HST_MAPPINGf[4:1] CH_NUMBER	0x-
Enable the TX FIFO.	HST_MAPPINGf[0] ENABLE	0x-

23.9.5.1.2.1.2 Main Sequence – Configure HSI Receiver

Table 23-699. HSI Configure HSI Receiver

Step	Register/Bit Field/Programming Model	Value
Set a clock frequency for the error detection counters.	HSR_DIVISOR_Pp[7:0] RX_RATE_DIV_VAL	0x-
Set the number of active HSI logical channels.	HSR_CHANNELS_Pp[4:0] CHAN_NUM_VAL	0x-
Set the frame timeout error counter.	HSR_COUNTERS_Pp[19:0] FT	0x-
Set the tailing bit error counter.	HSR_COUNTERS_Pp[23:20] TB	0x-
Set the frame burst error counter.	HSR_COUNTERS_Pp[31:24] FB	0x-
Associate the RX FIFO to an HSI port.	HSR_MAPPINGf[7] PORT_NUMBER	0x-
Associate the RX FIFO to an HSI logical channel.	HSR_MAPPINGf[4:1] CH_NUMBER	0x-
Enable the RX FIFO.	HSR_MAPPINGf[0] ENABLE	0x-
Set the mode in receive mode.	HSR_MODE_Pp[1:0] MODE_VAL	0x-
Set the data flow type in receive mode.	HSR_MODE_Pp[3:2] FLOW_VAL	0x-

23.9.5.1.2.1.3 Main Sequence – HSI Polling Method

23.9.5.1.2.1.3.1 Sub-sequence – HSI Transmit in Polling Method

Figure 23-211 is a procedure flow chart for HSI transmit in polling method.

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Figure 23-211. HSI Transmit in Polling Method

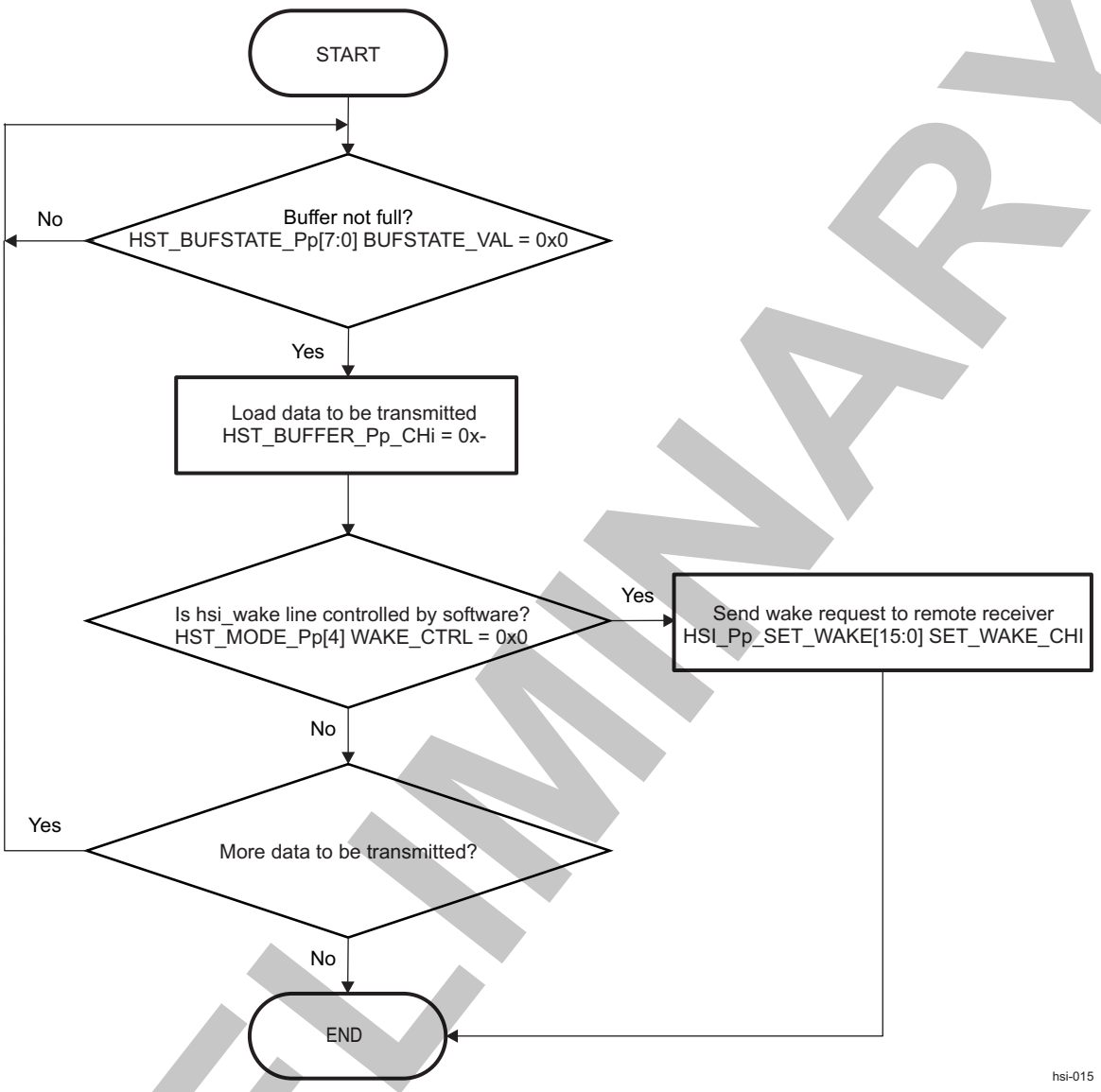

Table 23-700. Register Call Summary for Subsequence – HSI Transmit in Polling Method

Register Name	Register Name	Register Name
HST_BUFSTATE_Pp	HST_BUFFER_Pp_CHN_i	HST_MODE_Pp
HSI_Pp_SET_WAKE		

23.9.5.1.2.1.3.2 Subsequence – HSI Receive in Polling Method

Table 23-701. Event Servicing in HSI Receive in Polling Method

Step	Register/Bit Field/Programming Model	Value
IF: Is there data frame to be read?	HSR_BUFSTATE_Pp[7:0] BUFSTATE_VAL	=0x1
Identify number of words available in RX FIFO for reading.	HSR_MAPPINGf[13:10] WORDS	0x-
Read data from RX FIFO.	HSR_BUFFER_Pp_CHN_i[31:0] DATA	0x-

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Table 23-701. Event Servicing in HSI Receive in Polling Method (continued)

Step	Register/Bit Field/Programming Model	Value
ENDIF		

23.9.5.1.2.1.4 Main Sequence – HSI Interrupt Mode

Table 23-702. HSI Interrupt Mode

Step	Register/Bit Field/Programming Model	Value
Disable DMA engine.	DMA_GCR[0] SWITCH_OFF	0x1
Configure transmitter.	See Table 23-698.	
Configure receiver.	See Table 23-699.	
Enable HSI transmission interrupts.	See Table 23-703.	
WHEN HSI INTERRUPT OCCURS	See Figure 23-212.	
Enable HSI reception interrupts.	See Table 23-705.	
WHEN HSI INTERRUPT OCCURS	See Table 23-701.	

23.9.5.1.2.1.4.1 Subsequence – Interrupt Transmit Mode

Table 23-703. Enable HSI Transmit Interrupts

Step	Register/Bit Field/Programming Model	Value
Enable data accepted interrupt.	HSI_Pp_M_IRQrU_ENABLE[7:0] HST_ACCEPTED_ENI and/or HSI_Pp_D_IRQrU_ENABLE[7:0] HST_ACCEPTED_ENI and/or HSI_Pp_M_IRQr_ENABLE[7:0] HST_ACCEPTED_ENI and/or HSI_Pp_D_IRQr_ENABLE[7:0] HST_ACCEPTED_ENI	0x-

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Figure 23-212 is a procedure flow chart for event servicing in HSI transmission mode.

Figure 23-212. Event Servicing in HSI Transmission Mode

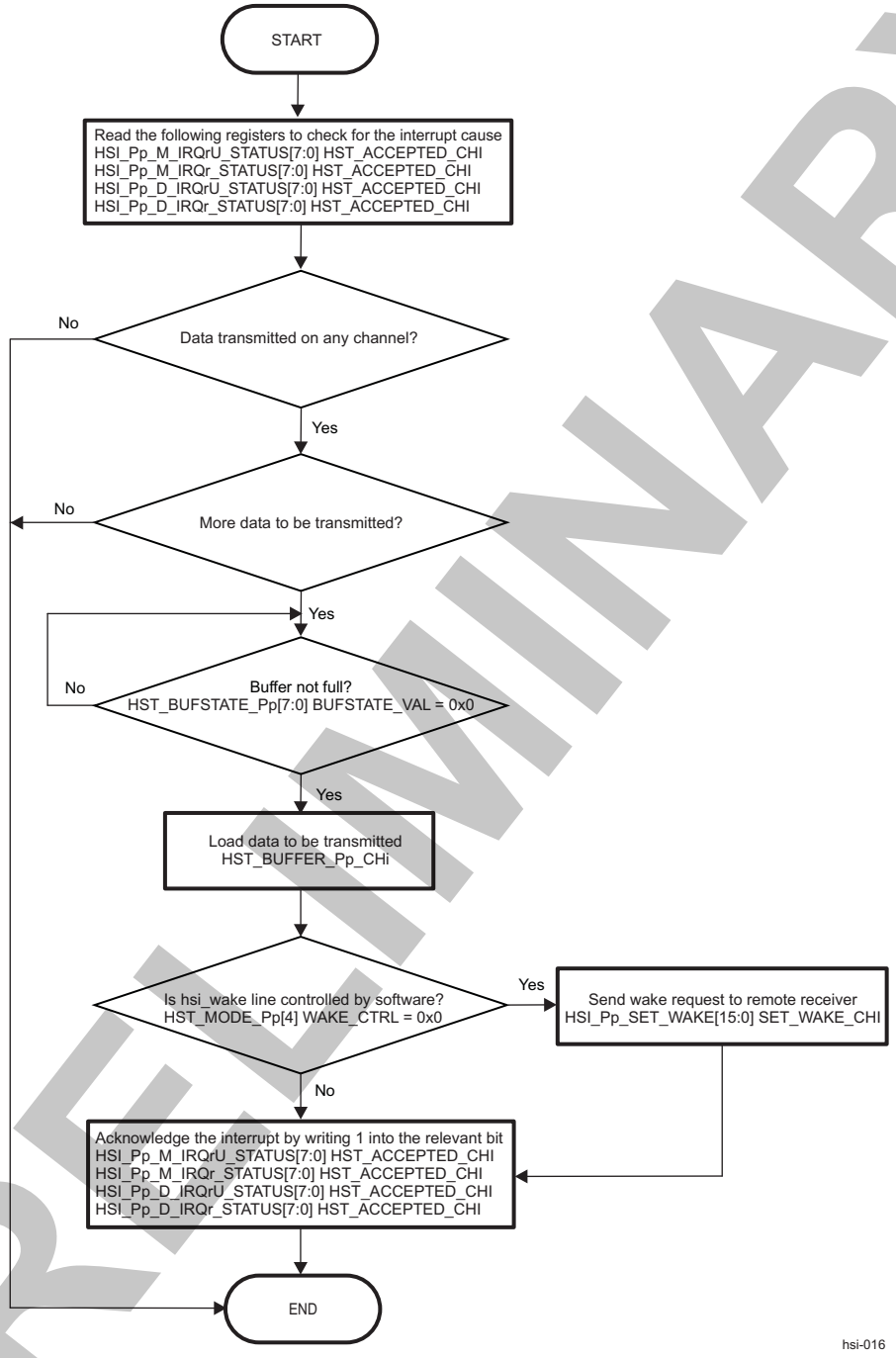

Table 23-704. Register Call Summary for Subsequence – Event Servicing in HSI Transmission Mode

Register Name	Register Name	Register Name
HSI_Pp_M_IRQrU_STATUS[7:0]HST_ACCEPTED_ CHI	HSI_Pp_D_IRQrU_STATUS[7:0]HST_ACCEPTED_CHI	HSI_Pp_M_IRQr_STATUS[7:0]HST_ACCEPTED_CHI
HSI_Pp_D_IRQr_STATUS[7:0] HST_ACCEPTED_CHI	HST_BUFFER_Pp_CHN_i[31:0] DATA	HST_MODE_Pp[4] WAKE_CTRL

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Table 23-704. Register Call Summary for Subsequence – Event Servicing in HSI Transmission Mode (continued)

Register Name	Register Name	Register Name
HSI_Pp_SET_WAKE[15:0] HSI_SET_WAKE_CHi		

23.9.5.1.2.1.4.2 Subsequence – Interrupt Receive Mode

Table 23-705. Enable HSI Receive Interrupts

Step	Register/Bit Field/Programming Model	Value
Enable break detected interrupt.	HSI_Pp_M_IRQrU_ENABLE[25] HSR_BREAK and/or HSI_Pp_D_IRQrU_ENABLE[25] HSR_BREAK and/or HSI_Pp_M_IRQr_ENABLE[25] HSR_BREAK and/or HSI_Pp_D_IRQr_ENABLE[25] HSR_BREAK	0x1
Enable wake detected interrupt.	HSI_Pp_M_IRQrU_ENABLE[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL and/or HSI_Pp_D_IRQrU_ENABLE[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL and/or HSI_Pp_M_IRQr_ENABLE[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL and/or HSI_Pp_D_IRQr_ENABLE[27] HSR_WAKE_RISE; [26] HSR_WAKE_FALL	0x1
Enable overrun interrupt.	HSI_Pp_M_IRQrU_ENABLE[23:16] HSR_OVERRUN_ENI and/or HSI_Pp_D_IRQrU_ENABLE[23:16] HSR_OVERRUN_ENI and/or HSI_Pp_M_IRQr_ENABLE[23:16] HSR_OVERRUN_ENI and/or HSI_Pp_D_IRQr_ENABLE[23:16] HSR_OVERRUN_ENI	0x-
Enable data available interrupt.	HSI_Pp_M_IRQrU_ENABLE[15:8] HSR_AVAILABLE_ENI and/or HSI_Pp_D_IRQrU_ENABLE[15:8] HSR_AVAILABLE_ENI and/or HSI_Pp_M_IRQr_ENABLE[15:8] HSR_AVAILABLE_ENI and/or HSI_Pp_D_IRQr_ENABLE[15:8] HSR_AVAILABLE_ENI	0x-

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Figure 23-213 is a procedure flow chart for event servicing in HSI reception mode.

Figure 23-213. Event Servicing in HSI Reception Mode

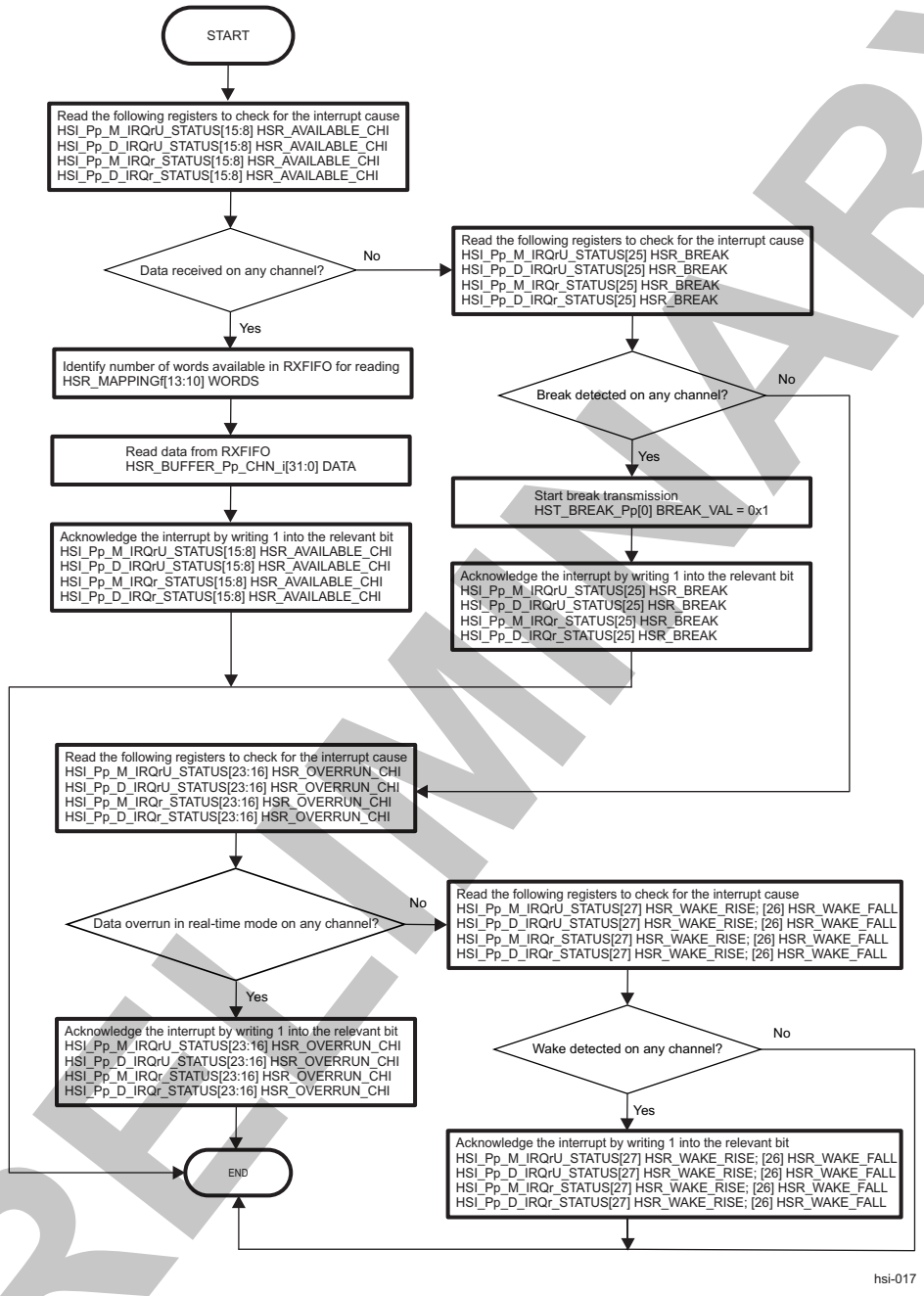

Table 23-706. Register Call Summary for Subsequence – Event Servicing in HSI Reception Mode

Register Name	Register Name	Register Name
HSI_Pp_M_IRQrU_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_D_IRQrU_STATUS[15:8] HSR_AVAILABLE_CHI	HSI_Pp_M_IRQr_STATUS[15:8] HSR_AVAILABLE_CHI
HSI_Pp_D_IRQr_STATUS[15:8] HSR_AVAILABLE_CHI	HSR_MAPPINGf[13:10] WORDS	HSR_BUFFER_Pp_CHN_i[31:0] DATA
HSI_Pp_M_IRQrU_STATUS[25] HSR_BREAK	HSI_Pp_D_IRQrU_STATUS[25] HSR_BREAK	HSI_Pp_M_IRQr_STATUS[25] HSR_BREAK
HSI_Pp_D_IRQr_STATUS[25] HSR_BREAK	HST_BREAK_Pp[0] BREAK_VAL	HSI_Pp_M_IRQrU_STATUS[23:16] HSR_OVERRUN_CHI

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Table 23-706. Register Call Summary for Subsequence – Event Servicing in HSI Reception Mode (continued)

Register Name	Register Name	Register Name
HSI_Pp_D_IRQrU_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_M_IRQr_STATUS[23:16] HSR_OVERRUN_CHI	HSI_Pp_D_IRQr_STATUS[23:16] HSR_OVERRUN_CHI

23.9.5.1.2.1.5 Main Sequence – HSI DMA Mode

23.9.5.1.2.1.5.1 Sub-sequence – DMA Configuration

Table 23-707. HSI DMA Configuration

Step	Register/Bit Field/Programming Model	Value
Perform a DMA software reset.	DMA_GRST[0] SWRESET	0x1
WAIT UNTIL DMA reset is complete.	DMA_GRST[0] SWRESET	= 0x0
Set autoidle mode configuration for DMA.	DMA_GCR[3] AUTOGATING	0x1
Configure HSI DMI receiver.	See Table 23-708.	
Configure HSI DMI transmit.	See Table 23-709.	
Enable DMA interrupts.	See Section 23.9.5.1.2.1.5.4.	
Enable DMA channel to start DMA transfer.	DMA_CCR_CSDP_i[23] ENABLE	0x1
WHEN DMA INTERRUPT OCCURS	See Table 23-702.	

23.9.5.1.2.1.5.2 Subsequence – DMA Receive Mode

Table 23-708. Configure DMA Receive Mode

Step	Register/Bit Field/Programming Model	Value
Set the transfer source to peripheral port.	DMA_CCR_CSDP_i[5:2] SRC	0x9
(Optional) Set the source burst enable.	DMA_CCR_CSDP_i[8:7] SRC_BURST_EN	0x1
Set the transfer destination to memory port.	DMA_CCR_CSDP_i[12:9] DST	0x8
(Optional) Set the destination burst enable.	DMA_CCR_CSDP_i[15:14] DST_BURST_EN	0x1
Set the source addressing mode to constant address.	DMA_CCR_CSDP_i[29:28] SRC_ADD_MODE	0x0
Set the destination addressing mode to post-incremented address.	DMA_CCR_CSDP_i[31:30] DST_ADD_MODE	0x1
Set the source start address.	DMA_CSSA_i[31:0] ADDR	0x-
Set the destination start address.	DMA_CDSA_i[31:0] ADDR	0x-
Set the number of elements in a block.	DMA_CEN_i[15:0] SIZE	0x-

23.9.5.1.2.1.5.3 Subsequence – DMA Transmit Mode

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Table 23-709. Configure DMA Transmit Mode

Step	Register/Bit Field/Programming Model	Value
Set the transfer source to memory port.	DMA_CCR_CSDP_i[5:2] SRC	0x8
(Optional) Set the source burst enable.	DMA_CCR_CSDP_i[8:7] SRC_BURST_EN	0x1
Set the transfer destination to peripheral port.	DMA_CCR_CSDP_i[12:9] DST	0x9
(Optional) Set the destination burst enable to single access.	DMA_CCR_CSDP_i[15:14] DST_BURST_EN	0x1
Set the source addressing mode to post-incremented address.	DMA_CCR_CSDP_i[29:28] SRC_ADD_MODE	0x1
Set the destination addressing mode to constant address.	DMA_CCR_CSDP_i[31:30] DST_ADD_MODE	0x0
Set the source start address.	DMA_CSSA_i[31:0] ADDR	0x-
Set the destination start address.	DMA_CDSA_i[31:0] ADDR	0x-
Set the number of elements in a block.	DMA_CEN_i[15:0] SIZE	0x-

23.9.5.1.2.1.5.4 Subsequence – Enable DMA Interrupts

Table 23-710. Enable DMA Interrupts

Step	Register/Bit Field/Programming Model	Value
Enable the DMA channels that shall generate an interrupt to a processor (MPU and/or DSP).	HSI_DMA_M_IRQENABLE[15:0] DMA_EN_CHI and/or HSI_DMA_D_IRQENABLE[15:0] DMA_EN_CHI	0x-
Enable the DMA full-block interrupt event.	DMA_CSR_CCIR_i[5] BLOCK_IE	0x1
Enable the DMA half-block interrupt event.	DMA_CSR_CCIR_i[2] HALF_IE	0x1
Enable the DMA time-out overflow interrupt event.	DMA_CSR_CCIR_i[0] TOUT_IE	0x1

23.9.5.1.2.1.5.5 Subsequence – DMA Interrupt Servicing

Table 23-711. Event Servicing in DMA Transmit/Receive Mode

Step	Register/Bit Field /Programming Model	Value
Identify which DMA channel has generated an interrupt.	HSI_DMA_M_IRQSTATUS[15:0] DMA_CHI and/or HSI_DMA_D_IRQSTATUS[15:0] DMA_CHI	0x-
Identify the interrupt event type.	DMA_CSR_CCIR_i[21] BLOCK_IS and/or DMA_CSR_CCIR_i[18] HALF_IS and/or DMA_CSR_CCIR_i[16] TOUT_IS	0x-
Acknowledge DMA global interrupt by setting the relevant bit to 1.	HSI_DMA_M_IRQSTATUS[15:0] DMA_CHI and/or HSI_DMA_D_IRQSTATUS[15:0] DMA_CHI	0x-

23.9.5.1.2.1.6 Main Sequence – HSI Error Reporting

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Table 23-712. Enable HSI Error Interrupts

Step	Register/Bit Field/Programming Model	Value
Enable error detected interrupt.	HSI_Pp_M_IRQrU_ENABLE[24] HSR_ERROR and/or HSI_Pp_D_IRQrU_ENABLE[24] HSR_ERROR and/or HSI_Pp_M_IRQr_ENABLE[24] HSR_ERROR and/or HSI_Pp_D_IRQr_ENABLE[24] HSR_ERROR	0x1

Table 23-713. Event Servicing Error

Step	Register/Bit Field/Programming Model	Value
Read interrupt status register.	HSI_Pp_M_IRQrU_STATUS[24] HSR_ERROR and/or HSI_Pp_D_IRQrU_STATUS[24] HSR_ERROR and/or HSI_Pp_M_IRQr_STATUS[24] HSR_ERROR and/or HSI_Pp_D_IRQr_STATUS[24] HSR_ERROR	0x-
Identify the interrupt event type.	HSR_ERROR_Pp[0] SIG HSR_ERROR_Pp[1] FTE HSR_ERROR_Pp[4] FBE HSR_ERROR_Pp[7] RME HSR_ERROR_Pp[11] TME	0x-
Clear the event by writing 1 into the relevant bit.	HSR_ERRORACK_Pp[0] SIG HSR_ERRORACK_Pp[1] FTE HSR_ERRORACK_Pp[4] FBE HSR_ERRORACK_Pp[7] RME HSR_ERRORACK_Pp[11] TME	0x1
Acknowledge the interrupt by writing 1 into the relevant bit.	HSI_Pp_M_IRQrU_STATUS[24] HSR_ERROR and/or HSI_Pp_D_IRQrU_STATUS[24] HSR_ERROR and/or HSI_Pp_M_IRQr_STATUS[24] HSR_ERROR and/or HSI_Pp_D_IRQr_STATUS[24] HSR_ERROR	0x1

23.9.6 HSI Register Manual

23.9.6.1 HSI Instance Summary

Table 23-714 summarizes the HSI instance.

Table 23-714. HSI Instance Summary

Module Name	Module Base Address	Size
HSI_TOP	0x4A05 8000	5 KiB
HSI_DMA_CHANNELS	0x4A05 9800	1 KiB
HSI_PORTS	0x4A05 A000	8 KiB

23.9.6.2 HSI_TOP Registers

23.9.6.2.1 HSI_TOP Register Summary

Table 23-715 summarizes the mapping of the HSI_TOP registers.

Table 23-715. HSI_TOP Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	HSI_TOP Physical Address
HSI_REVISION	R	32	0x0000 0000	0x4A05 8000
HSI_HWINFO	R	32	0x0000 0004	0x4A05 8004
HSI_SYSCONFIG	RW	32	0x0000 0010	0x4A05 8010
HSI_SYSSTATUS	R	32	0x0000 0014	0x4A05 8014

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Table 23-715. HSI_TOP Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	HSI_TOP Physical Address
HSI_Pp_M_IRQrU_STATUS (1)	RW	32	0x0000 0408 + (0x10 * b) + (0x8 * r)	0x4A05 8408 + (0x10 * b) + (0x8 * r)
HSI_Pp_M_IRQrU_ENABLE (1)	RW	32	0x0000 040C + (0x10 * b) + (0x8 * r)	0x4A05 840C + (0x10 * b) + (0x8 * r)
HSI_Pp_D_IRQrU_STATUS (1)	RW	32	0x0000 0430 + (0x10 * b) + (0x8 * r)	0x4A05 8430 + (0x10 * b) + (0x8* r)
HSI_Pp_D_IRQrU_ENABLE (1)	RW	32	0x0000 0434 + (0x10 * b) + (0x8 * r)	0x4A05 8434 + (0x10 * b) + (0x8 * r)
HSI_DMA_M_IRQSTATUS	RW	32	0x0000 0800	0x4A05 8800
HSI_DMA_M_IRQENABLE	RW	32	0x0000 0804	0x4A05 8804
HSI_Pp_M_IRQr_STATUS (1)	RW	32	0x0000 0808 + (0x10 * b) + (0x8 * r)	0x4A05 8808 + (0x10 * b) + (0x8 * r)
HSI_Pp_M_IRQr_ENABLE (1)	RW	32	0x0000 080C + (0x10 * b) + (0x8 * r)	0x4A05 880C + (0x10 * b) + (0x8 * r)
HSI_DMA_D_IRQSTATUS	RW	32	0x0000 0828	0x4A05 8828
HSI_DMA_D_IRQENABLE	RW	32	0x0000 082C	0x4A05 882C
HSI_Pp_D_IRQr_STATUS (2)	RW	32	0x0000 0830 + (0x10 * b) + (0x8 * r)	0x4A05 8830 + (0x10 * b) + (0x8 * r)
HSI_Pp_D_IRQr_ENABLE (2)	RW	32	0x0000 0834 + (0x10 * b) + (0x8 * r)	0x4A05 8834 + (0x10 * b) + (0x8 * r)
HSI_Pp_WAKE (2)	RW	32	0x0000 0C00 + (0x10 * b)	0x4A05 8C00 + (0x10 * b)
HSI_Pp_CLEAR_WAKE (2)	RW	32	0x0000 0C04 + (0x10 * b)	0x4A05 8C04 + (0x10 * b)
HSI_Pp_SET_WAKE (2)	RW	32	0x0000 0C08 + (0x10 * b)	0x4A05 8C08 + (0x10 * b)
RESERVED	RW	32	0x0000 1000	0x4A05 9000
DMA_GCR	RW	32	0x0000 1100	0x4A05 9100
DMA_GRST	RW	32	0x0000 1200	0x4A05 9200

(1) p = 1 to 2
r = 0 to 1
b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)

(2) p = 1 to 2
r = 0 to 1
b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)

23.9.6.2.2 HSI_TOP Register Description

Table 23-716 through Table 23-756 describe the HSI_TOP registers.

Table 23-716. HSI_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A05 8000	**Instance**	HSI_TOP
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI Internal Data

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Table 23-717. Register Call Summary for Register HSI_REVISION

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- HSI_TOP Register Summary: [0]

Table 23-718. HSI_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A05 8004	**Instance**	HSI_TOP
Description	Information about the IP module hardware configuration, that is, typically the module HDL generics (if any). Actual field format and encoding is decided by the module designer.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWINFO																															

Bits	Field Name	Description	Type	Reset
31:0	HWINFO	IP module hardware configuration	R	See (1).

(1) TI Internal Data

Table 23-719. Register Call Summary for Register HSI_HWINFO

MIPI-HSI

- HSI_TOP Register Summary: [0]

Table 23-720. HSI_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A05 8010	**Instance**	HSI_TOP
Description	This register allows controlling various parameters of the L4_CFG interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		MIDLEMODE		RESERVED							SIDLEMODE		FREE_EMU	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:12	MIDLEMODE	Master interface power management, standby/wait control 0x0: Force-standby 0x1: No-standby 0x2: Smart-standby 0x3: Smart-standby wakeup	RW	0x2
11:5	RESERVED	Reserved	R	0x00

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Bits	Field Name	Description	Type	Reset
4:3	SIDLEMODE	Slave interface power management, request/acknowledgment control 0x0: Force-idle 0x1: No-idle 0x2: Smart-idle 0x3: Smart-idle wakeup	RW	0x2
2	FREE_EMU	Sensitivity to emulation (debug) suspend input signal 0x0: Module is sensitive to emulation suspend. 0x1: Module is not sensitive to emulation suspend.	RW	0x0
1	SOFTRESET	Software reset 0x0: No reset applied 0x1: Software reset applied	RW	0x0
0	AUTOIDLE	Internal interface clock gating strategy 0x0: Interface clock is free-running 0x1: Automatic interface clock gating strategy, based on interconnect interface activity	RW	0x1

Table 23-721. Register Call Summary for Register HSI_SYSCONFIG

MIPI-HSI

- Software Reset: [0]
- Power Management: [1] [2] [3]
- Standby: [4]
- Idle: [5]
- Auto-Idle: [6]
- HSI Global Initialization: [7] [8] [9] [10]
- HSI_TOP Register Summary: [11]

Table 23-722. HSI_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A05 8014	**Instance**	HSI_TOP
Description	Status on module (reset done on bit 0, available for more status information)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESETDONE																															

Bits	Field Name	Description	Type	Reset
31:0	RESETDONE	internal reset monitoring Read 0x0: Internal reset is ongoing. Read 0x1: Internal reset is completed and the module is ready to be used.	R	0x0000 0001

Table 23-723. Register Call Summary for Register HSI_SYSSTATUS

MIPI-HSI

- Software Reset: [0]
- HSI Global Initialization: [1]
- HSI_TOP Register Summary: [2]

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Table 23-724. HSI_Pp_M_IRQrU_STATUS

Address Offset	0x0000 0408 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8408 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ status register for FIFO (8..15) events and for port p break, wake and error events. Events will signal interrupt for MPU line r (Mpuirq_r). Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_CHI								HSR_AVAILABLE_CHI								HST_ACCEPTED_CHI							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x00
27	HSR_WAKE_RISE	Receive wake rising edge detected on Port p	RW	0x0
26	HSR_WAKE_FALL	Receive wake falling edge detected on Port p	RW	0x0
25	HSR_BREAK	Break detected on Port p	RW	0x0
24	HSR_ERROR	Error detected on Port p	RW	0x0
23:16	HSR_OVERRUN_CHI	Data overrun in real-time mode channel 8..15 (LSB stands for channel 8 and MSB for channel 15).	RW	0x00
15:8	HSR_AVAILABLE_CHI	Data received on channel 8..15 (LSB stands for channel 8 and MSB for channel 15). The status bit shows data on the respective channel, while there are data in the FIFO. Clearing the status bit has no effect, while the FIFO is not empty.	RW	0x00
7:0	HST_ACCEPTED_CHI	Data transmitted on channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0xFF

Table 23-725. Register Call Summary for Register HSI_Pp_M_IRQrU_STATUS

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Transmit Mode/Receive Mode: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-726. HSI_Pp_M_IRQrU_ENABLE

Address Offset	0x0000 040C + (0x10 * b) + (0x8 * r)		p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 840C + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ enable register for FIFO (8..15) events and for port p break, wake and error events signaled to MPU line r (Mpuirq_r). Write 0: Event is masked. Write 1: Event is enabled.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_ENI								HSR_AVAILABLE_ENI								HST_ACCEPTED_ENI							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x00
27	HSR_WAKE_RISE	Receive wake rising edge detection enable for Port p	RW	0x0
26	HSR_WAKE_FALL	Receive wake falling edge detection enable for Port p	RW	0x0
25	HSR_BREAK	Break interrupt enable for Port p	RW	0x0
24	HSR_ERROR	Error interrupt enable for Port p	RW	0x0
23:16	HSR_OVERRUN_ENI	Overrun interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00
15:8	HSR_AVAILABLE_ENI	Data available interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00
7:0	HST_ACCEPTED_ENI	Data accepted interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00

Table 23-727. Register Call Summary for Register HSI_Pp_M_IRQrU_ENABLE

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Transmit Mode/Receive Mode: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-728. HSI_Pp_D_IRQrU_STATUS

Address Offset	0x0000 0430 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8430 + (0x10 * b) + (0x8* r)	**Instance**	HSI_TOP
Description	IRQ status register for FIFO (8..15) events and for port p break, wake and error events. Events will signal interrupt for DSP line r (Dspirq_r). Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_CHI								HSR_AVAILABLE_CHI								HST_ACCEPTED_CHI							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x00
27	HSR_WAKE_RISE	Receive wake rising edge detected on Port p	RW	0x0
26	HSR_WAKE_FALL	Receive wake falling edge detected on Port p	RW	0x0
25	HSR_BREAK	Break detected on Port p	RW	0x0
24	HSR_ERROR	Error on Port p	RW	0x0

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Bits	Field Name	Description	Type	Reset
23:16	HSR_OVERRUN_CHI	Data overrun in real-time mode channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00
15:8	HSR_AVAILABLE_CHI	Data received on channel 8..15 (LSB stands for channel 8 and MSB for channel 15). The status bit shows data on the respective channel, while there are data in the FIFO. Clearing the status bit has no effect, while the FIFO is not empty.	RW	0x00
7:0	HST_ACCEPTED_CHI	Data transmitted on channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0xFF

Table 23-729. Register Call Summary for Register HSI_Pp_D_IRQrU_STATUS

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Transmit Mode/Receive Mode: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-730. HSI_Pp_D_IRQrU_ENABLE

Address Offset	0x0000 0434 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8434 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ enable register for FIFO (8..15) events and for port p break, wake and error events signaled to DSP line r (Dspirq_r). Write 0: Event is masked. Write 1:Eevent is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_ENI								HSR_AVAILABLE_ENI								HST_ACCEPTED_ENI							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x00
27	HSR_WAKE_RISE	Receive wake rising edge detection enable for Port p	RW	0x0
26	HSR_WAKE_FALL	Receive wake falling edge detection enable for Port p	RW	0x0
25	HSR_BREAK	Break interrupt enable for Port p	RW	0x0
24	HSR_ERROR	Error interrupt enable for Port p	RW	0x0
23:16	HSR_OVERRUN_ENI	Overrun interrupt enable for channel 8..15	RW	0x00
15:8	HSR_AVAILABLE_ENI	Data available interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00
7:0	HST_ACCEPTED_ENI	Data accepted interrupt enable for channel 8..15 (LSB stands for channel 8 and MSB for channel 15)	RW	0x00

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Table 23-731. Register Call Summary for Register HSI_Pp_D_IRQrU_ENABLE

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Transmit Mode/Receive Mode: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-732. HSI_DMA_M_IRQSTATUS

Address Offset	0x0000 0800		
Physical Address	0x4A05 8800	**Instance**	HSI_TOP
Description	This register collects status for all of the DMA events able to generate interrupt to MPU: Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DMA_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	DMA_CHI	Channel 0..15 status (LSB stands for channel 0 and MSB for channel 15)	RW	0x0000

Table 23-733. Register Call Summary for Register HSI_DMA_M_IRQSTATUS

MIPI-HSI

- Interrupt Requests: [0]
- Interrupts: [1]
- DMA Interrupt Generation: [2]
- HSI Transmit Mode/Receive Mode: [3] [4]
- HSI_TOP Register Summary: [5]

Table 23-734. HSI_DMA_M_IRQENABLE

Address Offset	0x0000 0804		
Physical Address	0x4A05 8804	**Instance**	HSI_TOP
Description	This register masks and unmasks DMA sources of interrupt to MPU: Write 0: event is masked Write 1: event is enabled		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DMA_EN_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	DMA_EN_CHI	Channel 0..15 status (LSB stands for channel 0 and MSB for channel 15)	RW	0x0000

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Table 23-735. Register Call Summary for Register HSI_DMA_M_IRQENABLE

MIPI-HSI

- Interrupt Requests: [0]
- Interrupts: [1]
- HSI Transmit Mode/Receive Mode: [2]
- HSI_TOP Register Summary: [3]

Table 23-736. HSI_Pp_M_IRQr_STATUS

Address Offset	0x0000 0808 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8808 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ status register for FIFO (0..7) events and for port p break, wake and error events. Events will signal interrupt for MPU line r (Mpuirq_r). Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_CHI								HSR_AVAILABLE_CHI								HST_ACCEPTED_CHI							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x00
27	HSR_WAKE_RISE	Receive wake rising edge detected on Port p	RW	0x0
26	HSR_WAKE_FALL	Receive wake falling edge detected on Port p	RW	0x0
25	HSR_BREAK	Break detected on Port p	RW	0x0
24	HSR_ERROR	Error on Port p	RW	0x0
23:16	HSR_OVERRUN_CHI	Data overrun in real time mode channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
15:8	HSR_AVAILABLE_CHI	Data received on channel 0..7 (LSB stands for channel 0 and MSB for channel 7). The status bit shows data on the respective channel, while there are data in the FIFO. Clearing the status bit has no effect, while the FIFO is not empty.	RW	0x00
7:0	HST_ACCEPTED_CHI	Data transmitted on channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0xFF

Table 23-737. Register Call Summary for Register HSI_Pp_M_IRQr_STATUS

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Transmit Mode/Receive Mode: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

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Table 23-738. HSI_Pp_M_IRQr_ENABLE

Address Offset	0x0000 080C + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 880C + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ enable register for FIFO (0..7) events and for port p break, wake and error events signaled to MPU line r (Mpuirq_r). Write 0: Event is masked. Write 1: Event is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_ENI								HSR_AVAILABLE_ENI								HST_ACCEPTED_ENI							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x00
27	HSR_WAKE_RISE	Receive wake rising edge detection enable for Port p	RW	0x0
26	HSR_WAKE_FALL	Receive wake falling edge detection enable for Port p	RW	0x0
25	HSR_BREAK	Break interrupt enable for Port p	RW	0x00
24	HSR_ERROR	Error interrupt enable for Port p	RW	0x0
23:16	HSR_OVERRUN_ENI	Overrun interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
15:8	HSR_AVAILABLE_ENI	Data available interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
7:0	HST_ACCEPTED_ENI	Data accepted interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00

Table 23-739. Register Call Summary for Register HSI_Pp_M_IRQr_ENABLE

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Transmit Mode/Receive Mode: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-740. HSI_DMA_D_IRQSTATUS

Address Offset	0x0000 0828		
Physical Address	0x4A05 8828	**Instance**	HSI_TOP
Description	IRQ status register for all DMA events. Events generate interrupt for DSP. Read 0: Event has not occurred; Read 1: Event has occurred ; Write 0: Bit stays unchanged; Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DMA_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	DMA_CHI	IRQ event happened on DMA channel 0..15 (LSB stands for channel 0 and MSB for channel 15).	RW	0x0000

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Table 23-741. Register Call Summary for Register HSI_DMA_D_IRQSTATUS

MIPI-HSI

- Interrupt Requests: [0]
- Interrupts: [1]
- DMA Interrupt Generation: [2]
- HSI Transmit Mode/Receive Mode: [3] [4]
- HSI_TOP Register Summary: [5]

Table 23-742. HSI_DMA_D_IRQENABLE

Address Offset	0x0000 082C		
Physical Address	0x4A05 882C	**Instance**	HSI_TOP
Description	IRQ enable register for all DMA events signaled to DSP. Write 0: Event is masked. Write 1: Event is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DMA_EN_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	DMA_EN_CHI	Channel 0..15 (LSB stands for channel 0 and MSB for channel 15)	RW	0x0000

Table 23-743. Register Call Summary for Register HSI_DMA_D_IRQENABLE

MIPI-HSI

- Interrupt Requests: [0]
- Interrupts: [1]
- HSI Transmit Mode/Receive Mode: [2]
- HSI_TOP Register Summary: [3]

Table 23-744. HSI_Pp_D_IRQr_STATUS

Address Offset	0x0000 0830 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8830 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ status register for FIFO (0..7) events and for port p break, wake and error events. Events will signal interrupt for DSP line r (Dspirq_r). Read 0: Event has not occurred. Read 1: Event has occurred. Write 0: Bit stays unchanged. Write 1: Bit is reset to 0.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_CHI								HSR_AVAILABLE_CHI								HST_ACCEPTED_CHI							

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x00
27	HSR_WAKE_RISE	Receive wake rising edge detected on Port p	RW	0x0
26	HSR_WAKE_FALL	Receive wake falling edge detected on Port p	RW	0x0
25	HSR_BREAK	Break detected on Port p	RW	0x0
24	HSR_ERROR	Error on Port p	RW	0x0
23:16	HSR_OVERRUN_CHI	Data overrun in real time mode channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
15:8	HSR_AVAILABLE_CHI	Data received on channel 0..7 (LSB stands for channel 0 and MSB for channel 7). The status bit shows data on the respective channel, while there are data in the FIFO. Clearing the status bit has no effect, while the FIFO is not empty.	RW	0x00
7:0	HST_ACCEPTED_CHI	Data transmitted on channel 0..7 (LSB stands for channel 0 and MSB for channel 7).	RW	0xFF

Table 23-745. Register Call Summary for Register HSI_Pp_D_IRQr_STATUS

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Transmit Mode/Receive Mode: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-746. HSI_Pp_D_IRQr_ENABLE

Address Offset	0x0000 0834 + (0x10 * b) + (0x8 * r)	**Index**	p = 1 to 2 r = 0 to 1 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8834 + (0x10 * b) + (0x8 * r)	**Instance**	HSI_TOP
Description	IRQ enable register for FIFO (0..7) events and for port p break, wake and error events signaled to DSP line r (Dspirq_r). Write 0: Event is masked. Write 1: Event is enabled.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					HSR_WAKE	HSR_BREAK	HSR_ERROR	HSR_OVERRUN_ENI								HSR_AVAILABLE_ENI								HST_ACCEPTED_ENI							

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x00
27	HSR_WAKE_RISE	Receive wake rising edge detection enable for Port p	RW	0x0
26	HSR_WAKE_FALL	Receive wake falling edge detection enable for Port p	RW	0x0
25	HSR_BREAK	Break interrupt enable for Port p	RW	0x0
24	HSR_ERROR	Error interrupt enable for Port p	RW	0x0
23:16	HSR_OVERRUN_ ENI	Overrun interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
15:8	HSR_AVAILABLE_ ENI	Data available interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7)	RW	0x00
7:0	HST_ACCEPTED_ ENI	Data accepted interrupt enable for channel 0..7 (LSB stands for channel 0 and MSB for channel 7).	RW	0x00

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Table 23-747. Register Call Summary for Register HSI_Pp_D_IRQr_ENABLE

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- Interrupts: [6]
- HSI Transmit Mode/Receive Mode: [7] [8] [9] [10] [11] [12]
- HSI_TOP Register Summary: [13]

Table 23-748. HSI_Pp_WAKE

Address Offset	0x0000 0C00 + (0x10 * b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8C00 + (0x10 * b)	**Instance**	HSI_TOP
Description	Programmed wake state for each channel, in port p 0x0: No channel wakeup on WAKE line requested. 0x1: Channel wakeup requested		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSI_WAKE_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	HSI_WAKE_CHI	Channel 0..15 (LSB stands for channel 0 and MSB for channel 15)	R	0x0000

Table 23-749. Register Call Summary for Register HSI_Pp_WAKE

MIPI-HSI

- HSI Wake Generator: [0]
- Software Management of HSI Wake Generator: [1] [2]
- Automatic Management of HSI Wake Generator: [3]
- HSI_TOP Register Summary: [4]

Table 23-750. HSI_Pp_CLEAR_WAKE

Address Offset	0x0000 0C04 + (0x10 * b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8C04 + (0x10 * b)	**Instance**	HSI_TOP
Description	Clear register for programmed wake state on port p HST_WAKE for each channel 0x0: No effect 0x1: Clears bit		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSI_HSI_CLEAR_WAKE_CHI															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	HSI_CLEAR_WAKE_CHI	Channel 0..15 (LSB stands for channel 0 and MSB for channel 15)	W	0x0000

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Table 23-751. Register Call Summary for Register HSI_Pp_CLEAR_WAKE

MIPI-HSI

- Software Management of HSI Wake Generator: [0]
- HSI_TOP Register Summary: [1]

Table 23-752. HSI_Pp_SET_WAKE

Address Offset	0x0000 0C08 + (0x10 * b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 8C08 + (0x10 * b)	**Instance**	HSI_TOP
Description	Set function for wake state for each channel, in port p 0x0: No effect 0x1: Sets bit		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														HSI_READY_LVL	HSI_3_WIRES	HSI_SET_WAKE_CHI															

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17	HSI_READY_LVL	READY default level 0x0: READY defaults to 0. 0x1: READY defaults to 1.	RW	0x0
16	HSI_3_WIRES	Sets 3-wire behavior 0x0: Sets 4-wire behavior (wakeup with WAKE signal) 0x1: Sets 3-wire behavior (wakeup on line activity without WAKE signal)	RW	0x0
15:0	HSI_SET_WAKE_CHI	Sets programmed WAKE state for channel i Write 0x0: No effect Write 0x1: Sets bit	W	0x0000

Table 23-753. Register Call Summary for Register HSI_Pp_SET_WAKE

MIPI-HSI

- Software Management of HSI Wake Generator: [0] [1]
- HSI Transmit Mode/Receive Mode: [2] [3]
- HSI_TOP Register Summary: [4]

Table 23-754. DMA_GCR

Address Offset	0x0000 1100		
Physical Address	0x4A05 9100	**Instance**	HSI_TOP
Description	Global Control Register: suspend and clock gating		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												AUTOGATING	RESERVED		SWITCH_OFF

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3	AUTOGATING	DMA clock autogating enable 0x0: No DMA clock control 0x1: DMA clock control	RW	0x0
2:1	RESERVED	Reserved	R	0x0
0	SWITCH_OFF	DMA global clock control 0x0: DMA clock released 0x1: DMA clock cutoff	RW	0x0

Table 23-755. Register Call Summary for Register DMA_GCR

MIPI-HSI
- Power Management: [0]
- Auto-Idle: [1]
- DMA Engine Switch Off Mode: [2]
- HSI Global Initialization: [3]
- HSI Transmit Mode/Receive Mode: [4] [5]
- HSI_TOP Register Summary: [6]

Table 23-756. DMA_GRST

Address Offset	0x0000 1200		
Physical Address	0x4A05 9200	**Instance**	HSI_TOP
Description	DMA software reset control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															SWRESET

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	SWRESET	DMA software reset control bit 0x1: Writing 1 resets the DMA. It is automatically reset to 0 by hardware once software reset is done.	RW	0x0

Table 23-757. Register Call Summary for Register DMA_GRST

MIPI-HSI
- Software Reset: [0]
- HSI Transmit Mode/Receive Mode: [1] [2]
- HSI_TOP Register Summary: [3]

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23.9.6.3 HSI_DMA_CHANNELS Registers

23.9.6.3.1 HSI_DMA_CHANNELS Register Summary

Table 23-758 summarizes the mapping of the HSI_DMA_CHANNELS registers.

Table 23-758. HSI_DMA_CHANNELS Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	HSI_DMA_CHANNELS Base Address
DMA_CCR_CSDP_i (1)	RW	32	0x0000 0000 + (0x40 * i)	0x4A05 9800 + (0x40 * i)
DMA_CSR_CCIR_i (1)	RW	32	0x0000 0004 + (0x40 * i)	0x4A05 9804 + (0x40 * i)
DMA_CSSA_i (1)	RW	32	0x0000 0008 + (0x40 * i)	0x4A05 9808 + (0x40 * i)
DMA_CDSA_i (1)	RW	32	0x0000 000C + (0x40 * i)	0x4A05 980C + (0x40 * i)
DMA_CEN_i (1)	RW	32	0x0000 0010 + (0x40 * i)	0x4A05 9810 + (0x40 * i)
DMA_CDAC_CSAC_i (1)	R	32	0x0000 0018 + (0x40 * i)	0x4A05 9818 + (0x40 * i)
Reserved	R	32	0x0000 0028 + (0x40 * i)	0x4A05 9828 + (0x40 * i)

(1) i = 0 to 15

23.9.6.3.2 HSI_DMA_CHANNELS Register Description

Table 23-759 through Table 23-769 describe the HSI_DMA_CHANNELS registers.

Table 23-759. DMA_CCR_CSDP_i

Address Offset	0x0000 0000 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9800 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Stores source and destination parameters and channel control bits		
Type	RW		

31 30	29 28	27 26 25 24	23	22 21 20 19 18 17 16	15 14	13	12 11 10 9 8	7 6	5 4 3 2	1 0
DST_ADD_MODE	SRC_ADD_MODE	RESERVED	ENABLE	RESERVED	DST_BURST_EN	RESERVED	DST	SRC_BURST_EN	RESERVED	SRC	DATA_TYPE

Bits	Field Name	Description	Type	Reset
31:30	DST_ADD_MODE	Destination addressing mode 0x0: Constant address 0x1: Post-increment address	RW	0x0
29:28	SRC_ADD_MODE	Source addressing mode 0x0: Constant address 0x1: Post-increment address	RW	0x0
27:24	RESERVED	Reserved	R	0

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Bits	Field Name	Description	Type	Reset
23	ENABLE	Logical channel enable 0x0: Transfer stops and is reset. 0x1: Transfer is enabled. Automatically cleared by hardware once transfer is finished.	RW	0
22:16	RESERVED	Reserved	R	0
15:14	DST_BURST_EN	Destination burst enable 0x0: Single access 0x1: Single access 0x3: Burst 8 × 32 bits (not implemented) 0x2: Burst 4 × 32 bits	RW	0x0
13	RESERVED	Reserved	R	0
12:9	DST	Transfer destination 0x8: Transfer to memory port 0x9: Transfer to peripheral port	RW	0x0
8:7	SRC_BURST_EN	Source burst enable 0x0: Single access 0x1: Single access 0x3: Burst 8 × 32 bits (not implemented) 0x2: Burst 4 × 32 bits	RW	0x0
6	RESERVED	Reserved	R	0
5:2	SRC	Transfer source 0x8: Transfer from memory port 0x9: Transfer from peripheral port	RW	0x0
1:0	DATA_TYPE	Defines data types Implemented bit field but not used	RW	0x0

Table 23-760. Register Call Summary for Register DMA_CCR_CSDP_i

MIPI-HSI

- DMA Configuration: [0] [1] [2] [3] [4] [5] [6] [7] [8]
- HSI Transmit Mode/Receive Mode: [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21]
- HSI_DMA_CHANNELS Register Summary: [22]

Table 23-761. DMA_CSR_CCIR_i

Address Offset	0x0000 0004 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9804 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Interrupt enable and status register Interrupt flag fields will be cleared through read access using the following byte-enable values: 0xC 0xF		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										BLOCK_IS	RESERVED		HALF_IS	RESERVED	TOUT_IS	RESERVED										BLOCK_IE	RESERVED		HALF_IE	RESERVED	TOUT_IE

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Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	R	0x000
21	BLOCK_IS	Block transferred Read 0x1: Block transferred Read 0x0: No event	R	0
20:19	RESERVED	Reserved	R	0x0
18	HALF_IS	Half block reached Read 0x1:Half-block transferred Read 0x0: No event	R	0
17	RESERVED	Reserved	R	0
16	TOUT_IS	Time-out overflow event Read 0x1: Time-out occurred Read 0x0: No event	R	0
15:6	RESERVED	Reserved	R	0x000
5	BLOCK_IE	Interrupt is sent when a full block is transferred 0x0: No interrupt 0x1:Interrupt enable	RW	0
4:3	RESERVED	Reserved	R	0x0
2	HALF_IE	Interrupt is sent when a half block is transferred 0x0: No interrupt 0x1: Interrupt enable	RW	0
1	RESERVED	Reserved	R	0
0	TOUT_IE	Interrupt is sent when a time-out overflow occurs 0x0: No interrupt 0x1: Interrupt enable	RW	0

Table 23-762. Register Call Summary for Register DMA_CSR_CCIR_i

MIPI-HSI

- Interrupt Requests: [0] [1] [2] [3] [4] [5]
- DMA Interrupt Generation: [6] [7] [8] [9] [10] [11] [12]
- DMA Configuration: [13]
- HSI Transmit Mode/Receive Mode: [14] [15] [16] [17] [18] [19]
- HSI_DMA_CHANNELS Register Summary: [20]

Table 23-763. DMA_CSSA_i

Address Offset	0x0000 0008 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9808 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Stores source start address If the transfer configured from memory port, all bits are taken into account as an address. If the transfer configured from peripheral port, the lower 4 bits will determine the FIFO ID.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															

Bits	Field Name	Description	Type	Reset
31:0	ADDR	Source start address	RW	0x0000 0000

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Table 23-764. Register Call Summary for Register DMA_CSSA_i

MIPI-HSI

- DMA Configuration: [0]
- HSI Transmit Mode/Receive Mode: [1] [2]
- HSI_DMA_CHANNELS Register Summary: [3]

Table 23-765. DMA_CDSA_i

Address Offset	0x0000 000C + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 980C + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Stores destination start address If the transfer configured to memory port, all bits are taken into account as an address. If the transfer configured to peripheral port, the lower 4 bits will determine the FIFO ID.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															

Bits	Field Name	Description	Type	Reset
31:0	ADDR	Destination start address	RW	0x0000 0000

Table 23-766. Register Call Summary for Register DMA_CDSA_i

MIPI-HSI

- DMA Configuration: [0]
- HSI Transmit Mode/Receive Mode: [1] [2]
- HSI_DMA_CHANNELS Register Summary: [3]

Table 23-767. DMA_CEN_i

Address Offset	0x0000 0010 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9810 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Stores the number of 4-byte words in a DMA data block. Maximum is 65,536.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	SIZE	Number of elements in a block. Maximum is 65,536.	RW	0x0000

Table 23-768. Register Call Summary for Register DMA_CEN_i

MIPI-HSI

- DMA Interrupt Generation: [0]
- DMA Configuration: [1]
- HSI Transmit Mode/Receive Mode: [2] [3]
- HSI_DMA_CHANNELS Register Summary: [4]

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Table 23-769. DMA_CDAC_CSAC_i

Address Offset	0x0000 0018 + (0x40 * i)	**Index**	i = 0 to 15
Physical Address	0x4A05 9818 + (0x40 * i)	**Instance**	HSI_DMA_CHANNELS
Description	Monitors the progress of DMA transfer, by storing the 16-bit counter address for source and destination.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS_CDAC																ADDRESS_CSAC															

Bits	Field Name	Description	Type	Reset
31:16	ADDRESS_CDAC	Destination address	R	0x0000
15:0	ADDRESS_CSAC	Source address	R	0x0000

Table 23-770. Register Call Summary for Register DMA_CDAC_CSAC_i

MIPI-HSI

- DMA Configuration: [0] [1]
- HSI_DMA_CHANNELS Register Summary: [2]

23.9.6.4 HSI_PORTS Registers

23.9.6.4.1 HSI_PORTS Register Summary

Table 23-771 summarizes the mapping of the HSI_PORTS registers.

Table 23-771. HSI_PORTS Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	HSI_PORTS Physical Address
HST_ID_Pp (1)	R	32	0x0000 0000 + (0x1000* b)	0x4A05 A000 + (0x1000* b)
HST_MODE_Pp (1)	RW	32	0x0000 0004 + (0x1000* b)	0x4A05 A004 + (0x1000* b)
HST_FRAMESIZE_Pp (1)	R	32	0x0000 0008 + (0x1000* b)	0x4A05 A008 + (0x1000* b)
HST_TXSTATE_Pp (1)	R	32	0x0000 000C + (0x1000* b)	0x4A05 A00C + (0x1000* b)
HST_BUFSTATE_Pp (1)	R	32	0x0000 0010 + (0x1000* b)	0x4A05 A010 + (0x1000* b)
HST_DIVISOR_Pp (1)	RW	32	0x0000 0018 + (0x1000* b)	0x4A05 A018 + (0x1000* b)
HST_BREAK_Pp (1)	W	32	0x0000 0020 + (0x1000* b)	0x4A05 A020 + (0x1000* b)
HST_CHANNELS_Pp (1)	RW	32	0x0000 0024 + (0x1000* b)	0x4A05 A024 + (0x1000* b)
HST_ARBMODE_Pp (1)	RW	32	0x0000 0028 + (0x1000* b)	0x4A05 A028 + (0x1000* b)
HST_BUFFER_Pp_CHN_i (1)	W	32	0x0000 0080 + (0x1000* b) + (0x4 * i)	0x4A05 A080 + (0x1000* b) + (0x4 * i)
HST_SWAPBUFFER_Pp_CHN_i (1)	W	32	0x0000 00C0 + (0x1000* b) + (0x4 * i)	0x4A05 A0C0 + (0x1000* b) + (0x4 * i)
HST_MAPPINGf (1)	RW	32	0x0000 0100 + (0x4 * f)	0x4A05 A100 + (0x4 * f)
RESERVED	RW	32	0x0000 0144	0x4A05 A144

(1) p = 1 to 2
i = 0 to 7
f = 0 to 15
b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)

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Table 23-771. HSI_PORTS Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	HSI_PORTS Physical Address
HSR_ID_Pp (1)	R	32	0x0000 0800 + (0x1000* b)	0x4A05 A800 + (0x1000* b)
HSR_MODE_Pp (1)	RW	32	0x0000 0804 + (0x1000* b)	0x4A05 A804 + (0x1000* b)
HSR_FRAMESIZE_Pp (1)	R	32	0x0000 0808 + (0x1000* b)	0x4A05 A808 + (0x1000* b)
HSR_RXSTATE_Pp (1)	R	32	0x0000 080C + (0x1000* b)	0x4A05 A80C + (0x1000* b)
HSR_BUFSTATE_Pp (1)	R	32	0x0000 0810 + (0x1000* b)	0x4A05 A810 + (0x1000* b)
RESERVED	R	32	0x0000 081C + (0x1000* b)	0x4A05 A81C + (0x1000* b)
HSR_ERROR_Pp (1)	R	32	0x0000 0820 + (0x1000* b)	0x4A05 A820 + (0x1000* b)
HSR_ERRORACK_Pp (1)	W	32	0x0000 0824 + (0x1000* b)	0x4A05 A824 + (0x1000* b)
HSR_CHANNELS_Pp (1)	RW	32	0x0000 0828 + (0x1000* b)	0x4A05 A828 + (0x1000* b)
HSR_OVERRUN_Pp (2)	RW	32	0x0000 082C + (0x1000* b)	0x4A05 A82C + (0x1000* b)
HSR_OVERRUNACK_Pp (2)	R	32	0x0000 0830 + (0x1000* b)	0x4A05 A830 + (0x1000* b)
HSR_COUNTERS_Pp (2)	W	32	0x0000 0834 + (0x1000* b)	0x4A05 A834 + (0x1000* b)
HSR_BUFFER_Pp_CHN_i (2)	R	32	0x0000 0880 + (0x1000* b) + (0x4 * i)	0x4A05 A880 + (0x1000* b) + (0x4 * i)
HSR_SWAPBUFFER_Pp_CHN_i (2)	R	32	0x0000 08C0 + (0x1000* b) + (0x4 * i)	0x4A05 A8C0 + (0x1000* b) + (0x4 * i)
HSR_MAPPINGf (2)	RW	32	0x0000 0900 + (0x4 * f)	0x4A05 A900 + (0x4 * f)
RESERVED	RW	32	0x0000 0944	0x4A05 A944
RESERVED	RW	32	0x0000 0948	0x4A05 A948
HSR_DIVISOR_Pp (2)	RW	32	0x0000 094C + (0x1000* b)	0x4A05 A94C + (0x1000* b)

(2) p = 1 to 2
i = 0 to 7
f = 0 to 15
b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)

23.9.6.4.2 HSI_PORTS Register Description

Table 23-772 through Table 23-824 describe the HSI_PORTS registers.

Table 23-772. HST_ID_Pp

Address Offset	0x0000 0000 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A000 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Legacy identification on port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID_VAL																															

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Bits	Field Name	Description	Type	Reset
31:0	ID_VAL	Legacy ID	R	See (1).

(1) TI Internal Data

Table 23-773. Register Call Summary for Register HST_ID_Pp

MIPI-HSI
- HSI_PORTS Register Summary: [0]

Table 23-774. HST_MODE_Pp

Address Offset	0x0000 0004 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A004 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Defines operation mode and data flow on port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											WAKE_CTRL	FLOW_VAL		MODE_VAL	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4	WAKE_CTRL	Wake control 0x0: Software control 0x1: Automatic control	RW	0
3:2	RESERVED	Reserved	R	0x0
1:0	MODE_VAL	Mode 0x0: Sleep 0x1: Stream 0x2: Frame 0x3: Reserved	RW	0x0

Table 23-775. Register Call Summary for Register HST_MODE_Pp

MIPI-HSI
- Mode Register: [0] [1] [2] [3]
- HSI Transmit Mode/Receive Mode: [4] [5] [6] [7] [8]
- HSI_PORTS Register Summary: [9]

Table 23-776. HST_FRAMESIZE_Pp

Address Offset	0x0000 0008 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A008 + (0x1000* b)	**Instance**	HSI_PORTS
Description	This register is provided for legacy and possible future extension of protocol. Returns 0x1f.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SIZE_VAL							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	SIZE_VAL	In the current implementation it must be always written 31, meaning the frame payload size is 32 bits. Read 0x1F: Only possible value	R	0x1F

Table 23-777. Register Call Summary for Register HST_FRAMESIZE_Pp

MIPI-HSI
- Other Registers: [0]
- HSI_PORTS Register Summary: [1]

Table 23-778. HST_TXSTATE_Pp

Address Offset	0x0000 000C + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A00C + (0x1000* b)	**Instance**	HSI_PORTS
Description	Define the state of the transmitter on port p.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														TXSTATEVAL	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	TXSTATEVAL	State of the transmitter Read 0x0: Idle Read 0x1: Wait Read 0x2: Transmit Read 0x3: Start Read 0x4: Break Read 0x5: Reserved Read 0x6: Reserved Read 0x7: Sleep (disabled)	R	0x7

Table 23-779. Register Call Summary for Register HST_TXSTATE_Pp

MIPI-HSI
- Transmission Operations: [0]
- HSI_PORTS Register Summary: [1]

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Table 23-780. HST_BUFSTATE_Pp

Address Offset	0x0000 0010 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A010 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Transmitter state for FIFO 0..7 Each bit gives the state of transmit FIFOs: 0x1: FIFO full 0x0: FIFO not full		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BUFSTATE_VAL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	BUFSTATE_VAL	Each bit gives the state of transmit buffer register: 0x0: Buffer is not full. 0x1: Buffer is full.	R	0x00

Table 23-781. Register Call Summary for Register HST_BUFSTATE_Pp

MIPI-HSI

- Transmission Buffer: [0] [1]
- Transmission Operations: [2]
- HSI Transmit Mode/Receive Mode: [3]
- HSI_PORTS Register Summary: [4]

Table 23-782. HST_DIVISOR_Pp

Address Offset	0x0000 0018 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A018 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Transmission bit rate divisor for port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TX_RATE_DIV_VAL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	TX_RATE_DIV_VAL	This bit field B has a range [0..255] and it programs a division factor [1..256], B + 1. Example: Writing 0 divides by 1, writing 1 divides by 2, writing 2 divides by 3, etc.	RW	0x00

Table 23-783. Register Call Summary for Register HST_DIVISOR_Pp

MIPI-HSI

- Transmit Clock: [0]
- Other Registers: [1]
- HSI Global Initialization: [2]
- HSI Transmit Mode/Receive Mode: [3]
- HSI_PORTS Register Summary: [4]

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Table 23-784. HST_BREAK_Pp

Address Offset	0x0000 0020 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A020 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Transmit break strobe register on port p		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															BREAK_VAL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	W	0x0000 0000
0	BREAK_VAL	Send a break signal on the port Write 0x0: No break Write 0x1: Transmit break	W	0x0

Table 23-785. Register Call Summary for Register HST_BREAK_Pp

MIPI-HSI

- Break Pattern Transmission: [0] [1] [2]
- HSI Transmit Mode/Receive Mode: [3]
- HSI_PORTS Register Summary: [4]

Table 23-786. HST_CHANNELS_Pp

Address Offset	0x0000 0024 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A024 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Number of active channels on port p (this determines the number of the used channel descriptor bits on the MIPI port as well) It can be 1, 2, 4, 8, or 16.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											CHAN_NUM_VAL					

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	CHAN_NUM_VAL	Number of active channels up to 16 0x1: One logical channel used, number of the channel descriptor bits is 0. 0x2: Two logical channels used, number of the channel descriptor bits is 1. 0x4: Four logical channels used, number of the channel descriptor bits is 2. 0x8: Eight logical channels used, number of the channel descriptor bits is 3. 0x10: Sixteen logical channels used, number of the channel descriptor bits is 4.	RW	0x01

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Table 23-787. Register Call Summary for Register HST_CHANNELS_Pp

MIPI-HSI

- Other Registers: [0]
- HSI Transmit Mode/Receive Mode: [1]
- HSI_PORTS Register Summary: [2]

Table 23-788. HST_ARBMODE_Pp

Address Offset	0x0000 0028 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A028 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Arbitration type for the transmit FIFOs on port p.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															ARB_VAL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	ARB_VAL	Mode 0x0: Round robin 0x1: Priority	RW	0

Table 23-789. Register Call Summary for Register HST_ARBMODE_Pp

MIPI-HSI

- Other Registers: [0]
- Mapping: [1] [2]
- HSI Transmit Mode/Receive Mode: [3]
- HSI_PORTS Register Summary: [4]

Table 23-790. HST_BUFFER_Pp_CHN_i

Address Offset	0x0000 0080 + (0x1000* b) + (0x4 * i)	**Index**	p = 1 to 2 i = 0 to 7 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A080 + (0x1000* b) + (0x4 * i)	**Instance**	HSI_PORTS
Description	Transmit register for FIFO 0..7 Important: Write access to the register with 0xC and 0xF byteen loads its value into the transmit FIFO. If using only 16- bit accesses, the lower 2 bytes must be written first (byteen 0x3). Between two consecutive 16-bit FIFO-related access there cannot be any other FIFO-related OCP access.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

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Bits	Field Name	Description	Type	Reset
31:0	DATA	32 bits of data	W	0x0000 0000

Table 23-791. Register Call Summary for Register HST_BUFFER_Pp_CHN_i

MIPI-HSI

- DMA Basic Operation Outline: [0]
- Transmission Buffer: [1] [2]
- Transmission Operations: [3] [4] [5]
- Transmission Exceptions: [6]
- Transmit FIFO Architecture: [7] [8]
- FIFO Addressing: [9]
- HSI Transmit Mode/Receive Mode: [10] [11]
- HSI_PORTS Register Summary: [12]

Table 23-792. HST_SWAPBUFFER_Pp_CHN_i

Address Offset	0x0000 00C0 + (0x1000* b) + (0x4 * i)	**Index**	p = 1 to 2 i = 0 to 7 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A0C0 + (0x1000* b) + (0x4 * i)	**Instance**	HSI_PORTS
Description	Transmit register with byte swapping for FIFO 0..7 Important: Write access to the register with 0x3 and 0xF byteen loads its value into the transmit FIFO. If using only 16-bit accesses, the upper 2 bytes must be written first (byteen 0xC). Between two consecutive 16-bit FIFO-related access there cannot be any other FIFO-related OCP access.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWAPDATA																															

Bits	Field Name	Description	Type	Reset
31:0	SWAPDATA	32 bits of byte-swapped data	W	0x0000 0000

Table 23-793. Register Call Summary for Register HST_SWAPBUFFER_Pp_CHN_i

MIPI-HSI

- Transmission Buffer: [0]
- FIFO Addressing: [1]
- HSI_PORTS Register Summary: [2]

Table 23-794. HST_MAPPINGf

Address Offset	0x0000 0100 + (0x4 * f)	**Index**	f = 0 to 15
Physical Address	0x4A05 A100 + (0x4 * f)	**Instance**	HSI_PORTS
Description	TX FIFO configuration register. One register per FIFO.		
Type	RW		

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31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8	7	6	5 4 3 2	1 0
RESERVED		THRESHOLD	RESERVED	PORT_NUMBER	RESERVED	CH_NUMBER	ENABLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:10	THRESHOLD	Number of empty TX FIFO locations that will activate interrupt or DMA requests. DMA requests (if enabled) or interrupt assertion (if enabled) is triggered if the number of free locations in FIFO is less than the THRESHOLD value. 0x0: Less than 8 words in the FIFO 0x1: Less than 1 words in the FIFO 0x2: Less than 2 words in the FIFO … 0x8: Less than 8 words in the FIFO 0x9 through 0xF: No request generated	RW	0x0
9:8	RESERVED	Reserved	R	0x0
7	PORT_NUMBER	Associates the FIFO to a HSI port 0x0: Port 1 0x1: Port 2	RW	0
6:5	RESERVED	Reserved	R	0x0
4:1	CH_NUMBER	Associates the TX FIFO to a HSI logical channel number (0-15): 0x0: Logical channel number 0 0x1: Logical channel number 1 … 0xF: Logical channel number 15	RW	0x0
0	ENABLE	Enables the FIFO 0x0: Disabled 0x1: Enabled	RW	1

Table 23-795. Register Call Summary for Register HST_MAPPINGf

MIPI-HSI

- DMA Basic Operation Outline: [0]
- Other Registers: [1] [2] [3] [4] [5]
- Mapping: [6] [7]
- FIFO Subsystem Architecture: [8]
- Transmit FIFO Architecture: [9] [10]
- HSI Transmit Mode/Receive Mode: [11] [12] [13] [14]
- HSI_PORTS Register Summary: [15]

Table 23-796. HSR_ID_Pp

Address Offset	0x0000 0800 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A800 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Legacy identification		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID_VAL																															

Bits	Field Name	Description	Type	Reset
31:0	ID_VAL	Legacy ID	R	See (1)

(1) TI Internal Data

Table 23-797. Register Call Summary for Register HSR_ID_Pp

MIPI-HSI
- HSI_PORTS Register Summary: [0]

Table 23-798. HSR_MODE_Pp

Address Offset	0x0000 0804 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A804 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Defines operation mode and data flow on port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											WAKE_STATUS	FLOW_VAL			MODE_VAL	

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4	WAKE_STATUS	Level of WAKE line	R	-
3:2	FLOW_VAL	Flow 0x0: Synchronized 0x1: Pipelined 0x2: Real-time 0x3: Suspended	RW	0x3
1:0	MODE_VAL	Mode 0x0: Sleep (disabled) 0x1: Stream (1) 0x2: Frame (1) 0x3: Reserved	RW	0x0

(1) Selecting stream or frame mode, activates READY line and will cause start of communication. The mode should be set at the end of module's configuration, just before the start.

Table 23-799. Register Call Summary for Register HSR_MODE_Pp

MIPI-HSI
- Receive Operations: [0]
- Mode Register: [1]
- HSI Transmit Mode/Receive Mode: [2] [3]
- HSI_PORTS Register Summary: [4]

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Table 23-800. HSR_FRAMESIZE_Pp

Address Offset	0x0000 0808 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A808 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Legacy returns 0x1f		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													SIZE_VAL		

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	SIZE_VAL	0x1F	R	0x1F

Table 23-801. Register Call Summary for Register HSR_FRAMESIZE_Pp

MIPI-HSI

- HSI_PORTS Register Summary: [0]

Table 23-802. HSR_RXSTATE_Pp

Address Offset	0x0000 080C + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A80C + (0x1000* b)	**Instance**	HSI_PORTS
Description	Receiver state on port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														RXSTATEVAL	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:0	RXSTATEVAL	RX state Read 0x0: Idle Read 0x1: Receiving Read 0x2: Finished Read 0x3: Error Read 0x4: Halt Read 0x5: Time-out Read 0x6: Reserved Read 0x7: Sleep (disabled)	R	0x7

Table 23-803. Register Call Summary for Register HSR_RXSTATE_Pp

MIPI-HSI

- Receive Operations: [0] [1]
- HSI_PORTS Register Summary: [2]

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Table 23-804. HSR_BUFSTATE_Pp

Address Offset	0x0000 0810 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A810 + (0x1000* b)	**Instance**	HSI_PORTS
Description	State of receiver buffer register for port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BUFSTATE_VAL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	BUFSTATE_VAL	Each bit gives the state of receiver buffer register: 0x0: Buffer is not full. 0x1: Buffer is full.	R	0x00

Table 23-805. Register Call Summary for Register HSR_BUFSTATE_Pp

MIPI-HSI

- Receive Buffers: [0] [1] [2] [3]
- HSI Transmit Mode/Receive Mode: [4]
- HSI_PORTS Register Summary: [5]

Table 23-806. HSR_ERROR_Pp

Address Offset	0x0000 0820 + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A820 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Error detection state register for port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		RESERVED		TME		RESERVED		RME		RESERVED		TBE		RESERVED		FTE	SIG

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	RESERVED	Reserved	R	0x0
14:12	RESERVED	Reserved	R	0x0
11	TME	TX mapping error	R	0x0
10:8	RESERVED	Reserved	R	0x0
7	RME	RX mapping error	R	0x0
6:5	RESERVED	Reserved	R	0x0
4	TBE	Tailing bit error	R	0x0
3:2	RESERVED	Reserved	R	0x0
1	FTE	Frame time-out error	R	0x0
0	SIG	Signal error (legacy)	R	0x0

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Table 23-807. Register Call Summary for Register HSR_ERROR_Pp

MIPI-HSI

- Simultaneous Edges: [0]
- Error Counters: [1]
- Frame Time-Out Counter: [2]
- Frame Tailing Bit Counter: [3]
- Error Registers: [4] [5] [6] [7] [8]
- HSI Transmit Mode/Receive Mode: [9] [10] [11] [12] [13]
- HSI_PORTS Register Summary: [14]

Table 23-808. HSR_ERRORACK_Pp

Address Offset	0x0000 0824 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A824 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Error detection acknowledge register on port p: write 1 to clear.		
Type	W		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED		RESERVED		TME		RESERVED		RME		RESERVED		TBE		RESERVED		FTE	SIG

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	W	0x0000
15	RESERVED	Reserved	W	0x0
14:12	RESERVED	Reserved	W	0x0
11	TME	TX mapping error	W	0x0
10:8	RESERVED	Reserved	W	0x0
7	RME	RX mapping error	W	0x0
6:5	RESERVED	Reserved	W	0x0
4	TBE	Tailing bit error	W	0x0
3:2	RESERVED	Reserved	W	0x0
1	FTE	Frame time-out error	W	0x0
0	SIG	Signal error (legacy)	W	0x0

Table 23-809. Register Call Summary for Register HSR_ERRORACK_Pp

MIPI-HSI

- Errors: [0]
- Error Registers: [1]
- HSI Transmit Mode/Receive Mode: [2] [3] [4] [5] [6]
- HSI_PORTS Register Summary: [7]

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Table 23-810. HSR_CHANNELS_Pp

Address Offset	0x0000 0828 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A828 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Number of active channels on port p (this determines the number of the used channel descriptor bits on the MIPI port as well) It can be 1, 2, 4, 8, or 16.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CHAN_NUM_VAL							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:0	CHAN_NUM_VAL	Number of active channels 0x1: One logical channel used, number of the channel descriptor bits is 0 0x2: Two logical channels used, number of the channel descriptor bits is 1 0x4: Four logical channels used, number of the channel descriptor bits is 2 0x8: Eight logical channels used, number of the channel descriptor bits is 3 0x10: Sixteen logical channels used, number of the channel descriptor bits is 4	RW	0x01

Table 23-811. Register Call Summary for Register HSR_CHANNELS_Pp

MIPI-HSI

- HSI Transmit Mode/Receive Mode: [0]
- HSI_PORTS Register Summary: [1]

Table 23-812. HSR_OVERRUN_Pp

Address Offset	0x0000 082C + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A82C + (0x1000* b)	**Instance**	HSI_PORTS
Description	Overrun detection state register for those receive FIFOs that are mapped to port p		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OVERRUN_VAL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	OVERRUN_VAL	Bit n is set when overrun is detected on channel n Read 0x1: Overrun detected Read 0x0: No overrun	R	0x0000

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Table 23-813. Register Call Summary for Register HSR_OVERRUN_Pp

MIPI-HSI

- Overrun: [0]
- HSI_PORTS Register Summary: [1]

Table 23-814. HSR_OVERRUNACK_Pp

Address Offset	0x0000 0830 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A830 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Overrun acknowledge register for those receive FIFOs that are mapped to port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OVERRUNACK_VAL															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	OVERRUNACK_VAL	Bit n is set when overrun is acknowledged on channel n. Write 0x0: No action Write 0x1: Overrun acknowledge	W	0x0000

Table 23-815. Register Call Summary for Register HSR_OVERRUNACK_Pp

MIPI-HSI

- HSI_PORTS Register Summary: [0]

Table 23-816. HSR_COUNTERS_Pp

Address Offset	0x0000 0834 + (0x1000* b)		p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A834 + (0x1000* b)	**Instance**	HSI_PORTS
Description	Counters setting register for port p		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FB								TB				FT																			

Bits	Field Name	Description	Type	Reset
31:24	FB	Setting for Frame Burst Counter. Setting n as a value results in n + 1 counter value.	RW	0x00
23:20	TB	Setting for Tailing Bit Counter. Setting n as a value results in n + 1 counter value.	RW	0x0
19:0	FT	Setting for Frame Time-out counter. Set n as a value results in n+1 counter value.	RW	0x00000

Table 23-817. Register Call Summary for Register HSR_COUNTERS_Pp

MIPI-HSI

- Receive Operations: [0]
- HSI Transmit Mode/Receive Mode: [1] [2] [3]
- HSI_PORTS Register Summary: [4]

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Table 23-818. HSR_BUFFER_Pp_CHN_i

Address Offset	0x0000 0880 + (0x1000* b) + (0x4 * i)	**Index**	p = 1 to 2 i = 0 to 7 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A880 + (0x1000* b) + (0x4 * i)	**Instance**	HSI_PORTS
Description	Receive register for receive FIFO 0..7 Important: Read access to the register with 0xC and 0xF byteen removes the receive FIFO-related item. If using only 16-bit accesses, the lower 2 bytes must be read first (byteen 0x3). Between two consecutive 16-bit FIFO-related access there cannot be any other FIFO-related OCP access.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	Received data	R	0x--------

Table 23-819. Register Call Summary for Register HSR_BUFFER_Pp_CHN_i

MIPI-HSI

- DMA Basic Operation Outline: [0]
- Receive Buffers: [1] [2] [3] [4] [5]
- Receive FIFO Architecture: [6] [7]
- FIFO Addressing: [8]
- HSI Transmit Mode/Receive Mode: [9] [10]
- HSI_PORTS Register Summary: [11]

Table 23-820. HSR_SWAPBUFFER_Pp_CHN_i

Address Offset	0x0000 08C0 + (0x1000* b) + (0x4 * i)	**Index**	p = 1 to 2 i = 0 to 7 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A8C0 + (0x1000* b) + (0x4 * i)	**Instance**	HSI_PORTS
Description	Byte swapped receive register for receive FIFO 0..7 Important: Read access to the register with 0x3 and 0xF byteen removes the receive FIFO-related item. If using only 16-bit accesses, the upper 2 bytes must be read first (byteen 0xC). Between two consecutive 16-bit FIFO-related access there cannot be any other FIFO- related OCP access.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWAPDATA																															

Bits	Field Name	Description	Type	Reset
31:0	SWAPDATA	Received data swapped	R	0x--------

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Table 23-821. Register Call Summary for Register HSR_SWAPBUFFER_Pp_CHN_i

MIPI-HSI

- Receive Buffers: [0] [1]
- FIFO Addressing: [2]
- HSI_PORTS Register Summary: [3]

Table 23-822. HSR_MAPPINGf

Address Offset	0x0000 0900 + (0x4 * f)	**Index**	f = 0 to 15
Physical Address	0x4A05 A900 + (0x4 * f)	**Instance**	HSI_PORTS
Description	RX FIFO Configuration register. One register per FIFO.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		WORDS				RESERVED		PORT_NUMBER	RESERVED			CH_NUMBER			ENABLE

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:10	WORDS	Number of words available in the RX FIFO for reading	R	0x0
9:8	RESERVED	Reserved	R	0x0
7	PORT_NUMBER	Associates the RX FIFO to a HSI port 0x0: Port 1 0x1: Port 2	RW	0x0
6:5	RESERVED	Reserved	R	0x0
4:1	CH_NUMBER	Associates RX FIFO to a HSI logical channel 0x0: Logical channel number 0 0x1: Logical channel number 1 … 0xF: Logical channel number 15	RW	0x0
0	ENABLE	Enables or disables RX FIFO 0x0: Disabled 0x1: Enabled	RW	0x1

Table 23-823. Register Call Summary for Register HSR_MAPPINGf

MIPI-HSI

- DMA Basic Operation Outline: [0]
- Other Registers: [1]
- FIFO Subsystem Architecture: [2]
- Receive FIFO Architecture: [3]
- HSI Transmit Mode/Receive Mode: [4] [5] [6] [7] [8]
- HSI_PORTS Register Summary: [9]

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Table 23-824. HSR_DIVISOR_Pp

Address Offset	0x0000 094C + (0x1000* b)	**Index**	p = 1 to 2 b = 0 to 1 (for p = 1, b = 0 and p = 2, b = 1)
Physical Address	0x4A05 A94C + (0x1000* b)	**Instance**	HSI_PORTS
Description	Receive bit rate divisor for port p. This must be set for correct protocol timing detection (tailing time-out, frame time-out).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RX_RATE_DIV_VAL							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	RX_RATE_DIV_VAL	The functional clock source divided by this value is used as a clock base for the receive counters. Setting n as a value results in the n + 1 divisor value.	RW	0x00

Table 23-825. Register Call Summary for Register HSR_DIVISOR_Pp

MIPI-HSI

- Receive Error Detection Counters Clocks: [0]
- Frame Time-Out Counter: [1]
- HSI Transmit Mode/Receive Mode: [2]
- HSI_PORTS Register Summary: [3]

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23.10 High-Speed Multiport USB Host Subsystem

This section describes the high-speed (HS) multiport universal serial bus (USB) host subsystem of the device.

23.10.1 High-Speed Multiport USB Host Subsystem Overview

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The HS USB host subsystem is composed of:

- HS multiport USB host controller module
- USB TLL module
- Three HSIC digital front end (DFE) modules

The HS USB host subsystem consists of several ports delivered outside the device and several modes per port. These modes are:

- UTMI+ low pin-count interface (ULPI) for external PHY
- ULPI transceiverless link (TLL)
- Serial TLL
- High-speed interchip (HSIC)

The HS USB host controller module contains two quasi-independent host controllers that operate in parallel:

- The EHCI controller, based on the *Enhanced Host Controller Interface (EHCI) Specification for USB Release 1.1*, is responsible for HS traffic (480 Mbps), over ULPI/USB 2.0 transceiver macrocell interface (UTMI).
- The OHCI controller, based on the *Open Host Controller Interface (OHCI Specification for USB Release 1.0a*, is responsible for full-speed (FS)/low-speed (LS) traffic (12/1.5 Mbps, respectively), over a serial interface.

Each of the three external ports of the HS USB host controller module is owned by one of the controllers (EHCI or OHCI) at a given time. Each port can work in several modes:

- When the port is owned by the OHCI (FS) host, a 6-pin internal serial interface to the TLL is used.
- When the port is owned by the EHCI (HS) host, UTMI internal interface to the TLL or through ULPI to external PHY is used.

  See USB controller module internal architecture in Section 23.10.4.1, *USB Host Controller Functionality*.

The current subsystem does not support all dynamic USB speed negotiations, as expected from a standard USB host port at the same time. It supports:

- HS-only (with external HS physical layer [PHY]/HS TLL mode, or HSIC) on the EHCI
- FS-/LS-only (with external FS PHY/FS TLL mode) on the OHCI

The USB TLL module is the adapter on the host ports. It consists of two channels that are seen as emulating a pair of back-to-back PHYs and has:

- UTMI port, connected to the host controller module
- ULPI port, connected to a ULPI peripheral

The three HSIC digital front-ends (DFE) plug into the UTMI port of the host controller module and control HSIC-capable bidirectional I/O drivers driving the HSIC lines (strobe/data).

Figure 23-214 shows the HS USB host subsystem.

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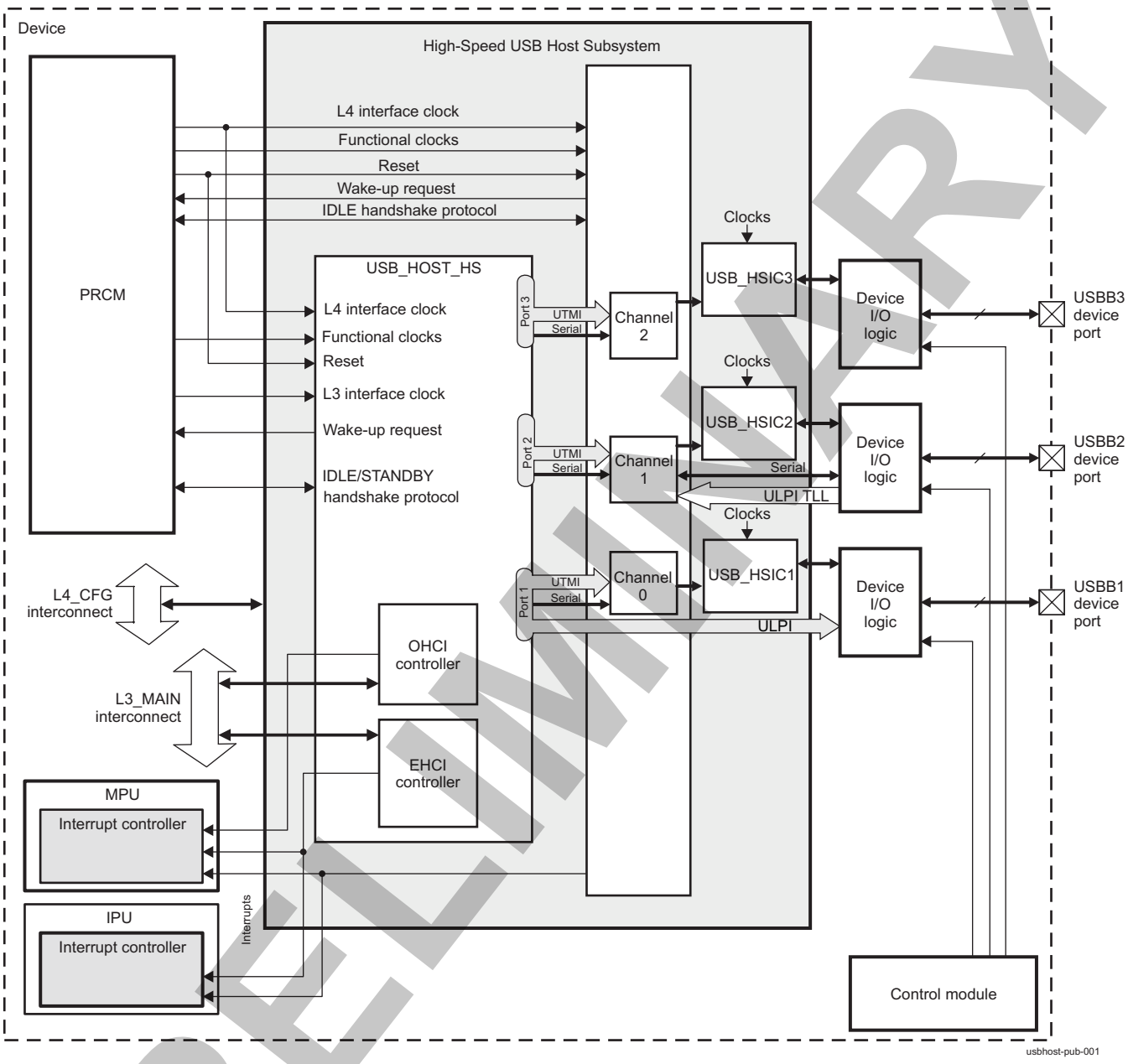
Figure 23-214. HS USB Host Subsystem Overview



23.10.1.1 Main Features

The HS multiport USB host subsystem supports the following features:

- **HS USB host controller module:**
  - One initiator on level 3 (L3)
  - One target on level 4 (L4)
  - Two IRQs
  - No DMA request
  - Implements a USB 2.0 HS host controller:
    - HS (480 Mbps) communication with HS USB peripherals or hubs
    - FS (12 Mbps) communication with FS USB peripherals or hubs

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- LS (1.5 Mbps) communication with LS USB peripherals

– Support for suspend, resume, remote wakeup
– Three downstream ports (3-port root hub)
– Heterogeneous port configuration (that is, different HS/FS PHYs with different clocking methods on different ports, supported simultaneously)
– Single FS host controller, compliant with OHCI software application programming interface (API), per-port power switching support
– Interface with UTMI PHYs (that is, the TLL module) on all ports (but only one is mapped on device balls)
  - 8-bit data path
  - Synchronous (on-chip) interface, independent clock input per port (that is, the TLL module provides clock to the host controller and to the remote USB controller).
  - HSIC front-end (after appropriate internal configuration)
– Interface with ULPI PHYs (external transceivers) on all ports (but only one is mapped on device balls)
  - 8-bit bidirectional data bus (SDR mode)
  - 12-pin interface
  - Independent clock input per port (ULPI PHY in output mode)
  - Supports only HS data transactions

NOTE: The HS USB host subsystem can support only the external charge pump of PHY (no support of internal charge pump for ULPI PHY).

– Interconnect initiator for built-in DMA operation of EHCI/OHCI
– Interconnect target for configuration
– Link power management (LPM) support in OHCI and EHCI hosts

- **USB TLL module:**
  – One interconnect target on L4
  – One IRQ
  – No DMA request
  – Three HS USB channels, each of them with four ports (A to D) (Not all C and D ports are mapped on device balls):
    - Port A: Host module UTMI+ port. Connects to the local link controller (host module). The UTMI "local" port is used in all configurations (that is, the entire channel can be seen as a protocol converted from that port to one of the other, "remote" ports. The port complies with UTMI+ version 1.0 and supports:
      - 8-data-bit, UTMI (HS/FS-capable)
      - UTMI+ L3 extensions
      - Vcontrol/Vstatus (from UTMI)
      - Serial FS 6-pin mode
    - Port B: Link-side UTMI+ port. Connects to HSIC front-end module.
    - Port C: PHY-side ULPI slave port. Connects to a remote (off-chip) ULPI link controller through I/O pads.
      - SDR ULPI mode (8-bit data width)
    - Port D: Serial multimode port.
      - Supports 6-pin unidirectional and 4-/3-/2-pin bidirectional modes
      - All modes are supported for TLL or PHY interface configuration, except 2-pin mode (which is TLL-only).
      - Supports sideband signals (pullup/down control, speed/suspend enable, etc.)

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- **HSIC module:** HSIC Digital Front-End (DFE) module is interfacing between:
  - one downstream port of a (multiport) HS link controller
    - 8-bit, 60 MHz UTMI
  - one set of bidirectional IOs (data + strobe)
    - HSIC electrical characteristics, as per *High Speed Inter-Chip (HSIC) Electrical Specification*
    - strobe is a 240 MHz clock-like signal
    - data is 480 Mbit/s, aligned with both strobe edges.

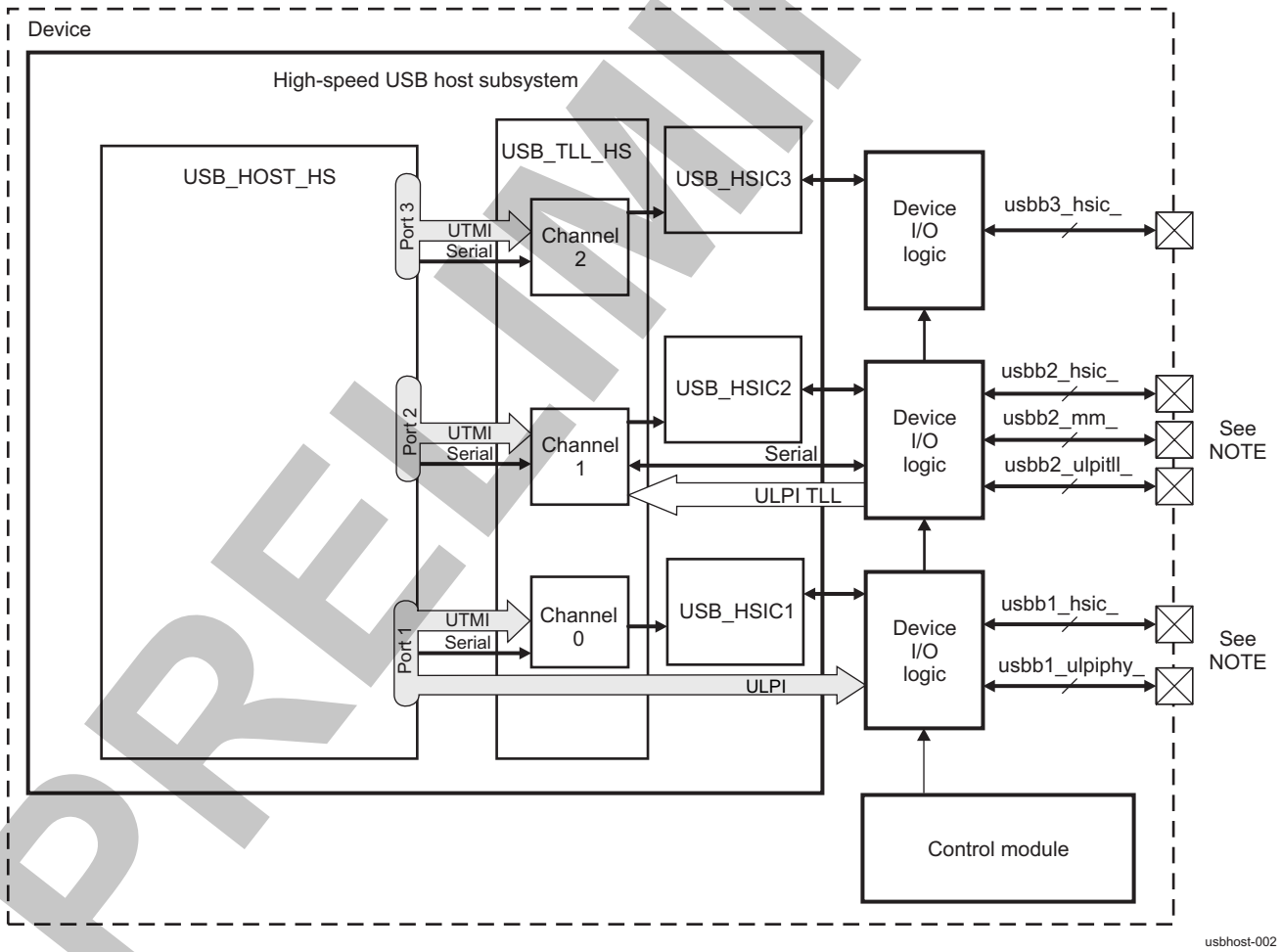
23.10.2 HS Multiport USB Host Subsystem Environment

The HS USB host subsystem provides three kinds of interfaces for connection:

- ULPIs for HS data transactions (up to 480 Mbps) (see Section 23.10.2.1, *ULPIs*)
- Serial interfaces, using the USB TLL module, for FS and LS data transactions (up to 12 Mbps) (see Section 23.10.2.2, *FS/LS Serial Interfaces*)
- HSIC interface to two HSIC lines over HSIC-capable I/O drivers (see Section 23.10.2.3, *HSIC Interface*)

Figure 23-215 is an overview of the environment of the HS USB host subsystem.

Figure 23-215. HS Multiport USB Host Subsystem Environment



NOTE: For more information about device-level signal names in different modes, see Section 23.10.2.1, *ULPIs*); Section 23.10.2.2, *FS/LS Serial Interfaces*; and Section 23.10.2.3, *HSIC Interface*.

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NOTE: Ports are configured independently and can be in different modes.

Even though all signals can be routed to independent device pads (that is, all port signals can be available simultaneously), port modes are mutually exclusive and are selected through USB Host controller and USB TLL module. See Section 23.10.5.2*Operational Modes Configuration (Selecting and Configuring USB Connectivity)*

For more information how the USB pins are multiplexed on device pads, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*.

23.10.2.1 ULPIs

The HS USB host subsystem supports the following configurations with the ULPIs:

- External USB transceiver:
  - ULPIs: 12-pin/8-bit data SDR version
- TLL:
  - SDR ULPI mode (12-pin/8-bit data width)

The HS USB host subsystem supports USB ports that use the ULPI mode to connect to an off-chip HS ULPI transceiver (12-pin/8-bit data SDR mode) for data transactions (up to 480 Mbps). FS and LS are not supported over the ULPI.

The device supports TLL logic interfaces on its ports in ULPI TLL interface mode. TLL modes enable glueless interconnect to another USB device port.

The external USB transceiver ULPIs and ULPI TLL interfaces cannot be used together on the same port. It is possible for one port to use ULPI and the other port to use ULPI TLL.

Figure 23-216 and Figure 23-217 show typical applications using the HS USB host subsystem with ULPI and the ULPI TLL interface, respectively.

Figure 23-216. External USB Transceiver ULPIs

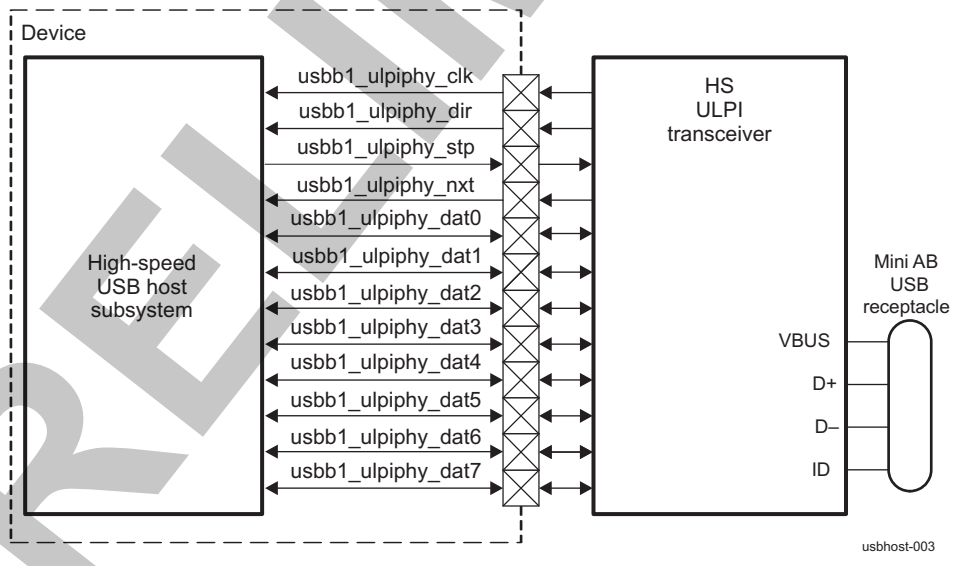

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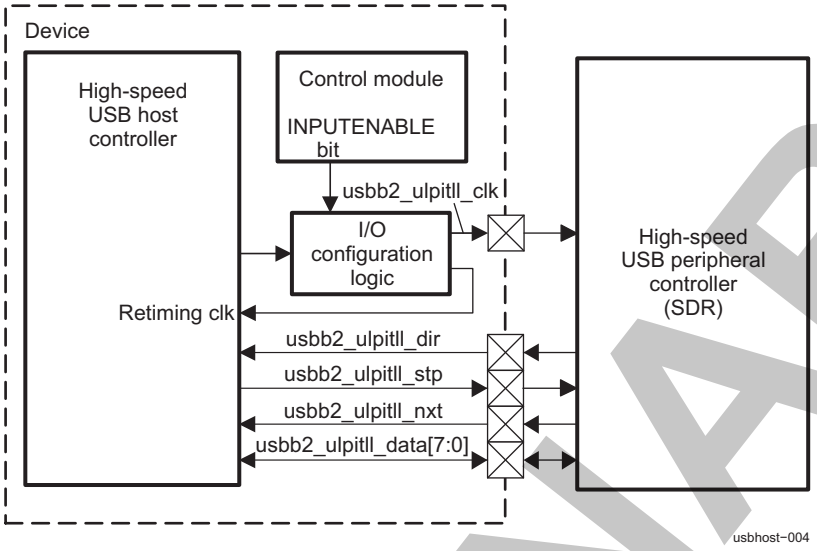
Figure 23-217. ULPI TLL Interfaces



The 12-pin ULPI uses an 8-bit data bus with data synchronous to the rising edge of the PHY (transceiver) clock (SDR mode).

NOTE: The recommended slew rate is not set by default and must be set in the respective CONTROL_SMART2IO_PADCONF_x registers. For more information, see Table 18-85 and Table 18-89 in Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*.

23.10.2.1.1 Transceiver Interface Configuration in ULPI Mode

The HS USB host subsystem supports only the 12-pin/8-bit data SDR version of the ULPI mode.

Figure 23-218 shows USB ports using the 12-pin/8-bit data SDR version of the ULPI mode.

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Figure 23-218. ULPIs – 12-Pin/8-Bit Data SDR Version

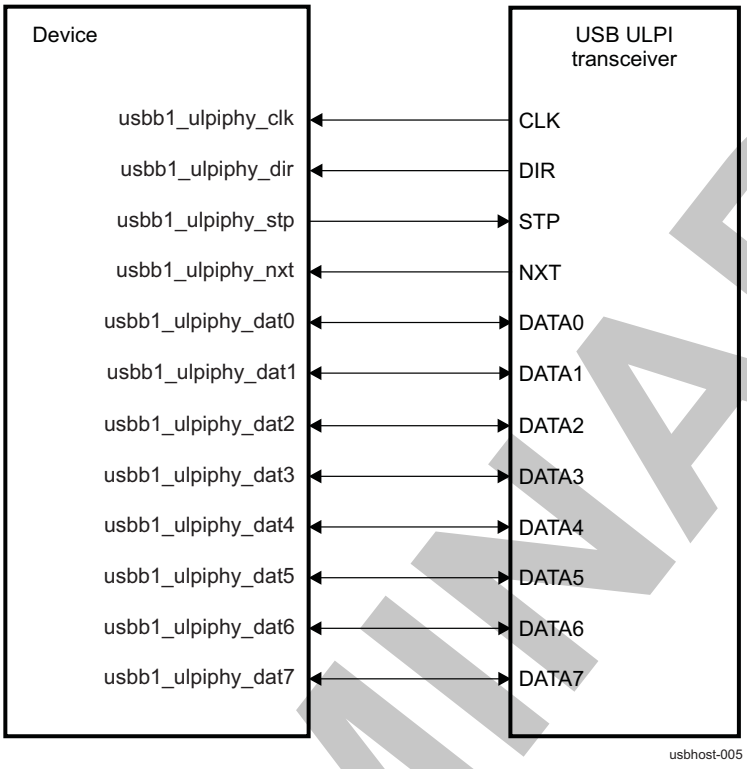

Table 23-826 describes the I/O pins of the USB ports using the 12-pin/8-bit data SDR version of the ULPI mode.

Table 23-826. ULPI – 12-Pin/8-Bit Data SDR Version I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value
HS USB Host Controller Port 1 (Device port USBB1)				
CLK	usbb1_ulpiphy_clk	I	Clock input from remote PHY IC	HiZ
DIR	usbb1_ulpiphy_dir	I	Data direction control from remote PHY IC	HiZ
STP	usbb1_ulpiphy_stp	O	Stop signal to remote PHY IC	1
NXT	usbb1_ulpiphy_nxt	I	Next signal from remote PHY IC	HiZ
DAT0	usbb1_ulpiphy_dat0	I/O	Bidirectional 8-bit data bus	HiZ
DAT1	usbb1_ulpiphy_dat1	I/O	Bidirectional 8-bit data bus	HiZ
DAT2	usbb1_ulpiphy_dat2	I/O	Bidirectional 8-bit data bus	HiZ
DAT3	usbb1_ulpiphy_dat3	I/O	Bidirectional 8-bit data bus	HiZ
DAT4	usbb1_ulpiphy_dat4	I/O	Bidirectional 8-bit data bus	HiZ
DAT5	usbb1_ulpiphy_dat5	I/O	Bidirectional 8-bit data bus	HiZ
DAT6	usbb1_ulpiphy_dat6	I/O	Bidirectional 8-bit data bus	HiZ
DAT7	usbb1_ulpiphy_dat7	I/O	Bidirectional 8-bit data bus	HiZ

(1) I = Input; O = Output

23.10.2.1.2 TLL Interface Configuration in ULPI Mode

The HS USB host controller is coupled with the USB TLL module to compose the ULPI TLL interface modes.

Figure 23-219 shows USB ports using the 12-pin/8-bit data SDR version of the ULPI TLL interface mode.

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Figure 23-219. ULPI TLL Interfaces – 12-Pin/8-Bit Data SDR Version

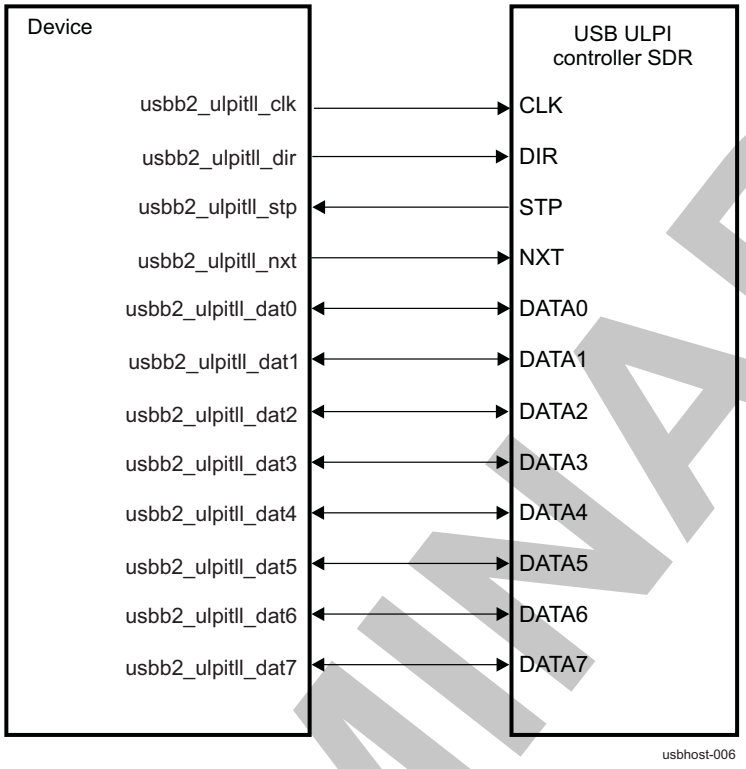

Table 23-827 describes the I/O pins of the USB ports using the 12-pin/8-bit data SDR version of the ULPI TLL interface mode.

Table 23-827. ULPI TLL Interface – 12-Pin/8-Bit Data SDR Version I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value
HS USB Host Controller Port 2 (Device port USBB2)				
CLK	usbb2_ulpitll_clk	O	Clock output to remote ULPI link controller [2]	0
DIR	usbb2_ulpitll_dir	O	Data direction control from remote ULPI link controller	0
STP	usbb2_ulpitll_stp	I	Stop signal to remote ULPI link controller	HiZ
NXT	usbb2_ulpitll_nxt	O	Next signal from remote ULPI link controller	0
DAT0	usbb2_ulpitll_dat0	I/O	Bidirectional 8-bit data bus	0
DAT1	usbb2_ulpitll_dat1	I/O	Bidirectional 8-bit data bus	0
DAT2	usbb2_ulpitll_dat2	I/O	Bidirectional 8-bit data bus	0
DAT3	usbb2_ulpitll_dat3	I/O	Bidirectional 8-bit data bus	0
DAT4	usbb2_ulpitll_dat4	I/O	Bidirectional 8-bit data bus	0
DAT5	usbb2_ulpitll_dat5	I/O	Bidirectional 8-bit data bus	0
DAT6	usbb2_ulpitll_dat6	I/O	Bidirectional 8-bit data bus	0
DAT7	usbb2_ulpitll_dat7	I/O	Bidirectional 8-bit data bus	0

(1) I = Input; O = Output

(2) This signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

23.10.2.2 FS/LS Serial Interfaces

The HS USB host subsystem supports the following configurations with the serial interfaces:

- External USB transceiver (see Section 23.10.2.2.3, *External USB Transceiver Interface Configurations in Serial Modes*)
  - Serial 6-pin PHY (transceiver) interfaces: 6-pin mode (TX: DAT/SE0 or TX: DP/DM unidirectional

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mode), 4-pin mode (DP/DM bidirectional mode), and 3-pin mode (DAT/SE0 bidirectional mode)

- TLL (see Section 23.10.2.2.4, *TLL Interface Configurations in Serial Modes*)
  - Serial 6-pin TLL interfaces: 6-pin mode (DAT/SE0 and DP/DM unidirectional modes), 4-pin mode (DP/DM bidirectional mode), 3-pin mode (DAT/SE0 bidirectional mode), and 2-pin mode (DAT/SE0 and DP/DM bidirectional modes)

CAUTION

Only FS and LS data transactions are possible in serial mode. Transceiver interface is serial (its frequency is that of the actual USB line) and combinatorial (no clock is passed).

Whether in TLL or external transceiver configuration, the serial interface follows the same principles: it is limited to FS/LS, and HS requires a parallel interface.

23.10.2.2.1 Encoding in Serial Mode

23.10.2.2.1.1 Unidirectional

When an external USB transceiver is connected to the device and is used in 6-pin unidirectional DAT/SE0 encoding mode, the encoding described in Table 23-828 is used.

Table 23-828. Signaling Between HS USB Host Subsystem and 6-Pin Unidirectional USB Transceiver (DAT/SE0 Signaling)

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description				
TXEN	Output	Input	When low, the USB transceiver drives D+ and D–.				
DAT and SE0	Output	Input	Controls the values output by the USB transceiver on D+ and D– when TXEN is low; ignored when TXEN is high.				
			TXEN	DAT	SE0	D+	D–
			0	0	0	0	1
			0	1	0	1	0
			0	X	1	0	0
			1	X	X	Undriven	Undriven
RCV	Input	Output	Output from transceiver differential receiver				
			D+	D–	RCV		
			0	0	X		
			0	1	0		
			1	0	1		
			1	1	X		
DP	Input	Output	Output from transceiver single-ended D+ signal receiver				
			D+	DP			
			0	0			
			1	1			
DM	Input	Output	Output from transceiver single-ended D- signal receiver				
			D–	DM			
			0	0			
			1	1			

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When an external USB transceiver is connected to the device and is used in 6-pin unidirectional DP/DM encoding mode, the encoding described in Table 23-829 is used.

Table 23-829. Signaling Between HS USB Host Subsystem and 6-Pin Unidirectional USB Transceiver (DP/DM Signaling)

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description				
TXEN	Output	Input	When low, the USB transceiver drives D+ and D–.				
DAT and SE0	Output	Input	Controls the values output by the USB transceiver on D+ and D– when TXEN is low; ignored when TXEN is high.				
			TXEN	DAT	SE0	D+	D–
			0	0	1	0	1
			0	1	0	1	0
			0	0	0	0	0
			1	X	X	Undriven	Undriven
RCV	Input	Output	Output from transceiver differential receiver				
			D+	D–	RCV		
			0	0	X		
			0	1	0		
			1	0	1		
			1	1	X		
DP	Input	Output	Output from transceiver single-ended D+ signal receiver				
			D+	DP			
			0	0			
			1	1			
DM	Input	Output	Output from transceiver single-ended D-signal receiver				
			D–	DM			
			0	0			
			1	1			

23.10.2.2.1.2 Bidirectional

When an external USB or USB OTG transceiver is connected to the device and is used in 3-pin bidirectional DAT/SE0 encoding mode, the encoding described in Table 23-830 is used.

Table 23-830. Signaling Between HS USB Host Subsystem and 3-Pin Bidirectional USB Transceiver Using DAT/SE0 Signaling

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description				
TXEN	Output	Input	When low, the USB transceiver drives D+ and D–.				
DAT and SE0	Output	Input	When TXEN is low, the device drives DAT and SE0 and the transceiver drives D+ and D– based on the values of DAT and SE0.				
	Output	Input	TXEN	DAT	SE0	D+	D–
			0	0	0	0	1
				1	0	1	0
				X	1	0	0
	Input	Output	TXEN	D+	D–	DAT	SE0
			1	0	0	0	1
				0	1	0	0
				1	0	1	0
				1	1	Undefined	0

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NOTE: The device does not support 3-wire bidirectional signaling using DP/DM signals.

When an external USB or USB OTG transceiver is connected to the device and is used in 4-pin bidirectional DP/DM encoding mode, the encoding described in Table 23-831 is used.

Table 23-831. Signaling Between HS USB Host Subsystem and 4-Pin Bidirectional USB Transceiver Using DP/DM Signaling

Logical Signal Name	Device Pin Direction	Transceiver Pin Direction	Description		
TXEN	Output	Input	When low, the USB transceiver drives D+ and D–.		
DM	Output	Input	Value driven to or received from D–		
			TXEN	DM	D–
			0	0	0
			0	1	1
	Input	Output	TXEN	D–	DM
			1	0	0
			1	1	1
DP	Output	Input	Value driven to or received from D+		
			TXEN	DP	D+
			0	0	0
			0	1	1
	Input	Output	TXEN	D+	DP
			1	0	0
			1	1	1
RCV	Input	Output	Output from transceiver differential receiver		
			D+	D–	RCV
			0	0	X
			0	1	0
			1	0	1
			1	1	X

23.10.2.2.2 Sideband Signals for Serial Modes

Serial interfaces carry only the USB data information. Sideband control and status (respectively, to/from the transceiver/TLL or to the bus lines themselves) require additional signals, which are usually implemented in a case-by-case, ad hoc way.

- Sideband control examples: FS/LS (slew rate control), transceiver suspend, connect (D+/D- pullup), pulldown enable, VBUS drive, etc.
- Sideband status example: VBUS level (VBUS valid, session valid, session end, etc.)
- Sideband signal implementations: Dedicated lines (one per sideband information bit), serial bus + interrupt line with register-mapped control/status (I^2C) UART, etc.)

Figure 23-220 and Figure 23-221 show system integration for sideband signals for two logically identical USB connections: one in transceiver configuration and one in TLL configuration. Although the sideband (purple) arrows are oriented from the controller to the transceiver in the two figures, the sideband information flow is bidirectional (that is, it flows from the controller to the transceiver [control] and from the transceiver to the controller [status]).

Figure 23-220 shows the transceiver configuration, where each side connects the sideband signals to its own transceiver. On the device (containing the USB TLL module), the sideband is decoded/re-encoded. The sideband signals available at the device boundary (and the USB TLL module) are decoded from the standard UTMI+ interface.

- The software-driven VBUS reporting procedure is described in Section 23.10.4.2.5.1.1, *VBUS*

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Management in Serial Transceiver Configurations.

Figure 23-220. Serial Interface Sideband Integration – Transceiver Configuration

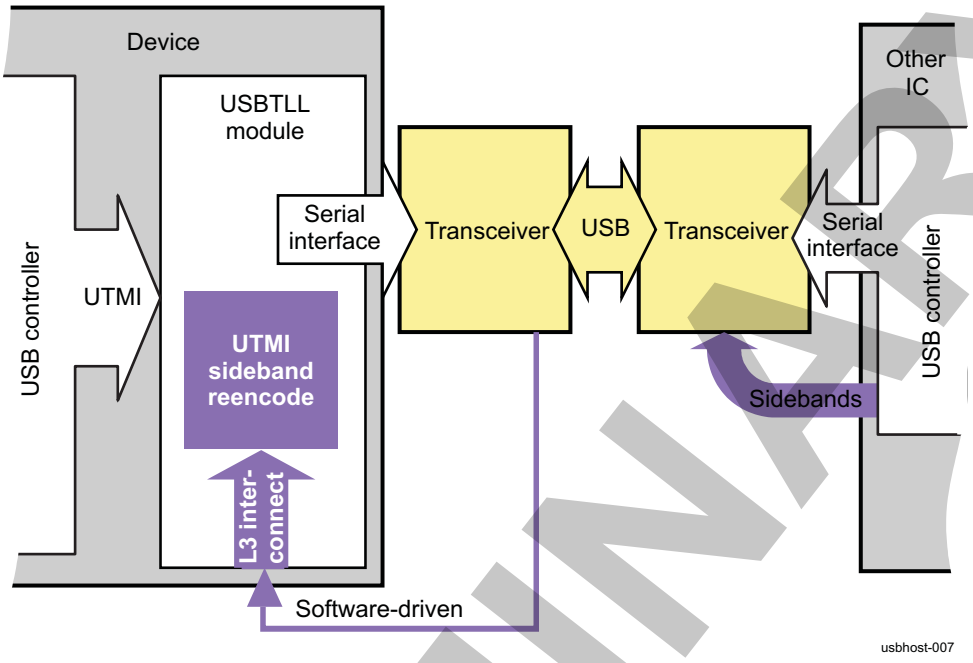

Figure 23-221 shows the TLL configuration, where both transceivers are emulated inside the USB TLL module.

- The transceiver of the local controller (left side of the figure) is working with the sideband information to/from the UTMI+ port. This is internal to the USB TLL module.
- The transceiver of the remote controller (right side of the figure) must communicate with its controller, which is on another IC. This is done in two ways:
  - The sideband input signals at the TLL module boundary (tllpuen, tlldrvvbus, tllvbusvalid, etc.)
  - The software-driven VBUS control procedure described in Section 23.10.4.2.5.2.2, *VBUS Emulation in Serial TLL Modes*)

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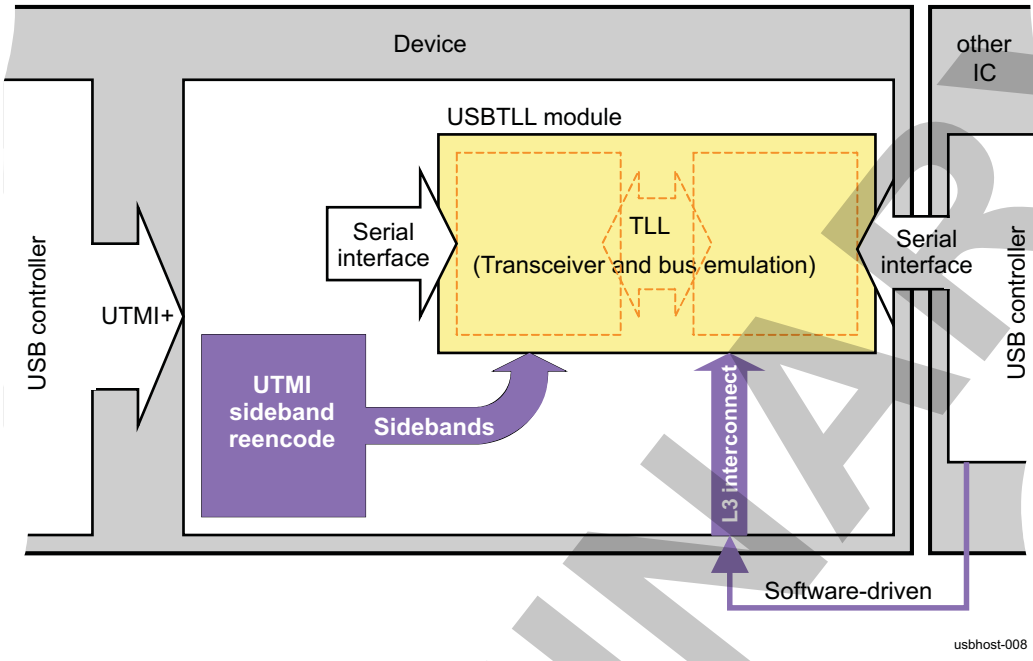
Figure 23-221. Serial Interface Sideband Integration – TLL Configuration



23.10.2.2.3 External USB Transceiver Interface Configurations in Serial Modes

An external USB transceiver is required for each USB port used in the system. It converts between appropriate signaling for the HS USB host subsystem and appropriate signaling for the USB wire.

The serial interface mode of the HS USB host subsystem includes support for several types of USB transceivers. It provides signaling to up to two external USB transceivers.

Several types of external transceiver signaling are supported. Signaling between the HS USB subsystem in serial interface mode and the external USB transceiver for monitoring and controlling the differential USB signal can be done through a 6-, 4-, or 3-wire signaling interface, with two or more control signals provided by additional signals or through an I^2C link.

The following subsections describe the transceiver interface modes supported by the HS USB host subsystem in the serial interface mode. In each case, the subsystem is connected to external transceivers, on the other side of the USB lines (D+/D–).

23.10.2.2.3.1 Unidirectional Transceiver Interface Modes: 6-Pin

The 6-pin modes are the "natural" transceiver interface modes for the FS transceivers in the sense that they mirror the internal makeup of the transceivers.

Two encodings exist for TX: DAT/SE0 and DP/DM.

When an external USB is connected to the device and is used in 6-pin unidirectional DAT/SE0 signaling mode, the signaling described in Table 23-828 is used.

Figure 23-222 shows a USB port using DAT/SE0 encoding.

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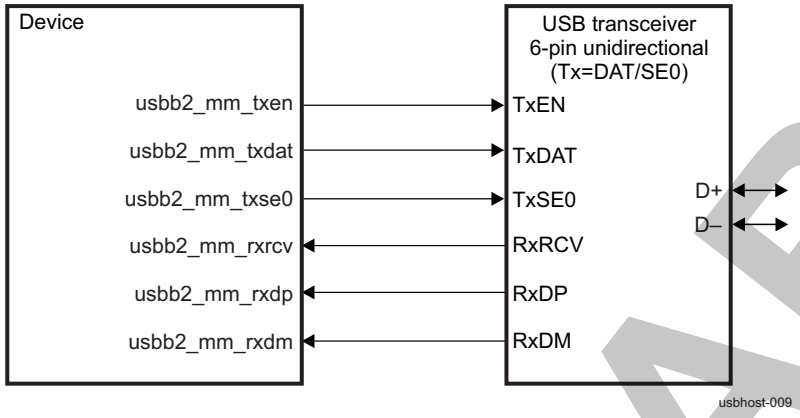
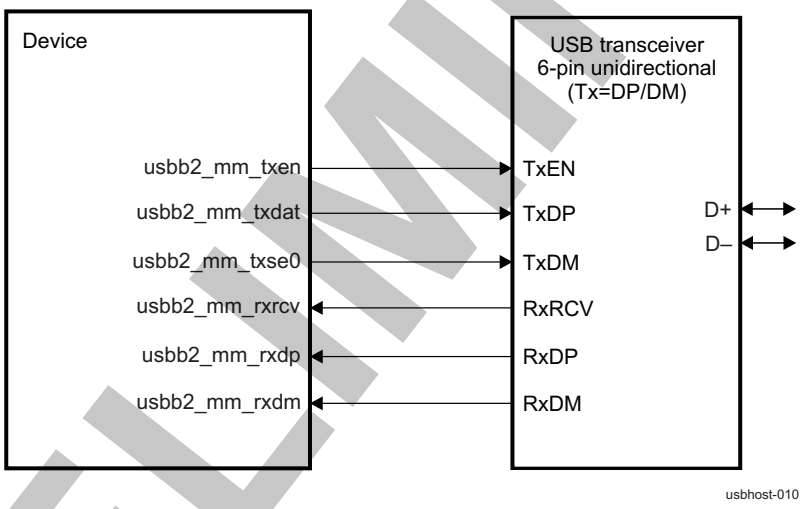
Figure 23-222. 6-Pin Unidirectional Using DAT/SE0 Signaling



When a USB is connected to the device and is used in 6-pin unidirectional DP/DM signaling mode, the signaling described in Table 23-829 is used.

Figure 23-223 shows a USB port using DP/DM encoding.

Figure 23-223. 6-Pin Unidirectional Using DP/DM Signaling



23.10.2.2.3.2 Bidirectional Transceiver Interface Modes: 3-Pin, 4-Pin

The bidirectional transceiver interface modes are pin-count optimizations of the unidirectional modes. They take advantage of the fact that a USB port is sending or receiving at any given time, but never both. The TX and RX paths of the unidirectional mode can be multiplexed on bidirectional lines. To prevent glitches at TX/RX turnaround, the same encoding is used for both directions (DAT/SE0 or DP/DM).

The signaling described in Table 23-830 is used when a USB transceiver is connected to the device and is used in 3-pin bidirectional DAT/SE0 signaling mode.

NOTE: The device does not support 3-wire bidirectional signaling using DP/DM signals.

Figure 23-224 shows a USB port using DAT/SE0 encoding.

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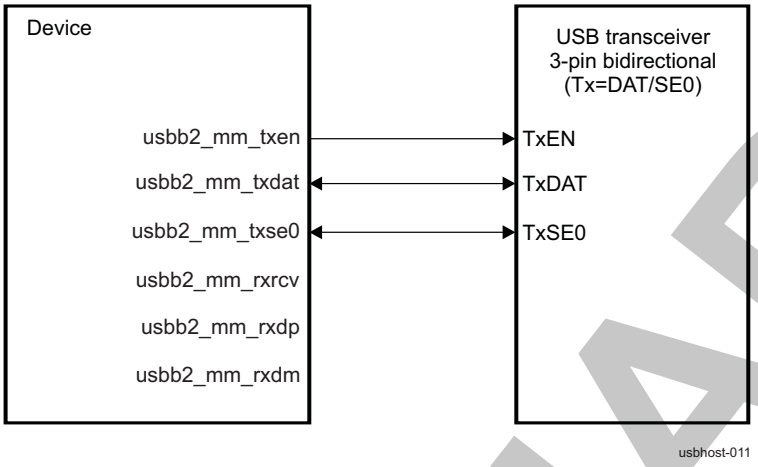
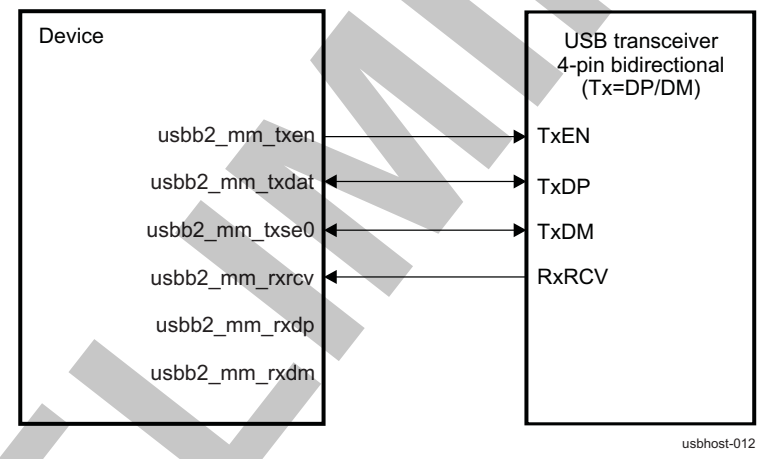
Figure 23-224. 3-Pin Bidirectional Using DAT/SE0 Signaling



The signaling described in Table 23-831 is used when a USB transceiver is connected to the device and is used in 4-pin bidirectional DP/DM signaling mode.

Figure 23-225 shows a USB port using DP/DM encoding.

Figure 23-225. 4-Pin Bidirectional Using DP/DM Signaling



23.10.2.2.4 TLL Interface Configurations in Serial Modes

The HS USB host subsystem supports unidirectional and bidirectional TLL logic interfaces on its ports. The TLL modes enable glueless interconnect to the USB device port of another device without needing a costly transceiver.

Serial interface modes are FS or LS only. Transceiver interface is serial (its frequency is that of the actual USB line) and combinatorial (no clock is passed).

23.10.2.2.4.1 Unidirectional TLL Serial Modes

The 6-pin TLL configurations are mirror images of the 6-pin transceiver configurations previously discussed. The same signals are mapped on the same physical pins, but in opposite directions.

Two possible modes exist, depending on the TX data encoding used by the external device.

Figure 23-226 shows an external device using DAT/SE0 encoding.

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Figure 23-226. 6-Pin Unidirectional TLL Using DAT/SE0 Signaling

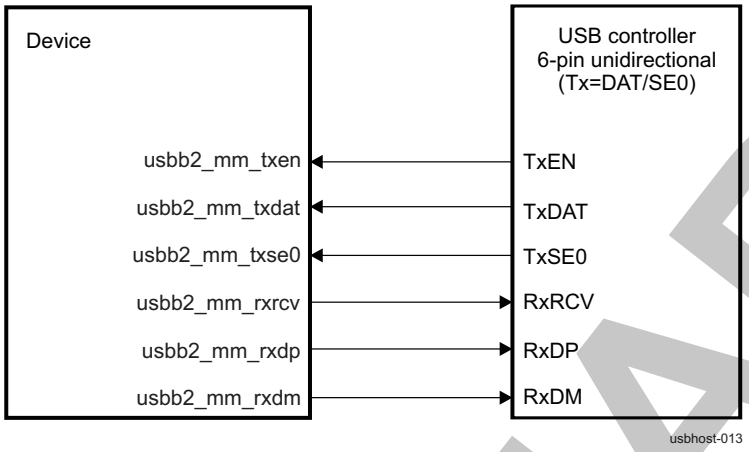
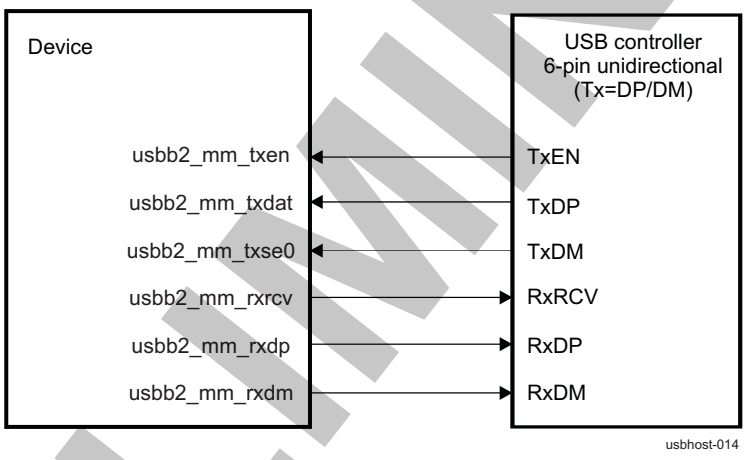


Figure 23-227 shows an external device using DP/DM encoding.

Figure 23-227. 6-Pin Unidirectional TLL Using DP/DM Signaling



23.10.2.2.4.2 Bidirectional TLL Serial Modes

The 3-pin/4-pin TLL configurations are mirror images of the 3-pin/4-pin transceiver configurations previously discussed. The same signals are mapped on the same physical pins, but in opposite directions (bidirectional lines remain bidirectional).

Two possible modes exist, depending on the TX data encoding used by the external device.

Figure 23-228 shows an external device using DAT/SE0 encoding.

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Figure 23-228. 3-Pin Bidirectional TLL Using DAT/SE0 Signaling

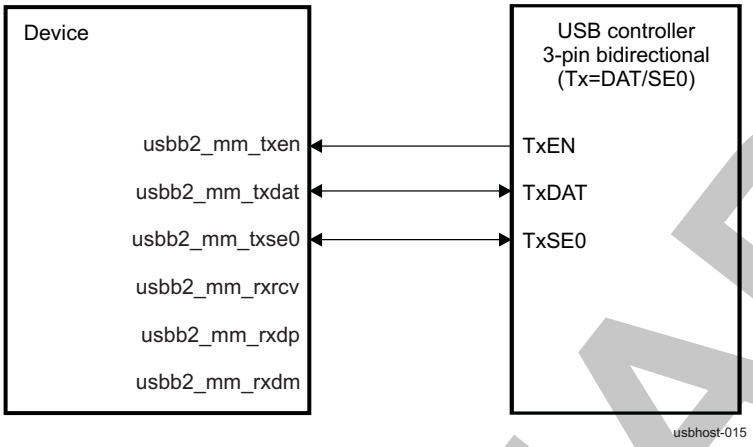
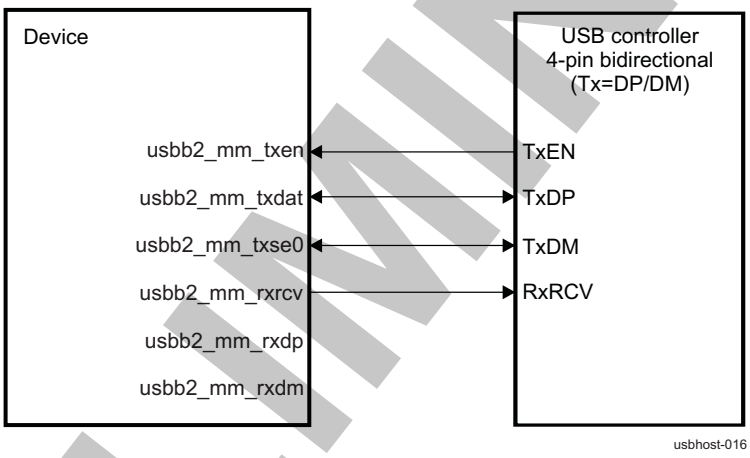


Figure 23-229 shows an external device using DP/DM encoding.

Figure 23-229. 4-Pin Bidirectional TLL Using DP/DM Signaling



The 2-pin TLL configurations have unique specifications:

- They require pullups/pulldowns to operate, because the bidirectional lines are not driven at all times like the other serial transceiver interfaces described previously. The connection of pull resistors depends on the speed of the controller.
- The module supports explicit 2-pin TLL modes, with DAT/SE0 or DP/DM encoding.
- Non-TLL modes (that is, transceiver configuration mode) can be used to implement the 2-pin functionality, using a specific connectivity.

Figure 23-230 shows a USB port using DP/DM encoding.

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Figure 23-230. 2-Pin Bidirectional TLL Using DP/DM Encoding, With 4-Pin Bidirectional USB Device

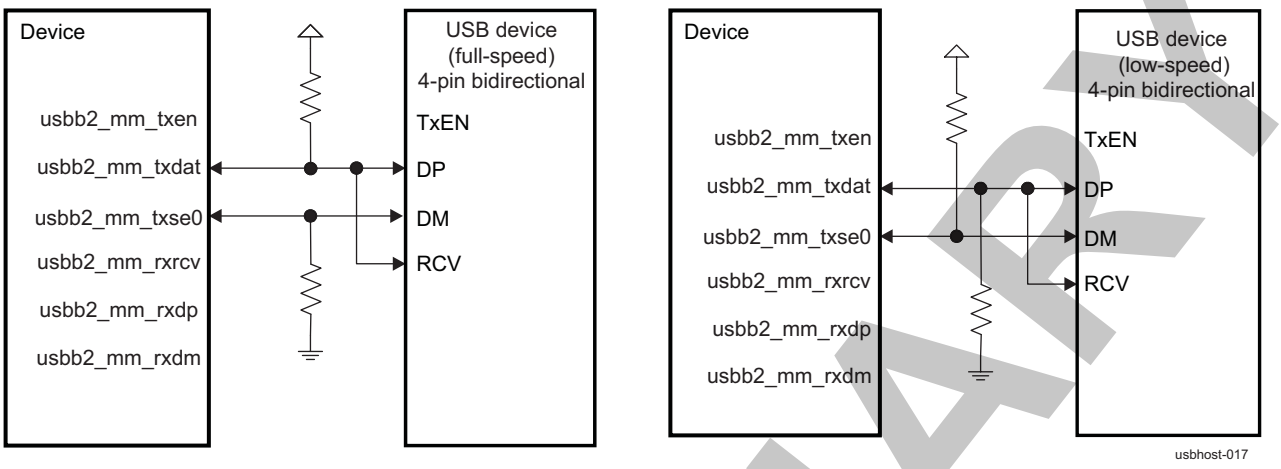

Table 23-832 shows the pullup/pulldown configuration for DP/DM encoding.

Table 23-832. Pullup/Pulldown Configuration for DP/DM Encoding

	Nonconnected Device (Any Speed)	Connected LS Device	Connected FS Device
DP	Pulldown	Pulldown	Pullup
DM	Pulldown	Pullup	Pulldown

Figure 23-231 shows a USB port using DAT/SE0 encoding.

Figure 23-231. 2-Pin Bidirectional TLL Using DAT/SE0 Encoding, With 3-Pin Bidirectional USB Device

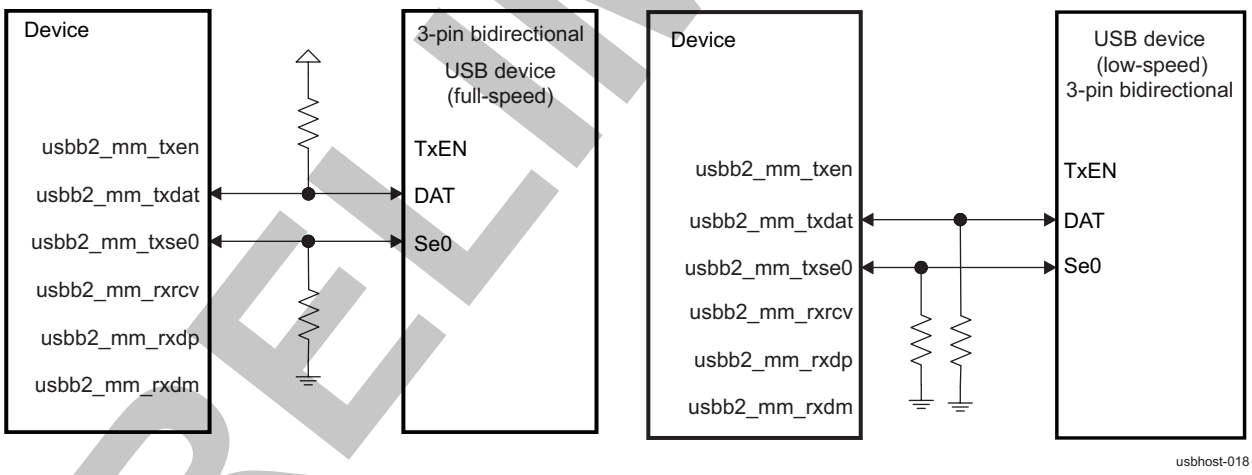

Table 23-833 shows the pullup/pulldown configuration for DAT/SE0 encoding.

Table 23-833. Pullup/Pulldown Configuration for DAT/SE0 Encoding

	Nonconnected Device (Any Speed)	Connected LS Device	Connected FS Device
DAT	Pulldown	Pulldown	Pullup
SE0	Pullup	Pulldown	Pulldown

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23.10.2.2.5 Interface Description in Serial Modes

Table 23-834 describes the I/O of the HS USB host subsystem serial interface.

Table 23-834. Multiple-Mode FS/LS Serial Interface I/O Description

Device Signal Name	I/O[1]	Description	Value at Reset
HS USB Host Controller Port 2 (Device port USBB2)			
usbb2_mm_txse0	I/O	SE0 function in 3-pin bidirectional DAT/SE0 mode	0
	I/O	DM function in 4-pin bidirectional DP/DM mode	
	O	SE0 output in 6-pin unidirectional DAT/SE0 mode	
	O	DM output in 6-pin unidirectional DP/DM mode	
	I/O	SE0-TLL in 2-/3-pin bidirectional DAT/SE0 TLL mode	
	I/O	DM-TLL in 2-/4-pin bidirectional DP/DM TLL mode	
	I	SE0-TLL input in 6-pin unidirectional DAT/SE0 TLL mode	
	I	DM-TLL input in 6-pin unidirectional DP/DM TLL mode	
usbb2_mm_txdat	I/O	DAT function in 3-pin bidirectional DAT/SE0 mode	HiZ
	I/O	DP function in 4-pin bidirectional DP/DM mode	
	O	DAT output in 6-pin unidirectional DAT/SE0 mode	
	O	DP output in 6-pin unidirectional DAT/SE0 mode	
	I/O	DAT-TLL in 2-/3-pin bidirectional DAT/SE0 TLL mode	
	I/O	DP-TLL in 2-/4-pin bidirectional DP/DM TLL mode	
	I	DAT-TLL input in 6-pin unidirectional DAT/SE0 TLL mode	
	I	DP-TLL input in 6-pin unidirectional DP/DM TLL mode	
usbb2_mm_txen	O	Transmit enable in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM or 6-pin unidirectional modes	1
	I	Transmit enable in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 6-pin unidirectional TLL modes (not used in 2-pin bidirectional TLL modes)	
usbb2_mm_rxrcv	I	Differential receiver signal input in 4-pin bidirectional DP/DM or 6-pin unidirectional modes (not used in 3-pin bidirectional DAT/SE0 mode)	HiZ
	O	Differential receiver signal output in the 4-pin bidirectional DP/DM TLL or 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 2-pin bidirectional TLL modes)	
usbb2_mm_rxdp	I	Single-ended DP receiver signal input in 6-pin unidirectional modes (not used in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM modes)	HiZ
	O	Single-ended DP receiver signal output in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 2-pin bidirectional TLL modes)	
usbb2_mm_rxdm	I	Single-ended DM receiver signal input in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM or 2-pin bidirectional TLL modes)	HiZ
	O	Single-ended DM receiver signal output in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 2-pin bidirectional TLL modes)	

[1] I = Input; O = Output

NOTE: ULPI (PHY) interfaces and ULPI TLL interfaces cannot be used together: either the ULPI (PHY) interfaces or the ULPI TLL interfaces are selected

23.10.2.3 HSIC Interface

The HS USB host subsystem supports the configurations with the HSIC interfaces shown in Figure 23-232.

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Figure 23-232. HSIC Interface

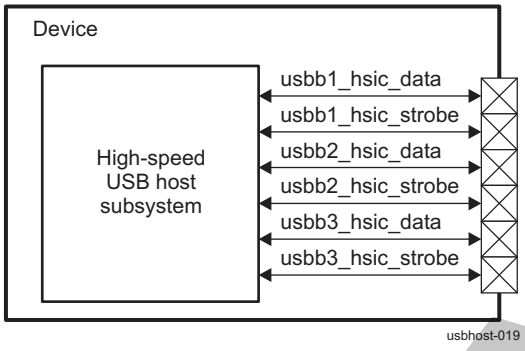

Table 23-835 describes the I/O of the HSIC interface of the HS USB host subsystem.

Table 23-835. HSIC Interface I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value
HS USB Host Controller Port 1 (Device port USBB1)				
DATA	usbb1_hsic_data	I/O	HSIC1 module data signal	HiZ
STROBE	usbb1_hsic_strobe	I/O	HSIC1 module strobe signal	HiZ
HS USB Host Controller Port 2 (Device port USBB2)				
DATA	usbb2_hsic_data	I/O	HSIC2 module data signal	HiZ
STROBE	usbb2_hsic_strobe	I/O	HSIC2 module strobe signal	HiZ
HS USB Host Controller Port 3 (Device port USBB3)				
DATA	usbb3_hsic_data	I/O	HSIC3 module data signal	HiZ
STROBE	usbb3_hsic_strobe	I/O	HSIC3 module strobe signal	HiZ

(1) I = Input; O = Output

23.10.3 HS Multiport USB Host Subsystem Integration

This section describes the integration of the HS USB host subsystem, including information about clocks, resets, and hardware requests.

The USB host controller module includes other modules and additional logic attached to the UTMI/ULPI ports. The HS USB host controller is connected to the L3 interconnect master (initiator) and L4_CFG interconnect slave (target) interfaces.

The elements of the USB HS host subsystem are:

- The multiport USB host controller. Each port uses one of the following modes:
  - ULPI, to a ULPI PHY (typically, off-chip)
  - UTMI, to a local UTMI (typically, on-chip) PHY or emulation of a PHY
- A local phase-locked loop (PLL), able to provide the USB-grade 48-, 60-, 480-MHz clocks
- Three TLL channels, bundled inside a USB TLL module. Each HS TLL channel can be seen as emulating a pair of back-to-back PHYs, and has:
  - A UTMI port, connected to a controller port (the host, in this case)
  - A ULPI port, connected to a (typically, off-chip) ULPI controller (peripheral, in this case)
- Three HSIC DFEs. The DFE plugs into the UTMI port of an HSIC-capable controller (the host, in this case), and controls HSIC-capable bidirectional I/O drivers driving the HSIC lines (strobe/data).

Figure 23-233 shows the HS USB subsystem integration.

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Figure 23-233. HS USB Subsystem Integration

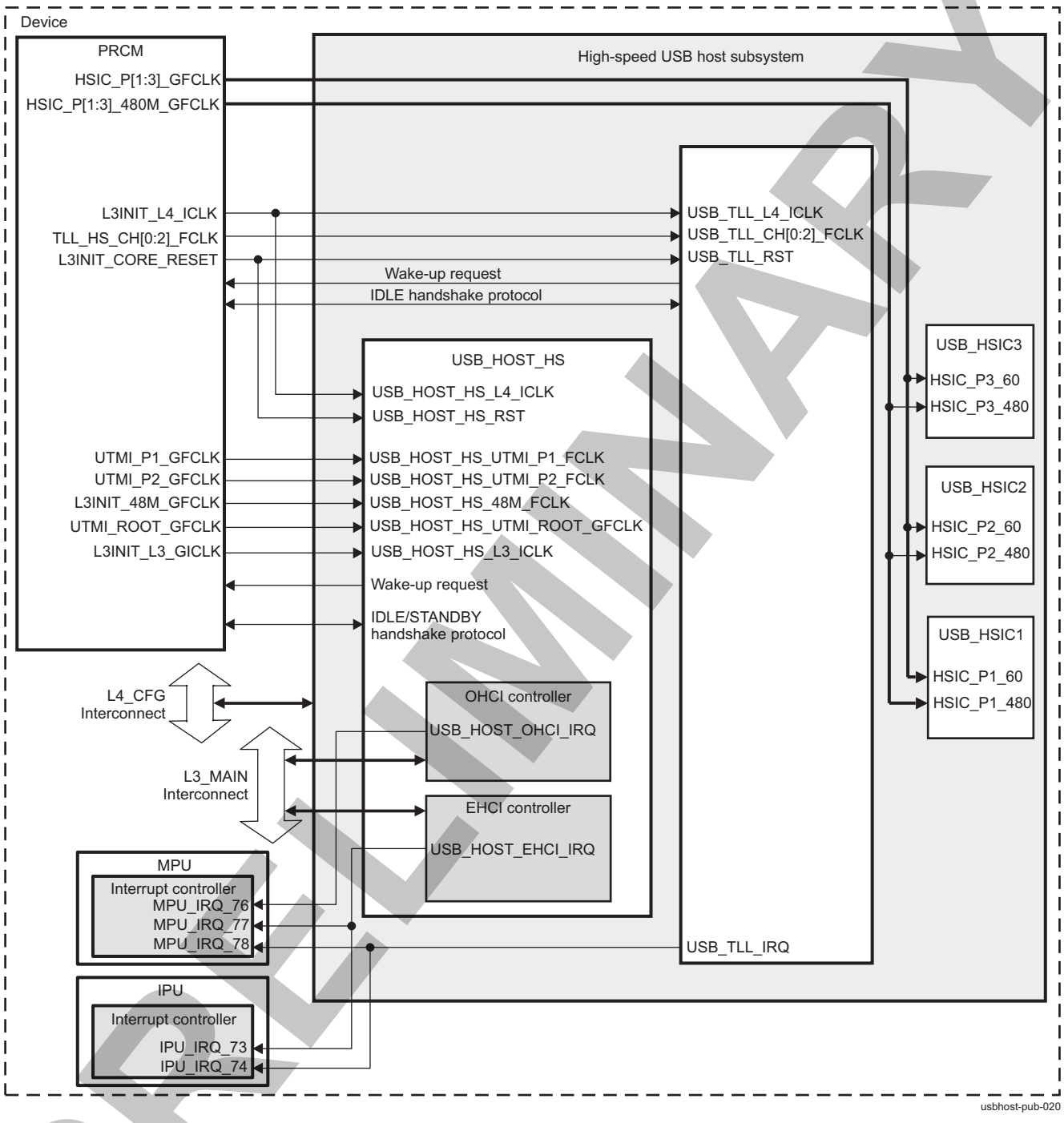

Table 23-836 through Table 23-838 summarize the integration of the module in the device.

Table 23-836. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
USB_HOST_HS	L3INIT	L3_MAIN L4_CFG
USB_TLL_HS	L3INIT	L4_CFG

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Table 23-837. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
USB_HOST_HS	USB_HOST_HS_L4_ICLK	L3INIT_L4_ICLK	PRCM	L4 interconnect enable signal for the slave interface on L4 (see Section 3.6.3.2)
	USB_HOST_HS_L3_ICLK	L3INIT_L3_ICLK	PRCM	L3 interconnect clock for the L3 master port interface (see Section 3.6.10)
	USB_HOST_HS_UTMI_P1_FCLK	UTMI_P1_GFCLK	PRCM	Port 1 UTMI interface functional clock (see Section 3.6.10 and Section 3.6.3.2.2)
	USB_HOST_HS_UTMI_P2_FCLK	UTMI_P2_GFCLK/usbb2_ulpiphy_clk	PRCM/external PHY IC	Port 2 UTMI interface functional clock (see Section 3.6.10 and Section 3.6.3.2.2)
	USB_HOST_HS_INIT_48M_FCLK	INIT_48M_GFCLK	PRCM	48-MHz functional clock for OHCI and EHCI (see Section 3.6.10)
	USB_HOST_HS_UTMI_ROOT_GFCLK	UTMI_ROOT_GFCLK	PRCM	60-MHz root hub clock (see Section 3.6.10)
USB_HSIC1	HSIC_P1_60	HSIC_P1_GFCLK	PRCM	60-MHz clock for the USB HSIC 1 (see Section 3.6.10)
	HSIC_P1_480	HSIC_P1_480M_GFCLK	PRCM	480-MHz clock for the USB HSIC 1(see Section 3.6.10)
USB_HSIC2	HSIC_P2_60	HSIC_P2_GFCLK	PRCM	60-MHz clock for the USB HSIC 2(see Section 3.6.10)
	HSIC_P2_480	HSIC_P2_480M_GFCLK	PRCM	480-MHz clock for the USB HSIC 2(see Section 3.6.10)
USB_HSIC3	HSIC_P3_60	HSIC_P3_GFCLK	PRCM	60-MHz clock for the USB HSIC 3 (see Section 3.6.10)
	HSIC_P3_480	HSIC_P3_480M_GFCLK	PRCM	480-MHz clock for the USB HSIC 3(see Section 3.6.10)
USB_TLL_HS	HS_USB_HOST_INIT_L4_ICLK	INIT_L4_ICLK	PRCM	L4 interconnect enable signal for the slave interface on L4 (see Section 3.6.3.2)
	TLL_CH0_FCLK	TLL_CH0_FCLK	PRCM	Functional clock for channel 0 (see Section 3.6.10)
	TLL_CH1_FCLK	TLL_CH1_FCLK	PRCM	Functional clock for channel 1 (see Section 3.6.10)
	TLL_CH2_FCLK	TLL_CH2_FCLK	PRCM	Functional clock for channel 2 (see Section 3.6.10)
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
USB_HOST_HS	USB_HOST_HS_RST	L3INIT_CORE_RST	PRCM	The signal resets the USB_HOST_HS module.
USB_TLL_HS	USB_TLL_HS_RST	L3INIT_CORE_RST	PRCM	The signal resets the USB_TLL_HS module.

Table 23-838. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
USB_HOST_HS	USB_HOST_EHCI_IRQ	MPU_IRQ_77	MPU INTC	Destination is MPU interrupt controller (INTC).
		IPU_IRQ_73	IPU INTC	Destination is IPU INTC.
	USB_HOST_OHCI_IRQ	MPU_IRQ_76	MPU INTC	Destination is MPU INTC.
USB_TLL_HS	USB_TLL_IRQ	MPU_IRQ_78	MPU INTC	Destination is MPU INTC.
		IPU_IRQ_74	IPU INTC	Destination is Cortex-M3 INTC.

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The HS USB host controller and TLL module are attached to the CORE reset domain. The L3INIT_CORE_RST signal resets the HS USB host controller and TLL module (see Chapter 3, *Power, Reset, and Clock Management*).

23.10.4 HS Multiport USB Host Subsystem Functional Description

This section describes the functionality of the HS USB host subsystem by describing the HS USB host controller, USB TLL module.

23.10.4.1 USB Host Controller Functionality

The full details of the standard OHCI and EHCI host controller APIs (implemented by the current module) are not repeated here. For more information, see the following specifications:

- *Open Host Controller Interface (OHCI) Specification for USB Release 1.0a*
- *Enhanced Host Controller Interface (EHCI) Specification for USB Release 1.1*

Figure 23-234 is an overview of the HS USB host controller internal architecture. It contains two independent, 3-port host controllers (OHCI and EHCI) that operate in parallel.

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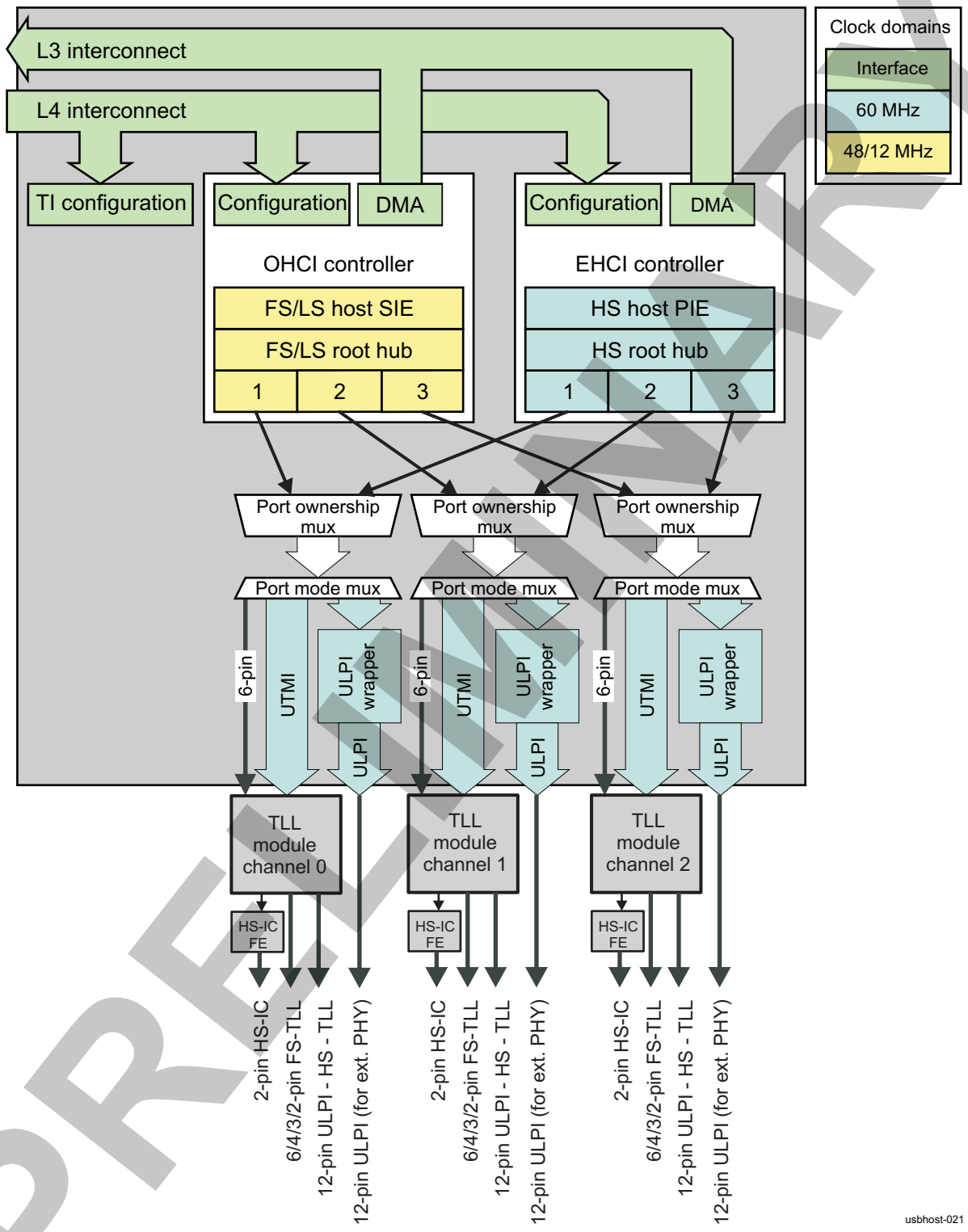
Figure 23-234. HS USB Host Controller Internal Architecture



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23.10.4.1.1 HS USB Host Controller Software Reset

The HS USB host controller has its own software-reset function through the UHH_SYSCONFIG[0] SOFTRESET bit. Setting this bit to 0x1 resets the HS USB host controller. The bit value of 0x1 remains until the reset completes. When the software reset completes, the SOFTRESET bit is automatically set to 0x0 and has the same effect as the hardware reset.

23.10.4.1.2 HS USB Host Controller Power Management

The USB protocol defines power-saving modes, where clocks can be shut down. The host asynchronously detects ULPI/UTMI events and asserts the wake-up output, which causes the clocks to restart.

To reduce dynamic power consumption, an efficient idle scheme in the device is based on:

- Efficient local autoclock gating for each module
- Implementation of control sideband signals between the PRCM module and each module

This enhanced idle control allows clocks to be activated and deactivated safely without complex software intervention. In both cases, the HS USB host controller power management is applied only to the interface clock domain.

The HS USB host controller has master (initiator) and slave (target) interfaces:

- As an initiator, the HS USB host controller implements the standby handshake protocol to inform the PRCM module when it enters standby mode and does not generate traffic on the interconnect.
- As a target, the HS USB host controller implements the IDLE handshake protocol to allow the PRCM module requiring it to enter idle mode.

NOTE: When the ULPI PHY interface is used and a FS/LS device is connected and suspended, the host controller places the ULPI interface in a mode where the ULPI clock (provided to OMAP by the external discrete USB PHY) is stopped.

23.10.4.1.2.1 Standby Handshake Protocol

The HS USB host controller can go into standby mode, in which case it stops generating transactions on the interconnect. To save power, the module standby leads the PRCM module to disable the USB clocks.

The HS USB host controller has an Mstandby/Mwait handshake mechanism with the PRCM module (see Chapter 3, *Power, Reset, and Clock Management*).

The module is ready to enter standby mode (indicated by the Mstandby signal to the PRCM module asserted) when there is no USB activity and the module is idle. It means:

- The module is committed not to start any new transaction on its master interface.
- The whole module is idle and, therefore, the power manager can start the procedure to turn off the interface clock, if needed. This procedure must be implemented using the slave power-management protocol.

The handshake mechanism lets the module go into standby mode based on the UHH_SYSCONFIG[5:4] STANDBYMODE bit field.

Table 23-839 lists the settings of standby mode.

Table 23-839. HS USB Host Controller Standby Mode Settings

MIDLEMODE Value	Selected Mode	Description
0x0	Force-standby	The HS USB host controller enters standby mode unconditionally (Mstandby is asserted unconditionally).
0x1	No-standby	The HS USB host controller never enters standby mode (Mstandby is never asserted).
0x2	Smart-standby	The HS USB host controller is ready to enter standby mode (Mstandby is asserted) when there is no more activity on the USB master interface of the interconnect.

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Table 23-839. HS USB Host Controller Standby Mode Settings (continued)

MIDLEMODE Value	Selected Mode	Description
0x3	Smart-standby + wakeup	The HS USB host controller enters smart mode with asynchronous (master) wakeup enabled.

23.10.4.1.2.2 IDLE Handshake Protocol

The PRCM module handles an IDLE handshake protocol for the HS USB host controller. The IDLE handshake protocol lets the PRCM module requiring the HS USB host controller to enter idle mode. Although this handshake is completely hardware and out of any software control, the way in which the HS USB host controller acknowledges the PRCM IDLE request is configurable through the UHH_SYSCONFIG[3:2] SIDLEMODE bit field. Table 23-840 lists the settings of SIDLEMODE and the related acknowledgment modes.

Table 23-840. HS USB Host Controller SIDLEMODE Settings

SIDLEMODE Value	Selected Mode	Description
0x0	Force-idle	The HS USB host controller acknowledges unconditionally the IDLE request from the PRCM module, regardless of its internal operations. Because such a mode does not prevent the loss of data when the clock is switched off, the mode must be used carefully.
0x1	No-idle	The HS USB host controller never acknowledges any IDLE request from the PRCM module. This mode is safe from a module point of view because it ensures the clocks remain active; however, it is not efficient from a power-saving perspective because it does not allow the PRCM output clock to be shut off, and thus the power domain to be set to a lower power state.
0x2	Smart-idle	The HS USB host controller acknowledges the IDLE request basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions, IRQs, or DMA requests are treated. This is the best approach for an efficient system power management.
0x3	Smart-idle + wakeup	The HS USB host controller enters smart mode with asynchronous (master) wakeup enabled.

23.10.4.1.2.3 Wake-Up Request

The wake-up request signal USBHOST_SWAKEUP is generated by the HS USB host controller to the PRCM module.

23.10.4.1.3 HS USB Host Controller Port Status

The USB port status is given through the UHH_HOSTCONFIG[8] P1_CONNECT_STATUS, [9] P2_CONNECT_STATUS, and [10] P3_CONNECT_STATUS bits. The default value of these bits is 0x0 indicating that peripheral is disconnected.

23.10.4.1.4 HS USB Host Controller Burst Control

To avoid buffer underflow, bursts must be enabled by setting the UHH_HOSTCONFIG[4:2] bit field to 0x7, and the UHH_HOSTCONFIG[5] ENA_INCR_ALIGN bit to 1.

23.10.4.1.5 OHCI Implementation Specifications

Some features of the OHCI API are optional and/or implementation-specific. The choices made in the current implementation, the HS USB host controller, are described in the following list and are reflected in the register descriptions (see Section 23.10.6.5, *OHCI Registers*). For all standard features, see the *Open Host Controller Interface (OHCI) Specification for USB Release 1.0a*.

- HCFMINTERVAL[30:16] FSMPS bit field (FullSpeedMaxPacketSize) = 0x0000: The host stops scheduling new packets 0 bit times before the end of the frame (that is, by default, there is no scheduling overrun protection). To be updated by the software driver.
- HCRHDESCRIPTORA[7:0] NDP bit field (NumberDownstreamPorts) = 0x03 = three ports

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- HCRHDESCRIPTORA[9] NPS bit (NoPowerSwitching) = 0: Ports are power-switched by default.
- HCRHDESCRIPTORA[8] PSM bit (PowerSwitchingMode) = 1: Per-port power switching is supported, although PPCM default setup has all ports controlled globally.
- HCRHDESCRIPTORA[31:24] POTPG bit field (PowerOnToPowerGood) = 0x0A = 10: Power ramp-up time is 10 x 2 ms = 20 ms.
- HCRHDESCRIPTORB[15:0] DR bit field (DeviceRemovable) = 0x0000: By default, no nonremovable devices (that is, devices attached to any of the ports) are removable.
- HCRHDESCRIPTORB[31:16] PPCM bit field (PortPowerControlMask) = 0x0000: By default, all ports are affected only by global power control.

23.10.4.1.6 UTMI Interface

The host controller supports three ports. Each host controller port is configured to be in UTMI or ULPI mode (see the UHH_HOSTCONFIG[21:16] Px_MODE bit field).

In UTMI mode, a port has its UTMI signal set broadcasting the outgoing packets (from the host to the peripherals) and gathering the incoming ones (from the addressed peripheral to the host). ULPI signals for that port are undefined/don't care on all ports.

The UTMI ports between the HS USB host controller and the USB TLL module are on-chip and remain invisible.

UTMI transparent mode is used to connect with the HSIC modules. (UHH_HOSTCONFIG[17:16] P1_MODE or [19:18] P2_MODE [21:20] or P3_MODE bit fields must be set to 0x3).

23.10.4.1.7 ULPI Interface

The host supports two ports. Each host controller port is configured to be either in UTMI or in ULPI mode (see the UHH_HOSTCONFIG[21:16] Px_MODE bit fields).

In ULPI mode, a port has its ULPI signal set broadcasting the outgoing packets (that is, from the host to the peripherals) and gathering the incoming packets (that is, from the addressed peripheral to the host). UTMI signal sets are undefined/don't care on all ports.

NOTE: The ULPI clock (part of the 12-wire ULPI interface) is expected to be routed by the system from the ULPI CLK input I/O pad to the clock input used by all HS modes (ULPI and UTMI) for the current port.Section 3.6.3.2.2

23.10.4.2 USB TLL Module Functionality

23.10.4.2.1 USB TLL Software Reset

Writing 0x1 to the USBTLL_SYSCONFIG[1] SOFTRESET bit resets the USB TLL module. The bit value of 0x1 remains until the reset completes. When the software reset completes, the SOFTRESET bit is automatically set to 0x0 and has the same effect as the hardware reset.

23.10.4.2.2 USB TLL Power Management

The USB protocol defines power-saving modes, where clocks can be shut down.

23.10.4.2.2.1 IDLE Handshake Protocol

The PRCM module handles an IDLE handshake protocol for the USB TLL module. The IDLE handshake protocol lets the PRCM module require the HS USB TLL module to enter idle mode.

The way in which the HS USB TLL module acknowledges the PRCM IDLE request is configurable through the USBTLL_SYSCONFIG[4:3] SIDLEMODE bit field. Table 23-841 lists related acknowledgment modes.

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Table 23-841. HS USB TLL Module SIDLEMODE Settings

SIDLEMODE Value	Selected Mode	Description
0x0	Force-idle	The HS USB host controller acknowledges unconditionally the IDLE request from the PRCM module, regardless of its internal operations.
0x1	No-idle	The HS USB host controller never acknowledges any IDLE request from the PRCM module.
0x2	Smart-idle	The HS USB host controller acknowledges the IDLE request, basing its decision on its internal activity.

23.10.4.2.3 USB TLL Channels and Ports

Following the same convention as UTMI and ULPI, the current specification is consistently PHY-centric (that is, directions are always given with respect to the transceiver emulated here by the TLL, and not with respect to the link controller): An input goes from the link controller to the TLL (transceiver emulator) (that is, it is an input for the USB TLL module). Reciprocally, an output goes from the TLL (transceiver) to the link controller (that is, it is an output for the USB TLL module).

By convention, the local link controller is the controller integrated on the same IC as the USB TLL module: This is the HS USB host controller in the device. The remote link controller is the other controller, located off-chip (that is, on another IC). One controller is always the USB host, the other is the USB peripheral, and they communicate through the USB TLL module.

A channel is defined as a independent USB path through the USB TLL module, which always converts the UTMI+ transceiver interface protocol coming from the local link controller (the HS USB host controller in the device). There are two channels of the USB TLL module in the device.

A USB port is a set of I/O signals that carry the data and control information from/to a USB line. Several port formats exist, with different capabilities. A channel has three ports. If the channel is active, two ports are active at the same time, depending on the configuration of the channel. The mode remains static throughout the USB operation.

23.10.4.2.4 USB TLL Channel Configuration

A channel configuration is a set of software settings that specifies the connection of two of the channel ports through the USB TLL module. USB data and control injected on one side (or port) comes out on the other side (or port) after a certain amount of processing, depending on the mode. Table 23-842, lists the modes.

All configurations connect the PHY UTMI port (attached to the HS USB host controller) to one of the other two ports (attached to a variety of transceivers or controllers on the pad side).

Table 23-842 describes the available modes and the software settings required for each. Channel i has the following settings:

- CHANMODE: TLL_CHANNEL_CONF_i[2:1] CHANMODE bit field
- FSLSMODE: TLL_CHANNEL_CONF_i[27:24] FSLSMODE bit field
- FSLSSERIALMODE_3PIN/6PIN: Either the ULPI PHY-side INTERFACE_CTRL_i[1] FSLSSERIALMODE_3PIN bit or the INTERFACE_CTRL_i[0] FSLSSERIALMODE_6PIN bit (only one at a time can be set to 1)

Table 23-842. USB TLL Channel Configuration

Configuration	Mode	CHANMODE	FSLSMODE	Other Settings	Ports	Speed	Remote Port Connection
1	UTMI transparent	0	N/A	–	A-B	–	UTMI transparent
2	ULPI synchronous TLL	0	N/A	FSLSSERIALMODE_3PIN/6PIN = 0	A-C	HFL	ULPI link (peripheral controller)
3	Serial UTMI to serial ULPI TLL	0	N/A	FSLSSERIALMODE_3PIN/6PIN = 1	A-C	FL	ULPI link (peripheral controller) supporting 3-/6-pin mode

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Table 23-842. USB TLL Channel Configuration (continued)

Configuration	Mode	CHANMODE	FSLSMODE	Other Settings	Ports	Speed	Remote Port Connection
4	Serial UTMI to serial TLL	1	0x4-0x7; 0xA-0xB	–	A-D	FL	Serial link (2-/3-/4-/6-pin)
4	Serial UTMI to serial PHY	1	0x0-0x3	–	A-D	FL	Serial transceiver (2-/3-/4-/6-pin)

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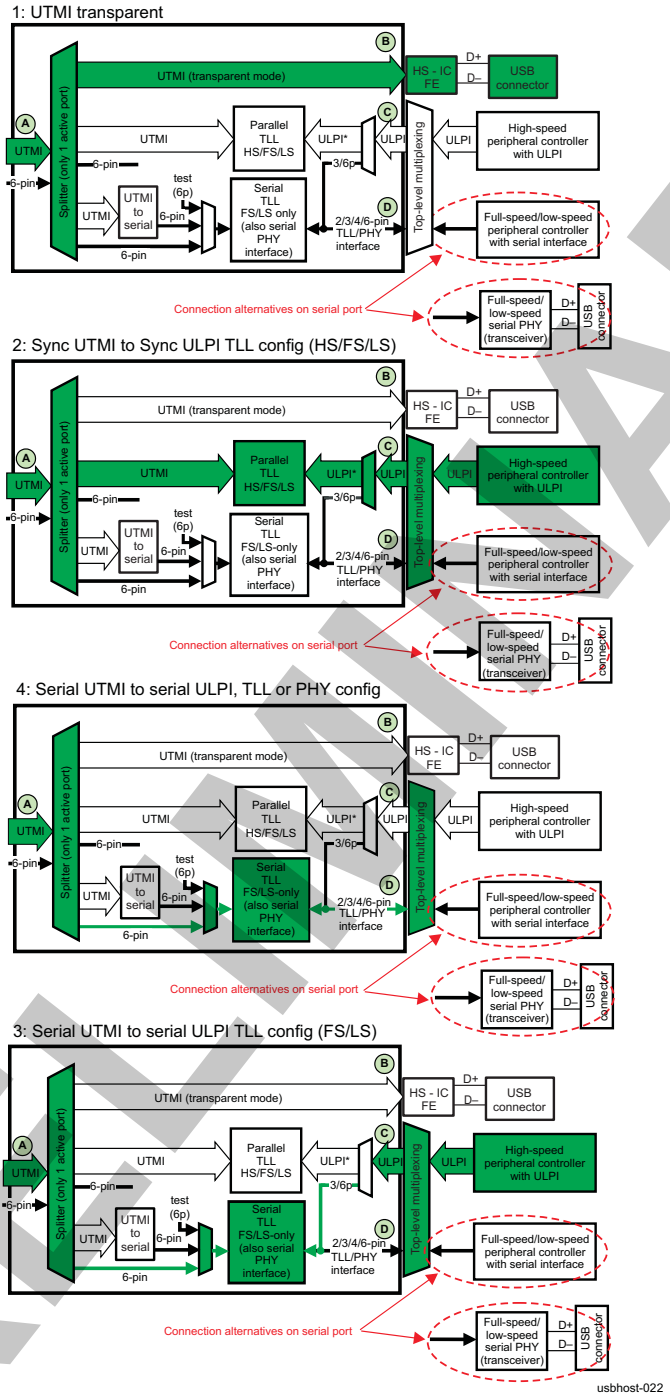
Figure 23-235. Per-Configuration Data Path Through USB TLL



23.10.4.2.5 USB TLL VBUS Management and Emulations

In transceiver configurations, a USB cable is present, including a 5-V VBUS supply line. On the other hand, in TLL configurations, the physical USB lines are emulated and have no physical existence. This is especially true for the VBUS line, which distributes the 5-V power provided by the default host (or A-device) to the entire bus. VBUS is also used for signaling purposes, and those features must be emulated:

- A peripheral detects the presence of a host by detecting the presence of VBUS.
- USB OTG defines an elaborate voltage-sensing scheme to dynamically switch on and off VBUS (start and stop sessions). In the context of TLL, this brings no power savings compared to a simple suspend.

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- In particular, USB OTG uses VBUS as a wake-up source (VBUS-pulsing SRP) for the default peripheral (or B-device).

For more information on how sideband controls are integrated, see Figure 23-220 and Figure 23-221 and the related explanations.

23.10.4.2.5.1 VBUS Control and Status for Transceiver (Non-TLL) Configurations

In non-TLL modes, VBUS exists, and the problem is to propagate control and status to and from the VBUS manager IC (typically, the transceiver).

Only serial transceiver configurations are concerned in the case of the HS USB host subsystem in the device.

23.10.4.2.5.1.1 VBUS Management in Serial Transceiver Configurations

VBUS management is not standardized in transceiver configurations. The chosen implementation is described in the following list (also see Figure 23-220).

- VBUS control required for host and OTG operation (VBUS drive, VBUS pullup "charge," VBUS pulldown "discharge") is assumed to be handled separately from the USB TLL module (that is, by software and straight to the power IC, which can be the transceiver, especially in OTG cases).
- The status of VBUS must be sampled by the appropriate hardware (again, most often the transceiver) and reported by software to the USB TLL module, using the TLL_CHANNEL_CONF_i[16] DRVVBUS and TLL_CHANNEL_CONF_i [15] CHRGVBUS bits, as indicated in Table 23-843.

Table 23-843 lists the values to write to the TLL_CHANNEL_CONF_i register depending on the status of VBUS observed by the transceiver on the VBUS line. The same register fields are also used in TLL configuration, and have been named according to that second configuration. In transceiver configurations, the signification of the fields is:

- DRVVBUS: Set to 1 to report a VBUS level greater than VBUS valid.
- CHRGVBUS: Set to 1 to report a VBUS level greater than session valid.

Table 23-843. VBUS Level Software Reporting for Serial Transceiver Configuration

VBUS Status	TLL_CHANNEL_CONF_i[16] DRVVBUS	TLL_CHANNEL_CONF_i[15] CHRGVBUS
VBUS valid	1	1
Session valid (A/B)	0	1
Session not valid	0	0
Session end	0	0

23.10.4.2.5.2 VBUS Emulation for TLL Configurations

The TLL VBUS emulation sums up all actions on the VBUS line and obtains a voltage level, which is reported in the VBUS status bits following the protocol. The level depends on the immediate VBUS actions and has no memory of previous levels, whereas an actual VBUS line behaves like an RC circuit and takes time to charge and discharge. This causes the following differences:

- The TLL level always jumps abruptly from session valid to session end (and back) with no transient time in between (where session is neither valid nor ended) as in real life.
- The charge feature is used for VBUS-pulsing SRP and is enabled long enough to go over the session valid threshold, but without reaching VBUS valid. In the TLL, the transition to session valid is immediate, and VBUS valid is never reached even if the charge is intentionally kept active.
- The discharge feature is used in real life to accelerate the voltage drop of an undriven VBUS toward the session-end level. For TLL, therefore, this is useless (although the UTMI input/ULPI register bit does exist, for compatibility), and is always don't care.

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23.10.4.2.5.2.1 VBUS Emulation in ULPI TLL Modes

Table 23-844 summarizes the VBUS emulation in ULPI TLL modes. VBUS controls are writable, static PHY-side registers on the ULPI side, and input signals on the ULPI ports (port A). VBUS status bits are read-only, volatile PHY-side registers on the ULPI, and output signals on the ULPI ports (port A).

Table 23-844. Emulation of VBUS Levels for UTMI-to-ULPI TLL Mode

VBUS Controls (Actions)			VBUS Level	VBUS Status		
OTG_CTRL_i[5] DRVVBUS	OTG_CTRL_i[4] CHRGVBUS	OTG_CTRL_i[3] DISCHRGVBUS		USB_INT_STATUS_i[1] VBUSVALID bit	USB_INT_STATUS_i[2] SESSVALID bit	USB_INT_STATUS_i[3] SESSEND bit
1	X	X	VBUS valid	1	1	0
0	1	X	VBUS valid	0	1	0
0	0	X	Session end	0	0	1

23.10.4.2.5.2.2 VBUS Emulation in Serial TLL Modes

In serial TLL modes, VBUS status and control is implemented with ad hoc sideband signals (see Figure 23-221).

VBUS control can be done in software by writing to the following fields of the TLL_CHANNEL_CONF_i register:

- DRVVBUS: Set to 1 to drive VBUS to 5 V (for A-device or host)
- CHRGVBUS: Set to 1 to pull up VBUS (for SRP)
- There is no pulldown (discharge) control, because the emulated VBUS has no latency and VBUS level goes to the session-end level as soon as it is neither driven nor pulled up.

Alternatively, VBUS drive can also be hardware-controlled through a dedicated input. (The DRVVBUS bit and input signal are OR-ed internally.)

VBUS status is available on dedicated output signals. If those outputs are not available at the top level, a software alternative is to use the voltage status reported on the interface (through the standard UTMI+ sideband signals) of the local controller (the HS USB host controller in the device) and to pass it to the remote controller (a peripheral controller) by means of an ad hoc software-controller interface other than the USB. This is based on the fact that the level of VBUS is the same on both extremities of the bus (that is, it does not matter which side does the measurement).

23.10.4.2.6 USB TLL Multimode Serial Port

The multimode serial port requires six bidirectional I/O pads to support all eight defined modes (selected in the TLL_CHANNEL_CONF_i[27:24] FSLSMODE bit field when field CHANMODE = 0x1 = UTMI-to-serial). Those modes are FS/LS only (that is, HS is not supported over a serial interface).

The pads are named TXEN, TXDAT, TXSE0, RXRCV, RXDP, and RXDM after their functionality in standard 6-pin mode (mode 0). Each pad has an input, output, and output-enable signal associated with it on the USB TLL entity.

Table 23-845 lists the function of each pad in each mode. USB TLL outputs are shown in yellow, inputs in blue, and bidirectional pads in green.

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Table 23-845. Serial Mode Description, Signal Functionality

Usual Name	6-Pin Mode	6-Pin Mode (Alt)	3-Pin Mode	4-Pin Mode	6-Pin TLL Mode	6-Pin TLL (Alt) Mode	3-Pin TLL Mode	4-Pin TLL Mode	2-Pin TLL Mode	2-Pin TLL (Alt) Mode
TLL_CHANNEL_CONF_i[27:24] FSLSMODE bit field	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0xA	0xB
TX encoding	DAT/SE0	DP/DM	DAT/SE0	DP/DM	DAT/SE0	DP/DM	DAT/SE0	DP/DM	DAT/SE0	DP/DM
RX encoding	DP/DM/RCV	DP/DM/RCV	DAT/SE0	DP/DM/RCV	DP/DM/RCV	DP/DM/RCV	DAT/SE0	DP/DM/RCV	DAT/SE0	DP/DM
Pin use	Unidirectional	Unidirectional	Bidirectional	Bidirectional	Unidirectional	Unidirectional	Bidirectional	Bidirectional	Bidirectional	Bidirectional
Pin count	6	6	3	4	6 or 5[1]	6 or 5[1]	3	4 or 3[2]	2	2
I/O Pad Function Per Mode										
TXEN	TX Enable	TX Enable	TX Enable	TX Enable	TX Enable	TX Enable	TX Enable	TX Enable	N/C	N/C
TXDAT	TX Diff Data	TX SE Plus Data	TX/RX Diff Data	TX/RX SE Plus Data	TX Diff Data	TX SE Plus Data	TX/RX Diff Data	TX/RX Diff Data	TX/RX Diff Data	TX/RX SE Plus Data
TXSE0	TX force SE0	TX SE Minus Data	TX/RX force SE0	TX/RX SE Minus Data	TX force SE0	TX SE Minus Data	TX/RX force SE0	TX/RX force SE0	TX/RX force SE0	TX/RX SE Minus Data
RXRCV	RX Diff Data	RX Diff Data	N/C	RX Diff Data	RX Diff Data	RX Diff Data	N/C	RX Diff Data	N/C	N/C
RXDP	RX SE Plus Data	RX SE Plus Data	N/C	N/C	RX SE Plus Data	RX SE Plus Data	N/C	N/C	N/C	N/C
RXDP	RX SE Minus Data	RX SE Minus Data	N/C	N/C	RX SE Minus Data	RX SE Minus Data	N/C	N/C	N/C	N/C

(1) RXRCV and RXDP carry the same information: RXDP can drive both inputs of the remote controller, and RXRCV can be kept unused.
(2) Same remark for TXDAT (for outputs) and RXRCV: TXDAT only is enough.

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23.10.4.2.7 USB TLL Attach/Connect Emulation for Serial Modes

This section applies to all serial TLL modes in the following circumstances:

- In UTMI-to-serial mode (TLL_CHANNEL_CONF_i[2:1] CHANMODE = 0x1) for all TLL values of the TLL_CHANNEL_CONF_i[27:24] FSLSMODE bit field (0x4–0x7; 0xA–0xB)
- In UTMI-to-ULPI TLL mode (TLL_CHANNEL_CONF_i[2:1] CHANMODE = 0x0) when the ULPI bus is switched to 6-pin or 3-pin serial modes

In those modes, the USB bus lines are emulated by USB TLL internal logic and are never available on the outside. The pullup/pulldown actions described in the USB specification cannot be applied directly, and the USB cable cannot be physically attached.

Because serial modes do not specify a standard format for those sideband settings, a custom software-controlled one is implemented:

- The TLL_CHANNEL_CONF_i[4] TLLATTACH bit emulates the physical attachment of the two controllers through a TLL cable:
  - When this bit is cleared, the local controller RX path shows only the local controller (the HS USB host controller) actions on the bus: TX driving, pullups, pulldowns. The same applies for the remote controller RX path (except that test override is not available).
  - When the bit is set, the actions of both sides are applied to the same bus and are resolved, similar to a real bus. The RX path for both sides shows the same bus state.
- The TLL_CHANNEL_CONF_i[5] TLLCONNECT bit emulates the USB electrical connect (that is, the pullup by the USB peripheral of one of the two USB lines [by a 1.5-kΩ resistor]), which causes the line state to transition from SE0 to J, which is detected by the USB host. The register bit is ORed with a USB TLL module input signal; the connect control can be software (L4_CFG interconnect write access) or hardware (input level). The speed of the connection is determined by the TLLFULLSPEED bit.
- The TLL_CHANNEL_CONF_i[6] TLLFULLSPEED bit determines the speed (full or low) of the USB connect to be emulated. The connect enable (controlled as previously defined) results in the pulling up of D+ (1 = full speed) or D– (0 = low speed) (see Table 23-846).
- The 15-kΩ pulldowns are implicit: Because they are supposed to be turned on at least on the host side of the bus, they do not require additional control.

NOTE: Sideband control and status actions such as pullups are included in parallel (that is, nonserial) standards (UTMI, ULPI), and do not require custom additions.

Table 23-846. Pullup Enable Emulation in Serial TLL Modes

TLL_CHANNEL_CONF_i Fields		Input Signal	Resulting TLL Pullup Emulation	
TLLFULLSPEED	TLLCONNECT	USB State	D+ Pullup	D– Pullup
1	0	Full-speed unconnected	Off	Off
1	1	Full-speed connected	On	Off
0	0	Low-speed unconnected	Off	Off
0	1	Low-speed connected	Off	On

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23.10.5 HS Multiport USB Host Subsystem Low-Level Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the HS USB host subsystem.

23.10.5.1 Global Initialization

23.10.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the HS USB host subsystem is used for the first time after a device reset. This initialization of surrounding modules is based on the integration of the HS USB host subsystem.

Table 23-847 describes the global initialization of surrounding modules.

Table 23-847. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	All required clocks must be enabled. For ULPI PHY mode, mux the UTMI_P1_GFCLK from the external pad. See Section 3.6.3.2, *CM Clock Source*, in Chapter 3, *Power, Reset, and Clock Management*.
MPU INTC or IPU INTC	The MPU or IPU INTC must be configured to enable the interrupts when interrupt requests are generated by the HS multiport USB host subsystem. See the respective functional description in Chapter 17, *Interrupt Controllers*, for the MPUs.
Interconnect (L3 and L4)	For more information, see Section 14.2, *L3 Interconnect*, and Section 14.3, *L4 Interconnect*.

23.10.5.1.2 HS Multiport USB Host Subsystem Global Initialization

This procedure in Table 23-848 initializes the HS multiport USB host subsystem after a power-on or software reset.

Table 23-848. HS Multiport USB Host Subsystem Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset on the TLL module.	USBTLL_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset is finished.	USBTLL_SYSSTATUS[0] RESETDONE	=0x1
Enable IRQ event for the TLL module.	USBTLL_IRQENABLE[1] FCLK_END_EN	0x1
Enable IRQ event for the TLL module.	USBTLL_IRQENABLE[0] FCLK_START_EN	=0x1
Perform a software reset on the HS USB controller.	UHH_SYSCONFIG[0] SOFTRESET	0x1
Wait until the EHCI HS host is out of reset.	UHH_SYSSTATUS[2] EHCI_RESETDONE	=0x0
Wait until the OHCI HS host is out of reset.	UHH_SYSSTATUS[1] OHCI_RESETDONE	=0x0
Enable IRQ event for the OHCI HS host.	HCINTERRUPTENABLE[31] MIE	0x1
Enable IRQ event for the EHCI HS host.	USBINTR[0] USBIE	0x1

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23.10.5.2 Operational Modes Configuration (Selecting and Configuring USB Connectivity)

Figure 23-236 shows how to select and configure the HS USB host subsystem connectivity.

Figure 23-236. Selecting and Configuring HS USB Host Subsystem Connectivity

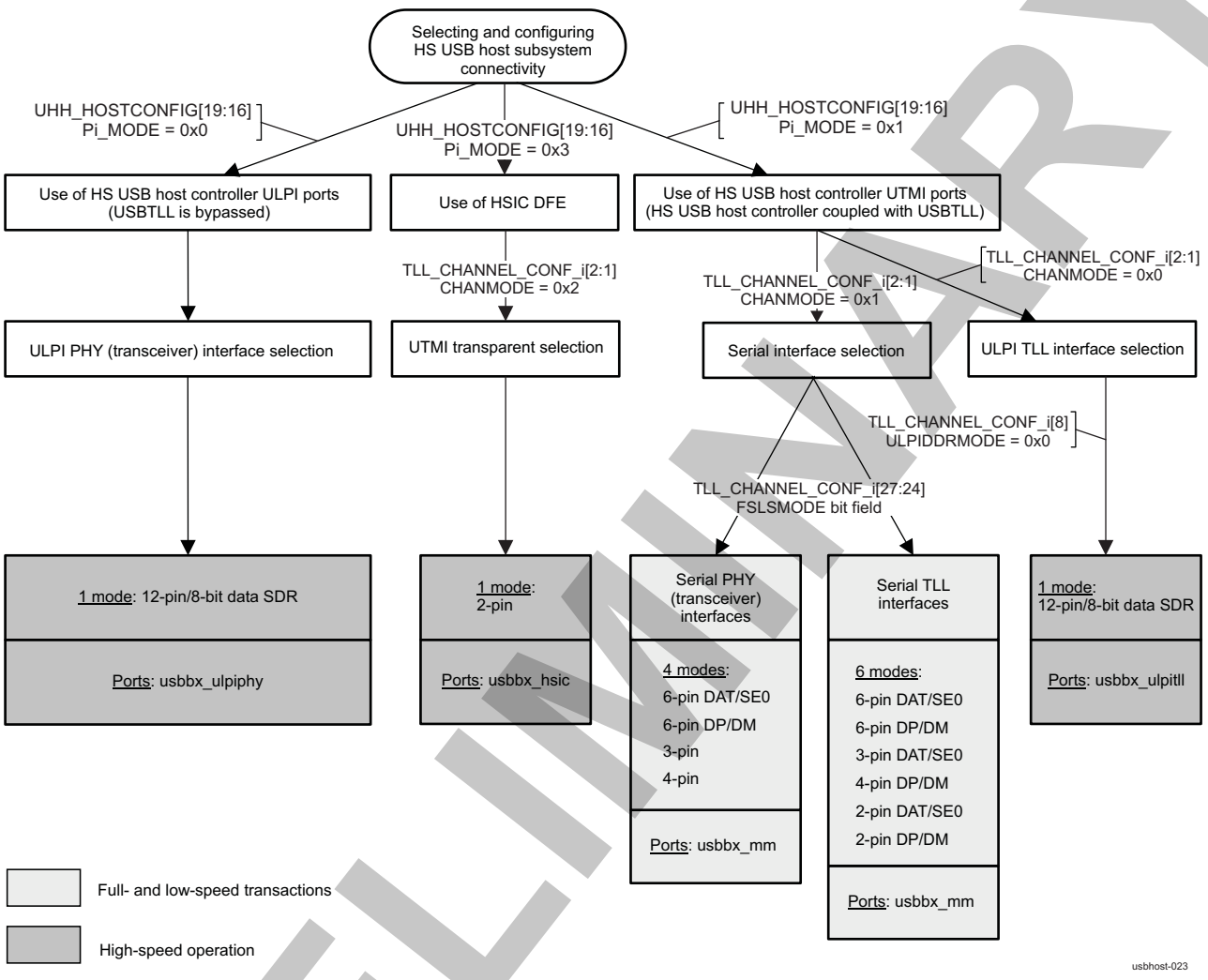

Table 23-849. Register Call Summary for Selecting and Configuring High-Speed USB Host Subsystem Connectivity

Register Name	
UHH_HOSTCONFIG	TLL_CHANNEL_CONF_i

23.10.5.3 USB TLL Registers

The USB TLL module contains two types of software-programmable registers: TLL control and status registers and ULPI PHY-side registers.

23.10.5.3.1 TLL Control and Status Registers

These 32-bit registers configure the various channels. These registers are accessed by the MPU through the L4_CFG interconnect. They are used primarily before USB activity starts. The registers are:

- OCP-standard registers for revision number, IRQ, clocking management, etc.
- TLL-specific registers

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23.10.5.3.2 ULPI PHY-Side Registers

Each TLL channel emulates a ULPI transceiver and therefore contains this set of 8-bit PHY-side registers, per ULPI specification. The registers are:

- All ULPI-mandatory standard registers and fields
- A selection of ULPI-optional standard registers and fields, when relevant to the TLL context
- Vendor-specific registers, mapped at the addresses specified for that purpose in the ULPI specification

These registers are accessed by the external (that is, off-chip) link controller over the ULPI port of each channel, in the 0x100-byte ULPI address space, using the ULPI register access protocol.

They are accessible by the L4_CFG interconnect: The ULPI register sets of all channels are mapped side by side in the upper part of the L4_CFG interconnect address space, where they can be accessed through byte accesses. If a conflict occurs between the two access modes, access over ULPI has priority, but both accesses eventually complete correctly. For normal USB activity, all register accesses are expected to go over ULPI, and register changes caused by L4_CFG interconnect accesses can compromise proper USB operation. The L4_CFG interconnect access port is intended for:

- Miscellaneous test and debug
- Nonintrusive observation of ongoing USB operations (test)
- Context restore: During USB suspend periods, the USB TLL module can be switched off to save power. When the module is switched on again, the ULPI register contents, which have been lost, can be restored over the L4_CFG interconnect before USB operations restart, provided they were saved elsewhere beforehand.

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23.10.6 HS USB Host Subsystem Register Manual

This section provides the register description of the subsystem.

23.10.6.1 HS USB Host Subsystem Instance Summary

Table 23-850 summarizes the HS USB Host Subsystem instance.

Table 23-850. HS USB Host Subsystem Instance Summary

Module Name	L4_CFG Base Address	Size
USB_TLL_HS_CONFIG	0x4A06 2000	2 KiB
USB_TLL_HS_ULPI	0x4A06 2800	2 KiB
UHH_CONFIG	0x4A06 4000	2 KiB
OHCI	0x4A06 4800	1 KiB
EHCI	0x4A06 4C00	1 KiB

23.10.6.2 USB_TLL_HS_CONFIG Registers

23.10.6.2.1 USB_TLL_HS_CONFIG Register Summary

Table 23-851 summarizes the USB_TLL_HS_CONFIG register mapping.

Table 23-851. USB_TLL_HS_CONFIG Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
USBTLL_REVISION	R	32	0x0000 0000	0x4A06 2000
USBTLL_HWINFO	R	32	0x0000 0004	0x4A06 2004
USBTLL_SYSCONFIG	RW	32	0x0000 0010	0x4A06 2010
USBTLL_SYSSTATUS	R	32	0x0000 0014	0x4A06 2014
USBTLL_IRQSTATUS	RW	32	0x0000 0018	0x4A06 2018
USBTLL_IRQENABLE	RW	32	0x0000 001C	0x4A06 201C
TLL_SHARED_CONF	RW	32	0x0000 0030	0x4A06 2030
TLL_CHANNEL_CONF_i (1)	RW	32	0x0000 0040 + (0x4 * i)	0x4A06 2040 + (0x4 * i)
USBTLL_SAR_CNTX_j (2)	RW	32	0x0000 0400 + (0x4 * j)	0x4A06 2400 + (0x4 * j)

(1) i = 0 to 2
(2) j = 0 to 6

CAUTION

The USB_TLL_HS_CONFIG registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.

23.10.6.2.2 USB_TLL_HS_CONFIG Register Description

through describe the USB_TLL_HS_CONFIG registers.

Table 23-852. USBTLL_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A06 2000	**Instance**	USB_TLL_HS_CONFIG
Description	OCP standard revision number, BCD encoded		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	Revision number	R	Ti internal data

Table 23-853. Register Call Summary for Register USBTLL_REVISION

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_CONFIG Register Summary: [0]

Table 23-854. USBTLL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A06 2004	**Instance**	USB_TLL_HS_CONFIG
Description	Information on hardware configuration of host		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SAR_CNTX_SIZE							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x000000
7:0	SAR_CNTX_SIZE	Save-and-Restore context size, in 32-bit words, i.e. number of 32-bit registers with significant context information, mapped from offset 0x400 upward.	R	0x07

Table 23-855. Register Call Summary for Register USBTLL_HWINFO

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_CONFIG Register Summary: [0]
- USB_TLL_HS_CONFIG Register Description: [1]

Table 23-856. USBTLL_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A06 2010	**Instance**	USB_TLL_HS_CONFIG
Description	OCP standard system configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							CLOCKACTIVITY	RESERVED			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	CLOCKACTIVITY	Enable autogating of OCP-derived internal clocks while module is idle. 0x0: OCP-derived internal clocks OFF during idle 0x1: OCP-derived internal clocks ON during idle	RW	0

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Bits	Field Name	Description	Type	Reset
7:5	RESERVED	Reserved	R	0x0
4:3	SIDLEMODE	Slave interface power management control. Idle Req/ack control 0x0: Force-idle mode. Sidleack[1] asserted after Sidlereq assertion 0x1: No-idle mode. Sidleack[1] never asserted. 0x2: Smart-idle mode. Sidleack[1] asserted after Sidlereq assertion when no more activity on the OCP.	RW	0x0
2	ENAWAKEUP	Asynchronous wake-up generation control (Swakeup) 0x0: Wake-up generation disabled 0x1: Wake-up generation enabled	RW	0
1	SOFTRESET	Module software reset Write 0x0: No effect Write 0x1: Starts softreset sequence.	W	0
0	AUTOIDLE	Internal autogating control 0x0: Clock always running 0x1: When no activity on OCP, clock is cut off.	RW	1

Table 23-857. Register Call Summary for Register USBTLL_SYSCONFIG

High-Speed Multiport USB Host Subsystem

- USB TLL Software Reset: [0]
- IDLE Handshake Protocol: [1]
- HS Multiport USB Host Subsystem Global Initialization: [2]
- USB_TLL_HS_CONFIG Register Summary: [3]

Table 23-858. USBTLL_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A06 2014	**Instance**	USB_TLL_HS_CONFIG
Description	OCP standard system status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	Indicates when the module has entirely come out of reset Read 0x0: Reset is ongoing Read 0x1: Reset is done	R	0

Table 23-859. Register Call Summary for Register USBTLL_SYSSTATUS

High-Speed Multiport USB Host Subsystem

- HS Multiport USB Host Subsystem Global Initialization: [0]
- USB_TLL_HS_CONFIG Register Summary: [1]

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Table 23-860. USBTLL_IRQSTATUS

Address Offset	0x0000 0018		
Physical Address	0x4A06 2018	**Instance**	USB_TLL_HS_CONFIG
Description	OCP standard IRQ status vector. Write 1 to clear a bit.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													ACCESS_ERROR	FCLK_END	FCLK_START

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	ACCESS_ERROR	Access error to ULPI register over OCP: USB clock must run for that type of access to succeed. 0x0: No event pending 0x1: Event pending	RW	0
1	FCLK_END	Functional clock is no longer requested for USB clocking 0x0: No event pending 0x1: Event pending	RW	0
0	FCLK_START	Functional clock is requested for USB clocking 0x0: No event pending 0x1: Event pending	RW	0

Table 23-861. Register Call Summary for Register USBTLL_IRQSTATUS

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_CONFIG Register Summary: [0]
- USB_TLL_HS_CONFIG Register Description: [1] [2]

Table 23-862. USBTLL_IRQENABLE

Address Offset	0x0000 001C		
Physical Address	0x4A06 201C	**Instance**	USB_TLL_HS_CONFIG
Description	OCP standard IRQ enable vector		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													ACCESS_ERROR_EN	FCLK_END_EN	FCLK_START_EN

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x00000000
2	ACCESS_ERROR_EN	Enable IRQ generation upon access error to ULPI register over L3 interconnect 0x0: IRQ event is masked 0x1: IRQ event is enabled	RW	0x0
1	FCLK_END_EN	IRQ event mask for FCLK_END interrupt (see USBTLL_IRQSTATUS[1]) 0x0: IRQ event is masked 0x1: IRQ event is enabled	RW	0x0
0	FCLK_START_EN	IRQ event mask for FCLK_START interrupt (see USBTLL_IRQSTATUS[0]) 0x0: IRQ event is masked 0x1: IRQ event is enabled	RW	0x0

Table 23-863. Register Call Summary for Register USBTLL_IRQENABLE

High-Speed Multiport USB Host Subsystem

- HS Multiport USB Host Subsystem Global Initialization: [0] [1]
- USB_TLL_HS_CONFIG Register Summary: [2]

Table 23-864. TLL_SHARED_CONF

Address Offset	0x0000 0030		
Physical Address	0x4A06 2030	**Instance**	USB_TLL_HS_CONFIG
Description	Common control register for all TLL channels		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														FCLK_REQ	FCLK_IS_ON

Bits	Field Name	Description	Type	Reset
31:2	RESERVED	Reserved	R	0x0000000
1	FCLK_REQ	Functional clock request, ORed from all channels depending on their respective USB bus state. Combined with the Fclk_is_on status to generate fclk_start/end IRQs. 0x0: Func clock input is not requested by TLL 0x1: Func clock input is requested by TLL	R	0x0
0	FCLK_IS_ON	Status of the functional clock input, provided by the system to the TLL module. The TLL module will only use that clock if the current status indicated that it is ready. Combined with the Fclk_request to generate fclk_start/end IRQs. 0x0: Functional clock input is not guaranteed ON (can actually be ON, OFF, or unstable) 0x1: Functional clock input is guaranteed ON and stable	RW	0x0

Table 23-865. Register Call Summary for Register TLL_SHARED_CONF

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_CONFIG Register Summary: [0]

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Table 23-866. TLL_CHANNEL_CONF_i

Address Offset	0x0000 0040 + (0x4 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2040 + (0x4 * i)	**Instance**	USB_TLL_HS_CONFIG
Description	Control and Status register for channel i.		
Type	RW		

31 30	29 28	27 26 25 24	23 22 21	20	19	18	17	16	15 14 13 12	11	10	9	8	7	6	5	4	3	2 1	0
RESERVED	FSLSLINESTATE	FSLSMODE	RESERVED	TESTTXSE0	TESTTXDAT	TESTTXEN	TESTEN	DRVVBUS	CHRGVBUS	RESERVED	ULPINOBITSTUFF	ULPIAUTOIDLE	UTMIAUTOIDLE	RESERVED	ULPIOUTCLKMODE	TLLFULLSPEED	TLLCONNECT	TLLATTACH	UTMISADEV	CHANMODE	CHANEN

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:28	FSLSLINESTATE	Line state for Full/low speed serial modes Bit 1 = D–/ Bit0 = D+ Read 0x0: Single-ended 0 Read 0x1: Full-Speed J = differential 1 Read 0x2: Full-Speed K = differential 0 Read 0x3: Single-ended 1 (illegal in USB)	R	0x0
27:24	FSLSMODE	Multiple-mode serial interface's mode select. Only when main channel mode is serial. No effect in other main modes. 0x0: 6-pin unidirectional PHY i/f mode. TX encoding is Dat/Se0 (default). 0x1: 6-pin unidirectional PHY i/f mode. TX encoding is Dp/Dm. 0x2: 3-pin bidirectional PHY i/f mode 0x3: 4-pin bidirectional PHY i/f mode 0x4: 6-pin unidirectional TLL mode. TX encoding is Dat/Se0. 0x5: 6-pin unidirectional TLL mode. TX encoding is Dp/Dm. 0x6: 3-pin bidirectional TLL mode 0x7: 4-pin bidirectional TLL mode 0xA: 2-pin bidirectional TLL mode. Encoding is Dat/Se0. 0xB: 2-pin bidirectional TLL mode. Encoding is Dp/Dm.	RW	0x0
23:21	RESERVED		R	0x0
20	TESTTXSE0	Force-Se0 transmit override value for serial mode test Don't care if TestEn = 0 (functional mode) or = TestTxen = 1 (TX = hiz) 0x0: drive differential value on TX according to TestTxDat 0x1: drive SE0 on TX	RW	0
19	TESTTXDAT	Differential data transmit override value for serial mode test Don't care if TestEn = 0 (functional mode) or = TestTxen = 1 (TX = hiz) or TestSe0 = 1 (TX = se0) 0x0: Drive full-speed K = differential 0 0x1: Drive full-speed J = differential 1	RW	0

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Bits	Field Name	Description	Type	Reset
18	TESTTXEN	Differential data transmit override value for serial mode test Don't care if TestEn = 0 (functional mode) 0x0: Drive Tx according to TestTxDat/Se0 0x1: Drive Tx Hiz (no drive: pullups determine line state)	RW	0
17	TESTEN	Enable manual test override for serial mode TX path (from local controller UTMI port) 0x0: No override. Tx is from local link controller 0x1: Override enabled	RW	0
16	DRVVBUS	VBUS-drive for ChanMode = serial * In TLL config, write 1 to emulate serial-side VBUS drive * In PHY config, write 1 to report "VBUS valid" status (of actual VBUS) to UTMI controller 0x0: VBUS not driven 0x1: VBUS driven to 5 V	RW	0
15	CHRGVBUS	VBUS-drive for ChanMode = serial * In TLL config, write 1 to emulate serial-side VBUS charge/pullup (OTG) * In PHY config, write 1 to reports "session valid" status (of actual VBUS) to UTMI controller 0x0: VBUS not charged, session not valid 0x1: VBUS charged, session valid	RW	0
14:12	RESERVED		R	0x0
11	ULPINOBITSTUFF	Disable bitstuff emulation in ULPI TLL for ULPI ChanMode 0x0: Bitstuff enabled, following USB standard 0x1: No bitstuff or associated delays (nonstandard)	RW	0
10	ULPIAUTOIDLE	For ChanMode = ULPI TLL only. Allow the ULPI output clock to be stopped when ULPI goes into asynchronous mode (low-power, 3-pin serial, 6-pin serial). No effect in ULPI input clock mode. 0x0: ULPI output clock always-on 0x1: ULPI output clock stops during asynchronous ULPI modes	RW	1
9	UTMIAUTOIDLE	For ChanMode = ULPI TLL only. Allow the UTMI clock (output) to be stopped when UTMII goes to suspended mode (suspendm = 0) 0x0: UTMI clock output always on 0x1: UTMI clock output gated upon suspend	RW	1
8	RESERVED		R	0
7	ULPIOUTCLKMODE	ULPI clocking mode select for ULPI TLL ChanMode. Hardcoded, for legacy only. Read 0x1: ULPI clock provided by PHY side (i.e. TLL, from functional clock). ULPI clock is output	R Rreturns 1s	1
6	TLLFULLSPEED	Sets PHY speed emulation in TLL (full/slow), which determines the line to pull up upon connect. The two connect source controls are: input m(N)_tllpuen, register field TllConnect. 0x0: Connect is Low-speed: D– pullup 0x1: Connect is Full-Speed: D+ pullup	RW	1
5	TLLCONNECT	Emulation of Full/Low-Speed connect (that is, D+ resp D– pullup) for serial TLL modes. Speed is determined by field TllSpeed. 0x0: Unconnected 0x1: Connected	RW	0

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Bits	Field Name	Description	Type	Reset
4	TLLATTACH	Emulates cable attach/detach for all serial TLL modes: * ChanMode = serial, in TLL mode (FsLsMode) * ChanMode = ULPI, in serial mode (6pin/3pin TLL) 0x0: Cable detach emulated on serial TLL 0x1: Cable attach emulated on serial TLL	RW	1
3	UTMIISADEV	Select the cable end "seen" by UTMI side of TLL, i.e. the emulated USB cable's orientation. The host must always be on A-side, peripheral on B-side. Reset value depends on generic DEFUTMIISHOST. 0x0: UTMI side is peripheral, ULPI side is host 0x1: UTMI side is host, ULPI side is peripheral	RW	1
2:1	CHANMODE	Main channel mode selection 0x0: UTMI-to-ULPI TLL mode (HS capable): to ULPI controller 0x1: UTMI-to-serial (FS/LS) mode: to serial controller (TLL) or serial PHY 0x2: Transparent UTMI mode: to UTMI PHY 0x3: No mode selected	RW	0x0
0	CHANEN	Active-high channel enable. A disabled channel is unclocked and kept under reset. 0x0: Channel i disabled 0x1: Channel i enabled	RW	0

Table 23-867. Register Call Summary for Register TLL_CHANNEL_CONF_i

High-Speed Multiport USB Host Subsystem

- USB TLL Channel Configuration: [0] [1]
- VBUS Control and Status for Transceiver (Non-TLL) Configurations: [2] [3] [4] [5] [6]
- VBUS Emulation for TLL Configurations: [7]
- USB TLL Multimode Serial Port: [8] [9]
- USB TLL Attach/Connect Emulation for Serial Modes: [10] [11] [12] [13] [14] [15] [16]
- Operational Modes Configuration (Selecting and Configuring USB Connectivity): [17]
- USB_TLL_HS_CONFIG Register Summary: [18]

Table 23-868. USBTLL_SAR_CNTX_j

Address Offset	0x0000 0400 + (0x4 * j)	**Index**	j = 0 to 6
Physical Address	0x4A06 2400 + (0x4 * j)	**Instance**	USB_TLL_HS_CONFIG
Description	Save and Restore context array. Array size is indicated in USBTLL_HWINFO. When in SAR mode, read to save and write to restore. Do not access when not in SAR mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTX																															

Bits	Field Name	Description	Type	Reset
31:0	CNTX	Context bits	RW	0x0000 0000

Table 23-869. Register Call Summary for Register USBTLL_SAR_CNTX_j

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_CONFIG Register Summary: [0]

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23.10.6.3 USB_TLL_HS_ULPI Registers

23.10.6.3.1 USB_TLL_HS_ULPI Register Summary

Table 23-870 summarizes the USB_TLL_HS_ULPI register mapping.

Table 23-870. USB_TLL_HS_ULPI Register Mapping Summary

Register Name [1]	Type	Register Width (Bits)	Address Offset	Physical Address
VENDOR_ID_LO_i	R	8	0x0000 0000 + (0x100 * i)	0x4A06 2800 + (0x100 * i)
VENDOR_ID_HI_i	R	8	0x0000 0001 + (0x100 * i)	0x4A06 2801 + (0x100 * i)
PRODUCT_ID_LO_i	R	8	0x0000 0002 + (0x100 * i)	0x4A06 2802 + (0x100 * i)
PRODUCT_ID_HI_i	R	8	0x0000 0003 + (0x100 * i)	0x4A06 2803 + (0x100 * i)
FUNCTION_CTRL_i	RW	8	0x0000 0004 + (0x100 * i)	0x4A06 2804 + (0x100 * i)
FUNCTION_CTRL_SET_i	RW	8	0x0000 0005 + (0x100 * i)	0x4A06 2805 + (0x100 * i)
FUNCTION_CTRL_CLR_i	RW	8	0x0000 0006 + (0x100 * i)	0x4A06 2806 + (0x100 * i)
INTERFACE_CTRL_i	RW	8	0x0000 0007 + (0x100 * i)	0x4A06 2807 + (0x100 * i)
INTERFACE_CTRL_SET_i	RW	8	0x0000 0008 + (0x100 * i)	0x4A06 2808 + (0x100 * i)
INTERFACE_CTRL_CLR_i	RW	8	0x0000 0009 + (0x100 * i)	0x4A06 2809 + (0x100 * i)
OTG_CTRL_i	RW	8	0x0000 000A + (0x100 * i)	0x4A06 280A + (0x100 * i)
OTG_CTRL_SET_i	RW	8	0x0000 000B + (0x100 * i)	0x4A06 280B + (0x100 * i)
OTG_CTRL_CLR_i	RW	8	0x0000 000C + (0x100 * i)	0x4A06 280C + (0x100 * i)
USB_INT_EN_RISE_i	RW	8	0x0000 000D + (0x100 * i)	0x4A06 280D + (0x100 * i)
USB_INT_EN_RISE_SET_i	RW	8	0x0000 000E + (0x100 * i)	0x4A06 280E + (0x100 * i)
USB_INT_EN_RISE_CLR_i	RW	8	0x0000 000F + (0x100 * i)	0x4A06 280F + (0x100 * i)
USB_INT_EN_FALL_i	RW	8	0x0000 0010 + (0x100 * i)	0x4A06 2810 + (0x100 * i)
USB_INT_EN_FALL_SET_i	RW	8	0x0000 0011 + (0x100 * i)	0x4A06 2811 + (0x100 * i)
USB_INT_EN_FALL_CLR_i	RW	8	0x0000 0012 + (0x100 * i)	0x4A06 2812 + (0x100 * i)
USB_INT_STATUS_i	R	8	0x0000 0013 + (0x100 * i)	0x4A06 2813 + (0x100 * i)
USB_INT_LATCH_i	R	8	0x0000 0014 + (0x100 * i)	0x4A06 2814 + (0x100 * i)
DEBUG_i	R	8	0x0000 0015 + (0x100 * i)	0x4A06 2815 + (0x100 * i)
SCRATCH_REGISTER_i	RW	8	0x0000 0016 + (0x100 * i)	0x4A06 2816 + (0x100 * i)
SCRATCH_REGISTER_SET_i	RW	8	0x0000 0017 + (0x100 * i)	0x4A06 2817 + (0x100 * i)
SCRATCH_REGISTER_CLR_i	RW	8	0x0000 0018 + (0x100 * i)	0x4A06 2818 + (0x100 * i)
EXTENDED_SET_ACCESS_i	RW	8	0x0000 002F + (0x100 * i)	0x4A06 282F + (0x100 * i)
UTMI_VCONTROL_EN_i	RW	8	0x0000 0030 + (0x100 * i)	0x4A06 2830 + (0x100 * i)
UTMI_VCONTROL_EN_SET_i	RW	8	0x0000 0031 + (0x100 * i)	0x4A06 2831 + (0x100 * i)
UTMI_VCONTROL_EN_CLR_i	RW	8	0x0000 0032 + (0x100 * i)	0x4A06 2832 + (0x100 * i)
UTMI_VCONTROL_STATUS_i	RW	8	0x0000 0033 + (0x100 * i)	0x4A06 2833 + (0x100 * i)
UTMI_VCONTROL_LATCH_i	R	8	0x0000 0034 + (0x100 * i)	0x4A06 2834 + (0x100 * i)
UTMI_VSTATUS_i	RW	8	0x0000 0035 + (0x100 * i)	0x4A06 2835 + (0x100 * i)
UTMI_VSTATUS_SET_i	RW	8	0x0000 0036 + (0x100 * i)	0x4A06 2836 + (0x100 * i)
UTMI_VSTATUS_CLR_i	RW	8	0x0000 0037 + (0x100 * i)	0x4A06 2837 + (0x100 * i)
USB_INT_LATCH_NOCLR_i	R	8	0x0000 0038 + (0x100 * i)	0x4A06 2838 + (0x100 * i)
VENDOR_INT_EN_i	RW	8	0x0000 003B + (0x100 * i)	0x4A06 283B + (0x100 * i)
VENDOR_INT_EN_SET_i	RW	8	0x0000 003C + (0x100 * i)	0x4A06 283C + (0x100 * i)
VENDOR_INT_EN_CLR_i	RW	8	0x0000 003D + (0x100 * i)	0x4A06 283D + (0x100 * i)
VENDOR_INT_STATUS_i	R	8	0x0000 003E + (0x100 * i)	0x4A06 283E + (0x100 * i)
VENDOR_INT_LATCH_i	R	8	0x0000 003F + (0x100 * i)	0x4A06 283F + (0x100 * i)

[1] i = 0 to 2

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23.10.6.3.2 USB_TLL_HS_ULPI Register Description

through describe the USB_TLL_HS_ULPI registers.

Table 23-871. VENDOR_ID_LO_i

Address Offset	0x0000 0000 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2800 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Lower byte of USB-IF-supplied 16-bit vendor ID Value is set for all channels. Default is Texas Instruments Vendor ID = 0x0451.		
Type	R		

7	6	5	4	3	2	1	0
VENDOR_ID_LO							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID_LO		R	0x51

Table 23-872. Register Call Summary for Register VENDOR_ID_LO_i

High-Speed Multiport USB Host Subsystem
- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-873. VENDOR_ID_HI_i

Address Offset	0x0000 0001 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2801 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Upper byte of USB-IF-supplied 16-bit vendor ID Value is set for all channels. Default is Texas-Instruments Vendor ID = 0x0451.		
Type	R		

7	6	5	4	3	2	1	0
VENDOR_ID_HI							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID_HI		R	0x04

Table 23-874. Register Call Summary for Register VENDOR_ID_HI_i

High-Speed Multiport USB Host Subsystem
- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-875. PRODUCT_ID_LO_i

Address Offset	0x0000 0002 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2802 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Lower byte of 16-bit product ID Value is set for all channels.		
Type	R		

7	6	5	4	3	2	1	0
PRODUCT_ID_LO							

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Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID_LO		R	0x00

Table 23-876. Register Call Summary for Register PRODUCT_ID_LO_i

High-Speed Multiport USB Host Subsystem
- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-877. PRODUCT_ID_HI_i

Address Offset	0x0000 0003 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2803 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Upper byte of 16-bit product ID Value is set for all channels.		
Type	R		

7	6	5	4	3	2	1	0
PRODUCT_ID_HI							

Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID_HI		R	0x00

Table 23-878. Register Call Summary for Register PRODUCT_ID_HI_i

High-Speed Multiport USB Host Subsystem
- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-879. FUNCTION_CTRL_i

Address Offset	0x0000 0004 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2804 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Controls UTMI function settings of the PHY. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	RESERVED		R	0
6	SUSPENDM	Active low PHY suspend: puts the ULPI bus in low-power mode. Automatically set back to 1 upon low-power mode exit. 0x0: PHY is in low-power mode. 0x1: PHY is not in low-power mode.	RW	1
5	RESET	Active high UTMI transceiver reset. Auto-cleared. Does not reset the ULPI interface or ULPI register set. 0x0: No ongoing reset/no action 0x1: Ongoing reset/apply reset	RW	0
4:3	OPMODE	Select the required bit encoding style during transmit 0x0: Normal operation 0x1: Nondriving 0x3: Reserved 0x2: Disable bit-stuff and NRZI encoding	RW	0x0

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Bits	Field Name	Description	Type	Reset
2	TERMSELECT	Controls the internal 1.5-kΩ HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. 0x0: HS termination enabled (other conditions) 0x1: FS termination enabled (other conditions)	RW	0
1:0	XCVRSELECT	Select the required transceiver speed. 0x0: Enable HS transceiver 0x1: Enable FS transceiver 0x3: Enable FS transceiver for LS packets (automatic FS preamble prepending) 0x2: Enable LS transceiver	RW	0x1

Table 23-880. Register Call Summary for Register FUNCTION_CTRL_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-881. FUNCTION_CTRL_SET_i

Address Offset	0x0000 0005 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2805 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Controls UTMI function settings of the PHY. SET register. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0x0
6	SUSPENDM	Active low PHY suspend: Puts the ULPI bus in low-power mode. Automatically set back to 1 upon low-power mode exit. Write 0: No effect on bit value Write 1: Set the bit to 1.	RW	0x1
5	RESET	Active high UTMI transceiver reset. Autocleared. Does not reset the ULPI interface or ULPI register set. Write 0: No effect on bit value Write 1: Set the bit to 1.	RW	0x0
4:3	OPMODE	Select the required bit encoding style during transmit. Write 0x0: No effect on bit value Write 01, 10, or 11: Set the bit [3], [4], or [4:3] to 1.	RW	0x0
2	TERMSELECT	Controls the internal 1.5-kΩ pullup resistor and 45-Ω HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. Write 0: No effect on bit value Write 1: Set the bit to 1.	RW	0x0
1:0	XCVRSELECT	Select the required transceiver speed. Write 0x0: No effect on bit value Write 01, 10, or 11: Set the bit [0], [1], or [1:0] to 1.	RW	0x1

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Table 23-882. Register Call Summary for Register FUNCTION_CTRL_SET_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-883. FUNCTION_CTRL_CLR_i

Address Offset	0x0000 0006 + (0x100 * i)	**Index**	i =0 to 1
Physical Address	0x4A06 2806 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Controls UTMI function settings of the PHY. CLR register Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0x0
6	SUSPENDM	Active low PHY suspend: Puts the ULPI bus in low-power mode. Automatically set back to 1 upon low-power mode exit. Write 0: No effect on bit value Write 1: Clear the bit to 0.	RW	0x1
5	RESET	Active high UTMI transceiver reset. Autocleared. Does not reset the ULPI interface or ULPI register set. Write 0: No effect on bit value Write 1: Clear the bit to 0.	RW	0x0
4:3	OPMODE	Select the required bit encoding style during transmit Write 0x0: No effect on bit value Write 01, 10, or 11: Clear the bit [3], [4], or [4:3] to 0.	RW	0x0
2	TERMSELECT	Controls the internal 1.5-kΩ pull-up resistor and 45-Ω HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. Write 0: No effect on bit value Write 1: Clear the bit to 0.	RW	0x0
1:0	XCVRSELECT	Select the required transceiver speed. Write 0x0: No effect on bit value Write 01, 10, or 11: Clear the bit [0], [1], or [1:0] to 0.	RW	0x1

Table 23-884. Register Call Summary for Register FUNCTION_CTRL_CLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-885. INTERFACE_CTRL_i

Address Offset	0x0000 0007 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2807 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Enables alternative interfaces and PHY features. Read/write address.		
Type	RW		

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7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	RESERVED		AUTORESUME	CLOCKSUSPENDM	RESERVED	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

Bits	Field Name	Description	Type	Reset
7	INTERFACE_PROTECT_DISABLE	Controls circuitry built into the PHY for protecting the ULPI interface when the link 3-states stp and data. 0x0: Enables the interface protect circuit 0x1: Disables the interface protect circuit	RW	0
6:5	RESERVED		R	0x0
4	AUTORESUME	Enables the PHY to automatically drive resume signaling. On by default. 0x0: AutoResume disabled 0x1: AutoResume enabled	RW	1
3	CLOCKSUSPENDM	Active low clock suspend for serial modes (6-pin/3-pin). 0x0: ULPI clock will stop during serial modes. 0x1: ULPI clock will run during serial modes.	RW	0
2	RESERVED		R	0
1	FSLSSERIALMODE_3PIN	Sets the ULPI interface to 3-pin (FS/LS only) serial mode. Auto-cleared when serial mode is exited. 0x0: ULPI is not in 3-pin mode. 0x1: ULPI is in 3-pin serial mode.	RW	0
0	FSLSSERIALMODE_6PIN	Sets the ULPI interface to 6-pin (FS/LS only) serial mode. Auto-cleared when serial mode is exited. 0x0: ULPI is not in 6-pin mode. 0x1: ULPI is in 6-pin serial mode.	RW	0

Table 23-886. Register Call Summary for Register INTERFACE_CTRL_i

High-Speed Multiport USB Host Subsystem

- USB TLL Channel Configuration: [0] [1]
- USB_TLL_HS_ULPI Register Summary: [2]

Table 23-887. INTERFACE_CTRL_SET_i

Address Offset	0x0000 0008 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2808 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Enables alternative interfaces and PHY features. SET register Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value).		
Type	RW		

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7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	RESERVED		AUTORESUME	CLOCKSUSPENDM	RESERVED	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

Bits	Field Name	Description	Type	Reset
7	INTERFACE_PROTECT_DISABLE	Controls circuitry built into the PHY for protecting the ULPI interface when the link 3-states stp and data. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
6:5	RESERVED	Reserved	R	0x0
4	AUTORESUME	Enables the PHY to automatically drive resume signaling. On by default. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
3	CLOCKSUSPENDM	Active low clock suspend for serial modes (6-pin/3-pin). Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	RESERVED	Reserved	R	0x0
1	FSLSSERIALMODE_3PIN	Sets the ULPI interface to 3-pin (FS/LS only) serial mode. Autocleared when serial mode is exited. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
0	FSLSSERIALMODE_6PIN	Sets the ULPI interface to 6-pin (FS/LS only) serial mode. Autocleared when serial mode is exited. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-888. Register Call Summary for Register INTERFACE_CTRL_SET_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-889. INTERFACE_CTRL_CLR_i

Address Offset	0x0000 0009 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2809 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Enables alternative interfaces and PHY features. CLR register. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value).		
Type	RW		

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7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	RESERVED		AUTORESUME	CLOCKSUSPENDM	RESERVED	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

Bits	Field Name	Description	Type	Reset
7	INTERFACE_PROTECT_DISABLE	Controls circuitry built into the PHY for protecting the ULPI interface when the link 3-states stp and data. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
6:5	RESERVED	Reserved	R	0x0
4	AUTORESUME	Enables the PHY to automatically drive resume signaling. On by default. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
3	CLOCKSUSPENDM	Active low clock suspend for serial modes (6-pin/3-pin). Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
2	RESERVED	Reserved	R	0x0
1	FSLSSERIALMODE_3PIN	Sets the ULPI interface to 3-pin (FS/LS only) serial mode. Autocleared when serial mode is exited. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
0	FSLSSERIALMODE_6PIN	Sets the ULPI interface to 6-pin (FS/LS only) serial mode. Autocleared when serial mode is exited. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

Table 23-890. Register Call Summary for Register INTERFACE_CTRL_CLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-891. OTG_CTRL_i

Address Offset	0x0000 000A + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 280A + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Controls UTMI+ OTG functions of the PHY. Read/write address.		
Type	RW		

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7	6	5	4	3	2	1	0
RESERVED		DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7:6	RESERVED		R	0x0
5	DRVVBUS	Drive 5 V on VBUS 0x0: No action 0x1: Drive VBUS.	RW	0
4	CHRGVBUS	Charge VBUS through a resistor for VBUS-pulsing SRP. 0x0: No action 0x1: Charge VBUS.	RW	0
3	DISCHRGVBUS	Discharge VBUS through a resistor, until the session-end VBUS state is reached. 0x0: No action 0x1: Discharge VBUS.	RW	0
2	DMPULLDOWN	Enables the 15-kΩ pulldown resistor on D– 0x0: Pulldown resistor not connected to D– 0x1: Pulldown resistor connected to D–	RW	1
1	DPPULLDOWN	Enables the 15-kΩ pulldown resistor on D+ 0x0: Pulldown resistor not connected to D+ 0x1: Pulldown resistor connected to D+	RW	1
0	IDPULLUP	Pullup to the (OTG) ID line to allow its sampling 0x0: Disable sampling of ID line. 0x1: Enable sampling of ID line.	RW	0

Table 23-892. Register Call Summary for Register OTG_CTRL_i

High-Speed Multiport USB Host Subsystem

- VBUS Emulation for TLL Configurations: [0] [1] [2]
- USB_TLL_HS_ULPI Register Summary: [3]

Table 23-893. OTG_CTRL_SET_i

Address Offset	0x0000 000B + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 280B + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Controls UTMI+ OTG functions of the PHY. SET register Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED		DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

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Bits	Field Name	Description	Type	Reset
7:6	RESERVED	Reserved	R	0x0
5	DRVVBUS	Drive 5 V on VBUS Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
4	CHRGVBUS	Charge VBUS through a resistor for VBUS-pulsing SRP. Write 0x0: No effect on bit value 0x1: Set the bit to 1.	RW	0x0
3	DISCHRGVBUS	Discharge VBUS through a resistor, until the session-end VBUS state is reached. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	DMPULLDOWN	Enables the 15-kΩ pulldown resistor on D– Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
1	DPPULLDOWN	Enables the 15-kΩ pulldown resistor on D+ Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
0	IDPULLUP	Pullup to the (OTG) ID line to allow its sampling Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-894. Register Call Summary for Register OTG_CTRL_SET_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-895. OTG_CTRL_CLR_i

Address Offset	0x0000 000C + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 280C + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Controls UTMI+ OTG functions of the PHY. CLR register. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED		DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7:6	RESERVED	Reserved	R	0x0
5	DRVVBUS	Drive 5 V on VBUS Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
4	CHRGVBUS	Charge VBUS through a resistor for VBUS-pulsing SRP. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

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Bits	Field Name	Description	Type	Reset
3	DISCHRGVBUS	Discharge VBUS through a resistor, until the session-end VBUS state is reached. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
2	DMPULLDOWN	Enables the 15k pulldown resistor on D– Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
1	DPPULLDOWN	Enables the 15kΩ pulldown resistor on D+ Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
0	IDPULLUP	Pullup to the (OTG) ID line to allow its sampling Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

Table 23-896. Register Call Summary for Register OTG_CTRL_CLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-897. USB_INT_EN_RISE_i

Address Offset	0x0000 000D + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 280D + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from low to high. By default, all transitions are enabled. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1

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Bits	Field Name	Description	Type	Reset
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Set the bit to 1	RW	1

Table 23-898. Register Call Summary for Register USB_INT_EN_RISE_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-899. USB_INT_EN_RISE_SET_i

Address Offset	0x0000 000E + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 280E + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from low to high. SET register. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value).		
Type	R		

7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1

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Bits	Field Name	Description	Type	Reset
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1

Table 23-900. Register Call Summary for Register USB_INT_EN_RISE_SET_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-901. USB_INT_EN_RISE_CLR_i

Address Offset	0x0000 000F + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 280F + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from low to high. CLR register. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED	Reserved	R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50 ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1

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Bits	Field Name	Description	Type	Reset
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1

Table 23-902. Register Call Summary for Register USB_INT_EN_RISE_CLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-903. USB_INT_EN_FALL_i

Address Offset	0x0000 0010 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2810 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from high to low. By default, all transitions are enabled. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_FALL	Generate an interrupt event notification when IdGnd changes from high to low. Event is automatically masked if IdPullup bit is clear to 0 and for 50 ms after IdPullup is set to 1.	RW	1
3	SESSEND_FALL	Generate an interrupt event notification when SessEnd changes from high to low.	RW	1
2	SESSVALID_FALL	Generate an interrupt event notification when SessValid changes from high to low. SessValid is the same as UTMI+ AValid.	RW	1
1	VBUSVALID_FALL	Generate an interrupt event notification when VbusValid changes from high to low.	RW	1

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Bits	Field Name	Description	Type	Reset
0	HOSTDISCONNECT_FALL	Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).	RW	1

Table 23-904. Register Call Summary for Register USB_INT_EN_FALL_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-905. USB_INT_EN_FALL_SET_i

Address Offset	0x0000 0011 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2811 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from high to low. SET register. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value).		
Type	R		

7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50 ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1

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Bits	Field Name	Description	Type	Reset
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x1

Table 23-906. Register Call Summary for Register USB_INT_EN_FALL_SET_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-907. USB_INT_EN_FALL_CLR_i

Address Offset	0x0000 0012 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2812 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Enables an interrupt event notification when the corresponding status bit changes from high to low. CLR register. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value).		
Type	R		

7	6	5	4	3	2	1	0
RESERVED			IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50 ms after IdPullup is set to 1. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1

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Bits	Field Name	Description	Type	Reset
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x1

Table 23-908. Register Call Summary for Register USB_INT_EN_FALL_CLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-909. USB_INT_STATUS_i

Address Offset	0x0000 0013 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2813 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Indicates the current value of the interrupt source signal.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED			IDGND	SESSEND	SESSVALID	VBUSVALID	HOSTDISCONNECT

Bits	Field Name	Description	Type	Reset
7:5	RESERVED	Reserved	R	0x0
4	IDGND	Value of UTMI+ IdDig output. Undefined unless IdPullup = 1 Read 0x1: ID pin is floating = OTG B = default peripheral Read 0x0: ID pin is grounded = OTG A = default host	R	0
3	SESSEND	Current value of UTMI+ SessEnd output. Read 0x1: VBUS is below Session-End threshold. Read 0x0: VBUS is above Session-End threshold.	R	0
2	SESSVALID	Current value of UTMI+ SessValid output. SessValid is the same as UTMI+ AValid. Read 0x1: VBUS is above Session-Valid threshold. Read 0x0: VBUS is below Session-Valid threshold.	R	0
1	VBUSVALID	Current value of UTMI+ VbusValid output. Read 0x1: VBUS is above Vbus-Valid threshold. Read 0x0: VBUS is below Vbus-Valid threshold.	R	0
0	HOSTDISCONNECT	Current value of UTMI+ Hostdisconnect output. Applicable only in host mode. Automatically reset to 0 when low-power mode is entered. Read 0x1: Peripheral disconnected Read 0x0: Peripheral not disconnected or nonhost mode	R	0

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Table 23-910. Register Call Summary for Register USB_INT_STATUS_i

High-Speed Multiport USB Host Subsystem

- VBUS Emulation for TLL Configurations: [0] [1] [2]
- USB_TLL_HS_ULPI Register Summary: [3]

Table 23-911. USB_INT_LATCH_i

Address Offset	0x0000 0014 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2814 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Set by unmasked changes on the corresponding status bits to generate the ULPI interrupt. Cleared upon read, and when low-power mode, serial mode, or carkit mode are entered.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED			IDGND_LATCH	SESSEND_LATCH	SESSVALID_LATCH	VBUSVALID_LATCH	HOSTDISCONNECT_LATCH

Bits	Field Name	Description	Type	Reset
7:5	RESERVED	Reserved	R	0x0
4	IDGND_LATCH	Set to 1 by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.	R	0
3	SESSEND_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.	R	0
2	SESSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid.	R	0
1	VBUSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.	R	0
0	HOSTDISCONNECT_LATCH	Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode.	R	0

Table 23-912. Register Call Summary for Register USB_INT_LATCH_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-913. DEBUG_i

Address Offset	0x0000 0015 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2815 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Indicates the current value of various signals useful for debugging.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED						LINE STATE	

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Bits	Field Name	Description	Type	Reset
7:2	RESERVED		R	0x00
1:0	LINE STATE	Current state of the USB line: D+ (bit 0) and D– (bit 1). Read 0x3: SE1 (LS/FS), Invalid (HS/Chirp) Read 0x2: LS: J state, FS: K state, HS: Invalid, Chirp: !Squelch AND !HS_Differential_Receiver_Output Read 0x1: LS: K state, FS: J state, HS: !Squelch, Chirp: !Squelch AND HS_Differential_Receiver_Output Read 0x0: SE0 (LS/FS), Squelch (HS/Chirp)	R	0x0

Table 23-914. Register Call Summary for Register DEBUG_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-915. SCRATCH_REGISTER_i

Address Offset	0x0000 0016 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2816 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Register byte for register access testing purposes. Value has no functional effect on PHY. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH	Scratch data	RW	0x00

Table 23-916. Register Call Summary for Register SCRATCH_REGISTER_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-917. SCRATCH_REGISTER_SET_i

Address Offset	0x0000 0017 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2817 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Register byte for register access testing purposes. Value has no functional effect on PHY. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value).		
Type	R		

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH	Scratch data Write 1 to a bit to set it to 1. Writing 0 has no effect on bit value.	RW	0x00

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Table 23-918. Register Call Summary for Register SCRATCH_REGISTER_SET_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-919. SCRATCH_REGISTER_CLR_i

Address Offset	0x0000 0018 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2818 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Register byte for register access testing purposes. Value has no functional effect on PHY. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value).		
Type	R		

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH	Scratch data Write 1 to a bit to clear it to 0. Writing 0 has no effect on bit value.	RW	0x00

Table 23-920. Register Call Summary for Register SCRATCH_REGISTER_CLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-921. EXTENDED_SET_ACCESS_i

Address Offset	0x0000 002F + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 282F + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	This address is used to access the extended register set; that is, addresses above 0x40.		
Type	RW		

7	6	5	4	3	2	1	0
SET_ACCESS							

Bits	Field Name	Description	Type	Reset
7:0	SET_ACCESS	This bit field is used to access the extended register set; that is, addresses above 0x40.	RW	0x00

Table 23-922. Register Call Summary for Register EXTENDED_SET_ACCESS_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-923. UTMI_VCONTROL_EN_i

Address Offset	0x0000 0030 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2830 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system. Enables an interrupt notification when the corresponding vcontrol_status bit changes. Read/write address. Lowest 4 bits are implemented, others are always-0, read-only.		
Type	RW		

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7	6	5	4	3	2	1	0
VC7_EN	VC6_EN	VC5_EN	VC4_EN	VC3_EN	VC2_EN	VC1_EN	VC0_EN

Bits	Field Name	Description	Type	Reset
7	VC7_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
6	VC6_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
5	VC5_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
4	VC4_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
3	VC3_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	VC2_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
1	VC1_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
0	VC0_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-924. Register Call Summary for Register UTMI_VCONTROL_EN_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-925. UTMI_VCONTROL_EN_SET_i

Address Offset	0x0000 0031 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2831 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system. Enables an interrupt notification when the corresponding vcontrol_status bit changes. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value).		
Type	RW		

7	6	5	4	3	2	1	0
VC7_EN	VC6_EN	VC5_EN	VC4_EN	VC3_EN	VC2_EN	VC1_EN	VC0_EN

Bits	Field Name	Description	Type	Reset
7	VC7_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
6	VC6_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
5	VC5_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
4	VC4_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

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Bits	Field Name	Description	Type	Reset
3	VC3_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
2	VC2_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
1	VC1_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0
0	VC0_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-926. Register Call Summary for Register UTMI_VCONTROL_EN_SET_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-927. UTMI_VCONTROL_EN_CLR_i

Address Offset	0x0000 0032 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2832 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system. Enables an interrupt notification when the corresponding vcontrol_status bit changes. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value).		
Type	RW		

7	6	5	4	3	2	1	0
VC7_EN	VC6_EN	VC5_EN	VC4_EN	VC3_EN	VC2_EN	VC1_EN	VC0_EN

Bits	Field Name	Description	Type	Reset
7	VC7_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
6	VC6_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
5	VC5_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
4	VC4_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
3	VC3_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
2	VC2_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
1	VC1_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0
0	VC0_EN	Enable alt_int assertion upon vcontrol_status bit change: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

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Table 23-928. Register Call Summary for Register UTMI_VCONTROL_EN_CLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-929. UTMI_VCONTROL_STATUS_i

Address Offset	0x0000 0033 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2833 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system. UTMI-standard Vcontrol vector byte is sent by the UTMI controller (other side of TLL) to its PHY (emulated here by the TLL). Alternatively, data can be also written directly into the register. Can contain any user-defined data. Vcontrol bit changes can be used to assert the ULPI ALT interrupt. Lowest 4 bits are implemented, others are always-0, read-only. (UTMI standard is 4-bit).		
Type	RW		

7	6	5	4	3	2	1	0
VC							

Bits	Field Name	Description	Type	Reset
7:0	VC	User-defined UTMI Control data byte	RW	0x00

Table 23-930. Register Call Summary for Register UTMI_VCONTROL_STATUS_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-931. UTMI_VCONTROL_LATCH_i

Address Offset	0x0000 0034 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2834 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system. Set by unmasked changes on the corresponding vcontrol_status bits to generate the ULPI ALT interrupt. Cleared upon read, and when low-power mode, serial mode or carkit mode are entered. Lowest 4 bits are implemented, others are always-0, read-only.		
Type	R		

7	6	5	4	3	2	1	0
VC7_CHANGE	VC6_CHANGE	VC5_CHANGE	VC4_CHANGE	VC3_CHANGE	VC2_CHANGE	VC1_CHANGE	VC0_CHANGE

Bits	Field Name	Description	Type	Reset
7	VC7_CHANGE	Unmasked change on vcontrol_status bit	R	0
6	VC6_CHANGE	Unmasked change on vcontrol_status bit	R	0
5	VC5_CHANGE	Unmasked change on vcontrol_status bit	R	0
4	VC4_CHANGE	Unmasked change on vcontrol_status bit	R	0
3	VC3_CHANGE	Unmasked change on vcontrol_status bit	R	0
2	VC2_CHANGE	Unmasked change on vcontrol_status bit	R	0
1	VC1_CHANGE	Unmasked change on vcontrol_status bit	R	0
0	VC0_CHANGE	Unmasked change on vcontrol_status bit	R	0

Table 23-932. Register Call Summary for Register UTMI_VCONTROL_LATCH_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

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Table 23-933. UTMI_VSTATUS_i

Address Offset	0x0000 0035 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2835 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system. UTMI-standard Vstatus vector byte is sent by the PHY (emulated here by the TLL) to the UTMI controller (other side of TLL): information written into this register goes directly to the UTMI controller, and can contain any user-defined data. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
VS							

Bits	Field Name	Description	Type	Reset
7:0	VS	User-defined UTMI status data byte	RW	0x00

Table 23-934. Register Call Summary for Register UTMI_VSTATUS_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-935. UTMI_VSTATUS_SET_i

Address Offset	0x0000 0036 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2836 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system. UTMI-standard Vstatus vector byte is sent by the PHY (emulated here by the TLL) to the UTMI controller (other side of TLL): information written into this register goes directly to the UTMI controller, and can contain any user-defined data. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value).		
Type	RW		

7	6	5	4	3	2	1	0
VS							

Bits	Field Name	Description	Type	Reset
7:0	VS	User-defined UTMI status data byte Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x00

Table 23-936. Register Call Summary for Register UTMI_VSTATUS_SET_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-937. UTMI_VSTATUS_CLR_i

Address Offset	0x0000 0037 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2837 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Part of nonstandard UTMI-to-ULPI mailbox system. UTMI-standard Vstatus vector byte is sent by the PHY (emulated here by the TLL) to the UTMI controller (other side of TLL): information written into this register goes directly to the UTMI controller, and can contain any user-defined data. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value).		
Type	RW		

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7	6	5	4	3	2	1	0
VS							

Bits	Field Name	Description	Type	Reset
7:0	VS	User-defined UTMI status data byte: Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x00

Table 23-938. Register Call Summary for Register UTMI_VSTATUS_CLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-939. USB_INT_LATCH_NOCLR_i

Address Offset	0x0000 0038 + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 2838 + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Set by unmasked changes on the corresponding status bits to generate the ULPI interrupt. Debug, nonstandard address to the standard register: Register is not cleared on read.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED			IDGND_LATCH	SESSEND_LATCH	SESSVALID_LATCH	VBUSVALID_LATCH	HOSTDISCONNECT_LATCH

Bits	Field Name	Description	Type	Reset
7:5	RESERVED	Reserved	R	0x0
4	IDGND_LATCH	Set to 1 by the PHY when an unmasked event occurs on IdGnd.	R	0x0
3	SESSEND_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessEnd.	R	0x0
2	SESSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessValid. SessValid is the same as UTMI+ AValid.	R	0x0
1	VBUSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on VbusValid.	R	0x0
0	HOSTDISCONNECT_LATCH	Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Applicable only in host mode.	R	0x0

Table 23-940. Register Call Summary for Register USB_INT_LATCH_NOCLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

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Table 23-941. VENDOR_INT_EN_i

Address Offset	0x0000 003B + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 283B + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Vendor-specific interrupt enables (mask) for miscellaneous ULPI alt_int events. Read/write address.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED							P2P_EN

Bits	Field Name	Description	Type	Reset
7:1	RESERVED		R	0x00
0	P2P_EN	Enable PHY-to-PHY ULPI wakeup upon inactive UTMI suspendm. 0x0: PHY-to-PHY wakeup enabled 0x1: PHY-to-PHY wakeup enabled	RW	0

Table 23-942. Register Call Summary for Register VENDOR_INT_EN_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-943. VENDOR_INT_EN_SET_i

Address Offset	0x0000 003C + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 283C + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Vendor-specific interrupt enable bit (mask) for miscellaneous ULPI alt_int events. Read/set address (write 1 to a bit to set it to 1, writing 0 has no effect on bit value).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED							P2P_EN

Bits	Field Name	Description	Type	Reset
7:1	RESERVED	Reserved	R	0x00
0	P2P_EN	Enable PHY-to-PHY ULPI wakeup upon inactive UTMI suspendm. Write 0x0: No effect on bit value Write 0x1: Set the bit to 1.	RW	0x0

Table 23-944. Register Call Summary for Register VENDOR_INT_EN_SET_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-945. VENDOR_INT_EN_CLR_i

Address Offset	0x0000 003D + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 283D + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Vendor-specific interrupt enables (mask) for miscellaneous ULPI alt_int events. Read/clear address (write 1 to a bit to clear it to 0, writing 0 has no effect on bit value).		
Type	R		

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7	6	5	4	3	2	1	0
RESERVED							P2P_EN

Bits	Field Name	Description	Type	Reset
7:1	RESERVED	Reserved	R	0x00
0	P2P_EN	Enable PHY-to-PHY ULPI wakeup upon inactive UTMI suspendm. Write 0x0: No effect on bit value Write 0x1: Clear the bit to 0.	RW	0x0

Table 23-946. Register Call Summary for Register VENDOR_INT_EN_CLR_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-947. VENDOR_INT_STATUS_i

Address Offset	0x0000 003E + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 283E + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Vendor-specific interrupt sources for miscellaneous ULPI alt_int events		
Type	R		

7	6	5	4	3	2	1	0
RESERVED							UTMI_SUSPENDM

Bits	Field Name	Description	Type	Reset
7:1	RESERVED		R	0x00
0	UTMI_SUSPENDM	UTMI suspendm status (active-low), source of TLL PHY-to-PHY wake-up interrupt. Read 0x1: UTMI interface is active (not suspended). Read 0x0: UTMI interface is suspended.	R	1

Table 23-948. Register Call Summary for Register VENDOR_INT_STATUS_i

High-Speed Multiport USB Host Subsystem

- USB_TLL_HS_ULPI Register Summary: [0]

Table 23-949. VENDOR_INT_LATCH_i

Address Offset	0x0000 003F + (0x100 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 283F + (0x100 * i)	**Instance**	USB_TLL_HS_ULPI
Description	Vendor-specific interrupt latches for miscellaneous ULPI alt_int events. Cleared upon read, and when low-power mode, serial mode or carkit mode are entered.		
Type	R		

7	6	5	4	3	2	1	0
RESERVED							P2P_LATCH

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Bits	Field Name	Description	Type	Reset
7:1	RESERVED		R	0x00
0	P2P_LATCH	PHY-to-PHY ULPI wake-up event latch. Set when ULPI is in low-power mode (suspendm = 0) and UTMI is active (suspendm = 1). Read 0x1: PHY-to-PHY wake-up event was latched, ALT interrupt active. Read 0x0: No PHY-to-PHY wake-up event was latched.	R	0

Table 23-950. Register Call Summary for Register VENDOR_INT_LATCH_i

High-Speed Multiport USB Host Subsystem
- USB_TLL_HS_ULPI Register Summary: [0]

23.10.6.4 UHH_CONFIG Registers

23.10.6.4.1 UHH_CONFIG Register Summary

Table 23-951 summarizes the UHH_CONFIG register mapping.

Table 23-951. UHH_CONFIG Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
UHH_REVISION	R	32	0x0000 0000	0x4A06 4000
UHH_HWINFO	R	32	0x0000 0004	0x4A06 4004
UHH_SYSCONFIG	RW	32	0x0000 0010	0x4A06 4010
UHH_SYSSTATUS	R	32	0x0000 0014	0x4A06 4014
UHH_HOSTCONFIG	RW	32	0x0000 0040	0x4A06 4040
UHH_DEBUG_CSR	RW	32	0x0000 0044	0x4A06 4044
UHH_SAR_CNTX_i (1)	RW	32	0x0000 0100 + (0x4 * i)	0x4A06 4100 + (0x4 * i)

(1) i = 0 to 383

CAUTION

The UHH_CONFIG registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.

23.10.6.4.2 UHH_CONFIG Register Description

through describe the UHH_CONFIG registers.

Table 23-952. UHH_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A06 4000	**Instance**	UHH_CONFIG
Description	USB high-speed host (UHH) revision identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

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Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	TI Internal data

Table 23-953. Register Call Summary for Register UHH_REVISION

High-Speed Multiport USB Host Subsystem
- UHH_CONFIG Register Summary: [0]

Table 23-954. UHH_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x4A06 4004	**Instance**	UHH_CONFIG
Description	Information on host hardware configuration		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SAR_CNTX_SIZE							

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x000000
9:0	SAR_CNTX_SIZE	Save-and-restore context size, in 32-bit words; that is, number of 32-bit registers with significant context information, mapped from offset 0x100 upward.	R	0x180

Table 23-955. Register Call Summary for Register UHH_HWINFO

High-Speed Multiport USB Host Subsystem
- UHH_CONFIG Register Summary: [0]
- UHH_CONFIG Register Description: [1]

Table 23-956. UHH_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A06 4010	**Instance**	UHH_CONFIG
Description	OCP standard system configuration register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		IDLEMODE		RESERVED	SOFTRESET

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Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x0000000
5:4	STANDBYMODE	Mstandby/Mwait/[Mwakeup] initiator power-management interface configuration 0x0: Force-standby mode. Mstandby asserted unconditionally. Asynchronous (master) wake-up disabled. 0x1: No-standby mode. Mstandby never asserted. Asynchronous (master) wakeup disabled. 0x2: Smart-standby mode. Mstandby asserted when initiator activity stops. Asynchronous (master) wake-up disabled. 0x3: USBHOST doesn't support Smart standby + wakeup feature. Hence this is always disabled and software programming to this mode would result in undesired behaviour.	RW	0x0
3:2	IDLEMODE	Sidlereq/Sidleack(1:0)/[Swakeup] target power management interface configuration. 0x0: Force-Idle mode. Sidleack asserted after Idlereq assertion. Asynchronous (slave) wake-up disabled. 0x1: No-idle mode. Sidleack never asserted. Asynchronous (slave) wakeup disabled. 0x2: Smart-idle mode. Sidleack asserted upon Idlereq assertion, after target activity is over. Asynchronous (slave) wake-up disabled. 0x3: Smart-idle wake-up mode. Like smart mode with asynchronous (slave) wakeup enabled.	RW	0x2
1	RESERVED		R	0
0	SOFTRESET	Module software reset Read 0x0: No reset pending Write 0x0: No effect Write 0x1: Starts softreset sequence. Read 0x1: Reset (soft or other) is pending.	RW	0

Table 23-957. Register Call Summary for Register UHH_SYSCONFIG

High-Speed Multiport USB Host Subsystem

- HS USB Host Controller Software Reset: [0]
- Standby Handshake Protocol: [1]
- IDLE Handshake Protocol: [2]
- HS Multiport USB Host Subsystem Global Initialization: [3]
- UHH_CONFIG Register Summary: [4]

Table 23-958. UHH_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A06 4014	**Instance**	UHH_CONFIG
Description	Module-specific system status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													EHCI_RESETDONE	OHCI_RESETDONE	RESERVED

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	EHCI_RESETDONE	Indicates when the EHCI HS host is out of reset Read 0x0: Out of reset Read 0x1: Under reset	R	1
1	OHCI_RESETDONE	Indicates when the OHCI FS/LS host is out of reset Read 0x0: Out of reset Read 0x1: Under reset	R	1
0	RESERVED		R	0

Table 23-959. Register Call Summary for Register UHH_SYSSTATUS

High-Speed Multiport USB Host Subsystem

- HS Multiport USB Host Subsystem Global Initialization: [0] [1]
- UHH_CONFIG Register Summary: [2]

Table 23-960. UHH_HOSTCONFIG

Address Offset	0x0000 0040		
Physical Address	0x4A06 4040	**Instance**	UHH_CONFIG
Description	Static configuration of the USB HS host		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
APP_START_CLK	RESERVED									P3_MODE		P2_MODE		P1_MODE		RESERVED					P3_CONNECT_STATUS	P2_CONNECT_STATUS	P1_CONNECT_STATUS	RESERVED		ENA_INCR_ALIGN	ENA_INCR16	ENA_INCR8	ENA_INCR4	AUTOPPD_ON_OVERCUR_EN	RESERVED

Bits	Field Name	Description	Type	Reset
31	APP_START_CLK	When the OHCI clocks are suspended, the system has to assert this signal to start the clocks (12 and 48 MHz). This should be de-asserted after the clocks are started and before the host is suspended again. (Host is suspended means HCFS = SUSPEND or all the OHCI ports are suspended).	RW	0
30:22	RESERVED		R	0x000
21:20	P3_MODE	Port 3 interface configuration. Each bit corresponds to an internal "strap" signal, and output: Bit 0 = ulpi_bypass Bit 1 = hsic_en 0x0: To external ULPI PHY, HS only 0x1: To UTMI PHY (or ULPI TLL), FS/LS capable 0x3: To HSIC digital front-end (DFE), HS only 0x2: Forbidden	RW	0x0

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Bits	Field Name	Description	Type	Reset
19:18	P2_MODE	Port 2 interface configuration. Each bit corresponds to an internal "strap" signal, and output: Bit 0 = ulpi_bypass Bit 1 = hsic_en 0x0: To external ULPI PHY, HS only 0x1: To UTMI PHY (or ULPI TLL), FS/LS capable 0x3: To HSIC digital front-end (DFE), HS only 0x2: Forbidden	RW	0x0
17:16	P1_MODE	Port 1 interface configuration. Each bit corresponds to an internal "strap" signal, and output: Bit 0 = ulpi_bypass Bit 1 = hsic_en 0x0: To external ULPI PHY, HS only 0x1: To UTMI PHY (or ULPI TLL), FS/LS capable 0x3: To HSIC digital front-end (DFE), HS only 0x2: Forbidden	RW	0x0
15:11	RESERVED		R	0x00
10	P3_CONNECT_STATUS	Connection status for port 3 Read 0x1: Peripheral connected and active on port Read 0x0: Disconnected	R	0
9	P2_CONNECT_STATUS	Connection status for port 2 Read 0x1: Peripheral connected and active on port Read 0x0: Disconnected	R	0
8	P1_CONNECT_STATUS	Connection status for port 1 Read 0x1: Peripheral connected and active on port Read 0x0: Disconnected	R	0
7:6	RESERVED		R	0x0
5	ENA_INCR_ALIGN	Force alignment of bursts to the respective burst-size boundaries. This bit must be set to 1 to avoid buffer underflow. 0x0: disable burst type 0x1: enable burst type	RW	0
4	ENA_INCR16	Control the use of INCR16-type bursts (in AHB sense) 0x0: disable burst type 0x1: enable burst type	RW	1
3	ENA_INCR8	Control the use of INCR8-type bursts (in AHB sense) 0x0: disable burst type 0x1: enable burst type	RW	1
2	ENA_INCR4	Control the use of INCR4-type bursts (in AHB sense) 0x0: disable burst type 0x1: enable burst type	RW	1
1	AUTOPPD_ON_OVERCUR_EN	Configure reaction upon port overcurrent condition 0x0: Port remains on upon overcurrent 0x1: Port is powered down automatically upon overcurrent	RW	0
0	RESERVED		R	0

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Table 23-961. Register Call Summary for Register UHH_HOSTCONFIG

High-Speed Multiport USB Host Subsystem

- HS USB Host Controller Port Status: [0]
- HS USB Host Controller Burst Control: [1] [2]
- UTMI Interface: [3] [4]
- ULPI Interface: [5]
- Operational Modes Configuration (Selecting and Configuring USB Connectivity): [6]
- UHH_CONFIG Register Summary: [7]

Table 23-962. UHH_DEBUG_CSR

Address Offset	0x0000 0044		
Physical Address	0x4A06 4044	**Instance**	UHH_CONFIG
Description	Debug control and status for the EHCI, OHCI hosts		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												OHCI_CCS_3	OHCI_CCS_2	OHCI_CCS_1	OHCI_GLOBALSUSPEND	RESERVED								OCHI_CNTSEL	EHCI_SIMULATION_MODE	EHCI_FLADJ					

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	OHCI_CCS_3	Current Connect Status of port 3 Read 0x1: periph connected Read 0x0: no periph connected	R	0
18	OHCI_CCS_2	Current Connect Status of port 2 Read 0x1: periph connected Read 0x0: no periph connected	R	0
17	OHCI_CCS_1	Current Connect Status of port 1 Read 0x1: periph connected Read 0x0: no periph connected	R	0
16	OHCI_GLOBALSUSPEND	OHCI global suspend status, asserted 5ms after the suspend order. Read 0x1: host is suspended Read 0x0: host is not suspended	R	0
15:8	RESERVED		R	0x00
7	OCHI_CNTSEL	Selection of a shorter "1 ms" counter in OHCI host, to speed up long USB phases like reset, resume, etc... (Used only for simulation.) 0x0: functional mode, 1ms = 12,000 x 12 MHz cycles 0x1: simulation mode, 1ms = 7 x 12 MHz cycles = 583 ns	RW	0
6	EHCI_SIMULATION_MODE	Sets the PHY to non-driving mode. (Used only for simulation.) 0x0: functional mode 0x1: PHY set to non-driving	RW	0

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Bits	Field Name	Description	Type	Reset
5:0	EHCI_FLADJ	EHCI host frame length adjust. Modify only when EHCI bitfield USBSTS.HCHalted = 1 Field value + 59,488 = 60,000 by default = number of 60 MHz UTMI/ULPI clock cycles per 1 ms USB frame = number of 480 MHz HS bits per 125 us HS USB microframe	RW	0x20

Table 23-963. Register Call Summary for Register UHH_DEBUG_CSR

High-Speed Multiport USB Host Subsystem

- UHH_CONFIG Register Summary: [0]

Table 23-964. UHH_SAR_CNTX_i

Address Offset	0x0000 0100 + (0x4 * i)	**Index**	i = 0 to 383
Physical Address	0x4A06 4100 + (0x4 * i)	**Instance**	UHH_CONFIG
Description	Save and restore context array. Array size is indicated in UHH_HWINFO. When in SAR mode, read out to save and write to restore. Do not access when not in SAR mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTX																															

Bits	Field Name	Description	Type	Reset
31:0	CNTX	Context bits	RW	0x0000 0000

Table 23-965. Register Call Summary for Register UHH_SAR_CNTX_i

High-Speed Multiport USB Host Subsystem

- UHH_CONFIG Register Summary: [0]

23.10.6.5 OHCI Registers

23.10.6.5.1 OHCI Register Summary

Table 23-966 summarizes the OHCI register mapping.

Table 23-966. OHCI Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
HCREVISION	R	32	0x0000 0000	0x4A06 4800
HCCONTROL	RW	32	0x0000 0004	0x4A06 4804
HCCOMMANDSTATUS	RW	32	0x0000 0008	0x4A06 4808
HCINTERRUPTSTATUS	RW	32	0x0000 000C	0x4A06 480C
HCINTERRUPTENABLE	RW	32	0x0000 0010	0x4A06 4810
HCINTERRUPTDISABLE	RW	32	0x0000 0014	0x4A06 4814
HCHCCA	RW	32	0x0000 0018	0x4A06 4818
HCPERIODCURRENTED	R	32	0x0000 001C	0x4A06 481C
HCCONTROLHEADED	RW	32	0x0000 0020	0x4A06 4820
HCCONTROLCURRENTED	RW	32	0x0000 0024	0x4A06 4824
HCBULKHEADED	RW	32	0x0000 0028	0x4A06 4828
HCBULKCURRENTED	RW	32	0x0000 002C	0x4A06 482C
HCDONEHEAD	R	32	0x0000 0030	0x4A06 4830

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Table 23-966. OHCI Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
HCFMINTERVAL	RW	32	0x0000 0034	0x4A06 4834
HCFMREMAINING	R	32	0x0000 0038	0x4A06 4838
HCFMNUMBER	R	32	0x0000 003C	0x4A06 483C
HCPERIODICSTART	RW	32	0x0000 0040	0x4A06 4840
HCLSTHRESHOLD	RW	32	0x0000 0044	0x4A06 4844
HCRHDESCRIPTORA	RW	32	0x0000 0048	0x4A06 4848
HCRHDESCRIPTORB	RW	32	0x0000 004C	0x4A06 484C
HCRHSTATUS	RW	32	0x0000 0050	0x4A06 4850
HCRHPORTSTATUS_1	RW	32	0x0000 0054	0x4A06 4854
HCRHPORTSTATUS_2	RW	32	0x0000 0058	0x4A06 4858
HCRHPORTSTATUS_3	RW	32	0x0000 005C	0x4A06 485C

CAUTION

The OHCI registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.

OHCI register descriptions conform to the OHCI USB standard: *Open Host Controller Interface Specification for USB, Release 1.0a*. For more information about these registers or for new specification releases, search OHCI on www.usb.org.

23.10.6.5.2 OHCI Register Description

through describe the OHCI registers.

Table 23-967. HCREVISION

Address Offset	0x0000 0000		
Physical Address	0x4A06 4800	**Instance**	OHCI
Description	OHCI revision number		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								REV							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	REV	OHCI specification revision the OHCI revision number upon which the USB host controller is based. Examples: 0x10 for 1.0, 0x21 for 2.1	R	0x10

Table 23-968. Register Call Summary for Register HCREVISION

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

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Table 23-969. HCCONTROL

Address Offset	0x0000 0004		
Physical Address	0x4A06 4804	**Instance**	OHCI
Description	HC operating mode register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					RWE	RWC	IR	HCFS		BLE	CLE	IE	PLE	CBSR	

Bits	Field Name	Description	Type	Reset
31:11	RESERVED	Reserved	R	0x000000
10	RWE	Remote wake-up enable This bit is used to enable or disable the remote wakeup feature upon detection of upstream resume signaling.	RW	0
9	RWC	Remote wake-up connected. This bit indicates whether the host controller supports remote wakeup signaling.	RW	0
8	IR	Interrupt routing This bit determines the routing of interrupts generated by events registered in HCINTERRUPTSTATUS. 0x0: All interrupts are routed to the normal host bus interrupt mechanism.. 0x1: Interrupts are routed to the system management Interrupt.	RW	0
7:6	HCFS	Host controller functional state 0x0: HCFS: USB reset 0x1: HCFS: USB resume 0x2: HCFS: USB operational 0x3: HCFS: USB suspend	RW	0x0
5	BLE	Bulk list processing enable 0x0: Bulk ED list is not processed after the next SOF. 0x1: Enables processing of bulk ED list in the next frame.	RW	0
4	CLE	Control list processing enable 0x0: Control ED list is not processed after the next SOF. 0x1: Enables processing of control ED list in the next frame.	RW	0
3	IE	Isochronous ED processing enabled by host controller driver 0x0: Isochronous EDs are not processed. 0x1: Enables processing of isochronous EDs	RW	0
2	PLE	Periodic list enable 0x0: Periodic ED lists are not processed after the next frame. 0x1: Enables processing of periodic ED lists in the next frame.	RW	0
1:0	CBSR	Control/bulk service ratio. Specifies the ratio between control and bulk EDs processed in a frame. 0x0: One control ED per bulk ED 0x1: Two control ED per bulk ED 0x2: Three control ED per bulk ED 0x3: Four control ED per bulk ED	RW	0x0

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Table 23-970. Register Call Summary for Register HCCONTROL

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-971. HCCOMMANDSTATUS

Address Offset	0x0000 0008		
Physical Address	0x4A06 4808	**Instance**	OHCI
Description	HC command and status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOC		RESERVED												OCR	BLF	CLF	HCR

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17:16	SOC	Scheduling overrun count This is used to monitor any persistent scheduling problems. These bits are incremented on each scheduling overrun error. It is initialized to 0x0 and wraps around at 0x3.	R	0x0
15:4	RESERVED	Reserved	R	0x000
3	OCR	Ownership change request. This bit is set to request a change of control of the host controller.	RW	0
2	BLF	Bulk list filled This bit is used to indicate whether there are any TDs on the bulk list. It is set whenever it adds a TD to an ED in the bulk list.	RW	0
1	CLF	Control list filled This bit is used to indicate whether there are any TDs on the control list. It is set whenever it adds a TD to an ED in the control list.	RW	0
0	HCR	Host controller reset (software reset). Set this bit to initiate a USB host controller reset. This resets most USB host controller OHCI registers. OHCI register accesses must not be attempted until a read of this register returns a 0. 0x0: No effect 0x1: USB host controller is reset.	RW	0

Table 23-972. Register Call Summary for Register HCCOMMANDSTATUS

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]
- OHCI Register Description: [1]

Table 23-973. HCINTERRUPTSTATUS

Address Offset	0x0000 000C		
Physical Address	0x4A06 480C	**Instance**	OHCI
Description	HC interrupt status		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	OC	RESERVED																							RHSC	FNO	UE	RD	SF	WDH	SO

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reserved	R	0
30	OC	Ownership change This bit is set when the HCCOMMANDSTATUS[3] OCR bit is set. Read 0x1: An ownership change has occurred. Write 0x0: No effect Write 0x1: Clears this bit	R	0
29:7	RESERVED	Reserved	R	0x000000
6	RHSC	Root hub status change When 0x1: A root hub status change has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
5	FNO	Frame number overflow When 0x1: A frame number overflow has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
4	UE	Unrecoverable error When 0x1: An unrecoverable error has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
3	RD	Resume detected When 0x1: A downstream device has issued a resume request. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
2	SF	Start of frame When 0x1: A SOF has been issued. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
1	WDH	Write done head When 0x1: The USB host controller has updated the HCDONEHEAD register. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
0	SO	Scheduling overrun When 0x1: A scheduling overrun has occurred. Write 0x0: No effect Write 0x1: Clears this bit	RW	0

Table 23-974. Register Call Summary for Register HCINTERRUPTSTATUS

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]
- OHCI Register Description: [1]

Table 23-975. HCINTERRUPTENABLE

Address Offset	0x0000 0010		
Physical Address	0x4A06 4810	**Instance**	OHCI
Description	HC interrupt enable		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIE	OC	RESERVED																						RHSC	FNO	UE	RD	SF	WDH	SO	

Bits	Field Name	Description	Type	Reset
31	MIE	Master interrupt enable When 0x1: Allows other enabled OHCI interrupt sources to propagate to the device interrupt controller When 0x0: OHCI interrupt sources are ignored. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
30	OC	Ownership change Write 0x0: No effect Write 0x1: Enable interrupt generation due to ownership change.	RW	0
29:7	RESERVED	Reserved	R	0x000000
6	RHSC	Root hub status change When 0x1 and MIE is 0x1: Allows root hub status change interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: Root hub status change interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
5	FNO	Frame number overflow When 0x1 and MIE is 0x1: Allows FNO interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: FNO interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
4	UE	Unrecoverable error When 0x1 and MIE is 0x1: Allows UE interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: UE interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
3	RD	Resume detected When 0x1 and MIE is 0x1: Allows RD interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: RD interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
2	SF	Start of frame When 0x1 and MIE is 0x1: Allows SF interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: SF interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
1	WDH	Write done head When 0x1 and MIE is 0x1: Allows WDH interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: WDH interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0
0	SO	Scheduling overrun When 0x1 and MIE is 0x1: Allows SO interrupts to propagate to the device interrupt controller When 0x0 or MIE is 0x0: SO interrupts do not propagate. Write 0x0: No effect Write 0x1: Sets this bit	RW	0

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Table 23-976. Register Call Summary for Register HCINTERRUPTENABLE

High-Speed Multiport USB Host Subsystem

- HS Multiport USB Host Subsystem Global Initialization: [0]
- OHCI Register Summary: [1]
- OHCI Register Description: [2] [3] [4] [5] [6] [7] [8] [9]

Table 23-977. HCINTERRUPTDISABLE

Address Offset	0x0000 0014		
Physical Address	0x4A06 4814	**Instance**	OHCI
Description	HC interrupt disable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIE	OC	RESERVED																						RHSC	FNO	UE	RD	SF	WDH	SO	

Bits	Field Name	Description	Type	Reset
31	MIE	Master interrupt enable Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE MIE bit	RW	0
30	OC	Ownership change. Write 0x0: No effect. Write 0x1: Disable interrupt generation due to ownership change.	RW	0
29:7	RESERVED	Reserved	R	0x000000
6	RHSC	Root hub status change Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE RHSC bit	RW	0
5	FNO	Frame number overflow Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE FNO bit	RW	0
4	UE	Unrecoverable error Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE UE bit	RW	0
3	RD	Resume detected Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE RD bit	RW	0
2	SF	Start of frame Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE SF bit	RW	0
1	WDH	Write done head Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE WDH bit	RW	0
0	SO	Scheduling overrun Always reads 0x0. Write 0x0: No effect Write 0x1: Clears the HCINTERRUPTENABLE SO bit	RW	0

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Table 23-978. Register Call Summary for Register HCINTERRUPTDISABLE

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-979. HCHCCA

Address Offset	0x0000 0018		
Physical Address	0x4A06 4818	**Instance**	OHCI
Description	HC HCCA address register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HCCA																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:8	HCCA	Physical address of the beginning of the HCCA	RW	0x000000
7:0	RESERVED	Reserved	R	0x00

Table 23-980. Register Call Summary for Register HCHCCA

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-981. HCPERIODCURRENTED

Address Offset	0x0000 001C		
Physical Address	0x4A06 481C	**Instance**	OHCI
Description	HC current periodic register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	PCED	Physical address of current ED on the periodic ED list	R	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-982. Register Call Summary for Register HCPERIODCURRENTED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-983. HCCONTROLHEADED

Address Offset	0x0000 0020		
Physical Address	0x4A06 4820	**Instance**	OHCI
Description	HC head control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHED																												RESERVED			

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Bits	Field Name	Description	Type	Reset
31:4	CHED	Physical address of head ED on the control ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-984. Register Call Summary for Register HCCONTROLHEADED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-985. HCCONTROLCURRENTED

Address Offset	0x0000 0024		
Physical Address	0x4A06 4824	**Instance**	OHCI
Description	HC current control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	CCED	Physical address of current ED on the control ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-986. Register Call Summary for Register HCCONTROLCURRENTED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-987. HCBULKHEADED

Address Offset	0x0000 0028		
Physical Address	0x4A06 4828	**Instance**	OHCI
Description	HC head bulk register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BHED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	BHED	Physical address of head ED on the bulk ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-988. Register Call Summary for Register HCBULKHEADED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-989. HCBULKCURRENTED

Address Offset	0x0000 002C		
Physical Address	0x4A06 482C	**Instance**	OHCI
Description	HC current bulk register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCED																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	BCED	Physical address of current ED on the bulk ED list	RW	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-990. Register Call Summary for Register HCBULKCURRENTED

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-991. HCDONEHEAD

Address Offset	0x0000 0030		
Physical Address	0x4A06 4830	**Instance**	OHCI
Description	HC head done register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DH																												RESERVED			

Bits	Field Name	Description	Type	Reset
31:4	DH	Physical address of last TD that was added to the Done queue	R	0x0000000
3:0	RESERVED	Reserved	R	0x0

Table 23-992. Register Call Summary for Register HCDONEHEAD

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]
- OHCI Register Description: [1]

Table 23-993. HCFMINTERVAL

Address Offset	0x0000 0034		
Physical Address	0x4A06 4834	**Instance**	OHCI
Description	HC frame interval register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIT	FSMPS															RESERVED	FI														

Bits	Field Name	Description	Type	Reset
31	FIT	Frame interval toggle This bit is toggled whenever it loads a new value to FI.	RW	0
30:16	FSMPS	Largest data packet size for full-speed packets, bit times This field specifies a value which is loaded into the largest data packet counter at the beginning of each frame.	RW	0x0000

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Bits	Field Name	Description	Type	Reset
15:14	RESERVED	Reserved	R	0x0
13:0	FI	Frame interval. Number of 12-MHz clocks in the USB frame. The nominal value is set to 11,999, to give a 1-ms frame.	RW	0x2EDF

Table 23-994. Register Call Summary for Register HCFMINTERVAL

High-Speed Multiport USB Host Subsystem

- OHCI Implementation Specifications: [0]
- OHCI Register Summary: [1]
- OHCI Register Description: [2] [3] [4]

Table 23-995. HCFMREMAINING

Address Offset	0x0000 0038		
Physical Address	0x4A06 4838	**Instance**	OHCI
Description	HC frame remaining register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRT	RESERVED															FR															

Bits	Field Name	Description	Type	Reset
31	FRT	Frame remaining toggle This bit is used for the synchronization between HCFMINTERVAL[13:0] FI and FR. This bit is loaded from the HCFMINTERVAL[31] FIT bit whenever FR reaches 0.	R	0
30:14	RESERVED	Reserved	R	0x00000
13:0	FR	Frame remaining This counter is decremented at each bit time. When it reaches 0, it is reset by loading the value of the USBHOST.HCFMINTERVAL[13:0] FI bit field at the next bit time boundary.	R	0x0000

Table 23-996. Register Call Summary for Register HCFMREMAINING

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]
- OHCI Register Description: [1]

Table 23-997. HCFMNUMBER

Address Offset	0x0000 003C		
Physical Address	0x4A06 483C	**Instance**	OHCI
Description	HC frame number register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FN															

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Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15:0	FN	Frame number This is incremented when HCFMREMAINING is reloaded. It is rolled over to 0x0000 after 0xFFFF.	R	0x0000

Table 23-998. Register Call Summary for Register HCFMNUMBER

High-Speed Multiport USB Host Subsystem • OHCI Register Summary: [0]

Table 23-999. HCPERIODICSTART

Address Offset	0x0000 0040		
Physical Address	0x4A06 4840	**Instance**	OHCI
Description	HC periodic start register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PS							

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:0	PS	Periodic start. The host controller driver must program this value to be about 10 percent less than the frame interval field value so that control and bulk EDs have priority for the first 10 percent of the frame; then periodic EDs have priority for the remaining 90 percent of the frame.	RW	0x0000

Table 23-1000. Register Call Summary for Register HCPERIODICSTART

High-Speed Multiport USB Host Subsystem • OHCI Register Summary: [0]

Table 23-1001. HCLSTHRESHOLD

Address Offset	0x0000 0044		
Physical Address	0x4A06 4844	**Instance**	OHCI
Description	HC low-speed threshold register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LST							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x00000
11:0	LST	Low-speed threshold	RW	0x628

Table 23-1002. Register Call Summary for Register HCLSTHRESHOLD

High-Speed Multiport USB Host Subsystem • OHCI Register Summary: [0]

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Table 23-1003. HCRHDESCRIPTORA

Address Offset	0x0000 0048		
Physical Address	0x4A06 4848	**Instance**	OHCI
Description	HC root hub A register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POTPG								RESERVED											NOCP	OCPM	DT	NPS	PSM	NDP							

Bits	Field Name	Description	Type	Reset
31:24	POTPG	Power-on to power-good time. Defines the minimum amount of time (2 ms * POTPG) between the USB host controller turning on power to a downstream port and when the USB host can access the downstream device.	RW	0x0A
23:13	RESERVED	Reserved	R	0x0
12	NOCP	No overcurrent protection. This function is not supported at the device level. 0x0: Overcurrent status is reported collectively for all downstream ports. 0x1: The USB host controller does not implement overcurrent protection inputs.	RW	0x0
11	OCPM	Overcurrent protection mode. This function is not supported at the device level.	RW	0x1
10	DT	Device type Always reads 0x0: Indicates that the USB host controller implemented is not a compound device.	R	0
9	NPS	No power switching 0x0: VBUS power switching is supported, either per-port or all-port switched per the power. 0x1: VBUS power switching is not supported; power is available to all downstream ports.	RW	0
8	PSM	Power switching mode 0x0: Indicates that all ports are powered at the same time 0x1: Individual port power switching is supported.	RW	1
7:0	NDP	Number of downstream ports These bits specify the number of downstream ports supported by the root hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OHCI is 15.	R	0x03

Table 23-1004. Register Call Summary for Register HCRHDESCRIPTORA

High-Speed Multiport USB Host Subsystem

- OHCI Implementation Specifications: [0] [1] [2] [3]
- OHCI Register Summary: [4]

Table 23-1005. HCRHDESCRIPTORB

Address Offset	0x0000 004C		
Physical Address	0x4A06 484C	**Instance**	OHCI
Description	HC root hub B register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPCM																DR															

Bits	Field Name	Description	Type	Reset
31:16	PPCM	Port power control mask. Each bit defines whether a corresponding downstream port has port power controlled by the global power control. When set, the port's power state is only affected by per-port power control. When cleared, the port is controlled by the global power switch. If the device is configured to global switch mode this field is not valid. Bit 0: Reserved, bit 1: Ganged-power mask on port 1, ..., bit 15: Ganged-power mask on port 15.	RW	0x0000
15:0	DR	Device removable. Each bit defines whether a corresponding downstream port has a removable device. When cleared, the attached device is removable. When set, the attached device is not removable. Bit 0: Reserved, bit 1: Device attached to port 1, ... bit 15: Device attached to port 15.	RW	0x0000

Table 23-1006. Register Call Summary for Register HCRHDESCRIPTORB

High-Speed Multiport USB Host Subsystem

- OHCI Implementation Specifications: [0] [1]
- OHCI Register Summary: [2]
- OHCI Register Description: [3] [4] [5] [6] [7] [8]

Table 23-1007. HCRHSTATUS

Address Offset	0x0000 0050		
Physical Address	0x4A06 4850	**Instance**	OHCI
Description	HC root hub status register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRWE	RESERVED														LPSC	DRWE	RESERVED														LPS

Bits	Field Name	Description	Type	Reset
31	CRWE	Clear remote wakeup enable Write 0x0: No effect Write 0x1: Clears the device remote wake-up enable bit	W	0
30:17	RESERVED	Reserved	R	0x0000
16	LPSC	Local power status change Always reads 0x0: The root hub does not support the local power status feature. Write 0x0: No effect Write 0x1: Sets port power status bits for all ports, if power switching mode is 0. Sets port power status bits for ports with their corresponding port power control mask bits cleared if power switching mode is 1.	RW	0
15	DRWE	Device remote wake-up enable. Enables a connect status change event as a resume event, causing a USB suspend to USB resume state transition and sets the resume detected interrupt status bit. Read 0x1: Connect status change is a remote wake-up event. Read 0x0: Connect status change is not a remote wake-up event. Write 0x0: No effect Write 0x1: Sets the device remote wake-up enable bit	RW	0

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Bits	Field Name	Description	Type	Reset
14:1	RESERVED	Reserved	R	0x0000
0	LPS	Local power status Always reads 0x0 Write 0x0: No effect Write 0x1: When in global power mode (power switching mode = 0), turns off power to all ports. If in per-port power mode (power switching mode = 1), turns of power to those ports whose corresponding port power control mask bit is 0.	RW	0

Table 23-1008. Register Call Summary for Register HCRHSTATUS

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1009. HCRHPORTSTATUS_1

Address Offset	0x0000 0054		
Physical Address	0x4A06 4854	**Instance**	OHCI
Description	HC port 1 status and control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRSC	RESERVED	PSSC	PESC	CSC	RESERVED							LSDA_CPP	PPS_SPP	RESERVED			PRS_SPR	POCI_CSS	PSS_SPS	PES_SPE	CCS_CPE

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved	R	0x000
20	PRSC	Port 1 reset status change. This bit is set when the port 1 port reset status bit has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
19	RESERVED		R	0
18	PSSC	Port 1 suspends status change. Set when the port leaves the suspend state; that is, after the full resume sequence has completed. Write 0x0: No effect Read 0x0: No resume completed (since either the last software clear, or the last port reset). Read 0x1: Resume completed on the port Write 0x1: Clears the bit	RW	0
17	PESC	Port 1 enable status change. This bit is set when the port 1 port enable status has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
16	CSC	Port 1 connect status change. This bit is set when the port1 port current connect status has changed due to a connect or disconnect event. If current connect status is 0 when a set port reset, set port enable, or set port suspend write occurs, this bit is set. Write 0x0: No effect Write 0x1: Clears this bit **Note:** If the HCRHDESCRIPTORB[1] DR bit is set, this bit is set only after a root hub reset to inform the system that the device is attached.	RW	0
15:10	RESERVED	Reserved	R	0x00

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Bits	Field Name	Description	Type	Reset
9	LSDA_CPP	Port 1 low-speed device attached/clear port power. This bit is valid only when port 1 current connect status is 1. Read 0x0: A full-speed device is attached to port 1. Read 0x1: A low-speed device is attached to port 1. Write 0x0: No effect Write 0x1: Clears the port 1 port power status	RW	0
8	PPS_SPP	Port 1 port power status/set port power Read 0x0: Port 1 power is enabled. Read 0x1: Port 1 power is not enabled. Write 0x0: No effect Write 0x1: Sets the port 1 port power status bit	RW	0
7:5	RESERVED	Reserved	R	0x0
4	PRS_SPR	Port 1 port reset status/set port reset Read 0x0: USB reset is not being sent to port 1. Read 0x1: Port 1 is signaling the USB reset. Write 0x0: No effect Write 0x1: Sets the port 1 port reset status bit and causes the USB host controller to begin signaling USB reset to port 1	RW	0
3	POCI_CSS	Port 1 overcurrent indicator (not implemented)/clear suspend status. Read 0x0: no port 1 port overcurrent condition has occurred. Read 0x1: a port 1 port overcurrent condition has occurred. Write 0x0: no effect. Write 0x1: when port 1 port suspend status is 1 causes resume signalling on port 1. When port 1 port suspend status is 0 has no effect.	RW	0
2	PSS_SPS	Port 1 port suspend status/set port suspend. This bit is cleared automatically at the end of the USB resume sequence and also at the end of the USB reset sequence. Write 0x0: No effect Read 0x0: Port 1 is not in the USB suspend state. Read 0x1: Port 1 is in the USB suspend state or is in the resume sequence. Write 0x1: If port 1 current connect status is 1, sets the port 1 port suspend status bit and places port 1 in USB suspend state. If current connect status is 0, sets instead connect status change to inform the USB host controller driver of an attempt to suspend a disconnected port.	RW	0
1	PES_SPE	Port 1 port enable status/set port enable. This bit is automatically set at completion of port 1 USB reset if it was not already set before the USB reset completed, and is automatically set at the end of a USB suspend if the port was not enabled when the USB resume completed. Read 0x0: Port 1 is not enabled. Read 0x1: Port 1 is enabled. Write 0x0: No effect Write 0x1: When port 1 current connect status is 1 sets the port 1 port enable status bit. When port 1 current status is 0 has no effect.	RW	0
0	CCS_CPE	Port 1 current connection status/clear port enable Read 0x0: No USB device is attached to port 1. Read 0x1: A USB device is currently attached to port 1. Write 0x0: No effect Write 0x1: Clears the port 1 port enable bit Note: This bit is set to 1 if the HCRHDESCRIPTORB[1 DR bit] is set to indicate a nonremovable device on port 1.	RW	0

Table 23-1010. Register Call Summary for Register HCRHPORTSTATUS_1

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

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Table 23-1011. HCRHPORTSTATUS_2

Address Offset	0x0000 0058		
Physical Address	0x4A06 4858	**Instance**	OHCI
Description	HC port 2 status and control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRSC	RESERVED	PSSC	PESC	CSC	RESERVED							LSDA_CPP	PPS_SPP	RESERVED			PRS_SPR	POCI_CSS	PSS_SPS	PES_SPE	CCS_CPE

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved	R	0x000
20	PRSC	Port 2 reset status change. This bit is set when the port 2 port reset status bit has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
19	RESERVED		RW	0
18	PSSC	Port 2 suspend status change. Set when the port leaves the suspend state; that is, after the full resume sequence has completed. Write 0x0: No effect Read 0x0: No resume completed (since either the last software clear, or the last port reset). Read 0x1: Resume completed on the port. Write 0x1: Clears the bit	RW	0
17	PESC	Port 2 enable status change. This bit is set when the port 2 port enable status has changed. Write 0x0: No effect Write 0x1: Clears this bit	RW	0
16	CSC	Port 2 connect status change. This bit is set when the port 2 port current connect status has changed due to a connect or disconnect event. If current connect status is 0 when a set port reset, set port enable, or set port suspend write occurs, this bit is set. Write 0x0: No effect Write 0x1: Clears this bit **Note:** If the HCRHDESCRIPTORB[1] DR bit is set, this bit is set only after a root hub reset to inform the system that the device is attached.	RW	0
15:10	RESERVED	Reserved	R	0x00
9	LSDA_CPP	Port 2 low-speed device attached/clear port power. This bit is valid only when port 2 current connect status is 1. Read 0x0: A full-speed device is attached to port 2. Read 0x1: A low-speed device is attached to port 2. Write 0x0: No effect Write 0x1: Clears the port 2 port power status	RW	0
8	PPS_SPP	Port 2 port power status/set port power Read 0x0: Port 2 power is enabled. Read 0x1: Port 2 power is not enabled. Write 0x0: No effect Write 0x1: Sets the port 2 port power status bit	RW	0
7:5	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
4	PRS_SPR	Port 2 port reset status/set port reset Read 0x0: USB reset is not being sent to port 2. Read 0x1: Port 2 is signaling the USB reset. Write 0x0: No effect Write 0x1: Sets the port 2 port reset status bit and causes the USB host controller to begin signaling USB reset to port 2	RW	0
3	POCI_CSS	Port 2 overcurrent indicator (not implemented)/clear suspend status. Read 0x0: no port 3 port overcurrent condition has occurred. Read 0x1: a port 3 port overcurrent condition has occurred. Write 0x0: no effect. Write 0x1: when port 2 port suspend status is 1 causes resume signalling on port 2. When port 2 port suspend status is 0 has no effect.	RW	0
2	PSS_SPS	Port 2 port suspend status/set port suspend. This bit is cleared automatically at the end of the USB resume sequence and also at the end of the USB reset sequence. Write 0x0: No effect Read 0x0: Port 2 is not in the USB suspend state. Read 0x1: Port 2 is in the USB suspend state or is in the resume sequence. Write 0x1: If port 2 current connect status is 1, sets the port 2 port suspend status bit and places port 2 in USB suspend state. If current connect status is 0, sets instead connect status change to inform the USB host controller driver of an attempt to suspend a disconnected port.	RW	0
1	PES_SPE	Port 2 port enable status/set port enable. This bit is automatically set at completion of port 2 USB reset if it was not already set before the USB reset completed, and is automatically set at the end of a USB suspend if the port was not enabled when the USB resume completed. Read 0x0: Port 2 is not enabled. Read 0x1: Port 2 is enabled. Write 0x0: No effect Write 0x1: When port 2 current connect status is 1 sets the port 2 port enable status bit. When port 2 current status is 0 has no effect.	RW	0
0	CCS_CPE	Port 2 current connection status/clear port enable Read 0x0: No USB device is attached to port 2. Read 0x1: A USB device is currently attached to port 2. Write 0x0: No effect Write 0x1: Clears the port 2 port enable bit **Note:** This bit is set to 1 if the HCRHDESCRIPTORB[1] DR bit is set to indicate a nonremovable device on port 2.	RW	0

Table 23-1012. Register Call Summary for Register HCRHPORTSTATUS_2

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

Table 23-1013. HCRHPORTSTATUS_3

Address Offset	0x0000 005C		
Physical Address	0x4A06 485C	**Instance**	OHCI
Description	HC Port 3 Status and Control Register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRSC	OCIC	PSSC	PESC	CSC	RESERVED						LSDA_CPP	PPS_SPP	RESERVED			PRS_SPR	POCI_CSS	PSS_SPS	PES_SPE	CCS_CPE

Bits	Field Name	Description	Type	Reset
31:21	RESERVED	Reserved	R	0x000
20	PRSC	Port 3 reset status change. This bit is set when the Port 3 port reset status bit has changed. Write 0x0: no effect. Write 0x1: clears this bit.	RW	0
19	OCIC	Port 3 overcurrent indicator change. This bit is set when the Port 3 port overcurrent indicator has changed. Write 0x0 no effect. Write 0x1: clears this bit.	RW	0
18	PSSC	Port 3 suspend status change. Set when the port leaves the suspend state, i.e. after the full resume sequence has completed. Write 0x0: No effect Write 0x1: Clears the bit Read 0x1: Resume completed on the port Read 0x0: No resume completed (since either the last SW clear, or the last port reset)	RW	0
17	PESC	Port 3 enable status change. This bit is set when the Port 3 port enable status has changed. Write 0x0: no effect. Write 0x1: clears this bit.	RW	0
16	CSC	Port 3 connect status change. This bit is set when the Port 3 port current connect status has changed due to a connect or disconnect event. If current connect status is 0 when a set port reset, set port enable, or set port suspend write occurs, this bit is set. Write 0x0: no effect. Write 0x1: clears this bit. Note: If the DR bit HCRHDESCRIPTORB[1] is set, this bit is set only after a root hub reset to inform the system that the device is attached.	RW	0
15:10	RESERVED	Reserved	R	0x00
9	LSDA_CPP	Port 3 low-speed device attached/clear port power. This bit is valid only when port 3 current connect status is 1. Read 0x0: a full-speed device is attached to port 3. Read 0x1: a low-speed device is attached to port 3. Write 0x0: no effect. Write 0x1: clears the port 3 port power status.	RW	0
8	PPS_SPP	Port 3 power status/set port power. Read 0x0: port 3 power is enabled. Read 0x1: port 3 power is not enabled. Write 0x0: no effect. Write 0x1: sets the port 3 port power status bit.	RW	0
7:5	RESERVED	Reserved	R	0x0
4	PRS_SPR	Port 3 reset status/set port reset. Read 0x0: USB reset is not being sent to port 3. Read 0x1: port 3 is signaling the USB reset. Write 0x0: no effect. Write 0x1: sets the port 3 port reset status bit and causes the USB host controller to begin signaling USB reset to port 3.	RW	0

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Bits	Field Name	Description	Type	Reset
3	POCI_CSS	Port 3 overcurrent indicator (not implemented)/clear suspend status. Read 0x0: no port 3 port overcurrent condition has occurred. Read 0x1: a port 3 port overcurrent condition has occurred. Write 0x0: no effect. Write 0x1: when port 3 port suspend status is 1 causes resume signalling on port 3. When port 3 port suspend status is 0 has no effect.	RW	0
2	PSS_SPS	Port 3 port suspend status/set port suspend. This bit is cleared automatically at the end of the USB resume sequence and also at the end of the USB reset sequence. Write 0x0: no effect. Read 0x0: port 3 is not in the USB suspend state. Read 0x1: port 3 is in the USB suspend state or is in the resume sequence. Write 0x1: If port 3 current connect status is 1, sets the port 3 port suspend status bit and places port 3 in USB suspend state. If current connect status is 0, sets instead connect status change to inform the USB host controller driver of an attempt to suspend a disconnected port.	RW	0
1	PES_SPE	Port 3 enable status/set port enable. This bit is automatically set at completion of port 3 USB reset if it was not already set before the USB reset completed, and is automatically set at the end of a USB suspend if the port was not enabled when the USB resume completed. Read 0x0: port 3 is not enabled. Read 0x1: port 3 is enabled. Write 0x0: no effect. Write 0x1: When port 3 current connect status is 1 sets the port 3 port enable status bit. When port 3 current status is 0 has no effect.	RW	0
0	CCS_CPE	Port 3 current connection status/clear port enable. Read 0x0: no USB device is attached to port 3. Read 0x1: port 3 currently has a USB device attached. Write 0x0: no effect. Write 0x1: clears the port 3 port enable bit. Note: This bit is set to 1 if the DR bit HCRHDESCRIPTORB[1] is set to indicate a non-removable device on port 3.	RW	0

Table 23-1014. Register Call Summary for Register HCRHPORTSTATUS_3

High-Speed Multiport USB Host Subsystem

- OHCI Register Summary: [0]

23.10.6.6 EHCI Registers

23.10.6.6.1 EHCI Register Summary

Table 23-1015 summarizes the EHCI register mapping.

Table 23-1015. EHCI Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
HCCAPBASE	R	32	0x0000 0000	0x4A06 4C00
HCSPARAMS	R	32	0x0000 0004	0x4A06 4C04
HCCPARAMS	R	32	0x0000 0008	0x4A06 4C08
USBCMD	RW	32	0x0000 0010	0x4A06 4C10
USBSTS	RW	32	0x0000 0014	0x4A06 4C14
USBINTR	RW	32	0x0000 0018	0x4A06 4C18

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Table 23-1015. EHCI Register Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
FRINDEX	RW	32	0x0000 001C	0x4A06 4C1C
CTRLDSSEGMENT	R	32	0x0000 0020	0x4A06 4C20
PERIODICLISTBASE	RW	32	0x0000 0024	0x4A06 4C24
ASYNCLISTADDR	RW	32	0x0000 0028	0x4A06 4C28
CONFIGFLAG	RW	32	0x0000 0050	0x4A06 4C50
PORTSC_i (1)	RW	32	0x0000 0054 + (0x4 * i)	0x4A06 4C54 + (0x4 * i)
INSNREG00	RW	32	0x0000 0090	0x4A06 4C90
INSNREG01	RW	32	0x0000 0094	0x4A06 4C94
INSNREG02	RW	32	0x0000 0098	0x4A06 4C98
INSNREG03	RW	32	0x0000 009C	0x4A06 4C9C
INSNREG04	RW	32	0x0000 00A0	0x4A06 4CA0
INSNREG05_UTMI	RW	32	0x0000 00A4	0x4A06 4CA4
INSNREG05_ULPI	RW	32	0x0000 00A4	0x4A06 4CA4
INSNREG06	RW	32	0x0000 00A8	0x4A06 4CA8
INSNREG07	R	32	0x0000 00AC	0x4A06 4CAC
INSNREG08	RW	32	0x0000 00B0	0x4A06 4CB0

(1) i = 0 to 2

CAUTION

The EHCI registers are limited to 32-bit data accesses; 16-bit and 8-bit accesses are not allowed and can corrupt register content.

EHCI register descriptions conform to the EHCI USB standard: *Enhanced Host Controller Interface (EHCI) Specification for USB, Release 1.1*. For more information about these registers or for new specification releases, search EHCI on www.usb.org.

23.10.6.6.2 EHCI Register Description

through describe the EHCI registers.

Table 23-1016. HCCAPBASE

Address Offset	0x0000 0000		
Physical Address	0x4A06 4C00	**Instance**	EHCI
Description	Host controller capability register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HCIVERSION																RESERVED								CAPLENGTH							

Bits	Field Name	Description	Type	Reset
31:16	HCIVERSION	Interface version number. It contains a BCD encoding of the EHCI revision number supported by this host controller. [7:4] Major revision [3:0] Minor revision	R	0x0100
15:8	RESERVED	Reserved	R	0x00
7:0	CAPLENGTH	Capability register length	R	0x10

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Table 23-1017. Register Call Summary for Register HCCAPBASE

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1018. HCSPARAMS

Address Offset	0x0000 0004		
Physical Address	0x4A06 4C04	**Instance**	EHCI
Description	Host controller structural parameters		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RESERVED			P_INDICATOR	N_CC				N_PCC				PRR	RESERVED		PPC	N_PORTS			

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:17	RESERVED	Reserved	R	0x0
16	P_INDICATOR	Port indicator support indication This bit indicates whether the ports support port indicator control. 0x1: The port status and control registers include a read/write field for controlling the state of the port indicator.	R	0
15:12	N_CC	Number of companion controllers This field indicates the number of companion controllers associated with this USB 2.0 host controller. 0x0: There are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. Others: There are companion USB 1.1 host controller(s). Port-ownership hand-off is supported. High-, full-, and low-speed devices are supported on the host controller root ports.	R	0x1
11:8	N_PCC	Number of ports per companion controller This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC can have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, etc. The number in this field must be consistent with N_PORTS and N_CC.	R	0x3
7	PRR	Port routing rules The first N_PCC ports are routed to the lowest-numbered function companion host controller, the next N_PCC ports are routed to the next lowest-function companion controller, and so on.	R	0
6:5	RESERVED	Reserved	R	0x0
4	PPC	Port power control This field indicates whether the host controller implementation includes port power control.	R	1

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Bits	Field Name	Description	Type	Reset
		0x0: The ports do not have port power switches. 0x1: The ports have port power switches.		
3:0	N_PORTS	Number of downstream ports This field specifies the number of physical downstream ports implemented on this host controller.	R	0x3

Table 23-1019. Register Call Summary for Register HCSPARAMS

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1] [2] [3]

Table 23-1020. HCCPARAMS

Address Offset	0x0000 0008		
Physical Address	0x4A06 4C08	**Instance**	EHCI
Description	Host controller capability parameters		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LPM	RESERVED	EECP								IST				RESERVED	ASPC	PFLF	BIT64AC

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x0000
17	LPM	Link power management capability 0: Link power management not supported 1: Link power management supported	R	1
16	RESERVED	Reserved	R	0
15:8	EECP	EHCI extended capabilities pointer This field indicates the existence of a capabilities list. 0x0: No extended capabilities are implemented. Others: The offset in PCI configuration space of the first EHCI extended capability.	R	0x00
7:4	IST	Isochronous scheduling threshold This field indicates where software can reliably update the isochronous schedule in relation to the current position of the executing host controller. The host controller can hold one microframe of isochronous data structures before flushing the state.	R	0x1
3	RESERVED	Reserved	R	0
2	ASPC	Asynchronous schedule park capability 0x1: The host controller supports the park feature for high-speed queue heads in the asynchronous schedule. The feature can be disabled or enabled and set to a specific level by using the USBHOST.USBCMD[11]ASPME bit and the USBHOST.USBCMD[9:8] ASPMC bit field.	R	1
1	PFLF	Programmable frame list flag 0x0: System software must use a frame list length of 1024 elements with this host controller.	R	1

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Bits	Field Name	Description	Type	Reset
		0x1: System software can specify and use a smaller frame list and configure the host controller through the USBHOST.USBCMD[3:2] FLS bit field. The frame list must always be aligned on a 4-K page boundary.		
0	BIT64AC	64-bit addressing capability This field documents the addressing range capability of this implementation. 0x0: Data structures using 32-bit address memory pointers 0x1: Data structures using 64-bit address memory pointers	R	0

Table 23-1021. Register Call Summary for Register HCCPARAMS

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1]

Table 23-1022. USBCMD

Address Offset	0x0000 0010		
Physical Address	0x4A06 4C10	**Instance**	EHCI
Description	USB command		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HIRD								ITC				RESERVED				ASPME	RESERVED	ASPMC		LHCR	IAAD	ASE	PSE	FLS			HCR	RS

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved	R	0x0
27:24	HIRD	Host-initiated resume duration. If LPM is enabled, this field is RW; otherwise, it is R. The minimum for K-state during resume from LPM: 0x0: 50 µs Each increment adds 75 µs.	RW	0x0
23:16	ITC	Interrupt threshold control This field is used by the system software to select the maximum rate at which the host controller issues interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. 0x00: Reserved 0x01: 1 microframe 0x02: 2 microframes 0x04: 4 microframes 0x08: 8 microframes (default, equates to 1 ms) 0x10: 16 microframes (2 ms) 0x20: 32 microframes (4 ms) 0x40: 64 microframes (8 ms) Others: Undefined	RW	0x08
15:12	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
11	ASPME	Asynchronous schedule park mode enable 0x0: Park mode is disabled. 0x1: Park mode is enabled.	RW	1
10	RESERVED	Reserved	R	0
9:8	ASPMC	Asynchronous schedule park mode count It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the asynchronous schedule. Valid values are 0x1 to 0x3. Software must not write 0 to this bit when park mode enable is 1 because this may result in undefined behavior.	RW	0x3
7	LHCR	Light host controller reset It allows the driver to reset the EHCI controller without affecting the state of the ports or the relationship to the companion host controllers. Read 0x0: Light host controller reset is complete and it is safe for host software to reinitialize the host controller. Read 0x1: Light host controller reset is still ongoing.	RW	0
6	IAAD	Interrupt on async advance doorbell This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Write 0x1: Ring the doorbell. Software must not write 1 to this bit when the asynchronous schedule is disabled. Doing so may yield undefined results.	RW	0
5	ASE	Asynchronous schedule enable This bit controls whether the host controller skips processing the asynchronous schedule. 0x0: Do not process the asynchronous schedule 0x1: Use the USBHOST.ASYNCLISTADDR register to access the asynchronous schedule.	RW	0
4	PSE	Periodic schedule enable This bit controls whether the host controller skips processing the periodic schedule. 0x0: Do not process the periodic schedule 0x1: Use the USBHOST.PERIODICLISTBASE register to access the periodic schedule.	RW	0
3:2	FLS	Frame list size This field specifies the size of the frame list. The size of the frame list controls which bits in the frame index register should be used for the frame list current index. 0x0: 1024 elements (4096 bytes) 0x1: 512 elements (2048 bytes) 0x2: 256 elements (1024 bytes), for resource-constrained environments 0x3: Reserved	RW	0
1	HCR	Host controller reset This control bit is used by software to reset the host controller. Write 0x1: Reset the host controller, the PCI configuration registers are not affected by this reset and all operational registers are set to their initial values. This bit is set to 0 by the host controller when the reset process is complete.	W	0

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Bits	Field Name	Description	Type	Reset
0	RS	Run/stop 0x1: Run, the host controller proceeds with execution of the schedule. The host controller continues execution as long as this bit is set to 1. 0x0: Stop, the host controller completes the current and any actively pipelined transactions on the USB and then halts.	RW	0

Table 23-1023. Register Call Summary for Register USBCMD

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1] [2] [3] [4] [5]

Table 23-1024. USBSTS

Address Offset	0x0000 0014		
Physical Address	0x4A06 4C14	**Instance**	EHCI
Description	USB status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ASS	PSS	REC	HCH	RESERVED				IAA	HSE	FLR	PCD	USBEI	USBI		

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved	R	0x0000
15	ASS	Asynchronous schedule status The bit reports the current real status of the asynchronous schedule. 0x0: The status of the asynchronous schedule is disabled. 0x1: The status of the asynchronous schedule is enabled.	R	0
14	PSS	Periodic schedule status The bit reports the current real status of the periodic schedule. 0x0: The status of the periodic schedule is disabled. 0x1: The status of the periodic schedule is enabled.	R	0
13	REC	Reclamation It is used to detect an empty asynchronous schedule.	R	0
12	HCH	Host controller halted This bit is a 0 whenever the USBHOST.USBCMD[0] RS bit is a 1. The host controller sets this bit to 1 after it has stopped executing as a result of the RS bit being set to 0, either by software or by the host controller hardware.	R	1
11:6	RESERVED	Reserved	R	0x00
5	IAA	Interrupt on async advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by setting the USBHOST.USBCMD[6] IAAD bit to 1. This status bit indicates the assertion of that interrupt source.	RW	0
4	HSE	Host system error	RW	0

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Bits	Field Name	Description	Type	Reset
		The host controller sets this bit to 1 when a serious error occurs during a host system access involving the host controller module.		
3	FLR	Frame list rollover The host controller sets this bit to 1 when the USBHOST.FRINDEX rolls over from its maximum value to 0. The exact value at which the rollover occurs depends on the frame list size.	RW	0
2	PCD	Port change detect The host controller sets this bit to 1 when any port for which the USBHOST.PORTSC_i[13] PO bit is set to 0 has a change bit transition from 0 to 1 or a USBHOST.PORTSC_i[6] FPR bit transition from 0 to 1. This bit is also set as a result of the USBHOST.PORTSC_i[1] CSC bit being set to 1 after system software has relinquished ownership of a connected port by setting the USBHOST.PORTSC_i[13] PO bit to 1.	RW	0
1	USBEI	USB error interrupt The host controller sets this bit to 1 when completion of a USB transaction results in an error condition.	RW	0
0	USBI	USB interrupt The host controller sets this bit to 1 on completion of a USB transaction, which results in the retirement of a transfer descriptor that had its IOC bit set. The host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).	RW	0

Table 23-1025. Register Call Summary for Register USBSTS

High-Speed Multiport USB Host Subsystem

- UHH_CONFIG Register Description: [0]
- EHCI Register Summary: [1]
- EHCI Register Description: [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]

Table 23-1026. USBINTR

Address Offset	0x0000 0018		
Physical Address	0x4A06 4C18	**Instance**	EHCI
Description	USB interrupt enable		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										IAAE	HSEE	FLRE	PCIE	USBEIE	USBIE

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5	IAAE	Interrupt on async advance enable 0x1: When the USBSTS[5] IAA bit is 1, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBSTS[5] IAA bit.	RW	0
4	HSEE	Host system error enable	RW	0

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Bits	Field Name	Description	Type	Reset
		0x1: When the USBSTS[4] HSE bit is 1, the host controller issues an interrupt. The interrupt is acknowledged by software clearing the USBSTS[4] HSE bit.		
3	FLRE	Frame list rollover enable 0x1: When the USBSTS[3] FLR bit is 1, the host controller issues an interrupt. The interrupt is acknowledged by software clearing the USBSTS[3] FLR bit.	RW	0
2	PCIE	Port change interrupt enable 0x1: When the USBSTS[2] PCD bit is 1, the host controller issues an interrupt. The interrupt is acknowledged by software clearing the USBSTS[3] FLR bit.	RW	0
1	USBEIE	USB error interrupt enable 0x1: When the USBSTS[1] USBEI bit is 1, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBSTS[1] USBEI bit.	RW	0
0	USBIE	USB interrupt enable 0x1: When the USBSTS[0] USBI bit is 1, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBSTS[0] USBI bit.	RW	0

Table 23-1027. Register Call Summary for Register USBINTR

High-Speed Multiport USB Host Subsystem

- HS Multiport USB Host Subsystem Global Initialization: [0]
- EHCI Register Summary: [1]

Table 23-1028. FRINDEX

Address Offset	0x0000 001C		
Physical Address	0x4A06 4C1C	**Instance**	EHCI
Description	USB frame index		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																FI															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED	Reserved	R	0x00000
13:0	FI	Frame index The value in this register is incremented at the end of each time frame.	RW	0x0000

Table 23-1029. Register Call Summary for Register FRINDEX

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1]

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Table 23-1030. CTRLDSSEGMENT

Address Offset	0x0000 0020		
Physical Address	0x4A06 4C20	**Instance**	EHCI
Description	4G segment selector		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDSS																															

Bits	Field Name	Description	Type	Reset
31:0	CDSS	This 32-bit register corresponds to the most-significant address bits [63:32] for all EHCI data structures.	R	0x00000000

Table 23-1031. Register Call Summary for Register CTRLDSSEGMENT

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1032. PERIODICLISTBASE

Address Offset	0x0000 0024		
Physical Address	0x4A06 4C24	**Instance**	EHCI
Description	Frame list base address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAL																RESERVED															

Bits	Field Name	Description	Type	Reset
31:12	BAL	Base address (low) These bits correspond to memory address signals.	RW	0x00000
11:0	RESERVED	Reserved	R	0x000

Table 23-1033. Register Call Summary for Register PERIODICLISTBASE

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1]

Table 23-1034. ASYNCLISTADDR

Address Offset	0x0000 0028		
Physical Address	0x4A06 4C28	**Instance**	EHCI
Description	Next asynchronous list address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPL																											RESERVED			

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Bits	Field Name	Description	Type	Reset
31:5	LPL	Link pointer low It contains the address of the next asynchronous queue head to be executed.	RW	0x0000000
4:0	RESERVED	Reserved	R	0x00

Table 23-1035. Register Call Summary for Register ASYNCLISTADDR

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1]

Table 23-1036. CONFIGFLAG

Address Offset	0x0000 0050		
Physical Address	0x4A06 4C50	**Instance**	EHCI
Description	Configured flag register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															CF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x00000000
0	CF	Configure flag This bit controls the default port-routing control logic. 0x0: Port routing control logic default-routes each port to an implementation-dependent classic host controller. 0x1: Port routing control logic default-routes all ports to this host controller.	RW	0

Table 23-1037. Register Call Summary for Register CONFIGFLAG

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description: [1] [2]

Table 23-1038. PORTSC_i

Address Offset	0x0000 0054 + (0x4 * i)	**Index**	i = 0 to 2
Physical Address	0x4A06 4C54 + (0x4 * i)	**Instance**	EHCI
Description	Port status/control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICEADDRESS								SUSPENDSTATUS	RESERVED	WDE	WCE	PTC				PIC		PO	PP	LS		SUSPENDL1	PR	SUS	FPR	RESERVED			PEDC	PED	CSC	CCS

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Bits	Field Name	Description	Type	Reset
31:25	DEVICEADDRESS	The USB device address for the device attached to and immediately downstream from the associated root port. R/W only if LPM is enabled; otherwise, R.	RW	0x00
24:23	SUSPENDSTATUS	Addition for LPM support. Indicates status of L1 suspend request: 0x0: Success 0x1: Not yet 0x2: Not supported 0x3: Time-out/error	R	0x0
22	RESERVED	Reserved	R	0
21	WDE	Wake on disconnect enable This field is 0 if the PP bit is 0. Write 0x1: Enables the port to be sensitive to device disconnects as wake-up events.	RW	0
20	WCE	Wake on connect enable This field is 0 if the PP bit is 0. Write 0x1: Enables the port to be sensitive to device connects as wake-up events.	RW	0
19:16	PTC	Port test control The port is operating in specific test modes as indicated by the specific value. The encoding of the test mode bits are: 0x0: Test mode not enabled 0x1: Test J_STATE 0x2: Test K_STATE 0x3: Test SE0_NAK 0x4: Test Packet 0x5: Test FORCE_ENABLE Others: Reserved	RW	0x0
15:14	PIC	Port indicator control (not implemented)	R	0x0
13	PO	Port owner This bit unconditionally goes to 0x0 when the USBHOST.CONFIGFLAG[0] CF bit makes a transition from 0 to 1. This bit unconditionally goes to 0 whenever the USBHOST.CONFIGFLAG[0] CF bit is 0. 0x1: A companion host controller owns and controls the port.	RW	1
12	PP	Port power The function of this bit depends on the value of the USBHOST.HCSPARAMS[4] PPC bit. The behavior is as follows: **PPC** / **PP** / **Operation** 0x0 / 0x0 / Forbidden 0x0 / 0x1 / Host controller does not have port power. control switches. Each port is hardwired to power. 0x1 / 0x0 / Host controller has port power control switches. Current switch state is off. 0x1 / 0x1 / Host controller has port power control switches. Current switch state is on. When an overcurrent condition is detected on a powered port and the USBHOST.HCSPARAMS[4] PPC bit is a 1, the PP bit in each affected port may be transitioned by the host controller from 1 to 0.	RW	0
11:10	LS	Line status These bits reflect the current logical levels of the D+ (bit 11) and D– (bit 10) signal lines. This field is valid only when the port enable bit is 0 and the current connect status bit is set to 1. The encoding of the bits is:	R	0x0

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Bits	Field Name	Description			Type	Reset
		Bits[11:10]	**USB State**	**Interpretation**		
		0x0	SE0	Not low-speed device, perform EHCI reset.		
		0x2	J-state	Not low-speed device, perform EHCI reset.		
		0x1	K-state	Low-speed device, release ownership of port.		
		0x3	Undefined	Not low-speed device, perform EHCI reset.		
9	SUSPENDL1	When this bit is set to 1, an LPM token is generated. 0: Suspend using L2 1: Suspend using L1 (LPM)			RW	0
8	PR	Port reset This field is 0 if the PP bit is 0. 0x0: Port is not in reset. 0x1: Port is in reset. Write 0x0: Terminate the bus reset sequence. Write 0x1 when at 0x0: The bus reset sequence is started.			RW	0
7	SUS	Suspend This field is 0 if the PP bit is 0. 0x0 when PED = 0x1: Port enabled 0x1 when PED = 0x1: Port in suspend state When PED = 0x0: Port disabled			RW	0
6	FPR	Force port resume This field is 0 if the PP bit is 0. 0x0: No resume (K-state) detected/driven on port 0x1: Resume detected/driven on port			RW	0
5:4	RESERVED	Reserved			R	0
3	PEDC	Port enabled/disabled change This field is 0 if the PP bit is 0. Read 0x0: No change. Read 0x1: Port enabled/disabled status has changed. Write 0x1: Clears this bit to 0.			RW	0
2	PED	Port enabled/disabled Software cannot enable a port by setting this bit to 1. The host controller only sets this to 1 when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. This field is 0 if the PP bit is 0. 0x0: Disable 0x1: Enable			RW	0
1	CSC	Connect status change Indicates a change has occurred in the port CCS bit. This field is 0 if the PP bit is 0. Read 0x0: No change Read 0x1: Change in current connect status Write 0x1: Clears this bit to 0			RW	0
0	CCS	Current connect status This value reflects the current state of the port, and may not correspond directly to the event that caused the CSC bit to be set. This field is 0 if the PP bit is 0.			R	0

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Bits	Field Name	Description	Type	Reset
		0x0: No device is present. 0x1: Device is present on port.		

Table 23-1039. Register Call Summary for Register PORTSC_i

High-Speed Multiport USB Host Subsystem
- EHCI Register Summary: [0]
- EHCI Register Description: [1] [2] [3] [4]

Table 23-1040. INSNREG00

Address Offset	0x0000 0090		
Physical Address	0x4A06 4C90	**Instance**	EHCI
Description	Implementation-specific register 0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																UFRAME_CNT															EN

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x00000
13:1	UFRAME_CNT	1-microframe length value, to reduce simulation time. SIMULATIONS ONLY, NOT AN ACTUAL REGISTER.	RW	0x0000
0	EN	Enable of this register	RW	0

Table 23-1041. Register Call Summary for Register INSNREG00

High-Speed Multiport USB Host Subsystem
- EHCI Register Summary: [0]

Table 23-1042. INSNREG01

Address Offset	0x0000 0094		
Physical Address	0x4A06 4C94	**Instance**	EHCI
Description	Implementation-specific register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT_THRESHOLD																IN_THRESHOLD															

Bits	Field Name	Description	Type	Reset
31:16	OUT_THRESHOLD	Programmable output packet buffer threshold, in 32-bit words	RW	0x0020
15:0	IN_THRESHOLD	Programmable input packet buffer threshold, in 32-bit words	RW	0x0020

Table 23-1043. Register Call Summary for Register INSNREG01

High-Speed Multiport USB Host Subsystem
- EHCI Register Summary: [0]
- EHCI Register Description: [1]

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Table 23-1044. INSNREG02

Address Offset	0x0000 0098		
Physical Address	0x4A06 4C98	**Instance**	EHCI
Description	Implementation-specific register 2		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				BUF_DEPTH											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x00000
11:0	BUF_DEPTH	Programmable packet buffer depth, in 32-bit words	RW	0x080

Table 23-1045. Register Call Summary for Register INSNREG02

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1046. INSNREG03

Address Offset	0x0000 009C		
Physical Address	0x4A06 4C9C	**Instance**	EHCI
Description	Implementation-specific register 3		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															BRK_MEM_TRSF

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	BRK_MEM_TRSF	Break memory transfer, in conjunction with INSNREG01 0x0: Disabled 0x1: Enabled	RW	1

Table 23-1047. Register Call Summary for Register INSNREG03

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1048. INSNREG04

Address Offset	0x0000 00A0		
Physical Address	0x4A06 4CA0	**Instance**	EHCI
Description	Implementation-specific register 4		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ULPI_CLK_SUSPM			NAK_FIX_DIS	RESERVED	SHORT_PORT_ENUM	HCCPARAMS_WRE	HCSPARAMS_WRE

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved.	R	0x000000
8:6	ULPI_CLK_SUSPM	Software control for ULPI FS/LS serial mode clock suspendm feature. By default this feature is disabled. One bit per port. Example: 3'b001, the feature enabled for Port 3 and Port 2 and disabled for Port 1.	RW	0x7
5	RESERVED	Reserved.	RW	0
4	NAK_FIX_DIS	Disable NAK fix (don't touch)	RW	0
3	RESERVED	Reserved	R	0
2	SHORT_PORT_ENUM	Scale down port enumeration time (debug)	RW	0
1	HCCPARAMS_WRE	Make read-only HCCPARAMS register writable (debug)	RW	0
0	HCSPARAMS_WRE	Make read-only HCSPARAMS register writable (debug)	RW	0

Table 23-1049. Register Call Summary for Register INSNREG04

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]
- EHCI Register Description:

Table 23-1050. INSNREG05_UTMI

Address Offset	0x0000 00A4		
Physical Address	0x4A06 4CA4	**Instance**	EHCI
Description	Implementation-specific register 5. Register functionality for UTMI mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														VBUSY		VPORT				VCONTROLLOADM		VCONTROL				VSTATUS					

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	VBUSY	Read 0x0: Vendor interface is done/inactive Read 0x1: Vendor interface is busy	R	0
16:13	VPORT	Vendor interface port selection 0x1: Port 1 vendor interface selected 0x2: Port 2 vendor interface selected	RW	0x0

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Bits	Field Name	Description	Type	Reset
12	VCONTROLLOADM	UTMI VcontrolLoadM output (active-low) 0x0: Load Vcontrol value into PHY 0x1: No Action	RW	0
11:8	VCONTROL	UTMI Vcontrol output, to be loaded into the PHY	RW	0x0
7:0	VSTATUS	UTMI Vstatus input image, from PHY	R	0x00

Table 23-1051. Register Call Summary for Register INSNREG05_UTMI

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1052. INSNREG05_ULPI

Address Offset	0x0000 00A4		
Physical Address	0x4A06 4CA4	**Instance**	EHCI
Description	Implementation-specific register 5. Register functionality for ULPI mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL	RESERVED			PORTSEL				OPSEL		REGADD						EXTREGADD								RDWRDATA							

Bits	Field Name	Description	Type	Reset
31	CONTROL	Control/status of the ULPI register access Write 0x0: No effect 0x0: ULPI access done 0x1: Start ULPI access	RW	0
30:28	RESERVED		R	0x0
27:24	PORTSEL	0x1: Port 1 selected for register access 0x2: Port 2 selected for register access	RW	0x0
23:22	OPSEL	0x2: Register access is write. 0x3: Register access is read.	RW	0x0
21:16	REGADD	ULPI direct register address, for any value different than 0x2F. 0x2F: Triggers an extended address	RW	0x00
15:8	EXTREGADD	Address for extended register accesses. Don't care for direct accesses.	RW	0x00
7:0	RDWRDATA	Read/write data of (resp. read/write) register access	RW	0x00

Table 23-1053. Register Call Summary for Register INSNREG05_ULPI

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

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Table 23-1054. INSNREG06

Address Offset	0x0000 00A8		
Physical Address	0x4A06 4CA8	**Instance**	EHCI
Description	AHB error status		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERRORCAP	RESERVED																			HBURST			BEATSEXP				BEATSCOMP				

Bits	Field Name	Description	Type	Reset
31	ERRORCAP	Indicator that an AHB error was encountered and values were captured Read 0x0: No error Write 0x0: Clear pending error Write 0x1: No action Read 0x1: Error pending	RW	0
30:12	RESERVED		R	0x00000
11:9	HBURST	HBURST Value of the control phase at which the AHB error occurred	R	0x0
8:4	BEATSEXP	Number of beats expected in the burst at which the AHB error occurred. Valid values are 0 to 16.	R	0x00
3:0	BEATSCOMP	Number of successfully completed beats in the current burst before the AHB error occurred	R	0x0

Table 23-1055. Register Call Summary for Register INSNREG06

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

Table 23-1056. INSNREG07

Address Offset	0x0000 00AC		
Physical Address	0x4A06 4CAC	**Instance**	EHCI
Description	AHB master error address		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASTERERRADD																															

Bits	Field Name	Description	Type	Reset
31:0	MASTERERRADD	AHB master error address	R	0x0000 0000

Table 23-1057. Register Call Summary for Register INSNREG07

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

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Table 23-1058. INSNREG08

Address Offset	0x0000 00B0		
Physical Address	0x4A06 4CB0	**Instance**	EHCI
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NEWBITFIELD1															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	NEWBITFIELD1		RW	0x0000

Table 23-1059. Register Call Summary for Register INSNREG08

High-Speed Multiport USB Host Subsystem

- EHCI Register Summary: [0]

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23.11 Super-Speed USB OTG Subsystem

This section describes the SuperSpeed (SS) USB On-The-Go (OTG) subsystem of the device.

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23.11.1 SuperSpeed USB OTG Subsystem Overview

The SS USB controller is a USB3 OTG dual-role-device (DRD) link controller supporting the following modes:

- USB 2.0 peripheral (function controller) in full- and high-speed (12 and 480 Mbps, respectively)
- USB 2.0 host in low-, full-, and high-speed (1.5, 12, 480 Mbps, respectively), with one downstream port but multipoint capability when a hub is connected to it (split transaction support, etc.)
- USB 3.0 peripheral (function controller) in super speed (5 Gbps)
- USB 3.0 host in super speed with one downstream port but multipoint capability when a hub is connected to it

The SuperSpeed USB OTG controller supports a single USB port that uses the ULPI interface mode to connect to an off-chip transceiver (12-pin, 8-bit data SDR mode) and to a USB 2.0/3.0 bus using an embedded USB 2.0 PHY and embedded USB 3.0 RX/TX PHYs.

NOTE: The current implementation of the SuperSpeed USB OTG subsystem does not support the dynamic role switching, that is, OTG protocols HNP, SRP, and ADP.

Figure 23-237 shows the SuperSpeed USB subsystem overview.

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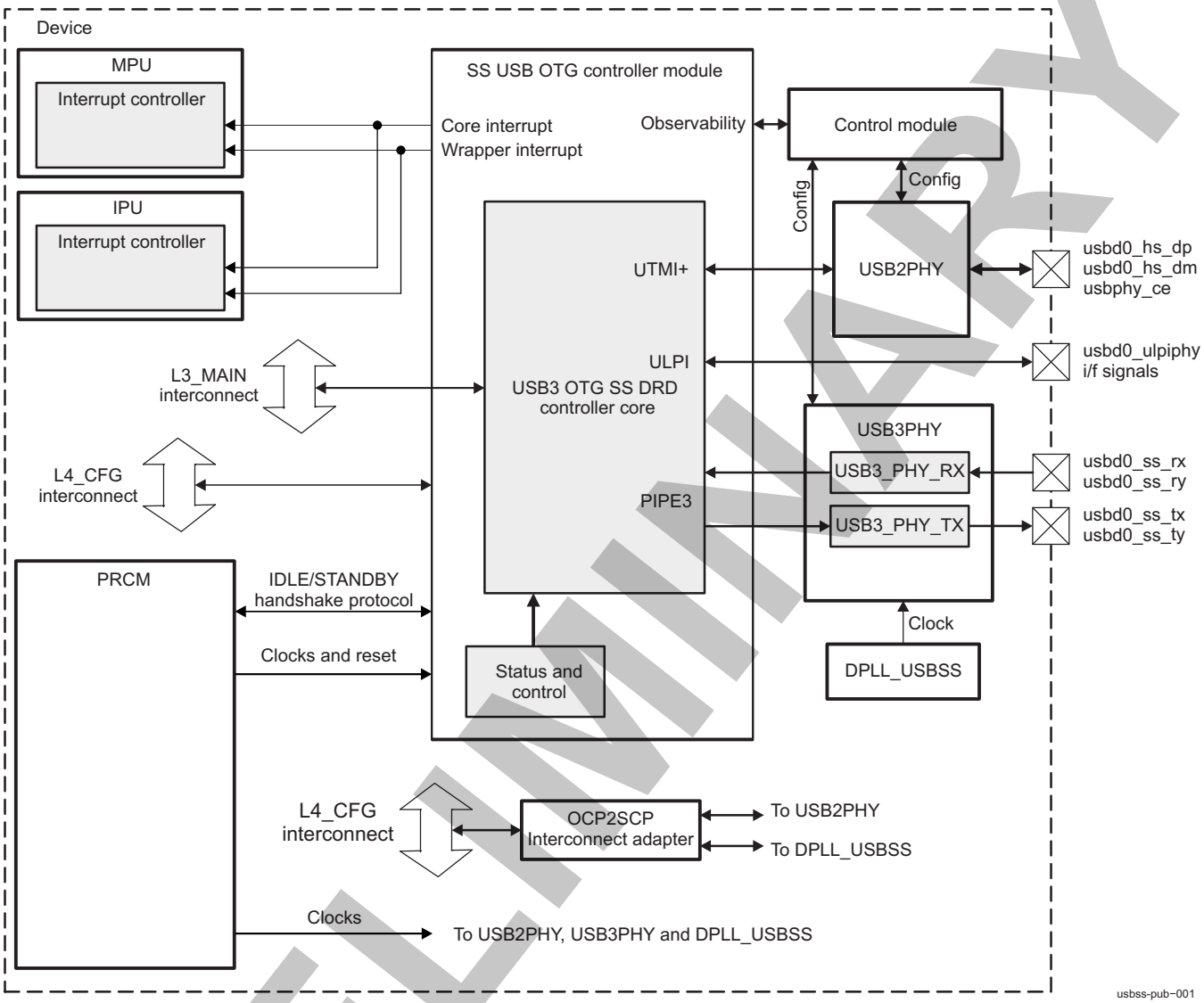
Figure 23-237. SuperSpeed USB OTG Subsystem Highlight



23.11.1.1 Main Features

The SuperSpeed USB controller features:

- Dual-role device (DRD) capability:
  - Peripheral (device role) operation in SS, high-speed (HS), full speed (FS)
  - Host role operation (single port with xHCI software API) in all speeds (SS, HS, FS, and low speed [LS])
- UTMI+ port for USB2.0 PHY interface (8 bit data @60 MHz)
- ULPI port for alternative, off-chip USB2 PHY interface (12-pin, 8-data-bit, SDR)
- PIPE port for USB3.0 SS PHY interface (32-bit data @125 MHz by default)
- Link power management (LPM)
- Logic retention for fast power transitions
- USB-HS OTG PHY (USB2PHY): contains the USB functions, drivers, receivers, and pads correct D+/D– signalling and battery charger detection (supporting dead-battery mode). Delivers a 3.3-V output signal (charger enable) to control external battery charger.

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- USB3PHY. The USB3PHY is embedded in the device and contains:
  - USB3_PHY_RX deserializer to receive data at SuperSpeed mode
  - USB3_PHY_TX serializer to transmit data at SuperSpeed mode
  - Power sequencer that contains a power control state machine, generating the sequences to power up/down the USB3_PHY_RX/USB3_PHY_TX
  - Dedicated DPLL (DPLL_USBSS)

23.11.2 SuperSpeed USB OTG Subsystem Environment

23.11.2.1 SuperSpeed USB OTG Subsystem I/O Interfaces

Figure 23-238 describes the I/O signals of the SuperSpeed USB subsystem interfaces.

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Figure 23-238. SuperSpeed USB Subsystem Environment

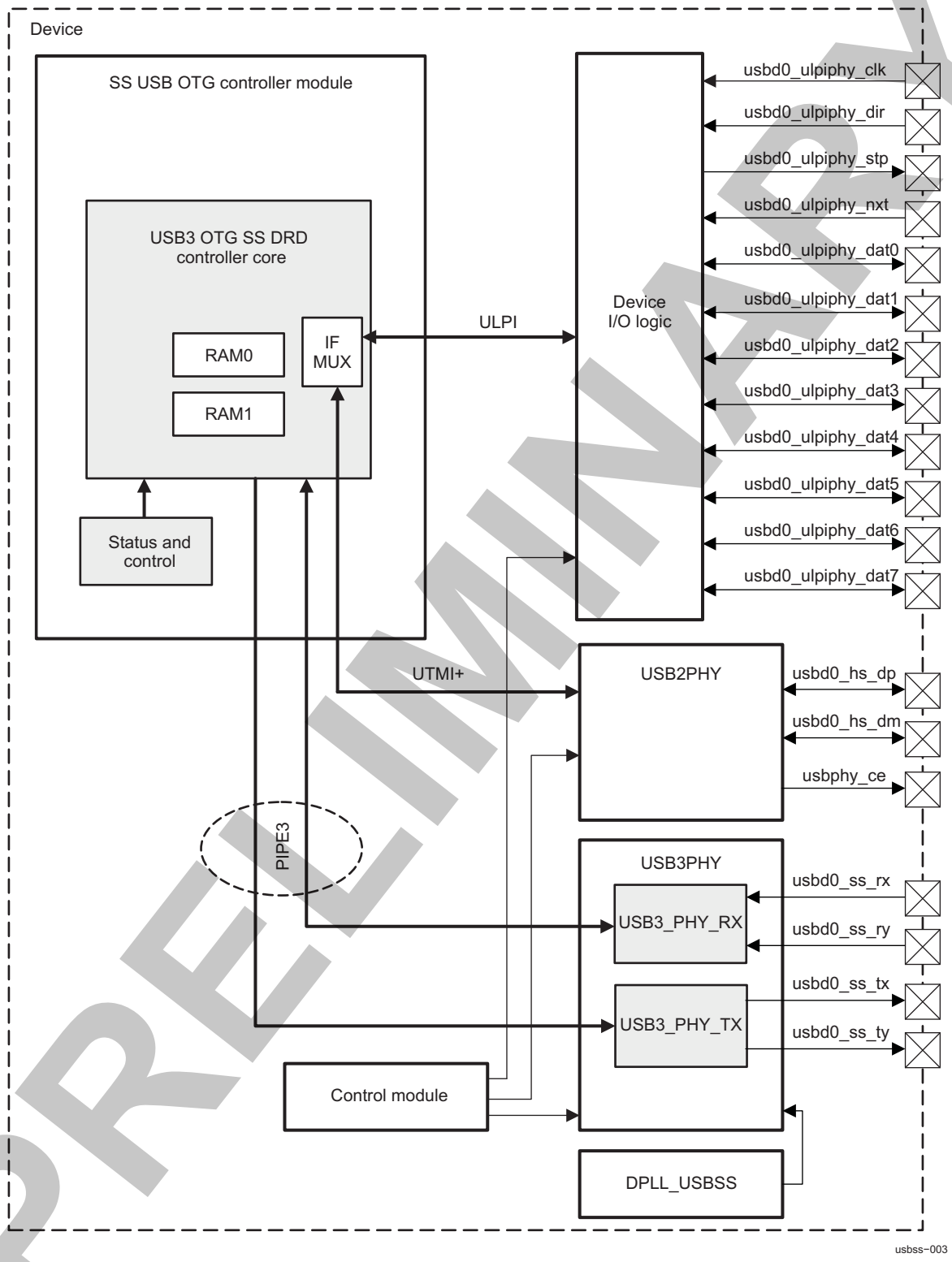

Table 23-1060 describes the I/O signals of the SuperSpeed USB subsystem interfaces shown in Figure 23-238

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Table 23-1060. Input/Output Description

Module Pin	Device-Level Signal Name	I/O[1]	Description	Reset Value
ULPI interface				
ULPI_CLK	usbd0_ulpiphy_clk	I	Clock input from external transceiver	HiZ
ULPI_DIR	usbd0_ulpiphy_dir	I	Data direction control from external transceiver	HiZ
ULPI_STP	usbd0_ulpiphy_stp	O	Output to external transceiver to stop data stream	1
ULPI_NXT	usbd0_ulpiphy_nxt	I	Next signal control from external transceiver	HiZ
ULPI_DATA0	usbd0_ulpiphy_data0	I/O	Data bit 0 to/from external transceiver	HiZ
ULPI_DATA1	usbd0_ulpiphy_data1	I/O	Data bit 1 to/from external transceiver	HiZ
ULPI_DATA2	usbd0_ulpiphy_data2	I/O	Data bit 2 to/from external transceiver	HiZ
ULPI_DATA3	usbd0_ulpiphy_data3	I/O	Data bit 3 to/from external transceiver	HiZ
ULPI_DATA4	usbd0_ulpiphy_data4	I/O	Data bit 4 to/from external transceiver	HiZ
ULPI_DATA5	usbd0_ulpiphy_data5	I/O	Data bit 5 to/from external transceiver	HiZ
ULPI_DATA6	usbd0_ulpiphy_data6	I/O	Data bit 6 to/from external transceiver	HiZ
ULPI_DATA7	usbd0_ulpiphy_data7	I/O	Data bit 7 to/from external transceiver	HiZ
USB2PHY				
CE	usbphy_ce	O	Charging enable signal	0
DP	usbd0_hs_dp	I/O	USB2 half-duplex differential pair	HiZ
DM	usbd0_hs_dm	I/O		HiZ
USB3PHY				
TX	usbd0_ss_tx	O	USB3 transmitter differential pair	HiZ
TY	usbd0_ss_ty	O		HiZ
RX	usbd0_ss_rx	I	USB3 receiver differential pair	HiZ
RY	usbd0_ss_ry	I		HiZ
USB frame sync output				
SYNC_USOF_ITP_CLK	sync_usof_itp_clk	O	4-kHz clock output, each edge locked to ITP/uSOF sync packets of SS/HS USB	0
SYNC_SOF_CLK	sync_sof_clk	O	0.5-kHz clock output, each edge locked to SOF sync packets of FS USB	0

(1) I = Input; O = Output; I/O = Bidirectional

NOTE: The path from a module pin to device pad(s) is defined at the device I/O logic level. The control module registers assign the specific function to the device pads. For more information on control module settings, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, of *Chapter 18, Control Module*.

23.11.2.2 SuperSpeed USB OTG Subsystem Application

23.11.2.2.1 USB3.0 OTG DRD Application

Figure 23-239 shows a typical application using the SuperSpeed USB subsytem. The application represents a full-featured integration and allows all of the capabilities of the controller used. The companion IC can actually be split in two, with a power IC either supplying (driver) or drawing (charger) power on VBUS, and a control IC performing the VBUS and OTG ID control functions, such as pulling, sensing, etc.

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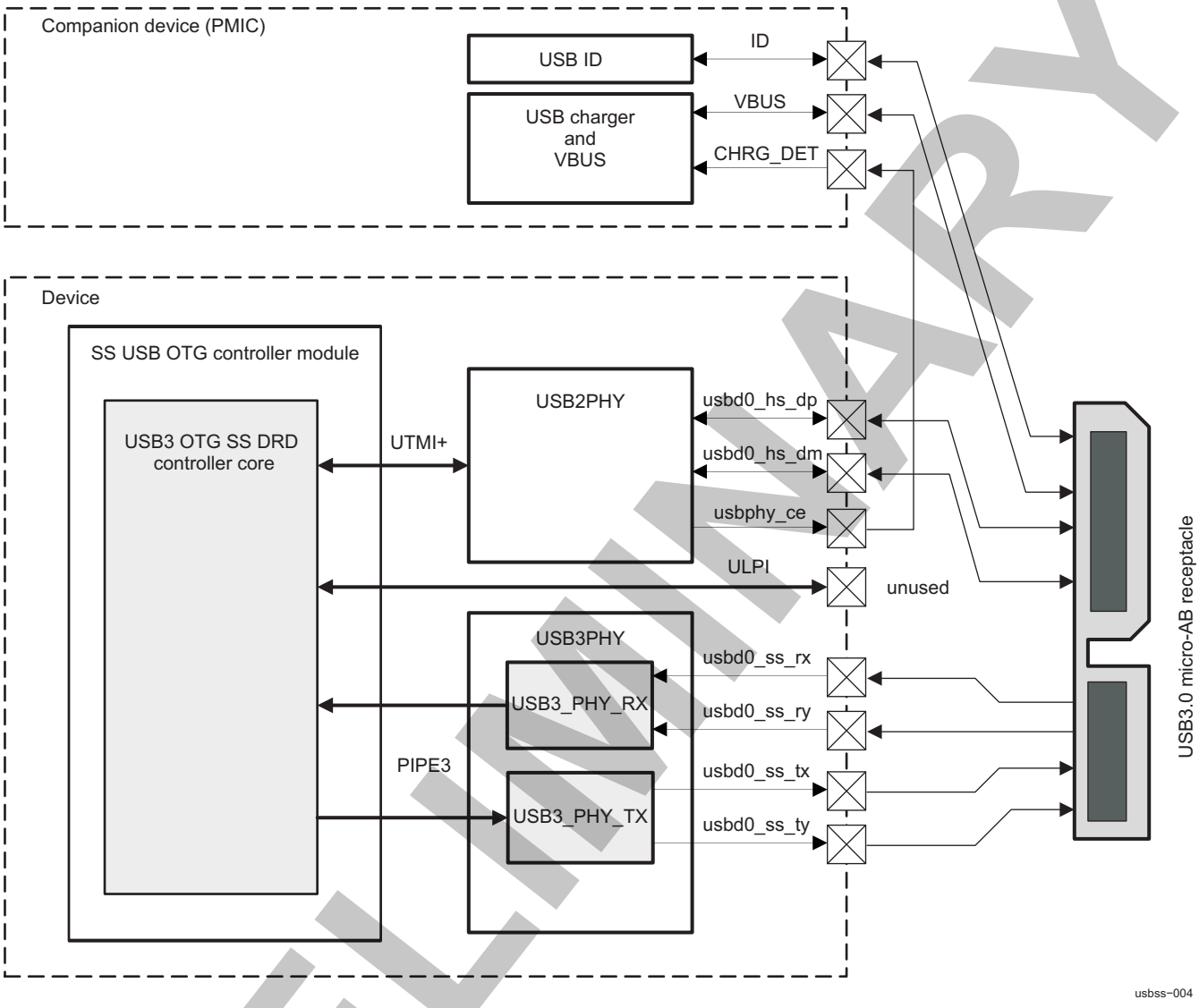
Figure 23-239. SuperSpeed USB Controller Application: USB3.0 OTG DRD



The USB3.0 micro-AB receptacle characterizes a USB3.0 OTG DRD, and allows the following attachments:

- Micro-A-type plugs, to attach to a USB peripheral/hub upstream port (or to another DRD, as host)
- Micro-B-type plugs, to attach to a USB host/hub downstream port (or to another DRD, as peripheral)
- To USB3.0 devices: The USB3.0 micro plug covers all contacts of the receptacle.
- To USB2.0 devices: The USB2.0 micro plug occupies only the wider, USB2.0 half of the receptacle. SuperSpeed signal pairs remain floating.

23.11.2.2.2 USB3.0 OTG DRD Alternative

NOTE: External ULPI PHY interface is used mostly for debug and test purposes. During normal operation, the internal USB2 PHY must be used.

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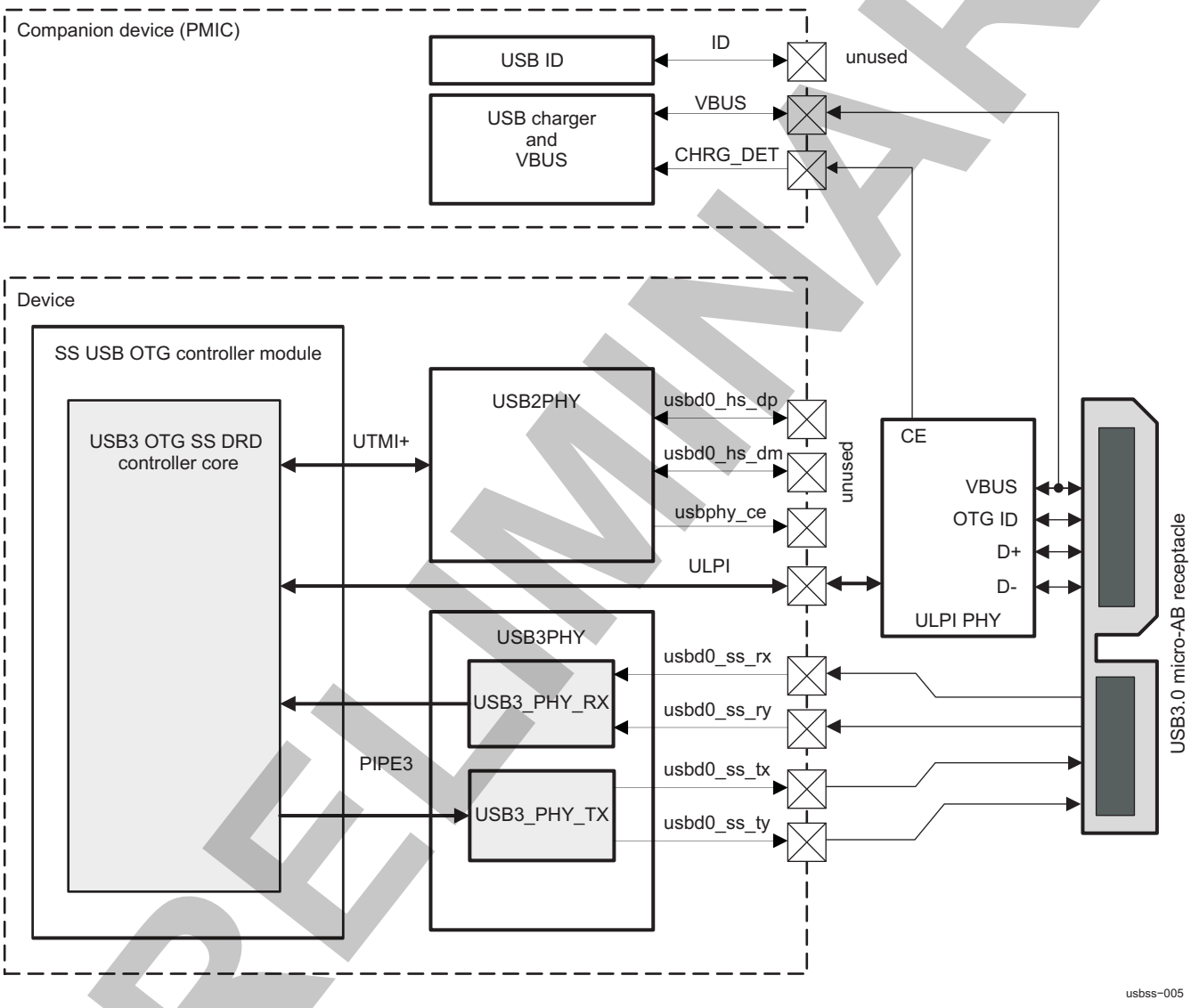
Figure 23-240 shows an alternative to Figure 23-238 (that is, a USB3.0 integration) in which an external ULPI PHY IC is used instead of the on-chip UTMI PHY (USB2PHY). Seen from outside the system, both integrations are functionally equivalent. Internally, the functions of the OTG ID and VBUS are taken over by the ULPI PHY. However, the (now optional) companion IC still can be required to draw (charger) power on VBUS or supply it with more than the ULPI PHY is capable of.

The external (ULPI) PHY interface is selected through USBOTGSS_GUSB2PHYCFG[4] ULPI_UTMI_SEL bit set to 0x1.

Figure 23-240. SuperSpeed USB Controller Application: USB3.0 OTG DRD (ULPI PHY)



23.11.2.2.3 USB2.0 OTG DRD

Figure 23-241 shows a USB2.0-only integration in which the USB3.0 capability is not available. Similarly to Figure 23-238, the companion IC can be split in two, with a power IC either supplying (driver) or drawing (charger) power on VBUS, and a control IC providing the VBUS and OTG ID control functions, such as pulling, sensing, etc.

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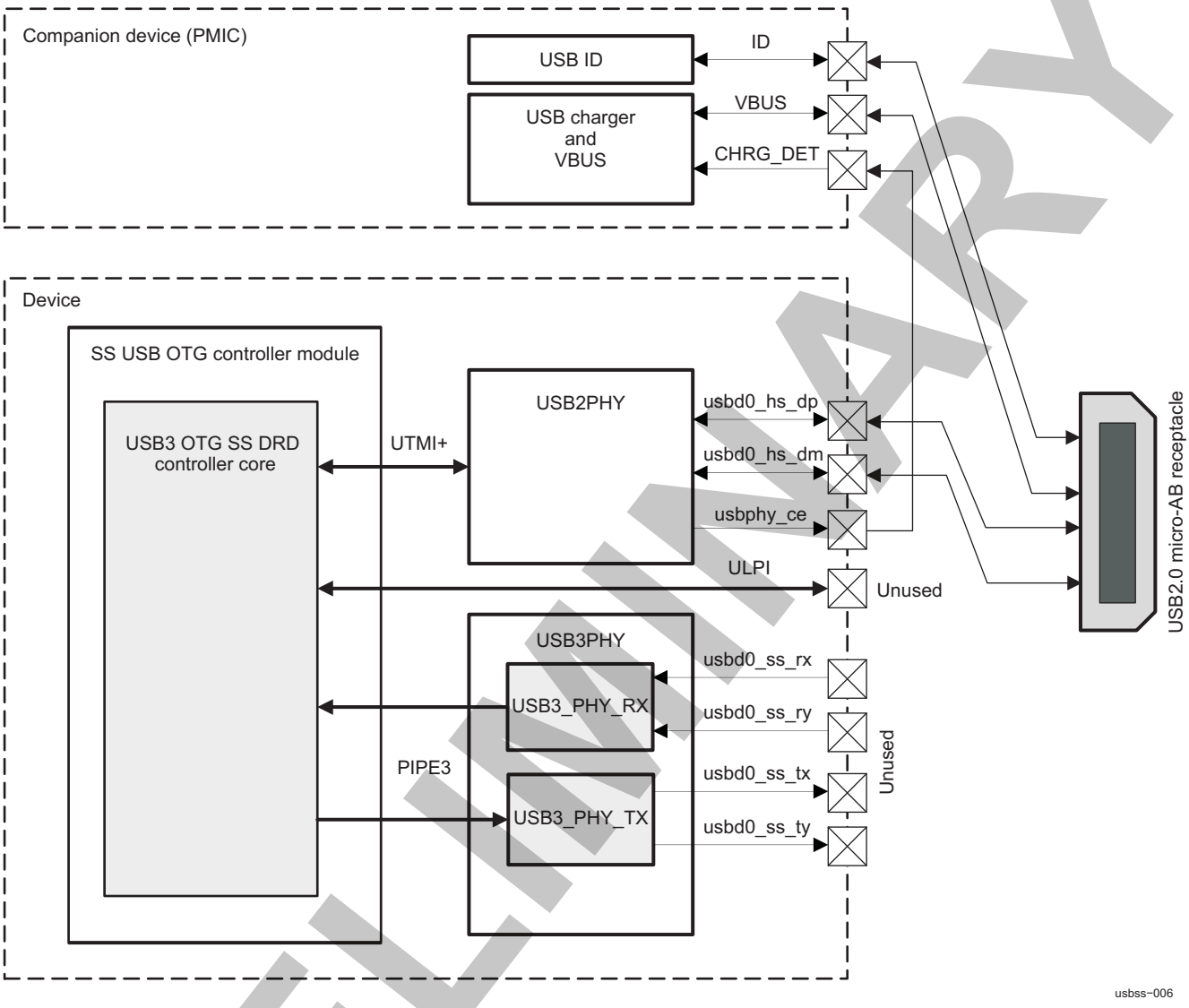
Figure 23-241. SuperSpeed USB Controller Application: USB2.0 OTG DRD



The USB2.0 micro-AB receptacle characterizes a USB2.0 OTG DRD and accepts the following:

- Micro-A-type plugs, which attach to a USB peripheral/hub upstream port (or another DRD, as host)
- Micro-B-type plugs, which attach to a USB host/hub downstream port (or another DRD, as peripheral)
- USB2.0 devices only: The USB2.0 micro plug covers all contacts of the receptacle.
- Not USB3.0 devices: The USB3.0 micro plug is incompatible and the SuperSpeed signal pairs of the cable remain floating.

23.11.2.2.4 USB2.0 OTG DRD Alternative

NOTE: External ULPI PHY interface is used mostly for debug and test purposes. During normal operation, the internal USB2 PHY must be used.

Figure 23-242 shows an alternative to Figure 23-241 (that is, a USB2.0-only integration) in which an external ULPI PHY IC is used instead of the on-chip UTMI USB2PHY. Seen from outside the system, both integrations are functionally equivalent. Internally, the functions of OTG ID and VBUS are taken over by the ULPI PHY. However, the (now optional) companion IC can still be required to draw (charger) power on VBUS or supply it with more than the ULPI PHY is capable of.

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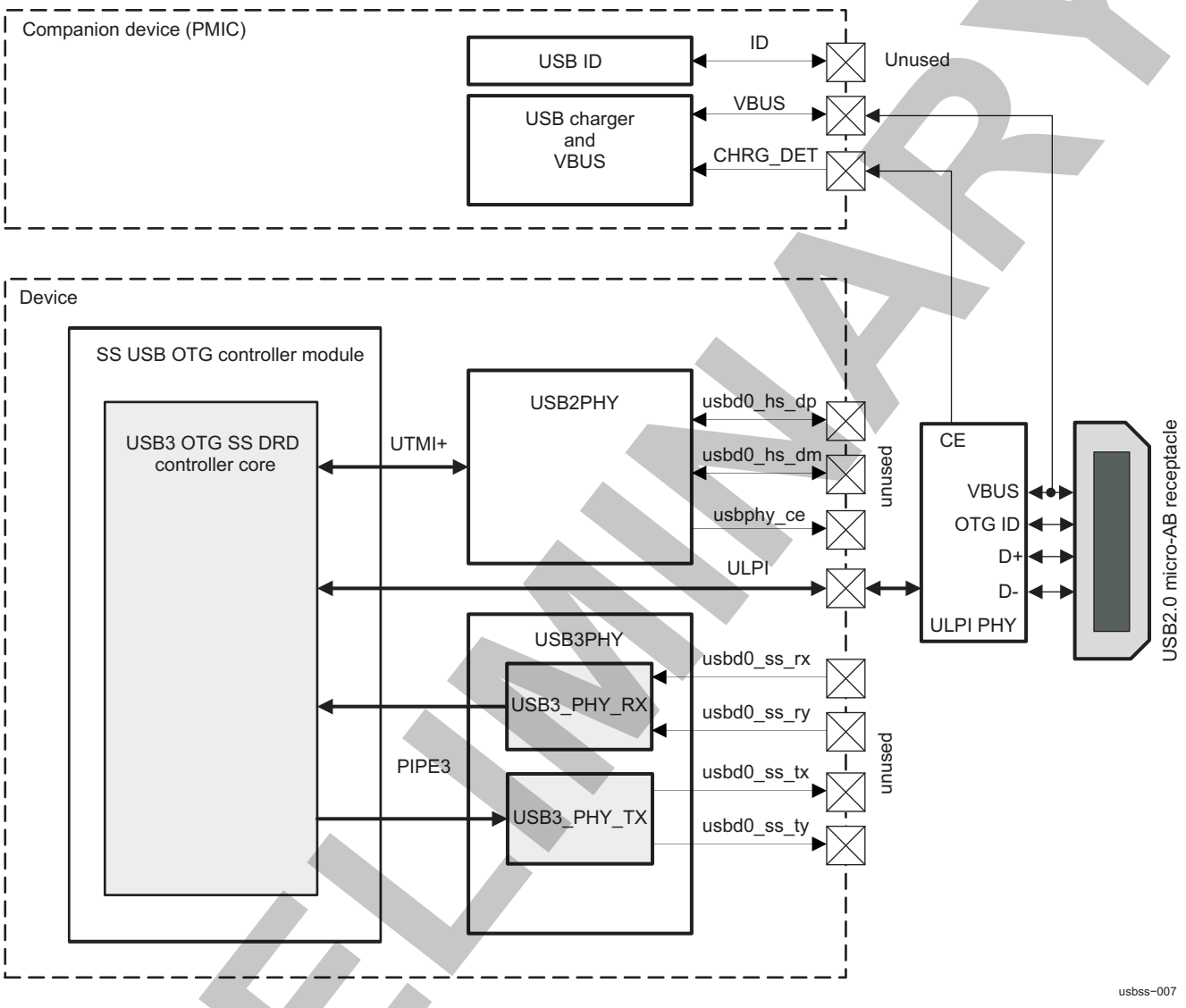
The external (ULPI) PHY interface is selected through USBOTGSS_GUSB2PHYCFG[4] ULPI_UTMI_SEL bit set to 0x1.

Figure 23-242. SuperSpeed USB Controller Application: USB2.0 OTG DRD (ULPI PHY)



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23.11.3 SuperSpeed USB OTG Subsystem Integration

The L3 (master) interconnect generates data traffic within the device. The L4 (slave) interconnect is a configuration port for register setting.

Figure 23-243 shows the SuperSpeed USB subsystem integration in the device.

Figure 23-243. SuperSpeed USB Subsystem Integration

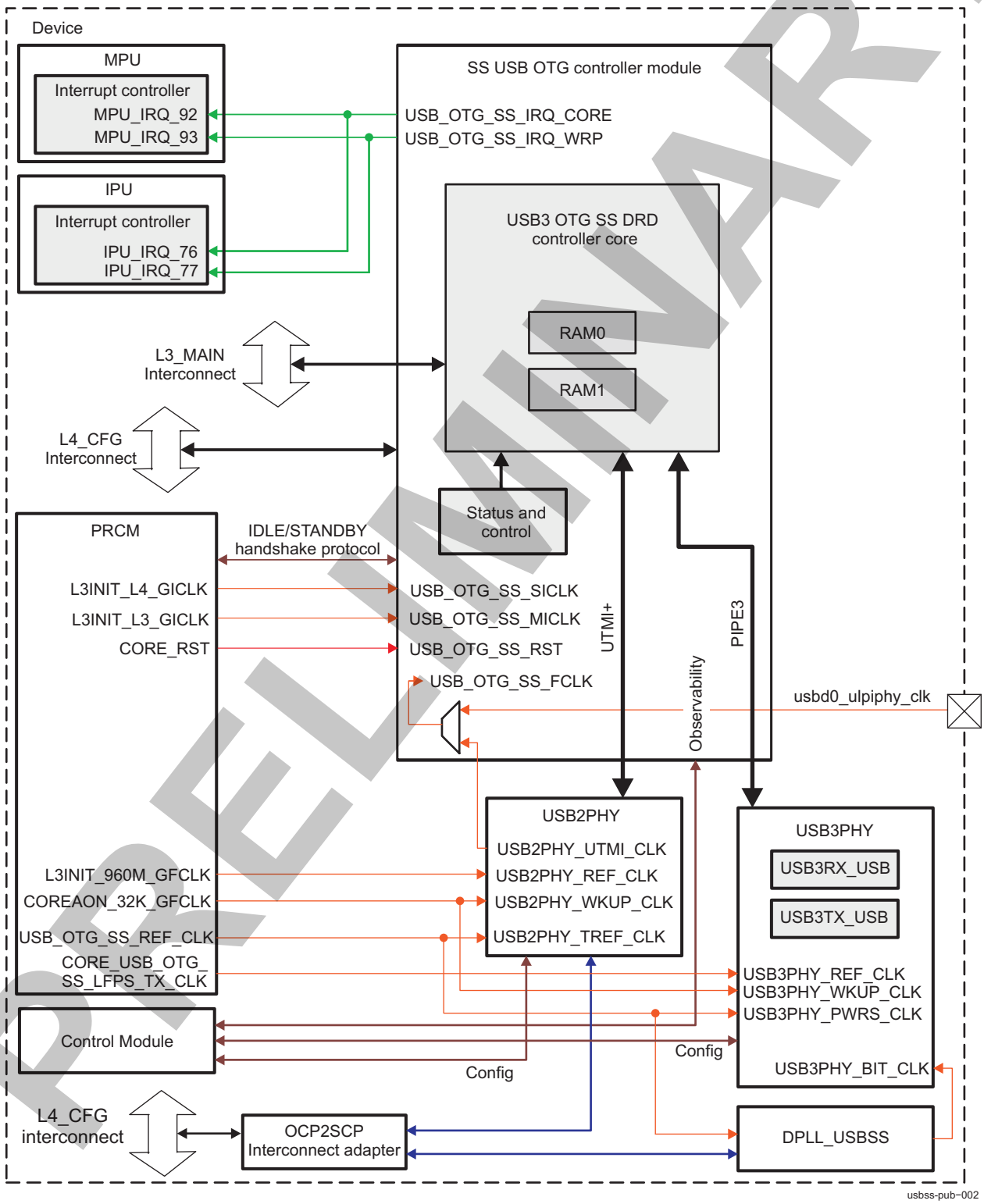

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Table 23-1061 through Table 23-1063 summarize the integration of the module in the device.

Table 23-1061. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
USB_OTG_SS	PD_L3INIT	L3_MAIN L4_CFG
USB2PHY	PD_L3INIT	L4_CFG
USB3PHY	PD_L3INIT	L4_CFG

Table 23-1062 lists the clocks provided to the SuperSpeed USB subsystem.

Table 23-1062. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
USB_OTG_SS	USB_OTG_SS_FCLK	OTG_60M_FCLK	USB2PHY or ULPI PHY	60-MHz UTMI/ULPI clock
	USB_OTG_SS_SICLK	L3INIT_L4_GICLK	PRCM	L4 interconnect enable signal for the slave interface on L4 Section 3.6.3.2, *CM Clock Source* in Section 3.1.1, *Power, Reset and Clock Management*
	USB_OTG_SS_MICLK	L3INIT_L3_GICLK	PRCM	L3 interconnect clock, for the L3 master port interface Section 3.6.10, *CD_L3_INIT Clock Domain* in Section 3.1.1, *Power, Reset and Clock Management*.
USB2PHY	USB2PHY_REF_CLK	L3INIT_960M_GFCLK	PRCM/DPLL_USB	Functional REF 960-MHz clock (from the DPLL_USB, PRCM controlled)
	USB2PHY_WKUP_CLK	COREAON_32K_GFCLK	PRCM	Wakeup 32-kHz functional clock
	USB2PHY_TREF_CLK	USB_OTG_SS_REF_CLK	PRCM	Fixed-frequency TREF functional clock
USB3PHY	DPLL_USBSS_REF_CLK	USB_OTG_SS_REF_CLK	PRCM	Functional DPLL REF clock derived from SYS_CLK
	USB3PHY_LFPS_CLK	CORE_USB_OTG_SS_LFPS_TX_CLK	PRCM	Fixed-frequency REF functional clock
	USB3PHY_PWRS_CLK	USB_OTG_SS_REF_CLK	PRCM	Fixed-frequency power sequencer functional clock
	USB3PHY_WKUP_CLK	COREAON_32K_GFCLK	PRCM	Wakeup and debounce 32-kHz functional clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
USB_OTG_SS	USB_OTG_SS_RST	CORE_RST	PRCM	USB_OTG_SS controller hardware reset

Table 23-1063 lists the interrupt lines that are driven out from the SuperSpeed USB controller.

Table 23-1063. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
USB_OTG_SS	USB_OTG_SS_IRQ_CORE	MPU_IRQ_92	MPU INTC	USB_OTG_SS main (core) interrupt request
		IPU_IRQ_76	IPU INTC	

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Table 23-1063. Hardware Requests (continued)

USB_OTG_SS_IRQ_WRP	MPU_IRQ_93	MPU INTC	USB_OTG_SS wrapper interrupt request
	IPU_IRQ_77	IPU_INTC	

23.11.4 SuperSpeed USB OTG Controller Functional Description

23.11.4.1 Reset

23.11.4.1.1 Software Reset

Software can perform a reset on SS USB OTG controller by following the sequence:

1. Write 1 to USBOTGSS_FLADJ[31] CORE_SW_RESET to assert the software reset to the core. This bit is not self-clearing. All core registers will be cleared to their default value. Wrapper registers will not be affected.
2. Write 0 to USBOTGSS_FLADJ[31] CORE_SW_RESET to deassert the software reset of the core.
3. Poll register field USBOTGSS_USBSTS[11] CNR until controller is ready (=0), before accessing the other core registers (the reset of the RAM-stored core registers can take several cycles to complete, see Section 23.11.4.1.2, *Active RAM Reset*).
4. USBOTGSS_WRAPPER registers can be reset by writing 1 to USBOTGSS_SYSCONFIG[17] WRAPRESET. Wrapper reset is completed when this bit is cleared back to 0 by hardware.

23.11.4.1.2 Active RAM Reset

The lower part of RAM0 contains some register values and descriptor cache (from RAM0 address 0 to DWC_USB3_DCACHE_DEPTH_INFO-1) that must be initialized. For that purpose, the core automatically writes all-0 words to a section of RAM0 immediateley after coming out of reset. This sequential process takes time (over 1000 interconnect clock cycles), during which functional read and write to the RAM-mapped registers are stalled. To avoid the stalls, the xHCI status bit USBOTGSS_USBSTS[11] CNR (controller not ready) can be polled until cleared (= 0).

Although this is a standard USB-host mode status bit, the method also works to access RAM-mapped registers of the USB-device.

23.11.4.2 Interrupts

Two interrupt lines come out from the USB controller module:

- USB_OTG_SS_IRQ_CORE: for SS USB OTG controller events
- USB_OTG_SS_IRQ_WRP: for SS USB OTG wrapper events

23.11.4.2.1 Core Events

The main interrupt line carries all events from the DRD core related to the USB device and USB host (xHCI). Those high-frequency events are associated with actual USB traffic. Since core IRQ is the only source event for that interrupt, and the status bit (USBOTGSS_IRQSTATUS_0[0] COREIRQ_ST) is self-clearing, the software does not actually need to access USBOTGSS_IRQSTATUS_0. Prior to the assertion of IRQ line USB_OTG_SS_IRQ_CORE, the core DMA (master) accesses main memory to write IRQ events to the IRQ event queue. If the master is in standby mode, an interrupt event brings it out of standby, as explained in Section 23.11.4.3.2, *System Power Management*.

For a description of core interrupts, see Synopsys® *Designware Cores SuperSpeed USB 3.0 Controller Databook*.

23.11.4.2.2 Wrapper Events

USB_OTG_SS_IRQ_WRP interrupt line is triggered by:

- VBUS and OTG ID controls changes in the mailbox mechanism (when UTMI is used, as opposed to

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ULPI)

- OTG events from the core
- The DMA (master's) port automatic reenabling, to allow new read/write accesses.

Table 23-1064 lists the event flags, and their mask, that can cause module interrupts.

Table 23-1064. SS USB OTG Wrapper Events

Event Flag	Event Mask	Description
USBOTGSS_IRQSTATUS_1[17] DMADISABLECLR	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[17] DMADISABLECLR_EN	DMA-disable self-clear IRQ. USBOTGSS_SYSCONFIG[17] DMADISABLE hardware-cleared (to 0) because of DMA access. Not triggered by a software clear.
USBOTGSS_IRQSTATUS_1[16] OEVT	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[16] OEVT_EN	OTG event in controller. The event is in status register USBOTGSS_OEVT.
USBOTGSS_IRQSTATUS_1[13] DRVVBUS_RISE	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[13] DRVVBUS_RISE_EN	Drive VBUS control rise
USBOTGSS_IRQSTATUS_1[12] CHRGVBUS_RISE	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[12] CHRGVBUS_RISE_EN	Charge VBUS control rise
USBOTGSS_IRQSTATUS_1[11] DISCHRGVBUS_RISE	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[11] DISCHRGVBUS_RISE_EN	Discharge VBUS control rise
USBOTGSS_IRQSTATUS_1[8] IDPULLUP_RISE	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[8] IDPULLUP_RISE_EN	ID pullup control rise
USBOTGSS_IRQSTATUS_1[5] DRVVBUS_FALL	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[5] DRVVBUS_FALL_EN	Drive VBUS control fall
USBOTGSS_IRQSTATUS_1[4] CHRGVBUS_FALL	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[4] CHRGVBUS_FALL_EN	Charge VBUS control fall
USBOTGSS_IRQSTATUS_1[3] DISCHRGVBUS_FALL	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[3] DISCHRGVBUS_FALL_EN	Discharge VBUS control fall
USBOTGSS_IRQSTATUS_1[0] IDPULLUP_FALL	USBOTGSS_IRQENABLE_SET_1/ USBOTGSS_IRQENABLE_CLR_1[0] IDPULLUP_FALL_EN	ID pullup control fall

23.11.4.3 Power Management

23.11.4.3.1 Overview

The high-speed USB controller has both master (initiator) and slave (target) interfaces:

- As an initiator, the high-speed USB OTG controller implements the standby handshake protocol to inform the PRCM module when it enters standby mode and does not generate traffic on the interconnect.
- As a target, the high-speed USB OTG controller implements the IDLE handshake protocol to allow the PRCM module requiring it to enter idle mode.

23.11.4.3.2 System Power Management

The standard idle request/acknowledge handshake is associated with the interconnect slave port. The default idle mode is smart-idle and is used for most operations.

Table 23-1065 describes the high-speed USB idle mode settings. For more information, see Section 3.1.1, *Power, Reset, and Clock Management*.

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Table 23-1065. USBOTGSS Controller Idle Mode Settings

USBOTGSS_SYSCONFIG[3:2] IDLEMODE Value	Selected Mode	Description
0x0	Force-idle	The HSUSBOTG host controller acknowledges unconditionally the idle request from the PRCM, regardless of its internal operations.
0x1	No-idle	The HSUSBOTG host controller never acknowledges any idle request from the PRCM.
0x2	Smart-idle	The HSUSBOTG host controller acknowledges the idle request, basing its decision on its internal activity. Namely, the acknowledge signal is asserted only when all pending transactions and IRQ requests are treated.
0x3	Smart-idle wakeup	The HSUSBOTG host controller enters smart mode with wakeup enabled. Controller may generate wakeup events when in idle state.

The standby/wait handshake is associated with the interconnect master port. The DMA is under direct software control. The software driver ensures that the master is shut down correctly when shutdown is required.

The default standby mode is smart-standby. USBOTGSS_SYSCONFIG[5:4] STANDBYMODE is 0x2 after reset and is used for most operations. Because there is no asynchronous wakeup source for the master, smart-standby and smart-standby/wakeup are functionally equivalent.

The master interface is controlled by a semi-automatic disable bit mapped in USBOTGSS_SYSCONFIG[16] DMADISABLE. To use this bit, the standby mode must be a smart-standby mode as follows:

- When the DMA must perform read/write accesses, the following sequence takes place entirely in hardware: The disable bit is cleared (USBOTGSS_SYSCONFIG[16] DMADISABLE = 0); and the controller comes out of standby (mstandby = 0) and waits for the PRCM handshake (mwait = 0) before the access can occur.
- When the DMA must stop for power management, software must place USB operation (transfer request block [TRB] processing) on hold and set the USBOTGSS_SYSCONFIG[16] DMADISABLE bit back to 1. This places the controller in standby (mstandby = 1).
- Core interrupts on the USB_OTG_SS_IRQ_CORE line must remain enabled even during low-power periods. The DMA can therefore write new events to the memory-mapped interrupt event queue at any time and clear the DMADISABLE bit to 0. For the software driver to keep track of DMADISABLE, the hardware clearing of DMADISABLE triggers another interrupt, USBOTGSS_IRQSTATUS_1[17] DMADISABLECLR.

To keep track of the DMADISABLE value, the system software is expected to have a single piece of code managing:

- The clearing to 0 of DMADISABLE through the DMADISABLECLR interrupt event
- The setting to 1 of DMADISABLE, by direct software write.

NOTE: This operation might require to be repeated, if the transition to idle is interrupted by a DMA access on the master.

NOTE:

- The aforementioned procedure is guaranteed only in smart-standby modes. In force-standby and no-standby modes, the requirements of the internal DMA and the DMADISABLE setting are overridden in the generation of mstandby to PRCM.
- The USBOTGSS_SYSCONFIG[16] DMADISABLE can also be cleared (written to 0) by software at any time, but this is redundant with the hardware's action and therefore must not used under normal circumstances.

Table 23-1066 describes the high-speed USB standby mode settings.

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Table 23-1066. USBOTGSS Controller Standby Mode Settings

USBOTGSS_SYSCONFIG[5:4] STANDBYMODE Value	Selected Mode	Description
0x0	Force-standby	The USBOTGSS controller enters standby mode unconditionally.
0x1	No-standby	The USBOTGSS controller never enters standby mode.
0x2	Smart-standby	The USBOTGSS controller is ready to enter standby mode when there is no more activity on the USB master interface of the interconnect.
0x3	Smart-standby wakeup	Equivalent to smart-standby

23.11.4.4 Software API Interface

23.11.4.4.1 xHCI USB Host Software API

The eXtensible Host Controller Interface for USB (see *eXtensible Host Controller Interface for USB (xHCI) revision 1.0 with errata (errata files 1.7)*) is a standarsized interface between a USB host controller (HC) and system software (HCD, for Host Controller Driver), based on a dedicated DMA (implemented over the master interface) and a standard control and status register set (mapped in the slave address space). The HC and HCD communicate through interrupts, memory-mapped registers and data structures mapped in system memory.

The xHCI software API is used to control the DRD:

- When in USB host mode (aka OTG A-host, OTG B-host).
- When the DRD is in USB device mode (aka peripheral, OTG A-peripheral, OTG B-peripheral, function), the xHCI interface is unused.
- xHCI does not control OTG functionality (even when in OTG-host mode) .
- additionally, some implementation-specific configuration are required (in non-xHCI so called global registers) before xHCI operation proper can start.

xHCI controls all USB speeds of the host mode, that is, Super-Speed (through the USB3PHY) but also High-, Full-, and Low- speed (through the HS/FS/LS USB2PHY or ULPI PHY). xHCI replaces and supersedes all previous host HCIs (HS-only EHCI, FS/LS OHCI and UHCI), and is therefore not backwards compatible with any of them.

The xHCI standard supports a number of options (so called capabilities) and configurations (port count), all of which are self-described in the controller's memory-mapped register. The software driver must read the options and act accordingly. The main characteristics of the controller are:

- USBOTGSS_HCSPARAMS1[31:24] MAXPORTS = 2 xHCI ports (this corresponds to a single USB2 plus USB3 physical port)
  - USBOTGSS_SUPTPRT2_DW2[15:8] CPC = 1: one xHCI USB2-capable port (HS/FS/LS)
  - USBOTGSS_SUPTPRT2_DW2[7:0] CPO = 1: USB2-capable port is xHCI port 1
  - USBOTGSS_SUPTPRT3_DW2[15:8] CPC = 1: one USB3-capable port (super-speed)
  - USBOTGSS_SUPTPRT3_DW2[7:0] CPO = 2: USB3-capable port is xHCI port 2
- USBOTGSS_HCSPARAMS1[18:8] MAXINTRS = 1: One interrupter (IRQ line)

The current implementation is configured by default for xHCI version 1.0 mode. A legacy mode is also available, which implements xHCI version 0.96 (*eXtensible Host Controller Interface for USB (xHCI) revision 0.96*).

- Default mode: xHCI 1.0 (USBOTGSS_CAPLENGTH[31:16] HCIVERSION = 0x0100).
- Legacy mode: xHCI 0.96 (HCIVERSION = 0x0096)

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NOTE: The following procedure must be used to switch the xHCI mode to the legacy version (xHCI 0.96):

1. Write 1 to USBOTGSS_FLADJ[31] CORE_SW_RESET to assert the software reset to the core. This bit is not self-clearing. All core registers will be cleared to their default value. Wrapper registers will not be affected.
2. Write 0 to USBOTGSS_FLADJ[29] XHCI_REVISION to select xHCI 0.96 (or to 1 to go back to xHCI 1.0 mode)
3. Write 0 to USBOTGSS_FLADJ[31] CORE_SW_RESET to deassert the software reset of the core.
4. Poll xHCI register field USBOTGSS_USBSTS[11] CNR until controller is ready (=0), before accessing the other core registers (the reset of the RAM-stored core registers can take several cycles to complete).

The host has the same extended capabilities regardless of the xHCI version, as described in the extended capability registers (Section 23.11.4.14.2, *xHCI Host Mapping*), as per the xHCI standard:

- Legacy support (not related to xHCI version)
- USB2.0 protocol support
- USB3.0 protocol support.

23.11.4.4.2 xHCI USB Device Software API

The device software API is used to control the DRD when in device mode (aka peripheral, OTG A-peripheral, OTG B-peripheral, function). The API is not standardized. It reuses some of the xHCI features, by using descriptors mapped in main memory, but relies more on register accesses.

The device software API controls all USB speeds of the device mode, that is, Super-Speed (through the SS USB3PHY) but also high and full speed (on the HS/FS/LS USB2PHY).

When the DRD is in USB host mode (aka OTG A-host, OTG B-host), the device API is unused.

23.11.4.4.3 OTG Control Software API

NOTE: The current implementation of the SuperSpeed USB OTG subsystem does not support the dynamic role switching, that is, OTG protocols HNP, SRP, and ADP.

23.11.4.5 UTMI+ USB2 HS/FS/LS PHY Interface

The USB Transceiver Macrocell Interface (UTMI+) is the de-facto standard interface to an on-chip HS/FS/LS PHY attached to the bidirectional D+/D- twisted pair. The default mode is 8-bit (datawidth) 60 MHz UTMI. Even though 16-bit, 30 MHz is also available through software reconfiguration, the lower clock frequency brings higher latencies in the protocol FSM and in cross-domain resynchronizations, which can cause maximum USB turnaround times to be exceeded, depending on the PHY characteristics: 16-bit mode must not be preferred without a good justification.

Activity on UTMI+ and ULPI is mutually exclusive. When the on-chip UTMI PHY is used, ULPI interface typically is not utilized.

23.11.4.5.1 Mailbox VBUS/ID Management

The UTMI+ sideband signals to manage VBUS and OTG ID lines can be routed to a mailbox logic. See also Figure 23-244,*SuperSpeed USB Subsystem Operation Diagram* for an illustration of the process :

- Any change on an OTG control output (drive, charge or discharge VBUS, pull up ID: utmi_drvvbus, utmi_chrgvbus, utmi_dischrgvbus, utmi_idpullup outputs respectively) trigger an interrupt. The software must read the new output value from USBOTGSS_UTMI_OTG_CTRL and transfer it to the companion device (PMIC).
- In the other direction, any status change in the companion (VBUS valid, A/B session valid, session end, ID dig: utmi_vbuvalid, utmi_avalid, utmi_bvalid, utmi_sessend, utmi_iddig inputs, respectively) is expected to trigger an interrupt , and the software to write the new status to the controller's OTG status

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mailbox (USBOTGSS_UTMI_OTG_STATUS), from where it will enter the controller's inputs.

- Note that ADP (which also involves VBUS) is expected to be handled directly through the core's API, with no mailbox required and no associated UTMI+ signal.

The PIPE powerpresent is the VBUS status used in USB3 mode. It monitors the same VBUS line as the USB2 mode, with the following relationship.

- In host mode, USB3 powerpresent = USB2 VBUS valid (that is, the VBUS drive by the local host is sufficient for remote devices / hubs to start)
- In device mode, USB3 powerpresent = USB2 B-Session valid (that is, VBUS provided by remote host is sufficient to start operation)

Because PIPE powerpresent has a different meaning in host and in device mode, and because of the redundancy with the UTMI signals, the controller ORes together the appropriate PIPE and UTMI inputs to create its internal VBUS status. For that reason, it is recommended to leave field USBOTGSS_UTMI_OTG_STATUS[9] POWERPRESENT at its default value (=0), and only to fill in the USB2 VBUS status fields in the same register.

23.11.4.5.2 UTMI Power Management for LPM

To the standard utmi_suspendm output used in "plain" USB, the current controller adds two non-standard outputs for the Link Power Management extension (see *USB 2.0 Link Power Management (LPM) Addendum*): utmi_l1_suspend_n and utmi_l1_sleep_n.

LPM relabels the two USB power states of plain USB as L0 (active) and L2 (suspended), and introduces third, intermediate state L1 (sleep). In L1, resume latencies are shorter than in L2, and are configurable by the host through the HIRD parameter (Host Initiated Resume Duration). The USB device will typically attempt to go to the lowest-power mode compatible with the HIRD, that is, which can be exited in time to respect the HIRD. This includes the potential suspension of the UTMI interface.

The state referred to as "idle" below is the state where all clocks in the module can be stopped, in order to perform power management operations (isolation, voltage scaling, retention, power gating, etc.), and is characterized by output sidleack = 2'b11 (idle).

As explained in Table 23-1067, *LPM Power Management On UTMI+*, each of the three UTMI signals is asserted (=0) when entering a specific low-power mode:

- utmi_suspendm: asserted (=0) when the UTMI clock needs to be stopped, potentially to put the controller in idle:
  - when entering L2/suspend ("plain" suspend) or
  - when entering L1/sleep + the HIRD is high enough.
- utmi_l1_suspend_n: asserted (=0) when entering L1/sleep + HIRD value is high enough to suspend.
- utmi_l1_sleep_n: asserted (=0) when entering L1/sleep + HIRD value is too low to suspend, that is, the UTMI clock cannot be stopped and the controller cannot go to idle.

Table 23-1067, *LPM Power Management On UTMI+*shows the value of each output depending on the mode. All three signals are active-low.

Table 23-1067. LPM Power Management On UTMI+

Link state	L0 (Active)	L1 (Sleep)	L1 (Sleep), Suspended	L2 (Suspend)	Idle = Reset = Isolation
utmi_suspendm	1	1	0	0	0
utmi_l1_suspend_n	1	1	0	1	0
utmi_l1_sleep_n	1	0	1	1	1

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NOTE:

- Following the assertion (=0) of utmi_suspendm, the UTMI clock is stopped by the PHY and the controller may go to idle. When in idle, the controller forces both utmi_suspendm and utmi_l1_suspend_n to 0 (active). In other words, the PHY will see the same input values, whether in L2/suspend or in "suspended L1/sleep" receive the same input is expected to remember which mode it must be in, by following the signal that is asserted first.
- As a consequence of the above, the controller blocks the deassertion (to 1) of utmi_suspendm and utmi_l1_suspend_n caused by for example a UTMI linestate change. The goal of that is to delay the restart of the UTMI clock until the controller is out of idle and ready to resume activity.

23.11.4.6 Operation Theory

This section provides an overview of the USB_OTG_SS controller basic operation.

For information about the complete programming sequence, see *Designware Cores SuperSpeed USB 3.0 Controller Databook*.

Figure 23-244 shows the operation of the complete subsystem: The USB_OTG_SS controller together with a USB2.0 PHY (HS/FS/LS-capable) and USB3.0 PHY (SS-capable); the MPU subsystem running software and connected to the main memory; and a companion IC (TWL6035) managing the VBUS and OTG ID.

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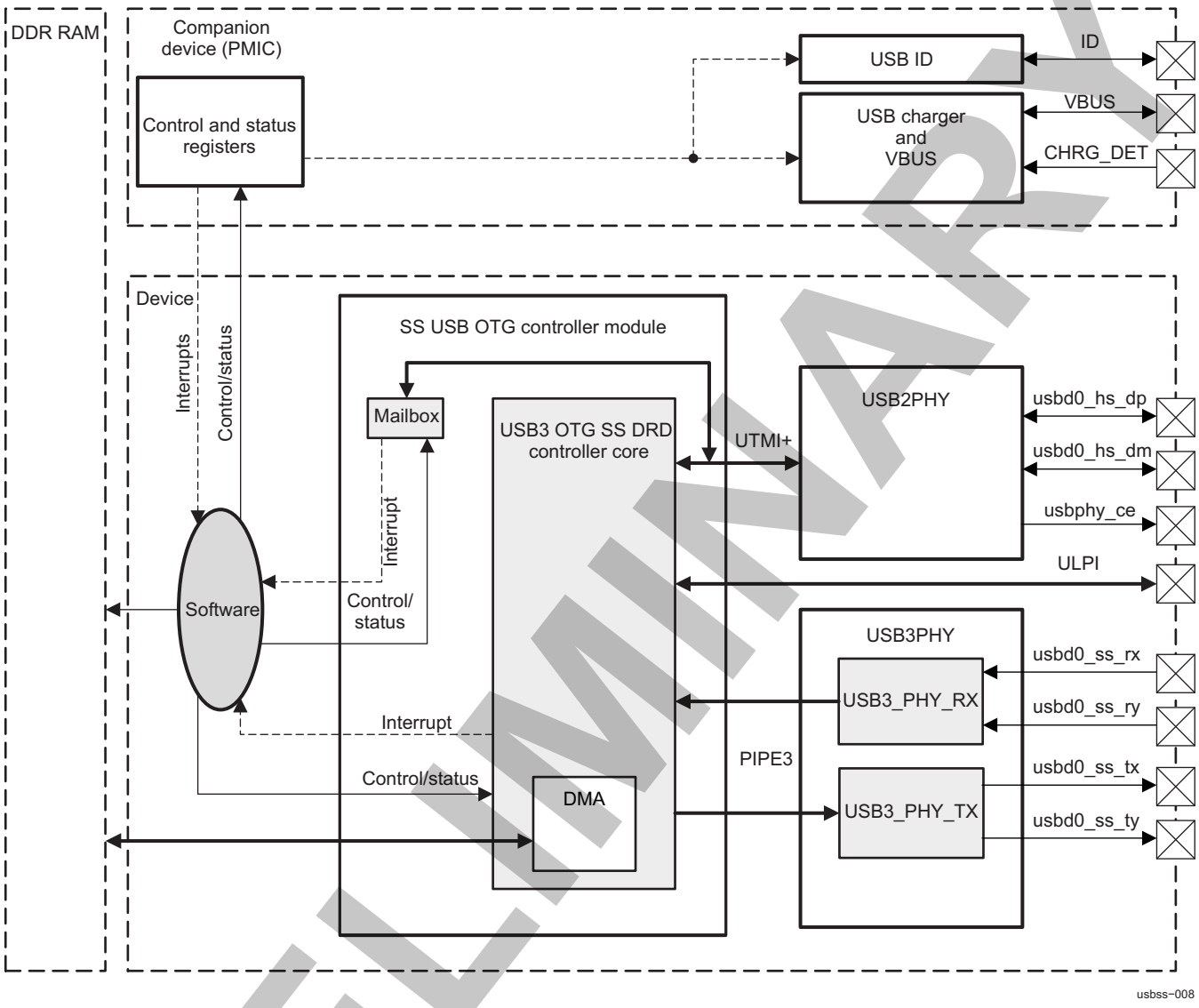
Figure 23-244. SuperSpeed USB Subsystem Operation Diagram



The eight USB I/O signals can be routed to a connector receptacle (for example USB3.0 micro-AB) to create a single USB3.0 OTG2 port. Alternatively, the four I/Os of the SS PHY can be left unconnected, with the remaining four routed to a connector receptacle (for example, the USB2.0 micro-AB) to create a single USB2.0 OTG2 port.

Data transfers proceed as follows:

1. USB software allocates blocks of the main memory for operation.
2. USB software issues commands to the controller (USB transmit, receive, etc.) together with the allocated addresses of the blocks.
3. The built-in DMA of the USB controller then executes the commands by either transmitting (read from memory, sent though USB PHY) or receiving (received through USB PHY, written to memory). The PHY used (either USB2 or USB3 PHY) depends on the configuration and context.
4. The USB controller returns a status to the software (using interrupts).

Operations involving:

- VBUS (from the simple drive/detection for the non-OTG host/peripheral to the more complex OTG control and status) and
- The OTG ID (DRD role determination)

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are expected to take place off-chip (that is, without a dedicated hardware link). Instead, the various control and status operations are expected to use ad-hoc channels supported by interrupts and miscellaneous communication interfaces. (For example, the TWL6035 PMIC is accessed through the I2C1 interface.). From a USB protocol standpoint, the latency associated with those ad-hoc channels is acceptable, because none of those operations is timing-critical. See Section 23.11.4.5.1, *Mailbox VBUS/ID Management* for more details on the mailbox mechanism.

23.11.4.7 External Buffer Control (EBC) Mode Operation

When the DMA is fetching (or writing) data to/from system memory, the assumption is that the data/free space is available as soon as the descriptors, that is, the TRBs, are filed to the controller. However, there are cases where the data is not really memory-mapped but stored in a FIFO, called below the EB for external buffer, and for which additional flow control is required.

The External Buffer Control (EBC) is a hardware interface that provides such a data flow control (throttling) with no additional software intervention. It is supported with the following limitations:

- Device mode only (not supported for host mode)
- BULK protocol, with EP size = bulk maximum packet size (64 bytes for FS, 512 for HS, 1024 for SS)
- Available on only two endpoints, one in each direction: EP15 IN (Tx), EP15 OUT (Rx)
- Large TRBs (multiple packets per descriptor)
- No multi-segment TRBs

NOTE:

- EBC-capable endpoints can be used in non-EBC mode as well: as long as the appropriate bit in USBOTGSS_DEV_EBC_EN has not been set, the endpoint retains its default behaviour, that is, Tx data (or space for Rx data) is available in system memory as soon as the TRB is given to the controller.
- EBC-operated endpoints must be configured (in the DEPCFG command) with command bitfield DEPCMDPAR1.LimitOutstandingTxDMA set to 1, to prevent several outstanding transactions from accessing the EB out of order, which is not allowed as the EB is a FIFO.
- EBC can operate in parallel with other device endpoints working in the regular, non-EBC mode.
- EBC mode provides standard and correct behaviour on the USB wire, even if the retries are not handled by the external buffer system, that is, even if data is not actually repeated upon retries.

23.11.4.7.1 IN (Tx) EP Operation In EBC Mode

Enabling procedure for the IN (transmit) EP in EBC mode:

1. Prepare the EB FIFO to handle the EBC hardware interface signals (described in Section 23.11.4.8.2, *Device-Mode Endpoint Commands*)
2. Write to 1 bitfield USBOTGSS_DEV_EBC_EN[15] INEP15 to enable the hardware interface on the controller side
3. Configure IN EP15 with the following requirements:
   - DEPCMDPAR1.LimitOutstandingTxDMA = 1 in DEPCFG command
   - TRB transfer descriptors pointing at the EB's memory mapping
   - (Optional) TRB structure can be a (linked list) loop stored in a special, read-only zone. This provides infinite recycling by preventing the DMA from upgrading TRBs and passing them to the software. This allows the transfer to proceed without any software intervention. Note that such a memory zone is not included in the controller, and requires specialized logic. For instance, it cannot use
     (a) a write-protected block of RAM, as the DMA writes would trigger MMU errors, or
     (b) a ROM, as the DMA writes would trigger system bus errors. Writes to this zone should be allowed to "fail silently", that is, have no effect and trigger no error.

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- EP size = maximum bulk packet size

4. Proceed like a non-EBC endpoint

Disabling the EP: If less than one packet-size of data is available in the EB, it is by construction invisible to the controller, and will never be fetched and transmitted (unless it is "pushed" over the threshold by more data). It is the responsibility of the system to ensure that no relevant data is stuck in the EB when the EP is disabled.

23.11.4.7.2 OUT (Rx) EP Operation in EBC Mode

Enabling procedure for the OUT (receive) EP in EBC mode:

1. Prepare the EB FIFO to handle the EBC HW interface signals (described in Section 23.11.4.8.2, *Device-Mode Endpoint Commands*)
2. Write to 1 bitfield USBOTGSS_DEV_EBC_EN[31] OUTEP15, to enable the hardware interface on the controller side
3. Configure OUT EP15 with the following requirements:
   - DEPCMDPAR1.LimitOutstandingTxDMA = 1 in DEPCFG command
   - TRB transfer descriptors pointing at the EB's memory mapping
   - EP size = maximum bulk packet size.
4. Proceed like a non-EBC endpoint

23.11.4.8 USB Device (Peripheral) Operation

The current section describes elements of device-mode operation. The controller in device-mode uses a dedicated set of programming registers, prefixed with a D, and described in Section 23.11.5.2, *DWC_USB3 registers*. For the complete programming model, refer to *DWC superspeed USB3 controller databook*.

Operation in USB device mode is controlled using the following tools:

- Device endpoint command registers: CSRs, accessed by the software driver through the controller slave (L4_CFG) interface. Commands pass the address in main memory of the transfer request block (TRB) to the controller DMA.
- TRBs: Mapped in main memory, TRBs describe the data buffers also located in main memory. Initially created by the software driver, read and updated by the controller DMA.
- Data buffers: Areas of main memory containing USB data to transmit or make available for received USB data. Data buffers are defined in the TRBs.
- Event buffer: Mapped in main memory, the event buffer is a circular buffer containing USB events written by the device controller and read by the device software driver.
- Interrupt line: flags core events

23.11.4.8.1 Device TRBs

Transfer request blocks (TRBs) are mapped in main memory as linked lists. They describe the data buffers also located in main memory. Initially created by the software driver, they are read by the controller DMA and updated by it, depending on USB activities.

Even through device TRBs are inspired by and similar to the host TRBs defined by the *Extensible Host Controller Interface (xHCI) for USB* specification, they are not identical. The main difference is that device TRBs are updated (written) by the controller DMA, unlike host TRBs, which are written only by the software driver and are read-only for the controller DMA.

NOTE: TRBs are structures implemented in the main memory.

Table 23-1068 through Table 23-1073 describe the 128 bits of the TRB as four 32-bit words.

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Table 23-1068. Device TRB Word Structure

Name	Address Offset
PARAM_LO	0x0
PARAM_HI	0x4
STATUS	0x8
CONTROL	0xC

Table 23-1069. Device TRB Detailed Field Summary

Device TRB field structure

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BPTRL																															
BPTRH																															
TRBSTS				Reserved		PCM1		BUFSIZ																							
Reserved		SID_SOFN													Reserved	IOC	ISP_IMI	TRBCTL					CSP	CHN	LST	HWO				

Table 23-1070. PARAM_LO

Bits	Field Name	Description	Type	Reset
31:0	BPTRL	Buffer pointer low: Data buffer's base address pointer, lower 32 bits.	RW	0x0000 0000

Table 23-1071. PARAM_HI

Bits	Field Name	Description	Type	Reset
31:0	BPTRH	Buffer pointer high: Data buffer's base address pointer, upper 32 bits.	RW	0x0000 0000

Table 23-1072. STATUS

Bits	Field Name	Description	Type	Reset
31:28	TRBSTS	TRB status. Updated by hardware transfer status information before releasing the TRB. 0x0: OK 0x1: MissedIsoc: Isochronous interval missed or incomplete. 0x2: SetupPending: Another SETUP was received during current control transfer data/status phase.	RW	0x0
27:26	Reserved		RO	0x0
25:24	PCM1	Packet count minus 1: Total number of packets in the buffer descriptor for high-speed, high-bandwidth isochronous IN endpoints in an Isoc-First TRB. 0x0: 1 packet 0x1: 2 packets 0x2: 3 packets 0x3: 4 packets	RW	0x0
23:0	BUFSIZ	Buffer size. Remaining size in bytes (to be sent/which can be received) in the TRB data buffer. Decremented by hardware after data is transferred. 0x000000: No remaining bytes in buffer 0xFFFFFF: 16 MiB – 1 remaining byte in buffer (maximum size)	RW	0x000000

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Table 23-1073. CONTROL

Bits	Field Name	Description	Type	Reset
31:30	Reserved		R	0x0
29:14	SID_SOFN	Stream ID/SOF number Stream-based bulk EP: The stream ID of the transfer. Isochronous EP: (micro)frame number in which the last packet of the buffer is transmitted (debug).	RW	0x0000
13:12	Reserved		R	0x0
11	IOC	Interrupt on complete. Applicable only when LST = 0, for a) IN EP or b) OUT EP when CSP = 1. Read-only for the USB controller DMA (hardware) Read 0: No action Read 1: XferInProgress event issued (with IOC bit set) on completion of buffer transfer.	R	0
10	ISP_IMI	Interrupt on short packet/interrupt on Missed ISOC. Controls the generation of the XferInProgress event. Read-only for the USB controller's DMA (hardware). Read 0: No action Read 1: XferInProgress event when: a) Receiving an unexpected short packet (OUT EP, LST = 0, CSP = 1) or b) The missed Isoc status is given (isochronous EP).	R	0
9:4	TRBCTL	TRB control. Type of TRB. Read-only for the USB controller DMA (hardware) Read 0x01: Normal (Bulk/Interrupt/Control-Data-n with n1) Read 0x02: Control-Setup Read 0x03: Control-Status-2 Read 0x04: Control-Status-3 Read 0x05: Control-Data-1 Read 0x06: Isochronous-1 (First TRB of Service Interval) Read 0x07: Isochronous-n (with n1) Read 0x08: Link TRB	R	0x0
3	CSP	Continue on short packet. Reaction of an OUT endpoint on reception of a short packet. Read-only for the USB controller DMA (hardware) Read 0: Generate XferComplete event and remove the stream. Read 1: Continue to the next buffer descriptor.	R	0
2	CHN	Chain buffers. Associates this TRB with the next in the same buffer descriptor. Always 0 in the last TRB of a buffer descriptor. Read-only for the USB controller DMA (hardware) Read 0: End of the current buffer descriptor. Read 1: Next TRB is part of the same buffer descriptor	R	0
1	LST	Last TRB. Indicates the last TRB in a list, that is, in a transfer for the endpoint/bulk-stream. Read-only for the USB controller DMA (hardware) Read 0: TRB list not complete Read 1: Last TRB	R	0
0	HWO	Hardware owner. TRB ownership. Set to 1 by software when creating the TRB. Software cannot modify the TRB again until cleared to 0 by hardware. There are exceptions for short packets on OUT endpoints and link TRBs. 0: Software-owned TRB 1: Hardware-owned TRB	RW	0

23.11.4.8.2 Device-Mode Endpoint Commands

Current subsection describes the endpoint commands passed by the device controller driver (software) to the device controller (hardware) through the appropriate memory-mapped control and status registers. The command is passed to endpoint i through register USBOTGSS_DEPCMD_i, with additional parameters passed through USBOTGSS_DEPCMDPAR0_i, USBOTGSS_DEPCMDPAR1_i and USBOTGSS_DEPCMDPAR2_i in case the 16-bit USBOTGSS_DEPCMD_i[31:16] CMDPARAM_EVTPARAM is not sufficent, depending on the command.

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Table 23-1074, *Device-mode Endpoint Commands Summary* is a summary of the EP commands, and which parameter registers are used (Y) in each case. Unused parameter registers are reserved. Each command is described in Section 23.11.4.8.2.1 through Section 23.11.4.8.2.9.

Table 23-1074. Device-mode Endpoint Commands Summary

	Command	Command full name	Parameter	PAR0	PAR1	PAR2
1	DEPCFG	Set EP configuration	64-bit	Y	Y	
2	DEPXFERCFG	Set EP transfer resource configuration	32-bit	Y		
3	DEPGETDSEQ	Get data sequence number	none			
4	DEPSETSTALL	Set stall	none			
5	DEPCSTALL	Clear stall	none			
6	DEPSTRTXFER	Start transfer	64-bit	Y	Y	
7	DEPUPDXFER	Update transfer	none			
8	DEPENDXFER	End transfer	none			
9	DEPSTARTCFG	Start new configuration	none			

23.11.4.8.2.1 Set EP Configuration (DEPCFG) Command

This command sets the configuration of the physical endpoint.

DEPCFG.CommandParam: unused (when USBOTGSS_DEPCMD_i register is written)

Additional parameters: 64-bit, stored in USBOTGSS_DEPCMDPAR0_i and USBOTGSS_DEPCMDPAR1_i, with the fields detailed in Table 23-1075 and Table 23-1076. Register USBOTGSS_DEPCMDPAR2_i is reserved.

Table 23-1075. USBOTGSS_DEPCMDPAR1_i Fields for DEPCFG Command

Bits	Field Name	Description	Type	Reset
31	FIFOBASED_EBCBASED	Isoc EP: TRBs never written back by the core, for FIFO-based data buffers. Bulk EP: Limit outstanding DMA transfers to 1 read + 1 write, required for EBC operation. 0: DISABLED Default EP behaviour (EBC not functional) 1: ENABLED Enable FIFO-based (for isoc EP) / EBC-based (for bulk EP) mode	RW	0x0
30	BULKBASED	Set to 1 for an isochronous EP to ignore intervals programmed in the TRBs, like a bulk EP. 0: DEFAULT Normal behaviour for isochronous EP 1: BBISOC Bulk-based isochronous EP	RW	0x0
29:26	EPNUMBER	Endpoint number for this physical EP. Control EP 0 OUT must be assigned to physical EP0 Control EP 0 IN must be assigned to physical EP1	RW	0x0
25	EPDIRECTION	Endpoint Direction for this physical endpoint Control EP 0 OUT must be assigned to physical EP0 Control EP 0 IN must be assigned to physical EP1 0: OUT direction (receive) 1: IN direction (transmit)	RW	0x0
24	STRMCAP	Stream Capable 0: NOTCAP EP is not stream-capable 1: CAP EP is stream-capable	RW	0x0
23:16	BINTERVAL_M1	bInterval value minus one, as reported in the EP descriptor. Set to 0 when operating in FS.	RW	0x0
15	LimitOutstandingTxDMA			
14	Reserved		RO	0x0
13	STREAMEVTEN	Stream Event DEPEVT enable 0: DIS event disabled 1: EN event enabled	RW	0x0
12	Reserved		RW	0x0

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Table 23-1075. USBOTGSS_DEPCMDPAR1_i Fields for DEPCFG Command (continued)

Bits	Field Name	Description	Type	Reset
11	RXTXFIFOEVTEN	RxTxFifoEvt DEPEVT event enable IN EP: FIFO underrun enable OUT EP: FIFO underrun enable 0: DIS event disabled 1: EN event enabled	RW	0x0
10	XFERNRDYEN	XferNotReady DEPEVT event enable 0: DIS event disabled 1: EN event enabled	RW	0x0
9	XFERINPROGEN	XferInProgress DEPEVT event enable 0 DIS event disabled 1 EN event enabled	RW	0x0
8	XFERCMPLEN	XferComplete DEPEVT event enable 0: DIS event disabled 1: EN event enabled	RW	0x0
7:5	Reserved		RW	0x0
4:0	INTRNUM	Interrupt/Event Buffer number on which interrupts for this EP are generated. Must be 0 if a single interrupter HW configuration. 0x00: INT0 Interrupt 0	RW	0x0

Table 23-1076. USBOTGSS_DEPCMDPAR0_i Fields for DEPCFG Command

Bits	Field Name	Description	Type	Reset
31	IGNORESEQNUM	Ignore Sequence Number: avoids resetting the sequence number upon DEPCFG command. Used to modify the DEPEVTEN event enable bits on the fly 0: RESET Sequence Number shall be reset to 0 1: IGNORE Sequence Number shall not change	RW	0x0
30:26	DSEQNUM	Data Sequence Number. Must be zero at initial EP configuration.	RW	0x0
25:22	BRSTSIZ	Burst Size minus 1 0x0: MIN 1-beat burst 0xF: MAX 16-beat burst	RW	0x0
24	STRMCAP	Stream Capable 0: NOTCAP EP is not stream-capable 1: CAP EP is stream-capable	RW	0x0
21:17	FIFONUM	FIFO number assigned to this EP. Control EP must have the same value for IN and OUT EP. OUT: use Rx FIFO number 0 IN: use only the lower 16 Tx FIFOs.	RW	0x0
16:14	Reserved		RW	0x0
13:3	MPS	Maximum Packet Size, in bytes	RW	0x0
2:1	EPTYPE	Endpoint type 0x0: CTRL Control EP 0x1: ISOC Isochronous EP 0x2: BULK Bulk EP 0x3: INT Interrupt EP	RW	0x0
0	Reserved		RW	0x0

23.11.4.8.2.2 Set EP Transfer Resource Configuration (DEPXFERCFG) Command

Command assigns a transfer resource to the endpoint. Resource is actually used between the start (Start Transfer) and the end (End Transfer command or XferComplete) of the transfer.

DEPCFG.CommandParam: unused (when USBOTGSS_DEPCMD_i register is written)

Additional parameters: 32-bit, stored in USBOTGSS_DEPCMDPAR0_i, with the fields detailed inTable 23-1077, *USBOTGSS_DEPCMDPAR0_i Fields for DEPXFERCFG Command*. Register USBOTGSS_DEPCMDPAR1_i and USBOTGSS_DEPCMDPAR2_i are reserved.

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Table 23-1077. USBOTGSS_DEPCMDPAR0_i Fields for DEPXFERCFG Command

Bits	Field Name	Description	Type	Reset
31:16	Reserved		RW	0x0
15:0	NUMXFERRES	Number of transfer resources allocated to this EP. Must be set to 1. 0x01: One resource	RW	0x0

23.11.4.8.2.3 Get Data Sequence Number (DEPGETDSEQ) Command

For non-isochronous EP only. Returns the current data sequence number for the EP, allowing it to be saved, and later restored using the DEPCFG command.

DEPCFG.CommandParam: unused (when USBOTGSS_DEPCMD_i register is written)

Additional parameters: None. Registers USBOTGSS_DEPCMDPAR0_i, USBOTGSS_DEPCMDPAR1_i and USBOTGSS_DEPCMDPAR2_i are reserved.

23.11.4.8.2.4 Set Stall (DEPSETSTALL) Command

Stalls all tokens to the EP, including if the EP is in NRDY state.

- OUT EP: ongoing packet completes normally, next OUT DP or token is stalled.
- IN EP, SS: current burst completes normally, next ACK TP is stalled.
- IN EP, HS/FS/LS: current packet completes normally, next IN token is stalled.
- Control EP: only the OUT direction shall be stalled
- Isochronous EP: not applicable, do not use

DEPCFG.CommandParam: unused (when USBOTGSS_DEPCMD_i register is written)

Additional parameters: None. Registers USBOTGSS_DEPCMDPAR0_i, USBOTGSS_DEPCMDPAR1_i, and USBOTGSS_DEPCMDPAR2_i are reserved.

23.11.4.8.2.5 Clear Stall (DEPCSTALL) Command

Clears the previously applied stall for the EP.

- Control EP: stall cannot be cleared by software: Hardware clears the stalls automatically when the next SETUP token is received.
- Non-Control EP: stall must be cleared by software. This also resets the DSeqNum to 0.
- Isochronous EP: not applicable, do not use

DEPCFG.CommandParam: unused (when USBOTGSS_DEPCMD_i register is written)

Additional parameters: None. Registers USBOTGSS_DEPCMDPAR0_i, USBOTGSS_DEPCMDPAR1_i, and USBOTGSS_DEPCMDPAR2_i are reserved.

23.11.4.8.2.6 Start Transfer (DEPSTRTXFER) Command

Indicates that a Transfer Descriptor (TD), that is, a list of TRBs that comprise one or more transfers, is ready to be processed. A pointer to the TD is recorded and is kept until the transfer ends (XferComplete event or DEPENDXFER command)

Hardware assigns the transfer a resource index number (XferRscIdx), returned in the USBOTGSS_DEPCMD_i register and in the Command Complete event, for use in subsequent Update and End Transfer commands.

Non-stream capable EP:

- StreamID must be set to 0
- HighPri is reserved

Stream-capable EP:

- StreamID must be non-zero and match the StreamID in the TRB at the Transfer Descriptor Address

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- HighPri may be set for one or more streams.
- Commands is issued for multiple streams, until the resources in DEPXFERCFG.NumXferRes are used up

DEPCFG.CommandParam:

- For isoc EP: CommandParam = StartMicroFramNum: 16-bit Frame / microframe number to which the first TRB of the transfer applies
- For stream-capable EP: CommandParam = StreamID: 16-bit USB stream ID associated to this transfer.

Additional parameters: 64-bit, stored in USBOTGSS_DEPCMDPAR0_i and USBOTGSS_DEPCMDPAR1_i, with the fields detailed in Table 23-1078 and Table 23-1079. Register USBOTGSS_DEPCMDPAR2_i is reserved.

Table 23-1078. USBOTGSS_DEPCMDPAR1_i Fields for DEPSTRTXFER Command

Bits	Field Name	Description	Type	Reset
31:0	TDADDR_LOW	Transfer Descriptor Address, lower 32 bits. Since TRBs must be aligned on a 16-byte boundary, the 4 LSBs of this field must be 0.	RW	0x0

Table 23-1079. USBOTGSS_DEPCMDPAR0_i Fields for DEPSTRTXFER Command

Bits	Field Name	Description	Type	Reset
31:0	TDADDR_HIGH	Transfer Descriptor Address, upper 32 bits. All 0 in 32-bit-address architectures.	RW	0x0

23.11.4.8.2.7 Update Transfer (DEPUPDXFER) Command

In the case of a circular TRB buffer, causes the hardware to re-cache the TRB following a TRB update by the software. Update includes the setting of HWO bit back to 1. The indicated resource transfer index identifies the updated TRB. It must have been previously started, then have completed its transfer (XferComplete event or an DEPENDXFER command)

Special No Response Update Transfer command is issued by setting CmdAct=0 and CmdIOC=0. In this case, no command complete (EpCmdCmplt) event is generated, CmdAct never changes, and another command may be issued to the same EP immediately. Do not use when software depends on the XferNotReady event to setup TRBs.

DEPCFG.CommandParam: CommandParam[6:0] = USBOTGSS_DEPCMD_i[22:16] = XferRscIdx: 7-bit Transfer resource index, assigned by the hardware to the transfer when it is started (DEPSTRTXFER command)

Additional parameters: None. Registers USBOTGSS_DEPCMDPAR0_i , USBOTGSS_DEPCMDPAR1_i , and USBOTGSS_DEPCMDPAR2_i are reserved.

23.11.4.8.2.8 End Transfer (DEPENDXFER) Command

Request DMA to stop for the EP/stream, because of an error condition. TRB is identified by its transfer resource index. ForceRM bit (USBOTGSS_DEPCMD_i[11] HIPRI_FORCERM) must be set to 1 to remove transfers from the queue. CmdIOC bit (USBOTGSS_DEPCMD_i[8] CMDIOC) must be set to 1 in order to an EP Command Complete event is generated after the transfer ends, to synchronize the conclusion of system bus traffic before the End Transfer command is completed.

Effect of the command:

- IN EP: A packet being transmitted may be truncated with the DPPABORT ordered set, any pending ACKs from the USB are ignored.
- OUT EP: Any data in the receive FIFO is moved to the corresponding memory buffer, until a packet boundary.
- TD processing stops, TRB status is not updated.

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- No XferComplete event is generated upon transfer end, only a CommandComplete event.

Use the command in the followng cases:

- To close EP when handling USBReset or SetConfiguration
- After receiving a ClearFeature (STALL) control transfer, before issuing Clear Stall, then Start Transfer
- After a XferInProgress event when the TRB after the one that caused the XferInProgress event has HWO=0
- For isochronous EP, if the host stops moving data for many intervals, to wait for the host to restart.

DEPCFG.CommandParam: CommandParam[6:0] = USBOTGSS_DEPCMD_i[22:16] = XferRscIdx: 7-bit Transfer resource index, assigned by the hardware to the transfer when it is started (DEPSTRTXFER command)

Additional parameters: None. Registers USBOTGSS_DEPCMDPAR0_i , USBOTGSS_DEPCMDPAR1_i , and USBOTGSS_DEPCMDPAR2_i are reserved.

23.11.4.8.2.9 Start New Configuration (DEPSTARTCFG) Command

Command issued to start a new configuration, in the following cases :

- Only to EP 0 (USBOTGSS_DEPCMD_i (i = 0))
- After power-on-reset with XferRscIdx=0 before starting to configure EP 0 and 1. CmdIOC bit (USBOTGSS_DEPCMD_i[8] CMDIOC) must be set to 0 and CmdAct bit CmdIOC bit (USBOTGSS_DEPCMD_i[10] CMDACT) must be polled because EP 0 is not yet configured with a valid interrupt number at that point.
- With XferRscIdx=2 when it receives SetConfiguration before starting to configure EP > 1.

Transfer resource allocation gets reset to the value in the XferRscIdx parameter (must be 0 or 2).

DEPCFG.CommandParam: CommandParam[6:0] = USBOTGSS_DEPCMD_i[22:16] = XferRscIdx: 7-bit Transfer resource index, assigned by software when the new configuration is started (DEPSTARTCFG command)

Additional parameters: None. Registers USBOTGSS_DEPCMDPAR0_i , USBOTGSS_DEPCMDPAR1_i , and USBOTGSS_DEPCMDPAR2_i are reserved.

23.11.4.8.3 Device-Mode Events

The current subsection describes the status events passed by the device controller (hardware) to the device controller driver (software) though the event buffer(s) mapped in system memory. Most events fit in a single (32-bit) dword. The one exception is the Vendor device test LMP received event, which takes 3 dwords.

Table 23-1080 gives a summary of all possible events

- Events are decoded from right to left (LSbits to MSbits)
- Each line is a different category of event, described in Section 23.11.4.8.3.1, *Endpoint Events (DEPEVT)* and Section 23.11.4.8.3.2, *Device events (DEVT)*. The number in the first column is a link to the corresponding event description table.
- Short field names (a1, a2, b1, etc.) are described in Table 23-1084.

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Table 23-1080. Device-Mode Events Summary

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	EventParam																EventStatus						EP event type				Physical EP num (0..31)					0 = DEPEVT
2	StreamID (only for bulk EP that supports streams)																a1	b1	c1	d1			4'b1 = XferComplete				Physical EP num (0..31)					0 = DEPEVT
3	IsocMicroFrameNum (for debug)																a2	b1	c1	d1			4'b2 = XferInProgress				Physical EP num (0..31)					0 = DEPEVT
4	StreamID (only for bulk EP that supports streams)																a3		b3				4'b3 = XferNotReady				Physical EP num (0..31)					0 = DEPEVT
5	(unused)																(unused)						4'b4 = RxTxFifoEvt				Physical EP num (0..31)					0 = DEPEVT
6	StreamID (only for bulk EP that supports streams)																a5 (idem)						4'b6 = StreamEvt				Physical EP num (0..31)					0 = DEPEVT
7	EventParam[15:12]				Command Type				EventParam[7:0]								EventStatus						4'b7 = EpCmdCmplt				Physical EP num (0..31)					0 = DEPEVT
8	(unused)				4'b2 = DepXferCfg				(unused)								a7						4'b7 = EpCmdCmplt				Physical EP num (0..31)					0 = DEPEVT
9	(unused)				4'b3 = DepGetDSeq				(unused)			CurDatSeqNum					(unused)						4'b7 = EpCmdCmplt				Physical EP num (0..31)					0 = DEPEVT
10	(unused)				4'b6 = DepStrtXfer					XferRscIdx							a9						4'b7 = EpCmdCmplt				Physical EP num (0..31)					0 = DEPEVT
11									EvtInfo												Device event sub-type		non-EP event type								1 = non-EP
12									(unused)												4'b0 = DisconnEvt		7'b0 = Device-Specific event (DEVT)								1 = non-EP
13									(unused)												4'b1 = UsbRst		7'b0 = Device-Specific event (DEVT)								1 = non-EP
14									(unused)												4'b2 = ConnectDone		7'b0 = Device-Specific event (DEVT)								1 = non-EP
15									(unused)			a13	b13								4'b3 = ULStChng		7'b0 = Device-Specific event (DEVT)								1 = non-EP
16									(unused)												4'b4 = WkUpEvt		7'b0 = Device-Specific event (DEVT)								1 = non-EP
17									(unused)												4'b6 = EOPF		7'b0 = Device-Specific event (DEVT)								1 = non-EP
18									(unused)												4'b7 = SOF		7'b0 = Device-Specific event (DEVT)								1 = non-EP
19									(unused)												4'b9 = ErrticErr		7'b0 = Device-Specific event (DEVT)								1 = non-EP
20									(unused)												4'b10 = CmdCmplt		7'b0 = Device-Specific event (DEVT)								1 = non-EP

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Table 23-1080. Device-Mode Events Summary (continued)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
21									(unused)												4'b11 = EvntOverflow				7'b0 = Device-Specific event (DEVT)							1 = non-EP
22									Vendor-Specific Device Test Field												4'b12 = VndrDevTstRcved				7'b0 = Device-Specific event (DEVT)							1 = non-EP
	Vendor-Defined Data (dword 1/2)																															
	Vendor-Defined Data (dword 2/2)																															

Table 23-1081 lists the event types, as used in the event buffer (dword 0 bits [7:0])

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Table 23-1081. Event Type

bit [7:1]	bit [0]	Name	Comments
don't care	0	DEPEVT	Device-mode, Endpoint-specific event
don't care	1	non-EP	Device-mode, non-endpoint-specific event
0000000	1	DEVT	Device-mode, Device event

Table 23-1082 lists the 4-bit endpoint events (DEPEVT), as used in the buffer (dword 0 bits [9:6]).

Table 23-1082. Endpoint Event (DEPEVT) Types

DEPEVT	Name	Comments
0x0	reserved	
0x1	XferComplete	Transfer complete
0x2	XferInProgress	Transfer in progress
0x3	XferNotReady	Transfer not ready
0x4	RxTxFifoEvt	Receive/Transmit FIFO event
0x5	reserved	
0x6	StreamEvt	Stream Event
0x7	EpCmdCmplt	Endpoint Command Complete
0x8 to 0xF	reserved	

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Table 23-1081 lists the 4-bit device-specific events (DEVT), as used in the buffer (dword 0 bits [11:8]).

Table 23-1083. Device-Specific Event (DEVT) Types

DEVT	Name	Comments
0x0	DisconnEvt	Disconnect detected
0x1	UsbRst	USB reset detected
0x2	ConnectDone	Connect done event
0x3	ULStChng	USB or Link state change event.
0x4	WkUpEvt	Host resume (wakeup) detected
0x5	reserved	
0x6	EOPF	End of periodic frame
0x7	SOF	Start of (micro-)frame
0x8	reserved	
0x9	ErrticErr	Erratic error
0xA	CmdCmplt	Generic command complete
0xB	EvntOverflow	Event buffer overflow
0xC	VndrDevTstRcved	Vendor device test LMP received from link partner.
0xD to 0xF	reserved	

Table 23-1084. Device-Mode Events Encoding, Short Fields

Field	Bits	Description
d1	12	XferComplete/XferInProgress EP event: 1'b1: Bus error occurred.
c1	13	XferComplete/XferInProgress EP event: 1'b1: TRB completed with short packet reception or last packet of isoc interval.
b1	14	XferComplete/XferInProgress EP event: 1'b1: IOC bit of the TRB that completed.
a1	15	XferComplete EP event: 1'b1: LST bit of the completed TRB.
a2	15	XferInProgress EP event: MissedIsoc: 1'b1: Interval did not complete successfully.
b3	13:12	XferNotReady EP event: requested stage when (control) transfer was not ready: 2'b00: Control SETUP request 2'b01: Control data request 2'b10: Control status request
a3	15	XferNotReady EP event: 1'b0: XferNotActive: Host initiated a transfer not present in the hardware. 1'b1: XferActive: Host initiated a transfer that is present but no valid TRBs are available.
a5	15:12	StreamEvt EP event (only for bulk EP that supports streams): 4'h2: StreamNotFound: No active, ready stream found in transfer resource cache. 4'h1: StreamFound: Active and ready stream found, traffic to the host initiated for that stream.
a7	15:12	EpCmdCmplt EP event, DepXferCfg command: 4'h1: Error: Software requesting more transfer resources than are configured in the hardware.
a9	15:12	EpCmdCmplt EP event, DepStrtXfer command:
b13	19:16	ULStChng device-specific event: Link state upon event. See DSTS register for encoding.
a13	20	ULStChng device-specific event: SS event. 1'b1: SS 1'b0: non-SS

23.11.4.8.3.1 Endpoint Events (DEPEVT)

Category of events is specific to data endpoints (EP). Several types of EP events exist, with different field structures.

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Table 23-1085. Endpoint Events (DEPEVT)

Description	
Endpoint event (DEPEVT)	
Size in event buffer:	1 dword
Key:	Event type = evt[0] = DEPEVT
Subfields:	Physical EP number = evt[5:1]
	EP event type = evt[9:6]
	EventStatus = evt[15:12]
	EventParam = evt[31:16]

Table 23-1086. Transfer complete EP event (XferComplete)

Description	
Type of endpoint event generated upon completion (sucessful or not) of a IN or OUT USB transfer.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = DEPEVT
	EP event type = evt[9:6] = XferComplete
Other fields:	EventParam = Stream ID = (if applicable, i.e. BULK EP with stream support)
	EventStatus = Bus Error flag + last isoc / short packet flag + IOC of TRB + LST of TRB
	Physical EP number

Table 23-1087. Transfer in progress EP event (XferInProgress)

Description	
Type of endpoint event generated during the processing of a still-ongoing transfer.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = DEPEVT
	EP event type = evt[9:6] = XferInProgress
Other fields:	EventParam = IsocMicroFrameNum
	EventStatus = Missed isoc flag + last isoc / short packet flag + IOC of TRB + LST of TRB
	Physical EP number (0 to 31)

Table 23-1088. Transfer not ready EP event (XferNotReady)

Description	
Type of endpoint event that indicates receipt of a transaction when no TRBs are available for the EP. For isochronous IN endpoints, a zero-length packet is sent. For non-isochronous endpoints, an NRDY is sent.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = DEPEVT
	EP event type = evt[9:6] = XferNotReady
Other fields:	EventParam = Stream ID = (if applicable, i.e. BULK EP with stream support)
	EventStatus = Xfer active flag + control phase (status/data)
	Physical EP number (0 to 31)
Generation of the event:	For stream-capable EP, generated each time the host attempts a transaction.
	For non-stream-capable EP, generated only on the first transaction attempt after an EP command to this EP.
	For isochronous EP, generated only once prior to the Start Transfer command to communicate the current bus time.

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Table 23-1089. FIFO EP event (RxTxFIFOEvt)

Description	
Type of endpoint event generated upon FIFO underrun / overrun, for debug only.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = DEPEVT
	EP event type = evt[9:6] = RxTxFIFOEvt
Other fields:	Physical EP number (0 to 31)
Generation of the event:	Only possible when thresholding is enabled
	FIFO underrun for IN EP = USB transmission
	FIFO overrun for OUT, non-isochronous EP = USB reception

Table 23-1090. Stream EP event (StreamEvt)

Description	
Type of EP event indicating that a stream-capable EP initiated a search within its transfer resource cache. The result of the search is in the EventStatus field.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = DEPEVT
	EP event type = evt[9:6] = StreamEvt
Other fields:	EventParam = Stream ID = (if applicable)
	EventStatus = Found / NotFound flag
	Physical EP number (0 to 31)

Table 23-1091. Device EP command complete event (EpCmdCmplt)

Description	
Category of EP events generated upon completion of an EP command. Several sub-types exist depending on the command. Those with specific field structures are listed in the chapters below.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = DEPEVT
	EP event type = evt[9:6] = EpCmdCmplt
Other fields:	EventParam (contains the Command type, and more depending on the command)
	EventStatus (depending on the command)
	Physical EP number (0 to 31)

Table 23-1092. Device EP command complete event (EpCmdCmplt): set transfer resource

Description	
Type of EP event generated upon completion of the Set transfer resource command	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = DEPEVT
	EP event type = evt[9:6] = EpCmdCmplt
	Command type = EventParam[11:8] = evt[27:24] = DepXferCfg
Other fields:	EventStatus = Error flag for the command
	Physical EP number (0 to 31)

Table 23-1093. Device EP command complete event (EpCmdCmplt): get data sequence

Description	
Type of EP event generated upon completion of the Get data sequence command	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = DEPEVT

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Table 23-1093. Device EP command complete event (EpCmdCmplt): get data sequence (continued)

Description	
	EP event type = evt[9:6] = EpCmdCmplt
	Command type = EventParam[11:8] = evt[27:24] = DepGetDSeq
Other fields:	EventParam[4:0] = CurDatSeqNum : current data sequence number
	Physical EP number (0 to 31)

Table 23-1094. Device EP command complete event (EpCmdCmplt): start transfer

Description	
Type of EP event generated upon completion of the Start transfer command	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = DEPEVT
	EP event type = evt[9:6] = EpCmdCmplt
	Command type = EventParam[11:8] = evt[27:24] = DepStartXfer
Other fields:	EventParam[7:0] = XferRscIdx : resource index number
	EventStatus = Error flag for the command
	Physical EP number (0 to 31)

23.11.4.8.3.2 Device events (DEVT)

All non-EP events are listed in Table 23-1096 through Table 23-1106. Note that the only type of non-EP event is the device event, that is, an event that applies to the entire device, as opposed to only an EP.

NOTE: DEVT described here must not to be confused with device-mode events, that is, all events generated by the controller when in USB device mode, including the EP events (DEPEVT) described in the previous section.

Table 23-1095. Device events (DEVT)

Description	
Device event (DEVT)	
Size in event buffer:	1 or 3 dword depending on event
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
Other fields:	device event type = evt[11:8]
	EvtInfo = evt[23:16]

Table 23-1096. Disconnect DEVT event (DisconnEvt)

Description	
Device event generated upon disconnect detection.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = DisconnEvt
Other fields:	none (EvtInfo is unused)

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Table 23-1097. USB reset DEVT event (UsbRst)

Description	
Device event generated upon USB reset detection.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = UsbRst
Other fields:	none (EvtInfo is unused)

Table 23-1098. Connect done DEVT event (ConnectDone)

Description	
Device event generated upon USB connect detection.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = ConnectDone
Other fields:	none (EvtInfo is unused)

Table 23-1099. USB / link status change DEVT event (ULStChng)

Description	
Device event generated upon USB / Link status change. In superspeed, generated only when entering the following USB3 LTSSM states: Rx.Detect, SS.Disabled, Polling, U1, U2, U3, or Recovery (only from U1, U2, U3).	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = WkUpEvt
Other fields:	EvtInfo[4] = SuperSpeed flag
	EvtInfo[3:0] = Link State

Table 23-1100. Wakeup DEVT event (WkUpEvt)

Description	
Device event generated upon detection of USB resume from the remote host. WARNING: Event is not generated by the device's own remote wakeup, or by the resume normally transmitted by the host in reply to that.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = WkUpEvt
Other fields:	none (EvtInfo is unused)

Table 23-1101. End of periodic frame DEVT event (EOPF)

Description	
Device event generated at the end of periodic frame.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = EOPF
Other fields:	none (EvtInfo is unused)

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Table 23-1102. Start of frame DEVT event (SOF)

Description	
Device event generated at the start of (micro-)frame.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = SOF
Other fields:	none (EvtInfo is unused)

Table 23-1103. Erratic error DEVT event (ErrticErr)

Description	
Device event generated upon erratic error event: Rxvalid / rxactive signals incorrectly asserted (by the USB2 PHY) for more than 2 ms on UTMI interface. Device then goes to Suspended, with a ULStChng event generated. Recovery from that error requires a soft disconnect.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = ErrticErr
Other fields:	none (EvtInfo is unused)

Table 23-1104. Command Complete DEVT event (CmdCmplt)

Description	
Device event generated upon (non-EP) command completion.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = CmdCmplt
Other fields:	none (EvtInfo is unused)

Table 23-1105. Event buffer overflow DEVT event (EvntOverflow)

Description	
Device event generated upon event buffer overflow: One or more events may have been dropped after this event, when buffer became full.	
Size in event buffer:	1 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = EvntOverflow
Other fields:	none (EvtInfo is unused)

Table 23-1106. Vendor device test LMP received DEVT event (DevTstRcved)

Description	
Device event generated upon receipt of vendor device test LMP from link partner	
Size in event buffer:	3 dword
Key fields:	Event type = evt[0] = non-EP
	non-EP event type = evt[7:1] = DEVT
	device event type = evt[11:8] = DevTstRcved
Other fields:	EvtInfo = LMP's Vendor-Specific Device Test Field
	LMP's Vendor-defined data (2 dwords = 64 bits total)

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23.11.4.9 USB Host Operation

The host operates in all speeds (SS, HS, FS, LS) per the standard xHCI API (see *Extensible Host Controller Interface [xHCI] for USB)*. It uses a dedicated set of programming registers (with no specific prefix, unlike the G, D, and O prefixes used for the global, device and OTG registers).

Optional xHCI features implemented by the controller are described by the memory-mapped capability descriptors, as per the standard.

23.11.4.9.1 Manual Far-end Receiver Detection in USB3 Host Mode

As per the USB3 standard (see LTSSM operation in *Universal Serial Bus 3.0 Specification*), an idle USB3 host (downstream) port must periodically check the status of its own transmitter regarding the presence of a connected receiver (far-end receiver detection a.k.a. TxDetectRx) in two cases:

- When the port is enabled (VBUS is supplied) but not connected yet, in order to check every 12 ms for a possible new connection.
- When the port is enabled, has connected, then suspended (to U3), in order to verify every 100 ms that the connection has not been broken.

Accordingly, the host controller's hardware state machine must periodically go and check the USB3 connection.

- This is not optimal because the host is constantly clocked and powered, while spending most of the time waiting. As a result, virtually all the time not spent transferring actual data will be spent in one of the two infinite loops above.
- On the other hand, note that the DRD controller is only in USB host mode if a USB peripheral device is connected to it, or at least the (A-side) cable of a USB device attached to it. By default, that is, with the connector receptacle empty, the DRD is in USB peripheral device mode.
- Also, note that the DRD is also required to drive VBUS (5V) whenever it is in USB host mode: the power spent to poll the connection status must be compared to the power spent to drive the VBUS, to decide if the optimizations described below are worth the effort. This is highly implementation-dependent.

The following low-power, software-controlled connection status polling alternative is available:

- Automatic hardware-controlled polling is disabled.
- An external, software-controller ad hoc timer is programmed for the desired polling period (12 or 100 ms).
- Whenever the timer rolls over, the software manually triggers the far-end receiver detection
- Between two detections, the USB core is placed in a low-power mode
- This continues until the connection status changes (during polling interval), or until another wakeup event occurs (at any time, as per USB protocol).

Section 23.11.4.9.1.1 through Section 23.11.4.9.1.3 describe this alternative, lower-power manual procedure in detail.

NOTE: The procedures in the subsequent sections:

- Relevant in USB host-mode only (hence the reliance on xHCI features). Unlike host mode where far-end termination on DSP repeats (and consumes power) forever, device-mode far-end termination on USP times out after 8 retries when in Rx.Detect state, and is not required at all when in U3 state: provided the adequate wakeup mechanism is in place, a USB peripheral device can eventually be placed in a low-power mode. Accordingly, the automatic detection procedure shall be active regardless when in USB device mode.
- Relevant in USB3 mode only. When operating as a USB2-only host (HS/FS/LS on the USB2 lines), far-end receiver detection (on the USB3 lines) does not apply.

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23.11.4.9.1.1 Manual receiver detection enabling

Manual mode is enabled (default hardware-driven mode is disabled) by writing field USBOTGSS_GUSB3PIPECTL[22] DISRXDETU3RXDET to 1. This can be done early in the controller's initialization, for example, even before the host/device role has been determined, since the setting has no effect in the default device mode.

From that point on, and assuming no change on the USB bus, the behaviour of the hardware core's LTSSM in host mode changes as follows:

- After reaching Rx.Detect.Quiet, stay in that state indefinitely (do no receiver detection) instead of exiting after a 12 ms timeout to Rx.Detect.Active state (and do receiver detection).
- While in U3 state, never do receiver detect, instead of doing so every 100 ms with infinite retries.

The recommended method to detect a connection change in manual mode is the LTSSM state readout in register USBOTGSS_PORTSC1/2[8:5] PLS

- A disconnection is characterized by a transition out of U3 (to Rx.Detect, etc…)
- A connection by a transition out of Rx.Detect (to Polling, etc…).

The procedure is to wait the appropriate time, then read the state. If the state has changed, the controller should be allowed to proceed normally. In the opposite case (no change), the controller can return to a low-power mode. In other words, it's not the specific state that the LTSSM has gone to that is of interest, it's the fact that the state has changed at all.

Another method is to use xHCI port state change events. However, the granularity of that method is not as good as, both in terms of LTSSM state (the PORTSC) time (the interrupt can be further delayed by moderation) LTSSM state granularity xHCI programming registers do not give access to the

23.11.4.9.1.2 Manual receiver detect procedure, waiting for connection (Rx.Detect)

Once manual receiver detect has been enabled (USBOTGSS_GUSB3PIPECTL[22] DISRXDETU3RXDET = 1, see Section 23.11.4.9.1.1), the following procedure is required in USB host mode to remain USB3 compliant. On the other hand, it must not be applied in USB device mode, as the automatic receiver detect is always enabled in that mode.

Whenever entering the (default) Rx.Detect LTSSM state (from any other state), the controller proceeds as usual through Rx.Detect.Reset and enter Rx.Detect.Active. In that last state, it automatically performs the expected receiver detect, once. Note that this first detection takes place with the PIPE interface in P2 state (that is, with PIPE clock running). The following detections (below) take place in P3 (PIPE clock stopped).

If the detection succeeds (USB3 device is connected), the LTSSM proceeds to Polling state as usual. No additional intervention is required.

If the detection fails (no USB3 device connected yet), the LTSSM proceed to Rx.Detect.Quiet as usual, and stays there forever, preventing any further receiver detection. The manual procedure starts then.

- The transition to Rx.Detect.Quiet can be detected by actively polling USBOTGSS_GDBGLTSSM[25:22] LTDBLINKSTATE and [21:18] LTDBSUBSTATE. Encoding is indicated in Table 23-1110, *LTSSM State/Substate Encoding* (core_ltdb_substate[3:0]). In any case, the transition to low-power mode (below) must first ensure that all clocks are stopped, which implies that PIPE is in P3, which in turn implies that the LTSSM sub-state is Rx.Detect.Quiet.
- An always-on timer (ad hoc, located outside the current USB controller) must be set to interrupt the software every 12 ms. The first interval must be made smaller to take the first wakeup latency into account.
- The USB controller must be placed in low-power mode. Details may vary depending on the transceiver/PLL properties.
  - all interrupts/software events cleared
  - system bus initiator in standby mode
  - system bus target in idle mode
  - all clock inputs stopped (including suspend clock that would normally run the 12-ms counter)
  - logic placed in retention mode (outputs isolated, etc…)
  - PIPE interface in P3 mode with the PIPE clock stopped. The controller goes to P3 state

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automatically after the first Rx detection (above) fails.

- When the timer rolls over (after 12 ms), bring the module back out of low-power mode. This includes restarting the interface and suspend clock. The PIPE interface remains in P3 (unclocked).
- Trigger the receiver detect by writing 1 to USBOTGSS_GUSB3PIPECTL[22] DISRXDETU3RXDET
- Wait for the receiver detection to take place. The delay depends on the provided suspend clock speed and on the PHY's response time.
- Poll the LTSSM state in xHCI register USBOTGSS_PORTSC1/2[8:5] PLS
- When the delay elapses (or if a connect event happens before that):
  - If the LTSSM state is still Rx.Detect, no receiver has been detected: port must return to Rx.Detect.Quiet substate. The controller can be placed back into low-power mode (see above). Procedure loops indefinitely until a receiver is detected.
  - If the LTSSM is different from Rx.Detect, a receiver has been detected: port advances to Polling state and proceed with USB3 polling as in the regular mode. Manual detection is over, and always-on 12-ms timer can be disabled and released.

The procedure above will be interrupted by any other state change on the bus, local or remote, as per xHCI: power-on reset, host mode exit, etc…

23.11.4.9.1.3 Manual receiver detect procedure, checking the connection (U3)

Once manual receiver detect has been enabled (USBOTGSS_GUSB3PIPECTL[22] DISRXDETU3RXDET = 1, see Section 23.11.4.9.1.1), the following procedure is required in USB host mode to remain USB3 compliant. On the other hand, it must not be applied in USB device mode, as the automatic receiver detect is always enabled in that mode.

A disconnection is characterized by a transition out of U3 (to Rx.Detect, etc…)

After entering the U3 LTSSM state (from U0), the controller stays there forever until a wakeup is issued by either side, and does not perform any receiver detection. The manual procedure starts there.

- The transition to U3 can be detected by actively polling USBOTGSS_PORTSC1/2[8:5] PLS. In any case, the transition to low-power mode (below) must first ensure that all clocks are stopped, which implies that PIPE is in P3, which in turn implies that the LTSSM sub-state is P3.
- An always-on timer (ad hoc, located outside the current USB controller) must be set to interrupt the software every 100 ms. The first interval must be made smaller to take the first wakeup latency into account.
- The USB controller must be placed in low-power mode. Details may vary depending on the transceiver / PLL properties.
  - all interrupts/software events cleared
  - system bus initiator in standby mode
  - system bus target in idle mode
  - all clock inputs stopped (including suspend clock that would normally run the 100 ms counter)
  - logic placed in retention mode (outputs isolated, etc…)
  - PIPE interface in P3 mode with the PIPE clock stopped, as implied by the U3 LTSSM state.
- When the timer rolls over (after 100 ms), bring the module back out of low-power mode. This includes restarting the interface and suspend clock. The PIPE interface remains in P3 (unclocked).
- Trigger the receiver detect by writing 1 to USBOTGSS_GUSB3PIPECTL[22] DISRXDETU3RXDET
- Wait for the receiver detection to take place. The delay depends on the provided suspend clock speed and on the PHY's response time.
- Poll the LTSSM state in xHCI register USBOTGSS_PORTSC1/2[8:5] PLS
- When the delay elapses (or if a connect event happens before that)
  - If the LTSSM state is still U3, the receiver is still connected. The controller can be placed back into low-power mode (see above). Procedure loops indefinitely unless the receiver connection is lost.
  - If the LTSSM is different from U3, the receiver detection has been lost: port advances to Rx.Detect state. Manual detection is over, and always-on 100 ms timer can be disabled and released.

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The procedure above will be interrupted by any other state change on the bus, local or remote, as per xHCI: USB wakeup, USB reset, power-on reset, host mode exit, etc…

23.11.4.10 USB OTG Operation

USB on-the-go (OTG) operation uses a dedicated set of programming registers, prefixed with an O (the letter). It generates a number of interrupt events, all of which are routed to IRQ line USB_OTG_SS_IRQ_WRP. Unlike the device and the host's operation, the OTG does not write interrupt status events to system memory through its master interface. Instead, the status must be read out directly from internal status registers. For the complete programming model, refer to the *DWC superspeed USB3 controller databook*

23.11.4.11 Trace Export Over USB

The current section describes a method to use a (USB3) bulk IN endpoint (EP) to export a stream of trace data to a remote (USB3) host. As such, it does not describe any specific feature of the existing core, only a guaranteed method to exploit the USB device for a specific purpose.

23.11.4.11.1 Trace Export Requirements

Trace data is a stream of data generated by monitoring the activity of a processor (CPU), and to be exported to a specialized equipment for analysis. The requirements are the following:

- Minimum or no software intervention while in continuous operation. The goal of that is not only to avoid polluting the trace (as any software operation runs on the CPU, and appears on trace), but also to avoid any perturbation on the observed (and potentially troublesome) software execution.
- Data integrity is preferred. For that reason, bulk (that is, retries) is preferred to retry-less isochronous, even though it has no bandwidth reservation.
- Simultaneous operation on other endpoints. It must be possible to run functional EPs of the USB device, while transmitting trace data. This assumes that the functional operation to be preserved is USB-device mode, the only one compatible with trace export.
- Sufficient bandwidth. This depends on the MPU type and count, but typically requires USB3 speed. The same method is also valid for USB2 speeds.

The current section focuses on the bulk IN EP's continuous operation, that is, the transmission of data from the current controller to a remote host, following initial configuration. A bulk OUT EP may also be used to control trace operations, but this is outside the scope of this section.

NOTE: The present method requires the following from the system:

- A memory-mapped buffer where the trace data is available, as advertised by the TRBs, and where it can be fetched by the USB controller's DMA engine.
- A dataflow pacing mechanism to control the DMA's fetching of trace data. Without this mechanism, the infinite, instantaneous TRB recycling explained below would cause the USB controller to (try and) saturate the available USB bandwidth. This would happen regardless of the availability of actual trace data.
- A way to write-protect a block of TRBs, so that they are never updated by the DMA: this will create an automatic (without software intervention) recycling of the TRBs, since they cannot be handed over to the software driver by the DMA, and will remain hardware-owned forever. The write protection causes "silent failures" on writes, that is, writes will not change the TRB value (have no effect) but that wil not trigger an error, either. For instance, storing predetermined TRBs in a ROM will not work if write accesses to the ROM are rejected by the interconnect.

23.11.4.11.2 Trace Export Procedure

The system relies on a TRB list mapped in a read-only block, as explained in Section 23.11.4.11.1, *Trace export requirements*. The list is turned into an infinite loop by a link TRB. An example is shown in Table 23-1107, *TRB Block Example For Trace Export*:

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- Three TRBs are mapped in a contiguous block.
- The first two TRBs (TRB1 and TRB2) are identical.
  - Normal TRB, chain bit set
  - TRB points at the trace data buffer (64-bit address 0x0000 0000 3300 0000)
  - Buffer has the maximum size that is a multiple of the maximum packet size (1 KiB)
- The reason there are two TRBs instead of only one is to allow the DMA's list processor to prefetch one while executing the other.
- The third and last TRB (TRB3) loops back to TRB1 (64-bit address 0x0000 0000 1234 ABC0)

For more information on the TRB data structure, see Section 23.11.4.8.1, *Device TRBs*.

Table 23-1107. TRB Block Example For Trace Export

Address	Data (32-bit)	Access	Comments
0x1234 ABC0	0x3300 0000	R	TRB1: debug-buffer pointer low
0x1234 ABC4	0x0000 0000	R	TRB1: debug-buffer pointer high
0x1234 ABC8	0x00FF FC00	R	TRB1: buffer size = 16Mbyte-1kbyte
0x1234 ABCC	0x0000 0015	R	TRB1: normal TRB, CHN=1
0x1234 ABD0	0x3300 0000	R	TRB2: debug-buffer low
0x1234 ABD4	0x0000 0000	R	TRB2: debug-buffer high
0x1234 ABD8	0x00FF FC00	R	TRB2: buffer size = 16Mbyte-1kbyte
0x1234 ABDC	0x0000 0015	R	TRB2: normal TRB, CHN=1
0x1234 ABE0	0x1234 ABC0	R	TRB3: TRB1 pointer low
0x1234 ABE4	0x0000 0000	R	TRB3: TRB1 pointer high
0x1234 ABE8	0x0000 0000	R	TRB3:
0x1234 ABEC	0x0000 0081	R	TRB3: link TRB

Initiating the trace export

1. Configure the controller in device mode (if not already done)
2. Configure a bulk IN endpoint for maximum performance: maximum packet size (1 KiB), bursting support, etc. Note that streaming is not relevant here, as there is only one stream of data.
3. Make sure no interrupt is enabled for the trace export endpoint, to prevent any software intervention during the (steady-state) transmission.
4. Configure the linked loop of TRBs as described in Section 23.11.4.11.1, *Trace export requirements*, and write-protect them against the USB controller's DMA
5. Start the transfer by linking to the first TRB of the loop.

Trace export steady-state (no software intervention)

1. Assuming that the dataflow pacing mentioned in the previous chapter is in place, the EP transmits data continuously.
2. Once a TRB is executed (that is, described trace data has been transmitted over USB), the DMA updates it by clearing the Hardware Owner (HWO) bit to 0, to hand it back to the software driver.
3. The TRB write fails silently, that is, HWO remains 1
4. When the DMA loops the TRB loop and reloads the same TRB, it is executed again, as if it had been refreshed by the software driver.

Stopping the trace export

- Done by ending the USB transfer by software. One possible method is to clear one of the HWO bits to 0, which will cause the list processor to stop when it reaches that point.

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23.11.4.12 Observability Debug Interface

The USBOTGSS_DEBUG_DATA register and the 32-bit debug_data output signal (to the device debug subsystem) allow observation of a selection of signals that are not otherwise available at the system boundary (device pads). The mode is controlled by the USBOTGSS_DEBUG_CFG and USBOTGSS_GDBGLSPMUX registers. By default, the observability system is in mode 0 and all bits of USBOTGSS_DEBUG_DATA are consequently tied low (= 0).

Table below summarizes the different modes.

Table 23-1108. DEBUG_DATA observability modes summary

USBOTGSS_DEBUG_CFG[2:0] SEL	USBOTGSS_GDBGLSPMUX[21:16] TRACEPORTMUXSEL	USBOTGSS_DEBUG_DATA
0x0	don't care	all-0
0x1	don't care	UTMI signals (see table below)
0x2	don't care	PIPE signals (see table below)
0x3	don't care	CORE signals (see table below)
0x4 or 0x5	0x3F	all-0
0x4	n	Trace vector n, lower 32 bits
0x5	n	Trace vector n, upper 32 bits

Tables below contain a bit-by-bit description of modes 1, 2 and 3. The value of the trace vector visible through mode 4 and 5 may change depending on the controller core version, and are not documented here.

Table 23-1109. Configurations Of Observability Output

Bit	USBOTGSS_DEBUG_CFG[2:0] SEL = 0x1	USBOTGSS_DEBUG_CFG[2:0] SEL = 0x2	USBOTGSS_DEBUG_CFG[2:0] SEL = 0x3
0	utmi_clk	pipe_txpclk_out	core_ltdb_substate[0](1)
1	utmi_databus16_8	pipe_txdatak[0]	core_ltdb_substate[1](1)
2	utmi_txvalid	pipe_txdatak[1]	core_ltdb_substate[2](1)
3	utmi_txvalidh	pipe_txdatak[2]	core_ltdb_substate[3](1)
4	utmi_txready	pipe_txdatak[3]	core_ltdb_link_state[0](1)
5	utmi_rxactive	pipe_elasticitybuffermode	core_ltdb_link_state[1](1)
6	utmi_rxvalid	pipe_txdetectrxloopback	core_ltdb_link_state[2](1)
7	utmi_rxvalidh	pipe_txelecidle	core_ltdb_link_state[3](1)
8	utmi_rxerror	pipe_txoneszeros	debug_mclk_usof_number[0](2)
9	utmi_reset	pipe_rxpolarity	core_gsts_buserraddvld
10	utmi_l1_suspend_com_n	pipe_rxeqtraining	core_u2_prt_state[0](3)
11	utmi_xcvrselect[0]	pipe_reset_n	core_u2_prt_state[1](3)
12	utmi_xcvrselect[1]	pipe_powerdown[0]	core_u2_prt_state[2](3)
13	utmi_termselect	pipe_powerdown[1]	core_u2_prt_state[3](3)
14	utmi_opmode[0]	pipe_txdeemph[0]	core_u2_prt_state[4](3)
15	utmi_opmode[1]	pipe_txdeemph[1]	core_u2mac_txrx_state_0[0](4)
16	utmi_linestate[0]	pipe_txmargin[0]	core_u2mac_txrx_state_0[1](4)
17	utmi_linestate[1]	pipe_txmargin[1]	core_u2mac_txrx_state_0[2](4)
18	utmi_idpullup	pipe_txmargin[2]	core_u2mac_txrx_state_0[3](4)
19	utmi_dppulldown	pipe_txswing	core_u2mac_txrx_state_0[4](4)
20	utmi_dmpulldown	pipe_rxtermination	core_u2mac_txrx_state_1[0](4)
21	utmi_drvvbus	pipe_rxpclk	core_u2mac_txrx_state_1[1](4)

(1) See Table 23-1110
(2) Only the LSB of the micro-SOF number is visible, which toggles every microframe (125 µs).
(3) See Table 23-1111.
(4) See Table 23-1112.

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Table 23-1109. Configurations Of Observability Output (continued)

Bit	USBOTGSS_DEBUG_CFG[2:0] SEL = 0x1	USBOTGSS_DEBUG_CFG[2:0] SEL = 0x2	USBOTGSS_DEBUG_CFG[2:0] SEL = 0x3
22	utmi_chrgvbus	pipe_rxdatak[0]	core_u2mac_txrx_state_1[2](4)
23	utmi_dischrgvbus	pipe_rxdatak[1]	core_u2mac_txrx_state_1[3](4)
24	utmi_txbitstuffenable	pipe_rxdatak[2]	core_u2mac_txrx_state_1[4](4)
25	utmi_txbitstuffenableh	pipe_rxdatak[3]	core_u2_dssr_state[0](5)
26	utmi_hostdisconnect	pipe_rxvalid	core_u2_dssr_state[1](5)
27	utmi_iddig	pipe_phystatus	core_u2_dssr_state[2](5)
28	utmi_avalid	pipe_elecidle	core_u2_dssr_state[3](5)
29	utmi_bvalid	pipe_rxstatus[0]	core_suspend_com_n
30	utmi_vbusvalid	pipe_rxstatus[1]	core_suspend_n
31	utmi_sessend	pipe_rxstatus[2]	core_sm2bl_cur_mode(6)

(5) See Table 23-1113.
(6) See Table 23-1114.

Table 23-1110 shows the encoding used for the link training SuperSpeed state machine (LTSSM) state (ltdb_link_state, 4 bit) and substate (ltdb_substate, 4 bit), which is available in the core observability mode as shown in Table 23-1109. The state and substate are also visible to the software in the USBOTGSS_GDBGLTSSM register. The substate can only be decoded relatively to the state (that is, all 8 bits must be decoded together). There are more substates in the current implementation than there are LTSSM substates defined by the standard (see *Universal Serial Bus Revision 3.0 Specification)*, because the implementation is finer grained than the standard. Table 23-1110 describes the relationship.

Table 23-1110. LTSSM State/Substate Encoding

core_ltdb_link_state[3:0]	core_ltdb_substate[3:0]	LTSSM State	LTSSM Substate	Implementation-Specific Substate Name	Description
0x0	x	U0	N/A	U0	U0: No substate
0x1	0x0	U1		U1_POWER	PHY power state P0-P1 request
0x1	0x1	U1		U1_POWER_A	Wait for PHY power change done
0x1	0x2	U1		U1_ACTIVE	Wait for remote/local U1 exit
0x1	0x3	U1		U1_EXIT_LOC_RESP	Start U1 exit and wait for min response from remote partner
0x1	0x4	U1		U1_EXIT_LOC_FIN	Locally initiated U1 exit
0x1	0x5	U1		U1_EXIT_REM	Remote initiated U1 exit
0x1	0x6	U1		U1_EXIT_P0	PHY power state P1-P0 request
0x1	0x7	U1		U1_EXIT_P0_A	Wait for PHY power change P1-P0 done
0x1	0x8	U1		U1_EXIT_DONE	U1 exit successful U1-Recovery
0x2	0x0	U2		U2_POWER	PHY power state P0-P2 request
0x2	0x1	U2		U2_POWER2	Wait for PHY power change done
0x2	0x2	U2		U2_ACTIVE	Wait for remote/local U2 exit
0x2	0x3	U2		U2_ACTIVE_0	Request to start receiver detection
0x2	0x4	U2		U2_ACTIVE_1	Wait for receiver detection response
0x2	0x5	U2		U2_EXIT_LOC_RESP	Start U2 exit and wait for minimum response from remote partner
0x2	0x6	U2		U2_EXIT_LOC_FIN	Locally initiated U2 exit
0x2	0x7	U2		U2_EXIT_REM	Remote initiated U2 exit
0x2	0x8	U2		U2_EXIT_P0	PHY power state P2–P0 request

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Table 23-1110. LTSSM State/Substate Encoding (continued)

core_ltdb_link_state[3:0]	core_ltdb_substate[3:0]	LTSSM State	LTSSM Substate	Implementation-Specific Substate Name	Description
0x2	0x9	U2		U2_EXIT_P0_A	Wait for PHY power change P1-P0 done
0x2	0xA	U2		U2_EXIT_DONE	U2 exit successful U2-Recovery
0x3	0x0	U3		U3_POWER	PHY power state P0-P2/P3 request
0x3	0x1	U3		U3_POWER3	Wait for PHY power change done
0x3	0x2	U3		U3_ACTIVE	Wait for remote/local U3 exit
0x3	0x3	U3		U3_ACTIVE_0	Request to start receiver detection
0x3	0x4	U3		U3_ACTIVE_1	Wait for receiver detection response
0x3	0x5	U3		U3_EXIT_LOC_POW	PHY power state P3-P0-P2 request
0x3	0x6	U3		U3_EXIT_LOC_POW_A	Wait for PHY power change done
0x3	0x7	U3		U3_EXIT_LOC_RESP	Start U3 exit and wait for minimum response from remote partner
0x3	0x8	U3		U3_EXIT_LOC_FIN	Locally initiated U3 exit
0x3	0x9	U3		U3_EXIT_REM_POW	PHY Power state P3-P0-P2 request
0x3	0xA	U3		U3_EXIT_REM_POW_A	Wait for PHY power change done
0x3	0xB	U3		U3_EXIT_REM	Remote initiated U3 exit
0x3	0xC	U3		U3_EXIT_P0	PHY power state P2/P3-P0 request
0x3	0xD	U3		U3_EXIT_P0_A	Wait for PHY power change P2/P3-P0 done
0x3	0xE	U3		U3_EXIT	Received remote/local U3 exit
0x3	0xF	U3		U3_EXIT_DONE	U3 exit successfu lU3-Recovery
0x4	0x0	SS.Disabled		SSD_POWER3	PHY power state P2/P3 request
0x4	0x1	SS.Disabled		SSD_POWER3A	Wait for PHY power change done
0x4	0x2	SS.Disabled		SSD_MAIN	Wait for RUN/STOP bit
0x5	0x0	Rx.Detect		RXD_INIT	PHY power state P2 request
0x5	0x1	Rx.Detect		RXD_POWER2	Wait for PHY power change done
0x5	0x2	Rx.Detect	Reset	RXD_RESET	Warm reset
0x5	0x3	Rx.Detect	Reset	RXD_RESET_T	Wait for RUN/STOP bit (device mode)
0x5	0x4	Rx.Detect	Active	RXD_ACTIVE0	Request to start receiver detection
0x5	0x5	Rx.Detect	Active	RXD_ACTIVE1	Wait for receiver detection response
0x5	0x6	Rx.Detect	Quiet	RXD_QUIET	wait for 12-ms timer timeout
0x6	0x0	SS.Inactive		SSI_RESET	PHY power state P0-P2 request
0x6	0x1	SS.Inactive		SSI_POWER2	Wait for PHY power change done
0x6	0x2	SS.Inactive	Quiet	SSI_QUIET0	Start 12-ms timer
0x6	0x3	SS.Inactive	Quiet	SSI_QUIET1	Wait for 12-ms timer timeout
0x6	0x4	SS.Inactive	Disconnect.Detect	SSI_DIS_DET0	Request to start receiver detection

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Table 23-1110. LTSSM State/Substate Encoding (continued)

core_ltdb_link_state[3:0]	core_ltdb_substate[3:0]	LTSSM State	LTSSM Substate	Implementation-Specific Substate Name	Description
0x6	0x5	SS.Inactive	Disconnect.Detect	SSI_DIS_DET1	Wait for receiver detection response
0x7	0x0	Polling		POLL_RESET	PHY power state P0 request
0x7	0x1	Polling		POLL_POWER0	Wait for PHY power change done
0x7	0x2	Polling	LFPS	POLL_LFPS	Send/receive Poll.LFPS
0x7	0x3	Polling	RxEQ	POLL_RXEQ	Send/receive TSEQ training set
0x7	0x4	Polling	Active	POLL_ACTIVE	Send/receive TS1 training set
0x7	0x5	Polling	Configuration	POLL_CONFIG	Send/receive TS2 training set
0x7	0x6	Polling	Idle	POLL_IDLE	Send/receive logical IDLE symbols
0x8	0x0	Recovery		RECOV_RESET	PHY power state P0 request
0x8	0x1	Recovery		RECOV_POWER0	Wait for PHY power change done
0x8	0x2	Recovery	Active	RECOV_ACTIVE	Send/receive TS1 training set
0x8	0x3	Recovery	Configuration	RECOV_CONFIG	Send/receive TS2 training set
0x8	0x4	Recovery	Idle	RECOV_IDLE	Send/receive logical IDLE symbols
0x9	0x0	Hot Reset		HRESET_RST	Request TCRRL to send TS2
0x9	0x1	Hot Reset		HRESET_GO	Start 12-ms timer
0x9	0x2	Hot Reset	Active	HRESET_ACT1	Send/receive TS1 training set with reset bit
0x9	0x3	Hot Reset	Active	HRESET_ACT2	Send/receive TS1 training set without reset bit
0x9	0x4	Hot Reset	Exit	HRESET_EXIT	Send/receive logical IDLE symbols
0xA	x	Compliance Mode	N/A	N/A	N/A
0xB	0x0	Loopback	Active	LPBK_IDLE	Wait for loopback start request
0xB	0x1	Loopback	Active	LPBK_MASTER	Master mode: Wait for loopback exit request
0xB	0x2	Loopback	Active	LPBK_SLAVE	Slave mode: Wait for loopback exit request
0xB	0x3	Loopback	Exit	LPBK_EXIT_LOC_RESP	Start loopback exit and wait for minimum response from remote partner
0xB	0x4	Loopback	Exit	LPBK_EXIT_LOC_FIN	Locally initiated loopback exit
0xB	0x5	Loopback	Exit	LPBK_EXIT_REM	Remote initiated loopback exit

Table 23-1111 to Table 23-1114 show the encoding used for various, nonstandard core observability fields.

The USB2 port described in Table 23-1111 can be either in HS, FS, or LS mode, depending on the configuration and on the attached USB device.

Table 23-1111. USB2 Port State Encoding

core_u2_prt_state[4:0]	USB2 Port State
0x00	PRT_DISCON
0x01	DISABLE
0x02	FSLS_RESET
0x03	WAIT_CHIRP
0x04	Reserved

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Table 23-1111. USB2 Port State Encoding (continued)

core_u2_prt_state[4:0]	USB2 Port State
0x05	DEV_CHIRP
0x06	HST_CHIRP_J
0x07	HST_CHIRP_K
0x08	HST_CHIRP_END
0x09	ENABLE
0x0A	AEOF
0x0B	SOF
0x0C	SUSPEND
0x0D	RESUME
0x0E	RESUME_END
0x0F	RESUME_DONE
0x10	TEST_PKT
0x11	PRE_ENABLE
0x12	SOF_END
0x13	TEST
0x14	Reserved
0x15	HST_CHIRP_DONE

The USB controller includes two USB2 media access controller (MAC) instances. Table 23-1112 describes their state. In the current single-port architecture, only one can be operational at a time.

- MAC 0 (core_u2mac_txrx_state_0[4:0]) is the FS/LS instance.
- MAC 1 (core_u2mac_txrx_state_1[4:0]) is the HS instance.

Table 23-1112. USB2 MAC State Encoding

core_u2mac_txrx_state_X[4:0](1)	USB2 MAC State	Note
0x00	IDLE	
0x01	SEND_SPLT	Host mode only
0x02	TKN2TKN	Host mode only
0x03	SEND_CRC5	Host mode only
0x04	TKN2DAT	Host mode only
0x05	WAIT_DPKT	Device mode only
0x06	RECV_ERR	
0x07	RECV_DATA	
0x08	SEND_HSHK	
0x09	SEND_EOP	
0x0A	SEND_DATA	
0x0B	WAIT_HSHK	
0x0C	CHK_CRC16	
0x0D	WAIT_DATA	
0x0E	TESTMOD	Device mode only
0x0F	WAIT_BUSIDLE	
0x10	WAIT_TURNAROUND	Device mode only
0x11	DATA_TO_STS	
0x12	WAIT_EOP	Host mode only

(1) X = 0 or 1

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The USB controller includes a 4-bit device speed/suspend/resume (DSSR) submodule, the state of which is described in Table 23-1113.

Table 23-1113. USB2 DSSR State Encoding

core_u2_dssr_state[3:0]	USB2 Port State
0x00	DEV_INIT
0x01	DEV_IDLE
0x02	PULLUP_EN
0x03	CHK_BUS
0x04	SEND_CHIRP
0x05	WAIT_HST_CHIRP
0x06	SUSPENDED
0x07	RESUMING
0x08	FLS_RESET
0x09	DLINE_PULSING
0x0A	PULSING_DONE
0x0B	DEV_CHIRP_END
0x0C	DEV_CHIRP_DONE
0x0D	REMOTE_WAKEUP
0x0E	RMWAKEUP_DONE

Table 23-1114 shows the current USB role encoding.

Table 23-1114. Current Mode Encoding

core_sm2bl_cur_mode	Current USB Mode (Role)
0x0	USB host
0x1	USB device

23.11.4.13 USB Frame Synchronization

Some systems may require a timing reference synchronized with the USB frames/microframes, as set by the USB host. For example, a USB data streaming application may rely on two clocks generated on either side of the USB interface (one in the USB host, the other in the USB device), and locked over the USB.

For that purpose, the controller generates two timing reference outputs

- SYNC_USOF_ITP_CLK: microframe/ITP LSbit count which toggles at every (125 us-long) HS/SS micro-frame boundary, that is, 8000 transitions per seconds or a 4-kHz square clock
- SYNC_SOF_CLK: frame LSbit count which toggles every (1 ms-long) FS/LS frame, that is, 1000 transitions per seconds or a 0.5-kHz square clock.

The USB protocol defines different bus timing reference depending on the role and speed:

- The timing master is by definition always the USB host, which broadcasts the LSKA/SOF/uSOF/ITP. The USB device, which receives those signals, is the timing slave.
- The reference can only be maintained if the device is receiving the required signals, that is, if it is not suspended (in USB2) or out of U0 (in USB3)
- In low-speed (LS, 1.5 Mbit/s), the host sends an SE0 "Low-Speed Keep-Alive" (LSKA) pulse every 1 ms (frame). Traffic stops before the frame's end and ensures that the LSKA pulse is sent at the exact time. However, note that the current controller is never a LS device (only a LS host): synchronization to the LSKA is not required.
- In full-speed (FS, 12 Mbit/s), the host sends a Start-Of-Frame (SOF) FS packet every 1 ms (frame), containing an frame number incremented by 1 each time. Traffic stops before the frame's end to ensure that the SOF FS packet is sent at the exact time.
- In high-speed (HS, 480 Mbit/s), the host sends a Start-Of-Frame (SOF) packet every 125 us

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(microframe), containing a frame number. The same frame number is repeated 8 times, then incremented by 1, etc… (1 frame = 8 micro-frames). Traffic stops before the frame's end to ensure that the SOF HS packet is sent at the exact time.

- In super-speed (SS, 5 Gbit/s), the host send a Isochronous Timestamp Packet (ITP) within each 125 us microframe, containing an ITP number incremented by 1 every microframe. The ITP is not send at exact intervals, but includes a field giving the packet's delay with respect to the ideal microframe boundary. This allows the USB device to resynchronize.

NOTE:

- The reference clock for the sync signals is:
  - The 125-MHz PIPE clock when in SS USB3 device mode
  - The 60-MHz UTMI/ULPI clock (USB_OTG_SS_FCLK) when in HS/FS USB2 device mode
  - The 60-MHz UTMI/ULPI clock (USB_OTG_SS_FCLK) when in host mode (any speed, including SS)
- In case of missing/corrupted SOF/ITP, the device still toggles the sync outputs, after a delay:
  - 128 ns after the expected microframe start in SS USB3 device
  - 200 ns after the expected microframe start in HS USB2 device
  - 3.5 us after the expected frame start in FS USB2 device
- In a FS device, only the frame sync (SYNC_SOF_CLK) toggles. The micro-frame sync (SYNC_USOF_ITP_CLK) is tied to 0.
- In a HS/SS device, both syncs toggle.
- The micro-frame sync SYNC_USOF_ITP_CLK is also available on the debug port (See Section 23.11.4.12, *Observability Debug Interface*).

23.11.4.14 Memory Map

The 128-KiB (17-bit address) address space of the USB SS controller module is split into three main blocks (see Figure 23-245):

- Wrapper registers: Contain the TI-specific registers, including the top-level interrupt management, power management, etc.
- Core registers (static mapping): Provide access to the core functional status and control registers.
- Core debug access (programmable, paged mapping): Provides access to the entire memory space of the core, which is much larger than the core registers. Designed to access the core buffer RAMs, remapped in memory for debug (read/write) access.

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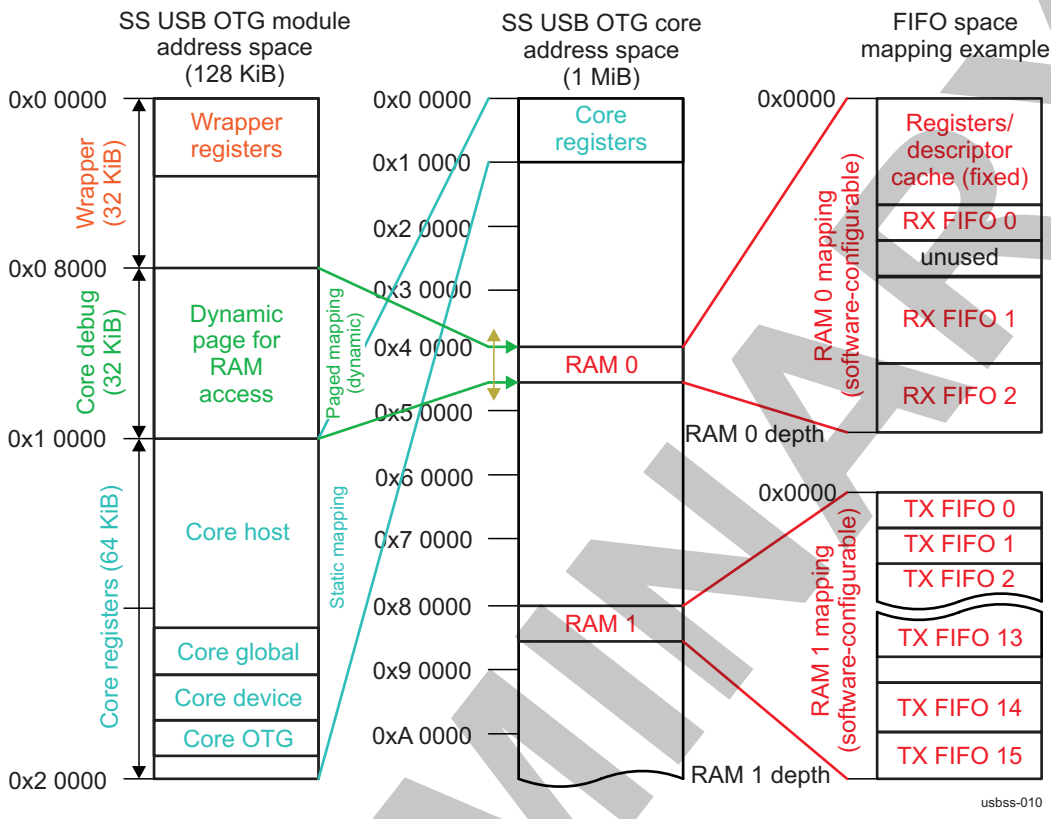
Figure 23-245. Module Vs Core Vs RAM Address Spaces And Mapping



23.11.4.14.1 Core Space Remapping

Unless otherwise specified, all offsets mentioned in this chapter are USB byte offsets of the controller module memory space or simply module offsets. However, the logic core embedded within the module also has its own memory space (with core offsets) and each FIFO can also be configured within its respective RAMs using FIFO configuration offsets.

The core space (1 MiB) is remapped within the (128 KiB) address space of the module, as shown in Figure 23-245. All functional registers of the core are located inside a single 64 KiB block and statically remapped inside the core register block of the subsystem (0x1 0000 to 0x1 FFFC). Normal operation does not require access to the rest of core's memory space.

The core memory space also contains the two internal RAM buffers (RAM0 and RAM1). The RAMs contain data and descriptor cache (read out of or written to main memory by the built-in DMA of controller) as well as some register fields (accessed by software through the core register block). The RAM content is accessed for debug purposes only and never directly during normal operation.

The data cache is composed of a number of TX and RX FIFOs mapped in RAM1 and RAM0, respectively. The mapping of each FIFO is programmable through the USBOTGSS_GTXFIFOSIZ0 through USBOTGSS_GRXFIFOSIZ15 and USBOTGSS_GRXFIFOSIZ0 through USBOTGSS_GRXFIFOSIZ2 registers by a base address/FIFO depth configuration pair. Both parameters are expressed in FIFO config physical addresses (that is, 64-bit word addresses) with the RAM base at address 0x0. Software must ensure that FIFOs are within the implemented RAM size, do not overlap each other, and do not encroach on the register/descriptor cache (lower addresses of RAM0)

The core memory space can be accessed by pages of 32 KiB each. Each of the 32 pages can be dynamically mapped to the core debug block of the module (0x0 8000 to 0x0 FFFC) by programming the USBOTGSS_MMRAM_OFFSET register. Each RAM is smaller than 32 KiB (or 4 K × 64-bit words) and fits inside a single page.

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NOTE: The core registers (mapped statically) can also be accessed in paged mode, but this feature is only a side effect of paging and must not be used.

Table 23-1115 summarizes the offsets of the structures visible in the (paged) core debug block:

- Core offset column: The byte offset of the structure within the 1-Mbyte core address space
- Page offset (OFFSET_MSB) column: The 32 K page offset of the structure within the core address space, with between parentheses the value of the 5-bit register field USBOTGSS_MMRAM_OFFSET[19:15] OFFSET_MSB.
- Module offset column: Byte offset at which the structure is visible from outside the USB3 subsystem, for the page offset indicated.
- FIFO base parameters are the byte base address of the FIFO structure with respect to the RAM base. FIFO base parameters are software programmable.
- FIFO size parameters are the size of the FIFO structure in bytes. FIFO size parameters are software programmable.
- RAM base/size are the hardcoded byte base address and size in bytes of the RAM structures.
- Cache base/size are the hardcoded byte base address and size in bytes of the descriptor-cache-register-storage structures.

Table 23-1115. Address Offsets Of Memory-Mapped Structures Within Core Debug Block

Memory-Mapped Structure	Core Offset	Page Offset (OFFSET_MSB)	Module Offset
Low core registers, base	0x0 0000	0x0 0000 (0x00)	0x8000
Low core registers, top	0x0 7FFF	0x0 0000 (0x00)	0xFFFF
High core registers, base	0x0 8000	0x0 8000 (0x01)	0x8000
High core registers, top	0x0 FFFF	0x0 8000 (0x01)	0xFFFF
RAM0 base	0x4 0000	0x4 0000 (0x08)	0x8000
RAM0 top	0x4 0000 + (RAM size - 1)	0x4 0000 (0x08)	0x8000 + (RAM size - 1)
Registers/descriptor cache base	0x4 0000	0x4 0000 (0x08)	0x8000
Registers/descriptor cache top	0x4 0000 + (cache size)	0x4 0000 (0x08)	0x8000 + (cache size)
RX FIFO base	0x4 0000 + (FIFO base)	0x4 0000 (0x08)	0x8000 + (FIFO base)
RX FIFO top	0x4 0000 + (FIFO base + FIFO size - 1)	0x4 0000 (0x08)	0x8000 + (FIFO base + FIFO size - 1)
RAM1 base	0x8 0000	0x8 0000 (0x10)	0x8000
RAM1 top	0x8 0000 + (RAM size - 1)	0x8 0000 (0x10)	0x8000 + (RAM size - 1)
TX FIFO base	0x8 0000 + (FIFO base)	0x8 0000 (0x10)	0x8000 + (FIFO base)
TX FIFO top	0x8 0000 + (FIFO base + FIFO size - 1)	0x8 0000 (0x10)	0x8000 + (FIFO base + FIFO size - 1)

Table 23-1116 lists the parameters used in Table 23-1115 and how they are calculated. All values can be retrieved by software from register bitfields. When the bitfield is read-only, the parameter (for example, RAM sizes) is fixed (that is, hardwired). When the bitfield is writable, the parameter is programmable by software. The ×8 mutiplication factor is a consequence of the 64-bit RAM physical addressing.

Table 23-1116. Parameters For Memory-Mapped Structures Offset Calculation

Parameter	Register Bitfield Value (Byte Address/Size)	Type
RAM0 size	8 × USBOTGSS_GHWPARAMS6[31:16] DWC_USB3_RAM0_DEPTH	R
RAM1 size	8 × USBOTGSS_GHWPARAMS7[15:0] DWC_USB3_RAM1_DEPTH	R
Descriptor cache size (in RAM0)	8 × USBOTGSS_GHWPARAMS8[31:0] USBOTGSS_DWC_USB3_DCACHE_DEPTH_INFO	R

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Table 23-1116. Parameters For Memory-Mapped Structures Offset Calculation (continued)

Parameter	Register Bitfield Value (Byte Address/Size)	Type
RX FIFO m base (in RAM0) (1)	8 × USBOTGSS_GRXFIFOSIZ0[31:16] RXFSTADDR through USBOTGSS_GRXFIFOSIZ2[31:16] RXFSTADDR	R/W
RX FIFO m size (in RAM0)(1)	8 × USBOTGSS_GRXFIFOSIZ0[15:0] RXFDEP through USBOTGSS_GRXFIFOSIZ2[15:0] RXFDEP	R/W
TX FIFO n base (in RAM1)(2)	8 × USBOTGSS_GTXFIFOSIZ0[31:16] TXFSTADDR through USBOTGSS_GTXFIFOSIZ15[31:16] TXFSTADDR	R/W
TX FIFO n size (in RAM1)(2)	8 × USBOTGSS_GTXFIFOSIZ0[15:0] TXFDEP through USBOTGSS_GTXFIFOSIZ15[15:0] TXFDEP	R/W

(1) m = 0 to 2
(2) n = 0 to 15

23.11.4.14.2 xHCI Host Mapping

The core host block is subdivided based on the *eXtensible Host Controller Interface for USB (xHCI)* specification, with subblocks mapped at specified offsets of the core host base. Table 23-1117 summarizes the offset of each block.

The constant offset primitives are:

- Host offset = 0x1 0000
- CAPLENGTH = 0x20 (readable from hardwired USBOTGSS_CAPLENGTH[7:0] CAPLENGTH register bitfield)
- RTSOFF = 0x440 (readable from hardwired USBOTGSS_RTSOFF[31:0] register)
- DBOFF = 0x480 (readable from hardwired USBOTGSS_DBOFF[31:0] register)
- xECP × 4 = 0x220 × 4 (readable from the hardwired USBOTGSS_HCCPARAMS[31:16] XECP register bitfield)

Table 23-1117. xHCI Host Register Block Offsets

Register Block Name	Block Offset Definition	Block Offset Value	Bottom Register In Block
Capability registers	Host offset	0x1 0000	USBOTGSS_CAPLENGTH
Operational registers	Host offset + CAPLENGTH	0x1 0020	USBOTGSS_USBCMD
Runtime registers	Host offset + RTSOFF	0x1 0440	USBOTGSS_MFINDEX
Doorbell registers	Host offset + DBOFF	0x1 0480	USBOTGSS_DB_j (j =0)
Extended capability registers	Host offset + (xECP × 4)	0x1 0880	USBOTGSS_USBLEGSUP

23.11.4.15 USB2PHY

The device-embedded USB2.0 physical layer (USB2PHY) contains the USB functions, drivers, receivers, and pads for correct D+/D– signaling, and the battery charger detection (supporting dead-battery mode). Delivers a 3.3-V output signal (charger enable [pin usbphy_ce]) to control an external battery charger. It also contains LDO and bandgap to provide voltage reference.

The embedded PHY does not support the OTG features of USB-OTG standards (that is, ID pin detection and VBUS detection). This function is exported to an external companion chip (for example, the TWL6035). See details in Section 23.11.4.5.1, *Mailbox VBUS/ID Management*

The following USB2PHY signal is routed internally to the GPIO module pin to generate interrupts when any of the following events occur:

- CHGDETECTED: This signal indicates the output of the charger detection protocol.

  0: Charger not detected

  1: Charger detected

  The value is latched until the charger protocol is reset.

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For information about how to enable this interrupt, see Section 25.1, *General-Purpose Interface*.

23.11.5 USBOTGSS Register Manual

23.11.5.1 USBOTGSS Instance Summary

Table 23-1118. USBSS Instance Summary

Module Name	Module Base Address	Size
USBOTGSS_WRAPPER	0x4A02 0000	64 KiB
DWC_USB3	0x4A03 0000	64 KiB
USB2PHY	0x4A08 4000	124 Bytes

NOTE: For OCP2SCP1, see the OCP2SCP1 register manual in Chapter 27, *Shared PHY Component Subsystems*.

23.11.5.2 DWC_USB3 registers

23.11.5.2.1 DWC_USB3 Register Summary

Table 23-1119. DWC_USB3 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
USBOTGSS_CAPLENGTH	R	32	0x0000 0000	0x4A03 0000
USBOTGSS_HCSPARAMS1	R	32	0x0000 0004	0x4A03 0004
USBOTGSS_HCSPARAMS2	R	32	0x0000 0008	0x4A03 0008
USBOTGSS_HCSPARAMS3	R	32	0x0000 000C	0x4A03 000C
USBOTGSS_HCCPARAMS	R	32	0x0000 0010	0x4A03 0010
USBOTGSS_DBOFF	R	32	0x0000 0014	0x4A03 0014
USBOTGSS_RTSOFF	R	32	0x0000 0018	0x4A03 0018
USBOTGSS_USBCMD	RW	32	0x0000 0020	0x4A03 0020
USBOTGSS_USBSTS	RW	32	0x0000 0024	0x4A03 0024
USBOTGSS_PAGESIZE	R	32	0x0000 0028	0x4A03 0028
USBOTGSS_DNCTRL	RW	32	0x0000 0034	0x4A03 0034
USBOTGSS_CRCR_LO	RW	32	0x0000 0038	0x4A03 0038
USBOTGSS_CRCR_HI	RW	32	0x0000 003C	0x4A03 003C
USBOTGSS_DCBAAP_LO	RW	32	0x0000 0050	0x4A03 0050
USBOTGSS_DCBAAP_HI	RW	32	0x0000 0054	0x4A03 0054
USBOTGSS_CONFIG	RW	32	0x0000 0058	0x4A03 0058
USBOTGSS_PORTSC1	RW	32	0x0000 0420	0x4A03 0420
USBOTGSS_PORTPMSC1	RW	32	0x0000 0424	0x4A03 0424
USBOTGSS_PORTLI1	R	32	0x0000 0428	0x4A03 0428
USBOTGSS_PORTHLPMC1	RW	32	0x0000 042C	0x4A03 042C
USBOTGSS_PORTSC2	RW	32	0x0000 0430	0x4A03 0430
USBOTGSS_PORTPMSC2	RW	32	0x0000 0434	0x4A03 0434
USBOTGSS_PORTLI2	R	32	0x0000 0438	0x4A03 0438
USBOTGSS_PORTHLPMC2	R	32	0x0000 043C	0x4A03 043C
USBOTGSS_MFINDEX	R	32	0x0000 0440	0x4A03 0440
USBOTGSS_IMAN	RW	32	0x0000 0460	0x4A03 0460

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Table 23-1119. DWC_USB3 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
USBOTGSS_IMOD	RW	32	0x0000 0464	0x4A03 0464
USBOTGSS_ERSTSZ	RW	32	0x0000 0468	0x4A03 0468
USBOTGSS_ERSTBA_LO	RW	32	0x0000 0470	0x4A03 0470
USBOTGSS_ERSTBA_HI	RW	32	0x0000 0474	0x4A03 0474
USBOTGSS_ERDP_LO	RW	32	0x0000 0478	0x4A03 0478
USBOTGSS_ERDP_HI	RW	32	0x0000 047C	0x4A03 047C
USBOTGSS_DB_j (1)	RW	32	0x0000 0480 + (0x4 * j)	0x4A03 0480 + (0x4 * j)
USBOTGSS_USBLEGSUP	RW	32	0x0000 0880	0x4A03 0880
USBOTGSS_USBLEGCTLSTS	RW	32	0x0000 0884	0x4A03 0884
USBOTGSS_SUPTPRT2_DW0	R	32	0x0000 0890	0x4A03 0890
USBOTGSS_SUPTPRT2_DW1	R	32	0x0000 0894	0x4A03 0894
USBOTGSS_SUPTPRT2_DW2	R	32	0x0000 0898	0x4A03 0898
USBOTGSS_SUPTPRT2_DW3	R	32	0x0000 089C	0x4A03 089C
USBOTGSS_SUPTPRT3_DW0	R	32	0x0000 08A0	0x4A03 08A0
USBOTGSS_SUPTPRT3_DW1	R	32	0x0000 08A4	0x4A03 08A4
USBOTGSS_SUPTPRT3_DW2	R	32	0x0000 08A8	0x4A03 08A8
USBOTGSS_SUPTPRT3_DW3	R	32	0x0000 08AC	0x4A03 08AC
USBOTGSS_GSBUSCFG0	RW	32	0x0000 C100	0x4A03 C100
USBOTGSS_GSBUSCFG1	RW	32	0x0000 C104	0x4A03 C104
USBOTGSS_GTXTHRCFG	RW	32	0x0000 C108	0x4A03 C108
USBOTGSS_GRXTHRCFG	RW	32	0x0000 C10C	0x4A03 C10C
USBOTGSS_GCTL	RW	32	0x0000 C110	0x4A03 C110
USBOTGSS_GSTS	RW	32	0x0000 C118	0x4A03 C118
USBOTGSS_GSNPSID	R	32	0x0000 C120	0x4A03 C120
USBOTGSS_GGPIO	RW	32	0x0000 C124	0x4A03 C124
USBOTGSS_GUID	RW	32	0x0000 C128	0x4A03 C128
USBOTGSS_GUCTL	RW	32	0x0000 C12C	0x4A03 C12C
USBOTGSS_GBUSERRADDRLO	R	32	0x0000 C130	0x4A03 C130
USBOTGSS_GBUSERRADDRHI	R	32	0x0000 C134	0x4A03 C134
USBOTGSS_GPRTBIMAPLO	RW	32	0x0000 C138	0x4A03 C138
USBOTGSS_GPRTBIMAPHI	R	32	0x0000 C13C	0x4A03 C13C
USBOTGSS_GHWPARAMS0	R	32	0x0000 C140	0x4A03 C140
USBOTGSS_GHWPARAMS1	R	32	0x0000 C144	0x4A03 C144
USBOTGSS_GHWPARAMS2	R	32	0x0000 C148	0x4A03 C148
USBOTGSS_GHWPARAMS3	R	32	0x0000 C14C	0x4A03 C14C
USBOTGSS_GHWPARAMS4	R	32	0x0000 C150	0x4A03 C150
USBOTGSS_GHWPARAMS5	R	32	0x0000 C154	0x4A03 C154
USBOTGSS_GHWPARAMS6	R	32	0x0000 C158	0x4A03 C158
USBOTGSS_GHWPARAMS7	R	32	0x0000 C15C	0x4A03 C15C
USBOTGSS_GDBGFIFOSPACE	RW	32	0x0000 C160	0x4A03 C160
USBOTGSS_GDBGLTSSM	R	32	0x0000 C164	0x4A03 C164
USBOTGSS_GDBGLSPMUX	RW	32	0x0000 C170	0x4A03 C170
USBOTGSS_GDBGLSP	R	32	0x0000 C174	0x4A03 C174
USBOTGSS_GDBGEPINFO0	R	32	0x0000 C178	0x4A03 C178
USBOTGSS_GDBGEPINFO1	R	32	0x0000 C17C	0x4A03 C17C

(1) j = 0 to 63

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Table 23-1119. DWC_USB3 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
USBOTGSS_GPRTBIMAP_HSLO	RW	32	0x0000 C180	0x4A03 C180
USBOTGSS_GPRTBIMAP_HSHI	R	32	0x0000 C184	0x4A03 C184
USBOTGSS_GPRTBIMAP_FSLO	RW	32	0x0000 C188	0x4A03 C188
USBOTGSS_GPRTBIMAP_FSHI	R	32	0x0000 C18C	0x4A03 C18C
USBOTGSS_GUSB2PHYCFG	RW	32	0x0000 C200	0x4A03 C200
USBOTGSS_GUSB2PHYACC	RW	32	0x0000 C280	0x4A03 C280
USBOTGSS_GUSB3PIPECTL	RW	32	0x0000 C2C0	0x4A03 C2C0
USBOTGSS_GTXFIFOSIZ0	RW	32	0x0000 C300	0x4A03 C300
USBOTGSS_GTXFIFOSIZ1	RW	32	0x0000 C304	0x4A03 C304
USBOTGSS_GTXFIFOSIZ2	RW	32	0x0000 C308	0x4A03 C308
USBOTGSS_GTXFIFOSIZ3	RW	32	0x0000 C30C	0x4A03 C30C
USBOTGSS_GTXFIFOSIZ4	RW	32	0x0000 C310	0x4A03 C310
USBOTGSS_GTXFIFOSIZ5	RW	32	0x0000 C314	0x4A03 C314
USBOTGSS_GTXFIFOSIZ6	RW	32	0x0000 C318	0x4A03 C318
USBOTGSS_GTXFIFOSIZ7	RW	32	0x0000 C31C	0x4A03 C31C
USBOTGSS_GTXFIFOSIZ8	RW	32	0x0000 C320	0x4A03 C320
USBOTGSS_GTXFIFOSIZ9	RW	32	0x0000 C324	0x4A03 C324
USBOTGSS_GTXFIFOSIZ10	RW	32	0x0000 C328	0x4A03 C328
USBOTGSS_GTXFIFOSIZ11	RW	32	0x0000 C32C	0x4A03 C32C
USBOTGSS_GTXFIFOSIZ12	RW	32	0x0000 C330	0x4A03 C330
USBOTGSS_GTXFIFOSIZ13	RW	32	0x0000 C334	0x4A03 C334
USBOTGSS_GTXFIFOSIZ14	RW	32	0x0000 C338	0x4A03 C338
USBOTGSS_GTXFIFOSIZ15	RW	32	0x0000 C33C	0x4A03 C33C
USBOTGSS_GRXFIFOSIZ0	RW	32	0x0000 C380	0x4A03 C380
USBOTGSS_GRXFIFOSIZ1	RW	32	0x0000 C384	0x4A03 C384
USBOTGSS_GRXFIFOSIZ2	RW	32	0x0000 C388	0x4A03 C388
USBOTGSS_GEVNTADRLO	RW	32	0x0000 C400	0x4A03 C400
USBOTGSS_GEVNTADRHI	RW	32	0x0000 C404	0x4A03 C404
USBOTGSS_GEVNTSIZ	RW	32	0x0000 C408	0x4A03 C408
USBOTGSS_GEVNTCOUNT	RW	32	0x0000 C40C	0x4A03 C40C
USBOTGSS_GHWPARAMS8	R	32	0x0000 C600	0x4A03 C600
USBOTGSS_GHWPARAMS9	R	32	0x0000 C604	0x4A03 C604
USBOTGSS_DCFG	RW	32	0x0000 C700	0x4A03 C700
USBOTGSS_DCTL	RW	32	0x0000 C704	0x4A03 C704
USBOTGSS_DEVTEN	RW	32	0x0000 C708	0x4A03 C708
USBOTGSS_DSTS	RW	32	0x0000 C70C	0x4A03 C70C
USBOTGSS_DGCMDPAR	RW	32	0x0000 C710	0x4A03 C710
USBOTGSS_DGCMD	RW	32	0x0000 C714	0x4A03 C714
USBOTGSS_DALEPENA	RW	32	0x0000 C720	0x4A03 C720
USBOTGSS_DEPCMDPAR2_i [(2)]	RW	32	0x0000 C800 + (0x10 * i)	0x4A03 C800 + (0x10 * i)
USBOTGSS_DEPCMDPAR1_i [(2)]	RW	32	0x0000 C804 + (0x10 * i)	0x4A03 C804 + (0x10 * i)
USBOTGSS_DEPCMDPAR0_i [(2)]	RW	32	0x0000 C808 + (0x10 * i)	0x4A03 C808 + (0x10 * i)
USBOTGSS_DEPCMD_i [(2)]	RW	32	0x0000 C80C + (0x10 * i)	0x4A03 C80C + (0x10 * i)
USBOTGSS_OCFG	RW	32	0x0000 CC00	0x4A03 CC00
USBOTGSS_OCTL	RW	32	0x0000 CC04	0x4A03 CC04

(2) i = 0 to 31

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Table 23-1119. DWC_USB3 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
USBOTGSS_OEVT	RW	32	0x0000 CC08	0x4A03 CC08
USBOTGSS_OEVTEN	RW	32	0x0000 CC0C	0x4A03 CC0C
USBOTGSS_OSTS	R	32	0x0000 CC10	0x4A03 CC10

23.11.5.2.2 DWC_USB3 Register Description

Table 23-1120. USBOTGSS_CAPLENGTH

Address Offset	0x0000 0000		
Physical Address	0x4A03 0000	**Instance**	DWC_USB3
Description	Capability registers length + host controller interface (HCI) version number		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HCIVERSION																RESERVED								CAPLENGTH							

Bits	Field Name	Description	Type	Reset
31:16	HCIVERSION	Host Controller Interface Version (xHCI), in BCD. Set by USBOTGSS_FLADJ[29] XHCI_REVISION field. Read 0x96: xHCI revision 0.96 Read 0x100: xHCI revision 1.0 + errata	R	0x0100
15:8	RESERVED		R	0x00
7:0	CAPLENGTH	Capability Register Length: length of the xHCI Capabilities registers bank, in bytes; also the offset of the xHCI Operational registers bank (starting with USBOTGSS_USBCMD), with respect to xHCI base (i.e. the current register)	R	0x20

Table 23-1121. Register Call Summary for Register USBOTGSS_CAPLENGTH

Super-Speed USB OTG Subsystem

- xHCI USB Host Software API: [0]
- xHCI Host Mapping: [1] [2]
- DWC_USB3 Register Summary: [3]
- DWC_USB3 Register Description: [4] [5]

Table 23-1122. USBOTGSS_HCSPARAMS1

Address Offset	0x0000 0004		
Physical Address	0x4A03 0004	**Instance**	DWC_USB3
Description	Host controller structural parameters 1 (xHCI)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXPORTS								RESERVED								MAXINTRS								MAXSLOTS							

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Bits	Field Name	Description	Type	Reset
31:24	MAXPORTS	See xHCI specification.	R	0x02
23:19	RESERVED		R	0x00
18:8	MAXINTRS	See xHCI specification.	R	0x001
7:0	MAXSLOTS	See xHCI specification.	R	0x40

Table 23-1123. Register Call Summary for Register USBOTGSS_HCSPARAMS1

Super-Speed USB OTG Subsystem

- xHCI USB Host Software API: [0] [1]
- DWC_USB3 Register Summary: [2]

Table 23-1124. USBOTGSS_HCSPARAMS2

Address Offset	0x0000 0008		
Physical Address	0x4A03 0008	**Instance**	DWC_USB3
Description	Host controller structural parameters 2 (xHCI)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXSCRATCHPADBUFS_LO					SPR	MAXSCRATCHPADBUFS_HI		RESERVED								RESERVED								ERSTMAX				IST			

Bits	Field Name	Description	Type	Reset
31:27	MAXSCRATCHPADBUFS_LO	Max Scratchpad Buffers, lower bits: See xHCI specification	R	0x01
26	SPR	Scratchpad Restore: See xHCI specification Read 0x1: Integrity of the scratchpad buffer required across power events Read 0x0: Scratchpad buffers may be freed and reallocated between power events	R	1
25:21	MAXSCRATCHPADBUFS_HI	Max Scratchpad Buffers, higher bits: see xHCI 1.0 standard	R	0x00
20:13	RESERVED		R	0x00
12:8	RESERVED		R	0x00
7:4	ERSTMAX	Event Ring Segment Table Max: See xHCI specification	R	0xF
3:0	IST	Isochronous Scheduling Threshold: See xHCI specification	R	0x1

Table 23-1125. Register Call Summary for Register USBOTGSS_HCSPARAMS2

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

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Table 23-1126. USBOTGSS_HCSPARAMS3

Address Offset	0x0000 000C		
Physical Address	0x4A03 000C	**Instance**	DWC_USB3
Description	Host controller structural parameters 3 (xHCI)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U2_DEVICE_EXIT_LAT																RESERVED								U1_DEVICE_EXIT_LAT							

Bits	Field Name	Description	Type	Reset
31:16	U2_DEVICE_EXIT_LAT	U2 device exit latency: Worst-case latency to transition from U2 to U0, in µs. Applies to all root hub ports. Read 0x7FF: Less than 2047 µs (maximum: Greater values are reserved.) Read 0x2: Less than 2 µs Read 0x1: Less than 1 µs Read 0x0: 0	R	0x07FF
15:8	RESERVED		R	0x00
7:0	U1_DEVICE_EXIT_LAT	U1 device exit latency: Worst-case latency to transition a root hub port link state (PLS) from U1 to U0, in µs. Read 0x2: Less than 2 µs Read 0x1: Less than 1 µs Read 0x0: 0 Read 0xA: Less than 10 µs (maximum: Greater values are reserved.)	R	0x0A

Table 23-1127. Register Call Summary for Register USBOTGSS_HCSPARAMS3

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1128. USBOTGSS_HCCPARAMS

Address Offset	0x0000 0010		
Physical Address	0x4A03 0010	**Instance**	DWC_USB3
Description	Host controller capability parameters (xHCI)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XECP																MAXPSASIZE				RESERVED			PAE	NSS	LTC	LHRC	PIND	PPC	CSZ	BNC	AC64

Bits	Field Name	Description	Type	Reset
31:16	XECP	xHCI Extended Capabilties Pointer. 32-bit dword offset, with respect to xHCI base, of the first item of the capability list.	R	0x0220
15:12	MAXPSASIZE	Maximum Primary Stream Array Size: See xHCI specification	R	0xF
11:9	RESERVED		R	0x0
8	PAE	Parse All Event data: see xHCI 1.0 standard w errata	R	0
7	NSS	No Secondary SID Support See xHCI specification	R	0

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Bits	Field Name	Description	Type	Reset
6	LTC	Latency Tolerance messaging Capability See xHCI specification	R	1
5	LHRC	Light HC Reset Capability: See xHCI specification	R	0
4	PIND	Port Indicators: See xHCI specification	R	0
3	PPC	Port Power Control: See xHCI specification	R	1
2	CSZ	Context Size: See xHCI specification	R	1
1	BNC	Bandwidth Negotiation Capability: See xHCI specification	R	0
0	AC64	64-bit Address Capability: See xHCI specification	R	0

Table 23-1129. Register Call Summary for Register USBOTGSS_HCCPARAMS

Super-Speed USB OTG Subsystem

- xHCI Host Mapping: [0]
- DWC_USB3 Register Summary: [1]

Table 23-1130. USBOTGSS_DBOFF

Address Offset	0x0000 0014		
Physical Address	0x4A03 0014	**Instance**	DWC_USB3
Description	Doorbell offset (xHCI): Byte offset of the doorbell register array (USBOTGSS_DB_j, with respect to the xHCI base (that is, USBOTGSS_CAPLENGTH register)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DOORBELL_ARRAY_OFFSET																														ZERO	

Bits	Field Name	Description	Type	Reset
31:2	DOORBELL_ARRAY_OFFSET	Byte address offset MSBs	R	0x0000 0120
1:0	ZERO	Byte address offset LSBs, always 0 (offset is 32-bit = 4-byte aligned)	R	0x0

Table 23-1131. Register Call Summary for Register USBOTGSS_DBOFF

Super-Speed USB OTG Subsystem

- xHCI Host Mapping: [0]
- DWC_USB3 Register Summary: [1]

Table 23-1132. USBOTGSS_RTSOFF

Address Offset	0x0000 0018		
Physical Address	0x4A03 0018	**Instance**	DWC_USB3
Description	RunTime space offset (xHCI): Byte offset of the runtime register bank (starting with USBOTGSS_MFINDEX), with respect to the xHCI base (that is, USBOTGSS_CAPLENGTH register)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RUNTIME_REG_SPACE_OFFSET																														ZERO	

Bits	Field Name	Description	Type	Reset
31:5	RUNTIME_REG_SPACE_OFFSET	Byte address offset MSBs	R	0x000 0022
4:0	ZERO	Byte address offset LSBs, always 0 (offset is 32-byte aligned)	R	0x00

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Table 23-1133. Register Call Summary for Register USBOTGSS_RTSOFF

Super-Speed USB OTG Subsystem

- xHCI Host Mapping: [0]
- DWC_USB3 Register Summary: [1]

Table 23-1134. USBOTGSS_USBCMD

Address Offset	0x0000 0020		
Physical Address	0x4A03 0020	**Instance**	DWC_USB3
Description	USB command register (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				EU3S	EWE	CRS	CSS	LHCRST	RESERVED			HSEE	INTE	HCRST	R_S

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11	EU3S	See xHCI specification.	RW	0
10	EWE	See xHCI specification.	RW	0
9	CRS	See xHCI specification.	RW	0
8	CSS	See xHCI specification.	RW	0
7	LHCRST	See xHCI specification.	RW	0
6:4	RESERVED		R	0x0
3	HSEE	See xHCI specification.	RW	0
2	INTE	See xHCI specification.	RW	0
1	HCRST	See xHCI specification.	RW	0
0	R_S	See xHCI specification.	RW	0

Table 23-1135. Register Call Summary for Register USBOTGSS_USBCMD

Super-Speed USB OTG Subsystem

- xHCI Host Mapping: [0]
- DWC_USB3 Register Summary: [1]
- DWC_USB3 Register Description: [2] [3] [4]

Table 23-1136. USBOTGSS_USBSTS

Address Offset	0x0000 0024		
Physical Address	0x4A03 0024	**Instance**	DWC_USB3
Description	USB status register (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HCE	CNR	SRE	RSS	SSS	RESERVED			PCD	EINT	HSE	RESERVED	HCH

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Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x0 0000
12	HCE	See xHCI specification.	R	0
11	CNR	Controller not ready (see xHCI specification). Runtime or other operational registers are not accessed until field is cleared. Beyond xHCI (that is, USB host mode) functionality, indicates when the reset of the RAM is accessible, which makes the RAM-mapped registers accessible. Read 0x1: Controller not ready Read 0x0: Controller ready, RAM-mapped registers accessible	R	0
10	SRE	See xHCI specification.	RW W1toClr	0
9	RSS	See xHCI specification.	R	0
8	SSS	See xHCI specification.	R	0
7:5	RESERVED		R	0x0
4	PCD	See xHCI specification.	RW W1toClr	0
3	EINT	See xHCI specification.	RW W1toClr	0
2	HSE	See xHCI specification.	RW W1toClr	0
1	RESERVED		R	0
0	HCH	See xHCI specification.	R	1

Table 23-1137. Register Call Summary for Register USBOTGSS_USBSTS

Super-Speed USB OTG Subsystem

- Software Reset: [0]
- Active RAM Reset: [1]
- xHCI USB Host Software API: [2]
- DWC_USB3 Register Summary: [3]
- DWC_USB3 Register Description: [4]
- USBOTGSS_WRAPPER Register Description: [5]

Table 23-1138. USBOTGSS_PAGESIZE

Address Offset	0x0000 0028		
Physical Address	0x4A03 0028	**Instance**	DWC_USB3
Description	Page size register (xHCI)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PAGE_SIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	PAGE_SIZE	See xHCI specification. When bit n is set to 1, a page size of 2^(n+12) is supported. Read 0x1: 4-KiB page supported	R	0x0001

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Table 23-1139. Register Call Summary for Register USBOTGSS_PAGESIZE

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1140. USBOTGSS_DNCTRL

Address Offset	0x0000 0034		
Physical Address	0x4A03 0034	**Instance**	DWC_USB3
Description	Device notification control register (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		RW	0x0000
15	N15	See xHCI specification.	RW	0
14	N14	See xHCI specification.	RW	0
13	N13	See xHCI specification.	RW	0
12	N12	See xHCI specification.	RW	0
11	N11	See xHCI specification.	RW	0
10	N10	See xHCI specification.	RW	0
9	N9	See xHCI specification.	RW	0
8	N8	See xHCI specification.	RW	0
7	N7	See xHCI specification.	RW	0
6	N6	See xHCI specification.	RW	0
5	N5	See xHCI specification.	RW	0
4	N4	See xHCI specification.	RW	0
3	N3	See xHCI specification.	RW	0
2	N2	See xHCI specification.	RW	0
1	N1	See xHCI specification.	RW	0
0	N0	See xHCI specification.	RW	0

Table 23-1141. Register Call Summary for Register USBOTGSS_DNCTRL

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1142. USBOTGSS_CRCR_LO

Address Offset	0x0000 0038		
Physical Address	0x4A03 0038	**Instance**	DWC_USB3
Description	Command ring control register, lower half (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_RING_PNTR																								RESERVED				CRR	CA	CS	RCS

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Bits	Field Name	Description	Type	Reset
31:6	CMD_RING_PNTR	See xHCI specification.	RW	0x000 0000
5:4	RESERVED		RW	0x0
3	CRR	See xHCI specification.	RW	0
2	CA	See xHCI specification.	RW	0
1	CS	See xHCI specification.	RW	0
0	RCS	See xHCI specification.	RW	0

Table 23-1143. Register Call Summary for Register USBOTGSS_CRCR_LO

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1144. USBOTGSS_CRCR_HI

Address Offset	0x0000 003C		
Physical Address	0x4A03 003C	**Instance**	DWC_USB3
Description	Command ring control register, upper half (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_RING_PNTR																															

Bits	Field Name	Description	Type	Reset
31:0	CMD_RING_PNTR	See xHCI specification.	RW	0x0000 0000

Table 23-1145. Register Call Summary for Register USBOTGSS_CRCR_HI

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1146. USBOTGSS_DCBAAP_LO

Address Offset	0x0000 0050		
Physical Address	0x4A03 0050	**Instance**	DWC_USB3
Description	Device context base address array pointer, lower half (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_CONTEXT_BAAP																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:6	DEVICE_CONTEXT_BAAP	See xHCI specification.	RW	0x000 0000
5:0	RESERVED		RW	0x00

Table 23-1147. Register Call Summary for Register USBOTGSS_DCBAAP_LO

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

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Table 23-1148. USBOTGSS_DCBAAP_HI

Address Offset	0x0000 0054		
Physical Address	0x4A03 0054	**Instance**	DWC_USB3
Description	Device context base address array pointer, upper half (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_CONTEXT_BAAP																															

Bits	Field Name	Description	Type	Reset
31:0	DEVICE_CONTEXT_BAAP	See xHCI specification.	RW	0x0000 0000

Table 23-1149. Register Call Summary for Register USBOTGSS_DCBAAP_HI

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1150. USBOTGSS_CONFIG

Address Offset	0x0000 0058		
Physical Address	0x4A03 0058	**Instance**	DWC_USB3
Description	Configure (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MAXSLOTSEN							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		RW	0x00 0000
7:0	MAXSLOTSEN	See xHCI specification.	RW	0x00

Table 23-1151. Register Call Summary for Register USBOTGSS_CONFIG

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1152. USBOTGSS_PORTSC1

Address Offset	0x0000 0420		
Physical Address	0x4A03 0420	**Instance**	DWC_USB3
Description	Port 1 (USB2) status and control (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WPR	DR	RESERVED		WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS	PIC		PORTSPEED			PP	PLS			PR	OCA	RESERVED		PED	CCS	

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Bits	Field Name	Description	Type	Reset
31	WPR	See xHCI specification	RW W1toSet	0
30	DR	See xHCI specification	R	0
29:28	RESERVED		R	0x0
27	WOE	See xHCI specification	RW	0
26	WDE	See xHCI specification	RW	0
25	WCE	See xHCI specification	RW	0
24	CAS	See xHCI specification	R	0
23	CEC	See xHCI specification	RW W1toClr	0
22	PLC	See xHCI specification	RW W1toClr	0
21	PRC	See xHCI specification	RW W1toClr	0
20	OCC	See xHCI specification	RW W1toClr	0
19	WRC	See xHCI specification	RW W1toClr	0
18	PEC	See xHCI specification	RW W1toClr	0
17	CSC	See xHCI specification	RW W1toClr	0
16	LWS	See xHCI specification	RW	0
15:14	PIC	See xHCI specification	RW	0x0
13:10	PORTSPEED	See xHCI specification	R	0x0
9	PP	See xHCI specification	RW	1
8:5	PLS	See xHCI specification	RW	0x4
4	PR	See xHCI specification	RW W1toSet	0
3	OCA	See xHCI specification	R	0
2	RESERVED		R	0
1	PED	See xHCI specification	RW W1toClr	0
0	CCS	See xHCI specification	R	0

Table 23-1153. Register Call Summary for Register USBOTGSS_PORTSC1

Super-Speed USB OTG Subsystem

- Manual Far-end Receiver Detection in USB3 Host Mode: [0] [1] [2] [3]
- DWC_USB3 Register Summary: [4]
- DWC_USB3 Register Description: [5]

Table 23-1154. USBOTGSS_PORTPMSC1

Address Offset	0x0000 0424		
Physical Address	0x4A03 0424	**Instance**	DWC_USB3
Description	Port 1 (USB2) Power mManagement status and control (xHCI) Note that the PMSC register makeup is protocol-dependent (here: USB2)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_TEST_CONTROL				RESERVED											HLE	L1_DEVICE_SLOT								BESL				RWE	L1S		

Bits	Field Name	Description	Type	Reset
31:28	PORT_TEST_CONTROL	See xHCI specification	RW	0x0
27:17	RESERVED		R	0x000
16	HLE	See xHCI specification	RW	0
15:8	L1_DEVICE_SLOT	See xHCI specification	RW	0x00
7:4	BESL	See xHCI 1.0 standard w. errata	RW	0x0
3	RWE	See xHCI specification	RW	0
2:0	L1S	See xHCI specification	R	0x0

Table 23-1155. Register Call Summary for Register USBOTGSS_PORTPMSC1

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1156. USBOTGSS_PORTLI1

Address Offset	0x0000 0428		
Physical Address	0x4A03 0428	**Instance**	DWC_USB3
Description	Port 1 (USB2) link info (xHCI)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINK_ERROR_COUNT															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	LINK_ERROR_COUNT	See xHCI specification.	R	0x0000

Table 23-1157. Register Call Summary for Register USBOTGSS_PORTLI1

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1158. USBOTGSS_PORTHLPMC1

Address Offset	0x0000 042C		
Physical Address	0x4A03 042C	**Instance**	DWC_USB3
Description	Port 1 (USB2) Hardware LPM Control (xHCI) Field structure is protocol-dependent (here: USB3)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		BESLD				L1_TIMEOUT								HIRDM	

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x0 0000
13:10	BESLD	See xHCI 1.0 standard w errata	RW	0x0
9:2	L1_TIMEOUT	See xHCI 1.0 standard w errata	RW	0x00
1:0	HIRDM	See xHCI 1.0 standard w errata	RW	0x0

Table 23-1159. Register Call Summary for Register USBOTGSS_PORTHLPMC1

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1160. USBOTGSS_PORTSC2

Address Offset	0x0000 0430		
Physical Address	0x4A03 0430	**Instance**	DWC_USB3
Description	Port 2 (USB3) status and control (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WPR	DR	RESERVED		WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS	PIC		PORTSPEED				PP		PLS				PR	OCA	RESERVED		PED	CCS

Bits	Field Name	Description	Type	Reset
31	WPR	See xHCI specification	RW W1toSet	0
30	DR	See xHCI specification	R	0
29:28	RESERVED		R	0x0
27	WOE	See xHCI specification	RW	0
26	WDE	See xHCI specification	RW	0
25	WCE	See xHCI specification	RW	0
24	CAS	See xHCI specification	R	0
23	CEC	See xHCI specification	RW W1toClr	0
22	PLC	See xHCI specification	RW W1toClr	0
21	PRC	See xHCI specification	RW W1toClr	0
20	OCC	See xHCI specification	RW W1toClr	0
19	WRC	See xHCI specification	RW W1toClr	0
18	PEC	See xHCI specification	RW W1toClr	0
17	CSC	See xHCI specification	RW W1toClr	0
16	LWS	See xHCI specification	RW	0
15:14	PIC	See xHCI specification	RW	0x0

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Bits	Field Name	Description	Type	Reset
13:10	PORTSPEED	See xHCI specification	R	0x0
9	PP	See xHCI specification	RW	1
8:5	PLS	See xHCI specification	RW	0x4
4	PR	See xHCI specification	RW W1toSet	0
3	OCA	See xHCI specification	R	0
2	RESERVED		R	0
1	PED	See xHCI specification	RW W1toClr	0
0	CCS	See xHCI specification	R	0

Table 23-1161. Register Call Summary for Register USBOTGSS_PORTSC2

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1162. USBOTGSS_PORTPMSC2

Address Offset	0x0000 0434		
Physical Address	0x4A03 0434	**Instance**	DWC_USB3
Description	Port 2 (USB3) power management (LPM) status and control (xHCI) Note that the PMSC register makeup is protocol-dependent (here: USB3)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FLA	U2_TIMEOUT								U1_TIMEOUT							

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	FLA	See xHCI specification	RW	0
15:8	U2_TIMEOUT	See xHCI specification	RW	0x00
7:0	U1_TIMEOUT	See xHCI specification	RW	0x00

Table 23-1163. Register Call Summary for Register USBOTGSS_PORTPMSC2

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1164. USBOTGSS_PORTLI2

Address Offset	0x0000 0438		
Physical Address	0x4A03 0438	**Instance**	DWC_USB3
Description	Port 2 (USB3) link info (xHCI)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LINK_ERROR_COUNT															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	LINK_ERROR_COUNT	See xHCI specification.	R	0x0000

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Table 23-1165. Register Call Summary for Register USBOTGSS_PORTLI2

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1166. USBOTGSS_PORTHLPMC2

Address Offset	0x0000 043C		
Physical Address	0x4A03 043C	**Instance**	DWC_USB3
Description	Port 2 (USB3) Hardware LPM Control (xHCI) Field structure is protocol-dependent (here: USB3)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED		R	0x0000 0000

Table 23-1167. Register Call Summary for Register USBOTGSS_PORTHLPMC2

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1168. USBOTGSS_MFINDEX

Address Offset	0x0000 0440		
Physical Address	0x4A03 0440	**Instance**	DWC_USB3
Description	Microframe index (xHCI)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MICROFRAME_INDEX															

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x0 0000
13:0	MICROFRAME_INDEX	See xHCI specification.	R	0x0000

Table 23-1169. Register Call Summary for Register USBOTGSS_MFINDEX

Super-Speed USB OTG Subsystem

- xHCI Host Mapping: [0]
- DWC_USB3 Register Summary: [1]
- DWC_USB3 Register Description: [2]

Table 23-1170. USBOTGSS_IMAN

Address Offset	0x0000 0460		
Physical Address	0x4A03 0460	**Instance**	DWC_USB3
Description	Interrupter Management (xHCI)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														IE	IP

Bits	Field Name	Description	Type	Reset
31:2	RESERVED		R	0x0000 0000
1	IE	Interrupt enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
0	IP	Interrupt pending. Set (to 1) when: IE = 1, USBOTGSS_IMOD[31:16] IMODC = 0, the associated event ring is not empty, USBOTGSS_ERDP_LO[3] EHB = 0. 0x0: No IRQ pending 0x1: IRQ pending	RW W1toClr	0

Table 23-1171. Register Call Summary for Register USBOTGSS_IMAN

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- USBOTGSS_WRAPPER Register Description: [1] [2]

Table 23-1172. USBOTGSS_IMOD

Address Offset	0x0000 0464		
Physical Address	0x4A03 0464	**Instance**	DWC_USB3
Description	Interrupter moderation (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMODC																IMODI															

Bits	Field Name	Description	Type	Reset
31:16	IMODC	Interrupt moderation counter: Loaded to IMODI whenever IP is cleared to 0, counts down to 0, and stops. IRQ is generated when counter is 0, event ring is not empty, USBOTGSS_IMAN[1] IE = 1, USBOTGSS_IMAN[0] IP = 1, USBOTGSS_ERDP_LO[3] EHB = 0. Can be directly written to at any time alter the interrupt rate	RW	0x0000
15:0	IMODI	Interrupt moderation interval: Minimum inter-IRQ interval, in 250-ns increments. 0xFA0: 1-ms interval (default) 0x0: IRQ throttling disabled: IRQs generated immediately. 0x1: 250-ns minimum interval	RW	0x0FA0

Table 23-1173. Register Call Summary for Register USBOTGSS_IMOD

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1]

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Table 23-1174. USBOTGSS_ERSTSZ

Address Offset	0x0000 0468		
Physical Address	0x4A03 0468	**Instance**	DWC_USB3
Description	Event ring segment table size (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERS_TABLE_SIZE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		RW	0x0000
15:0	ERS_TABLE_SIZE	See xHCI specification.	RW	0x0000

Table 23-1175. Register Call Summary for Register USBOTGSS_ERSTSZ

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1176. USBOTGSS_ERSTBA_LO

Address Offset	0x0000 0470		
Physical Address	0x4A03 0470	**Instance**	DWC_USB3
Description	Event ring segment table base address, lower half (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERS_TABLE_BAR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:6	ERS_TABLE_BAR	See xHCI specification.	RW	0x000 0000
5:0	RESERVED		RW	0x00

Table 23-1177. Register Call Summary for Register USBOTGSS_ERSTBA_LO

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1178. USBOTGSS_ERSTBA_HI

Address Offset	0x0000 0474		
Physical Address	0x4A03 0474	**Instance**	DWC_USB3
Description	Event ring segment table base address, upper half (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERS_TABLE_BAR																															

Bits	Field Name	Description	Type	Reset
31:0	ERS_TABLE_BAR	See xHCI specification.	RW	0x0000 0000

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Table 23-1179. Register Call Summary for Register USBOTGSS_ERSTBA_HI

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1180. USBOTGSS_ERDP_LO

Address Offset	0x0000 0478		
Physical Address	0x4A03 0478	**Instance**	DWC_USB3
Description	Event ring dequeue pointer, lower half (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERD_PNTR																												EHB	DESI		

Bits	Field Name	Description	Type	Reset
31:4	ERD_PNTR	See xHCI specification.	RW	0x000 0000
3	EHB	See xHCI specification.	RW W1toClr	0
2:0	DESI	See xHCI specification.	RW	0x0

Table 23-1181. Register Call Summary for Register USBOTGSS_ERDP_LO

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1]

Table 23-1182. USBOTGSS_ERDP_HI

Address Offset	0x0000 047C		
Physical Address	0x4A03 047C	**Instance**	DWC_USB3
Description	Event ring dequeue pointer, upper half (xHCI)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERD_PNTR																															

Bits	Field Name	Description	Type	Reset
31:0	ERD_PNTR	See xHCI specification.	RW	0x0000 0000

Table 23-1183. Register Call Summary for Register USBOTGSS_ERDP_HI

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1184. USBOTGSS_DB_j

Address Offset	0x0000 0480 + (0x4 * j)	**Index**	j = 0 to 63
Physical Address	0x4A03 0480 + (0x4 * j)	**Instance**	DWC_USB3
Description	Doorbell (xHCI)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DB_STREAM_ID																RESERVED								DB_TARGET							

Bits	Field Name	Description	Type	Reset
31:16	DB_STREAM_ID	See xHCI specification.	RW	0x0000
15:8	RESERVED		R	0x00
7:0	DB_TARGET	See xHCI specification.	RW	0x00

Table 23-1185. Register Call Summary for Register USBOTGSS_DB_j

Super-Speed USB OTG Subsystem

- xHCI Host Mapping: [0]
- DWC_USB3 Register Summary: [1]
- DWC_USB3 Register Description: [2]

Table 23-1186. USBOTGSS_USBLEGSUP

Address Offset	0x0000 0880		
Physical Address	0x4A03 0880	**Instance**	DWC_USB3
Description	USB legacy support capability		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							HCOOS	RESERVED							HCBOS	NCP								ECID							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	HCOOS	HC OS Owned Semaphore: See xHCI specification	RW	0
23:17	RESERVED		R	0x00
16	HCBOS	HC BIOS Owned Semaphore: See xHCI specification	RW	0
15:8	NCP	Next Capability Pointer: 32-bit dword offset of the next capability. Read 0x0: End of capability list	R	0x04
7:0	ECID	Extended Capability ID code (descriptor size, in bytes) Read 0x2: Supported protocol: MajRev.MinRev (12) Read 0x1: USB legacy support (8) Read 0xA: USB debug capability (56)	R	0x01

Table 23-1187. Register Call Summary for Register USBOTGSS_USBLEGSUP

Super-Speed USB OTG Subsystem

- xHCI Host Mapping: [0]
- DWC_USB3 Register Summary: [1]

Table 23-1188. USBOTGSS_USBLEGCTLSTS

Address Offset	0x0000 0884		
Physical Address	0x4A03 0884	**Instance**	DWC_USB3
Description	USB legacy control/status		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SB	SPC	SOOC	RESERVED								SHSE	RESERVED			SEI	SBE	SPCE	SOOE	RESERVED								SHSEE	RESERVED			USE

Bits	Field Name	Description	Type	Reset
31	SB	See xHCI specification.	RW W1toClr	0
30	SPC	See xHCI specification.	RW W1toClr	0
29	SOOC	See xHCI specification.	RW W1toClr	0
28:21	RESERVED		R	0x00
20	SHSE	See xHCI specification.	R	0
19:17	RESERVED		R	0x0
16	SEI	See xHCI specification.	R	0
15	SBE	See xHCI specification.	RW	0
14	SPCE	See xHCI specification.	RW	0
13	SOOE	See xHCI specification.	RW	0
12:5	RESERVED		R	0x00
4	SHSEE	See xHCI specification.	RW	0
3:1	RESERVED		R	0x0
0	USE	See xHCI specification.	RW	0

Table 23-1189. Register Call Summary for Register USBOTGSS_USBLEGCTLSTS

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1190. USBOTGSS_SUPTPRT2_DW0

Address Offset	0x0000 0890		
Physical Address	0x4A03 0890	**Instance**	DWC_USB3
Description	Supported protocol capability USB2, 32-bit dword 0		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAJREV								MINREV								NCP								ECID							

Bits	Field Name	Description	Type	Reset
31:24	MAJREV	Major Revision, BCD-encoded	R	0x02
23:16	MINREV	Minor Revision, BCD-encoded	R	0x00
15:8	NCP	Next Capability Pointer: 32-bit dword offset of the next capability. Read 0x0: End of capability list	R	0x04
7:0	ECID	Extended Capability ID code (descriptor size, in bytes) Read 0x2: Supported protocol: MajRev.MinRev (12) Read 0x1: USB legacy support (8) Read 0xA: USB debug capability (56)	R	0x02

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Table 23-1191. Register Call Summary for Register USBOTGSS_SUPTPRT2_DW0

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1192. USBOTGSS_SUPTPRT2_DW1

Address Offset	0x0000 0894		
Physical Address	0x4A03 0894	**Instance**	DWC_USB3
Description	Supported protocol capability USB2, 32-bit dword 1: Name String "USB "		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAR3								CHAR2								CHAR1								CHAR0							

Bits	Field Name	Description	Type	Reset
31:24	CHAR3	ASCII " " (space)	R	0x20
23:16	CHAR2	ASCII "B"	R	0x42
15:8	CHAR1	ASCII "S"	R	0x53
7:0	CHAR0	ASCII "U"	R	0x55

Table 23-1193. Register Call Summary for Register USBOTGSS_SUPTPRT2_DW1

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1194. USBOTGSS_SUPTPRT2_DW2

Address Offset	0x0000 0898		
Physical Address	0x4A03 0898	**Instance**	DWC_USB3
Description	Supported protocol capability USB2, 32-bit dword 2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSIC				RESERVED								HLC	IHI	HSO	RESERVED	CPC								CPO							

Bits	Field Name	Description	Type	Reset
31:28	PSIC	Port Speed ID Count. Reserved in xHCI 0.96 Read 0x0: USB2 High/Full/Low-speeds supported	R	0x0
27:20	RESERVED		R	0x00
19	HLC	Hardware LPM Capability.	R	1
18	IHI	Integrated Hub Implemented.	R	0
17	HSO	High-Speed Only	R	0
16	RESERVED		R	1
15:8	CPC	Compatible Port Count: Number of consecutive ports of the root hub that support this protocol, from CPO to CPO+CPC-1	R	0x01
7:0	CPO	Compatible Port Offset: Starting port number of root hub port(s) that support this protocol.	R	0x01

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Table 23-1195. Register Call Summary for Register USBOTGSS_SUPTPRT2_DW2

Super-Speed USB OTG Subsystem

- xHCI USB Host Software API: [0] [1]
- DWC_USB3 Register Summary: [2]

Table 23-1196. USBOTGSS_SUPTPRT2_DW3

Address Offset	0x0000 089C		
Physical Address	0x4A03 089C	**Instance**	DWC_USB3
Description	Supported protocol capability USB2, 32-bit dword 3		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PST							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	PST	Protocol Slot Type, see xHCI 1.0 standard w errata	R	0x00

Table 23-1197. Register Call Summary for Register USBOTGSS_SUPTPRT2_DW3

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1198. USBOTGSS_SUPTPRT3_DW0

Address Offset	0x0000 08A0		
Physical Address	0x4A03 08A0	**Instance**	DWC_USB3
Description	Supported protocol capability USB3, 32-bit dword 0		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAJREV								MINREV								NCP								ECID							

Bits	Field Name	Description	Type	Reset
31:24	MAJREV	Major Revision, BCD-encoded	R	0x03
23:16	MINREV	Minor Revision, BCD-encoded	R	0x00
15:8	NCP	Next Capability Pointer: 32-bit dword offset of the next capability. Read 0x0: End of capability list	R	0x00
7:0	ECID	Extended Capability ID code (descriptor size, in bytes) Read 0x2: Supported protocol: MajRev.MinRev (12) Read 0x1: USB legacy support (8) Read 0xA: USB debug capability (56)	R	0x02

Table 23-1199. Register Call Summary for Register USBOTGSS_SUPTPRT3_DW0

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

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Table 23-1200. USBOTGSS_SUPTPRT3_DW1

Address Offset	0x0000 08A4		
Physical Address	0x4A03 08A4	**Instance**	DWC_USB3
Description	Supported protocol capability USB3, 32-bit dword 1: Name String "USB "		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHAR3								CHAR2								CHAR1								CHAR0							

Bits	Field Name	Description	Type	Reset
31:24	CHAR3	ASCII " " (space)	R	0x20
23:16	CHAR2	ASCII "B"	R	0x42
15:8	CHAR1	ASCII "S"	R	0x53
7:0	CHAR0	ASCII "U"	R	0x55

Table 23-1201. Register Call Summary for Register USBOTGSS_SUPTPRT3_DW1

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1202. USBOTGSS_SUPTPRT3_DW2

Address Offset	0x0000 08A8		
Physical Address	0x4A03 08A8	**Instance**	DWC_USB3
Description	Supported protocol capability USB3, 32-bit dword 2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSIC				RESERVED												CPC								CPO							

Bits	Field Name	Description	Type	Reset
31:28	PSIC	Port Speed ID Count. Reserved in xHCI 0.96 Read 0x0: USB3 Super-Speed supported	R	0x0
27:16	RESERVED		R	0x000
15:8	CPC	Compatible Port Count: Number of consecutive ports of the root hub that support this protocol, from CPO to CPO+CPC-1	R	0x01
7:0	CPO	Compatible Port Offset: Starting port number of root hub port(s) that support this protocol.	R	0x02

Table 23-1203. Register Call Summary for Register USBOTGSS_SUPTPRT3_DW2

Super-Speed USB OTG Subsystem

- xHCI USB Host Software API: [0] [1]
- DWC_USB3 Register Summary: [2]

Table 23-1204. USBOTGSS_SUPTPRT3_DW3

Address Offset	0x0000 08AC		
Physical Address	0x4A03 08AC	**Instance**	DWC_USB3
Description	Supported protocol capability USB3, 32-bit dword 3		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PST							

Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x000 0000
4:0	PST	Protocol Slot Type, see xHCI 1.0 standard w errata	R	0x00

Table 23-1205. Register Call Summary for Register USBOTGSS_SUPTPRT3_DW3

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1206. USBOTGSS_GSBUSCFG0

Address Offset	0x0000 C100		
Physical Address	0x4A03 C100	**Instance**	DWC_USB3
Description	Global device Bus Configuration Register 0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			DESCBIGEND	DATBIGEND	RESERVED			INCR256BRSTENA	INCR128BRSTENA	INCR64BRSTENA	INCR32BRSTENA	INCR16BRSTENA	INCR8BRSTENA	INCR4BRSTENA	INCRBRSTENA

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		RW	0x0 0000
12	DESCBIGEND	Endian mode for descriptor accesses. 0x0: Little-Endian (default) 0x1: Big-Endian	RW	0
11	DATBIGEND	Endian mode for data accesses. 0x0: Little-Endian (default) 0x1: Big-Endian	RW	0
10:8	RESERVED		RW	0x0
7	INCR256BRSTENA	INCR256 Burst Type Enable. 256×64/8= 2-kByte burst.	RW	0
6	INCR128BRSTENA	INCR128 Burst Type Enable. 128×64/8= 1-kByte burst.	RW	0
5	INCR64BRSTENA	INCR64 Burst Type Enable. 64×64/8= 512-Byte burst.	RW	0
4	INCR32BRSTENA	INCR32 Burst Type Enable. 32×64/8= 256-Byte burst.	RW	0
3	INCR16BRSTENA	INCR16 Burst Type Enable. 16×64/8= 128-Byte burst.	RW	1
2	INCR8BRSTENA	INCR8 Burst Type Enable. 8×64/8= 64-Byte burst.	RW	1
1	INCR4BRSTENA	INCR4 Burst Type Enable. 4×64/8= 32-Byte burst: RECOMMENDED Enables bursts of beat length 1, 2, 3, 4, and prevents (16-byte) descriptor accesses from being broken up: highly recommended.	RW	1
0	INCRBRSTENA	Undefined Length INCR Burst Type Enable: DO NOT ENABLE When enabled, this has higher priority than other burst types.	RW	0

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Table 23-1207. Register Call Summary for Register USBOTGSS_GSBUSCFG0

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1208. USBOTGSS_GSBUSCFG1

Address Offset	0x0000 C104		
Physical Address	0x4A03 C104	**Instance**	DWC_USB3
Description	Global device bus configuration register 1		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			EN1KPAGE	BREQLIMIT				RESERVED							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x0 0000
12	EN1KPAGE	1k-page boundary enable 0x0: Master breaks requests only on 4-KiB boundaries. 0x1: Master breaks requests on all 1-KiB boundaries.	RW	0
11:8	PIPETRANSLIMIT	Maximum number of outstanding (read or write) pipelined sequential (i.e. in-order) transaction requests on the master interface (field value+1) 0xF: Up to 16 pending requests (maximum). 0x0: Single request mode. 0x1: Up to 2 pending requests	RW	0xF
7:0	RESERVED	Always write 0. (The result of writing a non-0 value is undetermined.)	RW	0x00

Table 23-1209. Register Call Summary for Register USBOTGSS_GSBUSCFG1

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1210. USBOTGSS_GTXTHRCFG

Address Offset	0x0000 C108		
Physical Address	0x4A03 C108	**Instance**	DWC_USB3
Description	Global TX threshold control register. Valid only in Host mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		USBTXPKTCNTSEL	RESERVED	USBTXPKTCNT				USBMAXTXBURSTSIZE								RESERVED		RESERVED		RESERVED											

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Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Always write 0, result of writing of a non-zero value is undetermined.	RW	0x0
29	USBTXPKTCNTSEL	USB Transmit Packet Count Enable: Enables/disables USB trasnmission multi-packet thresholding 0x0: Disabled: Transmission is only started on the USB after the entire packet has been fetched into the corresponding TXFIFO. Rest of the register must be all-zero. 0x1: Enabled: USB transmission is started only after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO This mode is only valid in the host, superspeed mode.	RW	0
28	RESERVED		R	0
27:24	USBTXPKTCNT	USB Transmit Packet Count : Number of packets that must be in the TXFIFO before transmission for the corresponding USB transaction (burst) can start. Don't care if USBTXPKTCNTSEL=0. 0xF: Maximum value 0x0: Use when and only when disabled (USBTXPKTCNTSEL=0) 0x1: Minimum value (when enabled)	RW	0x0
23:16	USBMAXTXBURSTSIZE	USB Maximum Transmit Burst Size. Max OUT burst size, when USBTXPKTCNTSEL=1. Avoids TX FIFO underrun when the system bus is slower than the USB. Only applies to SS Bulk / Iso / Int OUT endpoints in host mode. Don't care if USBTXPKTCNTSEL=0. 0x0: Use when and only when disabled (USBTXPKTCNTSEL=0) 0x1: Burst of up to 1 (minimum value when enabled) 0x10: Burst of up to 16 (maximum value)	RW	0x00
15:14	RESERVED	Always write 0, result of writing of a non-zero value is undetermined.	RW	0x0
13:11	RESERVED		R	0x0
10:0	RESERVED	Always write 0, result of writing of a non-zero value is undetermined.	RW	0x000

Table 23-1211. Register Call Summary for Register USBOTGSS_GTXTHRCFG

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1212. USBOTGSS_GRXTHRCFG

Address Offset	0x0000 C10C		
Physical Address	0x4A03 C10C	**Instance**	DWC_USB3
Description	Global RX Threshold Control Register		
Type	RW		

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31 30	29	28	27 26 25 24	23 22 21 20 19	18 17 16	15	14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	USBRXPKTCNTSEL	RESERVED	USBRXPKTCNT	USBMAXRXBURSTSIZE	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	USBRXPKTCNTSEL	USB ReceivePacket Count Enable Enables/disables USB reception multi-packet thresholding 0x0: The core can only start reception on the USB when the RX FIFO has space for at least one packet. Rest of the register must be all-zero. 0x1: The core can only start reception on the USB when the RX FIFO has space for at least packet. This mode is only valid in the host mode. It is only used for SuperSpeed.	RW	0
28	RESERVED		R	0
27:24	USBRXPKTCNT	USB Receive Packet Count: Number of packets that must be available in the RX FIFO before the core can start the corresponding USB RX transaction (burst). Don't care if USBRXPKTCNTSEL=0. 0xF: Maximum value 0x0: Use when and only when disabled (USBRXPKTCNTSEL=0) 0x1: Minimum value (when enabled)	RW	0x0
23:19	USBMAXRXBURSTSIZE	USB Maximum Receive Burst Size. Maxi IN burst size, when USBRXPKTCNTSEL = 1. When the system bus is slower than the USB, RX FIFO can overrun during a long burst. User can program a smaller value to this field to limit the RX burst size that the core can do. Only applies to SS Bulk / Iso / Int IN endpoints in host mode. Don't care if USBRXPKTCNTSEL=0. 0x0: Use when and only when disabled (USBRXPKTCNTSEL=0) 0x1: Burst of up to 1 (minimum value when enabled) 0x10: Burst of up to 16 (maximum value)	RW	0x00
18:16	RESERVED		R	0x0
15	RESERVED	Always write 0, result of writing of a non-zero value is undetermined.	RW	0
14:11	RESERVED		R	0x0
10:0	RESERVED	Always write 0, result of writing of a non-zero value is undetermined.	RW	0x000

Table 23-1213. Register Call Summary for Register USBOTGSS_GRXTHRCFG

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

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Table 23-1214. USBOTGSS_GCTL

Address Offset	0x0000 C110		
Physical Address	0x4A03 C110	**Instance**	DWC_USB3
Description	Global control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWRDNSCALE													MASTERFILTBYPASS	BYPSSETADDR	U2RSTECN	FRMSCLDWN		PRTCAPDIR		CORESOFTRESET	RESERVED		DEBUGATTACH	RAMCLKSEL		SCALEDOWN		DISSCRAMBLE	RESERVED		DSBLCLKGTNG

Bits	Field Name	Description	Type	Reset
31:19	PWRDNSCALE	Power Down Scale: In P3 state, pipe clock stops and is replaced internally by the suspend clock to create a 16kHz reference. Set field to Fs/16k, rounded up, with Fp suspend clock frequency. Required accuracy is 0-50% 0x2: 32kHz suspend clock (minimum frequency) 0x960: 38.4 MHz suspend clock 0x2EE: 12 MHz suspend clock 0x5DC: 24 MHz suspend clock 0x4B0: 19.2 MHz suspend clock 0x32D: 13 MHz suspend clock 0x659: 26 MHz suspend clock 0x1E85: 125 MHz suspend clock	RW	0x04B0
18	MASTERFILTBYPASS	Master Filter Bypass. Bypasses the double-synchronizers and the 5 ms debounce filters on UTMI+ inputs (the latter are not implemented).	RW	0
17	BYPSSETADDR	Override of the device address, bypassing the SET ADDRESS control transfer. For simulation only. 0x0: Functional mode 0x1: Device's address set directly to USBOTGSS_DCFG[9:3] DEVADDR	RW	0
16	U2RSTECN	If the super speed connection fails during POLL or LMP exchange, the device connects at non-SS mode. If this bit is set, then device attempts three more times to connect at SS, even if it previously failed to operate in SS mode.	RW	0
15:14	FRMSCLDWN	Frame scale-down This field scales down device view of a SOF (FS/LS) / uSOF (HS) / ITP (SS) duration. 0x0: SS/HS interval=125 us, FS interval=1ms (standard) 0x1: SS/HS interval=62.5 us, FS interval=0.5ms 0x3: SS/HS interval=15.625 us, FS interval=0.125ms 0x2: SS/HS interval=31.25 us, FS interval=0.25ms	RW	0x0
13:12	PRTCAPDIR	Port Capability Direction 0x1: Core acts as DRD in host mode 0x3: Core acts as OTG DRD, with the mode set by the ID 0x2: Core acts as DRD in device mode	RW	0x3

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Bits	Field Name	Description	Type	Reset
11	CORESOFTRESET	Core Soft Reset. When you reset PHYs (using USBOTGSS_GUSB2PHYCFG or USBOTGSS_GUSB3PIPECTL registers), you must keep the core in reset state until PHY clocks are stable. 0x0: No soft reset 0x1: Soft reset to core	RW	0
10:9	RESERVED		R	0x0
8	DEBUGATTACH	Debug Attach. When this bit is set: a) SS Link proceeds directly to the Polling link state (after RUN/STOP in the USBOTGSS_DCTL register is asserted) without checking remote termination. b) Link LFPS polling timeout is infinite c) Polling timeout during TS1 is infinite (in case link is waiting for TXEQ to finish).	RW	0
7:6	RAMCLKSEL	RAM Clock Select. No action, hardware always uses bus clock (config 2'b00) 0x0: AXI bus clock 0x1: PIPE clock 0x3: MAC clock (125 MHz) 0x2: PIPE/2 clock	RW	0x0
5:4	SCALEDOWN	Scale-Down Mode Enable Switches to shorter, non-standard protocol time intervals to speed up simulation. DO NOT MODIFY ON ACTUAL HARDWARE. 0x0: Disable scale-downs. Legal USB timing values are used. Always use on actual hardware. 0x1: Enables scaled down values of : - HS/FS/LS: all except Device-mode suspend and resume. - SS: Number of TxEq training sequences reduce to 8 - SS: LFPS polling burst time reduce to 100 ns - SS: LFPS warm reset receive reduce to 30 us - SS: more ... 0x3: SS/HS/FS/LS: scale down all the above 0x2: HS/FS/LS: scale-down of Device-mode suspend and resume. SS: No TxEq training sequences are sent.	RW	0x0
3	DISSCRAMBLE	Disable Scrambling. Transmit request to Link Partner on next transition to Recovery or Polling.	RW	0
2:1	RESERVED		R	0x0
0	DSBLCLKGTNG	Disable Clock Gating. When this bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled.	RW	0

Table 23-1215. Register Call Summary for Register USBOTGSS_GCTL

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1]

Table 23-1216. USBOTGSS_GSTS

Address Offset	0x0000 C118		
Physical Address	0x4A03 C118	**Instance**	DWC_USB3
Description	Global status register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CBELT								RESERVED													OTG_IP	BC_IP	ADP_IP	HOST_IP	DEVICE_IP	CSRTIMEOUT	BUSERRADDRVLD	RESERVED		CURMOD	

Bits	Field Name	Description	Type	Reset
31:20	CBELT	Current BELT Value In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.	R	0x3E8
19:11	RESERVED		R	0x000
10	OTG_IP	OTG interrupt status Read 0x1: Interrupt pending Read 0x0: No interrupt pending	R	0
9	BC_IP	Battery Charger interrupt status: NOT IMPLEMENTED	R	0
8	ADP_IP	ADP interrupt status: NOT IMPLEMENTED	R	0
7	HOST_IP	Host interrupt status Read 0x1: Interrupt pending Read 0x0: No interrupt pending	R	0
6	DEVICE_IP	Device interrupt status Read 0x1: Interrupt pending Read 0x0: No interrupt pending	R	0
5	CSRTIMEOUT	Control/Status Register access Timeout status flag. Write 0x0: No action Write 0x1: Clear the status flag. Read 0x1: CSR access timed out after 65,535 clock cycles Read 0x0: no CSR timeout	RW	0
4	BUSERRADDRVLD	Bus Error Address Valid status flag. Also flagged on USBOTGSS_USBSTS[2] HSE field (host mode) and DEPEVT[12] on XferComplete/XferInProgress event (device mode). Write 0x0: No action Write 0x1: Clear the status flag. Read 0x1: At least one bus error took place, the first one near address GBUSERRADDR. Read 0x0: No bus error since last clear; GBUSERRADDR is not valid	RW	0
3:2	RESERVED		R	0x0
1:0	CURMOD	Current Mode of Operation. Read 0x2: DRD Read 0x1: Host Read 0x0: Device	R	0x2

Table 23-1217. Register Call Summary for Register USBOTGSS_GSTS

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1] [2] [3]

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Table 23-1218. USBOTGSS_GSNPSID

Address Offset	0x0000 C120		
Physical Address	0x4A03 C120	**Instance**	DWC_USB3
Description	Synopsys ID: Core identification and release number. Software uses this register to configure release-specific features in the driver.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNOPSYSID_CORE																SYNOPSYSID_REL															

Bits	Field Name	Description	Type	Reset
31:16	SYNOPSYSID_CORE	SYNOPSYSID MSBytes: core identifier Read 0x5533: ASCII for "U3" = DWC_USB3	R	0x5533
15:0	SYNOPSYSID_REL	SYNOPSYSID LSBytes: version number For instance, version 1.00a => 0x100A Read 0x183A: version 1.83a Read 0x202A: version 2.02a	R	0x202A

Table 23-1219. Register Call Summary for Register USBOTGSS_GSNPSID

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1]

Table 23-1220. USBOTGSS_GGPIO

Address Offset	0x0000 C124		
Physical Address	0x4A03 C124	**Instance**	DWC_USB3
Description	Global general-purpose input/output register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPO																GPI															

Bits	Field Name	Description	Type	Reset
31:16	GPO	General-purpose output. DO NOT USE: NOT CONNECTED.	RW	0x0000
15:0	GPI	General-purpose inputs. TIED LOW.	R	0x0000

Table 23-1221. Register Call Summary for Register USBOTGSS_GGPIO

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1]

Table 23-1222. USBOTGSS_GUID

Address Offset	0x0000 C128		
Physical Address	0x4A03 C128	**Instance**	DWC_USB3
Description	Global user ID register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USERID																															

Bits	Field Name	Description	Type	Reset
31:0	USERID	Application-programmable ID field	RW	0x0000 0000

Table 23-1223. Register Call Summary for Register USBOTGSS_GUID

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1]

Table 23-1224. USBOTGSS_GUCTL

Address Offset	0x0000 C12C		
Physical Address	0x4A03 C12C	**Instance**	DWC_USB3
Description	Global user control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										NOEXTRDL	PSQEXTRRESSP			SPRSCTRLTRANSEN	RESBWHSEPS	CMDEVADDR	USBHSTINAUTORETRYEN	RESERVED			DTCT			DTFT							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		RW	0x000
21	NOEXTRDL	No Extra Delay between SOF and the 1st packet (when host) 0x0: 2 us delay between SOF and first packet. Some bandwith is lost. 0x1: No extra delay. May cause some devices to misbehave.	RW	0
20:18	PSQEXTRRESSP	Protocol Status Queue Extra Reserved Space (Debug only). Additional space in the PSQ reserved before the USB3 protocl transaction layer (U3PTL) initiates a new USB transaction and burst beats. 0x0: 0x1:	RW	0x0
17	SPRSCTRLTRANSEN	Sparse Control Transaction Enable. Valid in host mode only (any speed). 0x0: Feature disabled, no limitation on control transactions 0x1: Host controller schedules transactions for Control transfer in different [micro]frames to prevent incorrect behaviour from device.	RW	0
16	RESBWHSEPS	Reserving (more) Bandwidth for HS Periodic EPs. Valid in host mode only. 0x0: HC reserves 80% of the bandwidth for periodic EPs 0x1: HC reserves 85% of the bandwidth for periodic EPs, which allows 2 high speed, high bandwidth ISOC EPs.	RW	0

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Bits	Field Name	Description	Type	Reset
15	CMDEVADDR	Compliance Mode for Device Address. Valid in host mode only. 0x0: Device Address is equal to Slot ID. 0x1: Increment Device Address on each Address Device command. Slot ID may have different value than Device Address if max_slot_enabled < 128.	RW	1
14	USBHSTINAUTORETRYEN	Host IN Auto Retry Enable: host core behaviour upon data packet CRC errors or internal overrun scenarios in non-isochronous IN transfers. 0x0: Auto Retry Disabled: Host core to reply with a terminating retry ACK (Retry=1 and NumP=0) 0x1: Auto Retry Enabled: Host core to reply with a non-terminating retry ACK (Retry=1 and NumP!=0)	RW	0
13:11	RESERVED		RW	0x0
10:9	DTCT	Device Timeout Coarse Tuning: time the host waits for a response from device before timeout. Coarse setting. 0x0: Use DTFT instead 0x1: 500 us 0x3: 6.5 ms 0x2: 1.5 ms	RW	0x0
8:0	DTFT	Device Timeout Fine Tuning: time the host waits for a response from device before timeout. Fine setting. Timer runs on the 125 MHz clock (8 ns period), timeout is DTFT × 256 × 8 ns ~= DTFT × 2 us Don't care unless DTCT=0 0x1: ~ 2 us timeout (2,048 ns) 0x7D: 256 us timeout (maximum, exact value) 0x32: ~ 100 us timeout (102,400 ns) 0x5: ~ 10 us timeout (10,240 ns)	RW	0x010

Table 23-1225. Register Call Summary for Register USBOTGSS_GUCTL

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1226. USBOTGSS_GBUSERRADDRLO

Address Offset	0x0000 C130		
Physical Address	0x4A03 C130	**Instance**	DWC_USB3
Description	Global Bus Error (non-precise) Address, LSbits: Base address of the first system bus DMA transfer that got a bus error. Note that each DMA transfer can contain several bursts, each spanning several addresses. Valid when the USBOTGSS_GSTS[4] BUSERRADDRVLD field is 1. Cleared upon core reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUSERRADDRLO																															

Bits	Field Name	Description	Type	Reset
31:0	BUSERRADDRLO	BUSERRADDR[31:0]	R	0x0000 0000

Table 23-1227. Register Call Summary for Register USBOTGSS_GBUSERRADDRLO

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

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Table 23-1228. USBOTGSS_GBUSERRADDRHI

Address Offset	0x0000 C134		
Physical Address	0x4A03 C134	**Instance**	DWC_USB3
Description	Global Bus Error (non-precise) Address, MSbits: Base address of the first system bus DMA transfer that got a bus error. Note that each DMA transfer can contain several bursts, each spanning several addresses. Valid when the USBOTGSS_GSTS[4] BUSERRADDRVLD field is 1. Cleared upon core reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUSERRADDRHI																															

Bits	Field Name	Description	Type	Reset
31:0	BUSERRADDRHI	BUSERRADDR[63:32]	R	0x0000 0000

Table 23-1229. Register Call Summary for Register USBOTGSS_GBUSERRADDRHI

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1230. USBOTGSS_GPRTBIMAPLO

Address Offset	0x0000 C138		
Physical Address	0x4A03 C138	**Instance**	DWC_USB3
Description	Global port-to-SS USB instance mapping, low bits [31:0]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												BINUM1			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	BINUM1	SS USB instance number for port number 1 Application-programmable ID field	RW	0x0

Table 23-1231. Register Call Summary for Register USBOTGSS_GPRTBIMAPLO

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1232. USBOTGSS_GPRTBIMAPHI

Address Offset	0x0000 C13C		
Physical Address	0x4A03 C13C	**Instance**	DWC_USB3
Description	Global Port-to-SS USB Instance Mapping, high bits [63:32]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

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Bits	Field Name	Description	Type	Reset
31:0	RESERVED		R	0x0000 0000

Table 23-1233. Register Call Summary for Register USBOTGSS_GPRTBIMAPHI

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1234. USBOTGSS_GHWPARAMS0

Address Offset	0x0000 C140		
Physical Address	0x4A03 C140	**Instance**	DWC_USB3
Description	Global hardware parameters 0		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4 3	2 1 0
DWC_USB3_AWIDTH	DWC_USB3_SDWIDTH	DWC_USB3_MDWIDTH	DWC_USB3_SBUS_TYPE	DWC_USB3_MBUS_TYPE	DWC_USB3_MODE

Bits	Field Name	Description	Type	Reset
31:24	DWC_USB3_AWIDTH	Global hardware configuration parameter DWC_USB3_AWIDTH: (Master) Address Width (in bits)	R	0x20
23:16	DWC_USB3_SDWIDTH	Global hardware configuration parameter DWC_USB3_SDWIDTH: Slave Data Width (in bits)	R	0x20
15:8	DWC_USB3_MDWIDTH	Global hardware configuration parameter DWC_USB3_MDWIDTH: Master Data Width (in bits)	R	0x40
7:6	DWC_USB3_SBUS_TYPE	Global hardware configuration parameter DWC_USB3_SBUS_TYPE: (System bus) Slave type Read 0x0: Native slave	R	0x3
5:3	DWC_USB3_MBUS_TYPE	Global hardware configuration parameter DWC_USB3_MBUS_TYPE: (System bus) Master type Read 0x1: AXI (AMBA 3) master system bus	R	0x1
2:0	DWC_USB3_MODE	Global hardware configuration parameter DWC_USB3_MODE Read 0x2: Dual-role device (DRD) i.e. both device and host Read 0x1: Host-only Read 0x0: Device-only	R	0x2

Table 23-1235. Register Call Summary for Register USBOTGSS_GHWPARAMS0

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

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Table 23-1236. USBOTGSS_GHWPARAMS1

Address Offset	0x0000 C144		
Physical Address	0x4A03 C144	**Instance**	DWC_USB3
Description	Global hardware parameters 1		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DWC_USB3_RM_OPT_FEATURES	RESERVED	DWC_USB3_RAM_BUS_CLKS_SYNC	DWC_USB3_MAC_RAM_CLKS_SYNC	DWC_USB3_MAC_PHY_CLKS_SYNC	DWC_USB3_EN_PWROPT		DWC_USB3_SPRAM_TYP	DWC_USB3_NUM_RAMS		DWC_USB3_DEVICE_NUM_INT					DWC_USB3_ASPACEWIDTH				DWC_USB3_REQINFOWIDTH				DWC_USB3_DATAINFOWIDTH			DWC_USB3_BURSTWIDTH			DWC_USB3_IDWIDTH		

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30	DWC_USB3_RM_OPT_FEATURES	Global hardware configuration parameter DWC_USB3_RM_OPT_FEATURES: Remove Optional Features Read 0x1: Yes Read 0x0: No	R	0
29	RESERVED		R	0
28	DWC_USB3_RAM_BUS_CLKS_SYNC	Global hardware configuration parameter DWC_USB3_RAM_BUS_CLKS_SYNC: RAM vs. BUS clocks synchronous ? Read 0x1: Yes Read 0x0: No	R	0
27	DWC_USB3_MAC_RAM_CLKS_SYNC	Global hardware configuration parameter DWC_USB3_MAC_RAM_CLKS_SYNC: MAC vs. RAM clocks synchronous ? Read 0x1: Yes Read 0x0: No	R	0
26	DWC_USB3_MAC_PHY_CLKS_SYNC	Global hardware configuration parameter DWC_USB3_MAC_PHY_CLKS_SYNC: MAC vs. PHY clocks synchronous ? Read 0x1: Yes Read 0x0: No	R	0
25:24	DWC_USB3_EN_PWROPT	Global hardware configuration parameter DWC_USB3_EN_PWROPT: Power optimization Read 0x2: Clock hibernation Read 0x1: Clock Read 0x0: None	R	0x1
23	DWC_USB3_SPRAM_TYP	Global hardware configuration parameter DWC_USB3_SPRAM_TYP Read 0x1: Single-port RAM	R	1

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Bits	Field Name	Description	Type	Reset
22:21	DWC_USB3_NUM_RAMS	Global hardware configuration parameter DWC_USB3_NUM_RAMS: Number of internal RAMs Read 0x3: Three-RAM Read 0x2: Two-RAM Read 0x1: Single-RAM	R	0x2
20:15	DWC_USB3_DEVICE_NUM_INT	Global hardware configuration parameter DWC_USB3_DEVICE_NUM_INT: Number of interrupts (and event buffers) in device mode	R	0x01
14:12	DWC_USB3_ASPACEWIDTH	Global hardware configuration parameter DWC_USB3_ASPACEWIDTH	R	0x4
11:9	DWC_USB3_REQINFOWIDTH	Global hardware configuration parameter DWC_USB3_REQINFOWIDTH	R	0x4
8:6	DWC_USB3_DATAINFOWIDTH	Global hardware configuration parameter DWC_USB3_DATAINFOWIDTH	R	0x4
5:3	DWC_USB3_BURSTWIDTH	Global hardware configuration parameter DWC_USB3_BURSTWIDTH minus one, fixed to 8-1=7	R	0x7
2:0	DWC_USB3_IDWIDTH	Global hardware configuration parameter DWC_USB3_IDWIDTH minus 1 Note: Sets only the master port's ID width. Slave ID width is set by non-readable DWC_USB3_SIDWIDTH	R	0x3

Table 23-1237. Register Call Summary for Register USBOTGSS_GHWPARAMS1

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1238. USBOTGSS_GHWPARAMS2

Address Offset	0x0000 C148		
Physical Address	0x4A03 C148	**Instance**	DWC_USB3
Description	Global hardware parameters 2		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWC_USB3_USERID																															

Bits	Field Name	Description	Type	Reset
31:0	DWC_USB3_USERID	Global hardware configuration parameter DWC_USB3_USERID	R	0x0000 0000

Table 23-1239. Register Call Summary for Register USBOTGSS_GHWPARAMS2

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1240. USBOTGSS_GHWPARAMS3

Address Offset	0x0000 C14C		
Physical Address	0x4A03 C14C	**Instance**	DWC_USB3
Description	Global hardware parameters 3		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DWC_USB3_CACHE_TOTAL_XFER_RESOURCES							DWC_USB3_NUM_IN_EPS						DWC_USB3_NUM_EPS						DWC_USB3_ULPI_CARKIT	DWC_USB3_VENDOR_CTL_INTERFACE	RESERVED		DWC_USB3_HSPHY_DWIDTH		DWC_USB3_FSPHY_INTERFACE		DWC_USB3_HSPHY_INTERFACE		DWC_USB3_SSPHY_INTERFACE	

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30:23	DWC_USB3_CACHE_TOTAL_XFER_RESOURCES	Global hardware configuration parameter DWC_USB3_NUM_CACHE_TOTAL_XFER_RESOURCES: Cache total transfer resources	R	0x20
22:18	DWC_USB3_NUM_IN_EPS	Global hardware configuration parameter DWC_USB3_NUM_IN_EPS: Number of IN endpoints, with EP0 counting as one.	R	0x10
17:12	DWC_USB3_NUM_EPS	Global hardware configuration parameter DWC_USB3_NUM_EPS: Total number of endpoints (IN+OUT, with EP0 counting as 2 separate ones)	R	0x20
11	DWC_USB3_ULPI_CARKIT	Global hardware configuration parameter DWC_USB3_ULPI_CARKIT: ULPI (optional) car-kit mode implementation Read 0x1: CK mode implemented Read 0x0: CK mode not implemented	R	0
10	DWC_USB3_VENDOR_CTL_INTERFACE	Global hardware configuration parameter DWC_USB3_VENDOR_CTL_INTERFACE: (UTMI) Vendor Control i/f implementation Read 0x1: VC i/f implemented Read 0x0: VC i/f not implemented	R	0
9:8	RESERVED		R	0x0
7:6	DWC_USB3_HSPHY_DWIDTH	Global hardware configuration parameter DWC_USB3_HSPHY_DWIDTH: HS PHY data width Read 0x2: 8/16 bit UTMI @60/30 MHz Read 0x1: 16-bit UTMI @30 MHz Read 0x0: 8-bit UTMI @60 MHz	R	0x2
5:4	DWC_USB3_FSPHY_INTERFACE	Global hardware configuration parameter DWC_USB3_FSPHY_INTERFACE: Full (/Low)-Speed (serial) PHY interface Read 0x0: No FS/LS PHY i/f	R	0x0

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Bits	Field Name	Description	Type	Reset
3:2	DWC_USB3_HSPHY_INTERFACE	Global hardware configuration parameter DWC_USB3_HSPHY_INTERFACE: High-speed PHY interface Read 0x3: UTMI+ and ULPI i/f (mutually exclusive operation) Read 0x2: ULPI i/f Read 0x1: UTMI+ i/f Read 0x0: No HS (/FS/LS) PHY i/f	R	0x3
1:0	DWC_USB3_SSPHY_INTERFACE	Global hardware configuration parameter DWC_USB3_SSPHY_INTERFACE: Super Speed PHY interface. Read 0x1: PIPE i/f for USB3.0 Read 0x0: No SS PHY i/f	R	0x1

Table 23-1241. Register Call Summary for Register USBOTGSS_GHWPARAMS3

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1242. USBOTGSS_GHWPARAMS4

Address Offset	0x0000 C150		
Physical Address	0x4A03 C150	**Instance**	DWC_USB3
Description	Global hardware parameters 4		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWC_USB3_BMU_LSP_DEPTH				DWC_USB3_BMU_PTL_DEPTH				DWC_USB3_EN_ISOC_SUPT	RESERVED		DWC_USB3_NUM_SS_USB_INSTANCES					DWC_USB3_HIBER_SCRATCHBUFS			RESERVED					DWC_USB3_CACHE_TRBS_PER_TRANSFER							

Bits	Field Name	Description	Type	Reset
31:28	DWC_USB3_BMU_LSP_DEPTH	Global hardware configuration parameter DWC_USB3_BMU_LSP_DEPTH: Bus Management Unit / List Processor buffer depth	R	0x4
27:24	DWC_USB3_BMU_PTL_DEPTH	Global hardware configuration parameter DWC_USB3_BMU_PTL_DEPTH: Bus Management Unit / Protocol Transaction Layer buffer depth	R	0x8
23	DWC_USB3_EN_ISOC_SUPT	Global hardware configuration parameter DWC_USB3_EN_ISOC_SUPT: Enable Isochronous Support Read 0x1: Isochronous transfer type supported Read 0x0: Isochronous not supported	R	1

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Bits	Field Name	Description	Type	Reset
22:21	RESERVED		R	0x0
20:17	DWC_USB3_NUM_SS_USB_INSTANCES	Global hardware configuration parameter DWC_USB3_NUM_SS_USB_INSTANCES: Number of (independent) SS USB schedulers	R	0x1
16:13	DWC_USB3_HIBER_SCRATCHBUFS	Global hardware configuration parameter DWC_USB3_HIBER_SCRATCHBUFS: Number of 4-kbyte buffers required in system memory to store context during hibernation. Don't care since hibernation is not enabled.	R	0x1
12:6	RESERVED		R	0x00
5:0	DWC_USB3_CACHE_TRBS_PER_TRANSFER	Global hardware configuration parameter DWC_USB3_CACHE_TRBS_PER_TRANSFER	R	0x04

Table 23-1243. Register Call Summary for Register USBOTGSS_GHWPARAMS4

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1244. USBOTGSS_GHWPARAMS5

Address Offset	0x0000 C154		
Physical Address	0x4A03 C154	**Instance**	DWC_USB3
Description	Global hardware parameters 5		
Type	R		

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
RESERVED	DWC_USB3_DFQ_FIFO_DEPTH		DWC_USB3_DWQ_FIFO_DEPTH		DWC_USB3_TXQ_FIFO_DEPTH	DWC_USB3_RXQ_FIFO_DEPTH	DWC_USB3_BMU_BUSGM_DEPTH

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:22	DWC_USB3_DFQ_FIFO_DEPTH	Global hardware configuration parameter DWC_USB3_DFQ_FIFO_DEPTH	R	0x10
21:16	DWC_USB3_DWQ_FIFO_DEPTH	Global hardware configuration parameter DWC_USB3_DWQ_FIFO_DEPTH	R	0x20
15:10	DWC_USB3_TXQ_FIFO_DEPTH	Global hardware configuration parameter DWC_USB3_TXQ_FIFO_DEPTH	R	0x08
9:4	DWC_USB3_RXQ_FIFO_DEPTH	Global hardware configuration parameter DWC_USB3_RXQ_FIFO_DEPTH	R	0x08
3:0	DWC_USB3_BMU_BUSGM_DEPTH	Global hardware configuration parameter DWC_USB3_BMU_BUSGM_DEPTH	R	0x8

Table 23-1245. Register Call Summary for Register USBOTGSS_GHWPARAMS5

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

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Table 23-1246. USBOTGSS_GHWPARAMS6

Address Offset	0x0000 C158		
Physical Address	0x4A03 C158	**Instance**	DWC_USB3
Description	Global hardware parameters 6		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWC_USB3_RAM0_DEPTH																BUSFLTRSSUPPORT	BCSUPPORT	OTGSSSUPPORT	ADPSUPPORT	HNPSUPPORT	SRPSUPPORT	RESERVED		DWC_USB3_EN_FPGA	RESERVED	DWC_USB3_PSQ_FIFO_DEPTH					

Bits	Field Name	Description	Type	Reset
31:16	DWC_USB3_RAM0_DEPTH	Depth of RAM 0, in 64-bit words. RAM0 contains data cache and Rx FIFOs.	R	0x0B00
15	BUSFLTRSSUPPORT	Filtering (debounce) on OTG UTMI+ inputs (iddig,vbusvalid,avalid,bvalid,sessend). Reflects DWC_USB3_EN_OTG_FILTERS. Read 0x1: Implemented Read 0x0: Not implemented	R	0
14	BCSUPPORT	Battery Charger detection (ACA = Accessory Charger Adapter) support implemented internally. Reflects DWC_USB3_EN_BC. Note: Support can also be provided OUTSIDE the controller. Read 0x1: ACA supported by internal logic Read 0x0: ACA not supported, or supported by external logic	R	0
13	OTGSSSUPPORT	OTG SuperSpeed support (aka OTG3.0) Read 0x1: OTG3.0 supported Read 0x0: OTG3.0 not supported	R	0
12	ADPSUPPORT	OTG2.0 ADP (Attach Detection Protocol) support implemented internally. Reflects DWC_USB3_EN_ADP. Note: Support can also be provided OUTSIDE the controller. Read 0x1: ADP supported by internal logic Read 0x0: ADP not supported, or supported by external logic	R	0
11	HNPSUPPORT	OTG2.0 HNP (Host Negotiation Protocol) support. Set when in DRD mode. Read 0x1: Supported Read 0x0: Not supported	R	1
10	SRPSUPPORT	OTG2.0 SRP (Session Request Protocol) support. Read 0x1: Supported Read 0x0: Not supported	R	1
9:8	RESERVED		R	0x0
7	DWC_USB3_EN_FPGA	Global hardware configuration parameter DWC_USB3_EN_FPGA	R	0

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Bits	Field Name	Description	Type	Reset
6	RESERVED		R	0
5:0	DWC_USB3_PSQ_FIFO_DEPTH	Global hardware configuration parameter DWC_USB3_PSQ_FIFO_DEPTH	R	0x20

Table 23-1247. Register Call Summary for Register USBOTGSS_GHWPARAMS6

Super-Speed USB OTG Subsystem

- Core Space Remapping: [0]
- DWC_USB3 Register Summary: [1]

Table 23-1248. USBOTGSS_GHWPARAMS7

Address Offset	0x0000 C15C		
Physical Address	0x4A03 C15C	**Instance**	DWC_USB3
Description	Global hardware parameters 7		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWC_USB3_RAM2_DEPTH																DWC_USB3_RAM1_DEPTH															

Bits	Field Name	Description	Type	Reset
31:16	DWC_USB3_RAM2_DEPTH	Depth of RAM 2, in 64-bit words. RAM2 IS NOT IMPLEMENTED IN 2-RAM CONFIG: don't care	R	0x0308
15:0	DWC_USB3_RAM1_DEPTH	Depth of RAM 1, in 64-bit words. RAM1 contains Tx FIFOs.	R	0x0780

Table 23-1249. Register Call Summary for Register USBOTGSS_GHWPARAMS7

Super-Speed USB OTG Subsystem

- Core Space Remapping: [0]
- DWC_USB3 Register Summary: [1]

Table 23-1250. USBOTGSS_GDBGFIFOSPACE

Address Offset	0x0000 C160		
Physical Address	0x4A03 C160	**Instance**	DWC_USB3
Description	Global debug FIFO/queue space available		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPACE_AVAILABLE																RESERVED								FIFOQUEUESELECT_PORTSELECT							

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Bits	Field Name	Description	Type	Reset
31:16	SPACE_AVAILABLE	Space available (in the selected FIFO/queue), 64-bit words	R	0x0042
15:8	RESERVED		R	0x00
7:0	FIFOQUEUESELECT_PORTSELECT	FIFO/queue select or port select. Default value, when indicated, is the space available when empty, that is, the size of the FIFO/queue. PORTSELECT[3:0] selects the port number when accessing the USBOTGSS_GDBGLTSSM register. FIFOQUEUESELECT[7:0]: 0x3F: RX FIFO number 31 = SELECT-32 0x7F: RxReqQ number 31 = SELECT-96 0xA1: EventQ 0x0: TxFIFO number 0 = SELECT 0x1F: TxFIFO number 31 = SELECT 0x80: RxInfoQ number 0 = SELECT-128 0x5F: TxReqQ number 31 = SELECT-64 0xA0: DescFetchQ (default:16) 0x9F: RxInfoQ number 31 = SELECT-128 0x60: RxReqQ number 0 = SELECT-96 0x40: TxReqQ number 0 = SELECT-64 0x20: RxFIFO number 0 = SELECT-32 0xA2: ProtocolStatusQ (default: 32)	RW	0x00

Table 23-1251. Register Call Summary for Register USBOTGSS_GDBGFIFOSPACE

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1]

Table 23-1252. USBOTGSS_GDBGLTSSM

Address Offset	0x0000 C164		
Physical Address	0x4A03 C164	**Instance**	DWC_USB3
Description	Global debug LTSSM Port number is defined by USBOTGSS_GDBGFIFOSPACE[3:0] PORTSELECT		
Type	R		

31 30	29	28	27	26	25 24	23 22	21 20 19 18	17	16	15	14	13 12 11	10 9	8	7 6	5 4	3 2	1	0
RESERVED	PORTSHUTDOWN	PORTSWAPPING	PORTDIRECTION	LTDBTIMEOUT	LTDBLINKSTATE		LTDBSUBSTATE	ELASTICBUFFERMODE	TXELECIDLE	RXPOLARITY	TXDETRXLOOPBACK	LTDBPHYCMDSTATE	POWERDOWN	RXEQTRAIN	TXDEEMPHASIS	LTDBCLKSTATE	TXSWING	RXTERMINATION	TXONESZEROS

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	PORTSHUTDOWN		R	0
28	PORTSWAPPING		R	0

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Bits	Field Name	Description	Type	Reset
27	PORTDIRECTION	Current direction of the port. Read 0x1: Downstream (host) port Read 0x0: Upstream (device) port	R	0
26	LTDBTIMEOUT	LTSSM Debug Timeout	R	0
25:22	LTDBLINKSTATE	LTSSM Debug: Link State Read 0x3: U3 low-power state Read 0x4: SS.Disabled Read 0xB: Loopback Read 0x2: U2 low-power state Read 0x0: U0 active state Read 0xA: Compliance mode Read 0x6: SS.Inactive Read 0x1: U1 low-power state Read 0x8: Recovery Read 0x7: Polling Read 0x9: Hot Reset Read 0x5: Rx.Detect	R	0x4
21:18	LTDBSUBSTATE	LTSSM Debug: Link Sub-State. Note that the actual reset value (0x0) changes before the register can be read out.	R	0x2
17	ELASTICBUFFERMODE	Debug PIPE Status: ElasticBufferMode	R	0
16	TXELECIDLE	Debug PIPE Status: TxElecIdle	R	1
15	RXPOLARITY	Debug PIPE Status: RxPolarity	R	0
14	TXDETRXLOOPBACK	Debug PIPE Status: TxDetRxLoopback	R	0
13:11	LTDBPHYCMDSTATE	LTSSM Debug Phy Command State. Read 0x3: Delay Pipe_PowerDown P0 -> P1/P2/P3 request Read 0x4: Delay for internal logic Read 0x2: Wait for Phy_Status (Receiver detection) Read 0x0: PHY command state is in IDLE. No PHY request pending Read 0x1: Request to start Receiver detection Read 0x5: Wait for Phy_Status(Power state change request)	R	0x0
10:9	POWERDOWN	Debug PIPE Status: PowerDown	R	0x2
8	RXEQTRAIN	Debug PIPE Status: RxEqTrain	R	0
7:6	TXDEEMPHASIS	Debug PIPE Status: TxDeemphasis	R	0x1
5:3	LTDBCLKSTATE	LTSSM Debug Clock State Read 0x3: PHY is in P3 and PCLK is not running Read 0x4: P3 exit request to PHY Read 0x2: Wait for Phy_Status (P3 request) Read 0x0: PHY is in non-P3 state and PCLK is running Read 0x1: P3 entry request to PHY Read 0x5: Wait for Phy_Status (P3 exit request)	R	0x0
2	TXSWING	Debug PIPE Status: TxSwing	R	0
1	RXTERMINATION	Debug PIPE Status: RxTermination	R	0
0	TXONESZEROS	Debug PIPE Status: TxOnesZeros	R	0

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Table 23-1253. Register Call Summary for Register USBOTGSS_GDBGLTSSM

Super-Speed USB OTG Subsystem

- Manual Far-end Receiver Detection in USB3 Host Mode: [0]
- Observability Debug Interface: [1]
- DWC_USB3 Register Summary: [2]
- DWC_USB3 Register Description: [3]

Table 23-1254. USBOTGSS_GDBGLSPMUX

Address Offset	0x0000 C170		
Physical Address	0x4A03 C170	**Instance**	DWC_USB3
Description	Global debug LSP MUX, for internal use only		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRACEPORTMUXSEL								RESERVED		HOSTSELECT						DEVSELECT				EPSELECT			

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:16	TRACEPORTMUXSEL	Select the 64-bit analyzer trace vector. Not sensitive to warm reset (i.e. including software reset), only to power-on reset. 0x3F: Trace vector is forced to all-zero	RW	0x00
15:14	RESERVED		R	0x0
13:8	HOSTSELECT	Host LSP Select[13:8]. Valid only in Host mode.	RW	0x00
7:4	DEVSELECT	Host LSP Select[7:4] in Host mode Device LSP Select in Device mode	RW	0x0
3:0	EPSELECT	Host LSP Select[3:0] in Host mode Device LSP Select in Device mode	RW	0x0

Table 23-1255. Register Call Summary for Register USBOTGSS_GDBGLSPMUX

Super-Speed USB OTG Subsystem

- Observability Debug Interface: [0] [1]
- DWC_USB3 Register Summary: [2]
- USBOTGSS_WRAPPER Register Description: [3] [4]

Table 23-1256. USBOTGSS_GDBGLSP

Address Offset	0x0000 C174		
Physical Address	0x4A03 C174	**Instance**	DWC_USB3
Description	Global debug LSP, for internal use only		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG																															

Bits	Field Name	Description	Type	Reset
31:0	DEBUG	LSP debug information	R	0x0000 0000

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Table 23-1257. Register Call Summary for Register USBOTGSS_GDBGLSP

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1258. USBOTGSS_GDBGEPINFO0

Address Offset	0x0000 C178		
Physical Address	0x4A03 C178	**Instance**	DWC_USB3
Description	Global debug endpoint information register 0		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG																															

Bits	Field Name	Description	Type	Reset
31:0	DEBUG	EP debug information	R	0x0000 0000

Table 23-1259. Register Call Summary for Register USBOTGSS_GDBGEPINFO0

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1260. USBOTGSS_GDBGEPINFO1

Address Offset	0x0000 C17C		
Physical Address	0x4A03 C17C	**Instance**	DWC_USB3
Description	Global debug endpoint information register 1		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG																															

Bits	Field Name	Description	Type	Reset
31:0	DEBUG	EP debug information	R	0x0000 0000

Table 23-1261. Register Call Summary for Register USBOTGSS_GDBGEPINFO1

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1262. USBOTGSS_GPRTBIMAP_HSLO

Address Offset	0x0000 C180		
Physical Address	0x4A03 C180	**Instance**	DWC_USB3
Description	Global port to USB instance mapping register, high-speed, low bits [31:0]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												BINUM1			

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Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	BINUM1	HS USB instance number for port number 1 Application-programmable ID field	RW	0x0

Table 23-1263. Register Call Summary for Register USBOTGSS_GPRTBIMAP_HSLO

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1264. USBOTGSS_GPRTBIMAP_HSHI

Address Offset	0x0000 C184		
Physical Address	0x4A03 C184	**Instance**	DWC_USB3
Description	Global port to USB instance mapping register, high-speed, high bits [63:32]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED		R	0x0000 0000

Table 23-1265. Register Call Summary for Register USBOTGSS_GPRTBIMAP_HSHI

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1266. USBOTGSS_GPRTBIMAP_FSLO

Address Offset	0x0000 C188		
Physical Address	0x4A03 C188	**Instance**	DWC_USB3
Description	Global port to USB instance mapping register, full/low-speed, low bits [31:0]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												BINUM1			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3:0	BINUM1	FS USB instance number for port number 1 Application-programmable ID field	RW	0x0

Table 23-1267. Register Call Summary for Register USBOTGSS_GPRTBIMAP_FSLO

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1268. USBOTGSS_GPRTBIMAP_FSHI

Address Offset	0x0000 C18C		
Physical Address	0x4A03 C18C	**Instance**	DWC_USB3
Description	Global port to USB instance mapping register, full/low-speed, high bits [63:32]		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	RESERVED		R	0x0000 0000

Table 23-1269. Register Call Summary for Register USBOTGSS_GPRTBIMAP_FSHI

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1270. USBOTGSS_GUSB2PHYCFG

Address Offset	0x0000 C200		
Physical Address	0x4A03 C200	**Instance**	DWC_USB3
Description	Global USB2 (UTMI/ULPI) PHY configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSOFTRST	RESERVED												ULPIEXTVBUSINDICATOR	ULPIEXTVBUSDRV	ULPICLKSUSM	ULPIAUTORES	RESERVED	USBTRDTIM					RESERVED	ENBLSLPM	PHYSEL	SUSPHY	FSINTF	ULPI_UTMI_SEL	PHYIF	TOUTCAL		

Bits	Field Name	Description	Type	Reset
31	PHYSOFTRST	PHY Soft Reset. Active-high, fully static software reset for UTMI USB2 transceiver. 0x0: Reset inactive. 0x1: Reset active.	RW	0
30:19	RESERVED		R	0x000
18	ULPIEXTVBUSINDICATOR	ULPI External VBUS Indicator Indicates the ULPI PHY VBUS over-current indicator. 0x0: PHY uses an internal VBUS valid comparator. 0x1: PHY uses an external VBUS valid comparator.	RW	0
17	ULPIEXTVBUSDRV	ULPI External VBUS Drive Selects supply source to drive 5V on VBUS, in the ULPI PHY. 0x0: PHY drives VBUS with internal charge pump 0x1: PHY drives VBUS with an external supply.	RW	0
16	ULPICLKSUSM	Sets the ClockSuspendM bit in the Interface Control register on the ULPI PHY. Applicable only in serial FS/LS or Carkit modes. NOT APPLICABLE	RW	0
15	ULPIAUTORES	ULPI Auto Resume. Sets the AutoResume bit in Interface Control register on the ULPI PHY. 0x0: PHY does not use the AutoResume feature. 0x1: PHY uses the AutoResume feature.	RW	0
14	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
13:10	USBTRDTIM	USB 2.0 Turnaround Time, in PHY clock cycles. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM).	RW	0x9
9	RESERVED		R	0
8	ENBLSLPM	Enable UTMI Sleep. Controls assertion of utmi_sleep_n, utmi_l1_suspend_n outputs to the PHY when in the L1 state. 0x0: utmi_sleep_n, utmi_l1_suspend_n assertion from the core not transferred to the external PHY. 0x1: utmi_sleep_n, utmi_l1_suspend_n assertion from the core transferred to the external PHY.	RW	1
7	PHYSEL	PHY Select. (HS vs. serial): Unused, since serial PHY is not supported.	R	0
6	SUSPHY	Suspend enable for USB2.0 HS/FS/LS PHY (ULPI or UTMI). Set to 1 only after core initialization is complete. 0x0: USB2.0 PHY not placed in Suspend mode 0x1: USB2.0 PHY enters Suspend mode if port is suspended or unused.	RW	0
5	FSINTF	Full-Speed Serial Interface Select. UNUSED.	R	0
4	ULPI_UTMI_SEL	ULPI or UTMI+ Select 0x0: UTMI+ Interface 0x1: ULPI Interface	RW	0
3	PHYIF	PHY Interface. DO NOT USE. If UTMI+ is selected, configures 8- or 16-bit interface. If ULPI is selected, configures SDR or DDR mode. 0x0: 8-bit UTMI @60 MHz / SDR (12-pin) ULPI 0x1: 16-bit UTMI @30 MHz, not supported / DDR (8-pin) ULPI, not supported	RW	0
2:0	TOUTCAL	HS/FS Timeout Calibration. The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time factor; this factor is added to the high-speed/full-speed interpacket timeout duration in the core to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the linestate condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: 8 bit times per 60-MHz PHY clock cycle Full-speed operation: (depending on clock speed) 0.2 bit times per 60-MHz PHY clock cycle 0.25 bit times per 48-MHz PHY clock cycle	RW	0x0

Table 23-1271. Register Call Summary for Register USBOTGSS_GUSB2PHYCFG

Super-Speed USB OTG Subsystem

- USB3.0 OTG DRD Alternative: [0]
- USB2.0 OTG DRD Alternative: [1]
- DWC_USB3 Register Summary: [2]
- DWC_USB3 Register Description: [3]

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Table 23-1272. USBOTGSS_GUSB2PHYACC

Address Offset	0x0000 C280		
Physical Address	0x4A03 C280	**Instance**	DWC_USB3
Description	Global USB2 PHY access		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					DISULPIDRVR	NEWREGREQ	VSTSDONE	VSTSBSY	REGWR	REGADDR						RESERVED	EXTREGADDR							REGDATA							

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	DISULPIDRVR	Disable ULPI drivers, for carkit mode. Auto-cleared. NOT USED.	R	0
25	NEWREGREQ	New register request. Auto-cleared. Write 0x0: No action Write 0x1: Request new register access Read 0x1: Access request pending Read 0x0: No request pending	RW	0
24	VSTSDONE	VStatus Done Read 0x1: access is done. Read 0x0: Application has set the NEWREGREQ bit, access is not done.	R	0
23	VSTSBSY	VStatus busy Read 0x1: Access is in progress. Read 0x0: Access is done.	R	0
22	REGWR	Register write 0x0: Read 0x1: Write	RW	0
21:16	REGADDR	Register address ULPI PHY register address for immediate PHY register set access. Set to 6'h2F for extended PHY register set access.	RW	0x00
15:14	RESERVED		RW	0x0
13:8	EXTREGADDR	ULPI: PHY extended register address. UTMI+: Unused	RW	0x00
7:0	REGDATA	Register data (read and write data)	RW	0x00

Table 23-1273. Register Call Summary for Register USBOTGSS_GUSB2PHYACC

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1274. USBOTGSS_GUSB3PIPECTL

Address Offset	0x0000 C2C0		
Physical Address	0x4A03 C2C0	**Instance**	DWC_USB3
Description	Global USB3 PIPE control		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYSOFTRST	RESERVED			UX_EXIT_IN_PX	PING_ENHANCEMENT_EN	U1U2EXITFAIL_TO_RECOV	REQUEST_P1P2P3	STARTRXDETU3RXDET	DISRXDETU3RXDET	P1P2P3DELAY			DELAYP0TOP1P2P3	SUSPENDENABLE	DATWIDTH		ABORTRXDETINU2	SKIPRXDET	LFPSP0ALGN	P3P2TRANOK	P3EXSIGP2	LFPSFILT	RESERVED		TXSWING	TXMARGIN			TXDEEMPHASIS		ELASTICBUFFERMODE

Bits	Field Name	Description	Type	Reset
31	PHYSOFTRST	PHY Soft Reset. Active-high, fully static software reset for PIPE USB3 transceiver. 0x0: Reset inactive. 0x1: Reset active.	RW	0
30:28	RESERVED		RW	0x0
27	UX_EXIT_IN_PX	Workaround for SS PHY injecting a glitch on RxElecIdle while receiving Ux exit LFPS, and PowerDown change is in progress. 0x0: U1/U2/U3 exit done in PHY power state P0 0x1: U1/U2/U3 exit done in PHY power state P1/P2/P3 respectively	RW	0
26	PING_ENHANCEMENT_EN	Ping Enhancement Enable: Extended downstream port U1 ping receive timeout. Invalid for Upstream port. 0x0: U1 ping rx timeout is 300 ms (default) 0x1: U1 ping rx timeout extended to 500 ms	RW	0
25	U1U2EXITFAIL_TO_RECOV	Enhancement to prevent interoperability issue in case of incorrect LFPS handshake by the remote link. 0x0: LTSSM goes to SS Inactive when U1/U2 LFPS handshake fails (default) 0x1: LTSSM goes to Recovery when U1/U2 LFPS handshake fails, and to SS.Inactive only if recovery fails.	RW	0
24	REQUEST_P1P2P3	Control the systematic request of P1/P2/P3 for U1/U2/U3 0x0: No P1/P2/P3 change request upon immediate Ux exit (remotely or locally initiated) 0x1: Always request transition from P0 to P1/P2/P3 on PHY during transition from U0 to U1/U2/U3 on USB.	RW	0
23	STARTRXDETU3RXDET	Manual control for periodic Rx detection required in U3 and Rx.Detect, host mode. Write 0x0: No action Write 0x1: Trigger immediate Rx detection on transmitter.	RW	0
22	DISRXDETU3RXDET	Disable the HW-scheduled periodic Rx detection required in U3 and SS.Disabled, for host mode. 0x0: Rx detection is HW-scheduled every 12/100 ms when in SS.Disabled / U3 LTSSM state, respectively. This requires the suspend clock to run permanently. 0x1: HW-scheduled Rx detection is disabled, and must be SW-controlled using DoRxDetect.	RW	0
21:19	P1P2P3DELAY	If DelayP0toP1P2P3=1, delays the transition to P1/P2/P3 when entering U1/U2/U3 until P1P2P3Delay*8b10b errors occur, or RxValid=0 on PIPE.	RW	0x0

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Bits	Field Name	Description	Type	Reset
18	DELAYP0TOP1P2P3	Delay PHY change from P0 to P1/P2/P3 when link state changes from U0 to U1/U2/U3, respectively. 0x0: When entering U1/U2/U3, transition to P1/P2/P3 without checking RxElecIlde, RxValid on PIPE. 0x1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until RxElecIlde=1, RxValid=0 on PIPE	RW	1
17	SUSPENDENABLE	Suspend Enable for USB3.0 SS PHY. Set to 1 only after core initialization is complete. 0x0: USB3.0 PHY not placed in Suspend mode 0x1: USB 3.0 PHY enters Suspend mode when conditions are valid.	RW	0
16:15	DATWIDTH	PIPE Data Width (input from phy: refer to PIPE standard) Field updated to the input's value immediately after reset. Read 0x2: PIPE data is 8 bit @500 MHz Read 0x1: PIPE data is 16 bit @250 MHz Read 0x0: PIPE data is 32 bit @125 MHz	R	0x0
14	ABORTRXDETINU2	Abort Rx Detect in U2. For Downstream port only. 0x0: Receiver detection not aborted 0x1: When in U2, receiver detection will be aborted if U2 exit LFPS is received.	RW	0
13	SKIPRXDET	Skip Rx Detect. When set, the core skips Rx Detection if PIPE signal "RxElecIdle" is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation.	RW	0
12	LFPSP0ALGN	LFPS P0 Align. When set to 1: - The core deasserts LFPS transmission on the clock edge that it requests PHY power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. - The core requests symbol transmission two pipe_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state. 0x0: Default 0x1: DO NOT USE	RW	0
11	P3P2TRANOK	P3-to-P2 Transitions OK 0x0: P0 is always entered as an intermediate state during transitions between P2 and P3, as defined in the PIPE specification. 0x1: Core transitions directly from PHY power state P2 to P3 or from state P3 to P2. Illegal as per PIPE, use only if PHY cannot do LFPS in P3.	RW	0
10	P3EXSIGP2	PHY power state behaviour upon U3 exit handshake. 0x0: Default behaviour 0x1: Go to P2 before attempting a U3 exit handshake.	RW	0
9	LFPSFILT	LFPS Filter. When set, filter LFPS reception with PIPE "RxValid" signal in PHY power state P0, that is, ignore LFPS reception from the PHY unless both PIPE signals "RxElecIdle" and "RxValid" are deasserted.	RW	0
8:7	RESERVED		R	0x0
6	TXSWING	Tx Swing (output to PHY: refer to PIPE standard)	RW	0
5:3	TXMARGIN	Tx Margin[2:0] (output to PHY: refer to PIPE standard)	RW	0x0
2:1	TXDEEMPHASIS	Tx Deemphasis (output to PHY: refer to PIPE standard) The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode.	RW	0x1

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Bits	Field Name	Description	Type	Reset
0	ELASTICBUFFERMODE	Elastic Buffer Mode (output to PHY: refer to PIPE standard)	RW	0

Table 23-1275. Register Call Summary for Register USBOTGSS_GUSB3PIPECTL

Super-Speed USB OTG Subsystem

- Manual Far-end Receiver Detection in USB3 Host Mode: [0] [1] [2] [3] [4]
- DWC_USB3 Register Summary: [5]
- DWC_USB3 Register Description: [6] [7]

Table 23-1276. USBOTGSS_GTXFIFOSIZ0

Address Offset	0x0000 C300		
Physical Address	0x4A03 C300	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 0: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x0000
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0042

Table 23-1277. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ0

Super-Speed USB OTG Subsystem

- Core Space Remapping: [0] [1] [2]
- DWC_USB3 Register Summary: [3]

Table 23-1278. USBOTGSS_GTXFIFOSIZ1

Address Offset	0x0000 C304		
Physical Address	0x4A03 C304	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 1: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x0042
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0184

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Table 23-1279. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ1

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1280. USBOTGSS_GTXFIFOSIZ2

Address Offset	0x0000 C308		
Physical Address	0x4A03 C308	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 2: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x01C6
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0184

Table 23-1281. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ2

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1282. USBOTGSS_GTXFIFOSIZ3

Address Offset	0x0000 C30C		
Physical Address	0x4A03 C30C	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 3: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x034A
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0184

Table 23-1283. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ3

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

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Table 23-1284. USBOTGSS_GTXFIFOSIZ4

Address Offset	0x0000 C310		
Physical Address	0x4A03 C310	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 4: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x04CE
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0184

Table 23-1285. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ4

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1286. USBOTGSS_GTXFIFOSIZ5

Address Offset	0x0000 C314		
Physical Address	0x4A03 C314	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 5: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x0652
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1287. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ5

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1288. USBOTGSS_GTXFIFOSIZ6

Address Offset	0x0000 C318		
Physical Address	0x4A03 C318	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 6: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x0665
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1289. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ6

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1290. USBOTGSS_GTXFIFOSIZ7

Address Offset	0x0000 C31C		
Physical Address	0x4A03 C31C	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 7: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x0678
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1291. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ7

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1292. USBOTGSS_GTXFIFOSIZ8

Address Offset	0x0000 C320		
Physical Address	0x4A03 C320	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 8: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

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Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x068B
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1293. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ8

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1294. USBOTGSS_GTXFIFOSIZ9

Address Offset	0x0000 C324		
Physical Address	0x4A03 C324	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 9: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x069E
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1295. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ9

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1296. USBOTGSS_GTXFIFOSIZ10

Address Offset	0x0000 C328		
Physical Address	0x4A03 C328	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 10: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x06B1

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Bits	Field Name	Description	Type	Reset
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1297. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ10

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1298. USBOTGSS_GTXFIFOSIZ11

Address Offset	0x0000 C32C		
Physical Address	0x4A03 C32C	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 11: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x06C4
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1299. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ11

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1300. USBOTGSS_GTXFIFOSIZ12

Address Offset	0x0000 C330		
Physical Address	0x4A03 C330	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 12: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x06D7
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

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Table 23-1301. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ12

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1302. USBOTGSS_GTXFIFOSIZ13

Address Offset	0x0000 C334		
Physical Address	0x4A03 C334	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 13: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x06EA
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1303. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ13

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1304. USBOTGSS_GTXFIFOSIZ14

Address Offset	0x0000 C338		
Physical Address	0x4A03 C338	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 14: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x06FD
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1305. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ14

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

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Table 23-1306. USBOTGSS_GTXFIFOSIZ15

Address Offset	0x0000 C33C		
Physical Address	0x4A03 C33C	**Instance**	DWC_USB3
Description	Global Transmit FIFO Size 15: FIFO mapping in RAM1, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXFSTADDR																TXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	TXFSTADDR	Transmit FIFO RAM start address, in 64-bit RAM words. 0x0: Minimum (RAM1 base) 0x760: Maximum (up to RAM1 depth - 32)	RW	0x0710
15:0	TXFDEP	Transmit FIFO depth, in 64-bit RAM words. 0x780: Maximum depth (the whole buffer) 0x20: Minimum depth	RW	0x0013

Table 23-1307. Register Call Summary for Register USBOTGSS_GTXFIFOSIZ15

Super-Speed USB OTG Subsystem

- Core Space Remapping: [0] [1]
- DWC_USB3 Register Summary: [2]

Table 23-1308. USBOTGSS_GRXFIFOSIZ0

Address Offset	0x0000 C380		
Physical Address	0x4A03 C380	**Instance**	DWC_USB3
Description	Global Receive FIFO Size 0: FIFO mapping in RAM0, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXFSTADDR																RXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	RXFSTADDR	Receive FIFO RAM Start Address, in 64-bit RAM words. 0x0: Minimum (RAM0 base) 0x3C2: Maximum (base of descriptor cache in RAM0 - 32)	RW	0x071E
15:0	RXFDEP	Receive FIFO Depth, in 64-bit RAM words 0x20: Minimum depth 0x3E2: Maximum depth (the whole buffer)	RW	0x0185

Table 23-1309. Register Call Summary for Register USBOTGSS_GRXFIFOSIZ0

Super-Speed USB OTG Subsystem

- Core Space Remapping: [0] [1] [2]
- DWC_USB3 Register Summary: [3]

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Table 23-1310. USBOTGSS_GRXFIFOSIZ1

Address Offset	0x0000 C384		
Physical Address	0x4A03 C384	**Instance**	DWC_USB3
Description	Global receive FIFO size 1: FIFO mapping in RAM0, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXFSTADDR																RXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	RXFSTADDR	Receive FIFO RAM Start Address, in 64-bit RAM words. 0x0: Minimum (RAM0 base) 0x3C2: Maximum (base of descriptor cache in RAM0 - 32)	RW	0x08A3
15:0	RXFDEP	Receive FIFO Depth, in 64-bit RAM words 0x20: Minimum depth 0x3E2: Maximum depth (the whole buffer)	RW	0x0000

Table 23-1311. Register Call Summary for Register USBOTGSS_GRXFIFOSIZ1

Super-Speed USB OTG Subsystem

- Core Space Remapping: [0]
- DWC_USB3 Register Summary: [1]

Table 23-1312. USBOTGSS_GRXFIFOSIZ2

Address Offset	0x0000 C388		
Physical Address	0x4A03 C388	**Instance**	DWC_USB3
Description	Global receive FIFO size 2: FIFO mapping in RAM0, from staddr to (staddr+dep-1)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXFSTADDR																RXFDEP															

Bits	Field Name	Description	Type	Reset
31:16	RXFSTADDR	Receive FIFO RAM Start Address, in 64-bit RAM words. 0x0: Minimum (RAM0 base) 0x3C2: Maximum (base of descriptor cache in RAM0 - 32)	RW	0x08A3
15:0	RXFDEP	Receive FIFO Depth, in 64-bit RAM words 0x20: Minimum depth 0x3E2: Maximum depth (the whole buffer)	RW	0x0000

Table 23-1313. Register Call Summary for Register USBOTGSS_GRXFIFOSIZ2

Super-Speed USB OTG Subsystem

- Core Space Remapping: [0] [1] [2]
- DWC_USB3 Register Summary: [3]

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Table 23-1314. USBOTGSS_GEVNTADRLO

Address Offset	0x0000 C400		
Physical Address	0x4A03 C400	**Instance**	DWC_USB3
Description	Global event address: Lower 32 bits of start address of the external memory for the event buffer. During operation, hardware does not update this address.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVNTADRLO																															

Bits	Field Name	Description	Type	Reset
31:0	EVNTADRLO	EVNTADR[31:0]	RW	0x0000 0000

Table 23-1315. Register Call Summary for Register USBOTGSS_GEVNTADRLO

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1316. USBOTGSS_GEVNTADRHI

Address Offset	0x0000 C404		
Physical Address	0x4A03 C404	**Instance**	DWC_USB3
Description	Global event address: Upper 32 bits of start address of the external memory for the event buffer. During operation, hardware does not update this address.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVNTADRHI																															

Bits	Field Name	Description	Type	Reset
31:0	EVNTADRHI	EVNTADR[64:32]	RW	0x0000 0000

Table 23-1317. Register Call Summary for Register USBOTGSS_GEVNTADRHI

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1318. USBOTGSS_GEVNTSIZ

Address Offset	0x0000 C408		
Physical Address	0x4A03 C408	**Instance**	DWC_USB3
Description	Global event buffer size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVNTINTRPTMASK	RESERVED															EVENTSIZ															

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Bits	Field Name	Description	Type	Reset
31	EVNTINTRPTMASK	Event interrupt mask Prevents the interrupt from being generated when set to 1 The events are queued wven when the mask is set.	RW	0
30:16	RESERVED		R	0x0000
15:0	EVENTSIZ	Event buffer size Size of the event buffer in bytes; must be a multiple of 4. Programmed by software once during initialization.	RW	0x0000

Table 23-1319. Register Call Summary for Register USBOTGSS_GEVNTSIZ

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1320. USBOTGSS_GEVNTCOUNT

Address Offset	0x0000 C40C		
Physical Address	0x4A03 C40C	**Instance**	DWC_USB3
Description	Global event buffer count		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVNTCOUNT															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	EVNTCOUNT	Event count When read, returns the number of valid events in the event buffer in bytes When written, hardware decrements the count by the value written. The interrupt remains active while count is not 0.	RW	0x0000

Table 23-1321. Register Call Summary for Register USBOTGSS_GEVNTCOUNT

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1322. USBOTGSS_GHWPARAMS8

Address Offset	0x0000 C600		
Physical Address	0x4A03 C600	**Instance**	DWC_USB3
Description	Global hardware parameters 8		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWC_USB3_DCACHE_DEPTH_INFO																															

Bits	Field Name	Description	Type	Reset
31:0	DWC_USB3_DCACHE_DEPTH_INFO	Depth of data cache, in 64-bit words (fixed). The cache occupies RAM0 from word 0 to DCACHE_DEPTH_INFO-1: Rx FIFOs shall be mapped from word DCACHE_DEPTH_INFO to RAM0_DEPTH-1.	R	0x0000 071E

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Table 23-1323. Register Call Summary for Register USBOTGSS_GHWPARAMS8

Super-Speed USB OTG Subsystem

- Core Space Remapping: [0]
- DWC_USB3 Register Summary: [1]

Table 23-1324. USBOTGSS_GHWPARAMS9

Address Offset	0x0000 C604		
Physical Address	0x4A03 C604	**Instance**	DWC_USB3
Description	Global hardware parameters 9		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GHWPARAMS9																															

Bits	Field Name	Description	Type	Reset
31:0	GHWPARAMS9	NOT USED	R	0x0000 0000

Table 23-1325. Register Call Summary for Register USBOTGSS_GHWPARAMS9

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1326. USBOTGSS_DCFG

Address Offset	0x0000 C700		
Physical Address	0x4A03 C700	**Instance**	DWC_USB3
Description	Device configuration: Configures the core in device mode after power-on or after certain control commands or enumeration. Does not change after initial programming.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								IGNORESTREAMPP	LPMCAP	NUMP						INTRNUM				PERFRINT		DEVADDR								DEVSPD	

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		RW	0x00
23	IGNORESTREAMPP	Ignore Packet-Pending for Stream management. From stream-capable bulk endpoints only. 0x0: When Data Packet is received with PP=0 (OUT EP) or ACK is received with NumP=0 and PP=0 (IN EP), search another stream (CStream) to initiate to the host. This is non-optimal a) When host sets PP=0 even though it has not finished with the stream, and b) if the EP is configured with one transfer resource i.e. can't initiate another stream. 0x1: PP is ignored for stream selection, no another stream is searched when DP is received with (PP=0) or ACK with (NumP=0, PP=0), to enhance performance if system bus bandwidth is low or host responds to ERDY quickly.	RW	0

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Bits	Field Name	Description	Type	Reset
22	LPMCAP	Link Power Management (LPM) Capability. 0x0: not LPM capable: device cannot respond to LPM transactions. 0x1: LPM capable: device shall respond to LPM transactions.	RW	0
21:17	NUMP	Number of Receive Buffers. Indicates number of receive buffers to be reported in ACK TP. Value based on RxFIFO size, buffer sizes programmed in descriptors, and system latency.	RW	0x04
16:12	INTRNUM	Interrupt Number. Interrupt/EventQ number on which non-endpoint-specific device related interrupts (see DEVT) are generated.	RW	0x00
11:10	PERFRINT	Periodic Frame Interrupt. Time within a (micro)frame when the application must be notified using the End Of Periodic Frame Interrupt, which can be used to determine if all the periodic (isochronous, interrupt) traffic for that (micro)frame is complete. 0x0: 80% of the (micro)frame interval 0x1: 85% of the (micro)frame interval 0x3: 95% of the (micro)frame interval 0x2: 90% of the (micro)frame interval	RW	0x2
9:3	DEVADDR	Device Address. Configure upon set-address USB command, clear to 0 upon USB reset. 0x0: Default address for unenumerated device.	RW	0x00
2:0	DEVSPD	Device Speed: USB speed at which the core should connect. Actual bus speed is determined only after chirp completion, based on the speed of the attached USB host. 0x0: High Speed (HS): 480 Mbit/s 0x1: Full Speed (FS): 12 Mbit/s 0x3: Full Speed (FS): 12 Mbit/s on serial PHY: NOT SUPPORTED 0x4: Super Speed (SS): 5 Gbit/s 0x2: Low Speed (LS): 1.5 Mbit/s on serial PHY: NOT SUPPORTED	RW	0x0

Table 23-1327. Register Call Summary for Register USBOTGSS_DCFG

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1] [2] [3] [4]

Table 23-1328. USBOTGSS_DCTL

Address Offset	0x0000 C704		
Physical Address	0x4A03 C704	**Instance**	DWC_USB3
Description	Device control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RUNSTOP	CSFTRST	RESERVED	HIRDTHRES_4	HIRDTHRES_TIME				APPL1RES	RESERVED			KEEPCONNECT	L1HIBERNATIONEN	CRS	CSS	RESERVED			INITU2ENA	ACCEPTU2ENA	INITU1ENA	ACCEPTU1ENA	ULSTCHNGREQ			TSTCTL				RESERVED	

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Bits	Field Name	Description	Type	Reset
31	RUNSTOP	Run/Stop 0x0: Stop USB device controller operation and signal disconnect to attached host. Clear only after all active transfers have been removed. For USB 3.0 disconnection, proceed by changing the target state to RX_DET. USBOTGSS_DSTS[22] DEVCTRLHLT is set once disconect is complete and core is idle. 0x1: Start USB device controller operation, after programming the device CSR. Controller will not signal connect to the attached host until the bit is set.	RW	0
30	CSFTRST	Core Soft Reset. Auto-cleared. The reset has the following effect: - Interrupts are cleared. - Registers are cleared except: USBOTGSS_GSTS, USBOTGSS_GSNPSID, USBOTGSS_GGPIO, USBOTGSS_GUID, USBOTGSS_GUSB2PHYCFG, USBOTGSS_GUSB3PIPECTL, USBOTGSS_DCFG, USBOTGSS_DCTL, USBOTGSS_DEVTEN, USBOTGSS_DSTS. TxFIFOs and RxFIFO are flushed. - State machines are reset to the idle state, except the device slave. - Transactions on the device bus Master are terminated after completion. - Transactions on the USB are terminated immediately. Write 0x1: Start reset (self-clearing) Read 0x1: Reset ongoing Read 0x0: No ongoing reset, reset complete.	RW	0
29	RESERVED		R	0
28	HIRDTHRES_4	Host Initiated Resume Duration (HIRD) Threshold, MSbit: See HIRDTHRES_TIME	RW	0
27:24	HIRDTHRES_TIME	Host Initiated Resume Duration (HIRD) Threshold, LSBits = timeout value. utmi_l1_suspend_n is asserted in L1 when : (HIRD value >= HIRDTHRES_TIME) and (HIRDTHRES_4=1) utmi_sleep_n is asserted in L1 when : (HIRD value < HIRDTHRES_TIME) or (HIRDTHRES_4=0) 0x6: 510 us 0x1: 135 us 0xA: 810 us 0x7: 585 us 0x0: 60 us 0x2: 210 us 0x8: 660 us 0x9: 735 us 0xB: 885 us 0x4: 360 us 0x5: 435 us 0xC: 960 us (maximum: higher values are invalid) 0x3: 285 us	RW	0x0
23	APPL1RES	LPM Response Programmed by Application: Handshake response made to LPM token. Note that if USBOTGSS_DCFG[22] LPMCAP = 0, the response is always timeout (no response). 0x0: NYET handshake to correct LPM transaction if data is pending in Tx FIFO or if OUT (Rx) endpoints are in flow controlled state. 0x1: Core shall ACK correct LPM transaction regardless of Tx FIFO status and OUT (Rx) endpoint flow control.	RW	0

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Bits	Field Name	Description	Type	Reset
22:20	RESERVED		R	0x0
19	KEEPCONNECT	Used for Save-and-Restore operation. DO NOT USE, SAR NOT IMPLEMENTED 0x0: 0x1: Prevents device disconnection when RUNSTOP is cleared to 0. Enables the "Hibernation Request Event" when the link goes to U3/L2. Prevents LTSSM from automatically going to U0/L0 when host requests resume from U3/L2.	RW	0
18	L1HIBERNATIONEN	DO NOT USE, SAR NOT IMPLEMENTED	RW	0
17	CRS	Controller Restore State. DO NOT USE, SAR NOT IMPLEMENTED Write 0x0: Initiate restore process, sets USBOTGSS_DSTS[25] RSS to 1 Write 0x1:	RW	0
16	CSS	Controller Save State. DO NOT USE, SAR NOT IMPLEMENTED Write 0x0: Initiate save process, sets USBOTGSS_DSTS[24] SSS to 1 Write 0x1:	RW	0
15:13	RESERVED		R	0x0
12	INITU2ENA	Initiate U2 Enable. Cleared to 0 by USB reset. 0x0: May not initiate U2 0x1: May initiate U2	RW	0
11	ACCEPTU2ENA	Accept U2 Enable. Cleared to 0 by USB reset. 0x0: Reject U2 except when Force_LinkPM_Accept bit is set 0x1: Accept transition to U2 state if nothing is pending on the application side	RW	0
10	INITU1ENA	Initiate U1 Enable. Cleared to 0 by USB reset. 0x0: May not initiate U1 0x1: May initiate U1	RW	0
9	ACCEPTU1ENA	Accept U1 Enable. Cleared to 0 by USB reset. 0x0: Reject U1 except when Force_LinkPM_Accept bit is set 0x1: Accept transition to U1 state if nothing is pending on the application side.	RW	0
8:5	ULSTCHNGREQ	USB/Link State Change Request. A new request is indicated by a change of value. To issue the same request back-to-back, a 0 shall be written between the two requests. State change request result is reflected in USBOTGSS_DSTS. 0x6: SS: SS.Inactive 0x8: SS: Recovery HS/FS/LS: Remote wakeup request. Issue only when device is in early suspend or suspend state 0x5: SS: Rx.Detect 0xA: SS: Compliance 0xB: SS: Loopback 0x0: No action 0x4: SS: SS.Disabled	RW	0x0

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Bits	Field Name	Description	Type	Reset
4:1	TSTCTL	Test Control 0x1: Test_J mode 0x0: Test mode disabled 0x2: Test_K mode 0x4: Test_Packet mode 0x5: Tes_Force_Enable mode 0x3: Test_SE0_NAK mode	RW	0x0
0	RESERVED		R	0

Table 23-1329. Register Call Summary for Register USBOTGSS_DCTL

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1] [2] [3] [4] [5]

Table 23-1330. USBOTGSS_DEVTEN

Address Offset	0x0000 C708		
Physical Address	0x4A03 C708	**Instance**	DWC_USB3
Description	Device event enable: Enables the generation of device-specific events (see USBOTGSS_DEVT).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		INACTTIMEOUTRCVEDEN	VNDRDEVTSTRCVEDEN	EVNTOVERFLOWEN	CMDCMPLTEN	ERRTICERREN	RESERVED	SOFEN	EOPFEN	HIBERNATIONREQEVTEN	WKUPEVTEN	ULSTCNGEN	CONNECTDONEEN	USBRSTEN	DISCONNEVTEN

Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x0 0000
13	INACTTIMEOUTRCVEDEN	U2 Inactive Timeout Received Event Enable	RW	0
12	VNDRDEVTSTRCVEDEN	Vendor Device Test Received event Enable	RW	0
11	EVNTOVERFLOWEN	Event Overflow event Enable	RW	0
10	CMDCMPLTEN	Command Complete event Enable	RW	0
9	ERRTICERREN	Erratic Error event Enable	RW	0
8	RESERVED		RW	0
7	SOFEN	Start of (micro)Frame event Enable. For debug only.	RW	0
6	EOPFEN	End of Periodic Frame event Enable. For debug only.	RW	0
5	HIBERNATIONREQEVTEN	Hibernation Request Event Enable. DO NOT USE, HIBERNATION NOT IMPLEMENTED	RW	0
4	WKUPEVTEN	Resume/Remote Wakeup Detected Event Enable.	RW	0
3	ULSTCNGEN	USB/Link State Change event Enable	RW	0
2	CONNECTDONEEN	Connection Done event Enable	RW	0
1	USBRSTEN	USB Reset Enable	RW	0
0	DISCONNEVTEN	Disconnct Event Enable	RW	0

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Table 23-1331. Register Call Summary for Register USBOTGSS_DEVTEN

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1]

Table 23-1332. USBOTGSS_DSTS

Address Offset	0x0000 C70C		
Physical Address	0x4A03 C70C	**Instance**	DWC_USB3
Description	Device status		
Type	RW		

31 30	29	28	27 26	25	24	23	22	21 20 19 18	17	16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	DCNRD	SRE	RESERVED	RSS	SSS	COREIDLE	DEVCTRLHLT	USBLNKST	RXFIFOEMPTY		SOFFN	CONNECTSPD

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	DCNRD	Device Controller Not Ready Read 0x1: Core is completing the state transitions after hibernation exit. Wait before processing USBLNKST Read 0x0: Core is ready.	R	0
28	SRE	Save/Restore Error. NOT SUPPORTED.	R	0
27:26	RESERVED		R	0x0
25	RSS	Restore State Status, triggered by writing 1 to RSS Read 0x1: Restore is ongoing Read 0x0: Restore is complete / inactive	R	0
24	SSS	Save State Status, triggered by writing 1 to CSS Read 0x1: Save is ongoing Read 0x0: Save is complete / inactive	R	0
23	COREIDLE	Core Idle status. asserted when all RxFIFO data transferred to system memory, all completed descriptors are written, and all Event Counts are zero. Changes after reset, so that reset value may not match first readout. Read 0x1: core is idle Read 0x0: core has unfinished activities	R	1
22	DEVCTRLHLT	Device Controller Halted. Cleared (0) when the USBOTGSS_DCTL[31] RUNSTOP is written to 1. Set (1) after USBOTGSS_DCTL[31] RUNSTOP has been written to 0, core is idle and disconnect process is complete. When DEVCTRLHLT =1, no Device events are generated.	R	0

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Bits	Field Name	Description	Type	Reset
21:18	USBLNKST	USB/Link State. Encoding depends on the connection speed (SS or HS/FS/LS) Read 0x3: SS: LTSSM = U3 HS/FS/LS: Suspend state Read 0xE: HS/FS/LS: Reset Read 0x4: SS: LTSSM = SS_DIS HS/FS/LS: Disconnected state (default) Read 0xB: SS: LTSSM = LPBK Read 0xF: SS: LTSSM = Reset/Resume. USB resume or reset received from the host while in suspend. Write RECOV=8 to USBOTGSS_DCTL[8:5] ULSTCHNGREQ field to acknowledge it. HS/FS/LS: Resume Read 0x2: SS: LTSSM = U2 HS/FS/LS: Sleep state Read 0x0: SS: LTSSM = U0 HS/FS/LS: On state Read 0xA: SS: LTSSM = CMPLY Read 0x6: SS: LTSSM = SS_INACT Read 0x1: SS: LTSSM = U1 Read 0x8: SS: LTSSM = RECOV Read 0x7: SS: LTSSM = POLL Read 0x9: SS: LTSSM = HRESET Read 0x5: SS: LTSSM = RX_DET HS/FS/LS: Early Suspend state	R	0x4
17	RXFIFOEMPTY	Rx FIFO Empty Read 0x1: Rx FIFO is empty Read 0x0: Rx FIFO is not empty	R	1
16:3	SOFFN	received Start Of Frame's Frame Number	R	0x0000
2:0	CONNECTSPD	Connection Speed. USB speed at which the device has come up after speed detection through a chirp sequence. Read 0x3: Full Speed (FS): 12 Mbit/s on serial PHY: NOT SUPPORTED Read 0x2: Low Speed (LS): 1.5 Mbit/s on serial PHY: NOT SUPPORTED Read 0x1: Full Speed (FS): 12 Mbit/s Read 0x0: High Speed (HS): 480 Mbit/s Read 0x4: Super Speed (SS): 5 Gbit/s	R	0x4

Table 23-1333. Register Call Summary for Register USBOTGSS_DSTS

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]
- DWC_USB3 Register Description: [1] [2] [3] [4] [5]

Table 23-1334. USBOTGSS_DGCMDPAR

Address Offset	0x0000 C710		
Physical Address	0x4A03 C710	**Instance**	DWC_USB3
Description	Device generic command parameter: To be programmed before or along with the device command itself.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARAMETER																															

Bits	Field Name	Description	Type	Reset
31:0	PARAMETER	Parameter of the command; command-dependent.	RW	0x0000 0000

Table 23-1335. Register Call Summary for Register USBOTGSS_DGCMDPAR

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1336. USBOTGSS_DGCMD

Address Offset	0x0000 C714		
Physical Address	0x4A03 C714	**Instance**	DWC_USB3
Description	Device generic command: Generic command interface to send link management packets and notifications.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMDSTATUS	RESERVED				CMDACT	RESERVED	CMDIOC	CMDTYP							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	CMDSTATUS	Command Status. Read 0x1: CmdErr: Error while processing the command. Read 0x0: No error	R	0
14:11	RESERVED		R	0x0
10	CMDACT	Command active. Auto-cleared. Write 0x1: Start generic command execution (self-clearing) Read 0x1: Command active (ongoing) Read 0x0: No ongoing command, command complete.	RW	0
9	RESERVED		R	0
8	CMDIOC	Command Interrupt On Complete. Event mapped to interrupt number USBOTGSS_DCFG[16:12] INTNUM. Reads return 0. Write 0x1: Generic Command Completion event to be issued after executing the command.	W	0

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Bits	Field Name	Description	Type	Reset
7:0	CMDTYP	Command Type. Reads return 0. Write 0xC: Set Endpoint NRDY: Makes the core think that the given endpoint is in an NRDY state. If buffers are available in that endpoint, an ERDY is immediately transmitted. Parameter[4:0] = Physical Endpoint Number Write 0x3: Transmit Function Wake Device Notification (Notification-only in SuperSpeed) Parameter[7:0] - Interface Number (IntfNum) that caused remote wakeup Write 0x6: Transmit Function Host Role Request Device Notification (Notification-only in SuperSpeed) Parameter[1:0] = RSP Phase (Notification Type Specific) is INITIATE (2'b01) or CONFIRM (2'b10). Write 0xA: All FIFO Flush. (No parameter) Write 0x2: Set Periodic Parameters Parameter[9:0] (SystemExitLatency): Set value programmed by the host through the Set SEL device request, in microseconds. The Set SEL control transfer has 6 bytes of data and contains 4 values; Refer to the USB 3.0 spec, Section 9.4.12. Offset / Name / Meaning: 0 U1SEL Time in us for U1 System Exit Latency 1 U1PEL Time in us for U1 Device to Host Exit Latency 2 U2SEL Time in us for U2 System Exit Latency 4 U2PEL Time in us for U2 Device to Host Exit Latency If the device is enabled for U1 and U2, then the U2PEL should be programmed. If the device is enabled only for U1, then U1PEL should be programmed into this parameter. If the value is greater than 125 us, then the software must program a value of zero into this register. Write 0x1: Transmit Set Link Function LPM. (Reserved in non-SuperSpeed operations) Parameter[0] = [Force_LinkPM_Accept] (0: De-assert 1: Assert) Write 0x9: Selected FIFO Flush Parameter[4:0] = FIFO Number Paramer[5] = TX FIFO (1) or RX FIFO (0) Write 0x10: Run device Bus LoopBack Test: Issue this command first, then the Start Transfer command to EP 0 and 1. Configure EP0 as OUT and EP1 as IN. The core reads data from the IN buffers and writes it back to OUT buffers. The IN and OUT must have an equal amount of data buffer. The endpoint 1 Tx-FIFO default value of (512/8)+2 = 66 should be changed to (1024/8)+2 = 130 for loopback mode. Parameter[0] = enable (1) and disable (0) Loopback mode.	W	0x00

Table 23-1337. Register Call Summary for Register USBOTGSS_DGCMD

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1338. USBOTGSS_DALEPENA

Address Offset	0x0000 C720		
Physical Address	0x4A03 C720	**Instance**	DWC_USB3
Description	Device active USB endpoint enable. Set each bit (1) to enable the corresponding endpoint. Bits 0 and 1 are set after USB reset as they enable the control endpoint. All other bits are set according to enumeration, and cleared on a USB reset.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBACTEP15_IN	USBACTEP15_OUT	USBACTEP14_IN	USBACTEP14_OUT	USBACTEP13_IN	USBACTEP13_OUT	USBACTEP12_IN	USBACTEP12_OUT	USBACTEP11_IN	USBACTEP11_OUT	USBACTEP10_IN	USBACTEP10_OUT	USBACTEP9_IN	USBACTEP9_OUT	USBACTEP8_IN	USBACTEP8_OUT	USBACTEP7_IN	USBACTEP7_OUT	USBACTEP6_IN	USBACTEP6_OUT	USBACTEP5_IN	USBACTEP5_OUT	USBACTEP4_IN	USBACTEP4_OUT	USBACTEP3_IN	USBACTEP3_OUT	USBACTEP2_IN	USBACTEP2_OUT	USBACTEP1_IN	USBACTEP1_OUT	USBACTEP0_IN	USBACTEP0_OUT

Bits	Field Name	Description	Type	Reset
31	USBACTEP15_IN	USB Activate Endpoint 15 IN	RW	0
30	USBACTEP15_OUT	USB Activate Endpoint 15 OUT	RW	0
29	USBACTEP14_IN	USB Activate Endpoint 14 IN	RW	0
28	USBACTEP14_OUT	USB Activate Endpoint 14 OUT	RW	0
27	USBACTEP13_IN	USB Activate Endpoint 13 IN	RW	0
26	USBACTEP13_OUT	USB Activate Endpoint 13 OUT	RW	0
25	USBACTEP12_IN	USB Activate Endpoint 12 IN	RW	0
24	USBACTEP12_OUT	USB Activate Endpoint 12 OUT	RW	0
23	USBACTEP11_IN	USB Activate Endpoint 11 IN	RW	0
22	USBACTEP11_OUT	USB Activate Endpoint 11 OUT	RW	0
21	USBACTEP10_IN	USB Activate Endpoint 10 IN	RW	0
20	USBACTEP10_OUT	USB Activate Endpoint 10 OUT	RW	0
19	USBACTEP9_IN	USB Activate Endpoint 9 IN	RW	0
18	USBACTEP9_OUT	USB Activate Endpoint 9 OUT	RW	0
17	USBACTEP8_IN	USB Activate Endpoint 8 IN	RW	0
16	USBACTEP8_OUT	USB Activate Endpoint 8 OUT	RW	0
15	USBACTEP7_IN	USB Activate Endpoint 7 IN	RW	0
14	USBACTEP7_OUT	USB Activate Endpoint 7 OUT	RW	0
13	USBACTEP6_IN	USB Activate Endpoint 6 IN	RW	0
12	USBACTEP6_OUT	USB Activate Endpoint 6 OUT	RW	0
11	USBACTEP5_IN	USB Activate Endpoint 5 IN	RW	0
10	USBACTEP5_OUT	USB Activate Endpoint 5 OUT	RW	0
9	USBACTEP4_IN	USB Activate Endpoint 4 IN	RW	0
8	USBACTEP4_OUT	USB Activate Endpoint 4 OUT	RW	0
7	USBACTEP3_IN	USB Activate Endpoint 3 IN	RW	0
6	USBACTEP3_OUT	USB Activate Endpoint 3 OUT	RW	0
5	USBACTEP2_IN	USB Activate Endpoint 2 IN	RW	0
4	USBACTEP2_OUT	USB Activate Endpoint 2 OUT	RW	0
3	USBACTEP1_IN	USB Activate Endpoint 1 IN	RW	0
2	USBACTEP1_OUT	USB Activate Endpoint 1 OUT	RW	0
1	USBACTEP0_IN	USB Activate Endpoint 0 IN (control)	RW	0
0	USBACTEP0_OUT	USB Activate Endpoint 0 OUT (control)	RW	0

Table 23-1339. Register Call Summary for Register USBOTGSS_DALEPENA

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

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Table 23-1340. USBOTGSS_DEPCMDPAR2_i

Address Offset	0x0000 C800 + (0x10 * i)	**Index**	i = 0 to 31
Physical Address	0x4A03 C800 + (0x10 * i)	**Instance**	DWC_USB3
Description	Device physical endpoint-n command parameter 2. Must be programmed before issuing the command, if required by the command.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARAMETER2																															

Bits	Field Name	Description	Type	Reset
31:0	PARAMETER2	Command-dependent	RW	0x0000 0000

Table 23-1341. Register Call Summary for Register USBOTGSS_DEPCMDPAR2_i

Super-Speed USB OTG Subsystem

- Device-Mode Endpoint Commands: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- DWC_USB3 Register Summary: [10]

Table 23-1342. USBOTGSS_DEPCMDPAR1_i

Address Offset	0x0000 C804 + (0x10 * i)	**Index**	i = 0 to 31
Physical Address	0x4A03 C804 + (0x10 * i)	**Instance**	DWC_USB3
Description	Device physical endpoint-n command parameter 1 Must be programmed before issuing the command, if required by the command.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARAMETER1																															

Bits	Field Name	Description	Type	Reset
31:0	PARAMETER1	Command-dependent	RW	0x0000 0000

Table 23-1343. Register Call Summary for Register USBOTGSS_DEPCMDPAR1_i

Super-Speed USB OTG Subsystem

- Device-Mode Endpoint Commands: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- DWC_USB3 Register Summary: [10]
- USBOTGSS_WRAPPER Register Description: [11] [12]

Table 23-1344. USBOTGSS_DEPCMDPAR0_i

Address Offset	0x0000 C808 + (0x10 * i)	**Index**	i = 0 to 31
Physical Address	0x4A03 C808 + (0x10 * i)	**Instance**	DWC_USB3
Description	Device physical endpoint-n command parameter 0 Must be programmed before issuing the command.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARAMETER0																															

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Bits	Field Name	Description	Type	Reset
31:0	PARAMETER0	Command-dependent	RW	0x0000 0000

Table 23-1345. Register Call Summary for Register USBOTGSS_DEPCMDPAR0_i

Super-Speed USB OTG Subsystem

- Device-Mode Endpoint Commands: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]
- DWC_USB3 Register Summary: [11]

Table 23-1346. USBOTGSS_DEPCMD_i

Address Offset	0x0000 C80C + (0x10 * i)	**Index**	i = 0 to 31
Physical Address	0x4A03 C80C + (0x10 * i)	**Instance**	DWC_USB3
Description	Device physical endpoint-n command		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMDPARAM_EVTPARAM																CMDSTATUS				HIPRI_FORCERM	CMDACT	RESERVED	CMDIOC	RESERVED				CMDTYP			

Bits	Field Name	Description	Type	Reset
31:16	CMDPARAM_EVTPARAM	Read: Event parameters (see Section 23.11.4.8.3, *Device-Mode Events*). Write: Command parameters (see Section 23.11.4.8.2, *Device-Mode Endpoint Commands*) command-dependent: DEPSTRTXFER on isoc EP: [31:16] microframe number for the first TRB (StartMicroFramNum) DEPSTRTXFER on stream-capable EP: [31:16] USB stream ID for the transfer (StreamID) DEPUPDXFER/DEPENDXFER: [22:16] Transfer resource index returned by HW upon transfer start (XferRscIdx) DEPSTARTCFG: [22:16] Transfer resource index assigned by software upon new configuration start (XferRscIdx)	RW	0x0000
15:12	CMDSTATUS	Command Completion Status. Additional information about the command completion. Same format as bits 15:12 of the Endpoint Command Complete event.	RW	0x0
11	HIPRI_FORCERM	HighPriority/ForceRM. Write-only field, reads return 0. Start Transfer command: HighPriority value End Transfer command: ForceRM value Write 0x0: HighPriority/ForceRM=0 Write 0x1: HighPriority/ForceRM=1	RW	0
10	CMDACT	Command Active. Auto-cleared. Write 0x1: Execute the generic command. Read 0x1: Command execution is being started. Read 0x0: Endpoint is ready to accept another command, CmdStatus field is valid. The effects of the previously-issued command may not all have taken place yet.	RW	0
9	RESERVED	Register is stored in RAM, so that the field is actually writable (value is still don't care).	RW	0

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Bits	Field Name	Description	Type	Reset
8	CMDIOC	Command Interrupt On Complete. Event mapped to interrupt number DEPCFG.IntNum (the command). Reads return 0. Write 0x0: No interrupt on complete Write 0x1: generic Endpoint Command Complete event issued after executing the command.	RW	0
7:4	RESERVED	Register is stored in RAM, so that the field is actually writable (value is still don't care).	RW	0x0
3:0	CMDTYP	Command Type. Write 0x4: DEPSETSTALL: Set Stall (No Parameter) Write 0x3: DEPGETDSEQ: Get Data Sequence Number (No Parameter) Write 0x6: DEPSTRTXFER: Start Transfer (64-bit parameter) Write 0x2: DEPXFERCFG: Set Endpoint Transfer Resource Configuration (32-bit parameter) Write 0x8: DEPENDXFER: End Transfer (No Parameter) Write 0x1: DEPCFG: Set Endpoint Configuration (64-bit parameter) Write 0x9: DEPSTARTCFG: Start New Configuration (No Parameter) Write 0x5: DEPCSTALL: Clear Stall (No Parameter) Write 0x7: DEPUPDXFER: Update Transfer (No Parameter)	RW	0x0

Table 23-1347. Register Call Summary for Register USBOTGSS_DEPCMD_i

Super-Speed USB OTG Subsystem

- Device-Mode Endpoint Commands: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]
- DWC_USB3 Register Summary: [16]

Table 23-1348. USBOTGSS_OCFG

Address Offset	0x0000 CC00		
Physical Address	0x4A03 CC00	**Instance**	DWC_USB3
Description	OTG configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OTGSFTRSTMSK	OTGVERSION	HNPCAP	SRPCAP

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000
3	OTGSFTRSTMSK	Protects OTG, PHY and VBUS filters from the following software resets: xHCI USBOTGSS_USBCMD[1] HCRST (host), USBOTGSS_DCTL[30] CSFTRST (device). Note: In OTG2 applications, it is not recommended to program USBOTGSS_USBCMD[1] HCRST during role switch. 0x0: OTG logic reset by software resets 0x1: OTG logic not affected by software resets. Use only with USBOTGSS_GCTL[13:12] PRTCAPDIR = 0x3	RW	0

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Bits	Field Name	Description	Type	Reset
2	OTGVERSION	Debug, always write 0.	RW	0
1	HNPCAP	HNP Capabilty Enable. 0x0: HNP capability is disabled 0x1: HNP capability is enabled	RW	0
0	SRPCAP	SRP Capability enable. For A-device, SRP detection. For B-device, SRP generation. 0x0: SRP capability is disabled 0x1: SRP capability is enabled	RW	0

Table 23-1349. Register Call Summary for Register USBOTGSS_OCFG

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1350. USBOTGSS_OCTL

Address Offset	0x0000 CC04		
Physical Address	0x4A03 CC04	**Instance**	DWC_USB3
Description	OTG control IMPORTANT NOTE: Register is reinitialized on ID change, but is not affected by a software reset.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								OTG3_GOERR	PERIMODE	PRTPWRCTL	HNPREQ	SESREQ	TERMSELDLPULSE	DEVSETHNPEN	HSTSETHNPEN

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7	OTG3_GOERR	To be set upon TRSP_ACK_ERR, TRSP_CNF_ERR, or TRSP_WRST_ERR timeout. Auto-cleared. OTG3: NOT IMPLEMENTED, DO NOT SET. 0x0: Read 0x1: LTSSM transition to error state is pending Write 0x1: Sends LTSSM to error state during OTG 3.0 RSP	RW	0
6	PERIMODE	Peripheral Mode. Program the core to work as a peripheral or as a host. Read 0x1: OTG device acts as a peripheral Read 0x0: OTG device acts as a host	RW	1

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Bits	Field Name	Description	Type	Reset
5	PRTPWRCTL	Port Power Control. Set or cleared by software. Self-cleared in any of the following conditions: 1) transition to a_idle OTG state 2) aidl_bdis_tout event when in a_suspend OTG state 3) a_wait_bcon_tout event when in a_wait_bcon OTG state 4) transition to any b_* OTG state Write 0x0: Manually switch off VBUS drive. Write 0x1: Initiate the VBUS drive on the USB, when A-device. Read 0x1: VBUS is driven. Read 0x0: VBUS drive is off	RW	0
4	HNPREQ	HNP Request. Set (1) by software to initiate HNP request to the connected USB host. Clear (0) by software upon either USBOTGSS_OEVT[11] OTGBDEVHOSTENDEVNT or USBOTGSS_OEVT[8] OTGBDEVVBUSCHNGEVNT. 0x0: HNP request inactive. 0x1: HNP request active.	RW	0
3	SESREQ	Session Request. In the absence of USBOTGSS_OEVT[9] OTGBDEVSESSVLDDETEVNT after a request, the application must wait for at least TB_SRP_FAIL (6 secs) before another request. Write 0x0: No action Write 0x1: Initiate the SRP (data line pulsing) on the USB. Read 0x0: All reads return zero.	RW	0
2	TERMSELDLPULSE	TermSelect Data Line Pulse. Alternate SRP data line pulsing method on UTMI interface. 0x0: utmi_txvalid used for SRP generation (default) 0x1: utmi_termselect used for SRP generation	RW	0
1	DEVSETHNPEN	Device Set HNP Enable. To be set when HNP has been successfully enabled by the connected host, using the SetFeature.SetHNPEnable command. 0x0: HNP disabled in device 0x1: HNP enabled in device	RW	0
0	HSTSETHNPEN	Host Set HNP Enable. To be set when HNP has been successfully enabled on the connected device, using the SetFeature.SetHNPEnable command. 0x0: HNP disabled in host 0x1: HNP enabled in host	RW	0

Table 23-1351. Register Call Summary for Register USBOTGSS_OCTL

Super-Speed USB OTG Subsystem

- DWC_USB3 Register Summary: [0]

Table 23-1352. USBOTGSS_OEVT

Address Offset	0x0000 CC08		
Physical Address	0x4A03 CC08	**Instance**	DWC_USB3
Description	OTG event: OTG interrupt status. All writable bits are cleared by writing a 1.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICEMODE	RESERVED						OTGCONIDSTSCHNGEVNT	HRRCONFNOTIFEVNT	HRRINITNOTIFEVNT	OTGADEVIDLEEVNT	OTGADEVBHOSTENDEVNT	OTGADEVHOSTEVNT	OTGADEVHNPCHNGDETEVNT	OTGADEVSRPDETEVNT	OTGADEVSESSENDDETEVNT	RESERVED				OTGBDEVHOSTENDEVNT	OTGBDEVHNPCHNGEVNT	OTGBDEVSESSVLDDETEVNT	OTGBDEVBUSCHNGEVNT	RESERVED				BSESVLD	HSTNEGSTS	SESREQSTS	OEVTERROR

Bits	Field Name	Description	Type	Reset
31	DEVICEMODE	Dual-role device's mode, based on iddig input. Read 0x1: B-device = default peripheral Read 0x0: A-device = default host	R	1
30:25	RESERVED		R	0x00
24	OTGCONIDSTSCHNGEVNT	Connector ID status change event. Set in both A-device and B-device mode. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
23	HRRCONFNOTIFEVNT	Host Role Request Confirm Notifier Event. Set upon reception of HRR Device Notification TP with Confirm field set. Set in OTG3, SS, A-host or B-host mode only. OTG3: NOT IMPLEMENTED Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
22	HRRINITNOTIFEVNT	Host Role Request Initiate Notifier Event. Set upon reception of HRR Device Notification TP with Initiate field set. Set in OTG3, SS, A-host or B-host mode only. OTG3: NOT IMPLEMENTED Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
21	OTGADEVIDLEEVNT	A-device A-IDLE Event. Set when OTG FSM enters A-IDLE state from any other state. Set in A-device mode only. OTG3: NOT IMPLEMENTED Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
20	OTGADEVBHOSTENDEVNT	A-device B-host End Event. Set when connected B-device has completed its B-host role and returns to B-peripheral. Set in A-device mode only. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
19	OTGADEVHOSTEVNT	A-device Host Event. Set when device enters host role, upon initial connect to B-device as well as upon HNP from A-peripheral to A-host. Set in A-device mode only. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
18	OTGADEVHNPCHNGDETEVNT	A-device HNP change Detected Event. Set when there is an HNP event. Set in A-device mode only. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
17	OTGADEVSRPDETEVNT	A-device SRP Detected Event. Set when SRP request from B-device is detected. Set in A-device mode only. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
16	OTGADEVSESSENDDETEVNT	A-device Session End Detected Event. Set when UTMI input "a-vbus-valid" is deasserted (0). Set in A-device mode only. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
15:12	RESERVED		R	0x0
11	OTGBDEVHOSTENDEVNT	B-device Host End Event. Set completing B-host role and returning to default B-peripheral role. Set in B-device mode only. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
10	OTGBDEVHNPCHNGEVNT	B-device HNP Change Event. Set upon (success of failure of an) HNP attempt. Set in B-device mode only. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
9	OTGBDEVSESSVLDDETEVNT	B-device Session Valid Detected Event. Set when B-device succeeds in starting a session. Set in B-device mode only. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
8	OTGBDEVVBUSCHNGEVNT	B-device VBUS Change Event. Set when UTMI input "b-session-valid" transitions (to 0 or 1). Set in B-device mode only. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0
7:4	RESERVED		R	0x0
3	BSESVLD	B-Session Valid. Updated when OTGBDevVBUSChngEvnt is set. Read 0x1: B-session is valid on VBUS Read 0x0: B-session is not valid on VBUS	R	0
2	HSTNEGSTS	Host Negociation Status. Updated when OTGADevHNPChngEvnt or OTGBDevHNPChngEvnt is set. Read 0x1: Host negotiation success. Read 0x0: Host negotiation failure. In A-device, indicates imminent end of session indication from core. In B-device, it indicates that the timer used to wait for an A-device to signal a connection (b_ase0_brst_tmout) timed out resulting in B-device staying as B-peripheral.	R	0
1	SESREQSTS	Session Request Status. Updated when OTGBDevSessVldDetEvnt is set. Read 0x1: Session started as a result of successful SRP. Read 0x0: Session not started as a result of SRP.	R	0
0	OEVTERROR	No errors currently defined. Write 0x0: No action Write 0x1: Clear the event Read 0x1: Event was set by core Read 0x0: Event was not set	RW W1toClr	0

Table 23-1353. Register Call Summary for Register USBOTGSS_OEVT

Super-Speed USB OTG Subsystem

- Wrapper Events: [0]
- DWC_USB3 Register Summary: [1]
- DWC_USB3 Register Description: [2] [3] [4]
- USBOTGSS_WRAPPER Register Description: [5] [6] [7]

Table 23-1354. USBOTGSS_OEVTEN

Address Offset	0x0000 CC0C		
Physical Address	0x4A03 CC0C	**Instance**	DWC_USB3
Description	OTG event enable: OTG interrupt event enable.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							OTGCONIDSTSCHNGEVNTEN	HRRCONFNOTIFEVNTEN	HRRINITNOTIFEVNTEN	OTGADEVIDLEEVNTEN	OTGADEVBHOSTENDEVNTEN	OTGADEVHOSTEVNTEN	OTGADEVHNPCHNGDETEVNTEN	OTGADEVSRPDETEVNTEN	OTGADEVSESSENDDETEVNTEN	RESERVED				OTGBDEVHOSTENDEVNTEN	OTGBDEVHNPCHNGEVNTEN	OTGBDEVSESSVLDDETEVNTEN	OTGBDEVVBUSCHNGEVNTEN	RESERVED								

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	OTGCONIDSTSCHNGEVNTEN	Connector ID Status Change Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
23	HRRCONFNOTIFEVNTEN	Host Role Request Confirm Notifier Event Enable. OTG3: NOT IMPLEMENTED 0x0: Event disabled 0x1: Event enabled	RW	0
22	HRRINITNOTIFEVNTEN	Host Role Request Initiate Notifier Event Enable. OTG3: NOT IMPLEMENTED 0x0: Event disabled 0x1: Event enabled	RW	0
21	OTGADEVIDLEEVNTEN	A-device A-IDLE Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
20	OTGADEVBHOSTENDEVNTEN	A-device B-host End Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
19	OTGADEVHOSTEVNTEN	A-device Host Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
18	OTGADEVHNPCHNGDETEVNTEN	A-device HNP change Detected Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
17	OTGADEVSRPDETEVNTEN	A-device SRP Detected Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
16	OTGADEVSESSENDDETEVNTEN	A-device Session End Detected Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
15:12	RESERVED		R	0x0
11	OTGBDEVHOSTENDEVNTEN	B-device Host End Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
10	OTGBDEVHNPCHNGEVNTEN	B-device HNP Change Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0

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Bits	Field Name	Description	Type	Reset
9	OTGBDEVSESSVLDDETEVNTEN	B-device Session Valid Detected Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
8	OTGBDEVVBUSCHNGEVNTEN	B-device VBUS Change Event Enable. 0x0: Event disabled 0x1: Event enabled	RW	0
7:0	RESERVED		R	0x00

Table 23-1355. Register Call Summary for Register USBOTGSS_OEVTEN

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

Table 23-1356. USBOTGSS_OSTS

Address Offset	0x0000 CC10		
Physical Address	0x4A03 CC10	**Instance**	DWC_USB3
Description	OTG status		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				OTGSTATE				RESERVED	PERIPHERALSTATE	XHCIPRTPOWER	BSESVLD	VBUSVLD	CONIDSTS		

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x0 0000
11:8	OTGSTATE	[A-device and B-device] OTG state machine state, for debug. Default value can vary depending on integration. Read 0x3: a_wait_vfall Read 0xE: a_wait_switch Read 0xC: b_wait_acon Read 0x4: a_vbus_err Read 0xB: b_peripheral Read 0xF: b_wait_switch Read 0x2: a_wait_bcon Read 0x0: a_idle Read 0xA: b_srp_init Read 0x6: a_suspend Read 0x1: a_wait_vrise Read 0x8: a_wait_ppwr Read 0x7: a_peripheral Read 0x9: b_idle Read 0xD: b_host Read 0x5: a_host	R	0x8
7:5	RESERVED	Reserved	R	0x0

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Bits	Field Name	Description	Type	Reset
4	PERIPHERALSTATE	[A-device and B-device] Current role of the controller Read 0x1: Peripheral Read 0x0: Host	R	1
3	XHCIPRTPOWER	[A-device] xHCI host port power. Reflects host bit field USBOTGSS_PORTSC1/2[9] PP.	R	1
2	BSESVLD	[B-device] VBUS B-session valid status Read 0x1: B-session is valid. Read 0x0: B-session is not valid.	R	0
1	VBUSVLD	[A-device] VBUS valid status Read 0x1: VBUS is valid. Read 0x0: VBUS is not valid.	R	0
0	CONIDSTS	[A-device and B-device] Connector ID status. Default value can vary depending on integration. Read 0x1: Core is B-device. Read 0x0: Core is A-device.	R	1

Table 23-1357. Register Call Summary for Register USBOTGSS_OSTS

Super-Speed USB OTG Subsystem
- DWC_USB3 Register Summary: [0]

23.11.5.3 USBOTGSS_WRAPPER Registers

23.11.5.3.1 USBOTGSS_WRAPPER Register Summary

Table 23-1358. USBOTGSS_WRAPPER Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
USBOTGSS_REVISION	R	32	0x0000 0000	0x4A02 0000
USBOTGSS_SYSCONFIG	RW	32	0x0000 0010	0x4A02 0010
USBOTGSS_IRQSTATUS_RAW_0	RW	32	0x0000 0024	0x4A02 0024
USBOTGSS_IRQSTATUS_0	RW	32	0x0000 0028	0x4A02 0028
USBOTGSS_IRQENABLE_SET_0	RW	32	0x0000 002C	0x4A02 002C
USBOTGSS_IRQENABLE_CLR_0	RW	32	0x0000 0030	0x4A02 0030
USBOTGSS_IRQSTATUS_RAW_1	RW	32	0x0000 0034	0x4A02 0034
USBOTGSS_IRQSTATUS_1	RW	32	0x0000 0038	0x4A02 0038
USBOTGSS_IRQENABLE_SET_1	RW	32	0x0000 003C	0x4A02 003C
USBOTGSS_IRQENABLE_CLR_1	RW	32	0x0000 0040	0x4A02 0040
USBOTGSS_UTMI_OTG_CTRL	R	32	0x0000 0080	0x4A02 0080
USBOTGSS_UTMI_OTG_STATUS	RW	32	0x0000 0084	0x4A02 0084
USBOTGSS_MMRAM_OFFSET	RW	32	0x0000 0100	0x4A02 0100
USBOTGSS_FLADJ	RW	32	0x0000 0104	0x4A02 0104
USBOTGSS_DEBUG_CFG	RW	32	0x0000 0108	0x4A02 0108
USBOTGSS_DEBUG_DATA	R	32	0x0000 010C	0x4A02 010C
USBOTGSS_DEV_EBC_EN	RW	32	0x0000 0110	0x4A02 0110

23.11.5.3.2 USBOTGSS_WRAPPER Register Description

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Table 23-1359. USBOTGSS_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A02 0000	**Instance**	USBOTGSS_WRAPPER
Description	USBOTGSS_WRAPPER Revision Identifier		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	USBOTGSS_WRAPPER Revision	R	See (1)

(1) TI internal data

Table 23-1360. Register Call Summary for Register USBOTGSS_REVISION

Super-Speed USB OTG Subsystem

- USBOTGSS_WRAPPER Register Summary: [0]

Table 23-1361. USBOTGSS_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A02 0010	**Instance**	USBOTGSS_WRAPPER
Description	Controls various parameters of the master and slave interfaces.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														WRAPRESET	DMADISABLE	RESERVED								STANDBYMODE		IDLEMODE		RESERVED			

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	WRAPRESET	Software reset for the USBOTGSS_WRAPPER register set. Self-clearing. Does not affect the core register set. Write 0x0: No action Write 0x1: Request wrapper reset Read 0x1: Wrapper reset is ongoing Read 0x0: Wrapper reset is done / inactive	RW	0

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Bits	Field Name	Description	Type	Reset
16	DMADISABLE	Disable/Enable control of the DMA master (initiator) to block read/write accesses. Bit is auto-cleared (to 0) by HW in case of outgoing access, but must be set (to 1) manually. Write 0x0: Enable the DMA. The enabling can also be done by the hardware, i.e. bit it auto-cleared. Write 0x1: Disable the DMA. software must ensure that there are no ongoing transactions before setting this bit. The disabling can only be done by software. Read 0x1: DMA is disabled, outgoing read/write accesses are blocked. When in smart-standby mode, standby is requested. Read 0x0: DMA is enabled, outgoing read/write accesses are possible. When in smart-standby mode, standby exit is requested.	RW	1
15:6	RESERVED		R	0x000
5:4	STANDBYMODE	PM mode of local initiator (master). Initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby: initiator is unconditionally placed in standby state. 0x1: No-standby: initiator is unconditionally placed out of standby state. 0x3: Smart-Standby, wakeup-capable: initiator's standby state depends on internal conditions, i.e. the module's functional requirements. Asynchronous wakeup events can be generated. 0x2: Smart-standby: initiator's standby state depends on internal conditions, i.e. the module's functional requirements. Asynchronous wakeup events cannot be generated.	RW	0x2
3:2	IDLEMODE	PM mode of local target (slave). Target shall be capable of handling read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, regardless of the IP module's internal requirements. 0x1: No-idle mode: local target never enters idle state. 0x3: Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. Module shall not generate (IRQ- or DMA-request-related) wakeup events.	RW	0x2
1:0	RESERVED		R	0x0

Table 23-1362. Register Call Summary for Register USBOTGSS_SYSCONFIG

Super-Speed USB OTG Subsystem

- Software Reset: [0]
- Wrapper Events: [1]
- System Power Management: [2] [3] [4] [5] [6] [7] [8]
- USBOTGSS_WRAPPER Register Summary: [9]
- USBOTGSS_WRAPPER Register Description: [10] [11] [12]

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Table 23-1363. USBOTGSS_IRQSTATUS_RAW_0

Address Offset	0x0000 0024		
Physical Address	0x4A02 0024	**Instance**	USBOTGSS_WRAPPER
Description	Raw status of main core interrupt request. Set even if event is not enabled. Write 1 to set, used mostly for debug (regular status also gets set if enabled).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															COREIRQ_ST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	COREIRQ_ST	IRQ status for core: see status register USBOTGSS_IMAN[0] IP Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0

Table 23-1364. Register Call Summary for Register USBOTGSS_IRQSTATUS_RAW_0

Super-Speed USB OTG Subsystem

- USBOTGSS_WRAPPER Register Summary: [0]
- USBOTGSS_WRAPPER Register Description: [1]

Table 23-1365. USBOTGSS_IRQSTATUS_0

Address Offset	0x0000 0028		
Physical Address	0x4A02 0028	**Instance**	USBOTGSS_WRAPPER
Description	"regular" status of main core interrupt request. Set only when enabled, self-cleared unless it was set by writing to USBOTGSS_IRQSTATUS_RAW_0, for debug. Write 1 to clear (raw status also gets cleared).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															COREIRQ_ST

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	COREIRQ_ST	IRQ status for core: see status register USBOTGSS_IMAN[0] IP Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

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Table 23-1366. Register Call Summary for Register USBOTGSS_IRQSTATUS_0

Super-Speed USB OTG Subsystem

- Core Events: [0] [1]
- USBOTGSS_WRAPPER Register Summary: [2]

Table 23-1367. USBOTGSS_IRQENABLE_SET_0

Address Offset	0x0000 002C		
Physical Address	0x4A02 002C	**Instance**	USBOTGSS_WRAPPER
Description	Enable of main core interrupt request. Write 1 to set (i.e. to enable interrupt). Readout is the same as corresponding _CLR register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															COREIRQ_EN

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	COREIRQ_EN	IRQ enable for main core interrupt Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0

Table 23-1368. Register Call Summary for Register USBOTGSS_IRQENABLE_SET_0

Super-Speed USB OTG Subsystem

- USBOTGSS_WRAPPER Register Summary: [0]

Table 23-1369. USBOTGSS_IRQENABLE_CLR_0

Address Offset	0x0000 0030		
Physical Address	0x4A02 0030	**Instance**	USBOTGSS_WRAPPER
Description	Enable of main core interrupt request. Write 1 to clear (i.e. to disable interrupt). Readout is the same as corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															COREIRQ_EN

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	COREIRQ_EN	IRQ enable for main core interrupt Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0

Table 23-1370. Register Call Summary for Register USBOTGSS_IRQENABLE_CLR_0

Super-Speed USB OTG Subsystem

- USBOTGSS_WRAPPER Register Summary: [0]

Table 23-1371. USBOTGSS_IRQSTATUS_RAW_1

Address Offset	0x0000 0034		
Physical Address	0x4A02 0034	**Instance**	USBOTGSS_WRAPPER
Description	Raw status of secondary interrupt requests. Set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug (regular status also gets set).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DMADISABLECLR	OEVT	RESERVED		DRVVBUS_RISE	CHRGVBUS_RISE	DISCHRGVBUS_RISE	RESERVED		IDPULLUP_RISE	RESERVED		DRVVBUS_FALL	CHRGVBUS_FALL	DISCHRGVBUS_FALL	RESERVED		IDPULLUP_FALL

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	DMADISABLECLR	DMA-disable self-clear IRQ status: USBOTGSS_SYSCONFIG[17] DMADISABLE hardware-cleared (to 0) because of DMA access. Not triggered by a software clear. Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
16	OEVT	OTG event in core, IRQ status: see status register USBOTGSS_OEVT Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
15:14	RESERVED		R	0x0
13	DRVVBUS_RISE	Drive VBUS control rise IRQ status Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
12	CHRGVBUS_RISE	Charge VBUS control rise IRQ status Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
11	DISCHRGVBUS_RISE	Discharge VBUS control rise IRQ status Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
10:9	RESERVED		R	0x0
8	IDPULLUP_RISE	ID pullup control rise IRQ status Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
7:6	RESERVED		R	0x0
5	DRVVBUS_FALL	Drive VBUS control fall IRQ status Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
4	CHRGVBUS_FALL	Charge VBUS control fall IRQ status Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
3	DISCHRGVBUS_FALL	Discharge VBUS control fall IRQ status Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0
2:1	RESERVED		R	0x0
0	IDPULLUP_FALL	ID pullup control fall IRQ status Write 0x0: No action Write 0x1: Trigger IRQ event by software Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toSet	0

Table 23-1372. Register Call Summary for Register USBOTGSS_IRQSTATUS_RAW_1

Super-Speed USB OTG Subsystem

- USBOTGSS_WRAPPER Register Summary: [0]

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Table 23-1373. USBOTGSS_IRQSTATUS_1

Address Offset	0x0000 0038
Physical Address	0x4A02 0038 **Instance** USBOTGSS_WRAPPER
Description	Regular status of secondary interrupt requests. Set only when enabled. Write 1 to clear after interrupt is serviced (raw status also gets cleared).
Type	RW DMA-disable self-clear IRQ status: USBOTGSS_SYSCONFIG[17] DMADISABLE hardware-cleared (to 0) because of DMA access. Not triggered by a software clear. OTG event in core, IRQ status: see status register USBOTGSS_OEVT.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DMADISABLECLR	OEVT	RESERVED		DRVVBUS_RISE	CHRGVBUS_RISE	DISCHRGVBUS_RISE	RESERVED		IDPULLUP_RISE	RESERVED		DRVVBUS_FALL	CHRGVBUS_FALL	DISCHRGVBUS_FALL	RESERVED		IDPULLUP_FALL

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	DMADISABLECLR	DMA-disable self-clear IRQ status: USBOTGSS_SYSCONFIG[17] DMADISABLE hardware-cleared (to 0) because of DMA access. Not triggered by a software clear. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
16	OEVT	OTG event in core, IRQ status: see status register USBOTGSS_OEVT. Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
15:14	RESERVED		R	0x0
13	DRVVBUS_RISE	Drive VBUS control rise IRQ status Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
12	CHRGVBUS_RISE	Charge VBUS control rise IRQ status Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
11	DISCHRGVBUS_RISE	Discharge VBUS control rise IRQ status Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
10:9	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
8	IDPULLUP_RISE	ID pullup control rise IRQ status Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
7:6	RESERVED		R	0x0
5	DRVVBUS_FALL	Drive VBUS control fall IRQ status Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
4	CHRGVBUS_FALL	Charge VBUS control fall IRQ status Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
3	DISCHRGVBUS_FALL	Discharge VBUS control fall IRQ status Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0
2:1	RESERVED		R	0x0
0	IDPULLUP_FALL	ID pullup control fall IRQ status Write 0x0: No action Write 0x1: Clear pending event, if any Read 0x1: IRQ event pending Read 0x0: No event pending	RW W1toClr	0

Table 23-1374. Register Call Summary for Register USBOTGSS_IRQSTATUS_1

Super-Speed USB OTG Subsystem

- Wrapper Events: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- System Power Management: [10]
- USBOTGSS_WRAPPER Register Summary: [11]

Table 23-1375. USBOTGSS_IRQENABLE_SET_1

Address Offset	0x0000 003C		
Physical Address	0x4A02 003C	**Instance**	USBOTGSS_WRAPPER
Description	Enable secondary interrupt requests. Write 1 to set (that is, to enable interrupt). Readout is the same as corresponding _CLR register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DMADISABLECLR_EN	OEVT_EN	RESERVED		DRVVBUS_RISE_EN	CHRGVBUS_RISE_EN	DISCHRGVBUS_RISE_EN	RESERVED		IDPULLUP_RISE_EN	RESERVED		DRVVBUS_FALL_EN	CHRGVBUS_FALL_EN	DISCHRGVBUS_FALL_EN	RESERVED		IDPULLUP_FALL_EN

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	DMADISABLECLR_EN	DMA-disable self-clear, IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
16	OEVT_EN	OTG event in core, IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
15:14	RESERVED		R	0x0
13	DRVVBUS_RISE_EN	Drive VBUS control rise IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
12	CHRGVBUS_RISE_EN	Charge VBUS control rise IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
11	DISCHRGVBUS_RISE_EN	Discharge VBUS control rise IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
10:9	RESERVED		R	0x0
8	IDPULLUP_RISE_EN	ID pullup control rise IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
7:6	RESERVED		R	0x0
5	DRVVBUS_FALL_EN	Drive VBUS control fall IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0

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Bits	Field Name	Description	Type	Reset
4	CHRGVBUS_FALL_EN	Charge VBUS control fall IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
3	DISCHRGVBUS_FALL_EN	Discharge VBUS control fall IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0
2:1	RESERVED		R	0x0
0	IDPULLUP_FALL_EN	ID pullup control fall IRQ enable Write 0x0: No action Write 0x1: Set IRQ enable (i.e. enable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toSet	0

Table 23-1376. Register Call Summary for Register USBOTGSS_IRQENABLE_SET_1

Super-Speed USB OTG Subsystem

- Wrapper Events: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- USBOTGSS_WRAPPER Register Summary: [10]

Table 23-1377. USBOTGSS_IRQENABLE_CLR_1

Address Offset	0x0000 0040		
Physical Address	0x4A02 0040	**Instance**	USBOTGSS_WRAPPER
Description	Enable secondary interrupt requests. Write 1 to clear (that is, to disable interrupt). Readout is the same as corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DMADISABLECLR_EN	OEVT_EN	RESERVED		DRVVBUS_RISE_EN	CHRGVBUS_RISE_EN	DISCHRGVBUS_RISE_EN	RESERVED		IDPULLUP_RISE_EN	RESERVED		DRVVBUS_FALL_EN	CHRGVBUS_FALL_EN	DISCHRGVBUS_FALL_EN	RESERVED		IDPULLUP_FALL_EN

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17	DMADISABLECLR_EN	DMA-disable self-clear, IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
16	OEVT_EN	OTG event in core, IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
15:14	RESERVED		R	0x0
13	DRVVBUS_RISE_EN	Drive VBUS control rise IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
12	CHRGVBUS_RISE_EN	Charge VBUS control rise IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
11	DISCHRGVBUS_RISE_EN	Discharge VBUS control rise IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
10:9	RESERVED		R	0x0
8	IDPULLUP_RISE_EN	ID pullup control rise IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
7:6	RESERVED		R	0x0
5	DRVVBUS_FALL_EN	Drive VBUS control fall IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
4	CHRGVBUS_FALL_EN	Charge VBUS control fall IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
3	DISCHRGVBUS_FALL_EN	Discharge VBUS control fall IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0
2:1	RESERVED		R	0x0
0	IDPULLUP_FALL_EN	ID pullup control fall IRQ enable Write 0x0: No action Write 0x1: Clear IRQ enable (i.e. disable event) Read 0x1: IRQ event is enabled Read 0x0: IRQ event is disabled	RW W1toClr	0

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Table 23-1378. Register Call Summary for Register USBOTGSS_IRQENABLE_CLR_1

Super-Speed USB OTG Subsystem

- Wrapper Events: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
- USBOTGSS_WRAPPER Register Summary: [10]

Table 23-1379. USBOTGSS_UTMI_OTG_CTRL

Address Offset	0x0000 0080		
Physical Address	0x4A02 0080	**Instance**	USBOTGSS_WRAPPER
Description			
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DRVVBUS	CHRGVBUS	DISCHRGVBUS	RESERVED		IDPULLUP

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x000 0000
5	DRVVBUS	Drive 5V on VBUS. Plays the role of "hub_vbus_ctrl" in non-OTG host mode. Read 0x1: drive VBUS Read 0x0: no action	R	0
4	CHRGVBUS	Charge VBUS through a resistor for VBUS-pulsing SRP. Read 0x1: charge VBUS Read 0x0: No action	R	0
3	DISCHRGVBUS	Discharge VBUS through a resistor, until the session-end VBUS state is reached. Read 0x1: discharge VBUS Read 0x0: no action	R	0
2:1	RESERVED		R	0x0
0	IDPULLUP	Pull-up to the (OTG) ID line to allow its sampling Read 0x1: Enable sampling of ID line. Read 0x0: Disable sampling of ID line.	R	1

Table 23-1380. Register Call Summary for Register USBOTGSS_UTMI_OTG_CTRL

Super-Speed USB OTG Subsystem

- Mailbox VBUS/ID Management: [0]
- USBOTGSS_WRAPPER Register Summary: [1]

Table 23-1381. USBOTGSS_UTMI_OTG_STATUS

Address Offset	0x0000 0084		
Physical Address	0x4A02 0084	**Instance**	USBOTGSS_WRAPPER
Description			
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW_MODE	RESERVED																				PORT_OVERCURRENT	POWERPRESENT	TXBITSTUFFENABLE	RESERVED			IDDIG	SESSEND	SESSVALID	VBUSVALID	RESERVED

Bits	Field Name	Description	Type	Reset
31	SW_MODE	Controls the source of UTMI / PIPE status for VBUS and OTG ID (vbusvalid, sessvalid, sessend, iddig, powerpresent) 0x0: Hardware mode: OTG ID and VBUS status for the USB controller are taken from the UTMI inputs signals 0x1: Software mode: OTG ID and VBUS status for the USB controller are taken from the fields of the current register.	RW	1
30:11	RESERVED		R	0x0 0000
10	PORT_OVERCURRENT	Over-current status, for non-OTG host only. 0x0: No over-current indication 0x1: Over-current indication	RW	0
9	POWERPRESENT	Software-programmed value of PIPE3.0 PowerPresent (VBUS status) seen by the core, alternative to HW input.	RW	0
8	TXBITSTUFFENABLE	Software-programmed UTMI output txbitstuffenable[h] Note: as per UTMI+, used only in UTMI Opmode 0b11 (i.e. SYNC and EOP generation disabled) 0x0: No bitstuffing 0x1: Data bitstuffing enabled	RW	0
7:5	RESERVED		R	0x0
4	IDDIG	Software-programmed value of UTMI+ IdDig (OTG ID status) seen by the core, alternative to hardware input. Don't care until IdPullup = 1 for at least 50 ms 0x0: ID pin is grounded = OTG A = default Host 0x1: ID pin is floating = OTG B = default Peripheral	RW	1
3	SESSEND	Software-programmed value of UTMI+ SessEnd (VBUS status) seen by the core, alternative to HW input. 0x0: VBUS is above Session-End threshold 0x1: VBUS is below Session-End threshold	RW	1
2	SESSVALID	Software-programmed value of UTMI+ SessValid (VBUS status) seen by the core, alternative to hardware inputs AValid and BValid. 0x0: VBUS is below Session-Valid threshold 0x1: VBUS is above Session-Valid threshold	RW	0
1	VBUSVALID	Software-programmed value of UTMI+ VbusValid (VBUS status) seen by the core, alternative to hardware input. 0x0: VBUS is below Vbus-Valid threshold. 0x1: VBUS is above Vbus-Valid threshold	RW	0
0	RESERVED		R	0

Table 23-1382. Register Call Summary for Register USBOTGSS_UTMI_OTG_STATUS

Super-Speed USB OTG Subsystem

- Mailbox VBUS/ID Management: [0] [1]
- USBOTGSS_WRAPPER Register Summary: [2]

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Table 23-1383. USBOTGSS_MMRAM_OFFSET

Address Offset	0x0000 0100		
Physical Address	0x4A02 0100	**Instance**	USBOTGSS_WRAPPER
Description	Offset of Memory-mapped RAM accesses. Page is remapped from 0x8000 to 0xFFFF (32 KiB)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OFFSET_MSB								OFFSET_LSB															

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:15	OFFSET_MSB	Byte offset MSBits = page offset 0x0: Page offset for core register set, lower half. DO NOT USE: use static access at offset 0x1_0000+ instead. 0x1: Page offset for core register set, upper half. DO NOT USE: use static access at offset 0x1_0000+ instead. 0x18: Base page offset for RAM2 (= core byte address 0xC_0000) RAM NOT IMPLEMENTED 0x10: Base page offset for RAM1 (= core byte address 0x8_0000): Tx FIFOs. The RAM shall fit inside this page for up to 32 kByte = 8,192 x 64-bit words. 0x8: Base page offset for RAM0 (= core byte address 0x4_0000): Rx FIFOs, descriptors, registers. The RAM shall fit inside this page for up to 32 kByte = 8,192 x 64-bit words	RW	0x08
14:0	OFFSET_LSB	Byte offset LSBits, always 0	R	0x0000

Table 23-1384. Register Call Summary for Register USBOTGSS_MMRAM_OFFSET

Super-Speed USB OTG Subsystem

- Core Space Remapping: [0] [1]
- USBOTGSS_WRAPPER Register Summary: [2]

Table 23-1385. USBOTGSS_FLADJ

Address Offset	0x0000 0104		
Physical Address	0x4A02 0104	**Instance**	USBOTGSS_WRAPPER
Description	Jitter adjustment parameters		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CORE_SW_RESET	RESERVED	XHCI_REVISION	HOST_U3_PORT_DISABLE	HOST_U2_PORT_DISABLE	FLADJ_30MHZ											RESERVED															

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Bits	Field Name	Description	Type	Reset
31	CORE_SW_RESET	Active-high core software reset. Static, i.e. not self-clearing. After clearing, wait for reset completion by polling USBOTGSS_USBSTS[11] CNR bit. 0x0: Reset inactive 0x1: Reset active	RW	0
30	RESERVED		R	0
29	XHCI_REVISION	Switches to the legacy xHCI 0.96 host SW API mode. Changes shall take place under core software reset: [31] CORE_SW_RESET = 1. 0x0: xHCI version 0.96 0x1: xHCI version 1.0 + errata	RW	1
28	HOST_U3_PORT_DISABLE	USB3 port disable, overriding xHCI driver. 0x0: Port can be enabled. 0x1: Port stops reporting connect/disconnect events and remains in disabled state.	RW	0
27	HOST_U2_PORT_DISABLE	USB2 port disable, overriding xHCI driver. 0x0: Port can be enabled. 0x1: Port stops reporting connect/disconnect events and remains in disabled state.	RW	0
26:21	FLADJ_30MHZ	HS Jitter Adjustment, in 30-MHz periods	RW	0x20
20:0	RESERVED		R	0x00 0000

Table 23-1386. Register Call Summary for Register USBOTGSS_FLADJ

Super-Speed USB OTG Subsystem

- Software Reset: [0] [1]
- xHCI USB Host Software API: [2] [3] [4]
- USBOTGSS_WRAPPER Register Summary: [5]

Table 23-1387. USBOTGSS_DEBUG_CFG

Address Offset	0x0000 0108		
Physical Address	0x4A02 0108	**Instance**	USBOTGSS_WRAPPER
Description	Configuration of debug output (observability)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														SEL	

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2:0	SEL	selection of observed local signals 0x1: Debug output is a selection of UTMI (USB2 PHY) interface signals 0x0: Debug output is tied low (32'b0) 0x2: Debug output is a selection of PIPE (USB3 PHY) interface signals 0x4: Debug output is lower 32 bits controller core's internal trace vector, selected by USBOTGSS_GDBGLSPMUX[21:16] TRACEPORTMUXSEL 0x5: Debug output is upper 32 bits controller core's internal trace vector, selected by USBOTGSS_GDBGLSPMUX[21:16] TRACEPORTMUXSEL 0x3: Debug output is controller core's internal debug signals	RW	0x0

Table 23-1388. Register Call Summary for Register USBOTGSS_DEBUG_CFG

Super-Speed USB OTG Subsystem

- Observability Debug Interface: [0] [1] [2] [3] [4]
- USBOTGSS_WRAPPER Register Summary: [5]
- USBOTGSS_WRAPPER Register Description: [6]

Table 23-1389. USBOTGSS_DEBUG_DATA

Address Offset	0x0000 010C		
Physical Address	0x4A02 010C	**Instance**	USBOTGSS_WRAPPER
Description	Data currently visible on DEBUG output (observability) port See USBOTGSS_DEBUG_CFG[2:0] SEL bit field.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG31	DEBUG30	DEBUG29	DEBUG28	DEBUG27	DEBUG26	DEBUG25	DEBUG24	DEBUG23	DEBUG22	DEBUG21	DEBUG20	DEBUG19	DEBUG18	DEBUG17	DEBUG16	DEBUG15	DEBUG14	DEBUG13	DEBUG12	DEBUG11	DEBUG10	DEBUG9	DEBUG8	DEBUG7	DEBUG6	DEBUG5	DEBUG4	DEBUG3	DEBUG2	DEBUG1	DEBUG0

Bits	Field Name	Description	Type	Reset
31	DEBUG31	SEL = 1: utmi_sessend SEL = 2: pipe_rxstatus[2] SEL = 3: core_sm2bl_cur_mode	R	0
30	DEBUG30	SEL = 1: utmi_vbusvalid SEL = 2: pipe_rxstatus[1] SEL = 3: core_suspend_n	R	0
29	DEBUG29	SEL = 1: utmi_bvalid SEL = 2: pipe_rxstatus[0] SEL = 3: core_suspend_com_n	R	0
28	DEBUG28	SEL = 1: utmi_avalid SEL = 2: pipe_elecidle SEL = 3: core_u2_dssr_state[3]	R	0
27	DEBUG27	SEL = 1: utmi_iddig SEL = 2: pipe_phystatus SEL = 3: core_u2_dssr_state[2]	R	0
26	DEBUG26	SEL = 1: utmi_hostdisconnect SEL = 2: pipe_rxvalid SEL = 3: core_u2_dssr_state[1]	R	0

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Bits	Field Name	Description	Type	Reset
25	DEBUG25	SEL = 1: utmi_txbitstuffenableh SEL = 2: pipe_rxdatak[3] SEL = 3: core_u2_dssr_state[0]	R	0
24	DEBUG24	SEL = 1: utmi_txbitstuffenable SEL = 2: pipe_rxdatak[2] SEL = 3: core_u2mac_txrx_state_1[4]	R	0
23	DEBUG23	SEL = 1: utmi_dischrgvbus SEL = 2: pipe_rxdatak[1] SEL = 3: core_u2mac_txrx_state_1[3]	R	0
22	DEBUG22	SEL = 1: utmi_chrgvbus SEL = 2: pipe_rxdatak[0] SEL = 3: core_u2mac_txrx_state_1[2]	R	0
21	DEBUG21	SEL = 1: utmi_drvvbus SEL = 2: pipe_rxpclk SEL = 3: core_u2mac_txrx_state_1[1]	R	0
20	DEBUG20	SEL = 1: utmi_dmpulldown SEL = 2: pipe_rxtermination SEL = 3: core_u2mac_txrx_state_1[0]	R	0
19	DEBUG19	SEL = 1: utmi_dppulldown SEL = 2: pipe_txswing SEL = 3: core_u2mac_txrx_state_0[4]	R	0
18	DEBUG18	SEL = 1: utmi_idpullup SEL = 2: pipe_txmargin[2] SEL = 3: core_u2mac_txrx_state_0[3]	R	0
17	DEBUG17	SEL = 1: utmi_linestate[1] SEL = 2: pipe_txmargin[1] SEL = 3: core_u2mac_txrx_state_0[2]	R	0
16	DEBUG16	SEL = 1: utmi_linestate[0] SEL = 2: pipe_txmargin[0] SEL = 3: core_u2mac_txrx_state_0[1]	R	0
15	DEBUG15	SEL = 1: utmi_opmode[1] SEL = 2: pipe_txdeemph[1] SEL = 3: core_u2mac_txrx_state_0[0]	R	0
14	DEBUG14	SEL = 1: utmi_opmode[0] SEL = 2: pipe_txdeemph[0] SEL = 3: core_u2_prt_state[4]	R	0
13	DEBUG13	SEL = 1: utmi_termSELect SEL = 2: pipe_powerdown[1] SEL = 3: core_u2_prt_state[3]	R	0
12	DEBUG12	SEL = 1: utmi_xcvrselect[1] SEL = 2: pipe_powerdown[0] SEL = 3: core_u2_prt_state[2]	R	0
11	DEBUG11	SEL = 1: utmi_xcvrselect[0] SEL = 2: pipe_reset_n SEL = 3: core_u2_prt_state[1]	R	0
10	DEBUG10	SEL = 1: utmi_suspendm SEL = 2: pipe_rxeqtraining SEL = 3: core_u2_prt_state[0]	R	0
9	DEBUG9	SEL = 1: utmi_reset SEL = 2: pipe_rxpolarity SEL = 3: core_gsts_buserraddvld	R	0
8	DEBUG8	SEL = 1: utmi_rxerror SEL = 2: pipe_txoneszeros SEL = 3: debug_mclk_usof_number[0]	R	0
7	DEBUG7	SEL = 1: utmi_rxvalidh SEL = 2: pipe_txelecidle SEL = 3: core_ltdb_link_state[3]	R	0
6	DEBUG6	SEL = 1: utmi_rxvalid SEL = 2: pipe_txdetectrxloopback SEL = 3: core_ltdb_link_state[2]	R	0

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Bits	Field Name	Description	Type	Reset
5	DEBUG5	SEL = 1: utmi_rxactive SEL = 2: pipe_elasticitybuffermode SEL = 3: core_ltdb_link_state[1]	R	0
4	DEBUG4	SEL = 1: utmi_txready SEL = 2: pipe_txdatak[3] SEL = 3: core_ltdb_link_state[0]	R	0
3	DEBUG3	SEL = 1: utmi_txvalidh SEL = 2: pipe_txdatak[2] SEL = 3: core_ltdb_substate[3]	R	0
2	DEBUG2	SEL = 1: utmi_txvalid SEL = 2: pipe_txdatak[1] SEL = 3: core_ltdb_substate[2]	R	0
1	DEBUG1	SEL = 1: utmi_databus16_8 SEL = 2: pipe_txdatak[0] SEL = 3: core_ltdb_substate[1]	R	0
0	DEBUG0	SEL = 1: utmi_clk SEL = 2: pipe_txpclk SEL = 3: core_ltdb_substate[0]	R	0

Table 23-1390. Register Call Summary for Register USBOTGSS_DEBUG_DATA

Super-Speed USB OTG Subsystem

- Observability Debug Interface: [0] [1] [2]
- USBOTGSS_WRAPPER Register Summary: [3]

Table 23-1391. USBOTGSS_DEV_EBC_EN

Address Offset	0x0000 0110		
Physical Address	0x4A02 0110	**Instance**	USBOTGSS_WRAPPER
Description	Enable External Buffer Control (EBC) for selected endpoints. Device mode only.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTEP15	RESERVED															INEP15	RESERVED														

Bits	Field Name	Description	Type	Reset
31	OUTEP15	Enable EBC HW throttling for OUT EP 15 (USB receive) 0x0: EBC disabled 0x1: EBC enabled. USBOTGSS_DEPCMDPAR1_i[15] shall also be set to 1 in DEPCFG command for this EP.	RW	0
30:16	RESERVED		R	0x0000
15	INEP15	Enable EBC HW throttling for IN EP 15 (USB transmit) 0x0: EBC disabled 0x1: EBC enabled. USBOTGSS_DEPCMDPAR1_i[15] shall also be set to 1 in DEPCFG command for this EP.	RW	0
14:0	RESERVED		R	0x0000

Table 23-1392. Register Call Summary for Register USBOTGSS_DEV_EBC_EN

Super-Speed USB OTG Subsystem

- External Buffer Control (EBC) Mode Operation: [0]
- IN (Tx) EP Operation In EBC Mode: [1]
- OUT (Rx) EP Operation in EBC Mode: [2]
- USBOTGSS_WRAPPER Register Summary: [3]

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23.11.5.4 USB2PHY Registers

CAUTION

The USB2PHY registers are limited to 32-bit data accesses; 16- and 8-bit accesses are not allowed and can corrupt register content.

Reserved bit fields must not be modified.

NOTE: No USB2PHY register settings need to be done in order USB2PHY to operate in default USB2.0 (HS, FS, or LS mode) condition. Registers are provided only for debug purposes.

23.11.5.4.1 USB2PHY Register Summary

Table 23-1393. USB2PHY Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
USB2PHY_TERMINATION_CONTROL	RW	32	0x0000 0000	0x4A08 4000
USB2PHY_CHRG_DET	RW	32	0x0000 0014	0x4A08 4014
USB2PHY_GPIO	RW	32	0x0000 0030	0x4A08 4030
USB2PHY_AD_INTERFACE_REG3	RW	32	0x0000 0048	0x4A08 4048
USB2PHY_ANA_CONFIG2	RW	32	0x0000 0050	0x4A08 4050
USB2PHY_CEGPIO_REG	RW	32	0x0000 0078	0x4A08 4078

23.11.5.4.2 USB2PHY Register Description

Table 23-1394. USB2PHY_TERMINATION_CONTROL

Address Offset	0x0000 0000		
Physical Address	0x4A08 4000	**Instance**	USB2PHY
Description	Contains bits related to control of terminations in USB2PHY		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										MEM_USE_RTERM_RMX_REG	MEM_RTERM_RMX					RESERVED								RTERM_RMX							

Bits	Field Name	Description	Type	Reset
31:22	RESERVED	Reserved	RW	0x01C
21	MEM_USE_RTERM_RMX_REG	Override termination resistor trim code with MEM_RTERM_RMX bitfield value	RW	0

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Bits	Field Name	Description	Type	Reset
20:15	MEM_RTERM_RMX	The value written to this field is used as termination resistor trim code if bit [21] MEM_USE_RTERM_RMX_REG is set to 1	RW	0x00
14:6	RESERVED	Reserved	RW	0x000
5:0	RTERM_RMX	Returns the current value of RTERM_RMX	R	0x00

Table 23-1395. Register Call Summary for Register USB2PHY_TERMINATION_CONTROL

Super-Speed USB OTG Subsystem

- USB2PHY Register Summary: [0]

Table 23-1396. USB2PHY_CHRG_DET

Address Offset	0x0000 0014		
Physical Address	0x4A08 4014	**Instance**	USB2PHY
Description	This is the charger detect register. This register is not used in the dead battery case.		
Type	RW		

31 30	29	28	27	26	25	24	23	22	21	20 19	18	17	16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1	0
RESERVED	MEM_USE_CHG_DET_REG	MEM_DIS_CHG_DET	MEM_SRC_ON_DM	MEM_SINK_ON_DP	MEM_CHG_DET_EXT_CTL	MEM_RESTART_CHG_DET	CHG_DET_DONE	CHG_DETECTED	DATA_DET	RESERVED	MEM_CHG_ISINK_EN	MEM_CHG_VSRC_EN	COMP_DP	COMP_DM	RESERVED	MEM_FOR_CE

Bits	Field Name	Description	Type	Reset
31:30	RESERVED	Reserved	RW	0x0
29	MEM_USE_CHG_DET_REG	Use bits 28:24 and 18:17 from this register.	RW	0
28	MEM_DIS_CHG_DET	When read, returns current value of charger detect input. When MEM_USE_CHG_DET_REG = 1, the value written to this field overrides the corresponding charger detect input.	RW	0
27	MEM_SRC_ON_DM	When read, returns current value of charger detect input. When MEM_USE_CHG_DET_REG = 1, the value written to this field overrides the corresponding charger detect input.	RW	0
26	MEM_SINK_ON_DP	When read, returns current value of charger detect input. When MEM_USE_CHG_DET_REG = 1, the value written to this field overrides the corresponding charger detect input.	RW	0
25	MEM_CHG_DET_EXT_CTL	When read, returns current value of charger detect input. When MEM_USE_CHG_DET_REG = 1, the value written to this fileld overrides the corresponding charger detect input.	RW	0
24	MEM_RESTART_CHG_DET	Restart the charger detection protocol when this bit is set from 0 to 1	RW	0
23	CHG_DET_DONE	Charger detect protocol has completed	R	0
22	CHG_DETECTED	Reflects charger-enable (CE) output pin	R	0
21	DATA_DET	Output of the data detect comparator	R	0
20:19	RESERVED	Reserved	RW	0x0

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Bits	Field Name	Description	Type	Reset
18	MEM_CHG_ISINK_EN	When read, returns current value of charger detect input. When MEM_USE_CHG_DET_REG = 1, the value written to this field overrides the corresponding charger detect input.	RW	0
17	MEM_CHG_VSRC_EN	When read, returns current value of charger detect input. When MEM_USE_CHG_DET_REG = 1, the value written to this field overrides the corresponding charger detect input.	RW	0
16	COMP_DP	Comparator on the DP line value	R	0
15	COMP_DM	Comparator on the DM line value	R	0
14:1	RESERVED	Reserved	RW	0x0000
0	MEM_FOR_CE	Force output pin CE = 1, when this bit is set to 1.	RW	0

Table 23-1397. Register Call Summary for Register USB2PHY_CHRG_DET

Super-Speed USB OTG Subsystem

- USB2PHY Register Summary: [0]

Table 23-1398. USB2PHY_GPIO

Address Offset	0x0000 0030		
Physical Address	0x4A08 4030	**Instance**	USB2PHY
Description	GPIO mode configurations and read-only info fields		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM_USEGPIOMODEREG	MEM_GPIOMODE	MEM_DPGPIOGZ	MEM_DMGPIOGZ	MEM_DPGPIOA	MEM_DMGPIOA	DPGPIOY	DMGPIOY	RESERVED				MEM_DMGPIOPIPD	MEM_DPGPIOPIPD	RESERVED																			

Bits	Field Name	Description	Type	Reset
31	MEM_USEGPIOMODEREG	When set to 1, use bits 30:24 from this register instead of primary inputs.	RW	0
30	MEM_GPIOMODE	Overrides the GPIO MODE primary input	RW	0
29	MEM_DPGPIOGZ	Overrides the DP GPIO GZ primary input	RW	0
28	MEM_DMGPIOGZ	Overrides the DM GPIO GZ primary input	RW	0
27	MEM_DPGPIOA	Overrides the DP GPIO A primary input	RW	0
26	MEM_DMGPIOA	Overrides the DM GPIO A primary input	RW	0
25	DPGPIOY	DP GPIO Y output value status	R	0
24	DMGPIOY	DM GPIO Y output value status	R	0
23:20	RESERVED	Reserved	RW	0x0
19	MEM_DMGPIOPIPD	GPIO mode DM pulldown enabled. Overrides the corresponding primary input.	RW	0
18	MEM_DPGPIOPIPD	GPIO mode DP pulldown enabled. Overrides the corresponding primary input.	RW	0
17:0	RESERVED	Reserved	RW	0x0 0000

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Table 23-1399. Register Call Summary for Register USB2PHY_GPIO

Super-Speed USB OTG Subsystem

- USB2PHY Register Summary: [0]

Table 23-1400. USB2PHY_AD_INTERFACE_REG3

Address Offset	0x0000 0048		
Physical Address	0x4A08 4048	**Instance**	USB2PHY
Description	AD interface register 3		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MEM_SPARE_IN_LDO																RESERVED							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	RW	0x0000
17:10	MEM_SPARE_IN_LDO	This bit field can be used to compensate for external Common Mode Filter (CMF) or series switch resistance. Returns 0x0 on read, if VDDLDO is off. Example: If a CMF has series resistance of 4 ohms, that can be compensated by lower the output impedance of the driver by 4 ohms (0x4). **Note:** It is not recommended to use external components having more than 4-ohm series resistance on DP/DM path. If higher value of series resistance is used, PHY can only compensate that partially by using this option. 0x0: 0 ohms reduction in HS termination 0x1: 1 ohms reduction in HS termination 0x2: 2 ohms reduction in HS termination 0x3: 3 ohms reduction in HS termination 0x4: 4 ohms reduction in HS termination	RW	0x00
9:0	RESERVED	Reserved	R	0x000

Table 23-1401. Register Call Summary for Register USB2PHY_AD_INTERFACE_REG3

Super-Speed USB OTG Subsystem

- USB2PHY Register Summary: [0]

Table 23-1402. USB2PHY_ANA_CONFIG2

Address Offset	0x0000 0050		
Physical Address	0x4A08 4050	**Instance**	USB2PHY
Description	Used to configure and debug the analog blocks		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MEM_FSRX_TEST			RESERVED															

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		RW	0x000
19:15	MEM_FSRX_TEST	Following are the bit setting to improve HS eye diagram. These options should be used with higher value of external series resistance on DP/DM. bits [17:15] = 0x0: Default swing bits [17:15] = 0x3: 15-mV differential swing increase	RW	0x00

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Bits	Field Name	Description	Type	Reset
14:0	RESERVED	Reserved	RW	0x0000

Table 23-1403. Register Call Summary for Register USB2PHY_ANA_CONFIG2

Super-Speed USB OTG Subsystem

- USB2PHY Register Summary: [0]

Table 23-1404. USB2PHY_CEGPIO_REG

Address Offset	0x0000 0078		
Physical Address	0x4A08 4078	**Instance**	USB2PHY
Description	This register contains bits for configuring functionality for CE pad.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MEM_CE_SELECT							

Bits	Field Name	Description	Type	Reset
31:26	RESERVED	Reserved	R	0x00
25:16	RESERVED	Reserved	RW	0x271
15:6	RESERVED	Reserved	RW	0x000
5:0	MEM_CE_SELECT	CE pin output mode: 0x0 : Charger detected 0x1 : GPIO mode 0x2 : Suspendm 0x3 : !Suspendm 0x4 : Bus_reset 0x5 : !Bus_reset 0x6 : Suspendm + Bus_reset 0x7 : !(Suspendm + Bus_reset) 0x8 - 0xF: Reserved 0x10 - 0x28: Debug options	RW	0x00

Table 23-1405. Register Call Summary for Register USB2PHY_CEGPIO_REG

Super-Speed USB OTG Subsystem

- USB2PHY Register Summary: [0]

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23.12 SATA Controller

This chapter describes the features and functions of the device Serial Advanced Technology Attachment (SATA) host controller subsystem.

23.12.1 SATA Controller Overview

The SATA host controller handles data interactions between a local host system memory and a SATA mass storage device with minimal local host (LH) intervention.

In contrast to the parallel 16-bit - ATA (PATA) interface, the SATA interface takes advantage of serial data transmission/reception over a differential pair of conductors. SATA uses the command set from the ATA/ATAPI-6 standard augmented with native command queuing (NCQ) commands optimized for the serialized interface.

The device has one embedded SATA host bus adapter (HBA) controller with a single port. The device SATA host subsystem is composed of several functional components (see Figure 23-246):

- The core component of the SATA host controller subsystem (signified as SATA controller on the Figure 23-246) implements the transport and link layers of the SATA interface protocol ,i.e. all SATA media access control (MAC) functionalities.
- SATA_PHY encompasses the physical layer (PHY) components - serializer, de-serializer, etc. which adapt the generated by the SATA controller MAC logic parallel 10-bit output data stream for serial electrical transmission and reception.
- DPLL_SATA is a programmable (through registers of the integrated PLL controller - PLLCTRL_SATA) DPLL clock source that provides a high-speed clock to the SATA_PHY serializer/de-serializer components.
- An L4_CFG interface adapter - OCP2SCP3, which enables accessing the PLLCTRL_SATA registers via L4_CFG interconnect accesses.

For details regarding the device SATA host subsystem components - SATA_PHY, PLLCTRL_SATA, DPLL_SATA and interface adapter), see Section 27.1.1, *SATA PHY Subsystem Overview*, in Chapter 27, *Shared PHY Component Subsystems*.

Figure 23-246 shows an overview of the device-embedded SATA host controller subsystem.

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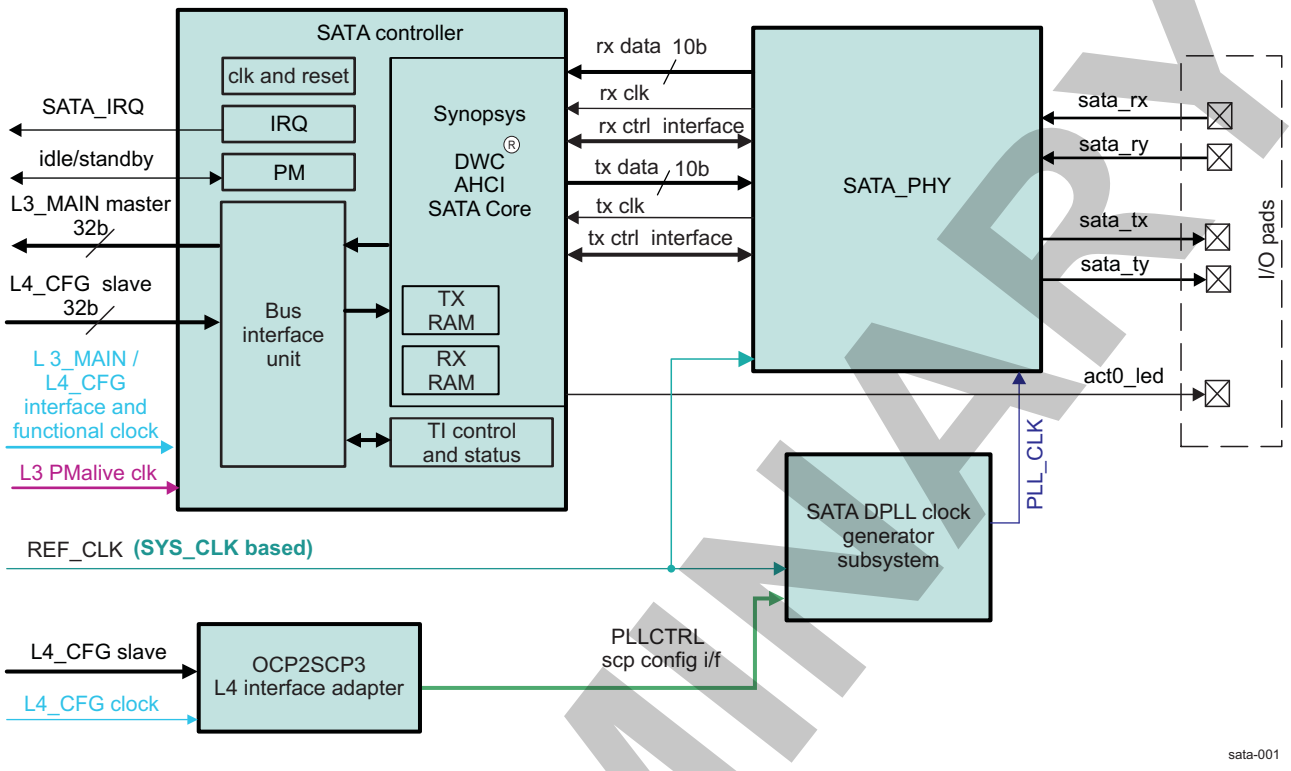
Figure 23-246. SATA Host Controller Subsystem Overview



23.12.1.1 SATA Controller

The SATA controller is the main functional component of the device-embedded SATA (Host Bus Adapter) HBA and is based on the Synopsys DesignWare® SATA Core advanced host controller interface (AHCI) module. The SATA controller handles data transactions at the link and transport layers of the SATA interface using the advanced host controller interface (AHCI) mechanism. The SATA controller core engine is a generation 2-compliant host (supporting 3 Gbps transfer speed) with integrated DMA and FIFO RAM buffers .

The SATA controller AHCI-based interactions involve extensive DMA processing of both data and command transfers, reducing much of the user overhead associated with standard ATA task file register servicing. The SATA HBA port programmable DMA acts as a master on the device L3_MAIN interconnect, which facilitates direct command/data transfers between host system memory and attached SATA storage devices.

The SATA controller has a slave configuration port accessible on the device L4_CFG interconnect. This port provides the user with an appropriate register interface for HBA setup, control and status, interrupt settings, DMA configuration, etc.

23.12.1.1.1 AHCI Mode Overview

The SATA core supports the AHCI hardware mechanism, which provides the user software with a suitable HBA register interface to manage SATA interface operations. Generally, the AHCI introduces a system memory structure that includes some generic control and status area and a list of command entries (which can have a depth from 1 up to 32 entries) assigned per HBA port. Each of the command list entries contains information necessary to program a SATA device and pointers to data transfer descriptors.

The AHCI mode of operation disregards the master/slave communication model. A certain SATA AHCI host controller port establishes a point-to-point connectivity with only a single SATA peripheral device at a time, which is always a master device.

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23.12.1.1.2 Native Command Queuing

The SATA AHCI engine supports NCQ and is capable of command queued protocol interactions with NCQ-compliant SATA mass storage devices. The NCQ commands generated by a SATA HBA port are loaded into command queues maintained at the peripheral device. The commands are stored in a queue and subsequently fetched and processed by peripheral device controller in sequences, which imply more native and highly-optimized for the device order of execution. The synchronization between an NCQ-aware SATA HBA and an NCQ-aware peripheral storage device involves implementation of the so called FPDMA queued command protocol, which ensures that HBA posts NCQ commands to the target SATA device in its demanded NCQ order.

23.12.1.1.3 SATA Transport Layer Functionalities

The SATA controller handles all of the transport layer functions of the SATA protocol. During reception it receives a frame information structure (FIS) from its link layer through the RX FIFO, decodes the type, and routes it to the proper location through the port DMA. During transmission it transfers a FIS constructed by the port DMA to the link layer through the TX FIFO. It also passes link layer errors and checks for transport layer errors to pass up to the system. The transport layer also contains the TX and RX FIFOs. These FIFOs are used as asynchronous data buffers between the serial domain and the bus clock domain. The size of these FIFOs affects the subsystem ability to buffer data before flow control must be asserted. It also affects the maximum transaction size that can be programmed into the port DMA.

23.12.1.1.4 SATA Link Layer Functionalities

The link layer maintains the link and supports all SATA link layer functionality, including:

- Out-of-band (OOB) transmit signaling
- Frame negotiation and arbitration
- Envelope framing/deframing
- Cyclic redundancy check (CRC) calculation (receive and transmit)
- 8b/10b encoding/decoding
- Flow control
- Frame acknowledgment and status
- Data width conversion
- Data scrambling/descrambling
- Primitive transmission
- Primitive detection and dropping
- Power management

23.12.1.2 SATA Controller Features

This section describes the features supplied by the SATA controller module. The SATA controller complies with the following standards:

- *Serial ATA Standard* specification (revision 2.6)
- *Serial ATA Advanced Host Controller Interface* specification (revision 1.1). The device SATA host controller also complies with the *Serial ATA Advanced Host Controller Interface* specification (revision 1.3), excluding support for the port multiplier FIS-based switching feature.

The main features of the SATA host controller are:

- Serial ATA 1.5-Gbps and 3-Gbps speeds (SATA-1 and SATA-2)
- Integrated RxFIFO and TxFIFO RAM data buffers
- Support of all SATA power management features
- AHCI support of 64-bit addressing mode (see device limitation note below)
- HBA port associated Internal DMA engine
- Hardware-assisted NCQ for up to 32 entries

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- Command completion coalescing (CCC) interrupts
- Activity LED generation

Additionally, link layer supports:

- 8b/10b encoding and decoding functionality
- RX elasticity buffer
- TX OOB sequence generation
- RX OOB sequence generation
- The differences between the SATA host controller and a standard SATA host controller defined by the *Serial ATA Gold Standard* specification (v2.6) are:
- Staggered spin-up is not supported (only one HBA AHCI port embedded).
- Only one port is supported by the device-embedded SATA HBA from up to 32 possible, according to the standard.
- The SATA controller is AHCI-mode compliant only and does not support standard ATA legacy modes of operation.
- Cold presence detection signals are not available. The SATA controller targets support for permanently attached SATA drives only.

The following features are not supported by the SATA host subsystem:

- Far-end analog loopback
- Cold presence detect (CPD) signal is not available at the system level. As a consequence, the SATA device hot-plug operation is not supported.
- Port multiplier feature is not supported by the device SATA controller port.
- Mechanical presence switch signal is not available at system level.
- Message signaled interrupts
- PHY layer functionalities of SATA controller are not integrated. These are assigned to the SATA_PHY transceiver integrated at the device level (outside SATA controller module itself).

NOTE: A save and restore mechanism is not supported for SATA. The SATA host controller must be restarted and reprogrammed every time it exits OFF mode or RETENTION mode.

The SATA controller master (DMA) interface features:

- 32-bit data
- 36 bits of the AHCI master address bus (byte-aligned addressing) implemented in the device. See device limitation note below.
- 1-bit tag-ID port, but the tag value is 1 on all accesses (that is, the feature is not used)
- Sequential burst support (16 x 32 bit – Dwords)

NOTE: Even though the SATA AHCI Controller supports 64-bit -addressing mode, only 36-lower bits of the 64-bit address bus are integrated (meaningful) in the device. This defines a 64-GiB AHCI master address space.

The SATA controller slave interface features:

- 32-bit data, 13-bit (byte-aligned) address
- Single access (no burst support)
- All accesses are expected to be 4 bytes wide, 32-bit aligned.

NOTE: Accesses smaller than 4 bytes wide (that is, byte enable patterns different from 4'b1111) are functional and do not generate an error. Misaligned addresses do not generate an error.

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23.12.2 SATA Controller Environment

Apart from the SATA communication-dedicated electrical connections to the SATA_PHY component, there is an additional SATA-defined-led drive generation signal that can be output at the device pad: uart3_cts_rctx. For more information about this signal pad configuration register mapping, see section Section 18.4.8, *Pad Functional Multiplexing and Configuration* in Chapter 18, *Control Module*. For more details regarding the behavior of activity LED generation, see Section 23.12.4.9, *Activity LED Generation Functionality*.

Table 23-1406. SATA Controller I/O Signals

Module Pin Name	Device Level Signal Name	I/O[1]	Description	Module Pin Reset Value
TXP[2]	sata_tx	O	TX output of the SATA PHY differential transmission line	0
TXN[2]	sata_ty	O	TY output of the SATA PHY differential transmission line	0
RXP[2]	sata_rx	I	RX input of the SATA PHY differential reception line	Hi-Z
RXN[2]	sata_ry	I	RY input of the SATA PHY differential reception line	Hi-Z
ACT0_LED	sata_actled	O	HBA port activity LED indication	Hi-Z

(1) I = Input; O = Output

(2) These signals are part of the interface between SATA PHY serializer / de-serializer and the externally attached SATA storage device.

NOTE: The path from module pin to device pad(s) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and is programmable in the Control Module registers. For more information, refer to the sections Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*, for more information.

The Figure 23-247 shows the SATA host controller subsystem environment summarizing the interface signals exported directly from SATA controller at the device boundary, as well as those exported after SATA_PHY processing at the device boundary. For more information on the interface between the SATA controller and SATA_PHY, seeChapter 27, *Shared PHY Component Subsytems*.

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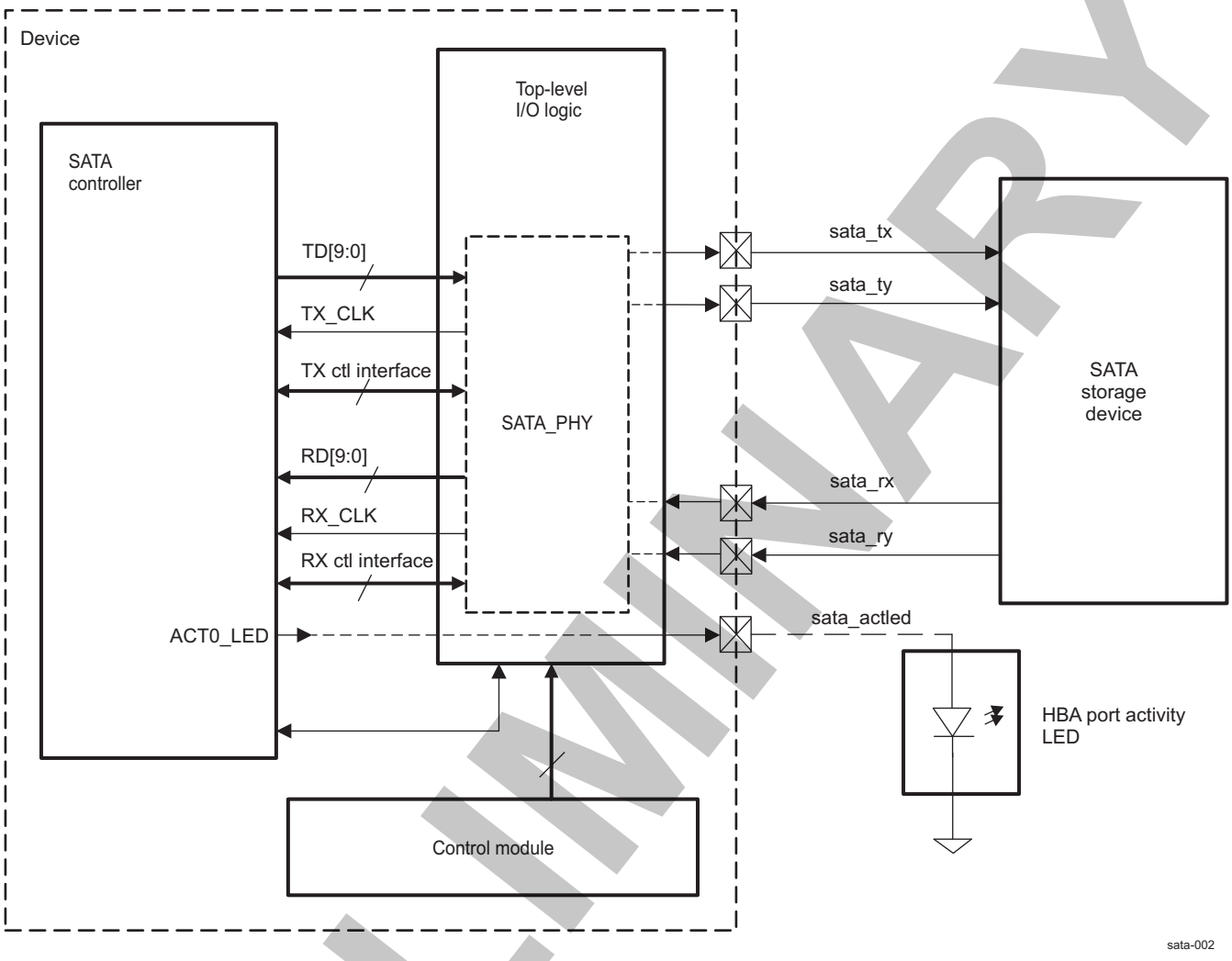
Figure 23-247. SATA Subsystem Environment



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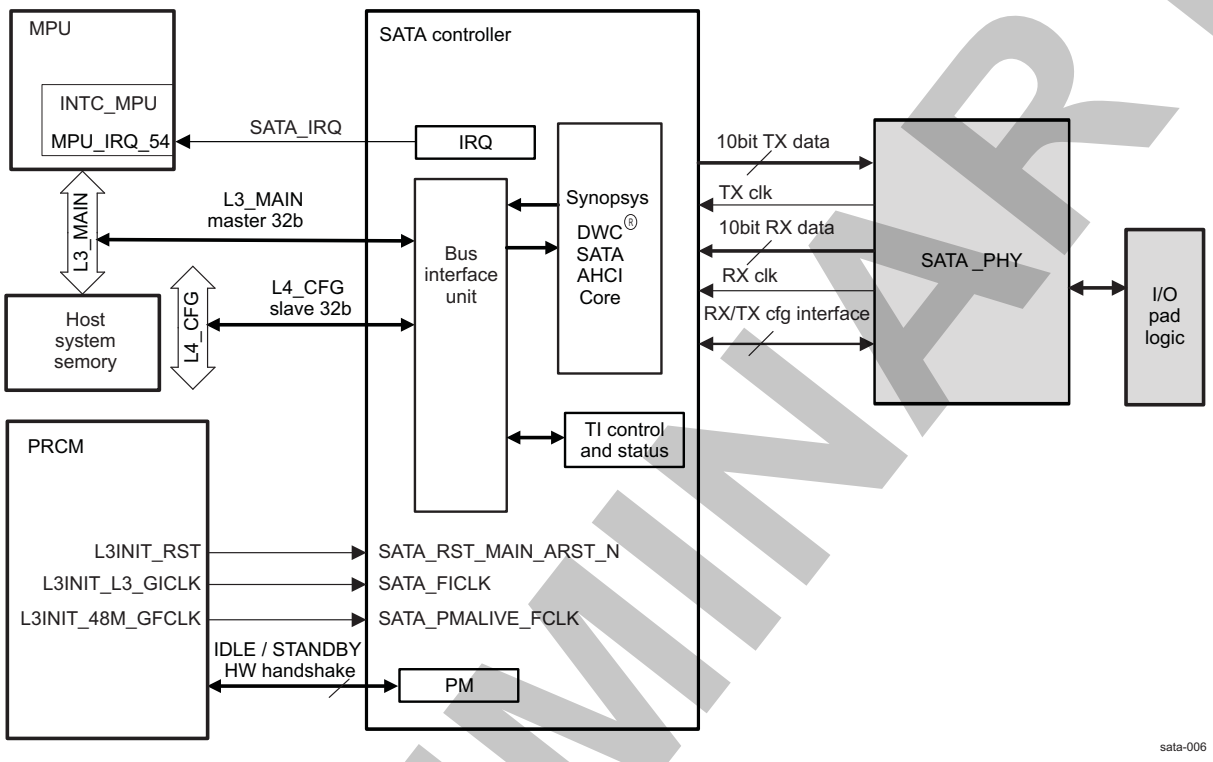
23.12.3 SATA Controller Integration

This section describes the SATA AHCI host controller integration in the device, including information about clocks, resets, and hardware requests. Figure 23-248 shows the SATA controller integration.

Figure 23-248. SATA Controller Integration



SATA controller integration includes these features:

- A single functional and interface clock (SATA_FICLK, shared between the master and the slave interfaces)
- A functional always-on clock (SATA_PMALIVE_FCLK to support entrance into and exit from the SATA defined low-power modes)
- A single hardware nonretention reset input (SATA_RST_MAIN_ARST_N)
- Idle/standby handshake protocol with the power, reset, and clock management (PRCM) module
- A single interrupt request generation line (SATA_IRQ, mapped to MPU_IRQ_54 of MPU INTC)
- No DMA or wakeup requests generation to surrounding modules
- L3_MAIN master interface
- L4_CFG-configuration slave interface

The SATA encoded symbol transmission/decoded symbol reception relies on two serial clocks , which are supplied indirectly from the DPLL_SATA through the SATA_PHY component.

NOTE: For more information about the IDLE hardware handshake and the wakeup request, see Section 3.1.1.1.2, *Module Level Clock Management* in Chapter 3, *Power, Reset, and Clock Management*.

Table 23-1407 through Table 23-1409 summarize the integration of the module in the device.

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Table 23-1407. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
SATA	PD_L3INIT	L4_CFG L3_MAIN

Table 23-1408. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SATA	SATA_FICLK	L3INIT_L3_GICLK	PRCM	SATA interface and functional clock
	SATA_PMALIVE_FCLK	L3INIT_48M_GFCLK	PRCM	Always-on SATA-specific, power-management support clock

Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SATA	SATA_RST_MAIN_ARST_N	L3INIT_RST	PRCM	A nonretention hardware reset

Table 23-1409. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
SATA	SATA_IRQ	MPU_IRQ_54	MPU INTC	SATA interrupt to MPU

NOTE:

- For a description of the interrupt source, see Section 23.12.4.5, *Interrupt Requests*.

NOTE:

- The SATA HBA does not generate DMA and wakeup hardware requests to the surrounding modules integrated in the device

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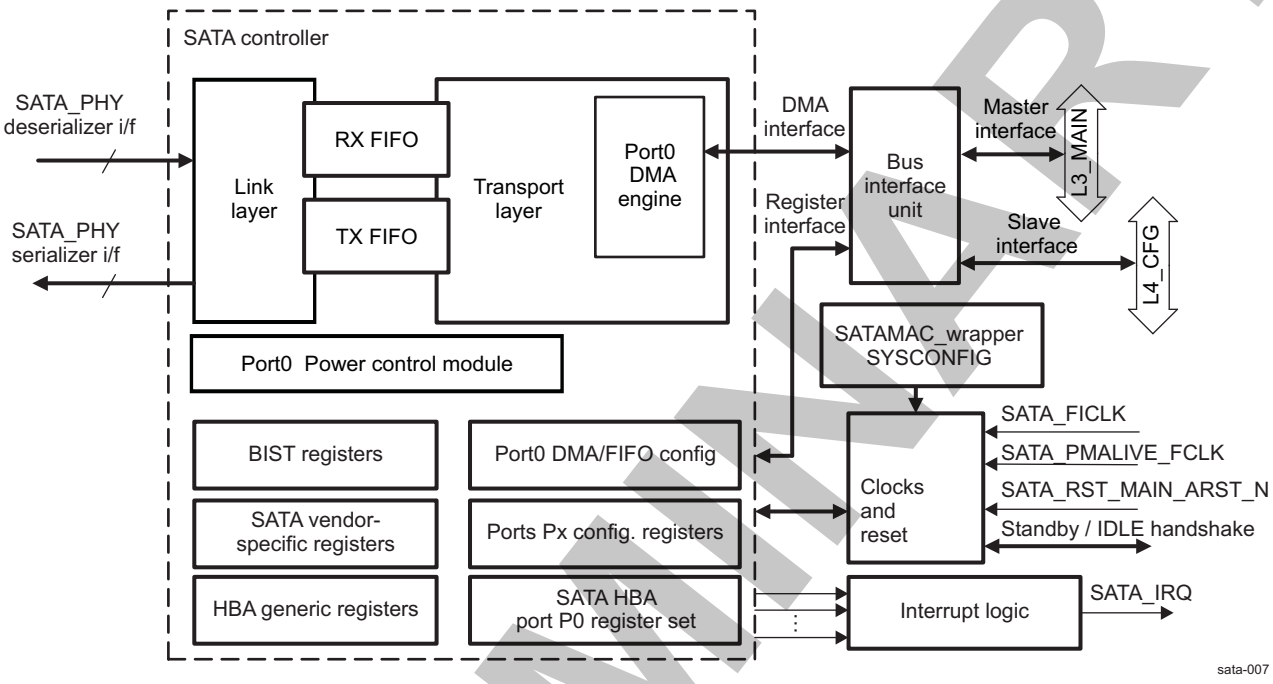
23.12.4 SATA Controller Functional Description

23.12.4.1 Block Diagram

Figure 23-249 shows a block diagram of the SATA host controller.

Figure 23-249. SATA Controller Functional Block Diagram



The SATA HBA port-associated DMA is a master on the device L3_MAIN interconnect. For a write to the attached storage device, this port reads FISs from the host system memory and pushes them into the transmit FIFO. When frame Dwords are received at RxFIFO, this interface is used to write the data out to the dedicated host system memory area. For details about DMA features and operation, see section Section 23.12.4.8, *DMA Port Configuration*.

The SATA controller has a configuration slave interface used to read and write all system registers. The slave interface includes the following functions:

- Configuring the SATA AHCI core (and indirectly, to a certain extent, the SATA_PHY physical component)
- Configuring the DMA for transmit and receive operations
- Initiating write transfers to the attached storage device
- Responding to interrupts and reads

Both the slave and master interface of the SATA host controller share the same functional and interface clock, that is, operate on the same frequency (see also Section 23.12.3, *SATA Controller Integration*) .

A bus interface unit adapts the SATA controller master and slave buses to the corresponding L3_MAIN and L4_CFG device interconnects.

NOTE: The **SATA controller AHCI Core registers** are part of the instance signified as **DWC_ahsata** inside the Section 23.12.6.1, *SATA Controller Instance Summary*.

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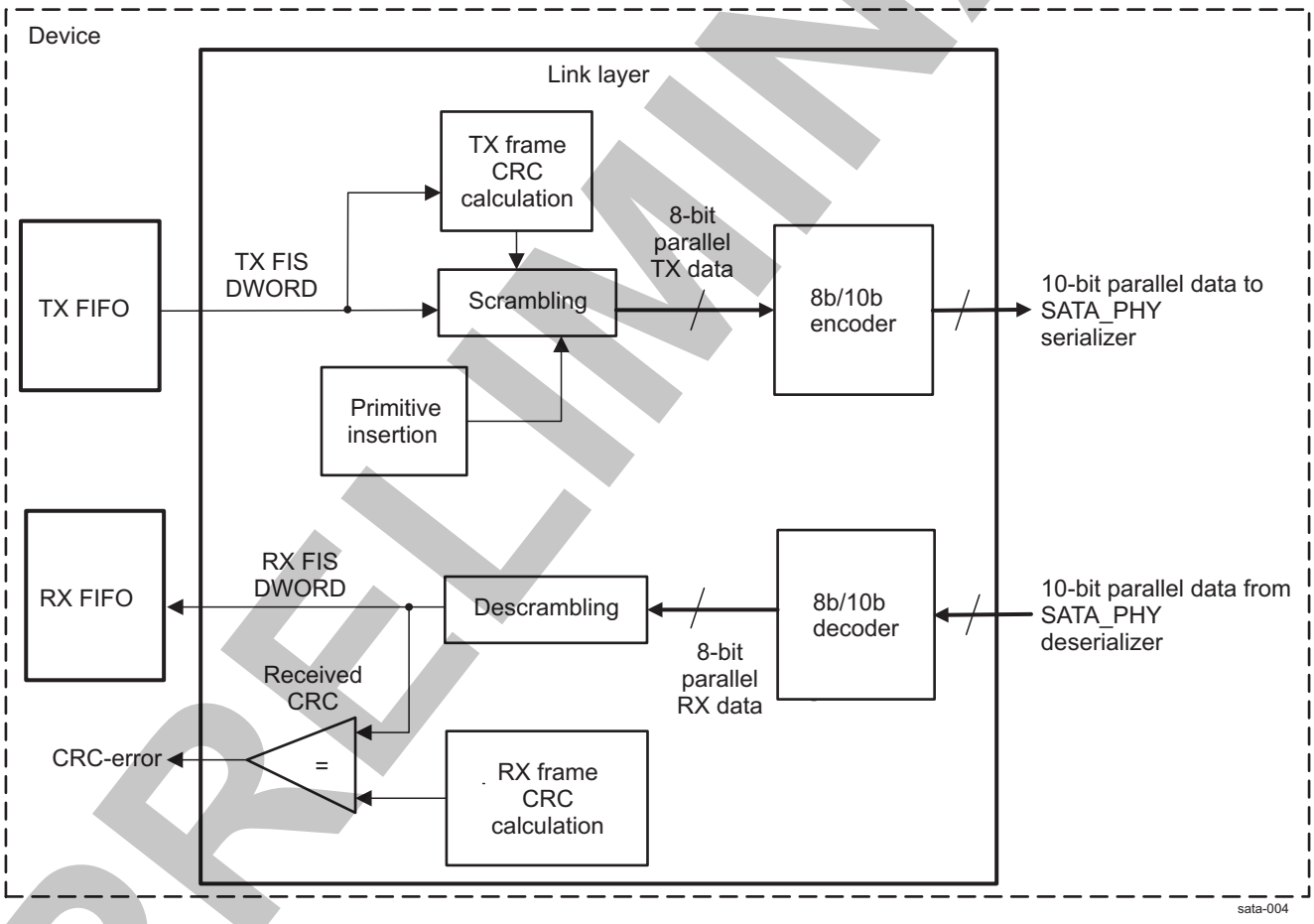
23.12.4.2 SATA Controller Link Layer Protocol and Data Format

One of the main tasks of the SATA HBA Link layer is to perform a parallel 8-bit FIS data to a 10-bit parallel code conversion (8b/10b encoding) . The encoded stream, which is a sequence of 10-bit parallel-encoded characters, is subsequently passed to the SATA_PHY serializer component to adapt to a serial 10-bit character transmission to the SATA peripheral device. For more details, see Section 27.1.1, *SATA PHY Subsystem Overview*, and Section 27.1.4, *SATA PHY Subsystem Functional Description,* in Chapter 27, *Shared PHY Component Subsytems*.

One of the main tasks of the SATA HBA Link receiver is to perform a 8b/10b decoding, in which process the parallel 10-bit characters coming out from the SATA_PHY de-serializer are decoded to parallel data or control bytes. The received symbols with invalid codes are rejected by the link layer and corresponding illegal reception errors are generated. For more details regarding the SATA_PHY de-serializer, see Section 27.1.1, *SATA PHY Subsystem Overview*, and Section 27.1.4, *SATA PHY Subsystem Functional Description,* in Chapter 27, *Shared PHY Component Subsytems*.

There are also other data process stages at the link layer, such as CRC calculation, scrambling/descrambling, primitive insertion/detection, etc. Figure 23-250 shows the primary stages of link Dword data processing.

Figure 23-250. Simplified Schema of Link Dword Processing



23.12.4.2.1 SATA 8b/10b Parallel Encoding/Decoding

The input to the link coder logic is a parallel (unencoded) data byte and an associated control variable: Z with two possible values (K, D). The Z value signifies the byte to be encoded either as a control character (K value) or a data character (D value). The data byte (ABCDEFGH, where A matches the least significant bit [LSB]) is divided into two asymmetric portions: a 5-bit one ABCDE (range: 0 to 31) and a 3-bit one FGH (range: 0 to 7).

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The encoding process is performed in two stages. At the first stage, the 5-bit portion is converted to a 6-bit subblock (abcdei); at the second stage, the 3-bit portion is converted to a 4-bit subblock (fghj). An additional parameter called running disparity (rd) is taken into account during code calculation at both the character transmission and reception link sides. It introduces code correlation between adjacent bytes so that the current subblock code can depend on the code of the previous subblock and its associated rd output value. As a consequence, depending on the input rd parameter and the 8b/10b encoded value, the encoding/decoding lookup tables might have two different entries for the same byte.

The 10-bit parallel-encoded character is passed to the 10-bit data input of the SATA_PHY serializer component, which further transmits it serially in a LSB to most significant bit (MSB) order (abcdeifghj). The receiver link receives and decodes the sequence in the same LSB to MSB order (abcdeifghj). While SATA encoder takes the full range of a data byte (0–255) encoding values, it uses only two values to encode control characters. For more information on the 8b/10b encoding/decoding process, see the SATA standard specification.

23.12.4.2.2 SATA Stream Dword Components

The basic unit of SATA information is Dword – a double sized word (32 bits). An encoded Dword has a 40-bit length (4 x 10 bits), but, for simplicity, unencoded Dword lengths are considered here. Each Dword is serially transmitted or received by the SATA_PHY components in LSB character to MSB character order.

- Primitives

  The shortest meaningful component of the SATA stream is the primitive, which consists of a single Dword. Different types of primitive characters are inserted into the SATA stream to maintain synchronization between the host and the SATA peripheral device. Primitives convey real-time state information regarding the SATA communication channel itself. For example, the SATA link layer generates primitives to perform flow control, synchronize power management state transitions, frame enveloping, etc. The transport layer is not aware of the lower level primitive Dwords. They are subject to processing only to the link layer.

- Primitive handshakes

  In some cases, the transmitter of a primitive can require that the receiver send an acknowledge Dword to confirm primitive reception, which is a primitive handshake.

  The first byte of a primitive Dword is always a control character (or Z = K) with two possible encodings. The remaining three data bytes (Z = D) contain the function of the primitive. According to the SATA standard, the transmitter and the receiver are not required to match the number of primitives sent and received.

  Table 23-1410 briefly summarizes the primitives used by SATA.

Table 23-1410. SATA Primitives Summary

Primitive Name	Short Description
ALIGNp	Sent in pairs to PHY component to readjust its internal operations
CONTp	After CONTp insertion, previous primitives are repeated continuously until a different primitive is inserted
DMATp	terminates DMA data transmission
EOFp	End of frame
HOLDp	Inserted to hold data when transmitter doesn't have data ready to transmit
HOLDAp	Acknowledges a HOLDp primitive
PMACKp	Acknowledges a power management request
PMNAKp	A power management request denial
PMREQ_Pp	Power management request to PARTIAL state
PMREQ_Sp	Power management request to SLUMBER state
R_ERRp	Reception error occurred
R_IPp	Current node is receiving data
R_OKp	Reception without error
R_RDYp	Receiver is ready for reception

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Table 23-1410. SATA Primitives Summary (continued)

Primitive Name	Short Description
SOFp	Start of frame
SYNCp	Synchronization primitive
WTRMp	Transmitter inserts this primitive while waiting to get the reception status from receiver
XRDYp	Transmitter has data ready for transmission

- SATA data frames

  SATA data frames incorporate data FISs constructed at the transport layer along with some primitives (see Figure 23-251). The maximum number of Dwords between SOFp to EOFp does not exceed 2064 Dwords, including the FIS type and CRC fields described here.

- Frame FIS components

  The FIS contents of a frame incorporate the Dwords that correspond to SATA target data structures. FIS Dwords are output from transport layer TxFIFO to the transmitter link 8b/10b encoder during transmission. In the case of reception, the FIS content is obtained at transport layer RxFIFO after being successfully decoded by the receiver link logic. The commands and data embedded into Frame FISs are generated/interpreted at a higher transport level of the SATA controller and are user software-accessible in the host system memory.

- CRC

  The CRC is the last Dword in a frame, immediately following the last FIS Dword of the frame and preceding the EOFp primitive. The 32-bit CRC calculation is performed only on the FIS Dwords of the frame contents, so that frame-inserted primitives such as HOLDp, CONTp, etc., are not taken into account. The CRC is aligned on a Dword boundary. CRC code computation expects an input of an even number of words and should be Dword-multiple. If an FIS block contains an odd number of words, the last FIS word is padded with 0s to a full Dword before the CRC is calculated.

  – During transmission: The CRC Dword is calculated on original FIS contents, before scrambling and serial 8b/10b encoding are performed.

  – During reception: The CRC Dword is calculated on the 8b/10b decoded and subsequently descrambled 8-bit FIS Dword contents. It is then compared to the CRC received from the source to perform error check analysis.

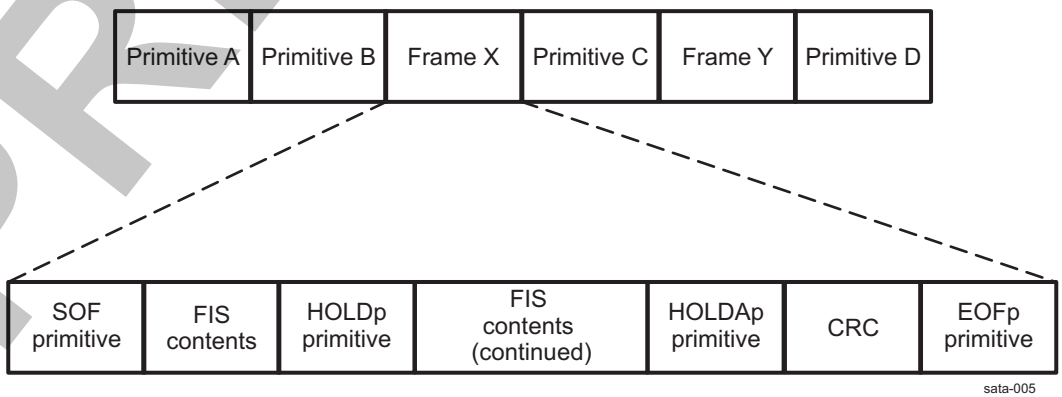
- Frame embedded primitives

  The beginning of a frame is marked with a SOFp primitive, and the end is marked with an EOFp primitive. Some primitives, such as HOLDp and HOLDAp acknowledge, can be inserted into frames between data FISs.

- SATA data stream

  As shown in Figure 23-251, the SATA data stream is composed of frames carrying the target data/command contents combined with various primitives generated to maintain consistency of transfers over the SATA interface.

Figure 23-251. SATA Data Stream Components



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23.12.4.2.3 Scrambling/Descrambling Processing

The contents of a frame are scrambled before being passed to the link 8b/10b encoder. Scrambling is performed on Dword quantities by XORing the data to be transmitted with the output of a linear feedback shift register (LFSR). All data words between the SOFp and EOFp are scrambled, including the CRC. Figure 23-250 shows the basic flow.

The SATA controller (as defined by the SATA standard) performs scrambling/descrambling processing for EMI reduction purposes. Two scramblers are instantiated within the SATA controller: The first, the data payload scrambler, scrambles FIS data payload contents (including the calculated CRC Dword); the second, the repeated primitive suppression scrambler, scrambles only the repeated primitive stream contents.

The scrambling runs as follows: A certain data payload Dword located between SOFp and EOFp is XORed with the data payload scrambler output. The resulting scrambled Dword is submitted to the 8b/10b encoder for transmission.

On reception, the Dword is decoded using a 10b/8b decoder, the scrambler output is XORed with the resulting Dword, and the resulting Dword is presented to the link layer. It is then used for CRC computation. The CRC Dword is scrambled in the same way as data payload characters.

For details on the scrambling/descrambling feature, see the *SATA Standard Specification* (rev.2.6).

23.12.4.3 Resets

23.12.4.3.1 Hardware Reset

The module is reinitialized in hardware (for more information about hardware reset, see Section 23.12.3, *SATA Controller Integration*).

For more information on the PRCM.L3INIT_RST hardware reset signal, refer to Section 3.5.4, *Reset Domains*, in Chapter 3, *Power, Reset, and Clock Management*.

This reset normally occurs on device power up or during a system bus failure. All components of the SATA AHCI core are initialized, including the HBA port and generic registers. The bus interface unit (BIU) and SATA AHCI core wrapper components are also impacted.

23.12.4.3.2 Software Initiated Resets

The SATA controller supports three levels of software reset, each of which has different impact over the SATA HBA hardware components and AHCI interface registers:

- Software reset (least intrusive)
- Port reset
- HBA reset (most intrusive)

NOTE: It is recommended that user software always starts with the least intrusive reset approach. Software chooses the next most intrusive reset only if the less intrusive reset does not succeed in clearing the condition.

23.12.4.3.2.1 Software Reset

Software reset impacts only the attached to the HBA port SATA peripheral device, without affecting the established communication between physical layers or HBA engine.

To issue a software reset, the user must prepare two H2D register FISs into the emptied command list of the port. The first FIS must have bits SRST = 0b1 and C = 0b0. The first FIS corresponding command header bits C and R are set as follows: C = 0b1 and R = 0b1.The second FIS has bits SRST = 0b0 and C = 0b0. The second FIS corresponding command header bits C and R are set as follows: C = 0b0 and R = 0b0.

However, steps must be taken before issuing the software reset to the peripheral device attached to the port. For details on software reset, see the AHCI specification .

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23.12.4.3.2.2 Port Reset

The port reset (also known as COMRESET) must be applied when the HBA port does not function properly after a software reset is issued to the port. The effect is that the SATA HBA port is reinitialized and communication between the phy layers of both the SATA host and the SATA target device is reestablished.

To trigger a COMRESET sequence on the SATA interface, user software must write 0x1 to the SATA_PxSCTL[3:0]DET bit field. The host receives a COMINIT signal sequence, indicating that the peripheral device has successfully reestablished communication. For more information on port reset, see the AHCI specification (revision 1.1).

NOTE: The port reset (COMRESET) method is the preferred AHCI mechanism for error recovery and should be used instead of the software reset.

23.12.4.3.2.3 HBA Reset

Software can globally reset the SATA controller, if a port reset does not clear the conditions successfully. On HBA reset, all SATA AHCI core interface registers are reset, **excluding those from the hardware initialization domain** - the SATA_PxCLB, SATA_PxCLBU, SATA_PxFB and SATA_PxFBU registers. All state machines that relate to data transfers and queuing return to IDLE state, and the port is reinitialized by sending COMRESET. The global reset is triggered when user software sets the SATA_GHC[0]HR = 0b1 bit. The HBA indicates that global reset is finished, deasserting the SATA_GHC[0]HR bit to 0b0 in hardware. Hence, user software must poll the HR bit to detect this condition. For more information, see the mentioned AHCI standard specification.

23.12.4.4 Power Management

The device SATA host controller subsystem power management can be identified at the following levels:

- SATA controller low power-management features (defined also in the SATA standard specification, revision 2.6)
- Idle/standby power-management protocol established between SATA controller and the device PRCM through a SATA AHCI core wrapper interface (signified as SATAMAC_wrapper instance inside the Section 23.12.6.1, *SATA Controller Instance Summary*).

This section describes the relationships that exist between both levels of SATA Controller power management.

23.12.4.4.1 SATA Specific Power Management

The SATA controller core supports both PARTIAL and SLUMBER low-power states, as described in the SATA standard specification (revision 2.6). These modes allow power savings by powering down part of SATA_PHY and gating off the clocks to the link layer. The port power control module is used to enter and exit these modes, which can have the normal functional clocks gated off.

23.12.4.4.1.1 PARTIAL Power Mode

In the PARTIAL power state, the SATA_PHY component transmits electrical IDLE to the device and the receiver is left on to receive OOB signals. This mode can also be used to support near-end analog loopback, if a device is attached.

23.12.4.4.1.2 Slumber Power Mode

In the SLUMBER power state, the transmitter is completely turned off. This allows for greater power savings but near-end analog loopback cannot be performed and there is a longer latency to exit the mode.

23.12.4.4.1.3 Software Control over Low Power States

The user has manual control over low power states through the SATA_PxCMD [31:28]ICC register bit field. This works if the link is in IDLE state; otherwise, writes to this field are ignored.

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23.12.4.4.1.4 Aggressive Power Management

Low power modes can be initiated by software when there are no pending transactions, but the SATA AHCI core also supports aggressive power management. In this mode, the subsystem automatically initiates the PARTIAL or SLUMBER state when there are no inflight commands. This is useful for power savings, but the price is increased latency if a low-power mode is entered and a transfer request is made. Software enables aggressive link-layer power management by setting the SATA_PxCMD[26]ALPE bit to 0x1. The link aggressive power management state (PARTIAL or SLUMBER) is selected using the SATA_PxCMD[27]ASP bit.

23.12.4.4.2 Idle/Standby Management Protocol

The idle/standby handshake protocol is implemented between the PRCM and SATA controller, with mode settings located in the SATAMAC_wrapper register (SATA_SYSCONFIG).

- The standard idle request/acknowledge handshake is associated with the L4_CFG slave port. The default idle mode is smart-idle, as indicated by the power-on reset (POR) value: SATA_SYSCONFIG[3:2]IDLEMODE = 0x2.

NOTE: No other mode is expected to be required in normal operation: no-idle and force-idle are used for debugging only. Because the module is not capable of asynchronous wakeup, the smart-idle/wakeup (IDLEMODE = 0x3) is strictly equivalent to smart-idle.

- The standby/wait handshake is associated with the L3_MAIN master port. Software is responsible to keep the DMA operations and the standby status in sync.

The default standby mode is smart-standby, as indicated by the POR value: SATA_SYSCONFIG[5:4]STANDBYMODE = 0x2. However, the SATA controller hardware does not provide any indication about DMA activity that could be used to drive the standby dynamically (that is, the smart mode): Smart-standby is therefore strictly equivalent to the force-standby mode (that is, the module remains in or goes to permanent standby).

The standby control procedures are therefore software-driven.

To exit standby:

1. Change the standby mode to no-standby by setting SATA_SYSCONFIG[5:4] = 0x1.
2. Optional: Confirm the SATA controller standby status through the PRCM. For more information, see Section 3.6.4.5, *Clock Domain Module Attributes*, in Chapter 3, *Power, Reset, and Clock Management*.
3. Only then, enable the controller DMA (AHCI list processor). For more information, see the AHCI specification.

To enter standby:

1. Disable the controller DMA (AHCI list processor). For more information, see the AHCI specification.
2. Ensure all pending transactions have completed. For more information, see the AHCI specification.
3. Change the standby mode to smart-standby (or force-standby) by setting SATA_SYSCONFIG[5:4] = 0x2.

CAUTION

The software is responsible to keep the DMA operations and the standby mode status in sync.

NOTE: Because the standby exit is software driven, it is by definition synchronous: the asynchronous wakeup is never activated, which means that the smart-standby and smart-standby/wakeup are equivalent (as well as force-standby).

For more information on the SATA Controller Idle/Standby Management Protocol with the device PRCM , see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

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23.12.4.4.3 Clock Gating Synchronization

The bus clock can also be gated off in either the PARTIAL or SLUMBER state, if the software guarantees there is nothing in flight, the clock can be stopped and started without glitches, and the clock can be restarted quickly when activity is initiated from the device side.

The following steps outline the procedure to stop the clock:

1. Put the link in a low power state (either PARTIAL or SLUMBER)
   - SATA MAC link layer can enter low power either manually see Section 23.12.4.4.1.3, *Software Control over Low Power States*) or automatically (see Section 23.12.4.4.1.4, *Aggressive Power Management*)
   - If there is no device attached (making it impossible to enter a low power state), the SATA_SYSCONFIG[16] OVERRIDE0 override bit can be set to 0b1 to stop the interface/functional clock (SATA_FICLK) and save power.
2. Initiate the clock stopping procedure.

CAUTION

If a SATA drive attached to the SATA HBA port has not entered a low power state (PARTIAL or SLUMBER), the user must not set the SATA_SYSCONFIG[16]OVERRIDE0 bit; otherwise, the link layer can be ruined, resulting in indeterminate SATA controller behavior.

Table 23-1411. Local Power-Management Features

Feature	Registers	Description
Slave idle modes	SATA_SYSCONFIG [3:2]IDLEMODE bit field	The available modes are: Force-idle, no-idle, and smart-idle wakeup disabled modes are available.
Master standby modes	SATA_SYSCONFIG [5:4]STANDBYMODE bit field	The available modes are: Force-standby, no-standby, smart-standby wakeup disabled
Clock-gate overriding mode	SATA_SYSCONFIG [16]OVERRIDE0 bit field	Clock stopping override function. Should not be applied when attached to port SATA peripheral device has not entered a Low-power mode.

For more information on the L3INIT_L3_GICLK functional clock gating in the device PRCM , refer to Section 3.1.1.1.4, *Clock Domain-Level Clock Management*, in the chapter, *Power, Reset and Clock Management*.

23.12.4.5 Interrupt Requests

This section describes all of the conditions that can generate an interrupt. Each condition is subject to the masking capabilities described in Section 23.12.4.5.4, *Interrupt Condition Control*.

23.12.4.5.1 Interrupt Generation

Both level and pulse interrupts are available. Exercise care when using the pulse interrupt. Because of the synchronization and interrupt aggregation from the internal core, clearing one interrupt as another interrupt occurs can prevent a new pulse from being generated. A new pulse is generated only if the first interrupt is completely cleared (that is, the level interrupt goes away) before the new interrupt event occurs. Thus, an interrupt can occur after the register write is issued to clear the first interrupt but before the interrupt is fully cleared. In this case, a new pulse is not issued and the level interrupt remains asserted. After issuing the write to clear an interrupt, software must read the interrupt status registers to ensure that a new interrupt has not occurred.

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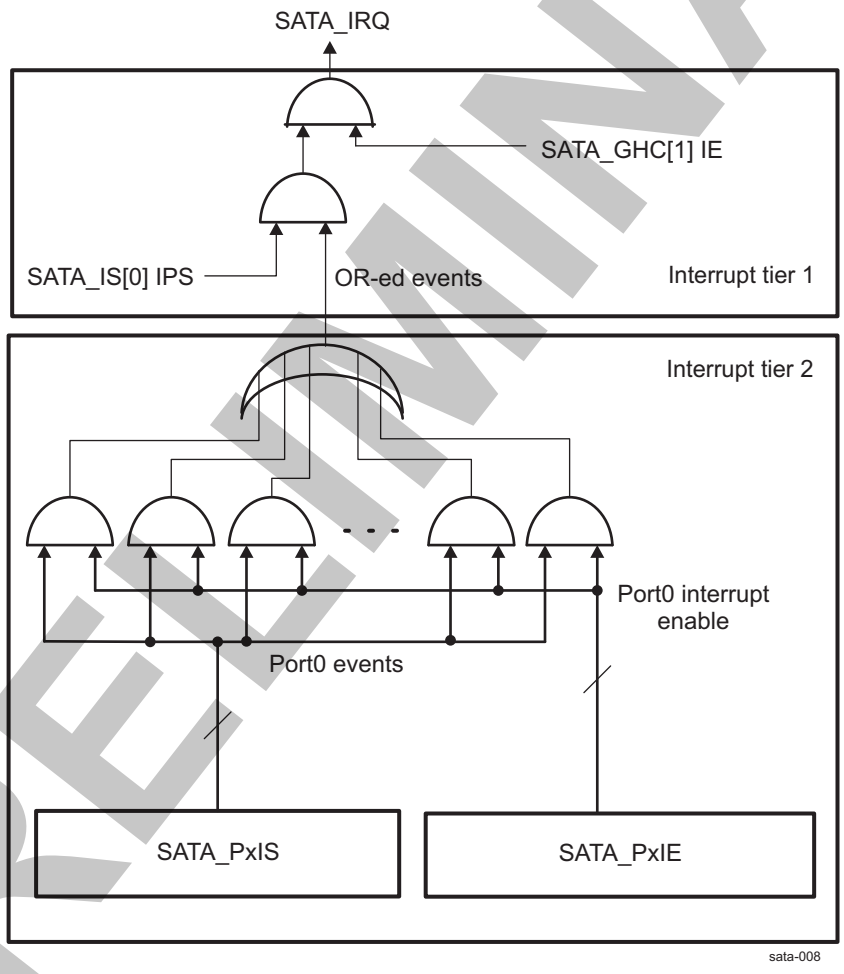
23.12.4.5.2 Levels of Interrupt Control

The AHCI directs that interrupts be indicated in a two-tier structure and thus associated with different HBA ports. Considering the device SATA HBA single-port implementation for the first tier, only the SATA_IS[0] IPS bit should be considered. It indicates if the only port available to the user (HBA port 0) has pending interrupts.

For the second tier, the SATA_PxIS register (where x = 0) indicates which specific interrupt condition(s) occurs to trigger an interrupt on port 0. In most cases, software writes 0x1 (Write One to Clear) to clear these bits, and then writes 0x1 to the SATA_IS [0]IPS bit to clear the interrupt. However, some interrupts in the SATA_PxIS register have alternate methods of being cleared (for details, see Section 23.12.6.2.2, *DWC_ahsata Register Description*). Section 23.12.4.5.3, *Interrupt Events Description*, describes all interrupt generating conditions.

Figure 23-252 shows the SATA controller two-tier interrupt propagation structure. Besides SATA_IS[0], which gates all interrupts at the port 0 level, the tier 1 interrupt is globally gated by the SATA_GHC[1] IE bit.

Figure 23-252. SATA Controller Interrupt Propagation Schema



NOTE: Regardless of the device SATA controller single HBA port implementation, user software must read/write the tier 1 SATA_IS[0] IPS register bit to process interrupts.

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23.12.4.5.3 Interrupt Events Description

This section describes the different events that are reflected in the SATA_PxIS register and that cause SATA_IRQ interrupt generation, if enabled, in the SATA_PxIE register. For more information regarding SATA_IRQ handling at the MPU subsystem interrupt controller - INTC_MPU level, see Section 17.3.2, *Interrupt Requests to INTC_MPU* in Chapter 17, *Interrupt Controllers*.

23.12.4.5.3.1 Task File Error Status

This event is registered whenever the SATA_PxTFD[7:0] STS bit field is updated by the device and the error bit SATA_PxTFD[0]STS_ERR is set. SATA_PxTFD[7:0] STS is updated when a new register FIS, PIO setup FIS, or set device bits FIS is received from the device.

23.12.4.5.3.2 Host Bus Fatal Error

This event is registered whenever an error is received by the SATA controller internal DMA master port from the configuration slave port.

23.12.4.5.3.3 Interface Fatal Error Status

This event is registered if an error is generated on the interface. The following conditions can cause this:

- SYNC escape during an H2D register or data FIS transmission
- One of the following errors during a data FIS transfer:
  - Protocol (SATA_PSERR[10] ERR_P)
  - CRC (SATA_PSERR[21] DIAG_C)
  - Handshake (SATA_PSERR[22] DIAG_H)
  - SATA_PHY not ready (SATA_PSERR[9] ERR_C)
- Unknown FIS received with a good CRC, but length greater than 64 bytes
- Physical region descriptor (PRD) table byte count of 0

NOTE: This is a fatal error in which the DMA is in an error state until software clears the SATA_PxCMD[0] ST bit or resets the interface with a port or global reset. For more information about software-initiated resets, see Section 23.12.4.3.2, *Software Initiated Resets*.

23.12.4.5.3.4 Interface Non-Fatal Error Status

This event is registered on the following error conditions:

- One or more of the following errors are registered during a non-data FIS transfer:
  - Protocol (SATA_PSERR[10] ERR_P)
  - CRC (SATA_PSERR[21] DIAG_C)
  - Handshake (SATA_PSERR[22] DIAG_H)
  - SATA_PHY not ready (SATA_PSERR[9] ERR_C)
- Command list underflow during a read operation when software builds a command table that has more total bytes than the transaction given to the device

NOTE: The conditions previously described are non-fatal and the SATA host controller continues to operate normally.

23.12.4.5.3.5 Overflow Status

This event is registered if command list overflow is detected during read or write when software builds a command table with fewer total bytes than the transaction given to the device.

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NOTE: This is a fatal error in which the DMA is in an error state until software clears the SATA_PxCMD[0] ST bit or resets the interface with a port or global reset. For more information about software-initiated resets, see Section 23.12.4.3.2, *Software Initiated Resets*.

23.12.4.5.3.6 PHYReady Change Status

This event is registered when the status of PHYReady changes. Its corresponding status bit (SATA_PxIS[22] PRCS) reflects the SATA_PxSERR[16]DIAG_N bit.

23.12.4.5.3.7 Port Connect Change Status

This event is registered when there was a change in the current connect status as reflected by the SATA_PxSERR[26]DIAG_X bit.

23.12.4.5.3.8 Descriptor Processed

This event is registered when a transaction completes. Its corresponding flag (SATA_PxIS[5] DPS) is set whenever a PRD with the I bit set transfers all of its data.

NOTE: The PRD interrupt is an opportunistic interrupt and should not be used to definitely indicate the end of a transfer. Two PRD interrupts can happen close in time so that the second interrupt is missed while the first PRD interrupt is being cleared.

When a PRD entry is exhausted, the HBA can be directed to generate an interrupt through the I bit in the PRD entry (although a PRD is not considered exhausted until all data FISs that transfer data pointed to by that PRD entry is complete). For example, if the data FIS is 8 KiB, and this is covered by three PRD entries, the data is not considered valid at the end of the first or second PRD because the CRC has not been checked, even though the data has been copied to memory or to the device. Therefore, if the I bit is set in the PRD entry, the HBA must hold onto it internally and not set PxIS.DPS until the data FIS is complete and the CRC is correct. Once correct, PxIS.DPS can be set and, if PxIE.DPE and GHC.IE are set, the HBA generates an interrupt.

Conversely, if the PRD entry is 16 KiB and two 8 KiB Data FISS are used to transfer all of the data pointed to by the PRD entry, the PRD interrupt associated with that PRD entry is not signaled until after the second data FIS transfer completes successfully.

23.12.4.5.3.9 Unknown FIS Interrupt

This status event indicates that an unknown FIS is received and copied into system memory.

23.12.4.5.3.10 Set Device Bits Interrupt

This status event indicates that a Set Device Bits FIS is received with the I bit set and copied to system memory.

23.12.4.5.3.11 DMA Setup FIS Interrupt

This status event indicates that a DMA Setup FIS is received with the I bit set and copied into system memory.

23.12.4.5.3.12 PIO Setup FIS Interrupt

This status event indicates that a PIO Setup FIS with the I bit set is copied into system memory and the data related to that FIS is transferred.

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23.12.4.5.3.13 Device to Host Register FIS Interrupt

This status event indicates that a D2H Register FIS is received with the I bit set and copied to system memory.

23.12.4.5.4 Interrupt Condition Control

There are several ways for software to control the conditions causing a non - command completion coalescing **(non-CCC)** SATA_IRQ interrupt assertion. The SATA_GHC[1] IE register bit serves as a global mask. If it is 0x0, all interrupts are masked. If it is 0x1, interrupts not masked by the SATA_IS (all interrupts for port 0) and SATA_PxIE registers can trigger an interrupt. The SATA_PxIE register matches the SATA_PxIS register bit for bit. If the corresponding bit in the SATA_PxIE register is set to 0x1, the interrupt is unmasked. If the corresponding is 0x0, the interrupt is masked off.

Table 23-1412 summarizes the SATA controller interrupt status bits and their corresponding interrupt enable bits at the second tier of the SATA controller interrupt generation schema.

Table 23-1412. Interrupt Events Summary

Event Status Flag	Interrupt Event Mask	Mapped to Interrupt Output	Brief Interrupt Event Description
SATA_PxIS [30]TFES	SATA_PxIE [30]TFEE	SATA_IRQ	Task File Error
SATA_PxIS [29]HBFS	SATA_PxIE [29]HBFE		Host Bus Fatal Error
SATA_PxIS [27]IFS	SATA_PxIE [27]IFE		Interface Fatal Error
SATA_PxIS [26]INFS	SATA_PxIE [26]INFE		Interface Non-Fatal Error
SATA_PxIS [24]OFS	SATA_PxIE [24]OFE		Overflow
SATA_PxIS [22]PRCS	SATA_PxIE [22]PRCE		Phy Ready Change
SATA_PxIS [6]PCS	SATA_PxIE [6]PCE		Port Connect Change
SATA_PxIS [5]DPS	SATA_PxIE [5]DPE		Descriptor Processed
SATA_PxIS [4]UFS	SATA_PxIE [4]UFE		Unknown FIS Received
SATA_PxIS [3]SDBS	SATA_PxIE [3]SDBE		Set Device Bits FIS Received
SATA_PxIS [2]DSS	SATA_PxIE [2]DSE		DMA Setup FIS Received
SATA_PxIS [1]PSS	SATA_PxIE [1]PSE		PIO Setup FIS Received
SATA_PxIS[0]DHRS	SATA_PxIE [0]DHRE		Device to Host Register FIS Received

NOTE: To ensure normal generation of the standard (single-event driven, non-CCC) interrupts described in Table 23-1412, the user must ensure that the CCC feature is disabled (that is, the SATA_CCC_CTL[0] EN bit is set to 0x0).

23.12.4.5.5 Command Completion Coalescing Interrupts

The SATA controller supports CCC, which can be thought of as interrupt pacing. Instead of being generated for every command completed, an interrupt can be triggered based on a certain number of commands completed and/or a timer time-out. This significantly reduces the load on the CPU by not allowing software to receive an interrupt every time a command is processed. Software can thus queue many commands or wait for many received FISes and process them as a batch. All CCC functions are controlled by the SATA_CCC_CTL, SATA_CCC_PORTS, and SATA_TIMER1MS registers. Setting SATA_CCC_PORTS[0]PRT = 0x1 makes the only available SATA controller HBA port 0 - CCC-aware. The SATA_CCC_CTL register can be used to program CCC logic to trigger an interrupt whenever a certain number of commands are complete and/or a timeout value (as specified by the TV field of SATA_CCC_CTL and SATA_TIMER1MS registers) occurs. For specific programming instructions, see the SATA_CCC_CTL description.

23.12.4.5.5.1 CCC Interrupt Based on Expired Timeout Value

To trigger a CCC interrupt on a port after an elapsed timer value, the following programming sequence must be implemented by user software:

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1. Software disables the CCC feature, clearing SATA_CCC_CTL[0] EN to 0b0.
2. Software sets SATA_CCC_PORTS[0] PRT = 0x1 to make HBA port 0 CCC-aware.
3. Software sets SATA_CCC_CTL[15:8] CC = 0x0, which provides that the expired timeout trigger condition is selected.
4. Software defines the 1-ms time-based unit by loading an appropriate number of interface/functional clock cycles into the 20-bit SATA_TIMER1MS[19:0] TIMV bit field. For example, its reset value of 0x186A0 (100 000 x SATA_FICLK cycles) provides that a 1-ms timeout base will be generated if SATA_FICLK = 100 MHz.
5. Software chooses the timeout value as the number of 1-ms intervals through the 16-bit SATA_CCC_CTL[31:16]TV bit field.
6. Software enables the CCC-interrupt feature, asserting SATA_CCC_CTL[0] EN bit to 0b1.

Assertion of bit SATA_CCC_CTL[0] EN to 0x1 is required to start the 1MS TIMER after the above described configuration steps are completed.

NOTE: On CCC event configuration, the CCC feature should be disabled (that is, SATA_CCC_CTL[0] EN should be kept at 0b0).

NOTE: Due to the single SATA controller HBA port integration, the source of the CCC interrupt, if enabled, is always HBA port 0. On a CCC interrupt, the SATA_CCC_CTL[7:3] INT read-only bit changes to 0x0 (its reset value is 0x1) . As a consequence, the STA_IS[0] IPS bit is set to 0x1.

23.12.4.5.5.2 CCC Interrupt Based on Completion Count

If the desired method to receive an interrupt is based on the completion of a certain number of commands, the following settings must be performed:

1. Software disables the CCC feature, clearing SATA_CCC_CTL[0] EN to 0b0.
2. Software sets SATA_CCC_PORTS[0] PRT = 0x1 to make HBA port 0 CCC-aware.
3. Software sets SATA_CCC_CTL[15:8] CC! = 0x0 to the desired number (1–255) of commands to be completed. The CC! = 0x0 provides that the count completion condition is selected.
4. Software enables the CCC-interrupt feature, asserting the SATA_CCC_CTL[0] EN bit to 0b1.

NOTE: On CCC event configuration , the CCC feature should be disabled (that is, SATA_CCC_CTL[0] EN should be kept at 0b0).

NOTE: Due to the single SATA controller HBA port integration, the source of the CCC interrupt, if enabled, is always HBA port 0. On a CCC interrupt, the SATA_CCC_CTL [7:3]INT read-only bit changes to 0x0 (its reset value is 0x1) . As a consequence, the STA_IS[0] IPS bit is set to 0x1.

23.12.4.6 System Memory FIS Descriptors

The SATA AHCI mode supports a command list of from 1 up to 32 entries (command slots) assigned to HBA port 0, which should be allocated and built into host system memory by user software. After receiving command/data messages from the attached port 0 SATA mass-storage drive, the HBA extracts the FIS Dwords, sorts them out, and stores them into different areas of RX FIS-allocated host system memory.

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23.12.4.6.1 Command List Structure Basics

Each command list entry has an associated command header (CH) that takes 32 bytes in host system memory, from which only the first 4 Dwords (16 bytes) are used. The CH contains different fields that detail the direction of transfer (H2D or D2H), type of command (ATA/ATAPI), reset behavior, PM ID, byte count and byte length of the PRD table, etc.

A command list slot CH specifies the base address of the underlying command table and information about the associated command FIS length. The command table in system memory has three main areas:

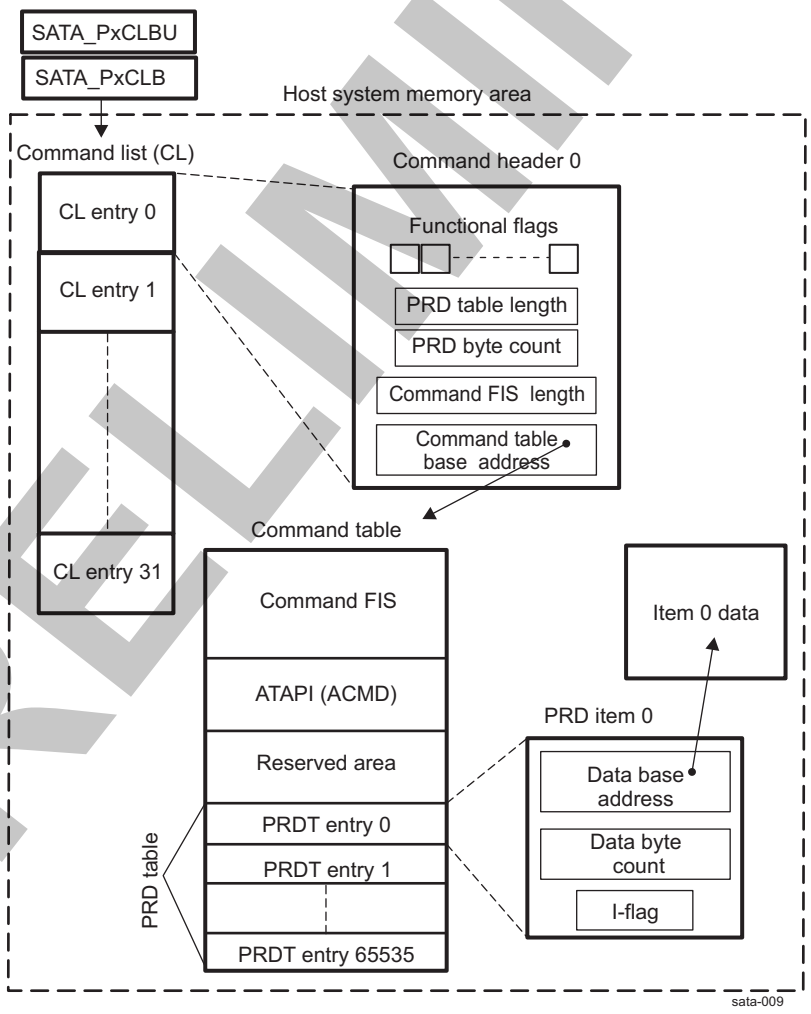
- A 64-byte command FIS area in which the user loads the command-associated FIS contents
- An ATAPI area in which a 12- or 16-byte ATAPI command is loaded, if specified in the CH (through bit A)
- A PRD table area that allows up to 65535 data descriptor entries

An entry of a PRD table (that is, a scatter/gather list item) specifies descriptor parameters of a data block transfer handled by the HBA port DMA.

Figure 23-253 shows the interrelations between the FIS-related structures that user software must allocate and build into the host system memory.

For details on command and data structures in host system memory, see the AHCI and SATA standard specifications.

Figure 23-253. Command List Descriptor Structures



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After allocating the necessary portions for the CL, command slots underlying data descriptors, and received FISs into host system memory, the base addresses of these memory locations must be provided by user software to the HBA through the hardware init domain registers: SATA_PxCLB (command list base address - lower bits), SATA_PxCLBU (command list base address-upper bits), SATA_PxFB (received FISs system memory area base address-lower bits) and SATA_PxFBU (received FISs system memory area base address-upper bits) . Thus, the command and data DMA engines can access the transfer context programming structures.

NOTE: SATA_PxCLBU / SATA_PxFBU registers store the upper half of the native 64-bit AHCI addresses. Because only 36-lower bits of the AHCI 64-bit address bus are integrated in the device, actually only the 4-lower bits within SATA_PxCLBU / SATA_PxFBU are meaningful. **The remaining 28-bits must be always written to '0'-s in the descriptors (SATA_PxCLBU[31:4]=0x0 / SATA_PxFBU[31:4]=0x0) .**
Default value for the SATA_PxCLBU / SATA_PxFBU registers is 0x0, so that a 32-bit SW driver which never accesses them works seamlessly, by accessing only the 32-bit (lower half) addresses which reside in the SATA_PxCLB / SATA_PxFB registers.

23.12.4.6.2 Supported Types of Commands

The following types commands are supported:

- Standard serial ATA nonqueued commands set.

  As opposed to NCQ, these commands are serviced, acknowledged one by one after a successful completion. The nonqueued SATA CL entries can take advantage of the PRD prefetching option indicated by the P flag in the corresponding CH (for more information, see the SATA specification). The ATA legacy commands are not supported by the SATA AHCI core.
- ATAPI commands
- ATAPI commands are supported by the SATA HBA engine. A request for an ATAPI command service is indicated by setting CH bit A to 0b1. The ATAPI command that the user builds into the ATAPI area of the command table can be 12 or 16 bytes in length and is indicated by the PIO Setup FIS sent by the SATA peripheral storage device requesting the ATAPI command. In addition, the SATA controller supports ATAPI active-LED generation (See Section 23.12.4.9, *Activity LED Generation Functionality*).

NCQ-commands

NCQ-commands are supported by the SATA controller HBA engine, the execution of which can be greatly facilitated by the CCC interrupt feature (for more information, see Section 23.12.4.5.5, *Command Completion Coalescing Interrupts*). As described in Section 23.12.1.1.2, *Native Command Queuing*, the NCQ commands have FPDMA queued command protocol mechanism, which implies that they are treated in a different way then standard SATA commands. The AHCI interface register set include specific registers, such as SATA_PxSACT, etc., to make the HBA aware of the outstanding NCQ slots in a command list. As opposed to standard nonqueued commands, NCQ commands are acknowledged before their actual completion, which accelerates the CL servicing for NCQ slots. The queue tag of the command requested by the SATA peripheral device is indicated to the HBA port by the TAG field in a DMA Setup FIS that an attached SATA peripheral device sends to the SATA controller host . The HBA then uses the tag value to index the NCQ commands updated by user software in the command list. The NCQ command descriptors are not allowed to use the prefetching option in CH because their order of execution is determined by the SATA target device.

23.12.4.6.3 Received FIS Structures

After stream decoding and primitive removal by the link layer, the validated FIS Dwords are extracted from the RxFIFO buffer by the transport layer DMA, and the original SATA storage drive FIS structures are recovered to a dedicated host system memory space. The DMA stores the received FISs into different memory areas based on FIS type. The unknown FIS reception is legal to HBA, as long as the length of the unknown FIS does not overrun the 64-byte size limit of the FIS descriptors. For details on received FISs memory area organization, see the AHCI and SATA standard specifications.

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23.12.4.6.4 FIS Descriptors Summary

The FISs that encapsulate SATA target commands and data contents can be divided into:

- FISs transmitted from the host to an attached SATA peripheral device (H2D FISs)
- FISs sent by an attached SATA peripheral device to the host (D2H FISS)

The H2D FISs are constructed by user software into system memory. he H2D FIS types are:

- H2D Register FIS
- H2D DMA Setup FIS
- H2D Data FIS

The D2H FISs are constructed by the attached SATA peripheral device transport layer. The D2H FIS types are as follows:

- D2H Register FIS
- D2H DMA Setup FIS
- PIO Setup FIS
- DMA Activate FIS
- Set Device Bits FIS
- D2H Data FIS

For details on different type of FIS contents, see the SATA standard specification (revision 2.6).

23.12.4.7 Transport Layer FIS-Based Interactions

23.12.4.7.1 Software Processing of the Port Command List

After user software instantiates the CL structures in host system memory, it must maintain them appropriately. The command list is advanced when the BSY, DRQ, and ERR bits of a serial ATA device task file are cleared, which is communicated through a D2H register FIS to HBA port. The HBA port 0 hardware clears the corresponding to the i-th completed command: SATA_PxCI [i] CI (SATA_PxCI [TAG] CI for NCQ) bit to notify user software that the next command FIS can be advanced into the CL. The software then builds the command slot components: CH fields, command table, and associated PRD data descriptors in system memory. Software asserts the SATA_PxCI[i+1] CI (or SATA_PxCI[TAG] CI bit for an NCQ indicated command) to activate the prepared CL command, which is possible only when SATA_PxCMD[0] ST = 0x1. The nonqueued commands in the CL are processed in ascending order of slots (linear processing). The SATA_PxCMD [12:8]CCS read-only field indicates the CL index of the command currently being issued by the HBA port.

The processing of NCQ command slots invokes additional register update/check steps. Before setting the SATA_PxCI[TAG] CI bit to 0b1 and posting an active NCQ command to the SATA HBA port, software must indicate an NCQ outstanding command at the position defined by the SATA peripheral device queue TAG by setting SATA_PxSACT[TAG] DS = 0x1. After the queued command is posted, the peripheral SATA device sends a Set Device Bits FIS to the HBA port to clear the SATA_PxSACT bits corresponding to the successfully completed NCQ commands.

Command-list processing is initially triggered by software setting SATA_PxCMD[0] ST = 0x1, which requires certain conditions to be satisfied.

NOTE: There are some restrictions to setting SATA_PxCMD[0] ST to 0x1. For more information, see the AHCI specification (revision 1.1).

The SATA controller is capable of command list override (CLO) operation. CLO is activated by setting SATA_PxCMD[3] CLO = 0b1, which is expected only when SATA_PxCMD[0] ST = 0x0 (that is, the command list is not processed by the HBA) to avoid HBA-indeterminate behavior. As a consequence of a CLO operation, the SATA_PxTFD register STS_DRQ and STS_BSY flags are cleared. For example, CLO is necessary when the DRQ and BSY flags cannot be cleared by HBA before issuing a software reset (because of some hang condition). For more information on CLO behavior, see the AHCI standard specification.

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23.12.4.7.2 Handling the Received FIS Descriptors

The HBA DMA facilitates the reception of the D2H FISs into host system memory. The reception is enabled by the user setting SATA_PxCMD[4] FRE to 0b1. The software is allowed to change the SATA_PxFB / SATA_PxFBU contents and thus move the FIS reception area to different system memory locations, if SATA_PxCMD[14] FR is cleared, which occurs after software writes SATA_PxCMD[4] FRE = 0b0. In this case, further FIS reception is blocked when the internal RxFIFO becomes full. Before setting SATA_PxCMD[4] FRE to 0x1, the user software must ensure that a valid address is programmed into the SATA_PxFB / SATA_PxFBU registers.

NOTE: The HBA port stores the unknown FISs (up to 64 bytes) in system memory but does not have a specified behavior to indicate an error condition on reception. The unknown FISs must be handled specifically by user software.

23.12.4.8 DMA Port Configuration

The SATA controller handles all data operations on its port with an internal DMA integrated in SATA AHCI core.

The SATA controller DMA transfers all information between system memory and the attached SATA peripheral device, as well as configuration and status FISs. The transmit and receive DMA data paths are independently programmable.

The burst size in both directions is fixed to 16 Dwords. The DMA issues transactions of this size or smaller (in Dword increments), depending on programmed transaction size.

NOTE: If the programmed transaction size is lower than 16-Dwords (burst size), then the DMA maxes out at transaction size.

The user can also separately program the transaction size for receive and transmit channels by setting the SATA_PxDMACR[7:4] RXTS and SATA_PxDMACR[3:0] TXTS bit fields. The transaction size is the minimum amount of data on which the DMA works. For example, if a FIS comes from the device to the host, the DMA does not begin transferring data into system memory until there is at least SATA_PxDMACR[7:4] RXTS number of Dwords in the receive FIFO. During transmit, the DMA reads data from system memory in SATA_PxDMACR[3:0] TXTS Dword increments to put into the transmit FIFO. Transactions can be broken up into multiple bursts of 16 Dword - size, crossing of a 1-KiB boundary (boundary between 1-KiB address blocks in memory), or end-of-frame. RXFIFO and TXFIFO transaction sizes are limited to maximum half the size of the integrated RXFIFO and TXFIFO buffers. For more information on maximum transaction sizes and RXFIFO/TXFIFO depths, see the SATA_PxDMACR and SATA_PPARAMR descriptions.

23.12.4.9 Activity LED Generation Functionality

The HBA port drives the device-level sata_actled signal that is active on the following conditions (see also Table 23-1406):

- If (SATA_PxCI [31:0]! = 0x0 or SATA_PxSACT[31:0]! = 0x0) and SATA_PxCMD[24] ATAPI = 0b0 (for active nonATAPI commands indication)
- If (SATA_PxCI [31:0]! = 0x0 or SATA_PxSACT[31:0]! = 0x0) and SATA_PxCMD[24] ATAPI = 0b1 and SATA_PxCMD[25] DLAE = 0b1 (for active ATAPI commands indication)

When SATA_PxCI and SATA_PxSACT are cleared to 0x0, the LED on the sata_actled signal-associated pad is driven off.

23.12.4.10 Supported Types of SATA Transfers

SATA controller AHCI mode defines two types of transfers between the host system memory and a SATA peripheral device: DMA and PIO data transfers. Whether the transaction is of a DMA type or PIO type, the HBA fetches and stores data to memory, offloading the CPU. No register is implemented for direct user access to the data port.

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PIO transfers specified by PIO Setup FISs are strongly discouraged because of their limited support of error indication. PIO commands use is limited to only few cases in which commands support only PIO mechanism, such as execution of the IDENTIFY DEVICE command and ATAPI command transfers in which the PACKET command is invoked. The SATA controller AHCI mechanism allows multiple DRQ blocks of data per PIO command.

23.12.4.10.1 Supported Higher Level Protocols

The following DMA, PIO, FPDMA-queued, and ATAPI command/data protocols are supported by the SATA controller AHCI engine:

- Standard SATA command-related
  - Nondata command protocol
  - PIO write protocol
  - PIO read protocol
  - DMA write protocol
  - DMA read protocol
- NCQ command-related
  - Write FPDMA-queued protocol
  - Read FPDMA-queued protocol
- ATAPI PACKET command-related
  - PACKET Nondata command protocol
  - PACKET PIO read/write protocol
  - PACKET DMA read/write protocol

23.12.4.11 SATA Controller AHCI Hardware Register Interface

Table 23-1413 summarizes the SATA host controller subsystem registers and divides them into functional categories.

Table 23-1413. Summary of SATA Host Subsystem Functional Registers

Register	Functional Category	Brief Register Description
SATA_SYSCONFIG	Device-level registers (wrapper of SATA AHCI core)	TI wrapper idle/standby power management configuration register
SATA_CDRLOCK(1)		TI wrapper register which defines default delay of received data valid information.
SATA_IDR	SATA vendor-specific (VS) register	TI high lander identification register
SATA_CAP	SATA controller generic registers	SATA HBA capabilities set 1
SATA_CAP2		SATA HBA capabilities set 2
SATA_VS		SATA HBA register showing supported AHCI specification revision
SATA_GPARAM1R		SATA HBA global parameters set 1
SATA_GPARAM2R		SATA HBA global parameters set 2
SATA_GHC		SATA HBA global AHCI settings
SATA_PPARAMR	SATA HBA ports-related registers	SATA HBA port x(2) parameter settings
SATA_PI		Enables SATA HBA port x(2) functionalities
SATA_IS		Enables all SATA HBA port x(2) associated interrupts (first tier of interrupt schema)
SATA_CCC_PORTS		Enables SATA CCC feature for the port x(2)
SATA_CCC_CTL		CCC feature parameters control and status
SATA_TIMER1MS		Time base for 1-ms unit of CCC timeout

(1) Under normal conditions, the user is supposed to keep this register at its default (power-on-reset) value.
(2) x = 0, as only SATA HBA port 0 is implemented

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Table 23-1413. Summary of SATA Host Subsystem Functional Registers (continued)

Register	Functional Category	Brief Register Description
SATA_PxCLB	SATA HBA Port Px[2] SATA Specification- defined Functional Registers	CL base address (lower-half of AHCI 64-bit address)
SATA_PxCLBU		CL base address (upper-half of AHCI 64-bit address)[3]
SATA_PxFB		Received FISs base address (lower-half of AHCI 64-bit address)
SATA_PxFBU		Received FISs base address (upper-half of AHCI 64-bit address)[3]
SATA_PxIE		Port x[2] non-CCC interrupt enable
SATA_PxIS		Port x[2] non-CCC interrupt event status
SATA_PxCMD		Port x[2] command register
SATA_PxTFD		Port x[2] task file data register
SATA_PxSIG		Port x[2] associated SATA signature register
SATA_PxSSTS		Port x[2] SStatus SATA register (See the SATA standard specification.)
SATA_PxSCTL		Port x [2]SControl SATA register (See the SATA standard specification.)
SATA_PxSERR		Port x [2]SError SATA register (See the SATA standard specification.)
SATA_PxSACT		Port x[2] SActive SATA register (See SATA standard specification.)
SATA_PxCI		Port x [2]command activation/completion indication register
SATA_PxSNTF		Port x[2] SNotification register (See the SATA standard specification.)
SATA_OOBR		OOB detection counters setup
SATA_PxDMACR	Non-standard Port Px[4] Control register	Port x[4] associated DMA configuration register
SATA_TESTR	SATA HBA BIST related registers	Test/normal mode switching
SATA_BISTAFR		BIST FIS-activate register
SATA_BISTCR		BIST control register
SATA_BISTFCTR		BIST FIS count register
SATA_BISTSR		BIST status register
SATA_BISTDECR		BIST Dword error count register

(3) Only the 4-lower bits meaningful in the device, the others must be kept at '0'
(4) x = 0, as only SATA HBA port 0 is implemented

23.12.5 SATA Controller Low Level Programming Model

This section describes the low-level hardware programming sequences for the configuration and use of the SATA host controller.

23.12.5.1 Global Initialization

23.12.5.1.1 Surrounding Modules Global Initialization

This section identifies the requirements to initialize the surrounding modules when the SATA host controller is used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the SATA host controller (for more information, see Section 23.12.2 and Section 23.12.3). Table 23-1414 describes the global initialization of surrounding modules.

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Table 23-1414. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module functional and interface clocks must be enabled (see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*).
Control Module	Module-specific pad muxing and other PHY power configurations must be set in the control module (see Section 18.4.8, *Pad Functional Multiplexing and Configuration* and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*).
MPU INTC	INTC_MPU must be configured to enable the interrupt from the SATA controller (see Section 17.3.2, *Interrupt Requests to INTC_MPU*, in Chapter 17, *Interrupt Controllers*).
L4_CFG and L3_MAIN interconnects	For more information about the interconnect configuration, see Section 14.2.3.2.1,*L3_MAIN Interconnect Agents* and Section 14.3.1, *L4 Interconnect Overview*, in Chapter 14, *Interconnect.*

NOTE: The MPU INTC configuration is required when using the interrupt communication mode.

23.12.5.1.2 SATA Controller Global Initialization

23.12.5.1.2.1 Main Sequence SATA Controller Global Initialization

Table 23-1415 describes the procedure to initialize the SATA host controller after a POR.

Table 23-1415. SATA Controller Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure the OCP2SCP3 adapter for PLLCTRL_SATA.	See Section 27.1.5, *SATA PHY Subsystem Low - Level Programming Model* in Chapter 27, *Shared PHY Component Subsytems*.	-
Configure the DPLL_SATA.	See Section 27.1.5, *SATA PHY Subsystem Low - Level Programming Model* in Chapter 27, *Shared PHY Component Subsytems*.	-
Configure the SATA_PHY.	See Section 27.1.5, *SATA PHY Subsystem Low - Level Programming Model* in Chapter 27, *Shared PHY Component Subsytems*.	-
Perform all firmware capability writes. (1)	See Section 23.12.5.1.2.2, *SubSequence—Firmware Capability Writes*.	-
Set up all appropriate structures in memory per the AHCI standard specification.	See Section 23.12.4.6, *System Memory FIS Descriptors*. See also the AHCI standard specification.	-
Write a valid CL memory base address to the SATA_PxCLB register.	SATA_PxCLB [31:10] CLB	CL Base address (lower-half)
	SATA_PxCLBU [3:0] CLBU	CL Base address (upper-half) Only 4-lower bits meaningful in the device, other must be always written to '0'-s
Write a valid Rx FIS memory base address to the SATA_PxFB register.	SATA_PxFB [31:8] FB	Rx FIS Base address (lower-half)
	SATA_PxFBU [3:0] FBU	Rx FIS Base address (upper-half) Only 4-lower bits meaningful in the device, other must be always written to '0'-s
Issue a software type of reset depending on the error condition.	See Section 23.12.4.3.2, *Software Initiated Resets*.	-
Set the appropriate bits in the SATA_PxCMD register.	See section Section 23.12.4.7.1, *Software Processing of the Port Command List* . See also the AHCI standard specification.	-

(1) This step has an effect only on hardware initialization.

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Table 23-1415. SATA Controller Global Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Program the SATA_PxSCTL register to configure SATA interface capabilities.	See the AHCI standard specification.	-
Program the SATA_PxDMACR register.	See Section 23.12.4.8, *DMA Port Configuration*.	-
Enable the interrupts at port 0.	SATA_IS[0] IPS	0x1
Enable the involved port 0 specific interrupts.	See Section 23.12.4.5.2, *Levels of Interrupt Control*, and Section 23.12.4.5.4, *Interrupt Condition Control*.	-
Enable the FIS reception in the SATA_PxCMD register.	SATA_PxCMD[4] FRE	0x1
Spin up the device (if required).	See the AHCI standard specification and the SATA standard specification.	-

NOTE: The SATA AHCI Controller always manipulates 64-bit memory pointers, and the master interface has 64-bit addresses, but the actual AHCI master interface integration in the device uses ONLY the 36-lower bits. In that case, even though the AHCI support indicates “64-bit” in the SATA_CAP[31] S64A, ONLY the 4-lower bits (SATA_PxCLBU [3:0] / SATA_PxFBU [3:0]) are meaningful in the device.**The upper 28 bits of the address, i.e.** SATA_PxCLBU [31:4] / SATA_PxFBU [31:4] **,must be always SW-programmed to '0'.**

NOTE: Default value of the SATA_PxCLBU / SATA_PxFBU registers is 0x0, so that a 32-bit SW driver which never accesses them works seamlessly, by accessing only the 32-bit (lower half) addresses which reside in the SATA_PxCLB / SATA_PxFB registers.

23.12.5.1.2.2 SubSequence – Firmware Capability Writes

Table 23-1416 lists the firmware capability write sequence by which SATA HBA initialization is performed.

NOTE: In the following sequence, SATA controller accesses hardware initialization domain registers that can be written only one time after POR.

Table 23-1416. Firmware Capability Writes

Step	Register/Bit Field/Programming Model	Value
Disable the staggered spin-up support feature.(1)	SATA_CAP[27] SSS	0x0
Enable the SATA controller port 0.	SATA_PI[0] PI	0x1
Disable the mechanical presence detect feature.(1)	SATA_CAP[28] SMPS	0x0
Disable the external signal-only connector.(1)	SATA_PxCMD[22:21] ESP	0x0
Disable the cold presence detect feature. (1)	SATA_PxCMD[20] CPD	0x0
Disable support for the mechanical presence switch.	SATA_PxCMD[19] MPSP	0x0
Disable the hot-plug-capable port feature.	SATA_PxCMD[18] HPCP	0x0
Clear the SATA_PxCMD[17] PMA bit as a notification that a single-target SATA device is attached to port 0.	SATA_PxCMD[17] PMA	0x0

(1) It makes no sense to enable staggered spin-up because only one HBA port is used.

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23.12.5.1.3 Issue Command - Main Sequence

The procedure in Table 23-1417 prepares a command list entry and issues its corresponding command.

Table 23-1417. Prepare and Issue a Command

Step	Register/Bit Field/Programming Model	Value
Build command header and command table into host system memory.	For details, see Section 23.12.4.6.1, *Command List Structure Basics*.	-
Create the command corresponding PRD table.		
Queue the command to the command list.	See Section 23.12.4.7.1, *Software Processing of the Port Command List*.	-
Set the SATA_PxCMD[0] ST bit to direct the DMA to start processing the CL.	SATA_PxCMD[0] ST	0x1 (1)
IF a nonNCQ command is issued:		
Set the corresponding SATA_PxCI.CI bit to activate a command already prepared in the i-th slot of the CL .	SATA_PxCI[i] CI	0x-
ELSE		
Indicate the NCQ slot positions through the SATA_PxSACT register. For details on TAG tracking, see Section 23.12.4.7.1.	SATA_PxSACT[TAG] DS	0x-
Set the corresponding SATA_PxCI.CI bit to activate the NCQ command already prepared in the i-th slot of the CL.	SATA_PxCI[TAG] CI	0x-

(1) See the AHCI standard specification for important restrictions when PXCMD[0] ST can be software-asserted to 1.

23.12.5.1.4 Receive FIS—Main Sequence

The procedure in Table 23-1418 is used to handle a FIS reception.

Table 23-1418. FIS Reception

Step	Register/Bit Field/Programming Model	Value
Read SATA_PxIS to determine the type of FIS.	For more information, see Section 23.12.4.7.2, *Handling the Received FIS Descriptors*.	-

23.12.6 SATA Controller Register Manual

23.12.6.1 SATA Controller Instance Summary

Table 23-1419. SATA Instance Summary

Module Name	Module Base Address	Size (Bytes)
DWC_ahsata	0x4A14 0000	4352
SATAMAC_wrapper	0x4A14 1100	256

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23.12.6.2 DWC_ahsata Registers

23.12.6.2.1 DWC_ahsata Register Summary

Table 23-1420. DWC_ahsata Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address (L4 Interconnect)
SATA_CAP	RW	32	0x0000 0000	0x4A14 0000
SATA_GHC	RW	32	0x0000 0004	0x4A14 0004
SATA_IS	RW	32	0x0000 0008	0x4A14 0008
SATA_PI	RW	32	0x0000 000C	0x4A14 000C
SATA_VS	R	32	0x0000 0010	0x4A14 0010
SATA_CCC_CTL	RW	32	0x0000 0014	0x4A14 0014
SATA_CCC_PORTS	RW	32	0x0000 0018	0x4A14 0018
SATA_CAP2	R	32	0x0000 0024	0x4A14 0024
SATA_BISTAFR	R	32	0x0000 00A0	0x4A14 00A0
SATA_BISTCR	RW	32	0x0000 00A4	0x4A14 00A4
SATA_BISTFCTR	R	32	0x0000 00A8	0x4A14 00A8
SATA_BISTSR	R	32	0x0000 00AC	0x4A14 00AC
SATA_BISTDECR	R	32	0x0000 00B0	0x4A14 00B0
SATA_OOBR	RW	32	0x0000 00BC	0x4A14 00BC
SATA_TIMER1MS	RW	32	0x0000 00E0	0x4A14 00E0
SATA_GPARAM1R	R	32	0x0000 00E8	0x4A14 00E8
SATA_GPARAM2R	R	32	0x0000 00EC	0x4A14 00EC
SATA_PPARAMR	R	32	0x0000 00F0	0x4A14 00F0
SATA_TESTR	RW	32	0x0000 00F4	0x4A14 00F4
SATA_VERSIONR	R	32	0x0000 00F8	0x4A14 00F8
SATA_IDR	R	32	0x0000 00FC	0x4A14 00FC
SATA_PxCLB	RW	32	0x0000 0100	0x4A14 0100
SATA_PxCLBU	RW	32	0x0000 0104	0x4A14 0104
SATA_PxFB	RW	32	0x0000 0108	0x4A14 0108
SATA_PxFBU	RW	32	0x0000 010C	0x4A14 010C
SATA_PxIS	RW	32	0x0000 0110	0x4A14 0110
SATA_PxIE	RW	32	0x0000 0114	0x4A14 0114
SATA_PxCMD	RW	32	0x0000 0118	0x4A14 0118
SATA_PxTFD	R	32	0x0000 0120	0x4A14 0120
SATA_PxSIG	R	32	0x0000 0124	0x4A14 0124
SATA_PxSSTS	R	32	0x0000 0128	0x4A14 0128
SATA_PxSCTL	RW	32	0x0000 012C	0x4A14 012C
SATA_PxSERR	RW	32	0x0000 0130	0x4A14 0130
SATA_PxSACT	RW	32	0x0000 0134	0x4A14 0134
SATA_PxCI	RW	32	0x0000 0138	0x4A14 0138
SATA_PxSNTF	RW	32	0x0000 013C	0x4A14 013C
SATA_PxDMACR	RW	32	0x0000 0170	0x4A14 0170

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23.12.6.2.2 DWC_ahsata Register Description

NOTE: Regardless of the SATA_CAP[17] SPM bit being read as 0b1, command-based switching Port Multiplier (PM) is unsupported by the only device SATA Controller port (Port 0). It is therefore recommended that user always configure attachment of a single mass storage device to device SATA port and disable the PM feature in software.

Table 23-1421. SATA_CAP

Address Offset	0x0000 0000		
Physical Address	0x4A14 0000	**Instance**	DWC_ahsata
Description	Capabilities register: Basic capabilities of the SATA AHCI core. Some fields can be written once after reset, read-only.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S64A	SNCQ	SSNTF	SMPS	SSS	SALP	SAL	SCLO	ISS				SNZO	SAM	SPM	FBSS	PMD	SSC	PSC	NCS					CCCS	EMS	SXS	NP				

Bits	Field Name	Description	Type	Reset
31	S64A	Supports 64-bit addressing Read 0x1: 64-bit addressing supported Read 0x0: 32-bit addressing supported	R	1
30	SNCQ	Supports NCQ Controller supports SATA NCQ by handling DMA setup FIS natively. Read 0x1: Supported Read 0x0: Not supported	R	1
29	SSNTF	Supports SNotification register Controller supports SATA_PxSNTF (SNotification) register and its associated functionality. Read 0x1: Supported Read 0x0: Not supported	R	1
28	SMPS	Supports mechanical presence switch Support of a mechanical presence switch for hot plug operation, depending on integration Writable once after power up, read-only afterward 0x0: Not supported 0x1: Supported	RW WSpecial	0
27	SSS	Supports staggered spin-up Controller can support this feature through SATA_PxCMD.SUD Writable once after power up, read-only afterward 0x0: Not supported 0x1: Supported	RW WSpecial	0
26	SALP	Supports aggressive link power management Read 0x1: Supported Read 0x0: Not supported	R	1
25	SAL	Supports Activity LED Read 0x1: Supported Read 0x0: Not supported	R	1

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Bits	Field Name	Description	Type	Reset
24	SCLO	Supports command list override Supports the SATA_PxCMD.CLO bit functionality for enumeration of PM devices Read 0x1: Supported Read 0x0: Not supported	R	1
23:20	ISS	Interface speed support Maximum speed the HBA can support Read 0x3: Gen 3 = 6 Gbps Read 0x2: Gen 2 = 3 Gbps Read 0x1: Gen 1 = 1.5 Gbps	R	0x2
19	SNZO	Supports Non-zero DMA offsets Read 0x1: Supported Read 0x0: Not supported	R	0
18	SAM	Supports AHCI mode only SATA controller supports AHCI mode only and does not support legacy, task file-based register interface. Read 0x1: Supported Read 0x0: Not supported	R	1
17	SPM	Supports PM SATA controller supports command-based switching PM on any port. Read 0x1: Supported Read 0x0: Not supported	R	1
16	FBSS	FIS-based switching supported Support of PM FIS-based switching. Read 0x1: Supported Read 0x0: Not supported	R	0
15	PMD	PIO Multiple DRQ Support of multiple DRQ block data transfers for the PIO command protocol Read 0x1: Supported Read 0x0: Not supported	R	1
14	SSC	SLUMBER state capable Support of transitions to the interface SLUMBER power management state Read 0x1: Supported Read 0x0: Not supported	R	1
13	PSC	PARTIAL state capable Support of transitions to the interface PARTIAL power management state Read 0x1: Supported Read 0x0: Not supported	R	1
12:8	NCS	Number of command slots: slots supported by the SATA controller, minus 1 Read 0x1F: 32 command slots	R	0x1F
7	CCCS	Command completion coalescing supported Read 0x1: Supported Read 0x0: Not supported	R	1
6	EMS	Enclosure management supported Read 0x1: Supported Read 0x0: Not supported	R	0
5	SXS	Supports external SATA Read 0x1: Supported Read 0x0: Not supported	R	0

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Bits	Field Name	Description	Type	Reset
4:0	NP	Number of ports: ports supported by the SATA controller, minus 1 Read 0x1: 2 ports Read 0x0: 1 port	R	0x00

Table 23-1422. Register Call Summary for Register SATA_CAP

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- Main Sequence SATA Controller Global Initialization: [1]
- SubSequence – Firmware Capability Writes: [2] [3]
- DWC_ahsata Register Summary: [4]
- DWC_ahsata Register Description: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14]

Table 23-1423. SATA_GHC

Address Offset	0x0000 0004		
Physical Address	0x4A14 0004	**Instance**	DWC_ahsata
Description	Global HBA control		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AE	RESERVED																													IE	HR

Bits	Field Name	Description	Type	Reset
31	AE	AHCI enable Always set because SATA controller supports AHCI mode only, as indicated by the SATA_CAP.SAM = 1	R	1
30:2	RESERVED		R	0x0000 0000
1	IE	Interrupt enable Global enable of SATA controller interrupts. Reset on global reset (SATA_GHC.HR = 1). 0x0: All interrupt sources from all ports are disabled (masked). 0x1: Interrupts are enabled and any SATA controller interrupt event causes interrupt output assertion.	RW	0
0	HR	HBA reset Global reset control Write 0x0: No action Write 0x1: Start global reset: All state machines that relate to data transfers and queuing return to an IDLE state, and all ports are reinitialized by sending COMRESET if staggered spin-up is not supported. If staggered spin-up is supported, it is the responsibility of the software to spin up each port after this reset completes. Read 0x1: Reset is ongoing. Read 0x0: Reset is inactive (done).	RW	0

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Table 23-1424. Register Call Summary for Register SATA_GHC

SATA Controller

- HBA Reset: [0] [1]
- Levels of Interrupt Control: [2]
- Interrupt Condition Control: [3]
- SATA Controller AHCI Hardware Register Interface: [4]
- DWC_ahsata Register Summary: [5]
- DWC_ahsata Register Description: [6] [7] [8] [9] [10]

Table 23-1425. SATA_IS

Address Offset	0x0000 0008		
Physical Address	0x4A14 0008	**Instance**	DWC_ahsata
Description	Interrupt status Indicates which port has a pending interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															IPS

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	IPS	Interrupt pending status. Bit-significant field. Bits are set by ports that have interrupt events pending in the SATA_PxIS bits and enabled in SATA_PxIE. Set bits are cleared by software writing 1 to them.	RW W1toClr	0

Table 23-1426. Register Call Summary for Register SATA_IS

SATA Controller

- Levels of Interrupt Control: [0] [1] [2] [3]
- Interrupt Condition Control: [4]
- SATA Controller AHCI Hardware Register Interface: [5]
- Main Sequence SATA Controller Global Initialization: [6]
- DWC_ahsata Register Summary: [7]
- DWC_ahsata Register Description: [8]

Table 23-1427. SATA_PI

Address Offset	0x0000 000C		
Physical Address	0x4A14 000C	**Instance**	DWC_ahsata
Description	Ports implemented Indicates which ports are exposed by the SATA controller and available for use		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															PI

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	PI	Ports implemented. Bit-significant field. Writable once after power up, read-only afterward. If a bit is set (1), the corresponding port is available; else (0) it is not. Only bits 0 to SATA_CAP.NP can be set to 1. At least one bit must be set to 1.	RW WSpecial	0

Table 23-1428. Register Call Summary for Register SATA_PI

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- SubSequence – Firmware Capability Writes: [1]
- DWC_ahsata Register Summary: [2]
- DWC_ahsata Register Description: [3]

Table 23-1429. SATA_VS

Address Offset	0x0000 0010		
Physical Address	0x4A14 0010	**Instance**	DWC_ahsata
Description	AHCI version supported: 1.3 WARNING: Controller complies fully with AHCI version 1.10 and also complies with AHCI version 1.3 except for FIS-based switching, which is not currently supported.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MJR																MNR															

Bits	Field Name	Description	Type	Reset
31:16	MJR	Major Version Number: 1	R	0x0001
15:0	MNR	Minor Version Number: 3.00	R	0x0300

Table 23-1430. Register Call Summary for Register SATA_VS

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]

Table 23-1431. SATA_CCC_CTL

Address Offset	0x0000 0014		
Physical Address	0x4A14 0014	**Instance**	DWC_ahsata
Description	CCC control Used to configure the CCC feature for the SATA controller Reset on global reset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TV																CC								INT					RESERVED		EN

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Bits	Field Name	Description	Type	Reset
31:16	TV	Timeout value. Time-out value. Specifies the CCC time-out value in 1-ms intervals Loaded prior to enabling CCC; becomes read-only when SATA_CCC_CTL.EN = 1 0x0: Reserved value; do not use. 0x1 - 0xFFFF: timeout slectable between within the range (1 - 65535) ms.	RW	0x0001
15:8	CC	Command completions Number of command completions necessary to cause a CCC interrupt Loaded prior to enabling CCC, becomes read-only when SATA_CCC_CTL.EN = 1 0x0: CCC interrupts generated based on the timer, not on completed commands count 0x1 - 0xFF: specifies the number of commands upon which completion a CCC interrupt is generated. The number of commands to complete before interrupt is triggered are selectable within the range (1 - 255) commands.	RW	0x01
7:3	INT	Interrupt Number of the interrupt used by the CCC feature, using the number of ports configured for the core When a CCC interrupt occurs, the SATA_IS.IPS[INT] bit is set to 1.	R	0x01
2:1	RESERVED		R	0x0
0	EN	Enable CCC enable 0x0: CCC feature is disabled and no CCC interrupts are generated. SATA_CCC_CTL.TV and .CC are writable. 0x1: CCC feature is enabled and CCC interrupts can be generated based on the time-out or command completion conditions. All other SATA_CCC_CTL fields are read-only.	RW	0

Table 23-1432. Register Call Summary for Register SATA_CCC_CTL

SATA Controller

- Interrupt Condition Control: [0]
- Command Completion Coalescing Interrupts: [1] [2] [3] [4]
- CCC Interrupt Based on Expired Timeout Value: [5] [6] [7] [8] [9] [10] [11]
- CCC Interrupt Based on Completion Count: [12] [13] [14] [15] [16]
- SATA Controller AHCI Hardware Register Interface: [17]
- DWC_ahsata Register Summary: [18]
- DWC_ahsata Register Description: [19] [20] [21] [22] [23]

Table 23-1433. SATA_CCC_PORTS

Address Offset	0x0000 0018		
Physical Address	0x4A14 0018	**Instance**	DWC_ahsata
Description	CCC ports Specifies the ports that are coalesced as part of the CCC feature when SATA_CCC_CTL.EN = 1 Reset on global reset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															PRT

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	PRT	Ports Bit-significant field Set a bit to 1 to make the corresponding port part of the CCC feature. Bits set to 1 in this register have the same bit set to 1 in register PI.	RW	0

Table 23-1434. Register Call Summary for Register SATA_CCC_PORTS

SATA Controller

- Command Completion Coalescing Interrupts: [0] [1]
- CCC Interrupt Based on Expired Timeout Value: [2]
- CCC Interrupt Based on Completion Count: [3]
- SATA Controller AHCI Hardware Register Interface: [4]
- DWC_ahsata Register Summary: [5]

Table 23-1435. SATA_CAP2

Address Offset	0x0000 0024		
Physical Address	0x4A14 0024	**Instance**	DWC_ahsata
Description	Extended capabilities		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													APST	NVMP	BOH

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	APST	Automatic PARTIAL to SLUMBER transitions Read 0x1: Supported Read 0x0: Not supported	R	1
1	NVMP	NVMHCI present Read 0x1: Supported Read 0x0: Not supported	R	0
0	BOH	BIOS/OS Handoff Read 0x1: Supported Read 0x0: Not supported	R	0

Table 23-1436. Register Call Summary for Register SATA_CAP2

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]

Table 23-1437. SATA_BISTAFR

Address Offset	0x0000 00A0		
Physical Address	0x4A14 00A0	**Instance**	DWC_ahsata
Description	Built-In, Self-Test (BIST) Activate FIS Register Reset on global reset or port reset		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																NCP								PD							

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	NCP	Noncompliant pattern Least significant byte of the received BIST Activate FIS second DWORD (bits [7:0]). This value defines the required pattern for far-end transmit-only mode (SATA_BISTAFR.PD = 0xC0 or 0xE0). If none of the listed values is decoded, the simultaneous switching pattern is transmitted by default. Read 0x4A: High frequency test pattern (HFTP) Read 0xF1: Low transition density pattern (LTDP) Read 0xB5: High transition density pattern (HTDP) Read 0x8B: Lone bit pattern (LBP) Read 0x7F: Simultaneous switching outputs pattern (SSOP) Read 0x78: Mid-frequency test pattern (MFTP) Read 0xAB: Low frequency spectral component pattern (LFSCP) Read 0x7E: Low frequency test pattern (LFTP)	R	0x00
7:0	PD	Pattern definition Pattern definition field of the received BIST Activate FIS - bits [23:16] of the first DWORD. Puts the SATA controller in one of the listed BIST modes Read 0x10: Far-end retimed Read 0xC0: Far-end transmit only Read 0xE0: Far-end transmit only with scrambler bypassed Read 0x8: Far-end analog (if PHY supports this mode)	R	0x00

Table 23-1438. Register Call Summary for Register SATA_BISTAFR

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]
- DWC_ahsata Register Description: [2] [3] [4]

Table 23-1439. SATA_BISTCR

Address Offset	0x0000 00A4		
Physical Address	0x4A14 00A4	**Instance**	DWC_ahsata
Description	BIST control register Reset on global reset or port reset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											FERLB	RESERVED	TXO	CNTCLR	NEALB	RESERVED		ERRLOSSEN	SDFE	RESERVED	LLC_RPD	LLC_DESCRAM	LLC_SCRAM	RESERVED		ERREN	FLIP	PV	PATTERN		

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Bits	Field Name	Description	Type[1]	Reset
31:21	RESERVED		R	0x000
20	FERLB	Far-end retimed loopback Write 0x0: No action Write 0x1: Puts the DWC_ahsata link into far-end retimed mode without the BIST activate FIS, regardless of whether the device is connected or disconnected (link in NOCOMM state) Read 0x0: Read returns 0	WO	0
19	RESERVED		R	0
18	TXO	Transmit only Write 0x0: No action Write 0x1: Initiate transmission of one of the noncompliant patterns defined by the SATA_BISTCR.PATTERN value when the device is disconnected. Read 0x0: Read returns 0.	WO	0
17	CNTCLR	Counter clear Clears BIST error count registers Write 0x0: No action Write 0x1: Clear SATA_BISTFCTR, SATA_BISTSR, and SATA_BISTDECR registers Read 0x0: Read returns 0	WO	0
16	NEALB	Near-end analog loopback This mode should be initiated in the PARTIAL or SLUMBER power state or with the device disconnected from the port PHY (link NOCOMM state). BIST Activate FIS is not sent to the device in this mode. Write 0x0: No action Write 0x1: Places the port PHY in near-end analog loopback mode. SATA_BISTCR.PATTERN bit field contains the appropriate pattern.	WO	0
15:14	RESERVED		R	0x0
13	ERRLOSSEN	Always keep this bit at default value.	RW	0
12	SDFE	Signal detect feature enable Not affected by global reset or port reset 0x0: Link layer feature to handle unstable/absent phy_sig_det signal is disabled. 0x1: Link layer feature to handle unstable/absent phy_sig_det signal is enabled.	RW	0
11	RESERVED	Only write 0 into this reserved field to avoid undefined results.	RW	0
10	LLC_RPD	Link layer control, repeat primitive drop In normal mode, the function can be changed only during port reset (SATA_PxSCTL.DET = 0x1). 0x0: Repeat primitive drop function disabled in normal mode, enabled in BIST mode 0x1: Repeat primitive drop function enabled in normal mode, disabled in BIST mode	RW	1
9	LLC_DESCRAM	Link layer control, descrambler In normal mode, the function can be changed only during port reset (SATA_PxSCTL.DET = 0x1). 0x0: Descrambler disabled in normal mode, enabled in BIST mode 0x1: Descrambler enabled in normal mode, disabled in BIST mode	RW	1

(1) WO = A write-only accessible bit field

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Bits	Field Name	Description	Type[1]	Reset
8	LLC_SCRAM	Link layer control, scrambler In normal mode, the function can be changed only during port reset (SATA_PxSCTL.DET = 0x1). Hardware–cleared (enabled) when the port enters a responder far-end transmit BIST mode with scrambling enabled (SATA_BISTAFR.PD = 0xC0). 0x0: Scrambler disabled in normal mode, enabled in BIST mode. 0x1: Scrambler enabled in normal mode, disabled in BIST mode.	RW	1
7	RESERVED		R	0
6	ERREN	Error enable Allow or filter (disable) PHY internal errors outside the FIS boundary to set corresponding SATA_PxSERR bits 0x0: Filter errors outside the FIS; allow errors inside the FIS. 0x1: Allow errors outside or inside the FIS.	RW	0
5	FLIP	Flip disparity Change disparity of the current test pattern to the opposite each time its state is changed by software.	RW	0
4	PV	Pattern version Selects either short or long version of the SSOP, HTDP, LTDP, LFSCP, COMP pattern 0x0: Short pattern version 0x1: Long pattern version	RW	0
3:0	PATTERN	Pattern Defines one of the listed SATA-compliant patterns for far-end retimed/ far-end analog/ near-end analog initiator modes, or noncompliant patterns for transmit-only responder mode when initiated by software writing to the SATA_BISTCR.TXO bit 0x6: Mid-frequency test pattern (MFTP) 0x1: High transition density pattern (HTDP) 0x7: High frequency test pattern (HFTP) 0x0: Simultaneous switching outputs pattern (SSOP) 0x2: Low transition density pattern (LTDP) 0x8: Low frequency test pattern (LFTP) 0x4: Composite pattern (COMP) 0x5: Lone bit pattern (LBP) 0x3: Low frequency spectral component pattern (LFSCP)	RW	0x0

Table 23-1440. Register Call Summary for Register SATA_BISTCR

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]
- DWC_ahsata Register Description: [2] [3] [4] [5] [6] [7] [8]

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Table 23-1441. SATA_BISTFCTR

Address Offset	0x0000 00A8		
Physical Address	0x4A14 00A8	**Instance**	DWC_ahsata
Description	BIST frame-information-structure CounT register Received BIST FIS count in the loopback initiator far-end retimed, far-end analog, and near-end analog modes. Updated each time a new BIST FIS is received. Reset by global reset, port reset (COMRESET), or by writing 1 to SATA_BISTCR.CNTCLR Does not roll over and freezes when the FFFF_FFFFh value is reached. It takes approximately 65 hours of continuous BIST operation to reach this value.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															

Bits	Field Name	Description	Type	Reset
31:0	COUNT	BIST FIS Count	R	0x0000 0000

Table 23-1442. Register Call Summary for Register SATA_BISTFCTR

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]
- DWC_ahsata Register Description: [2] [3]

Table 23-1443. SATA_BISTSR

Address Offset	0x0000 00AC		
Physical Address	0x4A14 00AC	**Instance**	DWC_ahsata
Description	BIST status register Errors detected in the received BIST FIS in the loopback initiator far-end retimed, far-end analog, and near-end analog modes Updated each time a new BIST FIS is received Reset on global reset, port reset (COMRESET), or by writing 1 to SATA_BISTCR.CNTCLR		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BRSTERR								FRAMERR															

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	BRSTERR	Burst error count. Accumulated each time a burst error condition is detected: DWORD error is detected in the received frame and 1.5 seconds (27,000 frames) passed since the previous burst error was detected. Value does not roll over and freezes at FFh. Read 0xFF: Max error count reached or exceeded Read 0x0: No error detected	R	0x00
15:0	FRAMERR	Frame error count. New value is added to the old value each time a new BIST frame with a CRC error is received. Does not roll over and freezes at FFFFh Read 0xFFFF: Maximum error count reached or exceeded. Read 0x0: No error detected	R	0x0000

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Table 23-1444. Register Call Summary for Register SATA_BISTSR

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]
- DWC_ahsata Register Description: [2] [3]

Table 23-1445. SATA_BISTDECR

Address Offset	0x0000 00B0		
Physical Address	0x4A14 00B0	**Instance**	DWC_ahsata
Description	BIST double-word error count register Number of DWORD errors detected in the received BIST frame in the loopback initiator far-end retimed, far-end analog, and near-end analog modes Updated each time a new BIST frame is received, when the parameter BIST_MODE = DWORD. Reset on global reset, port reset (COMRESET), or by writing 1 to SATA_BISTCR.CNTCLR.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWERR																															

Bits	Field Name	Description	Type	Reset
31:0	DWERR	DWORD error count. New value is added to the old value each time a new BIST frame is received. The DWERR value does not roll over, and freezes when it exceeds 0xFFFF_F000. Read 0x0: No error detected Read 0xFFFFF000: Max error count reached or exceeded	R	0x0000 0000

Table 23-1446. Register Call Summary for Register SATA_BISTDECR

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]
- DWC_ahsata Register Description: [2] [3]

Table 23-1447. SATA_OOBR

Address Offset	0x0000 00BC		
Physical Address	0x4A14 00BC	**Instance**	DWC_ahsata
Description	OOB register Controls the link layer OOB detection counters		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WE	CWMIN							CWMAX								CIMIN								CIMAX							

Bits	Field Name	Description	Type	Reset
31	WE	WRITE_ENABLE 0x0: SATA_OOBR bits [30:0] are read-only. 0x1: SATA_OOBR bits [30:0] can be written.	RW	0
30:24	CWMIN	COMWAKE_MIN, in OOB rx clock cycles Read-only when SATA_OOBR.WE = 0	RW WSpecial	0x0B
23:16	CWMAX	COMWAKE_MAX, in OOB rx clock cycles Read-only when SATA_OOBR.WE = 0	RW WSpecial	0x15

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Bits	Field Name	Description	Type	Reset
15:8	CIMIN	COMINIT_MIN, in OOB rx clock cycles Read-only when SATA_OOBR.WE = 0	RW WSpecial	0x24
7:0	CIMAX	COMINIT_MAX, in OOB rx clock cycles Read-only when SATA_OOBR.WE=0	RW WSpecial	0x40

Table 23-1448. Register Call Summary for Register SATA_OOBR

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]
- DWC_ahsata Register Description: [2] [3] [4] [5] [6] [7]

Table 23-1449. SATA_TIMER1MS

Address Offset	0x0000 00E0		
Physical Address	0x4A14 00E0	**Instance**	DWC_ahsata
Description	Timer 1 ms Configuration to generate the 1-ms tick for the CCC logic Must be initialized before using the CCC feature Reset on power up, not affected by global reset		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMV																							

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:0	TIMV	OCP bus clock frequency in kHz (for example, reset value is 100,000 = 100 MHz)	RW	0x1 86A0

Table 23-1450. Register Call Summary for Register SATA_TIMER1MS

SATA Controller

- Command Completion Coalescing Interrupts: [0] [1]
- CCC Interrupt Based on Expired Timeout Value: [2]
- SATA Controller AHCI Hardware Register Interface: [3]
- DWC_ahsata Register Summary: [4]

Table 23-1451. SATA_GPARAM1R

Address Offset	0x0000 00E8		
Physical Address	0x4A14 00E8	**Instance**	DWC_ahsata
Description	Global parameters register 1 Hardware configuration of the DWC AHCI SATA core		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALIGN_M	RX_BUFFER	PHY_DATA	PHY_RST	PHY_CTRL				PHY_STAT								LATCH_M	BIST_M	PHY_TYPE			RETURN_ERR	AHB_ENDIAN		S_HADDR	M_HADDR	S_HDATA				M_HDATA	

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Bits	Field Name	Description	Type	Reset
31	ALIGN_M	RX data alignment Read 0x1: Yes Read 0x0: No	R	1
30	RX_BUFFER	RX data buffer implemented Read 0x1: Yes Read 0x0: No	R	1
29:28	PHY_DATA	PHY data width (in 8- or 10-bit characters) Read 0x2: 4 characters Read 0x1: 2 characters Read 0x0: 1 character	R	0x0
27	PHY_RST	PHY reset mode Read 0x1: High Read 0x0: Low	R	1
26:21	PHY_CTRL	PHY control width (in bits)	R	0x00
20:15	PHY_STAT	PHY status width (in bits)	R	0x00
14	LATCH_M	Test mode lock-up latches Read 0x1: Yes Read 0x0: No	R	0
13	BIST_M	BIST loopback checking depth Read 0x1: DWORD Read 0x0: FIS	R	0
12:11	PHY_TYPE	PHY interface type Read 0x1: Preset Read 0x0: Configurable 0x2, 0x3: Reserved	R	0x0
10	RETURN_ERR	Error response on illegal access Read 0x1: Yes Read 0x0: No	R	0
9:8	AHB_ENDIAN	Endianness of master and slave Read 0x2: Pin-configurable dynamic endianness Read 0x1: Big-endian Read 0x0: Little-endian	R	0x0
7	S_HADDR	Slave address bus width Read 0x1: 64-bit address Read 0x0: 32-bit address	R	0
6	M_HADDR	Master address bus width Read 0x1: 64-bit address Read 0x0: 32-bit address	R	1
5:3	S_HDATA	Slave Data Bus Width Read 0x3: 256-bit Read 0x2: 128-bit Read 0x1: 64-bit Read 0x0: 32-bit	R	0x0
2:0	M_HDATA	Master Data Bus Width Read 0x3: 256-bit Read 0x2: 128-bit Read 0x1: 64-bit Read 0x0: 32-bit	R	0x0

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Table 23-1452. Register Call Summary for Register SATA_GPARAM1R

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]

Table 23-1453. SATA_GPARAM2R

Address Offset	0x0000 00EC		
Physical Address	0x4A14 00EC	**Instance**	DWC_ahsata
Description	Global parameters register 2 Hardware configuration of the DWC AHCI SATA core, continued		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DEV_CP	DEV_MP	ENCODE_M	RXOOB_CLK_M	RX_OOB_M	TX_OOB_M	RXOOB_CLK									

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x0 0000
14	DEV_CP	Cold presence detection implemented in core Read 0x1: Yes Read 0x0: No	R	1
13	DEV_MP	Mechanical presence switch implemented in core Read 0x1: Yes Read 0x0: No	R	1
12	ENCODE_M	8b/10b Encoding/encoding implemented in core Read 0x1: Yes Read 0x0: No	R	1
11	RXOOB_CLK_M	RX OOB clocking mode: Read 0x1: RX OOB detection uses separate clock Read 0x0: Rx OOB detection uses RX clock	R	0
10	RX_OOB_M	RX OOB mode: sequence generation implemented Read 0x1: Yes Read 0x0: No	R	1
9	TX_OOB_M	TX OOB mode: sequence generation implemented Read 0x1: Yes Read 0x0: No	R	1
8:0	RXOOB_CLK	RX OOB clock frequency, in MHz	R	0x096

Table 23-1454. Register Call Summary for Register SATA_GPARAM2R

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]

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Table 23-1455. SATA_PPARAMR

Address Offset	0x0000 00F0		
Physical Address	0x4A14 00F0	**Instance**	DWC_ahsata
Description	Port parameter register Hardware configuration of the DWC AHCI SATA core port selected by SATA_TESTR.PSEL		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				TX_MEM_M	TX_MEM_S	RX_MEM_M	RX_MEM_S	TXFIFO_DEPTH				RXFIFO_DEPTH			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11	TX_MEM_M	TX FIFO memory mode: Read 0x1: Synchronous Read 0x0: Asynchronous	R	0
10	TX_MEM_S	TX FIFO memory selection: Read 0x1: Internal memory Read 0x0: External memory	R	0
9	RX_MEM_M	RX FIFO memory mode: Read 0x1: Synchronous Read 0x0: Asynchronous	R	0
8	RX_MEM_S	RX FIFO memory selection: Read 0x1: Internal memory Read 0x0: External memory	R	0
7:4	TXFIFO_DEPTH	Tx FIFO Depth, in dwords (log2) Read 0x3: 8 dwords Read 0x6: 64 dwords Read 0x4: 16 dwords Read 0x5: 32 dwords	R	0x6
3:0	RXFIFO_DEPTH	Rx FIFO Depth, in dwords (log2) Read 0x6: 64 dwords Read 0x7: 128 dwords Read 0x4: 16 dwords Read 0x5: 32 dwords	R	0x7

Table 23-1456. Register Call Summary for Register SATA_PPARAMR

SATA Controller

- DMA Port Configuration: [0]
- SATA Controller AHCI Hardware Register Interface: [1]
- DWC_ahsata Register Summary: [2]

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Table 23-1457. SATA_TESTR

Address Offset	0x0000 00F4		
Physical Address	0x4A14 00F4	**Instance**	DWC_ahsata
Description	Test register Puts the SATA controller slave interface in a test mode and selects a port for BIST operation		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PSEL			RESERVED															TEST_IF

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18:16	PSEL	Port select: Selects the port for BIST operation 0x0: Port 0 is selected	RW	0x0
15:1	RESERVED		R	0x0000
0	TEST_IF	Test interface 0x0: Normal mode: read-back value of some registers might not match the value written, depending on ongoing operations. 0x1: Test mode: Normal operation is disabled; read-back value of the registers match the value written. The following registers/fields can be accessed in this mode: - SATA_GHC.IE - SATA_BISTAFR.NCP and .PD bits become writable. - SATA_BISTCR.LLC .ERREN .FLIP .PV, and .PATTERN - SATA_BISTFCTR, SATA_BISTSR, SATA_BISTDECR become writeable. - SATA_PxCLB / SATA_PxCLBU, SATA_PxFB / SATA_PxFBU - SATA_PxIS.UFS and write-1-to-clear bits become writeable. - SATA_PxIE - SATA_PxCMD.ASP .ALPE .DLAE .ATAPI and .PMA - SATA_PxTFD, SATA_PxSIG become writeable. - SATA_PxSCTL - SATA_PxSERR (write-1-to-clear) bits become writeable. Notes: 1) Interrupt is asserted if any IS register bit is set after setting the corresponding SATA_PxIS and SATA_PxIE bits, and SATA_GHC.IE = 1. 2) SATA_CAP.SMPS/SSS, SATA_PI, SATA_PxCMD.ESP/CPD/MPSP/HPCP cannot be used in test mode. They are written once after POR and become read-only. 3) Global reset must be issued (SATA_GHC.HR=1) after the TEST_IF bit is cleared following the test mode operation.	RW	0

Table 23-1458. Register Call Summary for Register SATA_TESTR

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]
- DWC_ahsata Register Description: [2]

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Table 23-1459. SATA_VERSIONR

Address Offset	0x0000 00F8		
Physical Address	0x4A14 00F8	**Instance**	DWC_ahsata
Description	Version register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION1	See (1).	R	0x-(1)

(1) TI internal data

Table 23-1460. Register Call Summary for Register SATA_VERSIONR

SATA Controller

- DWC_ahsata Register Summary: [0]

Table 23-1461. SATA_IDR

Address Offset	0x0000 00FC		
Physical Address	0x4A14 00FC	**Instance**	DWC_ahsata
Description	ID register, containing the 32-bit Highlander (HL) revision.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	See (1).	R	0x-(1)

(1) TI internal data

Table 23-1462. Register Call Summary for Register SATA_IDR

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]

Table 23-1463. SATA_PxCLB

Address Offset	0x0000 0100		
Physical Address	0x4A14 0100	**Instance**	DWC_ahsata
Description	Port command ist base address 32-bit base physical address for the command list for this port. Used when fetching commands to execute. The structure pointed to by this address range is 1 KiB in length.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLB																						ZERO									

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Bits	Field Name	Description	Type	Reset
31:10	CLB	Command list base address (bits 31:10)	RW	0x00 0000
9:0	ZERO	Always 0 as address is 1 KiB-aligned	R	0x000

Table 23-1464. Register Call Summary for Register SATA_PxCLB

SATA Controller
- HBA Reset: [0]
- Command List Structure Basics: [1] [2]
- SATA Controller AHCI Hardware Register Interface: [3]
- Main Sequence SATA Controller Global Initialization: [4] [5] [6]
- DWC_ahsata Register Summary: [7]
- DWC_ahsata Register Description: [8]

Table 23-1465. SATA_PxCLBU

Address Offset	0x0000 0104		
Physical Address	0x4A14 0104	**Instance**	DWC_ahsata
Description	Port Command List Base Upper address Upper half of the 64-bit base physical address for the command list for this Port. Used when fetching commands to execute. Remains all 0 when in 32-bit mode. Reserved & read-only when CAP.S64A=0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLBU																															

Bits	Field Name	Description	Type	Reset
31:0	CLBU	Command List Base Upper Address (bits 63:32)(1)	RW	0x0000 0000

(1) Only bits [3:0] are meaningful , the others must be always written to '0'.

Table 23-1466. Register Call Summary for Register SATA_PxCLBU

SATA Controller
- HBA Reset: [0]
- Command List Structure Basics: [1] [2] [3] [4] [5]
- SATA Controller AHCI Hardware Register Interface: [6]
- Main Sequence SATA Controller Global Initialization: [7] [8] [9] [10]
- DWC_ahsata Register Summary: [11]
- DWC_ahsata Register Description: [12]

Table 23-1467. SATA_PxFB

Address Offset	0x0000 0108		
Physical Address	0x4A14 0108	**Instance**	DWC_ahsata
Description	Port Frame-information-structure Base address 32-bit base physical address for received FISes for this port. The structure pointed to by this address range is 256 bytes in length.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FB																								ZERO							

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Bits	Field Name	Description	Type	Reset
31:8	FB	FIS base address (bits 31:8)	RW	0x00 0000
7:0	ZERO	Always 0 as address is 256-bytes aligned	R	0x00

Table 23-1468. Register Call Summary for Register SATA_PxFB

SATA Controller

- HBA Reset: [0]
- Command List Structure Basics: [1] [2]
- Handling the Received FIS Descriptors: [3] [4]
- SATA Controller AHCI Hardware Register Interface: [5]
- Main Sequence SATA Controller Global Initialization: [6] [7] [8]
- DWC_ahsata Register Summary: [9]
- DWC_ahsata Register Description: [10] [11] [12]

Table 23-1469. SATA_PxFBU

Address Offset	0x0000 010C		
Physical Address	0x4A14 010C	**Instance**	DWC_ahsata
Description	FIS Base Upper Address Upper half of the 64-bit base physical address for received FISes for this port. Remains all 0 with a 32-bit SW driver. Reserved & read-only when CAP.S64A=0		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FBU																															

Bits	Field Name	Description	Type	Reset
31:0	FBU	FIS Base Upper Address (bits 63:32)[1]	RW	0x0000 0000

[1] Only bits [3:0] are meaningful , the others must be always written to '0'.

Table 23-1470. Register Call Summary for Register SATA_PxFBU

SATA Controller

- HBA Reset: [0]
- Command List Structure Basics: [1] [2] [3] [4] [5]
- Handling the Received FIS Descriptors: [6] [7]
- SATA Controller AHCI Hardware Register Interface: [8]
- Main Sequence SATA Controller Global Initialization: [9] [10] [11] [12]
- DWC_ahsata Register Summary: [13]
- DWC_ahsata Register Description: [14] [15] [16]

Table 23-1471. SATA_PxIS

Address Offset	0x0000 0110		
Physical Address	0x4A14 0110	**Instance**	DWC_ahsata
Description	Port interrupt status Bits are set by internal conditions and cleared (when possible) by writing 1 to them. Reset on global reset.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPDS	TFES	HBFS	HBDS	IFS	INFS	RESERVED	OFS	IPMS	PRCS	RESERVED														DMPS	PCS	DPS	UFS	SDBS	DSS	PSS	DHRS

Bits	Field Name	Description	Type	Reset
31	CPDS	Cold port detect status Set when the pX_cp_det input changes its state due to the insertion or removal of a device Valid only if the port supports cold presence detection as indicated by the SATA_PxCMD.CPD bit set to 1. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
30	TFES	Task file error status Set whenever the SATA_PxTFD.STS register is updated by the device and the error bit (bit 0) is set. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
29	HBFS	Host bus fatal error status Set when master (DMA) detects an ERROR response from the slave Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
28	HBDS	Host bus data error status This bit is always cleared to 0. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
27	IFS	Interface fatal error status This bit is set when any of the following conditions is detected: 1) SYNC escape is received from the device during H2D register or data FIS transmission. 2) One or more of the following errors are detected during data FIS transfer: - 10B to 8B Decode Error (SATA_PxSERR.DIAG_B) - Protocol (SATA_PxSERR.ERR_P) - CRC (SATA_PxSERR.DIAG_C) - Handshake (SATA_PxSERR.DIAG_H) - PHY not ready (SATA_PxSERR.ERR_C) 3) Unknown FIS is received with good CRC, but the length exceeds 64 bytes. 4) PRD table byte count is 0. 5) DMA setup FIS is received with a TAG corresponding to inactive (SATA_PxSACT bit is cleared) command slot. Port DMA transitions to a fatal state until the software clears SATA_PxCMD.ST bit or resets the interface by way of port reset or global reset. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
26	INFS	Interface nonfatal error status Set when any of the following conditions is detected: 1) One or more of the following errors are detected during nondata FIS transfer: - 10b to 8b decode error (SATA_PxSERR.DIAG_B) - Protocol (SATA_PxSERR.ERR_P) - CRC (SATA_PxSERR.DIAG_C) - Handshake (SATA_PxSERR.DIAG_H) - PHY not ready (SATA_PxSERR.ERR_C) 2) Command list underflow during read operation (that is, DMA read) when the software builds a command table that has more total bytes than the transaction given to the device. In both cases port operation continues normally. When an error is detected during nondata FIS transmission, this FIS is retransmitted continuously until it succeeds, or until the software times out and resets the interface. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
25	RESERVED		R	0
24	OFS	Overflow status Set when command list overflow is detected during read or write operation when the software builds command table that has fever total bytes than the transaction given to the device. Port DMA transitions to a fatal state until the software clears SATA_PxCMD.ST bit or resets the interface by way of port reset or global reset. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0

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Bits	Field Name	Description	Type	Reset
23	IPMS	Incorrect PM status FIS received from a device in which the PM field did not match what was expected May be set during enumeration of devices on a PM due to the normal PM enumeration process Must be used only after enumeration is complete on the PM Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
22	PRCS	PhyRdy change status Reflects the state of SATA_PxSERR.DIAG_N To clear this bit, clear the SATA_PxSERR.DIAG_N bit to 0. Read 0x1: Internal pX_phy_ready signal changed state Read 0x0: Internal pX_phy_ready signal has not changed state since its last reset.	R	0
21:8	RESERVED		R	0x0000
7	DMPS	Device mechanical presence status Set when the pX_mp_switch input changes its state as a result of a mechanical switch attached to this port opening or closing Valid only when SATA_CAP.SMPS and SATA_PxCMD.MPSP are set Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
6	PCS	Port connect change status This bit reflects the state of the SATA_PxSERR.DIAG_X bit. Cleared only when SATA_PxSERR.DIAG_X is cleared Read 0x1: Change in current connect status Read 0x0: No change in current connect status	R	0
5	DPS	Descriptor processed A PRD with the I bit set has transferred all of its data. Note. This is an opportunistic interrupt and must not be used to definitively indicate the end of a transfer. Two PRD interrupts could occur close enough together that the second interrupt is missed when the first PRD interrupt is cleared. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
4	UFS	Unknown FIS interrupt An unknown FIS was received and has been copied into system memory. Cleared to 0 by the software clearing the SATA_PxSERR.DIAG_F bit to 0. Note: The UFS bit does not directly reflect the SATA_PxSERR.DIAG_F bit. SATA_PxSERR.DIAG_F bit is set immediately when an unknown FIS is detected, whereas the UFS bit is set when that FIS is posted to memory. The software should wait to act on an unknown FIS until the UFS bit is set to 1 or the two bits may become out of sync. Read 0x1: IRQ event active Read 0x0: Event inactive	R	0

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Bits	Field Name	Description	Type	Reset
3	SDBS	Set device bits interrupt A Set Device Bits FIS is received with the I bit set and copied into system memory. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
2	DSS	DMA setup FIS interrupt A DMA Setup FIS is received with the I bit set and copied into system memory. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
1	PSS	PIO setup FIS interrupt A PIO Setup FIS is received with the I bit set, copied into system memory, and the data related to the FIS is transferred. Note: This bit is set even when the data transfer resulted in an error. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0
0	DHRS	Device to host register FIS interrupt A D2H register FIS is received with the I bit set and copied into system memory. Write 0x0: No action Write 0x1: Clear event Read 0x1: IRQ event active Read 0x0: Event inactive	RW W1toClr	0

Table 23-1472. Register Call Summary for Register SATA_PxIS

SATA Controller

- Levels of Interrupt Control: [0] [1]
- Interrupt Events Description: [2]
- PHYReady Change Status: [3]
- Descriptor Processed: [4]
- Interrupt Condition Control: [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18]
- SATA Controller AHCI Hardware Register Interface: [19]
- Receive FIS—Main Sequence: [20]
- DWC_ahsata Register Summary: [21]
- DWC_ahsata Register Description: [22] [23] [24] [25] [26] [27]

Table 23-1473. SATA_PxIE

Address Offset	0x0000 0114		
Physical Address	0x4A14 0114	**Instance**	DWC_ahsata
Description	Port interrupt enable Enables and disables the reporting of the corresponding interrupt to system software When a bit is set (1), SATA_GHC.IE = 1, and the corresponding interrupt condition in SATA_PxIS is active, then the SATA controller interrupt output is asserted. When a bit is cleared (0), interrupt sources are still reflected in the status registers. Reset on global reset		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPDE	TFEE	HBFE	HBDE	IFE	INFE	RESERVED	OFE	IPME	PRCE	RESERVED														DMPE	PCE	DPE	UFE	SDBE	DSE	PSE	DHRE

Bits	Field Name	Description	Type	Reset
31	CPDE	Cold port detect enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
30	TFEE	Task file error enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
29	HBFE	Host bus fatal error enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
28	HBDE	Host bus data error enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
27	IFE	Interface fatal error enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
26	INFE	Interface on fatal error enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
25	RESERVED		R	0
24	OFE	Overflow enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
23	IPME	Incorrect PM enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
22	PRCE	PhyRdy change enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
21:8	RESERVED		R	0x0000
7	DMPE	Device mechanical presence enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
6	PCE	Port connect change enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
5	DPE	Descriptor processed interrupt enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
4	UFE	Unknown FIS interrupt enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0

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Bits	Field Name	Description	Type	Reset
3	SDBE	Set device bits interrupt enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
2	DSE	DMA setup FIS interrupt enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
1	PSE	PIO setup FIS interrupt enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0
0	DHRE	Device to host register FIS interrupt enable 0x0: Interrupt disabled 0x1: Interrupt enabled	RW	0

Table 23-1474. Register Call Summary for Register SATA_PxIE

SATA Controller

- Interrupt Events Description: [0]
- Interrupt Condition Control: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16]
- SATA Controller AHCI Hardware Register Interface: [17]
- DWC_ahsata Register Summary: [18]
- DWC_ahsata Register Description: [19] [20] [21]

Table 23-1475. SATA_PxCMD

Address Offset	0x0000 0118		
Physical Address	0x4A14 0118	**Instance**	DWC_ahsata
Description	Port command		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICC				ASP	ALPE	DLAE	ATAPI	ATPSE	RESERVED	ESP	CPD	MPSP	HPCP	PMA	CPS	CR	FR	MPSS	CCS					RESERVED			FRE	CLO	POD	SUD	ST

Bits	Field Name	Description	Type	Reset
31:28	ICC	Interface communication control Control of power management states of the interface If the link layer is in the L_IDLE state, writes cause the port to request a transition to a given interface state. If the link layer is not in the L_IDLE state, writes have no effect. When a nonreserved, non-0 (No-Op) value is written, the core performs the action and clears the field back to 0 (Idle) Write 0x0: No-Op 0x6: SLUMBER. SATA device can reject the request and the interface then remains in its current state. 0x1: Active Read 0x0: Port is ready to accept a new interface control command, although the transition to the previously selected state might not have occurred yet. 0x2: PARTIAL. SATA device can reject the request and the interface then remains in its current state.	RW	0x0

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Bits	Field Name	Description	Type	Reset
27	ASP	Aggressive SLUMBER/PARTIAL 0x0: If SATA_PxCMD.ALPE = 1, the port aggressively enters the PARTIAL state when it clears the SATA_PxCI register and the SATA_PxSACT register is cleared when it clears the SATA_PxSACT register and SATA_PxCI is cleared. 0x1: If SATA_PxCMD.ALPE = 1, the port aggressively enters the SLUMBER state when it clears the SATA_PxCI and the SATA_PxSACT register is cleared or when it clears the SATA_PxSACT register and SATA_PxCI is cleared.	RW	0
26	ALPE	Aggressive link power management enable 0x0: Aggressive power management state transition is disabled. 0x1: Port aggressively enters a lower link power state (PARTIAL or SLUMBER) based on the setting of SATA_PxCMD.ASP.	RW	0
25	DLAE	Drive LED on ATAPI enable 0x0: LED is never enabled. 0x1: Port asserts the pX_act_led output when commands are active and SATA_PxCMD.ATAPI = 1.	RW	0
24	ATAPI	Device is ATAPI Used by the port to determine whether or not to assert pX_act_led output when commands are active. 0x0: Connected device is not an ATAPI. 0x1: Connected device is an ATAPI.	RW	0
23	ATPSE	Auto PARTIAL to SLUMBER 0x0: No automatic transition from PARTIAL to SLUMBER 0x1: Link layer transitions from its PARTIAL power management state to SLUMBER state automatically, whether host software-, port (aggressive)-, or device-initiated.	RW	0
22	RESERVED		R	0x0
21	ESP	External SATA port Writable once after power up, read-only afterward 0x0: Port signal-only connector is not externally accessible. 0x1: Port signal-only connector is externally accessible. SATA_CAP.SXS is also set to 1. Mutually exclusive with SATA_PxCMD.HPCP	RW	0x0
20	CPD	Cold presence detect Writable once after power up, read-only afterward 0x0: Platform does not support cold presence detection on this port. 0x1: Platform supports cold presence detection on this port. SATA_PxCMD.HPCP should be set to 1.	RW	0
19	MPSP	Mechanical presence switch attached to port Writable once after power up, read-only afterward 0x0: Platform does not support a mechanical presence switch on this port. 0x1: Platform supports a mechanical presence switch attached to this port. SATA_PxCMD.HPCP should be set to 1.	RW	0

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Bits	Field Name	Description	Type	Reset
18	HPCP	Hot plug capable port Writable once after power up, read-only afterward 0x0: Port signal and power connectors are not externally accessible. 0x1: Port signal and power connectors are externally accessible through a joint signal-power connector for blindmate device hot plug.	RW	0
17	PMA	PM attached Software is responsible for detecting the presence of a PM. There is no autodetection. 0x0: No PM is attached to this port. 0x1: PM is attached to this port.	RW	0
16	CPS	Cold presence state Reports whether a device is currently detected on this port as indicated by the pX_cp_det input state (assuming SATA_PxCMD.CPD = 1). Read 0x1: Device detected Read 0x0: No device detected	R	0
15	CR	Command list running For details, see the AHCI state-machine in Section 5.3.2 of the AHCI specification. Read 0x1: Command list DMA engine for this port is running. Read 0x0: Command list is stopped for this port.	R	0
14	FR	FIS receive running For details, see Section 10.3.2 of the AHCI specification. Read 0x1: FIS receive DMA engine for the port is running. Read 0x0: FIS receive DMA engine for the port is stopped.	R	0
13	MPSS	Mechanical presence switch state Reports the state of a mechanical presence switch attached to this port as indicated by the pX_mp_switch input state (assuming SATA_CAP.SMPS = 1 and SATA_PxCMD.MPSP = 1) Cleared to 0 when SATA_CAP.SMPS = 0 Read 0x1: Switch is open. Read 0x0: Switch is closed.	R	0
12:8	CCS	Current command slot This field is valid when SATA_PxCMD.ST is set to 1 and is set to the command slot value of the command currently issued by the port. When SATA_PxCMD.ST transitions from 1 to 0, this field is reset to 0x00. After SATA_PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command is issued, the highest priority slot to issue from next is SATA_PxCMD.CCS + 1. For example, after the port issues its first command, if CCS = 0x00 and SATA_PxCI is set to 0x3, the next command issued is from command slot 1.	R	0x00
7:5	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
4	FRE	FIS receive enable Must not be set until SATA_PxFB / SATA_PxFBU is programmed with a valid pointer to the FIS receive area Base can be moved after clearing FRE and waiting for FR to clear to 0. 0x0: Received FISes are not accepted by the port, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. 0x1: Port can post received FISes into the FIS receive area pointed to by SATA_PxFB and SATA_PxFBU.	RW	0
3	CLO	Command list override Write 0x0: No effect Write 0x1: Request to clear SATA_PxTFD.STS_BSY and SATA_PxTFD.STS_DRQ to 0. Use only immediately prior to setting SATA_PxCMD.ST bit to 1 from a previous value of 0. Any other case results in indeterminate behavior. Read 0x1: Override is active, SATA_PxTFD.STS_BSY and SATA_PxTFD.STS_DRQ are being cleared. Read 0x0: Override is inactive.	RW	0
2	POD	Power-on device Writable if SATA_PxCMD.CPD = 1 (cold presence detection enabled), otherwise read-only -1. 0x0: Disabled 0x1: Port asserts the pX_cp_pod output pin so that it can be used to provide power to a cold-presence detectable port.	RW	0
1	SUD	Spin-up device Writable if SATA_CAP.SSS = 1 (staggered spin-up supported), else read-only 1. Read-only-0 on power-up until SATA_CAP.SSS bit is written with the required value. 0x0: Clearing the bit from 1 to 0 causes no action on the interface. 0x1: On edge-detect from 0 to 1, the port starts a COMRESET initialization sequence to the device.	RW	0
0	ST	Start 0x0: Port does not process the command list. On transition from 1 to 0, the SATA_PxCI register is cleared by the port on transition to an IDLE state. 0x1: Port processes the command list. On transition from 0 to 1, the port starts processing the command list at entry 0. SATA_PxSERR must be cleared prior to setting ST to 1. For important restrictions on when ST can be set to 1, See Section 10.3.1 of the AHCI specification.	RW	0

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Table 23-1476. Register Call Summary for Register SATA_PxCMD

SATA Controller

- Software Control over Low Power States: [0]
- Aggressive Power Management: [1] [2]
- Interface Fatal Error Status: [3]
- Overflow Status: [4]
- Software Processing of the Port Command List: [5] [6] [7] [8] [9] [10]
- Handling the Received FIS Descriptors: [11] [12] [13] [14]
- Activity LED Generation Functionality: [15] [16] [17]
- SATA Controller AHCI Hardware Register Interface: [18]
- Main Sequence SATA Controller Global Initialization: [19] [20] [21]
- SubSequence – Firmware Capability Writes: [22] [23] [24] [25] [26] [27]
- Issue Command - Main Sequence: [28] [29]
- DWC_ahsata Register Summary: [30]
- DWC_ahsata Register Description: [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58] [59] [60]

Table 23-1477. SATA_PxTFD

Address Offset	0x0000 0120		
Physical Address	0x4A14 0120	**Instance**	DWC_ahsata
Description	Port Task File Data: copies specific fields of the task file when FISes are received		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERR								STS_BSY	STS_CS2			STS_DRQ	STS_CS		STS_ERR

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	ERR	Err: Latest copy of the task file error register	R	0x00
7	STS_BSY	Status, busy Latest copy of the 8-bit task file status register, bit 7 STS_BSY = Interface is busy	R	0
6:4	STS_CS2	Status, command-specific Latest copy of the 8-bit task file status register, bits 6:4	R	0x7
3	STS_DRQ	Status, data request Latest copy of the 8-bit task file status register, bit 3 STS_DRQ = Data transfer is requested	R	1
2:1	STS_CS	Status, command-specific Latest copy of the 8-bit task file status register, bits 2:1	R	0x3
0	STS_ERR	Status, error Latest copy of the 8-bit task file status register, bit 0 STS_ERR = Error during the transfer	R	1

Table 23-1478. Register Call Summary for Register SATA_PxTFD

SATA Controller

- Task File Error Status: [0] [1] [2]
- Software Processing of the Port Command List: [3]
- SATA Controller AHCI Hardware Register Interface: [4]
- DWC_ahsata Register Summary: [5]
- DWC_ahsata Register Description: [6] [7] [8] [9] [10] [11]

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Table 23-1479. SATA_PxSIG

Address Offset	0x0000 0124		
Physical Address	0x4A14 0124	**Instance**	DWC_ahsata
Description	Port signature: Signature received from a device on the first D2H register FIS. Updated once after a reset sequence.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIG_LBAH								SIG_LBAM								SIG_LBAL								SIG_SCR							

Bits	Field Name	Description	Type	Reset
31:24	SIG_LBAH	Signature, LBA high (cylinder high) register	R	0xFF
23:16	SIG_LBAM	Signature, LBA mid (cylinder low) register	R	0xFF
15:8	SIG_LBAL	Signature, LBA low (sector number) register	R	0xFF
7:0	SIG_SCR	Signature, sector count register	R	0xFF

Table 23-1480. Register Call Summary for Register SATA_PxSIG

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]
- DWC_ahsata Register Description: [2]

Table 23-1481. SATA_PxSSTS

Address Offset	0x0000 0128		
Physical Address	0x4A14 0128	**Instance**	DWC_ahsata
Description	Port SATA status Current state of the interface and host, updated continuously and asynchronously. When the port transmits a COMRESET to the device, this register is updated to its reset values (that is, global reset, port reset, or COMINIT from the device).		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				IPM				SPD				DET			

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11:8	IPM	Interface power management: Current interface state Read 0x2: Interface in PARTIAL power management state Read 0x1: Interface in ACTIVE state Read 0x0: Device not present or communication not established Read 0x6: Interface in SLUMBER power management state	R	0x0

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Bits	Field Name	Description	Type	Reset
7:4	SPD	Current interface speed: Negotiated interface communication speed Read 0x3: Generation 3 communication rate negotiated (6 Gbps) Read 0x2: Generation 2 communication rate negotiated (3 Gbps) Read 0x1: Generation 1 communication rate negotiated (1.5 Gbps) Read 0x0: Device not present or communication not established	R	0x0
3:0	DET	Device detection: Interface device detection and PHY state Read 0x3: Device presence detected and PHY communication established Read 0x1: Device presence detected but PHY communication not established Read 0x0: No device detected and PHY communication not established Read 0x4: PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode	R	0x0

Table 23-1482. Register Call Summary for Register SATA_PxSSTS

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]

Table 23-1483. SATA_PxSCTL

Address Offset 0x0000 012C

Physical Address 0x4A14 012C **Instance** DWC_ahsata

Description Port SATA control
Control of SATA interface capabilities. Writes to this register result in action taken by the port PHY interface. Reads from the register return the last value written to it. Reset on global reset.
Wait for at least seven periods of the slower clock (OCP or parallel serdes clock) between writes, due to the internal clock domain crossing between the transport (OCP) and link (serdes I/F) layers.

Type RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PMP				SPM				IPM				SPD				DET			

Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19:16	PMP	PM port: This field is not used by the AHCI.	R	0x0
15:12	SPM	Select power management: This field is not used by the AHCI.	R	0x0

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Bits	Field Name	Description	Type	Reset
11:8	IPM	Interface power management transitions allowed: Indicates which power states the HBA is allowed to transition to. If an interface power management state is disabled, the HBA is not allowed to initiate that state and the HBA must PMNAK_P any request from the device to enter that state. The two MSBs are always 2'b00 (not writable), as for all unreserved field values. 0x0: No interface power management state restrictions 0x1: Transitions to the PARTIAL state disabled 0x3: Transitions to both PARTIAL and SLUMBER states disabled 0x2: Transitions to the SLUMBER state disabled	RW	0x0
7:4	SPD	Speed allowed: Highest allowable speed of the interface The two MSBs are always 2'b00 (not writable), as for all unreserved field values. 0x0: No speed negotiation restrictions 0x1: Limit speed negotiation to generation 1 communication rate. 0x2: Limit speed negotiation to a rate not greater than generation 2 communication rate.	RW	0x0
3:0	DET	Device detection initialization: Controls the HBA device detection and interface initialization. Can be modified only when SATA_PxCMD.ST = 0. Must have a value of 0x0 when SATA_PxCMD.ST = 1. MSB is always 1'b0 (not writable), as for all unreserved field values. 0x0: No device detection or initialization action requested 0x1: Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is transmitted on the interface. Software must leave the DET field set to 1h for a minimum of 1 ms to ensure that a COMRESET is sent on the interface. 0x4: Disable the serial ATA interface and put PHY in offline mode.	RW	0x0

Table 23-1484. Register Call Summary for Register SATA_PxSCTL

SATA Controller

- Port Reset: [0]
- SATA Controller AHCI Hardware Register Interface: [1]
- Main Sequence SATA Controller Global Initialization: [2]
- DWC_ahsata Register Summary: [3]
- DWC_ahsata Register Description: [4] [5] [6] [7]

Table 23-1485. SATA_PxSERR

Address Offset	0x0000 0130		
Physical Address	0x4A14 0130	**Instance**	DWC_ahsata
Description	Port SATA error Detected interface errors accumulated since the last time it cleared. When set, indicates that the corresponding error condition became true one or more times since the last time cleared. Write 1 to a bit to clear it. Cleared by global reset or port reset (COMRESET).		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					DIAG_X	DIAG_F	DIAG_T	DIAG_S	DIAG_H	DIAG_C	DIAG_D	DIAG_B	DIAG_W	DIAG_I	DIAG_N	RESERVED				ERR_E	ERR_P	ERR_C	ERR_T	RESERVED						ERR_M	ERR_I

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	DIAG_X	Exchanged: PHY COMINIT signal detected. Reflected in SATA_PxIS.PCS.	RW W1toClr	0
25	DIAG_F	Unknown FIS type: One or more FISes were received by the transport layer with good CRC, but had a type field that was not recognized/known and the length was = 64 bytes. Note: If the unknown FIS length exceeds 64 bytes, DIAG_F is not set and DIAG_T is set instead.	RW W1toClr	0
24	DIAG_T	Transport state transition error: Transport Layer protocol violation detected.	RW W1toClr	0
23	DIAG_S	Link sequence error: One or more Link state machine error conditions encountered, including device doing SYNC escape during FIS transmission.	RW W1toClr	0
22	DIAG_H	Handshake error: One or more R-ERRp received in response to frame transmission. May be the result of a CRC error detected by the device, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.	RW W1toClr	0
21	DIAG_C	CRC error: One ore more CRC errors detected by the link layer during FIS reception.	RW W1toClr	0
20	DIAG_D	Disparity error: Not used by AHCI, always 0.	R	0
19	DIAG_B	10bit-to-8bit decode error: Errors detected by the 10b8b decoder. Note: Set only when an error is detected on the received FIS data word. Not set when an error is detected on the primitive, regardless of whether it is inside or outside the FIS.	RW W1toClr	0
18	DIAG_W	Comm wake: Comm wake signal detected by the PHY.	RW W1toClr	0
17	DIAG_I	PHY internal error: Internal error detected by the PHY. Note: If the PHY does not support any errors, this bit is never set.	RW W1toClr	0
16	DIAG_N	PhyRdy change: Indicates that the PHY Ready signal changed state. Reflected in SATA_PxIS.PRCS.	RW W1toClr	0
15:12	RESERVED		R	0x0
11	ERR_E	Internal error: One or more errors detected on the master (DMA) or the slave (MMR access) interfaces.	RW W1toClr	0
10	ERR_P	Protocol error: Any of the following conditions: - Transport state transition error (DIAG_T) - Link sequence error (DIAG_S) - RxFIFO overflow - Link bad end error (WTRM instead of EOF received)	RW W1toClr	0
9	ERR_C	Nonrecovered persistent communication error: PHY Ready signal is negated due to loss of communication with the device or problems with the interface, but not after transition from ACTIVE to PARTIAL or SLUMBER power management state.	RW W1toClr	0
8	ERR_T	Nonrecovered transient data integrity error: Any of the following conditions are set during data FIS transfer: - ERR_P (Protocol) - DIAG_C (CRC) - DIAG_H (Handshake) - ERR_C (PHY Ready negation)	RW W1toClr	0
7:2	RESERVED		R	0x00

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Bits	Field Name	Description	Type	Reset
1	ERR_M	Recovered communication error: PHY Ready condition is detected after interface initialization, but not after transition from PARTIAL or SLUMBER power management state to ACTIVE state.	RW W1toClr	0
0	ERR_I	Recovered data integrity error: Any of the following conditions are set during non-data FIS transfer: - ERR_P (Protocol) - DIAG_C (CRC) - DIAG_H (Handshake) - ERR_C (PHY Ready negation)	RW W1toClr	0

Table 23-1486. Register Call Summary for Register SATA_PxSERR

SATA Controller

- PHYReady Change Status: [0]
- Port Connect Change Status: [1]
- SATA Controller AHCI Hardware Register Interface: [2]
- DWC_ahsata Register Summary: [3]
- DWC_ahsata Register Description: [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23]

Table 23-1487. SATA_PxSACT

Address Offset	0x0000 0134		
Physical Address	0x4A14 0134	**Instance**	DWC_ahsata
Description	Port SATA active (SActive): Indicates which command slots contain commands.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DS																															

Bits	Field Name	Description	Type	Reset
31:0	DS	Device status: Field is bit-significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. Set by Software prior to issuing a native queued command for a particular command slot. Prior to writing SATA_PxCI[TAG] to 1, software sets DS[TAG] to 1 to indicate that a command with that TAG is outstanding. The device clears bits by sending a set device bits FIS to the port. The port clears bits in this field that are set to 1 in the SActive field of the set device bits FIS. The port only clears bits that correspond to native queued commands completed successfully. Write only when SATA_PxCMD.ST bit is set to 1. Cleared when SATA_PxCMD.ST is written from 1 to 0. Not cleared by a port reset (COMRESET) or a software reset.	RW	0x0000 0000

Table 23-1488. Register Call Summary for Register SATA_PxSACT

SATA Controller

- Supported Types of Commands: [0]
- Software Processing of the Port Command List: [1] [2]
- Activity LED Generation Functionality: [3] [4] [5]
- SATA Controller AHCI Hardware Register Interface: [6]
- Issue Command - Main Sequence: [7] [8]
- DWC_ahsata Register Summary: [9]
- DWC_ahsata Register Description: [10] [11] [12] [13] [14]

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Table 23-1489. SATA_PxCI

Address Offset	0x0000 0138		
Physical Address	0x4A14 0138	**Instance**	DWC_ahsata
Description	Port command issue: Indicates that a command is constructed and may be carried out.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CI																															

Bits	Field Name	Description	Type	Reset
31:0	CI	Commands issue: Field is bit-significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by software to indicate to the port that a command is built in system memory for a command slot and may be sent to the device. When the port receives a FIS that clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field can only be set to 1 by software when SATA_PxCMD.ST is set to 1. Also cleared when SATA_PxCMD.ST is written from 1 to 0 by software.	RW	0x0000 0000

Table 23-1490. Register Call Summary for Register SATA_PxCI

SATA Controller

- Software Processing of the Port Command List: [0] [1] [2] [3] [4]
- Activity LED Generation Functionality: [5] [6] [7]
- SATA Controller AHCI Hardware Register Interface: [8]
- Issue Command - Main Sequence: [9] [10] [11] [12]
- DWC_ahsata Register Summary: [13]
- DWC_ahsata Register Description: [14] [15] [16] [17] [18] [19] [20]

Table 23-1491. SATA_PxSNTF

Address Offset	0x0000 013C		
Physical Address	0x4A14 013C	**Instance**	DWC_ahsata
Description	Port SATA notification: Used to determine if asynchronous notification events have occurred for directly connected devices and devices connected to a PM.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PMN															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	PMN	PM notify: Indicates whether a particular device with the corresponding PM port number issued a set device bits FIS to the SATA controller Port with the notification bit set: - PM Port 0h sets bit 0. - PM Port 0h sets bit 1. - etc. Write 1 to a bit to clear it. Reset on global reset but not on port reset (COMRESET) or software reset.	RW W1toClr	0x0000

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Table 23-1492. Register Call Summary for Register SATA_PxSNTF

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- DWC_ahsata Register Summary: [1]
- DWC_ahsata Register Description: [2]

Table 23-1493. SATA_PxDMACR

Address Offset	0x0000 0170		
Physical Address	0x4A14 0170	**Instance**	DWC_ahsata
Description	Port DMA control register. Not AHCI-standard. Writable only when SATA_PxCMD.ST = 0. Attempts to write a field value less than the minimum or more than the maximum cause the field to be set to the minimum or the maximum. Reset on global reset and port reset (COMRESET)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RXTS				TXTS			

Bits	Field Name	Description	Type	Reset
31:8	RESERVED		R	0x00 0000
7:4	RXTS	Receive transaction size: DMA transaction size for receive operations (system bus write, device read). 0x0: 1 dword 0x1: 2 dwords 0x2: 4 dwords 0x3: 8 dwords 0x4: 16 dwords 0x5: 32 dwords 0x6: 64 dwords; maximum value for the 128-dword RX FIFO of this implementation.	RW	0x6
3:0	TXTS	Transmit transaction size: DMA transaction size for transmit operations (system bus read, device write). 0x0: 1 dword 0x1: 2 dwords 0x2: 4 dwords 0x3: 8 dwords 0x4: 16 dwords 0x5: 32 dwords; maximum value for this implementation.	RW	0x5

Table 23-1494. Register Call Summary for Register SATA_PxDMACR

SATA Controller

- DMA Port Configuration: [0] [1] [2] [3] [4]
- SATA Controller AHCI Hardware Register Interface: [5]
- Main Sequence SATA Controller Global Initialization: [6]
- DWC_ahsata Register Summary: [7]

23.12.6.3 SATAMAC_wrapper Registers

23.12.6.3.1 SATAMAC_wrapper Register Summary

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Table 23-1495. SATAMAC_wrapper Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address (L4 Interconnect)
SATA_SYSCONFIG	RW	32	0x0000 0000	0x4A14 1100
SATA_CDRLOCK	RW	32	0x0000 0004	0x4A14 1104

23.12.6.3.2 SATAMAC_wrapper Register Description

Table 23-1496. SATA_SYSCONFIG

Address Offset	0x0000 0000		
Physical Address	0x4A14 1100	**Instance**	SATAMAC_wrapper
Description	This register controls the idle and standby modes of Highlander 08 modules.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															OVERRIDE0	RESERVED								STANDBYMODE		IDLEMODE		RESERVED			

Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	OVERRIDE0	Override for clock stopping. Normally the functional clock can be stopped only if the link is put into PARTIAL or SLUMBER power state. However, if there is no device attached (such as in a removable media situation) or the device is not started, the user can stop the functional clocks but not be able to enter a low-power state. In this case, software can set the OVERRIDE bit to 1, removing the requirement for a low-power state WARNING: If there is a device attached, the OVERRIDE bit is used, and the functional clock is stopped when the link is not in a low-power state it ruins the link and causes undetermined behavior. A port reset or full SATASS reset might be required to recover. 0x0: Normal mode 0x1: Override mode	RW	0
15:6	RESERVED		R	0x000

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Bits	Field Name	Description	Type	Reset
5:4	STANDBYMODE	Configuration of the local initiator-state management mode. By definition, the initiator can generate a read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: Local initiator is unconditionally placed in STANDBY state. Backup mode, for debug only 0x1: No-standby mode: local initiator is unconditionally placed out of STANDBY state. Backup mode, for debug only. 0x3: Smart-Standby wakeup-capable mode: Local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. The IP module can generate (master related) wakeup events when in STANDBY state. Mode is relevant only if the appropriate IP module mwakeup output is implemented. 0x2: Smart-standby mode: Local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. The IP module does not generate (initiated-related) wakeup events.	RW	0x2
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, the target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: The local target IDLE state follows (acknowledges) the system idle requests unconditionally, that is, regardless of the internal requirements of th e IP module. Backup mode, for debug only. 0x1: No-idle mode: The local target never enters IDLE state. Backup mode, for debug only. 0x3: Smart-idle wakeup-capable mode: The local target IDLE state eventually follows (acknowledges) the system idle requests, depending on the internal requirements of the IP module. IP module can generate (IRQ- or DMA-request-related) wakeup events when in IDLE state. Mode is only relevant if the appropriate IP module swakeup output(s) is (are) implemented. 0x2: Smart-idle mode: The local target IDLE state eventually follows (acknowledges) the system idle requests, depending on the internal requirements of the IP module. IP module does not generate (IRQ- or DMA-request-related) wakeup events.	RW	0x2
1:0	RESERVED		R	0x0

Table 23-1497. Register Call Summary for Register SATA_SYSCONFIG

SATA Controller

- Idle/Standby Management Protocol: [0] [1] [2] [3] [4]
- Clock Gating Synchronization: [5] [6] [7] [8] [9]
- SATA Controller AHCI Hardware Register Interface: [10]
- SATAMAC_wrapper Register Summary: [11]

Table 23-1498. SATA_CDRLOCK

Address Offset	0x0000 0004		
Physical Address	0x4A14 1104	**Instance**	SATAMAC_wrapper
Description	Programmable delay for CDR lock indication		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				CDR_LOCK_DELAY											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0 0000
11:0	CDR_LOCK_DELAY[(1)]	CDR lock delay, in parallel (10-bit) serdes interface clock cycles. Parallel clock is 300 MHz (3.3 ns period) for SATA-3 Gbps, 150 MHz (6.7 ns) for SATA-1.5 Gbps. 0x0: No CDR lock delay 0x7D0: Default CDR lock delay: 13.33 us (1.5 Gbps mode) or 6.67 us (3 Gbps mode)	RW	0x7D0

(1) Under normal conditions, this bitfield must be kept at its default (power-on-reset) value.

Table 23-1499. Register Call Summary for Register SATA_CDRLOCK

SATA Controller

- SATA Controller AHCI Hardware Register Interface: [0]
- SATAMAC_wrapper Register Summary: [1]

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MMC/SDIO

This chapter describes the features and functions of the multimedia card (MMC/SDIO) interface of the device.

NOTE: Some of the MMC/SDIO interfaces are not available in all OMAP54xx devices.

For details, see Section 1.5, *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

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24.1 MMC/SDIO Overview

The multimedia card high-speed/SDIO (MMC/SDIO) host controller provides an interface between a local host (LH) such as a microprocessor unit (MPU) or digital signal processor (DSP) and either MMC, SD® memory cards, or SDIO cards and handles MMC/SDIO transactions with minimal LH intervention.

Optionally, the controller is connected to the level 3 (L3_MAIN) interconnect to have a direct access to system memory. It also supports two direct memory access (DMA) slave channels or a DMA master access (in this case, slave DMA channels are deactivated) depending on its integration. These controllers are embedded MMC/SD (eMMC/SD) controllers.

The application interface manages transaction semantics. The MMC/SDIO host controller deals with MMC/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit, and checking for syntactical correctness.

The application interface can send every MMC/SDIO command and poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn of end of operation.

The application interface can read card responses or flag registers. It can also mask individual interrupt sources. All these operations can be performed by reading and writing control registers. The MMC/SDIO host controller also supports two DMA channels.

There are five MMC/SDIO host controllers inside the device:

Figure 24-1 gives an overview of the MMC/SDIO1 controller instance MMC1 (SD card).

Figure 24-2 gives an overview of the MMC/SDIO2 controller instance MMC2 (eMMC).

Figure 24-3 gives an overview of the MMC/SDIO3 controller instance MMC3 (WLAN SDIO).

Figure 24-4 gives an overview of the MMC/SDIO4 and MMC/SDIO5 controller instances (generic SDIO controllers).

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Figure 24-1. MMC/SDIO1 Overview

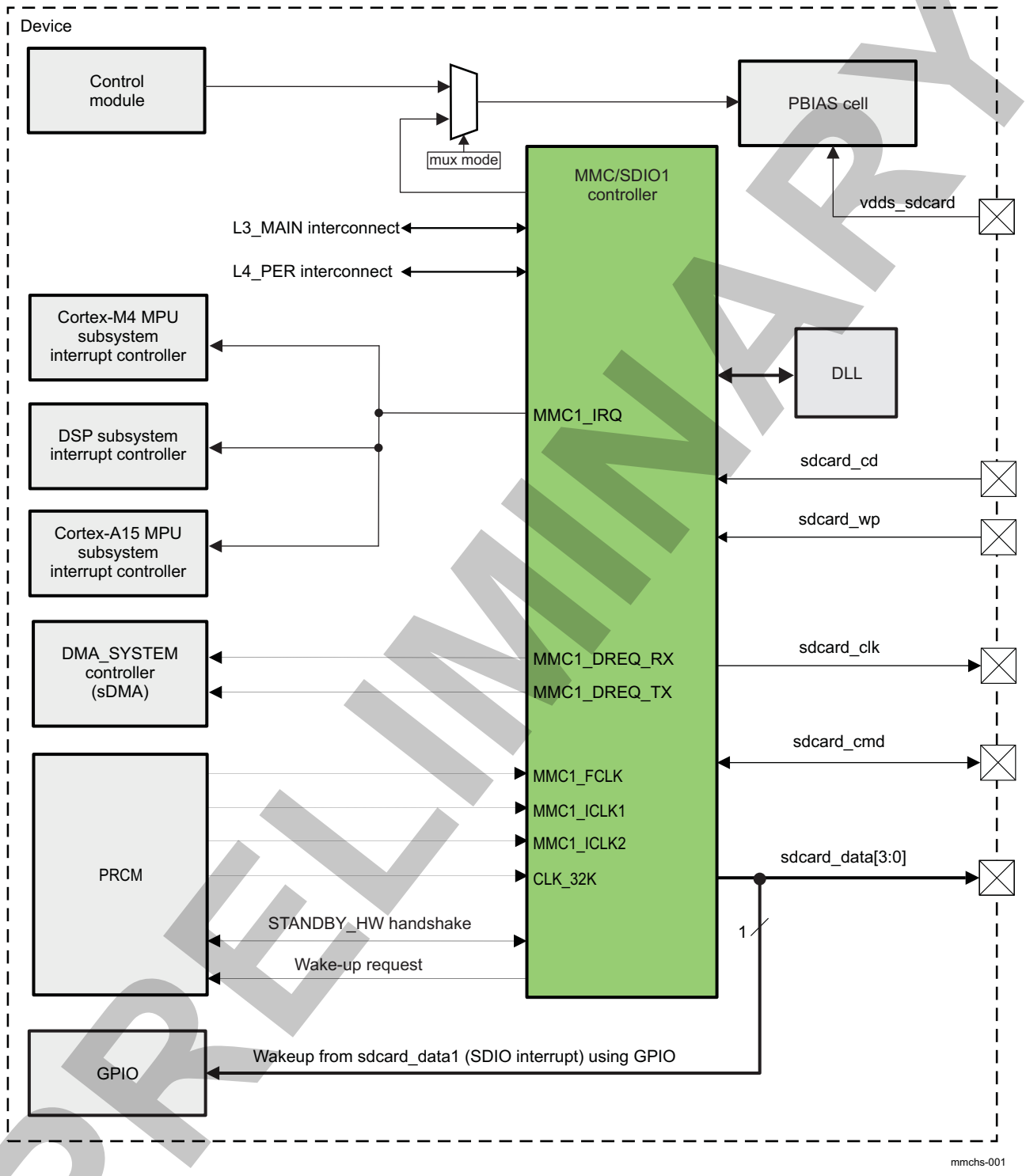

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Figure 24-2. MMC/SDIO2 Overview

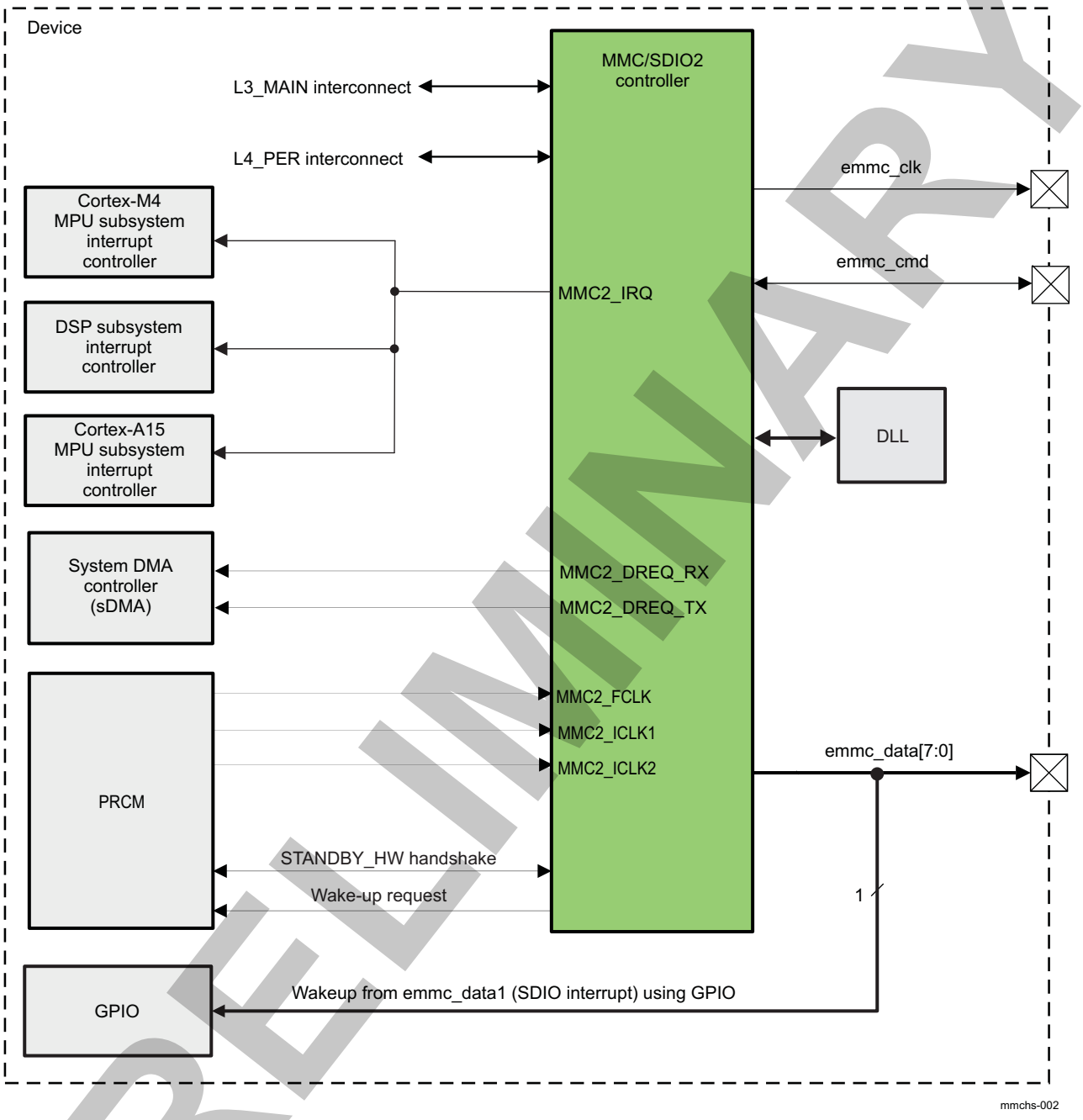

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Figure 24-3. MMC/SDIO3 Overview

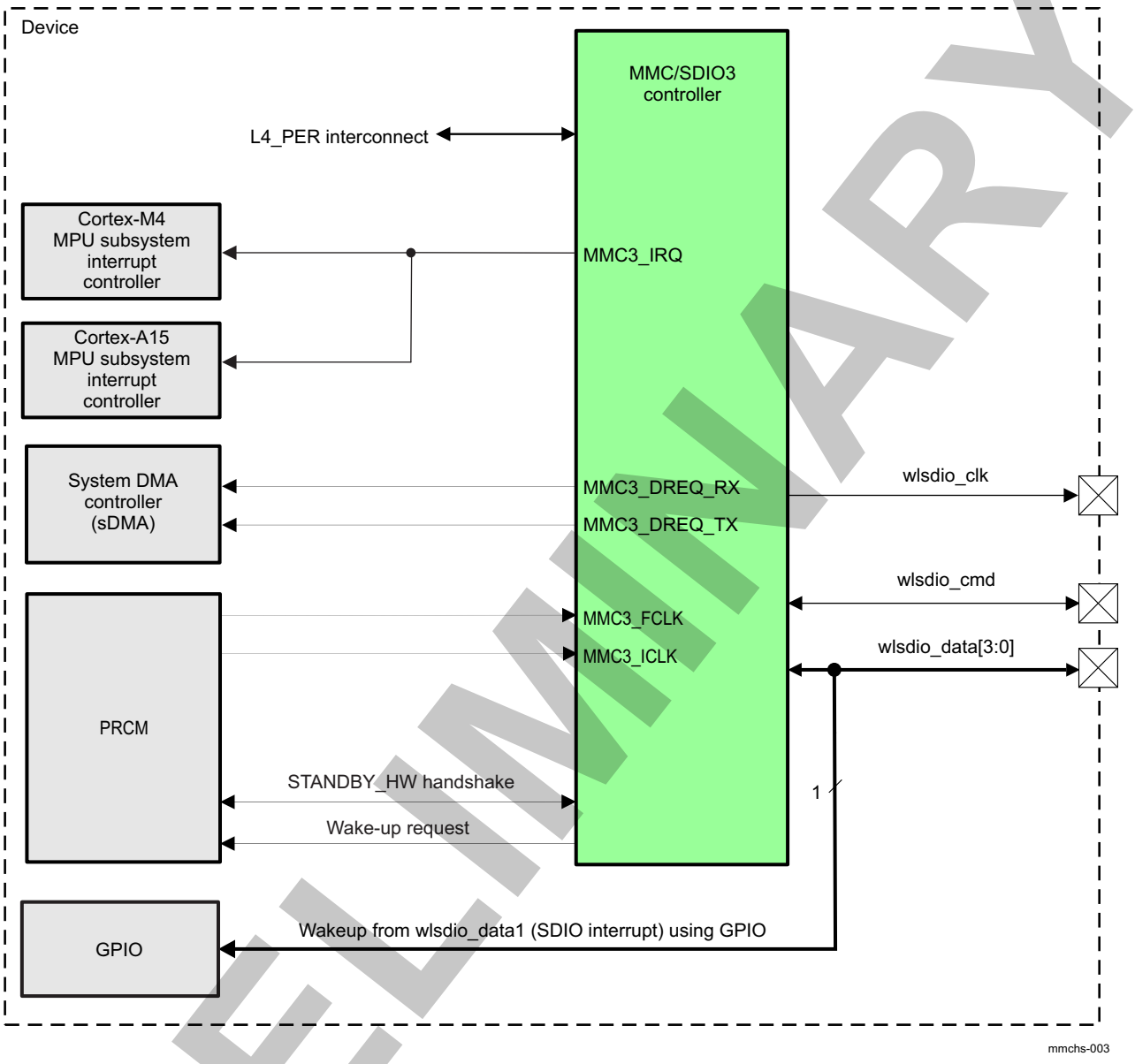

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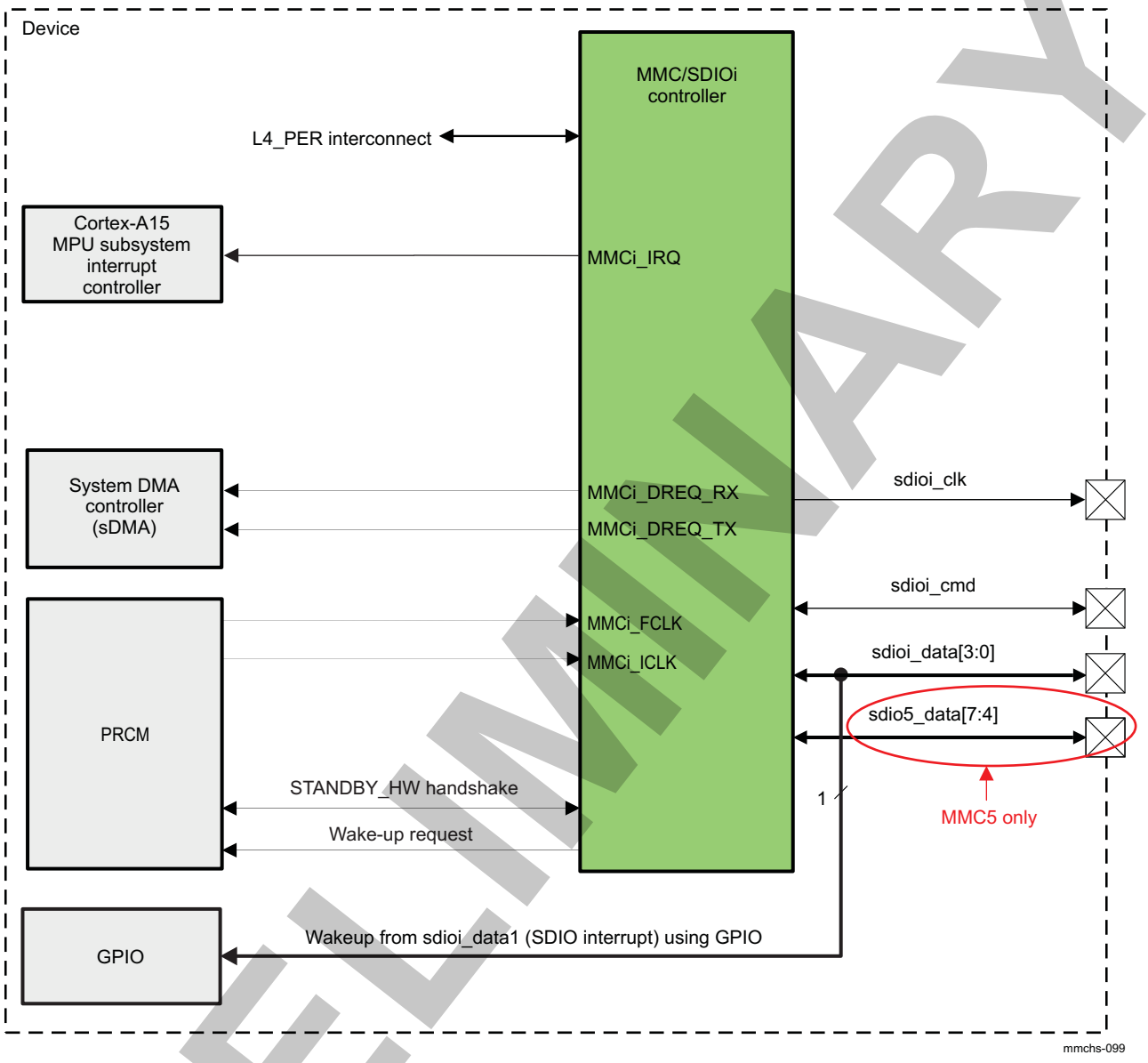
Figure 24-4. MMC/SDIOi Overview (where i = 4 or 5)



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24.1.1 MMC/SDIO Features

This section describes the features supplied by the MMC/SDIO modules.

Compliance with standards:

- Full compliance with MMC/eMMC command/response sets as defined in the JC64 MMC/eMMC standard specification, v4.5.
- Full compliance with SD command/response sets as defined in the SD Physical Layer specification v3.01
- Full compliance with SDIO command/response sets and interrupt/read-wait suspend-resume operations as defined in the SD part E1 specification v3.00
- Full compliance with SD Host Controller Standard Specification sets as defined in the SD card specification Part A2 v3.00

Main features of the MMC/SDIO host controllers:

- Flexible architecture allowing support for new command structure

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- 32-bit wide access bus to maximize bus throughput
- Designed for low power
- Programmable clock generation
- Support retention mode
- Dedicated DLL to support SDR104 mode (MMC1 only)
- Dedicated DLL to support HS200 mode (MMC2 only)
- Card insertion/removal detection and write protect detection (MMC1 only)
- L4 slave interface supports:
  - 32-bit data bus width
  - 8/16/32 bit access supported
  - 9-bit address bus width
  - Streaming burst supported only with burst length up to 7
  - WNP supported
- L3 initiator interface Supports:
  - 32-bit data bus width
  - 8/16/32 bit access supported
  - 32-bit address bus width
  - Burst supported
- Built-in 1024-byte buffer for read or write
- Two DMA_SYSTEM channels, one interrupt line
- Support JC 64 v4.4.1 boot mode operations
- Support SDA 3.00 Part A2 programming model
- Support SDA 3.00 Part A2 DMA feature (ADMA2)
- Supported data transfer rates:
  - MMC1 supports the following SD v3.0 data transfer rates:
    - DS mode (3.3V IOs): up to 12 MBps (24 MHz clock)
    - HS mode (3.3V IOs): up to 24 MBps (48 MHz clock)
    - SDR12 (1.8V IOs): up to 12 MBps (24 MHz clock)
    - SDR25 (1.8V IOs): up to 24 MBps (48 MHz clock)
    - SDR50 (1.8V IOs): up to 48 MBps (96 MHz clock, due to IO frequency limitation)
    - DDR50 (1.8V IOs): up to 48 MBps (48 MHz clock)
    - SDR104 (1.8V IOs) cards can be supported up to 192 MHz clock (96 MBps max)
  - MMC1 supports the Default SD mode 1-bit data transfer up to 24Mbps (3MBps)
  - MMC2 supports the following JC64 v4.5 data transfer rates:
    - Up to 192 MBps in eMMC mode, 8-bit SDR mode (192 MHz clock frequency)
    - Up to 96 MBps in eMMC mode, 8-bit DDR mode (48 MHz clock frequency)
  - MMC2 supports JC64 v4.5

The differences between the MMC/SDIO host controllers and a standard SD host controller defined by the *SD Card Specification, Part A2, SD Host Controller Standard Specification*, v3.00 are:

- The clock divider in the MMC/SDIO host controller supports a wider range of frequency than specified in the *SD Memory Card Specifications*, v3.0. The MMC/SDIO host controller supports odd and even clock ratio.
- The MMC/SDIO host controller supports configurable busy time-out.
- DMA_SYSTEM and ADMA2 64-bit modes are not supported.
- There is no external LED control.

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NOTE: Only even ratios are supported in DDR mode.

Table 24-1 lists the features supported in the 4.5 standard.

Table 24-1. Standard 4.5 Supported Features

Feature	Support	Limitation	Comment
Bus width	1-bit mode		x 1, 4, 8 bits
	4-bit mode		
	8-bit mode		
Support density	No hardware limitation for density support	Limitation can come from file system (32 GiB).	
Simple boot (CMD, alternate boot)	Yes		OMAP5 ROM code supports the following boot modes: 1. Alternate Boot 2. Raw (UDA) Boot 3. File System For more information about boot modes, see Section 28.3.7, *Memory Booting.* in Chapter 28, *Initialization.*
Sleep mode	Yes		
Reliable write	Yes		
Secure write protection	Yes		
Hardware reset	No		Use the reset command instead of GPIO if hardware reset is needed.
Secure memory block (RPMB)	Yes		
Partition feature	Yes		
Secure erase	Yes		
1.2 V	Yes		
DDR interface (bandwidth)	Up to 96 MBps in DDR mode – 8-bit		
High-priority interrupt (read while write)	Yes		
Background operation	Yes		
Enhanced reliable write	Yes		

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24.2 MMC/SDIO Environment

One MMC/SDIO host controller can support one MMC memory card, one SD memory card, or one SDIO card.

Other combinations (for example, two SD cards, one MMC, and one SD card) are not supported through a single controller.

- The MMC/SDIO1 controller integrates an internal transceiver that allows a direct connection to the MMC/SDIO card (1.8 V and 3 V), without external transceiver. It is connected to the L3_MAIN interconnect (internal DMA enabled) and supports 1- and 4-bit data transfers.
- The MMC/SDIO2 controller allows connecting MMC/SDIO cards (only 1.8-V cards) or an external device that uses the MMC/SDIO interface (JC64, for example). The module is connected to the L3_MAIN interconnect (internal DMA enabled) and supports 1-, 4-, and 8-bit data transfers.
- The MMC/SDIO3, MMC/SDIO4, and MMC/SDIO5 controllers allow connecting MMC/SDIO cards (only 1.8-V cards) or an external device that uses the MMC/SDIO interface (wireless LAN, for example). The modules are connected to the level 4 (L4) interconnect. MMC3 and MMC4 instances support 1- and 4-bit data transfers. MMC5 instance supports 1-, 4-, and 8-bit data transfers, but 8-bit data transfer is supported only with embedded devices.

24.2.1 MMC/SDIO Functional Modes

24.2.1.1 MMC/SDIO Connected to an MMC, SD, or SDIO Card

Figure 24-5 shows the MMC/SDIOi host controller (where i = 1, 3, and 4) connected to an MMC, SD, or SDIO card and its related external connections.

Figure 24-5. MMC/SDIOi Controller Connected to an MMC, SD, or SDIO Card (where i = 1, 3, and 4)

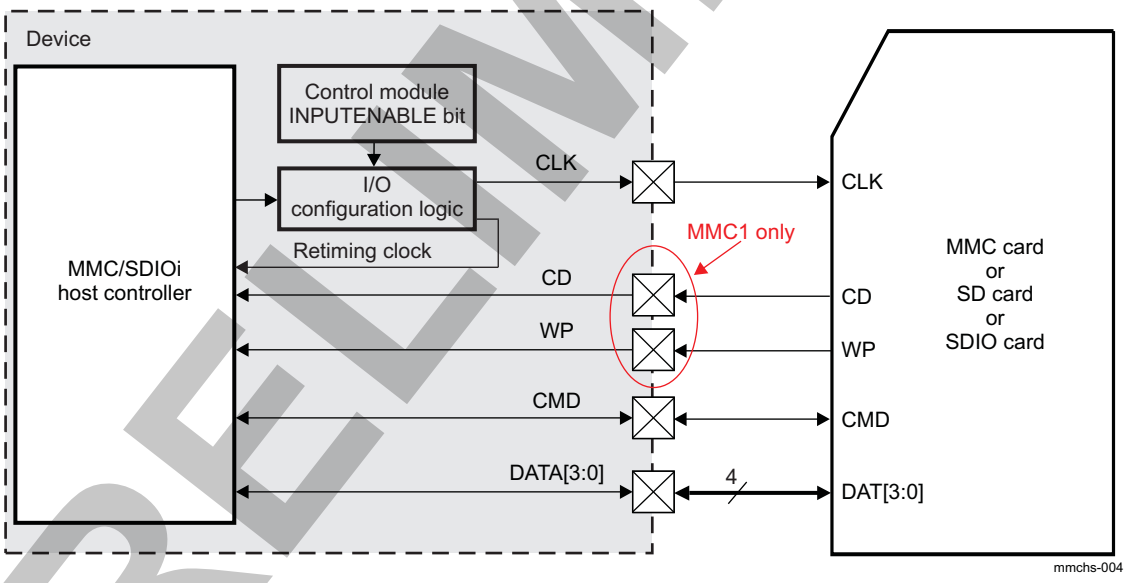

Table 24-2 describes the MMC/SDIOi host controller I/O's (where i = 1, 3, and 4).

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Table 24-2. Description of MMC/SDIOi host controller I/O's (where i = 1, 3, and 4)

Instance	Signal/Pad name	Generic Signal Name	I/O[1]	Description	Reset Value[2]
MMC1	sdcard_clk	CLK	O	External clock for MMC/SD/SDIO card[3]	0
	sdcard_cmd	CMD	I/O	Command signal	Hi-Z[4]
	sdcard_data[3:0]	DATA[3:0]	I/O	Data signals	Hi-Z[4]
	sdcard_cd	CD	I	Card insertion/removal detection signal	Hi-Z
	sdcard_wp	WP	I	Wriwe protect detection signal	Hi-Z
MMC3	wlsdio_clk	CLK	O	External clock for MMC/SD/SDIO card[3]	0
	wlsdio_cmd	CMD	I/O	Command signal	Hi-Z[4]
	wlsdio_data[3:0]	DATA[3:0]	I/O	Data signals	Hi-Z[4]
MMC4	sdio4_clk	CLK	O	External clock for MMC/SD/SDIO card[3]	0
	sdio4_cmd	CMD	I/O	Command signal	Hi-Z[4]
	sdio4_data[3:0]	DATA[3:0]	I/O	Data signals	Hi-Z[4]

(1) I = Input; O = Output; I/O = Bidirectional
(2) Hi-Z = High Impedance
(3) This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).
(4) Initialized as input upon reset

Figure 24-6 shows the MMC/SDIOi host controller (where i = 2 and 5) connected to an MMC, SD or SDIO card and its related external connections.

Figure 24-6. MMC/SDIOi Controller Connected to an MMC, SD, or SDIO Card (where i = 2 and 5)

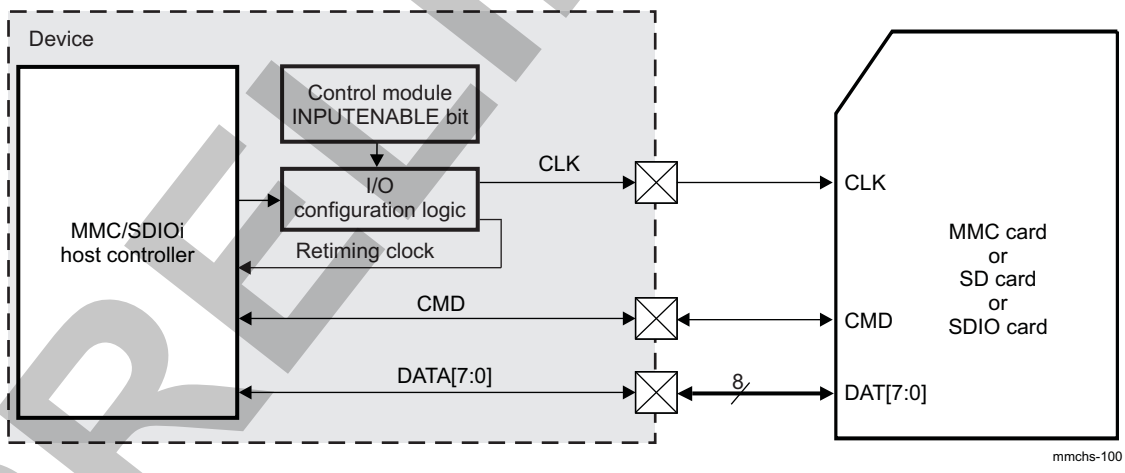

Table 24-3 describes the MMC/SDIOi host controller I/O's (where i = 2 and 5).

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Table 24-3. Description of MMC/SDIOi host controller I/O's (where i = 2 and 5)

Instance	Signal/pad name	Generic signal name	I/O[1]	Description	Reset value[2]
MMC2	emmc_clk	CLK	O	External clock for MMC/SD/SDIO card[3]	0
	emmc_cmd	CMD	I/O	Command signal	Hi-Z[4]
	emmc_data[7:0]	DATA[7:0]	I/O	Data signals	Hi-Z[4]
MMC5	sdio5_clk	CLK	O	External clock for MMC/SD/SDIO card[3]	0
	sdio5_cmd	CMD	I/O	Command signal	Hi-Z[4]
	sdio5_data[7:0]	DATA[7:0]	I/O	Data signals	Hi-Z[4]

(1) I = Input; O = Output; I/O = Bidirectional
(2) Hi-Z = High Impedance
(3) This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).
(4) Initialized as input upon reset

24.2.2 Protocol and Data Format

The bus protocol between the MMC/SDIOi host controller and the card is message-based. Each message is represented by one of the following parts:

- Command: A command starts an operation. The command is transferred serially from the MMC/SDIO host controller to the card on the CMD line.
- Response: A response is an answer to a command. The response is sent from the card to the MMC/SDIO host controller. It is transferred serially on the CMD line.
- Data: Data are transferred from the MMC/SDIO host controller to the card or from a card to the MMC/SDIO host controller using the data lines.
- Busy: The DATA[0] signal is maintained low by the card as far as it is programming the data received.
- CRC status: The CRC result is sent by the card through the DATA[0] line when executing a write transfer. In the case of transmission error, occurring on any of the active data lines, the card sends a negative CRC status on DATA[0]. In the case of successful transmission, over all active data lines, the card sends a positive CRC status on DATA[0] and starts the data programming procedure.

24.2.2.1 Protocol

There are two types of data transfer:

- Sequential operation
- Block-oriented operation

There are specific commands for each type of operation (sequential or block-oriented).

For information about commands and programming sequences supported by the MMC, SD, and SDIO cards, see the *Multimedia Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification (Part E1)*.

Figure 24-7 and Figure 24-8 show how sequential operations are defined. Sequential operation is only for 1-bit transfer and initiates a continuous data stream. The transfer terminates when a stop command follows on the sdmmci_cmd line.

NOTE: Stream commands are supported only by MMC cards.

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Figure 24-7. Sequential Read Operation (MMC Cards Only)

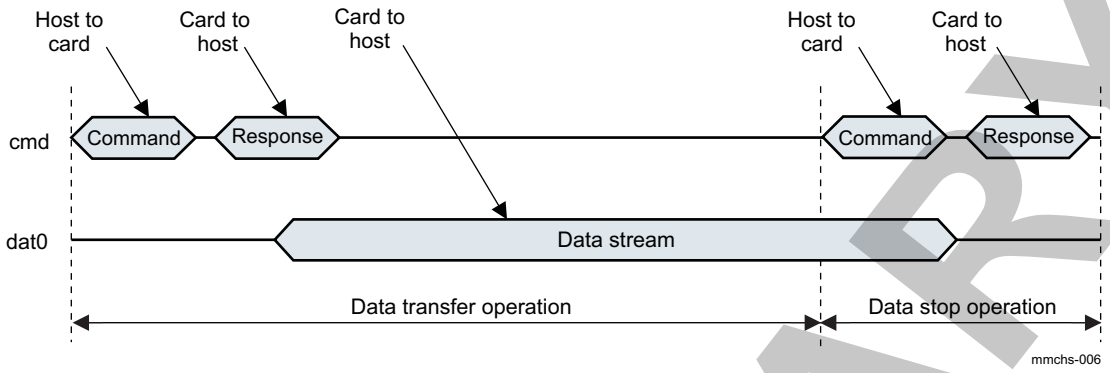

Figure 24-8. Sequential Write Operation (MMC Cards Only)

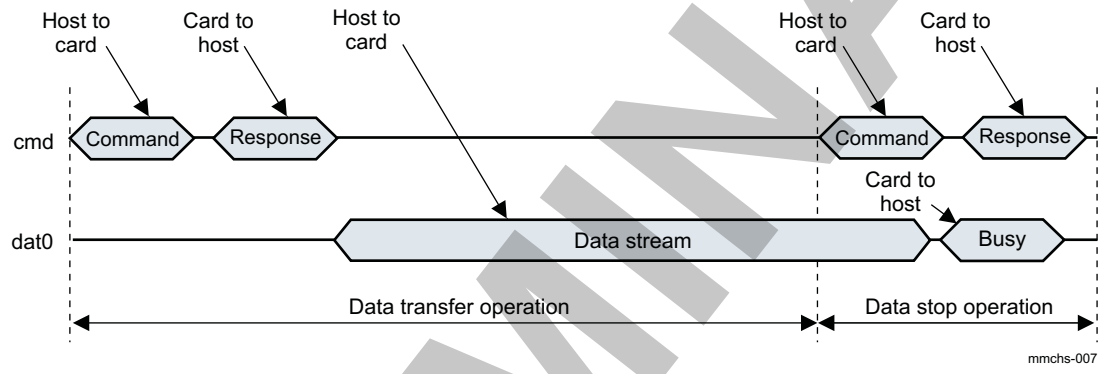

Figure 24-9 and Figure 24-10 show how multiple block-oriented operations are defined. A multiple block-oriented operation sends a data block plus CRC bits. The transfer terminates when a stop command follows on the sdmmci_cmd line. These operations are available for all kinds of cards.

Figure 24-9. Multiple Block Read Operation

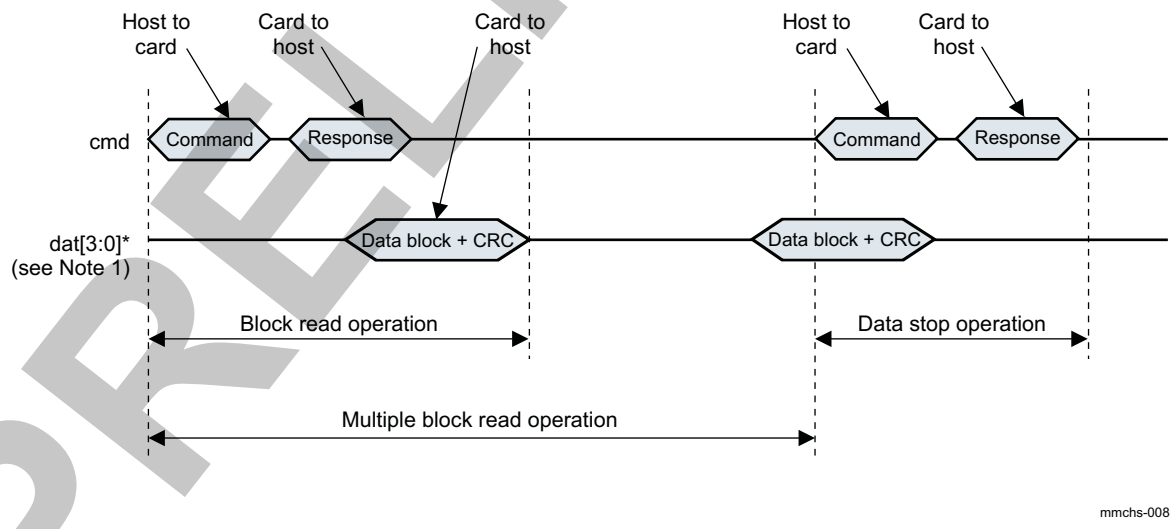

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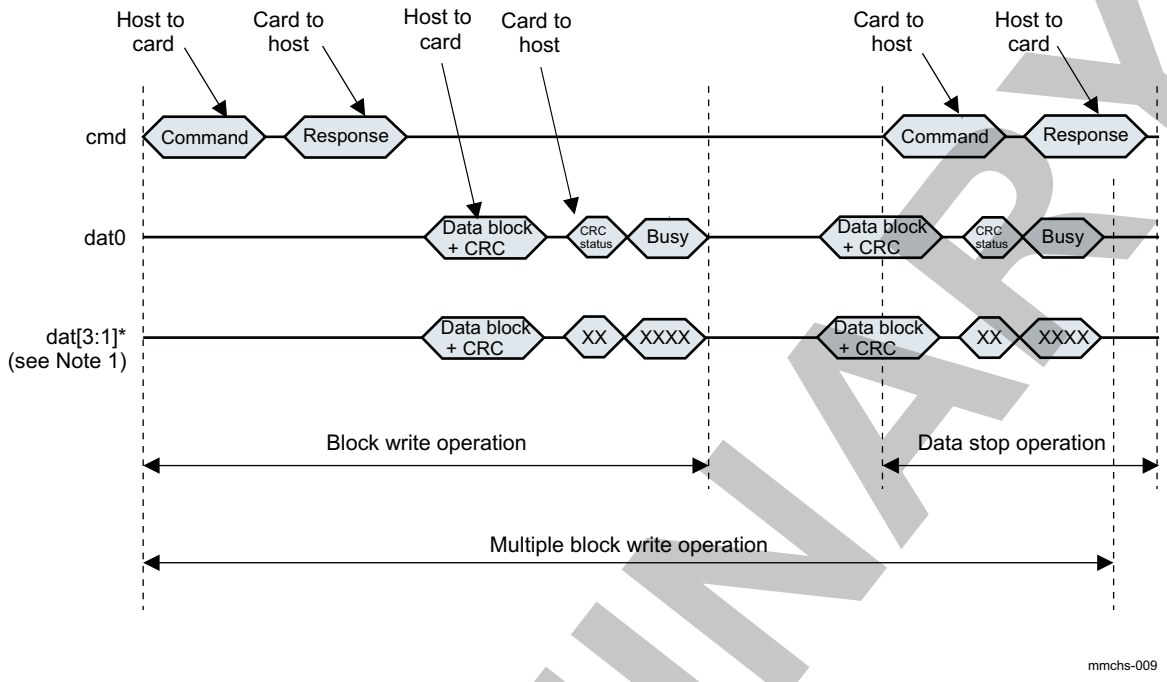
Figure 24-10. Multiple Block Write Operation With Card Busy Signal



NOTE:

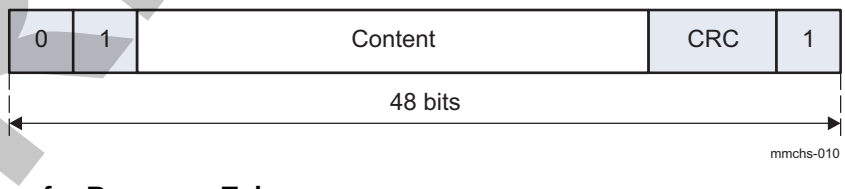
- The card busy signal is not always generated by the card; refer to Figure 24-9 and Figure 24-10, that show a particular case.
- Software must perform a software reset (set the MMCi.MMCHS_SYSCTL[26] SRD bit to 0x1) after a data time-out to ensure that CLK is stopped.
- For multiblock transfer, and especially for MMC cards, a transfer can be aborted without using a stop command. If a CMD23 is used before data transfer to define the number of blocks that will be transferred, then the transfer stops automatically after the last block (if the MMC card supports this feature).

24.2.2.2 Data Format

Coding Scheme for Command Token

Command tokens always start with 0 and end with 1. The second bit is a transmitter bit: 1 for a host command. The content is the command index (coded by 6 bits) and an argument (for example, an address), coded by 32 bits. The content is protected by 7-bit CRC checksum (see Figure 24-11).

Figure 24-11. Command Token Format



Coding Scheme for Response Token

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Response tokens always start with 0 and end with 1. The second bit is a transmitter bit: 0 for a card response. The content is different for each type of response (R1, R2, R3, R4, and R5, R6, R7 [for SD]) and the content is protected by 7-bit CRC checksum (see Figure 24-12 and Figure 24-13). Depending on the type of commands sent to the card, the MMCHS_CMD register must be configured differently to avoid false CRC or index errors to be flagged on command response (see Table 24-4). For more information about response types, see the *Multimedia Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification*.

Figure 24-12. Response Token Format (R1, R3, R4, R5, R6, R7)

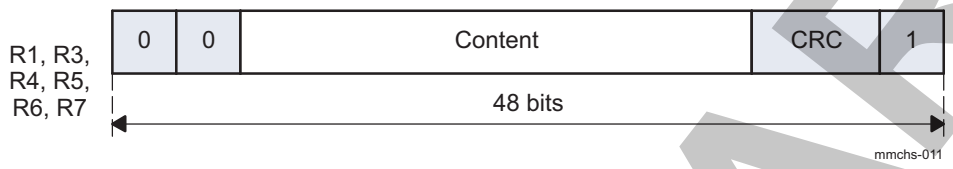

Figure 24-13. Response Token Format (R2)

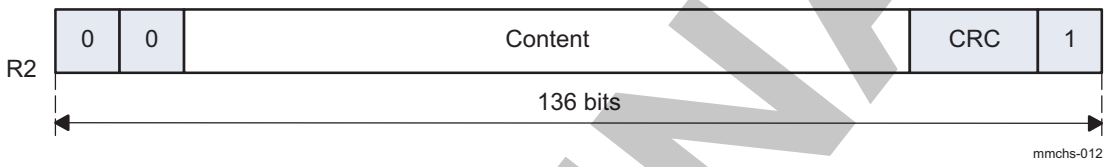

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Table 24-4. Relationship Between Configuration and Name of Response Type

Response Type MMCi.MMCHS_CMD[17:16] RSP_TYPE	Index Check Enable MMCi.MMCHS_CMD[20] CICE	CRC Check Enable MMCi.MMCHS_CMD[19] CCCE	Name of Response Type
00	0	0	No response
01	0	1	R2
10	0	0	R3 (R4 for SD cards)
10	1	1	R1, R6, R5, (R7 for SD cards)
11	1	1	R1b, R5b

Coding Scheme for Data Token

Data tokens always start with 0 and end with 1 (see Figure 24-14 through Figure 24-16).

Figure 24-14. Data Token Format for 1-Bit Transfers

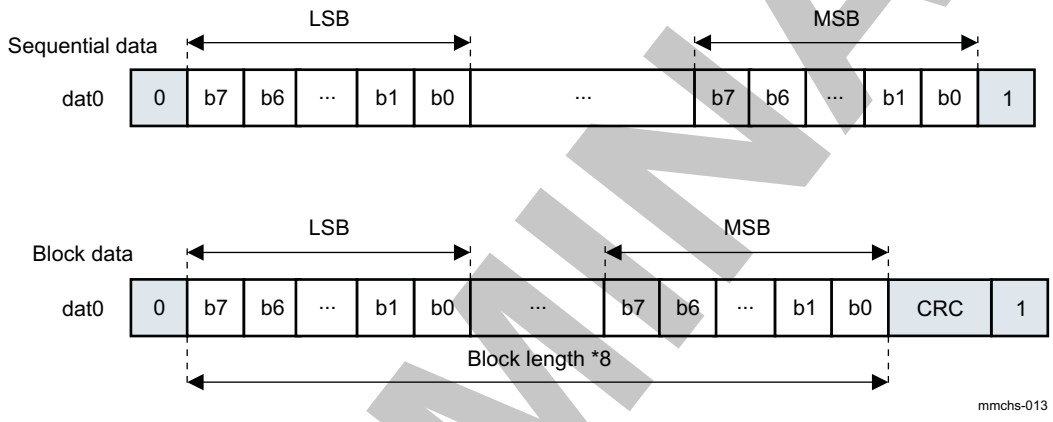

Figure 24-15. Data Token Format for 4-Bit Transfers

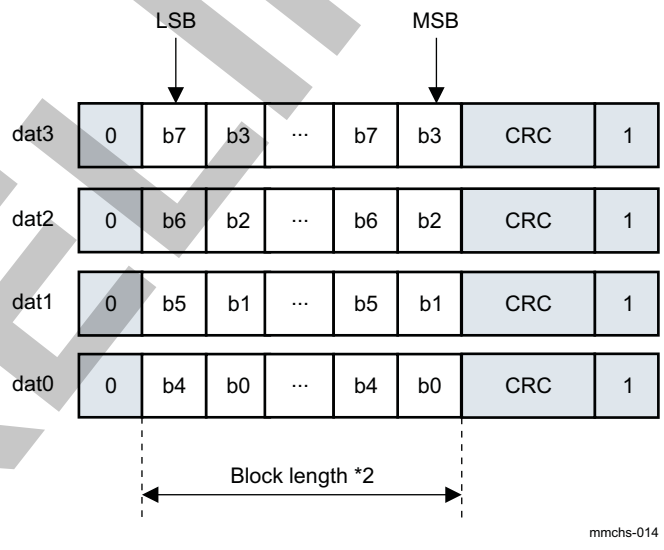

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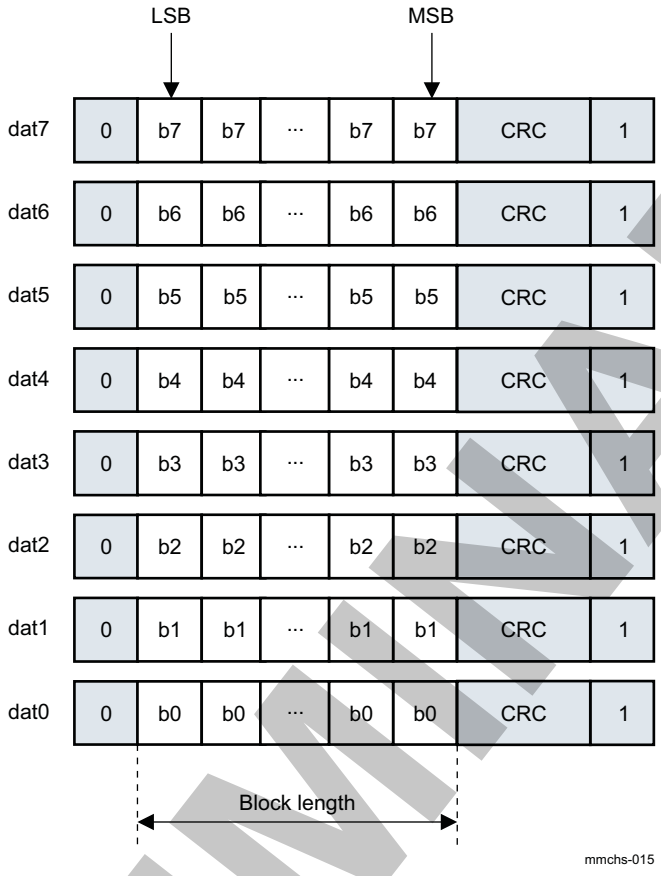
Figure 24-16. Data Token Format for 8-Bit Transfers



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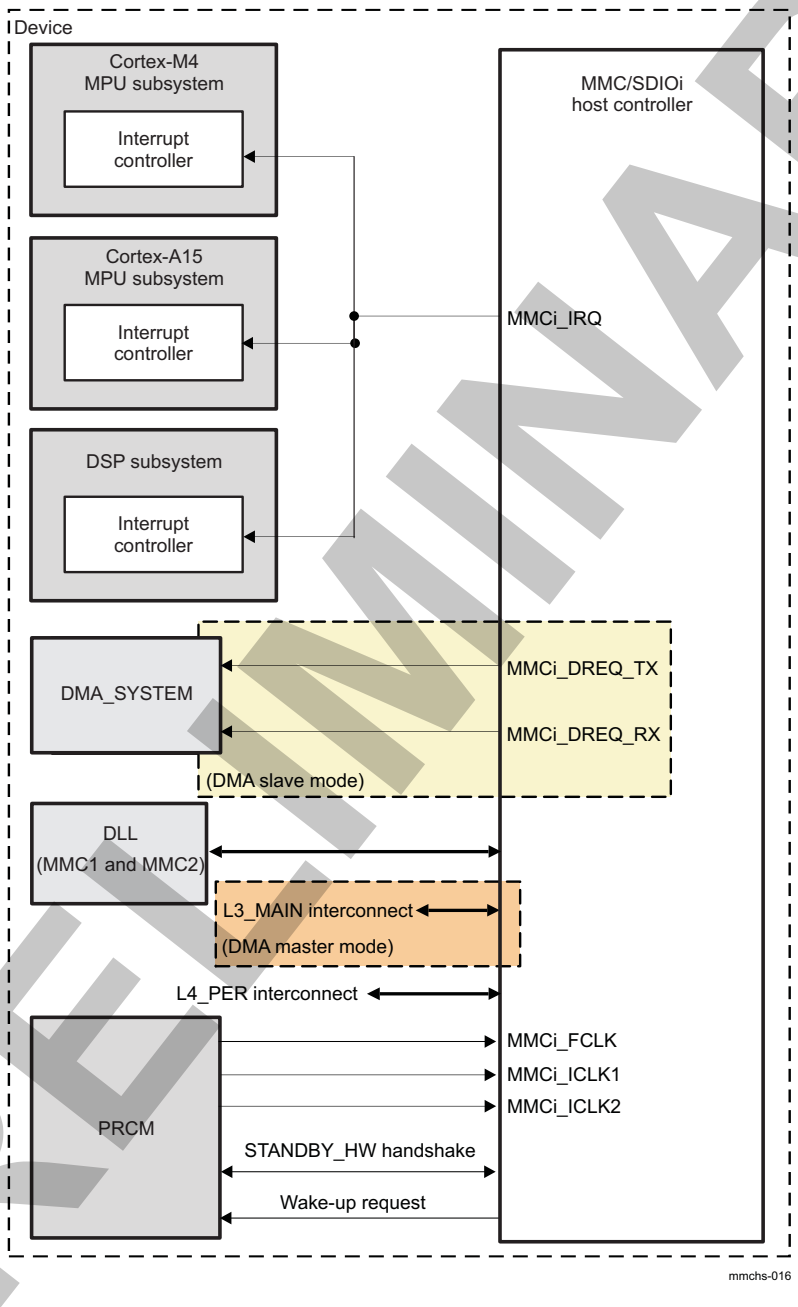
24.3 MMC/SDIO Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 24-17 shows the MMC/SDIO integration.

Figure 24-17. MMC/SDIO Controllers Integration



NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1, *Device Power-Management Architecture Building Blocks*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 24-5 through Table 24-7 summarize the integration of the module in the device.

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Table 24-5. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
MMC1	PD_L3INIT	L3 L4_PER
MMC2	PD_L3INIT	L3 L4_PER
MMC3	PD_CORE	L4_PER
MMC4	PD_CORE	L4_PER
MMC5	PD_CORE	L4_PER

Table 24-6. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MMC1	MMC1_FCLK	MMC1_GFCLK	PRCM	MMC1 function clock
	MMC1_ICLK2	L3INIT_L4_GICLK	PRCM	MMC1 interface clock
	MMC1_ICLK1	L3INIT_L3_GICLK	PRCM	MMC1 interface clock
	CLK_32K	SYS_32K	PRCM	MMC1 debounce clock
MMC2	MMC2_FCLK	MMC2_GFCLK	PRCM	MMC2 function clock
	MMC2_ICLK2	L3INIT_L4_GICLK	PRCM	MMC2 interface clock
	MMC2_ICLK1	L3INIT_L3_GICLK	PRCM	MMC2 interface clock
MMC3	MMC3_ICLK	L4PER_L4_GICLK	PRCM	MMC3 interface clock
	MMC3_FCLK	PER_48M_GFCLK	PRCM	MMC3 function clock
MMC4	MMC4_ICLK	L4PER_L4_GICLK	PRCM	MMC4 interface clock
	MMC4_FCLK	PER_48M_GFCLK	PRCM	MMC4 function clock
MMC5	MMC5_ICLK	L4PER_L4_GICLK	PRCM	MMC5 interface clock
	MMC5_FCLK	PER_96M_GFCLK	PRCM	MMC5 function clock
Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
MMC1	MMC1_RST	L3INIT_RET_RST	PRCM	L3 reset to MMC1
MMC2	MMC2_RST	L3INIT_RET_RST	PRCM	L3 reset to MMC2
MMC3	MMC3_RST	CORE_RST	PRCM	CORE reset to MMC3
MMC4	MMC4_RST	CORE_RST	PRCM	CORE reset to MMC4
MMC5	MMC5_RST	CORE_RST	PRCM	CORE reset to MMC5

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Table 24-7. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MMC1	MMC1_IRQ	IPU_IRQ_66	Cortex™-M4 INTC	MMC1 interrupt to Cortex-M4
	MMC1_IRQ	DSP_IRQ_16	DSP INTC	MMC1 interrupt to DSP
	MMC1_IRQ	MPU_IRQ_83	Cortex™-A15 INTC	MMC1 interrupt to Cortex-A15
MMC2	MMC2_IRQ	IPU_IRQ_67	Cortex-M4 INTC	MMC2 interrupt to Cortex-M4
	MMC2_IRQ	DSP_IRQ_17	DSP INTC	MMC2 interrupt to DSP
	MMC2_IRQ	MPU_IRQ_86	Cortex-A15 INTC	MMC2 interrupt to Cortex-A15
MMC3	MMC3_IRQ	IPU_IRQ_68	Cortex-M4 INTC	MMC3 interrupt to Cortex-M4
	MMC3_IRQ	MPU_IRQ_94	Cortex-A15 INTC	MMC3 interrupt to Cortex-A15
MMC4	MMC4_IRQ	MPU_IRQ_96	Cortex-A15 INTC	MMC4 interrupt to Cortex-A15
MMC5	MMC5_IRQ	MPU_IRQ_59	Cortex-A15 INTC	MMC5 interrupt to Cortex-A15
DMA Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
MMC1	MMC1_DREQ_TX	DMA_SYSTEM_DREQ_60	DMA_SYSTEM	MMC1 DMA TX
	MMC1_DREQ_RX	DMA_SYSTEM_DREQ_61	DMA_SYSTEM	MMC1 DMA RX
MMC2	MMC2_DREQ_TX	DMA_SYSTEM_DREQ_46	DMA_SYSTEM	MMC2 DMA TX
	MMC2_DREQ_RX	DMA_SYSTEM_DREQ_47	DMA_SYSTEM	MMC2 DMA RX
MMC3	MMC3_DREQ_TX	DMA_SYSTEM_DREQ_76	DMA_SYSTEM	MMC3 DMA TX
	MMC3_DREQ_RX	DMA_SYSTEM_DREQ_77	DMA_SYSTEM	MMC3 DMA RX
MMC4	MMC4_DREQ_TX	DMA_SYSTEM_DREQ_56	DMA_SYSTEM	MMC4 DMA TX
	MMC4_DREQ_RX	DMA_SYSTEM_DREQ_57	DMA_SYSTEM	MMC4 DMA RX
MMC5	MMC5_DREQ_TX	DMA_SYSTEM_DREQ_58	DMA_SYSTEM	MMC5 DMA TX
	MMC5_DREQ_RX	DMA_SYSTEM_DREQ_59	DMA_SYSTEM	MMC5 DMA RX

NOTE:

- For a description of the interrupt source, see Section 24.4.4, *Interrupt Requests*.
- For a description of the DMA source, see Section 24.4.5, *DMA Modes*.

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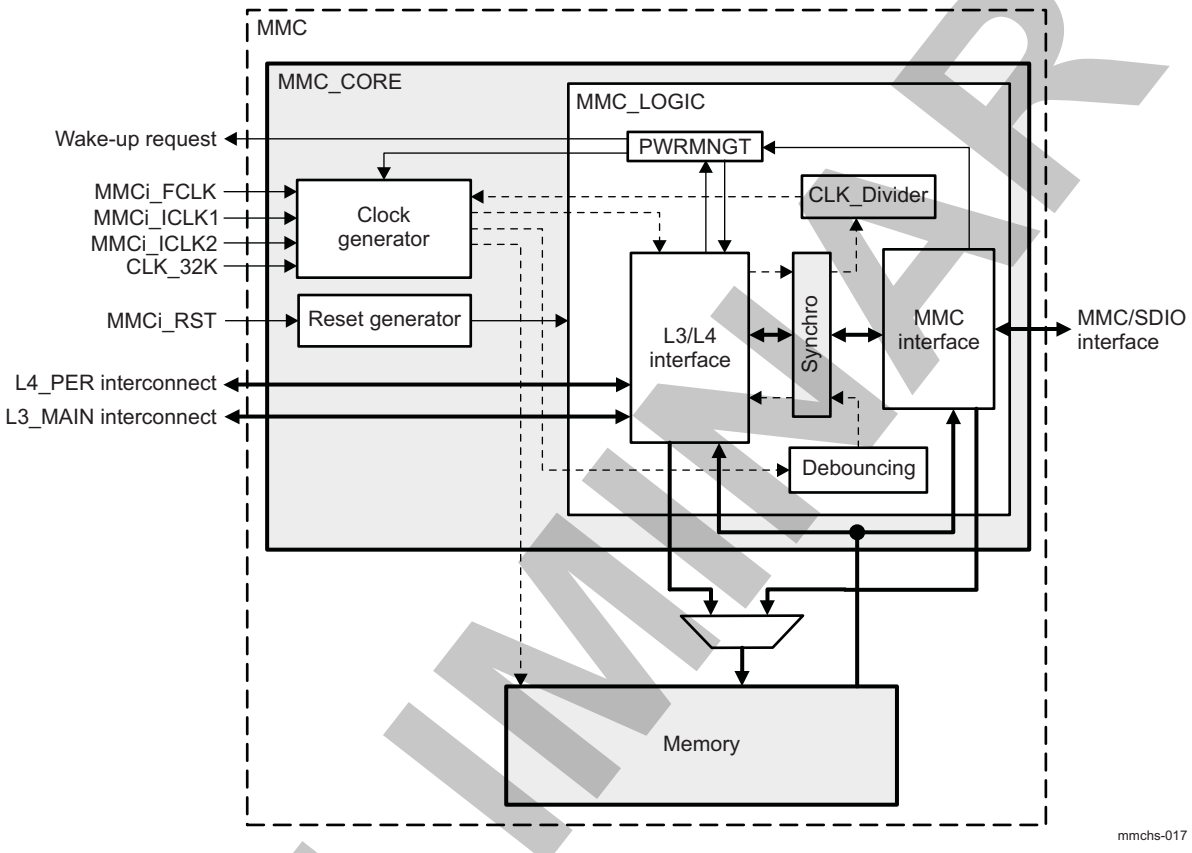
24.4 MMC/SDIO Functional Description

24.4.1 Block Diagram

Figure 24-18 is a block diagram of the MMC/SDIOi host controller.

Figure 24-18. MMC/SDIO Diagram



NOTE: The SD card detect feature is available only if the PD_L3INIT is ON.

24.4.2 Resets

24.4.2.1 Hardware Reset

The module is reinitialized by the hardware (see Table 24-6 for more information about reset signals).

The MMCi.MMCHS_SYSSTATUS[0] RESETDONE bit can be monitored by software to check whether the module is ready to use after a hardware reset.

NOTE: The functional clock (MMCi_FCLK) and interface clock (MMCi_ICLK) must be provided to the module to allow the RESETDONE status bit to be set.

The debounce clock (MMCi_32K) must be active to reset the module correctly.

This hardware reset signal has a global reset action on the module. All configuration registers and all state-machines are reset in all clock domains.

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24.4.2.2 Software Reset

The module is reinitialized by software through the MMCi.MMCHS_SYSCONFIG[1] SOFTRESET bit. This bit has the same effect on the module logic as the hardware signal (MMCi_RST), with the following exceptions:

- Debounce logic
- MMCi.MMCHS_PSTATE, MMCi.MMCHS_CAPA, and MMCi.MMCHS_CUR_CAPA registers (see the corresponding register description)

The SOFTRESET bit is active high. The bit is automatically reinitialized to 0 by hardware. The MMCi.MMCHS_SYSCTL[24] SRA bit has the same action on the design as the SOFTRESET bit.

The MMCi.MMCHS_SYSSTATUS[0] RESETDONE bit can be monitored by software to check whether the module is ready to use after a software reset.

Moreover, two partial software reset bits are provided:

- MMCi.MMCHS_SYSCTL[26] SRD
- MMCi.MMCHS_SYSCTL[25] SRC

These 2 reset bits are useful to reinitialize data or command processes, respectively, in case of line conflict. When these bits are set to 1, a reset process is automatically released when the reset completes:

- The MMCi.MMCHS_SYSCTL[26] SRD bit resets all finite state-machines (FSMs) and status management that handle data transfers on the interface and functional sides.
- The MMCi.MMCHS_SYSCTL[25] SRC bit resets all FSMs and status management that handle command transfers on the interface and functional sides.

24.4.3 Power Management

The MMC/SDIO host controller can enter into different modes and save power:

- Normal mode
- Idle mode

The two modes are mutually exclusive (the module can be in normal mode or in idle mode). The MMC/SDIO host controller is compliant with the handshake protocol of the power, reset, and clock management (PRCM) module.

When the MMC/SDIOi power domain is off, the only way to wake up the power domain and different MMC/SDIOi clocks is to monitor the state of the DATA[1] input pin through a different GPIO line for each MMC/SDIO interface (for more information, see Section 25.1, *GPIO Overview*, in Chapter 25, *GPIO*).

NOTE: The wakeup feature on the sdcard_clk line is not supported, although the CONTROL_CORE_PAD0_USBB3_HSIC_DATA_PAD1_SDCARD_CLK register is configured.

Normal Mode

The autogating of interface and functional clocks occurs when the following conditions are met:

- The MMCi.MMCHS_SYSCONFIG[0] AUTOIDLE bit is set to 1.
- There is no transaction on the MMC interface.

The autogating of interface and functional clocks stops when the following conditions are met:

- A register access occurs through the L4 interconnect.
- A wake-up event occurs (card insertion, card removal, an interrupt from a SDIO card).
- A transaction on the MMC/SD/SDIO interface starts.

When a card removal event is detected the MMC/SDIO host controller automatically clears MMCHS_HCTL[8] SDBP and MMCHS_SYSCTL[2] CEN bits. Then it enters into low power state with auto gated interface clock even if MMCHS_SYSCONFIG[0] AUTOIDLE bit is set to 0. The functional clock is internally switched off and only interconnect read and write accesses are allowed.

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Idle Mode

The MMCi_ICLK and MMCi_FCLK clocks provided to the MMC/SDIO host controller are switched off upon a PRCM module request. They are switched back upon module request.

The MMC/SDIO host controller complies with the handshaking protocol of the PRCM module:

- IDLE request from the system power manager
- Idle acknowledgment from the MMC/SDIO host controller
- Wake-up request from the MMC/SDIO host controller

The idle acknowledgment varies according to the MMCi.MMCHS_SYSCONFIG[4:3] SIDLEMODE bit field:

- 0x0: Force-idle mode. The MMC/SDIO host controller acknowledges the system power manager request unconditionally.
- 0x1: No-idle mode. The MMC/SDIO host controller ignores the system power manager request and behaves normally as if the request was not asserted.
- 0x2: Smart-idle mode. The MMC/SDIO host controller acknowledges the system power manager request according to its internal state.
- 0x3: Smart-idle wake-up-capable mode. The MMC/SDIO host controller acknowledges the system power manager request according to its internal state. However, the module may generate wake-up events when it is in IDLE state (related to IRQ or DMA requests)

During the smart-idle mode period, the MMC/SDIO host controller acknowledges that the MMCi_ICLK and MMCi_FCLK clocks may be switched off, regardless of the value set in the MMCi.MMCHS_SYSCONFIG[9:8] CLOCKACTIVITY bit field.

The debounce clock is used to debounce the signals related to the card insertion and the card removal that are also sources of wake-up in idle mode. The debounce clock must never be switched off by the system power manager in order to detect card removal in functional mode, and detect wake-up in idle mode.

Transition From Normal Mode to Smart-Idle Mode

Smart-idle mode is enabled when the MMCi.MMCHS_SYSCONFIG[4:3] SIDLEMODE bit field is set to 0x2 or 0x3.

The MMC/SDIOi host controller goes into idle mode when the PRCM issues an IDLE request, according to its internal activity.

The MMC/SDIO host controller acknowledges the IDLE request from the PRCM after ensuring the following:

- The current multi- or single-block transfer is complete.
- Any interrupt or DMA request is asserted.
- There is no card interrupt on the DATA[1] signal.

As long as the MMC/SDIOi controller does not acknowledge the IDLE request, if an event occurs, the MMC/SDIOi host controller can still generate an interrupt or a DMA request. In this case, the module ignores the IDLE request from the PRCM module.

As soon as the MMC/SDIOi controller acknowledges the IDLE request from the PRCM module:

- If smart-idle mode: The module does not assert any new interrupt or DMA request.
- If smart-idle wake-up-capable mode: The module may generate wake-up events related to an interrupt or DMA request.

Wake-Up Event in Smart-Idle Mode

The wake-up feature is enabled when both the MMCi.MMCHS_SYSCONFIG[2] ENAWAKEUP bit and one of the three bits MMCi.MMCHS_HCTL[26] REM, MMCi.MMCHS_HCTL[25] INS, MMCi.MMCHS_HCTL[24] IWE are set to 0x1.

The corresponding interrupt status enable bits must also be set before going in idle mode. Setting one of the following bits:

- MMCi.MMCHS_IE[8] CIRQ_ENABLE

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- MMCi.MMCHS_IE[7] CREM_ENABLE
- MMCi.MMCHS_IE[6] CINS_ENABLE

to 0x1 enables the wakeup event detection. The source of wakeup can be identified after idle mode exiting by reading one of the corresponding MMCHS_STAT bits.

The wakeup is generated only in smart-idle mode, when the module is in idle mode.

Table 24-8 lists the supported cases in smart-idle mode.

Table 24-8. Smart-Idle Mode and Wake-Up Capabilities

Mode	MMCi_ICLK Clock	MMCi_FCLK Clock	Wake-Up Event
Card interrupt	May be switched off(1)	May be switched off(1)	The module sends an asynchronous wake-up request when a card interrupt on the DATA[1] signal is detected.
Card insertion	May be switched off(1)	May be switched off(1)	The module sends an asynchronous wake-up request when card insertion is detected.
Card removal	May be switched off(1)	May be switched off(1)	The module sends an asynchronous wake-up request when card removal is detected.

(1) The MMC/SDIOi host controller assumes that both clocks may be switched off, regardless of the value set in the MMCi.MMCHS_SYSCONFIG[9:8] CLOCKACTIVITY bit field.

Transition From Smart-Idle Mode to Normal Mode

The MMC/SDIO host controller detects the end of the idle period when the PRCM module deasserts the IDLE request.

For the wake-up event, there is a corresponding interrupt status in the MMCi.MMCHS_STAT register. The MMC/SDIOi host controller operates the conversion between the wake-up and interrupt (or DMA request) upon exit from smart-idle mode, if the associated enable bit is set in the MMCi.MMCHS_ISE register.

Interrupts and wake-up events have independent enable and disable controls, accessible through the MMCi.MMCHS_HCTL and MMCi.MMCHS_ISE registers. The overall consistency must be ensured by software.

One of the bits MMCHS_STAT[8] CIRQ, MMCHS_STAT[7] CREM, MMCHS_STAT[6] CINS in the interrupt status register is updated with the event that caused the wake-up when one of the bits MMCHS_IE[8] CIRQ_ENABLE, MMCHS_IE[7] CREM_ENABLE, MMCHS_IE[6] CINS_ENABLE is enabled.

Then, the wake-up event at the origin of the transition from smart-idle mode to normal mode is converted into its corresponding interrupt or DMA request. (The MMCi.MMCHS_STAT register is updated and the status of the interrupt signal changes.)

When the IDLE request from the PRCM module is deasserted, the module switches back to normal mode. The module is fully operational.

Force-Idle Mode

Force-idle mode is enabled when the MMCi.MMCHS_SYSCONFIG[4:3] SIDLEMODE bit field is set to 0x0.

Force-idle mode is an idle mode in which the MMC/SDIOi host controller responds unconditionally to the IDLE request from the PRCM module. Moreover, in this mode, the MMC/SDIOi host controller unconditionally deasserts interrupts and DMA request lines if they are asserted.

The transition from normal mode to force-idle mode does not affect the bits of the MMCi.MMCHS_STAT register.

In force-idle mode, the interrupt and DMA request lines are deasserted. MMCi_ICLK and MMCi_FCLK can be switched off.

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CAUTION

In force-idle mode, an IDLE request from the PRCM module during a command or a data transfer can lead to an unexpected and unpredictable result. When the module is idle, any access to the module generates an error as long as the MMCi_ICLK clock is alive.

The module exits force-idle mode when the PRCM module deasserts the IDLE request. Then the module switches back to normal mode. The module is fully operational. Interrupt and DMA request lines are optionally asserted one clock cycle later.

Standby Mode

The MMC/SDIO host controller also provides standby information to the system power manager if the generic parameter MMCHS_HL_HWINFO[0] MADMA_EN is set to 1.

The MMC/SDIO host controller complies with the handshaking protocol of the PRCM module:

- Standby request from the MMC/SDIO host controller
- Wait acknowledgement from the PRCM module

The standby request varies according to the MMCi.MMCHS_SYSCONFIG[13:12] STANDBYMODE bit field:

- 0x0: Force-standby. The MMC/SDIO host controller sends the standby request to the system power manager unconditionally.
- 0x1: No-standby. The MMC/SDIO host controller does not generate any standby request to the system power manager and behaves normally
- 0x2: Smart-standby. The MMC/SDIO host controller sends the standby request to the system power manager according to the master L3 interface state.

Power Pad Control

The MMC/SDIO host controller has the ability to reduce the pad power leakage when no transfer is sent through the pad. According to the MMCHS_CON[15] PADEN there are two different pad power management modes: automatic and manual.

If MMCHS_CON[15] PADEN is set to 1, pads CLK, CMD, DATA[0] and DATA[i] (where i = 2 through 7) are always powerd on.

If MMCHS_CON[15] PADEN is set to 0, the power for pads CLK, CMD, DATA[0] and DATA[i] (where i = 2 through 7) is "ON" only when there is a transfer on going. This is automatically managed by an internal state machine of the MMC/SDIO host controller.

The DATA[1] pad active state is controlled through MMCHS_CON[11] CTPL in order to detect SDIO asynchronous interrupt when there is no transaction.

The delay between pad power "ON" and the command transmission is controlled through the MMCHS_PWCNT register which act as a programmable counter. It is also used to delay the pad power "OFF" after the end of transmission. By default this counter is reset which means that no additional delay is added. But there is approximately 6-7 clock cycles margin between pad power "ON" and real start of the command due to an internal state machine of the MMC/SDIO host controller.

NOTE: The MMCHS_PWCNT register is considered as static. No dynamic configuration during the transfer is supported. This results in an unpredictable behavior.

Local Power Management

Table 24-9 describes the power-management features available for the MMC/SDIOi modules.

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NOTE: For information about source clock gating and a description of the sleep/wake-up transitions, see Section 3.6, *Clock Management Functional Description*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 24-9. Local Power-Management Features

Feature	Registers	Description
Clock auto gating	MMCHS_SYSCONFIG[0] AUTOIDLE	This bit allows a local power optimization inside the module by gating the MMCi_ICLK clock upon the interface activity, or gating the MMCi_FCLK clock upon the internal activity.
Slave-idle modes	MMCHS_SYSCONFIG[3:4] SIDLEMODE	Force-idle, No-idle, Smart-idle and Smart-idle wake-up-capable modes are available.
Clock activity	MMCHS_SYSCONFIG[8:9] CLOCKACTIVITY	For configuration details, see Table 24-10.
Master standby modes	MMCHS_SYSCONFIG[12:13] STANDBYMODE	Force-standby, No-standby and Smart-standby modes are available.
Global wake-up enable	MMCHS_SYSCONFIG[2] ENAWAKEUP	This bit enables the wake-up feature at the module level.
Wake-up sources enable	MMCHS_HCTL register	This register holds one active-high enable bit per event source that is able to generate a wake-up signal.

Table 24-10. Clock Activity Settings

CLOCKACTIVITY Values	Clock State When Module is in IDLE State		Features Available When Module is in IDLE State	Wake-Up Events
	MMCi_ICLK	MMCi_ FCLK		
00	OFF	OFF	None	Card interrupt, Card insertion, Card removal
10	OFF	ON	None	
01	ON	OFF	None	
11	ON	ON	All	

CAUTION

The PRCM module has no hardware means of reading CLOCKACTIVITY settings. Thus, software must ensure consistent programming between the CLOCKACTIVITY and MMCi clock PRCM control bits. For a description of the Clock activity feature, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

24.4.4 Interrupt Requests

Several internal module events can generate an interrupt. Each interrupt has a status bit, an interrupt enable bit, and a signal status enable:

- The status of each type of interrupt is automatically updated in the MMCi.MMCHS_STAT register; it indicates which service is required.
- The interrupt status enable bits of the MMCi.MMCHS_IE register enable or disable the automatic update of the MMCi.MMCHS_STAT register on an event-by-event basis.
- The interrupt signal enable bits of the MMCi.MMCHS_ISE register enable or disable the transmission of an interrupt request on the interrupt line MMCi_IRQ (from the MMC/SDIOi host controller to the MPU subsystem INTC) on an event-by-event basis.

If an interrupt status is disabled in the MMCi.MMCHS_IE register, then the corresponding interrupt request is not transmitted, and the value of the corresponding interrupt signal enable in the MMCi.MMCHS_ISE register is ignored.

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When an interrupt event occurs, the corresponding status bit is automatically set to 0x1 (the MMC/SDIOi host controller updates the status bit) in the MMCi.MMCHS_STAT register. If a mask is later applied on the interrupt in the MMCi.MMCHS_ISE register, the interrupt request is deactivated.

When the interrupt source has not been serviced, if the interrupt status is cleared in the MMCi.MMCHS_STAT register and the corresponding mask is removed from the MMCi.MMCHS_ISE register, the interrupt status is not asserted again in the MMCi.MMCHS_STAT register and the MMC/SDIOi host controller does not transmit an interrupt request.

NOTE: If the buffer write ready (BWR) interrupt or the buffer read ready (BRR) only interrupt are not serviced and are cleared in the MMCi.MMCHS_STAT register, and the corresponding mask is removed, then the MMC/SDIOi host controller waits for the service of the interrupt without updating the status MMCi.MMCHS_STAT register or transmitting an interrupt request.

Table 24-11 lists the event flags, and their mask, that can cause module interrupts.

Table 24-11. Events

Event Flag	Event Mask	Map to	Description
MMCHS_STAT[29] BADA	MMCHS_IE[29] BADA_ENABLE	MMCi_IRQ	Bad access to data space. This bit is set automatically to indicate a bad access to buffer when not allowed: This bit is set during a read access to the data register (MMCHS_DATA) while buffer reads are not allowed (MMCHS_PSTATE[11] BRE = 0). This bit is set during a write access to the data register (MMCHS_DATA) while buffer writes are not allowed (MMCHS_PSTATE[10] BWE = 0).
MMCHS_STAT[28] CERR	MMCHS_IE[28] CERR_ENABLE	MMCi_IRQ	Card error. This bit is set automatically when there is at least one error in a response of type R1, R1b, R6, R5, or R5b. Only bits referenced as type E (error) in the status field in the response can set a card status error. An error bit in the response is flagged only if the corresponding bit in the card status response error MMCHS_CSRE is set. There is no card error detection for the auto CMD12 command.
MMCHS_STAT[26] TE	MMCHS_IE[26] TE_ENABLE	MMCi_IRQ	Tuning Error. This bit is set when an unrecoverable error is detected in a tuning circuit except during tuning procedure. The Tuning Error is with higher priority than the other error interrupts generated during data transfer.
MMCHS_STAT[25] ADMAE	MMCHS_IE[25] ADMAE_ENABLE	MMCi_IRQ	ADMA error. This bit is set when the host controller detects errors during an ADMA-based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA error status register. In addition, the host controller generates this interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state.
MMCHS_STAT[24] ACE	MMCHS_IE[24] ACE_ENABLE	MMCi_IRQ	Auto CMD12 error and Auto CMD23 error. This bit is set automatically when one of the bits MMCHS_AC12[4:0] changes from 0 to 1.
MMCHS_STAT[22] DEB	MMCHS_IE[22] DEB_ENABLE	MMCi_IRQ	Data end bit error. This bit is set automatically when detecting a 0 at the end bit position of read data on the DAT line or at the end position of the CRC status in write mode.
MMCHS_STAT[21] DCRC	MMCHS_IE[21] DCRC_ENABLE	MMCi_IRQ	Data CRC error. This bit is set automatically when there is a CRC16 error in the data phase response following a block read command or if there is a 3-bit CRC status difference of a position 010 token during a block write command.

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Table 24-11. Events (continued)

Event Flag	Event Mask	Map to	Description
MMCHS_STAT[20] DTO	MMCHS_IE[20] DTO_ENABLE	MMCi_IRQ	Data time-out error. This bit is set automatically according to the following conditions: • Busy time-out for R1b, R5b response type • Busy time-out after write CRC status • Write CRC status time-out • Read data time-out
MMCHS_STAT[19] CIE	MMCHS_IE[19] CIE_ENABLE	MMCi_IRQ	Command index error. This bit is set automatically when the response index differs from the corresponding command index previously emitted. The check is enabled through the MMCHS_CMD[20] CICE bit.
MMCHS_STAT[18] CEB	MMCHS_IE[18] CEB_ENABLE	MMCi_IRQ	Command end bit error. This bit is set automatically when detecting a 0 at the end bit position of a command response.
MMCHS_STAT[17] CCRC	MMCHS_IE[17] CCRC_ENABLE	MMCi_IRQ	Command CRC error. This bit is set automatically when a CRC7 error occurs in the command response. CRC check is enabled through the MMCHS_CMD[19] CCCE bit.
MMCHS_STAT[16] CTO	MMCHS_IE[16] CTO_ENABLE	MMCi_IRQ	Command time-out error. This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands that reply within five clock cycles, the time-out is still detected at 64 clock cycles.
MMCHS_STAT[15] ERRI	MMCHS_IE[15] ERRI_ENABLE	MMCi_IRQ	Error interrupt. If any of the bits in the error interrupt status register (MMCHS_STAT[24:15]) are set, this bit is set to 1.
MMCHS_STAT[10] BSR	MMCHS_IE[10] BSR_ENABLE	MMCi_IRQ	Boot status received interrupt. This bit is set automatically when the MMCHS_CON[18] BOOT_CF0 bit is set to 0x1 or 0x2 and a boot status is received on the dat0 line. This interrupt is useful only for the MMC card.
MMCHS_STAT[8] CIRQ	MMCHS_IE[8] CIRQ_ENABLE	MMCi_IRQ	Card interrupt. This bit is used only for SD, SDIO, and CE-ATA cards. In 1-bit mode, the interrupt source is asynchronous (can be a source of asynchronous wakeup). In 4-bit mode, the interrupt source is sampled during the interrupt cycle. In CE-ATA mode, the interrupt source is detected when the card drives the CMD line to 0 during one cycle after data transmission end.
MMCHS_STAT[7] CREM	MMCHS_IE[7] CREM_ENABLE	MMCi_IRQ	Card removal. This bit is set automatically when MMCHS_PSTATE[16] CINS changes from 1 to 0.
MMCHS_STAT[6] CINS	MMCHS_IE[6] CINS_ENABLE	MMCi_IRQ	Card insertion. This bit is set automatically when MMCHS_PSTATE[16] CINS changes from 0 to 1.
MMCHS_STAT[5] BRR	MMCHS_IE[5] BRR_ENABLE	MMCi_IRQ	Buffer read ready. This bit is set automatically during a read operation to the card (see class 2 block-oriented read commands) when one block specified by the MMCHS_BLK[10:0] BLEN bit field is completely written in the buffer. It indicates that the memory card has filled out the buffer and that the LH must empty the buffer by reading it.
MMCHS_STAT[4] BWR	MMCHS_IE[4] BWR_ENABLE	MMCi_IRQ	Buffer write ready. This bit is set automatically during a write operation to the card (see class 4 block-oriented write command) when the host can write a complete block as specified by the MMCHS_BLK[10:0] BLEN bit field. It indicates that the memory card has emptied one block from the buffer and that the LH can write one block of data into the buffer.

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Table 24-11. Events (continued)

Event Flag	Event Mask	Map to	Description
MMCHS_STAT[3] DMA	MMCHS_IE[3] DMA_ENABLE	MMCi_IRQ	DMA interrupt. This status is set when an interrupt is required in the ADMA instruction and after the data transfer completes.
MMCHS_STAT[2] BGE	MMCHS_IE[2] BGE_ENABLE	MMCi_IRQ	Block gap event. When a stop at the block gap is requested (MMCHS_HCTL[16] SBGR), this bit is automatically set when transaction is stopped at the block gap during a read or write operation.
MMCHS_STAT[1] TC	MMCHS_IE[1] TC_ENABLE	MMCi_IRQ	Transfer completed. This bit is always set when a read/write transfer is complete or between two blocks when the transfer is stopped because of a stop at block gap request (MMCHS_HCTL[16] SBGR). • In read mode: This bit is automatically set when a read transfer completes (MMCHS_PSTATE[9] RTA). • In write mode: This bit is automatically set when the DAT line use completes (MMCHS_PSTATE[2] DLA).
MMCHS_STAT[0] CC	MMCHS_IE[0] CC_ENABLE	MMCi_IRQ	Command complete. This bit is set when a 1-to-0 transition occurs in the register command inhibit (MMCHS_PSTATE[0] CMDI). If the command is a type for which no response is expected, then the command complete interrupt is generated at the end of the command. A command time-out error (MMCHS_STAT[16] CTO) has higher priority than command complete (MMCHS_STAT[0] CC). If a response is expected but none is received, then a command time-out error is detected and signaled, instead of the command complete interrupt.

NOTE: To send an interrupt request to the MMCi_IRQ line, the mask/unmask bit must be set in the MMCi.MMCHS_IE and MMCi.MMCHS_ISE registers.

The MMC/SDIOi host controller supports interrupt-driven operation and polling.

24.4.4.1 Interrupt-Driven Operation

An interrupt-enable bit must be set in the MMCi.MMCHS_IE register to enable the module internal source of interrupt.

When an interrupt event occurs, the single interrupt line is asserted and the LH must:

1. Read the MMCi.MMCHS_STAT register to identify which event occurred.
2. Write 1 into the corresponding bit of the MMCi.MMCHS_STAT register to clear the interrupt status and release the interrupt line (if a read is done after this write, this returns 0).

NOTE: In the MMCi.MMCHS_STAT register, the card interrupt (CIRQ) and error interrupt (ERRI) bits cannot be cleared.

The MMCi.MMCHS_STAT[8] CIRQ status bit must be masked by disabling the MMCi.MMCHS_IE[8] CIRQ_ENABLE bit (set to 0x0), and then the interrupt routine must clear the SDIO interrupt source in the SDIO card common control register (CCCR).

The MMCi.MMCHS_STAT[15] ERRI bit is automatically cleared when all status bits in the MMCi.MMCHS_STATregister (bits 31 through 16) are cleared.

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24.4.4.2 Polling

When the interrupt capability of an event is disabled in the MMCi.MMCHS_ISE register, the interrupt line is not asserted:

- Software can poll the status bit in the MMCi.MMCHS_STAT register to detect when the corresponding event occurs.
- Writing 1 into the corresponding bit of the MMCi.MMCHS_STAT register clears the interrupt status and does not affect the interrupt line state.

NOTE: See the previous note concerning clearing of the CIRQ and ERRI bits.

24.4.4.3 Asynchronous Interrupt

Asynchronous interrupt is defined in *SDIO Card Specification version 3.00, part E*. This interrupt is effective in 4-bit mode and is generated without SD clock. Asynchronous interrupt period is defined in the synchronous interrupt period after the last data block and until a next command is received.

Asynchronous interrupt period in a multiple block write operation.

If MMCHS_CAPA[29] AIS is set to 0, writing to MMCHS_AC12[30] AI_ENABLE is ignored. This bit is set to 0. A synchronous interrupt period starts two clocks after the last data block. If MMCHS_AC12[30] AI_ENABLE is set to 1, the asynchronous interrupt period starts four clocks after the start of the synchronous interrupt period. Four clocks after the start bit of the next command, the asynchronous interrupt period ends and goes back to the synchronous interrupt period.

24.4.5 DMA Modes

Two DMA management modes can be used to load data from memory to the internal buffer of the controller (or vice versa). These modes are exclusive and depend on the module integration.

- DMA master mode:

  DMA master mode is selected by setting the MMCHS_CON[20] DMA_MNS bit to 1. In this case, the controller has direct access to data using a specific algorithm called ADMA2 (prevents the system from being interrupted). Data are exchanged using the L3_MAIN master interface, which supports burst accesses to maximize throughput.

  NOTE: This mode is supported only by modules connected to the L3_MAIN interconnect. For more information and/or to check the value of the MMCHS_HL_HWINFO[0] MADMA_EN bit, see Section 24.1, *MMC/SDIO Overview*.

  This mode is available for modules MMC1 and MMC2.

- DMA slave mode:

  DMA slave mode is selected by setting the MMCHS_CON[20] DMA_MNS bit to 0. In this case, the controller is slave on the DMA transaction managed by two separated requests (MMCi_DMA_TX and MMCi_DMA_RX).

  NOTE: This mode is the only mode supported by modules that are not connected to the L3_MAIN interconnect (regardless of the value of the MMCHS_CON[20] DMA_MNS bit). For more information and/or to check the value of the MMCHS_HL_HWINFO[0] MADMA_EN bit, see Section 24.1, *MMC/SDIO Overview*.

  This mode is available for all MMC modules.

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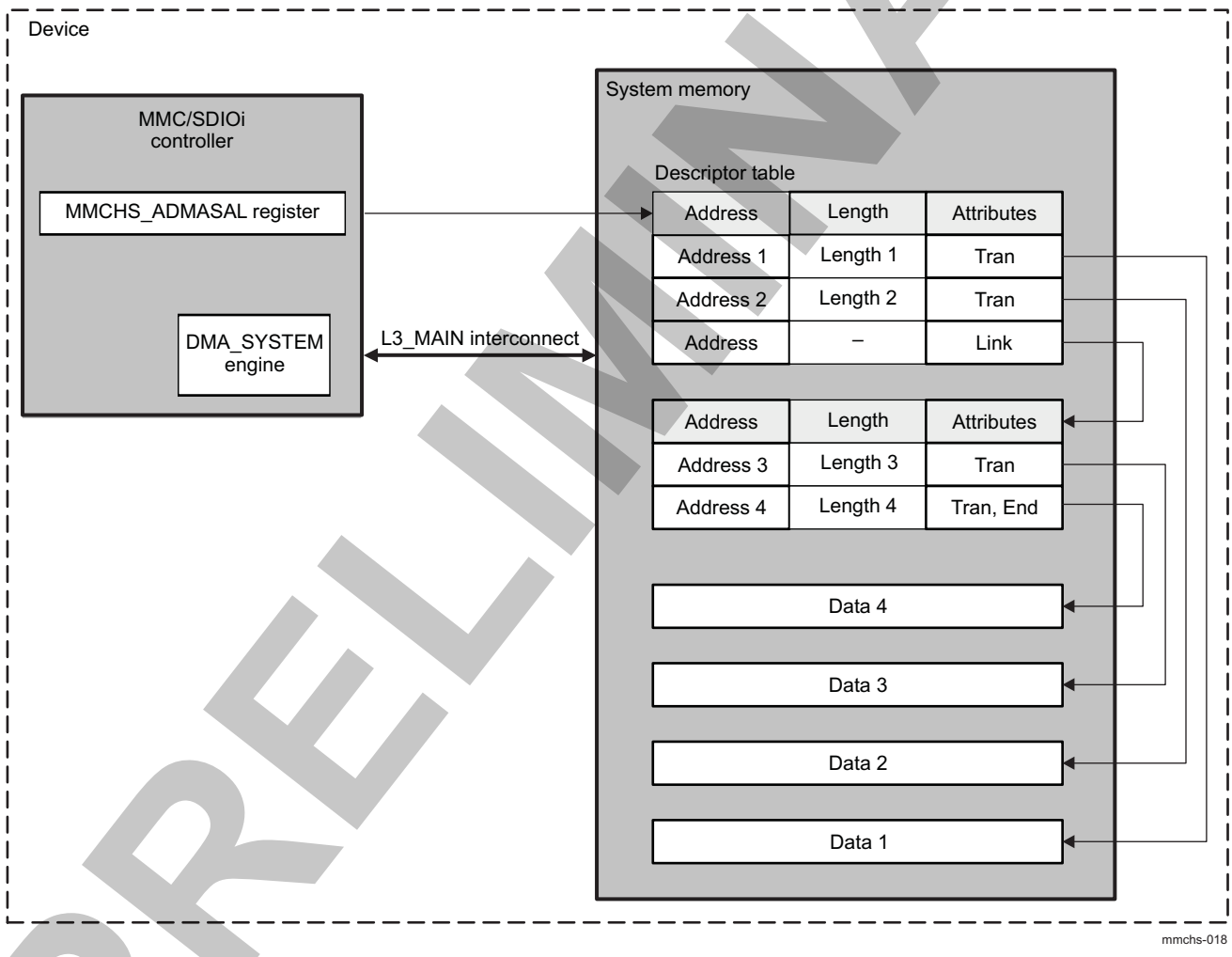
24.4.5.1 Master DMA Operations

The MMC/SDIOi host controller has direct access to the internal data. This feature is called advanced DMA (ADMA). It follows a specific algorithm (ADMA2) defined by an instruction in memory that starts at an address previously loaded in the MMCHS_ADMASAL register before any data command issued to the MMC card. Only 32-bit address spacing is supported by the controller for data storage.

NOTE: This mode is supported only by modules connected to the L3_MAIN interconnect. For more information and/or to check the value of the MMCHS_HL_HWINFO[0] MADMA_EN bit, see Section 24.1, *MMC/SDIO Overview*.

These instructions must be loaded by software in a 32-bit-addressed descriptor table in system memory, as shown in Figure 24-19. In this case the MMCHS_ADMASAL register is used as the program address pointer

Figure 24-19. ADMA Block Diagram Overview



24.4.5.1.1 Descriptor Table Description

Each descriptor line contains an address, a length, and attributes fields. The attributes define which operation will be processed. Every descriptor line is a 64-bit-wide register that is fetched in the controller using the L3_MAIN master interface, and requires two 32-bit accesses to memory.

Table 24-12 shows the structure of a descriptor line.

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Table 24-12. Descriptor Line Overview

Address Field		Length		Reserved		Attributes					
63	32	31	16	15	6	5	4	3	2	1	0
32-bit address		16-bit length		0x0		Act2	Act1	0	Int	Ent	Valid

The attribute of the descriptor line is divided into two parts:

- Attributes[5:4]: The action to be processed by the ADMA engine
- Attributes[3:0]: Additional parameters characterizing the behavior of the ADMA engine

Table 24-13 describes the available actions of a descriptor line.

Table 24-13. Available Actions of a Descriptor Line

Act2	Act1	Symbol	Comment	Operation
0	0	Nop	No operation	Do not execute the current line and go to the next line.
0	1	Rsv	Reserved	Reserved action. Behaves the same as the Nop command.
1	0	Tran	Transfer data	Transfer data of one descriptor line.
1	1	Link	Link descriptor	Link to another descriptor.

Table 24-14 describes the additional parameters of a descriptor line.

Table 24-14. Additional Parameters of a Descriptor Line

Bit	Description
Valid	Valid = 1 indicates that this descriptor line is effective. If Valid = 0, an ADMA error interrupt is generated and the ADMA is stopped. This prevents runaways.
End	End = 1 indicates the end of a descriptor. The transfer-complete interrupt is generated when the operation of the descriptor line is complete.
Int	Int = 1 generates a DMA interrupt when the operation of the descriptor line is complete.

24.4.5.1.2 Requirements for Descriptors

The following sections discuss restrictions and tips on how to correctly configure the descriptors to be used by the ADMA engine.

24.4.5.1.2.1 Data Length

There are three requirements to program descriptors:

- The minimum unit of address is 4 bytes.
- The maximum data length of each descriptor line is less than 64 KiB.
- Total length = $Length_1$ + $Length_2$+ $Length_3$ + ... + $Length_n$ must be a multiple of the block size.

If the total length of a descriptor is not a multiple of the block size, data transfer with the ADMA engine may not have been terminated. In this case, the controller returns a data time-out event and the transfer is aborted.

The block count register (the MMCHS_BLK[31:16] NBLK bit field) is defined as 16 bits and limits data transfers to a maximum of 65,535 blocks. If the ADMA data transfer size is less than or equal to the 65,535-block transfer, the block count register can be used. In this case, the total length of the descriptor table must be equivalent to "block size" by "block count." If the ADMA data transfer is greater than 65,535 blocks, the block count register must be disabled by setting the block count enable bit (MMCHS_CMD[1] BCE) to 0. In this case, the length of the data transfer is not designated by the block count but by the descriptor table.

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NOTE: The timing for detecting the last block on the SD bus may differ, which affects control of the read transfer active (MMCHS_PSTATE[9] RTA), write transfer active (MMCHS_PSTATE[8] WTA), and DAT line active (MMCHS_PSTATE[2] DLA) bits. In case of a read operation, more blocks than required may be read from the card. The host driver must ignore an out-of-range error if the read operation is for the last block of the memory area.

24.4.5.1.2.2 Supported Features

The ADMA engine does not support the suspend/resume function. However, the stop and continue functions are available.

When the stop-at-block-gap request (the MMCHS_HCTL[16] SBGR bit) is set during the ADMA operation, the block gap event interrupt is generated when the ADMA is stopped at block gap (the MMCHS_STAT[2] BGE bit). The host controller must stop the ADMA read operation by using read wait or by stopping the SD clock. While stopping ADMA, SD commands cannot be issued.

24.4.5.1.2.3 Error Generation

When an error occurs during an ADMA transfer, the ADMA operation is stopped and the ADMA error interrupt is generated. The ADMA error state field (the MMCHS_ADMAES[1:0] AES bit field) holds the state of the ADMA when it is stopped. Software can identify the erroneous descriptor line by using the following method:

- If the ADMA stopped at ST_FDS state, the ADMA system address register (MMCHS_ADMASAL) points to the erroneous descriptor line.
- If the ADMA stopped at ST_TFR or ST_STOP state, the ADMA system address register points to the descriptor line following the erroneous one.

24.4.5.1.3 Advanced DMA Description

The ADMA is a DMA controller embedded in each eMMC controller. It can be seen as a small sequencer that fetches a descriptor line and executes the corresponding action. The base address of the descriptor table is stored in the MMCHS_ADMASAL register.

NOTE: Software must write the base address of the descriptor table in the MMCHS_ADMASAL register before the first use of the ADMA engine.

The ADMA program is executed according to descriptor attributes (see Section 24.4.5.1.1, *Descriptor Table Description*) and an FSM, as shown in Figure 24-20.

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Figure 24-20. ADMA Finite State-Machine

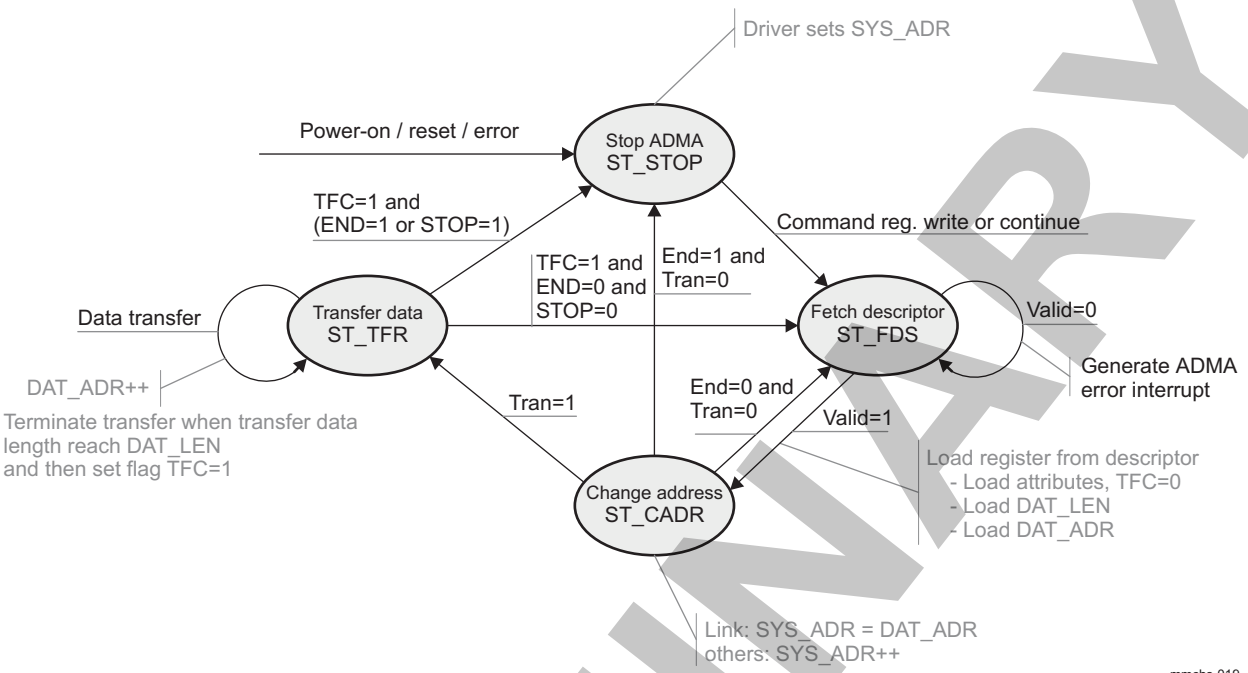

Table 24-15 describes each state of the ADMA FSM.

Table 24-15. ADMA2 States Description

State Name	Operation
ST_FDS (fetch descriptor)	ADMA2 fetches a descriptor line and sets parameters in internal registers. It then goes to ST_CADR state.
ST_CADR (change address)	Link operation loads another descriptor address to the ADMA system address register (MMCHS_ADMASAL). In other operations, the ADMA system address register is incremented to point to the next descriptor line. If End = 0, go to ST_FDS state. **NOTE**: ADMA2 does not stop at this state if some errors occur.
ST_TFR (transfer data)	Data transfer of one descriptor line is executed between system memory and the SD card: • If data transfer continues (End = 0), go to ST_FDS state. • If data transfer completes, go to ST_STOP state.
ST_STOP (stop DMA)	ADMA2 stays in this state in the following cases: • After power-on reset (POR) or software reset • All descriptor data transfers are complete. If a new ADMA operation is stated by writing the command register, go to ST_FDS state.

Table 24-16 gives the description of each symbol used in the ADMA FSM (see Figure 24-20).

Table 24-16. ADMA FSM Symbol Definition

Symbol	Definition
SYS_ADR	ADMA system address register
SYS_ADR++	Point to next descriptor line
DAT_ADR	Data address register (internal)
DAT_LEN	Data length register (internal)
TFC	Transfer complete flag (internal)
STOP	Stop-at-block-gap request

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24.4.5.2 Slave DMA Operations

The MMC/SDIOi host controller can be interfaced with a DMA controller. At the system level, the advantage is to discharge the LH of the data transfers. The module does not support wide DMA access (more than 1024 bytes) for SD cards, as specified in the *SD Card Specification* and *SD Host Controller Standard Specification*.

NOTE: This mode is implied by modules that are not connected to the L3_MAIN interconnect (regardless of the value of the MMCHS_CON[20] DMA_MNS bit). For more information and/or to check the value of the MMCHS_HL_HWINFO[0] MADMA_EN bit, see Section 24.4.5.1, *Master DMA Operations*.

The DMA request is issued if the following conditions are met:

- The MMCi.MMCHS_CMD[0] DE bit is set to 1 to trigger the initial DMA request (the write must be done when running the data transfer command).
- A command was emitted on the CMD line.
- There is enough space in the buffer of the MMC/SDIOi host controller to write an entire block (BLEN writes).

24.4.5.2.1 DMA Receive Mode

In a DMA block read operation (single or multiple), the request signal MMCi_DMA_RX is asserted to its active level when a complete block is written in the buffer. The block size transfer is specified in the MMCi.MMCHS_BLK[10:0] BLEN bit field.

MMCi_DMA_RX is deasserted to its inactive level when the DMA_SYSTEM module reads one word from the buffer.

Only one request is sent per block; the DMA controller can make a 1-shot read access or several DMA bursts, in which case the DMA controller must manage the number of burst accesses, according to the BLEN bit field block size.

New DMA requests are internally masked if the DMA_SYSTEM has not read exactly BLEN bytes and a new complete block is not ready. Because DMA accesses are 32-bit accesses, the number of DMA_SYSTEM reads is Integer(BLEN / 4) + 1.

The receive buffer never overflows. In multiple block transfers for block sizes larger than 512 bytes, when the buffer becomes full, the sdmmci_clk clock signal (provided to the card) is momentarily stopped until the DMA_SYSTEM or the MPU performs a read access, which reads a complete block in the buffer.

To summarize:

- DMA transfer size = BLEN buffer size in one shot or by burst
- One DMA request per block

Figure 24-21 shows DMA receive mode.

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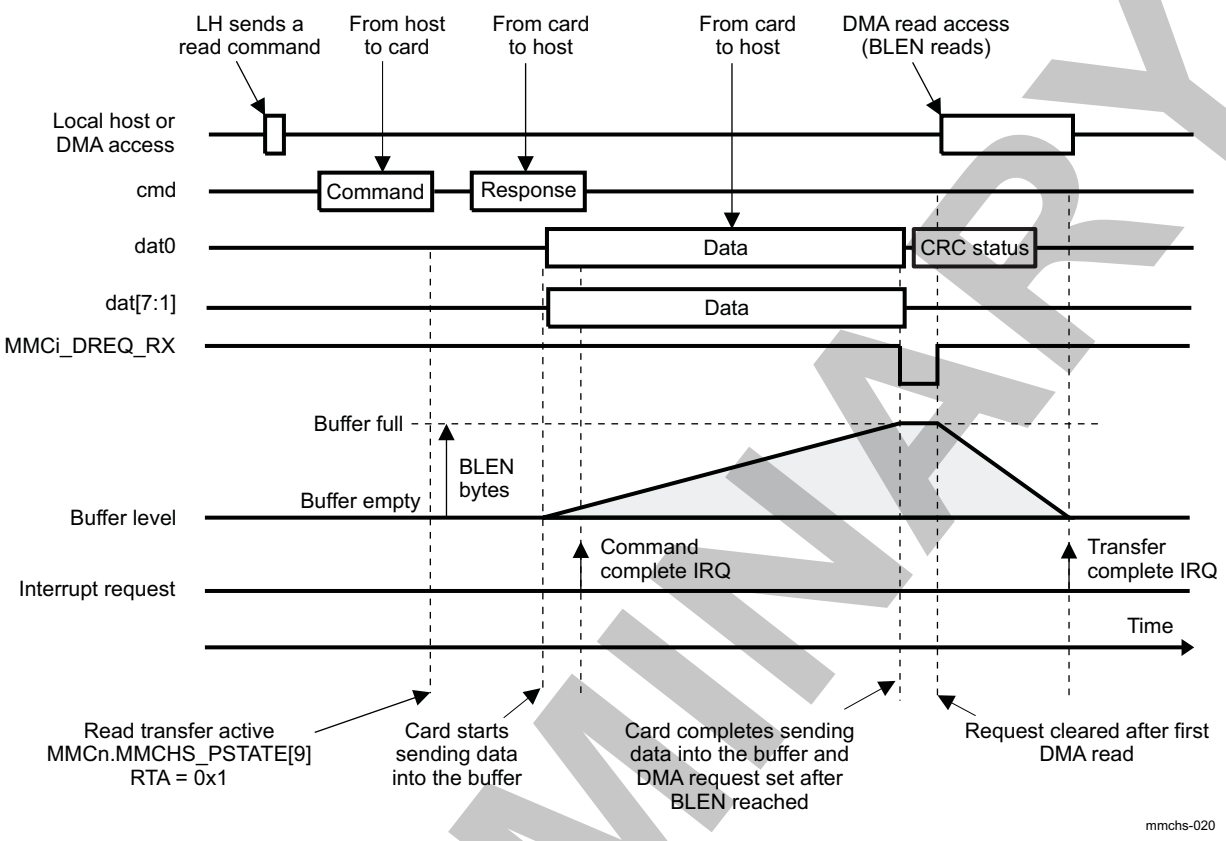
Figure 24-21. DMA Receive Mode



24.4.5.2.2 DMA Transmit Mode

In a DMA block write operation (single or multiple), the request signal MMCi_DMA_TX is asserted to its active level when a complete block is to be written to the buffer. The block size transfer is specified in the MMCi.MMCHS_BLK[10:0] BLEN bit field.

MMCi_DMA_TX is deasserted to its inactive level when the DMA_SYSTEM writes one word to the buffer.

Only one request is sent per block; the DMA controller can make a 1-shot write access or multiple write DMA bursts, in which case the DMA controller must manage the number of burst accesses, according to the BLEN bit field block size.

New DMA requests are internally masked if the DMA_SYSTEM has not written exactly BLEN bytes (because DMA accesses are 32-bit accesses, the number of DMA_SYSTEM reads is Integer(BLEN / 4) + 1) and if there is not enough memory space to write a complete block in the buffer.

To summarize:

- DMA transfer size = BLEN buffer size in one shot or by burst
- One DMA request per block

Figure 24-22 shows DMA transmit mode.

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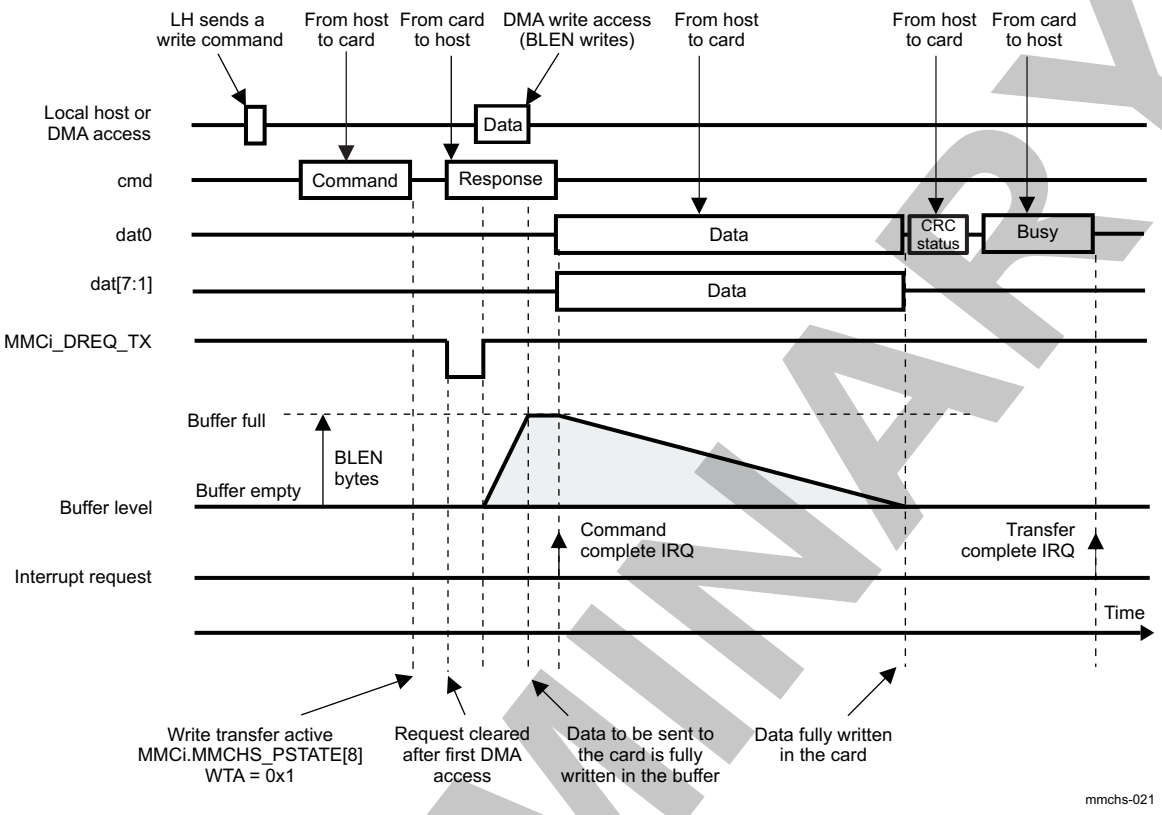
Figure 24-22. DMA Transmit Mode



24.4.6 Mode Selection

The MMC/SDIO host controller can be used in two modes: MMC and SD/SDIO. It has been designed to be the most transparent with the type of card.

The type of the card connected is differentiated by the software initialization procedure. Software identifies the type of card connected during software initialization. For each card type, there are corresponding commands. Some commands are not supported by all cards. For more information, see the *Multimedia Card System Specification*, *SD Memory Card Specifications*, and *SDIO Card Specification, Part E1*.

The purpose of the module is to transfer commands and data to whatever card is connected, respecting the protocol of the connected card.

Writes and reads to the card must respect the appropriate protocol of that card.

24.4.7 Buffer Management

24.4.7.1 Data Buffer

The MMC/SDIOi host controller uses a data buffer. This buffer transfers data from one data bus (interconnect) to another data bus (SD/SDIO or MMC card bus) and vice versa.

The buffer is the heart of the interface and ensures the transfer between the two interfaces (interconnect and the card).

To enhance performance, the data buffer is completed by a prefetch register and a post-write buffer that are not accessible by the host controller.

The read access time of the prefetch register is faster than that of the data buffer. The prefetch register allows data to be read from the data buffer at an increased speed by preloading data into the prefetch register.

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The entry point of the prefetch buffer and the post-write buffer is the 32-bit MMCi.MMCHS_DATA register. A write access to the MMCi.MMCHS_DATA register followed by a read access from the MMCi.MMCHS_DATA register corresponds to a write access to the post-write buffer followed by a read access to the prefetch buffer. As a consequence, it is normal that the data of the write access to the MMCi.MMCHS_DATA register and the data of the read access to the MMCi.MMCHS_DATA register are different.

The number of 32-bit accesses to the MMCi.MMCHS_DATA register that are needed to read (or write) a data block with a size of the MMCi.MMCHS_BLK[11:0] BLEN bit field is equal to the rounded up result of BLEN divided by 4.

The maximum block size supported by the host controller is hard-coded in the MMCi.MMCHS_CAPA[17:16] MBL bit field and cannot be changed.

A read access to the MMCi.MMCHS_DATA register is allowed only when the buffer read-enable status is set to 1 (the MMCi.MMCHS_PSTATE[11] BRE bit); otherwise, a bad access (the MMCi.MMCHS_STAT[29] BADA bit) is signaled.

A write access to the MMCi.MMCHS_DATA register is allowed only when the buffer write-enable status is set to 1 (the MMCi.MMCHS_PSTATE[10] BWE bit); otherwise, a bad access (the MMCi.MMCHS_STAT[29] BADA bit) is signaled and the data are not written.

The data buffer has two modes of operation to store and read of the first and second portions of the data buffer:

- When the size of the data block to transfer is less than or equal to MEM_SIZE/2 (in double-buffering), two data transfers can occur at the same time from one data bus to the other data bus, and vice versa. The MMC/SDIOi host controller uses the two portions of the data buffer in a ping-pong manner so that storing and reading the first and second portions of the data buffer are automatically interchanged from time to time. In this way, data can be read from one portion (for instance, through a DMA read access on the interconnect bus) while data (for instance, from the card) are being stored into the other portion, and vice versa. When BLEN is less than or equal to 0x200 (that is, less than or equal to 512 bytes), each of the two portions of the buffer that can be used have a size of BLEN (that is, 32 bits × BLEN divided by 4). No more than this total size of 2 × 32 bits × BLEN divided by 4 can be used.

CAUTION

The MMCi.MMCHS_CMD[4] DDIR bit must be configured before a transfer to indicate the direction of the transfer.

Figure 24-23 and Figure 24-24 show the buffer management for a write and a read, respectively.

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Figure 24-23. Buffer Management for a Write

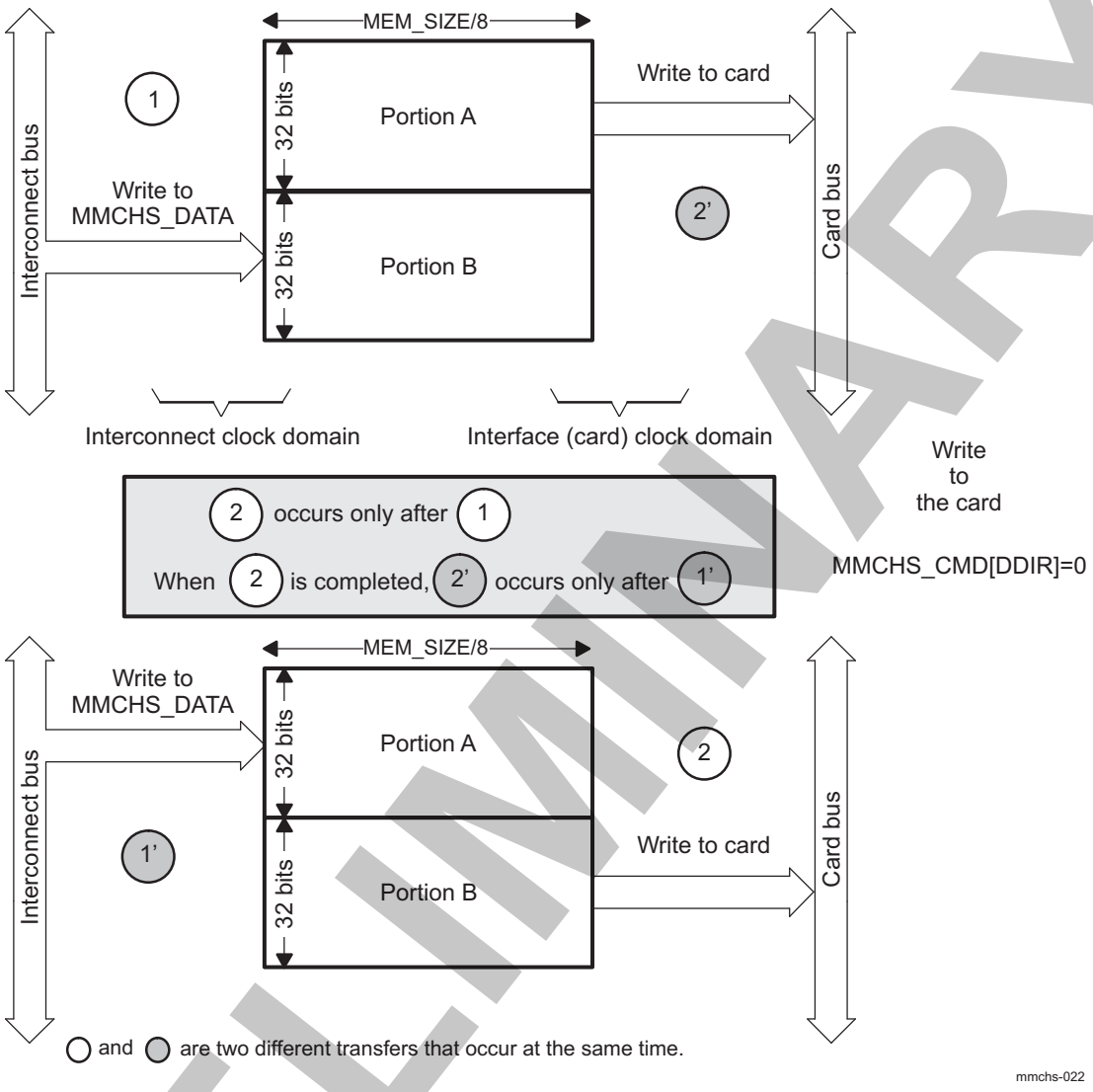

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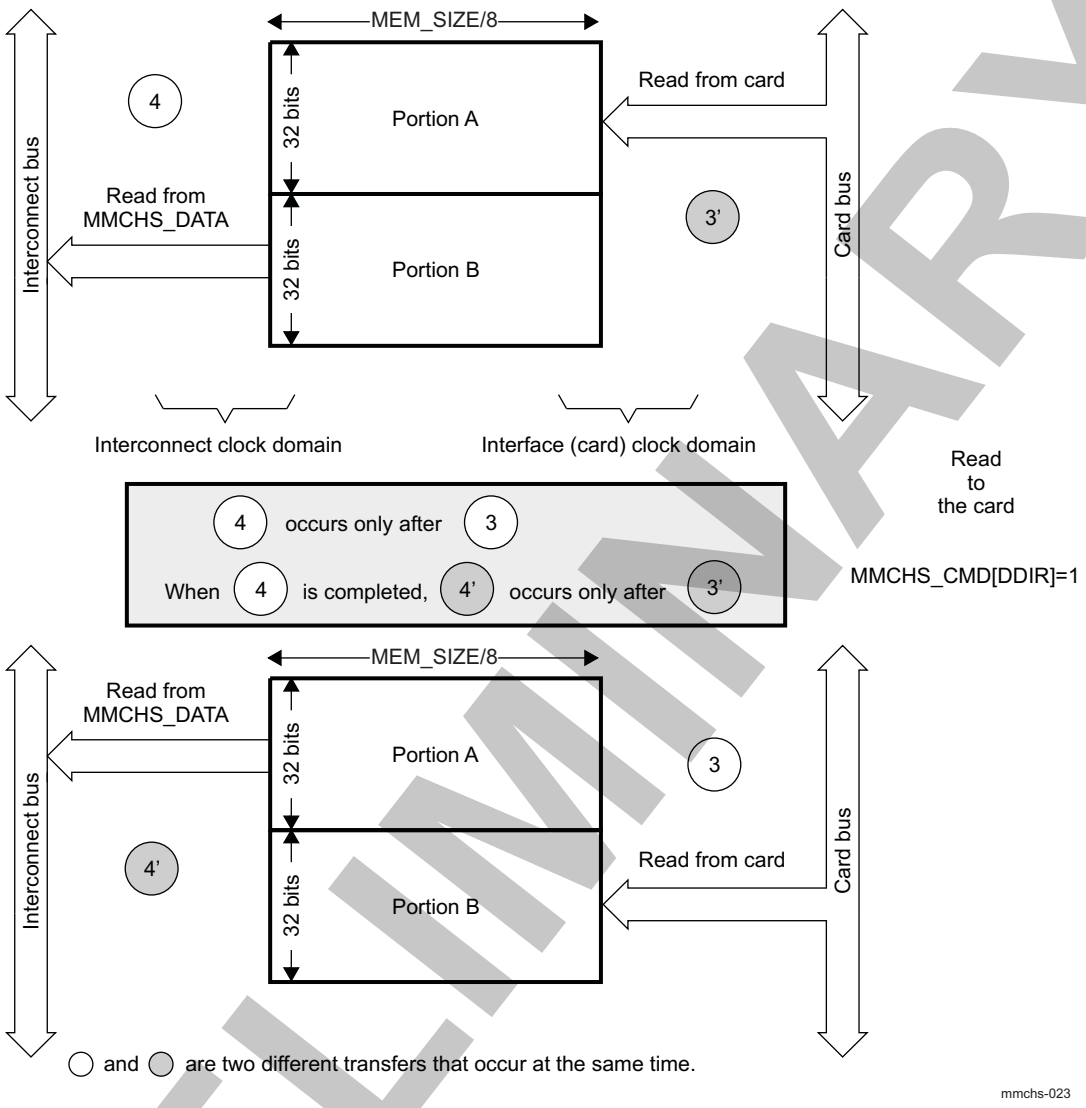
Figure 24-24. Buffer Management for a Read



- When the size of the data block to transfer is larger than MEM_SIZE / 2, only one data transfer at a time can occur from one data bus to the other data bus. The MMC/SDIOi host controller uses the entire data buffer as a single portion.

  In this mode, a bad access (the MMCi.MMCHS_STAT[29] BADA bit) is signaled when two data transfers occur at the same time from one data bus to the other data bus, and vice versa.

24.4.7.1.1 Memory Size, Block Length, and Buffer-Management Relationship

The maximum block length and buffer management that can be targeted by the system depend on the memory depth setting (see Table 24-17).

NOTE: Double-buffering is always the buffer management for large memory depth.

Table 24-17. Memory Size, BLEN, and Buffer Relationship

Memory Size (MMCHS_HL_HWINFO[5:2] MEM_SIZE in bytes)	**512**	**1024**
Maximum block length supported	512	1024

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Table 24-17. Memory Size, BLEN, and Buffer Relationship (continued)

Memory Size (MMCHS_HL_HWINFO[5:2] MEM_SIZE in bytes)	512	1024
Double-buffering for maximum block length	N/A	BLEN <= 512
Single-buffering for block length	BLEN <= 512	512 < BLEN <= 1024

NOTE: For single-buffering management, throughput on the MMC bus interface deteriorates in multiblock transfers, because the controller must wait for the filling or emptying of the buffer between each block transfer on the MMC bus. The clock is maintained on write MMC transfers (the MMCHS_CMD[4] DDIR bit is 0) and halted on read MMC transfers (the MMCHS_CMD[4] DDIR bit is 1).

24.4.7.1.2 Data Buffer Status

The data buffer status is defined in the following interrupt status register and status register:

- Interrupt status registers:
  - MMCi.MMCHS_STAT[29] BADA: Bad access to data space
  - MMCi.MMCHS_STAT[5] BRR: Buffer read ready
  - MMCi.MMCHS_STAT[4] BWR: Buffer write ready
- Status registers:
  - MMCi.MMCHS_PSTATE[11] BRE: Buffer read enable
  - MMCi.MMCHS_PSTATE[10] BWE: Buffer write enable

24.4.8 Transfer Process

The process of a transfer depends on the type of command. It can be with or without a response, and with or without data.

24.4.8.1 Different Types of Commands

Different types of commands are specific to the MMC, SD, and SDIO cards. For more information, see the *Multimedia Card System Specification*, *SD Memory Card Specifications*, *SDIO Card Specification, Part E1*; or *the SD Card Specification, Part A2, SD Host Controller Standard Specification*.

24.4.8.2 Different Types of Responses

Different types of responses are specific to the MMC, SD, and SDIO cards. For more information, see the *Multimedia Card System Specification*; *SD Memory Card Specifications*; *SDIO Card Specification, Part E1*, or the *SD Card Specification, Part A2, SD Host Controller Standard Specification*.

Table 24-18 describes how the MMC, SD, and SDIO responses are stored in the MMCHS_RSPxx registers.

Table 24-18. MMC, SD, SDIO Responses in the MMCHS_RSPxx Registers

Type of Response	Response Field	Response Register
R1, R1b (normal response), R3, R4, R5, R5b, R6, R7	RESP[39:8](1)	MMCHS_RSP10[31:0]
R1b (Auto CMD12 response), R1(Auto CMD23 response)	RESP[39:8](1)	MMCHS_RSP76[31:0]
R2	RESP[127:0](1)	MMCHS_RSP76[31:0] MMCHS_RSP54[31:0] MMCHS_RSP32[31:0] MMCHS_RSP10[31:0]

(1) RESP refers to the command response format described in the specifications mentioned.

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When the host controller modifies part of the MMCHS_RSPxx registers, it preserves the unmodified bits.

The host controller stores the Auto CMD12 response in the MMCHS_RSP76[31:0] register because the host controller may execute multiple block data transfers on the DATA line concurrently with a command. This allows the host controller to avoid overwriting the response of Auto CMD12 with the command response stored in the MMCHS_RSP10 register, and vice versa.

While executing Auto CMD23 the response of CMD23 is saved in the MMCHS_RSP76[31:0] register and the response of multiple-block read and write command is saved in the MMCHS_RSP10 register. The response error of CMD23 is indicated in the MMCHS_AC12 register, bits [7:0].

24.4.9 Transfer or Command Status and Errors Reporting

Flags in the MMC/SDIOi host controller show the status of communication with the card:

- A time-out (of a command, data, or response)
- A CRC error

Error conditions generate interrupts. For more information, see Table 24-19 and the register description.

Table 24-19. CC and TC Values Upon Error Detected

Error Hold in MMCi.MMCHS_STAT		CC	TC	Comments
29	BADA			No dependency with CC or TC BADA is related to the MMCHS_DATA register accesses. Its assertion does not depend on the ongoing transfer.
28	CERR	1		CC is set upon CERR.
22	DEB		1	TC is set upon DEB.
21	DCRC		1	TC is set upon DCRC.
20	DTO			DTO and TC are mutually exclusive. DCRC and DEB cannot occur with DTO.
19	CIE	1		CC is set upon CIE.
18	CEB	1		CC is set upon CEB.
17	CCRC	1		CC can be set upon CCRC. See CTO comment.
16	CTO			CTO and CC are mutually exclusive. CIE, CEB, and CERR cannot occur with CTO. CTO can occur at the same time as CCRC: It indicates a command abort due to contention on the CMD line. In this case no CC appears.

A MMCHS_STAT[20] DTO event can be asserted in the following conditions:

- Busy time-out for R1b, R5b response type
- Busy time-out after write CRC status
- Write CRC status time-out
- Read data time-out
- Boot acknowledge time-out

24.4.9.1 Busy Time-Out for R1b, R5b Response Type

Figure 24-25 shows the DTO event condition asserted when there is a busy time-out for Rb1, R5b response.

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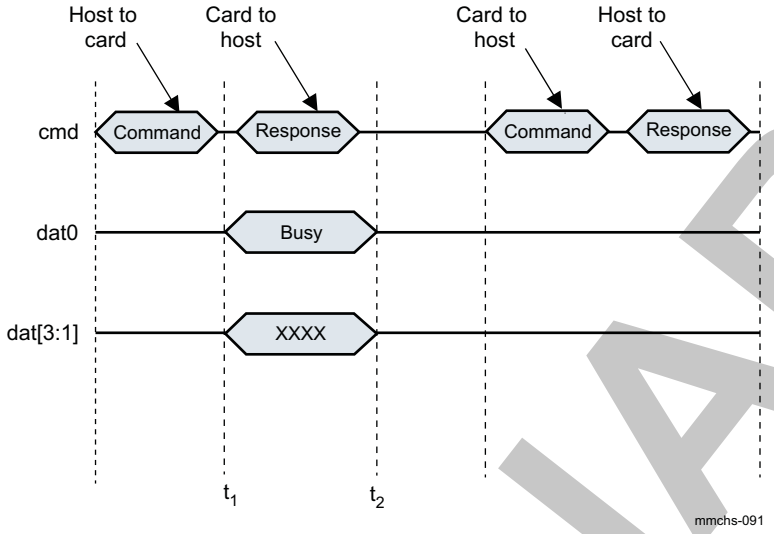
Figure 24-25. Busy Time-Out for R1b, R5b Response Type



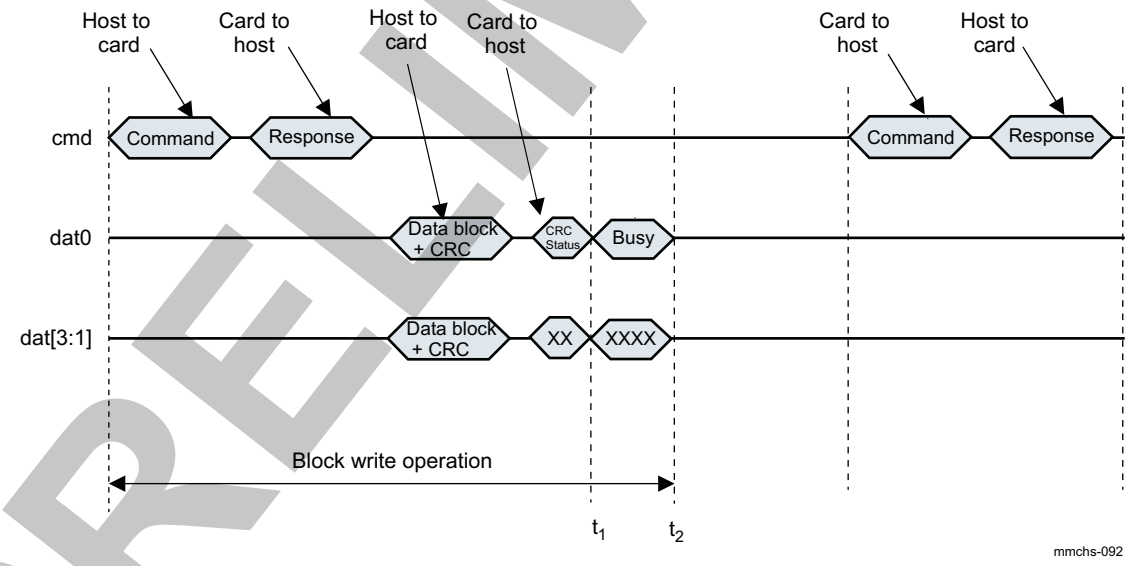
t_1 – Data time-out counter is loaded and starts after R1b, R5b response type.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

24.4.9.2 Busy Time-Out After Write CRC Status

Figure 24-26 shows the DTO event condition asserted when there is a busy time-out after write CRC status.

Figure 24-26. Busy Time-Out After Write CRC Status



t_1 – Data time-out counter is loaded and starts after CRC status.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

24.4.9.3 Write CRC Status Time-Out

Figure 24-27 shows the DTO event condition asserted when there is a write CRC status time-out.

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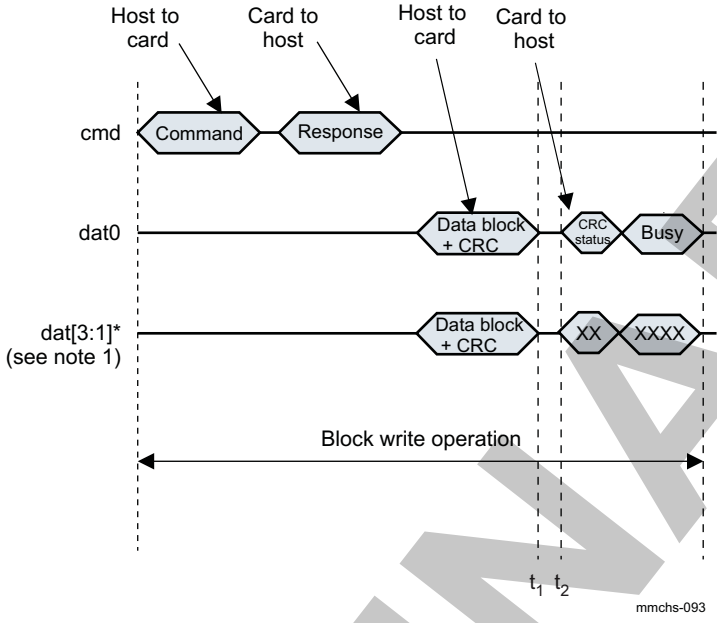
Figure 24-27. Write CRC Status Time-Out



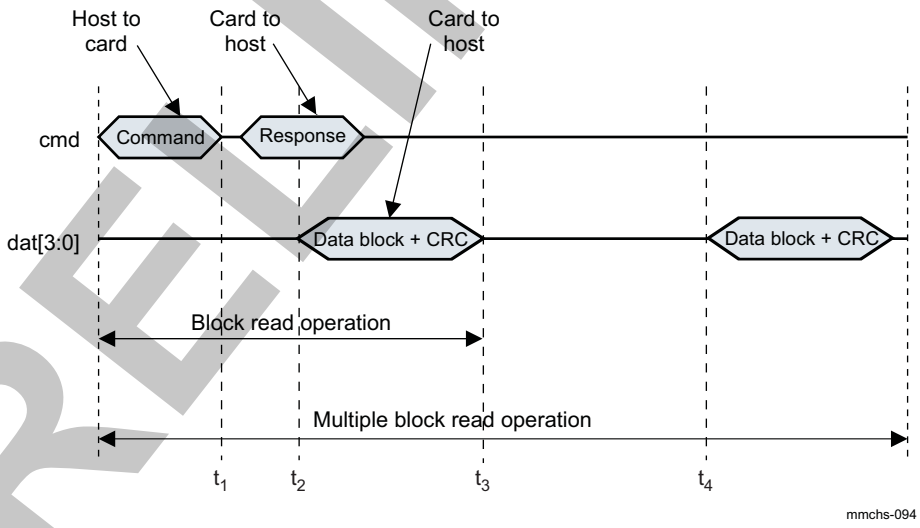
t_1 – Data time-out counter is loaded and starts after data block + CRC.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

24.4.9.4 Read Data Time-Out

Figure 24-28 shows the DTO event condition asserted when there is a read data time-out.

Figure 24-28. Read Data Time-Out



t_1 – Data time-out counter is loaded and starts after command transmission.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

t_3 – Data time-out counter is loaded and starts after data block + CRC transmission.

t_4 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

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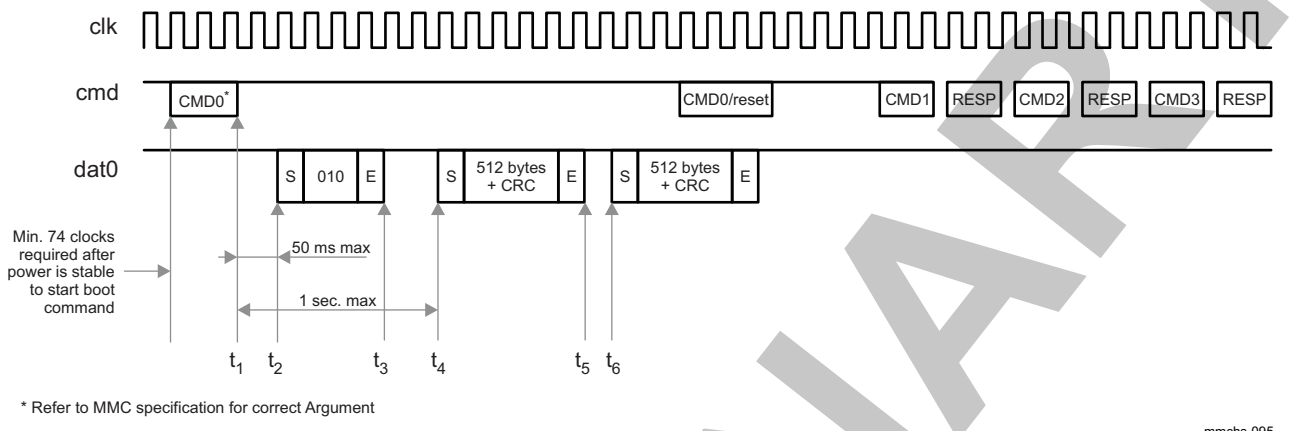
24.4.9.5 Boot Acknowledge Time-Out

Figure 24-29 shows the DTO event condition asserted when there is a boot acknowledge time-out and CMD0 is used.

Figure 24-29. Boot Acknowledge Time-Out When Using CMD0



t_1 – Data time-out counter is loaded and starts after CMD0.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

t_3 – Data time-out counter is loaded and starts.

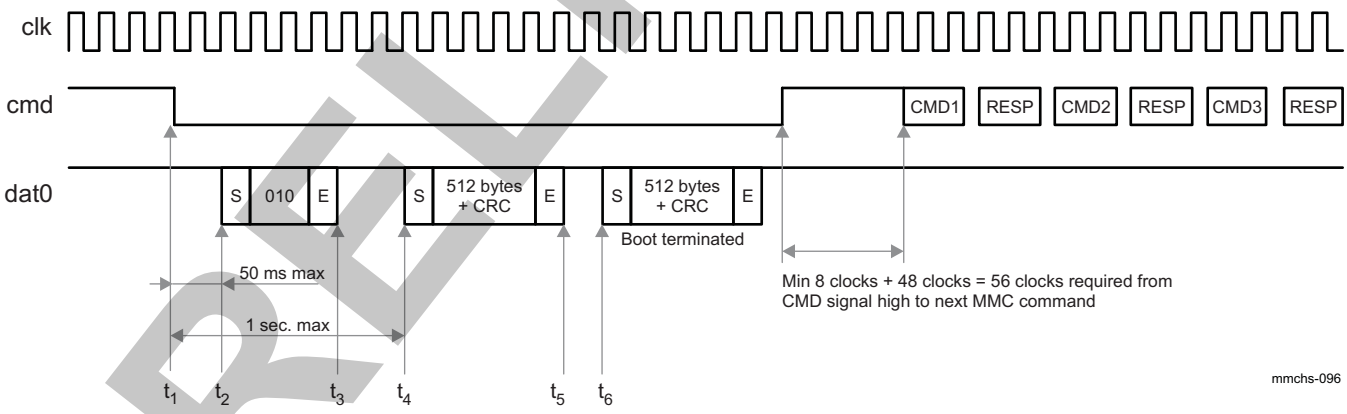
t_4 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

t_5 – Data time-out counter is loaded and starts after data + CRC transmission.

t_6 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

Figure 24-30 shows the DTO event condition asserted when there is a boot acknowledge time-out when the CMD line is tied to 0.

Figure 24-30. Boot Acknowledge Time-Out When CMD Line Tied to 0



t_1 – Data time-out counter is loaded and starts after the CMD line is tied to 0.

t_2 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

t_3 – Data time-out counter is loaded and starts.

t_4 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

t_5 – Data time-out counter is loaded and starts after data + CRC transmission.

t_6 – Data time-out counter stops and if it is 0, the MMCHS_STAT[20] DTO bit is generated.

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24.4.10 Auto Command 12 Timings

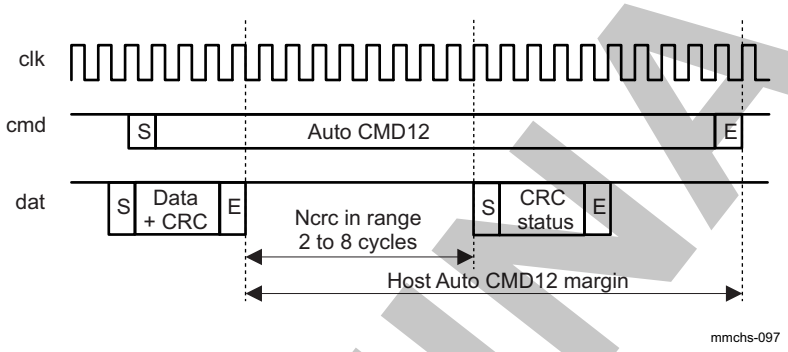
With the UHS definition of SD cards with higher frequency for MMC clock up to 208, the SD standard imposes a specific timing for the arrival of the auto command 12 (Auto CMD12) end bit.

24.4.10.1 Auto CMD12 Timings During Write Transfer

A margin named Ncrc in the range of two to eight cycles has been defined for SDR50 and SDR104 card components for write data transfers, because the Auto CMD12 end bit must arrive after the CRC status end bit.

Figure 24-31 shows the Auto CMD12 timings during write transfer.

Figure 24-31. Auto CMD12 Timings During Write Transfer



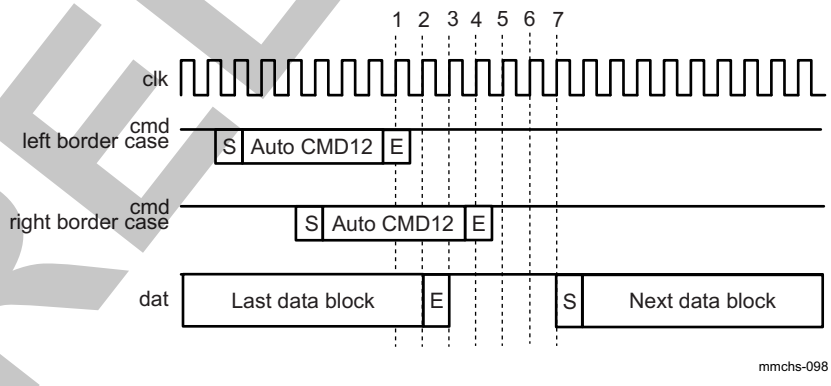
The host controller has a margin of 18 clock cycles to enure that the Auto CMD12 end bit arrives after the CRC status. This margin does not depend on the MMC/SD bus configuration, DDR, or standard transfer, 1-, 4-, or 8-bit bus width.

24.4.10.2 Auto CMD12 Timings During Read Transfer

With UHS cards, the gap timing between two successive cards is extended from two cycles to four cycles. It provides more flexibility for the host Auto CMD12 arrival to receive the last complete and reliable block. The MMCHS controller follows only the left border case defined by the SD UHS specification.

Figure 24-32 shows Auto CMD12 timings during read transfer.

Figure 24-32. Auto CMD12 Timings During Read Transfer



The Auto CMD12 arrival sent by the host controller is not sensitive to the MMC/SD bus configuration, whether it is a DDR or standard transfer and whether it is a 1-, 4-, or 8-bit bus width transfer.

24.4.11 Transfer Stop

Whenever a transfer is initiated, the transmission can be stopped before it finishes. Several cases are possible, depending on the transfer type:

- Multiple-block-oriented transfers (transfer length is known)

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- Continuous stream transfers (transfer has an infinite length)

NOTE: Because the MMC/SDIOi controller manages transfers based on a block granularity, the buffer accepts a block only if there is enough space to store it completely. Consequently, if a block is pending in the buffer, no command is sent to the card because the card clock will be shut off by the controller.

The MMC/SDIOi controller includes three features that make a transfer stop more convenient and easier to manage:

- Auto CMD12/Auto CMD23 (for eMMC and SD only):

  Auto CMD12/Auto CMD23 feature is enabled by setting the MMCi.MMCHS_CMD[3:2] ACEN bit field to 0x1 or to 0x2 respectively (this setting is relevant for an MMC/SD transfer with a known number of blocks to transfer). When the Auto CMD12/Auto CMD23 feature is enabled, the MMC/SDIOi controller automatically issues a CMD12/CMD23 command when the expected number of blocks is exchanged.
- Stop at block gap:

  This feature is enabled by setting the MMCi.MMCHS_HCTL[16] SBGR bit to 0x1. When enabled, this capability holds the transfer on until the end of a block boundary. If a stop transmission is needed, software can use this pause to send a CMD12 to the card.
- ADMA mode:

  For ADMA-capable modules (MMC1 and MMC2) (for more information, see Section 24.4.5, *DMA Modes*), the last instruction can stop the transfer (the END bit is enabled in the descriptor line).

NOTE: For MMC and SD cards, the stop-at-block-gap feature is not supported in read mode.

For SDIO cards, this setting can be supported in read mode if the card has read-wait capability.

NOTE: In SDR104 mode Auto CMD23 is used to stop multiple block read/write operation instead of Auto CMD12. In the other bus speed modes, if the card supports CMD23, Auto CMD23 is used instead of Auto CMD12.

Table 24-20 shows the common way to stop a transfer, indicating the command to send and the features to enable.

Table 24-20. MMC/SDIOi Controller Transfer Stop Command Summary

		Write Transfer		Read Transfer	
		SD/MMC	SDIO	SD/MMC	SDIO
Single block		Transfer ends automatically. Wait TC.	Transfer ends automatically. Wait TC.	Transfer ends automatically. Wait TC.	Transfer ends automatically. Wait TC.
Multiblocks (finite or infinite)	Before the programmed block boundary	Send CMD12/CMD23. Wait TC.	Send CMD52. Wait TC.	Send CMD12/CMD23. Wait TC.	Send CMD52. Wait TC.
	Stop at the end of the transfer (finite transfer only)	Auto CMD12/Auto CMD23 active. Transfer ends automatically. Wait TC.	Set MMCi.MMCHS_HCTL[16] SBGR bit to 0x1. Send CMD52. Wait TC.	Auto CMD12/Auto CMD23 active. Transfer ends automatically. Wait TC.	**If READ_WAIT supported** Stop at block gap. Wait TC.
					If READ_WAIT not supported Send CMD52. Wait TC.

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NOTE: The MMC/SDIOi controller sends the stop command to the card on a block boundary, regardless of when the command was written to the controller registers.

24.4.12 Retention Mode

This mode is enabled if the generic parameter bit MMCHS_HL_HWINFO[6] RETMODE is set to 1 during module integration. The controller can enter into retention mode when the module was previously set in idle mode. When the module goes into retention mode all clocks are left inactive at low level except for registers that are driven by a falling-edge clock, which are kept as free during retention mode. This also means that all divided functional clock subdomains are forced low when the module enters smart-idle mode. In force-idle mode, the system must ensure that all divided functional clocks are set inactive or are in bypass mode by configuring the MMCHS_SYSCTL register correctly before entering idle mode (under software responsibility).

24.4.13 Output Signals Generation

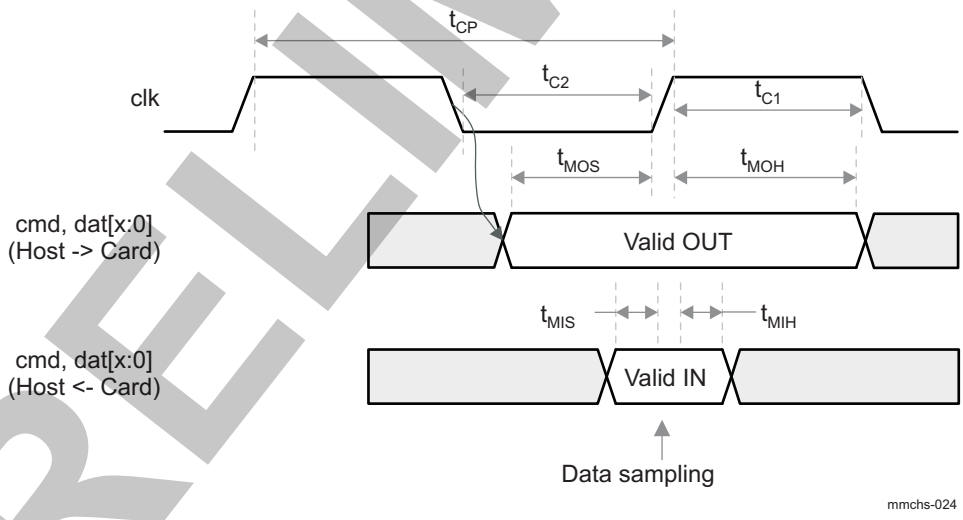
The MMC/SDIO output signals can be driven on the falling edge or rising edge, depending on the MMCHS_HCTL[2] HSPE bit. This feature allows achieving better timing performance, thus increasing data transfer frequency.

24.4.13.1 Generation on Falling Edge of MMC Clock

The controller defaults to this mode to maximize hold timings. In this case, the MMCHS_HCTL[2] HSPE bit is set to 0.

Figure 24-33 shows the output signals of the module when generating from the falling edge of the MMC clock.

Figure 24-33. Output Driven on Falling Edge



24.4.13.2 Generation on Rising Edge of MMC Clock

This mode increases setup timings and allows reaching higher bus frequency. This feature is activated by setting the MMCHS_HCTL[2] HSPE bit to 1. The controller must be set in this mode to support SDR transfers.

NOTE: Do not use this feature in DDR mode (when the MMCHS_CON[19] DDR bit is set to 1).

Figure 24-34 shows the output signals of the module when generating from the rising edge of the MMC clock.

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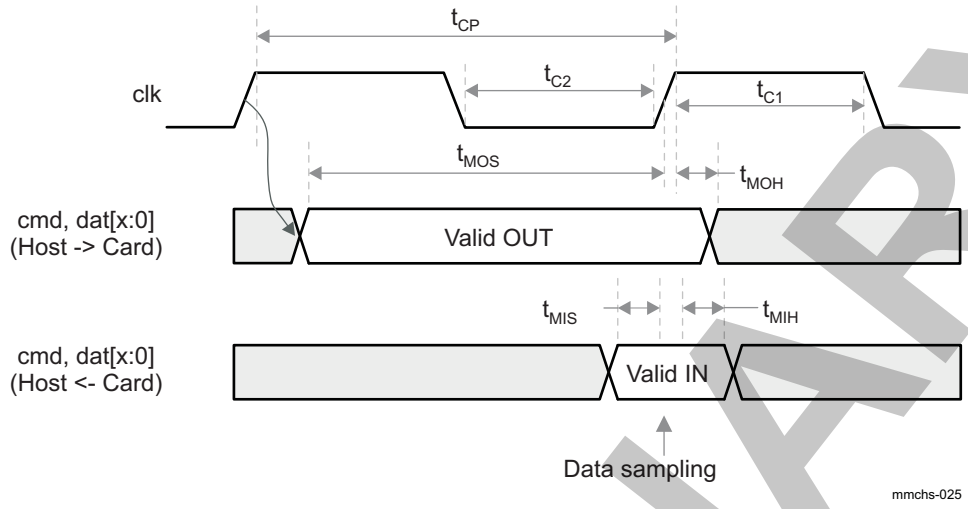
Figure 24-34. Output Driven on Rising Edge



24.4.14 Sampling Clock Tuning

In UHS-I mode the SD bus operates in high clock frequency mode and the data window from the card on CMD and DAT lines get smaller. The position of the data window varies depending on the card and the host system. To adjust the sampling clock when SDR104/HS200 operation mode is used the MMC/SDIOi host controller supports a tuning circuit. This tuning circuit is a dedicated DLL which delays the clock signal used for data sampling. The DLL is not part of the MMC/SDIOi host controller. It is instantiated at top level between the IOs and the host controller. There are two DLLs. One for MMC1 when SDR104 mode is used and one for MMC2 when HS200 mode is used.

In the default, lower frequency operation, a fixed sampling clock is used to receive signals on CMD and DAT lines. Before using the SDR104/HS200 or SDR50 (if MMCHS_CAPA2[13] TSDR50 = 0x1) modes software must execute the tuning procedure at the initialization sequence regardless of MMCHS_CAPA2[15:14] RTM value.

The software starts the tuning sequence by setting MMCHS_AC12[22] ET to 1. Then it issues CMD19 for a SD card or CMD21 for an eMMC device repeatedly until MMCHS_AC12[22] ET is set to 0. MMCHS_AC12[22] ET is reset when the tuning is complete or when the tuning is not complete within 40 tries. The software may abort this loop if the number of the loops reaches 40 or 150ms timeout occurs. In this case a fixed sampling clock is used and MMCHS_AC12[23] SCLK_SEL is set to 0. This indicates that the tuning procedure is failed. When MMCHS_AC12[23] SCLK_SEL is set to 1, this indicates that the tuning procedure is completed successfully. For more information about the DLL tuning procedure, see Section 24.5.1.2.4, *SDR104/HS200 DLL Tuning Procedure*.

24.4.15 Card Boot Mode Management

Boot operation mode lets the MMC/SDIOi host controller read boot data from the connected slave (MMC device) by keeping the CMD line low after power on (or sending CMD0 with a specific argument) before issuing CMD1. The data can be read from the boot area or user area, depending on the register setting.

Power-on boot defines a way for the boot code to be accessed by the MMC/SDIOi host controller without an upper-level software driver, thus speeding the time it takes for a controller to access the boot code.

The two possible ways to issue a boot command (issuing a CMD0 or driving the CMD line to 0 during the whole boot phase) are described in the following sections.

24.4.15.1 Boot Mode Using CMD0

Figure 24-35 shows the timing diagram of a boot sequence using CMD0.

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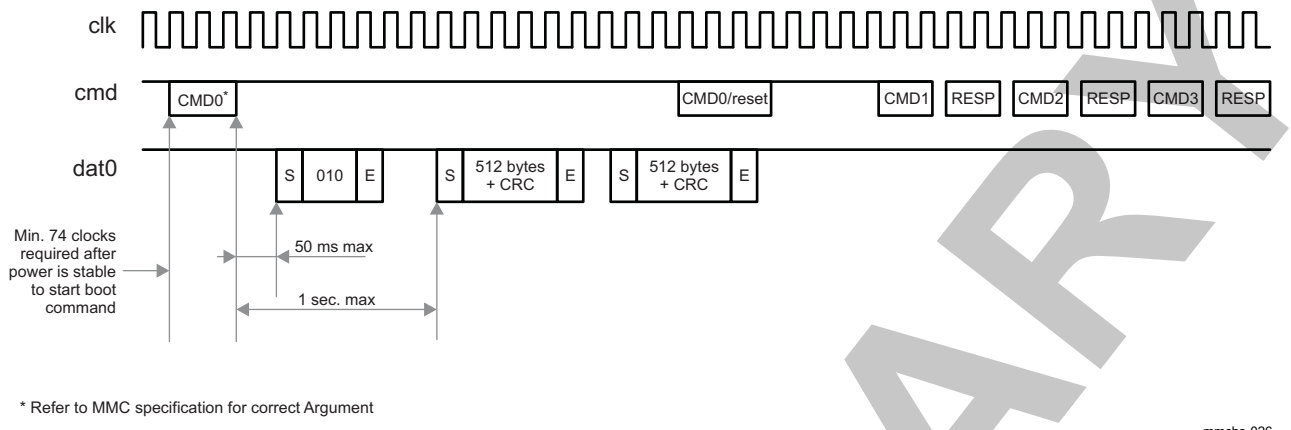
Figure 24-35. Boot Mode Using the CMD0 Timing Diagram



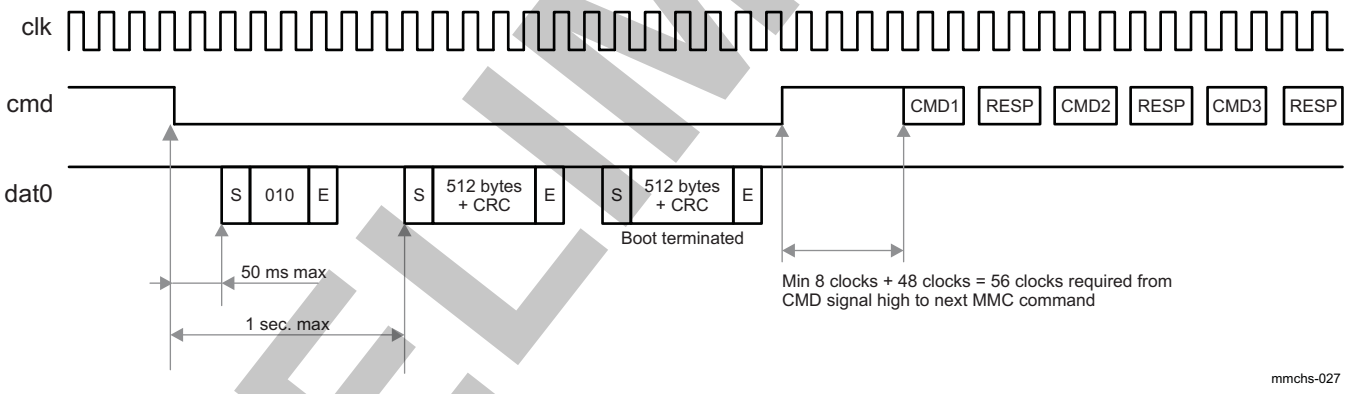
NOTE: Refer to MMC specification for correct Argument.

For more information about how to configure the MMC/SDIO host controller, see Section 24.5.1.2.3.1, *Boot Using the CMD0*.

24.4.15.2 Boot Mode With CMD Line Tied to 0

Figure 24-36 shows the timing diagram of a boot sequence with CMD line tied to 0.

Figure 24-36. Boot Mode With CMD Line Tied to 0 Timing Diagram



For more information about how to configure the MMC/SDIO host controller, see Section 24.5.1.2.3.2, *Boot With CMD Line Tied to 0*.

24.4.16 MMC CE-ATA Command Completion Disable Management

The MMC/SDIOi host controller supports CE-ATA features, in particular the detection of the command completion token. When a command that requires a CCS (the MMCHS_CON[12] CEATA bit is set to 1 and the MMCHS_CMD[3:2] ACEN bit field is set to 0x1) is launched, the host system is no longer allowed to emit a new command in parallel to the data transfer unless it is a command completion disable token.

The settings to emit a command completion disable token are:

- Set the MMCHS_CON[12] CEATA bit to 1.
- Set the MMCHS_CON[2] HR bit to 1.
- Clear the MMCHS_ARG register.
- Write into the MMCHS_CMD register with the value 0x00000000.

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When a command completion disable token was emitted (that is, the MMCHS_STAT[0] CC bit is received), the host system is again allowed to emit another type of command (for example, a CMD12 to abort transfer).

A critical case can be encountered when CCSD is emitted during the last data block transfer, and the sequence on the command line is sent close to the CCS token sent by the card.

Three possible cases are:

- CCS is received immediately before CCSD is emitted:

  An interrupt CIRQ is generated when CCS is detected, CCSD is transmitted to the card, and then an interrupt CC is generated when CCSD ends. In this case, the card considers the CCSD sequence.
- CCS is not generated or is generated during the CCSD transfer:

  The CCS bit cannot be detected (conflict is not possible because they drive the same level on the command line, and no CIRQ interrupt is generated; a CC interrupt is generated when CCSD ends).
- CCS is generated without CCSD token required:

  Only the interrupt CIRQ is generated when CCS is detected.

24.4.17 Test Registers

Test registers are available to comply with the *SD Host Controller Specification*. This feature is useful to generate interrupts manually for driver debugging.

The force event register (MMCHS_FE) is used to control the error status and error interrupt status for Auto CMD12 and Auto CMD23.

The system test register (MMCHS_SYSTEST) is used to control the signals that connect to I/O pins when the module is configured in the system test mode (the MMCHS_CON[4] MODE bit = 1) for boundary connectivity verification.

The MMCHS_HCTL[7] CDSS and MMCHS_HCTL[6] CDTL bits enable manual control of MMCHS_PSTATE[16] CINS and interrupt generating indicated in MMCHS_STAT[7] CREM and MMCHS_STAT[6] CINS.

24.4.18 MMC/SDIO Hardware Status Features

Table 24-21 describes the MMC/SDIO hardware status features.

Table 24-21. MMC/SDIO Hardware Status Features

Feature	Type	Register/Bit Field	Description
Interrupt flags		See Section 24.4.4, *Interrupt Requests.*	
CMD line signal level	Status	MMCHS_PSTATE[24] CLEV	Indicates the level of the command line
DAT lines signal level	Status	MMCHS_PSTATE[23:20] DLEV	Indicates the level of the data lines
Write protect switch pin level	Status	MMCHS_PSTATE[19] WP	Indicates whether the SD card is write protected or not.
Card detect pin level	Status	MMCHS_PSTATE[18] CDPL	Indicates the level of the sdcard_cd signal/pad
Card State Stable	Status	MMCHS_PSTATE[17] CSS	Used for testing. Indicates sdcard_cd stable state
Card inserted	Status	MMCHS_PSTATE[16] CINS	Indicates whether the SD card is inserted
Buffer read enable	Status	MMCHS_PSTATE[11] BRE	Readable data exists in the buffer.
Buffer write enable	Status	MMCHS_PSTATE[10] BWE	Indicates whether there is enough space in the buffer to write BLEN bytes of data
Read transfer active	Status	MMCHS_PSTATE[9] RTA	Used to detect completion of a read transfer.
Write transfer active	Status	MMCHS_PSTATE[8] WTA	Indicates a write transfer active
Re - Tuning Request	Status	MMCHS_PSTATE[3] RTR	Indicates whether the sampling clock needs re - tuning or not.
Data line active	Status	MMCHS_PSTATE[2] DLA	Indicates whether the data lines are active

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Table 24-21. MMC/SDIO Hardware Status Features (continued)

Feature	Type	Register/Bit Field	Description
Command Inhibit (DAT lines)	Status	MMCHS_PSTATE[1] DATI	Indicates whether issuing of command using data lines is allowed
Command inhibit (CMD line)	Status	MMCHS_PSTATE[0] CMDI	Indicates whether issuing of command using command line is allowed

Table 24-22 describes the MMC/SDIO preset value features.

Table 24-22. MMC/SDIO Preset Value Registers

Feature	Type	Register	Description
Preset value register	Status	MMCHS_PVINITSD	Preset Values for Initialization and Default Speed modes
Preset value register	Status	MMCHS_PVHSSDR12	Preset Values for High Speed and SDR12 speed modes
Preset value register	Status	MMCHS_PVSDR25SDR50	Preset Values for SDR25 and SDR50 speed modes
Preset value register	Status	MMCHS_PVSDR104DDR50	Preset Values for SDR104 and DDR50 speed modes

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24.5 MMC/SDIO Programming Guide

24.5.1 Low-Level Programming Models

24.5.1.1 Global Initialization

24.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the module must be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the MMC/SDIO modules. For more information, see Section 24.3, *MMC/SDIO Integration*, and Section 24.2, *MMC/SDIO Environment*.Table 24-23 shows the global initialization of surrounding modules.

Table 24-23. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. See Section 3.1.1, in Chapter 3, *Power, Reset, and Clock Management*.
Control module	Module-specific pad muxing and configuration must be set in the control module. See Chapter 18, *Control Module* .
(optional) MPU INTC (or DSP INTC)	MPU INTC configuration must be done to enable the interrupts from the MMCHS module. See Chapter 17, *Interrupt Controllers*.
(optional) DMA_SYSTEM (or DDMA)	DMA configuration must be done to enable the module DMA channel requests. See Chapter 16, *System DMA*.

NOTE: The MPU/DSP INTC and the DMA_SYSTEM/dDMA configurations are necessary if the interrupt and DMA-based communication modes are used.

24.5.1.1.2 MMC/SDIO Host Controller Initialization Flow

Table 24-24 shows the general boot process.

Table 24-24. MMC/SDIO Controller Meta Initialization Steps

Step	Access Type	Register/Bit Field/Programming Model	Value
Initialize clocks.		See Section 24.5.1.1.2.1, *Enable Interface and Functional Clock for MMC Controller.*	
Software reset of the controller.		See Section 24.5.1.1.2.2, *MMCHS Soft Reset Flow*.	
Set module hardware capabilities.		See Section 24.5.1.1.2.3,*Set MMCHS Default Capabilities*.	
Set module idle and wake-up modes.		See Section 24.5.1.1.2.4, *Wake-Up Configuration*.	

24.5.1.1.2.1 Enable Interface and Functional Clock for MMC Controller

Before any MMCHS register access, the MMCHS interface clock and functional clock in the PRCM module registers must be enabled. See Section 3.6.4.5, *Clock Domain Module Attributes*, in Chapter 3, *Power, Reset, and Clock Management*.

24.5.1.1.2.2 MMCHS Soft Reset Flow

Figure 24-37 shows the soft reset process of the MMCHS controller.

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Figure 24-37. MMC/SDIO Controller Software Reset Flow

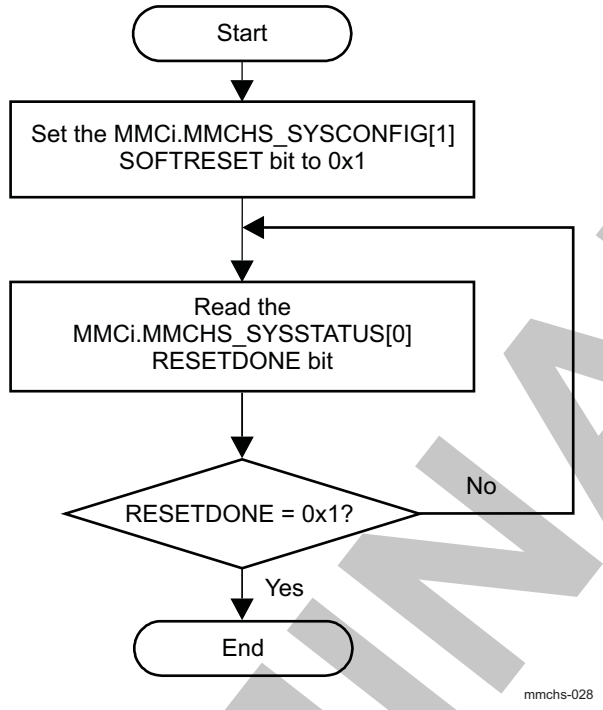

Table 24-25. Register Call Summary for Main Sequence – Software Reset Flow

Register Name	Register Name
MMCHS_SYSCONFIG	MMCHS_SYSSTATUS

24.5.1.1.2.3 Set MMCHS Default Capabilities

Software must read capabilities (in boot ROM, for example) and is allowed to set (write) the MMCi.MMCHS_CAPA[26:24] and MMCi.MMCHS_CUR_CAPA[23:0] bit fields before the MMC/SDIO host driver is started.

24.5.1.1.2.4 Wake-Up Configuration

Table 24-26 describes the MMCHS controller wake-up configuration.

Table 24-26. MMC/SDIO Controller Wake-Up Configuration

Step	Access Type	Register/Bit Field/Programming Model	Value
Configure wake-up bit (if necessary).	W	MMCi.MMCHS_SYSCONFIG[2] ENAWAKEUP	0x1
Enable wake-up events on SD card interrupt (if necessary).	W	MMCi.MMCHS_HCTL[24] IWE	0x1
SDIO card only: Enable card interrupt (if necessary).	W	MMCi.MMCHS_IE[8] CIRQ_ENABLE	0x1

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24.5.1.1.2.5 MMC Host and Bus Configuration

Figure 24-38 shows the MMC bus configuration process.

Figure 24-38. MMC/SDIO Controller Bus Configuration

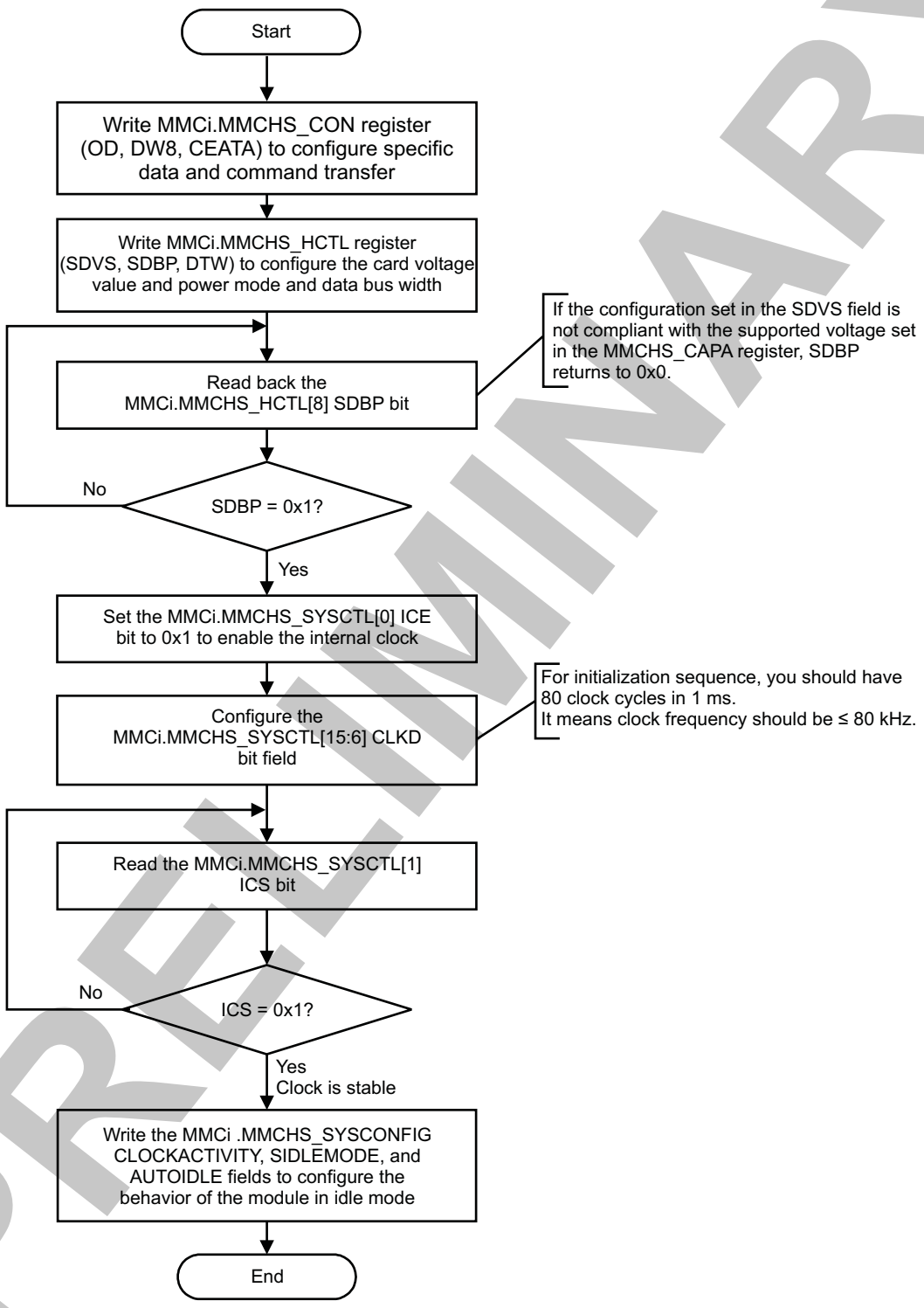

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Table 24-27. Register Call Summary for Main Sequence – Bus Configuration

Register Name	Register Name
MMCHS_CON	MMCHS_HCTL
MMCHS_SYSCONFIG	MMCHS_SYSCTL

24.5.1.2 Operational Modes Configuration

24.5.1.2.1 Basic Operations for MMC/SDIO Host Controller

The MMC/SDIO host controller performs data transfers: data to card (referred to as write transfers) and data from card (referred to as read transfers).

The host controller requires transfers to run on a block-by-block basis rather than on a DMA burst size basis. A single DMA request (or block request interrupt) is signaled for each block. Pipelining is supported as long as the block size is less than one half of the memory buffer size.

24.5.1.2.1.1 Card Detection, Identification, and Selection

Figure 24-39 and Figure 24-40 show the card detection, identification and selection process.

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Figure 24-39. MMC/SDIO Controller Card Identification and Selection – Part 1

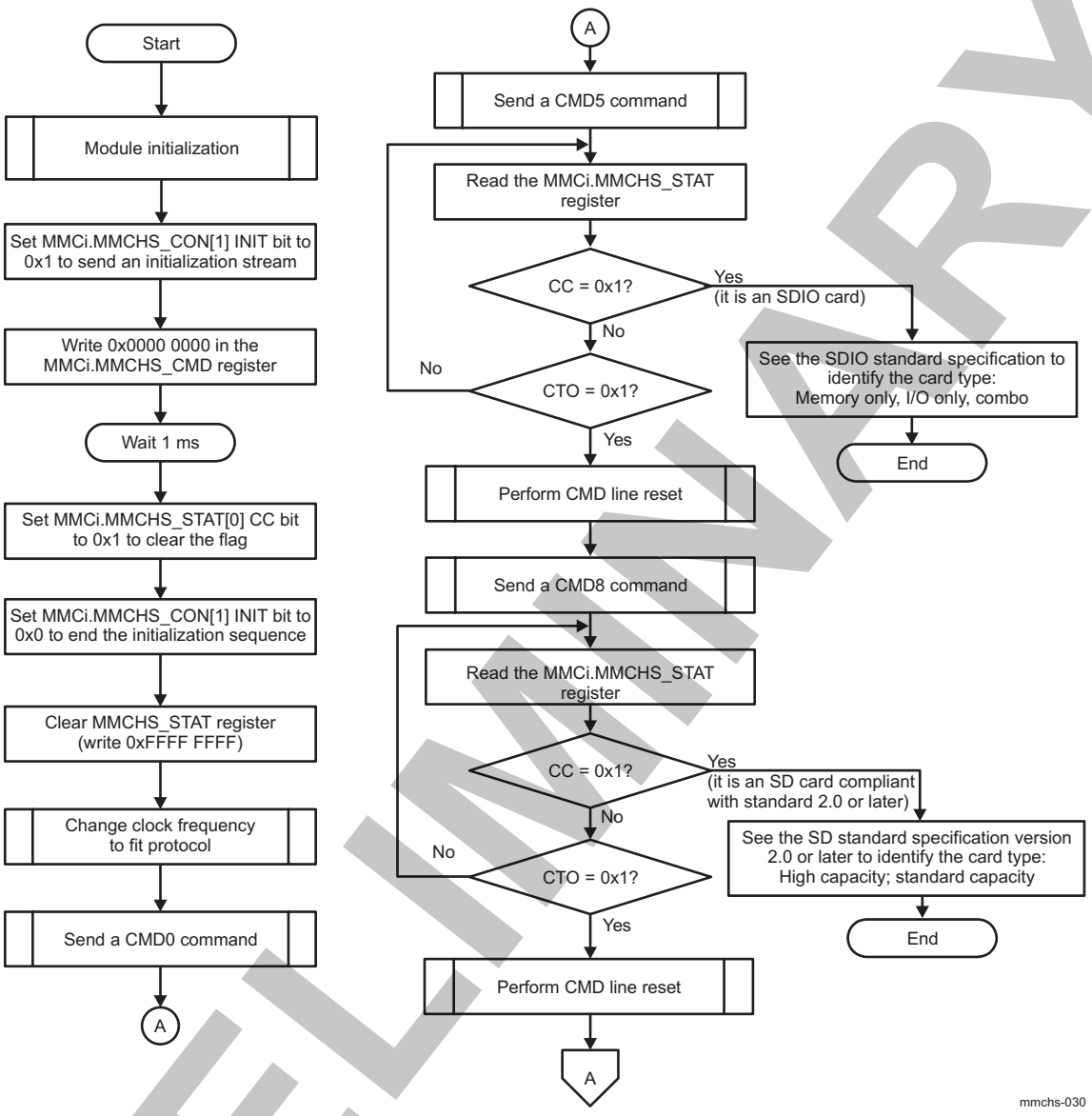

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Figure 24-40. MMC/SDIO Controller Card Identification and Selection – Part 2

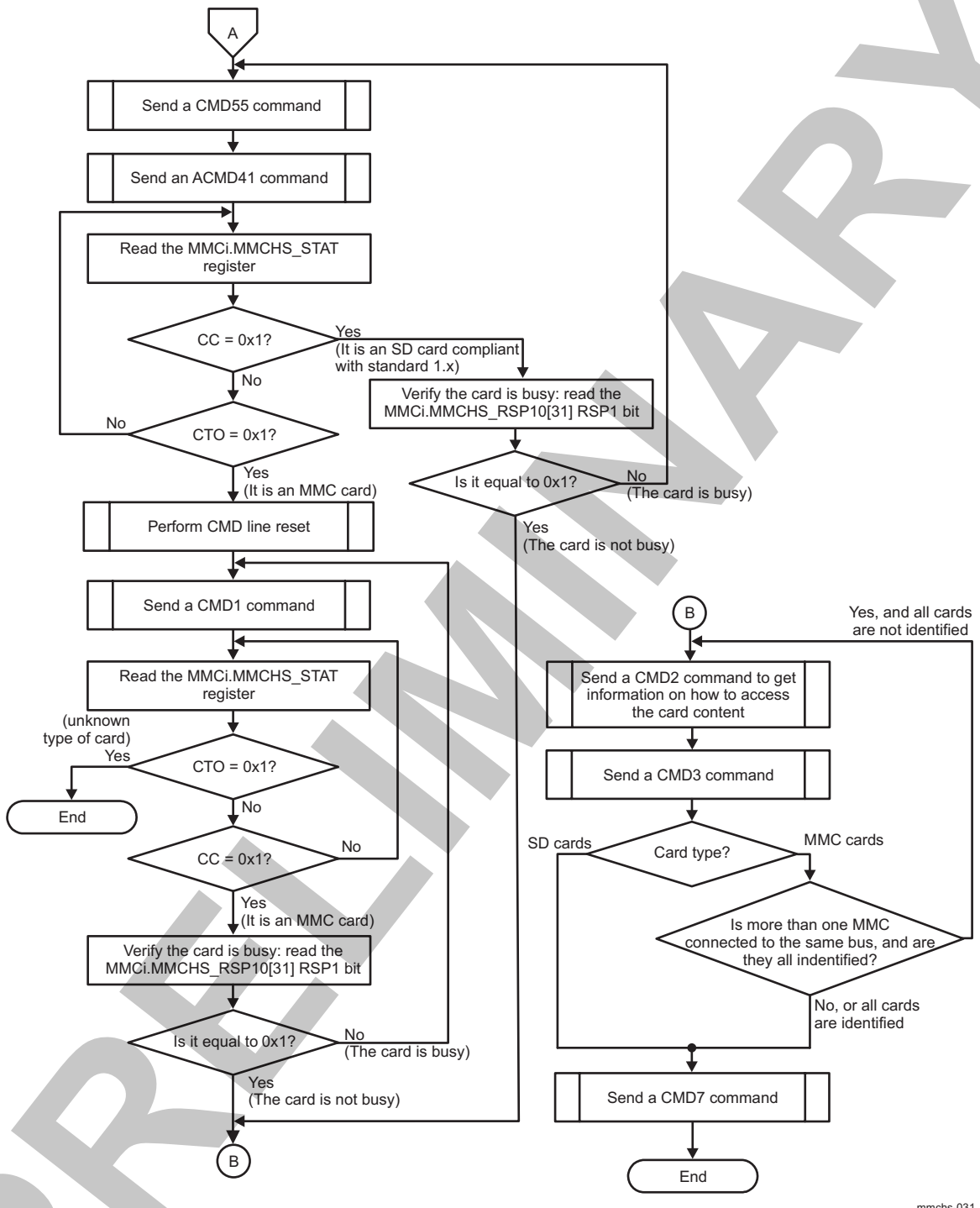

Table 24-28. Register Call Summary for Main Sequence – Card Identification and Selection

Register Name	Register Name	Register Name
MMCHS_CON	MMCHS_CMD	MMCHS_STAT
MMCHS_SYSCTL	MMCHS_RSP10	

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Table 24-29 lists the subprocess call summary.

Table 24-29. Subprocess Call Summary for Main Sequence – Card Identification and Selection

Subprocess Name	Cross-Reference
Initialize module.	See Section 24.5.1.1.2 , *MMC/SDIO Host Controller Initialization Flow*.
Change clock frequency to fit protocol.	See Section 24.5.1.2.1.7.2, *MMCHS Clock Frequency Change*.
Send a command.	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.
Perform CMD line reset.	See Section 24.5.1.2.1.1.1, *CMD Line Reset Procedure*.

24.5.1.2.1.1.1 CMD Line Reset Procedure

Table 24-30lists the CML line reset.

Table 24-30. CMD Line Reset

Step	Access Type	Register/Bit Field/Programming Model	Value
Initiate CMD line reset.	W	MMCi.MMCHS_SYSCTL[25] SRC	0x1
Poll the SRC bit until it is set to 0x1.	R	MMCi.MMCHS_SYSCTL[25] SRC	= 0x1
Wait until the SRC bit returns to 0x0 (reset procedure is completed).	R	MMCi.MMCHS_SYSCTL[25] SRC	= 0x0

24.5.1.2.1.2 Read/Write Transfer Flow in DMA_SYSTEM Mode With Interrupt

Figure 24-41 shows the read and write protocol in DMA slave mode with interrupt signaling. For more information about the DMA settings, see Section 16.5, *DMA_SYSTEM Basic Programming Model*, in Chapter 16, *System DMA*.

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Figure 24-41. MMC/SDIO Controller Read/Write Transfer Flow in DMA Slave Mode With interrupt

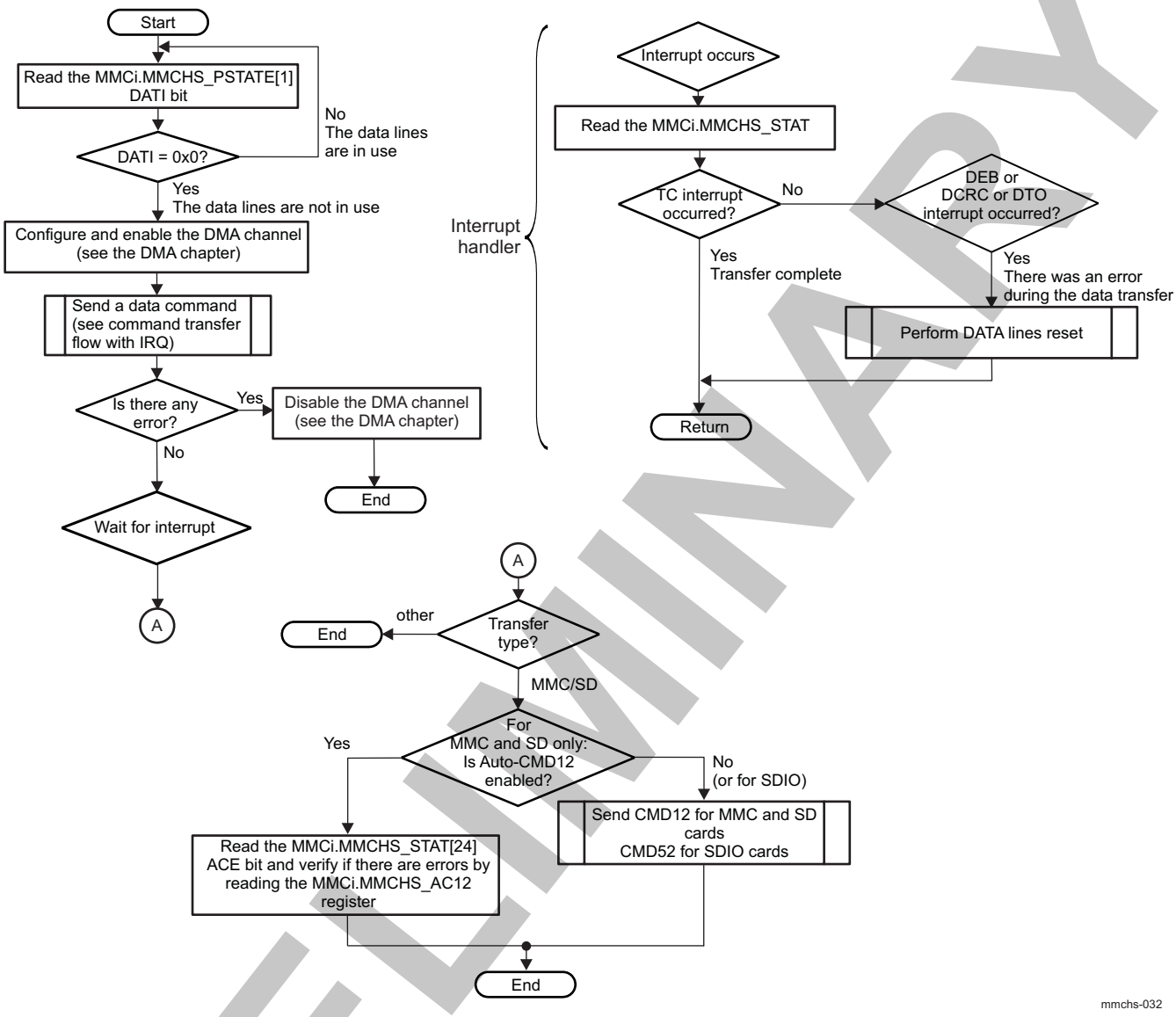

Table 24-31. Register Call Summary for Main Sequence – Read/Write Transfer Flow in DMA Mode With interrupt

Register Name	Register Name
MMCHS_PSTATE	MMCHS_STAT
MMCHS_SYSCTL	MMCHS_CMD

Table 24-32. Subprocess Call Summary for Main Sequence – MMC/SDIO Controller Read/Write Transfer Flow in DMA Mode With Interrupt

Subprocess Name	Cross-Reference
Send a data command.	See Figure 24-48.
Perform DATA lines reset.	See Section 24.5.1.2.1.2.1, *DATA Lines Reset Procedure*.

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24.5.1.2.1.2.1.1 DATA Lines Reset Procedure

Table 24-33 describes the DATA lines reset.

Table 24-33. DATA Lines Reset

Step	Access Type	Register/Bit Field/Programming Model	Value
Initiate DATA lines reset.	W	MMCi.MMCHS_SYSCTL[26] SRD	0x1
Poll the SRD bit until it is set to 0x1.	R	MMCi.MMCHS_SYSCTL[26] SRD	= 0x1
Wait until the SRD bit returns to 0x0 (reset procedure is complete).	R	MMCi.MMCHS_SYSCTL[26] SRD	= 0x0

24.5.1.2.1.3 Read/Write Transfer Flow in DMA_SYSTEM Mode With Polling

Figure 24-42 shows the read and write protocol in DMA mode. For more information about the DMA settings, see Section 16.5, *DMA_SYSTEM Basic Programming Model* in Chapter 16, *System DMA*.

Figure 24-42. MMC/SDIO Controller Read/Write Transfer Flow in DMA Mode With Polling

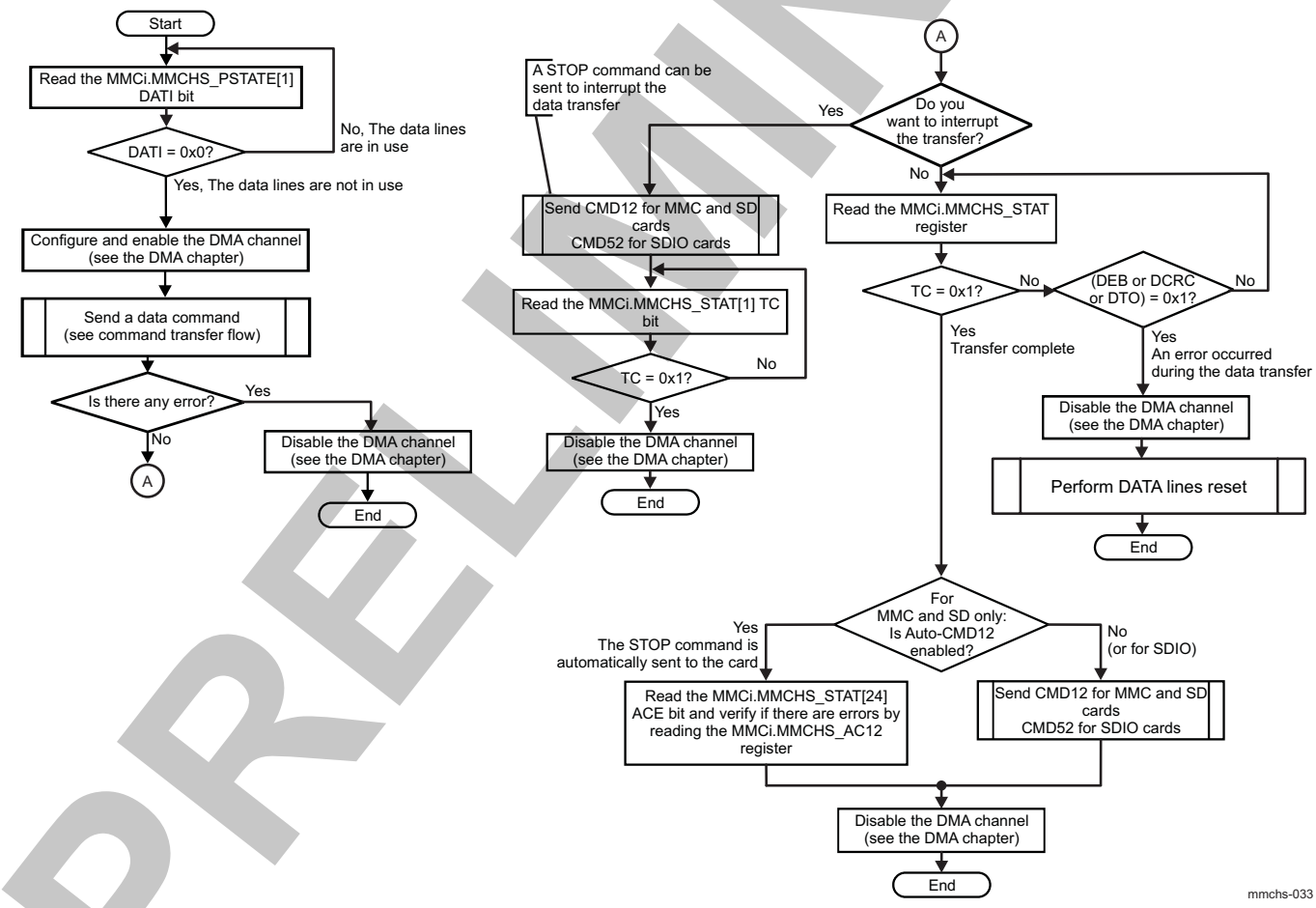

Table 24-34. Register Call Summary for Main Sequence – Read/Write Transfer Flow in DMA Mode With Polling

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_STAT	MMCHS_SYSCTL

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Table 24-34. Register Call Summary for Main Sequence – Read/Write Transfer Flow in DMA Mode With Polling (continued)

Register Name	Register Name	Register Name
MMCHS_CMD	MMCHS_AC12	

Table 24-35. Subprocess Call Summary for Main Sequence – Read/Write Transfer Flow in DMA Mode With Polling

Subprocess Name	Cross-Reference
Send command.	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.
Perform DATA lines reset.	See Section 24.5.1.2.1.2.1, *DATA Lines Reset Procedure*.

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24.5.1.2.1.4 Read/Write Transfer Flow Without DMA With Polling

Figure 24-43 shows a read/write transfer without using the DMA and with polling.

Figure 24-43. MMC/SDIO Controller Read/Write Transfer Flow Without DMA and With Polling

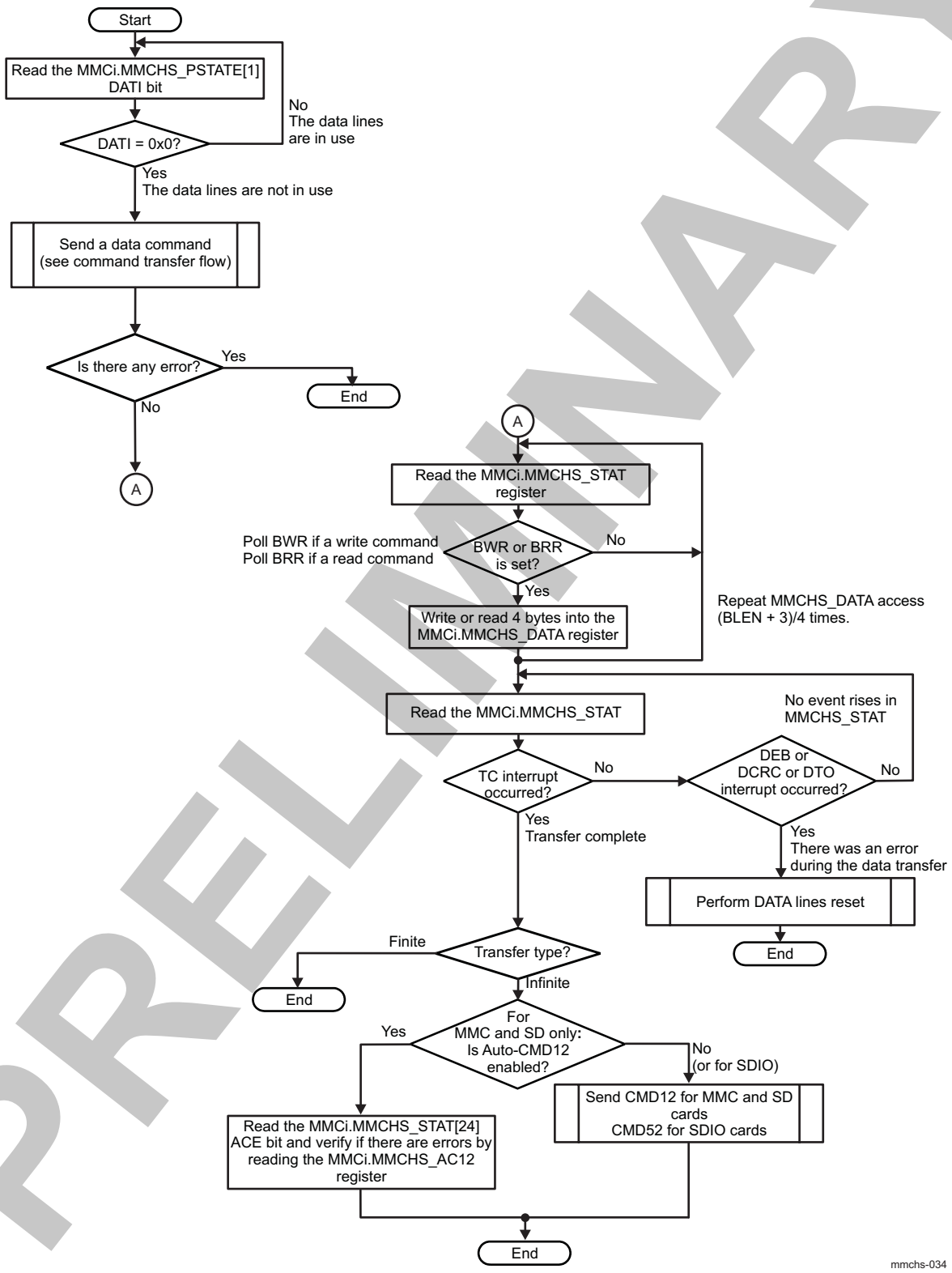

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Table 24-36. Register Call Summary for Main Sequence – Read/Write Transfer Flow Without DMA With Polling

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_DATA	MMCHS_STAT
MMCHS_SYSCTL	MMCHS_CMD	MMCHS_AC12

Table 24-37. Subprocess Call Summary for Main Sequence – Read/Write Transfer Flow Without DMA With Polling

Subprocess Name	Cross-Reference
Send data command.	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.
Perform DATA lines reset.	See Section 24.5.1.2.1.2.1, *DATA Lines Reset Procedure*.

24.5.1.2.1.5 Read/Write Transfer Flow in CE-ATA Mode

Figure 24-44 shows the read and write CE-ATA protocol when in polling mode.

Figure 24-44. MMC/SDIO Controller Read/Write in CE-ATA Mode

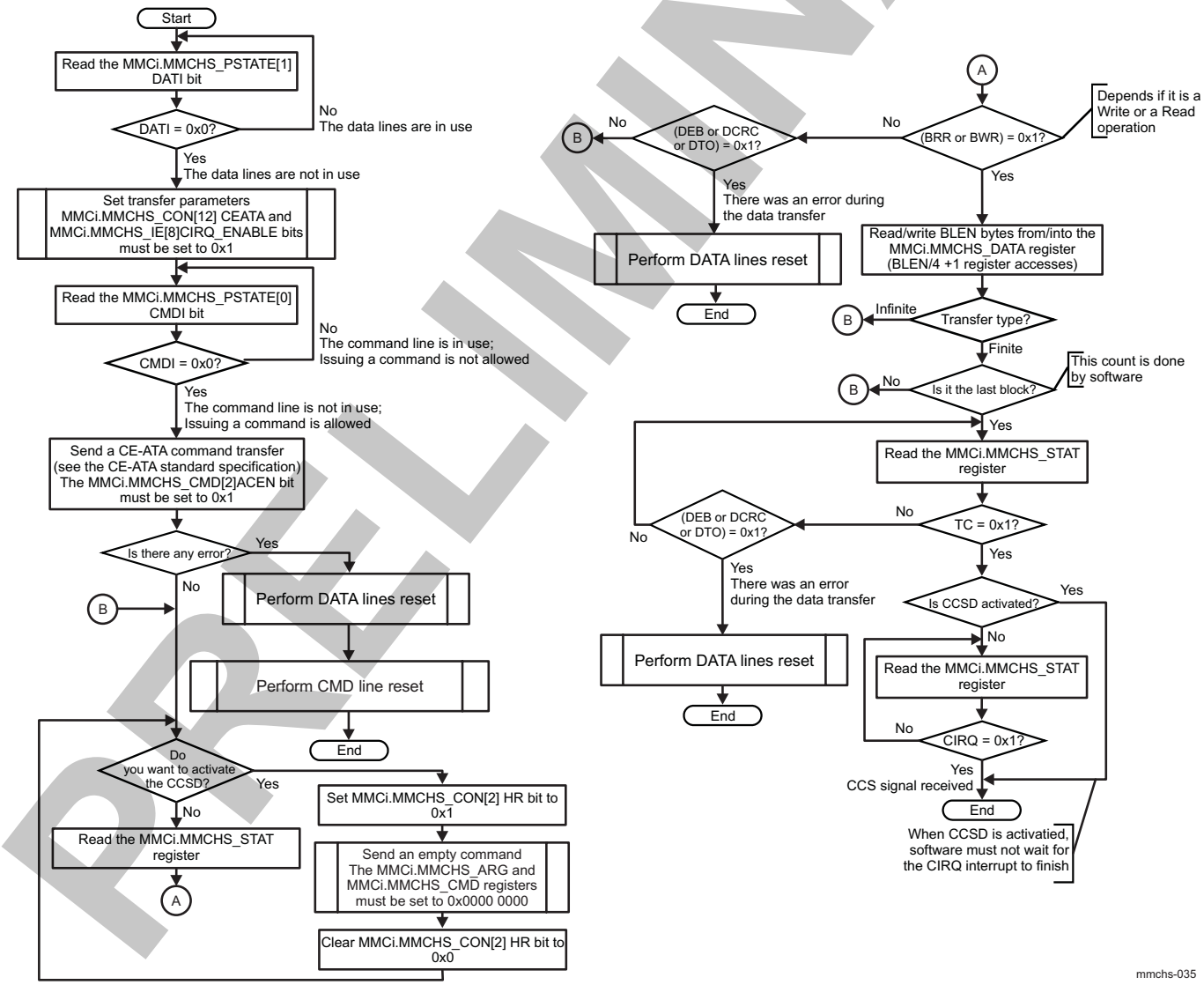

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Table 24-38. Register Call Summary for Main Sequence – Read/Write in CE-ATA Mode

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_CON	MMCHS_IE
MMCHS_CMD	MMCHS_STAT	
MMCHS_ARG	MMCHS_SYSCTL	

Table 24-39. Subprocess Call Summary for Main Sequence – Read/Write in CE-ATA Mode

Subprocess Name	Cross-Reference
Perform CMD line reset.	See Section 24.5.1.2.1.1.1, *CMD Line Reset Procedure*.
Perform DATA lines reset.	See Section 24.5.1.2.1.2.1, *DATA Lines Reset Procedure*.

CAUTION

CE-ATA protocol is supported only by MMC cards.

In CE-ATA mode, issuing a command during the transfer (except a CCSD command) is not allowed.

In CE-ATA mode, infinite transfers are not allowed; only finite transfers are permitted.

24.5.1.2.1.6 Suspend-Resume Flow

The suspend-and-resume feature is supported only by SDIO cards.

24.5.1.2.1.6.1 Suspend Flow

Figure 24-45 shows the suspend flow for SDIO cards.

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Figure 24-45. MMC/SDIO Controller Suspend Flow

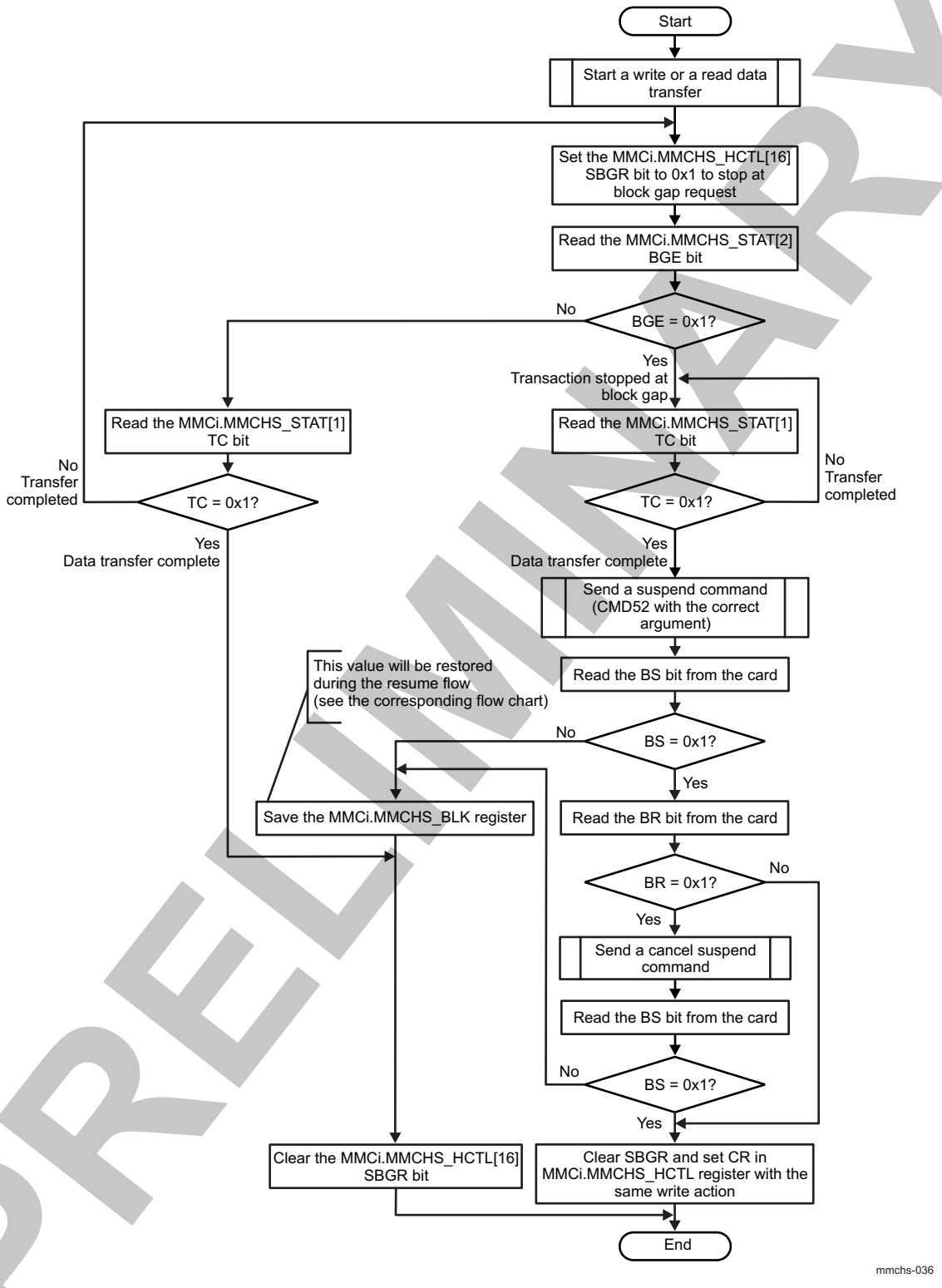

Table 24-40. Register Call Summary for Main Sequence – Suspend Flow

Register Name	Register Name	Register Name
MMCHS_HCTL	MMCHS_STAT	MMCHS_BLK

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Table 24-41. Subprocess Call Summary for Main Sequence – Suspend Flow

Subprocess Name	Cross-Reference
Start a write or a read data transfer.	See Section 24.5.1.2.1, *Basic Operations for MMC/SDIO Host Controller*.
Send a suspend command (CMD52 with the correct argument).	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.
Send a cancel suspend command.	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.

24.5.1.2.1.6.2 Resume Flow

Figure 24-46 shows the resume flow for SDIO cards.

Figure 24-46. MMC/SDIO Controller Resume Flow

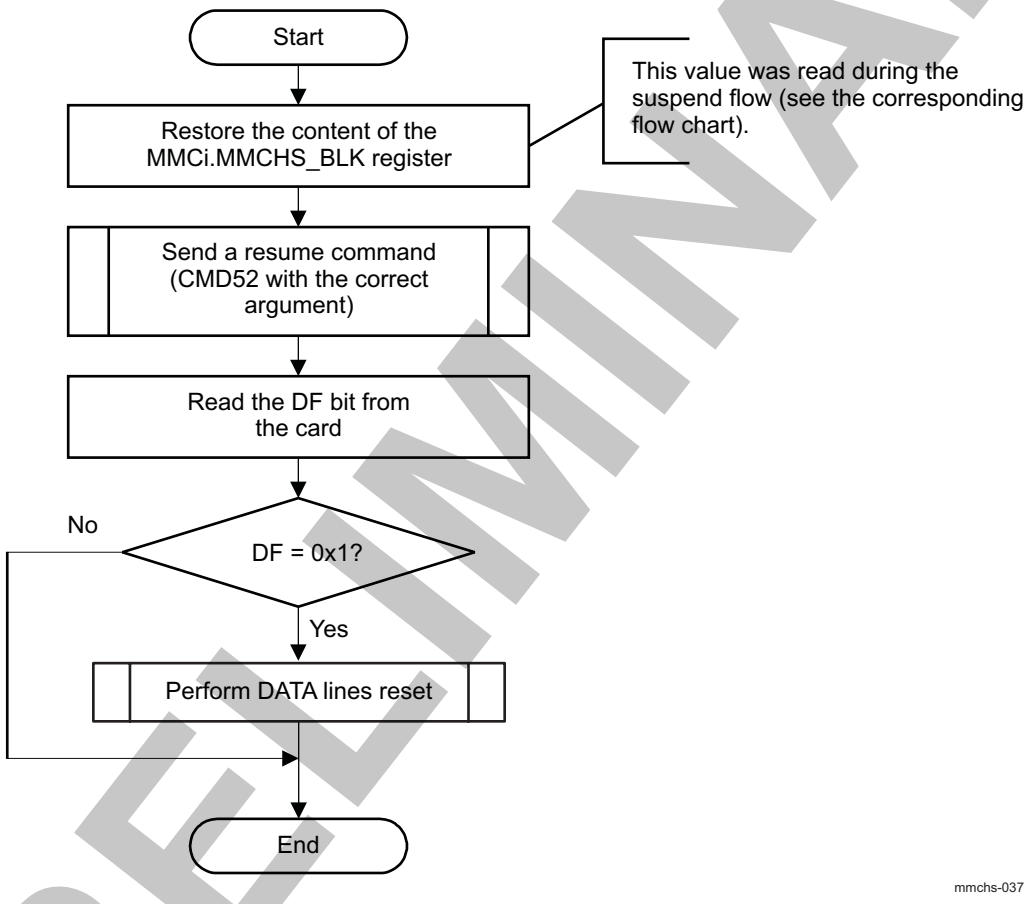

Table 24-42. Register Call Summary for Main Sequence - Resume Flow

Register Name	Register Name
MMCHS_BLK	MMCHS_SYSCTL

Table 24-43. Subprocess Call Summary for Main Sequence - Resume Flow

Subprocess Name	Cross-Reference
Send a resume command (CMD52 with the correct argument).	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.
Perform DATA lines reset.	See Section 24.5.1.2.1.2.1, *DATA Lines Reset Procedure*.

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24.5.1.2.1.7 Basic Operations – Steps Detailed

24.5.1.2.1.7.1 Command Transfer Flow

Figure 24-47 shows how to send a command to the card using polling instead of interrupts for event signaling.

Figure 24-47. MMC/SDIO Controller Command Transfer Flow With Polling

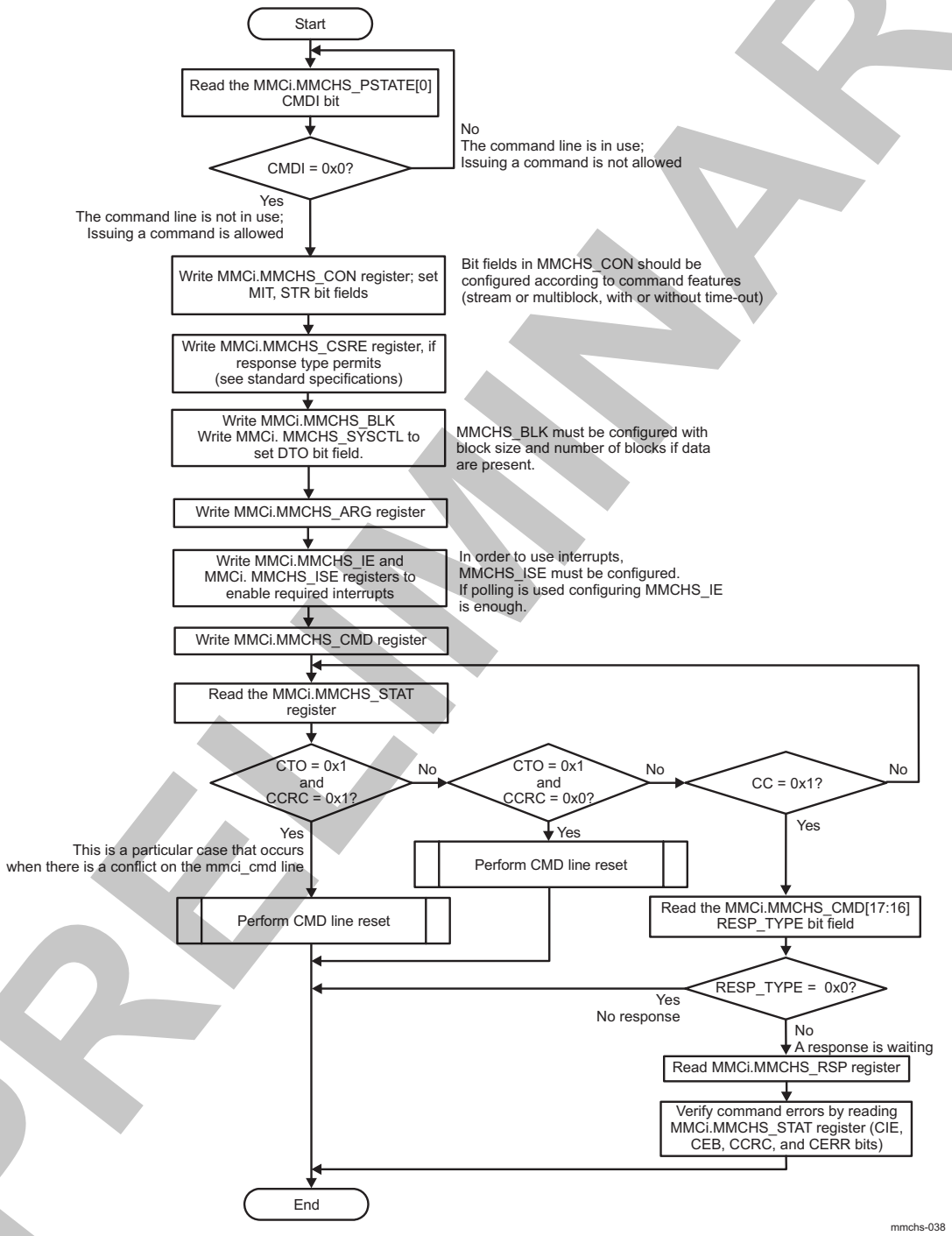

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Table 24-44. Register Call Summary for Main Sequence – Command Transfer Flow With Polling

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_CON	MMCHS_CSRE
MMCHS_STAT	MMCHS_BLK	MMCHS_SYSCTL
MMCHS_ARG	MMCHS_IE	MMCHS_CMD
MMCHS_RSP10	MMCHS_RSP32	MMCHS_RSP54
MMCHS_RSP76		

Table 24-45. Subprocess Call Summary for Main Sequence – Command Transfer Flow With Polling

Subprocess Name	Cross-Reference
Perform CMD line reset.	See Section 24.5.1.2.1.1.1, *CMD Line Reset Procedure*.

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Figure 24-48 shows how to send a command to the card using interrupts for event signaling.

Figure 24-48. MMC/SDIO Controller Command Transfer Flow With interrupts

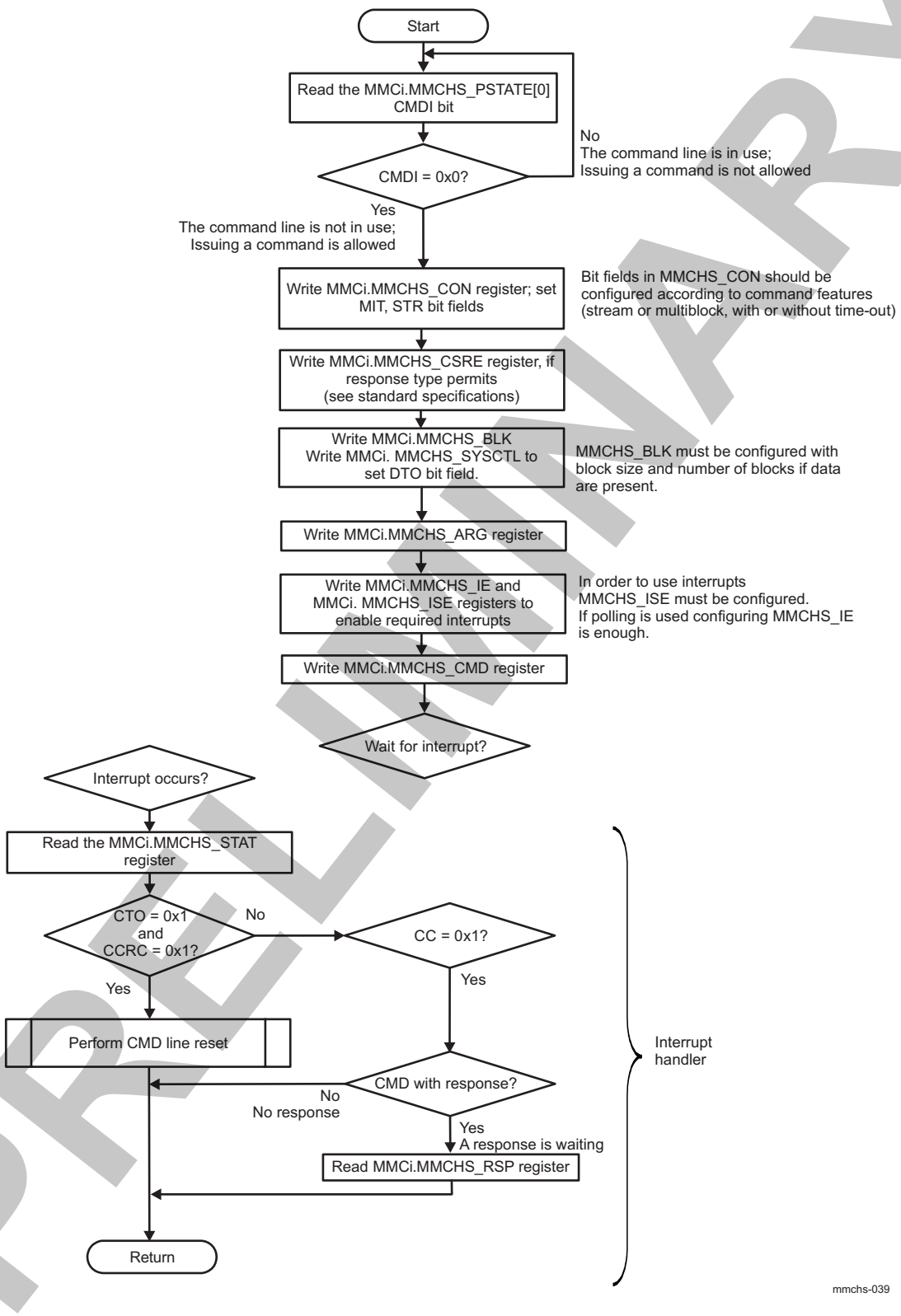

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Table 24-46. Register Call Summary for Main Sequence – Command Transfer Flow With Interrupts

Register Name	Register Name	Register Name
MMCHS_PSTATE	MMCHS_CON	MMCHS_CSRE
MMCHS_STAT	MMCHS_BLK	MMCHS_SYSCTL
MMCHS_ARG	MMCHS_IE	MMCi.MMCHS_ISE
MMCHS_RSP10	MMCHS_RSP32	MMCHS_RSP54
MMCHS_RSP76	MMCHS_CMD	

Table 24-47. Subprocess Call Summary for Main Sequence – Command Transfer Flow With Interrupts

Subprocess Name	Cross-Reference
Perform CMD line reset.	See Section 24.5.1.2.1.1.1, *CMD Line Reset Procedure*.

24.5.1.2.1.7.2 MMCHS Clock Frequency Change

Figure 24-49 shows the different steps that allow changing the MMC/SDIO output clock frequency.

Figure 24-49. MMC/SDIO Controller Clock Frequency Change Flow

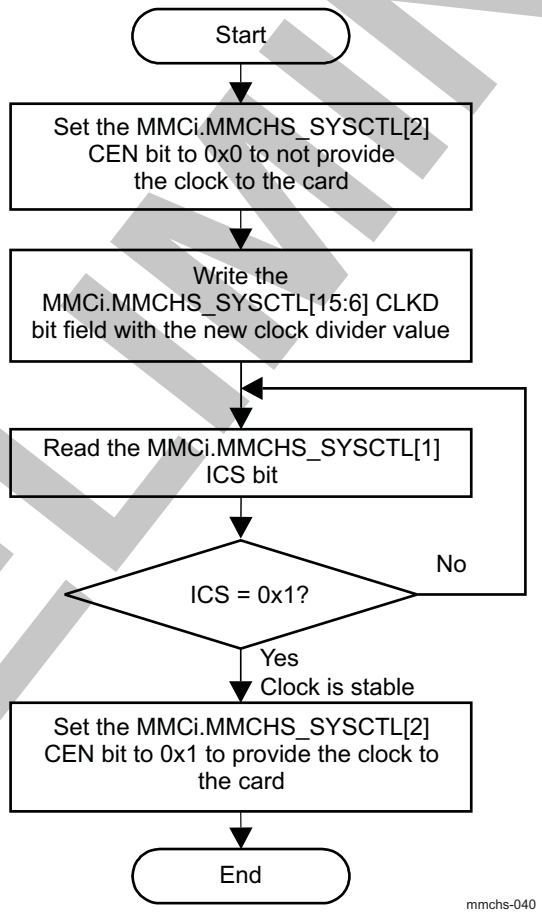

Table 24-48. Register Call Summary for Main Sequence – Clock Frequency Change Flow

Register Name
MMCHS_SYSCTL

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24.5.1.2.1.7.3 Bus Width Selection

Figure 24-50 shows the different steps that allow changing the MMC/SDIO bus width.

Figure 24-50. MMC/SDIO Controller Bus Width Configuration Flow

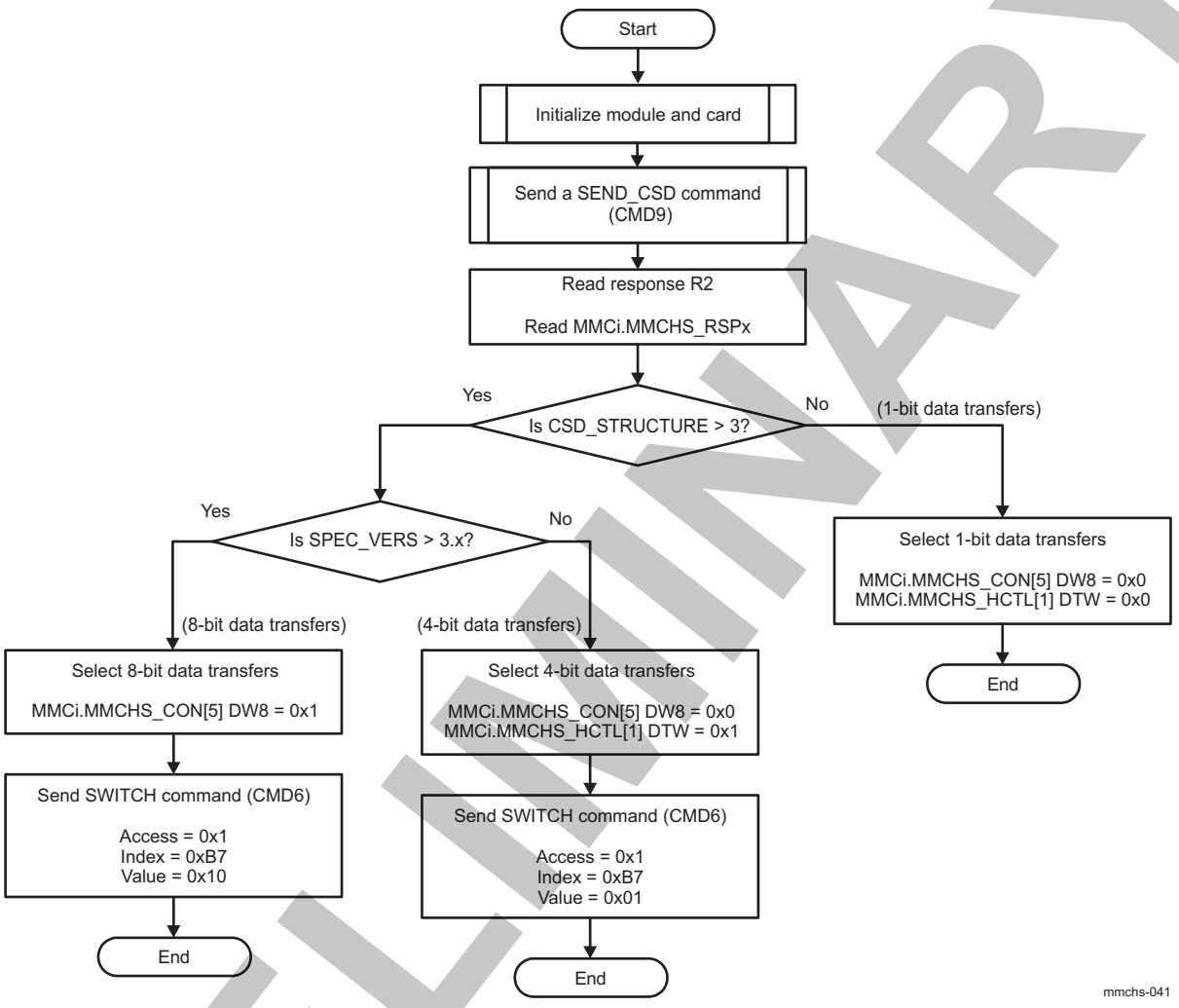

Table 24-49. Register Call Summary for Main Sequence – Bus Width Configuration Flow

Register Name	Register Name	Register Name
MMCHS_RSP10	MMCHS_RSP32	MMCHS_RSP54
MMCHS_RSP76	MMCHS_CON	MMCHS_HCTL

Table 24-50. Subprocess Call Summary for Main Sequence – Bus Width Configuration Flow

Subprocess Name	Cross-Reference
Initialize module and card.	See Section 24.5.1.1.2, *MMC/SDIO Host Controller Initialization Flow*. See Section 24.5.1.2.1.1, *Card Detection, Identification, and Selection*.
Send a SEND_CSD command (CMD9).	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.
Send SWITCH command (CMD6).	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.

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24.5.1.2.2 Bus Voltage Selection

The MMC/SDIO1 controller can operate with two types of card voltages: 1.8 V and 3.0 V. For this reason, dual voltage pads are implemented on this interface. For technological concerns, those pads must have an internal bias voltage reference to operate. The PBIAS module supplies this bias voltage, depending on the settings of the CTRL_MODULE_CORE_PAD.CONTROL_PBIAS register and the value of MMCHS_AC12[19] V1V8_SIGEN bit.

For more information about the PBIAS cell, see Section 18.4.9, *Extended-Drain I/O and PBIAS Cell*, in Chapter 18, *Control Module*.

CAUTION

The BIAS voltage must be set using the procedure described in *Section 18.5.1.2.1, Extended-Drain I/Os and PBIAS Cell Programming Guide*, in Chapter 18, *Control Module*. Failure to follow this procedure can damage the MMCHS interface.

Figure 24-51 shows how to configure the MMCHS controller to fit with power switching sequence.

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Figure 24-51. MMC/SDIO Power Switching Procedure

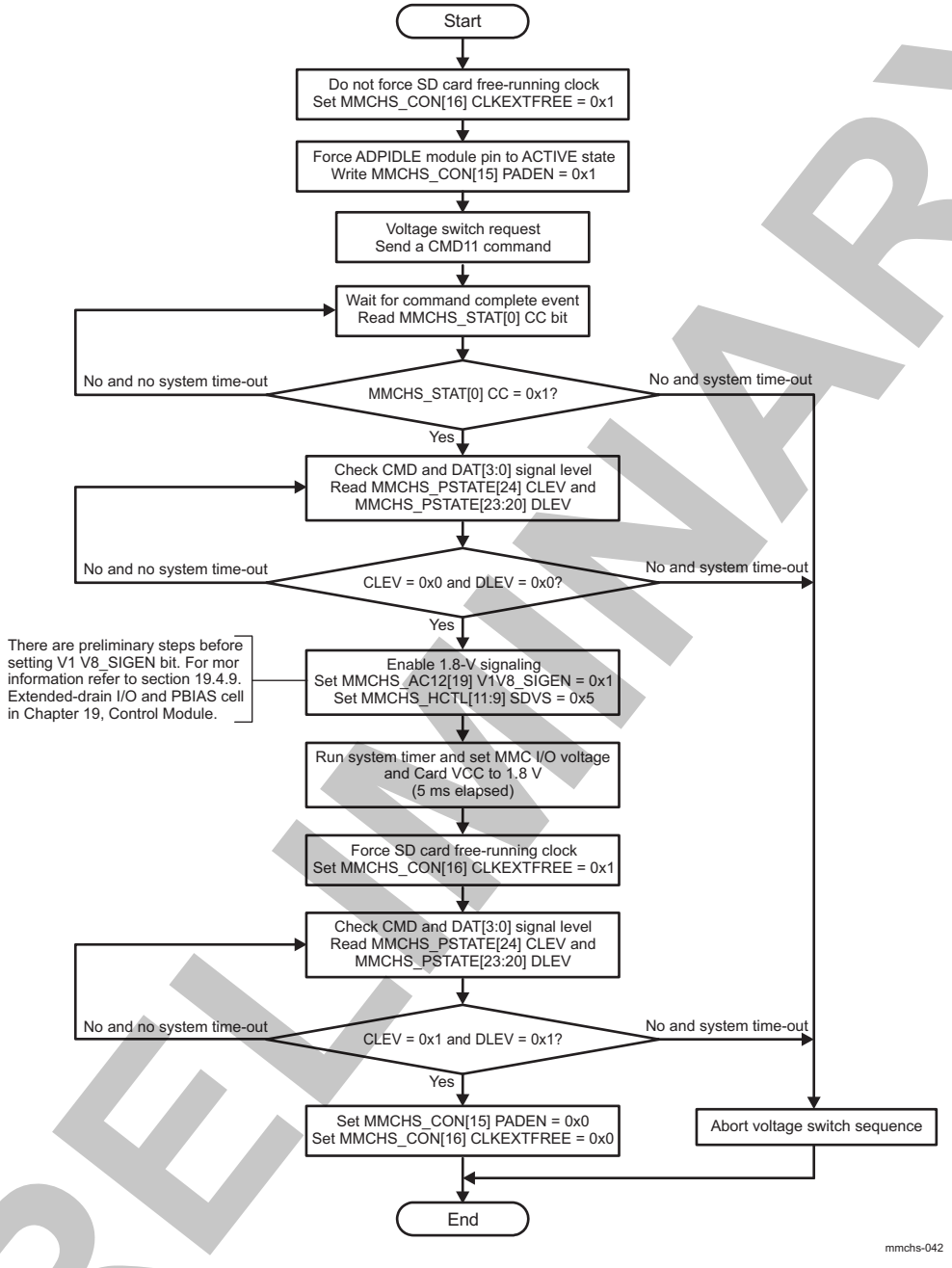

Table 24-51. Register Call Summary for Main Sequence – Power Switching Procedure

Register Name	Register Name
MMCHS_STAT	MMCHS_PSTATE
MMCHS_CMD	MMCHS_CON

Table 24-52. Subprocess Call Summary for Main Sequence – Power Switching Procedure

Subprocess Name	Cross-Reference
Send a READ_DAT_UNTIL_STOP command (CMD11).	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.

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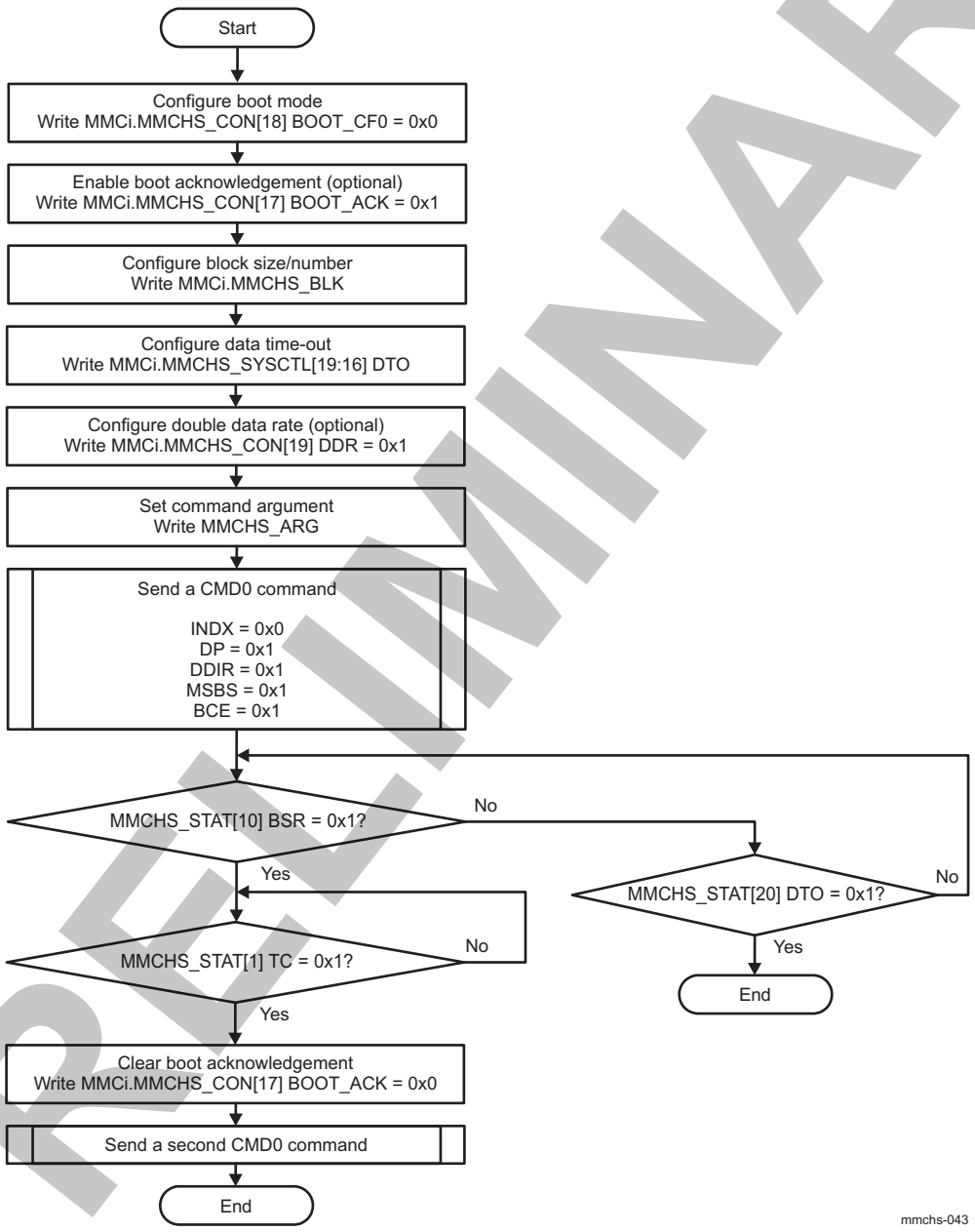
24.5.1.2.3 Boot Mode Configuration

The following sections describe the two possible ways to issue a boot command: issue a CMD0 or drive the CMD line to 0 during the whole boot phase.

24.5.1.2.3.1 Boot Using CMD0

Figure 24-52 shows the necessary steps to configure the controller boot mode using CMD0.

Figure 24-52. MMC/SDIO Controller Boot Using CMD0



To abort a boot sequence, the system must issue a CMD0 with the MMCHS_CMD[23:22] CMD_TYPE bit field set to 0x3 (the MMCHS_CON[17] BOOT_ACK bit previously cleared to 0x0) during the transfer to abort the transfer and enable the card to exit from boot state.

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Table 24-53. Register Call Summary for Main Sequence – Boot Using CMD0

Register Name	Register Name	Register Name
MMCHS_CON	MMCHS_BLK	MMCHS_SYSCTL
MMCHS_ARG	MMCHS_STAT	

Table 24-54. Subprocess Call Summary for Main Sequence – Boot Using CMD0

Subprocess Name	Cross-Reference
Send a CMD0 command.	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.

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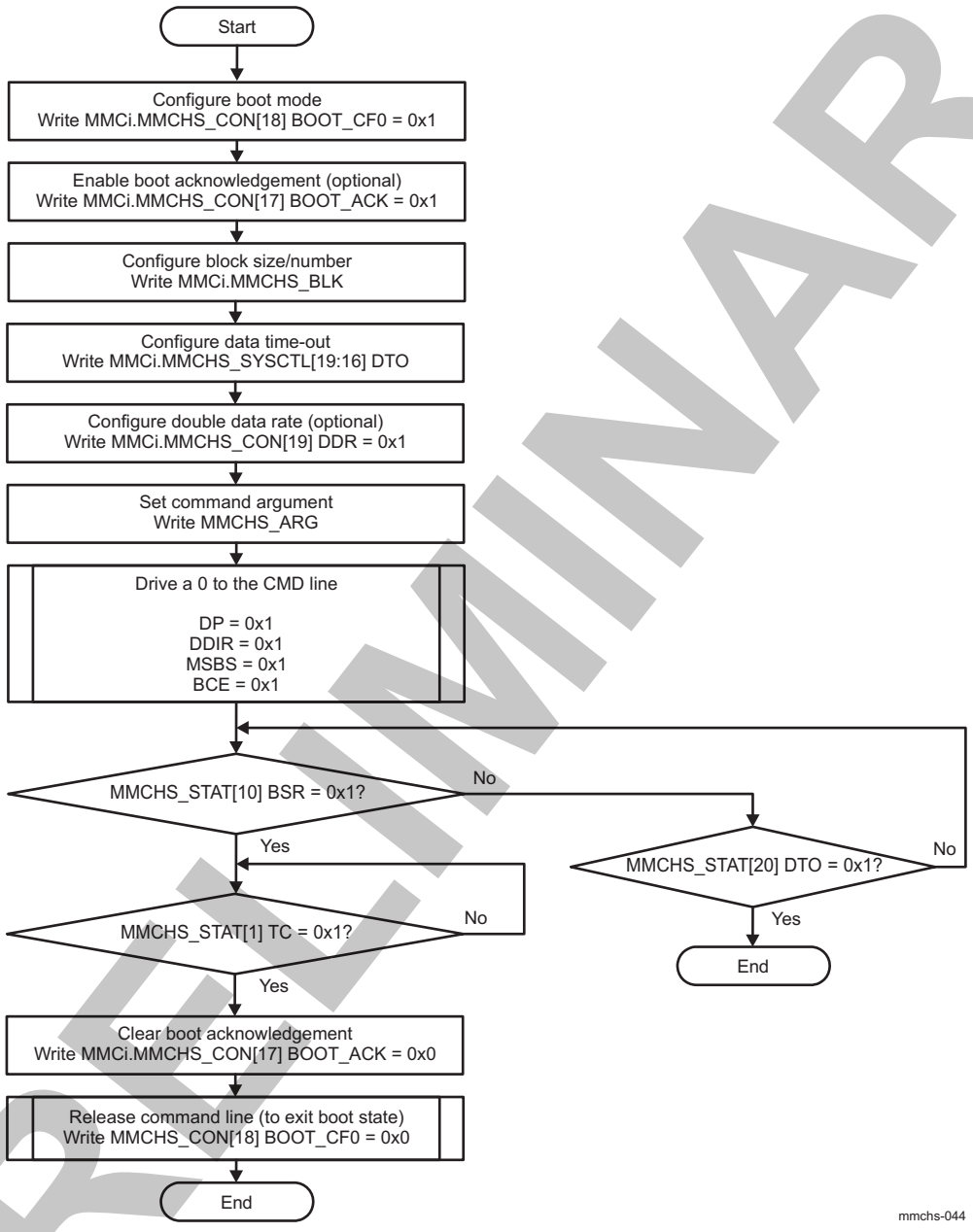
24.5.1.2.3.2 Boot With CMD Line Tied to 0

Figure 24-53 shows the necessary steps to configure the controller in this mode; the driver must follow this sequence.

Figure 24-53. MMC/SDIO Controller Boot With CMD Line Tied to 0



To abort the boot sequence, the system must clear the MMCHS_CON[18] BOOT_CF0 bit to 0x0 during the transfer to abort the transfer and enable the card to exit from boot state.

Table 24-55. Register Call Summary for Main Sequence – Boot Using CMD0

Register Name	Register Name	Register Name
MMCHS_CON	MMCHS_BLK	MMCHS_SYSCTL
MMCHS_ARG	MMCHS_STAT	MMCHS_CMD

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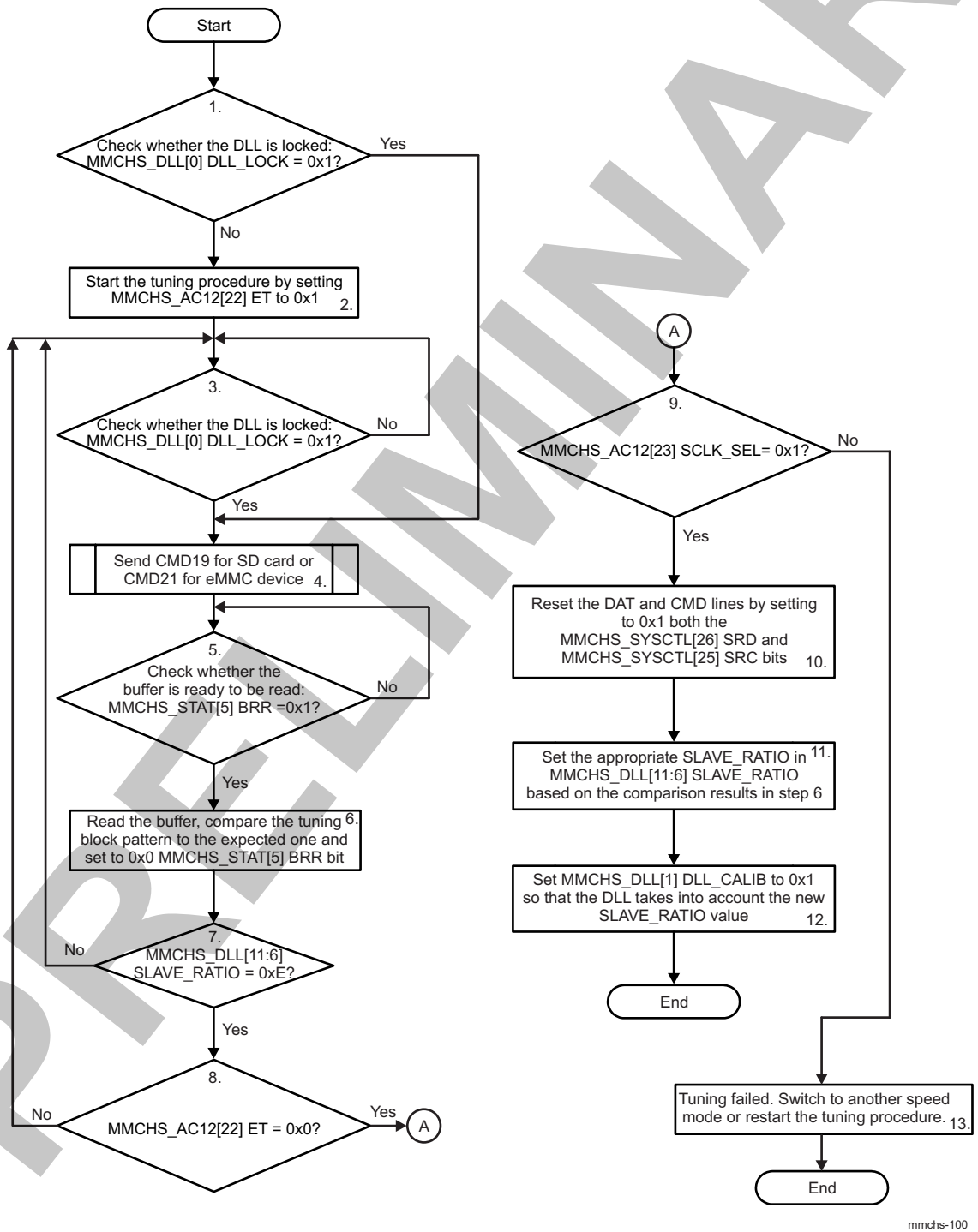
Table 24-56. Subprocess Call Summary for Main Sequence – Boot Using CMD0

Subprocess Name	Cross-Reference
Send a CMD0 command.	See Section 24.5.1.2.1.7.1, *Command Transfer Flow*.

24.5.1.2.4 SDR104/HS200 DLL Tuning Procedure

Figure 24-54 shows the DLL tuning procedure when SDR104 and HS200 modes are used.

Figure 24-54. SDR104/HS200 DLL Tuning Procedure



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24.6 MMC/SDIO Register Manual

24.6.1 MMC/SDIO Instance Summary

Table 24-57 lists the MMC/SDIO instances.

Table 24-57. MMC/SDIO Instance Summary

Module Name	Module Base Address	Size
MMC1	0x4809 C000	4 KiB
MMC3	0x480A D000	4 KiB
MMC2	0x480B 4000	4 KiB
MMC4	0x480D 1000	4 KiB
MMC5	0x480D 5000	4 KiB

24.6.2 MMC/SDIO Registers

24.6.2.1 MMC/SDIO Register Summary

Table 24-58 lists the MMC/SDIO registers.

Table 24-58. MMC1 and MMC2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MMC1 Physical Address	MMC2 Physical Address
MMCHS_HL_REV	R	32	0x0000 0000	0x4809 C000	0x480B 4000
MMCHS_HL_HWINFO	R	32	0x0000 0004	0x4809 C004	0x480B 4004
MMCHS_HL_SYSCONFIG	RW	32	0x0000 0010	0x4809 C010	0x480B 4010
MMCHS_SYSCONFIG	RW	32	0x0000 0110	0x4809 C110	0x480B 4110
MMCHS_SYSSTATUS	R	32	0x0000 0114	0x4809 C114	0x480B 4114
MMCHS_CSRE	RW	32	0x0000 0124	0x4809 C124	0x480B 4124
MMCHS_SYSTEST	RW	32	0x0000 0128	0x4809 C128	0x480B 4128
MMCHS_CON	RW	32	0x0000 012C	0x4809 C12C	0x480B 412C
MMCHS_PWCNT	RW	32	0x0000 0130	0x4809 C130	0x480B 4130
MMCHS_DLL	RW	32	0x0000 0134	0x4809 C134	0x480B 4134
MMCHS_SDMASA	RW	32	0x0000 0200	0x4809 C200	0x480B 4200
MMCHS_BLK	RW	32	0x0000 0204	0x4809 C204	0x480B 4204
MMCHS_ARG	RW	32	0x0000 0208	0x4809 C208	0x480B 4208
MMCHS_CMD	RW	32	0x0000 020C	0x4809 C20C	0x480B 420C
MMCHS_RSP10	R	32	0x0000 0210	0x4809 C210	0x480B 4210
MMCHS_RSP32	R	32	0x0000 0214	0x4809 C214	0x480B 4214
MMCHS_RSP54	R	32	0x0000 0218	0x4809 C218	0x480B 4218
MMCHS_RSP76	R	32	0x0000 021C	0x4809 C21C	0x480B 421C
MMCHS_DATA	RW	32	0x0000 0220	0x4809 C220	0x480B 4220
MMCHS_PSTATE	R	32	0x0000 0224	0x4809 C224	0x480B 4224
MMCHS_HCTL	RW	32	0x0000 0228	0x4809 C228	0x480B 4228
MMCHS_SYSCTL	RW	32	0x0000 022C	0x4809 C22C	0x480B 422C
MMCHS_STAT	RW	32	0x0000 0230	0x4809 C230	0x480B 4230
MMCHS_IE	RW	32	0x0000 0234	0x4809 C234	0x480B 4234
MMCHS_ISE	RW	32	0x0000 0238	0x4809 C238	0x480B 4238

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Table 24-58. MMC1 and MMC2 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	MMC1 Physical Address	MMC2 Physical Address
MMCHS_AC12	RW	32	0x0000 023C	0x4809 C23C	0x480B 423C
MMCHS_CAPA	RW	32	0x0000 0240	0x4809 C240	0x480B 4240
MMCHS_CAPA2	R	32	0x0000 0244	0x4809 C244	0x480B 4244
MMCHS_CUR_CAPA	RW	32	0x0000 0248	0x4809 C248	0x480B 4248
MMCHS_FE	W	32	0x0000 0250	0x4809 C250	0x480B 4250
MMCHS_ADMAES	RW	32	0x0000 0254	0x4809 C254	0x480B 4254
MMCHS_ADMASAL	RW	32	0x0000 0258	0x4809 C258	0x480B 4258
MMCHS_PVINITSD	R	32	0x0000 0260	0x4809 C260	0x480B 4260
MMCHS_PVHSSDR12	R	32	0x0000 0264	0x4809 C264	0x480B 4264
MMCHS_PVSDR25SDR50	R	32	0x0000 0268	0x4809 C268	0x480B 4268
MMCHS_PVSDR104DDR50	R	32	0x0000 026C	0x4809 C26C	0x480B 426C
MMCHS_REV	R	32	0x0000 02FC	0x4809 C2FC	0x480B 42FC

Table 24-59. MMC3, MMC4 and MMC5 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MMC3 Base Address	MMC4 Base Address	MMC5 Base Address
MMCHS_HL_REV	R	32	0x0000 0000	0x480A D000	0x480D 1000	0x480D 5000
MMCHS_HL_HWINFO	R	32	0x0000 0004	0x480A D004	0x480D 1004	0x480D 5004
MMCHS_HL_SYSCONFIG	RW	32	0x0000 0010	0x480A D010	0x480D 1010	0x480D 5010
MMCHS_SYSCONFIG	RW	32	0x0000 0110	0x480A D110	0x480D 1110	0x480D 5110
MMCHS_SYSSTATUS	R	32	0x0000 0114	0x480A D114	0x480D 1114	0x480D 5114
MMCHS_CSRE	RW	32	0x0000 0124	0x480A D124	0x480D 1124	0x480D 5124
MMCHS_SYSTEST	RW	32	0x0000 0128	0x480A D128	0x480D 1128	0x480D 5128
MMCHS_CON	RW	32	0x0000 012C	0x480A D12C	0x480D 112C	0x480D 512C
MMCHS_PWCNT	RW	32	0x0000 0130	0x480A D130	0x480D 1130	0x480D 5130
RESERVED	R	32	0x0000 0134	0x480A D134	0x480D 1134	0x480D 5134
MMCHS_SDMASA	RW	32	0x0000 0200	0x480A D200	0x480D 1200	0x480D 5200
MMCHS_BLK	RW	32	0x0000 0204	0x480A D204	0x480D 1204	0x480D 5204
MMCHS_ARG	RW	32	0x0000 0208	0x480A D208	0x480D 1208	0x480D 5208
MMCHS_CMD	RW	32	0x0000 020C	0x480A D20C	0x480D 120C	0x480D 520C
MMCHS_RSP10	R	32	0x0000 0210	0x480A D210	0x480D 1210	0x480D 5210
MMCHS_RSP32	R	32	0x0000 0214	0x480A D214	0x480D 1214	0x480D 5214
MMCHS_RSP54	R	32	0x0000 0218	0x480A D218	0x480D 1218	0x480D 5218
MMCHS_RSP76	R	32	0x0000 021C	0x480A D21C	0x480D 121C	0x480D 521C
MMCHS_DATA	RW	32	0x0000 0220	0x480A D220	0x480D 1220	0x480D 5220
MMCHS_PSTATE	R	32	0x0000 0224	0x480A D224	0x480D 1224	0x480D 5224
MMCHS_HCTL	RW	32	0x0000 0228	0x480A D228	0x480D 1228	0x480D 5228
MMCHS_SYSCTL	RW	32	0x0000 022C	0x480A D22C	0x480D 122C	0x480D 522C
MMCHS_STAT	RW	32	0x0000 0230	0x480A D230	0x480D 1230	0x480D 5230

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Table 24-59. MMC3, MMC4 and MMC5 Registers Mapping Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	MMC3 Base Address	MMC4 Base Address	MMC5 Base Address
MMCHS_IE	RW	32	0x0000 0234	0x480A D234	0x480D 1234	0x480D 5234
MMCHS_ISE	RW	32	0x0000 0238	0x480A D238	0x480D 1238	0x480D 5238
MMCHS_AC12	RW	32	0x0000 023C	0x480A D23C	0x480D 123C	0x480D 523C
MMCHS_CAPA	RW	32	0x0000 0240	0x480A D240	0x480D 1240	0x480D 5240
MMCHS_CAPA2	R	32	0x0000 0244	0x480A D244	0x480D 1244	0x480D 5244
MMCHS_CUR_CAPA	RW	32	0x0000 0248	0x480A D248	0x480D 1248	0x480D 5248
MMCHS_FE	W	32	0x0000 0250	0x480A D250	0x480D 1250	0x480D 5250
MMCHS_ADMAES	RW	32	0x0000 0254	0x480A D254	0x480D 1254	0x480D 5254
MMCHS_ADMASAL	RW	32	0x0000 0258	0x480A D258	0x480D 1258	0x480D 5258
MMCHS_PVINITSD	R	32	0x0000 0260	0x480A D260	0x480D 1260	0x480D 5260
MMCHS_PVHSSDR12	R	32	0x0000 0264	0x480A D264	0x480D 1264	0x480D 5264
MMCHS_PVSDR25SDR50	R	32	0x0000 0268	0x480A D268	0x480D 1268	0x480D 5268
MMCHS_PVSDR104DDR50	R	32	0x0000 026C	0x480A D26C	0x480D 126C	0x480D 526C
MMCHS_REV	R	32	0x0000 02FC	0x480A D2FC	0x480D 12FC	0x480D 52FC

24.6.2.2 MMC/SDIO Register Description

Table 24-60. MMCHS_HL_REV

Address Offset	0x0000 0000
Physical Address	0x4809 C000 0x480B 4000 0x480B 4000 0x480A D000 0x480D 1000 0x480D 1000 0x480D 5000 0x480D 5000
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	TI internal data

Table 24-61. Register Call Summary for Register MMCHS_HL_REV

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- MMC/SDIO Register Summary: [0] [1]

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Table 24-62. MMCHS_HL_HWINFO

Address Offset	0x0000 0004
Physical Address	0x4809 C004 0x480B 4004 0x480B 4004 0x480A D004 0x480D 1004 0x480D 1004 0x480D 5004 0x480D 5004
Description	Information about the IP module's hardware configuration.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RETMODE	MEM_SIZE					MERGE_MEM	MADMA_EN

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x000 0000
6	RETMODE	Retention Mode generic parameter This bit field indicates whether the retention mode is supported using the pin PIRFFRET. Read 0x1: Retention mode enabled Read 0x0: Retention mode disabled	R	0
5:2	MEM_SIZE	Memory size for FIFO buffer: Read 0x2: Memory of 1024 bytes, max block length is 1024 bytes Read 0x1: Memory of 512 bytes, max block length is 512 bytes Read 0x8: Memory of 4096 bytes, max block length is 2048 bytes Read 0x4: Memory of 2048 bytes, max block length is 2048 bytes	R	0x2
1	MERGE_MEM	Memory merged for FIFO buffer: This register defines the configuration of FIFO buffer architecture. If the bit is set STA and DFT shall support clock multiplexing and balancing. Read 0x1: A single memory is used with multiplexed addresses, data and clocks. Read 0x0: 2 memories instantiated, one per data transfer direction.	R	1
0	MADMA_EN	Master DMA enabled generic parameter: This register defines the configuration of the controller to know if it supports the master DMA management called ADMA. Read 0x1: Controller supports ADMA Read 0x0: No Master DMA (ADMA) management supported	R	0

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Table 24-63. Register Call Summary for Register MMCHS_HL_HWINFO

MMC/SDIO Functional Description

- Power Management: [0]
- DMA Modes: [1] [2]
- Master DMA Operations: [3]
- Slave DMA Operations: [4]
- Memory Size, Block Length, and Buffer-Management Relationship: [5]
- Retention Mode: [6]

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- MMC/SDIO Register Summary: [7] [8]
- MMC/SDIO Register Description: [9]

Table 24-64. MMCHS_HL_SYSCONFIG

Address Offset	0x0000 0010
Physical Address	0x4809 C010 0x480B 4010 0x480B 4010 0x480A D010 0x480D 1010 0x480D 1010 0x480D 5010 0x480D 5010
Description	Clock Management Configuration Register
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STANDBYMODE		IDLEMODE		FREEEMU		SOFTRESET	

Bits	Field Name	Description	Type	Reset
31:6	RESERVED		R	0x000 0000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state.Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state.Backup mode, for debug only. 0x3: Smart-Standby wakeup-capable mode: local initiator standby status depends on local conditions, i.e. the module's functional requirement from the initiator. IP module may generate (master-related) wakeup events when in standby state.Mode is only relevant if the appropriate IP module "mwakeup" output is implemented. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, i.e. the module's functional requirement from the initiator.IP module shall not generate (initiator-related) wakeup events.	RW	0x2

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Bits	Field Name	Description	Type	Reset
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's IDLE requests unconditionally, i.e. regardless of the IP module's internal requirements.Backup mode, for debug only. 0x1: No-idle mode: local target never enters idle state.Backup mode, for debug only. 0x3: Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's IDLE requests, depending on the IP module's internal requirements.IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state.Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) implemented. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's IDLE requests, depending on the IP module's internal requirements.IP module shall not generate (IRQ- or DMA-request-related) wakeup events.	RW	0x2
1	FREEEMU	Sensitivity to emulation (debug) suspend input signal. Functionality NOT implemented in MMCHS. 0x0: IP module is sensitive to emulation suspend 0x1: IP module is not sensitive to emulation suspend	RW	0
0	SOFTRESET	Software reset. (Optional) Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing Read 0x0: Reset done, no pending action	RW	0

Table 24-65. Register Call Summary for Register MMCHS_HL_SYSCONFIG

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- MMC/SDIO Register Summary: [0] [1]

Table 24-66. MMCHS_SYSCONFIG

Address Offset	0x0000 0110
Physical Address	0x4809 C110 0x480B 4110 0x480B 4110 0x480A D110 0x480D 1110 0x480D 1110 0x480D 5110 0x480D 5110
Description	System Configuration Register This register allows controlling various parameters of the Interconnect interface.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		STANDBYMODE		RESERVED		CLOCKACTIVITY		RESERVED			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE

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Bits	Field Name	Description	Type	Reset
31:14	RESERVED		R	0x0 0000
13:12	STANDBYMODE	Master interface power Management, standby/wait control. The bit field is only useful when generic parameter MMCHS_HL_HWINFO[0] MADMA_EN (Master ADMA enable) is set as active, otherwise it is a read only register read a '0'. 0x0: Force-standby. Mstandby is forced unconditionnaly. 0x1: No-standby. Mstandby is never asserted. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, i.e. the module's functional requirement from the initiator.IP module shall not generate (initiator-related) wakeup events.	RW	0x2
11:10	RESERVED		R	0x0
9:8	CLOCKACTIVITY	Clocks activity during wake up mode period. Bit8: Interface clock Bit9: Functional clock 0x0: Interface and Functional clock may be switched off. 0x1: Interface clock is maintained. Functional clock may be switched-off. 0x3: Interface and Functional clocks are maintained. 0x2: Functional clock is maintained. Interface clock may be switched-off.	RW	0x0
7:5	RESERVED	This bit is initialized to zero, and writes to it are ignored. Reads return 0.	R	0x0
4:3	SIDLEMODE	Power management 0x0: If an IDLE request is detected, the MMCHS acknowledges it unconditionally and goes in Inactive mode. Interrupt and DMA requests are unconditionally de-asserted. 0x1: If an IDLE request is detected, the request is ignored and the module keeps on behaving normally. 0x3: Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's IDLE requests, depending on the IP module's internal requirements.IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state.Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) implemented. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's IDLE requests, depending on the IP module's internal requirements.IP module shall not generate (IRQ- or DMA-request-related) wakeup events.	RW	0x2
2	ENAWAKEUP	Wakeup feature control 0x0: Wakeup capability is disabled 0x1: Wakeup capability is enabled	RW	1
1	SOFTRESET	Software reset. The bit is automatically reset by the hardware. During reset, it always returns 0. Write 0x0: No effect. Write 0x1: Trigger a module reset. Read 0x1: The module is reset. Read 0x0: Normal mode	RW	0
0	AUTOIDLE	Internal Clock gating strategy 0x0: Clocks are free-running 0x1: Automatic clock gating strategy is applied, based on the Interconnect and MMC interface activity	RW	1

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Table 24-67. Register Call Summary for Register MMCHS_SYSCONFIG

MMC/SDIO Functional Description • Software Reset: [0] • Power Management: [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13]
MMC/SDIO Programming Guide • MMC/SDIO Host Controller Initialization Flow: [14] [15] [16]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [17] [18] • MMC/SDIO Register Description: [19] [20] [21] [22] [23] [24]

Table 24-68. MMCHS_SYSSTATUS

Address Offset	0x0000 0114
Physical Address	0x4809 C114 0x480B 4114 0x480B 4114 0x480A D114 0x480D 1114 0x480D 1114 0x480D 5114 0x480D 5114
Description	System Status Register This register provides status information about the module excluding the interrupt status information
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	RESETDONE	Internal Reset Monitoring Note: the debounce clock , the system clock (Interface) and the functional clock shall be provided to the MMC/SD/SDIO host controller to allow the internal reset monitoring. Read 0x1: Reset completed. Read 0x0: Internal module reset is on-going	R	0

Table 24-69. Register Call Summary for Register MMCHS_SYSSTATUS

MMC/SDIO Functional Description • Hardware Reset: [0] • Software Reset: [1]
MMC/SDIO Programming Guide • MMC/SDIO Host Controller Initialization Flow: [2]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [3] [4]

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Table 24-70. MMCHS_CSRE

Address Offset	0x0000 0124
Physical Address	0x4809 C124 0x480B 4124 0x480B 4124 0x480A D124 0x480D 1124 0x480D 1124 0x480D 5124 0x480D 5124
Description	Card Status Response Error This register enables the host controller to detect card status errors of response type R1, R1b for all cards and of R5, R5b and R6 response for cards types SD or SDIO. When a bit MMCHS_CSRE[i] is set to 1, if the corresponding bit at the same position in the response MMCHS_RSP0[i] is set to 1, the host controller indicates a card error (MMCHS_STAT[CERR]) interrupt status to avoid the host driver reading the response register (MMCHS_RSP0). Note: No automatic card error detection for autoCMD12 is implemented; the host system has to check autoCMD12 response register (MMCHS_RESP76) for possible card errors.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSRE																															

Bits	Field Name	Description	Type	Reset
31:0	CSRE	Card status response error	RW	0x0000 0000

Table 24-71. Register Call Summary for Register MMCHS_CSRE

MMC/SDIO Functional Description
- Interrupt Requests: [0]

MMC/SDIO Programming Guide
- Basic Operations for MMC/SDIO Host Controller: [1] [2]

MMC/SDIO Register Manual
- MMC/SDIO Register Summary: [3] [4]
- MMC/SDIO Register Description: [5] [6]

Table 24-72. MMCHS_SYSTEST

Address Offset	0x0000 0128
Physical Address	0x4809 C128 0x480B 4128 0x480B 4128 0x480A D128 0x480D 1128 0x480D 1128 0x480D 5128 0x480D 5128
Description	System Test Register This register is used to control the signals that connect to I/O pins when the module is configured in system test (SYSTEST) mode for boundary connectivity verification. Note: In SYSTEST mode, a write into MMCHS_CMD register will not start a transfer. The buffer behaves as a stack accessible only by the local host (push and pop operations). In this mode, the Transfer Block Size (MMCHS_BLK[BLEN]) and the Blocks count for current transfer (MMCHS_BLK[NBLK]) are needed to generate a Buffer write ready interrupt (MMCHS_STAT[BWR]) or a Buffer read ready interrupt (MMCHS_STAT[BRR]) and DMA requests if enabled.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															OBI	SDCD	SDWP	WAKD	SSB	D7D	D6D	D5D	D4D	D3D	D2D	D1D	D0D	DDIR	CDAT	CDIR	MCKD

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Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	OBI	Out-Of-Band Interrupt (OBI) data value Read 0x1: The Out-of-Band Interrupt pin is driven high. Read 0x0: The Out-of-Band Interrupt pin is driven low.	R	0
15	SDCD	Card detect input signal (sdcard_cd) data value Read 0x1: The card detect pin is driven high. Read 0x0: The card detect pin is driven low.	R	0
14	SDWP	Write protect input signal (sdcard_wp) data value Read 0x1: The write protect pin sdcard_wp is driven high. Read 0x0: The write protect pin sdcard_wp is driven low.	R	0
13	WAKD	Wake request output signal data value Write 0x0: The pin SWAKEUP is driven low. Write 0x1: The pin SWAKEUP is driven high. Read 0x1: No action. Returns 1. Read 0x0: No action. Returns 0.	RW	0
12	SSB	Set status bit This bit must be cleared prior attempting to clear a status bit of the interrupt status register (MMCHS_STAT). Write 0x0: Clear this SSB bitfield. Writing 0 does not clear already set status bits; Write 0x1: Force to 1 all status bits of the interrupt status register (MMCHS_STAT) only if the corresponding bitfield in the Interrupt signal enable register (MMCHS_ISE) is set. Read 0x1: No action. Returns 1. Read 0x0: No action. Returns 0.	RW	0
11	D7D	DAT7 input/output signal data value Write 0x0: If SYSTEST[DDIR] = 0 (output mode direction), the DAT7 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Write 0x1: If SYSTEST[DDIR] = 0 (output mode direction), the DAT7 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Read 0x1: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT7 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 Read 0x0: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT7 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0	RW	0
10	D6D	DAT6 input/output signal data value Write 0x0: If SYSTEST[DDIR] = 0 (output mode direction), the DAT6 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Write 0x1: If SYSTEST[DDIR] = 0 (output mode direction), the DAT6 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Read 0x1: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT6 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 Read 0x0: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT6 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0	RW	0

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Bits	Field Name	Description	Type	Reset
9	D5D	DAT5 input/output signal data value Write 0x0: If SYSTEST[DDIR] = 0 (output mode direction), the DAT5 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Write 0x1: If SYSTEST[DDIR] = 0 (output mode direction), the DAT5 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Read 0x1: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT5 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 Read 0x0: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT5 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0	RW	0
8	D4D	DAT4 input/output signal data value Write 0x0: If SYSTEST[DDIR] = 0 (output mode direction), the DAT4 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Write 0x1: If SYSTEST[DDIR] = 0 (output mode direction), the DAT4 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Read 0x1: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT4 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 Read 0x0: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT4 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0	RW	0
7	D3D	DAT3 input/output signal data value Write 0x0: If SYSTEST[DDIR] = 0 (output mode direction), the DAT3 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Write 0x1: If SYSTEST[DDIR] = 0 (output mode direction), the DAT3 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Read 0x1: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT3 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 Read 0x0: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT3 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0	RW	0
6	D2D	DAT2 input/output signal data value Write 0x0: If SYSTEST[DDIR] = 0 (output mode direction), the DAT2 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Write 0x1: If SYSTEST[DDIR] = 0 (output mode direction), the DAT2 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Read 0x1: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT2 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 Read 0x0: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT2 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0	RW	0

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Bits	Field Name	Description	Type	Reset
5	D1D	DAT1 input/output signal data value Write 0x0: If SYSTEST[DDIR] = 0 (output mode direction), the DAT1 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Write 0x1: If SYSTEST[DDIR] = 0 (output mode direction), the DAT1 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Read 0x1: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT1 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 Read 0x0: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT1 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0	RW	0
4	D0D	DAT0 input/output signal data value Write 0x0: If SYSTEST[DDIR] = 0 (output mode direction), the DAT0 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Write 0x1: If SYSTEST[DDIR] = 0 (output mode direction), the DAT0 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. Read 0x1: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT0 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 Read 0x0: If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT0 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0	RW	0
3	DDIR	Control of the DAT[7:0] pins direction. Write 0x0: The DAT lines are outputs (host to card) Write 0x1: The DAT lines are inputs (card to host) Read 0x1: No action. Returns 1. Read 0x0: No action. Returns 0.	RW	0
2	CDAT	CMD input/output signal data value Write 0x0: If SYSTEST[CDIR] = 0 (output mode direction), the CMD line is driven low. If SYSTEST[CDIR] = 1 (input mode direction), no effect. Write 0x1: If SYSTEST[CDIR] = 0 (output mode direction), the CMD line is driven high. If SYSTEST[CDIR] = 1 (input mode direction), no effect. Read 0x1: If SYSTEST[CDIR] = 1 (input mode direction), returns the value on the CMD line (high) If SYSTEST[CDIR] = 0 (output mode direction), returns 1 Read 0x0: If SYSTEST[CDIR] = 1 (input mode direction), returns the value on the CMD line (low). If SYSTEST[CDIR] = 0 (output mode direction), returns 0	RW	0
1	CDIR	Control of the CMD pin direction. Write 0x0: The CMD line is an output (host to card) Write 0x1: The CMD line is an input (card to host) Read 0x1: No action. Returns 1. Read 0x0: No action. Returns 0.	RW	0
0	MCKD	MMC clock output signal data value Write 0x0: The output clock is driven low. Write 0x1: The output clock is driven high. Read 0x1: No action. Returns 1. Read 0x0: No action. Returns 0.	RW	0

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Table 24-73. Register Call Summary for Register MMCHS_SYSTEST

MMC/SDIO Functional Description • Test Registers: [0]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [1] [2]

Table 24-74. MMCHS_CON

Address Offset	0x0000 012C
Physical Address	0x4809 C12C 0x480B 412C 0x480B 412C 0x480A D12C 0x480D 112C 0x480D 112C 0x480D 512C 0x480D 512C
Description	Configuration Register This register is used: - to select the functional mode or the SYSTEST mode for any card. - to send an initialization sequence to any card. - to enable the detection on DAT[1] of a card interrupt for SDIO cards only. and also to configure : - specific data and command transfers for MMC cards only. - the parameters related to the card detect and write protect input signals.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SDMA_LNE	DMA_MNS	DDR	BOOT_CF0	BOOT_ACK	CLKEXTFREE	PADEN	OBIE	OBIP	CEATA	CTPL	DVAL		WPP	CDP	MIT	DW8	MODE	STR	HR	INIT	OD
R										RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW
0x000										0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21	SDMA_LNE	Slave DMA Level/Edge Request: The waveform of the DMA request can be configured either edge sensitive with early de-assertion on first access to MMCHS_DATA register or late de-assertion, request remains active until last allowed data written into MMCHS_DATA. 0x0: Slave DMA edge sensitive, Early DMA de-assertion 0x1: Slave DMA level sensitive, Late DMA de-assertion	RW	0
20	DMA_MNS	DMA Master or Slave selection: When this bit is set and the controller is configured to use the DMA, Interconnect master interface is used to get datas from system using ADMA2 procedure (direct access to the memory).This option is only available if generic parameter MADMA_EN is asserted to '1'. 0x0: The controller is slave on data transfers with system. 0x1: The controller is master on data exchange with system, controller must be configured as using DMA.	RW	0

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Bits	Field Name	Description	Type	Reset
19	DDR	Dual Data Rate mode: When this register is set, the controller uses both clock edge to emit or receive data. Odd bytes are transmitted on falling edges and even bytes are transmitted on rise edges. It only applies on Data bytes and CRC, Start, end bits and CRC status are kept full cycle. This bit field is only meaningful and active for even clock divider ratio of MMCHS_SYSCTL[CLKD], it is insensitive to MMCHS_HCTL[HSPE] setting. 0x0: Standard mode : data are transmitted on a single edge depending on MMCHS_HCTRL[HSPE]. 0x1: Data Bytes and CRC are transmitted on both edge.	RW	0
18	BOOT_CF0	Boot status supported: This register is set when the CMD line need to be forced to '0' for a boot sequence. CMD line is driven to '0' after writing in MMCHS_CMD. The line is released when this bit field is de-asserted and abort data transfer in case of a pending transaction. Write 0x0: CMD line is released when it was previously forced to '0' by a boot sequence. Write 0x1: CMD line forced to '0' is enabled and will be active after writing into MMCHS_CMD Read 0x1: CMD line forced to '0' is enabled Read 0x0: CMD line not forced	RW	0
17	BOOT_ACK	Book acknowledge received: When this bit is set the controller should receive a boot status on DAT0 line after next command issued. If no status is received a data timeout will be generated. 0x0: No acknowledge to be received 0x1: A boot status will be received on DAT0 line after issuing a command.	RW	0
16	CLKEXTFREE	External clock free running: This register is used to maintain card clock out of transfer transaction to enable slave module for example to generate a synchronous interrupt on DAT[1]. The Clock will be maintain only if MMCHS_SYSCTL[CEN] is set. 0x0: External card clock is cut off outside active transaction period. 0x1: External card clock is maintain even out of active transaction period only if MMCHS_SYSCTL[CEN] is set.	RW	0
15	PADEN	Control Power for MMC Lines: This register is only useful when MMC PADs contain power saving mechanism to minimize its leakage power. It works as a GPIO that directly control the ACTIVE pin of PADs. Excepted for DAT[1], the signal is also combine outside the module with the dedicated power control MMCHS_CON[CTPL] bit. 0x0: ADPIDLE module pin is not forced, it is automatically generated by the MMC fsms. 0x1: ADPIDLE module pin is forced to active state.	RW	0
14	OBIE	Out-of-Band Interrupt Enable MMC cards only: This bit enables the detection of Out-of-Band Interrupt on MMCOBI input pin. The usage of the Out-of-Band signal (OBI) is optional and depends on the system integration. 0x0: Out-of-Band interrupt detection disabled 0x1: Out-of-Band interrupt detection enabled	RW	0

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Bits	Field Name	Description	Type	Reset
13	OBIP	Out-of-Band Interrupt Polarity MMC cards only: This bit selects the active level of the out-of-band interrupt coming from MMC cards. The usage of the Out-of-Band signal (OBI) is optional and depends on the system integration. 0x0: Active high level 0x1: Active low level	RW	0
12	CEATA	CE-ATA control mode MMC cards compliant with CE-ATA:By default, this bit is set to 0. It is used to indicate that next commands are considered as specific CE-ATA commands that potentially use 'command completion' features. 0x0: Standard MMC/SD/SDIO mode. 0x1: CE-ATA mode next commands are considered as CE-ATA commands.	RW	0
11	CTPL	Control Power for DAT[1] line MMC and SD cards: By default, this bit is set to 0 and the host controller automatically disables all the input buffers outside of a transaction to minimize the leakage current. SDIO cards: When this bit is set to 1, the host controller automatically disables all the input buffers except the buffer of DAT[1] outside of a transaction in order to detect asynchronous card interrupt on DAT[1] line and minimize the leakage current of the buffers. 0x0: Disable all the input buffers outside of a transaction. 0x1: Disable all the input buffers except the buffer of DAT[1] outside of a transaction.	RW	0
10:9	DVAL	Debounce filter value All cards This register is used to define a debounce period to filter the card detect input signal (sdcard_cd). The usage of the card detect input signal (sdcard_cd) is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0x0: 33 us debounce period 0x1: 231 us debounce period 0x3: 8,4 ms debounce period 0x2: 1 ms debounce period	RW	0x3
8	WPP	Write protect polarity For SD and SDIO cards only This bit selects the active level of the write protect input signal (sdcard_wp). The usage of the write protect input signal (sdcard_wp) is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0x0: Active high level 0x1: Active low level	RW	0
7	CDP	Card detect polarity All cards This bit selects the active level of the card detect input signal (sdcard_cd). The usage of the card detect input signal (sdcard_cd) is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0x0: Active low level 0x1: Active high level	RW	0

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Bits	Field Name	Description	Type	Reset
6	MIT	MMC interrupt command Only for MMC cards. This bit must be set to 1, when the next write access to the command register (MMCHS_CMD) is for writing a MMC interrupt command (CMD40) requiring the command timeout detection to be disabled for the command response. 0x0: Command timeout enabled 0x1: Command timeout disabled	RW	0
5	DW8	8-bit mode MMC select For SD/SDIO cards, this bit must be set to 0. For MMC card, this bit must be set following a valid SWITCH command (CMD6) with the correct value and extend CSD index written in the argument. Prior to this command, the MMC card configuration register (CSD and EXT_CSD) must be verified for compliancy with MMC standard specification 4.x (see section 3.6). 0x0: 1-bit or 4-bit Data width (DAT[0] used, MMC, SD cards) 0x1: 8-bit Data width (DAT[7:0] used, MMC cards)	RW	0
4	MODE	Mode select All cards This bit select between Functional mode and SYSTEST mode. 0x0: Functional mode. Transfers to the MMC/SD/SDIO cards follow the card protocol. MMC clock is enabled. MMC/SD transfers are operated under the control of the CMD register. 0x1: SYSTEST mode The signal pins are configured as general-purpose input/output and the 1024-byte buffer is configured as a stack memory accessible only by the local host or system DMA. The pins retain their default type (input, output or in-out). SYSTEST mode is operated under the control of the SYSTEST register.	RW	0
3	STR	Stream command Only for MMC cards. This bit must be set to 1 only for the stream data transfers (read or write) of the adtc commands. Stream read is a class 1 command (CMD11: READ_DAT_UNTIL_STOP). Stream write is a class 3 command (CMD20: WRITE_DAT_UNTIL_STOP). 0x0: Block oriented data transfer 0x1: Stream oriented data transfer	RW	0
2	HR	Broadcast host response Only for MMC cards. This register is used to force the host to generate a 48-bit response for bc command type. It can be used to terminate the interrupt mode by generating a CMD40 response by the core (see section 4.3, "Interrupt Mode", in the MMC specification). In order to have the host response to be generated in open drain mode, the register MMCHS_CON[OD] must be set to 1. When MMCHS_CON[CEATA] is set to 1 and MMCHS_ARG set to 0x00000000 when writing 0x00000000 into MMCHS_CMD register, the host controller performs a 'command completion signal disable' token i.e. CMD line held to '0' during 47 cycles followed by a 1. 0x0: The host does not generate a 48-bit response instead of a command. 0x1: The host generates a 48-bit response instead of a command or a command completion signal disable token.	RW	0

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Bits	Field Name	Description	Type	Reset
1	INIT	Send initialization stream All cards. When this bit is set to 1, and the card is idle, an initialization sequence is sent to the card. An initialization sequence consists of setting the CMD line to 1 during 80 clock cycles. The initialisation sequence is mandatory - but it is not required to do it through this bit - this bit makes it easier. Clock divider (MMCHS_SYSCTL[CLKD]) should be set to ensure that 80 clock periods are greater than 1ms. (see section 9.3, "Power-Up", in the MMC card specification, or section 6.4 in the SD card specification). Note: in this mode, there is no command sent to the card and no response is expected 0x0: The host does not send an initialization sequence. 0x1: The host sends an initialization sequence.	RW	0
0	OD	Card open drain mode. Only for MMC cards. This bit must be set to 1 for MMC card commands 1, 2, 3 and 40, and if the MMC card bus is operating in open-drain mode during the response phase to the command sent. Typically, during card identification mode when the card is either in idle, ready or ident state. It is also necessary to set this bit to 1, for a broadcast host response (see Broadcast host response register MMCHS_CON[HR]) 0x0: No Open Drain 0x1: Open Drain or Broadcast host response	RW	0

Table 24-75. Register Call Summary for Register MMCHS_CON

MMC/SDIO Functional Description

- Power Management: [0] [1] [2] [3]
- Interrupt Requests: [4]
- DMA Modes: [5] [6] [7]
- Slave DMA Operations: [8]
- Generation on Rising Edge of MMC Clock: [9]
- MMC CE-ATA Command Completion Disable Management: [10] [11] [12]
- Test Registers: [13]

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- MMC/SDIO Host Controller Initialization Flow: [14]
- Basic Operations for MMC/SDIO Host Controller: [15] [16] [17] [18] [19]
- Bus Voltage Selection: [20]
- Boot Mode Configuration: [21] [22] [23] [24]

MMC/SDIO Register Manual

- MMC/SDIO Register Summary: [25] [26]
- MMC/SDIO Register Description: [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47]

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Table 24-76. MMCHS_PWCNT

Address Offset	0x0000 0130
Physical Address	0x4809 C130 0x480B 4130 0x480B 4130 0x480A D130 0x480D 1130 0x480D 1130 0x480D 5130 0x480D 5130
Description	Power Counter Register This register is used to program a mmc counter to delay command transfers after activating the PAD power, this value depends on PAD characteristics and voltage.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWRCNT															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:0	PWRCNT	Power counter register. This register is used to introduce a delay between the PAD ACTIVE pin assertion and the command issued. 0xFFFF: TCF x 65535 delay (card clock period) 0x0: No additional delay added 0x1: TCF delay (card clock period) 0xFFFE: TCF x 65534 delay (card clock period) 0x2: TCF x 2 delay (card clock period)	RW	0x0000

Table 24-77. Register Call Summary for Register MMCHS_PWCNT

MMC/SDIO Functional Description
- Power Management: [0] [1]

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- MMC/SDIO Register Summary: [2] [3]

Table 24-78. MMCHS_DLL

Address Offset	0x0000 0134
Physical Address	0x4809 C134 0x480B 4134 0x480B 4134
Description	DLL control and status register This register is used for tuning procedure required for SDR104 speed mode. It gives visibility and control on the DLL
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLL_SOFT_RESET	LOCK_TIMER	MAX_LOCK_DIFF								FORCE_SR_F	FORCE_SR_C								FORCE_VALUE	SLAVE_RATIO						RESERVED				DLL_UNLOCK_CLEAR	DLL_UNLOCK_STICKY	DLL_CALIB	DLL_LOCK

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Bits	Field Name	Description	Type	Reset
31	DLL_SOFT_RESET	Soft reset for DLL, active HIGH. Write 0x0: No action. Write 0x1: Issue soft reset Read 0x1: Reset is in progress Read 0x0: Reset completed.	RW	1
30	LOCK_TIMER	Timer for the dll_lock signal to be asserted after reset. 0x0: 1024 cycles (equivalent to DLL fast mode lock) 0x1: 66560 cycles	RW	0
29:22	MAX_LOCK_DIFF	Maximum number of taps that the master DLL clock period measurement can deviate without resulting in the master DLL losing lock.	RW	0x00
21:20	FORCE_SR_F	Forced fine delay value.	RW	0x0
19:13	FORCE_SR_C	Forced coarse delay value	RW	0x00
12	FORCE_VALUE	Put forced values to slave DLL, ignoring master DLL output and ratio value. 0x0: Do not put force value 0x1: Put force value.	RW	0
11:6	SLAVE_RATIO	Fraction of a clock cycle for the shift to be implemented, in units of 256ths of a clock cycle. 0x6: 135 degrees delay 0x3F: 4 clocks delay 0x8: 180 degrees delay 0x2: 45 degrees delay 0xA: 225 degrees delay 0x10: Full clock delay 0x0: 0 degree delay 0xC: 270 degrees delay 0x4: 90 degrees delay 0xE: 315 degrees delay	RW	0x00
5:4	RESERVED		R	0x0
3	DLL_UNLOCK_CLEAR	Clears the phy_reg_status_mdll_unlock_sticky flags of the DLL. 0x0: No effect. 0x1: Clears the flag.	RW	0
2	DLL_UNLOCK_STICKY	Asserted when any single period measurement exceeds MAX_LOCK_DIFF.	R	0
1	DLL_CALIB	Enables Slave DLL to update new delay values. 0x0: Disabled 0x1: Enabled	RW	0
0	DLL_LOCK	Master DLL lock status. Read 0x1: DLL is locked Read 0x0: DLL is not locked	R	0

Table 24-79. Register Call Summary for Register MMCHS_DLL

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- MMC/SDIO Register Summary: [0]

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Table 24-80. MMCHS_SDMASA

Address Offset	0x0000 0200
Physical Address	0x4809 C200 0x480B 4200 0x480B 4200 0x480A D200 0x480D 1200 0x480D 1200 0x480D 5200 0x480D 5200
Description	SDMA System Address / Argument 2 Register
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMA_ARG2																															

Bits	Field Name	Description	Type	Reset
31:0	SDMA_ARG2	SDMA System Address / Argument 2 This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23. (1) SDMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register. (2) Argument 2 This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23. If Auto CMD23 is used with ADMA, the full 32-bit block count value can be used. If Auto CMD23 is used without AMDA, the available block count value is limited by the Block Count register. 65535 blocks is the maximum value in this case.	RW	0x0000 0000

Table 24-81. Register Call Summary for Register MMCHS_SDMASA

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- MMC/SDIO Register Summary: [0] [1]
- MMC/SDIO Register Description: [2]

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Table 24-82. MMCHS_BLK

Address Offset	0x0000 0204
Physical Address	0x4809 C204 0x480B 4204 0x480B 4204 0x480A D204 0x480D 1204 0x480D 1204 0x480D 5204 0x480D 5204
Description	Transfer Length Configuration Register MMCHS_BLK[BLEN] is the block size register. MMCHS_BLK[NBLK] is the block count register. This register shall be used for any card.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NBLK																RESERVED				BLEN											

Bits	Field Name	Description	Type	Reset
31:16	NBLK	Blocks count for current transfer This register is enabled when Block count Enable (MMCHS_CMD[BCE]) is set to 1 and is valid only for multiple block transfers. Setting the block count to 0 results no data blocks being transferred. Note: The host controller decrements the block count after each block transfer and stops when the count reaches zero. This register can be accessed only if no transaction is executing (i.e, after a transaction has stopped). Read operations during transfers may return an invalid value and write operation will be ignored. In suspend context, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, The local host shall restore the previously saved block count. 0xFFFF: 65535 blocks 0x0: Stop count 0x1: 1 block 0x2: 2 blocks	RW	0x0000
15:12	RESERVED		R	0x0
11:0	BLEN	Transfer Block Size. This register specifies the block size for block data transfers. Read operations during transfers may return an invalid value, and write operations are ignored. When a CMD12 command is issued to stop the transfer, a read of the BLEN field after transfer completion (MMCHS_STAT[TC] set to 1) will not return the true byte number of data length while the stop occurs but the value written in this register before transfer is launched. 0x1: 1 byte block length 0x7FF: 2047 bytes block length 0x0: No data transfer 0x1FF: 511 bytes block length 0x800: 2048 bytes block length 0x2: 2 bytes block length 0x3: 3 bytes block length 0x200: 512 bytes block length	RW	0x000

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Table 24-83. Register Call Summary for Register MMCHS_BLK

MMC/SDIO Functional Description • Interrupt Requests: [0] [1] • Requirements for Descriptors: [2] • DMA Receive Mode: [3] • DMA Transmit Mode: [4] • Data Buffer: [5]
MMC/SDIO Programming Guide • Basic Operations for MMC/SDIO Host Controller: [6] [7] [8] [9] • Boot Mode Configuration: [10] [11]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [12] [13] • MMC/SDIO Register Description: [14] [15] [16] [17] [18] [19] [20] [21] [22]

Table 24-84. MMCHS_ARG

Address Offset	0x0000 0208
Physical Address	0x4809 C208 0x480B 4208 0x480B 4208 0x480A D208 0x480D 1208 0x480D 1208 0x480D 5208 0x480D 5208
Description	Command Argument Register This register contains command argument specified as bit 39-8 of Command-Format These registers must be initialized prior to sending the command itself to the card (write action into the register MMCHS_CMD register). Only exception is for a command index specifying stuff bits in arguments, making a write unnecessary.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARG																															

Bits	Field Name	Description	Type	Reset
31:0	ARG	Command argument bits [31:0]	RW	0x0000 0000

Table 24-85. Register Call Summary for Register MMCHS_ARG

MMC/SDIO Functional Description • MMC CE-ATA Command Completion Disable Management: [0]
MMC/SDIO Programming Guide • Basic Operations for MMC/SDIO Host Controller: [1] [2] [3] • Boot Mode Configuration: [4] [5]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [6] [7] • MMC/SDIO Register Description: [8]

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Table 24-86. MMCHS_CMD

Address Offset	0x0000 020C
Physical Address	0x4809 C20C 0x480B 420C 0x480B 420C 0x480A D20C 0x480D 120C 0x480D 120C 0x480D 520C 0x480D 520C
Description	Command and Transfer Mode Register MMCHS_CMD[31:16] = the command register MMCHS_CMD[15:0] = the transfer mode. This register configures the data and command transfers. A write into the most significant byte send the command. A write into MMCHS_CMD[15:0] registers during data transfer has no effect. This register shall be used for any card. Note: In SYSTEST mode, a write into MMCHS_CMD register will not start a transfer.
Type	RW

31 30	29 28 27 26 25 24	23 22	21	20	19	18	17 16	15 14 13 12 11 10 9 8	7 6	5	4	3 2	1	0
RESERVED	INDX	CMD_TYPE	DP	CICE	CCCE	RESERVED	RSP_TYPE	RESERVED		MSBS	DDIR	ACEN	BCE	DE

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29:24	INDX	Command index Binary encoded value from 0 to 63 specifying the command number send to card 0xD: CMD13 or ACMD13 0x33: CMD51 or ACMD51 0x3B: CMD59 or ACMD59 0x15: CMD21 or ACMD21 0x1E: CMD30 or ACMD30 0x8: CMD8 or ACMD8 0x5: CMD5 or ACMD5 0x2E: CMD46 or ACMD46 0x1B: CMD27 or ACMD27 0x2C: CMD44 or ACMD44 0x36: CMD54 or ACMD54 0x2: CMD2 or ACMD2 0x3E: CMD62 or ACMD62 0x4: CMD4 or ACMD4 0x39: CMD57 or ACMD57 0x32: CMD50 or ACMD50 0x6: CMD6 or ACMD6 0x1: CMD1 or ACMD1 0x1D: CMD29 or ACMD29 0x3F: CMD63 or ACMD63 0x28: CMD40 or ACMD40 0x3A: CMD58 or ACMD58 0x24: CMD36 or ACMD36 0x0: CMD0 or ACMD0	RW	0x00

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Bits	Field Name	Description	Type	Reset
		0x2D: CMD45 or ACMD45		
		0x38: CMD56 or ACMD56		
		0x3C: CMD60 or ACMD60		
		0xB: CMD11 or ACMD11		
		0x3D: CMD61 or ACMD61		
		0x20: CMD32 or ACMD32		
		0x3: CMD3 or ACMD3		
		0x17: CMD23 or ACMD23		
		0x30: CMD48 or ACMD48		
		0x31: CMD49 or ACMD49		
		0x11: CMD17 or ACMD17		
		0x23: CMD35 or ACMD35		
		0x35: CMD53 or ACMD53		
		0x2F: CMD47 or ACMD47		
		0xA: CMD10 or ACMD10		
		0x9: CMD9 or ACMD9		
		0x10: CMD16 or ACMD16		
		0x26: CMD38 or ACMD38		
		0x21: CMD33 or ACMD33		
		0x25: CMD37 or ACMD37		
		0x12: CMD18 or ACMD18		
		0x13: CMD19 or ACMD19		
		0x2B: CMD43 or ACMD43		
		0x37: CMD55 or ACMD55		
		0x18: CMD24 or ACMD24		
		0x14: CMD20 or ACMD20		
		0xE: CMD14 or ACMD14		
		0x16: CMD22 or ACMD22		
		0x2A: CMD42 or ACMD42		
		0x1C: CMD28 or ACMD28		
		0x7: CMD7 or ACMD7		
		0x19: CMD25 or ACMD25		
		0x1F: CMD31 or ACMD31		
		0x34: CMD52 or ACMD52		
		0x1A: CMD26 or ACMD26		
		0x29: CMD41 or ACMD41		
		0xF: CMD15 or ACMD15		
		0xC: CMD12 or ACMD12		
		0x27: CMD39 or ACMD39		
		0x22: CMD34 or ACMD34		
23:22	CMD_TYPE	Command type This register specifies three types of special command: Suspend, Resume and Abort. These bits shall be set to 00b for all other commands. 0x0: Others Commands 0x1: CMD52 for writing "Bus Suspend" in CCCR 0x3: Abort command CMD12, CMD52 for writing " I/O Abort" in CCCR 0x2: CMD52 for writing "Function Select" in CCCR	RW	0x0
21	DP	Data present select	RW	0

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Bits	Field Name	Description	Type	Reset
		This register indicates that data is present and DAT line shall be used. It must be set to 0 in the following conditions: - command using only CMD line - command with no data transfer but using busy signal on DAT[0] - Resume command 0x0: Command with no data transfer 0x1: Command with data transfer		
20	CICE	Command Index check enable This bit must be set to 1 to enable index check on command response to compare the index field in the response against the index of the command. If the index is not the same in the response as in the command, it is reported as a command index error (MMCHS_STAT[CIE] set to1). **Note:** The register CICE cannot be configured for an Auto CMD12, then index check is automatically checked when this command is issued. 0x0: Index check disable 0x1: Index check enable	RW	0
19	CCCE	Command CRC check enable This bit must be set to 1 to enable CRC7 check on command response to protect the response against transmission errors on the bus. If an error is detected, it is reported as a command CRC error (MMCHS_STAT[CCRC] set to 1). **Note:** The register CCCE cannot be configured for an Auto CMD12, and then CRC check is automatically checked when this command is issued. 0x0: CRC7 check disable 0x1: CRC7 check enable	RW	0
18	RESERVED		R	0
17:16	RSP_TYPE	Response type This bits defines the response type of the command 0x0: No response 0x1: Response Length 136 bits 0x3: Response Length 48 bits with busy after response 0x2: Response Length 48 bits	RW	0x0
15:6	RESERVED		R	0x000
5	MSBS	Multi/Single block select This bit must be set to 1 for data transfer in case of multi block command. For any others command this bit shall be set to 0. 0x0: Single block. If this bit is 0, it is not necessary to set the register MMCHS_BLK[NBLK]. 0x1: Multi block. When Block Count is disabled (MMCHS_CMD[BCE] is set to 0) in Multiple block transfers (MMCHS_CMD[MSBS] is set to 1), the module can perform infinite transfer.	RW	0
4	DDIR	Data transfer Direction Select This bit defines either data transfer will be a read or a write.	RW	0

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Bits	Field Name	Description	Type	Reset
		0x0: Data Write (host to card) 0x1: Data Read (card to host)		
3:2	ACEN	Auto CMD Enable - SD card only. This field determines use of auto command functions. There are two methods to stop Multiple-block read and write operation 1. Auto CMD12 Enable When this field is set to 01b, the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the Auto CMD Error Status register (MMCHS_AC12). The Host Driver shall not set this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. 2. Auto CMD23 Enable When this bit field is set to 10b, the Host Controller issues a CMD23 automatically before issuing a command specified in the Command Register. The Host Controller Version 3.00 and later shall support this function. The following conditions are required to use the Auto CMD23. – Auto CMD23 Supported (Host Controller Version is 3.00 or later) – A memory card that supports CMD23 (SCR[33]=1) – If DMA is used, it shall be ADMA. –Only when CMD18 or CMD25 is issued (**Note:** the Host Controller does not check command index.) Auto CMD23 can be used with or without ADMA. By writing the Command register, the Host Controller issues a CMD23 first and then issues a command specified by the Command Index in Command register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the Auto CMD Error Status register (MMCHS_AC12). 32-bit block count value for CMD23 is set to SDMA System Address / Argument 2 register (MMCHS_SDMASA). 0x0: Auto Command Disabled 0x1: Auto CMD12 enable or CCS detection enabled. 0x3: Reserved 0x2: Auto CMD23 Enable	RW	0x0
1	BCE	Block Count Enable Multiple block transfers only. This bit is used to enable the block count register (MMCHS_BLK[NBLK]). When Block Count is disabled (MMCHS_CMD[BCE] is set to 0) in Multiple block transfers (MMCHS_CMD[MSBS] is set to 1), the module can perform infinite transfer. 0x0: Block count disabled for infinite transfer.	RW	0

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Bits	Field Name	Description	Type	Reset
		0x1: Block count enabled for multiple block transfer with known number of blocks		
0	DE	DMA Enable This bit is used to enable DMA mode for host data access. 0x0: DMA mode disable 0x1: DMA mode enable	RW	0

Table 24-87. Register Call Summary for Register MMCHS_CMD

MMC/SDIO Environment
- Data Format: [0] [1] [2] [3]

MMC/SDIO Functional Description
- Interrupt Requests: [4] [5]
- Requirements for Descriptors: [6]
- Slave DMA Operations: [7]
- Data Buffer: [8]
- Memory Size, Block Length, and Buffer-Management Relationship: [9] [10]
- Transfer Stop: [11]
- MMC CE-ATA Command Completion Disable Management: [12] [13]

MMC/SDIO Programming Guide
- Basic Operations for MMC/SDIO Host Controller: [14] [15] [16] [17] [18] [19] [20]
- Bus Voltage Selection: [21]
- Boot Mode Configuration: [22] [23]

MMC/SDIO Register Manual
- MMC/SDIO Register Summary: [24] [25]
- MMC/SDIO Register Description: [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45]

Table 24-88. MMCHS_RSP10

Address Offset	0x0000 0210
Physical Address	0x4809 C210 0x480B 4210 0x480B 4210 0x480A D210 0x480D 1210 0x480D 1210 0x480D 5210 0x480D 5210
Description	Command Response[31:0] Register This 32-bit register holds bits positions [31:0] of command response type R1/R1b/R2/R3/R4/R5/R5b/R6/R7
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSP1																RSP0															

Bits	Field Name	Description	Type	Reset
31:16	RSP1	Command Response [31:16]	R	0x0000
15:0	RSP0	Command Response [15:0]	R	0x0000

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Table 24-89. Register Call Summary for Register MMCHS_RSP10

MMC/SDIO Functional Description • Different Types of Responses: [0] [1] [2] [3]
MMC/SDIO Programming Guide • Basic Operations for MMC/SDIO Host Controller: [4] [5] [6] [7]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [8] [9]

Table 24-90. MMCHS_RSP32

Address Offset	0x0000 0214
Physical Address	0x4809 C214 0x480B 4214 0x480B 4214 0x480A D214 0x480D 1214 0x480D 1214 0x480D 5214 0x480D 5214
Description	Command Response[63:32] Register This 32-bit register holds bits positions [63:32] of command response type R2
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSP3																RSP2															

Bits	Field Name	Description	Type	Reset
31:16	RSP3	Command Response [63:48]	R	0x0000
15:0	RSP2	Command Response [47:32]	R	0x0000

Table 24-91. Register Call Summary for Register MMCHS_RSP32

MMC/SDIO Functional Description • Different Types of Responses: [0]
MMC/SDIO Programming Guide • Basic Operations for MMC/SDIO Host Controller: [1] [2] [3]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [4] [5]

Table 24-92. MMCHS_RSP54

Address Offset	0x0000 0218
Physical Address	0x4809 C218 0x480B 4218 0x480B 4218 0x480A D218 0x480D 1218 0x480D 1218 0x480D 5218 0x480D 5218
Description	Command Response[95:64] Register This 32-bit register holds bits positions [95:64] of command response type R2
Type	R

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSP5																RSP4															

Bits	Field Name	Description	Type	Reset
31:16	RSP5	Command Response [95:80]	R	0x0000
15:0	RSP4	Command Response [79:64]	R	0x0000

Table 24-93. Register Call Summary for Register MMCHS_RSP54

MMC/SDIO Functional Description • Different Types of Responses: [0]
MMC/SDIO Programming Guide • Basic Operations for MMC/SDIO Host Controller: [1] [2] [3]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [4] [5]

Table 24-94. MMCHS_RSP76

Address Offset	0x0000 021C
Physical Address	0x4809 C21C 0x480B 421C 0x480B 421C 0x480A D21C 0x480D 121C 0x480D 121C 0x480D 521C 0x480D 521C
Description	Command Response[127:96] Register This 32-bit register holds bits positions [127:96] of command response type R1(Auto CMD23)/R1b(Auto CMD12)/R2
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSP7																RSP6															

Bits	Field Name	Description	Type	Reset
31:16	RSP7	Command Response [127:112]	R	0x0000
15:0	RSP6	Command Response [111:96]	R	0x0000

Table 24-95. Register Call Summary for Register MMCHS_RSP76

MMC/SDIO Functional Description • Different Types of Responses: [0] [1] [2] [3]
MMC/SDIO Programming Guide • Basic Operations for MMC/SDIO Host Controller: [4] [5] [6]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [7] [8] • MMC/SDIO Register Description: [9]

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Table 24-96. MMCHS_DATA

Address Offset	0x0000 0220
Physical Address	0x4809 C220 0x480B 4220 0x480B 4220 0x480A D220 0x480D 1220 0x480D 1220 0x480D 5220 0x480D 5220
Description	Data Register This register is the 32-bit entry point of the buffer for read or write data transfers. The buffer size is 32bits x256(1024 bytes). Bytes within a word are stored and read in little endian format. This buffer can be used as two 512 byte buffers to transfer data efficiently without reducing the throughput. Sequential and contiguous access is necessary to increment the pointer correctly. Random or skipped access is not allowed. In little endian, if the local host accesses this register byte-wise or 16bit-wise, the least significant byte (bits [7:0]) must always be written/read first. The update of the buffer address is done on the most significant byte write for full 32-bit DATA register or on the most significant byte of the last word of block transfer. Example 1: Byte or 16-bit access Mbyteen[3:0]=0001 (1-byte) => Mbyteen[3:0]=0010 (1-byte) => Mbyteen[3:0]=1100 (2-bytes) OK Mbyteen[3:0]=0001 (1-byte) => Mbyteen[3:0]=0010 (1-byte) => Mbyteen[3:0]=0100 (1-byte) OK Mbyteen[3:0]=0001 (1-byte) => Mbyteen[3:0]=0010 (1-byte) => Mbyteen[3:0]=1000 (1-byte) Bad
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															

Bits	Field Name	Description	Type	Reset
31:0	DATA	Data Register [31:0] In functional mode (MMCHS_CON[MODE] set to the default value 0) , A read access to this register is allowed only when the buffer read enable status is set to 1 (MMCHS_PSTATE[BRE]), otherwise a bad access (MMCHS_STAT[BADA]) is signaled. A write access to this register is allowed only when the buffer write enable status is set to 1(MMCHS_STATE[BWE]), otherwise a bad access (MMCHS_STAT[BADA]) is signaled and the data is not written.	RW	0x0000 0000

Table 24-97. Register Call Summary for Register MMCHS_DATA

MMC/SDIO Functional Description

- Interrupt Requests: [0] [1]
- Data Buffer: [2] [3] [4] [5] [6] [7] [8] [9]
- Transfer or Command Status and Errors Reporting: [10]

MMC/SDIO Programming Guide

- Basic Operations for MMC/SDIO Host Controller: [11]

MMC/SDIO Register Manual

- MMC/SDIO Register Summary: [12] [13]
- MMC/SDIO Register Description: [14] [15] [16] [17] [18] [19]

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Table 24-98. MMCHS_PSTATE

Address Offset	0x0000 0224
Physical Address	0x4809 C224 0x480B 4224 0x480B 4224 0x480A D224 0x480D 1224 0x480D 1224 0x480D 5224 0x480D 5224
Description	Present State Register The Host can get status of the Host Controller from this 32-bit read only register.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CLEV	DLEV				WP	CDPL	CSS	CINS	RESERVED				BRE	BWE	RTA	WTA	RESERVED				RTR	DLA	DATI	CMDI

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLEV	CMD line signal level This status is used to check the CMD line level to recover from errors, and for debugging. The value of this register after reset depends on the CMD line level at that time. Read 0x1: The CMD line level is 1. Read 0x0: The CMD line level is 0.	R	-
23:20	DLEV	DAT[3:0] line signal level DAT[3] => bit 23 DAT[2] => bit 22 DAT[1] => bit 21 DAT[0] => bit 20 This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. The value of these registers after reset depends on the DAT lines level at that time.	R	0x-
19	WP	Write protect switch pin level For SDIO cards only. This bit reflects the write protect input pin (sdcard_wp) level. The value of this register after reset depends on the protect input pin (sdcard_wp) level at that time. Read 0x1: If MMCHS_CON[WPP] is set to 0 (default), the card is not write protected, otherwise the card is protected. Read 0x0: If MMCHS_CON[WPP] is set to 0 (default), the card is write protected, otherwise the card is not protected.	R	-
18	CDPL	Card detect pin level This bit reflects the inverse value of the card detect input pin (sdcard_cd), debouncing is not performed on this bit and bit is valid only when Card State Stable (MMCHS_PSTAE[CSS]) is set to 1. Use of this bit is limited to testing since it must be debounced y software. The value of this register after reset depends on the card detect input pin (sdcard_cd) level at that time. Read 0x1: The value of the card detect input pin (sdcard_cd) is 0 Read 0x0: The value of the card detect input pin (sdcard_cd) is 1	R	-

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Bits	Field Name	Description	Type	Reset
17	CSS	Card State Stable This bit is used for testing. It is set to 1 only when Card Detect Pin Level is stable (MMCHS_PSTATE[CDPL]). Debouncing is performed on the card detect input pin (sdcard_cd) to detect card stability. This bit is not affected by a software reset. Read 0x1: No card or card inserted Read 0x0: Reset or Debouncing	R	0
16	CINS	Card inserted This bit is the debounced value of the card detect input pin (sdcard_cd). An inactive to active transition of the card detect input pin (sdcard_cd) will generate a card insertion interrupt (MMCHS_STAT[CINS]). A active to inactive transition of the card detect input pin (sdcard_cd) will generate a card removal interrupt (MMCHS_STAT[REM]). This bit is not affected by a software reset. Read 0x1: If MMCHS_CON[CDP] is set to 1, the card has been inserted from the card slot. If MMCHS_CON[CDP] is set to 0, no card is detected. The card may have been removed from the card slot. Read 0x0: If MMCHS_CON[CDP] is set to 1, no card is detected. The card may have been removed from the card slot. If MMCHS_CON[CDP] is set to 0, the card has been inserted.	R	0
15:12	RESERVED		R	0x0
11	BRE	Buffer read enable This bit is used for non-DMA read transfers. It indicates that a complete block specified by MMCHS_BLK[BLEN] has been written in the buffer and is ready to be read. It is set to 0 when the entire block is read from the buffer. It is set to 1 when a block data is ready in the buffer and generates the Buffer read ready status of interrupt (MMCHS_STAT[BRR]). Read 0x1: Read BLEN bytes enable. Readable data exists in the buffer. Read 0x0: Read BLEN bytes disable	R	0
10	BWE	Buffer Write enable This status is used for non-DMA write transfers. It indicates if space is available for write data. Read 0x1: There is enough space in the buffer to write BLEN bytes of data. Read 0x0: There is no room left in the buffer to write BLEN bytes of data.	R	0
9	RTA	Read transfer active This status is used for detecting completion of a read transfer. It is set to 1 after the end bit of read command or by activating a continue request (MMCHS_HCTL[CR]) following a stop at block gap request. This bit is set to 0 when all data have been read by the local host after last block or after a stop at block gap request. Read 0x1: read data transfer on going. Read 0x0: No valid data on the DAT lines.	R	0

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Bits	Field Name	Description	Type	Reset
8	WTA	Write transfer active This status indicates a write transfer active. It is set to 1 after the end bit of write command or by activating a continue request (MMCHS_HCTL[CR]) following a stop at block gap request. This bit is set to 0 when CRC status has been received after last block or after a stop at block gap request. Read 0x1: Write data transfer on going. Read 0x0: No valid data on the DAT lines.	R	0
7:4	RESERVED		R	0x0
3	RTR	Re-Tuning Request Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting MMCHS_AC12[22] ET. This bit isn't set to 1 if MMCHS_AC12[23] SCLK_SEL is set to 0 (using fixed sampling clock). Refer to MMCHS_CAPA2[15:14] RTM for more detail. Read 0x1: Sampling clock needs re-tuning Read 0x0: Fixed or well tuned sampling clock	R	0
2	DLA	DAT line active This status bit indicates whether one of the DAT line is in use. In the case of read transactions (card to host): This bit is set to 1 after the end bit of read command or by activating continue request MMCHS_HCTL[CR]. This bit is set to 0 when the host controller received the end bit of the last data block or at the beginning of the read wait mode. In the case of write transactions (host to card): This bit is set to 1 after the end bit of write command or by activating continue request MMCHS_HCTL[CR]. This bit is set to 0 on the end of busy event for the last block; host controller must wait 8 clock cycles with line not busy to really consider not "busy state" or after the busy block as a result of a stop at gap request. Read 0x1: DAT Line active Read 0x0: DAT Line inactive	R	0
1	DATI	Command inhibit(DAT) This status bit is generated if either DAT line is active (MMCHS_PSTATE[DLA]) or Read transfer is active (MMCHS_PSTATE[RTA]) or when a command with busy is issued. This bit prevents the local host to issue a command. A change of this bit from 1 to 0 generates a transfer complete interrupt (MMCHS_STAT[TC]). Read 0x1: Issuing of command using DAT lines is not allowed Read 0x0: Issuing of command using the DAT lines is allowed	R	0

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Bits	Field Name	Description	Type	Reset
0	CMDI	Command inhibit(CMD) This status bit indicates that the CMD line is in use. This bit is set to 0 when the most significant byte is written into the command register. This bit is not set when Auto CMD12 is transmitted. This bit is set to 0 in either the following cases: - After the end bit of the command response, excepted if there is a command conflict error (MMCHS_STAT[CCRC] or MMCHS_STAT[CEB] set to 1) or a Auto CMD12 is not executed (MMCHS_AC12[ACNE]). - After the end bit of the command without response (MMCHS_CMD[RSP_TYPE] set to "00") In case of a command data error is detected (MMCHS_STAT[CTO] set to 1), this register is not automatically cleared. Read 0x1: Issuing of command using CMD line is not allowed Read 0x0: Issuing of command using CMD line is allowed	R	0

Table 24-99. Register Call Summary for Register MMCHS_PSTATE

MMC/SDIO Functional Description

- Software Reset: [0]
- Interrupt Requests: [1] [2] [3] [4] [5] [6] [7]
- Requirements for Descriptors: [8] [9] [10]
- Data Buffer: [11] [12]
- Data Buffer Status: [13] [14]
- Test Registers: [15]
- MMC/SDIO Hardware Status Features: [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29]

MMC/SDIO Programming Guide

- Basic Operations for MMC/SDIO Host Controller: [30] [31] [32] [33] [34] [35]
- Bus Voltage Selection: [36]

MMC/SDIO Register Manual

- MMC/SDIO Register Summary: [37] [38]
- MMC/SDIO Register Description: [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55]

Table 24-100. MMCHS_HCTL

Address Offset 0x0000 0228

Physical Address
0x4809 C228
0x480B 4228
0x480B 4228
0x480A D228
0x480D 1228
0x480D 1228
0x480D 5228
0x480D 5228

Description Host Control Register
This register defines the host controls to set power, wakeup and transfer parameters.
MMCHS_HCTL[31:24] = Wakeup control
MMCHS_HCTL[23:16] = Block gap control
MMCHS_HCTL[15:8] = Power control
MMCHS_HCTL[7:0] = Host control

Type RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				OBWE	REM	INS	IWE	RESERVED				IBG	RWC	CR	SBGR	RESERVED				SDVS			SDBP	CDSS	CDTL	RESERVED	DMAS		HSPE	DTW	LED

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Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27	OBWE	Wakeup event enable for 'Out-of-Band' Interrupt. This bit enables wakeup events for 'Out-of-Band' assertion. Wakeup is generated if the wakeup feature is enabled (MMCHS_SYSCONFIG[ENAWAKEUP]). The write to this register is ignored when MMCHS_CON[OBIE] is not set. 0x0: Disable wakeup on 'Out-of-Band' Interrupt 0x1: Enable wakeup on 'Out-of-Band' Interrupt	RW	0
26	REM	Wakeup event enable on SD card removal This bit enables wakeup events for card removal assertion. Wakeup is generated if the wakeup feature is enabled (MMCHS_SYSCONFIG[ENAWAKEUP]). 0x0: Disable wakeup on card removal 0x1: Enable wakeup on card removal	RW	0
25	INS	Wakeup event enable on SD card insertion This bit enables wakeup events for card insertion assertion. Wakeup is generated if the wakeup feature is enabled (MMCHS_SYSCONFIG[ENAWAKEUP]). 0x0: Disable wakeup on card insertion 0x1: Enable wakeup on card insertion	RW	0
24	IWE	Wakeup event enable on SD card interrupt This bit enables wakeup events for card interrupt assertion. Wakeup is generated if the wakeup feature is enabled (MMCHS_SYSCONFIG[ENAWAKEUP]). 0x0: Disable wakeup on card interrupt 0x1: Enable wakeup on card interrupt	RW	0
23:20	RESERVED		R	0x0
19	IBG	Interrupt block at gap This bit is valid only in 4-bit mode of SDIO card to enable interrupt detection in the interrupt cycle at block gap for a multiple block transfer. For MMC cards and for SD card this bit should be set to 0. 0x0: Disable interrupt detection at the block gap in 4-bit mode 0x1: Enable interrupt detection at the block gap in 4-bit mode	RW	0
18	RWC	Read wait control The read wait function is optional only for SDIO cards. If the card supports read wait, this bit must be enabled, then requesting a stop at block gap (MMCHS_HCTL[SBGR]) generates a read wait period after the current end of block. Be careful, if read wait is not supported it may cause a conflict on DAT line. 0x0: Disable Read Wait Control. Suspend/Resume cannot be supported. 0x1: Enable Read Wait Control	RW	0
17	CR	Continue request This bit is used to restart a transaction that was stopped by requesting a stop at block gap (MMCHS_HCTL[SBGR]). Set this bit to 1 restarts the transfer. The bit is automatically set to 0 by the host controller when transfer has restarted i.e DAT line is active (MMCHS_PSTATE[DLA]) or transferring data (MMCHS_PSTATE[WTA]). The Stop at block gap request must be disabled (MMCHS_HCTL[SBGR]=0) before setting this bit. 0x0: No affect 0x1: transfer restart	RW	0

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Bits	Field Name	Description	Type	Reset
16	SBGR	Stop at block gap request This bit is used to stop executing a transaction at the next block gap. The transfer can restart with a continue request (MMCHS_HCTL[CR]) or during a suspend/resume sequence. In case of read transfer, the card must support read wait control. In case of write transfer, the host driver shall set this bit after all block data written. Until the transfer completion (MMCHS_STAT[TC] set to 1), the host driver shall leave this bit set to 1. If this bit is set, the local host shall not write to the data register (MMCHS_DATA). 0x0: Transfer mode 0x1: Stop at block gap	RW	0
15:12	RESERVED		R	0x0
11:9	SDVS	SD bus voltage select All cards. The host driver should set to these bits to select the voltage level for the card according to the voltage supported by the system (MMCHS_CAPA[VS18,VS30,VS33]) before starting a transfer. 0x6: 3.0V (Typical) 0x7: 3.3V (Typical) 0x5: 1.8V (Typical)	RW	0x0
8	SDBP	SD bus power Before setting this bit, the host driver shall select the SD bus voltage (MMCHS_HCTL[SDVS]). If the host controller detects the No card state, this bit is automatically set to 0. If the module is power off, a write in the command register (MMCHS_CMD) will not start the transfer. A write to this bit has no effect if the selected SD bus voltage MMCHS_HCTL[SDVS] is not supported according to capability register (MMCHS_CAPA[VS*]). 0x0: Power off 0x1: Power on	RW	0
7	CDSS	Card Detect Signal Selection This bit selects source for the card detection.When the source for the card detection is switched, the interrupt should be disabled during the switching period by clearing the Interrupt Status/Signal Enable register in order to mask unexpected interrupts caused by the glitch. The Interrupt Status/Signal Enable should be disabled during over the period of debouncing. 0x0: sdcard_cd is selected (for normal use) 0x1: MMCHS_HCTL[6] CDTL is selected (for test purpose)	RW	0
6	CDTL	Card Detect Test Level: This bit is enabled while MMCHS_HCTL[7] CDSS is set to 1 and it indicates whether the card is inserted or not. 0x0: No Card 0x1: Card Inserted	RW	0
5	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
4:3	DMAS	DMA Select Mode: One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register MMCHS_CAPA . Use of selected DMA is determined by DMA Enable of the Transfer Mode register. This register is only meaningful when MADMA_EN is set to 1. When MADMA_EN is set to 0 the bit field is read only and returned value is 0. 0x0: Reserved 0x1: Reserved 0x3: Reserved 0x2: 32-bit Address ADMA2 is selected	RW	0x0
2	HSPE	High Speed Enable: Before setting this bit, the Host Driver shall check the MMCHS_CAPA[21] HSS. If this bit is set to 0, the Host Controller outputs CMD line and DAT lines at the falling edge of the SD Clock. If this bit is set to 1, the Host Controller outputs CMD line and DAT lines at the rising edge of the SD Clock.This bit shall not be set when dual data rate mode is activated in MMCHS_CON[DDR]. 0x0: Normal speed mode 0x1: High speed mode	RW	0
1	DTW	Data transfer width For MMC card, this bit must be set following a valid SWITCH command (CMD6) with the correct value and extend CSD index written in the argument. Prior to this command, the MMC card configuration register (CSD and EXT_CSD) must be verified for compliance with MMC standard specification 4.x (see section 3.6). This register has no effect when the MMC 8-bit mode is selected (register MMCHS_CON[DW8] set to1), For SD/SDIO cards, this bit must be set following a valid SET_BUS_WIDTH command (ACMD6) with the value written in bit 1 of the argument. Prior to this command, the SD card configuration register (SCR) must be verified for the supported bus width by the SD card. 0x0: 1-bit Data width (DAT[0] used) 0x1: 4-bit Data width (DAT[3:0] used)	RW	0
0	LED	Reserved bit. LED control feature is not supported This bit is initialized to zero, and writes to it are ignored.	R	0

Table 24-101. Register Call Summary for Register MMCHS_HCTL

MMC/SDIO Functional Description
- Power Management: [0] [1] [2] [3] [4] [5]
- Interrupt Requests: [6] [7]
- Requirements for Descriptors: [8]
- Transfer Stop: [9] [10]
- Output Signals Generation: [11]
- Generation on Falling Edge of MMC Clock: [12]
- Generation on Rising Edge of MMC Clock: [13]
- Test Registers: [14] [15]

MMC/SDIO Programming Guide
- MMC/SDIO Host Controller Initialization Flow: [16] [17]
- Basic Operations for MMC/SDIO Host Controller: [18] [19]

MMC/SDIO Register Manual
- MMC/SDIO Register Summary: [20] [21]
- MMC/SDIO Register Description: [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42]

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Table 24-102. MMCHS_SYSCTL

Address Offset	0x0000 022C
Physical Address	0x4809 C22C 0x480B 422C 0x480B 422C 0x480A D22C 0x480D 122C 0x480D 122C 0x480D 522C 0x480D 522C
Description	SD System Control Register This register defines the system controls to set software resets, clock frequency management and data timeout. MMCHS_SYSCTL[31:24] = Software resets MMCHS_SYSCTL[23:16] = Timeout control MMCHS_SYSCTL[15:0] = Clock control
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SRD	SRC	SRA	RESERVED				DTO				CLKD								CGS	RESERVED				CEN	ICS	ICE

Bits	Field Name	Description	Type	Reset
31:27	RESERVED		R	0x00
26	SRD	Software reset for DAT line This bit is set to 1 for reset and released to 0 when completed. For more information about SRD bit manipulation, see Section 24.5.1.2.1.2.1*DATA Lines Reset Procedure*. DAT finite state machine in both clock domain are also reset. Here below are the registers cleared by MMCHS_SYSCTL[SRD]: - MMCHS_DATA - MMCHS_PSTATE: BRE, BWE, RTA, WTA, DLA and DATI - MMCHS_HCTL: SBGR and CR - MMCHS_STAT: BRR, BWR, BGE and TC Interconnect and MMC buffer data management is reinitialized. 0x0: Reset completed 0x1: Software reset for DAT line	RW	0
25	SRC	Software reset for CMD line For more information about SRC bit manipulation, see Section 24.5.1.2.1.1.1 *CMD Line Reset Procedure*. This bit is set to 1 for reset and released to 0 when completed. CMD finite state machine in both clock domain are also reset. Here below the registers cleared by MMCHS_SYSCTL[SRC]: - MMCHS_PSTATE: CMDI - MMCHS_STAT: CC Interconnect and MMC command status management is reinitialized. 0x0: Reset completed 0x1: Software reset for CMD line	RW	0

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Bits	Field Name	Description	Type	Reset
24	SRA	Software reset for all This bit is set to 1 for reset , and released to 0 when completed. This reset affects the entire host controller except for the capabilities registers (MMCHS_CAPA and MMCHS_CUR_CAPA). 0x0: Reset completed 0x1: Software reset for all the design	RW	0
23:20	RESERVED		R	0x0
19:16	DTO	Data timeout counter value and busy timeout. This value determines the interval by which DAT lines timeouts are detected. The host driver needs to set this bitfield based on - the maximum read access time (NAC) (Refer to the SD Specification Part1 Physical Layer), - the data read access time values (TAAC and NSAC) in the card specific data register (CSD) of the card, - the timeout clock base frequency (MMCHS_CAPA[TCF]). If the card does not respond within the specified number of cycles, a data timeout error occurs (MMCHS_STA[DTO]). The MMCHS_SYSCTL[DTO] register is also used to check busy duration, to generate busy timeout for commands with busy response or for busy programming during a write command. Timeout on CRC status is generated if no CRC token is present after a block write. 0xF: Reserved 0x0: TCF x 2^13 0x1: TCF x 2^14 0xE: TCF x 2^27	RW	0x0
15:6	CLKD	Clock frequency select These bits define the ratio between MMCi_FCLK and the output clock frequency on the CLK pin of either the memory card (MMC, SD or SDIO). 0x0: MMCi_FCLK bypass 0x1: MMCi_FCLK bypass 0x2: MMCi_FCLK / 2 0x3: MMCi_FCLK / 3 0x3FF: MMCi_FCLK / 1023	RW	0x000
5	CGS	Clock Generator Select - For SD cards Host Controller Version 3.00 supports this bit. This bit is used to select the clock generator mode in MMCHS_SYSCTL[15:6] CLKD. If the Programmable Clock Mode is supported (non-zero value is set to MMCHS_CAPA2[23:16] CM), this bit attribute is RW, and if not supported, this bit attribute is RO and zero is read. This bit depends on the setting of MMCHS_AC12[31] PV_ENABLE. If PV_ENABLE = 0, this bit is set by Host Driver. If PV_ENABLE = 1, this bit is automatically set to a value specified in one of Preset Value registers, see, Table 24-22.	R	0
4:3	RESERVED		R	0x0
2	CEN	Clock enable This bit controls if the clock is provided to the card or not. 0x0: The clock is not provided to the card . Clock frequency can be changed . 0x1: The clock is provided to the card and can be automatically gated when MMCHS_SYSCONFIG[AUTOIDLE] is set to 1 (default value) . The host driver shall wait to set this bit to 1 until the Internal clock is stable (MMCHS_SYSCTL[ICS]).	RW	0

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Bits	Field Name	Description	Type	Reset
1	ICS	Internal clock stable (status) This bit indicates either the internal clock is stable or not. Read 0x1: The internal clock is stable after enabling the clock (MMCHS_SYSCTL[ICE]) or after changing the clock ratio (MMCHS_SYSCTL[CLKD]). Read 0x0: The internal clock is not stable.	R	0
0	ICE	Internal clock enable This register controls the internal clock activity. In very low power state, the internal clock is stopped. Note: The activity of the debounce clock (used for wakeup events) and the interface clock (used for reads and writes to the module register map) are not affected by this register. 0x0: The internal clock is stopped (very low power state). 0x1: The internal clock oscillates and can be automatically gated when MMCHS_SYSCONFIG[AUTOIDLE] is set to 1 (default value) .	RW	0

Table 24-103. Register Call Summary for Register MMCHS_SYSCTL

MMC/SDIO Environment • Protocol: [0]
MMC/SDIO Functional Description • Software Reset: [1] [2] [3] [4] [5] • Power Management: [6] • Retention Mode: [7]
MMC/SDIO Programming Guide • MMC/SDIO Host Controller Initialization Flow: [8] • Basic Operations for MMC/SDIO Host Controller: [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] • Boot Mode Configuration: [24] [25]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [26] [27] • MMC/SDIO Register Description: [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43] [44] [45] [46] [47] [48] [49] [50] [51] [52] [53] [54] [55] [56] [57] [58] [59]

Table 24-104. MMCHS_STAT

Address Offset	0x0000 0230
Physical Address	0x4809 C230 0x480B 4230 0x480B 4230 0x480A D230 0x480D 1230 0x480D 1230 0x480D 5230 0x480D 5230
Description	Interrupt Status Register The interrupt status regroups all the status of the module internal events that can generate an interrupt. MMCHS_STAT[31:16] = Error Interrupt Status MMCHS_STAT[15:0] = Normal Interrupt Status
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		BADA	CERR	RESERVED	TE	ADMAE	ACE	RESERVED	DEB	DCRC	DTO	CIE	CEB	CCRC	CTO	ERRI	RESERVED				BSR	OBI	CIRQ	CREM	CINS	BRR	BWR	DMA	BGE	TC	CC

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Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	BADA	Bad access to data space This bit is set automatically to indicate a bad access to buffer when not allowed: -This bit is set during a read access to the data register (MMCHS_DATA) while buffer reads are not allowed (MMCHS_PSTATE[BRE] =0) -This bit is set during a write access to the data register (MMCHS_DATA) while buffer writes are not allowed (MMCHS_STATE[BWE] =0) Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Bad Access Read 0x0: No Interrupt.	RW	0
28	CERR	Card error This bit is set automatically when there is at least one error in a response of type R1, R1b, R6, R5 or R5b. Only bits referenced as type E(error) in status field in the response can set a card status error. An error bit in the response is flagged only if corresponding bit in card status response error MMCHS_CSRE in set. There is no card error detection for autoCMD12 command. The host driver shall read MMCHS_RSP76 register to detect error bits in the command response. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Card error Read 0x0: No Error	RW	0
27	RESERVED		R	0
26	TE	Tuning Error This bit is set when an unrecoverable error is detected in a tuning circuit except during tuning procedure (Occurrence of an error during tuning procedure is indicated by Sampling Select). By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning. To reset tuning circuit, Sampling Clock shall be set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Tuning Error, the Host Driver should discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from tuning circuit error. The bit is set if the lock is lost (but not during the tuning process) or if the lock counter expires without the lock being asserted. If the latter happens, the SW can decide to ignore the interrupt and wait some more for the lock to be set. 0x0: No Error 0x1: Error	RW	0
25	ADMAE	ADMA Error: This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register.In addition, the Host Controller generates this interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. ADMA Error State in the ADMA Error Status indicates that an error occurs in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: ADMA error Read 0x0: No Interrupt.	RW	0

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Bits	Field Name	Description	Type	Reset
24	ACE	Auto CMD error Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register (MMCHS_AC12) has changed from 0 to 1. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Auto CMD error Read 0x0: No Error.	RW	0
23	RESERVED		R	0
22	DEB	Data End Bit error This bit is set automatically when detecting a 0 at the end bit position of read data on DAT line or at the end position of the CRC status in write mode. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Data end bit error Read 0x0: No Error	RW	0
21	DCRC	Data CRC Error This bit is set automatically when there is a CRC16 error in the data phase response following a block read command or if there is a 3-bit CRC status different of a position "010" token during a block write command. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Data CRC error Read 0x0: No Error.	RW	0
20	DTO	Data timeout error This bit is set automatically according to the following conditions: - busy timeout for R1b, R5b response type - busy timeout after write CRC status - write CRC status timeout - read data timeout Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Time out Read 0x0: No error.	RW	0
19	CIE	Command index error This bit is set automatically when response index differs from corresponding command index previously emitted. It depends on the enable in MMCHS_CMD[CICE] register. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Command index error Read 0x0: No error.	RW	0
18	CEB	Command end bit error This bit is set automatically when detecting a 0 at the end bit position of a command response. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Command end bit error Read 0x0: No error.	RW	0

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Bits	Field Name	Description	Type	Reset
17	CCRC	Command CRC Error This bit is set automatically when there is a CRC7 error in the command response depending on the enable in MMCHS_CMD[CCCE] register. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Command CRC error Read 0x0: No Error.	RW	0
16	CTO	Command Timeout Error This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands that reply within 5 clock cycles - the timeout is still detected at 64 clock cycles. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Time Out Read 0x0: No error	RW	0
15	ERRI	Error Interrupt If any of the bits in the Error Interrupt Status register (MMCHS_STAT[24:15]) are set, then this bit is set to 1. Therefore the host driver can efficiently test for an error by checking this bit first. Writes to this bit are ignored. Read 0x1: Error interrupt event(s) occurred Read 0x0: No Interrupt.	R	0
14:11	RESERVED		R	0x0
10	BSR	Boot status received interrupt This bit is set automatically when MMCHS_CON[BOOT] is set 0x1 or 0x2 and a boot status is received on DAT[0] line. This interrupt is only useful for MMC card. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Boot status received interrupt. Read 0x0: No Interrupt.	RW	0
9	OBI	Out-Of-Band interrupt This bit is set automatically when MMCHS_CON[OBIE] is set and an Out-of-Band interrupt occurs on OBI pin. The interrupt detection depends on polarity controlled by MMCHS_CON[OBIP]. This interrupt is only useful for MMC card. The Out-of-Band interrupt signal is a system specific feature for future use, this signal is not required for existing specification implementation. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Interrupt Out-Of-Band occurs Read 0x0: No Out-Of-Band interrupt.	RW	0

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Bits	Field Name	Description	Type	Reset
8	CIRQ	Card interrupt This bit is only used for SD and SDIO and CE-ATA cards. In 1-bit mode, interrupt source is asynchronous (can be a source of asynchronous wakeup). In 4-bit mode, interrupt source is sampled during the interrupt cycle. In CE-ATA mode, interrupt source is detected when the card drives CMD line to zero during one cycle after data transmission end.All modes above are fully exclusive. The controller interrupt must be clear by setting MMCHS_IE[CIRQ] to 0, then the host driver must start the interrupt service with card (clearing card interrupt status) to remove card interrupt source. Otherwise the Controller interrupt will be reasserted as soon as MMCHS_IE[CIRQ] is set to 1. Writes to this bit are ignored. Read 0x1: Generate card interrupt Read 0x0: No card interrupt	R	0
7	CREM	Card removal This bit is set automatically when MMCHS_PSTATE[CINS] changes from 1 to 0. A clear of this bit doesn't affect Card inserted present state (MMCHS_PSTATE[CINS]). Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Card removed Read 0x0: Card state stable or Debouncing	RW	0
6	CINS	Card insertion This bit is set automatically when MMCHS_PSTATE[CINS] changes from 0 to 1. A clear of this bit doesn't affect Card inserted present state (MMCHS_PSTATE[CINS]). Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Card inserted Read 0x0: Card state stable or debouncing	RW	0
5	BRR	Buffer read ready This bit is set automatically during a read operation to the card (see class 2 - block oriented read commands) when one block specified by MMCHS_BLK[BLEN] is completely written in the buffer. It indicates that the memory card has filled out the buffer and that the local host needs to empty the buffer by reading it. Note: If the DMA receive-mode is enabled, this bit is never set; instead a DMA receive request to the main DMA controller of the system is generated. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Ready to read buffer Read 0x0: Not Ready to read buffer	RW	0

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Bits	Field Name	Description	Type	Reset
4	BWR	Buffer write ready This bit is set automatically during a write operation to the card (see class 4 - block oriented write command) when the host can write a complete block as specified by MMCHS_BLK[BLEN]. It indicates that the memory card has emptied one block from the buffer and that the local host is able to write one block of data into the buffer. Note: If the DMA transmit mode is enabled, this bit is never set; instead, a DMA transmit request to the main DMA controller of the system is generated. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Ready to write buffer Read 0x0: Not Ready to write buffer	RW	0
3	DMA	DMA interrupt : This status is set when an interrupt is required in the ADMA instruction and after the data transfer completion. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: No dma interrupt Read 0x0: Dma interrupt detected	RW	0
2	BGE	Block gap event When a stop at block gap is requested (MMCHS_HCTL[SBGR]), this bit is automatically set when transaction is stopped at the block gap during a read or write operation. This event does not occur when the stop at block gap is requested on the last block. In read mode, a 1-to-0 transition of the DAT Line active status (MMCHS_PSTATE[DLA]) between data blocks generates a Block gap event interrupt. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Transaction stopped at block gap Read 0x0: No block gap event	RW	0
1	TC	Transfer completed This bit is always set when a read/write transfer is completed or between two blocks when the transfer is stopped due to a stop at block gap request (MMCHS_HCTL[SBGR]). In Read mode: This bit is automatically set on completion of a read transfer (MMCHS_PSTATE[RTA]). In write mode: This bit is set automatically on completion of the DAT line use (MMCHS_PSTATE[DLA]). Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Data transfer complete Read 0x0: No transfer complete	RW	0

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Bits	Field Name	Description	Type	Reset
0	CC	Command complete This bit is set when a 1-to-0 transition occurs in the register command inhibit (MMCHS_PSTATE[CMDI]) If the command is a type for which no response is expected, then the command complete interrupt is generated at the end of the command. A command timeout error (MMCHS_STAT[CTO]) has higher priority than command complete (MMCHS_STAT[CC]). If a response is expected but none is received, then a command timeout error is detected and signaled instead of the command complete interrupt. Write 0x0: Status bit unchanged Write 0x1: Status is cleared Read 0x1: Command complete Read 0x0: No Command complete	RW	0

Table 24-105. Register Call Summary for Register MMCHS_STAT

MMC/SDIO Functional Description

- Power Management: [0] [1] [2] [3] [4] [5] [6]
- Interrupt Requests: [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39]
- Interrupt-Driven Operation: [40] [41] [42] [43] [44] [45]
- Polling: [46] [47]
- Requirements for Descriptors: [48]
- Data Buffer: [49] [50] [51]
- Data Buffer Status: [52] [53] [54]
- Transfer or Command Status and Errors Reporting: [55] [56]
- Busy Time-Out for R1b, R5b Response Type: [57]
- Busy Time-Out After Write CRC Status: [58]
- Write CRC Status Time-Out: [59]
- Read Data Time-Out: [60] [61]
- Boot Acknowledge Time-Out: [62] [63] [64] [65] [66] [67]
- MMC CE-ATA Command Completion Disable Management: [68]
- Test Registers: [69] [70]

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- Basic Operations for MMC/SDIO Host Controller: [71] [72] [73] [74] [75] [76] [77] [78]
- Bus Voltage Selection: [79]
- Boot Mode Configuration: [80] [81]

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- MMC/SDIO Register Summary: [82] [83]
- MMC/SDIO Register Description: [84] [85] [86] [87] [88] [89] [90] [91] [92] [93] [94] [95] [96] [97] [98] [99] [100] [101] [102] [103] [104] [105] [106] [107] [108] [109] [110] [111] [112]

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Table 24-106. MMCHS_IE

Address Offset	0x0000 0234
Physical Address	0x4809 C234 0x480B 4234 0x480B 4234 0x480A D234 0x480D 1234 0x480D 1234 0x480D 5234 0x480D 5234
Description	Interrupt Status Enable Register This register allows to enable/disable the module to set status bits, on an event-by-event basis. MMCHS_IE[31:16] = Error Interrupt Status Enable MMCHS_IE[15:0] = Normal Interrupt Status Enable
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		BADA_ENABLE	CERR_ENABLE	RESERVED	TE_ENABLE	ADMAE_ENABLE	ACE_ENABLE	RESERVED	DEB_ENABLE	DCRC_ENABLE	DTO_ENABLE	CIE_ENABLE	CEB_ENABLE	CCRC_ENABLE	CTO_ENABLE	NULL	RESERVED				BSR_ENABLE	OBI_ENABLE	CIRQ_ENABLE	CREM_ENABLE	CINS_ENABLE	BRR_ENABLE	BWR_ENABLE	DMA_ENABLE	BGE_ENABLE	TC_ENABLE	CC_ENABLE	

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	BADA_ENABLE	Bad access to data space Status Enable 0x0: Masked 0x1: Enabled	RW	0
28	CERR_ENABLE	Card Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
27	RESERVED		R	0
26	TE_ENABLE	Tuning Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
25	ADMAE_ENABLE	ADMA Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
24	ACE_ENABLE	Auto CMD Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
23	RESERVED		R	0
22	DEB_ENABLE	Data End Bit Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
21	DCRC_ENABLE	Data CRC Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
20	DTO_ENABLE	Data Timeout Error Status Enable 0x0: The data timeout detection is deactivated. The host controller provides the clock to the card until the card sends the data or the transfer is aborted. 0x1: The data timeout detection is enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
19	CIE_ENABLE	Command Index Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
18	CEB_ENABLE	Command End Bit Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
17	CCRC_ENABLE	Command CRC Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
16	CTO_ENABLE	Command Timeout Error Status Enable 0x0: Masked 0x1: Enabled	RW	0
15	NULL	Fixed to 0 The host driver shall control error interrupts using the Error Interrupt Signal Enable register. Writes to this bit are ignored	R	0
14:11	RESERVED		R	0x0
10	BSR_ENABLE	Boot Status Enable A write to this register when MMCHS_CON[BOOT_ACK] is set to 0x0 is ignored. 0x0: Masked 0x1: Enabled	RW	0
9	OBI_ENABLE	Out-of-Band Status Enable A write to this register when MMCHS_CON[OBIE] is set to '0' is ignored. 0x0: Masked 0x1: Enabled	RW	0
8	CIRQ_ENABLE	Card Status Enable A clear of this bit also clears the corresponding status bit. During 1-bit mode, if the interrupt routine doesn't remove the source of a card interrupt in the SDIO card, the status bit is reasserted when this bit is set to 1. 0x0: Masked 0x1: Enabled	RW	0
7	CREM_ENABLE	Card Removal Status Enable 0x0: Masked 0x1: Enabled	RW	0
6	CINS_ENABLE	Card Insertion Status Enable 0x0: Masked 0x1: Enabled	RW	0
5	BRR_ENABLE	Buffer Read Ready Status Enable 0x0: Masked 0x1: Enabled	RW	0
4	BWR_ENABLE	Buffer Write Ready Status Enable 0x0: Masked 0x1: Enabled	RW	0
3	DMA_ENABLE	DMA Status Enable 0x0: Masked 0x1: Enabled	RW	0
2	BGE_ENABLE	Block Gap Event Status Enable 0x0: Masked 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
1	TC_ENABLE	Transfer Complete Status Enable 0x0: Masked 0x1: Enabled	RW	0
0	CC_ENABLE	Command Complete Status Enable 0x0: Masked 0x1: Enabled	RW	0

Table 24-107. Register Call Summary for Register MMCHS_IE

MMC/SDIO Functional Description • Power Management: [0] [1] [2] [3] [4] [5] • Interrupt Requests: [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28] [29] [30] [31] • Interrupt-Driven Operation: [32] [33]
MMC/SDIO Programming Guide • MMC/SDIO Host Controller Initialization Flow: [34] • Basic Operations for MMC/SDIO Host Controller: [35] [36] [37]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [38] [39] • MMC/SDIO Register Description: [40] [41] [42] [43]

Table 24-108. MMCHS_ISE

Address Offset	0x0000 0238
Physical Address	0x4809 C238 0x480B 4238 0x480B 4238 0x480A D238 0x480D 1238 0x480D 1238 0x480D 5238 0x480D 5238
Description	Interrupt Signal Enable Register This register allows to enable/disable the module internal sources of status, on an event-by-event basis. MMCHS_ISE[31:16] = Error Interrupt Signal Enable MMCHS_ISE[15:0] = Normal Interrupt Signal Enable
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		BADA_SIGEN	CERR_SIGEN	RESERVED	TE_SIGEN	ADMAE_SIGEN	ACE_SIGEN	RESERVED	DEB_SIGEN	DCRC_SIGEN	DTO_SIGEN	CIE_SIGEN	CEB_SIGEN	CCRC_SIGEN	CTO_SIGEN	NULL	RESERVED				BSR_SIGEN	OBI_SIGEN	CIRQ_SIGEN	CREM_SIGEN	CINS_SIGEN	BRR_SIGEN	BWR_SIGEN	DMA_SIGEN	BGE_SIGEN	TC_SIGEN	CC_SIGEN	

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	BADA_SIGEN	Bad access to data space Signal Enable 0x0: Masked 0x1: Enabled	RW	0
28	CERR_SIGEN	Card Error Interrupt Signal Enable 0x0: Masked 0x1: Enabled	RW	0
27	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
26	TE_SIGEN	Tuning Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
25	ADMAE_SIGEN	ADMA Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
24	ACE_SIGEN	Auto CMD Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
23	RESERVED		R	0
22	DEB_SIGEN	Data End Bit Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
21	DCRC_SIGEN	Data CRC Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
20	DTO_SIGEN	Data Timeout Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
19	CIE_SIGEN	Command Index Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
18	CEB_SIGEN	Command End Bit Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
17	CCRC_SIGEN	Command CRC Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
16	CTO_SIGEN	Command timeout Error Signal Enable 0x0: Masked 0x1: Enabled	RW	0
15	NULL	Fixed to 0 The host driver shall control error interrupts using the Error Interrupt Signal Enable register. Writes to this bit are ignored	R	0
14:11	RESERVED		R	0x0
10	BSR_SIGEN	Boot Status Signal Enable A write to this register when MMCHS_CON[BOOT_ACK] is set to 0x0 is ignored. 0x0: Masked 0x1: Enabled	RW	0
9	OBI_SIGEN	Out-Of-Band Interrupt Signal Enable A write to this register when MMCHS_CON[OBIE] is set to '0' is ignored. 0x0: Masked 0x1: Enabled	RW	0
8	CIRQ_SIGEN	Card Interrupt Signal Enable 0x0: Masked 0x1: Enabled	RW	0

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Bits	Field Name	Description	Type	Reset
7	CREM_SIGEN	Card Removal Signal Enable 0x0: Masked 0x1: Enabled	RW	0
6	CINS_SIGEN	Card Insertion Signal Enable 0x0: Masked 0x1: Enabled	RW	0
5	BRR_SIGEN	Buffer Read Ready Signal Enable 0x0: Masked 0x1: Enabled	RW	0
4	BWR_SIGEN	Buffer Write Ready Signal Enable 0x0: Masked 0x1: Enabled	RW	0
3	DMA_SIGEN	DMA Interrupt Signal Enable 0x0: Masked 0x1: Enabled	RW	0
2	BGE_SIGEN	Black Gap Event Signal Enable 0x0: Masked 0x1: Enabled	RW	0
1	TC_SIGEN	Transfer Completed Status Enable 0x0: Masked 0x1: Enabled	RW	0
0	CC_SIGEN	Command Complete Status Enable 0x0: Masked 0x1: Enabled	RW	0

Table 24-109. Register Call Summary for Register MMCHS_ISE

MMC/SDIO Functional Description • Power Management: [0] [1] • Interrupt Requests: [2] [3] [4] [5] [6] • Polling: [7]
MMC/SDIO Programming Guide • Basic Operations for MMC/SDIO Host Controller: [8]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [9] [10] • MMC/SDIO Register Description: [11] [12] [13]

Table 24-110. MMCHS_AC12

Address Offset	0x0000 023C
Physical Address	0x4809 C23C 0x480B 423C 0x480B 423C 0x480A D23C 0x480D 123C 0x480D 123C 0x480D 523C 0x480D 523C
Description	Host Control 2 Register and Auto CMD Error Status Register This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD23. The Host driver can determine what kind of Auto CMD12 / CMD23 errors occur by this register. Auto CMD23 errors are indicated only in bits[4:1]. Bits[7:0] are valid only when the MMCHS_CMD[3:2] ACEN bitfield is configured to enable Auto CMD and the Auto CMD Error bit (MMCHS_STAT[24]ACE) is set.
Type	RW

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PV_ENABLE	AI_ENABLE	RESERVED						SCLK_SEL	ET	DS_SEL		V1V8_SIGEN	UHSMS			RESERVED								CNI	RESERVED		ACIE	ACEB	ACCE	ACTO	ACNE

Bits	Field Name	Description	Type	Reset
31	PV_ENABLE	Preset Value Enable Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set, automatic SDCLK frequency generation and driver strength selection is performed without considering system specific conditions. This bit enables the functions defined in the Preset Value registers, see, Table 24-22. If this bit is set to 0, MMCHS_SYSCTL[15:6] CLKD, MMCHS_SYSCTL[5] CGS and MMCHS_AC12[21:20] DS_SEL are set by Host Driver. If this bit is set to 1, MMCHS_SYSCTL[15:6] CLKD, MMCHS_SYSCTL[5] CGS and MMCHS_AC12[21:20] DS_SEL are set by Host Controller as specified in the Preset Value registers, see, Table 24-22. 0x0: SDCLK and Driver Strength (DS_SEL) are controlled by Host Driver. 0x1: Automatic Selection by Preset Value are Enabled.	RW	0
30	AI_ENABLE	Asynchronous Interrupt Enable This bit can be set to 1 if a card supports asynchronous interrupts and MMCHS_CAPA[29] AIS is set to 1. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver the Card Interrupt to the host when it is asserted by the Card. 0x0: Disabled 0x1: Enabled	RW	0
29:24	RESERVED		R	0x00
23	SCLK_SEL	Sampling Clock Select Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is set by tuning procedure and valid after the completion of tuning (when MMCHS_AC12[22] ET is cleared). Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Writing 1 to this bit is meaningless and ignored. A tuning circuit is reset by writing to 0. This bit can be cleared with setting MMCHS_AC12[22] ET. Once the tuning circuit is reset, it will take time to complete tuning sequence. Therefore, Host Driver should keep this bit to 1 to perform re-tuning sequence to compete re-tuning sequence in a short time. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. 0x0: Fixed clock is used to sample data 0x1: Tuned clock is used to sample data	RW	0

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Bits	Field Name	Description	Type	Reset
22	ET	Execute Tuning This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to MMCHS_AC12[23] SCLK_SEL. Tuning procedure is aborted by writing 0. This is Read-Write with automatic clear register 0x0: Not Tuned or Tuning Completed 0x1: Execute Tuning	RW	0
21:20	DS_SEL	Driver Strength Select Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depending on Driver Type A, C and D support bits (DTA, DTC and DTD respectively) in the MMCHS_CAPA2 register. This bit depends on setting of Preset Value Enable. If Preset Value Enable = 0, this field is set by Host Driver. If Preset Value Enable = 1, this field is automatically set by a value specified in the one of Preset Value registers, see, Table 24-22. 0x0: Driver Type B is selected (Default) 0x1: Driver Type A is selected 0x3: Driver Type D is selected 0x2: Driver Type C is selected	RW	0x0
19	V1V8_SIGEN	1.8V Signaling Enable This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5ms. Host Controller clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5ms. Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling (One of support bits is set to 1: SDR50, SDR104 or DDR50 in MMCHS_CAPA2 register) and the card or device supports UHS-I (S18A=1. Refer to Bus Signal Voltage Switch Sequence in the Physical Layer Specification Version 3.0x) see also Section 24.5.1.2.2 *Bus Voltage Selection* in Chapter 24 *MMC/SDIO*. 0x0: 3.3V Signaling 0x1: 1.8V Signaling	RW	0

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Bits	Field Name	Description	Type	Reset
18:16	UHSMS	UHS Mode Select This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1. If MMCHS_AC12[31] PV_ENABLE is set to 1, Host Controller sets MMCHS_SYSCTL[15:6] CLKD, MMCHS_SYSCTL[5] CGS and MMCHS_AC12[21:20] DS_SEL according to Preset Value registers, see, Table 24-22. In this case, one of preset value registers is selected by this field. Host Driver needs to reset MMCHS_SYSCTL[2] CEN before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets MMCHS_SYSCTL[2] CEN again. When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more detail. 0x6: Reserved 0x1: SDR25 0x7: Reserved 0x0: SDR12 0x2: SDR50 0x4: DDR50 0x5: Reserved 0x3: SDR104	RW	0x0
15:8	RESERVED		R	0x00
7	CNI	Command Not Issued By Auto CMD12 Error Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Read 0x1: Command not issued Read 0x0: No error	R	0
6:5	RESERVED		R	0x0
4	ACIE	Auto CMD Index Error - For Auto CMD12 and Auto CMD23 This bit is set if the Command Index error occurs in response to a command. Read 0x1: Error Read 0x0: No error	R	0
3	ACEB	Auto CMD End Bit Error - For Auto CMD12 and Auto CMD23 This bit is set when detecting that the end bit of command response is 0. Read 0x1: End bit Error Generated Read 0x0: No error	R	0
2	ACCE	Auto CMD CRC Error - For Auto CMD12 and Auto CMD23 This bit is set when detecting a CRC error in the command response. Read 0x1: CRC Error Generated Read 0x0: No error	R	0
1	ACTO	Auto CMD Timeout Error - For Auto CMD12 and Auto CMD23 This bit is set if no response is returned within 64 SDCLK cycles from the end bit of command. If this bit is set to1, the other error status bits (D04-D02) are meaningless. Read 0x1: Auto CMD Time Out Read 0x0: No error	R	0

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Bits	Field Name	Description	Type	Reset
0	ACNE	Auto CMD12 Not Executed If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the Host Controller cannot issue Auto CMD12 to stop memory multiple block data transfer due to some error. If this bit is set to 1, other error status bits (D04-D01) are meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Read 0x1: Auto CMD12 Not Executed Read 0x0: Auto CMD12 Executed	R	0

Table 24-111. Register Call Summary for Register MMCHS_AC12

MMC/SDIO Functional Description
- Interrupt Requests: [0]
- Asynchronous Interrupt: [1] [2]
- Different Types of Responses: [3]
- Sampling Clock Tuning: [4] [5] [6] [7] [8]

MMC/SDIO Programming Guide
- Basic Operations for MMC/SDIO Host Controller: [9] [10]
- Bus Voltage Selection: [11]

MMC/SDIO Register Manual
- MMC/SDIO Register Summary: [12] [13]
- MMC/SDIO Register Description: [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] [28]

Table 24-112. MMCHS_CAPA

Address Offset	0x0000 0240
Physical Address	0x4809 C240 0x480B 4240 0x480B 4240 0x480A D240 0x480D 1240 0x480D 1240 0x480D 5240 0x480D 5240
Description	Capabilities Register This register lists the capabilities of the MMC/SD/SDIO host controller.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		AIS	BIT64	RESERVED	VS18	VS30	VS33	SRS	DS	HSS	RESERVED	AD2S	RESERVED	MBL		BCF								TCU	RESERVED				TCF		

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		R	0x0
29	AIS	Asynchronous Interrupt Support Refer to SDIO Specification Version 3.00 about asynchronous interrupt. Read 0x1: Asynchronous Interrupt Supported Read 0x0: Asynchronous Interrupt Not Supported	R	1

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Bits	Field Name	Description	Type	Reset
28	BIT64	64 Bit System Bus Support Setting 1 to this bit indicates that the Host Controller supports 64-bit address descriptor mode and is connected to 64-bit address system bus. Read 0x1: 64 bit System bus address Read 0x0: 32 bit System bus address	R	0
27	RESERVED		R	0
26	VS18	Voltage support 1.8V Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset (via RESETN signal) Write 0x0: 1.8V Not supported Write 0x1: 1.8V Supported Read 0x1: 1.8V Supported Read 0x0: 1.8V Not Supported	RW	0
25	VS30	Voltage support 3.0V Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset (via RESETN signal) Write 0x0: 3.0V Not supported Write 0x1: 3.0V Supported Read 0x1: 3.0V Supported Read 0x0: 3.0V Not Supported	RW	0
24	VS33	Voltage support 3.3V Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset (via RESETN signal) Write 0x0: 3.3V Not supported Write 0x1: 3.3V Supported Read 0x1: 3.3V Supported Read 0x0: 3.3V Not Supported	RW	0
23	SRS	Suspend/Resume support (SDIO cards only) This bit indicates whether the host controller supports Suspend/Resume functionality. Read 0x1: The Host controller supports Suspend/Resume functionality. Read 0x0: The Host controller does not Suspend/Resume functionality.	R	1
22	DS	DMA support This bit indicates that the Host Controller is able to use DMA to transfer data between system memory and the Host Controller directly. Read 0x1: DMA Supported Read 0x0: DMA Not Supported	R	1
21	HSS	High speed support This bit indicates that the host controller supports high speed operations and can supply an up-to maximum card frequency. Read 0x1: High Speed Supported Read 0x0: High Speed Not Supported	R	1
20	RESERVED		R	0

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Bits	Field Name	Description	Type	Reset
19	AD2S	ADMA2 Support This bit indicates whether the Host Controller is capable of using ADMA2. It depends on setting of generic parameter MADMA_EN Read 0x1: ADMA2 Supported Read 0x0: ADMA2 not Supported	R	0
18	RESERVED		R	0
17:16	MBL	Maximum block length This value indicates the maximum block size that the host driver can read and write to the buffer in the host controller. This value depends on definition of generic parameter with a max value of 2048 bytes. The host controller supports 512 bytes and 1024 bytes block transfers. Read 0x2: 2048 bytes Read 0x1: 1024 bytes Read 0x0: 512 bytes	R	0x1
15:8	BCF	Base Clock Frequency For SD Clock This value indicates the base (maximum) clock frequency for the SD Clock. 8-bit Base Clock Frequency This mode is supported by the Host Controller Version 3.00. Unit values are 1MHz. The supported clock range is 10MHz to 255MHz. FFh : 255MHz .... : ..... 02h : 2MHz 01h : 1MHz 00h : Get information via another method If the real frequency is 16.5MHz, the lager value shall be set 0001 0001b (17MHz) because the Host Driver use this value to calculate the clock divider value (Refer to MMCHS_SYSCTL[15:6] CLKD) and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host System has to get information via another method. Read 0x0: The value indicating the base (maximum) frequency for the output clock provided to the card is system dependent and is not available in this register. Get the information via another method.	R	0x00
7	TCU	Timeout clock unit This bit shows the unit of base clock frequency used to detect Data Timeout Error (MMCHS_STAT[DTO]). Read 0x1: MHz Read 0x0: KHz	R	1
6	RESERVED		R	0
5:0	TCF	Timeout clock frequency The timeout clock frequency is used to detect Data Timeout Error (MMCHS_STAT[DTO]). Read 0x0: The timeout clock frequency depends on the frequency of the clock provided to the card. The value of the timeout clock frequency is not available in this register.	R	0x00

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Table 24-113. Register Call Summary for Register MMCHS_CAPA

MMC/SDIO Functional Description • Software Reset: [0] • Asynchronous Interrupt: [1] • Data Buffer: [2]
MMC/SDIO Programming Guide • MMC/SDIO Host Controller Initialization Flow: [3]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [4] [5] • MMC/SDIO Register Description: [6] [7] [8] [9] [10] [11] [12] [13]

Table 24-114. MMCHS_CAPA2

Address Offset	0x0000 0244
Physical Address	0x4809 C244 0x480B 4244 0x480B 4244 0x480A D244 0x480D 1244 0x480D 1244 0x480D 5244 0x480D 5244
Description	Capabilities 2 Register This register provides the Host Driver with information specific to the Host Controller implementation. The Host Controller may implement these values as fixed or loaded from flash memory during power on initialization. Refer to Software Reset For All in the Software Reset register for loading from flash memory and completion timing control.
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CM								RTM		TSDR50	RESERVED	TCRT				RESERVED	DTD	DTC	DTA	RESERVED	DDR50	SDR104	SDR50

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	CM	Clock Multiplier This field indicates clock multiplier value of programmable clock generator. Refer to MMCHS_SYSCTL [15:0]. Setting 00h means that Host Controller does not support programmable clock generator. 00h : Clock Multiplier is Not Supported 01h : Clock Multiplier M = 2 02h : Clock Multiplier M = 3 .... : ..... FFh : Clock Multiplier M = 256	R	0x00

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Bits	Field Name	Description	Type	Reset
15:14	RTM	Re-Tuning Modes This field selects re-tuning method and limits the maximum data length. Bit47-46 Re-Tuning Mode Re-Tuning Method Data Length There are two re-tuning timings: Re-Tuning Request controlled by the Host Controller and expiration of a Re-Tuning Timer controlled by the Host Driver. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue. The maximum data length per read/write command is restricted so that re-tuning procedures can be inserted during data transfers. (1) Re-Tuning Mode 1 The host controller does not have any internal logic to detect when the re-tuning needs to be performed. In this case, the Host Driver should maintain all re-tuning timings by using a Re-Tuning Timer. To enable inserting the re-tuning procedure during data transfers, the data length per read/write command shall be limited up to 4 MiB. (2) Re-Tuning Mode 2 The host controller has the capability to indicate the re-tuning timing by Re-Tuning Request during data transfers. Then the data length per read/write command shall be limited up to 4 MiB. During non data transfer, re-tuning timing is determined by either Re-Tuning Request or Re-Tuning Timer. If Re-Tuning Request is used, Re-Tuning Timer should be disabled. (3) Re-Tuning Mode 3 The host controller has the capability to take care of the re-tuning during data transfer (Auto Re-Tuning). Re-Tuning Request shall not be generated during data transfers and there is no limitation to data length per read/write command. During non data transfer, re-tuning timing is determined by either Re-Tuning Request or Re-Tuning Timer. If Re-Tuning Request is used, Re-Tuning Timer should be disabled. Re-Tuning Timer Control Example for Re-Tuning Mode 1 The initial value of re-tuning timer is provided by Timer Count for Re-Tuning field in this register. The timer starts counting by loading the initial value. When the timer expires, the Host Driver marks an expiration flag. On receiving a command request, the Host driver checks the expiration flag. If the expiration flag is set, then the Host Driver should perform the re-tuning procedure before issuing a command. If the expiration flag is not set, then the Host Driver issues a command without performing the re-tuning procedure. Every time the re-tuning procedure is performed, the timer loads the new initial value and the expiration flag is cleared. Re-Tuning Timer Control Example for Re-Tuning Mode 2 and Mode 3 The timer control is almost the same as Re-Tuning Mode 1 except the timer loads the new initial value after data transfer (when receiving Transfer Complete). In case of Mode 3, Timer Count for Re-Tuning is set either smaller value: Tuning effective time after re-tuning procedure or after data transfer. If a Host System goes into power down mode, the Host Driver should stop the re-tuning timer and set the expiration flag to 1 when the Host System resumes from power down mode. Read 0x3: Reserved Read 0x2: Auto Re-Tuning (for transfer) - Timer and Re-Tuning Request Read 0x1: Timer and Re-Tuning Request - Max data length 4 MiB Read 0x0: Timer - Max data length 4 MiB	R	0x0

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Bits	Field Name	Description	Type	Reset
13	TSDR50	Use Tuning for SDR50 If this bit is set to 1, this Host Controller requires tuning to operate SDR50. (Tuning is always required to operate SDR104.) Read 0x1: SDR50 requires tuning. Read 0x0: SDR50 does not require tuning.	R	0
12	RESERVED		R	0
11:8	TCRT	Timer Count for Re-Tuning This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 0 disables Re-Tuning Timer. Read 0x3: 4 seconds Read 0xE: Reserved Read 0xC: Reserved Read 0x4: 8 seconds Read 0xB: 1024 seconds Read 0xF: Get information from other source Read 0x2: 2 seconds Read 0x0: Re-Tuning Timer disabled Read 0xA: 512 seconds Read 0x6: 32 seconds Read 0x1: 1 second Read 0x8: 128 seconds Read 0x7: 64 seconds Read 0x9: 256 seconds Read 0xD: Reserved Read 0x5: 16 seconds	R	0xF
7	RESERVED		R	0
6	DTD	Driver Type D Support This bit indicates support of Driver Type D for 1.8 Signaling. Read 0x1: Driver Type D is Supported Read 0x0: Driver Type D is Not Supported.	R	1
5	DTC	Driver Type C Support This bit indicates support of Driver Type C for 1.8 Signaling. Read 0x1: Driver Type C is Supported. Read 0x0: Driver Type C is Not Supported.	R	1
4	DTA	Driver Type A Support This bit indicates support of Driver Type A for 1.8 Signaling. Read 0x1: Driver Type A is Supported. Read 0x0: Driver Type A is Not Supported.	R	1
3	RESERVED		R	0
2	DDR50	DDR50 Support Read 0x1: DDR50 is Supported. Read 0x0: DDR50 is Not Supported.	R	1
1	SDR104	SDR104 Support SDR104 requires tuning. Read 0x1: SDR104 is Supported. Read 0x0: SDR104 is Not Supported.	R	1

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Bits	Field Name	Description	Type	Reset
0	SDR50	SDR50 Support If SDR104 is supported, this bit shall be set to 1. Bit 13 indicates whether SDR50 requires tuning or not. Read 0x1: SDR50 is Supported. Read 0x0: SDR50 is Not Supported.	R	1

Table 24-115. Register Call Summary for Register MMCHS_CAPA2

MMC/SDIO Functional Description
- Sampling Clock Tuning: [0] [1]

MMC/SDIO Register Manual
- MMC/SDIO Register Summary: [2] [3]
- MMC/SDIO Register Description: [4] [5] [6] [7]

Table 24-116. MMCHS_CUR_CAPA

Address Offset	0x0000 0248
Physical Address	0x4809 C248 0x480B 4248 0x480B 4248 0x480A D248 0x480D 1248 0x480D 1248 0x480D 5248 0x480D 5248
Description	Maximum Current Capabilities Register This register indicates the maximum current capability for each voltage. The value is meaningful if the voltage support is set in the capabilities register (MMCHS_CAPA). Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset (via RESETN signal)
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CUR_1V8								CUR_3V0								CUR_3V3							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:16	CUR_1V8	Maximum current for 1.8V Read 0x0: The maximum current capability for this voltage is not available. Feature not implemented.	RW	0x00
15:8	CUR_3V0	Maximum current for 3.0V Read 0x0: The maximum current capability for this voltage is not available. Feature not implemented.	RW	0x00
7:0	CUR_3V3	Maximum current for 3.3V Read 0x0: The maximum current capability for this voltage is not available. Feature not implemented.	RW	0x00

Table 24-117. Register Call Summary for Register MMCHS_CUR_CAPA

MMC/SDIO Functional Description
- Software Reset: [0]

MMC/SDIO Programming Guide
- MMC/SDIO Host Controller Initialization Flow: [1]

MMC/SDIO Register Manual
- MMC/SDIO Register Summary: [2] [3]
- MMC/SDIO Register Description: [4]

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Table 24-118. MMCHS_FE

Address Offset	0x0000 0250
Physical Address	0x4809 C250 0x480B 4250 0x480B 4250 0x480A D250 0x480D 1250 0x480D 1250 0x480D 5250 0x480D 5250
Description	Force Event Register for Auto CMD Error Status and Error Interrupt status The Force Event Register is not a physically implemented register. Rather, it is an address at which the Auto CMD Error Status Register (MMCHS_AC12) can be written. Writing 1 : set each bit of the Auto CMD Error Status Register Writing 0 : no effect Rather, it is an address at which the Error Interrupt Status register can be written. The effect of a write to this address will be reflected in the Error Interrupt Status Register if the corresponding bit of the Error Interrupt Status Enable Register is set. Writing 1 : set each bit of the Error Interrupt Status Register Writing 0 : no effect Note: By setting this register, the Error Interrupt can be set in the Error Interrupt Status register. In order to generate interrupt signal, both the Error Interrupt Status Enable and Error Interrupt Signal Enable shall be set.
Type	W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		FE_BADA	FE_CERR	RESERVED		FE_ADMAE	FE_ACE	RESERVED	FE_DEB	FE_DCRC	FE_DTO	FE_CIE	FE_CEB	FE_CCRC	FE_CTO	RESERVED								FE_CNI	RESERVED		FE_ACIE	FE_ACEB	FE_ACCE	FE_ACTO	FE_ACNE

Bits	Field Name	Description	Type	Reset
31:30	RESERVED		NA	0x0
29	FE_BADA	Force Event Bad access to data space. Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
28	FE_CERR	Force Event Card error. Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
27:26	RESERVED		NA	0x0
25	FE_ADMAE	Force Event ADMA Error. Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
24	FE_ACE	Force Event for Auto CMD Error - For Auto CMD12 and Auto CMD23 Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
23	RESERVED		NA	0
22	FE_DEB	Force Event Data End Bit error. Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
21	FE_DCRC	Force Event Data CRC Error. Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0

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Bits	Field Name	Description	Type	Reset
20	FE_DTO	Force Event Data Timeout Error. Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
19	FE_CIE	Force Event Command Index Error. Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
18	FE_CEB	Force Event Command End Bit Error. Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
17	FE_CCRC	Force Event Command CRC Error. Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
16	FE_CTO	Command Timeout Error This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands that reply within 5 clock cycles - the timeout is still detected at 64 clock cycles. Write 0x0: Status bit unchanged Write 0x1: Status is cleared	W	0
15:8	RESERVED		NA	0x00
7	FE_CNI	Force Event Command not issue by Auto CMD12 error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
6:5	RESERVED		NA	0x0
4	FE_ACIE	Force Event for Auto CMD Index Error - For Auto CMD12 and Auto CMD23 Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
3	FE_ACEB	Force Event Auto CMD End Bit Error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
2	FE_ACCE	Force Event Auto CMD CRC Error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
1	FE_ACTO	Force Event Auto CMD Timeout Error Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0
0	FE_ACNE	Force Event Auto CMD12 Not Executed Write 0x0: No effect, No Interrupt. Write 0x1: Interrupt Forced	W	0

Table 24-119. Register Call Summary for Register MMCHS_FE

MMC/SDIO Functional Description
- Test Registers: [0]

MMC/SDIO Register Manual
- MMC/SDIO Register Summary: [1] [2]

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Table 24-120. MMCHS_ADMAES

Address Offset	0x0000 0254
Physical Address	0x4809 C254 0x480B 4254 0x480B 4254 0x480A D254 0x480D 1254 0x480D 1254 0x480D 5254 0x480D 5254
Description	ADMA Error Status Register When ADMA Error Interrupt is occurred, the ADMA Error States field in this register holds the ADMA state and the ADMA System Address Register holds the address around the error descriptor. For recovering the error, the Host Driver requires the ADMA state to identify the error descriptor address as follows: ST_STOP: Previous location set in the ADMA System Address register is the error descriptor address ST_FDS: Current location set in the ADMA System Address register is the error descriptor address ST_CADR: This sate is never set because do not generate ADMA error in this state. ST_TFR: Previous location set in the ADMA System Address register is the error descriptor address In case of write operation, the Host Driver should use ACMD22 to get the number of written block rather than using this information, since unwritten data may exist in the Host Controller. The Host Controller generates the ADMA Error Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. In this case, ADMA Error State indicates that an error occurs at ST_FDS state. The Host Driver may find that the Valid bit is not set in the error descriptor.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													LME	AES	

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	LME	ADMA Length Mismatch Error: (1) While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. (2) Total data length can not be divided by the block length. 0x0: No Error 0x1: Error	RW	0
1:0	AES	ADMA Error State his field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. 0x0: ST_STOP (Stop DMA)Contents of SYS_SDR register 0x1: ST_STOP (Stop DMA)Points the error descriptor 0x3: ST_TFR (Transfer Data)Points the next of the error descriptor 0x2: Never set this state(Not used)	RW	0x0

Table 24-121. Register Call Summary for Register MMCHS_ADMAES

MMC/SDIO Functional Description
- Requirements for Descriptors: [0]

MMC/SDIO Register Manual
- MMC/SDIO Register Summary: [1] [2]

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Table 24-122. MMCHS_ADMASAL

Address Offset	0x0000 0258
Physical Address	0x4809 C258 0x480B 4258 0x480B 4258 0x480A D258 0x480D 1258 0x480D 1258 0x480D 5258 0x480D 5258
Description	ADMA System address Low bits
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADMA_A32B																															

Bits	Field Name	Description	Type	Reset
31:0	ADMA_A32B	ADMA System address 32 bits.This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register. At the start of ADMA, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The Host Driver shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b.	RW	0x0000 0000

Table 24-123. Register Call Summary for Register MMCHS_ADMASAL

MMC/SDIO Functional Description

- Master DMA Operations: [0] [1]
- Requirements for Descriptors: [2]
- Advanced DMA Description: [3] [4] [5]

MMC/SDIO Register Manual

- MMC/SDIO Register Summary: [6] [7]

Table 24-124. MMCHS_PVINITSD

Address Offset	0x0000 0260
Physical Address	0x4809 C260 0x480B 4260 0x480B 4260 0x480A D260 0x480D 1260 0x480D 1260 0x480D 5260 0x480D 5260
Description	Preset Value for Initialization and Default Speed modes
Type	R

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSDS_SEL		RESERVED			DSCLKGEN_SEL	DSSDCLK_SEL										INITDS_SEL		RESERVED			INITCLKGEN_SEL	INITSDCLK_SEL										

Bits	Field Name	Description	Type	Reset
31:30	DSDS_SEL	Driver Strength Select Value - Default Speed mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Read 0x3: Driver Type D is Selected. Read 0x2: Driver Type C is Selected. Read 0x1: Driver Type A is Selected. Read 0x0: Driver Type B is Selected.	R	0x0
29:27	RESERVED		R	0x0
26	DSCLKGEN_SEL	Clock Generator Select Value - Default Speed mode This bit is effective when Host Controller supports programmable clock generator. Read 0x1: Programmable Clock Generator. Read 0x0: Host Controller Ver2.00 Compatible Clock Generator.	R	0
25:16	DSSDCLK_SEL	SDCLK Frequency Select Value - Default Speed mode 10-bit preset value to set MMCHS_SYSCTL[15:6] CLKD is described by a host system.	R	0x004
15:14	INITDS_SEL	Driver Strength Select Value - Initialization mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Read 0x3: Driver Type D is Selected Read 0x2: Driver Type C is Selected Read 0x1: Driver Type A is Selected Read 0x0: Driver Type B is Selected	R	0x0
13:11	RESERVED		R	0x0
10	INITCLKGEN_SEL	Clock Generator Select Value - Initialization mode This bit is effective when Host Controller supports programmable clock generator. Read 0x1: Programmable Clock Generator. Read 0x0: Host Controller Ver2.00 Compatible Clock Generator.	R	0
9:0	INITSDCLK_SEL	SDCLK Frequency Select Value - Initialization mode 10-bit preset value to set MMCHS_SYSCTL[15:6] CLKD is described by a host system.	R	0x1E0

Table 24-125. Register Call Summary for Register MMCHS_PVINITSD

MMC/SDIO Functional Description
- MMC/SDIO Hardware Status Features: [0]

MMC/SDIO Register Manual
- MMC/SDIO Register Summary: [1] [2]

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Table 24-126. MMCHS_PVHSSDR12

Address Offset	0x0000 0264
Physical Address	0x4809 C264 0x480B 4264 0x480B 4264 0x480A D264 0x480D 1264 0x480D 1264 0x480D 5264 0x480D 5264
Description	Preset Value for High Speed and SDR12 speed modes
Type	R

31 30	29 28 27	26	25 24	23 22 21 20 19 18 17 16	15 14	13 12 11	10	9 8	7 6 5 4 3 2 1 0
SDR12DS_SEL	RESERVED	SDR12CLKGEN_SEL		SDR12SDCLK_SEL	HSDS_SEL	RESERVED	HSCLKGEN_SEL		HSSDCLK_SEL

Bits	Field Name	Description	Type	Reset
31:30	SDR12DS_SEL	Driver Strength Select Value - SDR12 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Read 0x3: Driver Type D is Selected. Read 0x2: Driver Type C is Selected. Read 0x1: Driver Type A is Selected. Read 0x0: Driver Type B is Selected.	R	0x0
29:27	RESERVED		R	0x0
26	SDR12CLKGEN_SEL	Clock Generator Select Value - SDR12 mode This bit is effective when Host Controller supports programmable clock generator. Read 0x1: Programmable Clock Generator. Read 0x0: Host Controller Ver2.00 Compatible Clock Generator.	R	0
25:16	SDR12SDCLK_SEL	SDCLK Frequency Select Value - SDR12 mode 10-bit preset value to set MMCHS_SYSCTL[15:6] CLKD is described by a host system.	R	0x004
15:14	HSDS_SEL	Driver Strength Select Value - High Speed mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Read 0x3: Driver Type D is Selected. Read 0x2: Driver Type C is Selected. Read 0x1: Driver Type A is Selected. Read 0x0: Driver Type B is Selected.	R	0x0
13:11	RESERVED		R	0x0
10	HSCLKGEN_SEL	Clock Generator Select Value - High Speed mode This bit is effective when Host Controller supports programmable clock generator. Read 0x1: Programmable Clock Generator. Read 0x0: Host Controller Ver2.00 Compatible Clock Generator.	R	0
9:0	HSSDCLK_SEL	SDCLK Frequency Select Value - High Speed mode 10-bit preset value to set MMCHS_SYSCTL[15:6] CLKD is described by a host system.	R	0x002

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Table 24-127. Register Call Summary for Register MMCHS_PVHSSDR12

MMC/SDIO Functional Description

- MMC/SDIO Hardware Status Features: [0]

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- MMC/SDIO Register Summary: [1] [2]

Table 24-128. MMCHS_PVSDR25SDR50

Address Offset	0x0000 0268
Physical Address	0x4809 C268 0x480B 4268 0x480B 4268 0x480A D268 0x480D 1268 0x480D 1268 0x480D 5268 0x480D 5268
Description	Preset Value for SDR25 and SDR50 speed modes
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDR50DS_SEL		RESERVED			SDR50CLKGEN_SEL			SDR50SDCLK_SEL								SDR25DS_SEL		RESERVED			SDR25CLKGEN_SEL			SDR25SDCLK_SEL							

Bits	Field Name	Description	Type	Reset
31:30	SDR50DS_SEL	Driver Strength Select Value - SDR50 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Read 0x3: Driver Type D is Selected. Read 0x2: Driver Type C is Selected. Read 0x1: Driver Type A is Selected. Read 0x0: Driver Type B is Selected.	R	0x0
29:27	RESERVED		R	0x0
26	SDR50CLKGEN_SEL	Clock Generator Select Value - SDR50 mode This bit is effective when Host Controller supports programmable clock generator. Read 0x1: Programmable Clock Generator. Read 0x0: Host Controller Ver2.00 Compatible Clock Generator.	R	0
25:16	SDR50SDCLK_SEL	SDCLK Frequency Select Value - SDR50 mode 10-bit preset value to set MMCHS_SYSCTL[15:6] CLKD is described by a host system.	R	0x001
15:14	SDR25DS_SEL	Driver Strength Select Value - SDR25 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Read 0x3: Driver Type D is Selected. Read 0x2: Driver Type C is Selected. Read 0x1: Driver Type A is Selected. Read 0x0: Driver Type B is Selected.	R	0x0
13:11	RESERVED		R	0x0

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Bits	Field Name	Description	Type	Reset
10	SDR25CLKGEN_SEL	Clock Generator Select Value - SDR25 mode This bit is effective when Host Controller supports programmable clock generator. Read 0x1: Programmable Clock Generato. Read 0x0: Host Controller Ver2.00 Compatible Clock Generator.	R	0
9:0	SDR25SDCLK_SEL	SDCLK Frequency Select Value - SDR25 mode 10-bit preset value to set MMCHS_SYSCTL[15:6] CLKD is described by a host system.	R	0x002

Table 24-129. Register Call Summary for Register MMCHS_PVSDR25SDR50

MMC/SDIO Functional Description • MMC/SDIO Hardware Status Features: [0]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [1] [2]

Table 24-130. MMCHS_PVSDR104DDR50

Address Offset	0x0000 026C
Physical Address	0x4809 C26C 0x480B 426C 0x480B 426C 0x480A D26C 0x480D 126C 0x480D 126C 0x480D 526C 0x480D 526C
Description	Preset Value for SDR104 and DDR50 speed modes
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDR50DS_SEL		RESERVED			DDR50CLKGEN_SEL			DDR50SDCLK_SEL								SDR104DS_SEL		RESERVED			SDR104CLKGEN_SEL			SDR104SDCLK_SEL							

Bits	Field Name	Description	Type	Reset
31:30	DDR50DS_SEL	Driver Strength Select Value - DDR50 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Read 0x3: Driver Type D is Selected. Read 0x2: Driver Type C is Selected. Read 0x1: Driver Type A is Selected. Read 0x0: Driver Type B is Selected.	R	0x0
29:27	RESERVED		R	0x0
26	DDR50CLKGEN_SEL	Clock Generator Select Value - DDR50 mode This bit is effective when Host Controller supports programmable clock generator. Read 0x1: Programmable Clock Generator Read 0x0: Host Controller Ver2.00 Compatible Clock Generator	R	0

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Bits	Field Name	Description	Type	Reset
25:16	DDR50SDCLK_SEL	SDCLK Frequency Select Value - DDR50 mode 10-bit preset value to set MMCHS_SYSCTL[15:6] CLKD is described by a host system.	R	0x002
15:14	SDR104DS_SEL	Driver Strength Select Value - SDR104 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. Read 0x3: Driver Type D is Selected. Read 0x2: Driver Type C is Selected. Read 0x1: Driver Type A is Selected. Read 0x0: Driver Type B is Selected.	R	0x0
13:11	RESERVED		R	0x0
10	SDR104CLKGEN_SEL	Clock Generator Select Value - SDR104 mode This bit is effective when Host Controller supports programmable clock generator. Read 0x1: Programmable Clock Generator. Read 0x0: Host Controller Ver2.00 Compatible Clock Generator.	R	0
9:0	SDR104SDCLK_SEL	SDCLK Frequency Select Value - SDR104 mode 10-bit preset value to set MMCHS_SYSCTL[15:6] CLKD is described by a host system.	R	0x000

Table 24-131. Register Call Summary for Register MMCHS_PVSDR104DDR50

MMC/SDIO Functional Description • MMC/SDIO Hardware Status Features: [0]
MMC/SDIO Register Manual • MMC/SDIO Register Summary: [1] [2]

Table 24-132. MMCHS_REV

Address Offset	0x0000 02FC
Physical Address	0x4809 C2FC 0x480B 42FC 0x480B 42FC 0x480A D2FC 0x480D 12FC 0x480D 12FC 0x480D 52FC 0x480D 52FC
Description	Versions Register This register contains the hard coded RTL vendor revision number, the version number of SD specification compliancy and a slot status bit. MMCHS_REV[31:16] = Host controller version MMCHS_REV[15:0] = Slot Interrupt Status
Type	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VREV								SREV								RESERVED															SIS

Bits	Field Name	Description	Type	Reset
31:24	VREV	Vendor Version Number: IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 1.0 0x21 for 2.1	R	0x--

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Bits	Field Name	Description	Type	Reset
23:16	SREV	Specification Version Number This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. Read 0x3: Reserved Read 0x2: SD Host Specification Version 3.00. Read 0x1: SD Host Specification Version 2.00 - Including the feature of the ADMA and Test Register. Read 0x0: SD Host Specification Version 1.00.	R	0x02
15:1	RESERVED		R	0x0000
0	SIS	Slot Interrupt Status This status bit indicates the inverted state of interrupt signal for the module. By a power on reset or by setting a software reset for all (MMCHS_HCTL[SRA]), the interrupt signal shall be de-asserted and this status shall read 0.	R	0

Table 24-133. Register Call Summary for Register MMCHS_REV

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- MMC/SDIO Register Summary: [0] [1]
- MMC/SDIO Register Description: [2] [3]

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General-Purpose Interface

This chapter describes the general-purpose interface on the device.

NOTE: Some of the GPIO channels are not available in all OMAP54xx devices.

For details, see , *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

Topic **Page**

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25.2 General-Purpose Interface Environment 5753
25.3 General-Purpose Interface Integration 5757
25.4 General-Purpose Interface Functional Description 5761
25.5 General-Purpose Interface Programming Guide 5776
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25.1 General-Purpose Interface Overview

The general-purpose interface combines eight general-purpose input/output (GPIO) banks.

Each GPIO module provides 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 256 (8 × 32) pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations.
- Wake-up request generation in idle mode upon the detection of external events

These modules do not include pad control (pullup/down control, open-drain feature). For more information, see Section 18.4.8, *Pad Functional Multiplexing and Configuration,* in Chapter 18, *Control Module*.

Figure 25-1 is an overview of the general-purpose interface.

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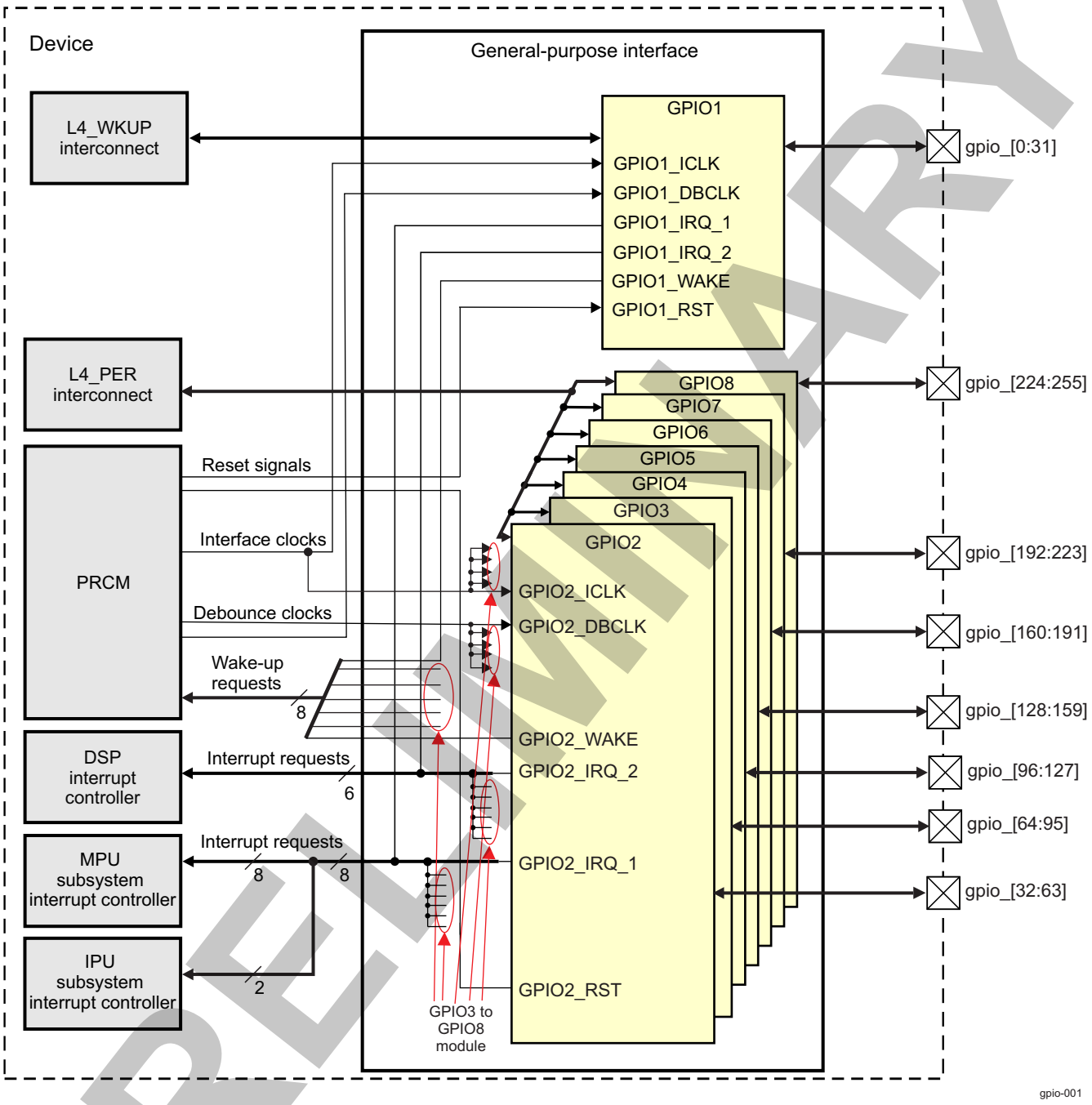
Figure 25-1. General-Purpose Interface Overview



The GPIO modules include the following global features:

- Two identical submodules can process synchronous interrupt requests from each channel to be used independently in a biprocessor environment. Each submodule controls its own synchronous interrupt request line. Each submodule also has its own interrupt-enable and interrupt status registers. The interrupt-enable register (GPIO_IRQSTATUS_SET_x [where x = 0 or 1]) selects the channel considered for the interrupt request generation. The interrupt status register (GPIO_IRQSTATUS_RAW_x) determines which channel has activated the interrupt request. Event detection on GPIO channels is reflected into GPIO_IRQSTATUS_RAW independently from the content of the interrupt-enable registers.
- Wake-up requests in idle mode from input channels are merged together to issue one wake-up signal per GPIO module.

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- Data input (capture)/output (drive)
- Power-management support

The general-purpose interface has 14 interrupt lines (two interrupt lines per GPIO1 through GPIO6 modules and one interrupt line per GPIO7 and GPIO8).

Each GPIO module produces a wake-up request signal to the power, reset, and clock management (PRCM) module.

Each channel in the GPIO modules has the following features:

- The GPIOi.GPIO_OE register controls the output capability for each pin.
- The output line level reflects the value written in the GPIOi.GPIO_DATAOUT register through the level 4 (L4) interconnect.
- The input line can be fed to the GPIO module through an optional and configurable debounce cell. (Because the debouncing time value is global for all ports of one GPIO module, up to five different debouncing time values are possible.)
- The value of the input line is sampled into the GPIOi.GPIO_DATAIN register and can be read through the L4 interconnect.
- In active mode, the input line can be used through level and edge detectors to trigger synchronous interrupts. The edge (rising, falling, or both) or the level used (logical 0, logical 1, or both) can be configured.
- In idle mode, the input line can be used to activate the asynchronous wake-up request (on edge detection: rising edge, falling edge, or both).

The module provides an alternative to the atomic test and set operations for the data-output register (GPIO_DATAOUT). For this register, the module implements the set-and-clear protocol register update (see Section 25.4.9, *General-Purpose Interface Set-and-Clear Protocol*).

All module registers are 8-, 16-, or 32-bit accessible through the OCP-compatible interface (little-endian encoding)

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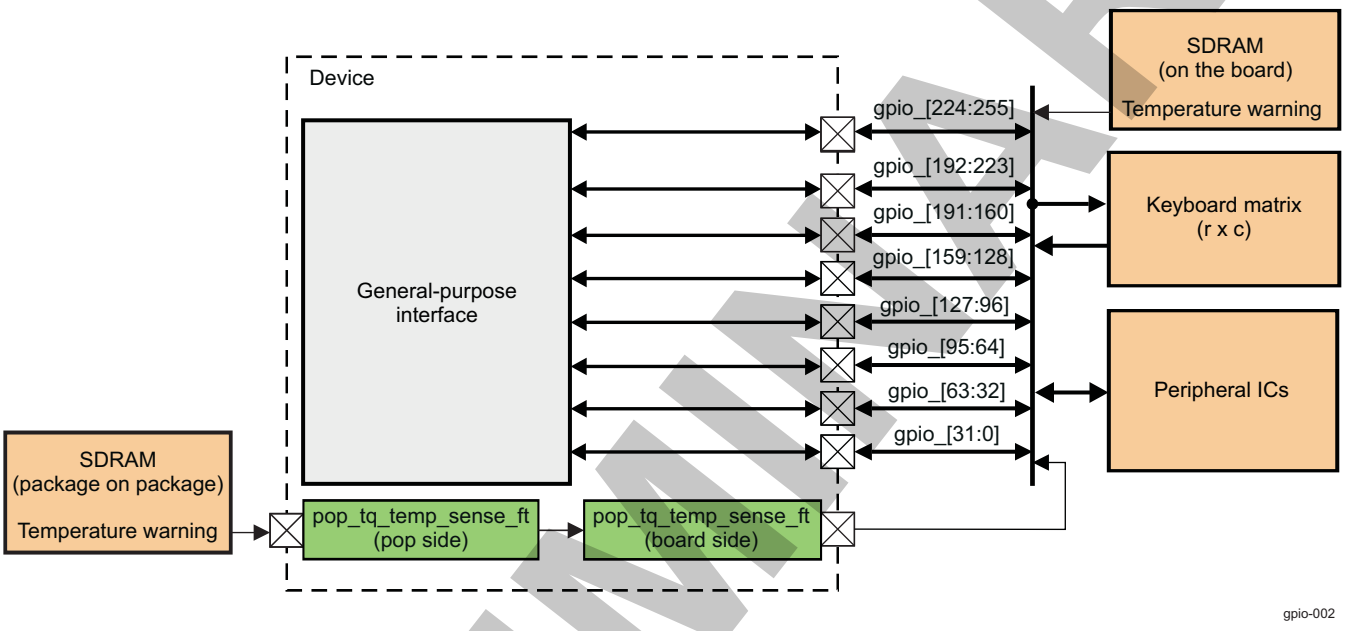
25.2 General-Purpose Interface Environment

The general-purpose interface combines eight GPIO modules for a flexible, user-programmable, general-purpose input/output (I/O) controller. The general-purpose interface implements functions that are not implemented with the dedicated controllers in the device and require simple input and/or output software-controlled signals. The GPIO allows a variety of custom connections and expands the I/O capabilities of the system to the real world.

Figure 25-2 shows a typical application using the general-purpose interface.

Figure 25-2. General-Purpose Interface Typical Application



NOTE: Temperature Sensing

Most memories provide a temperature sensor to control the autorefresh duty cycle. The device monitors the temperature of the external memory using the pop_tq_temp_sense_ft ball and a GPIO input. To do this, pop_tq_temp_sense_ft is connected to a GPIO through the customer board. This feature is application-dependent.

CAUTION

Because of buffer strength, an external serial resistor must be connected to the balls where gpio_46 through gpio_55 are muxed with MMC signals.

The general-purpose interface can physically connect the device to a keyboard matrix and peripheral integrated circuits (ICs).

25.2.1 General-Purpose Interface as a Keyboard Interface

The general-purpose interface can be used as a keyboard interface. Channels can be dedicated based on the keyboard matrix (r × c). Figure 25-3 shows row channels configured as inputs with the input debounce feature enabled. The row channels are driven high with an external pullup. Column channels are configured as outputs and drive a low level.

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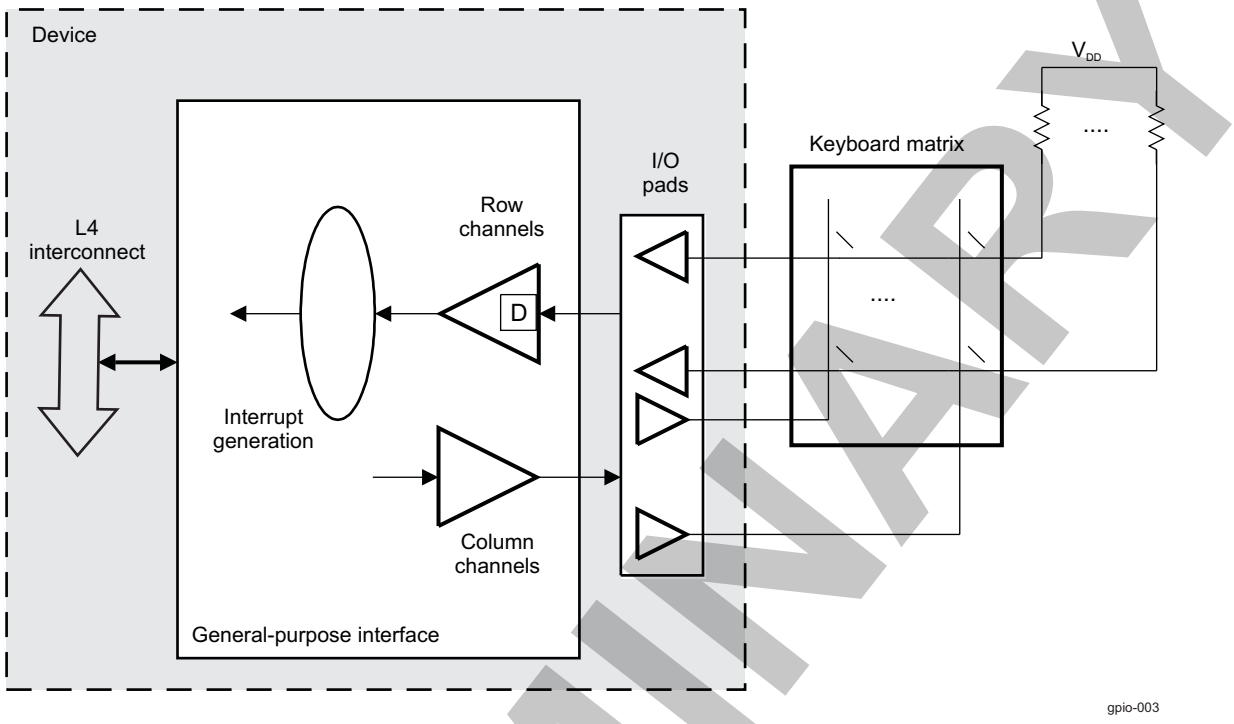
Figure 25-3. General-Purpose Interface Used as a Keyboard Interface



When a keyboard matrix key is pressed, the corresponding row and column lines are shorted together and a low level is driven on the corresponding row channel. This generates an interrupt based on the proper configuration (see Section 25.4.6, *Interrupt and Wake-up Requests*).

When the keyboard interrupt is received, the processor (microprocessor unit [MPU] and/or digital signal processor [DSP] subsystem) can disable the keyboard interrupt and scan the column channels for the key coordinates.

- The scanning sequence has as many states as column channels: For each step in the sequence, the processor drives one column channel low and the others high.
- The processor reads the values of the row channels and thus detects which keys in the column are pressed.

At the end of the scanning sequence, the processor establishes which keys are pressed. The keyboard interface can then be reconfigured in the interrupt waiting state.

25.2.2 General-Purpose Interface Signals

Table 25-1 describes the module signals.

Table 25-1. I/O Description

Signal	I/O[1]	Description	Reset Value[2]
gpio1_wkout[0:5]	O	GPIO (direct wake-up path)	Hi-Z
gpio1_wk[6:31]	I/O	GPIO (direct wake-up path)	Hi-Z
gpio2_[32:63]	I/O	GPIO	Hi-Z
gpio3_[64:95]	I/O	GPIO	Hi-Z
gpio4_[96:127]	I/O	GPIO	Hi-Z
gpio5_[128:156]	I/O	GPIO	Hi-Z
gpio5_in157	I	GPIO (inputs only)	Hi-Z
gpio5_[158:159]	I/O	GPIO	Hi-Z

(1) I = Input; O = Output; I/O = Bidirectional
(2) Hi-Z = High Impedance

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Table 25-1. I/O Description (continued)

Signal	I/O[1]	Description	Reset Value[2]
gpio6_[160:191]	I/O	GPIO	Hi-Z
gpio7_[192:223]	I/O	GPIO	Hi-Z
gpio8_[224:235]	I/O	GPIO	Hi-Z
gpio8_in[236:255]	I	GPIO (inputs only)	Hi-Z

Figure 25-4 shows the signal connections of GPIO1.

Figure 25-4. GPIO1 Signal Connections

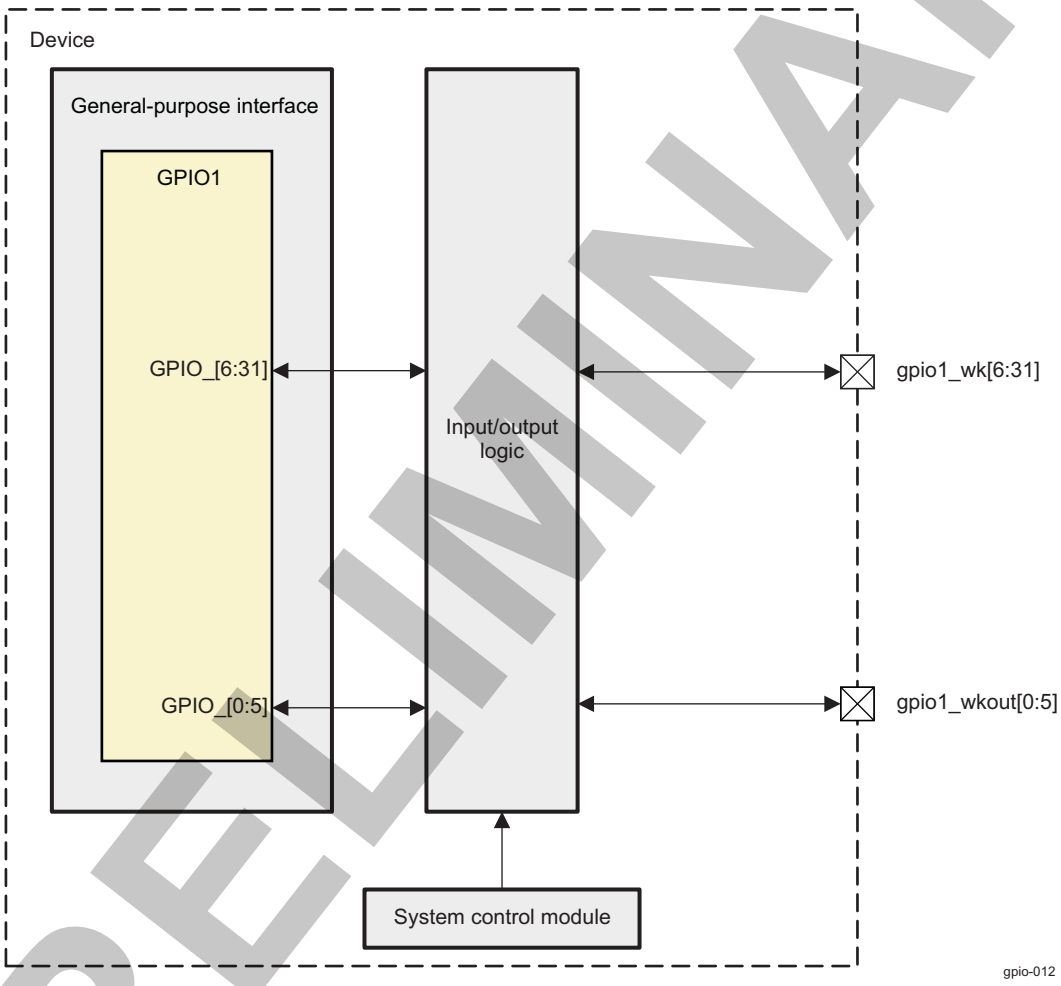

Figure 25-5 shows the signal connections of GPIO2 through GPIO8.

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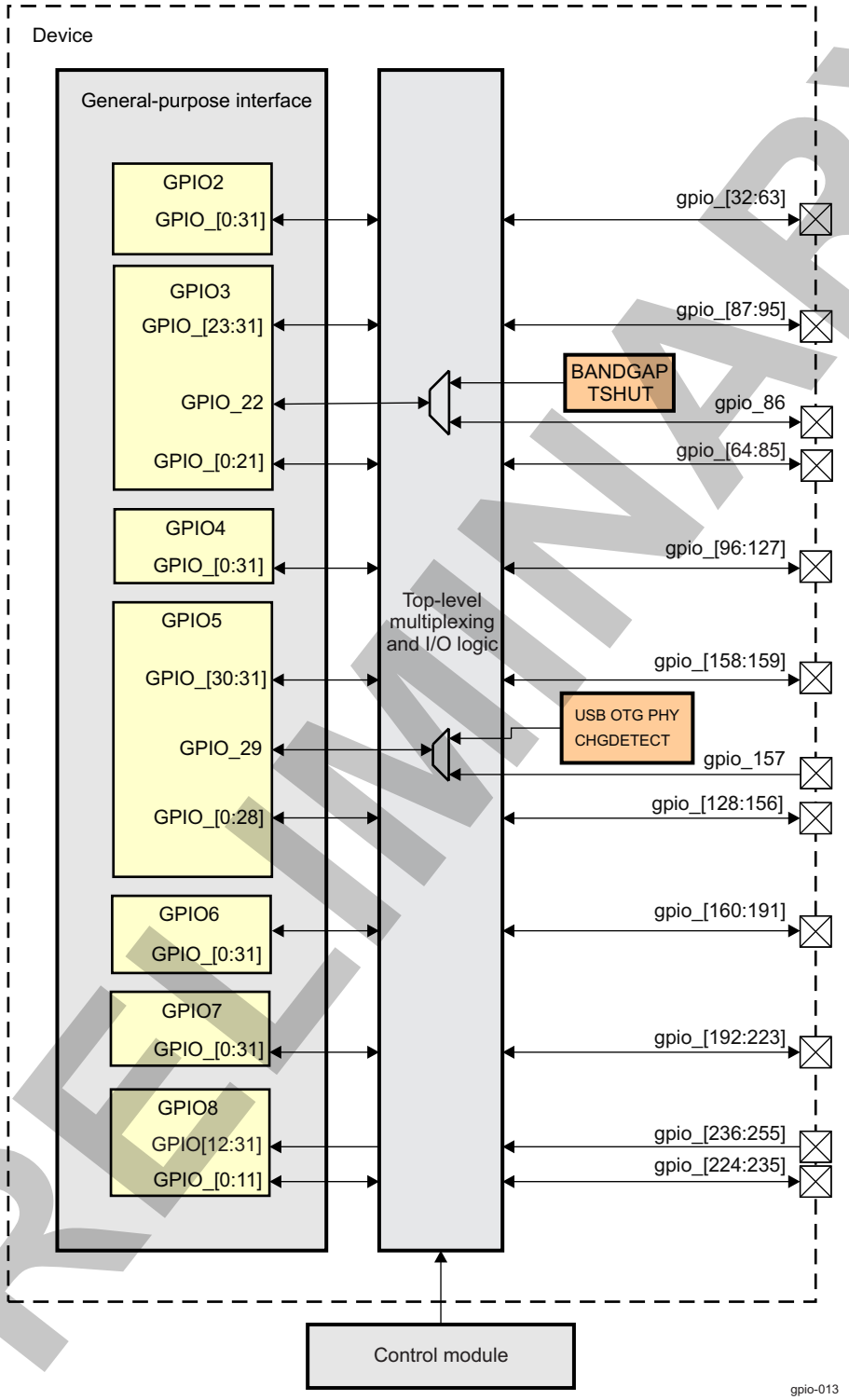
Figure 25-5. GPIO2 Through GPIO8 Signal Connections



NOTE: For more information about the GPIO1 through GPIO8 signals and channel description, see Section 25.4.7, *General-Purpose Interface Channels Description.*

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NOTE: For more information about GPIO signal multiplexing, see Section 18.4.8, *Pad Functional Multiplexing and Configuration, and Section 18.4.12.7.5 Device Interfaces Signal Group Controls Mapping* in Chapter 18, *Control Module*.

25.3 General-Purpose Interface Integration

This section describes module integration in the device, including information about clocks, resets, and hardware requests.

Figure 25-6 shows this module integration.

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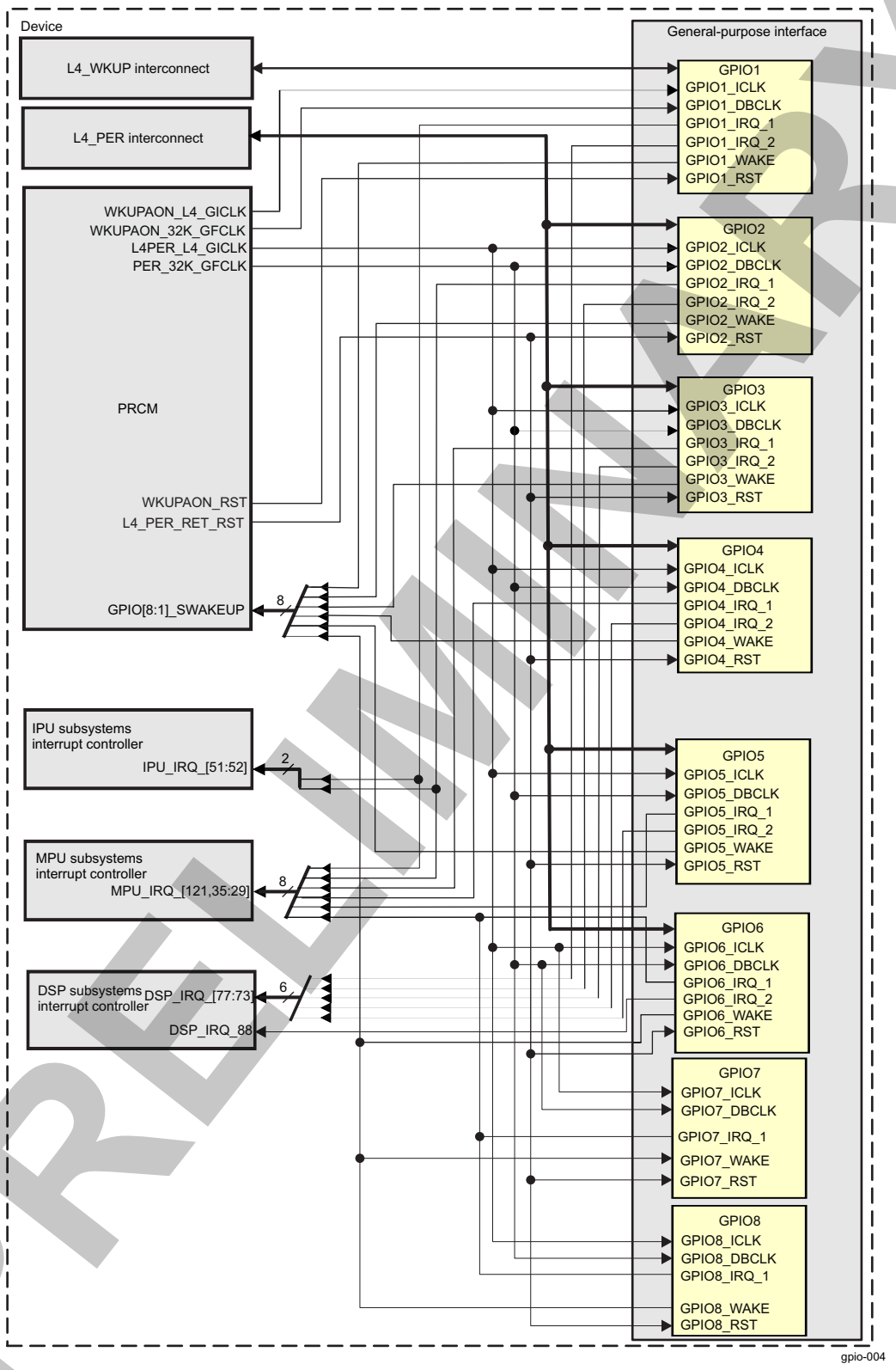
Figure 25-6. GPIO Integration



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NOTE: For more information about the IDLE hardware handshake and the wake-up request, see Section 3.1.1.1, *Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

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Table 25-2 through Table 25-4 summarize the integration of the module in the device.

Table 25-2. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
GPIO1	PD_WKUPAON	L4_WKUP
GPIOi (where i = 2 to 8)	PD_L4_PER	L4_PER

Table 25-3. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
GPIO1	GPIO1_ICLK	WKUPAON_GICLK	PRCM	GPIO interface clock
GPIO1	GPIO1_DBCLK	WKUPAON_32K_GFCLK	PRCM	GPIO debounce clock
GPIO2	GPIO2_ICLK	L4PER_L4_GICLK	PRCM	GPIO interface clock
GPIO2	GPIO2_DBCLK	PER_32K_GFCLK	PRCM	GPIO debounce clock
GPIO3	GPIO3_ICLK	L4PER_L4_GICLK	PRCM	GPIO interface clock
GPIO3	GPIO3_DBCLK	PER_32K_GFCLK	PRCM	GPIO debounce clock
GPIO4	GPIO4_ICLK	L4PER_L4_GICLK	PRCM	GPIO interface clock
GPIO4	GPIO4_DBCLK	PER_32K_GFCLK	PRCM	GPIO debounce clock
GPIO5	GPIO5_ICLK	L4PER_L4_GICLK	PRCM	GPIO interface clock
GPIO5	GPIO5_DBCLK	PER_32K_GFCLK	PRCM	GPIO debounce clock
GPIO6	GPIO6_ICLK	L4PER_L4_GICLK	PRCM	GPIO interface clock
GPIO6	GPIO6_DBCLK	PER_32K_GFCLK	PRCM	GPIO debounce clock
GPIO7	GPIO7_ICLK	L4PER_L4_GICLK	PRCM	GPIO interface clock
GPIO7	GPIO7_DBCLK	PER_32K_GFCLK	PRCM	GPIO debounce clock
GPIO8	GPIO8_ICLK	L4PER_L4_GICLK	PRCM	GPIO interface clock
GPIO8	GPIO8_DBCLK	PER_32K_GFCLK	PRCM	GPIO debounce clock
Resets				
GPIO1	GPIO1_RST	WKUPAON_RST	PRCM	GPIO reset signal
GPIO2	GPIO2_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO3	GPIO3_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO4	GPIO4_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO5	GPIO5_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO6	GPIO6_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO7	GPIO7_RST	L4_PER_RET_RST	PRCM	GPIO reset signal
GPIO8	GPIO8_RST	L4_PER_RET_RST	PRCM	GPIO reset signal

Table 25-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
GPIO1	GPIO1_IRQ_2	DSP_IRQ_73	DSP	An interrupt to DSP (second interrupt)
GPIO1	GPIO1_IRQ_1	MPU_IRQ_29	MPU	An interrupt to MPU subsystem interrupt controller (INTC) (first interrupt)
GPIO1	GPIO1_IRQ_1	IPU_IRQ_51	IPU	An interrupt to IPU subsystem INTC (first interrupt)
GPIO2	GPIO2_IRQ_2	DSP_IRQ_74	DSP	An interrupt to DSP (second interrupt)
GPIO2	GPIO2_IRQ_1	MPU_IRQ_30	MPU	An interrupt to MPU subsystem INTC (first interrupt)

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Table 25-4. Hardware Requests (continued)

GPIO2	GPIO2_IRQ_1	IPU_IRQ_52	IPU	An interrupt to IPU subsystem INTC (first interrupt)
GPIO3	GPIO3_RQ_2	DSP_IRQ_75	DSP	An interrupt to DSP (second interrupt)
GPIO3	GPIO3_IRQ_1	MPU_IRQ_31	MPU	An interrupt to MPU subsystem INTC (first interrupt)
GPIO4	GPIO4_IRQ_2	DSP_IRQ_76	DSP	An interrupt to DSP (second interrupt)
GPIO4	GPIO4_IRQ_1	MPU_IRQ_32	MPU	An interrupt to MPU subsystem INTC (first interrupt)
GPIO5	GPIO5_IRQ_2	DSP_IRQ_77	DSP	An interrupt to DSP (second interrupt)
GPIO5	GPIO5_IRQ_1	MPU_IRQ_33	MPU	An interrupt to MPU subsystem INTC (first interrupt)
GPIO6	GPIO6_IRQ_2	DSP_IRQ_88	DSP	An interrupt to DSP (second interrupt)
GPIO6	GPIO6_IRQ_1	MPU_IRQ_34	MPU	An interrupt to MPU subsystem INTC (first interrupt)
GPIO7	GPIO_IRQ_1	MPU_IRQ_35	MPU	An interrupt to MPU subsystem INTC (first interrupt)
GPIO8	GPIO_IRQ_1	MPU_IRQ_121	MPU	An interrupt to MPU subsystem INTC (first interrupt)

NOTE: For the description of the interrupt source, see Section 25.4.6, *Interrupt and Wake-Up Requests*.

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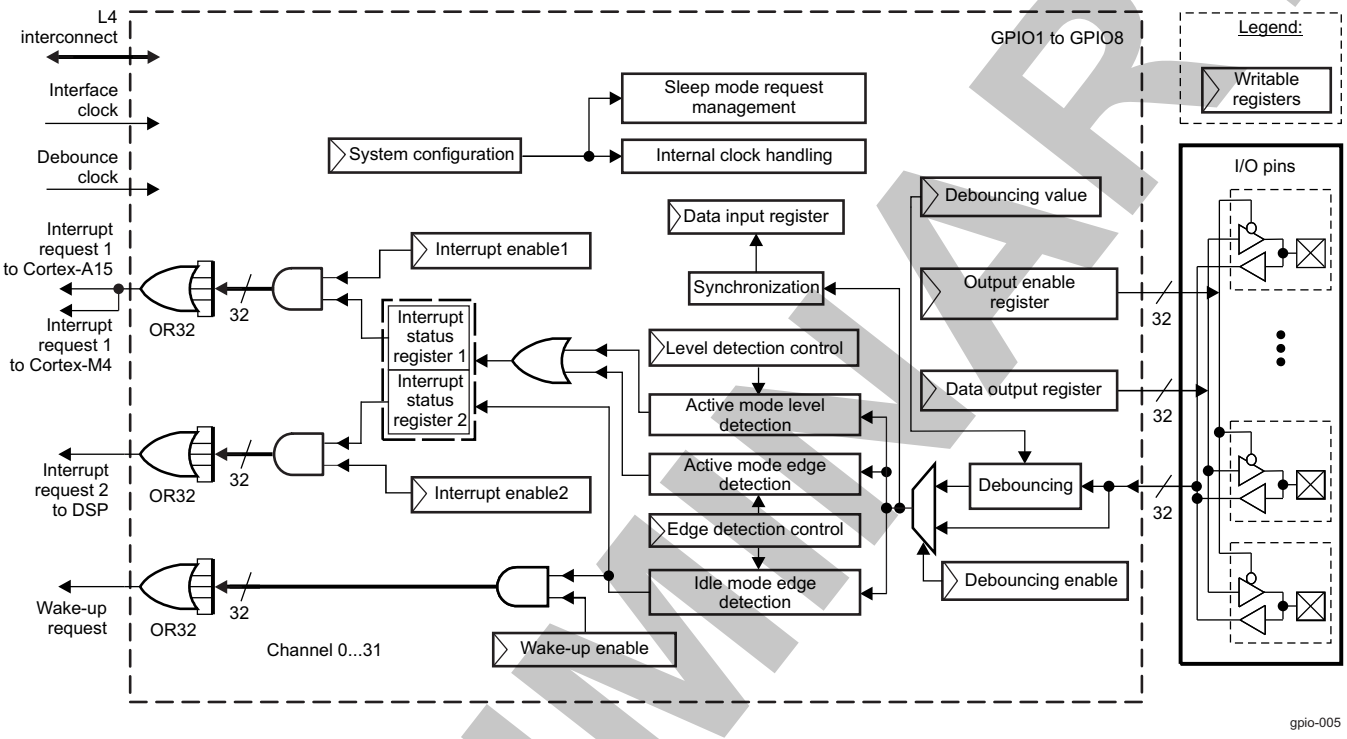
25.4 General-Purpose Interface Functional Description

25.4.1 General-Purpose Interface Block Diagram

Figure 25-7 shows the general-purpose interface block diagram.

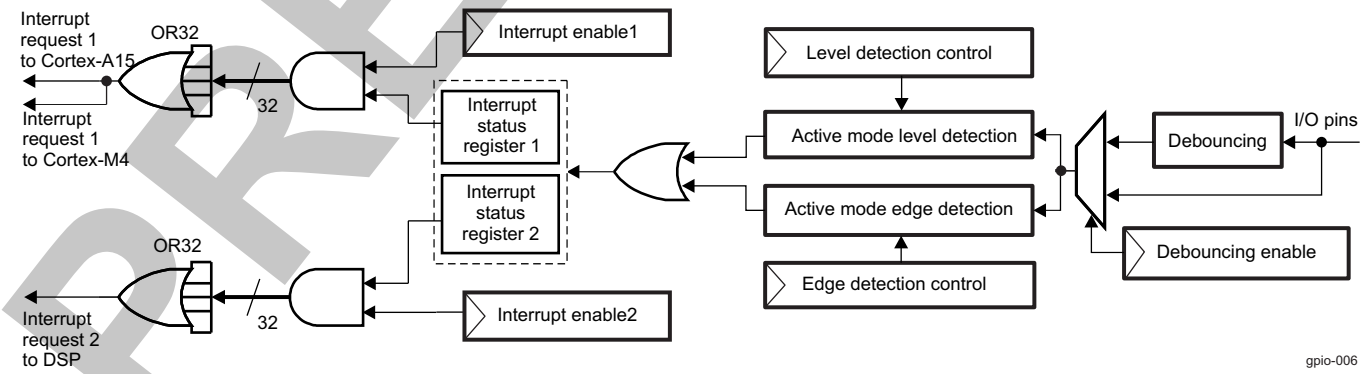
Figure 25-7. General-Purpose Interface Block Diagram



shows the details of the GPIO modules in the general-purpose interface block diagram, including their configuration registers and main functional paths:

- The synchronous path (for active mode operation) used to generate a synchronous interrupt request on expected event detection on any input GPIO. Synchronous interrupt request lines 1 and 2 are active based on their respective interrupt-enable1 and 2 registers (GPIOi.GPIO_IRQSTATUS_SET_0, GPIOi.GPIO_IRQSTATUS_SET_1, GPIOi.GPIO_IRQSTATUS_CLR_0, and GPIOi.GPIO_IRQSTATUS_CLR_1). See Figure 25-8.

Figure 25-8. Synchronous Path



- The asynchronous path (for idle mode operation) used to generate an asynchronous wake-up request on the expected edge detection on any input GPIO. The asynchronous wake-up request line is active based on the wake-up-enable register. See Figure 25-9.

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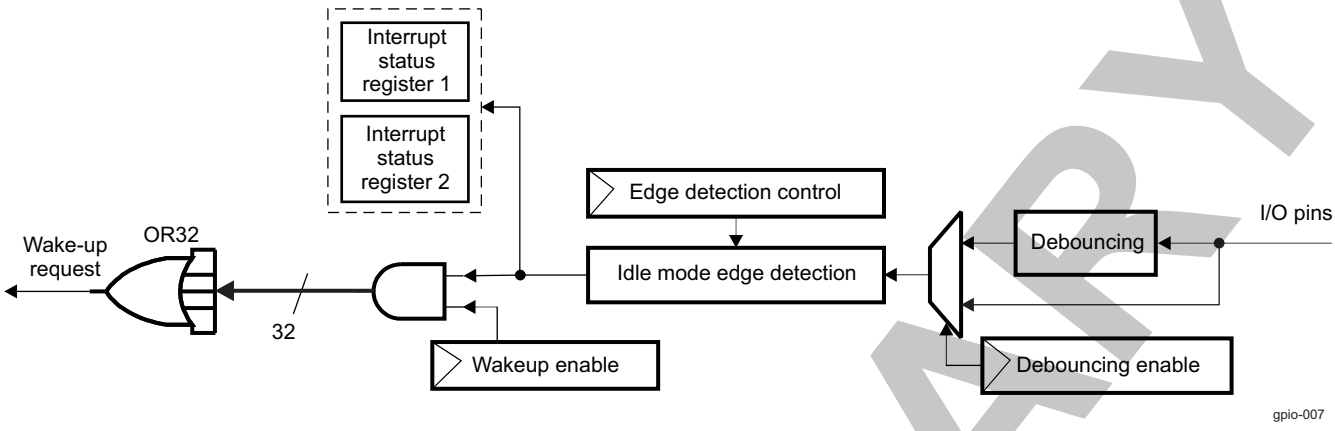
Figure 25-9. Asynchronous Path



- The blocks handling the internal clock (clock gating) and managing the sleep mode request/acknowledge protocol (enabling the synchronous path in active mode and the asynchronous path in idle mode)

25.4.2 General-Purpose Interface Interrupt and Wake-Up Features

25.4.2.1 Synchronous Path: Interrupt Request Generation

The general-purpose interface has 14 interrupt lines (two interrupt lines per GPIO module instance for biprocessor operation for GPIO1 through GPIO6 and one interrupt line for GPIO7 and GPIO8 module instance). The 14 interrupt signals are GPIOi_IRQ_1 (used by the MPU, IPU subsystems) and GPIOi_IRQ_2 (used by the DSP subsystem), where i = 1 to 7, and 8 (for interrupt line 2 [where i = 1 to 6]).

Synchronous interrupt requests from each channel are processed by two identical interrupt generation submodules used independently by the DSP subsystem on one side and by the MPU, IPU subsystems on the other side. Each submodule controls its own synchronous interrupt request line and has its own interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_SET_0, GPIOi.GPIO_IRQSTATUS_SET_1, GPIOi.GPIO_IRQSTATUS_CLR_0, and GPIOi.GPIO_IRQSTATUS_CLR_1) and interrupt status registers (GPIOi.GPIO_IRQSTATUS_RAW_0 and GPIOi.GPIO_IRQSTATUS_RAW_1). The interrupt-enable register selects the channel(s) considered for the interrupt request generation, and the interrupt status register determines which channel(s) activate the interrupt request. Event detection on GPIO channels is reflected in the interrupt status registers independent of the content of the interrupt-enable registers.

In active mode, when the GPIO configuration registers are set to enable the interrupt generation (see Section 25.4.6, *General-Purpose Interface Interrupt and Wake-Up Requests*), a synchronous path samples the transitions and levels on the input GPIO with the internally gated interface clock (see Section 25.4.5.2.4, *Module Power Saving*). When an event matches the programmed settings (see Section 25.4.6, *General-Purpose Interface Interrupt and Wake-Up Requests*), the corresponding bit in the interrupt status register (GPIO_IRQSTATUS_RAW_x [where x = 0 or 1]) is set to 1, and on the following interface clock cycle, interrupt lines 1 and/or 2 are activated (depending on the interrupt-enable registers GPIO_IRQSTATUS_SET_x [where x = 0 or 1]).

Because of the sampling operation, the minimum pulse width on the input GPIO to trigger a synchronous interrupt request is two times the internally gated interface clock period (that is, *N* times the interface clock period; see Section 25.4.5.2.4, *Module Power Saving*). This minimum pulse width must be met before and after any expected level transition detection. Level detection requires the selected level to be stable for at least two times the internally gated interface clock period to trigger a synchronous interrupt.

Because the module is synchronous, latency is minimal between the expected event occurrence and the activation of the interrupt line(s). This latency must not exceed three internally gated interface clock cycles plus two interface clock cycles when the debounce feature is not used.

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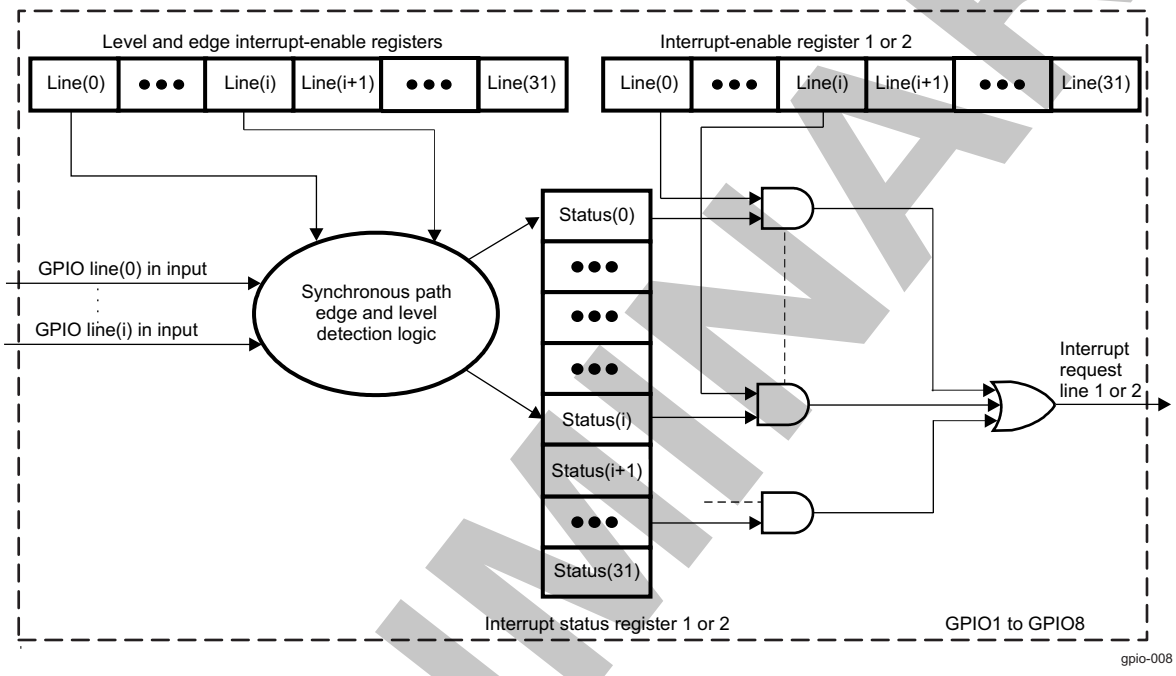
When the debounce feature is active, the latency depends on the value of the debouncing time register (GPIOi.GPIO_DEBOUNCINGTIME) (see Section 25.4.3, *General-Purpose Interface Clock Configuration*) and is less than three internally gated interface clock cycles plus two interface clock cycles plus GPIOi.GPIO_DEBOUNCINGTIME register value debounce clock cycles plus three debounce clock cycles.

Synchronous interrupt request line 1 is mapped on the MPU, IPU subsystems.

Synchronous interrupt request line 2 is mapped on the DSP INTC.

Figure 25-10 is an overview of the interrupt request generation.

Figure 25-10. Interrupt Request Generation



25.4.2.2 Asynchronous Path: Wake-Up Request Generation

The general-purpose interface has eight wake-up lines (one wake-up line per GPIO module instance) connected to the PRCM module.

Asynchronous wake-up requests from input channels are merged to issue one wake-up signal to the system per GPIO module. The wake-up-enable registers (GPIOi.GPIO_IRQWAKEN_0 and GPIOi.GPIO_IRQWAKEN_1) select the channel(s) considered for the wake-up request generation. The asynchronous wake-up request is reflected into the synchronous interrupt status registers (GPIOi.GPIO_IRQSTATUS_RAW_0 and GPIOi.GPIO_IRQSTATUS_RAW_1).

In idle mode (the interface clock is shut down and the GPIO configuration registers are programmed; see Section 25.4.6, *General-Purpose Interface Interrupt and Wake-Up Requests*), an asynchronous path detects the expected transition(s) on a GPIO input (based on register programming) and activates an asynchronous wake-up request by the sideband signal (GPIOi_SWAKEUP [where i = 1 to 8), if the wake-up-enable register is set.

When the system is awakened, the interface clock is restarted and synchronously set to 1 based on the input GPIO pin triggering the wake-up request and the corresponding bit in the interrupt status registers (GPIOi.GPIO_IRQSTATUS_RAW_0 and GPIOi.GPIO_IRQSTATUS_RAW). On the following internal clock cycle, interrupt lines 1 and/or 2 are active (active high) when the corresponding bits are set in the interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_SET_0, GPIOi.GPIO_IRQSTATUS_SET_0, GPIOi.GPIO_IRQSTATUS_CLR_0, and GPIOi.GPIO_IRQSTATUS_CLR_1).

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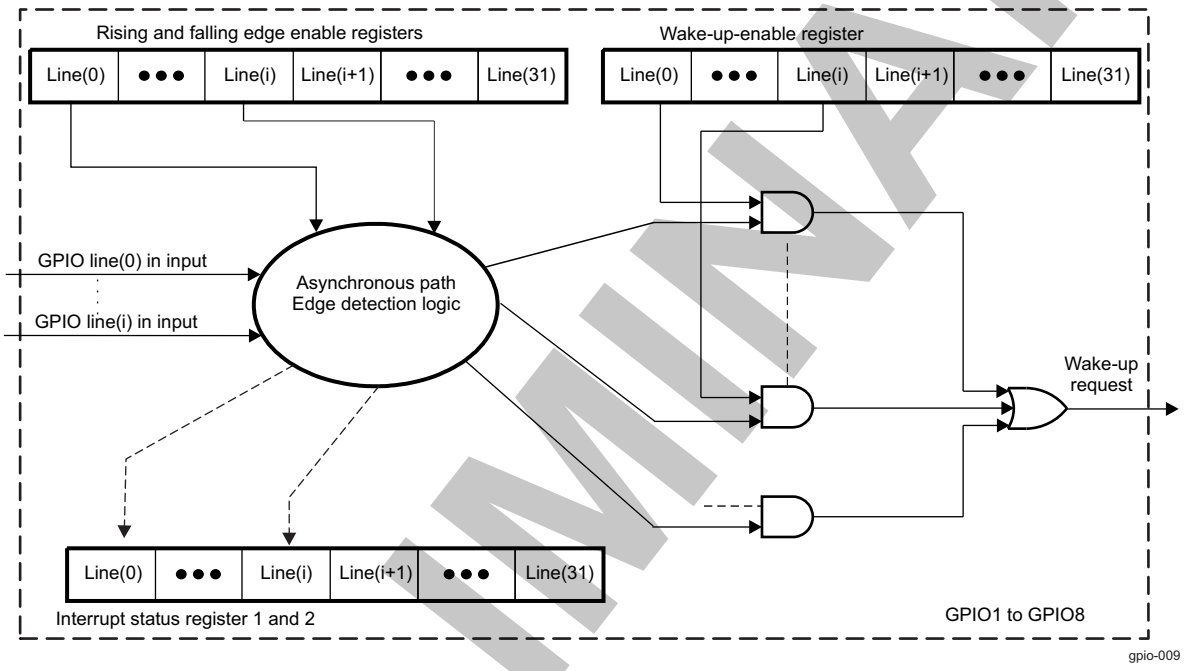
NOTE:

- If the debouncing is not enabled, there is no minimum input pulse width to trigger the wake-up request, because there is no sampling operation.
- If the debouncing is used, the minimum pulse width is set by the debouncing specified time.
- The ENAWAKEUP bit of the GPIO_SYSCONFIG register allows the enabling or disabling of the GPIO wake-up feature globally: if this bit is set to 0, GPIO_IRQWAKEN_x has no effect

Figure 25-11 is an overview of the wake-up request generation.

Figure 25-11. Wake-Up Request Generation



25.4.2.3 Wake-Up Event Conditions During Transition To/From IDLE State

In phase A, only the synchronous path is enabled. A synchronous interrupt request (see Section 25.4.2.1, *Synchronous Path: Interrupt Request Generation*) activates the interrupt line(s) and prevents the GPIO from transitioning into IDLE state until the interrupt is cleared.

In phase B, the asynchronous path and synchronous path are enabled during the first five functional clock cycles of SLEEPTRANS state. During this period a synchronous interrupt request (see Section 25.4.2.1, *Synchronous Path: Interrupt Request Generation*) prevents the GPIO from transitioning into IDLE state. A shorter pulse puts the module into IDLE state but triggers a wakeup once in IDLE.

In phase C, only the asynchronous path is enabled. A wake-up request (see Section 25.4.2.2, *Asynchronous Path: Wake-Up Request Generation*) triggers a wake-up request from the GPIO and when the module is awakened an interrupt is generated. If debouncing is not enabled, there is no minimum input pulse width to trigger the wake-up request.

In phase D, eight open-core protocol (OCP) clock cycles occur until the module is in FUNCT state, the synchronous path is enabled, and an event that fulfills the pulse width requirements (see Section 25.4.2.1, *Synchronous Path: Interrupt Request Generation*) activates the interrupt line(s).

In phase E, only the synchronous path is enabled. A synchronous interrupt request (see Section 25.4.2.1, *Synchronous Path: Interrupt Request Generation*) activates the interrupt line(s).

Figure 25-12 shows the wake-up event conditions.

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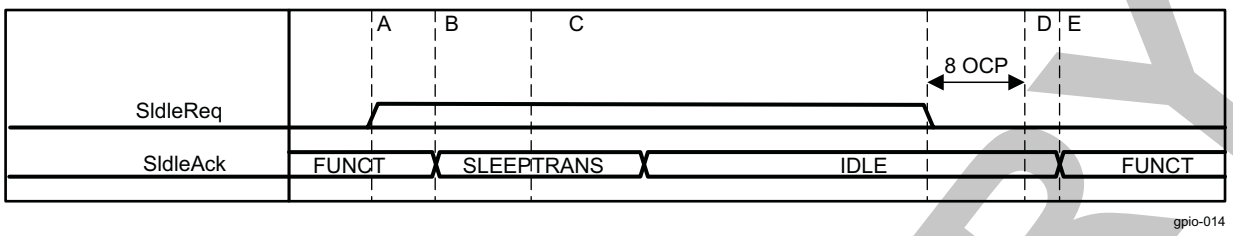
Figure 25-12. Wake-Up Event Conditions



25.4.2.4 Interrupt (or Wake-Up) Line Release

When the host processor (the MPU and/or DSP subsystem in the device) receives an interrupt request issued by the GPIO module, it reads the corresponding interrupt status register (GPIOi.GPIO_IRQSTATUS_0 or GPIOi.GPIO_IRQSTATUS_1) to determine which GPIO input triggered the interrupt (or the wake-up request).

After servicing the interrupt (or acknowledging the wake-up request), the software resets the status bit and releases the interrupt line by setting the corresponding bit of the interrupt status register to 1. If there is still a pending interrupt request to serve (all bits in the interrupt status register that are not masked by the interrupt-enable register are not cleared), the interrupt line is reasserted.

NOTE: The status bit must be reset to re-enter idle mode.

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25.4.3 General-Purpose Interface Clock Configuration

25.4.3.1 Clocking

Each GPIO module uses two clocks:

- Debounce clock: The 32-kHz debounce clock, GPIOi_DBCLK (where i = 1 to 8 with one debounce clock per module), comes from the PRCM module and is used to debounce the submodule logic (without the corresponding configuration registers). This module can sample the input line and filter the input level using a programmed delay.

  The debouncing value register (GPIOi.GPIO_DEBOUNCINGTIME) is used to set the debouncing time for all input lines in the GPIO module. Because the value is global for all the ports of one GPIO module, up to eight different debouncing values are possible. The debounce cell runs with the debounce clock (32 kHz). This register represents the number of clock cycle(s) to be used.

  The following formula describes the required input stable time to be propagated to the debounced output:

  Required input line stable = (the value of the GPIOi.GPIO_DEBOUNCINGTIME[7:0] DEBOUNCETIME bit field + 1) × 31,

  where the value of the GPIOi.GPIO_DEBOUNCINGTIME[7:0] DEBOUNCETIME bit field is from 0 to 255.

  For more information, see Section 3.6.8, *CD_L4_PER_Clock Domain*, and Section 3.6.4, *CD_WKUPAON Clock Domain*, in Chapter 3, *Power, Reset, and Clock Management*.

- Interface clock: The interface clock, GPIOi_ICLK (where i = 1 to 8), comes from the PRCM module and is used throughout the GPIO module (except within the debounce cell logic). GPIOi_ICLK clocks the data exchanges between the L4 interconnect and the internal logic. The clock-gating features allow module power consumption to be adapted to the activity.

  For more information, see Section 3.6.8, *CD_L4_PER_Clock Domain*, and Section 3.6.4, *CD_WKUPAON Clock Domain*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 25-3 describes the clocks in the GPIO modules.

Table 25-5 summarizes the functional clock configuration.

Table 25-5. Functional Clock Configuration

Interface Clock	GPIO_CTRL[2:1]GATINGRATIO	Functional Clock
GPIOi_ICLK (where i = 1 to 8)	00	GPIOi_ICLK /1 (where i = 1 to 8)
GPIOi_ICLK (where i = 1 to 8)	01	GPIOi_ICLK /2 (where i = 1 to 8)
GPIOi_ICLK (where i = 1 to 8)	10	GPIOi_ICLK /4 (where i = 1 to 8)
GPIOi_ICLK (where i = 1 to 8)	11	GPIOi_ICLK /8 (where i = 1 to 8)

25.4.4 General-Purpose Interface Hardware and Software Reset

The GPIO can be reset by using the domain reset (hardware reset) or by setting a dedicated configuration bit (software reset) in each GPIO module.

- Hardware reset: The GPIO2 to GPIO8 modules are attached to the L4_PER_RET_RST reset domain. GPIO1 is attached to the WKUPAON_RST reset domain.

  The hardware reset has a global reset action on the GPIO modules of the general-purpose interface. All configuration registers and internal logic are reset when it is active (low level). In each GPIO module, the GPIOi.GPIO_SYSSTATUS[0] RESETDONE bit monitors the internal reset status; it is set when the reset completes. For more information, see Section 3.5.4, *Reset Domains*, in Chapter 3, *Power, Reset, and Clock Management*.

- Software reset: Each GPIO module has its own software reset using the GPIOi.GPIO_SYSCONFIG[1] SOFTRESET bit. The software reset has the same effect as the hardware reset signal, but this reset can be applied on one or more modules.

  Setting the GPIOi.GPIO_SYSCONFIG[1] SOFTRESET bit to 1 resets the module. A bit value of 1 remains until the reset completes. When the software reset completes, the

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GPIOi.GPIO_SYSCONFIG[1] SOFTRESET bit is automatically reset to 0 and has the same effect as a hardware reset. The GPIOi.GPIO_SYSSTATUS[0] RESETDONE bit is cleared during a software reset. RESETDONE is set to 1 when the software reset completes.

25.4.5 General-Purpose Interface Power Management

25.4.5.1 Power Domain

GPIO1 is attached to the WKUPAON power domain (see Section 3.1.1.2, *Power Management*, in Chapter 3, *Power, Reset, and Clock Management*). This domain is composed of the logic permanently supplied to manage domain power state transitions and detect wake-up events. The WKUPAON power domain is continuously active. The GPIO2 to GPIO8 modules are attached to the L4PER power domain (see Section 3.1.1.2, *Power Management*, in Chapter 3, *Power, Reset, and Clock Management*). The L4PER power domain is not active continuously.

25.4.5.2 Power Management

25.4.5.2.1 Idle Scheme

To reduce dynamic consumption, an efficient idle scheme is based on the following:

- Efficient local autoclock gating for each module
- The implementation of control sideband signals between the PRCM module and each module

This enhanced idle control allows clocks to be activated and deactivated safely without requiring complex software management.

The idle mode request, idle acknowledge, and wake-up request (GPIOi_WAKEUP) are sideband signals between the PRCM module and the general-purpose interface (see Section 25.4.6.2, *Wake-Up Requests Generation*).

25.4.5.2.2 Operating Modes

Three operating modes are defined for the module:

- Active mode: The module runs synchronously on the interface clock; interrupts can be generated based on the configuration and external signals.
- Idle mode: Power-saving mode with the module in a waiting state. The interface clock can be stopped, an interrupt cannot be generated, and a wake-up signal can be generated based on the configuration and external signals.

  If the debounce clock provided by the PRCM module is active, the debounce cell can sample and filter the input to generate a wake-up event. If the debounce clock is inactive, the debounce cell gates all input signals and thus cannot be used.
- Disabled mode: The module is not used. The internal clock paths are gated, and an interrupt or wake-up request cannot be generated.

Idle mode is configured within the module and activated on request by the host processor through sideband signals (see Section 25.4.5.2.3, *System Power Management and Wakeup*).

The disabled mode is set by software through a dedicated configuration bit, GPIOi.GPIO_CTRL[0] DISABLEMODULE (0: The module is enabled and clocks are not gated; 1: The module is disabled and clocks are gated). It unconditionally gates the internal clock paths that are not used for the system interface. When setting the GPIO_CTRL[0] DISABLEMODULE bit (enabling or disabling the GPIO module), it is important to switch the debouncing clock on or off in the following order:

- The GPIO optional debouncing clock must be enabled before the GPIO module is set (GPIO_CTRL[0]DISABLEMODULE = 0x0).
- The GPIO optional debouncing clock must be disabled after the GPIO module is disabled (GPIO_CTRL[0]DISABLEMODULE = 0x1).

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25.4.5.2.3 System Power Management and Wakeup

The PRCM module can require the GPIO modules to be idled for power-saving purposes.

The general-purpose interface has eight identical idle mode request/acknowledge (handshake) mechanisms with the PRCM module (see Section 25.4.6.2, *Wake-Up Requests Generation*): one per GPIO module. The general-purpose interface allows the GPIO modules to enter idle mode based on the GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE bit field.

Idle acknowledge depends on the configuration and activity of each GPIO module:

- Smart-idle mode

  When the GPIO module is configured in smart-idle mode, it checks for more activity (capture of the input GPIO pins in the GPIOi.GPIO_DATAIN register is complete with no pending interrupt; all interrupt status bits are cleared), and there is no write access to the GPIO.GPIO_DEBOUNCINGTIME register, which is waiting to be synchronized.

  Idle acknowledge is then asserted and the module enters into idle mode. It waits for active system clock gating by the PRCM module (when all peripherals supplied by the same L4 interface clock domain are also ready for idle).

  In idle mode (that is, when the PRCM module gates the interface clock), no interrupt occurs.

- Smart-idle wake-up mode

  If the GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE bit field selects smart-idle or smart-idle wake-up mode, the GPIO module evaluates its internal capability to have the interface clock switched off. Once all internal activity ceases (the DATA INPUT REGISTER completed to capture the input GPIO pins, there is no pending interrupt, all interrupt status bits are cleared, and there is no write access to the GPIO_DEBOUNCINGTIME register pending to be synchronized), the idle acknowledge is asserted and the GPIO enters into Idle mode, ready to issue a wake-up request when the expected transition occurs on an enabled GPIO input pin. This wake-up request is effectively sent only if the GPIOi.GPIO_SYSCONFIG[2] ENAWAKEUP bit of the system configuration register enables the GPIO wake-up capability (see). When the system is awake, the IDLE request goes inactive, the idle acknowledge and wake-up request (if the GPIO triggered the wake-up in the system) signals are immediately deasserted, and the asynchronous wake-up request (if it exists) is reflected into the synchronous interrupt status registers.

- Force-idle mode

  When the GPIO module is configured in force-idle mode (the GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE bit field = 0x0) and receives an IDLE request from the PRCM module, the GPIO module waits unconditionally for active system clock gating by the PRCM module. (This occurs only when all peripherals supplied by the same L4 interface clock domain are also ready for idle.)

  When in idle mode (that is, when the PRCM module gates the interface clock), the module (in inactive mode) has no activity, the interface clock paths are gated, an interrupt cannot be generated, and the wake-up feature is totally inhibited.

- No-idle mode

  When the GPIO module is configured in no-idle mode (the GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE bit field = 0x1) and receives an IDLE request from the PRCM module, the GPIO module does not go into idle mode and the idle acknowledge is never sent.

NOTE: For more information about the idle modes, see Section 3.1.1.2, *Power Management*, in Chapter 3, *Power, Reset, and Clock Management*.

25.4.5.2.4 Module Power Saving

The GPIO module has local power management by internal clock-gating features:

- Internal interface clock gating: The clock for the system interface logic can be gated when the module is not accessed, if the GPIOi.GPIO_SYSCONFIG[0] AUTOIDLE bit is set. Otherwise, this logic is free-running on the interface clock.
- Clock gating for the input data sample logic: Clock for the input data sample logic can be gated when the data in the GPIOi.GPIO_DATAIN register is not accessed.

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- Clock gating for the event detection logic: Each GPIO module implements four clock groups used for the logic in the synchronous event detection. Each group of eight input GPIO pins has a separate enable signal depending on the edge/level detection register setting (because the input is 32 bits, four groups of eight inputs are defined for each GPIO module). If a group requires no detection, the corresponding clock is gated off.

  All channels are also gated using a one-out-of-N scheme. N is the GPIOi.GPIO_CTRL[2:1] GATINGRATIO bit field and can take the values 1, 2, 4, and 8. The interface clock is enabled for this logic one cycle every N cycles. When N is 1, there is no gating and this logic is free-running on the interface clock. When N is 2, 4, or 8, this logic runs at the equivalent frequency of interface clock frequency divided by N.
- Inactive mode: In inactive mode, all internal clock paths are gated.
- Disabled mode: All internal clock paths not used for the L4 interconnect are gated. The GPIOi.GPIO_CTRL[0] DISABLEMODULE bit controls a clock-gating feature at the module level. Setting this bit to 1 forces clock gating for all internal clock paths. Module internal activity is suspended. The L4 interconnect is not affected by this bit.

The interface clock gating is controlled with the GPIOi.GPIO_SYSCONFIG[0] AUTOIDLE bit, which is used to save power when the module is not used because of the multiplexing configuration selected at the chip level. This bit has precedence over all other internal configuration bits.

Table 25-6 describes the power-management features available for the general-purpose interface module.

NOTE: For information about source clock gating and sleep/wake-up transitions, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

For descriptions of the EnaWakeUp, IdleMode, ClockActivity, and StandbyMode features, see Section 3.1.1.1.2, *Module-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 25-6. Local Power-Management Features

Feature	Register Bits/Bit Fields	Description
Clock autogating	GPIOi.GPIO_SYSCONFIG[0] AUTOIDLE	It sets the clock-gating strategy for the OCP interface block.
Slave-idle modes	GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE	Force-idle, no-idle, and smart-idle wake-up-capable modes are available.
Clock activity	GPIOi.GPIO_CTRL[0] DISABLEMODULE	Enable and disable the module.
Debouncing enable	GPIOi.GPIO_DEBOUNCENABLE[31:0] DEBOUNCEENABLE	Debouncing mode is available.
Global wake-up enable	GPIOi.GPIO_SYSCONFIG[2] ENAWAKEUP	This bit enables the wake-up feature at the module level.
Wake-up sources enable	GPIOi.GPIO_IRQWAKEN_0[31:0] INTLINE GPIOi.GPIO_IRQWAKEN_1[31:0] INTLINE	This register enables or disables a specific IRQ request source to generate a wake-up signal.

Table 25-7 describes the clock activity settings.

Table 25-7. Clock Activity Settings

GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE	Selected Mode	Description	Wake-Up Events
00	Force-idle	The GPIO module goes into inactive mode independently of the internal module state, and the IDLE acknowledge is never sent.	No
01	No-idle	The GPIO module does not go into Idle mode and the IDLE acknowledge is never sent.	No

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Table 25-7. Clock Activity Settings (continued)

GPIOi.GPIO_SYSCONFIG[4:3] IDLEMODE	Selected Mode	Description	Wake-Up Events
10	Smart-idle	The GPIO module evaluates its internal capability to have the interface clock switched off. If there is no more internal activity, the IDLE acknowledge is asserted and the GPIO enters idle mode.	No
11	Smart-idle wake-up	The GPIO module evaluates its internal capability to have the interface clock switched off. If there is no more internal activity, the IDLE acknowledge is asserted and the GPIO enters idle mode.	Yes

25.4.6 General-Purpose Interface Interrupt and Wake-Up Requests

25.4.6.1 Interrupt Requests Generation

All interrupt sources (the 32 GPIO input channels) are merged to issue two synchronous interrupt requests in each GPIO module. Thus, the general-purpose interface has 16 interrupt lines (two interrupt lines per GPIO module instance).

- Synchronous interrupt request line 1 is mapped on the MPU and IPU INTCs.
- Synchronous interrupt request line 2 is mapped on the DSP INTC.

Table 25-8 lists the event flags, and their mask, that can cause module interrupts.

Table 25-8. Events

Event Flag	Event Mask	Synchronous	Sensitivity	Map to	Description
GPIOi.GPIO_IRQSTATUS_0 [31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_SET_0[31:0] INTLINE	Yes	Edge/ level	MPU_IRQ_n IPU_IRQ_n(1)	Corresponding to the first line of interrupt
GPIOi.GPIO_IRQSTATUS_1 [31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_SET_1[31:0] INTLINE	Yes	Edge/ level	DSP_IRQ_n(2)	Corresponding to the second line of interrupt
GPIOi.GPIO_IRQSTATUS_0 [31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_SET_0[31:0] INTLINE	Yes	Edge/ level	MPU_IRQ_n IPU_IRQ_n(1)	Corresponding to the first line of interrupt
GPIOi.GPIO_IRQSTATUS_1 [31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_SET_1[31:0] INTLINE	Yes	Edge/ level	DSP_IRQ_n(2)	Corresponding to the second line of interrupt
GPIOi.GPIO_IRQSTATUS_0 [31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_CLR_0[31:0] INTLINE	Yes	Edge/ level	MPU_IRQ_n IPU_IRQ_n(1)	Corresponding to the first line of interrupt
GPIOi.GPIO_IRQSTATUS_1 [31:0] INTLINE	GPIOi.GPIO_IRQSTATUS_CLR_1[31:0] INTLINE	Yes	Edge/ level	DSP_IRQ_n(2)	Corresponding to the second line of interrupt
GPIOi.GPIO_IRQSTATUS_0 [31:0] INTLINE	GPIOi.GPIO_IRQWAKEN_0 [31:0] INTLINE	No	Edge/ level	MPU_IRQ_n IPU_IRQ_n(1)	Corresponding to the first line of interrupt
GPIOi.GPIO_IRQSTATUS_1 [31:0] INTLINE	GPIOi.GPIO_IRQWAKEN_1 [31:0] INTLINE	No	Edge/ level	DSP_IRQ_n(2)	Corresponding to the second line of interrupt

(1) For GPIO1 and GPIO2 only
(2) For GPIO1 to GPIO6 only

Synchronous interrupt request line 1 and line 2 are active depending on their respective interrupt-enable1 and enable 2 registers (GPIOi.GPIO_IRQSTATUS_SET_0, GPIOi.GPIO_IRQSTATUS_SET_1, GPIOi.GPIO_IRQSTATUS_CLR_0, and GPIOi.GPIO_IRQSTATUS_CLR_1).

- interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_SET_0 and GPIOi.GPIO_IRQSTATUS_SET_1)

  The interrupt enable1 (or interrupt enable2) register allows masking of the expected transition on input

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GPIO to prevent the generation of an interrupt request on line 1 (or line 2). The interrupt-enable registers are programmed synchronously with the interface clock.

These registers can be accessed with direct read/write operations or by using the alternate set-and-clear protocol feature for register update. This feature allows setting or clearing explicit bits of these registers with a single write access (see Section 25.4.9, *General-Purpose Interface Set-and-Clear Protocol*).

- Interrupt status registers (GPIOi.GPIO_IRQSTATUS_0 and GPIOi.GPIO_IRQSTATUS_1)

  The interrupt status 1 (or interrupt status 2) register determines which of the input GPIO pins triggered the interrupt line1 (or interrupt line 2) request (or the wake-up line).

  When a bit in this register is set to 1, it indicates that the corresponding GPIO pin is requesting the interrupt (or the wakeup). To reset a bit in this register, set the appropriate bit to 1. However, an interrupt cannot be generated by writing 1 to the interrupt status 1 (or interrupt status 2) register.

  If 0 is written to a bit in this register, the value in the corresponding bit in the interrupt status 1 and remains unchanged. The interrupt status 1 (or interrupt status 2) register is synchronous with the interface clock. In idle mode, the event is detected through an asynchronous path, and interrupt status 2 registers are set when the GPIO module is awaken.

CAUTION

After servicing the interrupt, the status bit in the interrupt status register (GPIOi.GPIO_IRQSTATUS_0 or GPIOi.GPIO_IRQSTATUS_1) must be reset and the interrupt line released (by setting the corresponding bit of the interrupt status register to 1).

Before enabling an interrupt for the GPIO channel in the interrupt-enable register (GPIOi.GPIO_IRQSTATUS_SET_0 or GPIOi.GPIO_IRQSTATUS_SET_1) the corresponding status bit in the interrupt status register (GPIOi.GPIO_IRQSTATUS_0 or GPIOi.GPIO_IRQSTATUS_1) must be reset to prevent the occurrence of unexpected interrupts when enabling an interrupt for the GPIO channel.

25.4.6.2 Wake-Up Requests Generation

The GPIO1 module of the general-purpose interface is attached to the WKUPAON power domain (see Section 3.1.1.2, *Power Management*, in Chapter 3, *Power, Reset, and Clock Management*, and can wake up the system.

NOTE: The GPIO2 to GPIO8 modules belong to the L4PER power domain and thus their wake-up capabilities are operational only when the L4PER power domain is active.

All wake-up sources (the 32 input GPIO channels) are merged together to issue a single asynchronous wake-up request in each GPIO module following the expected transition(s) (based on register programming). Each GPIO module generates a wake-up signal to the PRCM module.

NOTE: Only gpio_wkx[10:0] and gpio_wkx[31:29] can be used to generate a direct wake-up event.

The asynchronous wake-up request line is active based on the GPIOi.GPIO_IRQWAKEN_0 and GPIO_IRQWAKEN_1 wake-up-enable registers (where i = 1 to 8).

The wake-up-enable register allows masking of the expected transition on input GPIO to prevent the generation of a wake-up request. The wake-up-enable register is programmed synchronously with the interface clock before any idle mode request coming from the host processor.

This register can be accessed with direct read/write operations.

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NOTE: There must be a correlation between the wake-up enable and interrupt-enable registers. If a GPIO pin has a wake-up configured on it, it must also have the corresponding interrupt enabled (on one of the two interrupt lines). Otherwise, it is possible to have a wake-up event, but after exiting the IDLE state, no interrupt is generated; thus, the corresponding bit from the interrupt status register is not cleared, and the module does not acknowledge a future IDLE request.

Table 25-9 lists the mapping of the wake-up signals.

Table 25-9. Wake-Up Signals

Name	Mapping	Comments
GPIOi_WAKE	GPIOi_SWAKEUP	Where i = 1 to 8. The destination is the PRCM module.

25.4.7 General-Purpose Interface Channels Description

Table 25-10 describes the GPIO channels.

Table 25-10. GPIO Channels Description

Channel Number	Type [1]	Mapping	Wake-Up Feature	Comments
GPIO1 Module				
[5:0]	O	gpio1_wkout[5:0]	Yes	Wake-up path
[31:6]	I/O	gpio1_wk[31:6]	Yes	Wake-up path
GPIO2 Module				
[31:0]	I/O	gpio2_[63:32]	Yes [2]	GPIO
GPIO3 Module				
[21:0]	I/O	gpio3_[85:64]	Yes [2]	GPIO
[22] [3]	I/O	gpio3_86	Yes [2]	GPIO
	I	thermal shutdown comparator output signal (TSHUT)	Yes [2]	Bandgap internal TSHUT
[31:23]	I/O	gpio3_[95:87]	Yes [2]	GPIO
GPIO4 Module				
[31:0]	I/O	gpio4_[127:96]	Yes [2]	GPIO
GPIO5 Module				
[28:0]	I/O	gpio5_[156:128]	Yes [2]	GPIO
[29] [3]	I	gpio5_in157	Yes [2]	GPIO (inputs only)
	I	CHGDETECT	Yes [2]	USB charge detect
[31:30]	I/O	gpio5_[159:158]	Yes [2]	GPIO
GPIO6 Module				
[31:0]	I/O	gpio6_[191:160]	Yes [2]	GPIO
GPIO7 Module				

(1) I = Input; O = Output; I/O = bidirectional

(2) Only when the L4_PER power domain is active

(3) The GPIO channel provides additional internal functionality (see the Comments column), besides its general-purpose I/O capabilities, when it is not connected to a pad of the device. For more information about pad configuration and multiplexing, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*.

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Table 25-10. GPIO Channels Description (continued)

Channel Number	Type [1]	Mapping	Wake-Up Feature	Comments
[31:0]	I/O	gpio7_[223:192]	Yes [2]	GPIO
GPIO8 Module				
[11:0]	I/O	gpio8_[235:224]	Yes [2]	GPIO
[31:12]	I	gpio8_in[255:236]		GPIO (inputs only)

NOTE: TSHUT is an output from the bandgap module. This signal is high during normal operation and goes low during a thermal shutdown event. When channel 22 of GPIO3 is not connected to a ball of the device (the corresponding pin is configured in a mode different from configuration mode 4; see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*, for more information about pin configuration), TSHUT is connected to channel 22 of GPIO3. The channel must be configured correctly so that it can generate an interrupt when a high-to-low transition occurs on TSHUT.

NOTE: Channel 29 in GPIO5 is internally connected inside the device to the charger detection (CHGDETECT) output of the USB OTG PHY module. This allows interrupt generation on the corresponding GPIO channel, if the mentioned event occurs.

NOTE: For more information about pin configuration, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*.

25.4.8 General-Purpose Interface Data Input/Output Capabilities

The output-enable register (GPIOi.GPIO_OE) controls the I/O capability of each pin. At reset, all the GPIO-related pins are configured as inputs, and their output capabilities are disabled. This register is not used within the module. Its only function is to carry the pad configuration.

When configured as an output (the desired bit reset in the GPIOi.GPIO_OE register), the value of the corresponding bit in the GPIOi.GPIO_DATAOUT register is driven on the corresponding GPIO pin. Data is written to the data-output register synchronously with the interface clock. This register can be accessed with read/write operations or by using the alternate set-and-clear protocol register update feature. This feature gives the possibility to set or clear specific bits of this register with a single write access to the set output data register (GPIOi.GPIO_SETDATAOUT) or to the clear output data register (GPIOi.GPIO_CLEARDATAOUT) address (see Section 25.4.9, *General-Purpose Interface Set-and-Clear Protocol*). If the application uses a pin as an output and does not want interrupt/wake-up generation from this pin, the application must properly configure the wake-up enable (GPIOi.GPIO_ WAKEUPENABLE) and the interrupt-enable (GPIOi.GPIO_IRQSTATUS_SET_0 and GPIOi.GPIO_IRQSTATUS_SET_1) registers.

When configured as an input (the desired bit is set to 1 in the GPIOi.GPIO_OE register), the state of the input can be read from the corresponding bit in the GPIOi.GPIO_DATAIN register. The input data is sampled synchronously with the interface clock and then captured in the data input register synchronously with the interface clock. When the GPIO pin levels change, they are captured into this register after two interface clock cycles (the required cycles to synchronize and write data). If the application uses a pin as an input, the application must properly configure the wake-up enable (GPIOi.GPIO_IRQWAKEN_0 and GPIOi.GPIO_IRQWAKEN_1) and the interrupt-enable (GPIOi.GPIO_IRQSTATUS_SET_0 and GPIOi.GPIO_IRQSTATUS_SET_0) registers to the interrupt and wake-up feature as needed. For using the alternate set-and-clear protocol, see Section 25.4.9, *General-Purpose Interface Set-and-Clear Protocol.*

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25.4.9 General-Purpose Interface Set-and-Clear Protocol

25.4.9.1 Description

The GPIO module implements the set-and-clear protocol register update for the following registers:

- GPIOi.GPIO_DATAOUT
- GPIOi.GPIO_IRQSTATUS_CLR_0
- GPIOi.GPIO_IRQSTATUS_CLR_1
- GPIOi.GPIO_IRQSTATUS_SET_0
- GPIOi.GPIO_IRQSTATUS_SET_1

This protocol is an alternative to the atomic test and set operations and consists of writing operations at dedicated addresses (one address for setting bit[s] and one address for clearing bit[s]). The data to write is 1 at bit position(s) to clear (or to set) and 0 at unaffected bit(s). Registers can be accessed in two ways:

- Standard: Full register read and write operations at the primary register address
- Set and clear: Separate addresses are provided to set (and clear) bits in registers. Writing 1 at these addresses sets (or clears) the corresponding bit into the equivalent register; writing 0 has no effect.

Therefore, for these registers, three addresses are defined for one unique physical register. Reading these addresses has the same effect and returns the register value.

25.4.9.2 Clear Instruction

25.4.9.2.1 Clear Register Addresses

- Clear interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_CLR_0 and GPIOi.GPIO_IRQSTATUS_CLR_1).

  A write operation in the GPIO_IRQSTATUS_CLR_0 (or GPIO_IRQSTATUS_CLR_1) register clears the corresponding bit in the same register when the written bit is 1; a written bit at 0 has no effect.

  A read of the clear interrupt enable0 (or enable1) register returns the value of the GPIO_IRQSTATUS_CLR_0 (or GPIO_IRQSTATUS_CLR_1) register.
- Clear data-output register (GPIOi.GPIO_CLEARDATAOUT).

  A write operation in the clear data-output register clears the corresponding bit in the data-output register when the written bit is 1; a written bit at 0 has no effect.

  A read of the clear data-output register returns the value of the data-output register.

25.4.9.2.2 Clear Instruction Example

Assume the data-output register (or one of the interrupt or wake-up-enable registers) contains the binary value 0b0000 0001 0000 0001 and bit 0 is to be cleared.

With the clear instruction feature, write 0b0000 0000 0000 0001 at the address of the clear data-output register (or at the address of the clear interrupt or wake-up-enable register). After this write operation, a reading of the data-output register (or the interrupt or wake-up-enable register) returns 0b0000 0001 0000 0000; bit 0 is cleared.

NOTE: Although the general-purpose interface registers are 32 bits wide, only the 16 least-significant bits (LSBs) are represented in this example.

Figure 25-13 is an example of a clear instruction.

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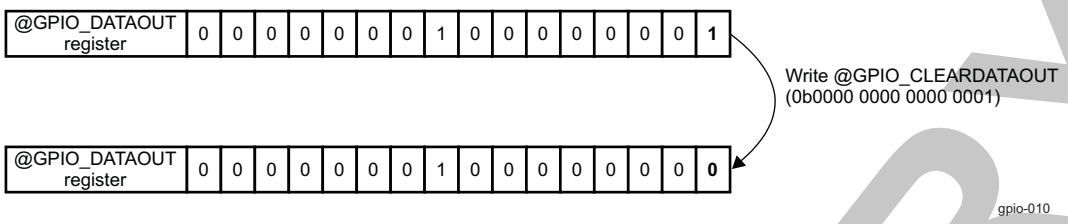
Figure 25-13. GPIO_CLEARDATAOUT Register Example



25.4.9.3 Set Instruction

25.4.9.3.1 Set Register Addresses

- Set interrupt-enable registers (GPIOi.GPIO_IRQSTATUS_SET_0 and GPIOi.GPIO_IRQSTATUS_SET_1).

  A write operation in the GPIOi.GPIO_IRQSTATUS_SET_0 (or GPIOi.GPIO_IRQSTATUS_SET_1) register sets the corresponding bit in the same register when the written bit is 1; a written bit at 0 has no effect.

  A read of the set interrupt-enable 0 (or enable1) register returns the value of the interrupt GPIOi.GPIO_IRQSTATUS_SET_0 (or GPIOi.GPIO_IRQSTATUS_SET_1) register.

- Set data-output register (GPIOi.GPIO_SETDATAOUT).

  A write operation in the set data-output register sets the corresponding bit in the data-output register when the written bit is 1; a written bit at 0 has no effect.

  A read of the set data-output register returns the value of the data-output register.

25.4.9.3.2 Set Instruction Example

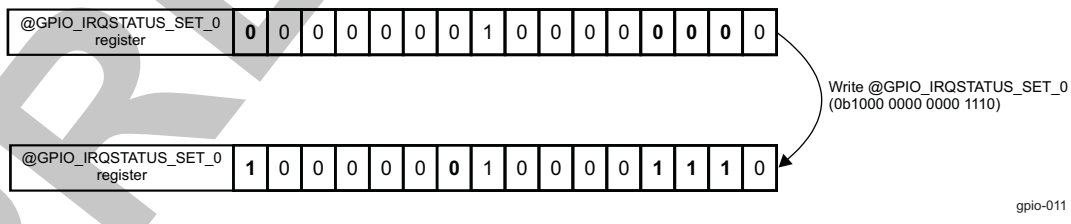
Assume the interrupt enable1 (or enable2) register (or the data-output register) contains the binary value 0b0000 0001 0000 0000 and bits 15, 3, 2, and 1 are to be set.

With the set instruction feature, the user has only to write 0b1000 0000 0000 1110 at the address of the GPIO_SETDATAOUT register. After this write operation, a reading of the GPIO_SETDATAOUT register returns 0b1000 0001 0000 1110: bits 15, 3, 2, and 1 have been set.

NOTE: Although the general-purpose interface registers are 32 bits wide, only the 16 LSBs are represented in this example.

Figure 25-14 is an example of a set instruction.

Figure 25-14. Write in GPIO_IRQSTATUS_SET_0 Register Example



The set wake-up-enable register offers the same feature with the wake-up-enable register.

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25.5 General-Purpose Interface Programming Guide

25.5.1 General-Purpose Interface Low-Level Programming Models

25.5.1.1 Global Initialization

25.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the general-purpose interface module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the environment and integration of the general-purpose interface. For more information, see Section 25.2, *General-Purpose Interface Environment*, and Section 25.3, *General-Purpose Interface Integration*.

Table 25-11. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	Module interface and functional clocks must be enabled. For more information about the module configuration, see Section 3.1.1.1, *Clock Management*, in Chapter 3 *Power, Reset, and Clock Management*.
Control module	Module specific pad muxing must be set in the control module. For more information about the module configuration, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18 *Control Module*.
MPU INTC	MPU INTC configuration must be done to enable the interrupts from the general-purpose interface module. See Section 17.4.1, *INTC_MPU Functional Description*, in Chapter 17, *Interrupt Controllers* .
DSP INTC	DSP INTC configuration must be done to enable the interrupts from the general-purpose interface module. See Section 5.3.2.6, *DSP INTC* , in Chapter 5, *DSP Subsystem*.

25.5.1.1.2 General-Purpose Interface Module Global Initialization

This procedure initializes the general-purpose Interface module after a power-on reset (POR) or software reset.

Table 25-12. General-Purpose Interface Global Initialization

Step	Register/Bit Field/Programming Model	Value
Execute software reset.	GPIO_SYSCONFIG[1] SOFTRESET	0x1
Wait until reset completed?	GPIO_SYSSTATUS[0] RESETDONE	= 0x1
Configure idle mode.	GPIO_SYSCONFIG[4:3] IDLEMODE	xx
Configure interface clock gating.	GPIO_SYSCONFIG[0] AUTOIDLE	x
Set clock-gating power saving.	GPIO_LEVELDETECT0[31:0] LEVELDETECT0 and GPIO_LEVELDETECT1[31:0} LEVELDETECT1 and GPIO_RISINGDETECT[31:0] RISINGDETECT and GPIO_FALLINGDETECT[31:0] FALLINGDETECT	0x0000 00FF
Set clock-gating ratio.	GPIO_CTRL [2:1] GATINGRATIO	xx
Configure GPIO channels as input or output.	GPIO_OE[31:0] OUTPUTEN	xxx
Set debounce time value.	GPIO_DEBOUNCINGTIME[7:0] DEBOUNCINGTIME	xxx
Enable/disable debouncing for desired input line.	GPIO_DEBOUNCENABLE[31:0] DEBOUNCENABLE	xxx
Interrupt and wake-up requests configuration		

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Table 25-12. General-Purpose Interface Global Initialization (continued)

Step	Register/Bit Field/Programming Model	Value
Configure detection events.	GPIO_LEVELDETECT0[31:0] LEVELDETECT0 and/or GPIO_LEVELDETECT1[31:0] LEVELDETECT1 and/or GPIO_RISINGDETECT[31:0] RISINGDETECT and/or GPIO_FALLINGDETECT[31:0] FALLINGDETECT	0x1
Enable/disable interrupts.	GPIO_IRQSTATUS_SET_0[31:0] INTLINE and/or GPIO_IRQSTATUS_SET_1[31:0] INTLINE	xxx
Enable/disable wake-up for GPIO channels.	GPIO_IRQWAKEN_0[31:0] INTLINE and/or GPIO_IRQWAKEN_1[31:0] INTLINE	xxx
Enable/disable wake-up generation.	GPIO_SYSCONFIG[2] ENAWAKEUP	0x1

25.5.1.2 General-Purpose Interface Operational Modes Configuration

25.5.1.2.1 General-Purpose Interface Read Input Register

Table 25-13. General-Purpose Interface Read Input Register

Step	Register/Bit Field/Programming Model	Value
Read input register value.	GPIO_DATAIN[31:0] DATAIN	xxxx

25.5.1.2.2 General-Purpose Interface Write Output Register

Table 25-14. General-Purpose Interface Write Output Register

Step	Register/Bit Field/Programming Model	Value
Write value to output register.	GPIO_DATAOUT[31:0] DATAOUT	xxx

25.5.1.2.3 General-Purpose Interface Set Bit Function

Table 25-15. General-Purpose Interface Set Bit Function

Step	Register/Bit Field/Programming Model	Value
Write 0x1 to set desired bit(s) in register.	GPIO_SETDATAOUT [31:0] INTLINE GPIO_IRQSTATUS_SET_0 [31:0] INTLINE GPIO_IRQSTATUS_SET_1 [31:0] INTLINE	0x-

25.5.1.2.4 General-Purpose Interface Clear Bit Function

Table 25-16. General-Purpose Interface Clear Bit Function

Step	Register/Bit Field/Programming Model	Value
Write 0x1 to clear desired bit(s) in register.	GPIO_CLEARDATAOUT [31:0] INTLINE GPIO_IRQSTATUS_CLR_0 [31:0] INTLINE GPIO_IRQSTATUS_CLR_1 [31:0] INTLINE	0x1

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25.6 General-Purpose Interface Register Manual

25.6.1 General-Purpose Interface Instance Summary

Table 25-17 summarizes the general-purpose interface instance.

Table 25-17. Instance Summary

Module Name	Base Address	Size
GPIO1	0x4AE1 0000	4 KiB
GPIO2	0x4805 5000	4 KiB
GPIO3	0x4805 7000	4 KiB
GPIO4	0x4805 9000	4 KiB
GPIO5	0x4805 B000	4 KiB
GPIO6	0x4805 D000	4 KiB
GPIO7	0x4805 1000	4 KiB
GPIO8	0x4805 3000	4 KiB

25.6.2 General-Purpose Interface Registers

25.6.2.1 General-Purpose Interface Register Summary

Table 25-18 summarizes the general-purpose interface GPIO1 to GPIO3 registers.

Table 25-18. General-Purpose Interface GPIO1 to GPIO3 Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPIO1 L4 Physical Address	GPIO2 L4 Physical Address	GPIO3 L4 Physical Address
GPIO_REVISION	R	32	0x0000 0000	0x4AE1 0000	0x4805 5000	0x4805 7000
GPIO_SYSCONFIG	RW	32	0x0000 0010	0x4AE1 0010	0x4805 5010	0x4805 7010
RESERVED			0x0000 0020	0x4AE1 0020	0x4805 5020	0x4805 7020
GPIO_IRQSTATUS_RAW_0	RW	32	0x0000 0024	0x4AE1 0024	0x4805 5024	0x4805 7024
GPIO_IRQSTATUS_RAW_1	RW	32	0x0000 0028	0x4AE1 0028	0x4805 5028	0x4805 7028
GPIO_IRQSTATUS_0	RW	32	0x0000 002C	0x4AE1 002C	0x4805 502C	0x4805 702C
GPIO_IRQSTATUS_1	RW	32	0x0000 0030	0x4AE1 0030	0x4805 5030	0x4805 7030
GPIO_IRQSTATUS_SET_0	RW	32	0x0000 0034	0x4AE1 0034	0x4805 5034	0x4805 7034
GPIO_IRQSTATUS_SET_1	RW	32	0x0000 0038	0x4AE1 0038	0x4805 5038	0x4805 7038
GPIO_IRQSTATUS_CLR_0	RW	32	0x0000 003C	0x4AE1 003C	0x4805 503C	0x4805 703C
GPIO_IRQSTATUS_CLR_1	RW	32	0x0000 0040	0x4AE1 0040	0x4805 5040	0x4805 7040
GPIO_IRQWAKEN_0	RW	32	0x0000 0044	0x4AE1 0044	0x4805 5044	0x4805 7044
GPIO_IRQWAKEN_1	RW	32	0x0000 0048	0x4AE1 0048	0x4805 5048	0x4805 7048
GPIO_SYSSTATUS	R	32	0x0000 0114	0x4AE1 0114	0x4805 5114	0x4805 7114
RESERVED		32	0x0000 0118	0x4AE1 0118	0x4805 5118	0x4805 7118
RESERVED		32	0x0000 011C	0x4AE1 011C	0x4805 511C	0x4805 711C
RESERVED		32	0x0000 0120	0x4AE1 0120	0x4805 5120	0x4805 7120
RESERVED		32	0x0000 0128	0x4AE1 0128	0x4805 5128	0x4805 7128
RESERVED		32	0x0000 012C	0x4AE1 012C	0x4805 512C	0x4805 712C
GPIO_CTRL	RW	32	0x0000 0130	0x4AE1 0130	0x4805 5130	0x4805 7130
GPIO_OE	RW	32	0x0000 0134	0x4AE1 0134	0x4805 5134	0x4805 7134
GPIO_DATAIN	R	32	0x0000 0138	0x4AE1 0138	0x4805 5138	0x4805 7138
GPIO_DATAOUT	RW	32	0x0000 013C	0x4AE1 013C	0x4805 513C	0x4805 713C
GPIO_LEVELDETECT0	RW	32	0x0000 0140	0x4AE1 0140	0x4805 5140	0x4805 7140

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Table 25-18. General-Purpose Interface GPIO1 to GPIO3 Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	GPIO1 L4 Physical Address	GPIO2 L4 Physical Address	GPIO3 L4 Physical Address
GPIO_LEVELDETECT1	RW	32	0x0000 0144	0x4AE1 0144	0x4805 5144	0x4805 7144
GPIO_RISINGDETECT	RW	32	0x0000 0148	0x4AE1 0148	0x4805 5148	0x4805 7148
GPIO_FALLINGDETECT	RW	32	0x0000 014C	0x4AE1 014C	0x4805 514C	0x4805 714C
GPIO_DEBOUNCENABLE	RW	32	0x0000 0150	0x4AE1 0150	0x4805 5150	0x4805 7150
GPIO_DEBOUNCINGTIME	RW	32	0x0000 0154	0x4AE1 0154	0x4805 5154	0x4805 7154
RESERVED		32	0x0000 0160	0x4AE1 0160	0x4805 5160	0x4805 7160
RESERVED		32	0x0000 0164	0x4AE1 0164	0x4805 5164	0x4805 7164
RESERVED		32	0x0000 0170	0x4AE1 0170	0x4805 5170	0x4805 7170
RESERVED		32	0x0000 0174	0x4AE1 0174	0x4805 5174	0x4805 7174
RESERVED		32	0x0000 0180	0x4AE1 0180	0x4805 5180	0x4805 7180
RESERVED		32	0x0000 0184	0x4AE1 0184	0x4805 5184	0x4805 7184
GPIO_CLEARDATAOUT	RW	32	0x0000 0190	0x4AE1 0190	0x4805 5190	0x4805 7190
GPIO_SETDATAOUT	RW	32	0x0000 0194	0x4AE1 0194	0x4805 5194	0x4805 7194

Table 25-19 summarizes the general-purpose interface GPIO4 to GPIO6 registers.

Table 25-19. General-Purpose Interface GPIO4 to GPIO6 Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPIO4 L4 Physical Address	GPIO5 L4 Physical Address	GPIO6 L4 Physical Address
GPIO_REVISION	R	32	0x0000 0000	0x4805 9000	0x4805 B000	0x4805 D000
GPIO_SYSCONFIG	RW	32	0x0000 0010	0x4805 9010	0x4805 B010	0x4805 D010
RESERVED			0x0000 0020	0x4805 9020	0x4805 B020	0x4805 D020
GPIO_IRQSTATUS_RAW_0	RW	32	0x0000 0024	0x4805 9024	0x4805 B024	0x4805 D024
GPIO_IRQSTATUS_RAW_1	RW	32	0x0000 0028	0x4805 9028	0x4805 B028	0x4805 D028
GPIO_IRQSTATUS_0	RW	32	0x0000 002C	0x4805 902C	0x4805 B02C	0x4805 D02C
GPIO_IRQSTATUS_1	RW	32	0x0000 0030	0x4805 9030	0x4805 B030	0x4805 D030
GPIO_IRQSTATUS_SET_0	RW	32	0x0000 0034	0x4805 9034	0x4805 B034	0x4805 D034
GPIO_IRQSTATUS_SET_1	RW	32	0x0000 0038	0x4805 9038	0x4805 B038	0x4805 D038
GPIO_IRQSTATUS_CLR_0	RW	32	0x0000 003C	0x4805 903C	0x4805 B03C	0x4805 D03C
GPIO_IRQSTATUS_CLR_1	RW	32	0x0000 0040	0x4805 9040	0x4805 B040	0x4805 D040
GPIO_IRQWAKEN_0	RW	32	0x0000 0044	0x4805 9044	0x4805 B044	0x4805 D044
GPIO_IRQWAKEN_1	RW	32	0x0000 0048	0x4805 9048	0x4805 B048	0x4805 D048
GPIO_SYSSTATUS	R	32	0x0000 0114	0x4805 9114	0x4805 B114	0x4805 D114
RESERVED		32	0x0000 0118	0x4805 9118	0x4805 B118	0x4805 D118
RESERVED		32	0x0000 011C	0x4805 911C	0x4805 B11C	0x4805 D11C
RESERVED		32	0x0000 0120	0x4805 9120	0x4805 B120	0x4805 D120
RESERVED		32	0x0000 0128	0x4805 9128	0x4805 B128	0x4805 D128
RESERVED		32	0x0000 012C	0x4805 912C	0x4805 B12C	0x4805 D12C
GPIO_CTRL	RW	32	0x0000 0130	0x4805 9130	0x4805 B130	0x4805 D130
GPIO_OE	RW	32	0x0000 0134	0x4805 9134	0x4805 B134	0x4805 D134
GPIO_DATAIN	R	32	0x0000 0138	0x4805 9138	0x4805 B138	0x4805 D138
GPIO_DATAOUT	RW	32	0x0000 013C	0x4805 913C	0x4805 B13C	0x4805 D13C
GPIO_LEVELDETECT0	RW	32	0x0000 0140	0x4805 9140	0x4805 B140	0x4805 D140
GPIO_LEVELDETECT1	RW	32	0x0000 0144	0x4805 9144	0x4805 B144	0x4805 D144
GPIO_RISINGDETECT	RW	32	0x0000 0148	0x4805 9148	0x4805 B148	0x4805 D148

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Table 25-19. General-Purpose Interface GPIO4 to GPIO6 Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	GPIO4 L4 Physical Address	GPIO5 L4 Physical Address	GPIO6 L4 Physical Address
GPIO_FALLINGDETECT	RW	32	0x0000 014C	0x4805 914C	0x4805 B14C	0x4805 D14C
GPIO_DEBOUNCENABLE	RW	32	0x0000 0150	0x4805 9150	0x4805 B150	0x4805 D150
GPIO_DEBOUNCINGTIME	RW	32	0x0000 0154	0x4805 9154	0x4805 B154	0x4805 D154
RESERVED		32	0x0000 0160	0x4805 9160	0x4805 B160	0x4805 D160
RESERVED		32	0x0000 0164	0x4805 9164	0x4805 B164	0x4805 D164
RESERVED		32	0x0000 0170	0x4805 9170	0x4805 B170	0x4805 D170
RESERVED		32	0x0000 0174	0x4805 9174	0x4805 B174	0x4805 D174
RESERVED		32	0x0000 0180	0x4805 9180	0x4805 B180	0x4805 D180
RESERVED		32	0x0000 0184	0x4805 9184	0x4805 B184	0x4805 D184
GPIO_CLEARDATAOUT	RW	32	0x0000 0190	0x4805 9190	0x4805 B190	0x4805 D190
GPIO_SETDATAOUT	RW	32	0x0000 0194	0x4805 9194	0x4805 B194	0x4805 D194

Table 25-20 summarizes the general-purpose interface GPIO7 and GPIO8 registers.

Table 25-20. General-Purpose Interface GPIO7 and GPIO8 Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	GPIO7 L4 Physical Address	GPIO8 L4 Physical Address
GPIO_REVISION	R	32	0x0000 0000	0x4805 1000	0x4805 3000
GPIO_SYSCONFIG	RW	32	0x0000 0010	0x4805 1010	0x4805 3010
RESERVED			0x0000 0020	0x4805 1020	0x4805 3020
GPIO_IRQSTATUS_RAW_0	RW	32	0x0000 0024	0x4805 1024	0x4805 3024
GPIO_IRQSTATUS_RAW_1	RW	32	0x0000 0028	0x4805 1028	0x4805 3028
GPIO_IRQSTATUS_0	RW	32	0x0000 002C	0x4805 102C	0x4805 302C
GPIO_IRQSTATUS_1	RW	32	0x0000 0030	0x4805 1030	0x4805 3030
GPIO_IRQSTATUS_SET_0	RW	32	0x0000 0034	0x4805 1034	0x4805 3034
GPIO_IRQSTATUS_SET_1	RW	32	0x0000 0038	0x4805 1038	0x4805 3038
GPIO_IRQSTATUS_CLR_0	RW	32	0x0000 003C	0x4805 103C	0x4805 303C
GPIO_IRQSTATUS_CLR_1	RW	32	0x0000 0040	0x4805 1040	0x4805 3040
GPIO_IRQWAKEN_0	RW	32	0x0000 0044	0x4805 1044	0x4805 3044
GPIO_IRQWAKEN_1	RW	32	0x0000 0048	0x4805 1048	0x4805 3048
GPIO_SYSSTATUS	R	32	0x0000 0114	0x4805 1114	0x4805 3114
RESERVED		32	0x0000 0118	0x4805 1118	0x4805 3118
RESERVED		32	0x0000 011C	0x4805 111C	0x4805 311C
RESERVED		32	0x0000 0120	0x4805 1120	0x4805 3120
RESERVED		32	0x0000 0128	0x4805 1128	0x4805 3128
RESERVED		32	0x0000 012C	0x4805 112C	0x4805 312C
GPIO_CTRL	RW	32	0x0000 0130	0x4805 1130	0x4805 3130
GPIO_OE	RW	32	0x0000 0134	0x4805 1134	0x4805 3134
GPIO_DATAIN	R	32	0x0000 0138	0x4805 1138	0x4805 3138
GPIO_DATAOUT	RW	32	0x0000 013C	0x4805 113C	0x4805 313C
GPIO_LEVELDETECT0	RW	32	0x0000 0140	0x4805 1140	0x4805 3140
GPIO_LEVELDETECT1	RW	32	0x0000 0144	0x4805 1144	0x4805 3144
GPIO_RISINGDETECT	RW	32	0x0000 0148	0x4805 1148	0x4805 3148
GPIO_FALLINGDETECT	RW	32	0x0000 014C	0x4805 114C	0x4805 314C
GPIO_DEBOUNCENABLE	RW	32	0x0000 0150	0x4805 1150	0x4805 3150
GPIO_DEBOUNCINGTIME	RW	32	0x0000 0154	0x4805 1154	0x4805 3154

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Table 25-20. General-Purpose Interface GPIO7 and GPIO8 Registers Summary (continued)

Register Name	Type	Register Width (Bits)	Address Offset	GPIO7 L4 Physical Address	GPIO8 L4 Physical Address
RESERVED		32	0x0000 0160	0x4805 1160	0x4805 3160
RESERVED		32	0x0000 0164	0x4805 1164	0x4805 3164
RESERVED		32	0x0000 0170	0x4805 1170	0x4805 3170
RESERVED		32	0x0000 0174	0x4805 1174	0x4805 3174
RESERVED		32	0x0000 0180	0x4805 1180	0x4805 3180
RESERVED		32	0x0000 0184	0x4805 1184	0x4805 3184
GPIO_CLEARDATAOUT	RW	32	0x0000 0190	0x4805 1190	0x4805 3190
GPIO_SETDATAOUT	RW	32	0x0000 0194	0x4805 1194	0x4805 3194

25.6.2.2 General-Purpose Interface Register Description

through describe the individual general-purpose interface registers.

Table 25-21. GPIO_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4AE1 0000	**Instance**	GPIO1
	0x4805 5000		GPIO2
	0x4805 7000		GPIO3
	0x4805 9000		GPIO4
	0x4805 B000		GPIO5
	0x4805 D000		GPIO6
	0x4805 1000		GPIO7
	0x4805 3000		GPIO8
Description	IP revision identifier (X.Y.R)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP revision	R	See(1)

(1) TI Internal Data

Table 25-22. Register Call Summary for Register GPIO_REVISION

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- General-Purpose Interface Register Summary: [0] [1] [2]

Table 25-23. GPIO_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4AE1 0010	**Instance**	GPIO1
	0x4805 5010		GPIO2
	0x4805 7010		GPIO3
	0x4805 9010		GPIO4
	0x4805 B010		GPIO5
	0x4805 D010		GPIO6
	0x4805 1010		GPIO7
	0x4805 3010		GPIO8
Description	System configuration register		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x0000000
4:3	IDLEMODE	0x0: Force-idle: An IDLE request is acknowledged unconditionally. 0x1: No-idle: An IDLE request is never acknowledged. 0x2: Smart-idle: The acknowledgment to an IDLE request is given based on the internal activity (see Section 25.4.5.2.3, *System Power Management and Wakeup*). 0x3: Smart-idle wakeup	RW	0x0
2	ENAWAKEUP	Wake-up control. 0x0: Wake-up generation is disabled. 0x1: Wake-up capability is enabled upon expected transition on input GPIO pin	RW	0
1	SOFTRESET	Software reset. Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads, it always returns 0. 0x0: Normal mode 0x1: The module is reset.	RW	0
0	AUTOIDLE	OCP clock gating control. 0x0: Internal interface OCP clock is free-running. 0x1: Automatic internal OCP clock gating, based on the OCP interface activity	RW	0

Table 25-24. Register Call Summary for Register GPIO_SYSCONFIG

General-Purpose Interface Functional Description • Asynchronous Path: Wake-Up Request Generation: [0] • General-Purpose Interface Hardware and Software Reset: [1] [2] [3] • System Power Management and Wakeup: [4] [5] [6] [7] [8] • Module Power Saving: [9] [10] [11] [12] [13] [14]
General-Purpose Interface Programming Guide • General-Purpose Interface Module Global Initialization: [15] [16] [17] [18]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [19] [20] [21]

Table 25-25. GPIO_IRQSTATUS_RAW_0

Address Offset	0x0000 0024		
Physical Address	0x4AE1 0024	**Instance**	GPIO1
	0x4805 5024		GPIO2
	0x4805 7024		GPIO3
	0x4805 9024		GPIO4
	0x4805 B024		GPIO5
	0x4805 D024		GPIO6
	0x4805 1024		GPIO7
	0x4805 3024		GPIO8
Description	Per-event raw interrupt status vector (corresponding to first line of interrupt)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status raw for interrupt line	RW	0x0000 0000

Table 25-26. Register Call Summary for Register GPIO_IRQSTATUS_RAW_0

General-Purpose Interface Functional Description
- Synchronous Path: Interrupt Request Generation: [0]
- Asynchronous Path: Wake-Up Request Generation: [1] [2]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [3] [4] [5]

Table 25-27. GPIO_IRQSTATUS_RAW_1

Address Offset	0x0000 0028		
Physical Address	0x4AE1 0028	**Instance**	GPIO1
	0x4805 5028		GPIO2
	0x4805 7028		GPIO3
	0x4805 9028		GPIO4
	0x4805 B028		GPIO5
	0x4805 D028		GPIO6
	0x4805 1028		GPIO7
	0x4805 3028		GPIO8
Description	Per-event raw interrupt status vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status raw for interrupt line	RW	0x0000 0000

Table 25-28. Register Call Summary for Register GPIO_IRQSTATUS_RAW_1

General-Purpose Interface Functional Description
- Synchronous Path: Interrupt Request Generation: [0]
- Asynchronous Path: Wake-Up Request Generation: [1]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [2] [3] [4]

Table 25-29. GPIO_IRQSTATUS_0

Address Offset	0x0000 002C		
Physical Address	0x4AE1 002C	**Instance**	GPIO1
	0x4805 502C		GPIO2
	0x4805 702C		GPIO3
	0x4805 902C		GPIO4
	0x4805 B02C		GPIO5
	0x4805 D02C		GPIO6
	0x4805 102C		GPIO7
	0x4805 302C		GPIO8
Description	Per-event interrupt status vector (enabled) (corresponding to first line of interrupt)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status for interrupt line	RW	0x0000 0000

Table 25-30. Register Call Summary for Register GPIO_IRQSTATUS_0

General-Purpose Interface Functional Description
• Interrupt (or Wake-Up) Line Release: [0]
• Interrupt Requests Generation: [1] [2] [3] [4] [5] [6] [7]
General-Purpose Interface Register Manual
• General-Purpose Interface Register Summary: [8] [9] [10]

Table 25-31. GPIO_IRQSTATUS_1

Address Offset	0x0000 0030		
Physical Address	0x4AE1 0030	**Instance**	GPIO1
	0x4805 5030		GPIO2
	0x4805 7030		GPIO3
	0x4805 9030		GPIO4
	0x4805 B030		GPIO5
	0x4805 D030		GPIO6
	0x4805 1030		GPIO7
	0x4805 3030		GPIO8
Description	Per-event enabled interrupt status vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status for interrupt line	RW	0x0000 0000

Table 25-32. Register Call Summary for Register GPIO_IRQSTATUS_1

General-Purpose Interface Functional Description
• Interrupt (or Wake-Up) Line Release: [0]
• Interrupt Requests Generation: [1] [2] [3] [4] [5] [6] [7]
General-Purpose Interface Register Manual
• General-Purpose Interface Register Summary: [8] [9] [10]

Table 25-33. GPIO_IRQSTATUS_SET_0

Address Offset	0x0000 0034		
Physical Address	0x4AE1 0034	**Instance**	GPIO1
	0x4805 5034		GPIO2
	0x4805 7034		GPIO3
	0x4805 9034		GPIO4
	0x4805 B034		GPIO5
	0x4805 D034		GPIO6
	0x4805 1034		GPIO7
	0x4805 3034		GPIO8
Description	Per-event interrupt-enable set vector (corresponding to first line of interrupt)		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status set for interrupt line	RW	0x0000 0000

Table 25-34. Register Call Summary for Register GPIO_IRQSTATUS_SET_0

General-Purpose Interface Functional Description
- General-Purpose Interface Block Diagram: [0]
- Synchronous Path: Interrupt Request Generation: [1]
- Asynchronous Path: Wake-Up Request Generation: [2] [3]
- Interrupt Requests Generation: [4] [5] [6] [7] [8]
- General-Purpose Interface Data Input/Output Capabilities: [9] [10] [11]
- Description: [12]
- Set Register Addresses: [13] [14] [15]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [16]
- General-Purpose Interface Set Bit Function: [17]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [18] [19] [20]

Table 25-35. GPIO_IRQSTATUS_SET_1

Address Offset	0x0000 0038		
Physical Address	0x4AE1 0038	**Instance**	GPIO1
	0x4805 5038		GPIO2
	0x4805 7038		GPIO3
	0x4805 9038		GPIO4
	0x4805 B038		GPIO5
	0x4805 D038		GPIO6
	0x4805 1038		GPIO7
	0x4805 3038		GPIO8
Description	Per-event enable set interrupt vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status set for interrupt line	RW	0x0000 0000

Table 25-36. Register Call Summary for Register GPIO_IRQSTATUS_SET_1

General-Purpose Interface Functional Description
- General-Purpose Interface Block Diagram: [0]
- Synchronous Path: Interrupt Request Generation: [1]
- Interrupt Requests Generation: [2] [3] [4] [5] [6]
- General-Purpose Interface Data Input/Output Capabilities: [7]
- Description: [8]
- Set Register Addresses: [9] [10] [11]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [12]
- General-Purpose Interface Set Bit Function: [13]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [14] [15] [16]

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Table 25-37. GPIO_IRQSTATUS_CLR_0

Address Offset	0x0000 003C		
Physical Address	0x4AE1 003C	**Instance**	GPIO1
	0x4805 503C		GPIO2
	0x4805 703C		GPIO3
	0x4805 903C		GPIO4
	0x4805 B03C		GPIO5
	0x4805 D03C		GPIO6
	0x4805 103C		GPIO7
	0x4805 303C		GPIO8
Description	Per-event interrupt-enable clear vector (corresponding to first line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status clear for interrupt line	RW	0x0000 0000

Table 25-38. Register Call Summary for Register GPIO_IRQSTATUS_CLR_0

General-Purpose Interface Functional Description
- General-Purpose Interface Block Diagram: [0]
- Synchronous Path: Interrupt Request Generation: [1]
- Asynchronous Path: Wake-Up Request Generation: [2]
- Interrupt Requests Generation: [3] [4]
- Description: [5]
- Clear Register Addresses: [6] [7] [8]

General-Purpose Interface Programming Guide
- General-Purpose Interface Clear Bit Function: [9]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [10] [11] [12]

Table 25-39. GPIO_IRQSTATUS_CLR_1

Address Offset	0x0000 0040		
Physical Address	0x4AE1 0040	**Instance**	GPIO1
	0x4805 5040		GPIO2
	0x4805 7040		GPIO3
	0x4805 9040		GPIO4
	0x4805 B040		GPIO5
	0x4805 D040		GPIO6
	0x4805 1040		GPIO7
	0x4805 3040		GPIO8
Description	Per-event enable clear interrupt vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Status clear for interrupt line	RW	0x0000 0000

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Table 25-40. Register Call Summary for Register GPIO_IRQSTATUS_CLR_1

General-Purpose Interface Functional Description • General-Purpose Interface Block Diagram: [0] • Synchronous Path: Interrupt Request Generation: [1] • Asynchronous Path: Wake-Up Request Generation: [2] • Interrupt Requests Generation: [3] [4] • Description: [5] • Clear Register Addresses: [6] [7] [8]
General-Purpose Interface Programming Guide • General-Purpose Interface Clear Bit Function: [9]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [10] [11] [12]

Table 25-41. GPIO_IRQWAKEN_0

Address Offset	0x0000 0044		
Physical Address	0x4AE1 0044	**Instance**	GPIO1
	0x4805 5044		GPIO2
	0x4805 7044		GPIO3
	0x4805 9044		GPIO4
	0x4805 B044		GPIO5
	0x4805 D044		GPIO6
	0x4805 1044		GPIO7
	0x4805 3044		GPIO8
Description	Per-event wake-up enable set vector (corresponding to first line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Wakeup set for interrupt line Setting a bit to 1 will enable wakeup for the corresponding event. Setting a bit to 0 will disable wakeup for the corresponding event.	RW	0x0000 0000

Table 25-42. Register Call Summary for Register GPIO_IRQWAKEN_0

General-Purpose Interface Functional Description • Asynchronous Path: Wake-Up Request Generation: [0] • Module Power Saving: [1] • Interrupt Requests Generation: [2] • Wake-Up Requests Generation: [3] • General-Purpose Interface Data Input/Output Capabilities: [4]
General-Purpose Interface Programming Guide • General-Purpose Interface Module Global Initialization: [5]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [6] [7] [8]

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Table 25-43. GPIO_IRQWAKEN_1

Address Offset	0x0000 0048		
Physical Address	0x4AE1 0048	**Instance**	GPIO1
	0x4805 5048		GPIO2
	0x4805 7048		GPIO3
	0x4805 9048		GPIO4
	0x4805 B048		GPIO5
	0x4805 D048		GPIO6
	0x4805 1048		GPIO7
	0x4805 3048		GPIO8
Description	Per-event wake-up enable set vector (corresponding to second line of interrupt)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	Wakeup set for interrupt line Setting a bit to 1 will enable wakeup for the corresponding event. Setting a bit to 0 will disable wakeup for the corresponding event.	RW	0x0000 0000

Table 25-44. Register Call Summary for Register GPIO_IRQWAKEN_1

General-Purpose Interface Functional Description
- Asynchronous Path: Wake-Up Request Generation: [0]
- Module Power Saving: [1]
- Interrupt Requests Generation: [2]
- Wake-Up Requests Generation: [3]
- General-Purpose Interface Data Input/Output Capabilities: [4]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [5]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [6] [7] [8]

Table 25-45. GPIO_SYSSTATUS

Address Offset	0x0000 0114		
Physical Address	0x4AE1 0114	**Instance**	GPIO1
	0x4805 5114		GPIO2
	0x4805 7114		GPIO3
	0x4805 9114		GPIO4
	0x4805 B114		GPIO5
	0x4805 D114		GPIO6
	0x4805 1114		GPIO7
	0x4805 3114		GPIO8
Description	System status register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

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Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	Read 0x0: Internal reset is ongoing. Read 0x1: Reset completed	R	0

Table 25-46. Register Call Summary for Register GPIO_SYSSTATUS

General-Purpose Interface Functional Description
• General-Purpose Interface Hardware and Software Reset: [0] [1]
General-Purpose Interface Programming Guide
• General-Purpose Interface Module Global Initialization: [2]
General-Purpose Interface Register Manual
• General-Purpose Interface Register Summary: [3] [4] [5]

Table 25-47. GPIO_CTRL

Address Offset	0x0000 0130		
Physical Address	0x4AE1 0130	**Instance**	GPIO1
	0x4805 5130		GPIO2
	0x4805 7130		GPIO3
	0x4805 9130		GPIO4
	0x4805 B130		GPIO5
	0x4805 D130		GPIO6
	0x4805 1130		GPIO7
	0x4805 3130		GPIO8
Description	GPIO control register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													GATINGRATIO		DISABLEMODULE

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2:1	GATINGRATIO	Clock gating ratio for event detection 0x0: N = 1 0x1: N = 2 0x2: N = 4 0x3: N = 8	RW	0x1
0	DISABLEMODULE	0x0: Module is enabled, clocks are not gated. 0x1: Module is disabled, internal clocks are gated	RW	0

Table 25-48. Register Call Summary for Register GPIO_CTRL

General-Purpose Interface Functional Description
• Clocking: [0]
• Operating Modes: [1] [2] [3] [4]
• Module Power Saving: [5] [6] [7]
General-Purpose Interface Programming Guide
• General-Purpose Interface Module Global Initialization: [8]

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Table 25-48. Register Call Summary for Register GPIO_CTRL (continued)

General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [9] [10] [11]

Table 25-49. GPIO_OE

Address Offset	0x0000 0134		
Physical Address	0x4AE1 0134	**Instance**	GPIO1
	0x4805 5134		GPIO2
	0x4805 7134		GPIO3
	0x4805 9134		GPIO4
	0x4805 B134		GPIO5
	0x4805 D134		GPIO6
	0x4805 1134		GPIO7
	0x4805 3134		GPIO8
Description	Output enable register. 0 = Output enabled ; 1 = Output disabled		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUTEN																															

Bits	Field Name	Description	Type	Reset
31:0	OUTPUTEN	Output enable 0x0: Output enabled 0x1: Output disabled	RW	0xFFFF FFFF

Table 25-50. Register Call Summary for Register GPIO_OE

General-Purpose Interface Overview • General-Purpose Interface Overview: [0]
General-Purpose Interface Functional Description • General-Purpose Interface Data Input/Output Capabilities: [1] [2] [3]
General-Purpose Interface Programming Guide • General-Purpose Interface Module Global Initialization: [4]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [5] [6] [7]

Table 25-51. GPIO_DATAIN

Address Offset	0x0000 0138		
Physical Address	0x4AE1 0138	**Instance**	GPIO1
	0x4805 5138		GPIO2
	0x4805 7138		GPIO3
	0x4805 9138		GPIO4
	0x4805 B138		GPIO5
	0x4805 D138		GPIO6
	0x4805 1138		GPIO7
	0x4805 3138		GPIO8
Description	Data input register (with sampled input data)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATAIN																															

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Bits	Field Name	Description	Type	Reset
31:0	DATAIN	Sampled input data	R	0x0000 0000

Table 25-52. Register Call Summary for Register GPIO_DATAIN

General-Purpose Interface Overview • General-Purpose Interface Overview: [0]
General-Purpose Interface Functional Description • System Power Management and Wakeup: [1] • Module Power Saving: [2] • General-Purpose Interface Data Input/Output Capabilities: [3]
General-Purpose Interface Programming Guide • General-Purpose Interface Read Input Register: [4]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [5] [6] [7]

Table 25-53. GPIO_DATAOUT

Address Offset	0x0000 013C		
Physical Address	0x4AE1 013C	**Instance**	GPIO1
	0x4805 513C		GPIO2
	0x4805 713C		GPIO3
	0x4805 913C		GPIO4
	0x4805 B13C		GPIO5
	0x4805 D13C		GPIO6
	0x4805 113C		GPIO7
	0x4805 313C		GPIO8
Description	Data-output register (data to set on output pins)		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATAOUT																															

Bits	Field Name	Description	Type	Reset
31:0	DATAOUT	Data to set on output pins	RW	0x0000 0000

Table 25-54. Register Call Summary for Register GPIO_DATAOUT

General-Purpose Interface Overview • General-Purpose Interface Overview: [0] [1]
General-Purpose Interface Functional Description • General-Purpose Interface Data Input/Output Capabilities: [2] • Description: [3]
General-Purpose Interface Programming Guide • General-Purpose Interface Write Output Register: [4]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [5] [6] [7]

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Table 25-55. GPIO_LEVELDETECT0

Address Offset	0x0000 0140		
Physical Address	0x4AE1 0140	**Instance**	GPIO1
	0x4805 5140		GPIO2
	0x4805 7140		GPIO3
	0x4805 9140		GPIO4
	0x4805 B140		GPIO5
	0x4805 D140		GPIO6
	0x4805 1140		GPIO7
	0x4805 3140		GPIO8
Description	Detect low-level register. 0 = Low-level detection disabled; 1 = Low-level detection enabled		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVELDETECT0																															

Bits	Field Name	Description	Type	Reset
31:0	LEVELDETECT0	Low-level detection 0x0: Low-level detection disabled 0x1: Low-level detection enabled	RW	0x0000 0000

Table 25-56. Register Call Summary for Register GPIO_LEVELDETECT0

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [0] [1]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [2] [3] [4]

Table 25-57. GPIO_LEVELDETECT1

Address Offset	0x0000 0144		
Physical Address	0x4AE1 0144	**Instance**	GPIO1
	0x4805 5144		GPIO2
	0x4805 7144		GPIO3
	0x4805 9144		GPIO4
	0x4805 B144		GPIO5
	0x4805 D144		GPIO6
	0x4805 1144		GPIO7
	0x4805 3144		GPIO8
Description	Detect high-level register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVELDETECT1																															

Bits	Field Name	Description	Type	Reset
31:0	LEVELDETECT1	0x0: High-evel detection disabled 0x1: High-level detection enabled	RW	0x0000 0000

Table 25-58. Register Call Summary for Register GPIO_LEVELDETECT1

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [0] [1]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [2] [3] [4]

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Table 25-59. GPIO_RISINGDETECT

Address Offset	0x0000 0148		
Physical Address	0x4AE1 0148	**Instance**	GPIO1
	0x4805 5148		GPIO2
	0x4805 7148		GPIO3
	0x4805 9148		GPIO4
	0x4805 B148		GPIO5
	0x4805 D148		GPIO6
	0x4805 1148		GPIO7
	0x4805 3148		GPIO8
Description	Detect rising edge register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RISINGDETECT																															

Bits	Field Name	Description	Type	Reset
31:0	RISINGDETECT	0x0: Rising edge detection disabled 0x1: Rising edge detection enabled	RW	0x0000 0000

Table 25-60. Register Call Summary for Register GPIO_RISINGDETECT

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [0] [1]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [2] [3] [4]

Table 25-61. GPIO_FALLINGDETECT

Address Offset	0x0000 014C		
Physical Address	0x4AE1 014C	**Instance**	GPIO1
	0x4805 514C		GPIO2
	0x4805 714C		GPIO3
	0x4805 914C		GPIO4
	0x4805 B14C		GPIO5
	0x4805 D14C		GPIO6
	0x4805 114C		GPIO7
	0x4805 314C		GPIO8
Description	Detect falling edge register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FALLINGDETECT																															

Bits	Field Name	Description	Type	Reset
31:0	FALLINGDETECT	0x0: Falling edge detection disabled 0x1: Falling edge detection enabled	RW	0x0000 0000

Table 25-62. Register Call Summary for Register GPIO_FALLINGDETECT

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [0] [1]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [2] [3] [4]

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Table 25-63. GPIO_DEBOUNCENABLE

Address Offset	0x0000 0150		
Physical Address	0x4AE1 0150	**Instance**	GPIO1
	0x4805 5150		GPIO2
	0x4805 7150		GPIO3
	0x4805 9150		GPIO4
	0x4805 B150		GPIO5
	0x4805 D150		GPIO6
	0x4805 1150		GPIO7
	0x4805 3150		GPIO8
Description	Debouncing enable register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBOUNCEENABLE																															

Bits	Field Name	Description	Type	Reset
31:0	DEBOUNCEENABLE	0x0: No debouncing 0x1: Debouncing activated	RW	0x0000 0000

Table 25-64. Register Call Summary for Register GPIO_DEBOUNCENABLE

General-Purpose Interface Functional Description
- Module Power Saving: [0]

General-Purpose Interface Programming Guide
- General-Purpose Interface Module Global Initialization: [1]

General-Purpose Interface Register Manual
- General-Purpose Interface Register Summary: [2] [3] [4]

Table 25-65. GPIO_DEBOUNCINGTIME

Address Offset	0x0000 0154		
Physical Address	0x4AE1 0154	**Instance**	GPIO1
	0x4805 5154		GPIO2
	0x4805 7154		GPIO3
	0x4805 9154		GPIO4
	0x4805 B154		GPIO5
	0x4805 D154		GPIO6
	0x4805 1154		GPIO7
	0x4805 3154		GPIO8
Description	Debouncing value register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEBOUNCETIME							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	DEBOUNCETIME	8-bit values specifying the debouncing time in 31-µs steps	RW	0x00

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Table 25-66. Register Call Summary for Register GPIO_DEBOUNCINGTIME

General-Purpose Interface Functional Description • Synchronous Path: Interrupt Request Generation: [0] [1] • Clocking: [2] [3] [4] • System Power Management and Wakeup: [5] [6]
General-Purpose Interface Programming Guide • General-Purpose Interface Module Global Initialization: [7]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [8] [9] [10]

Table 25-67. GPIO_CLEARDATAOUT

Address Offset	0x0000 0190		
Physical Address	0x4AE1 0190	**Instance**	GPIO1
	0x4805 5190		GPIO2
	0x4805 7190		GPIO3
	0x4805 9190		GPIO4
	0x4805 B190		GPIO5
	0x4805 D190		GPIO6
	0x4805 1190		GPIO7
	0x4805 3190		GPIO8
Description	Clear data-output register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	0x0: No effect 0x1: Clear the corresponding bit in the data-output register	RW	0x0000 0000

Table 25-68. Register Call Summary for Register GPIO_CLEARDATAOUT

General-Purpose Interface Functional Description • General-Purpose Interface Data Input/Output Capabilities: [0] • Clear Register Addresses: [1]
General-Purpose Interface Programming Guide • General-Purpose Interface Clear Bit Function: [2]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [3] [4] [5]

Table 25-69. GPIO_SETDATAOUT

Address Offset	0x0000 0194		
Physical Address	0x4AE1 0194	**Instance**	GPIO1
	0x4805 5194		GPIO2
	0x4805 7194		GPIO3
	0x4805 9194		GPIO4
	0x4805 B194		GPIO5
	0x4805 D194		GPIO6
	0x4805 1194		GPIO7
	0x4805 3194		GPIO8
Description	Set data-output register		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTLINE																															

Bits	Field Name	Description	Type	Reset
31:0	INTLINE	0x0: No effect 0x1: Set the corresponding bit in the data-output register	RW	0x0000 0000

Table 25-70. Register Call Summary for Register GPIO_SETDATAOUT

General-Purpose Interface Functional Description • General-Purpose Interface Data Input/Output Capabilities: [0] • Set Register Addresses: [1] • Set Instruction Example: [2] [3]
General-Purpose Interface Programming Guide • General-Purpose Interface Set Bit Function: [4]
General-Purpose Interface Register Manual • General-Purpose Interface Register Summary: [5] [6] [7]

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Keyboard Controller

This chapter describes the keyboard module (KBD) of the device.

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26.1 Keyboard Controller Overview 5798
26.2 Keyboard Controller Environment 5800
26.3 Keyboard Controller Integration 5803
26.4 Keyboard Controller Functional Description 5805
26.5 Keyboard Controller Programming Guide 5814
26.6 Keyboard Controller Register Manual 5818

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26.1 Keyboard Controller Overview

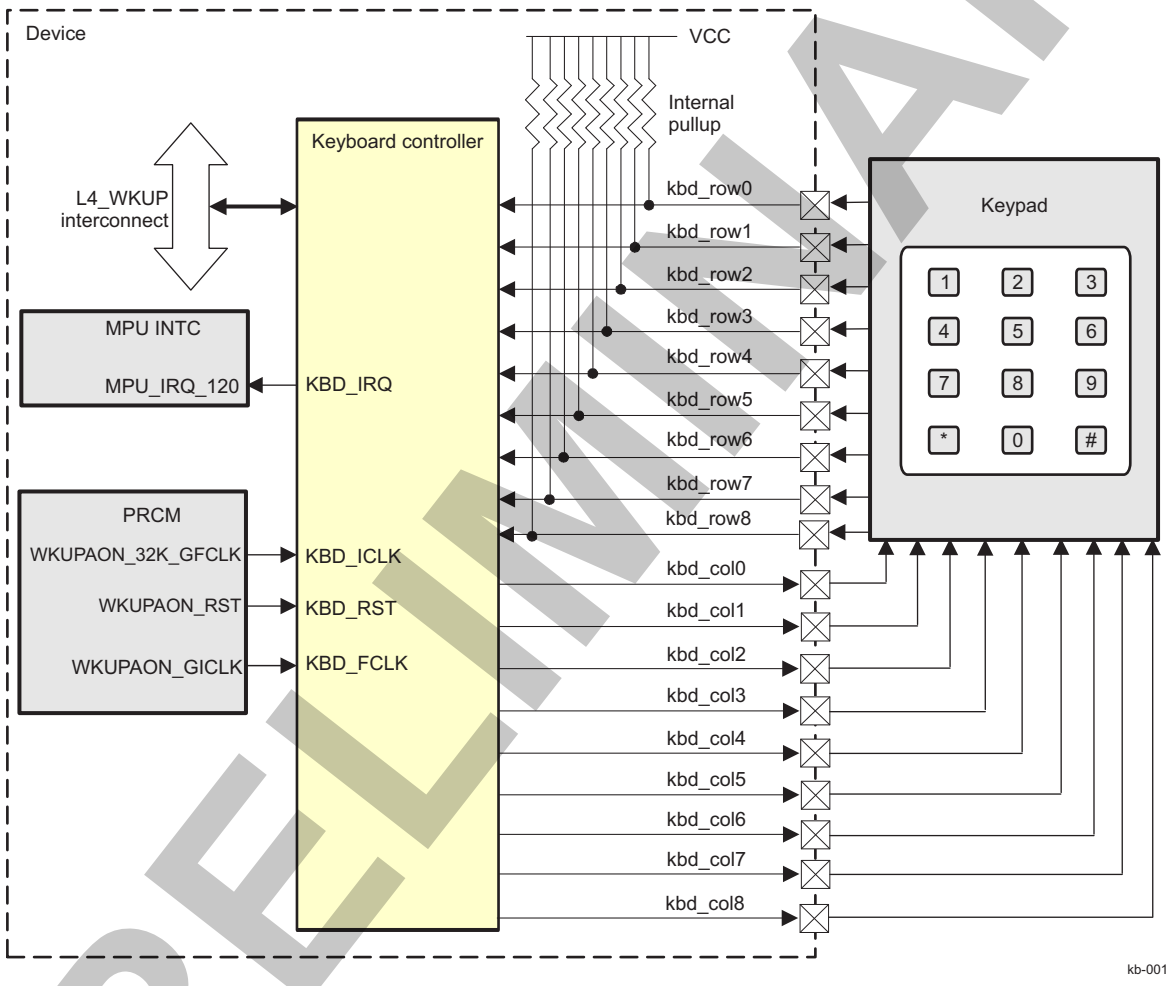
The keyboard controller implements a built-in scanning algorithm for hardware-based key-press decoding and reduces overhead in the microprocessor unit (MPU) software.

The keyboard controller includes a debouncing feature to ensure that only one key combination can be registered in the programmed time.

The keyboard controller can handle up to 9 × 9 keys, works on a 32-kHz clock, and can generate wake-up events when the chip is in sleep mode.

Figure 26-1 shows the keyboard controller.

Figure 26-1. Keyboard Controller Overview



The keyboard controller includes the following main features:

- Support of multiconfiguration keyboards up to 9 rows × 9 columns
- Each key coded on 1 bit in two 32-bit registers
- Long-key value or repeat timing reconfigurable on the fly
- Event detection on key press and key release
- Multikey-press detection and decoding
- Long-key detection on prolonged key press
- Integrated timer with four programmable comparison values
- Programmable time-out on permanent key press or after keyboard release
- Programmable interrupt generation on key events

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- Software reset capability
- Read/write-posted register access modes
- 8-/16-/32-bit access supported on the level 4 (L4) interface
- 32-bit data bus
- 7-bit address bus

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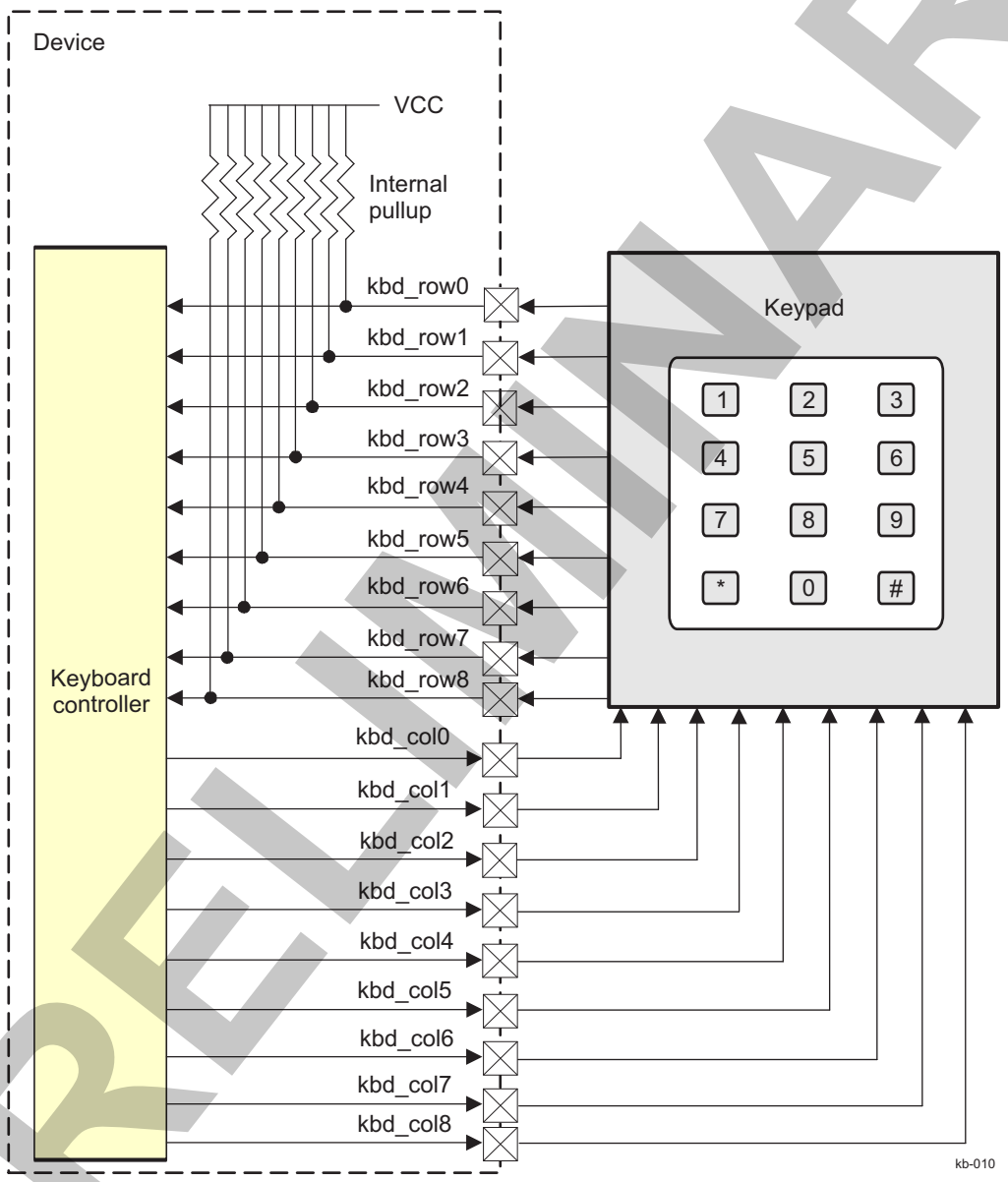
26.2 Keyboard Controller Environment

The keyboard controller external interface pins map on the device pads when the device IO cells are configured and multiplexed for the keypad function by the control module. For more information, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and Section 25.2.1, *General-Purpose Interface as a Keyboard interface*.

The external keypad typically connects directly to the keyboard controller of the device (see Figure 26-2).

Figure 26-2. Typical Keyboard Environment



26.2.1 Keyboard Controller Functions/Modes

The keyboard controller executes two functions:

- Keypad scanning and decoding for input of the external key presses. For more information, see Section 26.4.5, *Keyboard Controller Software Mode*, and Section 26.4.6, *Keyboard Controller Hardware Decoding Modes*.
- Device wakeup by interrupt request to the processor when a key is pressed and the device is in idle or sleep mode. For more information, see Section 26.4.6.4, *Keyboard Controller Interrupt Generation*.

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26.2.2 Keyboard Controller Signals

Table 26-1 describes the module signals and specifies their links to functions.

Table 26-1. I/O External Keyboard Signals

Signal	I/O[1]	Description	Reset Value	Function	Wake-Up Capability
kbd_row0	I	Keypad row 0 feed	HiZ (pulled up)	Key reading	Yes
kbd_row1	I	Keypad row 1 feed	HiZ (pulled up)	Key reading	Yes
kbd_row2	I	Keypad row 2 feed	HiZ (pulled up)	Key reading	Yes
kbd_row3	I	Keypad row 3 feed	HiZ (pulled up)	Key reading	Yes
kbd_row4	I	Keypad row 4 feed	HiZ (pulled up)	Key reading	Yes
kbd_row5	I	Keypad row 5 feed	HiZ (pulled up)	Key reading	Yes
kbd_row6	I	Keypad row 6 feed	HiZ (pulled up)	Key reading	Yes
kbd_row7	I	Keypad row 7 feed	HiZ (pulled up)	Key reading	Yes
kbd_row8	I	Keypad row 8 feed	HiZ (pulled up)	Key reading	Yes
kbd_col0	O	Keypad column 0 feed, active low	HiZ	Key reading	No
kbd_col1	O	Keypad column 1 feed, active low	HiZ	Key reading	No
kbd_col2	O	Keypad column 2 feed, active low	HiZ	Key reading	No
kbd_col3	O	Keypad column 3 feed, active low	HiZ	Key reading	No
kbd_col4	O	Keypad column 4 feed, active low	HiZ	Key reading	No
kbd_col5	O	Keypad column 5 feed, active low	HiZ	Key reading	No
kbd_col6	O	Keypad column 6 feed, active low	HiZ	Key reading	No
kbd_col7	O	Keypad column 7 feed, active low	HiZ	Key reading	No
kbd_col8	O	Keypad column 8 feed, active low	HiZ	Key reading	No

(1) I = Input; O = Output

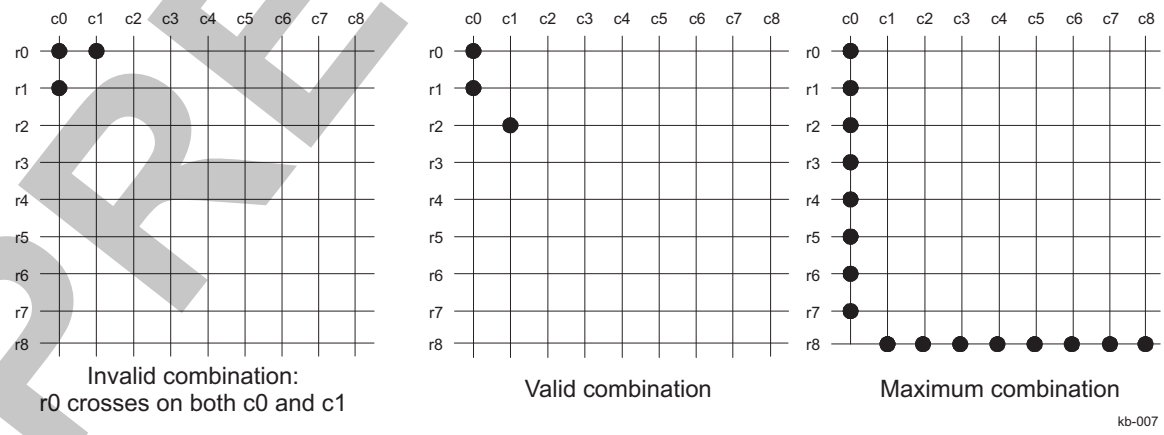
26.2.3 Protocols and Data Formats

The keyboard controller detects and decodes multikey combinations using the following rules:

- Any 2-key combination is valid and can be decoded.
- Combinations using more than two keys are valid only if the rows and columns used do not cross over on another key to be detected. This is caused by equipotent propagation on a row/column (multikey limitations).

Figure 26-3 shows an example of multikey limitation.

Figure 26-3. Multikey Limitation Example



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NOTE: When using the keyboard controller with a smaller keypad (for example, 5 × 5), unused rows must be tied high to prevent disturbing the scanning process. Normally, all rows must be pulled up internally at the I/O cells of the device.

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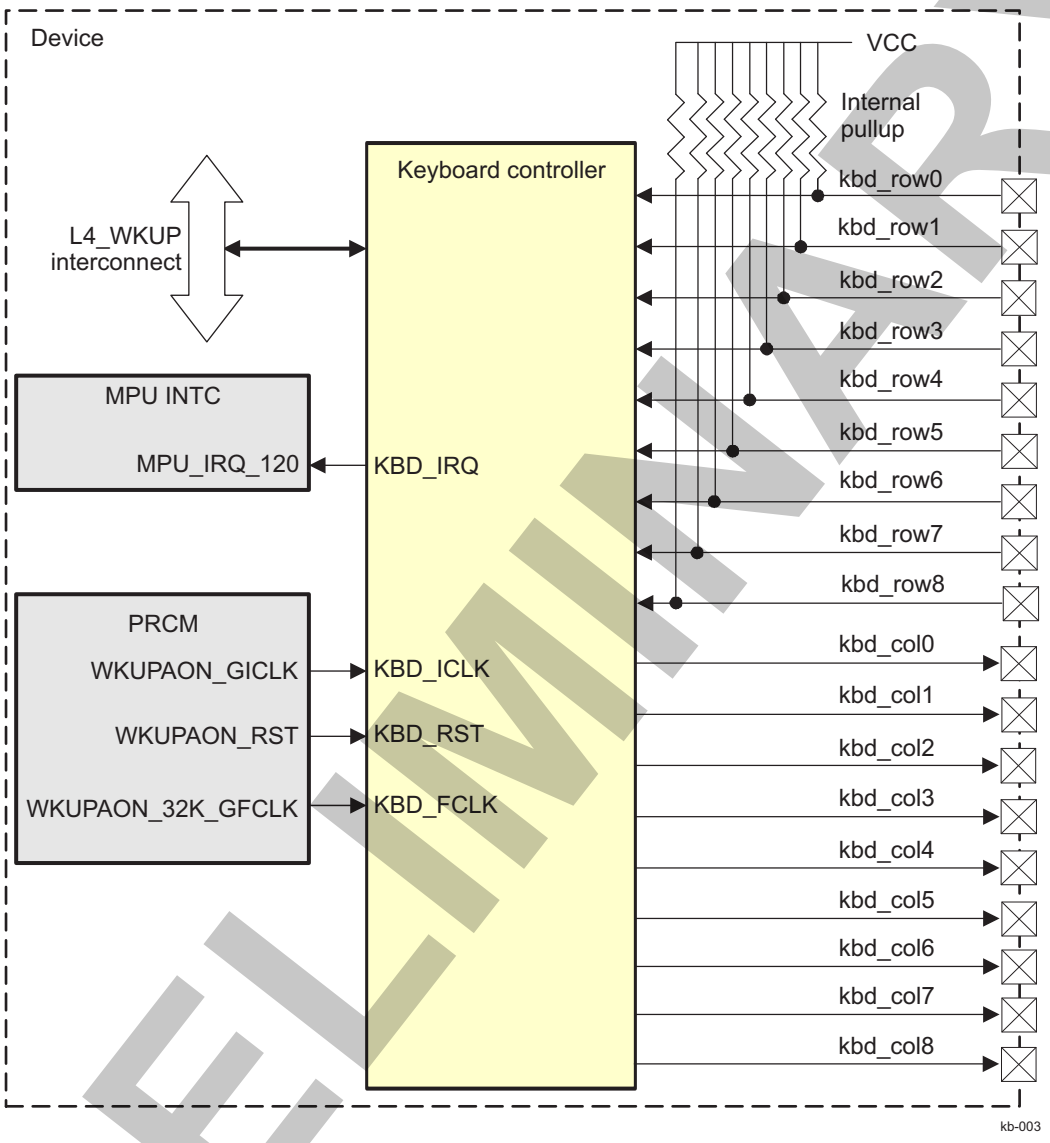
26.3 Keyboard Controller Integration

Figure 26-4 shows keyboard controller integration.

Figure 26-4. Keyboard Controller Integration



The control module must enable the internal pullups of the GPIO cells for all keypad rows (for more information about the configuration, see Chapter 18, *Control Module*).

Table 26-2 through Table 26-4 summarize the integration of the module in the device.

Table 26-2. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
KBD	PD_WKUPAON	Yes	L4_WKUP

Table 26-3. Clocks and Resets

		Clocks		
Module Instance	Destination Signal Name	Source Signal Name	Source	Description

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Table 26-3. Clocks and Resets (continued)

KBD	KBD_FCLK	WKUPAON_32K_GFCLK	PRCM	32-kHz functional clock. For information about PRCM clock gating and management, see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
KBD	KBD_ICLK	WKUPAON_GICLK	PRCM	L4-interconnect interface clock. For information about PRCM clock gating and management, see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.
			Resets	
KBD	KBD_RST	WKUPAON_RST	PRCM	Reset signal for the Keyboard controller.

Table 26-4. Hardware Requests

Interrupt Requests				
Module Instance	**Source Signal Name**	**Destination Signal Name**	**Destination**	**Description**
KBD	KBD_IRQ	MPU_IRQ_120	Cortex™-A15 INTC	Interrupt signal to the interrupt controller (INTC) of the MPU. For information about INTC interrupt control, see Chapter 17, *Interrupt Controllers*.

NOTE: For the description of the interrupt source, see Section 26.4.4, *Interrupt Requests*.

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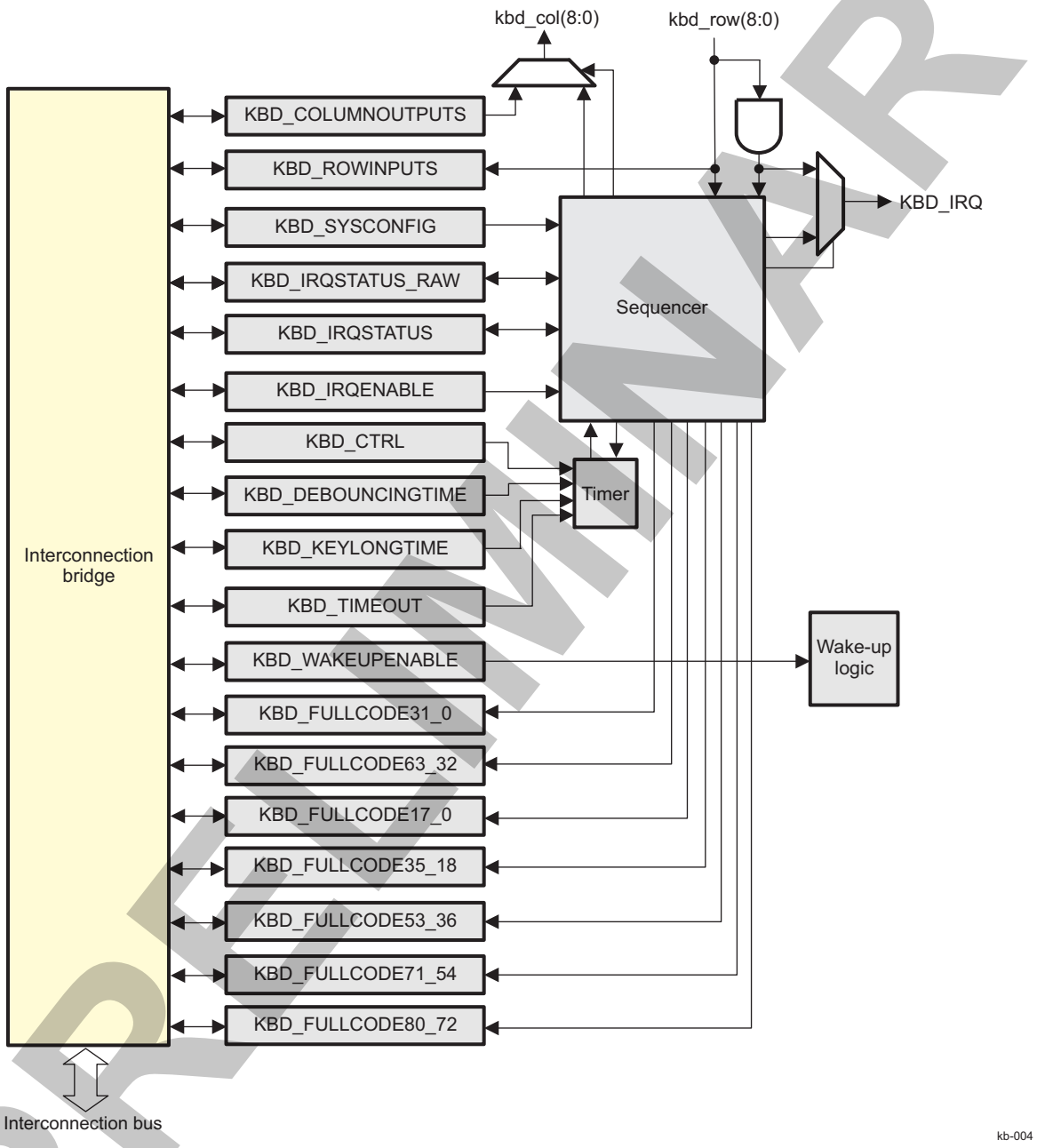
26.4 Keyboard Controller Functional Description

26.4.1 Keyboard Controller Block Diagram

Figure 26-5 shows the functional specification block diagram of the keyboard controller.

Figure 26-5. Keyboard Controller Block Diagram



The keyboard controller detects events issued on any key of the connected keyboard and generates an interrupt to alert the host processor. The built-in hardware-scan algorithm decodes the pressed keys, including multikey combinations.

To reduce MPU software overhead, the hardware performs detecting and decoding in the keyboard controller state-machine. However, hardware decoding can be deactivated so that software handles the scanning algorithm.

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The value of the columns output is determined in the KBD_COLUMNOUTPUTS[8:0] KBC_REG bit field. To activate a keypad row-column connection, the corresponding bit must be 0b0.

The following sections describe subfunctions and subfunction interactions (control and data paths).

26.4.2 Keyboard Controller Software Reset

To perform a software reset, set the KBD_SYSCONFIG[1] SOFTRESET bit to 1. When the software reset completes, the KBD_SYSCONFIG[1] SOFTRESET bit is automatically reset. Software must ensure that the software reset completes before performing mailbox operations.

26.4.3 Keyboard Controller Power Management

Table 26-5 describes the power-management features available for the keyboard controller.

NOTE: For information about source clock gating and a description of the sleep/wake-up transitions, see Section 3.1.1.1.4, *Clock Domain-Level Clock Management*, in Chapter 3, *Power, Reset, and Clock Management*.

Table 26-5. Local Power-Management Features

Feature	Registers	Description
Slave idle modes	KBD_SYSCONFIG[4:3] IDLEMODE	Force-idle, no-idle, and smart-idle modes are available.
Master standby modes	N/A	N/A
Wake-up sources enable	KBD_IRQWAKEEN	This register holds one active-high enable bit per event source able to generate a wake-up signal.

26.4.4 Keyboard Controller Interrupt Requests

Table 26-6 lists the event flags, and their mask, that can cause module interrupts.

Table 26-6. Events

Event Flag	Event Mask	Description
KBD_IRQSTATUS[3] MISS_EVENT	–	A miss event occurs.
KBD_IRQSTATUS[2] IT_TIMEOUT	KBD_IRQENABLE_SET/KBD_IRQENABLE_CLR[2] IT_TIMEOUT_EN	A time-out event is detected.
KBD_IRQSTATUS[1] IT_LONG_KEY	KBD_IRQENABLE_SET/KBD_IRQENABLE_CLR[1] IT_LONG_KEY_EN	A long-key event is detected.
KBD_IRQSTATUS[0] IT_EVENT	KBD_IRQENABLE_SET/KBD_IRQENABLE_CLR[0] IT_EVENT_EN	An event is detected.

26.4.5 Keyboard Controller Software Mode

The KBD_CTRL[1] NSOFTWARE_MODE bit selects software mode when it is set to 0.

In software mode, the keyboard controller internal sequencer, which performs automatic scanning and decoding, is disabled. Consequently, software must manually perform the scanning algorithm.

The scanning sequence is managed using the keyboard controller column outputs register (KBD_COLUMNOUTPUTS) and the keyboard controller row inputs register (KBD_ROWINPUTS). In this configuration, the keyboard interrupt is a logical ANDing of all bits of the KBD_ROWINPUTS register.

For more information about the software scan, see Section 26.5.1, *Keyboard Controller Low-Level Programming Model*.

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26.4.6 Keyboard Controller Hardware Decoding Modes

26.4.6.1 Functional Modes

When running in hardware (default) decoding mode (the KBD_CTRL[1] NSOFTWARE_ MODE bit is set to 1), the keyboard controller offers several functional modes; these modes are summarized in Table 26-7. The keyboard interrupt depends on the configuration in the keyboard controller interrupt-enable register (KBD_IRQENABLE_SET). If the event is enabled (bit 0 is set to 1), an interrupt is generated when the sequencer detects an event. Even if this interrupt is disabled, the flag status of the keyboard controller interrupt-status register (KBD_IRQSTATUS) is updated.

Table 26-7. Keyboard Controller Functional Modes

Functional Mode	Associated Interrupt	Associated Timer Value	Description	Control
Keyboard event	Event interrupt	Debouncing value	Occurs when a key is pressed or released Always enabled	KBD_CTRL[8:5] bits must be set to 0 to disable all the other features.
Long key	Long-key interrupt	Long-key value	Used to detect a key that is pressed for a long time Should be associated with the long-key time-out function or repeat mode	KBD_CTRL[5] LONG_KEY
Repeat key	Long-key interrupt	Long-key value	Generates an interrupt every long-key delay No time-out can be associated.	KBD_CTRL[8] REPEAT_MODE
Empty time-out	Time-out interrupt	Empty time-out value	Interrupt generated if no key is pressed during an empty time-out period.	KBD_CTRL[6] TIMEOUT_EMPTY
Long-key time-out	Time-out interrupt	Long-key time-out value	Associated with the long-key function Generated after a long-key interrupt if no event occurs during a long-key time-out period	KBD_CTRL[7] TIMEOUT_LONG_KEY

Each mode can be activated/deactivated by setting the corresponding bits (5, 6, 7, and 8) in the KBD_CTRL register with the appropriate values (for more information, see Section 26.6, *Keyboard Controller Register Manual*).

26.4.6.2 Keyboard Controller Timer

As described in the previous section, each functional mode is associated with a timer value. Depending on the selected mode, the keyboard controller timer is loaded with the corresponding value as set in the related registers:

- KBD_DEBOUNCINGTIME
- KBD_KEYLONGTIME
- KBD_TIMEOUT

Table 26-8 summarizes the values of the keyboard controller timer.

Table 26-8. Keyboard Controller Timer Values

Timer Value	Associated Register Field	Description
Debouncing time	KBD_DEBOUNCINGTIME[5:0] DEBOUNCING_VALUE	To remove the effects of glitches when an event occurs on the keyboard, the controller waits for a debouncing period before taking a snapshot of the current state on the keyboard matrix. The timer is loaded with the debouncing time value after each detected event on the keyboard matrix. An event interrupt is generated after this delay.

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Table 26-8. Keyboard Controller Timer Values (continued)

Timer Value	Associated Register Field	Description
Long-key time	KBD_KEYLONGTIME[11:0] LONG_KEY_VALUE	This is the delay before generating a long-key interrupt after an event interrupt. If the long-key mode is selected, the timer is loaded with the long-key time value after an event interrupt is generated. In repeat mode, the timer is reloaded with the same value after a long-key interrupt, and starts to count down again.
Long-key time-out	KBD_TIMEOUT[15:0] TIMEOUT_VALUE	The timer is loaded with the time-out value and then a long-key interrupt is generated and starts to count down. When it reaches 0, a time-out interrupt is generated and the keyboard controller returns to its IDLE state. This long-key time-out does not work in repeat mode.
Empty key time-out	KBD_TIMEOUT[15:0] TIMEOUT_VALUE	The time-out interrupt occurs if no key is pressed during this delay. The keyboard controller then returns to IDLE state.

The timer countdown period depends on three factors:

- The loaded value as set in:
  - KBD_DEBOUNCINGTIME
  - KBD_KEYLONGTIME
  - KBD_TIMEOUT
- The value of the prescale clock timer as set in the KBD_CTRL[4:2] PTV bit field. This programmable clock divider allows the reduction of the clock frequency used by the timer.
- The frequency of the keyboard controller functional clock (32 kHz)

The period is calculated as follows:

$T_{period} = (T_{value} + 1) \times 2^{PTV + 1} \times T_{clk}$

Where:

T_{value} is the value stored in the KBD_DEBOUNCINGTIME, KBD_KEYLONGTIME, or KBD_TIMEOUT register.

PTV is the value of the KBD_CTRL[4:2] PTV bit field.

T_{clk} is the period of the 32-kHz functional clock; that is, 31.25 µs.

The KBD_CTRL[4:2] PTV bit field determines the division factor of the timer clock. Table 26-9 lists the divider rates.

Table 26-9. Timer Prescale Values

KBD_CTRL[4:2] PTV Value	Divisor
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7	256

NOTE: The timer minimum period is 62.5 µs; its maximum period is 524.288 seconds.

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To prevent undefined results, the KBD_CTRL[4:2] PTV bit field must not be changed when the timer is running.

The timer value registers (KBD_DEBOUNCINGTIME, KBD_KEYLONGTIME, and KBD_TIMEOUT) can be updated at any time, whether or not the timer is running. Nevertheless, the timer is updated only on the fly for the long-key time value. The new debouncing and time-out values are loaded only on the next load. Depending on the updated register, two cases can occur:

- The KBD_KEYLONGTIME register is updated; the new value stored in the KBD_KEYLONGTIME register is loaded into the timer when the register is written. If the timer is already counting down when KBD_KEYLONGTIME is updated, it counts down from the new value loaded in KBD_KEYLONGTIME.
- The KBD_DEBOUNCINGTIME or KBD_TIMEOUT register is updated; the new value is considered only when the next timer loads. If the timer is counting down when the registers are updated, the timer continues counting down from the previous value and is loaded with the new one on the next load.

Regardless of the timer state (stopped, counting down any of the values previously described, etc.), when a new event occurs on the keyboard, the timer is stopped and loaded with the debouncing time value. It then starts counting down.

26.4.6.3 State-Machine Status

To facilitate debugging, each state of the state-machine is coded in a register that indicates the current state of the machine. Table 26-10 lists the corresponding codes.

Table 26-10. State-Machine Values

KBD_STATEMACHINE[3:0] Value	Description
0x0	Idle
0x1	Scanning
0x2	Load timer debouncing
0x3	Test timer debouncing
0x4	Generated interrupt event
0x6	Load timer long key
0x7	Test timer long key
0x8	Generated interrupt long key
0x9	Load timer time-out
0xA	Test timer time-out
0xB	Generated interrupt time-out
0xF	Other

26.4.6.4 Keyboard Controller Interrupt Generation

26.4.6.4.1 Interrupt-Generation Scheme

The keyboard controller generates the KBD_IRQ interrupt signal to external INTC. Each functional mode generates dedicated interrupt events (logged in the KBD_IRQSTATUS register) that can be masked using the KBD_IRQENABLE_CLR register, or unmasked using the KBD_IRQENABLE_SET register.

The KBD_IRQSTATUS register is updated when the selected functional mode generates an interrupt event. However, the KBD_IRQ signal is asserted on the related event only if the corresponding bit is set to 0x1 in the KBD_IRQENABLE_SET register.

NOTE: To reset the interrupt status bit, 1 must be written to the appropriate bit of the KBD_IRQSTATUS read/write register.

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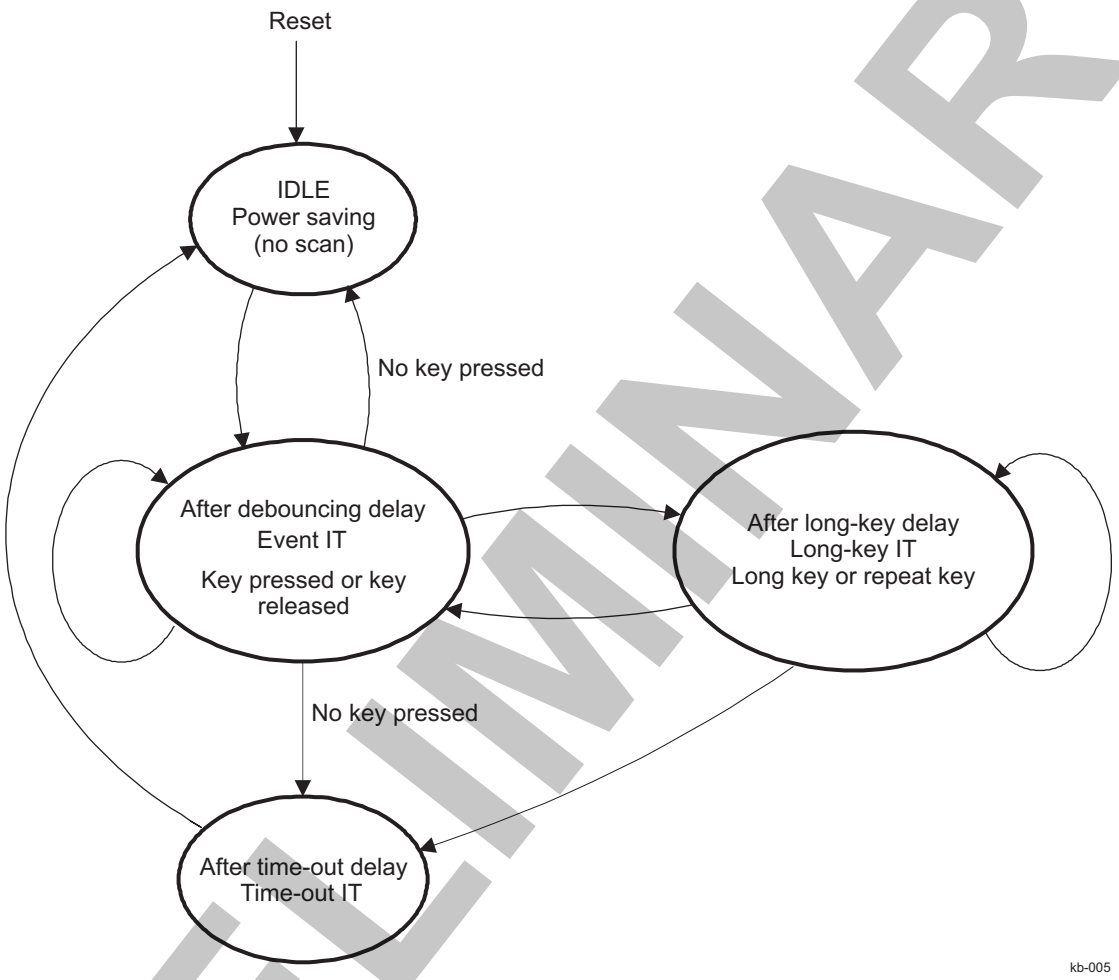
Figure 26-6 shows the different interrupt events generated in each keyboard controller functional mode and details the relationships between them.

NOTE: Depending on the selected mode, some interrupt events cannot be generated.

Figure 26-6. Functional Modes and Related Interrupt Events



While running in hardware-decoding mode, the keyboard controller performs automatic scans when not in IDLE state. When a key-press event occurs on the keyboard matrix, the keyboard controller leaves IDLE state and an interrupt event (the KBD_IRQSTATUS[0] IT_EVENT bit) is set after the timer counts down the debouncing delay. An IT_EVENT is generated when a key is pressed or released.

NOTE: An IT_EVENT is generated regardless of the selected functional mode. If no time-out is set and no more keys are pressed, the keyboard controller returns to IDLE state.

If long-key detection mode is set when the timer counts down the long-key delay, an interrupt long key (the KBD_IRQSTATUS[1] IT_LONG_KEY bit) is generated. If the repeat mode is set, the IT_LONG_KEY interrupt is generated periodically every long-key delay.

A time-out can also be set in event detection or long-key detection mode. In this case, a time-out interrupt (the KBD_IRQSTATUS[2] IT_TIMEOUT bit) is generated after the time-out delay timer expires. After such an interrupt, the keyboard controller always returns to IDLE state.

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NOTE: No time-out can be set in repeat mode. Only a keyboard event can stop the periodic interrupt generation.

26.4.6.4.2 Keyboard Buffer and Missed Events (Overrun Feature)

The keyboard controller has an overrun feature: A dedicated buffer allows the keyboard controller to memorize two successive events. If two successive events occur before a read is performed, the second event is stored and a second interrupt is generated when the first interrupt is cleared, allowing two consecutive key events to be received.

If a third event occurs before the first event is treated, a missed event interrupt (the KBD_IRQSTATUS[3] MISS_EVENT bit) is generated to report the lost event.

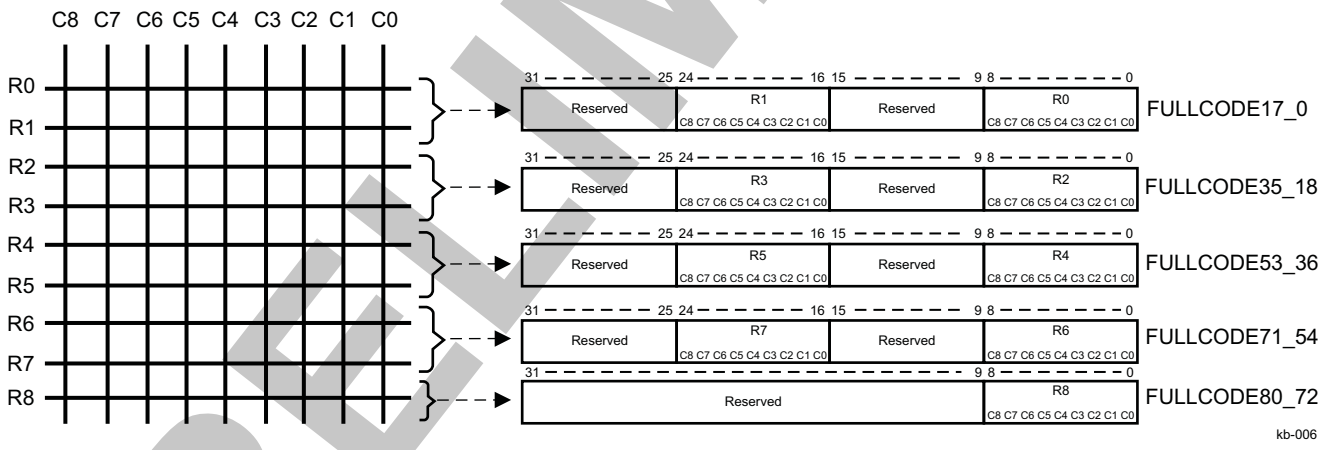
NOTE: The MISS_EVENT interrupt is not routed to the KBD_IRQ signal; software must check the KBD_IRQSTATUS[3] MISS_EVENT bit to detect any missed events.

26.4.7 Keyboard Controller Key Coding Registers

The keyboard controller matrix pressed keys state (indicating which columns/rows are connected) is reflected in the KBD_FULLCODE17_0 to KBD_FULLCODE80_72 registers, as shown in Figure 26-7. These registers are updated only when interrupt event status is inactive to prevent a lost event.

NOTE: The KBD_FULLCODE31_0 and KBD_FULLCODE63_32 registers, which are limited to supporting keyboards of a maximum 8 × 8 array size, can be used for back-to-back software compatibility.

Figure 26-7. Key Coding Registers



Each of the 9 × 9 keyboard size supporting registers (KBD_FULLCODE17_0 to KBD_FULLCODE71_54) stores the state of two keyboard rows. The KBD_FULLCODE80_72 register stores the state of the last row, R8:

- The KBD_FULLCODE17_0 register code rows 0, 1 (row 0 is coded between bits 0 and 8, row 1 is coded between bits 16 and 24)
- The KBD_FULLCODE35_18 register code rows 2, 3 (row 2 is coded between bits 0 and 8, row 3 is coded between bits 16 and 24)
- The KBD_FULLCODE53_36 register code rows 4, 5 (row 4 is coded between bits 0 and 8, row 5 is coded between bits 16 and 24)
- The KBD_FULLCODE71_54 register code rows 6, 7 (row 6 is coded between bits 0 and 8, row 7 is coded between bits 16 and 24)
- The KBD_FULLCODE80_72 register code row 8 (row 8 is coded between bits 0 and 8)

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In each of these registers (excluding KBD_FULLCODE80_72):

- Bit 0 corresponds to column(0) – row (i) key, … , bit 8 corresponds to column(8) – row (i) key.
- Bits from 9 to 15 are reserved.
- Bit 16 corresponds to column(0) – row (i + 1) key, … , bit 24 corresponds to column (8) – row (i + 1) key.
- Bits 31 to 25 are reserved, where i = 0, 2, 4, 6.

In the KBD_FULLCODE80_72 register, bit 0 corresponds to column (0) – row (8) key, …, the bit 8 corresponds to column (8) – row (8) key, and the remaining bits (from 9 to 31) are reserved.

Each of the 8 × 8-keyboard size supporting registers (KBD_FULLCODE31_0 and KBD_FULLCODE63_32) stores the state of four keyboard rows:

- The KBD_FULLCODE31_0 register code rows 0, 1, 2, and 3 (row 0 is coded between bits 0 and 7, row 1 is coded between bits 8 and 15, row 2 is coded between bits 16 and 23, and row 3 is coded between bits 24 and 31)
- The KBD_FULLCODE63_32 register code rows 4, 5, 6, and 7 (row 4 is coded between bits 0 and 7, row 5 is coded between bits 8 and 15, row 6 is coded between bits 16 and 23, and row 7 is coded between bits 24 and 31)

In these registers:

- KBD_FULLCODE31_0[0] corresponds to column (0) – row (0) key,…, KBD_FULLCODE31_0[7] corresponds to column (7) – row (0).
- KBD_FULLCODE31_0[8] corresponds to column (0) – row (1) key,..., KBD_FULLCODE31_0[15] corresponds to column (7) – row (1).
- KBD_FULLCODE31_0[16] corresponds to column (0) – row (2) key,..., KBD_FULLCODE31_0[23] corresponds to column (7) – row (2).
- KBD_FULLCODE31_0[24] corresponds to column (0) – row (3) key,..., KBD_FULLCODE31_0[31] corresponds to column (7) – row (3).
- KBD_FULLCODE63_32[0] corresponds to column (0) – row (4) key,..., KBD_FULLCODE63_32[7] corresponds to column (7) – row (4).
- KBD_FULLCODE63_32[8] corresponds to column (0) – row (5) key,..., KBD_FULLCODE63_32[15] corresponds to column (7) – row (5).
- KBD_FULLCODE63_32[16] corresponds to column (0) – row (6) key,..., KBD_FULLCODE63_32[23] corresponds to column (7) – row (6).
- KBD_FULLCODE63_32[24] corresponds to column (0) – row (7) key,..., KBD_FULLCODE63_32[31] corresponds to column (7) – row (7).

NOTE: The keyboard fullcode registers are not updated in software mode.

NOTE: When using a smaller keyboard (for example, 5 × 5 or 4 × 4), the bits of the unused columns/rows are not used.

26.4.8 Keyboard Controller Register Access

26.4.8.1 Write Registers Access

The keyboard module uses a posted-write scheme to update any internal registers. This means the write transaction is immediately acknowledged on the L4 interface, although the effective write operation occurs later due to a resynchronization in the functional clock domain. This has the advantage of not stalling the interconnect system or the CPU that requested the write transaction. For each functional register, a pending bit is provided that is set if there is a pending write access to this register. The pending bits are accessible in the keyboard pending write register (KBD_PENDING).

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In this mode, it is mandatory that the CPU checks the pending bits before any write access in the functional registers. If a write is attempted to a register with a previous access pending, the previous access is discarded without notice (this can also lead to unexpected results).

A register read following a posted write (on the same register) may not read the previous write value if the write posted process is not complete. Software synchronization must be used to avoid noncoherent read.

This posted period is defined as the interval between the posted write access request and the reset of the pending bit in the KBD_PENDING register, and can be quantified:

T (reset posted bit maximum) = 3 × Ticlk + 3 × Tfuncclk

The time it takes to accomplish the writing is:

T (write accomplish maximum) = 1 × Ticlk + 3 × Tfuncclk

where:

Ticlk is the L4 interface clock period, and Tfuncclk is the functional clock period.

26.4.8.2 Read Registers Access

The keyboard module uses a posted-read scheme for reading any internal register. The read transaction is immediately acknowledged on the L4 interface. The value of the functional register to be read must be previously synchronized. This has the advantage of not stalling the interconnect system or the CPU that requested the read transaction.

The posted-read scheme can be used only if Freq(KBD_FCLK) < Freq(KBD_ICLK)/4.

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26.5 Keyboard Controller Programming Guide

26.5.1 Keyboard Controller Low-Level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the module.

26.5.1.1 Global Initialization

26.5.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the keyboard module is to be used for the first time after a device reset. This initialization of surrounding modules is based on the integration and environment of the keyboard. For more information, see Section 26.2, *Keyboard Controller Environment,* and Section 26.3, *Keyboard Controller Integration*.

Table 26-11 describes the global initialization of surrounding modules.

Table 26-11. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	The module interface and functional clocks must be enabled. See Chapter 3, *Power, Reset, and Clock Management*.
Cortex-A15 MPU INTC	Interrupt request KBD_IRQ from the keyboard must be unmasked. For more information, see Section 17.1, *Interrupt Controllers Overview*.
Control module	The pad configuration registers must be configured to map the keyboard interface signals to the device pads to determine the signal directions and, for all keyboard rows, to enable the internal pull-ups of the associated IO cells. For more information about this configuration, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*.

26.5.1.1.2 Keyboard Controller Global Initialization

26.5.1.1.2.1 Main Sequence – Keyboard Controller Global Initialization

This procedure initializes the keyboard controller after a POR or software reset (see Table 26-12).

Table 26-12. Keyboard Controller Global Initialization

Step	Register/Bit Field/Programming Model	Value
Configure the debouncing time of filtering the glitches on pressing or releasing key.	KBD_DEBOUNCINGTIME[5:0] DEBOUNCING_VALUE	0x–
Configure the duration of a key press to allow shortcut detection (desired value of the long-key interrupt or repeat mode value).	KBD_KEYLONGTIME[11:0] LONG_KEY_VALUE	0x–
Configure the period of the long inactivity on the keyboard (desired value of the time-out interrupt).	KBD_TIMEOUT[15:0] TIMEOUT_VALUE	0x–
Define the logical value of the column outputs (KEYPAD configuration) (logical 0 bit = active column-row).	KBD_COLUMNOUTPUTS[8:0] KBC_REG	0x–
Perform the functional configuration of the keyboard module and the prescale clock timer value.	KBD_CTRL	0x00000–
Clear the interrupt-status register.	KBD_IRQSTATUS	0x0000000F
Enable (0b1)/disable (0b0) certain keyboard events for generating an interrupt request.	KBD_IRQENABLE_SET/KBD_IRQENABLE_CLR[2:0] IT_..._EN	0x–
Unmask (0b1)/mask (0b0) the expected source of wake-up event that generates a wake-up request.	KBD_IRQWAKEEN[2:0] WUP_..._ENA	0x–

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26.5.1.2 Operational Modes Configuration

26.5.1.2.1 Keyboard Controller in Hardware Decoding Mode (Default Mode)

26.5.1.2.1.1 Main Sequence – Keyboard Controller Hardware Mode

After reset, all available functional modes are disabled, except detect-event mode, which is always active. Table 26-13 describes the keyboard controller hardware mode.

Table 26-13. Keyboard Controller Hardware Mode

Step	Register/Bit Field/Programming Model	Value
Activate the internal keyboard controller sequencer by setting the bit.	KBD_CTRL[1] NSOFTWARE_MODE	0b1
Select the functional mode by setting its corresponding bit to 1.	KBD_CTRL[8:5]	0x–
Configure the duration of a key press to allow shortcut detection (desired value of the long-key interrupt or repeat mode value).	KBD_KEYLONGTIME[11:0] LONG_KEY_VALUE	0x–
Configure the period of the long inactivity on the keyboard (desired value of the time-out interrupt).	KBD_TIMEOUT[15:0] TIMEOUT_VALUE	0x–
Configure the debouncing time of filtering the glitches on pressing or releasing key.	KBD_DEBOUNCINGTIME[5:0] DEBOUNCING_VALUE	0x–
Clear the interrupt-status register.	KBD_IRQSTATUS	0x0000000F
Enable (by writing 1)/disable (by writing 0) certain keyboard event for generating an interrupt request	KBD_IRQENABLE_SET/KBD_IRQENABLE_CLR[2:0] IT_..._EN	0x–
Unmask (0b1)/mask (0b0) the expected source of wake-up event that generates a wake-up request.	KBD_IRQWAKEEN[2:0] WUP_..._ENA	0x–
Wait for the KBD_IRQ interrupt signal assertion.		
Read the interrupt-status register to determine which event caused the interrupt.	KBD_IRQSTATUS	
Read the KBD_FULLCODE17_0 to KBD_FULLCODE80_72 registers (or 8 × 8 keyboard-size-supporting KBD_FULLCODE31_0 and KBD_FULLCODE63_32 registers) to determine which key matrix combination was pressed.	KBD_FULLCODE17_0 [ROWi bits] (where i = 0 or 1) up to KBD_FULLCODE71_54 [ROWi bits] (where i = 6 or 7); KBD_FULLCODE80_72 [ROWi bits] (where i = 8); (or KBD_FULLCODE31_0[j] FULL_CODE_31_0 and KBD_FULLCODE63_32[k] FULL_CODE_63_32 bits (where j = 0 to 31, k = 32 to 63)	
Clear the corresponding bit(s) in the interrupt-status register by writing logical 1.	KBD_IRQSTATUS	0x1

NOTE: The long-key detection mode and the repeat mode cannot be used simultaneously, because they share the same interrupt status bit and are mutually exclusive. Software must ensure that only one of these modes at a time is selected.

NOTE: All interrupts are disabled on reset.

NOTE: When two events occur successively before the first event is read, the second interrupt is generated when the first interrupt is cleared. When more than two events in a row occur, the KBD_IRQSTATUS[3] MISS_EVENT bit is set. Software must check this bit, which is not reflected on the KBD_IRQ line.

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NOTE: The keyboard controller uses a posted-write scheme to update any internal register. Software must read the pending write status bits to ensure that the next write access is not discarded because of ongoing write synchronization. For more information, see Section 26.4.8.1, *Write Registers Access*.

26.5.1.2.2 Keyboard Controller Software Scanning Mode

26.5.1.2.2.1 Main Sequence – Keyboard Controller Software Mode

Table 26-14 describes the keyboard controller software mode.

Table 26-14. Keyboard Controller Software Mode

Step	Register/Bit Field/Programming Model	Value D
Deactivate the internal keyboard controller sequencer by clearing the bit.	KBD_CTRL[1] NSOFTWARE_MODE	0b0
Enable the interrupt event by setting the bit.	KBD_IRQENABLE_SET[0] IT_EVENT_EN	0b1
Wait for the KBD_CTL_IRQ interrupt signal assertion. Begin the software scan when the interrupt signal is asserted:		
1) Disable all columns to drive a logical 0 on the kbd_col[8:0] output by writing 0xFF. (logical 1 bit = inactive column-row)	KBD_COLUMNOUTPUTS[8:0] KBC_REG	0xFF
2) Drive kbd_col(i) output, (where i = 0 to 8), to 0 to capture a pressed-key-event, at the corresponding row input.	KBD_COLUMNOUTPUTS[i] KBC_REG (where i = 0 to 8)	0b0
3) Read the KBR_LATCH bit field of the KBD_ROWINPUTS register to determine which is the pressed key. IF: KBR_LATCH k-bit = 0 , where k = 0 to 8 Then, the corresponding k-row is connected to the column being enabled.	KBD_ROWINPUTS[8:0] KBR_LATCH	
END IF		
Repeat step 2) and step 3) for all existing columns.	KBD_IRQWAKEEN[2:0] WUP_..._ENA	0x–

NOTE: In software mode, during the manual keyboard scan, an interrupt is generated when a pressed key is detected.

26.5.1.2.3 Using the Timer

For information about programming the keyboard controller timer, see Section 26.4.6.2, *Keyboard Controller Timer*.

26.5.1.2.4 State-Machine Status Register

To see the state of the state-machine, see Section 26.4.6.3, *State-Machine Status*.

26.5.1.3 Keyboard Controller Events Servicing

Table 26-15 lists the keyboard controller event servicing.

Table 26-15. Keyboard Controller Event Servicing

Step	Register/ Bit Field / Programming Model	Value
Read the status register.	KBD_IRQSTATUS	
IF:	KBD_IRQSTATUS[2] IT_TIMEOUT	=1
Handle the timeout event.		

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Table 26-15. Keyboard Controller Event Servicing (continued)

Step	Register/ Bit Field / Programming Model	Value
Clear the corresponding status flag.	KBD_IRQSTATUS[2] IT_TIMEOUT	0x1
ELSE IF:	KBD_IRQSTATUS[1] IT_LONG_KEY	=1
Handle the long pressed key event.		
Clear the corresponding status flag.	KBD_IRQSTATUS[1] IT_LONG_KEY	0x1
ELSE IF:	KBD_IRQSTATUS[0] IT_EVENT	=1
Handle the pressed key event.		
Clear the corresponding status flag.	KBD_IRQSTATUS[0] IT_EVENT	0x1
ENDIF		
Disable the interrupts if needed.	KBD_IRQENABLE_CLR[2:0]	0x1

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26.6 Keyboard Controller Register Manual

26.6.1 Keyboard Controller Instance Summary

Table 26-16 summarizes the keyboard controller instances.

Table 26-16. Keyboard Controller Instance Summary

Module Name	Base Address	Size
KBD	0x4AE1 C000	4KB

26.6.2 Keyboard Controller Registers

26.6.2.1 Keyboard Controller Register Summary

Table 26-17 summarizes the keyboard controller register mapping.

Table 26-17. Keyboard Controller Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	KBD Base Address
KBD_REVISION	R	32	0x0000 0000	0x4AE1 C000
KBD_SYSCONFIG	RW	32	0x0000 0010	0x4AE1 C010
Reserved	R	32	0x0000 001C	0x4AE1 C01C
KBD_IRQSTATUS_RAW	RW	32	0x0000 0020	0x4AE1 C020
KBD_IRQSTATUS	RW	32	0x0000 0024	0x4AE1 C024
KBD_IRQENABLE_SET	RW	32	0x0000 0028	0x4AE1 C028
KBD_IRQENABLE_CLR	RW	32	0x0000 002C	0x4AE1 C02C
KBD_IRQWAKEEN	RW	32	0x0000 0030	0x4AE1 C030
KBD_PENDING	R	32	0x0000 0034	0x4AE1 C034
KBD_CTRL	RW	32	0x0000 0038	0x4AE1 C038
KBD_DEBOUNCINGTIME	RW	32	0x0000 003C	0x4AE1 C03C
KBD_KEYLONGTIME	RW	32	0x0000 0040	0x4AE1 C040
KBD_TIMEOUT	RW	32	0x0000 0044	0x4AE1 C044
KBD_STATEMACHINE	R	32	0x0000 0048	0x4AE1 C048
KBD_ROWINPUTS	R	32	0x0000 004C	0x4AE1 C04C
KBD_COLUMNOUTPUTS	RW	32	0x0000 0050	0x4AE1 C050
KBD_FULLCODE31_0	R	32	0x0000 0054	0x4AE1 C054
KBD_FULLCODE63_32	R	32	0x0000 0058	0x4AE1 C058
KBD_FULLCODE17_0	R	32	0x0000 005C	0x4AE1 C05C
KBD_FULLCODE35_18	R	32	0x0000 0060	0x4AE1 C060
KBD_FULLCODE53_36	R	32	0x0000 0064	0x4AE1 C064
KBD_FULLCODE71_54	R	32	0x0000 0068	0x4AE1 C068
KBD_FULLCODE80_72	R	32	0x0000 006C	0x4AE1 C06C

26.6.2.2 Keyboard Controller Register Description

Table 26-18. KBD_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4AE1 C000	**Instance**	KBD
Description	This register contains the IP revision code. A write to this register has no effect.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															

Bits	Field Name	Description	Type	Reset
31: 0	Reserved	IP Revision	R	0x1

Table 26-19. Register Call Summary for Register KBD_REVISION

Keyboard Controller Register Manual
- Keyboard Controller Register Summary: [0]

Table 26-20. KBD_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4AE1 C010	**Instance**	KBD
Description	This register controls the various parameters of the OCP interface		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										EMUFREE	IDLEMODE		RESERVED	SOFTRESET	RESERVED

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reads return 0.	R	0x000 0000
5	EMUFREE	Emulation mode 0x0: The KBDOCP module is frozen in emulation mode (PINSUSPENDN signal active). 0x1: The KBDOCP module runs free, regardless of PINSUSPENDN value.	RW	0
4:3	IDLEMODE	Power Management, req/ack control 0x0: Force-idle. An idle request is acknowledged unconditionally. 0x1: No-idle. An idle request is never acknowledged. 0x3: Reserved. Do not use. 0x2: Smart-idle. Acknowledgement to an idle request is given based on the internal activity of the module.	RW	0x0
2	RESERVED	Reads return 0.	R	0
1	SOFTRESET	Software reset. Write: initiate software reset Read: Reset done (0) / Reset ongoing (1) 0x0: Normal mode 0x1: The module is reset	RW	0
0	RESERVED	Reads return 0.	R	0

Table 26-21. Register Call Summary for Register KBD_SYSCONFIG

Keyboard Controller Functional Description
- Keyboard Controller Software Reset: [0] [1]
- Keyboard Controller Power Management: [2]

Keyboard Controller Register Manual
- Keyboard Controller Register Summary: [3]

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Table 26-22. KBD_IRQSTATUS_RAW

Address Offset	0x0000 0020		
Physical Address	0x4AE1 C020	**Instance**	KBD
Description	Per-event raw interrupt status vector Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MISS_EVENT	IT_TIMEOUT	IT_LONG_KEY	IT_EVENT

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads return 0	R	0x000 0000
3	MISS_EVENT	IRQ status for Miss event Read 0 : No event pending Write 0 : No action Read 1 : IRQ event pending Write 1 : Trigger IRQ event by software	RW	0
2	IT_TIMEOUT	IRQ status for Timeout Read 0 : No event pending Write 0 : No action Read 1 : IRQ event pending Write 1 : Trigger IRQ event by software	RW	0
1	IT_LONG_KEY	IRQ status for Long key Read 0 : No event pending Write 0 : No action Read 1 : IRQ event pending Write 1 : Trigger IRQ event by software	RW	0
0	IT_EVENT	IRQ status for Event Read 0 : No event pending Write 0 : No action Read 1 : IRQ event pending Write 1 : Trigger IRQ event by software	RW	0

Table 26-23. Register Call Summary for Register KBD_IRQSTATUS_RAW

Keyboard Controller Register Manual

- Keyboard Controller Register Summary: [0]

Table 26-24. KBD_IRQSTATUS

Address Offset	0x0000 0024		
Physical Address	0x4AE1 C024	**Instance**	KBD
Description	Per-event "enabled" interrupt status vector. Enabled status isn't set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled).		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MISS_EVENT	IT_TIMEOUT	IT_LONG_KEY	IT_EVENT

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads return 0	R	0x000 0000
3	MISS_EVENT	IRQ status for Miss event Read always returns zero Write 0 : No action Write 1 : Clear pending event, if any	RW	0
2	IT_TIMEOUT	IRQ status for Timeout Read 0 : No event pending Write 0 : No action Read 1 : IRQ event pending Write 1 : Clear pending event, if any	RW	0
1	IT_LONG_KEY	IRQ status for Long key Read 0 : No event pending Write 0 : No action Read 1 : IRQ event pending Write 1 : Clear pending event, if any	RW	0
0	IT_EVENT	IRQ status for Event Read 0 : No event pending Write 0 : No action Read 1 : IRQ event pending Write 1 : Clear pending event, if any	RW	0

Table 26-25. Register Call Summary for Register KBD_IRQSTATUS

Keyboard Controller Functional Description
- Keyboard Controller Interrupt Requests: [0] [1] [2] [3]
- Functional Modes: [4]
- Interrupt-Generation Scheme: [5] [6] [7] [8] [9] [10]
- Keyboard Buffer and Missed Events (Overrun Feature): [11] [12]

Keyboard Controller Programming Guide
- Keyboard Controller Global Initialization: [13]
- Keyboard Controller in Hardware Decoding Mode (Default Mode): [14] [15] [16] [17]
- Keyboard Controller Events Servicing: [18] [19] [20] [21] [22] [23] [24]

Keyboard Controller Register Manual
- Keyboard Controller Register Summary: [25]

Table 26-26. KBD_IRQENABLE_SET

Address Offset	0x0000 0028		
Physical Address	0x4AE1 C028	**Instance**	KBD
Description	Per-event interrupt enable bit vector Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													IT_TIMEOUT_EN	IT_LONG_KEY_EN	IT_EVENT_EN

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads return 0	R	0x0000 0000
2	IT_TIMEOUT_EN	IRQ enable for Timeout Read 0 : IRQ event is disabled Write 0 : No action Read 1 : IRQ event is enabled Write 1 : Set IRQ enable	RW	0
1	IT_LONG_KEY_EN	IRQ enable for Long key Read 0 : IRQ event is disabled Write 0 : No action Read 1 : IRQ event is enabled Write 1 : Set IRQ enable	RW	0
0	IT_EVENT_EN	IRQ enable for Event Read 0 : IRQ event is disabled Write 0 : No action Read 1 : IRQ event is enabled Write 1 : Set IRQ enable	RW	0

Table 26-27. Register Call Summary for Register KBD_IRQENABLE_SET

Keyboard Controller Functional Description
- Keyboard Controller Interrupt Requests: [0] [1] [2]
- Functional Modes: [3]
- Interrupt-Generation Scheme: [4] [5]

Keyboard Controller Programming Guide
- Keyboard Controller Global Initialization: [6]
- Keyboard Controller in Hardware Decoding Mode (Default Mode): [7]
- Keyboard Controller Software Scanning Mode: [8]

Keyboard Controller Register Manual
- Keyboard Controller Register Summary: [9]

Table 26-28. KBD_IRQENABLE_CLR

Address Offset	0x0000 002C		
Physical Address	0x4AE1 C02C	**Instance**	KBD
Description	Per-event interrupt enable bit vector Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													IT_TIMEOUT_EN	IT_LONG_KEY_EN	IT_EVENT_EN

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads return 0	R	0x0000 0000
2	IT_TIMEOUT_EN	IRQ enable for Timeout Read 0 : IRQ event is disabled Write 0 : No action Read 1 : IRQ event is enabled Write 1 : Clear IRQ enable	RW	0
1	IT_LONG_KEY_EN	IRQ enable for Long key Read 0 : IRQ event is disabled Write 0 : No action Read 1 : IRQ event is enabled Write 1 : Clear IRQ enable	RW	0
0	IT_EVENT_EN	IRQ enable for Event Read 0 : IRQ event is disabled Write 0 : No action Read 1 : IRQ event is enabled Write 1 : Clear IRQ enable	RW	0

Table 26-29. Register Call Summary for Register KBD_IRQENABLE_CLR

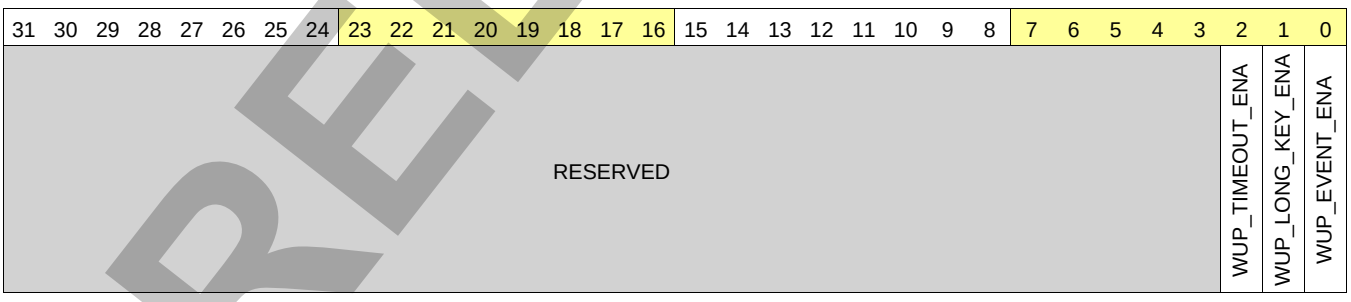
Keyboard Controller Functional Description
- Keyboard Controller Interrupt Requests: [0] [1] [2]
- Interrupt-Generation Scheme: [3]

Keyboard Controller Programming Guide
- Keyboard Controller Global Initialization: [4]
- Keyboard Controller in Hardware Decoding Mode (Default Mode): [5]
- Keyboard Controller Events Servicing: [6]

Keyboard Controller Register Manual
- Keyboard Controller Register Summary: [7]

Table 26-30. KBD_IRQWAKEEN

Address Offset	0x0000 0030		
Physical Address	0x4AE1 C030	**Instance**	KBD
Description	The Keyboard Wake-up Enable Register allows the user to mask the expected source of wake-up event that will generate a wake-up request. The KBD_IRQWAKEEN is programmed synchronously with the interface clock before any idle mode request comes from the host processor.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reads return 0.	R	0x0000 0000
2	WUP_TIMEOUT_ENA	Timeout wakeup enable. 0x0: Timeout wakeup generation disabled. 0x1: Timeout wakeup generation enabled.	RW	0
1	WUP_LONG_KEY_ENA	Long key wakeup enable. 0x0: Long key wakeup generation disabled. 0x1: Long key wakeup generation enabled.	RW	0

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Bits	Field Name	Description	Type	Reset
0	WUP_EVENT_ENA	Event wakeup enable. 0x0: Event wakeup generation disabled. 0x1: Event wakeup generation enabled.	RW	0

Table 26-31. Register Call Summary for Register KBD_IRQWAKEEN

Keyboard Controller Functional Description • Keyboard Controller Power Management: [0]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [1] • Keyboard Controller in Hardware Decoding Mode (Default Mode): [2] • Keyboard Controller Software Scanning Mode: [3]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [4] • Keyboard Controller Register Description: [5]

Table 26-32. KBD_PENDING

Address Offset	0x0000 0034		
Physical Address	0x4AE1 C034	**Instance**	KBD
Description	The software must read the pending write bits to insure that following write access will not be discarded due to on going write synchronization process. These bits are automatically cleared by internal logic when the write to the corresponding register is acknowledged.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												PEND_TIMEOUT	PEND_LONG_KEY	PEND_DEBOUNCING	PEND_CTRL

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads return 0.	R	0x000 0000
3	PEND_TIMEOUT	Write pending bit for KBD_TIMEOUT register Read 0x1: A write is pending to the KBD_TIMEOUT register Read 0x0: No write pending to the KBD_TIMEOUT register	R	0
2	PEND_LONG_KEY	Write pending bit for KBD_KEYLONGTIME register Read 0x1: A write is pending to the KBD_KEYLONGTIME register Read 0x0: No write pending to the KBD_KEYLONGTIME register	R	0
1	PEND_DEBOUNCING	Write pending bit for KBD_DEBOUNCINGTIME register Read 0x1: A write is pending to the KBD_DEBOUNCINGTIME register Read 0x0: No write pending to the KBD_DEBOUNCINGTIME register	R	0
0	PEND_CTRL	Write pending bit for KBD_CTRL register Read 0x1: A write is pending to the KBD_CTRL register Read 0x0: No write pending to the KBD_CTRL register	R	0

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Table 26-33. Register Call Summary for Register KBD_PENDING

Keyboard Controller Functional Description
- Write Registers Access: [0] [1]

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- Keyboard Controller Register Summary: [2]

Table 26-34. KBD_CTRL

Address Offset	0x0000 0038		
Physical Address	0x4AE1 C038	**Instance**	KBD
Description	This register sets the functional configuration of the module.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							REPEAT_MODE	TIMEOUT_LONG_KEY	TIMEOUT_EMPTY	LONG_KEY	PTV			NSOFTWARE_MODE	RESERVED

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reads return 0.	R	0x00 0000
8	REPEAT_MODE	Repeat mode enable. 0x0: Repeat mode detection disabled. 0x1: Repeat mode detection enabled.	RW	0
7	TIMEOUT_LONG_KEY	Timeout long key mode enable. 0x0: Timeout long key mode disabled. 0x1: Timeout long key mode enabled.	RW	0
6	TIMEOUT_EMPTY	Timeout empty mode enable. 0x0: Timeout long key mode disabled. 0x1: Timeout long key mode enabled.	RW	0
5	LONG_KEY	Long key mode enable. 0x0: Long key mode disabled. 0x1: Long key mode enabled.	RW	0
4:2	PTV	Pre-scale clock timer value.	RW	0x7
1	NSOFTWARE_MODE	Select hardware or software mode for key decoding. 0x0: Enable software mode. 0x1: Enable hardware decoding using internal sequencer.	RW	1
0	RESERVED	Reads return 0.	R	0

Table 26-35. Register Call Summary for Register KBD_CTRL

Keyboard Controller Functional Description
- Keyboard Controller Software Mode: [0]
- Functional Modes: [1] [2] [3] [4] [5] [6] [7]
- Keyboard Controller Timer: [8] [9] [10] [11] [12]

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- Keyboard Controller Global Initialization: [13]
- Keyboard Controller in Hardware Decoding Mode (Default Mode): [14] [15]
- Keyboard Controller Software Scanning Mode: [16]

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Table 26-35. Register Call Summary for Register KBD_CTRL (continued)

Keyboard Controller Register Manual • Keyboard Controller Register Summary: [17] • Keyboard Controller Register Description: [18] [19] [20]

Table 26-36. KBD_DEBOUNCINGTIME

Address Offset	0x0000 003C		
Physical Address	0x4AE1 C03C	**Instance**	KBD
Description	This register is used to filter glitches on the press key or release key.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEBOUNCING_VALUE							

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reads return 0.	R	0x000 0000
5:0	DEBOUNCING_VALUE	This value correspond to the desired value of debouncing time.	RW	0x00

Table 26-37. Register Call Summary for Register KBD_DEBOUNCINGTIME

Keyboard Controller Functional Description • Keyboard Controller Timer: [0] [1] [2] [3] [4] [5]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [6] • Keyboard Controller in Hardware Decoding Mode (Default Mode): [7]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [8] • Keyboard Controller Register Description: [9] [10] [11]

Table 26-38. KBD_KEYLONGTIME

Address Offset	0x0000 0040		
Physical Address	0x4AE1 C040	**Instance**	KBD
Description	This register is used to measure duration of a key press, to allow, shortcut detection.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				LONG_KEY_VALUE											

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reads return 0.	R	0x0 0000
11:0	LONG_KEY_VALUE	This value correspond to the desired value of the long key interrupt or repeat mode value.	RW	0x000

Table 26-39. Register Call Summary for Register KBD_KEYLONGTIME

Keyboard Controller Functional Description • Keyboard Controller Timer: [0] [1] [2] [3] [4] [5] [6] [7] [8]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [9] • Keyboard Controller in Hardware Decoding Mode (Default Mode): [10]

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Table 26-39. Register Call Summary for Register KBD_KEYLONGTIME (continued)

Keyboard Controller Register Manual • Keyboard Controller Register Summary: [11] • Keyboard Controller Register Description: [12] [13] [14]

Table 26-40. KBD_TIMEOUT

Address Offset	0x0000 0044		
Physical Address	0x4AE1 C044	**Instance**	KBD
Description	This register is used to detect a long inactivity on the keyboard.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TIMEOUT_VALUE															

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reads return 0.	R	0x0000
15:0	TIMEOUT_VALUE	This value correspond to the desired value of the time out interrupt.	RW	0x0000

Table 26-41. Register Call Summary for Register KBD_TIMEOUT

Keyboard Controller Functional Description • Keyboard Controller Timer: [0] [1] [2] [3] [4] [5] [6]
Keyboard Controller Programming Guide • Keyboard Controller Global Initialization: [7] • Keyboard Controller in Hardware Decoding Mode (Default Mode): [8]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [9] • Keyboard Controller Register Description: [10] [11] [12]

Table 26-42. KBD_STATEMACHINE

Address Offset	0x0000 0048		
Physical Address	0x4AE1 C048	**Instance**	KBD
Description	This register indicates the state of the sequencer.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												STATE_MACHINE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reads return 0	R	0x000 0000
3:0	STATE_MACHINE	The state of internal state machine.	R	0x0

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Table 26-43. Register Call Summary for Register KBD_STATEMACHINE

Keyboard Controller Functional Description
• State-Machine Status: [0]
Keyboard Controller Register Manual
• Keyboard Controller Register Summary: [1]

Table 26-44. KBD_ROWINPUTS

Address Offset	0x0000 004C		
Physical Address	0x4AE1 C04C	**Instance**	KBD
Description	This register stores the value of the rows input.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								KBR_LATCH							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reads return 0.	R	0x00 0000
8:0	KBR_LATCH	The value of the rows input.	R	0x000

Table 26-45. Register Call Summary for Register KBD_ROWINPUTS

Keyboard Controller Functional Description
• Keyboard Controller Software Mode: [0] [1]
Keyboard Controller Programming Guide
• Keyboard Controller Software Scanning Mode: [2] [3]
Keyboard Controller Register Manual
• Keyboard Controller Register Summary: [4]

Table 26-46. KBD_COLUMNOUTPUTS

Address Offset	0x0000 0050		
Physical Address	0x4AE1 C050	**Instance**	KBD
Description	This register holds the value of the columns output.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								KBC_REG							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reads return 0.	R	0x00 0000
8:0	KBC_REG	The value of the columns output.	RW	0x000

Table 26-47. Register Call Summary for Register KBD_COLUMNOUTPUTS

Keyboard Controller Functional Description
• Keyboard Controller Block Diagram: [0]
• Keyboard Controller Software Mode: [1]
Keyboard Controller Programming Guide
• Keyboard Controller Global Initialization: [2]
• Keyboard Controller Software Scanning Mode: [3] [4]
Keyboard Controller Register Manual
• Keyboard Controller Register Summary: [5]

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Table 26-48. KBD_FULLCODE31_0

Address Offset	0x0000 0054		
Physical Address	0x4AE1 C054	**Instance**	KBD
Description	The KBD_FULLCODE31_0 register codes the row 0, row 1, row 2 and row 3		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FULL_CODE_31_0																															

Bits	Field Name	Description	Type	Reset
31:0	FULL_CODE_31_0	A bit at one indicate that the corresponding key is pressed.	R	0x0000 0000

Table 26-49. Register Call Summary for Register KBD_FULLCODE31_0

Keyboard Controller Functional Description
- Keyboard Controller Key Coding Registers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]

Keyboard Controller Programming Guide
- Keyboard Controller in Hardware Decoding Mode (Default Mode): [11] [12]

Keyboard Controller Register Manual
- Keyboard Controller Register Summary: [13]
- Keyboard Controller Register Description: [14]

Table 26-50. KBD_FULLCODE63_32

Address Offset	0x0000 0058		
Physical Address	0x4AE1 C058	**Instance**	KBD
Description	The KBD_FULLCODE63_32 register codes the row 4, row 5, row 6 and row 7.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FULL_CODE_63_32																															

Bits	Field Name	Description	Type	Reset
31:0	FULL_CODE_63_32	A bit at one indicate that the corresponding key is pressed.	R	0x0000 0000

Table 26-51. Register Call Summary for Register KBD_FULLCODE63_32

Keyboard Controller Functional Description
- Keyboard Controller Key Coding Registers: [0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10]

Keyboard Controller Programming Guide
- Keyboard Controller in Hardware Decoding Mode (Default Mode): [11] [12]

Keyboard Controller Register Manual
- Keyboard Controller Register Summary: [13]
- Keyboard Controller Register Description: [14]

Table 26-52. KBD_FULLCODE17_0

Address Offset	0x0000 005C		
Physical Address	0x4AE1 C05C	**Instance**	KBD
Description	The KBD_FULLCODE17_0 register codes the row 0 and row 1. The row 0 is coded between bit 0 and 8, the row 1 is coded between bit 24 and		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ROW1								RESERVED								ROW0							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:16	ROW1	A bit at one indicate that the corresponding key is pressed.	R	0x000
15:9	RESERVED		R	0x00
8:0	ROW0	A bit at one indicate that the corresponding key is pressed.	R	0x000

Table 26-53. Register Call Summary for Register KBD_FULLCODE17_0

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0] [1] [2]
Keyboard Controller Programming Guide • Keyboard Controller in Hardware Decoding Mode (Default Mode): [3] [4]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [5] • Keyboard Controller Register Description: [6]

Table 26-54. KBD_FULLCODE35_18

Address Offset	0x0000 0060		
Physical Address	0x4AE1 C060	**Instance**	KBD
Description	The KBD_FULLCODE35_18 register codes the row 2 and row 3. The row 2 is coded between bit 0 and 8, the row 3 is coded between bit 24 and 16		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ROW3								RESERVED								ROW2							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:16	ROW3	A bit at one indicate that the corresponding key is pressed.	R	0x000
15:9	RESERVED		R	0x00
8:0	ROW2	A bit at one indicate that the corresponding key is pressed.	R	0x000

Table 26-55. Register Call Summary for Register KBD_FULLCODE35_18

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [1] • Keyboard Controller Register Description: [2]

Table 26-56. KBD_FULLCODE53_36

Address Offset	0x0000 0064		
Physical Address	0x4AE1 C064	**Instance**	KBD
Description	The KBD_FULLCODE53_36 register codes the row 4 and row 5. The row 4 is coded between bit 0 and 8, the row 5 is coded between bit 24 and 16.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ROW5								RESERVED								ROW4							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:16	ROW5	A bit at one indicate that the corresponding key is pressed.	R	0x000
15:9	RESERVED		R	0x00
8:0	ROW4	A bit at one indicate that the corresponding key is pressed.	R	0x000

Table 26-57. Register Call Summary for Register KBD_FULLCODE53_36

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [1] • Keyboard Controller Register Description: [2]

Table 26-58. KBD_FULLCODE71_54

Address Offset	0x0000 0068		
Physical Address	0x4AE1 C068	**Instance**	KBD
Description	The KBD_FULLCODE71_54 register codes the row 6 and row 7. The row 0 is coded between bit 0 and 8, the row 1 is coded between bit 24 and 16		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ROW7								RESERVED								ROW6							

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24:16	ROW7	A bit at one indicate that the corresponding key is pressed.	R	0x000
15:9	RESERVED		R	0x00
8:0	ROW6	A bit at one indicate that the corresponding key is pressed.	R	0x000

Table 26-59. Register Call Summary for Register KBD_FULLCODE71_54

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0] [1]
Keyboard Controller Programming Guide • Keyboard Controller in Hardware Decoding Mode (Default Mode): [2]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [3] • Keyboard Controller Register Description: [4]

Table 26-60. KBD_FULLCODE80_72

Address Offset	0x0000 006C		
Physical Address	0x4AE1 C06C	**Instance**	KBD
Description	The KBD_FULLCODE80_72 register codes the row 8. The row 8 is coded between bit 0 and 8.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ROW8							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00 0000
8:0	ROW8	A bit at one indicate that the corresponding key is pressed.	R	0x000

Table 26-61. Register Call Summary for Register KBD_FULLCODE80_72

Keyboard Controller Functional Description • Keyboard Controller Key Coding Registers: [0] [1] [2] [3] [4]
Keyboard Controller Programming Guide • Keyboard Controller in Hardware Decoding Mode (Default Mode): [5] [6]
Keyboard Controller Register Manual • Keyboard Controller Register Summary: [7] • Keyboard Controller Register Description: [8]

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Shared PHY Component Subsystems

This chapter describes the shared PHY component subsystems of the device.

NOTE: The following naming rule is applied across the chapter:

- RXP/ RXN and TXP/ TXN naming is used at SATA PHY and USB3 PHY module level
- rx/ry and tx/ty naming is used at device level

where:

RXP corresponds to sata_rx / usbd0_ss_rx.
RXN corresponds to sata_ry / usbd0_ss_ry.
TXP corresponds to sata_tx / usbd0_ss_tx.
TXN corresponds to sata_ty / usbd0_ss_ty.

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27.2 USB3 PHY Subsystem 5853
27.3 USB3 PHY and SATA PHY PLL Controllers Register Manual 5874

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27.1 SATA PHY Subsystem

This chapter describes the features and functions of the serial advanced technology attachment (SATA) PHY subsystem of the device.

27.1.1 SATA PHY Subsystem Overview

The physical layer (PHY) is responsible for transmitting and receiving the parallel 8b/10b encoded information as a serial data stream on the wire.

The SATA host controller subsystem instantiates a single serializer (transmitter), SATA_PHY_TX, and a single deserializer (receiver), SATA_PHY_RX. Together the transmitter and receiver are also signified as SATA_PHY throughout this chapter. The role of the TX and RX components is to adapt SATA Link parallel 10-bit input/output (I/O) data stream for a serialized differential transmission and reception over SATA electrical interface, respectively.

The high speed transmission clock is generated by and integrated into the SATA host subsystem dpll (DPLL_SATA).

The DPLL_SATA is configured and controlled through a SATA dedicated PLL controller (PLLCTRL_SATA) with associated registers, accessible over a L4_CFG interface adapter.

The components (SATA_PHY_RX, SATA_PHY_TX, DPLL_SATA, PLLCTRL_SATA, and PLLCTRL_SATA L4-interface adapter) build the SATA PHY subsystem. This subsystem is responsible for PHY components clock generation and physical layer transmission/reception within the device SATA subsystem.

Figure 27-1 gives an overview of the SATA PHY subsystem. As shown in Figure 27-1, at one side the SATA_PHY components directly interface the attached to host controller SATA mass storage device (over TXP/TXN transmission and RXP/RXN reception interface I/Os) and on the other side they interface the SATA controller, described in detail in Section 23.12, *SATA Controller*.

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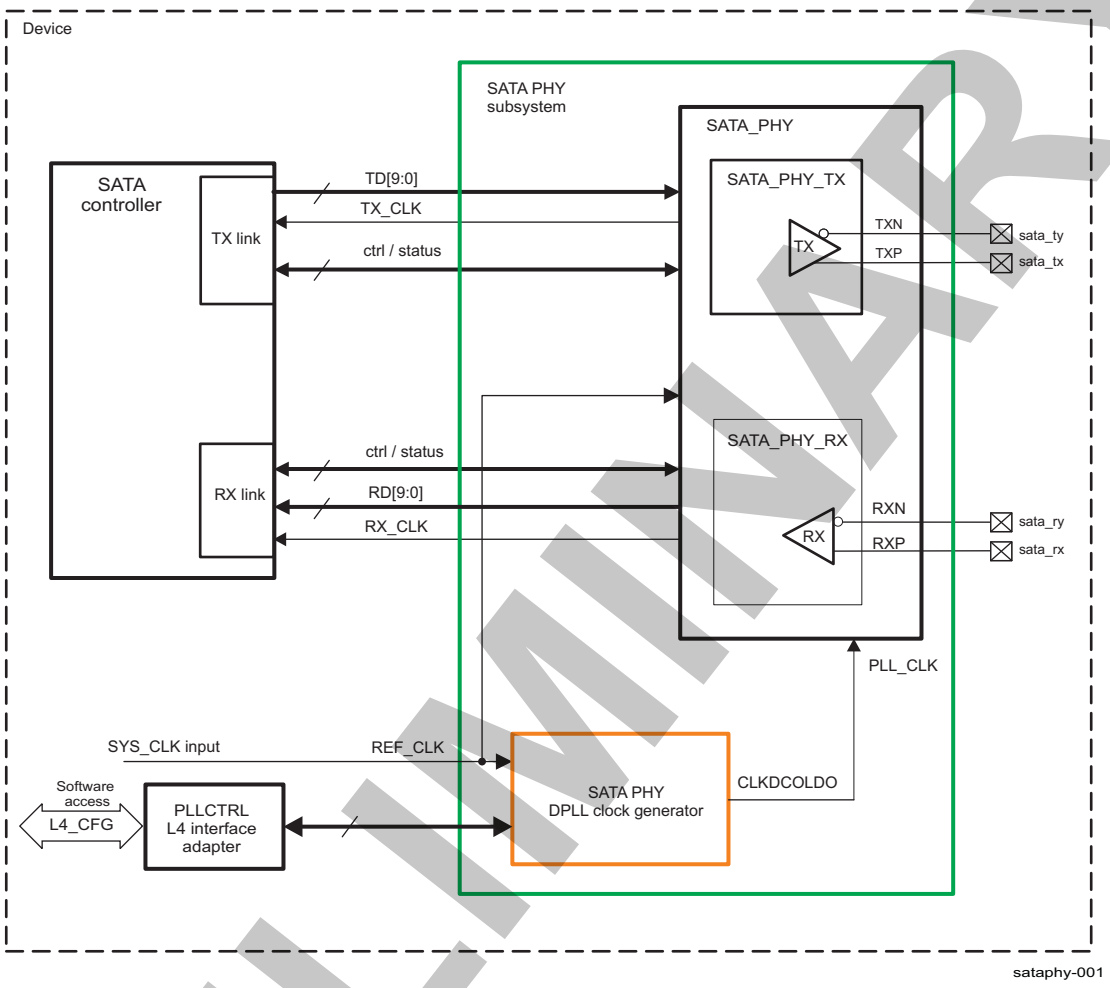
Figure 27-1. SATA PHY Subsystem Overview



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27.1.2 SATA PHY Subsystem Environment

27.1.2.1 SATA PHY I/O Signals

Table 27-1 lists the module pins and their corresponding signal names at the device level, and also specifies their links to functions.

Table 27-1. SATA PHY I/O Signals

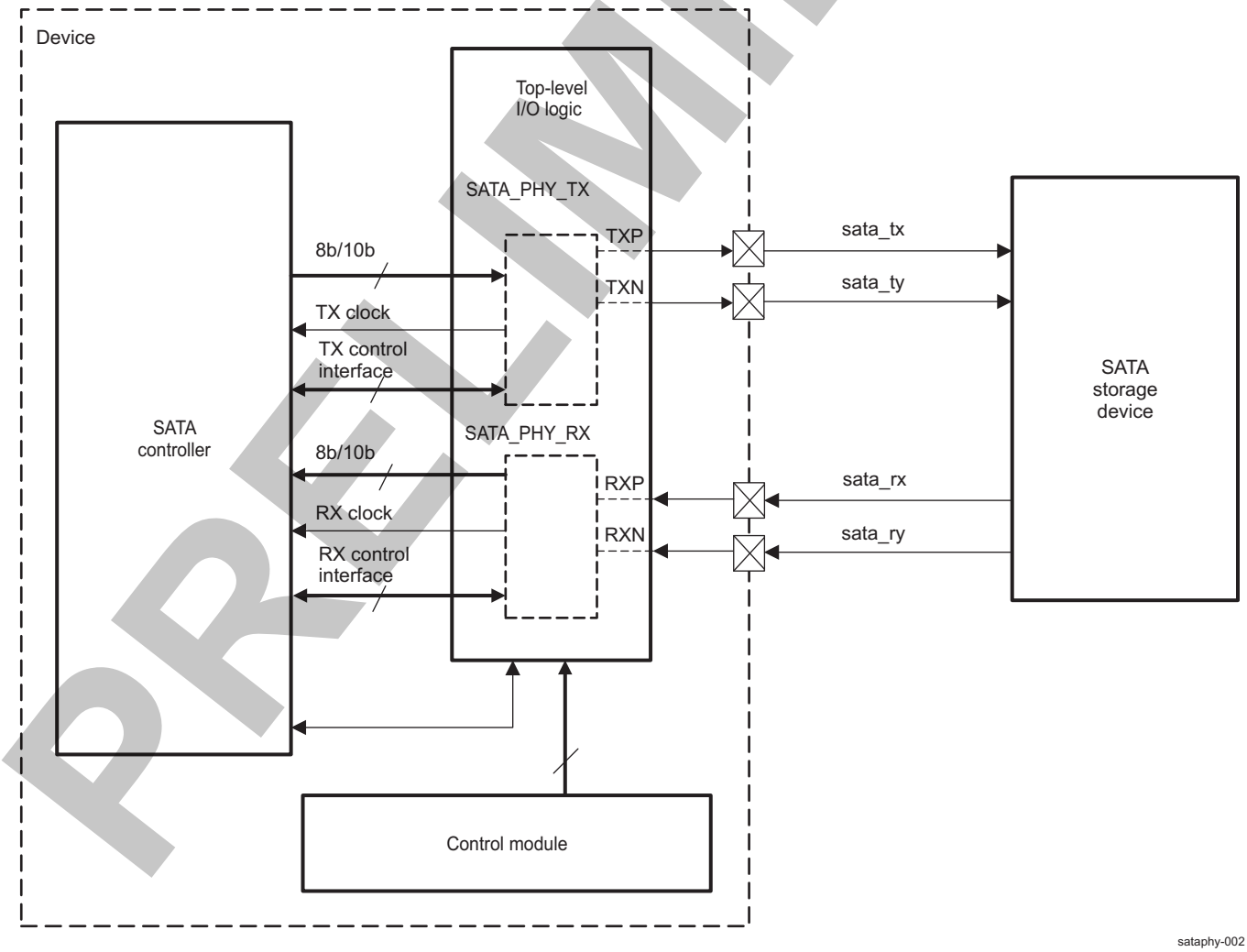
Module Pin Name	Device Level Signal Name	I/O[1]	Description	Module Pin Reset Value
TXP[2]	sata_tx	O	TX output of the SATA PHY differential transmission line	0
TXN[2]	sata_ty	O	TY output of the SATA PHY differential transmission line	0
RXP[2]	sata_rx	I	RX input of the SATA PHY differential reception line	HiZ
RXN[2]	sata_ry	I	RY input of the SATA PHY differential reception line	HiZ

(1) I = Input; O = Output

(2) The SATA PHY subsystem signals that implement the physical interface with an external SATA storage device.

Figure 27-2 shows module pin signals mapping to SATA PHY I/O signals visible at device pad level.

Figure 27-2. SATA PHY I/O Signals



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NOTE: The path from module pin to device pad(s) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and is programmable in the control module registers. See Section 18.4.8, *Pad Functional Multiplexing and Configuration* and Section 18.4.12.7.5, *Device Interfaces Signal Group Controls Mapping* in Chapter 18, *Control Module*, for more information.

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27.1.3 SATA PHY Subsystem Integration

This section describes the SATA PHY subsystem-related components (SATA_PHY, DPLL_SATA, PLLCTRL_SATA, OCP2SPC3) integration in the device, including information about clocks, resets, and hardware requests.

Figure 27-3 shows the SATA_PHY integration.

The SATA_PHY module integration features are:

- A low-power nonretention reset, L3INIT_RST
- A DPLL reference input clock, PLL_CLK
- Parallel 10-bit TD[9:0] (SATA_PHY_TX) and 10-bit RD[9:0] (SATA_PHY_RX) data interfaces to SATA controller
- TX_CLK output clock for the parallel TX data interface between SATA_PHY.SATA_PHY_TX and SATA controller
- RX_CLK output clock for the parallel RX data interface between SATA_PHY.SATA_PHY_RX and SATA controller
-
- REF_CLK clock input (SATA_REF_GFCLK)
- A device core control module command port to the SATA_PHY integrated power sequencer

The DPLL_SATA integration features are:

- A low-power nonretention reset, L3INIT_RST
- A power, reset, and clock management (PRCM) gated version of SYS_CLK (SATA_REF_GFCLK) supplying the DPLL_SATA.CLKINP pin
- A single high-frequency clock output (DPLL_SATA.CLKDCOLDO to the SATA_PHY TX/RX components)
- No high-speed (HS) divider integration
- Idle signaling implementation
- LDO and DCO PWRDNZ monitoring signals
- A DPLL_LOCK locked status indication output to SATA_PHY and the SATA controller

The PLLCTRL_SATA integration features are:

- A low-power nonretention reset, L3INIT_RST
- (OCP2SPC3) Interconnect adapter target interface
- Configuration/control programming interface to the DPLL_SATA
- No direct gate control for DPLL_SATA.CLKINP and CLKDCOLDO

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Figure 27-3. SATA PHY Subsystem Integration

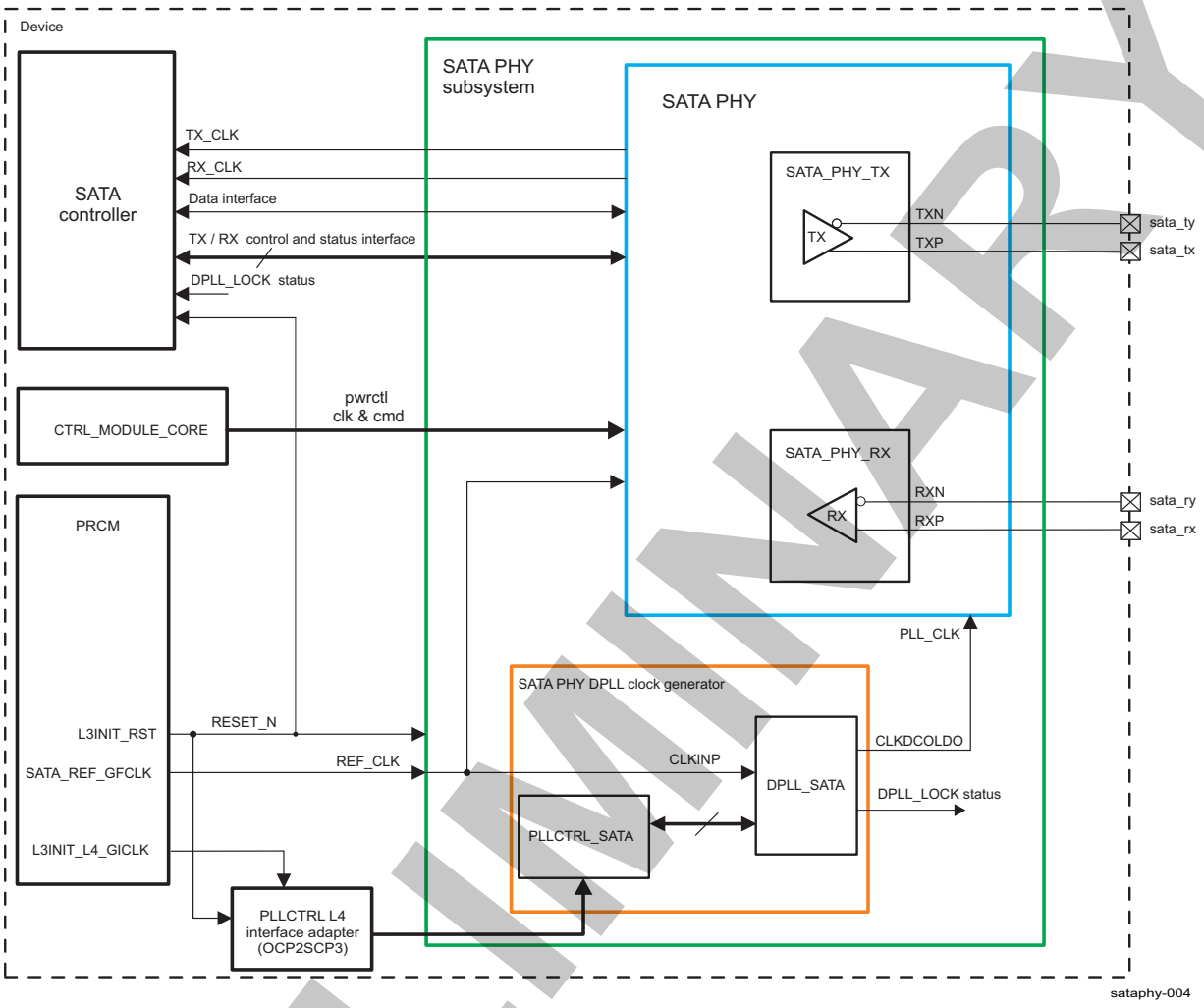

Table 27-2 through Table 27-4 summarize the integration of the module in the device.

Table 27-2. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
PLLCTRL_SATA	PD_L3INIT	OCP2SCP3 adapter SCP interconnects
DPLL_SATA		
OCP2SCP3		L4_CFG

Table 27-3. Clocks

Clocks				
Module Instance	Destination Signal Name	Source Signal Name	Source	Description
DPLL_SATA / SATA_PHY	REF_CLK	SATA_REF_GFCLK	PRCM	SATA DPLL and SATA PHY reference functional clock (SYS_CLK)
OCP2SCP3	L4CFG_ADAPTER_CLKIN	L3INIT_L4_GICLK	PRCM	PHY / DPLL L4_CFG adapter interface clock

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Table 27-4. Resets

Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
SATA_PHY subsystem	RESET_N	L3INIT_RST	PRCM	A nonretention reset to all SATA_PHY subsystem components

NOTE: The SATA_PHY, DPLL_SATA, and PLLCTRL_SATA modules do not generate DMA, interrupt, or wakeup hardware requests to the surrounding modules integrated in the device.

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27.1.4 SATA PHY Subsystem Functional Description

27.1.4.1 SATA PLL Controller L4 Interface Adapter Functional Description

The L4_CFG interconnect adapter (OCP2SCP3), allows user software to configure the PLLCTRL_SATA registers over the L4_CFG port. Hence it is expected that this adapter is configured to operate before any programming of the PLLCTRL_SATA.

Before initiating any software reset to this adapter, a value >= 0x6 should be written to the register bitfield OCP2SCP_TIMING[3:0] SYNC2.

L4_CFG interconnect adapter software reset is performed via writing OCP2SCP_SYSCONFIG[1] SOFTRESET to 0b1. The software reset completion is observed in bit OCP2SCP_SYSSTATUS[0] RESETDONE.

By default a smart-idle power mode is selected for OCP2SCP3. The smart-idle mode supported by OCP2SCP3 is not wake-up capable, which means software must explicitly take care to wake the OCP2SCP3 by setting the OCP2SCP_SYSCONFIG [4:3] IDLEMODE bit field to 0x1 (no idle), once it has previously gone to an idle mode.

By default OCP2SCP_SYSCONFIG[0] AUTOIDLE =0x1, which defines that the PLLCTRL L4 interface adapter automaticaly gates its L4 input clock based on L4_CFG interconnect activity. To enable a free-running clock, one should set bit AUTOIDLE to 0x0.

27.1.4.2 SATA PHY Serializer and Deserializer Functional Descriptions

27.1.4.2.1 SATA PHY Reset

No software reset is applicable to SATA_PHY. L3INIT reset assertion is automatically managed by hardware.

27.1.4.2.2 SATA_PHY Clocking

27.1.4.2.2.1 SATA_PHY Input Clocks

A standard high-speed 1.5 GHz input clock of SATA_PHY is provided by the DPLL_SATA.CLKDCOLDO output. PRCM. SATA_REF_GFCLK (derived from the SYS_CLK) should be enabled, to provide the necessary DPLL_SATA and SATA_PHY clocking within the SATA subsystem.

Depending on the SATA_REF_GFCLK (SYS_CLK derived) frequency, following settings should be made in the CTRL_MODULE_CORE.CONTROL_PHY_POWER_SATA[31:22] SATA_PWRCTL_CLK_FREQ bitfield for proper operation:

- 0x26: If SYSCLK = 38.4 MHz
- 0x1A: If SYSCLK = 26.0 MHz
- 0x13: If SYSCLK = 19.2 MHz
- 0x10: If SYSCLK = 16.8 MHz
- 0x0C: If SYSCLK = 12.0 MHz

27.1.4.2.2.2 SATA_PHY Output Clocks

The 10-bit data parallelly transmitted data between SATA_PHY_TX and SATA controller link logic is sampled with respect to the TX_CLK. Frequency of this clock is obtained as the SATA_PHY.PLL_CLK clock frequency:

- Divided by 10 if a 1.5-Gbps limit is negotiated by software setting DWC_ahsata.SATA_PxSCTL[7:4] SPD = 0x1
- Divided by 5 if a 3-Gbps limit is negotiated by software setting DWC_ahsata.SATA_PxSCTL[7:4] SPD = 0x0 or 0x2

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The actually negotiated between host and the attached SATA device speed is indicated in the read-only SATA controller.SATA_PxSSTS[7:4] SPD bit field. For more information, see Section 23.12.6, *SATA Controller Register Manual*, in Section 23.12, *SATA Controller*.

RX_CLK: The SATA_PHY_RX output RX_CLK is a clock that is recovered from the serial data received over the RXP/RXN lines serial data. The RX_CLK clock supplies the SATA controller link parallel 10-bit data reception logic.

27.1.4.2.3 SATA_PHY Power Management

The SATA_PHY power sequencer receives a power-up/power-down command input from the device general core control module. The power sequencer takes care to execute different stages of the SATA_PHY_TX and SATA_PHY_RX power-up/-down processes. Besides a power-up/-down functionality, the SATA PHY accepts power transition commands/states (Ready state, Partial or Slumber states) from the SATA controller link power management port .

27.1.4.2.3.1 SATA_PHY Power-Up/-Down Sequences

Powering up/down the SATA_PHY_TX and SATA_PHY_RX modules is triggered by software writing corresponding power-up/-down commands in the CTRL_MODULE_CORE.CONTROL_PHY_POWER_SATA register of the device core control module, as follows:

- CONTROL_PHY_POWER_SATA[21:14] SATA_PWRCTL_CLK_CMD = 0x0 (default value), commands both SATA_PHY_TX and SATA_PHY_RX to power-down (OFF) state.
- CONTROL_PHY_POWER_SATA[21:14] SATA_PWRCTL_CLK_CMD = 0x1, powers up the SATA_PHY_RX only.
- CONTROL_PHY_POWER_SATA[21:14] SATA_PWRCTL_CLK_CMD = 0x2, powers up the SATA_PHY_TX only.
- CONTROL_PHY_POWER_SATA[21:14] SATA_PWRCTL_CLK_CMD = 0x3, simultaneously powers up the SATA_PHY_RX and the SATA_PHY_TX.

For more information, see Chapter 18, *Control Module*.

27.1.4.2.3.2 SATA_PHY Low-Power Modes

Setting the DWC_ahsata.SATA_PxSCTL[3:0] DET bit field to 0x4 automatically puts the SATA_PHY_RX deserializer in offline mode. This software operation has no impact over the SATA_PHY_TX serializer.

NOTE: The SATA controller transition to partial or slumber mode has no impact over the SATA_PHY_RX deserializer.

NOTE: The SATA_PHY_TX.TX_CLK output clock is a free-running clock and cannot be gated, even when the transmitter is disabled by a SATA controller.

27.1.4.2.4 SATA_PHY Hardware Requests

No DMA, interrupt or wake-up requests are generated by the SATA_PHY to the surrounding SATA controller subsystem components.

27.1.4.3 SATA Clock Generator Subsystem Functional Description

The DPLL_SATA, which is located outside the PRCM boundaries and is part of the SATA host controller subsystem, directly injects a high-speed clock into the SATA_PHY serializer/deserializer input, PLL_CLK. The DPLL generator is controlled through a programmable interface from a dedicated PLL controller, PLLCTRL_SATA.

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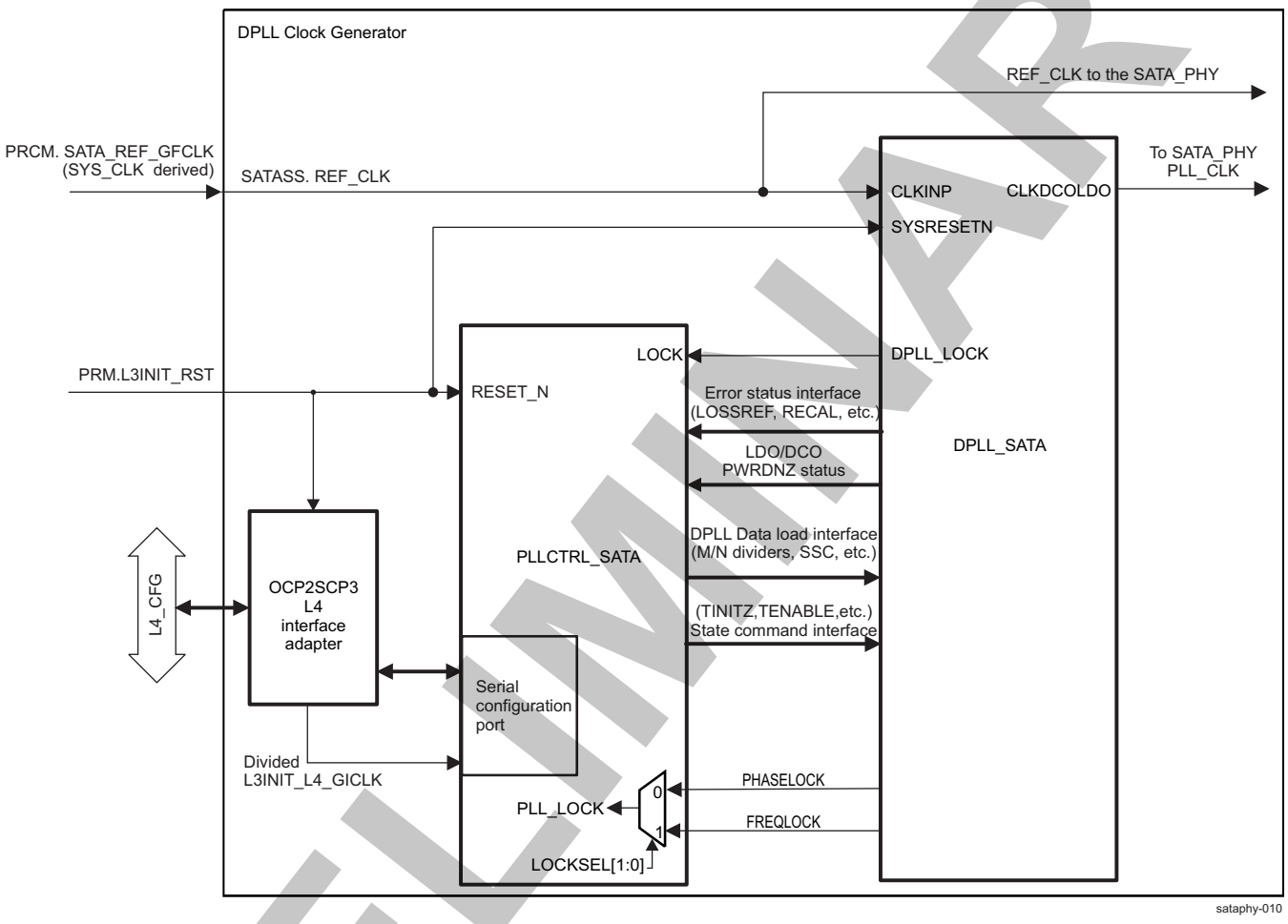
27.1.4.3.1 SATA DPLL Clock Generator Overview

The SCP interface of the SATA PLL controller (the PLLCTRL_SATA instance) is used to set the configuration of the digital phase-locked loop (DPLL) modules, primarily the various counter values. Figure 27-4 is an overview of the DPLL clock generator embedded into the SATA host controller subsystem.

Figure 27-4. SATA DPLL Clock Generator Overview



NOTE: The PLLCTRL_SATA module is user accessible on the L4_CFG interconnect. However, to make access possible, the user must configure the OCP2SCP3 instance prior to accessing the PLLCTRL_SATA registers.

The DPLL_SATA features are:

- A programmable 8-bit input divider: N
- A programmable 12-bit integer, 18-bit fractional loop multiplier: M
- Digital control and loop filter
- Internal oscillator output clock on internal LDO domain (CLKDCOLDO output)
- DPLL output clock spread spectrum clocking (SSC) support
- No retention capabilities
- No idle-bypass fast relock capabilities
- Idle-bypass low-power mode
- M/N bypass mode

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- Relock from standby

The PLLCTRL_SATA components features are:

- DPLL error and status notification
- DPLL initialization and configuration
- DPLL lock criteria selectable between frequency and phase lock
- Idle command implementation
- No software reset implementation

27.1.4.3.2 SATA DPLL Clock Generator Reset

The SATA PLL controller and SATA DPLL clock generator share a common hardware nonretention reset (L3INIT_RST) which comes from the device power and reset manager. When the DPLL_SATA hardware reset completes, the PLLCTRL_SATA.PLL_STATUS[0] PLLCTRL_RESET_DONE bit is automatically updated to 1. For more information on the hardware reset source, see Section 3.5.4, *Reset Domains*, in Chapter 3, *Power, Reset, and Clock Management*.

The PLLCTRL_SATA itself has no software reset capabilities.

The PLLCTRL_SATA performs a software reset sequence on the DPLL_SATA in hardware (through the TINITZ signal activation).

27.1.4.3.3 SATA DPLL Low-Power Modes

The power-management port (PMP) is not integrated for PLLCTRL_SATA. The DPLL_SATA has no retention capabilities. This means the DPLL digital power supply remains switched on during all modes of operation.

The low-power (LP) modes supported by DPLL_SATA are idle-bypass low power and MN-bypass modes, which are both characterized by:

- Internal LDO switched off
- DCO oscillator switched off
- CLKDCOLDO output pulled low

For more details on the PLL settings and conditions necessary to enter idle-bypass and MN-bypass low-power modes, see Section 27.1.4.3.6.4, *SATA DPLL Idle-Bypass Low-Power Mode*, and Section 27.1.4.3.6.5, *SATA DPLL MN-Bypass Mode*.

DPLL_SATA is held in a similar low-power state (DCO and LDO switched off, with CLKDCOLDO = 0) after POR, before the first PLL_GO command has been software-triggered on the PLL controller. See Section 27.1.4.3.6.1, *SATA Clock Generator Power Up*.

27.1.4.3.4 SATA DPLL Clocks Configuration

27.1.4.3.4.1 SATA DPLL Input Clock Control

The DPLL_SATA accepts the functional clock (SATA_REF_GFCLK) on its CLKINP pin (REF_CLK input at SATA SS level) directly from the device SCRM, without involving any PLLCTRL_SATA interractions. The SATA_REF_GFCLK is derived from SCRM.SYS_CLK, and can be optionally software-gated by setting the PRCM.CM_L3INIT_SATA_CLKCTRL[8] OPTFCLKEN_REF_CLK bit. The status of the SATA_REF_GFCLK clock can be monitored in the PRCM.CM_L3INIT_CLKSTCTRL[19] CLKACTIVITY_SATA_REF_GFCLK bit. See Section 3.6.4.5, *Clock Domain Module Attributes* in Chapter 3, *Power, Reset, and Clock Management*.

If CLKINP signal is lost for some time, the LOSSREF output signal, which serves as a feedback to PLLCTRL_SATA, is asserted high. When CLKINP resumes, the LOSSREF signal goes low (LOSSREF inactive state). The LOSSREF status signal can be monitored by software in the PLLCTRL_SATA.PLL_STATUS[3] PLL_LOSSREF bit.

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NOTE: PLLCTRL_SATA has no software or hardware mechanisms to control DPLL_SATA input clock, CLKINP.

27.1.4.3.4.2 SATA DPLL Output Clock Configuration

Only the DPLL_SATA output, CLKDCOLDO, is used to provide the high-speed clock at the PLL_CLK pin of the SATA_PHY. Only the REGM, REGN, and SD divider values are used within the DPLL clock generator subsystem to adjust the CLKDCOLDO output clock frequency. This is done by programming the PLLCTRL_SATA.PLLCTRL_SATA.PLL_CONFIGURATION1[20:9] PLL_REGM, PLLCTRL_SATA.PLL_CONFIGURATION1[8:1] PLL_REGN, and PLLCTRL_SATA.PLL_CONFIGURATION3[17:10] PLL_SD bit fields, respectively. The SATA DPLL CLKOUT and CLKOUTLDO outputs are not used, and internal REGM2 and REGM1 dividers are not software controllable.

NOTE: At the DPLL/PLLCTRL integration level, the PLL_REGM1[3:0] and PLL_REGM2[6:0] divider control signals are tied-off by hardware to 0x0 and 0x1, respectively.

For more details on output clock settings sequence, see Section 27.1.4.3.7.2, *SATA DPLL Clock Programming Sequence*.

27.1.4.3.4.2.1 SATA DPLL Output Clock Gating

There is no direct software gate control for the DPLL_SATA.CLKDCOLDO output.

The DPLL_SATA.CLKDCOLDO clock output is automatically gated (CLKDCOLDO pulled low) in the following scenarios:

- DPLL power-up sequence. For more information on the power-up sequence, see Section 27.1.4.3.6.1, *SATA Clock Generator Power Up*.
- DPLL entering a relock sequence. For more information on the relocking sequence, see Section 27.1.4.3.6.2, *SATA DPLL Sequences*.
- DPLL entering idle-bypass low-power mode. For more information on idle-bypass mode, see Section 27.1.4.3.6.4, *SATA DPLL Idle-Bypass Mode*.
- DPLL entering MN-bypass mode. For more information on MN-bypass mode, see Section 27.1.4.3.6.5, *SATA DPLL MN Bypass Mode*.

27.1.4.3.5 SATA DPLL Subsystem Architecture

Figure 27-5 is a simplified block diagram of the DPLL_SATA instance integration in the SATA clock generator subsystem.

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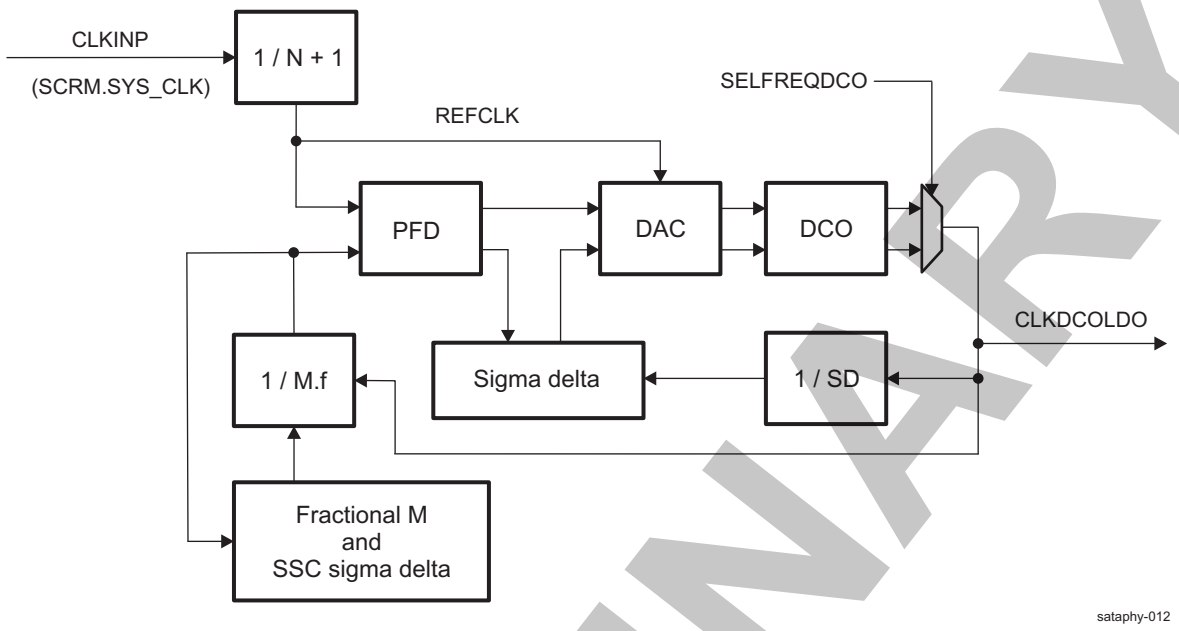
Figure 27-5. DPLL_SATA Functional Block Diagram



The input clock CLKINP goes to a predivider N + 1. The entire loop runs on the REFCLK clock after this predivider. The value of N + 1 is controlled through the PLLCTRL_SATA.PLL_CONFIGURATION1[8:1] PLL_REGN bit field.

The frequency ranges for the DPLL_SATA input clock (CLKINP) and the DPLL internal reference clock (REFCLK = CLKINP / N + 1) are:

- 0.62 to 60 MHz for CLKINP
- 0.62 to 2.5 MHz for the REFCLK

The output clock CLKDCOLDO is synthesized by digitally controlled oscillator (the DCO block), that automatically detects the frequency range. The CLKDCOLDO frequency can be given with CLKDCOLDO = CLKINP × M / (N + 1). For that purpose the feedback multiplier M must be configured through the PLLCTRL_SATA.PLL_CONFIGURATION1[20:9] PLL_REGM bit field.

The DPLL_SATA module supports fractional synthesis (that is, the frequency multiplication factor M can be programmed as fractional). This is achieved by having a sigma delta feedback divider (M). A fractional value (Fractional M) of 18 bits is supported enabling control for a better accuracy. Programming the 18-bit Fractional M value is done by setting the PLLCTRL_SATA.PLL_CONFIGURATION4[17:0] PLL_REGM_F bit field (similar to REGM). To enable integer only division Fractional M should be set to 000…0.

NOTE: Fractional synthesis is not supported for M > 4093.

The module also supports spread spectrum clocking (SSC) on its output clocks. SSC is used to spread the spectral peaking of the clock to reduce any electromagnetic interference (EMI). When SSC is enabled, the clock spectrum is spread by the amount of frequency spread, and the attenuation is given by the ratio of the frequency spread (df) and the modulation frequency (fm); that is, {10 × log10(df/fm)} dB.

The SSC is performed by changing the feedback divider (M) in a triangular pattern, which means the frequency of the output clock varies in a triangular pattern. The frequency of the triangular pattern is modulation frequency (fm). The peak (dM) or the amplitude of the triangular pattern as a percent of M is equal to the percent of the frequency spread (df); that is, dM/M = df/Fout.

Because this is in-band modulation for the DPLL_SATA, the modulation frequency must be within the loop bandwidth of the DPLL. A higher modulation frequency would result in lesser spreading in the output clock.

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The SSC can be enabled and disabled by asserting the PLLCTRL_SATA.PLL_SSC_CONFIGURATION1[0] EN_SSC bit. The acknowledge signal SSCACK, observed by the PLLCTRL_SATA.PLL_STATUS[12] SSC_EN_ACK bit, notifies the exact start and end of SSC. When EN_SSC is deasserted, SSC is disabled only after completion of one full cycle of the triangular pattern given by the modulation frequency. This is done to maintain the average frequency.

The modulation frequency (fm) can be programmed as a ratio of REFCLK/4; that is, the value programmed in the PLLCTRL_SATA.PLL_SSC_CONFIGURATION2[29:20] MODFREQDIVIDER bit field must be = REFCLK/(4*fm).The ModFreqDivider is split into Mantissa and $2^{Exponent}$ (ModFreqDivider = ModFreqDividerMantissa × $2^{ModFreqDividerExponent}$).

- The Mantissa is controlled by bits [29:23] of the PLLCTRL_SATA.PLL_SSC_CONFIGURATION2[29:20] MODFREQDIVIDER bit field.
- The Exponent is controlled by bits [22:20] of the PLLCTRL_SATA.PLL_SSC_CONFIGURATION2[29:20] MODFREQDIVIDER bit field.

Although the same value of ModFreqDivider could be obtained by different combinations of Mantissa and Exponent values, it is preferred to get the target ModFreqDivider by programming maximum Mantissa and minimum Exponent values.

To define the frequency spread (df), dM must be controlled as previously explained. To define dM, the step size of M for each REFCLK during the triangular pattern must be programmed. This is defined as follows:

- dM = ($2^{ModFreqDividerExponent}$) × ModFreqDividerMantissa × DeltaMStep, if ModFreqDividerExponent <= 3
- dM = 8 × ModFreqDividerMantissa × DeltaMStep, if ModFreqDividerExponent > 3

the DeltaMStep value is split into integer part and fractional part, as follows:

- The MSB of 3-bit integer part, DeltaMStepInteger is controlled by the PLLCTRL_SATA.PLL_SSC_CONFIGURATION2 [30] DELTAM2 bit and the remaining LSBs by bits [19:18] of the PLLCTRL_SATA.PLL_SSC_CONFIGURATION2[19:0] DELTAM bit field.
- The 18-bit fractional part, DeltaMStepFraction, is controlled by bits [17:0] of the PLLCTRL_SATA.PLL_SSC_CONFIGURATION2[19:0] DELTAM bit field.

If the PLLCTRL_SATA.PLL_SSC_CONFIGURATION1[2] DOWNSPREAD bit is set to 1, the frequency spread on the lower side is twice the programmed value. The frequency spread on the higher side is 0 (except for 20 percent overshot).

27.1.4.3.6 SATA DPLL Clock Generator Modes and State Transitions

The DPLL_SATA can be set in different modes during operation. PLLCTRL triggers DPLL_SATA state transitions to different static modes by means of TINITZ and TENABLE hardware control signals.

27.1.4.3.6.1 SATA Clock Generator Power Up

After power up, the DPLL_SATA.SYSRESETN input is automatically pulled low by PRM, together with PLLCTRL_SATA.RESET_N input. Because PRM.L3INIT_RST is an asynchronous reset, the DPLL_SATA input clock (DPLL_SATA.CLKINP) is not demanded upon reset. The LOSSREF signal, which monitors the presence of CLKINP clock, remains 1 during SYSRESETN = 0 irrespective of presence/absence on the CLKINP clock. If CLKINP is present upon reset assertion, the LOSSREF signal is deasserted to 0, a certain time after the hardware reset completion. During DPLL power-up mode, CLKDCOLDO clock is maintained inactive (pulled low). After POR, the DPLL_LOCK (internal lock loop) signal is maintained deasserted, too.

27.1.4.3.6.2 SATA DPLL Sequences

Once all the configuration values have been initially programmed into the PLLCTRL_SATA registers (see Section 27.1.4.3.7.2, *SATA DPLL Clock Programming Sequence*), the PLLCTRL_SATA.PLL_GO[0] PLL_GO bit should be set to update the configuration values and start the DPLL calibration and locking sequence.

After PLLCTRL_SATA.PLL_GO[0] PLL_GO bit is set high in software, the PLLCTRL_SATA state-machine takes the following action:

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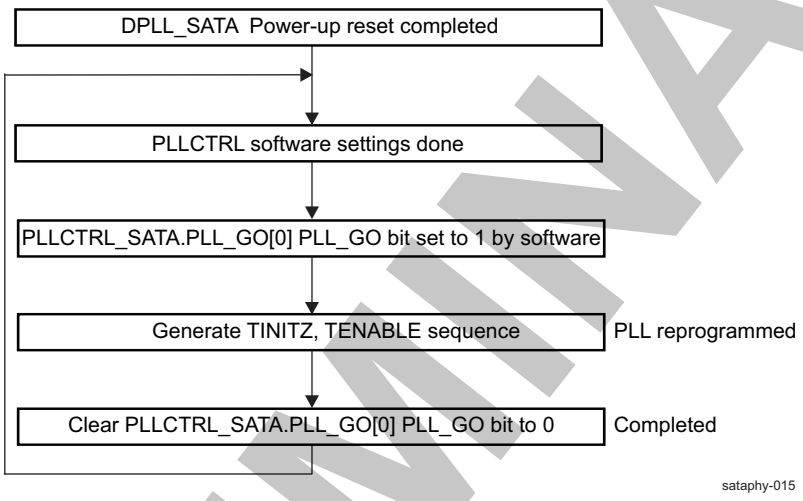
1. Sets TINITZ signal to 0. TINITZ acts as a soft reset to DPLL_SATA. This starts the DPLL initialization procedure. During initialization mode, the CLKDCOLDO, FREQLOCK, and PHASELOCK signals are kept at 0 and the BYPASSACK signal is kept at 1.
   VDDA power supply of DPLL should be active before DPLL_SATA initialization is performed, but it is not required to be switched on immediately after device power up.
2. The TENABLE signal is asserted high by the PLLCTRL hardware to load the user-programmed values of REGM, REGN, REGSD, and SELFREQDCO into DPLL registers.
3. After TENABLE is asserted, TINITZ is driven high (disabled) by the PLLCTRL to trigger a DPLL calibration and lock sequence after the loop control values are loaded. The module calibration-lock sequence will begin from the first CLKINP edge after TINITZ is disabled.

Figure 27-6 summarizes the software and hardware sequences flow of DPLL_SATA.

Figure 27-6. SATA PLL GO Sequence



NOTE: All thick-outlined blocks in Figure 27-6 show operations performed by software. Other blocks show operations performed by hardware.

DPLL_SATA Relock Sequence: When DPLL leaves a lost clock condition (LOSSREF = 1 → 0) or idle-bypass mode it enters relock sequence from the first CLKINP edge (after bypass mode leaving). Relock sequence is the same as calibration-lock sequence already described.

A DPLL relock sequence is also software triggered by setting PLLCTRL_SATA.PLL_GO[0] PLL_GO bit to 0b1 for DPLL parameters update.

When DPLL_SATA enters a relock sequence, CLKDCOLDO is pulled low. FREQLOCK and PHASELOCK status signals are also low. CLKDCOLDO output clock is activated after FREQLOCK or PHASELOCK signal goes high, depending on the selected locking criteria.

The PLLCTRL_SATA.PLL_GO[0] PLL_GO bit can be used by software to monitor if PLLCTRL locking process is still pending (PLL_GO = 0b1).

27.1.4.3.6.3 SATA DPLL Locked Mode

When DPLL_SATA finishes calibration and lock sequences it enters the LOCKED state. During the LOCKED state, LOSSREF is deasserted, BYPASSACK is deasserted, and the FREQLOCK or PHASELOCK signals are asserted.

DPLL lock event criteria (FREQLOCK or PHASELOCK) is software selectable through the PLLCTRL_SATA.PLL_CONFIGURATION2[10:9] PLL_LOCKSEL bit field.

The DPLL indicates it is in the LOCKED state to the PLLCTRL_SATA, SATA controller core controller, and SATA_PHY through assertion of the DPLL_LOCK signal, which reflects the internal lock loop status. The user software can monitor the DPLL locked event in the PLLCTRL_SATA.PLL_STATUS[1] PLL_LOCK bit, which is active high.

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27.1.4.3.6.4 SATA DPLL Idle-Bypass Mode

Idle-bypass fast relock mode is not supported for DPLL_SATA.

DPLL_SATA supports idle-bypass low-power mode. A transition from a normal operation to idle-bypass mode is performed when software sets the PLLCTRL_SATA.PLLCTRL_SATA.PLL_CONFIGURATION2[0] PLL_IDLE bit to 0x1. IDLE signal assertion triggers a power-down sequence on DPLL internal LDO analog blocks and DCO oscillator.

In idle-bypass low-power mode, the PHASELOCK and FREQLOCK output signals are asserted low and CLKDCOLDO goes low, respectively. Also, the internal reference clock REFCLK = CLKINP / N + 1 is gated inside the DPLL digital control logic to save power.

In the functional mode, DPLL_SATA.TICOPWDN output indicates to the PLL controller the status of the power-down signal (active high) of the internal DCO oscillator. The internal DCO oscillator is powered down in idle-bypass mode or during period from SYSRESETN 0 → 1 to module initialization. The DCO oscillator exits power down (TICOPWDN goes low) whenever the module internally tries to lock or relock after initialization or exiting idle-bypass mode.

In the functional mode, DPLL_SATA.LDOPWDN output indicates to the PLL controller the status of the power-down signal (active high) of the internal LDO. LDOPWDN goes high as soon as the internal LDO is powered down. LDOPWDN goes low after the LDO output voltage is stable. The internal LDO is powered down in period from SYSRESETN 0 → 1 to module initialization or when entering into idle-bypass mode. LDOPWDN is cleared whenever the module internally tries to lock or relock after initialization or exiting idle-bypass mode after the internal LDO output voltage has stabilized.

The DCO and LDO power ON/OFF states are reflected within the read-only PLLCTRL_SATA.PLL_STATUS[16] PLL_TICOPWDN and PLLCTRL_SATA.PLL_STATUS[15] LDOPWDN monitor bits.

To exit idle-bypass mode and restore clock generation, the user should set PLLCTRL_SATA.PLL_CONFIGURATION2[0] PLL_IDLE to 0x0, which deasserts the IDLE signal and DPLL_SATA automatically enters a relock sequence. The CLKDCOLDO output clock is activated after the FREQLOCK or PHASELOCK signal goes high, depending on selected locking criteria.

27.1.4.3.6.5 SATA DPLL MN-Bypass Mode

The MN-Bypass mode will be activated if REGM = 0 or 1 is loaded into the module on the rising edge of TENABLE. TINITZ also should be pulsed to enter MN-Bypass mode. The module enters a low-power mode by gating all its internal clocks (REFCLK) and powering down the internal LDO (LDOPWDN = 1) and DCO (DCOPWDN = 1). CLKDCOLDO remains gated (low) during this mode.

NOTE: When the PLLCTRL_SATA.PLL_CONFIGURATION1[20:9] PLL_REGM bit field is updated to 0x0 or 0x1, the CLKDCOLDO output clock is gated.

27.1.4.3.6.6 SATA DPLL Error Conditions

The PLL lock and recalibration signals can be monitored to detect the loss of lock condition and the DPLL requirement to recalibrate (caused by a large temperature change since the last lock request):

- The PLLCTRL_SATA.PLL_STATUS[2] PLL_RECAL bit informs whether the DPLL_SATA must be recalibrated.

The PLL reference clock (CLKINP) loss status and PLL-in-high-jitter condition can also be monitored:

- The PLLCTRL_SATA.PLL_STATUS[1] PLL_LOCK bit gives the SATA PLL LOCKED state.
- The PLLCTRL_SATA.PLL_STATUS[3] PLL_LOSSREF bit informs whether the PLLCTRL_SATA has lost the reference clock.
- The PLLCTRL_SATA.PLL_STATUS[5] PLL_HIGHJITTER bit informs whether the PLL has entered a high-jitter condition.

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27.1.4.3.7 SATA PLL Controller Functions

27.1.4.3.7.1 SATA PLL Controller Register Access

The configuration registers are accessed through the OCP2SCP3 L4 adapter register space using the SCP interface of the PLLCTRL_SATA. This includes all the configuration signals and returning status signals.

CAUTION

All writes must be 32-bit operations, because the SCP interface always transfers 32 bits; 16- or 8-bit operations may lead to unpredictable errors.

NOTE: Because the SATA_PHY directly provides parallel data interface clocks RX_CLK and TX_CLK to the SATA controller, the PLLCTRL_SATA and DPLL_SATA must be configured before any data transfer between the SATA controller and an external SATA storage device.

27.1.4.3.7.2 SATA DPLL Clock Programming Sequence

The DPLL_SATA factors must be calculated based on the required input and output frequencies, keeping the PLL internal reference frequency (REFCLK) in the appropriate range (0.62 to 2.5 MHz).

- The REGM factor is programmed in the PLLCTRL_SATA.PLL_CONFIGURATION1[20:9] PLL_REGM bit field.
- The fractional part of REGM factor is programmed in the PLLCTRL_SATA.PLL_CONFIGURATION4[17:0] PLL_REGM_F bit field.
- The REGN factor is programmed in the PLLCTRL_SATA.PLL_CONFIGURATION1[8:1] PLL_REGN bit field.
- The DCO frequency range is set in the PLLCTRL_SATA.PLL_CONFIGURATION2[3:1] PLL_SELFREQDCO bit field.
  - PLL_SELFREQDCO should be set to 0x2, if 500 MHz < CLKDCOLDO [MHz] < 1000 MHz
  - PLL_SELFREQDCO should be set to 0x4, if 1000 MHz < CLKDCOLDO [MHz] < 2000 MHz
- The SD divider is programmed in the PLLCTRL_SATA.PLL_CONFIGURATION3[17:10] PLL_SD bit field. The PLLCTRL_SATA.PLL_CONFIGURATION2[3:1] PLL_SELFREQDCO bit field should be programmed depending on the value of CLKDCOLDO = CLKINP × M / (N + 1). The formulas are shown in Figure 27-7.

Figure 27-7 shows the programming sequence.

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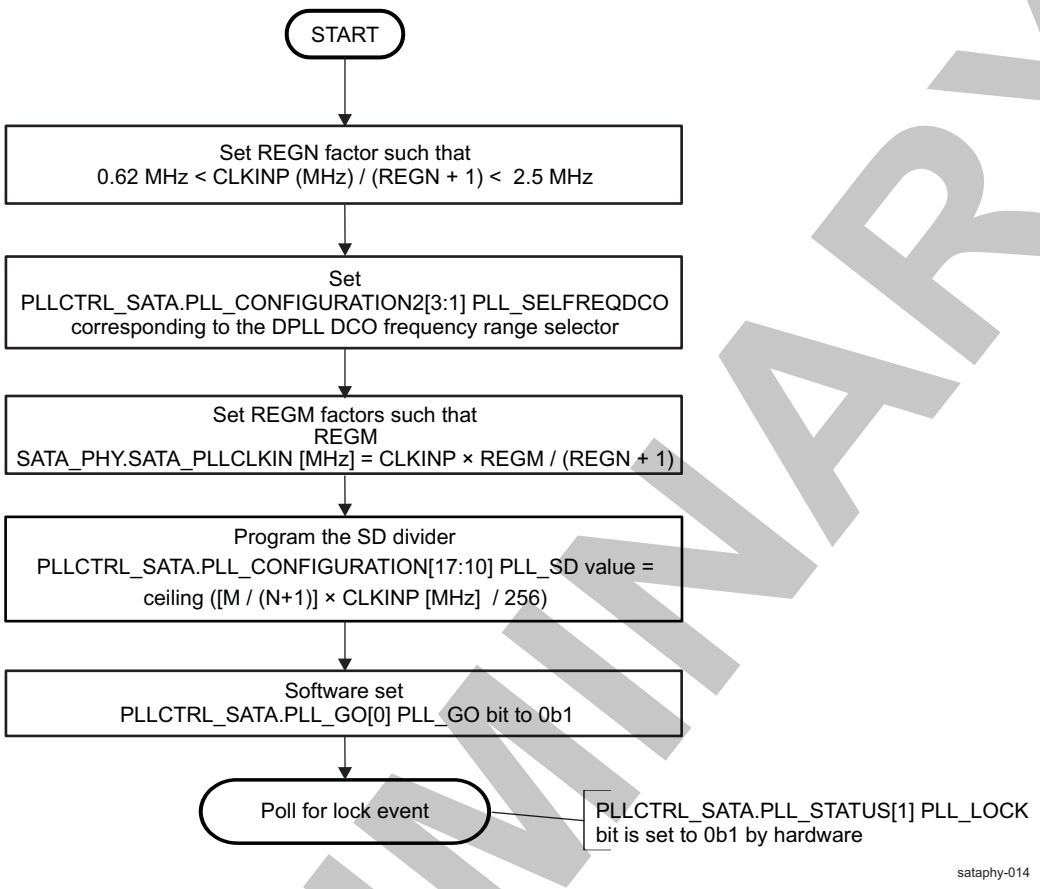
Figure 27-7. SATA PLL Programming Sequence



NOTE:

- The equation for SATA_PHY_TX/SATA_PHY_RX (MHz) applies to the CLKDCOLDO of the DPLL_SATA.
- For normal operation CLKDCOLDO output frequency of the DPLL_SATA should be either 750 MHz (SATA-1 mode) or 1500 MHz (SATA-2 mode).

Table 27-5 summarizes the registers for the PLLCTRL_SATA programming sequence.

Table 27-5. Register Call Summary for SATA PLL Programming Sequence

Register Name	Register Name	Register Name	Register Name
PLLCTRL_SATA.PLL_CONFIGURATION2	PLLCTRL_SATA.PLL_GO	PLLCTRL_SATA.PLL_STATUS	PLLCTRL_SATA.PLL_CONFIGURATION3

27.1.4.3.7.3 SATA DPLL Recommended Values

Table 27-6 lists the DPLL_SATA recommended values.

Table 27-6. Recommended Programming Values

Field Name	Value	Description
PLLCTRL_SATA.PLL_CONFIGURATION1[20:9] PLL_REGM	See (1).	Feedback clock divider

(1) The value of the bit field must be set according to the desired clock frequencies – 750 MHz for SATA-1 and 1.5 GHz for SATA-2 speeds.

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Table 27-6. Recommended Programming Values (continued)

Field Name	Value	Description
PLLCTRL_SATA.PLL_CONFIGURATION1[8:1] PLL_REGN	See (1).	Reference clock divider
PLLCTRL_SATA.PLL_CONFIGURATION2[10:9] PLL_LOCKSEL	0x-	Criteria to lock the PLL
PLLCTRL_SATA.PLL_CONFIGURATION2[3:1] PLL_SELFREQDCO	See (1).	Program based on the PLL choice and lock frequency.
PLLCTRL_SATA.PLL_CONFIGURATION2[0] PLL_IDLE	0	PLL active
PLLCTRL_SATA.PLL_CONFIGURATION3[17:10] PLL_SD	See (1).	Ceiling { [PLL_REGM / (PLL_REGN + 1)] × CLKINP(MHz) / 256 }
PLLCTRL_SATA.PLL_GO[0] PLL_GO	0x1	Write 1 when PLL is to be (re)locked with new parameters. This bit is cleared by hardware when the PLL request completes.

27.1.5 SATA PHY Subsystem Low-Level Programming Model

Table 27-7 summarizes the low-level programming sequence to set up the SATA PHY subsystem for SATA I/O operations.

Table 27-7. SATA PHY Subsystem Low-Level Programming Sequence

Step	Description	Comment
1.	Set the startup low-performance OPP in the appropriate PRCM registers.	For more information regarding demanded OPP, see the device *Data Manual*.
2.	Enable the PRCM.SATA_REF_GFCLK.	See Section 3.6.4.5, *Clock Domain Module Attributes*, in Chapter 3, *Power, Reset, and Clock Management*.
3.	Enable the PRCM.L3INIT_L4_GICLK clock to enable the OCP2SCP3 interface adapter operation.	See Section 3.6.4.5, *Clock Domain Module Attributes*, in Chapter 3, *Power, Reset, and Clock Management*.
4.	Software reset the OCP2SCP3 and poll until soft reset completion is indicated in status.	See Section 27.1.4.1.
5.	Set up division ratio between the OCP clock (PRCM.L3INIT_L4_GICLK) and SCP clock to supply the serial configuration register domains of the PLLCTRL_SATA.	See Section 27.1.4.1.
6.	Set up necessary SYNC1 and SYNC2 timings to ensure no blocking of transactions over the SCP bus.	. See Section 27.1.4.1.After this step user is ready to access PLLCTRL_SATA .
7.	Configure DPLL_SATA to generate frequency (CLKDCOLDO) = 1.5 GHz.	See Section 27.1.4.3.7.2 and Table 27-8.
8.	Soft assert bit PLLCTRL_SATA.PLL_GO[0] PLL_GO to 0x1.	Start the DPLL lock with desired parameters.
9.	Poll PLLCTRL_SATA.PLL_STATUS[1] PLL_LOCK bit until it is seen 1.	DPLL locked event
10.	Perform a SATA_PHY tuning required for SATA i/f operation	Follow steps described in Table 27-9, *SATA PHY Tuning Table*.
11.	Software trigger the SATA_PHY_TX power-up sequence.	For more details, see Section 27.1.4.2.3.1, *SATA_PHY Power-Up/-Down Sequences*.
12.	Software trigger the SATA_PHY_RX power-up sequence.	For more details, see Section 27.1.4.2.3.1, *SATA_PHY Power-Up/-Down Sequences*.

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Table 27-8. DPLL CLKDCOLDO Recommended Settings

Parameter	Setting				
F(CLKDCOLDO) MHz	1500				
SYS_CLK (MHz)	12	16.8	19.2	26	38.4
N	4	6	7	12	15
SELFREQDCO[2:0]	100	100	100	100	100
M	625	625	625	750	625
Frac	0	0	0	0	0
SD	6	7	6	6	6

Table 27-9. SATA PHY Tuning Table

Physical address[1] [bits to modify]	Preferred value setting[2]
0x4A09 600C [31:27]	**0b01000** for SATA 1.5 Gbps mode **0b00100** for SATA 3 Gbps mode
0x4A09 600C [17:14]	**0b1010** for SATA-Gen1x and SATA-Gen2x **0b0101** for SATA-Gen1m and SATA-Gen2m
0x4A09 6028 [23:19]	**0b11100** if spread-spectrum is ON. **0b00001** if spread-spectrum is OFF.
0x4A09 6028 [18:11]	**0b01100110**(regardless of spread-spectrum being ON or OFF)
0x4A09 6028 [28:26]	**0b011** for 1.5 Gbps with 1.5GHz PLL clock (PLL_CLK) **0b001** for 3 Gbps with 1.5GHz PLL clock (PLL_CLK)
0x4A09 600C [6:5]	**0b00**, for **3Gbps** @ PLL_CLK = 1.5GHz by DPLL_SATA output with 0x4A09 6028 [28:26] being set to **'0b001'**. **0b00** applies also for **1.5Gbps** @PLL_CLK=1.5GHz by DPLL_SATA output with 0x4A09 6028 [28:26] being set to **'0b011'**.
0x4A09 601C [31:30]	**0b01**
0x4A09 6024 [31:30]	**0b10**, assuming PLL_CLK=1.5GHz in both SATA 1.5Gbps and SATA 3Gbps speed modes
0x4A09 6038 [31:16]	**0x0000**
0x4A09 6038 [15:7]	**0b111110000**
0x4A09 6038 [2:1]	**0b11**
0x4A09 6044 [10:9]	**0b00**

(1) Accesses to these locations have to be done in 32-bits only. User must NOT modify SATA PHY bits different than those described in Table 27-9.

(2) These are the preferred settings of SATA_PHY, in case that SATA PHY PLL_CLK=1.5 GHz.

27.2 USB3 PHY Subsystem

This chapter describes the features and functions of the USB3 PHY subsystem of the device.

27.2.1 USB3 PHY Subsystem Overview

The USB3.0 physical layer (PHY) is responsible for transmitting the USB_OTG_SS controller media access layer (MAC) 32-bit parallel data output as a serial data stream over a differential pair (TXP/TXN) and converting the differentially received serial data (RXP/RXN) to 32-bit parallel input data demanded by the MAC receiver logic.

The USB3 PHY component operates with a 2.5 GHz-source clock, to achieve the USB 3.0 super-speed throughput of 5 Gbps. The USB3 PHY serializer/deserializer source clock is generated by a DPLL clock generator (DPLL_USB_OTG_SS) which isintegrated into the USB_OTG_SS host subsystem.

The DPLL_USB_OTG_SS is configured and controlled through the USB3 PHY dedicated PLL controller (PLLCTRL_USB_OTG_SS) with associated serial configuration port (SCP) accessible registers.

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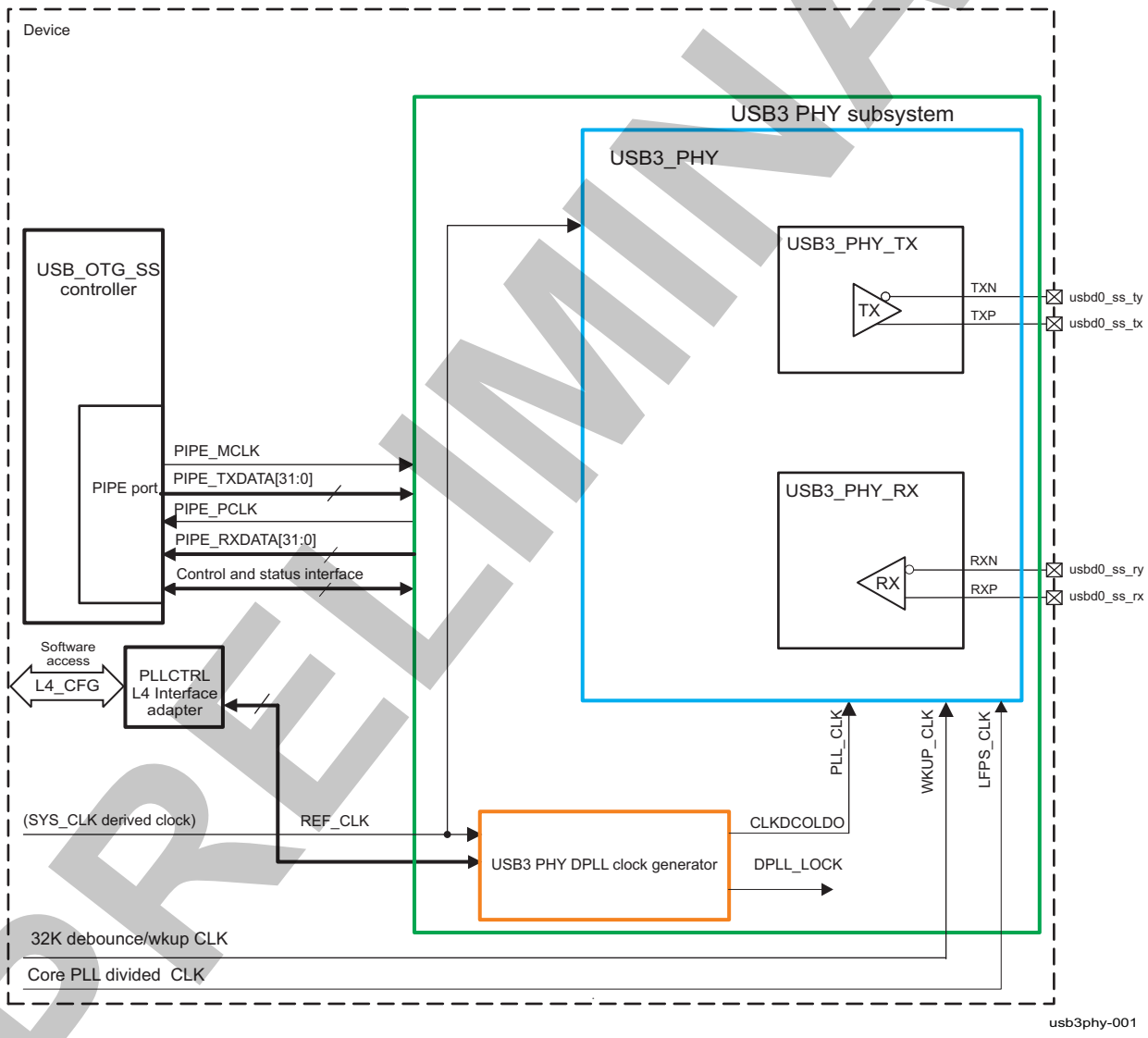
A common interconnect adapter component, OCP2SCP1, lets the user program the PLLCTRL_USB_OTG_SS component through the L4_CFG interconnect.

NOTE: The system of components (USB3_PHY_RX, USB3_PHY_TX, DPLL_USB_OTG_SS, PLLCTRL_USB_OTG_SS, and OCP2SCP1) is signified as the USB3 PHY subsystem throughout this chapter. This subsystem is responsible for PHY components clock generation and physical layer transmission/reception within the device USB3 PHY subsystem.

Figure 27-8 gives an overview of the USB3 PHY subsystem. Figure 27-8 shows that the USB3 PHY serializer and deserializer directly interract with the attached to USB OTG SS controller USB3.0 compatible device (over TXP/TXN transmission and RXP/RXN reception interface I/Os). The PIPE port interracts with the USB_OTG_SS MAC port, described in details in Section 23.11, *Super-Speed USB OTG Subsystem*.

Figure 27-8. USB3 PHY Subsystem Overview



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27.2.2 USB3 PHY Subsystem Environment

27.2.2.1 USB3 PHY I/O Signals

Table 27-10 represents module pins and their corresponding signal names at the device level, and also specifies their links to functions.

Table 27-10. USB3 PHY I/O Signals

Module Pin Name	Device-Level Signal Name	I/O[1]	Description	Module Pin Reset Value[2]
TXP[3]	usbd0_ss_tx	O	TX output of the USB3 PHY differential transmission line	0
TXN[3]	usbd0_ss_ty	O	TY output of the USB3 PHY differential transmission line	0
RXP[3]	usbd0_ss_rx	I	RX input of the USB3 PHY differential reception line	HiZ
RXN[3]	usbd0_ss_ry	I	RY input of the USB3 PHY differential reception line	HiZ

(1) I = Input; O = Output
(2) HiZ = High impedance
(3) The USB3 PHY signals that implement the physical interface with an external USB3 storage device

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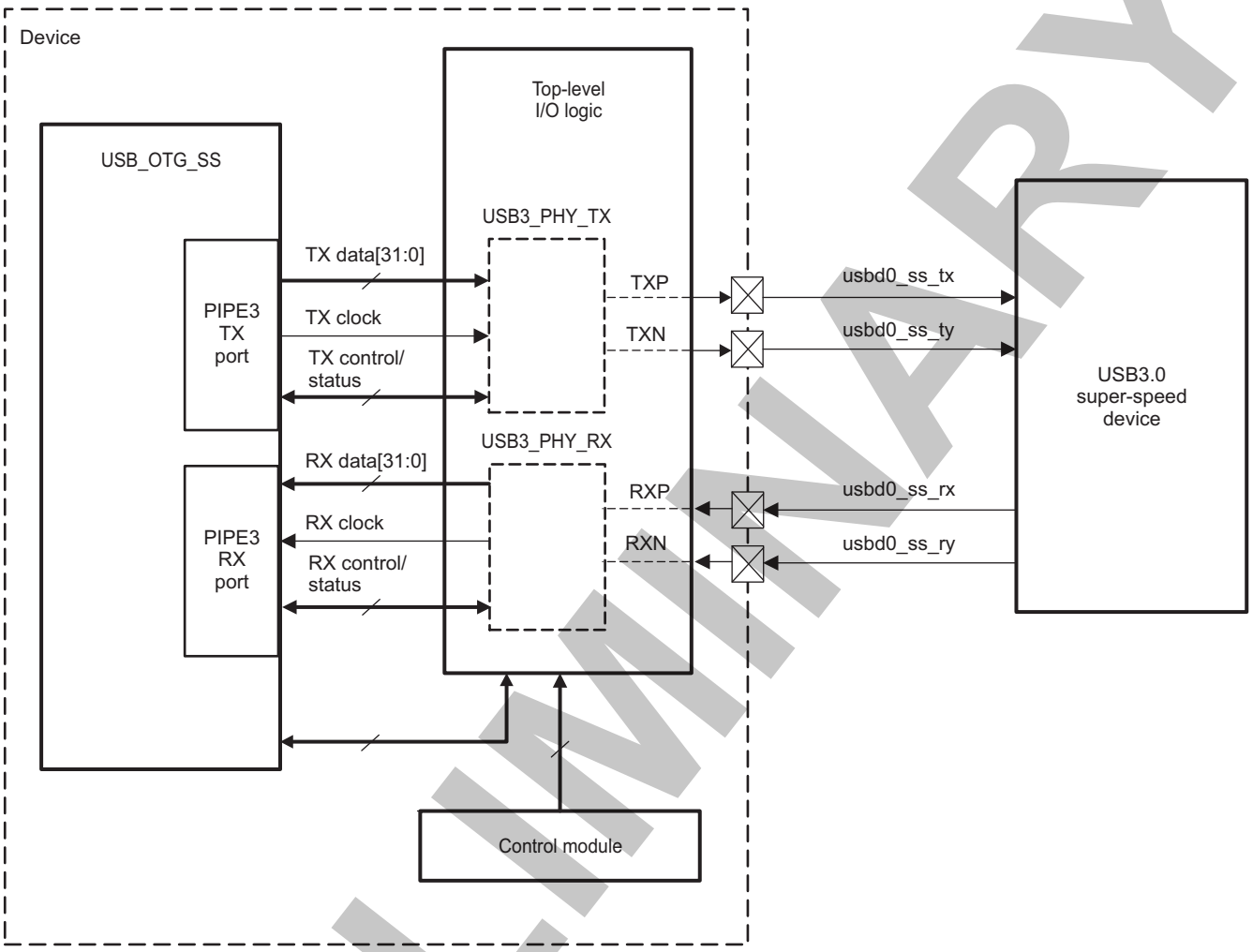
Figure 27-9 shows module pin signals mapping to USB3 PHY signals visible at the device pad level.

Figure 27-9. USB3 PHY I/O Signals



NOTE: The path from module pin to device pad(s) is defined at the device I/O logic level. The I/O logic maps the module signals to the different pads of the device and can be programmed in the control module registers. For more information, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, and *Section 18.4.12.7.5, Device Interfaces Signal Group Controls Mapping*, in Chapter 18, *Control Module*.

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27.2.3 USB3 PHY Subsystem Integration

This section describes the USB3 PHY subsystem-related components (USB3_PHY module, DPLL_USB_OTG_SS, PLLCTRL_USB_OTG_SS, and OCP2SPC1) integration in the device, including information about clocks, resets, and hardware requests.

Figure 27-10 shows the USB3 PHY integration.

The USB3 PHY module integration features:

- A low-power nonretention reset, L3INIT_RST
- A high-frequency input clock (PLL_CLK) tied to the DPLL_USB_OTG_SS.CLKDCOLDO output
- A local port connected to the USB_OTG_SS MAC PIPE3 port
- A clock output (PIPE_PCLK) to the USB_OTG_SS PIPE port
- A clock output (PIPE_MCLK) from the USB_OTG_SS PIPE port
- A common clock from PRCM - REF_CLK, to supply DPLL and PHY RX / TX logic
- PRCM.CORE_USB_OTG_SS_LFPS_TX_CLK clock tied to the USB3_PHY_TX
- A device CORE CONTROL MODULE command port to the power sequencer

The DPLL_USB_OTG_SS integration features:

- A low-power nonretention reset, L3INIT_RST
- A PRCM gated version of the device SYS_CLK (USB_OTG_SS_REF_CLK) supplying DPLL_USB_OTG_SS.CLKINP pin
- A single high-frequency clock output, DPLL_USB_OTG_SS.CLKDCOLDO, to the PLL_CLK input of the USB3 PHY TX/RX components.
- No HS divider integration
- IDLE signaling implementation
- LDO and DCO PWRDNZ monitoring signals
- A DPLL_LOCK LOCKED status indication

The PLLCTRL_USB_OTG_SS integration features:

- A low-power nonretention reset, L3INIT_RST
- (OCP2SPC1) Interconnect adapter target interface also providing the input SCP clock to the PLLCTRL_USB_OTG_SS
- Configuration/control programming interface to the DPLL_USB_OTG_SS
- No direct gate control for DPLL_USB_OTG_SS.CLKINP and CLKDCOLDO

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Figure 27-10. USB3 PHY Subsystem Integration

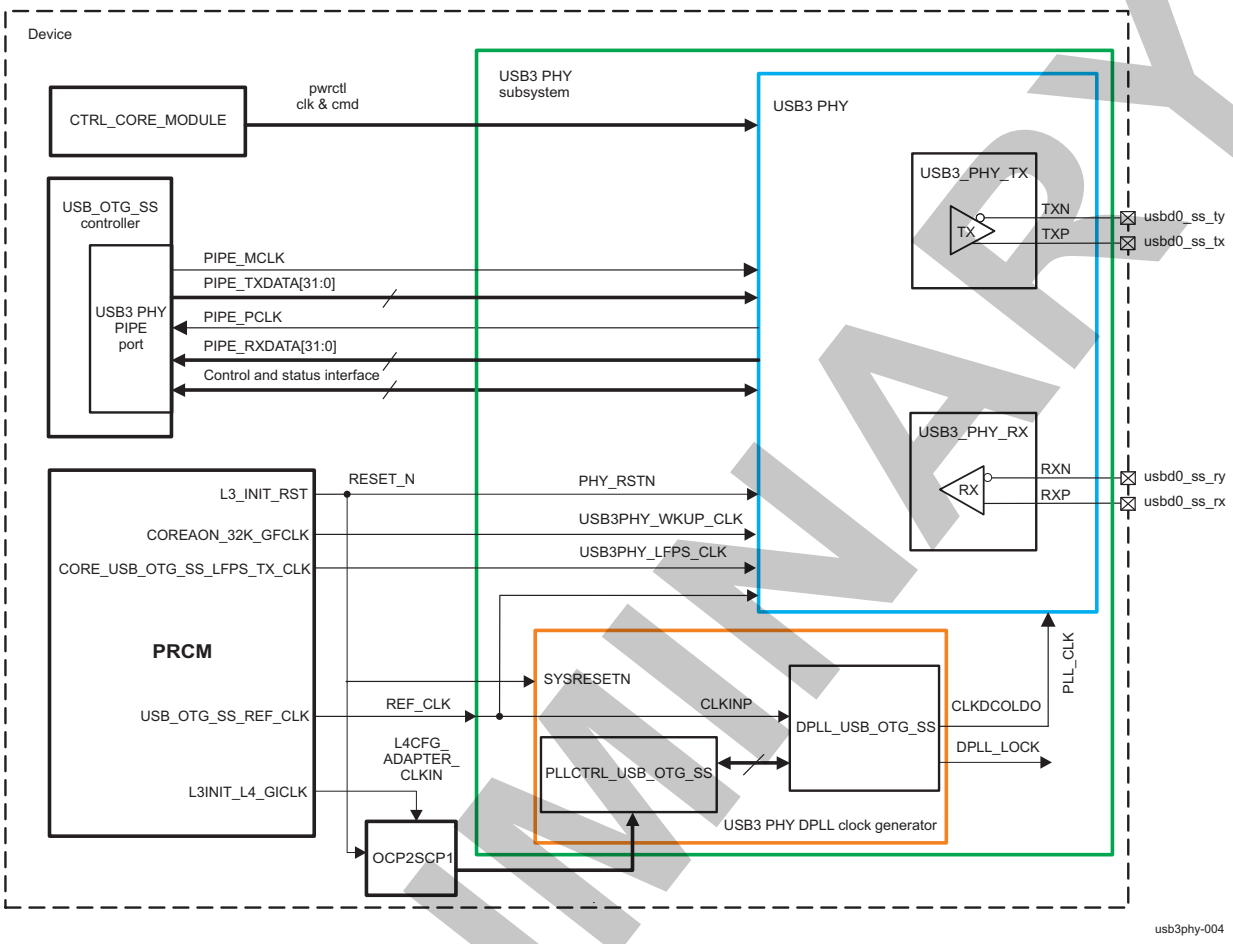

Table 27-11 through Table 27-13 summarize the integration of the module in the device.

Table 27-11. Integration Attributes

Module Instance	Attributes	
	Power Domain	Interconnect
PLLCTRL_USB_OTG_SS DPLL_USB_OTG_SS	PD_L3INIT	OCP2SCP1 adapter SCP interconnect
OCP2SCP1		L4_CFG

Table 27-12. Clocks

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
DPLL_USB_OTG_SS / USB3_PHY	REF_CLK	USB_OTG_SS_REF_CLK	PRCM	USB3 subsystem DPLL and PHY reference functional clock (SYS_CLK)
OCP2SCP1	L4CFG_ADAPTER_CLKIN	L3INIT_L4_GICLK	PRCM	L4_CFG adapter interface clock

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Table 27-13. Resets

Resets				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
USB3_PHY subsystem	RESET_N	L3INIT_RST	PRCM	A nonretention reset to all USB3_PHY subsystem components

NOTE: The USB3_PHY_RX generates a hardware wakeup request to the PRCM module.

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27.2.4 USB3 PHY Subsystem Functional Description

27.2.4.1 USB3 PHY Subsystem Block Diagram

27.2.4.2 Super-Speed USB PLL Controller L4 Interface Adapter Functional Description

The L4_CFG interconnect adapter (OCP2SCP1), allows user software to configure the PLLCTRL_USB_OTG_SS registers over the L4_CFG port. Hence it is expected that this adapter is configured to operate before any programming of the PLLCTRL_USB_OTG_SS.

Before initiating any software reset to this adapter, a value >= 0x6 should be written to the register bitfield OCP2SCP_TIMING[3:0] SYNC2.

L4_CFG interconnect adapter software reset is performed via writing OCP2SCP_SYSCONFIG[1] SOFTRESET to 0b1. The software reset completion is observed in bit OCP2SCP_SYSSTATUS[0] RESETDONE.

By default a smart-idle power mode is selected for OCP2SCP1. The smart-idle mode supported by OCP2SCP1 is not wake-up capable, which means software must explicitly take care to wake the OCP2SCP1 by setting the OCP2SCP_SYSCONFIG [4:3] IDLEMODE bit field to 0x1 (no idle), once it has previously gone to an idle mode.

By default OCP2SCP_SYSCONFIG[0] AUTOIDLE =0x1, which defines that the PLLCTRL L4 interface adapter automaticaly gates its L4 input clock based on L4_CFG interconnect activity. To enable a free-running clock, one should set bit AUTOIDLE to 0x0.

27.2.4.3 USB3 PHY Serializer and Deserializer Functional Descriptions

27.2.4.3.1 USB3 PHY Module Resets

27.2.4.3.1.1 Hardware Reset

The USB3 PHY active low reset which is sourced from PRCM module. L3INIT_RST is hardware-asserted upon power up. For more information on the hardware reset source , see Section 3.5.4, *Reset Domains*, in Chapter 3, *Power, Reset, and Clock Management*.

27.2.4.3.1.2 Software Reset

The USB3 PHY PIPE i/f logic is software reset from USB_OTG_SS over PIPE port by software assertion of the USBOTGSS_GUSB3PIPECTL[31] PHYSOFTRST bit to 0x1. The user must set USBOTGSS_GUSB3PIPECTL[31] PHYSOFTRST to 0x1 before triggering the serializer and deserializer power-up sequence in the CTRL_MODULE_CORE.CONTROL_PHY_POWER_USB register. For more information on power-up sequence, see Section 27.2.4.3.3.1, *USB3 PHY Power-Up/Down Sequences*.

The user should deassert USBOTGSS_GUSB3PIPECTL[31] PHYSOFTRST to 0x0, after the serializer and deserializer power-up sequence completes. For more information, see Section 27.2.4.3.3.1, *USB3 PHY Power-Up/Down Sequences*.

27.2.4.3.2 USB3 PHY Subsystem Clocking

27.2.4.3.2.1 USB3 PHY Subsystem Input Clocks

The USB3 PHY component receives a feedback clock, PIPE_MCLK, which is the reflected version of the PIPE_PCLK (PIPE port synchronizing clock) generated by the USB3 PHY component. The clock is turned on/off according to the PIPE power-down port states. As PIPE port works in source-synchronous mode, all data movement from the MAC layer to the PIPE interface is synchronous to PIPE_PCLK.

The USB3_PHY.PLL_CLK high-speed transmission (2.5 GHz) clock input pin is connected to the DPLL_USB_OTG_SS clock output, CLKDCOLDO. For more information on the DPLL_USB_OTG_SS.CLKDCOLDO output clock settings, see Section 27.2.4.4.4.2, *USB3 PHY DPLL Output Clock Configuration*.

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As shown in Figure 27-11, the same PRCM-sourced clock (USB_OTG_SS_REF_CLK), tied at the USB3 PHY subsystem REF_CLK input, supplies the USB3 PHY RX/TX components and the DPLL_USB_OTG_SS.CLKINP inputs.

The PHY associated power sequencer receives PRCM.USB_OTG_SS_REF_CLK as a functional clock. Software must notify the PHY logic about which REF_CLK frequency is selected by writing the CTRL_MODULE_CORE.CONTROL_PHY_POWER_USB[31:22] USB_PWRCTL_CLK_FREQ bit field, as follows:

- 0x26: If SYSCLK = 38.4 MHz
- 0x1A: If SYSCLK = 26.0 MHz
- 0x13: If SYSCLK = 19.2 MHz
- 0x10: If SYSCLK = 16.8 MHz
- 0x0C: If SYSCLK = 12.0 MHz

The USB3PHY_LFPS_CLK clock input is used to support different USB3_PHY functions, such as the low-frequency periodic signaling (LFPS) generator. This USB3_PHY_TX clock input is tied to the PRCM.CORE_USB_OTG_SS_LFPS_TX_CLK functional clock.

The USB3_PHY_RX deserializer I/O wake-up logic is supported by the PRCM.COREAON_32K_GFCLK clock (SCRM.SYS_32K based), applied at the USB3PHY_WKUP_CLK input.

27.2.4.3.2.2 USB3 PHY Subsystem Output Clocks

- PIPE_PCLK: The PIPE interface is source-synchronous. A PIPE_PCLK clock is generated by the USB3_PHY component, used to synchronize USB_OTG_SS PIPE port inputs, and reflected back as the PIPE_MCLK along with the PIPE outputs. The clock is turned on/off according to the power control port. All data movement from the PIPE interface to the USB_OTG_SS MAC layer is synchronous to this clock.

The PIPE_PCLK clock which drives the PIPE3 logic is sourced by the on-chip USB3_PHY. The PIPE interface is source-synchronous (that is, the clock is received from the PHY), used to synchronize USB_OTG_SS PIPE inputs, and reflected back along with the PIPE outputs as the PIPE_MCLK. The PIPE_PCLK clock is turned on/off according to the USB3_PHY power control port. For more details, see Section 27.2.4.3.3, *USB3 PHY Power Management*.

27.2.4.3.3 USB3 PHY Power Management

From one side the control over power up/down states of the USB3_PHY is provided through a power sequencer module tightly integrated with the the USB3_PHY physical layer TX/RX components.

27.2.4.3.3.1 USB3 PHY Power-Up/-Down Sequences

Powering-up/-down the USB3_PHY_TX and USB3_PHY_RX modules is triggered through software writing corresponding power-up/down commands in the CTRL_MODULE_CORE. CONTROL_PHY_POWER_USB register of the device core control module, as follows:

- CONTROL_PHY_POWER_USB[21:14] USB_PWRCTL_CLK_CMD=0x0 (default value) commands both USB3_PHY_TX and USB3_PHY_RX to power-down (OFF) state.
- CONTROL_PHY_POWER_USB[21:14] USB_PWRCTL_CLK_CMD=0x1 powers up the USB3_PHY_RX only.
- CONTROL_PHY_POWER_USB[21:14] USB_PWRCTL_CLK_CMD=0x2 powers up the USB3_PHY_TX only.
- CONTROL_PHY_POWER_USB[21:14] USB_PWRCTL_CLK_CMD=0x3 simultaneously powers up the USB3_PHY_RX and the USB3_PHY_TX

For more information, see Chapter 18, *Control Module*.

27.2.4.3.3.2 USB3 PHY Low-Power Modes

An implemented powerdown control port allows USB3_PHY to support four low-power states:

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- 0b00: P0, normal operation (used for all Polling, Configuration, Recovery, Loopback, and Hot_Reset states, and U0 state),
- 0b01: P1, low recovery time latency, power saving state (used for U1 state)
- 0b10: P2, longer recovery time latency, lower power state (used for U2, Rx.Detect and SS.Inactive states)
- 0b11: P2, lowest power state (used for SS.disabled and U3)

The USB3_PHY transitions from P0-active mode to low-power P1, or either of the two P2 states, is synchronized with USB_OTG_SS transitions from U0 active state to U1, U2, and U3 low-power states through the input PIPE_POWERDOWN[1:0]. The PIPE port low-power behavior is configured from various bit fields inside the USB_OTG_SS.USBOTGSS_GUSB3PIPECTL register. For more information on PIPE port low-power (LP) configuration, see Section 23.11.5.2.2, *DWC_USB3 Register Description* in Section 23.11, *Super-Speed USB OTG Subsystem*.

27.2.4.3.3.3 Clock Gating

The USB3_PHY component high-speed clocks, PLL_CLK and PIPE_PCLK, are gated during the P1 low-power state.

27.2.4.3.4 USB3 PHY Hardware Requests

An asynchronous wake-up request is generated to the PRCM module by the USB3_PHY_RX I/Os (RXP, RXN). When the wake-up request is acknowledged, the DPLL_USB_OTG_SS and PIPE_PCLK are restarted.

Neither interrupt nor DMA requests are generated.

27.2.4.4 USB3 PHY Clock Generator Subsystem Functional Description

The DPLL_USB_OTG_SS, which is located outside the PRCM boundaries and is part of the USB_OTG_SS controller subsystem, directly injects a high-speed clock into the USB3_PHY serializer/deserializer input, PLL_CLK. The DPLL generator is controlled through a programmable interface from a dedicated PLL controller, PLLCTRL_USB_OTG_SS.

27.2.4.4.1 USB3 PHY DPLL Clock Generator Overview

The SCP interface of the USB3 PHY PLL controller (PLLCTRL_USB_OTG_SS instance) is used to set the configuration of the DPLL modules, primarily the various counter values. Figure 27-11 is an overview of the DPLL clock generator embedded into the USB_OTG_SS controller subsystem.

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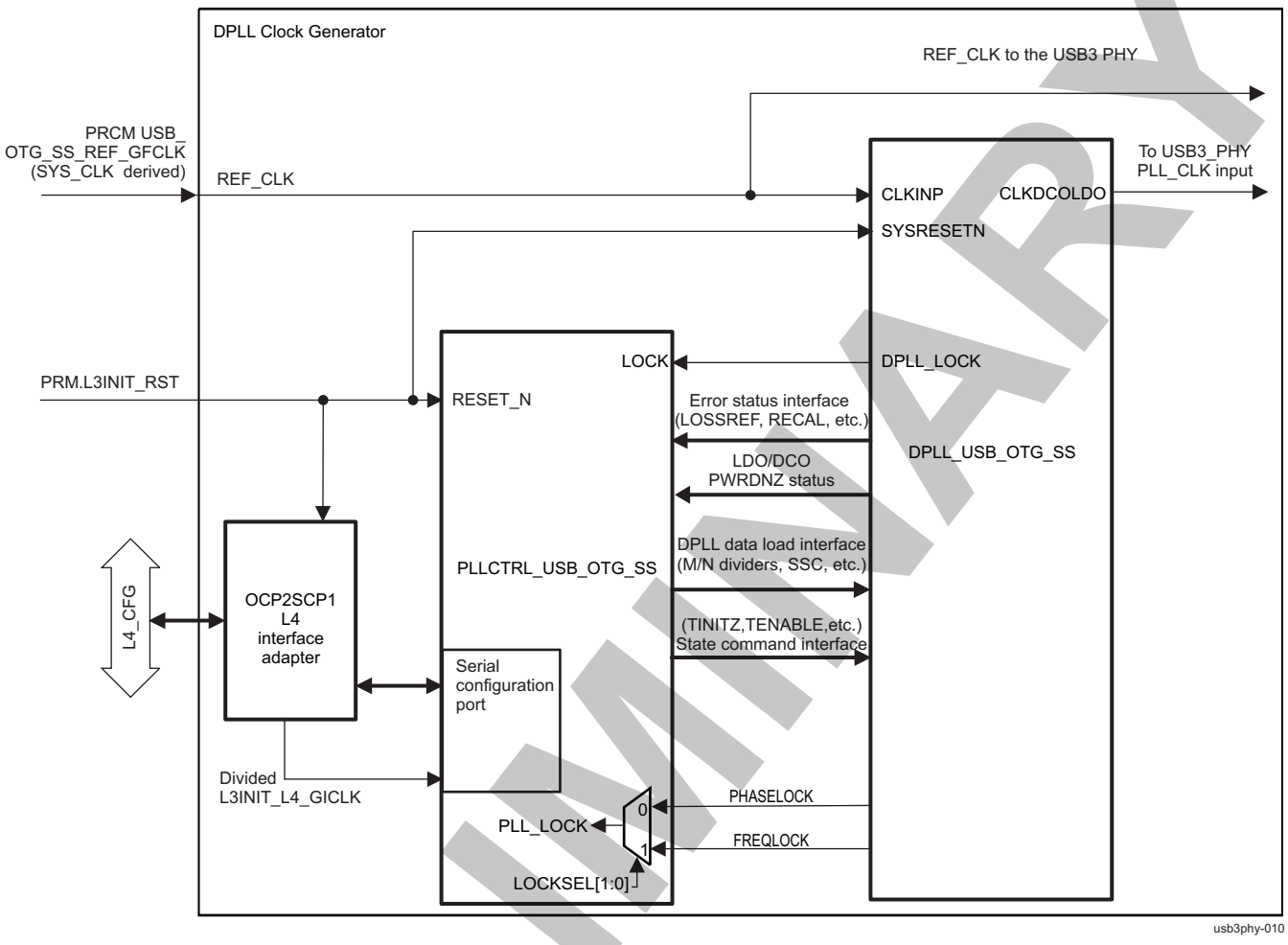
Figure 27-11. USB3 PHY DPLL Clock Generator Overview



NOTE: The PLLCTRL_USB_OTG_SS module is user accessible on the L4_CFG interconnect. However, to make access possible, the user should take care to configure the OCP2SCP1 instance before accessing the PLLCTRL_USB_OTG_SS registers.

The DPLL_USB_OTG_SS features:

- A programmable 8-bit input divider: N
- A programmable 12-bit integer, 18-bit fractional loop multiplier: M
- Digital control and loop filter
- Internal oscillator output clock on internal LDO domain (CLKDCOLDO output)
- DPLL output clock SSC (spread spectrum clocking) support
- No retention capabilities
- No Idle-bypass fast relock capabilities
- Idle-bypass low-power mode
- M/N bypass mode
- Relock from standby

The PLLCTRL_USB_OTG_SS components features:

- DPLL error and status notification
- DPLL initialization and configuration

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- DPLL lock criteria selectable between frequency and phase lock
- Idle command implementation
- No software reset implementation
- Automatic enable/disable control, synchronized with USB_OTG_SS controller PIPE port commands to set USB3_PHY to P1, P2, and P3 low-power states

27.2.4.4.2 USB3 PHY DPLL Clock Generator Reset

The USB3 PHY PLL controller and USB3 PHY DPLL clock generator share a common hardware nonretention reset, L3INIT_RST, which comes from the device power and reset manager. Upon DPLL_USB_OTG_SS hardware reset completion, the PLLCTRL_USB_OTG_SS.PLL_STATUS[0] PLLCTRL_RESET_DONE bit is automatically updated to 1. For more information on the hardware reset source, see Section 3.5.4, *Reset Domains* in Chapter 3, *Power, Reset, and Clock Management*.

The PLLCTRL_USB_OTG_SS itself has no software reset capabilities.

PLLCTRL_USB_OTG_SS performs a software reset sequence on the DPLL_USB_OTG_SS in hardware (through the TINITZ signal activation).

27.2.4.4.3 USB3 PHY DPLL Low-Power Modes

The power-management port (PMP) is not integrated for PLLCTRL_USB_OTG_SS. The DPLL_USB_OTG_SS has no retention capabilities. This means, the DPLL digital power supply remains switched on during all modes of operation.

The low-power modes supported by DPLL_USB_OTG_SS are Idle-bypass low-power and MN-bypass modes, which are both characterized by:

- Internal LDO switched off
- DCO oscillator switched off
- CLKDCOLDO output pulled low

For more details on the PLL settings and conditions necessary to enter Idle-bypass and MN-bypass low-power modes, see Section 27.2.4.4.6.4, *USB3 PHY DPLL Idle-bypass low-power Mode* , and Section 27.2.4.4.6.5, *USB3 PHY DPLL MN-Bypass Mode*.

DPLL_USB_OTG_SS is held in a similar low-power state (DCO and LDO switched off, with CLKDCOLDO = 0) after Power-up Reset, before first PLL_GO command has been software triggered on the PLL controller. See Section 27.2.4.4.6.1, *USB3 PHY Clock Generator Power Up*.

27.2.4.4.4 USB3 PHY DPLL Clocks Configuration

27.2.4.4.4.1 USB3 PHY DPLL Input Clock Control

The DPLL_USB_OTG_SS accepts the functional clock, USB_OTG_SS_REF_CLK, on its CLKINP pin (REF_CLK input at USB3 PHY subsystem level) directly from the device SCRM, without involving any PLLCTRL_USB_OTG_SS interractions. The USB_OTG_SS_REF_CLK is derived from SCRM.SYS_CLK. See Section 3.6.4.5, *Clock Domain Module Attributes* in Chapter 3, *Power, Reset, and Clock Management*.

If the CLKINP signal is lost for some time, the LOSSREF output signal, which serves as a feedback to PLLCTRL_USB_OTG_SS, is asserted high. When CLKINP resumes, LOSSREF goes low (LOSSREF inactive state). The LOSSREF status signal can be software-monitored in the PLLCTRL_USB_OTG_SS.PLL_STATUS[3] PLL_LOSSREF bit.

NOTE: PLLCTRL_USB_OTG_SS has no software or hardware mechanisms to control DPLL_USB_OTG_SS input clock (CLKINP).

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27.2.4.4.4.2 USB3 PHY DPLL Output Clock Configuration

Only the DPLL_USB_OTG_SS output, CLKDCOLDO, is used to provide the high-speed clock at the PLL_CLK pin of the USB3 PHY. Only the REGM, REGN, and SD divider values are used within the DPLL clock generator subsystem to adjust the CLKDCOLDO output clock frequency. This is done through programming the PLLCTRL_USB_OTG_SS.PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION1[20:9], PLL_REGM, PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION1[8:1], PLL_REGN, and PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION3[17:10] PLL_SD bit fields, respectively. The USB3 PHY DPLL CLKOUT and CLKOUTLDO outputs are not used, and internal REGM2 and REGM1 dividers are not software controllable.

NOTE: At DPLL/PLLCTRL integration level the PLL_REGM1[3:0] and PLL_REGM2[6:0] divider control signals are hardware tie-off to 0x0 and 0x1, respectively.

For more details on output clock settings sequence, see Section 27.2.4.4.7.2, *USB3 PHY DPLL Clock Programming Sequence*.

27.2.4.4.4.2.1 USB3 PHY DPLL Output Clock Gating

There is no direct software gate control for the DPLL_USB_OTG_SS.CLKDCOLDO output.

DPLL_USB_OTG_SS.CLKDCOLDO clock output is automatically gated (CLKDCOLDO pulled low) in the following scenarios:

- DPLL power-up sequence. For more information on power-up sequence, see Section 27.2.4.4.6.1, *USB3 PHY Clock Generator Power Up*.
- DPLL entering a relock sequence. For more information on relocking sequence, see Section 27.2.4.4.6.2, *USB3 PHY DPLL Sequences*.
- DPLL entering Idle-bypass low-power mode. For more information on idle-bypass mode, see Section 27.2.4.4.6.4, *USB3 PHY DPLL Idle-Bypass Mode*.
- DPLL entering MN-bypass mode. For more information on MN-bypass mode, see Section 27.2.4.4.6.5, *USB3 PHY DPLL MN-Bypass Mode*.

27.2.4.4.5 USB3 PHY DPLL Subsystem Architecture

Figure 27-12 is a simplified block diagram of the DPLL_USB_OTG_SS instance integration in the USB3 PHY clock generator subsystem.

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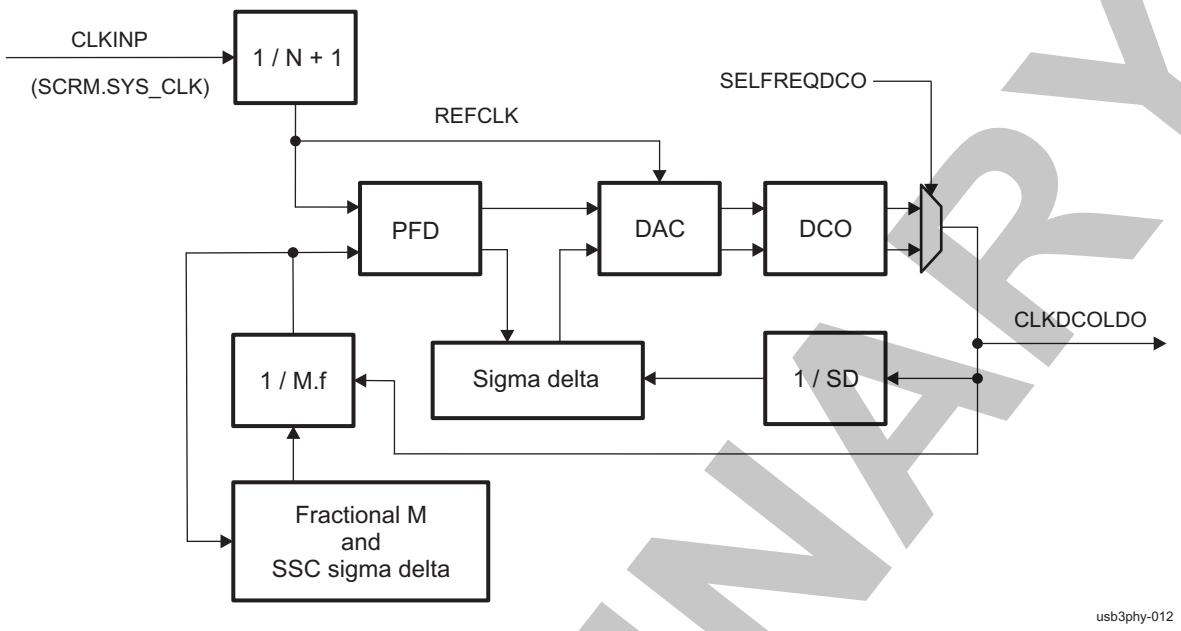
Figure 27-12. DPLL_USB_OTG_SS Functional Block Diagram



The input clock CLKINP goes to a predivider N + 1. The entire loop runs on the REFCLK clock after this predivider. The value of N + 1 is controlled through the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION1[8:1] PLL_REGN bit field.

The frequency ranges for the DPLL_USB_OTG_SS input clock - CLKINP and the DPLL internal reference clock, REFCLK = CLKINP / N + 1 are:

- 0.62 to 60 MHz for CLKINP
- 0.62 to 2.5 MHz for the REFCLK

The output clock CLKDCOLDO is synthesized by digitally controlled oscillator (the DCO block), that automatically detects the frequency range. The CLKDCOLDO frequency can be given with CLKDCOLDO = CLKINP×M / (N + 1). For that purpose the feedback multiplier M must be configured through the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION1[20:9] PLL_REGM bit field.

The DPLL_USB_OTG_SS module supports fractional synthesis (that is, the frequency multiplication factor M can be programmed as fractional). This is achieved by having a sigma delta feedback divider (M). A fractional value (Fractional M) of 18 bits is supported, thus enabling control for a better accuracy. Programming the 18-bit Fractional M value is done by setting the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION4[17:0] PLL_REGM_F bit field (similar to REGM). To enable integer only division, Fractional M should be set to 000…0.

NOTE: Fractional synthesis is not supported for M>4093.

The module also supports SSC on its output clocks. SSC is used to spread the spectral peaking of the clock to reduce any electromagnetic interference (EMI). When SSC is enabled, the clock spectrum is spread by the amount of frequency spread, and the attenuation is given by the ratio of the frequency spread (df) and the modulation frequency (fm); that is, {10×log10(df/fm)} dB.

The SSC is performed by changing the feedback divider (M) in a triangular pattern, which means the frequency of the output clock varies in a triangular pattern. The frequency of the triangular pattern is modulation frequency (fm). The peak (dM) or the amplitude of the triangular pattern as a percent of M is equal to the percent of the frequency spread (df); that is, $dM/M = df/F_{OUT}$.

Because this is in-band modulation for the DPLL_USB_OTG_SS, the modulation frequency must be within the loop bandwidth of the DPLL. A higher modulation frequency would result in less spreading in the output clock.

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The SSC can be enabled and disabled by asserting the PLLCTRL_USB_OTG_SS.PLL_SSC_CONFIGURATION1[0] EN_SSC bit. The acknowledge signal SSCACK, observed by the PLLCTRL_USB_OTG_SS.PLL_STATUS[12] SSC_EN_ACK bit, notifies the exact start and end of SSC. When EN_SSC is deasserted, SSC is disabled only after completion of one full cycle of the triangular pattern given by the modulation frequency. This is done to maintain the average frequency.

The modulation frequency (fm) can be programmed as a ratio of REFCLK/4; that is, the value programmed in the PLLCTRL_USB_OTG_SS.PLL_SSC_CONFIGURATION2[29:20] MODFREQDIVIDER bit field must be = REFCLK/(4×fm).The ModFreqDivider is split into Mantissa and $2^{Exponent}$ (ModFreqDivider = ModFreqDividerMantissa × $2^{ModFreqDividerExponent}$).

- The Mantissa is controlled by bits [29:23] of the PLLCTRL_USB_OTG_SS.PLL_SSC_CONFIGURATION2[29:20] MODFREQDIVIDER bit field.
- The Exponent is controlled by bits [22:20] of the PLLCTRL_USB_OTG_SS.PLL_SSC_CONFIGURATION2[29:20] MODFREQDIVIDER bit field.

Although the same value of ModFreqDivider could be obtained by different combinations of Mantissa and Exponent values, it is preferred to get the target ModFreqDivider by programming maximum Mantissa and minimum Exponent values.

To define the frequency spread (df), dM must be controlled as previously explained. To define dM, the step size of M for each REFCLK during the triangular pattern must be programmed.This is defined as follows:

- dM =($2^{ModFreqDividerExponent}$) × ModFreqDividerMantissa × DeltaMStep, if ModFreqDividerExponent <= 3
- dM = 8 × ModFreqDividerMantissa × DeltaMStep, if ModFreqDividerExponent > 3

DeltaMStep value is split into integer part and fractional part, as follows:

- The MSB of 3-bit integer part, DeltaMStepInteger, is controlled by the PLLCTRL_USB_OTG_SS.PLL_SSC_CONFIGURATION2[30] DELTAM2 bit and the remaining LSBs by bits [19:18] of the PLLCTRL_USB_OTG_SS.PLL_SSC_CONFIGURATION2[19:0] DELTAM bit field.
- The 18-bit fractional part, DeltaMStepFraction, is controlled by bits [17:0] of the PLLCTRL_USB_OTG_SS.PLL_SSC_CONFIGURATION2[19:0] DELTAM bit field.

If the PLLCTRL_USB_OTG_SS.PLL_SSC_CONFIGURATION1[2] DOWNSPREAD bit is set to 1, the frequency spread on the lower side is twice the programmed value. The frequency spread on the higher side is 0 (except for 20 percent overshot).

27.2.4.4.6 USB3 PHY DPLL Clock Generator Modes and State Transitions

The DPLL_USB_OTG_SS can be set in different modes during operation. PLLCTRL triggers DPLL_USB_OTG_SS state transitions to different static modes by means of the TINITZ and TENABLE hardware control signals.

27.2.4.4.6.1 USB3 PHY Clock Generator Power Up

After power up, the DPLL_USB_OTG_SS.SYSRESETN input is automatically pulled low by the PRM, together with the PLLCTRL_USB_OTG_SS.RESET_N input. Because PRM.L3INIT_RST is an asynchronous reset, the DPLL_USB_OTG_SS input clock (DPLL_USB_OTG_SS.CLKINP) is not demanded upon reset. The LOSSREF signal, which monitors the presence of CLKINP clock, remains 1 during SYSRESETN = 0 irrespective of presence/absence of the CLKINP clock. If CLKINP is present when reset is asserted, the LOSSREF signal is deasserted to 0, a certain time after the hardware reset completes. During DPLL power-up mode, CLKDCOLDO clock is maintained inactive (pulled low). After power-up reset, the DPLL_LOCK (internal lock loop) signal is maintained deasserted, too.

27.2.4.4.6.2 USB3 PHY DPLL Sequences

Once all the configuration values have been initially programmed into the PLLCTRL_USB_OTG_SS registers (see Section 27.2.4.4.7.2) , the PLLCTRL_USB_OTG_SS.PLL_GO[0] PLL_GO bit should be set to update the configuration values and start the DPLL calibration and locking sequence.

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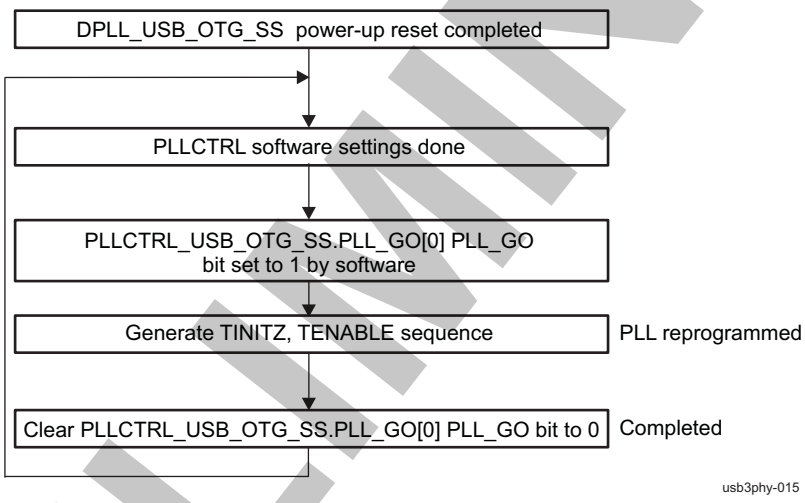
After the PLLCTRL_USB_OTG_SS.PLL_GO[0] PLL_GO bit is set high in software, the PLLCTRL_USB_OTG_SS state-machine takes the following action:

1. Sets the TINITZ signal to 0, which acts as a soft reset to DPLL_USB_OTG_SS. This starts the DPLL initialization procedure. During initialization mode, the CLKDCOLDO, FREQLOCK, and PHASELOCK signals are kept at 0 and the BYPASSACK signal is kept at 1.
   VDDA power supply of DPLL should be active before DPLL_USB_OTG_SS Initialization is performed, but it is not required to be switched on immediately after device power up.
2. The TENABLE signal is asserted high by PLLCTRL hardware to load the user-programmed values of REGM, REGN, REGSD, and SELFREQDCO into DPLL registers.
3. After TENABLE is asserted, TINITZ is driven high (disabled) by the PLLCTRL to trigger a DPLL calibration and lock sequence after the loop control values are loaded. The module calibration-lock sequence will begin from the first CLKINP edge after TINITZ is disabled.

Figure 27-13 summarizes the software and hardware sequences flow of DPLL_USB_OTG_SS.

NOTE: All thick-outlined blocks show operations performed by software. Other blocks show operations performed by hardware.

Figure 27-13. USB3 PHY PLL GO Sequence



DPLL_USB_OTG_SS relock sequence:

When the DPLL leaves a lost clock condition (LOSSREF = 1 → 0) or idle-bypass mode it enters relock sequence from the first CLKINP edge (after bypass mode leaving). Relock sequence is the same as calibration-lock sequence already described.

A DPLL relock sequence is also software triggered by setting the PLLCTRL_USB_OTG_SS.PLL_GO[0] PLL_GO bit to 0b1 for DPLL parameters update.

When DPLL_USB_OTG_SS enters a relock sequence, CLKDCOLDO is pulled low. FREQLOCK and PHASELOCK status signals are also low. CLKDCOLDO output clock is activated after the FREQLOCK or PHASELOCK signal goes high, depending on the selected locking criteria.

The PLLCTRL_USB_OTG_SS.PLL_GOUSB3PHY_PLL_GO[0] PLL_GO bit can be used by software to monitor if PLLCTRL locking process is still pending (PLL_GO = 0b1).

27.2.4.4.6.3 USB3 PHY DPLL Locked Mode

When DPLL_USB_OTG_SS finishes calibration and lock sequences it enters a locked state. During the locked state, LOSSREF and BYPASSACK are deasserted, FREQLOCK or PHASELOCK is asserted.

DPLL lock event criteria (FREQLOCK or PHASELOCK) is software-selectable through the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION2[10:9] PLL_LOCKSEL bit field.

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The DPLL signalizes the locked state to PLLCTRL_USB_OTG_SS, USB_OTG_SS core controller, and USB3 PHY through assertion of the DPLL_LOCK signal, which reflects the internal lock loop status. The user software can monitor the DPLL locked event in the PLLCTRL_USB_OTG_SS.PLL_STATUS[1] PLL_LOCK bit, which is active high.

27.2.4.4.6.4 USB3 PHY DPLL Idle-Bypass Mode

Idle-bypass fast relock mode is not supported for DPLL_USB_OTG_SS.

DPLL_USB_OTG_SS supports idle-bypass low-power mode. A transition from a normal operation to idle-bypass mode is performed when software sets the PLLCTRL_USB_OTG_SS.PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION2[0] PLL_IDLE bit to 0x1. IDLE signal assertion triggers a power-down sequence on DPLL internal LDO analog blocks and the DCO oscillator.

In idle-bypass low-power mode, the PHASELOCK and FREQLOCK output signals are asserted low and CLKDCOLDO goes low. Also, the internal reference clock REFCLK = CLKINP / N + 1 is gated inside the DPLL digital control logic to save power.

In the functional mode, the DPLL_USB_OTG_SS.TICOPWDN output indicates to the PLL controller the status of the power-down signal (active high) of the internal DCO oscillator. The internal DCO oscillator is powered down in idle-bypass mode or during period from SYSRESETN 0->1 to module initialization. The DCO oscillator exits power-down (TICOPWDN goes low) whenever the module internally tries to lock/relock after initialization or exiting idle-bypass mode.

In the functional mode, DPLL_USB_OTG_SS.LDOPWDN output indicates to the PLL controller the status of the power-down signal (active high) of the internal LDO. LDOPWDN goes high as soon as the internal LDO is powered down. LDOPWDN goes low after the LDO output voltage is stable. The internal LDO is powered down in the period from SYSRESETN 0 → 1 to module initialization or when entering into idle-bypass mode. LDOPWDN is cleared whenever the module internally tries to lock/relock after initialization or exiting idle-bypass mode after the internal LDO output voltage has stabilized.

The DCO and LDO power ON and OFF states are reflected within the read-only PLLCTRL_USB_OTG_SS.PLL_STATUS[16] PLL_TICOPWDN and PLLCTRL_USB_OTG_SS.PLL_STATUS[15] LDOPWDN monitor bits.

To exit idle-bypass mode and restore clock generation, the user should write PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION2[0] PLL_IDLE to 0x0, which deasserts the IDLE signal, and DPLL_USB_OTG_SS automatically enters a relock sequence. CLKDCOLDO output clock is activated after the FREQLOCK or the PHASELOCK signal goes high, depending on selected locking criteria.

27.2.4.4.6.5 USB3 PHY DPLL MN-Bypass Mode

The MN-bypass mode will be activated if REGM = 0 or 1 is loaded into the module on the rising edge of TENABLE. TINITZ also should be pulsed to enter MN-bypass mode. The module enters a low-power mode by gating all its internal clocks (REFCLK) and powering down internal LDO (LDOPWDN = 1) and DCO (DCOPWDN = 1). CLKDCOLDO remains gated (low) during this mode.

NOTE: When the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION1[20:9] PLL_REGM bit field is updated to 0x0 or 0x1, the CLKDCOLDO is gated.

27.2.4.4.6.6 USB3 PHY DPLL Error Conditions

The PLL lock and recalibration signals can be monitored to detect the loss-of-lock condition and the DPLL requirement to recalibrate (caused by a large temperature change since the last lock request):

- The PLLCTRL_USB_OTG_SS.PLL_STATUS[2] PLL_RECAL bit informs whether the DPLL_USB_OTG_SS must be recalibrated.

The PLL reference clock (CLKINP) loss status and PLL-in-high-jitter condition can also be monitored:

- The PLLCTRL_USB_OTG_SS.PLL_STATUS[1] PLL_LOCK bit gives the USB3 PHY PLL lock state.
- The PLLCTRL_USB_OTG_SS.PLL_STATUS[3] PLL_LOSSREF bit informs whether the

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PLLCTRL_USB_OTG_SS has lost the reference clock.

- The PLLCTRL_USB_OTG_SS.PLL_STATUS[5] PLL_HIGHJITTER bit informs whether the PLL has entered a high-jitter condition.

27.2.4.4.7 USB3 PHY PLL Controller Functions

27.2.4.4.7.1 USB3 PHY PLL Controller Register Access

The configuration registers are accessed through the OCP2SCP1 L4 adapter register space using the SCP interface of the PLLCTRL_USB_OTG_SS. This includes all the configuration signals and returning status signals.

CAUTION

All writes must be 32-bit operations, because the SCP interface always transfers 32 bits; 16- or 8-bit operations may lead to unpredictable errors.

NOTE: Because the USB3 PHY directly provides parallel data interface clocks RX_CLK and TX_CLK to the USB_OTG_SS MAC controller, the PLLCTRL_USB_OTG_SS and DPLL_USB_OTG_SS must be configured before any data transfer between the USB_OTG_SS controller MAC layer and an external USB3 device.

27.2.4.4.7.2 USB3 PHY DPLL Clock Programming Sequence

The DPLL_USB_OTG_SS factors must be calculated based on the required input and output frequencies, keeping the PLL internal reference frequency (REFCLK) in the appropriate range (0.62 to 2.5 MHz).

- REGM factor is programmed in the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION1[20:9] PLL_REGM bit field.
- Fractional part of REGM factor is programmed in the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION4[17:0] PLL_REGM_F bit field.
- REGN factor is programmed in the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION1[8:1] PLL_REGN bit field.
- DCO frequency range is set in the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION2[3:1] PLL_SELFREQDCO bit field.
  - PLL_SELFREQDCO should be set to 0x2 if 500 MHz < CLKDCOLDO [MHz] < 1000 MHz.
  - PLL_SELFREQDCO should be set to 0x4 if 1000 MHz < CLKDCOLDO [MHz] < 2000 MHz.
- SD divider is programmed in the PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION3[17:10] PLL_SD bit field. The PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION2[3:1] PLL_SELFREQDCO register bit field should be programmed depending on the value of CLKDCOLDO = CLKINP × M / (N + 1).

Figure 27-14 shows the formulae and programming sequence.

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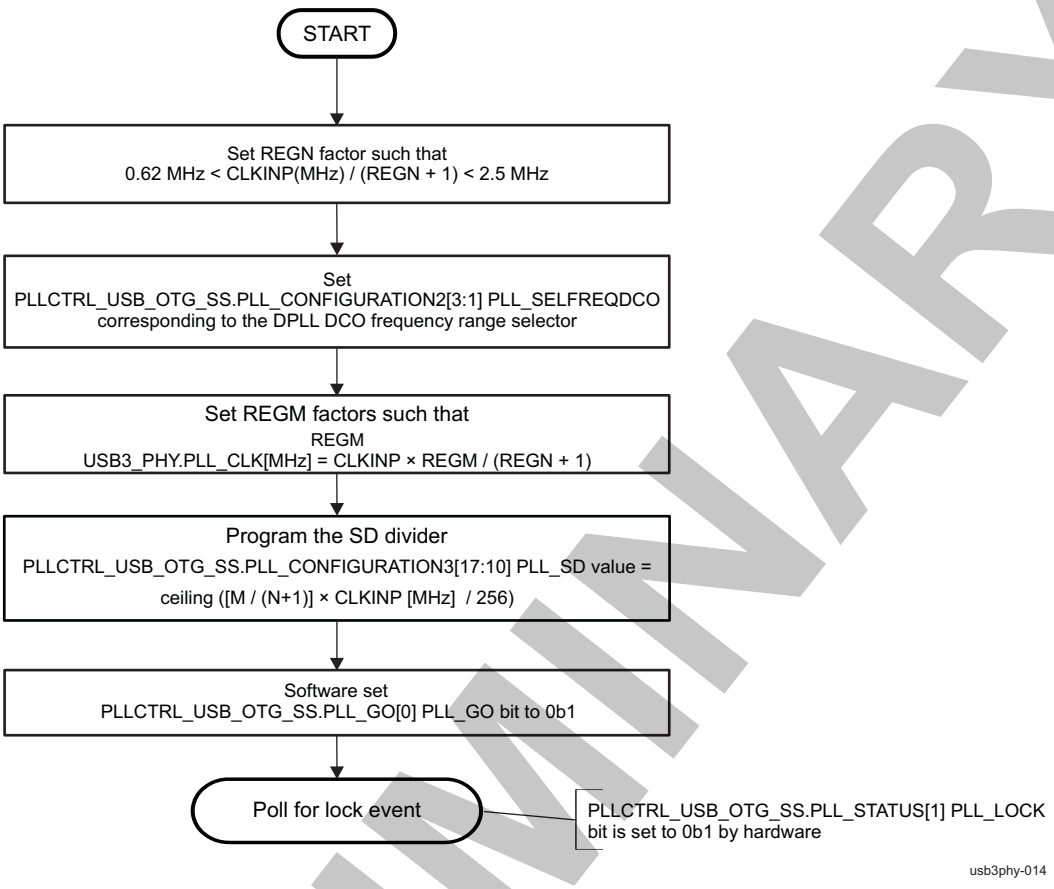
Figure 27-14. USB3 PHY PLL Programming Sequence



NOTE:

- The equation for USB3_PHY_TX/USB3_PHY_RX (MHz) applies to the CLKDCOLDO of the DPLL_USB_OTG_SS.
- CLKDCOLDO output frequency of the DPLL_USB_OTG_SS should be programmed to 2.5 GHz, for the super-speed USB (5 Gbps) mode.

Table 27-14 summarizes the registers for the PLLCTRL_USB_OTG_SS programming sequence.

Table 27-14. Register Call Summary for USB3 PHY PLL Programming Sequence

Register Name	Register Name	Register Name	Register Name
PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION2	PLLCTRL_USB_OTG_SS.PLL_GO	PLLCTRL_USB_OTG_SS.PLL_STATUS	PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION3

27.2.4.4.7.3 USB3 PHY DPLL Recommended Values

Table 27-15 lists the DPLL_USB_OTG_SS recommended values.

Table 27-15. Recommended Programming Values

Field Name	Value	Description
PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION1[20:9] PLL_REGM	See (1).	Feedback clock divider
PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION1[8:1] PLL_REGN	See (1).	Reference clock divider

(1) The value of the bit field must be set according to the desired clock frequency.

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Table 27-15. Recommended Programming Values (continued)

Field Name	Value	Description
PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION 2[10:9] PLL_LOCKSEL	0x-	Criteria to lock the PLL
PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION 2[3:1] PLL_SELFREQDCO	See (1).	Program based on the PLL choice and lock frequency.
PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION 2[0] PLL_IDLE	0	PLL active
PLLCTRL_USB_OTG_SS.PLL_CONFIGURATION 3[17:10] PLL_SD	See (1).	Ceiling { [PLL_REGM / (PLL_REGN+1)] × CLKINP(MHz) / 256 }
PLLCTRL_USB_OTG_SS.PLL_GO[0] PLL_GO	0x1	Write 1 when PLL is to be (re)locked with new parameters. This bit is cleared by hardware when the PLL request completes.

27.2.5 USB3 PHY Subsystem Low-Level Programming Model

The low-level programming sequence to set up the USB3 PHY subsystem for USB superspeed I/O operations is summarized in the Table 27-16

Table 27-16. USB3 PHY Subsystem Low-Level Programming Sequence

Step	Description	Comment
1.	Set the startup low performance OPP in the appropriate PRCM registers.	For more information regarding demanded OPP, see the device *Data Manual*.
2.	Enable the PRCM.USB_OTG_SS_REF_CLK.	See Section 3.6.4.5, *Clock Domain Module Attributes*, in Chapter 3, *Power, Reset, and Clock Management*.
3.	Enable the PRCM.L3INIT_L4_GICLK to enable the OCP2SCP1 interface adapter operation.	See Section 3.6.4.5, *Clock Domain Module Attributes*, in Chapter 3, *Power, Reset, and Clock Management*.
4.	Software reset the OCP2SCP1 and poll until soft reset completion is indicated in status.	See Section 27.2.4.2.
5.	Set up division ratio between the OCP clock (PRCM.L3INIT_L4_GICLK) and SCP clock to supply the serial configuration register domains of the PLLCTRL_USB_OTG_SS .	See Section 27.2.4.2.
6.	Set up necessary SYNC1 and SYNC2 timings to ensure no blocking of transactions over the SCP bus.	See Section 27.2.4.2. After this step, the user is ready to access the PLLCTRL_USB_OTG_SS registers.
7.	Configure DPLL_USB_OTG_SS to generate frequency (CLKDCOLDO) = 2.5 GHz.	See Section 27.2.4.4.7.2.
8.	Software-assert the PLLCTRL_USB_OTG_SS.PLL_GO[0] PLL_GO bit to 0x1	Start the DPLL lock with desired parameters.
9.	Poll the PLLCTRL_USB_OTG_SS.PLL_STATUS[1] PLL_LOCK bit until it reads 1.	DPLL locked event
10.	Perform a USB3_PHY tuning required for the Super-Speed OTG USB i/f operation	Follow steps described in Table 27-17, *USB3 PHY Tuning Table*.
11.	Set USBOTGSS_GUSB3PIPECTL[31] PHYSOFTRST to 0x1	Software reset the USB3 PHY over USB OTG SS controller PIPE port. Note that this reset does NOT impact settings made in step 10.
12.	Software-trigger the USB3_PHY_TX power-up sequence.	For more details, see Section 27.2.4.3.3.1.
13.	Software-trigger the USB3_PHY_RX power-up sequence.	For more details, see Section 27.2.4.3.3.1.

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Table 27-16. USB3 PHY Subsystem Low-Level Programming Sequence (continued)

Step	Description	Comment
14.	Clear USBOTGSS_GUSB3PIPECTL[31] PHYSOFTRST to 0x0	Deassert the software reset bit after power-up sequence completion is indicated

Table 27-17. USB3 PHY Tuning Table

Physical address[1] [bits to modify]	Preferred value setting[2]
0x4A08 440C [31:27]	**0b10000**
0x4A08 440C [17:14]	**0b1010**
0x4A08 4428 [23:11]	**0b1110001100110**
0x4A08 4428 [28:26]	**0b001**
0x4A08 440C [6:5]	**0b00**
0x4A08 441C [31:30]	**0b10**
0x4A08 4424 [31:30]	**0b11**
0x4A08 4438 [10:7]	**0b1001**
0x4A08 4438 [2]	**0b0**

(1) Accesses to these locations have to be done in 32-bits only. User must NOT modify USB3 PHY bits different than those described in Table 27-17.

(2) These are the preferred settings of USB3_PHY, in case that USB3 PHY PLL_CLK=2.5 GHz.

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27.3 USB3 PHY and SATA PHY PLL Controllers Register Manual

This chapter summarizes the SATA and USB3 PHY Subsystems PLL Controller registers

27.3.1 USB3 PHY and SATA PHY PLL Controllers Instance Summary

Table 27-18. USB3 PHY and SATA PHY PLL Controllers Instance Summary

Module Name	Module Base Address	Size
OCP2SCP1	0x4A08 0000	1 KiB
OCP2SCP3	0x4A09 0000	1 KiB
PLLCTRL_USB_OTG_SS	0x4A08 4C00	64 bytes
PLLCTRL_SATA	0x4A09 6800	64 bytes

27.3.2 OCP2SCP Registers

27.3.2.1 OCP2SCP Register Summary

Table 27-19. OCP2SCP Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	OCP2SCP1 Physical Address	OCP2SCP3 Physical Address
OCP2SCP_REVISION	R	32	0x0000 0000	0x4A08 0000	0x4A09 0000
OCP2SCP_SYSCONFIG	RW	32	0x0000 0010	0x4A08 0010	0x4A09 0010
OCP2SCP_SYSSTATUS	R	32	0x0000 0014	0x4A08 0014	0x4A09 0014
OCP2SCP_TIMING	RW	32	0x0000 0018	0x4A08 0018	0x4A09 0018

27.3.2.2 OCP2SCP Register Description

Table 27-20. OCP2SCP_REVISION

Address Offset	0x0000 0000		
Physical Address	0x4A08 0000 0x4A09 0000	**Instance**	OCP2SCP1 OCP2SCP3
Description	IP Revision Identifier (X.Y.R)		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision	R	See (1)

(1) TI internal data

Table 27-21. Register Call Summary for Register OCP2SCP_REVISION

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- OCP2SCP Register Summary: [0]

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Table 27-22. OCP2SCP_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x4A08 0010 0x4A09 0010	**Instance**	OCP2SCP1 OCP2SCP3
Description	SYSTEM CONFIGURATION REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											IDLEMODE		RESERVED	SOFTRESET	AUTOIDLE

Bits	Field Name	Description	Type	Reset
31:5	RESERVED	Reserved	R	0x000 0000
4:3	IDLEMODE	0x0: Force Idle mode. An idle request is acknowledged unconditionally. 0x1: No Idle mode. An idle request is never acknowledged. 0x2: Smart Idle mode. The acknowledgement to an idle request is given based on the internal activity. 0x3: Reserved	RW	0x2
2	RESERVED	Reserved.	R	0
1	SOFTRESET	Software Reset. Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware. During reads, it always returns 0. 0x0: Normal Mode 0x1: The module is reset.	RW	0
0	AUTOIDLE	L4-interconnect interface clock gating control. 0x0: Internal L4-interconnect interface clock is free-running 0x1: Automatic internal L4-interconnect interface clock gating, based on the L4-interconnect interface activity	RW	1

Table 27-23. Register Call Summary for Register OCP2SCP_SYSCONFIG

SATA PHY Subsystem
- SATA PLL Controller L4 Interface Adapter Functional Description: [5] [6] [7]

USB3 PHY Subsystem
- Super-Speed USB PLL Controller L4 Interface Adapter Functional Description: [12] [13] [14]

USB3 PHY and SATA PHY Register Manual
- OCP2SCP Register Summary: [15]

Table 27-24. OCP2SCP_SYSSTATUS

Address Offset	0x0000 0014		
Physical Address	0x4A08 0014 0x4A09 0014	**Instance**	OCP2SCP1 OCP2SCP3
Description	System Status register.		
Type	R		

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															RESETDONE

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0x0000 0000
0	RESETDONE	Read 0x1: Reset completed Read 0x0: Internal Reset is on-going	R	1

Table 27-25. Register Call Summary for Register OCP2SCP_SYSSTATUS

SATA PHY Subsystem • SATA PLL Controller L4 Interface Adapter Functional Description: [1]
USB3 PHY Subsystem • Super-Speed USB PLL Controller L4 Interface Adapter Functional Description: [3]
USB3 PHY and SATA PHY Register Manual • OCP2SCP Register Summary: [4]

Table 27-26. OCP2SCP_TIMING

Address Offset	0x0000 0018		
Physical Address	0x4A08 0018 0x4A09 0018	**Instance**	OCP2SCP1 OCP2SCP3
Description	Interrupt Status Register (legacy) for first line of interrupt.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						DIVISIONRATIO		SYNC1				SYNC2			

Bits	Field Name	Description	Type	Reset
31:10	RESERVED	Reserved.	R	0x00 0000
9:7	DIVISIONRATIO(1)	Division Ration of the SCP clock in relation to OCP input clock.	RW	0x0
6:4	SYNC1	Number of SCPclock cycles defining SYNC1	RW	0x0
3:0	SYNC2	Number of SCPclock cycles defining SYNC2	RW	0x1

(1) When value “000” is programmed for the SCP clock division ratio, and the transaction to be made is a valid transaction on the SCP interface, the DIVISIONRATIO value is set internally to 0x7 (to avoid a block on the OCP interface).

Table 27-27. Register Call Summary for Register OCP2SCP_TIMING

SATA PHY Subsystem • SATA PLL Controller L4 Interface Adapter Functional Description: [4] • SATA_PHY Clocking:
USB3 PHY Subsystem • Super-Speed USB PLL Controller L4 Interface Adapter Functional Description: [10] • USB3 PHY Subsystem Clocking:

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Table 27-27. Register Call Summary for Register OCP2SCP_TIMING (continued)

USB3 PHY and SATA PHY Register Manual • OCP2SCP Register Summary: [12]

CAUTION

To ensure correct operation, DIVISIONRATIO must not be modified. CAUTION: To ensure correct operation, the value of SYNC2 must be set to 0x6 or more.

27.3.3 PLLCTRL Registers

27.3.3.1 PLLCTRL Register Summary

Table 27-28. PLLCTRL Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	PLLCTRL_USB_OTG_SS Physical Address	PLLCTRL_SATA Physical Address
RESERVED	R	32	0x0000 0000	0x4A08 4C00	0x4A09 6800
PLL_STATUS	R	32	0x0000 0004	0x4A08 4C04	0x4A09 6804
PLL_GO	RW	32	0x0000 0008	0x4A08 4C08	0x4A09 6808
PLL_CONFIGURATION1	RW	32	0x0000 000C	0x4A08 4C0C	0x4A09 680C
PLL_CONFIGURATION2	RW	32	0x0000 0010	0x4A08 4C10	0x4A09 6810
PLL_CONFIGURATION3	RW	32	0x0000 0014	0x4A08 4C14	0x4A09 6814
PLL_SSC_CONFIGURATION1	RW	32	0x0000 0018	0x4A08 4C18	0x4A09 6818
PLL_SSC_CONFIGURATION2	RW	32	0x0000 001C	0x4A08 4C1C	0x4A09 681C
PLL_CONFIGURATION4	RW	32	0x0000 0020	0x4A08 4C20	0x4A09 6820

27.3.3.2 PLLCTRL Register Description

Table 27-29. PLL_STATUS

Address Offset	0x0000 0004		
Physical Address	0x4A08 4C04 0x4A09 6804	**Instance**	PLLCTRL_USB_OTG_SS PLLCTRL_SATA
Description	This register contains the status information		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PLL_TICOPWDN	PLL_LDOPWDN	RESERVED		SSC_EN_ACK	RESERVED				PLL_HIGHJITTER	RESERVED		PLL_LOSSREF	PLL_RECAL	PLL_LOCK	PLLCTRL_RESET_DONE

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Bits	Field Name	Description	Type	Reset
31:17	RESERVED		R	0x0000
16	PLL_TICOPWDN	PLL TICOPWDN status. Read 0x1: Internal oscillator power down Read 0x0: Internal oscillator power up	R	0
15	PLL_LDOPWDN	PLL LDOPWDN status. Read 0x1: PLL's internal LDO is power down Read 0x0: PLL's internal LDO is power up	R	0
14:13	RESERVED			0
12	SSC_EN_ACK	Spread Spectrum Clocking acknowledge Read 0x1: Spread Spectrum Clocking active Read 0x0: Spread Spectrum Clocking inactive	R	0
11:6	RESERVED		R	0x00
5	PLL_HIGHJITTER	PLL High Jitter status Read 0x1: PLL in high jitter condition: Phase error > 24% Read 0x0: PLL in normal jitter condition	R	0
4	RESERVED	Read returns zero.	R	0
3	PLL_LOSSREF	PLL Reference Loss status Read 0x1: Reference input inactive Read 0x0: Reference input active	R	0
2	PLL_RECAL	PLL re-calibration status If this bit is active, the PLL needs to be re-calibrated Read 0x1: Recalibration is required Read 0x0: Recalibration is not required	R	0
1	PLL_LOCK	PLL Lock status See the programming guide for the use of this bit Read 0x1: PLL is locked Read 0x0: PLL is not locked	R	0
0	PLLCTRL_RESET_DONE	PLLCTRL reset done status Read 0x1: Reset has completed Read 0x0: Reset is in progress	R	0

Table 27-30. Register Call Summary for Register PLL_STATUS

SATA PHY Subsystem
- SATA DPLL Clock Generator Reset: [0]
- SATA DPLL Clocks Configuration: [1]
- SATA DPLL Subsystem Architecture: [2]
- SATA DPLL Clock Generator Modes and State Transitions: [3] [4] [5] [6] [7] [8] [9]
- SATA PLL Controller Functions: [10]
- SATA PHY Subsystem Low-Level Programming Model: [11]

USB3 PHY Subsystem
- USB3 PHY DPLL Clock Generator Reset: [12]
- USB3 PHY DPLL Clocks Configuration: [13]
- USB3 PHY DPLL Subsystem Architecture: [14]
- USB3 PHY DPLL Clock Generator Modes and State Transitions: [15] [16] [17] [18] [19] [20] [21]
- USB3 PHY PLL Controller Functions: [22]
- USB3 PHY Subsystem Low-Level Programming Model: [23]

USB3 PHY and SATA PHY Register Manual
- PLLCTRL Register Summary: [24]

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Table 27-31. PLL_GO

Address Offset	0x0000 0008		
Physical Address	0x4A08 4C08 0x4A09 6808	**Instance**	PLLCTRL_USB_OTG_SS PLLCTRL_SATA
Description	This register contains the GO bit		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reads return zero.	R	0x0000 0000
0	PLL_GO	Request (re-)locking sequence of the PLL. 0x0: No pending action 0x1: Request PLL (re-)locking/locking pending	RW	0

Table 27-32. Register Call Summary for Register PLL_GO

SATA PHY Subsystem
- SATA DPLL Low-Power Modes: [0]
- SATA DPLL Clock Generator Modes and State Transitions: [1] [2] [3] [4] [5] [6] [7] [8] [9]
- SATA PLL Controller Functions: [10] [11] [12]
- SATA PHY Subsystem Low-Level Programming Model: [13] [14]

USB3 PHY Subsystem
- USB3 PHY DPLL Low-Power Modes: [15]
- USB3 PHY DPLL Clock Generator Modes and State Transitions: [16] [17] [18] [19] [20] [21] [22] [23] [24] [25]
- USB3 PHY PLL Controller Functions: [26] [27] [28]
- USB3 PHY Subsystem Low-Level Programming Model: [29] [30]

USB3 PHY and SATA PHY Register Manual
- PLLCTRL Register Summary: [31]
- PLLCTRL Register Description: [32]

Table 27-33. PLL_CONFIGURATION1

Address Offset	0x0000 000C		
Physical Address	0x4A08 4C0C 0x4A09 680C	**Instance**	PLLCTRL_USB_OTG_SS PLLCTRL_SATA
Description	This register contains the latched PLL and HSDIVDER configuration bits		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PLL_REGM										PLL_REGN								RESERVED	

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20:9	PLL_REGM	M Divider for PLL	RW	0x000
8:1	PLL_REGN	N Divider for PLL (Reference)	RW	0x00
0	RESERVED	Read returns zero.	R	0

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Table 27-34. Register Call Summary for Register PLL_CONFIGURATION1

SATA PHY Subsystem
- SATA DPLL Clocks Configuration: [0] [1]
- SATA DPLL Subsystem Architecture: [2] [3]
- SATA DPLL Clock Generator Modes and State Transitions: [4]
- SATA PLL Controller Functions: [5] [6] [7] [8]

USB3 PHY Subsystem
- USB3 PHY DPLL Clocks Configuration: [9] [10]
- USB3 PHY DPLL Subsystem Architecture: [11] [12]
- USB3 PHY DPLL Clock Generator Modes and State Transitions: [13]
- USB3 PHY PLL Controller Functions: [14] [15] [16] [17]

USB3 PHY and SATA PHY Register Manual
- PLLCTRL Register Summary: [18]

Table 27-35. PLL_CONFIGURATION2

Address Offset	0x0000 0010		
Physical Address	0x4A08 4C10 0x4A09 6810	**Instance**	PLLCTRL_USB_OTG_SS PLLCTRL_SATA
Description	This register contains the unlatched PLL and HSDIVDER configuration bits These bits are "shadowed" when automatic mode is selected		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					PLL_LOCKSEL		RESERVED					PLL_SELFREQDCO			PLL_IDLE

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x00004
10:9	PLL_LOCKSEL	Selects the lock criteria for the PLL 0x0: Phase Lock 0x1: Frequency Lock Other values: Reserved	RW	0x0
8:4	RESERVED		R	0x00
3:1	PLL_SELFREQDCO	DCO frequency range selector for DPLL_USB_OTG_SS 0x2 Set if DCO frequency is between 500MHz and 1000MHz 0x4 Set if DCO frequency is between 1000MHz and 2000MHz Other values: Reserved	RW	0x4
0	PLL_IDLE	PLL IDLE: 0x0: IDLE is not selected 0x1: IDLE is selected	RW	0

Table 27-36. Register Call Summary for Register PLL_CONFIGURATION2

SATA PHY Subsystem
- SATA DPLL Clock Generator Modes and State Transitions: [0] [1] [2]
- SATA PLL Controller Functions: [3] [4] [5] [6] [7] [8]

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Table 27-36. Register Call Summary for Register PLL_CONFIGURATION2 (continued)

USB3 PHY Subsystem • USB3 PHY DPLL Clock Generator Modes and State Transitions: [9] [10] [11] • USB3 PHY PLL Controller Functions: [12] [13] [14] [15] [16] [17]
USB3 PHY and SATA PHY Register Manual • PLLCTRL Register Summary: [18]

Table 27-37. PLL_CONFIGURATION3

Address Offset	0x0000 0014		
Physical Address	0x4A08 4C14 0x4A09 6814	**Instance**	PLLCTRL_USB_OTG_SS PLLCTRL_SATA
Description	HSDIVIDER configuration bits for the M5 and M6 dividers		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PLL_SD								RESERVED							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED		R	0x0000
17:10	PLL_SD	Sigma delta divider setting for DPLL_USB_OTG_SS based on the PLL lock configuration.	RW	0x00
9:0	RESERVED		RW	0x000

Table 27-38. Register Call Summary for Register PLL_CONFIGURATION3

SATA PHY Subsystem • SATA DPLL Clocks Configuration: [0] • SATA PLL Controller Functions: [1] [2] [3]
USB3 PHY Subsystem • USB3 PHY DPLL Clocks Configuration: [4] • USB3 PHY PLL Controller Functions: [5] [6] [7]
USB3 PHY and SATA PHY Register Manual • PLLCTRL Register Summary: [8]

Table 27-39. PLL_SSC_CONFIGURATION1

Address Offset	0x0000 0018		
Physical Address	0x4A08 4C18 0x4A09 6818	**Instance**	PLLCTRL_USB_OTG_SS PLLCTRL_SATA
Description	Configuration for PLL Spread Spectrum Clocking modulation		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													DOWNSPREAD	RESERVED	EN_SSC

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Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000
2	DOWNSPREAD	Forces the clock spreading only in the down spectrum. 0x0: Clock spreading not forced. 0x1: Spectrum spreading only in down direction.	RW	0
1	RESERVED		R	0
0	EN_SSC	Spread Spectrum Clocking enable 0x0: Spread Spectrum Clocking disabled 0x1: Spread Spectrum Clocking enabled	RW	0

Table 27-40. Register Call Summary for Register PLL_SSC_CONFIGURATION1

SATA PHY Subsystem • SATA DPLL Subsystem Architecture: [0] [1]
USB3 PHY Subsystem • USB3 PHY DPLL Subsystem Architecture: [2] [3]
USB3 PHY and SATA PHY Register Manual • PLLCTRL Register Summary: [4]

Table 27-41. PLL_SSC_CONFIGURATION2

Address Offset	0x0000 001C		
Physical Address	0x4A08 4C1C 0x4A09 681C	**Instance**	PLLCTRL_USB_OTG_SS PLLCTRL_SATA
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DELTAM2	MODFREQDIVIDER														DELTAM															

Bits	Field Name	Description	Type	Reset
31	RESERVED	Reads as zero	R	0
30	DELTAM2	MSB of DeltaM control bus.	RW	0
29:20	MODFREQDIVIDER	Modulation Frequency Divider control for SSC.	RW	0x000
19:0	DELTAM	DeltaM control for SSC.	RW	0x0 0000

Table 27-42. Register Call Summary for Register PLL_SSC_CONFIGURATION2

SATA PHY Subsystem • SATA DPLL Subsystem Architecture: [0] [1] [2] [3] [4] [5]
USB3 PHY Subsystem • USB3 PHY DPLL Subsystem Architecture: [6] [7] [8] [9] [10] [11]
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Table 27-43. PLL_CONFIGURATION4

Address Offset	0x0000 0020		
Physical Address	0x4A08 4C20 0x4A09 6820	**Instance**	PLLCTRL_USB_OTG_SS PLLCTRL_SATA
Description	Allows setting the fractional M divider and M2 divider for PLL.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PLL_REGM_F																							

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reads as 0x1	R	0x0001
17:0	PLL_REGM_F	Fractional part of M divider.	RW	0x0 0000

Table 27-44. Register Call Summary for Register PLL_CONFIGURATION4

SATA PHY Subsystem
- SATA DPLL Subsystem Architecture: [0]
- SATA PLL Controller Functions: [1]

USB3 PHY Subsystem
- USB3 PHY DPLL Subsystem Architecture: [2]
- USB3 PHY PLL Controller Functions: [3]

USB3 PHY and SATA PHY Register Manual
- PLLCTRL Register Summary: [4]

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Initialization

This chapter introduces the steps in the general-purpose (GP) device initialization.

NOTE: Some of the ROM code features, primarily those concerning the device I/O pads, are not available in all OMAP54xx devices.

For details, see Section 1.5, *OMAP543x Family and Device Identification*, in Chapter 1, *Introduction*, and the corresponding TRM appendix and device data manual.

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28.3 Device Initialization by ROM Code 5903
28.4 Services for HLOS Support 5975

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28.1 Initialization Overview

This chapter provides an overview of the requirements to initialize the OMAP™ device from power on to operating system (OS) and application execution, the overall initialization process (including hardware- and software-related steps), the general ROM code operational requirements, and behavior expectations.

28.1.1 Terminology

- **Bootstrap:** Initial software launched by the ROM code during the memory booting phase
- **Configuration Header (CH):** Optional structure that precedes the initial software and allows the redefinition of the ROM code default settings
- **Downloaded software:** Initial software downloaded into the internal static RAM (SRAM) by the ROM code during the peripheral booting phase
- **eFuse:** A one-time programmable memory location usually set at the factory
- **Flash loader:** Downloaded software launched by the ROM code during the preflashing stage. It also programs an image in external memories.
- **GP device:** General-purpose device
- **Initial software:** Software executed by any of the ROM code mechanisms (memory booting or peripheral booting). Initial software is a generic term for bootstrap and downloaded software.
- **Memory booting:** ROM code mechanism that consists of executing initial software from external memory
- **Master CPU:** The ARM® Cortex™-A15 MPCore™ CPU for which CPU-ID is 0. It configures the multicore platform and starts the ROM code to ensure device booting from a mass storage memory (memory booting) or a peripheral interface (peripheral booting).
- **Peripheral booting:** ROM code mechanism that consists of polling selected interfaces, downloading, and executing initial software (in this case, downloaded software) in the internal RAM
- **Permanent booting device:** Memory device containing, by default, the image to be executed during the booting sequence. It is the default memory booting device. The permanent booting device is used after a warm reset if no software booting configuration is programmed.
- **Preflashing:** A specific case of peripheral booting where the ROM code mechanism is used to program the external flash memory
- **ROM Code:** The on-chip software in OMAP ROM that implements booting
- **ROM Code-controlled Boot Phase:** This phase covers the sequence operations from the time the platform releases the reset to the time first user- or customer-owned software starts execution. This phase is fully controlled by the OMAP ROM code.
- **Save-And-Restore (SAR) RAM memory:** On-chip RAM memory that is not cleared after warm resets or wakeups from low-power modes
- **Slave CPU:** The ARM Cortex-A15 MPCore CPU for which CPU-ID is 1. It is brought to the wait-for-event (WFE) state by the ROM code, waiting to be woken up by the master CPU.
- **Software booting configuration:** A logical structure stored in the SAR memory that allows the redefinition of the ROM code default settings when booting after a warm reset

28.1.2 Initialization Process

Figure 28-1 is an overview of the initialization process and its steps:

- **Preinitialization:** Power, clock, and control connections must be present, and the boot configuration pins must be held at the desired logical levels.
- **Power, clock, reset ramp sequence:** Specific sequence that is applied by the power-management chip
- **ROM code:** Responsible for finding, for downloading, and for executing the initial software by using the master CPU
- **Initial software:** Software that prepares and passes control to application software or to the high-level operating system (HLOS)
- **Symmetric multiprocessing (SMP)-capable HLOS** or application (primarily for diagnostics)

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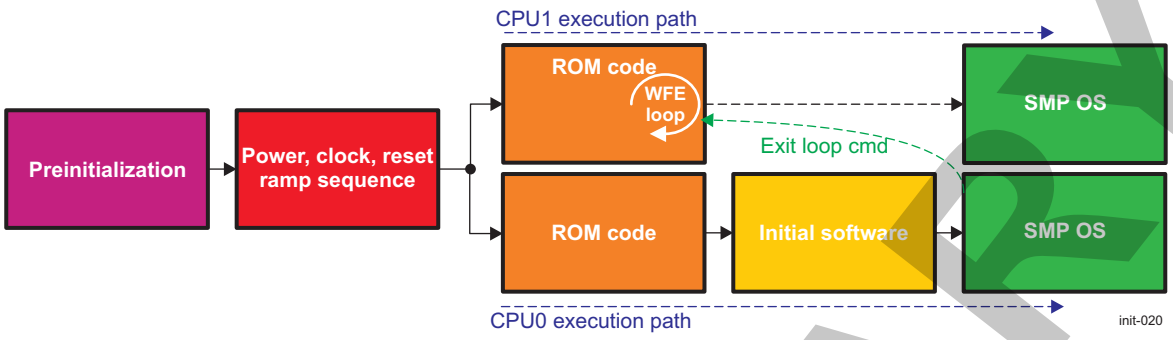
Figure 28-1. Initialization Process



The first two steps in the initialization process are hardware-oriented; however, they require an understanding of the process of configuring these system interface pins (balls on the OMAP device), which have software-configurable functionality. This configuration is an essential part of the chip configuration and is application-dependent. This chapter discusses these system-interface pins and the associated configuration registers that are vital to the correct initialization of the device.

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28.2 Preinitialization

To accomplish a successful boot-up operation with an OMAP GP device, certain hardware configuration settings must be in place. Clock, reset, and power connections, as well as pins involved in setting the boot memory space for the master CPU, must be connected and driven correctly to successfully initialize the device. The following sections describe the specific requirements for the preinitialization stage.

28.2.1 Power Requirements

The OMAP device can be supplied by an external power-management integrated circuit (PMIC). TI provides a global solution with the OMAP device connected to the power-management and audio-management IC companion chips.

Figure 28-2 shows the power connections between OMAP and the PMIC companion chip.

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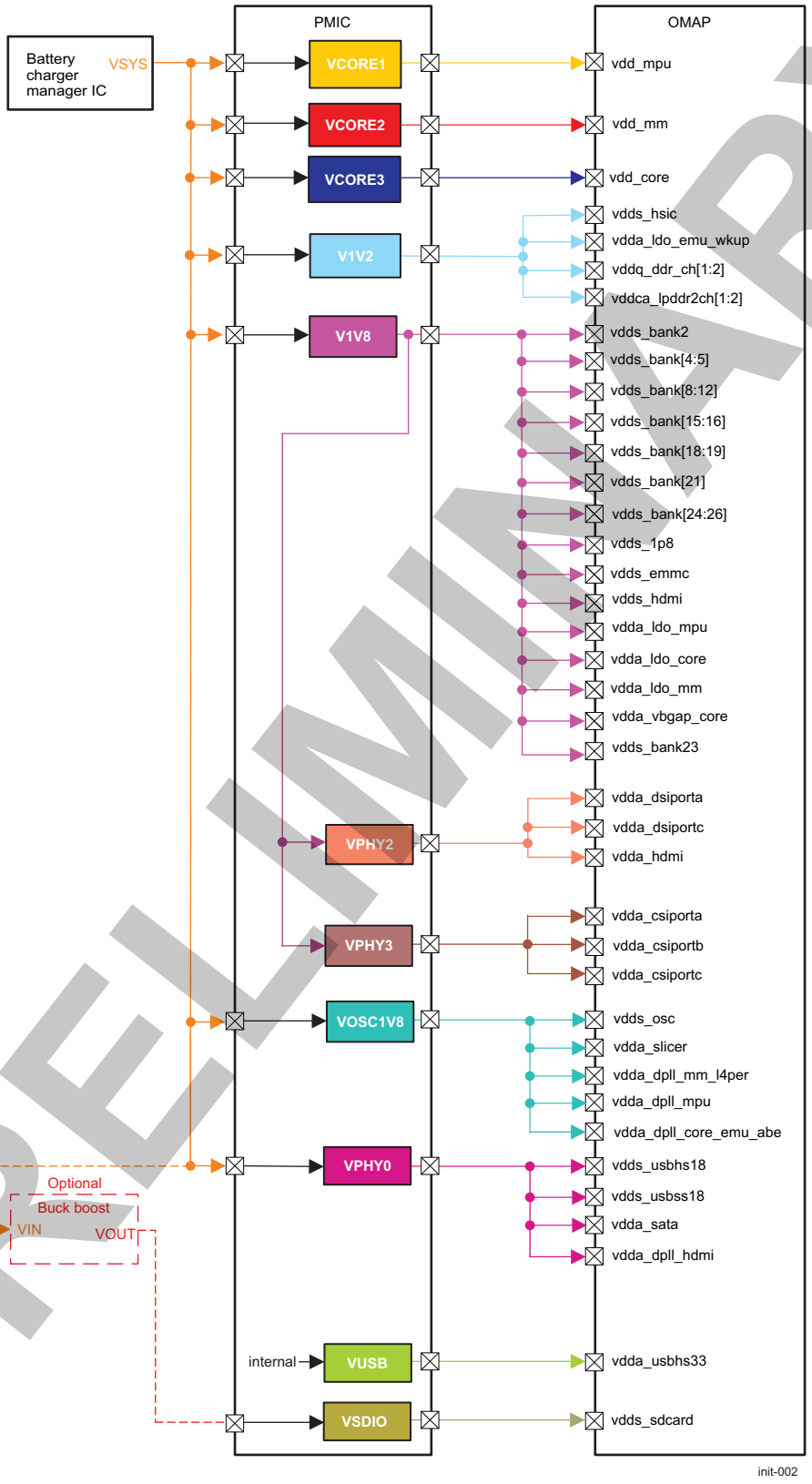
Figure 28-2. Power Supply Connections



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NOTE: Figure 28-2 is an example of power connections between the OMAP device and the PMIC. These connections depend on the actual application.

Table 28-1 describes the device power balls.

Table 28-1. OMAP Power Balls (1)

Voltage Ball Name	Power Supplied OMAP Internal Modules and Peripherals
vdd_core	OMAP subsystems and modules supplied in CORE voltage domain
vdd_mpu	• MPU subsystem
vdd_mm	• IVA subsystem • DSP subsystem • GPU subsystem
vdda_ldo_emu_wkup	• Wakeup • Emulation subsystem
vddq_ddr_ch1	EMIF channel 1 DQ I/Os (OMAP side only)
vddq_ddr_ch2	EMIF channel 2 DQ I/Os (OMAP side only)
vddq_vref_ddrch1	Supplies VDDQ_VREF generator for EMIF channel 1
vddq_vref_ddrch2	Supplies VDDQ_VREF generator for EMIF channel 2
vddca_lpddr2ch1	EMIF channel 1 CA I/Os (OMAP side only)
vddca_lpddr2ch2	EMIF channel 2 CA I/Os (OMAP side only)
vddca_vref_lpddr2ch1	Supplies VDDCA_VREF generator for EMIF channel 1
vddca_vref_lpddr2ch2	Supplies VDDCA_VREF generator for EMIF channel 2
vdds_hsic	USBB1, USBB2, USBB3 HSIC I/Os
vdda_dsiporta	DSI Port A lanes (dual-votage I/Os)
vdda_dsiportc	DSI Port C lanes (dual-votage I/Os)
vdda_hdmi	HDMI dual-votage I/Os
vdda_csiporta	CSI Port A lanes (dual-votage I/Os)
vdda_csiportb	CSI Port B lanes (dual-votage I/Os)
vdda_csiportc	CSI Port C lanes (dual-votage I/Os)
vdda_dpll_mm_l4per	Analog power supply for the DPLL_IVA and DPLL_PER
vdda_dpll_mpu	Analog power supply or the DPLL_MPU
vdda_dpll_core_emu_abe	Analog power supply fot the DPLL_CORE, DPLL_DEBUGSS, and DPLL_ABE
vdda_dpll_hdmi	Analog power supply for the DPLL_HDMI
vdda_ldo_mpu	Analog power supply for the OMAP internal MPU LDOs
vdda_ldo_core	Analog power supply for the OMAP internal CORE LDOs
vdda_ldo_mm	Analog power supply for the OMAP internal MM LDOs
vdda_vbgap_core	Analog power supply for the OMAP BANDGAPTS_CORE
vdda_usbhs33	Analog power supplies for the high speed (HS) USB I/Os
vdda_usbhs18	
vdda_usbss18	Analog power supply for SuperSpeed (SS) USB I/Os
vdda_sata	Analog power supply for SATA I/Os
vdds_sdcard	MMC1 module I/Os (SD™ card I/Os)
vdds_bank2	Bank of I/Os: HSI1, UART1 (dual-votage)
vdds_bank4	Bank of I/Os: HSI2, UART2 (dual-votage)
vdds_bank5	Bank of I/Os: TIMER9, TIMER10, DSIPORT B, DSIPORT C I/Os (dual voltage)
vdds_bank8	Bank of I/Os: MCSPI2, I2C4 (dual voltage)
vdds_bank9	Bank of I/Os: RFBI, GPIO6 (dual voltage)

(1) The package-on-package (POP) OMAP device provides feedthroughs from the bottom of the package to the POP interface. Among these feedthroughs (FEEDTHROUGH balls), several provide power to the top memory device. Based on memory requirements, the device must provide the correct power supply to the feedthroughs.

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Table 28-1. OMAP Power Balls [(1)] (continued)

Voltage Ball Name	Power Supplied OMAP Internal Modules and Peripherals
vdds_bank10	Bank of I/Os: TCTRL, TIMER5, TIMER6, TIMER8, TIMER11, I2C3, GPIO8 (dual voltage)
vdds_bank11	Bank of I/Os: ABE clocks, MCBSP2, MCPDM (dual voltage)
vdds_bank12	Bank of I/Os: DMIC (dual voltage)
vdds_bank15	Bank of I/Os: MMC3 module I/Os -("WLSDIO" dual-votage I/Os)
vdds_bank16	Bank of I/Os: UART5, I2C2 (dual voltage)
vdds_bank18	Bank of I/Os: MCSPI1, I2C5 (dual voltage)
vdds_bank19	Bank of I/Os: GPIO5 (dual voltage)
vdds_bank21	Bank of I/Os: UART6, UART3 (dual voltage)
vdds_bank23	Bank of I/Os: JTAG®
vdds_bank24	Bank of I/Os: System interface
vdds_bank25	Bank of I/Os: System interface (dual voltage)
vdds_bank26	Bank of I/Os: System interface, SmartReflex™ PMIC I^2C, I2C1 PMIC interface (dual voltage)
vdds_osc	F_{REF} XTAL oscillator (system interface I/Os)
vdda_slicer	F_{REF} slicer oscillator (system interface I/Os)
vdds_emmc	MMC2 module I/Os (eMMC I/Os)

For a complete description of the power balls on the OMAP package, see the *Device Data Manual*. For more information about power management, see Section 3.6 *Clock Management Functional Description*, in Chapter 3, *Power, Reset, and Clock Management*.

NOTE: The OMAP device package restricts the physical connection to only one memory type: LPDDR2 or DDR3. See more details about OMAP device family and packaging in Section 1.1, *Overview*, in Chapter 1, *Introduction*.

28.2.2 Interraction With the PMIC Companion

The ROM code does not perform any I^2C transactions with the PMIC. The following system conditions must be met to perform OMAP device initialization:

- The USB transceivers (USB2.0 and USB3.0 PHYs), internal to OMAP, are powered on any cold and warm reset, as expected by the USB peripheral booting feature.
- The SD card cage must be appropriately powered before entering the SD card boot feature on any cold and warm reset.
- The attached external SATA drive must be appropriately powered before entering the SATA boot feature on any cold and warm reset.

NOTE: In the OMAP device, the ROM code does not interact with the PMIC companion chip over the I^2C interface.

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28.2.3 Clock, Reset, and Control

28.2.3.1 Overview

Figure 28-3 shows the clock and reset environment where clocks and reset-related signals are gathered at the system level, the system-expansion signals, and the crystal oscillator connection scenario applicable to all OMAP devices.

Figure 28-3. Clock, Reset, and Control Environment

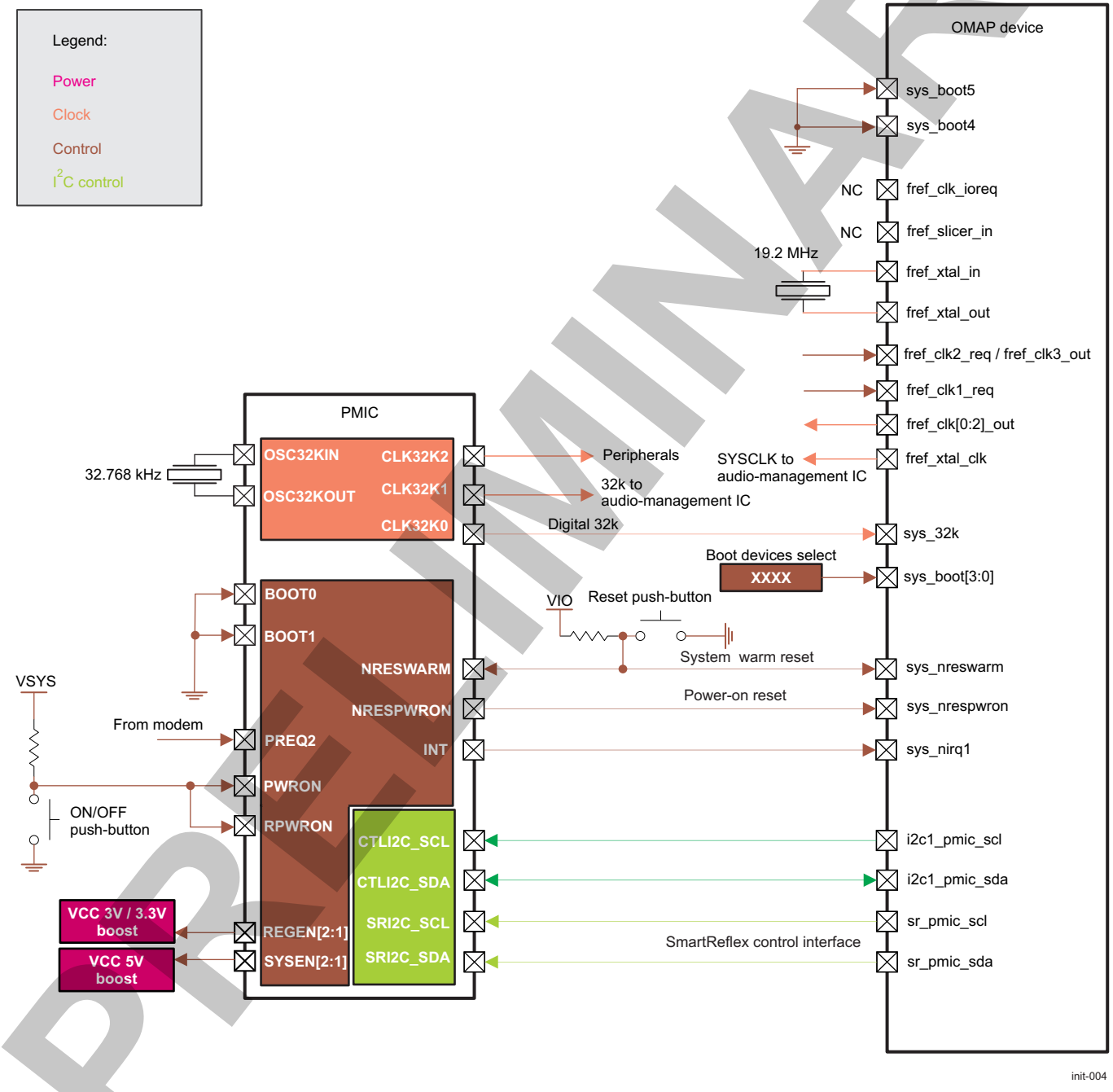

Figure 28-4 shows the device slicer-active mode connectivity scenario which applies only to the OMAP5430 device.

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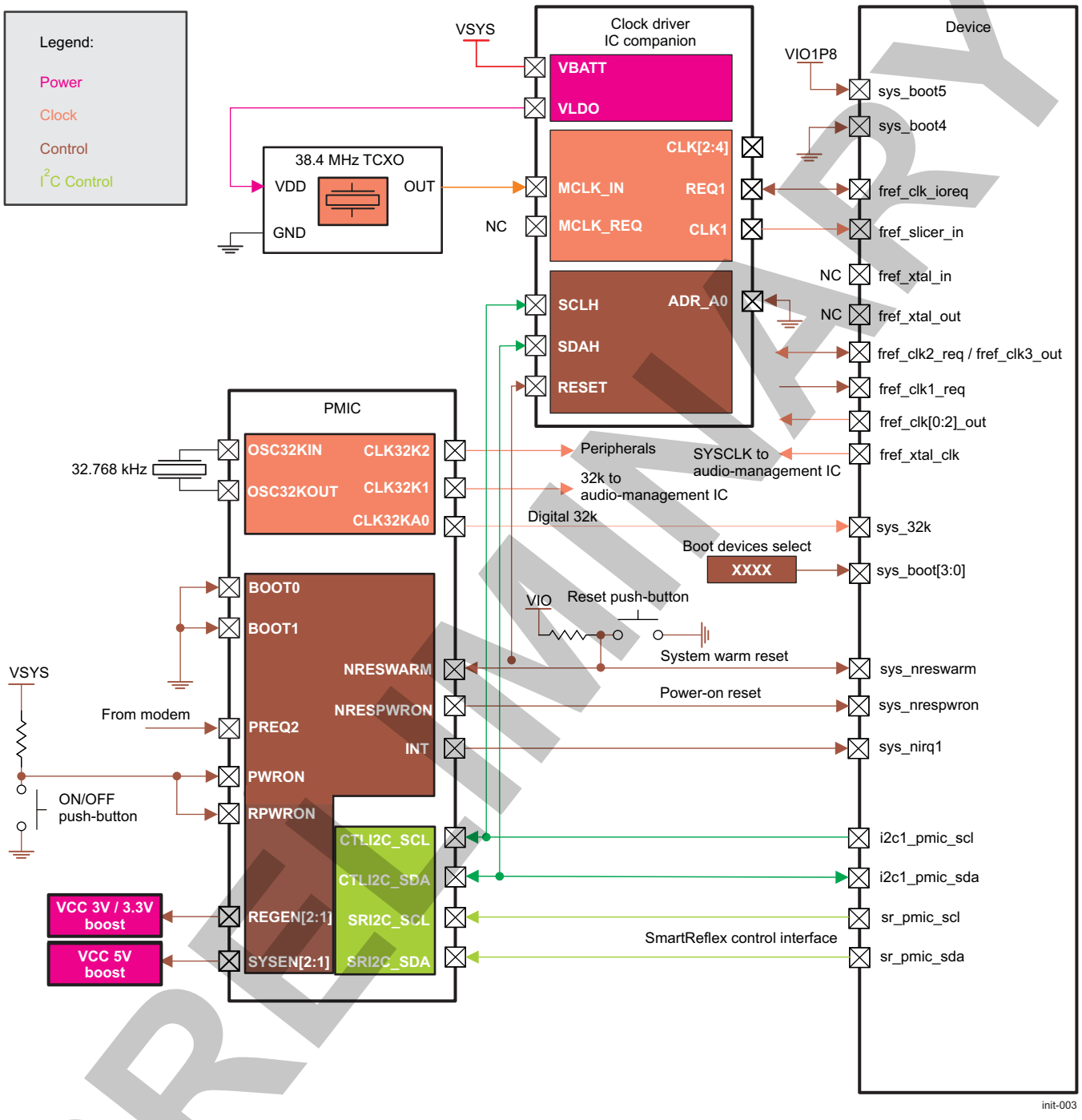
Figure 28-4. OMAP5430 Slicer-Active Mode Connectivity



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The main features of the system interface are:

- Accepts external 12, 16.8, 19.2, 26, and 38.4 MHz reference square clocks at the crystal oscillator input (fref_xtal_in) or at the clock slicer input (fref_slicer_in)
- Accepts crystal working on fundamental frequency 12, 16.8, or 19.2 MHz connected between OMAP fref_xtal_in and fref_xtal_out pads
- An output (fref_xtal_clk) to deliver the oscillator cell (FREF_XTAL) generated system clock to a companion audio-manager IC.
- Accepts 12, 16.8, 19.2, 26, or 38.4 MHz reference sine wave clock on slicer input

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- A 32-kHz CMOS clock input
- Four configurable clock outputs
- Two clock request inputs
- A bidirectional clock request (OMAP device to external clock source and vice versa)
- SYS_BOOT[3:0] input signals to define the boot mode
- SYS_BOOT[5:4] input signals to select clock configuration
- Two reset sources
  - Power-on reset (cold reset)
  - Bidirectional warm reset
- Two external interrupt lines
- Two external DMA requests
- Outputs for voltage control

NOTE: A mapping dependency table is implemented in the OMAP device that enables any clock output to be delivered upon any clock request input; the multiplexing nevertheless allows two options, as follows:

- Three clock outputs (out0, 1, 2) versus two clock request inputs (req1, 2)
- Four clock outputs (out0, 1, 2, 3) versus one clock request input (req1)

NOTE: The options to supply an external sine-wave clock or a square-wave clock (in the slicer-bypassed mode) through the fref_slicer_in pad are valid only for the OMAP5430 device. For more information on the slicer input restrictions in the OMAP5432 device, see Section A.11.2, *Clock and Reset* in Appendix A, *OMAP5432 Multimedia Device*.

28.2.3.2 Clocking Scheme

28.2.3.2.1 Required System Input Clocks

The OMAP device operation requires external input clocks, as follows:

- 32k clock: A 32.768-kHz crystal is connected to the PMIC companion chip that embeds the 32k-oscillator (a square CMOS clock can also be delivered on the 32k_xtalin pin of Power-management IC, if the 32k-crystal is connected on another device of the system). The resulting 32k-clock is delivered to the entire system on three outputs:
  - CLK32KAO is always on (meaning that when PMIC chip VIO pin is on; that is, it is in WAIT-ON or ACTIVE state). It is used to deliver a 32k clock to always-on domain of the OMAP device and, for example, a modem.
  - CLK32K1 is software-controlled and is delivered to the audio-management IC companion chip. (not shown in Figure 28-3) when requested by the OMAP device (this input is on by default at system boot).
  - CLK32K2 gated clock is software-controlled and is delivered when requested by the OMAP device (this input is on by default at system boot).
- The OMAP chip delivers digital clocks to other peripherals. The OMAP device supports different types of input clock sources at several frequencies:
  - Crystal source. An internal oscillator embedded in the OMAP device is used. The fref_clk_ioreq is then set as an input to be used by an external device to request the OMAP device to deliver the clock on fref_clk0_out.
  - External oscillator type source. The OMAP internal oscillator is disabled. In case of external oscillator, the fref_clk_ioreq is configured as output, to request the clock from the external source. There are two possibilities to apply an external clock, as follows:
    - The external source delivers a sine (slicer active) or square (slicer bypassed) single-ended clock on the fref_slicer_in pin.

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- An external square-wave-only clock is injected into the fref_xtal_in pad, with the fref_xtal_out pad remaining unconnected.

- Audio clock: The audio-management IC builds its own clock, either from the 32k clock or the high-speed (HS) clock (depending on the audio scenario). This internal clock is delivered to the device ABE subsystem (abe_clks input) for audio flow synchronization.
- The audio-management IC companion can receive a buffered oscillator HS clock, generated by the OMAP device crystal oscillator cell (in either osciallator-bypassed or oscillator-active modes) from the OMAP output pad (fref_xtal_clk).

Clock input modes are selected by the sysboot signals (sys_boot[5:4] pads) to let the system wake up in the proper mode, even after a cold boot (selection of the relevant input signal [fref_slicer_in or fref_xtal_in/out] and slicer/oscillator mode setting [on or bypass]).

The OMAP device provides the HS clock to other devices on three fref_clk[0:2]_out pads. An additional clock output signal (fref_clk3_out) is multiplexed (MuxMode=0x1) on the OMAP device pad fref_clk2_req. For more information on multiplexing, see Chapter 18, *Control Module*.

The audio-management IC receives a HS clock when the audio scenario requires it (some low-power audio player scenarios can be performed only with the 32k clock).

Table 28-2 lists the mapping for the OMAP clock input sources. Table 28-3 lists the PMIC clock requirements.

Table 28-2. Mapping for Input Sources

Input Source	Mapping	Frequency Range/List	Type
Internal oscillator	fref_xtal_in and fref_xtal_out	12, 16.8, or 19.2 MHz	Crystal connection pins
External HS clock	fref_slicer_in	12, 16.8, 19.2, 26, or 38.4 MHz	Sine or square single ended
External 32k clock	sys_32k	32.768 kHz (nom.)	Square
Audio-management IC companion	abe_clks	<19.2 MHz	Square

Table 28-3. PMIC Clock Requirements

Input Source	Mapping	Frequencies Range/List	Type
Internal oscillator	OSC32KIN and OSC32KOUT	32.768 kHz (nom.)	Crystal connection pins

CAUTION

Clock configurations depend on core voltage, and maximum clock frequencies may not apply to production. For more information, see the *Device Data Manual*.

28.2.3.2.2 Optional System Output Clocks

The OMAP device can output four alternate clocks, fref_clk[0:3]_out. Each output clock, 0 through 3, can be gated or enabled by the activation of any associated clock-request signal, fref_clk[1:2]_req or fref_clk_ioreq (when configured as an input clock request). The mapping of an input clock request versus clock output as well as request polarity is programmable in the *System Clock and Reset Manager* registers. For more information, see Section 3.3, *PRCM Subsystem Environment*, in Chapter 3, *Power, Reset, and Clock Management*.

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28.2.3.3 Reset Configuration

28.2.3.3.1 ON/OFF Interconnect and Power-On-Reset

The entire system is typically awakened by an ON/OFF push button connected to the PMIC chip. This signal belongs to the VSYS - system power domain and is active low (the PMIC internal pullup ties it to VSYS). The PMIC power-up event is propagated through its NRESPWRON output pin to the OMAP sys_nrespwron pad (that is, the OMAP device SYS_NRESPWRON input signal) when the PMIC power-up sequence is achieved. The reset pad sys_nrespwron (signal SYS_NRESPWRON) is used to reset all the chip at power-on reset (POR) when the chip core voltage and I/O voltage are correctly set (cold reset). The OMAP.SYS_NRESPWRON input pin is held low all the time during VDD core and I/O power-up. Because this signal is also provided to the audio-management IC companion, it resets its state-machine and gets some available functions even if the VDD-2V1 power supply is not provided.

28.2.3.3.2 Warm Reset

A warm reset can be asserted by the OMAP device, by an external button (typically for development platform), or by any other chip connected to it (normally tied to PMIC companion NRESWARM output pin).

The OMAP warm reset pad (sys_nreswarm - OMAP bidirectional signal SYS_NRESWARM) is used to trigger a warm reset on the OMAP device, which resets part of the device when it has already booted (for example, to recover from a software crash). The OMAP SYS_NRESWARM signal is a bidirectional reset. When an internal OMAP reset occurs, SYS_NRESWARM output goes low and resets all the peripherals. Because the SYS_NRESWARM output is open drain, an external pull up resistor is required.

The OMAP device releases the SYS_NRESWARM output signal after NRESPWRON is deasserted.

28.2.3.3.3 Peripheral Reset by GPIO

Most peripherals are reset and powered on or off by GPIO. By default, under POR, most OMAP device signals are in safe mode with a default value driven by the I/O cell. The value is driven by an internal pullup or pulldown. Depending on the peripheral reset active level, users must select one GPIO or another (according to the reset value).

Once POR is released, the value on the pad is driven by the default configuration of the device control module. Most of time, this configuration is aligned with the default value selected on the I/O cell.

The next step is application-dependent: Users must configure the device registers to validate GPIO use and the default configuration of the control module.

28.2.3.3.4 Warm Reset Impact on GPIOs

When a warm reset event occurs:

- The GPIO controller is reset. Consequently, the GPIO is automatically turned in input mode.
- The control module is not reset. Information related to signal multiplexing mode and pullup or pulldown configuration is still valid.

Therefore, when a warm reset event occurs, the output buffer is disabled. Consequently, two different behaviors can be defined with regard to what is expected by the platform:

- GPIO sensitive to warm reset:

  To prevent a floating pad, user software is designed to have the internal pad PU and PD resistors enabled immediately, before the software warm reset action, because the warm reset-sensitive GPIO controllers will change I/O direction to input after an OMAP warm reset. This is necessary if the warm reset-sensitive GPIO controller pin has been configured for output before the warm reset occurrence. The pulls-enabled-before-warm-reset condition should be set by default in case the user has configured a GPIO as an input, because in this case the user is expected to have enabled the internal PU and PD pads during GPIO configuration (unless external pull resistors were used).

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NOTE: If the PU and PD resistors are enabled immediately by software after a POR (cold reset) for a GPIO that is planned to be used only as an output, then unnecessary consumption can occur.

While the dynamically-enable-the-pull-just-before-warm-reset condition is possible during a software warm reset (because the user software is aware of the exact moment a warm reset event occurs), it is not possible when the warm reset is triggered by hardware (for example, a watchdog reset, SYS_NRESWARM signal assertion, and so forth), because the software is not aware of the exact moment of these warm reset assertions.

- GPIO not sensitive to warm reset:

  To avoid getting a floating signal during (and after) a warm reset event and to keep the same value that was driven before the reset, users must align the pull value with the drive value each time a dedicated GPIO register is accessed.

NOTE: To avoid unnecessary consumption, the user software must ensure that internal pull resistor is disabled when the GPIO buffer is driving.

For the description of the reset sequences, see Section 3.5, *Reset Management Functional Description*, in Chapter 3, *Power, Reset and Clock Management*.

NOTE:

- For more information about the OMAP device reset management, see Section 3.5, *Reset Management Functional Description* in Chapter 3, *Power, Reset, and Clock Management*.
- To determine the cause of the last reset, see Section 3.5, *Reset Management Functional Description* in Chapter 3, *Power, Reset, and Clock Management*.

28.2.3.4 Power and Audio-management IC Companions Control

- I^2C:

  The OMAP device interfaces: system interface (sys_x) I/Os, SR_PMIC, I2C1_PMIC are involved in system interractions between the OMAP and external power, reset and clock management IC companions.

  The OMAP and PMIC companion implement the basic power-management interface (SYS), as follows:

  – 32-kHz clock single input
  – Two system resets: power-on (cold) reset and warm reset
  – One power request
  – One interrupt

  The OMAP device and PMIC companion implement:

  – A dedicated (I2C1_PMIC) HS interface for control and configuration
  – A SmartReflex (SR_PMIC) interface for dynamic core voltages setting

  The device and battery charger IC companion chip implement a communication channel for battery charging control and configuration over the platform companion ICs control interface (I2C1_PMIC).

  The OMAP and audio-managment IC companion implement a communication channel for audio control and configuration over the platform companion ICs control interface (I2C1_PMIC).

  Internal pullup resistors are provided on the OMAP I2C1_PMIC interface pads. For more information, see the device *Data Manual*. The I^2C links must first be started in fast-speed mode. Therefore, the buffer default pullup value must support this mode.

  Some of the PMIC chip power resources are controlled through the SmartReflex link (I^2C-like). This control allows the host to drive the dynamic voltage frequency scaling (DVFS) and adaptive voltage scaling (AVS) operations of these resources. As with its I^2C interfaces, some internal pullup resistors are provided on the OMAP device SmartReflex I/Os. The link must be run at the highest speed allowed by the voltage controller of the OMAP device (lower than I^2C HS mode frequency).

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- INT:

  Both PMIC and audio-management IC companion devices can activate their output interrupt request signal (INT) at any time when they require the OMAP (host) device to monitor their activity. When receiving such an interruption, the OMAP checks, through the I^2C, to determine the source of the interrupt. These INT pins are active low.

28.2.3.5 PMIC Request Signals

The PMIC drives three external enable-output signals, which allows switching on some external resources at different stages of the power-up sequence:

- REGEN1 and REGEN2 are driven high at the beginning of the power-up sequence, before any internal power source is turned on. They belong to the VSYS power domain. REGEN1 can typically be used for buck boost control.
- SYSEN is driven high immediately after the VCORE power output is turned on. SYSEN allows switching on the additional power regulator to supply the MPU subsystem. SYSEN belongs to the VIO power domain.

The PMIC companion chip can receive three power resource requests: ENABLE[1, 2, 3] (only ENABLE2 is used). These pins allow an external device to request PMIC internal resources. The PMIC companion power behavior when pins are activated must be programmed after the first boot. Typically, ENABLE2 is allocated for a modem group.

28.2.4 Boot Configuration

The OMAP device implements six sampled-on-reset sys_boot pads.

Four external pads (sys_boot[3:0]) are used to select interfaces or devices for the booting list, as follows:

- sys_boot3 selects the peripheral (sys_boot3 = 0b0) or memory booting (sys_boot3 = 0b1) scheme.
- sys_boot[2:0] select the boot mode.

The sys_boot[5:4] pads select the OMAP clock source configuration.

All six pins are sampled and latched onto the CTRL_MODULE_CORE.CONTROL_STATUS[5:0] SYS_BOOT bit field after POR. After booting, these pads can be used for other functions such as GPIOs, and the associated register bit field is not updated by the new functionality. For more information about pad multiplexing configuration, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*.

NOTE: If used as GPIOs, the sys_boot[5:0] pads must be used only in output mode to ensure that the input values always match a certain hardware predefined boot pattern, interpreted after each POR.

28.2.4.1 System Clock Source Selection

Figure 28-5 is an overview of the system clock selection. Table 28-4 summarizes the selection.

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Figure 28-5. System Clock Selection Diagram

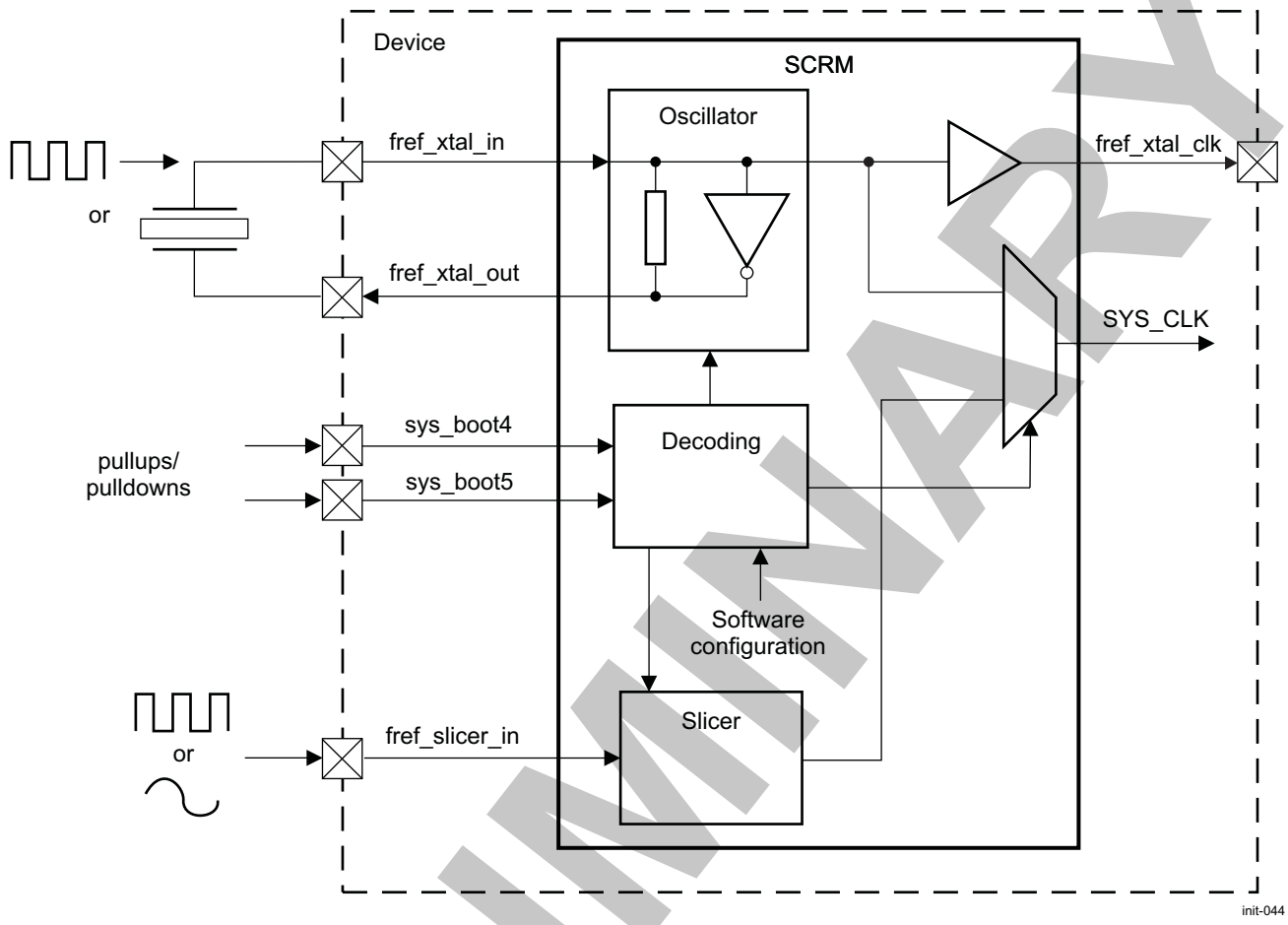

Table 28-4. System Clock Selection Summary

sys_boot[5:4]	SYS_CLK Source	Oscillator Mode	Slicer Mode	fref_clk_ioreq Mode
0b00	fref_xtal_in	Active	Power-down	Input
0b01[(1)]	fref_xtal_in	Bypass	Power-down	Output
0b10	fref_slicer_in	Power-down	Active	Output
0b11	fref_slicer_in	Power-down	Bypass	Output

(1) In the oscillator bypass case, the fref_xtal_out pin is left unconnected.

The OMAP device clock source settings description:

- sys_boot[5:4] = 0b00:
  - The system clock source is the on-chip oscillator tied between the fref_xtal_in and fref_xtal_out pads.
  - The slicer is powered down.
  - The fref_clk_ioreq signal is a clock request input by default In this mode.
- sys_boot[5:4] = 0b01:
  - The system clock source is external. The internal oscillator is bypassed to inject a square-wave system clock.
  - The slicer is powered down.
  - In this mode, the fref_clk_ioreq signal is an output that requests the clock from the external clock supplier.
- sys_boot[5:4] = 0b10:

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  - The system clock source is the on-chip slicer, supplied with a sine-wave clock from the external oscillator. The internal crystal oscillator cell is powered down.
  - The slicer is active.
  - The fref_clk_ioreq signal is an output that requests the clock from the external clock supplier.
- sys_boot[5:4] = 0b11:
  - The system clock source is external, bypassing the slicer to inject a square-wave system clock.
  - The internal oscillator is powered down.
  - The fref_clk_ioreq signal is an output that requests the clock from the external clock supplier.

NOTE: The options to supply an external sine-wave clock or a square-wave clock (in the slicer-bypassed mode) through the fref_slicer_in pad are valid only for the OMAP5430 device. For more information on the slicer input restrictions in the OMAP5432 device, see Section A.11.2, *Clock and Reset*, in Appendix A, *OMAP5432 Multimedia Device*.

28.2.4.2 Booting Device Order Selection

The ROM code creates the device list (order) based on information gathered from two locations:

- The first location is the sys_boot[3:0] external configuration pins sensed in the OMAP device CTRL_MODULE_CORE.CONTROL_STATUS register. The sys_boot[3:0] configuration pads have two main purposes: configure ROM code software in terms of interfaces and devices used for booting and configuring hardware after a POR or cold reset.
- The second location is the software booting configuration stored in the nonvolatile SAR memory, and used after a global warm reset.
- The third location is an on-board EEPROM (connected through I2C1) whenever sys_boot[3:0] value indicates this mode.

The SYSBOOT pins are used to index a booting device list from a table with possible booting scenarios. The order of examined booting devices is from the first to the third devices.

The following names are used in the tables:

- Memory types:
  - Execute in place (XIP): XIP memory without wait-signal monitoring enabled (NOR flash memory or other XIP device)
  - XIP wait: XIP memory with wait-signal monitoring
  - NAND: NAND flash memories (non-XIP)
  - OneNAND™: OneNAND and Flex-OneNAND™ flash memories
  - SD: SD card device on the device SDCARD I/O port (associated with the MMC1 controller instance.)
  - eMMC: eMMC™ memory device on the OMAP device eMMC I/O port (associated with the MMC2 controller instance). See Section 28.2.4.3, *Boot Peripheral Pin Multiplexing*.
  - SATA interface compatible storage devices such as solid state drives (SSDs) or hard-disk drives (HDDs). See Section 28.2.4.3, *Boot Peripheral Pin Multiplexing*.
- Peripheral interfaces:
  - USB: USB - HS and SS interface over the OMAP device USBD0 port
  - Universal asynchronous receiver/transmitter (UART): UART3 interface
- Table 28-5 lists the permanent booting devices in bold typeface.

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NOTE: If no valid software booting configuration is found in case of a warm reset, the ROM code builds a device list featuring only the permanent booting devices (in bold) defined by one of the following conditions:

- The sys_boot[3:0] configuration latched into the CTRL_MODULE_CORE.CONTROL_STATUS[3:0] SYSBOOT bit field upon POR
- Data stored in the I2C1 connected on-board EEPROM (the EEPROM itself selected in a sys_boot[3:0] value)

Hence, peripheral booting devices are skipped when the OMAP restarts from warm resets and no software booting configuration is invoked.

NOTE: Users can force the execution of the peripheral booting procedure after warm reset by using the software booting configuration feature.

Table 28-5 lists the booting device order when it is preferred to boot from a memory type device. This table is selected by ROM code when the sys_boot3 pin is tied high (= 1) after reset and before booting completes. If fast XIP booting is selected, the sys_boot3 pin controls the XIP wait-signal monitoring (that is, a logical high level enables wait-signal monitoring).

Table 28-5. Memory Preferred Booting

sys_boot[3:0]	Booting Devices Order		
	First	**Second**	**Third**
0b1000	**eMMC**	USB	N/A
0b1001	**NAND**	USB	N/A
0b1010	**SD**	**eMMC**	USB
0b1011	**SATA**	**SD**	USB
0b1100	**XIP**	USB	UART
0b1101	**OneNAND**	UART	N/A
0b1110	**eMMC** (boot partition only)	N/A	N/A
0b1111	**Fast XIP booting. Wait monitoring ON**	UART	USB

NOTE: When sys_boot[3:0] is tied to 1110, the ROM code boots from eMMC boot partition. If the ROM code fails to retrieve the booting image, it does not try boot from the user area contrary to other eMMC options in the table. This option does not provide the peripheral booting support (for example, USB).

Table 28-6 lists the booting device order when it is preferred to boot from a peripheral-type device. This table is selected by ROM code when the sys_boot3 pin is tied low (= 0). If fast XIP booting is selected, the sys_boot3 pin controls the XIP wait-signal monitoring (that is, a logical low level disables wait-signal monitoring).

Table 28-6. Peripheral Preferred Booting

sys_boot[3:0]	Booting Devices Order		
	First	**Second**	**Third**
0b0000	USB	**eMMC**	N/A
0b0001	USB	**NAND**	N/A
0b0010	USB	**SD**	**eMMC**
0b0011	USB	**SATA**	**SD**
0b0100	USB	UART	**XIP**
0b0101	UART	**OneNAND**	N/A
0b0110	**I2C1**(1)	N/A	N/A

(1) The booting device list is retrieved from an on-board EEPROM connected to the OMAP device through I2C1.

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Table 28-6. Peripheral Preferred Booting (continued)

sys_boot[3:0]	Booting Devices Order		
	First	Second	Third
0b0111	**Fast XIP booting. Wait monitoring OFF**	UART	USB

28.2.4.3 Boot Peripheral Pin Multiplexing

Table 28-7 lists the code pin multiplexing configuration supported by ROM according to boot peripheral.

Table 28-7. Pin Multiplexing According to Boot Peripheral

Boot Device	Boot Interface	Pads	Comments
eMMC	eMMC/JC64 memory component connected to the eMMC port	Only one device connected at the eMMC pads, on which MMC2 controller I/Os are muxed when MuxMode=0x0 (default)	Clock frequency: identification mode: 400 kHz. Booting from user area: Data transfer mode: 10 MHz (optionally up to 48 MHz with configuration header [CH]). Initial 1-bit single data rate (SDR) mode. Can optionally be extended to 4-bit and 8-bit SDR, as well as 4-bit and 8-bit double data rate (DDR) modes if a CH is used. Booting from boot partitions (Alternative Boot operation mode) is supported only at 8-bit/48 MHz/DDR. eMMC device powered by the companion chip or external supply. Supports 1.8-V I/O interface. Support for low- and high-capacity memory components.
SD	SD removable card connected to the SDCARD port	Only one device connected at the SD card pads, on which MMC1 controller I/Os are multiplexed when MuxMode=0x0 (default).	Clock frequency: identification mode: 400 kHz; Data transfer mode 10 MHz (optionally up to 19.2MHz) 3 V VCC power supply. Initial 1-bit mode, optional up to 4-bit mode. Support for low- and high-capacity memory components
NAND	Raw NAND flash	GPMC i/f signals, available when MuxMode=0x4 on different OMAP interface (UART1, UART2, and HSI2) pads .	8/16 bit IO width Support for Single-level and Multi-level cell NAND Flash from 512Mb to 64Gibit Supports identification through ONFI Connected to GPMC interface Chip Select 0 (gpmc_ncs0)
OneNAND	OneNAND / FlexOneNAND flash memory		NAND flash with integrated controller and NOR like bus Connected to GPMC interface Chip Select 0.
XIP	NOR flash		NOR (CFI) or other XIP device, connected to GPMC interface Chip Select 0.
SATA	SSD, HDD	SATA i/f pads (no MuxMode)	Serial ATA device (hard drive or flash device integrating a SATA controller e.g SSD) connected to the SATA interface.

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Table 28-7. Pin Multiplexing According to Boot Peripheral (continued)

Boot Device	Boot Interface	Pads	Comments
USB	USB OTG SS/HS	USBD0 i/f pads, as follows: • MuxMode=0x0 - USBD0_HS pads • USBD0_SS pads (no MuxMode)	USB OTG Super Speed (USB_OTG_SS) controller through the OMAP embedded Super Speed (USB3_PHY) and High Speed (USB_PHY_CORE) PHY transceivers, hence only UTMI port is utilized. **ROM Code does NOT support booting through external for the OMAP device USB PHY transceivers connected on the device USB ULPI port.** No support for OTG features.
UART	UART3 port serial interface	UART3 RX and TX signals available on UART3 pads (MuxMode=0x0)	No flow control is required

NOTE: The general-purpose memory controller (GPMC) chip-select pads gpmc_ncs[1:4] have selected pull-downs at device level after reset. Because ROM code alters only the gpmc_ncs[0] configuration, it is not possible to accomplish the GPMC boot on CS0, if user has connected other GPMC devices on CS1, CS2, CS3, or CS4. That is, more than one chip-select signals would be activated at the time of GPMC boot. Booting devices that take advantage of GPMC are XIP, fast XIP, NAND, and OneNAND.

NOTE: The ROM code examines the interfaces that are selected to be searched until a valid bootable interface or device is found. The activities on the pads of the searched interfaces must be considered if they are connected to any other peripherals for any other purposes (for example, an LED connected to a GPMC pad muxed internally to a GPIO).

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28.3 Device Initialization by ROM Code

This section describes high-level booting concepts and provides basic knowledge for booting on the OMAP device.

28.3.1 Booting Overview

28.3.1.1 Booting Types

Booting is the process of starting a bootstrap from one of the booting devices.

The ROM code has two functions for booting: Peripheral booting and memory booting.

- In peripheral booting, the ROM code polls a selected communication interface such as UART or USB, downloads the executable code over the interface, and executes it in internal RAM. Downloaded software from an external host can be used to program flash memories connected to the OMAP. This special case of peripheral booting is called preflashing; software downloaded for preflashing is called the flash loader. The flash loader burns a new client application image in external flash memory. Initial software is a generic term for bootstrap, downloaded software, and flash loader. Asoftware (warm) reset can be performed after the image is burned.
- In memory booting, the ROM code finds the bootstrap in permanent memories such as flash memory, memory cards, or SATA SSD or HDD memory devices and executes it. This process is normally performed after a cold or warm OMAP reset.

The ROM code detects whether the OMAP device should download software from a peripheral interface (USB or UART) by using the sys_boot[3:0] pad configuration. This mechanism encompasses initial flashing in production (external memory is empty) and reflashing in service (external memory is already programmed).

28.3.1.2 ROM Code Architecture

Figure 28-6 shows the ROM code architecture. It is split into three main layers with a top-down approach: high-level, drivers, and hardware abstraction layer (HAL). One layer communicates with a lower-level layer through a unified interface.

- The high-level layer performs the main tasks of the public ROM code: multicore startup, watchdog and clock configurations, interrupt management, and main booting routine.
- The driver layer implements the logical and communication protocols for any booting device in accordance with the interface specification.
- The HAL implements the lowest level code for interacting with the hardware infrastructure IPs. End booting devices (typically external flash components) are attached to the device I/O pads.

Figure 28-6 shows the three layers with their modules.

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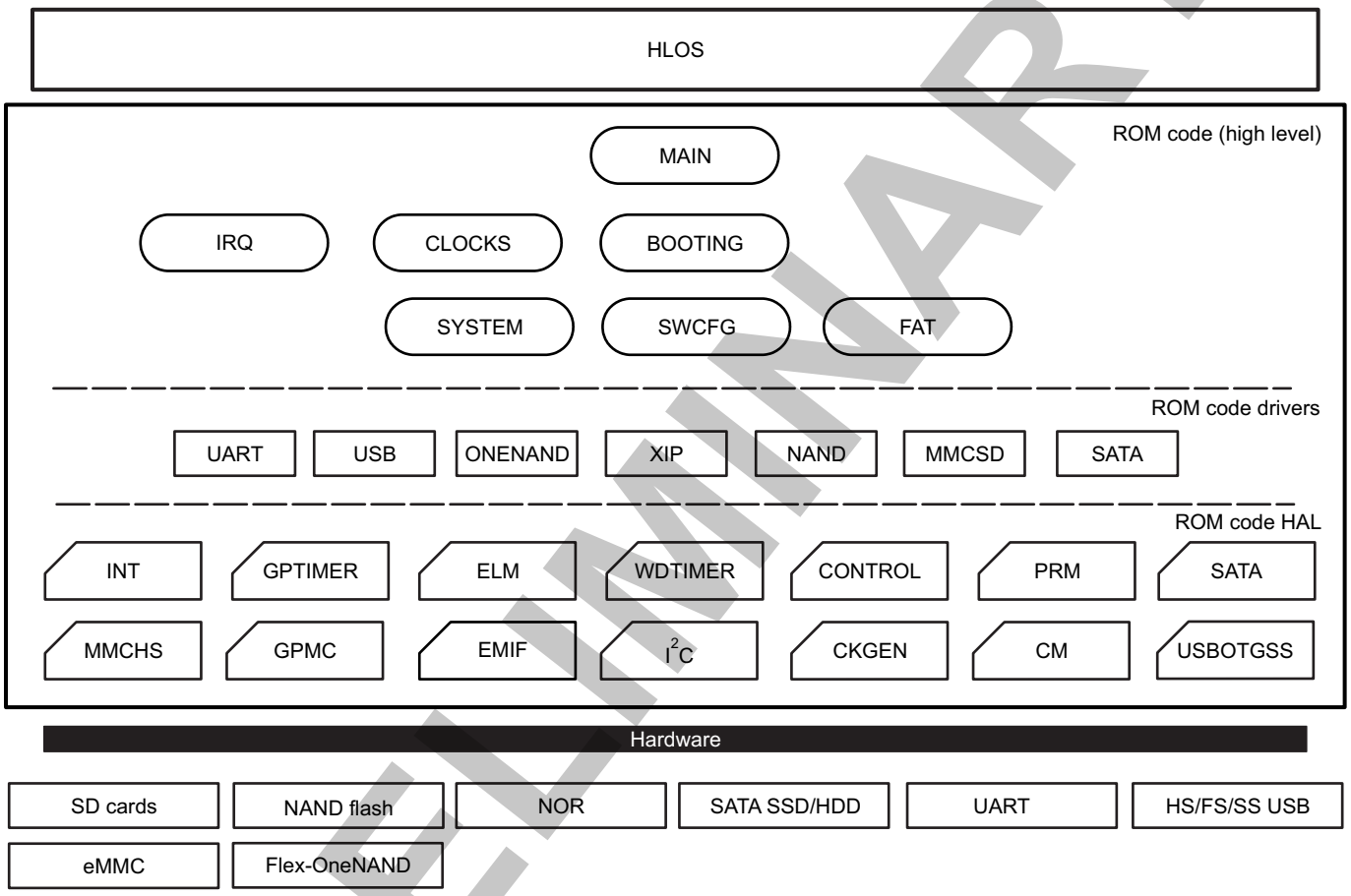
Figure 28-6. ROM Code Architecture



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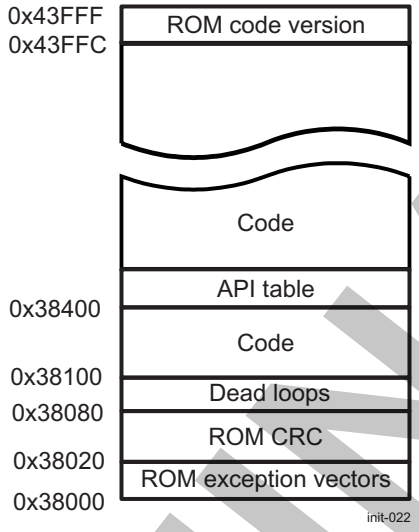
28.3.2 Memory Maps

28.3.2.1 ROM Memory Map

Figure 28-7 shows the 48-KiB ROM memory map.

Figure 28-7. ROM Memory Map



- ROM exception vectors

  Exceptions are redirected to ROM exception vectors (see Table 28-8). The reset exception is redirected to the public ROM code startup. Other exceptions are redirected to RAM handlers by loading appropriate addresses to the PC register.

Table 28-8. ROM Exception Vectors

Address	Exception	Content
0x38000	Reset	Branch to the ROM code startup
0x38004	Undefined	PC = 0x4031 F004
0x38008	Software interrupt (SWI)	PC = 0x4031 F008
0x3800C	Prefetch abort	PC = 0x4031 F00C
0x38010	Data abort	PC = 0x4031 F010
0x38014	Unused	PC = 0x4031 F014
0x38018	IRQ	PC = 0x4031 F018
0x3801C	FIQ	PC = 0x4031 F01C

- ROM code cyclic redundancy check (CRC)

  The ROM code CRC is calculated as 32-bit CRC code (CRC-32-IEEE 802.3) for the address range 0x38000–0x43FFF. The 4-byte CRC code is stored at location 0x38020.

- Dead loops

  Dead loops are branch instructions coded in ARM mode. They have multiple purposes (see Table 28-9).

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Table 28-9. Dead Loops

Address	Purpose
0x38080	Undefined exception default handler
0x38084	SWI exception default handler
0x38088	Prefetch abort exception default handler
0x3808C	Data abort exception default handler
0x38090	Unused exception default handler
0x38094	IRQ exception default handler
0x38098	FIQ exception default handler

- Code

  This space is used to hold code and constant data.
- API table

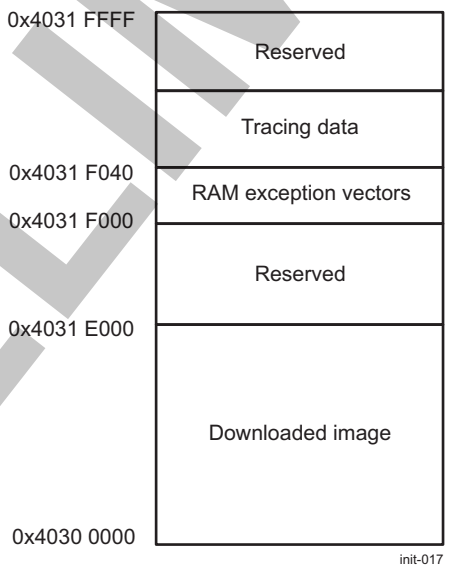
  The purpose of this table is to allow external code access to system maintenance, utility, and device driver functions which are used for ensuring the ROM code boot functionality. These functions can be reused at run time by calling a fixed address hardcoded in this table.
- ROM code version

  The ROM code version consists of two decimal numbers: major and minor. It can be used to identify the ROM code release version burned in a given IC. The ROM code version is a 32-bit hexadecimal value at address 0x43FFC.

28.3.2.2 RAM Memory Map

The partitioning of the on-chip SRAM (L3 OCM RAM) shown in Figure 28-8 is used during the booting process. Tracing areas can also be accessed when calling API functions.

Figure 28-8. RAM Memory Map



- Downloaded image

  This space is used by the public ROM code to store a downloaded booting image. It can be up to 120KiB.
- RAM exception vectors

  The RAM exception vectors provide an easy way to redirect exceptions to the custom handler. Table 28-10 lists the contents of the RAM space reserved for RAM vectors. The first eight addresses are ARM instructions that load the value in the subsequent eight addresses into the PC. These instructions are executed when an exception occurs because they are called from ROM exception vectors. Undefined, SWI, unused, and FIQ exceptions are redirected to a hardcoded dead loop.

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Prefetch abort, data abort, and IRQ exception are redirected to predefined ROM handlers. Users can redirect an exception to another handler by writing its address to the appropriate location from 0x4031 F024 to 0x4031 F03C, or by overriding the branch (load into PC) instruction between addresses from 0x4031 F004 to 0x4031 F01C.

Table 28-10. RAM Exception Vectors

Address	Exception	Content
0x4031 F000	Reserved	Reserved
0x4031 F004	Undefined	PC = [0x4031 F024]
0x4031 F008	SWI	PC = [0x4031 F028]
0x4031 F00C	Prefetch abort	PC = [0x4031 F02C]
0x4031 F010	Data abort	PC = [0x4031 F030]
0x4031 F014	Unused	PC = [0x4031 F034]
0x4031 F018	Interrupt request (IRQ)	PC = [0x4031 F038]
0x4031 F01C	Fast interrupt request (FIQ)	PC = [0x4031 F03C]
0x4031 F020	Reserved	0x38090
0x4031 F024	Undefined	0x38080
0x4031 F028	SWI	0x38084
0x4031 F02C	Prefetch abort	Address of default prefetch abort handler(1)
0x4031 F030	Data abort	Address of default data abort handler (1)
0x4031 F034	Unused	0x38090
0x4031 F038	IRQ	Address of default IRQ handler
0x4031 F03C	FIQ	0x38098

(1) The default handlers for prefetch and data abort perform reads from CP15 debug registers to retrieve the reason for the abort:
- In case of prefetch abort: the IFAR register is read from CP15 and stored into R0. The IFSR register is read and stored into the R1 register. Then the ROM code jumps to the prefetch abort dead loop (38088h).
- In case of data abort: the DFAR register is read from CP15 and stored into R0. The DFSR register is read and stored into the R1 register. Then the ROM code jumps to the data abort dead loop (3808Ch).

- Tracing data

  This area contains trace vectors reflecting the execution path of the ROM code. Table 28-11 describes the public ROM code tracing data. For more information about ROM code tracing, see Section 28.3.9, *Tracing*.

Table 28-11. Tracing Data

Address	Size (Bytes)	Description
0x4031 F040	4	Current tracing vector, word 1
0x4031 F044	4	Current tracing vector, word 2
0x4031 F048	4	Current tracing vector, word 3
0x4031 F04C	4	Current tracing vector, word 4
0x4031 F050	4	Cold reset run tracing vector, word 1
0x4031 F054	4	Cold reset run tracing vector, word 2
0x4031 F058	4	Cold reset run tracing vector, word 3
0x4031 F05C	4	Cold reset run tracing vector, word 4
0x4031 F060	4	Current copy of the PRM_RSTST register (reset reasons)

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28.3.3 Overall Booting Sequence

Figure 28-9 shows the ROM code flow chart.

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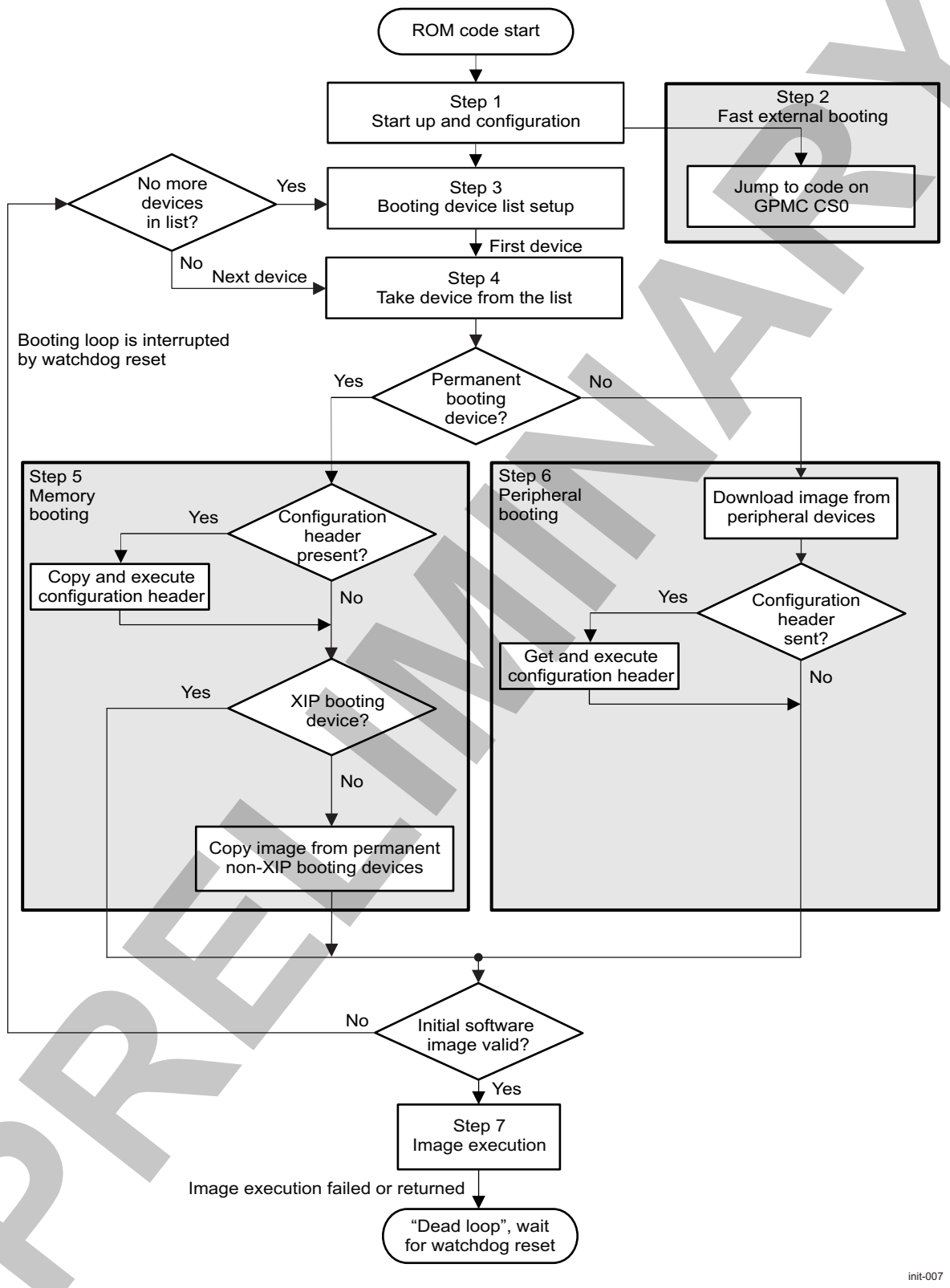
Figure 28-9. Overall Booting Sequence



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The main loop of the booting module goes through the booting device list and tries to get an image from the currently selected booting device. The ROM code performs the following steps:

Step 1. Basic configuration and initialization. Reading of SYSBOOT pins or software booting configuration.

Step 2. The path named fast external boot is a special low-latency boot mode. It consists of a blind jump to an external addressable memory. See Section 28.3.6, *Fast External Booting.*

Step 3. A booting device list is created (see Section 28.3.4.3, *Booting Device List Setup*). The list consists of all devices to be searched for a booting image. The list is created based on the sys_boot pins, the on-board EEPROM, or the software booting configuration described in Section 28.3.4.5, *Software Booting Configuration*. The software booting configuration structure is in the SAR memory and can be written by software before executing a software reset. After a software reset, the software booting configuration has priority over the sys_boot signals and EEPROM (also selected by sys_boot signals) configuration.

Step 4. The main loop of the booting procedure goes through the booting device list and tries to search for an image from the currently selected booting device. This loop is exited if a valid booting image is found and successfully executed or when the watchdog expires. If an image is found, ROM code executes memory booting or peripheral booting, depending on the type of the current booting device:

- Memory booting is executed when the booting device is XIP memory, NAND, OneNAND/Flex-OneNAND, eMMC or SD, SATA SSD/HDD.
- Peripheral booting is executed when the booting device is UART or USB.

Step 5. Memory booting reads data from memory-type devices. Memory booting is described in detail in Section 28.3.7, *Memory Booting*.

Step 6. Peripheral booting downloads data from communication interfaces. Peripheral booting is described in Section 28.3.5, *Peripheral Booting*.

Step 7. For the GP device, the image automatically starts.

An additional feature of the booting module is the execution of the Configuration Header (CH). The CH configures the system for faster and more flexible booting from the selected permanent or peripheral booting device. The CH, which is optional, is described in *Section 28.3.8.2, Configuration Header*.

28.3.4 Startup and Configuration

28.3.4.1 Startup

Figure 28-10 shows the ROM code start-up sequence.

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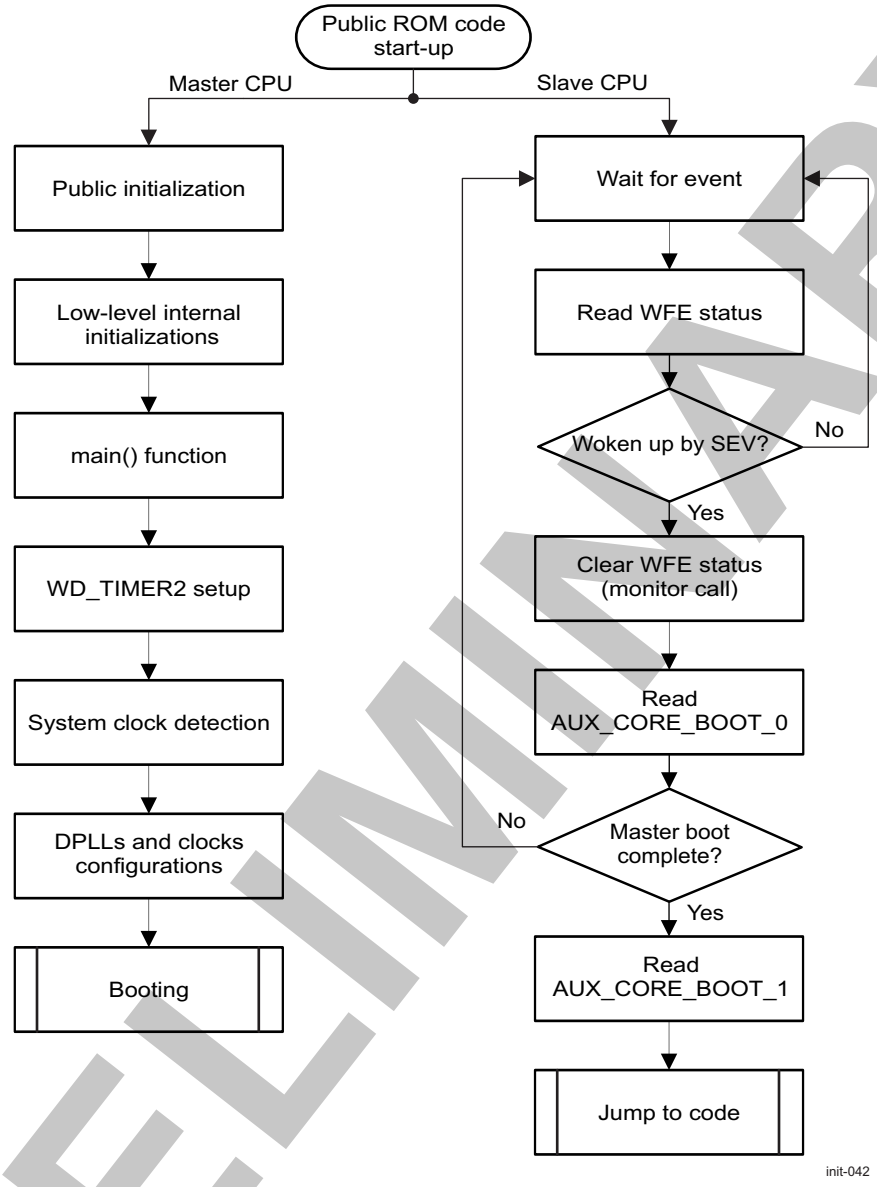
Figure 28-10. ROM Code Multiprocessor Start-Up Sequence



The master CPU L1 instruction cache and branch prediction mechanisms are activated as part of the public boot process. The base address of the public vector is configured to the reset vector of ROM code (0x38000). The memory management unit (MMU) remains switched off during boot (thus, L1 data cache is off). The master CPU performs the basic initialization of the public side. Next, the MMU configures WD_TIMER2 (set to 3 minutes), detects system clock, and configures the system clock. Finally, the MMU jumps to the booting routine.

No specific configuration is performed for the slave CPU, which keeps its default configuration after reset (L1 instruction and data caches off, branch prediction off, MMU off, no remap of the base address of the public vector). The slave CPU is rapidly held in wait-for-event (WFE) state. It stays in this state while the master CPU completes the public boot process and until jumping to the external software (for example, HLOS). At this stage, the external software can wake up the slave CPU by executing an SEV command.

Two internal memory-mapped registers are available to the OS for communicating start-up information. The AUX_CORE_BOOT_0 and AUX_CORE_BOOT_1 registers are in the MPU WakeupGen domain.

- AUX_CORE_BOOT_0 is used as a status register to signal the slave CPU that it must wake up after the send event operation initiated by the master CPU.

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- AUX_CORE_BOOT_1 contains the physical address location to which the slave CPU must jump after wakeup.

See the memory mapping of these registers in Chapter 4, *Dual Cortex-A15 MPU Subsystem*.

28.3.4.2 Clocking Configuration

The ROM code detects the system input clock frequency (gauging feature of TIMER1). The supported system frequencies in the OMAP device are:

- 12 MHz
- 16.8 MHz
- 19.2 MHz
- 26 MHz
- 38.4 MHz

After detecting the input clock, the ROM code configures the clocks and DPLLs required for ROM code execution.

The configured DPLLs are:

- DPLL_PER: locked to provide clocks to peripheral blocks
- DPLL_CORE: locked to provide L3_MAIN interconnect, L4 interconnect, and EMIF clocks
- DPLL_MPU: locked
- DPLL_USB_OTG_SS / DPLL_USB DPLLs: Locked only in case of USB peripheral booting. It is left untouched otherwise.
- DPLL_SATA: locked only in the case of the SATA memory booting. It is left untouched otherwise.

The DPLLs and PRCM clock dividers are configured with the default values of the ROM code (depending on the detected system input clock) after cold or warm reset in order to give the same working conditions to the ROM code sequence.

Table 28-12 summarizes the default ROM code clock settings.

Table 28-12. ROM Code Default Clock Settings

Clock	Frequency (MHz)	Source
DPLL_CORE clock with F_{DPLL} locked frequency	2128	DPLL_CORE.REF_CLK input
EMIF_PHY_GCLK[1]	44.33	DPLL_CORE (M2)
CORE_DPLL_SCRM_CLK	266	DPLL_CORE (M3)
CORE_DLL_GCLK	266	DPLL_CORE.HSDIVIDER (H11)
CORE_X2_CLK	266	DPLL_CORE.HSDIVIDER (H12)
CORE_CLK	266	CORE_X2_CLK
CORE_USB_OTG_SS_LFPS_TX_CLK	34.3	DPLL_CORE.HSDIVIDER (H13)
CORE_GPU_CLK	212.8	DPLL_CORE.HSDIVIDER (H14)
CORE_IPU_ISS_BOOST_CLK	212.8	DPLL_CORE.HSDIVIDER (H22)
CORE_ISS_MAIN_CLK	152	DPLL_CORE.HSDIVIDER (H23)
BB2D_GFCLK	177.3	DPLL_CORE.HSDIVIDER(H24)
L3_ICLK	133	CORE_CLK
L4_ICLK	66.5	L3_ICLK
MPU_DPLL_HS_CLK	266	CORE_X2_CLK
IVA_DPLL_HS_CLK	266	CORE_X2_CLK
DPLL_PER – clock with Fdpll locked frequency	768	DPLL_PER.REF_CLK input
FUNC_192M_CLK	192	DPLL_PER (M2)

(1) This clock is intentionally set up at low frequency to ensure correct initialization of external DRAM components.

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Table 28-12. ROM Code Default Clock Settings (continued)

Clock	Frequency (MHz)	Source
PER_DPLL_SCRM_CLK	192	DPLL_PER (M3)
FUNC_256M_CLK	256	DPLL_PER.HSDIVIDER (H11)
DSS_GFCLK	192	DPLL_PER.HSDIVIDER (H12)
PER_GPU_CLK	192	DPLL_PER.HSDIVIDER (H14)
DPLL_MPU - clock with Fdpll locked frequency	2200	DPLL_MPU.REF_CLK input (MPU_DPLL_CLK)
MPU_DPLL_CLK	550	PRM
MPU_GCLK	550	DPLL_MPU (M2)
DPLL_USB - clock with Fdpll locked frequency (2)	960	DPLL_USB. REF_CLK
L3INIT_480M_GFCLK	480	DPLL_USB (M2)
L3INIT_60M_GFCLK	60	L3INIT_480M_GFCLK
DPLL_USB_OTG_SS - clock with F_{DPLL} locked frequency (2)	2500	DPLL_USB_OTG_SS. REF_CLK
DPLL_SATA - clock with Fdpll locked frequency (3)	1500	DPLL_SATA. REF_CLK

(2) This clock is locked specifically if USB peripheral or SATA memory booting is selected.
(3) This clock is locked specifically if USB peripheral or SATA memory booting is selected.

However it is possible to override the default clock settings. There are three ways to change DPLLs and all related clock divider, gating, and multiplexer configurations during the boot:

- ROM code default settings, described in Table 28-12. They are always applied at any reset.
- Software booting configuration after a software reset, described in Section 28.3.4.5, *Software Booting Configuration*
- The CH, described in Section 28.3.8.2, *Configuration Header*. The CH lets users have a known configuration (about GPMC and clock registers) after memory or peripheral booting. This configuration can be blocked by the software booting configuration. For more information, see Table 28-14, *Software Booting Configuration Strcuture*.

28.3.4.3 Booting Device List Setup

The ROM code creates a device list based on two sources:

- The software booting configuration (if present after a warm reset). The software booting configuration structure is stored in nonvolatile RAM SAR memory.
- The sys_boot[3:0] signals latched in the control module are used to index the device table from which the list of devices is extracted.
- One of the values of the sys_boot pins defines the device list that is extracted from an on-board EEPROM (if available).

Figure 28-11 shows how the ROM code sets up the device list depending on the reset source.

NOTE: Only permanent booting devices are put on the list when reset is not power on and devices are taken from the sys_boot pins or on-board EEPROM. Users can force peripheral booting after software reset using the software booting configuration.

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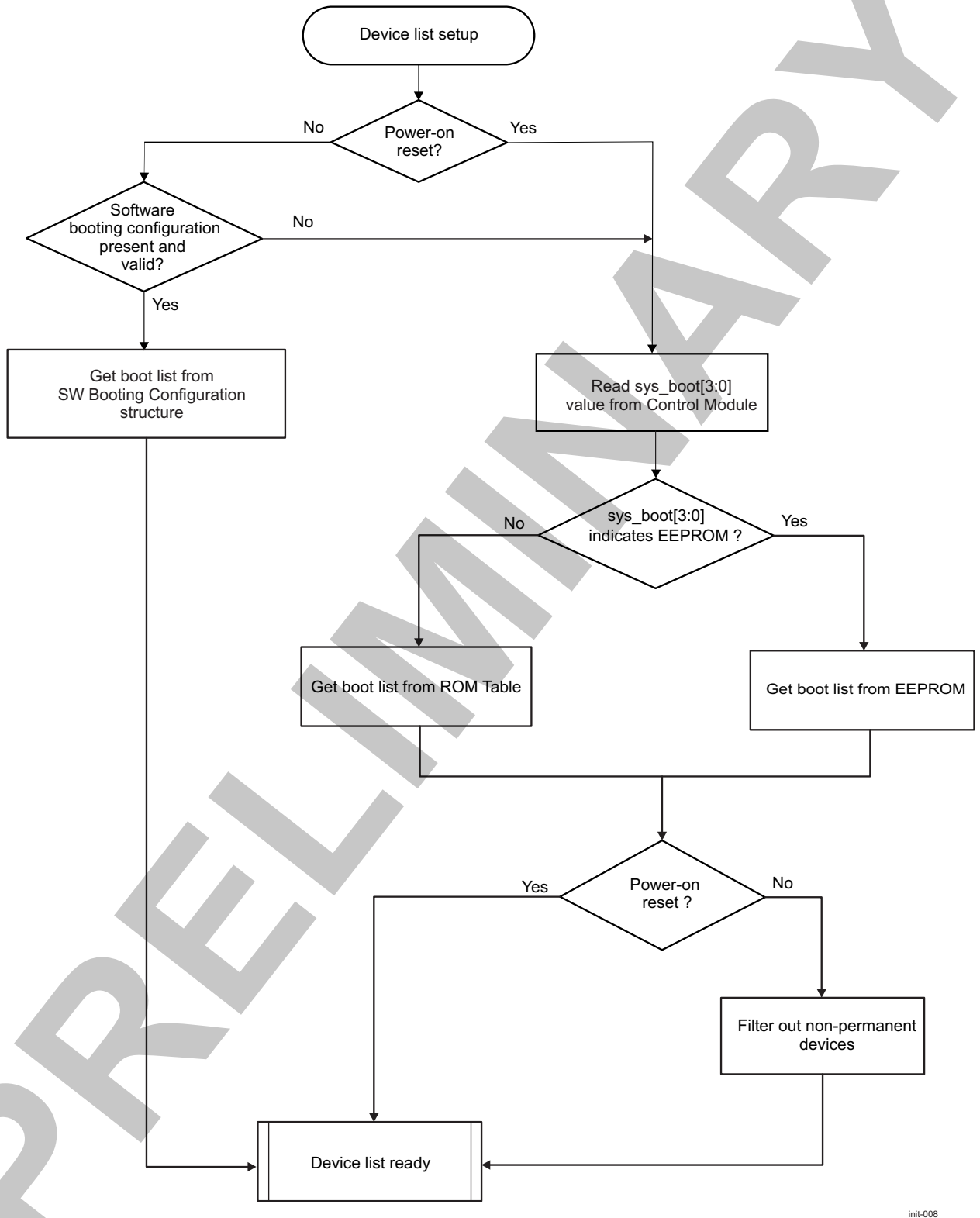
Figure 28-11. Device List Setup



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28.3.4.4 Boot Device List Retrieved from EEPROM

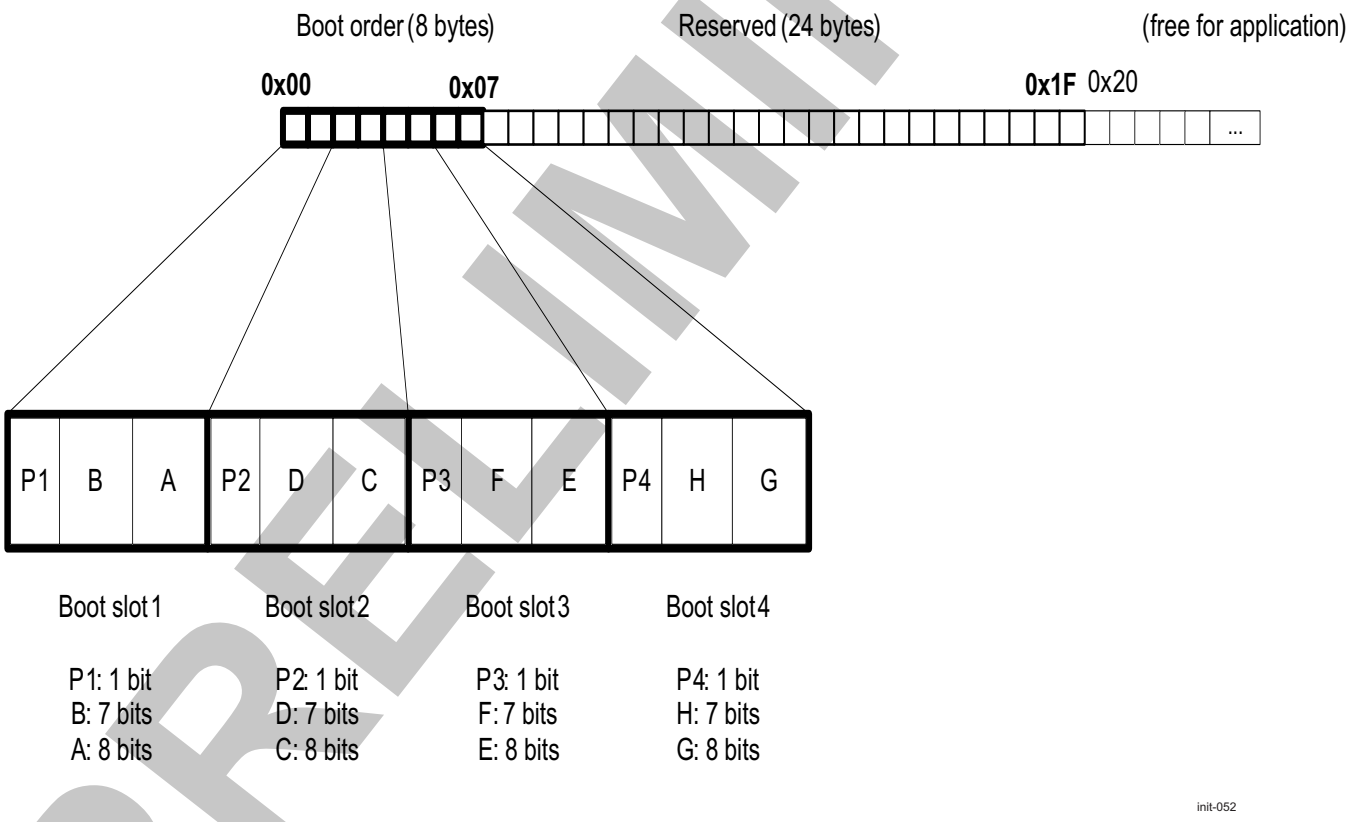
It is possible for the ROM code to retrieve the boot device list from on-board EEPROM connected to I2C1. The end user can reconfigure the boot-device order to match the expectation of the ROM code if the various options proposed in Table 28-5 and Table 28-6 do not fit the application.

NOTE: The I^2C option listed in Table 28-6 is not a boot option, because it is not intended to retrieve a booting image from the EEPROM. This option is defined for the purpose of retrieving the boot device order.

When sys_boot[3:0] pins indicates the I^2C boot option (value 0110 as defined in Table 28-6), then the ROM code initializes the I2C1 interface and reads eight consecutive bytes from address zero of the non-volatile EEPROM. The component is assumed to be wired at I^2C address 0x50. This address is hardcoded and cannot be changed, so the system must comprehend this non-flexible aspect. Even though the ROM code only makes use of the first eight bytes, it is recommended to leave the first 24 remaining bytes reserved for future evolution.

As shown in Figure 28-12, it is possible to configure a maximum of four boot slots, which can hold two boot devices each. Each boot slot has a permanent bit (P1 to P4). The boot slot is filtered out if the permanent bit is not set and a global warm reset occurs. If the bit is set, the boot slot is considered in any case of cold or warm boot.

Figure 28-12. EEPROM Non-Volatile Memory Layout



The device IDs to be populated in boot slots A, B, C, D, E, F, G, and H are defined as follows:

- 01h – XIP
- 02h – XIP (with wait monitoring)
- 03h – NAND
- 04h – OneNAND
- 05h – SD card
- 06h – eMMC (boot partition)

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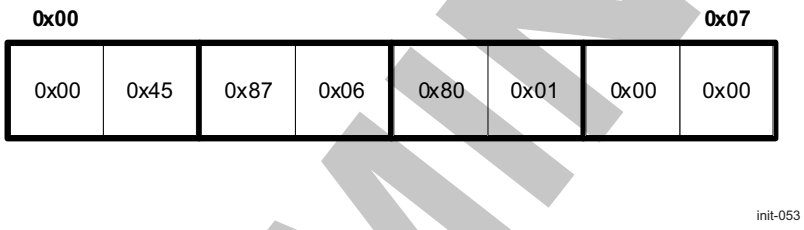
- 07h – eMMC
- 09h – SATA
- 43h – UART3
- 45h – USB
- Other values – Reserved

As an example, consider the following boot device order: USB → eMMC → XIP. This boot option does not exist in the SYSBOOT memory and peripheral booting table, so the I^2C option can be used. The following 8 bytes sequence would be stored:

- Boot slot 1: A=0x45 (USB), B=0x00 (No device, P1=0)
- Boot slot 2: C=0x06 (eMMC boot partition), D=0x87 (eMMC user area, P2=1)
- Boot slot 3: E=0x01 (XIP), F=0x80 (P3=1)
- Boot slot 4: G=0x0 (no device), H=0x00 (no device, P4=0)

Figure 28-13 shows the byte ordering. The system would boot with this boot device order after having configured the sys_boot[3:0] value to 0110 (see Table 28-6). In this example, eMMC and XIP are exercised on any reset (P2=P3=1), while the USB is skipped on a warm reset (P1=0).

Figure 28-13. Example of EEPROM Configuration for USB → eMMC → XIP



28.3.4.5 Software Booting Configuration

The software booting configuration is a logical structure stored in SAR RAM memory, which is not cleared after warm resets or wakeups from low-power modes.

28.3.4.5.1 Public Use of SAR RAM

At system level, the OMAP device SAR RAM memory is divided into four banks. The public ROM code uses only the first bank, which is always public-accessible.

The public ROM code offers some flexibility about the location of the software booting configuration structure. The PUBLIC_SW_BOOT_CFG_ADDR pointer defines the start address of the structure within the SAR RAM bank (see Table 28-13).

Table 28-13. Public Use of SAR RAM

Logical name	Address	Size (Bytes)	Description
PUBLIC_SW_BOOT_CFG_ADDR	0x4AE2 6DFC	4	Public software booting configuration pointer. The word value at this location is: - Reset (zero) on a cold reset. - Read on a warm reset.
PUBLIC_SAR_RAM_1_FREE	0x4AE2 6FC4	...	Recommended address for start of software booting configuration structure described in Section 28.3.4.5.2, *Software Booting Configuration Structure*.
PUBLIC_SAR_RAM_2_BASE	0x4AE2 7000	...	Start of SAR RAM bank 2

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As mentioned previously, the software booting configuration feature is optional. Hence, the public ROM code decides to use the feature based on the value read on a warm reset at the address pointed to by the PUBLIC_SW_BOOT_CFG_ADDR pointer. If the value matches the range 0x4AE2 6FC8 to 0x4AE2 6FFC, the ROM code extracts the structure at that address. The value pointed to by PUBLIC_SW_BOOT_CFG_ADDR is always overwritten to 0 on a cold reset.

It is possible to use the public SAR RAM area for any other purpose, such as storing traces for HLOS use. Obviously, care must be taken not to overwrite the locations used for low-power modes and/or software booting configuration, if used.

28.3.4.5.2 Configuration Structure for Software Booting

Table 28-14 describes the configuration structure for software booting . It offers three levels of flexibility for redefining the ROM code defaults after a warm reset:

- Redefining the default device booting list (from ROM code defaults given by SYSBOOT pins configuration)
- Redefining the default clock settings
- Redefining time-out linked to the peripheral booting mechanism

NOTE: The sections are provided as a linked list; therefore, the order and number of items is not relevant.

The ROM code searches for the next section at the location based on the size filled in the previous section. The clock configuration from software booting configuration may override the CH settings, if the appropriate bit is set in the configuration structure for software booting.

Table 28-14. Software Booting Configuration Structure

Field	Size (Bytes)	Description
Booting Configuration		
Section 1 key	4	Synchronization key for section 1: 0xCF00 AA01
Section 1 size	4	Size of section 1: 0x0000 000C (12)
Flags	2	Bits [4:1]: Mask the CH; when a bit is set to 1, a CH item is not analyzed: [1]: SETTINGS [2]: RAM [3]: FLASH (GPMC) [4]: MMCSD
First device	2	Devices to be put into the device list: 0x01: XIP 0x02 XIP (with wait monitoring) 0x03: NAND 0x04: OneNAND 0x05: SD card 0x06: eMMC (boot partition, BP1 or BP2) 0x07: eMMC 0x09: SATA 0x43: UART3 0x45: USB internal transceiver only 0x46: Other values: Reserved
Second device	2	
Third device	2	
Padding	2	Reserved
Clock Settings		
Section 2 key	4	Synchronization key for section 2: 0xCF00 AA02
Section 2 size	4	Size of section 2: 0x0000 008C (140)

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Table 28-14. Software Booting Configuration Structure (continued)

Field	Size (Bytes)	Description
Flags	4	Bit mask of various switches, active when set to 1: Bit [0]: Clock configuration defined in this structure is applied. Bit [1]: Reserved Bit [2]: Apply general clock settings. Bit [3]: Set and lock DPLL_PER. Bit [4]: Set and lock DPLL_MPU. Bit [5]: Set and lock DPLL_CORE. Bit [6]: Set and lock DPLL_USB (USB HS DPLL). Bit [7]: Bypass DPLL_PER before setting clocks. Bit [8]: Bypass DPLL_MPU before setting clocks. Bit [9]: Bypass DPLL_CORE before setting clocks. Bit [10]: Bypass DPLL_USB (USB HS DPLL) before setting clocks. Bits [31:11]: Reserved
General Clock Settings		
CM_CLKSEL_CORE	4	Register value
CM_BYPCLK_DPLL_MPU	4	Register value
CM_BYPCLK_DPLL_IVA	4	Register value
CM_MPU_MPU_CLKCTRL	4	Register value
CM_CLKSEL_USB_60MHZ	4	Register value
MPU DPLL Settings		
CM_CLKMODE_DPLL_MPU	4	Register value
CM_AUTOIDLE_DPLL_MPU	4	Register value
CM_CLKSEL_DPLL_MPU	4	Register value
CM_DIV_M2_DPLL_MPU	4	Register value
Core DPLL Settings		
CM_CLKMODE_DPLL_CORE	4	Register value
CM_AUTOIDLE_DPLL_CORE	4	Register value
CM_CLKSEL_DPLL_CORE	4	Register value
CM_DIV_M2_DPLL_CORE	4	Register value
CM_DIV_M3_DPLL_CORE	4	Register value
CM_DIV_H11_DPLL_CORE	4	Register value
CM_DIV_H12_DPLL_CORE	4	Register value
CM_DIV_H13_DPLL_CORE	4	Register value
CM_DIV_H14_DPLL_CORE	4	Register value
CM_DIV_H21_DPLL_CORE	4	Register value
CM_DIV_H22_DPLL_CORE	4	Register value
CM_DIV_H23_DPLL_CORE	4	Register value
CM_DIV_H24_DPLL_CORE	4	Register value
PER DPLL Settings		
CM_CLKMODE_DPLL_PER	4	Register value
CM_AUTOIDLE_DPLL_PER	4	Register value
CM_CLKSEL_DPLL_PER	4	Register value
CM_DIV_M2_DPLL_PER	4	Register value
CM_DIV_M3_DPLL_PER	4	Register value
CM_DIV_H11_DPLL_PER	4	Register value
CM_DIV_H12_DPLL_PER	4	Register value
CM_DIV_H14_DPLL_PER	4	Register value

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Table 28-14. Software Booting Configuration Structure (continued)

Field	Size (Bytes)	Description
USB HS DPLL Settings		
CM_CLKMODE_DPLL_USB	4	Register value
CM_AUTOIDLE_DPLL_USB	4	Register value
CM_CLKSEL_DPLL_USB	4	Register value
CM_DIV_M2_DPLL_USB	4	Register value
Peripheral Booting Time-out Configuration		
Section 3 key	4	Synchronization key for section 3: 0xCF00 AA03
Section 3 size	4	Size of the section 3: 0x0000 0008 (8)
Flags	2	Bit [0]: If cleared (= 0), the time-out USB field is ignored. Bit [1]: If cleared (= 0), the time-out boot message field is ignored. Other bits: Reserved
Time-out USB	2	Maximum time allowed for the host to complete the USB enumeration. • 0x0000: OMAP device waits indefinitely for the host to complete USB enumeration. • Others: The value expressed in milliseconds defines the maximum time the OMAP device will wait for the host to complete the USB enumeration (maximum 65.5 seconds).
Time-out boot message	2	Maximum time allowed for the host to send a booting message. • 0x0000: OMAP device waits indefinitely for the host to send a booting message. • Others: The value expressed in milliseconds defines the maximum time the OMAP device will wait for the host to send a booting message (maximum 65.5 seconds).
Padding	2	

28.3.5 Peripheral Booting

28.3.5.1 Description

The ROM code can boot from two different peripherals:

- USB: Super-, high-, and full-speed USB from internal transceiver
- UART3: 115.2 Kbps, 8 bits, even parity, 1 stop-bit, no flow control

The purpose of booting from a peripheral is to download a flash loader code from an external host. This booting method is used primarily for programming flash memories connected to the OMAP device (for example, in the case of initial flashing, firmware update or servicing). Figure 28-16 shows the overall peripheral booting procedure. It consists of a synchronization phase (handshake between the host and the OMAP device) and a transfer phase. The synchronization phase is similar for UART and USB boots. Both transfer phases use the same procedure.

When booting from the UART, the ROM code first initializes the UART3 interface. Then the ROM code sends an ASIC ID block of data. From there, it expects to receive a boot message from the host within 300 ms, by default. Figure 28-14 shows this procedure.

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Figure 28-14. Synchronization Phase for UART

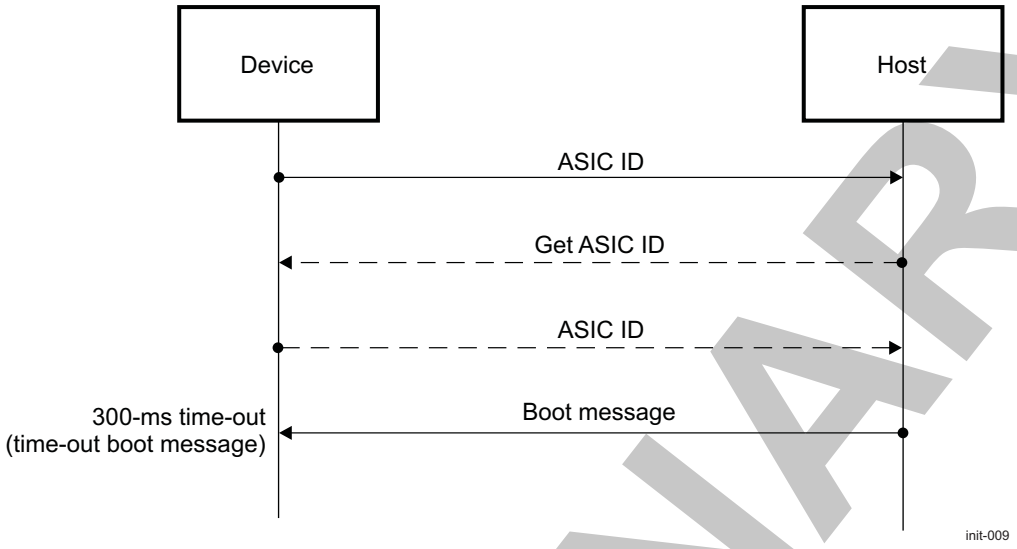
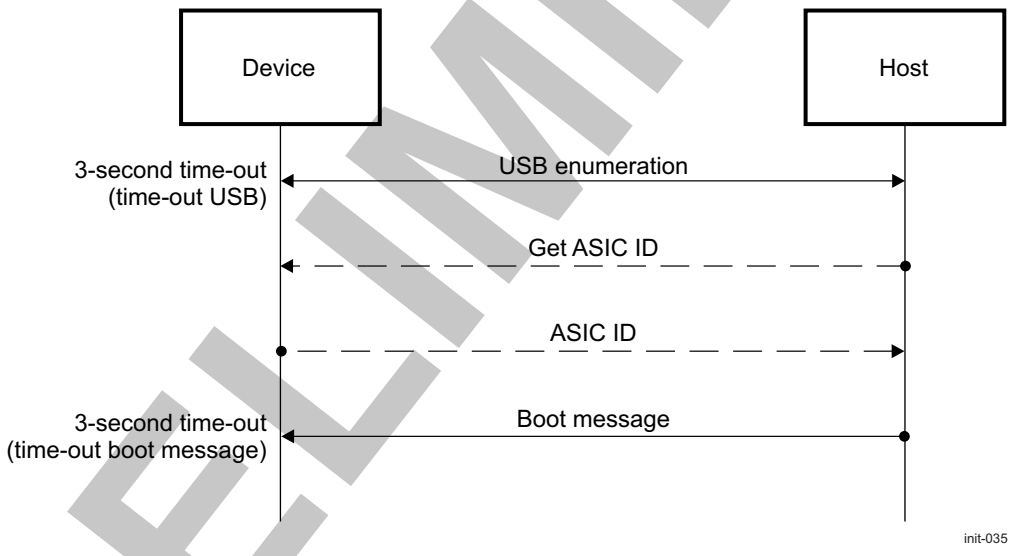


Figure 28-15 shows the procedure when booting from the USB.

Figure 28-15. Synchronization Phase for USB



During the synchronization phase (see Figure 28-14 and Figure 28-15), the OMAP device can provide a small packet of data called the ASIC ID (described in Table 28-15). It is a simple structure that contains different kinds of information, such as ROM version, checksums, and ID.

The default time-outs involved during the synchronization phase can be redefined after a warm reset by means of the software booting configuration (described in Section 28.3.4.5, *Software Booting Configuration*). The host can decide the desired operation by providing a booting message (see Table 28-19). This message can be: Get ASIC ID, peripheral boot, change device, or next device. If the OMAP device receives the Get ASIC ID boot message, it sends back the ASIC ID contents.

If the change device or next device message is received, the ROM code stops the current peripheral booting procedure and returns to the main booting, which decides about the next booting device according to the boot message received.

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If the peripheral boot message is received without a time-out, the OMAP device is entering the transfer phase. From there, the flash loader image size (as a 32-bit word) and the flash loader image itself are expected to be received. The ROM code waits up to 1 minute for completion of image size reception, and up to 1 more minute to download the image. If the download procedure does not complete before this time, the peripheral booting procedure aborts. ROM code continues to examine the devices included in the booting device list. If the download procedure passes, then the image can be executed.

The flash loader image is downloaded directly into internal RAM from address 0x4030 0000 and the maximum size of the downloaded image is 120KiB.

NOTE: Sending an image size of zero skips the peripheral booting procedure.

The USB or UART connection is left open at the end of the transfer phase and once exiting the ROM code for the initial software to take over. It means the initial software can reuse the currently established connection. In the case of a USB connection, the endpoints can be reused as such, without closing the connection and performing a full enumeration again.

Table 28-15. ASIC ID Structure

ASIC ID Item	Size (Bytes)	Description
Items	1	Number of subblocks
ID subblock	7	Device identification information
Reserved subblock	4	This subblock is transmitted, but does not contain useful information in case of GP device.
Reserved subblock	23	This subblock is transmitted, but does not contain useful information in case of GP device.
Reserved subblock	35	This subblock is transmitted, but does not contain useful information in case of GP device.
Checksum subblock	11	CRC (4 bytes)

Table 28-16. Items

Offset	Size (Bytes)	Description
0x00	1	0x05: Number of subblocks USB 0x04: Number of subblocks UART(1)

(1) The checksum subblock is not transmitted over the UART.

Table 28-17. ID Subblock

Offset	Size (Bytes)	Description
0x01	1	0x01: Subblock ID
0x02	1	0x05: Subblock size
0x03	1	0x01: Fixed value
0x04	2	0x54, 0x30: OMAP5430 device
0x06	1	0x07: CH enabled (read from eFuse) 0x17: CH disabled (read from eFuse)
0x07	1	ROM revision 0x02: ES2.0

Table 28-18. Checksum Subblock(1)

Offset	Size (Bytes)	Description
0x46	1	0x15: Subblock ID
0x47	1	0x09: Subblock size
0x48	1	0x01: Fixed value
0x49	4	ROM CRC

(1) The checksum subblock is not transmitted over the UART.

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Table 28-18. Checksum Subblock[1] (continued)

Offset	Size (Bytes)	Description
0x4D	4	0x0000 0000: For GP device

Table 28-19. Booting Messages

Message Name	Value	Description
Peripheral boot	0xF003 0002	Continue peripheral booting.
Get ASIC ID	0xF003 0003	ASIC ID request. The Get ASIC ID request message is optional. If received, the ROM code sends its ASIC ID data to the host in return. The host can issue the Get ASIC ID message multiple times if required. Table 28-15 describes the structure of the ASIC ID.
Change device	0xF003 xx06	Skip current peripheral booting and continue booting from device type indicated by xx: 0x01: XIP 0x02: XIP (with wait monitoring) 0x03: NAND 0x04: OneNAND 0x05: SD card 0x06: eMMC (from boot partition BP1 or BP2) 0x07: eMMC 0x09 SATA 0x43: UART 3 0x45: USB (from internal transceiver) Others: Reserved
Next device	0xFFFF FFFF	Skip current device and move to the next device on the device list.
Memory booting	Others	Skip current peripheral booting and move to the first device for memory booting.

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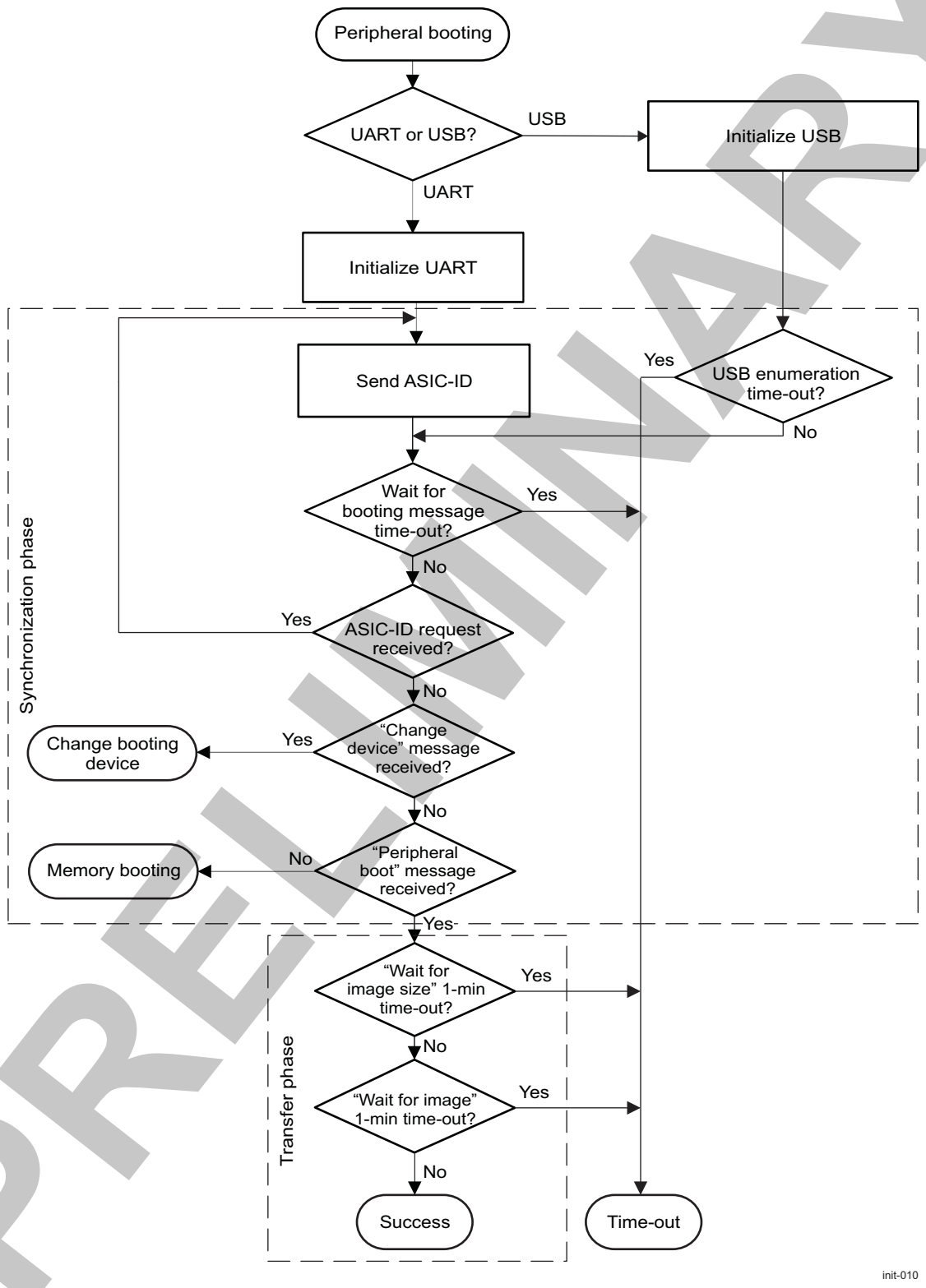
Figure 28-16 shows the peripheral booting procedure.

Figure 28-16. Peripheral Booting Procedure



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28.3.5.2 Initialization Phase for UART Boot

The ROM code supports booting from a UART interface with the following characteristics:

- UART interface 3
- Communication parameters set to 115.2 Kbps, 8 bits, even parity, 1 stop-bit, no flow control
- Two-pin interface: RX/TX
- The boot message default time-out is 300 ms (time-out boot message)

28.3.5.3 Initialization Phase for USB Boot

The ROM code supports booting from a USB interface with the following characteristics:

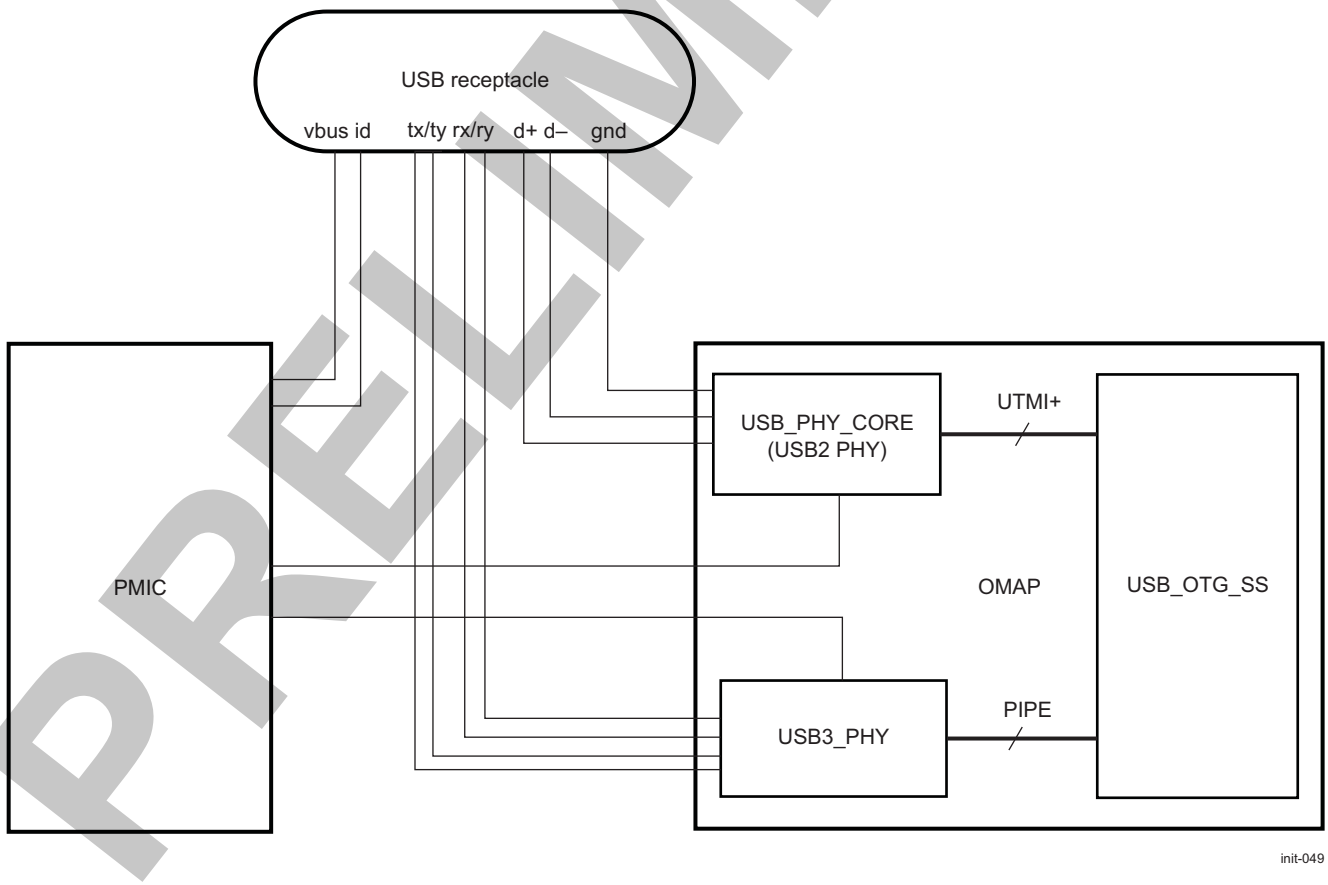
- Using the SS USB OTG (USBOTGSS) module through the USBD0 interface
- OMAP integrated USB transceiver (USB3_PHY or USB_PHY_CORE)
- Enumeration default time-out is 3 seconds (time-out USB)
- The boot message default time-out is 3 seconds (time-out boot message).

NOTE: Even though using OTG-capable hardware, the ROM code does not handle any OTG-specific features.

28.3.5.3.1 System Interconnection

Figure 28-17 shows the interconnection between the USB3 subsystem and its environment components

Figure 28-17. USB3 Subsystem



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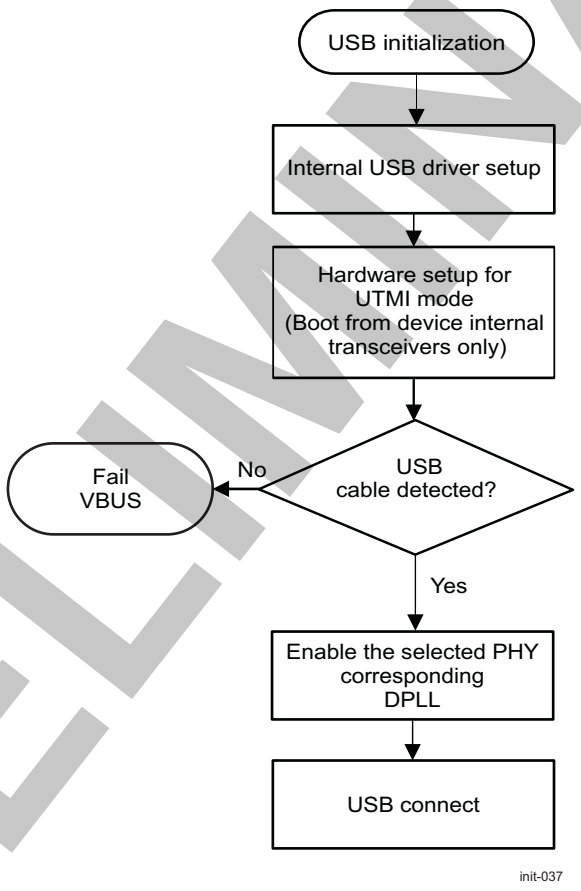
The ROM code supports booting through the USB3 subsystem and enumerates either as an USB2 or USB3 device depending on the nature of the cable connected to board receptacle. OMAP PHYs are assumed to be properly powered by the companion chip before entering the peripheral booting procedure (the ROM code does not take any action related to USB PHYs powering).

micro-B connector plugs into the on-board USB3 receptacle. If the host is USB2-compliant, then TXP/TXN/RXP/RXN differential pairs are left unconnected. In this case, the OMAP device enumerates as a USB2 device through legacy D+/D- differential pair. If an USB3 host is detected (USB3PHY receiver detection mechanism), then the OMAP device enumerates as a USB3 device.

NOTE: The internal USB3_PHY (SS) and USB_PHY_CORE (HS) transceivers must be powered and configured upon startup. No action is expected from the OMAP device ROM code for their configuration.

Figure 28-18 shows the USB initialization procedure.

Figure 28-18. USB Initialization Procedure



NOTE: The ROM code does not consider the USB PHYs charger detection circuitry status.

NOTE: The ROM code assumes that VBUS is always present.

28.3.5.3.2 SATA Peripheral Device Flashing over USB Interface

In the next scheme (see Figure 28-19), it is assumed that the new version of the firmware OMAPFlash Host is located in the PC host. In the same way, the application loaded to OMAP internal L3 On-chip RAM (using the peripheral boot function of the OMAP ROM code) is called OMAPFlash Second.

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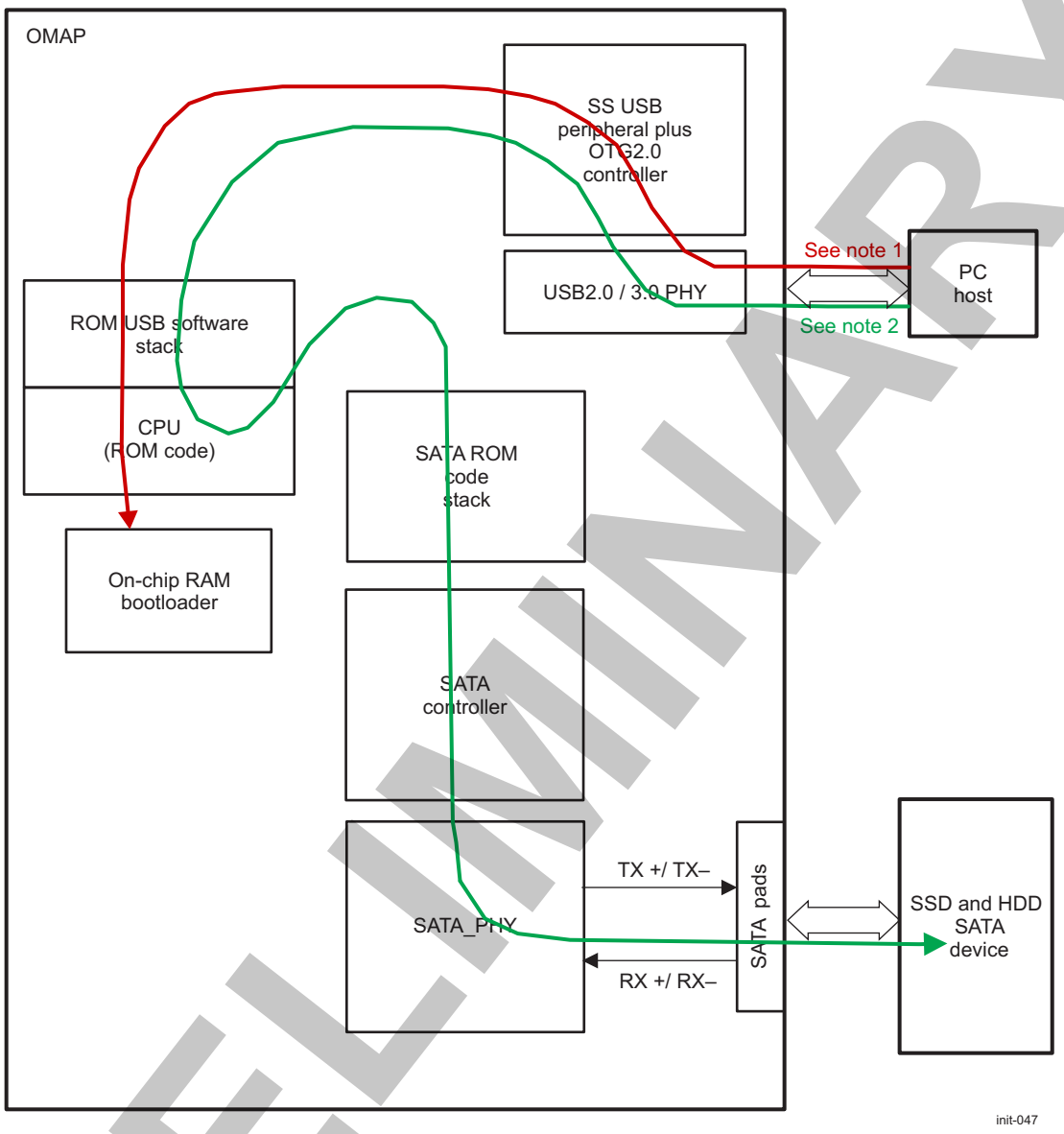
Figure 28-19. SATA Flashing Over USB



(1) ROM boots from USB controller and downloads OMAPFlash Second in RAM.

(2) The PC host is allowed to flash the OMAP firmware located in the SATA device.

28.3.5.3.3 USB Driver Descriptors

USB devices use descriptors to report their attributes. A descriptor is a data structure with a defined format. Each descriptor begins with a byte-wide field that contains the total number of bytes in the descriptor followed by a byte-wide field that identifies the descriptor type. Using descriptors allows concise storage of the attributes of individual configurations so that each configuration can reuse descriptors or portions of descriptors from other configurations that have the same characteristics. Where appropriate, descriptors contain references to string descriptors. String descriptors contain displayable, human-readable description information. These descriptor details can be used for tool development or debugging:

- Device descriptor

  A device descriptor contains general information about a USB device, including global information that applies to the device and all device configurations. A USB device has only one device descriptor. A device-qualifier descriptor is required because the ROM code uses the HS feature of the USB core. Table 28-20 lists the device descriptors.

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Table 28-20. Device Descriptor

Field	Value	Description
bLength	0x12	Size of this descriptor in bytes
bDescriptorType	0x01	Device descriptor type
bcdUSB	0x0210	USB specification release number in binary coded decimal (BCD) format
bDeviceClass	Vendor-specific (0xFF)	Class code
bDeviceSubClass	Vendor-specific (0xFF)	Subclass code
bDeviceProtocol	Vendor-specific (0xFF)	Protocol code
bMaxPacketSize0	0x40	Maximum packet size for endpoint 0
idVendor	0x0451	Vendor ID (Texas Instruments), TI default value
idProduct	0xD01-	Product ID, TI default value
bcdDevice	0x0000	Device release number
iManufacturer	See Section 28.3.5.3.4.	Index of string descriptor describing manufacturer
iProduct	See Section 28.3.5.3.4.	Index of string descriptor describing product
iSerialNumber	See Section 28.3.5.3.4.	Index of string descriptor describing device serial number
bNumConfigurations	0x01	Number of possible configurations

- Device-qualifier descriptor

  The device-qualifier descriptor contains information about a HS-capable device that changes if the device operates at its other speed. This descriptor is retrieved by the host using the GetDescriptor() request (standard device request). Table 28-21 lists the device-qualifier descriptors.

Table 28-21. Device-Qualifier Descriptor

Field	Value	Description
bLength	0x0a	Size of this descriptor in bytes
bDescriptorType	0x06	Device-qualifier descriptor type
bcdUSB	0x0210	USB specification release number in BCD
bDeviceClass	0xFF	Class code
bDeviceSubClass	0xFF	Subclass code
bDeviceProtocol	0xFF	Protocol code
bMaxPacketSize0	0x40	Maximum packet size for endpoint 0
bNumConfigurations	0x01	Number of possible configurations
bReserved	0x00	Reserved for future use

- Configuration descriptor

  This descriptor gives information about a specific device configuration. It describes the number of interfaces supported by the configuration (see Table 28-22).

Table 28-22. Configuration Descriptor

Field	Value	Description
bLength	0x09	Size of this descriptor in bytes
bDescriptorType	0x02	Configuration descriptor type
wTotalLength	–	Combined length of all descriptors
bNumInterfaces	0x01	Number of interfaces supported
bConfigurationValue	0x01	Value to use as an argument for the SetConfiguration() request
iConfiguration	Index	Index of string descriptor describing this configuration
bmAttributes	0xC0	Power setting and remote wakeup
bMaxPower	0x32	Maximum power consumption of the USB device

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- Other speed configuration descriptor

  This descriptor describes the configuration of a HS-capable device if it operates at its other possible speed (see Table 28-23).

Table 28-23. Other Speed Configuration Descriptor

Field	Value	Description
bLength	0x09	Size of this descriptor in bytes
bDescriptorType	0x07	Other speed configuration descriptor type
wTotalLength	–	Combined length of all descriptors
bNumInterfaces	0x01	Number of interfaces supported
bConfigurationValue	0x01	Value to use as an argument for the SetConfiguration() request
iConfiguration	Index	Index of string descriptor describing this configuration
bmAttributes	0xC0	Power setting and remote wakeup
bMaxPower	0x32	Maximum power consumption of the USB device

- Interface descriptor

  This descriptor describes a specific interface in a configuration (see Table 28-24).

Table 28-24. Interface Descriptor

Field	Value	Description
bLength	0x09	Size of this descriptor in bytes
bDescriptorType	0x04	Interface descriptor type
bInterfaceNumber	0x00	Number of this descriptor
bAlternateSetting	0x00	Value to select the alternate setting
bNumEndpoints	0x02	Number of endpoints used for this interface
bInterfaceClass	0xFF	Class code
bInterfaceSubClass	0xFF	Subclass code
bInterfaceProtocol	0xFF	Protocol code
iInterface	Index	Index of string descriptor describing this interface

- Endpoint descriptor

  Each endpoint used for an interface has its own descriptor. This descriptor contains information required by the host to determine the bandwidth requirements of each endpoint. This descriptor is returned as part of the GetDescriptor(Configuration) request (see Table 28-25 and Table 28-26).

Table 28-25. BULK IN Endpoint Descriptor

Field	Value	Description
bLength	0x07	Size of this descriptor in bytes
bDescriptorType	0x05	Endpoint descriptor type
bEndpointAddress	0x81 (1 IN)	Address of the endpoint on the USB device
bmAttributes	0x02 (Bulk)	Type of transfer
wMaxPacketSize	See (1).	Number of endpoints used for this interface
bInterval	0x00	Maximum NAK rate

(1) The maximum size is 0x0200 (512 bytes) for HS bulk endpoint and 0x0040 (64 bytes) for FS bulk endpoint.

Table 28-26. BULK OUT Endpoint Descriptor

Field	Value	Description
bLength	0x07	Size of this descriptor in bytes
bDescriptorType	0x05	Endpoint descriptor type
bEndpointAddress	0x01 (1 OUT)	Address of the endpoint on the USB device

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Table 28-26. BULK OUT Endpoint Descriptor (continued)

Field	Value	Description
bmAttributes	0x02 (Bulk)	Type of transfer
wMaxPacketSize	See (1).	Number of endpoints used for this interface
bInterval	0x00	Maximum NAK rate

(1) The maximum size is 0x0200 (512 bytes) for HS bulk endpoint and 0x0040 (64 bytes) for FS bulk endpoint.

- String descriptors

  String descriptors use UNICODE encoding. The strings in a USB device can support multiple languages. When requesting a string descriptor, the requester specifies the desired language using a 16-bit language ID (LANGID) defined by the USB interface. String index 0 for all languages returns a string descriptor that contains an array of 2-byte LANGID codes supported by the device.

  For the description of the different string descriptors, see:

  – The language ID string descriptor (Table 28-27)
  – The manufacturer ID string descriptor (Table 28-28)
  – The product ID string descriptor (Table 28-29)
  – The configuration string descriptor (Table 28-30)
  – The interface string descriptor (Table 28-31)

Table 28-27. Language ID String Descriptor

Field	Value	Description
bLength	0x04	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type
wLangId	0x0409 (US English)	Language ID code

Table 28-28. Manufacturer ID String Descriptor

Field	Value	Description
bLength	0x24	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type
bString	Texas Instruments	Manufacturer string

Table 28-29. Product ID String Descriptor

Field	Value	Description
bLength	0x12	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type
bString	OMAP5430	Product string

Table 28-30. Configuration String Descriptor

Field	Value	Description
bLength	0x08	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type
bString	pbc	Configuration string

Table 28-31. Interface String Descriptor

Field	Value	Description
bLength	0x08	Size of this descriptor in bytes
bDescriptorType	0x03	String descriptor type

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Table 28-31. Interface String Descriptor (continued)

Field	Value	Description
bString	pbi	Interface string

28.3.5.3.4 USB Customized Vendor and Product IDs

When OMAP ROM Code enumerates through USB, one may want to use his/her own vendor and product IDs rather than TI defaults. Product and Vendor IDs are transmitted as part of the USB Standard Device Descriptor during the USB device enumeration process (resp. idProduct and idVendor 16 bits fields).

Product IDs (PIDs) and vendor IDs (VIDs) are stored as part of OMAP chip eFuses and readable from control module. The built-in USB ROM driver behaves differently whether the VID value is either left unfused, or fused with a customer-specific VID. Thus, two main cases are distinguished:

- VID is fused with a customer-specific ID value
- VID is left unfused

Table 28-32 lists standard USB ROM device descriptors. Table 28-33 lists USB ROM descriptor strings.

Table 28-32. USB ROM Standard Device Descriptor

Device Descriptor Field	Size (Bytes)	VID<>0x0000[1] (fused)	VID=0x0000 (unfused)[2]
bLength	1	0x12	
bDescriptorType	1	0x1	
bcdUSB	2	0x0200 (if enumerated in USB2.0 High or Full Speed) 0x0300 (if enumerated in USB3.0 Super Speed)	
bDeviceClass	1	0xFF	
bDeviceSubClass	1	0xFF	
bDeviceProtocol	1	0xFF	
bMaxPacketSize0	1	0x40 (64 bytes if enumerated in USB2.0 high or full speed) 0x09 (2^9 = 512 bytes if enumerated in USB3.0 super speed)	
idVendor	2	(VID value from control module)	0x0451
idProduct	2	(PID value from control module)	0xD011
bcdDevice	2	0x0000	
iManufacturer	1	0x20	0x21
iProduct	1	0x24	0x25
iSerialNumber	1	0	
bNumConfigurations	1	1	

(1) VID other than 0x0 and VID other than 0xFFFF and VID other than 0x0451 values
(2) VID==0x0 or VID==0xFFFF or VID==0x0451

Table 28-33. USB ROM Descriptor Strings

String Descriptor	Size (bytes)	VID<>0x0000	VID=0x0000(unfused)[1]
Serial Number		N/A	
Configuration	8	"pbc"	
Interface	8	"pbi"	
Product	8 / 18	N/A	"OMAP5430"
Manufacturer	8 / 36	N/A	"Texas Instruments"

(1) VID==0x0451

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The ROM code transmits additional descriptors as part of the enumeration procedure: configuration descriptor, device qualifier, language ID string, configuration string, interface string, and function string descriptors. Those do not depend on the VID or PID value.

28.3.5.3.5 USB Driver Functionality

- Transactions supported:
  - Control transactions: Used for standard device requests
  - Bulk transactions: Used for data transfer in the image downloading stage. The ASIC ID is sent to the BULK IN endpoint and the image is transferred from the host over the BULK OUT endpoint.

  The OMAP USB device first attaches to the host as an FS device. In the reset mechanism, the USB core requests HS operation. If the HS negotiation in the reset phase succeeds, further transactions are at HS; otherwise, they are at FS. After reset, the USB driver checks for the speed of the device, whether it is FS or HS. Depending on the speed configured by the host, the standard USB device requests are answered with the corresponding descriptors.
- Standard device request restrictions:

  Some standard device requests are not supported by the driver because the USB driver is dedicated for use by the ROM code for peripheral booting. Table 28-34 lists the standard device requests supported by the driver.

Table 28-34. Standard Device Requests Supported

Request	Description	Support
CLEAR_FEATURE	Sets or clears a specific feature	Supported only for the ENDPOINT_HALT feature
GET_CONFIGURATION	Returns the current device configuration value	Yes
GET_DESCRIPTOR	Returns the specified descriptor	Yes
GET_INTERFACE	Returns the selected alternate setting for the specified interface	Yes
GET_STATUS	Returns the status for the specified recipient	Yes
SET_ADDRESS	Sets the device address	Yes
SET_CONFIGURATION	Sets the device configuration	Yes
SET_DESCRIPTOR	Updates existing descriptors or adds new descriptors	Runtime updating of descriptors is not supported.
SET_FEATURE	Sets or enables a specific feature	Supported only for the ENDPOINT_HALT feature
SET_INTERFACE	Selects an alternate setting in an interface	Runtime setting of alternate features is not supported.
SYNCH_FRAME	Sets and reports an endpoint synchronization frame	No, because isochronous transfers are not used

28.3.6 Fast External Booting

28.3.6.1 Overview

The fast external boot is a special memory booting mode, possible only on OMAP GP devices. It consists of a blind jump to a code in an external XIP memory device connected to GPMC CS0. Fast external booting is set up by means of the SYSBOOT configuration pins and lets customers create their own booting code.

The jump is performed with minimum on-chip ROM code execution.

28.3.6.2 Fast External Booting Procedure

Figure 28-20 shows the procedure for fast external boot. The code is at the beginning and is written in Assembly Language. The code does not use any RAM and is designed for fast execution.

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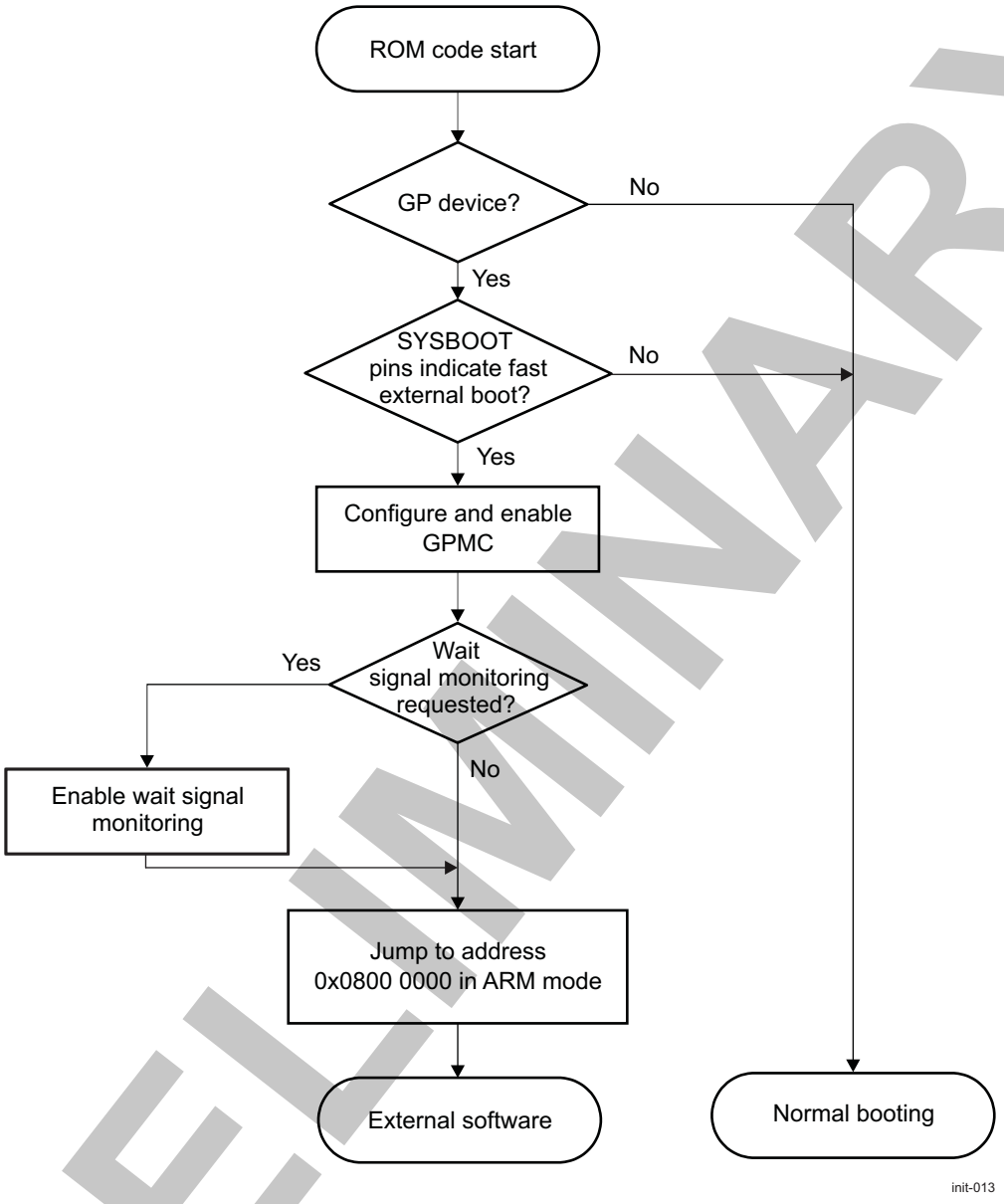
Figure 28-20. Fast External Boot Procedure



28.3.7 Memory Booting

28.3.7.1 Overview

The memory booting process starts an external code in memory devices. ROM code can use only the memory type of booting devices as permanent booting devices (that is, devices examined after both cold [POR] and warm resets). Temporary booting devices are examined only after cold resets. The supported permanent booting devices are:

- NOR flash devices
- NAND flash devices
- OneNAND and Flex-OneNAND devices
- eMMC memories
- SD cards
- SATA SSD and HDD storage memory devices

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Two main groups of permanent booting devices are distinguished by code shadowing. Code shadowing means copying code from a nondirectly addressable device (non-XIP) to RAM, where the code can be executed. Directly addressable devices are XIP devices.

Figure 28-21 shows the general memory booting procedure common to all types of devices. First, CH is copied to internal RAM. It is copied even for XIP devices, because the OMAP device can temporarily lose a connection with XIP memory during CH execution (for example, while updating interface timings). The second step is to shadow the image, if the device is not XIP. The last step is image execution and any return from image results in a dead loop.

If CH copying or shadowing fails, memory booting returns to the main booting procedure, which selects the next device for booting.

A booting image is considered to be present on a GP device, when the first 4 bytes word of the sector is not equal to 0000 0000h or FFFF FFFFh.

During the first read sector (512 bytes) call, sectors are copied to a temporary OMAP on-chip SRAM buffer. Once the image is found and the destination address is known, the content of the temporary buffer is moved to the target OMAP on-chip SRAM location so it is required to reread the first image sector. For a GP device, the GP header is not copied into target buffer location; therefore, only executable code is in device on-chip RAM, with the first executable instruction at the destination address.

eMMC, SD cards, NAND, OneNAND/Flex-OneNAND and SATA SSD or HDD devices can hold up to four copies of the booting image. Therefore, the ROM code searches for one valid image out of the four copies, if present, by walking over the first blocks of mass storage space. Other XIP devices (NOR) use only one copy of the booting image.

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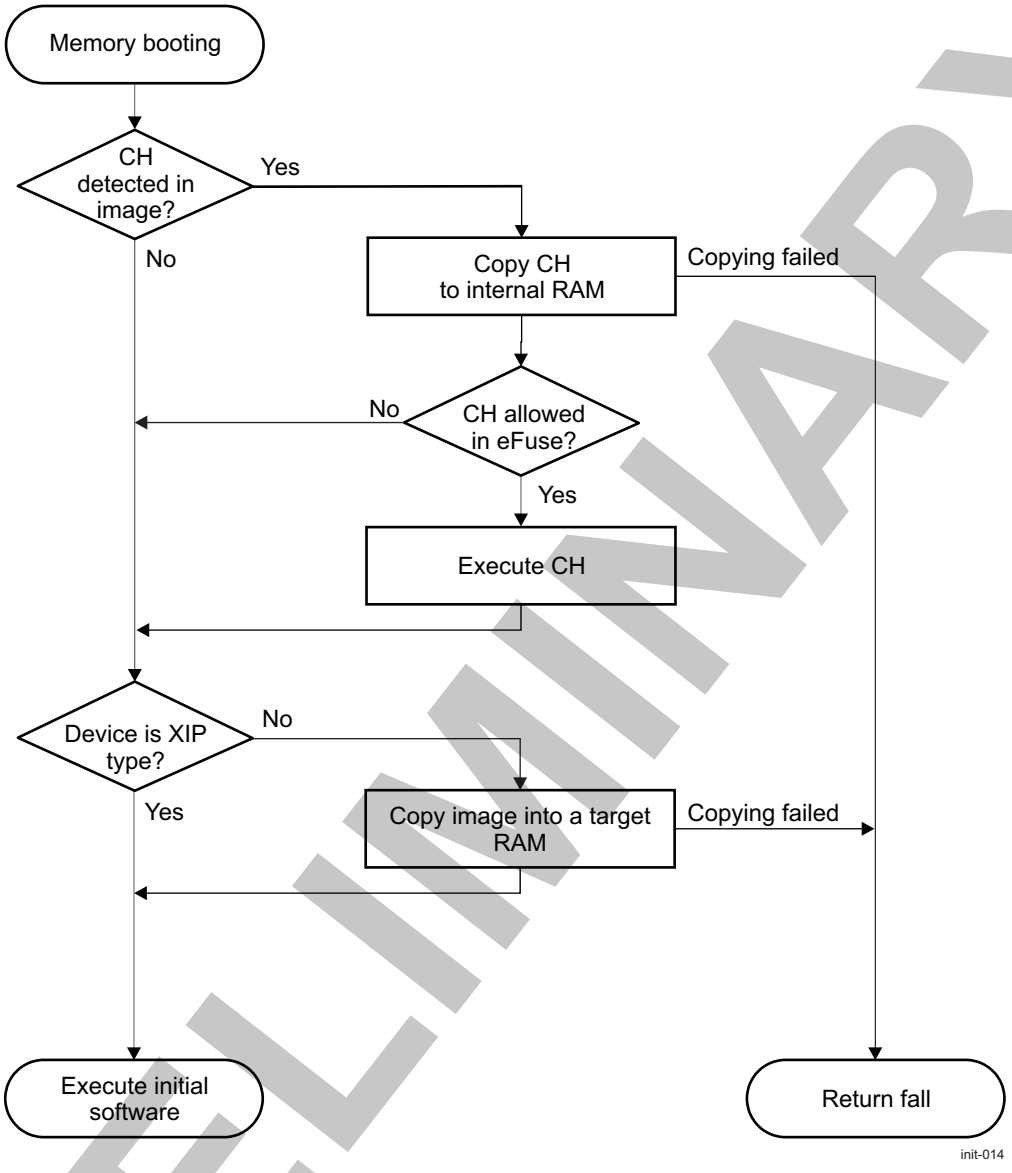
Figure 28-21. Memory Booting Procedure



28.3.7.2 Non-XIP Memory

Figure 28-22 shows the procedure used when memory booting runs with non-XIP devices. The shaded procedures are specific to each device. NAND and OneNAND/Flex-OneNAND devices use up to four copies of the image in the first four physical blocks. Therefore, the ROM code searches for the image in the first four physical blocks of these devices. Other devices use only one copy of the image and the block loop runs only once.

During image shadowing on a GP device, the CH is expected to be in a separate sector before the initial software.

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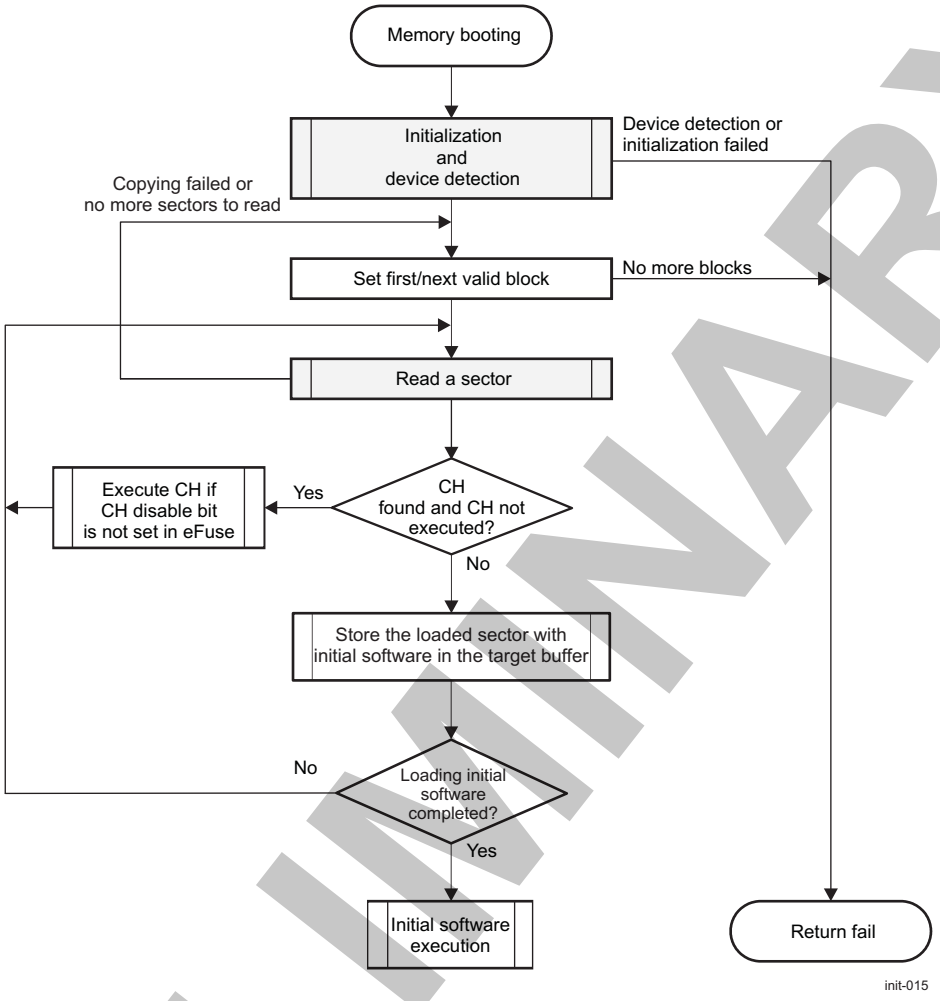
Figure 28-22. Image Shadowing on GP Device



For more information about the GPMC module, see Section 15.4.1, *GPMC Overview*, in Chapter 15, *Memory Subsystem*.

Section 28.3.7.4, Section 28.3.7.5, Section 28.3.7.6, and Section 28.3.7.7describe the supported device types.

28.3.7.3 XIP Memory

The ROM code can boot directly from XIP devices, such as NOR flash memories, that have the following characteristics:

- The GPMC is the communication interface.
- Memories up to 1Gibit (128MiB) can be connected.
- x16 data bus width only
- Asynchronous protocol and address/data multiplexed mode
- The GPMC clock is 66.5 MHz.
- The device is connected to CS0 mapped to address 0x0800 0000.
- The wait pin gpmc_wait0 signal is monitored according to the sys_boot configuration pins.

For an XIP memory booting, no user intervention is required; the following debugging steps are described. Only the CH, which is not mandatory, lets users change clock settings and GPMC parameters. Failure in CH copying causes a return to the main booting procedure, which selects the next device for booting.

Booting from an XIP device consists of the following steps:

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1. Configure the GPMC for XIP device access.
2. Verify that the CH is present at address 0x0800 0000. If the CH is present, copy the entire sector (512 bytes) to internal RAM and execute the CH.
3. Set the image location:
   - 0x0800 0000 if the CH is not found
   - 0x0800 0200 if the CH is found
4. Verify that a bootable image is at the image location.
5. If the image is found, execute it.
6. If the image is not found, return from XIP booting to the main booting loop.

28.3.7.3.1 GPMC Initialization

Table 28-35 lists the timing settings of the GPMC when set for XIP and other address-data accessible devices, such as OneNAND and Flex-OneNAND. Table 28-35 is included for debug information.

Table 28-35. XIP Timing Parameters

Parameter	Value (Clock Cycles)[1]	Register Initialization (where i = 0–7)	Reset Value
Write cycle period	17	The GPMC_CONFIG5_i[12:8] WRCYCLETIME bit field is set to 0x11.	0x11
Read cycle period	17	The GPMC_CONFIG5_i[4:0] RDCYCLETIME bit field is set to 0x11.	0x11
CS low time	1	The GPMC_CONFIG2_i[3:0] CSONTIME bit field is set to 0x1.	0x1
CS high time	16	The GPMC_CONFIG2_i[12:8] CSRDOFFTIME bit field is set to 0x10.	0x10
ADV low time	1	The GPMC_CONFIG3_i[3:0] ADVONTIME bit field is set to 0x1.	0x1
ADV high time	2	The GPMC_CONFIG3_i[12:8] ADVRDOFFTIME bit field is set to 0x2.	0x2
OE low time	3	The GPMC_CONFIG4_i[3:0] OEONTIME bit field is set to 0x3.	0x6
OE high time	16	The GPMC_CONFIG4_i[12:8] OEOFFTIME bit field is set to 0x10.	0x10
WE low time	3	The GPMC_CONFIG4_i[19:16] WEONTIME bit field is set to 0x3.	0x05
WE high time	15	The GPMC_CONFIG4_i[28:24] WEOFFTIME bit field is set to 0xF.	0x10
Data latch time	15	The GPMC_CONFIG5_i[20:16] RDACCESSTIME bit field is set to 0xF.	0x0F

[1] The one clock cycle is approximately 15 ns, which corresponds to a 66.5-MHz frequency.

There is no specific identification routine executed before booting from an XIP device.

NOTE: The device ROM Code enables the gpmc_a16 to gpmc_a25 address signals on their device-corresponding pads in the control module (CTRL_MODULE_CORE_PAD) by setting the appropriate GPMC muxmode. Therefore, all GPMC address lines are accessible for GPMC booting. For more details, see Section 18.4.8.3, *Pad Multiplexing Register Fields*, of Chapter 18, *Control Module*.

28.3.7.4 NAND

NAND flash memory is not an XIP device; it requires shadowing before the code can be executed. ROM code support for the NAND flash devices has the following characteristics:

- The GPMC is the communication interface.
- Device from 512 Mibit (64MiB)
- x8 and x16 bus width
- Support for large page size (2048 bytes + 64 spare bytes) or very large page size (4096 bytes + 128/218 spare bytes)
- Chip enable (CE) don't care devices only
- Single-level cell (SLC) and multilevel cell (MLC) devices

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- Device identification based on ONFI or ROM table
- ECC correction: 8 bits per sector for most devices (16 bits per sector for devices with large spare area)
- GPMC timings are adjusted for NAND access.
- The GPMC clock is 66.5 MHz.
- The device is connected to CS0.
- The gpmc_wait0 wait-pin signal is connected to the NAND BUSY output.
- Four physical blocks are searched for an image. Block size depends on the device.

For NAND memory booting, no user intervention is needed; the information in the following subsections is included for debugging. Only the CH, which is not mandatory, lets the user change clock settings and GPMC parameters. Failure in CH copying causes a return to the main booting procedure, which selects the next device for booting.

28.3.7.4.1 Initialization and NAND Detection

The initialization routine for NAND consists of three parts: GPMC initialization, device detection with parameter determination, and bad block detection.

- GPMC initialization

  The GPMC interface is configured so that it can access NAND. Because NAND memories do not need the address bus, it is released. The data bus width is initially set to 8 bits. If necessary, it is changed to 16 bits after the device parameters are determined. Table 28-36 shows the GPMC configuration used during NAND boot. Table 28-36 is included for debug information.

Table 28-36. NAND Timing Parameters

Parameter	Value (Clock Cycles)	Register Initialization (where i = 0–7)	Reset Value
Write cycle time	20	GPMC_CONFIG5_i[12:8] WRCYCLETIME = 0x14	0x11
Read cycle time	20	GPMC_CONFIG5_i[4:0] RDCYCLETIME = 0x14	0x11
CS low time	0	GPMC_CONFIG2_i[3:0] CSONTIME = 0x0	0x1
CS low to OE low time	5	GPMC_CONFIG4_i[3:0] OEONTIME = 0x5	0x6
CS low to OE high time	16	GPMC_CONFIG4_i[12:8] OEOFFTIME = 0x10	0x10
CS low to WE low time	1	GPMC_CONFIG4_i[19:16] WEONTIME = 0x1	0x5
CS low to WE high time	15	GPMC_CONFIG4_i[28:24] WEOFFTIME = 0xF	0x10
CS low to data latch time	14	GPMC_CONFIG5_i[20:16] RDACCESSTIME = 0xE	0xF

- Device detection and parameters

  The ROM code first performs an initial wait for device auto initialization (with a 250-ms time-out) with polling of the ready information. Then, it must identify the NAND type connected to the GPMC interface. The GPMC is initialized using 8 bits, asynchronous mode. The NAND device is reset (command FFh) and its status is polled until ready for operation (with a 100-ms time-out). The ONFI Read ID (command 90h/address 20h) is sent to the NAND device. If it replies with the ONFI signature (4 bytes) then a Read parameters page (command ECh) is sent. The information provided in Table 28-37 is then extracted: page size, spare area size, number of pages per block, and the addressing mode. The remaining data bytes from the parameter page stream are ignored.

Table 28-37. ONFI Parameters Page Description

Offset	Description	Size (Bytes)
6	Features supported	2
80	Number of data bytes per page	4
84	Number of spare bytes per page	2

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Table 28-37. ONFI Parameters Page Description (continued)

Offset	Description	Size (Bytes)
92	Number of pages per block	4
101	Number of address cycles	1

If the ONFI Read ID command fails (it will be the case with any device not supporting ONFI), then the device is reset again with polling for device to be ready (with 100-ms time-out). Then, the standard Read ID (command 90h/address 00h) is sent. If the Device ID (second byte of the ID byte stream) is recognized as being a supported device, then the device parameters are extracted from an internal ROM code table. Table 28-38 lists the supported NAND devices.

Table 28-38. Supported NAND Devices

Capacity	Device ID	Bus Width	Page Size in Bytes
512 Mibit	F0h	8	2048
512 Mibit	C0h	16	2048
512 Mibit	A0h	8	2048
512 Mibit	B0h	16	2048
512 Mibit	F2h	8	2048
512 Mibit	C2h	16	2048
512 Mibit	A2h	8	2048
512 Mibit	B2h	16	2048
1 Gibit	F1h	8	2048
1 Gibit	C1h	16	2048
1 Gibit	A1h	8	2048
1 Gibit	B1h	16	2048
2 Gibit	DAh	8	2048 (4096)
2 Gibit	CAh	16	2048 (4096)
2 Gibit	AAh	8	2048 (4096)
2 Gibit	BAh	16	2048 (4096)
2 Gibit	83h	8	2048 (4096)
2 Gibit	93h	16	2048 (4096)
4 Gibit	DCh	8	2048 (4096)
4 Gibit	CCh	16	2048 (4096)
4 Gibit	ACh	8	2048 (4096)
4 Gibit	BCh	16	2048 (4096)
4 Gibit	84h	8	2048 (4096)
4 Gibit	94h	16	2048 (4096)
8 Gibit	D3h	8	2048 (4096)
8 Gibit	C3h	16	2048 (4096)
8 Gibit	A3h	8	2048 (4096)
8 Gibit	B3h	16	2048 (4096)
8 Gibit	85h	8	2048 (4096)
8 Gibit	95h	16	2048 (4096)
16 Gibit	D5h	8	2048 (4096)
16 Gibit	C5h	16	2048 (4096)
16 Gibit	A5h	8	2048 (4096)
16 Gibit	B5h	16	2048 (4096)
16 Gibit	86h	8	2048 (4096)
16 Gibit	96h	16	2048 (4096)
32 Gibit	D7h	8	2048 (4096)

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Table 28-38. Supported NAND Devices (continued)

Capacity	Device ID	Bus Width	Page Size in Bytes
32 Gibit	C7h	16	2048 (4096)
32 Gibit	A7h	8	2048 (4096)
32 Gibit	B7h	16	2048 (4096)
32 Gibit	87h	8	2048 (4096)
32 Gibit	97h	16	2048 (4096)
64 Gibit	DEh	8	2048 (4096)
64 Gibit	CEh	16	2048 (4096)
64 Gibit	AEh	8	2048 (4096)
64 Gibit	BEh	16	2048 (4096)

After retrieving parameters from the table, the page size and block size are updated based on the fourth byte of the NAND ID data. Because of inconsistency among manufacturers, only devices recognized to be at least 2 Gibit have these parameters updated. Therefore, the ROM code supports 4-KiB page devices, but only if their size, according to the table, is at least 2 Gibit. Devices that are smaller than 2 Gibit have the block size parameter set to 128 KiB (when the page size is 2 KiB). Table 28-39 lists the fourth ID data byte encoding used in the ROM code.

Table 28-39. Fourth NAND ID Data Byte

Item	Description	I/O Number							
		7	6	5	4	3	2	1	0
Page size	512 bytes							0	0
	2048 bytes							0	1
	4096 bytes							1	0
	8192 bytes							1	1
Cell type [1]	2 levels					0	0		
	4 levels					0	1		
	8 levels					1	0		
	16 levels					1	1		
Block size	64 KiB			0	0				
	128 KiB			0	1				
	256 KiB			1	0				
	512 KiB			1	1				

(1) Read by ROM code only when the manufacturer code (first ID byte) is 98h

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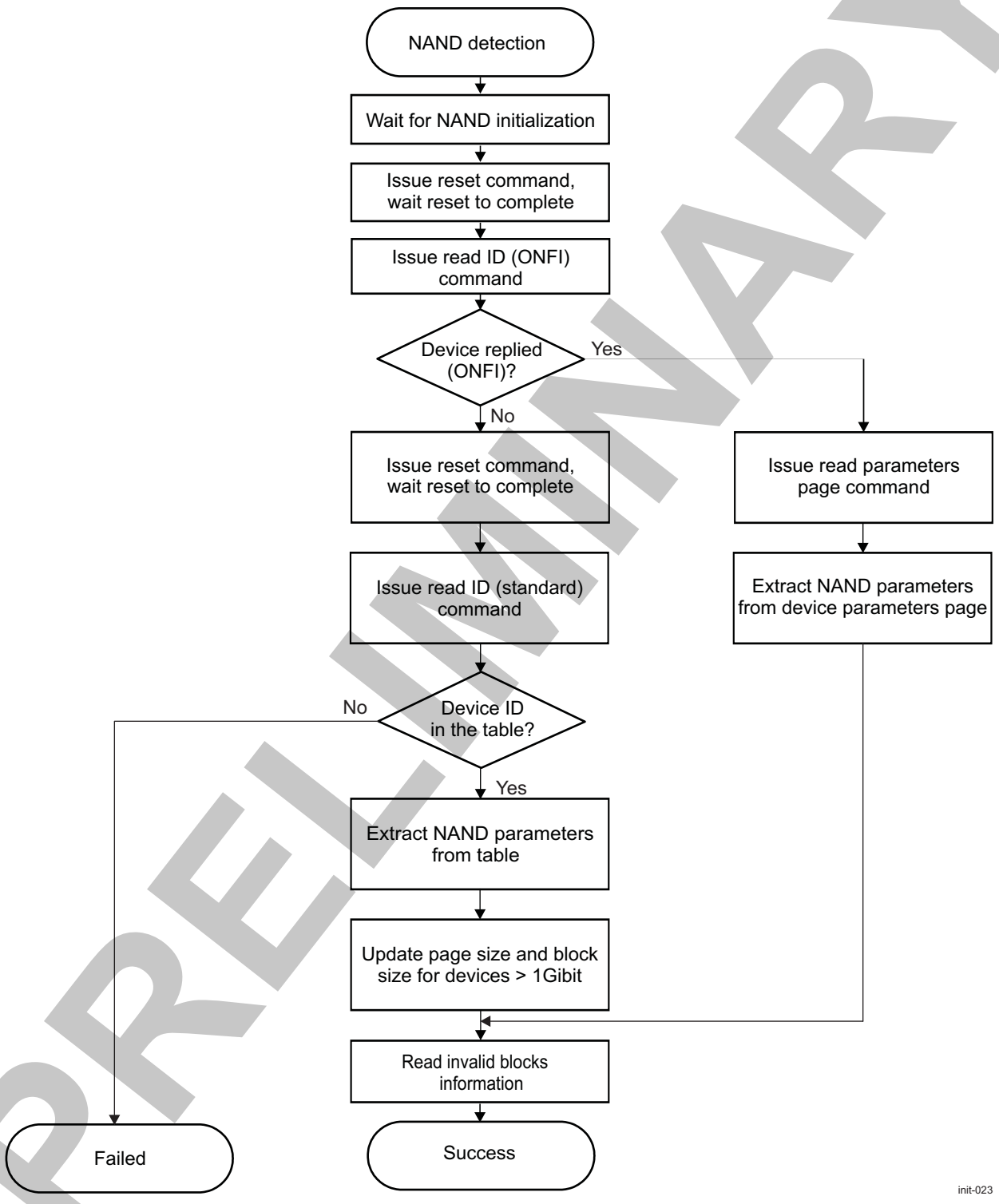
Figure 28-23 shows the detection procedure. When the NAND device is successfully detected, the ROM code changes the GPMC to 16-bit bus width, if necessary.

Figure 28-23. NAND Device Detection



- Bad block verification

  Invalid blocks contain invalid bits whose reliability cannot be ensured by the manufacturer. These bits are identified in the factory or during the programming and reported in the initial invalid block information in the spare area on the first and second page of each block. Because the ROM code

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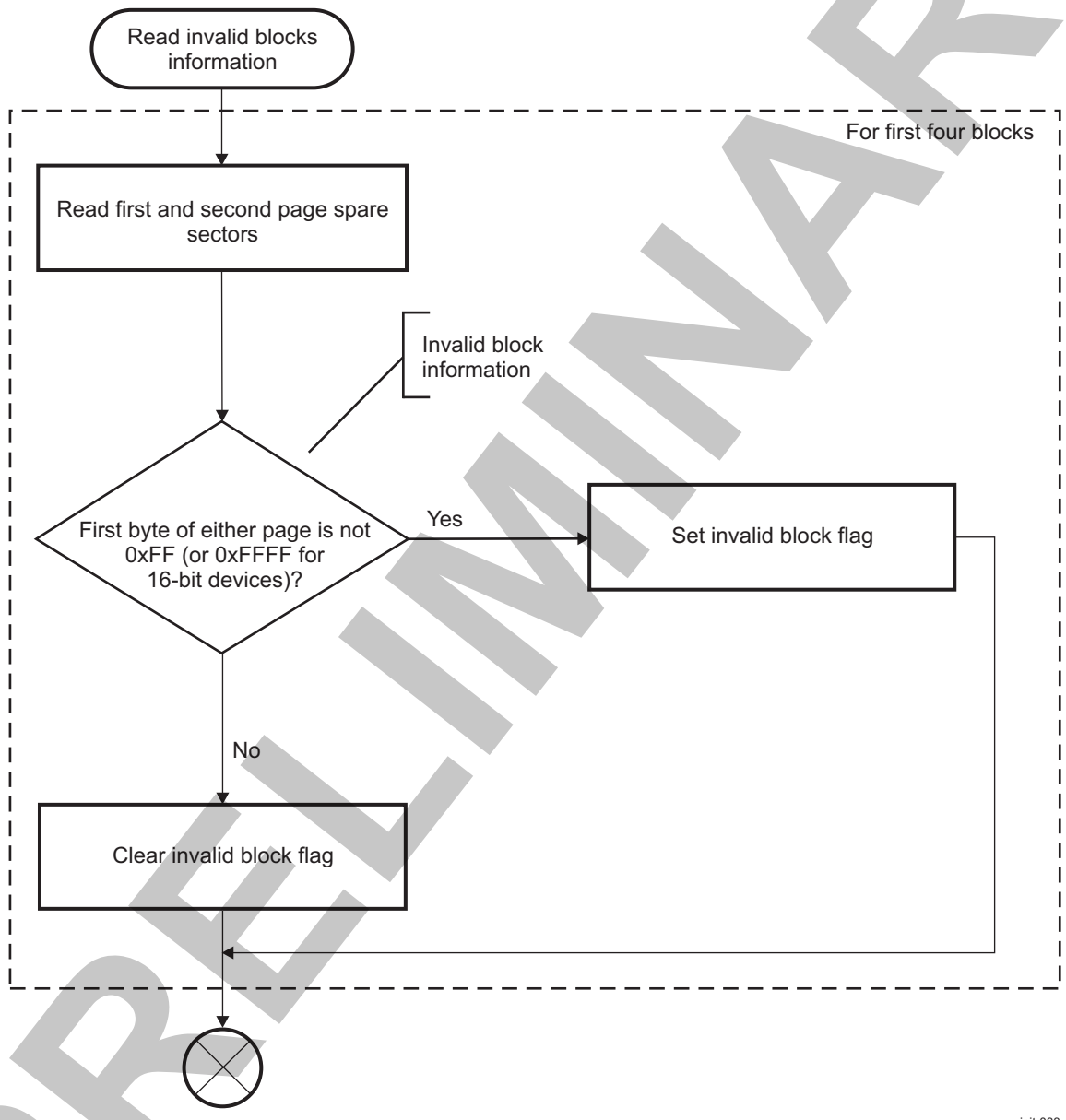
looks for an image in the first four blocks, it detects the validity status of these blocks. Blocks detected as invalid are not accessed later. Block validity status is coded in the spare areas of the first two pages of a block (first byte equal to FFh in the first and second pages for an 8-bit device/first word equal to FFFFh in the first and second pages for a 16-bit device).

Figure 28-24 shows the invalid block detection routine. The routine consists in reading spare areas and checking the validity data pattern.

Figure 28-24. Bad NAND – Invalid Block Detection



28.3.7.4.2 NAND Read Sector Procedure

During the booting procedure, the ROM code reads 512-byte sectors from the NAND device. The reading fails in two cases:

- The accessed sector is in a block marked as invalid.
- The accessed sector contains an error that cannot be corrected with ECC.

The ROM code uses normal read (command 00h 30h) for reading NAND page data.

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Page data can contain errors caused by memory alteration. The ROM code uses an ECC correction algorithm to detect and possibly correct those errors. The default ECC correction applied is BCH 8b/sector using the GPMC and ELM hardware.

For device ID codes D3h, C3h, D5h, C5h, D7h, C7h, DEh, and CEh when the manufacturer code (first ID byte) is 98h, the cell type information is checked in the fourth byte of ID data. If it is equal to 10b, the ECC correction applied is BCH 16b/sector.

The BCH data is automatically calculated by the GPMC on reading each 512-byte sector. The computed ECC is compared against the ECC stored in the spare area for the corresponding page. Depending on the page size, the amount of ECC data bytes stored in the corresponding spare area is different. Figure 28-25 and Figure 28-26 show the mapping of ECC data inside the spare area for 2-KiB page and 4-KiB page devices, respectively. If both ECC data are equal, the read sector function returns the read 512-byte sector without error. Otherwise, the ROM code tries to correct errors in the corresponding sector (this procedure is assisted by the ELM hardware) and returns the data if successful. If errors are uncorrectable, the function returns with FAIL.

Figure 28-25. ECC Data Mapping for 2-KiB Page and 8b BCH Encoding

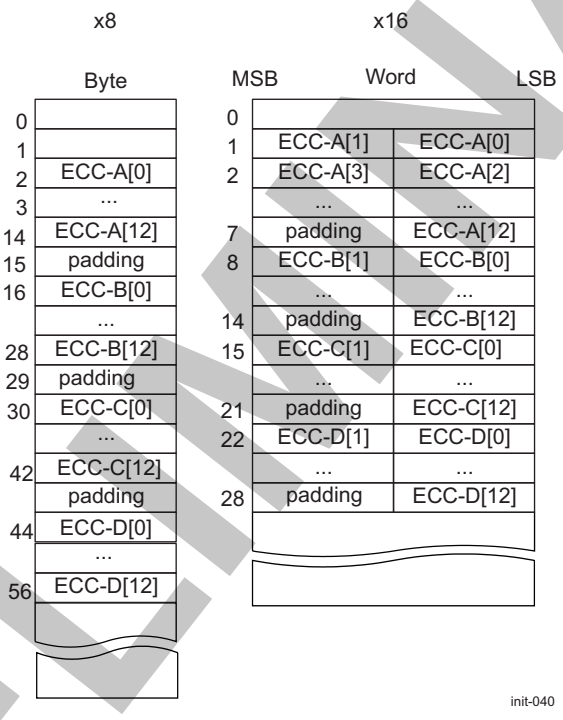

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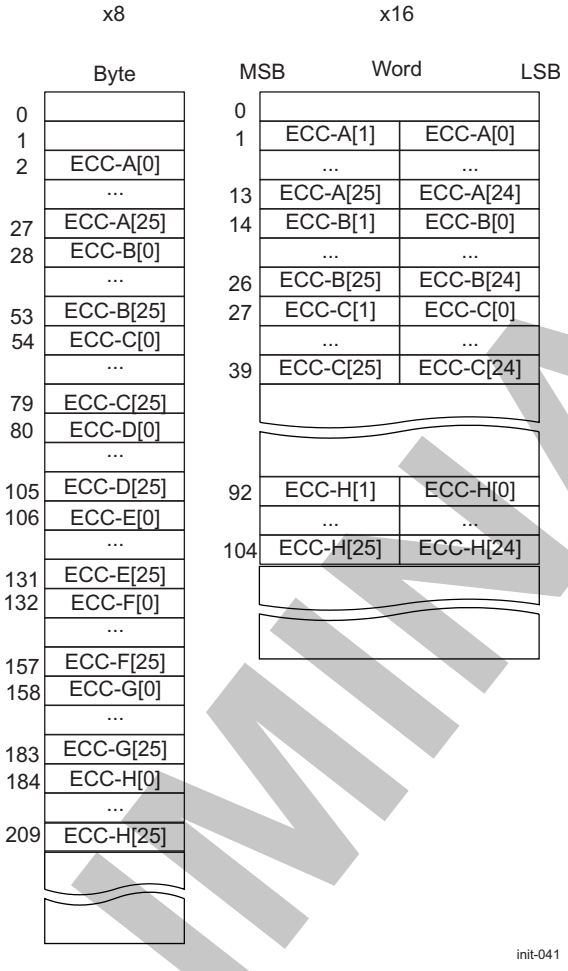
Figure 28-26. ECC Data Mapping for 4-KiB Page and 16b BCH Encoding



28.3.7.5 OneNAND/Flex-OneNAND

The ROM code support for OneNAND/Flex-OneNAND devices has the following characteristics:

- Devices from 512 Mibits
- The GPMC is the communication interface.
- x16 data bus width only
- Asynchronous protocol and address/data multiplexed mode
- GPMC reset default timings are used.
- The GPMC clock is 66.5 MHz.
- The device is connected to GPMC CS0 mapped to address 0x0800 0000.
- The wait pin signal gpmc_wait0 is not monitored.
- Four physical blocks are searched for an image. The block size is 128KiB (typically).
- The image size must NOT exceed the block size
- Data correction is fully handled by the OneNAND/FlexOneNAND device

The OneNAND/Flex-OneNAND device is a NAND matrix coupled with RAM buffers and a NOR-type interface. ECC correction handling is done automatically by the internal state-machine. The page to be accessed is first loaded in the RAM buffer using memory-mapped registers. Then, the page is read directly from the buffer using a NOR-type interface.

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For OneNAND/Flex-OneNAND memory booting, no user intervention is required. The information in the following sections is included for debugging. Only the CH, which is not mandatory, lets users change clock settings and GPMC parameters. Failure in CH copying causes a return to the main booting procedure, which selects the next device for booting.

28.3.7.5.1 Initialization and OneNAND/Flex-OneNAND Detection

The initialization routine for OneNAND/Flex-OneNAND consists of two parts: GPMC initialization and device detection with parameter determination.

- GPMC initialization

  The ROM code first initializes the GPMC interface in XIP mode (that is, asynchronous 16-bit multiplexed mode). Wait signal monitoring is disabled.

- Device detection and parameters

  The ROM code identifies a OneNAND/Flex-OneNAND device by reading the device identification data. There are two ways to read identification data: using serial commands and reading from fixed memory-mapped registers. The ROM code reads identification data using both methods and compares the results. When the comparison passes, the ROM code assumes that the OneNAND/Flex-OneNAND device is connected. If the device is successfully recognized, the ROM code reads the device configuration (number and size of data buffers) and configures it for asynchronous mode (default).

28.3.7.5.2 OneNAND/Flex-OneNAND Read Sector Procedure

When booting requests a sector from the OneNAND/Flex-OneNAND device, the ROM code performs the load operation, which transfers the content of the requested sector to the data buffer RAM. The ROM code waits until the operation completes, polling the OneNAND/Flex-OneNAND interrupt register. The status register is then checked and the ROM code returns FAIL if the operation completes with an error. Otherwise, the data buffer RAM is copied to the destination buffer. Figure 28-27 shows this procedure.

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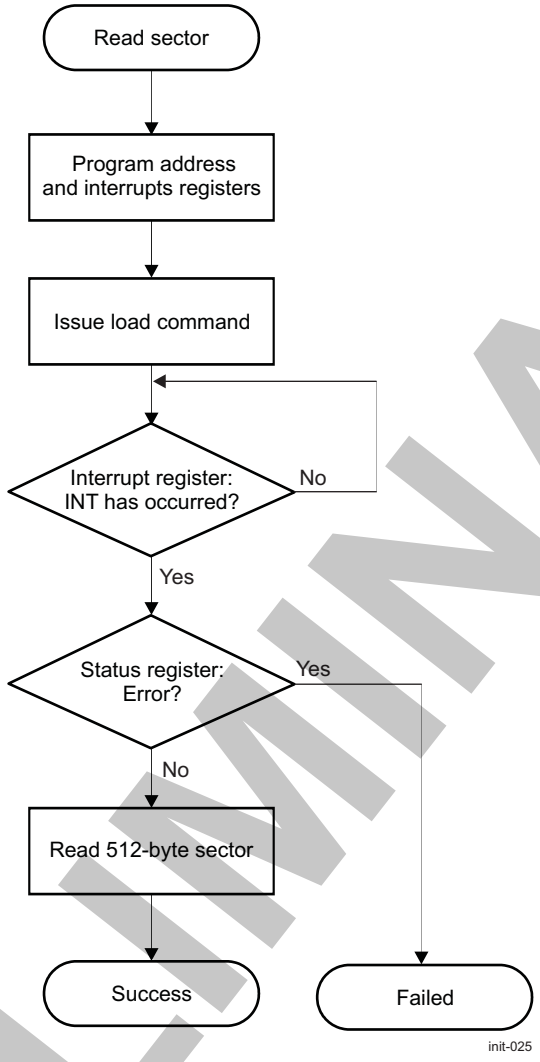
Figure 28-27. OneNAND/Flex-OneNAND Read Sector



28.3.7.5.3 OneNAND/Flex-OneNAND Support Limitations

As described in Section 28.3.7.5.1, *Initialization and OneNAND/Flex-OneNAND Detection*, the ROM code checks only the coherency of the device ID obtained by two different methods. There is no table of supported Flex-OneNANDs in ROM code. This removes any dependency of the ROM code on device IDs from different manufacturers. However, the driver works with the following assumption:

- Page size is assumed to be 2048 bytes, divided into four 512-byte sectors. In case of OneNAND/Flex-OneNAND, with 4096-byte pages, divided into eight sectors, users must program only the first sectors (sectors 0 through 3) of each page. Sectors 4 through 7 of each page are not considered by the driver.

28.3.7.6 eMMC Memories and SD Cards

The OMAP device allows booting from eMMC embedded memories or SD cards connected to OMAP embedded MMC2 or MMC1 controllers I/Os, respectively. The booting interface is selected by configuration of the SYS_BOOT pins.

The OMAP device high speed MMC/SD/SDIO host controller (MMCHS) handle the physical layer, while the ROM code handles the simplified logical protocol layer (read-only protocol). A limited range of commands is implemented in the ROM code.

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The SD card interface supports 1.8-V/3-V digital I/Os. The selection on I/O voltage level is done using the PBIAS circuitry. The PBIAS reference level is sensed by the ROM code and PBIAS cell voltage setup appropriately before any communication with the SD card device. The eMMC interface supports only 1.8-V digital I/Os.

The OMAP device supports three booting modes:

- Raw (Boot): The booting image is read from one of the selectable partitions in raw mode (this mode is also called Alternative Boot Operation mode and applies to eMMC only).
- Raw (UDA): The booting image is read from the user data area (eMMC and SD).
- File system (FAT12/16/32 with or without master boot record): The image data is read from a booting file within a file system in the user data area (eMMC and SD).

NOTE: File system mode is not supported when booting from an eMMC partition.

28.3.7.6.1 eMMC Memories

The ROM code supports booting from eMMC cards, with the following conditions:

- eMMC memory devices compliant with *Embedded MultiMediaCard (eMMC) eMMC/Card Product Standard, High Capacity, including Reliable Write Boot, and Sleep Modes, Dual Data Rate, Multiple Partitions Supports and Security Enhancement v4.5* from the MMCA Technical Committee. The exception is the hardware reset feature. For example, if the user software requires eMMC device hardware reset, it can be accomplished with a GPIO. To correctly boot from eMMC when using Alternative Boot Operation mode, it is recommended to tie the eMMC RST_N signal to the signal indicating a platform warm reset (nRESWARM).
- eMMC device connected to the OMAP MMC2 controller I/O interface available on the OMAP eMMC pads (one device only connected to the bus).
- The eMMC memory device is powered externally by a PMIC or other power supply.
- When booting from user area: Initial (default) 1-bit SDR mode, optional 4-bit and 8-bit SDR- and DDR-modes using Configuration Header
- Initial SDR- and DDR- modes supported
- Clock frequency when booting from user area:
  - Identification mode: 400 kHz
  - Data transfer mode: 10 MHz, optionally up to 48 MHz by Configuration Header
  - Support for eMMC boot partitions. eMMC booting from boot partitions (BPs), which is typical for booting in Alternative Boot operation mode, is always done at 8-bit / 48 MHz / DDR.

28.3.7.6.1.1 System Conditions and Limitations

The ROM code does not provide a bus direction control signaling in case of using MMC interface 2 with level shifters.

NOTE: The ROM Code does not support large 4-KiB sectors as defined in the latest standard.

The ROM code expects that the eMMC device is powered externally and supplies are set and stable when entering the booting procedure.

The ROM code supports the alternative boot operation mode specific to eMMC devices as described in the *Partition Management* and *Boot Operation Mode* sections of the eMMC Standard. It does not support the hardware boot operation mode (CMD line held low for 74 emmc_clk cycles) described in the same document.

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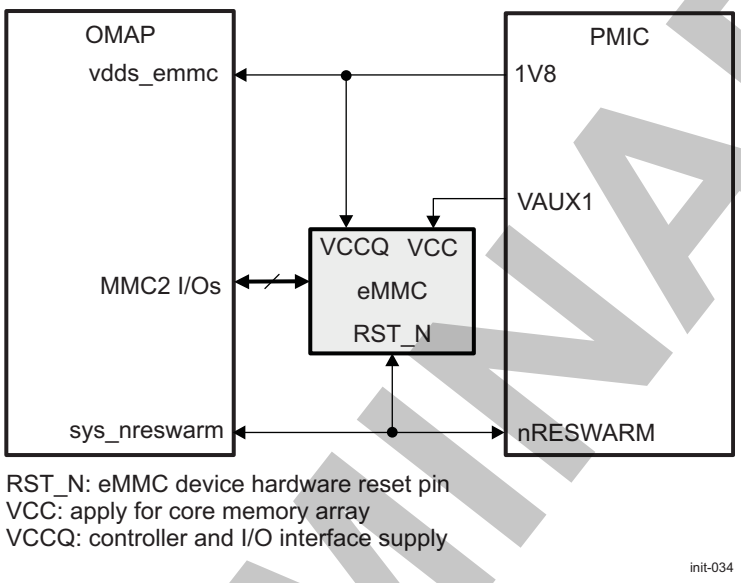
28.3.7.6.1.2 eMMC Memory Connection

An eMMC device typically requires two supplies: one for the core memory array (VCC) and one for the device interface I/Os and controller (typical VCCQ = 1.8 V). Both memory device supply pins can possibly be merged into one, thus requiring only one power supply.

Figure 28-28 shows an example of the system connection between the PMIC, memory device, and OMAP device.

Figure 28-28. eMMC Connection



NOTE: For correct handling of eMMC boot partitions when using alternative boot operation mode, it is recommended to tie the eMMC RST_N signal to the signal indicating a platform warm reset (nRESWARM).

The ROM code performs the necessary I/O pin muxing configuration to route the MMC2 I/O signals on the eMMC pads depending on the selected SYSBOOT configuration.

28.3.7.6.2 SD Cards

The ROM code supports booting from SD cards under the following conditions:

- SD cards compliant with *SD Specifications Part 1 Physical Layer Specification Version 4.00*and the *SD Specifications Part 2 File System Specification Version 3.00* from the SD Association. These include low- (SDSC) and high-capacity (SDHC) cards.
- SD card connected to SDCARD pads interface (OMAP MMC1 controller I/Os). Only one card is allowed to be connected to the bus.
- 3-V VCC power supply
- Initial 1-bit MMC mode, optional 4-bit mode
- Clock frequency:
  - Identification mode: 400 kHz
  - Data transfer mode: Up to 10 MHz (optionally up to 19.2 MHz)

28.3.7.6.2.1 System Conditions and Limitations

Even though the ROM Code identities SDXC cards, it does not handle its specificities such as exFAT support. It does neither support UHS-I nor UHS-II speed grades.

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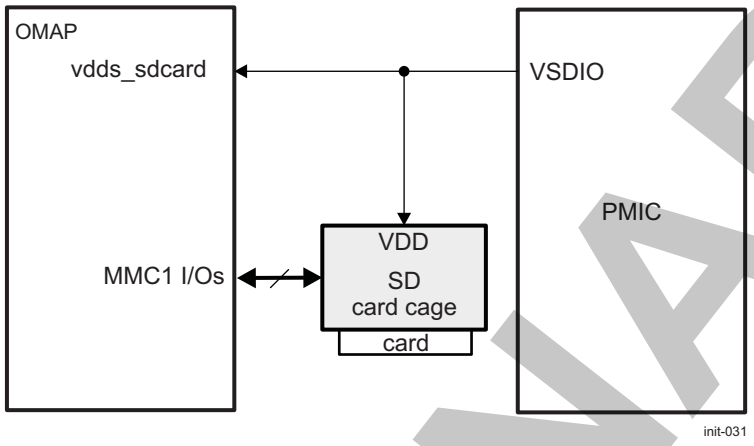
28.3.7.6.2.2 SD Card Connection

A, SD card can be connected to the SD card interface, typically through a card cage.

Figure 28-29 shows the typical connection between the power IC, the card, and the OMAP device.

Figure 28-29. MMC/SD Card Connection



NOTE: The ROM code does not handle the card detection feature on the card cage.

28.3.7.6.2.3 Booting Procedure

If the selected booting device is eMMC, then a first attempt to trigger alternative boot operation mode is tried. If the eMMC device replies within a fixed timeout, then the booting image is directly retrieved from one of the possible partitions specified in the local EXT_CSD.BOOT_PARTITION_ENABLE bit field for the eMMC device (this is referred to as the Raw(Boot) mode). Raw(Boot) mode improves the boot time by avoiding the regular eMMC/SD identification phase (usually done at low speed). When the booting image is retrieved, the ROM code continues the boot process.

If the time-out elapses, then the ROM code proceeds with normal identification. SD cards do not support Alternative Boot Operation mode, and therefore are always going through normal identification.

If normal identification succeeds, then it next determines whether the SD card or eMMC device contains a known file system. If the file system is known, then the booting image is extracted from the file system hierarchy. If a file system is not detected, then the Raw(UDA) mode is assumed.

Figure 28-30 is the high level flow chart of the eMMC and SD booting procedure.

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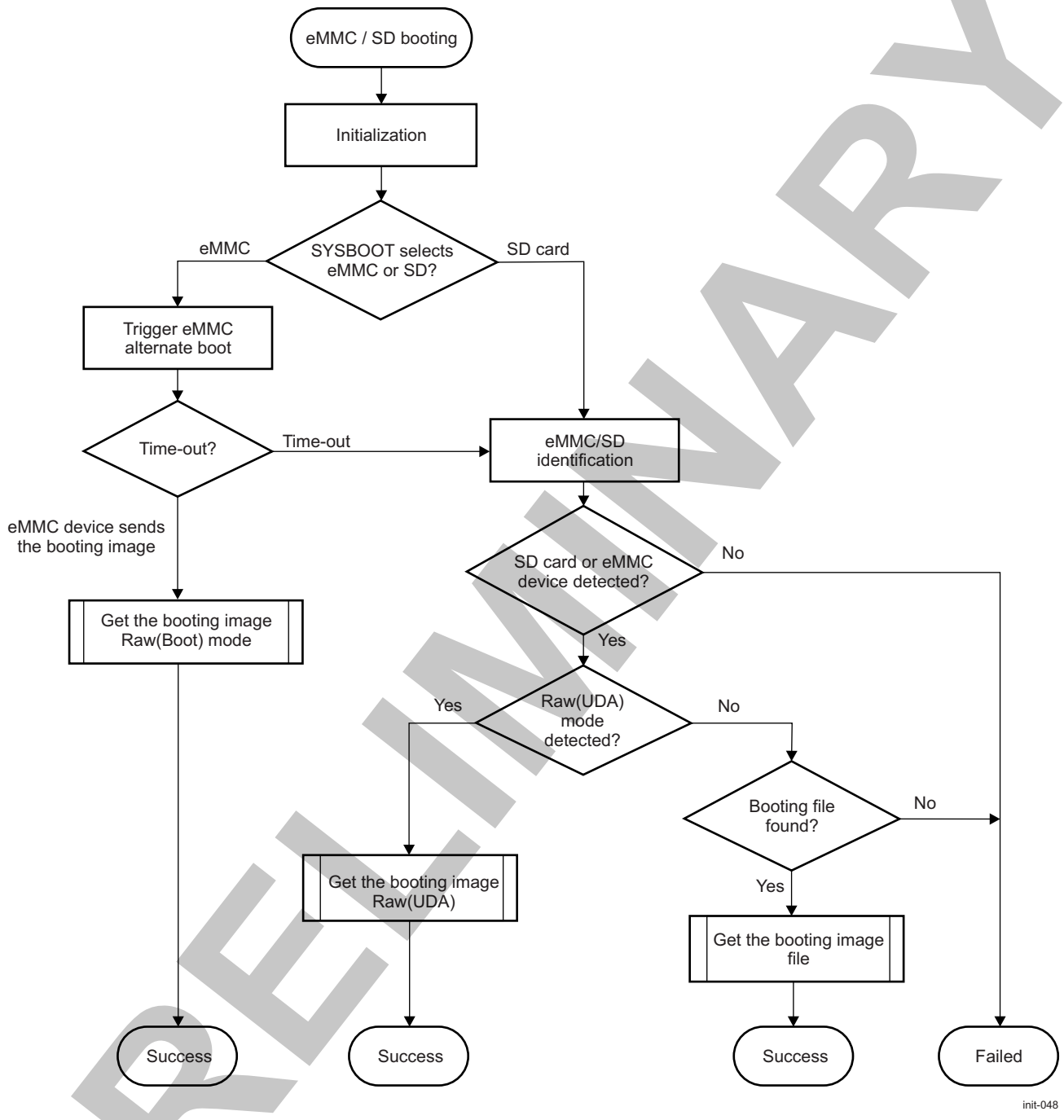
Figure 28-30. eMMC and SD Booting



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28.3.7.6.2.4 eMMC Partitions Handling in Alternative Boot Operation Mode

To trigger alternative boot operation mode, the ROM code sends a specific CMD0 + Argument 0xFFFF FFFA. Then, the ROM code waits up to 50 ms for the eMMC device to return a boot-acknowledge signal. If the time-out elapses, then the ROM code skips alternative boot operation mode. Booting from eMMC partitions can be done in 8-bit mode at 48 MHz / DDR. This configuration is static and cannot be changed.

28.3.7.6.2.4.1 eMMC Devices Preflashing

For correct handling of eMMC partitions in alternative boot operation mode, it is necessary to prepare the eMMC device at flashing time with the following settings applied to the device EXT_CSD register:

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- The BOOT_ACK and BOOT_PARTITION_ENABLE fields must be updated accordingly (EXT_CSD[179], bit 6 and bits [5:3], respectively) to activate the boot acknowledge signal and select the partition from which to boot. There are several boot options selectable in the BOOT_PARTITION_ENABLE bit field, as follows:
  - Booting from boot partition 1 (BP1)
  - Booting from boot partition 2 (BP2)
  - Booting from User Area

  For more details, see the eMMC Standard documentation.
- RST_N must be enabled for correct handling of the warm reset cases (EXT_CSD[162] bits [1:0] = 0x1).
- The BOOT_BUS_WIDTH fields (EXT_CSD[177]) must be updated properly based on OMAP alternate boot operation: 8-bit / 48 MHz / DDR mode.
- Optionally the BOOT_CONFIG_PROT (EXT_CSD[178]) may be updated for altering access permissions to the selected partitions.

NOTE: Although an alternate boot from user area is possible, alternate booting from BP1 or BP2 is recommended.

NOTE: It is possible to permanently or temporarily lock the boot configuration through the use of the BOOT_CONFIG_PROT register. For more details, see the eMMC Standard documentation.

NOTE:

- It is highly recommended to refer to the eMMC Standard for details on EXT_CSD handling.
- The EXT_CSD is updated by using a SWITCH command as detailed in the eMMC standard.
- The mentioned EXT_CSD fields are retained after a power cycle so only one “flashing” phase is required

28.3.7.6.2.4.2 eMMC Device State After ROM Code Execution

If alternative boot operation mode is successful, and the booting image is properly retrieved, then the eMMC device state remains in the BOOT state even after the execution has passed to the initial software. The initial software must bring the device out of the BOOT state.

28.3.7.6.2.4.3 Consideration on OMAP Global Warm Reset

Once the system has booted and upon triggering a warm reset at OMAP level (it can be triggered by the warm-reset push button, a timer, watchdog, etc.), it is important that the eMMC device is properly brought to its PRE-IDLE state so that the next Alternative Boot operation succeeds. This is ensured by the RST_N pin to be connected to OMAP sys_nreswarm ball and eMMC device nRESWARM pin. Not doing so would make the boot procedure fail after a warm reset.

28.3.7.6.2.4.4 Booting Image Size

In Raw(Boot) mode, the size of the booting image is determined after the first sector read access. In case of GP device, the boot image size is contained within the GP header. This ensures that the ROM code is only retrieving the necessary size of data and not the full contents of the partition.

28.3.7.6.2.4.5 Booting Image Layout

In Raw(Boot) mode only one copy of the booting image is maintained, as opposed to up to four copies in Raw(UDA) mode.

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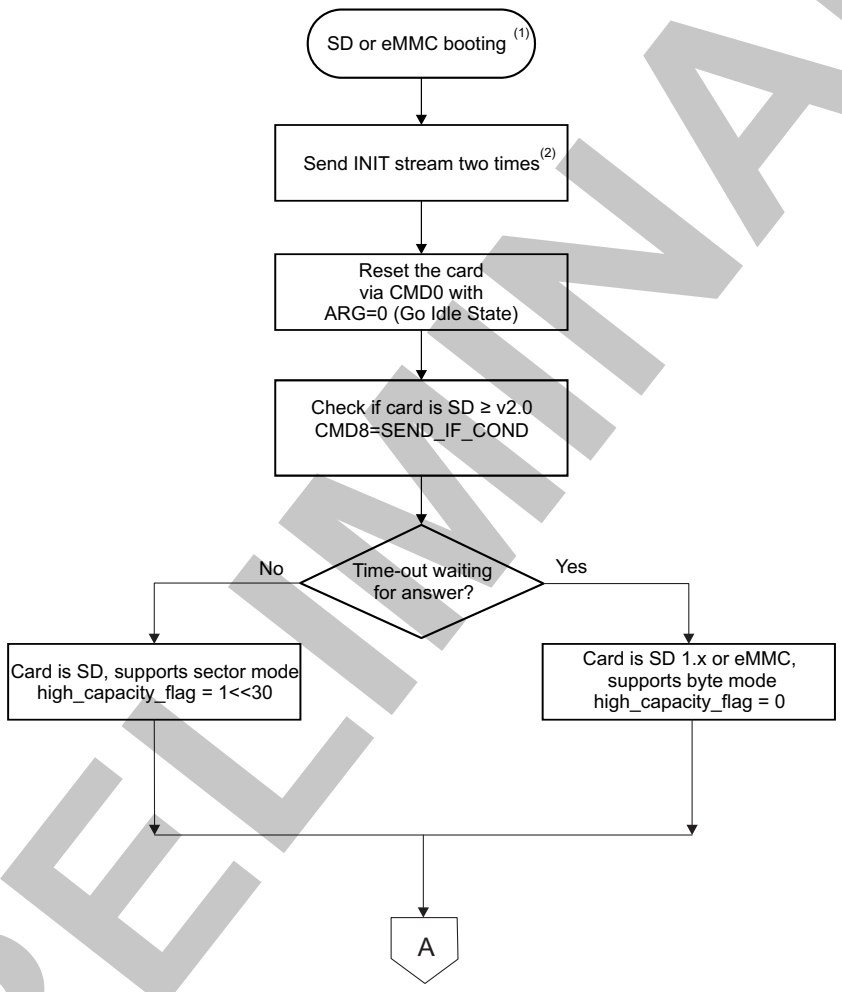
28.3.7.6.3 SD and eMMC Initialization and Detection

If the eMMC Alternate Boot operation fails in time-out, or the requested boot device is an SD card, the ROM code initializes the memory device or card connected on the eMMC and SD card interface using 1.8 V for eMMC and standard high-voltage range (3.0 V) for SD card I/Os. If neither a card nor memory device is detected, the ROM code moves to the next booting device. The standard identification process and relative card address (RCA) assignment are performed. The ROM code assumes that only one memory or card is connected on the bus. This is done using the CMD line common to the SD and eMMC memory devices. The eMMC and SD standards describe this phase as the initialization phase.

Figure 28-31 shows the eMMC and SD detection procedure.

Figure 28-31. SD and eMMC Detection Procedure



Note 1: MMC bus clk = 160 kHz

Note 2: MMC bus clk = 400 kHz

Note3: VHS / test pattern are specific to SD standard in this state.
eMMC CMD8 (=SEND_EXT_CSD) is NOT relevant in this state and this is the way to discriminate the SD v eMMC card

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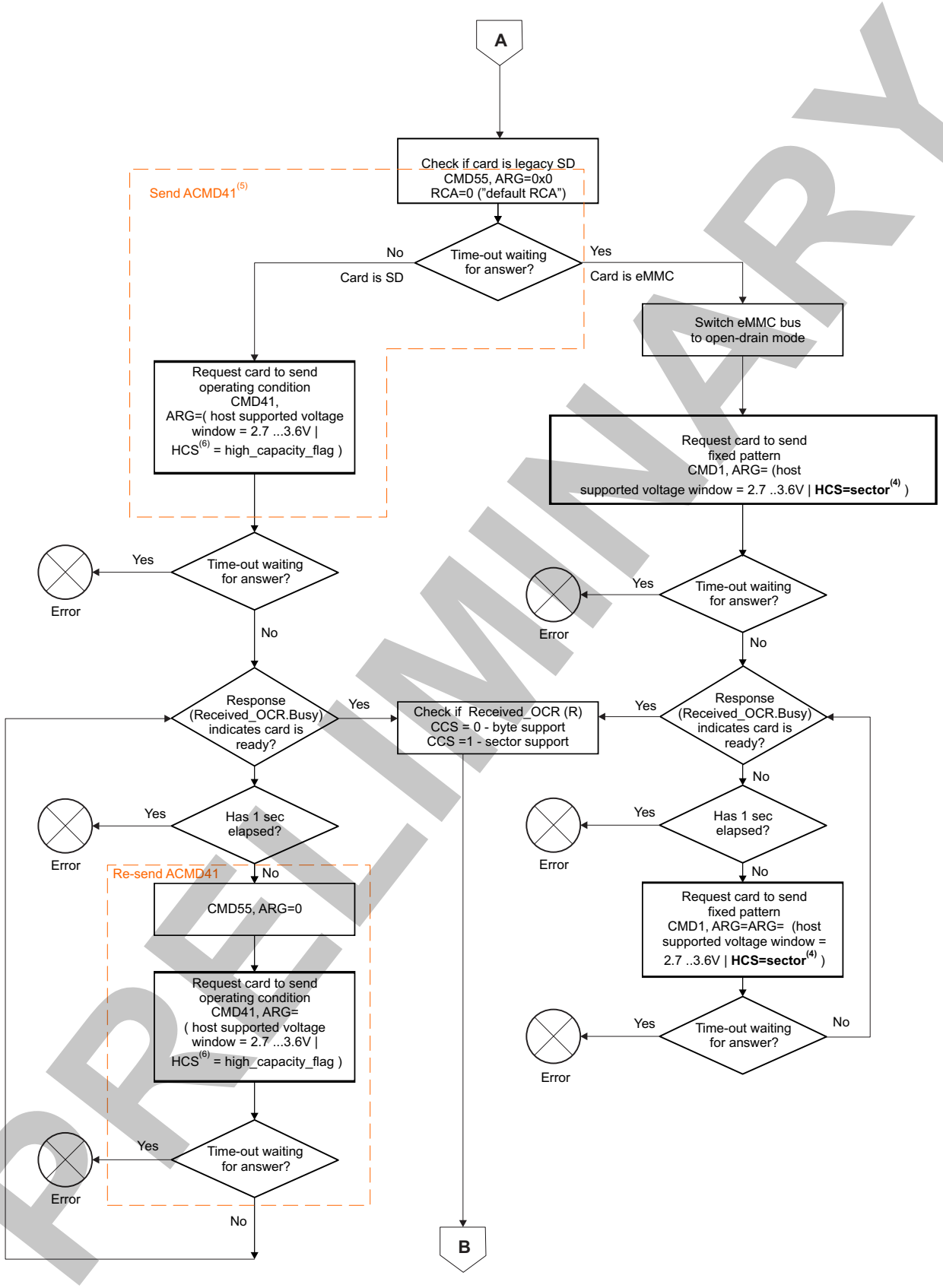

Note 4: Host indicates it is capable of sector addressing
Note 5: Refered to as the first ACMD41 that starts initialization in SD standard. Subsequent ACMD41 provide same argument
Note 6 : Host sets hcs per response from CMD8 as described in SD standard

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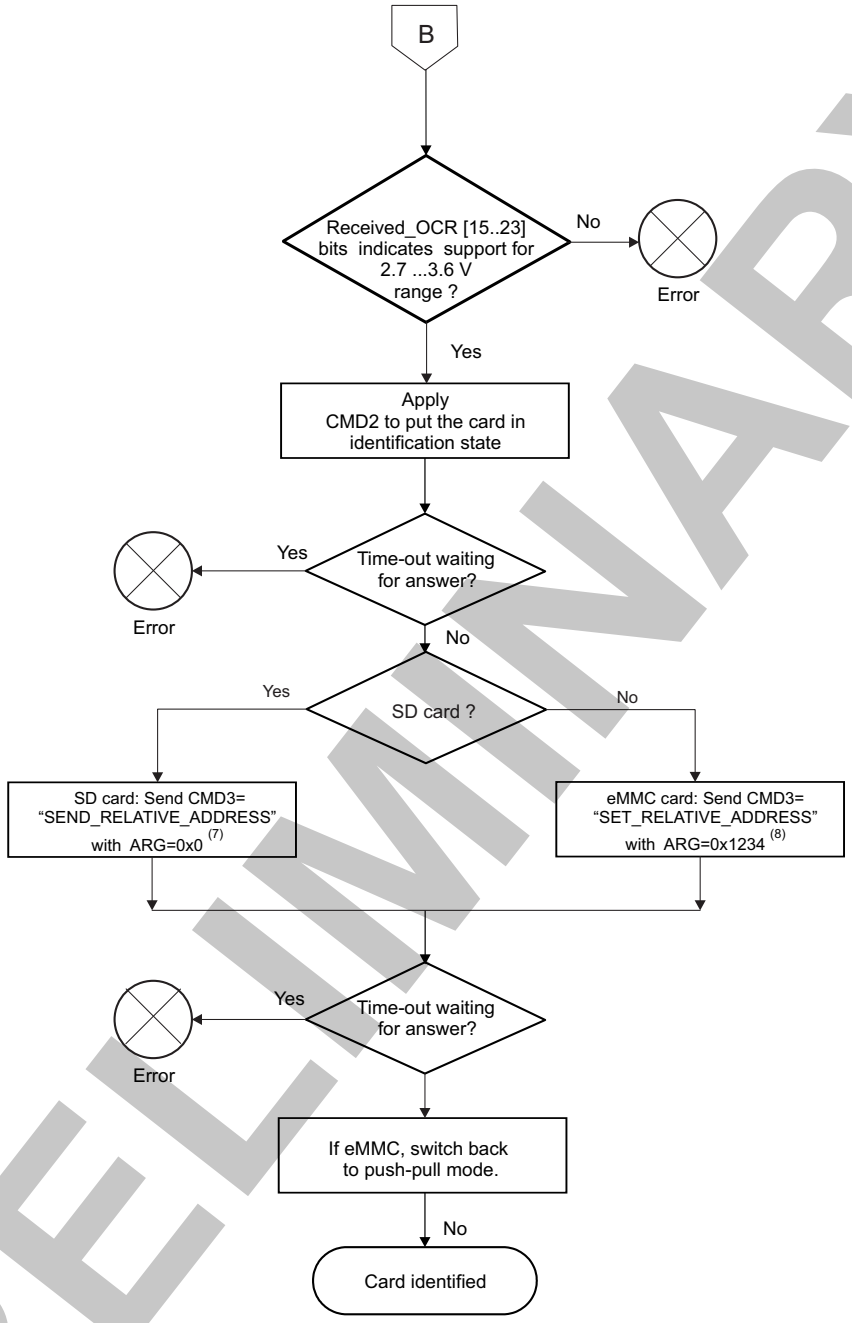

Note 7 : Card sends back a new RCA value that ROM Code keeps internally
Note 8: Card stores the new RCA value provided by the ROM Code.

init-026c

28.3.7.6.4 Read Sector Procedure

The contents of an eMMC or SD card may be formatted as raw binary (referred to as Raw(UDA) or within a FAT file system. The ROM Code reads out sectors from raw image or the booting file within the file system and boots from it.

- **Raw mode**

  In Raw(UDA) mode, an image can be at one of the four consecutive locations in the main area: offset 0x0 (0 KiB)/0x20000 (128 KiB)/0x40000 (256 KiB)/0x60000 (384 KiB). For this reason, the size of a

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booting image must not exceed 128 KiB. However, a device with an image greater than 128 KiB can be flash starting at one of the aforementioned locations. Therefore, the ROM code does not check the image size. The only drawback is that the image crosses the subsequent image boundary. Raw mode is detected by reading sectors 0, 256, 512, and 768. The content of these sectors is verified for the presence of a TOC structure. For a GP device, a GP header must be located at the beginning of the booting image, as described in Section 28.3.8.2, *Configuration Header*. Image data is read directly from continuous sectors of a card. If raw mode is not detected, file system mode is assumed.

- File system handling

  The read sector procedure uses the standard SD/eMMC read data procedure. The sector address is generated based on the booting memory file map collected during initialization. Thus, the ROM code can freely address sectors in the booting file space.

28.3.7.6.5 File System Handling

The eMMC / SD cards can hold a file system that the ROM code reads. The image used by the booting procedure is taken from a booting file named MLO. This file must be in the root directory on an ***active*** primary partition of type FAT12/16 or FAT32.

An eMMC/SD card can be configured as floppy-like or hard-drive-like:

- When acting like a floppy, the content of the card is a single FAT12/16/32 file system without an MBR holding a partition table.
- When acting like a hard drive, an MBR is present in the first sector of the card. This MBR holds a table of partitions, one of which must be FAT12/16/32, primary, and active.

According to the *MultiMediaCard FAT16 File System Specification* from the MMCA Technical Committee, the card must always hold an MBR, except when using a floppy-like file system. However, depending on the operating system used, the eMMC / SD card is formatted with or without partitions (using an MBR). The ROM code supports both types: floppy-like or hard-drive-like. The ROM code retrieves a map of the booting file from the FAT. The booting file map is a collection of all FAT entries related to the booting file (a FAT entry points to a cluster holding part of the file). The booting procedure uses this map to access any 512-byte sector in the booting file without involving the ROM code FAT module. Figure 28-32 shows the complete process.

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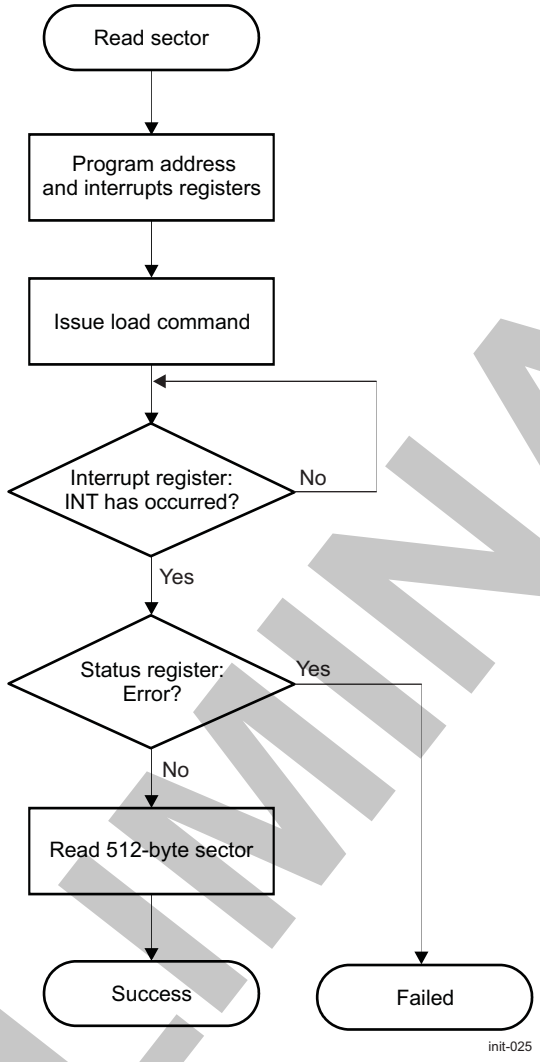
Figure 28-32. SD/MMC Get Booting File



28.3.7.6.5.1 MBR and FAT File System

This paragraph describes functions used by the ROM code to recognize whether an MBR with a FAT is used. It is not intended to fully describe the MBR and the FAT file system detection and reading procedure. The ROM code can detect FAT12/16/32 allocation table types. It cannot boot on devices with NTFS or Linux® FS partitions. Some memory devices that support file systems can be formatted with or without MBR; therefore, the first task of the ROM code is to detect whether the device is holding an MBR in the first sector.

The MBR is the first sector of a memory device. It consists of executable code, four partition entries, and one signature. The aim of such a structure is to divide the hard disk in partitions used primarily to boot different systems (for instance, Microsoft Windows®). Table 28-40 describes this structure, and Table 28-41 describes the partition table entry.

Table 28-40. Master Boot Record Structure

Offset	Length (Bytes)	Entry Description
0000h	446	Optional code
01BEh	16	Partition table entry
01CEh	16	Partition table entry
01DEh	16	Partition table entry

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Table 28-40. Master Boot Record Structure (continued)

Offset	Length (Bytes)	Entry Description
01EEh	16	Partition table entry
01FEh	2	Signature (0xAA55)

Table 28-41. Partition Table Entry

Offset	Length (Bytes)	Entry Description	Value
0000h	1	Partition state	00h: Inactive 80h: Active
0001h	1	Partition start head	Hs
0002h	2	Partition start cylinder and sector	Cs[7:0] – Cs[9:8] – Ss[5:0]
0004h	1	Partition type	01h: FAT12 04h, 06h, 0Eh: FAT16 0Bh, 0Ch, 0Fh: FAT32
0005h	1	Partition end head	He
0006h	2	Partition end cylinder and sector	Ce[7:0]–Ce[9:8]–Se[5:0]
0008h	4	First sector position relative to the beginning of media	LBAs = Cs.H.S + Hs.S + Ss – 1
000Ch	4	Number of sectors in partition	LBAe = Ce.H.S + He.S + Se – 1 Nb s = LBAe – LBAs + 1

SD/eMMC booting consists of the following steps:

1. Detection of MBR

   The ROM code first checks whether the MBR signature is present, and then it searches an active FAT12/16/32 partition in all four MBR partition entries, based on the Type field. If the MBR entries are not valid, or if no usable partition is found, the ROM code returns to the booting procedure with FAIL. The extended partitions are not checked; the booting file must reside in a primary partition. Each partition entry is checked to determine the following:

   (a) If the partition type is set to 00h, all fields in the entry must be 00h.

   (b) The partition is within physical boundaries (that is, the partition is inside and it fits the total physical sectors).

   See Figure 28-33 for more information about MBR detection.

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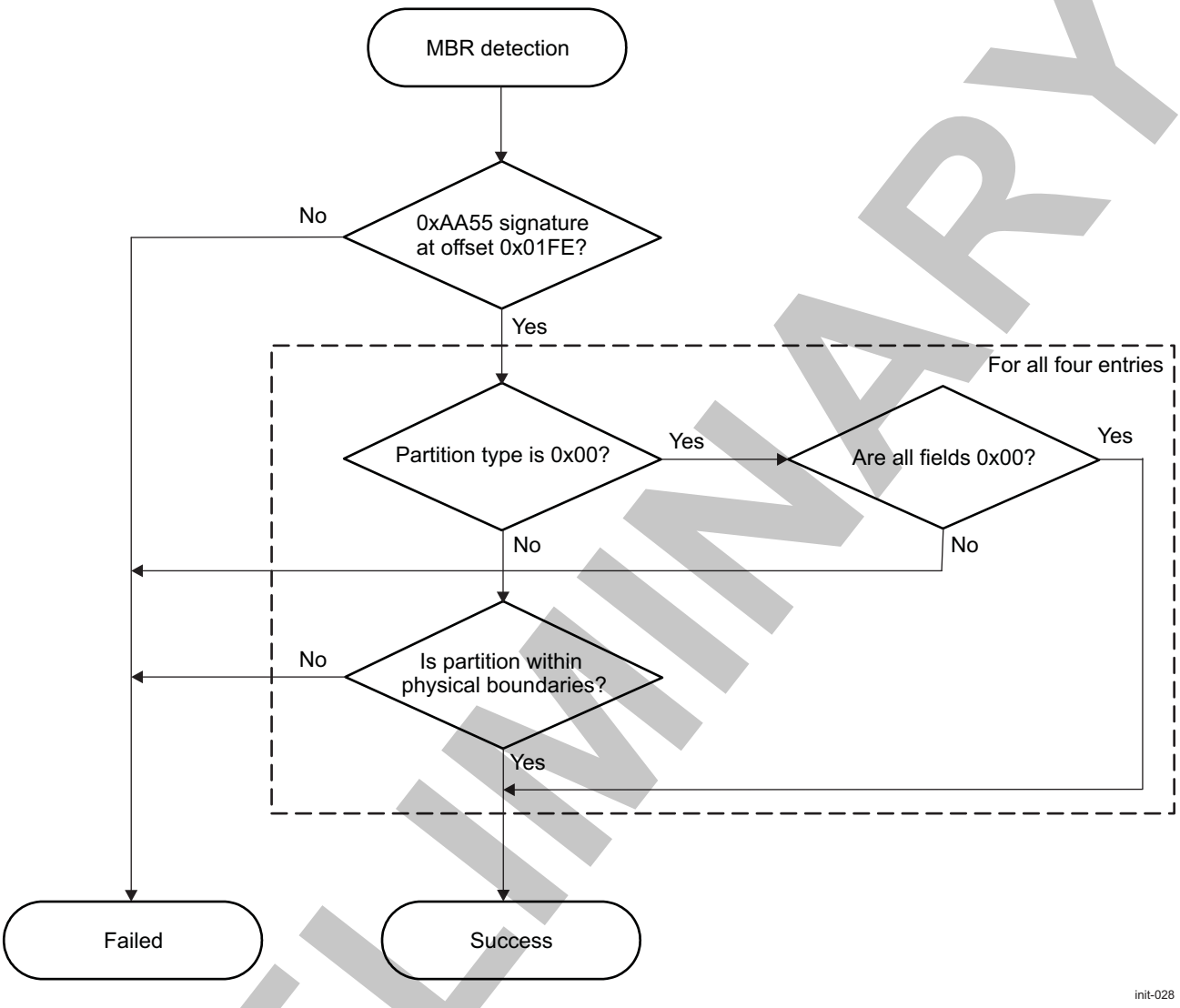
Figure 28-33. MBR Detection Procedure



2. Get the MBR partition.

   Once identified, the ROM code gets the partition using the procedure described in Figure 28-33. The partition type is checked to be FAT12/16 or FAT32. Its state must be 00h (inactive) or 80h (active). The ROM code returns with FAIL if no active primary FAT12/16/32 is found, or the test fails if there is more than one active partition. If an active partition is found, its first sector is read and used later. If no MBR is present (in case of a floppy-like system), the first sector of the device is read and used later. The read sector is checked to be a valid FAT12/16 or FAT32 partition. If this fails, the ROM code returns with FAIL if another partition type is used (for instance, Linux FS) or if the partition is not valid.

   The FAT file system consists of several parts:

   - Boot sector, which holds the BIOS parameter block (BPB). Not all are used by the ROM code.
   - FAT, which describes the use of each cluster of the partition
   - Data area, which holds the files, directories, and root directory (for FAT12/16, the root directory has a specific fixed location)

   To check whether a sector holds a valid FAT12/16/32 partition, many fields of the boot sector (used by all FAT types) that require specific values are checked. Figure 28-34 shows more about getting the partition.

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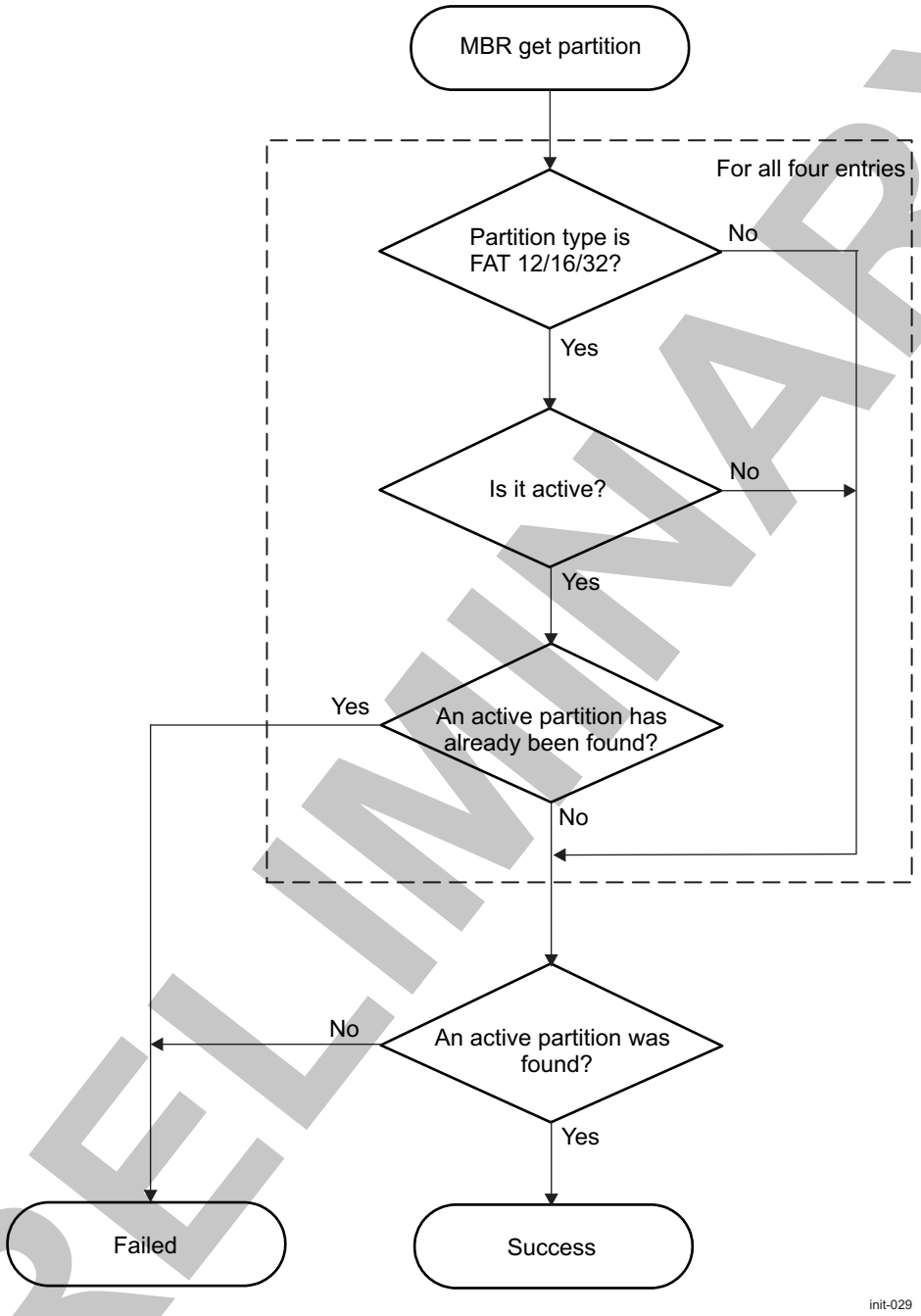
Figure 28-34. MBR, Get Partition



3. Find the booting file.

   When a partition is found, the root directory entries are searched for a booting file named MLO in the root directory of the FAT12/16/32 file system. The file is not searched in any other location. For a FAT12/16 file system, the root directory has a fixed location, which is cluster 0. For a FAT32 file system, its cluster location is given by BPB_RootClus. The formula to find the sector number (relative to device sector 0, not partition sector 0) of a cluster is given by the following equation:

$$Cluster_{sector} = BPB\_HiddSec + BPB\_RsvdSecCnt + BPB\_NumFATs \cdot BPB\_FATSz + Cluster \cdot BPB\_SecPerCLus$$

init-E001

NOTE: BPB_FATSz is BPB_FATSz16 for FAT12/16, or BPB_FATSz32 for FAT32.

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NOTE: The BPB_HiddSec field can contain 0, even though the FAT file system is somewhere other than on sector 0 (floppy-like). The ROM code uses the partition offset taken from the MBR instead of this field, which can be wrong. If no MBR is found (floppy-like), the value 0 is used.

Each entry in the root directory is 32 bytes and holds information about the file (the filename, date of creation, rights, cluster location, and so forth). See Table 28-42.

Table 28-42. FAT Directory Entry

Offset	Length (Bytes)	Name	Description
0000h	11	DIR_Name	Short Name (8 + 3)
000Bh	1	DIR_Attr	File attributes: 01h – ATTR_READ_ONLY 02h – ATTR_HIDDEN 04h – ATTR_SYSTEM 08h – ATTR_VOLUME_ID 10h – ATTR_DIRECTORY 20h – ATTR_ARCHIVE 0Fh – ATTR_LONG_NAME
000Ch	1	DIR_NTRes	Reserved. Set to 00h.
000Dh	1	DIR_CrtTimeTenth	Millisecond stamp at file creation
000Eh	2	DIR_CrtTime	Time file was created.
0010h	2	DIR_CrtDate	Date file was created.
0012h	2	DIR_LstAccDate	Last access date
0014h	2	DIR_FstClusHi	High word of the first cluster number of this entry
0016h	2	DIR_WrtTime	Time of last write
0018h	2	DIR_WrtDate	Date of last write
001Ah	2	DIR_FstClusLo	Low word of the first cluster number of this entry
001Ch	4	DIR_FileSize	File size in bytes

The ROM code checks each entry in the root directory until either the booting file is found or the entry is empty (first byte is 00h), or when the end of the root directory is reached. Entries with the ATTR_LONG_NAME attribute (LFN) and first byte at E5h (erased file) are ignored. When found, the first cluster offset of the file is read from the DIR_FstClusHi/DIR_FstClusLo fields. There is a slight difference between FAT12/16 and FAT32 when handling the root directory. On FAT12/16, this directory has a fixed location (see Table 28-42) and length fixed by BPB_RootEntCnt, which is the total of 32-byte entries. Therefore, handling this directory is straightforward. On FAT32, the root directory is like a standard file. The FAT must be used to retrieve each sector of the directory. Step 4 describes the way in which the FAT is handled.

4. Buffer FAT entries in the FAT buffer.

   When the booting file is found, the ROM code reads the FAT and buffers the singly-linked chain of clusters in the FAT buffer that is used during boot to access the booting file directly, sector by sector. For FAT12/16 and for FAT32, multiple copies of the FAT exist (ROM code supports only two copies), after the boot sector.

$$FATn_{sector} = BPB\_HiddSec + BPB\_RsvdSecCnt + BP\_FatSz \cdot n$$

init-E002

   The size of the FAT buffer is given by BPB_FATSz16 or BPB_FATSz32. The ROM code checks each copy of the FAT if the values are identical. If the values are different, the ROM code uses the value from the last FAT copy. With the FAT32 file system, the copy system can be disabled according to a flag in BPB_ExtFlags[7]. If this flag is set, the FAT BPB_ExtFlags[3:0] bit field is used. In this case, no verification is made by the ROM code with other copies of FAT.

   The FAT is a simple array of values, each referring to a cluster in the data area. One entry of the array is 12, 16, or 32 bits, depending on the file system in use. The value in an entry defines whether the

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cluster is being used or not, and if another cluster must be considered. This creates a singly-linked chain of clusters defining the file. Table 28-43 describes the meaning of an entry.

NOTE: For compatibility, cluster 0 and cluster 1 are not used for files, and these entries must contain:

- FF8h and FFFh (for FAT12)
- FFF8h and FFFFh (for FAT16)
- 0FFFFFF8h and 0FFFFFFFh (for FAT32)

Table 28-43. FAT Entry Description

FAT12	FAT16	FAT32	Description
000h	0000h	00000000h	Free cluster
001h	0001h	00000001h	Reserved cluster
002h–FEFh	0002h–FFEFh	00000002h–0FFFFFEFh	Used cluster; value points to next cluster
FF0h–FF6h	FFF0h–FFF6h	0FFFFFF0h–0FFFFFF6h	Reserved values
FF7h	FFF7h	0FFFFFF7h	Bad cluster
FF8h–FFFh	FFF8h–FFFFh	0FFFFFF8h–0FFFFFFFh	Last cluster in file

NOTE: FAT32 uses only bits [27:0]; the upper 4 bits are usually 0 and must remain untouched.

When accessing the root directory for FAT32, the ROM code starts from the root directory cluster entry and follows the linked chain to retrieve the clusters.

When the booting file has been found, the ROM code buffers each FAT entry corresponding to the file in a sector way. This means each cluster is translated to one or several sectors, depending on how many sectors are in a cluster (BPB_SecPerClus). This buffer is used later by the booting procedure to access the file.

28.3.7.7 SATA Device Boot Operation

The SATA is a host interface dedicated for mass storage memory devices. SATA aims to connect SATA disk drive compliant SSD (SATA solid state drive) or HDD (hard disk drive) for mass storage use case only.

The mass storage device (SSD or HDD) is intended to be connected through SATA standard connector (in case of HDD) or directly soldered on the board (in case of SSD). In the latter case, the SATA mass-storage device is actually permanently attached to the OMAP device.

The OMAP embedded SATA host controller has a single port (P0) implementation, and one internal electrical transceiver (SATA_PHY). For more information on the device-embedded SATA (SATA AHCI core and wrapper), see Section 23.12, *SATA Controller*. For more details on SATA subsystem integrated SATA PHY transceiver components, see Section 27.1, *SATA PHY Subsystem*. A system integration block diagram is provided in following section.

28.3.7.7.1 SATA Booting Overview

The device attached to the OMAP SATA for boot operation must meet the following requirements:

- It must be compliant with the *Serial ATA Standard* specification, rev. 2.6.
- It must support READ SECTOR(s) ATA command (code 0x20) as defined in the ATA / ATAPI - 7 specification.
- It must be connected directly to the OMAP SATA IOs – sata_tx / sata_ty, sata_rx / sata_ry (no port multiplier connected).

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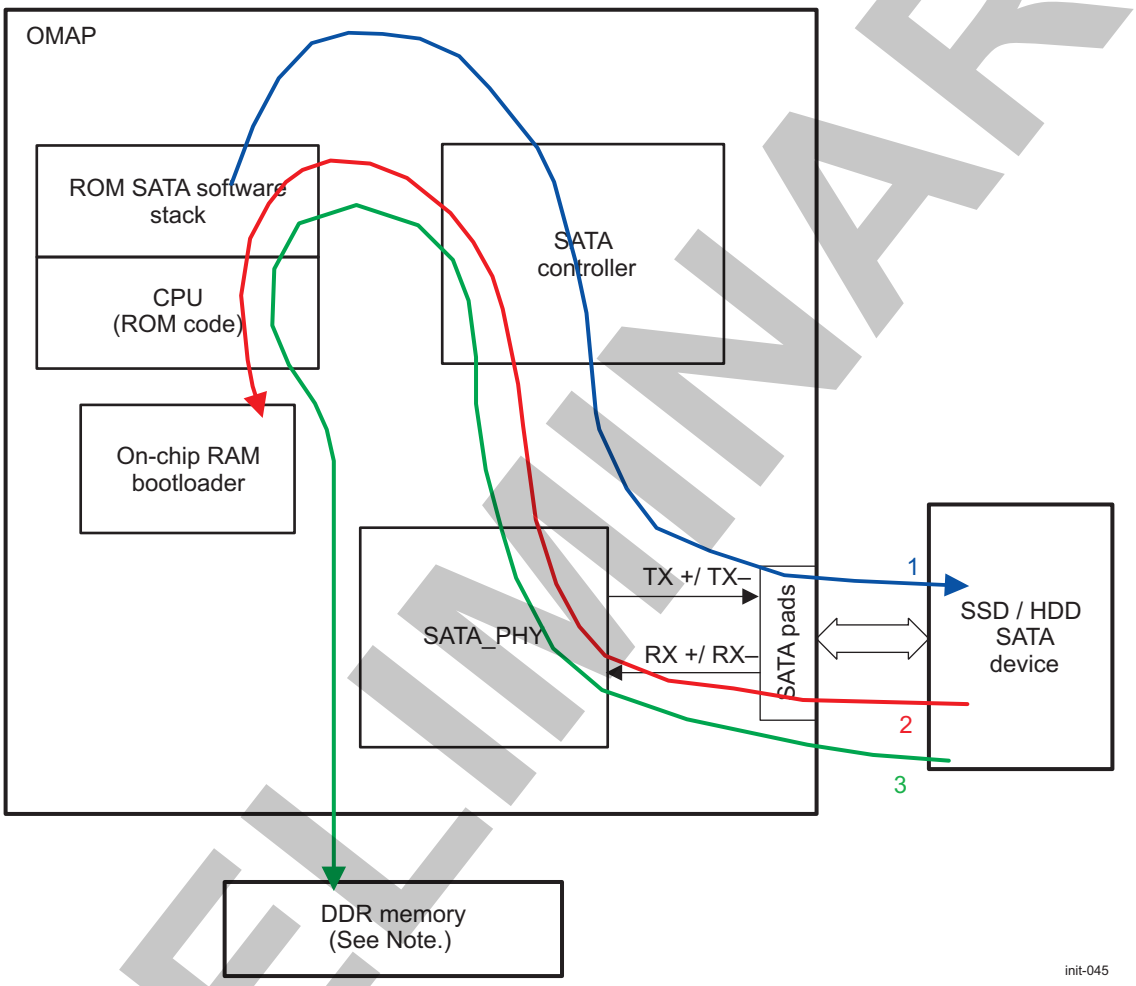
- It must have been already powered by the companion chip or external supply before start of the boot procedure.
- It must be taken in consideration for the device that maximum power on ready time allowed by ROM Code is 900ms. First COMRESET procedure targeting the attached device is triggered 300ms after OMAP SATA subsystem initialization by ROM Code.

Figure 28-35 highlights the booting of the platform from the SSD device.

Figure 28-35. Booting from a Permanently-Attached SSD Device



The OMAP booting from an attached SATA mass storage memory device is performed in the following steps:

1. At reset or power on, the OMAP device ROM code boots and checks for the SSD / HDD to be ready.
2. The SSD / HDD transfers the boot-loader to the internal RAM of device.
3. The OS in the SSD or HDD is downloaded into DDR memory and the platform is ready.

28.3.7.7.2 SATA Power-Up Initialization Sequence

Figure 28-36 shows all messages exchanges between power-on event up to when the platform is ready. The sequencing aims to depict the complete sequence without any specific connecting issues that may appear.

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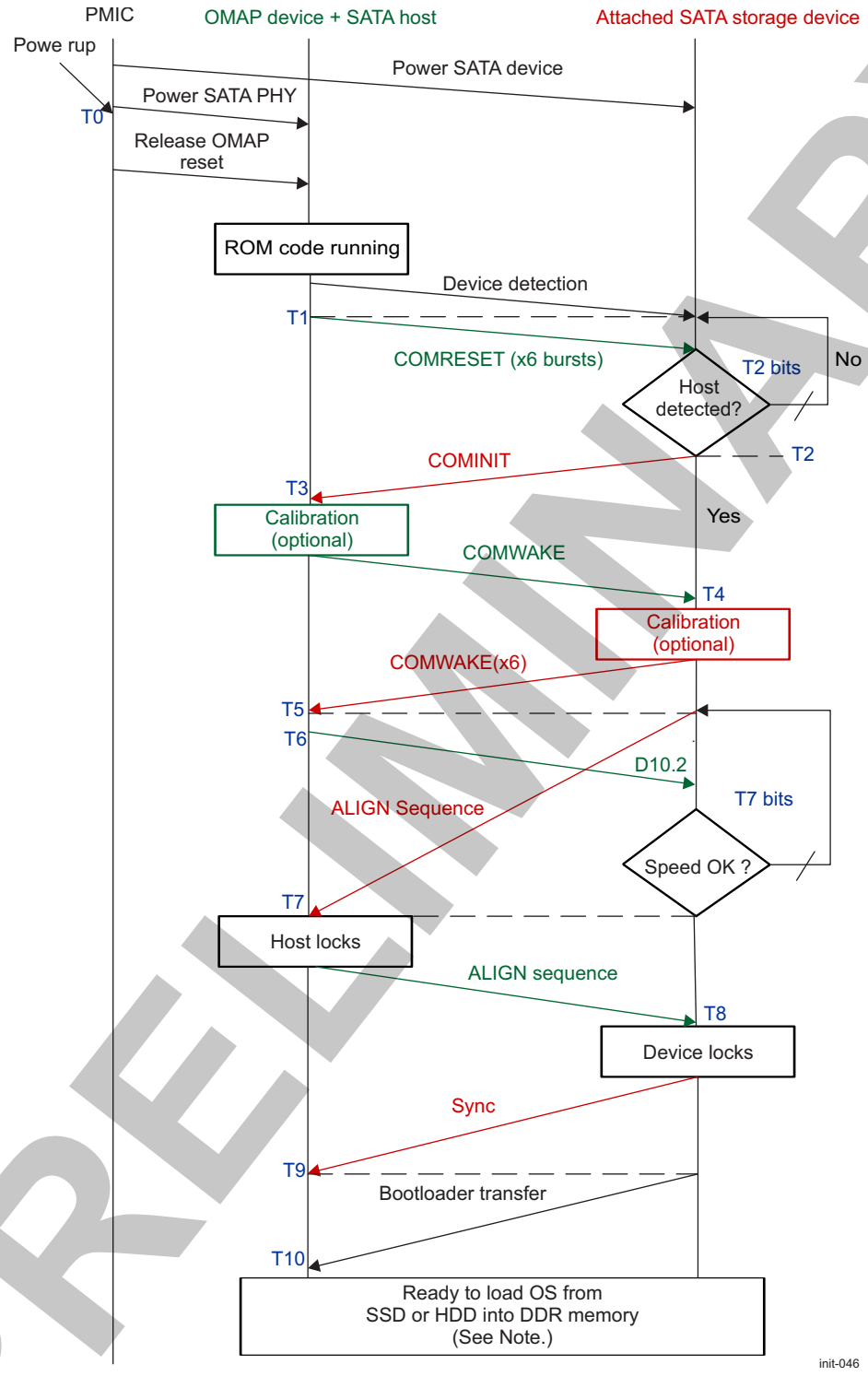
Figure 28-36. SATA Power-on Initialization Sequencing



The following time phases can be identified during booting from SATA interface:

- T0: the SATA_PHY is powered and OMAP reset is maintained until all Power-management IC companion powers are set.
- T1: the ROM code validates a SATA SSD device detection.
- Within the T1-T2 time interval: the SATA host issues a COMRESET sequence for a minimum of 6 bursts (and a multiple of 6) to force a hardware reset to the SATA peripheral device.

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- T2: As long as the attached SATA SSD device does not explicit reset request (COMINIT), the host issues COMRESET sequences
- Within the T2-T3 time interval, once the host release the COMRESET sequence (made of 6 bursts minimum), the device responds with a COMINIT to request a communication initialization (It requests a reset from the host).
- Within the T3-T4 time interval, the SATA host controller may calibrate at T3, but issues a COMWAKE sequence to the peripheral in order to inform the other part the wish to use the link.
- Within the T4-T5 time interval, the SSD device responds and may calibrate. The device response is made of 6 burst COMWAKE sequence.
- Within the T5-T6 time interval, SATA host controller shall start transmitting D10.2 characters no later than a defined moment.
- Within the T6-T7 time interval, when the OMAP host detects the COMWAKE from the device, it starts transmitting D10.2 character at its lowest speed.
- At the same time within T5-T7 time interval, continuous stream of device ALIGN sequence (following the 6 bursts COMWAKE sequence) starting at the device highest speed.
- T7: Without any SATA host's answer (D10.2 character), the device ALIGN sequence is repeated for as many slower speeds as are supported. When host receives ALIGN sequence, it locks.
- in case no proposed speeds are supported by the host, the device enters in error state.
- in case no ALIGNp sequence is received by the host within a defined time gap after detecting the release of the device COMWAKE, the host restarts the power on sequence indefinitely until stop by user intervention.
- Within the T7-T8 time interval, as soon as the OMAP device SATA host locks, it issues an ALIGN sequence to the attached SATA SSD device that also locks
- Within the T8-T9 time interval, the SATA peripheral device sends a SYNC primitive to inform the communication link is established.
- Within the T9-T10 time interval, once the link has been set successfully, the boot loader is transferred from the SATA peripheral device to OMAP internal on-chip RAM

After passing through all above described phases, the OMAP is ready to load OS source from SSD to the device DDR RAM (LPDDR2 or DDR3).

28.3.7.7.3 System Conditions and Limitations for SATA Boot

The following system conditions and limitations are defined by ROM Code implementation:

- The ROM Code sets Gen2 speed (3 Gbps) for a SATA boot operation.
- The ROM Code expects that the SATA I/Os are connected to OMAP SATA subsystem at system reset (i.e. a permanently attached boot device).
- The ROM Code expects that the SATA device is powered externally and supplies are set and stable upon entering the booting procedure. The ROM Code does not perform any software action to the companion device with respect to powering the SATA device.
- The ROM Code allows the SATA device 300ms power on ready time before starting the device detection. In case that the detection fails, the ROM Code retries 3 times with 200ms delay before returning and reporting a SATA boot failure.
- The ROM Code does not handle or enable advanced SATA power modes (slumber and partial).

The ROM Code initializes SATA subsystem after SATA boot is started, as defined in this chapter. The ROM Code does not close SATA connection after it was initialized following procedure defined in Section 28.3.4.3, *Booting Device List Setup*.

28.3.7.7.4 SATA Read Sector Procedure in FAT Mode

The booting medium may hold a FAT file system which the ROM Code is able to read and process. The image used by the booting procedure is taken from a specific booting file named "HLO". This file has to be located in the root directory on an active primary partition of FAT12 / 16 or FAT32 type.

A SATA drive can be configured either as floppy-like or hard-drive-like.

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- When acting as floppy-like, the content of the card is a single file system without any **Master Boot Record (MBR)** holding a partition table.
- When acting as hard-drive-like, a **MBR** is present in the first sector of the card. This **MBR** holds a table of partitions, one of which must be **FAT 12/ 16 / 32, primary and active**.

Refer to the Section 28.3.7.6.5.1, *MBR and FAT File System*, for a more detailed description of FAT file system support.

28.3.8 Image Format

28.3.8.1 Overview

An image has two major parts:

- An optional CH
- Software to execute

The CH can contain several parameters set by users to speed up booting. It is further described in Section 28.3.8.2, *Configuration Header*.

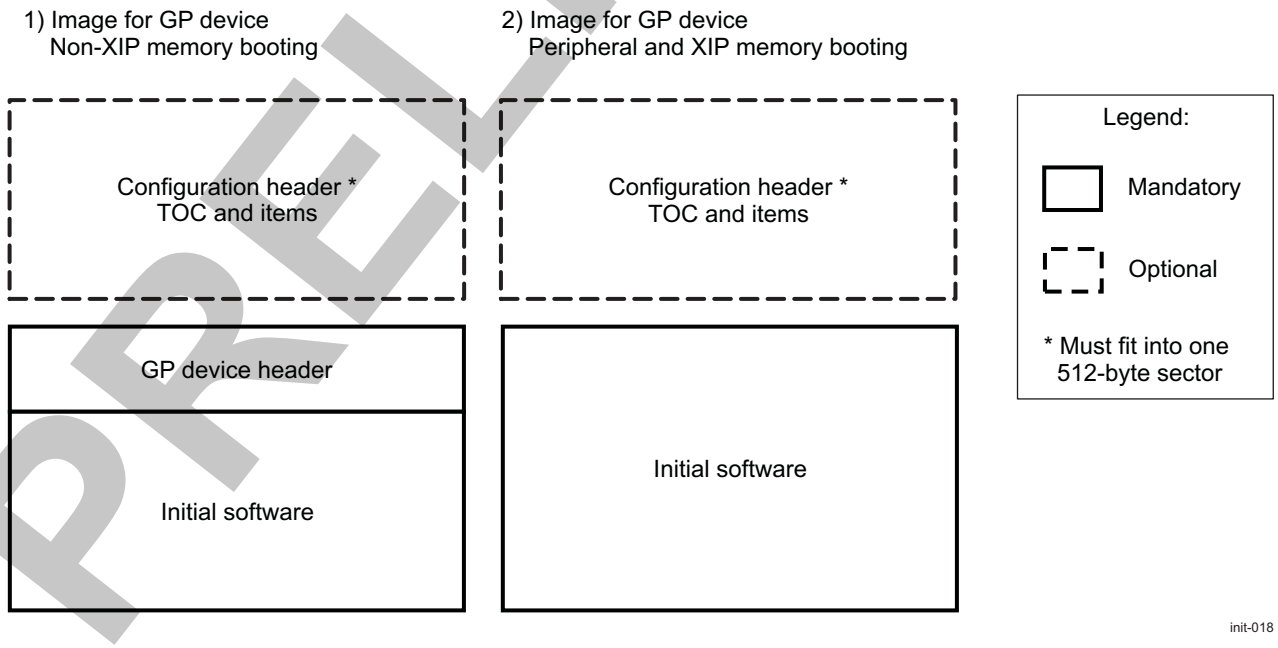
The second part contains the software that is loaded into the memory and executed.

Figure 28-37 is an overview of the boot image formats. There are two image types:

1. GP non-XIP memory booting: This image type is used for memories that require shadowing (for example, eMMC). A GP image for non-XIP memory may NOT contain a CH and start straight from the GP header. Next, there must be a small header (referred to as a GP header) that contains information about the size and the destination address.
2. When the memory device is of XIP type (for example, NOR), the GP header is not required, and the image can contain code for direct execution. Optionally, the first sector can contain a CH. The same image format is used for peripheral booting (where the code is transferred to internal RAM).

NOTE: A GP image for non-XIP memory may NOT contain a CH and start straight from the GP header.

Figure 28-37. Image Formats



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28.3.8.2 Configuration Header

The ROM code default settings (such as clock frequencies, EMIF, GPMC, or MMCHS interfaces) can be tuned by the user by using the CH.

The CH can contain the following parts:

- Settings: Various clock settings (mandatory)
- RAM: EMIF settings
- FLASH: Flash interface (GPMC) settings
- eMMC / SD: MMC2 / MMC1 interface settings

The beginning of the CH is a table of contents (TOC), which points to each item. This is described in Figure 28-38. Each TOC item is a simple structure described in Table 28-44. The complete CH (CH TOC and items) should fit in a 512-byte sector.

The ROM code identifies the presence of a CH by reading the first TOC item if it contains a known string (CHSETTINGS, CHRAM, etc.). Next, the TOC is identified and searched until a 0xFFFF FFFF offset is found. The CH is read and parameters are executed sequentially.

For the sake of simplicity, each field represents the content of a register to be modified. Only fields required for the configuration are used; fields for status, for instance, are not modified and therefore are not shown in the tables.

Figure 28-38. CH Format

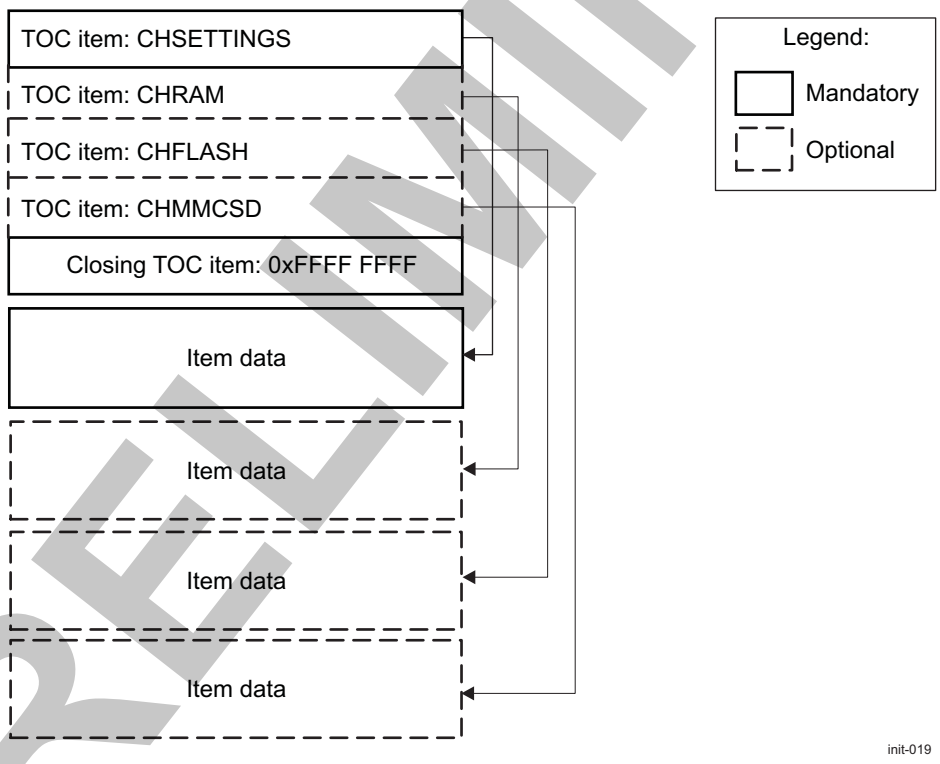

Table 28-44. CH TOC Item

Offset	Field	Size (Bytes)	Description
0x0000	Start	4	Offset from the start address of the TOC to the actual address of item contents
0x0004	Size	4	Size of item
0x0008	Reserved	4	Unused
0x000C	Reserved	4	Unused

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Table 28-44. CH TOC Item (continued)

Offset	Field	Size (Bytes)	Description
0x0010	Reserved	4	Unused
0x0014	Filename	12	12-character name of a item, including the zero termination character(\0)

The ROM Code recognizes sections pointed to by the TOC based on the filename as described in Table 28-45

- The 'X-LOADER', '2ND', 'MLO', 'ULO', or 'HLO' section contains the Initial Software
- Optionally, TOC may contain CH sections. The "CHSETTINGS" is a mandatory section of CH and is used to recognize CH presence.

Table 28-45. TOC Filenames

Filename	Item Type	Usage	Description
X-LOADER	Initial Software	XIP Memory Booting	"eXternal LOADER"
MLO	Initial Software	eMMC / SD Memory Booting	"Mmc LOader"
HLO	Initial Software	SATA Memory Booting	"Hdd LOader"
ULO	Initial Software	USB Peripheral Booting	"Usb LOader"
2ND	Initial Software	UART Peripheral Booting	"Secondary Loader"
CHSETTINGS	Configuration Header	Memory & Peripheral Booting	Configuration Header General Setting Item
CHRAM	Configuration Header	Memory & Peripheral Booting	Configuration Header EMIF Item
CHFLASH	Configuration Header	Memory & Peripheral Booting	Configuration Header GPMC Item
CHMMCSD	Configuration Header	Memory & Peripheral Booting	Configuration Header eMMC/SD Item

28.3.8.2.1 CHSETTINGS Item

The CHSETTINGS configuration header contains settings specific to the clock system. The ROM code configures the OMAP clocking to some default settings as described in Section 28.3.4.2, *Clocking Configuration*. The CH CHSETTINGS section contains a method to override the ROM code default clock settings.

Table 28-46 describes the fields. The clocking procedure and the clocking setting structure are described in Section 28.3.4.5, *Software Booting Configuration*.

Table 28-46. CHSETTINGS Item

Offset	Field	Description
0000h	Section key	Key used for item verification: C0C0C0C1h
0004h	Valid	Enables/disables the section: 00h: Disable Others: Enable
0005h	Version	Configuration header version 01h Others: Reserved
0006h	Reserved	
0008h	Clocking settings	Described in Table 28-14, *Software Booting Configuration Structure*, starting from the FLAGS field.

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28.3.8.2.2 CHRAM Item

The CHRAM configuration header contains settings specific to the SDRAM memory controller (EMIF). Table 28-47 describes the fields. The ROM code does not configure the EMIF by default, because it cannot assume any external SDRAM type. Therefore, if the ROM code is needed to configure the SDRAM access, the user must provide the appropriate timing details in the CHRAM structure. For more information, see Section 15.3.6, *EMIF Register Manual*, in Section 15.3, *EMIF Controller*.

NOTE: If the boot image contains an optional Configuration Header for EMIF configuration at boot time, I/O settings must be provided (in below listed CHRAM Item structure) to override the default Control Module reset values.

Table 28-47. CHRAM Item

Offset	Field	Size (Bytes)	Description
0000h	Section key	4	Key used for section verification: C0C0C0C2h.
0004h	Valid	1	Enables/disables the section: 00h: Disable Other: Enable
0005h	Reserved	3	Reserved
0008h	SdramConfig (EMIF1,2)	4	SDRAM configuration register (EMIF1,2.EMIF_SDRAM_CONFIG)
000Ch	SdramConfig2 (EMIF1,2)	4	SDRAM configuration2 register (EMIF1,2.EMIF_SDRAM_CONFIG_2)
0010h	SdramRefresh (EMIF1,2)	4	SDRAM Refresh control register (EMIF1,2.EMIF_SDRAM_REFRESH_CONTROL)
0014h	SdramRefreshShdw (EMIF1,2)	4	SDRAM Refresh Control Shadow Register (EMIF1,2.EMIF_SDRAM_REFRESH_CONTROL_SHADOW)
0018h	SdramTim1 (EMIF1,2)	4	SDRAM timing 1 register (EMIF1,2.EMIF_SDRAM_TIMING_1)
001Ch	SdramTim2 (EMIF1,2)	4	SDRAM timing 2 register (EMIF1,2.EMIF_SDRAM_TIMING_2)
0020h	SdramTim3 (EMIF1,2)	4	SDRAM timing 3 register (EMIF1,2.EMIF_SDRAM_TIMING_3)
0024h	SdramTim1Shdw (EMIF1,2)	4	SDRAM timing 1 shadow register (EMIF1,2.EMIF_SDRAM_TIMING_1_SHADOW)
0028h	SdramTim2Shdw (EMIF1,2)	4	SDRAM timing 2 shadow register (EMIF1,2.EMIF_SDRAM_TIMING_2_SHADOW)
002Ch	SdramTim3Shdw (EMIF1,2)	4	SDRAM timing 3 shadow register (EMIF1,2.EMIF_SDRAM_TIMING_3_SHADOW)
0030h	PwrMgtCtrl (EMIF1,2)	4	Power mgt control Register (EMIF1,2.EMIF_POWER_MANAGEMENT_CONTROL)
0034h	PwrMgtCtrlShdw (EMIF1,2)	4	Power mgt control Shadow Register (EMIF1,2.EMIF_POWER_MANAGEMENT_CONTROL_SHADOW)
0038h	DdrPhyCtrl1 (EMIF1,2)	4	DDR PHY Control 1 Register (EMIF1,2. EMIF_DDR_PHY_CONTROL_1)
003Ch	DdrPhyCtrl2 (EMIF1,2)	4	DDR PHY Control 2 Register (EMIF1,2. EMIF_DDR_PHY_CONTROL_2)
0040h	DdrPhyCtrl1Shdw (EMIF1,2)	4	DDR PHY Control 1 Shadow Register (EMIF1,2. EMIF_DDR_PHY_CONTROL_1_SHADOW)
0044h	ExtPhyCtrl [1..24] (EMIF1,2)	96	External PHY Control Registers
00A4h	ControlLpDdr2Ddr3ChX_0	4	LPDDR2: CONTROL_LPDDR2CH1_0 / CONTROL_LPDDR2CH1_1 DDR3: CONTROL_DDR3CH1_0 / CONTROL_DDR3CH2_0
00A8h	ControlDdrChX_0	4	CONTROL_DDRCH1_0 / CONTROL_DDRCH2_0
00ACh	ControlDdrChX_1	4	CONTROL_DDRCH1_1 / CONTROL_DDRCH2_1

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Table 28-47. CHRAM Item (continued)

Offset	Field	Size (Bytes)	Description
00B0h	EmifXSdramConfigExt	4	EMIF1_SDRAM_CONFIG_EXT / EMIF2_SDRAM_CONFIG_EXT
00B4h	Reserved	8	Reserved
00BCh	ModeReg1 (EMIF1,2)	1	MR1 mode register value (LPDDR2 only, reserved for DDR3)
00BDh	ModeReg2 (EMIF1,2)	1	MR2 mode register value (LPDDR2 only, reserved for DDR3)
00BEh	ModeReg3 (EMIF1,2)	1	MR3 mode register value (LPDDR2 only, reserved for DDR3)
00BFh	Reserved	1	Reserved
00C0h	CoreFreqConfigM2Div	1	CORE M2 divider value after PRCM Frequency update
00C4h	DMM LISA Map 0	4	DMM LISA section 0 mapping (for more information about the DMM module architecture, see Section 15.2, *Dynamic Memory Manager*, in Chapter 15, *Memory Subsystem*)
00C8h	Flags	4	Setting bits 0 to 3 requests ROM code to configure the appropriate channel/chip select: Bit[0]: Configure EMIF1 CS0 Bit[1]: Configure EMIF1 CS1 Bit[2]: Configure EMIF2 CS0 Bit[3]: Configure EMIF2 CS1 Bits[8:11] - EMIF temperature monitoring timeout 0x0: Temperature monitoring disabled 0x1: Timeout 1 second 0x2: Timeout 2 seconds 0x3: Timeout 3 seconds 0x5: Timeout 5 seconds 0xA: Timeout 10 seconds Bits[4:7] and Bits[12:31] - Reserved

NOTE:

- The ROM code supports different types of SDRAM memory, LPDDR2 or DDR3 memory (as set in the SDRAM configuration register and indicated e-fuse), which depend on the OMAP device package. For more details, see Section 1.1, *Overview*, in Chapter 1, *Introduction*.
- The same kind of SDRAM (same type, timings, and density) must be attached to both chip selects (CSs) of the same controller when requesting the configuration of both CSs for a given EMIF interface (for example, if bits 0 and 1 of the Flags field are set, it is assumed that both EMIF1 CSs are attached to the same kind of memory).

NOTE: It is mandatory that the same type of SDRAM memory (same type and timings) is attached to both EMIF controllers. The ROM Code does not support hybrid configurations, such as EMIF1 tied to LPDDR2 memory and EMIF2 is tied to DDR3 memory.

Similarly, the ROM Code does not support assymetric densities on both controllers.

28.3.8.2.2.1 Enabling of LPDDR2 Temperature Monitoring Feature

When the LPDDR2 memory type is used, the temperature monitoring feature can be enabled by setting the appropriate bits in the CHRAM Flags field:

- • If the value is 0, the temperature monitoring feature is disabled.
- If the value is non-zero, the ROM Code checks the MR4 register inside the LPDDR2 SDRAM component by mode register read operations, at the time of memory initialization. As long as the SDRAM Refresh Rate field is not 0x3 (Temperature ≤ 85° C), it indicates an abnormal temperature state, and the ROM Code waits for MR4 to return to the 0x03 value. The waiting loop cannot exceed

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the timeout indicated by the “EMIF temperature monitoring timeout” value in the Flags field. If the timeout expires, the ROM Code simply resumes EMIF initialization.

28.3.8.2.3 CHFLASH Item

The CHFLASH configuration header contains settings specific to the general-purpose memory controller (GPMC). For more information, see Section 15.4.1, *GPMC Overview*, in Chapter 15, *Memory Subsystem*. Table 28-48 describes the fields.

Table 28-48. CHFLASH Item

Offset	Field	Description
0000h	Section Key	Key used for section verification: C0C0C0C3h.
0004h	Valid	Enables/disables the section: 00h: Disable Others: Enable
0005h	Reserved	
0008h	GPMC_SYSCONFIG (LSB)	Register values
000Ah	GPMC_IRQENABLE (LSB)	
000Ch	GPMC_TIMEOUT_CONTROL (LSB)	
000Eh	GPMC_CONFIG (LSB)	
0010h	GPMC_CONFIG1_0	
0014h	GPMC_CONFIG2_0	
0018h	GPMC_CONFIG3_0	
001Ch	GPMC_CONFIG4_0	
0020h	GPMC_CONFIG5_0	
0024h	GPMC_CONFIG6_0	
0028h	GPMC_CONFIG7_0	
002Ch	GPMC_PREFETCH_CONFIG1	
0030h	GPMC_PREFETCH_CONFIG2 (LSB)	
0032h	GPMC_PREFETCH_CONTROL (LSB)	
0034h	GPMC_ECC_CONFIG	
0036h	GPMC_ECC_CONTROL	
0038h	GPMC_ECC_SIZE_CONFIG (LSB)	
003Ch	Reserved	

28.3.8.2.4 CHMMCSD Item

The CHMMCSD configuration header contains settings specific to the high-speed MMC/SD/SDIO host controller (MMCHS). For more information, see Chapter 24, *MMC/ SD/ SDIO*. Table 28-49 describes the fields.

Table 28-49. CHMMCSD Item

Offset	Register Modified	Description
0000h	Section key	Key used for section verification C0C0C0C4h
0004h	Valid	Enables/disables the section: 00h: Disable Other: Enable
0005h	Reserved	
0008h	MMCHS_SYSCTRL(MSW)	Update MMCHS SYSCTL interface register with the value specified in these fields. The register is not updated if the value is 0xFFFFFFFF.
000Ah	MMCHS_SYSCTRL(LSW)	

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Table 28-49. CHMMCSD Item (continued)

Offset	Register Modified	Description
000Ch	MMCHS interface bus width	Configure the MMCHS interface bus width according to the field value : 1: Configured to 1 bit (SDR) 2: Configured to 4 bits (SDR) 4: Configured to 8 bits (SDR)(1) 8: Configured to 4 bits (DDR)(1) 16: Configured to 8 bits (DDR)(1) 0xFFFF FFFF: Do not update bus width. Others: Reserved

(1) The 8 bits SDR and 4 / 8-bits DDR (resp. value 4,8 and 16) are ONLY applicable to eMMC devices.

The ROM code provides a booting parameter structure to the initial software (see Section 28.3.8.4, *Image Execution*). This structure contains a field that indicates whether the configuration header items have been correctly processed. For a CHMMCSD item, if the MMCHS_SYSCTL and bus width fields are set to 0xFFFF FFFF, the booting parameters report that the CHMMCSD section has not been executed, regardless of the value of the Valid field.

28.3.8.3 GP Header

When the booting memory device is non-XIP (for example, MMC) the image must contain a small header, located before the executable code, and having the size of the software to load and the destination address of where to store it. Table 28-50 describes the image format. The GP header is not required when booting from an XIP memory device (for example, NOR) or in case of peripheral booting. In this case, the peripheral or memory booting image starts directly with executable code.

Table 28-50. GP Header Format

Field	Non-XIP Device Offset	XIP Device Offset	Size (Bytes)	Description
Size	0x0000	–	4	Size of the image
Destination	0x0004	–	4	Address where to store the image or code entry point
Image	0x0008	0x0000	x	Executable code

NOTE: The Destination address field stands for:

- Target address for the image copy from the non-XIP storage to the target XIP location (for example, internal RAM or SDRAM)
- Entry point for image code

Users must take care to locate the code entry point to the target address for image copy.

28.3.8.4 Image Execution

The image is executed when the ROM code performs the branch to the first executable instruction in the initial software. For a GP device in non-XIP, the execution address is the first word after the GP header. The branch is performed in public ARM supervisor mode. The R0 register points to the booting parameter structure that contains information about booting execution. Table 28-51 shows the booting parameter structure.

Table 28-51. Booting Parameter Structure

Offset	Field	Size (Bytes)	Description
0x00	Booting message	4	Last received booting message

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Table 28-51. Booting Parameter Structure (continued)

Offset	Field	Size (Bytes)	Description
0x04	Memory booting device descriptor	4	Pointer to the memory device descriptor that has been used during the memory booting process
0x08	Current booting device	1	Code of device used for booting: 0x01: XIP 0x02 XIP (with wait monitoring) 0x03: NAND 0x04: OneNAND 0x05: SD cards 0x06: eMMC (boot partition) 0x07: eMMC 0x9: SATA 0x43: UART3 0x45: USB Others: Reserved
0x09	Reset reason	1	Current reset reason bit mask (bit = 1, event present): direct copy from lower byte of PRM_RSTST: [0]: Power-on (cold) reset [1]: Global software warm reset [2]: Reserved [3]: MPU watchdog reset [4]: Reserved [5]: External warm reset [6]: VDD MPU voltage manager reset [7]: VDD IVA voltage manager reset
0x0A	CH flags	1	Configuration header items flag. Each item is described by 1 bit. A set bit indicates that the item was executed: [0]: CHSETTINGS [1]: CHRAM [2]: CHFLASH [3]: CHMMCSD Other bits: Reserved

28.3.9 Tracing

Tracing in the public ROM code consists in three 32-bit vectors for which each bit corresponds to a particular way point in the ROM code execution sequence. Table 28-52 through Table 28-54 list the organization of the tracing data in RAM. Tracing vectors are initialized at the beginning of the start-up phase and are updated all along the boot process.

There are two sets of tracing vectors (Table 28-11). The first set is the current trace information (after a cold or warm reset). The second set holds a copy of trace vectors collected at the first ROM code run after a cold reset. As a result, after a warm reset it is possible to have visibility on the boot scenario that occurred during a cold reset.

Table 28-52 lists the organization of tracing vector 1.

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Table 28-52. Tracing Vector 1

Bit	Group	Meaning
0	Boot	Passed the public reset vector
1	Boot	Entered main function
2	Boot	Running after the cold reset
3	Boot	Main booting routine entered
4	Memory boot	Memory booting started
5	Peripheral boot	Peripheral booting started
6	Boot	Booting loop reached last device
7	Boot	GP header found
8	Peripheral Boot	Booting message Skip peripheral booting received
9	Peripheral Boot	Booting message Change device received
10	Peripheral boot	Booting message Peripheral booting received
11	Peripheral boot	Booting message Get ASIC ID received
12	Peripheral boot	Device initialized
13	Peripheral boot	ASIC ID sent
14	Peripheral boot	Image received
15	Peripheral boot	Peripheral booting failed
16	Peripheral boot	Booting message not received (time-out)
17	Peripheral boot	Image size not received (time-out)
18	Peripheral boot	Image not received (time-out)
19	Reserved	
20	Boot	Configuration header found
21	Boot	CHSETTINGS item processed
22	Boot	CHRAM item processed
23	Boot	CHFLASH item processed
24	Boot	CHMMCSD item processed (clock)
25	Boot	CHMMCSD item processed (bus width)
26	Boot	CHMMCSD item processed (eMMC DDR mode)
27	Reserved	
28	Boot	SWCFG general detected
29	Boot	SWCFG clocks detected
30	Boot	SWCFG time-out detected
31	Reserved	

Table 28-53 lists the organization of tracing vector 2.

Table 28-53. Tracing Vector 2

Bit	Group	Meaning
0	Configuration Header	CHSATA item processed
1	Reserved	
2	Reserved	
3	Reserved	
4	USB	USB connected
5	USB	USB configured
6	Reserved	
7	Reserved	
8	Reserved	
9	Reserved	Reserved

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Table 28-53. Tracing Vector 2 (continued)

Bit	Group	Meaning
10	Reserved	Reserved
11	Reserved	Reserved
12	Memory boot	Memory booting trial (first block)
13	Memory boot	Memory booting trial (second block)
14	Memory boot	Memory booting trial (third block)
15	Memory boot	Memory booting trial (fourth block)
16	Reserved	Reserved
17	Reserved	
18	Reserved	
19	Reserved	
20	Reserved	
21	Reserved	
22	Reserved	
23	Reserved	
24	Reserved	
25	Reserved	
26	Reserved	
27	Reserved	
28	Reserved	
29	Reserved	
30	Boot	Jumping to Initial Software (GP device)
31	Reserved	Reserved

Table 28-54 lists the organization of tracing vector 3.

Table 28-54. Tracing Vector 3

Bit	Group	Meaning
0	Reserved	Reserved
1	Memory boot	Memory booting device XIP
2	Memory boot	Memory booting device XIPWAIT
3	Memory boot	Memory booting device NAND
4	Memory boot	Memory booting device OneNAND
5	Memory boot	Memory booting device MMC1 (SD cards)
6	Memory boot	Memory booting device: eMMC (from boot partition)
7	Memory boot	Memory booting device MMC2: eMMC (from user area)
8	Reserved	
9	Memory boot	Memory booting device: SATA
10	Reserved	
11	Reserved	
12	Reserved	
13	Reserved	
14	Reserved	
15	Reserved	
16	Reserved	
17	Reserved	
18	Reserved	Reserved

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Table 28-54. Tracing Vector 3 (continued)

Bit	Group	Meaning
19	Peripheral boot	Peripheral booting device UART3
20	Reserved	Reserved
21	Peripheral boot	Peripheral booting device USB
22	Reserved	Reserved
23	Reserved	Reserved
24	Reserved	
25	Reserved	
26	Reserved	
27	Reserved	
28	Boot	Started to retrieve device list from I^2C1 connected EEPROM
29	Boot	Failed to retrieve device list from I^2C1 connected EEPROM
30	Reserved	
31	Reserved	

Table 28-55. Tracing Vector 4

Bit	Group	Meaning
[23:0]	Reserved	
24	MMC/SD	SD card detected PBIAS configuration is 1.8V
[27:24]	Reserved	
28	SATA	SATA is configured
29	SATA	SATA retried
30	SATA	SATA failed
31	Reserved	

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28.4 Services for HLOS Support

The ROM code provides different services that can be called on GP devices for L1 and L2-cache maintenance, Enter in Low Power, etc. These services are implemented in monitor mode and must be called by using the SMC instruction. The caller must ensure the save and restore of the processor registers before and after calling the Monitor Service.

The following code example shows how the monitor ROM code functions can be accessed by an application running in public mode:

```
;-------------------------------------------------------------------------------
; FUNCTION: SetL2CacheLatency
;
; DESCRIPTION: Function calls the Monitor Service to setup the L2 Cache Latency
;
; INPUTS:  r0 Tag RAM Latency to set
;          r1 Data RAM Latency to set
; RETURN:
;
;-------------------------------------------------------------------------------
SetL2CacheLatency           FUNCTION

  PUSH {R1-R12, LR}
  LDR R12, =0x105
  SMI 0x1
  POP {R1-R12, PC}
  ENDFUNC
```

28.4.1 Caches Maintenance

Table 28-56. Clean L1 and/or L2 cache

Function ID	**Description**	
R12 = 0x103	This function cleans and invalidates the CPU L1-cache and if requested in the input parameter R0, clean the full L2-cache.	
Parameters		
Type	*Location*	*Description*
Input	R0	if not equal to 0, clean L2-cache
Output		
Return		

28.4.2 CP15 Registers

Table 28-57. Write L2 Cache Auxiliary Control

Function ID	**Description**	
R12 = 0x104	This function writes the CP15 L2 Cache Auxiliary Control Register with the input given value in R0.	
Parameters		
Type	**Location**	**Description**
Input	R0	Value to set in the register
Output		
Return		

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Table 28-58. Write Tag and Data RAM Latency Control Register

Function ID	Description	
R12 = 0x105	This function writes the L2 Cache Tag and Data RAM Latency in the CP15 L2 Control Register with the input given value in R0 and R1.	
Parameters		
Type	**Location**	**Description**
Input	R0 R1	Tag RAM Latency to set Data RAM Latency to set
Output		
Return		

Table 28-59. Write L2 Cache Prefetch Control Register

Function ID	Description	
R12 = 0x106	This function writes the CP15 L2 Cache Prefetch Control Register with the input given value in R0.	
Parameters		
Type	**Location**	**Description**
Input	R0	Value to set in the register
Output		
Return		

Table 28-60. Write Auxiliary Control Register

Function ID	Description	
R12 = 0x107	This function writes the CP15 Auxiliary Control Register with the input given value in R0.	
Parameters		
Type	**Location**	**Description**
Input	R0	Value to set in the register
Output		
Return		

28.4.3 Wakeup Generator

Table 28-61. Write AMBA IF Register

Function ID	Description	
R12 = 0x108	This function writes the WakeupGen AMBA I/F Register with the input given value in R0.	
Parameters		
Type	**Location**	**Description**
Input	R0	value to set in the register
Output		
Return		

28.4.4 Low Power

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Table 28-62. Enter in Low Power

Function ID	Description	
R12 = 0x100	This function configures the MPU Subystem and CPU to enter in the given Low Power Mode.	
Parameters		
Type	**Location**	**Description**
Input	R0	R0- pointer to target modes structure (see the below table)
Output		
Return		

Table 28-63. Power API - PWR_Modes_t Structure

Offset	Field	Size	Value
0x0	Cpu_Mode	1 Byte	0: NO_CHANGE (doesn't change the CPU setting) 1: ON 2: INACTIVE 3: CSWRET 4: Reserved 5: OFF 6: FORCED_OFF (only on CPU 1)
0x4	Mpu_Mode	1 Byte	0: NO_CHANGE (doesn't change the MPU setting) 1: ON 2: INACTIVE 3: CSWRET 4,5: Reserved
0x8	Core_Mode	1 Byte	0: ON 1,2: Reserved

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On-Chip Debug Support

This chapter describes the on-chip debug support.

NOTE: The L3_MAIN interconnect is instantiation of the NoC interconnect from Arteris, Inc. Arteris is a registered trademark of Arteris, Inc.

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NoC is an abbreviation for Network On Chip.

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29.1 Introduction

Debugging a system that contains an embedded processor involves an environment that connects high-level debugging software running on a host computer to a low-level debug interface supported by the target device. Between these levels, a debug and trace controller (DTC) facilitates communication between the host debugger and the debug support logic on the target chip.

The DTC is a combination of hardware and software that connects the host debugger to the target system. The DTC uses one or more hardware interfaces and/or protocols to convert actions dictated by the debugger user to JTAG® commands and scans that execute the core hardware.

The debug software and hardware components let the user control multiple central processing unit (CPU) cores embedded in the device in a global or local manner. This environment provides:

- Synchronized global starting and stopping of multiple processors
- Starting and stopping of an individual processor
- Each processor can generate triggers that can be used to alter the execution flow of other processors.

System topics include but are not limited to:

- System clocking and power-down issues
- Interconnection of multiple devices
- Trigger channels

The device provides the following on-chip debug support features:

- External debug interfaces:
  - Primary debug interface - IEEE1149.1 (JTAG) or IEEE1149.7 (complementary superset of JTAG)
    - Used for debugger connection
    - Default mode is IEEE1149.1 but debugger can switch to IEEE1149.7 via an IEEE1149.7 adapter module
    - Controls ICEPick™ (generic test access port [TAP] for dynamic TAP insertion) to allow the debugger to access several debug resources through its secondary (output) JTAG ports (for more information, see Section 29.3.3.1, *ICEPick Secondary TAPs*).
    - For more information about IEEE1149.1, see Section 29.2.1, *IEEE1149.1*.
    - For more information about IEEE1149.7, see Section 29.2.2, *IEEE1149.7*.
  - Secondary debug interface – MIPI® Narrow Interface for Debug and Trace (NIDnT)
    - Used for end product debug
    - Debugger can be plugged instead of SD card
    - For more information about NIDnT, see Section 29.2.4, *Narrow Interface for Debug and Trace (NIDnT)*.
  - Debug (trace) port
    - Can be used to export processor or system trace off-chip (to an external trace receiver)
    - Can be used for cross-triggering with an external device
    - Configured through debug resources manager (DRM) module instantiated in the debug subsystem
    - For more information about debug (trace) port, see Section 29.2.3, *Debug (Trace) Port* , and Section 29.10, *Concurrent Debug Modes*.
- Dynamic TAP insertion
  - Controlled by ICEPick
  - For more information, see Section 29.3.3, *Dynamic TAP Insertion.*
- Power and clock management
  - Debugger can get the status of the power domain associated to each TAP.
  - Debugger may prevent the application software switching off the power domain.
  - Application power management behavior can be preserved during debug across power transitions.

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  - For more information, see Section 29.5.1, *Power and Clock Management.*
- Reset management
  - Debugger can configure ICEPick to assert, block, or extend the reset of a given subsystem.
  - For more information, see Section 29.5.2, *Reset Management.*
- Cross-triggering
  - Provides a way to propagate debug (trigger) events from one processor, subsystem, or module to another:
    - Subsystem A can be programmed to generate a debug event, which can then be exported as a global trigger across the device.
    - Subsystem B can be programmed to be sensitive to the trigger line input and to generate an action on trigger detection.
  - Two global trigger lines are implemented
  - Device-level cross-triggering is handled by the XTRIG (TI cross-trigger) module implemented in the debug subsystem
  - Various ARM® CoreSight™ cross-trigger modules implemented to provide support for CoreSight triggers distribution
    - CoreSight Cross-Trigger Interface (CS_CTI) modules
    - CoreSight Cross-Trigger Matrix (CS_CTM) modules
  - For more information about cross-triggering, see Section 29.4.2, *Cross-Triggering.*
- Suspend
  - Provides a way to stop a closely coupled hardware process running on a peripheral module when the host processor enters debug state
  - For more information about suspend, see Section 29.4.3, *Suspend.*
- MPU watchpoint
  - Embedded in MPU subsystem
  - Provides visibility on MPU to EMIF direct paths
  - For more information, see Section 29.7, *MPU Memory Adaptor.(MA_MPU) Watchpoint*
- Processor trace
  - Only Cortex™-A15 (MPU) trace is supported
  - Program trace only (no data trace)
  - Supported by a CoreSight Program Trace Macrocell (CS_PTM) module (per MPU core)
  - Three exclusive trace sinks:
    - CoreSight Trace Port Interface Unit (CS_TPIU) – trace export to an external trace receiver
    - CTools Trace Buffer Router (CT_TBR) in system bridge mode – trace export through USB
    - CT_TBR in buffer mode – trace history stored into on-chip trace buffer
  - For more information, see Section 29.8, *Processor Trace.*
- System instrumentation (trace)
  - Supported by a CTools System Trace Module (CT_STM), implementing:
    - MIPI System Trace Protocol (STP1.0) for trace export througn Parallel Trace Interface (PTI)
    - MIPI STP2.0 for trace export through Advanced Trace Bus (ATB)
  - Real-time software trace
    - MPU software instrumentation through CoreSight STM (CS_STM) (STP2.0)
    - System-on-chip (SoC) software instrumentation through CT_STM (STP2.0)
  - OCP watchpoint (OCP_WP_NOC)
    - OCP target traffic monitoring: OCP_WP_NOC can be configured to generate a trigger upon watchpoint match (that is, when target transaction attributes match the user-defined attributes).
    - SoC events trace

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    - DMA transfer profiling
  - Statistics collector (performance probes)
    - Computes traffic statistics within a user-defined window and periodically reports to the user through the CT_STM interface
    - Embedded in the L3_MAIN interconnect
    - Three instances:
      - One instance dedicated to target load monitoring
      - Two instances dedicated to master latency monitoring
  - IVA instrumentation (hardware accelerator [HWA] profiling)
    - Supported through a software message and system trace event (SMSET) module embedded in the IVA subsystem
  - Power-management events profiling (PM instrumentation [PMI])
    - Monitoring major power-management events. The PM state changes are handled as generic events and encapsulated in STP messages.
  - Clock-management events profiling (CM instrumentation [CMI])
    - Monitoring major clock management events. The CM state changes are handled as generic events and encapsulated in STP messages.
    - Two instances, one per CM
      - CM1 Instrumentation (CMI1) module mapped in the PD_CORE_AON power domain
      - CM2 Instrumentation (CMI2) module mapped in the PD_CORE power domain
  - For more information, see Section 29.9, *System Instrumentation.*
- Performance monitoring
  - Supported by subsystem counter timer modules (SCTMs) for digital signal processor (DSP) and interrup processing unit (IPU) subsystems
  - Supported by performance monitoring unit (PMU) for MPU subsystem
  - For more information, see Section 29.6, *Performance Monitoring*.

For easy integration into applications, a set of application-programming interfaces (APIs) for debug-IP programming and a software message library are provided. CToolsLib is a library of embedded target APIs to enable easy programmatic access to the chip tools (CTools), which are system-level debug facilities included in the debug subsystem capabilities of TI devices. More information about the APIs, download files, and other useful links for available libraries can be found on the CToolsLib Wiki site:

http://processors.wiki.ti.com/index.php/CToolsLib

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29.2 Debug Interfaces

29.2.1 IEEE1149.1

The target debug interface has the following signals:

- Five standard IEEE1149.1 JTAG signals: nTRST, TCK, TMS, TDI, and TDO
- A return clock (RTCK) due to the clocking requirements of the ARM968™ processor
- Two EMU [1:0] or five EMU [4:0] TI extensions, depending on the pin count (14 or 20 pins) in the JTAG header of the device

Table 29-1 describes the IEEE1149.1 signals.

Table 29-1. IEEE1149.1 Signals

Pin Name	Internal Signal Name	Type(1)	Pull Type (2)	Function	Description
jtag_ntrst	nTRST	I	PD	Test reset	When asserted (active low), resets all test and debug logic in the device along with the IEEE1149.1 interface
jtag_tck	TCK	I	PD	Test clock	This is the test clock used to drive an IEEE1149.1 TAP state-machine and logic. This is either a free-running clock or a gated clock, depending on the DTC attached to the device and the RTCK monitoring.
jtag_rtck	RTCK	O	N/A	Returned (synchronized) test clock	Depending on the DTC attached to the device, the JTAG signals are either clocked from RTCK or the RTCK is monitored by the DTC to the gate TCK.
jtag_tms_tmsc	TMS	I	PU	Test mode select	Directs the next state of the IEEE1149.1 TAP state-machine.
jtag_tdi	TDI	I	PU	Test data input	Scans data input to the device.
jtag_tdo	TDO	O	PU	Test data output	Scans data output by the device.
drm_emu0	EMU0	I/O	PU	Emulation 0	Channel 0 trigger or boot mode or trace port
drm_emu1	EMU1	I/O	PU	Emulation 1	Channel 1 trigger or boot mode or trace port
drm_emu2(3)	EMU2(3)	O	PD	Emulation 2	Trace port
drm_emu3(3)	EMU3(3)	O	PD	Emulation 3	Trace port
drm_emu4(3)	EMU4(3)	O	PD	Emulation 4	Trace port

(1) I = Input; O = Output; I/O = bidirectional

(2) PU = internal pullup; PD = internal pulldown

(3) 20-pin JTAG header only

The device JTAG ID code can be accessed through ICEPick. For information about the JTAG ID code value, see Chapter 1, *Introduction*.

29.2.2 IEEE1149.7

In addition to the legacy standard JTAG mode of operation, the target debug interface can also be switched to a compressed JTAG mode of operation; this mode is commonly called the IEEE1149.7 standard. An IEEE1149.7 adapter module runs a 2-pin communication protocol on top of an IEEE1149.1 JTAG TAP. Using a variety of compression formats, the debug-IP logic serializes the IEEE1149.1 transactions to reduce the number of pins needed to implement a JTAG debug port. The device implements only a subset of the IEEE1149.7 protocol (see Table 29-3).

NOTE: At power-on reset (POR), the default debug interface mode is IEEE1149.1. For the scan sequence required to switch modes, see the IEEE1149.7 specification.

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The IEEE1149.7 communication protocol can switch between serial and parallel formats. The parallel format consists of the IEEE1149.1 signals, TCK, TMS, TDI, TDO, nTRST, and a return clock (RTCK), if stalls are required. The serial format uses two signals, TCK and TMSC. The values of the TMS, TDI, TDO, and RTCK signals are multiplexed on the bidirectional pin, jtag_tms_tmsc, by the Debug-IP logic. Each TCK of the DTC is serialized into a packet, which is transmitted to the IEEE1149.7 adapter, where it is converted back to parallel. The TDO and RTCK information are returned during the packet transmission.

NOTE: Only MScan, Oscan0, and Oscan4 formats can be used if the device requires stalls.

Table 29-2 describes the IEEE1149.7 signals.

Table 29-2. IEEE1149.7 Signals

Pin Name	Internal Signal Name	Type[1]	Pull Type [2]	Function	Description
jtag_tck	TCK	I	PD	Test clock	This is the test clock used to drive an IEEE1149.1 TAP state-machine and logic. This is either a free-running or a gated clock, depending on the DTC attached to the device and the TMSC RDY field monitoring.
jtag_tms_tmsc	TMSC	I/O	PU	Test mode control and data scan	Compressed JTAG packet. The TMSC signal is driven only when the TCK signal is low. The signal level must be maintained by a keeper while the TCK signal is high.

(1) I = Input; O = Output; I/O = bidirectional
(2) PU = internal pullup; PD = internal pulldown

The device provides a NODE ID identifier to support platform with up to four identical OMAP5430 devices for multidrop debug. The identifier is provided by two external pins (sys_nodeid[1:0]) sensed during the boot sequence.

NOTE: An PCB pull is required on each of the sys_nodeid[1:0] pins.

Table 29-3 summarizes the IEEE1149.7 features subset supported by the device.

Table 29-3. IEEE1149.7 Features Subset

	IEEE1149.7 Feature	Device Support	Comment
Configuration	Class 4 TAP	✓	Supports 2-pin operation
	Class 5 TAP	✓	BDX or CDX channel (CT_UART)
Optional Components	FRST	–	Functional reset (done through ICEPick)
	TRST	–	Test reset
	RDBK capability	✓	Read back of register data
	Auxiliary pin functions	–	Reuse of TDI and TDO pins
	TCKWID	✓	Programmable TCK width

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Table 29-3. IEEE1149.7 Features Subset (continued)

	IEEE1149.7 Feature	Device Support	Comment
Scan Formats	JScan0	✓	Parallel mode
	JScan1	✓	Parallel with firewall
	JScan2	✓	Parallel with super-bypass select
	JScan3	✓	Parallel with register select
	SScan0	–	Segmented scan
	SScan1	–	Segmented scan + stalls
	SScan2	–	Segmented scan
	SScan3	–	Segmented scan + stalls
	Oscan0	✓	Support stalls
	Oscan1	✓	Nonstall mode
	Oscan2	✓	Bidirectional transfers
	Oscan3	✓	Host to target only
	Oscan4	✓	Support stalls
	Oscan5	✓	Pipelined
	Oscan6	✓	Bidirectional transfers
	Oscan7	✓	Host to target only
	Mscan	✓	Multi devices mode + stalls
Power Control	Power down logic	–	Handled by ICEMelter

The debug subsystem instantiates a CTools UART (CT_UART) module (see row 2 of Table 29-3) responsible for providing a way to send and receive blocks of data, which is compliant with the IEEE1149.7 data channel interface specification. The CT_UART module contains two buffers, one for sending data to the DTC controller (the TX buffer) and one for receiving data from the DTC controller (the RX buffer). The CT_UART module generates an interrupt (DEBUGSS_IRQ_CT_UART) to the INTC_MPU (MPU_IRQ_90 interrupt line) when one of the following conditions occurs:

- TX buffer empty
- Data ready on RX buffer

29.2.3 Debug (Trace) Port

On-chip debug and trace events can be exported to external equipment through the debug (trace) port of the device. The following exportable debug events and trace sources are supported:

- Debug events
  - Triggers. For more information about triggers, see Section 29.4.2, *Cross-Triggering*.
- Trace sources
  - Processor trace: Cortex-A15 MPU trace supported by the CS_PTM module. For more information about the processor trace, see Section 29.8, *Processor Trace*.
  - System trace: Trace coming from various system instrumentation modules, and supported by the CT_STM module. For more information about the system trace, see Section 29.9, *System Instrumentation*.

Not all debug and trace features can be supported concurrently because of the limited number of pins allocated to debug. Thus, multiplexing among debug and trace sources is implemented. The configuration and the debug/trace source selection occur through the DRM module embedded in the debug subsystem.

Table 29-4 describes the trace port signals.

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Table 29-4. Trace Port Signals

Pin Name	Internal Signal Name	I/O[1]	Pull Type [2]	Description
drm_emu19	EMU19	O	PD	Debug resource manager pin 19
drm_emu18	EMU18	O	PD	Debug resource manager pin 18
drm_emu17	EMU17	O	PD	Debug resource manager pin 17
drm_emu16	EMU16	O	PD	Debug resource manager pin 16
drm_emu15	EMU15	O	PD	Debug resource manager pin 15
drm_emu14	EMU14	O	PD	Debug resource manager pin 14
drm_emu13	EMU13	O	PD	Debug resource manager pin 13
drm_emu12	EMU12	O	PD	Debug resource manager pin 12
drm_emu11	EMU11	O	PD	Debug resource manager pin 11
drm_emu10	EMU10	O	PD	Debug resource manager pin 10
drm_emu9	EMU9	O	PD	Debug resource manager pin 9
drm_emu8	EMU8	O	PD	Debug resource manager pin 8
drm_emu7	EMU7	O	PD	Debug resource manager pin 7
drm_emu6	EMU6	O	PD	Debug resource manager pin 6
drm_emu5	EMU5	O	PD	Debug resource manager pin 5
drm_emu4	EMU4	O	PD	Debug resource manager pin 4
drm_emu3	EMU3	O	PD	Debug resource manager pin 3
drm_emu2	EMU2	O	PD	Debug resource manager pin 2
drm_emu1	EMU1	I/O	PU	Debug resource manager pin 1
drm_emu0	EMU0	I/O	PU	Debug resource manager pin 0

(1) I = Input; O = Output; I/O = bidirectional
(2) PU = internal pullup; PD = internal pulldown

NOTE: The drm_emu[19:0] pins are shared with other functional (application) pins on the device boundary. To use the drm_emu[19:0] pins, the user must program the device application pin manager (control module) appropriately. For more information, see Chapter 18, *Control Module*.

For more information about DRM multiplexing and concurrent debug modes, see Section 29.10, *Concurrent Debug Modes*.

29.2.4 Narrow Interface for Debug and Trace (NIDnT)

Typically, the device-wide debug port is no more available on a packaged end product phone due to connectivity and footprint constraints. The device provides a NIDnT on MMC connector compliant to the MIPI NIDnT specification. The NIDnT port provides the following pins:

- 1 clock – n_clk
- 4 data – n_d[3:0]

Table 29-5 summarizes the NIDnT debug pins mapping.

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Table 29-5. NIDnT Mapping

Module	Control Module Multiplexing				
	MUX0	MUX3	MUX4	MUX5	MUX6
SD card (MMC)	sdcard_clk	jtag_rctk	–	n_clk	–
	sdcard_cmd	jtag_tdo	uart6_rx	–	n_d2
	sdcard_dat0	jtag_tdi	–	n_d0	–
	sdcard_dat1	jtag_ntrst	–	n_d1	–
	sdcard_dat2	jtag_tms_tmsc	–	n_d2	–
	sdcard_dat3	jtag_tck	–	n_d3	–

The NIDnT standard supports several overlay modes. A DRM register provides a means of switching NIDnT overlay modes by software. The overlay mode selection register is immune to warm reset and functional (that is, nondebug) power and voltage transitions.

Table 29-6 shows the NIDnT overlay modes supported in the device.

Table 29-6. NIDnT Overlay Modes in the Device

NIDnT Overlay Mode 0 (Functional)	NIDnT Overlay Mode 1[1] (MIN-pin debug)	NIDnT Overlay Mode 2[1] (Legacy debug)	NIDnT Overlay Mode 3[1] (Not supported in the device)	NIDnT Overlay Mode 4[1] (Debug + PTIv1/PTIv2 [dedicated clk] + user extension)	NIDnT Overlay Mode 5[1] (Debug + PTIv1/PTIv2 [dedicated clk])	NIDnT Overlay Mode 6 (PTIv1/PTIv2 + user extension)	NIDnT Overlay Mode 7 (Not supported in the device)
CLK out	–	RTCK out	N/A	TRC_CLK out	TRC_CLK out	TRC_CLK out	N/A
CMD in/out	–	TDO out	N/A	USER_EXT[2] in/out	TRC_DATA[2] out	USER_EXT[2] in/out	N/A
DAT0 in/out	–	TDI in	N/A	TRC_DATA[0] out	TRC_DATA[0] out	TRC_DATA[0] out	N/A
DAT1 in/out	–	nTRST in	N/A	TRC_DATA[1] out	TRC_DATA[1] out	TRC_DATA[1] out	N/A
DAT2 in/out	TMSC in/out	TMS in	N/A	TMSC in/out	TMSC in/out	TRC_DATA[2] out	N/A
DAT3 in/out	TCKC in	TCK in	N/A	TCKC in	TCKC in	TRC_DATA[3] out	N/A

(1) The NIDnT overlay modes with the TCKC or TCK pin function do not work when external level shifters are used.

(2) USER_EXT is a user-defined signal and can be either input or output. A common implementation uses this pin for UART_RX (that is, input to the SoC).

The NIDnT overlay mode selection will override SDCARD pin mapping. For example, selecting overlay mode 5 will override the SDCARD pin mapping as follows:

- Sdcard_clk = MUX5 = n_clk (TRC_CLK)
- Sdcard_cmd = MUX6 = n_d2 (TRC_DATA[2])
- Sdcard_data0 = MUX5 = n_d0 (TRC_DATA[0])
- Sdcard_data1 = MUX5 = n_d1 (TRC_DATA[1])
- Sdcard_data2 = MUX3 = jtag_tmsc (TMSC)
- Sdcard_data3 = MUX3 = jtag_tck (TCKC)

For more information about the NIDnT concept, see the *MIPI Alliance Test and Debug – NIDnT-Port* specification.

29.2.5 IEEE1149.1 Expansion Port

The device also provides a JTAG expansion port (with inverted JTAG signals) to attach a MODEM device (or other IC). Table 29-7 describes the JTAG expansion port signals.

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Table 29-7. IEEE1149.1 Expansion Port Signals

Pin Name	Internal Signal Name	Type	Function
jtagtapext_ntrst	nTRST	O	Test reset for external modem or other IC
jtagtapext_tck	TCK	O	Test clock for external modem or other IC
jtagtapext_rtck	RTCK	I	Returned (synchronized) test clock for external modem or other IC
jtagtapext_tmsc	TMS	O	Test mode select for external modem or other IC
jtagtapext_tdi	TDI	I	Test data input for external modem or other IC
jtagtapext_tdo	TDO	O	Test data output for external modem or other IC

The JTAG expansion is handled by:

- Inserting the MDM secondary TAP in the ICEPICK scan chain (see Table 29-9 for ICEPICK scan chain).
- Routing the MDM secondary TAP to device pads (for more details, see Chapter 18, *Control Module*).

29.2.6 Trace Connector and Board Layout Considerations

Because the device supports processor trace and system trace exports, one of the following header configurations may be required at board level:

- A 60-pin header in place of the traditional TI 14-pin
- A TI 20-pin emulation header

For more information about the trace connectors and board layout considerations for these high-speed signals, see *Emulation and Trace Headers* (TI literature number SPRU655).

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29.3 Debugger Connection

29.3.1 ICEPick Module

The debugger connects to the device through its JTAG interface. The first level of debug interface seen by the debugger is the IEEE1149.7 adapter connected to the ICEPick module embedded in the debug subsystem.

NOTE: ICEPick version D (ICEPick-D) is used in the device.

SoC designs typically have multiple processors, each having a JTAG TAP embedded in the processor. The ICEPick module manages these TAPs and the power, reset, and clock controls for modules that have TAPs.

The ICEPick module is visible only from the debugger point of view and thus cannot be programmed by application software. The debugger can configure ICEPick through its own TAP controller. The ICEPick TAP has an instruction length of 6 bits and is the primary TAP. It is always visible in the scan chain and is used to control and monitor the other secondary TAPs.

ICEPick provides the following debug capabilities:

- Debug connect logic for enabling or disabling most ICEPick instructions
- Dynamic TAP insertion
  - Serially linking up to 16 TAP controllers (the device implements 7 TAPs)
  - Individually selecting one or more of the TAPs for scan without disrupting the instruction register (IR) state of other TAPs
- Power, reset, and clock management (PRCM)
  - Provides the power and clock states of each domain
  - Provides debugger control of the power domain of a processor. Can force the domain power and clocks on, and prohibit the domain from being clock-gated or powered down while a debugger is connected.
  - Applies system reset
  - Provides wait-in-reset (WIR) boot mode
  - Provides global and local WIR release
  - Provides global and local reset blocking

The ICEPick module implements a connect register, which must be configured with a predefined key to enable the full set of JTAG instructions. Once the debug connect key is properly programmed, ICEPick signals and subsystems emulation logics should be turned on.

For more information about ICEPick dynamic TAP insertion, see Section 29.3.3, *Dynamic TAP Insertion*.

For more information about ICEPick PRCM features, see Section 29.5, *Power, Reset, and Clock Management Debug Support*.

29.3.2 ICEPick Boot Modes

The initial configuration of ICEPick is determined by the level of the drm_emu0 and drm_emu1 pins at POR release. At POR, drm_emu0 and drm_emu1 are automatically configured as inputs. The drm_emu0 and drm_emu1 pins are free when POR is released.

Table 29-8 summarizes the ICEPick boot modes.

Table 29-8. ICEPick Boot Modes at POR

drm_emu1	drm_emu0	TAPs in the TDI → TDO Path	Other Effects/Comments
0	0	None	Reserved (do not use)
0	1	None	Reserved (do not use)
1	0	ICEPick	TAP only + WIR mode

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Table 29-8. ICEPick Boot Modes at POR (continued)

drm_emu1	drm_emu0	TAPs in the TDI → TDO Path	Other Effects/Comments
1	1	ICEPick	TAP only (default mode)

29.3.2.1 Default Boot Mode

In ICEPick-only configuration, none of the secondary TAPs are selected. The ICEPick TAP is the only TAP between device-level TDI and TDO pins. This mode is the recommended boot mode.

29.3.2.2 Wait-In-Reset

The device can boot to invoke WIR mode. If the device is booted in this mode, all processors within the device that support a TAP through ICEPick are held in reset until released. Individual processors can be released from reset (local), or all processors held in the reset state can be released at the same time (global).

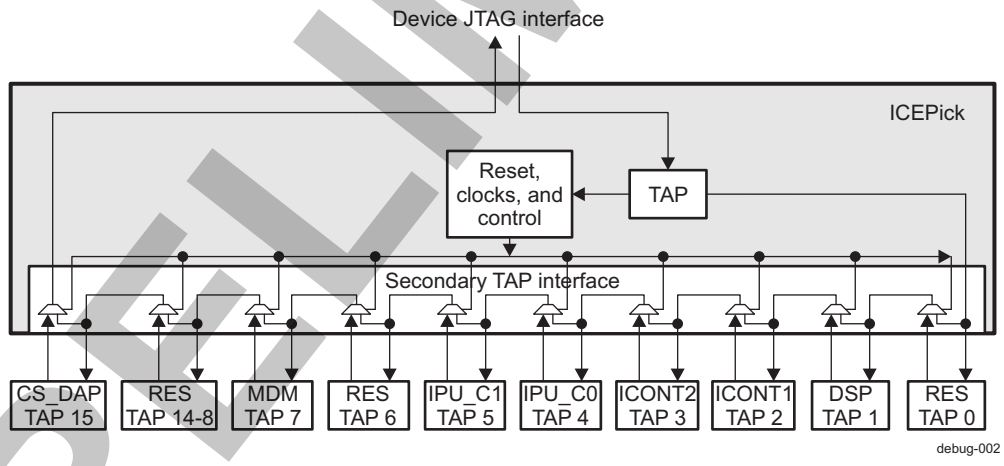
29.3.3 Dynamic TAP Insertion

29.3.3.1 ICEPick Secondary TAPs

To include more or fewer secondary TAPs in the scan chain, the debugger must use the ICEPick TAP router to program the TAPs. At its root, ICEPick is a scan-path linker that lets the DTC selectively choose which subsystem TAPs are accessible through the device-level debug interface. Each secondary TAP can be dynamically included in or excluded from the scan path. From the external JTAG interface point of view, secondary TAPs that are not selected appear not to exist.

Figure 29-1 shows the TAPs in the ICEPick scan chain.

Figure 29-1. ICEPick Scan Chain



NOTE: RES = Reserved/not used

Table 29-9 lists the secondary debug TAPs connected to the ICEPick scan chain along with the modules that can be accessed. The TAP number shows the position of the TAP in the scan chain.

Table 29-9. ICEPick Secondary Debug TAP Mapping

Secondary JTAG Port	CoreSight	TAP Number	Modules Accessed Through That JTAG Port
Reserved	No	0	–
DSP	No	1	C64x+™/ICEMaker
IVA ICONT1	No	2	ARM968/ICECrusher™-9

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Table 29-9. ICEPick Secondary Debug TAP Mapping (continued)

Secondary JTAG Port	CoreSight	TAP Number	Modules Accessed Through That JTAG Port
IVA ICONT2 (vDMA)	No	3	ARM968/ICECrusher-9
IPU	No	4	Cortex-M4/ICECrusher-CS
	No	5	Cortex-M4/ICECrusher-CS
Reserved	No	6	–
MDM	No	7	MODEM expansion port
Reserved	No	8-14	–
CS_DAP (APB-AP)	Yes	15	MPU_C0, MPU_C1(1)
	Yes		CS_PTM x 2(1)
	Yes		CS_CTI x 2(1)
	Yes		CS_STM(1)
	Yes		CS_TF_MPU(1)
	No		DAP_PC(1)
	No		ATB_FIFO_SGU(1)
	Yes		CT_TBR(2)
	Yes		CS_TF_DEBUGSS(2)
	Yes		CS_TPIU(2)
	No		DRM(2)
	Yes		CT_STM(2)
	Yes		CS_CTI(2)
CS_DAP (AHB-AP)	No		IVA SMSET
	No		IVA hardware accelerators
	No		NOC statistics collectors (three instances)
	No		OCP_WP_NOC
	No		CMI1
	No		CMI2
	No		PMI

(1) Embedded in MPU
(2) Embedded in DEBUGSS

NOTE: MA_MPU watchpoint programming is restricted to the MPU. Programming from the CS_DAP APB access port is not supported.

The MPU timestamp registers are part of the PRCM_MPU programming model and can be accesses from the two MPU cores.

For more information about ICEPick scan sequences (adding one or more TAPs to the scan chain), see:

http://processors.wiki.ti.com/images/f/f6/Router_Scan_Sequence-ICEpick-D.pdf

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Besides secondary debug TAPs, ICEPick also supports power, reset, and clock controls for non-JTAG debug cores. The debug cores are accessible through CS_DAP.

Table 29-10 summarizes the ICEPick debug core mapping.

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Table 29-10. ICEPick Debug Core Mapping

Debug Core	Module
0	MPU
1	IVA ILF3
2	IVA IME3
3	IVA CALC3
4	IVA IPE3
5	IVA MC3
6	IVA ECD3

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29.4 Primary Debug Support

29.4.1 Processor Native Debug Support

29.4.1.1 Cortex-A15 Processor

The dual Cortex-A15 processor supports the following native debug features:

- Halt mode and monitor mode debugging
- Six breakpoints and four watchpoints
- Asynchronous aborts
- Performance monitoring
- Cross-triggering: Allows stopping one CPU upon debug event (for example, breakpoint) detection in the other CPU

For more information about Cortex-A15 native debug support features, see the *Cortex-A15 Technical Reference Manual*.

29.4.1.2 Cortex-M4 Processor

The Cortex-M4 processor supports the following native debug features:

- Program halt and stepping
- Hardware breakpoints, breakpoint instruction
- Data watchpoint on access to data add, add range, and data value
- Register value accesses
- Debug monitor exception
- Memories accesses

For more information about Cortex-M4 native debug support features, see the *Cortex-M4 Technical Reference Manual*.

29.4.1.3 DSP

The DSP core supports limited advanced event triggering (AET) with the following capabilities:

- Hardware program breakpoints: Specify addresses or address ranges that can generate events, such as halting the processor or triggering the trace capture.
- Data watchpoints: Specify data variable addresses, address ranges, or data values that can generate events such as halting the processor or triggering the trace capture.

Known restrictions of this DSP core:

- No DSP processor trace support
- No real-time mode debug mode support
- Limited AET support, only two watchpoint units
- No HSRTDX support

29.4.1.4 IVA ARM968

The ARM968E-S processor (in each ICONT) supports the following native debug features through its EmbeddedICE-RT logic:

- Two hardware watchpoints/breakpoints
- Halt mode and monitor mode debugging
- Debug control and status registers
- Debug communications channel

For more information about ARM968 native debug support features, see the *ARM968E-S Technical Reference Manual*.

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29.4.1.5 IVA Hardware Accelerators

Hardware accelerators offer the following debug capabilities through their embedded SYNCBOX module:

- Manual halt: Halt occurs at the SYNCBOX task boundary when requested by the debugger.
- Single-step execution at SYNCBOX task level (from 1 to *n* macroblocks depending on the user software)
- Cross-triggering: Hardware accelerator can halt (after the execution of current SYNCBOX task) based on trigger event detection.
- Global run

Table 29-11 summarizes the debug capabilities of the hardware accelerator SYNCBOX.

Table 29-11. Hardware Accelerator Debug Capability Options

Feature	IME3	IPE3	MC3	CALC3	ILF3	ECD3
Core reset	–	–	–	–	–	–
Execution request	–	–	–	–	–	–
Trigger output	–	–	–	–	–	–
Trigger input	✓	✓	✓	✓	✓	✓
Number of trigger channels	1	1	1	1	1	1
Number of counters	0	0	0	0	0	0
Number of watchpoints	0	0	0	0	0	0
Number of hardware breakpoints	0	0	0	0	0	0

29.4.2 Cross-Triggering

The device supports a cross-triggering feature that provides a way to propagate debug (trigger) events from one processor subsystem/module to another. For example, a given subsystem A can be programmed to generate a debug event, which can then be exported as a global trigger across the device. Another subsystem B can be programmed to be sensitive to the trigger line input and to generate an action on trigger detection.

Examples of debug events are: Processor entering debug state, watchpoint match, CS_PTM trigger, CT_TBR full, CT_TBR acquisition complete, and so forth.

Examples of debug actions are: Debug request generation, restart (Cortex-A15 synchronous run), interrupt request generation, start/stop trace, and so forth.

Subsystem cross-triggering is consolidated at the device level by the XTRIG module, which is embedded in the debug subsystem.

NOTE: XTRIG is not programmatically visible from the JTAG interface or any device processor. Thus, cross-triggering is programmed at the subsystem level.

29.4.2.1 MPU Subsystem Cross-Triggering

The MPU subsystem provides:

- Support for cross-triggering between MPU cores using CS_CTI_MPU_C0 and CS_CTI_MPU_C1, programmable through AXI bus accesses or by debugger from the CS_DAP APB bus directly
- CS_CTM_MPU matrix to carry cross-triggers
  - Between CS_CTI_MPU_C0 and CS_CTI_MPU_C1
  - Outside Cortex-A15 MPCore, to CS_CTM_S
- CS_CTI_S to collect trigger events from CS_STM and DAP_PC
- CS_CTM_S to combine the triggers from CS_CTI_S with system and MPU core triggers:
- Trigger interface from CS_CTM_S to debug subsystem

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- Support for global or synchronous run when both Cortex-A15 CPUs are halted
- Support for COMMTX/COMMRX routing through CS_CTI_MPU_C0 and CS_CTI_MPU_C1 to the interrupt line (MPU_IRQ_1 for CS_CTI_MPU_C0, MPU_IRQ_2 for CS_CTI_MPU_C1)
- Cross-triggering between CS_PTMs and CT_TBR:
  - CS_PTM can generate a trigger that can be used to stop CT_TBR data capture
  - CT_TBR can send buffer-full or acquisition-complete events to the CS_PTM

The MPU subsystem cross-triggering logic allows stopping one MPU core at debug event detection in the other MPU core. For example, a watchpoint detected by MPU_C0 can break MPU_C1 execution, and vice versa. This is also known as symmetric multiprocessor platform (SMP) debug and is supported through CS_CTI_MPU programming.

The MPU subsystem may export/import trace triggers events to/from the debug subsystem through the CoreSight SoC triggering channels:

- CS_PTM
- CS_STM
- CT_TBR
- CS_TPIU

Figure 29-2 highlights the cross-triggering scheme implemented at the MPU subsystem level. A debug event from either processor core can be programmed to have a specific debug action on the other core or drive a SoC trigger line and generate a debug action into another application subsystem or debug and trace component. In addition to that, a watchpoint capability is implemented in the MPU subsystem memory adapter (MA_MPU), thus allowing the user to track the MA transactions from/to external memory through trigger to any of the MPU cores. For more information, see Section 29.7, *MPU Memory Adaptor (MA_MPU) Watchpoint*..

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Figure 29-2. MPU Subsystem Cross-Triggering

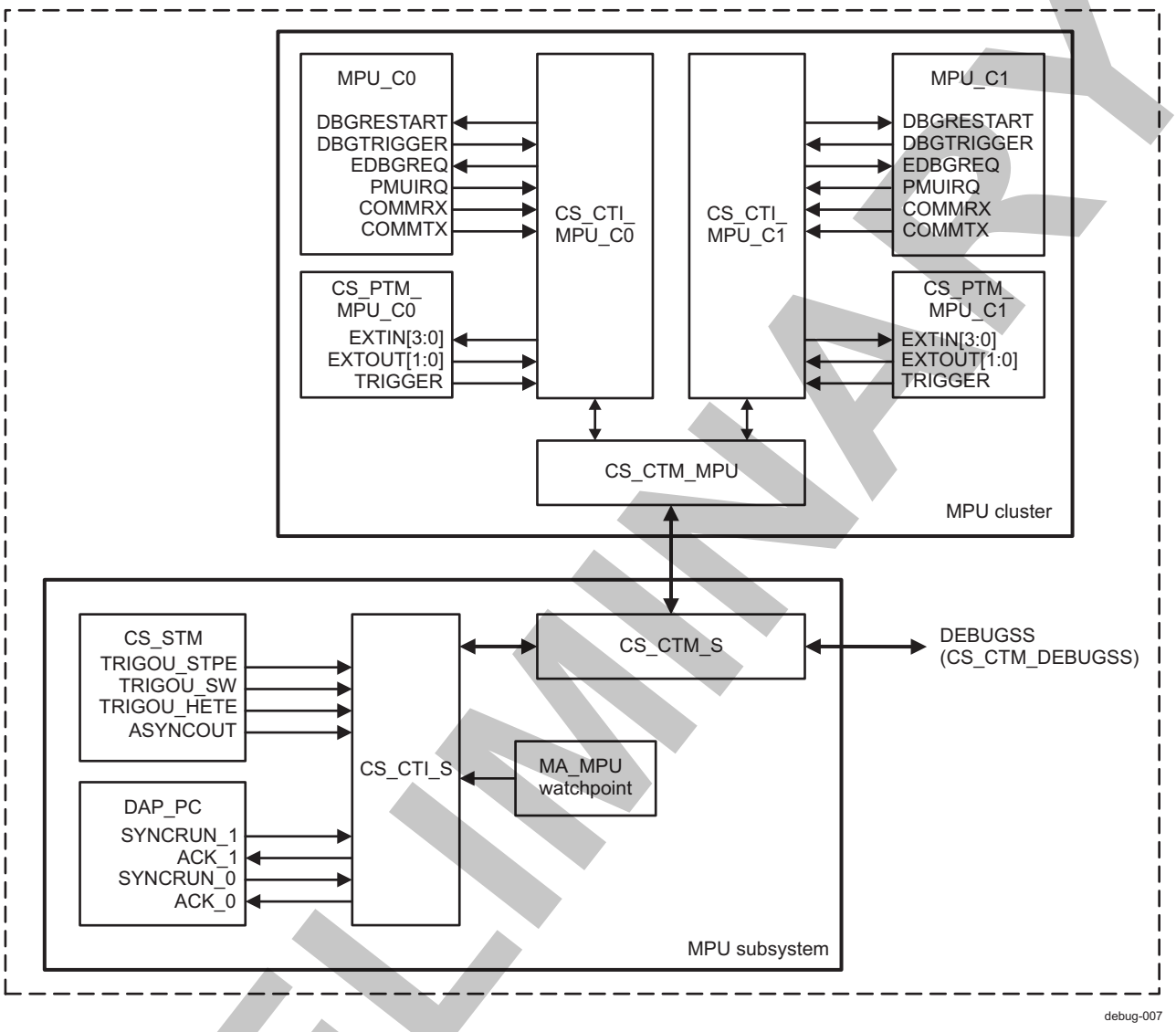

Table 29-12 and Table 29-13 summarize the CS_CTI_MPU connections inside the MPU cluster.

Table 29-12. CS_CTI_MPU Trigger Sources

CS_CTI_MPU Trigger Input CTITRIGIN[7:0]	Source Module	Source Module Output	Description
CTITRIGIN[0]	Cortex-A15 CPU	DBGTRIGGER	Debug state entered
CTITRIGIN[1]	Cortex-A15 CPU	PMUIRQ(1)	PMU interrupt
CTITRIGIN[3:2]	CS_PTM	EXTOUT[1:0]	CS_PTM debug resources reuse
CTITRIGIN[4]	Cortex-A15 CPU	COMMTX	Communication TX channel interrupt (TX channel is empty)
CTITRIGIN[5]	Cortex-A15 CPU	COMMRX	Communication RX channel interrupt (RX channel is full)
CTITRIGIN[6]	CS_PTM	TRIGGER	CS_PTM trigger
CTITRIGIN[7]	–	–	Tied low

(1) This signal is also routed to an INTC_MPU input (MPU_IRQ_131 for Cortex-A15 CPU0 PMU; MPU_IRQ_132 for Cortex-A15 CPU1 PMU).

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Table 29-13. CS_CTI_MPU Trigger Outputs

CS_CTI_MPU Trigger Output CTITRIGOUT[7:0]	Destination Module	Destination Module Input	Description
CTITRIGOUT[0]	Cortex-A15 CPU	EDBGREQ	Debug request (causes the processor to enter debug state)
CTITRIGOUT[4:1]	CS_PTM	EXTIN[3:0]	Trace trigger
CTITRIGOUT[5]	–	–	Unused, open
CTITRIGOUT[6]	INTC_MPU	MPU_IRQ_i[(1)]	CS_CTI_MPUi interrupt
CTITRIGOUT[7]	Cortex-A15 CPU	DBGRESTART	Debug restart (causes the processor to exit debug state)

(1) i = 1 for CS_CTI_MPU_C0; i = 2 for CS_CTI_MPU_C1.

Table 29-14 summarizes the mapping of the CS_CTM_MPU trigger channels.

Table 29-14. CS_CTM_MPU Trigger Channel Mapping

CS_CTM_MPU Trigger Channel	Type[(1)]	Mapped To
Channel 0	I/O	CS_CTI_MPU_C0
Channel 1	I/O	CS_CTI_MPU_C1
Channel 2	I/O	CS_CTM_S
Channel 3	I/O	unused

(1) I = Input; O = Output; I/O = bidirectional

Table 29-15summarize the CS_CTI_S connections inside the MPU subsystem.

Table 29-15. CS_CTI_S Trigger Inputs

CS_CTI_S Trigger Input CTITRIGIN[7:0]	Source Module	Source Module Output	Description
CTITRIGIN[1:0]	DAP_PC	SYNCRUN[1:0]	Debugger has requested a synchronous run directive
CTITRIGIN[2]	CS_STM	TRIGOUTSPTE	Stimulus port trigger
CTITRIGIN[3]	CS_STM	TRIGOUTSW	Write to trigger location
CTITRIGIN[4]	CS_STM	TRIGOUTHETE	Hardware event
CTITRIGIN[5]	CS_STM	ASYNCOUT	Alignment synchronization
CTITRIGIN[6]	MA_MPU watchpoint	MA_WP_TRIGGER	MA_MPU watchpoint trigger
CTITRIGIN[7]	–	–	Unused

Table 29-16 summarizes the mapping of the CS_CTM_S trigger channels.

Table 29-16. CS_CTM_S Trigger Channel Mapping

CS_CTM_S Trigger Channel	Type[(1)]	Mapped To
Channel 0	I/O	CS_CTM_MPU
Channel 1	I/O	CS_CTI_S
Channel 2	I/O	CS_CTM_DEBUGSS
Channel 3	I/O	Unused

(1) I = Input; O = Output; I/O = bidirectional

For more information about Cortex-A15 CPU, CS_CTI, and CS_PTM signals description, see the ARM *Cortex™-A15 Technical Reference Manual*.

29.4.2.2 Debug Subsystem Cross-Triggering

The debug subsystem implements two cross-triggering schemes:

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- TI cross-triggering scheme
- CoreSight cross-triggering scheme

The debug subsystem provides cross-triggering support in three different ways:

- XTRIG module (TI cross-trigger module) to support merge and distribution of TI asynchronous triggers (two channels per interface)
- CS_CTM_DEBUGSS (CoreSight cross-trigger matrix) to support merge and distribution of CoreSight triggers (four channels per interface) to CoreSight components inside and outside of the debug subsystem
- CT_CTA module (CTools cross-trigger adapter) to support conversion between TI asynchronous trigger format (two channels) and CoreSight handshake based asynchronous trigger format

This cross-triggering architecture of the debug subsystem allows it to provide the following features:

- Migration of a trigger originating from a CoreSight trigger source and ending at a TI trigger sink
- Migration of a trigger originating from a TI trigger source and ending at a CoreSight trigger sink
- Migration of a trigger originating from a CoreSight trigger source and ending in the debug subsystem at a CoreSight trigger sink using the four available CoreSight trigger channels
- Migration of a trigger originating from a CoreSight source in the debug subsystem to a CoreSight trigger sink outside the debug subsystem using the four available CoreSight trigger channels
- Support for routing CoreSight cross-triggers (from the MPU subsystem) to CoreSight modules within the debug subsystem:
  - CT_TBR
  - CS_TPIU
- Support for routing TI cross-triggers to CoreSight modules within the debug subsystem:
  - CT_TBR
  - CS_TPIU
- Support for routing input triggers from CT_TBR (buffer full, acquisition complete) outside of the debug subsystem

Figure 29-3 highlights the cross-triggering scheme implemented at the debug subsystem level.

Figure 29-3. Debug Subsystem Cross-Triggering

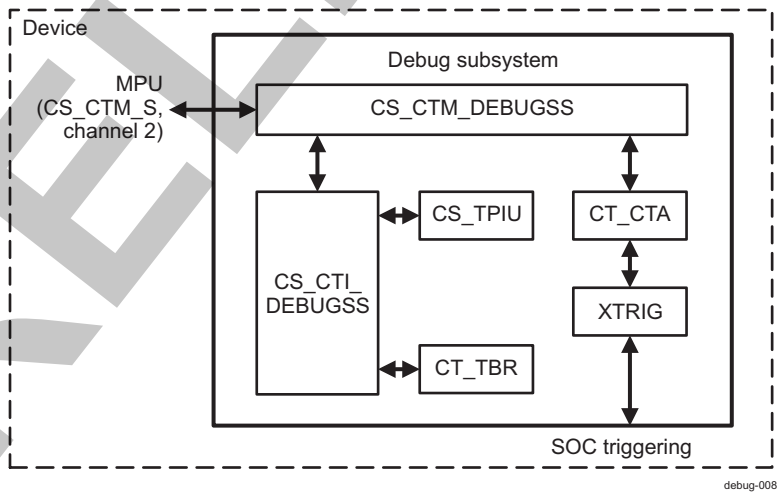

Table 29-17 and Table 29-18 summarize the CS_CTI_DEBUGSS connections inside the debug subsystem.

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Table 29-17. CS_CTI_DEBUGSS Trigger Sources

CS_CTI_DEBUGSS Trigger Input CTITRIGIN[7:0]	Source Module	Source Module Output	Description
CTITRIGIN[0]	–	–	Unused
CTITRIGIN[1]	–	–	Unused
CTITRIGIN[2]	CT_TBR	ACQCOMP	Acquisition complete
CTITRIGIN[3]	Warm reset	–	Warm reset detection(1)
CTITRIGIN[7:4]	–	–	Unused

(1) Can be used to halt the trace formatter in CT_TBR or CS_TPIU to support a use case of stopping trace upon warm reset detection.

Table 29-18. CS_CTI_DEBUGSS Trigger Outputs

CS_CTI_MPU Trigger Output CTITRIGOUT[7:0]	Destination Module	Destination Module Input	Description
CTITRIGOUT[0]	–	–	Unused
CTITRIGOUT[1]	–	–	Unused
CTITRIGOUT[2]	CS_TPIU	TRIGIN	Trigger processing
CTITRIGOUT[3]	CS_TPIU	FLUSHIN	Flush operation
CTITRIGOUT[4]	CT_TBR	TRIGIN	Trigger processing
CTITRIGOUT[5]	CT_TBR	FLUSHIN	Flush operation
CTITRIGOUT[7:6]	–	–	Unmapped

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29.4.2.3 SoC-Level Cross-Triggering

Table 29-19 summarizes the device cross-triggering capabilities.

Table 29-19. XTRIG

Subsystem	Module		MPU Cores	CS_PTM/CT_TBR	Cortex-M4	Cortex-M4	Target Core	DSP-C64x	IVA ARM968	IVA ARM968	HWA	SMSET	PMI	CMI	NOC_SC	OCP_WP_NOC	EMU0/EMU1
		Trigger Input / Trigger Source	✓	✓	✓	✓	–	✓	✓	✓	–	✓	✓	✓	✓	✓	✓
MPU	MPU Cores	✓		✓	✓	✓	–	✓	✓	✓	–	✓	✓	✓	✓	✓	
	CS_PTM / CT_TBR	✓	✓		✓	✓	–	–	–	–	–	✓	✓	✓	✓	✓	–
IPU	Cortex-M4	✓	✓	–		✓	–	✓	✓	✓	–	✓	✓	✓	✓	✓	–
	Cortex-M4	✓	✓	–	✓		–	✓	✓	✓	–	✓	✓	✓	✓	✓	–
ABE subsystem	Target Core	–	–	–	–	–		–	–	–	–	–	–	–	–	–	–
DSP subsystem	C64x	✓	✓	–	✓	✓	–		✓	✓	✓	✓	✓	✓	✓	✓	✓
IVA subsystem	ARM968 ICONT	✓	✓	–	✓	✓	–	✓		✓	✓	✓	✓	✓	✓	✓	✓
	ARM968 VDMA	✓	✓	–	✓	✓	–	✓	✓		✓	✓	✓	✓	✓	✓	✓
	HWA	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–
	SMSET	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–
Power manager	PMI	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–
Clock manager	CMI	–	–	–	–	–	–	–	–	–	–	–	–		–	–	–
SoC	NOC_SC	–	–	–	–	–	–	–	–	–	–	–	–	–		–	–
	OCP_WP_NOC	✓	✓	✓	✓	✓	–	✓	✓	✓	–	✓	✓	✓	✓		✓
	EMU0, EMU1	✓	✓	✓	✓	✓	–	✓	✓	✓	–	✓	✓	✓	✓	✓	

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NOTE: The following modules support only trigger inputs:

- IVA hardware accelerators
- IVA SMSET
- PMI
- CMI
- NOC_SC

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29.4.3 Suspend

The device supports a suspend feature, which provides a way to stop a closely coupled hardware process running on a peripheral-IP when the host processor enters debug state. The suspend mechanism is important for debug to ensure that peripheral-IPs operate in a lock-step manner with a host controller processor.

An entry is provided for each peripheral-IP that must consider the suspend signals from a number of processors (MPU or DSP). For each peripheral-IP, sensitivity to the suspend signals is defined within two possibilities (and so coded using 1 bit):

- Peripheral-IP is sensitive to the suspend line request.
- Peripheral-IP ignores the suspend line request.

For more information about how to program the sensitivity, see the corresponding peripheral-IP TRM chapter.

29.4.3.1 Debug Aware Peripherals and Host Processors

Table 29-20 lists the mapping of the device processors to the suspend control input lines.

Table 29-20. Debug Subsystem Suspend Input Lines

Suspend Input Line	Host Processor
0	DSP
1	IVA ICONT1
2	IVA ICONT2
3	IPU_C0
4	IPU_C1
5	MPU_C0
6	MPU_C1

Table 29-21 lists the mapping of the device peripheral-IPs to the suspend control output lines.

Table 29-21. Debug Subsystem Suspend Output Lines

Suspend Output Line	Peripheral-IP Module
0	KBD
1	MCBSP1 (ABE)
2	MCBSP2 (ABE)
3	MCBSP3 (ABE)
4	WD_TIMER3 (ABE)
5	TIMER5 (ABE)
6	TIMER6 (ABE)
7	TIMER7 (ABE)
8	TIMER8 (ABE)
9–15	Reserved
16	TIMER1
17	TIMER2
18	TIMER3
19	TIMER4
20	TIMER9
21	TIMER10
22	TIMER11
23	Reserved
24	HSI
25	I2C1

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Table 29-21. Debug Subsystem Suspend Output Lines (continued)

Suspend Output Line	Peripheral-IP Module
26	I2C2
27	I2C3
28	I2C4
29	Reserved
30	DMA_SYSTEM
31	COUNTER_32K
32	Statistics collector
33	I2C5
34–36	Reserved
37	WD_TIMER2

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29.5 Power, Reset, and Clock Management Debug Support

The global PRCM module implements facilities to support debug across power and clock domain cycles. The debugger can control or get the status of each power and clock domain associated with an ICEPick secondary TAP.

ICEPick provides a set of directives allowing the debugger to:

- Get visibility on the associated power and clock domains state. This includes:
  - Current power setting indicating whether the power domain is on or off
  - Loss of power detected since the software last checked the status
  - Current clock setting indicating whether the clock domain is on or off
  - Sleep desired (PM and CM indicate that the debug settings in ICEPick are changing the application state. If it were not for the ICEPick controls, the power or clock would be turned off.)
  - Subsystem reset state
  - Subsystem has entered a debug state that requires the attention of the host debug software.
- Override power/clock control settings to wake up a power or clock domain or to prevent a power or clock domain from going to sleep once it is in ACTIVE state
- Assert/block/extend reset; release from extended reset (WIR)

ICEPick handles debug power management at the device level. In addition, the device implements a second level of debug power management through the DAP_PC module integrated in the MPU subsystem, which provides the same capabilities as ICEPick for the two Cortex-A15 CPUs. Each Cortex-A15 CPU core is in its own independent power domain, which DAP_PC manages. The hierarchical debug power-management approach provided by DAP_PC at the subsystem level and by ICEPick at the device level ensures a theoretically independent debug capability for each Cortex-A15 CPU core.

NOTE: The debugger must properly sequence global ICEPick and local DAP_PC commands:

- To force clocks/power:
  1. The debugger must first force it for the MPU subsystem at the ICEPick level.
  2. The debugger must then force it for a specific Cortex-A15 CPU at the DAP_PC level.
- To release clocks/power:
  1. The debugger must first release it for a specific Cortex-A15 CPU at the DAP_PC level.
  2. The debugger must then release the MPU subsystem controls at the ICEPick level.

29.5.1 Power and Clock Management

29.5.1.1 Power and Clock Control Override From Debugger

The debugger can override the application software power and clock management settings through the ICEPick module. It can configure ICEPick to force a domain active or prevent it from going to sleep once it is active. This can be achieved through the following debugger directives:

- FORCEACTIVE
- INHIBITSLEEP

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29.5.1.1.1 Debugger Directives

29.5.1.1.1.1 FORCEACTIVE Debugger Directive

To ensure that the subsystem debug registers can always be accessed, regardless of the application power-management scenarios, a FORCEACTIVE directive can be issued through the debugger along the entire debug session. From an application standpoint, the system state, status, and timing are preserved, but the subsystem power domain is never shut down. Therefore, the emulation setup is preserved across power transitions, regardless of where the debug hardware is implemented.

If the debugger connects and the subsystem were previously powered down, a FORCEACTIVE directive wakes up the system and allows the debugger to take control of the system.

29.5.1.1.1.2 INHIBITSLEEP Debugger Directive

The debugger can use the INHIBITSLEEP directive to keep a subsystem powered and clocked, even if the applicative settings request that this subsystem go to sleep. Contrary to the FORCEACTIVE directive, the INHIBITSLEEP command does not wake up a subsystem that is already powered down by the application.

The typical use of the INHIBITSLEEP directive is to prevent power and clock transitions on the subsystem during a debug session. In this situation, when the applicative scenario initiates a transition, the transition does not take place, but from an applicative point of view the subsystem is not accessible.

29.5.1.1.2 Intrusive Debug Model

The use of debugger directives is intrusive from the standpoint of the power and clock controls, because they affect the power-management behavior of the application.

29.5.1.2 Debug Across Power Transition

29.5.1.2.1 Nonintrusive Debug Model

To preserve the power-management behavior of the device and allow the subsystem power and clock to be switched off by application software, the subsystem TAP must be disconnected from the ICEPick scan chain. The subsystem is then completely ignored by the debugger and the host-to-target communication is no longer affected by the state of the subsystem power and clocks. The debugger can still be informed that the disconnected subsystem entered the debug state by polling the Debug Attention status bit from ICEPick. The debugger can then insert the TAP, take control of the subsystem power and clock, and examine the system state.

This debug model is nonintrusive, because it allows the power-management behavior of the application to be preserved.

29.5.1.2.2 Debug Context Save and Restore

29.5.1.2.2.1 Debug Context Save

The device partitioning is such that not all the debug components are mapped to an always-on domain. Typically, the programmer wants the debug setup to be preserved along a debug session, including subsystem power cycling. When debug registers are memory mapped and not implemented within the emulation power domain, the application software must save the state of the debug registers before going to sleep and restore them upon wakeup.

29.5.1.2.2.2 Debug Context Restore

When the application software performs a context restore, it must be able to write to all the debug registers to restore their contents, regardless of the previous ownership. After subsystem power domain ramp up, the debug resources are in the available state, and ownership is restored. The debug context save and restore sequences are protected. All debug functionality is disabled and debugger accesses are blocked.

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29.5.2 Reset Management

The debugger can take control of the system reset for each subsystem through ICEPick. The debugger can configure ICEPick to assert, block, or extend the subsystem reset.

29.5.2.1 Debugger Directives

29.5.2.1.1 Assert Reset

The debugger can program ICEPick to generate a subsystem reset request to the device reset management module. The debugger reset event is then merged with system reset events.

29.5.2.1.2 Block Reset

The debugger can program ICEPick to request the device reset management module to block an unsafe application system or subsystem reset event.

A reset originated by some safe reset sources cannot be blocked by the debugger.

29.5.2.1.3 Wait-In-Reset

WIR mode is latched from boot mode (see Section 29.3.2, *Boot Modes*) and allows the user to hold a secondary TAP module in reset state when a reset is applied (and thus, extend the reset). This mode lets the user control the following system level activities:

- Gain emulation control of any processor in a power domain at POR
- Capture and extend system-generated functional resets while running (under emulation control or not)
- Hold an entire power domain in reset until emulation control of the subsystem can be established
- Stall the entire system while reset is extended to a power domain
- Reset extension is visible external to the power domain.
- Debug execution of code from the first cycle of execution
- Prevent processor execution of random instructions in uninitialized program memory at power up
- Download code before any code execution takes place
- Coordinate debug initialization across multiple cores before code execution begins

WIR mode extends only the processor reset. During reset extension, the debugger can still access modules such as L2 memory and MMU, even if they are embedded in the device subsystem affected by WIR.

When the debugger task is complete, the DTC releases the subsystem reset by programming the corresponding ICEPick TAP control register.

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29.6 Performance Monitoring

29.6.1 MPU Subsystem Performance Monitoring

29.6.1.1 Performance Monitoring Unit

The Cortex-A15 processor includes a PMU that enables events, such as cache misses and instructions executed, to be counted over a period of time. The PMU provides six counters to gather statistics about the operation of the processor and memory system. Each counter can count any of the events available in Cortex-A15. Upon counter overflow, PMU can generate an interrupt on its PMUIRQ output. This interrupt signal is mapped to the CTITRIGIN[1] input and routed to an INTC_MPU input (MPU_IRQ_131 for Cortex-A15 CPU0 PMU; MPU_IRQ_132 for Cortex-A15 CPU1 PMU).

The Cortex-A15 PMU outputs 52 events (PMUEVENT[51:0]) to CS_PTM (see Table 29-22).

Table 29-22. PMU Events

PMU Event	Description
0	Software increment
1	Instruction fetch that causes a refill
2	Instruction fetch that causes a TLB refill
3	Data read or write operation that causes a refill
4	Data read or write operation that causes a cache access
5	Data read or write operation that causes a TLB refill
6	Data read architecturally executed
7	Data write architecturally executed
8,9	Number of instructions renamed: b00 = No instructions renamed b01 = One instruction renamed b10 = Two instructions renamed
10	Exception taken
11	Exception return architecturally executed
12	Change to context ID retired
13	Software change of PC
14	Immediate branch architecturally executed
15	Number of predictable function returns
16	Unaligned access architecturally executed
17	Branch mispredicted or not predicted
18	Branches or other change in program flow
19	Java byte code executed
20	Software Java byte code executed
21	Jazelle® backward branches executed
22	Coherent line fill request that misses in other uniprocessors
23	Request for coherent line fill that hits in other uniprocessors
24	Instruction cache dependent stalls
25	Data cache dependent stalls
26	TLB miss dependent stalls
27	STREX passed
28	STREX failed
29	Data eviction
30	Issue does not dispatch any instruction.
31	Issue is empty.
32	Main execution unit pipe
33	Second execution unit pipe

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Table 29-22. PMU Events (continued)

PMU Event	Description
34	Load/store pipe
35, 36	Number of floating-point instructions renamed: b00 = No floating-point instruction renamed b01 = One floating-point instruction renamed b10 = Two floating-point instructions renamed
37, 38	Number of Neon instructions renamed: b00 = No Neon instruction renamed b01 = One Neon instruction renamed b10 = Two Neon instructions renamed
39	PLD stall
40	Write stall
41	Instruction main TLB miss stall
42	Data main TLB miss stall
43	Instruction micro TLB miss stall
44	Data micro TLB miss stall
45	DMB stall
46	Integer core clock enabled
47	Data engine clock enabled
48	ISB
49	DSB
50	DMB
51	External interrupt

For more information about Cortex-A15 PMU, see the *ARM Cortex-A15 Technical Reference Manual*.

29.6.1.2 L2 Cache Controller

The MPU subsystem includes 2 MiB of L2 cache (L2CACHE_MPU) and L2 cache controller (L2CACHE_CTRL_MPU). The L2 cache controller includes logic to support cache event monitoring.

Table 29-23 summarizes the L2 cache events.

Table 29-23. L2 Cache Events

Event	Event Description
0	Eviction of a line from the L2 cache
1	Data read hit in the L2 cache
2	Data read lookup to the L2 cache. Subsequently results in a hit or miss.
3	Data write hit in the L2 cache
4	Data write lookup to the L2 cache. Subsequently results in a hit or miss.
5	Data write lookup to the L2 cache with Write-Through attribute. Subsequently results in a hit or miss.
6	Instruction read hit in the L2 cache
7	Instruction read lookup to the L2 cache. Subsequently results in a hit or miss.
8	Prefetch line-fill sent to L3
9	Allocation into the L2 cache caused by a write (with Write-Allocate attribute) miss

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The L2 cache controller implements two 32-bit event counters. The L2 cache controller can be configured to generate interrupts on error conditions or event counter overflow or increment. The L2 cache controller interrupt is routed to MPU_IRQ_0. When an interrupt occurs, software can look at the relevant interrupt status register to determine the source of the interrupt.

29.6.2 IPU Subsystem Performance Monitoring

29.6.2.1 Subsystem Counter Timer Module

The IPU subsystem includes a subsystem counter timer module (SCTM), which is embedded in shared cache and provides additional data to the user timing or profiling capability. SCTM integrates eight profiling counters that collect:

- Forty-four shared cache events
- Four sleep/deep-sleep events from Cortex-M4 cores (one sleep and one deep sleep event per core)

Table 29-24 describes the repartition of the IPU SCTM counters.

Table 29-24. IPU SCTM Counters Repartition

Counters	Features
0–1	Timer and event
2–3	64-bit chained + shadowing
4–5	64-bit chained + shadowing
6–7	Event

29.6.2.2 Cache Events

Table 29-25 summarizes the SCTM events for the IPU subsystem.

Table 29-25. SCTM Events for IPU Subsystem

Input Index	Event Description
1	Cache locks
2	Cache line replacements
3	Cache evictions
4	Cache maintenance operations (slave 0)
5	Cache maintenance operations (slave 1)
6	Cache maintenance operations (slave 2)
7	Cache maintenance operations (slave 3)
8	Cache OCP access (slave 0)
9	Cache OCP access (slave 1)
10	Cache OCP access (slave 2)
11	Cache OCP access (slave 3)
12	Cacheable access (slave 0)
13	Cacheable access (slave 1)
14	Cacheable access (slave 2)
15	Cacheable access (slave 3)
16	Cache bank conflicts (slave 0)
17	Cache bank conflicts (slave 1)
18	Cache bank conflicts (slave 2)
19	Cache bank conflicts (slave 3)
20	Cache allocations
21	Cache write buffer accesses (slave 0)
22	Cache write buffer accesses (slave 1)

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Table 29-25. SCTM Events for IPU Subsystem (continued)

Input Index	Event Description
23	Cache write buffer accesses (slave 2)
24	Cache write buffer accesses (slave 3)
25	Cache line fills (slave 0)
26	Cache line fills (slave 1)
27	Cache line fills (slave 2)
28	Cache line fills (slave 3)
29	Cache write fills (slave 0)
30	Cache write fills (slave 1)
31	Cache write fills (slave 2)
32	Cache write fills (slave 3)
33	Cache read fills (slave 0)
34	Cache read fills (slave 1)
35	Cache read fills (slave 2)
36	Cache read fills (slave 3)
37	Cache misses (slave 0)
38	Cache misses (slave 1)
39	Cache misses (slave 2)
40	Cache misses (slave 3)
41	Cache hits (slave 0)
42	Cache hits (slave 1)
43	Cache hits (slave 2)
44	Cache hits (slave 3)
45	IPU_C1 deep sleep
46	IPU_C1 sleep
47	IPU_C0 deep sleep
48	IPU_C0 sleep

NOTE: Input index [0] is reserved for free-running subsystem clock (used for total cycle profiling).

29.6.3 DSP Subsystem Performance Monitoring

29.6.3.1 Subsystem Counter Timer Module

The DSP subsystem includes an SCTM, which is embedded in the DSP megamodule and provides additional data to the user timing or profiling capability. SCTM integrates eight profiling counters that collect L1 and L2 events.

Table 29-24 describes the repartition of the DSP SCTM counters.

Table 29-26. DSP SCTM Counters Repartition

Counters	Features
0–1	Timer and event
2–7	Event (no chaining)

29.6.3.2 L1 and L2 Events

Table 29-27 summarizes the SCTM events for DSP subsystem.

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Table 29-27. SCTM Events for DSP Subsystem

Event	Event Description
1	L1 Slave0 (program) tag hit
2	L1 Slave1 (data) tag hit
3	L1 Slave0 (program) tag miss
4	L1 Slave1 (data) tag miss
5	L1 Slave0 (program) fill buffer hit
6	L1 Slave1 (data) fill buffer hit
7	L1 Slave1 (data) write buffer access
8	L1 Allocation FIFO
9	L1 Slave0 (program) bank conflict
10	L1 Slave1 (data) bank conflict
11	L1 Slave0 (program) cached request
12	L1 Slave1 (data) cached request
13	L1 Slave0 (program) waiting for fill buffer
14	L1 Slave1 (data) waiting for fill buffer
15	L1 Slave0 (program) waiting for maintenance
16	L1 Slave1 (data) waiting for maintenance
17	L1 Eviction occurred
18	L1 Replacement occurred
19	L1 Allocation failed due to locked lines occurred
20	L2 tag hit
21	L2 tag miss
22	L2 fill buffer hit
23	L2 write buffer access
24	L2 allocation FIFO
25	L2 cached request
26	L2 waiting for fill buffer
27	L2 waiting for maintenance
28	L2 eviction occurred
29	L2 replacement occurred
30	L2 allocation failed due to locked lines occurred
31	Tied-off to 0

NOTE: Input index [0] is reserved for the free-running subsystem clock (used for total cycle profiling).

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29.7 MPU Memory Adaptor (MA_MPU) Watchpoint

The MPU subsystem implements a watchpoint allowing the user tracking the MA_MPU transactions from/to external memory.

The watchpoint can be programmed to generate a trigger when a MA_MPU transaction satisfies a set of user-defined attributes:

- Access within or outside an address region
- Access type (instruction, data, read, write)
- Transaction target (on-chip, memory channel, chip select)
- Qualifier
- Transaction originating from a specific core
- Specific transaction followed by memory barrier (DSB, DMB)
- Memory barrier (DSB, DMB) followed by specific transaction

When the MA_MPU transaction attributes match the debug use case setup, the MPU debug logic captures the transaction data and associated qualifiers:

- Read or write data (128-bit) for the specific beat of the burst
- Address (MSB field)
- MReqInfo (19-bit)
- Byte enables
- Burst type
- Burst length
- Target

When the MA_MPU watchpoint is configured to track memory barriers in order to investigate potential ordering issues, the debugger will report:

- Attributes of the transaction immediately following the memory barrier
- Attributes of the matching transaction chained to the memory barrier

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29.8 Processor Trace

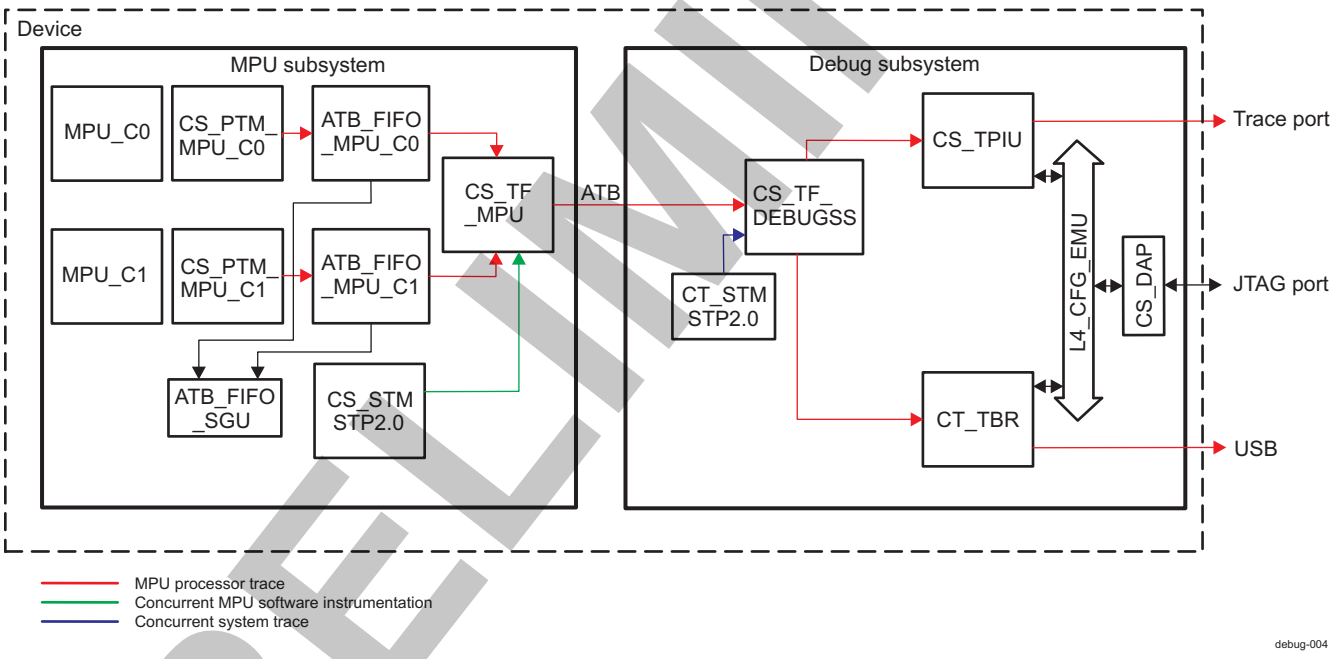
The device supports only Cortex-A15 (MPU) trace. The main MPU trace characteristics are:

- Program trace only (no data trace)
- Separate CS_PTM for each MPU core
- Three exclusive trace sinks:
  - CS_TPIU – trace exported to an external trace receiver
  - CT_TBR (buffer mode) – trace stored into on-chip buffer
  - CT_TBR (system bridge mode) – trace exported through USB
- Trace can be optionally:
  - Cycle accurate useful for profiling sections of code
  - Interleaved dynamically between the two MPU cores by CS_TF_MPU

NOTE: Depending on use case, the device may not be able to interleave two cycle accurate traces without overflow (bandwidth restriction).

Figure 29-4 shows an overview of the processor trace flow.

Figure 29-4. Processor Trace Flow



29.8.1 MPU Trace Export

The debug subsystem implements three exclusive trace sinks:

- CS_TPIU
- CT_TBR (buffer mode)
- CT_TBR (system bridge mode)

Two MPU trace streams are supported, one per MPU core. The two MPU cores program traces are exported to the PD_EMU domain (through asynchronous bridges) and then interleaved by the CS_TF_MPU.

A concurrent software instrumentation flow from the local CS_STM component (STP 2.0) can also be interleaved with the MPU program traces.

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Two ATB_FIFO modules (ATB_FIFO_MPU_C0 and ATB_FIFO_MPU_C1) are implemented in the trace path between the Cortex-A15 CPUs and the CS_TF_MPU module. The ATB_FIFO allows concurrent trace capture and export. It provides buffering in the trace export path and therefore allows absorbing peaks of trace data. The depth of the ATB_FIFOs is 16 entries.

The CS_TF_MPU sends the MPU trace (or CS_STM software instrumentation) to a trace funnel in the debug subsystem (CS_TF_DEBUGSS) through a single ATB interface. The CS_TF_DEBUGSS redirects the MPU trace to the three exclusive trace sinks.

NOTE: It is strongly recommended to disable trace sinks not in use when generating trace to an in-use trace sink to eliminate undesirable throughput throttling effects.

Besides the ATB_FIFOs, the MPU subsystem also instantiates an ATB_FIFO statistics gathering unit (ATB_FIFO_SGU) which provides silicon and presilicon characterization information of ATB_FIFO. The FIFO_LEVEL_OUT output of ATB_FIFO, which gives visibility of the number of used entries, is used for the statistics gathering. ATB_FIFO may be full under the following conditions:

- Arbitration collisions in the trace funnel when more than one ATB trace stream is being generated at the same time (tracing of multiple CPUs simultaneously)
- Trace sink does not have the bandwidth to meet peak bandwidth demands from the trace generator on a single ATB trace stream

The following statistics are gathered per ATB_FIFO:

- Peak utilization depth of the FIFO
- Number of consecutive cycles that FIFO level is at or above the programmable FIFO threshold when there is an ATB command pending
- Number of ATB bus stall cycles

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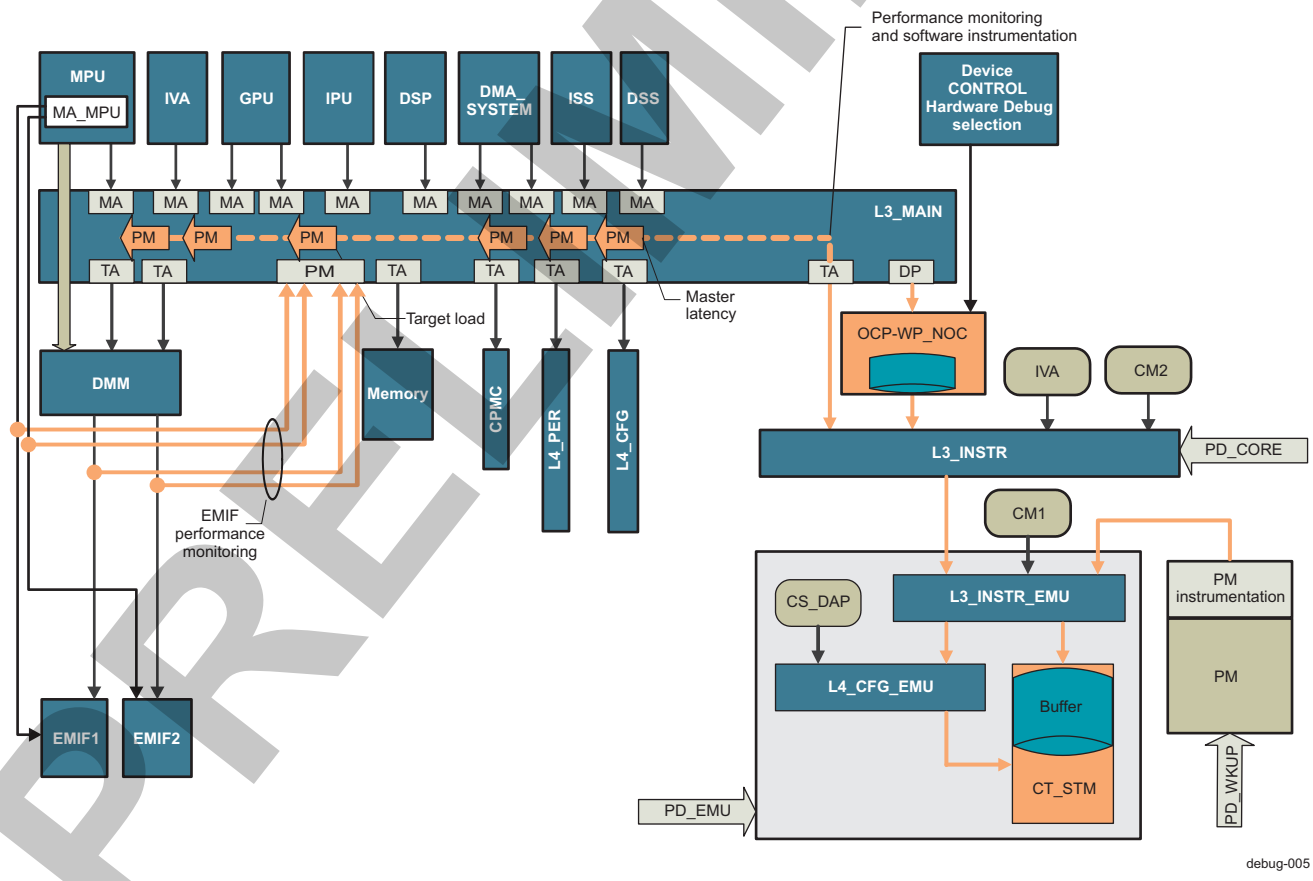
29.9 System Instrumentation

The device supports the following system instrumentation features:

- Real-time software trace
  - MPU software instrumentation via CS_STM (STP2.0) (see Section 29.9.3.1, *MPU Software Instrumentation*)
  - SoC software instrumentation via CT_STM (STP2.0) (see Section 29.9.3.2, *SoC Software Instrumentation*)
- OCP watchpoint
  - OCP target traffic monitoring (see Section 29.9.4.1, *OCP Target Traffic Monitoring*)
  - SoC events trace (see Section 29.9.4.2, *Messages Triggered from System Events*)
  - DMA transfer profiling (see Section 29.9.4.3, *DMA Transfer Profiling*)
- Statistics collector
  - Target load monitoring (see Section 29.9.6.1, *Target Load Monitoring*)
  - Master latency monitoring (see Section 29.9.6.2, *Master Latency Monitoring*)
- HWA load monitoring (see Section 29.9.5, *IVA Pipeline*)
- PM events trace (see Section 29.9.7, *PM Instrumentation* [PMI])
- CM events trace (see Section 29.9.8, *CM Instrumentation* [CMI])

Figure 29-5 is an overview of the device system instrumentation framework.

Figure 29-5. System Instrumentation Framework



29.9.1 MIPI STM (CT_STM)

CT_STM is a trace module that aids in software debugging. The main features of this module are:

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- Implements MIPI STP protocol (rev 1.0 for PTI export; rev 2.0 for ATB export) with the following characteristics:
  - Highly optimized for software-generated traces
  - Automatic timestamping of messages
  - Support for 8-, 16-, and 32-bit data types
- Collects the following information:
  - Software messages
  - Hardware instrumentation trace from hardware agents:
    - OCP_WP_NOC
    - PMI
    - CMI
    - SMSET
    - L3 NoC statistics collectors
- Supports the following trace export paths:
  - Parallel Trace Interface (PTI) export - directly to an external trace receiver
  - ATB export - to CS_TPIU or CT_TBR
- Available in 1-, 2-, or 4-pin mode with single- or dual-edge clock, depending on the trace bandwidth requirements and characteristics of the trace receiver
- Dedicated 128 × 48-bit FIFO buffer

A maximum of 255 different bus masters can be connected to the STM trace port through a bus arbiter. STP recognizes two distinct modes of tracing (software and hardware types), which use slightly different message combinations to output different types of data. The bus masters can be configured for either type to optimize the system for the different types of trace data.

29.9.2 System Trace Export

29.9.2.1 CT_STM PTI Export

System trace can be exported to an external trace receiver through the PTI of the CT_STM module. To achieve this, the debugger or application software must ensure to program the DRM module properly (that is, according to Table 29-37). The messages are encoded as defined by MIPI STP-1.0.

The CT_STM has a configurable export width of 1, 2, or 4 data (STM_DATA) pins plus a dedicated export clock (STM_CLK). The CT_STM can operate in DDR or SDR mode.

The device system trace does not make use of CT_TBR for buffering when the trace stream is exported to an external trace receiver through the PTI. The CT_STM implementing a dedicated buffer allows a CS_PTM trace to be concurrently captured into CT_TBR.

29.9.2.1.1 CT_STM Trace Export Clock Configuration

The CT_STM trace export clock is derived from DPLL_DEBUGSS output clock.

The CT_STM trace export frequency can be tuned independently of the CS_TPIU trace export frequency.

The CT_STM trace capture clocking is restricted to the L3_INSTR_EMU interconnect clock.

Table 29-28 shows possible CT_STM clock configurations. The following equations apply:

- DPLL_DEBUGSS output clock frequency when locked = 2 × [M / (N+1)] × SYS_CLK frequency.
- STM_CLK frequency = DPLL_DEBUGSS frequency / 2 × (M5 +1).

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Table 29-28. STM_CLK Frequency

DEBUGSS Clock Source	SYS_CLK Frequency, MHz	DPLL_DEBUGSS M / N	DPLL_DEBUGSS Frequency, GHz	HS_DIV Factor	CS_TPIU (2x)	STM_CLK, MHz
SYS_CLK	38.4	125/5	1.6	M5 = 7	2	100
		75/3	1.44	M5 = 7		90
		125/3	2.4	M5 = 11		100

29.9.2.2 CT_STM ATB Export

If a trace receiver cannot be attached to the device, or relevant CT_STM trace port pins are unavailable for a particular reason, the user can configure the CT_STM module to redirect the STP trace stream as an ATB stream to the CS_TPIU or CT_TBR and enable local timestamp. This is accomplished by outputting a local timestamp granularity (LTSG) message, which is a TI addition to the MIPI standard messages.

NOTE: For CT_STM timestamps when output to the ATB interface, the timestamp (TS) field is no longer the CT_STM FIFO depth, but is the time from the previous message.

Granularity is a function of the instrumentation port clock frequency.

29.9.2.3 Trace Streams Interleaving

Two levels of interleaving system instrumentation flows and arbitrating between instrumentation masters are implemented:

- CORE L3 instrumentation interconnect interleaves data coming from the following bus masters:
  - OCP_WP_NOC
  - L3 NoC statistics collectors, or software instrumentation (interleaving at the L3 level)
  - CMI2
  - IVA SMSET and ARM968 (software instrumentation)
- EMU L3 instrumentation interconnect interleaves data coming from the following bus masters:
  - CORE L3 instrumentation interconnect
  - CMI1
  - PMI

29.9.3 Software Instrumentation

29.9.3.1 MPU Software Instrumentation

The CS_STM embedded in the MPU subsystem provides extended stimulus port registers designated to be accessible by software with minimum instrumentation cycles overhead.

Each extended stimulus port occupies 256 consecutive bytes in the memory map and is write-only. Up to 64K instrumentation channels are available at MPU level.

The CS_STM supports "guaranteed" or invariant timing transactions:

- Guaranteed transactions are guaranteed to be traced. This might involve stalling the MPU core to ensure the transaction is accepted by the CS_STM.
- Invariant timing transactions are not guaranteed to be traced. These transactions take an invariant amount of time regardless of the state of the CS_STM.

The CS_STM implements tracing of software writes to its stimulus ports using a dedicated AXI slave interface. In addition to the AXI interface, the CS_STM provides a hardware event input interface (HWEVENTS[31:0]). The HWEVENTS[31:0] input bus is connected to the MPU hardware debug observability signals going out to the MPU hardware debug port (MPUHWDBGOUT[31:0]). This enables any of the signals observed on MPUHWDBGOUT[31:0] to act as a hardware event to the CS_STM. The

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CS_STM can be programmed to generate a debug packet on a rising edge transition on any signal of the HWVENTS[31:0] input bus. Because some of the signals mapped on the MPUHWDBGOUT[31:0] bus are active low, a 32-bit programmable register – MPU.STM_HWEVENTS_INV, is implemented for polarity inversion. Each bit of MPU.STM_HWEVENTS_INV when set to 0x1 inverts the polarity of the corresponding signal of MPUHWDBGOUT[31:0] going to HWEVENTS[31:0]. This programmable register is part of the WUGEN_MPU address map (see Section 4.4.10, *WUGEN_MPU Registers*, in Chapter 4, *Dual Cortex-A15 MPU Subsystem*, for its description).

NOTE: The MPUHWDBGOUT[31:0] signals can be routed to the hw_dbg[31:0] device pads through various hardware debug observability MUXes controlled by device control module (CTRL_MODULE). For more information, see Section 18.4.11, *Hardware Observability*, in Chapter 18, *Control Module*.

To save power, the output port can be gated off (to all zeros) by setting the CTRL_MODULE. CONTROL_HWOBS_CONTROL[0] HWOBS_MACRO_ENABLE bit to 0x0. Ungated version of MPUHWDBGOUT[31:0] (not gated with CTRL_MODULE. CONTROL_HWOBS_CONTROL[0] HWOBS_MACRO_ENABLE) is sent to HWEVENTS[31:0] input of STM so each of these signals can generate a debug packet on the trace port.

The message structures in STP-2.0 are optimized to provide an efficient transport.

29.9.3.2 SoC Software Instrumentation

The CT_STM module embedded in the debug subsystem provides a flexible interface for trace instrumentation.

The device provides support for real-time software trace through user-defined message writes to specific memory mapped register (MMR) locations. Software masters can transmit trace data from the operating system (OS) processes or tasks on 256 different channels, with each channel being defined by the software protocol implemented. The different channels can be used to group different types of data logically so that it is easy to filter out the data irrelevant to the ongoing debugging task. The message structures in STP-2.0 are optimized to provide an efficient transport for software data through the CT_STM module.

The software masters are:

- MPU subsystem
- DAP (for testing purpose)
- DSP subsystem
- IPU subsystem
- SDMA controller write port (DMA_SYSTEM_WR)
- IVA subsystem

Each software master has a master ID assigned to it.

Software messages can be interleaved with other hardware messages.

Software messages are intrusive and use both processor cycles and memory.

29.9.4 OCP Watchpoint

29.9.4.1 OCP Target Traffic Monitoring

The L3_MAIN interconnect provides six functional probes embedded and attached to the following L3_MAIN targets:

- GPMC
- L4_PER
- L4_CFG
- DMM_P1 (DMM target port 1)

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- DMM_P2 (DMM target port 2)
- OCMC_RAM

The probes output are muxed together and then sent to the L3_MAIN interconnect debug port. A component called OCP_WP_NOC is used to collect data from functional probes and then transmit captured data to the CT_STM module. The OCP_WP_NOC drives a Probe-ID signal to the L3_MAIN interconnect for probe selection. The probe selection is exclusive, meaning that interleaving is not possible.

The OCP_WP_NOC provides the following main features:

- Monitoring the OCP traffic originated by all initiators that can access the selected target where the probe is attached
- Filtering OCP monitored bus traffic by:
  - Address range
  - Initiator-ID (see Table 29-30)
  - Transaction type
  - Transaction qualifier
- Generating a trigger upon watchpoint match
- Starting and stopping OCP traffic monitoring upon:
  - WP address match
  - External trigger
- Profiling DMA transfers
- Generating hardware message upon system event
- OCP_WP_NOC messages can be interleaved with software messages
- Programming from:
  - Debugger
  - Application

NOTE: The OCP_WP_NOC is restricted to monitor request flow only.

Table 29-29 summarizes the OCP targets that can be monitored by the OCP_WP_NOC and their respective probe-ID.

Table 29-29. L3_MAIN Interconnect Functional Probe Mapping

Probe-ID	L3 OCP Target
000	Reserved
001	GPMC
010	L4_PER
011	L4_CFG
100	DMM_P1 (DMM target port 1)(1)
101	DMM_P2 (DMM target port 2)(1)
110	OCMC_RAM
111	Reserved

(1) Does not allow tracking MPU transactions routed through Memory Adapter and DMM.

The user can program the OCP_WP to extract the traffic from a specific set of initiators (maximum four master IDs). Table 29-30 lists the master ID reported by the L3_MAIN debug port for the device initiators.

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Table 29-30. Master ID Mapping (Debug View)

Master ID	Initiator
0x0	MPU
0x4	CS_DAP
0x8	DSP
0xC	IVA
0xD	IVA ICONT1 (software instrumentation)
0xE	IVA ICONT2 (software instrumentation)
0x10	ISS
0x11	IPU
0x12	FDIF
0x14	DMA_SYSTEM_RD
0x15	DMA_SYSTEM_WR
0x16	BB2D_P1
0x17	BB2D_P2
0x18	GPU_P1
0x19	GPU_P2
0x1C	DSS
0x24	HSI
0x28	MMC1
0x29	MMC2
0x2A	SATA
0x30	USB_HOST_HS
0x33	USB_OTG_SS

NOTE: For information about master ID values from a protection/error logging point of view, see , *Master NIU Identification*, in Chapter 14, *Interconnect*.

29.9.4.2 Messages Triggered from System Events

The OCP_WP_NOC can be programmed to export a message through the CT_STM upon detection of a system event (interrupt, DMA request, etc.). A bus of 16 system events pre-selected at SoC level from a large number of observable events is routed to the OCP_WP_NOC. This can be useful to determine interrupts latencies:

- Interrupt request traced through OCP_WP_NOC system event detection
- ISR boundary tracked either through CT_STM software trace or OCP_WP_NOC address range detection

The OCP_WP_NOC implements a dedicated port for the 16 system events that is connected to the device control module (CTRL_MODULE) hardware debug (hw_wkdbg[15:0] and hw_dbg[31:16]) output bus. The CTRL_MODULE handles the selection and exports a user-defined subset of the SoC observable events to the OCP_WP_NOC. The mapping of these events is presented in Chapter 18, *Control Module*.

29.9.4.3 DMA Transfer Profiling

The OCP_WP_NOC can be configured to profile DMA transfers. This feature provides to the user visibility on:

- DMA logical channel interleaving
- DMA channel ID
- DMA transfer duration (time stamp)
- DMA burst size

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- DMA reads
- DMA writes

When operating in this mode, the OCP_WP_NOC exports to CT_STM:

- DMA channel ID
- Burst size
- R/W

The CT_STM module encapsulates the information above in a compact STP message.

The address range filtering remains active but OCP address data are not encapsulated into the trace message to maximize CT_STM throughput.

29.9.5 IVA Pipeline

The device takes advantage of the system trace infrastructure to provide visibility to the user regarding IVA microtask sequencing. This is supported through a SMSET module instantiated in the IVA subsystem. The microtask boundaries are handled as generic events and encapsulated in STP messages with an event-ID and local timestamp and exported through the CT_STM module.

The IVA instrumentation scheme allows the user to understand microtask dependencies, hardware accelerators load balancing, and potential bottlenecks. DMA transfer boundaries are reported as IVA events. Software messages from ARM968 execution can be interleaved with IVA events.

29.9.6 NOC Statistics Collector

The L3_MAIN interconnect supports a built-in performance monitoring feature by implementing a statistics collector (NOC_SC) component, which computes traffic statistics within a user-defined window and periodically reports to the user through the CT_STM interface. Three NOC_SC instances are instantiated in the device:

- One statistics collector dedicated to SDRAM load monitoring – SC_SDRAM (see Section 29.9.6.1, *Target Load Monitoring*, for more information)
- Two statistics collectors dedicated to master latency monitoring – SC_LAT0 and SC_LAT1 (see Section 29.9.6.2, *Master Latency Monitoring* , for more information)

Statistics collectors (SDRAM and LAT0/1) can report:

- Average burst length in bytes/packet per sampling window
- Average throughput in bytes/cycle
- Percent link occupancy on the request link (for store transactions) during a sampling window
- Percent link occupancy on the response link (for load transactions) during a sampling window
- Percent arbitration conflict cycles on the request link
- Percent initiator busy cycles on the response link
- Histogram of payload length in bytes (for example, 0–16, 16–32, 32–128) each sampling window.
- Histogram of quality of service (QoS) metric for IVA initiator (for example, low priority, high priority) each sampling window.

The performance metrics are interleaved with software instrumentation data at the L3_MAIN interconnect level.

The performance monitoring probes implement three main functions:

- Events detection
- Transactions filtering
- Aggregation

The probes can be configured to detect the NTTP and OCP link events summarized in Table 29-31.

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Table 29-31. Performance Monitoring Events Detection

Link Event	NTTP	OCP	Definition
NONE	✓	✓	No event selected
ANY	✓	✓	Any clock cycles
TRANSFER	✓	✓	Word has been accepted by the receiver.
WAIT	✓	–	Transfer has been initiated but the transmitter currently has no data to send.
BUSY	✓	✓	Receiver applies flow control
PKT	✓	✓	Transfer of a new packet header
DATA	✓	✓	Transfer of a payload word
IDLES	✓	✓	No communication over the link
LATENCY	✓	–	Debug bit detection

The probes can be configured to filter the traffic based on the criteria summarized in Table 29-32.

Table 29-32. Performance Filtering Options

Probe Filtering Options	Comment
Master address	Mask and match
Slave address(1)	
UserInfo	
Read	
Write	
Error	
OCP address(2)	

(1) SC_LAT0/1 only
(2) SC_SDRAM only

The probes implement a user-defined set of counters that aggregate the events sampled by the detector and filtered according to the user setup.

NOTE: Statistics collectors counter values are accessible by application software.

Table 29-33 summarizes the performance probe aggregation modes.

Table 29-33. Aggregation Modes

Aggregation Mode	Description
FILTER_HIT	The counter increments by 1 when the filter hits.
MIN_MAX_HIT	The counter increments by 1 when the filter hits and the selected event information is within range. – Payload length (bytes) – Pressure value – Request/response latency (clock cycles)
EVT_INFO	The selected event information is added to the counter value when the filter hits. Payload length (bytes) Pressure value Request/response latency (clock cycles)
AND_FILTER	The counter increments by 1 when all unit filters hit.
OR_FILTER	The counter increments by 1 when at least one unit filter hits.
SUM_REQ_EVT	The counter sums the events from any request port.
SUM_RSP_EVT	The counter sums the events from any response port.
SUM_ALL_EVT	The counter sums the events from any port.
EXT_EVT	The counter increments by 1 when selected external event input signal is sampled high.

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29.9.6.1 Target Load Monitoring

The L3_MAIN interconnect implements five performance monitoring probes on LPDDR2 memory channels. The traffic statistics are computed within a user-defined window and periodically reported to the user through the CT_STM interface.

SC_SDRAM supports the following main features:

- Five probe inputs:
  - Probe 0 (128 bit-wide) – EMIF1_SYS
  - Probe 1 (128 bit-wide) – EMIF2_SYS
  - Probe 2 (128 bit-wide) – MA_MPU_P1
  - Probe 3 (128 bit-wide) – MA_MPU_P2
  - Probe 4 (64 bit-wide) – EMIF1_LL
- Eight 32-bit counters shared concurrently:
  - Counter 0 with two filters
  - Counter 1 with one filter
  - Counter 2 with two filters
  - Counter 3 with one filter
  - Counter 4 with one filter
  - Counter 5 with one filter
  - Counter 6 with one filter
  - Counter 7 with one filter
- Simple (with one element) or complex (with several elements) filters available
- Filtering according to:
  - Initiator of traffic
  - Access priorities
  - OCP address
- No latency counter. Only bandwidth measurement on this collector.
- 32-bit collecting window counter
- Dump identifier is 0x0 (tie-off value)
- Dumps frames at L3_MAIN interconnect slave address 0x19 (L3_INSTR)

Table 29-34 summarizes the SC_SDRAM configuration.

Table 29-34. SC_SDRAM Configuration

Counters	Min Max	Filter Elements	L3 Target				
Counter 0	Yes	2	EMIF1_SYS	EMIF2_SYS	MA_MPU_P1	MA_MPU_P2	EMIF1_LL
Counter 1	Yes	1	EMIF1_SYS	EMIF2_SYS	MA_MPU_P1	MA_MPU_P2	EMIF1_LL
Counter 2	Yes	2	EMIF1_SYS	EMIF2_SYS	MA_MPU_P1	MA_MPU_P2	EMIF1_LL
Counter 3	Yes	1	EMIF1_SYS	EMIF2_SYS	MA_MPU_P1	MA_MPU_P2	EMIF1_LL
Counter 4	Yes	1	EMIF1_SYS	EMIF2_SYS	MA_MPU_P1	MA_MPU_P2	EMIF1_LL
Counter 5	Yes	1	EMIF1_SYS	EMIF2_SYS	MA_MPU_P1	MA_MPU_P2	EMIF1_LL
Counter 6	Yes	No	No	No	MA_MPU_P1	MA_MPU_P2	EMIF1_LL
Counter 7	Yes	No	No	No	MA_MPU_P1	MA_MPU_P2	EMIF1_LL

29.9.6.2 Master Latency Monitoring

The device L3_MAIN interconnect implements twelve performance monitoring probes on the main L3 initiators:

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- MPU
- DSP
- DMA_SYSTEM_RD
- DMA_SYSTEM_WR
- IVA
- IPU
- DSS
- ISS
- GPU_P1
- GPU_P2
- BB2D_P1
- BB2D_P2

The master latency statistics are computed within a user-defined window and periodically reported to the user through the CT_STM interface.

The probes can be configured to filter latencies in four classes and report to the user a latency distribution along execution.

Because the performance metrics and the software events are exported through a unified export channel, it is possible to correlate latency trends with ongoing execution and system context.

Because computing latency requires maintaining the state between request and response ports, the probe cannot compute latency statistics on 100 percent of the initiator traffic. Hence, latency histograms must be extracted on large execution windows to be accurate.

29.9.6.2.1 SC_LAT0 Configuration

SC_LAT0 supports the following main features:

- Eight probe inputs:
  - Probe 0: MPU
  - Probe 1: DSP
  - Probe 2: DMA_SYSTEM_RD
  - Probe 3: DMA_SYSTEM_WR
  - Probe 4: DSS
  - Probe 5: ISS
  - Probe 6: GPU_P1
  - Probe 7: BB2D_P1
- Four 32-bit counters shared concurrently:
  - Counter 0 with one filter
  - Counter 1 with one filter
  - Counter 2 with one filter
  - Counter 3 with one filter
- Filtering according to:
  - L3 target
  - Access priorities
- 10-bit counter for latency measurement
- 32-bit collecting window counter
- Identifier is 0x1 (tie-off value)
- Dumps frames at slave address 0x19 (L3_INSTR)

Table 29-35 summarizes the SC_LAT0 configuration.

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Table 29-35. SC_LAT0 Configuration

Counters	Min Max	Filter Elements	L3 Master							
Counter 0	Yes	1	MPU	DSP	DMA_SYSTEM_RD	DMA_SYSTEM_WR	DSS	ISS	GPU_P1	BB2D_P1
Counter 1	Yes	1	MPU	DSP	DMA_SYSTEM_RD	DMA_SYSTEM_WR	DSS	ISS	GPU_P1	BB2D_P1
Counter 2	Yes	1	MPU	DSP	DMA_SYSTEM_RD	DMA_SYSTEM_WR	DSS	ISS	GPU_P1	BB2D_P1
Counter 3	Yes	1	MPU	DSP	DMA_SYSTEM_RD	DMA_SYSTEM_WR	DSS	ISS	GPU_P1	BB2D_P1

29.9.6.2.2 SC_LAT1 Configuration

SC_LAT1 supports the following main features:

- Six probe inputs:
  - Probe 0: IVA
  - Probe 1: MPU
  - Probe 2: DMA_SYSTEM_WR
  - Probe 3: GPU_P2
  - Probe 4: IPU
  - Probe 5: BB2D_P2
- Four 32-bit counters shared concurrently:
  - Counter 0 with one filter
  - Counter 1 with one filter
  - Counter 2 with one filter
  - Counter 3 with one filter
- Filtering according to:
  - L3 target
  - Access priorities
- 10-bit counter for latency measurement
- 32-bit collecting window counter
- Identifier is 0x2 (tie-off value)
- Dumps frames at slave address 0x19 (L3_INSTR)

Table 29-36 summarizes the SC_LAT1 configuration.

Table 29-36. SC_LAT1 Configuration

Counters	Min Max	Filter Elements	L3 Master					
Counter 0	Yes	1	IVA	MPU	DMA_SYSTEM_WR	GPU_P2	IPU	BB2D_P2
Counter 1	Yes	1	IVA	MPU	DMA_SYSTEM_WR	GPU_P2	IPU	BB2D_P2
Counter 2	Yes	1	IVA	MPU	DMA_SYSTEM_WR	GPU_P2	IPU	BB2D_P2
Counter 3	Yes	1	IVA	MPU	DMA_SYSTEM_WR	GPU_P2	IPU	BB2D_P2

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29.9.6.2.3 Statistics Collector Alarm Mode

Statistic collectors can be used to provide the application software with information about the NoC or SDRAM reaching corner cases (for example, too much traffic for a given OPP) while in application mode where for an end product use case the debug subsystem (which is normally exporting the statistic frames) is off. An interrupt-based scheme using a dedicated signal (L3_MAIN_IRQ_STAT_ALARM) is implemented to avoid CPU polling periodically statistic registers. This interrupt alert is mapped to the MPU_IRQ_16 interrupt line and is fired when a given metric is out of specified range (below the programmed MIN threshold or above the programmed MAX threshold).

NOTE: NTTP statistic collectors (SC_LAT0/1) support latency measurement. However, comparison cannot be done on the latency counter. In case of latency measurement the comparison has to be done on number of latencies in user defined range, not on the latency value itself.

29.9.6.2.4 Statistics Collector Suspend Mode

The statistics collector module implements a suspend input that is used to avoid statistics collector counters to be updated while the processor has entered the debug state. This avoids triggering false alerts upon execution resume. When the statistics collector is asserted to 1, it freezes the monitoring process. When it goes back to 0, the monitoring resumes.

NOTE: If a frame is being dumped, it will not be stopped by suspend.

Each statistic collector has an ignore suspend register, which can be used to disable the suspend feature.

29.9.7 PM Instrumentation

The device takes advantage of the system trace infrastructure to provide visibility to the user about the major power-management events. This is supported through a PMI module (PM profiler) instantiated in the PRM module. The PRM state changes are handled as generic events and encapsulated in STP hardware messages and exported through the CT_STM module. The nature of the PM events does not require accurate timestamping and thus, timestamping is handled at CT_STM or trace receiver level.

The PM events are organized by class. Any PM state change from a specific class refreshes the entire instrumentation frame associated with that class. The STP message structure includes a PM event-ID indicating the class of the PM events.

The PM event classes supported are:

- Logic voltage domain OPP change
- Memory voltage domain OPP change
- Logic power domain state change
- Memory power domain state change

The PMI has a unique hardware master ID assigned to it.

The PMI supports the possibility to report on activity in different event classes in the same sampling window. The user can size the capture sampling window.

Software events from the PM routines instrumentation can be interleaved with the PM hardware events. The user can take advantage of that feature to understand latencies for a specific power-management scenario or strategy.

29.9.8 CM Instrumentation

The device instantiates two CMI modules (CM profilers), one in CM1 (CMI1), and one in CM2 (CMI2). CMI1 and CMI2 are instantiations of the same debug-IP and can operate concurrently. Each of them has a separate unique hardware master ID assigned to it.

The CM events profiling is similar to the PMI. Two exclusive instrumentation modes are supported:

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- Clock activity:
  - Exposes to the user a snapshot of the state of all the clock domains derived from the same DPLL when CM detects a state change in the clock domain
  - Exposes to the user a snapshot of the DPLL settings when the CM signals a DPLL programming
- Module activity:
  - Exposes to the user periodically the active cycles count of the target modules
  - Exposes to the user periodically the active cycles count of the initiator modules

It provides visibility to the user about the state of the major clock domains along the application code execution. The STP message reports the effective state of the clock domain and therefore can highlight scenarios where a particular dependency is preventing the clock domain from being switched off.

The CM event classes supported are:

- Events capture mode – four classes:
  - Clock domain state
  - DPLL settings update
  - Clock frequency divider ratio
  - Clock source selection update
- Module activity collection mode – two classes:
  - Target module activity
  - Initiator module activity

When in events capture mode, the CMI supports the possibility of reporting on activity in different event classes in the same sampling window. The user can size the capture sampling window.

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29.10 Concurrent Debug Modes

The debugger or application software can program the DRM to route a specific debug function to each device debug port pin.

Because of the limited number of pins allocated to debug, debug and trace source signals are multiplexed.

Table 29-37 summarizes the trace port configuration.

Table 29-37. Trace Port Configuration

Pin Name	Internal Signal Name	I/O	Trigger	JTAG 20-Pin Header	CS_TPIU (MPU Trace [CS_PTM] interleaved with software instrumentation [CS_STM])	CT_STM (System Trace)
					16-Bit Mode (up to 16 data pins)	
drm_emu19	EMU19	O		EMU4	TRACEDATA[15]	STM_DATA[x] / STM_CLK
drm_emu18	EMU18	O		EMU3	TRACEDATA[14]	STM_DATA[x] / STM_CLK
drm_emu17	EMU17	O		EMU2	TRACEDATA[13]	STM_DATA[x] / STM_CLK
drm_emu16	EMU16	O			TRACEDATA[12]	STM_DATA[x] / STM_CLK
drm_emu15	EMU15	O			TRACEDATA[11]	STM_DATA[x] / STM_CLK
drm_emu14	EMU14	O			TRACEDATA[10]	STM_DATA[x] / STM_CLK
drm_emu13	EMU13	O			TRACEDATA[9]	STM_DATA[x] / STM_CLK
drm_emu12	EMU12	O			TRACEDATA[8]	STM_DATA[x] / STM_CLK
drm_emu11	EMU11	O			TRACEDATA[7]	STM_DATA[x] / STM_CLK
drm_emu10	EMU10	O			TRACEDATA[6]	STM_DATA[x] / STM_CLK
drm_emu9	EMU9	O			TRACEDATA[5]	STM_DATA[x] / STM_CLK
drm_emu8	EMU8	O			TRACEDATA[4]	STM_DATA[x] / STM_CLK
drm_emu7	EMU7	O			TRACEDATA[3]	STM_DATA[x] / STM_CLK
drm_emu6	EMU6	O			TRACEDATA[2]	STM_DATA[x] / STM_CLK
drm_emu5	EMU5	O			TRACEDATA[1]	STM_DATA[x] / STM_CLK
drm_emu4	EMU4	O			TRACEDATA[0]	STM_DATA[x] / STM_CLK
drm_emu3	EMU3	O			TRACECTL	STM_DATA[x] / STM_CLK
drm_emu2	EMU2	O			TRACECLK	STM_DATA[x] / STM_CLK
drm_emu1	EMU1	I/O	Trigger1	EMU1		STM_DATA[x] / STM_CLK
drm_emu0	EMU0	I/O	Trigger0	EMU0		STM_DATA[x] / STM_CLK

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NOTE: The configuration of the trace port must comply with Table 29-37; otherwise, it will be ignored by DRM hardware. For example, if Trigger0 is programmed on EMU10 and Trigger1 is programmed on EMU11, this configuration is ignored.

CT_STM (STMv1) port configuration provides full flexibility to map either STM_CLK or any STM_DATA line to any device debug port pin. Examples (recommended mapping) with no concurrent CS_TPIU trace:

- In 1-pin mode:
  - STM_CLK mapped to drm_emu0
  - STM_DATA[0] mapped to drm_emu1
- In 2-pin mode:
  - STM_CLK mapped to drm_emu2
  - STM_DATA[0] mapped to drm_emu0
  - STM_DATA[1] mapped to drm_emu1
- In 4-pin mode:
  - STM_CLK mapped to drm_emu2
  - STM_DATA[0] mapped to drm_emu0
  - STM_DATA[1] mapped to drm_emu1
  - STM_DATA[2] mapped to drm_emu4
  - STM_DATA[3] mapped to drm_emu5

The CS_STM (STMv2) trace clock is always mapped to drm_emu2 (as shown in Table 29-37).

Table 29-38 summarizes the concurrent debug and trace in the device.

Table 29-38. Concurrent Debug and Trace

Debug Use Case	Concurrent Debug Flows	Debug Pins	Trace Pins		
		Triggers	Data	Control	Clock
0	CS_PTM		18	1	1
	CT_STM				
	Triggers				
1	CS_PTM		16	1	1
	CT_STM				
	Triggers	2			
2	CS_PTM		16	1	1
	CT_STM		1	–	1
	Triggers				
3	CS_PTM		8	1	1
	CT_STM		4	–	1
	Triggers	2			
4	CS_PTM		11	1	1
	CT_STM		4	–	1
	Triggers	2			

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29.11 Memory Mapping

Table 29-39 summarizes the memory mapping of the debug modules.

Table 29-39. Debug Modules Memory Mapping

Memory Space	Module Name	Start Address (hex)	End Address (hex)	Size
L3_EMU_SLX	CT_STM_ADD_SP_0(1)	0x5400 0000	0x540F FFFF	1 MiB
	CT_STM_ADD_SP_1(1)	0x5410 0000	0x5413 FFFF	256 KiB
	DBG_MPU_C0(2)	0x5414 0000	0x5414 0FFF	4 KiB
	PMU_MPU_C0(2)	0x5414 1000	0x5414 1FFF	4 KiB
	DBG_MPU_C1(2)	0x5414 2000	0x5414 2FFF	4 KiB
	PMU_MPU_C1(2)	0x5414 3000	0x5414 3FFF	4 KiB
	CS_CTI_MPU_C0(2)	0x5414 8000	0x5414 8FFF	4 KiB
	CS_CTI_MPU_C1(2)	0x5414 9000	0x5414 9FFF	4 KiB
	CS_PTM_MPU_C0(2)	0x5414 C000	0x5414 CFFF	4 KiB
	CS_PTM_MPU_C1(2)	0x5414 D000	0x5414 DFFF	4 KiB
	CS_TF_MPU(2)	0x5415 8000	0x5415 8FFF	4 KiB
	DAP_PC(2)	0x5415 9000	0x5415 9FFF	4 KiB
	CS_STM_MPU(2)	0x5415 A000	0x5415 AFFF	4 KiB
	ATB_FIFO_SGU(2)	0x5415 B000	0x5415 BFFF	4 KiB
	CS_STI_MPU(2)	0x5415 C000	0x5415 CFFF	4 KiB
	T2AYNC_APB_MPU_DEBUG_MPU_MPU(2)	0x5415 F000	0x5415 FFFF	4 KiB
	DRM(3)	0x5416 0000	0x5416 0FFF	4 KiB
	CT_STM_CONF_PORT(3)	0x5416 1000	0x5416 1FFF	4 KiB
	CS_TPIU(3)	0x5416 3000	0x5416 3FFF	4 KiB
	CS_TF_DEBUGSS_1(3)	0x5416 4000	0x5416 4FFF	4 KiB
	CT_TBR(3)	0x5416 7000	0x5416 7FFF	4 KiB
	CT_UART(3)	0x5416 8000	0x5416 8FFF	4 KiB
	CS_CTI_DEBUGSS(3)	0x5416 9000	0x5416 9FFF	4 KiB
	OCP2SCP_DEBUGSS(3)	0x5417 1000	0x5417 1FFF	4 KiB
	L4_CFG_EMU_CONF_REGS(3)	0x5417 2000	0x5417 2FFF	4 KiB
	L3_INSTR_EMU_CONF_REGS(1)	0X5418 0000	0X5418 0FFF	4 KiB
MPU config	MA_MPU watchpoint	0x482A F200	0x482A F2FF	256B
L4_CFG	CMI1	0x4A00 4F00	0x4A00 4FFF	256B
	CMI2	0x4A00 9F00	0x4A00 9FFF	256B
	OCP_WP_NOC	0x4A10 2000	0x4A10 2FFF	4 KiB
L4_WKUP	PMI	0x4A30 7F00	0x4A30 7FFF	256B
IVA configuration	ICECRUSHER_IVA (ICONT1)	0x5A04 0000	0x5A04 07FF	2 KiB
	ICECRUSHER_IVA (ICONT2)	0x5A04 0800	0x5A04 0FFF	2 KiB
	SMSET	0x5A04 1000	0x5A04 1FFF	4 KiB
L3 configuration	SC_SDRAM	0x4500 0400	0x4500 05FF	512B
	SC_LAT0	0x4500 0600	0x4500 07FF	512B
	SC_LAT1	0x4500 0800	0x4500 09FF	512B
DSP configuration	SCTM_DSP	0x01C3 0400	0x01C3 05FF	512B
IPU configuration	SCTM_IPU	0x5508 0400	0x5508 07FF	1 KiB

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Table 29-39. Debug Modules Memory Mapping (continued)

Memory Space	Module Name	Start Address (hex)	End Address (hex)	Size
	ICECRUSHER_IPU x 2[4]	0xE004 2000	0xE004 2FFF	4 KiB

(1) Debug IPs mapped on L3_INSTR_EMU (located inside DEBUGSS)
(2) Debug IPs mapped through L3_INSTR_EMU and then L4_CFG_EMU interconnects from L3_MAIN (located inside MPU)
(3) Debug IPs mapped on L4_CFG_EMU (located inside DEBUGSS)
(4) Private memory access per Cortex-M4 core

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OMAP5432 Multimedia Device

This appendix describes the functional differences between the OMAP5432 and OMAP5430 multimedia devices.

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A.3	**Power, Reset, and Clock Management**	**6041**
A.4	**Memory Subsystem**	**6042**
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A.6	**Interrupt Controllers**	**6048**
A.7	**System Control Module**	**6055**
A.8	**Serial Communication Intrefaces**	**6075**
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A.1 Introduction

A.1.1 Overview

OMAP5432 multimedia device is based on enhanced OMAP™ architecture and uses 28-nm technology. It is offered in a non-POP, DDR3-enabled package and has a subset of the OMAP5430 communication interfaces and system balls.

For the terminal assignment and ball characteristics, see the *OMAP5432 Data Manual*.

A.1.2 Description

The OMAP5432 is offered in a 754-ball; 17 × 17 mm; 0.5-mm ball pitch s-PBGA package, which does not support the package-on-package (POP) concept. Also, some of the OMAP device pads are not available on the package balls. As a consequence:

- Stacked mode and LPDDR2 memories are not supported. The OMAP5432 supports DDR3/DDR3L memory interface through bottom ballout.
- Some of the interfaces offered in the die are not available.
- Some of the interfaces offered in the die are restricted.
- Some of the device system pins are not supported.

CAUTION

Because all subsystems and modules are still present on the die, the removed functionality must be carefully handled to maintain reliability.

A.1.2.1 Unsupported Interfaces

The following interfaces are not supported in the OMAP5432 device:

- LPDDR2 EMIF memory interface
- MIPI® HSI modem interface port 1
- Universal asynchronous receiver/transmitter 6 (UART6)
- HS USB host subsystem high-speed interchip 1 (HSIC1) interface
- HS USB host subsystem ULPI TLL interface
- SS USB DRD subsystem ULPI PHY interface
- MMC/SD/SDIO5

A.1.2.2 Interface Restrictions

The following restrictions apply to the OMAP5432 interfaces:

- General-purpose memory controller (GPMC)
  - Chip-select 7 signal (gpmc_ncs7) is not available at the device ballout.
- UART1
  - UART1 is available on different device balls, that is, on balls timer11_pwm_evt, timer5_pwm_evt, timer6_pwm_evt,and timer8_pwm_evt in mux mode 2.
- UART4
  - UART4 is a 2-wire (TX/RX) interface. UART4 flow-control (RTS/CTS) pins are not available.
- MCSPI1
  - Chip-selects 2 and 3 (CS2 and CS3) are not available.
- HS USB Host subsystem
  - USB host port 2 (USBB2) in FS serial mode is limited to 2-/3-wire serial mode.
- General-purpose input/output (GPIO)

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- The following GPIO channels are not available:
  - gpio1_wk8 to gpio1_wk10
  - gpio3_64 to gpio3_75
  - gpio3_92 and gpio3_93
  - gpio5_145 and gpio5_146
  - gpio5_149 to gpio5_151

A.1.2.3 Unsupported System Pins

The following restrictions apply to the OMAP5432 system interfaces:

- PRCM
  - On-chip slicer cell is not supported. That is, system clock source can be only the oscillator cell (crystal, or external square input).
  - Clock outputs fref_clk2_out and fref_clk3_out are not available.
  - Hardware clock requests fref_clk1_req and fref_clk2_req are not supported.
- System DMA (DMA_SYSTEM) controller
  - External DMA request 1 (sys_ndmareq1) is not supported. sys_ndmareq0 is available on different device ball (on uart6_rts in mux mode 1)
- Debug subsystem
  - Hardware observability signals hw_wkdbg10, hw_wkdbg11, and hw_wkdbg12 are not available.

A.1.2.4 Block Diagram

Figure A-1 describes the supported subsystems in OMAP5432 devices.

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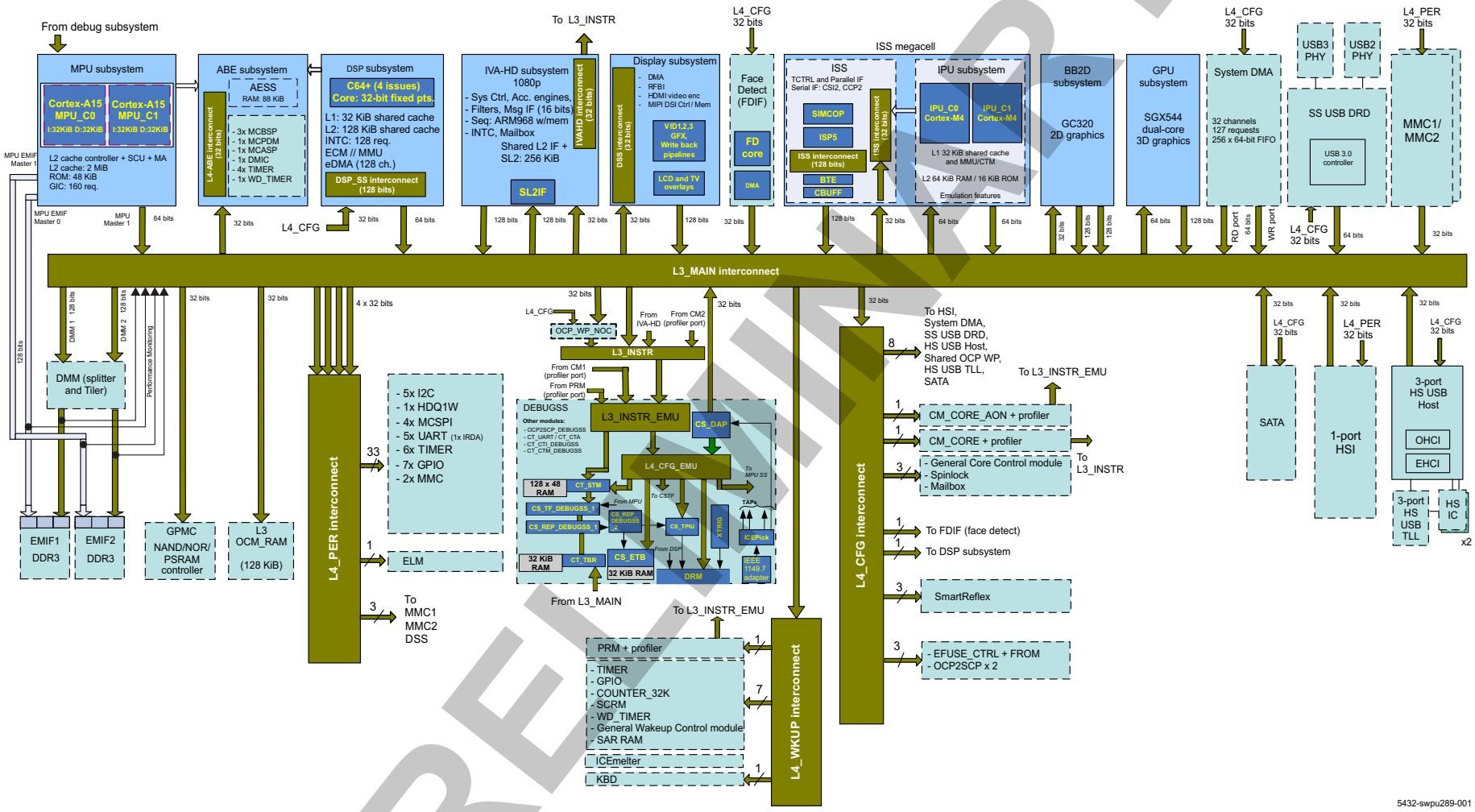
Figure A-1. OMAP5432 Block Diagram



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A.2 Memory Mapping

NOTE: This subsection provides a quick reference about the unavailable modules and their memory mapping. Table rows highlighted in orange indicate modules that are not functional in OMAP5432. These modules are still present on the die; therefore, their mappings are provided to control their activity and for debug purposes.

A.2.1 L4_CFG Memory Space Mapping

The L4_CFG interconnect is a 16-MB space composed of the L4_CFG interconnect configuration registers and the module registers.

Table A-1 describes the mapping of the registers for the L4_CFG interconnect.

Table A-1. L4_CFG Memory Space Mapping

Region Name	Related IP Name	Start Address (hex)	End Address (hex)	Size	Description
L4_CFG_AP	L4_CFG	0x4A00 0000	0x4A00 07FF	2 KiB	Address protection
L4_CFG_AL	L4_CFG	0x4A00 0800	0x4A00 0FFF	2 KiB	Link agent
IA_IP0	L4_CFG	0x4A00 1000	0x4A00 1FFF	4 KiB	Initiator port
TP_CTRL_MODULE_CORE_TARG	CTRL_MODULE_CORE	0x4A00 2000	0x4A00 2FFF	4 KiB	Module target port
TA_CTRL_MODULE_CORE_TARG	L4_CFG	0x4A00 3000	0x4A00 3FFF	4 KiB	L4 target agent
TP_CM_CORE_AON_TARG	CM_CORE_AON	0x4A00 4000	0x4A00 4FFF	4 KiB	Module target port
TA_CM_CORE_TARG	L4_CFG	0x4A00 5000	0x4A00 5FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A00 6000	0x4A06 7FFF	Reserved	Reserved
TP_CM_CORE_TARG	CM_CORE	0x4A00 8000	0x4A08 9FFF	8 KiB	Target port
TA_CM_CORE_TARG	L4_CFG	0x4A00 A000	0x4A00 AFFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A00 B000	0x4A01 FFFF	Reserved	Reserved
TP_USB_OTG_SS_TARG	USB_OTG_SS	0x4A02 0000	0x4A03 FFFF	128 KiB	Module target port
TA_USB_OTG_SS_TARG	L4_CFG	0x4A04 0000	0x4A04 0FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A04 1000	0x4A05 5FFF	84 KiB	Reserved
TP_DMA_SYSTEM_TARG	DMA_SYSTEM	0x4A05 6000	0x4A05 6FFF	4 KiB	Module target port
TA_DMA_SYSTEM_TARG	L4_CFG	0x4A05 7000	0x4A05 7FFF	4 KiB	L4 target agent
TP_HSI_TOP_ADDRSP0_TARG	HSI address space 0	0x4A05 8000	0x4A05 8FFF	4 KiB	Module target port - HSI top (Maddrspace 0)
TP_HSI_DMA_ADDRSP1_TARG	HSI address space 1	0x4A05 9000	0x4A05 9FFF	4 KiB	Module target port - HSI DMA (Maddrspace 1)
TP_HSI_PORT1_ADDRSP2_TARG	HSI address space 2	0x4A05 A000	0x4A05 AFFF	4 KiB	Module target port - HSI port 1 (Maddrspace 2)
TP_HSI_PORT2_ADDRSP3_TARG	HSI addres space 3	0x4A05 B000	0x4A05 BFFF	4 KiB	Module target port - HSI port 2 (Maddrspace 3)
TA_HSI_TARG	L4_CFG	0x4A05 C000	0x4A05 CFFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A05 D000	0x4A05 DFFF	4 KiB	Reserved
Reserved	Reserved	0x4A05 E000	0x4A05 FFFF	8 KiB	Reserved
Reserved	Reserved	0x4A06 0000	0x4A06 0FFF	4 KiB	Reserved
Reserved	Reserved	0x4A06 1000	0x4A06 1FFF	4 KiB	Reserved
TP_USB_TLL_HS_TARG	USB_TLL_HS	0x4A06 2000	0x4A06 2FFF	4 KiB	Module target port
TA_USB_TLL_HS_TARG	L4_CFG	0x4A06 3000	0x4A06 3FFF	4 KiB	L4 target agent
TP_USB_HOST_HS_TARG	USB_HOST_HS	0x4A06 4000	0x4A06 4FFF	4 KiB	Module target port
TA_USB_HOST_HS_TARG	L4_CFG	0x4A06 5000	0x4A06 5FFF	4 KiB	L4 target agent

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Table A-1. L4_CFG Memory Space Mapping (continued)

Region Name	Related IP Name	Start Address (hex)	End Address (hex)	Size	Description
TP_DSP_TARG	DSP	0x4A06 6000	0x4A06 6FFF	4 KiB	Target port
TA_DSP_TARG	L4_CFG	0x4A06 7000	0x4A06 7FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A06 8000	0x4A06 BFFF	16 KiB	Reserved
Reserved	Reserved	0x4A06 C000	0x4A06 CFFF	4 KiB	Reserved
Reserved	Reserved	0x4A06 D000	0x4A06 DFFF	4 KiB	Reserved
Reserved	Reserved	0x4A06 E000	0x4A06 EFFF	4 KiB	Reserved
Reserved	Reserved	0x4A06 F000	0x4A06 FFFF	4 KiB	Reserved
Reserved	Reserved	0x4A07 0000	0x4A07 3FFF	16 KiB	Reserved
Reserved	Reserved	0x4A07 4000	0x4A07 4FFF	4 KiB	Reserved
Reserved	Reserved	0x4A07 5000	0x4A07 5FFF	4 KiB	Reserved
Reserved	Reserved	0x4A076000	0x4A07 6FFF	4 KiB	Reserved
Reserved	Reserved	0x4A07 7000	0x4A07 FFFF	36 KiB	Reserved
TP_OCP2SCP1_TARG	OCP2SCP1	0x4A08 0000	0x4A08 3FFF	16 KiB	Module target port
TP_OCP2SCP1_USB_PHY_CORE_TARG	OCP2SCP1 (USB_PHY)	0x4A08 4000	0x4A08 43FF	1 KiB	Module target port
TP_OCP2SCP1_USB3_PHY_RX_TARG	OCP2SCP1 (USB3_PHY_RX)	0x4A08 4400	0x4A08 47FF	1 KiB	Target port
TP_OCP2SCP1_USB3_PHY_TX_TARG	OCP2SCP1 (USB3_PHY_TX)	0x4A08 4800	0x4A08 4BFF	1 KiB	Target port
TP_OCP2SCP1_DPLLCTRL_USB_OTG_SS_TARG	OCP2SCP1 (USB_OTG_SS)	0x4A08 4C00	0x4A0D CFFF	1 KiB	Tarteg port
Reserved	Reserved	0x4A08 5000	0x4A08 7FFF	12 KiB	Reserved
TA_OCP2SCP1_TARG	L4_CFG	0x4A08 8000	0x4A08 8FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A08 9000	0x4A08 FFFF	28 KiB	Reserved
TP_OCP2SCP3_TARG	OCP2SCP3	0x4A09 0000	0x4A09 3FFF	16 KiB	Target port
Reserved	Reserved	0x4A09 4000	0x4A09 43FF	1 KiB	Reserved
Reserved	Reserved	0x4A09 4400	0x4A09 47FF	1 KiB	Reserved
Reserved	Reserved	0x4A09 4800	0x4A09 4BFF	1 KiB	Reserved
Reserved	Reserved	0x4A09 4C00	0x4A09 4FFF	1 KiB	Reserved
Reserved	Reserved	0x4A09 5000	0x4A09 53FF	1 KiB	Reserved
Reserved	Reserved	0x4A09 5400	0x4A09 5FFF	3 KiB	Reserved
TP_OCP2SCP3_SATA_PHY_RX_TARG	OCP2SCP3 (SATA_PHY_RX)	0x4A09 6000	0x4A09 63FF	1 KiB	Target port
TP_OCP2SCP3_SATA_PHY_TX_TARG	OCP2SCP3 (SATA_PHY_TX)	0x4A09 6400	0x4A09 67FF	1 KiB	Target port
TP_OCP2SCP3_DPLLCTRL_SATA_TARG	OCP2SCP3 (DPLLCTRL_SATA)	0x4A09 6800	0x4A09 6BFF	1 KiB	Target port
Reserved	Reserved	0x4A09 6C00	0x4A09 7FFF	5 KiB	Reserved
TA_OCP2SCP3_TARG	L4_CFG	0x4A09 8000	0x4A09 8FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A09 9000	0x4A09 FFFF	28 KiB	Reserved
Reserved	Reserved	0x4A0A 0000	0x4A0A 3FFF	1 KiB	Reserved
Reserved	Reserved	0x4A0A 4000	0x4A0A 43FF	1 KiB	Reserved
Reserved	Reserved	0x4A0A 4400	0x4A0A 47FF	1 KiB	Reserved
Reserved	Reserved	0x4A0A 4800	0x4A0A 4FFF	2 KiB	Reserved
Reserved	Reserved	0x4A0A 5000	0x4A0A 53FF	1 KiB	Reserved
Reserved	Reserved	0x4A0A 5400	0x4A0A 57FF	1 KiB	Reserved
Reserved		0x4A0A 5800	0x4A0A 5FFF	2 KiB	Reserved
Reserved	Reserved	0x4A0A 6000	0x4A0A 63FF	1 KiB	Reserved
Reserved	Reserved	0x4A0A 6400	0x4A0A 67FF	1 KiB	Reserved

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Table A-1. L4_CFG Memory Space Mapping (continued)

Region Name	Related IP Name	Start Address (hex)	End Address (hex)	Size	Description
Reserved	Reserved	0x4A0A 6800	0x4A0A 7FFF	6 KiB	Reserved
Reserved	Reserved	0x4A0A 8000	0x4A0A 8FFF	4 KiB	Reserved
Reserved	Reserved	0x4A0A 9000	0x4A0B 5FFF	56 KiB	Reserved
Reserved	Reserved	0x4A0B 6000	0x4A0B 6FFF	4 KiB	Reserved
Reserved	Reserved	0x4A0B 7000	0x4A0B 7FFF	4 KiB	Reserved
Reserved	Reserved	0x4A0B 8000	0x4A0C CFFF	84 KiB	Reserved
Reserved	Reserved	0x4A0C D000	0x4A0C DFFF	4 KiB	Reserved
Reserved	Reserved	0x4A0C E000	0x4A0C EFFF	4 KiB	Reserved
Reserved	Reserved	0x4A0C F000	0x4A0D 8FFF	40 KiB	Reserved
TP_SMARTREFLEX_MPU_TARG	SMARTREFLEX_MPU	0x4A0D 9000	0x4A0D 9FFF	4 KiB	Module target port
TA_SMARTREFLEX_MPU_TARG	L4_CFG	0x4A0D A000	0x4A0D AFFF	4 KiB	L4 target agent
TP_SMARTREFLEX_MM_TARG	SMARTREFLEX_MM	0x4A0D B000	0x4A0D BFFF	4 KiB	Module target port
TA_SMARTREFLEX_MM_TARG	L4_CFG	0x4A0D C000	0x4A0D CFFF	4 KiB	L4 target agent
TP_SMARTREFLEX_CORE_TARG	SMARTREFLEX_CORE	0x4A0D 0000	0x4A0D DFFF	4 KiB	Module targe port
TA_SMARTREFLEX_CORE_TARG	L4_CFG	0x4A0D E000	0x4A0D EFFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A0D F000	0x4A0D FFFF	16 KiB	Reserved
TP_EFUSE_CTRL_CUST_TARG	EFUSE_CTRL_CUST	0x4A0E 0000	0x4A0E 0FFF	4 KiB	Module target port
TA_EFUSE_CTRL_CUST_TARG	L4_CFG	0x4A0E 1000	0x4A0E 1FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A0E 2000	0x4A0F 3FFF	72 KiB	Reserved
TP_MAILBOX_TARG	MAILBOX	0x4A0F 4000	0x4A0F 4FFF	4 KiB	Target port
TA_MAILBOX_TARG	L4_CFG	0x4A0F 5000	0x4A0F 5FFF	4 KiB	L4 target agent
TP_SPINLOCK_TARG	SPINLOCK	0x4A0F 6000	0x4A0F 6FFF	4 KiB	Module target port
TA_SPINLOCK_TARG	L4_CFG	0x4A0F 7000	0x4A0F 7FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A0F 8000	0x4A10 1FFF	40 KiB	Reserved
TP_OCP_WP_NOC_TARG	OCP_WP_NOC	0x4A10 2000	0x4A10 2FFF	4 KiB	Module target port
TA_OCP_WP_NOC_TARG	L4_CFG	0x4A10 3000	0x4A10 3FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A10 4000	0x4A10 9FFF	24 KiB	Reserved
TP_FDIF_TARG	EDIF	0x4A10 A000	0x4A10 AFFF	4 KiB	Module target port
TA_FDIF_TARG	L4_CFG	0x4A10 B000	0x4A10 BFFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A10 C000	0x4A13 FFFF	208 KiB	Reserved
TP_SATA_TARG	SATA	0x4A14 0000	0x4A14 FFFF	64 KiB	Module target port
TA_SATA_TARG	L4_CFG	0x4A15 0000	0x4A15 0FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A15 1000	0x4A20 1FFF	716 KiB	Reserved
Reserved	Reserved	0x4A21 2000	0x4A20 2FFF	4 KiB	Reserved
Reserved	Reserved	0x4A20 3000	0x4A20 3FFF	4 KiB	Reserved
Reserved	Reserved	0x4A20 4000	0x4A20 4FFF	4 KiB	Reserved
Reserved	Reserved	0x4A20 5000	0x4A20 5FFF	4 KiB	Reserved
Reserved	Reserved	0x4A20 6000	0x4A20 6FFF	4 KiB	Reserved
Reserved	Reserved	0x4A20 7000	0x4A20 7FFF	4 KiB	Reserved
Reserved	Reserved	0x4A20 8000	0x4A20 8FFF	4 KiB	Reserved
Reserved	Reserved	0x4A20 9000	0x4A20 9FFF	4 KiB	Reserved
TP_MA_MPU_NTTP_FW_CFG_TARG	GPMC	0x4A20 A000	0x4A20 AFFF	4 KiB	Module target port
TA_MA_MPU_NTTP_FW_CFG_TARG	L4_CFG	0x4A20 B000	0x4A20 BFFF	4 KiB	L4 target agent
TP_EMIF_OCP_FW_CFG_TARG	EMIF_OCP_FW	0x4A20 C000	0x4A20 CFFF	4 KiB	Module target port
TA_EMIF_OCP_FW_CFG_TARG	L4_CFG	0x4A20 D000	0x4A20 DFFF	4 KiB	L4 target agent

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Table A-1. L4_CFG Memory Space Mapping (continued)

Region Name	Related IP Name	Start Address (hex)	End Address (hex)	Size	Description
Reserved	Reserved	0x4A20 E000	0x4A20 FFFF	8 KiB	Reserved
TP_GPMC_FW_CFG_TARG	GPMC	0x4A21 0000	0x4A21 0FFF	4 KiB	Module target port
TA_GPMC_FW_CFG_TARG	L4_CFG	0x4A21 1000	0x4A21 1FFF	4 KiB	L4 target agent
TP_OCMC_RAM_FW_CFG_TARG	OCMC_RAM	0x4A21 2000	0x4A21 2FFF	4 KiB	Module target port
TA_OCMC_RAM_FW_CFG_TARG	L4_CFG	0x4A21 3000	0x4A21 3FFF	4 KiB	L4 target agent
TP_GPU_FW_CFG_TARG	GPU	0x4A21 4000	0x4A21 4FFF	4 KiB	Module target port
TA_GPU_FW_CFG_TARG	L4_CFG	0x4A21 5000	0x4A21 5FFF	4 KiB	L4 target agent
TP_ISS_FW_CFG_TARG	ISS	0x4A21 6000	0x4A21 6FFF	4 KiB	Module target port
TA_ISS_FW_CFG_TARG	L4_CFG	0x4A21 7000	0x4A21 7FFF	4 KiB	L4 target agent
TP_IPU_FW_CFG_TARG	IPU	0x4A21 8000	0x4A21 8FFF	4 KiB	Module target port
TA_IPU_FW_CFG_TARG	L4_CFG	0x4A21 9000	0x4A21 9FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A21 A000	0x4A21 BFFF	8 KiB	Reserved
TP_DSS_FW_CFG_TARG	DSS	0x4A21 C000	0x4A21 CFFF	4 KiB	Module target port
TP_DSS_FW_CFG_TARG	L4_CFG	0x4A21 D000	0x4A21 DFFF	4 KiB	L4 target agent
TP_IVA_SL2IF_FW_CFG_TARG	IVA_SL2IF	0x4A21 E000	0x4A21 EFFF	4 KiB	Module target port
TA_IVA_SL2IF_FW_CFG_TARG	L4_CFG	0x4A21 F000	0x4A21 FFFF	4 KiB	L4 target agent
TP_IVA_CONFIG_FW_CFG_TARG	IVA	0x4A22 0000	0x4A22 0FFF	4 KiB	Module target port
TA_IVA_CONFIG_FW_CFG_TARG	L4_CFG	0x4A22 1000	0x4A22 1FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A22 2000	0x4A22 2FFF	4 KiB	Reserved
Reserved	Reserved	0x4A22 3000	0x4A22 3FFF	4 KiB	Reserved
TP_DEBUGSS_CT_TBR_FW_CFG_TARG	DEBUGSS	0x4A22 4000	0x4A22 4FFF	4 KiB	Module targe prot
TA_DEBUGSS_CT_TBR_FW_CFG_TARG	L4_CFG	0x4A22 5000	0x4A22 5FFF	4 KiB	L4 target agent
TP_L3_INSTR_FW_CFG_TARG	L3_INSTR	0x4A22 6000	0x4A22 6FFF	4 KiB	Module target port
TA_L3_INSTR_FW_CFG_TARG	L4_CFG	0x4A22 7000	0x4A22 7FFF	4 KiB	L4 target agent
TP_ABE_FW_CFG_TARG	ABE	0x4A22 8000	0x4A22 8FFF	4 KiB	Module target port
TA_ABE_FW_CFG_TARG	L4_CFG	0x4A22 9000	0x4A22 9FFF	4 KiB	L4 target agent
Reserved	Reserved	0x4A22 A000	0x4ADF FFFF	12MB	Reserved

A.2.2 L4_PER Memory Space Mapping

The L4_PER interconnect is a 16-MB memory space composed of the L4_PER interconnect configuration registers and the module registers.

Table A-2 describes the mapping of the registers for the L4_PER interconnect.

NOTE: All memory spaces described as modules provide direct access to the module registers outside the L4_PER interconnect. All other accesses are internal to the L4_PER interconnect.

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Table A-2. L4_PER Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4_PER	0x4800 0000	0x4800 07FF	2 KiB	Address protection (AP)
	0x4800 0800	0x4800 0FFF	2 KiB	Link agent (LA)
	0x4800 1000	0x4800 13FF	1 KiB	Initiator port 0 (IP0)
	0x4800 1400	0x4800 17FF	1 KiB	Initiator port 1 (IP1)
	0x4800 1800	0x4800 1BFF	1 KiB	Initiator port 2 (IP2)
	0x4800 1C00	0x4800 1FFF	1 KiB	Initiator port 3 (IP3)
Reserved	0x4800 2000	0x4801 FFFF	120 KiB	Reserved
UART3	0x4802 0000	0x4802 0FFF	4 KiB	Module
	0x4802 1000	0x4802 1FFF	4 KiB	L4 interconnect
Reserved	0x4802 2000	0x4803 1FFF	64 KiB	Reserved
TIMER2	0x4803 2000	0x4803 2FFF	4 KiB	Module
	0x4803 3000	0x4803 3FFF	4 KiB	L4 interconnect
TIMER3	0x4803 4000	0x4803 4FFF	4 KiB	Module
	0x4803 5000	0x4803 5FFF	4 KiB	L4 interconnect
TIMER4	0x4803 6000	0x4803 6FFF	4 KiB	Module
	0x4803 7000	0x4803 7FFF	4 KiB	L4 interconnect
Reserved	0x4803 8000	0x4803 DFFF	24 KiB	Reserved
TIMER9	0x4803 E000	0x4803 EFFF	4 KiB	Module
	0x4803 F000	0x4803 FFFF	4 KiB	L4 interconnect
Reserved	0x4804 0000	0x4805 0FFF	68 KiB	Reserved
GPIO7	0x4805 1000	0x4805 1FFF	4 KiB	Module
	0x4805 2000	0x4805 2FFF	4 KiB	L4 interconnect
GPIO8	0x4805 3000	0x4805 3FFF	4 KiB	Module
	0x4805 4000	0x4805 4FFF	4 KiB	L4 interconnect
GPIO2	0x4805 5000	0x4805 5FFF	4 KiB	Module
	0x4805 6000	0x4805 6FFF	4 KiB	L4 interconnect
GPIO3	0x4805 7000	0x4805 7FFF	4 KiB	Module
	0x4805 8000	0x4805 8FFF	4 KiB	L4 interconnect
GPIO4	0x4805 9000	0x4805 9FFF	4 KiB	Module
	0x4805 A000	0x4805 AFFF	4 KiB	L4 interconnect
GPIO5	0x4805 B000	0x4805 BFFF	4 KiB	Module
	0x4805 C000	0x4805 CFFF	4 KiB	L4 interconnect
GPIO6	0x4805 D000	0x4805 DFFF	4 KiB	Module
	0x4805 E000	0x4805 EFFF	4 KiB	L4 interconnect
Reserved	0x4805 F000	0x4805 FFFF	4 KiB	Reserved
I2C3	0x4806 0000	0x4806 0FFF	4 KiB	Module
	0x4806 1000	0x4806 1FFF	4 KiB	L4 interconnect
Reserved	0x4806 2000	0x4806 5FFF	16 KiB	Reserved
UART5	0x4806 6000	0x4805 6FFF	4 KiB	Module
	0x4806 7000	0x4806 7FFFF	4 KiB	L4 interconnect
UART6	0x4806 8000	0x4806 8FFF	4 KiB	Module
	0x4806 9000	0x4806 9FFF	4 KiB	L4 interconnect
UART1	0x4806 A000	0x4806 AFFF	4 KiB	Module
	0x4806 B000	0x4806 BFFF	4 KiB	L4 interconnect
UART2	0x4806 C000	0x4806 CFFF	4 KiB	Module
	0x4806 D000	0x4806 DFFF	4 KiB	L4 interconnect
UART4	0x4806 E000	0x4806 EFFF	4 KiB	Module
	0x4806 F000	0x4806 FFFF	4 KiB	L4 interconnect

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Table A-2. L4_PER Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
I2C1	0x4807 0000	0x4807 0FFF	4 KiB	Module
	0x4807 1000	0x4807 1FFF	4 KiB	L4 interconnect
I2C2	0x4807 2000	0x4807 2FFF	4 KiB	Module
	0x4807 3000	0x4807 3FFF	4 KiB	L4 interconnect
Reserved	0x4807 4000	0x4807 5FFF	8 KiB	Reserved
Reserved	0x4807 6000	0x4807 6FFF	4 KiB	Reserved
	0x4807 7000	0x4807 7FFF	4 KiB	Reserved
ELM (error locator module)	0x4807 8000	0x4807 8FFF	4 KiB	Module
	0x4807 9000	0x4807 9FFF	4 KiB	L4 interconnect
I2C4	0x4807 A000	0x4807 AFFF	4 KiB	Module
	0x4807 B000	0x4807 BFFF	4 KiB	L4 interconnect
I2C5	0x4807 C000	0x4807 CFFF	4 KiB	Module
	0x4807 D000	0x4807 DFFF	4 KiB	L4 interconnect
Reserved	0x4807 E000	0x4808 5FFF	32 KiB	Reserved
TIMER10	0x4808 6000	0x4808 6FFF	4 KiB	Module
	0x4808 7000	0x4808 7FFF	4 KiB	L4 interconnect
TIMER11	0x4808 8000	0x4808 8FFF	4 KiB	Module
	0x4808 9000	0x4808 9FFF	4 KiB	L4 interconnect
Reserved	0x4808 A000	0x4809 7FFF	56 KiB	Reserved
McSPI1	0x4809 8000	0x4809 8FFF	4 KiB	Module
	0x4809 9000	0x4809 9FFF	4 KiB	L4 interconnect
McSPI2	0x4809 A000	0x4809 AFFF	4 KiB	Module
	0x4809 B000	0x4809 BFFF	4 KiB	L4 interconnect
MMC1	0x4809 C000	0x4809 CFFF	4 KiB	Module
	0x4809 D000	0x4809 DFFF	4 KiB	L4 interconnect
Reserved	0x4809 E000	0x480A CFFF	60 KiB	Reserved
MMC3	0x480A D000	0x480A DFFF	4 KiB	Module
	0x480A E000	0x480A EFFF	4 KiB	L4 interconnect
Reserved	0x480A F000	0x480B 1FFF	12 KiB	Reserved
HDQ1W	0x480B 2000	0x480B 2FFF	4 KiB	Module
	0x480B 3000	0x480B 3FFF	4 KiB	L4 interconnect
MMC2	0x480B 4000	0x480B 4FFF	4 KiB	Module
	0x480B 5000	0x480B 5FFF	4 KiB	L4 interconnect
Reserved	0x480B 6000	0x480B 7FFF	8 KiB	Reserved
MCSPI3	0x480B 8000	0x480B 8FFF	4 KiB	Module
	0x480B 9000	0x480B 9FFF	4 KiB	L4 interconnect
MCSPI4	0x480B A000	0x480B AFFF	4 KiB	Module
	0x480B B000	0x480B BFFF	4 KiB	L4 interconnect
Reserved	0x480B C000	0x480D 0FFF	84 KiB	Reserved
MMC4	0x480D 1000	0x480D 1FFF	4 KiB	Module
	0x480D 2000	0x480D 2FFF	4 KiB	L4 interconnect
Reserved	0x480D 3000	0x480D 4FFF	8 KiB	Reserved
MMC5	0x480D 5000	0x480D 5FFF	4 KiB	Module
	0x480D 6000	0x480D 6FFF	4 KiB	L4 interconnect
Reserved	0x480D 7000	0x480F EFFF	160 KiB	Reserved
DSS	0x480F F000	0x480F FFFF	4 KiB	L4 interconnect
	0x4810 0000	0x4810 0FFF	4 KiB	Module

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Table A-2. L4_PER Memory Space Mapping (continued)

Module Name	Start Address (hex)	End Address (hex)	Size	Description
DISPC	0x4810 1000	0x4810 1FFF	4 KiB	Display configuration plus data
RFBI	0x4810 2000	0x4810 2FFF	4 KiB	Display configuration plus data
Reserved	0x4810 3000	0x4810 3FFF	4 KiB	Reserved
DSI1_A	0x4810 4000	0x4810 4FFF	4 KiB	Display configuration plus data
Reserved	0x4810 5000	0x4810 7FFF	12 KiB	Reserved
L4_DSS	0x4810 8000	0x4810 8FFF	4 KiB	L4 interconnect
DSI1_C	0x4810 9000	0x4810 9FFF	4 KiB	Display configuration plus data
Reserved	0x4810 A000	0x4813_FFFF	216 KiB	Reserved
HDMI (WRP)	0x4814 0000	0x4815_FFFF	128 KiB	HDMI wrapper: Display configuration plus data
HDMI (NHDCP)	0x4816 0000	0x4816 FFFF	64 KiB	Display configuration plus data
HDMI (NHDCP)	0x4817 0000	0x4817 7FFF	32 KiB	Display configuration plus data
HDMI (HDCP)	0x4817 8000	0x4817 FFFF	32 KiB	Display configuration plus data
Reserved	0x4818 0000	0x48FF FFFF	14.5MB	Reserved

A.3 Power, Reset, and Clock Management

A.3.1 PRCM Environment

The following signals are supported by the PRCM module, but are not available at the OMAP5432 device boundary:

- On-chip slicer cell is not supported. That is, system clock source can be only the oscillator cell with crystal or external square input.
- Clock outputs fref_clk2_out and fref_clk3_out are not available.
- Hardware clock requests fref_clk1_req and fref_clk2_req are not supported.

Table A-3 lists the external clock signals, I/Os, and module reset values. Highlighted rows represent nonfunctional pins in OMAP5432 devices.

Table A-3. External Clock Signals

Pin	Signal	I/O[1]	PMFW Module	Description
sys_32k	SYS_32K	I	SCRM	32-kHz clock input (sleep clock)
fref_clk_ioreq	SYSCLK_REQ	I/O	SCRM	System clock request. Input when pins sysboot4 = 0 and sysboot5 = 0 (oscillator mode). Output when pins sysboot4 = 0 and sysboot5 = 1 (CLOCK_SLICER mode).
fref_slicer_in	SLICER_IN	I	SCRM	System clock input to the CLOCK_SLICER. It can be sinusoidal or square input signal.
fref_slicer_az	SLICER_AZ	I	SCRM	Connected to ground at package level
fref_xtal_in	XTAL_IN	I	SCRM	Oscillator drive input from crystal
fref_xtal_out	XTAL_OUT	O	SCRM	Oscillator drive output to crystal
fref_xtal_clk	XTAL_CLK	O	SCRM	Oscillator buffered output
fref_clk[1:2]_req	CLK[1:2]_REQ	I	SCRM	Auxiliary clocks request
fref_clk[0:1]_out	CLK[0:1]_OUT	O	SCRM	Auxiliary clocks outputs 0 to 1
fref_clk[2:3]_out	CLK[2:3]_OUT	O	SCRM	Auxiliary clocks outputs 2 to 3

(1) I = Input; O = Output; I/O = Input and output (bidirectional)

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A.3.2 PRCM Use Guidelines

- Use a crystal or a external clock oscillator IC for the system clock input. Sine clock input option is not supported.
- Functional and interface clocks for the unsupported modules must be gated (disabled) (see Section 3.6, *Clock Management Functional Description,* in Chapter 3, *Power, Reset, and Clock Management*). All unsupported modules and functionality are listed in Section A.1, *Introduction.*
- Because of DDR3 memories used in place of LPDDR2:
  - At boot time, software must set the EMIF clock domain into SW_WKUP mode (CM_EMIF_CLKSTCTRL[1:0] CLKTRCTRL=0x2).
  - The static dependency between MPU and EMIF, which is set by default at reset, must never be cleared by the software (CM_MPU_STATICDEP[4] EMIF_STATDEP = 1).
- All wake-up events from the unsupported modules must be disabled (see Section 3.6, *Clock Management Functional Description,* in Chapter 3, *Power, Reset, and Clock Management*).

A.4 Memory Subsystem

A.4.1 GPMC Controller

The following signals are supported by the GPMC but are not available outside OMAP5432 device:

- Chip-select signal 7 (gpmc_ncs7)

NOTE: Cells highlighted in orange in Table A-4, *GPMC I/O Description*, indicate signals with no dedicated balls in OMAP5432 device.

Table A-4 lists the GPMC subsystem I/O pins of the OMAP5432 device.

Table A-4. GPMC I/O Description

Pin Name	Device Signal	I/O[1]	Description
A[26:17]	gpmc_a[25:16]	O	Address
A[16:1]/D[15:0]	gpmc_ad[15:0]	I/O	Multiplexed address/data
nCS[6:0]	gpmc_ncs[6:0]	O	Chip-selects (active low)
nCS7	gpmc_ncs7	O	Chip-select (active low)
CLK	gpmc_clk	O[2]	Clock generated for the external memory or device
nADV/ALE	gpmc_nadv_ale	O	Address valid (active low). Also used as address latch enable (active high) for NAND protocol memories.
nOE/nRE	gpmc_noe_nre	O	Output enable (active low). Also used as read enable (active low) for NAND protocol memories.
nWE	gpmc_nwe	O	Write enable (active low)
nBE0/CLE	gpmc_nbe0_cle	O	Lower-byte enable (active low). Also used as command latch enable for NAND protocol memories.
nBE1	gpmc_nbe1	O	Upper-byte enable (active low).
nWP	gpmc_nwp	O	Write protect (active low)
WAIT[2:0]	gpmc_wait[2:0]	I	External wait signal for NOR and NAND protocol memories. The wait signals can be mapped on any of the chip-selects.

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)

(2) This output signal is also used as retiming input (the INPUTENABLE bit in the corresponding pad configuration register must be set to 1).

A.4.2 EMIF Controller

NOTE: The OMAP5432 is designed to interface with DDR3/DDR3L memories mounted on board (PCB). LPDDR2-SDRAM memories are not supported.

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NOTE: Orange highlighting in Table A-5 indicate signals with no dedicated balls in OMAP5432 device.

Table A-5 describes the module signals and specifies their links to functions used to connect LPDDR2 type of memories. The LPDDR2 data PHY signals are shared with the DDR3 ones.

Table A-5. I/O Signals (LPDDR2)

Module Pin	Device I/O Signal	I/O[1]	Description
EMIF1 Data PHYs			
DQ[31:0]	ddrch1_dq[31:0]	I/O	Data bus
DQM[3:0]	ddrch1_dm[3:0]	I/O	Data mask
DQS[3:0]	ddrch1_dqs[3:0]	I/O	Data strobe
NDQS[3:0]	ddrch1_ndqs[3:0]	I/O	Data strobe invert
EMIF1 LPDDR2 Command PHY			
CA[9:0]	lpddr2ch1_ca[9:0]	O	Double-data rate (DDR) command/address
CK	lpddr2ch1_ck	O	Clock
NCK	lpddr2ch1_nck	O	Clock invert
NCS[1:0]	lpddr2ch1_ncs[1:0]	O	Chip-selects 1:0 (active low)
CKE[1:0]	lpddr2ch1_cke[1:0]	O	Clock-enables 1:0
EMIF2 Data PHYs			
DQ[31:0]	ddrch2_dq[31:0]	I/O	Data bus
DQM[3:0]	ddrch2_dm[3:0]	I/O	Data mask
DQS[3:0]	ddrch2_dqs[3:0]	I/O	Data strobe
NDQS[3:0]	ddrch2_ndqs[3:0]	I/O	Data strobe invert
EMIF2 LPDDR2 Command PHY			
CA[9:0]	lpddr2ch2_ca[9:0]	O	DDR command/address
CK	lpddr2ch2_ck	O	Clock
NCK	lpddr2ch2_nck	O	Clock invert
NCS[1:0]	lpddr2ch2_ncs[1:0]	O	Chip-selects 1:0 (active low)
CKE[1:0]	lpddr2ch2_cke[1:0]	O	Clock-enables 1:0

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)

Table A-6 describes the module signals and specifies their links to functions used to connect DDR3 type of memories. DDR3 data PHY signals are shared with the LPDDR2 ones.

Table A-6. I/O Signals (DDR3)

Module Pin	Device I/O Signal	I/O[1]	Description
EMIF1 Data PHYs			
DQ[31:0]	ddrch1_dq[31:0]	I/O	Data bus
DQM[3:0]	ddrch1_dm[3:0]	I/O	Data mask
DQS[3:0]	ddrch1_dqs[3:0]	I/O	Data strobe
NDQS[3:0]	ddrch1_ndqs[3:0]	I/O	Data strobe invert
EMIF1 DDR3 Command PHYs			
A[15:0]	ddr3ch1_a[15:0]	O	Row/column address bus
BA[2:0]	ddr3ch1_ba[2:0]	O	Bank select
CKA	ddr3ch1_cka	O	Differential clock, set a (DDR3 command PHY 0)
NCKA	ddr3ch1_ncka	O	Differential clock, set a (DDR3 command PHY 0)
C KiB	ddr3ch1_ckb	O	Differential clock, set b (DDR3 command PHY 1)
NC KiB	ddr3ch1_nckb	O	Differential clock, set b (DDR3 command PHY 1)

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)

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Table A-6. I/O Signals (DDR3) (continued)

Module Pin	Device I/O Signal	I/O[1]	Description
NCS[1:0]	ddr3ch1_ncs[1:0]	O	Rank select 1:0 (active low)
CKE[1:0]	ddr3ch1_cke[1:0]	O	Clock enable for rank 1:0
NCAS	ddr3ch1_ncas	O	Command
NRAS	ddr3ch1_nras	O	Command
NWE	ddr3ch1_nwe	O	Command
NRESET	ddr3ch1_nreset	O	Asynchronous reset (active low)
ODT[1:0]	ddr3ch1_odt[1:0]	O	On-die termination for rank 1:0
EMIF2 Data PHYs			
DQ[31:0]	ddrch2_dq[31:0]	I/O	Data bus
DQM[3:0]	ddrch2_dm[3:0]	I/O	Data mask
DQS[3:0]	ddrch2_dqs[3:0]	I/O	Data strobe
NDQS[3:0]	ddrch2_ndqs[3:0]	I/O	Data strobe invert
EMIF2 DDR3 Command PHYs			
A[15:0]	ddr3ch2_a[15:0]	O	Row/column address bus
BA[2:0]	ddr3ch2_ba[2:0]	O	Bank select
CKA	ddr3ch2_cka	O	Differential clock, set a (DDR3 command PHY 0)
NCKA	ddr3ch2_ncka	O	Differential clock, set a (DDR3 command PHY 0)
C KiB	ddr3ch2_ckb	O	Differential clock, set b (DDR3 command PHY 1)
NC KiB	ddr3ch2_nckb	O	Differential clock, set b (DDR3 command PHY 1)
NCS[1:0]	ddr3ch2_ncs[1:0]	O	Rank select 1:0 (active low)
CKE[1:0]	ddr3ch2_cke[1:0]	O	Clock enable for rank 1:0
NCAS	ddr3ch2_ncas	O	Command
NRAS	ddr3ch2_nras	O	Command
NWE	ddr3ch2_nwe	O	Command
NRESET	ddr3ch2_nreset	O	Asynchronous reset (active low)
ODT[1:0]	ddr3ch2_odt[1:0]	O	On-die termination for rank 1:0

A.5 System DMA

A.5.1 DMA_SYSTEM Environment

The external DMA request sys_ndmareq1cannot be used with the OMAP5432 device. Also, sys_ndmareq0 is available on different device ball than in OMAP5430, that is, on uart6_rts in mux mode 1.

Table A-7 describes the external DMA_SYSTEM request signals.

Table A-7. External DMA_SYSTEM Request Signals

Module Signal Name	Device Signal Name	I/O[1]	Description
EXT_SYS_DREQ_0	sys_ndmareq0	I	External DMA request 0 (system expansion)
EXT_SYS_DREQ_1	sys_ndmareq1	I	External DMA request 1 (system expansion)

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)

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A.5.2 DMA_SYSTEM Integration

A.5.2.1 DMA Requests to the DMA_SYSTEM Controller

NOTE: This subsection provides a quick reference about the unavailable modules, which interact with the DMA_SYSTEM. Cells highlighted in orange in the tables indicate modules with removed functionality in the OMAP5432 device. These modules are still present on the die; therefore, their mappings are provided to control their activity and for debug purposes.

Table A-8 lists the DMA_SYSTEM request mapping of the OMAP5432 devices.

Table A-8. DMA_SYSTEM Controller Request Mapping

DMA Request Line	Source	Description
DMA_SYSTEM_DREQ_0	Reserved	Reserved
DMA_SYSTEM_DREQ_1	EXT_SYS_DREQ_0	External DMA request 0 (system expansion)
DMA_SYSTEM_DREQ_2	EXT_SYS_DREQ_1	External DMA request 1 (system expansion)
DMA_SYSTEM_DREQ_3	GPMC_DREQ	GPMC data transmit request from prefetch engine
DMA_SYSTEM_DREQ_4	Reserved	Reserved
DMA_SYSTEM_DREQ_5	DISPC_DREQ	Frame update request
DMA_SYSTEM_DREQ_6	CT_TBR_DREQ	DEBUG subsystem CT_TBR request
DMA_SYSTEM_DREQ_7	MCASP_DREQ_AXEVT	MCASP transmit request
DMA_SYSTEM_DREQ_8	ISS_DREQ_1	Imaging subsystem request 1
DMA_SYSTEM_DREQ_9	ISS_DREQ_2	Imaging subsystem request 2
DMA_SYSTEM_DREQ_10	Reserved	Reserved
DMA_SYSTEM_DREQ_11	ISS_DREQ_3	Imaging subsystem request 3
DMA_SYSTEM_DREQ_12	ISS_DREQ_4	Imaging subsystem request 4
DMA_SYSTEM_DREQ_13	RFBI_DREQ	Display subsystem RFBI request
DMA_SYSTEM_DREQ_14	MCSPI3_DREQ_TX0	MCSPI3 transmit request channel 0
DMA_SYSTEM_DREQ_15	MCSPI3_DREQ_RX0	MCSPI3 receive request channel 0
DMA_SYSTEM_DREQ_16	MCBSP2_DREQ_TX	MCBSP2 transmit request
DMA_SYSTEM_DREQ_17	MCBSP2_DREQ_RX	MCBSP2 receive request
DMA_SYSTEM_DREQ_18	MCBSP3_DREQ_TX	MCBSP3 transmit request
DMA_SYSTEM_DREQ_19	MCBSP3_DREQ_RX	MCBSP3 receive request
DMA_SYSTEM_DREQ_20	Reserved	Reserved
DMA_SYSTEM_DREQ_21	Reserved	Reserved
DMA_SYSTEM_DREQ_22	Reserved	Reserved
DMA_SYSTEM_DREQ_23	Reserved	Reserved
DMA_SYSTEM_DREQ_24	I2C3_DREQ_TX	I2C3 transmit request
DMA_SYSTEM_DREQ_25	I2C3_DREQ_RX	I2C3 receive request
DMA_SYSTEM_DREQ_26	I2C1_DREQ_TX	I2C1 transmit request
DMA_SYSTEM_DREQ_27	I2C1_DREQ_RX	I2C1 receive request
DMA_SYSTEM_DREQ_28	I2C2_DREQ_TX	I2C2 transmit request
DMA_SYSTEM_DREQ_29	I2C2_DREQ_RX	I2C2 receive request
DMA_SYSTEM_DREQ_30	ISS_DREQ_5	Imaging subsystem request 5
DMA_SYSTEM_DREQ_31	ISS_DREQ_6	Imaging subsystem request 6
DMA_SYSTEM_DREQ_32	MCBSP1_DREQ_TX	MCBSP1 transmit request
DMA_SYSTEM_DREQ_33	MCBSP1_DREQ_RX	MCBSP1 receive request
DMA_SYSTEM_DREQ_34	MCSPI1_DREQ_TX0	MCSPI1 transmit request channel 0
DMA_SYSTEM_DREQ_35	MCSPI1_DREQ_RX0	MCSPI1 receive request channel 0
DMA_SYSTEM_DREQ_36	MCSPI1_DREQ_TX1	MCSPI1 transmit request channel 1

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Table A-8. DMA_SYSTEM Controller Request Mapping (continued)

DMA Request Line	Source	Description
DMA_SYSTEM_DREQ_37	MCSPI1_DREQ_RX1	MCSPI1 receive request channel 1
DMA_SYSTEM_DREQ_38	MCSPI1_DREQ_TX2	MCSPI1 transmit request channel 2
DMA_SYSTEM_DREQ_39	MCSPI1_DREQ_RX2	MCSPI1 receive request channel 2
DMA_SYSTEM_DREQ_40	MCSPI1_DREQ_TX3	MCSPI1 transmit request channel 3
DMA_SYSTEM_DREQ_41	MCSPI1_DREQ_RX3	MCSPI1 receive request channel 3
DMA_SYSTEM_DREQ_42	MCSPI2_DREQ_TX0	MCSPI2 transmit request channel 0
DMA_SYSTEM_DREQ_43	MCSPI2_DREQ_RX0	MCSPI2 receive request channel 0
DMA_SYSTEM_DREQ_44	MCSPI2_DREQ_TX1	MCSPI2 transmit request channel 1
DMA_SYSTEM_DREQ_45	MCSPI2_DREQ_RX1	MCSPI2 receive request channel 1
DMA_SYSTEM_DREQ_46	MMC2_DREQ_TX	MMC2 transmit request
DMA_SYSTEM_DREQ_47	MMC2_DREQ_RX	MMC2 receive request
DMA_SYSTEM_DREQ_48	UART1_DREQ_TX	UART1 transmit request
DMA_SYSTEM_DREQ_49	UART1_DREQ_RX	UART1 receive request
DMA_SYSTEM_DREQ_50	UART2_DREQ_TX	UART2 transmit request
DMA_SYSTEM_DREQ_51	UART2_DREQ_RX	UART2 receive request
DMA_SYSTEM_DREQ_52	UART3_DREQ_TX	UART3 transmit request
DMA_SYSTEM_DREQ_53	UART3_DREQ_RX	UART3 receive request
DMA_SYSTEM_DREQ_54	UART4_DREQ_TX	UART4 transmit request
DMA_SYSTEM_DREQ_55	UART4_DREQ_RX	UART4 receive request
DMA_SYSTEM_DREQ_56	MMC4_DREQ_TX	MMC4 transmit request
DMA_SYSTEM_DREQ_57	MMC4_DREQ_RX	MMC4 receive request
DMA_SYSTEM_DREQ_58	MMC5_DREQ_TX	MMC5 transmit request
DMA_SYSTEM_DREQ_59	MMC5_DREQ_RX	MMC5 receive request
DMA_SYSTEM_DREQ_60	MMC1_DREQ_TX	MMC1 transmit request
DMA_SYSTEM_DREQ_61	MMC1_DREQ_RX	MMC1 receive request
DMA_SYSTEM_DREQ_62	UART5_DREQ_TX	UART5 transmit request
DMA_SYSTEM_DREQ_63	UART5_DREQ_RX	UART5 receive request
DMA_SYSTEM_DREQ_64	MCPDM_DREQ_UP_LINK	MCPDM uplink request
DMA_SYSTEM_DREQ_65	MCPDM_DREQ_DN_LINK	MCPDM downlink request
DMA_SYSTEM_DREQ_66	DMIC_DREQ	DMIC DMA request
DMA_SYSTEM_DREQ_67	Reserved	Reserved
DMA_SYSTEM_DREQ_68	Reserved	Reserved
DMA_SYSTEM_DREQ_69	MCSPI4_DREQ_TX0	MCSPI4 transmit request channel 0
DMA_SYSTEM_DREQ_70	MCSPI4_DREQ_RX0	MCSPI4 receive request channel 0
DMA_SYSTEM_DREQ_71	DSI1_A_DREQ_0	Display subsystem DSI1_A request 0
DMA_SYSTEM_DREQ_72	DSI1_A_DREQ_1	Display subsystem DSI1_A request 1
DMA_SYSTEM_DREQ_73	DSI1_A_DREQ_2	Display subsystem DSI1_A request 2
DMA_SYSTEM_DREQ_74	DSI1_A_DREQ_3	Display subsystem DSI1_A request 3
DMA_SYSTEM_DREQ_75	HDMI_DREQ	Display subsystem HDMI audio request
DMA_SYSTEM_DREQ_76	MMC3_DREQ_TX	MMC3 transmit request
DMA_SYSTEM_DREQ_77	MMC3_DREQ_RX	MMC3 receive request
DMA_SYSTEM_DREQ_78	UART6_DREQ_TX	UART6 transmit request
DMA_SYSTEM_DREQ_79	UART6_DREQ_RX	UART6 receive request
DMA_SYSTEM_DREQ_80	DSI1_C_DREQ_0	Display subsystem DSI1_C request 0
DMA_SYSTEM_DREQ_81	DSI1_C_DREQ_1	Display subsystem DSI1_C request 1
DMA_SYSTEM_DREQ_82	DSI1_C_DREQ_2	Display subsystem DSI1_C request 2
DMA_SYSTEM_DREQ_83	DSI1_C_DREQ_3	Display subsystem DSI1_C request 3

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Table A-8. DMA_SYSTEM Controller Request Mapping (continued)

DMA Request Line	Source	Description
DMA_SYSTEM_DREQ_84	Reserved	Reserved
DMA_SYSTEM_DREQ_85	Reserved	Reserved
DMA_SYSTEM_DREQ_86	Reserved	Reserved
DMA_SYSTEM_DREQ_87	Reserved	Reserved
DMA_SYSTEM_DREQ_88	Reserved	Reserved
DMA_SYSTEM_DREQ_89	Reserved	Reserved
DMA_SYSTEM_DREQ_90	Reserved	Reserved
DMA_SYSTEM_DREQ_91	Reserved	Reserved
DMA_SYSTEM_DREQ_92	Reserved	Reserved
DMA_SYSTEM_DREQ_93	Reserved	Reserved
DMA_SYSTEM_DREQ_94	Reserved	Reserved
DMA_SYSTEM_DREQ_95	Reserved	Reserved
DMA_SYSTEM_DREQ_96	Reserved	Reserved
DMA_SYSTEM_DREQ_97	Reserved	Reserved
DMA_SYSTEM_DREQ_98	Reserved	Reserved
DMA_SYSTEM_DREQ_99	Reserved	Reserved
DMA_SYSTEM_DREQ_100	AESS_DREQ_FIFO0	Audio back-end (audio engine) – request FIFO 0
DMA_SYSTEM_DREQ_101	AESS_DREQ_FIFO1	Audio back-end (audio engine) – request FIFO 1
DMA_SYSTEM_DREQ_102	AESS_DREQ_FIFO2	Audio back-end (audio engine) – request FIFO 2
DMA_SYSTEM_DREQ_103	AESS_DREQ_FIFO3	Audio back-end (audio engine) – request FIFO 3
DMA_SYSTEM_DREQ_104	AESS_DREQ_FIFO4	Audio back-end (audio engine) – request FIFO 4
DMA_SYSTEM_DREQ_105	AESS_DREQ_FIFO5	Audio back-end (audio engine) – request FIFO 5
DMA_SYSTEM_DREQ_106	AESS_DREQ_FIFO6	Audio back-end (audio engine) – request FIFO 6
DMA_SYSTEM_DREQ_107	AESS_DREQ_FIFO7	Audio back-end (audio engine) – request FIFO 7
DMA_SYSTEM_DREQ_108	Reserved	Reserved
DMA_SYSTEM_DREQ_109	Reserved	Reserved
DMA_SYSTEM_DREQ_110	Reserved	Reserved
DMA_SYSTEM_DREQ_111	Reserved	Reserved
DMA_SYSTEM_DREQ_112	Reserved	Reserved
DMA_SYSTEM_DREQ_113	Reserved	Reserved
DMA_SYSTEM_DREQ_114	Reserved	Reserved
DMA_SYSTEM_DREQ_115	Reserved	Reserved
DMA_SYSTEM_DREQ_116	Reserved	Reserved
DMA_SYSTEM_DREQ_117	Reserved	Reserved
DMA_SYSTEM_DREQ_118	Reserved	Reserved
DMA_SYSTEM_DREQ_119	Reserved	Reserved
DMA_SYSTEM_DREQ_120	Reserved	Reserved
DMA_SYSTEM_DREQ_121	Reserved	Reserved
DMA_SYSTEM_DREQ_122	Reserved	Reserved
DMA_SYSTEM_DREQ_123	I2C4_DREQ_TX	I2C4 transmit request
DMA_SYSTEM_DREQ_124	I2C4_DREQ_RX	I2C4 receive request
DMA_SYSTEM_DREQ_125	ISS_DREQ_7	Imaging subsystem request 7
DMA_SYSTEM_DREQ_126	ISS_DREQ_8	Imaging subsystem request 8

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A.6 Interrupt Controllers

A.6.1 Interrupt Controllers Environment

This section describes the INTC application fields from the environment point of view (external connections).

Table A-9 describes the I/O signals that can be used by external devices to generate interrupts to the INTC_MPU or INTC_IPU. Orange highlighting indicates the unavailable external interrupts in OMAP5432.

Table A-9. Interrupt Controllers I/O Signals

Signal Name	I/O[1]	Reset Value	Description	INTC_MPU	INTC_IPU
sys_nirq1	I	1	TWL-Power IC can use this pin to generate a system wake-up event to INTC_MPU.	✓	–
sys_nirq2	I	1	TWL-Audio IC can use this pin to generate a system wake-up event to INTC_MPU.	✓	–
gpio1_[7:0]	I/O	–	External devices can use GPIO modules to generate interrupts to INTC_MPU or INTC_IPU. There are eight dedicated interrupt lines (for GPIO1 to GPIO8) to the INTC_MPU and two dedicated interrupt lines (for GPIO1 and GPIO2) to the INTC_IPU. Each GPIO module can generate a single interrupt whenever there is at least one event in any one of the configured 32 GPIO inputs.	✓	✓
gpio1_[10:8]	I/O	–		✓	✓
gpio1_[31:11]	I/O	–		✓	✓
gpio2_[63:32]	I/O	–		✓	✓
gpio3_[75:64]	I/O	–		✓	–
gpio3_[91:76]	I/O	–		✓	–
gpio3_[93:92]	I/O	–		✓	–
gpio3_[95:94]	I/O	–		✓	–
gpio4_[127:96]	I/O	–		✓	–
gpio5_[144:128]	I/O	–		✓	–
gpio5_[146:145]	I/O	–		✓	–
gpio5_[148:147]	I/O	–		✓	–
gpio5_[151:149]	I/O	–		✓	–
gpio5_[159:152]	I/O	–		✓	–
gpio6_[191:160]	I/O	–		✓	–
gpio7_[223:192]	I/O	–		✓	–
gpio8_[255:224]	I/O	–		✓	–

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)

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A.6.2 Interrupt Controllers Integration

NOTE: This subsection provides a quick reference about the unavailable modules, which have their interrupt requests mapped on the MPU and IPU interrupt controllers (INTCs). Rows highlighted in orange indicate modules with removed functionality in the OMAP5432. These modules are still present on the die; therefore, their mappings are provided to control their activity and for debug purposes.

A.6.2.1 Interrupt Requests to INTC_MPU

Table A-10 shows the INTC_MPU interrupt mapping.

Table A-10. INTC_MPU Interrupt Mapping

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
MPU_IRQ_0	MPU_CLUSTER_IRQ_INTERR	MPU_CLUSTER	Illegal writes to interrupt controller memory map region(1)
MPU_IRQ_1	CS_CTI_MPU_C0_IRQ	CS_CTI_MPU_C0	TRIGOUT[6] of Cross Trigger Interface 0 (CTI0)(1)
MPU_IRQ_2	CS_CTI_MPU_C1_IRQ	CS_CTI_MPU_C1	TRIGOUT[6] of Cross Trigger Interface 1 (CTI1)(1)
MPU_IRQ_3	MPU_CLUSTER_IRQ_AXIERR	MPU_CLUSTER	Error indication for AXI write transactions with a BRESP error condition(1)
MPU_IRQ_4	ELM_IRQ	ELM	Error location process completion(2)
MPU_IRQ_5	Reserved	Reserved	Reserved
MPU_IRQ_6	Reserved	Reserved	Reserved
MPU_IRQ_7	EXT_SYS_IRQ_1	EXT_SYS	External interrupt (active low)
MPU_IRQ_8	Reserved	Reserved	Reserved
MPU_IRQ_9	L3_MAIN_IRQ_DBG_ERR	L3_MAIN	Reports debug errors on L3
MPU_IRQ_10	L3_MAIN_IRQ_APP_ERR	L3_MAIN	Reports application or nonattributable errors on L3
MPU_IRQ_11	PRM_IRQ_MPU	PRM	PRCM module
MPU_IRQ_12	DMA_SYSTEM_IRQ_0	DMA_SYSTEM	System DMA interrupt request 0(3)
MPU_IRQ_13	DMA_SYSTEM_IRQ_1	DMA_SYSTEM	System DMA interrupt request 1(3)
MPU_IRQ_14	DMA_SYSTEM_IRQ_2	DMA_SYSTEM	System DMA interrupt request 2(4)
MPU_IRQ_15	DMA_SYSTEM_IRQ_3	DMA_SYSTEM	System DMA interrupt request 3(4)
MPU_IRQ_16	L3_MAIN_IRQ_STAT_ALARM	L3_MAIN	L3 NoC Statistic Collector Alarm
MPU_IRQ_17	MCBSP1_IRQ	MCBSP1	McBSP1 / PORCOMMONIRQ: Common Synchronous Interrupt Request line(2)
MPU_IRQ_18	SMARTREFLEX_MPU_IRQ	SMARTREFLEX_MPU	SmartReflex MCU interrupt request
MPU_IRQ_19	SMARTREFLEX_CORE_IRQ	SMARTREFLEX_CORE	SmartReflex Core interrupt request
MPU_IRQ_20	GPMC_IRQ	GPMC	General-purpose memory controller module(2)
MPU_IRQ_21	GPU_IRQ	GPU	3D graphics module interrupt
MPU_IRQ_22	MCBSP2_IRQ	MCBSP2	McBSP 2 / PORCOMMONIRQ: Common Synchronous Interrupt Request line(2)
MPU_IRQ_23	MCBSP3_IRQ	MCBSP3	McBSP 3 / PORCOMMONIRQ: Common Synchronous Interrupt Request line(2)
MPU_IRQ_24	ISS_IRQ_5	ISS	Imaging subsystem interrupt request(4)
MPU_IRQ_25	DISPC_IRQ	DISPC	Display controller interrupt request(3)
MPU_IRQ_26	MAILBOX_IRQ_USER0	MAILBOX	Mailbox user 0 interrupt request
MPU_IRQ_27	Reserved	Reserved	Reserved
MPU_IRQ_28	DSP_IRQ_MMU	DSP	DSP MMU interrupt

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Table A-10. INTC_MPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
MPU_IRQ_29	GPIO1_IRQ_1	GPIO1	GPIO module 1 - interrupt 1[4]
MPU_IRQ_30	GPIO2_IRQ_1	GPIO2	GPIO module 2 - interrupt 1[4]
MPU_IRQ_31	GPIO3_IRQ_1	GPIO3	GPIO module 3 - interrupt 1
MPU_IRQ_32	GPIO4_IRQ_1	GPIO4	GPIO module 4 - interrupt 1
MPU_IRQ_33	GPIO5_IRQ_1	GPIO5	GPIO module 5 - interrupt 1
MPU_IRQ_34	GPIO6_IRQ_1	GPIO6	GPIO module 6 - interrupt 1
MPU_IRQ_35	GPIO7_IRQ_1	GPIO7	GPIO module 7 - interrupt 1
MPU_IRQ_36	WD_TIMER3_IRQ	WD_TIMER3	Watchdog timer module 3 overflow (watchdog controlled by Mini64)
MPU_IRQ_37	TIMER1_IRQ	TIMER1	General-purpose timer module 1 (Timer 1ms / Wakeup domain)
MPU_IRQ_38	TIMER2_IRQ	TIMER2	General-purpose timer module 2 (Timer 1ms / CORE domain)
MPU_IRQ_39	TIMER3_IRQ	TIMER3	General-purpose timer module 3[4]
MPU_IRQ_40	TIMER4_IRQ	TIMER4	General-purpose timer module 4[4]
MPU_IRQ_41	TIMER5_IRQ	TIMER5	General-purpose timer module 5 (Audio BE)[2]
MPU_IRQ_42	TIMER6_IRQ	TIMER6	General-purpose timer module 6 (Audio BE)[2]
MPU_IRQ_43	TIMER7_IRQ	TIMER7	General-purpose timer module 7 (Audio BE)[2]
MPU_IRQ_44	TIMER8_IRQ	TIMER8	General-purpose timer module 8 (Audio BE)[2]
MPU_IRQ_45	TIMER9_IRQ	TIMER9	General-purpose timer module 9[4]
MPU_IRQ_46	TIMER10_IRQ	TIMER10	General-purpose timer module 10 (Timer 1ms / CORE domain)
MPU_IRQ_47	TIMER11_IRQ	TIMER11	General-purpose timer module 11[4]
MPU_IRQ_48	MCSPI4_IRQ	MCSPI4	McSPI module 4
MPU_IRQ_49	Reserved	Reserved	Reserved
MPU_IRQ_50	Reserved	Reserved	Reserved
MPU_IRQ_51	Reserved	Reserved	Reserved
MPU_IRQ_52	Reserved	Reserved	Reserved
MPU_IRQ_53	DSI1_A_IRQ	DSI1_A	Display DSI1_A interrupt request[3]
MPU_IRQ_54	SATA_IRQ	SATA	SATA interrupt request
MPU_IRQ_55	DSI1_C_IRQ	DSI1_C	Display DSI1_C interrupt request[3]
MPU_IRQ_56	I2C1_IRQ	I2C1	I^2C module 1[4]
MPU_IRQ_57	I2C2_IRQ	I2C2	I^2C module 2[4]
MPU_IRQ_58	HDQ1W_IRQ	HDQ1W	HDQ1W module interrupt
MPU_IRQ_59	MMC5_IRQ	MMC5	MMC5 interrupt request[4]
MPU_IRQ_60	I2C5_IRQ	I2C5	I^2C module 5
MPU_IRQ_61	I2C3_IRQ	I2C3	I^2C module 3[4]
MPU_IRQ_62	I2C4_IRQ	I2C4	I^2C module 4[4]
MPU_IRQ_63	Reserved	Reserved	Reserved
MPU_IRQ_64	Reserved	Reserved	Reserved
MPU_IRQ_65	MCSPI1_IRQ	MCSPI1	McSPI module 1[3]
MPU_IRQ_66	MCSPI2_IRQ	MCSPI2	McSPI module 2[4]
MPU_IRQ_67	HSI_IRQ_MPU_P1	HSI	HSI interrupt request - Port 1 combined interrupt[4]
MPU_IRQ_68	HSI_IRQ_MPU_P2	HSI	HSI interrupt request - Port 2 combined interrupt[4]
MPU_IRQ_69	FDIF_IRQ_3	FDIF	Face detect interrupt 3
MPU_IRQ_70	UART4_IRQ	UART4	UART module 4
MPU_IRQ_71	HSI_IRQ_MPU_DMA	HSI	HSI DMA engine[4]
MPU_IRQ_72	UART1_IRQ	UART1	UART module 1
MPU_IRQ_73	UART2_IRQ	UART2	UART module 2
MPU_IRQ_74	UART3_IRQ	UART3	UART module 3 (also infrared - IRDA)[3]
MPU_IRQ_75	PBIAS_IRQ	PBIAS	Merged interrupt for PBIASlite1 and 2

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Table A-10. INTC_MPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
MPU_IRQ_76	USB_HOST_HS_IRQ_OHCI	USB_HOST_HS	USB_HOST_HS - OHCI controller interrupt
MPU_IRQ_77	USB_HOST_HS_IRQ_EHCI	USB_HOST_HS	USB_HOST_HS - EHCI controller interrupt(4)
MPU_IRQ_78	USB_TLL_HS_IRQ	USB_TLL_HS	USB_TLL_HS Interrupt(4)
MPU_IRQ_79	Reserved	Reserved	Reserved
MPU_IRQ_80	WD_TIMER2_IRQ	WD_TIMER2	WDT2 interrupt
MPU_IRQ_81	Reserved	Reserved	Reserved
MPU_IRQ_82	Reserved	Reserved	Reserved
MPU_IRQ_83	MMC1_IRQ	MMC1	MMC1_IRQ(3)
MPU_IRQ_84	Reserved	Reserved	Reserved
MPU_IRQ_85	Reserved	Reserved	Reserved
MPU_IRQ_86	MMC2_IRQ	MMC2	MMC/SDIO module 2(3)
MPU_IRQ_87	Reserved	Reserved	Reserved
MPU_IRQ_88	Reserved	Reserved	Reserved
MPU_IRQ_89	DEBUGSS_IRQ_CT_UART_TX	DEBUGSS	CT_UART interrupt generated when TX empty
MPU_IRQ_90	DEBUGSS_IRQ_CT_UART_RX	DEBUGSS	CT_UART interrupt generated when data ready on RX
MPU_IRQ_91	MCSPI3_IRQ	MCSPI3	McSPI module 3
MPU_IRQ_92	USB_OTG_SS_IRQ_CORE	USB_OTG_SS	USB_OTG_SS - interrupt CORE (main source of interrupts)(4)
MPU_IRQ_93	USB_OTG_SS_IRQ_WRP	USB_OTG_SS	USB_OTG_SS - Interrupt wrapper(4)
MPU_IRQ_94	MMC3_IRQ	MMC3	MMC/SDIO module 3(4)
MPU_IRQ_95	Reserved	Reserved	Reserved
MPU_IRQ_96	MMC4_IRQ	MMC4	MMC/SDIO module 4(4)
MPU_IRQ_97	Reserved	Reserved	Reserved
MPU_IRQ_98	Reserved	Reserved	Reserved
MPU_IRQ_99	AESS_IRQ_MPU	AESS	Audo engine subsystem interrupt (in ABE)
MPU_IRQ_100	IPU_IRQ_MPU	IPU	IPU MMU interrupt
MPU_IRQ_101	HDMI_IRQ	HDMI	Display HDMI interrupt request(3)
MPU_IRQ_102	SMARTREFLEX_MM_IRQ	SMARTREFLEX_MM	SmartReflex IVA interrupt request
MPU_IRQ_103	IVA_IRQ_SYNC_1	IVA	Sync interrupt from ICONT2 (VDMA)(3)
MPU_IRQ_104	IVA_IRQ_SYNC_0	IVA	Sync interrupt from ICONT1(3)
MPU_IRQ_105	UART5_IRQ	UART5	UART module 5
MPU_IRQ_106	UART6_IRQ	UART6	UART module 6
MPU_IRQ_107	IVA_IRQ_MAILBOX_0	IVA	IVA-HD subsystem interrupt request (Mailbox interrupt 0)
MPU_IRQ_108	MCASP_IRQ_AREVT	MCASP	McASP receive interrupt (audio BE)(2)
MPU_IRQ_109	MCASP_IRQ_AXEVT	MCASP	McASP transmit interrupt (audio BE)(2)
MPU_IRQ_110	EMIF1_IRQ	EMIF1	EMIF1 interrupt request
MPU_IRQ_111	EMIF2_IRQ	EMIF2	EMIF2 interrupt request
MPU_IRQ_112	MCPDM_IRQ	MCPDM	McPDM interrupt (audio BE)(2)
MPU_IRQ_113	DMM_IRQ	DMM	DMM interrupt(4)
MPU_IRQ_114	DMIC_IRQ	DMIC	DMIC interrupt (audio BE)(2)
MPU_IRQ_115	Reserved	Reserved	Reserved
MPU_IRQ_116	Reserved	Reserved	Reserved
MPU_IRQ_117	Reserved	Reserved	Reserved

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Table A-10. INTC_MPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
MPU_IRQ_118	Reserved	Reserved	Reserved
MPU_IRQ_119	EXT_SYS_IRQ_2	EXT_SYS	External interrupt 2 (active low)
MPU_IRQ_120	KBD_IRQ	KBD	Keyboard controller interrupt
MPU_IRQ_121	GPIO8_IRQ_1	GPIO8	GPIO module 8 - interrupt 1
MPU_IRQ_122	Reserved	Reserved	Reserved
MPU_IRQ_123	Reserved	Reserved	Reserved
MPU_IRQ_124	Reserved	Reserved	Reserved
MPU_IRQ_125	BB2D_IRQ	BB2D	BB2D interrupt request
MPU_IRQ_126	CTRL_MODULE_CORE_IRQ_THERMAL_ALERT	CTRL_MODULE_CORE	Thermal alert is generated by the CTRL_MODULE when one of the three thermal sensors go over a defined threshold value.
MPU_IRQ_127	Reserved	Reserved	Reserved
MPU_IRQ_128	Reserved	Reserved	Reserved
MPU_IRQ_129	Reserved	Reserved	Reserved
MPU_IRQ_130	Reserved	Reserved	Reserved
MPU_IRQ_131	MPU_CLUSTER_IRQ_PMU_C0	MPU_CLUSTER	PMU Interrupt signal from MPU core 0
MPU_IRQ_132	MPU_CLUSTER_IRQ_PMU_C1	MPU_CLUSTER	PMU Interrupt signal from MPU core 1
MPU_IRQ_133	Reserved	Reserved	Reserved
MPU_IRQ_134	Reserved	Reserved	Reserved
MPU_IRQ_135	Reserved	Reserved	Reserved
MPU_IRQ_136	Reserved	Reserved	Reserved
MPU_IRQ_137	Reserved	Reserved	Reserved
MPU_IRQ_138	Reserved	Reserved	Reserved
MPU_IRQ_139	Reserved	Reserved	Reserved
MPU_IRQ_140	Reserved	Reserved	Reserved
MPU_IRQ_141	Reserved	Reserved	Reserved
MPU_IRQ_142	Reserved	Reserved	Reserved
MPU_IRQ_143	Reserved	Reserved	Reserved
MPU_IRQ_144	Reserved	Reserved	Reserved
MPU_IRQ_145	Reserved	Reserved	Reserved
MPU_IRQ_146	Reserved	Reserved	Reserved
MPU_IRQ_147	Reserved	Reserved	Reserved
MPU_IRQ_148	Reserved	Reserved	Reserved
MPU_IRQ_149	Reserved	Reserved	Reserved
MPU_IRQ_150	Reserved	Reserved	Reserved
MPU_IRQ_151	Reserved	Reserved	Reserved
MPU_IRQ_152	Reserved	Reserved	Reserved
MPU_IRQ_153	Reserved	Reserved	Reserved
MPU_IRQ_154	Reserved	Reserved	Reserved
MPU_IRQ_155	Reserved	Reserved	Reserved
MPU_IRQ_156	Reserved	Reserved	Reserved
MPU_IRQ_157	Reserved	Reserved	Reserved
MPU_IRQ_158	Reserved	Reserved	Reserved
MPU_IRQ_159	Reserved	Reserved	Reserved

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(1) Internally generated within the MPU subsystem
(2) Shared with INTC_DSP
(3) Shared with INTC_DSP and INTC_IPU
(4) Shared with INTC_IPU

A.6.2.2 Interrupt Requests to INTC_IPU

Table A-11 shows the INTC_IPU interrupt mapping.

Table A-11. INTC_IPU Interrupt Mapping

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
IPU_IRQ_0	–	–	MSP initial value in exception vector table
IPU_IRQ_1	RESET_IRQ	RESET	Reset
IPU_IRQ_2	NMI_IRQ	NMI	External NMI inputs(1)
IPU_IRQ_3	HARD_FAULT_IRQ	HARD_FAULT	All fault conditions, if the fault handle is not enabled(1)
IPU_IRQ_4	MEM_MANAGE_FAULT_IRQ	MEM_MANAGE_FAULT	Memory management fault; access to illegal locations(1)
IPU_IRQ_5	BUS_FAULT_IRQ	BUS_FAULT	Bus error (on AHB interface)(1)
IPU_IRQ_6	USAGE_FAULT_IRQ	USAGE_FAULT	Program error(1)
IPU_IRQ_7	Reserved	Reserved	Reserved
IPU_IRQ_8	Reserved	Reserved	Reserved
IPU_IRQ_9	Reserved	Reserved	Reserved
IPU_IRQ_10	Reserved	Reserved	Reserved
IPU_IRQ_11	SV_CALL_IRQ	SV_CALL	Service system call(1)
IPU_IRQ_12	DEBUG_MON_IRQ	DEBUG_MON	BP, WP or external debug request(1)
IPU_IRQ_13	Reserved	Reserved	Reserved
IPU_IRQ_14	PEND_SV_IRQ	PEND_SV	Pendable request for system device(1)
IPU_IRQ_15	SYS_TICK_TIMER_IRQ	SYS_TICK_TIMER	System tick timer has fired(1)
IPU_IRQ_16	XLATE_MMU_FAULT_IRQ	XLATE_MMU_FAULT	xlate_mmu_fault (from L2_MMU)(2)
IPU_IRQ_17	SCACHE_MMU_IRQ	SCACHE_MMU	Shared cache or MMU maintenance complete(2)
IPU_IRQ_18	CTM_TIM_EVENT1_IRQ	CTM_TIM_EVENT1	CTM timer event (timer 1)(2)
IPU_IRQ_19	SPINLOCK_IRQ	SPINLOCK	Semaphore interrupt (1 to each core)(2)
IPU_IRQ_20	ICE_NEMU_IRQ	ICE_NEMU	ICECrusher (1 to each core)(2)
IPU_IRQ_21	IPU_IMP_FAULT_IRQ	IPU_IMP_FAULT	Ducati imprecise fault (from interconnect)(2)
IPU_IRQ_22	CTM_TIM_EVENT2_IRQ	CTM_TIM_EVENT2	CTM timer event (timer 2)(2)
IPU_IRQ_23	DISPC_IRQ	DISPC	Display controller interrupt request(3)
IPU_IRQ_24	DSI1_A_IRQ	DSI1_A	Display DSI1_A interrupt request(3)
IPU_IRQ_25	Reserved	Reserved	Reserved
IPU_IRQ_26	HDMI_IRQ	HDMI	Display HDMI interrupt request(3)
IPU_IRQ_27	ISS_IRQ_0	ISS	Interrupt from ISS
IPU_IRQ_28	ISS_IRQ_1	ISS	Interrupt from ISS
IPU_IRQ_29	ISS_IRQ_2	ISS	Interrupt from ISS
IPU_IRQ_30	ISS_IRQ_3	ISS	Interrupt from ISS
IPU_IRQ_31	ISS_IRQ_4	ISS	Interrupt from ISS(4)
IPU_IRQ_32	ISS_IRQ_5	ISS	Interrupt from ISS(5)
IPU_IRQ_33	FDIF_IRQ_1	FDIF	Face detect interrupt 1
IPU_IRQ_34	DMA_SYSTEM_IRQ_0	DMA_SYSTEM	System DMA interrupt request 0(3)
IPU_IRQ_35	DMA_SYSTEM_IRQ_1	DMA_SYSTEM	System DMA interrupt request 1(3)
IPU_IRQ_36	DMA_SYSTEM_IRQ_2	DMA_SYSTEM	System DMA interrupt request 2(5)

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Table A-11. INTC_IPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
IPU_IRQ_37	DMA_SYSTEM_IRQ_3	DMA_SYSTEM	System DMA interrupt request 3(5)
IPU_IRQ_38	IVA_IRQ_MAILBOX_2	IVA	IVA-HD subsystem interrupt request (Mailbox interrupt 2)
IPU_IRQ_39	IVA_IRQ_SYNC_1	IVA	Sync interrupt from ICONT2 (VDMA)(3)
IPU_IRQ_40	IVA_IRQ_SYNC_0	IVA	Sync interrupt from ICONT1(3)
IPU_IRQ_41	I2C1_IRQ	I2C1	I^2C module 1(5)
IPU_IRQ_42	I2C2_IRQ	I2C2	I^2C module 2(5)
IPU_IRQ_43	I2C3_IRQ	I2C3	I^2C module 3(5)
IPU_IRQ_44	I2C4_IRQ	I2C4	I^2C module 4(5)
IPU_IRQ_45	UART3_IRQ	UART3	UART module 3 (also infrared - IRDA)(3)
IPU_IRQ_46	L3_MAIN_IRQ_APP_ERR	L3_MAIN	Reports application or nonattributable errors on L3
IPU_IRQ_47	PRM_IRQ_IPU	PRM	PRCM module
IPU_IRQ_48	SMARTREFLEX_CORE_IRQ	SMARTREFLEX_CORE	SmartReflex Core or SmartReflex MM
IPU_IRQ_49	HSI_IRQ_MPU_DMA	HSI	HSI - MPU DMA interrupt request(5)
IPU_IRQ_50	MAILBOX_IRQ_USER2	MAILBOX	Mailbox user 2 interrupt request
IPU_IRQ_51	GPIO1_IRQ_1	GPIO1	GPIO module 1 - interrupt 1(5)
IPU_IRQ_52	GPIO2_IRQ_1	GPIO2	GPIO module 2 - interrupt 1(5)
IPU_IRQ_53	TIMER3_IRQ	TIMER3	General-purpose timer module 3(5)
IPU_IRQ_54	TIMER4_IRQ	TIMER4	General-purpose timer module 4(5)
IPU_IRQ_55	TIMER9_IRQ	TIMER9	General-purpose timer module 9(5)
IPU_IRQ_56	TIMER11_IRQ	TIMER11	General-purpose timer module 11(5)
IPU_IRQ_57	MCSPI1_IRQ	MCSPI1	McSPI module 1(3)
IPU_IRQ_58	MCSPI2_IRQ	MCSPI2	McSPI module 2(5)
IPU_IRQ_59	DSI1_C_IRQ	DSI1_C	Display DSI1_C interrupt request(3)
IPU_IRQ_60	Reserved	Reserved	Reserved
IPU_IRQ_61	Reserved	Reserved	Reserved
IPU_IRQ_62	Reserved	Reserved	Reserved
IPU_IRQ_63	Reserved	Reserved	Reserved
IPU_IRQ_64	DMM_IRQ	DMM	DMM interrupt(5)
IPU_IRQ_65	BB2D_IRQ	BB2D	BB2D interrupt request
IPU_IRQ_66	MMC1_IRQ	MMC1	MMC/SDIO module 1(3)
IPU_IRQ_67	MMC2_IRQ	MMC2	MMC/SDIO module 2(3)
IPU_IRQ_68	MMC3_IRQ	MMC3	MMC/SDIO module 3(5)
IPU_IRQ_69	Reserved	Reserved	Reserved
IPU_IRQ_70	Reserved	Reserved	Reserved
IPU_IRQ_71	Reserved	Reserved	Reserved
IPU_IRQ_72	Reserved	Reserved	Reserved
IPU_IRQ_73	USB_HOST_HS_IRQ_EHCI	USB_HOST_HS	USB_HOST_HS - Interrupt EHCI controller(5)
IPU_IRQ_74	USB_TLL_HS_IRQ	USB_TLL_HS	USB_TLL_HS Interrupt(5)
IPU_IRQ_75	Reserved	Reserved	Reserved
IPU_IRQ_76	USB_OTG_SS_IRQ_CORE	USB_OTG_SS	USB_OTG_SS controller - interrupt CORE (main interrupt source)(5)
IPU_IRQ_77	USB_OTG_SS_IRQ_WRP	USB_OTG_SS	USB_OTG_SS - Interrupt wrapper(5)
IPU_IRQ_78	HSI_IRQ_MPU_P1	HSI	HSI interrupt request - Port 1 combined interrupt(5)

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Table A-11. INTC_IPU Interrupt Mapping (continued)

Interrupt Line (Destination)	Interrupt Line (Source)	Root Source Module	Description
IPU_IRQ_79	HSI_IRQ_MPU_P2	HSI	HSI interrupt request - Port 2 combined interrupt(5)

(1) Internally generated within IPU_Cx (where x = 0, 1)
(2) Internally generated within IPU subsystem
(3) Shared with INTC_DSP and INTC_MPU
(4) Shared with INTC_DSP
(5) Shared with INTC_MPU

A.6.3 INTCs Use Guidelines

All interrupts that are highlighted in orange must be kept masked (reset default state) during normal operation.

For information about the INTC_MPU, see *ARM Cortex-A15 MP Core Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

For information about the INTC_IPU (NVIC), see *ARM Cortex-M4 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

A.7 System Control Module

A.7.1 Control Module Signals

Table A-12 lists the control module hardware observability outputs configured to observe the debug signals of the device module. It describes the module signals and specifies their links to functions. Highlighted signals are not available in OMAP5432.

Table A-12. Control Module I/O Description

Signal	I/O(1)	Description	Reset Value(2)
hw_dbg[9:0]	O	Internal hardware observability signals 0 to 9	HiZ
hw_dbg[12:10]	O	Internal hardware observability signals 10 to 12	HiZ
hw_dbg[31:13]	O	Internal hardware observability signals 13 to 31	HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

A.7.2 Pad Multiplexing Register Fields

NOTE: This subsection provides a quick reference about the device pads, that are not connected to any pin. Cells highlighted in orange in the tables indicate pads with removed functionality in the OMAP5432 device. These pads are still present on the die; therefore, their configuration settings are provided to control their activity and for debug purposes.

Table A-13 and Table A-14 provide for each pad configuration register field the address offset and associated signal name for each multiplexing mode (as set by the MUXMODE bit field). Mode 0 is always defined. Modes with no signal name are undefined for the given pad.

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Table A-13. Device Wake-Up Control Module Pad Configuration Register Fields

CTRL_MODULE_WKUP_PAD [Register name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_LLIA_WAKEREQIN_PAD1_LLIB_WAKEREQIN[15:0]	0x040	llia_wakereqin	c2c_wakereqin				hw_wkdbg14	gpio1_wk14	safe_mode_wakeup1
CONTROL_WKUP_PAD0_LLIA_WAKEREQIN_PAD1[31:16]	0x040	llib_wakereqin	sys_c2c_pwkup				hw_wkdbg13	gpio1_wk15	safe_mode_wakeup0
CONTROL_WKUP_PAD0_DRM_EMU0_PAD1_DRM_EMU1[15:0]	0x044	drm_emu0					hw_wkdbg6	gpio1_wk6	safe_mode_wakeup2
CONTROL_WKUP_PAD0_DRM_EMU0_PAD1_DRM_EMU1[31:16]	0x044	drm_emu1					hw_wkdbg7	gpio1_wk7	safe_mode_wakeup3
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK[15:0]	0x048	jtag_ntrst							safe_mode_wakeup4
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK[31:16]	0x048	jtag_tck							safe_mode_wakeup5
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMSC[15:0]	0x04C	jtag_rtck							safe_mode_wakeup6
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMSC[31:16]	0x04C	jtag_tmsc							safe_mode_wakeup7
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO[15:0]	0x050	jtag_tdi							safe_mode_wakeup8
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO[31:16]	0x050	jtag_tdo							safe_mode_wakeup9
CONTROL_WKUP_PAD0_SYS_32K_PAD1_FREF_CLK_IOREQ[15:0]	0x054	sys_32k							
CONTROL_WKUP_PAD0_SYS_32K_PAD1_FREF_CLK_IOREQ[31:16]	0x054	fref_clk_ioreq						gpio1_wk13	safe_mode_wakeup10
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK1_OUT[15:0]	0x058	fref_clk0_out					hw_wkdbg9	gpio1_wk12	safe_mode_wakeup11
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK1_OUT[31:16]	0x058	fref_clk1_out					hw_wkdbg5	gpio1_wk11	safe_mode_wakeup12

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Table A-13. Device Wake-Up Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_WKUP_PAD [Register name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_FREF_CLK2_OUT_PAD1_FREF_CLK2_REQ[15:0]	0x05C	fref_clk2_out					hw_wkdbg10	gpio1_wk10	safe_mode_wakeup13
CONTROL_WKUP_PAD0_FREF_CLK2_OUT_PAD1_FREF_CLK2_REQ[31:16]	0x05C	fref_clk2_req	fref_clk3_out		sys_ndmareq0		hw_wkdbg11	gpio1_wk9	safe_mode_wakeup14
CONTROL_WKUP_PAD0_FREF_CLK1_REQ_PAD1_SYS_NRESPWRON[15:0]	0x060	fref_clk1_req			sys_ndmareq1		hw_wkdbg12	gpio1_wk8	safe_mode_wakeup15
CONTROL_WKUP_PAD0_FREF_CLK1_REQ_PAD1_SYS_NRESPWRON[31:16]	0x060	sys_nrespwron							
CONTROL_WKUP_PAD0_SYS_NRESWARM_PAD1_SYS_PWR_REQ [15:0]	0x064	sys_nreswarm							
CONTROL_WKUP_PAD0_SYS_NRESWARM_PAD1_SYS_PWR_REQ[31:16]	0x064	sys_pwr_req					hw_wkdbg15		safe_mode_wakeup16
CONTROL_WKUP_PAD0_SYS_NIRQ1_PAD1_SYS_NIRQ2[15:0]	0x068	sys_nirq1						gpio1_wk16	
CONTROL_WKUP_PAD0_SYS_NIRQ1_PAD1_SYS_NIRQ2[31:16]	0x068	sys_nirq2						gpio1_wk17	
CONTROL_WKUP_PAD0_SR_PMIC_SCL_PAD1_SR_PMIC_SDA[15:0]	0x06C	sr_pmic_scl							
CONTROL_WKUP_PAD0_SR_PMIC_SCL_PAD1_SR_PMIC_SDA[31:16]	0x06C	sr_pmic_sda							
CONTROL_WKUP_PAD0_SYS_BOOT0_PAD1_SYS_BOOT1[15:0]	0x070	sys_boot0			drm_emu2	drm_emu15	hw_wkdbg0	gpio1_wkout0	safe_mode_wakeup17
CONTROL_WKUP_PAD0_SYS_BOOT0_PAD1_SYS_BOOT1[31:16]	0x070	sys_boot1			drm_emu3	drm_emu16	hw_wkdbg1	gpio1_wkout1	safe_mode_wakeup18
CONTROL_WKUP_PAD0_SYS_BOOT2_PAD1_SYS_BOOT3 [15:0]	0x074	sys_boot2			drm_emu4	drm_emu17	hw_wkdbg2	gpio1_wkout2	safe_mode_wakeup19
CONTROL_WKUP_PAD0_SYS_BOOT2_PAD1_SYS_BOOT3[31:16]	0x074	sys_boot3			drm_emu5	drm_emu18	hw_wkdbg3	gpio1_wkout3	safe_mode_wakeup20

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Table A-13. Device Wake-Up Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_WKUP_PAD [Register name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_SYS_BOOT4_PAD1_SYS_BOOT5[15:0]	0x078	sys_boot4			drm_emu6	drm_emu19	hw_wkdbg4	gpio1_wkout4	safe_mode_wakeup21
CONTROL_WKUP_PAD0_SYS_BOOT4_PAD1_SYS_BOOT5[31:16]	0x078	sys_boot5	Reserved				hw_wkdbg8	gpio1_wkout5	safe_mode_wakeup22

Table A-14. Device Core Control Module Pad Configuration Register Fields

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_EMMC_CLK_PAD1_EMMC_CMD[15:0]	0x040	emmc_clk						gpio2_46	safe_mode_core0
CONTROL_CORE_PAD0_EMMC_CLK_PAD1_EMMC_CMD[31:16]	0x040	emmc_cmd						gpio2_47	safe_mode_core1
CONTROL_CORE_PAD0_EMMC_DATA0_PAD1_EMMC_DATA1[15:0]	0x044	emmc_data0						gpio2_48	safe_mode_core2
CONTROL_CORE_PAD0_EMMC_DATA0_PAD1_EMMC_DATA1[31:16]	0x044	emmc_data1						gpio2_49	safe_mode_core3
CONTROL_CORE_PAD0_EMMC_DATA2_PAD1_EMMC_DATA3[15:0]	0x048	emmc_data2						gpio2_50	safe_mode_core4
CONTROL_CORE_PAD0_EMMC_DATA2_PAD1_EMMC_DATA3[31:16]	0x048	emmc_data3						gpio2_51	safe_mode_core5
CONTROL_CORE_PAD0_EMMC_DATA4_PAD1_EMMC_DATA5[15:0]	0x04C	emmc_data4						gpio2_52	safe_mode_core6
CONTROL_CORE_PAD0_EMMC_DATA4_PAD1_EMMC_DATA5[31:16]	0x04C	emmc_data5						gpio2_53	safe_mode_core7
CONTROL_CORE_PAD0_EMMC_DATA6_PAD1_EMMC_DATA7[15:0]	0x050	emmc_data6						gpio2_54	safe_mode_core8
CONTROL_CORE_PAD0_EMMC_DATA6_PAD1_EMMC_DATA7[31:16]	0x050	emmc_data7						gpio2_55	safe_mode_core9

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_C2C_CLKOUT0_PAD1_C2C_CLKOUT1[15:0]	0x054	c2c_clkout0				gpmc_nadv_ale		gpio2_33	safe_mode_core20
CONTROL_CORE_PAD0_C2C_CLKOUT0_PAD1_C2C_CLKOUT1[31:16]	0x054	c2c_clkout1			kbd_col8	gpmc_nbe0_cle		gpio2_34	safe_mode_core21
CONTROL_CORE_PAD0_C2C_CLKIN0_PAD1_C2C_CLKIN1[15:0]	0x058	c2c_clkin0				gpmc_nwp	gpmc_nbe1	gpio2_35	safe_mode_core19
CONTROL_CORE_PAD0_C2C_CLKIN0_PAD1_C2C_CLKIN1[31:16]	0x058	c2c_clkin1			kbd_row8	gpmc_clk		gpio2_36	safe_mode_core18
CONTROL_CORE_PAD0_C2C_DATAIN0_PAD1_C2C_DATAIN1[15:0]	0x05C	c2c_datain0			kbd_row0	gpmc_ad0		gpio2_37	safe_mode_core10
CONTROL_CORE_PAD0_C2C_DATAIN0_PAD1_C2C_DATAIN1[31:16]	0x05C	c2c_datain1			kbd_row1	gpmc_ad1		gpio2_38	safe_mode_core11
CONTROL_CORE_PAD0_C2C_DATAIN2_PAD1_C2C_DATAIN3[15:0]	0x060	c2c_datain2			kbd_row2	gpmc_ad2		gpio2_39	safe_mode_core12
CONTROL_CORE_PAD0_C2C_DATAIN2_PAD1_C2C_DATAIN3[31:16]	0x060	c2c_datain3			kbd_row3	gpmc_ad3		gpio2_40	safe_mode_core13
CONTROL_CORE_PAD0_C2C_DATAIN4_PAD1_C2C_DATAIN5[15:0]	0x064	c2c_datain4			kbd_row4	gpmc_ad4		gpio2_41	safe_mode_core14
CONTROL_CORE_PAD0_C2C_DATAIN4_PAD1_C2C_DATAIN5[31:16]	0x064	c2c_datain5			kbd_row5	gpmc_ad5		gpio2_42	safe_mode_core15
CONTROL_CORE_PAD0_C2C_DATAIN6_PAD1_C2C_DATAIN7[15:0]	0x068	c2c_datain6			kbd_row6	gpmc_ad6		gpio2_43	safe_mode_core16
CONTROL_CORE_PAD0_C2C_DATAIN6_PAD1_C2C_DATAIN7[31:16]	0x068	c2c_datain7			kbd_row7	gpmc_ad7		gpio2_44	safe_mode_core17
CONTROL_CORE_PAD0_C2C_DATAOUT0_PAD1_C2C_DATAOUT1[15:0]	0x06C	c2c_dataout0			kbd_col0	gpmc_ad8	hw_dbg16	gpio2_56	safe_mode_core22
CONTROL_CORE_PAD0_C2C_DATAOUT0_PAD1_C2C_DATAOUT1[31:16]	0x06C	c2c_dataout1			kbd_col1	gpmc_ad9	hw_dbg17	gpio2_57	safe_mode_core23

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_C2C_DATAOUT2_PAD1_C2C_DATAOUT3[15:0]	0x070	c2c_dataout2			kbd_col2	gpmc_ad10	hw_dbg18	gpio2_58	safe_mode_core24
CONTROL_CORE_PAD0_C2C_DATAOUT2_PAD1_C2C_DATAOUT3[31:16]	0x070	c2c_dataout3			kbd_col3	gpmc_ad11	hw_dbg19	gpio2_59	safe_mode_core25
CONTROL_CORE_PAD0_C2C_DATAOUT4_PAD1_C2C_DATAOUT5 [15:0]	0x074	c2c_dataout4			kbd_col4	gpmc_ad12	hw_dbg20	gpio2_60	safe_mode_core26
CONTROL_CORE_PAD0_C2C_DATAOUT4_PAD1_C2C_DATAOUT5[31:16]	0x074	c2c_dataout5			kbd_col5	gpmc_ad13	hw_dbg21	gpio2_61	safe_mode_core27
CONTROL_CORE_PAD0_C2C_DATAOUT6_PAD1_C2C_DATAOUT7[15:0]	0x078	c2c_dataout6			kbd_col6	gpmc_ad14	hw_dbg22	gpio2_62	safe_mode_core28
CONTROL_CORE_PAD0_C2C_DATAOUT6_PAD1_C2C_DATAOUT7[31:16]	0x078	c2c_dataout7			kbd_col7	gpmc_ad15	hw_dbg23	gpio2_63	safe_mode_core29
CONTROL_CORE_PAD0_C2C_DATA8_PAD1_C2C_DATA9[15:0]	0x07C	c2c_data8				gpmc_a16	hw_dbg24	gpio4_113	safe_mode_core30
CONTROL_CORE_PAD0_C2C_DATA8_PAD1_C2C_DATA9[31:16]	0x07C	c2c_data9				gpmc_a17	hw_dbg25	gpio4_114	safe_mode_core31
CONTROL_CORE_PAD0_C2C_DATA10_PAD1_C2C_DATA11[15:0]	0x080	c2c_data10				gpmc_a18	hw_dbg26	gpio4_115	safe_mode_core32
CONTROL_CORE_PAD0_C2C_DATA10_PAD1_C2C_DATA11[31:16]	0x080	c2c_data11				gpmc_a19	hw_dbg27	gpio4_116	safe_mode_core33
CONTROL_CORE_PAD0_C2C_DATA12_PAD1_C2C_DATA13[15:0]	0x084	c2c_data12				gpmc_a20	hw_dbg28	gpio4_117	safe_mode_core34
CONTROL_CORE_PAD0_C2C_DATA12_PAD1_C2C_DATA13[31:16]	0x084	c2c_data13				gpmc_a21	hw_dbg29	gpio4_118	safe_mode_core35
CONTROL_CORE_PAD0_C2C_DATA14_PAD1_C2C_DATA15[15:0]	0x088	c2c_data14				gpmc_a22	hw_dbg30	gpio4_119	safe_mode_core36
CONTROL_CORE_PAD0_C2C_DATA14_PAD1_C2C_DATA15[31:16]	0x088	c2c_data15				gpmc_a23	hw_dbg31	gpio4_120	safe_mode_core37

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_LLIA_WAKEREQOUT_PAD1_LLIB_WAKEREQOUT[15:0]	0x08C	llia_wakereqout	c2c_wakereqout			gpmc_wait0		gpio2_45	safe_mode_core39
CONTROL_CORE_PAD0_LLIA_WAKEREQOUT_PAD1_LLIB_WAKEREQOUT[31:16]	0x08C	llib_wakereqout				gpmc_ncs0		gpio2_32	safe_mode_core38
CONTROL_CORE_PAD0_HSI1_ACREADY_PAD1_HSI1_CAREADY[15:0]	0x090	hsi1_acready	cam_strobe		usbb2_ulpitll_clk			gpio3_64	safe_mode_core40
CONTROL_CORE_PAD0_HSI1_ACREADY_PAD1_HSI1_CAREADY[31:16]	0x090	hsi1_caready			usbb2_ulpitll_nxt			gpio3_65	safe_mode_core41
CONTROL_CORE_PAD0_HSI1_ACWAKE_PAD1_HSI1_CAWAKE[15:0]	0x094	hsi1_acwake			usbb2_ulpitll_dir			gpio3_66	safe_mode_core42
CONTROL_CORE_PAD0_HSI1_ACWAKE_PAD1_HSI1_CAWAKE[31:16]	0x094	hsi1_cawake			usbb2_ulpitll_stp			gpio3_67	safe_mode_core43
CONTROL_CORE_PAD0_HSI1_ACFLAG_PAD1_HSI1_ACDATA[15:0]	0x098	hsi1_acflag			usbb2_ulpitll_data0			gpio3_68	safe_mode_core44
CONTROL_CORE_PAD0_HSI1_ACFLAG_PAD1_HSI1_ACDATA[31:16]	0x098	hsi1_acdata			usbb2_ulpitll_data1			gpio3_69	safe_mode_core45
CONTROL_CORE_PAD0_HSI1_CAFLAG_PAD1_HSI1_CADATA[15:0]	0x09C	hsi1_caflag			usbb2_ulpitll_data2			gpio3_70	safe_mode_core46
CONTROL_CORE_PAD0_HSI1_CAFLAG_PAD1_HSI1_CADATA[31:16]	0x09C	hsi1_cadata			usbb2_ulpitll_data3			gpio3_71	safe_mode_core47
CONTROL_CORE_PAD0_UART1_TX_PAD1_UART1_CTS[15:0]	0x0A0	uart1_tx			usbb2_ulpitll_data4			gpio3_72	safe_mode_core48
CONTROL_CORE_PAD0_UART1_TX_PAD1_UART1_CTS[31:16]	0x0A0	uart1_cts			usbb2_ulpitll_data5	gpmc_wait3		gpio3_73	safe_mode_core49
CONTROL_CORE_PAD0_UART1_RX_PAD1_UART1_RTS[15:0]	0x0A4	uart1_rx			usbb2_ulpitll_data6			gpio3_74	safe_mode_core50
CONTROL_CORE_PAD0_UART1_RX_PAD1_UART1_RTS[31:16]	0x0A4	uart1_rts			usbb2_ulpitll_data7	gpmc_ncs7		gpio3_75	safe_mode_core51

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_HSI2_CAREADY_PAD1_HSI2_ACREADY[15:0]	0x0A8	hsi2_caready			usbb1_ulpiphy_clk	gpmc_wait1		gpio3_76	safe_mode_core52
CONTROL_CORE_PAD0_HSI2_CAREADY_PAD1_HSI2_ACREADY[31:16]	0x0A8	hsi2_acready			usbb1_ulpiphy_nxt	gpmc_ncs1		gpio3_77	safe_mode_core53
CONTROL_CORE_PAD0_HSI2_CAWAKE_PAD1_HSI2_ACWAKE[15:0]	0x0AC	hsi2_cawake			usbb1_ulpiphy_dir	gpmc_a24		gpio3_78	safe_mode_core54
CONTROL_CORE_PAD0_HSI2_CAWAKE_PAD1_HSI2_ACWAKE[31:16]	0x0AC	hsi2_acwake			usbb1_ulpiphy_stp	gpmc_a25		gpio3_79	safe_mode_core55
CONTROL_CORE_PAD0_HSI2_CAFLAG_PAD1_HSI2_CADATA[15:0]	0x0B0	hsi2_caflag			usbb1_ulpiphy_data0	gpmc_wait2		gpio3_80	safe_mode_core56
CONTROL_CORE_PAD0_HSI2_CAFLAG_PAD1_HSI2_CADATA[31:16]	0x0B0	hsi2_cadata			usbb1_ulpiphy_data1	gpmc_ncs2		gpio3_81	safe_mode_core57
CONTROL_CORE_PAD0_HSI2_ACFLAG_PAD1_HSI2_ACDATA[15:0]	0x0B4	hsi2_acflag			usbb1_ulpiphy_data2	gpmc_ncs3		gpio3_82	safe_mode_core58
CONTROL_CORE_PAD0_HSI2_ACFLAG_PAD1_HSI2_ACDATA[31:16]	0x0B4	hsi2_acdata			usbb1_ulpiphy_data3	gpmc_ncs4		gpio3_83	safe_mode_core59
CONTROL_CORE_PAD0_UART2_RTS_PAD1_UART2_CTS[15:0]	0x0B8	uart2_rts	mcspi3_somi		usbb1_ulpiphy_data4	gpmc_nwe	hw_dbg16	gpio3_84	safe_mode_core60
CONTROL_CORE_PAD0_UART2_RTS_PAD1_UART2_CTS[31:16]	0x0B8	uart2_cts	mcspi3_cs0		usbb1_ulpiphy_data5	gpmc_noe_nre	hw_dbg17	gpio3_85	safe_mode_core61
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[15:0]	0x0BC	uart2_rx	mcspi3_simo		usbb1_ulpiphy_data6	gpmc_ncs5	hw_dbg18	gpio3_86	safe_mode_core62
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX[31:16]	0x0BC	uart2_tx	mcspi3_clk		usbb1_ulpiphy_data7	gpmc_ncs6	hw_dbg19	gpio3_87	safe_mode_core63
CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBB1_HSIC_DATA[15:0]	0x0C0	usbb1_hsic_strobe						gpio3_92	safe_mode_core64
CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBB1_HSIC_DATA[31:16]	0x0C0	usbb1_hsic_data						gpio3_93	safe_mode_core65

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_USBB2_HSIC_STROBE_PAD1_USBB2_HSIC_DATA[15:0]	0x0C4	usbb2_hsic_strobe						gpio3_94	safe_mode_core66
CONTROL_CORE_PAD0_USBB2_HSIC_STROBE_PAD1_USBB2_HSIC_DATA[31:16]	0x0C4	usbb2_hsic_data						gpio3_95	safe_mode_core67
CONTROL_CORE_PAD0_TIMER10_PWM_EVT_PAD1_DSIPORTA_TE0[15:0]	0x0C8	timer10_pwm_evt						gpio6_188	safe_mode_core68
CONTROL_CORE_PAD0_TIMER10_PWM_EVT_PAD1_DSIPORTA_TE0[31:16]	0x0C8	dsiporta_te0						gpio6_189	safe_mode_core69
CONTROL_CORE_PAD0_DSIPORTA_LANE0X_PAD1_DSIPORTA_LANE0Y[15:0]	0x0CC	dsiporta_lane0x							
CONTROL_CORE_PAD0_DSIPORTA_LANE0X_PAD1_DSIPORTA_LANE0Y[31:16]	0x0CC	dsiporta_lane0y							
CONTROL_CORE_PAD0_DSIPORTA_LANE1X_PAD1_DSIPORTA_LANE1Y[15:0]	0x0D0	dsiporta_lane1x							
CONTROL_CORE_PAD0_DSIPORTA_LANE1X_PAD1_DSIPORTA_LANE1Y[31:16]	0x0D0	dsiporta_lane1y							
CONTROL_CORE_PAD0_DSIPORTA_LANE2X_PAD1_DSIPORTA_LANE2Y[15:0]	0x0D4	dsiporta_lane2x							
CONTROL_CORE_PAD0_DSIPORTA_LANE2X_PAD1_DSIPORTA_LANE2Y[31:16]	0x0D4	dsiporta_lane2y							
CONTROL_CORE_PAD0_DSIPORTA_LANE3X_PAD1_DSIPORTA_LANE3Y[15:0]	0x0D8	dsiporta_lane3x							
CONTROL_CORE_PAD0_DSIPORTA_LANE3X_PAD1_DSIPORTA_LANE3Y[31:16]	0x0D8	dsiporta_lane3y							
CONTROL_CORE_PAD0_DSIPORTA_LANE4X_PAD1_DSIPORTA_LANE4Y[15:0]	0x0DC	dsiporta_lane4x							
CONTROL_CORE_PAD0_DSIPORTA_LANE4X_PAD1_DSIPORTA_LANE4Y[31:16]	0x0DC	dsiporta_lane4y							

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_DSIPORTC_LANE0X_PAD1_DSIPORTC_LANE0Y[15:0]	0x0E0	dsiportc_lane0x							
CONTROL_CORE_PAD0_DSIPORTC_LANE0X_PAD1_DSIPORTC_LANE0Y[31:16]	0x0E0	dsiportc_lane0y							
CONTROL_CORE_PAD0_DSIPORTC_LANE1X_PAD1_DSIPORTC_LANE1Y[15:0]	0x0E4	dsiportc_lane1x							
CONTROL_CORE_PAD0_DSIPORTC_LANE1X_PAD1_DSIPORTC_LANE1Y[31:16]	0x0E4	dsiportc_lane1y							
CONTROL_CORE_PAD0_DSIPORTC_LANE2X_PAD1_DSIPORTC_LANE2Y[15:0]	0x0E8	dsiportc_lane2x							
CONTROL_CORE_PAD0_DSIPORTC_LANE2X_PAD1_DSIPORTC_LANE2Y[31:16]	0x0E8	dsiportc_lane2y							
CONTROL_CORE_PAD0_DSIPORTC_LANE3X_PAD1_DSIPORTC_LANE3Y[15:0]	0x0EC	dsiportc_lane3x							
CONTROL_CORE_PAD0_DSIPORTC_LANE3X_PAD1_DSIPORTC_LANE3Y[31:16]	0x0EC	dsiportc_lane3y							
CONTROL_CORE_PAD0_DSIPORTC_LANE4X_PAD1_DSIPORTC_LANE4Y[15:0]	0x0F0	dsiportc_lane4x							
CONTROL_CORE_PAD0_DSIPORTC_LANE4X_PAD1_DSIPORTC_LANE4Y[31:16]	0x0F0	dsiportc_lane4y							
CONTROL_CORE_PAD0_DSIPORTC_TE0_PAD1_TIMER9_PWM_EVT[15:0]	0x0F4	dsiportc_te0						gpio6_191	safe_mode_core71
CONTROL_CORE_PAD0_DSIPORTC_TE0_PAD1_TIMER9_PWM_EVT[31:16]	0x0F4	timer9_pwm_evt	sync_sof_clk	sync_usof_itp_clk				gpio6_190	safe_mode_core70
CONTROL_CORE_PAD0_I2C4_SCL_PAD1_I2C4_SDA[15:0]	0x0F8	i2c4_scl	jtagtapext_tdi					gpio7_200	safe_mode_core104
CONTROL_CORE_PAD0_I2C4_SCL_PAD1_I2C4_SDA[31:16]	0x0F8	i2c4_sda	jtagtapext_rtck					gpio7_201	safe_mode_core105

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_MCSPI2_CLK_PAD1_MCSPI2_SIMO[15:0]	0x0FC	mcspi2_clk	jtagtapext_tck					gpio7_197	safe_mode_core101
CONTROL_CORE_PAD0_MCSPI2_CLK_PAD1_MCSPI2_SIMO[31:16]	0x0FC	mcspi2_simo	jtagtapext_tmsc				hw_dbg20	gpio7_198	safe_mode_core102
CONTROL_CORE_PAD0_MCSPI2_SOMI_PAD1_MCSPI2_CS0[15:0]	0x100	mcspi2_somi	jtagtapext_tdo				hw_dbg21	gpio7_199	safe_mode_core103
CONTROL_CORE_PAD0_MCSPI2_SOMI_PAD1_MCSPI2_CS0[31:16]	0x100	mcspi2_cs0	jtagtapext_ntrst		dispc_fid			gpio7_196	safe_mode_core100
CONTROL_CORE_PAD0_RFBI_DATA15_PAD1_RFBI_DATA14[15:0]	0x104	rfbi_data15	mcspi2_cs1		dispc_data15	kbd_col6	drm_emu19	gpio6_181	safe_mode_core83
CONTROL_CORE_PAD0_RFBI_DATA15_PAD1_RFBI_DATA14[31:16]	0x104	rfbi_data14			dispc_data14	kbd_col7	drm_emu18	gpio6_180	safe_mode_core82
CONTROL_CORE_PAD0_RFBI_DATA13_PAD1_RFBI_DATA12[15:0]	0x108	rfbi_data13			dispc_data13	kbd_col8	drm_emu17	gpio6_179	safe_mode_core81
CONTROL_CORE_PAD0_RFBI_DATA13_PAD1_RFBI_DATA12[31:16]	0x108	rfbi_data12			dispc_data12	kbd_row6	drm_emu16	gpio6_178	safe_mode_core80
CONTROL_CORE_PAD0_RFBI_DATA11_PAD1_RFBI_DATA10[15:0]	0x10C	rfbi_data11			dispc_data11	kbd_row7	drm_emu15	gpio6_177	safe_mode_core79
CONTROL_CORE_PAD0_RFBI_DATA11_PAD1_RFBI_DATA10[31:16]	0x10C	rfbi_data10			dispc_data10	kbd_row8	drm_emu14	gpio6_176	safe_mode_core78
CONTROL_CORE_PAD0_RFBI_DATA9_PAD1_RFBI_DATA8[15:0]	0x110	rfbi_data9			dispc_data9	kbd_row3	drm_emu13	gpio6_175	safe_mode_core77
CONTROL_CORE_PAD0_RFBI_DATA9_PAD1_RFBI_DATA8[31:16]	0x110	rfbi_data8			dispc_data8	kbd_col3	drm_emu12	gpio6_174	safe_mode_core76
CONTROL_CORE_PAD0_RFBI_DATA7_PAD1_RFBI_DATA6[15:0]	0x114	rfbi_data7			dispc_data7	jtagtapext_tdi	drm_emu11	gpio6_173	safe_mode_core97
CONTROL_CORE_PAD0_RFBI_DATA7_PAD1_RFBI_DATA6[31:16]	0x114	rfbi_data6			dispc_data6	jtagtapext_tdo	drm_emu10	gpio6_172	safe_mode_core96

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_RFBI_DATA5_PAD1_RFBI_DATA4[15:0]	0x118	rfbi_data5			dispc_data5	jtagtapext_tmsc	drm_emu9	gpio6_171	safe_mode_core95
CONTROL_CORE_PAD0_RFBI_DATA5_PAD1_RFBI_DATA4[31:16]	0x118	rfbi_data4			dispc_data4	jtagtapext_tck	drm_emu8	gpio6_170	safe_mode_core94
CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2[15:0]	0x11C	rfbi_data3			dispc_data3	jtagtapext_ntrst	drm_emu7	gpio6_169	safe_mode_core93
CONTROL_CORE_PAD0_RFBI_DATA3_PAD1_RFBI_DATA2[31:16]	0x11C	rfbi_data2			dispc_data2	uart3_tx_irtx	drm_emu6	gpio6_168	safe_mode_core92
CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[15:0]	0x120	rfbi_data1			dispc_data1	uart3_rx_irrx	drm_emu5	gpio6_167	safe_mode_core91
CONTROL_CORE_PAD0_RFBI_DATA1_PAD1_RFBI_DATA0[31:16]	0x120	rfbi_data0			dispc_data0	jtagtapext_rtck	drm_emu4	gpio6_166	safe_mode_core90
CONTROL_CORE_PAD0_RFBI_WE_PAD1_RFBI_CS0[15:0]	0x124	rfbi_we			dispc_vsync		drm_emu2	gpio6_162	safe_mode_core99
CONTROL_CORE_PAD0_RFBI_WE_PAD1_RFBI_CS0[31:16]	0x124	rfbi_cs0			dispc_hsync		drm_emu3	gpio6_163	safe_mode_core98
CONTROL_CORE_PAD0_RFBI_A0_PAD1_RFBI_RE[15:0]	0x128	rfbi_a0			dispc_de	kbd_row4		gpio6_165	safe_mode_core75
CONTROL_CORE_PAD0_RFBI_A0_PAD1_RFBI_RE[31:16]	0x128	rfbi_re			dispc_pclk	kbd_col4		gpio6_164	safe_mode_core74
CONTROL_CORE_PAD0_RFBI_HSYNC0_PAD1_RFBI_TE_VSYNC0[15:0]	0x12C	rfbi_hsync0			dispc_data17	kbd_col5		gpio6_160	safe_mode_core72
CONTROL_CORE_PAD0_RFBI_HSYNC0_PAD1_RFBI_TE_VSYNC0[31:16]	0x12C	rfbi_te_vsync0			dispc_data16	kbd_row5	jtag_sel	gpio6_161	safe_mode_core73
CONTROL_CORE_PAD0_GPIO6_182_PAD1_GPIO6_183[15:0]	0x130	gpio6_182			dispc_data18	kbd_col0		gpio6_182	safe_mode_core84
CONTROL_CORE_PAD0_GPIO6_182_PAD1_GPIO6_183[31:16]	0x130	gpio6_183			dispc_data19	kbd_col1		gpio6_183	safe_mode_core85

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_GPIO6_184_PAD1_GPIO6_185[15:0]	0x134	gpio6_184			dispc_data20	kbd_col2	hw_dbg22	gpio6_184	safe_mode_core86
CONTROL_CORE_PAD0_GPIO6_184_PAD1_GPIO6_185[31:16]	0x134	gpio6_185			dispc_data21	kbd_row0	hw_dbg23	gpio6_185	safe_mode_core87
CONTROL_CORE_PAD0_GPIO6_186_PAD1_GPIO6_187[15:0]	0x138	gpio6_186			dispc_data22	kbd_row1	hw_dbg24	gpio6_186	safe_mode_core88
CONTROL_CORE_PAD0_GPIO6_186_PAD1_GPIO6_187[31:16]	0x138	gpio6_187			dispc_data23	kbd_row2	hw_dbg25	gpio6_187	safe_mode_core89
CONTROL_CORE_PAD0_HDMI_CEC_PAD1_HDMI_HPD[15:0]	0x13C	hdmi_cec						gpio7_192	safe_mode_core106
CONTROL_CORE_PAD0_HDMI_CEC_PAD1_HDMI_HPD[31:16]	0x13C	hdmi_hpd						gpio7_193	safe_mode_core107
CONTROL_CORE_PAD0_HDMI_DDC_SCL_PAD1_HDMI_DDC_SDA[15:0]	0x140	hdmi_ddc_scl						gpio7_194	safe_mode_core108
CONTROL_CORE_PAD0_HDMI_DDC_SCL_PAD1_HDMI_DDC_SDA[31:16]	0x140	hdmi_ddc_sda						gpio7_195	safe_mode_core109
CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[15:0]	0x144	csiportc_lane0x			cpi_data9			gpio8_in253	safe_mode_core127
CONTROL_CORE_PAD0_CSIPORTC_LANE0X_PAD1_CSIPORTC_LANE0Y[31:16]	0x144	csiportc_lane0y			cpi_data8			gpio8_in252	safe_mode_core126
CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[15:0]	0x148	csiportc_lane1x			cpi_data11			gpio8_in255	safe_mode_core129
CONTROL_CORE_PAD0_CSIPORTC_LANE1X_PAD1_CSIPORTC_LANE1Y[31:16]	0x148	csiportc_lane1y			cpi_data10			gpio8_in254	safe_mode_core128
CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[15:0]	0x14C	csiportb_lane0x				cpi_data12		gpio8_in246	safe_mode_core120
CONTROL_CORE_PAD0_CSIPORTB_LANE0X_PAD1_CSIPORTB_LANE0Y[31:16]	0x14C	csiportb_lane0y				cpi_data13		gpio8_in247	safe_mode_core121

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[15:0]	0x150	csiportb_lane1x				cpi_data15		gpio8_in249	safe_mode_core123
CONTROL_CORE_PAD0_CSIPORTB_LANE1X_PAD1_CSIPORTB_LANE1Y[31:16]	0x150	csiportb_lane1y				cpi_data14		gpio8_in248	safe_mode_core122
CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[15:0]	0x154	csiportb_lane2x				cpi_vsyncin		gpio8_in251	safe_mode_core125
CONTROL_CORE_PAD0_CSIPORTB_LANE2X_PAD1_CSIPORTB_LANE2Y[31:16]	0x154	csiportb_lane2y				cpi_hsyncin		gpio8_in250	safe_mode_core124
CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[15:0]	0x158	csiporta_lane0x			cpi_pclk			gpio8_in236	safe_mode_core110
CONTROL_CORE_PAD0_CSIPORTA_LANE0X_PAD1_CSIPORTA_LANE0Y[31:16]	0x158	csiporta_lane0y			cpi_wen			gpio8_in237	safe_mode_core111
CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[15:0]	0x15C	csiporta_lane1x			cpi_data1			gpio8_in239	safe_mode_core113
CONTROL_CORE_PAD0_CSIPORTA_LANE1X_PAD1_CSIPORTA_LANE1Y[31:16]	0x15C	csiporta_lane1y			cpi_data0			gpio8_in238	safe_mode_core112
CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[15:0]	0x160	csiporta_lane2x			cpi_data3			gpio8_in241	safe_mode_core115
CONTROL_CORE_PAD0_CSIPORTA_LANE2X_PAD1_CSIPORTA_LANE2Y[31:16]	0x160	csiporta_lane2y			cpi_data2			gpio8_in240	safe_mode_core114
CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[15:0]	0x164	csiporta_lane3x			cpi_data4			gpio8_in242	safe_mode_core116
CONTROL_CORE_PAD0_CSIPORTA_LANE3X_PAD1_CSIPORTA_LANE3Y[31:16]	0x164	csiporta_lane3y			cpi_data5			gpio8_in243	safe_mode_core117
CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[15:0]	0x168	csiporta_lane4x			cpi_data6			gpio8_in244	safe_mode_core118
CONTROL_CORE_PAD0_CSIPORTA_LANE4X_PAD1_CSIPORTA_LANE4Y[31:16]	0x168	csiporta_lane4y			cpi_data7			gpio8_in245	safe_mode_core119

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE[15:0]	0x16C	cam_shutter					sys_nodeid0	gpio8_224	safe_mode_core130
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE[31:16]	0x16C	cam_strobe					sys_nodeid1	gpio8_225	safe_mode_core131
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_TIMER11_PWM_EVT[15:0]	0x170	cam_globalreset	cam_shutter		cpi_fid			gpio8_226	safe_mode_core132
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_TIMER11_PWM_EVT[31:16]	0x170	timer11_pwm_evt		uart1_tx	cpi_data12		hw_dbg26	gpio8_227	safe_mode_core133
CONTROL_CORE_PAD0_TIMER5_PWM_EVT_PAD1_TIMER6_PWM_EVT[15:0]	0x174	timer5_pwm_evt	sdcard_cd	uart1_cts	cpi_data13			gpio8_228	safe_mode_core134
CONTROL_CORE_PAD0_TIMER5_PWM_EVT_PAD1_TIMER6_PWM_EVT[31:16]	0x174	timer6_pwm_evt	sdcard_wp	uart1_rx	cpi_data14			gpio8_229	safe_mode_core135
CONTROL_CORE_PAD0_TIMER8_PWM_EVT_PAD1_I2C3_SCL[15:0]	0x178	timer8_pwm_evt	sdcard_wp	uart1_rts	cpi_data15		hw_dbg27	gpio8_230	safe_mode_core136
CONTROL_CORE_PAD0_TIMER8_PWM_EVT_PAD1_I2C3_SCL[31:16]	0x178	i2c3_scl						gpio8_231	safe_mode_core137
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_GPIO8_233[15:0]	0x17C	i2c3_sda						gpio8_232	safe_mode_core138
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_GPIO8_233[31:16]	0x17C	gpio8_233	Reserved	timer8_pwm_evt	cpi_hsync			gpio8_233	safe_mode_core139
CONTROL_CORE_PAD0_GPIO8_234_PAD1_ABE_CLKS[15:0]	0x180	gpio8_234	Reserved		cpi_vsync			gpio8_234	safe_mode_core140
CONTROL_CORE_PAD0_GPIO8_234_PAD1_ABE_CLKS[31:16]	0x180	abe_clks			abemcasp_axr			gpio4_96	safe_mode_core141
CONTROL_CORE_PAD0_ABEDMIC_DIN1_PAD1_ABEDMIC_DIN2[15:0]	0x184	abedmic_din1			abemcasp_ahclkr	abemcbsp3_fsx		gpio4_97	safe_mode_core142
CONTROL_CORE_PAD0_ABEDMIC_DIN1_PAD1_ABEDMIC_DIN2[31:16]	0x184	abedmic_din2			abemcasp_axr	abemcbsp3_dx		gpio4_98	safe_mode_core143

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_ABEDMIC_DIN3_PAD1_ABEDMIC_CLK1[15:0]	0x188	abedmic_din3				abemcbsp3_dr		gpio4_99	safe_mode_core144
CONTROL_CORE_PAD0_ABEDMIC_DIN3_PAD1_ABEDMIC_CLK1[31:16]	0x188	abedmic_clk1				abemcbsp3_clkx		gpio4_100	safe_mode_core145
CONTROL_CORE_PAD0_ABEDMIC_CLK2_PAD1_ABEDMIC_CLK3[15:0]	0x18C	abedmic_clk2	abemcbsp1_fsx		abemcasp_amutein			gpio4_101	safe_mode_core146
CONTROL_CORE_PAD0_ABEDMIC_CLK2_PAD1_ABEDMIC_CLK3[31:16]	0x18C	abedmic_clk3	abemcbsp1_dx		abemcasp_aclkx			gpio4_102	safe_mode_core147
CONTROL_CORE_PAD0_ABESLIMBUS1_CLOCK_PAD1_ABESLIMBUS1_DATA[15:0]	0x190	abeslimbus1_clock	abemcbsp1_clkx		abemcasp_afsr			gpio4_103	safe_mode_core148
CONTROL_CORE_PAD0_ABESLIMBUS1_CLOCK_PAD1_ABESLIMBUS1_DATA[31:16]	0x190	abeslimbus1_data	abemcbsp1_dr		abemcasp_aclkr			gpio4_104	safe_mode_core149
CONTROL_CORE_PAD0_ABEMCBSP2_DR_PAD1_ABEMCBSP2_DX[15:0]	0x194	abemcbsp2_dr			abemcasp_axr			gpio4_105	safe_mode_core150
CONTROL_CORE_PAD0_ABEMCBSP2_DR_PAD1_ABEMCBSP2_DX[31:16]	0x194	abemcbsp2_dx			abemcasp_amuteout			gpio4_106	safe_mode_core151
CONTROL_CORE_PAD0_ABEMCBSP2_FSX_PAD1_ABEMCBSP2_CLKX[15:0]	0x198	abemcbsp2_fsx			abemcasp_afsx			gpio4_107	safe_mode_core152
CONTROL_CORE_PAD0_ABEMCBSP2_FSX_PAD1_ABEMCBSP2_CLKX[31:16]	0x198	abemcbsp2_clkx			abemcasp_ahclkx			gpio4_108	safe_mode_core153
CONTROL_CORE_PAD0_ABEMCPDM_UL_DATA_PAD1_ABEMCPDM_DL_DATA[15:0]	0x19C	abemcpdm_ul_data	abemcbsp3_dr		abemcasp_axr3			gpio4_109	safe_mode_core154
CONTROL_CORE_PAD0_ABEMCPDM_UL_DATA_PAD1_ABEMCPDM_DL_DATA[31:16]	0x19C	abemcpdm_dl_data	abemcbsp3_dx		abemcasp_axr2			gpio4_110	safe_mode_core155

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_ABEMCPDM_FRAME_PAD1_ABEMCPDM_LB_CLK[15:0]	0x1A0	abemcpdm_frame	abemcbsp3_clkx		abemcasp_axr1			gpio4_111	safe_mode_core156
CONTROL_CORE_PAD0_ABEMCPDM_FRAME_PAD1_ABEMCPDM_LB_CLK[31:16]	0x1A0	abemcpdm_lb_clk	abemcbsp3_fsx					gpio4_112	safe_mode_core157
CONTROL_CORE_PAD0_WLSDIO_CLK_PAD1_WLSDIO_CMD[15:0]	0x1A4	wlsdio_clk	mcspi4_clk					gpio5_128	safe_mode_core158
CONTROL_CORE_PAD0_WLSDIO_CLK_PAD1_WLSDIO_CMD[31:16]	0x1A4	wlsdio_cmd						gpio5_129	safe_mode_core159
CONTROL_CORE_PAD0_WLSDIO_DATA0_PAD1_WLSDIO_DATA1[15:0]	0x1A8	wlsdio_data0	mcspi4_simo					gpio5_130	safe_mode_core160
CONTROL_CORE_PAD0_WLSDIO_DATA0_PAD1_WLSDIO_DATA1[31:16]	0x1A8	wlsdio_data1	mcspi4_somi					gpio5_131	safe_mode_core161
CONTROL_CORE_PAD0_WLSDIO_DATA2_PAD1_WLSDIO_DATA3[15:0]	0x1AC	wlsdio_data2	mcspi4_cs0					gpio5_132	safe_mode_core162
CONTROL_CORE_PAD0_WLSDIO_DATA2_PAD1_WLSDIO_DATA3[31:16]	0x1AC	wlsdio_data3						gpio5_133	safe_mode_core163
CONTROL_CORE_PAD0_UART5_RX_PAD1_UART5_TX[15:0]	0x1B0	uart5_rx				sdio4_data1	hw_dbg28	gpio5_134	safe_mode_core164
CONTROL_CORE_PAD0_UART5_RX_PAD1_UART5_TX[31:16]	0x1B0	uart5_tx				sdio4_data2	hw_dbg29	gpio5_135	safe_mode_core165
CONTROL_CORE_PAD0_UART5_CTS_PAD1_UART5_RTS[15:0]	0x1B4	uart5_cts				sdio4_data0	hw_dbg30	gpio5_136	safe_mode_core166
CONTROL_CORE_PAD0_UART5_CTS_PAD1_UART5_RTS[31:16]	0x1B4	uart5_rts				sdio4_data3	hw_dbg31	gpio5_137	safe_mode_core167
CONTROL_CORE_PAD0_I2C2_SCL_PAD1_I2C2_SDA[15:0]	0x1B8	i2c2_scl						gpio5_138	safe_mode_core168
CONTROL_CORE_PAD0_I2C2_SCL_PAD1_I2C2_SDA[31:16]	0x1B8	i2c2_sda						gpio5_139	safe_mode_core169

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_MCSPI1_CLK_PAD1_MCSPI1_SOMI[15:0]	0x1BC	mcspi1_clk					usbd0_ulpiphy_clk	gpio5_140	safe_mode_core170
CONTROL_CORE_PAD0_MCSPI1_CLK_PAD1_MCSPI1_SOMI[31:16]	0x1BC	mcspi1_somi					usbd0_ulpiphy_nxt	gpio5_141	safe_mode_core171
CONTROL_CORE_PAD0_MCSPI1_SIMO_PAD1_MCSPI1_CS0[15:0]	0x1C0	mcspi1_simo					usbd0_ulpiphy_dir	gpio5_142	safe_mode_core172
CONTROL_CORE_PAD0_MCSPI1_SIMO_PAD1_MCSPI1_CS0[31:16]	0x1C0	mcspi1_cs0					usbd0_ulpiphy_data0	gpio5_143	safe_mode_core173
CONTROL_CORE_PAD0_MCSPI1_CS1_PAD1_I2C5_SCL[15:0]	0x1C4	mcspi1_cs1					usbd0_ulpiphy_data1	gpio5_144	safe_mode_core174
CONTROL_CORE_PAD0_MCSPI1_CS1_PAD1_I2C5_SCL[31:16]	0x1C4	i2c5_scl		uart4_rx				gpio5_147	safe_mode_core175
CONTROL_CORE_PAD0_I2C5_SDA_PAD1_PERSLIMBUS2_CLOCK[15:0]	0x1C8	i2c5_sda		uart4_tx				gpio5_148	safe_mode_core176
CONTROL_CORE_PAD0_I2C5_SDA_PAD1_PERSLIMBUS2_CLOCK[31:16]	0x1C8	gpio5_145	mcspi1_cs2	uart4_cts	sdio5_clk		usbd0_ulpiphy_data2	gpio5_145	safe_mode_core177
CONTROL_CORE_PAD0_PERSLIMBUS2_DATA_PAD1_UART6_TX[15:0]	0x1CC	gpio5_146	mcspi1_cs3	uart4_rts	sdio5_cmd		usbd0_ulpiphy_data3	gpio5_146	safe_mode_core178
CONTROL_CORE_PAD0_PERSLIMBUS2_DATA_PAD1_UART6_TX[31:16]	0x1CC	uart6_tx			sdio5_data3	usbb2_mm_rxdp		gpio5_149	safe_mode_core179
CONTROL_CORE_PAD0_UART6_RX_PAD1_UART6_CTS[15:0]	0x1D0	uart6_rx			sdio5_data2	usbb2_mm_rxdm		gpio5_150	safe_mode_core180
CONTROL_CORE_PAD0_UART6_RX_PAD1_UART6_CTS[31:16]	0x1D0	uart6_cts	sys_ndmareq1		sdio5_data1	usbb2_mm_rxrcv		gpio5_151	safe_mode_core181
CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[15:0]	0x1D4	uart6_rts	sys_ndmareq0		sdio5_data0	usbb2_mm_txse0	usbd0_ulpiphy_stp	gpio5_152	safe_mode_core182
CONTROL_CORE_PAD0_UART6_RTS_PAD1_UART3_CTS_RCTX[31:16]	0x1D4	uart3_cts_rctx	sata_actled		sdio5_data7	usbb2_mm_txen	usbd0_ulpiphy_data4	gpio5_153	safe_mode_core183

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[15:0]	0x1D8	uart3_rts_irsd	hdq_sio		sdio5_data6	usbb2_mm_txdat	usbd0_ulpiphy_data5	gpio5_154	safe_mode_core184
CONTROL_CORE_PAD0_UART3_RTS_IRSD_PAD1_UART3_TX_IRTX[31:16]	0x1D8	uart3_tx_irtx			sdio5_data5	sdio4_clk	usbd0_ulpiphy_data6	gpio5_155	safe_mode_core185
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[15:0]	0x1DC	uart3_rx_irrx			sdio5_data4	sdio4_cmd	usbd0_ulpiphy_data7	gpio5_156	safe_mode_core186
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_USBB3_HSIC_STROBE[31:16]	0x1DC	usbb3_hsic_strobe						gpio5_158	safe_mode_core187
CONTROL_CORE_PAD0_USBB3_HSIC_DATA_PAD1_SDCARD_CLK[15:0]	0x1E0	usbb3_hsic_data						gpio5_159	safe_mode_core188
CONTROL_CORE_PAD0_USBB3_HSIC_DATA_PAD1_SDCARD_CLK[31:16]	0x1E0	sdcard_clk			jtag_rtck		n_clk		safe_mode_core189
CONTROL_CORE_PAD0_SDCARD_CMD_PAD1_SDCARD_DATA2[15:0]	0x1E4	sdcard_cmd			jtag_tdo	uart6_rx		n_d2	safe_mode_core190
CONTROL_CORE_PAD0_SDCARD_CMD_PAD1_SDCARD_DATA2[31:16]	0x1E4	sdcard_data2			jtag_tmsc		n_d2		safe_mode_core193
CONTROL_CORE_PAD0_SDCARD_DATA3_PAD1_SDCARD_DATA0[15:0]	0x1E8	sdcard_data3			jtag_tck		n_d3		safe_mode_core194
CONTROL_CORE_PAD0_SDCARD_DATA3_PAD1_SDCARD_DATA0[31:16]	0x1E8	sdcard_data0			jtag_tdi		n_d0		safe_mode_core191
CONTROL_CORE_PAD0_SDCARD_DATA1_PAD1_USBD0_HS_DP[15:0]	0x1EC	sdcard_data1			jtag_ntrst		n_d1		safe_mode_core192
CONTROL_CORE_PAD0_SDCARD_DATA1_PAD1_USBD0_HS_DP[31:16]	0x1EC	usbd0_hs_dp				uart3_rx_irrx			safe_mode_core195
CONTROL_CORE_PAD0_USBD0_HS_DM_PAD1_I2C1_PMIC_SCL[15:0]	0x1F0	usbd0_hs_dm				uart3_tx_irtx			safe_mode_core196
CONTROL_CORE_PAD0_USBD0_HS_DM_PAD1_I2C1_PMIC_SCL[31:16]	0x1F0	i2c1_pmic_scl							

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Table A-14. Device Core Control Module Pad Configuration Register Fields (continued)

CTRL_MODULE_CORE_PAD [Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_I2C1_PMIC_SDA_PAD1_USBD0_SS_RX[15:0]	0x1F4	i2c1_pmic_sda							
CONTROL_CORE_PAD0_I2C1_PMIC_SDA_PAD1_USBD0_SS_RX[31:16]	0x1F4	usbd0_ss_rx							

A.7.3 CTRL_MODULE_WKUP Registers

To select a default read latency of 8 for DDR3 in OMAP5432, the CONTROL_PROT_EMIF1_SDRAM_CONFIG[13:10] EMIF1_SDRAM_CL and CONTROL_PROT_EMIF2_SDRAM_CONFIG[13:10] EMIF2_SDRAM_CL bits have a reset value of 0x8.

A.7.4 SCM Use Guidelines

- All PADCONF bit fields, which appear in orange in Table A-13 and Table A-14, must be left in mux7, safe mode.

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A.8 Serial Communication Intrefaces

A.8.1 UART/IrDA/CIR

The OMAP5432 device has the following restrictions to UART controllers:

- UART6 is not available for use
- UART4 has a 2-pin (TX/RX) interface. Flow-control pins (CTS/RTS) are not available.

Table A-15 lists UART modules signals. Highlighted signals are not mapped on any pad in OMAP5432 device.

Table A-15. UART I/O Description

Signal	I/O[1]	Description	Reset
uart1_rx	I	Serial data input	HiZ
uart1_tx	O	Serial data output	1
uart1_cts	I	Clear to send	HiZ
uart1_rts	O	Request to send	1
uart2_rx	I	Serial data input	HiZ
uart2_tx	O	Serial data output	1
uart2_cts	I	Clear to send	HiZ
uart2_rts	O	Request to send	1
uart3_rx_irrx	I	Serial data input, IR and remote RX	HiZ
uart3_tx_irtx	O	Serial data output, IR TX	1
uart3_cts_rctx	I/O	Clear to send (input), remote TX (output)	1
uart3_rts_irsd	O	Request to send, IR enable	1
uart4_rx	I	Serial data input	HiZ
uart4_tx	O	Serial data output	1
uart4_cts	I	Clear to send	HiZ
uart4_rts	O	Request to send	1
uart5_rx	I	Serial data input	HiZ
uart5_tx	O	Serial data output	1
uart5_cts	I	Clear to send	HiZ
uart5_rts	O	Request to send	1
uart6_rx	I	Serial data input	HiZ
uart6_tx	O	Serial data output	1
uart6_cts	I	Clear to send	HiZ
uart6_rts	O	Request to send	1

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)

Table A-16 lists the base address and address space for the UART/IrDA/CIR module instances in the OMAP5432 device.

NOTE: Orange highlighting in Table A-16 indicates modules with removed functionality in the OMAP5432 device. The modules are still present on the die; therefore, their mappings are provided to control their activity and for debug purposes.

Table A-16. UART/IrDA/CIR Instance Summary

Module Name	Base Address	Size
UART1[1]	0x4806 A000	4 KiB
UART2[1]	0x4806 C000	4 KiB

(1) UART mode only

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Table A-16. UART/IrDA/CIR Instance Summary (continued)

Module Name	Base Address	Size
UART3[2]	0x4802 0000	4 KiB
UART4[1]	0x4806 E000	4 KiB
UART5[1]	0x4806 6000	4 KiB
UART6[1]	0x4806 8000	4 KiB

(2) UART, IrDA, or CIR mode

A.8.1.1 UART/IrDA/CIR Use Guidelines

For the unsupported UART1 and UART6 module, the following guidelines must be followed:

- Keep SYSC_REG[4:3] IDLEMODE = 0x0.
- Keep SYSC_REG[2] ENWAKEUP = 0x0.
- Set SYSC_REG[0] AUTOIDLE = 0x1.
- Keep all interrupts masked.

A.8.2 Multichannel SPI

The OMAP5432 device has the following limitations to MCSPI controllers:

- MCSPI1 chip-selects 2 and 3 (mcspi1_cs2 and mcspi1_cs3) are not available for use.

Table A-17 shows MCSPI signals. Signals that are not mapped to any pads on the OMAP5432 device are highlighted.

Table A-17. McSPI I/O Description

Signal Name	I/O	Description	Reset
mcspi1_clk	I/O[1]	SPI1 module serial clock[2]	HiZ[3]
mcspi1_simo	I/O[1]	SPI1 module serial data (slave input, master output)	HiZ
mcspi1_somi	I/O[1]	SPI1 module serial data (slave output, master input)	HiZ
mcspi1_cs0	O	SPI1 module chip-select 0	HiZ
mcspi1_cs1	O	SPI1 module chip-select 1	0
mcspi1_cs2	O	SPI1 module chip-select 2	0
mcspi1_cs3	O	SPI1 module chip-select 3	0
mcspi2_clk	I/O[1]	SPI2 module serial clock[2]	HiZ
mcspi2_simo	I/O[1]	SPI2 module serial data (slave input, master output)	HiZ
mcspi2_somi	I/O[1]	SPI2 module serial data (slave output, master input)	HiZ
mcspi2_cs0	O	SPI2 module chip-select 0	HiZ
mcspi2_cs1	O	SPI2 module chip-select 1	0
mcspi3_clk	I/O[1]	SPI3 module serial clock[2]	HiZ
mcspi3_simo	I/O[1]	SPI3 module serial data (slave input, master output)	HiZ
mcspi3_somi	I/O[1]	SPI3 module serial data (slave output, master input)	HiZ
mcspi3_cs0	I/O[1]	SPI3 module chip-select 0	HiZ
mcspi4_clk	I/O[1]	SPI4 module serial clock[2]	HiZ

(1) Depends on mode selection - master or slave SPI.
(2) This output signal is also used as retiming input (the CONTROL_PADCONF_x.INPUTENABLE bit must be set to 1).
(3) HiZ = High impedance

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Table A-17. McSPI I/O Description (continued)

Signal Name	I/O	Description	Reset
mcspi4_simo	I/O[1]	SPI4 module serial data (slave input, master output)	HiZ
mcspi4_somi	I/O[1]	SPI4 module serial data (slave output, master input)	HiZ
mcspi4_cs0	I/O[1]	SPI4 module chip-select 0	HiZ

A.8.3 MIPI HSI

The OMAP5432 device has the following restrictions to HSI controller:

- HSI port 1 is not available for use.

Table A-18 describes the HSI module I/O signals. The unavailable pins are highlighted with orange.

Table A-18. HSI I/O Signals

Pin Name	I/O[1]	Description	Reset Value[2]
hsi1_cawake	I	HSI port 1 wake-up signal from an external serial transmitter	HiZ
hsi1_cadata	I	HSI port 1 receiver data from an external transmitter	HiZ
hsi1_caflag	I	HSI port 1 receiver flag from an external transmitter	HiZ
hsi1_acready	O	HSI port 1 synchronization signal to an external transmitter	1
hsi1_acwake	O	HSI port 1 wake-up signal to an external serial receiver	0
hsi1_acdata	O	HSI port 1 transmission data (level transmission signaling) to an external receiver	0
hsi1_acflag	O	HSI port 1 transmission flag (bit transition signaling) to an external receiver	1
hsi1_caready	I	HSI port 1 synchronization signal from an external receiver	HiZ
hsi2_cawake	I	HSI port 2 wake-up signal from an external serial transmitter	HiZ
hsi2_cadata	I	HSI port 2 receiver data from an external transmitter	HiZ
hsi2_caflag	I	HSI port 2 receiver flag from an external transmitter	HiZ
hsi2_acready	O	HSI port 2 synchronization signal to an external transmitter	1
hsi2_acwake	O	HSI port 2 wake-up signal to an external serial receiver	0
hsi2_acdata	O	HSI port 2 transmission data (level transmission signaling) to an external receiver	0
hsi2_acflag	O	HSI port 2 transmission flag (bit transition signaling) to an external receiver	1
hsi2_caready	I	HSI port 2 synchronization signal from an external receiver	HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

A.8.4 High-Speed USB Host Subsystem

The HS USB host subsystem has the following limitations in the OMAP5432 device:

- The HS ULPI TLL interface is not supported.
- The serial TLL interface is limited to 2-/3-pin modes.
- The HSIC1 interface is not supported.

Table A-19 describes the I/O pins of the USB ports using the 12-pin/8-bit data SDR version of the ULPI mode.

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Table A-19. ULPI – 12-Pin/8-Bit Data SDR Version I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
HS USB Host Controller Port 1 (Device port USBB1)				
CLK	usbb1_ulpiphy_clk	I	Clock input from remote PHY IC	HiZ
DIR	usbb1_ulpiphy_dir	I	Data direction control from remote PHY IC	HiZ
STP	usbb1_ulpiphy_stp	O	Stop signal to remote PHY IC	1
NXT	usbb1_ulpiphy_nxt	I	Next signal from remote PHY IC	HiZ
DAT0	usbb1_ulpiphy_dat0	I/O	Bidirectional 8-bit data bus	HiZ
DAT1	usbb1_ulpiphy_dat1	I/O	Bidirectional 8-bit data bus	HiZ
DAT2	usbb1_ulpiphy_dat2	I/O	Bidirectional 8-bit data bus	HiZ
DAT3	usbb1_ulpiphy_dat3	I/O	Bidirectional 8-bit data bus	HiZ
DAT4	usbb1_ulpiphy_dat4	I/O	Bidirectional 8-bit data bus	HiZ
DAT5	usbb1_ulpiphy_dat5	I/O	Bidirectional 8-bit data bus	HiZ
DAT6	usbb1_ulpiphy_dat6	I/O	Bidirectional 8-bit data bus	HiZ
DAT7	usbb1_ulpiphy_dat7	I/O	Bidirectional 8-bit data bus	HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

Table A-20 describes the I/O pins of the USB ports using the 12-pin/8-bit data SDR version of the ULPI TLL interface mode. None of the pins are available in OMAP5432 device.

Table A-20. ULPI TLL Interface – 12-Pin/8-Bit Data SDR Version I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
HS USB Host Controller Port 2 (Device port USBB2)				
CLK	usbb2_ulpitll_clk	O	Clock output to remote ULPI link controller	0
DIR	usbb2_ulpitll_dir	O	Data direction control from remote ULPI link controller	0
STP	usbb2_ulpitll_stp	I	Stop signal to remote ULPI link controller	HiZ
NXT	usbb2_ulpitll_nxt	O	Next signal from remote ULPI link controller	0
DAT0	usbb2_ulpitll_dat0	I/O	Bidirectional 8-bit data bus	0
DAT1	usbb2_ulpitll_dat1	I/O	Bidirectional 8-bit data bus	0
DAT2	usbb2_ulpitll_dat2	I/O	Bidirectional 8-bit data bus	0
DAT3	usbb2_ulpitll_dat3	I/O	Bidirectional 8-bit data bus	0
DAT4	usbb2_ulpitll_dat4	I/O	Bidirectional 8-bit data bus	0
DAT5	usbb2_ulpitll_dat5	I/O	Bidirectional 8-bit data bus	0
DAT6	usbb2_ulpitll_dat6	I/O	Bidirectional 8-bit data bus	0
DAT7	usbb2_ulpitll_dat7	I/O	Bidirectional 8-bit data bus	0

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

Table A-21 describes the I/O of the HS USB host subsystem serial interface. The highlighted rows indicate the unavailable pins. The highlighted cells in description indicate the unavailable modes of that pin.

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Table A-21. Multiple-Mode FS/LS Serial Interface I/O Description

Device Signal Name	I/O[1]	Description	Value at Reset[2]
HS USB Host Controller Port 2 (Device port USBB2)			
usbb2_mm_txse0	I/O	SE0 function in 3-pin bidirectional DAT/SE0 mode	0
	I/O	DM function in 4-pin bidirectional DP/DM mode	
	O	SE0 output in 6-pin unidirectional DAT/SE0 mode	
	O	DM output in 6-pin unidirectional DP/DM mode	
	I/O	SE0-TLL in 2-/3-pin bidirectional DAT/SE0 TLL mode	
	I/O	DM-TLL in 2-/4-pin bidirectional DP/DM TLL mode	
	I	SE0-TLL input in 6-pin unidirectional DAT/SE0 TLL mode	
	I	DM-TLL input in 6-pin unidirectional DP/DM TLL mode	
usbb2_mm_txdat	I/O	DAT function in 3-pin bidirectional DAT/SE0 mode	HiZ
	I/O	DP function in 4-pin bidirectional DP/DM mode	
	O	DAT output in 6-pin unidirectional DAT/SE0 mode	
	O	DP output in 6-pin unidirectional DAT/SE0 mode	
	I/O	DAT-TLL in 2-/3-pin bidirectional DAT/SE0 TLL mode	
	I/O	DP-TLL in 2-/4-pin bidirectional DP/DM TLL mode	
	I	DAT-TLL input in 6-pin unidirectional DAT/SE0 TLL mode	
	I	DP-TLL input in 6-pin unidirectional DP/DM TLL mode	
usbb2_mm_txen	O	Transmit enable in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM or 6-pin unidirectional modes	1
	I	Transmit enable in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 6-pin unidirectional TLL modes (not used in 2-pin bidirectional TLL modes)	
usbb2_mm_rxrcv	I	Differential receiver signal input in 4-pin bidirectional DP/DM or 6-pin unidirectional modes (not used in 3-pin bidirectional DAT/SE0 mode)	HiZ
	O	Differential receiver signal output in the 4-pin bidirectional DP/DM TLL or 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 2-pin bidirectional TLL modes)	
usbb2_mm_rxdp	I	Single-ended DP receiver signal input in 6-pin unidirectional modes (not used in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM modes)	HiZ
	O	Single-ended DP receiver signal output in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 2-pin bidirectional TLL modes)	
usbb2_mm_rxdm	I	Single-ended DM receiver signal input in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 or 4-pin bidirectional DP/DM or 2-pin bidirectional TLL modes)	HiZ
	O	Single-ended DM receiver signal output in 6-pin unidirectional TLL modes (not used in 3-pin bidirectional DAT/SE0 TLL or 4-pin bidirectional DP/DM TLL or 2-pin bidirectional TLL modes)	

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

Table A-22 describes the I/O of the HSIC interface of the HS USB host subsystem. The unsupported pins by HSIC modules in OMAP5432 are highlighted in orange.

Table A-22. HSIC Interface I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
HS USB Host Controller Port 1 (Device port USBB1)				
DATA	usbb1_hsic_data	I/O	HSIC1 module data signal	HiZ
STROBE	usbb1_hsic_strobe	I/O	HSIC1 module strobe signal	HiZ
HS USB Host Controller Port 2 (Device port USBB2)				
DATA	usbb2_hsic_data	I/O	HSIC2 module data signal	HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

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Table A-22. HSIC Interface I/O Description (continued)

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
STROBE	usbb2_hsic_strobe	I/O	HSIC2 module strobe signal	HiZ
HS USB Host Controller Port 3 (Device port USBB3)				
DATA	usbb3_hsic_data	I/O	HSIC3 module data signal	HiZ
STROBE	usbb3_hsic_strobe	I/O	HSIC3 module strobe signal	HiZ

A.8.5 SuperSpeed USB OTG Subsystem

The OMAP5432 device has the following restrictions to USB OTG subsystem:

- The alternative to internal USB2.0 PHY, ULPI PHY interface is not available for use.

Table A-23 describes the I/O signals of the SuperSpeed USB subsystem interfaces. The unavailable pins are shown in orange.

Table A-23. Input/Output Description

Module Pin	Device-Level Signal Name	I/O[1]	Description	Reset Value[2]
ULPI interface				
CLK	usbd0_ulpiphy_clk	I	Clock input from external transceiver	HiZ
DIR	usbd0_ulpiphy_dir	I	Data direction control from external transceiver	HiZ
STP	usbd0_ulpiphy_stp	O	Output to external transceiver to stop data stream	1
NXT	usbd0_ulpiphy_nxt	I	Next signal control from external transceiver	HiZ
DATA0	usbd0_ulpiphy_data0	I/O	Data bit 0 to/from external transceiver	HiZ
DATA1	usbd0_ulpiphy_data1	I/O	Data bit 1 to/from external transceiver	HiZ
DATA2	usbd0_ulpiphy_data2	I/O	Data bit 2 to/from external transceiver	HiZ
DATA3	usbd0_ulpiphy_data3	I/O	Data bit 3 to/from external transceiver	HiZ
DATA4	usbd0_ulpiphy_data4	I/O	Data bit 4 to/from external transceiver	HiZ
DATA5	usbd0_ulpiphy_data5	I/O	Data bit 5 to/from external transceiver	HiZ
DATA6	usbd0_ulpiphy_data6	I/O	Data bit 6 to/from external transceiver	HiZ
DATA7	usbd0_ulpiphy_data7	I/O	Data bit 7 to/from external transceiver	HiZ
USB2PHY				
CE	usbphy_ce	O	Charging enable signal	0
DP	usbd0_hs_dp	I/O	USB2 half-duplex differential pair	HiZ
DM	usbd0_hs_dm	I/O		HiZ
USB3PHY				
TX	usbd0_ss_tx	O	USB3 transmitter differential pair	HiZ
TY	usbd0_ss_ty	O		HiZ
RX	usbd0_ss_rx	I	USB3 receiver differential pair	HiZ
RY	usbd0_ss_ry	I		HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

A.9 MMC/SD/SDIO

The OMAP5432 device has the following restrictions to MMC/SD/SDIO controllers:

- MMC/SD/SDIO controller 5 is not available for use.

Table A-24 describes MMC/SD/SDIO1 signals.

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Table A-24. MMC/SD/SDIO1 I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
CLK	sdcard_clk	O	Clock	0
CMD	sdcard_cmd	I/O	Command	HiZ
DATA0	sdcard_data0	I/O	Data bus	HiZ
DATA1	sdcard_data1	I/O	Data bus	HiZ
DATA2	sdcard_data2	I/O	Data bus	HiZ
DATA3	sdcard_data3	I/O	Data bus	HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

Table A-25 describes MMC/SD/SDIO2 signals.

Table A-25. MMC/SD/SDIO2 I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
CLK	emmc_clk	O	Clock	0
CMD	emmc_cmd	I/O	Command	HiZ
DATA0	emmc_data0	I/O	Data bus	HiZ
DATA1	emmc_data1	I/O	Data bus	HiZ
DATA2	emmc_data2	I/O	Data bus	HiZ
DATA3	emmc_data3	I/O	Data bus	HiZ
DATA4	emmc_data4	I/O	Data bus	HiZ
DATA5	emmc_data5	I/O	Data bus	HiZ
DATA6	emmc_data6	I/O	Data bus	HiZ
DATA7	emmc_data7	I/O	Data bus	HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

Table A-26 describes MMC/SD/SDIO3 signals.

Table A-26. MMC/SD/SDIO3 I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
CLK	wlsdio_clk	O	Clock	0
CMD	wlsdio_cmd	I/O	Command	HiZ
DATA0	wlsdio_data0	I/O	Data bus	HiZ
DATA1	wlsdio_data1	I/O	Data bus	HiZ
DATA2	wlsdio_data2	I/O	Data bus	HiZ
DATA3	wlsdio_data3	I/O	Data bus	HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

Table A-27 describes MMC/SD/SDIO4 signals.

Table A-27. MMC/SD/SDIO4 I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
CLK	sdio4_clk	O	Clock	0
CMD	sdio4_cmd	I/O	Command	HiZ
DATA0	sdio4_data0	I/O	Data bus	HiZ
DATA1	sdio4_data1	I/O	Data bus	HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

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Table A-27. MMC/SD/SDIO4 I/O Description (continued)

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
DATA2	sdio4_data2	I/O	Data bus	HiZ
DATA3	sdio4_data3	I/O	Data bus	HiZ

Table A-28 describes MMC/SD/SDIO5 signals. The signals that are not supported in OMAP5432 are highlighted with orange.

Table A-28. MMC/SD/SDIO5 I/O Description

Signal	Device Signal Name	I/O[1]	Description	Reset Value[2]
CLK	sdio5_clk	O	Clock	0
CMD	sdio5_cmd	I/O	Command	HiZ
DATA0	sdio5_data0	I/O	Data bus	HiZ
DATA1	sdio5_data1	I/O	Data bus	HiZ
DATA2	sdio5_data2	I/O	Data bus	HiZ
DATA3	sdio5_data3	I/O	Data bus	HiZ
DATA4	sdio5_data4	I/O	Data bus	HiZ
DATA5	sdio5_data5	I/O	Data bus	HiZ
DATA6	sdio5_data6	I/O	Data bus	HiZ
DATA7	sdio5_data7	I/O	Data bus	HiZ

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)
(2) HiZ = High impedance

Table A-29 describes MMC/SD/SDIO instance summary. The modules that are not supported in OMAP5432 are highlighted with orange.

Table A-29. MMC/SD/SDIO Instance Summary

Module Name	Base Address	Size
MMC1	0x4809 C000	4 KiB
MMC2	0x480B 4000	4 KiB
MMC3	0x480A D000	4 KiB
MMC4	0x480D 1000	4 KiB
MMC5	0x480D 5000	4 KiB

A.10 General-Purpose Interface

Table A-30 describes the GPIO channels.

Table A-30. GPIO Channels Description

Channel Number	Type [1]	Mapping	Wake-Up Feature	Comments
GPIO1 Module				
[5:0]	O	gpio1_wkout[5:0]	Yes	Wake-up path
[7:6]	I/O	gpio1_wk[7:6]	Yes	Wake-up path
[10:8]	I/O	gpio1_wk[10:8]	Yes	Wake-up path
[31:11]	I/O	gpio1_wk[31:11]	Yes	Wake-up path

(1) I = Input; O = Output; I/O = Input/Output (bidirectional)

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Table A-30. GPIO Channels Description (continued)

Channel Number	Type [1]	Mapping	Wake-Up Feature	Comments
GPIO2 Module				
[31:0]	I/O	gpio2_[63:32]	Yes [2]	GPIO
GPIO3 Module				
[11:0]	I/O	gpio3_[75:64]	Yes [2]	GPIO
[21:12]	I/O	gpio3_[85:76]	Yes [2]	GPIO
[22][3]	I/O	gpio3_86 thermal shutdown comparator output signal (TSHUT)	Yes [2]	GPIO
	I		Yes [2]	Bandgap internal TSHUT
[27:23]	I/O	gpio3_[91:87]	Yes [2]	GPIO
[29:28]	I/O	gpio3_[93:92]	Yes [2]	GPIO
[31:30]	I/O	gpio3_[95:94]	Yes [2]	GPIO
GPIO4 Module				
[31:0]	I/O	gpio4_[127:96]	Yes [2]	GPIO
GPIO5 Module				
[16:0]	I/O	gpio5_[144:128]	Yes [2]	GPIO
[18:17]	I/O	gpio5_[146:145]	Yes [2]	GPIO
[20:19]	I/O	gpio5_[148:147]	Yes [2]	GPIO
[23:21]	I/O	gpio5_[151:149]	Yes [2]	GPIO
[29][3]	I	gpio5_in157	Yes [2]	GPIO (input only)
	I	CHGDETECT	Yes [2]	USB charge detect
[31:30]	I/O	gpio5_[159:158]	Yes [2]	GPIO
GPIO6 Module				
[31:0]	I/O	gpio6_[191:160]	Yes [2]	GPIO
GPIO7 Module				
[31:0]	I/O	gpio7_[223:192]	Yes [2]	GPIO
GPIO8 Module				
[11:0]	I/O	gpio8_[235:224]	Yes [2]	GPIO
[31:12]	I	gpio8_[255:236]		GPIO (inputs only)

(2) Only when the PER power domain is active

(3) The GPIO channel provides additional internal functionality (see the Comments column), besides its general-purpose I/O capabilities, when it is not connected to a pad of the device. For more information about pad configuration and multiplexing, see Section 18.4.8, *Pad Functional Multiplexing and Configuration*, in Chapter 18, *Control Module*.

A.11 Initialization

A.11.1 Power Connections

Table A-31 describes the device power balls. The highlighted balls are not used and not in OMAP

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Table A-31. Power Balls

Voltage Ball Name	Power Supplied OMAP Internal Modules / Peripherals
vdd_core	OMAP subsystems/modules supplied in the CORE voltage domain
vdd_mpu	• MPU subsystem
vdd_mm	• IVA subsystem • DSP subsystem • GPU subsystem
vdda_ldo_emu_wkup	• Wakeup • Emulation subsystem
vddq_ddr_ch1	EMIF channel 1 DQ I/Os (OMAP side only)
vddq_ddr_ch2	EMIF channel 2 DQ I/Os (OMAP side only)
vddq_vref_ddrch1	Supplies VDDQ_VREF generator for EMIF channel 1
vddq_vref_ddrch2	Supplies VDDQ_VREF generator for EMIF channel 2
vddca_lpddr2ch1	EMIF channel 1 CA I/Os (OMAP side only)
vddca_lpddr2ch2	EMIF channel 2 CA I/Os (OMAP side only)
vddca_vref_lpddr2ch1	Supplies VDDCA_VREF generator for EMIF channel 1
vddca_vref_lpddr2ch2	Supplies VDDCA_VREF generator for EMIF channel 2
vdds_hsic	USBB1, USBB2, USBB3 HSIC I/Os
vdda_dsiporta	DSI port A lanes (dual voltage I/Os)
vdda_dsiportc	DSI port C lanes (dual voltage I/Os)
vdda_hdmi	HDMI dual voltage I/Os
vdda_csiporta	CSI port A lanes (dual voltage I/Os)
vdda_csiportb	CSI port B lanes (dual voltage I/Os)
vdda_csiportc	CSI port C lanes (dual voltage I/Os)
vdda_dpll_mm_l4per	Analog power supply for the DPLL_IVA and DPLL_PER
vdda_dpll_mpu	Analog power supply or the DPLL_MPU
vdda_dpll_core_emu_abe	Analog power supply fot the DPLL_CORE, DPLL_DEBUGSS, and DPLL_ABE
vdda_dpll_hdmi	Analog power supply for the DPLL_HDMI
vdda_ldo_mpu	Analog power supply for the OMAP internal MPU LDOs
vdda_ldo_core	Analog power supply for the OMAP internal CORE LDOs
vdda_ldo_mm	Analog power supply for the OMAP internal MM LDOs
vdda_vbgap_core	Analog power supply for the OMAP BANDGAPTS_CORE
vdda_usbhs33	Analog power supplies for the high-speed USB I/Os
vdds_usbhs18	Analog power supplies for the high-speed USB I/Os
vdda_usbss18	Analog power supply for SuperSpeed USB I/Os
vdda_sata	Analog power supply for SATA I/Os
vdds_sdcard	MMC1 module I/Os (SD Card I/Os)
vdds_bank2	Bank of I/Os: HSI1, UART1 (dual voltage)
vdds_bank4	Bank of I/Os: HSI2, UART2 (dual voltage)
vdds_bank5	Bank of I/Os: TIMER9, TIMER10, DSIPORT B, DSIPORT C I/Os (dual voltage)
vdds_bank8	Bank of I/Os: MCSPI2, I2C4 (dual voltage)
vdds_bank9	Bank of I/Os: RFBI, GPIO6 (dual voltage)
vdds_bank10	Bank of I/Os: TCTRL, TIMER5, TIMER6, TIMER8, TIMER11, I2C3, GPIO8 (dual voltage)
vdds_bank11	Bank of I/Os: ABE clocks, MCBSP2, MCPDM (dual voltage)
vdds_bank12	Bank of I/Os: DMIC (dual voltage)
vdds_bank15	Bank of I/Os: MMC3 module I/Os -(WLSDIO dual voltage I/Os)
vdds_bank16	Bank of I/Os: UART5, I2C2 (dual voltage)
vdds_bank18	Bank of I/Os: MCSPI1, I2C5 (dual voltage)
vdds_bank21	Bank of I/Os: UART6, UART3 (dual voltage)

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Table A-31. Power Balls (continued)

Voltage Ball Name	Power Supplied OMAP Internal Modules / Peripherals
vdds_bank23	Bank of I/Os: JTAG®
vdds_bank24	Bank of I/Os: System interface
vdds_bank25	Bank of I/Os: System interface
vdds_bank26	Bank of I/Os: System interface, SmartReflex™PMIC I^2C, I2C1 PMIC interface (dual voltage)
vdds_osc	Fref XTAL oscillator (system interface I/Os)
vdda_slicer	Fref slicer oscillator (system interface I/Os)
vdds_emmc	MMC2 module I/Os (eMMC I/Os)

The OMAP5432 package does not provide any feedthrough balls.

A.11.2 Clock and Reset

Table A-32 lists the mapping for the OMAP clock input sources. Table A-33 lists the system clock source selection through sys_boot pins. The configurations that are not supported in OMAP5432 are highlighted with orange.

Table A-32. Mapping for Input Sources

Input Source	Mapping	Frequency Range/List	Type
Internal oscillator	fref_xtal_in/fref_xtal_out	12, 16.8, or 19.2 MHz	Crystal connection pins
External HS clock	fref_slicer_in	12, 16.8, 19.2, 26, or 38.4 MHz	Sine or square single ended
External 32k clock	sys_32k	32.768 kHz (nom.)	Square
Audio-management IC companion	abe_clks	19.2 MHz	Square

Table A-33. System Clock Selection Summary

sys_boot[5:4]	SYS_CLK Source	Oscillator Mode	Slicer Mode	fref_clk_ioreq Mode
0b00	fref_xtal_in	Active	Power down	Input
0b01 (1)	fref_xtal_in	Bypass	Power down	Output
0b10	fref_slicer_in	Power down	Active	Output
0b11	fref_slicer_in	Power down	Bypass	Output

(1) In the oscillator bypass case, fref_xtal_out pin is left unconnected

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Glossary

PRELIMINARY

1

1MS— One milisecond

2

2D— Two Dimensional

3

3A— AF + AE + AWB

3D— Three Dimensional

8

8B— 8 bits

A

A/D— Analog to Digital Converter

ABB— Adaptive Body Bias

ABBLDO— Adaptive Body Bias Low Drop Out

ABE— Audio Back End

ACB— ac–bias frequency

ACBI— ac–bias line transitions per interrupt

ACE— ASIC Compiler Environment.

ACK— Acknowledge

ADC— Analog–to–Digital Converter/Conversion.

ADMA— Audio DMA

ADPLL— All Digital Phase Locked Loop. A closed loop frequency control system whose function is based on the phase–sensitive detection of the phase difference between the input signal and the output signal of the controlled oscillator (CO).

ADPLLLJ— All Digital Phase-Locked Loop Low-Jitter

AE— Audio Engine. The AESS own processor.

AES— Advanced Encryption Standard

AESS— Audio Engine Subsystem

AEW— Auto Exposure and Auto White Balance

AF— Auto Focus

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AFE— Analog Front End

AHB— Advanced High-performance Bus

AHB-AP— Advanced High-performance Bus - Access Port

AHCI— Advanced Host Controller Interface

ALE— Address Latch Enable

AMBA— Advanced Micro-Controller Bus Architecture

AMMU— Attribute Memory Management Unit

ANSI— American National Standards Institute

AP— Address Protection

APB— Advanced Peripheral Bus

APB-AP— Advanced Peripheral Bus - Access Port

APE— Application Engine

API— Application Programming Interface

AR— Automatic Reload

ARGB— Alpha Red Green Blue

ARM— Advanced RISC Machine

ASCII— American Standard Code for Information Interchange

ASIC— Application–Specific Integrated Circuit. A chip built for a particularapplication. In the context of this document, this refers to the FPGA that resides on the EVM board.

ASP— Application–Specific Peripheral

ATA— Interface standard for the connection of storage devices (Advanced Technology Attachment)

ATAPI— ATA Packet Interface

ATB— AMBA Advanced Trace Bus

ATC— Audio Traffic Controller

AVS— Adaptive Voltage Scaling

AWB— Auto White Balance

AXI— Adavced eXtensible Interface

B

B— Byte, 8 bits

BAYER— Bayer Filter mosaic. A color filter array (CFA) for arranging RGB color filters on a square grid of photosensors.

BB— Bus Busy

BBM— BITSTREAM Buffer Management

BCD— Binary–Coded Decimal.

BCH— Bose-ChaudhurI-Hocquenghem

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BE— Big Endian.

BFSW— Buffer Switch

BGA— Ball Grid Array

BGAP— Band Gap

BIOS— Built–In Operating System

BIST— Built–In Self–Test

BIU— Bus Interface Unit

BL— Buffer Logic

BNC— British Naval Connector, Bayonet Nut Connector, or Bayonet Neill Concelman

BOF— Beginning of Frame

BPP— Bits Per Pixel

BS— Block Synchronization

BSC— Boundary Scan Chain

BSMEM— Bit Stream Memory

BTA— Bus Turn Around

BTE— Burst Translation Engine

BW— Band Width

BYS— Bayer Scaler

Bluetooth— A short–range radio technology aimed at simplifying communications among network devices and betweendevices and the Internet. It also aims to simplify data synchronizationbetween network devices and other computers.

C

C2C— Chip-to-Chip

CABAC— Context-Adaptive Binary Arithmetic Coding

CALC3— Transform and Quantization Calculation Engine

CAS— Column Address Strobe

CAVLC— Context-Adaptive Variable Length Coder

CB— Copy Back

CBP— Coded Block Pattern

CBUFF— Circular Buffer

CCC— Command Completion Coalescing feature

CCCR— Card Common Control Registers (SDIO)

CCP— Compact Camera Port

CDP— Coprocessor Data Operation

CDR— Clock Data Recovery

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CE— Chip Enable

CEA-861-D— HDMI 1.3 video standart. It defines the video timing requirements, discovery structures, and data transfer structure.

CEC— Consumer Electronics Control

CFA— Color Filter Array

CFI— Common Flash Interface device

CH— Configuration Header. To use different settings than ROM Code defaults, i.e. clock frequencies, SDRAM/DDRAM settings, GPMC settings if the customer wants.

CID— Card Identification Number

CIR— Consumer Infra Red

CL— Command List

CLB— Command List Base Address

CLE— Command Latch Enable

CLK— Clock

CLO— Command List Override feature

CLUT— Color Look-Up Table

CM— Clock Management

CMEM— Coefficient Memory (also referred as COEFF)

CMOS— Complimentary Metal Oxide Semiconductor

CO— Controlled Oscillator

CODEC— Coder/Decoder or Compression/Decompression. A device that codes in one direction of transmission and decodes in another direction of transmission.

COMINIT— An OOB Signal Sequence generated by physical layer of the attached SATA device as part of the SATA protocol

COMRESET— An OOB Signal Sequence generated by physical layer of the SATA host as part of the SATA protocol

COMWAKE— COMWAKE OOB signal defined in SATA protocol

CP15— Coprocessor 15. This coprocessor controls the operation andconfiguration of the TI925T.

CP7— USB3.0 CP7 transmit pattern

CP8— USB3.0 CP8 transmit pattern

CPFROM— Customer Programable eFuse ROM

CPI— Camera Parallel Interface

CPR— Clock, Power, Reset

CPS— Cell Search Platform

CPSR— Current Program Status Register

CPU— Central Processing Unit.

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CRC— Cyclic Redundancy Check

CS— Chip–Select

CSI— Camera Serial Interface

CSL— Chip Support Library

CSW— Control Space Width

CSWR— Closed switch retention

CTM— Counter-Timer Module

CTRL— Control

CTS— Clear to Send

CTT— Clock Tree Tool

ConnID— Connection Identifier.An Initiator Module Identifier. A ConnID is transmitted in-band with the request and is for error logging mechanism.

D

D2D— Die-to-Die

D2H— Device to Host transfer of a FIS

DBB— Digital Baseband

DBI— Display Buffer Interface

DC— Direct Current

DCC— Duty Cycle Correction Circuit

DCD— Data Carrier Detect

DCO— Digitally Controlled Oscillator

DCS— Display Command Set

DCT— Discrete Cosine Transform.

DDC— Display Data Channel

DDMA— DSP Subsystem Direct Memory Access module

DDR— Double Data Rate

DE— Data Enable

DES— Data Encryption Standard.

DFF— Digital Flip-Flop

DFT— Design For Test

DI— Data In

DISPC— Display Controller

DL— Data Lenght

DLB— Data Loopback.

DLL— Delay-Locked Loop

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DMA— Direct Memory Access.

DMC— Data Memory Controller

DMEM— Data Memory

DMIC— Digital Microphone Controller

DMM— Dynamic Memory Management

DMT— Display Monitor Timing

DO— Data Out

DPC— Defect Pixel Correction

DPCM— Differential Pulse Code Modulation

DPI— Display Parallel Interface

DPLL— Digital Phase–Locked Loop. Digital implementation of PLL.

DPS— Digital Power Switching

DRD— Dual-Role Device (a type of OTG USB device)

DRDY— Data Ready

DRM— Digital Rights Management

DRQ— Data Transfer Requested flag in the SATA / ATA task file

DSI— Display Serial Interface

DSP— Digital Signal Processor.

DSR— Data Set Ready

DSS— Display Sub-System. Also DISS

DT— Data Type

DTBC— Data Buffer Controller

DTC— Debug and Trace Controller

DTCM— Data Tightly Coupled Memory

DTR— Data Transmit Ready

DVFS— Dynamic Voltage and Frequency Scaling

DVI— Digital Video Interface

DWORD— Double WORD (32-bit sized portion of data)

E

EA— Enumeration Address

EAV— End of Active Video

ECC— Error Checking and Correction. Also Error Correction Code.

ECD3— Entropy Coder/Decoder

ED— Endpoint Descriptor

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EFUSE— Electrical Fuse. A one-time programmable memory location usually set at the factory

EHCI— Enhanced Host Controller Interface

EMC— External Memory Controller

EMI— Electromagneric interference

EMIF— External Memory Interface

EOB— End of Block

EOF— End of Frame

EOL— End of Line

EOT— End of Transfer

EP— Entry Point

ES— Erase Status

F

FAT— File Allocation Table

FB— Received FISes base address

FC— Frame Counter

FCLK— Functional Clock

FCS— Frame Check Sequence

FD— Face Detect

FE— Framing Error.

FEC— Frame End Code

FF— Flip-Flop

FIFO— First In First Out.

FIQ— Fast Interrupt Request. See ISR.

FIR— Fast Infrared

FIS— Frame Information Structure defined in SATA standard as user payload of a frame

FM— Frequency Modulate

FROM— eFuse ROM

FS— Full-Speed

FSC— Frame Start Code. Also Frame Start Count.

FSM— Finite State Machine.

FSR— Fault Status Register

FV— Focus Value

FW— Firewall

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G

GBC— Green Balance Correction

GDP— Generic Dot Product

GFX— Graphics

GHB— Global History Buffer

GP— General-purpose

GPIO— Genreal Purpose Input Output

GPMC— General Purpose Memory Controller

GPU— Graphics-processing unit

GSM— Global System for Mobile Communications

GZ— Ground Zero

H

H.263— Video Codec Standart

H.264— Video Codec Standart

H/W— Hardware

H2D— Host to Device transfer of a FIS

H3A— Hardware 3A statistics engine. See 3A.

HAL— Hardware Abstraction Layer

HBA— Host bus adapter

HBP— Horizontal Back Porch

HC— Host Controller

HCI— Host Controller Interface

HD— High Definition

HDCP— High-bandwidth Digital Content Protection

HDD— Hard-disk drive

HDMI— High-Definition Multimedia Interface

HDQ— Single-wire communication interface

HDTV— High-Definition Television

HFP— Horizontal Front Porch

HLOS— High-Level Operating System

HNP— Host Negotiation Protocol (OTG feature)

HPF— High-Pass Filter

HPI— Host Port Interface

HS— High-Speed

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HSE— Horizontal Sync End

HSI— High Speed Synchronous Serial Interface

HSS— Horizontal Sync Start

HSSCLL— High-Speed Serial Control Channel

HSW— Horizontal Synchronization Pulse Width

HSYNC— Horizontal Synchronization.

HW— Hardware

HWA— Hardware Accelerators.

HWOBS— Hardware Observability

HWSEQ— Hardware Sequencer

I

I/F— Interface

I/O— Input/Output

I2C— Inter–Integrated Circuit.

I2S— Inter–IC Sound.

IA— Identifier Address

ICE— In–Circuit Emulation

ICEPICK— Generic TAP for emulation control

ICLK— Interface Clock

ICONT— Imaging Controller

ICR— Intersystem Communication Registers

ID— Identification

IDCT— Inverse Discrete Cosine Transform. See DCT.

ILF3— Improved Loop Filter engine

IM— Initiator Module. A module is an initiator whenever it is able to initiate read and write requests to the chip interconnect (typically: processors , DMA...).

IME3— Improved Motion Estimation engine

IMX— Image Extension coprocessor

INT— Interrupt .

INTC— Interrupt Controller

IP— Intellectual Property

IPC— Interprocessor Communication. (also referred to as “mailbox” on occasion)

IPE3— Intra Prediction Estimation engine

IPIPE— Image Pipe

IPIPEIF— Image Pipe Interface

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IPU— Image-processing unit

IQ— Inverse Quantization

IR— Incremental Redundancy Buffer

IRQ— Interrupt Request.

ISA— Instruction Set Architecture

ISIF— Image Sensor Interface

ISO— Isochronous.

ISP— Image Signal Processor

ISR— Interrupt Service Routine.

ISS— Image SubSystem

IST— Interrupt Service Thread.

ITCM— Instruction Tightly Coupled Memory

IV— Initialization Vector

IVA— Image and Video Accelerator

IVA-HD— High Definition Image and Video Accelerator

IrDA— Infrared Data Association.

J

JEDEC— Joint Electronic Devices Engineering Council

JPEG— Joint Photographics Experts Group

JTAG— Joint Test Action Group.

K

KiB— Kibibyte, 1024 bytes

KBD— Keyboard

Kbps— Kilobits per second

L

L1— Level 1 cache/memory

L2— Level 2 cache/memory

L3— First level of interconnect in OMAP platform

L4— Seconf level of interconnect in OMAP platform

LA— Logical Address

LAN— Local Area Network

LANGID— 16-bit Language ID

LBA— Logical Block Addressing

LC— Logical Channel

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LCD— Liquid Crystal Display.

LCM— Logical Channel to Memory

LCh— Logical DMA Channel. Also LCH

LD— Lens Distortion

LDC— Load (from memory) to Coprocessor

LDC2— Lens Distortion Correction

LDM— Load Multiple

LDO— Low Dropout

LE— Little Endian.

LEC— Line End Code

LED— Light Emitting Diode.

LF— Loop Filter

LFN— Long File Name

LFPS— Low Frequency Periodic Signaling defined in USB 3.0 SuperSpeed standard

LFSR— Linear-Feedback Shift Register

LH— Local Host

LINK— Link Layer Device

LISA— Local Interconnect and Synchronization Agent

LLC— Link Layer Control

LLP— Low-Level Protocol

LP— Low-Power, operation mode for PHY

LPCM— Linear Pulse Code Modulation

LPDDR— Low Power Double Data Rate

LPF— Loop Filter

LPM— Low Power Mode (also refered as LPMODE)

LPP— Lines Per Panel

LS— Low-Speed

LSB— Least Significant Bit

LSC— Line Start Code

LSE— IVA Load and Store Engine

LSM— LISA Section Manager

LSR— Linear Shift Register

LSW— Least Significant Word

LUT— Look-up Table

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M

M2— Micro Memory

MAC— Message Authentication Code

MiB— Mebibyte, 1024 KiB

MBAFF— MB-Level Adaptive Frame/Field

MBR— Master Boot Record

MC3— Motion Compensation Engine

MCSPI— Multichannel Serial Port Interface

MCU— Microcontroller Unit. Refers to the MPU.

ME— Motion Estimation

MEMIF— Memory Interface

MIF— Memory InterFace

MIPI— Mobile Industry Processor Interface

MIR— Medium Infrared

MJPEG— Motion JPEG

MMC— Multimedia Card

MMC/SD— Multimedia Card/Secure Data

MMR— Memory Mapped Register

MMU— Memory Management Unit.

MP3— MPEG Layer 3.

MPEG— Motion Pictures Expert Group.

MPEG1— The first MPEG compression scheme specification.

MPU— Microprocessor Unit.

MS— Memory Stick

MSB— Most Significant Bit

MSGIF— Message Interface

MUX— Multiplex/Multiplexer

Mb— Megabit

Mbps— Mega bits per second

McBSP— Multichannel Buffered Serial Port.

Modem— Modulator Demodulator

MuxMode— 3 bits field of the PIN Control register field which enables to change the mode. Mode programming is assumed by software and selects a function on the device external interface.

N

N/A— Not Applicable

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NAC— Network Access Control

NAK— Not Acknowledged

NAND— NAND Flash memory.

NC— Not Connected

NCQ— Native Command Queuing feature of SATA

NIU— Network Interface Unit

NMI— Nonmaskable Interrupt. An interrupt that can be neither masked nor disabled.

NOP— No OPeration (DSP/CPU instruction)

NOR— A type of flash memory

NRZI— Non-Return-to-Zero Inverted

NSF— Noise Filter

NVB— Number of Valid Bytes

NVIC— Nested Vectored Interrupt Controller

NVM— Non-volatile Memory

O

OCM— On-chip Memory

OCP— Open–Core Protocol

OCPI— Open–Core Protocol Interface

OE— Output Enable

OHCI— Open Host Controller Interface. This is an industry standard USB Host Controller Interface.

OMAP— Open Multimedia Application Platform

OOB— Out of Band signaling

OPP— Operating Performance Point

OS— Operating System

OSI— (OSI model) Open Systems Interconnection Basic Reference Model

OTG— On-The-Go (USB 2.0 specification)

P

PA— Program Address

PATA— Parallel-ATA

PB— Peripheral Bus. Refers to the TIPB.

PBIAS— PMOS Bias transistor to provide the bias voltage to extended drain IOs

PC— Program Counter

PCB— Printed Circuit Board

PCI— Peripheral Component Interconnect.

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PCLK— Pixel Clock

PCM— Pulse Code Modulation.

PCS— Personal Communication System.

PD— Program Data

PDC— Power-down Controller

PDM— Pulse Density Modulation

PE— Parity Error

PF— Packet Footer

PFPW— Prefetch and Prewrite posting engine

PH— Packet Header

PHY— Physical Layer Device

PI— Pixel Interpolation

PID— Protocol Identifier. The PID register is used in Windows CE mode only.

PIO— A programmed input/output transfer supported by IDE devices

PIPE3— A parallel data interface which connects USB OTG SS Controller with the USB3 PHY wrapper

PKA— Public Key Accelerator

PLD— Programmable Logic Devices

PLL— Phase–Locked Loop.

PM— Programming Model

PMA— Physical Media Attachment sublayer

PMC— Program Memory Controller

PMFW— Power Management FrameWork

PMIC— Power management Integrated Circuit

PMP— Power Management Port

PMU— Performance Monitoring Unit

POR— Power–On Reset

PPA— Primary Protected Application.

PPC— Palm–size PC

PPI— Physical Layer Protocol Interface

PPL— Pixels per Line

PRCM— Power, Reset, Clock Management module

PRD— Physical Region Descriptor

PRM— Power and Reset manager

PRT— PRD Table

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PS— Packet Start

PSC— Prescaler Counter

PSS— Program Suspend Status

PT— Packet Type

PTI— Parallel Trace Interface

PTV— Prescale Clock Timer Value. Sets the value of the divisor used in scaling the clock.

PU/PD— Pull-Up / Pull-Down

PVT— Process, Voltage and Temperature; i.e. PVT dispertion

PWL— Pulse Width Light (modulator). A 4096–bit randomsequence generator that provides control of the LCD backlighting and keypad.

PWM— Pulse Width Modulation

PWR— Power

Q

QIQ— Quantization and Inverse Quantization

QM— Quantizer Matrix

QMEM— Quantizer Memory

QMR— Quantizer Matrix Reciprocal

QP— Quantization Parameter

QVGA— Quarter Video Graphics Array. One–fourth the resolution of VGA.

R

R/W— Read/Write. Also RW.

R5— Release 5 of 3GPP specifications on IMS and HSDPA standards

R6— Release 6 of 3GPP specifications on Wireless LAN networks, HSUPA, MBMS and enhancements to IMS standards

RAM— Random Access Memory.Fast-access but volatile memory type.

RCA— Relative Card Address

RDR— Receive Data Register

RE— Read Enable

REQ— Request

RF— Radio Frequency

RFB— Remote Frame Buffer

RFBI— Remote Frame Buffer Interface

RFF— Retention Flip-Flop

RGB— Red Green Blue

RGBA— Red Green Blue Alpha

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RI— Ring Indicator

RM— Reed-Muller code

RNG— Random Number Generator

RO— Read Only

ROM— Read Only Memory. A semiconductor storage element containing permanent data that cannot be changed.

RSS— Reset System Simulator

RST— Reset

RT— Real–Time

RTA— Retention Till Access

RTL— Register Transfert Level

RTOS— Real–Time Operating System

RTS— Request to Send

RV— RealVideo (codec)

RVLC— Reversible Variable Length Coder

RX— Receive/Receiver

RXD— Receive Data

RXN— PHY differential receiver (de-serializer) negative line

RXP— PHY differential receiver (de-serializer) positive line

S

S/PDIF— Sony/Philips Digital Interface

S/W— Software

SAM— Signal Amplitude Modulation

SAR— Save and Restore. Hardware context saving for power saving.

SATA— Serial ATA

SATASS— SATA subsystem

SAV— Start of Active Video

SB— Silicon Backplane (Trade Mark)

SBC— Stream Buffer Controller

SBH— Synchronization Box Handler

SCL— Serial Clock. Programmable serial clock used in the I2C interface. Also SCLK.

SCM— System Control Module

SCP— Serial Configuration Port

SCR— SDIO Configuration Registers

SCRM— System Clock and Reset Manager

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SCTM— System Counter Timer Module

SCU— Snoop Control Unit

SD— Secure Digital card. A non-volatile memory card.

SDA— Serial Data. Serial data bus in the I2C interface.

SDIO— Secure Digital Input/Output

SDMA— System Direct Memory Access module

SDR— Single Data Rate

SDRAM— Synchronous Dynamic Random Access Memory

SDRC— SDRAM Controller.

SFL— Subframe Length

SGX— Accronym for Grafics Accelerator (GFX in ES1.0)

SIMCOP— Still image coprocessor

SIMD— Single Instruction-Stream, Multiple Data-Stream

SIR— Slow Infrared

SL2— Shared Level 2 (memory/interface)

SL2IF— Shared L2 Interface

SLC— Single Level Cell devices

SLM— Static Leakage Management

SLVS— Scalable Low Voltage Signaling

SMC— Shared Message Channel

SMEM— Sample Memory

SMIA— Standard Mobile Imaging Architecture

SMP— Symmetric Multiprocessor Platform

SMPS— Switch Mode Power Supply

SMSET— Software Message and System Event Trace module

SN— Slave NIU

SNR— Signal-to-Noise Ratio

SOC— System-On-a-Chip

SOF— Start Of Frame

SP— Serial Port or Small Page

SPC— Serial Port Control

SPI— Serial Port Interface. A signaling protocol for exchanging serial data.

SR— SmartReflex

SR3-APG— SmartReflex3 Automatic Power Gating

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SRAM— Static Random Access Memory

SRC— Sample Rate Conversion

SRG— Sample Rate Generator

SRMD— Single Request, Multiple Data

SRP— Session Request Protocol (OTG feature)

SS— Subsystem

SSC— Spread Spectrum Clocking

SSD— Solid State Drive

SSI— Serial Synchronous Interface

SSM— Security State Machine

ST— Start Timer

STC— Store from Coprocessor (to memory) or System Time Clock, which is the master clock in an MPEG2 encoder or decoder system.

STM— Synchronous Transfer Mode or Store Multiple.

STN— Super–Twist Nematic. A technique for improving LCD display screens by twisting light rays.

SW— Software

SWI— Software Interrupt

SXGA— Super eXtended Graphics Array

SYSC— System Control Module

SYSCTRL— IVA System Control module

SmartReflex— Dynamic voltage sensing module that generates the voltage error signal proportional to the difference in desired voltage and the current voltage

T

TA— Target Agent

TAP— Test Access Port

TC— Traffic Controller. Allows asynchronous operation among the external memory interface, the MPU, and the DSP.

TCK— Test Clock

TCM— Tightly Coupled Memory

TCTRL— Timing Control module

TD— Transfer Descriptor

TDI— Test Data Input

TDM— Time Division Multiplex/Multiplexing

TDO— Test Data Output

TFT— Thin Film Transistor. A type of LCD flat panel display screen in which each pixel is controlled by one to four transistors.

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TI— Texas Instruments

TILER— Tiling Isometric Lightweight Engine for Rotation

TL— Transmission Line

TLB— Translation Lookaside Buffer. A cache that contains entries for virtual–to–physical address translation and access permission checking.

TLL— Transceiver Less Link. This is logic which allows the user to connect two USB transceiver interfaces together directly without the use of differential transceivers.

TM— Target Module. A target module cannot generate read/write requests to the chip interconnects, but respond to these requests. However it may generate interrupts or DMA request to the system (typically: peripherals, memory controllers).

TMDS— Transition Minimized Differential Signaling. A technology for transmitting high-speed serial data and is used by the DVI and HDMI video interfaces.

TMS— Test Mode Select

TOC— Table of Contents

TP— Tiny Page

TRM— Technical Reference Manual

TRST— Test Reset

TRX— USB Tranceiver. The USB analog driver/receiver.

TS— Transmission Start

TSHUT— Temperature Shutdown.

TTB— Translation Table Base. It points to the base of a table in physical memory that contains section and page table descriptors.

TTH— Translation Table Hierarchy

TTL— Transistor Transistor Logic

TWL— Table Walking Logic

TX— Transmit//Transmitter

TXD— Transmit Data

TXN— PHY differential transmitter (serializer) negative line

TXP— PHY differential transmitter (serializer) positive line

U

UART— Universal Asynchronous Receiver/Transmitter. Another name for the asynchronous serial port.

UE— Unrecoverable Error

UHS— Definition of SD cards with higher frequency

UI— Unit Intervals

ULPI— UTMI+ Low Pin Interface (12-pin interface standard for connecting USB core logic to a USB transceiver)

ULPM— Ultra Low Power Mode

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ULPS— Ultra Low Power State

UMC— Unified Memory Controller

USB— Universal Serial Bus. An external bus standard that supports data transfer rates of 12M bps (12 million bits per second). A single USB port can be used to connect up to 127 peripheral devices.

USSE— Universal Scalable Shader Engine

UTMI— USB 2.0 Transceiver Macrocell Interface

V

VA— Virtual Address

VBP— Vertical Back Porch

VC— Virtual Channel

VC-1— Video Codec Standart

VDMA— Video Direct Memory Access module

VESA— Video Electronics Standards Association

VFP— Vertical Front Porch

VGA— Video Graphics Array. An industry standard for video cards.

VLC— Variable Length Decoder

VLCD— Variable Length Coding and Decoding coprocessor

VLCDJ— Variable-Length Coder/Decoder for JPEG

VLD— Variable Length Coder

VLIW— Very Long Instruction Word

VMODE— Bi-level voltage control interface

VOLCON— Voltage Controller

VP— Video Port

VS— Vertical Synchronization

VSE— Vertical Sync End

VSS— Vertical Sync Start

VSW— Vertical Synchronization Pulse Width

VSYNC— Vertical Synchronization. A bidirectional vertical timing signal occurring once per frame with a pulse–width defined as an integral number of lines (half–lines for interlaced mode). Also VS.

W

WB— Write Buffer

WC— Word Count

WD— Watchdog. A timer that requires the user program or OS periodically write to the count register before the counter underflows and triggers a reset.

WDT— Watchdog Timer. See WD.

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WE— Write Enable

WFI— Wait For Interrupt

WIR— Wait In Reset

WLAN— Wireless Local Area Network

WNP— Write Non-Posted

WP— Write Protect

WT— Write Through

WUGEN— Wake-Up Generator

Word16— 16 bits word

X

XIP— eXecution In Place

Y

YUV— Luminance-Bandwidth-Chrominance

e

eMMC— Embedded Multimedia Card

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